Low-voltage direct current distribution grids : main AC/DC converter, power quality, and protections analysis

César Augusto Slongo

université de BORDEAUX

THÈSE PRÉSENTÉE

POUR OBTENIR LE GRADE DE

DOCTEUR DE L'UNIVERSITÉ DE BORDEAUX

ÉCOLE DOCTORALE DES SCIENCES PHYSIQUES ET DE L'INGÉNIEUR

SPÉCIALITÉ ÉLECTRONIQUE

Par César Augusto SLONGO

Titre

Réseaux de distribution à courant continu/basse tension : analyse du convertisseur CA/CC principal, de la qualité de l'énergie et des protections

Low-voltage direct current distribution grids: main AC/DC converter, power quality, and protections analysis

Sous la direction de : Octavian CUREA

Soutenue le 02 octobre 2023

Membres du jury :

Mme SECHILARIU, Manuela	Professeure	Univ. de Tech. de Compiègne	Pres. du Jury
M. QUEVAL, Loïc,	Prof. Assoc.	Université Paris-Saclay	Rapporteur
M. MARTINEZ De ALEGRIA, Iñigo	Prof. Assist.	UPV/EHU	Rapporteur
M. DAKYO, Brayima	Professeur	Université du Havre	Examinateur
M. CUREA, Octavian	Professeur	ESTIA Inst. of Techn.	Directeur

Membres invités :

M. LLARIA LEAL, Alvaro	Prof. Assist.	ESTIA Inst. of Techn.	Co-encadrant
M. YANG, Xavier	Docteur	EDF R&D	Invité

Titre :

Réseaux de distribution à courant continu/basse tension : analyse du convertisseur CA/CC principal, de la qualité de l'énergie et des protections

Résumé :

Au cours des dernières décennies, l'utilisation du courant continu est devenue un moteur potentiel pour l'intégration des sources d'énergie renouvelables et des équipements de stockage dans les réseaux de distribution, dans le but de concevoir un modèle énergétique plus efficace. Il est possible de trouver différents exemples mis en place dans cette thématique à travers le monde, avec un nombre important de projets en cours de développement en Asie et en Europe. Les avantages associés à l'utilisation des systèmes de distribution en courant continu vont de l'augmentation de l'efficacité énergétique grâce à la mutualisation des convertisseurs de puissance, jusqu'à l'amélioration de la contrôlabilité et de la fiabilité en utilisant des architectures de réseaux interconnectés. Néanmoins, il est possible d'observer que le domaine des systèmes à courant continu basse tension manque encore de normes, notamment en ce qui concerne les méthodes d'évaluation de la qualité de l'énergie et les schémas de protection. Les indicateurs permettant d'évaluer différents phénomènes liés à la qualité de l'énergie en courant continu sont encore à définir. En plus de cela, le domaine de la protection en courant continu fait face à des nouveaux défis, comme la protection contre le choc électrique et l'application de la sélectivité dans un environnement avec une faible puissance de court-circuit. Dans ce contexte, cette thèse présente trois objectifs majeurs. Le premier consiste à identifier, concevoir et implémenter une topologie de convertisseur CA/CC, qui puisse être utilisée pour déployer un système de distribution. Un sujet important étudié dans ce travail concerne cette topologie, ainsi que ses caractéristiques de gestion des défauts. Le deuxième objectif est de concevoir un schéma de protection sélective. Enfin, le dernier objectif est d'identifier les phénomènes liés à la qualité de l'énergie en courant continu et comment le comportement du convertisseur principal, en termes de composants et de contrôle, impacte ces phénomènes. D'un point de vue global, ces travaux peuvent contribuer à fournir des informations complémentaires aux études de normalisation en cours, qui sont cruciales pour le développement des futurs systèmes de distribution à courant continu. De ce fait, cette thèse apporte quatre contributions scientifiques principales : la conception et réalisation d'un convertisseur CA/CC incluant une isolation galvanique moyenne-fréquence et des interrupteurs de puissance à base de transistors en Carbure de Silicium ; le développement d'une méthodologie permettant le dimensionnement des équipements de protection contre court-circuit dans une installation électrique à courant continu basse tension, à travers les techniques de limitation de courant et en employant des disjoncteurs CC mécaniques et des fusibles CC ultra-rapides ; l'application des méthodes pour la détermination de l'impédance fréquentielle du convertisseur principal afin d'évaluer la propagation des perturbations spectrales ; la conception d'un système de contrôle dédié au convertisseur principal, qui permet de changer la dynamique de celui-ci en fonction d'une performance souhaitée face aux perturbations transitoires.

Mots clés :

Réseaux de distribution à courant continu/basse tension ; Electronique de puissance ; Protections ; Qualité de l'énergie.

Title :

Low-voltage direct current distribution grids: main AC/DC converter, power quality, and protections analysis

Abstract :

In recent decades, the use of direct current has become a potential driver for the integration of renewable energy sources and storage equipment with the aim of designing a more efficient power distribution model. It is possible to observe different ecosystems emerging in this field throughout the world, with many projects under development in Asia and Europe. The benefits associated with the use of DC distribution systems range from increased energy efficiency through the mutualization of power converters, to improved controllability and reliability through interconnected grid architectures. Nevertheless, it is possible to observe that the field around low voltage direct current systems still lacks standards, especially with regard to power quality assessment methods and protection schemes. The indicators making it possible to evaluate different phenomena related to power quality in direct current are still to be defined. In addition, the field of DC protection faces new challenges, such as protection against electric shock and the application of selectivity in an environment with low short-circuit power. In this context, this doctoral thesis has three main objectives. The first is to identify and design an AC/DC converter topology, which can be used to deploy a distribution system. An important aspect studied in this work concerns the topology of the converter is its fault handling characteristics. The second main objective is to design a selective protection scheme. Finally, the last objective is to identify the phenomena related to the quality of DC power and how the behavior of the main converter, in terms of components and control, impacts these phenomena. From a global perspective, this work can help inform ongoing standardization studies, which are crucial for the development of future DC distribution systems. This thesis brings four scientific contributions: the design and implementation of an AC/DC converter with medium-frequency galvanic isolation and power switches based on Silicon Carbide; the development of a methodology for the sizing of protection equipment against short-circuit in a low voltage direct current electrical installation, through current limitation techniques and using mechanical DC circuit breakers and ultra-fast DC fuses; the application of methods for determining the frequency impedance of the main converter for the evaluation of the propagation of spectral disturbances; the design of a control system for the main converter allowing the variation of its dynamics according to a desired performance to mitigate transient disturbances.

Keywords:

Low voltage direct current **(**LVDC) distribution grids; Power Electronics; Protections; Power quality.

ACKNOWLEDGEMENTS

Even if embarking in a PhD journey means to accept solitude in many steps of the way, in my perspective, when I look back, I find myself overwhelmed with joy from memories of the people who were by my side, without whom it would be impossible to reach the end of this adventure. My immeasurable gratitude towards those who were crucial presences in this part of my life can be divided in four groups.

At first, I would like to thank my supervisors, starting by my thesis main supervisor Octavian Curea. Thank you for the opportunity you gave me to work with you and your team, discovering the research world. Thank you also for all the time and expertise you shared with me through significant conversations, but always with a touch of humor. Then, I would like to thank my co-supervisor Alvaro Llaria who was always available to help me with my difficulties from all origins. Thank you as well for using all your brilliant proficiency in scientific writing to assist me during these three years. It was a real pleasure to work with you both. You have been real masters to me, inspiring me scientifically, professionally, and personally. I would like to thank two other members of our team, Zina Boussaada and Nesrine Boussaada, for all the companionship, conversations, advice, and plans which helped me significantly to reach my goal. Finally, from an academic point of view, I would like to thank Loïc Queval and Iñigo Martinez de Alegria, for accepting the important role of reviewer and for the valuable propositions for the improvements of the thesis manuscript. I would also like to thank Manuela Sechilariu and Brayima Dakyo for the time invested in the evaluation of this project, for sharing their knowledge with me, and for helping me progress with precise advice.

In a second place, I would like to thank the R4P team in SYSTEM Department of EDF R&D. Thank you everyone for the warm and hearty reception in the team, thank you also for the all the meaningful conversations around the coffee space, for the laughs and companionship, it really gave a deep sense to my life and to my path. More specifically, I would like to thank my team leaders Mathieu Caujolle and Justine Yuan for presenting me this sublime research subject and for all your support and precise advice at all times. Next, I dedicate a special thanks to all my co-supervisors from EDF, who invested their time to discuss with me and to teach me essential concepts and subjects: Geoffrey Auran and Boris Deneuville for all your help and expertise in the protection domain; Xavier Yang and Ludovic Bertin for all the support concerning the power quality, power electronics and electromagnetic compatibility domain; Kevin Lorenzo and Sarah Nasr for the exceptional guidance of the projects around DC Systems. Then, I would like to thank all the members of the team who were not directly involved in my PhD but found time anyway to help me when I needed the most, thank you Gaetan Villeret, Quentin Wohlschlegel and Michael Jubert. Finally, I would like to thank the best office mate I have ever had, Dumitru Mecineanu, for all the times you were there to discuss with me, to help me, or just to listen.

In a third place, I would like to thank all my friends and PhD colleges, life during these three years was a lot easier with you all in it. A special thanks to Maria Veizaga, Meriem Zanoun, Yara Daaboul, Frédéric Reymond-Laruina, Elsy El Sayegh, Youba Nait Belaid, Mohand Nait Belaid, Adama Arama, Yehya Rifai, Cesar Peinado Moraes, Humberto Carneiro de Sousa and Gustavo Corrêa Pereira. Each one of you has a significant contribution to my journey, thank you for being there and thank you for showing me the real meaning of friendship. Finally, I would like to thank my family in France, Gabriel Melo, Vanessa Câmara, Lucas Bezerra and Ana Beatriz Lima for all the unconditional support.

Lastly, but most importantly, I would like to thank my family. Thank you, my father, for listening to me and for all the powerful words you always said to me, making me move forward towards my goal. Thank you, my mother, for the kind-hearted care you gave me throughout my journey and for

sharing your scientific expertise with me. Thank you, my brother, for the indescribable syntony you helped me create between us and thank you for being my strength and discernment when I most needed. Thank you, my sister-in-law, for inspiring me with your sense of discipline and relentless dedication. Finally, thank you, my fiancée, for being the most incredible source of motivation, support, and courage I have ever found in my life. It would have been impossible to reach my goals without you all.

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LIST OF ABBREVIATIONS

μC – Microcontroller

AC – Alternating Current

ACB – Air Circuit Breaker

ADC – Analog-to-Digital Converter

CB – Circuit Breaker

DAB – Double Active Bridge

DC – Direct Current

DCy – Duty Cycle

DPS – Double Phase-Shift

DSO – Distribution System Operator

DSP – Digital and Signal Processor

EMC – Electromagnetic Compatibility

EMT – Electromagnetic Transient

EPS – Extended Phase-Shift

ESS – Energy Storage System

ETCB – Electronic Tripping Circuit Breaker

EV – Electric Vehicle

FC – Fuel Cell

FPGA – Field Programable Gate Array

GaN – Gallium Nitride

HCB – Hybrid Circuit Breaker

HV – High-Voltage

HVAC – High-Voltage Alternating Current

HVDC – High-Voltage Direct Current

IC- Interlink Converter

IGBT – Insulated Gate Bipolar Transistor

IMD – Insulation Monitoring Device

ITIC - Information Technology Industry Council

ITOC – Inverse Time Overcurrent

LCC – Line Commutated Converter

LV – Low-Voltage

LVAC – Low-Voltage Alternating Current

LVDC – Low-Voltage Direct Current

M – Modulation Index

MG - Microgrid

MMC – Modular Multilevel Converter

MOSFET – Metal-Oxide Semiconductor Field Effect Transistor

MOV – Metal-Oxide Varistor

MPPT – Maximum Power Point Tracking

MV – Medium-Voltage

MVDC – Medium-Voltage Direct Current

NLM – Nearest Level Modulation

NPC – Neutral Point Clamp

PCC – Point of Common Coupling

PD – Protection Device

PELV – Protected Extra-Low-Voltage

PFC – Power Factor Corrector

PI – Proportional-Integral

PLL – Phase Locked Loop

PQ – Power Quality

PS – Phase-Shifted

PTP – Point-To-Point

PV - Photovoltaic

PWM – Pulse Width Modulation

RCD – Residual Current Device

RDAB – Resonant Double Active Bridge

RDF – Ripple Distortion Factor

RES – Renewable Energy Source

RMS – Root Mean Squared

SAB – Single Active Bridge

SELV – Separated Extra-Low-Voltage

SG – Smart Grid

SiC – Silicon Carbide

SPS – Single Phase-Shifted

SPWM – Sinusoidal Pulse Width Modulation

SRC – Series Resistive Capacitive

SSCB – Solid State Circuit Breaker

SVM – Space Vector Modulation

TMCB – Thermomagnetic Circuit Breaker

TPS – Triple Phase-Shifted

TVS – Transient Voltage Suppressor

UFF – Ultra-Fast Fuse

VSC – Voltage Source Converter

WBG – Wide Band Gap

WT – Wind Turbine

ZCS – Zero Current Switching

ZOH – Zero-Order Holder

ZVS – Zero Voltage Switching

GENERAL INTRODUCTION

Systems responsible for distributing electricity around the world are facing new challenges, notably associated to the integration of Renewable Energy Sources (RES) and Energy Storage Systems (ESS) to the power grid. In fact, in a global context of climate change, which is deeply associated to carbon dioxide emission, a high presence of RES and ESS in the energy mix to increase local consumption may be crucial to contribute to the energy transition movement. In this scenario, Low-Voltage Direct Current (LVDC) distribution systems are rising in the last few years as a potential driver and enabler of the integration of these assets in the distribution grid [**SLO23b, DIA15, DIA16a, DIA16b**].

Since technologies like batteries, fuel-cells and photovoltaic panels are naturally interfaced by a LVDC grid, several AC/DC conversion steps can be avoided, which represents a global gain in terms of energy efficiency [**SEC14**]. In addition, it is also possible to observe a great increase in DC-compatible loads used in commercial and residential buildings, such as electric vehicles, electronic equipment, heat pumps, LED lighting, and others [**DIA15**]. Consequently, a DC grid would represent a natural choice to link DC consumption and DC generation. Consequently, the drive towards LVDC distribution systems may start in a consumption/local generation perspective and potentially evolve to public distribution system in the future.

For the reasons presented above, the field around LVDC distribution systems is gaining significant attention recently, in a way that different ecosystems are being created around the world, especially in Asia and Europe. Nonetheless, the LVDC domain for distribution grids still lacks maturity and still faces some challenges. Among them, one of the most relevant is the absence of specific standards, especially around power electronics, protection schemes and power quality. Selective protection strategies against short-circuit and electric shock should be further addressed, taking the low short-circuit power limitation of power electronics converter in consideration. In addition, indicators to evaluate steady-state and transient behavior of DC voltage and current linked to the definition of power quality (PQ) are yet to be defined.

This doctoral thesis is developed through an industrial partnership with the Paris-Saclay center of Research and Development of Electricité de France (EDF R&D), which is a global actor in the energy generation domain, and Enedis, which is the French Distribution System Operator. From the industrial perspective, either from the generation or distribution sides, it is important to understand what the possible advantages are of deploying a LVDC system compared to classic AC systems, in what scenarios and how it can be technically feasible. This thesis is mainly focused on the technical and not economical side of this analysis. In a more precise way, the industrial perspective for this work can be summarized in three main objectives:

- **The conception and implementation an AC/DC interlink converter prototype between the LVAC and the LVDC distribution grids**
- **The development of a cost-effective selective protection scheme for future LVDC distribution systems for the safety of users, assets, and the grid itself against short-circuit and electric shock**
- **The evaluation of power quality of LVDC distribution system in terms of steady-state and transient phenomena through well-defined and potentially standardizable indicators**

Each one of these goals can be evaluated from a scientific point of view, where other sub-objectives can be defined.

- **AC/DC converter prototype:**
  - Definition of the best suited converter topology for the perimeter of this work
  - Design of a control system
  - Sizing of each component of the converter (switches, filters and modulation)
  - Different experimental tests

- **Protection scheme in LVDC**
  - Study of the short-circuit endurance of the AC/DC converter
  - Definition of an adapted grounding system
  - Definition of DC protection devices against short-circuit and electric shock
  - Design of an integrated selective protection scheme

- **Power quality evaluation in LVDC**
  - Definition of transient and steady-state power quality related phenomena in DC
  - Definition of different indicators to evaluate these phenomena
  - Study of how the AC/DC converter impacts PQ indicators
  - Definition of a strategy to address the subject of disturbance propagation in LVDC

To accomplish the objectives enumerated above a scientific approach is used to define the development steps shown in Figure I.1. At the end of each step, intermediary results are analysis and validated, serving as a base for the next step.

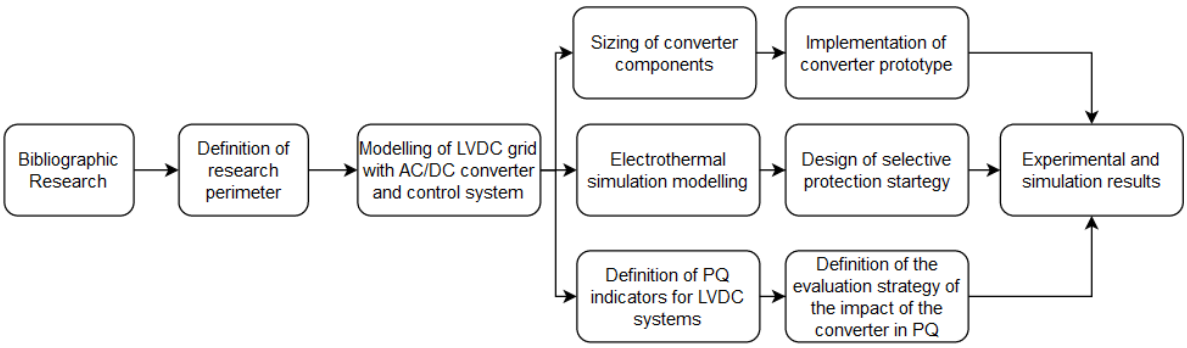

Figure I.1 Scientific approach

In Chapter 1, bibliographic research is conducted with the objective of investigating the LVDC domain from an overall perspective. More specifically, the goal is to address for example what types of LVDC distribution systems exist, what grid architectures are used around the world and what are the most used distribution voltage levels. In the same style of state-of-the-art research, Chapter 2 presents details on the three main aspects of these research, which are power electronics, protection schemes and power quality assessment methods. It is in this chapter that specific challenges are identified, in relation with the three main objectives presented above. To approach them, Chapter 3 demonstrates the set of solutions proposed, in terms of converter modelling and sizing, design of a selective protection plan and definition of power quality analysis strategy. Finally, Chapter 4 shows and examines experimental and simulation results.

Chapter 1. Overview on LVDC distribution grids

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1.1. Introduction

In the last two decades, the scientific and industrial communities saw significant modifications being made in the ancient model of electrical systems around the world, either for electricity transportation or distribution grids. The challenges related to climate crisis and carbon neutral energy consumption encouraged scientists to imagine a more energy efficient world in the future. In this scenario, it is getting more and more clear that Renewable Energy Sources (RES) and Energy Storage Systems (ESS) may be part of a more sustainable model of living in the planet. Considering this fact, it is possible to conclude that a key aspect for this new model to prosper resides in how to facilitate the integration of RES and ESS in the existing electrical systems. Considering that in most cases, both these energy assets are naturally interfaced by a direct-current (DC) link, the use of DC for distribution grids is rising as a promising concept.

Nonetheless, considering that the AC infrastructure will continue to exist for next decades, it is important to understand how both systems can coexist in a harmonious environment. In this way, the main objective of this chapter is to evaluate the multiple characteristics of hybrid AC/DC distribution grids.

Through the first section it will be possible to understand where, how and when direct current was used in electrical systems, until nowadays with the emerging possibility of using DC for distribution grids. The second section presents details regarding the possible advantages from the use of DC in distribution grids when compared to classic AC. The third section addresses the multiple types of architectures for LVDC distribution grids and their characteristics. In the fourth section, a discussion is presented around different existing standards. The fifth section introduces information about the three most important LVDC ecosystems around the world. Finally, the last section demonstrates the importance of the choice of the distribution voltage level and what are the most recent trends in the subject.

1.2. Historical context

1.2.1. The first steps of electricity distribution systems

At the end of the nineteenth century, during the second industrial revolution, electricity was finding its way into becoming a largely used energy transportation method, the contention between Edison and Tesla-Westinghouse arose. The matter under consideration was the use of Alternate current (AC) systems proposed by Tesla, or Direct Current (DC) systems proposed by Edison, to transport and distribute electrical power [**REY76, FAI12**]. At the time, AC power systems prevailed mainly due to the advent of the transformer [**HAL61**], which was able to increase the transmission voltage levels, leading to a substantial reduction in the conduction losses. In this perspective, AC transmission and distribution systems spread all over the world, representing at that time the most efficient way of ensuring the energy flow between generation and consumption.

A classic architecture of the complete AC power chain in an electrical system is shown in Figure 1.1. In this model, energy generation sets normally deliver power at a Medium Voltage level (MV). Subsequently, to be transmitted, the voltage level is stepped up by a substation into a High Voltage level (HV). Finally, another substation steps down the voltage level into MV and a distribution transformer

delivers the energy to residential and commercial sectors at a Low Voltage level (LV). Based on the IEC60038 standard, Table 1.1 shows the standard voltage domains used in France (HTA in France correspond to the MV domain).

Given the success of the AC technology to transmit and distribute energy, for some decades, DC power systems were restricted to some specific applications and scenarios, such as submarines/ships and satellites, trains, subways and trams [**SHI22**].

Table 1.1: Voltage level domains in France

Class		French Standard (AC)	French Standard (DC)
High-Voltage	**HTB**	U_n* > 50kV	U_n ** > 75kV
	HTA	1kV < U_n <= 50kV	1.5kV < U_n <= 75kV
Low-Voltage	**BT**	50V < U_n <= 1kV	120V < U_n <= 1.5kV
Extra Low-Voltage	**TBT**	U_n <= 50V	U_n <= 120V
* AC - U_n is the RMS line voltage; **DC - U_n is the voltage between two poles			

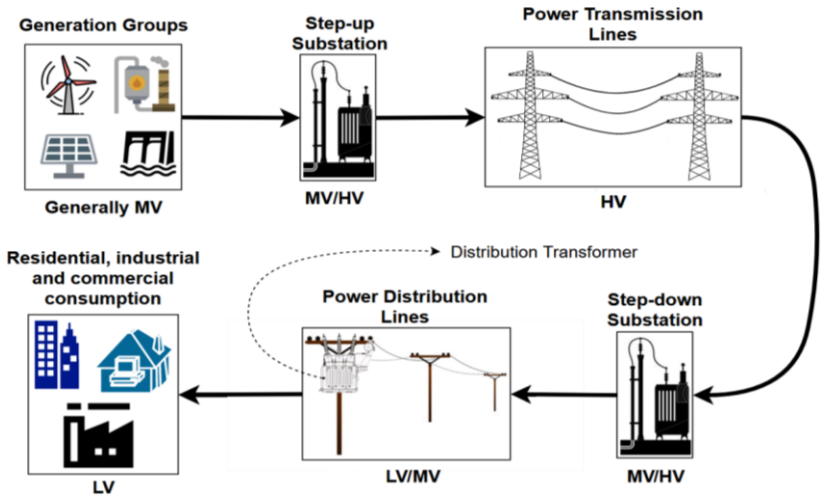

Figure 1.1: Classic architecture of an electrical power system

1.2.2. The first worldwide use of DC in non-islanded power systems

In the last few decades, though, the discussion between the use of AC and DC from energy transmission re-emerged due to some technological breakthroughs, such as the improvements in the Power Electronics sector.

The first great change in an AC dominated world, was the use of High-Voltage DC (HVDC) to transport electricity through long distances. Upon the first commercial installation of an HVDC system in Gotland (Sweden) [**RUD00**] in 1954, this strategy has been largely used in many countries. With few exceptions, the main use of HVDC is to interconnect AC power systems with a point-to-point (PTP) architecture [**AKH14**]. Besides the economic gains for long distances, HVDC is also the most usual technical approach that can be used when asynchronous AC systems (i.e. AC systems that operate with different frequencies) must be linked. An example of HVDC system is the 800km transmission line in Brazil, connecting Itaipu (Hydropower plant – 50Hz) with a conversion station in São Paulo (60Hz). The system can transmit 6300MW through a ±600kV$_{DC}$ bipolar line and at the time it was built (1984),

it represented the greatest HVDC system in the world in terms of power and DC voltage level. Figure 1.2 shows the architecture used in Itaipu [**GRA05**].

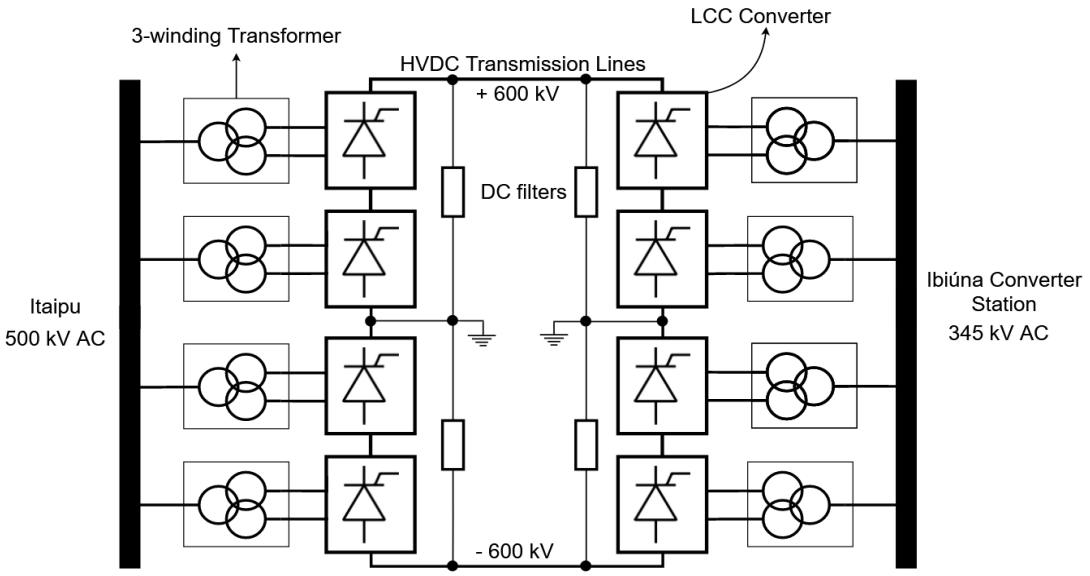

Figure 1.2: Itaipu HVDC transmission (Brazil)

HVDC transmission systems benefit from lower loss effects to increase the capacity of transmitting energy when compared to HVAC systems. From another perspective, for the same power transmission, HVDC systems need less infrastructure in terms of conductors. Even if the initial investment for an HVDC system remains higher than the one for HVAC, at a certain transmission length, HVDC becomes economically more attractive than HVAC [**RUD00**]. Loss phenomena evoked here are due to the skin effect and the reactive power and it may be important to present a way of quantifying them.

- In the AC domain, the density of the current that passes through a conductor is higher near the periphery of the conductor [**ALA88**] and decays exponentially based on the depth from the conductor's surface. This nonuniform characteristic results in an increase of the conductor's resistance. The skin depth (δ) represents the depth of the conductor where the current density is at 37% of its value at the surface. With the skin depth (1.1), it is possible to calculate the resistance of the conductor considering the skin effect. An approximation proposed by IEC 60287-1-1 [**IEC06**] is showed below. In the DC domain, however, the electric current is uniformly spread over the conductor cross-section reducing the conductor's resistance, and consequently reducing the system global losses.

$$\delta = \sqrt[2]{\frac{1}{\pi f \mu \sigma}} \tag{1.1}$$

$$R_{AC} = R_{DC}\left(1 + \frac{x_s^4}{192+0.8x_s^4}\right) \tag{1.2}$$

$$x_s^4 = \left(\frac{8\pi f K_s}{R_{DC}10^7}\right)^2 \tag{1.3}$$

f: frequency (Hz)

μ: magnetic permeability of the material (H/m)

σ: conductivity of the material (S/m)

K_s: equals to 1 for round conductors

δ: skin depth (m)

- Inductive and capacitive impedances of an AC line is proportional with the length of that line. So, the longer the line, the higher the reactive component, which increases losses. In addition, the reactive power generated by the natural capacitance of AC conductors (C_0) is proportional to the square of the phase voltage (equation 1.4. Consequently, the higher the transmission voltage level, the shorter the length of the power line that can operate without reactive compensation. However, in a DC line, those effects do not exist because there is no reactive power. Therefore, for the same rated power level, a DC line can deliver more energy.

$$Qc = V \cdot I_c = V \cdot [3 \cdot V \cdot \Sigma(C_0) \cdot \omega] \quad (1.4)$$

Finally, and still regarding the HVDC domain, it seems important to highlight the conversion topologies used to deploy an HVDC transmission system in terms of power electronics. Historically, the first converter topology used in HVDC was the Line-Commutated Converter (LCC). The latest version of this architecture is thyristor-based and works at the line frequency (50/60 Hz). Its use is restricted to interconnect AC power systems endowed with high short-circuit capacities [**AKH14**]. In Figure 1.2, it is possible to observe a classic 12-pulses LCC.

The second architecture is based on transistors (normally IGBTs - Insulated Gate Bipolar Transistors). These semiconductors are not only capable of being turned on, like the thyristor, but they are also capable of being turned off. Associated with a Nearest-Level Modulation (NLM) control, the VSC can be used in a large spectrum of appliances because it offers better controllability of the power flow. It is adapted for black-start operations, grid forming control, both active and reactive decoupled control, and does not require specific short-circuit power to function. The newest architecture of VSC is called Modular Multilevel Converter (MMC). Its modules can be composed by different structures (half-bridge or full-bridge for example) and they can be connected in series, allowing the converter to operate at a high-voltage level. Figure 1.3 shows a classic VSC topology.

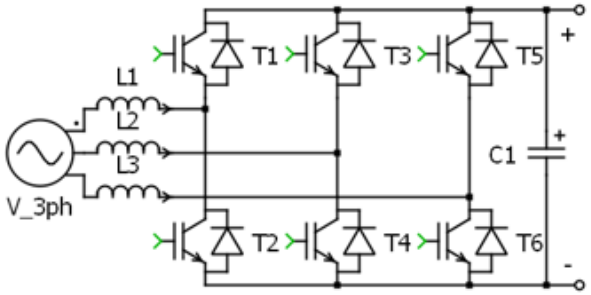

Figure 1.3: 3-phase 2-level VSC

The MMC is also capable of delivering a multilevel voltage, offering new advantages in terms of harmonic spectrum and facilitating filtering of voltage and current. An example of a real application of the MMC topology is the HVDC interconnection INELFE 1 between France and Spain [**SIE16**].

1.2.3. DC in the low-voltage distribution domain

Apart from the HVDC domain, in some fields there are power systems that historically employ a DC as a way of distributing electricity in low voltage. There is evidence highlighting that DC

distribution systems are present in spacecraft, telecommunications, traction, and shipboard power systems [**GHA13**]. The preference to use DC over classic AC systems in these systems is normally due to specific characteristics they have.

Well established uses of LVDC distribution systems, resulting from different investigations in the telecommunications sector, are the DC supplied Data centers. The growth in the number and consumption of Data centers around the world stimulated research regarding the efficiency improvement in the power supply of those facilities. Studies concluded that an internal distribution of 380-400V_{DC} was able to optimize the energy use **[PRA07]** in around 7%. Since then, some standards in the LVDC distribution domain are being established based on the choices made for Data centers, mainly in terms of equipment and electrical devices.

Nonetheless, following the improvements in power electronics in terms of costs reduction and efficiency increase, DC power systems became more and more competitive in a more global perspective. In this scenario, the use of DC in distribution grids are gaining visibility. To understand the international movement towards low-voltage DC (LVDC) distribution systems, it is important to acknowledge the fact that from a LV point of view the world is already DC-dominated.

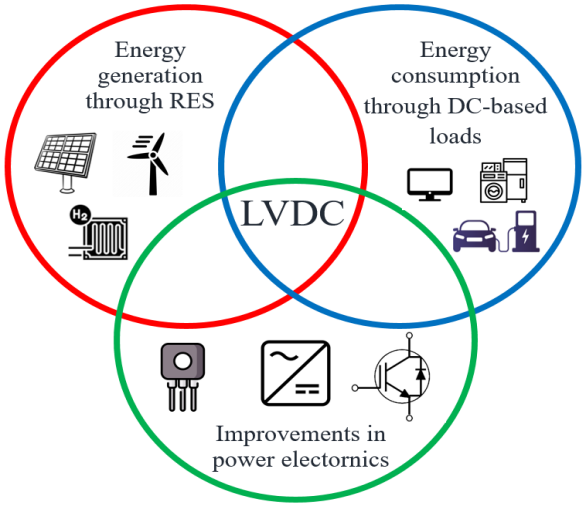

Figure 1.4: Triad on which LVDC distribution systems are based

In the first place, it is possible to observe a strong growth of DC-based electronic loads. Computers, phones, telecommunication devices, electric vehicles [**LOC14**], battery-powered devices and others are now a part of people's daily life, and they are naturally DC-interfaced. On the same LV world, but in the energy generation side, some important RES and ESS are also DC-based devices. Technologies such as Fuel Cells (FC) and Photovoltaic Panels (PV) will certainly make part of distribution systems in the future, increasing its participation in the energy mix of the world as its costs decreases and its efficiency increases. For example, in France, in 2019 there was a reduction of 26% in the cost of PV modules used in continental cities [**CRE19**]. This whole scenario is promoting research, projects and many studies in the domain lately.

In the same way, assuming that microgrids (MGs) and distributed generation will be a part of the future concept of energy distribution systems, the scientific community seems to be getting interested in DC MGs **[CAU19, SIL21, DJA22]**. In general terms, a low-voltage MG represents a set of loads and micro-sources (locally generating an active power generally inferior to 100kW) interconnected by a reduced size grid **[LAS02]**. Considering that PV generation, storage and efficient energy consumption are three of the most important supports for the deployment of MGs, it is possible to imagine a distribution system through a LVDC backbone.

Another aspect to consider is that, nowadays, humanity faces a global context of climate impacts, in such a way that the world is really concerned about factors just as sustainability and environmental care. This situation led to the development of a new worldwide energy model, characterized by the increase in the portion represented by RES in the energy mix. Consequently, this new model also envisages a considerable reduction in the use of fossil fuel-based energy sources. Therefore, one of the keys to answer to this problematic is to have power systems that may be able to optimally connect with RES to boost their presence in the energy mix. Considering this context, it is possible to observe that DC power systems may provide some possibilities of RES integration and better adaptability for DC-based loads.

However, considering that LVAC distribution systems are very mature after many decades of operation, it seems to be necessary to investigate, in detail, what are the real advantages of using DC over AC, in what use-cases, and how to quantify it.

1.3. Motivations of using DC for distribution grids

Following the reasoning started at the previous sub-chapter regarding possible advantages of DC over AC, it is important to search for scientific data which can prove in which scenarios it is economically beneficial to use DC in distribution systems. Further on, a review will present a perspective of how DC power systems can contribute to a more efficient and sustainable energy model.

The advantages mentioned here will be defined mostly by a comparison between new DC distribution architectures and classic AC systems. Many parameters could be used to make such comparison: investment cost to implement both systems (CAPEX), operational costs to exploit the systems (OPEX), direct environmental impact, resilience, efficiency, controllability, and reliability **[BAC15].**

The present research will consider the last three aspects: efficiency, controllability and reliability. Those parameters were chosen because they represent important indicators for future distribution systems. Besides that, these three indicators do not necessarily need feedback from finished projects and well-established infrastructures, which allows a comparison with classic LVAC grids, since LVDC distribution systems are still finding their way into modern Smart-grid (SG) architectures.

1.3.1. Energy efficiency

An improvement in the energy efficiency in a distribution system is analyzed here as the capability of reducing the losses in the power chain (in the grid conductors or the conversion stages, for example) while maintaining the correct operation of the distribution system.

As already evoked, in the actual global context, the concept of distributed generation through RES is becoming increasingly important. It represents one of the alternatives presented by the scientific community to decentralize the energy production and to increase the presence of RES in the energy mix. Considering that PV, storage and even variable speed wind turbines are all DC friendly, it seems logic to investigate a way of distributing the energy generated through those sources directly in DC. It would avoid the use of some conversion bricks, which can be observed in Figure 1.5, thus improving efficiency. Some comparative data show that the use of PV associated to a LVDC distribution system can represent a gain in overall efficiency up to 8% **[FRE15]** or still up to 13% [**GAR11a**].

From the consumption side, efficiency improvements are also necessary since the global residential energy consumption grew around 7% annually from 1990 to 2008 and is going to reach a 250% augmentation in 2030 compared to data from 2010 [**GAR11a**]. Besides, the exponential growth in the use of electronic devices (Data centers, computers, phones, LED lighting, electric vehicles, space cooling devices, heat pumps...) is considerably increasing the percentage of DC energy consumption. From [**DIA15**], it is possible to see that, in 2015, 50% of all the building loads are DC-based. This scenario would also benefit from a LVDC distribution power system, reducing even more the conversion stages, consequently increasing the energy efficiency (Figure 1.5).

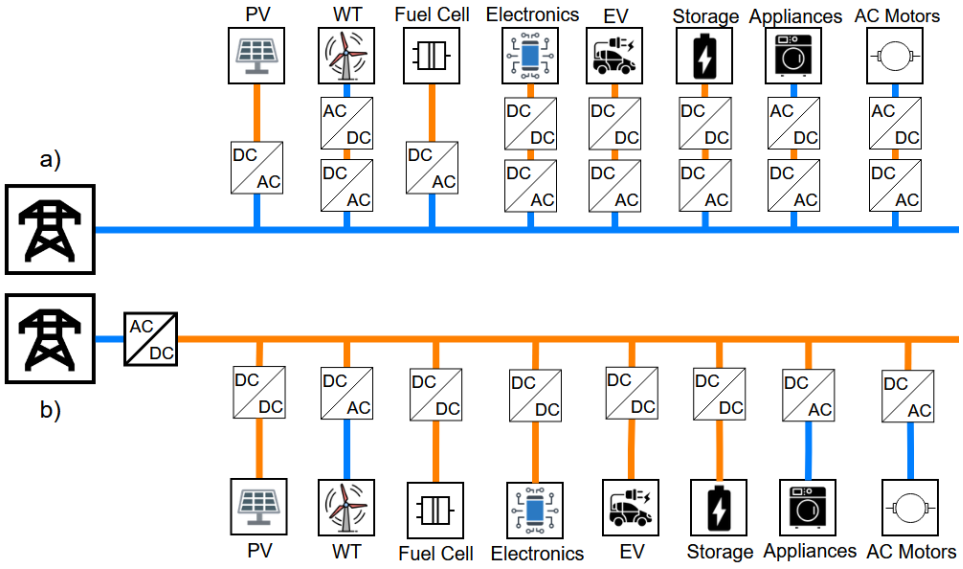

Figure 1.5: LVAC (a) vs LVDC (b) distribution scheme comparison

To prove this point, there are studies that focus on reviewing already existent DC-compliant equipment and estimating efficiency gains if compared to classic AC-powered equivalents. For example, considering an average residential installation in the USA, switching from classic appliances to DC-based technologies can represent energy savings that go up to 33%, with 14% of losses avoided by suppressing AC to DC conversion steps **[GAR11b].** Even further, high-efficiency prototypes of DC adapted end-use loads, such as refrigerators, wall adapters and task lighting are already being developed **[GER19]**. Likewise, in terms of power electronics for LVDC appliances, current topologies of DC/DC converters are able to outperform the most part of AC/DC converter bricks in terms of energy density and efficiency **[WEI15, GWO14]**. For instance, Figure 1.6 shows a classic conversion topology of AC power supplies for electronic appliances, composed by a single-phase rectifier, a Power-Factor Corrector (PFC) and two cascaded DC/DC converters. This architecture performance is around 88% or lower (for low costs models), while connecting the appliance directly in V_d (in a LVDC distribution bus) may increase the efficiency up to 93% **[WUN14].** Still regarding load-associated converters, there are studies demonstrating that their performance has an important impact in the global efficiency of a distribution system, in such a way that 1% of efficiency variation can cause up to 10% of variation in total losses [**KAK12**].

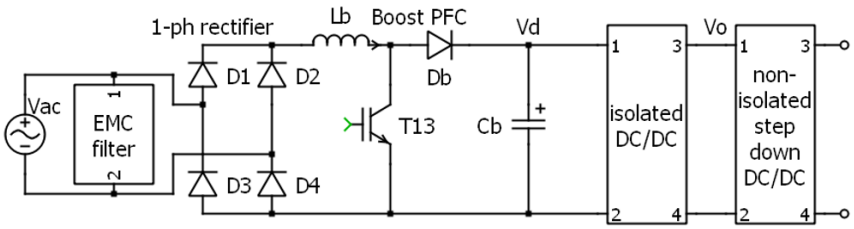

Figure 1.6: Classic AC/DC switched power supply

A third factor to be considered is that the electricity transport over a distance is intrinsically more efficient with DC than with AC. In terms of power systems, if a distribution network is considered and for the same feeding current level, DC systems can transmit more energy than their AC counterparts. This is because, as described in section 1.2.2, in a DC system there is no skin effect and there is no reactive power.

Subsequently, some results from practical appliances from around the world will be presented. They will allow a realistic view from the possible efficiency advantages presented above. It must be considered though, that LVDC distribution systems are still an emerging concept, so most of the presented data come from simulation predictions, demonstrators, or experimental testbeds.

1.3.1.1. Data analysis on studies investigating the efficiency of LVDC distribution systems

The following analysis will be classified in two categories: internal building LVDC distribution or public LVDC distribution (Figure 1.7).

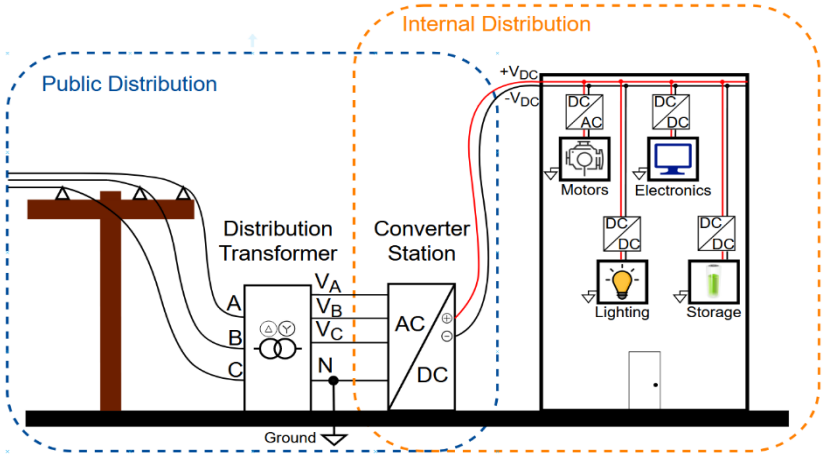

Figure 1.7: Distinction between public and internal distribution systems

This division has the objective to clarify the differences between the technological choices associated with each one of these systems and how they impact the efficiency. When the converter station is integrated in the facility been powered, it is usually considered a part of the internal distribution. The other case is when the converter station feeds a set of facilities, it is usually more powerful, located near the distribution transformer and followed by distribution lines. In this case, the converter station is considered a part of the public distribution.

Starting with internal distribution grids, many studies have been conducted in past few years, comparing the efficiency of the classic LVAC distribution with new LVDC architectures. Generally, they seek to explore the advantages of an internal DC-based distribution that were already discussed. The most part of the publications in this area are simulation based **[ANA10, VOS14, BRE16, GER18, GLA16]**. However, there is also some experimental research, through testbeds and prototypes **[BOE15, FRE15, WEI15]** installed in different facilities. The analysis of those previous scientific investigations led to some common base knowledge.

Since an internal DC distribution is a natural link to PV generation, efficiency is higher when there is a considerable amount of on-site DC energy generation **[WEI15, FRE15]**. Also, the presence of energy storage systems is a factor that increases the global efficiency of the DC-based power system **[VOS14, GLA16]** since the AC/DC converter is less requested to operate. This is mainly due to two situations:

a) The PV generation cannot fully supply the power system: in this case the batteries will supply the required energy and no energy will be requested from the utility grid.

b) The PV groups generate more energy than required: in this case the batteries will be recharged, storing the energy surplus and no energy will be sent to the utility grid.

Also, there are some other aspects that significantly influence the global efficiency of the DC distribution system. The efficiency of the power electronics converters varies based on the power level they are suppling and the nominal power level they were designed to operate. When supplying low power, converters generally operate with a low efficiency **[GER18]**, and that is a significant situation to be considered. Also, end-use loads play an important role for efficiency aspects, and for comparison reasons between AC and DC, similar technologies must be considered **[BRE16]**.

Regarding this last aspect, experimental research in the area shows that, over time, in general it is possible to make some structural changes and adapt different sets of loads to work with a DC distribution bus **[WEI15]**, leading to a more efficient use of electric energy. Installed DC distribution systems supplying LED lighting **[BOE15]** in buildings or even more complex motor-based loads **[FRE15]** also show favorable results to the use of a DC distribution in terms of energy savings. Table 1.2 compiles some of the assumptions made and results obtained by publications cited above.

In the present moment, the high costs associated to all the technology needed to an efficient DC distribution for residential or commercial applications may be one of the primary reasons that are holding back its feasibility. However, even this situation may change in the future **[GLA16]**. The growth interest in DC in the industrial market will keep on promoting the development of more efficient and less expensive DC-based devices.

Previous research also includes studies that are dedicated to the analysis of the public part of an LVDC distribution system **[MAN15, ATI16, DAS17 and GEL15]**, that is when the converter station and the DC distribution lines are managed by the power grid operator. However, publications and papers with this focus are more unusual in academic conferences and studies, mainly because studies that include a public DC distribution are more difficult to be conducted.

Considering that, in a public distribution scenario the power grid lines are considerably longer, the technology of the conductors used, and the distribution voltage level are important choices, since they usually impact more the overall efficiency of the system than in the case of an internal distribution. However, since there are no well-established standards, different voltage levels are proposed by the literature. For very small distances and low-power grids, it is possible to imagine a low-voltage distribution (under 120V) that does not require complex protection devices and can be compatible with electronic end-use loads **[MAN15]**.

Table 1.2: Previous Research Analysis on internal DC distribution systems Efficiency

	ANA10	VOS14	BRE16	GLA16
Study nature	Simulation	Simulation	Simulation	Simulation
Focus	Commercial and residential	Residential	Commercial	Residential
Energy Sources	PV, ESS, WT, AC grid	PV, ESS, AC grid	PV, ESS, AC grid	PV, ESS, AC grid
Loads	Multiple	Multiple	Multiple	Multiple
Converters' efficiency	Static in relation to power variation	Variable in relation to power variation	Variable in relation to power variation	Variable in relation to power variation
Other considerations	It presents a different analysis for commercial and residential situations	Bidirectional power flow in the main AC/DC converter	It highlights the importance of similar technologies for fair comparison	It highlights the elevate cost of the DC technology and evaluates the impact of ESS
Efficiency improvement with DC	Residential: 15-22% Commercial: 10-11%	With storage: 14% Without storage: 5%	PV, ESS: 3.4% PV, ESS + AC grid: 1.3%	With storage: 14-25% Without storage: 9-20%

	GER18	CHA20	JOS22	ALS22
Study nature	Simulation	Simulation	Simulation	Simulation
Focus	Commercial	Residential	Commercial	Residential
Energy Sources	PV, ESS, AC grid	PV, ESS	PV, ESS, AC grid	PV, AC grid
Loads	Only DC-internal	Multiple	Multiple (AC, efficient AC and DC)	Multiple (AC and DC)
Converters' efficiency	Variable in relation to power variation	Static in relation to power variation	Static in relation to power variation	Variable in relation to power variation
Other considerations	Explores the possibilities of futuristic ZNE buildings. Considers some unrealistic situations for the present	It considers a small-scale residential facility and focuses on the performance of loads	It uses a microgrid optimization software to make a technical-economic analysis	It highlights that efficiency of LVDC distribution system increases substantially with direct use of PV energy.
Efficiency improvement with DC	Average building: 9.9-11.9% Best scenario (unrealistic): 17.9-18.5%	14% when comparing energy efficient loads for both AC and DC distribution system	It highlights a 10% energy consumption reduction with 48V DC loads	15% with a good PV generation to energy consumption ratio
	BOE15	**FRE15**	**WEI15**	
Study nature	Experimental	Experimental	Experimental	
Focus	Commercial	Commercial	Commercial	
Energy Sources	PV, AC grid	PV, AC grid	PV, AC grid	
Loads	LED lighting	LED Lighting	Multiple	
Converters' efficiency	Variable in relation to power variation	Variable in relation to power variation	Variable in relation to power variation	
Other considerations	Part of the ENIAC project DCC+G	Microgrid designed by BOSCH	Part of the ENIAC project DCC+G. Adapts multiple loads to work in DC	
Efficiency improvement with DC	For nominal power: 2% For 2x nominal power: 5%	Improvement of PV energy use: 6-8%	Normal conditions: 2.7% Almost 100% of local generation: 5.5% Improvement of PV energy use: 7%	

In another way, for longer and more powerful lines, in order to obtain a higher efficiency, it is also possible to choose a higher voltage level **[DIA16a]**. Previous research **[DAS17]** considers even a medium-voltage direct current (MVDC) layer as a link with the LVDC distribution, instead of the classic AC utility grid. It represents an unrealistic situation for the present scenario for the current state of power systems, since MVDC grids are still rare around the world [**MES15**]. Nonetheless, it consists of a possibility for the future with the objective of achieving greater compatibility levels. Table 1.3 summarizes studies considering a DC utility grid.

Another important consideration regarding public distribution is the efficiency of the converter connecting the AC utility grid with the DC distribution. Considering that, compared with an internal distribution, the converter rated power level can be considerably higher since the set of fed loads may be wider, its impact in the global efficiency is also more important. There are studies that evaluate the efficiency of the main AC/DC converter, here defined Interlink Converter (IC), in different situations, showing that in light-load scenarios the efficiency is substantially lowered, and that the converter is the responsible for most of the system losses **[GEL15]**. Finally, concerning efficiency gains, the only common point from different studies regarding public LVDC distribution seems to be that the presence of on-site DC energy generation (PV and storage) can significantly improve the efficiency of a DC distribution **[ATI16, GEL15]**.

Table 1.3: Previous Research Analysis on public DC distribution systems Efficiency

	MAN15	GEL15	ATI16	DAS17
Study nature	Simulation	Simulation	Simulation	Simulation
Focus	Public Distribution for Residential sector	Public Distribution for Residential sector	Public Distribution for Residential sector	Public Distribution for Residential sector
Energy Sources	AC grid	AC grid	PV, AC grid	AC grid
Loads	Multiple	Multiple	Multiple	Multiple
Converters efficiency	Variable	Variable	Static	Static
Intermediary converter	No	No	No	No
Other considerations	Assumption that many loads are compatible with 48VDC distribution. Highlights the importance of more detailed analysis.	Strong focus on characterizing load variation to evaluate the performance of the central AC/DC converter.	Highlights that on-site PV generation improves the efficiency of a DC distribution	Focus on doing a fair comparison in terms of loads between both distribution systems
Efficiency improvement with DC distribution	6.36%	No comparison	No improvement	1%

1.3.1.2. Inferences

It is possible to see that the absence of proper standards in the area complicates the notion of boundaries for research in the domain. In addition, since every study has a specific focus, chooses a set of parameters, and makes a certain number of assumptions, it is not simple to compare the results obtained in each case. However, this review has a particular significance, in the sense of showing the possibilities and potential gains, in terms of efficiency, that a LVDC distribution can bring to the domain of power systems, especially for future SGs with high RES generation and storage.

Another conclusion is that most part of the efficiency gains and consequent reduction of energy-associated costs directly affect the end-user and not the DSO. Apart from use-cases like EV charging stations [**HUY22**] and public LED lighting, from a DSO perspective, the investment to create a public LVDC distribution grid remains higher than the efficiency gains, making the payback period very long. However, this reality could change in the future due to the reduction in technology costs. Consequently, having the expertise to be able to deploy distribution systems in LVDC may be important for DSOs or different operators of private electric systems.

The promising results for internal LVDC grids showed the possibility to change the domain of DC in power systems, going from some small specific applications in power systems to a reliable, efficient, and wider way of distributing electrical energy. The movement towards LVDC grids will continue to be potentialized with the continuous growth in the use of DC-based loads and the continuous development, and consequent reduction on the costs of the technologies associated with a DC distribution (PV, storage, converters). Hence, it seems that this progression in this direction will be driven from downstream loads, appliances, and local generation slowly progressing to the upstream distribution grid (from private internal grids to public distribution systems).

1.3.2. Controllability and reliability

Another advantage of using DC for distribution grids is the higher level of controllability if compared to a classic AC equivalent. Regarding this aspect, the first thing to be considered is the

presence of an IC upstream the DC distribution grid. An interlink converter is capable of controlling the power flow between the AC utility grid and the DC distribution grid. Modern PWM-modulated vectorial control can regulate reactive power in the AC side at the same time as active power (in DC current source mode) or the DC voltage (in voltage source mode).

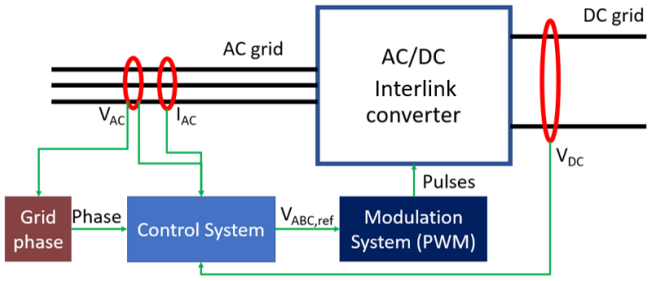

Figure 1.8: Classic interlink rectifier scheme for LVDC

Figure 1.8 represents the control and modulation scheme of an IC. From this perspective, it is possible to see that an active fully controllable device upstream the distribution grid is also able to guarantee a certain level of immunity from disturbances in the AC utility grid.

The control system is often designed through a vectorial approach using the Park transformation. With this mathematical technique, voltage and current are converted from a rotating reference frame (abc) to a static DC reference frame (dq). Such technique allows the use of a simple Proportional-Integral controller to easily force current steady-state error to zero. In addition, active and reactive power are controlled separately by the direct (d) and quadrature (q) components of the current (I_d and I_q). I_d is responsible to establish active power drawn from the AC grid, while I_q is responsible for the reactive power. Finally, an external voltage control loop can be implemented to impose a reference value for I_d in order to regulate the DC bus voltage [**KIM22**].

Further on, it is important to make a comparison between power flow in AC and DC. In classic AC systems with synchronous/induction generators, the reactive power balance can be ensured through voltage drop in the power lines, while active power balance can be estimated through voltage frequency variation. In DC, since there is no reactive power, the stability between generation and consumption is a function of the DC voltage. The active power flow can be estimated and controlled by the different energy sources through the voltage-drop in the distribution line. From this perspective, simple and non-centralized voltage-current or voltage-power droop control systems can be used for each component connected to the LVDC distribution grid [**YU13, KIM18**]. The idea behind this strategy is that, in function of the DC bus voltage, the device-associated converter locally modifies the energy consumption/generation [**SEC14**]. Figure 1.9 illustrates this general concept.

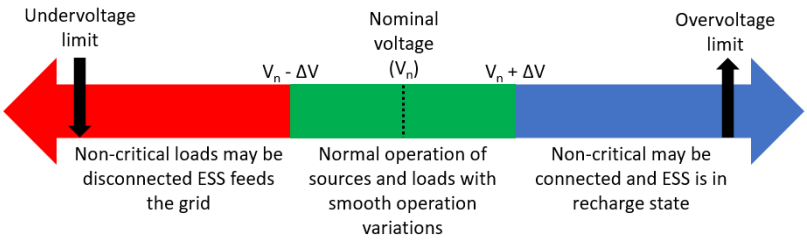

Figure 1.9: General voltage droop control for LVDC distribution systems

The main advantages of this type of decentralized control are: the low cost associated to the infrastructure, high reliability since no connection or communication to a central controller is needed, and high scalability since the presence of new loads and sources does not impact the general

infrastructure of the distribution system. The main disadvantage of this control type is the voltage drop in distribution conductors, since voltage is not the same throughout the grid. To solve this problem, many different strategies have been proposed in the literature [**PEY18, DRA14, HUA15**].

In future residential and commercial buildings, in which ESS and local RES will be present, this enhanced controllability with a simple management strategy could be useful to create a flexible and reliable distribution system.

1.3.3. Synchronization and resiliency

The last aspect, which seems to be a great advantage in using LVDC for distributing electricity is the ease of source hybridization and parallelization. Since in DC the fundamental frequency is zero, no phase synchronization is needed. Therefore, interconnect RES, ESS and to adapt the grid in real-time in order to match consumption requirements or recover from fault is simpler if compared to the AC case.

Even further, using DC is a way of bypassing the synchronization issue of ring-based grid topologies. This kind of architecture has a high level of resiliency and availability since there may be multiple paths of feeding consumers. Many studies have proposed to adopt this topology, associated with the adapted protection strategy, in future smart grids [**TIW22, SAL19a, ABD19**]. For situations that require the highest possible availability, LVDC can also be an enabler for meshed distribution grids [**SAA22**].

Still regarding the subject, using the same triple-conductor infrastructure of AC systems, it is possible to deploy a bipolar distribution architecture, which is capable of managing two DC poles independently. In this case, if there is an exploitation problem or fault in one pole, loads can be managed to be supplied by the other pole. More detail on all these characteristics on different grid topologies will be discussed in next section.

1.4. Architectures of LVDC distribution grids

As already seen, some of the grid topologies that can be deployed in LVDC present interesting operation characteristics to enhance reliability and resiliency. For this reason, it is important to analyze what are the possibilities and trade-offs associated to each configuration. Since this subject is relatively recent and the scientific knowledge around it is still beginning to get established, there are many different architectures proposed in the literature. Here, an analysis will be made to classify those topologies according to 5 different aspects: number of independently controlled poles, bus voltage behavior, number of different voltage bus, type of distributed energy and configuration of the distribution grid.

1.4.1. Number of poles managed separately by the interlink converter

- Monopolar distribution:

In this architecture one (asymmetric-monopolar) or two (symmetric-monopolar) voltage levels are available through the distribution grid, as illustrated in Figure 1.10. This architecture is the simplest in terms of cabling and power electronics. However, there is only one interlink converter to manage voltage regulation. For the asymmetric-unipolar distribution grid, loads can only be supplied by a (0, $+V_{DC}$) voltage. On the other way, the symmetric-monopolar structure provides one additional voltage level ($-V_{DC}/2$, 0, $+ V_{DC}/2$), often created by a capacitive voltage divider. Nonetheless, the fact of having

one single converter upstream the grid can cause voltage imbalance problems if there are more energy flowing from one semi-pole than the other one. Solution exists to bypass this issue, but it often involves using other converters in cascade [**BRO17, CHE19**].

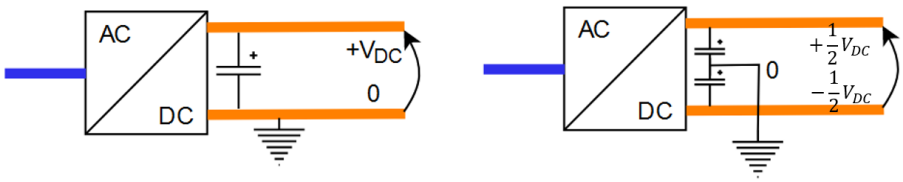

Figure 1.10: Asymmetric-monopolar and symmetric-monopolar distribution grid topologies

- Bipolar distribution:

Alternatively, Figure 1.11 shows this other possibility that supply three voltage levels through with two independently regulated poles. If compared to a unipolar distribution, with the addition of one distributed conductor and a second AC/DC converter in series with the first one, it is possible to operate with two times the power [**CHE19**]. With this configuration, one can also have more availability and reliability **[KAK10, LI18, MOU19]**. In case of a line fault, it is possible to keep the power supply with the not faulty line. In addition, with the proper earthing system, the voltage to the ground is always half of the pole-to-pole voltage, which is also important in terms of security and protection.

Nonetheless, it represents a more complex and more expensive solution. To operate correctly, the AC/DC converter must be capable of managing the possible load imbalance and the consequent voltage fluctuations for each pole.

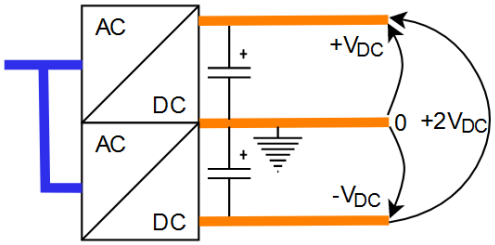

Figure 1.11: Bipolar distribution grid topology

1.4.2. Bus voltage behavior

- Constant bus voltage:

In this case, the voltage level that is distributed through a common bus is regulated by the interlink AC/DC converter to reach a constant value. Generally, in this case there is a voltage control loop, which is activated in function of which converter is controlled in grid-forming mode (in the interlink converter or in the ESS converter). Usually, this configuration is obtained when there is a single-layer centralized controller, imposing the behavior of sources. Figure 1.12 illustrates a general constant bus architecture with central control.

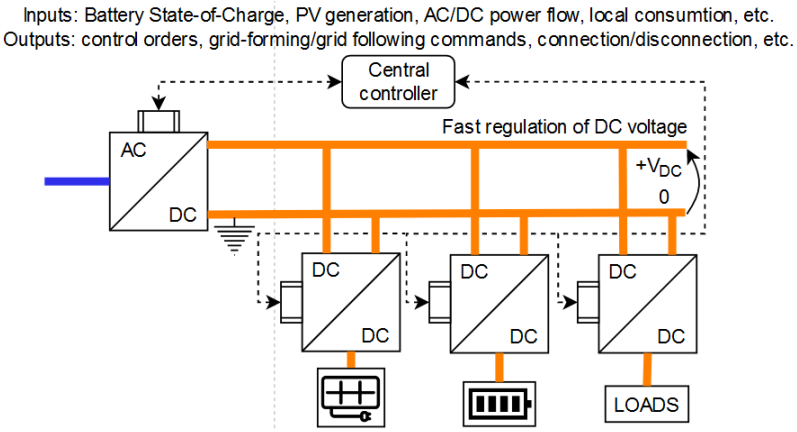

Figure 1.12: General constant voltage DC bus architecture

- Variable bus voltage:

In this particular architecture, the voltage in the DC bus can vary between acceptable limits. For example, a LVDC distribution grid supervised by a decentralized droop-control strategy is subject to a variable voltage in the DC bus (Figure 1.9). In this case, in function of the fluctuating voltage, the droop-control is responsible to locally impose current/voltage references to the converters associated to source and loads, which globally maintains the ratio generation-consumption. In general, a secondary control is responsible to avoid voltage deviations. To do so, different strategies have already been proposed [**DRA13, HUA15, PEY18, LIU23**].

Even if it represents a very specific application, another example of this scenario is when a facility has local PV generation, and the Maximum Power Point Tracking (MPPT) algorithm is executed by the central AC/DC converter and the PV group is directly connected to the common DC bus. As a result, it is possible to observe a variable distribution voltage level that depends on the PV generation throughout the day **[FRE15]** (Figure 1.13).

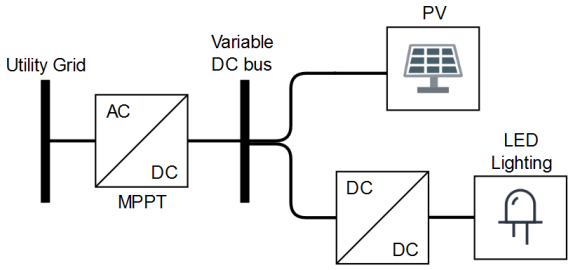

Figure 1.13: Variable bus voltage DC microgrid (BOSCH)

1.4.3. Number of different voltage bus

- Single bus:

This topology is composed by a unique DC common bus, therefore, there is only one distribution voltage level (DC side of Figure 1.5). It is certainly the most current architecture in the literature, even for real experimental projects **[WEI15, BOE15]**. In general, for distribution grids, it is the most profitable architecture, since the diversity of loads is high, and it is more economically viable to have a single voltage and low-power load-associated DC/DC converters that adapt the distribution voltage level in function of load requirements.

- Multiple bus:

In the context of a more specific scenario, this topology is composed by more than one DC bus, and consequently there is more than one voltage been distributed. This configuration can be envisaged, for example, in the presence of microgrid clusters to improve flexibility, reliability and availability.

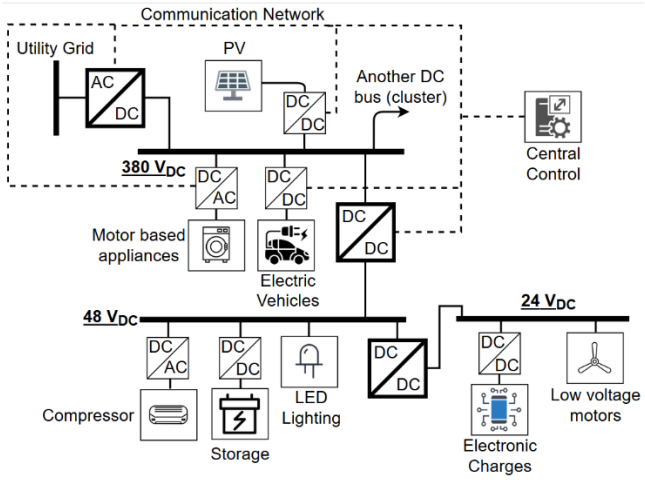

Figure 1.14: Three-level LVDC Distribution Architecture

In this scenario the power flow can be managed through the control of the voltage level in each interconnexion point **[DIA16a]**. It becomes profitable to have this type of structure when there are multiple supply-equivalent loads connected to the grid. In this case, the mutualization of a DC/DC conversion step may justify the investment in the infrastructure of an additional distribution bus. It can be the case for new $48V_{DC}$ USB-C powered devices for bureau/household appliances or LED lighting for example. A three-level architecture can be imagined in this case **[DRA14]**: $380V_{DC}$ for high power appliances, 48V for medium-power appliances and $24V_{DC}$ for low-power appliances (Figure 1.14).

1.4.4. Type of distributed energy

- Full DC:

A full-DC distribution is the denomination adopted here to describe a distribution system that uses DC in the entire power chain: public distribution and internal distribution. It remains an unusual architecture, since, as already discussed, the movement towards DC distribution systems seems to be starting from a downstream point of view, for only then evolve to a full DC model.

- Hybrid AC/DC:

The term hybrid AC/DC distribution is used here to describe a distribution system that uses both AC and DC at some point in the power chain. Here, three subdivisions can be highlighted:

- Public LVAC with internal LVDC distribution system: it represents the most used architecture among the studies and experimental demonstrators. It seems to be the most economically pertinent infrastructure for the current state of the maturity of the multiple technologies associated to distribution systems (distinction shown in Figure 1.7).

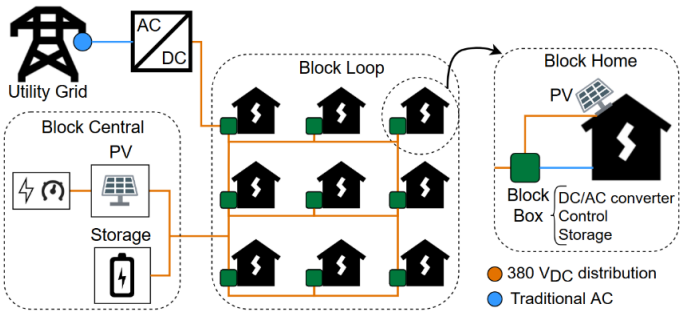

Figure 1.15: KAFB military base representative scheme

- Public LVDC with internal LVAC distribution system: a small-scale example of this type of hybrid architecture is the Microgrid project at Kirtland Airforce Base (KAFB-USA) developed by Sandia National Laboratories and Emera Technologies [SAND2019-11746O]. In this project, the main distribution system operates in DC to improve energy efficiency associated to PV generation and storage. However, internally, each home operates with traditional AC (Figure 1.15) due to the better compatibility with appliances available in the market.
- Parallelized LVAC and LVDC distribution system: in this case, both the AC and the DC infrastructure are available. It can be used for cases where there are both DC and AC loads and sources. It allows to exploit the advantages from both systems, parallel connection of sources in DC and protectability in AC for example [**NAL23**].

1.4.5. Configuration of the distribution grid

- Radial: This configuration is the simplest one in terms of infrastructure, maintenance, power flow and protection management. It corresponds to the way classic LVAC distribution systems are generally deployed. Figure 1.16 illustrates the radial configuration.
- Ring: In this architecture loads and sources are disposed through a loop-like distribution system, in such a way that there are always two points of access to the distribution grid (Figure 1.17). In comparison to radial grids, ring-based systems are more reliable and have a higher efficiency regarding consumption of local RES generation [**HAT20, HAT22**]. Nonetheless, the cost associated to maintenance, control, protection and infrastructure is higher as well.
- Meshed: This structure can be defined as multiple ring-shaped grids disposed in a nested configuration (Figure 1.17). It's the most complex structure, in terms of infrastructure, maintenance and management but it is the most reliable and flexible as well [**PIR23**].
- Interconnected: Local distribution systems of anyone of the previous architectures can be connected to others in the proximity, creating the denomination of interconnected distribution system [**PIR23**]. This architecture can be deployed to optimize the power flow, the equilibrium between local consumption and local generation, and the reliability of the distribution grid. In addition, having more than one connection to the AC grid may be useful to ensure proper operation when generation through RES is not enough to supply loads.

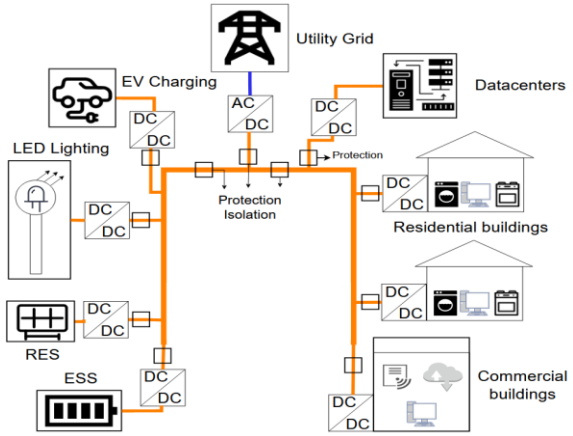

Figure 1.16: Radial LVDC distribution grid

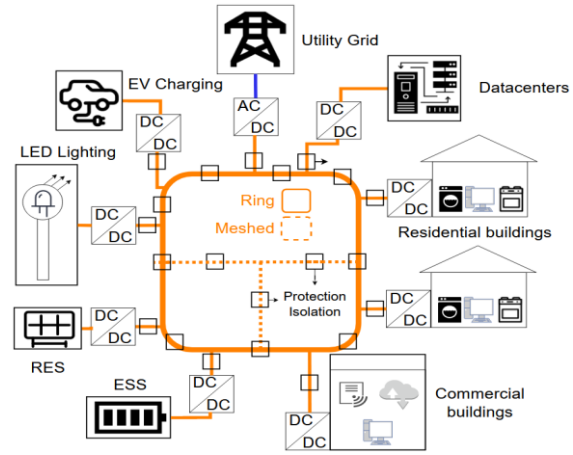

Figure 1.17: Ring-based and meshed LVDC distribution grids

1.5. Standardization in the LVDC domain

In the two previous subchapters, many possibilities were discussed regarding the use of DC for distribution systems in different architectures. However, their technical feasibility depends as well on regulations. Standards represent a common, globally spoken language between manufacturers, DSOs, grid designers and electricians. Their main objective is to establish uniform applicable rules for all the subdomains involved in a distribution system, such as: protection, voltage levels, insulation, physical installation, conductors, etc. Consequently, standards bring a concrete sense of reliability to enterprises or facilities thinking on adopting a DC-based energy supply and profiting from its benefits. For this reason, it seems important to look for available standardization supporting the deployment of LVDC systems.

1.5.1. Existing standards and guidelines

In terms of international standardization, the major reference for electrical power systems is the International Electrotechnical Commission (IEC). It is organized around different Technical Committees (TC) or Sub-Committees (SC) and their respective association of Working Groups (WGs). Regarding IEC standards, there is a list of standards that address LVDC systems, even if they are not specific to the DC world.

Other organizations such as the Institute of Electrical and Electronic Engineers (IEEE), the European Telecommunications Standards Institute (ETSI), the International Telecommunication Union (ITU) and the National Fire Protection Association (NFPA) also have standards covering some aspects of the LVDC domain.

Some technical notes have already reviewed and regrouped a large number of standards with a connection to LVDC systems [**IEC17a, CIR21**]. Table 1.4 shows some of the most relevant and already existent standards, technical reports, and guidelines in the subject.

Table 1.4: Existing standards around LVDC domain

Standard	Focus	Important aspects
IEC TR 63282	Voltage levels and Power Quality (PQ) phenomena	Recommendation of LVDC distribution voltage level and definition of PQ parameters
IEC 60364	Private LV electrical installations for buildings	Protection requirements and earthing systems in LVDC
IEC 60947	LV switchgear and controlgear	Specification for different types of protection devices in LVDC
IEC 61000	Electromagnetic Compatibility (EMC)	DC ripple evaluation and measurement
IEC 61660	Short-circuit currents in d.c. auxiliary installations in power plants and substations	Calculation methods for cable modeling and short-circuit currents magnitude
IEC 62477	Safety requirements for power electronic converter systems and equipment	Recommendations for protection and control of rectifiers
IEEE P2030.10	DC Microgrids for Rural and Remote Electricity Access Applications	General designing recommendations for DC microgrids
NFPA70	National Electrical Code (USA)	Rules for DC earthing systems, PV installations and EV recharge
ETSI EN 301 605	Earthing for 400VDC data and telecom equipment	Rules for respecting high levels of EMC

1.5.2. Progress in the development of future standards

Considering the state of the art of existing standards, the first established fact is that the environment around LVDC distribution lacks regulations in many directions **[DIA15, DIA16a]**. In this way, several of the existing standards only cover specific use-case scenarios. There are no definitive rules in terms of DC voltage levels, installation procedures, protection devices or power quality aspects. These basic standards are an essential key to the future development and deployment of LVDC distribution. Motivated by this aspect, the same organizations are already focusing their efforts into making these standards become a reality **[ELS15, KUM17b]**.

The IEC's Standardization Management Board (SMB) started to address the subject through Strategic Group 4 (SG4) which was responsible for "LVDC distribution systems up to $1500V_{DC}$" and was assembled in 2009. IEC SMB/SG4 focused its efforts on subjects like distribution architectures, protection and operation equipment. In 2017 the System Committee for Low Voltage Direct Current and Low Voltage Direct Current for Electricity Access (SyC LVDC) was formalized through a first plenary meeting. Transversally regrouping the expertise of multiple TCs and SCs, its objective is to provide guidance and coordination for the development of future standards in the LVDC domain. A

non-exhaustive list of the multiple contributors of the SyC LVDC can be found in their Strategic Business Plan (SBP) [**IEC22**].

In addition, two pre-standardization organizations must be highlighted as well: the CIGRE (Conseil International des Grands Réseaux Electriques) and the CIRED (Congrès International des Réseaux Electriques de Distribution). The CIGRE is recurrently addressing the subject through its Study Committee (SC) B4 on DC Systems and Power Electronics and SC C4 on PQ analysis in the energy transition. On its turn, the CIRED is also looking into the subject through its WG 2019-1 on DC Distribution Networks. Through both organizations, state of the art reports, as well as technical analysis and recommendations for future standards were already presented [**YAN22, CIR21**].

1.6. LVDC ecosystems around the world

It is possible to observe that the standardization community has already identified the need to progress and to boost the development of regulation in the LVDC domain. Along with it, there are other para-regulatory organizations around the world which are providing experience feedback and technical recommendations for the use of LVDC in different niches. The most relevant initiatives are happening in Europe, in the United States of America (USA) and in China.

1.6.1. Europe

In Europe, the environment around LVDC is getting more and more dynamic during the last decade. In this context, there are two countries that must be highlighted regarding their presence in the LVDC world: Germany and the Netherlands. Coming from different environments, some key organizations from both countries have very similar objectives, even actively working together in standardization, technical meetings, and conferences. Without going directly into a technical analysis, it seems important to investigate their work.

In Germany, the first organization contributing to the development of LVDC systems was the ZVEI (German Electrical and Electronic Manufacturer's Association). Representing more than 1600 companies from different fields, they created two consortium research projects, DC-INDUSTRIE 1 from 2016 to 2019, and DC-INDIUSTRIE 2 from 2019 until present. combining multiple expertise to establish solid knowledge around LVDC distribution grids, with a special focus on the industrial domain. DC-INDUSTRIE 2 was funded by the German Federal Ministry for Economic Affairs and Climate Action since the use of DC may bring energy efficiency advantages over classic grids. Recently, the ZVEI founded the Open Direct Current Alliance (ODCA), bringing along 33 industrial partners, and several academic partners as well. Their objective is to provide technical knowledge and solutions around the DC technology, in order to contribute to the worldwide use of DC distribution grids.

On the other way, in the Netherlands a company called DC Systems (founded in 2009) were the first in the country to propose integrated solutions (power supply, protection, and electrical equipment) for LVDC. Recently, in 2020, DC Systems was bought by Schneider Electrics expanding its domain, influence, and expertise in the field. Along with EATON, they founded the Current OS foundation, whose objective is to regroup a set of rules as a unified standard for DC microgrids. In contrast with the German initiative, Current OS is focusing in residential, commercial, and public lighting domain.

Even if the focus of both initiatives is slightly different, the main objective of both organizations converges to using LVDC in distribution systems with the objective of increasing their level of

controllability, compatibility with loads and integration with RES and ESS. The main characteristic of the solutions proposed by these organization will be presented thereafter.

1.6.1.1. DC-INDUSTRIE and ODCA

Before the foundation of ODCA, the second part of the DC-Industry project launched an extensive document, in which their main strategy was presented [**DCI22**]. Their proposition of using DC in industrial grids comes from the fact that, in modern installations, around 70% of the electrical energy is consumed by electric motors. Many of them are controlled by variable-speed drives (VSD), which have an intermediary DC bus. Added to the possibility of local generation through RES (notably PV), it becomes interesting to connect everything through a DC distribution system, avoiding unnecessary AC/DC conversion stages.

Technical recommendations presented by DC-INDUSTRIE 2 focus on the Industry 4.0 concept and aim to create an open and scalable system in LVDC (400-800V_{DC}), considering both bus-type and ring-type grid topologies. The concept of distribution grid they are exploring is based on DC sectors, which consists in regrouping similar equipment and appliances based on technical characteristics. The basic structure of the distribution grid can be observed in Figure 1.18.

A DC sector is connected to the main 650V_{DC} bus through a DC breaker, which has two compulsory functions: overcurrent/short-circuit and line protection. It may also have other roles, such as isolation, pre-charging, discharging, protection against ground fault, and protection against under and overvoltage. The proposed configuration also ensures that a fault inside the perimeter of a DC sector may cause operational dysfunction in other equipment belonging to the same DC sector, but never elsewhere.

In terms of the management of the grid, a hierarchical control system is suggested and consists of 4 stages: participant management (inner), power flow management, source management and energy management (external). The first two control loops are executed for each equipment through a decentralized strategy. It consists in regulating the output current of each device based on the locally measured DC voltage level using characteristic curves (voltage-current droop control). Both the external loops are not imperative for grid stability and need a communication system to operate. They are responsible for other grid functions such as maintaining the state-of-charge of ESS or optimizing local consumption without importing energy from the utility grid.

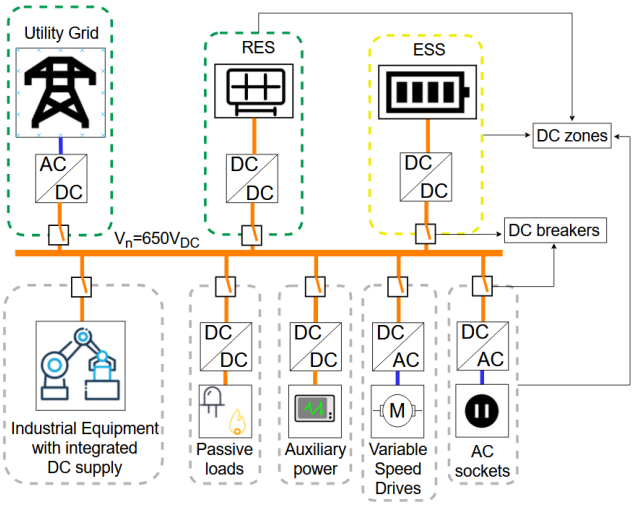

Figure 1.18: DC grid structure proposed by ODCA

Some other important recommendations following the same system concept are also made by DC-INDUSTRIES technical report, regarding mainly operation voltage bands, grounding systems, protection, Electromagnetic Compatibility (EMC), and grid stability. More detail on their protection scheme, protection devices and EMC recommendations will be discussed further on in Chapter 2. Since the other subjects are not the focus of this research, additional detail on them will not be presented here.

The system architecture, which was briefly discussed in this subject, was already implemented in real facilities and demonstrators. Among the most important ones are the Mercedes-Benz Factory 56 in Sindelfingen, the Fraunhofer IISB demonstrator in Erlangen and the BWM Group plant in Dingolfing, all of them in Germany.

1.6.1.2. DC Systems and Current OS

Analogously to the German initiative, DC Systems, along with the Current OS foundation, already presented details on technical recommendations about their concept of LVDC grids [**DCS22**]. Motivated by the power capacity saturation of electrical grids in the Netherlands, their main goal is to create a standardized LVDC environment to support the integration of decentralized RES generation and the development of microgrids. Through the foundation, their objective is to provide clear guidelines for manufacturers to develop products which are compatible with their protocol. While, ODCA has an open strategy for different technologies of converters or protection devices for example, Current OS provides a complete, integrated, and closed solution with a catalogue of Current OS-compatible devices. Among them, it is important to highlight: a 350/700V_{DC} IC which is responsible for managing the AC/DC interconnection link; the Current Router, which is a complex solid-state protection device with multiple functions; DC/DC converters for 48V_{DC} 240W USB-C applications.

In terms of grid management and stability, Current OS suggests a similar strategy as OCDA, based on decentralized voltage-power droop control. On the other hand, voltage bands are different. Their concept of LVDC microgrid is available for 350 or 700V_{DC} in terms of nominal voltage. Respectively, voltage levels may vary from 250 to 540V_{DC}, and from 500 to 1080V_{DC}. A rough approximation of their control strategy through droop curves and voltage bands is shown in Figure 1.19.

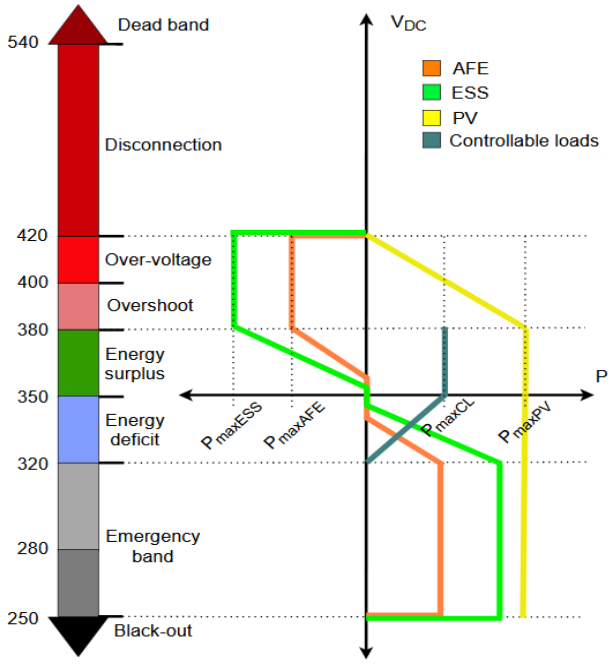

Figure 1.19: Voltage-power droop control for LVDC grids operation by Current OS

Since the voltage in the DC grid is a mirror of the equilibrium between the available production and consumption, it is possible to observe that for the AC/DC IC for example, its power remains at zero when voltage is around the nominal level. When voltage variates beyond a certain level, either the IC is feeding the AC grid from the DC grid (energy surplus), or it is feeding the DC grid from the AC grid (energy deficit). In the other hand, PV generation is always at its maximum power and is not modulated by droop control unless voltage level grows beyond normal operation bands. Finally, for non-critical controllable loads, such as EV charging, it is also possible to modulate its operation through droop control, where the power is progressively reduced as voltage levels fall.

Another important aspect of the protocol provided by current OS involves protection schemes. The proposed solution is based on specific grounding systems, solid-state protection devices, safety functions for maintenance and a zone strategy. More details regarding this subject will be presented in Chapter 2.

The protocol from DC Systems has already been implemented in some real applications. The two most relevant examples are a DC-powered commercial building named Circl in Amsterdam, and a 5km DC-compatible provincial road (N470) equipped PV, ESS, DC-powered traffic lights and public lighting in Delft.

1.6.2. USA

The main driver of LVDC and hybrid AC/DC distribution grids in the USA is the EMerge Alliance. They are an open industry association, with different industrial, academic and regulation-related partners. Among them there are institutes of technology, products manufacturers, system designers and international standardization organizations. The association is actively working towards the development of standards in the LVDC domain. A list is presented in Table 1.5. From their perspective, the use of DC in distributions systems is based on a triad of benefits: resiliency, sustainability and energy saving.

Regarding the available standards, the first one is denominated EMerge Alliance Occupied Space Standard (version 2.0), it establishes structural parameters to an internal LVDC distribution of $24V_{DC}$ for buildings, as well as it proposes a set of compatible devices that are available in the market. The second standard is called EMerge Alliance Data/Telecom (version 2.0), it defines a hybrid AC/DC power infrastructure for Data centers and telecom offices with a DC distribution voltage level of $380V_{DC}$. The last one defines operation characteristics for DC meter, in terms of EMC and voltage/current measurements.

Table 1.5: Standards developed by EMerge Alliance

Already available	Work-in-progress	New propositions
Occupied Space	DC and hybrid microgrids	AC/DC dual input appliances
Data/Telecom Center	Microgrid Interconnection	DC circuit protection
ANSI DC metering		DC microgrids connectors

The philosophy behind EMerge Alliance is that the technology to build DC or hybrid AC/DC grids already exists around the world, and what is lacking is the know-how on the coordination and regulation of the use of this technology. In this way, they are constantly promoting workshops and creating partnerships to build the know-how around the domain through education and cooperation. Along with the National Renewable Energy Laboratory and the Lawrence Berkeley National Laboratory, Emerge Alliance worked in a project funded by the U.S. Department of Energy, in which

the focus was DC grids for buildings. More specifically, they aimed to investigate the technical challenges associated to the use of DC and to develop metrics to evaluate performance in these systems [**BRO17**].

Apart from Emerge Alliance, the LVDC ecosystem in the USA is quickly evolving and other actors are already contributing to its development. The Clean Energy Research Center Buildings Energy Efficiency is working on quantifying energy savings associated to the use of DC as well as in an optimized way of managing power in DC grids. Other private initiatives are also present. Among them it is possible to highlight the concept of DC Home developed by Next Energy and the DC microgrid by Honda, in Texas, California, which is the largest DC microgrid in North America [**BEC15**].

1.6.3. China

The most part of experimental demonstrators, publicly funded projects, and permanent fully operational facilities in the LVDC domain are in China. Motivated by global environment issues and with the objective of reaching carbon neutrality through RES, an important ecosystem around LVDC is getting built in China. With a lot of investment from the Chinese Energy Foundation, there are more than 20 LVDC demonstrators currently operating in the country [**MA23**]. With a diversity of use-cases, there is a strong effort to integrate EV charging stations, LED lighting, large amounts of PV generation and batteries in the most recent architectures of DC distribution grids.

Compared to the USA or the European market, DC-compatible equipment is more mature in China. There are demonstration projects such as the one in Ruicheng, in the Shanxi Province, where a DC grid feeds multiple Smart-Home sand several household appliances are directly supplied in DC. Another example, is the project in the district Xiong'an, where a distribution system of an entire village will be deployed in LVDC [**MA23**], including residential and commercial buildings, offices, hospitals, etc. The main objective with this type of projects is to improve existing standards providing field technical feed-back and boosting the commercialization of DC-compatible equipment. It is possible to see that LVDC projects and demonstrators in China have already surpassed the status of proof-of-concept, achieving larger scales through the use of technology which is rapidly becoming mature.

In terms of regulation, the development of national standards is very ahead of the rest of the world as well. In 2020, the latest version of the GB/T 39462 Chinese national standard was launched, in the subject of safety requirements for LVDC. In the same direction, in 2022, another national standard was released, the T/CABEE-030 standard which covers many design requirements for DC buildings, taking into consideration protection equipment, power electronics and grid management for example.

1.7. Distribution voltage level

Among the multiple subjects evaluated by standardization and pre-standardization organizations, one of the most important one is the choice the distribution voltage level. It has an impact in almost every aspect of the infrastructure of a distribution system: insulation, conductors, converters, protection devices, PQ analysis, etc. Consequently, it seems important to investigate the subject and what has already been proposed.

1.7.1. Existing standards

The most part of the standards recommending the adoption of a certain voltage level are related to specific applications: telecommunication, Data centers or rural grids [**IEE21**].

Table 1.6: Voltage recommendations

Voltage between lines (unipolar) or line and midpoint (bipolar)		
U_{nom}	**U_{min}**	**U_{max}**
350V	320V	380V *
		440V **
700V	640V	760V
Voltage between lines (bipolar)		
U_{nom}	**U_{min}**	**U_{max}**
±350V (700V)	±320V (640V)	±380V (760V) *
		±440V (880V) **
±700V (1400V)	±640V (1280V)	±750V (1500V)
* Commercial facility ** Non-commercial facility		

However, there are also some advances in the conception of a wider and more global standard. The technical report IEC TR 63282 [**IEC20]** that was already cited here, presents some recommendations concerning voltage levels, which are summarized at Table 1.6.

1.7.2. Results issued from scientific publications

Considering that there is some progress yet to be done in the standard domain, it seems important to investigate academic studies and their conclusions. They represent another side of the effort to construct solid knowledge to support further research and experimental projects.

The voltage level around $380V_{DC}$ is already used in many telecommunication-related facilities such as Data centers. The experience feedback obtained from this domain is the main reason why many authors **[FRE15**, **VOS14, BOE15, GER18]** chose to adopt a similar voltage level in their studies. In addition, $380V_{DC}$ correspond to the internal voltage of many high-power appliances **[BRE16]**, which can be supplied by bipolar lines **[WEI15]**.

In the case of a DC distribution system connected to a DC public distribution grid, it is possible to imagine a higher voltage level, such as $750V_{DC}$ or $1500V_{DC}$ to maximize efficiency. For similar voltages, in the literature, there are also some more innovative architectures, such as a double bipolar line **[DIA16a]**. As shown in Figure 1.20, the first distribution line has one of its poles converted into another bipolar distribution line through a DC/DC converter.

In the case of internal residential or commercial distribution systems, the loads generally require a lower voltage level. A $48V_{DC}$ or $24V_{DC}$ distribution could be a standard for lighting and low-power appliances, but those levels should be restricted to small-sized spaces, because of the high losses associated with using a very-low voltage level. In the same way it is also possible to imagine the use of a $120V_{DC}$ distribution. This level could be chosen because it represents the boundary for Separated Extra-Low Voltage (SELV) and Protected Extra-Low Voltage (PELV) systems, conforming to

IEC61140. In **[WEI12b]**, authors show that only 0.3% efficiency gain is achieved when passing from a distribution voltage level of $120V_{DC}$ to $240V_{DC}$. In practice, it means that the efficiency gain may not be worth since a higher voltage level would imply the use of a more expensive protection devices.

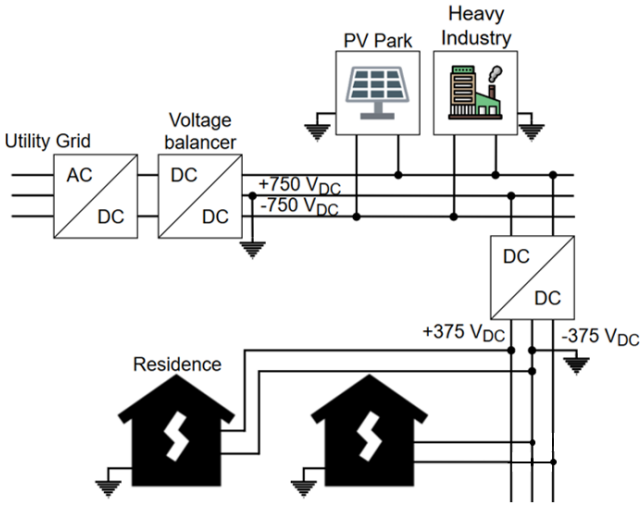

Figure 1.20: Double bipolar LVDC distribution architecture

There are also other studies that compare multiple voltage levels, and their results represent an important starting point for further research **[ANA10, DIA16a, MOU19].** Generally, three different voltage levels are recommended, depending mostly on the characteristics of the final loads. For low power appliances, such as electronic devices and IT-equipment in small offices or single rooms, the most recurring recommendation is to use 24 or $48V_{DC}$. A voltage level of up to $450V_{DC}$ (usually around $350V_{DC}$) is recommended for medium power, to provide a link to small or medium renewable energy sources and to feed office buildings. For LVDC distribution systems that interconnect high power energy sources with industrial facilities and large buildings, the recommendation is a voltage level up to $1500V_{DC}$ ($750V_{DC}$ bipolar for example).

Finally, a summary of some of the available standards and codes regarding the voltage level in the DC domain, as well as some DC-based applications is also proposed in Figure 1.21.

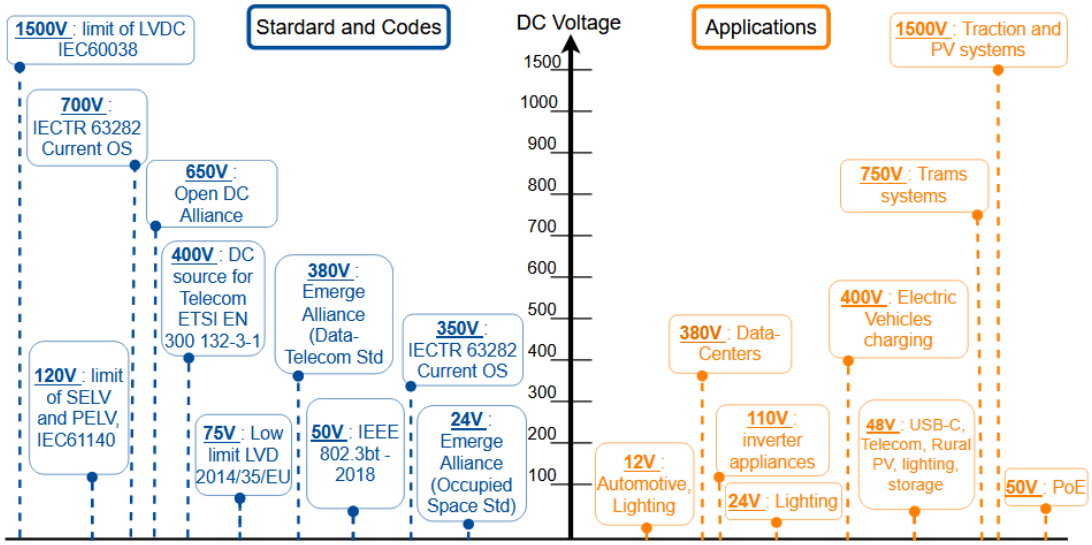

Figure 1.21: Standards for DC voltage levels

It is possible to observe that the choice of the voltage level is deeply connected to the requirements of the loads fed by the distribution system. When developing a public LVDC distribution architecture, it is crucial to take into consideration the different types of voltage level compatibilities at a consumption level. It is also very important to consider the impact of the adopted voltage level in the protection devices associated to the system.

That said, it is possible to imagine different options, regarding the voltage levels throughout the entire distribution architecture. However, the most adopted voltage levels by the literature for LVDC distribution in studies and real applications are within the 350-400V_{DC} range for low-power and 650-750V_{DC} for high-power. This is because it represents a good trade-off between protection, efficiency, and infrastructure costs. In addition, there already exist standards and equipment in the market designed for this voltage level range.

Finally, considering a public distribution, the adopted voltage level also must be evaluated through an economic point of view. For the power system operator, the best solution is to select a distribution voltage that is compatible with the electrical conductors that are already in operation with LVAC. In the United Kingdom, for example, the most used LVAC cables are rated for 600V_{AC} (phase-to-ground) and should withstand at least 849 V_{DC}, which is the peak value of the AC voltage [**ANT13**].

1.8. Conclusion

In the last few years, hybrid AC/DC grids emerged as a new concept for facilitating RES and ESS integration in the distribution system. In addition, the exponential growth of DC-based electronic consumption, through EV, electronic loads, VSD controlled motors and LED lighting is driving the development of the environment around LVDC systems.

It is possible to observe that the use of DC in future architectures of distribution grids brings multiple advantages, regarding energy efficiency, controllability, and resiliency. Energy saving is feasible through the mutualization of multiple AC/DC conversion steps through a central converter, associated to the absence of dissipative effects in DC. In addition, the absence of synchronization issues and the facility to control de power flow in the grid grant an enhanced sense of reliability to LVDC distribution grids. DC can be used to deploy different grid architectures, from classic single voltage radial structures to complex multi-bus distribution systems. Another advantage of LVDC is that architectures such as bipolar or ring-based, are easily deployed with the same infrastructure in terms of conductors as in AC but ensure a higher level of reliability.

Different ecosystems around the world are already exploring these advantages in order to build systems concepts, demonstrators, experimental projects through several alliances and cooperation agreements. Nonetheless, it is possible to observe that standardization and regulation around the LVDC domain still has a long way to go. Even if, the domain of voltage levels is beginning to reach a common ground for international standardization organizations, there are other subjects that must still progress. It is the case of EMC and power quality recommendations, power electronics operation and protection schemes for example. These three aspects are identified as vital for the future development of hybrid AC/DC distribution grids. As so, they will be the focus of the Chapter 2.

Chapter 2. KEY ASPECTS FOR THE DESIGN OF LVDC DISTRIBUTION GRIDS: POWER ELECTRONICS, PROTECTION, AND POWER QUALITY

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2.1. Introduction

This chapter focuses on three aspects that have a major importance in the domain of LVDC distribution systems, which are power electronic converters, protection strategies, and power quality. The objective is to present a review, from equipment and system points of view, on what possibilities exist regarding these three aspects, in order to conceive a distribution system that can operate properly.

In section 2.2 a discussion around different converter topologies is presented. A main distinction is made between two different categories of converters: non-isolated converters and isolated converters. Technical details about the advantages and drawbacks of each group of converters will be presented along with some of their most important operation characteristics. At the end of this section, the behavior of each converter under short-circuit is analyzed, which is useful for the choices made in Chapter 3.

Section 2.3 presents two of the main challenges associated to protection schemes in LVDC, which are selectivity rules and the protection against electric shock. A set of DC protection devices is analyzed, and different combinations are investigated with the objective of answering the challenges identified.

Finally, section 2.4 explores the domain around power quality, with a focus on different related phenomena and how they can be characterized in LVDC distribution systems. A fundamental distinction is made between transient and steady-state phenomena, which allows a first classification of PQ indicators. This section ends with a reflection around possible solutions to ensure high power quality levels in a distribution grid.

2.2. Power electronics for LVDC distribution grids

For the different architectures of hybrid AC/DC distribution grids explored in Chapter 1, the most part of them considered at least one connection to an AC utility grid. In addition, in most cases the AC/DC interlink represents the most robust and powerful conversion structure in the grid. It is responsible to manage the energy exchanges with the AC infrastructure, as well as it is the structure with the most important role to maintain grid stability. The local presence of ESS can contribute to it, however the AC/DC IC has the major control functionalities, and it is also responsible for other important features of the distribution grid, such as the earthing system, galvanic isolation from the AC grid when needed, and others.

Given the importance of ICs, this section will survey different topologies of power electronic converters, which can be used to deploy a hybrid AC/DC distribution grid. The main operation characteristics of each structure is detailed further on. The objective is to provide a clear view of the advantages and downsides of each topology.

Considering that hybrid distribution grids do not have bulky short-circuit capacities and that it may be interesting to be able to use functionalities such as black start and reactive power control, LCC-type topologies do not seem to be adapted for the scenarios explored here. This analysis focuses on VSC topologies, which can bring such control capacities [**ONI16**].

A first important difference of the multiple topologies of power electronics converters distinguishes those that do not have an integrated galvanic isolation from the ones that do have it. Consequently, it is possible to determine two families of converters, which are studied in the next sections.

2.2.1. Non-isolated AC/DC voltage-source converters

Non-isolated converters do not have a transformer integrated in their topology and the converter AC side is not isolated from the DC side. However, it does not mean that no transformer can be used. If needed, the converters which will be presented next can be associated in cascade with a classic transformer. Here the concept of classic galvanic isolation is applied to describe the employ of a low-frequency (50/60Hz) transformer to physically interrupt the conduction path between two parts of a distribution grid. In practice, this is useful when a dissociation between the AC and the DC earthing systems is needed. In addition, for the concept of hybrid AC/DC distribution grid explored here, an input transformer is usually needed as well to step-down the AC voltage. In fact, the control system of VSC topologies can only operate properly when the DC voltage is higher than the AC peak line voltage, which is around 565V for classic triphasic systems with a 230V phase voltage. That is because, if the DC voltage is low than this value, the reverse diodes are directly polarized, and the converter behaves like a passive rectifier. Since one of the recommended voltage levels for DC distribution is around $350V_{DC}$, as already mentioned in Chapter 1, AC input voltage may need to be decreased.

Even if low-frequency transformers are a simple and well-known technology, they need high volume magnetic cores and a high number of turns in the winding to avoid the core's saturation in terms of magnetic flux density. Consequently, these transformers have a low power density, which means their power-volume and power-weight ratio is low [**DIN17, IQB22**]. In practice, it means that for the same electric installation, low-frequency transformers will occupy more space than other options such as medium-frequency transformers, which may be a problem when an already sized AC facility is converted to DC.

That being considered, there are different topologies that make part of the non-isolated AC/DC category of converters. The following analysis will be based on the available structures that seems suitable for low-voltage DC distribution grids.

2.2.1.1. Two-level voltage source converter

The two-level voltage source converter represents the most basic topology in terms of power electronics. It is a fully controllable structure since each semiconductor in each of the three commutating cells is capable to be turned on and turned off at any time. As a result, it can regulate voltage or current levels through PWM modulation strategies [**GRA03**]. Aside from the operation voltage level, this converter has the same structure as the one shown in Figure 1.3. It is the most frequent topology for unipolar distribution systems [**FLO07, WAN16**].

This type of converter is usually controlled through a vectorial approach. The Park transform is used to create a rotational based reference in which voltage and current components are DC. As already explained in Chapter 1, it allows the use of simple control rules to regulate voltage and current, as well as the dissociation of the active and reactive power control. The main advantages of this topology are its simplicity, low number of semiconductors, and high level of reliability.

2.2.1.2. The Neutral Point Clamped converter (NPC)

The architecture of the NPC converter is presented in Figure 2.1 and, as it can be seen in this configuration, semiconductors are submitted only to half of the voltage in the DC bus due to the voltage being clamped by the mid-point connected diodes [**KIM19**]. This topology becomes very advantageous when considering medium/high-voltage systems or to avoid the need to oversize the semiconductors in terms of breakdown voltage. In addition, it is capable of commutate between 3 voltage levels, $\pm V_{DC}$ and zero. The addition of one voltage level considerably improves the voltage/current harmonic content.

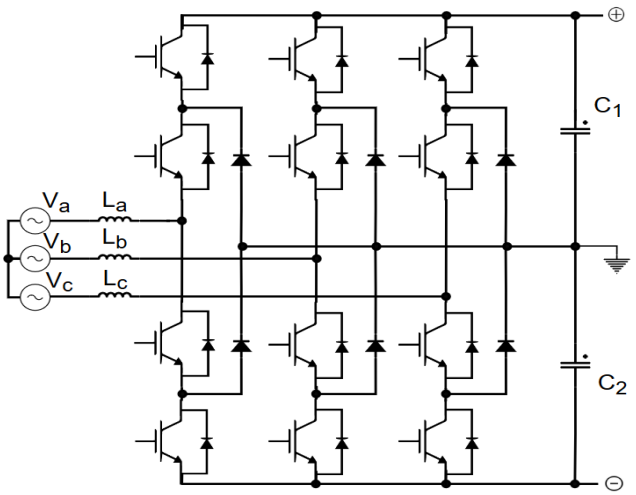

Figure 2.1 NPC topology

The NPC converter has a direct connection to the medium point capacitors, which facilitates their voltage regulation through a similar vectorial control strategy as in the 2-level VSC case. That is the main reason why this architecture is usually chosen to single converter based bipolar distributions **[KAN15, CHO15]**. However, voltage unbalance may require additional active structures (voltage balancer) or special control strategies to ensure the proper operation of the converter, such as zero-sequence injection or additional cascade DC/DC converters [**KIM19**].

2.2.1.3. Modular Multilevel Converter

As already briefly discussed in the first chapter section 1.2.2, the MMC is the most recent architecture of VSC and it is being used in HVDC systems because the DC voltage is divided across each module, resulting in a tolerable voltage stress to which each semiconductor is subjected during commutation. A generic representation of the structure of the MMC is shown in Figure 2.2 MMC topology.

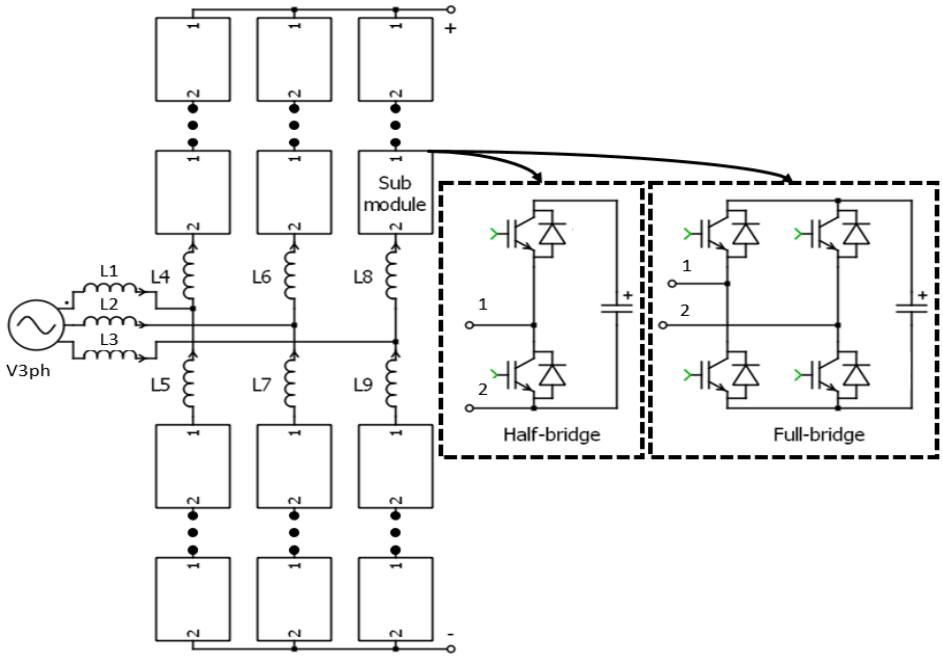

Figure 2.2 MMC topology

Besides, it can generate multiple voltage levels, proportionally to the number of modules in each converter arm. Even though it represents a very expensive solution for LVDC, there are studies in the literature that are suggesting the use of this topology to ensure a high-efficiency and high-power quality supply **[ZHO15, ZHO16, ZHA23].** The full-bridge MMC is also capable of rapidly blocking short-circuit currents **[WAN16]**, which can be a great advantage in terms of protection schemes requirements.

It is, however, the most complex and expensive structure among the topologies analyzed here. The number of semiconductors is high, which may render the modulation and control systems far more complicated than the ones employed in the previous topologies. It also needs a significantly higher number of capacitors, which may represent a weakness in terms of reliability. It can be used in LVDC, but the previous topologies represent a more competitive solution [**CAI17**], which may restrict its use to very high-power quality requiring systems.

2.2.2. Isolated AC/DC converters

In this class of converters, to change voltage levels and to guarantee the dissociation of earthing systems they have a medium or high frequency transformer integrated in the topology, which is interfaced by two conversion stages. The input and output converters can be controlled to feed the transformer medium/high frequency voltage waves, which results in a considerable reduction in passive components size and cost, regarding filters and even the transformer itself [**NAN12**].

Historically, these types of topologies were not used for high power applications since they were less efficient than classic low-frequency transformers and the power electronics needed was too expensive. Nonetheless, more recent designs of converters, optimizing the number of switches and using new semiconductor technology seems to be changing this historical fact [**ISM22**]. These converters are already being proposed as a solution to deploy HVDC systems [**ALE12, BAS14**]. Isolated converters already exist using wide-band gap components [**PNI21**] resulting in more efficient and robust structures. In addition, the association of the transformer with the interlink converters allows the active control of the power flow as well as the improvement of power quality indicators [**SAL19b, SAL19c, MEE20**].

In addition to the volume and potential cost reduction for passive components, these converter topologies can also benefit from additional features, regarding fault management and short-circuit current limitation for example. The global architecture of these converters can be observed in Figure 2.3.

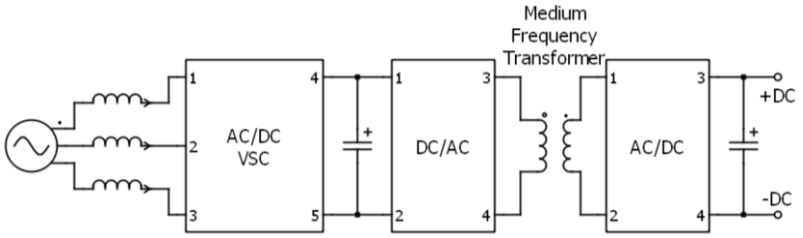

Figure 2.3 Scheme of an Interlink Converter (IC) based on a medium-frequency transformer

Since there are additional active converters in the power chain, many possibilities of control exist. For example, the last two DC/AC and AC/DC stages can be used to control the DC bus directly, in terms of voltage and current, while the VSC can be used to control interactions with the AC grid. All the possibilities created by isolated converters make them a suitable possibility for hybrid AC/DC distribution grids [**SHA21**].

When compared to the topologies using low-frequency transformers, isolated converters impose the association of more than one conversion stage, forming a larger and more complex converter topology. From one this point of view, it represents a reduction in the reliability level. For these topologies to operate as expected, the transformer must have proper designed magnetic cores, with materials that are not submitted to high losses regarding the increase of the frequency. In the same way, in order to keep a high efficiency level, specific conductors must be used in the transformer, since medium/high frequencies worsen the phenomenon of impedance increase caused by the skin effect.

Since the first AC/DC conversion brick is represented in most cases by one of the topologies described in section 2.2.1, next sections focus on the DC/AC/DC conversion topologies.

2.2.2.1. Single Active Bridge (SAB)

The SAB is a unidirectional topology which is composed by an active full bridge structure in the primary side of the transformer and a passive full bridge in the secondary side. In this type of topology, the transformer does not need to be fed with sinusoidal voltage waves. Since they are designed to operate in medium/high frequencies, in most of the modulation and control strategies, the active bridge imposes square-shaped voltage waves to the primary side of the transformer. Figure 2.4 shows a SAB topology and illustrative shapes of voltage wave in the input of the transformer. Among the most applied modulation techniques, there is the Duty-Cycle modulation (DCy) and the Phase-Shift (PS) modulation [**COE21**].

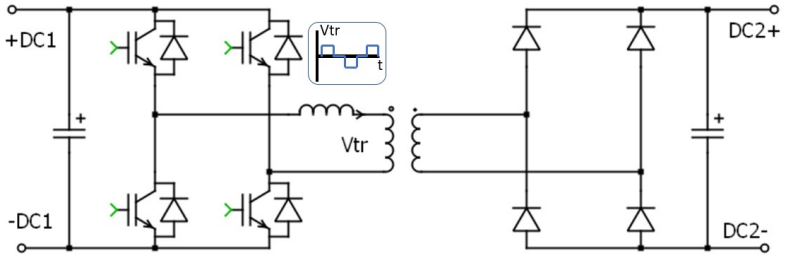

Figure 2.4 SAB converter topology

The SAB is a very simple structure in terms of power electronics and control system. Both voltage and current can be regulated by simple PI controllers in classic cascade operation [**BAL23**]. Consequently, it is robust and the cost to its implementation is low. As it will be seen in the next subsection, another advantage of this topology concerns its active ability to manage faults. Due to the active bridge being configured in buck-like operation mode, the SAB is able to actively manage a fault in the output DC side (DC2) and to limit the short-circuit current [**CAI17, HAR15**].

It is important to highlight as well that the SAB can also be controlled to achieve turn-on soft switching in the active bridge. Soft switching is a technique in which active semiconductors can be commanded to modify its state (ON to OFF, or OFF to ON) when either voltage or current are zero. With this technique it is possible to improve the efficiency of the converter by reducing commutation losses, since there is no power being dissipated. When voltage is zero, the process is called Zero Voltage Switching (ZVS), while when the current is zero, it is called Zero Current Switching (ZCS). In the case of the SAB, it is possible to achieve ZVS at the turn-on stage of the active switches [**TIN13**]. If no soft switching is achieved, the state change is called hard switching and commutation losses exist. illustrates the case of the SAB, where turn-on stage operates in ZVS, and the turn-off stage is hard commutation.

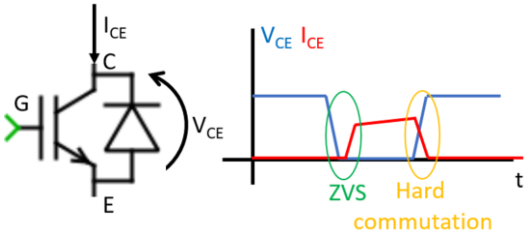

Figure 2.5 Commutation in the SAB

However, due to the second bridge operating as a passive stage, the control strategies are limited. In reality, there is only one degree of freedom to regulate voltage and current waves [**JHA22**], which is either the duty cycle or the shifting angle of the square waves generated by both active arms of the SAB. Due to its unidirectional characteristic, its possible applications include the AC/DC interface of EV charging stations, wind turbines or unidirectional hybrid distribution systems, where exchanges with the AC utility grid are not possible or desirable.

2.2.2.2. Dual Active Bridge (DAB)

The DAB is the bidirectional version of the SAB with two active H-bridges at each side of the transformer. This converter is slightly more complex than the SAB, having 4 additional controllable switches, but it remains a good trade-off between new functionalities and reliability. Figure 2.6 presents the DAB topology.

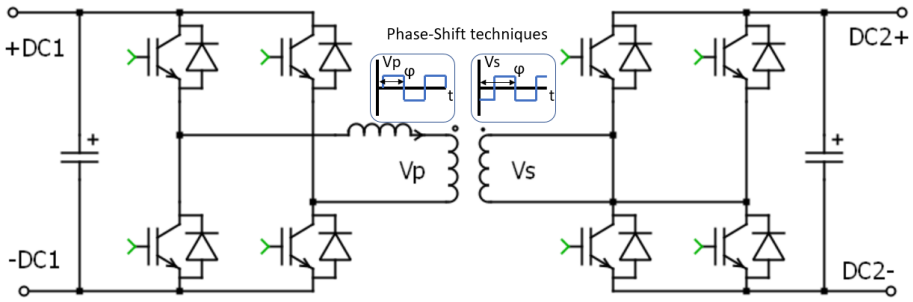

Figure 2.6 DAB converter topology

Since it is made of completely controllable switches, there are more possibilities in terms of efficiency, degrees of freedom, control and modulation strategies. Regarding modulation techniques, there are five types of systems which are the most used in the DAB: the Half-Passive (HP), the Single Phase-Shift (SPS), the Double Phase-Shift (DPS), the Extended Phase-Shift (EPS) and the Triple Phase-Shift (TPS) [**ALH20, HOU20**]. In the HP modulation, depending on the power flow direction, one of the bridges is commanded to operate as a fully passive structure and the topology becomes equivalent to the SAB. All other four modulation strategies use both active bridges to manage the power flow.

It is by far the most employed basic brick in DC/DC, AC/DC or AC/AC conversion structures. The DAB has recently been proposed as a power electronics solution to LVDC grids [**CAI17, WAN22, KUM17a, MAL22, NAN13, SHA21, IQB22, LI21, LAI23**], E-mobility [**ALH20, SHA21**], PV production [**ALH20, ALA17, GEO15, SHA21**], wind turbines [**ALH20, SHA21**], storage systems [**ISL17, KAR18, GEO15, SHA21**], MVDC interconnections [**ALH20, MAL22, IQB22, DWO22, LAI23**], DC railroad power supply [**VER19, SHA21**], and Shipboard applications [**ISM22**].

As it can be observed, significant research is being conducted using DABs to deploy converters in many different applications, especially as an interface for RES interconnection and to deploy LVDC

grids originating from an AC or DC upstream power grid. Concerning protection aspects, the DAB performs better than the SAB. It can actively manage faults in both DC sides depending on the power flow. The first H-bridge can be controlled to limit the short- circuit current in the opposite DC side and vice-versa [**CAI17, HAR15**]. A final advantage of this topology is that it can reach soft switching operation for all switches. Depending on the operation point and through different strategies involving modulation, control techniques and passive components design [**ALH23, LAG18, VER19, COE21, SHE09, CAL16**], the DAB can even reach ZVS and ZCS.

The Resonant Double Active Bridge is a variation of the DAB, in which a resonant circuit is design to create sinusoidal or quasi-sinusoidal current waves at the medium/high frequency transformer [**PAV12, ARA18, ARA20**]. Among the possibilities of creating a resonant circuit in the AC side of the DAB, the most used technique is to design a Series Resonant Circuit (SRC) through the addition of a capacitor in series with the transformer [**DUY15, HAM22, HU19, PAV12, NAM20**]. Figure 2.7 shows the RDAB topology with a SRC and the typic wave forms in the transformer input/output.

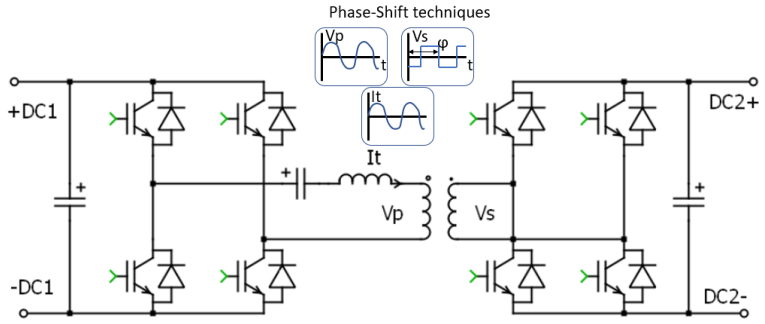

Figure 2.7 RDAB topology

In one way, the smoother waves reduce the voltage stress in the transformer and create a better environment regarding electro-magnetic disturbances emission [**BAT23**] and, in other way, the resonant circuit may be useful to increase the range in which the converter can operate in soft switching mode [**SHA20, HU19, DUY15, ALH20**]. Consequently, commutation losses are reduced which can improve the efficiency of the converter if compared with the previous topologies. However, it needs additional passive components, which represent supplementary volume, cost, and a decrease in the reliability level [**ALH20**]. For example, the additional capacitor aging may impact the resonance frequency of the SRC, which may disturb the normal operation of the control system.

2.2.3. Behavior of converters under DC short-circuit

Each converter topology has its own behavior during faults in the DC side of the converter. Even so, it is important to consider that, to avoid destruction inside a semiconductor module, when large current levels are measured, the control system usually sends opening signals to all transistors.

Regarding the first two non-isolated topologies (2-level VSC and NPC) the steps through which the converters passe during a short-circuit at the DC side are very similar **[YANA12, WAN16]**. Their behavior during faults can be categorized in three main successive stages:

1. Capacitor discharge: the output filtering capacitor will be quickly discharged into the fault passing through the DC grid.
2. Antiparallel diodes freewheeling: once the output capacitor is discharged, line inductance imposes a current which also feeds the fault. The current flows through the antiparallel diodes in the converter, which are positively polarized since DC voltage is close to zero.

3. AC grid fault feeding: the positive polarization of antiparallel diode gives free passage for the AC grid to feed the fault. It is in this stage that steady-state current levels are reached.

Figure 2.8 and Figure 2.9 illustrate some of the current paths for the three stages of a DC fault. It is possible to see that the antiparallel diodes always make part of the short-circuit current's path. Therefore, for these topologies it is important to highlight that these diodes must be able to withstand the fault currents for the determined period that allows the protections systems to work properly.

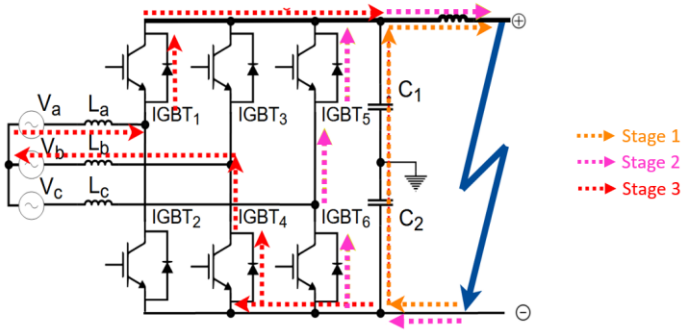

Figure 2.8 Short circuit behavior of the 2-level VSC

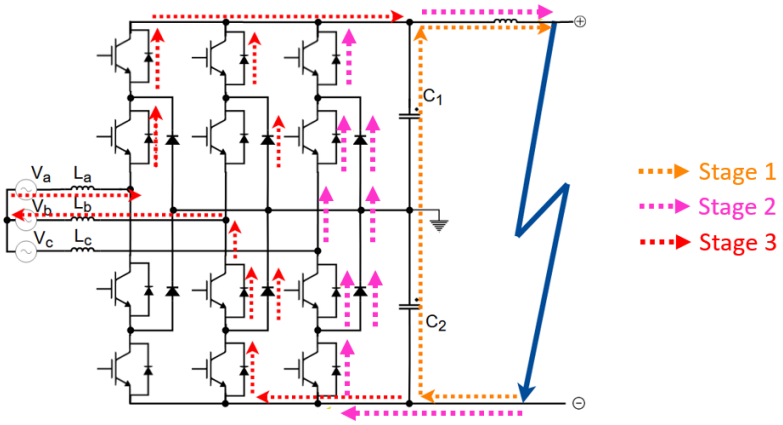

Figure 2.9 Short-circuit behavior of the NPC

In contrast with both the previous topologies, the MMC is able to actively manage DC short-circuits, depending on the internal structure of its modules. In terms of fault behavior, the hybrid and full-bridge MMC are capable of completely stopping fault currents. This happens due to its internal organization of capacitors and switches. In fact, a full-bridge module can generate negative voltage, which can block completely the polarization of antiparallel diodes, preventing the AC grid of feeding a DC fault. In addition, the negative voltage generated by the capacitors opposes the DC short-circuit current, resulting in a quick drop in current level [**XU21**].

It is possible to see from Figure 2.10 that if the total capacitor voltage from all full-bridge modules is superior to the AC peak line voltage, the antiparallel diodes will not be polarized and do not open the path for the AC grid to feed the DC fault [**ZEN15**]. It is possible to see as well that the fault current imposed by the arm and line inductors is rapidly attenuated since there is a contrary voltage being imposed by the modules' capacitors.

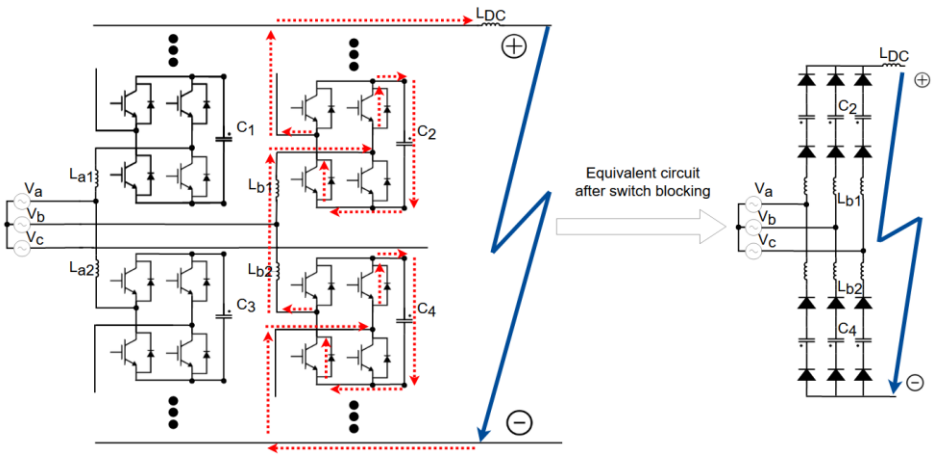

Figure 2.10 Short-circuit behavior of the full-bridge or hybrid MMC

In terms of operation during DC faults, all the presented isolated topologies are able to actively react to faults and to limit the short-circuit current in the DC output side and in the AC transformer. However, the way through which each topology is capable of doing it is slightly different. While the SAB can only act during faults through one degree of freedom, the DAB and the RDAB grant other possibilities in function of the modulation technique.

During a fault, the SAB can limit the short-circuit currents through the control system, in which it is possible to maintain the current levels at a certain reference regardless of the DC voltage variation. In reality, the control system can adapt the duty-cycle of the square waves (DCy modulation) or the angle of phase-shifting (PS modulation) with the objective to limit the steady-state current levels. It is only possible, because the antiparallel diodes of the active bridge are not polarized as in the case of the 2-level VSC or the NPC. Nonetheless, there is a transient phenomenon that is created right after the fault, due to the discharge of passive components in the short-circuit loop.

Figure 2.11 illustrates the behavior of the SAB under fault, which can be categorized in three phases:

1. Capacitor discharge: the output capacitor in the faulty DC side of the grid will be quickly discharged into the fault and the current passes through the DC grid.
2. Diodes freewheeling: when the output capacitor has no more energy, line inductance imposes a current which also feeds the fault. The current flows through the diodes of the passive bridge, which are positively polarized since DC voltage is close to zero.
3. Steady-state current limitation: the current passing through the diodes can be controlled and limited by the active bridge with the objective of reaching a certain steady-state level.

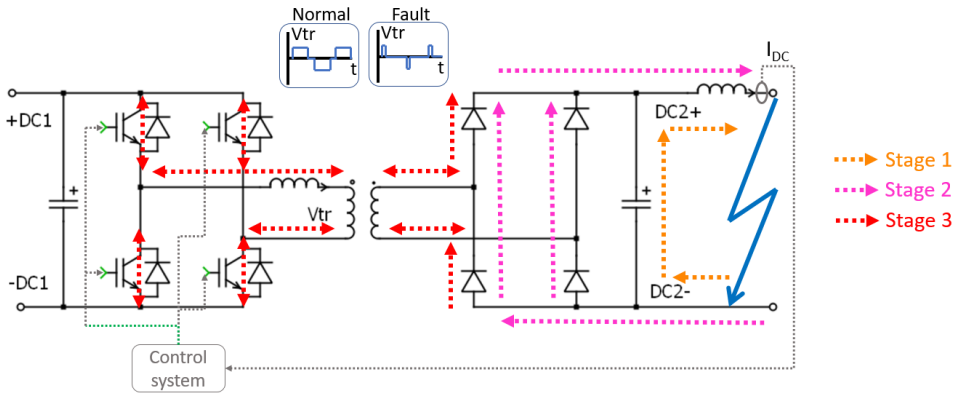

Figure 2.11 Short-circuit behavior of the SAB

The first two stages are also observed in the DAB and in the RDAB. Even if, the transient behavior and current waves are different between these two topologies, the short-circuit loops are basically the same. For these topologies, however, the freewheeling stage happens through the positive polarization of the antiparallel diodes in the switches of the bridge in the faulty DC side. The advantage of the DAB and the RDAB over the SAB is that the third stage may not be necessary to avoid the destruction of the converter. The normal operation of both topologies can naturally limit the short-circuit current level in the transformer, and consequently, in the faulty DC side. Fault currents have a lower RMS value than the rated value of current [**CHE21, RAH19, HAR15**]. The voltage across the series inductor is a function of the voltage levels in both the primary and secondary side of the transformer. Since the voltage in the faulty side of the transformer is close to zero, the voltage across the series inductor reaches lower values than during the normal operation. Consequently, the current levels are limited to under rated values as well, without any specific designed control action.

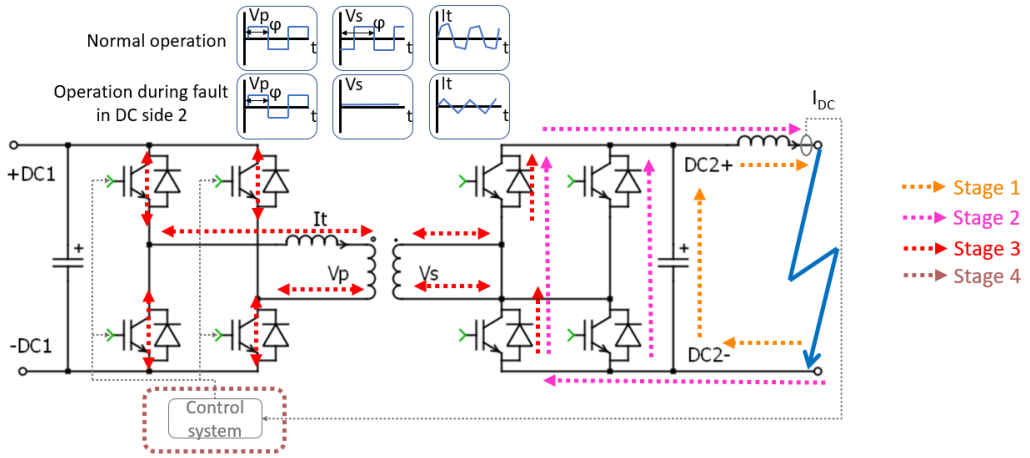

Figure 2.12 Short-circuit behavior of the DAB

This way, in the case of a short-circuit, for the DAB and the RDAB two other stages can be categorized following stage (1) and stage (2) already defined for the SAB:

3. Natural current limitation: the third stage is represented by steady-state operation with voltage and current levels being lower than rated values.
4. Output current control: a fourth stage can be deployed to use the non-faulty bridge to control the converter with the objective of following a current reference in the output DC side. This last stage gives a flexibility degree to the converter operation, and it could be used in protection schemes, for example.

2.2.4. Overview

It is possible to observe that many possibilities exist regarding power electronics converters which can play the role of an interlink converter in a hybrid distribution grid. The first group of converters with classic galvanic isolation are a mature technology in the LV domain, while topologies using medium frequency transformer are still being investigated as a potential solution, bringing advantages such as the reduction of the passive elements, in terms of volume and potentially the cost in a near future. For the designing of a LVDC distribution grid, the type of desired galvanic isolation is the first choice to be made considering power electronics.

With the objective to provide a clearer and summarized view of the potential of each topology studied here, Table 2.1 and Table 2.2 contain a global comparison of advantages, down-sides and trade-offs of these converters inside their category.

Table 2.1 Non-isolated converters

Topology	Advantages	Down-sides
2-L VSC	Simplicity, robustness, low number of semiconductors, low cost	Passive short-circuit behavior, incapacity to manage voltage imbalance for bipolar distribution grids
NPC	Low harmonic distortion, low voltage stress in switches, voltage imbalance regulation	Passive short-circuit behavior, high number of switches
MMC	Lowest harmonic distortion and voltage stress in switches, active capacity of controlling short-circuit currents (full-bridge), best control functionalities	Complex control and modulation system, highest number of switches, highest cost

Table 2.2 Isolated converters

Topology	Advantages	Down-sides
SAB	Simplicity, robustness, short-circuit current limitation through control system	Only one degree of freedom, high voltage stress in the transformer
DAB	Multiple degrees of freedom, enhanced control capacity, efficiency, high range for soft switching, natural fault current limitation	Modulation and control system complexity
RDAB	Highest range for soft switching, enhanced power quality, natural fault current limitation	Additional passive components, high cost and high volume

Based on this analysis, since galvanic isolation seems to be necessary to dissociate the LVAC and LVDC grids, as it is proposed by CurrentOS [**DCS22**] and OCDA [**DCI22**], from the perspective of this research, it is interesting to investigate the isolated topologies for LVDC applications. The main characteristics that justify this choice are the possibility of limiting short-circuit currents easily and the possibility of using a medium-frequency transformer instead of a low-frequency one.

More specifically, in terms of topology, the best suited AC/DC brick to operate in the first conversion stage of the converter looks to be the 2-LVSC. It offers a low complexity level and high reliability through a low cost compared to the other topologies. The NPC becomes interesting for bipolar grids, but when put in cascade with other converter topologies, the medium-point access is not exploited. This way, the NPC loses one of its main advantages. Regarding the MMC, the cost associated to this topology is too high and the operation in low voltage does not justify this cost. One of the main reasons for using MMCs is to have low voltage stress is power switches, which does not happen in the LV domain. Some MMC topologies are capable of limiting short-circuit currents, but when connected in cascade with an isolated DC/DC converter, which is also capable of doing so, even this feature loses its value. In respect to the output DC/AC/DC conversion steps, the DAB represents a good trade-off between simplicity, reliability, and control features. The complete topology modelling will be explored in the next chapter.

2.3. Safety and protection systems in LVDC

As already seen in the first Chapter, another important subject which is not yet completely defined in standards is protection systems in LVDC. They represent one of the most important foundations for all power systems, and their objective is to protect electricity users, appliances connected

to the grid, and the grid itself [**AKH14**]. This way, it is important to understand what the specificities of protection schemes in DC are, what protection devices exist to be used in LVDC, what recommendations are made by standards if they exist, and what is being proposed in the literature to overcome the potential challenges.

Therefore, this section will address the protection subject, from a review perspective. Technical details will be discussed on the challenges related to protection schemes for LVDC distribution systems, protection devices, fault detection strategies and existing standards in the domain.

2.3.1. Challenges associated to the protection of LVDC distribution grids

Protection systems in AC have already acquired a high maturity level through many years of operation **[CHE17, BAC15]**. On the contrary, in DC, protection schemes are a non-standardized and developing domain which needs to answer to new challenges and requirements. In fact, one of the greater challenges related to DC distribution is the design and implementation of a well-coordinated protection system. In general terms, there are two main difficulties: the application of selectivity firstly and, in a second place, the protection against electric shock.

2.3.1.1. Application of selectivity rules

Selectivity represents the capacity of a protection scheme to isolate only the portion of the grid that has been affected by a fault. As a result, a selective protection architecture can minimize the interruption of the power supply to end-users. Figure 2.13 illustrates the selectivity concept. The expected operation of the system is that the first upstream protection device should detect the fault and isolate it. For both diagrams, the fault takes place between “End-users A” group and “Protection device 2”. Therefore, it is “Protection device 2” that is supposed to isolate the fault, maintaining the normal power supply to “End-users B”. However, in the left diagram, it is "Protection device 1” that opens the current path, consequently interrupting the power supply for both “End-users A” and “B”.

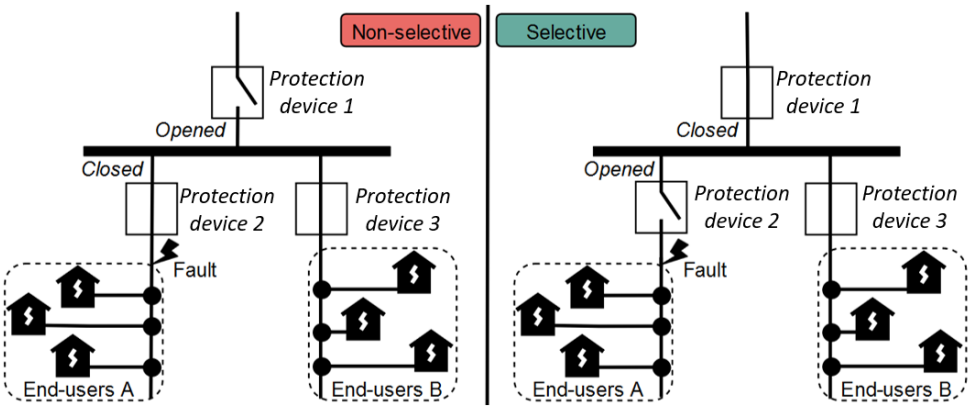

Figure 2.13 Selectivity concept

In AC, the entire power chain is selective, from the high-voltage transmission to the customers distribution board. Different types of circuit breakers and fuses are all coordinated to ensure selectivity. Their objective is to protect final consumers from electric shocks and equipment in general (cables, electric/electronic devices…) from overcurrent, overvoltage or undervoltage. In the case of a fault, if the first upstream protection device is not capable of clearing it, then, and only then, a farther upstream back-up protection must operate. In a low-voltage domain, this scenario is only possible due to the high

short-circuit power of the grid and the capacity of the grid itself to endure high-level currents for a considerable period.

However, in DC, power is supplied through power electronics converters, which have a limited short-circuit power. Consequently, the protection scheme must be adapted to operate with lower short-circuit currents, which can be problematic for fault detection. There is often a trade-off involved, a high-level short-circuit current allow protection devices to operate correctly, however it may put the converters' semiconductors in danger. On the other way, a low short-circuit current does not put equipment at risk but it may not be enough to trip classic protection devices. In most cases, in order to preserve the converter lifetime, during a fault not only the current level supplied by the converter must not exceed certain relatively small thresholds, but also the period of time the converter is able to supply this current is usually very short. This operation mode generally does not leave proper margins to selectively coordinate all protection devices. In addition, depending on the earthing system and the thermal withstand capacity of the converter, it may be necessary to detect an isolation fault in the public distribution domain (if it is conceived in DC), which is not a usual need in classic AC distributions.

A possible solution is the oversizing of the AC/DC and DC/DC converters. However, there is another trade-off involved. If a more powerful converter is able to withstand fault conditions with higher short-circuit currents, it also will perform with a considerably lower efficiency under normal conditions **[GEL15]**. It is possible to observe the need of a more solid cost-benefice analysis to determine what is more advantageous: to employ the use of converters in their ideal dimensioning and point of operation with a more complex and expensive protection scheme, or to adopt the use of oversized converters in exchange of a simpler protection scheme and a worst efficiency.

Other solutions can also be proposed, such as the use of current-limiting converter topologies or ultra-fast protection devices. In both cases, the converter is not at risk because the short-circuit current is either limited between accepted boundaries, or the time response for the protection device to operate correctly is very short. The trade-off is that the fast protection devices are, the more expansive they are as well.

2.3.1.2. Protection against electric shock

An electric shock can be caused by the result of a direct or an indirect contact. The first designation is applied when a person directly touches an active part of the distribution (typically a conductor). The second situation happens when there is an insulation fault, where the electric part of a device has its electric potential increased in relation the ground when touching an active part of the system.

The part of the protection scheme dedicated to electric shocks is deeply influenced by the earthing system. Considering electric installations for buildings, the IEC 60364 standard **[IEC05]** defines which are the earthing systems existing in DC. As it will be presented next, the same concepts available in AC also can be applied to DC.

Figure 2.14 to Figure 2.18 illustrate the 5 possible earthing configurations: IT, TT, TN-S, TN-C and TN-C-S for an LVDC distribution. While in an IT configuration there is no ground connection (or a high impedance ground connection), TT and TN systems have a direct ground connection at the level of the main supply converter. The difference between TT and TN is that, in TT the metallic cases from appliances and devices in the user side are connected to the ground locally, while in TN they are connected to the ground at a centralized connection through a conductor wire (Protective Earth conductor in TN-S and one of the normally distributed conductors in TN-C). A fifth configuration is

possible, combining TN-C in the beginning of the installation followed by a TN-S architecture, which is called TN-C-S.

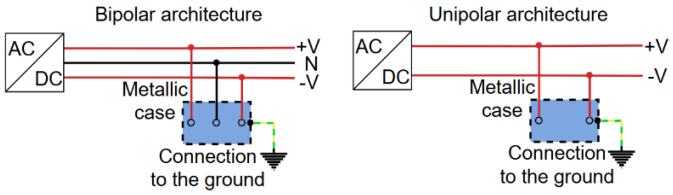

Figure 2.14 IT earthing system

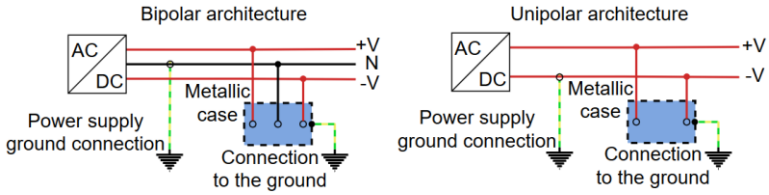

Figure 2.15 TT earthing system

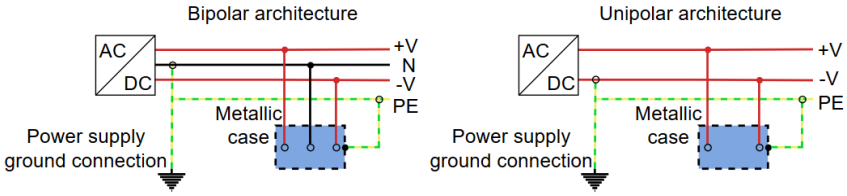

Figure 2.16 TN-S earthing system

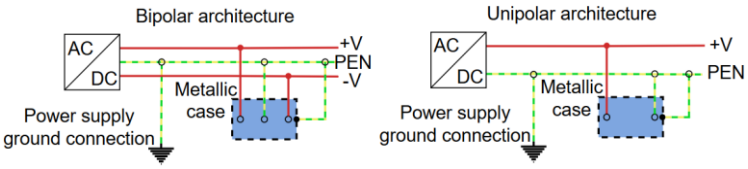

Figure 2.17 TN-C earthing system

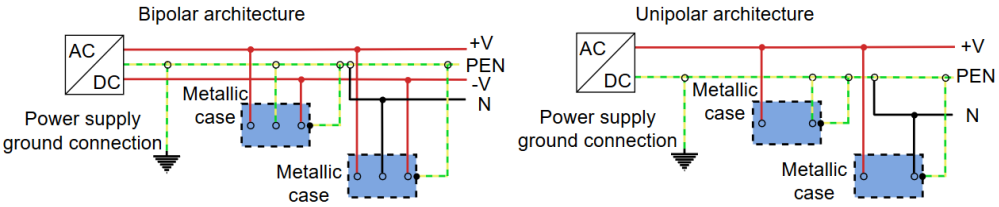

Figure 2.18 TN-C-S earthing system

Although earthing systems are defined in DC as well, the use of each one of the configurations is still not clearly defined in standards. Consequently, a deeper analysis must be carried out to define which are the possibilities to be employed in LVDC distribution systems. It involves guaranteeing the tripping of protection devices used for the detection of ground faults. The difficulty lies on calculating accurate fault currents (including transients) for protection device calibration, since the short-circuit current supplied by the converter is highly dependent of its internal architecture [**SLO22a**].

2.3.2. Protection devices

The correct operation of protection schemes is intrinsically based on the behavior and coordination of the different protection devices and protection measures which can be adopted to ensure high safety levels in the operation for a distribution grid. From the previews section it is possible to observe that interrupting faults in DC (Annex A. Arc Extinction in DC systems), reaching high selectivity levels, and protecting users from electric shock may be considerably more complex than in AC. In addition, the absence of DC-specific standards complicates even more the conception of reliable and solid protection schemes. In this scenario, it is important to review which technologies of protection devices are available for use in LVDC and which ones are capable of answering to the specific demands of DC systems.

2.3.2.1. Thermal-magnetic circuit breakers (TMCBs)

Just as in AC, Thermal-Magnetic Circuit Breakers (TMCBs) can also operate in DC systems. TMCBs are usually used in the last stages of a distribution system, being observed in the user electric panel, for example. They are usually composed by two electric contacts, a tripping system, and an extinction chamber. Two distinct modes of tripping can be emphasized, overload tripping and short-circuit tripping. An overload situation can be endured for larger periods of time than a short-circuit because the level of current is a lot closer to the rated current of the installation. Classic LVDC TMCBs overload detection is based on thermic dilation phenomenon, while short circuit detection is based on a magnetic circuit, which operates considerably quicker to open the electric circuit. This particular tripping behavior is usually represented in Inverse Time Overcurrent (ITOC) or Inverse Definite Minimum Time (IDMT) curves. An example of these curves is shown in Figure 2.19.

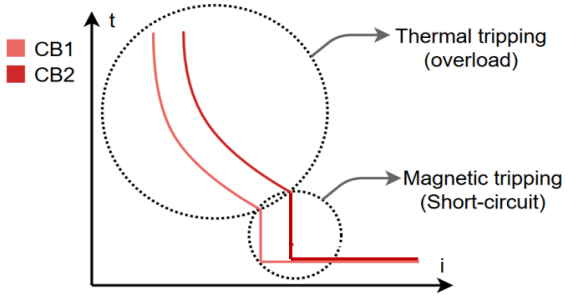

Figure 2.19 Selective characteristic of 2 Circuit breakers

These curves are especially useful to understand the current and time selectivity strategies, defined in (a) and (b):

a) Current selectivity: for this type of coordination, it is the current level of a short circuit or overload that imposes different opening delays for two protection devices in cascade, with the one presenting the smaller rate tripping current being opened firstly. In Figure 2.20 (a), it is possible to observe that selectivity is achieved between the PD1 and PD2 curves, in zone “s”, since the tripping current of PD2 (It_2) is smaller than the one of PD1 (It_1).

b) Time selectivity: in this case, a chronometric function is implemented in both protection devices in cascade, either for the same tripping current threshold or as a complement of the current selectivity. The downstream protection device will always have a shorter tripping time delay compared to the one upstream. It is also important to specify that the time selectivity is only possible if the upstream protection device can withstand the current level for the designed time delay. In Figure 2.20 (b), selectivity is also achieved in zone “s”, but in relation to the tripping

time. Since the tripping time of PD2 (Tt_2) is higher than the tripping time of PD1 (Tt_1), PD2 will always operate before PD1 for the same fault current level.

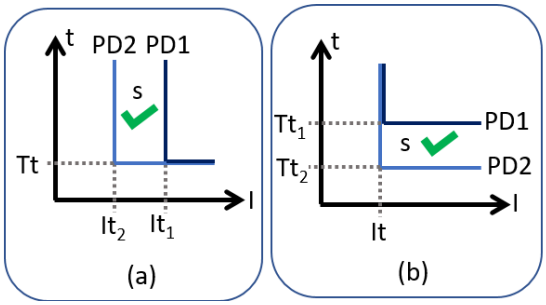

Figure 2.20 Current (a) and time (b) selectivity

Other types of selectivity strategies exist [**NER01**], such as logic selectivity, energy selectivity and zone selectivity. Nonetheless they will not be the focus of this work, since these approaches are often used for more complex systems (in MV notably), where a higher level of reliability is needed and justifies a more expensive protection scheme.

In a technical report created by ABB **[ABB10a]**, it is possible to see that the thermal operation of CBs does not change from AC to DC. This is explained by the fact that the effect responsible for this tripping is the heat generated from the current flow and, in these terms, there is no change between AC RMS and DC current levels. Nonetheless, for instantaneous short-circuit tripping, the response time is different due to the ferromagnetic phenomena involved. So, in general, for the same time response, DC circuit breakers need a higher current level.

Finally, in terms of categories, TMCBs can be characterized according to their ITOC curve. Usually, what changes is the magnetic tripping overcurrent thresholds. The most used types are B, C, D, K, and Z. B and C TMCBs are suited for residential and commercial applications, D and K are suited for heavy industrial loads (motors), and Z can be used with very sensitive equipment (power electronics). There two standards that regulate some characteristics of the curves of each type of TMCBs, the IEC 60947-2 [**IEC16**] and IEC 60898-1 [**IEC15a**]. The first one leaves to manufacturers to decide the magnetic tripping current and imposes only an envelope of ±20% around the defined tripping current level to be respected. On the other hand, the second standard defines clear envelope limits for TMCBs type B, C, and D, which can be seen in Table 2.3. These different types of curves are employed by manufacturers such as ABB and Schneider in their DC compatible circuit breakers [**SCH18b, ABB15a**].

Table 2.3 Magnetic tripping of TMCBs according to IEC 60898-2

Type	Tripping envelope
B	$3I_{rated} < I_{tripping} < 5I_{rated}$
C	$5I_{rated} < I_{tripping} < 10I_{rated}$
D	$10I_{rated} < I_{tripping} < 20I_{rated}$

2.3.2.2. Electronic tripping circuit breakers

Electronic tripping circuit breakers (ETCBs) are more expensive than the previously analyzed ones, but they offer a large range of additional functionalities. Along with the arc extinction chamber and the electric structure needed to open a circuit in a distribution system, ETCBs have an electronic tripping unit or digital relay, which can be configured to execute a variety of protection functions, such as: overload, short-circuit, undervoltage, overtemperature and others [**ABB10b**]. This electronic unit

can be external to the CB or built into it. They work through measuring sensors and a microprocessor, and they are able to reproduce multiple virtual tripping curves, which can be adapted in case of changes in the distribution system operation or architecture. They are usually utilized in situations that demand more subtle coordination in the overall protection scheme.

Among the different types of CBs that can be used with electronic tripping, it is possible to highlight the already seen MCCBs and also the Air Circuit Breakers (ACBs). ACBs are generally employed as a centralized protection device, protecting the entire facility, residence, or building. They are usually equipped with a large air-filled chamber for arc extinction, as its name suggests. An advantage of ACBs is that the rated current, voltage and short-circuit breaking capacity are usually higher than the beforehand presented CBs. Although ETCBs are accurate, configurable, and their operation is independent of the local temperature, the electronic circuits present in the tripping unit are less robust than the thermal-magnetic tripping seen previously, resulting considerably more sensible to electromagnetic disturbances for example.

2.3.2.3. Solid-state circuit breakers

Solid-state circuit breakers (SSCBs) are the new line of circuit breakers bringing novel benefits for distribution systems based in energy sources which need a fast reaction to faults. These CBs are composed of semiconductors, therefore they do not need to physically disconnect the circuit to stop the current flow. Considering this fact, no electric arc is generated during fault clearance. In addition, the response time of an SSCB to a fault can be more than a hundred times faster (order of microseconds) if compared to the classic thermal-magnetic circuit breaker (order of milliseconds) [**TRA20**]. The time response is a function of the delay associated to current measurement, the delay of calculations inside the computational engine controlling the SSCB (including Analog-to-Digital Conversion), the delay of transmission of the opening signal to the switches, and the delay associated to the transitory behavior of the SCCB during the opening of the circuit.

Even if there is no arc generated during a fault clearance with SSCBs, when power electronics switches are opening the circuit, the fast variation in line current can create a large overvoltage transitory which must be mitigated to avoid any damage. Usually, the technique applied to solve this problem is to design a hybrid dissipative-storage snubber circuit. Different topologies of snubber circuits exist for this type of application [**RAH22**], such as Resistor-Capacitor (RC) snubber, Diode-Resistor-Capacitor (DRC) snubber, or the DRC plus a Metal-Oxide Varistor (DRC-MOV) snubber. MOVs operate like a variable resistor, whose resistivity value changes in function of the voltage to which they are submitted. Consequently, they are a valuable component for SSCBs to limit the transitory overvoltage [**WU20, KHE22**]. For the snubbers presented here, different design methods exist in the literature [**LIU17, SUN21**]. Still regarding the internal topology, since they are made of power electronics switches, SSCBs can be unidirectional [**JAL22**] or bidirectional [**SOL21**], in accordance with the part of the distribution system they are protecting. As expected, the bidirectional structure needs additional active switches and control system features in order to operate correctly [**YAN21**]. Figure 2.21 shows a bidirectional SSCB with DRC snubbers, which is present in multiple studies [**LIU17, RAH22, PUR21, JAL22**].

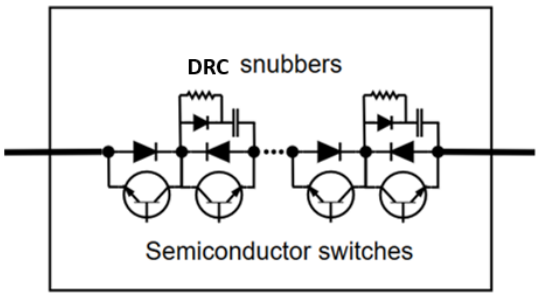

Figure 2.21 Solid-state circuit breaker topology

There are four main potential downsides which can be identified regarding SSCBs. The first one is associated with their cost, which is more elevated than the classic circuit breaker architectures. The second one concerns the generation of non-negligeable losses during its normal on-state operation, which can be considerably higher than classic AC CBs losses [**TRA20**]. The third weakness is related to the fact that SSCBs are composed by a set of electronic circuits, which can be significantly influenced by electromagnetic disturbances, making them less robust and potentially less reliable than previously presented CBs. Finally, a possible fourth disadvantage is that until now it is difficult to evaluate the lifetime of an SSCB since they are a new technology in the LVDC domain.

Regardless of these drawbacks, the potential of SSCBs in terms of quick fault clearance and safety enhancement with no electric arc are making them suited for future hybrid AC/DC distribution systems [**SUN21, CHA22, KHE21**]. SSCBs are the core device used in the protection scheme proposed by DC Systems and Current OS foundation and is also one possibility for the DC breakers in the protection methodology proposed by DC-Industrie2 and ODCA. In addition, new semiconductor structures known as Wide Band-Gap (Silicon Carbide - SiC and Gallium Nitride -GaN) can be used in new topologies of SSCBs to solve some of the problems presented above **[BEH19]**, notably the losses in normal operation state [**SHE15**]. In this scenario, there are manufacturers such as ABB [**ABB22**], Schneider, and Blixt, which are developing different types of SSCBs for the LVDC domain, which are already certified by the IEC.

2.3.2.4. Hybrid circuit breakers

Another recent structure that combines the architectures of solid-state and mechanical circuit breakers to benefit from their respective advantages is the Hybrid Circuit Breaker (HCB). While maintaining the optimal conduction performance of a mechanical circuit breaker, the HCB can reach a response-time for disconnection of less than 5 milliseconds with the maximum rated current. This type of CB is also proposed as a possible solution for the DC breakers presented in the protection scheme of DC-Industrie2.

The classic architecture of an HCB **[CHE18, CAL12]** is showed in Figure 2.22. Through it, it is possible to see that the classic operation of a hybrid circuit breaker happens in three stages:

1) In steady state, the current passes by the mechanical contacts.
2) When a fault is detected, the mechanical contactor begins to open, creating an arc. The arc voltage induces the semiconductors into turn-on mode, and the current passes by the switches, since they represent a path with less impedance.
3) When the transient recovery voltage is reached in the contactor terminals, a turn-off signal is sent to the switches. Due to the line inductance, the voltage will rise, and the current will then pass through the MOV, where the energy will be dissipated, and the current will reach zero.

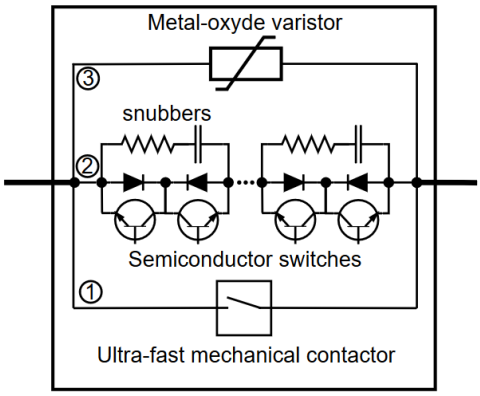

Figure 2.22 Hybrid circuit breaker topology

Also, more recent research is using adapted topologies to create soft-switching (ZVS and ZCS) in HCBs with the objective to reduce even more voltage and current constraints to which power electronic switches are submitted during the fault clearance [**LAZ19, HAG21**].

Even if there are possible advantages associated to the use of HCBs in relation to both SSCBs and classic MECBs, this type of technology is less mature than SSCBs and less reliable than MECBs. For these reasons, until the moment, there are few options available in the market which can be used in LVDC distribution systems.

2.3.2.5. Ultra-fast fuses

A fuse is a protection device connected in series with the protected circuit. It is composed of two electric terminals, interconnected by a metal strip through a heat absorbing material, as shown in Figure 2.23. Its operation is based on an inverse time-current characteristic, so that the melt down time of the metallic strip decreases when the current increases.

It is possible to observe in manufacturer's technical guides that there are AC fuses that can also be used in DC **[SIE12]**. However, taking into consideration the arc extinction problematic, for the same fuse technology, the rated voltage level is always lower in DC. There are also other architectures of DC fuses that are designed with a larger gap between their electrodes and a faster melt down time, in order to reduce the possibility of an electric arc **[CHE17]**.

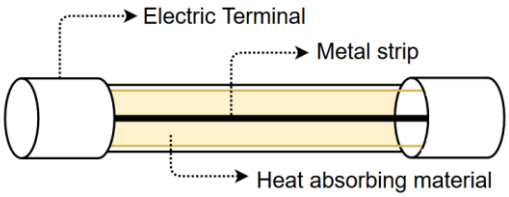

Figure 2.23 Classic fuse structure

Ultra-fast (UF) fuses are a specific category of fuses which seems to be well suited for LVDC. They are the class with the fastest time response available in the market and can be employed to protect power electronics switches [**BUS10**]. The capacity of a fuse to stop a fault can be measured by two indicators. The first one is the value of Melting Point (i^2t), measured in Ampere-Squared-Seconds, which is the equivalent thermal energy needed for the fuse to melt. It is usually used to coordinate multiple fuses in cascade. The second one is the ITOC curves of the fuses, which is useful to coordinate a fuse with a CB or other fuses in cascade. Figure 2.24 shows the ITOC curves of two fuses (F_1 and F_2) in cascade with a selective coordination. The red zone is characterized by a constant i^2t value, which is why it is almost a straight line in a logarithmic scale.

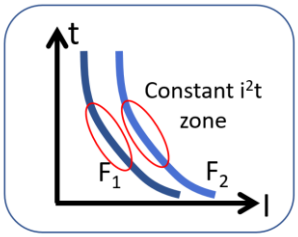

Figure 2.24 ITOC curves of ultra-fast fuses

2.3.2.6. Residual current devices

Residual Current Devices (RCDs) are constantly monitoring the presence of a leakage current, which is the indicator of a ground fault. In a distribution system RCDs, are specifically used to avoid electric shock, and they are crucial for installations using TT earthing systems. In TT grounding configuration, the resistance of earth electrodes may be elevated, which making fault current levels too small to allow classic TMCBs to clear a fault in the time established by [**IEC05**]. These periods can be observed in Table 2.4. Consequently, a time-independent protection device is needed in these cases. AC RCDs are composed by a magnetic coil, through which the active and neutral conductors of a distribution system pass. In a normal operation of the system, when there is no leakage current, the sum of the currents passing through the coil are very close to zero. As a result, no electromagnetic field is generated and no current passes in the coil. If a ground fault happens, then the sum of currents is no longer close to zero, and a current is generated in the RCD's coil. Finally, if the value of the leakage current surpasses a tripping threshold creating an electromagnetic field, the RCD opens the circuit.

Table 2.4 Disconnection time requirements [IEC05]

	50V < U ≤ 120V	120V < U ≤ 230V	230V < U ≤ 400V	U > 400V
TN or IT	5s	5s	0.4s	0.1s
TT	5s	0.4s	0.2s	0.1s

This simple operation based on a current transformer works in AC systems, since the alternating current produced by an imbalance between neutral and active conductors generates a variable electromagnetic field in the primary side coil. The secondary side of the transformer then sees a voltage between its terminals, causing the device to trip. On the other hand, in DC, since there is no periodic changing in electromagnetic fields, RCDs cannot operate. A DC RCD which is independent of external energy supply, as robust and low cost as the AC one, does not exist yet. Nonetheless, there are SSCBs with shunt current sensors based on Hall Effect to detect ground faults and operate as RCDs do. These sensors are able to measure DC current from the two (monopolar) or three (bipolar) conductors of a distribution grid and when associated with an electronic comparator, they are able to detect leakage currents. One example of SSCBs with integrated leakage current detection is the Current Router from DC Systems [**DCS22**].

2.3.2.7. Insulation monitoring device

Particularly useful when used for protecting IT earthing systems, Insulation Monitoring Devices (IMDs) are constantly measuring the impedance of conductors to the ground and are always equipped with sound or visual warnings to inform about significant alterations. It is an important device in IT distribution grids to avoid two successive ground faults which result in a short circuit. The use of this devices for DC IT distribution systems up to 1500V is defined by the IEC 61557-8 international standard [**IEC14**]. It specifies rules for measurement of current, voltage and impedance calculation, including the specifications of all the performance and safety requirements as well.

2.3.3. Different protection strategies against overcurrent

Once the presentation of the major protection devices which can be used in LVDC is done, it may also be interesting to understand what combinations are possible to protect the distribution system against overcurrent. Next sections summarize the most common coordination strategies among multiple studies conducted around the world. Many possibilities exist in terms of fault detection [**AHM21**], such as overcurrent, differential and current derivative methods. This work focuses on simple overcurrent-based fault detection methods since they are the simplest and less expensive ones.

2.3.3.1. Fuse-based protection scheme

Considering the challenge of the coordination between the circuit breakers, time response and the converters short-circuit behavior, added to the fact that solid-state circuit breakers are not mature in the market yet, there are some studies that draw on fuses to ensure the protection of the distribution system **[BAY20, RAV20, REY21].** In fact, fuses are already standardized, and they represent a cheap solution a simple overcurrent fault detection. However, their major inconvenient is the need of maintenance to replace them, whenever there is a fault. In addition, from preview studies, it is possible to see that the system time constant τ plays an important role on the fuse operation **[SAL09]**, and to allow a fuse dependent protection system to operate correctly, it is necessary for the system to have a high equivalent capacitance **[RAV20]**. The presented reasons make fuses to be feasible as a backup protection in most cases, but they can also be used as the main protection in specific easy access parts of the distribution, especially in the small ones **[CHE17]**.

2.3.3.2. CBs-based protection scheme

Circuit breakers are still the most reliable way of ensuring the disconnection of a faulty part in a distribution grid. In the literature, there are encouraging results concerning the use of new technologies around CBs and novel coordination strategies that can fit the requirements imposed by the converters short-circuit endurance characteristics.

Concerning TMCBs, current selectivity approach is considered, just as it is done in AC. However, it is important to highlight that its use may be problematic to protect sources which are not capable of limiting short-circuit currents. Different ITOC curves show a relatively slow reaction time to clear faults (limited to 10ms) [**SCH18b**]. In addition, even the curves with the smaller tripping thresholds (B and Z) may be too much for the converter associated to these types of sources. Consequently, it may hinder the sizing of the power electronics associated to power supplies.

If ETCBs are considered, since they are equipped with a computational engine, many possibilities exist. Classic overcurrent detection can be applied if the distribution grid allows it with current or time selectivity. However, knowing that for small distribution systems, time and current margins can be very small, communication protocols can be deployed between the CBs to improve selectivity issues **[MON14].**

Finally, ultra-fast hybrid **[CHE18, YAS18]** or solid-state CBs [**EMH14, EMH17, LIU17, PAR13]** bring many possibilities, since their fast time response to clear a fault allows proper margins, which can be used to coordinate the entire chain of protection devices without the need of overcomplicated fault detection strategies. One example is that very small delays can be considered for cascade SSCBs, easily implementing time selectivity [**KHE21**]. Since the fault clearance time is short, margins are not difficult to design, and overcurrent detection is usually enough to achieve a selective scheme.

2.3.3.3. Hybrid protection scheme

In this scenario, both circuit breakers and fuses are combined to ensure the safety in a distribution system. In this approach, fuses are either a back-up protection, or placed in easily accessible maintenance places. There is also evidence provided in the literature that it is possible to well-coordinate fuses with hybrid CBs **[SAL09]** or even with classic overcurrent ones **[BAR07, SOC16]** to ensure safety throughout the distribution network. It seems to be a promising strategy since there are also additional methods to coordinate fuses with thermal withstand of power electronic converters [**BUS10**]. Consequently, the most interesting possibility would be to connect fuses in cascade with the converter as a first line of protection, with CBs downstream. ITOC curves from both devices can be used to coordinate them.

2.3.3.4. Breaker-less protection scheme

This approach is based on the capacity of power electronic converters to limit or to completely cancel the fault currents and do not require the use of CBs **[CAI13]**. After detecting a fault, the converter current controller sets the current to a small or null value. The low-level currents allow the use of electric contactors to disconnect the circuit. Finally, the converter is set to operate normally again.

2.3.4. Protection measures against electric shock

To avoid electric shock by direct contacts, **[IEC05]** requires all active parts of the system to be well insulated, through its basic insulation in addition to the insulation provided by shells and ducts. RCDs are suggested only as a non-obligatory additional protection measure.

On the other hand, the protection of people against indirect contacts depends deeply on the earthing systems. In TN ground connection, an insulation fault behaves just like a short-circuit. Therefore, the protection devices used for overcurrent are suitable for this kind of configuration. However, taking into account that the conductor connected to the earth is distributed, the global impedance of the faulty circuit must be considered, because high impedance values can complicate the operation of the protection devices. In TT grounding, an RCD is imperative because it is not time dependent. A clear statement that TT systems shall not be used in DC is put in **[IEC05]**. In IT, either there is no connection to the earth, or the connection is made through a high impedance. For both scenarios, an insulation fault would result in a low-level current, since the only current path would be the cable-to-earth capacities or a high value impedance. However, to ensure safety, the IEC 60364 **[IEC05] s**tandard presents some requirements:

1. In DC, the maximum electric potential to earth for metallic parts of devices under fault is limited to 120V.
2. An Insulation monitoring device (IMD) should be employed to detect the first insulation fault.
3. An automatic disconnection device must be set in the case of a second fault. The global faulty circuit impedance must be taken into consideration, in order to ensure its correct operation.

Other additional protective measures are also possible, such as the use of double or reinforced insulation with class II materials (devices and cables) or the use of load-associated isolating transformers, which provide galvanic isolation interrupting the ground fault path (Figure 2.25).

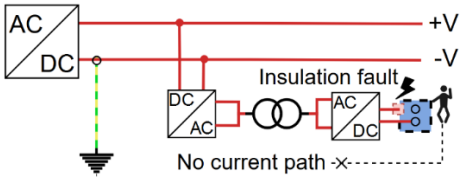

Figure 2.25 Galvanic isolation principle

2.3.5. Overview

It is possible to see that the protection scheme design in LVDC is a real challenge. The presence of power electronics converters offering small short-circuit capacity in many places in the grid render the choice of adapted protection devices more complex. Another problem is that each converter has its own internal topology, and short-circuit currents are intrinsically dependent on it. Consequently, the development of universal rules and standards in the domain is more challenging. Either existing standards are imprecise, or they cover very specific use-cases. However, it is important to highlight that many possibilities exist, which were presented in section 2.3. Available technologies of DC protection devices and power electronics converters may take protection schemes in LVDC to another horizon. Table 2.5 summarizes the protection devices analyzed in section 2.3, their main advantages and drawbacks for LVDC distribution systems.

The objective of future studies must be to find optimal trade-offs between power electronics sizing, choice of protection devices and fault detection methods. One of the main objectives of passing from AC to DC systems is energy efficiency and economic savings, although if the costs of the protection system are too high, the use of DC for distribution systems becomes economically unfeasible.

Table 2.5 Overview of protection devices

	Use	Advantages	Drawbacks
TMCB	Overcurrent	Simple operation, low cost, standardized	High reaction time
ETCB	Overcurrent and electric shock	Flexibility of configuration	High reaction time
SSCB	Overcurrent and electric shock	Lowest reaction time	Very high cost, not yet standardized
HCB	Overcurrent and electric shock	Moderate steady-state losses, moderate reaction time	Low level of technical maturity
UFF	Overcurrent	Simple operation, low cost, standardized	Maintenance, dependent of time constant
RCD	Electric shock	Time-independent	Does not yet exist in DC
IMD	Electric shock	Visual warnings of ground fault	No automatic disconnection

2.4. Power quality in LVDC

Another crucial aspect to be analyzed in LVDC distributions is the Power Quality (PQ) domain. It represents certain boundaries in terms of voltage characteristics that must be respected to maintain the entire system operating correctly. The analysis presented in section 2.4 will cover some definitions provided by recent advances in standardization and several studies available in the literature.

In the first place it is essential to distinguish the difference between the steady-state and the transient phenomena. Harmonic disturbances, voltage imbalance and low-frequency voltage variations (flicker) are steady-state power quality indices for power systems, and they are normally measured every 10 minutes (Europe) or 15 minutes (USA). Transient power quality indices such as surges are often used for electromagnetic compatibility (EMC) coordination in equipment level.

There are systems that can produce a quasi-ideal DC voltage (PV, batteries, fuel cells), where the voltage can be assumed constant. However, in this study, AC/DC and DC/DC VSC converters are considered, which generate high/medium frequency current/voltage disturbances **[BAR18]**. In addition, the introduction of traditional rectifiers (thyristors or diode) may create voltage harmonics of fundamental frequency on the DC bus. With the objective to avoid dangerous variations in voltage levels, it is necessary to establish parameters of voltage variations, thresholds, and maximum duration of fluctuations. It represents a relevant step to support the development of DC distributions. The desirable characteristics of PQ are described in **[IEC20]** and can be divided in two main aspects:

a) Voltage levels remain between an acceptable limit (Transient phenomena).
b) Ripple and high frequency disturbances remain below defined limits (Steady-state phenomena).

2.4.1. Transient phenomena

Transient phenomena are disturbances that affect the voltage level, making it rise or decrease in relatively short periods of time. For the correct operation of a DC distribution, it is crucial that voltage levels all around the power chain remain between certain boundaries **[BAR18]**. Figure 2.26 illustrates the most important transient phenomena, which were initially defined in AC systems but can be identified as well in DC.

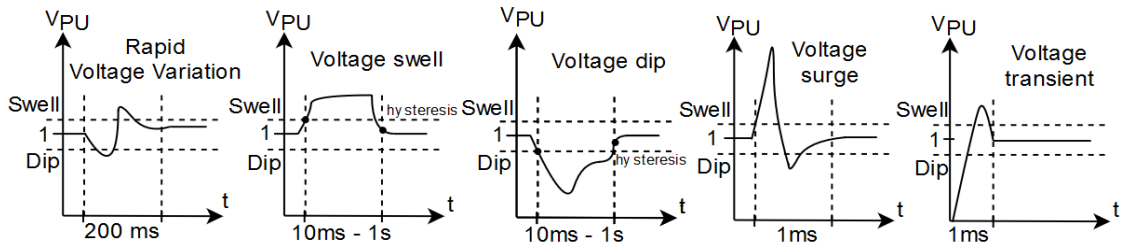

Figure 2.26 Generic examples of voltage transient disturbances [IEC20]

Rapid voltage variations are defined as a rapid transition between two steady-state voltage levels that are inside the normal operation band. It generally represents a 3-5% voltage variation during around 200 milliseconds **[IEC20].** It generally happens during a change in equipment operation (DC motor turn-on, irradiation rise in PV, load switch). Some examples and calculation methods are provided in **[BAR18].**

In AC, a voltage swell is defined as a rise in the voltage level above 10% of its nominal value **[IEC15b].** In DC, a similar concept can be used, however a specific threshold is not suggested in the literature. In **[IEC20]**, voltage swells are described as unpredictable and random, and in **[BAR18]**, they are shown to be associated with large load variations or to the opening of mechanical contractors.

In an equivalent way, a voltage dip is defined in AC as the sudden decrease of voltage levels beyond 10% of its nominal value. This phenomenon can take place because of wrong concurrent voltage regulations, load changes, but most of all during faults **[MAG06]**. To maintain the good operation of the power system, the equipment ride-through must be considered, as well as the capacity of the main

converter to bring the voltage back to acceptable levels. In a DC distribution, the characteristic of being interfaced by active elements (converters) makes the system less vulnerable to voltage dips, avoiding equipment malfunction **[IEC20]**.

However, one consideration must be made regarding the connection of all devices composed by power electronics and capacitive output filters to an LVDC grid. If these devices do not include a mechanism of pre-charging, the result is an elevated current draw, which usually causes a voltage dip. To avoid this phenomenon, it is important to pre-charge the capacitive filters with active or passive components. Different solutions are possible, and some manufacturers are already addressing the subject [**DCS22**]. Furthermore, this matter is covered by the standard IEC 61000-4-29 [**IEC00**], which specifies immunity tests for DC supplied equipment against voltage dips and interruptions. Nevertheless, these rules are rarely taken into consideration to evaluate DC grid equipment [**MAR21**].

Finally, voltage surge is the term employed to describe a remarkable increase in the voltage level, during relatively short periods of time. Usually, it happens due to three main reasons: lightning, capacitor bank connection or not proper circuit switch-off **[IEC20]**. When a lightning strikes a power system, a huge overvoltage travels around the lines, while during a circuit switch-off, the line inductance also creates a potentially high overvoltage. This phenomenon is very hazardous because the voltage levels can surpass the insulation limits, putting all the equipment in danger. Since converters are normally interfaced with capacitors, the effects of voltage surges in semiconductors are generally mitigated.

2.4.2. Steady-state phenomena

These phenomena are permanent disturbances that can be measured periodically in power systems. They are the consequence of the operation and distribution of different equipment in the DC grid. Consequently, they are not generated by external factors and are naturally present in the operation of the distribution system.

The first steady-state phenomenon to be highlighted is voltage unbalance. It affects in particular bipolar architectures, where unbalanced load distribution between the two poles and the neutral result in unequal voltage levels in each pole. In this case, there are two solutions: the most common is to use two converters, in order to decouple the system **[IEC20]**, or to use a single converter with either a voltage balancer **[KIM19]** or an internal strategy of current reinjection for achieving a proper voltage balance **[CAI16, KUN17, LI18]**.

A second important phenomenon to be analyzed is ripple and medium/high frequency disturbance. In a realistic, non-ideal scenario, the voltage in a DC distribution has some low, medium, and high frequency components. In practice, these components are manifested through periodic voltage variations around the steady-state value, and, in fact, which is a possible definition of ripple **[MAG06]**. A more technical way of defining this disturbance is proposed in IEC 61000-4-17 [**IEC99**], and it states that ripple represents the quantity obtained from a measured current or voltage by removing the direct component of it **[BAR18]**. A graphic representation is available at Figure 2.27.

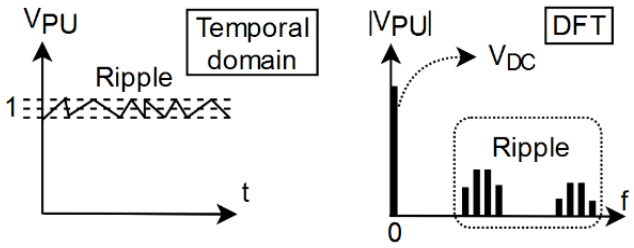

Figure 2.27 Voltage ripple in temporal (left) and frequency (right) domain

The main cause of this phenomenon is the commutation of semiconductors in power electronic converters. The switching generates non-DC components in the current, which causes a ripple voltage. The resulting ripple depends on the converter topology, commutation frequency, modulation, and control system.

2.4.3. Power quality assessment methods in LVDC

From previous sections, it is possible to see that currently available standards do not present a clear view regarding PQ assessment methods for the LVDC domain. Some of the techniques usually applied to address the subject which already exist in AC may be considered for use in DC as well. However, since definitions such as natural voltage RMS, mean voltage, harmonics, and fundamental frequency may vary its signification or do not exist in DC, for most of AC PQ indicators, changes must be proposed. A solid understanding on how to quantify PQ in DC is crucial for a correct global operation throughout the distribution systems and it is a key for the spread of DC grids around the world.

2.4.3.1. Transient phenomena

Nowadays, there are technical studies that are reviewing the definition of transient phenomena in AC and proposing adapted methods and rules for the DC domain. In [**EMP21**], regarding the obtention of supply voltage magnitude, voltage dip and voltage swell, the proposition is to modify the calculation of the voltage RMS value in terms of time window. In AC, in can be done either from a full cycle (20ms for 50Hz) or for a half-cycle (10ms for 50Hz). Those values may be replaced either by mean DC voltage or by DC voltage RMS value calculated according to a not yet specified time window.

Going even further, the IEC [**IEC20**] proposes time thresholds, which are able to characterize different transient phenomena according to its duration. The main characteristics of different voltage level disturbances can be observed in Figure 2.28. These definitions represent a great step towards large rules for PQ assessment, since the behavior of DC systems may be considerably different from AC equivalents in terms of time constants and transient phenomena propagation. The next stage would be to determine proper thresholds in terms of voltage associated to each of the described phenomena. This is a real challenge since, once again, DC systems behave naturally different form AC. The presence of power electronics converters all around a DC distribution system may complicate the definition of appropriate thresholds and transient ride-through characteristics. This is because their operation is highly dependent on its internal topology and control system, which is variable and hard to reproduce.

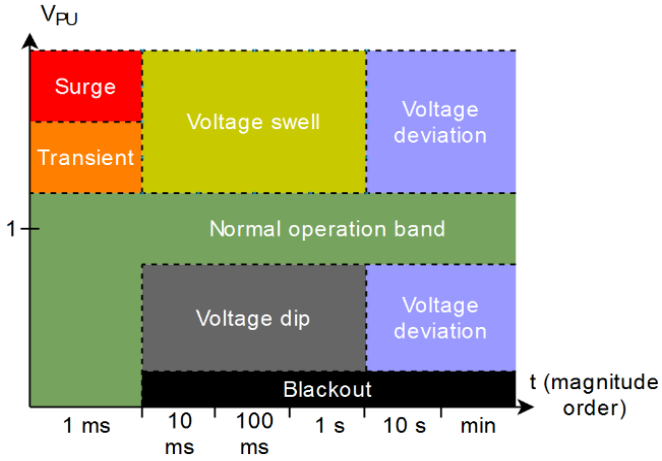

Figure 2.28 Different types of voltage level disturbances

2.4.3.2. Steady-state phenomena

The same situation is noticed for steady-state phenomena as well, but this time more significant changes must be made. The first thing to consider is that in DC there is no fundamental frequency for FFT calculation. This way, traditionally used PQ indicators like THD, harmonics and inter-harmonics magnitude lose their meaning. Starting with basic definitions, since there is no fundamental frequency, disturbances at specific frequencies may be called spectral components [**EMP21**]. Other than that, all the spectral analysis must be thought over. Although, it is important to consider that, the global PQ analysis methodology is similar to the one conducted in AC since spectral disturbance sources and sensitive equipment are almost the same [**YAN22**].

The best way to evaluate disturbances caused by spectral components is to define voltage/current ripple indicators. In **[MAR07]**, some methods of ripple evaluation are proposed for LVDC distributions and **[BAR18]** also shows several approaches to rate ripple voltage: the peak-ripple factor (IEV 161-02-26), the RMS-ripple factor (IEV161-02-27) and the Discrete Fourier Transform (DFT) based Ripple Distortion Factor (RDF), defined in equation (2.1). The IEC 61000-4-17 standard [**IEC99**] defines the notion of peak-peak ripple, but the concept is only applicable to line-frequency operating rectifiers, with diodes or thyristors. Switching-mode VSC converters are not included in its definition.

$$RDF = \sqrt{\sum_0^k \left(\frac{V_k}{V_{mean}}\right)^2} \tag{2.1}$$

In [**YAN22**] it is possible to see five different PQ indicators related to spectral components and ripple: peak-peak ripple, distortion level, total DC RMS ripple, ripple spectrum, and spectral energy. The authors precise methods of calculation and interpretation for each one of them. All PQ indicators presented here were obtained for voltage levels, however the same equations and the same reasoning can also be applied for current levels. A definition of these indicators is given next:

a) Peak-peak ripple: it is the ratio between the amplitude associated to the DC voltage and the mean value. Since it considers only the maximum and the minimum values, it is useful to evaluate voltage variation due to spectral components.

$$Ripple_{P-P} = abs\left(\frac{V_{max}-V_{min}}{V_{mean}}\right) \cdot 100\% \tag{2.2}$$

b) DC distortion level: it represents the total RMS value of all spectral components of a measured voltage. This calculation can be made either in time domain or in frequency domain. This fact is due to “Parseval’s Theorem”, which states that the Fourier Transform maintains the total

energy of a signal. However, it seems to be easier to obtain it in the frequency domain, since there is no need to calculate the DC component, as shown in equation 2.3 [**MAR21**]. It is important to highlight that "*k*" is not related to any fundamental frequency, but it is rather considered as the maximum spectral component in a FFT analysis in relation to the time window which was chosen for measurement.

$$DC_{distortion\_frequency} = V_{AC-rms} = \sqrt{\sum_0^k V_k^2} \quad (2.3)$$

c) Total DC RMS ripple: also called ripple factor, it is also expressed as a percentage quantity. It represents the ratio between the DC distortion level and the DC mean voltage level. In the same way, it can also be calculated in time or frequency domain (equation 2.4). Since it takes the pure DC component of the DC voltage, it is useful to quantify the distortion caused by spectral components.

$$Ripple_{rms} = \frac{V_{AC-rms}}{V_{DC}} \cdot 100\% \quad (2.4)$$

d) Ripple spectrum: it characterizes the representation of voltage/current non-null frequency spectral components. The frequency of the multiple spectral components depends, once again, on the time window employed to calculate the FFT. All components must be defined it terms of amplitude and phase.
e) Spectral energy: this indicator takes into consideration the calculation of DC RMS ripple for different frequency bands. Since the applied measurement and calculation methods may change, authors define that measurements conducted in the 0-9kHz frequency band must follow the IEC 61000-4-7 and the IEC 61000-4-30 methods and that higher frequency bands must follow the CISPR 16-2-1 and CISPR 16-3 methods.

Other than the presented equations, it is equally important to define time windows for each type of calculation. This subject is also covered by [**YAN22**]. Three main calculation windows are defined, as follows:

a) Instantaneous RMS measurement (Ti): it represents the time duration of measurement for the calculation of RMS values. The suggested value is 10ms. It can be used for ripple calculations, but also for transient phenomena identification such as voltage dips.
b) Spectral window (Tw): it represents the time window which is taken into consideration for FFT calculation. Both 200ms and 1s are suggested as possible values, depending on the precision needed by the situation.
c) Recording period (Tm): it represents the period of time between measurements. Multiple AC-based possibilities are suggested, such as 1 min, 5min, 10min or 15 min.

In terms of RMS measurement and recording period, the time windows may be like the ones adopted for AC systems, since the calculations are similar as well. On the other hand, for the spectral time window, in DC it is important to reach an enhanced precision in terms of frequency analysis and consequently to use a larger time window than in AC, since spectral disturbances may cover a large set of frequency values, which are not multiples of a fundamental frequency.

Most of the concepts explored above are also used by other authors in the literature [**MAR19, MAR21, BAR18, CIP22**]. Besides ripple evaluation, there are other recent research works considering supply voltage level and spectral analysis to make some interesting propositions on the assessment of PQ indicators **[CIO17, KAI19, MAR19]**. All these possibilities presented by the scientific community represent a significant step towards the definition of future standards in the LVDC PQ domain.

A last essential consideration to be made is that the behavior of power electronics converters, which are present at every equipment or device in a DC grid, is very difficult to estimate when they face disturbances in the grid. That is because this behavior depends on the internal topology, electronic components, output filters and control system of the converters. One solution to this problem could be the identification of a frequency dependent model of converters from the DC grid point of view. Since the converter behavior also depends on its operation point, this impedance model may be defined for multiple power operation ranges [**YAN22**]. With different models of frequency dependent impedances, it would be possible to analyze the propagation of disturbances, resonance effect and other phenomena, with the help of a frequency domain software.

2.4.4. Possible solutions to maintain high power quality levels

The techniques which can be used to ensure a certain level of PQ to LVDC distribution systems are actually very similar to the ones already used in AC. Regarding transient phenomena, since they are unpredictable most of the times, it is necessary to design a robust distribution system, with equipment capable of withstanding certain levels of disturbance. For example, the correct operation of the protection scheme is crucial. Fault clearance periods, restart and disconnections must respect certain rules to avoid dangerous voltage dips, voltage surges and even blackouts. Another crucial aspect to avoid risky voltage variations is to offer a high level of stability, which is ensured by a well-designed grid management system, in terms of guaranteeing the balance between generation and consumption.

In respect to steady-state phenomena, it is more complicated to ensure a correct behavior of the distribution system. For now, it is possible to establish that standards are far from defining EMC levels. From the point of view of the DC grid, there is no definition of PQ thresholds to be respected and, from equipment side, neither immunity nor emission levels are regulated. In addition to that, measurement methods must still be standardized as well. Nonetheless, it is possible to highlight techniques which will certainly be used in the future to mitigate steady-state phenomena, decreasing the magnitude of spectrum components and ripple for example.

To minimize the effects of ripple voltage/current, classic passive filters can be used (C, LC, RC, RLC). A first vigilance point is that the frequency dependent behavior of this components is very important to guarantee the correct operation of this type of solution, especially for distribution grids where high frequency spectrum components are present. A second aspect which needs to be monitored is that the addition of passive filters impacts the global impedance of the grid from the equipment point of view, which may cause resonance effects. Other than that, the internal control of current-voltage loops associated with the modulation system can be designed to minimize the ripple voltages **[PHA19, SOM16, TCA18, XU18].** In the case of more constraining systems in terms of harmonic disturbance, even an active filter (converter based) can be used to almost extinguish voltage ripple completely **[LAI17]**. The last presented solutions may bring a high-performance level, but the trade-off involves the cost associated to their implementation, which may be significant when compared to already cited passive solutions.

2.4.5. Overview

It is possible to observe that standards covering PQ in the LVDC domain are rare, and either do not address current characteristics of DC systems or they cover very specific scenarios. One of the main problems associated to the definition of solid knowledge and rules to guide the LVDC domain is the absence of experimental data. LVDC distribution systems are still rare in the world, and rules concerning

EMC for example are conceived through studies which are based in real experimental scenarios. As already quoted, this is a closed loop process, the more demonstrators and experimental research exist in the domain, the more data is available to substantiate standardization [**MEL22**], and the wider is the range of existing standards, the higher is the level of reliability for future LVDC distribution grids. However, high efforts can be seen from the international standardization community, in the direction of defining new PQ indicators, some of them from scratch, other based on already existing information about AC systems. It represents an important starting point, since many of those indicators are already defined, and calculation methods are already associated to them.

2.5. Conclusion

Three crucial aspects of hybrid AC/DC distribution grids were analyzed in this chapter. Starting with an investigation of different topologies of ICs, different trade-offs have been analyzed, such as cost-robustness, complexity-performance, and efficiency-fault-ride-through. An essential difference between two families of converters was made according to the type of galvanic isolation used along with each type of converter. While classic galvanic isolation has the advantage of being simple and reliable to implement, solid-state galvanic isolation significantly increases the power density of ICs and brings additional features, such as short-circuit limitation.

Second section looked into protection schemes and protection devices. Different standards and multiple studies were reviewed, which tried to bring a clear view of the subject adapted to the LVDC domain. It is necessary to highlight that the solution to some of the challenges associated to the protection schemes in LVDC, such as the application of selectivity and the protection against electric shocks, may be possible through different combinations of protection devices and fault detection algorithms. A crucial trade-off, which is still to be clearly defined, concerns the cost associated to each solution in relation to its performance.

Finally, PQ phenomena and PQ assessment methods were discussed in the last section. It can be observed that existing standards must be adapted to the DC world, but the already present expertise associated to AC systems may be useful as a starting point. Different PQ indicators were defined based on past studies and international standards, however the reliability of this indicators in real experimental scenarios is still to be verified.

A last relevant aspect to be highlighted is that future research works should perform integrated studies, considering the three subjects addressed in this chapter since they mutually influence each other. From one side, the correct operation of the protection system directly impacts the characteristics of transient phenomena, and in the other side, the measurements needed for protection systems to operate are directly disturbed by steady-state phenomena related to PQ indicators. In addition, power electronics have a considerable influence of both PQ and protection systems. The limited fault ride-through capacity of converters and their possible active features to limit short-circuit currents are new characteristics which need to be considered for the design of the protection scheme. Further, the behavior of converters is the origin of ripple, spectrum components and voltage variation, which are important PQ phenomena.

Chapter 3. DESCRIPTION OF THE DIFFERENT DESIGN METHODS AND PROPOSED SOLUTIONS

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3.1. Introduction

This chapter has the objective to present the different choices that guide this research. These choices were made based on different criteria and involve different methodologies used to address the key aspects of this research, which are protection schemes and power quality in LVDC. Since it is not possible to cover all types of DC distribution grids, a well framed case study needs to be defined, aiming at the proposition of solutions for the research answers presented in the beginning of this work. The information presented here serve as well as a base for the results shown and discussed in Chapter 4.

Section 3.2 describes the distribution grid architecture chosen to be studied in this work. Important subjects such as voltage level, grid topology, type of galvanic isolation and main appliances connected to the grid will be discussed in this section. Section 3.3 explains the conception of multiple simulation models. This section represents a large part of this work. Section 3.4 presents the methods used to design the experimental prototype of IC, which will be used further on to validate the simulation modelling and to highlight different phenomena in practice. Finally, the last two sections address, respectively, the design of a selective protection scheme for LVDC distribution systems, and methods to analyze PQ phenomena with a focus on the influence of the IC.

3.2. Distribution grid model

In Chapter 1, many existing possibilities concerning the structure of the distribution grid were presented. As an inference, several voltage levels are possible, along with different architectures, which may be the distribution of more than one pole or the presence of more than one DC bus. The directions analyzed through the studies reviewed in previous chapters guided the choices made in this chapter. This section will focus on the global structure of the distribution system.

3.2.1. Grid topology

As already mentioned, the focus of this research is put on the use of LVDC distribution grids for the residential domain or for commercial buildings. The grid topology theorized here is adapted to this case study and can be observed in Figure 3.1. In this situation, since complex grid topologies, which could demand expensive protection schemes and would not be economically feasible, a simple solution is chosen, where an effort was made to reduce costs associated to stages in the design of the distribution system and necessary equipment.

For a residential or commercial facility, there is no need of multiplicity in terms of distributed voltage levels since equipment and appliances should be standardized in a near future, and other voltages can be locally generated by simple conversion stages. In addition, the possibility of redundancy in terms of poles in the distribution grid does not pay off, as it would involve additional converters or feature which are costly. Still, in the same way, multiple connections to the AC utility grid may not be suited for the present context of distribution grids. As internal LVDC distribution systems spread all over the world, as a way of driving the using of RES, it may become economically reasonable to interconnect multiple local LVDC distribution systems to enhance reliability. However, for the time being, it represents an unrealistic scenario.

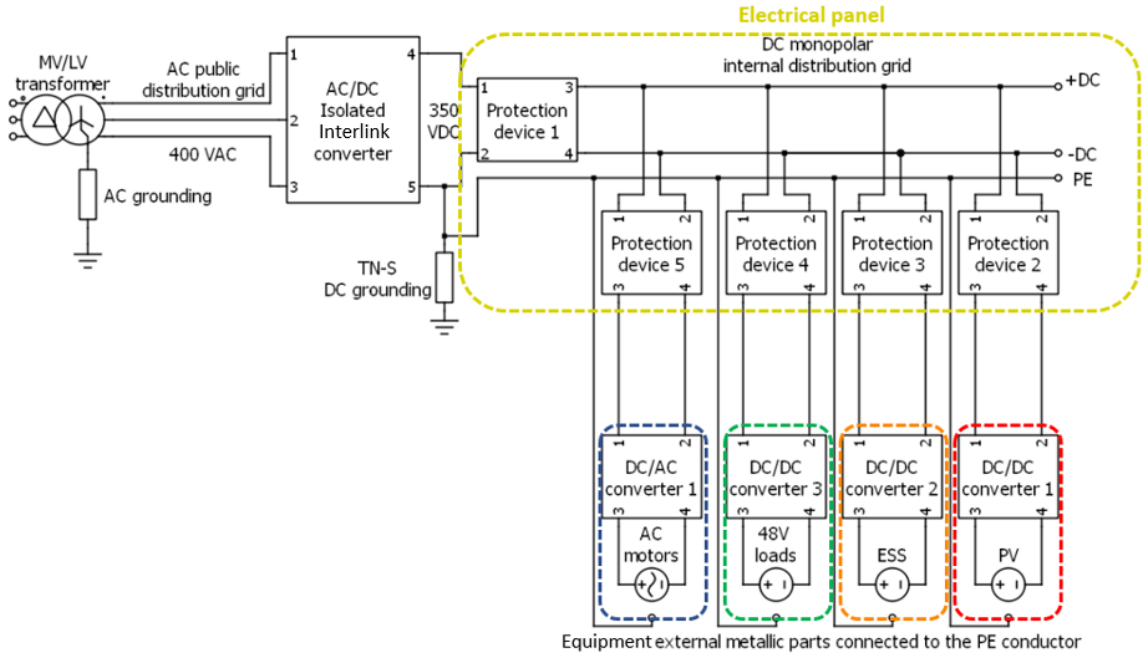


Figure 3.1 Grid topology studied in this work

Taking all the facts above into consideration, the grid topology which will be studied in this research has the following characteristics:

- Monopolar
- Constant or variable voltage level (depending on the control of the interlink converter)
- Single bus with specific conversion stages to other levels, except for shared power feeders
- Hybrid distribution system, public LVAC and internal LVDC
- TNS earthing system
- Converter with galvanic isolation
- ESS operation in grid-following mode.

It is important to consider that inside a residential or commercial building, the physical space may not be abundant. Consequently, it may be crucial to reduce the space occupied by the converters and protection systems as much as possible. For this reason, as already discussed in Chapter 2, in this research a medium-frequency galvanic isolation is considered, which has a considerably higher power density than classic low-frequency ones. Its role in the distribution system will be explained with more details further on in this chapter. Another aspect which is essential for a distribution system is the grounding structure. It impacts the protection scheme directly, especially the protection against earth faults and electric shock. Among the multiple possibilities available for DC systems, in this research the TNS grounding was chosen and the reasons behind it will be discussed later as well.

Analyzing Figure 3.1, it is possible to see that, in a facility were many loads are fed in $48V_{DC}$, it may be interesting to mutualize this specific DC/DC conversation step, from an energy efficiency point of view. An example of such a situation would be a commercial building where multiple offices having electronic devices, such as computers, monitors, and routers, are fed by the $48V_{DC}$ USB-C.

In this concept, all protection devices would be regrouped in the electrical panel of the facility. The objective is to recreate a similar aspect as it is already done in classic AC distribution systems. More details on the specific characteristics of the protection devices will be provided at the last section of this chapter.

3.2.2. Distribution voltage level

The distribution voltage level is the first aspect to be analyzed when a distribution system model is proposed. It has a large influence in the behavior of the grid and in the sizing of all electric materials used in the distribution system, including ICs, load converters, isolation, protection devices and measurement devices.

It was possible to see from Chapter 1 that the choice of the distribution voltage level or levels (if more than one level is systematically distributed along a facility) must be made according to multiple trade-offs. Three main aspects were used in this research, compatibility with equipment, overall distribution efficiency and protection capability.

With a voltage level lower and close to 400V, some AC equipment available in the market can be used with minor or no internal modification. For example, equipment which has an internal DC bus, such as speed-driver-based appliances, may be used directly. Since the classic rectified 230VAC single-phase voltage is around 325V, there would probably not be voltage isolation problems. In addition, this voltage level range represents a good trade-off between protection and efficiency, as it was already demonstrated and proved in the case of Data centers for example, which adopt similar voltage levels (350, 380 or 400VDC). It seems to be the best candidate voltage level to be used in future standards covering the domain of private distribution systems. Finally, this voltage level can easily be stepped down to lower levels without the need of isolated DC/DC converters. Synchronous buck converters, for example, can have a high-level performance while generating 48VDC, which will certainly be useful in future LVDC distribution systems with USB-C powering. For these reasons, the voltage level evaluated as the best suited for the application studied here is 350VDC.

3.3. Design of simulation models

To start the study with the distribution system concept presented in the last section, the first adopted method is to use a simulation software for electrotechnics. It must allow to create models of power electronics converters and grid models as well. There are different software simulation tools that can be used for these purposes, such as EMTP, MATLAB or PLECS. An advantage of the library available in PLECS is that many of the existing components are not completely blocked for the users, in a way that it is possible to search for specific details in the operation of these blocks with the objective to understand or even modify their operation. Finally, basic models of power electronic switches offered by PLECS are simple and can be complexified over time according to the needs of the designer. It represents an advantage since for initial designs, simulations do not take large amounts of time to be implemented, which is not the case for other simulation platforms such as MATLAB/Simulink. For these purposes, in this research the chosen software is PLECS.

Because the development of an experimental prototype is foreseen as another method of analysis in this research, most of the work done in simulation took into consideration what would be possible to reproduce in the laboratory. Consequently, electrical quantities, voltage, power and current levels used in simulation are adapted to this scenario. The main objective here is to remain representative of real-case situations while using scales that could be compared with what is done in practice in parallel.

Another aspect which is important to mention is that, since this research is focused on the DC side of the hybrid distribution grid, the key elements will be the last two conversion stages and the medium-frequency transformer. In terms of operation, they are the parts of the converter which impact

the most the DC grid and, consequently, a larger effort is made on their reliable modelling and their behavior analysis.

As already mentioned, for this distribution system concept, a converter with galvanic isolation was selected. Consequently, the power conversion topology chosen to be implemented in simulation is composed by a first AC/DC stage, followed by another DC/AC stage, a medium-frequency transformer, and a final AC/DC conversion step. The overall structure was already presented in Chapter 2, Figure 2.3. Next sections will show a more detailed version of each conversion bricks as well as the different methods used for the design of each individual component of those converters.

3.3.1. Input AC/DC converter

For the first AC/DC converter, the 2-level VSC was chosen, because of its simplicity and low cost of implementation. Figure 3.2 shows the architecture used in PLECS to simulate the behavior of this converter. In Figure 3.3 it is possible to see the topology of the converter in terms of power electronics.

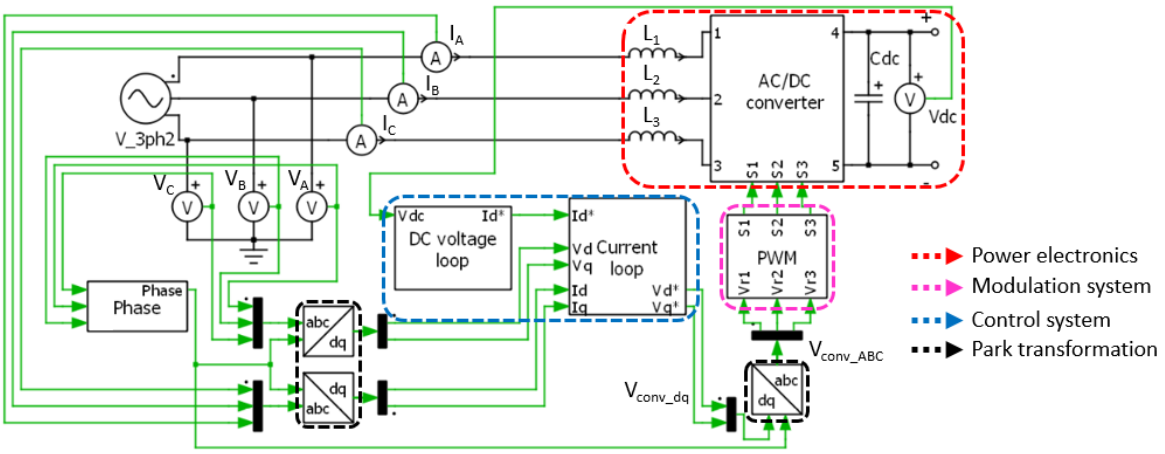


Figure 3.2 Input AC/DC converter model

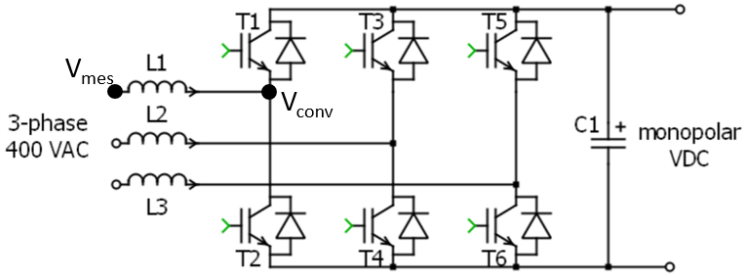


Figure 3.3 2-level VSC topology

3.3.1.1. Control system

For the control system of the 2-level VSC, a classic vectorial strategy is chosen. As already described in section 1.3.2, through the Park Transform it is possible to decompose a balanced three-phase system with a static reference into a two DC components system based on two 90° separated axis (direct *d* and quadrature *q*) with a rotating reference. This new frame has the same angular velocity of the AC grid, which is normally tracked by a Phase-Locked Loop technique (PLL). For this study, since no frequency-variation of the AC grid is considered, there is no need of a Phase-Locked Loop, which

would be necessary in an experimental implementation. Figure 3.4 Park transformation and *dq* frame demonstrates the operation principle of the *dq* frame.

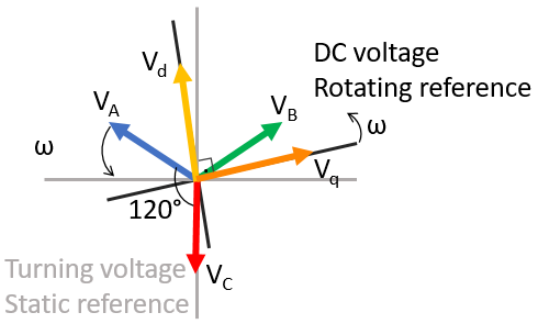


Figure 3.4 Park transformation and *dq* frame

With this new reference it is possible to model the behavior of the 2-level VSC in an open loop configuration, which is necessary for the design of the control system. A cascade control system composed by an inner current loop and an external voltage loop is proposed here as the solution to regulate the AC currents and the DC voltage. The method and all the mathematic equations can be found in detail in [**AKK16**]. From the mathematical model it is possible to find equations (3.1) and (3.2), which correspond to Kirchhoff's second law for the current passing through reactors L_1, L_2, and L_3 in the *dq* frame, where L is the value of inductance in the *dq* frame.

$$\frac{di_d}{dt} = \frac{1}{L}(V_{conv_d} - V_{mes_d} + i_q \omega L) \tag{3.1}$$

$$\frac{di_q}{dt} = \frac{1}{L}(V_{conv_q} - V_{mes_q} - i_d \omega L) \tag{3.2}$$

It is possible to see that the variation of i_d depends on i_q and vice-versa. To avoid this coupling phenomenon, it is possible to design the control system to cancel it, as shown in Figure 3.5. In addition, if the voltage phasor is aligned to *d* axis, active and reactive power can be determined by equations (3.3) and (3.4):

$$P = V_{conv_d} \cdot i_d \tag{3.3}$$

$$Q = -V_{conv_q} \cdot i_q \tag{3.4}$$

In practice, it means that the direct component of the current is used to impose the active power and the quadrature component is used to impose the reactive power. Considering that i_d and i_q are DC quantities, Proportional-Integral (PI) controllers are used in the continuous domain to keep the steady-state error at zero. These controllers are an ideal trade-off between implementation simplicity and performance, principally when implemented in the continuous domain.

The next step is the design of the external loop to control the DC voltage. In this case, the direct current component can be used to control the DC voltage, and its reference comes from the output of the external voltage loop. To regulate the DC voltage through the power flow of the AC/DC converter, the controller can be designed to use the quadratic value of measured DC voltage [**AKK16**]. Here, the regulation is also done through a PI controller.

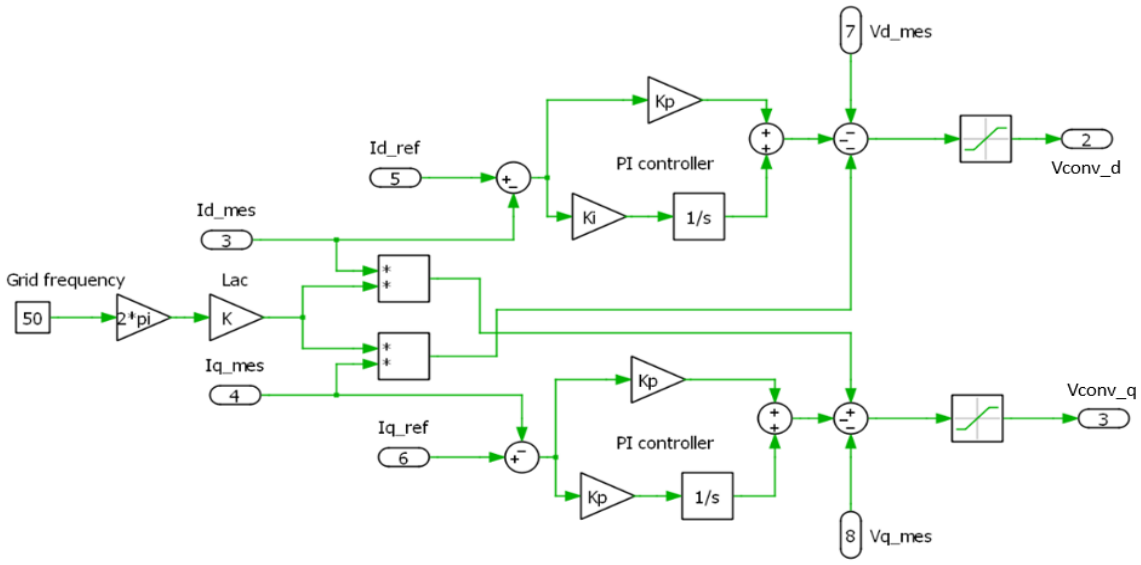


Figure 3.5 Inner current loop of the 2-level VSC

One aspect that must be analyzed in detail here is the overshoot caused by the zero of a PI controller, which is the point in which the transfer function of the controller is zero. Some techniques exist to mitigate the influence of the zero in the dynamic behavior of the regulated quantity. The one used here is the Feedforward technique, which consists into injecting the reference through the proportional gain with an opposing sign, this way reducing the influence of the PI zero in the overshoot without impacting too much the dynamic time response. Equation (3.5) shows the idea behind the feedforward PI controller and its implementations is shown in Figure 3.6.

$$i_{d_{ref}} = \left(V_{DC_{ref}}^2 - V_{DC_{mes}}^2\right)\left(K_p + \frac{K_i}{s}\right) - K_p V_{DC_{ref}}^2 \tag{3.5}$$

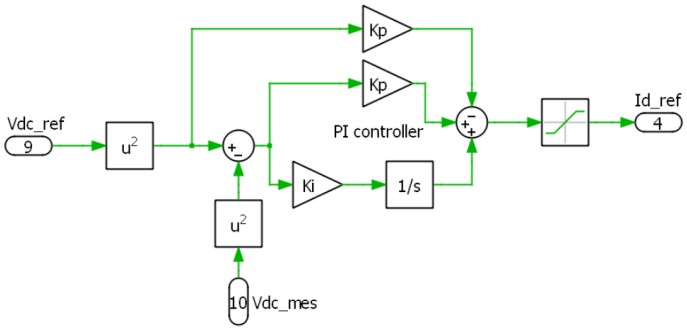


Figure 3.6 External voltage loop of the 2-level VSC

3.3.1.2. Modulation strategy

Many possibilities exist for the modulation technique in the 2-level VSC [**GRA03**], and the most employed ones are: the classic sinusoidal pulse-width modulation (SPWM), modulation with third harmonic injection, space-vector modulation (SVM), and the discontinuous modulation.

In this study, the symmetrical naturally sampled SPWM is used in a first moment. It represents the simplest way of generating the control pulses to drive the semiconductors. The upgrade of the modulation system into regularly sampled SPWM with third harmonic injection can be easily performed in PLECS' simulation environment, which can be useful if an experimental implementation is foreseen. An illustrative demonstration of the implemented modulation system can be observed in Figure 3.7 and Figure 3.8.

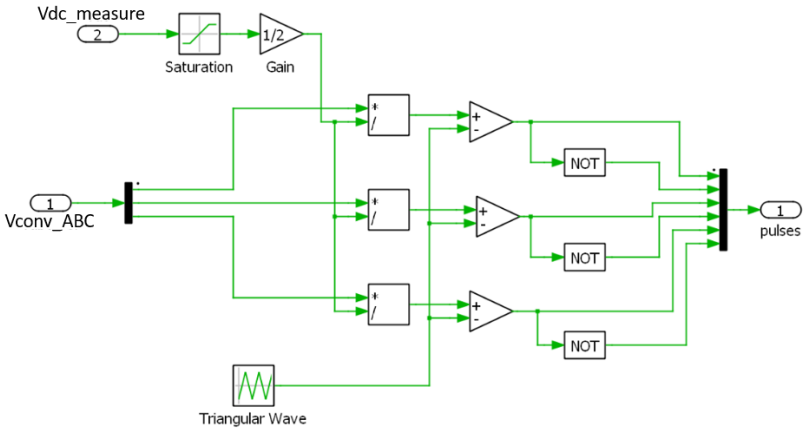


Figure 3.7 Modulation system scheme of the 2-level VSC

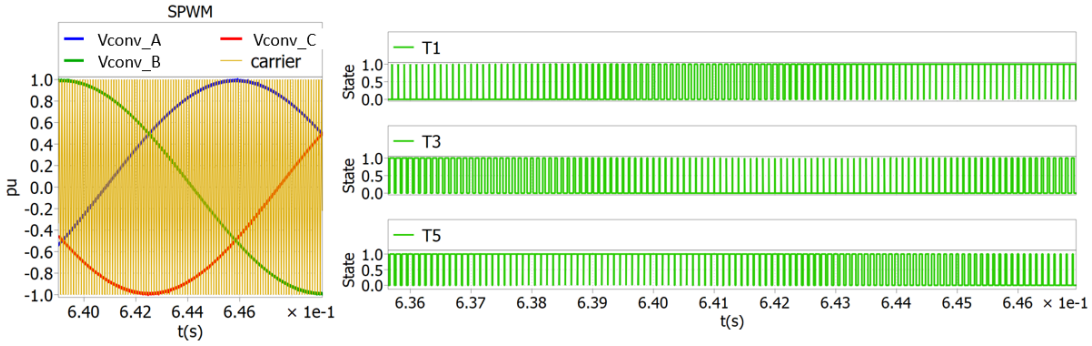


Figure 3.8 SPWM in the 2-level VSC

It is possible to observe that the amplitude of the voltage references created by the control system ($\hat{V}_{abc}$) is normalized according to the DC voltage. Consequently, a signal variating from 0 to the maximum modulation index (M) is generated to be compared with the triangular carrier wave, which here has a frequency of 10kHz. In this case M=1, but the ration can be easily adapted for other types of modulation as well, according to the equation (3.6):

$$\hat{V}_{abc} = M\frac{V_{dc}}{2} \tag{3.6}$$

Figure 3.8 shows the modulation waves being compared to the carrier wave (right) generating the control pulses (left) which are then sent to the gates of the transistors. In the figure only the control of transistors T1, T3 and T5 is shown, but the control pulses of the downside transistors are complementary to the upside transistors.

3.3.1.3. Input and output filters

In the input of the converter, to guarantee a current inertia component with an instantaneous current-source behavior, a first-order inductive filter was implemented. Other possibilities exist, such as second-order inductive-capacitive filters, however this choice is made based on simplicity and cost of implementation once again. Many possibilities exist to the design of the inductive filter. The method used here is the one presented in [**GRA03**], suited for grounded midpoint scenarios. In this method, analytical equations are considered to calculate the RMS value of total harmonic current ($I_{h\text{-}total}$) in the AC side, for 2-level VSCs. It takes into consideration the switching period (T_{sw}), the DC voltage (V_{DC}), the inductance of the reactors in the AC side (L) and the modulation index (M).

For a simple sinusoidal modulation, which is the case of the model considered here, the equation is as follows:

$$I_h = 3\left(\frac{V_{DC}}{L}\right)^2 \frac{T_{sw}^2}{48}\left(\frac{3}{2}M^2 - \frac{4\sqrt{3}}{\pi}M^3 + \frac{9}{8}M^4\right) \quad (3.7)$$

The notion of Total Harmonic Distortion (THD), which represents the ratio between I_h and the RMS value of the fundamental frequency component (I_f), can be used here in order to represent a constraint for the sizing of the input filter. Its calculation is as follows:

$$THD_i = \frac{I_h}{I_f} \cdot 100 \quad (3.8)$$

From these equations, it is possible to derive another equation relating the maximum desired current THD with the inductance of the AC reactors:

$$L \geq \sqrt{100\frac{3\,V_{DC}^2}{I_f\,THD_{i-max}}\frac{T_{sw}^2}{48}\left(\frac{3}{2}M^2 - \frac{4\sqrt{3}}{\pi}M^3 + \frac{9}{8}M^4\right)} \quad (3.9)$$

The output filter used in this topology is a simple first-order capacitive filter. The method used here to choose the capacitance value is based on [**VUJ18**]. The technique considers the influence of the modulation index and the phase angle to calculate the maximum voltage undulation during steady-state operation, which must respect a certain limit of DC peak to peak voltage variation. For the case where there is no reactive power being transferred and the phase angle is zero, the equation is:

$$C \geq \frac{I_{ac_{peak}}}{8 f_{sw} \Delta V_{max}} \quad (3.10)$$

3.3.2. DC/AC/DC converter with galvanic isolation

As already seen in the first two chapters, different options exist for this conversion stage. From a cost and complexity perspective, the topology chosen to be designed in this study is the DAB. However, a slight modification is made in the normal operation of the DAB, in a way that it behaves like a situational SAB. In fact, to simplify the implementation in order to be representative of the operation of the prototype which will be presented further on, only one of the bridges is actively controlled at a time, depending on the power direction. A scheme of the simulation model can be observed in Figure 3.10.

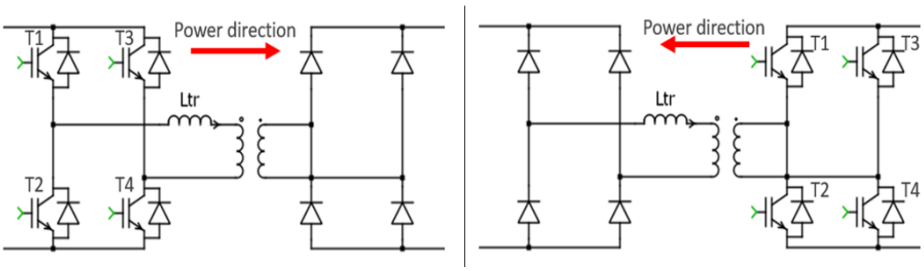


Figure 3.9 Modified DAB operation scheme

The base-topology of the converter in terms of power electronics is shown in Figure 3.9. To facilitate the analysis made in future sections, only the case of the left figure is considered, where power is drawn from the AC grid, which represents the most recurrent scenario for grids such as the one studied here. Since the global energy management of the grid is not the focus of this research, the unidirectional study will be used to conduct further design stages.

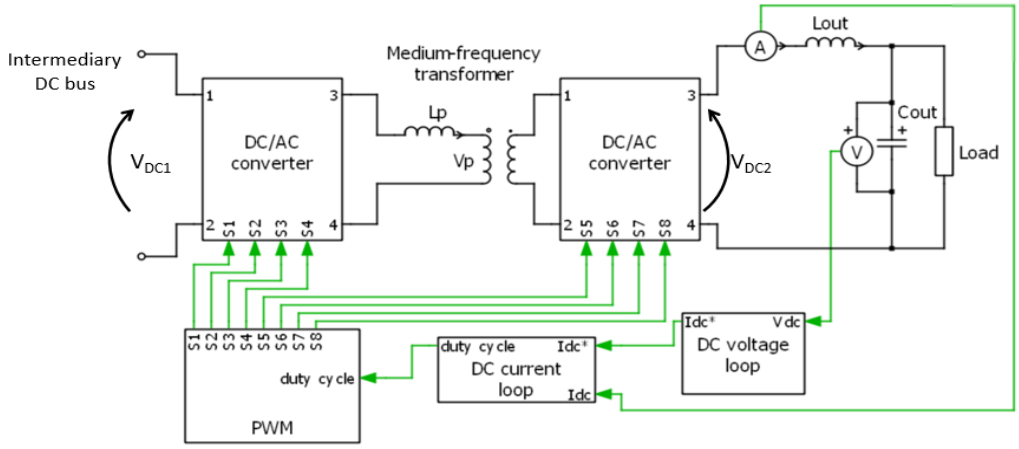


Figure 3.10 Simulation model of the bidirectional DC/AC/DC converter

3.3.2.1. Control system

Since this stage of the converter is used directly to control the main DC bus of the distribution system, it is studied here with much more detail than the control system of the 2-level VSC. The final objective is for the simulation model to serve as a base for the implementation of the experimental prototype further on. While for the 2-level VSC only a continuous domain control is considered, for the modified DAB, a digital control version is designed. It is important to understand this process, since the real implementation of the control system will be done through a computational engine, which operates in the discrete time domain [**LIU09, TRI10**].

The control strategy used for this converter [**SLO22b**] is, once again, the double nested loops. The internal loop is responsible for regulating the current passing through the output reactance, and the external loop controls the output DC voltage (V_{DC2}). In addition, once more the PI controller is chosen for the control system, which is interesting in this stage since the digital implementation of a PI controller is rather simple.

As already seen, in the continuous Laplace domain, PI controllers are the addition of a pure proportional gain and an integral gain. To convert it into a digital model, the strategy proposed here is to use Tustin's Transformation [**HIN20**] to go from the Laplace domain to the Z discrete domain. It is important to highlight that Tustin transform may cause instabilities related to the commutation process. If it is the case, backward Euler or weighted Tustin [**YAN10**] can be used as well and may solve the problem.

$$PI_{continuos}: H(s) = K_p + \frac{K_i}{s} => \ PI_{discrete}: H(Z) = \frac{r_0 + r_1 \cdot Z^{-1}}{1 - Z^{-1}} \tag{3.14}$$

Where:

$$s = 2 \cdot f_{samp} \cdot \frac{Z-1}{Z+1}, r_0 = \frac{\frac{K_i}{f_{samp}} + 2 \cdot K_p}{2}, r_1 = \frac{\frac{K_i}{f_{samp}} - 2 \cdot K_p}{2} \tag{3.15}$$

The final objective is to find a control law which could be executed by a computational device. From this point, it is necessary to convert the equations to the discrete time domain, obtaining the recurrence equations of the digital version of the PI controllers. They are a function of the sample (k), the control variable (Y), and the error between the commanded reference and the actual measured output (X).

$$PI_{digital}: Y[k] = Y[k-1] + r_0 \cdot X[k] - r_1 \cdot X[k-1] \tag{3.16}$$

In a real system the acquisition of voltage and current measurements is done through different types of sensors and analog-to-digital converters (ADCs). It is important to highlight that their performance may impact the control system and, consequently, they must be taken into consideration during the design of this control system. In most cases, sensors have a conversion gain associated, which are called K_{Imes} for the current measuring sensor and K_{Vmes} for the voltage equivalent.

From this point, measures are already reduced to an analog processing voltage signal, which is the input of the ADCs. The N-bit ADCs can be modeled by sampling and quantization processes. The sampling stage is represented here by a Zero-Order Holder (ZOH) operating at the sampling frequency f_{samp}, while the quantization is represented by a gain called K_{bin} and a rounding operation. These two steps are responsible to change the continuous scale variating from zero to the maximum reference voltage of the ADC, to the 2^N available quantization levels that will be interpreted by the computational device. In this process, N is the resolution in bits of the ADC output and, as a consequence, $K_{bin} = 2^N - 1$.

Taking all these gains into consideration, the results in the adapted recurrence equations can be seen below. The external loop calculates the current reference, and the internal current loop gives the duty cycle as an input to the modulation system.

A last optional step is considered here to maintain the calculation time reduced while using reasonable computational power. To achieve this goal, it is chosen to consider only integer variables. To do that it is necessary to adapt r_0 and r_1 coefficients through a gain called K_{int}, so that they can always be integers. Coefficient K_{int} is a multiple of 10 and it can be chosen according to the precision required by the control loop.

$$I_r[k] = I_r[k-1] + \frac{K_1}{K_2} K_{int} \cdot r_{0V} \cdot \Delta V[k] - \frac{K_1}{K_2} K_{int} \cdot r_{1V} \cdot \Delta V[k-1] \tag{3.17}$$

$$D_c[k] = D_c[k-1] + \frac{K_2}{K_3} K_{int} \cdot r_{0i} \cdot \Delta I[k] - \frac{K_2}{K_3} K_{int} \cdot r_{1i} \cdot \Delta I[k-1] \tag{3.18}$$

Where:

$$K_1 = \frac{K_{bin}}{V_{refADC}} \cdot K_{Vmes}, K_2 = \frac{K_{bin}}{V_{refADC}} \cdot K_{Imes}, K_3 = K_{bin}, K_{int} = 10^m \tag{3.19}$$

After these final considerations, the result is a hybrid simulation model, where the power electronics calculations are made in continuous time domain and the control system operates in the discrete time domain. Figure 3.11 illustrates this concept while Figure 3.12 shows the model in PLECS simulation platform.

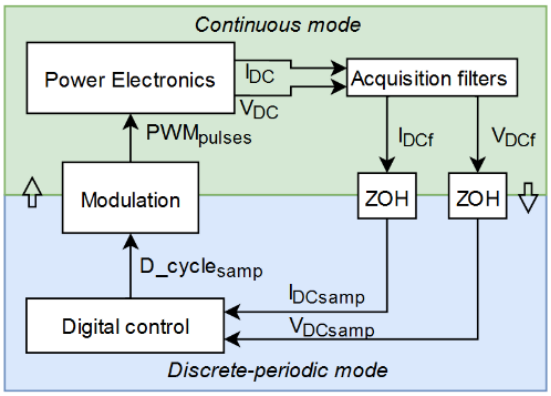


Figure 3.11 Hybrid simulation model

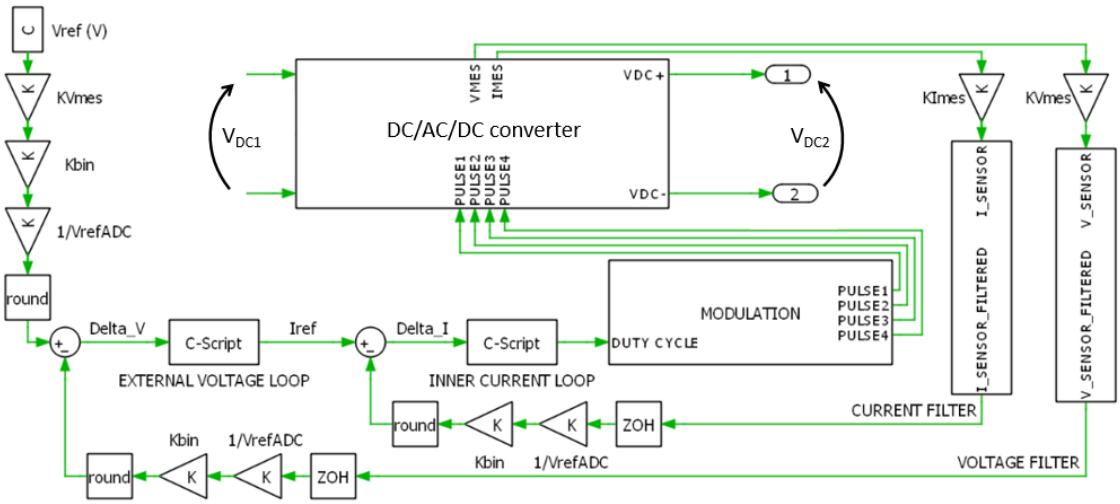


Figure 3.12 Complete control model of the modified DAB

The final objective of this simulation modelling strategy is to try to be as close as possible of the real experimental prototype. Consequently, the choice of the multiple parameters that make part of the determination of the control laws will be made in parallel with the implementation of the prototype. Multiple results will be presented further on.

3.3.2.2. Modulation system

The modulation system in this topology needs to guarantee a zero-mean voltage in the medium frequency transformer to avoid the saturation of its magnetic core. Since for each operation point the DAB behaves exactly like the SAB, there are two main options for the modulation system, which were already discussed in Chapter 2: the duty-cycle modulation and the phase-shift modulation. The output voltage feature, which is the voltage in the primary side of the transformer, is essentially the same for both modulation systems. The difference is the way each arm of the active bridge is controlled in terms of conduction state of the switches.

Since calculations are easier to make in function of duty-cycle than phase-shift angle, the duty-cycle modulation is chosen to pilot the converter proposed here. The scheme of the modulation system is shown in Figure 3.13. Duty-cycle coming from the control system is compared to a triangular carrier wave of 40kHz, generating the pulses which control the gate of the transistors. The chosen switching frequency represents a reasonable trade-off between the capacity of computational engines to send a new value of duty-cycle to the modulation system per each switching period, and the reduction of the filtering capacity of passive components. In practice, the higher the switching frequency, the smaller the inductance and capacitance values of passive filters, however the higher is the needed computational power, since the calculation window is smaller.

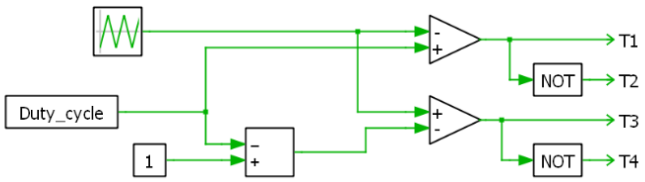


Figure 3.13 Modulation system for adapted DAB

A graphic representation of this system can be observed below, in Figure 3.14 (left). The result is an alternating voltage square wave form, which is the input voltage of the medium-frequency transformer. The features of the wave can be observed in Figure 3.14 (right), where α is the duty cycle

calculated by the control system and T_{sw} is the commutation period. It is important to highlight that, in this modulation strategy, the duty cycle must be limited to 50% to avoid the overlapping of the control pulses.

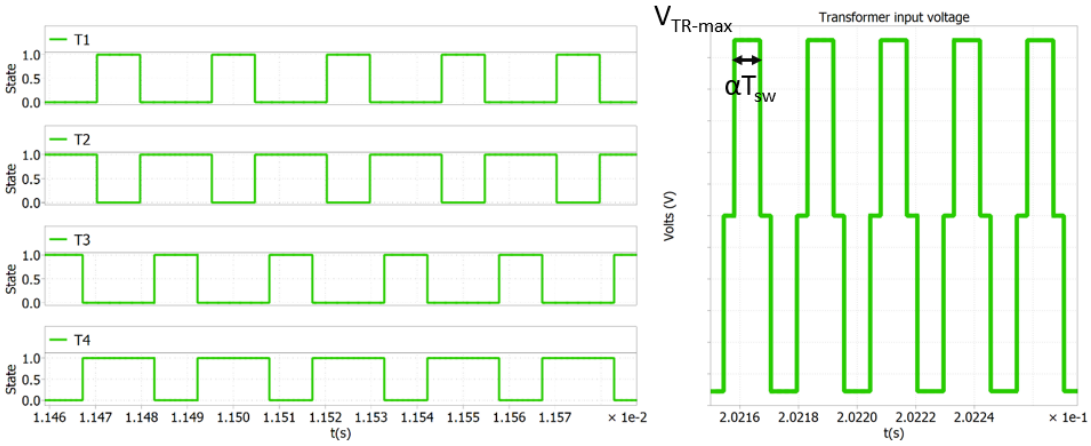


Figure 3.14 PWM control pulses

3.3.2.3. Input and output filters

The input filter for the modified DAB is the same capacitor already designed as the output filter of the 2-level VSC to ensure the same stability of the first DC bus as the one already studied in simulation. The output filter considered for this topology is a second-order LC filter. The reactor is used to limit the instantaneous variation of current in case of short-circuit in the DC distribution grid and to extend the continuous conduction operation mode of the converter. This operation mode is achieved when the current in the output of the converter does not reach zero at each switching period.

To calculate the inductance, a simple analysis can be made according to the Kirchhoff's laws. The filter can be seen in Figure 3.15, along with the typical wave form of the rectified voltage on the DC output (V_{red}), whose non-null voltage period is αT_{sw}.

Using Kirchhoff's second law it is possible to obtain:

$$V_{red} - V_{DC2} = L\frac{di}{dt} \tag{3.20}$$

Considering the instantaneous mean values of the equation above, assuming V_{DC2} as constant during a commutation period, and knowing that a single-phase full bridge diode rectifier doubles the frequency of the voltage wave, it is possible to obtain the following equation, from which it is possible to determine the L value that limits the current variation:

$$L \geq \frac{(V_{DC1-max} - V_{DC2})\alpha T_{sw}}{\Delta I_{max}} \tag{3.21}$$

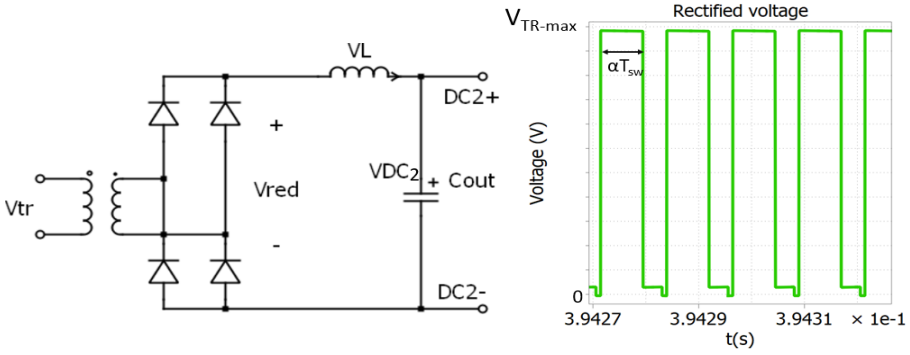


Figure 3.15 Output filter design

For the calculation of the output capacitor, the cut-off frequency equation was used to allow a 3dB attenuation on a desired frequency. This filter is generally designed to mitigate the influence of the lowest frequencies present in the output DC voltage (V_{DC2}), which may come from the input converter or from the AC grid. However, a second capacitor may be needed to filter spectral components in higher frequencies.

$$C \geq \frac{1}{(2\pi f)^2 L} \tag{3.22}$$

3.3.2.4. Medium-frequency transformer

In this first part of the modelling on the converter topology, a simple ideal transformer is used. The only parameters considered here for now is the transformation ratio, and the leakage inductance of the transformer (L_{tr}). A more detailed model will be considered further on in parallel with the construction of the experimental prototype. For this initial model, the transformation ratio is considered as unitary, and the leakage inductance value is 50µH.

3.3.3. Thermal modelling

The design of a protection plan adapted to hybrid AC/DC distribution systems must take into consideration the analysis of the behavior of ICs when submitted to short-circuits. A fault ride-through capability is, in the end, a level of thermal endurance. From this point of view, the most vulnerable components in terms of temperature transient are power semiconductors. Consequently, it is important to investigate the thermal modelling of power switches and what is the impact of fault-related temperature transients.

PLECS' simulation environment allows the modelling of the thermal behavior of power switches. In general terms, temperature variations in power switches are due to two types of preponderant losses: conduction and commutation losses. Considering the structure of a commutation cell, as shown in Figure 3.16, conduction losses (Zone 2) correspond to the power dissipation in the internal On-state resistance of switches. They are calculated when the top-side switch (T1) conducts, and the down-side switch (T2) is blocked and vice-versa. On the other hand, commutation or switching losses come from the intermediary state of switch, in which it is neither conducting neither blocking. In this state, either current is falling, and voltage is rising (Zone 3), either the opposite (Zone 1). Usually, Zones 1 and 3 are defined in manufacturers' datasheets through dissipated energy levels, E_{off} for turning-off energy dissipation and E_{on} for turning-on energy dissipation.

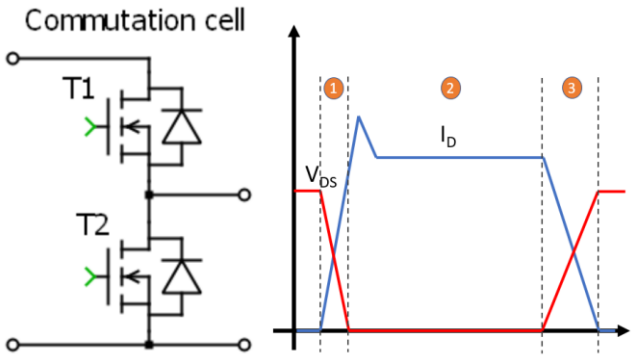


Figure 3.16 Conduction and commutation losses in a power switch

Inside the PLECS' model of power switches, it is possible to define conduction and commutation losses in terms of datasheet graphics or equations. From these inputs, PLECS can perform

the calculation of the instantaneous power dissipation in the power switches according to the following equations:

$$V_f = V_t(T_j) + R_{DS_{ON}}(T_j) \cdot I_D \tag{3.23}$$

$$P_{cond} = V_f \cdot I_D \tag{3.24}$$

$$P_{switch} = \left(E_{on}(T_j, I_D, V_{DS}) + E_{off}(T_j, I_D, V_{DS})\right) \cdot f_{sw} \tag{3.25}$$

with:

V_f - forward voltage in the power switch

I_D - current in the power switch

V_{DS} - blocking voltage in the power switch

V_t - threshold voltage in the power switch

$R_{DS_{ON}}$ - channel resistance during ON-state

T_j - junction temperature

P_{cond} - conduction loss

P_{switch} - switching loss

Note that the threshold voltage and the ON-state resistance are usually a function of the junction temperature of the power switch, while the dissipated energy during commutation is a function of the junction temperature, the current, and blocking voltage.

Beside from the modelling of losses, in PLECS environment it is also possible to build a thermal circuit, where different components can be represented. Losses coming from power switches are converted in heat flow by a block called Heat-Sink. From there it is possible to determine thermal impedances corresponding to each one of the interfaces between the components. An illustrative representation of this technique is shown in Figure 3.17.

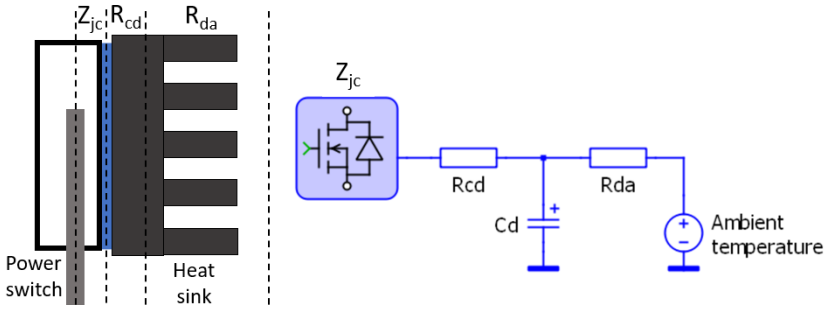


Figure 3.17 Thermal modelling of power switches

with:

Z_{jc} - thermal resistance between junction and case

R_{cd} - thermal resistance between case and heatsink

R_{da} - thermal resistance between heatsink and air

With the models above it is possible to supervise the temperature variation for different operation points of the IC, as well as measure its thermal endurance during different types of faults.

3.4. Prototype materials design

Besides simulation models, the second method proposed in this work to address the protection and power quality aspects in hybrid distribution systems, is the construction of an experimental prototype composed by an IC, protection devices and load-simulation equipment. The first objective of this proposition is to use the developed equipment to improve simulation models, so that they are reliable, and results correspond to real laboratory scenarios. In second place, different experiments may be able to confirm certain assumptions made theoretically and also show eventual challenges which were not foreseen during previous stages of this research.

3.4.1. Semiconductors

The most important components in power electronics converters are the power switches. For all designs presented in sections 3.3.1and 3.3.2, different technologies of semiconductors can be considered. A first distinction can be made according to the characteristics of the internal junctions in a switch. From a power electronics point of view, two types of switches stand out: Insulated-Gate Bipolar Transistor (IGBTs) and Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs).

Both technologies ruled over the domain of power electronics for the last few decades. Being able to use conductivity modulation due to the double polarity, IGBTs have the capacity to keep conduction losses low even when operating in high-voltage level systems [**GON20**]. In the other way around, MOSFETs offer the advantage of high turn-off speed due to inexistent reverse recovery time and charge recombination. Consequently, their switching losses remain low, which enables the use of this semiconductors in high frequency switching converters [**GON20**].

A second important characteristic of power switches is the chemical composition of the semiconductors. Silicon-based (Si) switches exist for decades and the experience around its utilization in different power switches and converter topologies is vast. They are still used today in the most part of the power switches available in the market.

Nonetheless, another technology of semiconductors arrived bringing some advantages in crucial aspects if compared to classic silicon-based switches. They are known as Wide-Band Gap (WBG) semiconductors, and the most promising chemical compositions are the Silicon Carbide (SiC) and the Gallium Nitride (GaN). The addition of Carbon and Nitrogen increases the junction temperature limit of the semiconductors, going from 150°C with pure silicon to 175°C or even 200°C [**OZP04**]. Besides, due to the enhanced dielectric strength created by a wider band gap than Si, SiC and GaN semiconductors provide a higher breakdown field, resulting in the capability of blocking higher voltage levels [**OZP04**]. Another advantage of this effect is that for the same breakdown voltage, On-state resistance of WBG semiconductors is considerably lower. Finally, the electron mobility in WBG semiconductors is also higher, meaning that turning-off and turning-on times are lower, which makes those devices suited for high-frequency operation converters [**BEI19**].

However, there are also some differences between SiC and GaN semiconductors. While the electron mobility is higher with GaN, the thermal conductivity is higher with SiC [**OZP04, SHA22**]. This way it is possible to see that GaN devices may be more adapted for high switching frequency applications [**BEI19, MIL13**], while SiC may be suited for high power applications [**TRI14, TRI16, SHA22**].

Since one of the main objectives of this work is to find an optimal design of selective protection scheme and considering that the short-circuit endurance of the IC is a challenge, it seems that the best option is to profit from the good efficiency, high thermal conductivity, and high frequency operation of SiC MOSFETs. They have already been used in similar converter topologies [**LAG18**, **VER19**] for DC applications and they will be used for the design of the IC.

3.4.2. Medium-frequency transformer

The design of medium-frequency transformers can be highly complicated, since it involves determining multiple parameters, like magnetic core material and size, conductors' type, parasitic impedances, maximum magnetic field and others [**KAW22, JIM21**]. The designing stage is often done with the help of Finite Element Modelling software, as it allows to accurately represent the magnetic flux as a function of the geometrical shape of the transformer [**SAH21, AGA23**]. Although, considering that accurately modelling and construction of a medium-frequency transformer is not the main objective of this research, a simple designing method is going to be used.

The first stage is to determine the best material for the magnetic core, in terms of operation voltage and specially operation frequency. From previous studies, it is possible to see that the most used materials for this type of transformer are amorphous alloy, nanocrystalline and ferrite. Interesting comparisons are made in [**ZHA22, FOU20**] showing that amorphous alloy may be privileged for high power applications due to its high saturation magnetic flux density, while ferrite may be favored for high frequency application since the core losses are low. On its turn, nanocrystalline is a good compromise between both characteristics, but it is still an expensive material.

All that being considered and knowing that the prototype to be built will not be designed for high power operation, the best option seems to be a Ferrite core. Different types of ferrite cores exist [**MAG01**], among them two stand out for their low core losses and optimal frequency operation: the Ferrite N87 [**TDK23**] and N97 [**EPC06**]. Both operate optimally from 25 to 500 kHz and the losses of N87 (57 kW/m^3) are slightly superior to N97 (45kW/m^3) at 25kHz operation.

The second stage of the designing process concerns the calculation of the primary and secondary number of windings to avoid the saturation of the transformer. To address this subject, it is possible to use Faraday's law (3.26), parametrized and rearranged for the current application with squared voltage waves [**FOU20**], in order to obtain the minimum number of winding turns in the primary side (3.27) in function of the maximum magnetic field.

$$V(t) = -N\frac{d\Phi(t)}{dt} \tag{3.26}$$

$$N = \frac{V_{DC}}{4fAB_{max}} \tag{3.27}$$

Where:

Φ - magnetic flux

N - number of turns in the winding

V_{DC} - maximum voltage in the primary side of the modified DAB

f - frequency of the squared waves in the transformer

A - effective area of the magnetic core

B_{max} - saturation magnetic field

A final consideration is that, to avoid high conduction losses due to the increase of resistance caused by the skin effect in medium-frequency range, in general, this type of transformer is made with Litz-wire [**KAW22**]. In practice, for a defined current, Litz-wire is made from multiple small section insulated conductor strands composing one wire. This way, the equivalent area of the conductors through which current is passing is greater than if a single core conductor is considered. Since resistivity is inversely proportional to the effectively used section area of the conductor, the resistance of the wire decreases.

3.4.3. Capacitors

Considering the entire IC (Figure 2.3), it is possible to see that there are two capacitive filters. The first one is placed at the output of the 2-level VSC, which is also the input of the modified DAB. The second one is placed at the output of the modified DAB. Two different approaches are necessary for the choice of the technology of both capacitors.

The first capacitor filter needs to have a considerable energy storage capacity since the switching frequency of the 2-level VSC is not elevated (10kHz). It also needs to be able to operate in voltage levels above 600V since the 2-level VSC can only be controlled over the input peak AC voltage level between two phases (563V). That being considered, the best options for this filter are electrolytic or polypropylene film capacitors. Due to the Equivalent Series Resistance (ESR) being low for most of the film capacitors and no imperative need of high energy density, this is the technology chosen for the first capacitive filter.

For the second capacitive filter, the output voltage is not that elevated (350V) and there is no need of high storage capacity, since the frequency of the rectified wave in the output of the modified DAB is 80kHz. Another important aspect is that this filter must be responsible for mitigating the presence of high frequency spectral components coming from semiconductors switching. In this way, two different technologies may be needed, the first one having a certain voltage inertia behavior, and the second one to filter high frequency components. The appropriate composition seems to be the association of an electrolytic capacitor for voltage inertia and stability with a polypropylene film for improving power quality in the distribution system.

3.4.4. Output inductor

The inductor present in the output filter of the modified DAB needs a particular attention in terms of design. Since it is placed after the rectifier, this inductor is going to be submitted to a strong DC component, which may saturate the magnetic core of the inductor if it is not correctly dimensioned. To avoid this phenomenon, which may be responsible for considerable reduction in the reactor's inductance, the technique usually applied is to increase the capacity of the inductor to store energy. To do that, one option is to use local or distributed gaps in the magnetic core.

A magnetic material, which looks to be the most adapted one to this type of application, is the iron powder. Since its fabrication procedure involves the use of high pressures to condensate iron powder in a solid shaped structure, it naturally offers a distributed gap, which increases its capability of storing energy. The trade-off associated to the presence of a gap is the reduction of relative magnetic permeability, which means in practice that more turns are necessary in the winding to achieve a certain level of inductance.

To choose the correct core shape, area, and number of turns in the winding, manufacturers usually provide graphics relating the energy stored in the inductor with the magnetomotive force (3.28) necessary to generate this energy. In [**MIC07**] it is possible to find a demonstration of design of DC inductors. The same strategy is used in this work, in which the storage energy of the inductor is calculated in function of the operation point and conducts, at the end, to the calculation of the minimum turns in the reactor's winding to produce the desired energy. The factor relating the magnetomotive force with the stored energy is the magnetic flux, which is a function of the material of the magnetic core.

$$Stored\ Energy = \frac{1}{2}LI^2 = \Phi \cdot (N \cdot I) \tag{3.28}$$

3.4.5. Computational device

The computational engine is defined here as the digital core responsible for acquiring the analogic measurements, converting them into digital values, doing the calculations necessary for control loops and generating the control pulses which are sent to the power switches. From previous studies [**BUC12, TRI10, WAT11**], it is possible to see that, in power electronics, the most used computational engine are microcontrollers (µCs), Digital Signal Processors (DSPs), and Field Programmable Gate Arrays (FPGAs).

The advantage of using µCs is that they are the least expensive component among the ones cited above, and they are simple to configure. They usually have one ADC unit for the acquisition of different measures, and, in addition, power electronics dedicated µCs include PWM units which are user-friendly to use. From another perspective, they are the least performing computational engine. Floating-point, and sometimes even integer operations, can be complicated to execute in real time if the switching frequency of the converter is considerably high.

One great benefit offered by DPSs is the presence of hardware multiplication through Multiply and Accumulate units. They allow a considerable reduction of the number of clock cycles needed to execute operations with integer and floating-point variables by parallelizing these operations. This may be useful for successive computations in loops which must be executed in short periods of time. This is exactly the case of control loop calculations for power electronics converters. Another upside of DSPs is the recurrent presence of more than one ADC core. Consequently, it is possible to execute the acquisition of multiple signals measurements in parallel, which results in another improvement in the overall performance. In addition, DSPs may also have a Direct Memory Access (DMA) which can be used by the ADC core to store measured values without passing through the Microcontroller Unit (MCU). In practice it may represent a gain in terms of calculation time because the MCU may have less tasks to execute.

Finally, regarding FPGAs, they bring the best overall performance. Sometimes equipped with a microprocessor, they can execute complex digital processing functions in short time windows. They are composed of arrays of logic blocks which are completely programmable. Thus, they have high flexibility, and their performance can be adapted to the needs of specific applications. They include multiple Input/Output ports which are also more performant in terms of functioning speed, allowing real-time operation. In addition, they have the capacity of allocating hardware to execute multiple functions in parallel, which makes FPGAs the best option for high-performance power electronics converters.

From this perspective, since DSPs are more performant options than µCs, a less expensive solution than FPGAs, and considering that they are easier to program, in this work they are chosen as the main computational engine for the IC.

3.5. Selective protection scheme design

As already seen in Chapter 2, it is usual for the protection scheme to be divided in two different strategies: protection against short-circuit, and protection against electric shock. Concerning the protection again short-circuit, two types of short-circuit must be studied: pole-to-pole and pole-to-ground (according to Figure 3.18). The first to be analyzed are the pole-to-pole faults (sections 3.5.1.2 to 3.5.1.5), and the pole-to-ground faults will be addressed in a following special section (3.5.1.6), since the earthing system plays a very important role in this last case.

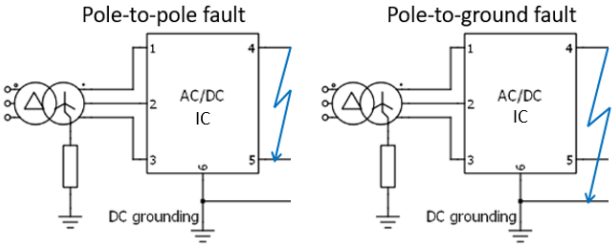


Figure 3.18 Types of faults in an asymmetrical monopolar DC grid

3.5.1. Current limitation-based protection plan

This is the main technique of the overall protection scheme designed in this work. One of the benefits of using solid-state galvanic isolation through a medium-frequency transformer is that the conversion steps associated to it allow a limitation of short-circuit currents. Through this technique, it is possible to improve the thermal endurance of the IC and source-associated converters, which makes it simpler to design a selective protection plan with proper security margins.

The methodology proposed here is to use Thermo-Magnetic Circuit Breakers (TMCBs) or ultra-fast fuses (UFF) as a first line of protection for the IC and source-associated converters, which are also equipped with current limiting control and complete shut-off capability as a back-up protection. Since the IC is the main responsible for feeding the distribution system, it is also secured by AC protection as a third line of protection. Next, all different feeders used to power loads are protected by DC TMCBs. Each stage of the protection plan will be described in next sections.

3.5.1.1. Current limitation technique for the IC

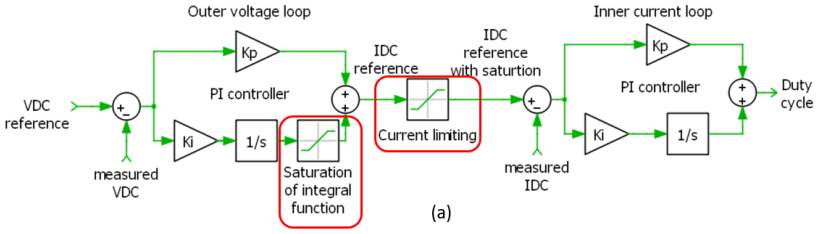
To understand the following proposition of control strategy, it is important to understand the behavior of the DAB during fault. What happens is that the discharge of the output capacitor in the fault will create a voltage dip, which the control system will try to compensate by harshly increasing the current reference. As a final consequence, the current levels will increase drastically as well, potentially damaging the power switches. This way, a control strategy to avoid this dynamic is necessary.

The technique described here do not correspond to the natural current limiting capability of the classic DAB operation described in Chapter 2. The objective here is to introduce a control law in the regulation loops to limit the current to any desired value, including zero current operation. The modified DAB proposed here allows this type of control operation since there is no forward polarized diodes during short circuits and the current feeding the fault can be completely stopped or limited acting on the duty-cycle.

The simplest way of implementing this functionality in the control system of the converter is to act in the reference of the inner current loop. Since the output current reference is given by the outer

control loop, it is possible to act in the voltage control laws to change the value of the current reference according to the situation. In practice, in the continuous domain, it means to add a saturation function in the output of the controller (Figure 3.19-a), and in a digital domain, it can be easily done with a simple comparison (Figure 3.19-b). This technique must consider the saturation of the integral function of the voltage controller (anti-windup) to prevent it from reaching very high values, which could slow down considerably the return to normal operation.

Aiming at a robust protection scheme, it is usually important to consider the worst-case scenario. Regarding the strategy presented above, the worst-case would be the failure of the first line of protection during current limitation operation of the converter. This problem can be solved through a temporization followed by a complete shut-off of the converter. Based on the execution period of the control loop, a flag can be used to maintain the current limiting operation through a certain period. After that time delay, it is possible to force the current reference to zero and shut-off the converter stopping the power flow. The entire dynamic can be observed in Figure 3.20, which represents in practice the fault ride-through characteristic of the converter.



I_{max} = X; %Maximum value of current
I_{k}_ref = f(I_{k-1},r_0,r_1); %Recurrence equation of the voltage control loop
If (I_{k}_ref > X) %Comparison loop to saturate current reference
{I_{k}_ref = X;}

(b)

Figure 3.19 Current limitation technique in continuous (a) and digital (b) domains

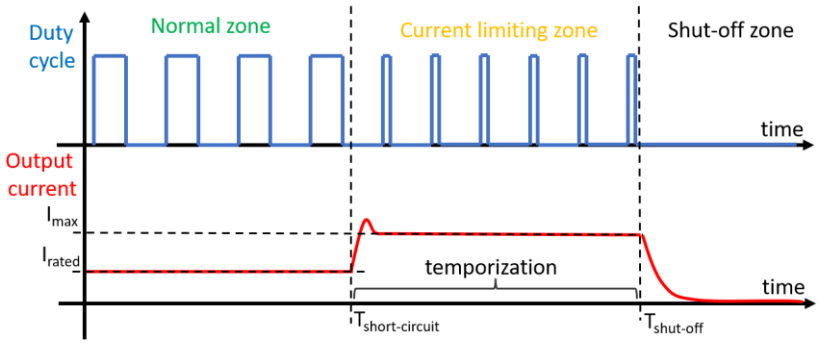


Figure 3.20 Fault ride-through and current limitation technique

Note that, since the impedance of a short-circuit is usually low, to limit the short-circuit current as proposed above depends on reducing the duty cycle to very low values. In a digital system, the lowest the duty cycle can go without reaching zero (shut-off stage) is determined by the computational device and the resolution of the PWM unit. This way, the higher the voltage levels used in the converter being controlled, the harder it is to limit the short-circuit currents to low values.

This technique may be useful for increasing the thermal endurance of the converter, restricting the uncontrolled augmentation of current level during faults. In this manner, the current limitation may result in enough thermal endurance to enable the use of classic protection devices in cascade, such as ultra-fast DC fuses or DC TMCBs.

3.5.1.2. First line of protection of the IC against short-circuit

As already stated, the fact of being capable of limiting short-circuit currents may allow the use of classic protection devices for the IC. The use of TMCBs seems to be a better overall solution than UFFs. Fuses are associated to the need of maintenance and needing of replacement in case of melting, while TMCBs can be easily rearmed if the fault is cleared. However, ITOC curves of TMCBs offer larger margins (±20% according to IEC 60947-2 [**IEC16**]), compared to UFFs (maximum ±10% according to IEC 60269-4 [**IEC09**]). This way, depending on the rated current and characteristics of protection devices downstream (protecting load feeders for example), and the thermal endurance of the IC, it may not be possible to use a TMCB to protect it without breaking selectivity. In this case, an UFF must be designed to protect the IC.

From another perspective, the use of UFFs to protect the IC should not be problematic. Even maintenance should be rare, considering that if the protection scheme is well designed, the UFF will only melt in the case of a fault in the DC bus or in case of failure of downstream protection devices.

3.5.1.3. AC protection in the IC

Another possible problem for the strategy presented above would be the complete failure of the control system. The consequence of that would be high current levels passing through the power switches of the IC. If this situation persists for a long-time duration, it could result in fire by overheating, component failure and even explosion. To prevent that from happening, it is possible to use TMCBs at the AC side of the IC, respecting the rules of selectivity and the temporization described in the section 3.5.1.1.

3.5.1.4. Protection of load feeders

The strategy proposed here is to protect load feeders with DC TMCBs as well. In order to design a selective protection scheme, it is important to coordinate the operation of TMCBs with the UFF or TMCB protecting the IC. To do that, rules presented in [**SOC16**] for fuse-TMCB coordination and in [**NER01**] for TCMB-TMCB coordination may be used. The complete coordination of the IC with the load feeders can be observed in Figure 3.21.

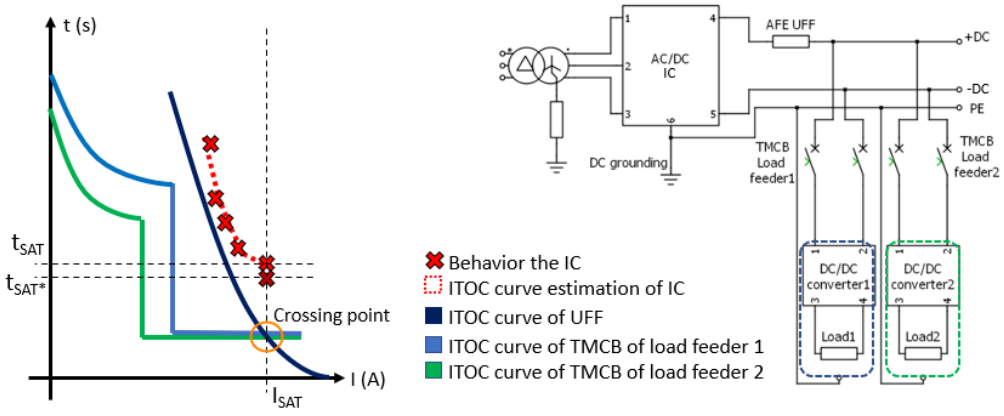


Figure 3.21 Coordination of protection devices protecting the IC and load feeders

Note that, to maintain the full selectivity functionality in the system, current levels must be limited to smaller values than the crossing point shown in Figure 3.21. If short-circuit levels reach higher values than the one on the crossing point, it means that the UFF protecting the IC will melt, and all loads will be shut-off. Consequently, the crossing point is a good candidate for the maximum current considered in the current limitation technique.

Looking into different ITOC characteristics of TMCBs, it is worth mentioning that the more the tripping curves of protecting load feeders are placed to the left, the greater are the margins for selective coordination. In this perspective, Z curve TMCBs become particularly interesting, as the ones possessing the smallest tripping current thresholds.

Another important consideration is that t_{SAT} represents the period of time through which the IC can maintain the current at the saturation limit imposed by the control system. This value may be used as base for the determination of the temporization associated to the complete shut-off of the IC. A certain margin can be used here as well to avoid destruction, which, in practice, means using t_{SAT*} instead of t_{SAT}.

A last important aspect to be highlighted is that, as already discussed in the previous chapter, the operation of classic protection devices to stop a fault creates an electric arc. The overvoltage created by the electric arc may be dangerous for the semiconductors in the output of the IC, which may conduct to the need of overvoltage protection. To solve this problem, many possibilities exist, such as the use of MOVs or Transient Voltage Suppressor (TVS) diodes, however this specific aspect is not studied in this research.

A flowchart representing the methodology employed in this work to reach a selective protection coordination is shown in Figure 3.22. This methodology should be followed, once a first design of the IC is already made according to all the aspects already mentioned in previous sections of this chapter, in addition to the rated power of the installation.

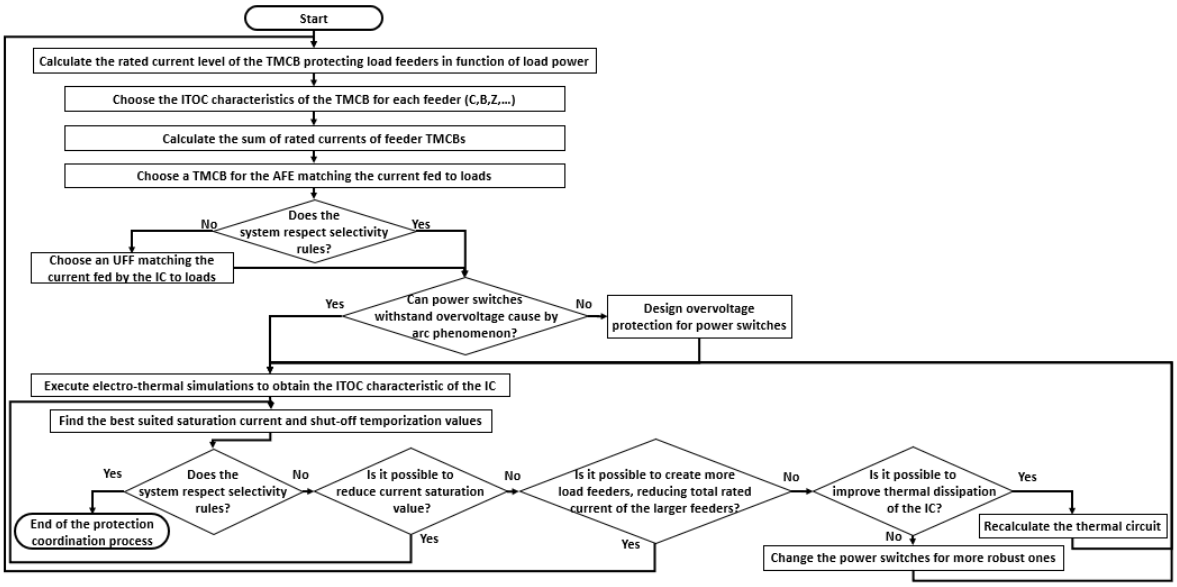


Figure 3.22 Selective protection coordination flowchart

3.5.1.5. Protection of ESS and PV

The distribution system designed in this work may consider the presence of ESS and PV. From this perspective, additional and specific protections must be used in feeders in which these devices are connected. The challenge associated to the presence of ESS and PV can be summarized in the following two aspects. First, during a fault in the ESS/PV feeder, being energy sources, they represent additional short-circuit currents in the fault. Second, a fault in the DC bus, which should trip the central IC protection, would continue to be fed by PV and batteries even when the IC is already disconnected from the grid, creating a nonintentional islanding mode operation. Both cases can be observed in Figure 3.23.

This way, it is important to shut-off the feeders in which these systems are connected in all fault scenarios. Overcurrent protection is not well suited in this case as a first line of protection to the distribution grid, since it is potentially unable to prevent damages in the grid. Similar scenarios are already covered by standards, such as the NF EN 50549-1 [**NFR19**] on requirements for connecting generation plants in LV domain. The recommendation here, which seems adapted for DC systems as well, is the use of anti-islanding protection devices. In AC systems, these protection devices trip through over/under voltage detection and over/underfrequency detection. In DC systems, their operation would be simpler since no frequency measurement is needed. In the aforementioned NF EN 50549-1 standard, the recommendation is an instantaneous tripping for a voltage level under 85% and over 110% of the rated voltage of the distribution system. These values may be used as a base for DC systems as well, however they may be adapted according to grid operation strategies. For droop-control based DC grids for example, both thresholds may be extended, since a natural voltage fluctuation is necessary to indicate generation-consumption imbalance.

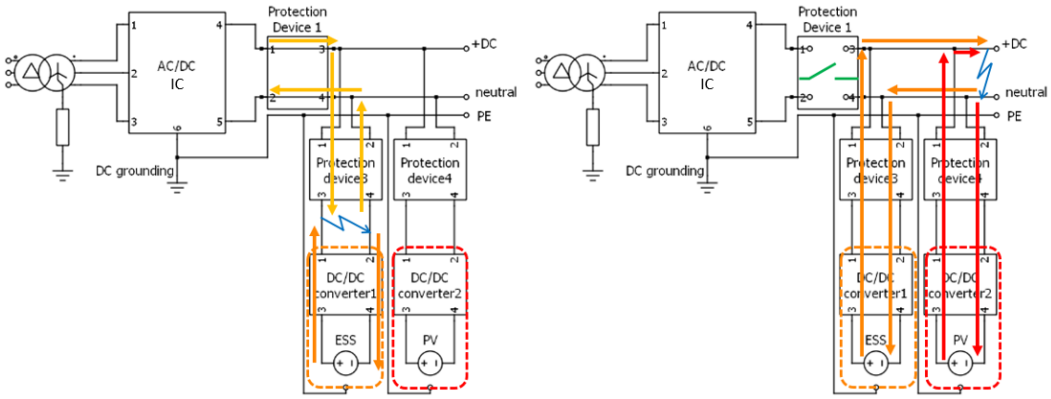


Figure 3.23 Fault scenarios with ESS and PV – feeder fault (left), DC bus fault (right)

In addition to the anti-islanding protection, it is also important to protect the DC/DC converter associated to PV or ESS. To do that, the topology of the converter considered here is crucial. The use of buck/boost topology as the interlink converter, which has no current limitation control, would conduct to the need of very short time response protection (SSCBs). This statement is more preponderant in the case of ESS, given the high short circuit current levels of this type of system.

This way, the proposition here is to use the SAB for PV and the DAB for ESS. Since the disconnection of the equipment must be done instantaneously, the strategy of current limitation presented for the IC must be adapted. From the moment that the control system of the DC/DC converter detects a current greater than the rated current, it should force the duty-cycle to zero and shut-off completely the power flow. In case of control system failure, an UFF can be employed to isolate ESS and PV from the system, as a back-up protection device.

3.5.1.6. Protection against pole-to-ground fault and electric shock

Before entering the subject of pole-to-ground fault and electric shock, it is necessary to understand the choice of the earthing system. As already stated, in the concept of hybrid distribution system studied in this work, the TN-S earthing system is chosen. Three main aspects seem to make TN-S the best solution for residential and commercial DC distribution grids. First, this type of distribution system does not need a high level of scalability, solving a major drawback of TN-S systems. Second, IEC 60364-1 [**IEC05**] declares that RCDs are only needed as complementary protection. This statement comes from the fact that the fault loop of a pole-to-ground fault is the same as the one of a pole-to-pole fault, which means that the main overcurrent protection should be enough to protect the system in this case as well. Third, DC distribution systems present many interlink converters connected to the grid,

which implies that common-mode disturbances may be present at considerable values. Since the PE conductor in TN-S grounding represents a low-impedance path for leakage currents, the impact in voltage related to PE may remain at acceptable levels.

Following the ideas presented above, it is possible to see that no additional protection measures are imperative to protect the system against pole-to-ground faults. However, it is possible to profit from the measuring systems associated to the IC to create a residual current detection. The idea here would be to use them to measure the current from both poles and take advantage of the computational engine to supervise the comparison between the two values. Similar to AC RCDs, a threshold could be configured in the control system to trip instantaneously the complete shut-off of the IC in case of leakage currents exceeding the threshold. This way, the residual current detection operates as another line of protection for the safety of users.

As already established in Chapter 2, an electric shock can be originated from a direct or an indirect contact. Once again, it seems pertinent to follow the recommendations presented in IEC 60364-1 [**IEC05**]. The use of class II installation equipment and cables should be enough to protect users from a direct contact. An indirect contact or insulation fault, on its turn, behaves like a pole-to-ground fault with slight modifications of the fault loop, and the measures presented above should be adequate to protect users. An important remark is that to protect users, a threshold of residual current of 80mA is being proposed by the international technical specification IEC/TS 63053 [**IEC17b**].

3.6. Influence of the front-end AC/DC converter in power-quality phenomena

The Power Quality (PQ) domain is vast, including multiple phenomena which need to be characterized and evaluated to grant acceptable levels of EMC in a distribution system. For DC systems, the analysis of PQ is particularly challenging since standards did not yet determine which precise indicators are to be considered. With the objective to address a part of this subject, this work will focus on the influence of the IC, as the voltage source of the distribution system, in relation to PQ phenomena.

3.6.1. Transient disturbances assessment

It is possible to observe a considerable influence of grid-connected converters in this type of phenomena. From one point of view, if the operation limits of power electronics devices are respected, voltage inertia components as well as the control system are able to mitigate voltage transients, dips and swells. Consequently, the presence of the IC, as well as the multiple interlink converters, may operate like a shield to moderate the impact of this phenomena in loads.

3.6.1.1. Voltage transients, dips, and swells from the AC grid

The impact of disturbances coming from the AC grid can be measured and evaluated according to well established standards. In addition, they usually do not create high level disturbances in the DC side of the grid. Overvoltage transients in the AC grid not surpassing the limits of breakdown voltage of the power switches used in the 2-level VSC rarely impact the DC grid. Its output capacitive bus may be designed to grant enough instantaneous voltage inertia for the modified DAB to operate and maintain voltage between acceptable values. The 2-level VSC being a natural voltage step-up topology, in general switches are chosen to endure considerably high-voltage levels, which renders the system even more robust against voltage transients.

Voltage sags and swells in the AC grid are even simpler to manage. In this work, it becomes more evident since the distribution system is deployed to two distinct conversion steps with two control loops in cascade. This configuration is capable of compensating AC sags and swells permanently in a defined operation range, which is an important PQ indicator of sensibility to AC voltage variations. Figure 3.24 illustrates the operation dynamic in case of voltage sags and swells.

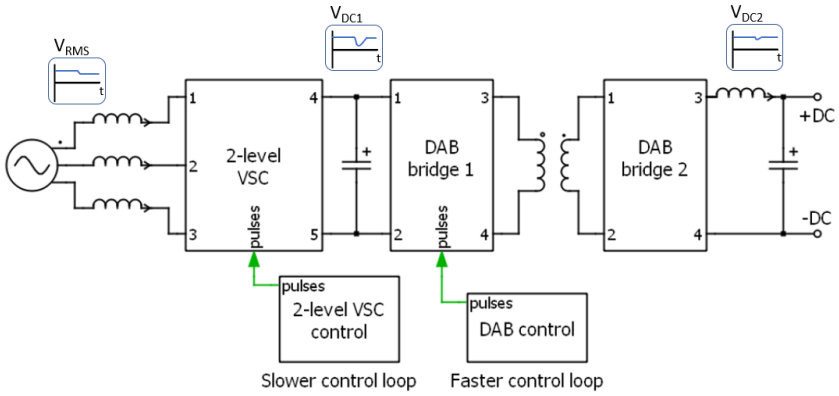


Figure 3.24 Sensibility to voltage dips and swells

AC voltage variations will directly impact the first capacitive DC bus, even if less drastically than voltage transients. The control loop of the 2-level, which is the slower one, is responsible for bringing the voltage in the capacitive bus back to normal operation values. On its turn the faster loop of the modified DAB is responsible for maintaining the normal voltage in the distribution grid according to the slower modification of its input voltage.

Even if there is an analytical way of calculating the operation limits of the converter to compensate voltage sags and swells, the simulation models conceived in this work are a simpler way of achieving the same results. This analysis must consider individual and cascade operation of the 2-level VSC and the DAB.

3.6.1.2. Voltage transients, dips, and swells in the DC distribution grid

The same phenomenon in DC is more complicated to evaluate since no established rules regulating the domain are available yet. Nonetheless, once again it is possible to see that design and operation of the IC and other interlink converters throughout the grid are deeply associated to these phenomena.

The main causes of voltage transients are lightning strikes, fault arcs, and the re-powering of the distribution system. Concerning lighting, the facility must be equipped with well-designed lightning rods and earthing systems to avoid destructive overvoltage. In terms of overvoltage caused by fault arcs, a possible solution was presented in the last section to protect interlink converters, and consequently loads. In relation to the mechanism of re-powering the system, the IC may be equipped with a soft-start function in the control system. In practice, it consists in slowly incrementing the voltage reference imposed at the voltage control loop, this way avoiding dangerous voltage variation dynamics. Figure 3.25 illustrates this technique.

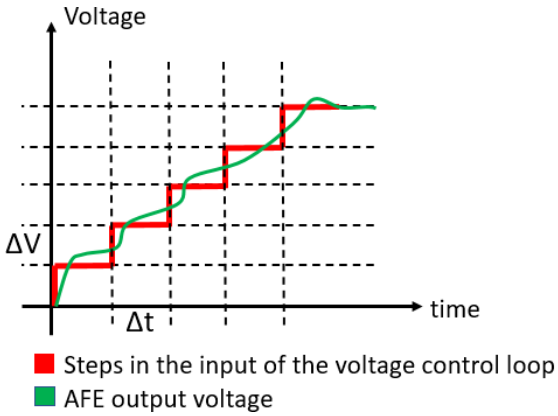


Figure 3.25 Soft-start technique used in the IC

Concerning voltage dips, the main origins of these phenomena are related to load changes. In this aspect of PQ analysis, DC systems present some particularities. As it was already shown in this chapter, DC/DC converters used as an interface with loads, PV and ESS in DC distribution grids, usually have an input capacitive filter. The connection or start-up of these converters may be the source of high inrush currents, which can heavily impact the voltage of the DC grid by creating voltage dips.

From this perspective, when a DC/DC interlink converter is connected to the grid, two problems emerge: the high inrush currents can trip protection devices of the feeder and the voltage dip can impact the operation of the other feeders. Consequently, additional components are imperative to maintain the correct operation of the distribution grid. The idea is to use components capable of limiting the inrush currents or to pre-charge the input capacitors of the converters connected to the grid, which can be done through resistors, reactors, or power electronics.

Other situations of load increase with less drastic inrush currents may also cause voltage dips in the DC distribution system. This condition can be handled by the control loops of the converter. In this scenario, two control features associated to the IC are important to highlight, which are the time response, and the overshoot. Time response can be considered as the time employed by the IC to make the distribution voltage level return to normal operation band, while the overshoot represents the percentage of voltage exceeding the targeted voltage in relation to the maximum voltage change caused by load variation. A graphic representation of both indicators is shown in Figure 3.26.

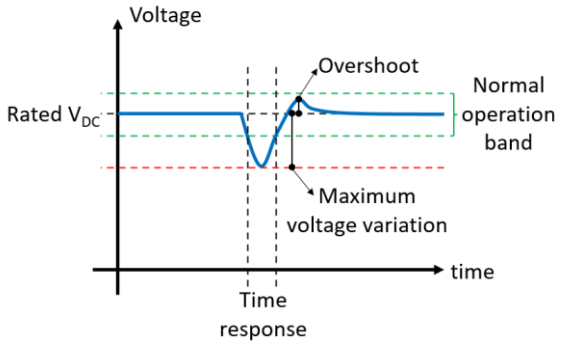


Figure 3.26 Time response and overshoot of the IC in the presence of load variation

Although according to [**IEC20**] time slots were already fixed to differentiate PQ phenomena, normalized voltage envelopes defining operation zones are yet to be defined. This way, it is not yet possible to impose solid generalizable rules for the operation of ICs control systems.

Voltage swells are also caused by load variations most of the times. Thus, the same methodology applied to address voltage dips can be also used to deal with voltage swells. Once again, the control

system of the IC plays an important role to mitigate the impact of this phenomenon in the distribution grid.

3.6.1.3. Attempt of finding established rules to regulate the behavior of the IC

As seen in the last few paragraphs, the operation of the IC represents an important impact on the analysis of PQ related phenomena in LVDC distribution grids. This way, an interesting perspective for the future seems to be the standardization of the performance of the IC in terms of the indicators already mentioned (time response and overshoot), among others.

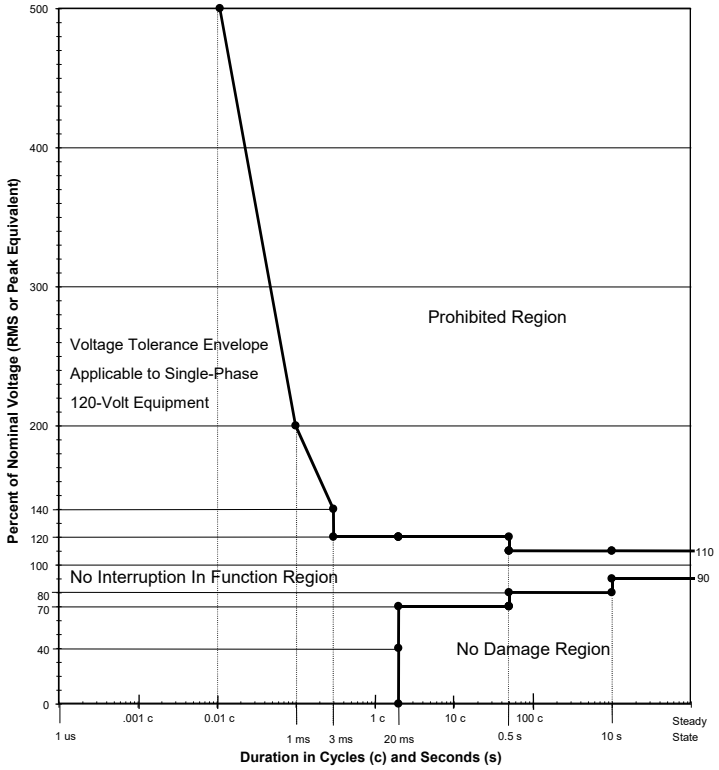


Figure 3.27 ITIC curve for IT equipment immunity to voltage variations [ITI97]

Two transitory voltage immunity curves are well known to define the operation limits for equipment connected to a distribution grid, which are the one defined in the IEC61000-4-11 and the one proposed by the Information Technology Industry Council (ITIC) [**FER22, CHI09**]. Since the ITIC curve is the most conservative (Figure 3.27), the proposition here is to use it and its limits as a base to configure the control system of the IC. It means to use the ITIC curve as a power furniture requirement instead of equipment immunity to disturbances. Time and voltage envelope may need to be changed in the future, according to the characteristics of DC systems, but this methodology may represent a starting point.

The idea is to set certain control parameters of the IC, such as proportional and integral gains, to execute different types of load variations, and to observe if the control response of the IC corresponds to the limits established by the ITIC curve. It can be done either in simulation or field experiments.

3.6.2. Steady-state disturbances assessment

As it can be expected, the operation of the IC also has a major effect in steady-state disturbances for DC distribution systems. It is possible to see that not only the IC is responsible for ensuring certain

steady-state voltage characteristics, but its internal components, control and modulation systems influence the way that current disturbances created by non-linear electronic-piloted loads impact the DC bus voltage.

3.6.2.1. Different characteristics in the IC influencing PQ indicators

Since the IC considered here is a complex structure, that is composed by different conversion stages and control systems, multiple are the factors that affect the presence and intensity of spectral components in the output DC voltage. As already discussed in Chapter 2, it looks pertinent to analyze steady-state PQ indicators, such as RMS ripple and distortion spectrum, by frequency slot, since measuring techniques and calculations may be different. A parallel analysis can be made regarding which feature of the IC is the most significant in certain frequency range to mitigate disturbances, as summarized in Figure 3.28.

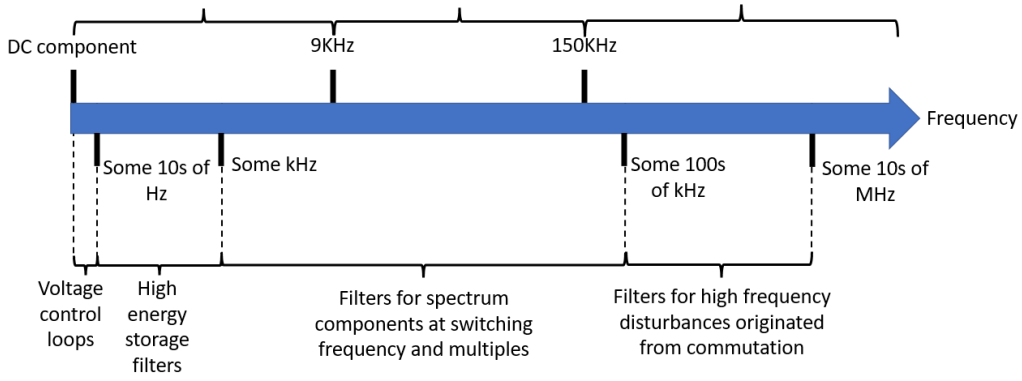


Figure 3.28 Frequency slots according to distinct measuring techniques and according to the impact of different features of the IC

The frequency slots considered here are: [0-9kHz], [9kHz-150kHz] and [>150kHz]. They were already identified by other research works [**SLO22a, YAN20**], in which it is possible to see that each one of these slots may be associated to specific measuring techniques.

a. Frequency slot from 0 to 9kHz

The first element influencing the presence of disturbances in the DC distribution voltage is the control system of the IC. It has a bandwidth associated to its time response to voltage variations (e.g., load changes). From this perspective, it can be seen as a filter for very low frequency spectral components of DC voltage (few Hz to some tens of Hz). Disturbances in this frequency slot are generally related to resonance phenomena between multiple regulation systems, which can cause instability. It may be a crucial aspect to be studied in ring-based grid topologies where there is more than one voltage source converter, and the distribution system is controlled by drop-control algorithms. This is the reason why the regulation speed of control loops in parallel must respect certain decoupling laws. Since it is not the case for the current work, no more details will be presented next concerning the subject.

Another type of spectral disturbance in this frequency slot is related to the use of passive rectifiers. The AC voltage coming from the utility grid may be disturbed by harmonics from 0-2kHz, and they may impact the DC grid as well. This way, high energy storage filters may be needed in the IC. A pertinent candidate to this function seems to be the output capacitive filter of the 2-level VSC, this way low-frequency disturbances do not impact the operation of the modified DAB. Consequently, when designing this filter, it is important to look for capacitor technologies with high ripple current features.

Finally, for relatively low switching frequency modulation systems, the disturbances created by the current chopping at the switching frequency and its multiples may impact the DC grid as well.

Therefore, another filter is needed to mitigate the presence of these perturbations. The best suited candidate appears to be the output filter of the modified DAB, since it may be designed to attenuate disturbances created from switching in both conversion steps of the IC.

b. Frequency slot from 9 to 150kHz

In this frequency range, most part of disturbances introduced by the IC in the DC voltage come from the current chopping. Thus, the solution to attenuate them is practically the same as the one presented in the last paragraph. An important comment must be made though: the output filter of the IC needs to ensure a certain voltage inertia, which is mandatory for stability and for the voltage control system. Consequently, it is important to design the filter to bring a certain capability of storing energy while maintaining a sufficient level of capacitance to filter the required frequencies. For filters working in this frequency slot, features like Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) are crucial since they impact the frequency-dependent impedance of the capacitors and their filtering ability. From this perspective, if a single capacitor is not capable of offer both characteristics, it may be necessary to use different technologies in parallel.

c. Frequency slot for spectral components above 150kHz

In this frequency slot, two disturbance sources can be highlighted. The first one is the same already mentioned coming from current chopping, this time appearing at frequencies which are multiple of the switching frequency of the conversion steps in the IC. A method of addressing this problem has already been presented.

The second type of disturbance is also related to commutation, but it is associated to drastic voltage variations in power switches. Since there are always parasitic/stray inductances in every converter associated to connectors, electronic board routes and bus bars, drastic state changes generate voltage transients at high frequencies, which can achieve hundreds of kHz or some tens of MHz. The natural frequency of these disturbances depends on the capacitive effects associated to power switches, filters, and on the parasitic inductances. They represent a potentially problematic effect since they are a source of conducted and irradiated Electromagnetic Interference. Further, these disturbances can affect not only the IC itself and its operation, but also sensible equipment connected to DC grid, as they may disturb measuring sensors, microcontrollers, drivers, and electronic voltage sources.

The classic solution to this type of voltage transients is to use snubber filters as close as possible to the power switches. Nonetheless, it is important to highlight that snubbers for SiC MOSFETs, which were chosen as the main technology for power switches in this work, are particularly important. One of the main advantages of SiC MOSFETs is the capability of switching at high frequencies. The inconvenient associated to this fact is that the high-speed voltage variations may generate violent voltage transitory phenomena. Many methods exist to design this type of snubber circuits but, since this work will use an experimental prototype, methods such as the one proposed in [**ROH20b**] seem to be well suited for this application. Different types of snubber circuit exist as well, the proposition here is to use the simplest one, which is the use of one capacitor per commutation cell (Figure 3.29). The design of the snubber capacitor is based on an energy inequality, in which the capacitor must be capable of storing the energy of the stray inductance during commutation. The calculation is shown in equation (3.29), where V_{surge} is the maximum transient voltage measured during commutation.

$$\frac{1}{2}CV^2 > \frac{1}{2}LI^2 \rightarrow C_f > \frac{L_S I_m^2}{V_{surge}^2 - V_{DC}^2} \tag{3.29}$$

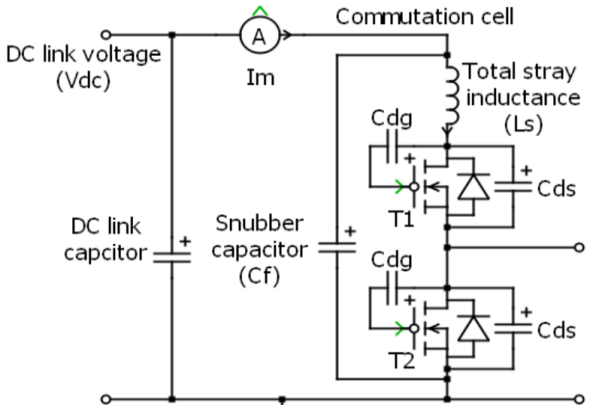


Figure 3.29 Proposition of snubber capacitor

3.6.2.2. Frequency-dependent impedance identification methods

The characteristics of the voltage wave in a DC distribution grid are a function of the voltage delivered by the IC, and of the load disturbance emissions through cable impedances. In previous paragraphs, only the voltage delivered by the IC was addressed. However, it is equally important to understand how to evaluate the impact of load disturbances. From this perspective, a crucial point for steady-state PQ studies in the DC domain seems to be the frequency-dependent behavior of the IC under the effect of load disturbance emission. To understand this aspect, it looks important to investigate the way steady-state PQ analysis is done in AC and what differences exist, in this context, for a similar analysis in DC. In this scenario, two aspects are important to be compared. First, the main power furniture architecture. While classic AC distribution grids include a low-frequency power transformer upstream of the point-of-common-coupling (PCC), DC distribution grids have an IC upstream. Second, classic AC distribution grids are rarely significantly disturbed by low-frequency (LF) components above 2kHz, which is not the case of DC systems since switching converters are often used.

In the AC case, the LF impedance seen from the distribution system is not complicated to determine. It usually corresponds to the transformer short-circuit impedance and it is sufficient to accurately estimate the impact of low-frequency disturbances from characterized loads on the PCC voltage (Figure 3.30). In contrast, the IC in LVDC systems has a dynamic non-linear behavior in the presence of disturbances, which, in addition, needs to be defined for a larger frequency range than the AC case. One possibility to address this subject is to represent the behavior of the IC through a frequency-dependent impedance model (Figure 3.30). The challenge comes from the fact that the IC impedance non-linearly depends on the frequency and on its operating point [**RYG16**]. Nonetheless, different methods exist to determine this impedance model [**SLO23a, SUM04, JOR11, JES15, ZHO14**].

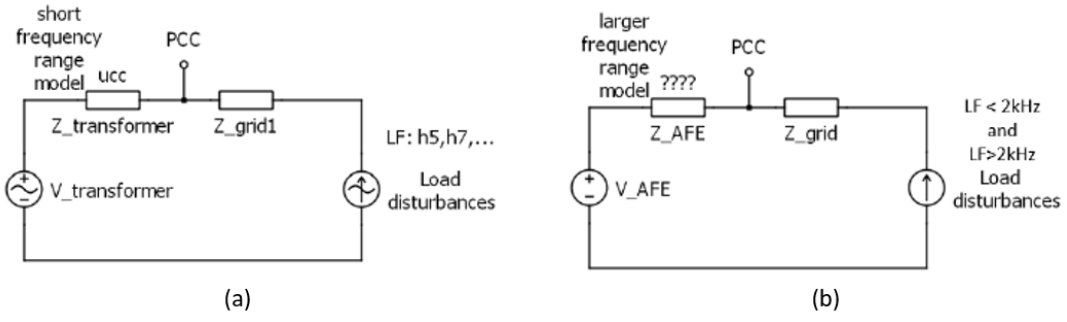


Figure 3.30 Comparison between steady-state PQ analysis in classic AC (a) and DC (b) distribution systems

In this work, the chosen technique consists in injecting a known current disturbance in the IC, measuring the impact in the output voltage and calculating the frequency-dependent impedance model through Fast-Fourier Transform (FFT). As shown in Figure 3.31, the shapes of the disturbing current are selected to be a squared wave, and a variable frequency sinusoidal wave. The first method is easier to execute, mostly in real experimentations since it needs to be executed only once to determine a multifrequency impedance model. However, in this first method, the intensity of each spectral component decreases, which hinders the capacity of performing high accuracy measurements. In contrast, the method of variable frequency sinusoidal disturbance waves needs to be executed as many times as the number of desired spectral components used to define the impedance model. However, since the magnitude of the disturbing current at each frequency is controlled, it remains considerably more precise than the first method.

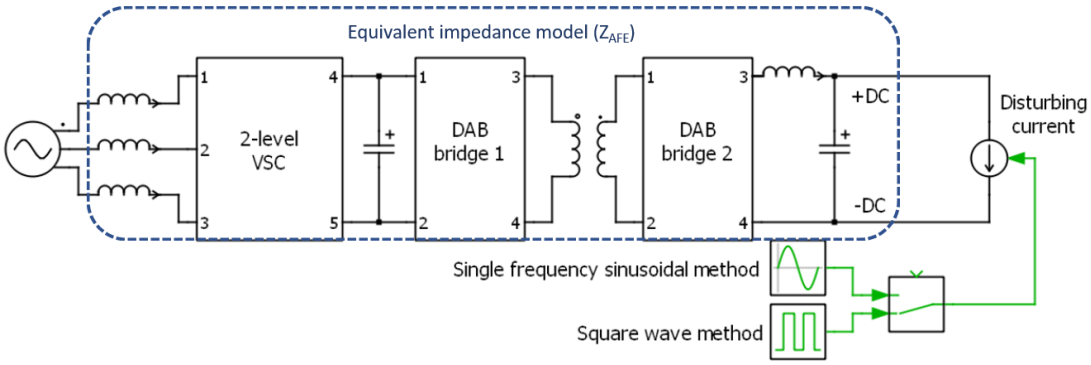


Figure 3.31 Current injection methods for frequency-dependent impedance identification

This way squared waves can be used for a rough determination of the impedance model, while the sinusoidal method can be employed for precise frequency ranges, in order to evaluate specific phenomena or to validate the impedance value found at a certain frequency. A last aspect to be considered is that, in parallel to dependence of frequency, the impedance model is also dependent on the operation point of the converter. Thus, it is important to define precise validity limits for the impedance model. One option is to consider the power as a parameter, and to define steps related to its nominal power as an operation limit for each impedance model.

3.6.2.3. Disturbance propagation studies

Different strategies exist to study the propagation and intensity of disturbances in distribution systems. Since experimental measurements are not always simple to perform, accurate simulation models seem to be the best suited answer to estimate PQ indicators in different scenarios. Several types of simulation exist though, and it is important to define which ones are the best adapted to this work.

Electromagnetic transient (EMT) time domain simulation allows the observation of precise current/voltage waves over time, transitory behavior, and control actions. On its turn, frequency-domain simulation can represent the steady-state behavior of a distribution grid in terms of spectral components with far smaller calculation time, when compared to time domain simulation. Consequently, it becomes evident that EMT time-domain simulation is well-suited for the evaluation of transient PQ phenomena, while frequency-domain simulation seems to be the best choice for steady-state PQ analysis.

In this perspective, characterizing the behavior of the IC by frequency-dependent impedance models allows the complete representation of a distribution grid in the frequency-domain. The voltage delivered by the IC can be represented as a frequency-dependent voltage source and disturbances coming from feeders can be represented by frequency-dependent current sources. This complete simulation

model permits the analysis of the impact of different levels of disturbances in the DC voltage, which will certainly be useful in the future, to determine EMC levels for DC distribution systems.

3.7. Conclusion

The third chapter of this work discussed in detail the multiple choices made to conduct the analysis of DC distribution systems, with a focus on the modelling of power electronics, selective protection schemes and the influence of the IC in PQ indicators.

The complete modelling of the proposed architecture of distribution grid served as the basis for the design of a method of conceiving a selective protection scheme based on current limitation techniques, fuses and TMCBs. For the concept of distribution grid explored in this work, it looks to be a reasonable choice. It avoids huge oversizing of the IC, and it employs classic protection devices, which are standardized and are not as expensive as other solutions such as SSCBs. The method presented here was used for a specific scenario, where different equipment was defined according to certain features. However, it should be possible to apply the same reasoning for other cases, where the voltage source converters are capable of limiting short-circuit currents.

In terms of PQ indicators, it becomes evident that the IC plays a major role in the propagation of spectral disturbances, as well as in the repercussion of transient phenomena. This chapter showed exhaustively which features of the IC may be considered to control and mitigate these phenomena. It is also possible to identify the need for future standards to impose certain characteristics for voltage-source converters, such as the response time and the frequency-dependent impedance according to the operation ranges.

In the next chapter, most part of the modelling approaches presented here will be used in practice, either and simulation and in the experimental prototype, to validate the protection scheme proposed in this chapter, together with the PQ assessment methods.

Chapter 4. SIMULATION AND EXPERIMENTAL RESULTS

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4.1. Introduction

This last chapter presents the results obtained through the different methods discussed in Chapter 3. The conception of a last version of the simulation model is presented, in addition to the steps followed for the implementation of the front-end converter prototype. Both the simulation model and the experimental prototype are used to confirm certain hypothesis made before, and they serve as a base for the design of the proposed protection plan and the power quality analysis.

Section 4.2 will bring details on the modelling of the bidirectional IC theorized in Chapter 3 with a particular focus on the operation of the input 2-level VSC. Section 4.3 shows what are the materials used to build the AC/DC converter and how to obtain a correct operation of this converter, based on the characteristics of its components. Considering all the elements used in 4.3 for the experimental prototype, section 4.4 describes how the simulation model is adapted to match, as much as possible, the characteristics of the real converter. Here, the control system's performance is analyzed, along with the thermal models of power switches. In section 4.5, the methodology presented in Chapter 3 for the design of selective protection schemes in LVDC is employed in practice with TMCBs and fuses. Finally, section 4.6 explains the behavior of the converter submitted to transient disturbances, along with the application of the method of frequency-dependent impedance identification of the AC/DC converter.

4.2. The bidirectional IC simulation model

A first simulation model was designed in this work, representing a bidirectional grid with the adapted IC. The main topology was already introduced in Chapter 3 and is composed by a 2-level VSC and a modified DAB. This section will present further details on the operation of this architecture, starting by the design of filters, following the equations, discussed in Chapter 3 as well. The complete topology can be seen in Figure 4.1. The first step here will be the design and analysis of the 2-level VSC.

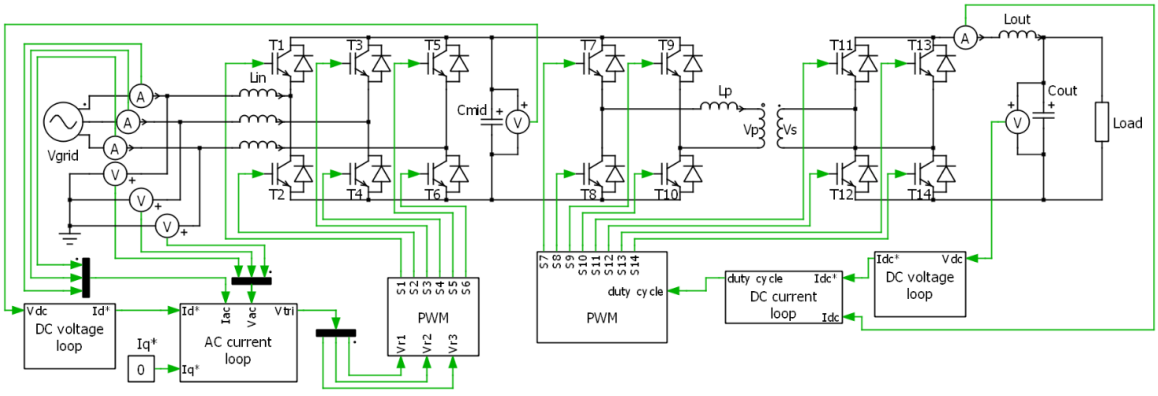

Figure 4.1 Complete Bidirectional IC topology

There are multiple possibilities concerning the AC voltage, which are related to standard low voltage levels. In this work, a classic level of 400V RMS (V_{grid} in Figure 4.1) is chosen. It is used recurrently for LVAC distribution systems around the world, and particularly in France. The voltage in the intermediary DC bus must be greater than the peak AC voltage for the 2-level VSC's control system to operate, but it must not be too high, otherwise the power switches in the DAB must need to withstand high blocking voltage levels. For this reason, an intermediary voltage in the capacitive bus (C_{mid} in Figure 4.1) of around 650V can be adopted. Regarding the output voltage level, Chapter 2 already demonstrated

the advantages of using values around 350V for the DC distribution system, which is the voltage used in this work as well.

In terms of power, the operation point chosen for these simulations is around 3.8kW, which should be close to the desired power of the prototype. This power corresponds to a 5.6A line RMS current in the AC side of the distribution grid.

4.2.1. 2-level VSC input and output filters

According to equation (3.4) and for an operation point found in simulation with the characteristics shown in Table 4.1, the value of L can be calculated. It results in the subsequent inequality: $L \geq 19\text{mH}$. In this case, the value of 20mH for the reactors in the AC side is chosen.

Table 4.1 Operation point for input inductive filter sizing

V_{DC}	I_F	$THD_{I\text{-}MAX}$	T_{SW}	M
680V	5.6A	5%	0.1ms	0.95

Using equation (3.5), for the following operation point in Table 4.2, it is possible to find that the capacitance must be greater than 500µF. To ensure a high-level filtering of the output voltage a 600µF capacitor is chosen.

Table 4.2 Operation point for output capacitive filter

V_{DC}	I_F	$I_{AC\text{-}PEAK}$	f_{SW}	ΔV_{MAX}
680V	5.6A	8A	10kHz	0.2V

4.2.2. 2-level VSC control system

An operation point corresponding to an output voltage and current of $680V_{DC}$ and $10A_{AC}$, respectively, is chosen to test the control system. The result of a 170V (25% of the nominal voltage) step is a 5%-time response of 15ms and an overshoot of around 20%. From Figure 4.2, it is possible to see that the Feedforward technique, described in Chapter 3 above, improves the dynamic behavior of the control system reducing the overshoot from 45% to 20%, with very little impact in the time response. It significantly reduces the current transient as well, from a maximum peak of 60A to 42A. The set of parameters employed in the control system are shown in the Table 4.3.

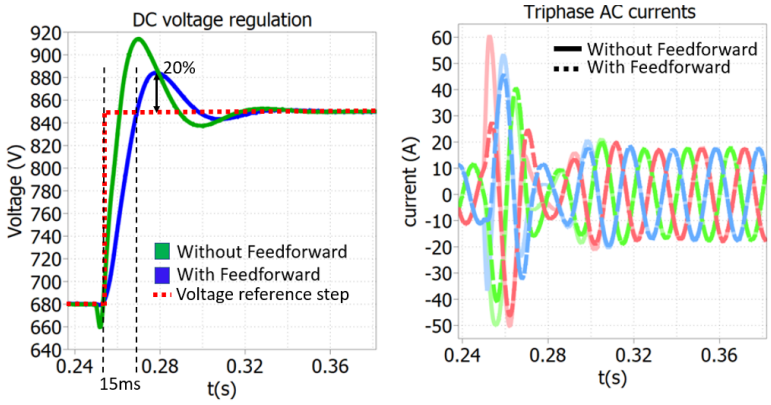

Figure 4.2 The 2-level VSC control performance

Table 4.3 The 2-level VSC control parameters

Inner loop				Outer loop	
Direct current regulation		Quadrature current regulation			
Ki	Kp	Ki	Kp	Ki	Kp
14400	17	14400	17	0.015	0.0001

4.2.3. Confirmation of design rules

In addition to the dynamic performance ensured by the control system, it is also important to verify if the design rules applied to choose the input and output filters are respected.

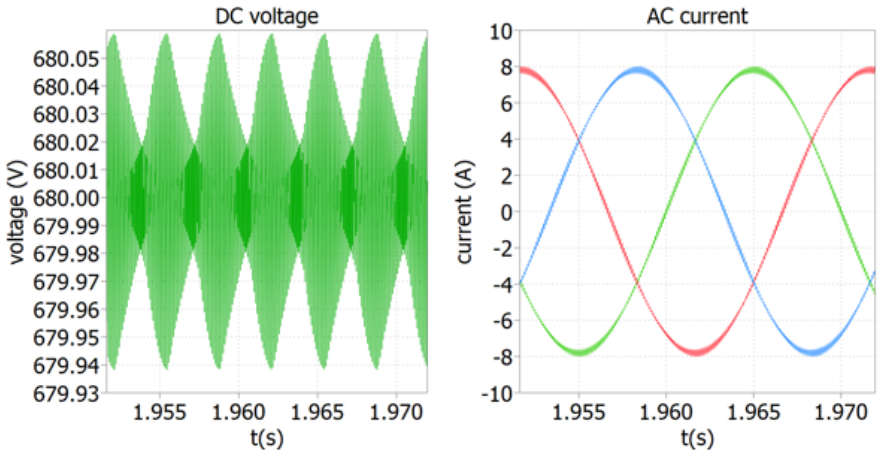

Figure 4.3 DC voltage and AC currents for the defined operation point

While the inductors in the input of the 2-level VSC may limit the current THD to 5%, the output capacitor must limit the peak-to-peak voltage variation to 0.2V. Results can be observed in Figure 4.3, and PLECS calculations show a current THD of around 2.1% and a maximum voltage variation during a switching period of around 0.15V, which confirms that the designing rules are respected.

4.2.4. Overall analysis and changes in the modelling strategy

From the results presented by the sections above, it can be seen that for the design methods presented in Chapter 3, the 2-level VSC behaves like expected. Consequently, this simulation model could be used in the digital representation of a bidirectional LVDC distribution system.

Nonetheless, from the point of view of research interest, this work is not focused on studying the bidirectionality of the proposed distribution grid. In addition, it will still take some time until distribution system operators (DSOs) become capable of managing DC metering and power flow import from private DC distribution grids. In this perspective, it seems pertinent to conceive a simpler AC/DC conversion topology, which would be easier to reproduce in a prototype, but would still permit protection and power quality analysis for DC distribution grids.

4.3. Prototype design of unidirectional AC/DC converter

This section presents an alternative unidirectional topology, still based on the design methods presented in Chapter 3, specially for the last conversion stages. Figure 4.4 illustrates the new AC/DC converter model.

The final objective of this simulation modelling strategy is to try to get as close as possible as the real experimental prototype. Consequently, the choice of the parameters related to the control laws and filters will be made in parallel with the implementation of the prototype.

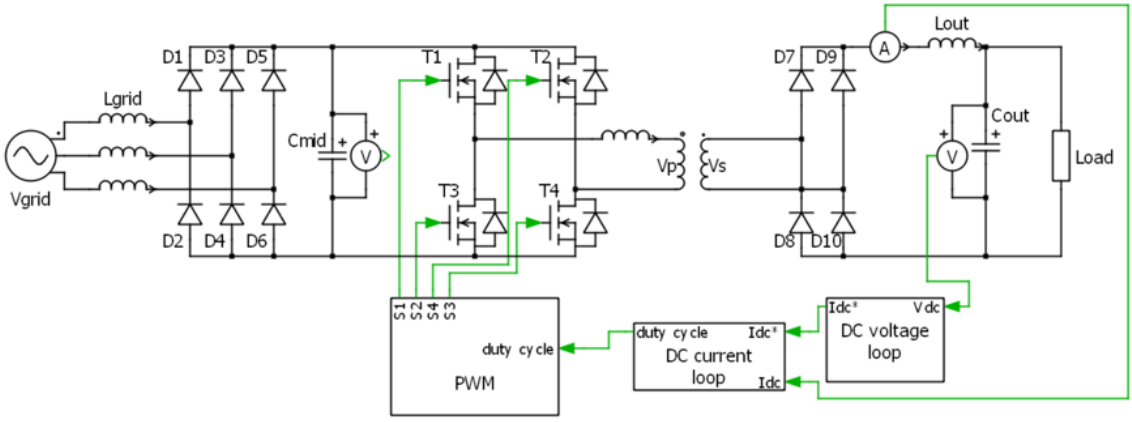

Figure 4.4 AC/DC converter used to deploy the DC distribution grid proposed by this work

4.3.1. Main design considerations related to the unidirectional AC/DC converter

In this topology, the input converter is a simple three-phase full-wave diode-based rectifier. This means that some changes may be needed in the sizing of the filters, which may impact the converter's behavior. The most important changes are listed below:

a. Input inductive filters are no longer needed. In this simulation, an arbitrary value of L_{grid}=200µH is used to estimate the upstream grid inductance.
b. The intermediary capacitive bus will certainly need to be recalculated, since low-frequency disturbances, such as 6th, 12th and 18th voltage harmonics, are produced by the passive rectifier.
c. The DAB will permanently operate like the SAB, which means that only one bridge is to be controlled. The control and filter design methods for this conversion step remains the same as the ones presented in Chapter 3.Chapter 3.
d. Low-frequency current harmonics will be injected in the AC grid (5th, 7th, 11th, 13th). This aspect should be analyzed carefully. However, it is not in the scope of this work, which is focused on disturbances in the DC side.
e. Transient phenomena are also impacted by the modification in the AC/DC converter, since in this new topology, there is no active voltage regulation of the intermediary DC bus.

Next sections will present the details around the choice of the passive components in parallel with the real implementation of the prototype. This parallel work is interesting from a research point of view, since the simulation models are the base for the choice of components integrating the prototype. On its turn, through the progressive implementation of the prototype, it is possible to enrich the simulation models with more realistic characteristics of each component.

4.3.2. Filters and passive components

Through the strategies defined in Chapter 3, it is possible to determine the characteristics of the passive components and filters used in the AC/DC converter topology.

4.3.2.1. Intermediary capacitor

To compensate from the absence of an intermediary voltage regulation and to avoid high-level low-frequency disturbances in the final DC voltage, a capacitive bus of 1200µF is chosen (C_{mid} in Figure 4.4). It is twice the value of the one calculated for the 2-level VSC. As already evoked, film capacitors are to be privileged for this type of application. In practice, two 600µF 900V KEMET C44U capacitors [**KEM19**] are associated in parallel. They have an ESR of 2.2mΩ and an ESL of 40nH.

4.3.2.2. Output inductor

To define the inductance, the material and number of turns for the output inductor, it is necessary to define an operation point. A 3.5kW operation is chosen, which corresponds to 10A circulating in the DC distribution grid. The objective here is to remain representative of a real scale scenario while remaining in a power level that could be managed in a laboratory context. From equation (3.21), and for the following operation point (Table 4.4) found in simulation, it is possible to obtain the inequality $L \geq 483\mu H$.

Table 4.4 Operation point for output inductor sizing of DC/DC isolated converter

V_{Cmid}	V_{DC}	α	ΔI_{MAX}	I_{DC}
565V	350V	36%	4A	10A

From this operation point, it is possible to calculate the energy that must be stored in the inductor and determine the number of turns necessary in the winding, through data provided by manufacturers. For the energy stored in the inductor requested by the chosen operation point (around 25000µJ for a DC current of 10A) and using a E220-40/G020 from Micrometals [**MIC07**], it is possible to estimate the number of turns to 50.

The inductor's winding is made with copper wires of 1.5mm² diameter (AWG16). According to the manual fabrication of the inductor, a RLC meter is used to confirm the inductance value and series resistance in the switching frequency of the SAB (40kHz). Results are an inductance L_{out} (Figure 4.4) of 443µH with a series resistance R_{Lout} of 600mΩ.

4.3.2.3. Output capacitors

For the calculation of the output capacitor C_{out} (Figure 4.4), the cut-off frequency equation was used to allow a 3dB attenuation at 500Hz, which results in an output capacitor of 228µF. For the purpose of further real implementation, a 220µF electrolytic TDK capacitor (C_{out1}) is chosen [**TDK19**]. This capacitor has an ESL of 20nH and an ESR that can be estimated as 250mΩ at 10kHz.

It is possible to observe that the ESR of this first capacitor is high. For this reason, another capacitor with lower ESR is used here as well to mitigate the propagation of conducted high-frequency disturbances due to commutation related phenomena. A lower ESR means that the equivalent impedance of the capacitor remains smaller for higher frequencies, improving its filtering band. A 2.2µF TDK film capacitor (C_{out2}) is used for this purpose [**TDK20**], in parallel with the first capacitor. It offers an ESL of 25nH and a ESR of 8mΩ at 10kHz.

4.3.2.4. Medium-frequency transformer

The magnetic core is chosen to be a Ferrite N87 with a double E shape [**TDK13**]. For this core geometry, it is possible to execute the calculation of the number of turns to avoid core saturation, using equation (3.27). With the following characteristics (Table 4.5) of the magnetic core, and operation point, the primary winding must have at least 25 turns.

Table 4.5 Values considered for the medium-frequency transformer sizing

E_{MAX}	f_{SW}	A	B_{MAX}
1000V	40kHz	10.9cm²	2500gauss

The real implementation of the transformer is made with a primary winding of 30 turns and a double secondary side with 15 turns in each winding. The objective here is to allow a certain level of flexibility for experimental tests in reduced voltage (1:0.5 ratio) or un full voltage (1:1 ratio). In addition, to avoid a high impedance in the windings at 40kHz, the coils are made with Litz-wire with 46 0.1mm² copper strands.

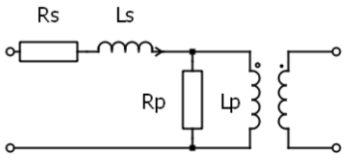

Figure 4.5 Medium-frequency transformer simulation model

The medium-frequency transformer is submitted to short-circuit and open-circuit tests with the RLC meter with the objective of finding an equivalent circuit which can be used in simulation. A classic equivalent model is considered here, which can be seen in Figure 4.5. Short-circuit tests can be employed to estimate R_s and L_s components of the model, while R_p and L_p can be found using open circuit test. In practice, L_p represents the magnetization inductance of the transformer, L_s the leakage inductance, R_s the power losses in the windings, and R_p the losses in the magnetic core. Those parameters are summarized in Table 4.6.

Table 4.6 Medium-frequency transformer measured parameters

R_s	L_s	R_p	L_p
340mΩ	28µH	750kΩ	12.8mH

4.3.3. Power switches

Since the analysis carried out in this work is much more focused on the DC side of the AC/DC converter, a higher importance is given to the choice of the power switches from the SAB. It can also be justified by the fact that they are the ones who impact the DC grid the most and are also impacted the most by phenomena in the distribution grid.

From this perspective, a three-phase full-wave silicon diode-based rectifier is implemented in the input of the AC/DC converter. A 35A module from HY Electronics is chosen [**HYE14**] along with a heat-sink, which is not studied in detail.

For the active bridge of the SAB, the best option seems to be the use of SiC MOSFETs, profiting from their high maximum junction temperature, fast switching and reduced on-state resistance. Thus, a TO-247-3, 900V, 36A, SiC MOSFET from CREE is selected [**CRE21**].

The same semiconductor technology is considered for the diodes of the passive bridge in the SAB. In this case, CREE 650V, 28A (at a case temperature of 135°C), TO-247-3 SiC diodes are chosen [**CRE14**]. The particularity here is that they have essentially no switching losses and that in the case, there are two SiC diodes in parallel connected by the middle pin.

4.3.4. Driver of SiC MOSFETs

SiC MOSFETs usually need high gate-to-source voltage to switch (up to 20V) with high slew rate voltage, since switching frequency may be elevated. For this reason, specific drivers must be chosen. For this work, MAX22701E gate drivers from Maxim Integrated were selected. They provide integrated functions such as Miller Clamp diodes and Undervoltage Lockout, to protect the MOSFETs from glitches and voltage supply malfunctions. In addition, an active low-input is also used to prevent false commutation orders and short-circuit in one commutation cell. From the datasheet [**MAX21**], it is possible to identify the connection of the drivers with the SiC MOSFETs along with the necessary capacitive filters. In the design presented by this work, a resistor of 10Ω is used as gate resistor, and 15V isolated voltage supplies are employed to control the MOSFETs.

4.3.5. Computational device

The best option for the application studied in this work seems to be a DSP. Consequently, a DSP from Microchip of the dsPIC33CK256MP508 family is used [**MIC22**]. It was chosen because of 4 crucial characteristics:

- Presence of MCU (Microcontroller Unit) with hardware multiplier.
- High-speed PWM including multiple features and simple dead-time configurations.
- Two dedicated 12-bit ADC cores.
- Simple programming interface.

The presence of an MCU with hardware multiplier is important so that all the calculations can be done inside a commutation period, with the objective of actualizing the duty-cycle value once per period. This is particularly important for the current limitation technique, where the control system must react as fast as possible to limit short-circuit current. In practice, for a switching frequency of 40kHz, all the calculations must be done at maximum time of 25µs. On its turn, the double ADC core allows the acquisition of voltage and current measurements in parallel, which accelerates the start of the control loops calculations.

Some of these functions were implemented in the PLECS' simulation interface, following the methodology defined in Chapter 3 for the control system. The recurrence control laws can be implemented using Update functions on C-script blocs, which ensure the actualization of duty-cycle once per switching period. All the gains associated with other stages, which are presented next, will be taken into consideration in the simulation model as well.

4.3.6. Voltage and current measurements

For the operation of the double cascade control loops, the output current and voltage must be measured. Those measurements are made by means of two sensors which must deliver a low voltage output signal to the computational engine responsible for control calculations.

4.3.6.1. DC Voltage sensor

The simplest and less expansive way of performing a voltage measurement is using a resistive voltage divider. It must be sized to respect the voltage limits accepted by the ADCs of the computational engine, and to respect the power dissipation of the resistors included in the divider. Without an external voltage supply, the voltage limit of the ADC core corresponds to the voltage supply of the DSP, which in this case is 3.3V. Nonetheless, there is no galvanic isolation, which means the ground reference must be the same between the voltage divider and the DSP. Considering also a maximum voltage of 600V in the DC distribution system and leaving a margin of 10% in the maximum ADC voltage, the calculation for the voltage divider is given by equation (4.1).

$$\frac{V_{max-ADC}}{V_{max-DCgrid}} = \frac{R2}{R1+R2} \tag{4.1}$$

It is possible to choose *R2* as a 4.7kΩ and *R1* as two 470kΩ in series. From *R1* and *R2*, and neglecting the current absorbed by the ADC, it is possible to determine the maximum power dissipated in the resistors. The calculation is as follows in equation (4.2). To leave a certain margin, resistors of 1W are chosen. In addition, a 200nF capacitor (C_{f1}) is connected in parallel to *R2* to limit the influence of noise and high-frequency disturbances in the voltage measurement. The cut-off frequency of the measuring circuit can be estimated as 170Hz, according to equation (4.3).

$$P_{R1-R2} = \frac{V_{max-DCgrid}{}^2}{(R1+R2)} = 0.381W \tag{4.2}$$

$$f_c = \frac{1}{2\pi C\left(\frac{R1R2}{R1+R2}\right)} \tag{4.3}$$

Considering the 12-bit ADC, it means that the resolution of the voltage measuring system, in terms of DC grid voltage, is close 0.15V. It seems to be enough since 0.15V represent 0.042% of the nominal voltage (350V).

4.3.6.2. DC Current sensor

To perform the measurement of current in the output of the AC/DC converter, a Hall Effect sensor is chosen. The magnetic field generated by the current passing thru the sensor creates a Hall voltage, which is used to determine the current level. In our application, the 50A ACS758-050U from Allegro Microsystems is used [**ALL22**]. It has 40mV/A with a 5V supply, which means a 26.6mV/A at 3.3V supply. In practice, a current measuring resolution of 30mA is achieved with this configuration, which seems to be enough, since the current regulation loop is not the external loop.

In the output of the sensor, manufacturers recommend the use of a low-pass RC filter. For this application, a resistor of 1kΩ (R_f) and a capacitor of 200nF (C_{f2}) where used, which results in a cut-off frequency of around 800Hz (4.4). The passband is wider for the current measurement system because current dynamic behavior is faster than the voltage one.

$$f_c = \frac{1}{2\pi RC} \tag{4.4}$$

4.3.6.3. Management of voltage and current acquisitions

Inside the DSP, the main executed program will be the one where the recurrence equations are defined. Inside a while loop, it is executed constantly. To optimize the complete operation of the system, additional functions should be run through a system of interruptions. This is the case of ADCs and the acquisition of voltage and current measurements. The implementation of this dynamics is shown in the diagram below (Figure 4.6).

The idea behind this operation is to execute a software filtering through the calculation of mean voltage and current values, in which 4 consecutive measurements are used. The main program waits for the correct calculation of these mean values to calculate the recurrence equations and to send the new duty-cycle value to the PWM unit.

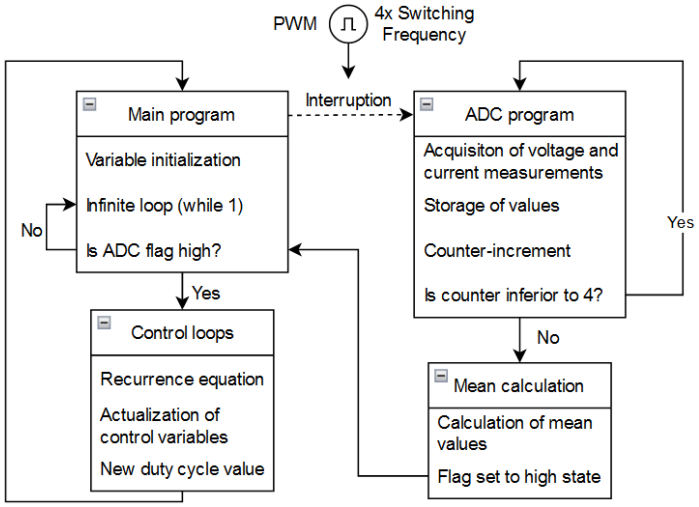

Figure 4.6 Diagram representing the operation of ADCs through interruptions

4.3.7. Prototype

Before demonstrating the implementation process of the converter prototype, it may be useful to recall the choices made in terms of technology and characteristics adopted for individual components. Table 4.7 summarizes it.

Table 4.7 Bill of materials for AC/DC converter prototype

Intermediary capacitor	Output inductor	Output capacitors	Input rectifier	Medium-frequency transformer
2x 600µF 900V KEMET C44U film capacitors	443µH E220-40/G020 Micrometals Iron-power magnetic core	220µF B43545 TDK electrolytic capacitor, and 2.2µF B32922P/Q film capacitor	HY Electronics SBR25/35A three-phase diode rectifier	TDK N87 Ferrite B66387 magnetic core and 46x 0.1mm² Litz wire
Active bridge	**Output rectifier**	**Drivers**	**Computational device**	**Voltage/current sensors**
CREE TO-247-3, 900V, 36A, SiC MOSFET C3M0021120D	CREE TO-247-3 650V, 28A SiC diodes C3D20065D	Maxim Integrated gate driver for SiC MOSFETs MAX22701E	Microchip DSP dsPIC33CK256MP508	470kΩ-4.7kΩ voltage divider and Allegro Hall-effect sensor ACS758-050U

The construction of the AC/DC converter prototype was executed in three subsequent steps. A proof of concept was made to operate at some hundred watts. Once the operation was validated, a first version of the prototype was conceived. Finally, some editions were made in the SAB in terms of electronic disposition and additional circuits to improve the EMC, such as the reduction of cable lengths, longer distance of control system and power switches and electronic board optimization. The scheme in which the conception of the prototype was based can be observed in Figure 4.7.

There are some low-level electronic components which are not shown in the scheme. For example, it is worth mentioning that high-power side of each driver is supplied thorough a 24V/15V isolated DC/DC converter, while the DSP, the control side of each driver and the current sensor are supplied through a 24V/3.3V isolated DC/DC converter. In addition, each one of the circuits dedicated to the control of MOSFETs includes its own set of capacitive filters associated. The numbers associated to each part of the different version of the prototype correspond to the components listed below, which are also shown in Figure 4.7:

1) Three-phase input coming from the autotransformer.

2) Three-phase full-wave silicon diode rectifier and heatsink.

3) 24V auxiliary voltage supply for multiple electronic components.

4) Intermediary capacitive bus with two 900V 600µF capacitors in parallel.

5) Active bridge of the SAB with SiC MOSFETs, drivers and auxiliary electronic components.

6) Snubber capacitors, which were the last integrated components of the AC/DC converter.

7) Medium-frequency transformer.

8) Passive bridge of the SAB with SiC diodes.

9) Output iron powder 443µF inductor.

10) Output capacitive bus, with two capacitors (220µF electrolytic and 2.2µF film).

11) Current and voltage sensors.

12) Adaptative interface between the DSP and the converter's electronic board.

13) Output DC voltage connectors.

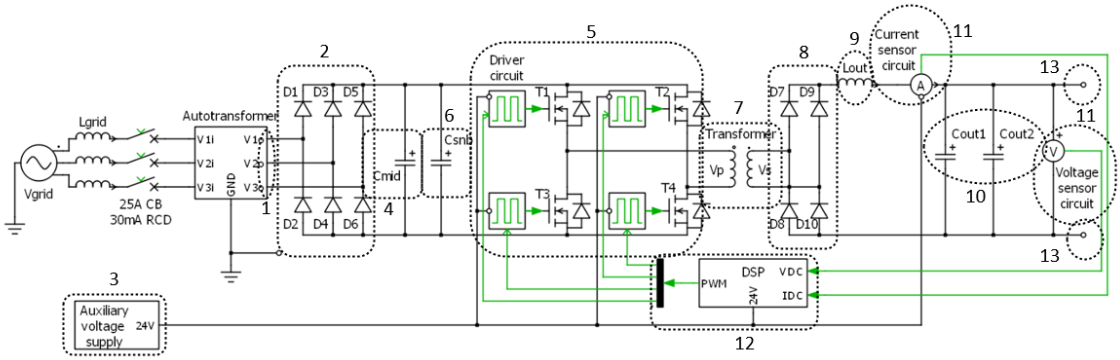

Figure 4.7 Illustrative scheme of the last version of the prototype

4.3.7.1. First prototype

The first version of the prototype was used to test the set of components together: SiC MSOFETs, drivers, filters, and medium-frequency transformer (Figure 4.8). The operation point with maximum power executed with this set up was 80V and 2A.

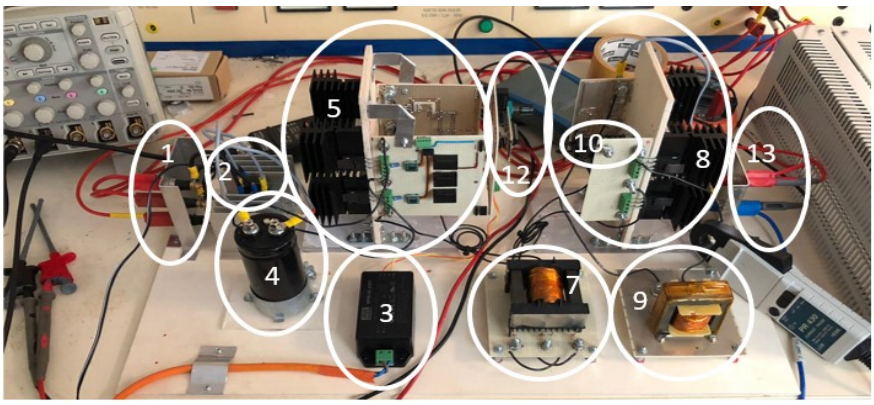

Figure 4.8 Proof of concept

Here it is possible to see that there were no snubber capacitors, the intermediary capacitor had a smaller capacitance (500µF) than the one calculated in 4.3.2.1, there was no high-frequency filter dedicated capacitor (C_{out2}) and, finally, that the transformer magnetic core where a smaller version of the one calculated in 4.3.2.4. Even if it does not correspond exactly to the envisaged converter, through a simple set up it was possible to validate the operation of the system.

4.3.7.2. Second prototype

For the first version (Figure 4.9), proper electronic boards were designed for the SAB, and the intermediary capacitor and the medium-frequency transformer were already designed following the rules presented previously in this chapter.

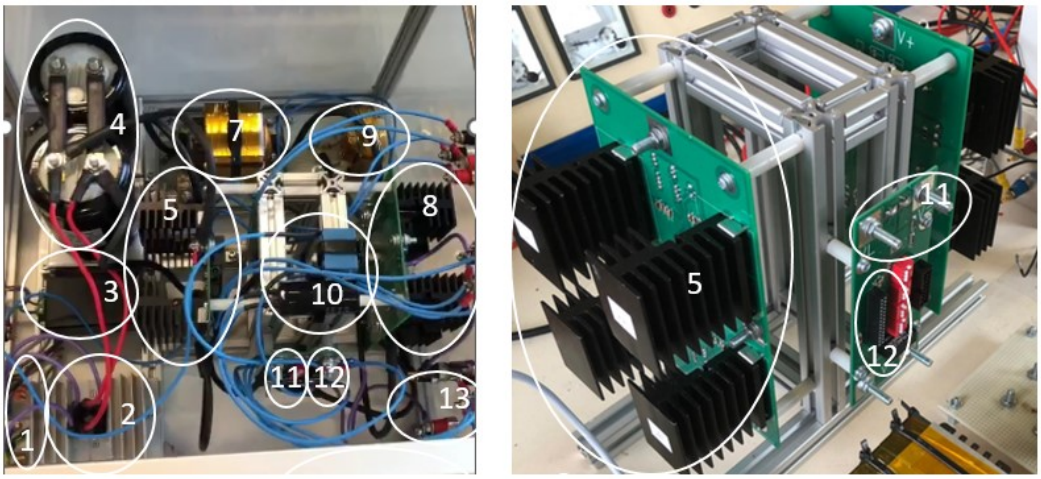

Figure 4.9 First version of the AC/DC converter prototype

The first measurements conducted with this converter prototype were done in open loop, connecting a resistive load, and using the autotransformer to variate the output DC voltage. The results showed that SiC MOSFETs commutation generated a considerable overvoltage, which could be measured in the primary side of the medium-frequency transformer. It can be observed in Figure 4.10.

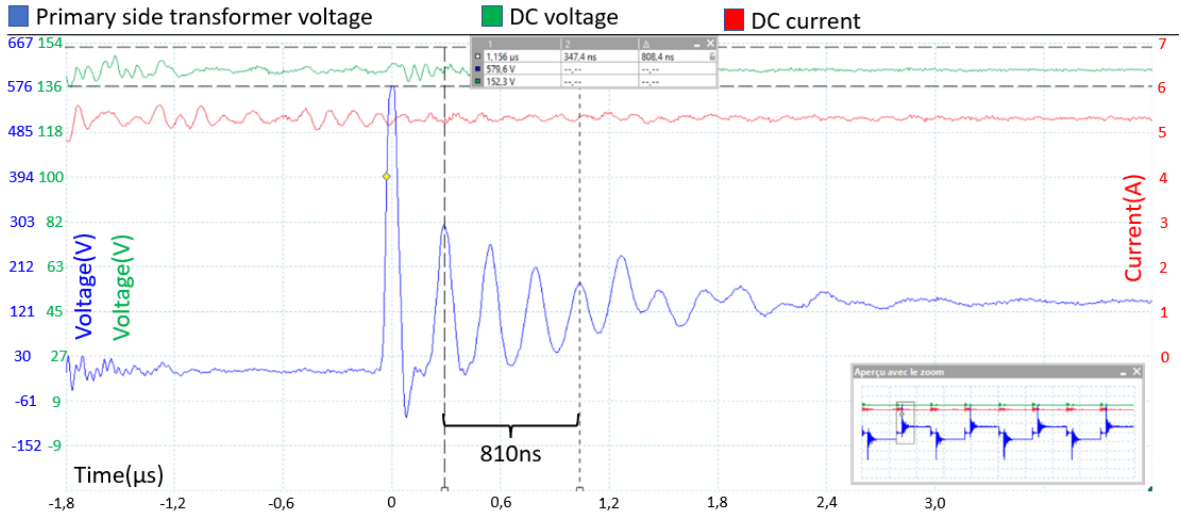

Figure 4.10 Medium frequency transformer primary side voltage (blue), DC current (red), and DC voltage (green)

It is possible to observe that the active bridge of the SAB feeds 40kHz squared voltage waves to the transformer, and the non-zero voltage interval is controlled by the duty-cycle imposed by the DSP to the driver of the MOSFETs. For an operation point of 150V in the DC bus and 5.5A, the overvoltage peak reached almost 580V. This level of overvoltage is not acceptable for higher output DC voltages,

because a risk of destroying the SiC MSOFETs exists. Moreover, it is possible to see that the voltage transitory behavior impacts voltage and current at the DC side, introducing high-frequency disturbances. One possible solution is to insert a snubber circuit, capable of delivering the necessary energy for stray and parasitic inductance during commutation, thus reducing the overvoltage.

The choice of not using this kind of overvoltage mitigating circuit in the first prototype from the beginning is because there is always a trade-off associated to the use of snubbers. Since they are often composed by capacitors, resistors and even diodes, the system reliability level is lowered. In addition, capacitors aging may cause disfunctions in the circuit operation and not expected overvoltage levels may put power switches in danger. Nevertheless, for many applications, snubbers are necessary to limit normal operation overvoltage created by power switches commutation. Using equations 3.25 and 3.26, it is possible to calculate the minimum value of capacitance in the snubber circuit to limit the overvoltage. From equation (3.29) in section 3.6.2.1 and from the datasheet of SiC MOSFETs, the values presented in Table 4.8 can be considered for the design of the snubber capacitor.

Table 4.8 Values used to design the snubber capacitor

f_{surge}	C_{oss}	V_{surge}	V_{DC}	I_m
3.7MHz	180pF	575V	150V	5.5A

From these values and based on Figure 3.29, L_s is estimated at around 10µH and the snubber capacitor must offer a capacitance of at least 1nF. To take the phenomenon of capacitance reduction with frequency increase due to parasitic inductance, two 22nF polypropylene film capacitors were used in parallel. Using the RLC meter at 1MHz, the association of snubber capacitors where at a 28nF capacitance, which should be enough to reduce the overvoltage in the SiC MOSFETs during commutation.

4.3.7.3. Third prototype

The set of equipment used during the experimental tests for the purpose of studying LVDC grids is shown in Figure 4.11., and a more detailed figure on the AC/DC converter is presented in Figure 4.11.

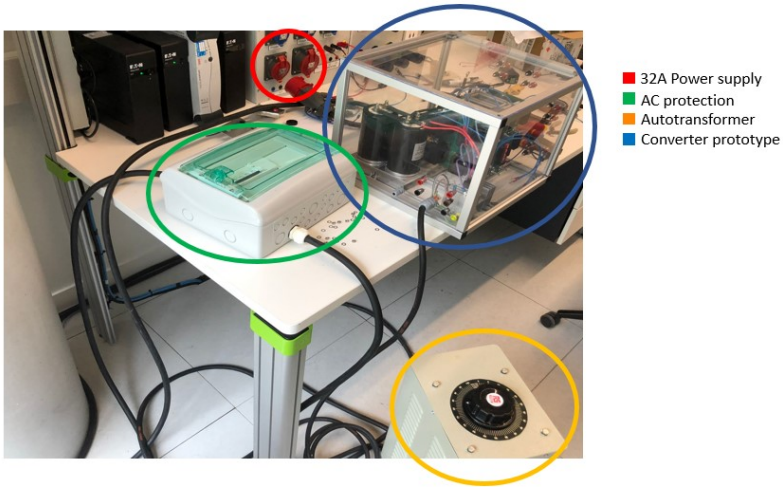

Figure 4.11 Laboratory testbed

In this set up, as it can be seen in Figure 4.12, another electronic board is designed (Annex B. Electronic board design models for the third version of prototype). This time, the active bridge, the passive bridge, and the controller are all put on the same board. The objective is to optimize the disposition of components to reduce EMI effects, guarding certain distances and avoiding cable connections between the control circuit and the power switches.

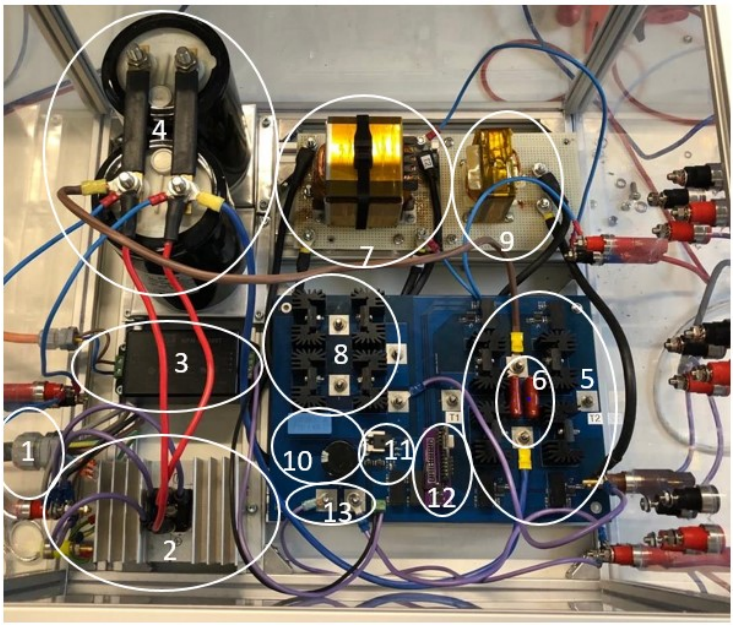

Figure 4.12 AC/DC converter prototype

To test the behavior of the final AC/DC converter prototype, an operation point of 230VDC and 8A is reached in open loop, using a resistive load bank. A smaller power level than the rated design power is used to avoid destruction of converter prototype. The result is shown in Figure 4.13. It is possible to see that the optimization of the disposition of components in the electronic board, along with the presence of snubber capacitors, allow a considerable reduction of the overvoltage level in the SiC MOSFETs due to commutation.

Conversely, it is possible to see that an 810kHz weakly amortized voltage undulation is created. It happens probably due to the resonance between the snubber capacitors and the parasitic inductances from power switches and traces in the electronic board. A possibility to avoid this kind of phenomenon is to associate a resistor in series with the snubber capacitors. This solution is not explored here since it represents another source of energy dissipation and the voltage fluctuations do not seem to be dangerous. In fact, these fluctuations are not destructive for the converter and for the grid because they are not instable and divergent.

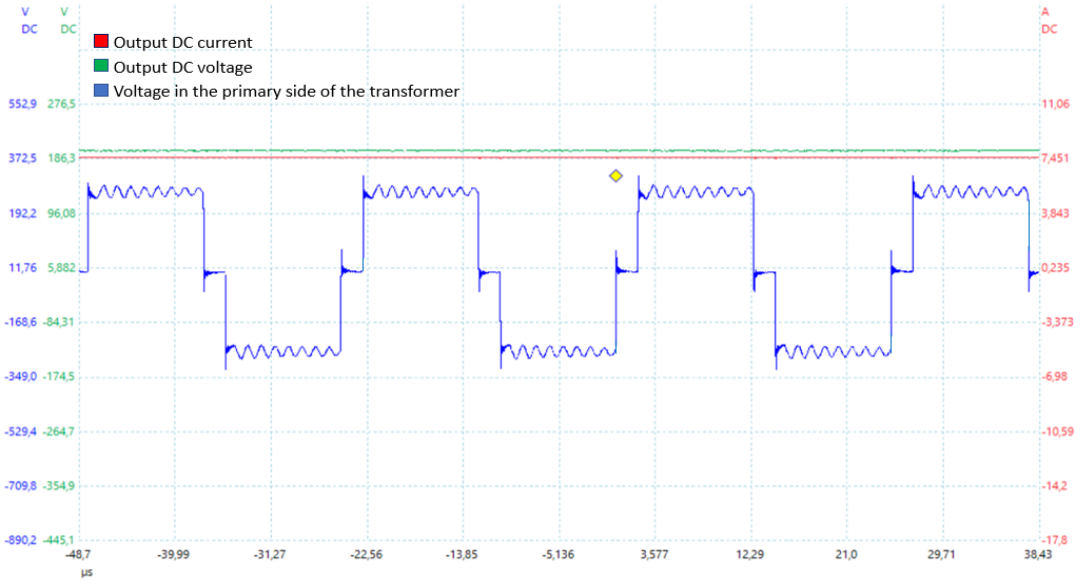

Figure 4.13 AC/DC prototype voltage/current waves in an operation point of 230V-8A

4.4. Final simulation model

Several components used in the prototype are then modelled in PLECS simulation platform. A relatively detailed simulation model will allow the observation of reliable electro-magnetic transients for the following PQ and protection analysis. Figure 4.14 illustrates the simulation model and its subsystems. In red it is possible to see the power electronics model, in green the modulation system, in blue the control one, and in orange current and voltage sensors.

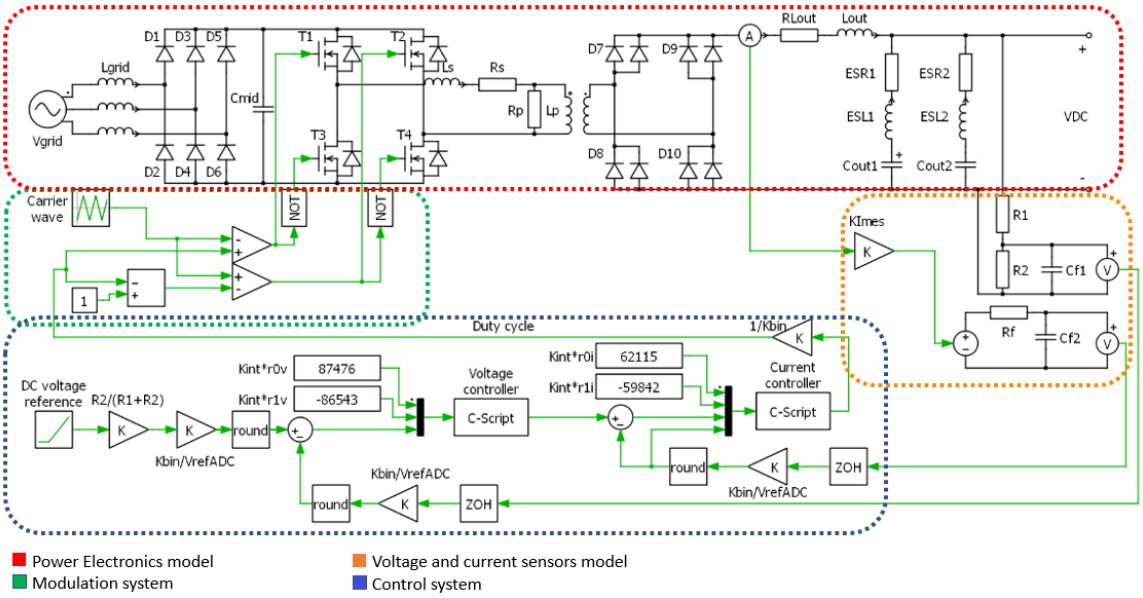

Figure 4.14 Complete final simulation model

The modelling of commutation phenomena, such as transitory overvoltage, involves the identification of parasitic stray inductances, structural capacitive effects in the MOSFETs, and gate excitation behavior. This low-level modelling is not the final objective of this work, which means that these phenomena are not studied in detail in simulation. From this perspective, snubber capacitors and their effect are not taken into consideration in the simulation model, which allows a considerable reduction in simulation time.

4.4.1. Control system

The methodology presented in Chapter 3 is applied here to design the control system of the AC/DC converter showed in section 3.3.2.1. In this context, different gains associated to voltage and current measurements, to the ADC resolution and voltage supply, are taken into consideration and shown in Table 4.9.

Table 4.9 Parameters for the control system implemented in simulation

V_{refADC}	K_{bin}	f_{samp}	K_{Imes}	K_{Vmes}	K_{int}
3.3V	4095	40kHz	0.026V/A	0.005V/V	10^5

For the parameters presented above, it is then possible to deduce the values of r_0 and r_1 from the classic proportional K_P and integral K_I gains of the continuous PI controllers. The values used are shown in Table 4.10, and are calculated from equations (3.9), (3.11), and (3.12).

Table 4.10 Parameters of the PI controllers

Current Loop				Voltage Loop			
K_P	K_I	r_0	r_1	K_P	K_I	r_0	r_1
50	50000	0.62115	-0.59842	7	1200	0.87196	-0.86823

With the objective of testing the performance of the control system, a 245-350V step was used in the DC voltage reference, which represents a voltage variation of 30% in relation to the final operation point. The result can be observed in Figure 4.15 (left) showing a 95%-time response of 7ms and essentially no overshoot in the DC voltage. The DC current in the output inductor in Figure 4.15 (right) has a faster dynamic behavior, which will be necessary to quickly limit short-circuit currents. The current overshoot seems to be acceptable since the current takes only 500µs to decrease to a mean level of 12A.

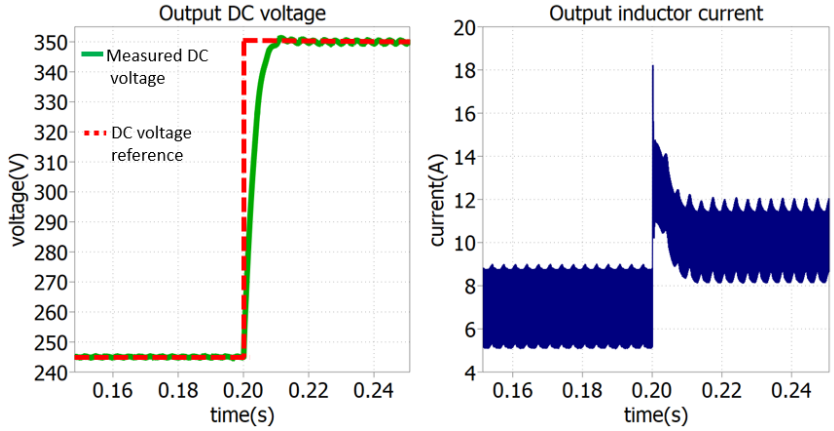

Figure 4.15 Simulated control system performance

Soft-switching of SiC MOSFETs can also be achieved with the SAB. Through the simulation model implemented in this work, it is possible to observe a zone of ZVS, which is shown in Figure 4.16. However, a more detailed model of the power switches is necessary to determine a reliable range of operation in which the converter can execute ZVS. The operation point fixed in Figure 4.16 is the same as the one used to test the control performance (350V and 10A).

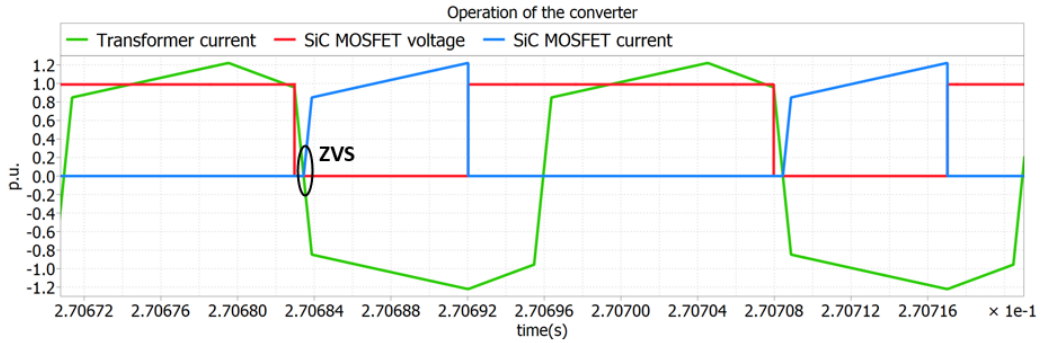

Figure 4.16 ZVS in the SAB - simulation results

4.4.2. Thermal modelling

Considering the power switches used in the prototype, as well as the operation of the SAB, the weaker components in terms of thermal endurance are the SiC diodes of the rectifier. They are directly polarized in the case of a fault and the entire fault current passes through them. In that scenario, since a

protection analysis is carried out in this work, it seems important to find a way of representing the thermal behavior of these diodes in simulation. The simulation model with the thermal circuit can be observed in Figure 4.17.

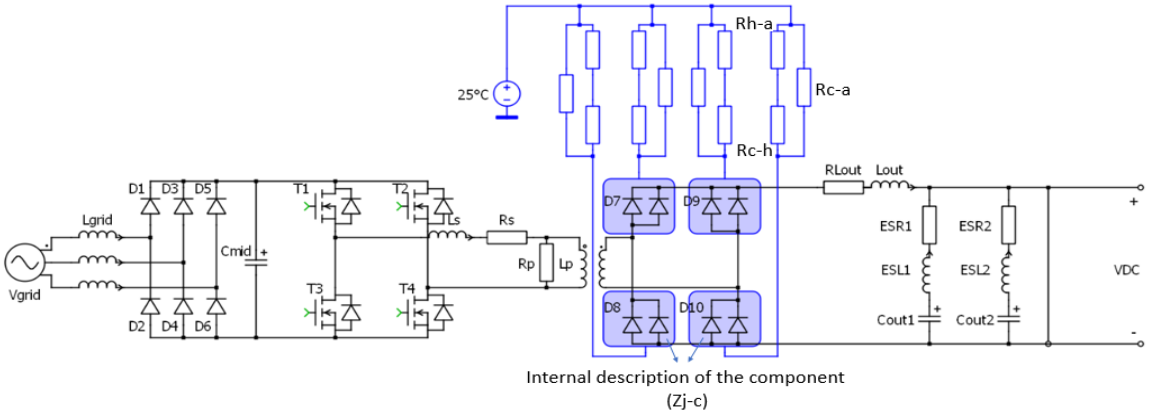

Figure 4.17 Thermal modelling of SiC diodes

In Figure 4.17, four thermal resistances represent the interfaces between components from the point of view of the heat flow:

- $Z_{j\text{-}c}$ - thermal resistance between the diode junction and the diode case.
- $R_{c\text{-}h}$ - thermal resistance between the diode case and the heat-sink.
- $R_{h\text{-}a}$ - thermal resistance between the heat-sink and the air.
- $R_{c\text{-}a}$ - thermal resistance between the diode case and the air.

The transient impedance between junction and case $Z_{j\text{-}c}$ is not directly represented in Figure 4.17 because it is given as an input of the internal characteristic of each diode. It is provided in the datasheet of SiC diodes and PLECS uses an approximation through RC Cauer networks from points defined by the user in the transient impedance curve, as shown in Figure 4.18. $R_{c\text{-}h}$ is estimated at 0.5°C/W, based on measurements made by Onsemi [**ONS22**] with TO247 SiC MOSFET cases and thermal grease between the MOSFETS and the heat-sink. On its turn, the value of $R_{h\text{-}a}$ can be found in the datasheet of the heat-sinks used in the prototype [**AAV15**], which is 5.6°C/W. Finally, the value of $R_{c\text{-}a}$ is 40°C/W, which is provided by the datasheet of the SiC diodes [**CRE14**].

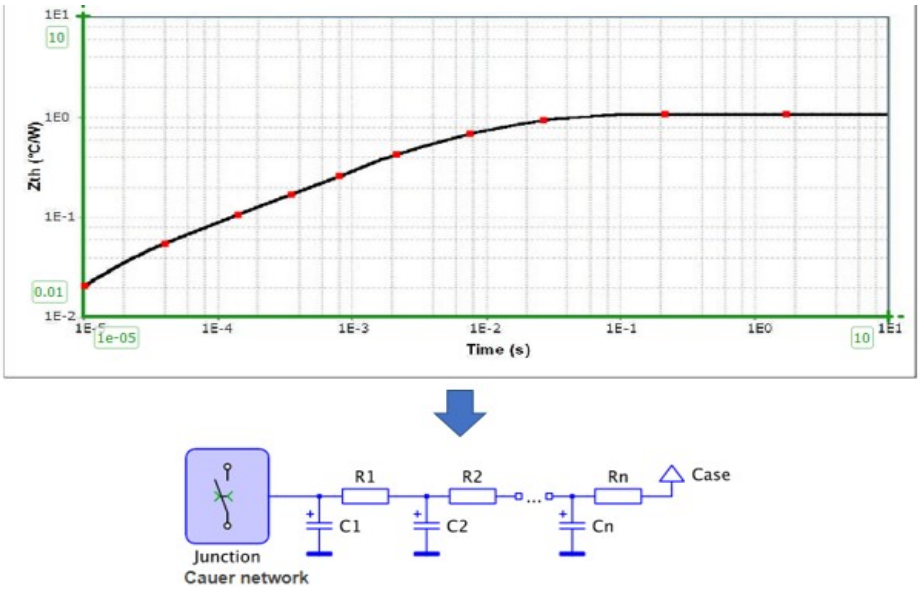

Figure 4.18 Transient impedance model between junction and case

Table 4.11 RC values of the Cauer Network representing the impedance between junction and case of SiC diodes

	1	2	3	4	5
R	0.06037°C/W	0.132°C/W	0.4142°C/W	0.04601°C/W	0.3984°C/W
C	0.4201mJ/°C	1.418mJ/°C	3.318mJ/°C	17.93mJ/°C	22.3mJ/°C

The next stage of the thermal modeling is the characterization of commutation and conduction losses of the SiC diodes. As already evoked, they have essentially no commutation losses, and those due to the conduction are defined through equation (4.5). This mathematical equivalence is defined in the datasheet and corresponds to the classic ON-state equivalent circuit of diodes, which is the series association of a voltage source and a resistor. In equation (4.5), in relation to I_D the zero-order coefficient corresponds to the threshold voltage (V_T) and the first-order coefficient is the ON-state resistance (R_T).

$$V_{ON} = \left(0.98 - \left(T_j \cdot \frac{1.6}{1000}\right)\right) + I_D \cdot \left(0.04 + \left(T \cdot \frac{0.522}{1000}\right)\right) \tag{4.5}$$

To estimate the precision of the thermal model, a 10 minutes simulation was executed, and the same operation point was reproduced with the prototype to compare the results. The operation point corresponds to an output DC with a voltage of 230V and a DC current of 8A. In Figure 4.19 it is possible to observe the simulation result.

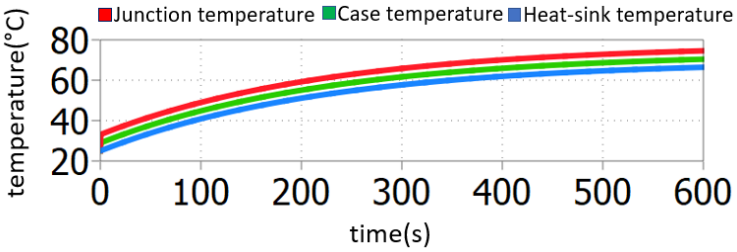

Figure 4.19 Thermal simulation using PLECS

The variation of temperature in the prototype was evaluated with a FLIR E96 industrial thermal camera. Once the operation point was reached, 10 minutes were counted on the clock and then the temperature was measured. The result can be observed in Figure 4.20. In the left side of the figure, there is a thermal image of the diode rectifier bridge and in the right side, the active bridge with SiC MOSFETs is shown.

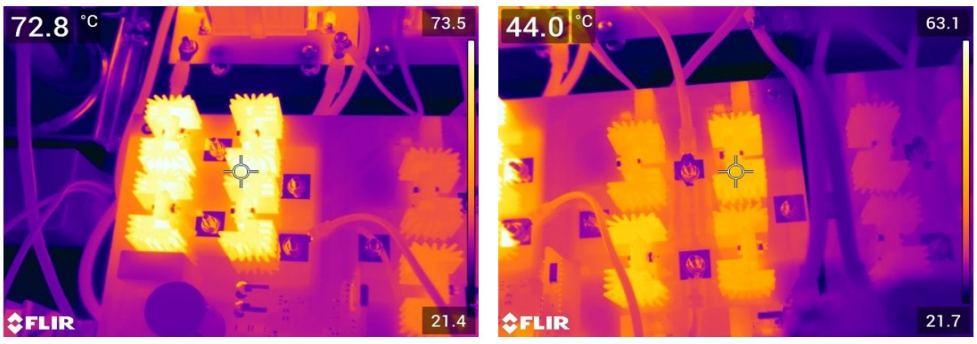

Figure 4.20 Thermal image of the diode rectifier bridge (left) and the active bridge (right)

From PLECS simulation, it is possible to find that the case temperature reaches 70.5°C after 10 minutes, corresponding to a junction temperature of 77°C, and the thermal image shows that the highest temperature point is at around 73.5°C. Even if there is a reflection phenomenon caused by the heat-sink (especially in the left-side figure), it remains an estimated temperature which is close to the one obtained with the simulation model. Another conclusion is that, as expected, the diode rectifier bridge is the

weakest point in terms of thermal endurance, since for the same operation point and thermal circuit, the active bridge is at lower temperature (around 44°C).

4.4.3. Current limitation

Through the simulation model, it is also possible to evaluate the performance of the current limitation technique evoked in Chapter 3. To do so, a 350VDC-10A operation point is reached. In t=0.03s a short circuit is executed directly at the output of the AC/DC converter (zero distribution length) with a fault impedance of 10mΩ. A comparison between the behavior of the converter with and without current limitation can be seen in Figure 4.21.

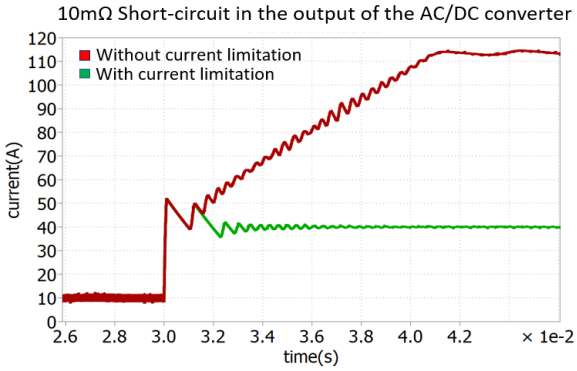

Figure 4.21 Current limitation technique

It is possible to observe that without the saturation of the current reference, the control system tries to compensate the voltage dip created by the short-circuit increasing the duty-cycle and increasing the current. It goes up until the limit of duty-cycle is achieved. Conversely, when the current reference is submitted to a saturation function, the control system progressively reduces the duty-cycle to keep the current at a certain determined value which here is considered to be 40A. This way, it is possible to virtually create enough thermal endurance to make the first line protection device operate, whether is the central protection device or the one protecting a load feeder.

4.5. Protection strategy to reach selectivity with load feeders

Regarding the protection plan, this work focuses on protecting the front-end AC/DC converter, as well as load feeders, while respecting overcurrent selectivity rules at the same time. The strategy described in Chapter 3 will be used for the conception of this stage of the protection plan. Since the AC/DC converter prototype is designed for a maximum operation of 3.5kW, the study developed by this work around protection schemes represents a scaled-down analysis. This type of initial study may be useful to conceive a protection strategy without taking the risks of dangerous high-power operation points.

4.5.1. Protection against DC overcurrent using TMCBs

As already discussed, the focus of this work is to look for simple overcurrent detection methods of reaching selectivity, using protection devices made with classic and standardized technologies, such as fuses and TMCBs. The first stage of the strategy used here is to address the protection against overcurrent (overload and short-circuit). Due to the maximum output current of the AC/DC converter

prototype being around 10A, two load feeders are considered, one at a rated current of 6A and the other one at 4A.

Following the protection strategy described in Figure 3.22 Selective protection coordination flowchart, it means that a 10A DC TMCB may be used to protect the AC/DC converter, and downstream two TMCBs of 6A and 4A may be used to protect each load feeder. The set is shown in Figure 4.22. The most logic choice here seems to be Z-curve TMCBs, since they have the lowest tripping current envelopes.

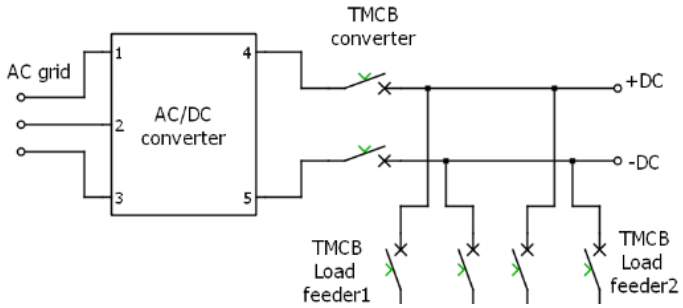

Figure 4.22 Protection scheme using three TMCBs

To continue this study, ABB S282-Z UC TMCBs are chosen. From the datasheet [**ABB15b**], it is possible to identify that the short-circuit tripping current envelope is between 3 and 4.5 times the rated current. A selectivity analysis based on ITOC curves is presented next in Figure 4.23. The idea is to compare the ITOC curve of the highest rated current TMCB protecting load feeders (6A) with the central TMCB (10A) protecting the AC/DC converter. If selectivity is respected in this case, it will be respected for all other load feeders as well.

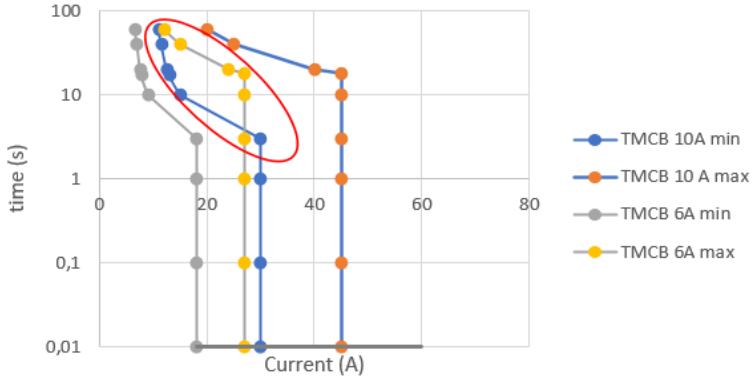

Figure 4.23 Selectivity analysis between TMCBs

It is possible to observe that from a short-circuit magnetic tripping point of view, there is no crossing points, and selectivity rules are respected. However, in the overload zone, there is an area (encircled in red in Figure 4.23) in which selectivity is not respected. Consequently, two options are possible. Either the 6A load feeder must be split into two new feeders with a lower rated current, or the central TMCB may be replaced by an UF DC fuse. The second option looks to be the most suited one since it is not always possible to split load feeders.

4.5.2. Protection against DC overcurrent using UF fuses and TMCBs

For this attempt of respecting selectivity rules, 10A UF fuses from Mersen were chosen instead of the front TMCB. In the datasheet [**MER16**] it is possible to find the ITOC curve of the fuse, which makes it possible to compare it with the one from the highest rated current TMCB of load feeders. The

result is shown in Figure 4.24 and the fuse's ITOC envelope corresponds to a ±8% value of the rated current.

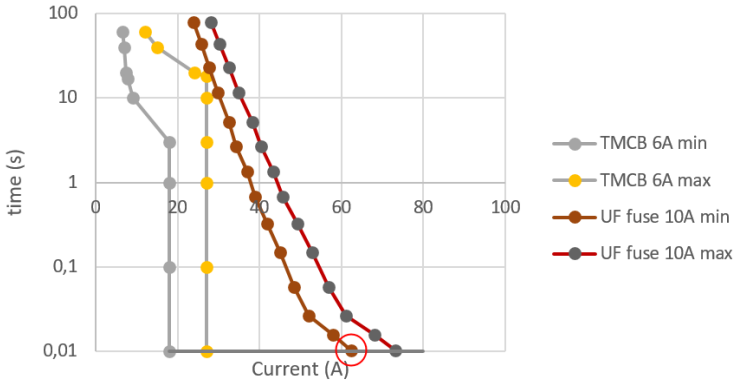

Figure 4.24 Selectivity analysis between UF fuse and TMCBs

It is possible to observe that the only crossing points between the ITOC curves is at the limit of the TMCB curve (red circle), which means above this point (60A), selectivity rules are respected for all load feeders, in the short-circuit and in the overload zones. For these set of protection devices, the complete scheme is shown in Figure 4.25.

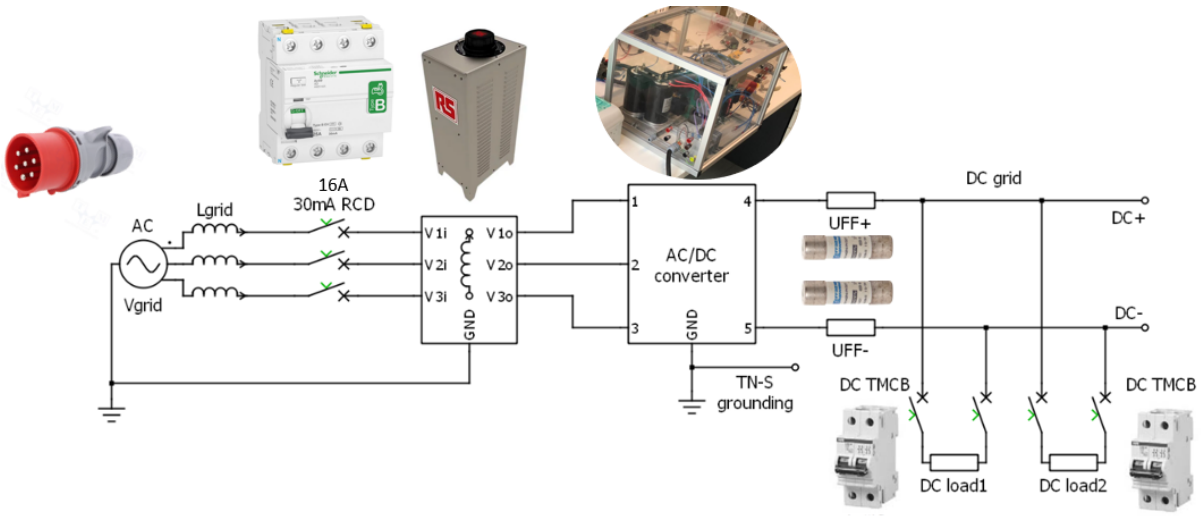

Figure 4.25 Protection devices used in the testbed

DC UF fuses are placed in both positive and negative poles, because the prototype can be used to test different grounding systems where the negative pole needs to be protected as well as the positive one, such as TN-S grounding.

The protection in the AC side is a 16A TMCB associated with a 30mA RCD. The TMCB is the first line of protection in case of short-circuit in the autotransformer and a last line of protection in case of short-circuit at the DC side. The rated current of 16A is selected because this is the limit of the three-phase plug. On its side, the RCD is important to prevent AC insulation faults in the autotransformer or in the prototype's case.

The next stage of the strategy is to define a saturation value for the current reference and to make sure the converter withstands the short-circuit currents. The saturation current can also be chosen to limit the maximum current fed by the AC/DC converter to a smaller value than the one in the crossing point in Figure 4.24, this way a full selectivity is achieved. From this perspective, a saturation value of 60A seems to be a reasonable option.

4.5.3. Short-circuit behavior of the AC/DC converter and thermal endurance

The main idea here is to perform short-circuit simulations to obtain points representing the thermal endurance of the AC/DC converter. These points will be placed in the ITOC graph to ensure that the time delay took by the fuse to stop a fault is smaller than the time which the converter can withstand the short-circuit current. The limit time during fault tolerated by the converter is deeply related to the evolution of the junction temperature of SiC diodes.

The steady-state operation point before the short-circuit is the one for which the temperature was verified with the thermal camera. It corresponds to an output current of 8A and a case temperature of 70.5°C, which is represented in Figure 4.20. From this simulation result, it is possible to observe that the junction temperature of the diode bridge of the SAB is estimated as 77°C, which is used as the starting point for short-circuit simulation. To reach different magnitudes of short-circuit current, different fault impedances where used, following the diagram shown in Figure 4.26. In addition, the time delay which the converter can withstand is measured leaving an 8.75°C margin (5%) of the 175°C junction temperature limit. The results for different magnitudes of short-circuit current can be observed in Table 4.12.

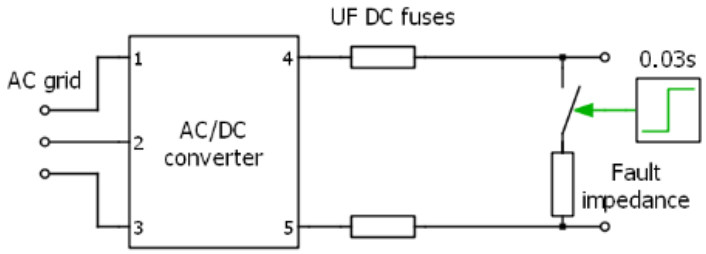

Figure 4.26 Variable fault impedance simulation

Table 4.12 Short-circuit thermal endurance time delay of the AC/DC converter

AC/DC converter prototype thermal endurance		
Short-circuit current (A)	**Time delay to reach Tj=166.25°C (s)**	**Short-circuit impedance (Ω)**
60	0.1	0.01
50	0.185	8.75
40	0.35	11.6
30	0.875	17.5
20	∞	35

From this point, it is possible to plot these points in the ITOC graph presented before in Figure 4.24, with the 6A TMCB and 10A UF fuse. The result can be observed next, in Figure 4.27.

It is possible to see that, in the red circled area, SiC diodes will reach their maximum junction temperature before the UF fuse can melt to stop the fault. Two possibilities exist to avoid this problem. The first one is to operate changes in the thermal circuit of heat dissipation in the converter, changing the heat-sinks for others with lower thermal impedance for example, or adding forced air cooling. The other option is to use the UF fuses to protect the converter in the case of short-circuit currents higher than the saturation limit, which can be reached if the current limitation control fails. In addition, the strategy is to use the capacity of the converter to shut-down the power supply for current levels below the saturation limit.

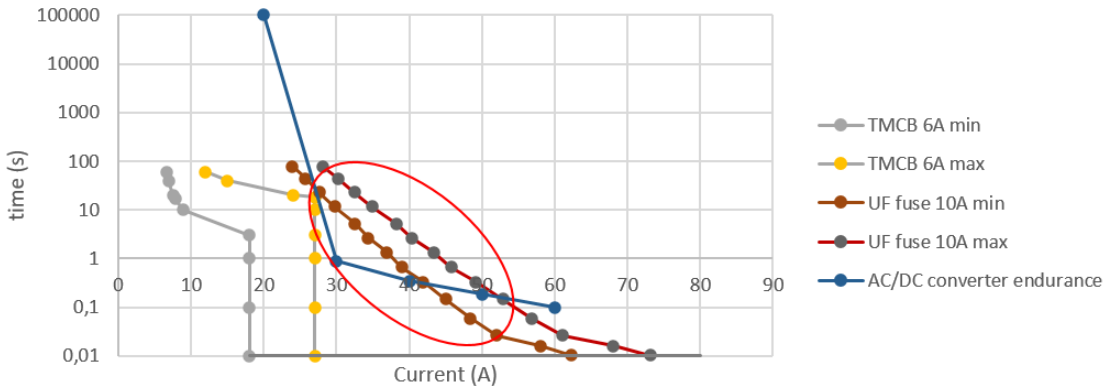

Figure 4.27 Complete selectivity analysis

To avoid changing hardware in the converter, the second option is adopted here. The current saturation limit in this case is 60A, and for this level of fault current, the converter can withstand around 100ms. Which means that, if the converter detects a current level above from 20 A (selectivity limit), it should interrupt the power flow in 100ms at maximum. Half of this period can be used as a temporal delay for TMCBs to operate in case the fault is in one load feeder. This implies that the control system must stop the power flow in 50ms. An example of this operation can be seen in Figure 4.28, for a fault current of 60A in which the converter is in current limitation mode.

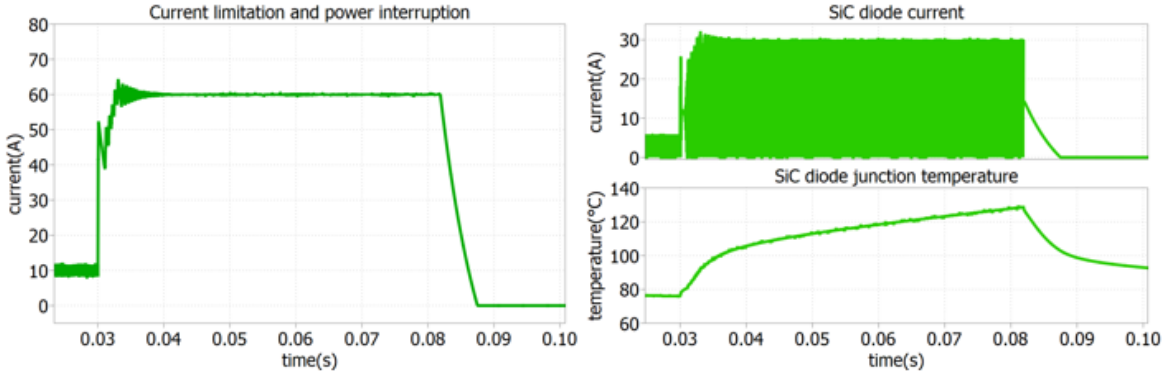

Figure 4.28 AC/DC converter operation under 60A fault

A last consideration to be made is that in the datasheet of the fuses employed here, no information is provided in respect to the overvoltage generated during fusion. Therefore, experimental tests must be conducted to measure this voltage level and to confirm if SiC diodes can withstand it. If it is not the case, MOVs, TVS diodes or other solutions must be considered.

4.6. Performance of the AC/DC converter in terms of power quality

In this last section, the simulation model and the prototype were used to evaluate the performance of the AC/DC converter from the power quality (PQ) perspective. Voltage dips are the most common transient disturbance impacting distribution grids, thus it seems important to give a special attention to their potential impact from a DC perspective. Consequently, from a transient point of view, the main focus here is to study the behavior of the converter when submitted to voltage dips coming from the AC grid, and how the control system manages voltage dips created in the DC grid by load variations. In terms of steady-state evaluation, the indicators defined in section 2.4.3.2 from Chapter 2 will be applied to characterize the generated DC voltage. Furthermore, an adaptation of the method proposed in section 3.6.2.2 to find a frequency dependent model of the AC/DC converter is presented.

4.6.1. Immunity of the AC/DC converter to AC and DC voltage dips

For this study, the last presented unidirectional simulation model is employed. Since voltage dips are the most frequent transient phenomena impacting grid-connected devices, it is important to evaluate how the AC/DC converter reacts to them, either in AC or in DC. In the case of voltage dips coming from the AC grid, an alteration in the input three-phase voltage level is created and maintained for 600ms (average voltage dip duration), considering different percentages of variations. On the other hand, for DC voltage dips, load changes are executed in several percentages, generating different behaviors in the DC grid and in the converter. In this case, the ITIC curve can be used to see if the converter respects the time periods determined by the curve for different levels of voltage variation. Results can be observed in Figure 4.29.

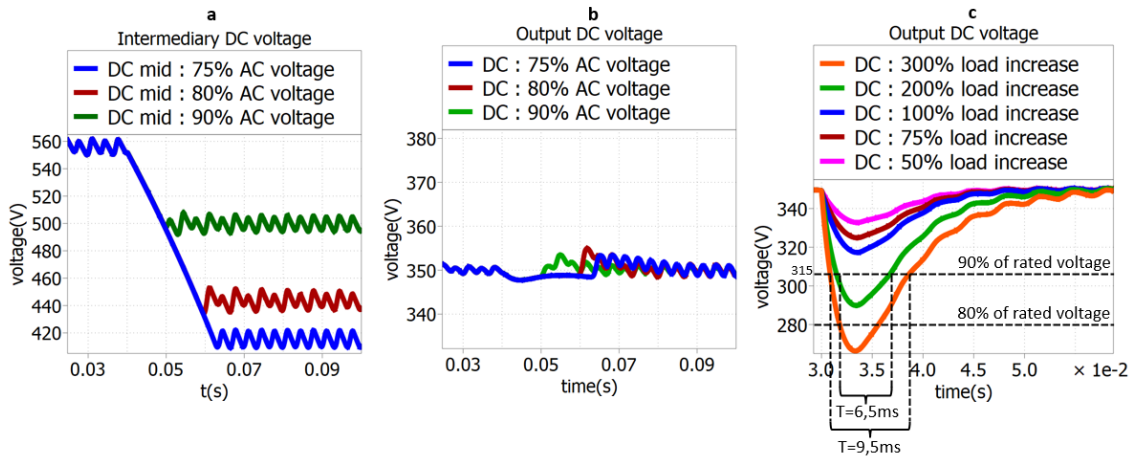

Figure 4.29 Impact of AC (a,b) and DC voltage dips (c) in the DC distribution system

In Figure 4.29 (a) it is possible to see the voltage levels in the intermediary DC bus for different levels of AC voltage dips. As expected, the voltage level goes down according to the percentage of the AC voltage in the input. The impact of this voltage variation in the output voltage of the converter can be observed in Figure 4.29 (b). For all the scenarios studied, the control system is able to bring the voltage back to rated value with small variations in a few hundreds of milliseconds. Finally, in Figure 4.29 (c), different cases of load variations are studied for an initial operation point of $350V_{DC}/5A$. It is possible to observe that for 50,75 and 100% load increase, the DC voltage does not reach levels inferior to 315 volts, which means that according to the ITIC curve, voltage remains in normal operation band. In the case of 200% load increase, DC voltage reaches the 80-90% band. However, the control system brings the voltage back to normal operation band in 6.5ms, which is considerably faster than the 10s limit showed in the ITIC curve. The 70%-80% voltage band is reached in the last simulation with a 300% load increase. Once again, the control system operates in 9.5ms, which is quicker than the 500ms established in the ITIC curve.

4.6.2. Output DC voltage characteristics

From a steady-state point of view, the DC voltage in the distribution grid can be evaluated according to indicators such as the RMS DC ripple and the peak-to-peak DC ripple. The operation point from Figure 4.13 is analyzed here, where the DC voltage is the curve represented in green. A zoomed temporal representation of the DC voltage is shown in Figure 4.30 (left), while a spectral equivalent is depicted in Figure 4.30 (right).

In the spectral representation it is possible to identify 3 relevant components. The 300Hz component, which comes from the three-phase rectifier at the input of the converter, the 80kHz component from the rectified 40kHz switched voltage wave in the transformer, and the components around 810kHz which come from the transient voltage disturbance generated during the commutation of SiC MOSFETs. From these measurements, it is possible to calculate some PQ indicators from equations defined in section 2.4.3.2, applying a time window of 10ms for mean and RMS values and a 200ms window for RMS and peak-to-peak ripple. Results are summarized in Table 4.13, which shows that the DC voltage has a low distortion level.

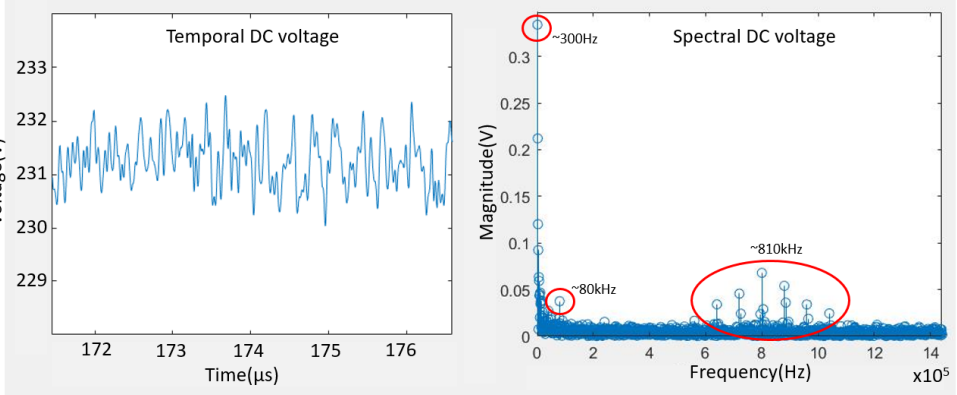

Figure 4.30 Temporal and spectral characteristics of the DC voltage

Table 4.13 PQ indicators for the output DC voltage

Mean voltage	RMS voltage	RMS Ripple	Peak-to-peak Ripple
231.2V	231.21V	0.39%	2.33%

4.6.3. Frequency-dependent impedance model

As a final result of this thesis, an experimental application of the current injection method shown in Figure 3.31 is used to determine a frequency-dependent equivalent impedance model for the AC/DC converter in the 0-2kHz frequency range with reasonable precision. This method is explained in detail in [**SLO23a**]. To be executed in practice, the disturbing current source is represented by a switched resistor banc. A power Si MOSFET with a simple control is connected in series with the resistor banc to generate the 50Hz pulse current waves observed in Figure 4.31(left).

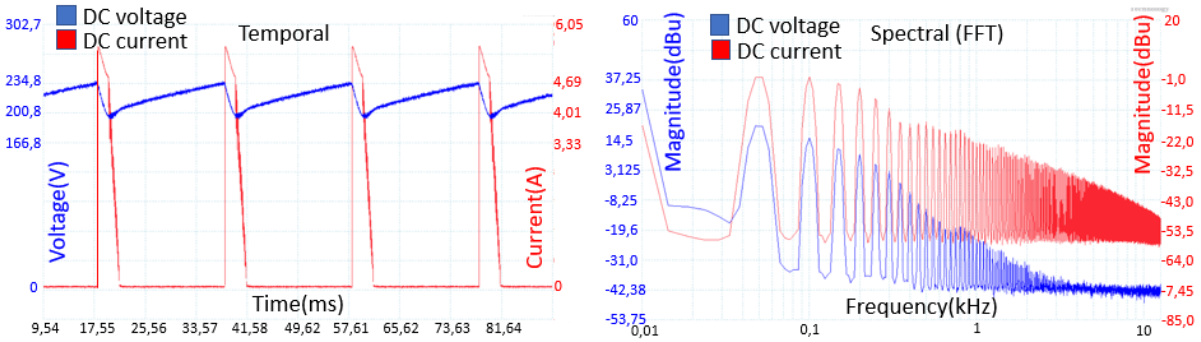

Figure 4.31 Temporal (left) and spectral (right) behavior of the DC voltage (blue) with 50 Hz pulsed disturbance (red)

With a variable resistor it is possible to modify the duty cycle in the control of the MOSFET. It is then possible to use a 50% duty-cycle, as described in section 3.6.2.2, or to reduce it to a lower value. The advantage of choosing a lower duty-cycle is that, since the pulse is closer to a Dirac delta function, the FFT has more spectral components. A 50% duty-cycle wave generates only impair multiples of its natural frequency. For this reason, a 10% duty-cycle is fixed. The spectral distribution can be observed in Figure 4.31(right). From the spectral distribution of DC voltage and current, it is possible to calculate the frequency-dependent impedance model, which is shown in Figure 4.32.

It is possible to observe a first resonance point around 400Hz in Figure 4.32. It corresponds to the output LC filter of the AC/DC converter, which was initially calculated to have a resonance frequency of 500Hz. The difference may come from the imprecisions in the capacitance and inductance values of individual components of the output filter.

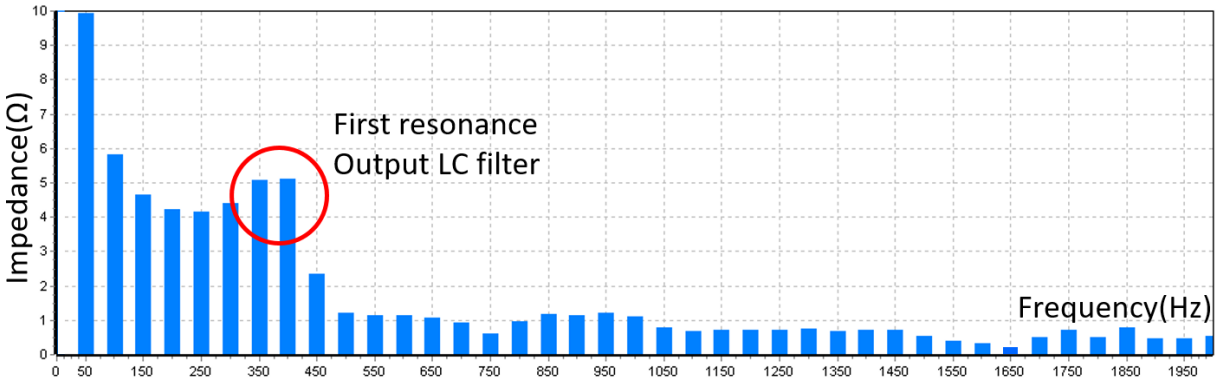

Figure 4.32 Frequency-dependent impedance values of AC/DC converter corresponding to a 0-2kHz range

The same method can be used for larger frequency ranges, 0-9kHz and 9-150kHz for example. In this application, an impedance value is calculated at each 50Hz step because the natural frequency of the pulses is 50Hz. It is possible to see from Figure 4.31(right) that for frequencies higher than 2kHz, this method becomes imprecise since the magnitude of current spectral components decreases progressively. Thus, higher frequency pulses can be used for spectral ranges above 2kHz.

A second experimental test is executed here using a pulsating disturbing current wave with a natural frequency of 10kHz, as it is shown in Figure 4.33. It is possible to observe that this time, since the base frequency is more elevated, it is possible to deduce impedance values for frequency values up to 150kHz. The downside of this method is that the increase of natural frequency results consequently in a reduced precision.

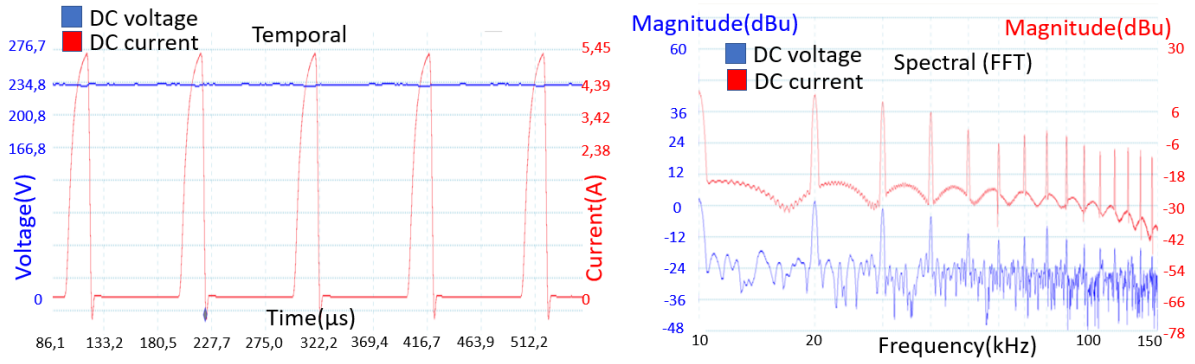

Figure 4.33 Temporal (left) and spectral (right) behavior of the DC voltage (blue) with pulsed 10kHz disturbance (red)

Once again, this method allows the calculation of a first approximation in terms of impedance model. It could be used in parallel with more precise methods such as frequency scanning for specific points of interest regarding spectral components. The obtained impedance model can be used then in frequency-domain simulation software to work as an equivalent of short-circuit impedance of a low-frequency transformer for LVAC grids. Associated to frequency-domain voltage and current sources, it would be possible to model an LVDC grid and to execute a complete power quality and disturbance propagation analysis.

4.7. Conclusion

The simulation model built in PLECS platform is particularly useful to understand the behavior of power electronics converters integrated in a distribution grid. Through the model developed in this work, it was possible to simulate short-circuits and to understand how these fault scenarios impact power switches. It is also possible to see that for the SAB topology considered in this chapter, SiC diodes were the weakest components in terms of thermal endurance. However, the SiC technology is well suited to increase the thermal endurance of power converters. Their possibility of reaching higher junction temperatures (175 to 200°C), associated to smaller ON-state resistance (R_{DSon}), allows a considerable increase in the time this switch can withstand high-current levels.

Another important inference concerns the protection plan. As it was demonstrated, it is possible to create a selective protection scheme for LVDC distribution systems using current limitation techniques in the front-end converter, TMCBs and UF fuses. It may be a solution explored in the future to avoid the use of overexpansive protection equipment or complex coordination between different protection devices.

Finally, the behavior of the converter in relation to AC and DC voltage dips has been evaluated, showing that the proposed control system and the power electronics architecture is reasonably robust. The quality of the DC voltage is evaluated next according to indicators such as RMS DC ripple, demonstrating that the AC/DC converter can provide voltage with low spectral disturbances. In addition, a method applied to identify a frequency-dependent impedance model for the front-end converter provided impedance values which could be used next to evaluate the propagation of load disturbance. It can be concluded that the design methods implemented in this chapter give reasonable results in terms of voltage characteristics and spectral disturbances. A last aspect to highlight is that the dynamic behavior of the control system developed in this work also allows the front-end converter to react in acceptable delays to mitigate transient disturbances such as voltage dips.

GENERAL CONCLUSION AND PERSPECTIVES

In this doctoral thesis the use of LVDC for distribution grids is analyzed from the perspective of power electronics, protection schemes and power quality. Systems based in DC grid architectures are being proposed all around the world as potential enhancers of Renewable Energy Sources and Energy Storage Systems integration in the energy mix. Nonetheless, the domain around LVDC still lacks maturity and well consolidated solutions to some scientific and industrial problems, such as the definition of selective protection schemes and the definition of power quality assessment methods. This research work attempts to contribute to these challenges, specifically trying to achieve the following objectives:

- **The design and implementation an AC/DC converter prototype capable of deploying a low power representation of an LVDC distribution grid**
- **The development of a cost-effective selective protection scheme for future LVDC distribution systems for the safety of users, assets, and the grid itself against short-circuit and electric shock**
- **The evaluation of power quality of LVDC distribution system in terms of steady-state and transient phenomena through well-defined and potentially standardizable indicators**

From Chapter 1 it is possible to observe that using DC instead of AC can be really advantageous in scenarios where there is significant local energy generation through PV and ESS and energy consumption in DC. Gains in terms of energy efficiency vary according to different hypothesis, but most studies developed in the subject show encouraging results. From this chapter it is also possible to see that, even in the absence of specific standards, 350-400V_{DC} full-DC grids are already being deployed around the world in different ecosystems and configurations.

In Chapter 2 the three main subjects of this thesis were approached from an exploratory point of view. At a first moment, it is possible to conclude that, isolated converters with medium-frequency transformers are a reasonable choice for LVDC systems since they have a significantly high-power density and can also be controlled to limit short-circuit currents in the DC side. In addition, through this chapter it is possible to observe that two of the major challenges associated to protection schemes in LVDC are associated to the application of selectivity rules and to the protection against electric shock. In the same train of thought, it is also possible to observe that different protection devices and coordination strategies exist to try to overcome these problems. Finally, from this chapter it is also possible to identify different transient and steady-state metrics to evaluate power quality in DC systems, such as voltage sags, voltage swells, RMS DC ripple, and distortion level.

Through Chapter 3 the perimeter of the study conducted in this work is defined around a monopolar LVDC grid, deployed through an isolated front-end AC/DC converter with a TN-S earthing system. Electrothermal simulation models of the converter are designed to support protection and power quality studies, in parallel to the sizing of the experimental prototype. At this stage this work differentiate itself from most research in the domain due to the use of silicon carbide semiconductors in the DC/DC isolated converter and to the presence of an output inductor to limit short-circuit current in the DC grid side. Furthermore, an important point is that a methodology is defined to investigate the possibility of achieving selective protection schemes for the LVDC grid through current limiting techniques of the front-end converter. Moreover, a study of power quality related phenomena from the perspective of the front-end converter shows that its control system can potentially be designed to avoid or mitigate the most part of transient phenomena. In addition, in the end of this chapter it is possible to identify

frequency bands for steady-state power quality evaluation and which components of the front-end converter impact specific bands.

In Chapter 4 the most part of simulation and experimental results are shown. Concerning the AC/DC converter prototype, it is possible to observe considerable improvements in each new version, in terms of electromagnetic compatibility, spectral distortion of DC voltage and maximum power. The use of silicon carbide MOSFETs and diodes with lower channel resistance and higher maximum junction temperature than silicon equivalents enhance the thermal endurance of the converter. These features associated to fault current control designed in Chapter 3 allow the use of classic protection devices against short-circuits, such as ultra-fast fuses and DC thermomagnetic circuit breakers. This aspect is important because it shows that selectivity can be achieved with cost-effective devices. Additionally, in respect to power quality assessment, it is possible to observe that the designed control system is robust against AC and DC voltage sags, which is demonstrated by the comparison of the converter time response with time thresholds defined by the ITIC curve for electronic equipment. Regarding the evaluation of the DC voltage through steady-state indicators, it is possible to observe that the output voltage of the AC/DC converter has a low level of spectral distortion, and the existing spectral components are similar to the ones expected in theory. Finally, a frequency-dependent impedance model identification method is proposed for disturbance propagation analysis. The method prove itself to be simple to execute and variating the frequency of pulses different frequency bands can be explored, based on the zone of interest and on the desired precision.

After the completion of this work, is it possible to see that multiple steps can be considered for future works. As with any comprehensive study, certain limitations appeared through the course of this research, which opens paths for future contributions in the domain of LVDC distribution grids. In terms of power electronics, the prototype was tested for a maximum voltage of 230V which is still far from the $350V_{DC}$ being used in different LVDC ecosystems around the world. The same observation can be done in terms of power, since the 3.5kW of the AC/DC converter are inferior to the power needed in a small house. Consequently, an improved and potentially bidirectional version of the prototype may be needed for further studies. Moreover, the closed-loop control system and fault current limitation technique were only executed in simulation and an experimental version is still to be implemented.

From the protection point of view, short-circuit tests were realized only in simulation and directly in the output of the AC/DC converter. In future studies, cables must be considered and their influence in short-circuit currents must be evaluated. Additionally, real short-circuit tests must be executed to validate the fault current limitation and shut-off strategy, and selectivity rules between ultra-fast fuses and DC thermomagnetic circuit breakers, especially in load feeders. All these tests must ensure that for several fault scenarios, power switches remain operational and do not reach the maximum junction temperature. Additional tests with fuses and DC circuit breakers are also needed to determine the level of overvoltage created during arc extinction. They would allow proper sizing of anti-overvoltage components to avoid destruction of power switches in case of fault interruption.

Finally, regarding power quality assessment methods, this work focused mainly on the influence of the front-end AC/DC converter in multiple indicators. It is necessary to expand the concepts explored in this thesis for the case where there are multiple converters connected to the grid and cable models are also considered. Once the closed-loop control is validated and operational, real tests can be executed to evaluate the immunity of the grid to AC and DC transient phenomena. From the perspective of steady-state evaluation, the same indicators used to analyze the output DC voltage of the AC/DC converter may be also used in experimental scenarios with non-linear loads. Finally, the frequency-dependent impendence model should be characterized for larger frequency bands, up to 150kHz, to be used for disturbance propagation studies. Consequently, new tests and measurements are needed as well.

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ANNEX A. ARC EXTINCTION IN DC SYSTEMS

An electric arc is created when the inductive effect of a circuit creates a high voltage between two conductive parts that are being separated in order to keep the current flowing. It is exactly what happens when a protection device tries to clear a fault by physically interrupting the circuit. If the air around the arc is sufficiently ionized, it may not stop even with the zero current crossing, in the case of AC systems. For DC systems, to extinguish an electric arc is even more difficult since there is no natural current zero crossing (Figure A.1).

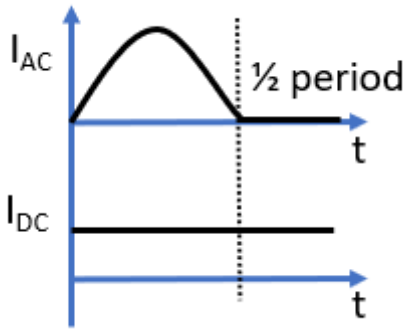

Figure A.1 Comparison of AC and DC systems regarding arc extinction

In reality, the electric arc has a non-linear voltage-current characteristic and the capacity to extinguish it in DC is generally related to increasing its resistance. Consequently, the voltage between the two disconnected parts of the circuit rises and the current reaches zero **[KIM18b]**. As showed in Figure A.2, the condition to extinguish the arc is $\left(\frac{di}{dt} < 0\right)$, so to stop the current flow it is necessary to reach a high arc voltage level ($V_A > V_S$) **[ABB10a].** Also, the extinction time is related to the time constant of the equivalent circuit $\left(\tau = \frac{L}{R}\right)$.

$$L\,\frac{di}{dt} = V_S - Ri - V_A \tag{A.1}$$

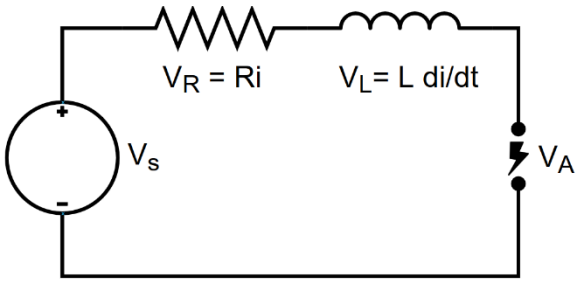

Figure A.2 Equivalent circuit of an electric arc

ANNEX B. ELECTRONIC BOARD DESIGN MODELS FOR THE THIRD VERSION OF PROTOTYPE

For the third prototype the PCB design software KiCAD is used. The correct connections between different electronic components are made using the scheme editor. It is possible to observe the power side of the board in Figure B.1 and the control/measurement part of the board in Figure B.2

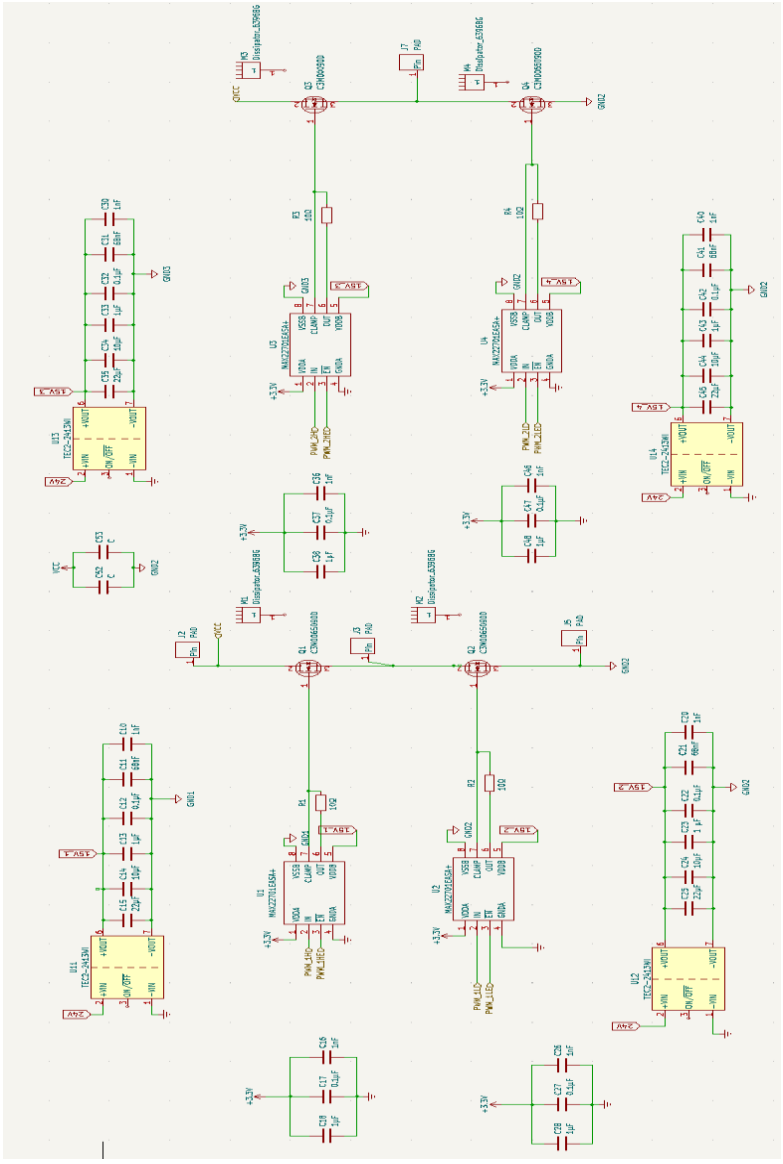

Figure B.1 Power side of the electronic board of the third prototype

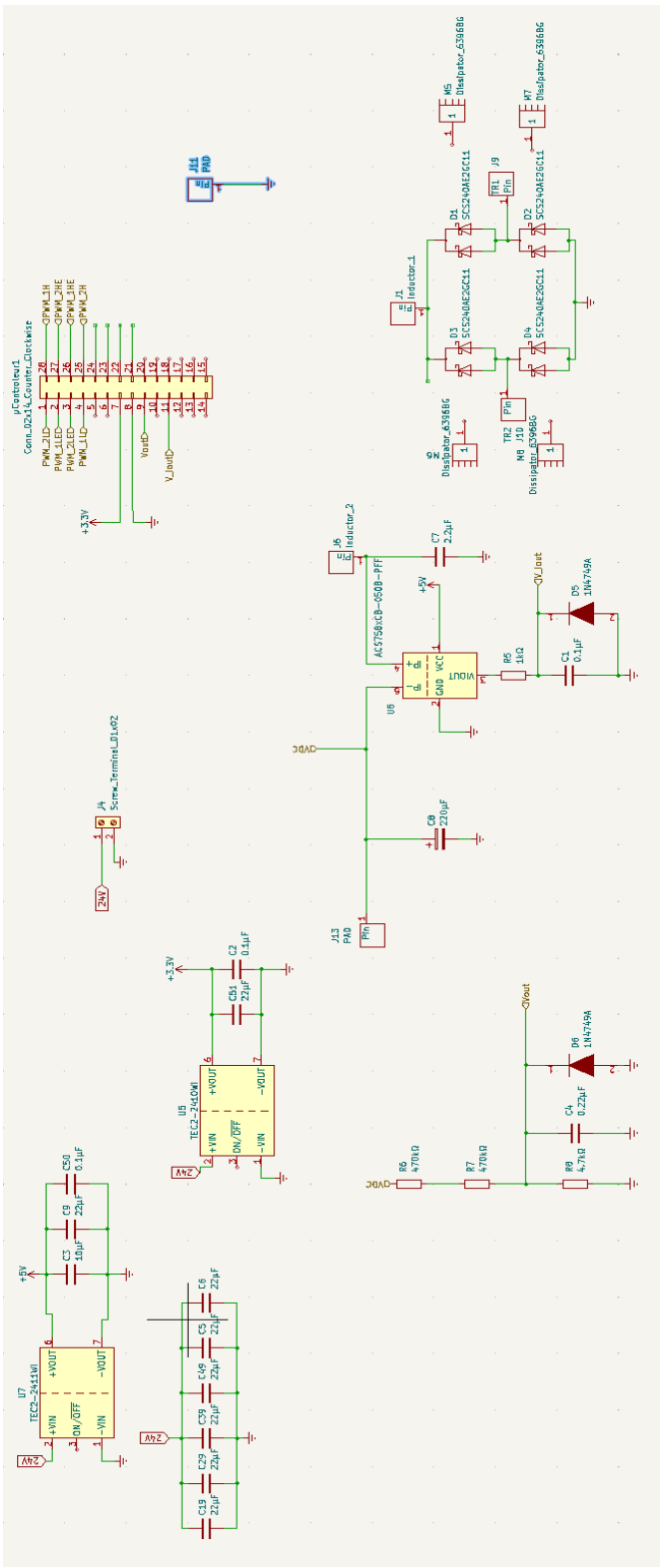

Figure B.2 Control/measurement side of the electronic board of the third prototype

In a second moment, the disposition of the electronic components and the traces in the electronic board are studied with the help of the PCB editor, along with the set of different layers and ground plane. The final result can be observed in

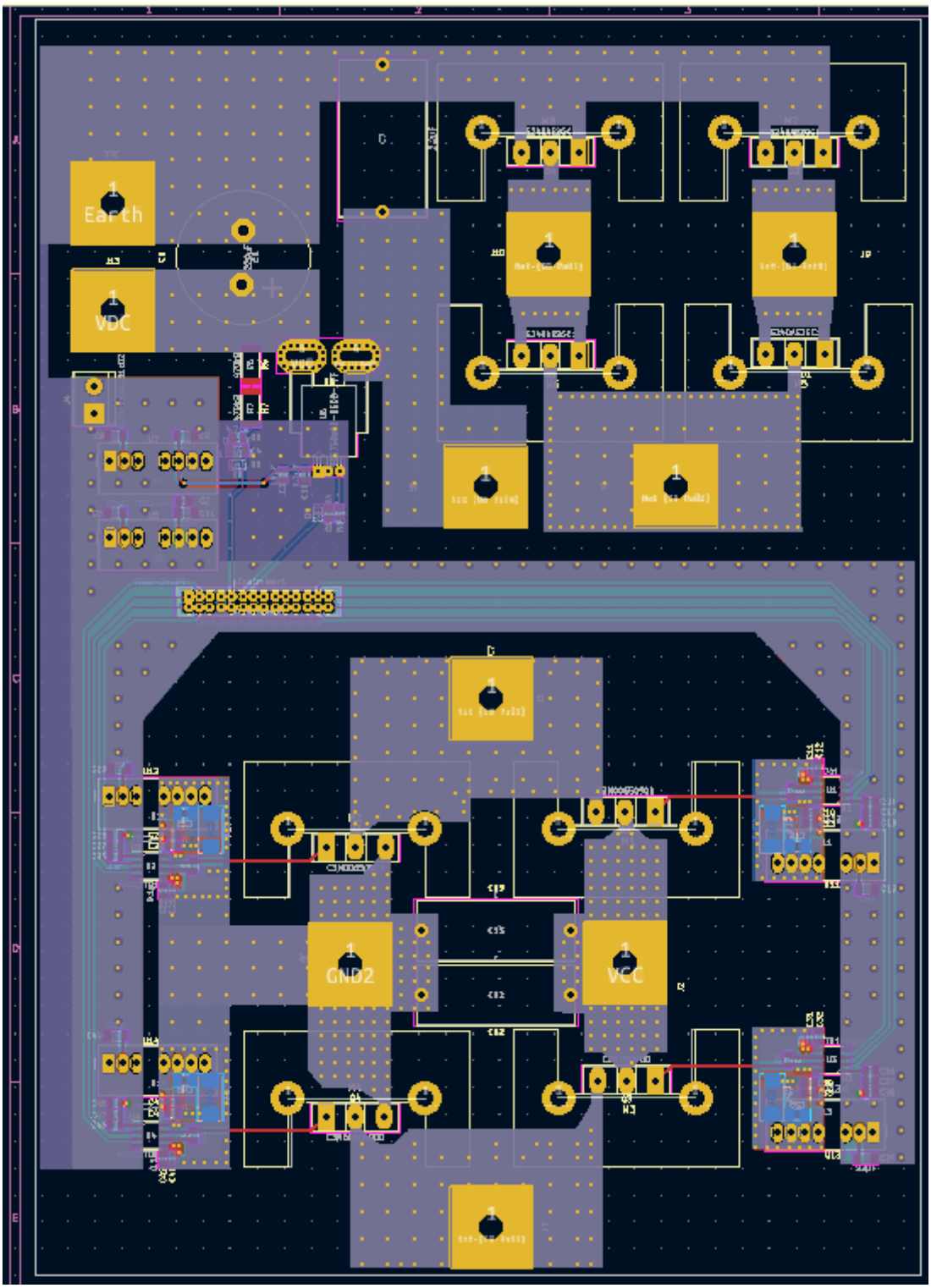

Figure B.3 Electronic board design for the third prototype