# Contribution to the fault-tolerant distributed control of multiphase converters dedicated to supplying microprocessors for automotive applications

Miguel Mannes Hillesheim


# THÈSE

**En vue de l'obtention du**

## DOCTORAT DE L'UNIVERSITÉ DE TOULOUSE

**Délivré par :**

Institut National Polytechnique de Toulouse (Toulouse INP)

**Discipline ou spécialité :**

Génie Electrique

---

**Présentée et soutenue par :**

M. MIGUEL MANNES HILLESHEIM

le lundi 13 décembre 2021

**Titre :**

Contribution au contrôle distribué tolérant à la panne des convertisseurs multiphases dédiés à l'alimentation de microprocesseurs pour application automobile

---

**École doctorale :**

Génie Electrique, Electronique, Télécommunications (GEETS)

**Unité de recherche :**

Laboratoire Plasma et Conversion d'Énergie (LAPLACE)

**Directeur(s) de Thèse :**

M. MARC COUSINEAU

M. GUILLAUME GATEAU

**Rapporteurs :**

M. ERIC LABOURE, SUPELEC

M. YVES LEMBEYE, UNIVERSITE GRENOBLE 1

**Membre(s) du jury :**

MME XUEFANG LIN-SHI, INSA LYON, Présidente

M. CYRILLE GAUTIER, SAFRAN SA, Membre

M. ÉRIC ROLLAND, NXP SEMICONDUCTORS, Invité(e)

M. GUILLAUME GATEAU, TOULOUSE INP, Membre

M. MARC COUSINEAU, TOULOUSE INP, Membre

M. NICOLAS ROUGER, TOULOUSE INP, Membre

# Remerciements

## Résumé

Les systèmes d'aide à la conduite automobile sont en mesure de prendre le contrôle du véhicule en cas de danger. La redondance et la capacité de reconfiguration en cas de panne des ordinateurs embarqués sont fondamentales pour assurer la continuité de la mission. L'alimentation des cœurs des processeurs se fait généralement à l'aide de convertisseurs multiphases qui offrent naturellement plusieurs chemins de courant (redondants) vers le processeur en raison de leur topologie parallèle. Cependant, l'organe de contrôle du convertisseur représente une faiblesse en termes de disponibilité car implanté majoritairement de manière centralisé. NXP Semiconductors a initié un partenariat avec le laboratoire LAPLACE afin de financer cette thèse pour l'étude d'un mode de contrôle distribué tolérant à la panne. Cette thèse se focalise sur l'utilisation d'une méthode de contrôle distribué, ne présentant aucun point de panne singulier, pour développer un organe de gestion de l'entrelacement des signaux de commande, modulaire et redondant, ainsi que pour maitriser son fonctionnement, en termes de temps de réponse et de stabilité.

Le Chapitre I présente le contexte et l'état de l'art. Le contexte concerne la stratégie de sûreté de fonctionnement intégré utilisée par NXP ; une étude des exigences et des technologies récentes est présentée pour comprendre les enjeux de la conception des alimentations des processeurs modernes ; la tendance de l'augmentation de la charge de calcul requise et de la consommation électrique résultante est mise en évidence ; et l'adoption de convertisseurs multiphases est justifiée. Un état de l'art couvre alors principalement les techniques de contrôle distribué modulaire appliquées à la régulation de la tension de la charge et à l'équilibrage des courants des phases, puis aux techniques d'entrelacement, nécessaires au fonctionnement des convertisseurs multiphases.

Les Chapitres II et III présentent l'étude théorique et l'évaluation respectivement de deux techniques d'entrelacement par approche distribuée préexistantes La même approche de modélisation est appliquée dans chaque chapitre pour obtenir un modèle à multiples entrées et multiples sorties conforme aux spécificités de chaque approche, dans le but d'identifier enfin les conditions de stabilité à respecter. Les particularités liées à la modélisation et à la mise en œuvre des simulations de validation sont décrites. Par la suite, une technique de choix de

correcteur pour l'optimisation de la réponse transitoire est proposée. Les singularités de chaque approche sont discutées et des simulations sont fournies à des fins de vérification.

Le Chapitre IV présente l’élaboration d'une nouvelle approche originale de contrôle distribué pour l'entrelacement des signaux de commande, ainsi que son analyse. Il s'agit d'une approche à signaux mixtes, composée de quelques éléments de logique numérique et d'un noyau analogique. L'étude théorique et l'évaluation de cette nouvelle technique d'entrelacement sont présentées, ainsi que des résultats de simulation. Une preuve de concept a été élaborée en utilisant des composants CMS associées sur une carte de circuit imprimé. La réponse dynamique est vérifiée expérimentalement pour les perturbations modales, cas de démarrage et de reconfiguration. Le comportement lors d'un événement de panne de communication est également observé, comprenant le cas d'un court-circuit de ligne à la masse et de court-circuit de ligne à ligne.

Mots Clés: Défaillance opérationnelle, tolérant à la panne, redondance, contrôle distribué, reconfiguration, continuité de mission, entrelacement, modulaire, extensible, chaine circulaire.

## Abstract

Advanced Driver-Assistance Systems can take control of the vehicle in case of danger. Redundancy and reconfiguration ability in case of fault occurrence are fundamental to ensure mission continuity. The supply of computer cores is made usually with multiphase converters that offer naturally multiple (redundant) current paths to the processor thanks to its parallel topology. However, converter controller is a weakness in terms of availability usually implemented in a centralized way. NXP Semiconductors has initiated a partnership with the LAPLACE laboratory to finance this thesis for the study of a fault tolerant distributed control mode. This thesis focuses on the use of a distributed control method, presenting no single point of failure, to develop a modular and redundant control signal interleaving management unit, as well as to control its operation, in terms of response time and stability.

Chapter I presents the context and state of the art. The context presents the NXP safety path; a survey of requirements and techniques is developed to understand up-to-date processors power supply; trends of workload and power consumption increases are highlighted; and the adoption of multiphase converter topology is verified. The state of the art covers mainly the modular distributed techniques applied on voltage regulation and current balance, and then on interleaving techniques, needed to multiphase converter operation.

Chapter II and III present the theoretical studies and evaluations of two preexisting distributed interleaving techniques. The same modeling technique is applied in each chapter to develop a multiple inputs multiple outputs model compliant with the specificities of each approach and then reveal the stability concern. Subsequently, a technique of choice of corrector for the optimization of the transient response is proposed. The singularities of each approach are discussed and simulations are provided for verification.

Chapter IV presents the conception of an improved original interleaving approach for control signal interleaving, as well as its analysis. It is a mixed-signal approach, consisting of a few digital logic devices and an analogue core. The theoretical study and evaluation of the new interleaving technique is presented, as well as simulation results. A proof of concept was developed using standard SMD components on a printed circuit board. The dynamic response of this interleaving approach is verified for modal disturbances, cases of start-up and

reconfiguration, where a module is inserted/removed during operation. The behavior during communication fault event are also shown, comprising the cases of a line shorted to ground and line-to-line short circuit.

Key words: Fail-operational, fault-tolerant, distributed control, reconfiguration, mission continuity, interleaving, modular, scalable, circular-chain.

# Contests

# List of figure

# List of tables

# List of acronyms

| | |
|---|---|
| AAA | American Automobile Association |
| ADAS | Advanced Driver-Assistance Systems |
| OpAmp | Operational Amplifier |
| AVP | Adaptive Voltage Positioning |
| AVS | Adaptive Voltage Scaling |
| CLTF | Close Loop Transfer Function |
| CP | Charge Pump |
| CPU | Central Processing Unit |
| DLL | Delay Locked Loop |
| DPD | Differential Phase Detector |
| DVFS | Dynamic Frequency Voltage Scaling |
| DVS | Dynamic Voltage Scaling |
| FVT | Final Value Theorem |
| FIVR | Fully Integrated Voltage Regulator |
| GPU | Graphics Processing Unit |
| IVR | Integrated Voltage Regulators |
| LC | Local Controller |
| LL | Load Line |
| MCG | Multiphase Clock Generator |
| MIMO | Multiple Input Multiple Output |
| NNP | Neural Network Processors |
| OLTF | Open Loop Transfer Function |
| PD | Phase-delay |
| PD | Phase Detector |
| PDLC | Phase-Delay Local Controller |
| PLL | Phase Locked Loop |
| PoL | Point of Load |
| PRM | Pre Regulation Module |
| SAC | Sine Amplitude Converter |
| SMD | Surface Mount Device |
| SMPS | Switching Mode Power Supplies |
| SPOF | Single Point Of Failure |
| TCG | Triangular Carrier Generators |
| VCDL | Voltage Controlled Delay Loop |
| VRM | Voltage Regulator Module |
| VTM | Voltage Transformation Module |

# General introduction

The mobility sector passes nowadays through a revolution. Electrical assistance is widely available in bikes and scooters. Fully autonomous vehicles are already available in the market. These vehicles can be individual or fit small groups of people, such as cars we know today. Recently general public flying taxis are being tested. These vehicles are composed of multiple electronic devices and computers. High availability and safety concerns have to be handled to avoid injures and damage. To overcome these challenges, safety strategies are evolving from the level “fail silent” (device disabled) to “fail operational” (fault corrected on-the-fly), when the device reconfigures to guarantee mission continuity in case of a failure.

This work is part of the partnership between NXP Semiconductors and “Laboratoire Plasma et Conversion d’Energie” (LAPLACE) on the development of embedded systems for the autonomous mobility. This work treats specifically the study and development of a modular fail operational control for multiphase power converters needed to supply the autonomous driving embedded computers. The studied techniques can be applied in any type of series and/or parallel multicellular converter topologies.

The fail tolerant control with reconfiguration ability is sought using modular distributed control without single point of failure. The distributed control of multicell converters requires the generation of interleaved PWM signals, the balance of current/voltages between cells and the output regulation. The ultimate objective of this thesis is the study and evaluation of the distributed control for future market introduction of a NXP product for core processor supply in automotive applications. This work focusses mostly on the interleaving approaches.

Chapter I presents the context and state of the art. The context includes the NXP safety path and focuses the step to reach fail operational power supplies for processors. The approach developed is based on distributed control without single point of failure. A survey of requirements and techniques is developed to understand up-to-date processors power supply; trends of workload and power consumption increase are highlighted; and the adoption of multiphase converter topology is verified. The state of the art covers mainly the modular distributed techniques applied on voltage regulation and current balance, and then on interleaving techniques.

Chapter II and III present the theoretical studies and evaluations of two preexisting distributed interleaving techniques. Chapter II studies a digital approach and chapter III studies an analog approach. The same modeling technique is applied in each chapter to develop a Multiple Inputs Multiple Outputs (MIMO) model compliant with the specificities of each approach and then reveal the stability concern. Modeling and simulation issues are described and a transient response optimization technique is proposed. Multiple specific items of each approach are discussed and simulations are provided for verification.

Chapter IV presents the conception of an improved original interleaving approach and its analysis. It is a mixed signal approach, composed of a few digital logic devices and an analogue core. The theoretical study and evaluation of the new interleaving technique is presented. Simulation results are shown and a proof-of-concept to validate the mixed signal interleaving approach presented. The modular distributed controller was conceived using functions on SMD components and multiple of them were associated on a printed circuit board. The dynamic response of this interleaving approach is verified for modal disturbances, cases of start-up and reconfiguration, where a module is inserted during operation. The behavior during communication fault event are also shown, comprising the case of a line shorted to ground.

In the same manner, Annex F presents a top level view of the architecture used for development of an integrated circuit using NXP SmartMOS10 technology applying the concepts developed in this document. Each module integrated is composed of a half-bridge power stage, a distributed carrier generator, a current sense and balance loop, a voltage regulation loop and a voltage reference.

# Author's bibliography

**Journals:**

- Mannes Hillesheim, Miguel, Marc Cousineau, Miguel Vivert, Guillaume Aulagnier, and Guillaume Gateau. "Eigendecomposition of a Digital Iterative Decentralised Interleaving for Multicellular Converters." *Mathematics and Computers in Simulation*, July 2020, S037847542030241X. https://doi.org/10.1016/j.matcom.2020.07.014.

- Q. D. Phan, G. Gateau, P. C. Nguyen, M. Cousineau, H. P. To, B.A. Nguyen, L. Veit, R. De Milly, and M. Mannes Hillesheim. "A Fast, Decentralized, Self-Aligned Carrier Method for Multicellular Converters." Applied Sciences 11, no. 1, 2021. doi: 10.3390/app11010137

- M. Vivert, M. Cousineau, P. Ladoux, J. Fabre, M. Mannes-Hillesheim, R. Diez, D. Patino, « Decentralised Control for Balancing the Cell-Voltages of a High Conversion Ratio Flying Capacitor Multilevel Converter, » JESTIE 2021 (Accepted for publication the 15 of September 2021)

**International conferences:**

- Hillesheim, Miguel Mannes, Marc Cousineau, and Loic Hureau. "Reconfigurable Partial-Decentralized Control of a Multiphase Converter for Fail-Operational Automotive Processor Power Supply." In *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, P.1-P.8. Genova, Italy: IEEE, 2019. https://doi.org/10.23919/EPE.2019.8915561.

- Gateau, M. Cousineau, M. Mannes-Hillesheim and P. Q. Dung, "Digital Decentralized Current Control for Parallel Multiphase Converter," 2019 IEEE International Conference on Industrial Technology (ICIT), Melbourne, Australia, 2019, pp. 1761-1766, doi: 10.1109/ICIT.2019.8755049

- G. Gateau, M. Cousineau, M. Mannes-Hillesheim, T. Robert and P. Q. Dung, "High Dynamic Current Control Using Decentralized PWM Generation for Parallel Multiphase Converter," 2020 IEEE International Conference on Industrial Technology (ICIT), Buenos Aires, Argentina, 2020, pp. 480-486, doi: 10.1109/ICIT45562.2020.9067112

- Q. Phan, G. Gateau, M. Cousineau, L. Veit, R. De Milly and M. Mannes-Hillesheim, "Ultra-fast Decentralized Self-Aligned Carrier Principle for Multiphase/Multilevel Converters," 2020 IEEE International Conference on Industrial Technology (ICIT), Buenos Aires, Argentina, 2020, pp. 517-522, doi: 10.1109/ICIT45562.2020.9067108

**National conferences:**

- M. Mannes-Hillesheim, M. Cousineau, G. Gateau, "Analyse Modale de l'Auto-Entrelacement de Porteuses par Approche Numérique Itérative," Symposium de Génie Electrique 2018, Nancy, France, juillet 2018.

**Patents:**

- "DISTRIBUTED INTERLEAVING CONTROL OF MULTIPHASE SMPCS", Application Number 19306559.6 , NXP USA, Inc. and INSTITUT NATIONAL POLYTECHNIQUE DE TOULOUSE, date de dépôt 12/02/2020, inventeurs : Miguel MANNES HILLESHEIM, Marc Michel COUSINEAU, Eric Pierre ROLLAND, Philippe GOYHENETCHE and Guillaume Jacques Leon AULAGNIER.

- "DISTRIBUTED CONTROL OF A VOLTAGE REGULATOR", Application Number 19306578.6, NXP USA, Inc. and INSTITUT NATIONAL POLYTECHNIQUE DE TOULOUSE, date de dépôt 12/02/2020, inventeurs : Guillaume Jacques Leon AULAGNIER, Miguel MANNES HILLESHEIM, Eric Pierre ROLLAND, Philippe GOYHENETCHE and Marc Michel COUSINEAU.

- "MODULAR INTERLEAVING TECHNIQUES FOR SCALABLE POWER ELECTRONICS CONVERTER", Application Number 20305395.4, NXP USA, Inc. and INSTITUT NATIONAL POLYTECHNIQUE DE TOULOUSE, date de dépôt 12/02/2020, inventeurs : Miguel MANNES HILLESHEIM, Marc Michel COUSINEAU, Eric Pierre ROLLAND, Philippe GOYHENETCHE and Guillaume Jacques Leon AULAGNIER.

# I. Context and state of the art

The AAA Foundation for Traffic Safety published in 2019 an article entitled “Think You’re In Your Car More? You’re Right. Americans Spend 70 Billion Hours Behind the Wheel” showing an increase of more than 6 percent on driving time from 2014-15 and 2016-17. Current technology, involving automation and robotics, pushes the development of autonomous driving vehicles and soon the mass deployment of robot taxis. It will allow people to do other activities while moving and improve mobility of non-enabled people.

In the other hand, according with the World Health Organization 2018 report “Every year the lives of approximately 1.35 million people are cut short as a result of a road traffic crash. Between 20 and 50 million more people suffer non-fatal injuries, with many incurring a disability as a result of their injury. (…) Road traffic crashes cost most countries 3% of their gross domestic product.” In most of the cases, the crashes are caused by human error and could be avoided.

While the governments are enforcing regulations, the automotive industry is developing more sophisticated Advanced Driver-Assistance Systems (ADAS) to take control of the vehicle in case of danger. ADAS can be defined as the group of electronic systems that assists the drivers in driving and parking functions. Anti-lock braking systems (ABS), traction control, cruise control and automatic braking are some examples of ADAS systems. These ADAS systems require sensors, processors and actuators.

At the same time, the embedded computers workload is rising also because of the autonomous driving trend. These embedded computers are critical, so redundancy and reconfiguration ability are fundamental to ensure mission continuity in case of fault occurrence. This thesis is dedicated to improve the availability of the energy conversion stages that supply those computers.

Other demand from the very competitive automotive market is to offer very flexible and scalable solutions capable to address a wide range of market segments, i.e. being able to adapt to a wide range of computing workloads and consequently the required electrical power. The supply of computer cores is made usually with multiphase converters. Multiphase converters

use parallel topology to offer naturally multiple (redundant) current paths to the load. However, their weakness in terms of availability is due to the use of a centralized converter controller.

NXP Semiconductors is the world leader in power management solutions for the automotive industry. Willing to propose solutions with these two characteristics, redundancy and scalability, NXP Semiconductors started the partnership with the LAPLACE laboratory in a research project leading to this thesis. The track to be studied is the use of distributed control: scalable, reconfigurable, and without Single Point Of Failures (SPOFs); a current topic in the LAPLACE research line.

This chapter will provide an introduction about the NXP safety strategy, the control architectures, an overview on processor's power supplies as well as an overview of the current trend on the processor's market. The end of this chapter will be dedicated to a brief state of the art on voltage regulation, leg current balance and also the generation of interleaved signals.

## I.1. Safety strategy

NXP plan to introduced new safety solutions is shown in Figure I-1. The actual solutions are able to detect and react to a failure. However the reaction is limited, essentially by turning-off the power system and asserting an output signal to, for example, turn-off the communications and prevent non-correct information to be delivered.


*Figure I-1 – NXP plan to improve safety. [1]*

The context of this work is to go further and propose a processor power supply with features able to reach the fail operational status, where a reconfiguration is performed in case of failure to keep the system operational and guarantee the mission continuity. Differently of the common sense, the different features making a system can have different safety goals, such as supplying correctly a processor. It is not necessary to all the features to be fail operational to classify a system as fail operational. This work will focus only on the control structure of the microprocessor power supply.

## I.2. Control architectures

As computer networks and electric grids can have multiple architectures, the same is applicable to control systems. When multiple control elements are put together in order to achieve a common task, the control architecture can be conceived in multiple different ways. Those control architectures can be summarized in three different categories: centralized, decentralized and distributed. These different architectures are illustrated in Figure I-2.

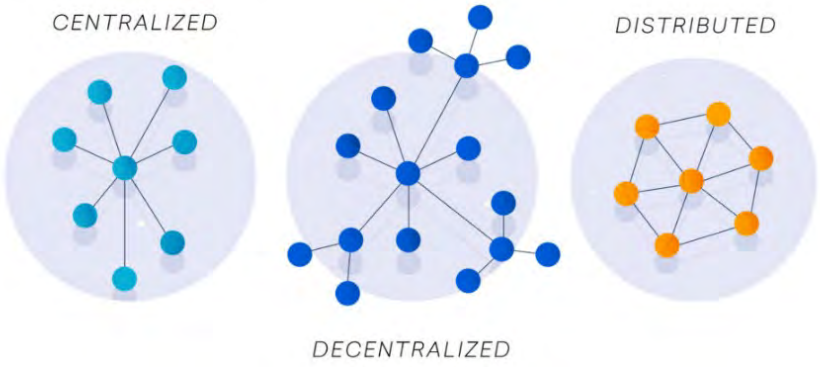



*Figure I-2 – Network architectures: centralized, decentralized and distributed. [2]*

The centralized approach is based on a leader element and many followers. They are the most common, being easy to design and fast to develop, scalable but prone to failures, mainly because of the dependent failure with root cause in the leader.

The decentralized approach is based on  a nest with many hubs where the followers are connected. They are less prone to failures than a centralized architecture, but the hubs still being cause of dependent failures.

In distributed approach, all elements are in the same rank, multiple connections are used and hubs are avoided. As a result, no Single Point Of Failure (SPOF) is present, eliminating completely dependent failure. The circular chain of communications is an example of scalable and distributed architecture.

## I.3. Power management

As the processors evolve, its power management functions evolve as well. As the technological node reduces and workload increases, lower voltages and higher currents are required. Some techniques to minimize the processor power dissipation are described in the Texas Instruments application report "*Adaptive (Dynamic) Voltage (Frequency) Scaling – Motivation and Implementation*" [3].

Usually, to a given technological node, the processor performance increases with its supply voltage level, meaning faster clock signals can be applied and higher workload can be

handled. Due to process variations, some processors can handle faster clocks than others at the same voltage, but its current and power dissipation are higher.

Adaptive Voltage Scaling (AVS) and Dynamic Voltage Scaling (DVS) were introduced to optimize the power consumption to each specific device. AVS adjusts the supply voltage for process and aging, while the DVS adjusts for temperature. Figure I-3 shows how the supply voltage of different devices (weak, nominal and strong) is adjusted to get the same power consumption and handle the same workload. The power dissipation is equalized by adjusting the supply voltage and, as a result, no more than necessary electrical power is used.

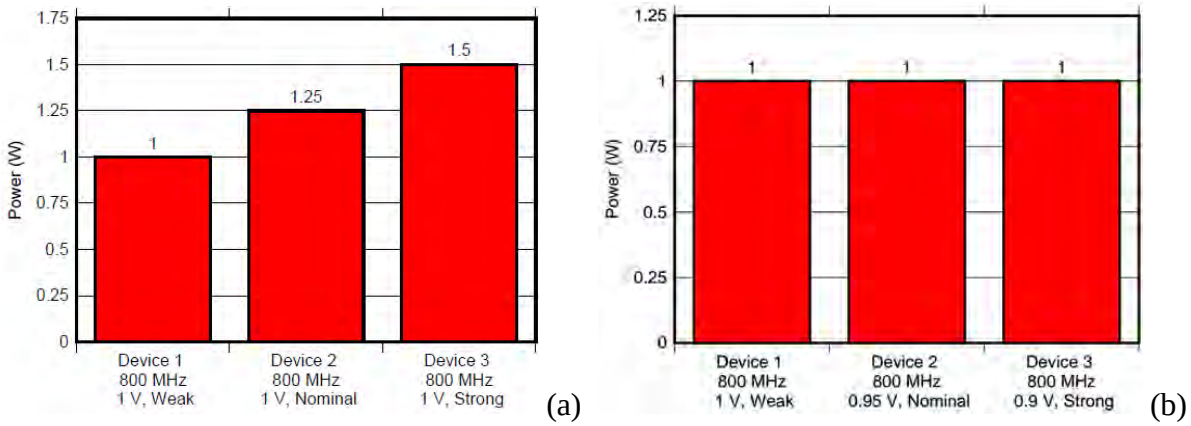



*Figure I-3 – AVS, power dissipation: a) before and b) after AVS adjustment. [3].*

When a different workload (clock) is required, the dependency between voltage supply and workload can be used to change the processor's performance. The processor supply voltage (and power dissipation) can be adjusted to ensure correct operation. This technique is called Dynamic Frequency Voltage Scaling (DVFS), where the supply voltage is adjusted on-the-fly to correspond to the clock frequency (workload) required. Figure I-4 (a) shows the power dissipation plot for different frequencies and (b) the energy required per instruction. A minimum can be seen in (b), being the optimal point for the processor operation, i.e. the lower energy per instruction rate. This point indicates where the processors work with optimal power consumption.

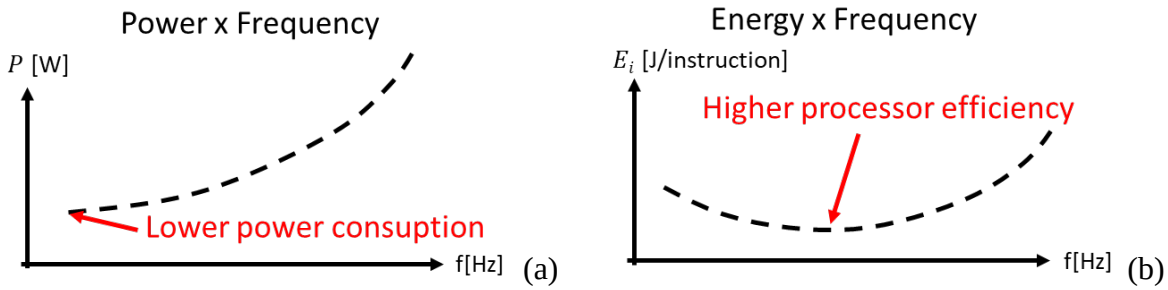



*Figure I-4 – DVFS: a) power consumption vs. frequency, b) energy per instruction.*

Originally, most of the digital circuit power consumption was related with gate switching, i.e. clock frequency. However, process evolution and parameter optimization led to a significant increase of leakage power, i.e. power consumption not related to the clock, responsible for around 50% of the power consumption since 45 nm process, as shown in Figure I-5.

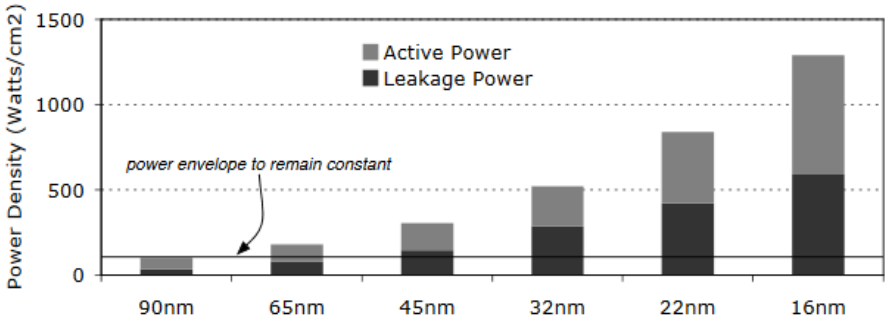



*Figure I-5 – Evolution of active and leakage power densities with node technology. Source: Intel.*

As processor leakage power became an issue, fast cycles of "processing then rest" were introduced, thanks to clock modulation, to operate always at the more efficient point. During the rest time (idle), some processors regions are unsupplied to avoid leakage. Examples of power consumption as a function of active time can be seen in Figure I-6, where total energy consumption in case (b) is smaller than in case (a) for a same workload (not in scale).

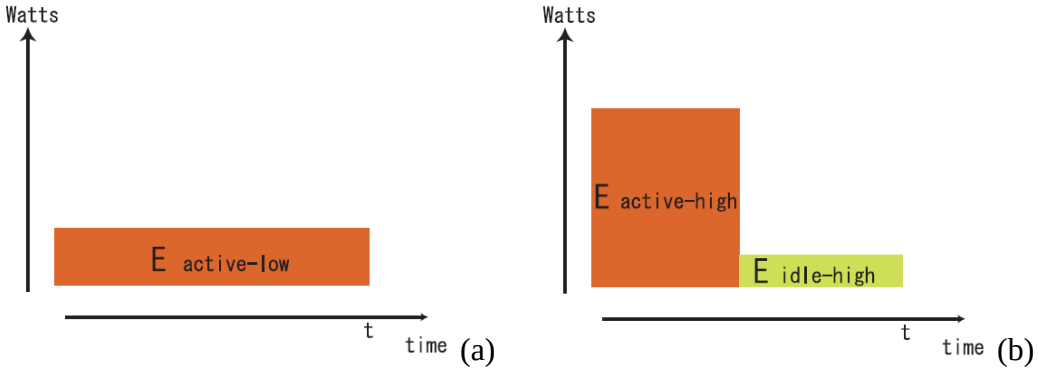



*Figure I-6 – Clock modulation: a) 100% active-low, b) 50% active high + 50% idle. [4]*

The combination of DVFS and clock modulation result in a wide variety of possible combinations. These combinations are mapped and the processor is able to choose the best configuration to minimize the power consumption based on the workload, as shown in Figure I-7.

When using clock modulation, the power consumption is no more constant, as seen in Figure I-6. This induces to the power supply very fast load transients, i.e. current transients. To handle this, a predictive technique called Adaptive Voltage Positioning (AVP) was introduced. Without AVP, the converter tries always to regulate the voltage in the middle of the voltage tolerance range to accommodate overshoots and undershoots, as shown in Figure I-8.

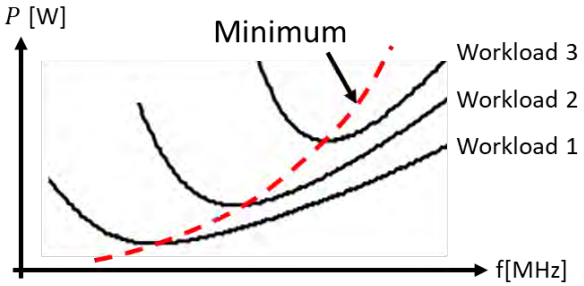



*Figure I-7 – DVFS and clock modulation. Best efficiency mapping for different workloads.*

The AVP technique consists basically in adjusting the load voltage based on the current required. This dependency is also called Load Line (LL) because it is equivalent to a virtual resistance connecting an ideal voltage source (reference) with the load. The AVP allows to reduce both the output filter capacitor by a factor two and the power consumption.

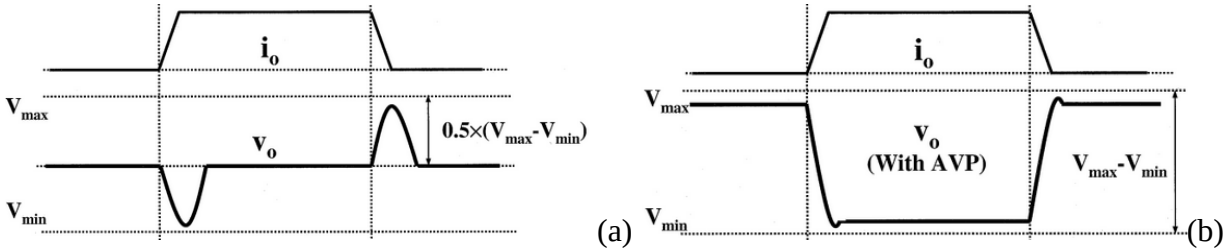



*Figure I-8 – Load regulation, output voltage and current waveforms : a) without AVP, b) with AVP. [5]*

Figure I-9 shows all these techniques combined in a same chart. With AVS, all processor operation points stay on the same iso-power line to a given frequency and workload. The DVFS allows the processor to change between iso-power lines. And finally, AVP allows the processor to stay within limits during the clock modulation fast transients.

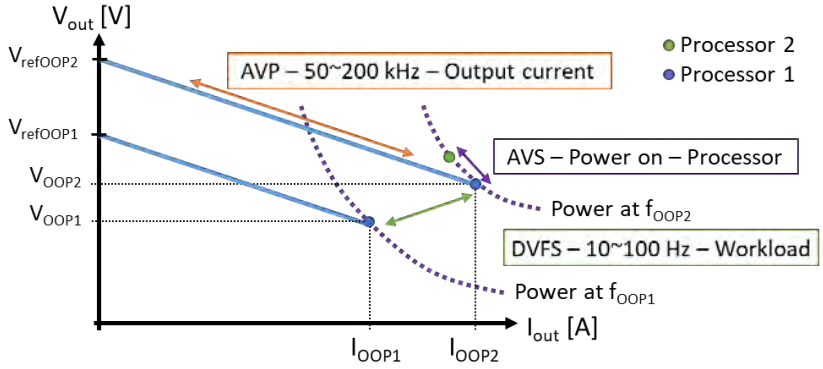



*Figure I-9 – Combined impact of AVS, DVFS and AVP techniques in the processor supply chart.*

A simplified scheme with all these techniques is shown in Figure I-10. On the processors side, AVS takes into account the process variations, temperature and aging to choose the most adapted voltage reference level. Additionally, the clock modulation and DVFS will then adjust the processor voltage and operation to the workload. The Voltage Regulator Module (VRM) refers to the Point of Load (PoL) regulator used to supply processors. The VRM will apply AVP to improve transients and reduce even further processor power consumption.

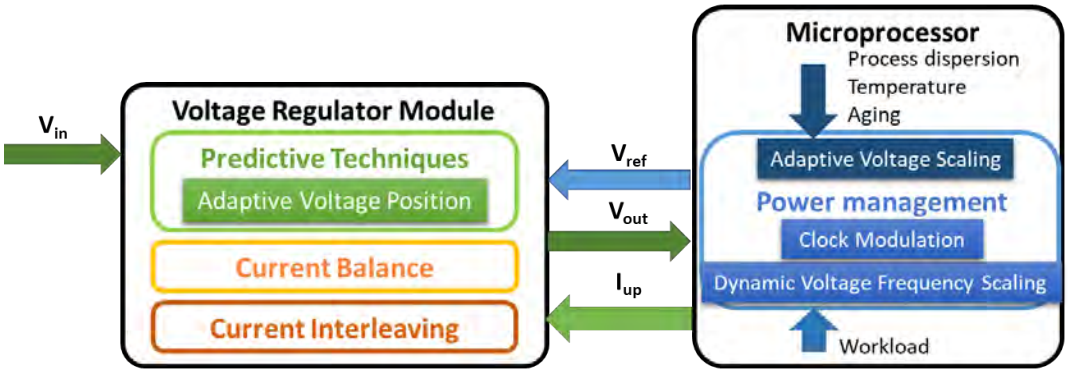



*Figure I-10 – Simplified scheme of VRM and processor control techniques.*

Multiphase Buck converters are usually chosen due to the ability to deliver high current and being able to handle fast transients. The scheme of a Buck converter with 3 legs is shown in Figure I-11 (a). The converter control is composed of three main features: output voltage regulation, leg current balance and PWM leg control signal interleaving. The interleaving consists in equally spacing the switching commands on each leg (e.g. ON-time) to obtain a higher fundamental frequency in the combined inductor current at the output, as shown in the waveforms of Figure I-11 (b).

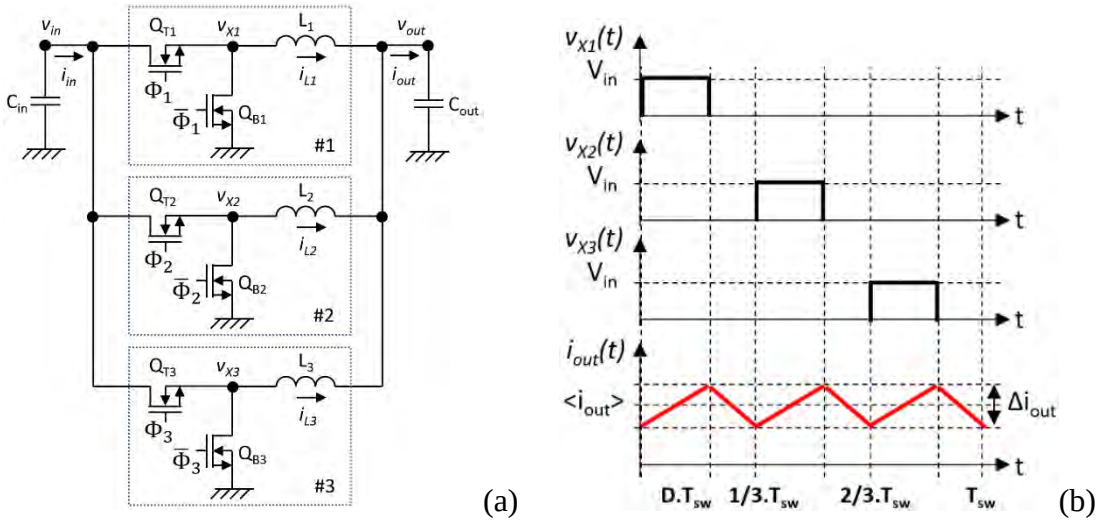



*Figure I-11 – Multiphase Buck converter (3 legs): a) topology, b) signal waveforms.*

Once multicore processors were introduced, the power management become trickier because each core may require a different optimal supply voltage based on its own workload. For this reason, Integrated Voltage Regulators (IVR) were introduced. IVRs are Switching Mode Power Supplies (SMPS) integrated within the processors. In some cases, multiple IVR are integrated and each one is dedicated to supply a processor core individually. Instead of each core using the highest required core voltage, each core has only a minimum voltage overhead and thus the wasted energy is the minimum possible, as shown in Figure I-12.

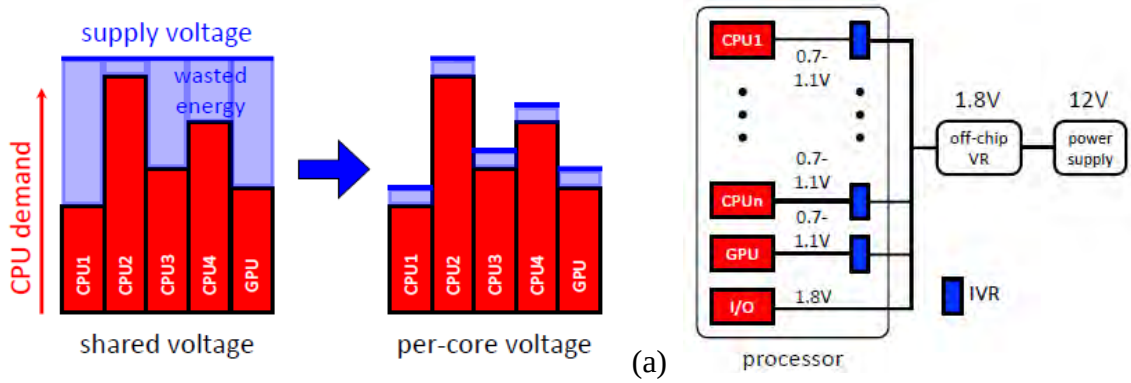



*Figure I-12 – FIVR: a) supply principle using either integrated LDO or IVR, b) supply scheme. [6, p.]*

These approach was introduced in the Intel Core i7-4700MQ Processor, shown in Figure I-13 (a), in a single die approach, called Fully Integrated Voltage Regulator (FIVR). Each domain highlighted in (d) is supplied by a dedicated converter. The converter topology used is a 3-level flying capacitor multiphase converter (c) with inductors integrated in the package (b). The inductors are very small, an astonishing 58 integrated inductor pattern can be count, operating as 2, 4, 6 or 8 multiphase converters can be observed in (e). The converter specification is shown in (f).

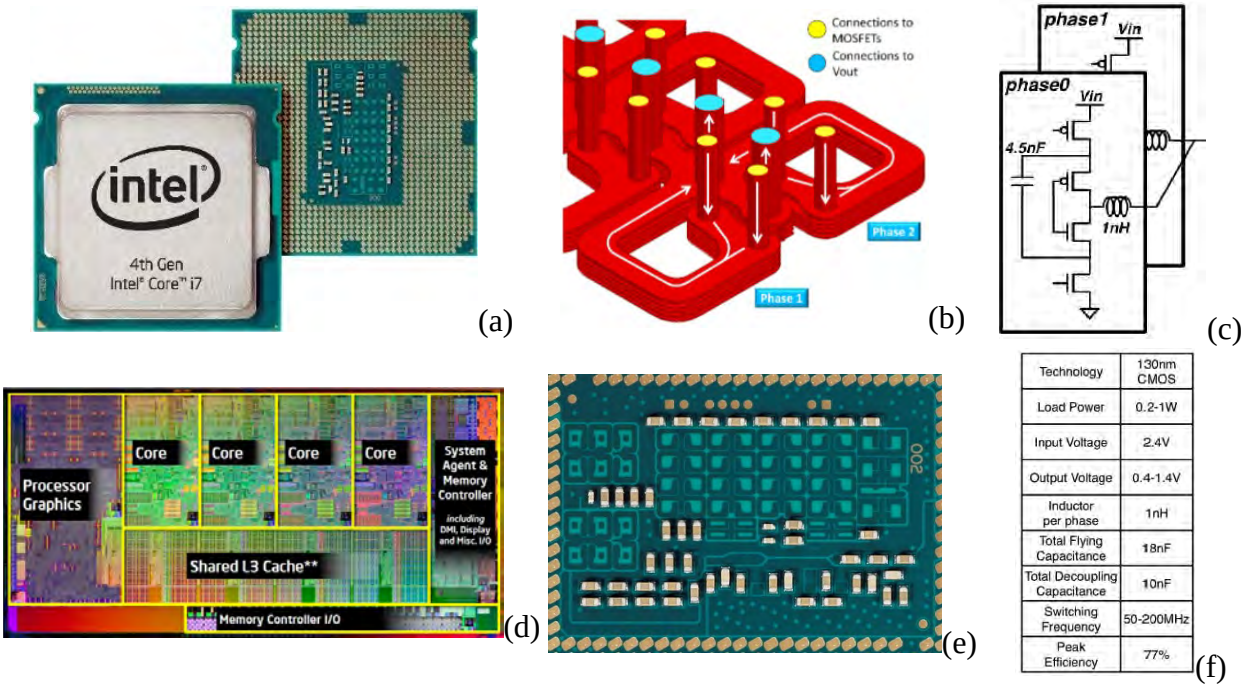



*Figure I-13 – Intel Core i7-4700MQ Processor: a) package, b) integrated inductors, c) converter topology, d) processor die, e) integrated inductors and capacitors view, f) converter specification. [7]*

Since the introduction of processors to the consumer market, the number of phases increases. This tendency is mainly due to the increase of the delivered power as the supply voltage within the processor technological node is reduced, resulting in higher current. With the FIVR introduction and its ability locally to divide the voltage by two and double the current,

the voltage delivered by the upstream VRM took a step back and increased, while the phase number stabilized.

Numerous power supply topologies were introduced and abandoned, such VRMs with coupled inductors, as well as the FIVR which was not kept in the following generation. However, Intel may reintroduce it as technology evolves or different trade-offs will appear. Figure I-14 shows some striking points of the VRM evolution with the number of phases associated. The number of phases should remain at these level (around 12) in the processor market as more efficient processors are introduced and thermal management issues are solved.

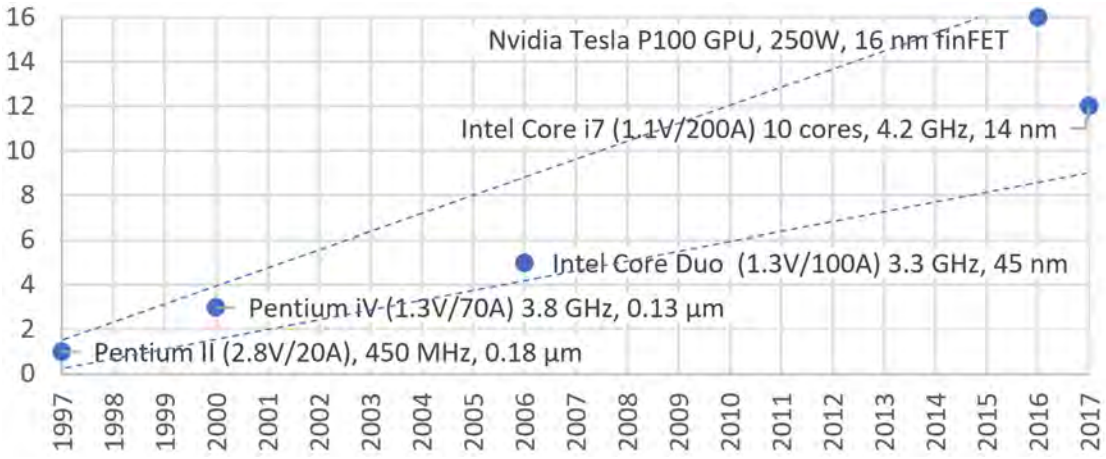



*Figure I-14 – Increasing number of phases tendency.*

In the recent years, the artificial intelligence boom occurred. To improve performances, these applications prefer specialized circuits like GPUs and specialized Neural Network Processors (NNP). As a result, the processor's die sizes increased as well as their power consumption requirements. A die size comparison can be seen in Figure I-15.

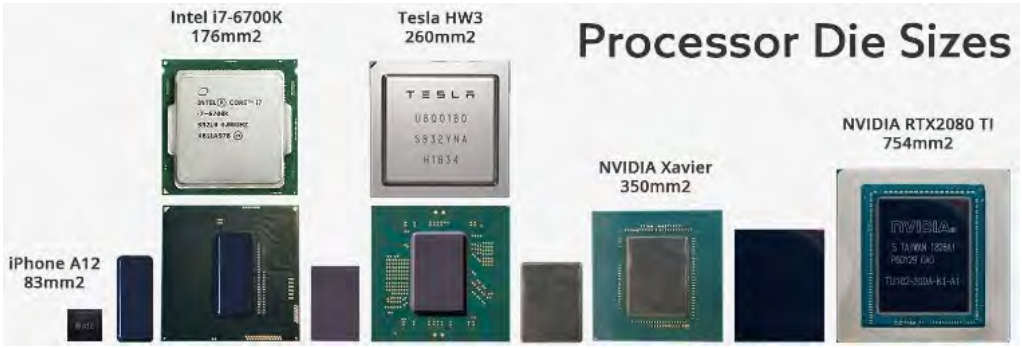
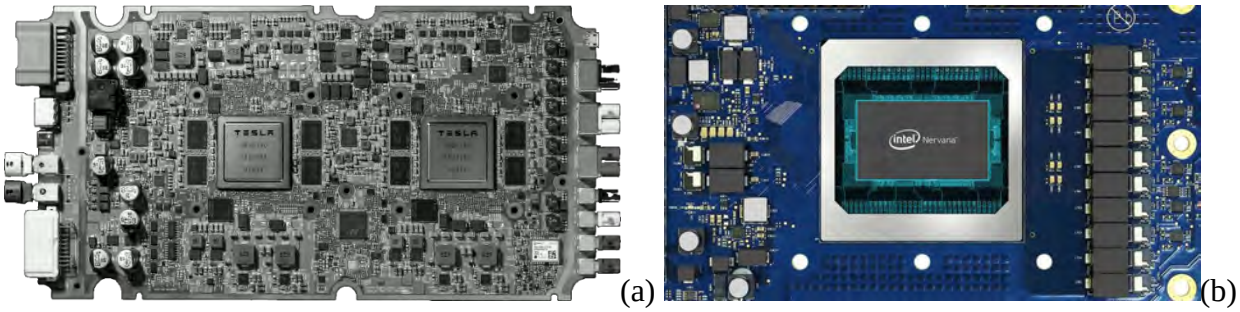



*Figure I-15 – Processor's die size comparison. [8]*

Tesla's HW3 self-driving car computer deployed in Tesla Model 3, shown in Figure I-16 (a), is dedicated to autonomy level between 2 and 3. Its electronic board is composed by two processing units, each one supplied by a 2 phases Buck converter. The processors are very efficient, so only two standard power stages are sufficient. It should be noted a higher number of phases would increase redundancy and reduce the volume.

Intel and Nvidia introduced more big chips specialized in neural network processing for training neural networks and potentially accomplish autonomous driving level 5. These processors have huge size and very high power consumption. A 12-phase power supply can be seen in the right hand side of Intel Nervana NNP board, shown in Figure I-16 (b). This huge processor size induces drawbacks related to thermal management and reliability, what may raise concerns in the automotive industry.



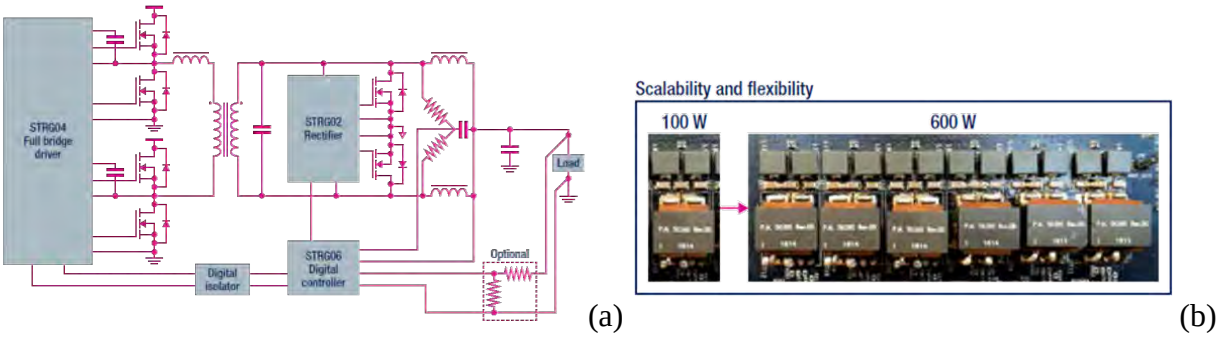

(a) (b)

*Figure I-16 – a) Tesla's HW3 self-driving (level 2/3) car computer, b) Intel Nervana NNP*

Aiming to reduce the power conversion losses, processors can be supplied with direct conversion from 48V without intermediate rails. This solution was first introduced in datacenter application where the amount of converted power is very high, but it can also be used in automotive applications as 48V battery lines are available in some hybrid vehicle topologies.

The most common approach is based on isolated solutions, where the high conversion ratio is achieved thanks to a transformer. To improve scalability and keep redundancy, these approaches use as well multiphase solutions.

Figure I-17 (a) shows one ST semiconductors solution based on a Full-Bridge commutation cell at the primary, a resonant circuit and a current doubler at the secondary, and (b) shows its scalability up to 6 phases.

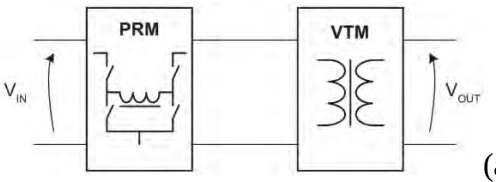



(a) (b)

*Figure I-17 - ST semiconductors 48V direct conversion approach: a) topology, b) multiphase operation.*

Vicor proposed a disruptive solution where multiple transformers, transistors and drivers are integrated together. Vicor solution is also unique because no feedback is present in the transformer unit, i.e. it works in open loop. The output voltage is regulated by varying the transformer's input voltage with a Buck-Boost converter. The two stages are called "PRMs (Pre

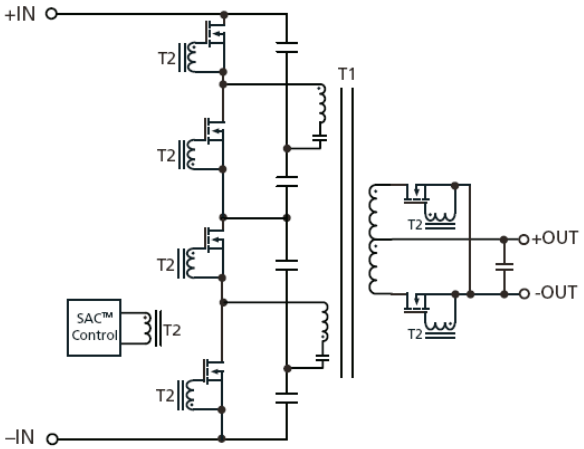
Regulation Modules) or Buck-Boost converter and VTMs (Voltage Transformation Modules) or current multipliers at the point of load". The VTMs are made up of numerous resonant converters, called by Vicor as Sine Amplitude Converter (SAC$^{TM}$), as shown in Figure I-18. Their inputs are connected in series while theirs outputs are connected in parallel, obtaining then a current multiplication effect.




(a)

Fully resonant.
Zero Voltage Switching (ZVS).
Zero Current Switching (ZCS).
Efficiencies of 92% to 98%.
Power from 150 W to 1 kW.
Switching frequency up to1.7 MHz.

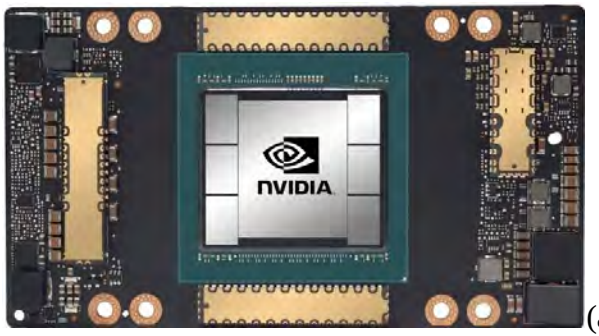
(b)



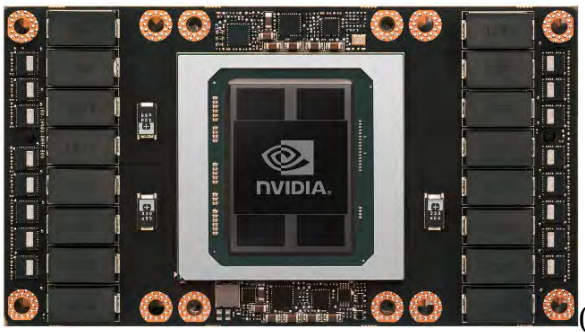

(c)

*Figure I-18 – Vicor a) Factorized Power Architecture block diagram, b) typical SAC specifications, c) SAC/VTM topology. Source: Vicor.*

Vicor solution is already being used by Nvidia in its most recent A100 Tensor Core data center solution, shown in Figure I-19 (a), where 4 VTMs (brass color chip) can be seen, while Nvidia Tesla P100 solution (b) uses a 4+4+8 multiphase power supply. The A100 board has a maximum Total Power Dissipation (TPD) of 400W.




(a)




(b)

*Figure I-19 – Nvidia GPU boards: a) A100 Tensor Core, b) Tesla P100.*

In contrast with the multiphase solution, the VTM's one seems to present multiple SPOF. The multiphase Buck converter intrinsic redundant characteristic contribute to obtain high reliability. For that reason, the multiphase is still the most adapted solution for the automotive industry, where the operating conditions, lifetime and cost requirements are tougher than in datacenter applications.

To improve even more the multiphase Buck reliability, the fail operational status has to be reached by applying a control architecture without SPOFs and able to reconfigure in case of

fault. For this reason, the next section will introduce the state-of-the-art of the decentralized and distributed control methods applied for multiphase Buck converters.

## I.4. State of the art

This state of the art gives an overview of the decentralized and distributed control techniques developed for the multiphase Buck converters. The state of the art is divided in two distinct sections. One will be dedicated to a few examples of voltage regulation techniques combined with the leg current balance. The second will be dedicated to a deep analysis and classification of the carrier interleaving techniques.

The state of the art will focus in techniques where all elements have equal importance, so called democratic, master-less, decentralized, or distributed. These solutions are preferred because of modularity and present no controller SPOF.

### I.4.1. Voltage regulation and current balance

The multiphase Buck converter voltage regulation and current balance can be done in multiple different ways. This state-of-the-art will highlight only few options. The voltage regulation can be either centralized or distributed in a cooperative way. In most of the cases, the controllers use droop sharing techniques, like associating multiple converters with AVP. The current balance can be done by sharing the average current though a shared wire or by a circular chain of communications. Four examples will be presented to illustrate these four possible combinations.

#### I.4.1.1. Current balance distribution

The first step to distribute the converter controller is to balance the current in a distributed manner, i.e. resulting in a partial distributed system. In these systems, a local adjustment is made to equalize the leg current based on the available information without a central controller intervention.

##### I.4.1.1.1. Shared wire

International rectifier introduce in 2003 a scalable partial distributed approach based on a centralized voltage controller (IR3080) and a multiple phase IC (IR3086). The phase IC is composed of power stages, drivers and controllers able to combine the average current value in a shared wire and adjust it. This sharing technique was patented much earlier in 1988 by K. T. Small and all in “Single Wire Current Phase Paralleling Of Power Supplies” [9] and discussed in [10] by Lin and Chen. It is shown in Figure I-20 (a) for a voltage control mode (top) and for a current control mode (bottom).

#### I.4.1.1.2. Circular chain

An equivalent technique but using a circular chain of communications was proposed by Bolloch and all [11]. It is shown in Figure I-20 (b). In this approach, each leg controller can only access the current information of its own leg and the ones of its close neighbors to adjust the local duty-cycle. Inter-controller communications are made in the circular chain. Even if only the partial information is available, the system is able to balance correctly the leg currents and regulate the output voltage thanks to a centralized voltage controller (providing the D signal).

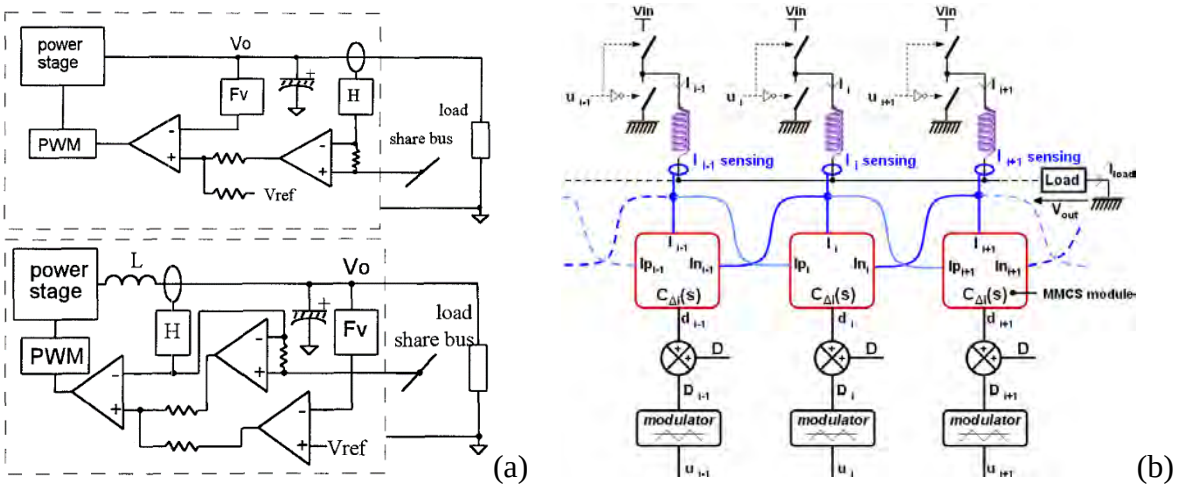



*Figure I-20 – Current balance distribution: a) Shared (single) wire [10], b) Circular chain [11].*

#### I.4.1.2. Voltage regulation distribution

When the voltage regulation is distributed, each leg becomes an independent converter. A converter using a classical PI voltage controller behaves in closed loop like an ideal voltage source. As a result, the legs can no more be connected in parallel because of the concurrent voltage loops, as very high recirculation currents would flow in between then, leading to potential destruction or useless power dissipation.

One solution to connect them together is to allow each converter to behave as a non-ideal voltage source. The converters can be connected together through real resistors, but virtual ones can be emulated by using the AVP technique (load line), resulting in limited recirculation currents with no unnecessary power dissipation. This technique works because the sensed load voltage carries the information of the current that shall be delivered. It is known that this technique has poor current balancing ability, because of mismatches in the voltage references, controller droop gains or load voltage sensors. For that reason, an additional current balancing technique can be added to improve the accuracy of the control system.

#### I.4.1.2.1. Shared wire

To improve the current balancing, a shared wire can be added to either obtain the leg current average value or take the average value of the reference voltages. The method using the average value of the reference voltages was proposed by Zhang and Huang [12], as shown in Figure I-21, where each leg's references $V_{ref}$ are tied together.

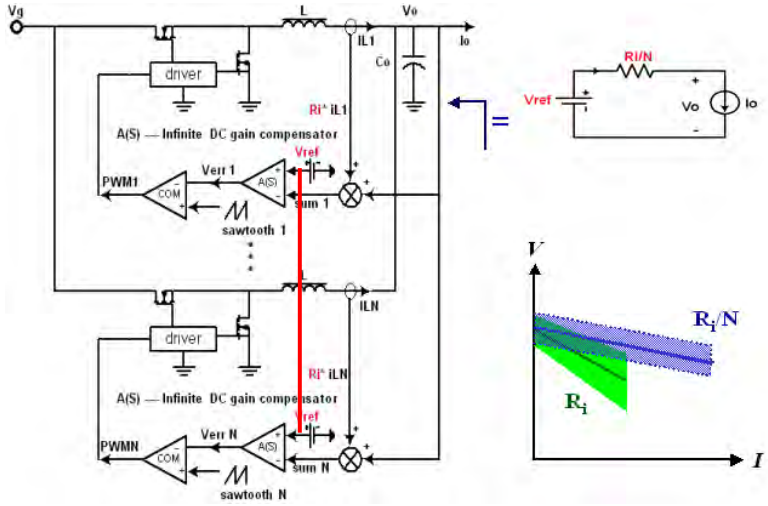



*Figure I-21 – Zhang and Huang Modularized Voltage Regulator with shared wire average voltage reference [12].*

This technique solves only a part of the problem, as the droop gain and the load voltage measurement mismatches cannot be compensated.

Ericson PoL regulators from BMR series (463 to 467) uses the droop technique and they can be associated together in parallel using a leader/followers approach. To balance the current, the leader broadcasts its output current in a digital communication link and the followers adjust their own reference voltages to match the leader current, as shown in Figure I-22 (a) without balance and (b) when balance is enabled. As a result, the leader imposes the converter voltage/current characteristics.

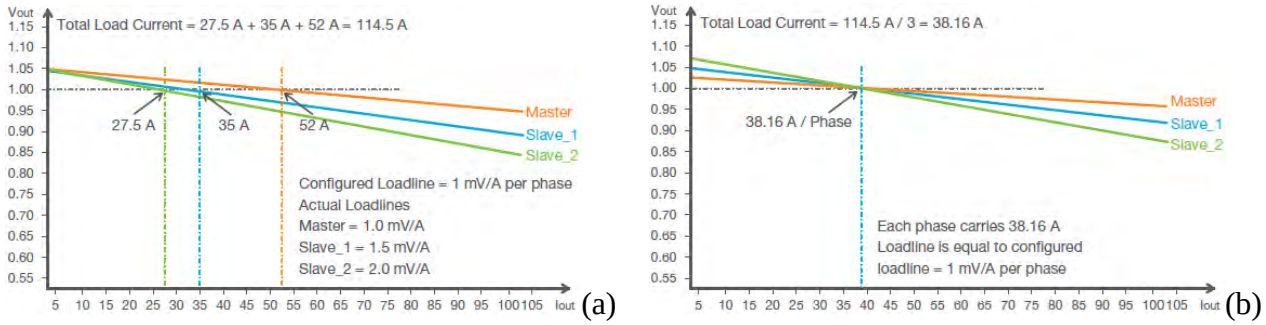



*Figure I-22 – Ericson BMR series POL regulators current balance strategy: a) no balance, b) with balance.*

#### I.4.1.2.2. Circular chain

To avoid SPOF and improve current balance, the association of droop converters with a circular chain current balancing technique was proposed by COUSINEAU in [13]. In each leg, the difference of the local leg current and the adjacent currents is used by the controller to adjust the droop and obtain the same current in all legs, as shown in Figure I-23.

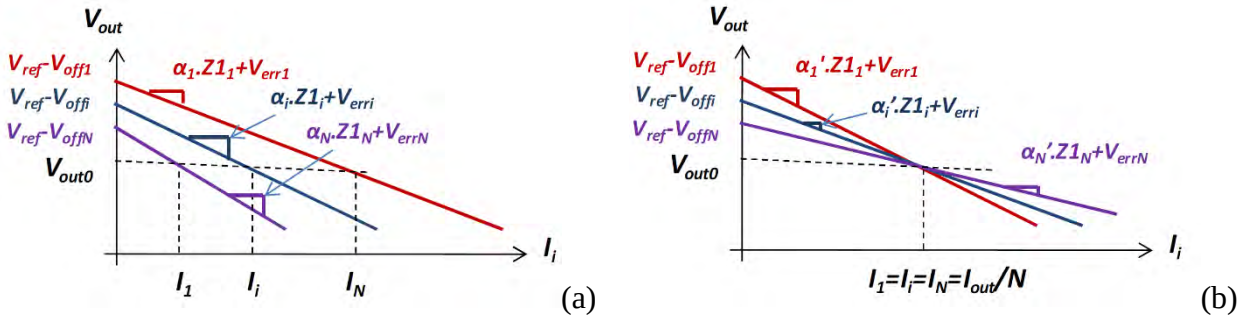



*Figure I-23 – Cousineau droop slope adjustment technique to balance leg currents [13]: a) no balance, b) with balance.*

This technique presents a drawback as the average current appears as a gain in the control loop, so the balance has different performances with different current values.

### I.4.1.3. Voltage regulation and current balance techniques summary

As a conclusion, the droop technique with the circular chain current balancing technique is the most suitable to obtain modularity with no SPOF, as shown in Table I-1, because centralized control and shared wires shall be avoided.

*Table I-1 – Voltage regulation and balance techniques combinations.*

| | | Voltage regulation | |
|---|---|---|---|
| | | Centralized | Distributed |
| Current Balance | Shared wire | Modular [9], [10] | Modular [12] |
| | Circular chain | Modular [11] | Modular / No SPOF [13] |

## I.4.2. Interleaved clock generation

Interleaved converters presented in the literature and available in the market can be classified in two groups.

The first group represents the ones using a centralized controller, called also multiphase controller. The centralized controller is associated with a specified number of switching-cells integrated or not in a power module.

The second group represents the scalable controllers, also called stackable or modular. In this approach, controller and power stage are associated in the same chip. Each chip is a complete converter that can be associated with others to build a multiphase converter.

In both cases, the switching-cell modulator requires interleaved clock signals or interleaved carriers. The interleaved carriers can be, in many cases, obtained from the interleaved clocks. Therefore, in both operation modes, a Multiphase Clock Generator (MCG) is required.

Some interleaving solutions are dedicated exclusively to scalable solutions, such as detecting the switching instant, interleaving bus, reducing the output subharmonic oscillation. Others are adaptations of centralized interleaving solutions to scalable operation.

This section presents how are implanted classical centralized MCGs and how they are implanted in the scalable approaches.

#### I.4.2.1. Centralized Multiphase Clock Generators

There are several different ways to generate interleaved clocks. This section will present the most used, such as the ring oscillator, DLL, a clock divider, and others.

The ring oscillator is the simplest way to generate interleaved clocks. It is composed by inverter gates connected in a closed chain. This structure has two main weakness. First, the clock frequency depends on the number of elements and on its delay. Second, it only works with odd numbers of switching-cells and then clock signals.

A Delay Locked Loop (DLL) is able to control the clock frequency through a feedback loop and generate the exact number of clocks required. It is composed by a Voltage Controlled Delay Loop (VCDL) and a phase/frequency feedback. The VCDL is an association of controlled delay cells. Each delay cell is associated with an interleaved clock signal. The phase/frequency feedback is composed by a Phase Detector (PD), a Charge Pump (CP) and a Loop Filter (capacitor). A DLL example is shown in Figure I-24.

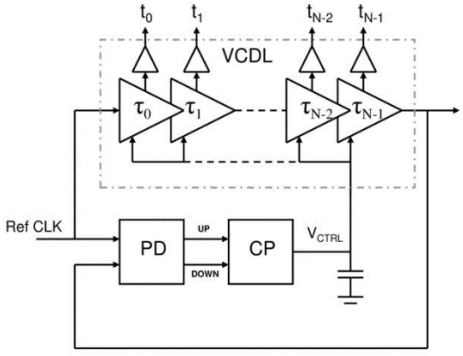
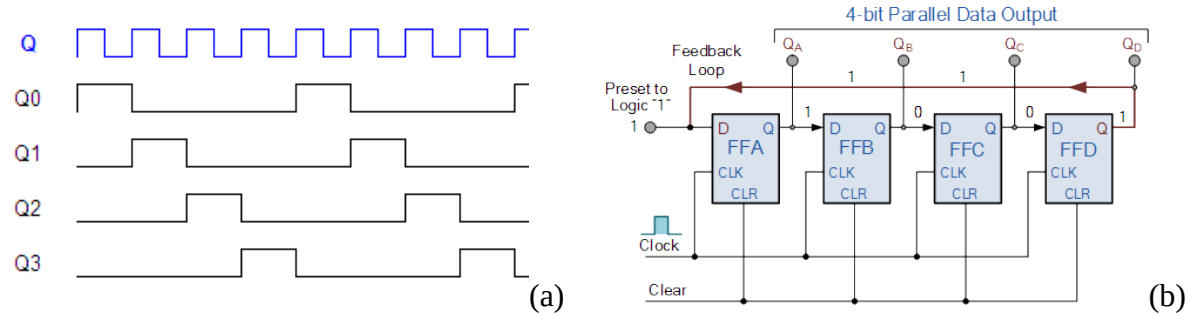



*Figure I-24 – DLL circuit example. [14]*

Interleaved clocks can also be obtained through a high frequency clock and a phase splitter, i.e. a state machine equivalent to a clock divider. The phase splitter has one clock input and several outputs. The input frequency is normally the product of the output clock frequency

with the number of clock signals required. A pulse is sent through each output in a sequential manner, synchronized to each period of the input clock. It can be implanted using a shift register or a counter with a decoder, such as the one shown in Figure I-25.




(a) (b)

*Figure I-25 – Phase splitter: a) time diagram, b) scheme. [15]*

These techniques were also described and used in scalable converters. They will not be presented necessarily in this document. The reconfiguration ability will be discussed later.

#### I.4.2.2. Master-Slave Clock Generators

The leader-followers techniques have at least an element (the leader) that works in a different manner regarding to the other devices (the followers).

##### I.4.2.2.1. Voltage Controlled Delay Loop

The use of a ring oscillator was described in a patent by Hendrix and all in [16]. It shows an odd number of converters using a ring configuration to achieve interleaving. The reconfiguration is an issue in this approach because two converters have to be bypassed each time to avoid the oscillator from stopping.

Linear Technologies introduced in 1999 the PolyPhase™ trend mark [17]. The interleaving technique is based on a clock signal being transmitted in an open daisy chain connections. The elements are cascaded and each one sends a clock signal to the next in the chain with a delay. The delay between input and output clocks is selected through an input "PHMODE" in each element. It is suitable for 2-, 3-, 4-, 6- and 12-phase interleaved operation. Some interleaved applications of the PolyPhase™ module LTM4636-1 datasheet is shown in Figure I-26. This implementation is not suitable to reconfiguration during operation because the delay value is chosen by hardware and only some phase-delay values are possible.

KOHAMA and all introduced in [18] uses a similar scalable interleaving technique based on a Voltage Controlled Delay Loop (VCDL) as shown in Figure I-27. The delay value is shared through a shared wire and its value is automatically adjusted based on the number of active modules, as the delay control voltage $v_R$ is dependent on the number of connected slaves.

Reconfiguration is very simple: the slave local resistor can be disconnected and the delay bypassed. Zhang introduced in [19] a similar VCDL system with improved delay computation.

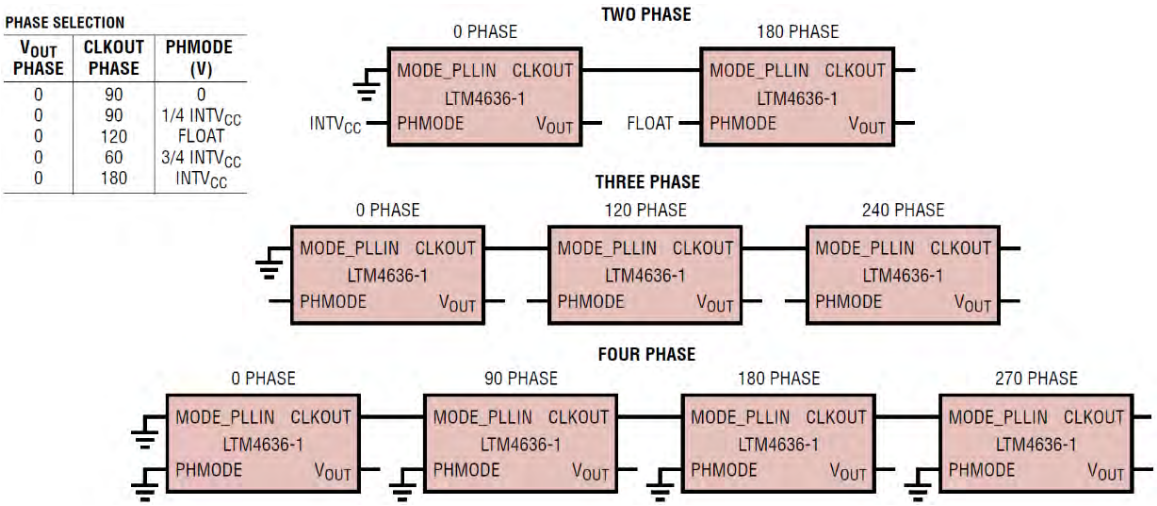



*Figure I-26 – LTM4636-1 datasheet « Figure 4. Phase Selection Examples » extract.*

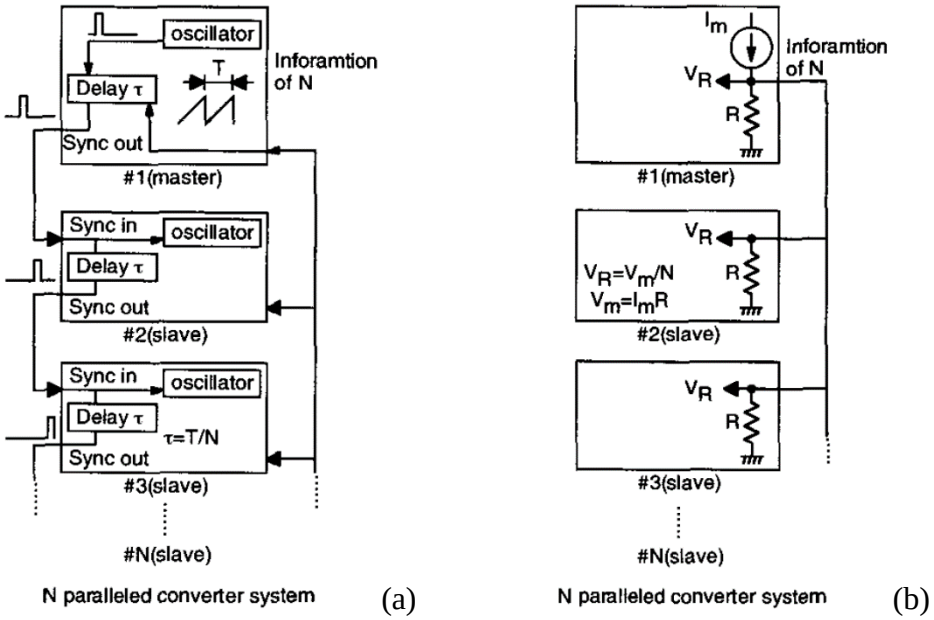



*Figure I-27 – KOHAMA and all interleaving technique [18]: a) connections, b) delay calculation.*

The Renesas ISL8018 uses a similar but quite specific approach. The SYNCIN pin of the $N^{th}$ module (with $N$ the number of legs) has a detection threshold equal to 0.9V, where the rising edge triggers the converter ON pulse. The SYNCHOUT pin of the $N-1^{th}$ module sources a current pulse $I_{SYNC}$, starting at every clock cycle. The current source is turned off when the voltage reaches 1V and the capacitor is discharged to restart a new cycle. The phase-delay is set by attaching a capacitor across SYNCIN/SYNCHOUT to GROUND, setting the slew rate. The waveforms are shown in Figure I-28. This approach uses only two connections, but it does not allow reconfiguration as all parameters are constant.

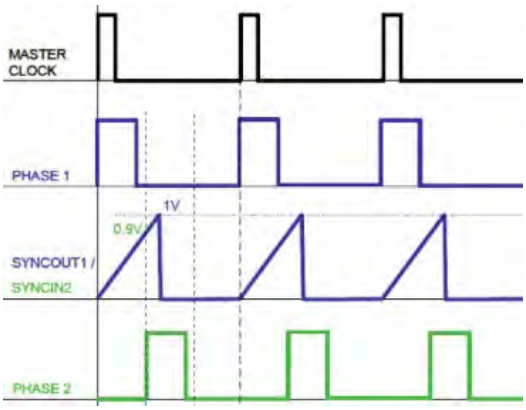



*Figure I-28 – Renesas ISL8018 interleaving technique.*

As a conclusion, these systems operate in open-loop, differently than a DLL, then all delays are not necessarily equal. As a result, the phases may not be precisely interleaved, also due to the cumulative errors.

#### I.4.2.2.2. Global Reference

International Rectifiers introduced in [20] the XPhase$^{TM}$ series, including the control IC IR3080 and the phase IC IR3086, shown in Figure I-29. In this partial decentralized application, the interleaving technique is based on a synchronization signal being transmitted by the control IC to all phase ICs, in this case, a triangular signal. Each phase ICs uses a local voltage divider and a comparator to generate the local interleaved High-Side turn-on signal. It is suitable for interleaved operation on, theoretically, any number of phases, but not for reconfiguration.

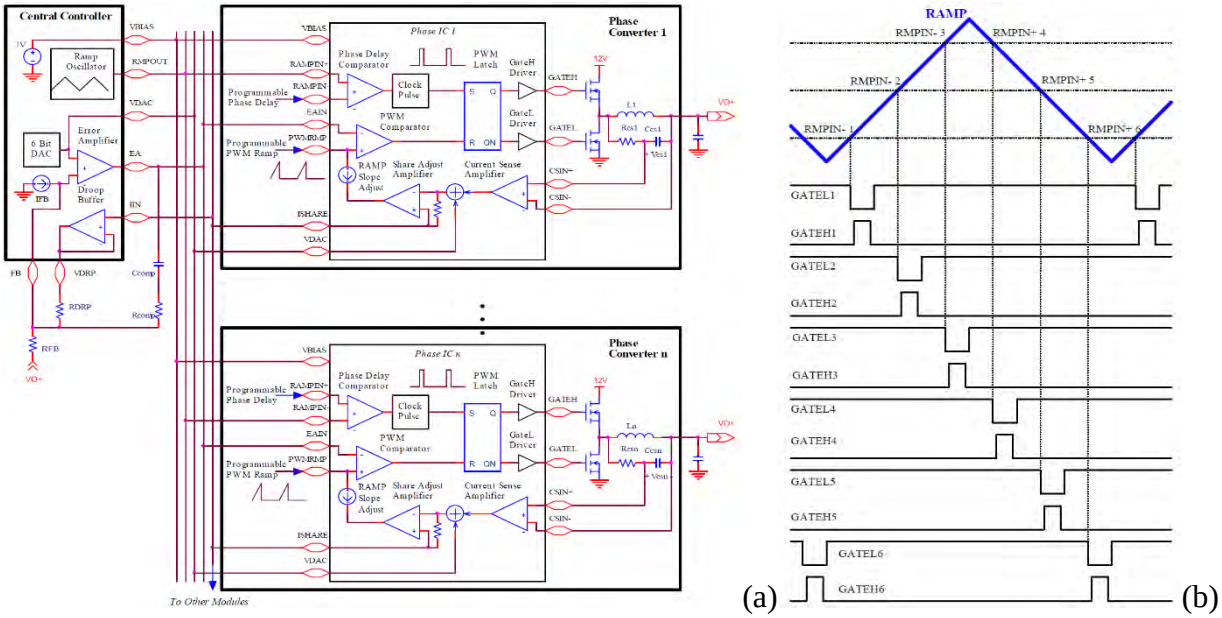



*Figure I-29 – IR XPhase$^{TM}$ global reference technique [20]: a) Scheme, b) Reference ramp and synchronized PWM signals.*

Analog Device LTC3310S and Maxim MAX8686 uses a similar scalable interleaving technique up to four and eight phases, respectively, but the synchronization is made with a

digital clock signal instead of the analogue triangular signal. Texas Instruments TPS543C20 requires only one resistor to set the phase-delay, but can only operate with two phases. These approaches are not suitable for reconfiguration because the phase-delay is chosen by hardware.

The modules family BMR46x from Ericson, LGA80D series from ARTESYN, and ISL8272M from Renesas use a shared clock signal for synchronization. The phase-delay selection is made by software using a digital communication link. Reconfiguration can be made during operation by the master controller. A limited number of phase-delays are possible, e.g. BMR462-466 are limited to 16 possible values (22.5° steps), while BMR461 products support 128 values (2.8° steps).

GRÉGOIRE uses in [21] a circular-chain of communications and a local controllers to compute the local phase-delay, as shown in Figure I-30 (a). Each local controller has a feedback loop to position automatically the local phase-delay in between the neighbors' ones. Interleaving is achieved without a master controller. A digital sawtooth signal, i.e. a counter output, is used for synchronization. GATEAU implanted in [22] a similar technique but using just a clock signal to synchronize the different carrier generators, as shown in Figure I-30 (b). These systems can be easily reconfigured by bypassing the communication links of the removed module, although the synchronization line still being a single point of failure.

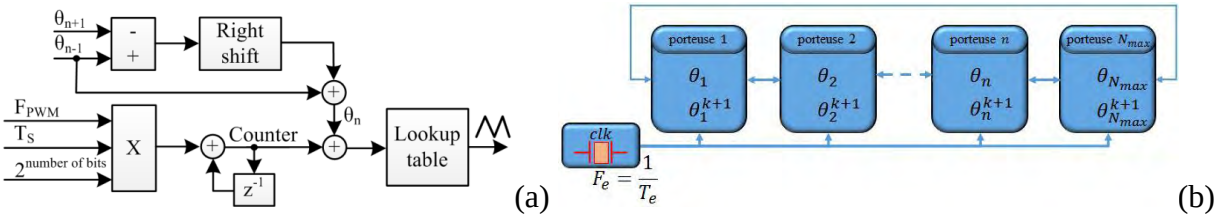



*Figure I-30 – Global reference digital approach with local controller: a) GRÉGOIRE shared ramp (Counter) and local controller [21], b) GATEAU shared clock and local controllers [22].*

#### I.4.2.2.3. Phase Splitter

To improve the phase-delay accuracy, International Rectifiers introduced the XPhase3$^{TM}$ trend mark, including the control IC IR3500 and the phase IC IR3505. This partial decentralized interleaving technique is similar to a shift register, where each phase IC has a D-type flip-flop element of the shift register. A clock signal at the apparent switching frequency is sent to all modules while a closed daisy chain communication line is used to transmit the High-Side turn-on enable from one phase IC to the next. The interleaving precision is improved because the time base is generated in a single element. The control IC identifies the number of phases during start-up, and it can verify the clock line and daisy chain connections integrity during operation. Reconfiguration is easy as a phase IC can be bypassed and the clock generator can adjust the apparent frequency.

A similar technique was implanted earlier by Texas Instruments in the stackable controllers TPS40140 and TPS40180. The master modules send a clock signal to all modules at a multiple of the switching frequency to establish a precise time base. However, one clock pulse is missed to indicate the master position and to synchronized all elements, as shown in Figure I-31 (a). Each slave module uses an auxiliary input to configure its pulse synchronization. The synchronization clock is not necessarily at the apparent switching frequency, as some slave positions can be unpopulated. E.g. the TPS40180 has two clock configurations: 6 and 8 times the switching frequency, for 2-, 3-, and 6- phases operation, and for 2-, 4-, and 8- phases operation, respectively, so 5- 7- correctly interleaving cannot be achieved. The leader-followers connections are also different between these two product references. While TPS40180 uses a specific resistor to define the operation mode of each element, TPS40140 uses a resistor ladder of equal resistors, as shown in Figure I-31 (b).

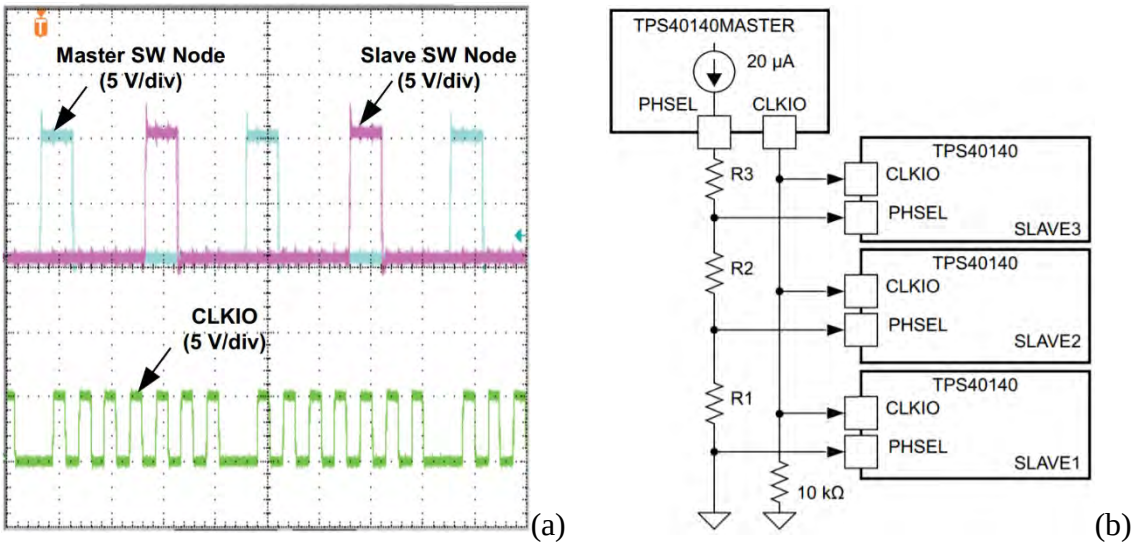



*Figure I-31 – TPS40140 and TPS40180 interleaving approach: a) TPS40180 clock signal and interleaving SW node signals and b) scheme.*

The point of connection on the resistor ladder define the operation mode and allows the leader to identify the number of followers connected. Each TPS40140 device has two phases controlled in phase opposition, and up to 4 modules can be connected together (8 phases properly interleaved). TPS40180 supports until 16 phases. This architecture is not suitable for reconfiguration because of the resistor configuration. A reconfiguration can be made by bypassing a resistor in the ladder configuration (patent pending, application number 20305395.4).

### I.4.2.3. Masterless techniques

The previous techniques require a leader controller to send the clock and the followers roles are well defined by their connections. It introduces SPOFs, limits flexibility and

reconfiguration capabilities. This section will present some masterless interleaving techniques, where all elements are equal and observe the whole system from the same point of view. The solutions compose two main categories: the interleaving bus and the circular chain.

#### I.4.2.3.1. Interleaving bus

The interleaving bus category is a generalization of all techniques that use a commonly sensed shared information to achieve interleaving.

PERREAULT introduce an analogue interleaving bus in [23] to interleave a multiphase converter, as shown in Figure I-32 (a). In this approach, each module injects a current pulse through the shared wire in phase with its clock. Each module uses a PLL to lock the local clock in between the combined signal from the others modules, as shown by the local scheme in Figure I-32 (b). The PLL couples the different clock generators and the system converges to an interleaved state, independently of the start condition and on the number of elements. In steady state, the interleaving bus voltage should be as constant as possible without subharmonic oscillations. However, the analogue approach may be exposed to mismatch and noise sensitivity issues.

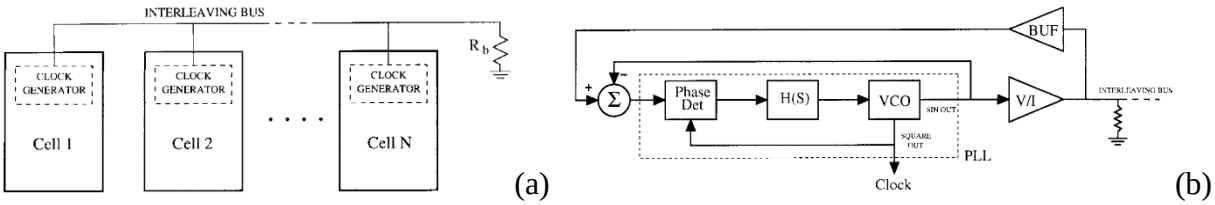



*Figure I-32 – Interleaving bus approach [23]: a) modules interconnections, b) module scheme.*

KUDTONGNGAM introduced in [24] a similar approach, but by introducing a constant current once each two periods, as shown in Figure I-33 (a). It results in discrete voltage levels appearing in the interleaving bus, such as a stair. Then each module can identify the number of active modules and adjust its phase-delay to the previous interleaving bus voltage rising edge, as shown in Figure I-33 (b).

These two techniques are very interesting because they transmit the phase-delay reference and the optimal position in the same wire. Nevertheless, the shared wire is a SPOF and should be avoided. For that reason, techniques using only shared information or local sense emerged. Some of them will be presented here.

#### I.4.2.3.1. Local measurement

FENG and all introduced an automatic interleaving method for a parallel converter in [25] based on the detection of the switching instants. The switching instants were observed over

the output voltage through the high frequencies emitted during the switching-cell commutation. A PLL is implanted similarly as the one in the interleaving bus approach.

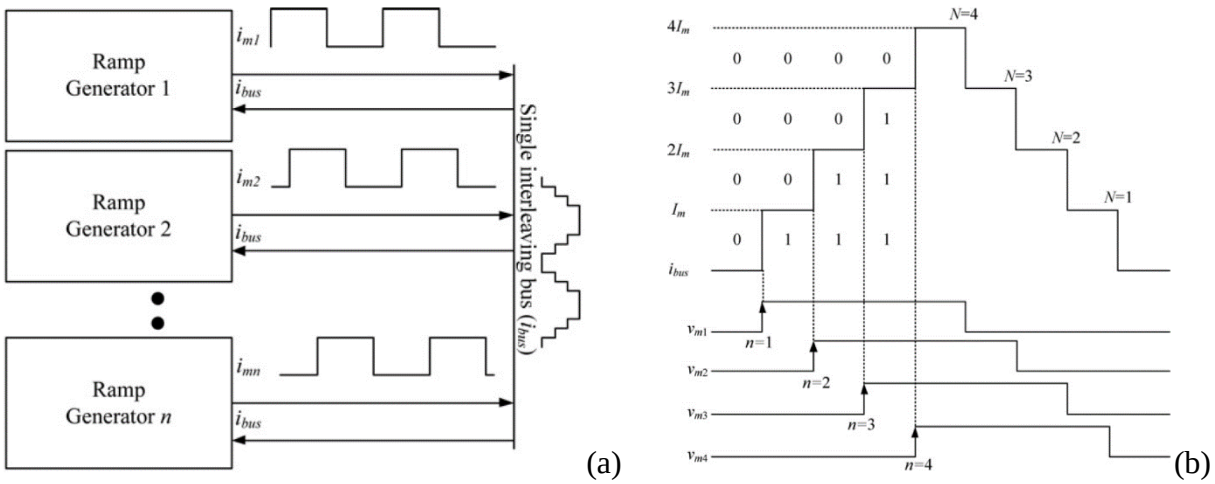



*Figure I-33 – Discrete levels interleaving bus [24]: a) Modules connection scheme, b) Bus voltage principle.*

More recently, DUTTA and all presented a similar approach for a cascaded multilevel DC-AC converter in [26]. Each local controller senses the output current with the combined effect of all switching-cells and adjust the local phase-delay to reduce the sub-harmonic oscillations. The principle scheme is shown in Figure I-34 (a).

SINHA and all presented a decentralized interleaving technique for a parallel converter in [27] where each local controller uses only the local phase current information. The connection scheme is shown in Figure I-34 (b). The interleaving is possible because all phase currents are coupled through the output voltage node.

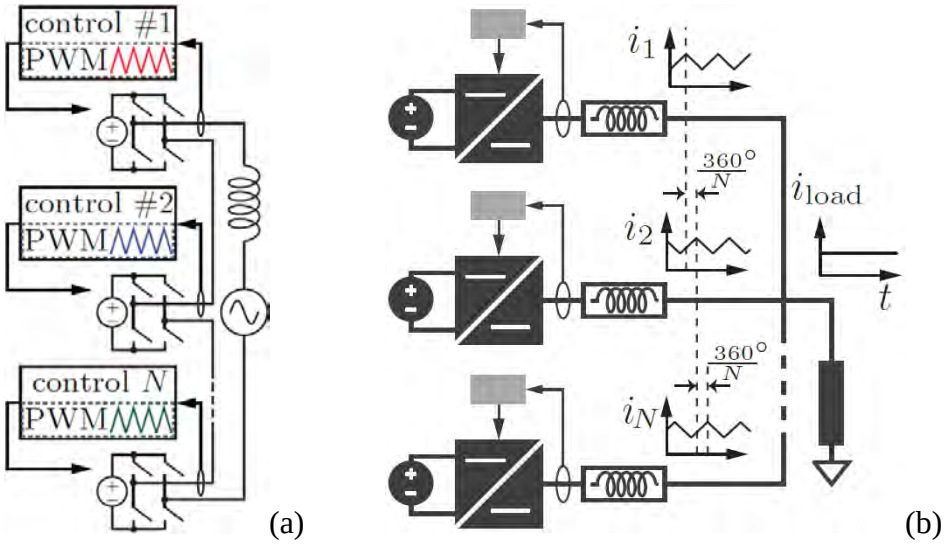



*Figure I-34 – Decentralized interleaving using local measurements: a) Series case [26], b) Parallel case [27].*

It can be noted the technique used by SINHA may have issues related to noise immunity and mismatches because the other elements contribution is measured indirectly. This solution

may also impact the filter design or impose restrictions, as well as the response time, becoming an application issue. This technique may not be suitable for high performance PoL applications.

#### I.4.2.3.2. Circular chain

This category is composed by modules connected in a daisy chain communication architecture. Each element only exchanges a signal with its neighbors to achieve interleaving.

COUSINEAU introduced in [28] an analogue interleaving approach where the elements communicate their triangular carrier, as shown in Figure I-35. In each element, a local controller positions the local triangular carrier “tri” in between the neighbor’s ones “trip” and “trin”, for previous and next, respectively. This approach is modular, does not present SPOF and can reconfigure by bypassing its communications, achieving a new interleaved state for any number of active modules. More recently, this implementation gained more interest and was explored in different ways. Xiao simplified the implementation in [29] using some digital logic.

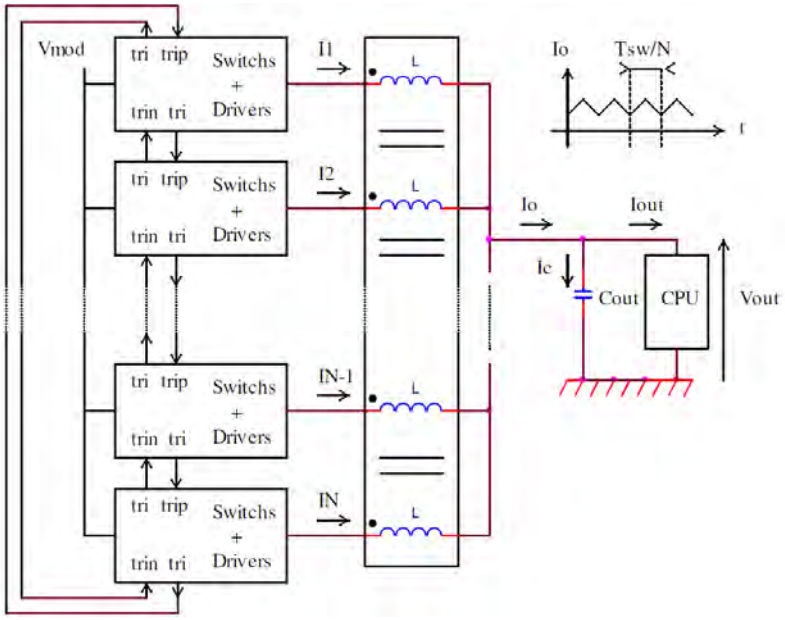



*Figure I-35 – Circular-chain based interleaving technique [28].*

BROADMEADOW and all used in [30] a high speed low latency digital communication link to interleave their converters. Once a period, each module receives a synchronization message from its neighbors, as shown in Figure I-36 with the dotted arrows. A local controller identifies the message time difference, i.e. the error, then position the local carrier in the middle. This technique can present issues during reconfiguration if fast bypass is not available due to the higher communication complexity.

MURRAY introduced in [31] a different technique to interleave converters using a variable frequency hysteretic current-mode control. As shown in Figure I-37, each module receives the neighbors’ gate signals, then compute the average switching period and phase-shift.

Two local controller are required. One adjusts the current ripple to equalize the switching periods, the second adjusts the current peak to obtain a phase-shift and consequently achieve interleaving. This approach has a limitation: it requires the information of the number of active modules *N* to compute the appropriate phase-shift.

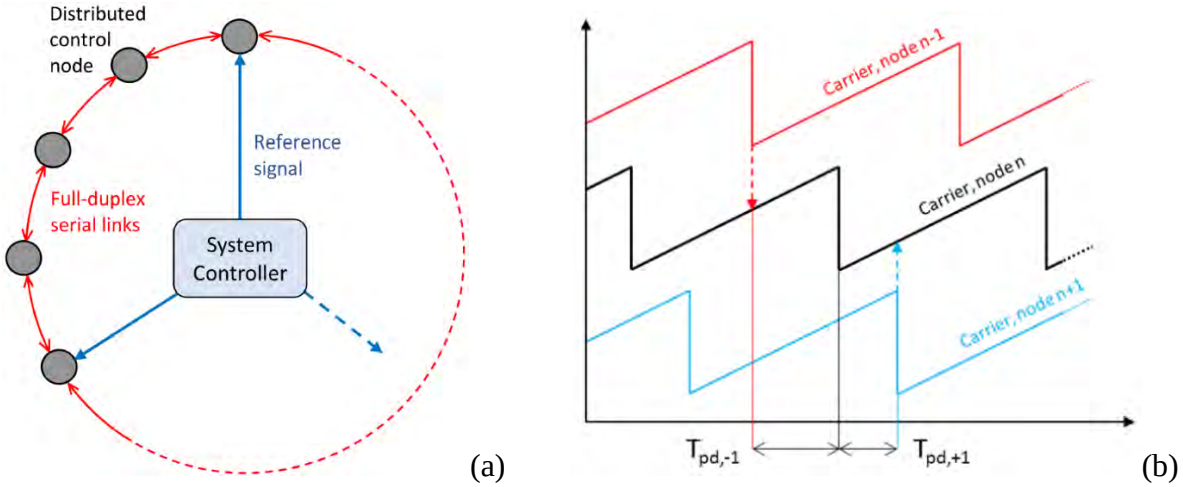



*Figure I-36 – Broadmeadow interleaving technique [30]: a) Simplified block diagram, b) Carrier waveforms, the dotted arrows represents a message.*

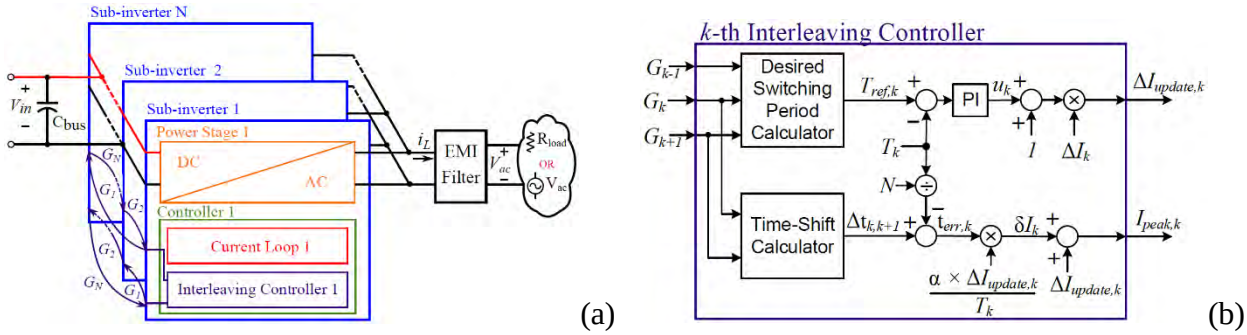



*Figure I-37 – Murray interleaved sub-inverters using circular chain [31]: a) Converter and control architecture, b) Local controller scheme.*

### I.4.2.4. Interleaving techniques summary

Considering a reconfigurable solution, these interleaving techniques can be grouped into 4 main categories related to how the modules get their phase reference and how they get the phase-delay. These two values can be either global or local.

*Table I-2 – Interleaving techniques mapping.*

| | | Phase-delay | |
|---|---|---|---|
| | | Local | Global |
| Phase reference | Local | Circular chain [28]–[31] | Voltage controlled delay loop [18], [19] |
| | Global | Global reference [32]<br>Phase splitter | Interleaving bus [23], [24]<br>Local measurement [25]–[27] |

The technique using local measurements has the global phase-delay and phase reference information without SPOF. However it does not seem to be compatible with VRM applications due to the reasons already exposed.

The techniques using the circular chain combine local averaging computations to obtain the phase-delay and the phase reference. This technique is modular and reconfiguration can be obtained by bypassing the communications based on a local decision. This technique seems to be the most adapted to obtain modularity and reconfiguration ability in a VRM application.

## I.5. Scientific approach

This thesis proposes and applies a formal method to model a system composed of identical control elements, called local controllers, all connected in a circular chain. It consists on the modeling of the individual local controller and the required communication links to set the whole system using matrix approach. The stability concern is simply solved using system diagonalization. This technique is applied on three different distributed interleaving systems, the third one being a new improved self-interleaving method. Concern involving the discontinuity on the angle are discussed, being fundamental for model simulation purposes.

The chapter II is dedicated to the study of the technique involving the circular chain of communications introduce by GATEAU [22] that uses a shared clock line (global phase reference). This study will allow further understanding of the circular chain technique not yet fully exposed, including the modeling, the system diagonalization and the stability concern. A transient response optimization method is proposed. Operators to avoid wrong interleaving for simulation purposes and practical implementation are described. Model simulations involving modal response, reconfiguration and start-up are shown. The particular case of a local controller with the correction disabled is studied, such as the case of communication/connection issue. An additional case with multiple circular chains, i.e. connections with the second/third/… neighbor, is studied. A generalization is proposed to generalize the results to a generic system using shared wire approach.

The chapter III is dedicated to the study of the technique involving the circular chain of communications introduce by COUSINEAU [28] where the local controllers exchange only the triangular carriers. A procedure similar to the one in chapter II is applied. The first part of the study include the modeling, system diagonalization and stability concern. A transient response optimization method is proposed and applied to design the equivalent controller. Model simulations involving modal response, reconfiguration and start-up are shown using the operator to avoid wrong interleaving. The steady-state values are revealed as a function of the

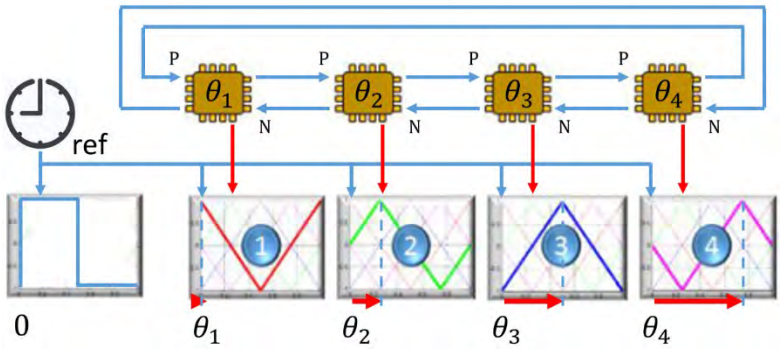
start arrangement. Some relations between mismatch and interleaving accuracy are provided. The particular case of a controller with infinite gain (comparator) is briefly analyzed. Circuit based simulations are used to validate the proposed model.

A new technique is proposed in chapter IV combining the advantages of the two approaches studied in the previous chapters. It can be summarized as the use of digital communication signals, as well as the decoupling between phase-delay control and carrier generation. The first part of the study describes the different elements involved and mainly the static relationships. The second part of the study focuses on the dynamic behavior of each building block. The third part include the overall modeling, system diagonalization and stability concern. Model simulations involving modal response is shown. Fault hazard impacts are described and the expected steady-state arrangement is revealed. A proof-of-concept is developed using a printed circuit board and standard SMDs to validate the results shown, including local controllers, the start-up modal pre-positioning and fault injection devices. Practical measurements are shown to correlate with the simulation results provide by the models previously proposed.

The perspectives, developed in Annex F, show the ongoing and non-accomplished works, including the integrated device developed with NXP SmartMOS10HV technology. The device consist of a converter with fully distributed control designed for parallel operation. The interleaving approach is the same presented in chapter IV. The voltage regulation is based on parallelized voltage regulators with AVP and the current balance uses a circular chain of communications to adjust the voltage references. The current balance technique is exposed and modeled, the constraints are exposed to the corrector calculation.

# II. Digital interleaving study

This chapter focuses on the solution introduced in [21], [22] that describes a digital solution to decentralized interleaving system where the carrier generators are synchronized with a shared reference clock signal. The Phase-Delay Local Controllers (PDLCs) are connected in a circular chain configuration to adjust their local Phase-Delay (PD) in between their neighboring PDs, as shown in Figure II-1. This circular chain approach is theoretically extensible to an infinite number of elements. The non-active PDLCs are simply bypassed by making a direct link between their respective neighbors in order to keep the chain of communications closed. When a reconfiguration is required, by either inserting or removing an active cell of the converter, a local decision is made to bypass or not the communications of the cell, so that the PDLCs reconfigure automatically their respective PDs without a centralized/supervisor decision. Ignoring the shared signal, this approach provide a good answer to SPOF issues by removing the notion of master.




$$\boldsymbol{\theta} = \begin{bmatrix}\theta_1\\ \theta_2\\ \theta_3\\ \theta_4\end{bmatrix} = 2\pi \begin{bmatrix}0.00\\ 0.25\\ 0.50\\ 0.75\end{bmatrix}$$

**P**: input from Previous
**N**: input from Next

*Figure II-1 – Circular chain of inter-cell communications composed of four PDLCs (N = 4) associated with four carrier generators.*

The challenge here, related to the stability analysis of this system in steady-state, is the large number of variables to manage and their coupling, i.e. the multiplicity of feedback loops involved. The PDs are state-variables and must be studied all together. Several differential excitation modes exist. Therefore, the stability of the decentralized interleaving device must be carefully analyzed for both start-up and reconfiguration singular cases.

## II.1. Decentralized interleaving and analytic model

In this approach, each sub-system is composed by a PDLC that provides a PD and a carrier generator. A global synchronization clock signal at the switching frequency is used by

the carrier generator as phase reference, i.e. the rising edge of the clock signal is considered as the zero angle position. The carrier generator implements an internal signal generator which uses the local PD parameter to generate a phased carrier with respect to the phase reference imposed by the external clock.

The PDLC involves a digital feedback loop to put the local PD in between the PDs of its neighboring cells. The PDLC will be modelled in this sub-chapter to reveal the system behavior. The iterations are considered synchronous for modelling, i.e. an iteration is done once all PDs have been updated. The PD values treated in this work are normalized, i.e. in between 0 and 1, and the quantization effects are not taken into account.

### II.1.1. Local controller modelling

In this approach, the PDs are numeric and sampled data due to the numerical implementation. As a result, the PDs signals $\theta^k$ are causal discrete-time signals, i.e. null for $k < 0$, where $k$ is the iteration number. The discrete-domain step function is denoted $u^k$. The values of ${\theta_P}^k$ and ${\theta_N}^k$ are the **P**revious and **N**ext neighboring PDs of the considered PDLC. For practical reason, it is important to mention that the values of the carrier positions are normalized, i.e. ranging from 0 to 1 instead of 0 to 2π radians. Their average value is the target position $\tilde{\theta}^k$ for the next iteration, computed at the iteration $k$, evaluated by the simple Eq. (II-1).

$$\tilde{\theta}^k = 0.5\left({\theta_P}^k + {\theta_N}^k\right) \tag{II-1}$$

$\theta^k$ is the local PD, and ${\varepsilon_\theta}^k$ is the local PD error evaluated by Eq. (II-2).

$${\varepsilon_\theta}^k = \tilde{\theta}^k - \theta^k \tag{II-2}$$

$\Delta\theta^k$ is the correction applied at the next iteration, given by the generic discrete transfer function $C(z)$ in Eq. (II-3). The stability study has to choose the $C(z)$ to ensure convergence.

$$\frac{\Delta\theta(z)}{\varepsilon_\theta(z)} = C(z) \tag{II-3}$$

Eq. (II-4) gives the new PD obtained $\theta^{k+1}$ for the local controller at the iteration $k+1$.

$$\theta^{k+1} = \theta^k + \Delta\theta^k \tag{II-4}$$

The block diagram of an PDLC is shown in Figure II-2.

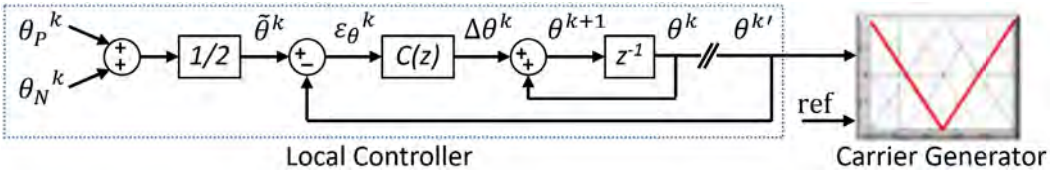



*Figure II-2 – Block diagram of the Phase-Delay Local Controller (PDLC) using digital feedback and a carrier generator.*

The iteration evolution of the local PD $\theta^k$ is illustrated in Figure II-3 where neighboring PDs, ${\theta_P}^k$ and ${\theta_N}^k$, cannot move.

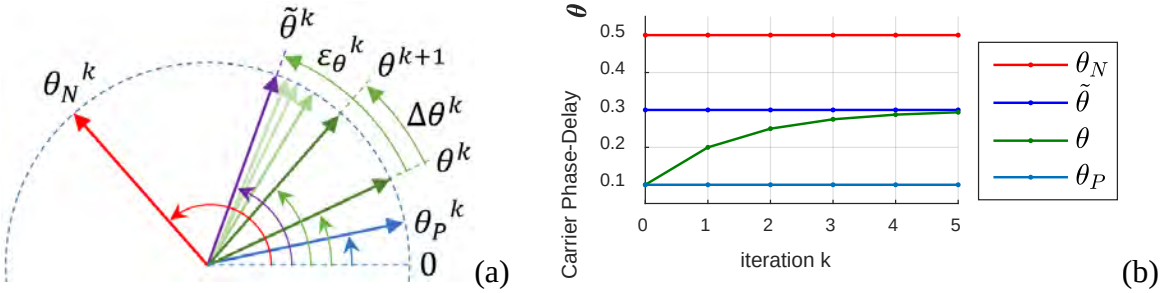



*Figure II-3 – Iterative local PD control phasor diagram: a) phase diagram, b) discrete-time diagram.*

Eq. (II-5) is the local controller open-loop discrete transfer function in the Z-domain.

$$\frac{\theta(z)'}{\theta(z)} = C(z)\frac{1}{z-1} \tag{II-5}$$

where $\theta(z)$ and $\theta(z)'$ represent respectively an injection and measurement to obtain the open-loop transfer function.

The closed-loop pole values depends on the corrector $C(z)$. Discrete control theory establishes that the system is stable if the closed-loop poles absolute value are less than 1, i.e. each poles must be located into the unit circle, the circle itself being the stability limit criterion.

Eq. (II-6) is the closed-loop local controller discrete response including the corrector $C(z)$ in the Z-domain taking into account the initial value $\theta_0$ and the input $\tilde{\theta}$. Two terms are shown, the first one corresponds to the free response dependent on the start value $\theta_0$ and the second corresponds to the forced response dependent on $\tilde{\theta}(z)$.

$$\theta(z) = \frac{z}{z-[1-C(z)]}\,\theta_0 + \frac{C(z)}{z-[1-C(z)]}\tilde{\theta}(z) \tag{II-6}$$

However, the variable $\tilde{\theta}$ is a combination of the previous and next PDs, i.e. other state-variables connected through the circular chain. Therefore, the study of the system response by only focusing on the behavior of independent local loops is not accurate. The stability of the local loop does not guarantee the stability of the overall system. Later on, a similar expression will be shown for the complete system.

### II.1.2. Overall system modelling

The study of the system's stability with a generic number $N$ of PDLCs including the several connections existing between them has to be performed. The overall system will be then modeled using a matrix approach. The PD values $\theta$ of all PDLC are numbered arbitrarily from

1 to $N$ going by the circular chain next neighbor direction, as shown in in Figure II-1. The PDs from $\theta_1$ to $\theta_N$ are then represented by a column vector $\boldsymbol{\theta}$ (in bold in the following equations).

In regard to the schematic shown by Figure II-2, the several error computation involved by the circular chain connection architecture can be represented using the matrix $\boldsymbol{L}$. It is similar to the Laplacian matrix in graph theory. The matrix $\boldsymbol{L}$, for $N$ equal to 6 and $\boldsymbol{\theta}$ the vector of the PDs sorted in ascending order (1 to $\boldsymbol{N}$) is shown in Eq. (II-7). It is an $N$-order square matrix composed of a negative unitary diagonal surrounded by factors 0.5.

$$\boldsymbol{L}_6 = \begin{bmatrix} -1 & 0.5 & 0 & 0 & 0 & 0.5 \\ 0.5 & -1 & 0.5 & 0 & 0 & 0 \\ 0 & 0.5 & -1 & 0.5 & 0 & 0 \\ 0 & 0 & 0.5 & -1 & 0.5 & 0 \\ 0 & 0 & 0 & 0.5 & -1 & 0.5 \\ 0.5 & 0 & 0 & 0 & 0.5 & -1 \end{bmatrix} \quad \text{(II-7)}$$

This matrix is used to calculate the PD errors $\varepsilon_{\theta 1}$ to $\varepsilon_{\theta N}$ present in the column vector $\boldsymbol{\varepsilon_\theta}$ derived from $\boldsymbol{\theta}$. The error vector at iteration $k$ is calculated with Eq. (II-8), where $\boldsymbol{\varphi}$ is an additive term, required to insure continuity of the computation in a trigonometric circle, that will be discussed latter. The $\boldsymbol{\varphi}$ vector is considered here constant and will be calculated by the "*phase-delay target operator*". Its value does not affect the stability study.

$$\boldsymbol{\varepsilon_\theta}^k = \boldsymbol{L}\,\boldsymbol{\theta}^k + \boldsymbol{\varphi} \quad \text{(II-8)}$$

From now on, all composing elements of the model are known, particularly the matrix $\boldsymbol{L}$ for the communication links and the vector $\boldsymbol{\varphi}$ for the error calculation. Figure II-4 shows a block diagram using the matrix $\boldsymbol{L}$ operator with $N = 6$. This system is linear, and the stability study can be easily performed.

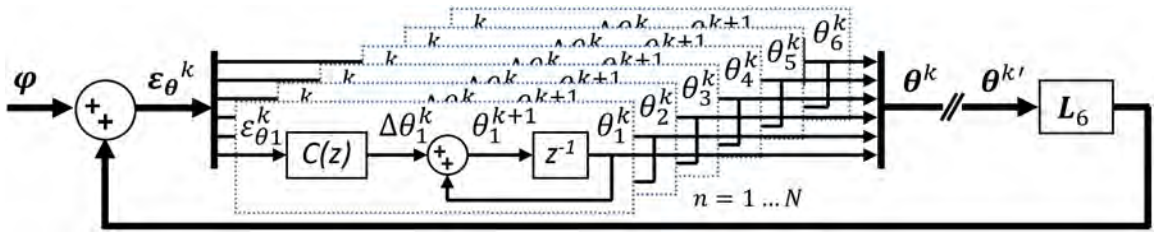



*Figure II-4 – Matrix representation of the complete system with $N = 6$.*

It derives Eq.(II-9), the open-loop discrete transfer function in the Z-domain.

$$\frac{\boldsymbol{\theta}(z)'}{\boldsymbol{\theta}(z)} = -\,\boldsymbol{L}\,C(z)\,\frac{1}{z-1} \quad \text{(II-9)}$$

The system closed-loop discrete transfer function can be written as represented by Eq. (II-10) that is comparable with Eq. (II-6) (monovariable), where $\boldsymbol{I}$ is the identity matrix and $\boldsymbol{\theta_0}$ is a column vector filled with the starting values of the PDs.

$$\boldsymbol{\theta}(z) = \left[z\boldsymbol{I} - \left(\boldsymbol{I} + \boldsymbol{L}\,C(z)\right)\right]^{-1} z\boldsymbol{I}\,\boldsymbol{\theta_0} + \left[z\boldsymbol{I} - \left(\boldsymbol{I} + \boldsymbol{L}\,C(z)\right)\right]^{-1} C(z)\boldsymbol{I}\,\boldsymbol{\varphi}(z) \qquad \text{(II-10)}$$

Now, the system's stability can be verified by diagonalization or eigendecomposition. In this case the diagonalization is convenient because the corrector $C(\mathrm{z})$ has a generic transfer function and its root locus can be plotted. The diagonalization and stability study will be performed analytically with respect to $C(\mathrm{z})$. The system diagonalization reveals the decoupled system dynamics, called the modal responses, and which determine the response of the overall system to external excitations. The whole system is stable if all modal responses are stable.

## II.2. Circulant matrices

The matrix $\boldsymbol{L}$ and the feedback loops couple all PDs together. A change of basis allows to decompose the original coupled system into several independent systems. The matrices $\boldsymbol{L}$ is real, symmetric and circulant due to the circular chain architecture. Several interesting properties come from the fact that a matrix is circulant.

### II.2.1. Circulant matrix diagonalization

Circulant matrices of order $N$ are diagonalisable with the Discrete Fourier Transform [33] (DFT) matrix $\boldsymbol{W}$ (eigenvectors) for $N$ samples, as shown in Eq. (II-11). The change of basis matrix $\boldsymbol{W}$ is the unitary DFT matrix, so $\boldsymbol{W}^* \times \boldsymbol{W} = \boldsymbol{I}$, with $\boldsymbol{W}^* = \boldsymbol{W}^{-1}$, where $\boldsymbol{W}^*$ is the conjugate transpose of $\boldsymbol{W}$ and equals to its inverse. Thus, the multiplication of $\boldsymbol{W}^*$ with the PD vector $\boldsymbol{\theta}$ produces the DFT of the PDs.

$$\boldsymbol{W} = \frac{1}{\sqrt{N}}\begin{pmatrix} 1 & 1 & 1 & \cdots & 1 \\ 1 & \omega & \omega^2 & \cdots & \omega^{(N-1)} \\ 1 & \omega^2 & (\omega^2)^2 & \cdots & \omega^{2(N-1)} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & \omega^{(N-1)} & \omega^{2(N-1)} & \cdots & \omega^{(N-1)^2} \end{pmatrix} \qquad \begin{matrix} \text{where} \\ \omega = e^{\sqrt{-1}\frac{2\pi}{N}} \end{matrix} \qquad \text{(II-11)}$$

Any circulant matrix $\boldsymbol{C}$ is a sum of a the shift matrix $\boldsymbol{S}$, shown in Eq. (II-12).

$$\boldsymbol{C} = \sum_{i=0}^{N-1} c_i\,\boldsymbol{S}^i \qquad \boldsymbol{S} = \begin{pmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ 0 & 0 & 0 & \ddots & \vdots \\ \vdots & \vdots & \vdots & \ddots & 1 \\ 1 & 0 & 0 & \cdots & 0 \end{pmatrix} \qquad \text{(II-12)}$$

The eigenvalue matrix $\boldsymbol{\Lambda_C}$ of the circulant matrix $\boldsymbol{C}$ can be derived from Eq. (II-13).

$$\boldsymbol{\Lambda_C} = \boldsymbol{W}\,\boldsymbol{C}\,\boldsymbol{W^{-1}} = \sum_{i=0}^{N-1} c_i\,\boldsymbol{U}^i \qquad \boldsymbol{U} = \begin{pmatrix} 1 & 0 & 0 & \cdots & 0 \\ 0 & \omega & 0 & \cdots & 0 \\ 0 & 0 & \omega^2 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & \omega^{(N-1)} \end{pmatrix} \qquad \text{(II-13)}$$

### II.2.2. Complex conjugate orthogonal eigenvectors

The matrix $\boldsymbol{W}$ columns are denoted $w_i$ with $i = 0 \dots N-1$. Even if the columns $w_i$ are orthogonal eigenvectors, some of them can be written such as the conjugate of another, as shown in Eq. (II-14). As matrix $\boldsymbol{W}$ is symmetric, it is also valid for its rows and the same property is valid for $\boldsymbol{W}^*$. As all the processed PDs $\boldsymbol{\theta}$ are real, the modal coefficient ${\theta^*}_{N-i}$ found with those ${w_i}^*$ vectors will be the complex conjugate of those found with ${w_{N-i}}^*$.

$$\begin{matrix} \lambda_{N-i} = \overline{\lambda_i} \\ w_{N-i} = \overline{w_i} \\ \boldsymbol{\theta} \in \mathbb{R}^{\boldsymbol{N}} \Leftrightarrow {\theta^*}_{N-i} = {w_{N-i}}^* \, \boldsymbol{\theta} = \overline{w_i}^* \, \boldsymbol{\theta} = \overline{{\theta^*}_i} \end{matrix} \qquad i = \begin{cases} 1 \dots \dfrac{N-1}{2}, & if\ N\ is\ odd. \\ 1 \dots N/2-1, & if\ N\ is\ even. \end{cases} \tag{II-14}$$

As a consequence, $N$ coefficients can represent the intrinsic information. The complex eigenvectors give two coefficients while the real ones gives only one. Those rows that can be written such as the conjugate of another have also the same eigenvalue. The matrix $\boldsymbol{L}$ has only $M$ different eigenvalues, where $M$ is an integer that satisfies the condition of Eq. (II-15).

$$M = \begin{cases} \dfrac{N+1}{2}, & if\ N\ is\ odd. \\ N/2+1, & if\ N\ is\ even. \end{cases} \tag{II-15}$$

A reduced representation can be used as decomposition matrix to represent the carried information. This matrix is named $\boldsymbol{V}$. It is N-by-M matrix and is composed of the $M$ first columns of $\boldsymbol{W}$. The columns of $\boldsymbol{V}$ are named $v_m$ with $m = 0 \dots M-1$. The rows of $\boldsymbol{V}^*$ and their respective spectrum with $N = 8$ ($M = 5$) are shown in Figure II-5.

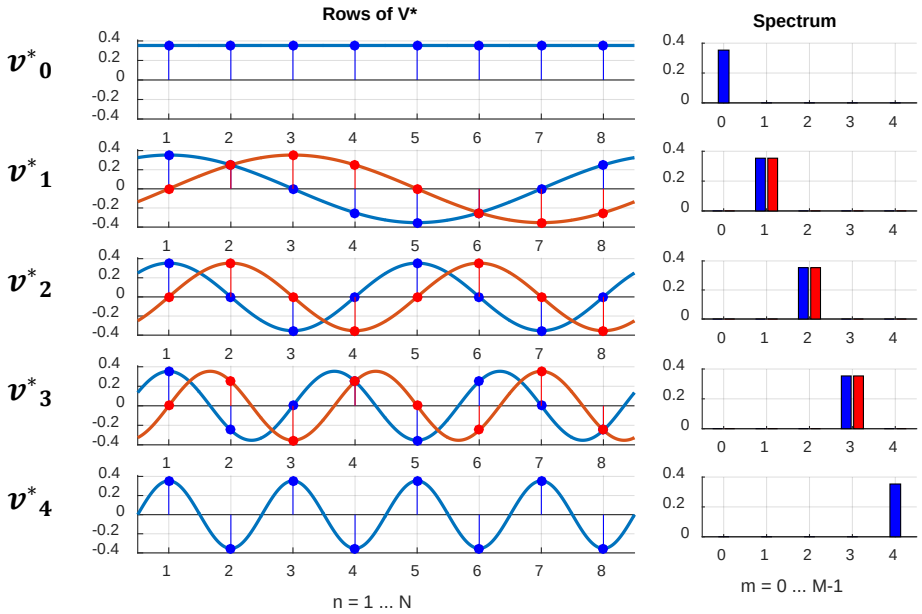



*Figure II-5 – Rows of $\boldsymbol{V}^*$ and their Spectrum ($N = 8$). blue/red lines: real/imaginary coefficients.*

Each of them has an equivalent row in $\boldsymbol{V}^*$, denoted ${v^*}_m$, that has a number of cycles $m$ related to its fundamental frequency. This number of cycles $m$ will be used thereafter as the

modal index. For that reason, the indexation starts from 0. The vector $v^*_0$ is real constant, so it will provide the average value, or also the common mode information of the decomposed variable. The eigenvectors of the double modes ($N = 8$, $m$ from 1 to 3) are complex and are naturally in quadrature (orthogonal) with their real part.

### II.2.3. L matrix eigenvalues

The eigenvalues of the circulant matrix are indeed known. All eigenvalues of $\boldsymbol{L}$ have to be identified to ensure the stability of all modal responses and to adjust the convergence speed. Gerschgorin's theorem shows that the eigenvalues of $\boldsymbol{L}$ are real and in between $-2$ and 0. The eigenvalues of $\boldsymbol{L}$ are shown in Eq. (II-16), where the complex exponential is rewritten in the cosine form. The $N$ diagonal elements $\lambda_{ii}$ of $\boldsymbol{\Lambda}$ are denoted $\lambda_i$ for $i = 0 \dots N-1$.

$$\lambda_i = \frac{e^{\sqrt{-1}\frac{2\pi i}{N}} + e^{-\sqrt{-1}\frac{2\pi i}{N}}}{2} - 1 = \cos\frac{2\,\pi\,i}{N} - 1, \qquad i = 0 \dots N-1 \tag{II-16}$$

As said previously, the $M$ different values can be found with $i = 0 \dots M-1$. Figure II-6 illustrates the $M$ values found with Eq. (II-16) for $N$ odd and even. For convenient reason, to regroup double eigenvalues, for $i \geq M$, $i$ can be written as $i - N$. In this way, the duplicated values have the same index. These duplicated values are related to the double modes shown in Figure II-5. If $N$ is even, a last eigenvalue equal to 2 is found for $i$ equal to $N/2$. In both cases, the first eigenvalue $\lambda_0$ is null.


*Figure II-6 – Eigenvalues of* $\boldsymbol{L}$ *for a) N = 5 (M = 3), b) N = 6 (M = 4).*

As this system has only $M$ different eigenvalues, the study of the system can be done using only these $M$ eigenvalues of $\boldsymbol{L}$.

## II.3. Change of basis

The state matrix $\boldsymbol{L}$ diagonalization is described in Eq. (II-17).

$$\boldsymbol{\Lambda} = \boldsymbol{W}^*\boldsymbol{L}\boldsymbol{W} \tag{II-17}$$

This system will be studied using the eigenvalues and the transformation matrices of $\boldsymbol{L}$ to reveal its stability. To do so, a change of basis expressed by the set of Eq. (II-18) is applied to the system, resulting in the Discrete Fourier Transform of all system signals.

$$\boldsymbol{\theta}^* = \boldsymbol{W}^*\,\boldsymbol{\theta}, \qquad \boldsymbol{\phi}^* = \boldsymbol{W}^*\,\boldsymbol{\phi}, \qquad \boldsymbol{\varepsilon_\theta}^* = \boldsymbol{W}^*\,\boldsymbol{\varepsilon_\theta} \qquad \boldsymbol{\theta_0}^* = \boldsymbol{W}^*\,\boldsymbol{\theta_0} \tag{II-18}$$

It should be noted that $\boldsymbol{\varepsilon_\theta}^*$, the error vector DFT, can be used to visualize the corrector performance, i.e. modal settling time, by looking the time required to mitigate it. Expression to compute its absolute value is shown in Eq. (II-19).

$$|\boldsymbol{\varepsilon_\theta}^*| = abs\big(dft(\,\boldsymbol{\varepsilon_\theta})\big) = abs(\,\boldsymbol{W}^*\,\boldsymbol{\varepsilon_\theta}) \tag{II-19}$$

Each element of $|\boldsymbol{\varepsilon_\theta}^*|$ is shown in Eq. (II-20). The components express the residual disturbance contained in each mode during simulation. It has to converge to zero as the system goes to steady-state.

$$|\varepsilon_\theta{}^*|_m = abs(\,\boldsymbol{w^*}_{\boldsymbol{m}}\,\boldsymbol{\varepsilon_\theta}), \qquad m = 0 \ldots M-1 \tag{II-20}$$

The others coefficients not chosen in Eq. (II-20) are duplicated (complex conjugated) because $\boldsymbol{\varepsilon_\theta}$ is always real. The open-loop discrete transfer function in the Z-domain in Eq. (II-9) is rewritten in a diagonal form in Eq. (II-21).

$$\frac{\boldsymbol{\theta}^*(z)'}{\boldsymbol{\theta}^*(z)} = -\,\boldsymbol{\Lambda}\,C(\mathrm{z})\,\frac{1}{z-1} \tag{II-21}$$

As the eigenvalue matrix $\boldsymbol{\Lambda}$ is diagonal, Eq. (II-21) can be rewritten in $N$ independent modal open-loop transfer functions (OLTF) as denoted in Eq. (II-22) using the diagonal index $i$, where the $N$ diagonal elements of $\boldsymbol{\Lambda}$ are denoted $\lambda_i$ for $i = 0 \ldots N-1$.

$$\frac{\theta_i{}^*(z)'}{\theta_i{}^*(z)} = -\,\lambda_i\,\frac{1}{z-1}C(\mathrm{z}), \qquad i = 0 \ldots N-1 \tag{II-22}$$

It should be noted that the diagonal OLTF in Eq. (II-22) is quite similar to the previous local OLTF of Eq. (II-5) where the only difference is the multiplicative term $-\lambda_i$. Nevertheless, its value is important and can compromise the system stability. Eq. (II-22) shows that the OLTF of each mode has the same identical corrector $C(\mathrm{z})$ multiplied with different eigenvalues. As a result, the modes cannot be independently controlled because of the feedback matrix $\boldsymbol{L}$. Using different correctors for each PDLC invalidates the approach presented here witch rely on identical correctors $C(\mathrm{z})$ to make the diagonalisation.

The closed-loop transfer function (CLTF) of Eq. (II-10) can also be written in a diagonal form such as in Eq. (II-23).

$$\boldsymbol{\theta}^*(z) = \big[z\boldsymbol{I} - \big(\boldsymbol{I} + \boldsymbol{\Lambda}\,C(z)\big)\big]^{-1}\,z\boldsymbol{I}\,\boldsymbol{\theta_0}^* + \big[z\boldsymbol{I} - \big(\boldsymbol{I} + \boldsymbol{\Lambda}\,C(z)\big)\big]^{-1}\,C(z)\,\boldsymbol{\varphi}^*(z) \tag{II-23}$$

Eq. (II-23) can be rewritten as a system of $N$ independent transfer functions provided by Eq. (II-24) because all matrices in Eq. (II-23) are diagonal.

$$\theta^*{}_i(z) = \frac{z}{z - \left(1 + \lambda_i\, C(z)\right)}\ \theta_0{}^*{}_i + \frac{C(\mathrm{z})}{z - \left(1 + \lambda_i\, C(z)\right)}\ \varphi^*{}_i(z),\ \ i = 0 \ldots N-1 \qquad \text{(II-24)}$$

It should also be noted that the diagonal CLTF term of Eq. (II-24) is quite similar to the previous local CLTF of Eq. (II-6) where the only difference is the multiplicative term $-\lambda_i$, as expected. The eigenvalues $\lambda_i$ must be found to establish the stability criteria and determine the several independent modal responses.

The revealed transfer functions are similar to the case of one single loop (II-6), but with the eigenvalues $\lambda_i$ playing as a multiplicative factor, instead of the constant −1. Two important points have to be highlighted here. At first, the mode 0 (common mode) pole is always equals to 1 because $\lambda_0 = 0$. Second, all differential modes, i.e. $m = 1 \ldots M-1$ cannot be independently controlled because the eigenvalues come from the feedback matrix $\boldsymbol{L}$ imposed by the circular chain architecture, as described previously. It is also important to note that all local controllers are identical, so they use the same corrector. These conclusions are valid for any type of local controller chosen.

It should be noted finally that this system does not take in account the average value of the PDs (common mode value) with the PDLC computations. As a consequence, this system is not able to impose any PD value because the common mode is not controllable, only relative values are controlled. The PDs and their average values may have any absolute value. If this observation is an issue, it can be avoided in noise sensitive applications using one constant PD for instance, but this solution may raise other stability considerations addressed in section II.8.

## II.4. **Stability concern**

The corrector $C(z)$ has to guarantee stability and convergence of all differential modes. To do so, in this discrete system model, all closed-loop poles have to be located inside the unit circle. Besides that, the controller specifications normally impose basic closed-loop constraints, such as steady-state error (static gain), settling time and damping. The corrector can be very simple or more complex, depending on the flexibility required. However, best trade-offs can be made with higher number of poles and zeros provided by the corrector $C(\mathrm{z})$. Eq. (II-25) shows four possible correctors $C(z)$, which are respectively proportional, integral, proportional-integral, and lead-lag.

| Proportional | Integral | Proportional-Integral | Lead-Lag | |
|---|---|---|---|---|
| $C(\mathrm{z}) = \alpha$ | $C(\mathrm{z}) = \alpha\ \frac{z}{z-1}$ | $C(\mathrm{z}) = \alpha\ \frac{z - z_{OL}}{z-1}$ | $C(\mathrm{z}) = \alpha\ \frac{z - z_{OL}}{z - p_{OL}}$ | (II-25) |

These correctors have, 1, 1, 2, and 3 freedom degrees, respectively. The three first controllers can be considered as special cases of the lead-lag controller. The proportional controller has $z_{OL} = p_{OL}$ that compensate each other, the integral controller has $z_{OL} = 0$ and $p_{OL} = 1$, the proportional-integral controller has $p_{OL} = 1$.

While the poles and zeros values imposes the possible locations of the closed-loop poles (root locus), this is the gain value α who sets closed-loop poles values (pole-zero plot). As the eigenvalue $\lambda_i$ appears as a gain factor, all modal root locus are the same. Nevertheless the pole-zero plots are different for each mode. The root locus analysis (lines) and pole-zero locations (poles "x" and zeros "o") of all modal CLTF using the correctors transfer functions $C(z)$, presented in Eq. (II-25), are revealed in Figure II-7 for $N = 8$, where the closed-loop poles of five different transfer functions ($M = 5$) are shown. The coefficients values $\alpha = 1$, $z_{OL} = 1/4$, $p_{OL} = 1/2$ are chosen to illustrate this example.

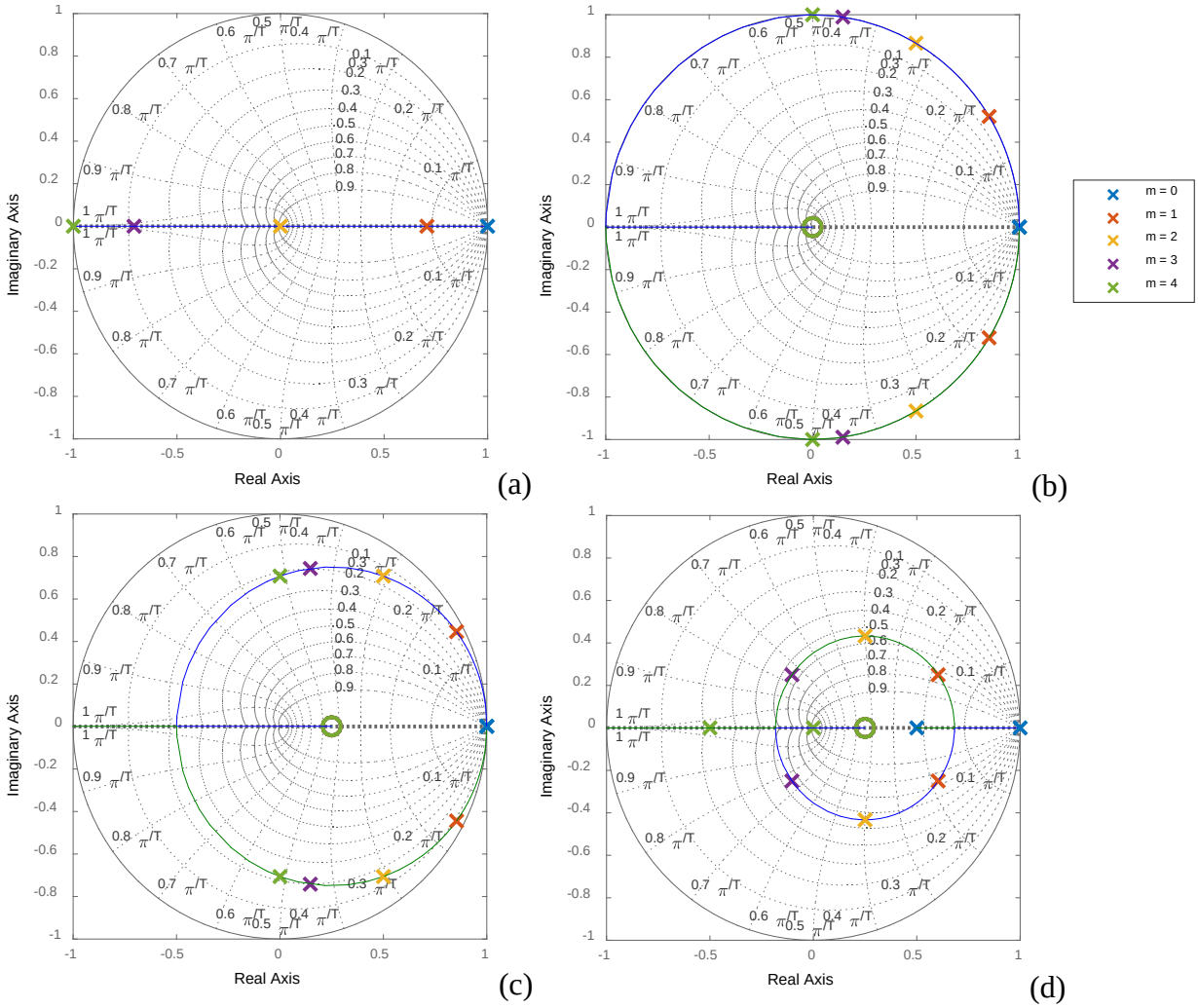



*Figure II-7 – Modal root locus analysis and pole-zero locations for $C(z)$: a) proportional, b) integral, c) proportional-integral, and d) lead-lag (with N = 8 the number of PDLCs and M = 5 the number of independent modes).*

All closed-loop poles are visible in these figures. Note that the mode 0 corresponds to the common mode which is not regulated. Each modal CLTF has different poles values due to its specific eigenvalue, but all zeros overlap. The integral controller is the only one in these particular cases that do not present a stable root locus, all poles are on the unit circle. This is because the open-loop transfer function becomes a double integrator, then, as known, a double integrator is always in stability limit, leading to undamped oscillations.

The proportional controller has only one coefficient, so a trade-off has to be made between the static gain, the settling time and the damping factor. It means that the coefficient α has to be as high as possible to ensure a small static error, but not too high to prevent the poles going outside the unit circle. As shown in Figure II-7 (a), $\alpha = 1$ places mode 4 pole on the unit circle. The proportional-integral and lead-lag controllers present double poles for each mode. As they have more freedom degrees, better pole locations can be achieved, i.e. closer to the origin and providing higher damping. The lead-leg controller's three coefficients can potentially provide a very good trade-off concerning static gain, global transient response and modal transient response.

From now, a complete study of the stability and system dynamic responses for the proportional and lead-lag correctors will be developed. It will be done for any α and $N$ to reveal the stability criteria and to optimize the settling time.

### II.4.1. Proportional corrector

The proportional corrector represented by the gain α is the simplest case because the transfer function order does not change and all pole values are real. In this study, the gain α is also called "the convergence factor". The system dynamics can be easily identified from Figure II-4, Eq. (II-9) and Eq. (II-10). The state matrix $\boldsymbol{A}$ , in Eq. (II-26), can be easily introduced for the stability study.

$$\boldsymbol{A} = \boldsymbol{I} + \alpha\, \boldsymbol{L}, \tag{II-26}$$

The stability can now be studied using the eigen decomposition of the matrix $\boldsymbol{A}$, revealing the system eigenvalues, i.e. the poles of the system. The eigenvalue matrix of $\boldsymbol{A}$ is named $\boldsymbol{\Lambda_A}$.The $\boldsymbol{\Lambda_A}$ expression is shown in Eq. (II-27).

$$\boldsymbol{\Lambda_A} = \boldsymbol{W}^{*}\boldsymbol{A}\boldsymbol{W} = \mathbf{I} + \alpha\, \boldsymbol{\Lambda} \tag{II-27}$$

The $N$ diagonal elements $\lambda_{Aii}$ of $\boldsymbol{\Lambda_A}$, named $\lambda_{Ai}$ for $i = 0 \ldots N-1$, are the $N$ modal poles of the diagonal representation shown in Eq. (II-28). As shown earlier, there are only $M$

different eigenvalues, so only $M$ modes have to be studied. As a result, the poles of the *diagonal modal transfer function* described in (II-24) are revealed in Eq. (II-28).

$$\lambda_{Am} = 1 + \alpha\,\lambda_m, \quad m = 0 \dots M-1 \tag{II-28}$$

#### II.4.1.1. Stability Criterion

To guarantee the stability, all differential modes ($m \neq 0$) have to be damped correctly, i.e. its eigenvalues' absolute value must be less than 1, so the convergence factor α has to respect the condition $0 < \alpha < 1$ to ensure stability. The demonstration is shown in Eq. (II-29).

$$\begin{aligned} &\text{Assuming} && |\lambda_{Am}| = |1 + \alpha\,\lambda_m| < 1, \quad -2 \le \lambda_m < 0, \quad \mathrm{m} = 1 \dots M-1 \\ &\text{then} && |1 + \alpha\,\lambda_m| < 1 \iff -1 < 1 + \alpha\,\lambda_m < 1 \iff 0 < \alpha < 1 \end{aligned} \tag{II-29}$$

It makes a difference compare to the model taking into account only one single loop. Indeed, the system seemed to be stable for α between 0 and 2 because the eigenvector does not appear. Figure II-8 shows the different eigenvalues as a function of $\alpha$. The values for α equal to 1, 3/4 and 1/2 are highlighted. It shows the trade-off between stability (being in the range –1 to 1) and the system dynamics (being close to 0) made with the choice of α. Increasing α from 0 to 0.5 decreases $\lambda_{Ai}$ absolute values. When α is greater than 0.5, some eigenvalues become negative and their absolute value increase. Those modes are still stable, but they have an under-damped oscillating response. It should be noted the last mode (mode 4) reaches the stability limit when $\alpha = 1$.

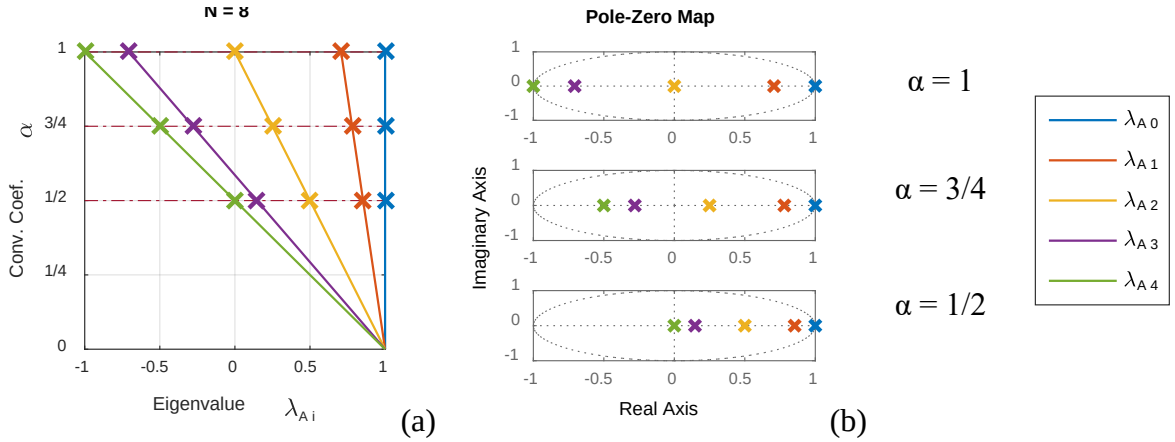



*Figure II-8 – Eigenvalue analysis with N = 8. a) Eigenvalue $\lambda_{Ai}$ vs. Convergence Coefficient α, b) Pole-zero plot for α equal to 1, 3/4 and 1/2.*

#### II.4.1.2. Settling Time Optimization

The settling time of a mode depends both on the local controller computation frequency/ period and on the corrector parameters. Indeed, there is no physical process behind this interleaving system, i.e. no inertia, power or energy involved. The computation period can also

be completely independent of the carrier period. The computation period is limited mainly by the serial communication bandwidth, if used, and by the computation delays.

Based on the corrector parameters, initial value ${\theta_0}^*_i$ and ${\varphi^*}_i(z)$, the discrete domain modal responses ${\theta^*}_m(k)$ can be computed to each mode by taking the inverse Z-transform (operator noted $\mathcal{L}^{-1}$) of ${\theta^*}_i(z)$, shown in Eq. (II-24). This result is shown in Eq. (II-30), where ${\theta^*}_{mh}(k)$ is the natural (homogeneous) response and ${\theta^*}_{mf}(k)$ is the forced (non-homogeneous) response, *m* is the mode number, H is the Homogeneous marker and F is the non-homogeneous (Forced) marker.

$$ {\theta^*}_m(k) = \mathcal{L}^{-1}\{{\theta^*}_i(z)\} = {\theta^*}_{mH}(k) + {\theta^*}_{mF}(k), \;\; m = 0 \dots N-1 \qquad \text{(II-30)} $$

where

$$ {\theta^*}_{mH}(k) = \mathcal{L}^{-1}\left\{\frac{z}{z-\left(1+\lambda_i\, C(z)\right)}\,{\theta_0^*}_m\right\} \quad {\theta^*}_{mF}(k) = \mathcal{L}^{-1}\left\{\frac{C(z)}{z-\left(1+\lambda_i\, C(z)\right)}\,{\varphi^*}_m(z)\right\} $$

Then, based on the corrector parameters, the number of iterations for convergence can be computed, for example, by the number *k* of iterations necessary to reduce the absolute value of each natural (homogeneous) differential mode response ${\theta^*}_{mH}$ to less than 5% of its initial value ${\theta_0^*}_m$. The natural (homogeneous) modal response ${\theta^*}_{mh}$ shown in Eq. (II-31) is found by computing the inverse Z-transform shown in Eq. (II-30).

$$ {\theta^*}_{mH}(k) = {\lambda_{\mathrm{Am}}}^{\mathrm{k}}\,{\theta_0^*}_m, \;\; \mathrm{k} \geq 0, \qquad m = 1 \dots M-1 \qquad \text{(II-31)} $$

Eq. (II-32) shows the general formula for the number of iterations required derived from Eq. (II-31).

$$ \begin{gathered} abs\left(\frac{{\theta^*}_{mH}(k)}{{\theta_0^*}_m}\right) = abs\left({\lambda_{\mathrm{Am}}}^{\mathrm{k}}\right) \leq 5\% \quad \Rightarrow \\ k_{5\%\_\mathrm{m}} \geq \frac{log(0.05)}{log\left(abs(\lambda_{\mathrm{Am}})\right)}, \;\; m = 0 \dots M-1 \end{gathered} \qquad \text{(II-32)} $$

Table II-1 shows the number of iterations required for the convergence of the differential modes in the cases of Figure II-8. The mode 4 is at the limit of stability and oscillates with $\alpha = 1$. The modes 1 and 2 speeds up when α increases.

*Table II-1 – Number of iterations for 5% response ($N = 8$).*

| | $k_{5\%\_1}$ | $k_{5\%\_2}$ | $k_{5\%\_3}$ | $k_{5\%\_4}$ |
|---|---|---|---|---|
| α = 1 | 8.6 | 0 | 8.6 | +∞ |
| α = 3/4 | 12 | 2.2 | 2.4 | 4.3 |
| α = 1/2 | 19 | 4.3 | 1.6 | 0 |

It shows explicitly the number of iterations required for each differential mode with a given α parameter. With different configurations observed, it is not easy to guess which would be the optimal one. As numerous performances depend on the same parameter, a criterion has to be proposed to find a trade-off helping to choose α. Each differential mode eigenvalue has to be reduced in absolute value to speed up the response. One option is to improve the worst case by reducing as much as possible the absolute value of the larger eigenvalue. A second option is to improve the response globally such as minimizing either the quadratic sum of the $\lambda_{\mathrm{Am}}$ or the number of iterations $k_{5\%}$ of each mode. The results of these three approaches are shown in Figure II-9 for $N = 8$.

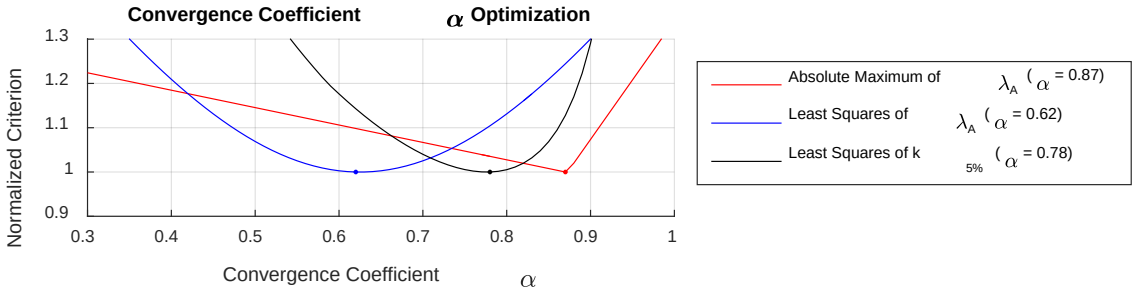



*Figure II-9 – Optimized Convergence Coefficient α. Minimising criterion: absolute maximum, least squares of $\lambda_{Am}$ and least squares of $k_{5\%\_m}$.*

The minimum value using the absolute maximum criterion is found with $\alpha = 0.87$. It is also the point where the absolute values of $\lambda_{A1}$ and $\lambda_{A4}$ are equal. The minimum value using the $\mathbf{\Lambda_A}$ eigenvalue least squares criterion is found with $\alpha = 0.62$. Finally, the minimum value using the $k_{5\%}$ least squares criterion is found with $\alpha = 0.78$. Each criterion gives different optimum values. For this configuration with $N = 8$, a convenient value is about 3/4.

It should be noted, in this system, the convergence dynamics depend also on which modes are excited. Indeed, if only fast modes are excited the convergence is faster. For instance, if mode 1 is not excited with $\alpha = 1/2$, its convergence would be faster than the case where $\alpha = 3/4$ and all modes are excited. An example will be shown latter.

### II.4.1.3. Eigenvalues and Stability vs. Number of Active PDLCs

Using this distributed democratic approach for the interleaving of the carriers, the ability of self-reconfiguration if an active PDLC is added or removed is inherent to this system. So the eigenvalues have to be computed for several numbers of active PDLCs. The eigenvalues are computed as a function of $\alpha$ in Figure II-10 for the cases of $N$ ranging from 5 to 8. Several lines are drawn expressing the values of the existing eigenvalues that are related to $N$. $\lambda_{A0}$, which is related to the common mode, is constant equal to 1, independent of $N$ and $\alpha$, because the system is made to control only PD differences.

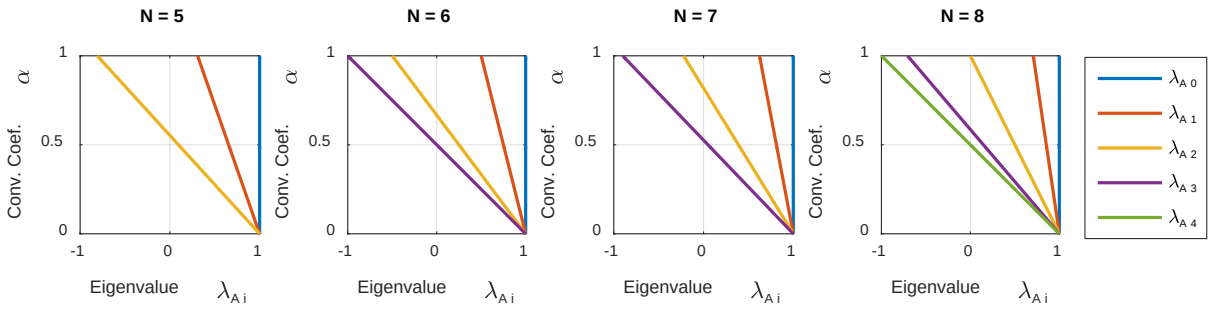



*Figure II-10 – Eigenvalues vs. Convergence Coefficient α for different numbers of active PDLCs (N = 5…8)*

All differential modes are controllable because their eigenvalues depend on the parameter $\alpha$. The differential modes are double and overlap themselves two-by-two (studied together), $M$ going from 1 to $(N-1)/2$. If $N$ is even, the last mode ($m = N/2$) is a single mode.

When $\alpha$ is equal to 1 with $N$ even, the last mode $N/2$ reaches the stability limit. Nevertheless, if $N$ is odd, the value of the last mode does not reach $-1$, but only if $N$ tends towards infinity. Thus, the limit of stability is never reached for the case of $N$ odd. Therefore, this system is stable for any value of $N$ if $0 < \alpha < 1$.

A reconfiguration event is the modification during operation of the number $N$ of active PDLCs. Non-active PDLCs are bypassed in order to maintain closed the chain of communications and become invisible (transparent) to active PDLCs. As seen before, all eigenvalues depend on a single convergence factor α, and a trade-off has to be made. On the other hand, when a reconfiguration is made, α remains the same and the eigenvalues have to continue, in a reasonable limit, to ensure stability and fast convergence time. The bypassed PDLCs are no longer taken into account in the stability analysis. Figure II-11 shows the pole locations for different values $N$ of active PDLCs with α equal to 3/4 and 1.

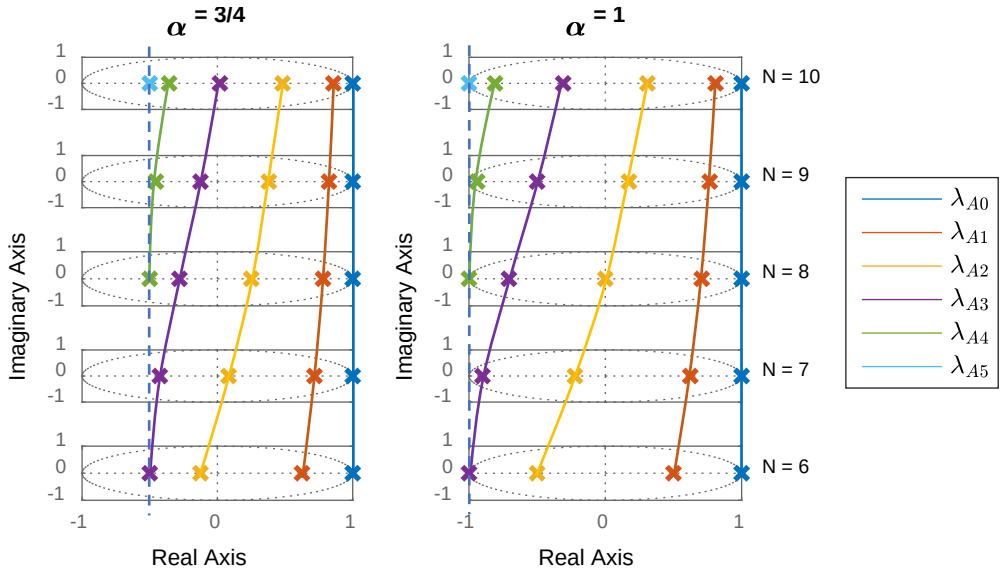



*Figure II-11 – Root locus for α equal to 3/4 and 1 and N ranging from 6 to 10*

As shown in the figure, the number of existing modes is a function of $N$. As $N$ increases, the eigenvalues shift to the right, and the new ones appear on the left. As the eigenvalues change, they stay always in the same range between $1-2\alpha$ and 1, e.g. [-1/2 1] for α equal to 3/4 and [-1 1] for α equal to 1. As previously demonstrated in section II.4.1.1 Stability Criterion, this system is stable for any value of $N$ if $0 < \alpha < 1$.

The 5% response should also be optimal when $N$ varies. However the number of active modules is unknown and all local controllers should be equal. To simplify the design, the same α is used for any $N$ value and a relative time response degradation is observed.

The parameter $k_{5\%\_m}$ shows the performance of each mode independently. However, to optimize all modes together, a new parameter combining all mode performances has to be proposed. One possibility is to use the least squares of $k_{5\%\_m}$ as a fonction of the convergence coefficient α and the number $N$ of active PDLCs, as shown in Figure II-12.

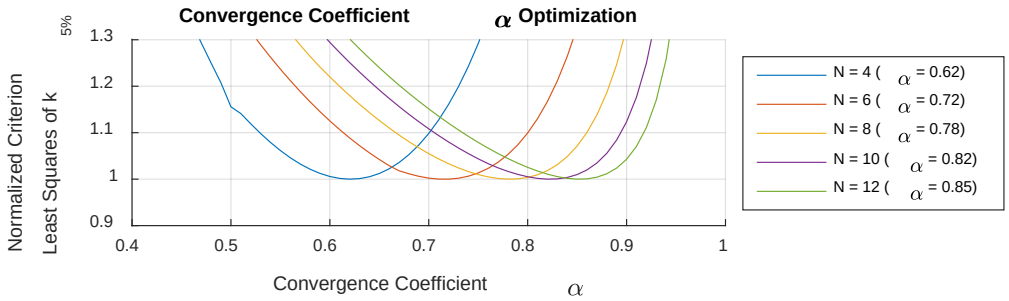



*Figure II-12 – Optimized Convergence Coefficient α using least squares of $k_{5\%\_m}$ criterion. Sensibility to $N$.*

The several curves show the minimum is in general between 0.6 and 0.9, and it goes up with $N$. This happens because $\lambda_1$ goes down with $N$ and the $1^{st}$ mode $(m = 1)$ becomes dominant. The curves would shift slightly to the right for $N$ odd because the eigenvalues are slightly smaller in this case. A global optimum can be chosen at 3/4, where most of the curves loose less than 10% relative to the optimum. More information about the parameter combining all mode performances can be find in [34].

### II.4.2. Lead-lag corrector

The lead-lag corrector shown in Eq. (II-25) brings more flexibility to the controller design because three parameters can be chosen, i.e. gain, zero and pole values. These parameters are considered as Open-Loop (OL) zero $z_{OL}$ and pole $p_{OL}$, both real numbers. The properties developed during the previous study of the proportional controller are still valid here using the proposed corrector. Complementary explanations about the corrector design will be given here.

II.4.2.1. Stability criterion

With the lead-lag corrector, the new expression of the modal natural (homogeneous) response $\theta^*_{mh}$ is shown in Eq. (II-33). It can be used to define the stability criterion and the dynamic responses of the differential modes, i.e. the settling time or 5% response. $\theta^*_{mh}$ is found by inserting the corrector transfer function $C(z)$ at the first term of Eq. (II-30), where *m* is the mode number and *h* is the homogeneous marker.

$$\theta^*_{mh}(z) = \frac{z^2 - (p_{OL}+1)\,z + p_{OL}}{z^2 - (p_{OL}+1+\alpha\,\lambda_m)\,z + (p_{OL}+\alpha\,\lambda_m\,z_{OL})}\;{\theta_0}^*_i, \qquad \mathrm{m} = 0 \ldots \mathrm{M}-1 \quad \text{(II-33)}$$

To simplify the study and further implementation, some relations are proposed. The stability criterion and its constraint are shown in Eq. (II-34). This result is valid for any value of $N$.

$$0 < \alpha < \frac{1+p_{OL}}{1+z_{OL}} \quad \Leftrightarrow \quad 0 < z_{OL} < p_{OL} < 1 \qquad \text{(II-34)}$$

The demonstration is shown in Annex A.

II.4.2.2. Transient response optimization

To optimize the transient response, the 5% settling time remains a good criterion. An eigen decomposition can be performed and the eigenvalues can be used to compute the number of iterations required for convergence. However, if only the dominant pole is considered, it would be inaccurate because the zeros of the transfer functions disturb and delays the response. For this reason, the diagonalization is preferred. The number of iterations for 5% convergence $k_{5\%}$ should be the number $k > 0$ of iterations necessary to reduce the absolute value of each natural (homogeneous) differential mode response $\theta^*_{mh}$ to less than 5% of its initial value ${\theta_0}^*_m$. The envelope on Bode diagram is considered to simplify the analysis. So $k_{5\%}$ is the number of iterations $k > 0$ when the envelope reaches the 5% criterion. Depending on the modal eigenvalue $\lambda_m$ and α, four different pole cases can be found: two complex conjugate poles, two real coincident poles, two real different poles or one real pole. Their partial fraction decomposition is shown in Eq. (II-35) with its envelope, found by applying the inverse Z-transform to the partial fractions.

$$\begin{array}{lll} p_1, p_2 \in \mathbb{C},\ p_2 = {p_1}^* & \dfrac{r}{1-p_1\,z^{-1}} + \dfrac{r^*}{1-{p_1}^*\,z^{-1}} & 2\,|r|\,|p_1|^k \\ p_1, p_2 \in \mathbb{R},\ p_2 = p_1 & \dfrac{r_1}{1-p_1\,z^{-1}} + \dfrac{r_2\,p_1\,z^{-1}}{(1-p_1\,z^{-1})^2} & |r_1 + k\,r_2|\,|p_1|^k \end{array} \qquad \text{(II-35)}$$

| | | |
|---|---|---|
| $p_1, p_2 \in \mathbb{R},\ \ p_2 \neq p_1$ | $\frac{r_1}{1-p_1\,z^{-1}} + \frac{r_2}{1-p_2\,z^{-1}}$ | $\lvert r_1\,\lvert p_1\rvert^k + r_2\,\lvert p_2\rvert^k\rvert$ |
| $p_1 \in \mathbb{R}$ | $\frac{r_1}{1-p_1\,z^{-1}} + \frac{r_2\,z^{-1}}{1-p_1\,z^{-1}}$ | $\left\lvert r_1 + \frac{r_2}{\lvert p_1\rvert}\right\rvert \lvert p_1\rvert^k$ |

A settling time solution can be found analytically for the first and last cases, but only numeric solution can be used for the others.

The time response depends on numerous parameters ($z_{OL}$, $p_{OL}$, α, $N$ and $m$) and all of them could be optimized based on the closed-loop criteria. It gives a $5^{th}$ order problem where a comparison criterion has to be defined. In practice, results are hard to visualize and verify.

For simplification proposes, the values $z_{OL} = 1/4$ and $p_{OL} = 1/2$ are chosen without further justification because they provide a good trade-off. The stability is ensured for $0 < \alpha < 1.2\ (6/5)$. Table II-2 shows the number of iterations required for convergence of the differential modes. The mode 4 is at the limit of stability and oscillates for $\alpha = 6/5$.

*Table II-2 – Number of iterations for 5% response using lead-lag corrector ($N = 8$).*

| | $k_{5\%\_4}$ | $k_{5\%\_3}$ | $k_{5\%\_2}$ | $k_{5\%\_1}$ |
|---|---|---|---|---|
| $\alpha = 6/5$ | $+\infty$ | 6.4 | 4.0 | 6.8 |
| $\alpha = 1$ | 5.3 | 3.0 | 4.5 | 7.2 |
| $\alpha = 3/4$ | 3.4 | 3.9 | 5.2 | 7.9 |

Table II-2 shows explicitly the number of iterations required for each differential mode with a given α parameter. With different configurations observed, it is not easy to guess which would be the optimal one. So the normalized least squares of $k_{5\%}$ is used to provide a general criterion for each α value.

Chosen $z_{OL}$ and $p_{OL}$ values and the normalized least squares of $k_{5\%\_\mathrm{m}}$, the problem is reduced to a $2^{nd}$ order problem, depending only on α and $N$. This system has an unknown number of active modules and all local controllers are identical. To simplify the design of the optimal 5% settling time, a parametric plot of the least squares of $k_{5\%}$ versus the convergence coefficient $\alpha$ and $N$ is shown in Figure II-13 for $N = 8$.

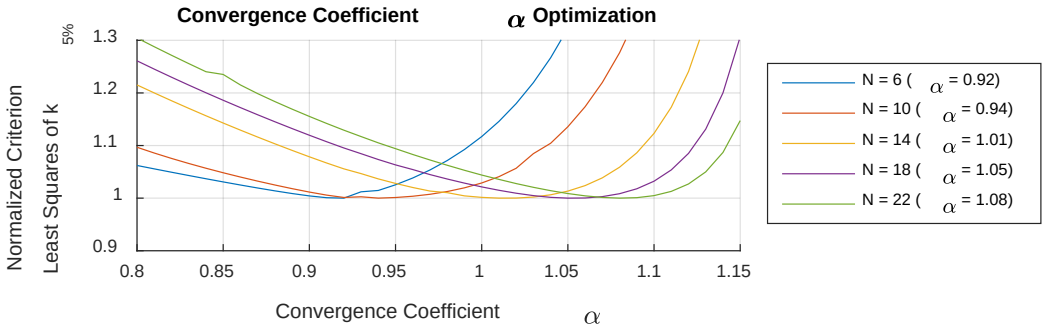



*Figure II-13 – Optimized Convergence Coefficient α using least squares of $k_{5\%}$ criterion. Sensibility to N.*

The curves show the minimum is in general between 0.9 and 1.1, and it goes up with *N*. It happens because $\lambda_1$ goes down with *N* and $1^{st}$ mode ($m = 1$) becomes dominant. The curves would shift slightly to the right for *N* odd because the eigenvalues are slightly smaller in this case. A unitary α seems to be a global optimum, for which in most cases the performance will be only 10% worse than the optimum.

In this system, the convergence dynamics is less dependent on which modes are excited because their related 5% settling times are harmonized, more uniform, i.e. the modal settling times are almost the same. This is due to the additional parameters provided by the lead-lag corrector.

### II.4.2.3. Diagonal Response

The dynamic behavior of the overall system will be simulated and the settling times compared with the ones predicted. A Multiple Input Multiple Output (MIMO) transfer function based model is defined and simulated using MathWorks MATLAB®. In the simulations performed hereafter, the system starts in its expected equilibrium state with all the carriers well interleaved. Each mode is excited individually one after the other, from the common mode (mode 0) to the last one (mode 4) using the system eigenvectors (lines of the DFT matrix) as signal components. To do so, the disturbance signal $\boldsymbol{D}(z)$, composed of a sequence of orthogonal disturbances shown in Eq. (II-36), is summed with the corrector output.

$$\boldsymbol{D}(z) = \frac{1}{2\,N}\,\boldsymbol{v}_0\,z^{-4} + \sum_{m=1}^{M-1} real(a_m \boldsymbol{v}_m)\,z^{-10m-1} \qquad \text{(II-36)}$$

where $a_m$ are complex coefficients.

Figure II-14 shows the simulation results of a system with eight PDLCs (*N* = 8) and $\alpha$ equal to either 1 or 6/5. Each simulation result consists of the modal disturbance applied $\boldsymbol{d}^* = |\boldsymbol{V}^*\,\boldsymbol{d}|$, the PD $\boldsymbol{\theta}$ behavior, the local error $\boldsymbol{\varepsilon_\theta}$, and its modal decomposition $|\boldsymbol{\varepsilon_\theta}^*|$, to observe the total mode disturbance.

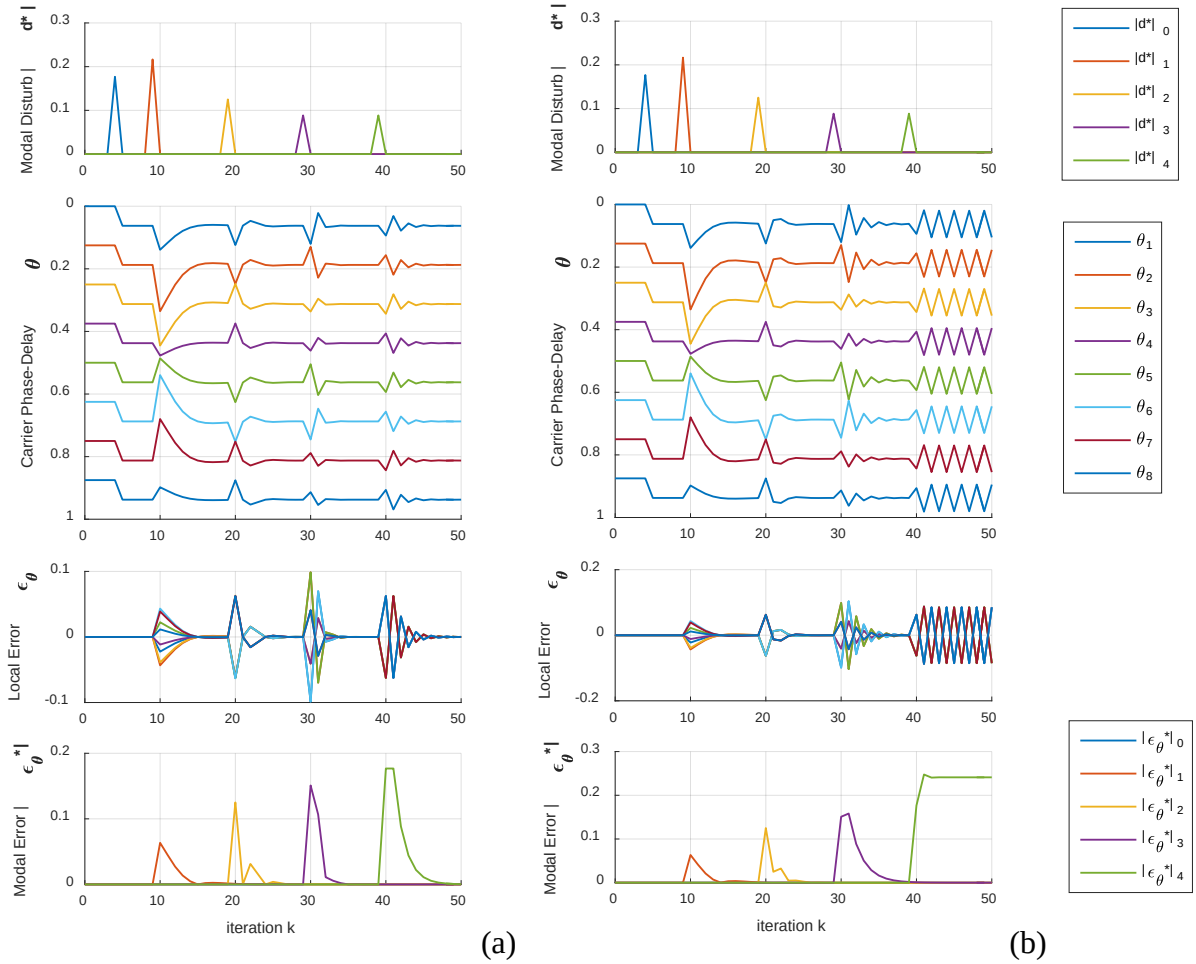



*Figure II-14 – Dynamic modal response (N = 8) a) α = 1; b) α = 6/5.*

Using the modal disturbance $\boldsymbol{D}(z)$, it is possible to distinctly observe the modal excitations of each independent mode being applied successively. The PD values behave as expected. The deviations that appear are characterized by their eigenvectors' shape behavior (kind of sine wave) and their cycle number, as shown in Figure II-5.

For the case illustrated in Figure II-14 (a), all modes are correctly damped. For the case in Figure II-14 (b), the mode 4 ($m = 4$) is at its stability limit as demonstrated by the stability criterion. So it oscillates without damping because one pole value is equal to $-1$. This simulation confirms the expected value of the number of iterations required for convergence forecasted in Table II-2. It can be seen with $\alpha = 1$ case, all modes have different oscillation frequencies (different damping), but almost the same settling time as a result of the harmonization obtained using least squares strategy.

### II.4.3. General case stability criterion

As mentioned earlier, the proportional, integral, and proportional-integral are particular cases of the lead-lag controller. Eq. (II-37) shows the general stability criterion with its constraint for all correctors previously introduced, allowing to choose the α range where the

system is stable to a given pole and zero couple. It should be noted this expression is not yet mathematically proven and acts only as a rule-of-thumb.

$$0 < \alpha < \frac{1 + p_{OL}}{1 + z_{OL}} \quad \Leftrightarrow \quad \begin{matrix} 0 \leq z_{OL} \leq p_{OL} \leq 1 \\ p_{OL} - z_{OL} < 1 \end{matrix} \tag{II-37}$$

This expression is valid for the proportional controller ($z_{OL} = p_{OL}$), where the $z_{OL}$ and $p_{OL}$ compensate each other, and for the proportional-integral controller ($p_{OL} = 1$) also. Moreover, it should be noted the integral controller, which is instable, no does not respect the second constraint ($p_{OL} = 1$, $z_{OL} = 0$, then $p_{OL} - z_{OL} = 1$).

Since the stability condition established and the dynamic responses verified, the implementation related issues will be discussed. This study aims to guarantee the implemented system behaves as predicted by the model developed previously.

## II.5. Phase-delay target operator and wrong interleaving discussion

The principle of correction by comparison with the neighbors has been used previously in the literature for different purposes. For instance, in [11] a current balance system equalizes the values of several inductor currents with the circular chain. With this principle applied for the interleaving, it should be noted the system equalizes the PD differences between the neighbors, not its absolute values. In the approach presented in [28], the PD differences and their corrections are made in a relative manner to each local carrier.

In the approach presented here, the PDs are related to a global phase reference, as shown in Figure II-3. Thus, there is a discontinuity between the last and the first PD due to the trigonometric circle itself, and therefore the operator $\boldsymbol{L}$ does not work for all PDLCs. Using normalized PD, the discontinuity appears when the PD approaches the value 1 from the negative side, as shown in the Figure II-15 (a), but also when the PD approaches 0 from the positive side. Figure II-15 (b) shows a well-interleaved system with five carriers ($N = 5$) where the normalized PD differences are all equal to 0.2 ($1/N$). The PD error has to be equal to zero. Figure II-15 (c) shows the expected target position $\tilde{\theta}_1$ for the first carrier and the computed average value of the positions of its neighbors. These two values are different and in phase opposition.

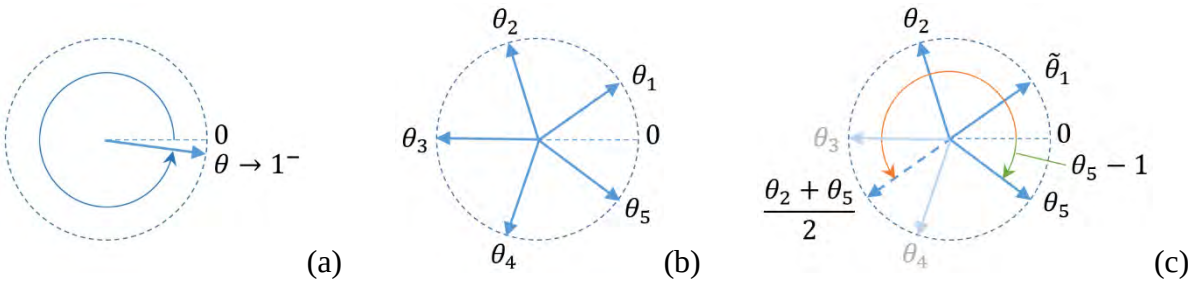



*Figure II-15 – PD representation: a) PD discontinuity around 1 and 0, b) Well-interleaved system with five carriers, c) Expected target $\tilde{\theta}_1$ and average position of $\theta_1$ neighbours.*

As the expected target position $\tilde{\theta}_1$ is different from the $\theta_1$ position, i.e. the neighbors' position average, this system requires then additional operations such as those described in [21], [22], [35]. Issues are described in [30] as *"ambiguous phase ordering"* and *"ambiguity in steady-state"*, linked with the error signal calculation. The "phase-delay target operator" introduced here are able to evaluate the error and compute a new PD value despite the discontinuity.

To illustrate the *phase-delay target operator* necessity, the values of the PD column vectors $\boldsymbol{\theta}$ and $\boldsymbol{L\,\theta}$ are shown in Eq. (II-38) and Eq. (II-39) respectively, using the position values relative to the well-interleaved system shown in Figure II-15 (b).

$$\boldsymbol{\theta} = [0.1 \quad 0.3 \quad 0.5 \quad 0.7 \quad 0.9]^T \tag{II-38}$$

$$\boldsymbol{L\,\theta} = [0.5 \quad 0.0 \quad 0.0 \quad 0.0 \quad -0.5]^T \tag{II-39}$$

As anticipated, the $\boldsymbol{L\,\theta}$ operation, required to compute the several local errors, does not give the null error vector expected for a well-interleaved system. As the error operator result is wrong, the PDLCs having a neighbor across the discontinuity ($\theta_1$ and $\theta_5$) have a local error different from zero. This value can be compensated by an additive term $\boldsymbol{\varphi}$ introduced earlier, as shown in Eq. (II-8). In this particular case, the required $\boldsymbol{\varphi}$ value evaluated from a well-interleaved system is given in Eq. (II-40).

$$\boldsymbol{\varphi} = -\boldsymbol{L\,\theta} = [-0.5 \quad 0.0 \quad 0.0 \quad 0.0 \quad 0.5]^T \tag{II-40}$$

The sum of all the elements of the $\boldsymbol{\varphi}$ vector is null. This vector has always the same shape and can be generalized for any value of $N$. Any of its $N$ rotations $\boldsymbol{S}^i\,\boldsymbol{\varphi}$, $i = 0 \ldots N-1$, is a valid vector, only the discontinuity is moved. The PD discontinuity is in between its non-null values, in this case between the $5^{th}$ and the $1^{st}$. Their signs define if the PD values are in an increasing or decreasing sequence. In the real system, each $\varphi_i$ value is evaluated locally in real time in the $i^{th}$ PDLC, taking into account the local and the neighbors' PDs. For this reason, special attention has to be paid to the initial values of the PDs to obtain a proper $\boldsymbol{\varphi}$ vector and avoid any mistake in the interleaving.

Figure II-16 shows another case where the system is well interleaved but all the PDs are shifted by −0.2 units. It uses the same $\boldsymbol{\varphi}$ vector described in Eq. (II-40). As shown, the discontinuity position is no longer around zero, and $\theta_1$ may be smaller than zero. Thus, some PDs values may be now outside the range from 0 to 1.

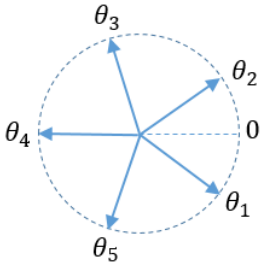



*Figure II-16 – Correct interleaving obtained using the $\boldsymbol{\varphi}$ vector (some PDs values are outside the range [0, 1]).*

Eq. (28) shows the solution for $\boldsymbol{\theta}$ and $\boldsymbol{\varphi}$ related to Figure II-16.

$$\boldsymbol{\theta} = [-0.1 \quad 0.1 \quad 0.3 \quad 0.5 \quad 0.7]^T \qquad \boldsymbol{\varphi} = [-0.5 \quad 0.0 \quad 0.0 \quad 0.0 \quad 0.5]^T \qquad \text{(II-41)}$$

A negative value is obtained because a second operator is required to keep each PD in the range [0, 1]. It is called the "*modulo operator*" and gives a positive remainder after division by 1 (normalized value, equivalent to 360° or 2π). The *modulo operator* removes 1 if the value is higher than 1 and adds 1 if the value is smaller than 0.

The updated $\boldsymbol{\theta}$ and $\boldsymbol{\varphi}$ vectors are shown in Eq. (II-42). All PD values in $\boldsymbol{\theta}$ are now in the range [0, 1], and $\boldsymbol{\varphi}$ is updated. Both vectors are circularly shifted of one element to the right with respect to $\boldsymbol{\theta}$ and $\boldsymbol{\varphi}$ in Eq. (II-38) and Eq. (II-40), respectively. Any circularly shifted version of these vectors is valid. The amount of zero elements in sequence in the $\boldsymbol{\varphi}$ vector has to be equal to $N - 2$.

$$\boldsymbol{\theta} = [0.9 \quad 0.1 \quad 0.3 \quad 0.5 \quad 0.7]^T \qquad \boldsymbol{\varphi} = [0.5 \quad -0.5 \quad 0.0 \quad 0.0 \quad 0.0]^T \qquad \text{(II-42)}$$

The whole algorithm implemented in the local controller is shown in the flowchart of Figure II-17. The first condition prevents undesired disturbances during start-up, when neighboring PD can be coincident. It can be seen in [22], during start-up, the PD in phase opposition is moving while it remains correctly in the middle of its neighbors. This condition makes PD in phase opposition constant only at the beginning, achieving better transient response and avoiding undesired disturbances. When neighboring PD are different, the target PD is corrected depending on the neighboring PD arrangement and on the local PD.

The discontinuity handler adjusts the target value. It is trigged when the neighbors PDs are in a decreasing ordering, i.e. $\theta_P > \theta_N$. Then a correction is made based on the local PD value. It should be noted the target value can be outside the PD normal range. It happens when

the PD has to cross the discontinuity. After the control routine, i.e. error calculation and correction, the modulo operator is applied to keep the local PD in the expected range.

With all these precautions, the PD discontinuity around 1 and 0 is overcome and considered as if it does not exist. In the simulations, the $\boldsymbol{\varphi}$ vector is kept constant and the second operator is applied using post-processing.

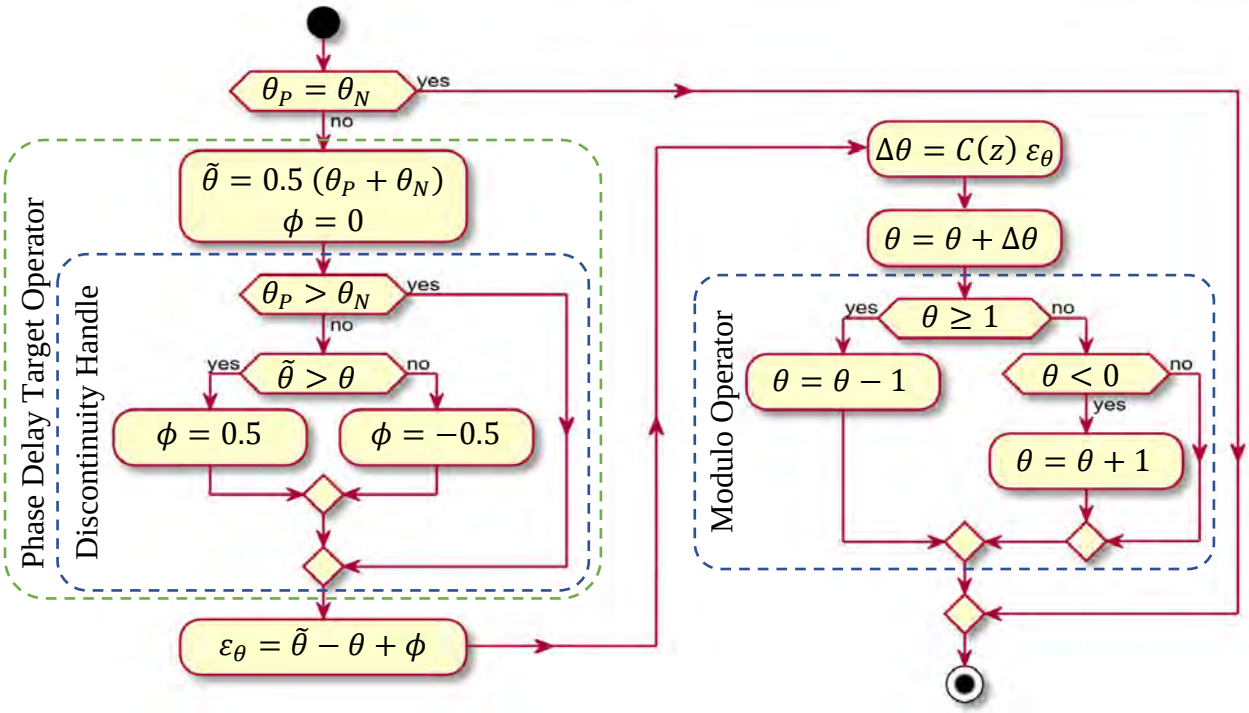



*Figure II-17 – Phase-delay Local Controller Flowchart.*

Figure II-18 (a) and (b) show other cases where the phase differences are equal to 2/*N*. In the case (a), as the number of elements is odd, the system seems to be well interleaved. In case (b), in contrast, where the number of elements is even, there is an evident interleaving problem because some PDs are coincident. This issue appears if the phase differences (1/N) are multiplied by any integer in between 2 and *N*. In the limit case, for any *N* value, all PDs are coincident, i.e. the phase differences are equal to 1 (or zero) and no interleaving effect is observed.


*Figure II-18 – Interleaving issue when phase differences are equal to 2/N: a) N odd case (N = 5), b) N even case (N = 6).*

Multiple solutions for $\boldsymbol{\theta}$ and $\boldsymbol{\varphi}$ in case (b) can justify this arrangement. Two cases are shown in Eq. (II-43) and Eq. (II-44). A wrong interleaving with successive PD differences of 2/*N* is observed in both cases. The first one is not possible because the error operator would not allow to compensate ±0.5 twice in the $\boldsymbol{\varphi}$ vector. The second one, however, is possible. This shows the presence of two discontinuities because two sequences ±0.5 are present in the $\boldsymbol{\varphi}$ vector.

$$\boldsymbol{\theta} = [0.1 \quad 0.5 \quad 0.9 \quad 1.3 \quad 1.7]^T \qquad \boldsymbol{\varphi} = [-1.0 \quad 0.0 \quad 0.0 \quad 0.0 \quad 1.0]^T \qquad \text{(II-43)}$$

$$\boldsymbol{\theta} = [0.1 \quad 0.5 \quad 0.9 \quad 0.3 \quad 0.7]^T \qquad \boldsymbol{\varphi} = [-0.5 \quad 0.0 \quad 0.5 \quad -0.5 \quad 0.5]^T \qquad \text{(II-44)}$$

To ensure a correct interleaving, the $\boldsymbol{\varphi}$ vector has to contain only one discontinuity (±0.5 values). So special care has to be taken during start-up and reconfigurations to avoid going to these states. To do so, the PD values have to be in an ascending order where coincident values can be tolerated. Concerning a reconfiguration during operation, the bypass of a deactivated PDLC is simple because the system normally is already correctly interleaved and so ordered. On the other hand, in order to anticipate an insertion of a "sleeping" PDLC, its PD has to be pre-positioned between its neighboring PDs to anticipate an insertion, such as it being active but not visible.

The start-up disposition of the PDs requires also special care to obtain correct interleaving. The expression on Eq. (II-45) generalizes the condition to obtain an ideal start-up condition that leads to correct interleaving arrangement, where the summation represents the sum of true statements. The cases that respects this condition are called a "Proper Interleaving Arrangement" (PIA). It consists on having only one PD that is not in a non-strict growing sequence, i.e. the next PD greater than or equal to the local PD. In a PIA, the only elements that do not respect this rule are the ones close to the phase-delay discontinuity.

$$\sum_{i=1}^{i=N} \theta_i > \theta_{iNext} = 1 \qquad \begin{cases} \theta_{iNext} = \theta_{i+1}, & if\ i < N \\ \theta_{iNext} = \theta_1, & if\ i = N \end{cases} \qquad \text{(II-45)}$$

This concept can also be applied in steady-state arrangements. It can be noted that the arrangements on Figure II-15 (a) and Figure II-16 are PIA because only $\theta_5 > \theta_1$ and $\theta_1 > \theta_2$, respectively. It can be noted that the arrangements on Figure II-18 are not PIA because in (a) $\theta_3 > \theta_4$ and $\theta_5 > \theta_1$ and in (b) $\theta_3 > \theta_4$ and $\theta_6 > \theta_1$. So the summation in (II-45) is higher than 1. Examples of these cases will be given in the next section.

## II.6. Convergence and steady-state value

It is well understood now that the steady-state value depends on the target vector $\boldsymbol{\varphi}$, which, in turn, depends on the vector $\boldsymbol{\theta}$. The vector $\boldsymbol{\varphi_0}$ is constant if the vector $\boldsymbol{\theta}$ is properly chosen at the beginning, then the $\boldsymbol{\varphi}(z)$ signal is expressed in Eq. (II-46).

$$\boldsymbol{\varphi}(z) = z\,/(z-1)\,\boldsymbol{\varphi_0} \tag{II-46}$$

In this way, as this system is causal, the value $\boldsymbol{\theta}$ converges in steady-state towards the value $\boldsymbol{\theta_{ss}}$ that can be calculated using the Final Value Theorem (FVT) if all differential modes are damped and the $\boldsymbol{\varphi}(z)$ common mode is limited. The mathematical expression to calculate the steady-state value for this discrete system is shown in Eq. (II-47).

$$\boldsymbol{\theta_{ss}} = \lim_{k\to\infty} \boldsymbol{\theta}^k = \lim_{z\to 1} (z-1)\,\boldsymbol{\theta}(z) \tag{II-47}$$

When in steady-state, $\boldsymbol{\varphi}(z)$ is constant and its common mode is null i.e. $sum(\boldsymbol{\varphi}) = 0$, the result in Eq. (II-48) is found by inserting Eq. (II-10) in Eq. (II-47) and solving.

$$\boldsymbol{\theta_{ss}} = \overline{\boldsymbol{\theta_0}} - \boldsymbol{L}^{+}\,\boldsymbol{\varphi_0} \tag{II-48}$$

where $\overline{\boldsymbol{\theta_0}} = 1/N\ \mathbf{1}_{NxN}\,\boldsymbol{\theta_0}$ is a vector in which each element is the average value of $\boldsymbol{\theta_0}$, and $\boldsymbol{L}^{+}$ is the pseudo-inverse of $\boldsymbol{L}$. It should be noted that the matrix $\boldsymbol{L}$ is singular because one eigenvalue is null and has no inverse. $\boldsymbol{L}^{+}$ can be evaluated using Eq. (II-49).

$$\boldsymbol{L}^{+} = \boldsymbol{W}\,\boldsymbol{\Lambda}^{+}\,\boldsymbol{W}^{-1} \tag{II-49}$$

where $\boldsymbol{\Lambda}^{+}$ is formed from $\boldsymbol{\Lambda}$ by taking the reciprocal of all the non-zero elements.

Eq. (II-48) reveals that, as expected, the steady-state depends on the start-up configuration $\boldsymbol{\theta_0}$ that provides also $\boldsymbol{\varphi_0}$, and, more importantly, on $\boldsymbol{L}^{+}$ that comes from the communication chain configuration matrix $\boldsymbol{L}$. The steady-state value does not depend on the corrector $\boldsymbol{C}(z)$. It should be noted that if $\boldsymbol{\theta_{ss}}$ is outside the range 0 to 1, the correct result is obtained by applying the modulo operator to each value.

## II.7. Reconfiguration and start-up simulations

As soon as the state of a PDLC changes, activated to be inserted into or deactivated to be removed from the chain, the remaining PDLCs have to modify their PDs to reach a new steady-state disposition where all the carriers are correctly interleaved again. The behavior of the several PDs in reaction to a reconfiguration event has to be studied carefully. A reconfiguration event excites the different modes, and the convergence towards the correct interleaving must be guaranteed. One can notice that these simulations of reconfiguration proposed here illustrate a real case of a decentralized interleaving operation.

The following simulations are performed using the lead-lag controller presented earlier. As the phase-delay target operator cannot be implanted in Matlab when using annexed code, the $\boldsymbol{\varphi}$ vector is predefined to a convenient value using pre-processing, and the modulo operator is applied using post-processing. The reconfiguration responses are analyzed hereafter, first with the removal case, followed by the insertion case and then with the specific case studies of start-up.

### II.7.1. PDLC removal

The simulation of a reconfiguration proposed here illustrates the cases of a PDLC removal (the PDLC is bypassed). The removal is the simplest reconfiguration case because the system is already interleaved and there is no initial value to care about.

Figure II-19 shows two reconfiguration simulations starting with nine well-interleaved PDLCs. The PDLC3 is disabled and bypassed at the first iteration, then the eight remaining active PDLCs reconfigure and reach another interleaving state. These eight PDLCs have the same dynamics revealed previously. Figure II-19 (a) shows the reconfiguration response with $\alpha$ = 1, and Figure II-19 (b) shows the reconfiguration response with $\alpha$ = 6/5.

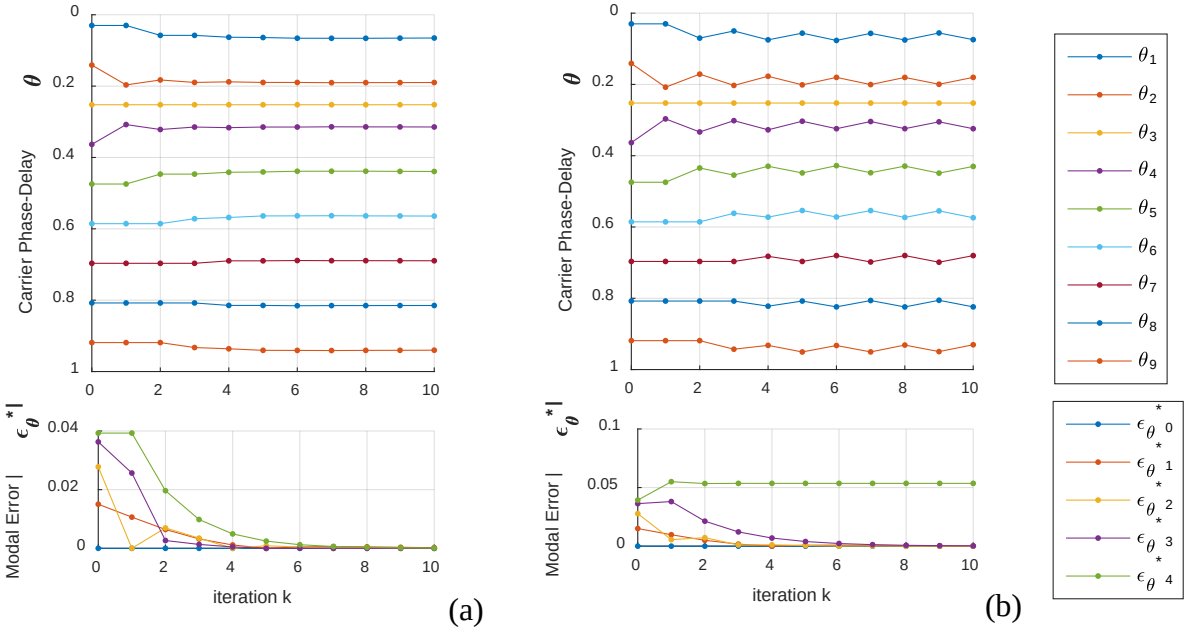



*Figure II-19 – Reconfiguration response (N from 9 to 8): Local Controller 3 is bypassed, a) α = 1, b) α = 6/5.*

As expected, the system converges towards a new state of appropriate interleaving and the disabled PDLC, the sleeping one, continue to adjust its own PD to centralize its position between its neighbors. The simulations show that all differential modes are excited at the beginning. All modes are damped with respect to the values of Table I. In (a), all components of $|\boldsymbol{\varepsilon_\theta}^*|$ are mitigated very quickly and no particular mode dominates the settling time. In (b),

the mode 4 is at the limit of stability, so $|\varepsilon_\theta{}^*|_4$ is not damped and oscillates indefinitely. These two responses correspond exactly to the expected theoretical modal response detailed previously.

### II.7.2. PDLC insertion

The simulation of a reconfiguration event proposed here illustrates the cases of a PDLC insertion, i.e. a previously bypassed sleeping PDLC becoming visible to its neighboring PDLCs in the communication chain. This event also excites all the different modes, and the convergence towards the correct interleaving must be guaranteed.

Figure II-20 shows two reconfiguration simulations with eight PDLCs. At the beginning, seven PDLCs are well interleaved, and PDLC5, pre-positioned or not, is inserted. These eight PDLCs have the same dynamics as those revealed previously with $\alpha$ = 1 to ensure stability. Figure II-20 (a) shows the reconfiguration response where PD5 is pre-positioned in between its neighbors, and Figure II-20 (b) shows the case where its initial value is null.

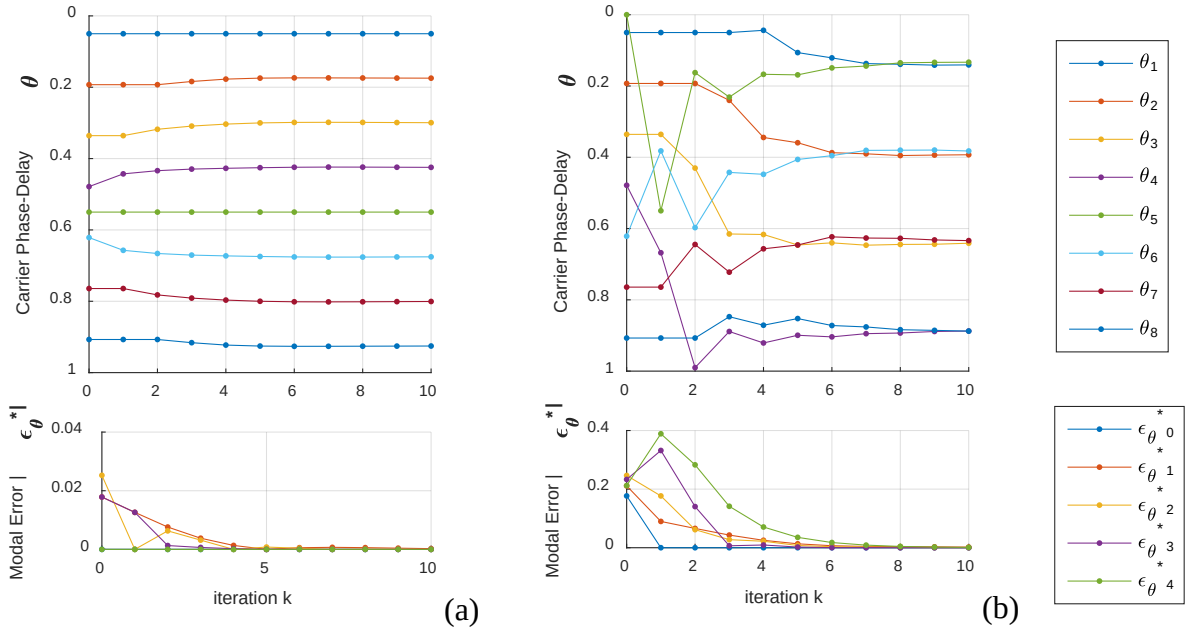



*Figure II-20 – Reconfiguration response (N from 7 to 8, α = 2/3): Local Controller 5 is inserted a) in the middle of its neighbors, b) with a null starting value.*

The simulations show in Figure II-20 (a) and (b) the PDs converge either to a good and wrong steady-state with phase differences of 1/N and 2/N, respectively. The correct interleaving state is reached in Figure II-20 (a) because $\theta_5$ is pre-positioned. Consequently, $\boldsymbol{\varphi}(z)$ keeps a constant value $\boldsymbol{\varphi_0}$. On the other hand, this is not the case in Figure II-20 (b). The null starting value of $\theta_5$ disturbs PDLC4's phase-delay target operator, and that disturbance causes a nonconforming modification in $\boldsymbol{\varphi}$. After the first iteration, PDLC5's phase-delay target

operator is also disturbed because $\theta_4$ and $\theta_6$ cross each other and modify again $\boldsymbol{\varphi}$. These $\boldsymbol{\varphi}$ values lead to a wrong interleaving arrangement.

As a conclusion, to avoid wrong interleaving arrangements, at the beginning of a reconfiguration event, the $\boldsymbol{\theta}$ vector has to respect a specific shape to generate a proper $\boldsymbol{\varphi}$ vector. To do so, inactive PDLCs (bypassed) have to keep their PD computations active and correctly positioned in between their neighbors.

### II.7.3. Convergence behavior vs. start-up positions

Now that reconfiguration events, insertion and removal cases, have been considered, it is important to focus on the stat-up of the system. Indeed, depending on the original positions of the carrier, the system may or not converge towards the appropriate interleaving. Several start-up cases have to be considered. Figure II-21 shows in (a) a classical start-up procedure such as the one described in [21], [22], [28] where one PD is put in phase opposition to the others. It shows in (b) an alternative start-up procedure where the PDs are put in two separate groups. The starting values are chosen to avoid $\boldsymbol{\theta}$ values going outside the range 0 to 1 and then to avoid any changes in the $\boldsymbol{\varphi}$ vector.

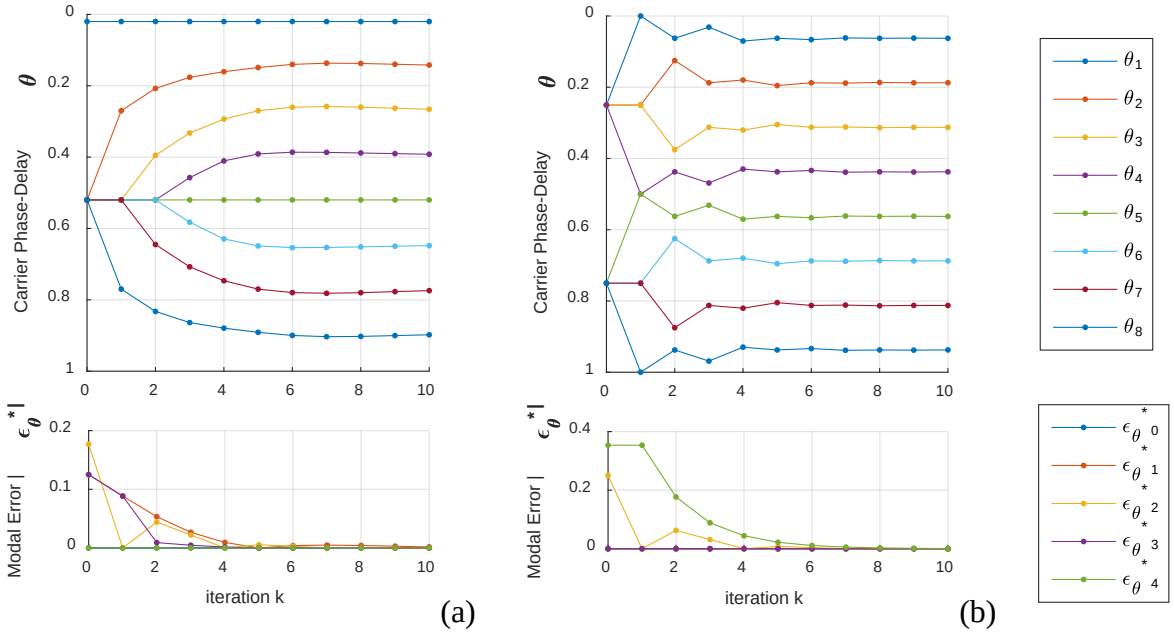



*Figure II-21 – Start-up response (N = 8): a) one element in phase opposition (1+7), b) with two separated groups (4+4).*

In both cases the convergence is ensured and the settling times are slightly different. Indeed, the $\boldsymbol{\theta}$ values at the beginning determine the disturbed modes. In case (a), the differential modes 1, 2 and 3 are disturbed, while in case (b), the differential modes 2 and 4 are disturbed. The correct steady-state interleaving is reached in both cases and the global settling times are similar because their modal settling times are quite uniform. A slow mode can be avoided to

optimize the settling time, e.g. chose case (b) if the mode 1 is the slower, choose (a) if mode 4 is the slower. As case (a) does not disturbs the mode 4, it would converge even if mode 4 is at the limit of stability.

The case (b) brings redundancy because more than one PD can be considered in phase opposition. It is an important feature for fault tolerant systems and gives more flexibility during start-up.

## II.8. Freeze a carrier phase-delay

In some applications using the proportional controller [21], [22], [35], one PD is freeze (cannot change value) to overcome instability with $\alpha = 1$. Other applications have specific requirements to avoid noise issues. For example, one PD is imposed to overcome the impact of the switching noise. An imposed carrier position may be required by applications using an external clock with synchronous requirements. This section introduces the eigenvalue study, the time response and its dynamic analysis for the case with one PD kept constant.

When the original position of a carrier is imposed and permanent, its local controller gain is null and its PD is no longer computed. The computations made inside its PDLC are turned off. It is equivalent to canceling the terms of the corresponding row of the $\boldsymbol{L}_{\mathrm{N}}$ matrix. The communication chain configuration with six carriers ($N = 6$), where $\theta_1$ is constant, is named $\boldsymbol{L}_{6-1}$ and expressed in Eq. (II-50).

$$\boldsymbol{L}_{6-1} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0.5 & -1 & 0.5 & 0 & 0 & 0 \\ 0 & 0.5 & -1 & 0.5 & 0 & 0 \\ 0 & 0 & 0.5 & -1 & 0.5 & 0 \\ 0 & 0 & 0 & 0.5 & -1 & 0.5 \\ 0.5 & 0 & 0 & 0 & 0.5 & -1 \end{bmatrix} \tag{II-50}$$

The $\boldsymbol{L}_{\mathrm{N}-1}$ eigenvalues are real, ranging between $-2$ and 0. It is no longer circulant, so the diagonalization matrix $\boldsymbol{W}$ is not the DFT matrix anymore. Then, the concepts of common mode and sinusoidal components are no longer valid. The eigenvalues of $\boldsymbol{L}_{\mathrm{N}-1}$ can be computed using Eq. (II-51) for any $N$ value. This expression is not proven analytically.

$$\lambda_i = \cos\frac{\pi\, i}{N} - 1, \qquad i = 0 \ldots N-1 \tag{II-51}$$

There are two differences to the general case. The first one is all modes are simple, no double modes. As a result, $M$ is equal to $N$. The second difference is that $\lambda_i$ is never equal to 2 ($-2 < \lambda_i < 0$). So the general stability criterion upper limit becomes non strict, i.e. $\alpha$ can be equal to the upper limit and the system is still stable with $N$ even, as shown in Eq. (II-52).

$$0 < \alpha \leq \frac{1 + p_{OL}}{1 + z_{OL}} \quad \Leftrightarrow \quad \begin{matrix} 0 \leq z_{OL} \leq p_{OL} \leq 1 \\ p_{OL} - z_{OL} < 1 \end{matrix} \tag{II-52}$$

### II.8.1. Proportional corrector

For the proportional corrector, the modal poles, i.e. eigenvalues, can still be easily evaluated as a function of α by Eq. (II-28). The eigenvalues $\lambda_{Ai}$ of the differential modes $(i = 1 \ldots N-1)$ can be computed as previously and are shown in Figure II-22 for $N$ going from 5 to 8. The important major difference is the system is unconditional stable even if α is equal to 1.

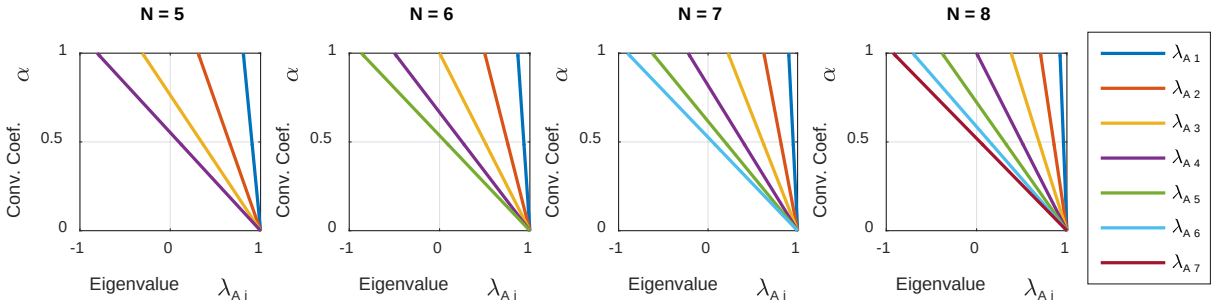



*Figure II-22 – One constant PD: Eigenvalues vs. Convergence Coefficient for N from 5 to 8.*

Table II-3 presents the iteration number for convergence for the case with $N = 8$ and one PD constant, for $\alpha$ equal to 1, 3/4 and 1/2. The last mode, mode 7 in this case, is stable and no longer in stability limit with $\alpha = 1$ for any $N$ value. However, mode 1 is almost 4 times slower than the case where PD can change values.

*Table II-3 – Iteration number for 5% response ($N = 8$) with one PD constant.*

| | $k_{5\%\_7}$ | $k_{5\%\_6}$ | $k_{5\%\_5}$ | $k_{5\%\_4}$ | $k_{5\%\_3}$ | $k_{5\%\_2}$ | $k_{5\%\_1}$ |
|---|---|---|---|---|---|---|---|
| α = 1 | 39 | 9.4 | 4.1 | 1 | 4.1 | 9.4 | 39 |
| α = 3/4 | 3.7 | 2.4 | 0.9 | 2.2 | 4.8 | 12 | 51 |
| α = 1/2 | 1.9 | 2.6 | 3.5 | 5.3 | 9.1 | 20 | 78 |

Table II-3 presents the same pattern seen in Table II-1, and all the previous observations are still valid, such as the convergence of the overall system depends on the type of modes that are excited.

### II.8.2. Reconfiguration response

Figure II-23 shows two simulation results using the same conditions described previously, but $\theta_1$ is constant to 0. At the first iteration, PDLC3 is removed from the chain of communications. As PDLC1 provides a constant PD, its error is never corrected locally (blue line), and the other PDs have to change their value to cancel their own local error, and consequently PDLC1 error. In case (a), $|\varepsilon_\theta{}^*|_7$ is quickly reduced to zero while $|\varepsilon_\theta{}^*|_1$ dominates

the response. Indeed, it is much slower than the other modes. In case (b), $|\varepsilon_\theta{}^*|_1$ and $|\varepsilon_\theta{}^*|_7$ have the same convergence speed, but $|\varepsilon_\theta{}^*|_7$ has a much higher disturbance at start-up, so it dominates the response. No sustained oscillation is observed, confirming the unconditional stability of this approach.

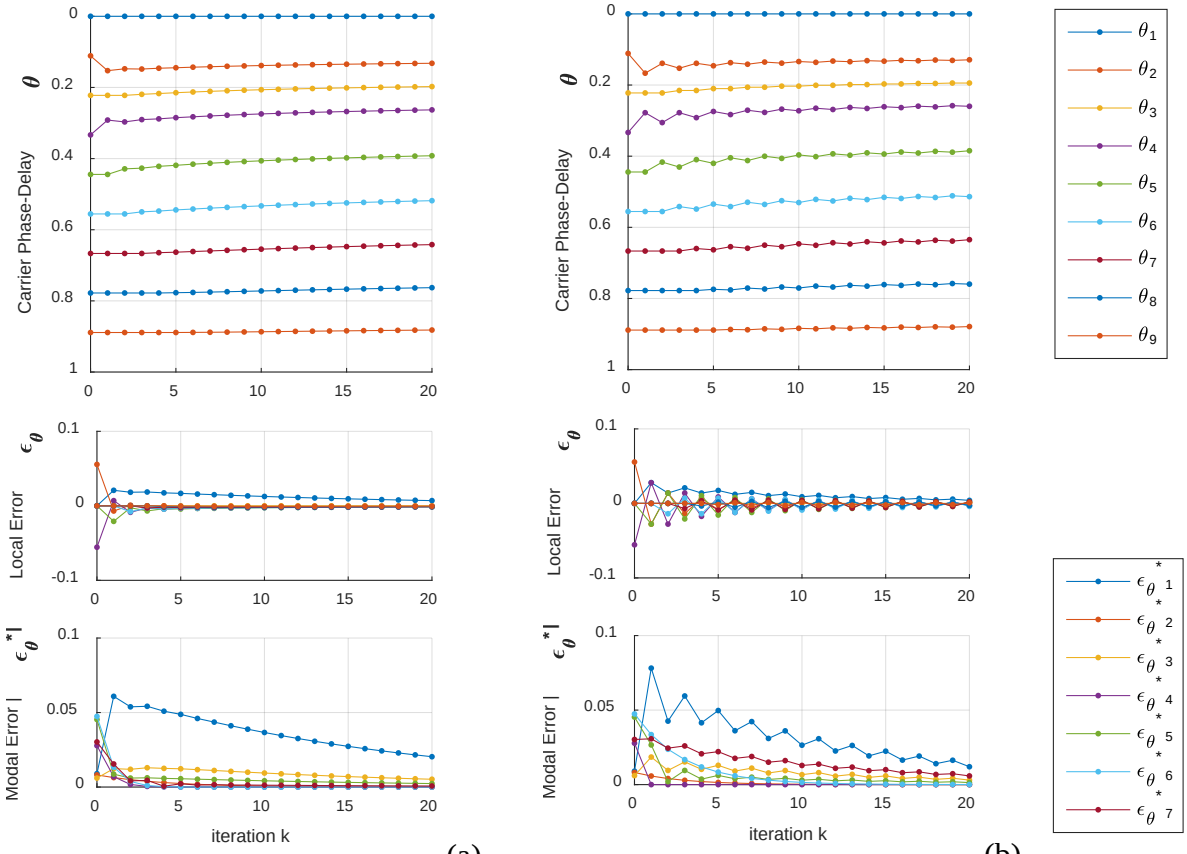



*Figure II-23 – Reconfiguration response: PD1 $\theta_1$ is constant, and PDLC3 is disabled and bypassed ($N = 8$), a) $\alpha = 3/4$, b) $\alpha = 1$.*

## II.9. **Multiple circular chains**

Others circular chain arrangements can be used to improve redundancy or settling time. Instead of looking at only the close neighbors, each PDLC could have access to the second neighbors or third neighbors in the chain and try as well to place the local PD in between their PDs. Figure II-24 show an alternative configuration where a connection with the $j^{th}$ neighbors is used. To simplify the formulation, a common corrector $C(z)$ is used and a particular gain is introduced in each feedback loop. It should be noted that multiple different correctors could be associated with the gains $k_n$.

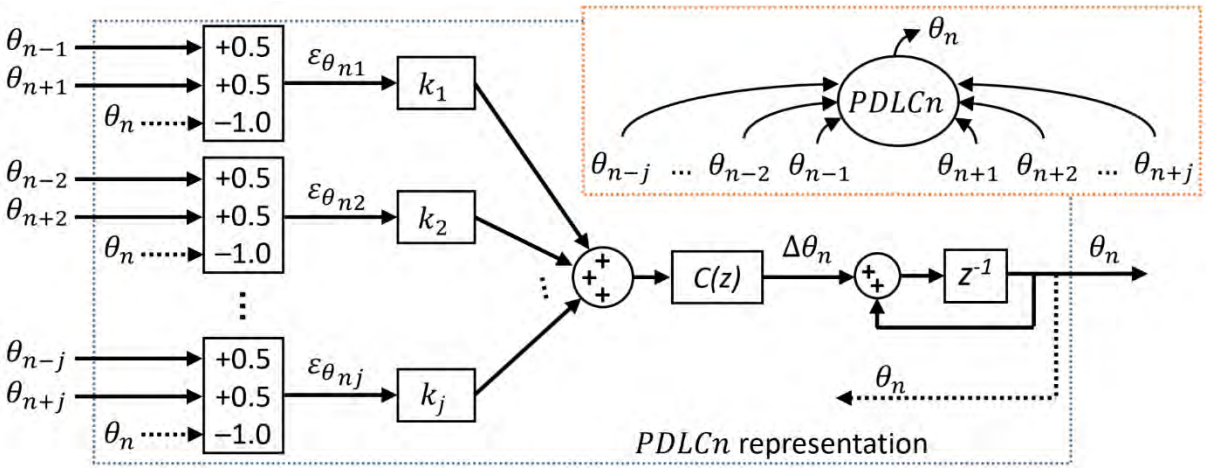



*Figure II-24 – PDLC with multiple feedback and its representation with a common corrector $C(z)$.*

Eq. (II-53) is the open-loop discrete transfer function in the Z-domain.

$$\frac{\boldsymbol{\theta}(z)'}{\boldsymbol{\theta}(z)} = -\left(k_1 \boldsymbol{L}^1 + k_2 \boldsymbol{L}^2 + \cdots + k_J \boldsymbol{L}^J\right) \frac{1}{z-1} C(\mathrm{z}) = -\sum_{\mathrm{j}=1}^{J=N} k_j \boldsymbol{L}^j \frac{1}{z-1} C(\mathrm{z}) \qquad \text{(II-53)}$$

where $k_\mathrm{j}$ are the gains associated to the $j^{th}$ neighbor connection, i.e. the error related to the $j^{th}$ neighbors.

The gain $k_\mathrm{j}$ is normally a positive real number or equal to zero when the connection is not used or not available. $\boldsymbol{L}^\mathrm{j} = 0.5\left(\boldsymbol{S}^{-\mathrm{j}} + \boldsymbol{S}^\mathrm{j}\right) - \boldsymbol{I}$ and its diagonal form is $\boldsymbol{\Lambda}^\mathrm{j} = \boldsymbol{W}^* \boldsymbol{L}^\mathrm{j} \boldsymbol{W} = 0.5\left(\boldsymbol{U}^{-\mathrm{j}} + \boldsymbol{U}^\mathrm{j}\right) - \boldsymbol{I}$. It shall be noted the terms $j$ in $\boldsymbol{L}^\mathrm{j}$ and $\boldsymbol{\Lambda}^\mathrm{j}$ are not powers of $\boldsymbol{L}$ and $\boldsymbol{\Lambda}$, even if $\boldsymbol{L}^1 = \boldsymbol{L}$ and $\boldsymbol{\Lambda}^1 = \boldsymbol{\Lambda}$. It can be shown the $i^{th}$ diagonal element of $\boldsymbol{\Lambda}^\mathrm{j}$ noted $\lambda_i^j = \cos\frac{2\,\pi\,i\,j}{N} - 1$.

The homogeneous system closed-loop discrete transfer function ( $\boldsymbol{\varphi}(z) = 0$ ) is represented by Eq. (II-54).

$$\boldsymbol{\theta}(z) = \left[z\boldsymbol{I} - \left(\boldsymbol{I} + C(z) \sum_{\mathrm{j}=1}^{J=N} k_j \boldsymbol{L}^j\right)\right]^{-1} z\boldsymbol{I}\,\boldsymbol{\theta_0} \qquad \text{(II-54)}$$

The CLTF on Eq. (II-54) can also be written in a diagonal form such as in Eq. (II-55). The diagonalization is made using the DFT matrix, as shown previously.

$$\boldsymbol{\theta}^*(z) = \left[z\boldsymbol{I} - \left(\boldsymbol{I} + C(z) \sum_{\mathrm{j}=1}^{J=N} k_j \boldsymbol{\Lambda}^j\right)\right]^{-1} z\boldsymbol{I}\,\boldsymbol{\theta_0}^* \qquad \text{(II-55)}$$

Eq. (II-55) can be rewritten as $N$ independent transfer functions as shown in Eq. (II-56) because all matrices in Eq. (II-55) are diagonal.

$$\theta^*{}_i(z) = \frac{z}{z - \left(1 + C(z)\sum_{\mathrm{j}=1}^{J=N} k_j\,\lambda_i^j\right)}\;\theta_0{}^*{}_i, \qquad i = 0 \ldots N-1 \tag{II-56}$$

It is known that all $\lambda_i^j$ are comprised between –2 and 0 ($-2 \le \lambda_i^j < 0$). The general stability criterion for the previously presented controllers is shown in Eq. (II-57).

$$0 < \sum_{\mathrm{j}=1}^{J=N} k_j < \frac{1 + p_{OL}}{1 + z_{OL}} \quad \Leftrightarrow \quad \begin{array}{c} 0 \le z_{OL} \le p_{OL} \le 1 \\ p_{OL} - z_{OL} < 1 \\ \alpha = 1, \qquad k_j \ge 0 \end{array} \tag{II-57}$$

If pushed to the limit, this approach consists in using Full State Feedback (FSF) offering the possibility to implement any closed-loop behavior. At last, this approach is no longer considered because modular aspect would be lost and the complexity of the communication network, i.e. the number of connections involved in the global system, increases drastically.

### II.9.1. Settling time

In the approach previously presented, the lower modes are normally slower because their related eigenvalues are closer to zero (smaller in absolute value). When using a second circular chain, other set of modes can be privileged. The controller can be simplified to $C(z) = 1$ to compare this approach with the proportional controller previously presented. The modal pole values in the general case with $C(z) = 1$ are shown in Eq. (II-58).

$$\lambda_{Am} = 1 + \sum_{\mathrm{j}=1}^{J=N} k_j\,\lambda_m^j = 1 + k_1\,\lambda_m^1 + k_2\,\lambda_m^2 + \cdots k_J\,\lambda_m^J, \qquad m = 0 \ldots M-1 \tag{II-58}$$

where $\lambda_m$ are the diagonal elements of $\boldsymbol{\Lambda}$ and $k_j$ is the gain associated with the $j^{th}$ neighbors connection.

To illustrate this, a system with nine PDLCs ($N = 9, M = 5$) with a second circular chain is proposed, where each PDLC is communicating with the third neighbors in the chain. For the proportional controller $C(z) = 1$, the modal poles are defined in Eq. (II-59).

$$\lambda_{Am} = 1 + k_1\,\lambda_m^1 + k_3\,\lambda_m^3, \qquad m = 1 \ldots M-1 \tag{II-59}$$

This expression can be compared with the case where only the first neighbor circular chain was used, shown in Eq. (22). It can be noted $k_1$ is equivalent to α and $\lambda_m^1$ is equal to $\lambda_m$ itself. An additional freedom degree linked with the third neighbor connection $k_3$ can be noted.

Table 1 shows the number of iterations required for convergence of the several differential modes in the cases of Figure II-24.

*Table II-4 – Number of iterations for 5% response ($N = 9$).*

| | $k_{5\%\_4}$ | $k_{5\%\_3}$ | $k_{5\%\_2}$ | $k_{5\%\_1}$ |
|---|---|---|---|---|
| $k_1 = 0.6, k_3 = 0.1$ | 2.6 | 1.3 | 2.9 | 8.7 |
| $k_1 = 0.4, k_3 = 0.3$ | 2.0 | 3.3 | 2.0 | 3.2 |
| $k_1 = 0.1, k_3 = 0.6$ | 1.3 | 18 | 0.7 | 1.2 |
| $k_1 = 0, k_3 = 2/3$ | 0 | $+\infty$ | 0 | 0 |

The table shows the modes 1, 2 and 4 go faster as $k_1$ goes down to zero and $k_3$ goes up to 2/3. However, the mode 3 slows down and become uncontrollable when $k_1 = 0$ because $\lambda_3^3 = 0$, i.e. $\lambda_{A3}$ is not dependent on $k_3$.

### II.9.2. Convergence behavior

A particular convergence behavior can be noted when $k_3$ is privileged over $k_1$. Figure II-25 shows two start-up simulations, in (a) for the case ($k_1 = 0.4$, $k_3 = 0.3$) and in (b) for the case ($k_1 = 0.1$, $k_3 = 0.6$).

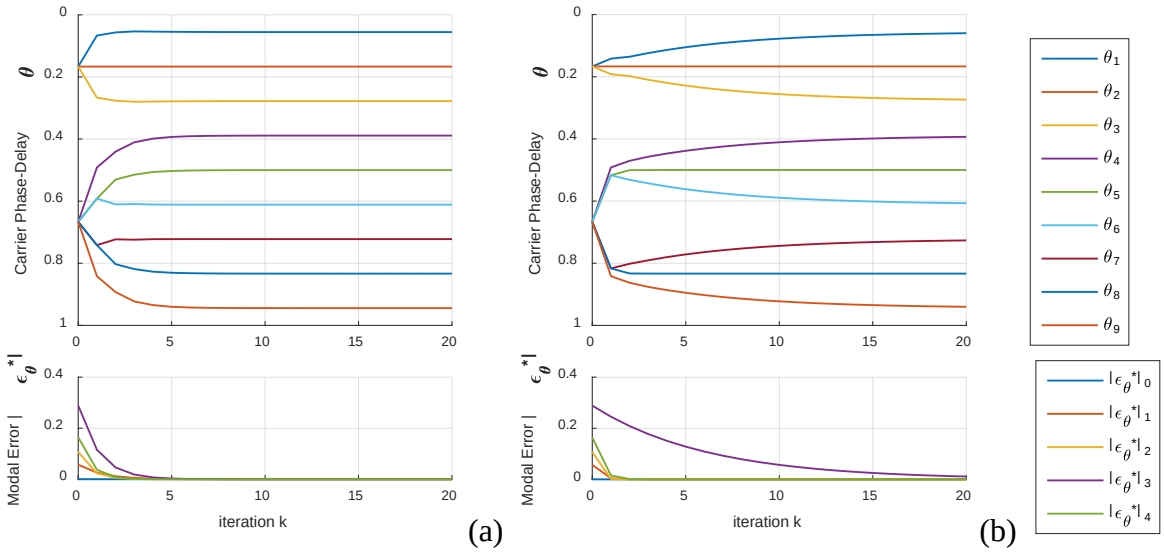



*Figure II-25 – Start-up simulation ($N = 9$), (1+8): a) $k_1 = 0.4$, $k_3 = 0.3$, b) $k_1 = 0.1$, $k_3 = 0.6$.*

The PDs reach the expected interleaving very fast in the case (a). However, in case (b) the PDs reach the expected interleaving very fast with their third neighbor because $k_3$ ($j = 3$) is privileged. As $N = 9$, three well interleaved groups ($N/j$) are formed. When the remaining disturbed modes are damped, mode 3 in this case, all PDs are well interleaved.

### II.9.3. Reconfiguration

This special circular chain is not suitable for reconfiguration. When a PDLC is bypassed, besides sending the previous and next neighbor's PDs, it has to maintain the circular chain with

the $j^{th}$ as well. Nevertheless, this is not feasible with the circular chain. It should be noted that changing the topology of the communications network due to reconfiguration event requires for each case a complete and dedicated stability study.

## II.10. Shared wire generalization and discussion

The modeling techniques shown here can also be extrapolated to reveal the stability criteria of a hypothetical system using the shared wire technique. In this case, each LC compares the average value of the PDs shared on a single wire with its local PD. All error can be compute by the specific operator $\boldsymbol{L}$ shown in Eq. (II-60), that is a circulant matrix, and the eigenvalues are revealed.

$$\boldsymbol{L} = \boldsymbol{W}\boldsymbol{\Lambda}\boldsymbol{W}^{*} = \frac{1}{N}\mathbf{1}_{NxN} - \boldsymbol{I} \qquad \lambda_i = \begin{cases} 0, & i = 0 \\ -1, & otherwise \end{cases} \qquad \text{(II-60)}$$

It shall be noted that the common mode cannot be controlled because its first eigenvalue ($i = 0$) is null and all the differential modes have the same transient response because all related eigenvalues are equal.

All modes have the same behavior with the shared wire approach because a disturbance applied in any LC will be seen in an equal manner by all LCs, while in the circular chain, the closest connection LCs will perceive the disturbance earlier than the others.

## II.11. Conclusions

In this chapter, a complete analytical study of a digital iterative distributed interleaving strategy has been developed. It highlights the existence of several modal responses whose number and dynamics depend on the number of carriers involved in the system. The stability criterion has been established for any number of active local controllers used. A convergence speed parameter has been defined to choose an appropriate convergence coefficient value for each application case. Examples have been given to show the resulting modal dynamics for different values of convergence coefficient.

The ability to quickly converge towards the expected steady-state has been demonstrated both for the particular case of system reconfiguration during operation with the removal or the insertion of a local controller and for the case of system start-up with different phase-delay for the carriers. Guidelines for the implementation of the PDLC are provided, ensuring correct steady-state disposition. Recommendations for the reconfiguration and start-up dispositions are also provided with an analytical expression of the dispositions reached after convergence.

The stabilizing effect of using a constant position for one carrier has been also highlighted. In that particular case, an unconditional stability is obtained at the cost of a loss of dynamic performance, even when using the best value for the convergence coefficient. The effect of multiple circular chains is also analyzed and revealed as well as the general case with all elements contributing on a single shared wire.

The robustness of this distributed interleaving strategy is limited due to the shared line needed to share the phase-delay reference, i.e. the shared clock. This also adds the requirement either to provide of an external clock or one LC must send its clock to the others LCs. In the second case, one element would have a feature different to the others, resulting in a singular element and consequently an additional SPOF.

In case of detection of fault occurrence leading to a defective PD communication line, the system can reconfigure to keep constant the phase-delay of the LC that cannot receive the correct information. However, the shared clock remains a concern in terms of SPOF. For that reason, this approach is not recommended for system requiring high availability and mission continuity in case of fault occurrence.

# III. Triangular carrier self-alignment study

The triangular carrier self-alignment modular approach studied in this chapter was first described by COUSINEAU in [28]. It uses only analog circuits to generate interleaved triangular carriers. In this approach, a given number $N$ of Triangular Carrier Generators (TCG), are connected in a circular chain, where each TCG receives the neighboring TCG's triangular waveforms and send them back its own triangular waveform. This approach is modular and suitable to reconfiguration, as inactive TCG bypass its connections in the chain. Figure III-1 shows a schematic view of the several TCGs connected with their neighbors forming a closed chain of inter-module communications. The TCG is composed by three elements, a bypass circuit, a Triangular Signal Generator (TSG) and an adjustable gain differential amplifier ($\beta$) as a controller.

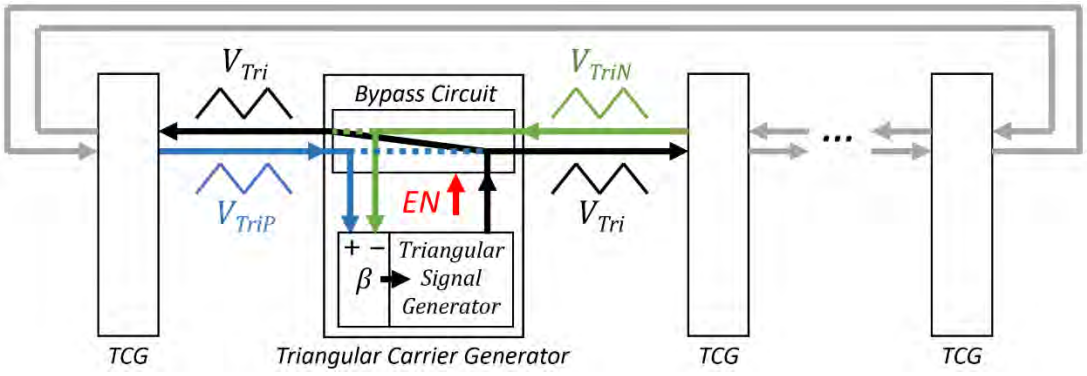



*Figure III-1 – Triangular Carrier Generators exchanging analog waveforms to interleave themselves.*

This approach is different to the numeric interleaving approach previously presented in chapter II. Then a summary list with advantages and disadvantages is given.

Advantages:

- No global clock required;
- Full modularity and no SPOF;
- No phase delay discretization.

Disadvantages:

- Triangular signal shape changes during reconfiguration disturbing the duty-cycle / PWM signal relation;
- Noise immunity issues on analog connections;
- Matching issues on triangular signal (DC level, peak-to-peak amplitude, slew-rate symmetry, frequency).

This system has been implemented in real applications [13] using an structure based on current sources. The experimental results proof its effectiveness. Nevertheless, the complete modelling and stability study has not been already proposed and verified. This study is now detailed hereafter. Besides providing the stability criterion, closed-loop performance constraints (settling time vs. static error) are shown and a settling time optimization procedure is proposed. A limited study reveals the mismatch (frequency, DC level) effect on static error.

## III.1. **Working principle and modeling**

The $i^{th}$ TSG generates a triangular signal $V_{tri\_i}$. It should be noted that, in the following explanations, all signals $V_{tri}$ generated are considered ideal. They are symmetrical, have constant slew-rate value $\pm S_R$ and are bounded by two threshold voltages, a lower limit $vl$ and an upper limit $vh$, resulting in a signal with free running frequency $f_0$, period $T_0$. The $f_0$ expression is shown in Eq. (III-1) when the voltage thresholds are the constant values $V_H$ and $V_L$.

$$f_0 = \frac{0.5\ S_R}{V_H - V_L} \tag{III-1}$$

To obtain interleaved carriers, each module has to place the local triangular signal $V_{tri}$ PD in between its Previous and Next neighboring TCGs triangular signals $V_{triP}$ and $V_{triN}$ phase delays, respectively. It can be obtained by superimposing $V_H$ and $V_L$ with an auxiliary signal $V_{thld}$, where $V_{thld}$ is a factor $\beta$ of the difference of the neighboring triangular signals $V_{triP}$ and $V_{triN}$, shown in Eq. (III-2), generated with the adjustable gain ($\beta$) differential amplifier.

$$V_{thld}(t) = \beta \left(V_{triP}(t) - V_{triN}(t)\right) \tag{III-2}$$

Thus, the generated triangular signal $V_{tri}$ amplitude is modulated, affecting its PD. By geometrical construction, $V_{tri}$ is guided in phase to reach its steady-state position. The control input signal $V_{thld}$ turns the TSG into a Voltage Controlled Oscillator (VCO). This neighbor connections are effectively feedback-loops that lead each triangular signal to center itself in between its two neighbors. When a given number $N \geq 3$ of TCGs are connected together in a circular chain, all PDs are correct and the carriers tend to be located in the middle of its neighbors, resulting in a well interleaved system. Figure III-2 shows the principle of operation waveforms, where $vh(t) = V_H + V_{thld}(t)$ and $vl(t) = V_L + V_{thld}(t)$.

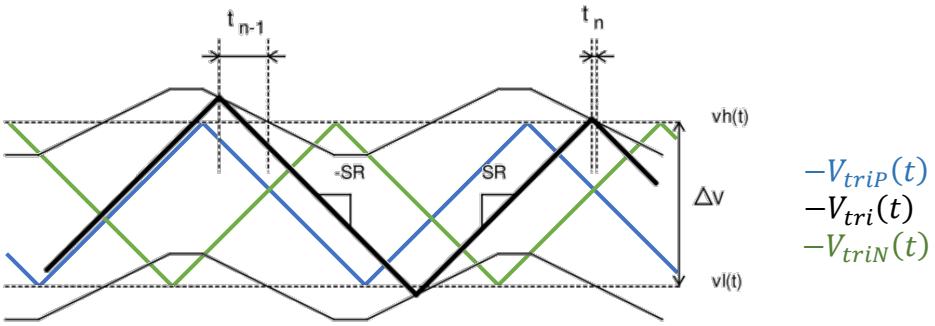



*Figure III-2 – Triangular Carrier Self-Alignment principle of operation, Phase-Advance case reaching a stable position [28].*

### III.1.1. Phase-delay value

A measurement of the triangular signal PD is necessary to reference one carrier PD to the others. The proposed measurement is based on the time delay to a similar reference triangular signal $V_{ref}$ with a constant period $T_0$, as shown by the purple waveform shown in Figure III-3. The triangular signal $V_{tri}$ (in blue) can take values within and beyond $V_L$ and $V_H$. Assuming the triangular signals have the same DC level, the expected time delay $\Delta t_{V_{tri}}$ is the horizontal distance between $V_{ref}$ and the next $V_{tri}$ value with the same slope. A slope projection is used when $V_{tri}$ amplitude is smaller than $V_{ref}$.

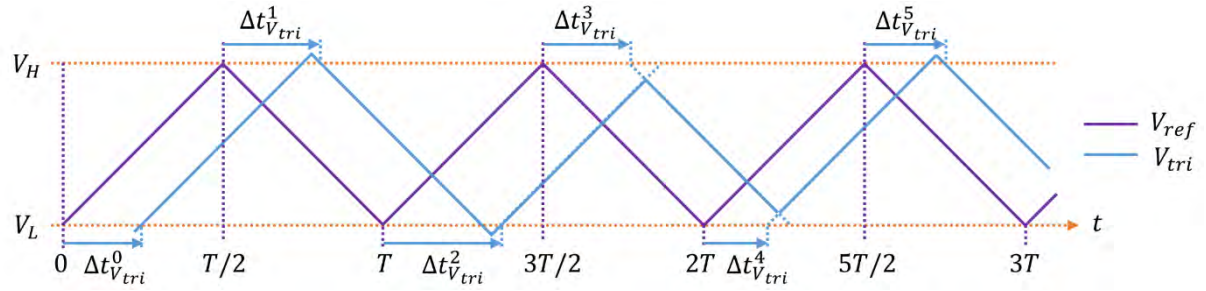



*Figure III-3 – Triangular signal time delay measurement.*

When $V_{tri}$ has a higher amplitude than $V_{ref}$, going out of the $V_L$ to $V_H$ range, then $\Delta t^k_{V_{tri}}$ presents a positive discontinuity and increases with time. When $V_{tri}$ has a smaller amplitude than $V_{ref}$ and does not touch $V_L$ nor $V_H$ levels, then $\Delta t^k_{V_{tri}}$ presents a negative discontinuity and decreases with time.

As the slew rate are considered equal and constant, the PD changes at each commutation of $V_{ref}$, i.e. each change of the slope sign, and is kept constant until the next commutation. Figure III-4 shows the time delay and phase delay plot for modeling with the values shown in Figure III-3.

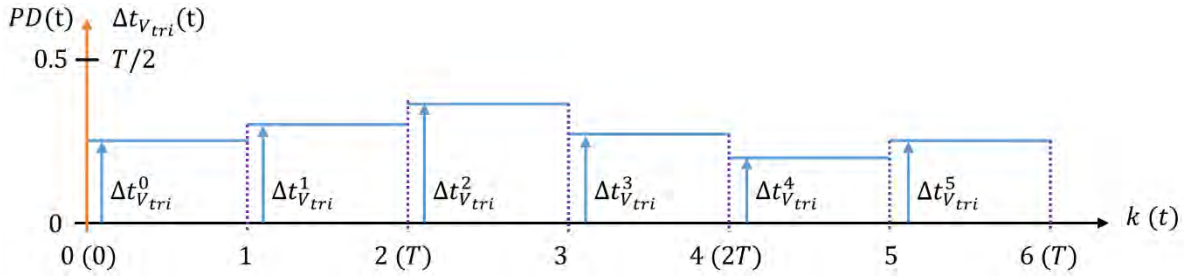



*Figure III-4 – Time delay measurement plot for modeling.*

The resulting $\Delta t_{V_{tri}}(t)$ is similar to a continuous-time waveform reconstruction from a sample sequence $\Delta t^k_{V_{tri}}$using a zero-order hold, such as shown in Eq. (III-3), where $rect(\,)$ is the rectangular function.

$$\Delta t(t) = \sum_{k=-\infty}^{\infty} \Delta t^k_{V_{tri}}\, rect\left(\frac{2\,t - T_0/2 - k\,T_0}{T_0}\right) \qquad \text{(III-3)}$$

The signal $\Delta t_{V_{tri}}(t)$ can be modelled as the output of a linear time-invariant system with impulse response equal to a rectangular function, where the inputs are a sequence of Dirac functions scaled to the sampled values. The sampling frequency is equal to 2 $f_0$ because each period $T_0$ induces two samples.

A normalized PD $\theta$ is evaluated with Eq. (III-4), resulting in values ranging between 0 and 1.

$$\theta^k = \frac{\Delta t^k_{V_{tri}}}{T_0} \qquad \text{(III-4)}$$

Now the similarity of the obtained PD signal with a discrete system representation is shown, the input sampled values expression has to be found to complete the model.

### III.1.2.Single TCG model

Figure III-5 shows details of the signal waveforms involved in a given TCG. $V_{triP}$ and $V_{triN}$ are the triangular signals of the Previous and Next neighboring TCGs. The values $\theta_P$ and $\theta_N$ are the related PDs. $V_{thld}$ is the local threshold voltage from Eq. (III-2) superimposed over $V_H$. The target position $\tilde{\theta}^k$ is located at the crossing of $V_{triP}$ and $V_{triN}$. The target local generated triangular signal is named $V_{trgt}$.

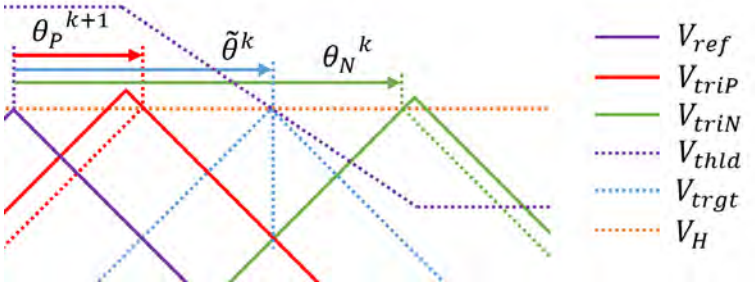



*Figure III-5 – Target position shown based on of neighbor positions.*

Figure III-5 shows that at the iteration $k$, $V_{triP}$ has already commutated, so its PD is already updated from $\theta_P{}^k$ to $\theta_P{}^{k+1}$. This is natural due to the sequential nature of the commutations, i.e. the commutations are not simultaneous. Therefore, at a given iteration $k$, the target position $\tilde{\theta}^k$ represents the average value of $\theta_P{}^{k+1}$ and $\theta_N{}^k$ values, as indicated in Eq. (III-5).

$$\tilde{\theta}^k = 0.5\left(\theta_P{}^{k+1} + \theta_N{}^k\right) + \varphi^k \tag{III-5}$$

where $\varphi^k$ represents the PD target operator result required to handle the PD discontinuity as discussed in chapter II.

The local PD $\theta^k$ is used to evaluate the local PD error $\varepsilon_\theta{}^k$, expressed in Eq. (III-6).

$$\varepsilon_\theta{}^k = \tilde{\theta}^k - \theta^k \tag{III-6}$$

Now, it must be considered the discrete transfer function $C(z)$ that establishes the relationship between the correction applied for the next iteration $\Delta\theta$ and the error $\varepsilon_\theta$. The expression of $C(z)$ can be determined analyzing the waveforms around to the commutation instant using a geometric approach as demonstrated in Annex B. The result is shown in Eq. (III-7) with its validity conditions to guarantee the geometric consistency. The corrector $C(z)$ is equivalent to a proportional gain $\alpha$ called here "convergence coefficient"

$$C(z) = \frac{\Delta\theta(z)}{\varepsilon_\theta(z)} = \alpha = \frac{4\,\beta}{1+2\,\beta}, \qquad \begin{matrix} \theta_P{}^{k+1} \le \theta^k \le \theta_N{}^k \\ \dfrac{\theta_N{}^k - \theta_P{}^{k+1}}{2} \le 0.5 \end{matrix} \tag{III-7}$$

$$-0.5 < \beta < +\infty \;\Leftrightarrow\; -\infty < \alpha < 2$$

It should be noted that this expression is valid even beyond these limits. If $-0.5 < \beta < 0$, $\alpha$ is negative, resulting in a positive feedback, so this range shall be rejected. If $\beta \to +\infty$, $\alpha$ tends to 2 and the operation is equivalent of using comparators, such as in [29].

Eq. (III-8) gives the new PD obtained $\theta^{k+1}$ reached by the local triangular signal at the iteration $k+1$. It is made up of the previous PD plus the correction applied and a disturbance

parameter $d^k$. The disturbance parameter is a consequence of the triangular waveform imperfections and will be discussed latter in III.7.

$$\theta^{k+1} = \theta^k + \Delta\theta^k + d^k \tag{III-8}$$

Figure III-6 shows a block diagram of all previously described PD operations. It reveals that the triangular carrier self-alignment system is similar to the one made up of discrete Local Controller (LC) previously presented. This model can be used for stability and convergence studies. As all PDs are measured regarding the same reference signal $V_{ref}$, the iterations of all LCs happen at the same instant ($V_{ref}$ peak/valley), simplifying the whole system modelling.

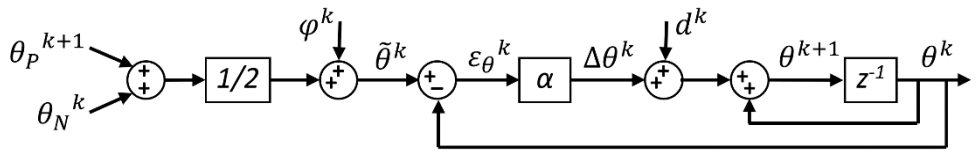



*Figure III-6 – PD local Controller block diagram.*

Eq. (III-9) gives the latest local PD obtained $\theta^{k+1}$ by successive substitutions of all previous equations (III-5) to (III-8). The next local PD $\theta^{k+1}$ depends on the next Previous neighbor PD ${\theta_P}^{k+1}$, resulting in a non-causal system.

$$\theta^{k+1} = (1-\alpha)\,\theta^k + 0.5\,\alpha\left({\theta_P}^{k+1} + {\theta_N}^k\right) + \alpha\,\varphi^k + d^k \tag{III-9}$$

To solve this problem, the modelling of the overall system is required, including the whole closed chain of communications.

### III.1.3. Overall system modelling

A system with a generic number $N$ of LCs is now considered. The LCs in circular chain are numbered from 1 to $N$ in the next direction, so the PD values are numbered from $\theta_1$ to $\theta_N$, and can be represented by a column matrix $\boldsymbol{\theta}$ (in bold in the equations). For computation purpose, the Previous PD vector $\boldsymbol{\theta}_P$ and the Next PD vector $\boldsymbol{\theta}_N$ are defined in Eq. (III-10) using the circular shift matrix $\boldsymbol{S}$ and its conjugate transposed $\boldsymbol{S}^*$, equal to its transposed $\boldsymbol{S}^T$ because $\boldsymbol{S}$ is real.

$$\boldsymbol{\theta}_P = \boldsymbol{S}\,\boldsymbol{\theta} \qquad\qquad \boldsymbol{\theta}_N = \boldsymbol{S}^*\,\boldsymbol{\theta} \tag{III-10}$$

The shift matrix $\boldsymbol{S}$ for the case with $N = 4$ is shown in Eq. (III-11).

$$\boldsymbol{S} = \begin{bmatrix} 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \tag{III-11}$$

The matrix form of Eq. (III-5), (III-6) and (III-8) are shown in Eq. (III-12), (III-13) and (III-14), respectively.

$$\widetilde{\boldsymbol{\theta}}^{k} = 0.5\left({\boldsymbol{\theta}_P}^{k+1} + {\boldsymbol{\theta}_N}^{k}\right) + \boldsymbol{\varphi}^{k} \quad \text{(III-12)}$$

$${\boldsymbol{\varepsilon}_\theta}^{k} = \widetilde{\boldsymbol{\theta}}^{k} - \boldsymbol{\theta}^{k} \quad \text{(III-13)}$$

$$\boldsymbol{\theta}^{k+1} = \boldsymbol{\theta}^{k} + \alpha\, {\boldsymbol{\varepsilon}_\theta}^{k} + \boldsymbol{d}^{k} \quad \text{(III-14)}$$

where $\boldsymbol{\varphi}^{k}$ is the target operator result vector and $\boldsymbol{d}^{k}$ is the disturbance vector.

Eq. (III-15) gives the new PD $\boldsymbol{\theta}^{k+1}$ obtained by replacing (III-10) in (III-12), then in (III-13) and then in (III-14), where $\boldsymbol{I}$ is an order *N* identity matrix.

$$\boldsymbol{\theta}^{k+1} = \boldsymbol{\theta}^{k} + \alpha\,[0.5\,(\boldsymbol{S}\,\boldsymbol{\theta}^{k+1} + \boldsymbol{S}^{*}\,\boldsymbol{\theta}^{k}) + \boldsymbol{\varphi}^{k} - \boldsymbol{\theta}^{k}] + \boldsymbol{d}^{k} \quad \text{(III-15)}$$

Figure III-7 shows the discrete time model block diagram based on Eq. (III-15). This system is linear, and the stability study can be easily performed.

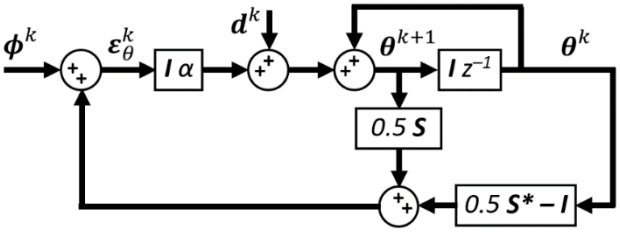



*Figure III-7 – Triangular carrier self-alignment full system block diagram.*

Eq. (III-16) is the recurrence expression of $\boldsymbol{\theta}^{k+1}$ find from Eq. (III-15) as a function of $\boldsymbol{\theta}^{k}$ and the inputs $\boldsymbol{\varphi}^{k}$ and $\boldsymbol{d}^{k}$. The system is causal and depends on the actual PD values and on the actual inputs.

$$\boldsymbol{\theta}^{k+1} = \boldsymbol{A}\,\boldsymbol{\theta}^{k} + (\boldsymbol{I} - \alpha\,0.5\,\boldsymbol{S}\,)^{-1}\,(\alpha\,\boldsymbol{\varphi}^{k} + \boldsymbol{d}^{k}) \quad \text{(III-16)}$$

where $$\boldsymbol{A} = (\boldsymbol{I} - \alpha\,0.5\,\boldsymbol{S}\,)^{-1}\,[(1-\alpha)\,\boldsymbol{I} + \alpha\,0.5\,\boldsymbol{S}^{*}]$$

The closed-loop discrete transfer function of the system is shown in Eq. (III-17) with the initial condition $\boldsymbol{\theta_0}$, where $\boldsymbol{\theta_0}$ is a column vector filled with the starting PD values and $\boldsymbol{I}$ is the identity matrix.

$$\boldsymbol{\theta}(z) = (z\boldsymbol{I} - \boldsymbol{A})^{-1}\left[z\boldsymbol{I}\,\boldsymbol{\theta_0} + (\boldsymbol{I} - \alpha\,0.5\,\boldsymbol{S}\,)^{-1}\left(\alpha\,\boldsymbol{\varphi}(z) + \boldsymbol{d}(z)\right)\right] \quad \text{(III-17)}$$

The system stability can be verified by diagonalization followed by root-analysis. The system diagonalization reveals the several decoupled dynamics, called the modal responses, which help to determine the response of the overall system to any external excitation. The whole system is stable if each of the modal dynamics are stable.

### III.1.4.Model validity domain

The model validity domain determines the operational conditions where this study results are valid, i.e. stability criterion and settling time. Two main concerns have to be discussed, the model itself and the corrector transfer function.

The local PD correction $\Delta\theta$ is not always proportionally dependent on the error $\varepsilon_\theta$. As mentioned previously, the difference of the neighbors' triangular carriers $V_{thld}$ is superimposed to the local carrier levels $V_H$ and $V_L$. Considering the neighbor signals as static, i.e. no correction applied to them, a mapping of the correction obtained as a function of all possible combinations of neighbor PDs differences named $\Delta\theta_{P,N} = \theta_N - \theta_P$, the error $\varepsilon_\theta$ and the particular case with gain $\alpha = 0.5$ is shown in Figure III-8.

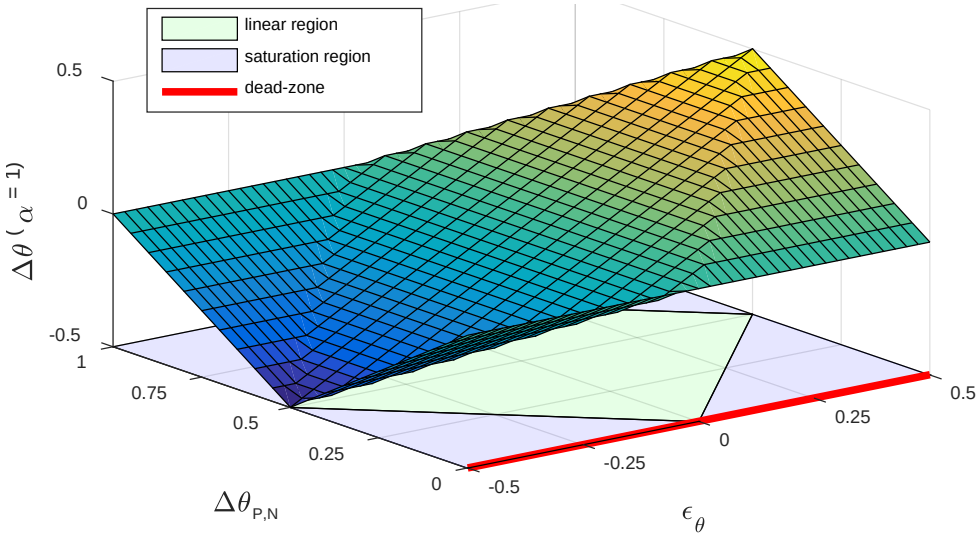



*Figure III-8 – Correction as a function of the local error $\varepsilon_\theta$ and the neighbor delays $\Delta\theta_{P,N}$ for $\alpha = 1.0$.*

Three regions can be distinguished in Figure III-8: 1) a linear region in green where the correction is proportional to the error, i.e. $\Delta\theta = \alpha\ \varepsilon_\theta$; 2) a saturation region in blue where $\Delta\theta$ is limited; 3) a dead-zone in red where the correction is null to any error value. The model is then only valid in the region 1 where the correction is proportional to the error.

As a conclusion, the corrector transfer function $C(z)$ is valid around a steady-state operation point considering limited disturbances in some particular cases, e.g. $\Delta\theta_{P,N}$ close to zero or close to 1. Modal excitations and reconfigurations involving small disturbances can be simulated with high confidence. However the results for the start-up case may be less reliable.

## III.2. **Change of basis and modal transfer functions**

The change of basis allows to decompose the original coupled system into several independent monovariable systems. It requires rewriting the system's equations in a diagonal form. As all matrices involved in this system ($\boldsymbol{I}$, $\boldsymbol{S}$ and $\boldsymbol{S}^*$) are circulanting, they are all diagonalizable with the Discrete Fourier Transform (DFT) matrix, shown in Section II.2.1. The diagonal expression of $\boldsymbol{S}$ and $\boldsymbol{S}^*$ are provided in Eq. (III-18), where $\boldsymbol{U}$ and $\boldsymbol{U}^*$ are the diagonal eigenvalue matrices of $\boldsymbol{S}$ and $\boldsymbol{S}^*$ respectively. One can note that $\boldsymbol{S}$ and $\boldsymbol{U}$ are the matrices

normally referred to as "shift and clock matrices" respectively, introduced by J. J. Sylvester in the 1880s.

$$\boldsymbol{U} = \boldsymbol{W}^{*}\boldsymbol{S}\boldsymbol{W} \qquad\qquad \boldsymbol{U}^{*} = \boldsymbol{W}^{*}\boldsymbol{S}^{*}\boldsymbol{W} \tag{III-18}$$

A change of basis expressed by the set of Eq. (III-19) is applied to the system.

$$\boldsymbol{\theta}^{*} = \boldsymbol{W}^{*}\,\boldsymbol{\theta} \qquad \boldsymbol{\phi}^{*} = \boldsymbol{W}^{*}\,\boldsymbol{\phi} \qquad \boldsymbol{\varepsilon_{\theta}}^{*} = \boldsymbol{W}^{*}\,\boldsymbol{\varepsilon_{\theta}} \qquad \boldsymbol{\theta_0}^{*} = \boldsymbol{W}^{*}\,\boldsymbol{\theta_0} \tag{III-19}$$

The system's equation, shown in Eq. (III-17), after diagonalization is made up using $\boldsymbol{W}$ and shown in Eq. (III-20).

$$\boldsymbol{\theta}^{*}(z) = \{z\boldsymbol{I} - \boldsymbol{\Lambda_A}\}^{-1}\{z\boldsymbol{\theta_0}^{*} + (\boldsymbol{I} - \alpha\ 0.5\ \boldsymbol{U}\,)^{-1}\,[\alpha\,\boldsymbol{\phi}^{*}(z) + \boldsymbol{d}^{*}(z)]\} \tag{III-20}$$

where $\boldsymbol{\Lambda_A}$ is the closed-loop diagonal eigenvalue matrix, shown in Eq. (III-21).

$$\boldsymbol{\Lambda_A} = \boldsymbol{W}^{*}\boldsymbol{A}\boldsymbol{W} = (\boldsymbol{I} - \alpha\ 0.5\ \boldsymbol{U}\,)^{-1}\,[(1-\alpha)\,\boldsymbol{I} + \alpha\ 0.5\ \boldsymbol{U}^{*}] \tag{III-21}$$

The transfer functions matrix in Eq. (III-20) is rewritten as $N$ independent transfer function on Eq. (III-22), because, assuming all inverse matrices exists, all matrices in Eq. (III-19) are diagonal. The $N$ diagonal elements $\lambda_{Aii}$ of $\boldsymbol{\Lambda_A}$ are named $\lambda_{Ai}$, for $i = 0 \ldots N-1$. The same is established for $\boldsymbol{U}$ and $\boldsymbol{U}^{*}$, where $\lambda_i$ and $\lambda_i{}^{*}$ are the diagonal values, respectively.

$$\theta^{*}{}_{i}(z) = \frac{z}{z-\lambda_{Ai}}\ \theta_0{}^{*}{}_{i} + \frac{1}{z-\lambda_{Ai}}\frac{1}{1-\alpha\ 0.5\ \lambda_i}\left[\alpha\ \varphi^{*}{}_{i}(z) + d^{*}{}_{i}(z)\right],\quad i = 0 \ldots N-1 \tag{III-22}$$

It can be noted that each closed-loop eigenvalue corresponds to a modal closed-loop pole. The Eq. (III-23) shows the analytical expression of $\lambda_{Ai}$ as a function of the gain $\alpha$ and $\lambda_i$.

$$\lambda_{Ai} = \frac{1-\alpha\ (1-0.5\ \lambda_i{}^{*})}{1-\alpha\ 0.5\ \lambda_i} \qquad i = 0 \ldots N-1 \tag{III-23}$$

The $\boldsymbol{S}$ eigenvalues are known and shown in. Eq. (III-24) for any value of $N$.

$$\lambda_i = \exp\left(j\frac{2\,\pi\,i}{N}\right) = 1\angle\frac{2\,\pi\,i}{N} \qquad i = 0 \ldots N-1 \tag{III-24}$$

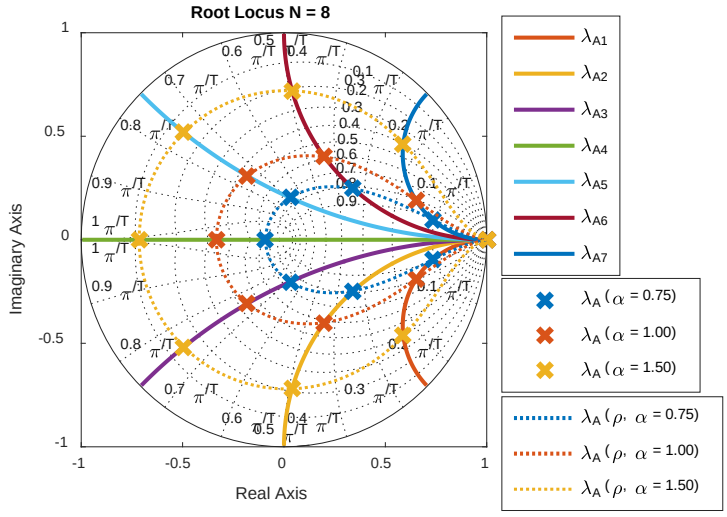
## III.3. **Stability Concern**

The corrector has only one degree of freedom, the gain $\alpha$. The common mode eigenvalue does not depends on $\alpha$ and is equals to one ($\lambda_{A0} = 1$). To guarantee stability and convergence in this discrete system, all closed-loop poles of the differential modes (i ≠ 0) have to be located inside the unit circle, i.e. their eigenvalues' absolute values must be less than 1. The stability condition with its constraints are shown in Eq. (III-25). This result is valid for any $N$ value.

$$|\lambda_{Ai}| < 1 \quad \Leftrightarrow \quad 0 < \alpha < 2 \quad \Leftrightarrow \quad 0 < \beta < +\infty, \quad i = 1 \ldots N-1 \tag{III-25}$$

The demonstration is provided in Annex C.

In order to illustrate with an example, the root locus for a system with $N = 8$ are shown in Figure III-9. All poles start at 1 when gain $\alpha$ is equal to 0 and go over the unit circle when the gain $\alpha$ is equal to 2, being equivalent to $\beta$ going to infinity.




| α | 0.75 | 1.0 |
|---|---|---|
| $\lambda_{A1}$ | 0.74 ∠ -7.4° | 0.68 ∠ -16° |
| $\lambda_{A2}$ | 0.42 ∠ -36° | 0.45 ∠ -63° |
| $\lambda_{A3}$ | 0.21 ∠ -81° | 0.36 ∠ -120° |
| $\lambda_{A4}$ | 0.09 ∠ -180° | 0.33 ∠ -180° |
| $\lambda_{A5}$ | 0.21 ∠ 81° | 0.36 ∠ 120° |
| $\lambda_{A6}$ | 0.42 ∠ 36° | 0.45 ∠ 63° |
| $\lambda_{A7}$ | 0.74 ∠ 7.4° | 0.68 ∠ 16° |

*Figure III-9 – Root locus for $N = 8$ with pole-zero mapping for tree particular cases: $\alpha = 0.75$, $\alpha = 1.0$ and $\alpha = 1.5$.*

Based on the z-domain model, this plot confirms that a limited positive gain $\beta$ leads to a stable system. If comparators are used ($\beta \to +\infty$), all differential modes are in stability limit (all poles placed on the unitary circle) and oscillates.

In Chapter II, the open-loop modal transfer functions have real eigenvalues that appeared as gain factors, so only one root locus exists and all pole-zero are located there, independently of the $N$ value. However, in the present case, such simplicity cannot be observed. The closed-loop eigenvalues can be expressed as a function of the matrix $\boldsymbol{S}$ eigenvalues. The matrix $\boldsymbol{S}$ eigenvalues are complex, their absolute values are all equal to 1, but their arguments are different, such as $\lambda_i = 1\angle\rho$, where $\rho$ depends on $N$ and $i$. Figure III-9 shows dotted lines as a function of the eigenvalue angle $\rho$, ranging between 0 and 2π, for several given α values. The lines $\lambda_A(\rho, \alpha)$ are independent of $i$, showing the locations where the eigenvalues will land for any $N$ values. The non-plotted line $\lambda_A(\rho, \alpha = 2.0)$ is coincident with the unit circle, as shown in Eq. (III-26).

$$\lambda_{Ai}|\alpha = 2 = \lambda_i{}^* \;\Rightarrow\; |\lambda_{Ai}|_{|\alpha = 2} = |\lambda_i{}^*| = |\lambda_i| = 1, \quad i = 0 \ldots N-1 \qquad \text{(III-26)}$$

It should be noted that the poles' placement presents a symmetry with respect to the real axis. The symmetric poles correspond to the double modes, where $w_{N-i} = w_i{}^*$ and $\lambda_{A(N-i)} = \lambda_{Ai}{}^*$. To avoid showing redundant information, the modal index $m = 0 \ldots M-1$ can be used, where $M$ is defined as in the previous study.

### III.3.1. Settling time and voltage gain design

The settling time depends on the triangular signal frequency $f_0$ and on the number of iterations required to reject a disturbance. The value of the triangular signal frequency is imposed by the application.

The number of iterations for convergence can be computed, for example, by the number $k$ of iterations necessary to reduce the absolute value of each differential mode natural (homogeneous) response ${\theta^*}_{mh}$ to less than 5% of its initial value ${{\theta_0}^*}_m$. The modal natural (homogeneous) response ${\theta^*}_{mh}$ shown in Eq. (III-27) can be found by applying the inverse Z-transform to the first term of Eq. (III-22), where $m$ is the mode number and $h$ is the homogeneous marker.

$$ {\theta^*}_{mh}(k) = {\lambda_{\mathrm{Am}}}^{\mathrm{k}} {{\theta_0}^*}_m = |\lambda_{\mathrm{Am}}|^{\mathrm{k}} \left(1\angle\varphi_{\lambda_{\mathrm{Am}}}\right)^{\mathrm{k}} {{\theta_0}^*}_m, \quad \begin{cases} \mathrm{k} \geq 0 \\ \lambda_{\mathrm{Am}} = |\lambda_{\mathrm{Am}}|\angle\varphi_{\lambda_{\mathrm{Am}}} \\ m = 1 \ldots M-1 \end{cases} \qquad \text{(III-27)} $$

Eq. (24) shows the general formula for the number of iterations derived from Eq. (III-28).

$$ k_{5\%\_\mathrm{m}} = \frac{log(0.05)}{log(|\lambda_{\mathrm{Am}}|)}, \qquad m = 1 \ldots M-1 \qquad \text{(III-28)} $$

Table III-1 shows the number of iterations required for convergence for the several differential modes in the case $N = 8$. Note that no mode converges when $\alpha = 2$.

*Table III-1 – Number of iterations for 5% convergence criterion ($N = 8$, $M = 5$, 4 differential modes, 4 eigenvalues).*

| | md1: $k_{5\%\_1}$ | md2: $k_{5\%\_2}$ | md3: $k_{5\%\_3}$ | md4: $k_{5\%\_4}$ |
|---|---|---|---|---|
| $\alpha = 2$ | $+\infty$ | $+\infty$ | $+\infty$ | $+\infty$ |
| $\alpha = 1.5$ | 10 | 9.2 | 8.9 | 8.9 |
| $\alpha = 1$ | 7.7 | 3.7 | 2.9 | 2.7 |
| $\alpha = 0.75$ | 10 | 3.5 | 1.9 | 1.2 |

Table III-1 shows explicitly the number of iterations required for each differential mode with a given α parameter. Observing the different configurations, it is not easy to guess which would be the optimal one. All differential mode eigenvalue absolute values, and consequently the response time, have to be reduced to speed-up the global response on any type of disturbance. As these values depend on α, a criterion has to be established to find a trade-off. Supposing all modes have the same importance, the criterion to choose the optimal configuration can be the quadratic sum. The quadratic sum can be applied on the eigenvalues or on the number of iterations $k_{5\%}$ of each differential mode. Only the differential modal values ($m = 1 \ldots M-1$)

are considered in order not to overweight the double modes. These two approach results are shown in the plot of Figure III-10 for $N = 8$.

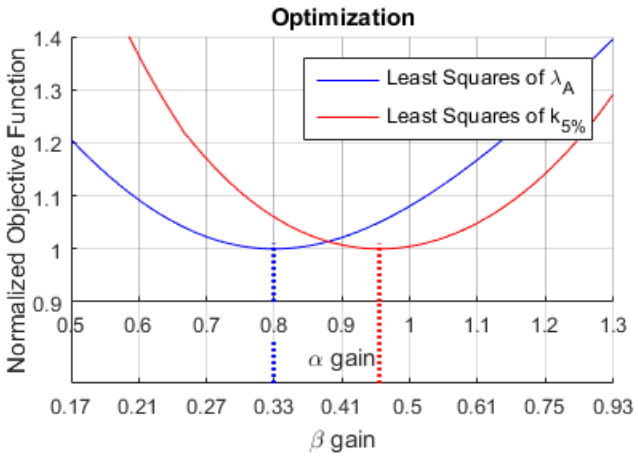



*Figure III-10 – Optimized Convergence Coefficient α. Minimising criterion: least squares of $\lambda_{Am}$ and least squares of $k_{5\%\_m}$.*

The minimum value using the eigenvalue least squares criterion is found with $\alpha$ = 0.8, while the minimum value using the $k_{5\%}$ least squares criterion is found with $\alpha$ = 0.95. The least squares of $k_{5\%}$ criterion is preferable because the response is more uniform due to the smaller response time dispersion. As a conclusion, for $N = 8$, the optimal voltage gain $\beta$ would be in the range 0.4 and 0.5.

Considering the first model with only the local loop, the case $\alpha = 1$ ($\beta = 0.5$) corresponds to the one shoot response, and is similar to the digital system described previously. However, the overall digital implementation is not stable in this condition, while the Triangular Carrier Self-Alignment seems to be stable, according to the proposed model.

### III.3.2.Eigenvalues and stability vs. number of active LCs

This system has the intrinsic ability to reconfigure, so the eigenvalues have to be computed for several number of active LCs required in the application. The root locus analysis for the cases of $N = 4 \ldots 9$ are shown in Figure III-11 with the gain $\alpha$ ranging from 0 to 2.

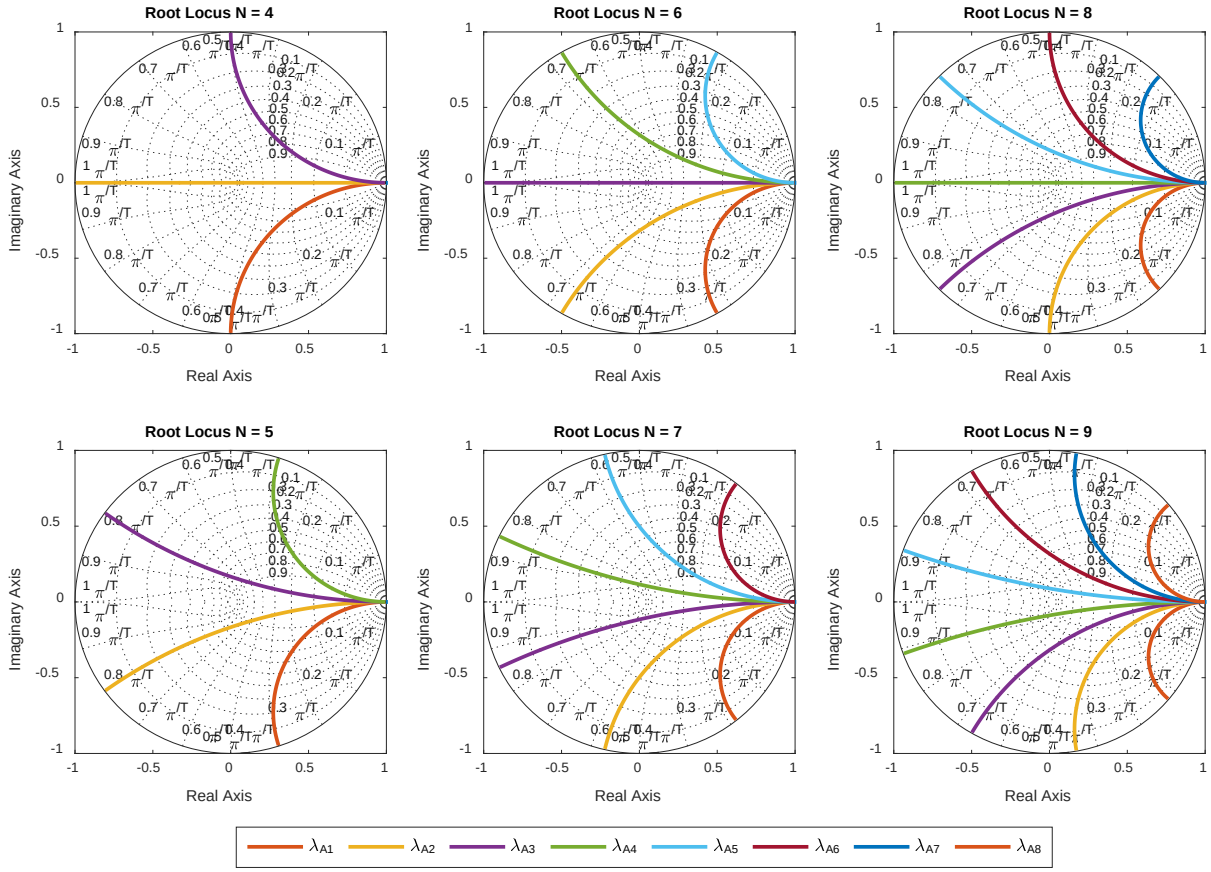



*Figure III-11 – Root locus for $N = 4 \ldots 9$ with $\alpha$ ranging from 0 to 2.*

All $\lambda_{A0}$ related to the common mode are constant, equal to 1 and not shown. All differential modes are controllable because their eigenvalues depend on the parameter $\alpha$. All differential modes are double and have a pole symmetrical to the imaginary axis (its conjugate), except when $N$ is even, where the mode $N/2$ is a single mode.

A reconfiguration event is the modification during operation of the number $N$ of active LCs. Non-active LCs are bypassed, i.e. the chain of communication remains closed, and become invisible to active LCs. As seen before, all eigenvalues depend on a single convergence factor $\alpha$, and a trade-off has to be made. On the other hand, when a reconfiguration is made, $\alpha$ remains the same, but the eigenvalues change.

The 5% response convergence speed should also be optimal when $N$ varies. However the number of active modules is unknown and all local controllers have to be equal by definition. To simplify the design, the same $\alpha$ is used in all cases and the relative response degradation is verified. A parametric plot of the least squares of $k_{5\%}$ as a function of the convergence coefficient $\alpha$ and the value of $N$ is shown in Figure III-12.

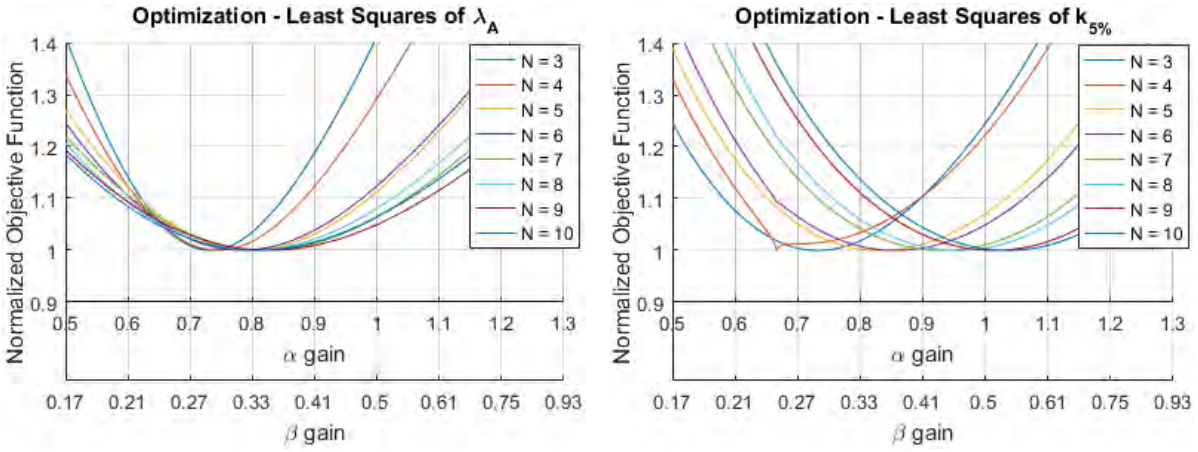



*Figure III-12 – Optimized Convergence Coefficient α using least squares of $\lambda_A$ and $k_{5\%}$ criterion. Sensibility to N.*

The curves show the minimum for $\alpha$ is in general between 0.7 and 0.9, and it goes up with $N$. The least squares of $k_{5\%}$ give a best time response trade-off. The optimum is much more dependent on $N$ than in the previous case, being between 0.65 and 1.05 in the range of $N$ shown. The simulations presented here after are made using $N = 8 \pm 1$, so $\alpha$ is chosen around the optimized value to $N = 8$ using the least squares of $\lambda_A$ and the least squares of $k_{5\%}$, being 0.8 and 1.0, respectivelly.

In this approach, the corrector is of type proportional represented by the Convergence Coefficient $\alpha$. So, other than the transient response, $\alpha$ impacts the static gain and consequently the steady-state error. It would be natural to choose a higher $\alpha$ value to further reduction of the steady-state error. The disturbance impact in the steady-state error will be discussed in III.7.

## III.4. **Diagonal response**

The dynamic behavior of the overall system has been simulated and the settling time compared with the one predicted. A space state system based model is defined and simulated using MathWorks MATLAB®. In the simulations performed hereafter, the system starts in its expected equilibrium state with all the carriers well interleaved. Each mode is excited individually one after the other, from the common mode (mode 0) to the last one (mode 4) using the system eigenvectors (lines of the DFT matrix) as components of the disturbance signal $\boldsymbol{d}$.

Figure III-13 shows the simulation results of a system with eight LCs ($N = 8$) and $\alpha$ equal to either 0.8 or 1. Each simulation result is composed of the modal disturbance applied $\boldsymbol{d}^* = |\boldsymbol{W}^{-1}\boldsymbol{d}|$, the PD $\boldsymbol{\theta}$ waveforms, and the local error $\boldsymbol{\varepsilon_\theta}$ modal decomposition $|\boldsymbol{\varepsilon_\theta}^*|$ to observe the total mode disturbance. For simulation purposes, the target operator introduced in the digital case is required. Eq. (14) is taken to find the $\boldsymbol{\varphi}$ required considering $\boldsymbol{d} = \boldsymbol{0}$ and

$\boldsymbol{\theta}^{k+1} = \boldsymbol{\theta}^{k}$, where $\boldsymbol{\theta}^{k}$ is the expected PD in a well interleaved system. It results in the same values for $\boldsymbol{\varphi}$ found in the digital case shown in Eq. (II-40).

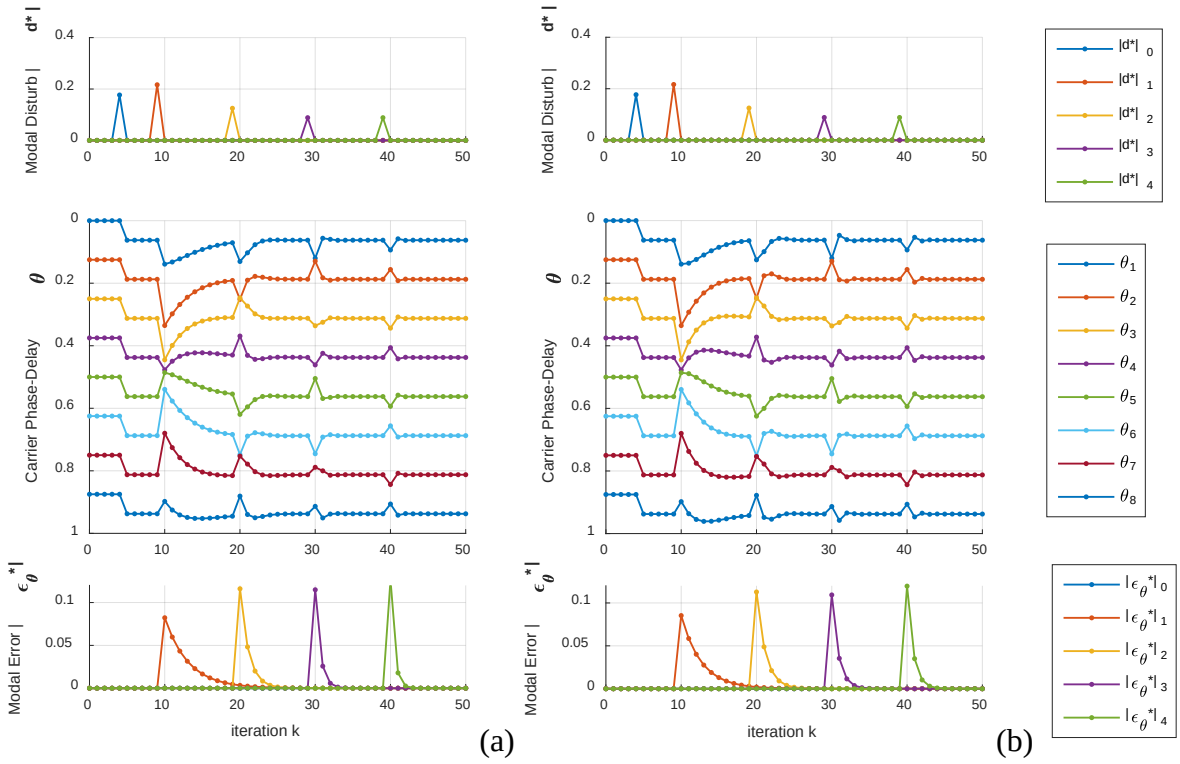



*Figure III-13 – Dynamic modal response (N = 8) a) α = 0.8; b) α = 1.0.*

The deviations that appear have the eigenvectors' shape (similar to sine wave) and cycle number shown in Figure II-5. The PD values behave as expected. It is possible to distinctly observe the modal excitations being applied successively. All modes are correctly damped and the convergence speed confirm the figures shown in Table III-1.

A singularity should be noted on $\boldsymbol{\theta}$ waveforms. The $\boldsymbol{\theta}$ waveforms do not have the same shape as the components of $|\boldsymbol{\varepsilon}_{\boldsymbol{\theta}}{}^{*}|$. When the mode 1 is disturbed on Figure III-13 (a), the $\theta_1$ response has almost a straight line shape. It is due to the inverse Z-transform of the single complex pole. The single complex pole response $\lambda_{\mathrm{Am}}{}^{\mathrm{k}}$ changes the amplitude and phase, i.e. rotates the modal component, as seen in the modal response shown in Eq. (III-27). When complex conjugated poles are found, only the amplitude changes because the complex parts compensate each other.

## III.5. **Reconfiguration simulations**

As soon as a TCG state changes (activated/deactivated), the active TCGs evolve their triangular signal PDs to reach a new steady-state arrangement where all the carriers are correctly interleaved again. The model is used in reconfiguration simulations and its responses are analyzed hereafter, first with the removal case, then the insertion case.

The simulations show the differential modes are excited at the beginning and the responses have the same dynamics revealed previously on Table III-1.

### III.5.1.TCG removal

The simulation of a reconfiguration proposed here illustrates the cases of a TCG removal (one TCG is bypassed). The removal is the simplest reconfiguration case because the system is already interleaved and there is no initial value to care about.

Figure III-14 (a) shows a simulation starting with nine well-interleaved TCGs. The local controller TCG3 is disabled and bypassed at the first iteration, then the eight active TCGs reconfigure and reach another interleaving state with $\alpha$ = 1.0.

### III.5.2.TCG insertion

The insertion reconfiguration is optimal when the reactivated TCGs are pre-positioned in between its neighbors, not necessarily in the middle. As a result, the errors are small, corrector non-linear behavior is avoided and settling time is known.

Figure III-14 (b) shows a reconfiguration simulation starting with seven well-interleaved TCGs. The local controller TCG5 is disabled and positioned in between its neighbors. TCG5 becomes visible at the first iteration, then the eight active TCGs reconfigure and reach another interleaving state.

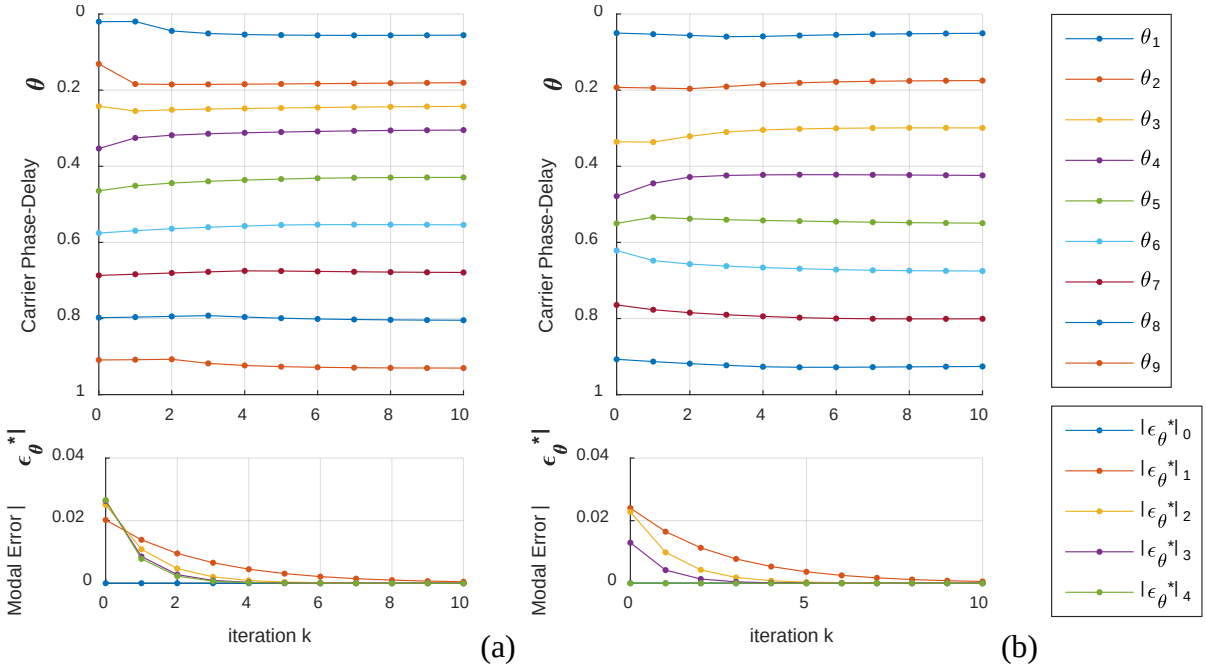



*Figure III-14 – Reconfiguration response, α = 1.0: a) N from 9 to 8, TCG3 is bypassed, b) N from 7 to 8, TCG5 is introduced.*

All components of $|\boldsymbol{\varepsilon_\theta}^*|$ are mitigated very quickly in both cases and the new correct interleaved state is reached.

The model proposed in this work is not able to reveal what happens when the system is outside the linear zone. However, it can be thought that if the reactivated TCGs is not too far from the linear zone, i.e. close enough to the area bounded by the neighbors, its neighbors are likely to be in the same condition, so the system shall converge to the correct interleaved state. For large differences, no conclusion can be stated due to the system nature. There is a risk of convergence to an incorrect or a non-usual interleaved arrangement. It can only be verified through simulation and practical implementation. For that reason, in any cases, a disabled TCG will always be pre-positioned in between its two neighbors.

## III.6. **Convergence and steady-state value**

The discrete time transfer function can be used to reveal the PDs' steady-state arrangement to a given start condition if the system's start condition (all PD errors) is in a linear region. To do so, a valid target vector $\boldsymbol{\varphi}$ required by the model has to be computed from the PD initial values $\boldsymbol{\theta_0}$ at start-up. Then, the PDs' steady-state values $\boldsymbol{\theta_{ss}}$ can be calculated using the Final Value Theorem (FVT) if all differential modes are damped. The result in Eq. (III-29) is found by inserting Eq. (III-17) into Eq. (II-47) and solving. The steady-state depends on the start-up configuration $\boldsymbol{\theta_0}$ that provides $\boldsymbol{\varphi}$, and, more importantly, on $\boldsymbol{L}^+$, related to the circular communication chain configuration. As a result, the gain $\alpha$ and the delay on $\boldsymbol{\theta_P}$ connection do not affect $\boldsymbol{\theta}$ final values.

$$\boldsymbol{\theta_{ss}} = \overline{\boldsymbol{\theta_0}} - \boldsymbol{L}^+ \left( \boldsymbol{\varphi} + \frac{1}{\alpha}\, \boldsymbol{d} \right) \tag{III-29}$$

Again, a term related to the disturbance input $\boldsymbol{d}$ appears in the expression. This expression is valid if $\boldsymbol{d}(z)$ is constant, i.e. $\boldsymbol{d}(z) = \boldsymbol{d}\, u(z)$, where $u(z)$ is the step function, and the common mode of $\boldsymbol{d}$ is null, i.e. the sum of all elements of $\boldsymbol{d}$ is null ($\boldsymbol{d}^*{}_0 = 0$), what prevents $\boldsymbol{\theta}$ from sliding permanently.

It can be highlighted, like in any control system using proportional gain, the interest of increasing the corrector gain to reduce the disturbance impact in the steady-state values. The relationship between the disturbance $\boldsymbol{d}$ and the steady-state local error $\boldsymbol{\varepsilon_{\theta_{ss}}}$ is revealed in the same way in Eq. (III-30).

$$\boldsymbol{\varepsilon_{\theta_{ss}}} = -\frac{1}{\alpha}\, \boldsymbol{d} \tag{III-30}$$

To choose the minimum gain $\alpha$, the expression of $\boldsymbol{d}$ has to be analyzed. The term $\boldsymbol{d}$ is related to all existing disturbances in the system, such as frequency mismatch, triangular wave mismatch, and electronic circuit mismatch.

## III.7. Disturbance estimation and error sensibility

Willing to limit the closed-loop steady-state error $\boldsymbol{\varepsilon_{\theta_{ss}}}$, the relation between the circuit parameters and the disturbance $\boldsymbol{d}$ has to be revealed. This allows the system definer to specify the system building blocks tolerances to reach the expected performance, in this case $\boldsymbol{\varepsilon_{\theta_{ss}}}$.

Numerous parameters can cause disturbances in the PDs, but just some of them are discussed here. It is assumed each TCG is impacted by a disturbance $d_i$ , $i = 0 \ldots N-1$, independent of the others TCGs that compose the disturbance vector $\boldsymbol{d}$. In an arbitrary TCG, the disturbance $d$ is related to $V_H$ and $V_L$ values. All the others parameters, such as slew rates and gains, are considered equal in all TCGs on purpose of this this study.

To find the expression of the equivalent disturbance $d$, the voltages $V_H$ and $V_L$ are rewritten in two components, the differential mode $\Delta V_0$ ($\Delta V_0 = V_\mathrm{H} - V_\mathrm{L}$) and the common mode $V_{\mathrm{DC0}}$ ($V_{\mathrm{DC0}} = (V_\mathrm{H} + V_\mathrm{L})/2$). For modelling purpose, $\delta v_{\mathrm{dm}}$ is the local voltage deviation to the average differential mode $\Delta V_0$ and $\delta v_{\mathrm{cm}}$ is the local voltage deviation to the average common mode $V_{\mathrm{DC0}}$.

The PD expression can be evaluated using Eq. (III-8) ($\Delta\theta^k = 0$). Then $d^k$ expression of the disturbed triangular wave can be generically written as shown in Eq. (III-31). It can be noted $d^k$ is composed of a common mode $\bar{d}$ (cumulative) and an oscillating mode $\tilde{d}$ (non-cumulative).

$$d^k = \bar{d} + (-1)^k \tilde{d} \tag{III-31}$$

Figure III-15 and its impact on the PD.

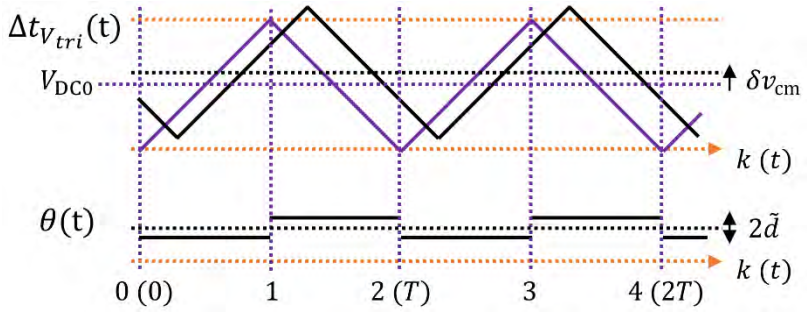



*Figure III-15 – Reference and disturbed triangular waves.*

It should be noted the triangular wave common mode does not modify the period, but it disturbs the PD measurement, i.e. there is no cumulative effect ($\bar{d} = 0$). In the other hand, the triangular wave differential mode modifies systematically the period, but does not cause oscillation ($\tilde{d} = 0$).

To obtain $\bar{d}$ from $\Delta V_0$ and $\delta v_{\mathrm{dm}}$, the term $\tilde{d}$ has to be supressed. It can be done by computing the PD difference between two non-consecutive iterations $\delta\theta$, as shown in Eq. (III-32).

$$\delta\theta = \theta^{k+2} - \theta^{k} = d^{k+1} + d^{k} = 2\,\bar{d} \qquad \therefore \bar{d} = ½\,\delta\theta = \delta T/T_0 = \frac{\delta v_{\mathrm{dm}}}{\Delta V_0} \tag{III-32}$$

Similarly, to obtain $\tilde{d}$ from $\Delta V_0$ and $\delta v_{\mathrm{dm}}$, the term $\bar{d}$ has to be suppressed. It can be done by computing the difference between two consecutive iteration PD differences $\delta\theta$, as shown in Eq. (III-33).

$$\delta\theta = (\theta^{k+2} - \theta^{k+1}) - (\theta^{k+1} - \theta^{k}) = d^{k+1} - d^{k} = 2\,\tilde{d} \quad \therefore \tilde{d} = ½\,\delta\theta = 2\frac{\delta v_{\mathrm{cm}}}{V_{\mathrm{DC0}}} \tag{III-33}$$

As a general rule, all mismatches impacting the frequency (e.g. average slew rate) can be generalized on the $\bar{d}$ value, while the mismatches impacting the symmetry (e.g. positive/negative slew rate) will impact the components $\tilde{d}_{\mathrm{i}}$.

The expressions in Eq. (III-34) shows the relations between the disturbance $\bar{d}$ to a frequency deviation $\delta f$ through a small signal approximation, where $T$ and $T_0$ are the local and reference carrier periods, respectively, and $f$ and $f_0$ their frequencies, respectively. The average local error $\overline{\varepsilon_\theta}$ is also shown in Eq. (III-34).

$$\begin{gathered} 1 + \delta\theta = 1 + 2\,\bar{d} = \frac{T}{T_0} = \frac{f_0}{f_0 + \delta f} \cong 1 - \frac{\delta f}{f_0} \\ \begin{array}{cc} T = 1/f & \therefore \bar{d} \cong -\dfrac{1}{2}\,\dfrac{\delta f}{f_0} \\ T_0 = 1/f_0 & \\ f = f_0 + \delta f & \therefore \overline{\varepsilon_\theta} \cong \dfrac{1}{2\alpha}\,\dfrac{\delta f}{f_0} \end{array} \end{gathered} \tag{III-34}$$

To guarantee the validity of the model, the disturbance common mode $\boldsymbol{d}^*_0$ has to be null, even if the local components $\bar{d}_{\mathrm{i}}$ are not null. It is achieved when the reference triangular signal frequency $f_0$ is the average frequency of all active modules. As a consequence, the steady-state frequency is the average of all active TWGs' frequencies and the interleaving error is only due to their frequency mismatches.

Even if the average value of the oscillating component $\tilde{d}$ is null, it also affects the PWM signals PD generated from the triangular carrier. It is because the PWM signal is referenced only to one commutation (valley or peak), resulting in a systematic shift. This is a weakness of this approach, as the PD error is dependent not only on the frequency but also on the signal symmetry, so frequency trimming is not effective to reduce interleaving error.

To conclude, mathematical expressions can be derived and used to provide design recommendations such as local controller gain and frequency accuracy requirements to achieve the local error accuracy target. For instance, with a required local error accuracy $\overline{\varepsilon_\theta} = \pm 1\%$, the frequency accuracy has to be better than $\pm 2\%$ if the local controller gain $\alpha = 1$. The complete expression of the final error regarding all parameters is not developed in this document.

## III.8. Particular case using comparators ($\alpha = 2$)

The approach presented by XIAO in [29] uses comparators to change the slope direction of the triangular signals, similar to applying an infinite voltage gain ($\alpha = 2$). Considering the model still valid in this case, all poles are on the unit circle and all differential modes oscillate, and theoretically, there is no convergence.

However, even if there is no convergence when the gain $\alpha = 2$, all triangular carriers change the sign of their slope at the neighbors' crossing instant, such as in a correctly interleaved system with no mismatches. As these are contradictory situations, the system cannot be correctly interleaved.

As shown previously, a DC level mismatch causes an oscillating disturbance. To solve the convergence issue, XIAO added in his approach a saturation in the triangular signals to keep them between $V_L$ and $V_H$, avoiding DC level mismatch and force convergence.

## III.9. Circuit based simulations

Circuit based simulations are realized to validate the model proposed.

Figure III-16, Figure III-17 and Figure III-18 show two simulations each with 8 active TCGs to reveal the behavior of a system in (a) with limited positive gain $\beta$ $(\alpha = 1, \beta = 0.5)$ and in (b) a system with comparators $(\alpha = 2, \beta \to +\infty)$. The clock and triangular signals are shown on the top and bottom, respectively, with the following color code:

FC1.clk FC2.clk FC3.clk FC4.clk FC5.clk FC6.clk FC7.clk FC8.clk
FC1.Vtri FC2.Vtri FC3.Vtri FC4.Vtri FC5.Vtri FC6.Vtri FC7.Vtri FC8.Vtri

where FCx stands for $x^{th}$ LC, also named LCx.

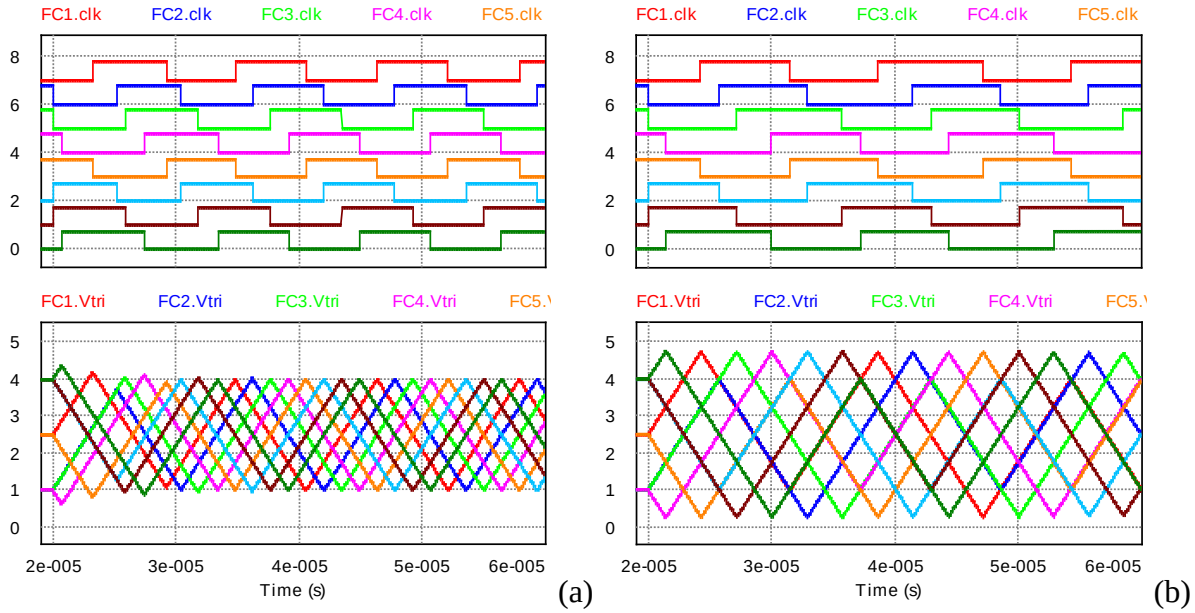



*Figure III-16 – Simulation Mode 2: a)* $\alpha = 1, \beta = 0.5$*; b)* $\alpha = 2, \beta \to +\infty$.

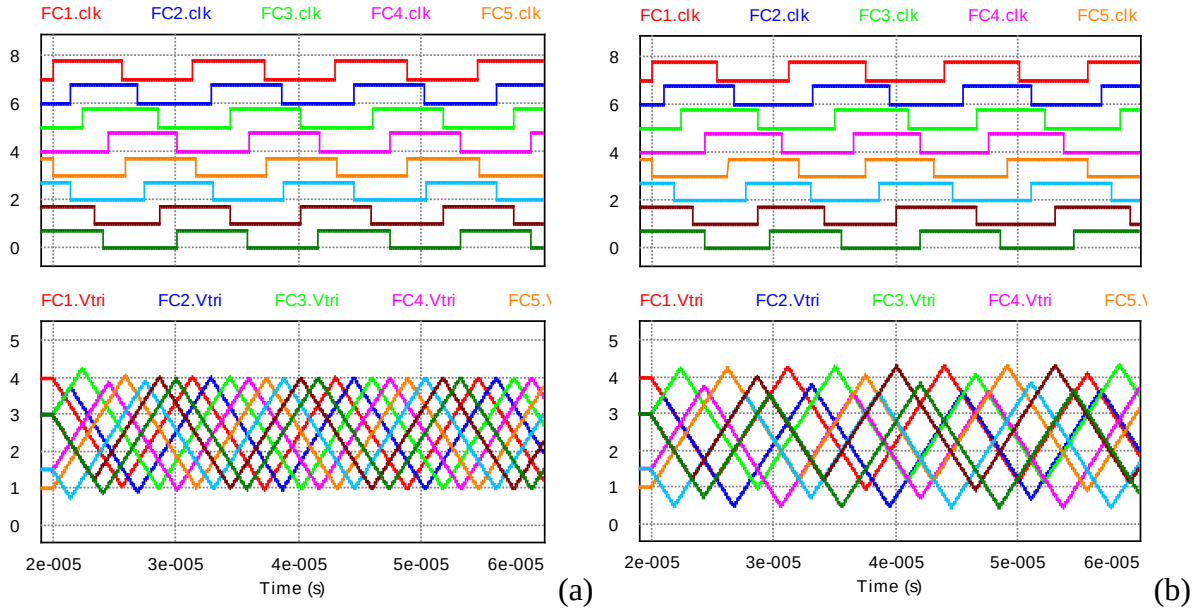



*Figure III-17 – Simulation Mode 3: a)* $\alpha = 1, \beta = 0.5$*; b)* $\alpha = 2, \beta \to +\infty$.

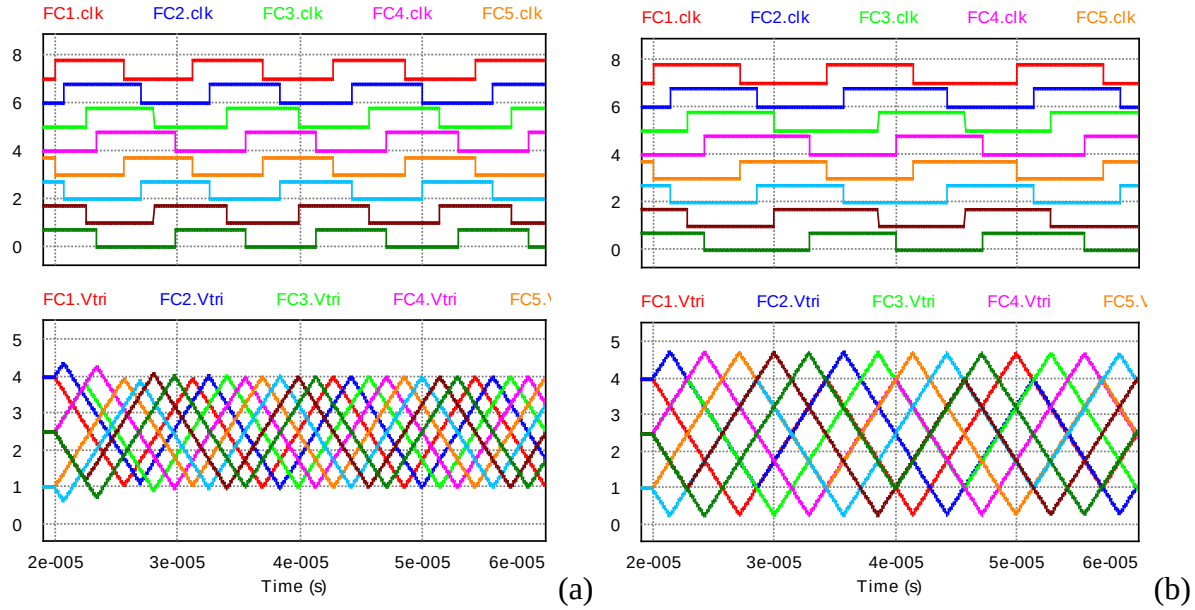



*Figure III-18 – Simulation Mode 4: a)* $\alpha = 1, \beta = 0.5$*; b)* $\alpha = 2, \beta \to +\infty$.

As expected, based on the z-domain model, all modes are damped when $\beta$ is a limited positive gain $(\alpha = 1, \beta = 0.5)$. According with the proposed model, the ideal system with comparators $(\alpha = 2, \beta \to +\infty)$ and without delays results in non-damped oscillations. The model satisfactorily represents the transient performance, showing the stability limit when $\beta \to +\infty$, resulting in all poles close to the unitary circle.

Figure III-19 shows two simulations to reveal the start-up response of a system with $\alpha = 1$. In (a) start-up by groups (4+4) and (b) start-up in phase opposition(1+7).

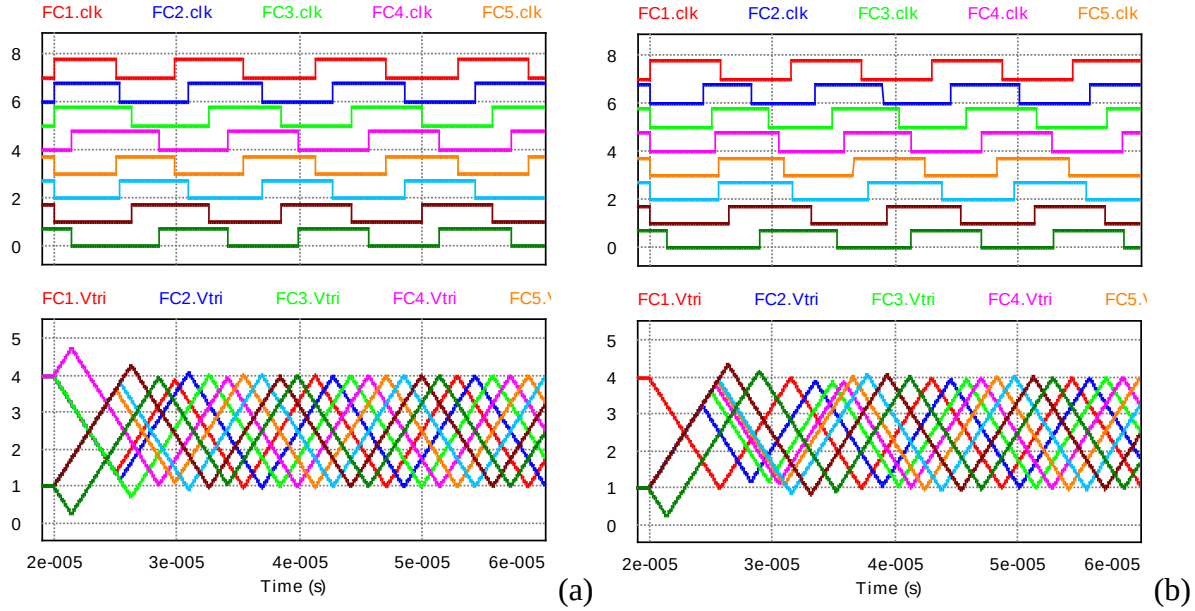



*Figure III-19 – Start-up response,* $\alpha = 1, N = 8$*: a) start-up by groups (4+4), b) start-up in phase opposition(1+7).*

It can be noted that the start-up by groups converges faster (Mode 1 is not disturbed) than the start-up with one LC in phase opposition as revealed by the model.

Considering the first model with only the local loop, the case $\alpha = 1$ ($\beta = 0.5$) corresponds to the one shoot response, and is similar to the digital system described previously. However, the overall digital implementation is not stable in this condition, while the Triangular Carrier Self-Alignment is shown with these simulations.

Figure III-20 show a simulation of the particular case using comparators ($\alpha = 2, \beta \to +\infty$) introduced by XIAO. In the simulation, only Mode 4 is disturbed at the beginning and triangular signals kept between $V_L$ and $V_H$.

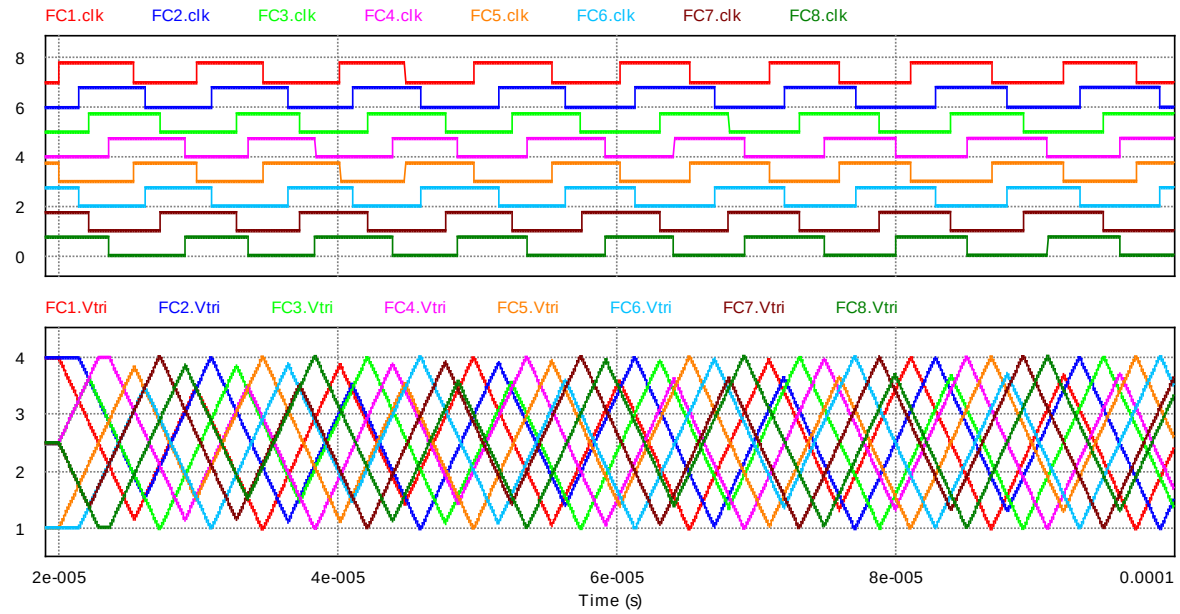



*Figure III-20 – Simulation Mode 4 using comparators ($\alpha = 2, \beta \to +\infty$) with triangular signals kept between $V_L$ and $V_H$.*

It can be noted in Figure III-20 that the system converges slowly to the expected steady-state interleaving, even if $\alpha = 2, \beta \to +\infty$.

## III.10. **Conclusion**

This chapter has presented a complete model of the triangular carrier self-alignment approach and analyzed its stability criterion.

The proposed model shows the system is robust and can work properly in a wide range of gain and large number of LCs. However, the proportional controller (one freedom degree) limits the system performance because it links directly the transient response with the static error, requiring a trade-off.

The interleaving method using analog signals at the communication links between devices complicate bypass circuits (analog switches and buffers are needed). Moreover, intrinsic mismatch between triangular signal generators (analog signals) cause phase-delay (interleaving) errors that cannot be avoided by frequency adjustment (trimming).

The ability to compute a proper correction even when the local phase-delay not in between the neighbors is an additional strength. Nevertheless, its inability to interleave between coincident neighbors makes start-up with numerous coincident carriers risky. Moreover, the mismatch impact in this condition (at start-up with very close neighbors) is still unknown.

Reconfiguration disturbs the PWM signals when the triangular signal play the role of carrier. Using the control signal superimposed on only one threshold would improve this point, e.g. making correction on triangle peak threshold if duty cycle is low. However the triangle peaks would be well interleaved while the triangle valleys would be subject to the mismatch, resulting in an increase on interleaving error.

The following 4 points summarize the triangular carrier self-alignment approach main weaknesses to be addressed in order to improve the system:

- Non-flexible controller;
- Uses analog signal;
- Unable to interleave between coincident neighbors;
- PWM disturbance during reconfiguration.

# IV. New approach: digital signal self-interleaving system

This chapter introduces a new modular distributed self-interleaving approach based on elements exchanging only digital signals, such as clock signals. This chapter includes the design process required to obtain the system parameter values leading to high availability with good transient and static performances. A model and the study of its dynamic behavior are provided. Additionally, fault events in the communication lines are considered, described and simulated. The methods to detect and overcome this fault events are also described.

## IV.1. Self-interleaving features

The circular-chain numeric interleaving and the triangular carrier self-interleaving methods have been deeply studied in chapter II and III respectively, where models have been proposed, their stability criterion stablished and their performance limits demonstrated.

The interleaving system features can be classified in three main categories: topology, availability and performance. The feature categories and their goals for this interleaving system are listed on Table IV-1.

*Table IV-1 –New interleaving system features/goals.*

| Feature category | Goal |
|---|---|
| Topology | Modularity, scalability, unrestricted carrier type |
| Availability | Fail-operational, no Single Point Of Failure (SPOF) |
| Performance | Communication noise immunity, mismatch sensitivity, settle time, static error, smooth transient (no duty-cycle discontinuity) |

From now, the previous systems' accomplished goals will be summarized. Then, their limitations will be highlighted. A new auto-interleaving method will be proposed, providing appropriate improvements, followed by its detailed theoretical study and its implementation. Finally, experimental results will be provided to demonstrate the validity of the proposed method.

### IV.1.1. Advantages, features to keep

The advantages and features of the two interleaving techniques of chapter II and III to keep in the new approach are listed below.

Advantages shared by both implementations:

a. Modularity: all modules are equal, i.e. no master required;
b. Fail-operational when a communication line fails (note a fault detection is however required).

Advantages of the circular-chain numeric interleaving due to its digital implementation:

c. Digital communications, i.e. high noise immunity;
d. Flexible local controller corrector (not only proportional), i.e. better closed-loop performance;
e. Several possible carrier waveform choices and modulation techniques, i.e. carrier generator dissociated from the local controller;
f. No mismatch issue.

Advantages of the triangular carrier self-interleaving mainly due to its analog implementation:

g. No shared wire, i.e. no wire connecting all elements (a global clock signal for instance);
h. Theoretical unlimited scalability and with perfect interleaving: Continuous phase-delay values (not pre-defined/discrete).

It should be noted the circular-chain numeric interleaving has a major drawback due to the required global clock share-wire. This common wire is a SPOF. So a system architecture such as the triangular carrier self-interleaving should be considered. However, its limitations and weaknesses, mismatches and noise dependences for instance, have to be improved. This will be discussed thereafter.

### IV.1.2. Limitations, features to improve

To develop a robust circular chain interleaving system, the triangular carrier self-interleaving weaknesses have to be listed and discussed. The main issues are:

a. Matching issues: the control is based on arithmetical operations over analog signals;

Each local controller and carrier generator has its own local references (voltages, currents). They can be slightly different from one to the other. On one hand, comparing two mismatched signals leads to make inevitable mistakes. On the other hand, comparing the time delay between two digital signals based on their rising and falling edges avoid all mismatch issues.

b. Low noise immunity: the external analog signals are used to generate the local phase correction.

The self-alignment principle is based on modifying the local Schmitt trigger thresholds using the difference of the neighbors' triangular carrier analog signals. In that case, any external electrical noise injection can alter the Schmitt trigger commutation instant and therefore the

phase position accuracy. Filtering the control signal is not recommended because it would add an additional phase-delay on the commutation and generate a systematic error.

c. Disturbance issues: PWM disturbance during reconfiguration due to transient on carrier amplitudes;

The Schmitt trigger thresholds are strongly affected during the transient/reconfiguration event, leading to affect the several carrier amplitudes. Therefore, the duty-cycles of the PWM signals are also affected, resulting in transient on both output voltage regulation and leg current balance. To avoid this issues, the carrier amplitudes have to remain constant. Note that, to implement the self-interleaving function, the carrier slope may be changed instead of the Schmitt trigger thresholds, but the slope values should be kept constant during the whole period.

d. Closed-loop issues: trade-off between settle time and static error;

By nature, the equivalent local controller implied by the analog computation is a simple proportional. A more sophisticated controller allowing to implement a more complex control law has to be identified, so that the different closed-loop performance indicators (static gain, settling time, damping) can be set independently.

e. Carrier choice: the interleaving principle is attached to the triangular carrier;

The local controller computes the neighbors' triangular carrier difference and superposes it on the triangular signal generator thresholds. A more generic method has to be proposed that dissociates these two intrinsic points, i.e. the shape of the carrier and the interleaving management.

f. Inter-connection number issue: a large number of connections is required (4 per LC).

To reduce communication lines, each neighbor connections can be a input/output and perform AND operations by wire. E.g. if the outputs are of type open drain, when connected together, each local controller would obtain on the wire the AND result of the LCs outputs. However, reducing the number of connections may compromise the fail-operational status and potentially add some SPOFs.

These 6 points can be summarized as the following actions to take:

a. Avoid comparing analog signals from different sources;
b. Avoid using an external analog signal to control directly the local phase-delay;
c. Avoid altering the carrier shape during a period;
d. Use a more sophisticated controller transfer function;
e. Use a local control structure made of several dissociated functions (local controller + VCO);
f. Mutualize connections if possible.

The study of the new interleaving technique will be described thereafter.

## IV.2. **New improved self-interleaving technique building blocks**

To avoid signal mismatches, the module communications have to be based on digital signals, such as a clock signal. Many multiphase control structures do not require interleaved carriers but only interleaved clocks, such as peak/valley detection current-mode control or Digital PWM (D-PWM). In the literature and in many commercial applications, the interleaved clocks are generated from a global synchronization clock and a local Delay Locked Loop (DLL). In these applications, one oscillator generates the global synchronization clock and imposes the frequency to the other modules. The local interleaved clocks are generated using DLLs. Then, for our case, if a carrier is required, it can be generated using the same phase-delay of the local interleaved clock one.

Now, in order to remove any SPOF, if the global synchronization clock is avoided, an oscillator has to be associated to each local interleaved signal. To obtain the targeted interleaving, a Voltage Controlled Oscillator (VCO) has to be used and a feedback loop is required to position its phase-delay in the middle of other two neighboring signals. It is comparable to a PLL system that locks the VCO output clock signal $clk_o$ to an input clock signal $clk_i$, using a phase detector and a loop filter, such as the one shown in Figure IV-1.

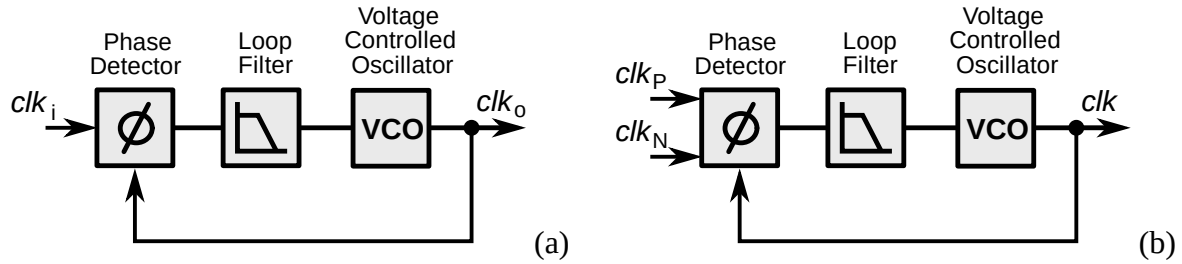



*Figure IV-1 – Phase-Locked Loop: a) Classical, b) Expected self-interleaving block diagram.*

However, to provide the interleaving with this new approach, a particular phase detector has to be designed, not only to observe the clock frequency, but also to interleave the local VCO clock signal $clk$ with the two external clock signals $clk_P$ and $clk_N$.Figure IV-1(b) shows an example of the expected block diagram of the circular-chain interleaving module that dissociates clearly each function block of the structure.

It should be noted that the triangular carrier self-interleaving system, previously described in chapter III, is an application case of this approach, but using some analog shortcuts. Indeed, in that previous case, the “PLL” function is resulting of the analog computations made and is not that clear such as a classical PLL circuit: the subtraction of the neighbors’ carriers is equivalent of a phase detector, the voltage gain is equivalent to the loop filter, the triangular carrier generator with adjustable threshold acts like a VCO and includes a built-in feedback.

Thereafter, the implementation of each function composing the expected self-interleaving block diagram has to be identified.

### IV.2.1. VCO and triangular carrier generator

The objective of this new system is to interleave clock signals and then obtain interleaved carrier signals of any shape if required. So, a VCO that generates a clock signal is required. It is known that the carrier generator, previously described in chapter III, has an internal digital signal that is locked on the triangular carrier. So the digital signal Phase-Delay (PD) is the same as the triangular signal PD. The triangular carrier generator based on operational amplifiers can be slightly modified to become a classic VCO, such as the one shown in Figure IV-2 from Texas Instruments® LM358 datasheet. The equivalent signals OUTPUT1, OUTPUT2 and $+V_C{}^*$ will be called $clk$, $v_{tri}$ and $u$, respectively, in this study. Here, the level of the signal $u$ imposes the clock frequency. The peak of the triangular signals is aligned with the clock rising-edge and its valley is aligned with the clock falling-edge.

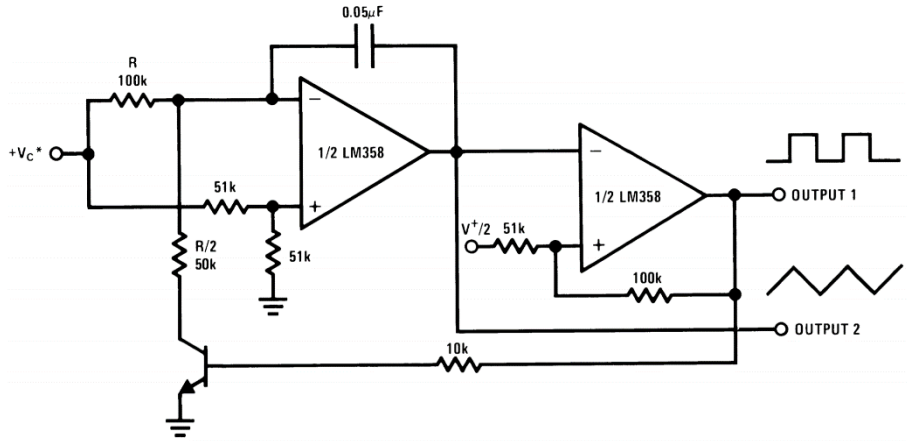



*Figure IV-2 – Texas Instruments LM358 datasheet: VCO and triangular carrier generator.*

Now, if the edges of the square clock signals involved in the system are equally spaced in time, so the square clock signals become interleaved. So the triangular signals will be interleaved accordingly.

### IV.2.2. Phase detector

The PDs present between the local and the neighbors' digital signals can be computed using a common phase detectors such as the one used in a PLL or a DLL circuit. It should be noted that a Charge-Pump (CP) (charge manager using two control signal $UP$ and $DN$) is included in the phase detector. The position error of the local clock can be obtained by making the difference of two phase detector outputs, i.e. resulting in a Differential Phase Detector (DPD). An exclusive OR (XOR, $\oplus$) logic gate is commonly used as a phase detector operator.

An example of this operation is shown in Figure IV-3, where (a) shows a carrier correctly positioned (interleaved) and (b) shows a carrier slightly late (phase-delay case), where $v_{triP}$, $v_{tri}$ and $v_{triN}$ are respectively the previous, the local and the next triangular signals, $clk_P$, $clk$ , $clk_N$ are their related clock signals, all with the same frequency, and $\theta_P$, $\theta$, $\theta_N$ are their respective PDs.

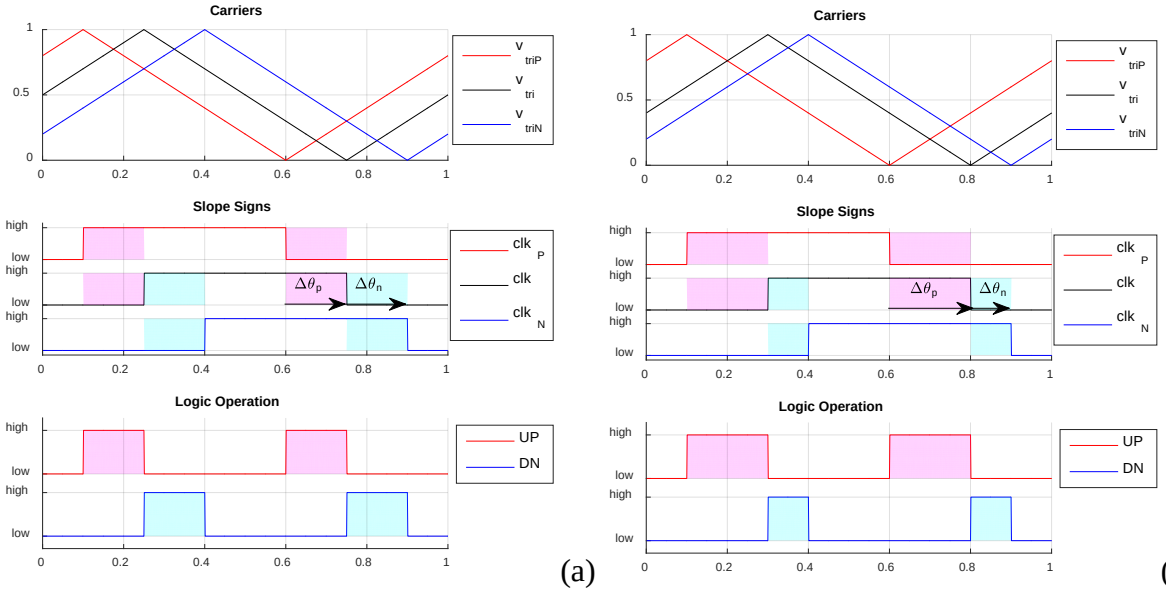



*Figure IV-3 – Phase detector operations on digital signals (outputs of the Schmitt triggers): a) carrier correctly positioned, b) carrier slightly late.*

Eq. (IV-1) develops the required phase detector expressions used in Figure IV-3.

$$UP = clk_P \oplus clk \qquad DN = clk \oplus clk_N \qquad \text{(IV-1)}$$

It should be noted that, in case (a), the PD of signals $v_{triP}$ and $v_{tri}$ is equal to the PD of signals $v_{tri}$ and $v_{triN}$. The same remark applies for their respective clock signals. Then, the pink and blue surfaces observed on the XOR logic gate outputs are equal. However, in case (b), the PDs are different and the resulting pink and blue surfaces are different. The charge-pump converts these surfaces into two amounts of charges delivered to the loop filter. The loop filter convert the charges to a voltage to control the local VCO.

Nevertheless, the XOR DPD has its limitations because each unitary phase detector (XOR gate) is not equivalent to a bijective function. In other words, the XOR operation periodical average ($\langle\, clk_A \oplus clk_B \,\rangle_{T_0}$) results on a signal which duty-cycle is proportional to the absolute value of the phase difference, as shown in Eq. (IV-2), where $clk_A$ and $clk_B$ are two clock signals at the same frequency with period $T_0$ and the normalized phase-delay $\theta_A$ and $\theta_B$, respectively. It does not indicate if each signal is in phase-delay or phase-advance.

$$\theta_A, \theta_B \in [\,0, 1[, \qquad \Delta\theta_{A,B} = \theta_B - \theta_A \quad \Longrightarrow \qquad \text{(IV-2)}$$

$$\langle\, clk_A \oplus clk_B \,\rangle_{T_0} = f(\theta_A, \theta_B) = \begin{cases} 2\left|\Delta\theta_{A,B}\right|, & if\ \left|\Delta\theta_{A,B}\right| \le 0.5 \\ 2 - 2\left|\Delta\theta_{A,B}\right| & if\ 0.5 < \left|\Delta\theta_{A,B}\right| < 1 \end{cases}$$

It can be noted that a plot of the XOR phase detector function presents a "V" shape if $\theta_A$ or $\theta_B$ is equals to 0.5. It can be generalized with a triangular shape for different $\theta_A$ or $\theta_B$ values.

Now, the position error of the local signal with its two neighbors is provided by making the average of the difference of two phase detector output signals. The perceived error $\varepsilon_\theta{}'$ when using the XOR gates is shown in Eq. (IV-3).

$$\begin{cases} \theta_P, \theta, \theta_N \in [\,0, 1[ \\ \theta_N \ge \theta_P \end{cases} \Rightarrow$$
$$\varepsilon_\theta{}' = f(\theta_P, \theta, \theta_N) = \frac{\langle\, clk_P \oplus clk \,\rangle_{T_0} - \langle\, clk \oplus clk_N \,\rangle_{T_0}}{4} \qquad \text{(IV-3)}$$

Then, the perceived error $\varepsilon_\theta{}'$ results in a subtraction of two triangular functions. Its value depends both on the relative position of the local signal $\varepsilon_\theta$ and also the distance in phase of the two neighbors $\Delta\theta_{P,N} = \theta_N - \theta_P$. The result is shown in Figure IV-4.

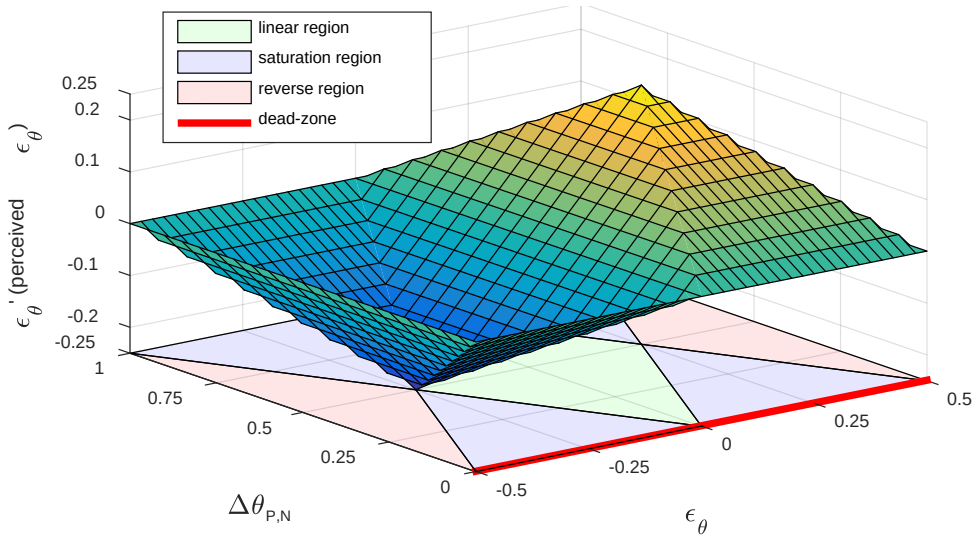



*Figure IV-4 – Perceived error with XOR phase detector.*

Figure IV-4 shows that the response of DPD described in Eq. (IV-3) results in 4 distinct regions:

a. Linear region (green): perceived error $\varepsilon_\theta{}'$ equals to $\varepsilon_\theta$;
b. Saturation region (blue): perceived error $\varepsilon_\theta{}'$ non null and do not varies with $\varepsilon_\theta$;
c. Reverse region (pink): perceived error $\varepsilon_\theta{}'$ decreases while $\varepsilon_\theta$ increases.
d. Dead zone (red): perceived error $\varepsilon_\theta{}'$ null while $\varepsilon_\theta$ non null;

It should be noted that all initial condition complying with a Proper Interleaving Arrangement (PIA) are in the DPD linear region and leads consequently to a correct interleaving if the system is stable and the disturbances are moderated.

The XOR gate reacts to the rising and falling edges of the signals, resulting in two measurements per period. However, the double measurement can bring issues. For instance, if the clock signal duty-cycles are not equal, a dead-zone around the region where the error is close to zero may appear. This dead-zone will generate jitter and must be eliminated. A different logic can be used to solve this issue, such as detecting only the phase-delay around one edge, for instance around the falling edge (triangle valley) shown in Eq. (IV-4).

$$UP = \overline{clk_P} \cdot clk \qquad DN = \overline{clk} \cdot clk_N \qquad \text{(IV-4)}$$

This single edge approach provides the same results as the ones of the XOR gate, but the error measurement operator gain is divided by 2.

Now special care has to be taken regarding the dead-zone around the region where neighbors are coincident, i.e. $\Delta\theta_{P,N} = 0$. This region can bring uncertainty during start-up. Moreover, when high number of local controllers is used, it may result in non-deterministic steady-state condition. This approach has also a limited lock-in range, so the frequency difference of the clock signals has to be small.

In a real case with disturbances, the dead-zone can lead to a wrong interleaving even if the start condition is PIA. Then, the linear region can be increased around the origin ($\varepsilon_\theta = 0, \Delta\theta_{P,N} = 0$) to guarantee a correct interleaving in steady-state. Other DPD options to increase the linear region around the origin are discussed in Annex E.

The single edge approach is adopted, due to the continuity insured in the whole PD operational domain. Its transient response could be slower in some cases due to the perceived error being smaller than the real error outside the linear region. However, the system stays in the linear region in normal operation even in extreme cases where some elements are in the bounds of $\varepsilon_\theta{}' = \varepsilon_\theta$ , such as the case of start-up by groups ($\Delta\theta_{P,N} = 0.50, |\varepsilon_\theta| = 0.25$) and the singular case of reconfiguration from 4 to 3 active carriers ($\theta_P - \theta_N = 0.75, |\varepsilon_\theta| = 0.25$).

The single edge approach presents the advantage of performing the interleaving base on the detection of only one edge of the clock signal, either the rising or falling-edge. Then, the events synchronized with these edges will be correctly interleaved. For instance, when a triangular carrier is used with low duty-cycle, in order to avoid any PWM signal interleaving error related to carrier symmetry mismatches, it is better to interleave the edges related to the triangle valley.

### IV.2.3. Loop filter

The durations of the phase detector output signals $UP$ and $DN$ are converted into an equivalent amount of charges by the charge-pump circuit. It should be noted that the charge-pump output is a current named $i_P$ with high frequency content because the current sources are switched. As the name explains, the Loop Filter remove the high frequency content and sets the PLL closed-loop behavior.

The system proposed here must have the VCO voltage constant in between periods, requiring them a very low cut-off frequency. However, it implies in a very limited transient response. To filter properly the CP current and have a good transient response, the loop filter will be divided in two: a periodic average circuit and a generic controller. Its simplified electrical diagram is shown in Figure IV-5.

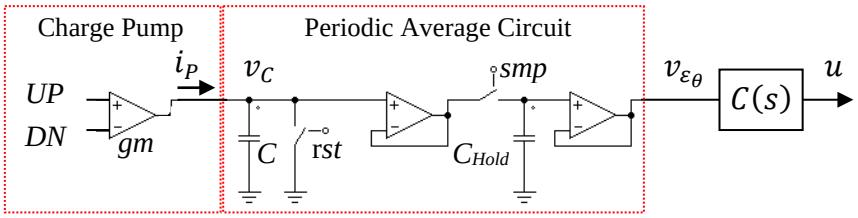



*Figure IV-5 – Simplified electrical diagram used to compute the periodic average of the charge-pump current.*

The charge-pump output is connected to a capacitor $C$ to store the resulting charges within a full clock period, producing a voltage $v_C$ proportional to the average $i_P$ value. Then, $v_C$ is sampled, i.e. a copy is stored in the capacitor $C_{Hold}$, using the "smp" signal. When "smp" is not active, $C_{Hold}$ holds the last sampled voltage. Then, $v_C$ is reset to zero using the signal "rst" at each period, avoiding any integration effect. The resulting maintained voltage is noted $v_{\varepsilon_\theta}$ because it is a voltage representing the error. The sampling and reset operations are synchronized with the opposite clock edge used for the error measurement. As a result, a half period delay is added in the control loop. The control signals and voltage waveforms are shown later in Figure IV-9.

#### IV.2.3.1. Periodic Average Circuit

Figure IV-6 shows the current $i_C$ waveform of the charge-pump circuit when the local carrier is constant and the neighbor's difference is kept constant $\Delta\theta_{P,N} = 0.5$. At the same time, the neighbor's frequency changes so that the PDs change to produce a local error in a cosine shape with an amplitude of 0.25 and a period equal to 10 carrier periods. It is clearly shown that the current $i_C$ is directly dependent of the interleaving error and consequently the amount of charges provided to (blue area) or removed from (pink area) the capacitor.

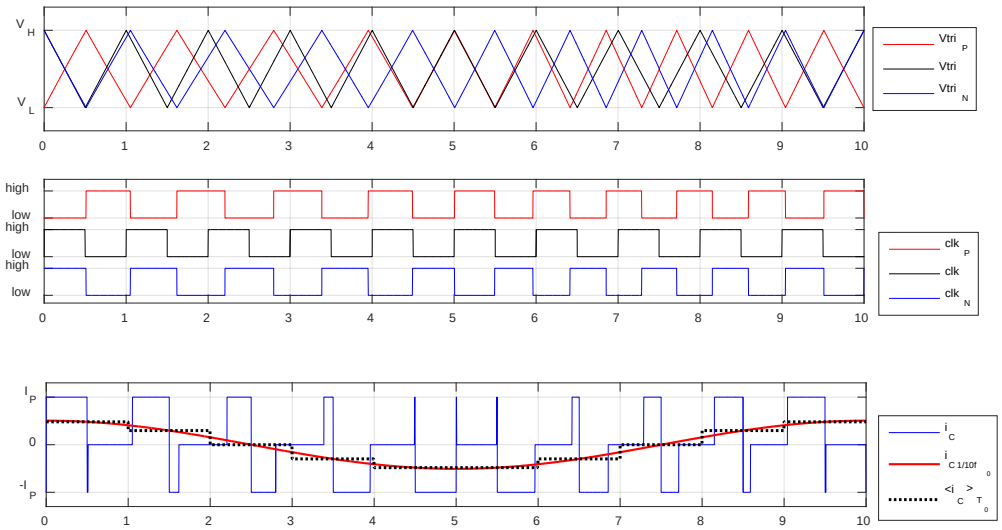



*Figure IV-6 – Current of the charge-pump circuit $i_C$ as a function of the neighbor's PD (with $\theta_N - \theta_P = 0.5$), the fundamental $i_{C\,1/10\,f_0}$ and the periodical average $\langle i_C \rangle_{T_0}$.*

The $i_C$ fundamental harmonic waveform $i_{C\,1/10\,f_0}$ at 1/10 of the carrier frequency is shown. The curb $\langle i_C \rangle_{T_0}$ is the periodic average of $i_C$, i.e. a constant current applied within the period $T_0$, between $k\,T_0$ and $(k+1)\,T_0$. Both signals $i_C$ and $\langle i_C \rangle_{T_0}$ are representative of the error. It is confirmed by their Fast Fourier transform shown in Figure IV-7, where the frequency axis is normalized to the carrier frequency.

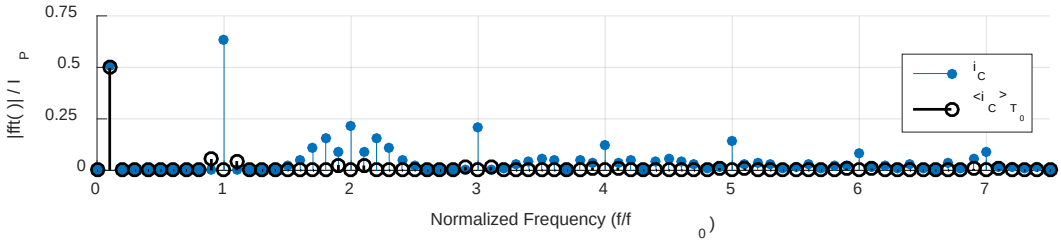



*Figure IV-7 – Normalized Fast Fourier Transform (FFT) of $i_C$ and $\langle i_C \rangle_{T_0}$.*

The $i_C$ signal FFT presents several high frequency harmonics. The desired information is provide at low frequency (here $f_0/10$), but the dominant harmonic at the carrier frequency $f_0$ has to be filtered. It can be noted most of the high frequency harmonics are mitigated with the $\langle i_C \rangle_{T_0}$ signal FFT.

#### IV.2.3.2. Corrector

The corrector $C(s)$ add compensation poles and zeros to ensure the system closed-loop criteria, such as a small static error, the system stability and the transient response performances. The controller output $u$ (VCO control voltage input) should also be kept constant each period to avoid disturbing the slope of the VCO triangular signal during reconfigurations and steady-state operation. However, as a periodic average of the error is made, the voltage $u$ will vary slowly during the period if the corrector $C(s)$ has proportional behavior.

The controller *C*(*s*) can be implemented by several means. For instance, with a simple analog Op-Amp and its appropriate feedback made of resistors and capacitors. The resulting controller would be very flexible because many different transfer functions could be synthetized. The correction is considered to have slow variation between two successive samples and to be constant in steady-state. A switched capacitor approach could also be considered to implement the sampling circuit and the corrector *C*(*s*) at the same time in a unique stage (both functions would be merged).

Considering all these elements, a small-signal model of one interleaving bloc will be proposed. Then the whole system with $N$ interleaved carriers will be modelled and its stability criteria will be revealed.

## IV.3. **Single loop model**

The static behavior of all elements was developed in the previous section. Now, a small signal continuous time model of a single interleaving element is proposed. As presented earlier, three subsystem have to be modeled. They are:

1. The Error Detector $H_{error}(s)$, composed by:
    a. The Phase Detector,
    b. The Charge-Pump,
    c. The Periodic Average circuit,
2. The Corrector $C(s)$, composed by:
    a. A stage providing the appropriate poles and zero,
3. The VCO $H_{VCO}(s)$.

The error detector, noted $H_{error}(s)$, combine three subsystems that are involved in an unique transfer function. Figure IV-8 shows a simplified block diagram representing the LC internal elements, where $C(s)$ and $H_{VCO}(s)$ are the controller and the VCO transfer functions respectively. As shown in the figure, it is assumed that an additional noise signal $n(t)$ appears at the corrector input and also an additional disturbance signal $d(t)$ appears at the VCO input.

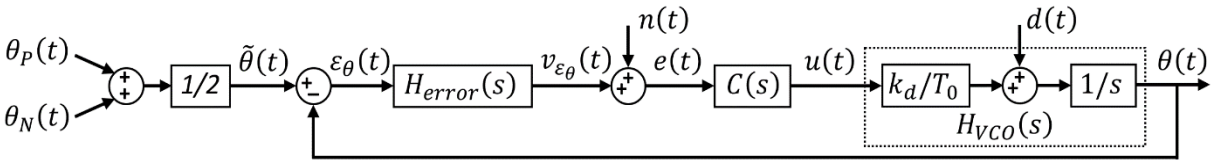



*Figure IV-8 – Small signal block diagram representing one LC elements.*

In our application, described later, the corrector $C(s)$ is composed by an operational amplifier with a feedback loop. Its transfer function, noted $C(s) = U(s)/E(s)$, will be chosen later.

The signal $\theta$ represents the normalized PD measurement of the local clock signal to a virtual reference clock signal at the frequency $f_0$. It should be noted that no real reference clock signal appears in this system, but a virtual one is used here for modeling reasons. The classical VCO transfer function linearized around an operation point is composed by an integrator and a normalized gain $k_d$ $[V^{-1}]$, called the VCO gain factor, such as $H_{VCO}(s) = \Theta(s)/V_c(s) = k_d/(T_0 \cdot s)$. The disturbance signal $d(t)$ is assumed constant and represents the frequency difference $\delta f$ of the local oscillator frequency $f = f_0 + \delta f$ with the steady-state frequency noted $f_0$, then $d(t) = \delta f$.

### IV.3.1. Error detector

The analog triangular carrier self-interleaving circuit shown in the previous chapter share its triangular carrier waveform with its neighbors. In that case, the PD measurement of the local carrier seemed to be sampled, but this is not correct. Indeed, the triangular carrier PD is available during the whole period, its value is constant and the corrections are sampled when the triangular signal slope changes.

In this new approach, the clock signals edges are used to obtain the PD and the PD can be identified only during the switching instant. In the single edge approach, the PD is observed only once a period. As a result, the PD measured is by nature sampled. However, the correction signal $u$ is a continuous signal.

Figure IV-9 shows a simulation result involving the signals of Figure IV-5 and Figure IV-8. On top of the figure are shown three analog triangular carriers $v_{triP}$, $v_{tri}$ and $v_{triN}$, related to the previous, local and next PDLC respectively. For each of them, the associated digital clock signals $clk_P$, $clk$ and $clk_N$ are also shown, which are the Schmitt trigger output signals used by the local carrier generators of Figure IV-2. In one carrier generator, the carrier and the clock signals are always locked in the same phase and frequency because one is constructed based on the other. It should be noted that the clock edges are aligned with the peak and valley of the triangular signal.

In this simulation, the local clock signal period is assumed to be always uniform equal to $T_0$. At the $k^{th}$ time period, the local clock rising edge instant is noted $k$, related to time instant $kT_0$. The PD between $clk_P$ and $clk$ falling edges at the previous half period is noted ${\Delta\theta_P}^k$, and the PD between $clk$ and $clk_N$ falling edges at the previous full period is noted ${\Delta\theta_N}^k$.

The signals $v_C$ and $v_{\varepsilon_\theta}$ related to the periodical average circuit are also shown with their iterations with control signal. A first signal called $smp$ is generated by comparing the triangular

carrier with a constant voltage level resulting in a digital signal centered with the triangle peak and showing a 10% duty-cycle. Then, the sample signal $smp$ and reset signal $rst$ are generated using logic gates with the clock signal, with $smp = sync \cdot \overline{clk}$ and $rst = sync \cdot clk$. One can observe that $v_C$ increases with a constant rate when $UP$ is high and decreases with the same constant rate when $DN$ is high, $v_{\varepsilon_\theta}$ assumes the same value as $v_C$ when $smp$ is high and $v_C$ goes back to its initial positions when $rst$ is high.

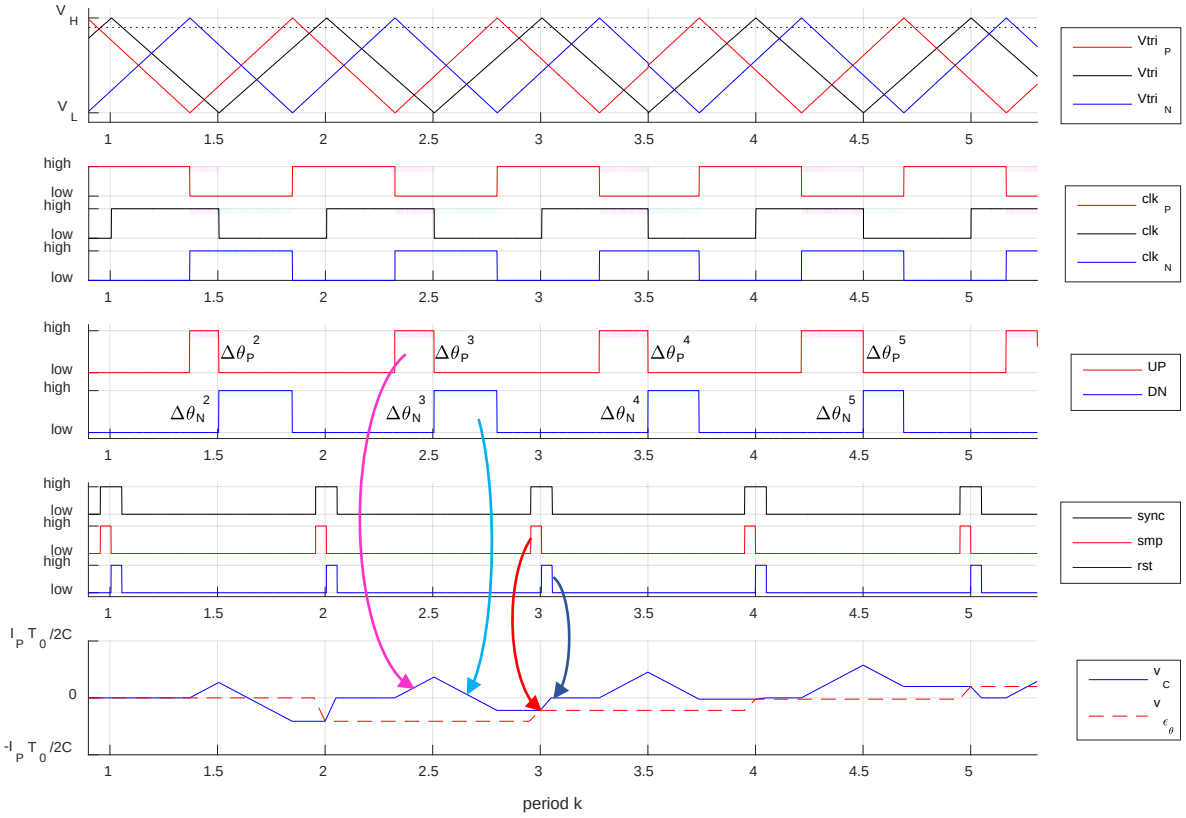



*Figure IV-9 – Simulation of the single edge error PD measurement method.*

The static relationship between the charge-pump current and the clock signal PDs has been shown in the last section. Now, the dynamic relationship existing between the three clock signals $clk_P(t)$, $clk(t)$, $clk_N(t)$ and the sampled PD error $v_{\varepsilon_\theta}(t)$ has to be revealed.

The expression of the maintained voltage $v_{\varepsilon_\theta}(t)$, shown in Eq. (IV-5), is the convolution of $v_C{}^*(t)$, the capacitor $C$ sampled voltage, $h_{\mathrm{ZOH}}(t)$, the Zero-Order hold impulse response, and $rect(\cdot)$ is the rectangular function.

$$v_{\varepsilon_\theta}(t) = v_C{}^*(t) * h_{\mathrm{ZOH}}(t) \qquad \text{where} \qquad h_{\mathrm{ZOH}}(t) = rect\left(\frac{t - T_0/2}{T_0}\right) \qquad \text{(IV-5)}$$

The capacitor $C$ sampled voltage expression is shown in Eq. (IV-6).

$$v_C{}^*(t) = \sum_{k=-\infty}^{\infty} v_{\mathrm{C}}(k\,T_0) \cdot \delta\left(\frac{t - k\,T_0}{T_0}\right) \tag{IV-6}$$

The capacitor $C$ voltage $v_{\mathrm{C}}(k\,T_0)$ can be written using its fundamental expression related to the integral of the charge-pump output current $i_{\mathrm{P}}(t)$. Its expression shown in Eq. (IV-7) is composed by the current integral during a period $T_0$ plus its initial voltage value. Due to the reset circuit, it is assumed the initial capacitor voltage $v_{\mathrm{C}}\big((k-1)\,T_0\big)$ is null. Then, it become easy to determine the charge stored into the capacitor during the k$^{th}$ period, noted $Q^k$.

$$v_{\mathrm{C}}(k\,T_0) = \frac{1}{C}\int_{(k-1)\,T_0}^{k\,T_0} i_{\mathrm{P}}(t)\,dt + \cancel{v_{\mathrm{C}}\big((k-1)\,T_0\big)} = \frac{Q^k}{C} \tag{IV-7}$$

The charge-pump output current $i_{\mathrm{C}}(t)$ expression is shown in Eq. (IV-8), where $I_{\mathrm{P}}$ is a constant reference current, $UP(t)$ and $DN(t)$ are its digital input control signals.

$$i_{\mathrm{P}}(t) = I_{\mathrm{P}}\,[UP(t) - DN(t)] \tag{IV-8}$$

The charge $Q^k$ can be identified from Eq. (IV-7) and then solved, as shown in Eq. (IV-9).

$$Q^k = \int_{(k-1)\,T_0}^{k\,T_0} i_{\mathrm{P}}(t)\,dt = I_{\mathrm{P}}\,T_0\left({D_{UP}}^k - {D_{DN}}^k\right) \tag{IV-9}$$

with

$${D_{UP}}^k = \frac{1}{T_0}\int_{(k-1)\,T_0}^{k\,T_0} UP(t)\,dt = \frac{{\mathrm{t}_L}^k - {\mathrm{t}_P}^k}{T_0}$$

$${D_{DN}}^k = \frac{1}{T_0}\int_{(k-1)\,T_0}^{k\,T_0} DN(t)\,dt = \frac{{\mathrm{t}_N}^k - {\mathrm{t}_L}^k}{T_0}$$

where ${\mathrm{t}_P}^k$, ${\mathrm{t}_L}^k$ and ${\mathrm{t}_N}^k$ are the instant where each interleaved $clk$ falling edge event happens, ${D_{UP}}^k$ and ${D_{DN}}^k$ are UP and DW signals duty cycles at period $k$.

There are two main ways to measure a phase-delay: either using instantaneous phasor values or using the time delay between the instants where the signals passes through the same level. It should be noted that the calculated charge in Eq. (IV-9) is equals to the definition using times delays, shown in Eq. (IV-10).

$$\Delta\theta_P{}^k \triangleq \frac{\Delta t_P{}^k}{T_0} \qquad\qquad \Delta\theta_N{}^k \triangleq \frac{\Delta t_N{}^k}{T_0} \tag{IV-10}$$

where $\Delta t_P{}^k = {\mathrm{t}_L}^k - {\mathrm{t}_P}^k$ $\qquad$ $\Delta t_N{}^k = {\mathrm{t}_N}^k - {\mathrm{t}_L}^k$

It should be noted that equalizing the $\Delta t_P{}^k$ and $\Delta t_N{}^k$, i.e. $v_{\varepsilon_\theta}(t)$ equals to zero, leads to a properly interleaved system. Nevertheless, the phasor delay approach is needed to determine the transient behavior.

The phasor delay approach generate an instantaneous value, where all PDs are sampled together, i.e. synchronized at the same instant. However, the clock signal reveals its PD only in the edge event, the PDs at the falling edge events are expressed in Eq. (IV-11).

$$\theta_P(\mathrm{t}_P{}^k) = \frac{\mathrm{t}_P{}^k}{T_0} - k \qquad \theta(\mathrm{t}_L{}^k) = \frac{\mathrm{t}_L{}^k}{T_0} - k \qquad \theta_N(\mathrm{t}_N{}^k) = \frac{\mathrm{t}_N{}^k}{T_0} - k \qquad \text{(IV-11)}$$

To obtain the equivalent phasor measurement, $\theta_P$ and $\theta_N$ values must be expressed at the instant $\mathrm{t}_L{}^k$. The previous and next sampled PDs can be rewritten as a function of the local sampling time, as shown in Eq. (IV-12).

$$\theta_P(\mathrm{t}_P{}^k) = \theta_P\left(\mathrm{t}_L{}^k - \Delta t_P{}^k\right) \qquad \theta_N(\mathrm{t}_N{}^k) = \theta_N\left(\mathrm{t}_L{}^k + \Delta t_N{}^k\right) \qquad \text{(IV-12)}$$

From now, all required relations to determine $v_{\varepsilon_\theta}(t)$ are known and can be solved to express the perceived error. By substituting Eq. (IV-12) in Eq. (IV-11), then successively in Eq. (IV-10), Eq. (IV-9), Eq. (IV-7), Eq. (IV-6) and finally Eq. (IV-5), the expression of $v_{\varepsilon_\theta}(t)$ in Eq. (IV-13) is obtained after a rearrangement. Some matrix notation representing convolution sum have been also used to simplify the equation.

$$v_{\varepsilon_\theta}(t) = \frac{2\, I_\mathrm{P}\, T_0}{C}\, \delta(t - T_0/2) * h_{\mathrm{ZOH}}(t) * \sum_{k=-\infty}^{\infty} \begin{bmatrix} 0.5 \\ -1 \\ 0.5 \end{bmatrix}^T \begin{bmatrix} \theta_P\left(k\, T_0 - \Delta t_P{}^k\right) \\ \theta(k\, T_0) \\ \theta_N\left(k\, T_0 + \Delta t_N{}^k\right) \end{bmatrix} \cdot \delta\left(\frac{t - k\, T_0}{T_0}\right) \qquad \text{(IV-13)}$$

Eq. (IV-13) highlights that $\theta_P$ and $\theta_N$ are depend on themselves, $\Delta t_P{}^k$ and $\Delta t_N{}^k$, respectively, because the PD vary between periods and consequently $\Delta t_P{}^k$ and $\Delta t_N{}^k$ change. In chapter III the chain delay was constant (one sampling period to the previous) and the PD constant until next period.

### IV.3.2. Error detector Laplace transfer function

Now, error detector Laplace transfer function noted $V_{\varepsilon_\theta}(s)$ has to be obtained from $v_{\varepsilon_\theta}(t)$. However, it cannot be done with the expression of Eq. (IV-13) because $\theta_P$ and $\theta_N$ expressions have delays ($\Delta t_P{}^k$ and $\Delta t_N{}^k$) dependent on themselves. To avoid this issue, $\Delta t_P{}^k$ and $\Delta t_N{}^k$ can be approximated by their steady-state expected values, which is $T_0/N$ for a well interleaved system, under the assumption of small disturbances around the steady-state positions. This hypothesis is formulated on Eq. (IV-14).

$$\theta_P\left(k\, T_0 - \Delta t_P{}^k\right) \cong \theta_P(k\, T_0 - T_0/N) = \delta(t - T_0/N) * \theta_P(k\, T_0) \qquad \text{(IV-14)}$$

$$\theta_N\left(k\,T_0 + \Delta {t_N}^k\right) \cong \theta_N(k\,T_0 + T_0/N) = \delta(t + T_0/N) * \theta_N(k\,T_0)$$

The simplified expression of $v_{\varepsilon_\theta}(t)$ is detailled in Eq. (IV-15).

$$v_{\varepsilon_\theta}(t) \cong \frac{2\,I_P\,T_0}{C}\,\delta(t - T_0/2) * h_{ZOH}(t) * \sum_{k=-\infty}^{\infty} \begin{bmatrix} 0.5\,\delta(t - T_0/N) \\ -1 \\ 0.5\,\delta(t + T_0/N) \end{bmatrix}^T * \begin{bmatrix} \theta_P(t) \\ \theta(t) \\ \theta_N(t) \end{bmatrix} \cdot \delta\left(\frac{t - k\,T_0}{T_0}\right) \quad \text{(IV-15)}$$

The Laplace transform $V_{\varepsilon_\theta}(s)$ of $v_{\varepsilon_\theta}(t)$ approximation in Eq. (IV-15) is expressed in Eq. (IV-16).

$$V_{\varepsilon_\theta}(s) = \mathcal{L}\left\{\, v_{\varepsilon_\theta}(t) \,\right\} = \frac{2\,I_P\,T_0}{C} H_{ZOH}(s)\,H_{delay}(s) \begin{bmatrix} 0.5\,H_{delayP}(s) \\ -1 \\ 0.5\,H_{delayN}(s) \end{bmatrix}^T \begin{bmatrix} \Theta_P(s) \\ \Theta(s) \\ \Theta_N(s) \end{bmatrix} \quad \text{(IV-16)}$$

where:

$$H_{ZOH}(s) = \mathcal{L}\left\{\, h_{ZOH}(t) \,\right\} = \frac{1 - \mathrm{e}^{-sT_0}}{sT_0} \qquad H_{delay}(s) = \mathcal{L}\left\{\, \delta(t + T_0/2) \,\right\} = \mathrm{e}^{\frac{-sT_0}{2}}$$

$$H_{delayP}(s) = \mathcal{L}\left\{\, \delta(t - T_0/N) \,\right\} = \mathrm{e}^{\frac{-sT_0}{N}} \qquad H_{delayN}(s) = \mathcal{L}\left\{\, \delta(t + T_0/N) \,\right\} = \mathrm{e}^{\frac{sT_0}{N}}$$

It can be observed that the block diagram in Figure IV-8 is not coherent with this transfer function because the delay transfer functions $H_{delayP}(s)$ and $H_{delayN}(s)$ are missing, being valid only in the case where $\theta_P$ and $\theta_N$ are constant.

### IV.3.3. Plant transfer function

It is proposed here to consider the plant transfer function noted $P(s)$, i.e. the combination of process and actuator transfer functions, as the function composed of $H_{error}(s)$ and $H_{VCO}(s)$, where $H_{error}(s)$ is composed by the three first terms of $V_{\varepsilon_\theta}(s)$, while the last two terms are equivalent to the loop subtractor and the error calculation. The plant transfer function is shown in Eq. (IV-17). In the single loop case, the PDs inputs $\Theta_P(s)$ and $\Theta_N(s)$ are considered null and do not appears in $P(s)$.

$$P(s) = \frac{V_{\varepsilon_{\theta H}}(s)}{U(s)} = \mathrm{H}_{error}(s)\,H_{VCO}(s) \quad \text{(IV-17)}$$

where: $\mathrm{H}_{error}(s) = \dfrac{2\,I_P\,T_0}{C}\,H_{ZOH}(s)\,H_{delay}(s) \qquad H_{VCO}(s) = \dfrac{k_d}{s\,T_0}$

It should be noted that $P(s)$ is independent of the period $T_0$ because term $T_0$ in $\mathrm{H}_{error}(s)$ simplify with the term ${T_0}^{-1}$ in $H_{VCO}(s)$. The controller transfer function $C(s)$ is not

present in $P(s)$ and is considered in series with it in the forward path. An applicative case with the following parameters is defined:

| | | |
|---|---|---|
| $f_0 = 88\ kHz$ | $I_P = 2 \text{ x } 2.5\ V/16\ k\Omega$ | $k_d = \frac{1}{2.5\ V}\frac{10\ k\Omega}{50\ k\Omega}$ |
| $T_0 = 1/f_0 = 11.36\ us$ | $C = 1\ nF$ | |

Figure IV-10 shows bode diagram of $P(s)$ to the presented applicative case.

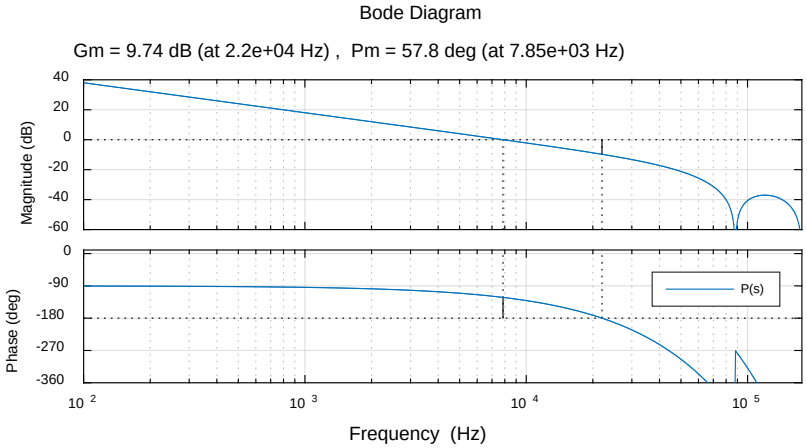



*Figure IV-10 – P(s) bode diagram with phase and gain margins.*

This applicative case plant $P(s)$ has acceptable phase margin (>57°) at 7.85 kHz, where its magnitude is 0 dB. As conclusion, this system does not present particular stability issues. Assuming a closed-loop cutoff frequency $f_c$ equals to 7.85 kHz, the expected damping factor is $\xi \cong PM/100 = 0.58$ if the corrector do not changes the phase in $f_c$ region. A proportional controller with a unitary gain would provide the expected transient response. A phase lag can be added to increase the static gain and cancel the steady-state error.

At this point, the model of one local control loop is known, but it cannot reveal the stability criterion and dynamic behaviors of the global system. To do so, similar studies made in the previous chapters on the global system response will be carried out with this one.

## IV.4. **Overall system modelling**

As in the previous chapters, the local errors are computed using the matrix $\boldsymbol{L}$ that represents the circular chain of communications, i.e. the connections between the LCs. It is assumed that all LCs in the circular chain are identical, including an error detector, a VCO, and a controller as well.

The same procedure is adopted here to find the overall system model. The study of the system stability with a generic number $N$ of LCs, including the several connections existing between them, is performed using a matrix approach. According to the circular-chain sequence, the PDs are numbered arbitrarily from 1 to $N$, from previous to next direction, from $\theta_1$ to $\theta_N$,

and then represented by a column vector $\boldsymbol{\theta}$ (in bold in the following equations). The order of all matrices and vectors is $N$. The block diagram representing the all the elements of this interleaving system is shown in Figure IV-11.

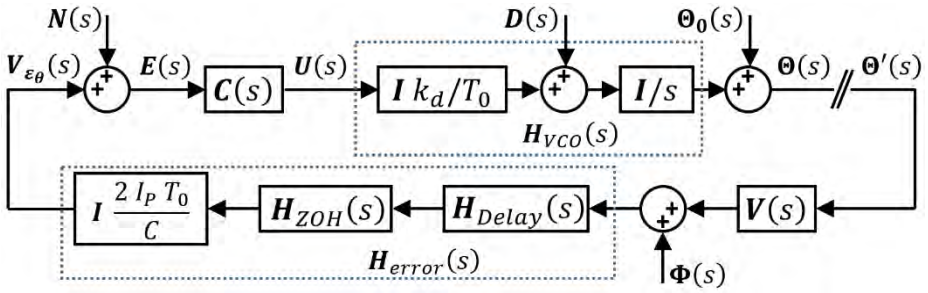



*Figure IV-11 – Overall system model block diagram.*

For computation purpose, the previous PD vector $\boldsymbol{\theta}_P$ and the next PD vector $\boldsymbol{\theta}_N$ are defined in Eq. (IV-18) using the circular shift matrix $\boldsymbol{S}$ expressed in Eq. (III-11) and its conjugate transposed $\boldsymbol{S}^*$, equal to its transposed $\boldsymbol{S}^T$ because $\boldsymbol{S}$ is real.

$$\boldsymbol{\theta}_P = \boldsymbol{S}\,\boldsymbol{\theta} \qquad\qquad \boldsymbol{\theta}_N = \boldsymbol{S}^*\,\boldsymbol{\theta} \tag{IV-18}$$

The target PD in the vector format, noted $\widetilde{\boldsymbol{\theta}}(t)$, is shown in Eq. (IV-19), where $\boldsymbol{\varphi}(t)$ vector is calculated by the "*target operator*". $\boldsymbol{\varphi}(t)$ does not affect the stability study.

$$\widetilde{\boldsymbol{\theta}}(t) = 0.5\,[\boldsymbol{\theta}_P(t) + \boldsymbol{\theta}_N(t)] + \boldsymbol{\varphi}(t) \tag{IV-19}$$

The PD error in the vector format, noted $\boldsymbol{\varepsilon}_\theta(t)$, is shown in Eq. (IV-20), where $\boldsymbol{L}$ is a matrix representing the circular chain connections.

$$\boldsymbol{\varepsilon}_\theta(t) = \widetilde{\boldsymbol{\theta}}(t) - \boldsymbol{\theta}(t) = \boldsymbol{L}\,\boldsymbol{\theta}(t) + \boldsymbol{\varphi}(t) \tag{IV-20}$$

The Laplace transform of the error $\boldsymbol{\varepsilon}_\theta(t)$ is noted $\mathbf{E}_{\boldsymbol{\Theta}}(s)$ and shown in Eq. (IV-21).

$$\boldsymbol{E}_{\boldsymbol{\Theta}}(s) = \boldsymbol{L}\,\boldsymbol{\Theta}(s) + \boldsymbol{\Phi}(s) \tag{IV-21}$$

However, the error detector circuit of Figure IV-8 cannot detect directly $\varepsilon_\theta$, only the voltage $v_{\varepsilon_\theta}$ related to it. The $V_{\varepsilon_\theta}(s)$ expression in the single loop case shown by Eq. (IV-16) can be rewritten in the matrix format noted $\boldsymbol{V}_{\varepsilon_\theta}(s)$ as detailed in Eq. (IV-22).

$$\boldsymbol{V}_{\varepsilon_\theta}(s) = \frac{2\,I_P\,T_0}{C} H_{ZOH}(s)\,H_{delay}(s)\,\boldsymbol{E}_{\boldsymbol{\Theta}}{}'(s) \tag{IV-22}$$

where $\boldsymbol{E}_{\boldsymbol{\Theta}}{}'(s)$, shown in Eq. (IV-23), is the perceived error,

$$\boldsymbol{E}_{\boldsymbol{\Theta}}{}'(s) = \boldsymbol{L}(s)\,\boldsymbol{\Theta}(s) + \boldsymbol{\Phi}(s) \tag{IV-23}$$

and $\boldsymbol{L}(s)$, shown in Eq. (IV-24), is a matrix representing the circular chain connections with the neighbors' delays $H_{delayP}(s)$ and $H_{delayN}(s)$.

$$\boldsymbol{L}(s) = 0.5\left(H_{delayP}(s)\,\boldsymbol{S} + H_{delayN}(s)\,\boldsymbol{S}^*\right) - \boldsymbol{I} \tag{IV-24}$$

This expression can be simplified by removing from the model the neighbors measurement delays $H_{delayP}(s)$ and $H_{delayN}(s)$. Then, the error vector $\boldsymbol{E_\Theta}(s)$ can appear in the final expression, as shown in Eq. (IV-25), because $\boldsymbol{L}(s)$ becomes $\boldsymbol{L}$. It should be noted that $\boldsymbol{L}(j0) = \boldsymbol{L}$.

$$\boldsymbol{V}_{\varepsilon_\theta}(s) = \frac{2\, I_\mathrm{P}\, T_0}{C} H_{ZOH}(s)\, H_{delay}(s)\, \boldsymbol{E_\Theta}(s) \tag{IV-25}$$

The corrector and the VCO matrix transfer functions, $\boldsymbol{C}(s)$ and $\boldsymbol{H}_{VCO}(s)$, are diagonal. Their expressions are provided in Eq. (IV-26), where $\boldsymbol{I}$ is the identity matrix and $\boldsymbol{D}(s)$ the VCO frequency disturbance vector.

$$\boldsymbol{C}(s) = \frac{\boldsymbol{U}(s)}{\boldsymbol{E}(s)} = C(s)\,\boldsymbol{I} \qquad \boldsymbol{\Theta}(s) = \boldsymbol{H}_{VCO}(s)\begin{bmatrix}\boldsymbol{U}(s)\\ \boldsymbol{D}(s)\end{bmatrix} = \begin{bmatrix}H_{VCO}(s)\,\boldsymbol{I} & \frac{1}{s}\boldsymbol{I}\end{bmatrix}\begin{bmatrix}\boldsymbol{U}(s)\\ \boldsymbol{D}(s)\end{bmatrix} \tag{IV-26}$$

The connections between the error detector and the corrector have in common the same disturbances, noted $\boldsymbol{N}(s)$ in the vector format as shown in Eq. (IV-27).

$$\boldsymbol{E}(s) = \boldsymbol{V}_{\varepsilon_\theta}(s) + \boldsymbol{N}(s) \tag{IV-27}$$

The plant transfer function comprising the Multiple Inputs and Multiple Outputs (called a MIMO system) of this system is noted $\boldsymbol{P}(s)$ and shown in Eq. (IV-28).

$$\boldsymbol{P}(s) = \frac{\boldsymbol{V}_{\varepsilon_\theta}(s)}{\boldsymbol{U}(s)} = -\mathrm{H}_{error}(s)\, H_{VCO}(s)\, \boldsymbol{L}(s) \tag{IV-28}$$

If all modules, including the controllers, are identical, the MIMO open-loop transfer function noted $\boldsymbol{oL}(s)$ and shown in Eq. (IV-29).

$$\boldsymbol{oL}(s) = \frac{\boldsymbol{\Theta}(s)}{\boldsymbol{\Theta}'(s)} = -\mathrm{H}_{error}(s)\, C(s)\, H_{VCO}(s)\, \boldsymbol{L}(s) \tag{IV-29}$$

## IV.5. Change of basis and modal transfer functions

All matrix transfer functions are diagonal and circulant, except $\boldsymbol{L}(s)$, that is only circulant. To obtain the modal open-loop transfer function, $\boldsymbol{L}(s)$ has to be diagonalized using the DFT matrix. The same DFT matrix as the one shown in Section II.2.1 will be used. A change of basis expressed by the set of equations developed in Eq. (IV-30) is applied to the system.

$$\boldsymbol{\Theta}^*(s) = \boldsymbol{W}^*\, \boldsymbol{\Theta}(s) \qquad\qquad \boldsymbol{\Theta}'^*(s) = \boldsymbol{W}^*\, \boldsymbol{\Theta}'(s) \tag{IV-30}$$

Then, the diagonal formulation of Eq. (IV-29) can be written. Its expression is detailed in Eq. (IV-31).

$$\boldsymbol{oL}^*(s) = \frac{\boldsymbol{\Theta}^*(s)}{\boldsymbol{\Theta}'^*(s)} = -\mathrm{H}_{error}(s)\, C(s)\, H_{VCO}(s)\, \boldsymbol{L}^*(s) \tag{IV-31}$$

where $$\boldsymbol{L}^*(s) = \boldsymbol{W}\ \boldsymbol{L}(s)\ \boldsymbol{W}^*$$

Eq. (IV-31) can be rewritten as a system of $N$ independent transfer functions in Eq. (IV-32) because $\boldsymbol{oL}^*(s)$ is diagonal. The $N$ diagonal elements ${V^*}_{ii}(s)$ of $\boldsymbol{L}^*(s)$ are named ${L^*}_i(s)$, for $i = 0 \ldots N-1$, and the same for $\boldsymbol{oL}^*(s)$ with diagonal elements renamed ${oL^*}_i(s)$.

$$oL^*{}_i(s) = \frac{\Theta^*{}_i(s)}{\Theta'^*{}_i(s)} = -\mathrm{H}_{error}(s)\ C(s)\ H_{VCO}(s)\ L^*{}_i(s) \qquad \text{(IV-32)}$$

where:
$$L^*{}_i(s) = \cos(2\pi\ i/N - j\ s\ T_0) - 1, \qquad i = 0 \ldots N-1$$
$j$ is the complex variable $\sqrt{-1}$

Comparing the eigenvalues of $\boldsymbol{L}$ with the eigenvalues of $\boldsymbol{L}(s)$, an additional term $-j\ s\ T_0$ appears in the cosine. It should be noted that ${L^*}_{N-i}(s) = {L^*}_i(s)^*$ in all double modes, for $i = 1 \ldots M-1$, $M$ is defined in Eq. (II-15), but ${L^*}_i(s)^* \neq {L^*}_i(-s)$, i.e. the conjugated of ${L^*}_i(s)$ is different of ${L^*}_i(-s)$, revealing that this is not a classical control system. ${L^*}_i(s)$ values are real, but it has a non-null complex component.

It should be noted that ${L^*}_i(s)$ can be split in a real and a complex components as shown in Eq. (IV-33). Indeed, classical control system have null complex component. The diagonal components of $\boldsymbol{L}(s)$ are complex-coefficient systems as shown in [36].

$$L^*{}_i(s) = {L^*}_{i_{Re}}(s) + j\ {L^*}_{i_{Im}}(s), \qquad i = 0 \ldots N-1 \qquad \text{(IV-33)}$$

where
$$L^*{}_{i_{Re}}(s) = \cos(2\pi\ i/N)\cos(j\ s\ T_0) - 1$$
$$L^*{}_{i_{Im}}(s) = -j\sin(2\pi\ i/N)\sin(j\ s\ T_0)$$

The values of $|L^*{}_i(s)|$, for $i = 0 \ldots M-1$, are plotted in Figure IV-12 (a), showing the values for positive and negative frequencies. Figure IV-12 (b) show the real and complex decomposition of $|L^*{}_i(s)|$.

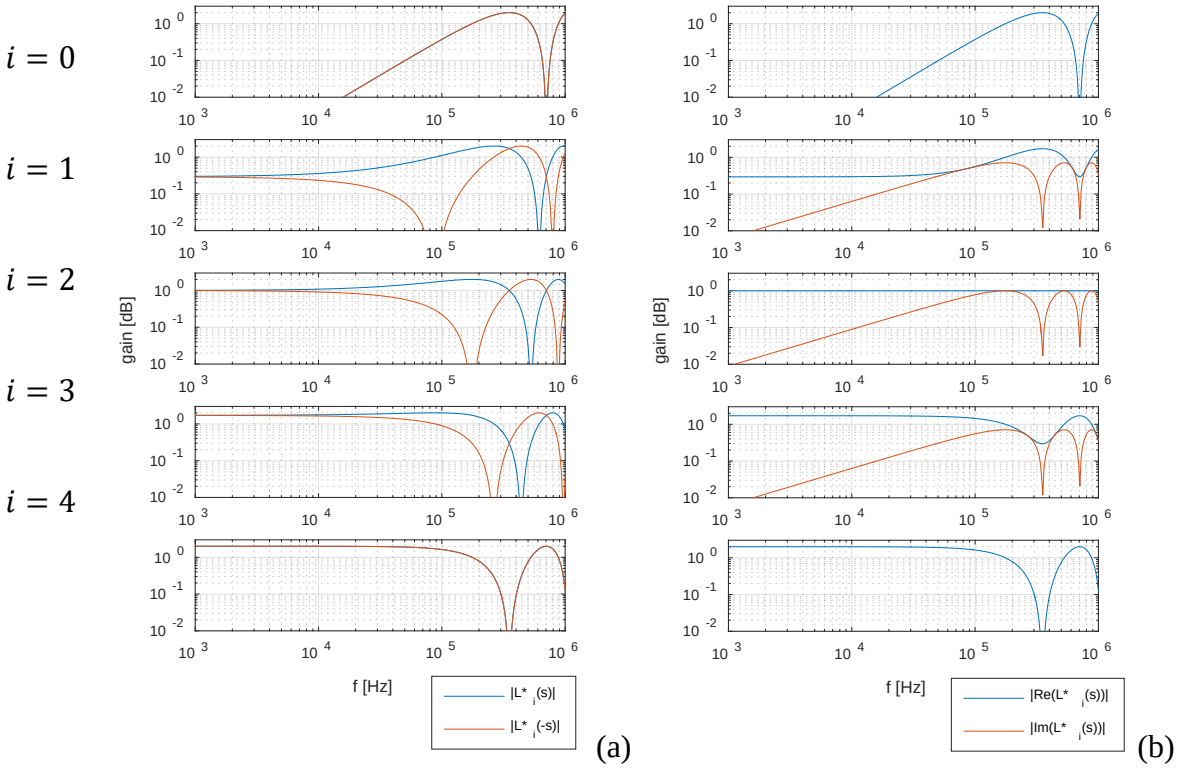



*Figure IV-12 – $L^*_i(s)$ Transfer function: a) Positive and negative frequencies, b) Real and imaginary components.*

It should be noted that $L^*_i(j0) = \lambda_i$. Additionally, it can be noted for $i = 4$ (higher gain) that $L^*_i(s) \cong \lambda_i$ are similar until the expected cutoff frequency $\pm$7.85 kHz. For the other $i = 1, 2, 3$, the components of $|L^*_i(s)|$ become different of $|L^*_i(-s)|$for at lower frequencies. However, these modes have smaller gains and will have smaller bandwidth. As a result, these differences will not be perceived within the mode bandwidth. For $i = 0$, the mode is not controllable because the gain is very low.

As a conclusion, the system is quite complex. The standard matrix $\boldsymbol{L}$ could be a good approximation of $\boldsymbol{L}(s)$ to simplify the model and help to design the corrector. If the model is simplified replacing $\boldsymbol{L}(s)$ by $\boldsymbol{L}$, $\boldsymbol{L}^*(s)$ becomes $\boldsymbol{\Lambda}$ developed in Eq. (II-17) and each mode gets a different gain equal to $\lambda_i$, i.e. the eigenvalues of $\boldsymbol{L}$ detailed in Eq. (II-16).

## IV.6. **Stability concern**

To reveal the stability concern, the static error constraint must analyzed before the corrector synthesis.

### IV.6.1. Static gain constraint

An integrator can be added to the controller $C(s)$ to cancel the error brought by the disturbance input $\boldsymbol{D}(s)$. However, common mode deviation in the noise input $\boldsymbol{N}(s)$ would saturate the VCO control voltage $u$. The common mode cannot be controlled because $L^*_0(s)$ is

comparable to zero. This last point can become a real issue because it can generate frequency deviations an break the loop.

In order to design the controller static gain to attenuate $\boldsymbol{D}(s)$, the relationship between the disturbance $\boldsymbol{D}(s)$ and the local error $\boldsymbol{E_\Theta}(s)$ has to be revealed. To do so, the signals $\boldsymbol{E_\Theta}(s)$ and $\boldsymbol{D}(s)$ are diagonalized, as shown in Eq. (IV-34).

$$\boldsymbol{E_\Theta}^*(s) = \boldsymbol{W^{-1}}\,\boldsymbol{E_\Theta}(s) \qquad\qquad \boldsymbol{D}^*(s) = \boldsymbol{W^{-1}}\,\boldsymbol{D}(s) \tag{IV-34}$$

The diagonal transfer functions from $\boldsymbol{D}^*(s)$ to $\boldsymbol{E_\Theta}^*(s)$ is shown in Eq. (IV-35), where differential mode transfer functions are also shown, within the modal bandwidth, i.e. $|oL^*{}_i(s)| > 1$.

$$\frac{\boldsymbol{E_\Theta}^*(s)}{\boldsymbol{D}^*(s)} = \frac{T_0/k_d}{\mathrm{H}_{error}(s)\,C(s)}\left(\boldsymbol{I} - \boldsymbol{oL}^*(s)\right)^{-1}\boldsymbol{oL}^*(s)\,, \qquad |oL^*{}_i(s)| > 1 \implies$$
$$\frac{E_\Theta{}^*{}_i(s)}{D^*{}_i(s)} = \frac{T_0/k_d}{\mathrm{H}_{error}(s)\,C(s)}, \quad i = 1 \ldots N-1 \tag{IV-35}$$

It can be noted that $C(s)$ can reduce the differential mode disturbances $D^*{}_i(s)$. In steady-state, the differential mode errors are reduced by a factor $C(j0)$, so the interest of having $|C(j0)| \to \infty$, i.e. having at least an integrator in $C(s)$. As a conclusion, a controller with a high static gain is good to reduce the differential modes.

Nevertheless, a high static gain can cause side effects related to the common mode. To understand the issue, the signal $\boldsymbol{u}(t)$ common mode final value $\boldsymbol{u}_{0\,SS}$ has to be revealed. To do so, the signals $\boldsymbol{U}(s)$ is diagonalized as $\boldsymbol{D}(s)$ and $\boldsymbol{N}(s)$, as shown in Eq. (IV-36).

$$\boldsymbol{U}^*(s) = \boldsymbol{W^{-1}}\,\boldsymbol{U}(s) \tag{IV-36}$$

The diagonal transfer functions from $\boldsymbol{N}^*(s)$ to $\boldsymbol{U}^*(s)$ is shown in Eq. (IV-37). As the common mode open-loop transfer function $|oL^*{}_0(s)| \ll 1$ because $L^*{}_0(s) \cong 0$, the related common mode transfer function can be easily found, as shown in this equation.

$$\frac{\boldsymbol{U}^*(s)}{\boldsymbol{N}^*(s)} = \left(\boldsymbol{I} - \boldsymbol{oL}^*(s)\right)^{-1} C(s) \qquad \frac{U^*{}_0(s)}{N^*{}_0(s)} = \frac{C(s)}{1 - oL^*{}_0(s)} = C(s) \tag{IV-37}$$

$D^*{}_0(s)$ is null by definition. Indeed, as $f_0$ is the average of all local free-running frequencies, the sum of $d_i = \delta f_i/k_d$ is null. So, the final value of $u^*{}_0(t)$, noted $u^*{}_{0\,SS}$, shown in Eq. (IV-38), is obtained by applying the final value theorem to Eq. (IV-37).

$$u^*{}_{0\,SS} = \lim_{t\to\infty} u^*{}_0(t) = U^*{}_0(0) = |C(0)|\,N^*{}_0(0) \tag{IV-38}$$

It is assumed that $|N^*{}_0(j0)|$ has a limited value. $u^*{}_{0\,SS}$ is also limited if $|C(j0)|$ is limited as well, otherwise the signal $u$ would saturate in some of the local controllers and

produce infinite value due to the controller integrator. A saturated local controller modify the transient response because it acts like if the loop was opened. As a consequence, $C(s)$ cannot implement an integrator, then $|C(j0)| < \infty$.

The component $u^*_{0\,SS}$ causes a second side effect, it causes a deviation of the average frequency $\Delta f_0$ in steady-state, noted $\Delta f_{0\,SS}$. Its expression is shown in Eq. (IV-39).

$$\Delta f_{0\,SS} = \frac{k_d}{\sqrt{N}}\, u^*_{0\,SS} \qquad |\Delta f_{0\,SS}| = k_d\, \Delta u_{sat} \tag{IV-39}$$

where $\Delta u_{sat}$ is the maximum $u$ deviation from its neutral value.

So, to limit the frequency deviation in a small range, $|C(j0)|$ has to be limited and $|N^*_0(0)|$ has to be as low as possible. A clear trade-off on $|C(j0)|$ value has to be considered, impacting both the modal steady-state error and the frequency deviation.

### IV.6.2. Corrector synthesis

As seen in the previous chapter, some trade-off have to be made because the modes present different gains, related to their eigenvalues, but all of them use the same corrector. The corrector is synthetized to provide the largest bandwidth with minimum phase margin of 55° combined with a phase-lag to increase the static gain. The matrix $\boldsymbol{V}(s)$ is simplified and replaced by $\boldsymbol{L}$.

In the use case considered here with $N = 8$, the differential Mode 4 has the higher eigenvalue equals to 2, so the controller proportional gain must to be 0.50 to keep the same cut-off frequency. A zero is added to the controller to increase the static gain. The zero frequency is placed at 145 Hz, at least 8 times smaller than the cut-off frequency of Mode 1 to keep enough phase margin. The controller static gain then limited to is 100, what reduces the proportional gain to 0.48. The controller transfer function is shown in Eq. (IV-40). All results shown here after are using this controller.

$$C(s) = \frac{1.10m\ s + 1}{2.31m\ s + 0.01} \tag{IV-40}$$

Figure IV-13 shows the bode diagrams of the modal OLTF shown in Eq. ((IV-32)) for $N = 8$ $(M = 5)$, $C(s) = 0.5$ and $\boldsymbol{L}(s) = \boldsymbol{L}$, then $L^*_i(s) = \lambda_i$. As $\lambda_i = \lambda_{N-i}$, only the values with $i = 0 \ldots M - 1$ are shown. Moreover, the common mode (mode 0) cannot be controlled because $\lambda_0 = 0$, so only the differential modes are studied, then $i = 1 \ldots M - 1$.

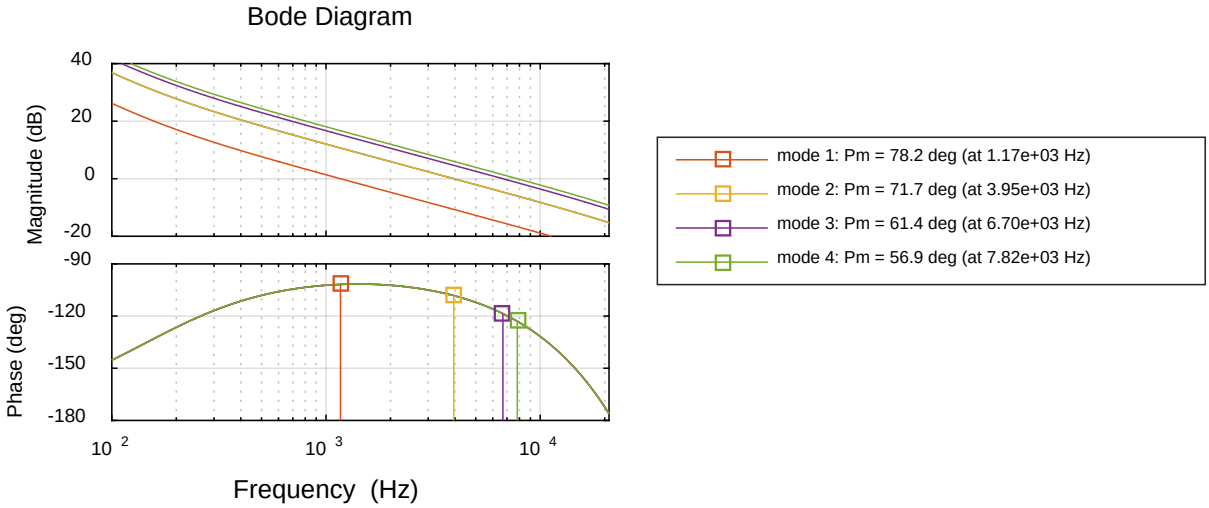



*Figure IV-13 – Modal open-loop transfer function plot for $N = 8$ $(M = 5)$ and $\boldsymbol{L}(s) = \boldsymbol{L}$.*

A disturbance rejection simulation is made with each of the modal transfer functions as shown in Figure IV-14. This simulation result is similar to the expected responses of the components of $|\boldsymbol{\varepsilon_\theta}^*|$.

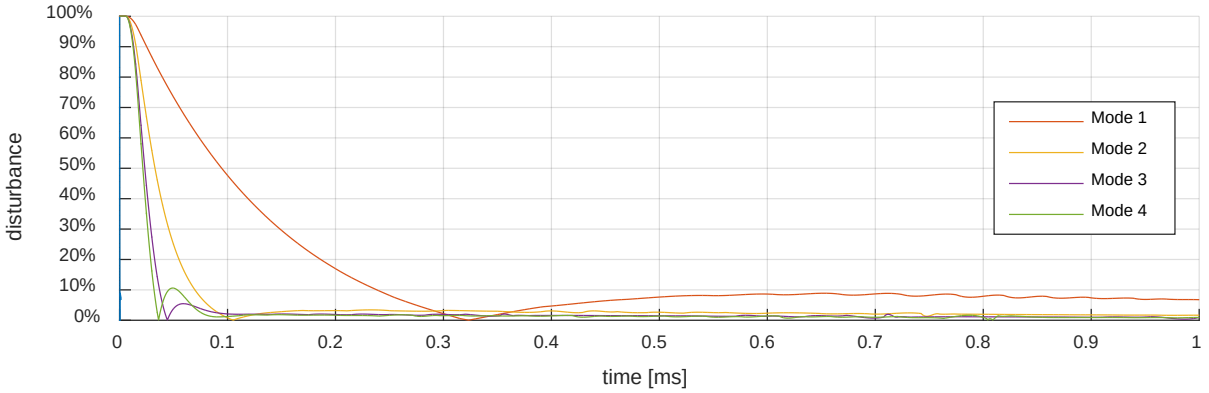



*Figure IV-14 – Modal closed-loop disturbance rejection simulation for $N = 8$ $(M = 5)$ and $\boldsymbol{L}(s) = \boldsymbol{L}$.*

The rise time $T_{rise}$ for these underdamped system is defined as the time from 0% to 100%. The rise time, overshoot and overshoot time $T_{OV}$ are obtained from the model simulation shown in Figure IV-14. Table IV-2 summarizes the modal performances obtained in this study: $N = 8$ $(M = 5)$ and $\boldsymbol{L}(s) = \boldsymbol{L}$.

*Table IV-2 – Modal performances obtained with the model in the case study.*

| Mode i | Cut-off freq $f_{c_i}$ | Phase Margin | $T_{rise}$ | $k_{i\_5\%}$ | Overshoot | $T_{OV}$ |
|---|---|---|---|---|---|---|
| 1 | 1.17 kHz | 78.2° | 323 us | 28.4 | 8.87 % | 652 us |
| 2 | 3.95 kHz | 71.7° | 105 us | 9.24 | 3.38 % | 232 us |
| 3 | 6.70 kHz | 61.4° | 44.3 us | 3.90 | 5.41 % | 59.1 us |
| 4 | 7.82 kHz | 56.9° | 36.1 us | 3.18 | 10.5 % | 49.2 us |

It can be noted that all modes' phase margins are greater than 55°, i.e. within the specifications. Also, the modes' rise times are different as expected, because they all depend on their associated cutoff frequency.

It can be noted that mode 1 has an important overshoot when compared to the expected value from its phase margin. This is because the phase-lag open-loop zero is close to the mode 1 cut-off frequency and disturbs its closed-loop response, similarly to a proportional-integral controller. The zero effect can be removed with a phase-lag controller based on an integral-proportional equivalent topology.

These rise time responses are valid only when all modules are located in between their local neighbors. The response is slowed down if some LCs are not in between their neighbors because the perceived errors reach limited values (saturation). In that case, the stability criterion will not be analyzed because the number of cases to considered will be very high and the non-linear system to be analyzed will become very complex.

### IV.6.3. Diagonal response

The dynamic behavior of the overall system has been simulated and the observed settling times compared with the ones predicted. A MIMO transfer function based model is defined and simulated using MathWorks MATLAB®. In the simulations performed hereafter, the system starts from its expected equilibrium state with all the carriers well interleaved. Each mode is excited individually, one after the other, from the common mode (mode 0) to the last one (mode 4) using the system eigenvectors (lines of the DFT matrix) as components of the disturbance signal $\boldsymbol{d}$.

Figure IV-15 shows the simulation results of a system with eight LCs ($N = 8$) and the controller previously designed. Each simulation result consists of the applied modal disturbance $\boldsymbol{d}^* = |\boldsymbol{W}^{-1}\boldsymbol{d}|$, the waveforms of the PDs $\boldsymbol{\theta}$, the local errors $\boldsymbol{\varepsilon_\theta}$ and the modal error decompositions $|\boldsymbol{\varepsilon_\theta}^*|$ to observe the total mode disturbances. For simulation purposes, the target operator introduced in the previous chapter for the digital case is required.

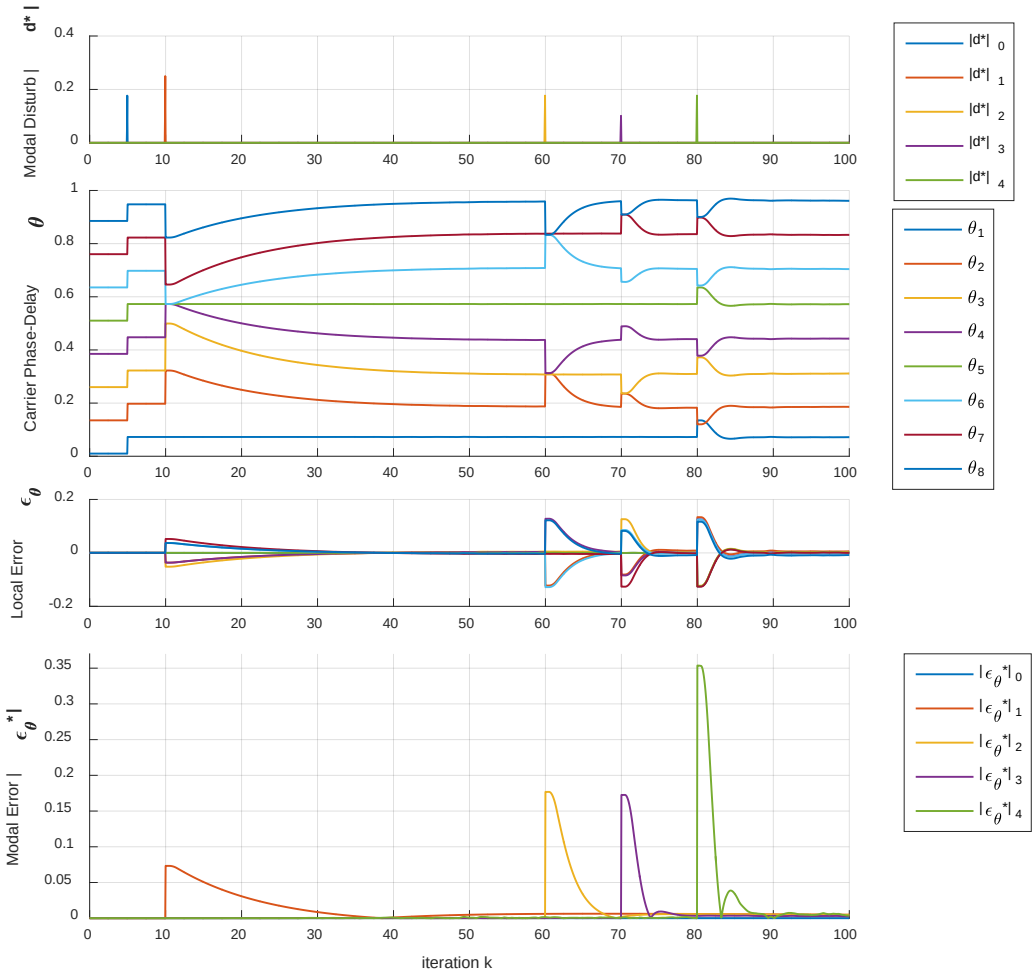



*Figure IV-15 – Dynamic modal responses with N = 8 and controller $C(s)$ of Figure IV-13.*

The PD values behave as expected. It is possible to distinctly observe the modal excitations being applied successively and their respective responses. All modes are stable and $k_{i\_5\%}$ observed on $|\boldsymbol{\varepsilon_\theta}^*|$ corresponds to the simulated values from the modal transfer functions shown in Table IV-2.

## IV.7. **Fault hazards impact**

Considering the implementation of the real system in an integrated circuit, the devices or wire links are always exposed to fault issues, such as short-circuits or disconnections (open-circuits). Most of the faults can be placed in two categories: short to ground and short to adjacent pin. The short to ground is a generic fault because causes a level freeze. The level freeze happens due a short to any level or pin disconnection, because most of the inputs have internal pull-up or pull-down.

When an inter-LC communication wire is stuck to a constant level, its input comparator with hysteresis will be provide a constant logical level. As a result, when comparing the constant input with the local clock, the UP or DN signal will have 50% duty cycle. The 50%

duty cycle is equivalent to a detection of ±180° with its neighbor. It is equivalent to introducing an additional factor ±0.25 in the $\boldsymbol{\varphi}$ vector. The correctors will slowly saturate and cause consequently frequency deviation. During the time between the fault and the saturation, the PD will be in PD an unequal distribution because the others LCs will try to compensate an error that cannot be eliminated. After the saturation, the PD will be properly interleaved, but with a frequency deviation.

Let consider now a system with $N$ LCs in which the communication input of one LC is stuck to a constant level so that the LC detects a PD equal to –0.5. The resulting wrong error is approximately equal to –0.25. The other LCs compensate equally this interleaving issue, each local error been approximately equal to $0.25/N$. The PD steady-state values can be derived from Eq. (II-8) and solved with the Final Value Theorem on Eq. (II-47), and the result expressed in Eq. (IV-41).

$$\boldsymbol{\theta} = mod\big(\boldsymbol{L}^{+}(\boldsymbol{\varepsilon}_{\theta} - \boldsymbol{\varphi})\big) = mod\big(\boldsymbol{L}^{+}(0.25/N\,\boldsymbol{I} - \boldsymbol{\varphi})\big) \qquad \text{(IV-41)}$$

where $\mathbf{1} = [1]_{1\times N}$, $\boldsymbol{L}^{+}$ is the pseudo-inverse of $\boldsymbol{L}$, and $mod(\cdot)$ is the module operator to correct the common-mode, i.e. keep the PDs between 0 and 1.

The level freeze fault can be easily detected by analyzing the UP/DN signals or verifying directly the clk signals received from the neighbors, i.e. verify if a rising and a falling edge are detected in each period.

When a short-circuit occurs on adjacent communication wires, considering a AND operation by wire is obtained, both LC perceive the same rising and falling edges on its inputs. It should be noted that one LC notes its own rising edges while the other notes its own falling edges. As only one of the edges is used for the PD measurement, one of the LC controllers perceives its neighbor as coincident because detects its own edge, while the other LCs can detect properly the PD because it can detect the neighbor edge. This will cause some frequency deviation, and the impact on the interleaving error will be small because the PD error detected will be only equal to $0.5/N$. Because the sum of the errors has to be cancelled, the others LC errors, due to the compensations, would be approximately $0.5/N^2$.

## IV.8. **Proof-of-concept development**

This section is dedicated to the development of the new interleaving proof-of-concept for model validation. The data obtained will be analyzed and the comparisons with the proposed model predictions will be verified.

The proof-of-concept is an electronic board where the interleaving LCs are implemented with basic functions, such as NAND gates, flip-flops, switches, comparators and operational amplifiers, in addition to resistors, capacitors and diodes. All these functions are of the type of commercial discrete Surface Mount Devices (SMD).

The board shown in Figure IV-16 is composed by 6 identical carrier generators, each of them with a LCs and a bypass circuit. Additionally, shared functions are placed aside, composed of a start-up synchronization circuit (reset), a slope generator for phase-delay sampling and a fault introduction circuit composed by inter-connection analog switches.

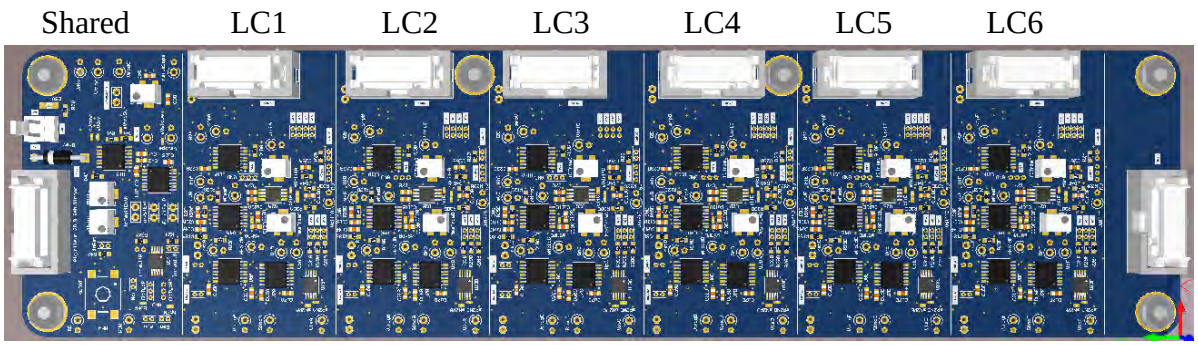



*Figure IV-16 – Proof-of -concept board with 6 LCs and shared functions.*

Each LC has two inputs, noted “CssP” and “CssN”, to receive the previous and next LC signals. Each LC has also two outputs, noted “Css2P” and “Css2N”, to send signals to the previous and next LCs. The nature of the signal sent to the neighbors depends if the LC is bypassed or not, i.e. deactivated or activated.

The LCs on the board are connected to their close neighbors. “Css2N” of the $i^{th}$ LC is connected to “CssP” of the $i + 1^{th}$ LC and “Css2P” of the $i + 1^{th}$ LC is connected to “CssN” of the $i^{th}$ LC. The circular chain of communications has to be closed with a cable using the connectors placed at the upper left and right sides of the board, connecting the LC6 to LC1. Multiple boards can be connected together, connecting LC6 to LC7 and LC12 to LC1, where LC7 to LC12 are the LCs of the second board for instance.

### IV.8.1. Triangular carrier generator and pre-positioning

The triangular carrier generator circuit is shown in Figure IV-17. It consists of a Schmitt trigger made up of a comparator with hysteresis (1) and an operational amplifier in an integrator configuration (2). The comparator output called “Vtrig” is equivalent to the clock signal “clk”. The operational amplifier output is the triangular carrier called “Vtri”.

To analyze the modal response, “Vtri” signal has to be set to a predefined value at the begging. The additional circuits required to pre-position the signal “Vtri” are also shown in

Figure IV-17. The comparator (1) initial position is controlled at its non-inversing input with an analog switch “s0”. The operational amplifier (2) output voltage is set to a predefined value thanks to the switch “s2” and the feedback resistors using the jumpers “Go” (open-loop gain) and “Gx” (gain x), where x is equals to 1, 2 and 4. The switch “s1” is added to force the operational amplifier polarity and to avoid the output voltage dependence with the comparator output. So the voltages “V0” (initial voltage) and “V0ax” (auxiliary initial voltage) determine in which quadrant the phase-delay starts. An additional comparator generates the digital signal “Sync” (Sinc) aligned with the triangular signal peak used for SMP and RST synchronization.

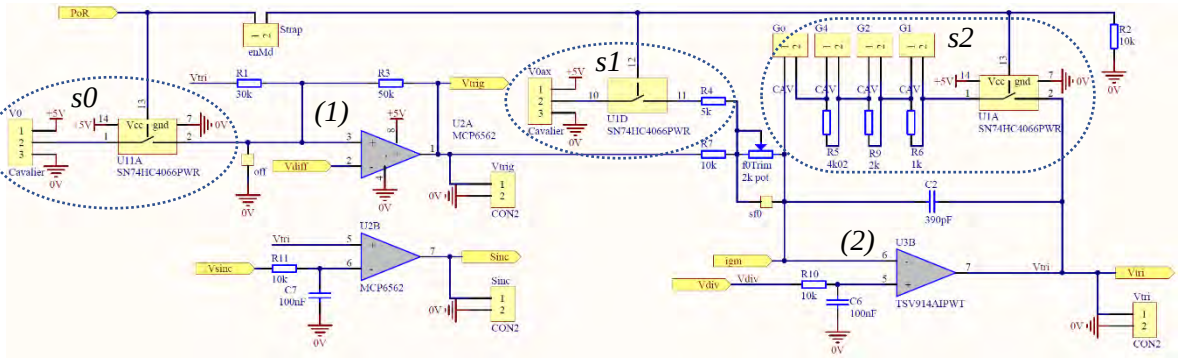



*Figure IV-17 – Triangular carrier generator and its additional circuits required for “Vtri” pre-prepositioning.*

Figure IV-18 shows the 24 combinations of “V0”, “V0ax” and “Gx” (Go always closed), required to pre-position “Vtri” phase-delays within 15° steps.

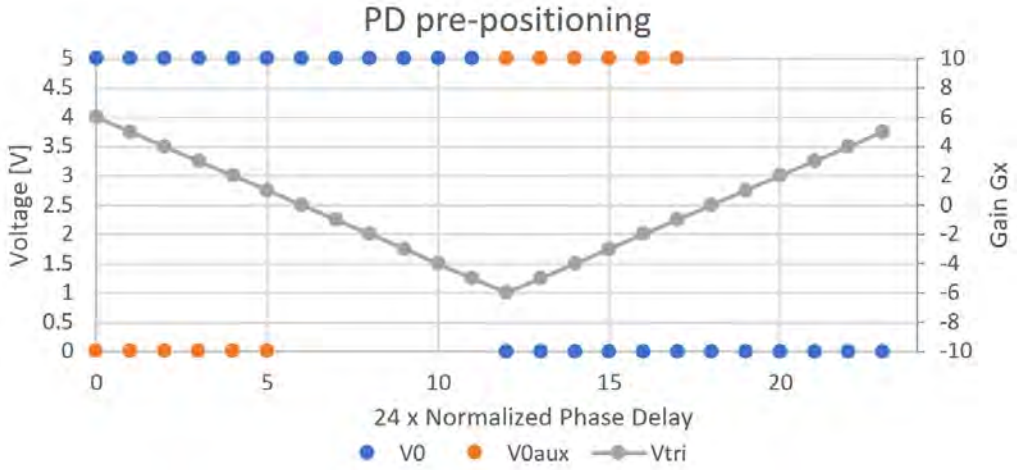



*Figure IV-18 – 24 combinations of “V0”, “V0ax” and “Gx” to pre-position “Vtri” phase-delays.*

### IV.8.2. New interleaving local controllers

Table IV-3 shows the initial position chosen based on the initial modal error required.

*Table IV-3 – Modal initial position and modal error.*

| | Local controller pre-positioning | | | | | | | | Initial modal error | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LC1 | LC2 | LC3 | LC4 | LC5 | LC6 | LC7 | LC8 | $\lvert\varepsilon_\theta{}^*\rvert_1$ | $\lvert\varepsilon_\theta{}^*\rvert_2$ | $\lvert\varepsilon_\theta{}^*\rvert_3$ | $\lvert\varepsilon_\theta{}^*\rvert_4$ |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mode 1 | 0 | 18 | 14 | 12 | 12 | 12 | 10 | 6 | 0.071 | 0.000 | 0.012 | 0.000 |
| Mode 2 | 0 | 18 | 18 | 18 | 12 | 6 | 6 | 6 | 0.000 | 0.177 | 0.000 | 0.000 |
| Mode 3 | 0 | 22 | 16 | 16 | 12 | 8 | 8 | 2 | 0.005 | 0.000 | 0.172 | 0.000 |
| Mode 4 | 0 | 18 | 18 | 12 | 12 | 6 | 6 | 0 | 0.000 | 0.000 | 0.000 | 0.354 |

The new interleaving local controller is composed of a digital and an analog core.

The digital core, shown in Figure IV-19 manages the start-up synchronization, generate the sample-and-hold control signals, and the “Up” and “Down” (UP/DN) signals that represents the phase-delay. The neighbors clock signals are applied on “VtrigP” and “VtrigN”, while the local clock is applied on “Vtrtr”. To avoid measurement errors, the D flip-flop at the left enables the measurement and corrections at start-up with the beginning of the carrier period, while the other on the right synchronizes the by-pass with the carrier period.

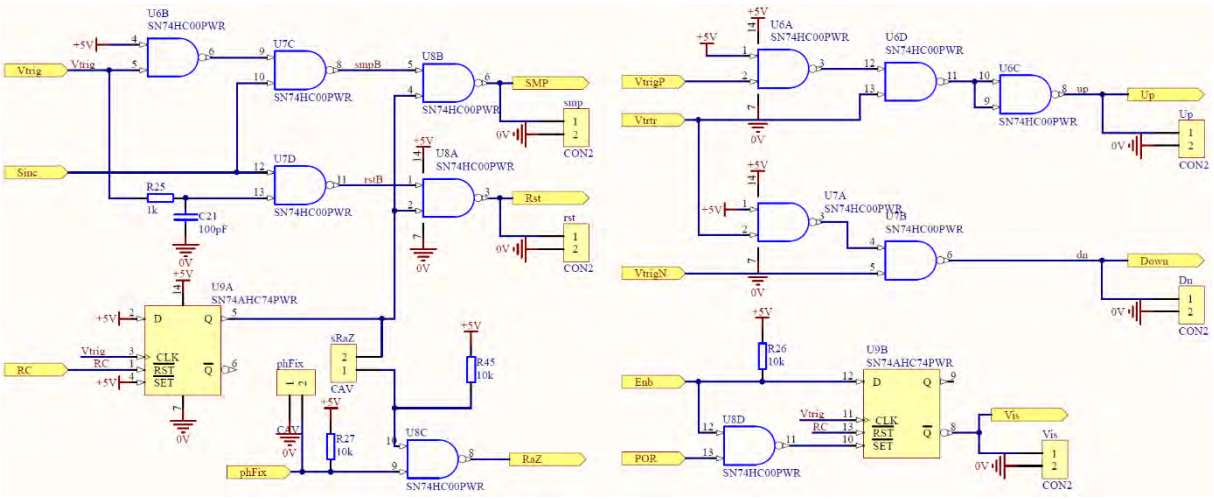



*Figure IV-19 – New interleaving digital core.*

The analog core shown in Figure IV-20 is composed, from left to right, of an integrator with reset, a sampling circuit, a voltage follower, a proportional corrector with phase-lag, and an amplifier to manipulate the triangular carrier generator frequency. The last amplifier injects a current proportional to the correction “eV” at the inverting input of the amplifier (2) shown in Figure IV-17.

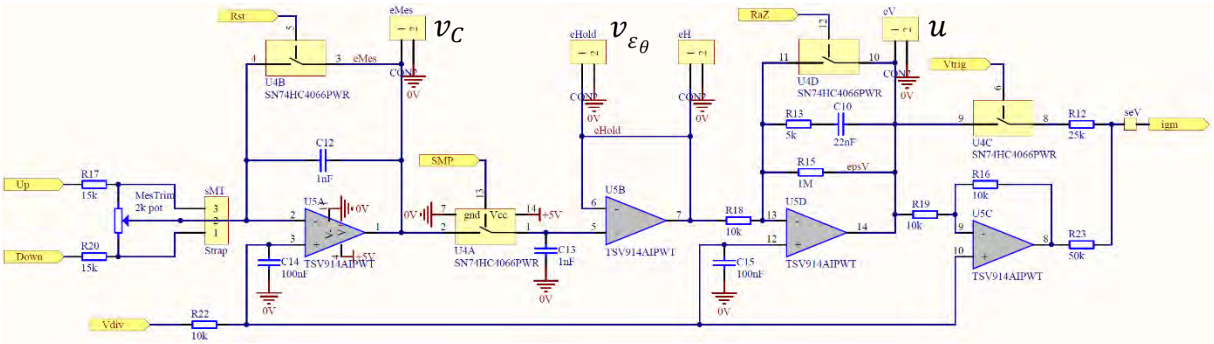



*Figure IV-20 – New interleaving analog core.*

The measure can be trimmed using “MesTrim” trimmer potentiometer to avoid static error.

### IV.8.3. Fault introduction

The fault introduction module is located upstream LC1, i.e. between the LC1 and the circular-chain connector.

Three fault types can be applied individually or simultaneously (with separated control) on the lines “CssP” of LC1 and “CssN” of LC connected to LC1 though the cable. The faults are: open (disconnection), short-circuit to 5V and short-circuit to GND.

Additionally, a short-circuit fault can also be introduced to connect “CssN” to “CssP” though an impedance.

## IV.9. Experimental validation

The experimental validation will be done using two proof-of-concept boars, a Teledyne LeCroy WaveRunner 8108HD 12-bit oscilloscope with 8 analog and 16 digital channels, a Keysight Tektronix 5 SERIES MSO58 8 analog channels mixed signal oscilloscope. The boards are powered with an external 5V DC power supply. A Keysight Tektronix MDO3014 4 channels oscilloscope was used for debug purposes. The experimental validation bench is shown in Figure IV-21.

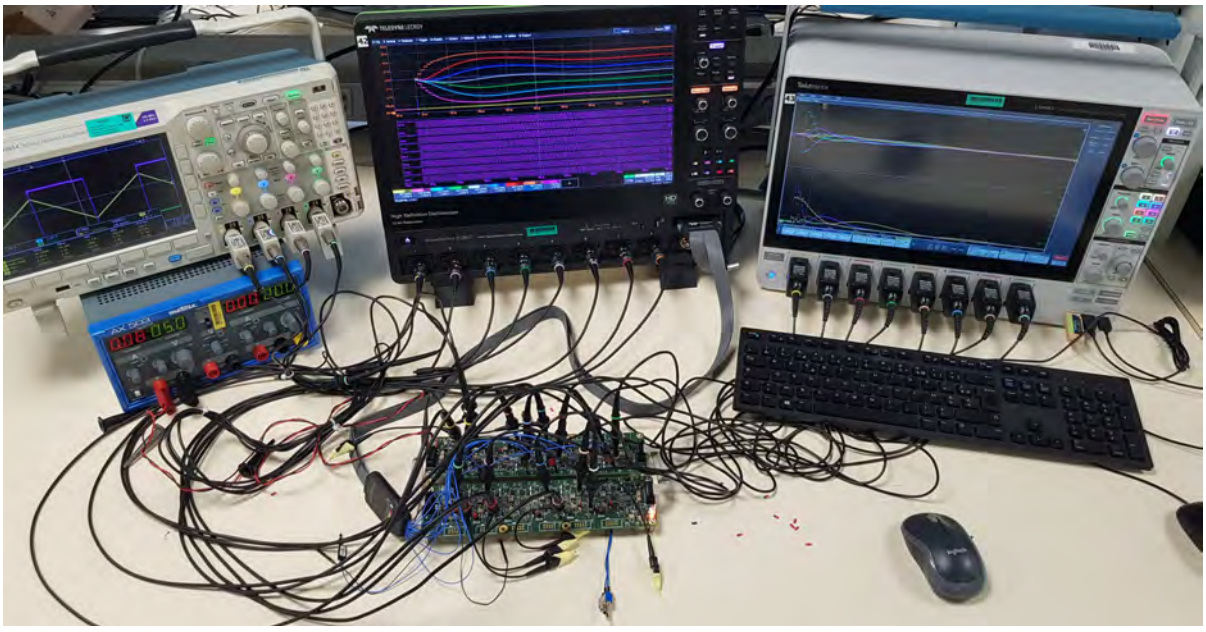


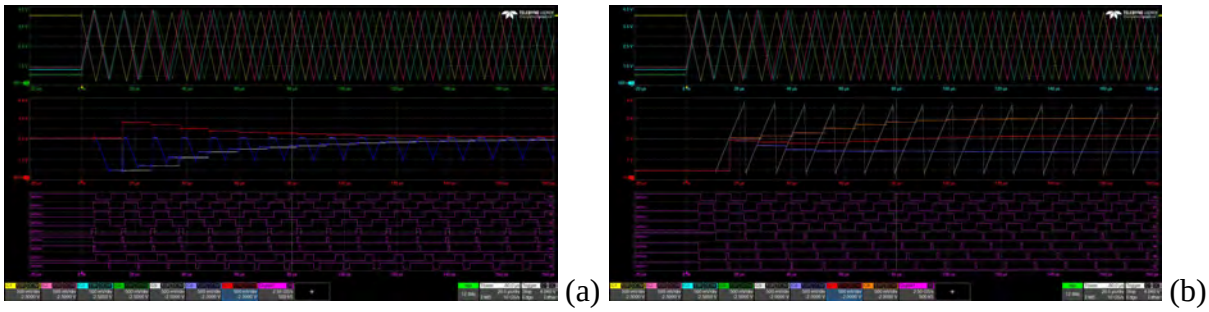
*Figure IV-21 – Experimental validation bench, LeCroy oscilloscope in the middle and Tektronix oscilloscope on the right.*

The 8 analog channels of the LeCroy oscilloscope are used to observe the sampled PDs (top) and the digital channels are used to monitor the oscillators clock signals clk (bottom). The

8 analog channels of the Tektronix oscilloscope are used to observe the LC errors (top), then 4 the math channels are programmed to show the modal content of the measured errors (bottom).

### IV.9.1. Local controller validation

The local controller validation starts with the observation of the different signals in order to be sure that all digital and analog control signals are functional and if the local controllers are able to interleave the carriers. Figure IV-22 shows in (a) and (b) the start-up response with 4 local controllers in 1+3 configuration.



(a) (b)

*Figure IV-22 – Local controller validation: a) LC2 signals detail; b) sampled PDs detail.*

In Figure IV-22 (a) are shown on the trop the 4 triangular signals of the 4 LCs from 1 to 4, in yellow, red, blue and green, respectively. In the middle are shown the LC2 measured error $v_c$ (white), the sampled error $v_{\varepsilon_\theta}$ (blue) and the correction $u$ (red). The digital signals from 0 to3 are the LC clk1 to clk4 respectively. The other digital signals from 4 to 8 are the sync, SMP, RST, UP and (not) DN signals of LD2.

In Figure IV-22 (b) shows in the middle a ramp representing the PD relative to LC1 (white). The ramp is sampled by the other LCs, resulting in the waveforms in blue, red and orange for LCs 2 to 4, respectively. The sampled values are proportional to the PDs regarding LC1 (reference). Digital signals 4 to 8 are the LC1 to LC4 SMP signals. LC1 SMP signal is used to reset the ramp signal, while LC2 to LC4 SMP signals used to sample and hold the ramp signal. The other signals are the same.

All LC validation were successful, additionally, the triangular carrier generators and the local controllers were trimmed. The triangular signals peak-to-peak value is superior than the 3.0 V designed because of the comparator delay. Then, the average open-loop frequency was set to 88 kHz instead of 100 kHz original value.

### IV.9.2. Diagonal response validation

The diagonal/modal responses were be validated using the carrier pre-positioning shown in Figure IV-23. Due to the larger triangle signal amplitude and frequency trim (reduces the pre-positioning gain), an additional 0.5 step was added and the whole gain range (7.5) was

used, resulting in 60 stat positions. Some rotation were also needed to obtain propre start, mainly because triangle signal overshoot occurrences when initial value was close to the peak.

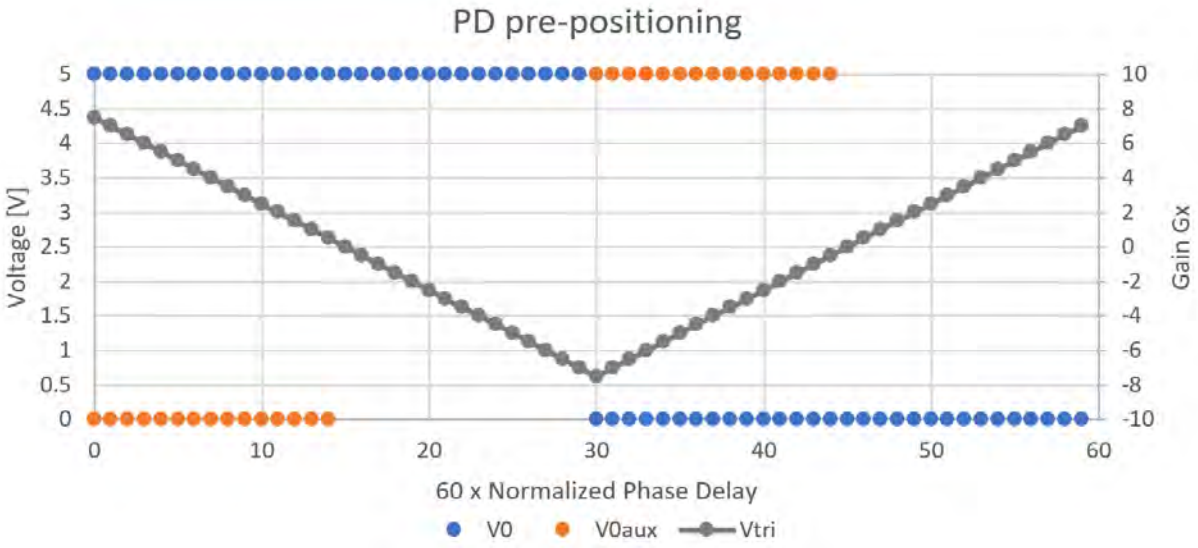


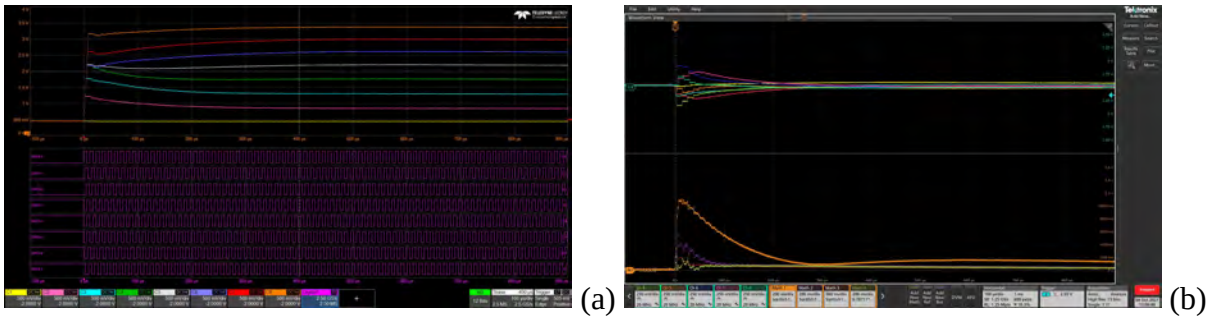

*Figure IV-23 – 60 combinations of "V0", "V0ax" and "Gx" to pre-position "Vtri" phase-delays.*

Table IV-4 shows the adapted experimental positions used during the measurements.

*Table IV-4 – Experimental modal initial position and modal error.*

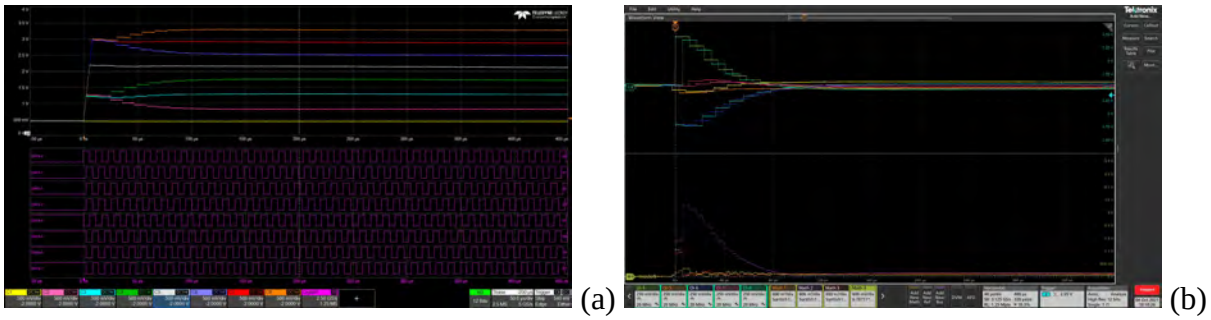
| | Local controller pre-positioning | | | | | | | | Initial modal error | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LC1 | LC2 | LC3 | LC4 | LC5 | LC6 | LC7 | LC8 | $\lvert\varepsilon_\theta{}^*\rvert_1$ | $\lvert\varepsilon_\theta{}^*\rvert_2$ | $\lvert\varepsilon_\theta{}^*\rvert_3$ | $\lvert\varepsilon_\theta{}^*\rvert_4$ |
| Mode 1 | 59 | 44 | 33 | 29 | 29 | 29 | 24 | 14 | 0.074 | 0 | 0.005 | 0 |
| Mode 2 | 53 | 38 | 38 | 38 | 23 | 8 | 8 | 8 | 0.006 | 0.177 | 0.006 | 0 |
| Mode 3 | 59 | 48 | 48 | 33 | 28 | 23 | 8 | 8 | 0.002 | 0 | 0.172 | 0 |
| Mode 4 | 48 | 48 | 33 | 33 | 18 | 18 | 3 | 3 | 0.012 | 0 | 0.012 | 0.354 |

The responses of a system with 8 local controllers are shown in the following Figure IV-24, Figure IV-25, Figure IV-26, and Figure IV-27. The LeCroy scope plots show in the top are the representation of the PDs $\boldsymbol{\theta}$ from $\theta_1$ to $\theta_8$ upwards and the digital signals are the $clks$ from 1 to 8; the Tektronix scope plots show on the top the local errors $\boldsymbol{\varepsilon_\theta}$ and on the bottom the absolute value of the modal local errors $|\boldsymbol{\varepsilon_\theta}^*|$ components 1 to 4. $|\varepsilon_\theta{}^*|_4$ was scaled with a factor $\sqrt{2}/2$.



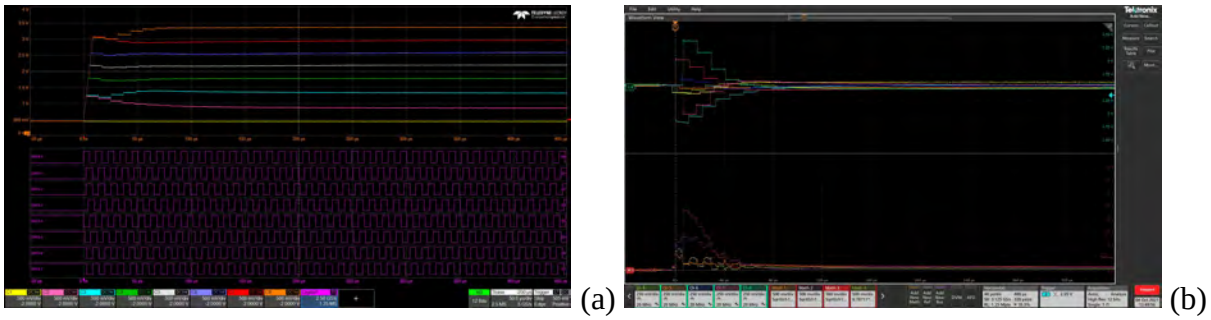
(a) (b)

*Figure IV-24 – Mode 1 diagonal response: a) PDs and clks; b) errors and modal errors.*



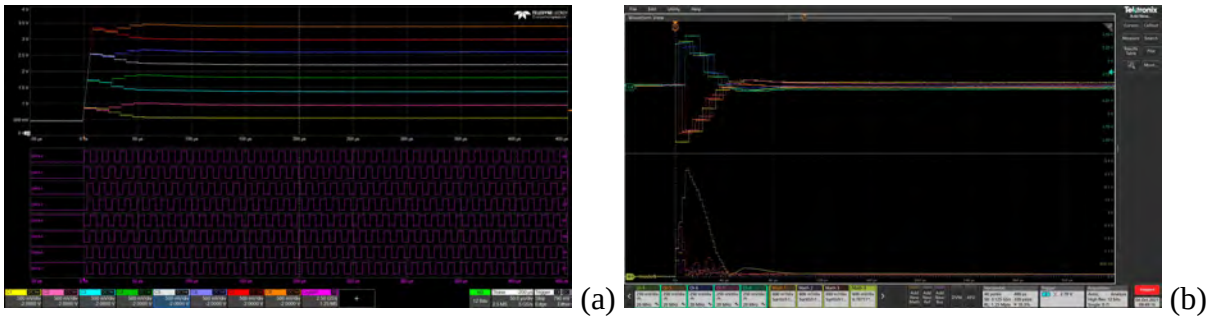
(a) (b)

*Figure IV-25 – Mode 2 diagonal response: a) PDs and clks; b) errors and modal errors.*



(a) (b)

*Figure IV-26 – Mode 3 diagonal response: a) PDs and clks; b) errors and modal errors.*



(a) (b)

*Figure IV-27 – Mode 4 diagonal response: a) PDs and clks; b) errors and modal errors.*

The modal responses are stable and correspond to the expected values obtained with the model. The sampled modal error measurements are summarized on Table IV-5, where:

$T_{rise}$: rise time from initial value to the first minimum;

$V_{T_{rise}}$: voltage at the first minimum;

$V_0$: initial voltage;

$V_{OV}$: overvoltage after first minimum;

$OV_{\%}$: percentual overvoltage calculated as in Eq. (IV-36);

$T_{OV}$: over voltage time.

$$OV_{\%} = \frac{V_{\mathrm{OV}} - V_{T_{rise}}}{V_0 - V_{T_{rise}}} \tag{IV-42}$$

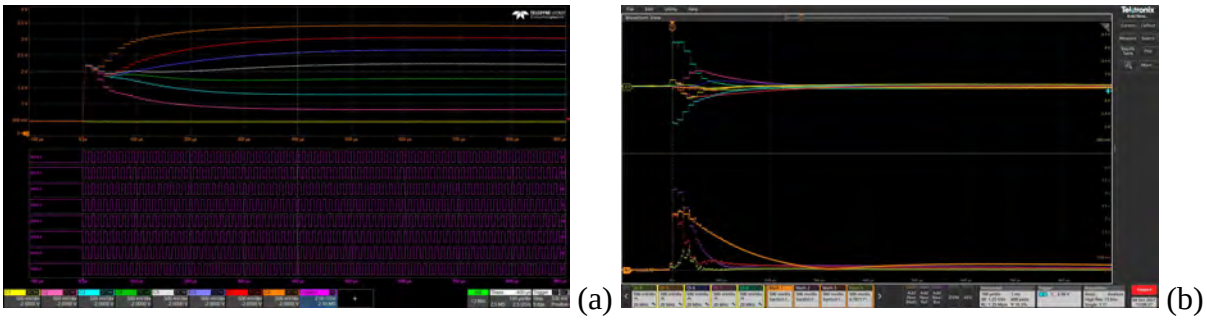
*Table IV-5 – Modal performances measured in the case study.*

| Mode i | $T_{rise}$ | $V_{T_{rise}}$ | $V_0$ | $V_{OV}$ | $OV_{\%}$ | $T_{OV}$ |
|---|---|---|---|---|---|---|
| 1 | 294.8 us | 0.0866 V | 1.08 V | 0.156 V | 6.94 % | 576.3 us |
| 2 | 101.9 us | 0.0185 V | 3.32 V | 0.183 V | 5.00 % | 212.2 us |
| 3 | 49.3 us | 0.115 V | 2.32 V | 0.219 V | 4.70 % | 78.3 us |
| 4 | 44.0 us | 0.0385 V | 4.56 V | 0.407 V | 8.13 % | 57.3 us |

The experimental modal errors were computed from the sampled local error, while the model modal error are based on the continuous time value. Despite this, the measured values are very close to the ones shown in Table IV-2, even the corrector zero impact on Mode 1 can be observed. This validate the proposed model ability to anticipate the system performance.

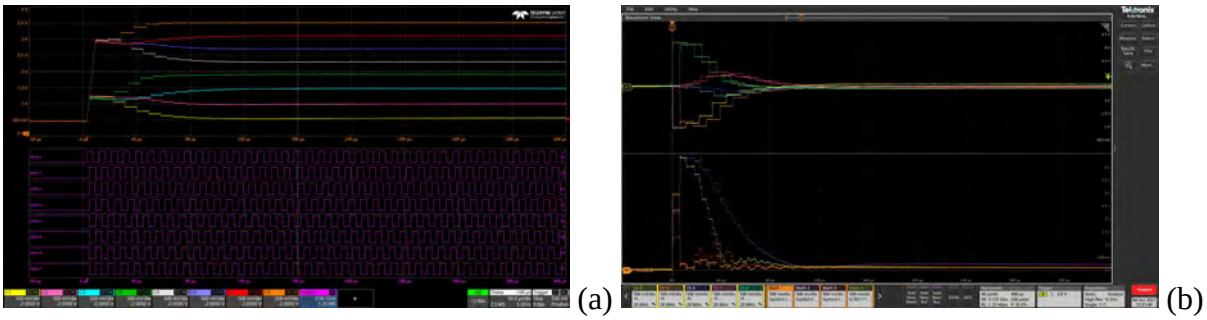
### IV.9.3. Start-up response validation

The start-up transients are also verified. Figure IV-28 shows the start-up response measurements with one PD in phase opposition (1+7). Figure IV-29 shows the start-up response measurements with by groups (4+4).



(a) (b)

*Figure IV-28 – Start-up response with one PD in phase opposition (1+7): a) PDs and clks; b) errors and modal errors.*



(a) (b)

*Figure IV-29 – Start-up response by groups (4+4): a) PDs and clks; b) errors and modal errors.*

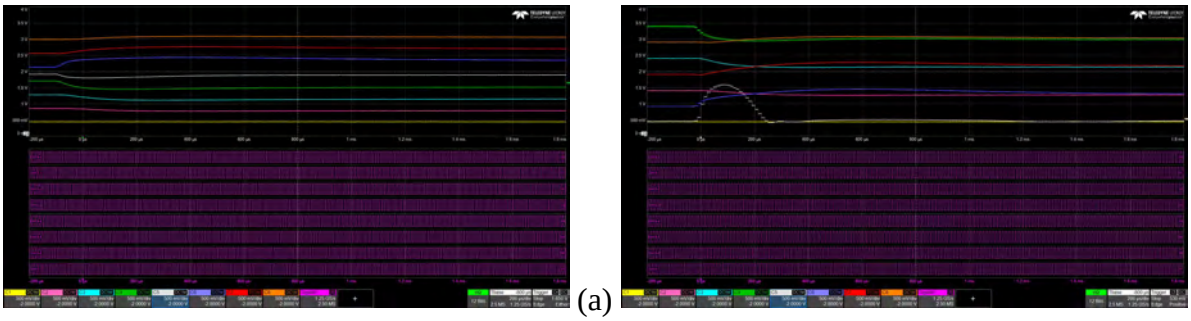
The start-up responses measurements support the behavior predicted with the model, showing that the start-up response by groups (4+4) converges faster than the start-up with one PD in phase opposition because the Mode 1 is not disturbed.

### IV.9.4. Reconfiguration response validation

These reconfiguration simulations were meant to demonstrate the necessity of pre-positioning a bypassed between their neighbors when inserted. Figure IV-30 (a) shows a well interleaved system where $\theta_5$ is pre-positioned between $\theta_4$ and $\theta_6$ and then inserted to complete $N = 8$. The transient is smooth, but takes time to achieve steady-state because Mode 1 is disturbed.

Multiples unsuccessfully attempts were made to obtain a proper measurement where LC5 is coincident with $\theta_1$ at the begging, even using the pre-positioning. When bypassed, LC5 was always able to position itself between its neighbors. This is a good result, observed in the particular case $N = 7$ (LC5 bypassed), but the cause and the extension to other values of $N$ has to be demonstrated.

Figure IV-30 (b) shows a measurement where LC5 is bypassed at the beginning $N = 7$ and the PD differences are $2/N$. It should be noted that $\theta_5$ is in between its neighbors, even if coincident with $\theta_1$. When LC5 is inserted, the PDs arrange themselves by groups, as expected, such as shown in Figure II-18. The signals still interleaved, but not in a Proper Interleaved Arrangement. As a result, the spectral content of the modulated signals is not optimal, considering optimal the highest as possible.



(a) (b)

*Figure IV-30 – LC5 insertion transient measurement, PD differences: a)* $1/N$*; b)* $2/N$.

### IV.9.5. Short to ground fault response validation

The behavior in case of connection link failure were reveals theoretically using the final value theorem. However, the measurement is needed to observe if the system diverges, and in negative case, what happens when the fault is removed.

Figure IV-31 shows a use case where the connection from LC1 to LC8 is shorted to ground during operation, i.e. LC8 input “CssN” is connected to 0V using the fault introduction

module. The experiment presents divided in 4 different states. The first state is at the beginning where all the LCs are properly interleaved.

When the fault is applied (0 ms), the second state starts. In this state, the LCs try to correct the error using the proportional corrector and a fast PD rearrangement can be observed. The PDs are in a non-uniform arrangement and get closer, what indicates an increasing frequency. This goes until a LC saturates.

The third state starts when a LC saturates (at 82 ms). At this point, one of the loops is broken. As this specific LC stops correcting the accepts to have a non-null error, a new steady-state proper interleaving is obtained, but with a frequency deviation.

The fourth state starts when the fault is removed (120 ms). The controller memory (integral effect) is slowly being removed and converges to the initial condition with proper interleaving and with the correct frequency.

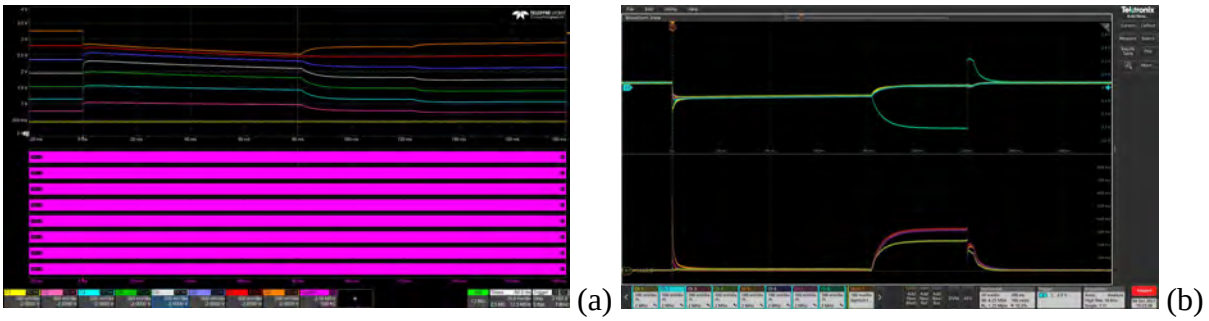

(a) (b)

*Figure IV-31 – LC8 CssN short to ground fault transient measurement: a) PDs and clks; b) errors and modal errors.*

### IV.9.6. Noisy immunity: frequency jitter measurement

A jitter measurement was performed in the interleaved system in steady-state with $N = 8$ to observe the noise immunity aspect of this proof-of-concept, shown in Figure IV-32. The clk signals of LCs 1 to 4 are shown on the left and of LCs 5 to 8 are shown on the right side, each of them with their histogram of the measured frequency jitter. It can be noted that the frequency deviation is limited to $\pm 15\ Hz$, corresponding to $\pm 0.017\%$ of the central frequency $88.6\ kHz$. Considering that no special care was taken other than the placement of a few decoupling capacitors to improve the noise immunity, this is a quite good result, proving this approach has good noise immunity.


*Figure IV-32 – Noise immunity: frequency jitter measurement.*

## IV.10. **Conclusion**

This chapter has presented the complete design and modeling of a new approach for the self-interleaving of carriers using digital signals for the inter-LC communications. A controller has been designed to meet the system stability criterion and obtain good transient performance. A proof-of-concept has been built and experimental measurements have been performed. The experimental results support the developed theoretical study.

This innovative approach is robust and can work properly with many active local controllers. The controller is flexible and easy to design using classical control theory because the diagonal systems where revealed. The controller chosen guarantees a good transient performance with low static error. Reconfiguration events are operational. They do not disturbs the duty-cycle of the PWM signals because the method consists to sample the error at each period. The LC events are synchronized with the beginning of each clock period to avoid incorrect PD measurement.

The corrector designed was used in the proof-of-concept and the modal behavior has been measured and correlates with the theoretical one. The measurements during start-up transients with multiple disturbed modes also correlate with the theoretical, each individual mode had its expected transient without interactions with the other modes.

Thanks to the digital signals used, the communication links between devices are now robust and present no matching issues. It should be noted however, the inability to interleave between coincident neighbors makes start-up with numerous elements risky. But this issue can

be solved using a different PD detector that extends the error detection to the region where the neighbors are coincident.

Nevertheless, no issues were observed during experimental measurements with the error detector used. The performance was even better than expected, where the insertion of a non-pre-positioned lead ways to a correct interleaving. This may be the result of the interaction with the others LCs, i.e. the group behavior surpass local flaws. No conclusion can be stated because these special cases with coincident neighbors are in limit of validity of the proposed model.

The introduction of a short to ground fault did not lead to a catastrophic failure in the tested used case. Only a frequency deviation and a temporary incorrect interleaving were observed. As soon as the fault was removed, the system recovered to the correct interleaving.

The frequency jitter measurement proved this approach has good noise immunity. An integrated circuit implementation will probably perform even better.

# Conclusion

The theoretical procedure presented in this thesis where able to correlate with the circuit based simulations and the proof-of-concept experimental validation. This study provides the tools needed to design a robust distributed interleaving system, with good transient, static and noise immunity performances.

The study of the digital approach in chapter II brough basic understanding of the circular chain constraints, mainly about the fact that a trade-off is needed to select the closed loop performance because all modes share almost the same transfer function with only a different gain. A transient optimization method was proposed and applied. Important elements for simulation were also highlighted and verified. The necessity of the shared clock line was the major issue to discard this interleaving approach.

The study of the triangular carrier self-alignment in chapter III brough understanding to the modeling of non-synchronized systems by referring all of them to the same phase reference. After modeling, the stability criteria was revealed and transient performance optimization performance. A cyclic delay appears in the interconnections and a rotation effect was seen in the transient responses. The usage of analog connections and mismatch issues were the major issue to discard this interleaving approach.

A new approach was proposed using digital signals self-interleaving in chapter IV. The conception was meant to avoid the issues on the two previous studied approaches. A basic structure was proposed, the modeling and corrector design performed. The modeling and theoretical study were validated with simulation and then a proof-of-concept was shown. The proof-of-concept validations present very good performance, being robust and easy to implement.

As perspective, the implementation this new approach in an integrated circuit and validation remains to be done, as well as use of the interleaved clocks to generate the interleaved PWM signals of a multiphase converter.

## References


[1] “Three things to know about functional safety.” https://www.nxp.com/company/blog/three-things-to-know-about-functional-safety:BL-3-THINGS-TO-KNOW-FUNCTIONAL-SAFETY (accessed Oct. 18, 2021).

[2] “Difference Between Centralized vs Decentralized vs Distributed network,” *Crypto Post Gazette*, Feb. 02, 2020. https://www.cryptopostgazette.com/centralized-vs-decentralized-vs-distributed-network/ (accessed Oct. 18, 2021).

[3] F. Dehmelt, “Adaptive (Dynamic) Voltage (Frequency) Scaling—Motivation and Implementation.” 2014.

[4] A. Miyoshi, C. Lefurgy, E. Van Hensbergen, R. Rajamony, and R. Rajkumar, “Critical power slope: understanding the runtime effects of frequency scaling,” in *Proceedings of the 16th international conference on Supercomputing*, 2002, pp. 35–44. Accessed: Dec. 20, 2016. [Online]. Available: http://dl.acm.org/citation.cfm?id=514200

[5] Kaiwei Yao, Ming Xu, Yu Meng, and F. C. Lee, “Design considerations for vrm transient response based on the output impedance,” *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1270–1277, Nov. 2003, doi: 10.1109/TPEL.2003.818824.

[6] W. Kim, “Fine-Grain Power Management in Multicore SoCs using Integrated Voltage Regulators - 6.5_Gu-yeon Wei.pdf,” 2013. Accessed: Feb. 10, 2017. [Online]. Available: http://pwrsocevents.com/wp-content/uploads/2012-presentations/session-6/6.5_Gu-yeon%20Wei.pdf

[7] E. A. Burton *et al.*, “FIVR #x2014; Fully integrated voltage regulators on 4th generation Intel #x00AE; Core #x2122; SoCs,” in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Mar. 2014, pp. 432–439. doi: 10.1109/APEC.2014.6803344.

[8] C. Bos, “Tesla’s New HW3 Self-Driving Computer — It’s A Beast (CleanTechnica Deep Dive),” *CleanTechnica*, Jun. 15, 2019. https://cleantechnica.com/2019/06/15/teslas-new-hw3-self-driving-computer-its-a-beast-cleantechnica-deep-dive/ (accessed Oct. 18, 2021).

[9] K. T. Small, *Single wire current share paralleling of power supplies*. Google Patents, 1988. Accessed: Aug. 24, 2017. [Online]. Available: http://www.google.com/patents/US4717833

[10] C.-S. Lin and C.-L. Chen, “Single-Wire Current-S are Paralleling of Current-Mode Controlled DC Power Supplies,” 1998, Accessed: Aug. 21, 2017. [Online]. Available: https://pdfs.semanticscholar.org/b49d/8de03042b36e428f33dee4f2584573a906a8.pdf

[11] M. Le Bolloch, M. Cousineau, and T. Meynard, “New masterless modular current-sharing technique for DC/DC parallel converters,” in *Power Electronics and Motion Control Conference (EPE/PEMC), 2010 14th International*, 2010, pp. T3-73. Accessed: Sep. 07, 2017. [Online]. Available: http://ieeexplore.ieee.org/abstract/document/5606884/

[12] X. Zhang and A. Huang, “MVRC and its tolerance analysis for microprocessor power management,” 2006. Accessed: Aug. 23, 2017. [Online]. Available: http://ieeexplore.ieee.org/iel7/11209/36090/01711734.pdf

[13] M. Cousineau and Z. Xiao, “Fully masterless control of parallel converter,” in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, 2013, pp. 1–10. Accessed: Sep. 07, 2017. [Online]. Available: http://ieeexplore.ieee.org/abstract/document/6631848/

[14] S. Pierre, “End OF Column Circuits – Design Review - ppt download.” https://slideplayer.com/slide/12468413/ (accessed Oct. 18, 2021).
[15] “Johnson Ring Counter and Synchronous Ring Counters,” *Basic Electronics Tutorials*, Aug. 30, 2013. https://www.electronics-tutorials.ws/sequential/seq_6.html (accessed Oct. 18, 2021).
[16] M. A. M. Hendrix, R. V. D. Wal, J. J. Leijssen, and J. A. M. V. Erp, “Interleaved switching converters in ring configuration,” US7394232B2, Jul. 01, 2008 Accessed: Jul. 23, 2018. [Online]. Available: https://patents.google.com/patent/US7394232B2/en?q=modular&q=interleaved&q=converter&oq=modular+interleaved+converter&page=1
[17] W. Chen, “High efficiency, high density, PolyPhase converters for high current applications,” in *Analog Circuit Design*, Elsevier, 1999, pp. 272–285. doi: 10.1016/B978-0-12-385185-7.00014-7.
[18] T. Kohama, Y. Minoda, and T. Ninomiya, “New synchronizing circuit for switching power module with automatic interleaving operation,” in *Telecommunications Energy Conference, 2002. INTELEC. 24th Annual International*, 2002, pp. 510–515. Accessed: Aug. 23, 2017. [Online]. Available: http://ieeexplore.ieee.org/abstract/document/1048704/
[19] X. Zhang and Z. Huang, “A novel distributed interleaving scheme to achieve scalable phase design for microprocessor power management,” in *Proc. IEEE Power Electron. Spec. Conf*, 2006, pp. 1–7. Accessed: Aug. 23, 2017. [Online]. Available: http://ieeexplore.ieee.org/iel7/11209/36090/01711950.pdf
[20] W. Huang, G. Schuellein, and D. Clavette, “A scalable multiphase buck converter with average current share bus,” in *Applied Power Electronics Conference and Exposition, 2003. APEC’03. Eighteenth Annual IEEE*, 2003, vol. 1, pp. 438–443. Accessed: Aug. 23, 2017. [Online]. Available: http://ieeexplore.ieee.org/abstract/document/1179250/
[21] L.-A. Grégoire, M. Cousineau, S. I. Seleme jr, and P. Ladoux, “Real-Time Simulation of Interleaved Converters with Decentralized Control,” *Renewable Energy and Power Quality Journal*, pp. 268–273, May 2016, doi: 10.24084/repqj14.287.
[22] G. Gateau, P. Q. Dung, M. Cousineau, P. T. Do, and H. N. Le, “Digital implementation of decentralized control for multilevel converter,” in *System Science and Engineering (ICSSE), 2017 International Conference on*, 2017, pp. 558–562.
[23] D. J. Perreault and J. G. Kassakian, “Distributed interleaving of paralleled power converters,” *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 44, no. 8, pp. 728–734, 1997.
[24] J. Kudtongngam, P. Liutanakul, and V. Chunkag, “Automatic interleaving technique using single interleaving bus for paralleling power converters,” *IET Power Electronics*, vol. 8, no. 8, pp. 1519–1530, 2015, doi: 10.1049/iet-pel.2014.0406.
[25] L. Feng and Q. Wenlong, “Implementation of an automatic interleaving approach for parallel DC/DC converter without interleaving bus,” in *Sixth International Conference on Electrical Machines and Systems, 2003. ICEMS 2003.*, Nov. 2003, vol. 1, pp. 368–371 vol.1.
[26] S. Dutta *et al.*, “Decentralized Carrier Interleaving in Cascaded Multilevel DC-AC Converters,” in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Toronto, ON, Canada, Jun. 2019, pp. 1–6. doi: 10.1109/COMPEL.2019.8769699.
[27] M. Sinha, S. Dhople, B. Johnson, M. Rodriguez, and J. Poon, “Decentralized interleaving of paralleled dc-dc buck converters,” Jul. 2017, pp. 1–6. doi: 10.1109/COMPEL.2017.8013331.

[28] M. Cousineau, M. Le Bolloch, N. Bouhalli, E. Sarraute, and T. Meynard, “Triangular carrier self-alignment using modular approach for interleaved converter control,” in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1–10. Accessed: Sep. 07, 2017. [Online]. Available: http://ieeexplore.ieee.org/abstract/document/6020123/

[29] Z. Xiao and M. Cousineau, “Modular interleaved carrier generator using a straightforward implementation method,” in *Electronics, Control, Measurement, Signals and their application to Mechatronics (ECMSM), 2013 IEEE 11th International Workshop of*, 2013, pp. 1–6. Accessed: Sep. 07, 2017. [Online]. Available: http://ieeexplore.ieee.org/abstract/document/6648934/

[30] M. A. H. Broadmeadow and K. D. Sands, “Self-organising technique for carrier synchronisation and phase offset distribution in modular, fault-tolerant converters,” *The Journal of Engineering*, vol. 2019, no. 17, pp. 4283–4287, 2019, doi: 10.1049/joe.2018.8057.

[31] S. K. Murray, M. Nasr, M. Ashourloo, and O. Trescases, “Masterless Interleaving Scheme for Parallel-Connected Inverters Operating with Variable Frequency Hysteretic Current-Mode Control,” in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, Mar. 2019, pp. 277–283. doi: 10.1109/APEC.2019.8722262.

[32] S. I. Seleme, L. A. Gregoire, M. Cousineau, and P. Ladoux, “Decentralized Controller for Modular Multilevel Converter,” in *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2016, pp. 1–8.

[33] B. Hunt, “A matrix theory proof of the discrete convolution theorem,” *IEEE Transactions on Audio and Electroacoustics*, vol. 19, no. 4, pp. 285–288, Dec. 1971, doi: 10.1109/TAU.1971.1162202.

[34] M. Mannes Hillesheim, M. Cousineau, M. Vivert, G. Aulagnier, and G. Gateau, “Eigendecomposition of a digital iterative decentralised interleaving for multicellular converters,” *Mathematics and Computers in Simulation*, p. S037847542030241X, Jul. 2020, doi: 10.1016/j.matcom.2020.07.014.

[35] Q.-D. Phan, A.-N. Le, D.-T. Nguyen, M.-T. Nguyen, and G. Gateau, “Modified Decentralized Control for Multiphase Converters,” p. 7, 2019.

[36] O. Troeng, B. Bernhardsson, and C. Rivetta, “Complex-coefficient systems in control,” in *2017 American Control Conference (ACC)*, Seattle, WA, USA, May 2017, pp. 1721–1727. doi: 10.23919/ACC.2017.7963201.

[37] M. M. Hillesheim, M. Cousineau, and L. Hureau, “Reconfigurable Partial-Decentralized Control of a Multiphase Converter for Fail-Operational Automotive Processor Power Supply,” in *2019 21st European Conference on Power Electronics and Applications (EPE ’19 ECCE Europe)*, Genova, Italy, Sep. 2019, p. P.1-P.8. doi: 10.23919/EPE.2019.8915561.

## Annex A **Proof 1: Lead-lag controller stability criterion**

The stability criterion can be find by studding the system's modal closed loop poles $p_1$ and $p_2$. The differential mode natural (homogeneous) transfer function response is shown in Eq. (A-1).

$$\theta^*_{mh}(z) = \frac{z^2 - (p_{OL} + 1)\, z + p_{OL}}{z^2 - (p_{OL} + 1 + \alpha\, \lambda_m)\, z + (p_{OL} + \alpha\, \lambda_m\, z_{OL})}\, {\theta_0}^*_i, \quad \mathrm{m} = 1 \ldots \mathrm{M} - 1 \qquad \text{(A-1)}$$

Poles $p_1$ and $p_2$ can be found by applying the Bhaskara's formula to the denominator, as shown in Eq. (A-2).

$$\begin{matrix} a_d = 1 \\ b_d = -(p_{OL} + 1 + \alpha\, \lambda_m) \\ c_d = p_{OL} + \alpha\, \lambda_m\, z_{OL} \end{matrix} \quad p_{1\_m}, p_{2\_m} = \frac{-b_d \pm \sqrt{{b_d}^2 - 4\, a_d\, c_d}}{2\, a_d}, \quad \mathrm{m} = 0 \ldots \mathrm{M} - 1 \qquad \text{(A-2)}$$

Solve the Bhaskara's formula analytically without any considerations proves to be very hard. Looking at the root locus, it can be noticed in Figure II-7(d) that the blue root locus line is always inside the unit circle for $\alpha > 0$. However, the green root locus line for $\alpha > 0$ is equals to $-1$ when it passes through the unit circle. As both poles are real and different, ${b_d}^2 - 4\, a_d\, c_d > 0$. As the sought pole is the smaller one and $a_d > 0$, it comes from the negative square root term. To stay in the unit circle, the simplified condition shown in Eq. (A-2) can be written as shown in Eq. (A-3) to define the stability criterion.

$$p_{2\_m} = \frac{-b_d - \sqrt{{b_d}^2 - 4\, a_d\, c_d}}{2\, a_d} > -1, \qquad \begin{cases} -2 \le \lambda_m < 0 \\ a_d > 0 \\ \mathrm{m} = 1 \ldots \mathrm{M} - 1 \end{cases} \qquad \text{(A-3)}$$

Eq. (A-4) shows the development of Eq. (A-3).

$$\begin{aligned} if\ a_d = 1 \quad &\Rightarrow \quad -\sqrt{{b_d}^2 - 4\, c_d} > b_d - 2 \\ if\ {b_d}^2 - 4\, c_d > 0 \quad &\Rightarrow \quad {b_d}^2 - 4\, c_d < (b_d - 2)^2 \\ then \quad &\Rightarrow \quad {b_d}^2 - 4\, c_d < {b_d}^2 - 4\, b_d + 4 \\ &\Rightarrow \quad -c_d < -b_d + 1 \\ &\Rightarrow \quad c_d - b_d > -1 \end{aligned} \qquad \text{(A-4)}$$

Eq. (A-5) by replacing $b_d$ and $c_d$ from Eq. (A-2) in Eq. (A-4) result.

$$
\begin{aligned}
&(p_{OL} + \alpha\,\lambda_m\,z_{OL}) + (p_{OL} + 1 + \alpha\,\lambda_m) > -1 \\
&\Rightarrow \quad \alpha\,\lambda_m(1 + z_{OL}) > -2\,(1 + p_{OL}) \\
&\Rightarrow \quad \alpha\,\lambda_m > -2\,\frac{1 + p_{OL}}{1 + z_{OL}} \qquad \text{(A-5)} \\
&if \ -2 \le \lambda_m < 0 \quad \Rightarrow \quad \alpha < \frac{1 + p_{OL}}{1 + z_{OL}}
\end{aligned}
$$

The final condition is find combining this condition with the start one ($\alpha > 0$).

## Annex B **Proof 2: Triangular carrier self-alignment C(z) corrector expression**

The local triangular signal commutation instant is studied to determine the expression of the correction value $\Delta\theta^k$ as a function of the error $\varepsilon_\theta$ and other implementation parameters.

Figure B-1 shows in details the waveforms near the iteration instant, where local triangular carrier $V_{tri}$ rises until touching the threshold voltage $V_{thld}$.

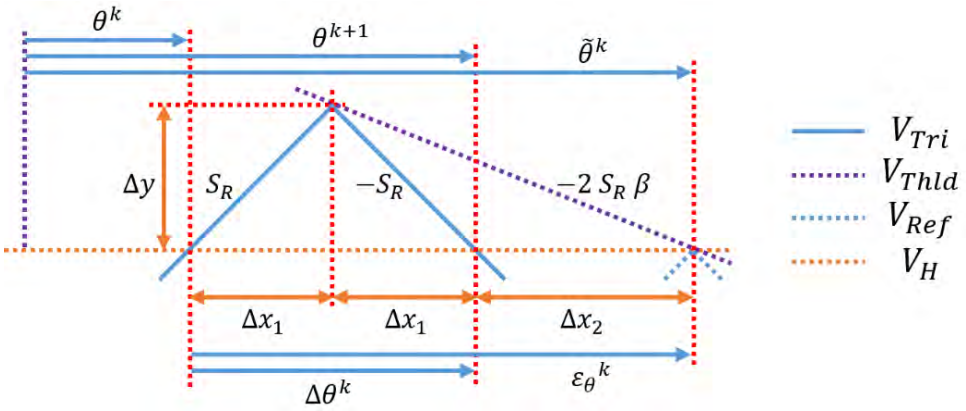



*Figure B-1 – Iteration instant details.*

To ensure the result is a linear expression, two conditions have to be verified:

1. the PDs are in an ascending sequence as shown in Eq. (B-1);

$$\theta_P{}^{k+1} \le \theta^k \le \theta_N{}^k, \quad \frac{\theta_N{}^k - \theta_P{}^{k+1}}{2} \le 0.5 \tag{B-1}$$

2. Vtri commutation happens in an instant when $V_{thld}$ has a slope equal to $-2\,S_R\,\beta$, with the constraints shown in Eq. (B-2).

$$-\infty < -2\,\beta\,S_R < S_R \quad \Longrightarrow \quad -0.5 < \beta < +\infty \tag{B-2}$$

Starting with two basic equations:

$$\Delta\theta^k = 2\,\Delta x_1 \tag{B-3}$$

$$\varepsilon_\theta{}^k = 2\,\Delta x_1 + \Delta x_2 \tag{B-4}$$

Solve $\Delta x_2$ to $\Delta x_1$:

$$\begin{aligned} \Delta y = S_R\,\Delta x_1 &= 2\,\beta\,S_R\,(\Delta x_1 + \Delta x_2) \\ \Longrightarrow \quad \Delta x_1 &= 2\,\beta\,(\Delta x_1 + \Delta x_2) \end{aligned} \tag{B-5}$$

$$\Longrightarrow \quad \Delta x_2 = \frac{1-2\,\beta}{2\,\beta}\Delta x_1$$

Solve $\varepsilon_\theta$ to $\Delta x_1$:

$$\varepsilon_\theta = 2\,\Delta x_1 + \Delta x_2$$

$$\Longrightarrow \quad \varepsilon_\theta = 2\,\Delta x_1 + \frac{1-2\,\beta}{2\,\beta}\Delta x_1$$

$$\Longrightarrow \quad \varepsilon_\theta = \frac{4\,\beta}{2\,\beta}\Delta x_1 + \frac{1-2\,\beta}{2\,\beta}\Delta x_1 \tag{B-6}$$

$$\Longrightarrow \quad \varepsilon_\theta = \frac{1+2\,\beta}{2\,\beta}\Delta x_1$$

Then:

$$\Delta x_1 = \frac{2\,\beta}{1+2\,\beta}\varepsilon_\theta \quad \Longrightarrow \quad \Delta\theta = 2\,\frac{2\,\beta}{1+2\,\beta}\varepsilon_\theta \tag{B-7}$$

It proves:

$$\mathrm{C}(z) = \frac{\Delta\theta(z)}{\varepsilon_\theta(z)} = \alpha = \frac{4\,\beta}{1+2\,\beta}, \qquad \begin{array}{c} {\theta_P}^{k+1} \le \theta^k \le {\theta_N}^k \\ \dfrac{{\theta_N}^k - {\theta_P}^{k+1}}{2} \le 0.5 \\ -0.5 < \beta < +\infty \end{array} \tag{B-8}$$

It should be noted that this expression is valid even beyond these limits.

## Annex C **Proof 3: Triangular carrier self-interleaving stability criterion.**

The differential close loop eigenvalues formula and its validity conditions are given in Eq. (C-1).

$$\lambda_{Ai} = \frac{1 - \alpha\,(1 - 0.5\,\lambda_i{}^*)}{1 - \alpha\,0.5\,\lambda_i}, \qquad -\infty < \alpha < 2, \qquad i = 0 \ldots N-1 \tag{C-1}$$

The stability condition shown in Eq. (C-2) is derived from Eq. (C-1), where $\alpha \in \mathbb{R}$ that respects the inequality has to be find.

$$|\lambda_{Ai}| = \left|\frac{1 - \alpha\,(1 - 0.5\,\lambda_i{}^*)}{1 - \alpha\,0.5\,\lambda_i}\right| < 1, \quad \begin{matrix} -1 \le |\lambda_i| < 1 \\ \therefore -1 \le Re(\lambda_i) < 1' \end{matrix} \quad i = 1 \ldots N-1 \tag{C-2}$$

Using absolute value properties, the inequality in Eq. (C-2) is rewritten such as in Eq. (C-3):

$$\left|\frac{1 - \alpha\,(1 - 0.5\,\lambda_i{}^*)}{1 - \alpha\,0.5\,\lambda_i}\right| < 1 \;\Leftrightarrow\; \frac{|1 - \alpha\,(1 - 0.5\,\lambda_i{}^*)\,|}{|1 - \alpha\,0.5\,\lambda_i|} < 1, \quad \begin{matrix} if\ (1 - \alpha\,0.5\,\lambda_i) \neq 0 \\ \therefore \alpha \neq -2 \end{matrix} \tag{C-3}$$

There is no $\alpha$ restriction solution if $\lambda_i$ is a complex number. The only pure real $\lambda_i$ value is –1 and it leads to a restriction $\alpha \neq -2$.

The new inequality in Eq. (C-3) can be rewritten as in Eq. (C-4).

$$|1 - \alpha\,(1 - 0.5\,\lambda_i{}^*)\,| < |1 - \alpha\,0.5\,\lambda_i| \tag{C-4}$$

As this is a complex expression, the absolute value operator in Eq. (C-4) can be rewritten by its definition in Eq. (C-5).

$$\sqrt{Re(Num)^2 + Im(Num)^2} < \sqrt{Re(Den)^2 + Im(Den)^2} \tag{C-5}$$

where:

$$Re(Num) = 1 - \alpha + \alpha\,0.5\,Re(\lambda_i{}^*) \qquad Im(Num) = \alpha\,0.5\,Im(\lambda_i{}^*)$$
$$Re(Den) = 1 - \alpha\,0.5\,Re(\lambda_i) \qquad Im(Den) = -\alpha\,0.5\,Im(\lambda_i)$$

It can be noted that the complex parts in Eq. (C-5) are equal, then, the inequality to be true, it has to respect the condition in Eq. (C-6).

$$Re(Num)^2 < Re(Den)^2 \tag{C-6}$$

An term equal to $Re(Den)$ can be find in $Re(Num)$ by adding and removing one unity, i.e. (+1 –1), as shown in Eq. (C-7).

$$Re(Num) = (2-\alpha) - [1 - \alpha\ 0.5\ Re(\lambda_i{}^*)] = (2-\alpha) - Re(Den) \tag{C-7}$$

Eq. (C-8) shows the development of the first square of Eq. (C-6).

$$\begin{gathered}(2-\alpha)^2 - 2\ (2-\alpha)\ Re(Den) + Re(Den)^2 < Re(Den)^2 \\ \Longrightarrow \quad (2-\alpha)^2 - 2\ (2-\alpha)\ [1 - \alpha\ 0.5\ Re(\lambda_i{}^*)] < 0\end{gathered} \tag{C-8}$$

By putting $(2-\alpha)$ as a common factor, the expression in (C-8) expression can be rewritten as in Eq. (C-9).

$$\begin{cases}\text{if } (2-\alpha) > 0 \\ \quad \therefore \alpha < 2\end{cases} \quad \Longrightarrow \quad (2-\alpha)\ \alpha\ [Re(\lambda_i{}^*) - 1] < 0 \tag{C-9}$$

Knowing Eq. (C-10),

$$\begin{gathered}-1 \le |\lambda_i| < 1 \quad \Longrightarrow \quad -1 \le Re(\lambda_i) = Re(\lambda_i{}^*) < 1, \qquad i = 1 \ldots N-1 \\ \therefore -2 \le Re(\lambda_i{}^*) - 1 < 0\end{gathered} \tag{C-10}$$

Then Eq. (C-11) can be derived from (C-9).

$$(2-\alpha)\ \alpha > 0 \quad \Leftrightarrow \quad 0 < \alpha < 2 \tag{C-11}$$

The stability criterion in Eq.(C-11) in valid the whole interval shown because the restrictions in Eq. (C-1), Eq. (C-3) and Eq. (C-9) are valid.

# Annex D **Triangular carrier self-alignment simulation guidelines**

The system state equations are shown in Eq. (D-1) and Eq. (D-2).

$$\boldsymbol{\theta}^{k+1} = (\boldsymbol{I} - \alpha\, 0.5\, \boldsymbol{S}\,)^{-1}\,[(1-\alpha)\,\boldsymbol{I} + \alpha\, 0.5\, \boldsymbol{S}^{*}]\,\boldsymbol{\theta}^{k} + (\boldsymbol{I} - \alpha\, 0.5\, \boldsymbol{S}\,)^{-1}\,(\alpha\,\boldsymbol{\varphi}^{k} + \boldsymbol{d}^{k}) \quad \text{(D-1)}$$

$$\boldsymbol{\varepsilon}_{\theta}{}^{k} = 0.5\, \boldsymbol{S}\, \boldsymbol{\theta}^{k+1} + (0.5\, \boldsymbol{S}^{*} - \boldsymbol{I})\, \boldsymbol{\theta}^{k} + \boldsymbol{\varphi}^{k} \quad \text{(D-2)}$$

This system can then be written in a discrete state space representation for simulation, such as in Eq. (D-3) and Eq. (D-4).

$$\boldsymbol{x}^{k+1} = \mathbf{A}\, \boldsymbol{x}^{k} + \mathbf{B}\, \boldsymbol{u}^{k} \quad \text{(D-3)}$$

$$\boldsymbol{x}^{k+1} = \mathbf{A}\, \boldsymbol{x}^{k} + \mathbf{B}\, \boldsymbol{u}^{k} \quad \text{(D-4)}$$

The PDs $\boldsymbol{\theta}$ are the state variables $\boldsymbol{x}$ are, the local errors $\boldsymbol{\varepsilon}_{\theta}$ are placed as output variable $\boldsymbol{y}$ for observation. The input signals $\boldsymbol{\varphi}$ and $\boldsymbol{d}$ are placed in the input $\boldsymbol{u}$, as shown in Eq. (D-5). Any other connection is required because the system is already in the closed-loop form. Being thus, the natural response found is directly the closed-loop system behavior being sought.

$$\boldsymbol{x} = \boldsymbol{\theta} \qquad \boldsymbol{y} = \boldsymbol{\varepsilon}_{\boldsymbol{\theta}} \qquad \boldsymbol{u} = \begin{bmatrix} \boldsymbol{\varphi} \\ \boldsymbol{d} \end{bmatrix} \quad \text{(D-5)}$$

By comparison of Eq. (D-3) with Eq. (D-1), the equivalent matrices for space state representation are shown in Eq. (D-6) are found.

$$\boldsymbol{A} = (\boldsymbol{I} - \alpha\, 0.5\, \boldsymbol{S}\,)^{-1}\,[(1-\alpha)\,\boldsymbol{I} + \alpha\, 0.5\, \boldsymbol{S}^{*}] \qquad \boldsymbol{B} = (\boldsymbol{I} - \alpha\, 0.5\, \boldsymbol{S}\,)^{-1}[\,\alpha\boldsymbol{I} \quad \boldsymbol{I}\,] \quad \text{(D-6)}$$

The error expression in Eq. (D-2) can be rewritten as a function of the state variables $\boldsymbol{\theta}$ and of the input vector $\boldsymbol{u}$. By comparison of Eq. (D-4) with Eq. (D-2), the equivalent matrices for space state representation are shown in Eq. (D-7) are found.

$$\boldsymbol{C} = 0.5\, \boldsymbol{S}\, \boldsymbol{A} + 0.5\, \boldsymbol{S}^{*} - \boldsymbol{I} \qquad \boldsymbol{D} = 0.5\, \boldsymbol{S}\, \boldsymbol{B} + [\,\boldsymbol{I} \quad \mathbf{0}\,] \quad \text{(D-7)}$$

By post processing the modal disturbances and modal error are calculated, such as shown in Eq. (D-8), but only its *M* first components are generally shown to avoid plotting redundant data.

$$|\boldsymbol{d}^{*}| = |\boldsymbol{W}^{*}\, \boldsymbol{d}| \qquad |\boldsymbol{\varepsilon}_{\theta}{}^{*}| = |\boldsymbol{W}^{*}\, \boldsymbol{\varepsilon}_{\theta}| \quad \text{(D-8)}$$

# Annex E **Other differential phase detector implementations**

Small manipulations can be done to displace the dead zone away and extend the linear zone in the proper region.

The modification to displace the $\theta_N - \theta_P = 0$ dead zone consists in adding a delay in one of the $UP/DN$ logic inputs, as shown in Eq. (E-1), where a normalized delay $\theta_d = t_d/T_0$ is added to $L$ in $UP$ and the same delay is added to $N$ in $DN$.

$$UP = \bar{P} \cdot delay(L, \theta_d) \qquad DN = \bar{L} \cdot delay(N, \theta_d) \tag{E-1}$$

$$\text{where} \quad delay(L(t), \theta_d) = L(t - T_0\theta_d) \qquad delay(N(t), \theta_d) = N(t - T_0\theta_d)$$

As a result, part of the perceived error response is shifted in the $\theta_N - \theta_P$ by $\theta_d$. The result is shown in Figure E-1, where $\theta_d$ is equal to 0.1. The picture shows the $\theta_d$ shift in the $\theta_N - \theta_P$ axis. The optimal $\theta_d$ value is not discussed in this work.

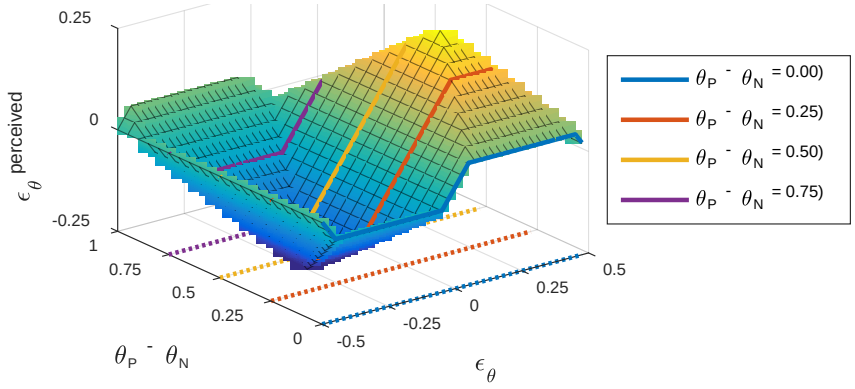



*Figure E-1 – Shifted perceived error plot when* $\theta_d = 0.1$.

The picture shows the $\theta_d$ shift in the $\theta_N - \theta_P$ axis. This system pushes away the dead zone in the perceived error when $\theta_N - \theta_P$ is close to zero.

Other possibility is to use two Phase Frequency Detector (PFD) to enlarge the perceived error range and presumably the lock-in range too, as shown in as shown in Figure E-2 (a). The PFD is composed basically of two D-type flip-flops and a reset circuit as shown in Figure E-2 (b). The previous and next clock signals are considered as references (REF), one in each PFD. The local clock is connected in both feedback inputs (VAR). Two charge pumps are also necessary, so their outputs are connected together to feed the loop filter.

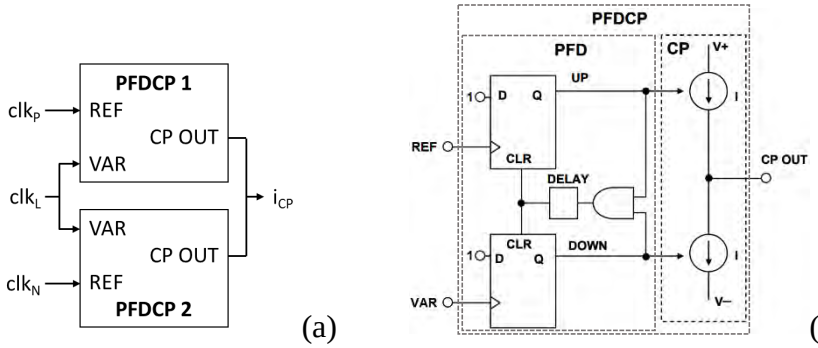



*Figure E-2 – Error detector: a) composed of two PFDCP, b) PFDCP: Phase Frequency Detector (PFD) and Charge Pump (CP).*

The perceived error plot when the three signals have the same frequency is shown in Figure E-3.

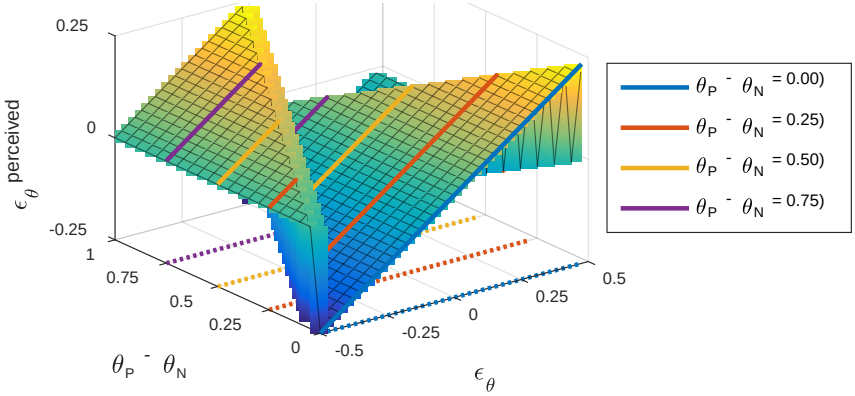



*Figure E-3 – Perceived error by an error detector composed of two PFDCP.*

The correct range of the perceived error region is larger in the region where $\theta_N - \theta_P$ values are small, being almost 50% of the total area, while it was only about 25% in the XOR and derivate cases. It is a huge advantage, but this criteria is not sufficient. It can be noted as well this approach result in two discontinuities in the phase detector transfer function (bounds of the region where $\varepsilon_\theta{}' = \varepsilon_\theta$ and $\theta_N - \theta_P = 0$) and a second stable equilibrium point ($|\varepsilon_\theta| = 0.5$) This can result in carriers placed in phase opposition to their expected value. It can be an issue during start-up, for example, when some elements are placed exactly at the discontinuity, having $\theta_P - \theta_L = 0.5$ and $|\varepsilon_\theta| = 0.25$ or $\theta_N - \theta_P = 0$. It can lead to non-causal behavior.

Indeed, the start-up condition are not so accurate due to noise and mismatches, so the final reached stead-state may not be linked to the initial conditions because at least two stable equilibrium points exist. Additional logic could be added to try to avoid these discontinuities, however these studies will not be carried out in this work.

Combining both PFD outputs in a single charge pump ($UP_{CP} = UP_1 + UP_2, DN_{CP} = DN_1 + DN_2$) would result in a gain reduction of 50% outside the region $\theta_P < \theta_L < \theta_N$, i.e. when the local is not between the neighbors.

# Annex F **Development of a modular distributed control monolithic fully integrated multiphase converter**

This annex is dedicated to the description of an integrated circuit development using NXP SmatMOS10 technology. This approach is intended to mitigate the SPOF in the distributed control architecture. The architecture is the same as the system described in [37], shown in Figure F-1, but with improvements in the current balance and interleaving approach, as shown in the previous chapter. With these changes, this device is more robust and goes a step closer to market requirements.

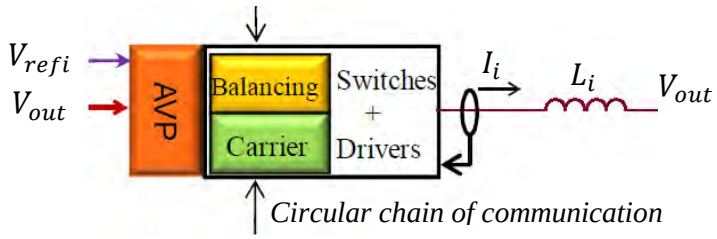



*Figure F-1 – One module block diagram of a distributed multiphase converter shown in [13].*

The following sections will explain the changes proposed in the current balance architecture, and then describe in detail de implementation of each block.

## Annex F.1 **Distributed voltage regulation and current balance**

The AVP technique make the output voltage $V_{out}$ dependent on the converter output current $I_{out}$. The converter output can be modelled as a voltage reference $V_{ref}$ in series with virtual output impedance called usually Load Line $R_{LL}$. In a multiphase converter with centralized control architecture, the AVP control technique is applied following the static relation $V_{out} = V_{ref} - R_{LL} \times I_{out}$, where the $I_{out}$ is the sum of all legs currents $I_i$.

The AVP can also be implemented to each leg and then combined in the same output, as shown in [12], [13]. Zhang shows in [12] that when independent references are used in each regulator, the combined output voltage tolerance is reduced (the shared voltage reference line is not mandatory). Using the shared voltage reference line reduces the leg current differences, but leg current $I_i$ still dependent on the equivalent local load line characteristic $R_{LLi}$.

The circular chain current balance technique shown in [13] is distributed and has no single point of failure because it uses only module-to-module connections. The current balance is made by adjusting the load line to combine all in the currents in a focal point, as shown in

Figure I-23. The current balance correctors with integrator can annul the error, but one current balance controller is disabled in order to avoid correction divergence. As no shared line is used, the focal point is always on the regulator characteristics where the balance regulator is disabled, and consequently the voltage precision improvement is lost.

A detailed study of this approach shows the current balance loop is non-linear because the multiplication of the corrected slope $\alpha'_i$ with $I_i$, two state variables. Additionally, this system can diverges because current balance errors are applied to two cascaded integrators. As a result, this current balance approach has two drawbacks:

1- The loop gain and consequently transient response depends on $I_{out}$.

2- The closed loop line load characteristics $R_{LL}$ may change if all correctors are activated with non-limited gain;

To remove the non-linearity, the voltage references should be adjusted to equalize the leg currents instead of changing the load line to balance the current. To have the voltage precision improvement when using current balance, all balance correctors must be active and have the same limited static gain.

## Annex F.2 **Voltage references adjustment: static behavior**

The output voltage and leg current tolerance analysis shall be written to reveal the advantages of using the voltage references adjustment with the circular chain. The static AVP relation is applied in each of the modular converter's legs, following the expression shown in Eq. (F-1).

$$V_{out} = V_{refi} - R_{LLi} \times I_i + R_{Ci} \times \varepsilon_i, \qquad i = 0 \dots N-1 \tag{F-1}$$

where $\varepsilon_i$ is the current error in the ith leg given by $\varepsilon_i = \frac{I_{i-1}+I_{i+1}}{2} - I_i$ and the current balance loop has static gain equals to $R_{Ci}$. The combined output voltage can be seen in Eq. (F-2).

$$V_{out} = \frac{1}{\sum_{i=1}^{N} \frac{1}{R_{LLi}}} \left\{ \sum_{i=1}^{N} \frac{V_{refi}}{R_{LLi}} + \sum_{i=1}^{N} \frac{R_{Ci} \times \varepsilon_i}{R_{LLi}} - I_{out} \right\} \tag{F-2}$$

The same load line $R_{LL}$ of the centralized case can be observed when each leg load line $R_{LLi}$ is equal to $R_{LLi} = N \times R_{LL}$. Considering the simplification where $R_{LLi} = N \times R_{LL}$ and $R_{Ci} = R_C$, the equivalent output voltage is shown in Eq. (F-3).

**Annex F**

$$V_{out} = \frac{\sum_{i=1}^{N} V_{refi}}{N} + R_C \sum_{i=1}^{N} \varepsilon_i - R_{LL} \times I_{out} \quad \text{(F-3)}$$

It should be noted that the output voltage $V_{out}$ tolerance benefits of the average of all voltage references $V_{refi}$. Additionally, the sum of the current leg errors is null, $\sum_{i=1}^{N} \varepsilon_i = 0$, so the current balance loop do not impacts the output voltage if $R_C$ is limited. As a result, this current balance structure with limited static gains allows to balance current keeping voltage reference tolerance improvement.

By replacing $V_{out}$ from Eq. (F-3) in Eq. (F-1) and considering $\sum_{i=1}^{N} \varepsilon_i = 0$, then the local current loop error can be expressed as shown in Eq. (F-4).

$$\varepsilon_i = \frac{\frac{\sum_{i=1}^{N} V_{refi}}{N} - V_{refi}}{R_{Ci}} - \frac{R_{LL} \times I_{out} - R_{LLi} \times I_i}{R_{Ci}} \quad \text{(F-4)}$$

This approach fulfill the two requirements. Eq. (F-3) shows the output voltage benefits of the voltage refence average and without impact of the current balance. Eq. (F-4) shows the current balance can mitigate local voltage reference and local load line deviations.