Contribution to wake-up radio design for sensor network applications

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Contribution à la conception et à la modélisation de wake-up radio pour réseaux de capteurs

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Résumé

L'utilisation de la wake-up radio (WUR) dans les applications de réseaux de capteurs est en croissance constante car elle permet de réduire considérablement la consommation d'énergie globale et d'augmenter la durée de vie de la batterie des capteurs. Le rôle de la WUR est de permettre à la radio principale de rester en mode veille le plus longtemps possible si aucune action n'est requise.

Cependant, la plupart des publications discutent de la théorie, de la simulation SPICE, ou des mesures de WUR, pour une seule topologie de WUR à la fois. Dans cette thèse, nous comparons plusieurs topologies. Ce travail décrit en détail le processus de simulation des circuits, la modélisation théorique, la conception de PCB, les mesures et l'optimisation du prototype. De plus, cette étude a réalisé des simulations de différents scénarios dans OMNeT++ pour examiner le comportement des nœuds dotés d'un WUR semi-actif sous différents modèles et frameworks. Nous avons proposé une méthode de modélisation de la couche physique pour considérer les performances de la WUR et son impact sur la transmission de données, complémentaire à la modélisation de la couche MAC.

Le Chapitre II a présenté une analyse et classification complète de l'état de l'art de la technologie de la wake-up radio. Nous avons résumé les principales caractéristiques du WUR sur la base de notre revue de la littérature, incluant type, technologie, sensibilité, consommation d'énergie, fréquence, modulation, latence, débit de données et adressage. L'analyse et les premiers résultats de simulation ont été fournis comme étude préliminaire pour un design adaptable à des cas particuliers, préparant l'implémentation et la modélisation de l'appareil.

Dans le Chapitre III, nous nous sommes concentrés sur la conception et la modélisation de la wake-up radio semi-active. Il peut y avoir des réveil manqués ou indésirés lors de la transmission, augmentant ainsi le temps de transmission et l'énergie moyenne par bit transmis. Pour tenir compte avec précision de ces effets, une modélisation exacte de la WUR est nécessaire. Nous avons détaillé le processus de simulation SPICE, le développement d'un modèle théorique ainsi que la conception et les mesures des prototypes pour la wake-up radio semi-active. Nous avons fourni une description complète de la wake-up radio, y compris ses parties analogiques et numériques.

Au Chapitre IV, nous nous sommes concentrés sur l'optimisation du système de wake-up radio semi-active Ce chapitre est divisé en trois parties, chacune abordant le processus d'optimisation sous différents angles. La première partie a comparé les performances de la wake-up radio semi-actif en utilisant deux approches d'intégration différentes: une fabrication

hétérogène, combinant PCB et CMOS intégré ; et une intégration PCB plus classique. La seconde partie a détaillé le processus de conception pour notre PCB à 4 couches et un résumé des règles de conception que nous avons suivies. La dernière partie de ce chapitre présente le développement d'un prototype à partir d'un module Arduino équipée d'une WUR à 4 couches optimisée. Nous avons détaillé tout le processus, de la conception à la réalisation.

Au Chapitre V, nous nous sommes concentrés sur l'utilisation du simulateur de réseau comme un outil efficace pour les réseaux de capteurs, en particulier dans le contexte des réseaux de capteurs sans fil (WSN) caractérisés par un grand nombre de nœuds et des ressources limitées. Cette démarche nous permet de surmonter les contraintes matérielles et de refléter les mesures du monde réel, réduisant ainsi les coûts expérimentaux et améliorant l'efficacité du développement. Ce chapitre a montré la valeur de l'utilisation du simulateur de réseau dans l'évaluation de la WUR et offre une comparaison des différents modèles et cadres.

En résumé, notre travail a fourni une analyse au niveau système de l'utilisation des WURs dans les WSNs, apportant un soutien pour les recherches futures dans ce domaine.

Mots clés

Wake-up radio; Réseaux de capteurs sans fil; Modélisation de circuits analogiques et RF; Conception de CI; Simulation de réseaux de capteurs

Résumé vulgarisé

L'utilisation de la wake-up radio (WUR) dans les applications de réseaux de capteurs est en croissance constante car elle permet de réduire considérablement la consommation d'énergie globale et d'augmenter la durée de vie de la batterie des capteurs. Le rôle de la WUR est de permettre à la radio principale de rester en mode veille le plus longtemps possible si aucune action n'est requise. Cependant, la plupart des publications discutent de la théorie, de la simulation SPICE, ou des mesures de WUR, pour une seule topologie de WUR à la fois. Dans cette thèse, nous comparons plusieurs topologies. Ce travail décrit en détail le processus de simulation des circuits, la modélisation théorique, la conception de PCB, les mesures et l'optimisation du prototype. De plus, cette étude propose des simulations de différents scénarios dans OMNeT++ pour examiner le comportement des nœuds dotés d'un WUR semi-actif sous différents modèles et frameworks. Nous proposerons une méthode de modélisation de la couche physique pour considérer les performances de la WUR et son impact sur la transmission de données, complémentaire à la modélisation de la couche MAC. En conclusion, cette thèse apporte une contribution au développement de la conception de la radio de réveil pour les applications de réseau de capteurs, fournissant une analyse au niveau du système qui soutient la poursuite des recherches dans ce domaine.

Abstract

The use of wake-up radio (WUR) in sensor network applications has been continuously growing, as it allows to significantly reduce the overall power consumption and increase the lifetime of sensors' battery. The role of the wake-up radio is to allow the main radio to remain in sleep mode as long as possible if no action is required.

However, most of the related work discusses the theory, SPICE simulation, or measurement of only one wake-up radio topology at a time. In this thesis, we comprehensively compare all methods. This work described in detail the whole process of WUR circuit simulation, theoretical modeling, PCB implementation, prototype testing and optimization. Furthermore, this study conducted simulations of different scenarios in OMNeT++ to investigate the behavior of nodes equipped with semi-active WUR under different models and frameworks. We proposed a physical layer modeling approach to consider the performance of the wake-up radio and its impact on data transmission, which is complementary to the MAC layer modeling.

Chapter II presented a comprehensive analysis and classification of the state-of-the-art for wake-up radio technology. We summarize the main characteristics of WUR based on our review of the literature, including type, technology, sensitivity, power consumption, frequency, modulation, latency, data rate, and addressability. And the analysis and initial simulation results were provided as a preliminary study for the design which can be easily adapted to the particular cases and prepared for the implementation and modeling of the device.

In Chapter III, we focused on the design and modeling of semi-active wake-up radio. There may be false wake-ups or missed wake-ups during the transmission, thus increasing the transmission time and the average energy per transmitted bit. To accurately account for these effects, an accurate modeling of the WUR is necessary. We gave the detailed process of SPICE simulation, development of a theoretical model, as well as the prototype design and measurement for a semi-active wake-up radio. we provided a comprehensive description of the wake-up radio, including its analog and digital parts.

In chapter IV, we concentrated on the optimization of the semi-active wake-up radio system. This chapter is partitioned into three sections that each approach the optimization process from different perspectives. The first part compared the performances of the semi-active wake-up radio using two different integration approaches: a heterogeneous fabrication, combining PCB and integrated CMOS; and a more classical PCB integration. The second part provided the design process for our 4-layer PCB. and a summary of the design rules that we followed during this process. The final part of this chapter presents the development of a prototype of an Arduino

shield equipped with an optimized 4-layer WUR. And we detailed the entire process from shield design to realization.

In chapter V, we focused on using network simulator as an effective tool in the sensor networks, particularly within the context of wireless sensor networks (WSNs) characterized by a great number of nodes and limited resources. This approach allows us to overcome material constraints and reflect real-world measurements, thus reducing experimental costs and improving development efficiency. This chapter highlights the value of using network simulator in WUR assessment and provides a comparison of different models and framework, providing a basis for future research on WUR in WSN.

In summary, our work provided a system-level analysis of the use of wake-up radios in wireless sensor networks, providing support for further research in this field.

Key words

Wake-up radio; Wireless sensor networks; Analog and RF circuit modeling; IC design; Sensor network simulation.

Vulgarized abstract

The use of wake-up radio (WUR) in sensor network applications has been continuously growing, as it allows to significantly reduce the overall power consumption and increase the lifetime of sensors' battery. The role of the wake-up radio is to allow the main radio to remain in sleep mode as long as possible if no action is required. However, most of related works discuss theory, SPICE simulation, or measurements, for only one WUR topology at a time. In this thesis, we compare several topologies. This work describes in detail the whole process of WUR circuit simulation, theoretical modeling, PCB implementation, prototype testing and optimization. Furthermore, this study conduct simulations of different scenarios in OMNeT++ to investigate the behavior of nodes equipped with semi-active WUR under different models and frameworks. We propose a physical layer modeling approach to consider the performance of the wake-up radio and its impact on data transmission, which is complementary to the MAC layer modeling. In summary, this thesis gives a contribution to the development of wake-up radio design for sensor network applications, providing a system-level analysis that supports further research in this field.

Table of contents

Abbreviations

Ack	Acknowledge
ASK	Amplitude Shift Keying
AWGN	Additive White Gaussian Noise
CDF	Cumulative Distribution Function
CMOS	Complementary Metal-Oxide-Semiconductor
D_d	Data Transmit Range
D_{wu}	Wake-Up Range
ED	Envelope Detector
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EPB	Energy Per Bit
FSK	Frequency Shift Keying
MCU	Microcontroller Unit
OOK	On-Off Keying
OSI	Open Systems Interconnection
PCE	Power Conversion Efficiency
RFID	Radio Frequency Identification
SNR	Signal to Noise Ratio
SR	Slew Rate
ULP MCU	Ultra-Low Power Microcontroller
V_{OS}	Offset Voltage
V_{ov}	Overdrive Voltage
V_{th}	Threshold Voltage
WUP	Wake-Up Packet
WUR	Wake-Up Radio
WSN	Wireless Sensors Network

Publications

International Conferences

- R. Ding and W. Tatinian, "Design and modeling of heterogeneous semi-active wake-up radio for sensor network applications," 2023 21st IEEE Interregional NEWCAS Conference (NEWCAS), Edinburgh, United Kingdom, 2023.

- R. Ding and W. Tatinian, "Hierarchical Modeling of 868MHz Wake-up Radio in OMNeT++," 2022 37th Conference on Design of Circuits and Integrated Systems (DCIS), Pamplona, Spain, 2022.

- R. Ding and W. Tatinian, "Contribution to wake-up radio design for wireless sensor network." 2021 36th Conference on Design of Circuits and Integrated Systems (DCIS). Vila do Conde, Portugal, 2021.

National Conferences

- R. Ding and W. Tatinian, "Electrical modeling of wake-up radio for false wake-up prediction in sensor networks." 16ème Colloque du GDR SoC2. 2022.

- R. Ding and W. Tatinian, "Contribution to wake-up radio design for wireless sensor network." 1er Workshop CSC-Polytech, Paris, 2022.

- R. Ding and W. Tatinian, "Study of rectenna topologies of semi-active wake-up radio applications." 15ème Colloque National du GDR SoC2, 2021.

Chapter I: General introduction

I.1 Background

Over the past decades, wireless sensor networks (WSNs) have been widely used in various fields, such as military, industrial, environmental monitoring and marine exploration applications [1]. Wireless sensor networks consist of a dense deployment of sensor nodes, equipped with the capability of wireless communication and monitoring and analyzing various environmental or physical conditions [2].

With the growing number of communicating objects and the energy constraints of wireless sensor nodes, their limited battery still restricts the development of large-scale network application. Since the radio receiver is one of the components with the highest power consumption, aside from the transmitter, it may cause the problem of power wastage in the receiver's idle listening. One solution is to turn off the main radio and introduce a wake-up radio (WUR). This is a small chip that requests a very low power to stay on for a continuous idle listening of the channel and turn on the main radio only when needed.

In the structure of wake-up radio's strategy, the main radio remains in deep standby or off mode until the request is received. Instead, the wake-up radio is always on to receive the messages. When the transmission part has a data packet to send, it will send a wake-up packet first. Then, the wake-up radio detects the wake-up message and generates an interrupt to the microcontroller unit (MCU) to switch it from standby mode to active mode. Next, the main radio will be turned on to exchange data packets in a conventional manner. The structure of this receiving part is shown in Figure 1.1:

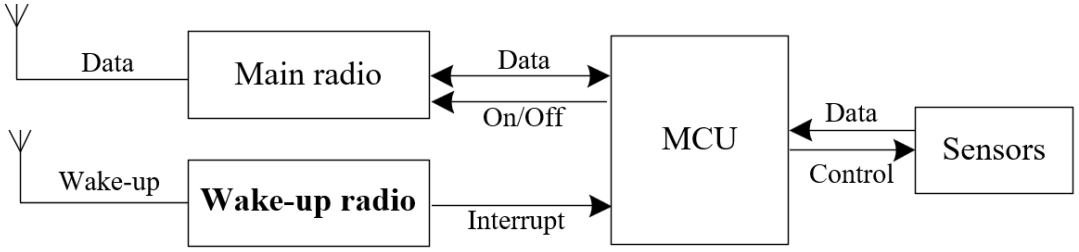

Figure 1.1 Principal block diagram of wake-up radio-based receiver

I.2 Motivation and objective

Although a lot of works have published on this topic, most of them tend to study individual aspects like theory, SPICE simulation, or measurements. In this work, we provide a complete discussion, addressing all these areas comprehensively.

Our primary attention is on discrete semi-active wake-up radio. While most research usually discusses one WUR topology at a time, we compare multiple topologies in detail, covering from theory and SPICE simulations to measuring prototypes.

Moreover, to estimate the quality of the communication, it is particularly important to account for the probability of false wake-up or missed wake-up. Because it will not only affect the function of a single node, but also increase the transmission time and the average energy of each transmitted bit, thus affecting the entire data transmission. To accurately account for these effects, accurate modeling of WUR is required.

Finally, we implement some wake-up radio models in a sensor network simulator and run some scenarios with these new models to see how the wake-up radio behaves in practice, by comparing between theory, SPICE simulations and measurements.

In all these works, we will highlight our contributions to the field of wake-up radio technology by linking our findings to the existing state-of-the-art.

I.3 Thesis work

The adopted methodology begins with electrical simulations on the WUR to preliminarily assess its potential performance. Subsequently, we proceed on theoretical modeling. The most challenging task in the theoretical study is to establish a model for nonlinear components, especially the diodes of the rectifier, as the model must maintain accuracy across a dynamic range of several tens of dB. We then assemble and test the circuits, comparing the results with the simulation. Afterwards, we optimize the WUR, including the layout and routing of the prototype to enhance its robustness. Furthermore, we also develop a node that combines WUR with other key modules, allowing us to evaluate the performance of WUR-based nodes in real-world situations. And then, the models are updated based on actual measurements and compared

to theoretical predictions. In the end, we can perform the simulations of these models in a network simulator OMNeT++.

This thesis describes in detail the whole process of WUR circuit simulation, theoretical modeling, PCB implementation, prototype testing and optimization. Additionally, this study conducts simulations of different scenarios in OMNeT++ to investigate the behavior of nodes equipped with semi-active WUR under different models and frameworks. We propose a physical layer modeling approach to consider the performance of the wake-up radio and its impact on data transmission, which is complementary to the MAC layer modeling.

The rest of manuscript is organized as follows: Chapter II presents a comprehensive analysis and classification of the state-of-the-art for wake-up radio technology. In Chapter III, we focus on the design and modeling of semi-active wake-up radio. In chapter IV, we concentrate on the optimization of the semi-active wake-up radio system. Chapter V highlights the value of using network simulator, providing a comparison of different models of WUR and framework. Finally, Chapter VI gives a general conclusion and some perspectives to end this manuscript.

I.4 Reference

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[2] U. M. Colesanti, C. Crociani, and A. Vitaletti, “On the accuracy of omnet++ in the wireless sensornetworks domain: simulation vs. testbed,” in *Proceedings of the 4th ACM workshop on Performance evaluation of wireless ad hoc, sensor, and ubiquitous networks*, 2007, pp. 25–31.

Chapter II: State-of-the-art of wake-up radio and preliminary study of semi-active wake-up radio

II.1 Introduction

This chapter presents a comprehensive analysis and classification of the state-of-the-art wake-up radio (WUR) technology. The characteristics of each type of WUR are discussed in detail. We then choose to focus on the semi-active wake-up radio and analyze the key components of the circuit. Furthermore, we divide the semi-active WUR circuit into the analog part and the digital part, and study them separately. Performances of semi-active WUR are simulated and presented.

The remainder of this chapter is organized as follows: Section II.2 discusses the state-of-the-art of wake-up radio. In Section II.3, we study the rectifiers in semi-active wake-up radios, including how to choose nonlinear components and rectifier topologies. And then, preliminary simulations and analyzes based on discrete components of semi-active wake-up radio are given in Sections II.4 and 5. Finally, Section II.7 concludes the chapter.

II.2 State-of-the-art of wake-up radio

Numerous studies are conducted on the use of wake-up radios in wireless sensor networks (WSNs) to reduce power consumption. This section presents a state-of-the-art review of WUR literature. By the power supply method, it can be classified into three groups of wake-up radio circuits: fully-passive, fully-active, and semi-active. To ensure clarity in the discussions, we will divide each type of WUR into three categories based on technology: prototypes constructed using off-the-shelf discrete components, implementations with complementary metal-oxide-semiconductor (CMOS) technology for integrated circuits, and those based on radio-frequency identification (RFID) technology.

The use of off-the-shelf discrete components simplifies the rapid prototyping of WUR.

CMOS implementations integrate all components directly onto silicon, resulting in more compact circuits and better performance for the same function. And RFID technology is another option. These WUR can draw power from the electromagnetic field generated by the reader device, which are mainly used in passive WUR. And then, we also analyze the selection of RF modulation and carrier frequency in WUR. The state-of-the-art of wake-up radio is investigated by studying the following main characteristics:

Sensitivity: it's the minimum signal strength that the wake-up radio can successfully detect and process while maintaining the functionality. This determines the transmit distance of the wake-up radio at the same transmission power and frequency.

Power consumption: it's the amount of electrical energy consumed by the wake-up radio. In battery-powered systems, it directly affects the battery life.

Frequency: generally, it refers to the carrier frequency of the wake-up signal.

Modulation: it's the process of manipulating the wake-up signal and combining it with a carrier to make it suitable for channel transmission. Typically, the information of the signal source contains a DC component and a lower frequency component, which is referred to as a baseband signal.

Latency: it generally refers to the time it takes between when the transmitter sends a wake-up signal and when the main radio wakes up.

Data rate: it represents the quantity of bits transmitted through a communication channel per unit time, generally expressed in bits per second (bps), It's influenced by factors such as the modulation, baseband frequency, and signal-to-noise ratio, etc. [1]. High data rate can reduce wake-up latency, but they may lead to decreased sensitivity. On the other hand, at lower data rate, the transmitter needs to spend more time on sending, resulting in higher power consumption on the transmitting side [2].

Addressability: it's the ability to selectively activate nodes in the network to achieve more efficient communication [1]. By assigning a unique address to the main radio in each node, unnecessary activation of other nodes can be prevented, to save energy. This requires the wake-up radio to decode the received wake-up signal to determine if the signal is intended for the main radio in its node.

Our review of the state-of-the-art is based on the main characteristics mentioned above. If

certain characteristics are not discussed, it may be due to their lesser significance in the respective research articles, or the authors didn't mention them.

II.2.2 Fully-passive wake-up radio

Fully-passive wake-up radio circuits do not necessitate a power supply. Although the WUR circuit requires power to operate, it does not require external battery power. This can be achieved by harvesting energy from the incoming RF signal.

Energy harvesting circuits can capture energy from wind, heat, light or electromagnetic radiation in the environment and convert it into electrical energy. This energy can either be used to power comparators and ultra-low-power micro-controllers, or be stored in capacitors. Better energy harvesting efficiency will lead to better performance of fully-passive wake-up radios [1]. However, we need to attach more hardware to the WUR to provide this functionality. This increases the size and complexity of the circuit. In addition, the process of energy recovery leads to a delay in main radio's wake-up due to the need for sufficient time to accumulate energy. Therefore, the transmitter may transmit the wake-up signal longer, which consumes more energy [4].

Passive wake-up radio is mainly made using discrete Schottky diodes, RFID or integrated CMOS technologies. CMOS technology is more popular due to its low power consumption and low threshold voltage in ICs. RFID is also widely used because it already has energy harvesting capabilities, which reduces development time.

Discrete

The first proof of concept for WUR was presented by Gu et al. (2005) [5]. They proposed the structure of a Basic Radio-Triggered Circuit shown in Figure 2.1, which was an entirely passive circuit that was simulated using SPICE. The circuit operated at a frequency of 433MHz and achieved a transmission distance of 3m at a transmit power of +10dBm with a latency of 5ms. To evaluate the application lifetime of the sensor network, the authors used the NS-2 network simulator. Their findings showed that WUR can save up to 98% of energy for systems without power management. The authors also proposed structures with longer transmission distances, such as energy harvesting circuits, which could store energy from the radio signal

and use it later. However, this required adding some delay. Furthermore, a multi-frequency technology called radio-triggered identification (RTID) was presented, which provided better selectivity in energy management services.

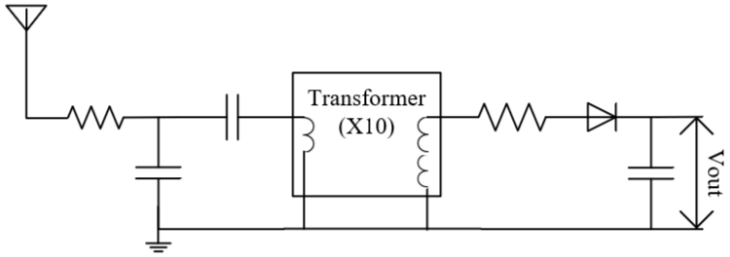

Figure 2.1 Radio trigger circuit with step-up transformer

CMOS

Chung et al. (2011) [6] proposed a passive integrated WUR fabricated using the 0.18μm CMOS process. The device consisted of a RF front-end and a 512-bit digital baseband with non-volatile memory. The RF front end comprised of a voltage multiplier (VM), voltage limiter, demodulator, modulator, ring oscillator, power-on reset (POR), and bias circuit. The voltage multiplier operated by harvesting RF energy. In read mode, the device achieved a sensitivity of −17dBm with a power consumption of 2.64μW. The oscillator frequency was measured to be approximately 2.07MHz, and the power-up time was 100μs.

Kamalinejad et al. (2014) [7] designed and simulated a WUR circuit using a 0.13μm CMOS technology. The circuit consisted of a rectifier, a bandgap reference generator, and a low power comparator. In the rectifier, the authors developed a bias scheme to increase the gate voltage of the switching transistor. They employed a quasi-floating gate architecture with the gate of the switching transistor connected to a boosted voltage level to achieve high power conversion efficiency (PCE) at small input levels. The rectifier rectified the differential RF and detected the envelope of the OOK wake-up signal. Then the rectified DC voltage was utilized to power the comparator and the bandgap reference generator. The block diagram is shown in Figure 2.2. Simulation results indicated a sensitivity of −33dBm at a wake-up signal of 100kbps. However, the authors only did the simulation, and thus further experimental validation was required.

Zgaren et al. (2015) [8] implemented a WUR in the 0.13μm CMOS process. This WUR included an antenna shared with the main transceiver, an RF-DC rectifier, and a comparator

with a voltage reference. The RF-DC rectifier was used to generate the envelope of the OOK signal, which was converted into a DC voltage to power the comparator. The WUR achieved a sensitivity of −53dBm with a data rate of 100kbps and a power dissipation of 0.2μW. There are other studies that also investigated CMOS technology, as reported in [9-11].

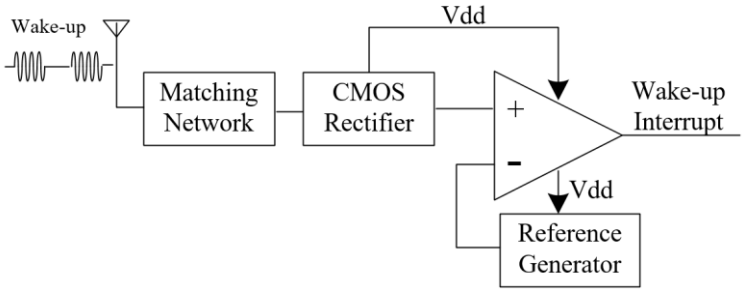

Figure 2.2 Wake-up radio block diagram

RFID

RFID technology is one of the possible approaches to achieve passive WUR, since it has a well-defined communication protocol and uses energy harvesting to enable this communication [12].

Wireless Identification and Sensing Platform (WISP) was the first fully programmable platform without external power supply that used power transmitted from a long range ultra-high frequency (UHF) RFID reader. It included a 16-bit micro-controller with an analog-to-digital converter, as shown in Figure 2.3. The center frequency was 915MHz. Experimental tests presented that the distance could be up to 4.5m with a transmit power equal to +30dBm. However, this also meant that the sensitivity was only −6.7dBm [13].

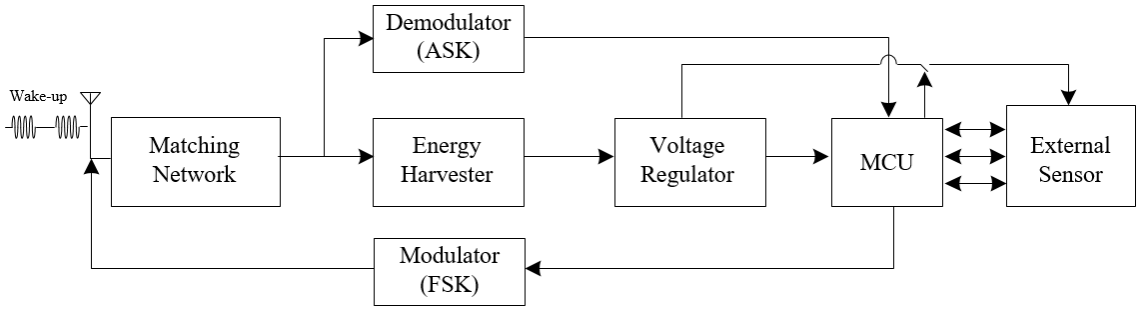

Figure 2.3 WISP Platform Block Diagram

Ba et al. (2013) [14] introduced a new passive WUR called WISP-Mote, which used passive programmable RFID tags as wake-up radios for traditional sensor nodes. To extend the wake-up range, they disabled WISP-reader communication and eliminated all other

computational loads in the WISP MCU. Then, they characterized the WISP-Mote with field tests in different operating environments. The results showed that the WISP-Mote had a relatively stable wake-up range of up to 4.5m* in an open environment. In a noisy environment, the probability of waking up reaches 80% when the communication distance is 3m*. They also tested with duty cycling approaches, where a timer was set and the firing of the timer wakes up the node. They found that wake-up radio sensor networks have great potential over duty cycling for energy efficiency, while providing similar latency and packet delivery performance [15].

In [12], Chen et al. (2015) also proposed the energy harvester WISP-Mote (EH-WISP-Mote), which paralleled the WISP-mote circuit with the energy harvesting circuit to provide additional energy harvesting capability to extend the wake-up range, as shown in Figure 2.4. During testing, they found that the wake-up range reaches 5.2m* and the total wake-up area was increased by 30%.

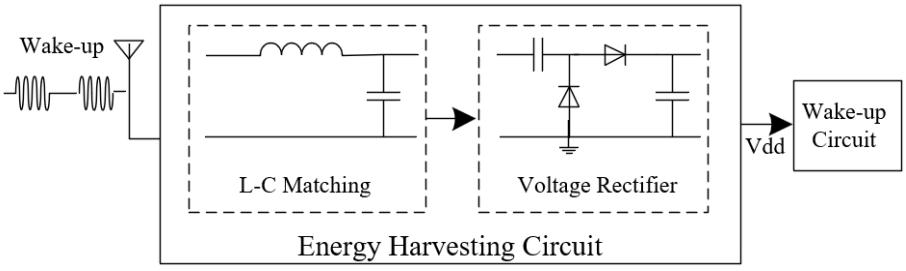

Figure 2.4 Energy harvesting circuit in EH-WISP-Mote

The Range EnhAnCing energy Harvester-Mote (REACH-Mote) was composed of an energy harvesting circuit and an ultra-low power wake-up circuit (pulse generator) presented in Figure 2.5, and had a communication range of up to 11.3m* on broadcast-based wake-ups. The energy harvesting module was improved by increasing the number of energy harvesters and connecting them in series to increase the output voltage. A voltage regulator and a front control switch using the Tmote Sky WSN platform were added to change the supply voltage. By sleeping on low voltage power, the Tmote Sky had a lower trigger wake-up requirement. When the Tmote Sky woke up, the power returned to 3V. The improved prototype, named REACH2-Mote, achieved a wake-up range of 13.4m [3], [12].

De Donno et al. (2014) [16] introduced two types of fully-passive 868MHz WURs, called WWU (Write Wake Up) and MWU (Multicast Wake Up), using UHF RFID tags. The WWU

*The authors didn't mention the value of transmit power.

was ID-based, had a transmission range of up to 11m with a transmission power of +30dBm, and a delay of 258ms. The MWU was diffusion-based, composed of a single-stage full-wave rectifier and a DC-DC charge pump. It had a transmission range of 10m, but a smaller delay of 30ms [17].

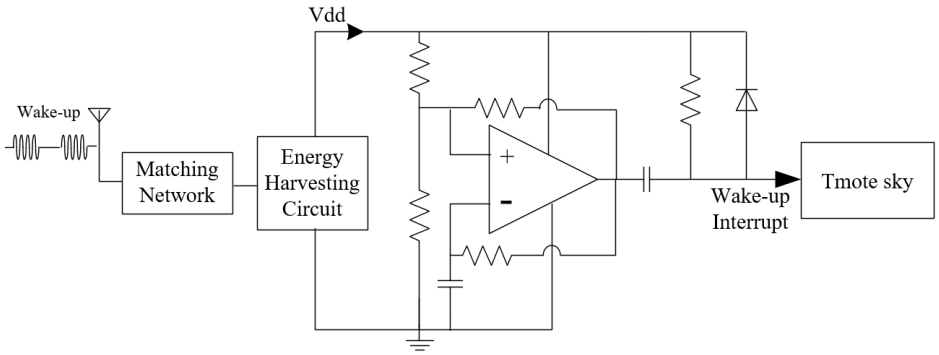

Figure 2.5 Main components of the REACH-Mote system

II.2.3 Fully-active wake-up radio

Unlike fully-passive WUR, which doesn't rely on a power supply, a fully-active WUR is powered by an external power source to operate and usually listens for signals in an always-on manner. It typically consumes more power. However, it can offer faster response times and better performance in certain situations, especially when it comes to longer communication ranges and complex signal processing. Based on the results of survey, it can be concluded that CMOS technology is the most commonly utilized technology for fully-active wake-up radio, due to its low power consumption and high level of integration.

Discrete

Petroli et al. (2014) [18] presented a novel topology that operated in the 2.4GHz ISM band and complied to the IEEE 802.15.4 standard. The receiver's front end was composed of an antenna, low noise amplifier, power divider, and filters, as illustrated in Figure 2.6. The LNA and filter were designed using integrated technology. A prototype was fabricated using off-the-shelf methods to validate the feasibility of the proposed design. The prototype hardware considered four different channels, allowing node addressing. However, the test results of the prototype have not been published yet. The authors also introduced two protocols, FLOOD-WUP and GREEN-WUP, which employed selective wake-up and dynamic address allocation

to enhance system performance. FLOOD-WUP was a flooding wake-up protocol that achieves better latency vs. energy consumption performance, while GREEN-WUP was a hop-count-based converge casting wake-up protocol. Compared to traditional WSN protocols, the new approach demonstrated superior performance in terms of addressing delay and power consumption.

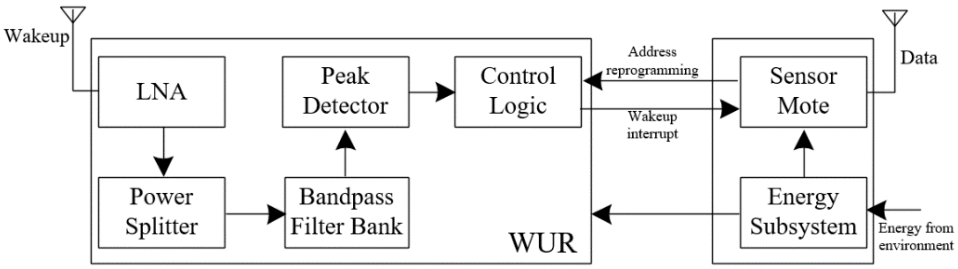

Figure 2.6 Block diagram of WUR with 4 channels for addressing

CMOS

CMOS fully-active wake-up radio can be broadly categorized into two groups based on the presence of mixers or oscillators. In cases where these high-power consumption components are present, the sensitivity of WUR is enhanced at the cost of increased power consumption. Conversely, with the envelope detector (ED), power consumption in the nanowatt range can be achieved.

Frequency-mixing topology

Many frequency-mixing topology proposed in active circuits use heterodyne methods, as showed in Figure 2.7. The principle is to mix the received RF signal with the local oscillator circuit to generate an intermediate frequency (IF) signal. The IF signal is then amplified and detected to restore the original signal. Milosiu et al. (2013) achieved a 7μW 2.4GHz wake-up radio with −80dBm sensitivity in [19]. And in [20]**,** Liu et al. (2020) proposed a WUR which incorporated an inductor-capacitor voltage-controlled oscillator (LC-VCO) and a frequency locked loop (FLL) achieved a sensitivity of −92.6dBm, but also consumed a very high power of 495μW.

Additionally, super-regenerative amplifiers are commonly used in WUR systems due to their lower power consumption and better sensitivity. When the wake-up receiver is in standby mode, the super-regenerative amplifier continuously generates and attenuates an oscillating

signal, thereby facilitating the sensitive detection of radio frequency signals. Upon receiving the wake-up signal, the super-regenerative amplifier amplifies the signal and outputs it to the subsequent circuit to initiate the main chip of the system. The WUR in [21] proposed by Cho et al. (2015) achieved a power consumption of 42.5μW at data rate of 100kbps and the sensitivity reaches −72dBm. Based on this super-regenerative architecture, Petäjäjärvi et al. (2016) in [22] proposed a WUR using Hybrid Broadcast Channel (HBC). Their approach used self-quenching and relaxed synchronization at 1.25kbps, achieving −97dBm sensitivity while consuming 40μW.

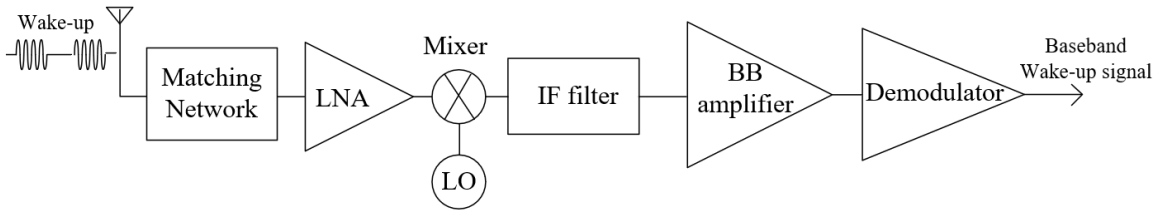

Figure 2.7 Block diagram of heterodyne WUR

Furthermore, for frequency-mixing topology, power consumption is usually limited by the high power of the LO. low power high sensitivity uncertain IF Architecture is another implementation for forming a wake-up receiver: it uses a low power ring oscillator to down convert the RF signal to the IF frequency, as shown in Figure 2.8. Since the signal is amplified at the IF frequency, its consumption is lower.

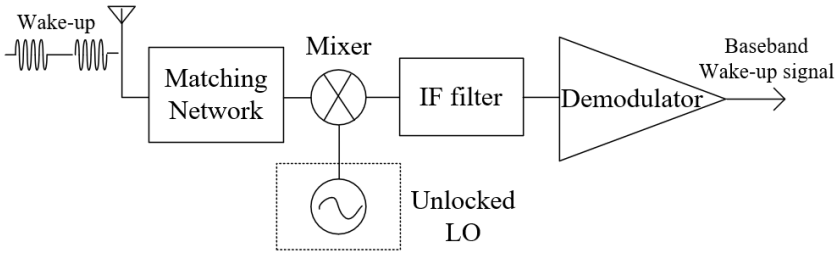

Figure 2.8 Block diagram of uncertain IF WUR

Pletcher et al. (2008) [23] introduced a comprehensive implementation of WUR using an uncertain-IF architecture. This design approach relaxed the requirements for phase noise and frequency accuracy, thereby enabling the utilization of a free-running ring oscillator for LO generation and eliminating the need for a PLL. The WUR comprised a bulk acoustic wave (BAW) resonator for network impedance matching, a front-end IF amplifier for radio frequency

(RF) signal conditioning and amplification, and an envelope detector. The implemented WUR achieves a sensitivity of −72dBm at a bit error rate of 100kbps while consuming 52μW of power [24].

RFED-based technology

The radio frequency envelope detection (RFED) architecture has been the most widely adopted approach for developing a WUR [22]. It's a simple and low-cost solution that is highly sensitive to weak signals, making it suitable for low-power, low-data-rate wake-up radio applications.

In [25], a WUR utilizing ED technology was presented by Wang et al. (2018), boasting a sensitivity of −69dBm and a remarkably low power consumption of 4.5nW. To achieve reasonable immunity to interference, a combination of techniques was employed, including low carrier frequency operation and reduced WUR data rates, as well as the implementation of passive, high-Q transformers/filters to achieve a 25dB gain passively. These measures ensured effective operation in the presence of interfering signals. Moreover, a sub-μW WUR was introduced by Mangal et al. (2019) in [26] with a sensitivity of −79dBm. This achievement was made possible by utilizing multi-stage passive energy detectors and a high-Q input matching network. However, it should be noted that the implementation of such techniques came at the cost of relaxing latency constraints. Other active WUR that were based on ED technology can be found in [27-30].

RFID

Jurdak et al. (2010) [31] provided comprehensive information regarding WUR designs utilizing commercially available active RFID tags. The analysis confirmed that RFIDImpulse, equipped with Adaptive Low Power Mode, consumed approximately 20 times less energy, compared to IEEE 802.15.4 in low traffic scenarios. In terms of operation, when a node transmitter intended to send a packet, it activated the RFID reader to trigger the corresponding RFID tag. The signal received by the neighbouring receiver generates a wake-up interrupt to the local MCU, which subsequently awakened the radio and prepared to receive incoming packets. However, it was worth noting that this receiver didn't use addressing to selectively awaken sensor nodes. The authors then provided simulations and comparisons of binary tree

scenarios for B-MAC, IEEE 802.15.4, and RFID Impulse's WUR designs. The results showed that RFIDImpulse had the lowest overall energy consumption, which was about 20 times lower than IEEE 802.15.4 and 13 times lower than B-MAC [32].

II.2.4 Semi-active wake-up radio

The majority of proposed WUR design approaches are semi-active, resulting in compromised consumption and sensitivity [33]. In such approaches, only a part of components necessitates a continuous power supply from external sources. The prevalent technique involves implementing an envelope detector utilizing passive components such as Schottky diodes or MOSFETs. Then, active components such as correlators and comparators are utilized to generate interrupts to the microcontroller unit for addressing, as presented in Figure 2.9. This approach is considered the most common among the various WUR design methods available.

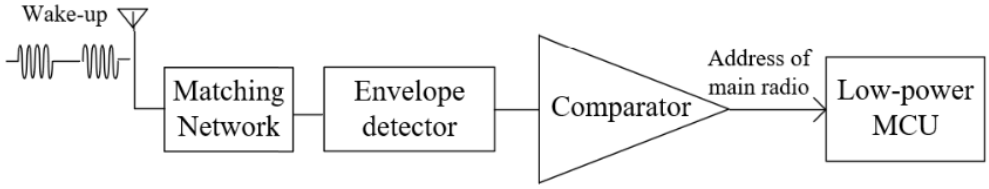

Figure 2.9 Block diagram of most common used semi-active WUR

Discrete

The first operational WUR prototype was developed by Van der Doorn et al. (2009) [34]. In this study, the author proposed the integration of a low-power MCU to facilitate the exposure and decoding of wake-up signal and to notify the AT-mega128L processor through an interrupt. The power consumption of WUR was 819μW in listen mode with a sensitivity of −28dBm. Despite the short communication distance and high-power consumption, the author has sorted out various requirements such as low cost, low interference, 10-meter range, and low delay that WUR should meet through prototype testing. This achievement inspired follow-up research in this field.

Magno et al. (2016) [33] proposed a low-sensitivity low-power wake-up radio, which employed OOK modulation and was composed of four main building blocks: matching network, passive envelope detector, comparator, and preamble detector. Upon reception of a valid wake-up address, the output of the preamble detector interrupts a low-power MCU responsible for

address matching and triggering the main sensor node. This WUR outperformed previous techniques, providing a flexible solution with low power consumption (1.2μW), high sensitivity (−55dBm) and addressability. Experimental results demonstrated that addressing could reduce false/missed wake-ups. Simulation of real-world scenarios comparisons with other WUR solutions and duty-cycling protocols were also done in this paper.

Recently, Kazdaridis et al. (2021) proposed a method for enhancing the sensitivity of the WUR based on the circuit in [33]. This method was capable of significantly improving the sensitivity of the WUR to a level lower than −70dBm, while keeping the power consumption at a similar level. The authors noted that in all previously published WUR, the signal from the envelope detector was directly fed to the comparator, which meant that the sensitivity of the WUR was dependent on the characteristics of the comparator used. To address this issue, the authors proposed inserting an operational amplifier between the envelope detector and the comparator. This arrangement amplified the low-level signal DC signal, which was then further amplified by the comparator. The consumption of the operational amplifier was 450nA. And then, the authors chose a high input offset voltage (V_{OS}) but low-consumption (110nA) comparator, as the proposed circuit was no longer dependent on the V_{OS} of the comparator. However, this WUR introduced an external fixed reference as the negative input of the comparator, which may not be optimal from a convenience standpoint [35].

In addition, instead of relying on a low-power MCU for decoding, Ammar et al. (2015) [36] proposed a WUR that used an address decoder based on flip-flops and a low-power clock generator. The proposed RF front-end WUR employed passive circuit elements, which resulted in no static current consumption. In active mode, their serial code detector, which served as an address decoder, dissipated 13.41μW. Although the WUR based on flip-flops consumed more power, it could significantly reduce latency to only 80μs. Based on this, Khodr et al. (2017) [37] proposed an enhanced address decoder design. Their approach involved using XNOR gates with open drain output and replacing all AND gates with a single pull-up resistor, which could reduce power consumption and circuit complexity.

AS393x

There are many proposals in the literature where authors employed a commercially available WUR chip for address decoding in their prototypes. One such chip is the AS393x

series from Austria Microsystems, which is a 3D low-power, low-frequency Amplitude Shift Keying (ASK) WUR capable of generating a wake-up interrupt upon detecting a signal at a carrier frequency between 15-150KHz. One of its unique features is its integrated correlator, which allows for the implementation of a 16-bit or 32-bit wake-up address decoding scheme, making it a pattern recognizer. The AS393x WUR boasts a maximum sensitivity of −69 dBm, with current consumption varying from 1.7μA to 12μA. Its capabilities make it an attractive option for designers looking for a WUR solution.

Gamm et al. (2010) [38] introduced the first in-band sub-carrier modulation WUR system based on AS3932, representing the first complete WUR transceiver. In this system, the main radio also functioned as a transmitter to generate the wake-up signal. The WUR had an active power consumption of 7.8μW, while achieving a maximum sensitivity of −52dBm with a data rate of 250kbps. Figure 2.10 shows the block diagram of the proposed senor node. The AS3932 extracted the 125KHz signal from the 868MHz wake-up signal and decoded the original data for address comparison. Once the address was matched, the main node was triggered, and an antenna switch was used to bypass the WUR, allowing data exchange to occur via the main radio.

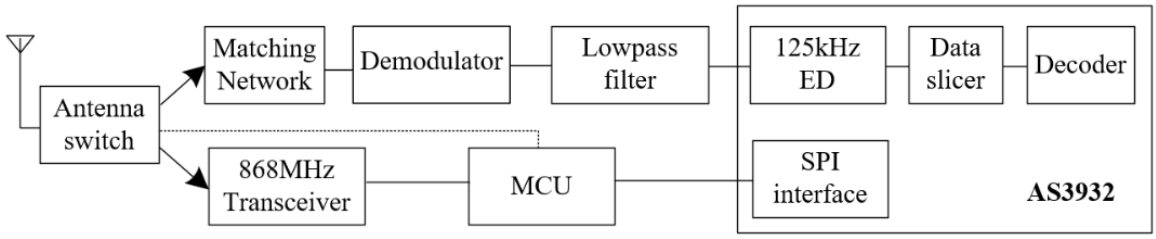

Figure 2.10 Block diagram of the proposed senor node in [38]

Cabarcas et al. (2020) [39] presented an application of WUR, which supported a dual-stack architecture designed to operate in the 915MHz and 2.4GHz ISM bands for the WUR and main radio, respectively. Their approach featured a passive demodulator, combining with AS3933 chip as the WUR. The overall architecture is presented in Figure 2.11.

Oller et al. (2013) [40] compared a SuA-WUR (not embedded with AS393x) and AS393x-based WUR. They concluded that SuA-WUR was a more energy-saving and cost-effective alternative based on AS3933. SuA-WUR had lower power consumption and was not so complicated in hardware components. Although it currently didn’t support the addressing

function, it could use alternative energy-saving addressing methods. They also looked at several criteria for systems from the perspective of WUR. The criteria studied include the type of antenna, the use of noise filters, and the number of rectifier stages and impedance matching inductors. Measurements were performed analysing the effect of receiver height and distance from the location of the transmitter, the material composition of the WUR, the output power of the transmitter, and the type of environment (inside or outside).

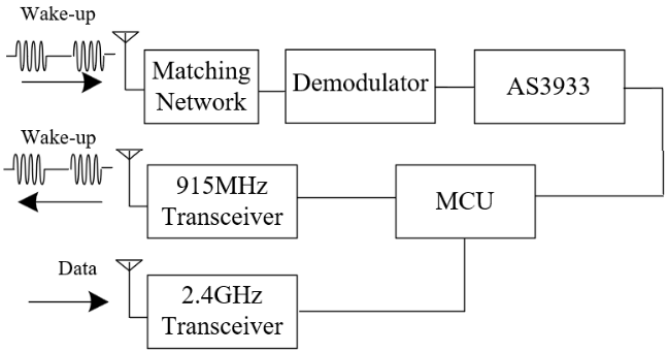

Figure 2.11 Block diagram of the node combining with AS3933 chip

CMOS

The first complete implementation of a WUR with a power consumption of around 10μW was presented by Durante et al. (2009) The solution included on-chip MOS detector, programmable amplifiers, and integrators. For reasons of flexibility in implementation, an FPGA was dedicated to digital decoding. Its static power consumption was 12.5μW and the sensitivity/data rate was −57dBm/100kbps [41].

Ishige et al. (2016) [42] proposed a WUR which comprised a LC matching network, a 30-stage CMOS voltage multiplier, and a Schmitt trigger comparator. The voltage multiplier was specifically designed for 65 nm SOTB (Silicon On Thin Buried Oxide) technology to enable low voltage operation. Simulation results demonstrated that the WUR achieved a sensitivity of −30 dBm, and the comparator had a power consumption of 6.7nW. However, it should be noted that an external reference voltage was used and only simulation results were available.

Moody et al. (2019) [43] compared the performance of passive and active CMOS detectors in WUR by modeling them. They analyzed the detectors' sensitivity and power consumption, taking into account the lack of RF gain and the noise produced by the detectors. Based on their findings, they determined that the choice between the two types of detectors depended on the

IF bandwidth and DC power requirements of the application. Passive detectors were superior for low bias currents (<100nA) due to their better noise sensitivity and lower power consumption, whereas active detectors were more suitable for higher IF bandwidths and dc powers due to their lower thermal noise and decreased overall contribution of noise.

Mangal et al. (2019) [44] proposed a WUR which was fabricated in 0.13μm CMOS and operated from a 0.5V supply. The sensitivity was −56.4dBm with a power consumption of 222nW. A 10 stages voltage multiplying self-mixer using MOS transistors in weak inversion consumed 2.7nW and offers multi-stage conversion gain at baseband. The block diagram is shown in the Figure 2.12. The authors point out that the sensitivity of the envelope detector (ED) is affected by flicker noise and that it has a delay of more than 10ms due to its low bandwidth. Selectivity to modulated interferers is limited by the RF matching network. Compared with ED, the self-mixer technique offers better sensitivity and shorter delay, according to the authors.

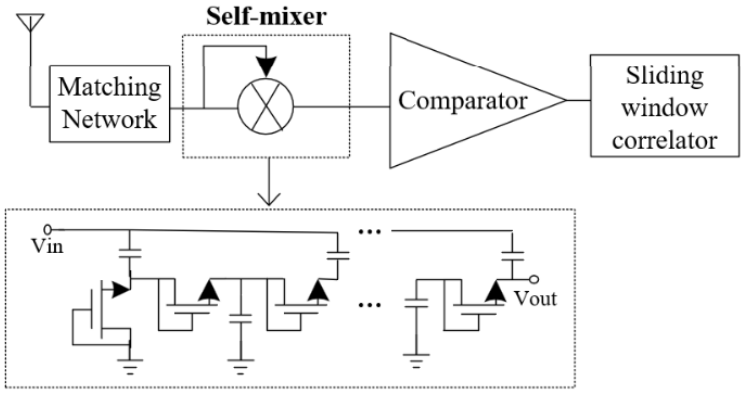

Figure 2.12 block diagram of WUR based on self-mixer

Galante-Sempere et al. (2022) [45] compared the performance of an off-chip RFED WUR implemented with AS3933 and a fully integrated CMOS WUR. The off-chip WUR showed higher selectivity due to a high-Q input filter, while the fully integrated WUR achieved a sensitivity of −63.2dBm with low power consumption (6.77μW). The circuit included a single MOSFET-based envelope detector with an integrated transformer to enhance sensitivity while keeping power consumption low. However, this design resulted in a larger circuit area. The study highlights the choice of implementation depends on specific requirements such as selectivity, sensitivity, power consumption, and circuit area.

RFID

Malinowski et al. (2007) [46] used a 300MHz RFID WUR to activate CargoNet, which was an ultra-low-power WSN mote based on the MSP430. The RFID WUR circuit was composed of an LC tank that amplified the signal received by the antenna and a Schottky diode that functioned as an envelope detector. Additionally, an operational amplifier provided voltage gain. The sensitivity was −65dBm with a power consumption of 2.8μW.

Figure 2.13 presents the sensitivity as a function of power consumption for the WUR related work published in recent years. Each dot represents a study, with the majority of them being concentrated within the encircled region. A linear trend indicates a correlation between sensitivity and power consumption. In general, higher power consumption results in better sensitivity. In this thesis, our WUR achieves a sensitivity of −47dBm at a power consumption of 1.7μW, shown in red on the figure. Its sensitivity and power consumption relationship are within the typical range, compared with the existing literature. It's worth to note that some points lie outside the circle, with those in the upper often representing earlier publications. Additionally, the two reference papers to the left of the circle achieved high sensitivity with very low power consumption. However, in practice, sensitivity is influenced by various factors, such as the technology used, component selection, implementation complexity, and other characteristics like modulation, frequency, and data rate, etc. Case-specific analysis is necessary to fully understand each situation.

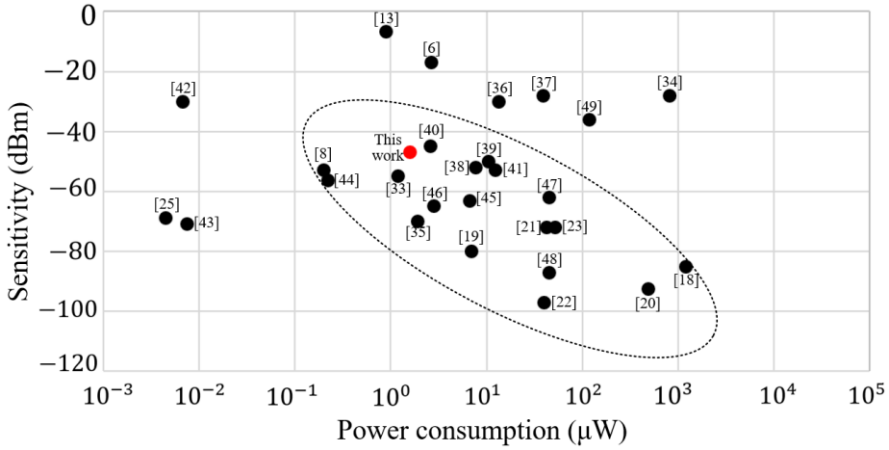

Figure 2.13 Sensitivity as a function of power consumption

II.2.5 Choice of modulation and frequency

Choice of modulation

After conducting a comprehensive analysis, it's concluded that On-Off Keying (OOK) and Frequency Shift Keying (FSK) are the two most extensively utilized modulation techniques in wake-up radio applications. It is worth noting that a substantial proportion of the wake-up radios described earlier utilize OOK modulation. OOK stands for the simplest form of Amplitude Shift Keying (ASK) which represents digital data such as the presence or absence of a carrier wave. In this case, a '1' is encoded by transmitting the RF carrier, while a '0' is simply the absence of the carrier. OOK modulation is easier to implement and requires less complex hardware. Additionally, OOK modulation requires only one frequency band, which makes it simpler to implement in low-power and low-cost devices.

In contrast, FSK modulation is more complex and dissipates more power, as it necessitates the use of an accurate local oscillator and I/Q signal path to demodulate the received RF signals. FSK modulation is also a digital modulation technique in which the information signal is modulated onto the frequency of the carrier signal. Compared to OOK modulation, FSK is more resilient to noise and interference. This is because the receiver only needs to detect the frequency of the carrier signal, which is less susceptible to noise.

Bea et al. (2015) [47] proposed a WUR designed with the demodulation of FSK. This WUR incorporated a digitally controlled oscillator, which was coupled with an envelope detector. The power consumption of this WUR was 45μW, which was relatively high when compared to its operating frequency of 80 MHz. Abe et al. (2014) [48] presented a method for reducing power consumption in the FSK wake-up radio, which comprised two main parts: an ultra-low power energy detection receiver (EDRX) and an address detection FSK receiver (ADRX). The ADRX was activated only when a wake-up packet was detected by the EDRX, thereby reducing power consumption. The ADRX used the FSK modulated address information from the second data packet (ADP) to activate the main receiver. The EDRX performed bit-length detection, while the ADRX performed address detection, resulting in improved noise immunity and lower average power consumption. The proposed receiver achieved a sensitivity of −87dBm while consuming an average power of 45.5μW.

Furthermore, Taris et al. (2015) [49] proposed a novel low power demodulator compatible with both OOK and FSK modulations, which featured an LC oscillator coupled with an envelope detector and is implemented using a 65nm CMOS technology. The circuit consumed 120μW, and properly demodulated OOK and FSK modulated signal at 2.4GHz with data rate up to 500kbps.

In general, both OOK and FSK modulation are popular choices in wake-up radio applications. The design of WUR systems leans towards using OOK, given its simplified implementation and lower power consumption. Similarly, in this thesis, we also opt for OOK modulation. Nonetheless, in scenarios where communication channels are noisy or congested, FSK modulation might prove to be a more suitable choice. The selection of the modulation technique is dependent on the specific requirements of the application, such as power consumption, reliability, and robustness.

Choice of frequency

Selecting an appropriate frequency for wake-up radio is also an important factor that affects several characteristics such as receiving antenna size, operating range, matching network, and selection of required components. Previous studies indicated a trend for wake-up radio from sub-GHz bands to 2.4 GHz. Based on Friis equation, with a sensitivity of −30dBm, transmit power of +10dBm, and a carrier frequency of 868 MHz, the theoretical maximal transmit distance is 4 meters. However, at higher frequencies, such as 2.4 GHz, the signal attenuation increases, causing it to decrease more quickly than a sub-GHz signal. This leads to needing more power to keep the same transmit distance. Nonetheless, the 2.4 GHz frequency provides a higher data rate and allows more compact antenna sizes compared to 868MHz. However, the 2.4GHz band is often congested and subject to interference, which can negatively affect signal reliability and robustness. In cases where higher data rates are crucial and interference levels are manageable, 2.4GHz can be a better choice.

Moreover, reducing the transmission frequency can increase the transmission distance, but it also increases the antenna's size. Based on the relationship between wavelength and the speed of light ($\lambda=c/f$), a quarter-wavelength antenna at 868MHz, the antenna size is 8cm, compared to 3.2cm for 2.4GHz.

Depending on the application scenario, both antenna size and signal attenuation caused by high frequency must be considered. In this thesis, we adopt 868MHz as the carrier frequency. The 868MHz bands are authorized by European regulations for data transmission, making them suitable for license-free radio frequency communications, providing simple and effective solutions.

Table 2.1 summarizes the main characteristics of WUR based on our review of the literature, including type, technology, sensitivity, power consumption, frequency, modulation, latency, data rate, and addressability.

Table 2.1 Comparison of wake-up radios' characteristics in the literature

Reference	Year	Type	Technology	Sensitivity	Consumption	Frequency	Modulation	Latency	Data rate	Addressability
[5]	2005	Passive	Discrete	−25dBm	–	433MHz	OOK	5ms	–	Yes
[6]	2011	Passive	180nm CMOS	−17dBm	2.64μW	900MHz	ASK	100μs	–	–
[7]	2014	Passive	130nm CMOS	−33dBm	–	868MHz	OOK	30μs	100kbps	No
[8]	2015	Passive	130nm CMOS	−53dBm	0.2μW	915 MHz	OOK	–	100kbps	–
[13]	2007	Passive	RFID	−6.7dBm	0.9μW	915MHz	–	2ms	140kbps	No
[14]	2014	Passive	RFID	−80dBm	–	915MHz	ASK	–	–	Yes
[12]	2015	Passive	RFID	–	–	915MHz	–	10ms	–	–
[17]	2014	Passive	RFID	−16dBm	–	868MHz	–	258ms	–	Yes
[18]	2014	Active	Discrete	−85dBm	1.2mW	2.4GHz	OOK	–	250kbps	Yes
[19]	2013	Active	130nm CMOS	−80dBm	7μW	2.4GHz	OOK	30ms	10kbps	Yes
[20]	2020	Active	28nm CMOS	−92.6dBm	495μW	2.4GHz	OOK	128μs/64μs	62.5kbps/250kbps	–
[21]	2015	Active	65nm CMOS	−72dBm	42.5μW	160MHz	OOK	–	100kbps	–
[22]	2016	Active	CMOS	−97dBm	40μW	28MHz	PWM	–	1.25kbps	Yes
[23]	2008	Active	90nm CMOS	−72dBm	52μW	2GHz	OOK	–	100kbps	No
[25]	2018	Active	180nm CMOS	−69dBm	4.5nW	113.5MHz	OOK	–	300bps	–
[26]	2019	Active	65nm CMOS	−79dBm	420pW	434MHz	OOK	10ms	100bps	–
[31]	2010	Active	RFID	–	80μW	2.4GHz	ASK	32μs	250kbps	–
[34]	2009	Semi-active	Discrete	−28dBm	819μW	868MHz	OOK	23.7ms	1.724kbps	Yes
[33]	2016	Semi-active	Discrete	−55dBm	1.2μW	868MHz	OOK	60μs	1kbps	Yes
[35]	2021	Semi-active	Discrete	−70dBm	1.9μW	868MHz	OOK	–	–	Yes
[36]	2015	Semi-active	Discrete	−30dBm	13.41μW	868MHz	OOK	80μs	200kbps	Yes
[37]	2017	Semi-active	Discrete	−28dBm	39μW	2.4GHz	OOK	16.06ms	1kbps	Yes
[38]	2010	Semi-active	AS393x	−52dBm	7.8μW	868MHz	OOK	13ms	250kbps	Yes
[39]	2020	Semi-active	AS393x	−50dBm	10.5μW	915MHz	OOK	–	250kbps	Yes
[40]	2013	Semi-active	Discrete	−45dBm	2.6μW	868MHz	OOK	–	1kbps	Yes
[41]	2009	Semi-active	120nm CMOS	−53dBm	12.5μW	2.4GHz	OOK	–	100kbps	–
[42]	2016	Semi-active	65 nm SOTB	−30 dBm	6.7nW	920MHz	–	–	–	No
[43]	2019	Semi-active	130nm CMOS	−71dBm	7.4nW	433MHz	OOK	–	200bps	Yes
[44]	2019	Semi-active	130nm CMOS	−56.4dBm	220nW	550MHz	OOK	100μs	400kbps	–
[45]	2022	Semi-active	CMOS	−63.2dBm	6.77μW	868MHz	OOK	–	0.5kbps	Yes
[46]	2007	Semi-active	RFID	−65dBm	2.8μW	300MHz	OOK	–	–	Yes
[47]	2015	Active	180nm CMOS	−62dBm	45μW	80 MHz	FSK	102μs	312kbps	–
[48]	2014	Active	65nm CMOS	−87dBm	45.5μW	924.4MHz	FSK	–	50kbps	Yes
[49]	2015	Active	65 nm CMOS	−36dBm/−27dBm	120μW	2.4 GHz	OOK/FSK	–	150kbps/300kbps	No

II.3 Study of rectifier in semi-active wake-up radio

In the context of wake-up radio, the rectifier is an essential component because it allows the radio to convert the incoming electromagnetic waves into usable DC current. As we mentioned before, for the WUR operating at 868MHz and transmit power of +10dBm, the RF signal power received by the antenna is already −30dBm or less at a separation distance of 5m. A good rectifier is especially important for improving sensitivity of the wake-up radio. A general block diagram of a rectifier is shown in Figure 2.14:

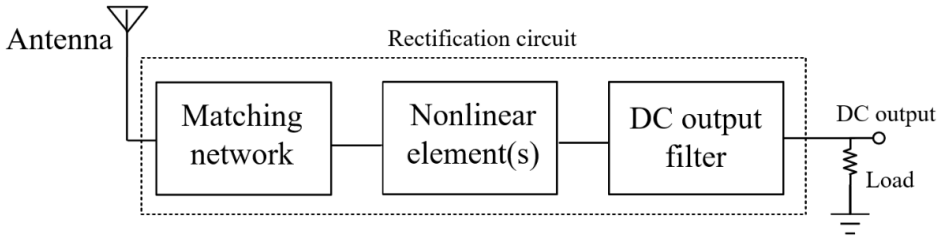

Figure 2.14 A general block diagram of a rectifier

Matching network: The matching network should be optimized to match the impedance of the antenna to the rectifier, which helps to maximize the power transfer efficiency.

Nonlinear elements: They are used to rectify the AC signal to DC. The diode is the most commonly used and the key element in rectifier circuits. Since the peak voltage of the AC signal obtained from the antenna and matching network is very low, it is best to use a diode with the lowest possible bias voltage [50].

DC output filter: This is a low pass filter which most often consists of a parallel capacitance block. The role of this filter is to remove the fundamental and harmonic frequencies from the output.

II.3.1 Efficiency of rectifier

The rectifier is the first stage of WUR and is responsible for rectifying the incoming RF signal to DC voltage. It must be capable of operating at low input voltage and providing an acceptable conversion efficiency at low power levels. RF-DC conversion efficiency can be optimal by using an efficient diode, choosing an appropriate topology, and allowing good impedance matching between the diode and the antenna. In this section, particular emphasis

will be put on the selection of the key element and the topology of rectifier.

II.3.2 Key element of rectifier: Schottky diode

The diode can be one source of power losses, and its performance has a significant impact on the performance of rectifiers. Schottky diodes are commonly used in rectifiers for wake-up radio due to their low forward voltage drop, which leads to higher efficiency. Figure 2.15 shows the equivalent circuit:

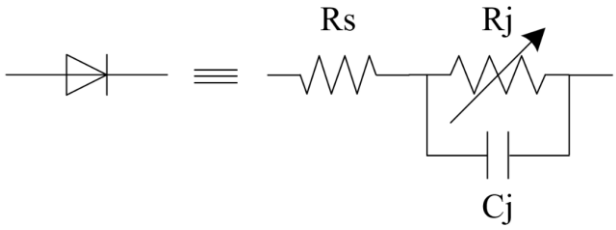

Figure 2.15 Equivalent circuit of Schottky diode

R_s is the series resistance, it limits the efficiency of diodes. Because the current flowing through the diode will dissipate the power in the semiconductor.

R_j is the parasitic junction resistance of the diode, which reflects the ohmic loss of the diode and is a function of the total current flowing through the diode. It is expressed as a function of the bias current I_b:

$$R_j = \frac{8.33\times10^{-5}nT}{I_b+I_s} \tag{2.1}$$

Where I_s is the saturation current, T is the temperature and n is the ideality factor.

The diode junction capacitance, denoted as C_j, is dependent on the bias voltage V_b and can be mathematically expressed using the following formula:

$$C_j = C_{j0} \times (1 - \frac{V_b}{V_j})^{-M} \tag{2.2}$$

where C_{j0} is the zero-bias junction capacitance of the diode. V_j is the amount of reverse bias potential applied on the device. M is the grading coefficient, which is a constant related to the geometry and material properties of the diode.

II.3.3 Choice of Schottky diode

Three key parameters of the diode impact the RF-DC conversion efficiency [51]. The series

resistance (R_s) limits the efficiency by means of dissipation losses, the zero-bias junction capacitance (C_{j0}) affects the harmonic currents through the diode and the breakdown voltage (V_b) limits the power handling capability of the rectifier. Generally, the reduction in C_{j0} will result in increasing of Rs and decreasing of V_b. We must make a good compromise between the parameters when designing a diode.

For low-power WUR applications, the received power is quite low, necessitating the selection of a diode with a low threshold voltage V_{th}. Table 2.2 presents three widely used commercial Schottky diodes. Among them, SMS7630 has the lowest V_{th}. Moreover, it has a low C_{j0} of only 0.14pF, which can have small harmonic currents through the diode to decrease the noise, making it suitable for high-frequency low-power applications. Thus, we choose the SMS7630 in our WUR application.

Table 2.2 Comparison of Three Schottky Diode Parameters

Parameter	**Bat1503W**	**SMS7630**	**HSMS2820**
$V_{th}(V)$	0.41	0.24	0.34
$C_{j0}(pF)$	0.26	0.14	0.7
$V_b(V)$	4	2	15
$R_s(\Omega)$	4.5	20	6

II.3.4 Different topologies of rectifier

There are different topologies of RF rectifier. The most popular rectifier topologies are the single series-mounted, the single shunt-mounted, the voltage multiplier, and the Graetz bridge. The serial and shunt topologies are the most used in the literature of the energy harvesting system. Moreover, we can also use the voltage multiplier or the Graetz bridge topology to improve the DC output. Each of the topologies has its advantages and disadvantages, which depends on the input power, the technology, and the required output voltage.

Series-mounted topology

The basic structure of a series-mounted rectifier is shown in Figure 2.16. The single diode is placed between the matching network and the DC filter. This topology is easy to implement, because it uses fewer components, so that it has less losses. For this reason, the series-mounted

structure is dedicated to low power levels. The choice is made for selecting zero-voltage diodes with low threshold voltage and low junction capacitance.

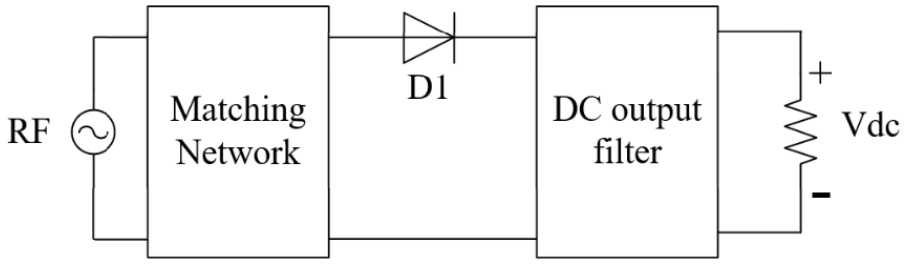

Figure 2.16 Structure of a series-mounted topology of rectifier

Shunt-Mounted topology

As shown in Figure 2.17, the diode is mounted in parallel between the two filters. This topology allows the recovery of low power levels with an efficiency close to the series-mounted topology. In addition, the anode or the cathode of the diode is connected to ground, it's therefore self-biased by the DC voltage which it generates.

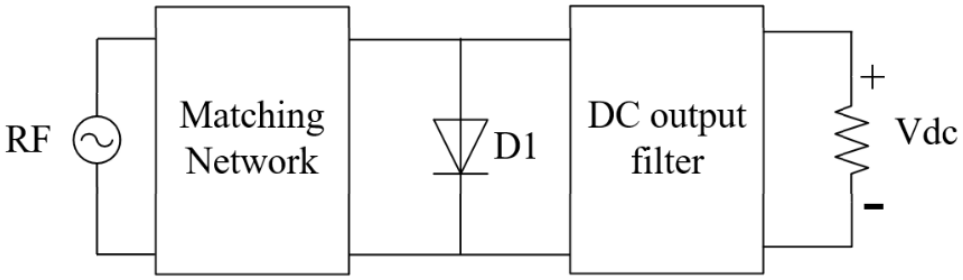

Figure 2.17 Structure of a shunt-mounted topology of rectifier

Voltage multiplier topology

Figure 2.18 presents a single stage voltage multiplier topology of rectifier. The capacitor C_1 stores the charges and biases diode D_2. This configuration provides a higher DC voltage in comparison to a single diode rectifier.

Furthermore, although increasing the number of stages can theoretically increase the output voltage, it also decreases the overall efficiency of the detector. This is because each stage introduces some loss due to the resistance of the components used, and this loss accumulates as more stages are added. The authors in [33] presented that a single-stage envelope detector is the optimal choice for wake-up radios. It provides high efficiency, sensitivity, and low noise compared to a multi-stage detector.

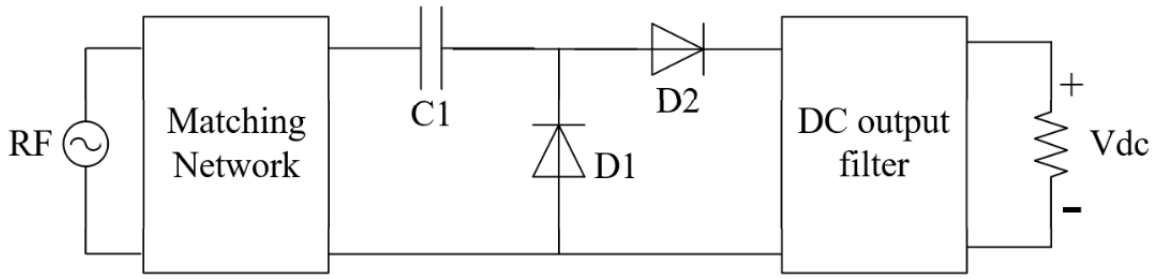

Figure 2.18 Structure of a single stage voltage multiplier topology of rectifier

Graetz bridge topology

The Graetz bridge topology is a full-wave rectification, similar to the voltage multiplier. As shown in Figure 2.19, the diodes D_2 and D_3 are conducting during the positive half-wave while the diodes D_1 and D_4 are blocked, and the opposite is true during the half-wave negative period. The positive and negative half-waves must cross two threshold voltages of the diode, which increase the loss. This is the reason why this structure is not suitable for low-level input power. However, it has the advantage of offering good power handling if high breakdown voltage diodes are used.

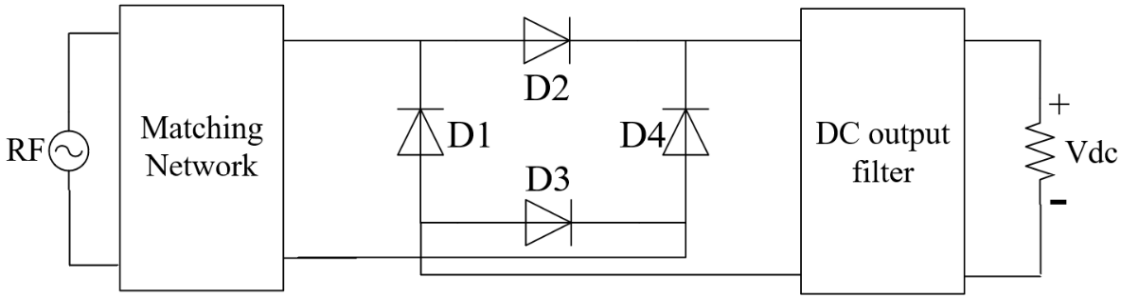

Figure 2.19 Structure of a single stage voltage multiplier topology of rectifier

II.3.5 Choice of topology of rectifier

The choice of rectifier topology depends on various factors such as required output voltage, available input power, and size constraints. Different rectifier circuit topologies have their advantages and disadvantages, and the best compromise between conflicting criteria such as RF-DC conversion efficiency, compactness, and robustness should be considered.

The single-diode topology and voltage multiplier topology have similar output voltages at the very low input level. In addition, the voltage multiplier topology provides much higher DC voltage above −25dBm of input power. However, the bridge topology is not sensible to small

input power. We will conduct simulation verification in the next section.

II.4 Semi-active wake-up radio's analog part analysis

In this thesis, we choose to focus on semi-active wake-up radio which is a trade-off between the two other topologies as it has a low power consumption and an acceptable transmit distance. And the discrete components method is our preferred approach due to its straightforward implementation, heightened flexibility, and to save time for our subsequent modeling. The circuit is usually based on a very simple circuit design, and it is optimized for energy efficiency, rather than high data rate [52]. As shown in Figure 2.20, the semi-active wake-up radio circuit usually consists of a matching network, an envelope detector, a reference voltage generator, a comparator, and a preamble detector.

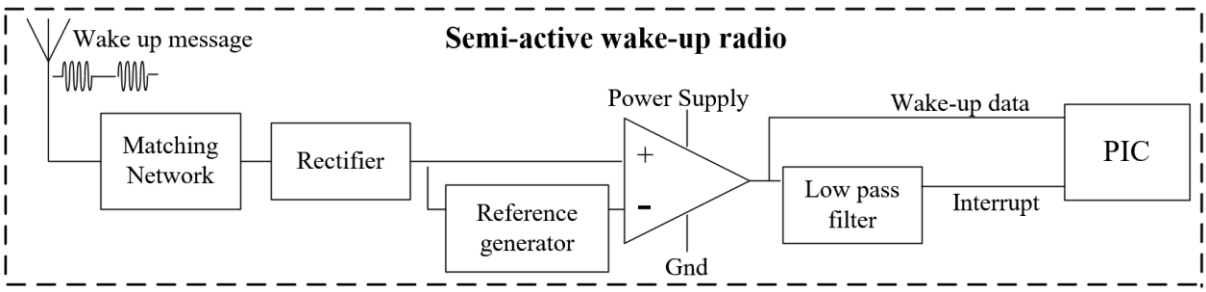

Figure 2.20 Block diagram of semi-active wake-up radio

II.4.2 Elements of the analog circuit

As previously mentioned in the above sections, it's necessary to create both the reference voltage and the signal at the input of the comparator. The reference voltage generator can be passive by using a simple RC low-pass filter. By adjusting the values of capacitors and resistors, the threshold value is theoretically held at 50% of the non-inverting comparator input. The low V_{th} Schottky diode SMS7630 is used, which has less leakage and small forward voltage.

The comparator is the only part that requires power to be supplied in the analog part. It reshapes the output of rectifier to approach a high level Boolean signal '1', which will be decoded by the PIC.

When selecting a comparator for WUR, several factors must be taken into consideration to

ensure optimal performance. Firstly, the comparator should have low power consumption. Secondly, the comparator must have a small offset because the voltage offset affects the sensitivity. Thirdly, the comparator should be fast enough to respond to the wake-up signal quickly and accurately. Fourthly, it should also be compatible with the voltage supply of the wake-up radio. The low-pass filter should send an interrupt to wake up the PIC micro-controller and exceed the lower limit of the TTL input high level of the PIC.

For instance, MAX903 from Maxim Integrated has ultra-high fast propagation delay and 1mV input offset, but the power consumption is very high, equal to 1.8mA. On the other hand, LPV7215 from Texas Instruments has 0.3mV input offset and 580nA power consumption but has a delay of 4.5μs. TLV3491 has moderate characteristics. Table 2.3 shows the characteristics of the three comparators.

Table 2.3 Comparison of three comparators' parameters

Parameter	**TLV3491**	**MAX903**	**LPV7215**
Consumption(μA)	0.8	1800	0.58
Offset (mV)	3	1	0.5
Supply Range (V)	1.8~5.5	5~10	1.8~5.5
Delay (us)	6	0.008	4.6
Package	SOIC	SOIC	SOT-23

In this thesis, a WUR with a data rate of 8kbps is designed. So, there is no need for the comparator to have a very fast propagation delay. Thus, TLV3491 and LPV7215 are chosen in this thesis.

The preamble detector that we use is a RC integrator with a lower cut-off frequency. It sends an interrupt to wake up the PIC, so that the PIC wakes up only if a preamble is received. Then it starts decoding the following address. This is done to minimize false/missed wake-ups caused by the noise and the interferences. Also, with this addressing capability, the wake-up message can trigger only the desired node. Although this will increase the overall latency, it can reduce the power consumption at the system level.

The electronic circuit of series-mounted rectifier of semi-active wake-up radio is illustrated in Figure 2.21.

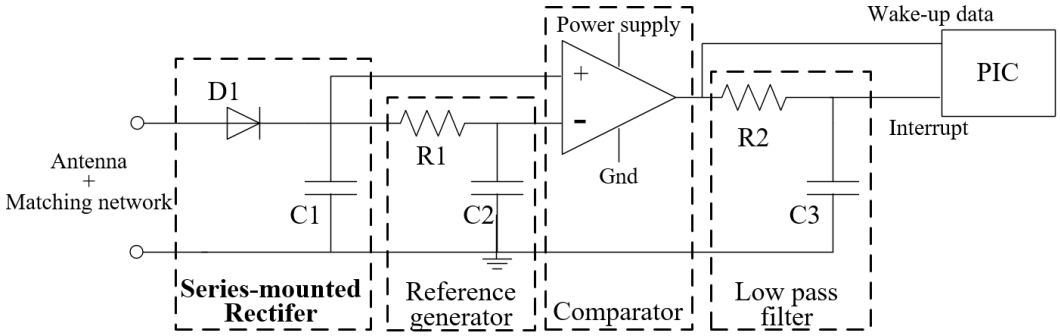

Figure 2.21 Electrical circuit of series-mounted rectifier of semi-active wake-up radio

II.4.3 Example of SPICE simulation result

To get the performances of the four rectifier topologies in semi-active wake-up radio circuit, transient analysis with SPICE models is run. The circuit is supplied by a voltage source generating an OOK modulation with a carrier frequency of 868 MHz and a transmission rate of 8kbps. In case of OOK modulation with a square wave, the corresponding baseband frequency would be 4kHz. The input power injected into the circuit varied from −50dBm to −10dBm. Figure 2.22 presents the SPICE simulation results of both 4 topologies with input power at −30dBm. For each topology, V_{in+} and V_{in-} of the comparator are represented.

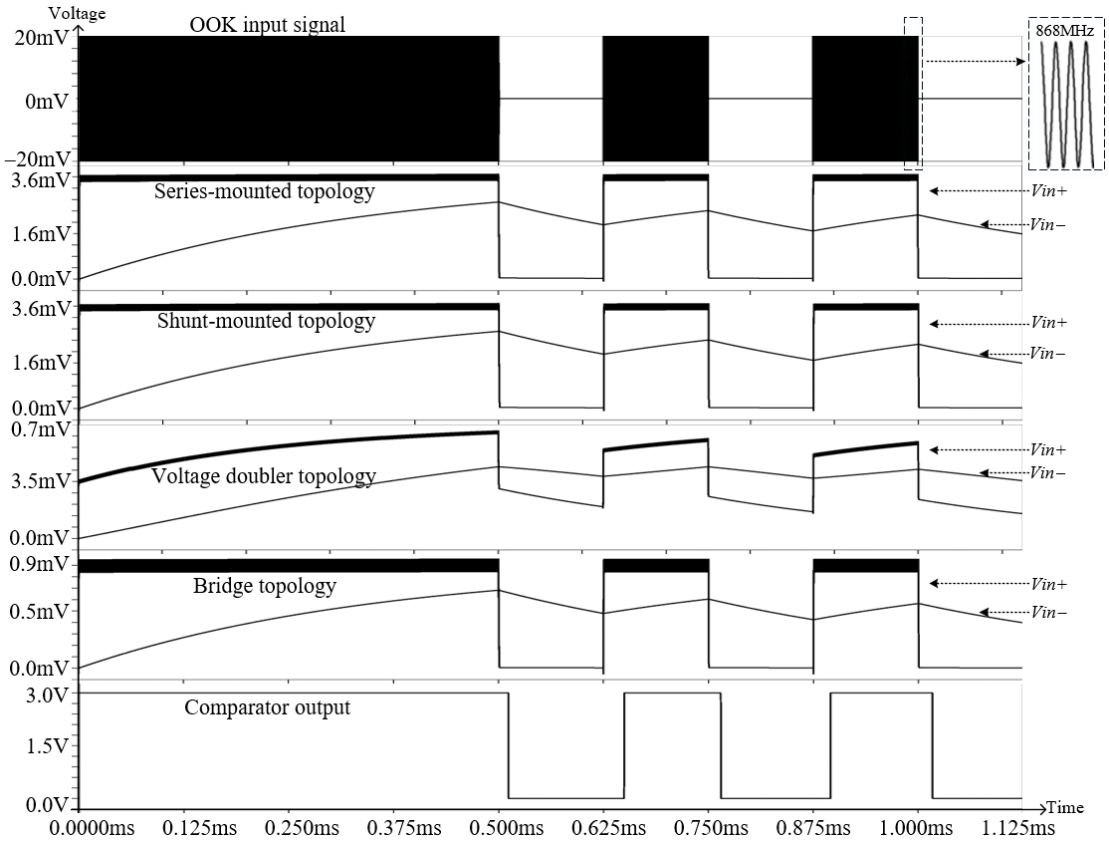

Figure 2.22 Simulation results of four topologies of rectifier with input power at −30dBm

II.5 Semi-active wake-up radio’s digital part analysis

In the previous section, we discussed the analog components of a semi-active wake-up radio (WUR) system, which are responsible for demodulating the OOK signal and initiating the wake-up process. In this section, we will shift the focus to the digital part, which is responsible for processing the demodulated OOK signal and activating the MCU for addressing. We will examine the importance of addressability in WUR systems and show the key points of the ultra-low power MCU programming.

II.5.1 Addressing mechanism

A well-designed wake-up system ought to activate the main radio only when the wake-up call is intended for that particular sensor. If all nodes within the sensor network adopt the same wake-up strategy, an attempt to awaken one node will trigger all nearby nodes, leading to a considerable loss of energy. Such a scenario may result in the unnecessary activation of sensors, thus wasting battery power [53]. Moreover, in the absence of addressability, every incoming message received by the WUR would trigger the node, leading to an increase in energy consumption due to eavesdropping [18].

To solve this problem, a potential solution involves incorporating a preamble detection and addressing capability into the WUR system to activate only the intended nodes. However, it is important to ensure that address decoding and command reading do not result in excessive power consumption. Thus, introducing an ultra-low power microcontroller (ULP MCU) is a suitable choice. Upon detecting the preamble, the ULP MCU wakes up from sleep mode. The preamble must be sufficiently long to cover the start-up time of the ULP MCU’s oscillator, which is the output of the preamble detector. To initiate data reading, a flag between the preamble and data is necessary to demarcate the message's start and generate an enable signal, allowing the MCU to start reading data. This data includes the main radio's address, which is also the output of the comparator. This approach may increase overall wake-up latency, but it diminishes false/missed wake-ups and system-level power consumption. The addressing time is proportional to the received message's data rate and is dependent on the address length and

baud rate.

II.5.2 Programming of ultra-low-power microcontroller (ULP MCU)

PIC is the name of the Microchip Micro-controller (MCU) family, which consists of a micro-processor, I/O ports, timers, and other integrated internal hardware. In this thesis, the Microchip product (PIC12LF1552) is chosen, which consumes only 60nW at 3V of standby mode. The Curiosity development board for programming the PIC12LF1552 is shown in Figure 2.23.

For programming, we mainly use the sleep-mode, the IOC (interrupt-on-change) and the Timer sampling function. In order to save power consumption, the PIC enters a sleep-mode when there is no incoming signal. Upon the generation of an interrupt by the preamble detector, the PIC is awakened and proceeds to read the output of the comparator. Once it detects the flag of sampling (low level), the PIC starts the data processing.

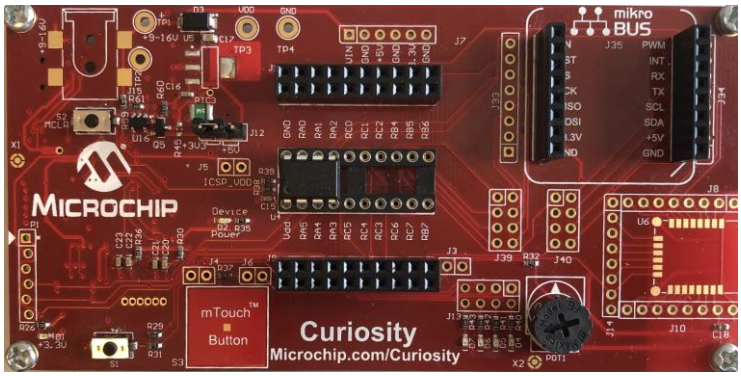

Figure 2.23 Curiosity development board

The PIC's sleep-mode disables its oscillator, which allows the device to operate in a low-power state. There are several events that can wake up the device from sleep, including resets, external interrupts, and interruptions by devices that can operate during sleep. To utilize the interrupt-on-change (IOC) feature to wake up the PIC, an interrupt can be generated by detecting a signal with either a rising or falling edge. Our approach is to set one of the I/O ports to connect to the preamble detector. Since the input type of the PIC is TTL, a logic 1 (V_{dd} = 3V) is only detected when the input reaches 1.55V. Therefore, the preamble mechanism can prevent interference and ensure accurate detection.

Timer0 is utilized to sample data, which is then compared to the pre-stored address of the

main radio to verify its correctness. To achieve a sampling rate of 8 kbps, the sampling time is calculated to be 125µs. The minimum system frequency of F_{osc}= 2MHz is set. Then an interrupt is generated by Timer0 when it overflows, indicating the start of the data sampling process.

II.7 Conclusion

According to different power supply methods, WUR can be divided into fully-passive, fully-active, and semi-active. For fully-passive wake-up radio, although the power consumption is relatively low, their sensitivities are low compared to active radios. The wake-up range is usually several meters, which limits the performance. On the other hand, the fully active WUR can solve the constraints of fully-passive WUR. It usually has a relative long wake-up range but requires a permanent power supply. And the semi-active WUR is the most common approach, the consumption and sensitivity are balanced.

Furthermore, the power consumption, size and performance of WUR depend on its technology and implementation. Discrete components enable rapid implementation, allowing designers to simplify the WUR prototyping process. But CMOS-based WUR has lower power consumption and smaller size. Our initial work is based on discrete semi-active wake-up radio with addressing capability.

During the design of a wake-up radio system its efficiency and overall performance should be maximized. We also provide an analysis of how to select key components and topology of the circuit. When selecting a diode, the choice is made for selecting zero-voltage diodes with low threshold voltage and low junction capacitance. When selecting a comparator, power consumption, sensitivity, speed, voltage supply, and input offset are important factors to consider. And we provided the comparison of different topologies of rectifier. Moreover, we also perform a simulation of the WUR circuit, as well as a programming analysis of the addressing part. The results are provided as a preliminary study for the design which can be easily adapted to the particular cases and prepared for the implementation and modeling of the device.

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Chapter III: Design and modeling of semi-active wake-up radio

III.1 Introduction

In this chapter, we focus on the design and modeling of semi-active wake-up radio. We first conduct the SPICE simulation and implementation of semi-active wake-up radio with different rectifier topologies. Following this, we perform theoretical modeling of free space propagation, different rectifier topologies, as well as the analog and digital parts of the semi-active WUR. The precision of the WUR's circuit modeling is important to optimizing the overall consumption of sensor networks.

By using a wake-up radio on top of the main radio in the nodes, the main radio can remain in sleep mode as long as possible, ideally if it has no action (transmit or receive) to perform in the network. The counterpart is that there may be false wake-ups or missed wake-ups during the transmission, thus increasing the transmission time and the average energy per transmitted bit: when the WUR is disturbed by noise or interference, most of this can be prevented by the PIC micro-controller; when the wake-up radio misinterprets the wake-up signal and fails to wake up the main radio, the transmitter will retransmit the wake-up packet many times until it successfully wake up the main radio. To accurately account for these effects, an accurate modeling of the WUR is necessary.

Most of the models used nowadays are based on the on-off wake-up method: in the simulation, the node wakes up if the transmission distance is less than the wake-up distance; otherwise, the node does not wake up. For example, in Figure 3.1, the wake-up distance is depicted as D_{wu}, and the transmit distance between Node0 and Node1 (resp. Node2) is expressed as D_1 (resp. D_2). In other words, the model divides the space into a white zone where the radio always wakes up and a black zone where the radio never wakes-up. In practice, the model should also account for a “grey zone” where the wake-up probability is not always 0 or 1 but depends on the ratio D_i/D_{wu}, where D_i is the distance between the receiving node and the transmitter.

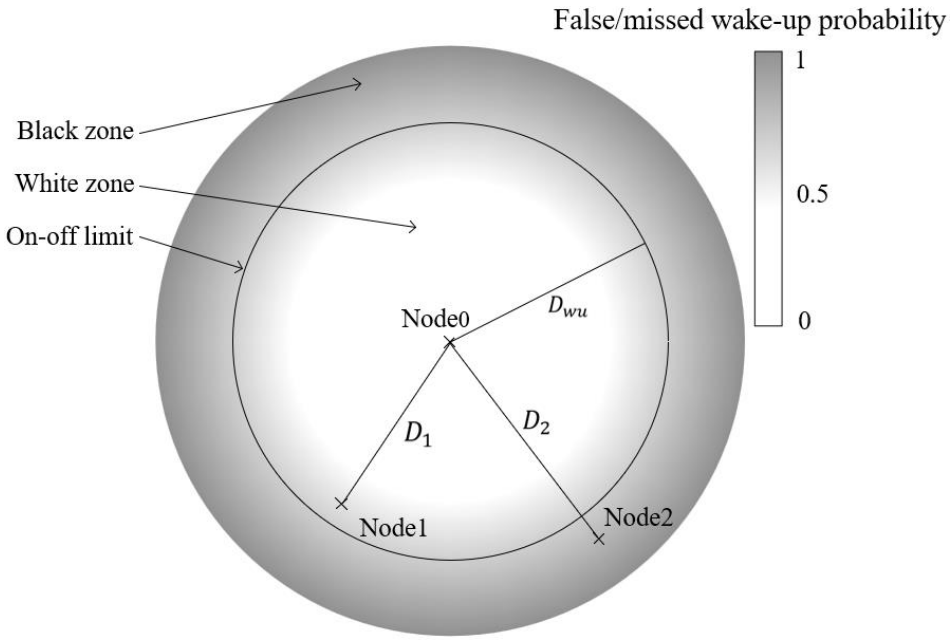


Figure 3.1 Description of false/missed wake-up probability

SPICE simulations provide a quick and effective method to assess circuit behavior before the prototype is built. However, while SPICE simulations are relatively fast to execute, they rely heavily on the accuracy of the models used for each component. This may not always show the real-world performance.

On the other hand, the development of physical prototypes is significantly more time-consuming and costly. It involves the physical fabrication of the circuit, which can be a lengthy process depending on the complexity of the design. However, prototypes provide a high degree of accuracy as they operate under real-world conditions.

Theoretical modeling is the fastest approach, which is often based on established principles and equations. It provides an initiated understanding of system without the need for any physical construction or extensive computer simulations. However, it's accuracy is the lowest.

In this work, we provide a comprehensive description of the wake-up radio, including its analog and digital parts. And we also characterized the delay and false/missed wake-ups that significantly affect the accuracy of the WUR model.

The remainder of this chapter is organized as follows: Section III.2 presents the SPICE simulation and implementation of semi-active wake-up radios with different rectifier topologies. Section III.3 discusses the modeling of free space propagation. Section III.4 introduces the models describing the response of three types of rectifier circuits, which will be validated

through simulation results. Sections III.5 and III.6 respectively discuss the modeling of the remaining analog and digital parts of the wake-up radio. Finally, Section III.7 concludes this chapter.

III.2 SPICE simulations, and performance comparison of semi-active wake-up radio with different rectifier topologies

In this section, we aim to provide a more comprehensive analysis of semi-active WUR with different rectifier topologies, building upon the previous chapter where the fundamentals, advantages and disadvantages of each topology were discussed. The focus of this section will be on the SPICE simulations of the wake-up radio with series-mounted, shunt-mounted and voltage doubler rectifier topologies.

Before the SPICE simulation, we first choose the components' SPICE models or values, and then proceed to the circuit simulation. The agreement between these simulation results and theoretical expectations provides an initial validation of the results. And then in section III.7, the measurements are presented and further emphasize the effectiveness of the choices.

Figure 3.2(a) presents the series-mounted rectifier topology in semi-active wake-up radio circuit. In this configuration, C_1 is added to eliminate the harmonic noise from the rectified signal. Due to the non-linear behavior of diodes, they generate frequency harmonics from the incident power [1]. And this capacitor eliminates all harmonics and allows only the DC component to pass through [2]. The appropriate value of the filtering capacitor is important for reducing output voltage ripple and improving overall circuit reliability. When choosing the capacitor value, simulation shows that the value should not be too close to the C_2 value of the RC low-pass filter to avoid affecting system performance. For our WUR operating at high frequency (868MHz), parasitic effects and the impedance of the capacitor significantly influence circuit performance. Through simulations, we find that a value of 22pF strikes the right balance between filtering and speed (response time).

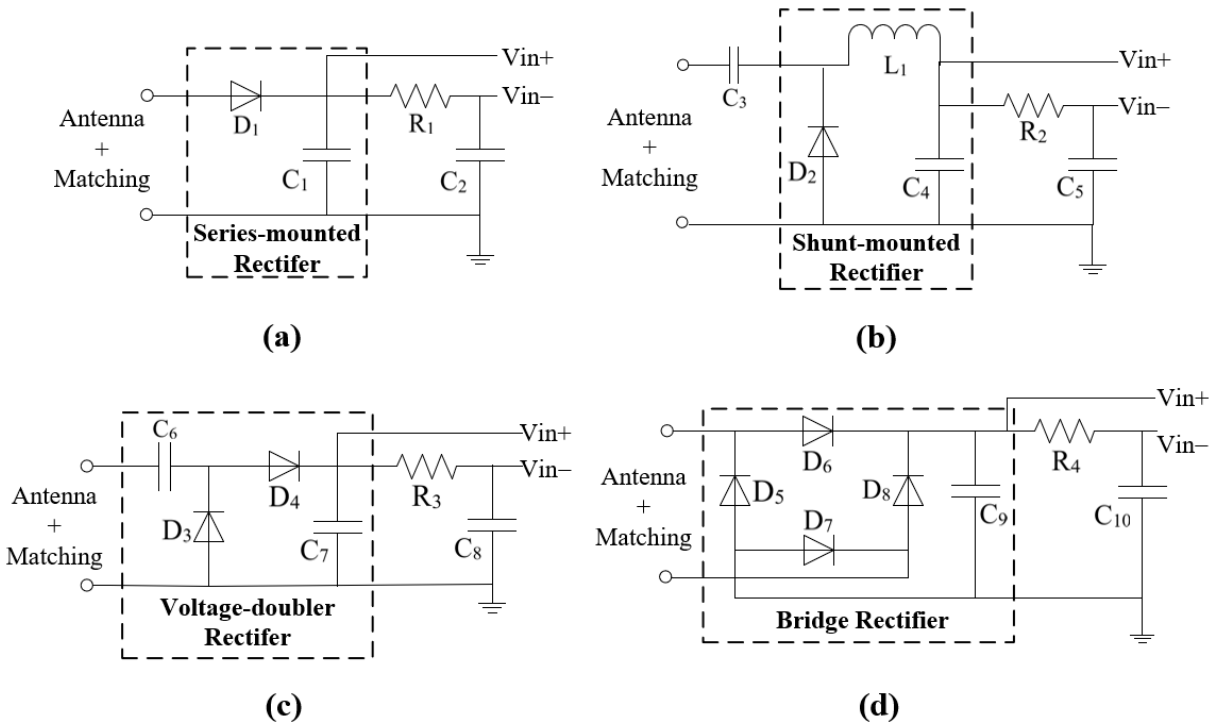


Figure 3.2 Rectifier topologies in semi-active wake-up radio circuit: (a) series-mounted topology; (b) shunt-mounted topology; (c) voltage doubler topology; (d) bridge topology

For the V_{in-} of the comparator, an adaptive threshold mechanism is adopted (R_1-C_2), which is also served as a reference generator. By adjusting the values of the capacitor and resistor, the threshold voltage V_{in-} is kept around 50% of the V_{in+} signal level. This is used to increase the dynamic range of the WUR and is suitable for weak and strong signals. In addition, energy from the antenna is utilized for threshold generation instead of a voltage divider, which reduces static power consumption.

The resistor and capacitor are connected in series to form an RC circuit. The time taken for the capacitor to charge up to half of its voltage is denoted as 0.7τ, where τ is the time constant of the circuit ($\tau = R_1C_2$), with R_1 being the resistance value and C_2 being the capacitance value [3]. If the C_2 is too small, it may result in a large corresponding resistance, forming a bridge circuit with the comparator's input impedance. However, a too large C_2 may negatively affect the response speed. Thus, we opt for C_2=1nF to achieve a balance between filtering and response speed. Then the calculation for resistance is as follows:

$$T = \frac{1}{4kHz} = 250\mu s \tag{3.1}$$

$$\tau = T_{bit} \cdot \frac{1}{0.7} = 357\mu s \tag{3.2}$$

$$R_1 = \frac{\tau}{C_2} \approx 350K\Omega \tag{3.3}$$

Where f is the baseband frequency. This leads to the value of R_1.

Figure 3.2(b) shows the shunt-mounted rectifier topology. In the front-end of the circuit, a DC block capacitor C_3 is used to prevent DC current from the rectifier to the microwave source, avoiding any interference with the RF source due to the DC signal. To ensure optimal rectifier performance and minimize signal loss, we need to choose a capacitance value that offers a low capacitive reactance at the operating frequency (RF short-circuit), typically less than a few ohms [4]. At an operating frequency of 868 MHz, according to [4], we assume a reactance of less than 2Ω, and the reactance calculation formula is used [5]:

$$X_c = \frac{1}{2\pi fc} \tag{3.4}$$

Where f is the operating frequency, and C is the value of the DC blocking capacitor.

From this calculation, a capacitance value of 91pF is obtained. Thus, a 100pF capacitor is selected as a commercially standard value, and then confirm through SPICE simulation.

Additionally, the RF choke L_1, positioned between the diode and the output low-pass filter, helps in forming the RF loop and effectively captures energy in the diode, facilitating the conversion of power into DC current. The RF choke can be realized by an inductor or a quarter-wavelength transmission line [1] [6]. common-mode current doesn't balance out with equal and opposite currents, leading to potential interference. As presented in [7], we chose the reactance of the RF choke to be 10 times the load impedance of the circuit, ensuring that its reactance is at least 500 ohms at the lowest operating frequency to eliminate or minimize the AC component. The reactance formula for the inductor is as follows [5]:

$$X_L = 2\pi fL \tag{3.5}$$

Where f is the operating frequency and L is the RF choking inductor's value.

Upon calculation, we obtain an inductor value of 92nH. Here, we select 100nH as the inductor value for the RF choke.

The voltage doubler rectifier circuit, as illustrated in Figure 3.2(c), is composed of two diodes and two capacitors, and can be regarded as a combination of a series topology and the shunt topology. During the negative half-cycle, diode D_3 conducts and charges DC blocking capacitor C_6; during the positive half-cycle, energy from the antenna stored in C_6 are transmitted

to the output through the conducting diode D_4. The advantage of the voltage doubler is that it can achieve higher DC output voltages.

It can be noted that in both the voltage doubler topology and the shunt topology, the DC blocking capacitor between the matching network and the diode serves a similar purpose, preventing DC current and allowing RF signals to pass through. However, in the voltage doubler topology, the DC blocking capacitor C_6 also acts as an energy storage element responsible for storing and releasing energy during each half-cycle [8]. Therefore, C_6 needs a sufficiently large capacitance value to ensure minimal voltage fluctuations throughout the energy storage and release process. In this design, we chose a capacitance value of 47nF for C_6.

Furthermore, Figure 3.2(d) shows a bridge rectifier circuit. Unlike the previous three topologies, it utilizes the entire input waveform. During the positive half-cycle, more current flows more through diodes D_6 and D_7 than D_5 and D_8. In the negative half-cycle, the situation is reversed. However, it may not be optimal for low power levels, as the signal must always cross two diodes.

To get a comparison of the performances for each topology, a more comprehensive transient analysis is conducted, neglecting the insertion loss due to the mismatch between the antenna and the rectifier. This assumption is usually verified in practice, by using a multistage LC adaptation network. A voltage source supplies the circuit, generating an OOK modulation with a carrier frequency of 868MHz and a baseband frequency of 8kbps. To mimic the antenna characteristic impedance, the source is simulated with a resistance of 50Ω. Then, the voltage amplitude varies from 3.5mV to 200mV which corresponds to a maximum theoretical power injected into the circuit in the range −45dBm to −15dBm approximately. The calculation formula is as follows [9] :

$$P_{RF_{max}} = \frac{(V_S)^2}{8 \cdot Z_{ant}} \tag{3.6}$$

Where V_S represents the input peak voltage and Z_{ant} is the impedance of the antenna.

The more energy in the RF signal, the greater the voltage change at the output of the rectifier, which is sensed by the comparator. In literature the evolution of DC output is often converted to output DC power referred to the comparator input impedance, and the efficiency is computer as the ratio between the DC power and the RF input power. However, in the very particular case

of low power wake-up radio, we think that the DC voltage provided by the rectifier is more relevant than the DC power. Figure 3.3 presents the DC output of four rectifier topologies.

The voltage oscillation during the high-state is mainly due to the small size of the rectifier output capacitance and is the main limitation of the sensitivity. Thus, a study is performed to compare the input sensitivity of each topology. For this purpose, another set of transient simulations has been run to determine the minimal input power that guarantees a correct comparator output (cf. Table 3.1). The above-mentioned capacitor of interest also impacts the slew rate, so it can be adjusted depending on the specifications one has to achieve.

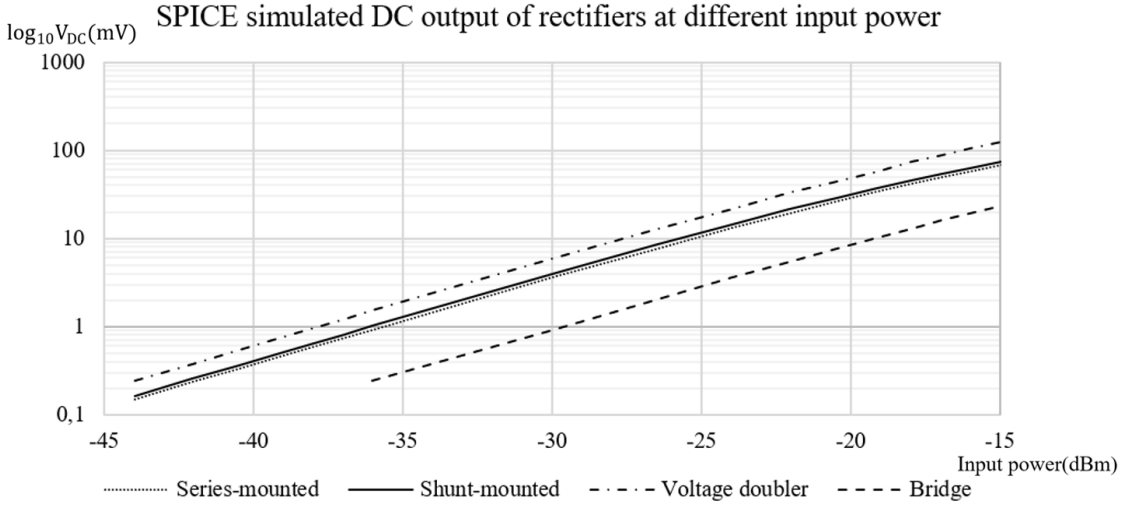


Figure 3.3 The DC output of four rectifiers at input power from −45dBm ~ −10dBm

The slew rate is an important characteristic of such circuits as it can affect the data rate or the bit error rate, and thus the consumption of the overall receiver, including the main radio and not only the wake-up. In simulations, the slew rate is simulated on the “minus” input of the comparator during a transition from the maximum off-to-on or on-to-off state of the modulation. They are compared for each topology at −30dBm. The results are reported in Table 3.1.

Table 3.1 Comparison of four topologies of rectifier

Topology	**V_{dc} (mV) @−30dBm**	**Slew rate (mV/µs) @−30dBm**	**Sensitivity (dBm)**	**SNR_{min} (dBm) @−70dBm**
Series-Mounted	3.59	27.87	−46.5	−42.76
Shunt-mounted	3.96	5.47	−47.1	−42.76
Voltage Doubler	5.97	18.32	−46.8	−45.25
Bridge	0.92	11.69	−40.5	−37.5

Finally, the noise effect is studied. The noise is simulated in the time domain by adding a current source in parallel to each resistive and active component. The source generates a white gaussian noise corresponding to the thermal noise at 300K. A noise is also added to the RF source and varying the signal over noise ratio (SNR) shows the maximal allowed SNR to keep a correct comparator output.

It has to be noted that the results present in the table may slightly vary according to design choices. They are still suitable for architecture exploration or preliminary feasibility study of low power designs implying semi-active wake-up radio.

Additionally, in the simulations, we found that the most critical parameter that affects the sensitivity is the input offset voltage V_{os}. Figure 3.4 presents the OOK signal with an input power at –43dBm (close to the expected sensitivity of the device), which contains a preamble and the address "1010" of the main radio of the destination node. And a source of noise is added to the RF signal, with a noise power level of –70dBm.

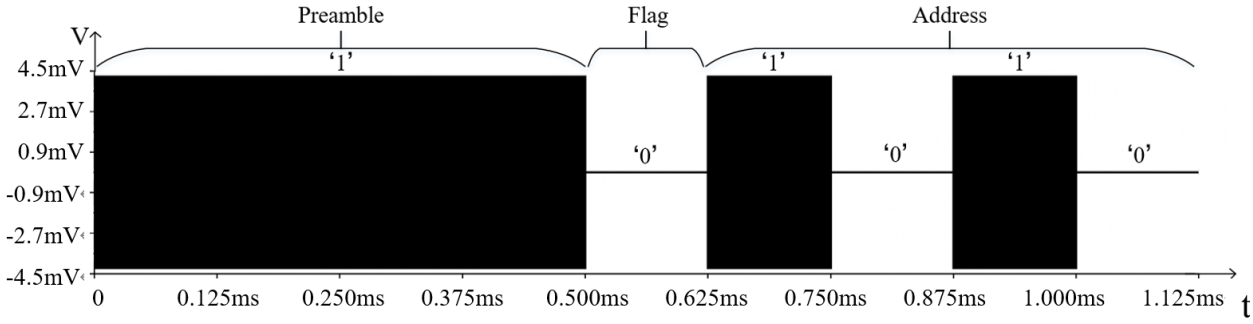


Figure 3.4 Input OOK signal of SPICE simulation

Since the voltage of V_{in-} is close to 50% of the signal level of V_{in+}, but the comparator adds an offset to V_{in+}, the difference between V_{in-} and offset will decrease continuously as the input signal decreases. Finally, V_{in-} can never exceed the offset, and then the output tends to be distorted. Figure 3.5 presents an example of the wake-up packet reception in series-mounted topology WUR with the positive (V_{in+}) and negative (V_{in-}) inputs of the comparator respectively, as well the output of the comparator, which compares the ideal output and the output with offset.

Furthermore, due to the existence of the offset on V_{in+}, the comparator has better identification of bit '1' compared to bit '0'. Therefore, different OOK data show different sensitivities. Table 3.2 shows the sensitivities of different address in series-mounted topology.

Other topologies also exhibit variations in sensitivities for different addresses, those details will not be further presented here.

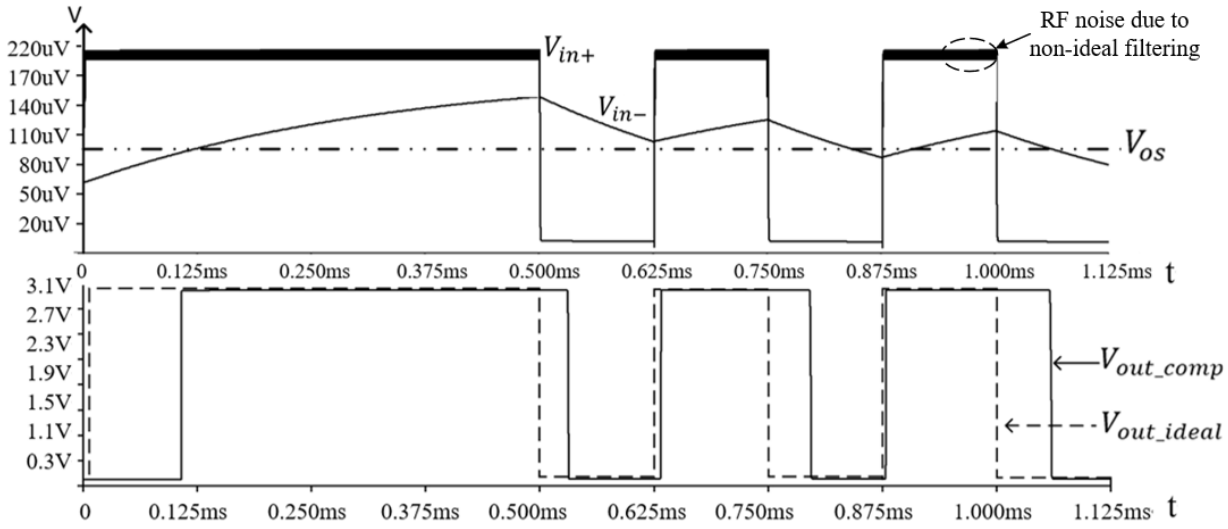


Figure 3.5 Simulation result of the comparator input and output voltages in series-mounted topology

Table 3.2 Sensitivities of different address in series-mounted topology

Preamble + Address	**Sensitivity @Noise −70dBm**
0b111101000	−40.34dBm
0b111101001	−42.58dBm
0b111101010	−42.76dBm
0b111101011	−43.15dBm
0b111101100	−42.95dBm
0b111101101	−43.76dBm
0b111101110	−43.76dBm
0b111101111	−44.42dBm

III.3 Modeling of free space propagation

Following our preliminary research on wake-up radio, we now advance to the development of a theoretical model for the WUR circuit. The formulas obtain from the modeling will provide the foundation for future scenario simulations within sensor networks. In wireless communication systems, free space propagation refers to the transmission of electromagnetic waves in a space without interference from other objects. To analyze and predict signal propagation and attenuation in WUR circuit, the free space propagation model is employed, and

the Friis transmission formula is utilized to estimate the path loss between the transmitting and receiving antennas. We consider two antennas in free space (with no nearby obstacles), with a distance of d between the transmitting antenna (gain G_T) and the receiving antenna (gain G_R), operating at frequency f. The configuration is illustrated in Figure 3.6.

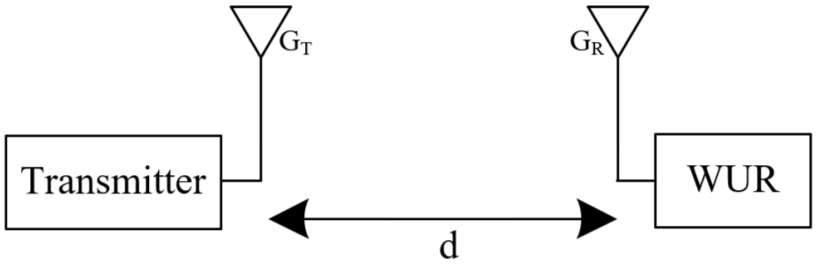


Figure 3.6 Block diagram of free space propagation

We assume that the total power P_T is transmitted to an omnidirectional and lossless transmitting antenna, with the receiving antenna located in the far field of the transmitting antenna [10]. Assuming that the antennas are well-matched in terms of impedance and polarization, the received power P_R can be expressed as:

$$P_R = \frac{P_T G_T G_R c^2}{(4\pi f d)^2} \tag{3.7}$$

where c is the speed of light, which is equal to 3×10^8 m/s.

This Friis equation, which relates free space path loss, antenna gain, and wavelength to the received and transmitted power. Given the relationship between wavelength λ and frequency f with the speed of light c ($\lambda = c/f$), another form of the equation is:

$$P_R = \frac{P_T G_T G_R \lambda^2}{(4\pi d)^2} \tag{3.8}$$

In addition, since the transmitted and received power are often provided in dBm, and the antenna gain is given in unit dBi, the Friis equation in logarithmic scale is expressed as:

$$[P_R]_{dBm} = [P_T]_{dBm} + [G_T]_{dBi} + [G_R]_{dBi} - [P_{LOSS}]_{dB} \tag{3.9}$$

where P_{LOSS} represents the path loss, given in dB by the following expression:

$$[P_{LOSS}]_{dB} = 10\log_{10}\left[\frac{\lambda^2}{(4\pi d)^2}\right] = 20\log_{10}[\frac{\lambda}{4\pi d}] \tag{3.10}$$

III.4 Modeling of different topologies of rectifier

This section presents the theoretical model of rectifier that provides quite accurate results

for a very low development time, in the absence of a suitable spice model. This approach is particularly beneficial when a suitable SPICE model is unavailable. We will demonstrate the model's effectiveness by comparing its performance to the results of SPICE simulations.

In traditional methodologies for diode analysis, it is common to assume that the amplitude of the input voltage surpasses the forward conduction voltage of the diode. However, in the context of wake-up radio applications, the signals received by wireless devices are typically quite small and may be lower than the diode's forward voltage. Despite this, the rectifier circuit still operates. Given this situation, traditional methods of analysis become insufficient. Therefore, it is essential to identify and develop circuit modeling methods that are specifically suited to the characteristics and requirements of WUR applications.

Our modeling is based on two different methods: Newton's method and Wallis' method. Newton's approach offers a higher precision. On the other hand, Wallis' method proves to be effective for voltages below −10 dBm, which has the advantage in terms of CPU time. The following parts will discuss in detail the modeling and analysis of three topologies of rectifier circuits for WUR applications: series-mounted, shunt-mounted, and voltage doubler topology.

However, due to the poor sensitivity of the bridge topology in the SPICE simulations for wake-up radio systems, we don’t conduct modeling for the rectifier of the bridge topology. Furthermore, we also don’t produce a PCB for the WUR of this topology in the subsequent measurements.

III.4.1 Modeling of series-mounted topology

To determine the input of comparator V_{in+}, which is the output of rectifier as well, equations for the DC output voltage of a diode detector were developed in [11]. The transfer characteristics for sine inputs show that their AC-induced error term involves a zero-order modified Bessel function of the first kind. Besides, if the smoothing capacitor is sufficiently large, the AC error is independent on frequency, so voltage drop across the capacitor can be neglected between the peaks of the rectified waveform. This allows to determine the detector’s AC-DC transfer function [11].

Figure 3.7 shows the electrical circuit of the series-mounted diode rectifier, where V_p is the

input peak voltage, f is the carrier frequency and C_1 is the charge capacitor that regulates the voltage. V_d is the instantaneous voltage appearing across the diode, V_{in+} is the DC output voltage, and R_1 is the load resistance of the rectifier. For our circuit, R_1 is the input resistance of the comparator TLV3491, which is measured about 1.6 MΩ.

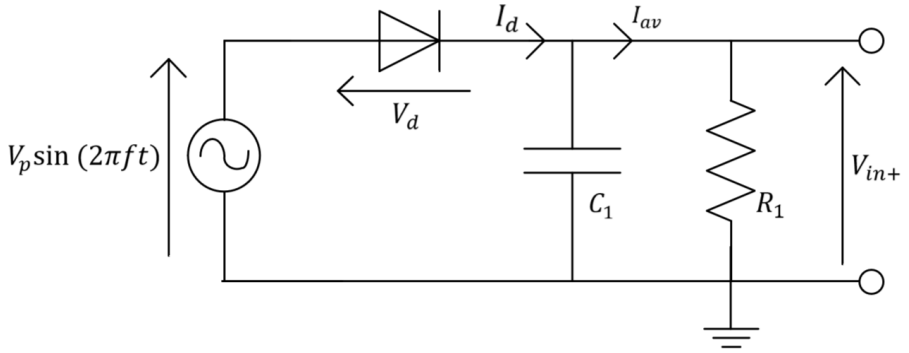


Figure 3.7 Simplified electrical circuit of a series-mounted diode rectifier

The current-voltage (I-V) equation for a Schottky diode can be expressed as [12]:

$$I_d = I_{sat}[\exp\left(\frac{V_d}{V_T}\right) - 1] \tag{3.11}$$

Where $V_T = kT/q$, represents the thermal voltage; q is the elementary charge of an electron; k is the Boltzmann's constant and T is the physical temperature in Kelvins. Additionally, based on the circuit in Figure 3.7, we have:

$$V_d = V_p \sin(2\pi ft) - V_{in+} \tag{3.12}$$

$$V_{in+} = I_{av} \cdot R_1 \tag{3.13}$$

Therefore, the average current flowing through the diode is the key to the problem. This can be expressed as follows:

$$I_{av} = \frac{V_{in+}}{R_1} = \frac{1}{T}\int_0^T I_d dt \tag{3.14}$$

Here, T covers the entire duration of one complete cycle. According to the Shockley diode equation (3.12) and the derivation in [11], the expression of I_{av} then becomes:

$$I_{av} = I_{sat}\left[\exp\left(\frac{-V_{in+}}{V_T}\right) I_0\left(\frac{V_p}{V_T}\right) - 1\right] \tag{3.15}$$

where $I_0(\cdot)$ is the modified Bessel function of the first kind. The series expansion for $I_0(x)$ is given as:

$$I_0(x) = \sum_0^\infty \frac{(\frac{x}{2})^{2n}}{(n!)^2} \tag{3.16}$$

Here, x is the argument, and k is the index of summation. This series converges for all

values of x. And then the function for the DC output voltage is defined as:

$$f(V_{in+}) = V_{in+} - R_1 \cdot I_{sat}\left[exp\left(\frac{-V_{in+}}{V_T}\right) I_0\left(\frac{V_p}{V_T}\right) - 1\right] \tag{3.17}$$

To find the value of V_{in+} for this function $f(V_{in+}) = 0$, we propose to adopt Newton-Raphson algorithm as an alternative to the method presented in [11]. This approach offers faster calculation speed and converts the solution of this nonlinear equation into a series of linear equation solutions [13]. Starting with an initial guess of V_p, the circuit then finds new points and re-linearizes, repeating the process until convergence is achieved:

$$x_{n+1} = x_n - \frac{f(x_n)}{f'(x_n)} \tag{3.18}$$

Where x_n (resp. x_{n+1}) is the V_{in+} value at the n^{th} (resp. $(n+1)^{th}$) iteration. Newton's method yields to an accurate calculation whether the input voltage reaches the diode's breakdown voltage or is as small as 1pV.

Furthermore, since the WUR is low power, we are more interested in a small input power to speed up. Impedance of the comparator is very large versus the filter capacitor. In the process of capacitive filtering, we regard V_{in+} as a constant, so the average value of the current over a cycle is 0.

According to formulas (3.12) and (3.15), we have:

$$I_{av} = \frac{1}{T}\int_0^T I_{sat}\left[\exp\left(\frac{V_p \sin(2\pi ft) - V_{in+}}{V_T}\right) - 1\right] dt \tag{3.19}$$

$$I_{av} = \frac{I_{sat}}{T}\int_0^T \exp\left(\frac{V_p \sin(2\pi ft)}{V_T}\right) \exp\left(-\frac{V_{in+}}{V_T}\right) dt - I_{sat} \tag{3.20}$$

The first exponential in the current equation can be expanded by Taylor series [14]:

$$e^x = \sum_{n=0}^{\infty} \frac{x^n}{n!} \tag{3.21}$$

Then, equation (3.21) can be transformed into the following expression:

$$I_{av} = \frac{I_{sat}}{T}\int_0^T \sum_{n=0}^{\infty} \frac{1}{n!} \left(\frac{V_p \sin(2\pi ft)}{V_T}\right)^n \exp\left(-\frac{V_{in+}}{V_T}\right) dt - I_{sat} \tag{3.22}$$

We hope to find a simplified method that is equally accurate for input powers from −45dBm to −10dBm. In this range, we can neglect the current through R_1. In this condition, we have:

$$I_{av} = \frac{I_{sat}}{T} \exp\left(\frac{-V_{in+}}{V_T}\right) \sum_{n=0}^{\infty} \frac{1}{n!} \left(\frac{V_{in+}}{V_T}\right)^n \int_0^T sin^n(2\pi ft) dt - I_{sat} = 0 \tag{3.23}$$

The solution is given as a function of Wallis integral [15]. The integral of the sine term in equation (3.23) can be represented by the Wallis formula for the sine function, which is defined

by terms of the following sequence $(W_n)_{n\geq 0}$:

$$W_n = \int_0^{\frac{\pi}{2}} sin^n x\, dx \tag{3.24}$$

It can be proved that odd power terms have no contribution to the voltage output in our case, so we operate the index substitution $n = 2m$. Then we can get the DC output voltage as:

$$V_{in+} = V_T \cdot ln\left[\sum_{n=0}^{\infty} \frac{1}{(2m)!} \cdot \left(\frac{V_p}{V_T}\right)^{2m} \cdot \frac{2W_{2m}}{\pi}\right] \tag{3.25}$$

The W_{2m} in (3.25) can be expressed as:

$$W_{2m} = \frac{\pi}{2} \frac{(2m)!}{(2^m \cdot m!)^2} \tag{3.26}$$

The first three terms of the sequence have been taken. Figure 3.8 presents V_{in+} as a function of input voltage V_p, which compares Newton's method, Wallis' method, and the SPICE simulation results. We can conclude that they all work well on small input power intervals and thus there is no need to complexify the models to get accurate results.

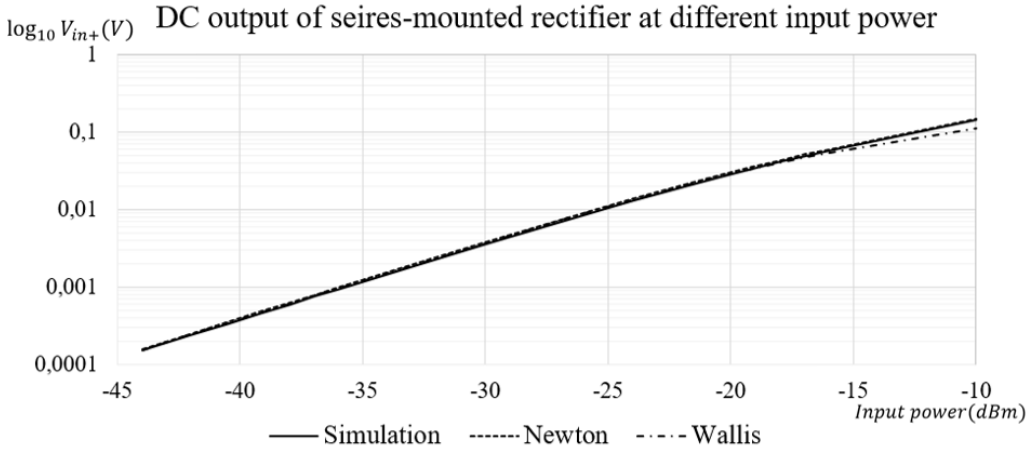


Figure 3.8 V_{in+} as a function of input power for series-mounted topology

To evaluate the performance of the three methods, their execution times are measured. This is achieved utilizing the chrono library in C++. Table 3.3 shows the execution times required by each method to compute 200 values, ranging from 1mV to 200mV.

Table 3.3 Comparison of execution time of three methods for computing 200 values

Methods	**Execution time**
[11]	201365μs
Newton	151103μs
Wallis	135283μs

III.4.2 Modeling of shunt-mounted topology

The circuit diagram of the shunt-mounted topology is shown in Figure 3.9. As in the previous series-mounted topology, $V_p \sin(2\pi ft)$ represents the AC component of the input voltage. When $V_p \sin(2\pi ft)$ is negative, the diode conducts and clamps the blocking capacitor close to zero. And then, the L-C filter remove the AC component of the output, similarly to the series-mounted topology. This assumption will be demonstrated in the subsequent calculation.

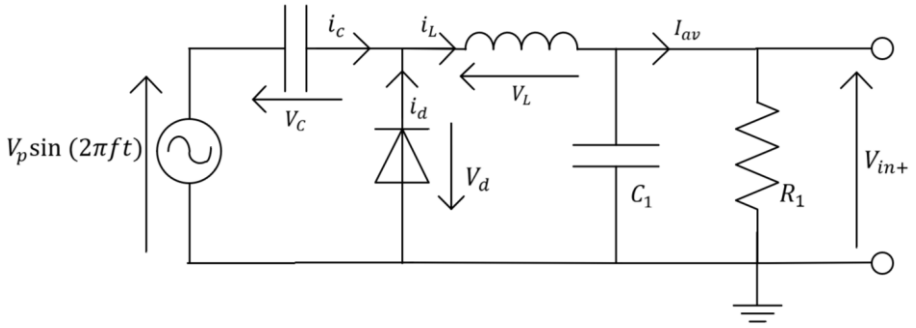


Figure 3.9 The electrical circuit of a shunt-mounted diode rectifier

A simple analysis of the circuit results in the following equations:

$$i_L = i_C + i_D \tag{3.27}$$

$$V_d = V_c - V_{in+} \tag{3.28}$$

The voltage across the DC blocking capacitor can be expressed as the sum of its DC and AC components, which can be represented by the equation:

$$V_C = V_{c\_DC} + V_{c\_AC} \tag{3.29}$$

The DC component of V_C is equal to the negative output of the rectifier $-V_{in+}$. Furthermore, based on the inference and equation provided in [16], the AC component is equal to the magnitude of the ripple voltage. Thus, the equation of V_C can be expressed as:

$$V_C = -V_{in+} + \frac{V_{in}}{\sqrt{1+(R_g 2\pi fC)^2}} \tag{3.30}$$

Here, R_g represents the internal resistance of the input source, simulating the characteristic impedance of the antenna which is 50 ohms. Moreover, our operating frequency is 868MHz, and the value of the capacitor is 100pF. Due to $(R_g 2\pi fC)^2 \gg 1$, the expression of AC part is close to 0. Thus, we have:

$$V_C = -V_{in+} \tag{3.31}$$

$$V_d = -V_{in+} - V_p \sin(2\pi ft) \tag{3.32}$$

The equation for the current at the output node is:

$$i_L = C\frac{dV_c}{dt} + I_{sat}[exp\frac{V_d}{V_T} - 1] \tag{3.33}$$

Since the output exhibits a periodic characteristic and the capacitor does not consume energy, the term corresponding to the capacitor equals zero.

$$i_L = I_{sat}[exp\frac{-V_p \sin(2\pi ft) - V_{in+}}{V_T} - 1] \tag{3.34}$$

$$I_{av} = \frac{1}{T}\int_0^T I_{sat}\left[\exp\left(\frac{-V_p \sin(2\pi ft) - V_{in+}}{V_T}\right) - 1\right] dt \tag{3.35}$$

$$I_{av} = \frac{I_{sat}}{T}\int_0^T \exp\left(-\frac{V_p \sin(2\pi ft)}{V_T}\right)\exp\left(-\frac{V_{in+}}{V_T}\right) dt - I_{sat} \tag{3.36}$$

Similar to the computation method used in equation (3.26), we expand the first exponential term in equation (3.42) using the Taylor series as shown in equation (3.27). Then, we have:

$$I_{av} = \frac{I_{sat}}{T}\int_0^T \sum_{n=0}^{\infty}\frac{1}{n!}\left(-\frac{V_p \sin(2\pi ft)}{V_T}\right)^n \exp\left(-\frac{V_{in+}}{V_T}\right) dt - I_{sat} \tag{3.37}$$

As we are only computing for the positive half cycle (where n=2m), the negative sign in the first term in (3.37) can be disregarded. It is worth noting that equation (3.37) is identical to the one used in the series-mounted rectifier topology (equation (3.22)). Therefore, the results obtained from the shunt-mounted topology are the same as those from the series-mounted topology.

And then, we can apply either the Newton or Wallis method for calculations, which is identical to the approach used in the series-mounted topology. Figure 3.10 shows V_{in+} as a function of input power in the shunt-mounted topology, comparing the results obtained from Newton's method, Wallis' method, and the SPICE simulation.

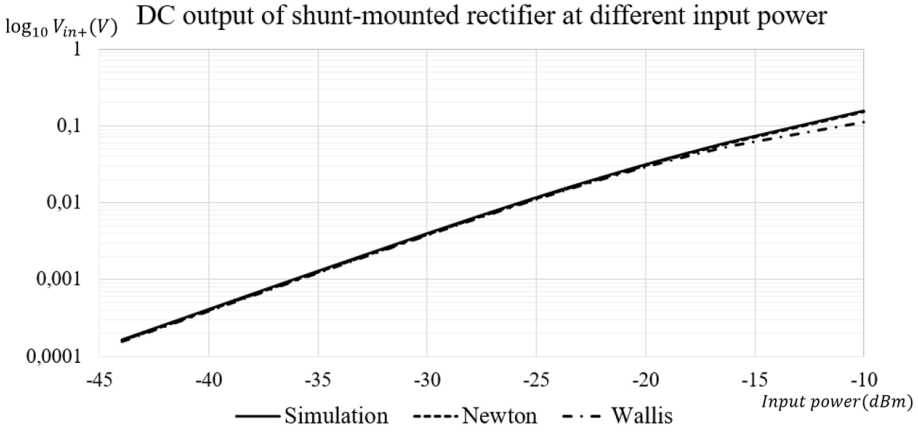


Figure 3.10 V_{in+} as a function of input power for shunt-mounted topology

III.4.3 Modeling of voltage-doubler topology

This part will transition to an examination of the voltage doubler rectifier, as illustrated in Figure 3.11. The various assumptions and conditions apply in this analysis are identical to those established in the discussion of the single-diode topology. Here, the computation of the output voltage as a function of input power for the voltage doubler rectifier will be explored.

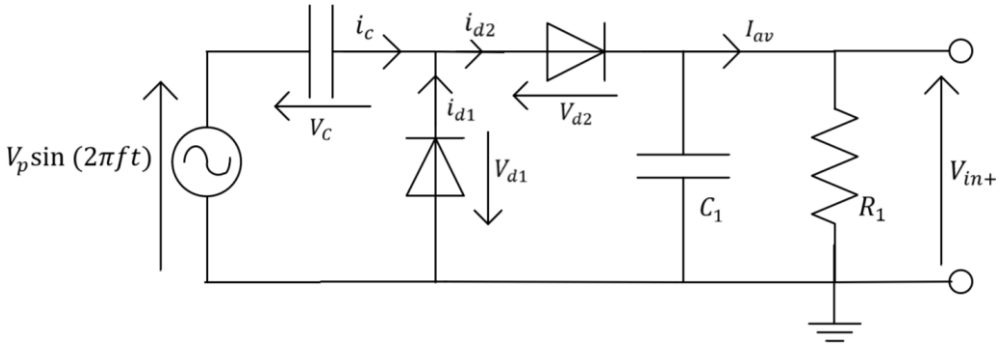


Figure 3.11 The electrical circuit of a voltage doubler diode rectifier

Given the periodicity of the output of rectifier, the average current flowing through diode D_2 per cycle should be equivalent to the average current flowing out of the output node:

$$I_{av} = \frac{1}{T}\int_0^T I_{sat}\left[\exp\left(\frac{V_{d2}}{V_T}\right) - 1\right] dt \tag{3.38}$$

Furthermore, under the assumption that the extra DC voltage drop induced by the capacitive equivalent load is fully filtered out, along with the entire output ripple, the DC voltage present on each diode within the voltage doubler rectifier circuit would remain identical. The value observed on each diode is defined as follows:

$$V_{d1} = V_{d2} = V_p \sin(2\pi ft) - \frac{V_{in+}}{2} \tag{3.39}$$

By substituting equation (3.39) into (3.38), we can obtain:

$$I_{av} = \frac{1}{T}\int_0^T I_{sat}\left[\exp\left(\frac{V_p \sin(2\pi ft) - \frac{1}{2}V_{in+}}{V_T}\right) - 1\right] dt \tag{3.40}$$

Similarly, equation (3.40) can be solved using either the Newton or Wallis method. Figure 3.12 illustrates a comparative analysis of V_{in+} as a function of input power in the voltage doubler topology. The comparison includes results from Newton's and Wallis' methods, as well as the SPICE simulation.

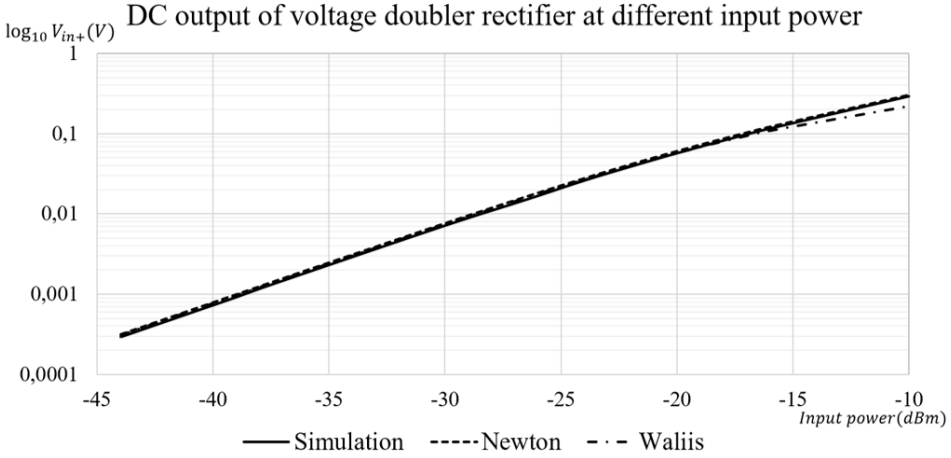


Figure 3.12 Vin+ as a function of input power for voltage doubler topology

III.5 Modeling of semi-active wake-up radio's analog part

This section focuses on the modeling of the analog part of a semi-active WUR, exclusive of the rectifier. In the following part, we will discuss the various circuit characteristics, and their effects on the performance of the WUR, providing a comprehensive understanding of the analog circuits.

III.5.1 Comparator

The most critical parts for accurate modeling are the comparator offset and propagation delay which are already shown in section III.2.1; both of these parameters can greatly affect the overall sensitivity of the device in some working conditions. The electrical delay is due to the low-pass filters inherent to the comparator topology and the wake-up topology as well. The minimal delay across the structure is the maximal value of the comparator internal delay and the delay due to the low-pass filters. It is not clear before designing the wake-up radio which one will be predominant. So, the electrical simulation of the device has to be run in order to refine the modeling of the delay.

As for the reference generator, a RC integrator is used to generate an adaptive threshold, which is theoretically held at 50% of the level of V_{in+}. The transient response, required for the capacitor to charge halfway is equivalent to approximately 0.7τ considering the following equation:

$$V_{in-}(t) = V_{in+} \cdot (1-e^{-\frac{\tau}{RC}}) \quad (3.41)$$

Then, the comparator compares the two input values, taking into account the effects of delay and offset.

III.5.2 Wake-up interrupt / preamble detector

The preamble detector that we use is also an RC integrator with a lower cut-off frequency, which has the same equation as (3.41). It sends an interrupt to wake up the PIC. The formula for calculating the lower limit of the TTL input high level V_{IH} is as follows [17]:

$$V_{IH} = 0.25 * V_{DD} + 0.8 = 1.55V \quad (3.42)$$

With a high level of comparator's output V_{DD} of 3V.

Besides, the output of the RC integrator increases exponentially as the capacitor charges at a rate determined by the time constant τ. Thus, with T_{bit} representing the period of 1 bit, after at least 0.7*τ (τ = 0.462ms in this case, cf. interrupt to PIC in Figure 3.13), the output of the RC integrator can reach the lowest value of V_{IH}, which is at least 2.6*T_{bit} (T_{bit} = 125µs). Hence, in the calculation, we need to consider whether the duration of the preamble can exceed 2.6*T_{bit}, when the comparator overcomes the offset and delay then outputs the high level, and when the output of preamble detector reaches V_{IH}. Additionally, we also need to evaluate whether the remaining preamble duration after sending an interrupt is sufficient to cover the wake-up time of the PIC. Figure 3.13 presents data out from the comparator and the preamble detector.

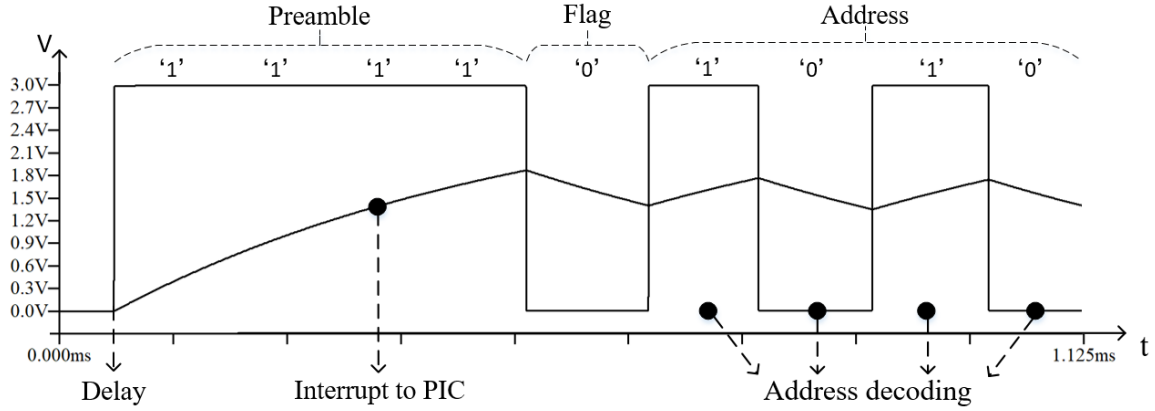


Figure 3.13 The output of the comparator and the preamble detector

III.6 Modeling of semi-active's digital part

After the modeling of the analog components, we now turn our attention to the digital aspects of the system. The digital part is the PIC module, which is essential for evaluating received messages. It classifies them as either noise or signal and calculates binary errors. A correctly designed WUR is triggered only upon receiving a specific code. However, in certain situations, random noise within the radio may cause the RC integrator to interrupt, causing to a false wake-up. This can lead to unnecessary uptime for the receiver and a waste of energy. However, we have to consider the power consumption of the PIC module during different stages. In sleep mode, the PIC consumes as low as 60nW, while during data processing, the power consumption increases to 234µW.

The wake-up time for addressing is directly proportional to the length of the address and the data rate. It is determined by the packet propagation delay. In addition, the message contains a 4-bit preamble, a 1-bit flag code, and a 4-bit address of the main radio. The packet delay is calculated in the following formula:

$$Packet\ delay = N_{bits} * T_{bits} \tag{3.43}$$

Where N_{bits} is the number of bits used for the address.

If the PIC is woken up, it reads the output of the comparator and waits for the flag of sampling (low level). Once it detects the flag, then the PIC starts the acquisition $T_{bit}/2$ after the next high level appears, and then every T_{bit}. If the received address is correct, the PIC wakes up the main radio via an interrupt. The method of decoding the address is illustrated in Figure 3.13.

III.6.1 Transmit delay consideration

It's worth noting that, except for the delays induced by the comparator, and the PIC decoding, the signal's transmission delay and propagation delay also have to be considered. The transmission delay corresponds to the time taken by the transmitter to send out the data and it depends on the length of the data, which is equal to the packet delay in equation (3.43). The propagation delay is the time it takes for the data to travel from the transmitter to the receiver, a ratio of distance to the speed of light.

Table 3.4 provides an example of the delays involved in the entire transmission and reception process of a wake-up packet with a length of 9 bits, over a distance of 10 meters.

Table 3.4 Examples of the delays during the entire transmission and reception process

Type	Delay time
Transmission delay	1125μs
Propagation delay	0.033μs
Comparator	60μs
Packet delay	1125μs

III.6.2 Transmit error probability (BER / PER)

A false/missed wake-up appears when the WUR cannot detect the wake-up packet due to noise or distance or when the noise causes an accidental wake-up. To model this, an additive white gaussian noise (AWGN) channel is added to the transmitted signals. The distinction of Mark (transmission of bit '1') and Space (transmission of bit '0') is based on the PIC sampling the comparator's output. To get the wake-up error probability, P_{eS} (Probability of space error) and P_{eM} (Probability of mark error) are calculated, which are the error probability for high bits to be sampled low and the error probability for low bits to be sampled high, respectively. Here, the weightage given to each type of error is represented by a coefficient α, it signifies the probability of occurrence of each error. And when we sum the probabilities of a Space error and a Mark error, the total should equal to BER. For non-coherent detection of OOK modulation with an envelope detector, the bit error rate is expressed as [18]:

$$BER = \alpha P_{eS} + (1-\alpha)P_{eM} \tag{3.44}$$

Where α is the possibility coefficient of occurrence of Space error, on the contrary, (1-α) is the possibility coefficient of occurrence of Mark error. The formula of P_{eS} and P_{eM} are given by [18]:

$$P_{eS} = exp\left(-(1+\frac{E_b}{4N_0})\right) \tag{3.45}$$

$$P_{eM} = 1 - Q(\sqrt{\frac{2E_b}{N_0}}, \sqrt{2+\frac{E_b}{2N_0}}) \tag{3.46}$$

With E_b/N_0 the energy per bit to noise power spectral density ratio, and Q(·,·) the Marcum-Q function of order one.

$$Q(a,b) = \int_b^\infty x e^{-\frac{a^2+x^2}{2}} I_0(x) dx \quad (3.47)$$

Here, $I_0(x)$ represents the zero order modified Bessel function of the first kind, which is the same equation as (3.16). And then, the false/missed wake-up probability P_{FP} is expressed as:

$$P_{FP} = 1 - (1 - P_{BER})^k \quad (3.48)$$

With k the size of the wake-up packet.

Moreover, since the offset is negative and the voltage applied to the comparator inputs are very low, it is almost impossible to misjudge bit 0 as 1. Therefore, in the theoretical model, we set the value of a to 1, neglecting the Mark error (α = 1). In addition, k is taken as the number of bits '1' present in the wake-up packet.

III.7 Implementation of different topologies of rectifier in semi-active wake-up radio

The focus of this section will be on the experimental measurements, and performance comparisons with the SPICE simulation of the wake-up radios with different rectifier topologies.

III.7.1 Experimental measurement

The prototypes of semi-active wake-up radio with three topologies (series, shunt and voltage doubler) are designed and fabricated, which are presented in Figure 3.14, with a detailed explanation of series-mounted topology prototype. Due to the lower sensitivity of the bridge topology in the SPICE simulations, it is not well-suited for ultra-low-power WUR. Thus, we choose not to fabricate a PCB for the bridge topology and instead focus on developing and measuring PCBs for the other three topologies.

The devices operate with a monopole antenna and are powered by two AAA batteries (3V), not displayed in the figure. In addition, each prototype is equipped with two LEDs that indicate when the micro-controller is awoken from sleep mode and receives the correct main radio's address, which are helpful for debugging purposes.

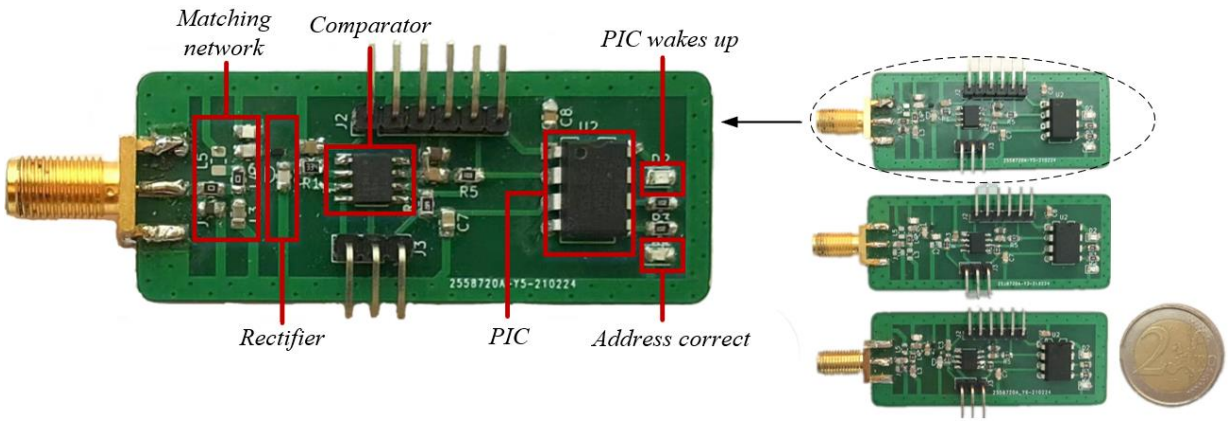


Figure 3.14 Semi-active WUR prototypes with different rectifier topologies: detailed explanation of series-mounted topology prototype

Furthermore, we employ the through-hole technology (THT) version of the PIC component in our PCB for faster and easier development. However, THT components on the PCB result in significant distributed inductance. To avoid interference with the WUR, we increase the distance between the analog section and the PIC to reduce crosstalk. Consequently, we position the PIC 20mm away from the WUR. We also respect the 3W rule, which recommends that the spacing between signal lines should be at least three times their width, to minimize crosstalk between the relatively long lines connecting the outputs of comparators and detectors to separate PIC pins [19].

For PCB development, we initially choose a 2-layer board for preliminary measurement analysis to achieve simplicity and cost reducing. To obtain good RF performance, the return path should be continuous and as wide as possible. Thus, the bottom layer is set as a complete ground plane. We form a ground fence around the RF section using vias to isolate the rest of the circuit. Decoupling capacitors are also added to the power supply to further optimize the performance. Table 3.5 displays the component and PCB design specifications.

Table 3.5 Component and PCB design Specifications

Component	**Model/Package**
Antenna	8WHIP3H-SMA
Diode	SMS7630
Comparator	TLV3491
ULP MCU	PIC12LF1552
Resistance	0805 SMD
Capacitor	0805 SMD
Inductor	0805 SMD

Parameter	**Value**
PCB layers	2-layer
PCB Thickness	1.6mm
Dielectric constant	4.5
Metal thickness	35µm
Minimum trace width	0.127mm
Minimum trace spacing	0.127mm
Drill Hole Size	0.15-6.30mm

Additionally, we reserve space for a 4-stage LC filter between the antenna and rectifier to form a matching network. When there is an impedance mismatch between the circuit and its antenna, part of the incident power from the antenna is reflected, reducing the power available for rectification. The main goal of impedance matching is to eliminate reflections of RF signals and suppress harmonic components and interference outside the working frequency. Maximum power transfer can be achieved when the load impedance is conjugate to the source impedance. In this work, the characteristic impedance of the antenna is 50 ohms.

During reception, the antenna acts as the source and the WUR as the load. So, we need to get the WUR to match with 50 ohms. We can use the Smith chart to design matching circuits by using capacitors and inductors to shift the impedance to the 50 ohms point. Simulation software can help us choose the values. However, actual component values significantly differ from simulated ones. This occurs because at 868MHz, the parasitic impedance of the trace, pad, and ground return path create an additional parasitic loop. Also, the calculated width of the 50ohms microstrip line on the 2-layer board exceeds 2.5mm [20], so we cannot use the 50ohms microstrip line for routing, thus changing the Smith diagram. Therefore, the characteristic impedance and transmission line loss can first be simulated by the software to simulate a rough impedance matching network, and then we proceed to practical “by hand” matching process. An example of adjusting a matching network using a Smith chart in a network analyzer is shown in Figure 3.15.

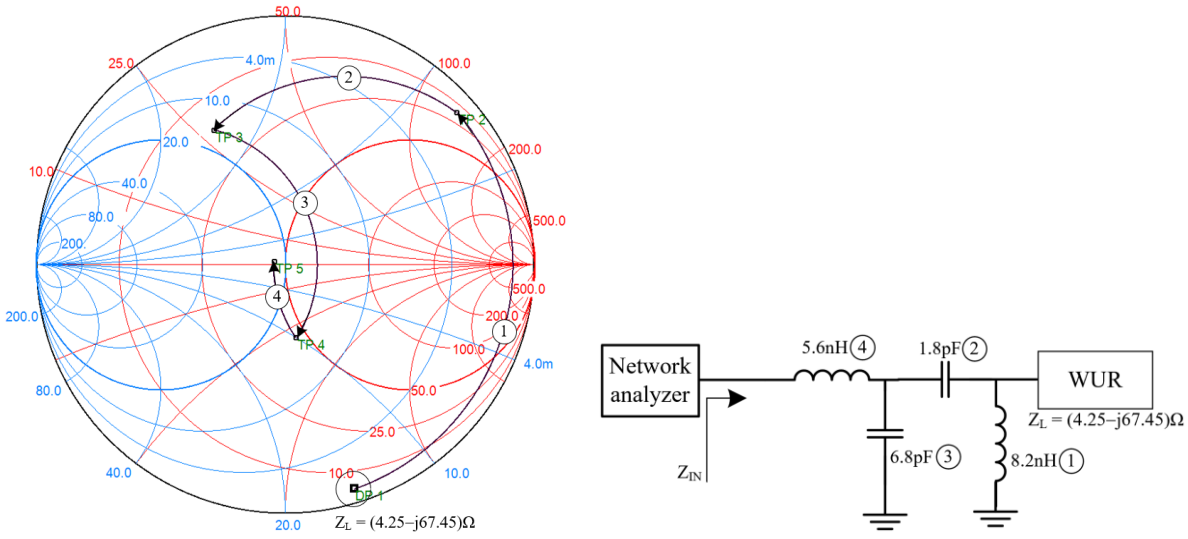


Figure 3.15 Example of tuning a matching network to achieve 50-ohm impedance by using smith chart

Here are our detailed steps for impedance matching:

1) Calibrate the network analyzer using a 3.5mm calibration kit, and determine the initial impedance value of the WUR;
2) Use Smith simulation tools to simulate matching network components and gain a general understanding of the component value range;
3) With the help of a network analyzer, perform impedance transformations using multi-stage L-C components to achieve 50-ohm impedance.

Furthermore, to evaluate the performance of the impedance matching network, we measure the circuit's return loss (S11 parameter). Scanning the 500MHz to 1.2GHz frequency range, an example of the measurement result is shown in Figure 3.16. The circuit's return loss at 868MHz is -22.5dB, which corresponds to approximately 0.56% of the power being reflected at this frequency. This circuit ensures that most of the energy is transmitted to the rectification circuit at 868MHz, achieving good impedance matching network performance and meeting our requirements.

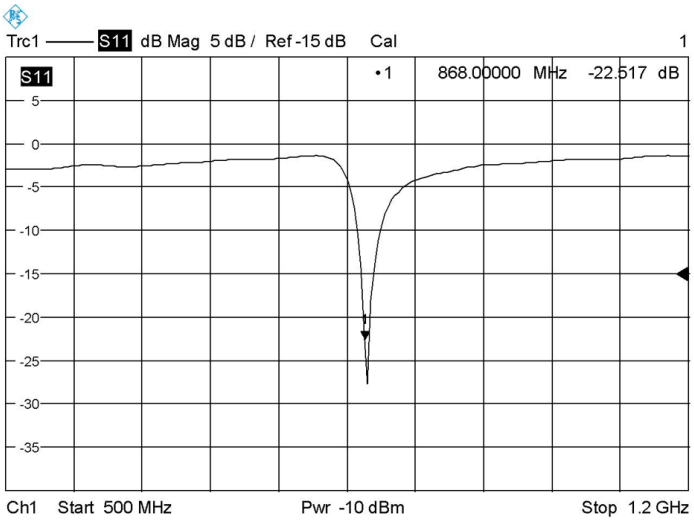
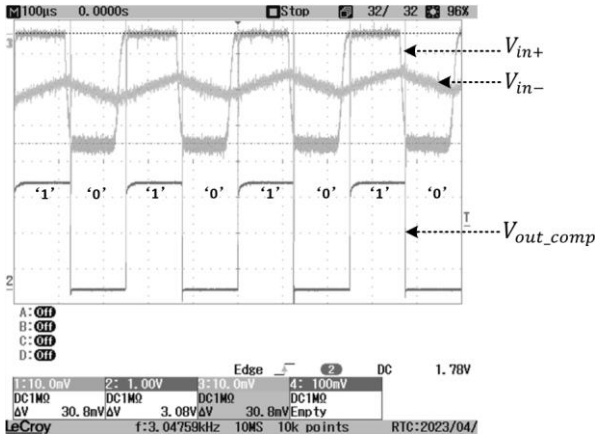
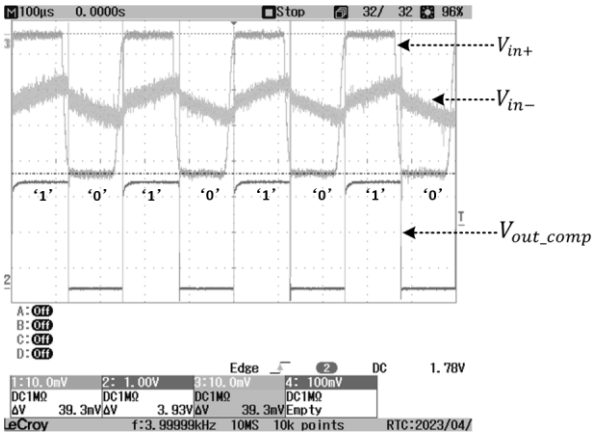


Figure 3.16 Example of return loss of a 2-layer prototype

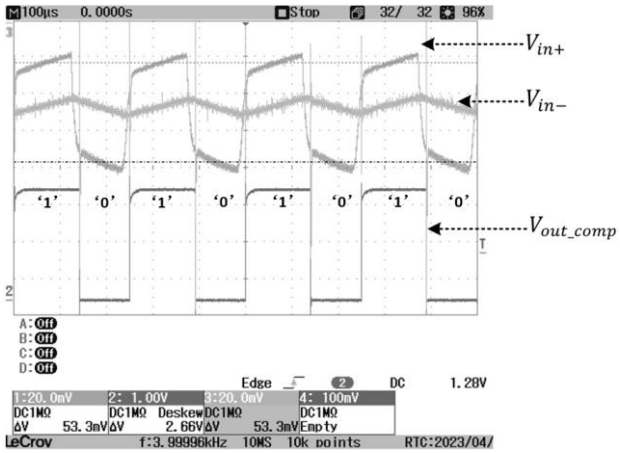
We then proceed to measure the prototypes, an OOK modulation at 868MHz is generated with a Tektronix AWG7102. The device's characteristics such as maximum transmission distance, sensitivity, and consumption are measured, with the transmit power at +10dBm and the data rate at 8kbps. The measurements of comparator input and output voltages at an input power of −25dBm are presented in Figure 3.17.



(a) WUR with series-mounted rectifier topology



(b) WUR with Shunt-mounted recitifer topology



(c) WUR with voltage doubler rectifier topology

Figure 3.17 Comparators' input and output measurements of each WUR prototype @-25dBm input power

Table 3.6 shows the measurement results of three prototypes of WUR with different rectifier topologies. Although the output of the voltage doubler is higher, it has to overcome twice the diode loss. As a result, its sensitivity is not as low as that of the mono-diode topologies. Moreover, the shunt-mounted topology of the WUR has better sensitivity than the series-mounted one, because its rectifier is measured a higher DC voltage. A higher DC voltage means a greater signal strength that the WUR can receive, allowing the WUR to work reliably at lower signal strengths, thereby increasing its sensitivity. It's worth noting that, in ideal circumstances, these two types of rectifiers would have similar RF-DC performance. However, due to differences in circuit implementation, layout design, and the influence of the matching network, this is not the case in practical situations.

Table 3.6 Measurement results of three prototypes

Topology	Parameter					
	Sensitivity (dBm)	***Maximum distance(m)***	***Consumption (nA)***	***Comp_offset (mV)***	***Output of rectifier @-25dBm (mV)***	***Noise (dBm)***
Series	–33.33	8.05	700	2.71	30.8	–67.45
Shunt	–35.54	10.38	700	2.67	39.3	–67.45
Doubler	–30.89	6.08	700	3.11	53.3	–67.45

By varying the input power, the DC output voltage of the rectifiers are measured using an oscilloscope. The measurement results are illustrated in Figure 3.18, which shows that the observed voltage levels closely resemble the simulation results.

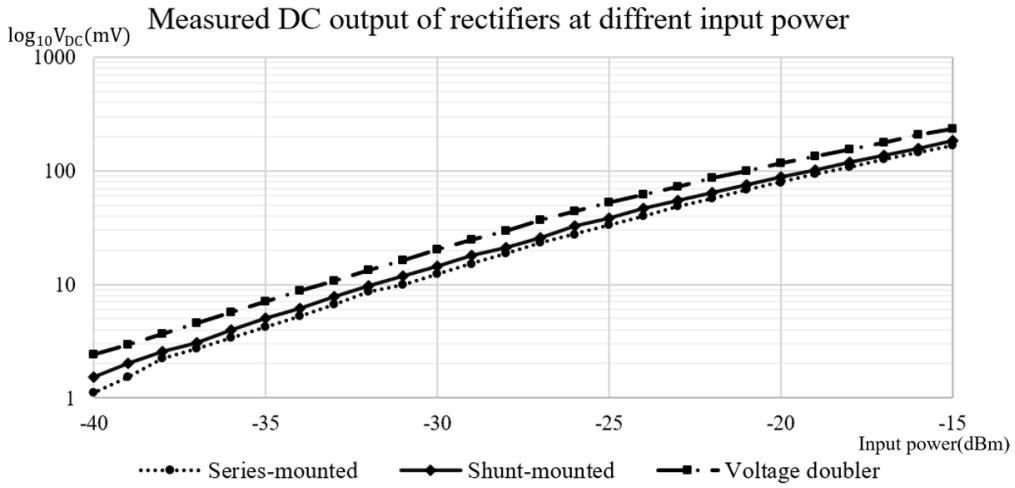


Figure 3.18 Measured DC output of rectifiers at different input power

Furthermore, to evaluate the false wake-up of each WUR prototypes, we sent 100 times a wake-up packet for a fixed distance, and repeat the measurement for the distance varying from 5 to 8.5m, with the transmit power equal to +10dBm. And then we measure the number of times that the PIC did not generate a wake-up signal, which represents the probability of false wake-up. We found that at smaller distances, WUR is generally awakened, and its false wake-up can be ignored. At higher distances, the WUR never wakes up. Therefore, the points with false wake-up probability can be measured around its sensitivity.

To fit a curve to these measured false wake-up points, we adopt the error function. According to the Central Limit Theorem: under appropriate conditions, the mean of a large number of mutually independent random variables converges to a standard normal distribution

[21], so the Continuous Uniform Law can be used. The error function is the cumulative distribution function of the Gaussian distribution, making it suitable for handling data that is normally distributed. The error function, denoted by erf, can be defined as:

$$erf(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt \tag{3.49}$$

We can change integration variable by $t^2 = z^2/2$. Since t is not negative, so that $t = z/\sqrt{2}$. we have:

$$erf(x) = 2\left(\frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x\sqrt{2}} e^{-z^2/2}\, dz - \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{0} e^{-z^2/2}\, dz\right) \tag{3.50}$$

The integral in the above equation (3.8) is recognized as the cumulative distribution function (CDF) for a standard normal distribution, typically denoted as Φ(x):

$$\Phi(x) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x} e^{-z^2/2}\, dz \tag{3.51}$$

Specifically, we can use this integral form of Φ(x) to express the error function:

$$erf(x) = 2\Phi(x/\sqrt{2}) - \Phi(0) = 2\Phi(x/\sqrt{2}) - 1 \tag{3.52}$$

$$\Phi(x) = \frac{1+erf(x/\sqrt{2})}{2} \tag{3.53}$$

For a generic normal distribution with mean distance μ_d, and deviation σ_d, the cumulative distribution function (CDF) [22] related to the error function is defined by:

$$\Phi(d) = \frac{1}{2}\left(1 + erf\left(\frac{d-\mu_d}{\sigma_d\sqrt{2}}\right)\right) \tag{3.54}$$

We apply this statistical model to determine the probability of a false wake-up as a function of transmit distance. And then we import the data and perform a nonlinear fit via the least squares method. For example, as for the WUR with series-mounted rectifier topology, we find the equation of false wake-up within the range of 5 to 8.5m. The objective of this fitting process is to identify two parameters, μ_d and σ_d, which stand for the mean and standard deviation of the fitted normal distribution, respectively. As a result of the minimization of the total squared error in the fitting process, the values of μ_d and σ_d are found to be 6.26m and 0.87m, respectively. Figure 3.19 illustrates the measuring points and the fitted curve of CDF for WUR with series-mounted rectifier topology.

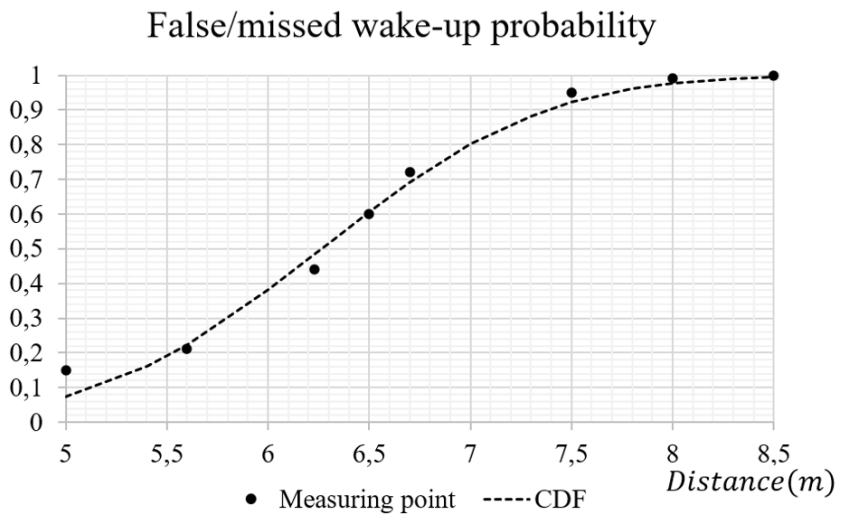


Figure 3.19 False wake-up probability as a function of distance for WUR with series-mounted topology

By using the same approach, we establish the fitted curve of the CDF for the three prototypes of different topologies. Figure 3.20 compares the false wake-up probability as a function of distance for these prototypes.

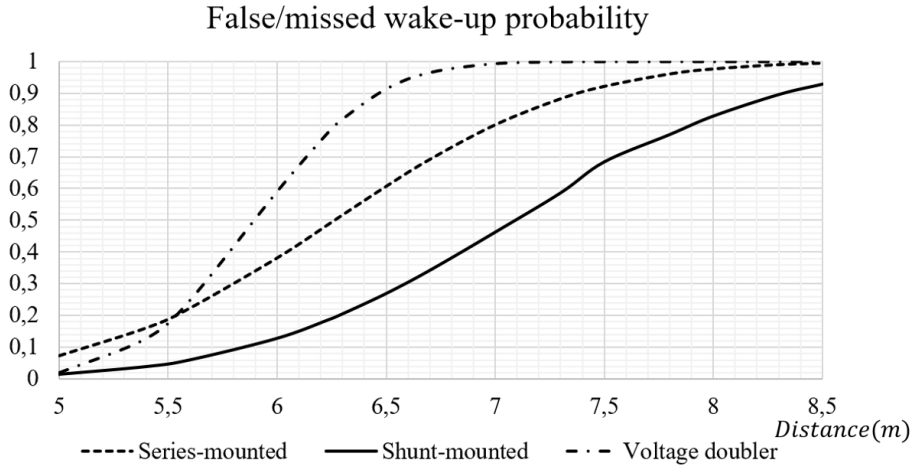


Figure 3.20 Comparison of false wake-up probability as a function of distance for different topologies

To illustrate the impact of different addresses on sensitivity, as an example, we test the sensitivity of three different addresses for the series-mounted topology WUR, along with their corresponding distances at a transmission power of +10dBm. The test results are shown in Table 3.7, which demonstrate the sensitivities for these three addresses. This variation can be attributed to several factors, such as the comparator's offset and the delay of both the comparator and PIC.

Table 3.7 Measured sensitivity and corresponding distance of three different addresses at +10dBm for series-mounted topology WUR

Address	Measured sensitivity	Corresponding distance@+10dBm
0b1010	–33.33dBm	8.06m
0b1100	–33.12dBm	7.86m
0b1111	–32.76dBm	7.54m

III.7.2 Results comparison with SPICE simulation

Table 3.8 shows the comparison of the measured and SPICE simulated results for three rectifier topologies of WUR, where the difference between the measured and simulated sensitivity mainly come from the uncertainty on the voltage offset in the comparator, that cannot be known precisely before the measurements.

Table 3.8 Comparison of results of measurement and SPICE simulation

Parameters	Series-mounted		Shunt-mounted		Doubler	
	Measure	***SPICE***	***Measure***	***SPICE***	***Measure***	***SPICE***
Sensitivity (dBm)	–33.33	–42.76	–35.54	–44.1	–30.89	–42.95
Maximum distance (m)	8.06	23.8	10.38	27.9	6.08	24.4
Output of rectifier@–25dBm (mV)	30.8	10.89	39.3	11.48	53.3	17.27
Comparator_consumption (nA)	700	835	700	835	700	835
Comparator_offset (mV)	2.71	0.084	2.67	0.084	3.11	0.084
Noise (dBm)	–67.45	–70	–67.45	–70	–67.45	–70

III.8 Conclusion

In this chapter, we give the detailed process of SPICE simulation, development of a theoretical model, as well as the prototype design and measurement for a semi-active wake-up radio.

We simulate the performances of four semi-active WUR topologies in terms of sensitivity, SNR, and RF to DC conversion. Our studies emphasize the sensitivity decrease as a function of the number of active devices (diodes), and depict the variation of the DC voltage for each topology.

Following the simulation, the theoretical model is developed, which can save significant time in prototype realization and measurement. It can effectively estimate and optimize circuit performance. However, while the theoretical model provides a starting point, there are many practical factors that can impact system performance, necessitating a careful consideration through experimental measurement. And we also consider the issues of false wake-up and delay to quantify robustness, which is important to optimize the system performance.

We then proceed to design and measure the semi-active WUR with three topologies of rectifier. We provide the detailed description of designing and measuring the prototypes. Furthermore, the results of measurements and SPICE simulations are compared.

III.9 Reference

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Chapter IV: Optimization and hardware integration of nodes with wake-up radio for wireless sensor network applications

IV.1 Introduction

In this chapter, we concentrate on the optimization of the semi-active wake-up radio system. This chapter is partitioned into three sections that each approach the optimization process from different perspectives.

The first part compares the performances of the semi-active wake-up radio using two different integration approaches: a heterogeneous fabrication, combining PCB and integrated CMOS; and a more classical PCB integration. The critical and most consuming part of the device is designed on purpose by using a CMOS integrated technology, based on the g_m/I_d methodology, to improve the sensitivity and reduce the overall consumption of the device. SPICE results are provided, including worst case and Monte-Carlo simulations.

Next, the focus shifts towards the optimization of the WUR prototypes. This section explores the process of designing the 4-layer PCB, comparing the performance before and after optimization. Additionally, it provides a summary of the design rules followed during optimization.

The final part of this chapter presents the development of a prototype of an Arduino shield equipped with an optimized 4-layer WUR, main radio, and other sensors. This section details the entire process from shield design to realization. We then provide the test of the WUR system and analysis of the collected data, providing a comprehensive overview of the practical implementation process.

The remainder of this chapter is organized as follows: Section IV.2 presents the design and implementation of the heterogeneous semi-active wake-up radio using two different integration approaches. Section IV.3 provides an in-depth look into the optimization process of WUR prototypes, discussing the design rules and the comparative results. Section IV.4 discusses the

development of an Arduino shield prototype, from design to the measurement. Section IV.5 concludes the chapter.

IV.2 Design of heterogeneous semi-active wake-up radio

In chapter III, we presented the off-the-shelf semi-active WUR and compared the experimental results and the SPICE simulations. Our prototype achieves the static power consumption of 700nA and the sensitivity of −33.33dBm (example of series-mounted rectifier topology). We found that the difference between the measured and simulated sensitivity mainly comes from the uncertain voltage offset of the comparator, which is measured equal to 2.7mV. Moreover, the comparator is the only analog active part in the circuit. Thus, it makes sense to design a heterogenous wake-up radio composed of PCB analog circuits, which will be more robust to components matching and integrated CMOS comparator optimized in terms of sensitivity and consumption. In this section, we will provide the design process of a simple solution to optimize the wake-up radio circuit with given design specifications.

IV.2.1 g_m/I_d design methodology

To design integrated circuits such as a low-power comparator, the g_m/I_d method has been used for several decades with satisfying results. In classical MOS circuit design, its mathematical analysis is generally based on a square-law model of drain current versus gate-source voltage [1]. The circuit needs to be biased in the strong inversion region. Also, the model assumes that when the overdrive voltage V_{ov} is negative ($V_{ov} = V_{gs} – V_{th} < 0$), the current is zero. However, the g_m/I_d method is based on the fact that, in a MOS transistor, a drain current still exists in the weak and moderate inversion regions, where the gate-source voltage can be lower than the threshold voltage and as the gate-source voltage increases, the drain current increases as well. Additionally, it is found that operating below strong inversion region can bring advantages such as higher gain, lower power consumption and less harmonic distortion [1]. Therefore, more and more low-power designs bias the transistor below strong inversion. The resulting high gain and low power consumption, which are the most important considerations for the comparators in wake-up radio, prove to be better than those obtained with general

purpose chips for this application.

To ensure that the required specifications are met, multiple trade-offs must be considered during the design of the comparator. The g_m/I_d ratio reflects the efficiency of converting the current (or power) consumption into transconductance [2]. For a given technology process, when gm/Id increases to a certain value, the MOS works below strong inversion, then the circuit has higher intrinsic gain, lower power consumption, and minimum gate equivalent thermal noise, but the speed and matching are worse [3]. Conversely, when the g_m/I_d value is small, the circuit has a high speed, but a low intrinsic gain, and a large power consumption. The speed-efficiency trade-off is shown in Figure 4.1.

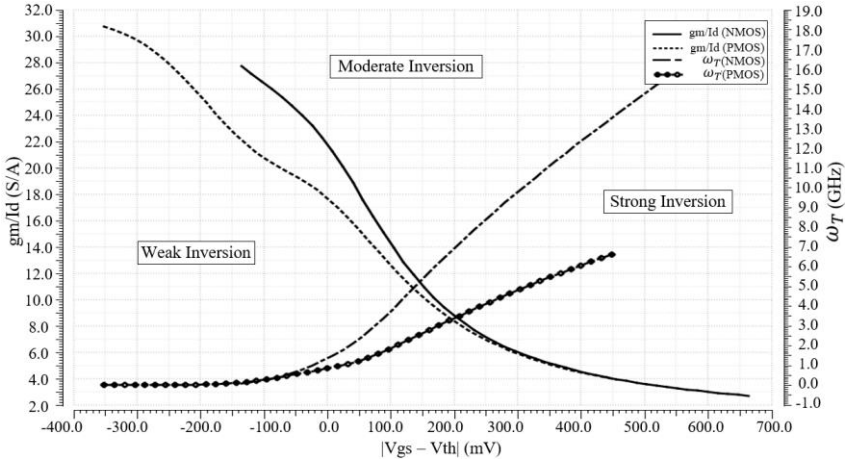


Figure 4.1 Speed-efficiency tradeoff of NMOS and PMOS with W/L = 10µm/1µm on AMS 0.35µm technology

At the same time, the larger length (L) transistor has a larger gain, a better matching, but a smaller bandwidth. Therefore, when determining the size of the device, it is necessary to make a trade-off between intrinsic gain, power consumption, speed, noise, and device area according to one's needs.

IV.2.2 Purpose-designed CMOS comparator

This part presents the design process of the comparator to meet the WUR's specifications. The proposed comparator is designed and simulated with an AMS 0.35µm CMOS technology. Figure 4.2 shows the electrical circuit of the open-loop comparator, which includes a differential pair (M1, M2), a common-source amplifier (M7), and a CMOS inverter (M8, M9). The other transistors are used for bias purpose.

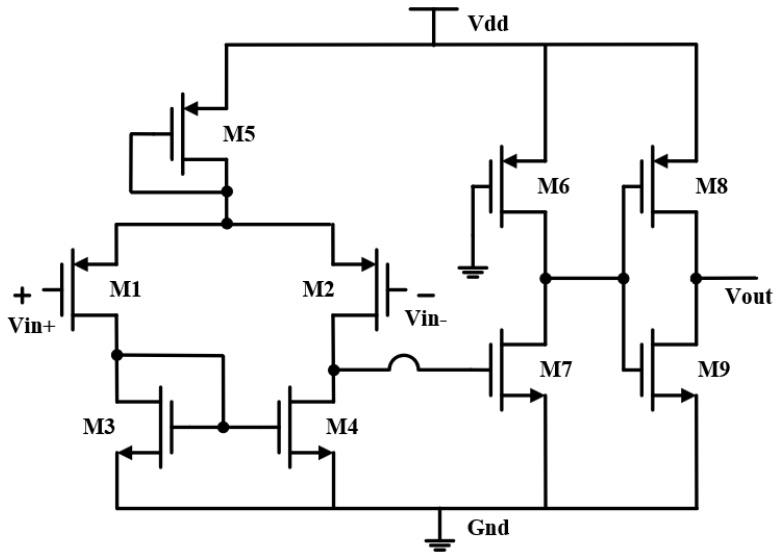


Figure 4.2 Electrical circuit of the CMOS open-loop comparator

Design considerations

The main objective of our optimization is to obtain the best sensitivity with a suitable slew rate and a similar power consumption to the commercial comparator TLV3491 that we are using. By applying a classical operational amplifier architecture is an excellent and simple way to obtain a high-gain, low-offset, open-loop comparator [4]. The static power consumption of the comparator is set to at most 700nA in the worst case to match the TVL3491 characteristics. As for the gain, when WUR reached its maximum sensitivity, the output voltage of the rectifier is tested to be 6.16mV. Therefore, the comparator needs to switch to high-level output voltage when the input voltage is as low as a few millivolts. Next, we will give the design process of the first stage in detail.

Table 4.1 CMOS comparator design specifications

Specifications	Value
Technology	0.35μm
Power supply	3V
Current Consumption	700nA
Slew rate	1V/μs
Input voltage range	0~750mV
Input voltage resolution	1mV
Gain	70dB

Design of the PMOS differential pair

The first step is to choose the type of the input pair (M1, M2). As for the NMOS input pair,

the minimum input voltage is given by the sum of the gate-source voltage (V_{GS}) across the input pair and the overdrive (V_{ov}) of the current source. Although it has higher g_m under the same area, it cannot be well biased in saturated region because our input is too small. Therefore, we choose PMOS input pair, which has the advantage of a smaller noise figure, so they generate less noise at lower frequencies than NMOS [3]. Moreover, having PMOS input pair can make the second stage an NMOS common source amplifier, so that its gain can be maximized (the g_m of NMOS is larger under the same current and size). In this way, it is possible to reduce the number of stages, which lowers consumption and area. As depicted in Figure 4.2, the first stage consists of an input pair (M1, M2), a current mirror active load (M3, M4) and a current source M5. For matching constraints, M1=M2 and M3=M4.

Input pair(M1,M2): Since the input is very small, the first stage has a higher impact on the overall system offset than the later stages. At this point, a large gain of the first stage is needed. In addition, the standard deviation of matching error is usually inversely proportional to the size of the transistor [3], so the minimum size of MOS should not be taken. And then, the greater the gain of the first stage, the smaller the input-referred offset [5]. The gain of the input pair is:

$$A_1 = -\frac{g_m}{g_{dsn}+g_{dsp}} \tag{4.1}$$

Where g_m is the PMOS transistors transconductance and $g_{dsn/p}$ is the equivalent conductance introduced by channel length modulation of the n/p transistor, which increases with the increase of channel length L. Hence, we can have a big gain by picking a large g_m/I_d or large L. Moreover, the noise is inversely proportional to g_m [3], so a large g_m/I_d needs to be chosen to reduce noise. However, g_m is constrained by speed. The slew rate and g_m/I_d ratio are inversely related for [6]:

$$SR = \frac{\omega_T}{g_m/I_d} \tag{4.2}$$

Where ω_T is the transition pulsation of the transistor.

Firstly, we specify the current for the input pair. Considering that the last stage needs to drive a RC integrator, it requires more consumption. Therefore, each pair is biased to get a current of 100nA. Secondly, we need to find appropriated g_m/I_d and L. The curve of the ω_T as a function of g_m/I_d is simulated, we choose $(g_m/I_d)_{1,2}$ as big as possible that allow the slew rate to meet the requirement. Then $(g_m/I_d)_{1,2}$ is taken equal to 18, and the channel length of 6μm is selected. Thirdly, we simulate I_d/W as a function of g_m/I_d curve to obtain the value of channel

width (W) equal to 4.8μm.

Current mirror transistors (M3–M4): The choice of the g_m/I_d of the current mirror load is constrained by the input voltage range and the RMS noise specifications. The following conditions must be met to make the input pair work in the saturation area:

$$V_{in,min} \geq V_{GS3,4} - |V_{GS1,2}| + |V_{ov1,2}| \quad (4.3)$$

Where $V_{ov1,2}$ is the overdrive voltage of M1 and M2. By simulating g_m/I_d as a function of $V_{GS3,4}$, it can be concluded that g_m/I_d needs to be greater than 9. Furthermore, $V_{GS3,4}$ is used to bias the NMOS in the second stage. It can be noticed that the DC operating points of M4 and NMOS of the second stage are the same. Therefore, we should also adjust the size of M3 and M4 to ensure that V_{ov} is not too large, so as to ensure a small power consumption and the saturation of the transistor in the second stage. Hence, we make M3 and M4 operate in moderate inversion to guarantee good matching and noise properties as well, which leads to g_m/I_d ranging between 15.8 and 21. However, the transistors are used as a current mirror, which has an output noise proportional to gm. In order to have smaller current noise, we take the value of g_m/I_d equal to 16.5.

Current source (M5): The PMOS current source is used to distribute the current and balance the operation of the input pair. We avoid using a current mirror to bias the current source, because a current mirror mismatch can cause both systematic and random errors in the current source, then the current I_5 produced by M5 will deviate from its nominal value [3]. Since the comparators are low-input and low-power, little deviation can cause a big impact. We finally get a self-biased PMOS current source. In addition, eliminating the current mirror can reduce power consumption of one stage. The size of M5 can be obtained from the required current value. And to limit the standard deviation of error, larger transistor sizes are needed. In the case of a symmetrical circuit, the noise on both sides will partially cancel each other out [7].

Design of the second amplifier stage

The second stage is a common-source structure, which is formed by using a current source M6 as the load and M7 as the amplifier. For current load, M6 gate is connected to the ground to avoid using current mirror. We adjust the size of M6 to have a bias current equal to 300nA.

Additionally, the total gain of the comparator is obtained by multiplying the gain of the first stage and the gain of the second stage. After completing the simulation of the first level, we find that the gain of the first level is 45dB, so it is enough for the gain of the second level to reach 25dB. As mentioned above, the V_{GS} of M4 and M7 are the same, and the corresponding g_m/I_d is about 16.5. Similarly, we determine the size of M7 through the steps in the design of the first stage.

Design of the inverter

Since the channel length modulation equivalent resistance r_{o6} in the second stage obtained is relatively large, when it is compared with the load impedance, the driving capability of the circuit will be limited in this case. In order to reduce the output resistance and increase the current driving capability, we add another stage, an inverter is a good choice, because it only consumes power during conversion [2]. Regarding the effect of size on energy consumption, the minimum sized devices is theoretically optimal for reducing energy per operation [8]. And to obtain equal rise time and fall time, we take the width of PMOS as twice that of NMOS. When it performs level conversion operation, its current consumption is simulated to be 500nA on average. The result of the transistors' sizes is presented in Table 4.1.

Table 4.2 Summary of the transistors' dimensions

Transistors	gm/Id	W(um)	L(um)	W/L
M1,2	17.8	5	6	0.83
M3,4	16.5	5	30	0.167
M5	1.78	0.6	74	0.009
M6	0.38	0.5	30	0.017
M7	16.3	0.5	1	0.5
M8	26.5	1	0.35	2.86
M9	0.8	0.5	0.35	1.43

IV.2.3 Layout of the comparator

The proposed layout is based on the common centroid (CC) technique to minimize the effect of process variations on the electrical characteristics [9], [10]. For the differential pair

(M1, M2) and the current mirror load (M3, M4), which rely on precise balance of transistor characteristics, the transistor matching is very important [11]. Thus, to reduce spatial variations and process gradients as much as possible, CC layout is applied to these two pairs. Additionally, dummy devices are added close to each transistor, to maintain a consistent environment and limit boundary-related effects [11]. Furthermore, each group of transistors is surrounded by a guard ring, which can also help to isolate different parts of the circuit and minimize interferences and external noise effects. Figure 4.3 illustrates the layout of the comparator. The core area of the comparator is 57.6 µm × 52.5 µm.

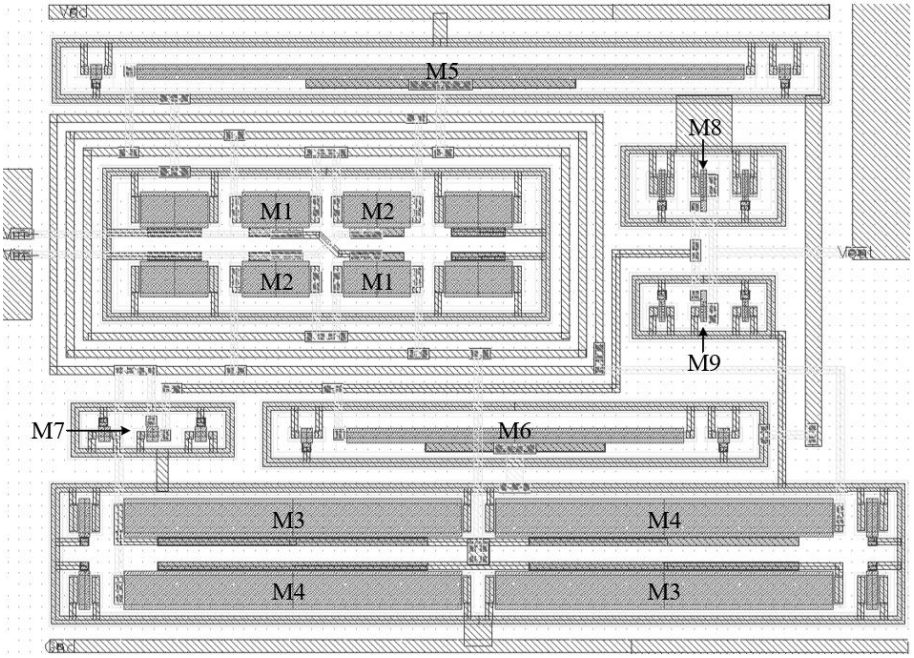


Figure 4.3 Layout of the CMOS comparator

IV.2.4 Simulation Results

This section presents the simulation results of both the comparator and the wake-up radio (electrical simulations). The electrical schematic, illustrated in Figure 4.4, features the CMOS comparator that we discussed earlier. The comparator input voltages are the rectifier's measured output voltages of a reference prototype with an input power set approximately equal to (and slightly higher than) the wake-up sensitivity. The input resistance of the ultra-low power microcontroller (ULP MCU) is also taken into account to accurately estimate the slew rate. Represented as R_3 and R_4 in the schematic, these resistors' corresponding values are measured and set to 5.2MΩ.

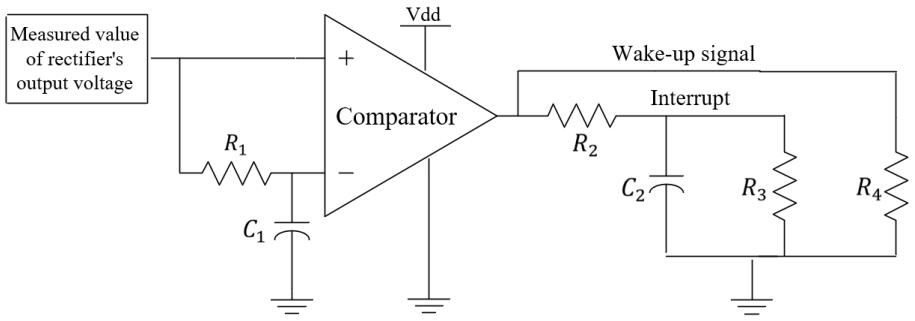


Figure 4.4 Simulated circuit schematic

Corner and Monte Carlo simulations are analyzed to assess the robustness of the comparator to process variations. The comparator's performance is evaluated under various process corners, namely Typical-Typical (TT), Fast-Fast (FF), Slow-Slow (SS), Fast-Slow (FS), and Slow-Fast (SF). The Monte Carlo simulation is run 200 times for random process values. Figure 4.5 shows the effect of process variations on the outputs of comparator (V_{out_comp}) and interrupt generator (V_{out_int}) for the input resolution voltage of 3.2mV. This process variation should be taken into account for modeling because, in practice, the acquisition time is set to half a period of the baseband signal. Therefore, if the delay caused by the process variation is higher than the quarter of a period of the baseband signal, there will be a false wake-up or a missed wake-up.

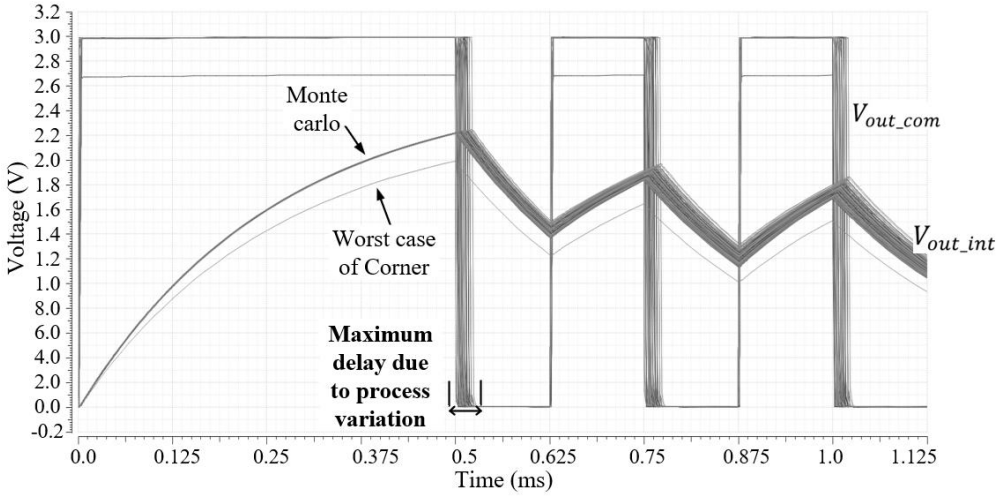


Figure 4.5 Transient simulation results of wake-up data and interrupt using Monte Carlo with 200 iterations

We also import the spice model of the TLV3491 for spice simulation and, in order to evaluate the false/missed wake-up in the circuit simulation, we generate 100 files for random gaussian white noise with different amplitudes. We then add a noise source to the input of the

circuit and record the number of times these 100 noise files caused output errors at different input voltages. Similarly, these 100 random noise files are added to the input of the CMOS comparator and the number of false wake-ups at different input voltage levels (i.e. distance) is recorded. By applying the cumulative distribution function (CDF) formula [12], we find the false wake-up probability's fitting curves for the process typical case and the worst case of CMOS comparator, respectively. Figure 4.6 illustrates the comparison of the false wake-ups probability's curves, which shows that the CMOS comparator significantly reduces false wake-ups compared to TLV3491 in both typical and worst cases.

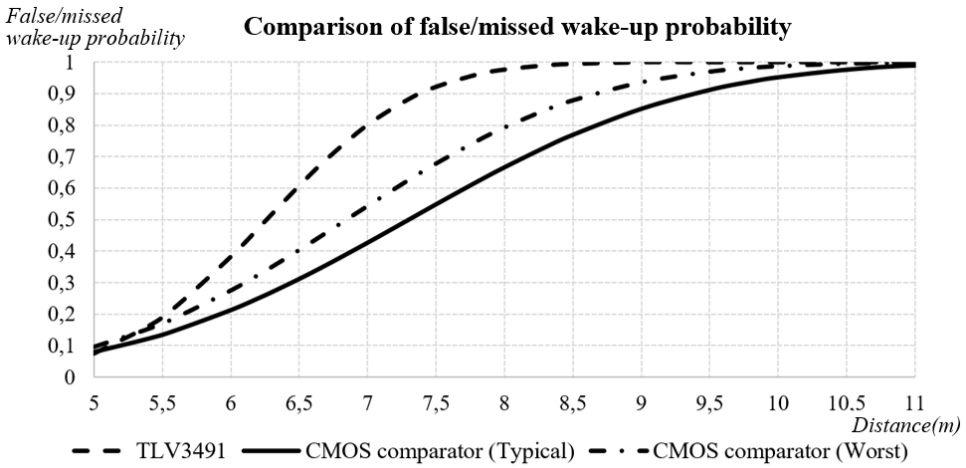


Figure 4.6 Comparison of false wake-up probability between TLV3491 and integrated CMOS comparator (typical and worst case)

Table 4.3 presents the comparison of performances between TLV3491 and the integrated CMOS comparator, revealing improvements in both sensitivity and power consumption for the two process cases.

Table 4.3 Comparison of performances: simulation result of devices using commercial component TLV3491 and CMOS comparator

Parameters	**Comparator used in wake-up device**		
	TLV3491	***CMOS comparator (Typical)***	***CMOS comparator (Worst)***
Sensitivity (dBm)	−33.3	−40	−36.1
Max distances (m) @+10dBm	8	17	11
Comsumption (nA)	800	473	652
Offset (mV)	3	0.6	1.4
Vmin of rectifier (mV)	6.16	1.1	3.2

IV.3 Optimization of semi-active wake-up radio prototypes

In this section, we focus on the optimization of the WUR prototypes. We will provide the design process for our 4-layer PCB, compare the results before and after the optimization, and a summary of the design rules that we followed during this process.

IV.3.1 Electromagnetic compatibility (EMC)

Dealing with electromagnetic interferences (EMI) is a common challenge to all electronic systems. They are characterized by electromagnetic phenomena that degrade the performance of devices. EMI can originate from the regular operation of various electronic devices or from external electromagnetic sources [13]. The electromagnetic compatibility (EMC) refers to the ability of devices to operate normally within their electromagnetic environment [14]. In this context, the robustness of a device against the EMI is significantly influenced by the quality of its PCB design.

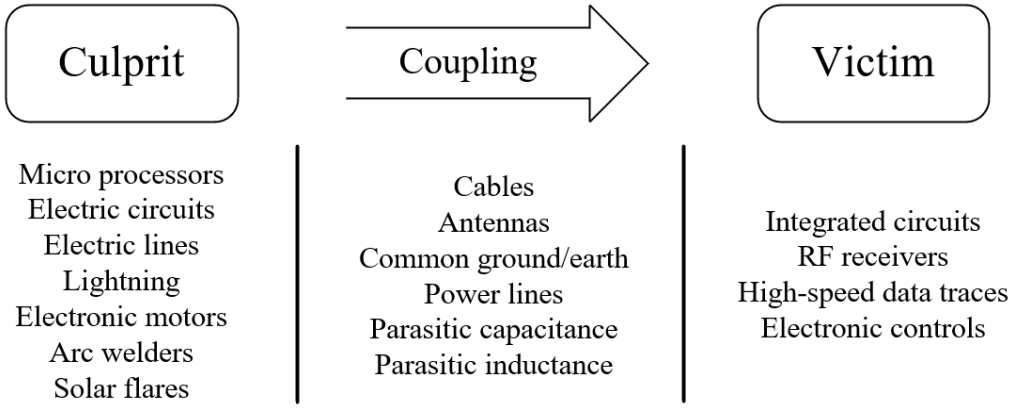


Figure 4.7 Composition of the electromagnetic interference model

Specifically, WUR is vulnerable to electromagnetic interference because they typically operate in low-power mode and transmit at relatively low power. Therefore, in the process of designing a PCB for a wake-up radio, we must fully consider EMC, combined with appropriate design strategies and layout techniques, to ensure its stable operation in various electromagnetic environments. Untreated electromagnetic interference may interfere with the reception of the wake-up signal, causing false wake-ups. Considering this issue, three key elements need to be addressed: the culprit, the coupling mechanism, and the victim, as shown in Figure 4.7. Next,

we will detail the optimization process for a 4-layer prototype, including the changes made during the optimization.

IV.3.2 4-layer prototype design

In the design of a 2-layer PCB, the distance between the signal lines and the ground plane is relatively large, leading to a weaker compensation of the return flow effect. Additionally, the current path in the grounding structure influences the electromagnetic coupling between circuits, while the size of the closed-loop area determines the intensity of radiated noise. By dedicating one or more layers for the power plane and ground plane in a multilayer PCB, the ground loop area can be reduced, and common-mode radiation and return flow impedance are lowered, thus significantly decreasing the radiation emission of a 2-layer PCB.

In our design, we adopt a signal-ground-power-ground PCB stackup, as shown in Figure 4.8. This structure allows the signal layer and power plane to be closely coupled with their adjacent ground planes. The power plane helps to reducing the voltage drop on the power lines and frees up more space on the PCB. Furthermore, the presence of multiple ground planes is beneficial as they can reduce the reference plane impedance and minimize common-mode radiation [15].

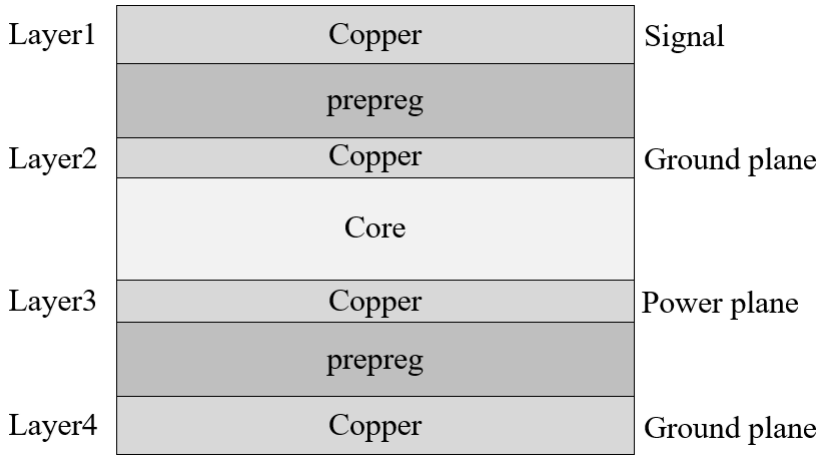


Figure 4.8 A standard 4-Layer PCB Stackup

In terms of specific design modifications, we position the connectors on one edge of the board to minimize noise and ensured the I/O connector is distanced from sensitive signals. Surface-mount components replaced the PIC's THT package to further mitigate noise. And then,

all pins from the PIC are brought out via the I/O connector, facilitating the programming. Moreover, we opt to place a button cell battery on the backside of the board, instead of using Dupont wires to connect to the AAA batteries as is done in the 2-layer board design.

To further reduce noise, we introduce densely placed ground vias on both sides along the entire path of the high-speed sensitive signal line, ensuring a robust connection with the primary ground plane. Ground vias are uniformly distributed across the entire PCB (excluding areas where power planes exist), aiming to minimize the loop area and noise to the maximum extent. Additionally, each power entry point on the PCB is connected to the ground plane through decoupling capacitors, effectively curtailing low-frequency noise on the power lines.

Figure 4.9 shows a photo of the optimized 4-layer PCB for the WUR with a voltage doubler rectifier topology, measuring 34mm*32mm. Upon testing, the sensitivity of the optimized PCB is measured to be −40dBm, which has an improvement of 10dB from the 2-layer prototype's sensitivity.

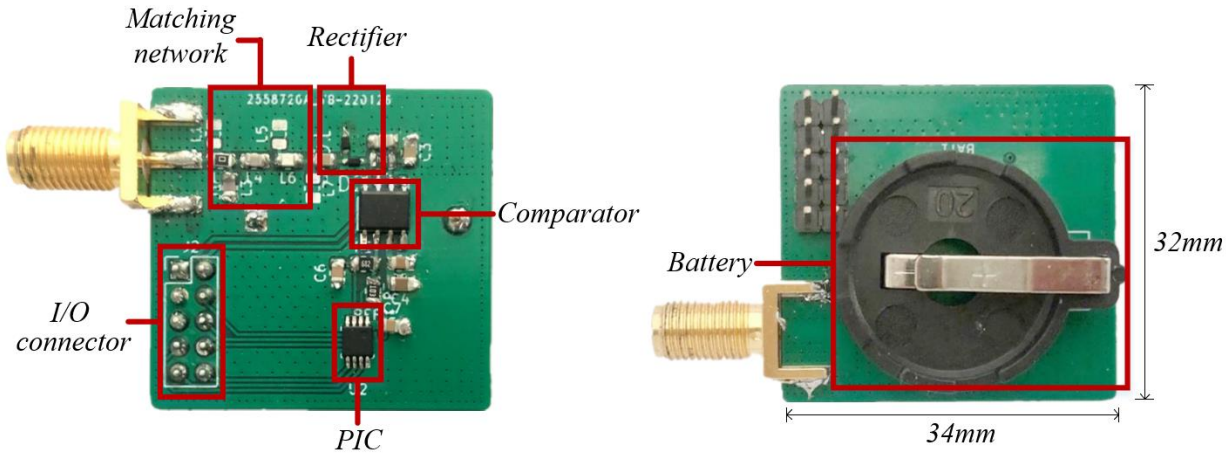


Figure 4.9 4-layer WUR prototype

IV.3.3 Summary of layout design rules

Here is a summary of rules that we adhere to while designing the layout of PCB for the wake-up radio:

(1) Multi-layer PCB structure

Single and double-layer PCBs are generally suitable for low and medium frequency circuits. However, in the RF frequency range, multi-layer boards should be considered [16].

These provide additional ground planes that significantly reduce ground impedance (noise). As the power layer and ground layer can offer the smallest loop area for the signal ground wire, multi-layer boards exhibit optimal resistance to interference. Signal layers should be tightly coupled with their adjacent planes (power or ground), and where feasible, power and ground planes should also be closely connected.

The use of a multi-layer PCB enables separation of signals and ground planes, thus reducing interference and improving signal integrity. Additionally, it facilitates optimal component and routing layout, thus reducing overall board dimensions. Different layers can be used for specific functions such as power planes, ground planes, and signal layers, which helps to better manage current and minimize ground loops.

(2) Component layout

In the design process, all circuit components should be positioned according to the functional units of the circuit [17]. The board can be partitioned based on different power voltages, digital and analog circuits, or high-speed and low-speed circuits.

It is preferable to place all connectors on one side of the board, as in the presence of common-mode radiation, cables can act as common-mode transmitting antennas. As soon as an I/O signal enters through a connector, it must immediately enter the I/O driver to avoid coupling with interference signals.

(3) Wiring layout

Avoiding long-distance parallel wiring and increasing the distance between lines can help to reduce crosstalk. It's also preferable not to cross signal lines with power lines and ground lines. Corners of lines should avoid right angles, and signal lines on different layers should be wired vertically.

High-speed signal lines, which are prone to electromagnetic interference, should be kept as close to the ground loop as possible [18]. In the case of mixed digital-analog circuits, layouts should be divided into separate analog and digital parts, each with its own wiring.

Considering the correlation between the electromagnetic radiation of the PCB and the intensity, area and frequency of the current, reducing the area of the signal loop is the key. It is important to control the area of the signal loop, placing critical signals on adjacent ground planes. To avoid radiating energy in differential mode, RF signals should not pass

through the ground plane.

(4) Minimize PCB dimensions

We aim to reduce the length of the tracks to lower the board's sensitivity and minimize the impact of parasitic capacitance and inductance. Moreover, lessening the vias that span different layers for signal transfer can help cut down noise generation [19].

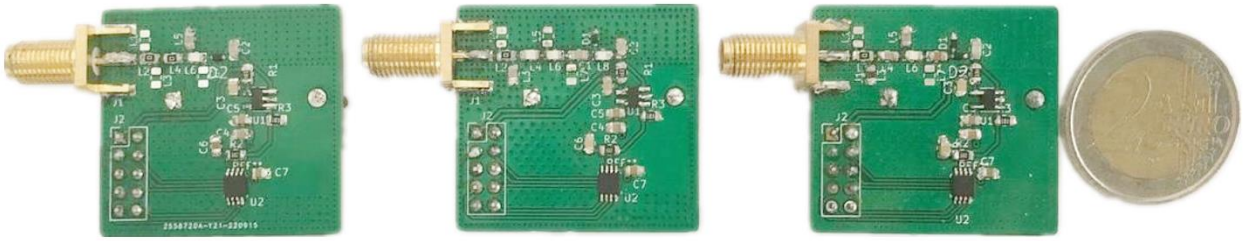
(5) Ground and Power Lines

"Ground" is defined as the low-impedance path for signal return. In practice, however, it is susceptible to interference. Voltage drops and interference superimposed on the useful signal occur when current flows through it [17]. Within RF frequency range, the signal takes the path with minimal inductance, typically the ground directly beneath the signal line, to minimizes the loop area and the loop inductance. For best results, no significant gaps should exist in the ground plane.

In the design phase, ground is segmented into different systems like digital, analog, and RF ground to avoid ground impedance coupling interference. Each ground line should have a single connection point at an appropriate location for continuity. Power lines and ground lines must be considered together. To reduce the characteristic impedance between them, they should be as thick and close together as possible, minimizing the power loop area. The use of decoupling capacitors, positioned as close to the chip as possible, helps provide necessary current and limit the current changes, thus reducing radiation.

IV.3.4 Experimental measurement

To achieve higher performances, we switched from the TLV3491 comparator to the LPV7215 [20], which has a smaller offset. Experimental measurements demonstrate that this change result in an additional 3dB improvement in sensitivity, thereby validating the comparator proposed in the first section of this chapter: reducing the comparator's offset indeed improves sensitivity. So that it makes sense to design a heterogeneous WUR. Consequent to these modifications, we develop a prototype for each of the three rectifier topologies, as illustrated in Figure 4.10.



Series-mounted topology *Shunt-mounted topology* *Voltage doubler topology*

Figure 4.10 4-layer semi-active WUR prototypes with different rectifier topologies

Then, we employ the same approach for impedance matching as in Chapter III. To assess the performance of the impedance matching network on the 4-layer prototypes, we measure the circuit's return loss S11 with a network analyzer over a frequency range from 500MHz to 1.2GHz. As shown in Figure 4.11, the return loss of a prototype at 868MHz is -27.9dB.

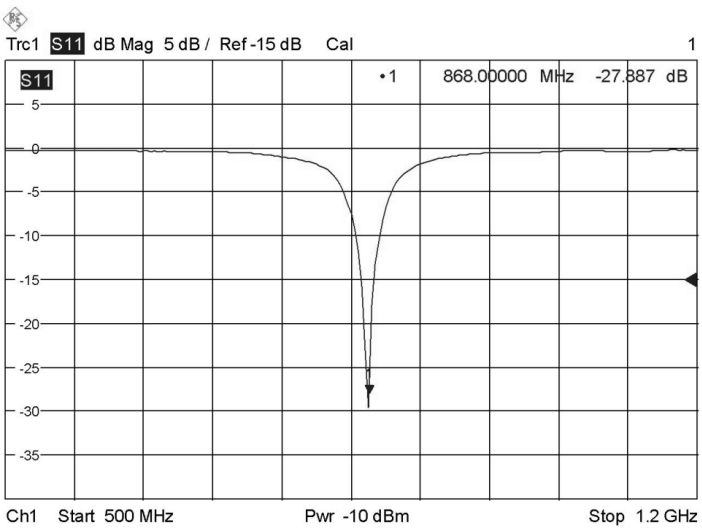
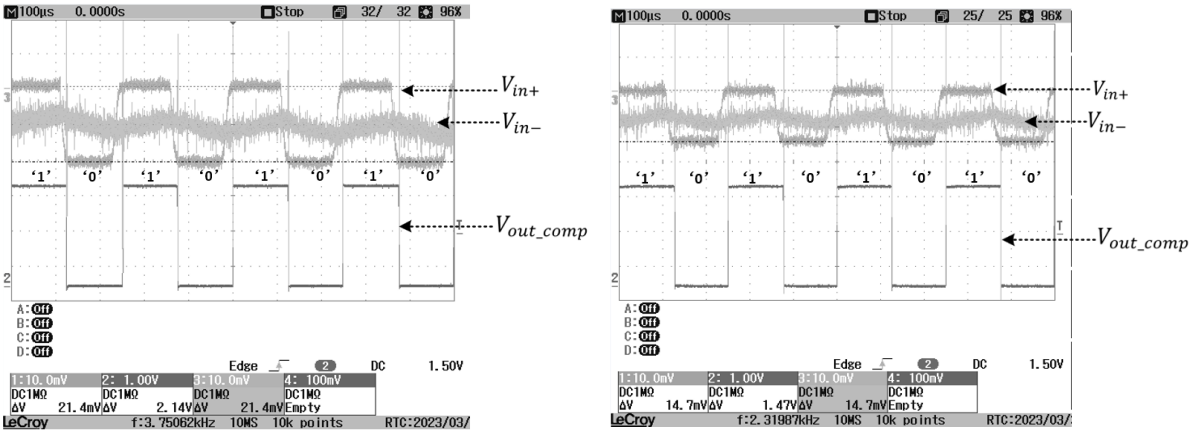


Figure 4.11 Example of return loss of a 4-layer prototype

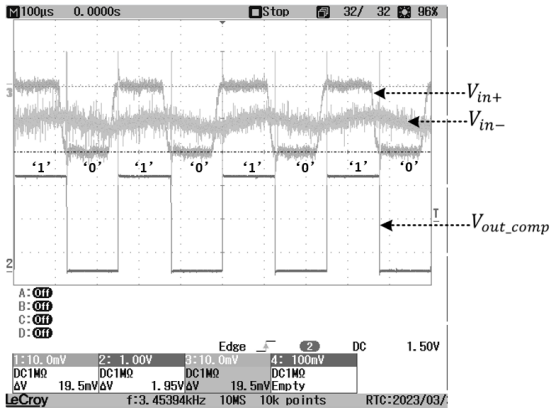
Then, prototypes are tested employing the Tektronix AWG7102, which generated an OOK-modulated signal at 868MHz and a data rate of 8kbps, in a same manner as Chapter III. Key performance characteristics such as the maximum transmission distance, sensitivity, and the DC output of the rectifiers are measured. The results are captured at an input power of −35dBm, including comparator input and output voltages, are shown in Figure 4.12.

Table 4.4 presents the measured results of the 4-layer WUR prototypes with three rectifier topologies. In accordance with the previously 2-layer prototypes' results, the sensitivity of the voltage doubler is found to be less optimal than that of the single-diode topology. Moreover, the WUR with shunt-mounted prototype has better sensitivity compared to the series topology,

this phenomenon is due to the smaller offset in the comparator in WUR of parallel topology, which improves its sensitivity. So, even though the comparators are commercial components, there could still be variations in their offset voltages due to manufacturing tolerances and differences in specifications. Also, it is worth noting that the 4-layer prototypes show a different measurement result where the output of the series topology rectifier exceeds that of the parallel topology, which deviates from the results obtained from the 2-layer board. However, these results emphasize the reality that actual implementations may vary due to several factors, including differences in circuit design, matching network and layout.



(a)WUR with series-mounted rectifier topology (b) WUR with Shunt-mounted recitifer topology



(c) WUR with voltage doubler rectifier topology

Figure 4.12 Comparators' input and output measurements of each WUR prototype @−25dBm input power

The DC output voltage of the rectifier is studied by modifying the input power, with measurements taken using an oscilloscope. As presented in Figure 4.13, the voltage doubler topology has a larger DC output when the input power is high (above −25dBm). Conversely, the DC output of the series rectifier is larger at lower input power, which is consistent with our

theoretical understanding. On the other hand, the parallel rectifier topology, yielding a smaller output than the series rectifier, could potentially be influenced by factors such as the layout design and quality of components.

Table 4.4 Measured results of the 4-layer WUR prototypes with three rectifier topologies

Topology	**Parameter**				
	Sensitivity (dBm)	***Maximum distance(m) @+10dBm***	***Consumption (nA)***	***Comp_offset (mV)***	***Output of rectifier @–35dBm (mV)***
Series	−46.6	37.1	580	0.74	21.4
Shunt	−47	39	580	0.70	14.7
Doubler	−43.5	26.2	580	0.75	19.5

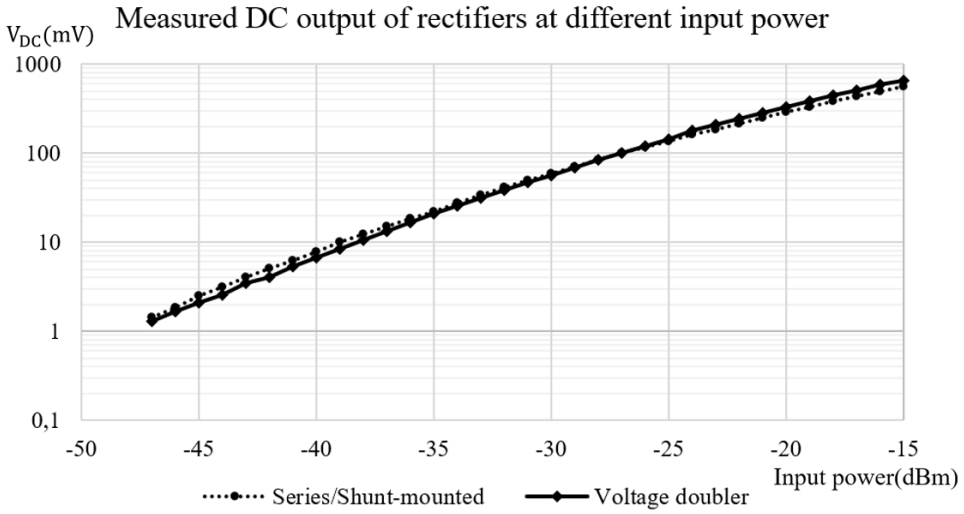


Figure 4.13 Measured DC output of rectifiers (in log scale) at different input power of 4-layer prototypes

In addition, under the testing condition with a transmission power of +10dBm, we perform curve fitting to the measured points and cumulative distribution function (CDF) of false/missed wake-up for the three WUR topologies. The comparison of these prototypes' false/missed wake-up probabilities as a function of distance is illustrated in Figure 4.14. However, none of these prototypes reach their theoretical sensitivities. This can be attributed to our testing under normal environmental conditions, rather than in a signal-shielded location. These results reflect real-world circumstances, where the impact of noise also increases with distance. Hence, maintaining signal integrity and reducing environmental noise are important in the effective operation of a WUR. While designing for maximal sensitivity is essential, it is also necessary

to consider actual operating conditions and potential sources of interference.

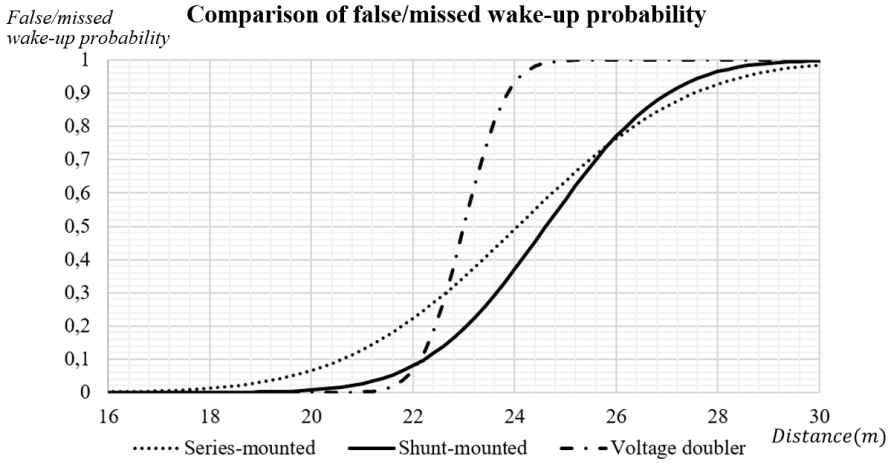


Figure 4.14 Comparison of false/missed wake-up probability as a function of distance for 4-layer prototypes with different topologies

IV.3.4 Performances' comparison

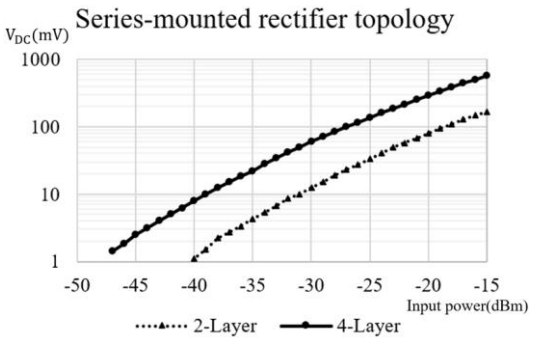
Table 4.5 provides a comparative analysis of the measurement results between the 4-layer and 2-layer prototypes, both employing a series-mounted rectifier topology. The 14dB improvement in sensitivity is mainly due to our targeted EMC optimization of the PCB, which result in a significant increase in the DC output of the rectifier. In addition, the use of comparators with reduced offset and lower power consumption is also beneficial to the performance improvement of the prototype.

Table 4.5 Comparison of the measurements between the 4-layer and 2-layer prototypes with the series-mounted topology

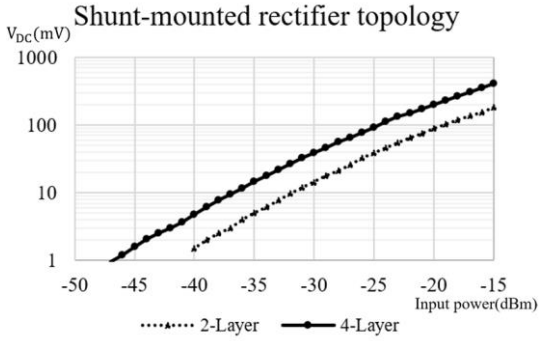
Parameters	**Comparison of results**	
	2-Layer	***4-Layer***
Sensitivity (dBm)	−33.33	−46.6
Maximum distance (m) @+10dBm	8.06	37.1
Output of rectifier@−25dBm (mV)	10.89	30.8
Comp_consumption (nA)	700	580
Comp_offset (mV)	−2.7	−1.5

Figure 4.15 presents a comparison of the DC output of each type of rectifiers in both 2-layer and 4-layer boards across each topology. It's evident that all 4-layer prototypes show improvements compared to their two-layer prototypes. And the improvement is more obvious

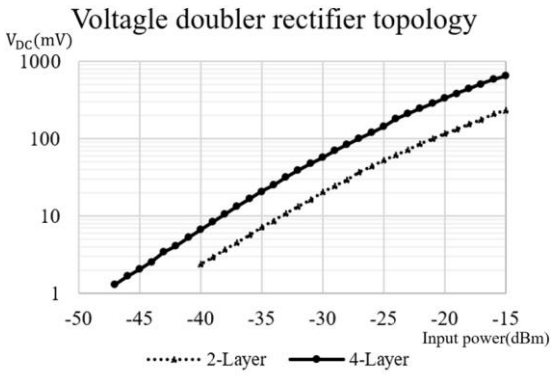
in the series-mounted topology than in the shunt-mounted topology. This difference may be due to factors discussed earlier, such as layout design and component quality. It may also be attributed to the shunt-mounted topology utilizing more components than the series topology, including an additional DC blocking capacitor and an RF choke. This introduces more uncontrollable variables into the system.



(a) WUR with series-mounted rectifier topology



(b) WUR with shunt-mounted rectifier topology



(c) WUR with voltage doubler rectifier topology

Figure 4.15 Measured DC output (in log scale) comparison between 2-layer and 4-layer prototypes for each rectifier topology at different input power

IV.4 Development of Arduino shield prototype

Examining the wake-up radio in isolation does not truly reflect its performance in actual applications. In the real-world, WUR works in conjunction with a multitude of other hardware modules, such as the main radio, the main micro-controller, and various sensors. The complexity and potential issues of these practical operations are often not reflected when testing WUR alone.

Therefore, we decide to develop a comprehensive node, integrating WUR with other key

modules. This approach allows us to observe and analyze the performances of WUR in real-world scenarios directly within the hardware platform. One particularity of our node design is that our WUR can operate at a frequency different from the main radio. This feature helps to avoid channel conflicts, enhance network reliability. Furthermore, to implement multi-hop in wireless sensor networks, we also introduce an additional 868MHz transceiver in the node, specifically for awakening the WUR. The block diagram of the node, as shown in Figure 4.16, illustrates the connections between the key modules.

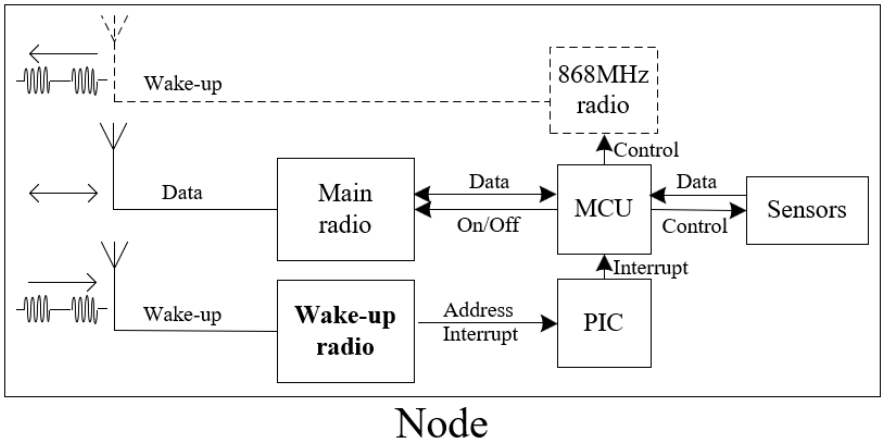


Figure 4.16 Principal block diagram of wake-up radio-based node

Our objective for the node is to realize the following functionality: when the WUR detects a wake-up signal transmitted from the base station, the PIC first determines whether the received wake-up packet is targeted for the main radio within its node. If confirmed, the PIC sends an interrupt to the MCU to wake it from sleep.

At the same time, once the MCU is awakened, it also controls the other sensors to become active. Following this, the MCU has to transition the main radio into its receiving mode for data packet reception. Immediately afterward, the MCU activates the 868MHz transceiver to wake up the neighboring WURs, further extending network communication.

Upon successful receipt of the data packet, the main receiver sends an acknowledge (Ack) signal back to the base station, confirming successful data transmission. The received data is then stored onto the SD card module for future use. Once this process is complete, all modules except the WUR revert to a sleep state to save power. This operational mechanism ensures energy efficiency and accurate communication in the node. Next, we will detail the design, development and measurement process of the node.

IV.4.1 List of modules in the node

The node is developed using an Arduino UNO 3.0 [21], chosen for its open source, ease of programming and supported by a large number of compatible modules and applications. The core of Arduino UNO is the Atmel's Atmega328P [22] micro-controller operating at 16MHz, equipped with six analog input pins and 14 digital I/O pins. The photo of Arduino UNO is shown in Figure 4.17.

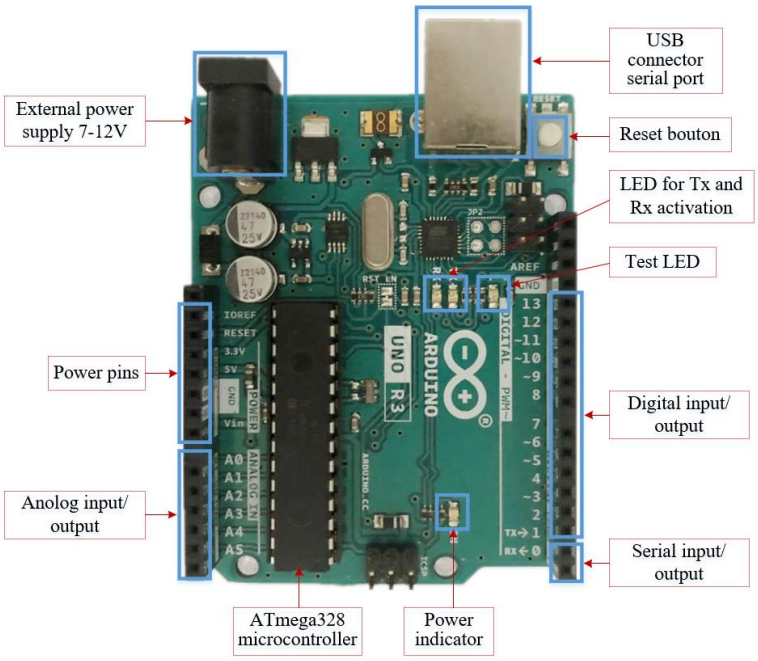


Figure 4.17 Arduino UNO development board

Arduino UNO comes with a USB connection, a DC power jack, an ICSP header, and a reset button. It can be powered either from a USB connection or an external power source within a range of 6 to 20V.

Programming is facilitated by the Arduino Software (IDE), which also hosts the Serial Monitor, a tool for displaying data received from the Arduino board via a USB connection. Significantly, Arduino's micro-controllers are pre-programmed with a bootloader, negating the need for a separate hardware programmer. The software and Arduino Language are released under an open-source license. Coupled with its affordability and simplicity, so it is a good choice for developing our node.

Following the selection of Arduino UNO as our core development platform, we identify additional modules compatible with the Arduino environment to fulfill the specific functional

requirements of our node, which can be programmed using Arduino IDE. Among these modules, a temperature and humidity sensor has been selected to serve as a representative sensor in our initial explorations. The data captured by this sensor will be encapsulated within the data packets transmitted in our wireless sensor network, thereby providing a practical illustration of sensor data collection and transmission in a wireless sensor network (WSN). The list of these modules within our node, are as in Table 4.6.

Table 4.6 List of modules used in the node

Module type	Model name
MCU	Arduino UNO
Temperature and humidity sensor	DHT11
Main radio	NRF24L01
868MHz transceiver	CC1101
SD card	Micro SD
Wake-up radio	Custom designed

IV.4.2 Implementation with micro-controller Arduino UNO

For our setup, we plan to develop three units: one node serves as a base station, which transmits data packets, and two nodes functioning as receivers. For ease of distinction, we label them as 'Base station' and 'Node'. Each node will exhibit its unique ID and address, with the capability to receive commands from the base station.

The base station is designed to send data packets containing measurements from a temperature sensor. Unlike the base station, the nodes do not require these sensors as they are strictly receivers in our setup. To illustrate their functionalities and interrelations, refer to the base station and node functional block diagram (Figure 4.18).

To extend battery life, all units including the base station and nodes operate on the principle of entering sleep or idle mode when not active. These devices are battery powered. The WUR in the nodes contributes to energy efficiency, only waking up the main components of the nodes when necessary to receive data packets from the base station.

In the case of the base station, a controlled button is incorporated for initiating data transmission. When data needs to be sent, the button is pressed, sending an interrupt to the

MCU. The base station's MCU then wakes up and begins controlling the two radios to send the Wake-up packet and Data packet. After transmission is complete, the base station waits to receive an Ack, records this in the SD card, and enters sleep mode if an Ack timeout occurs.

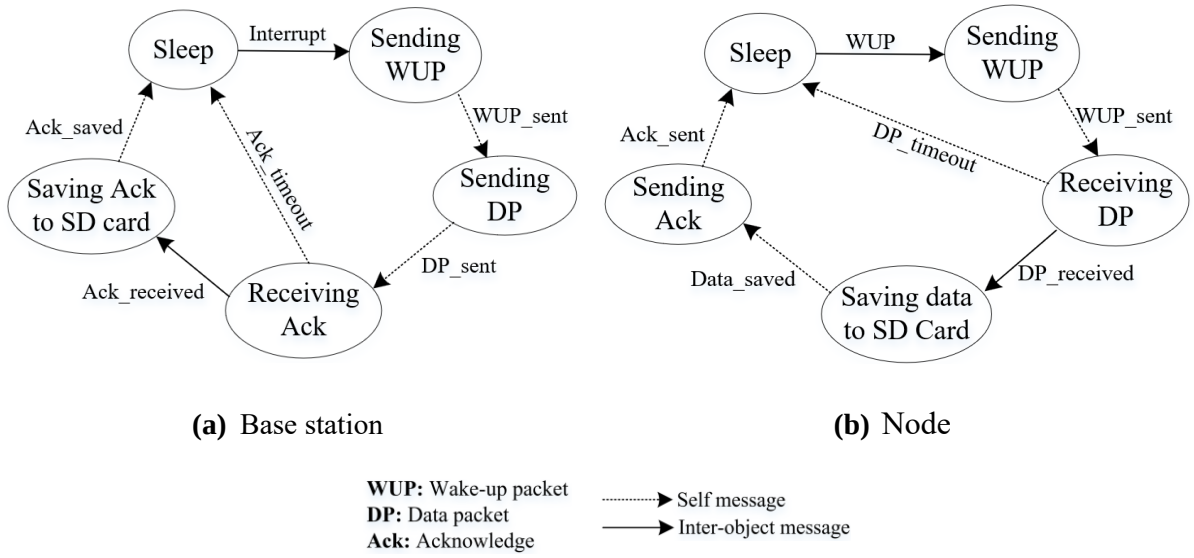


Figure 4.18 Activity diagram of proposed transmis sion mechanism: (a) Base station communication process, (b) Node communication process

After establishing the general overview and power management strategy, we proceed to discuss each block in the design, taking into account key considerations for embedded programming. During the operation and debugging of the system, we employ the Arduino IDE and related libraries for data analysis, while the Arduino Serial Monitor serves as our tool for reading and accessing information.

DHT11

The DHT11 is a low-cost digital sensor for sensing temperature and relative humidity [23]. It can interface with an Arduino, providing real-time measurements of humidity and temperature. The sensor operates within a voltage range from 3 to 5 volts, drawing a maximum current of 2.5mA. Figure 4.19 displays the picture of the DHT11 sensor module and illustrates its connection methodology. It includes a 10KΩ pull-up resistor and power-on LED for the signal line.

Pin	DHT11	Arduino
1	Vcc	5V
2	Data	digIO5
3	Gnd	Gnd

Figure 4.19 DHT11 temperature and humidity module

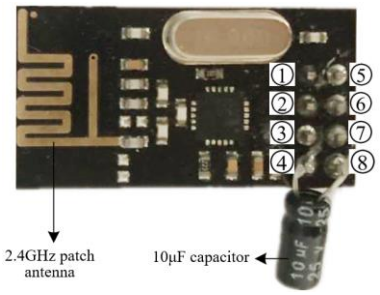
NRF24L01

The NRF24L01, produced by Nordic Semiconductor, serves as the main radio in our network [24]. This module operates within the 2.4GHz and 2.5GHz range of the ISM band using FSK modulation. Its power must comply with a voltage threshold of 3.6V. Nevertheless, all other pins can operate at 0V/+5V. The key specifications of the NRF24L01 module are summarized in Table 4.8:

Table 4.7 Key specifications of NRF24L01 module

Feature	Specifications
Supply voltage	3.3V
Frequency	2.4GHz
Modulation	FSK
Data rate	1Mbps
Transmit power	0dBm
Reception sensitivity	−90dBm

It's worth noting that power supply noise is one of the most common issues encountered when attempting successful communication with the NRF24L01 module. To overcome this issue and improve the NRF24L01's performance and reliability, we solder a 10μF capacitor onto the power ports (Gnd and Vcc) to reduce interference. Communication between the NRF24L01 and the Arduino UNO micro-controller is established via Serial Peripheral Interface (SPI) [25]. The picture of the module and the connection method are shown in Figure 4.20:



Pin	NRF24	Arduino	Pin	NRF24	Arduino
1	IRQ	–	**5**	MISO	digIO12
2	MOSI	digIO11	**6**	SCK	digIO13
3	CS	digIO7	**7**	CE	digIO18
4	Vcc	3.3V	**8**	Gnd	Gnd

Figure 4.20 The NRF24L01 module and pin-to-pin connections to Arduino UNO

Once the module's pins and some variables are defined, we need to initialize the wireless communication address. The NRF24L01 is capable of simultaneously receiving data from up to six different channels, as illustrated in Figure 4.21. Each node is assigned a specific frequency pipe for effective communication. In our application, we are utilizing two such pipes.

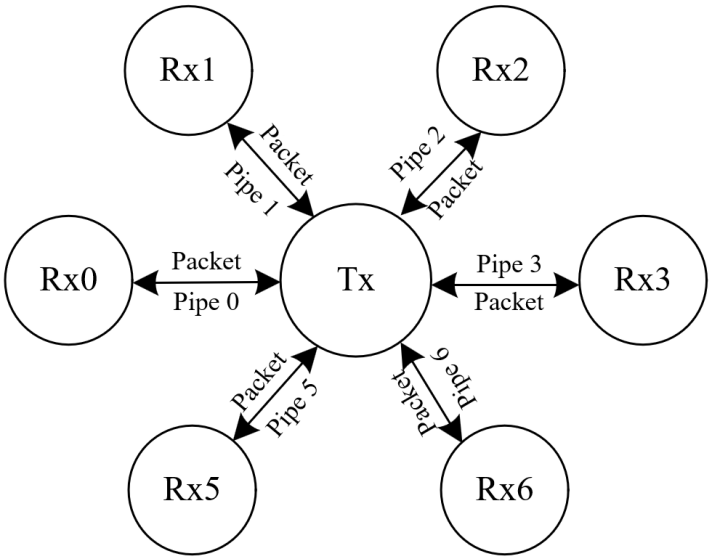


Figure 4.21 NRF24L01's frequency band with pipe separation

The NRF24L01 has a maximum buffer size of 32 bytes, meaning any transmitted message should not exceed this size. The type of transmitted data is not limited to variables or strings - in fact, any data that fits within the buffer size can be sent.

CC1101

The CC1101, a high-performance sub-1GHz RF transceiver from Texas Instruments, is specifically designed for ultra-low-power wireless applications [26]. It allows for transmission and reception in the ISM* and SDR* frequency bands near 315/433/868/915MHz. In our design, it is employed as an 868MHz transmitter to activate the wake-up radio.

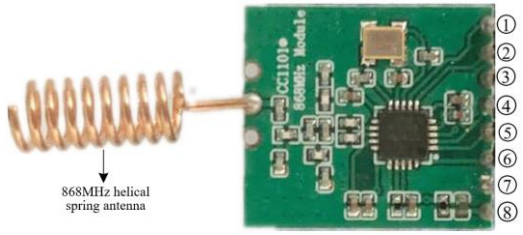
Accurate transmission of wake-up packets demands precise frequency and bit rate settings, which the CC1101 provides through a range of configurable registers. These registers need to be meticulously set according to the specifications in Table 4.9 to ensure proper signal transmission. TI's proprietary tool SmartRF Studio can assist in generating optimal register settings directly via its interface graphics [27].

Table 4.8 Key specifications of CC1101 module

Feature	Specifications
Supply voltage	3.3V
Frequency	868MHz
Modulation	OOK
Data rate	8kbps
Transmit power	+10dBm

In addition to configuring the registers according to the above specifications, the correct OOK modulation setting is also critical. PATABLE is an 8-byte table used to select PA (Power Amplifier) control settings. Programming the PATABLE allows for controlled PA ramping up and ramping down, as well as ASK modulation shaping for bandwidth reduction. OOK modulation is simply turning the PA on and off, thereby modulating '1' and '0' accordingly.

Communication between the CC1101 and Arduino UNO is also realized via SPI. The module's picture and connection method are illustrated in Figure 4.22:



Pin	CC1101	Arduino	Pin	CC1101	Arduino
1	CS	digIO10	**5**	CLK	digIO13
2	GDO0	digIO2	**6**	MOSI	digIO11
3	GDO2	–	**7**	Gnd	Gnd
4	MISO	digIO12	**8**	Vcc	3.3V

Figure 4.22 The CC1101 module and pin-to-pin connections to Arduino UNO

In our setup, for the CLK, MOSI, and CSN pins input from Arduino to CC1101 (highlighted in grey in Figure 4.22), It's necessary to use a 3.3V voltage pin instead of 5V to prevent potential damage to the CC1101. Therefore, for these three pins on the CC1101, we introduce a bridge circuit to shift the 5V to 3.3V, as depicted in Figure 4.23.

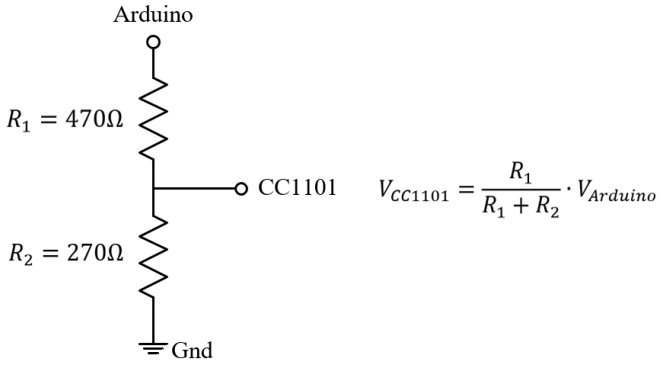
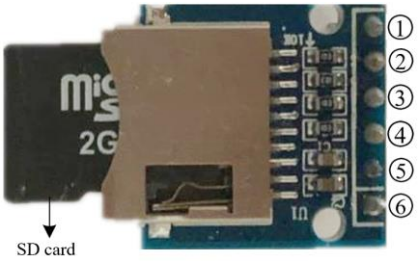


Figure 4.23 The voltage divider circuit

Micro SD card

During our measurements, significant amounts of data need to be collected. So it’s not practical to stay connected to the computer to observe and analyze the data through the serial monitor. Thus, storing this information on an SD card becomes a favorable solution. It allows us to gather data flexibly during the experiment, independent of the device's location and connectivity status. After the completion of measurements, we can then process the data on a computer.

To address this need, we adopt a Micro SD card reader module, which enables data transfer between Micro SD cards and provides methods for reading and writing data. In our case, it's also connected to Arduino UNO via an SPI, the detailed connection method is depicted in the following figure.



Pin	SD	Arduino	Pin	SD	Arduino
1	CS	digIO9	**4**	MISO	digIO12
2	CLK	digIO13	**5**	Vcc	3.3V
3	MOSI	digIO11	**6**	Gnd	Gnd

Figure 4.24 The Micro SD card module and pin-to-pin connections to Arduino UNO

An aspect to note when using the SD card module is that it is essential to level shift the pins from 5V to 3.3V, similar to what we did with the CC1101 using a voltage divider. The pins that need to be converted are marked in gray in Figure 4.24. And we need to avoid using models with integrated level shifters, as when the SD card is deselected, the 5V to 3.3V hardware on the microSD breakout board doesn't disengage from the MISO line, which can interfere with all other chips on the SPI bus.

IV.4.3 Shield prototype design

Upon verifying that all modules function correctly in conjunction, we develop an Arduino shield - a 2-layer PCB that plugs directly into an Arduino. This shield is designed with convenience as a priority, offering multiple sockets on its surface that enable easy insertion and removal of various modules.

Moreover, the shield provides the advantages of stability and reliability. All modules directly connect to the shield, bypassing the issues of connection disruptions caused by loose or tangled wires, ensuring an orderly and robust hardware setup.

Figure 4.25 shows the top and bottom side of the shield, with sockets for all the modules labeled accordingly. We also incorporate two buttons for facilitating debugging on the board: one connected to an Arduino interrupt, serving as our command for the base station to send data, and another connected to an analog input for debugging purposes. In addition, the shield is equipped with 4 LEDs to indicate PIC wake-up (LED1), PIC's correct address reception (LED2), main radio receiving data (LED3), and main radio transmitting data (LED4).

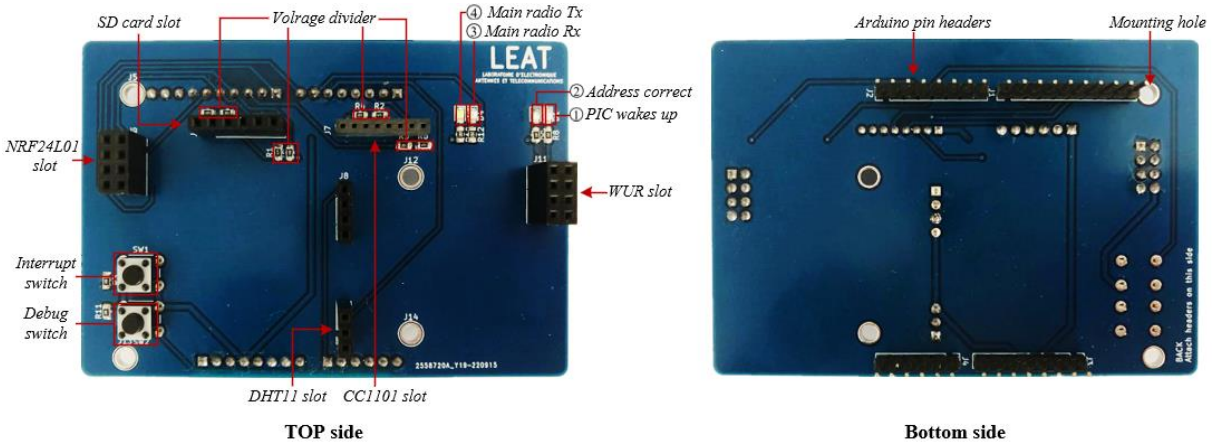


Figure 4.25 Arduino shield diagram

The final stage of our development involve implementing a power-saving sleep mode for both our modules and the Arduino. By putting these components into a low-power sleep mode, we can achieve significant energy savings, crucial for long-term operation of our system.

For Arduino, we employ its “Power down” mode, which offers the greatest power savings [21]. In this sleep mode, only the external interrupts and the Watchdog Timer remain active, reducing power consumption to the minimum. Arduino can be awakened from this deep sleep mode reliably using an external interrupt pin. In our case, this external interrupt is triggered by a hardware button.

In conjunction with the Arduino's sleep mode, we also implement a low-power mode for our modules. The mode transition is executed by the Arduino setting the appropriate registers within each module. Once awakened, the Arduino can prompt the modules to exit their low power state and resume operation. Table 4.11 presents the power consumption of various

modules in different modes. And Table 4.12 provides the delays when the modules wake up or switch states.

Table 4.9 Power consumption of modules in different modes

Module	Active mode	Standby mode	Sleep mode
Arduino UNO	98.4mA	1.62mA	360μA
DHT11	2.5mA	1mA	150μA
NRF24L01	Tx: 11.3mA, Rx: 13.1mA	26μA	900nA
CC1101	Tx: 30mA	–	200nA
SD card	Read/Write: 400mA	1mA	–
Wake-up radio	580nA	–	–

Table 4.10 Delays of module wake-up and state switching

Module	Wake-up delay	Mode transfer delay
Arduino UNO	1ms	–
DHT11	18ms	40μs
NRF24L01	1.5ms	130μs
CC1101	0.8ms	31μs
SD card	–	1ms

IV.4.4 Experimental measurement of scenario with 3 nodes

We establish a network composed of one base station and two sensor nodes for testing. Each sensor node is assigned a unique network ID, recognized by the base station, to proper handling of its data. The base station is designated as node 0, while the sensor nodes are designated as nodes 1 and 2, respectively.

Despite having only one base station and two sensor nodes manufactured, this setup allows us to feed the test results into a network simulator for emulating larger network environments without the need to actually fabricate and deploy more devices. This approach not only saves costs but also provides results that reflect the actual environment. Figure 4.27 illustrates the experimental setup for the measurement.

We carry out two testing scenarios, considering different situations regarding communication distances within the network and different node wake-up mechanisms.

In the first scenario, the base station (Node 0) successfully woke up two nodes (Node 1 and

Node 2) using the broadcast method and then sent them information. This scenario presupposes that all nodes are within the communication range of the wake-up radio, hence eliminating the need for multi-hop communication.

The second scenario simulates a more complex communication environment, where Node 2 is located beyond the base station's direct communication range. In this case, Node 1 plays the role of a relay, assisting in transmitting the wake-up signal from the base station to Node 2, before all nodes receive information from the base station.

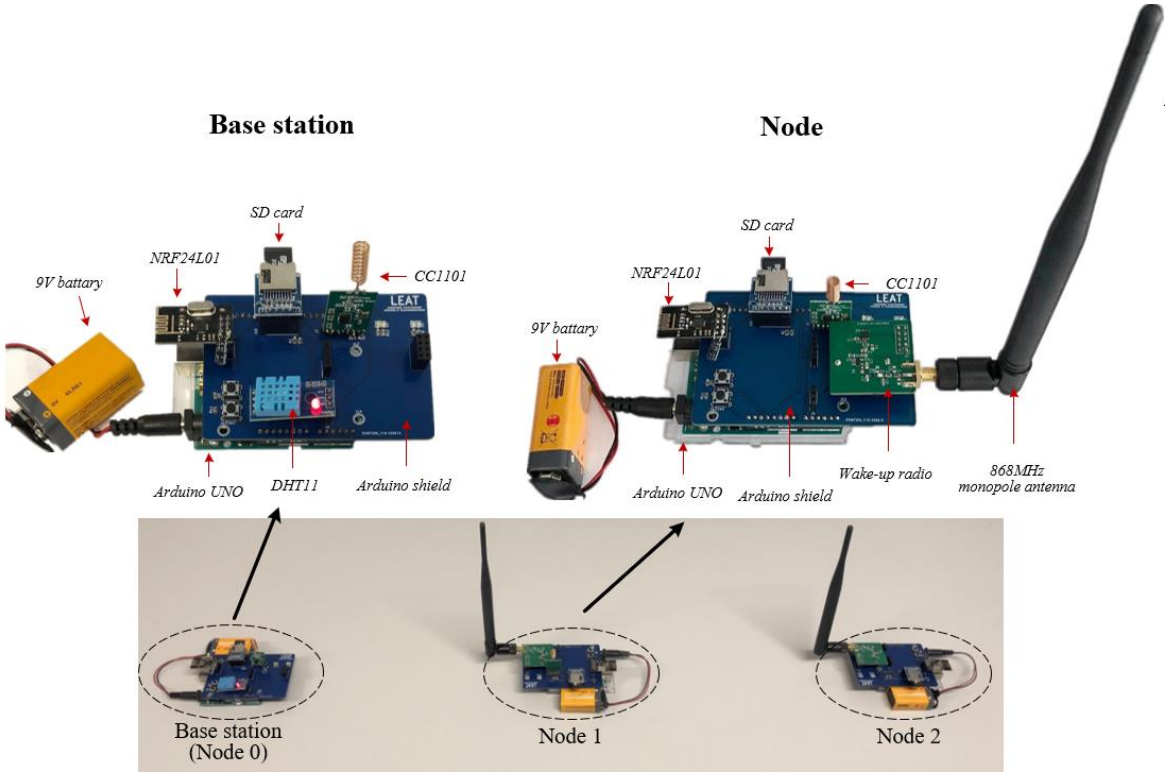


Figure 4. 26 Photo of the experimental setup for the measurement

For accurate testing and data collection, we utilized an SD card for data logging, including the wake-up count for each node and their respective information reception, as well as the reception of the Ack of the base station.

Figure 4.27 provides an example from our measurements to illustrate the content of the stored data. We used the base station to send 10 rounds of data measured by the temperature and humidity sensor DHT11 to Node 1 and Node 2. It is worth noting that Node 2 needs to be woken up by Node 1.

Figure 4.27 (a) and (b) show the data recorded on the SD cards of Node 1 and Node 2, respectively. This includes the count of the main MCU Arduino’s wake-up times, and the data

received by the main radio. Node 1 is activated 8 times, while Node2 is activated 6 times, followed by the data they receive.

Figure 4.27 (c) presents the data stored on the SD card of the base station. Each time an Ack signal is received, the base station records the Ack and its corresponding round number. In our case, '111' and '222' are the Acks transmitted by Node 1 and Node 2, respectively. The figure shows that no Ack is recorded in the fourth round, while only Node 1's Ack is received in rounds 6 and 9. This information allows us to perform the statistical analysis of the data.

	A	B	C	D
1	Wake-up sign	Number of wake-ups	Humidity	Temperature
2	WakeUp	1	19%	26C
3	WakeUp	2	20%	26C
4	WakeUp	3	20%	26C
5	WakeUp	4	20%	26C
6	WakeUp	5	20%	26C
7	WakeUp	6	21%	26C
8	WakeUp	7	21%	26C
9	WakeUp	8	21%	26C

(a) Node1

	A	B	C	D
1	Wake-up sign	Number of wake-ups	Humidity	Temperature
2	WakeUp	1	19%	26C
3	WakeUp	2	20%	26C
4	WakeUp	3	20%	26C
5	WakeUp	4	20%	26C
6	WakeUp	5	21%	26C
7	WakeUp	6	21%	26C

(b) Node2

	A	B	C
1	Sent sign	Number of rounds	Label of node
2	Round	1	111
3	Round	1	222
4	Round	2	111
5	Round	2	222
6	Round	3	111
7	Round	3	222
8	Round	5	111
9	Round	5	222
10	Round	6	111
11	Round	8	111
12	Round	8	222
13	Round	9	111
14	Round	10	111
15	Round	10	222

(c) Base station

Figure 4.27 Data stored in the SD cards

After processing and analyzing these data, we find that if the wake-up radio can successfully trigger the main receiver, the transmission and reception of information are usually successful. This further reinforce our system design principle - that through effective and timely wake-up mechanisms, efficient node communication can be achieved in both single-hop and multi-hop network environments.

On the other hand, through these two test scenarios, we also recognize the challenges and limitations of the system in complex environments, such as ensuring the accurate and efficient transmission of information when the wake-up signal needs to pass through multiple hops. This

provides practical data support and new research directions for our next steps.

IV.5 Conclusion

In this chapter, we explore the design, implementation, and optimization efforts to improve the performance of our WUR.

We start by detailing the design process of an optimized WUR circuit with design specifications. We successfully develop a comparator, achieving an input voltage offset of 0.6mV and power dissipation of 473nA under a 3V supply. Compared to the initial comparator, TLV3491, characterized by a 700nA quiescent current and 2.7mV input offset, the improved design shows significant advancement.

Subsequently, we focus on enhancing the PCB design of the WUR, adopting a series of strategies including a 4-layer PCB structure and circuit layout design strategies. In fact, these improvements show significant improvements in reducing electromagnetic interference and enhancing signal integrity. Consequently, the sensitivity of the 4-layer WUR improved by 14dB compared to its 2-layer counterpart. Test results confirm an increase in system reliability and stability, thereby justifying our design changes.

Moreover, this chapter emphasize the significance of practical considerations such as circuit implementation, layout design, and impedance matching networks that can impact performance and measurement outcomes. Particularly, we observe that real-world implementations might not always reflect the theoretical sensitivity, and environmental noise also has a huge impact. These factors must be considered during the design process.

Finally, we present the development of a cost-effective WUR node that provide insights into the implementation of a complete WSN application involving multiple actions, i.e., waking up, wireless data transmission, and extracting information via an SD card.

Building upon the foundation of our study, we develop a functional Arduino shield prototype for the WUR node, followed by implementing two different testing scenarios that closely resemble real-world network conditions. In one scenario, all nodes are within the communication range of the wake-up radio, whereas in the other, a multi-hop communication environment is created, with one node acting as a relay to help pass the wake-up signal. It

demonstrates that if the wake-up radio successfully woke the main receiver, a successful data packet transmission is generally ensured.

This comprehensive exploration of the WUR's optimization and practical implementation has laid a solid foundation for future work. It shows the potential of semi-active wake-up radios in wireless sensor network applications.

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Chapter V: Simulation of sensor networks with semi-active wake-up radio in OMNeT++

V.1 Introduction

In this chapter, we focus on using network simulator as an effective tool in the sensor networks, particularly within the context of wireless sensor networks (WSNs) characterized by a great number of nodes and limited resources. This approach allows us to overcome material constraints and reflect real-world measurements, thus reducing experimental costs and improving development efficiency [1].

Our research is aimed at the development of the physical layer in the OSI model. Building upon our previous investigations in theoretical modeling, circuit simulation results, and prototype measurements. And we chose OMNeT++ software as our network simulation tool.

We initially develop several models without a framework and compared their performances. A set of hierarchical models based on electrical simulation, mathematical prediction, and measurements are then implemented in OMNeT++. We provide a modeling methodology that accounts for wake-up radio characteristics within sensor network communications. The models provide indications on the WUR's sensitivity and probability of false wake-up or missed wake-up. The models are then used in a case-study that evaluates the energy per transmitted bit. The accuracy of the models as a function of the CPU time is provided.

Furthermore, we extend the INET framework with our WUR models to explore the overall performance of the WUR system. We first build a comprehensive wireless network model for WUR using the INET framework, and add mobility to the nodes to evaluate the pros and cons of WUR nodes with three different rectifier topologies.

The remainder of this chapter is organized as follows: Section V.2 presents our work focusing on the physical layer of the OSI model and describes the trade-offs between accuracy, CPU time, and development time during the model evaluation. And then, Section V.3 conducts a detailed description of the electrical models of semi-active wake-up radio, evaluating their performance in a scenario. In Section V.4, we evaluate the performance of the comprehensive

WUR wireless network, featuring node mobility, within the context of the INET framework. Finally, Section V.5 concludes the chapter.

V.2 Implementations of physical layer in OMNeT++

The Open Systems Interconnection (OSI) model, developed by the international organization for standardization, is a conceptual model that enables diverse communication systems to communicate using standard protocols. It provides standards to ensure that different computer systems can interact with each other [2]. The OSI model is not only a theoretical framework but also a tool for designing and understanding network communications. This model divides network communication into 7 layers, as shown in Figure 5.1.

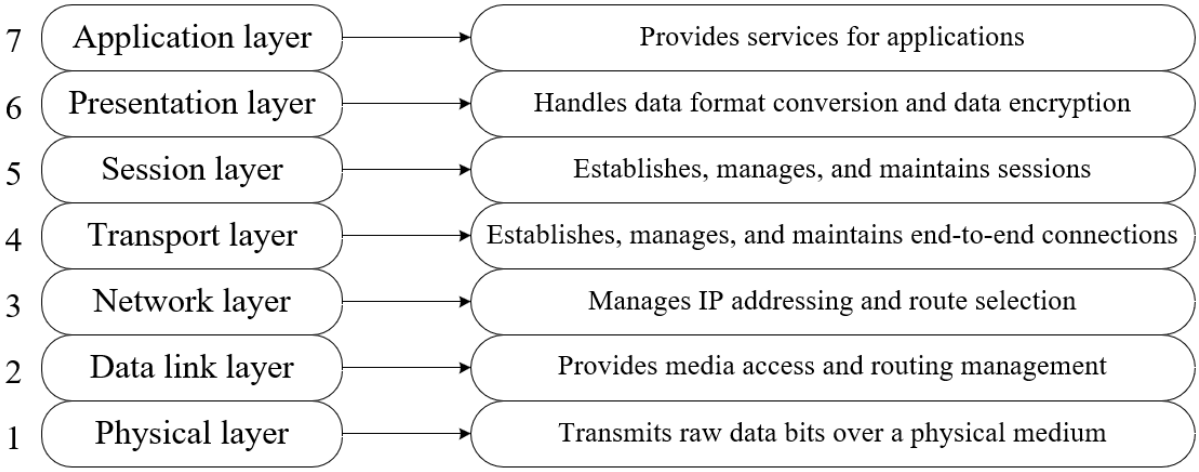


Figure 5.1 Open System Interconnection (OSI) model

Our network simulations concentrate on the development of the WUR's physical layer, based on our previous explorations in theoretical modeling, circuit simulation results, and prototypes' measurements. As the lowest layer of the OSI model, the physical layer is responsible for converting binary data into signals for transmission between network devices, and for managing the transmission of signals via physical media such as radio waves or cables. It is an important part of wireless nodes, responsible for controlling the operating frequency of transceivers, setting modulation information, and carrying out data transmission and reception [3]. Up to now, there is still a lot to be explored in the specific construction of the WUR physical layer.

We chose OMNeT++ 6.0, as our network simulation tool. OMNeT++ (Objective Modular

Network Testbed in C++) is an open-source, object-oriented, visual, discrete event simulation framework that is free for academic and educational use. It allows communication between modules by passing messages and provides a graphical user interface (GUI), which allows us to visually observe the internal situation of the simulation model, including the operation status of the network and the message flow [4].

OMNeT++ provides efficient tools for describing the structure of actual systems. The modeling is accomplished by using layered embedded modules that communicate by transmitting messages to each other. This structure allows developers to encapsulate specific functions or components in modules. Object-oriented programming makes the construction process of the simulation system more organized and flexible. The top-level module is called the system module, which includes sub-modules and compound modules, and there are no limits on the depth of module embedding [5]. Figure 5.2 presents the structure of simple and compound module.

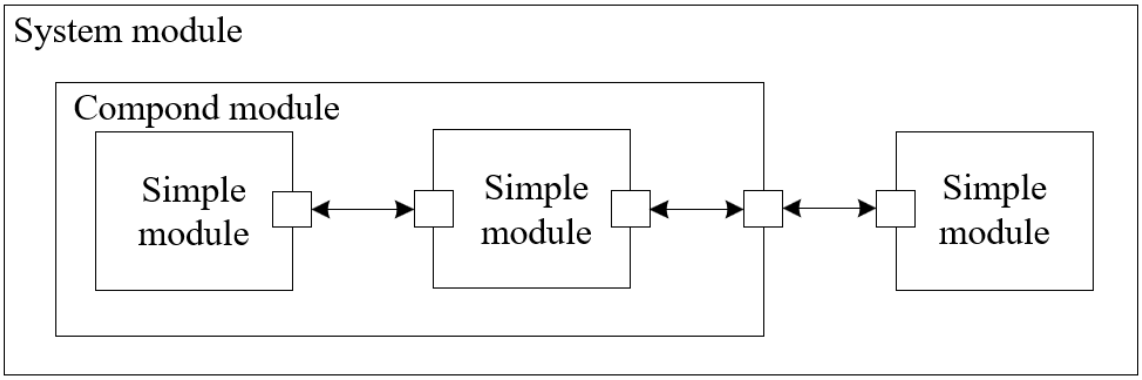


Figure 5.2 Simple and compound module

There are 4 main types of files in the construction and execution of the simulation model:

NED files: Define the topology of the model, which is convenient for a network's model description. The network description can include a set of component descriptions (channels, simple/complex models), and these component descriptions can be reused in other network descriptions. The parameters, sub-modules, and ports of each module are specified in this file.

CC files: For each module in the NED file, we need to give the implementation of the module in the CC file. This implementation code is responsible for the main behavior and logic of the module.

MSG files: These files serve to define the message types of variables and add data files on

them. Modules communicate by exchanging messages.

INI files: Input parameters, network settings, and different simulation cases are given in this file. These parameters include factors such as address and power consumption of the radios. In each simulation, we can change the inputs and scenarios in this file to evaluate the system under different conditions.

In our network simulation, we focus on a wireless network with multiple wake-up radio nodes, considering the total power consumption and delay of a certain number of nodes, including the power consumption of the receiver, additional delay, false wake-up, and retransmission, etc. We will conduct a detailed simulation and evaluation of the performance of our WUR's physical layer, which is an important supplement to MAC layer modeling.

For WUR's modeling in OMNeT++, development time and cost are measured in three key dimensions: accuracy, CPU time, and development time. These dimensions are interconnected to form a triangular trade-off diagram, as shown in the Figure 5.3.

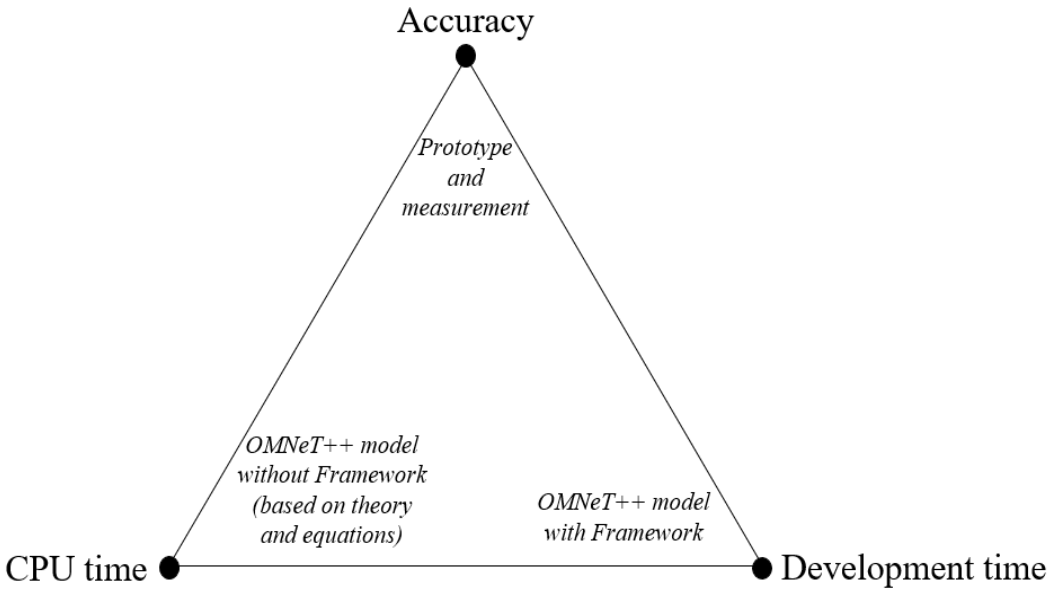


Figure 5.3 OMNeT++ network modeling triangle trade-off diagram

High-precision models generated through prototyping and measurements yield accurate results. But this approach requires significant time and resources, especially for physical design and real-world measurements.

On the other hand, models in OMNeT++ without a framework are based on theory and equations. These models can minimize CPU computational time. While such methods can

deliver results quickly and efficiently, they might sacrifice accuracy by relying on theoretical foundations and equations rather than actual measured data.

Finally, OMNeT++ models developed with a framework minimize the time required for development. By utilizing predefined modules and functionalities, the need to write code from the beginning is eliminated. While this approach reduces development time significantly, it may increase CPU time due to the inherent complexity of the included functions.

V.3 Evaluation of semi-active wake-up radio's electronical models without framework

In this section, we focus on the development and evaluation of electrical models for semi-active wake-up radio in an environment without a framework. As the frameworks in OMNeT++ do not provide a node model with WUR functionality, we developed a new physical layer modeling method to account for the characteristics of WUR in sensor network communications. To maintain the focus of our study on WUR, we introduced only a main radio module in the node to simulate the wake-up action and conduct data communication.

In OMNeT++, we implemente a set of hierarchical models based on electrical simulation, mathematical prediction, and measurement. This is aimed at evaluating the accuracy of each model and examining the sensitivity of WUR as well as the possibility of false wake-up or missed wake-ups, which also serve as the extension and supplement to the electrical modeling in Chapter III. These models are applied in scenarios where signals are propagated from the transmitter to multiple nodes, with comparisons made in terms of CPU time and accuracy.

V.3.1 Modeling description

Base station

The base station sends a 32-bit data packet to the nodes every 60 seconds, randomly selecting a time between 0 and 50 seconds. It first sends a WUP containing broadcast address to wake up the nodes. After 0.5 second wake-up time, it sends a DP to the nodes within the data transmit range (D_d), and then waits to receive an Acknowledge (Ack). After the Ack timeout, if

all Acks are received, it will enter the next round. Otherwise, if no Acks from more than two nodes are received, it continues to send the broadcast address and repeat the above process; if only one node's Ack is not received, the address of this node is sent. After the time of the round is up, it is forced to enter the next round. If the transmitter has not received an Ack from a node in 10 rounds, it is judged that the node has died. The flowchart of base station is presented in Figure 5.4.

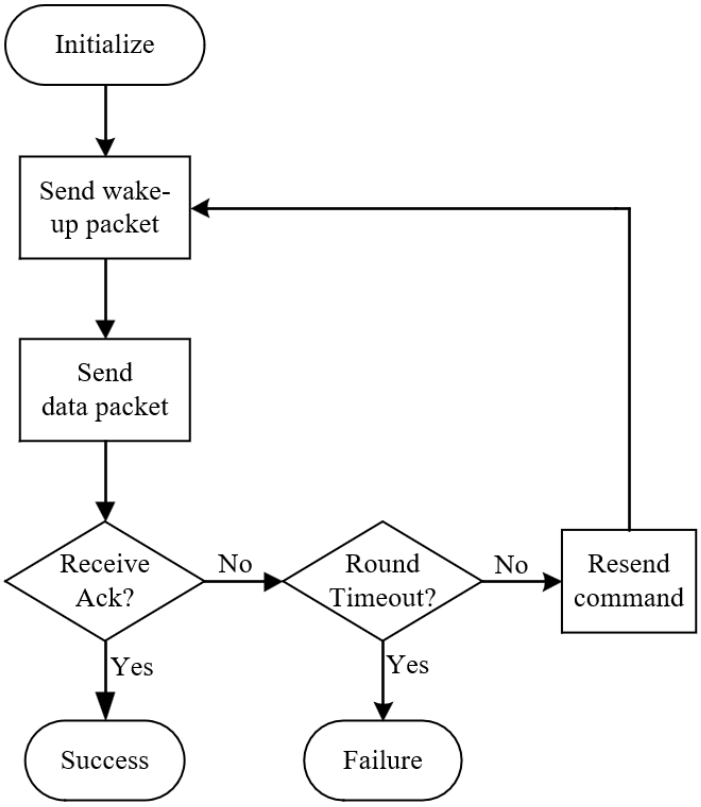


Figure 5.4 Flowchart of the base station without framework

Node

The node is an OMNeT++ composite module, which is shown in Figure 5.5. Each node contains a WUR module, a PIC micro-controller module, a main radio module, a module including the location information of the nodes, and a battery module.

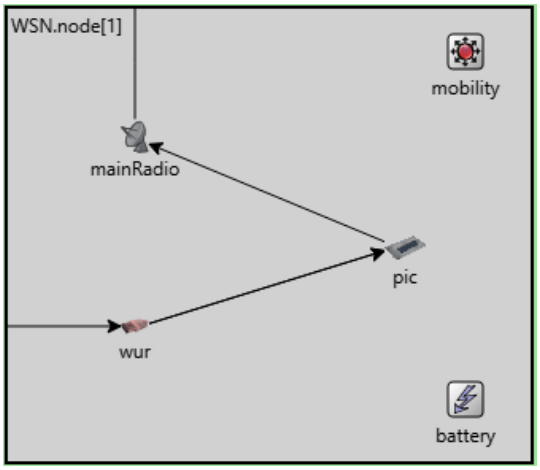
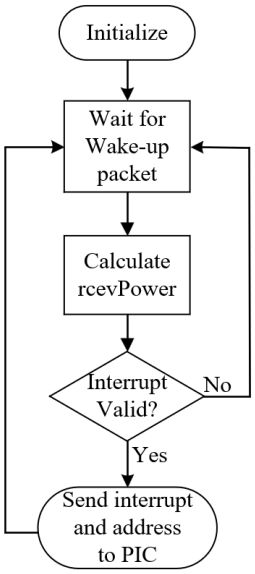


Figure 5.5 The composite module of the node

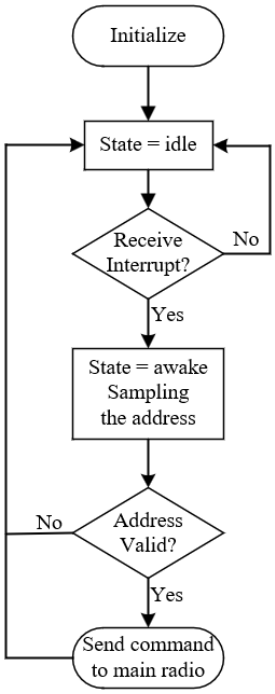
(1) Wake-up radio: Each WUR within wake-up range (D_{wu}) detects activity on the channel. And once the WUR receives a wake-up task, it analyzes the wake-up packet (WUP) and transmits the interrupt and address to the PIC. The wake-up radio consists of 4 parts: rectifier, reference generator, comparator and RC integrator, which are designed as C++ classes instead of separate OMNeT++ modules, in order to provide a clean interface and avoid memory overhead. Figure 5.6(a) shows the flowchart of the wake-up radio.

(2) PIC micro-controller: The PIC module is responsible for the evaluation (classification as signal or noise and packet error calculation) of the received WUP, which is presented in Figure 5.6 (b). It performs address decoding and decides whether to trigger an interrupt to wake up the main radio. If the address is valid, the PIC sends commands to control the main radio, whether to transfer or broadcast or listen. It contains a routing table to find out if a neighbor's address is received, and then wakes them up.

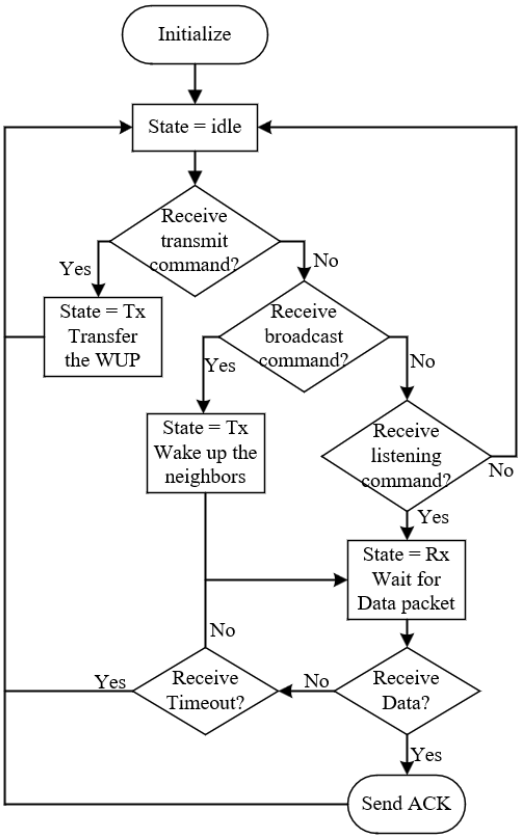
(3) Main radio: If the main radio receives the broadcast command of PIC, it broadcasts the signal to the nodes within the D_{wu} distance. Each node broadcasts only once, and then the main radio switches to the listening mode; if it receives the transmit command, it only transmits the WUP to the neighbors. If it receives a listen command, it waits for data packet. After receiving the data packet, the main radio sends an Ack to the transmitter and then switches to sleep mode. If no packet is received, it will switch to sleep mode until the listening time is over. Fig.13 (c) shows the flowchart of the main radio.



(a) Wake-up radio



(b) PIC



(c) Main radio

Figure 5.6 Flowcharts of the node without framework

V.3.2 Simulation scenario

As mentioned earlier, the wake-up radio doesn't need to operate at the same frequency as the main radio. So, it is common to see the wake-up radio operating at 868MHz, while the main radio operates at 2.4GHz [6]. Under these conditions, the attenuation of the WUR in the transmission channel is reduced compared to the working frequency of 2.4GHz, and the data rate of the main radio is higher compared to 868MHz. However, despite this frequency variation, due to the ultra-low power requirements of the WUR, the maximum transmission distance of the wake-up radio is still less than that of the main radio [7]. Therefore, some scenarios need to cover communication through multi-hop, as shown in Figure 5.7. In this configuration, the base station sends data packets (DPs) to nodes N1 and N2. The main radio of N2 needs to be woken up by the WUP of N1 to receive the DP, and then sends an Ack after successful reception to signal the base station.

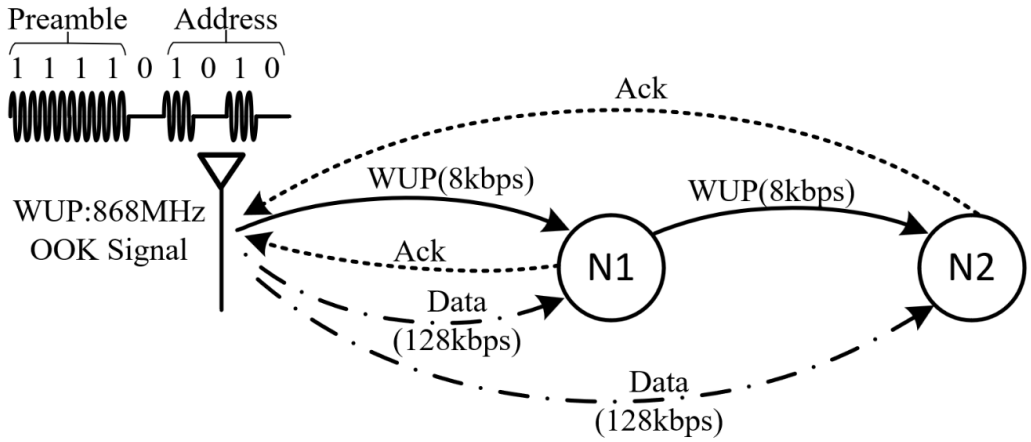


Figure 5.7 Wake-up and data transmission description

To estimate the quality of the communication, it is particularly important to account for the probability of false wake-up or missed wake-up as it can affect not only the function of one single node but also the overall data transmission. E. g., in the figure, the transmitter cannot wake up N2 directly, so it wakes up N1 and N1 wakes up N2. Therefore, a missed wake-up on N1 will result in a missed wake-up on N2.

The test scenario, depicted in Figure 5.8, features a base station and three nodes, where the D_{wu} is also indicated. To ensure a thorough evaluation, the scenario is divided into three cases with the nodes placed at varying distances: Case 1 involves the node N1, positioned relatively

close to the base station. Case 2 involves N1 and N2 (hop=1), in correspondence with Figure 5.7. Case 3 features N3, located at the boundary of D_{wu}. The base station transmits data to the nodes and continues to resend until an Ack packet is received, or the time limit is reached, after which the next transmission begins. Each case is simulated for a duration of 100 hours. In the simulation, no transmission collisions are considered.

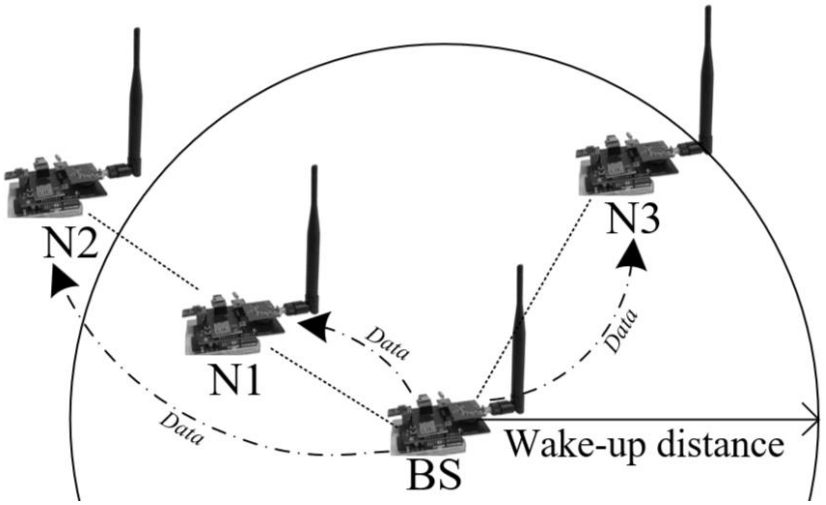


Figure 5.8 OMNeT++ sensor network simulation scenario

V.3.3 Implemented models

To compare theoretical hypothesis and practical validation, we develop 4 models. Each of these models is applied to the scenarios described above and utilizing the 2-layer WUR with a series-mounted rectifier topology as an illustrative example. We primarily select this specific setup to focus on comparing the models rather than evaluating the performance of various WUR setups.

The first model is based on the on-off methods, which considers the node wakes up if the transmission distance is less than the wake-up distance; otherwise, the node does not wake up. The second model and the third model are based on simplified mathematical equations and SPICE simulations respectively, both of which are described in chapter III. And then the fourth one is based on experimental measurements. The packets propagate according to the timeline depicted in Figure 5.9. And the parameters used for the 4 models are summarized in Table 5.1.

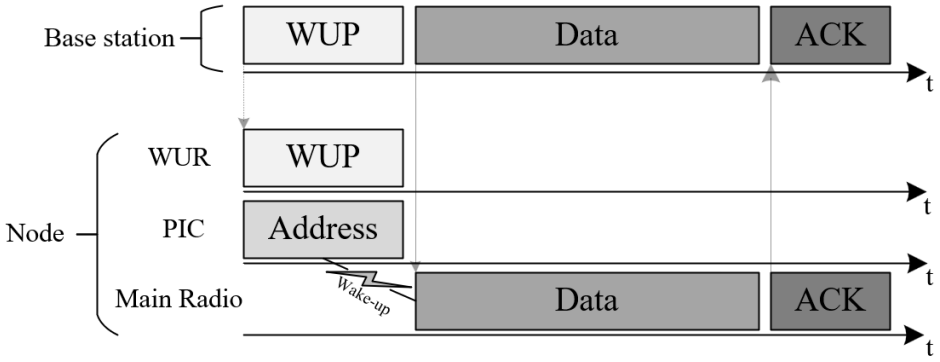


Figure 5.9 Timeline of packet propagating

Table 5.1 Parameters used for the models' evaluation

Parameter	Description	Value
f	Frequency of wake-up radio	868MHz
D_{wu}	Wake-up packet range	8.06m
D_d	Data packet range	50m
R_{wu}	Data rate of wake-up packet	8kbps
R_d	Data rate of data packet	128kbps
L_{WUP}	Wake-up packet length	9bits
L_{DP}	Data packet length	32bits
P_{trans}	Transmit power of base station	+10dBm
P_{idle}^{PIC}	Consumption when PIC is idle	60nW
P_{awake}^{PIC}	Consumption when PIC is awake	360μW
P_{idle}^{radio}	Consumption when main radio is idle	60μW
P_{listen}^{radio}	Consumption when main radio listens	1.5mW
P_{Rx}^{radio}	Consumption when main radio receives	44.1mW
P_{Tx}^{radio}	Consumption when main radio transmits	90mW

V.3.4 Simulation results

Energy per useful bit

In the first simple model, since there is no false wake-up, the energy per bit (EPB) value of the 4 nodes is the same. For other models, different false wake-up equations and power consumption have a greater impact on EPB, especially the EPB of the Node3 on the boundary is quite dependent on the model. Therefore, actual measurement is necessary. The EPB obtained for each model are summarized in Table 5.2, where the reference EPB is given by the model based on the on-off model.

Table 5.2 The normalize energy per bit of each case in 4 models

Type of model	Normalize energy per bit		
	Case1	***Case2***	***Case3***
On-off	1	1	1
Theory	1.21	2.66	1.74
Simulation	1.284	3.68	17.72
Measurement	1.283	3.67	17.71

Simulation performance

The CPU time and simulated events (real-time) per second for each model are collectively evaluated across all three cases within the scenario, and executed simulations for a long time (1000 hours). Table 5.3 provides a comparison of model performances in the scenario to get an accuracy/CPU time ratio for each model.

The mathematical prediction gives quite accurate results for a very low development time, at the cost of a higher CPU time, most particularly if an iterative calculus is required (Newton method). On the other hand, the on-off model is quite fast but the false/missed wake-up prediction is not accurate in case the transmit distance is close to the D_{wu} distance. The reference CPU time is around 10 seconds for the entire simulation with the on-off model. Besides, our simplified Wallis method is faster than Newton method in the theoretical model with no significant accuracy loss.

Table 5.3 Comparison of models' performances

Type of model	Parameter of performances	
	CPU time (sec)	***speed (Event/sec)***
On-off	10.54	318831
Theory(Newton)	18.71	257073
Theory'(wallis)	15.51	310156
SPICE simulation	15.04	299406
Measurement	13.49	315294

Comparison of power consumption: original vs optimized WUR

As an extension of our initial development and simulations, we highlight the contribution of optimized WUR to the wake-up process by inserting the previously described heterogeneous WUR into our OMNeT++ simulations. We adopt the SPICE simulation model. Using the same scenarios, we execute simulations for a span of 100 hours.

False/missed wake-up during transmission can result in increased transmission time and average energy per transmitted bit. Table III presents the simulation results for normalized energy per bit (referenced to CMOS comparator's typical) and false/missed wake-up probability.

For N1 in Case 1, which is located closer to the base station, the results of the simulations do not vary much. However, for Case 3 of the TLV3491, its consumption is much greater due to a higher false/missed wake-up probability at the boundary, which is located at 7.2m. The error probability of TLV3491 exceeds 0.8 at this location, while the CMOS comparator's is 0.47. Furthermore, the EPB for Case 2 of the CMOS comparator is higher than for Case 3 because the error of N1 may result in the error of N2.

Table 5.4 Comparison of normalize energy per bit and false/missed wake-up probability for heterogeneous WUR and commercial WUR

WUR with different comparator	**Normalize energy per bit**			**False/missed wake-up (%)**		
	Case1	***Case2***	***Case3***	***Case1***	***Case2***	***Case3***
TLV3491	1.24	3.58	15.61	27.6	73.0	93.1
CMOS comparator (Typical)	1	2.29	1.87	2.4	57.8	48.2
CMOS comparator (Worst)	1.14	2.84	2.20	14.8	65.0	56

Furthermore, we compared the performance of the 4-layer WUR and the 2-layer WUR, utilizing the measurement model. Under the same conditions and within three cases of scenario, the false/missed wake-up of the 4-layer WUR are nearly absent, thus emphasizing the importance of sensitivity enhancement for WURs. Table 5.5 shows the simulation results for normalized energy per bit (referenced to the 4-layer prototype) and false wake-up probability.

Table 5.5 Comparison of normalize energy per bit and false wake-up probability for 4-layer and 2-layer prototypes

WUR	**Normalize energy per bit**			**False/missed wake-up (%)**		
	Case1	***Case2***	***Case3***	***Case1***	***Case2***	***Case3***
2-layer prototype	1.27	3.67	15.99	27.6	73.0	93.1
4-layer prototype	1	1.0004	1.0007	0	0.017	0.067

The results of these simulations highlight the contribution of the optimized WUR to lower power consumption and emphasize the importance of accurately take into account the physical (electrical) behavior of the circuits in high level (sensor level) simulations.

V.4 Evaluation of node's performances with framework

The objective of this section is to demonstrate the process and performance of simulating WUR with the INET framework. We first create a comprehensive wireless network model for WUR using the INET framework, and then add mobility to nodes in the model for performance evaluation. Afterwards, we perform a comparative analysis of the advantages and disadvantages of WUR nodes for three different rectifier topologies. Frameworks can provide a wide range of pre-existing models and modules, significantly reducing development time and complexity. However, this comes at the cost of increased CPU time during simulation.

V.4.1 INET framework

The INET framework is an open source OMNeT++ simulation environment model library, which provides a great diversity of protocols, agents and other models for communication network researchers [8]. By using this framework, we can conduct a comprehensive analysis of node performance and key parameters under different conditions, which can help us understand and construct the entire network system more quickly, thus optimize overall network performance [9].

We chose the INET framework because it's considered the standard protocol model library for OMNeT++, containing a large number of protocols and components. This enables us to perform the network simulation and analysis in a unified environment. Additionally, in the list of simulation models officially provided by OMNeT++, many frameworks are no longer updated, which leads to incompatibility with the latest OMNeT++ 6.0 version, or may not be suitable for WSN simulation. Therefore, the INET framework is our first choice.

In particular, while building our wireless network models and adjusting configurations, we not only employ wireless node modules equipped with wireless network interfaces, but also incorporate pre-existing support modules from the INET framework. These include the 'radioMedium' module (serving as a data transmission medium for radio wave propagation) and the 'visualizer' module (serving as a visualization layer showing the effects of signals, messages, and radio wave propagation) [8],[10]. Using these modules can also simplify the

construction process and accelerated our development speed. The wireless network structure using INET framework is depicted in Figure 5.10.

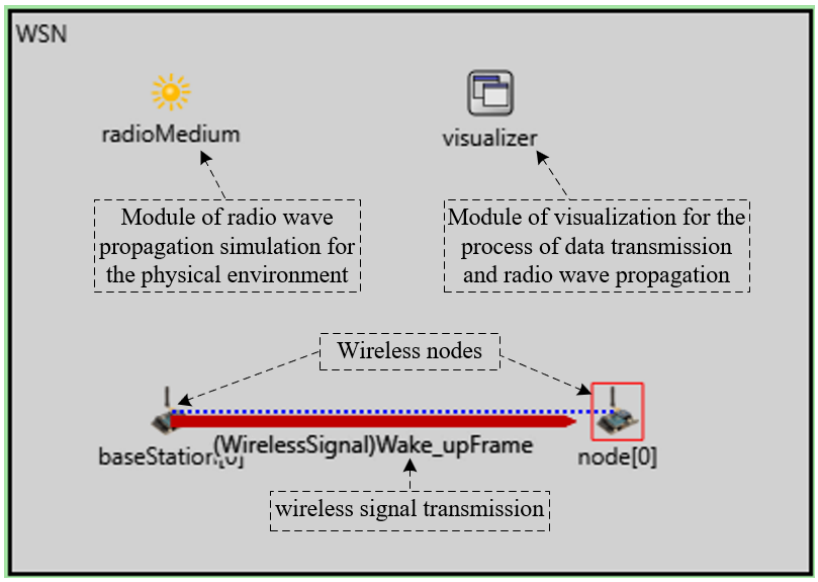


Figure 5.10 The structure of the WSN using INET framework

V.4.2 Modeling description

In the communication model of wireless nodes within the INET framework, packet serves as the fundamental information unit of network transmission [11]. Each packet is mainly composed of two parts: header (containing information such as the addresses of the source and destination systems) and body (containing the actual data to be transmitted) [12]. When the sender wants to send a packet, its application layer first generates the original data, then sends a message object representing the packet to the lower layers. Each layer will add or remove respective fields in the header. In the physical layer, this packaged data is converted into binary and transmitted through the physical medium. And when the packet arrives at the receiver, each layer reads and removes its respective header information, passing the remaining part to the upper layer, until the data reaches the application layer. The cross-layer communication process of wireless nodes in the INET framework is shown in Figure 5.11.

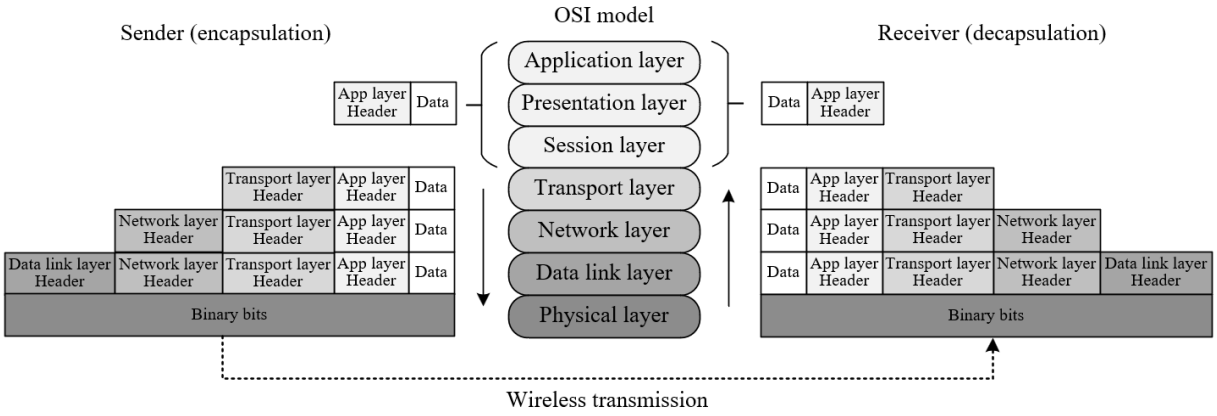


Figure 5.11 Cross-layer communication of wireless node in INET framework

In our simulation, to focus more on the wireless signal propagation at the physical layer, we simplify the model of the wireless node in INET framework. The pre-defined network and transport layers in the model are removed, and the application layer is replaced with a simple module that can be easier modified and controlled. As shown in Figure 5.12, all these components build a wireless sensor network system, and each component is interconnected in a low-coupling manner through the INET standard interface, which is convenient for various parts of the system to be flexibly modified and expanded. Among them, solid arrows represent message passing, while dotted arrows represent simple function calls. For example, most modules call functions in resources to indicate that energy is being consumed.

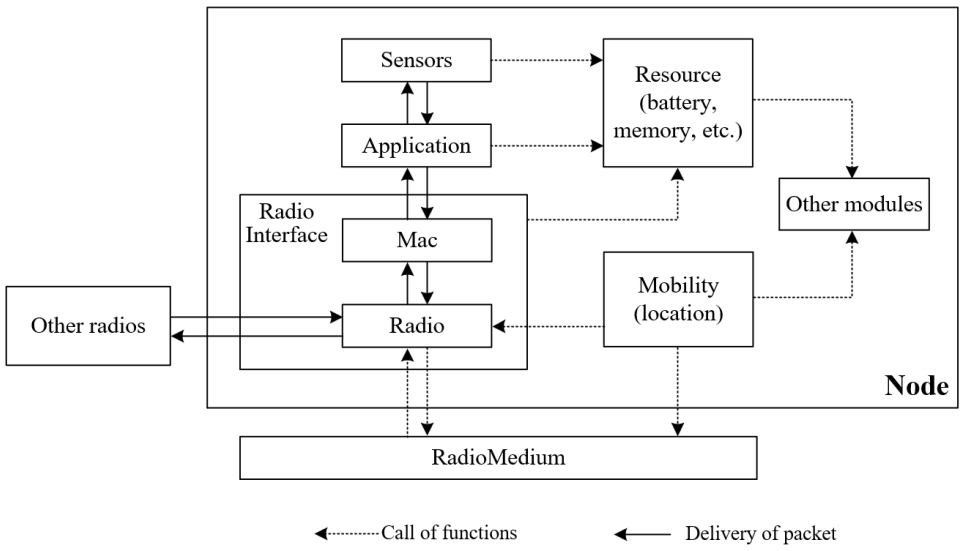
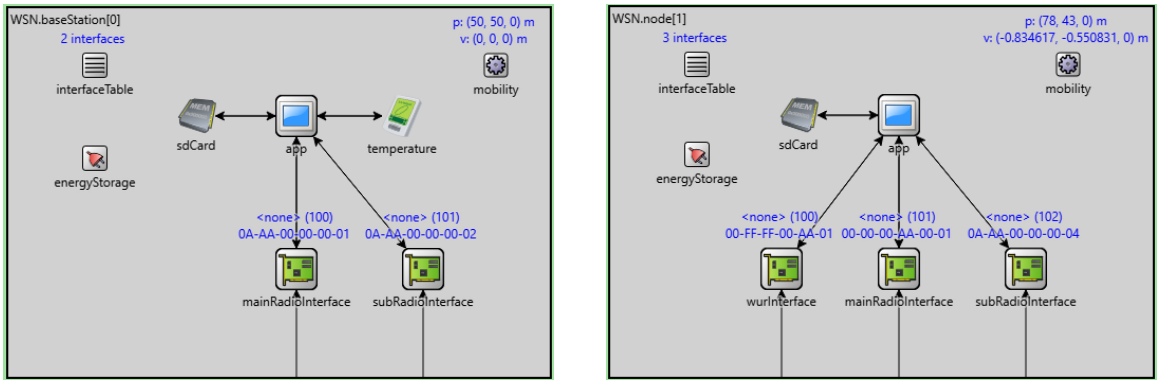


Figure 5.12 Interaction flow among modules of the simplified wireless node in INET framework

To accurately simulate the processes of data measurement, transmission, and their energy

consumption, we introduce simple modules acting as sensors. Furthermore, besides the wake-up radio interface, we also introduce two additional radio interface models (main radio interface and 868MHz radio interface) for data packets' transmission and reception, and to wake up the wake-up radio. This configuration is the same as the Arduino shield prototype's setup described in Section IV.4. All these advancements contribute to a more comprehensive node functionality. Figure 5.13 depicts the composite module of our base station and node.



(a) Base station (b) Node

Figure 5.13 The composite module of base station and node with INET framework in OMNeT++

In the following, we will present the models and their components of the base station, node, and radio medium, respectively.

Base station

(1) App: In conventional network models, the application layer serves as the interface between the user and the network, responsible for sending and processing network data [13]. Typically, this layer contains programs that are run by users to accomplish specified tasks. In our model, the application layer module acts as the control center of the node, providing functionalities such as decision-making, time control, and standard interfaces. Therefore, we can regard the application layer as the "Arduino" micro-controller of our simulation model, setting high-level strategies for network communication, such as when to send data and how to process received data. This application module receives information from the radio interfaces and sensors, and processes it based on its type. Figure 5.14 presents the flowchart of the application module at the base station.

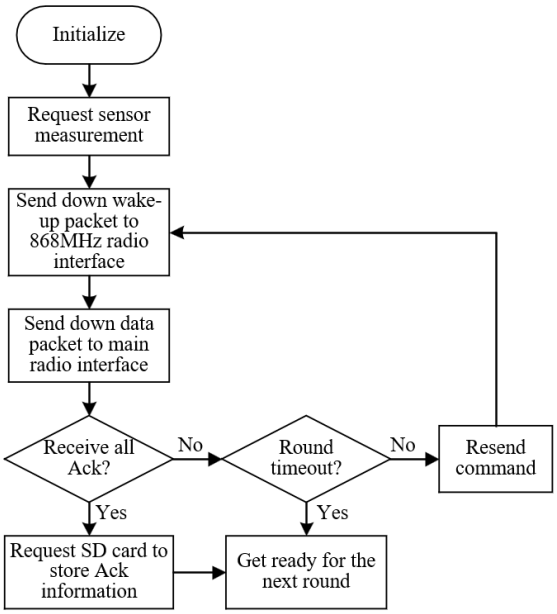


Figure 5.14 Flowchart of the app at the base station with INET framework

(2) Radio interface: Each radio interface includes a MAC layer and a physical layer, as shown in Figure 5.15, the composite module in OMNeT++. There are two interfaces in the base station, which represent the main radio and the 868MHz radio, respectively.

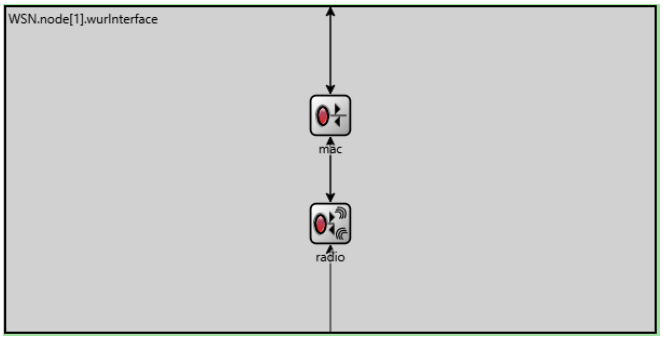


Figure 5.15 The composite module of the radio interface with INET framework in OMNeT++

Among them, the MAC layer is responsible for encapsulating the bitstream received from the physical layer into data frames for use by the upper-layer modules. It also processes packets sent by the application layer, handling packet encapsulation and managing the state of the radio as required. In addition, the MAC layer also decides whether to send acknowledge (Ack) [14]. Here, we adopt and expand a simple MAC module from the INET framework named 'AckingMac'. This simple MAC module provides basic functionality for packet encapsulation and decapsulation [15]. Figure 5.14 presents the flowchart of the MAC layer in the radio interface module at the base station. Notably, the two interfaces at the base station can use the same MAC layer. For the 868MHz radio, it only needs to be set not to use Ack in the '.ini' file

(user configuration file).

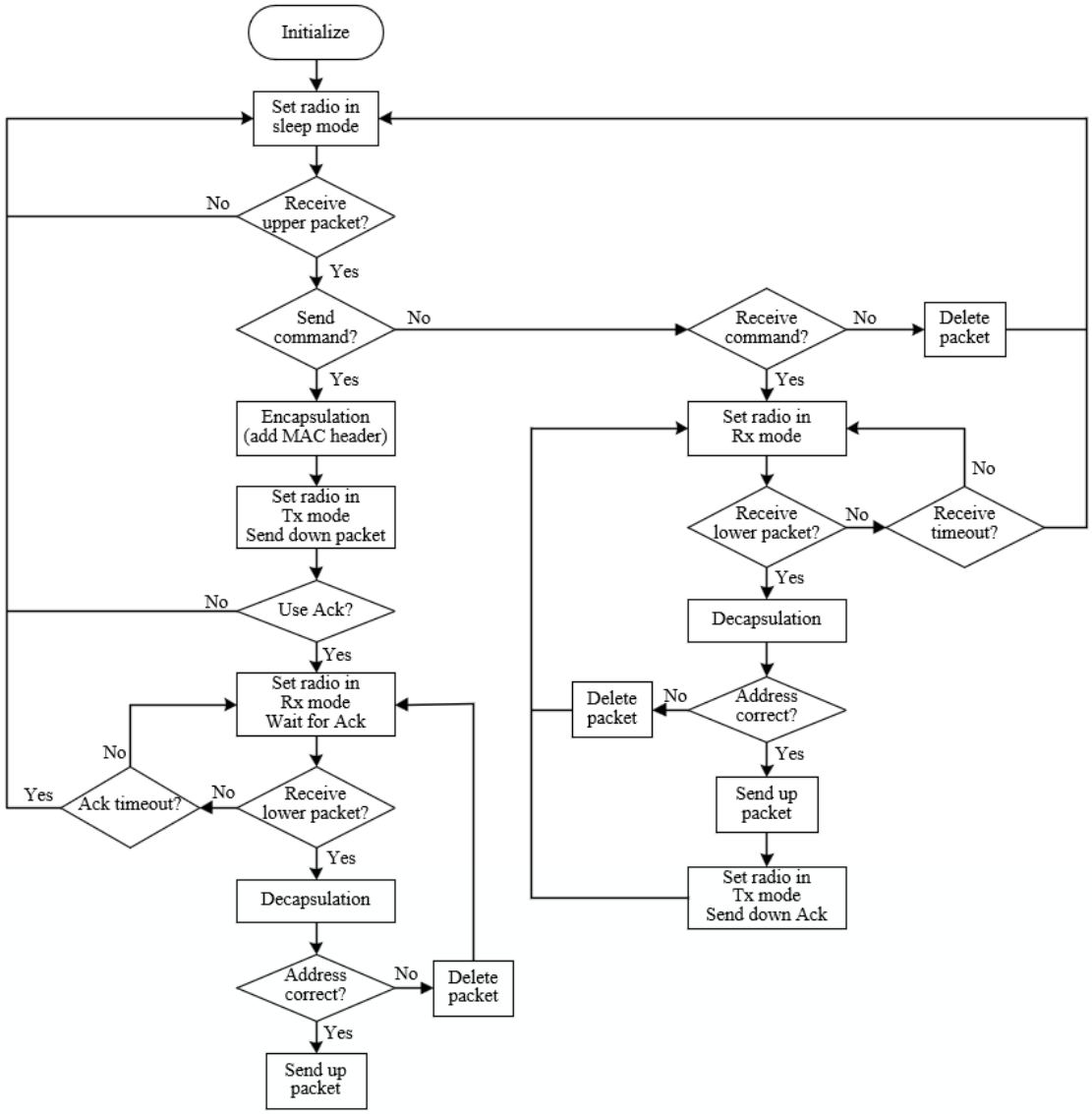


Figure 5.16 Flowchart of MAC layer in radio Interface at the base station with INET framework

Furthermore, the physical layer of the radio interface module needs to handle each received data packet based on the strength of the received signals. It first decides whether the packet can be successfully received, and then whether to open the packet for upward transmission or to consider it as noise and discard it. In our model, both radios use the 'UnitDiskRadio' from the INET framework. We simply need to set up the power of background noise, communication range, sensitivity, and energy consumption in the initialization file.

Node

(1) App: In the node, the application layer is usually in sleep mode, only being woken up

when a valid wake-up signal is received. And then, it analyses the address extracted from the WUR and carries out the corresponding operations, such as awakening the main radio to receive data packets or transmitting wake-up signals to nearby nodes via the 868MHz radio. The flowchart of the application layer is shown in Figure 5.17.

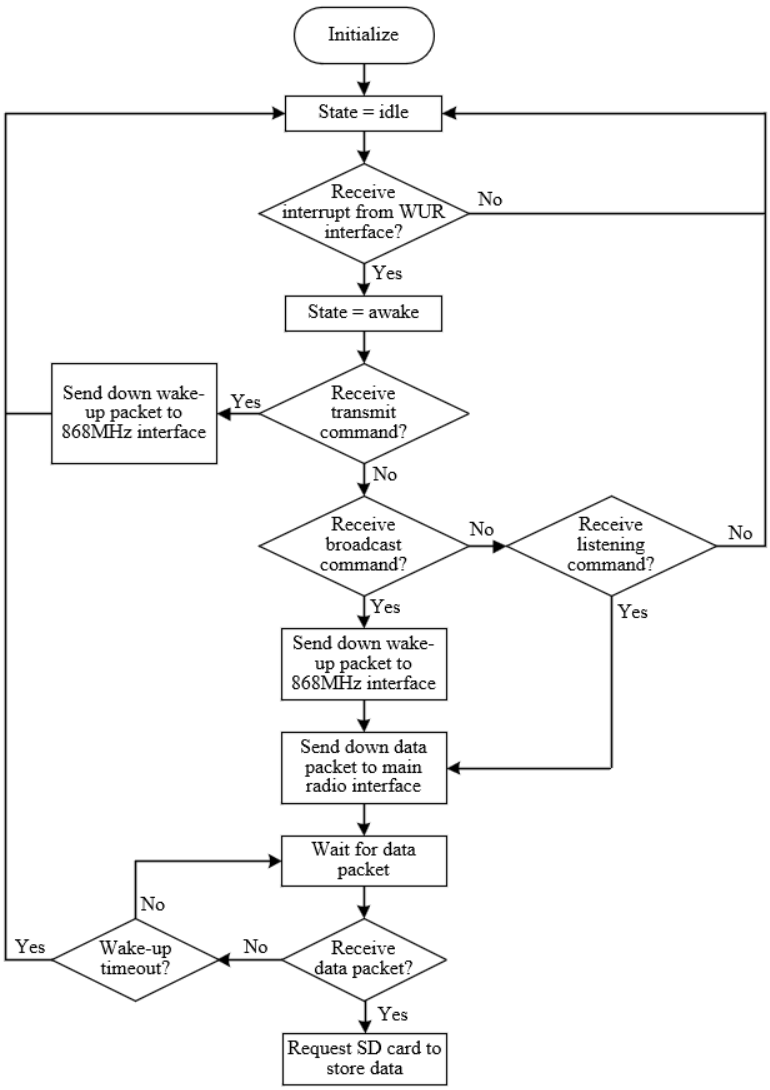


Figure 5.17 Flowchart of the app at the node with INET framework

(2) Radio interface: There are three radio interfaces within the node, including the main radio responsible for receiving data packets and the 868MHz radio for awakening other nodes. The interfaces of the main radio and the 868MHz radio are the same as those in the base station. We only need to set their self-address, whether to use the Ack, transmission range, and power consumption in the '.ini' file.

In addition, the node also contains a wake-up radio interface. In the MAC layer of the WUR,

we made some modifications to allow it to always be in receiving mode without putting the radio into sleep. It serves as the PIC micro-controller, checking whether the received address is correct and forwarding packets to the application layer.

And for the physical layer of the WUR, we conduct a more detailed and accurate modeling. Although the INET framework provides a wide range of physical layer radio models, from the simple ‘UnitDiskRadio’ to more advanced models with modulation implementation, none of these models are specifically designed for WUR or OOK modulation. To address this, we enhance the standard ‘UnitDiskRadio’ model [15], transforming it into the 'WakeUpRadio' model, as described in Section V.3. The revised model can execute tasks such as computing packet error rates, recognizing addresses, and passing the wake-up signal to the upper layer. The flowchart of this model is depicted in Figure 5.18.

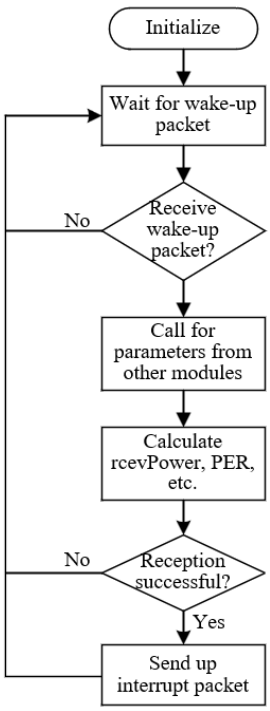


Figure 5. 18 Flowchart of the wake-up radio at the node with INET framework

Radio Medium

When simulating wireless network with INET framework, an additional module is required to represent the transmission medium, i.e., the Radio medium module. It can realistically reflect the physical processes through the simulation of the wireless communication environment. We adopt the ‘UnitdiskRadioMedium’ module, which handles the modeling of signal propagation

and mobility attenuation of signals, taking into account interference and other physical phenomena. As shown in Figure 5.19, ‘UnitdiskRadioMedium’ incorporates other components, which model physical processes such as the propagation of radio signals in space, the analog representation of radio signals, and the decrease in power as signals propagate through space.

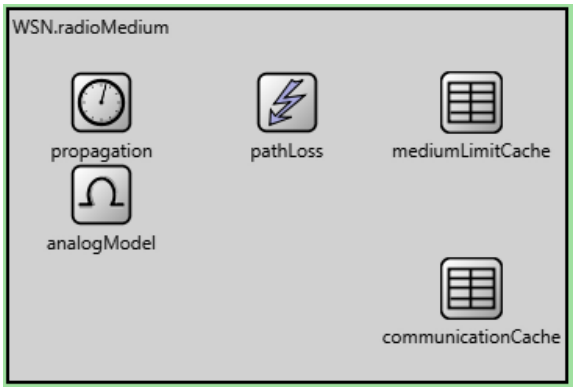


Figure 5.19 Composite module for ‘UnitdiskRadioMedium’ of INET framework in OMNeT++

V.4.3 Simulation scenario

In wireless sensor network, the node can be either stationary or mobile. The 'Mobility' module is responsible for controlling and managing the movement of nodes. Whenever the position of a node changes, this module updates the graphical representation and publishes the new location on the relevant modules of the node, so that other modules are informed in real time. Moreover, the 'Mobility' module is also in charge of handling collisions and boundary conditions. In our simulation scenario, in addition to maintaining the “wake-up and data transmission” settings described in Figure 5.7, we further incorporated the simulation of nodes’ movements to compare the performances of 4-layer WUR nodes with three different rectifier topologies.

For a comprehensive evaluation, we set different node positions and moving trajectories, which are divided into three cases, as shown in Figure 5.20:

Case 1 involves the node N1, which is located near the base station, and performs a uniform linear movement back and forth on a specified path.

Case 2 includes the nodes N2, N3 and N4. The nodes move along circular paths, but at different speeds. N4 needs to wake up from N2 or N3 to receive data packets. Their initial position is determined by the wake-up distance of the voltage doubler topology, which has the

lowest sensitivity. Half of the circular movements of N2 and N3 remained within this wake-up distance, and the other half exceeded this range. While maintaining node positions, we simulated two other topologies. It is worth noting that the wake-up range is larger due to the better sensitivity of the single-diode (series-mounted and shunt-mounted) topologies, but this distance still does not include the position of N4.

Case 3 merges nodes from cases 1 and 2 and adds the node N5. This node continuously moves eastward until it disappears. Our loss criterion is that if the base station does not receive its Ack from a node for 10 consecutive rounds. Then the base station eliminates this lost node and continues to transmit packets to other nodes. And our main observation points include the time when the base station receives the packet loss information, the location of N5 when this loss information is received, the total number of packets that N5 has acquired, and whether other nodes can continue to operate. Moreover, when N5 moves, it can be awakened by surrounding nodes or also activate those nearby nodes.

The parameters used are the same as the actual parameters in the Arduino shield in Chapter IV. The strategy for wake-up and retransmission remains the same: the base station sends a wake-up packet and a DP to the node until an Ack is obtained or the time limit is reached, which marks the start of the next transmission. Each simulation lasts 100 hours without considering transmission collisions.

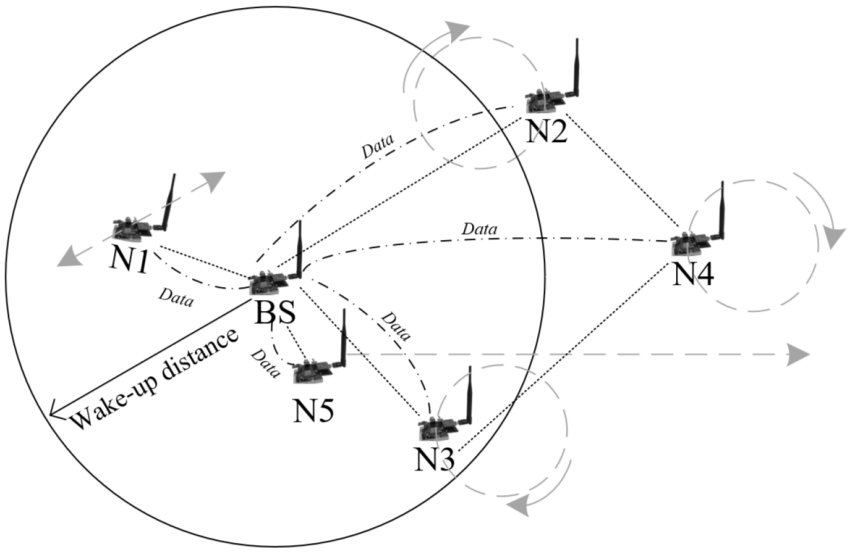


Figure 5.20 OMNeT++ sensor network simulation scenario with movement track

V.4.4 Simulation results

Energy per useful bit and false/missed wake-up

To evaluate the performances of different WUR topologies, we adopt the measurement model and the test results of the 4-layer WUR for the three topologies. The energy per bit (EPB) and the false/missed wake-up for each case are summarized in Table 5.6, where the reference EPB is based on the Case 1 of voltage doubler typology WUR.

In Case 1, the voltage doubler topology shows the lowest EPB. This is because it has the lowest probability of false/missed wake-up over shorter distances. The other two single-diode topologies also perform well in this case, with very few false/missed wake-up.

In Case 2, the voltage doubler has the highest EPB due to its lowest sensitivity. While the sensitivities of the two single-diode topologies are comparable, the series-mounted topology has a slightly lower false/missed wake-up close to the boundary, resulting in a reduced EPB.

In Case 3, all three topologies have higher EPB than the first two cases. This rise can be attributed to the continuous retransmission from the base station to Node5. Additionally, false/missed wake-up from Case 1 are also considered. It is worth noting that the false/missed wake-up of the voltage doubler is lower in this case compared to case 2. This improvement is due to Node5 helping neighboring nodes relay wake-up packets early in the simulation. However, there is no significant difference between case 3 and case 2 for the two single-diode topologies.

In conclusion, voltage doubler topology WUR is the first choice for short-distance communication. Series-mounted topology WUR is preferred for communication at distances close to the edge of sensitivity. And shunt-mounted topology WUR serves as a balanced choice for mixed communication distances.

Table 5.6 Comparison of normalize energy per bit and false wake-up probability for different rectifier topologies of WUR

WUR	**Normalize energy per bit**			**False/missed wake-up (%)**		
	Case1	***Case2***	***Case3***	***Case1***	***Case2***	***Case3***
Series-mounted	1.012	2.58	2.85	2.49	71.3	71.2
Shunt-mounted	1.002	2.62	2.96	0.41	74.6	74.7
Voltage doubler	1	3.50	4.15	0.033	87.7	80.7

Analysis of Node5 in Case 3

Furthermore, Table 5.7 provides the simulation results of Node5 in Case 3 for three topologies WUR, which shows the time from when the base station realizes that Node 5 is lost, the corresponding distance between Node 5, the base station at this time, and the total number of DPs received by Node 5.

Since the sensitivities of the two single-diode topologies are similar, and the base station judges the loss of nodes according to the number of rounds, it is possible for the base station to realize the loss of N5 at the same time for the two single-diode topologies. Considering that a node moves at a uniform speed, at a given time, its distance from the base station remains the same. However, we observed that the shunt-mounted topology received more packets than the series-mounted topology. This is because the shunt-mounted topology has a lower false/missed wake-up most of the time except at the border. Although the series-mounted topology may perform better at the border, the high false/missed wake-up in these regions means that it can actually receive a limited number of packets.

For the voltage doubler topology, the base station detects the absence of N5 earlier than other topologies due to its lowest sensitivity. Therefore, when node loss is detected, Node5 is located closer to the base station than the distance reported for the single diode configuration. This also results in the voltage doubler topology WUR receiving fewer DPs overall.

Table 5.7 Simulation results of Node5 in Case 3 for three topologies WUR

WUR	Lost time (s)	Lost distance (m)	Number of DP received
Series-mounted	6540	70.4	83
Shunt-mounted	6540	70.4	87
Voltage doubler	5940	64.4	68

Comparison of simulation performance with and without framework

In addition, we also compare the simulation CPU time and speed with and without the INET framework. We employ the 2-layer WUR's measurement model and scenario detailed in Section V.3, where nodes remain stationary. As shown in Table 5.8, there is a clear difference in the CPU time and the number of simulated events per second between the two models. The CPU time of the model using INET framework significantly increased, and the simulation speed decreased by nearly half. This shows that although developing the OMNeT++ model within a

framework can shorten the development time, the complexity of the internal module structure of the framework increases the number of events that need to be processed, resulting in longer running time and lower speed.

Table 5.8 Comparison of models' performances with and without INET Framework

Type of model	**Parameter of performances**	
	CPU time (sec)	***speed (Event/sec)***
Without INET framework	13.49	315294
With INET framework	178.63	179033

V.5 Conclusion

In this chapter, we focus on using a network simulator to evaluate the performance of wake-up radio in wireless sensor networks. Through OMNeT++ software, we simulate the performance of WUR system at low cost and efficiently. Our research is the development of the physical layer in the OSI model, based on the results from theoretical modeling, SPICE simulation results, and prototype analysis from our previous work.

We first develop several models without frameworks and compare their performance. We provide a comparison of these models' performances in a simple scenario to get an accuracy/CPU time ratio and energy per useful bit for each model. The results are provided as a preliminary study for the design and they can easily be transposed to more complex structures.

Subsequently, we extend the INET framework incorporating our WUR model to evaluate the overall performance of the WUR system. We build a complete WUR node model and add mobility, to compare the performances of WUR nodes with three different rectifier topologies.

In summary, this chapter highlights the value of using network simulator in WUR assessment and provides a comparison of different models and framework, providing a basis for future research on WUR in WSN.

V.6 Reference

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Chapter VI: General conclusion and perspective

VI.1 Conclusion

In this thesis, Chapter I initially presents the context of WSN, along with a brief introduction to the operating principle of wake-up radio. Subsequently, the motivation and objectives of this thesis are explained. And we then describe the methodology adopted for the study and provide the organizational structure.

Chapter II gives a review of the state-of-the-art for wake-up radio technology. We summarize the main characteristics of WUR based on our review of the literature, including type, technology, sensitivity, power consumption, frequency, modulation, latency, data rate, and addressability. And then, we chose to focus on the semi-active wake-up radio and analyzed how to select key components and topology of the circuit. And we provide the comparison of different topologies of rectifier. Moreover, we also perform a simulation of the WUR circuit, as well as a programming analysis of the addressing part.

In Chapter III, we turn our attention to the design and modeling of the semi-active wake-up radio. We start with a detailed SPICE simulation for various rectifier designs within our semi-active wake-up radio. While many publications typically discuss a single WUR topology, our research compares several topologies. Following this, we introduce our theoretical modeling of free space propagation, different rectifier topologies, as well as the analog and digital parts of the semi-active WUR. This approach not only considers the performance of the wake-up radio but also evaluates its impact on data transmission, serving as a complement to the conventional MAC layer modeling predominant in existing literature. This theoretical modeling can effectively estimate and optimize circuit performance and save significant time in prototype realization and measurement. And we also considered the issues of false wake-up and delay to quantify robustness, which is important to optimize the system performance. The chapter concludes with a comprehensive description of the prototype design process and its measurements.

In Chapter IV, we explore the optimization of the semi-active wake-up radio system. This

chapter is structured into three sections, each examining the optimization process from different perspectives. In the first part, we compare the performance of the semi-active wake-up radio using two integration methods: the classical PCB integration and our newly proposed heterogeneous fabrication. This heterogeneous WUR is a novel concept of WUR circuits, which is different from most publications. To validate our designs, we present the improvements in our optimized comparator using both worst-case and Monte-Carlo SPICE simulations. The next section focuses on our 4-layer PCB design which shows better sensitivity than the 2-layer WUR. Another contribution here is addressing electromagnetic compatibility (EMC) of the device. We summarize the design rules specifically to this low power and high frequency circuits. The final part of this chapter details the development process of an Arduino expansion board prototype equipped with the optimized 4-layer WUR. We discuss the entire process, from shielding design to implementation. Subsequently, we implement two distinct test scenarios on the WUR system and analyze the gathered data.

In Chapter V, we discuss the use of network simulators as effective tools in sensor networks. Particularly within the context of WSNs characterized by a vast number of nodes and constrained resources, simulators offer a way to decrease experimental costs and increase development efficiency. A contribution of our work is the comprehensive simulation of the WUR's physical layer in the network simulator, based on our previous investigations in theoretical modeling, circuit simulation results, and prototype measurements. We initially develop several models without a specific framework and ran simulations in OMNeT++, evaluating the performance among these models. Next, we further contribute to the field by extending the INET framework, incorporating the model of our WUR-based node. To evaluate the overall performance of the WUR system, the WUR-based node model is added with mobility features and its performances are compared across three distinct rectifier topologies.

In summary, this thesis gave a contribution to the development of wake-up radio design for sensor network applications, providing a system-level analysis that supports further research in this field.

VI.2 Perspective

As for the future work perspective, firstly, with reference to Chapter IV, we can produce the optimized CMOS comparator, and measure the heterogeneous wake-up radio.

Secondly, as previously mentioned, there is a notable difference between the measured and simulated sensitivity mainly due to the uncertain voltage offset of the comparator. Hence, we can remove the reference generator and use the offset of the MOSFET itself as the reference, as shown in Figure 6.1. In the case that the comparator offset remains the same, we will obtain an extra half of the input difference of the comparator, as well as a better sensitivity.

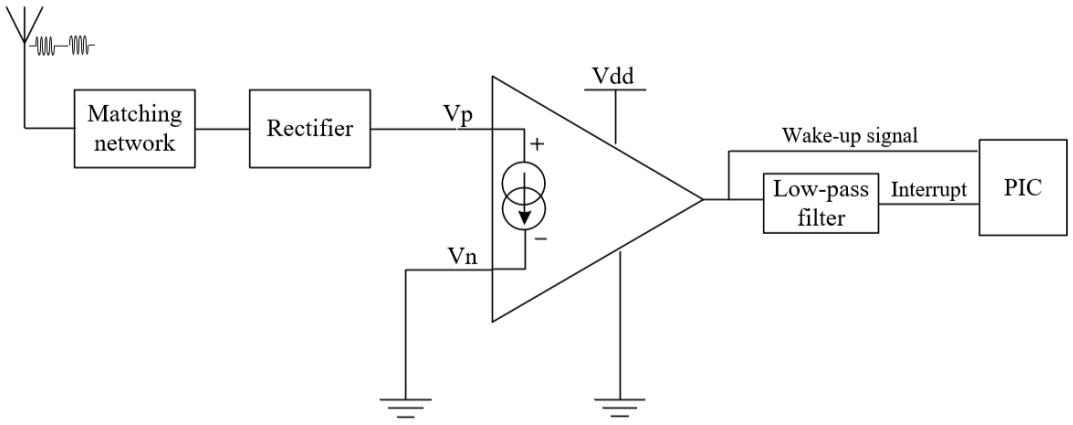

Figure 6.1 Block diagram of wake-up radio with comparator cathode grounded (Gnd as the reference)

Thirdly, the use of integrated rectifiers is worth exploring. The goal is to find a CMOS technology with a low V_{th} suitable for diodes in rectifiers [1], as depicted in Figure 6.2. By employing this CMOS rectifier, we might increase the received power to enhance system performance. Additionally, such integration offers the benefit of a compact design.

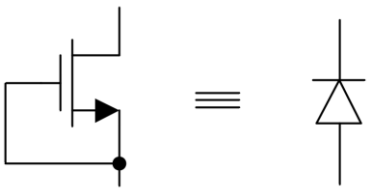

Figure 6.2 NMOS configuration using as a diode

Lastly, we can incorporate more complicated MAC layer protocols to refine our WUR models. In Chapter V, our focus is to model the physical layer of the WUR, while employing a simple MAC layer that only performs simple functions such as sending Acks. To better simulate

and control WUR communication, future work could consider implementing more complex MAC protocols within OMNeT++. MAC protocols play a key role in coordinating wake-up radio activities. They also assist nodes in efficiently sharing channels, preventing conflicts, and reducing latency, etc [2]. In addition to simulations in OMNeT++, we can also integrate these MAC protocols into our shield prototype. After testing the nodes, we can then compare the results.

VI.3 Reference

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