Cryptographic Extensions for Embedded Processors

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Security of Embedded Systems

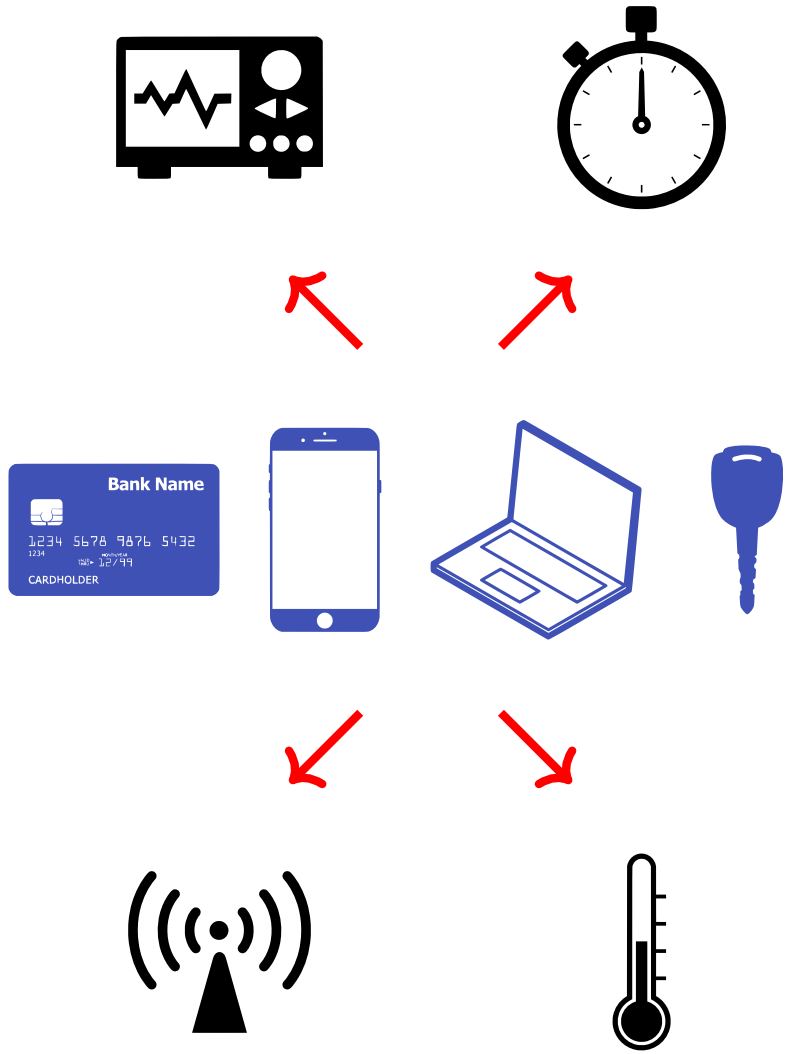
Cryptography:

Embedded systems use mathematically robust ciphers.

Side-channel attack (SCA):

Attack observing physical measurements:

- Execution time
- Power consumption
- Electromagnetic radiation
- Temperature
- ...



Different Implementation Methods

Hardware implementation:

- Efficient for a dedicated task
- Not very flexible

Software implementation:

- High flexibility
- Basic instructions are not designed for cryptography

Instruction set extension (ISE):

- Add new instructions for cryptographic operations
- A trade-off between software and hardware implementations
- Better performance while maintaining flexibility

Thesis Objectives

Develop ISEs to protect against SCA:

- New instructions for masking countermeasure
- Support high security levels
- Flexible masking solution implemented in software and hardware

Implementation and evaluation:

- Implement our ISEs on an open source RISC-V processor
- Performance and area results of the FPGA implementation
- Security assessment of our solutions

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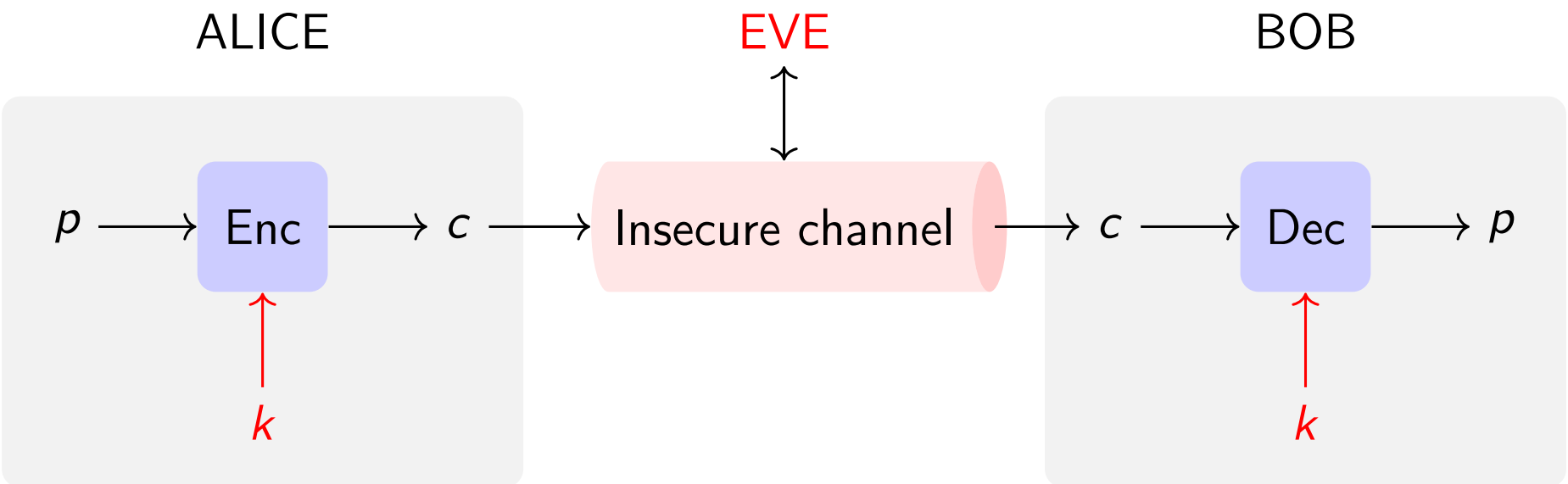
Symmetric Cryptography

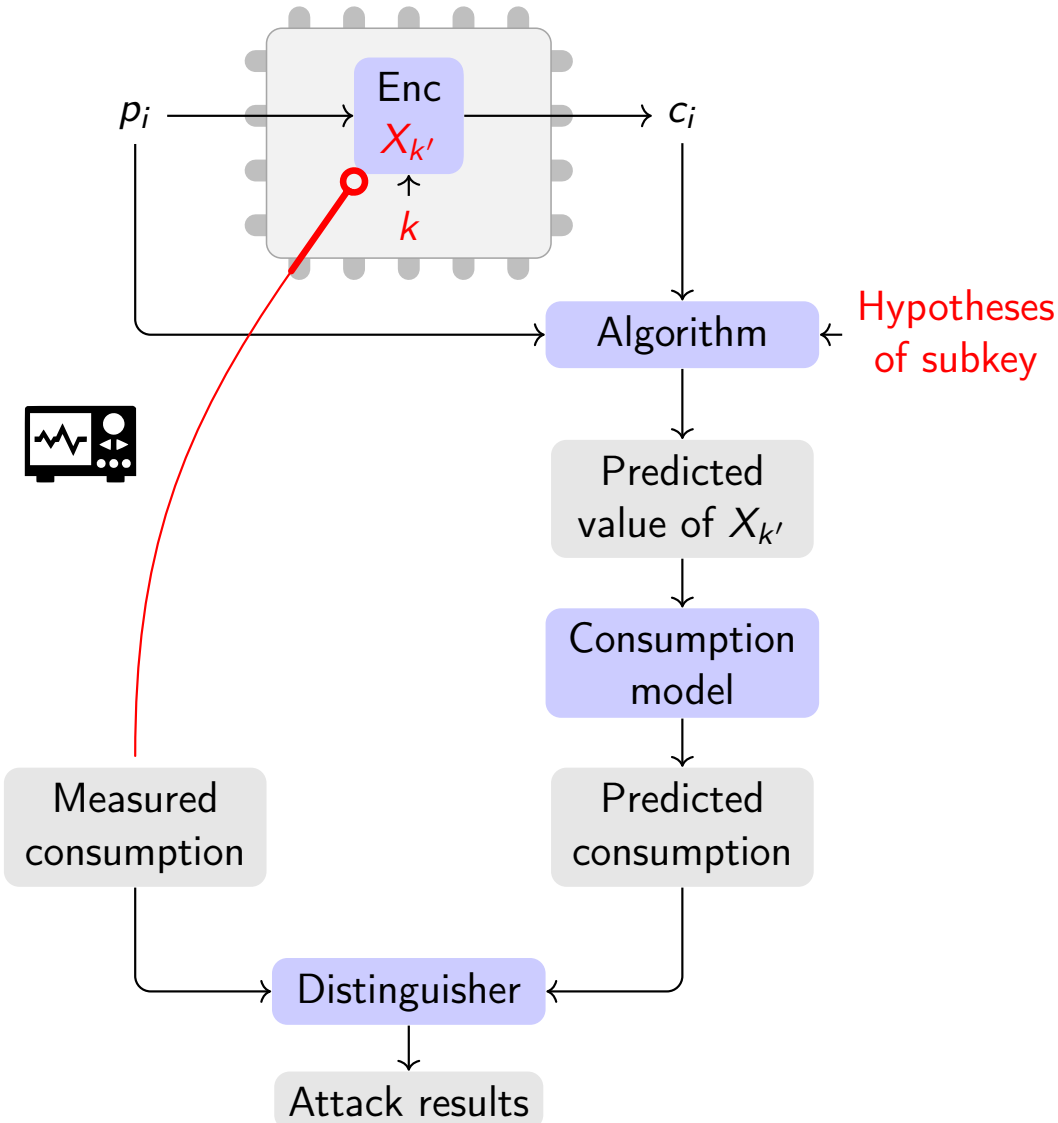


- Enc encrypts a plaintext p into a ciphertext c using a secret key k
- Dec decrypts the ciphertext c using the same secret key k
- Eve can read the ciphertext c without obtaining any secret

Power Analysis Attacks [KJJ99]

Measure power consumption to deduce secret data:

- Target a sensitive variable
- Measure consumption
- Predict consumption
- Statistical comparison



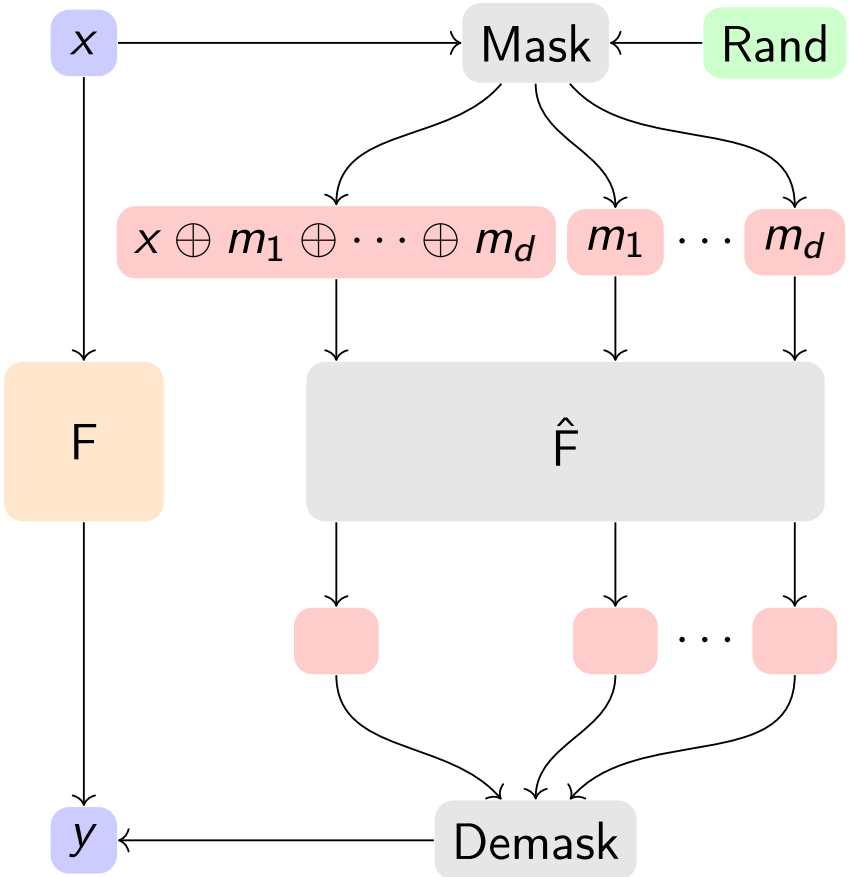
Masking Countermeasure [Cha+99]

Boolean masking of order d:

- Mask the variable x in $d+1$ shares

  $(x \oplus m_1 \oplus \cdots \oplus m_d, m_1, \cdots, m_d)$

  with $m_1, \cdots, m_d$ random masks
- Apply a d-order masked function $\hat{\mathrm{F}}$
- Demask to get y



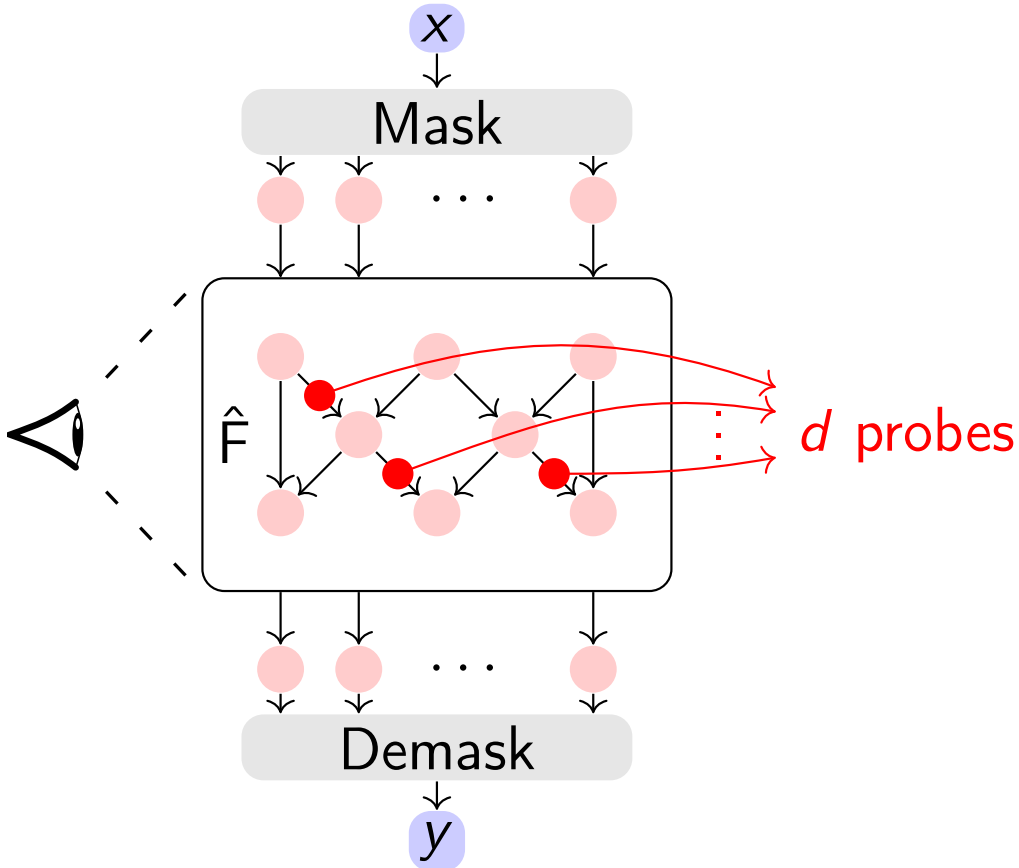
Evaluating the Security of Masked Functions

Security analysis:

- Performing SCA Attacks
- Proving security in a theoretical model

Probing model [ISW03]:

- Probe exact values of d intermediate variable
- Mask and demask functions are not probed



Recombinations of Shares [RP10]

Boolean AND masked at order 1:

- x masked in two shares (x_0, x_1)
- y masked in two shares (y_0, y_1)
- Get xy by demasking (z_0, z_1):

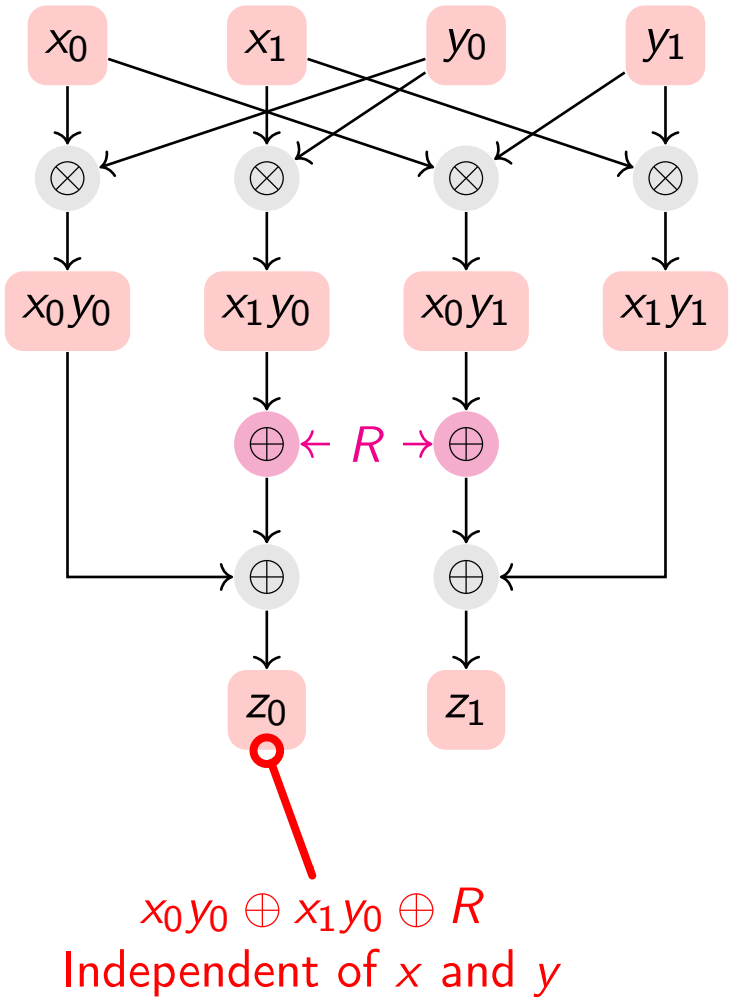
$$z_0 \oplus z_1 = xy$$

Recombinations of shares:

Masked variables can be demasked during calculation.

Prevent recombinations:

Add random values at well-chosen places.



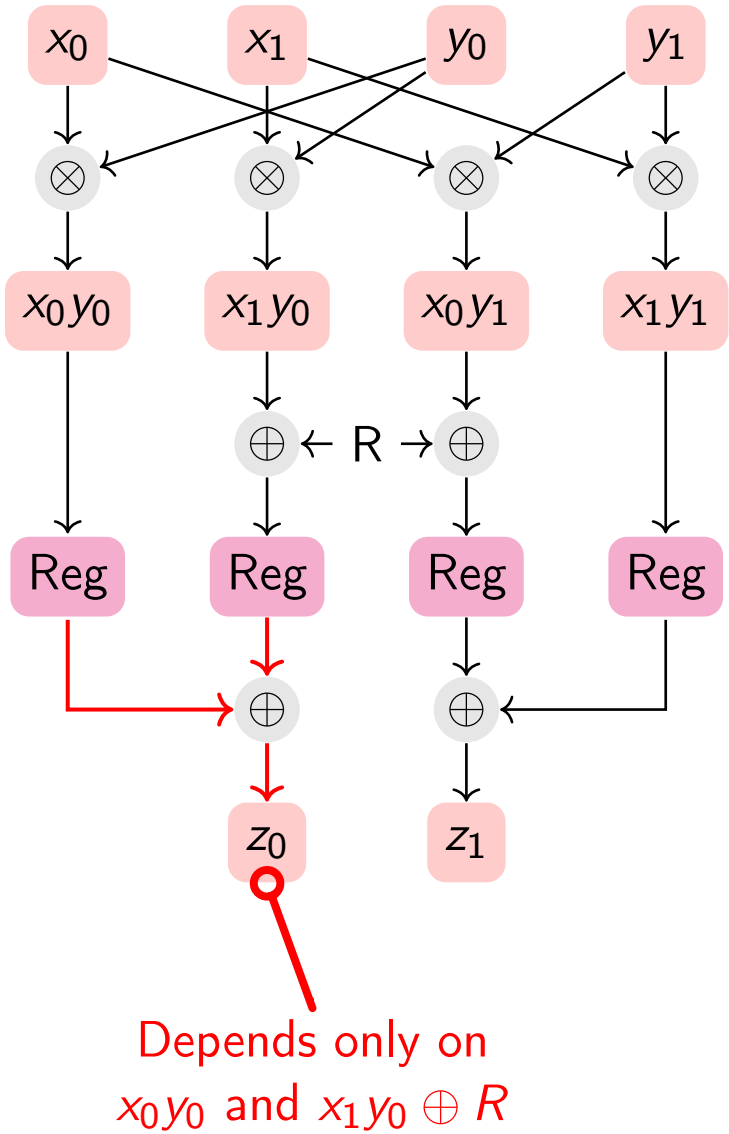
Security against Glitches

Glitch reconbinaisons [MPG05]:

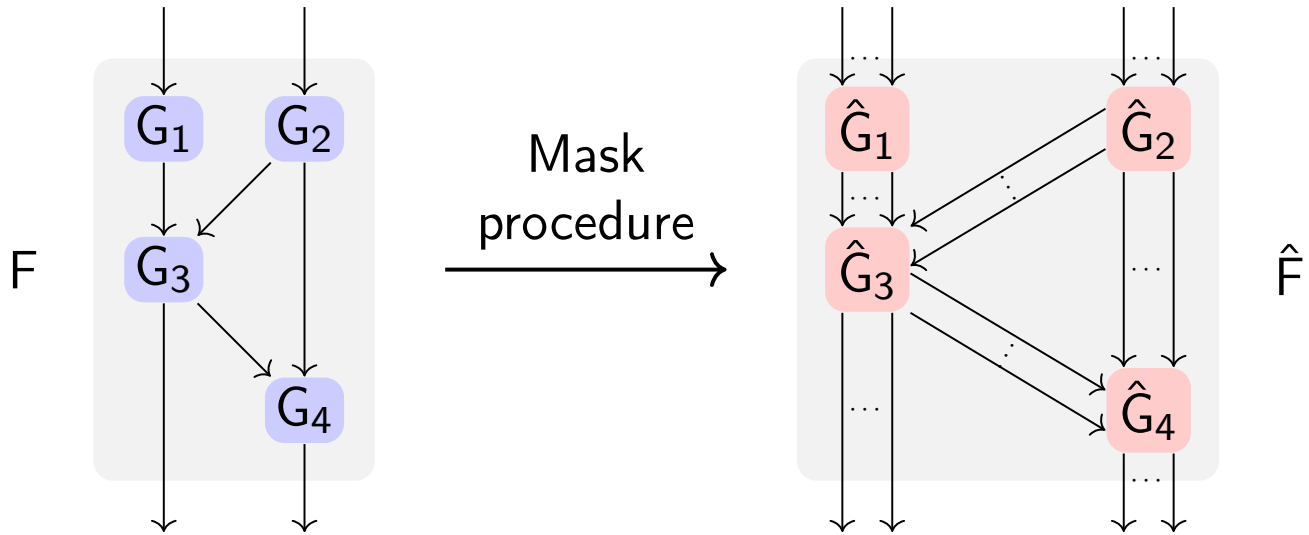
Glitches can reveal information.

Prevent glitch recombinations [GMK16]:

Add registers to stop glitches.



How to Mask a Large Function?



Composition of masked functions [RP10]:

- Divide the function into parts small enough to be easily masked
- Mask each part and compose them
- Composition of secure parts is not always secure

Composability properties:

- Strong Non-Interference (SNI) [Bar+16]
- Probe Isolating Non-Interference (PINI) [CS20]

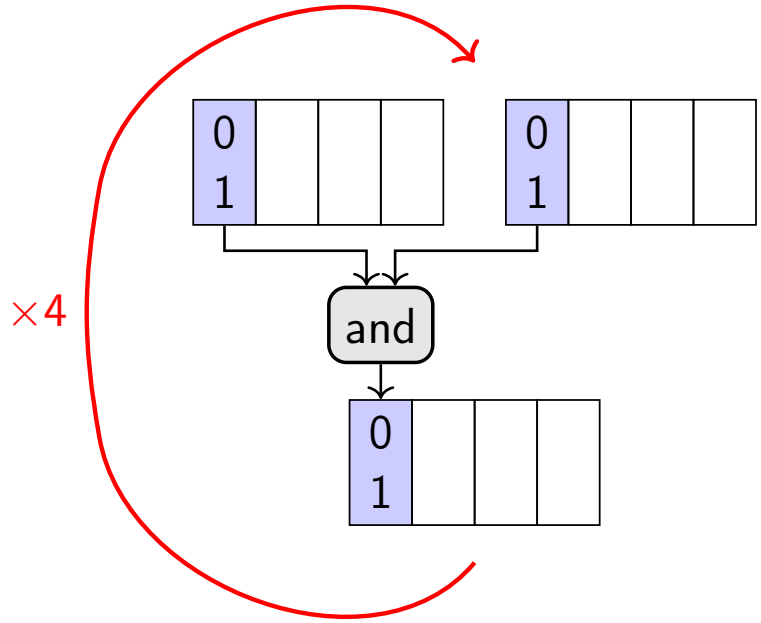
Bit Slicing Implementations

Boolean calculations in processors:

- Calculation on only one bit
- Under utilization of resources

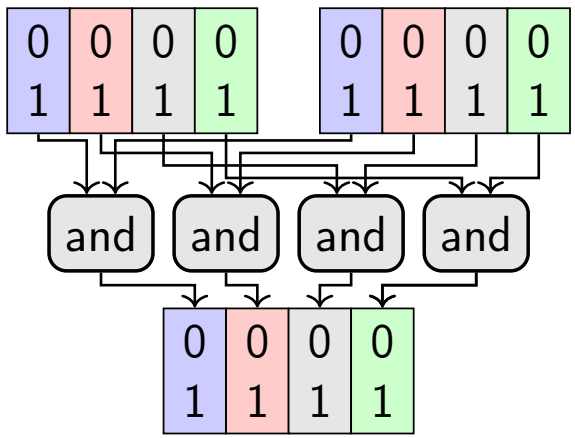
Bit slicing (BS) [Bih97]:

- Parallel calculation on several independent data bits
- High-throughput implementations



USUBA [MD19]:

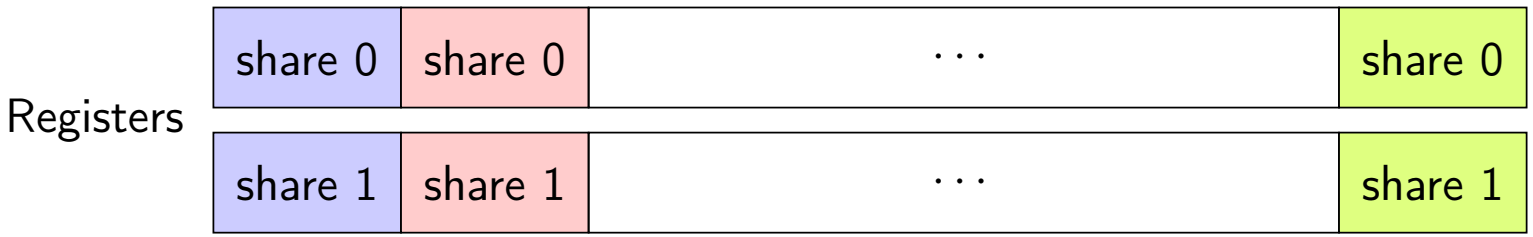
- Language to describe BS implementations
- A compiler allows to synthesize USUBA codes into C codes



How to Mask Bit Slicing Implementations?

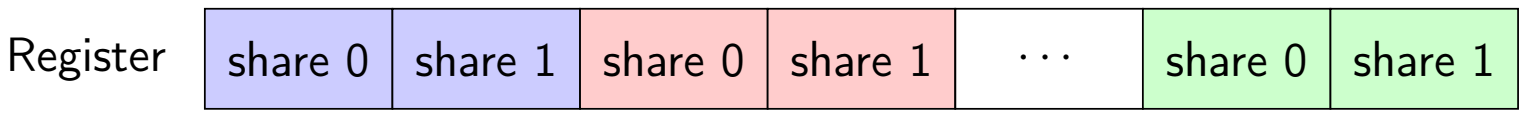
Masking using Tornado [Bel+20]:

- Shares of one bit are placed into different physical registers
- Recombinations of shares can occur by writing a register



Share slicing [JS17]:

- Shares of one bit are placed in the same physical register
- Avoids recombinations of shares



Masked ISE of the State of the Art

- Protection limited to small masking orders
- Not flexible enough to change the masking order at design time and run time

Reference	RISC-V	Masking order	Flexbility at design time	Flexbility at run time
[Gro+16]	✓	$\{1, 2, 3, 4\}$	✓	✗
[DGH19]	✓	1	✗	✗
[Gao+21]	✓	1	✗	✗
SKIVA [Kia+21]	✗	$\{1, 3\}$	✗	✓
SME [MP21]	✓	$\{1, 2, 3\}$	✓	✗

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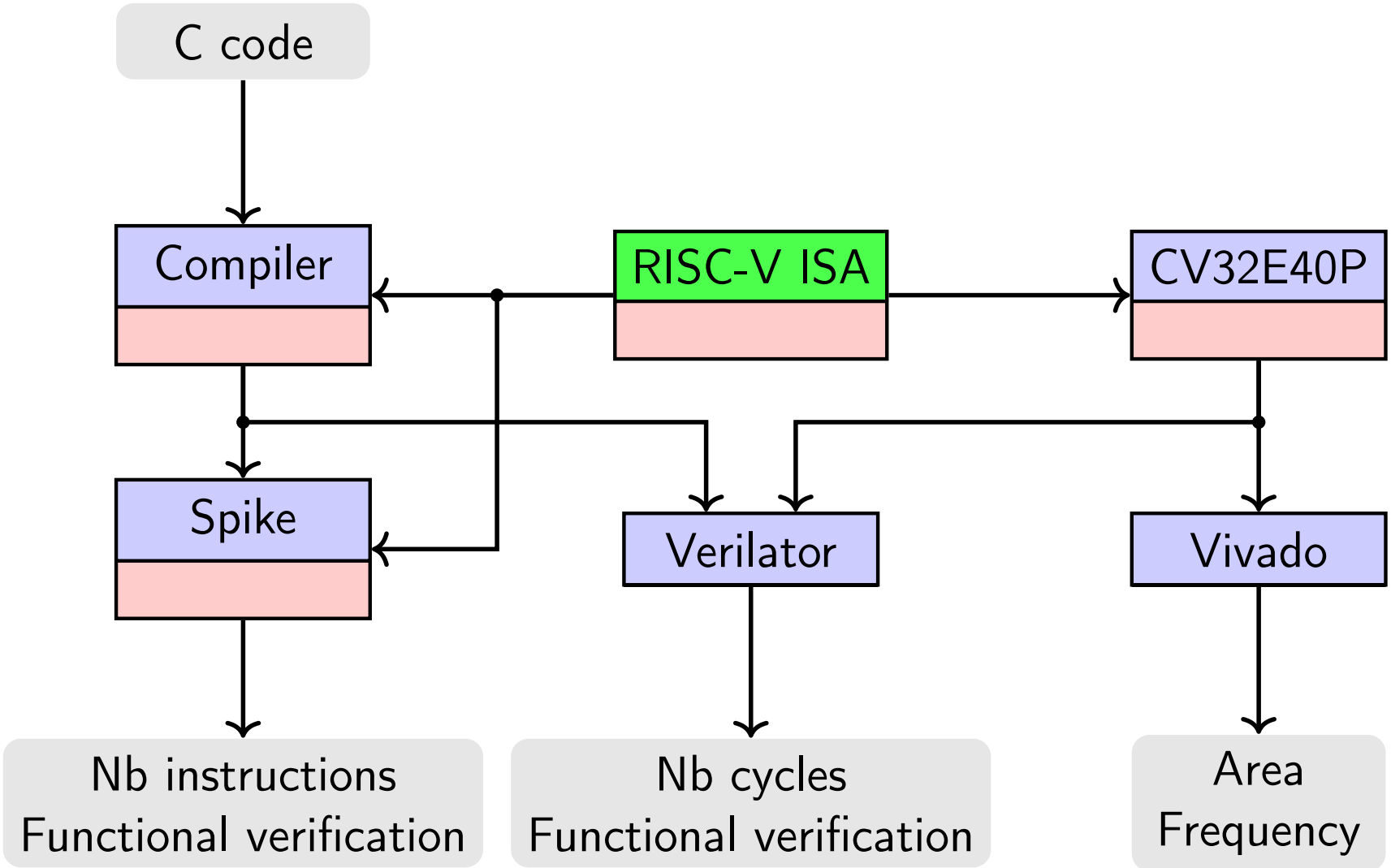
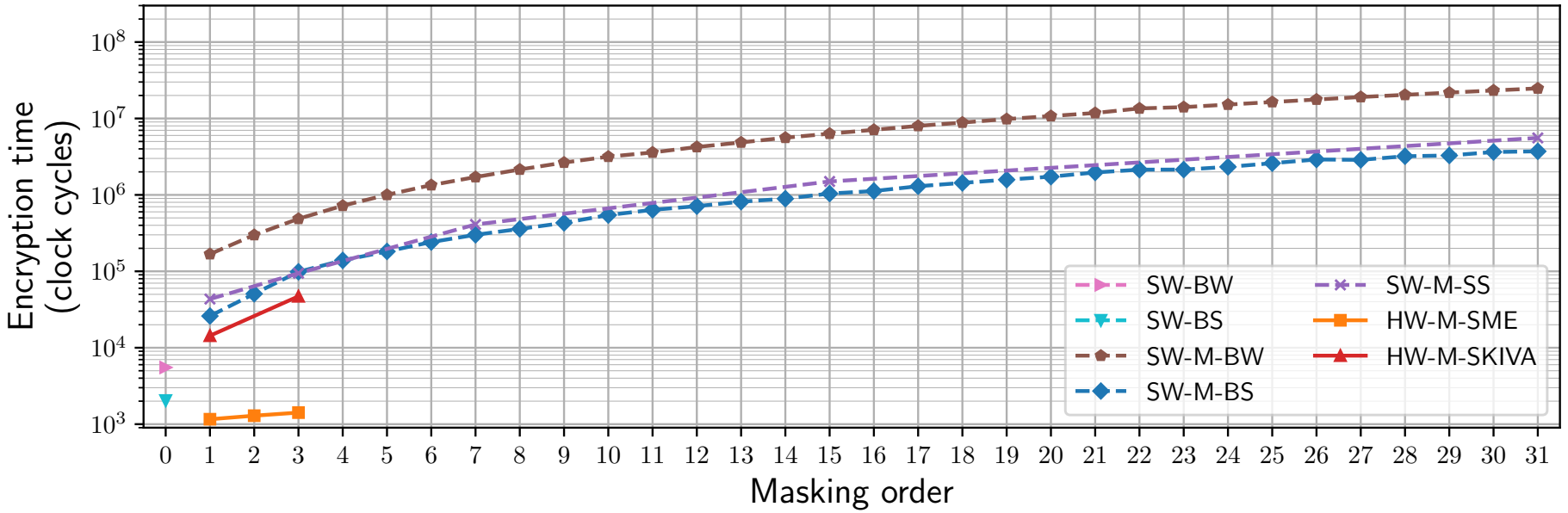
Experimental Environment



Reimplementation of Works from the State of the Art



Encryption times in **log scale** for one AES block:

- SW-BW is unmasked and byte-wise [DR02]
- SW-BS is unmasked and bit-sliced [MD19]
- SW-M-BW is masked and byte-wise [Cor+14]
- SW-M-BS is masked and bit-sliced [Bel+20]
- SW-M-SS is masked and share-slicing [JS17]
- HW-M-SME is masked with SME [MP21]
- HW-M-SKIVA is masked with SKIVA [Kia+21]

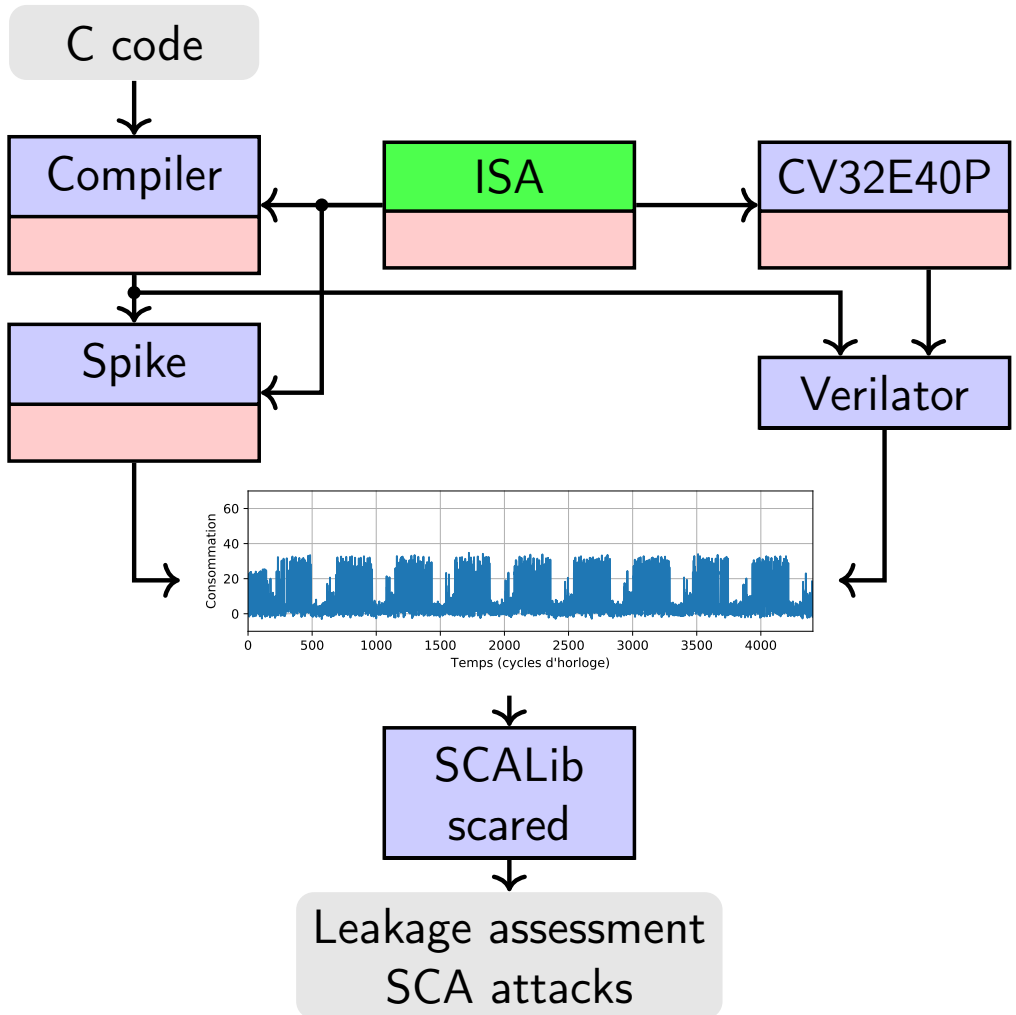
Analysis of Resistance against SCA Attacks

Generation of simulated consumption traces:

- Extracts internal state of the register file
- Simulates consumption with Hamming distance

SCA analysis:

- Leakage assessment of order 1
- SCA attacks of order 1



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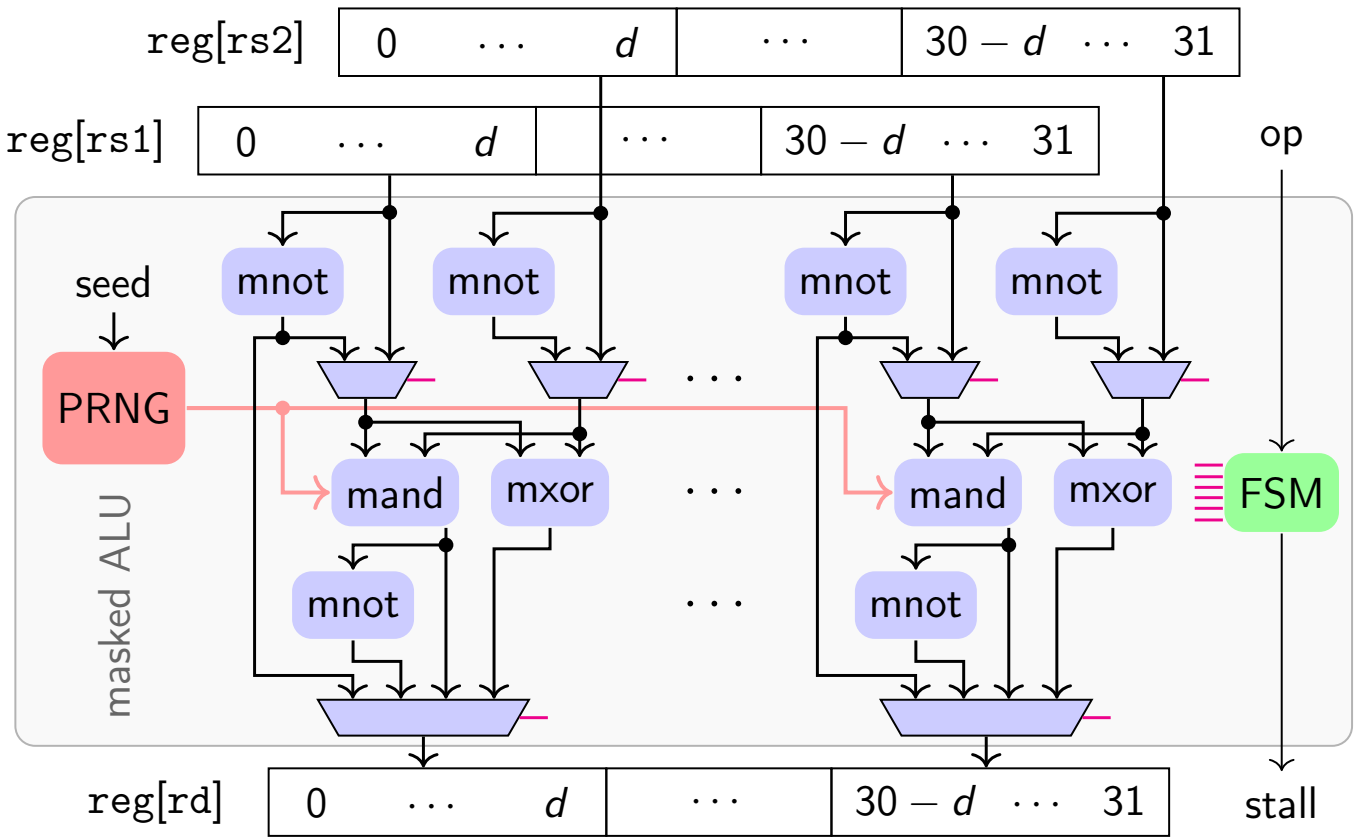
ISE1: Specification of our Extension

- Masked instructions for share slicing implementations
- Masking order $d \in \{1, \cdots, 31\}$ is fixed at synthesis time
- Masked codes are generated using USUBA
- PINI instructions for secure code by direct composition

Instruction	Format	Latency	Random bits
masked AND	`ise1.and rd, rs1, rs2`	2	$32(d-2)$
masked OR	`ise1.or rd, rs1, rs2`	2	$32(d-2)$
masked NOT	`ise1.not rd, rs1, rs2`	1	0
masked XOR	`ise1.xor rd, rs1, rs2`	1	0

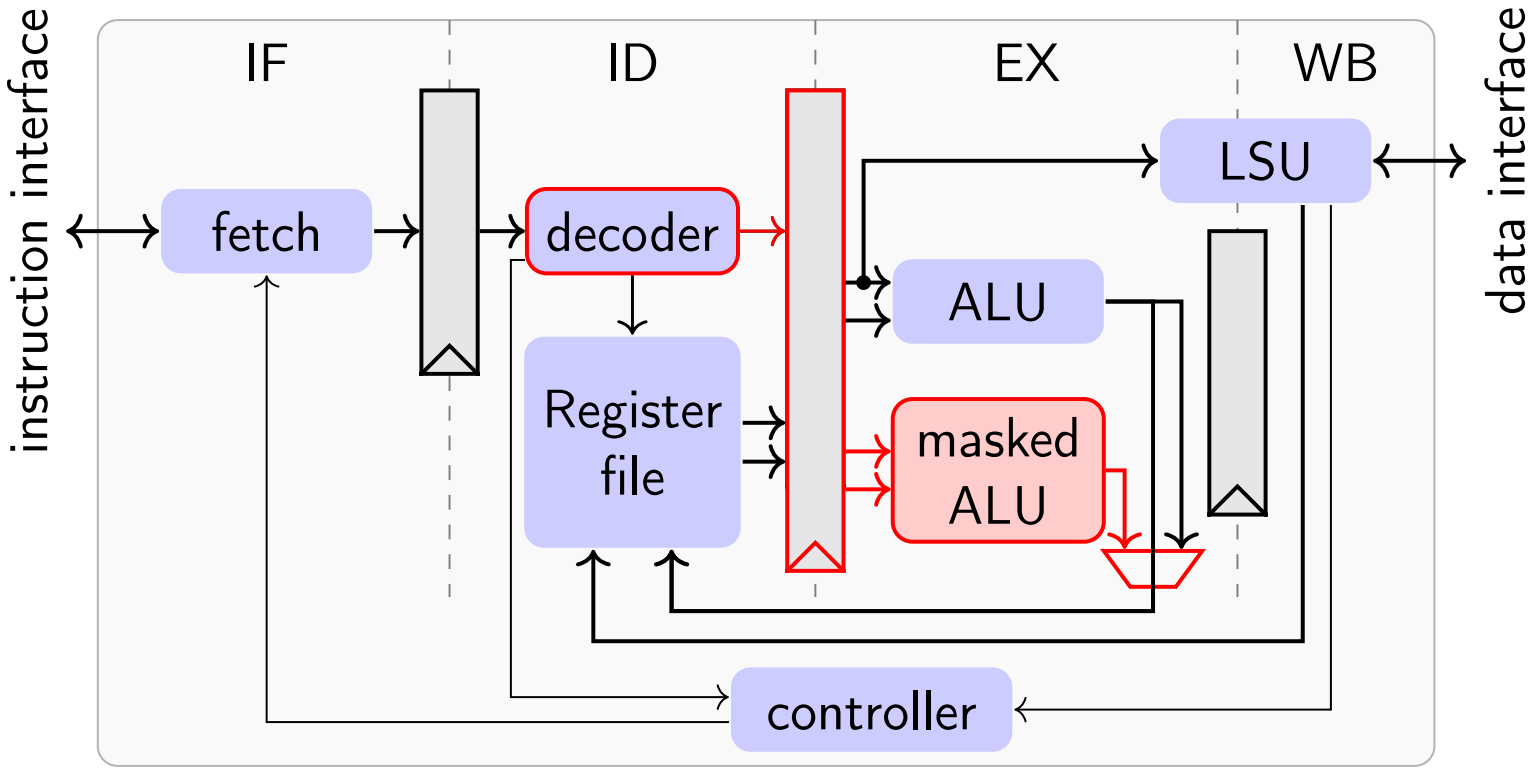
ISE1: Proposed Masked ALU

- Source registers are divided into blocks of $d + 1$ bits
- Masked PINI gates mand, mxor and mnot are applied to each block
- An FSM controls the masked ALU
- A PRNG provides random values

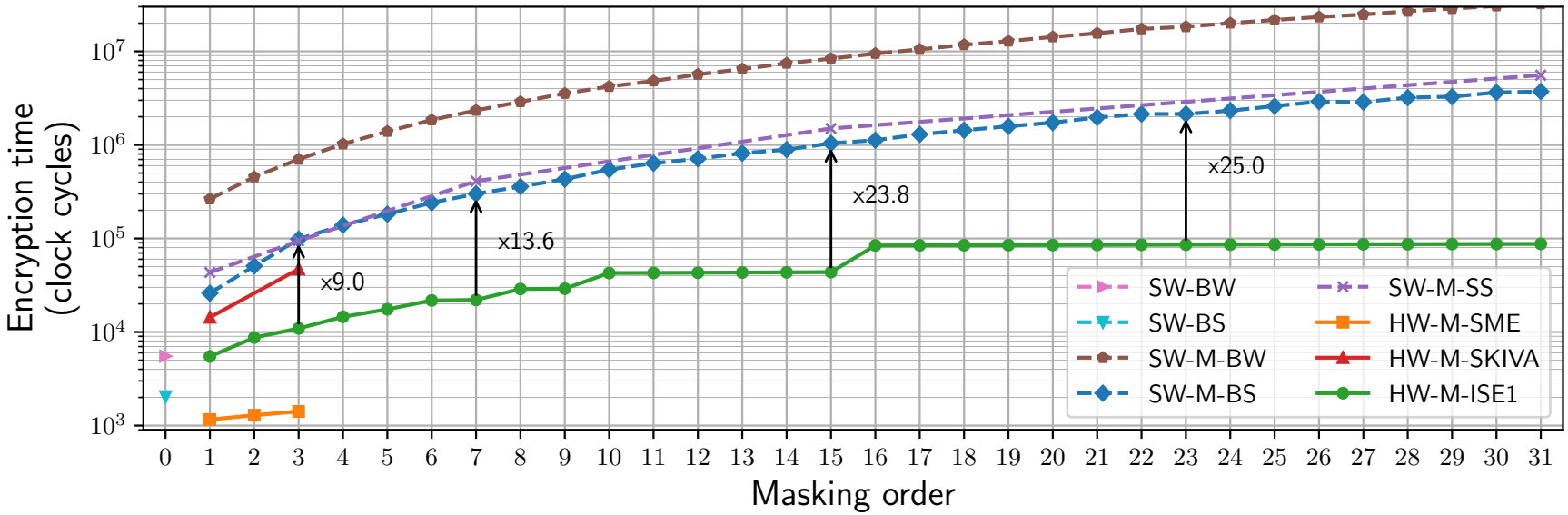


ISE1: Integration into the CV32E40P Core

- CV32E40P is a 32-bit RISC-V processor from the OpenHW Group
- Red parts are added or modified for our masked ISE1



ISE1: Evaluation of Performances



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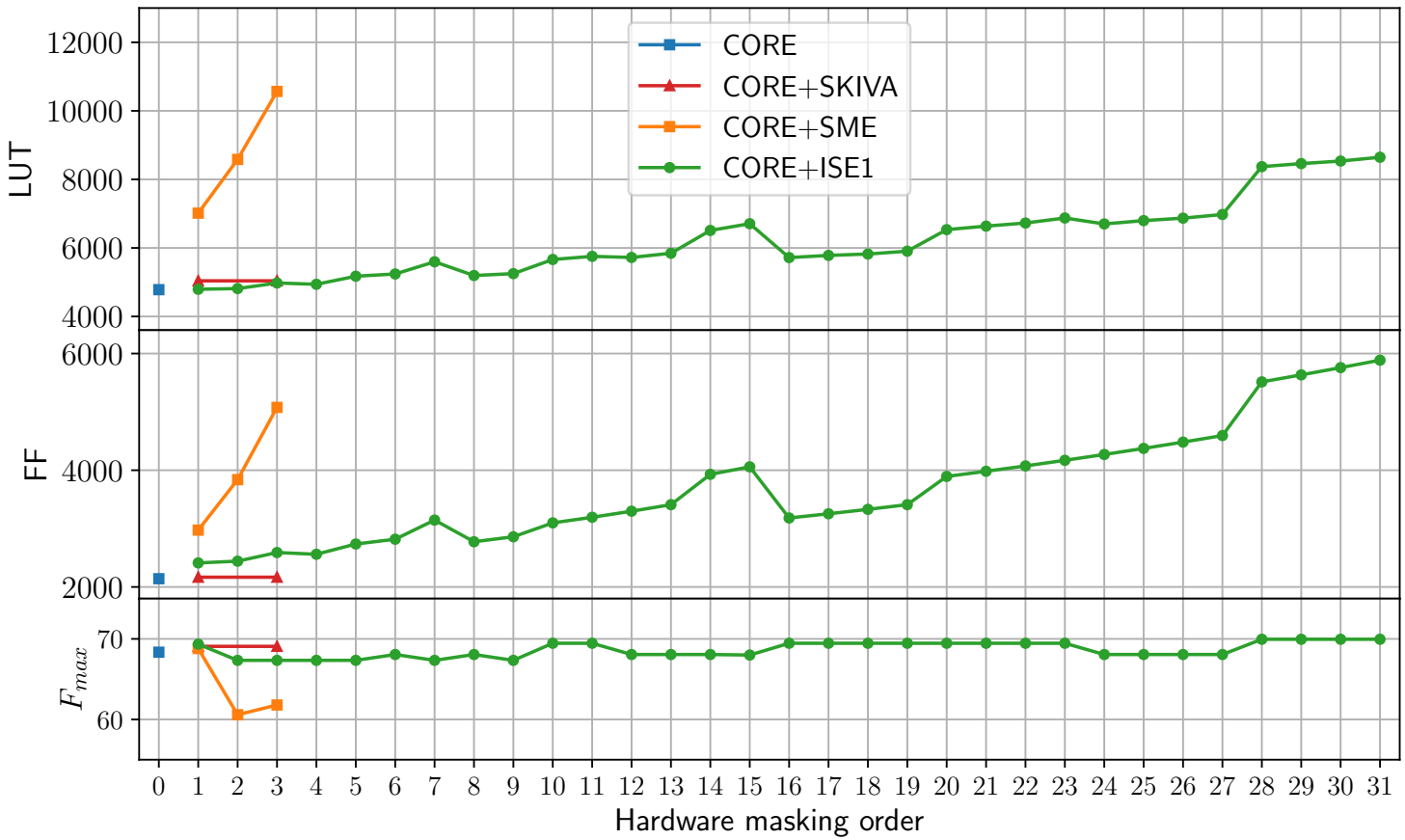
- SW-M-SS is masked and share-slicing [JS17]
- HW-M-SME is masked with SME [MP21]
- HW-M-SKIVA is masked with SKIVA [Kia+21]
- HW-M-ISE1 is masked with our masked ISE1

Implementation on FPGA

Area/frequency results on a Digilent Arty A7 FPGA board of the CV32E40P with Skiva, SME and our masked ISE1.



ISE2: Specification of our Extension

Constraints of ISE1:

- ISE1 encrypts several independent blocks in parallel
- Limits usable encryption modes

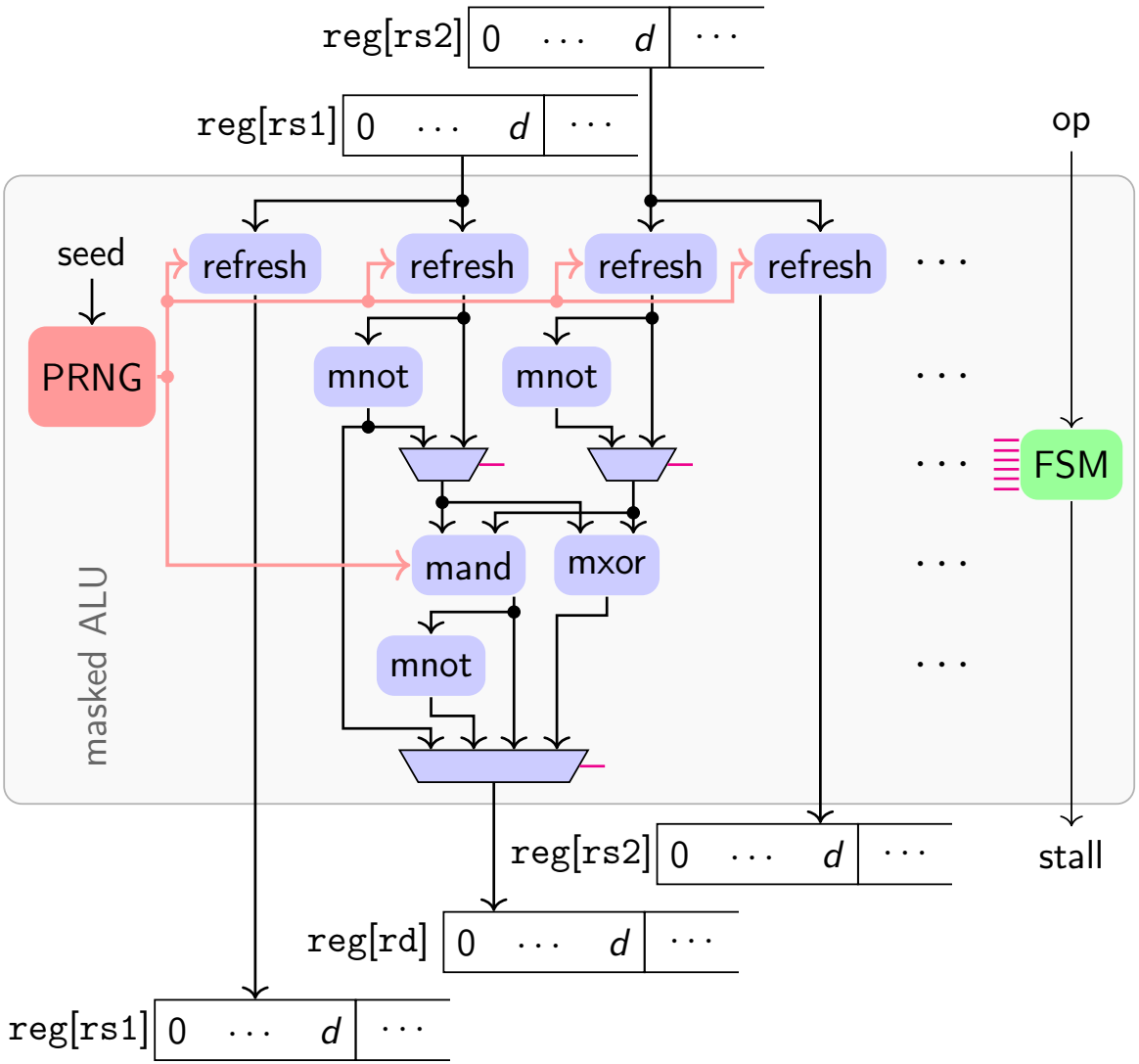
Our masked ISE2:

- Extends ISE1 to reduce the number of independent blocks encrypted in parallel
- Allows to mask one block at a time at orders 1, 3, 7, 15
- Larger and slower than ISE1

Instruction	Format	Latency	Random bits
masked SLL	`ise2.sll rd, rs1, rs2`	1	0
masked SRL	`ise2.srl rd, rs1, rs2`	1	0
masked SLLI	`ise2.slli rd, rs1, imm`	1	0
masked SRLI	`ise2.srli rd, rs1, imm`	1	0

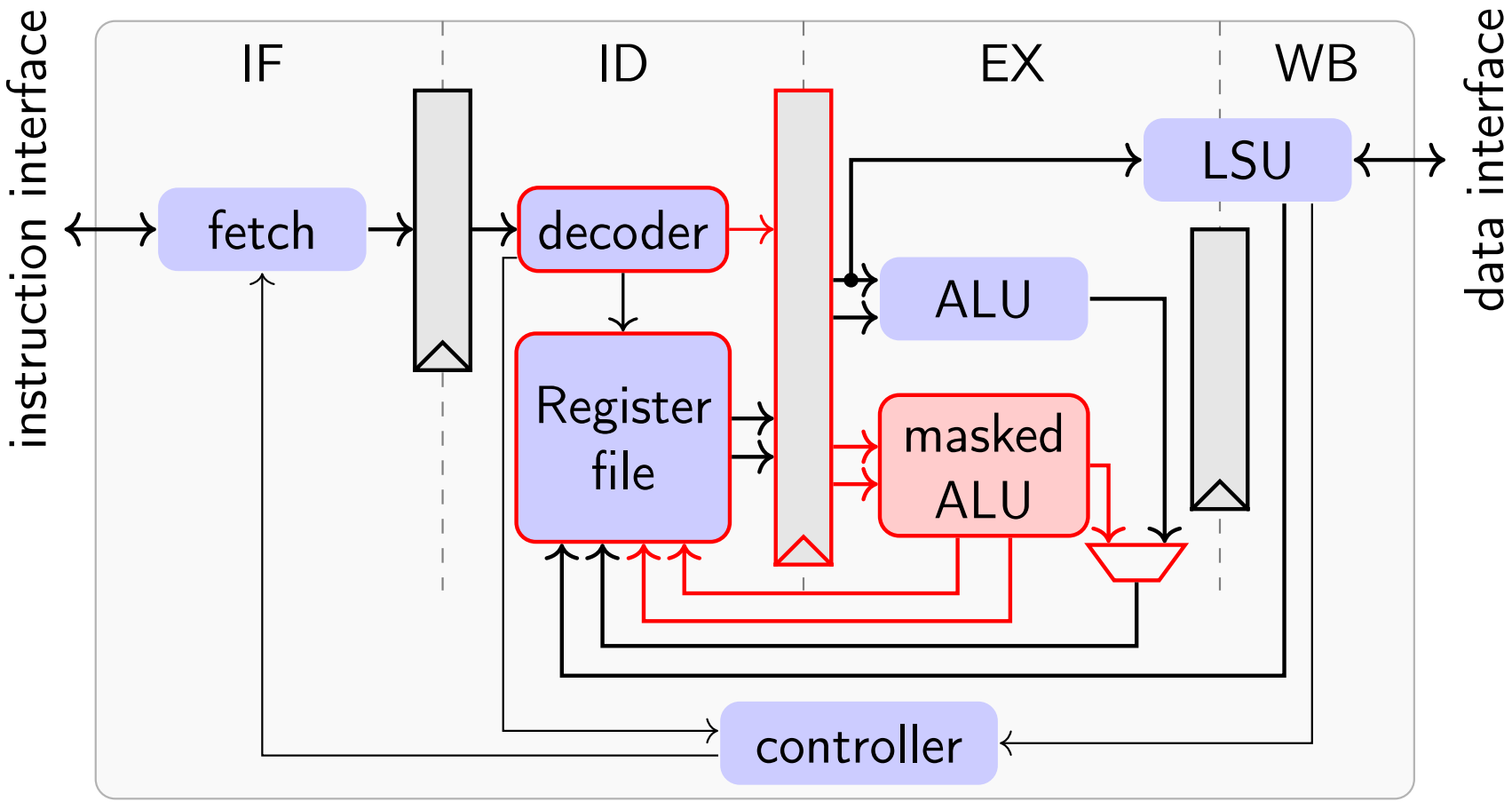
ISE3: Specification of our Extension

- Modifies ISE1 to increase security
- Source registers are refreshed at each use
- Protection against an attacker probing $d/2$ bits per instruction

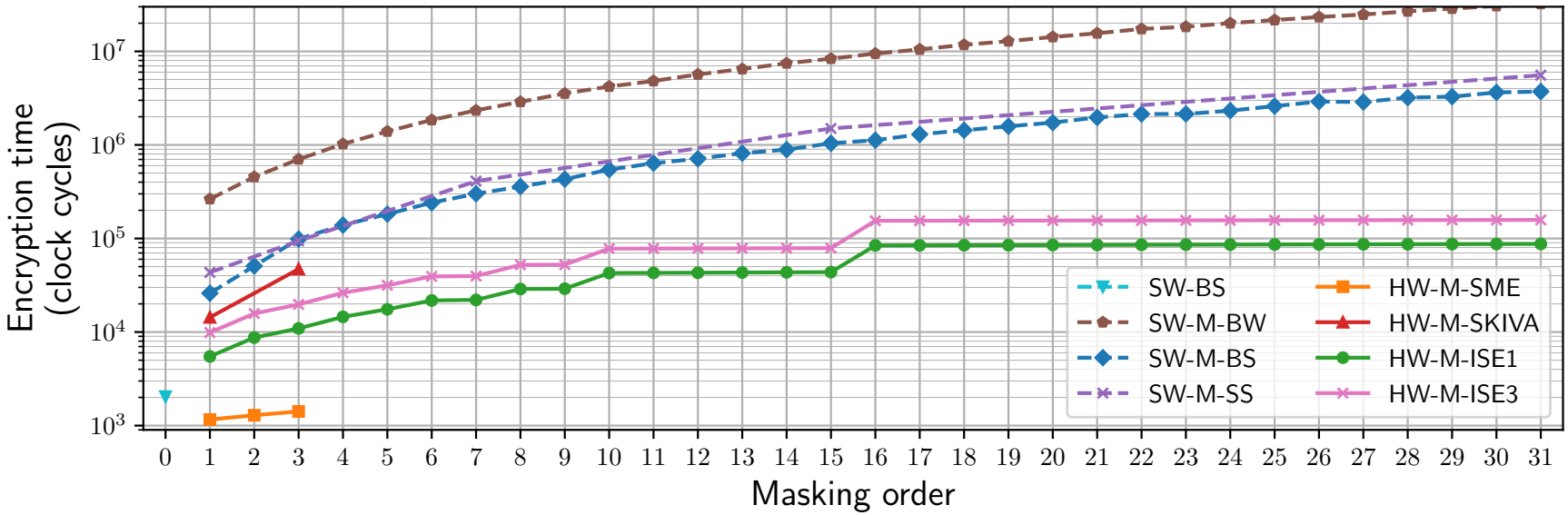


ISE3: Integration into the CV32E40P Core

Red parts are added or modified for our masked ISE3.



ISE3: Evaluation of Performances



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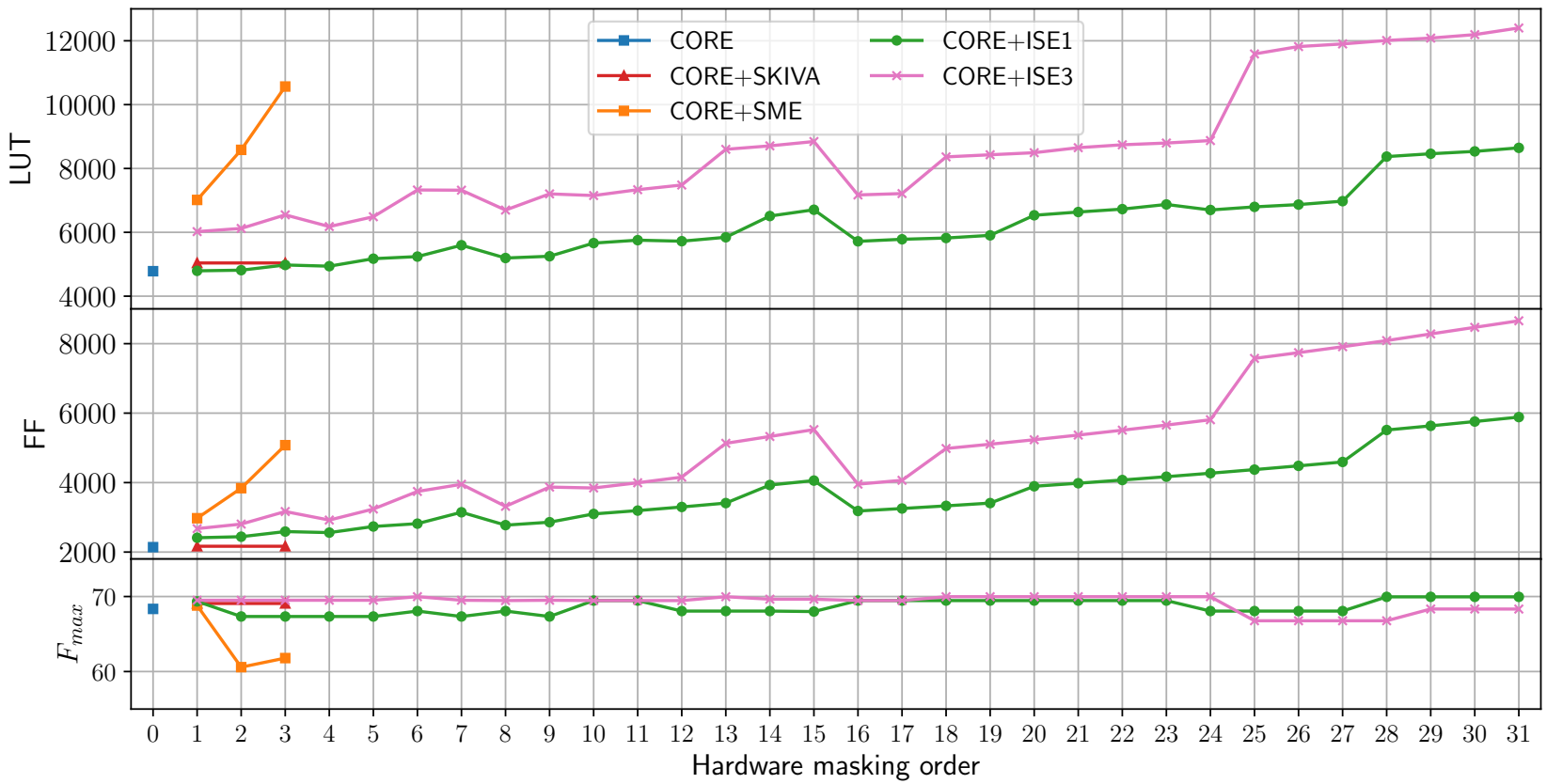
- SW-M-SS is masked and share-slicing [JS17]
- HW-M-SME is masked with SME [MP21]
- HW-M-SKIVA is masked with SKIVA [Kia+21]
- HW-M-ISE1 is masked with our masked ISE1
- HW-M-ISE3 is masked with our masked ISE3

ISE3: Implementation on FPGA

Area/frequency results on a Digilent Arty A7 FPGA board of the CV32E40P with Skiva, SME, our masked ISE1 and our masked ISE3.



HW-SW: Mixed Masking Solution

Hardware masking:

Our masked ISE1 whose order d_{H} is fixed at the synthesis time.

Software masking:

Secure composition over the masked instructions to mask at order:

$$d = (d_{\mathrm{S}} + 1)(d_{\mathrm{H}} + 1) - 1,$$

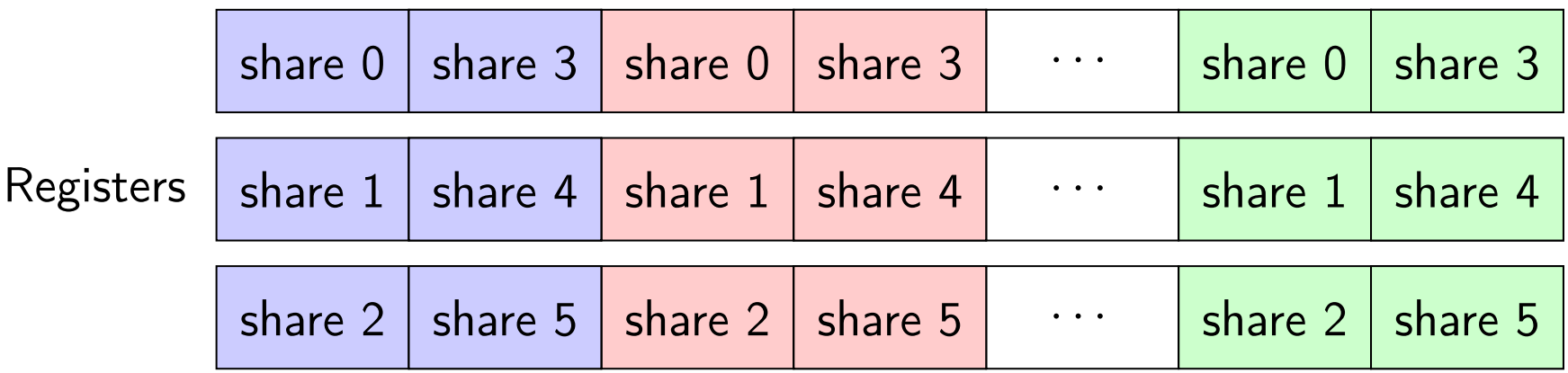
where d_{S} is the software masking order fixed at compilation time.

Flexibility of our solution:

- Allows to adapt the level of security over time
- Allows different cost/performance trade-offs

HW-SW: Our Masked Representation

- Mask at order d_{S} by placing the shares in different registers
- Each share is masked at order d_{H} using share slicing representation
- Total masking order is $d = (d_{\mathrm{S}} + 1)(d_{\mathrm{H}} + 1) - 1$



HW-SW: Our Masking Scheme

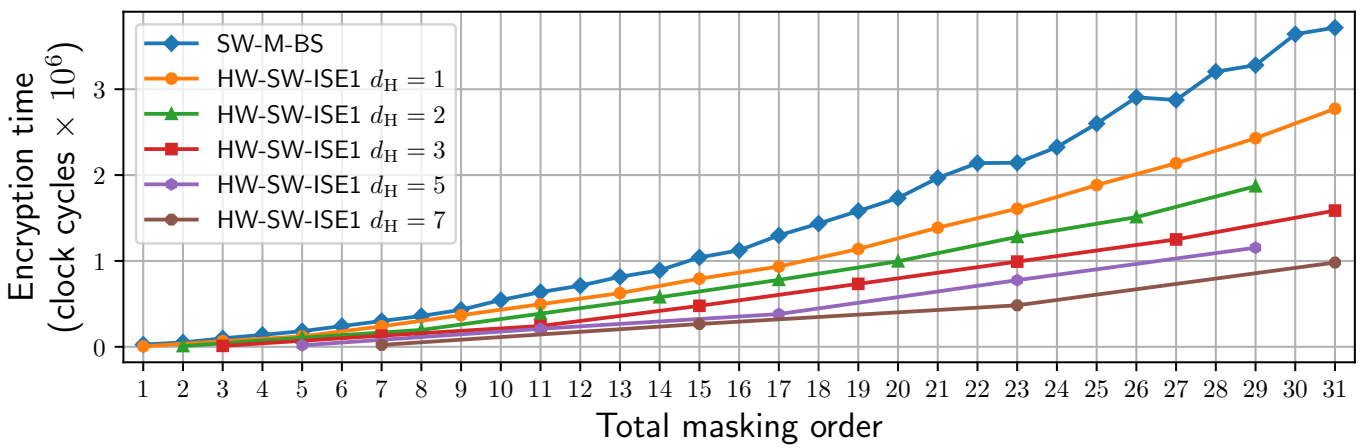
- AND gate masked in software at order d_S and PINI
- Replace elementary operations by instructions of ISE1 masked at order d_H
- Resulting AND gate is PINI and masked at total order:

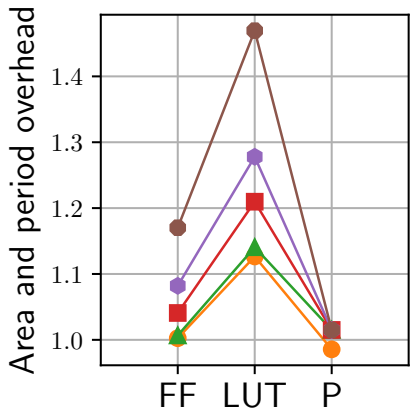
$$d = (d_S + 1)(d_H + 1) - 1$$

Require: $x_i \in \mathrm{GF}(2)^{d_S+1}$ et $y_i \in \mathrm{GF}(2)^{d_S+1}$
Ensure: $z_i \in \mathrm{GF}(2)^{d_S+1}$
  for $i = 0$ à d_S **do**
    $u_{i,i} \leftarrow \mathrm{ise1.and}(x_i, y_i)$
    for $j = i + 1$ à d_S **do**
      $r_{i,j} \xleftarrow{\$} \mathrm{GF}(32)$
      $a_{i,j} \leftarrow \mathrm{ise1.xor}(y_j, r_{i,j})$
      $b_{i,j} \leftarrow \mathrm{ise1.and}(x_i, a_{i,j})$
      $c_{i,j} \leftarrow \mathrm{ise1.not}(x_i)$
      $d_{i,j} \leftarrow \mathrm{ise1.and}(c_{i,j}, r_{i,j})$
      $u_{j,i} \leftarrow \mathrm{ise1.xor}(b_{i,j}, d_{i,j})$
      $a_{j,i} \leftarrow \mathrm{ise1.xor}(y_i, r_{i,j})$
      $b_{j,i} \leftarrow \mathrm{ise1.and}(x_j, a_{j,i})$
      $c_{j,i} \leftarrow \mathrm{ise1.not}(x_j)$
      $d_{j,i} \leftarrow \mathrm{ise1.and}(c_{j,i}, r_{i,j})$
      $u_{j,i} \leftarrow \mathrm{ise1.xor}(b_{j,i}, d_{j,i})$
    end for
  end for
  for $i = 0$ à d_S **do**
    $v_{i,0} \leftarrow u_{i,j}$
    for $j = 1$ à d_S **do**
      $v_{i,j} \leftarrow \mathrm{ise1.xor}(v_{i,j-1}, u_{i,j})$
    end for
    $z_i \leftarrow v_{i,d_S}$
  end for

HW-SW: Implementation Results of our Solution

Encryption times in log scale for one AES block and area/period overheads for our ISE masked at orders $d_{\mathrm{H}} \in \{1, 2, 3, 5, 7\}$ and various total orders.





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Conclusion and Future Prospects

Our contributions:

- ISEs for masking countermeasure
- High order masking
- Good speeds up with a limited silicon cost
- Flexibility at synthesis time and compile time
- Can be used on various cryptosystems

Future works:

- Implement other cryptosystems with our solutions
- Security evaluation using physical attacks
- Masked ISE optimized for post-quantum cryptography

End of Presentation

Thank you for your attention

Do you have any questions?

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