Electrical and morphological characterizations of the hybrid bonding level down to submicron pitches

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Titre : Caractérisation morphologique et électrique du collage hybride jusqu'aux pas submicroniques

Résumé : L'intégration 3D, qui consiste à empiler les puces de différentes technologies et fonctionnalités les unes sur les autres, a émergé au cours des dernières années comme une alternative de la loi de Moore pour poursuivre l'élaboration de puces multifonctions et l'amélioration des performances des circuits intégrés. Le collage hybride, une des différentes techniques de l'intégration 3D, peut répondre aux besoins de miniaturisation avec la possibilité de réduire le pas d'interconnexion au-dessous d'un micromètre, ce qui permettra la conception des dispositifs plus performants notamment pour les capteurs d'image. Les effets d'une telle miniaturisation sur les propriétés thermomécaniques et électriques ainsi que sur la robustesse des interconnexions en collage hybride sont, cependant, inconnues.

L'objectif de cette thèse est d'étudier, dans une intégration par collage hybride, les défis de la réduction du pas d'interconnexion jusqu'en dessous du micromètre. La méthodologie a consisté d'étudier, avec la réduction du pas, le mécanisme de fermeture de l'interface de collage, la fiabilité des interconnexions au niveau collage hybride ainsi que leurs performances électriques. En utilisant la technique de Microdiffraction de Laue à l'ESRF, une orientation cristalline favorisant la fermeture de l'interface à l'échelle submicronique a été mise en évidence. La résistivité de contact extraite par une nouvelle méthode d'estimation a permis de définir les spécifications de fabrication pour obtenir une reconstruction parfaite de l'interface Cu-Cu avec une résistivité de contact proche de celle de joint des grains de Cu. Malgré la modification du mode de défaillance en électromigration avec une cavité tueuse au niveau des plots de collage pour les pas inférieurs à 3.5 μm, les performances électriques à des conditions normales d'utilisation ne sont pas affectées. A l'aide d'une nouvelle méthodologie de test, nous avons montré que le mode de dégradation en claquage de diélectrique (TDDB) au niveau de collage hybride est atypique par rapport au BEoL standard. Des analyses fines ont permis de lier ce comportement à une couche de Cu_2O, présente à l'interface Cu/SiO_2, qui agit comme une barrière et qui rend l'intégration Cu/SiO_2 immune à la diffusion de cuivre. Cette compréhension fine du mécanisme de collage et de la robustesse de l'interface a permis de démontrer que le collage hybride est possible au moins jusqu'au pas de 0.67 μm et de proposer de nouvelles architectures pour améliorer la performance électrique.

Mots-clés : Intégration 3D, collage hybride, pas d'interconnexion submicronique, fiabilité

Title: Electrical and morphological characterizations of the hybrid bonding level down to submicron pitches

Abstract: The 3D integration technology has emerged in the last decade as a key process to combine multi-functional and technological integrated circuit devices to produce a single chip with small form factor and enhanced electrical performances. The hybrid bonding technology, one of the different 3D stacking options, is adapted for advanced device miniaturization with the possibility of reducing the hybrid bonding pitch below one micrometer. This would allow the design of more efficient devices especially for image sensors. However, the impact of such aggressive interconnection pitch scaling on the bonding mechanism, the electrical performance and the reliability of the hybrid bonding level remains to be studied.

The goal of this PhD thesis is to study, for the Cu/SiO_2 hybrid bonding integration, the challenges of reducing the hybrid bonding pitch down to sub-micron. To target this, we studied a possible change in the Cu interface closure mechanism with the reduction of the Cu pad width. Using the Laue-microdiffraction technique at the ESRF, a specific crystalline orientation favorizing the closure of Cu-Cu interface at the sub-micron pitch level was put in evidence. From an electrical point of view, new methods were developed to precisely extract the Cu-Cu interface resistivity allowing the define the fabrication specifications to obtain an interface reconstruction close to Cu grain boundary one. Despite the modification of the electromigration degradation mode with a killer defect at the hybrid bonding level for Cu pads below 3.5 μm in width, the electrical performances at use conditions are not affected. Moreover, using a new test methodology, we have put in evidence for the first time at the hybrid bonding level a modified degradation mode under Time Dependent Dielectric Breakdown (TDDB) as compared to standard BEoL behaviour. Deep analyses on the atomic and ionic diffusion mechanisms allowed to link this modified behaviour to the presence of a thin Cu_2O layer at the Cu/SiO_2 interface, which behaves as a barrier against Cu diffusion in SiO_2. This profound understanding of the bonding mechanism and interface robustness and reliability allowed us to demonstrate that hybrid bonding is possible at least down to 0.67 μm and to propose new architectures allowing enhanced electrical performances with pitch reduction.

Keywords: 3D integration, hybrid bonding, submicron pitch, reliability

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Acronyms

AFM Atomic Force Microscopy
BEoL Back End of Line
BSI Back Side Illuminated
BTS Bias Temperature Stress
CBKR Cross Bridge Kelvin Resistor
CIS CMOS Image Sensor
CKR Cross Kelvin Resistor
CMOS Complementary Metal Oxide Semiconductor
CMP Chemical Mechanical Polishing
CTE Coefficient of Thermal Expansion
C-V Capacitance-Voltage
CVS Constant Voltage Stress
CZM Cohesive Zone Model
DC Daisy Chain
DoCE Design of Computer Experiments
D2W Die-to-Wafer
EBSD Electron Backscatter Diffraction
ECD Electrochemical Deposition
EELS Electron Energy Loss Spectroscopy
EM Electromigration
FC-CCD Face-Centered Central Composite Design
FEM Finite Element Modeling
FEoL Front End of Line
HB Hybrid Bonding
HBM Hybrid Bonding Metal
HBV Hybrid Bonding Via
HCM Hard Contact Model
HTS High Temperature Storage
IC Integrated Circuit
IFP Inverse Pole Figure
ILD Inter-Layer Dielectric
IMD Inter-Metal Dielectric
IO Input/Output
ISP Image Signal Processor
ITRS International Roadmap for Devices and Systems
KoZ Keep-out Zone
LHS Latin Hypercube Sampling
LPD-ICPMS Liquid Phase Decomposition - Inductively Coupled Plasma Mass Spectroscopy
LRVS Linear Ramped Voltage Sweep
ML Metal Line
MTTF Mean Time-to-Failure
OBIRCH Optical Beam Induced Resistance Change
PCB Printed Circuit Board
PVD Physical Vapor Deposition technique
RC Resistance-Capacitance
SAM Scanning Acoustic Microscopy
SEM Scanning Electron Microscopy
SFT Strain Free Temperature

SiP System-in-Package
SiV Stress induced Voiding
TC Thermal Cycling
TDDB Time Dependent Dielectric Breakdown
TEM Transmission Electron Microscopy
TSV Through Silicon Via
TTF Time-to-Failure
TVS Triangular Voltage Sweep
TXRF Total X-Ray Fluorescence
W2W Wafer-to-Wafer
2FI Two-Factor Interaction

General Introduction

I The need of high performance integrated circuits

An integrated circuit (IC) is a set of electronic devices that are processed and electrically connected onto a semiconductor material named wafer. An IC is built with the primary objective of embedding as many transistors as possible on a single semiconductor chip. According to their design assembly, integrated circuits have undergone several generations of advancements and developments. The latest generation is called the ultra large scale integration embedding transistors higher than one million [1]. Nowadays, rather than the transistor count, the technology node is used to designate the IC generation. The technology node (also designated as process node and process technology) refers to the set of fabrication processes and design rules to reach a given level of miniaturization.

In 1965, Gordon E. Moore, the co-founder of Intel, made his famous observation that the density of components at a minimum cost roughly double each year [2]. A decade later, in 1975, Moore adjusted his vision to a double each two years [3]. This became known as the Moore's Law. As of 2022, the 3 nm technology node (corresponding to ICs integrating hundreds of billions of transistors) entered volume production but with a production yield below 80 % [4] [5]. However, only a handful of manufacturers are now able to follow this path. Many other manufacturers continue to work on producing earlier nodes, mainly above 28 nm.

Many challenges arise from this downscaling of the technology node, one of which is the exploding manufacturing cost. In addition, for technology nodes in the range of ten manometers, quantum effects are no longer negligible. This leads to increased power consumption and heat generation due to leakage current in the transistors [6]. This effect eventually led to a decrease in the production yield.

With the advancement of technology nodes, higher density of interconnection network is needed. This leads to an increase in the resistor-capacitance (RC) delay coming from the interconnects. The signal delay problematic is an active topic of interest in the microelectronics domain [7] [8] [9] [10]. An example of the calculated gate and interconnect delay with the advancement of the technology node (down to 100 nm) is shown in figure 1 [8]. As technology scales down, gate delay is reduced; however, interconnect delay increases and dominates the signal propagation delay. Thus, resistor-capacitor effect is a major limiting factor in interconnect performance as feature size scales down due to the effect of reducing the scaling on the interconnect resistance and capacitance. As shown in figure 1, many approaches have been done to reduce the RC interconnect delay by

replacing the aluminum with the metal copper having lower electrical resistivity and the use of low-k dielectrics as compared to SiO_2 with k=3.9 [11][12][13]. Even though this approach led to an improved interconnect delay, this is somehow not sufficient. In fact, a study in 2017 reported that for the 22 nm node, the interconnect delay counts for more than 80 % of the total signal delay [10].

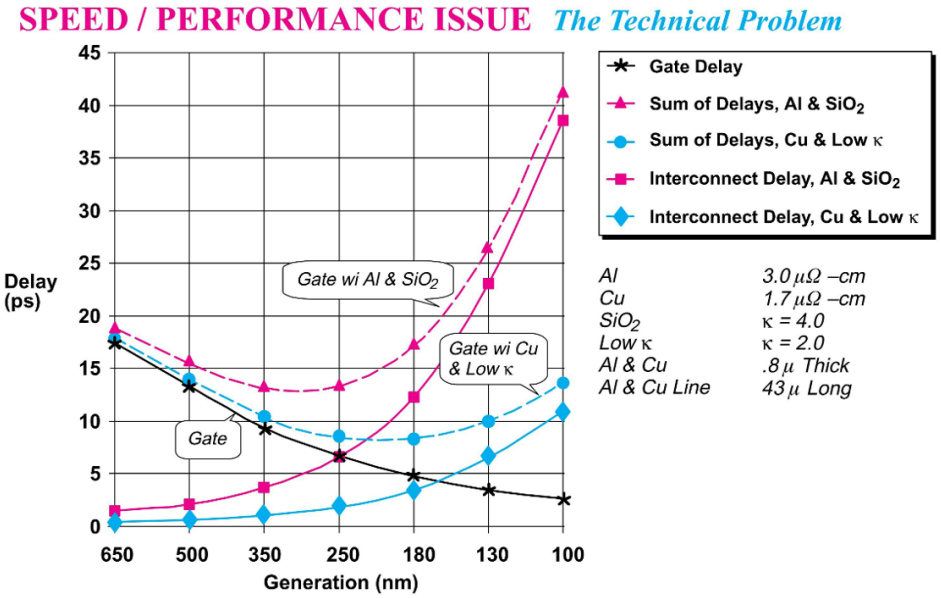

Figure 1: Calculated gate and interconnect delays with the advancement of the technology nodes down to 100 nm [7].

To keep up with the pace of transistor miniaturization and achieve better electrical performance, the more than Moore trend was adapted by many manufacturers as an alternative to the Moore's path. As defined by the international roadmap for devices and systems (ITRS), more than Moore ¨refers to the incorporation into devices of functionalities that do not necessarily scale according to Moore's Law but provide additional value in different ways¨ [14]. More than Moore improves the IC performance through heterogeneous integration, which is the functional combination of dissimilar (electrical, optical, thermal, magnetic, mechanical) components with its corresponding technology node onto a silicon substrate, encapsulated within a single package. Standard assembly techniques for heterogeneous integration achievement are wire-bonding or flip-chip. These approaches are referred as the system-in-package (SiP) [15]. For these approaches, the electrical connections between the different chips are indirect and achievable only via the package substrate. New integration strategies have been developed to achieve heterogeneous integration with reduced form factor and direct interconnection between the chips allowing increased performance. Such approaches are referred as 3D integration.

II 3D stacked integrated circuits: evolution to hybrid bonding

To illustrate the 3D integration approach and technologies, we will take the example of the complementary metal oxide semiconductor (CMOS) image sensor (CIS), which is the

one of the main applications for these technologies. The CIS can be decomposed into two main chips: the array of pixels and the image signal processor (ISP) or the logic chip. 3D integration allows heterogeneous integration (more than Moore trend) as well as an increase in the transistor density through 3D chip stacking (more Moore trend). A schematic illustration of the 3D stacking approach is shown exemplary in figure 2 (b) and (c). As compared to the 2D integration approach that involves multiple horizontal connections of multiple chip functions (figure 2 (a)), 3D integration allows reduced form factor.

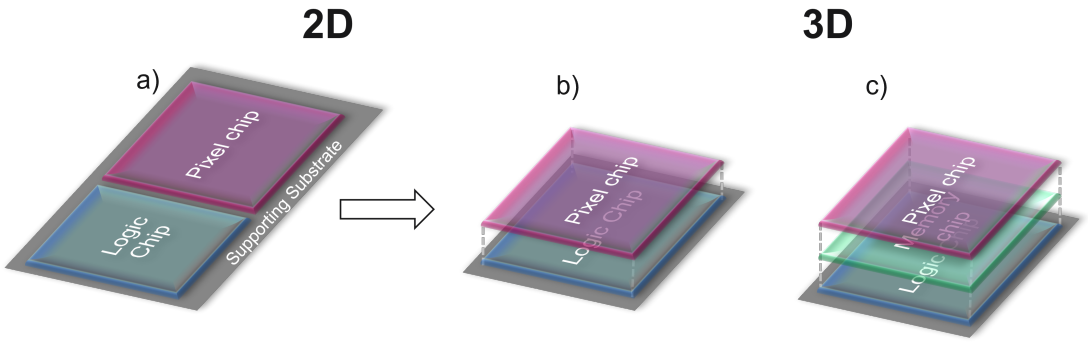

Figure 2: a) 2D planar approach. 3D integration for heterogeneous systems applied to image sensor case with b) two chips stacking and c) three chips staking.

The 3D integration approach offers many advantages. For the CIS case, 3D stacking of the pixel and ISP chips can reduce the chip surface by 30 % while maintaining the resolution and the same size of the pixels [16].

Another advantage of 3D stacking is technology optimization. The ISP and pixel chips are usually processed with different technology nodes, each has its own characteristics. By using 3D integration, these two chips can be fabricated independently and then stacked vertically.

Most importantly, 3D integration allows a reduction of the RC interconnect signal delay and therefore an enhanced performance. With 3D integration, the chips are connected vertically, in contrary to the 2D approach where the different chips are connected with printed circuit board (PCB) or an interposer. The lengths of the interconnects are smaller leading to a reduction of the electrical resistance. The signal delay induced by the interconnect is thus lowered. For the same reason, the power consumption is lower.

Beside the advantages, 3D stacking opened the door for new architectures in image sensors such as the one illustrated in figure 2 (c) with a three chips stacking design. A memory can be inserted in between the pixel and the logic chips that allows high speed readout [17].

The 3D stacking technologies have evolved during the last ten years with the main objectives of achieving higher performance and increased interconnect stacking density. One approach for 3D stacking is the through silicon via (TSV) technology. A schematic

illustration of a 3D stacked image sensor using the TSV technology is shown in figure 3 (b). The TSV is compatible with the back side illuminated (BSI) image sensor case (see figure 3 (a)). In the 3D approach with TSV (figure 3 (b)), the carrier wafer for the BSI case is replaced by the ISP chip, and the two wafers are vertically connected by SiO_2/SiO_2 direct bonding. The two chips are then connected using TSVs. The first 3D stacked CIS using TSVs was introduced by Sony in 2013 [16].

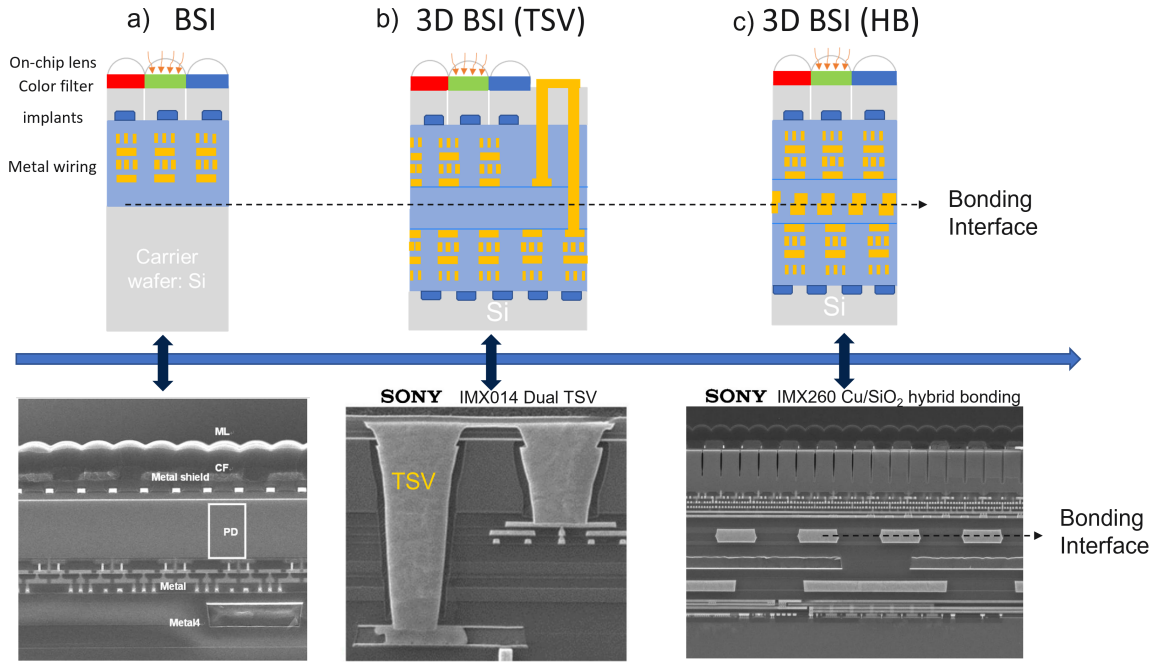

Figure 3: Schematic (top) and cross sections (bottom) illustrations of the evolution of BSI technologies with a) BSI image sensor [18] b) 3D stacked CIS using TSV [19] and b) 3D stacked CIS using the hybrid bonding technology [19].

One of the recent 3D stacking integrations is hybrid bonding, which is one of the most scalable technologies. This technology is based on replacing the homogeneous dielectric/dielectric bonding interface between the two tiers, for the case of a 3D stacked CIS with TSVs, with a metal/dielectric hybrid interface without TSV. A schematic illustration of a 3D stacked image sensor using the hybrid bonding technology is shown in figure 3 (c). As compared to 3D stacking with TSVs, the hybrid bonding technique does not need exclusion regions (referred as keep-out zone - KOZ - to prevent active devices from being impacted by TSV-induced stress) since the connection between the two chips is achieved through the interface only. Moreover, the metal pads at the hybrid bonding interface are highly shrinkable, enabling to achieve higher interconnection density as compared to TSVs or other 3D stacking technologies (solder bumps, micro bumps). The first 3D stacked image sensor product using the hybrid bonding technology was demonstrated by Sony in 2016 [20].

Since the first studies on the hybrid bonding technology, many integrations were developed depending on the design of metal pads at the interface as well the dielectric properties. The details on the different architectures will be given in chapter 1. It must

be noted that the reliability and electrical performance depend on each type of hybrid bonding integration. The one of interest for my PhD is based on wafer-to-wafer (W2W) Cu/SiO_2 hybrid bonding with a via+pad (referred as hybrid bonding via - HBV + hybrid bonding metal - HBM in our study) design at the bonding level [21]. Hybrid bonding pitch reduction, down to sub-micron, is key for many applications such as image sensors and memory. However, many challenges arise that should be understood and targeted to succeed with sub-micron hybrid bonding pitch achievement. The main challenges are presented in the following section, as deduced with regard to the specific Cu/SiO_2 hybrid bonding integration used in my PhD.

III Main challenges with hybrid bonding pitch reduction

This section aims to discuss the different challenges that are expected to face successful hybrid bonding with pitch reduction especially in the sub-micron region for the specific process of the Cu/SiO_2 hybrid bonding configuration of interest in my PhD. It will also serve as a basis for the different studies that are to be presented in this manuscript. More details will be given for each specific subject at the beginning of its corresponding chapter.

III.1 Achieving hybrid bonding with high electric yield

With the reduction of the hybrid bonding pitch, especially in the sub-micron pitch region, a major concern is the achievement of a high electric yield. Several parameters could impact the electric yield such as the lack of Cu-Cu interface closure as well as any impact of W2W overlay.

Establishing Cu-Cu connection at interface

The establishment of Cu-Cu interface connection and reconstruction is key with sub-micron pitch reduction. Before bonding, a chemical mechanical polishing (CMP) step is needed to prepare the two wafers to be bonded. During this step, a Cu in recess to SiO_2 can take place that is referred as Cu dishing (see figure 4 (a)). After bonding at room temperature, an annealing step is needed to establish possible connections at the interface (see figure 4 (b)). The achievement of Cu-Cu connections at interface is mainly impacted by two main parameters that are the thermomechanical behaviour of Cu pads and the contact resistivity that qualifies the electrical connections at the interface.

For the thermomechanical behaviour, most of the studies on the Cu-Cu interface closure mechanism for the hybrid bonding technology are done using numerical simulations methods while modeling single Cu pad at the interface embedded in a dielectric material. Two main models are reported in the literature to describe the Cu-Cu bonding mechanism as following:

1. The first is Cu-Cu interface closure driven by the thermomechanical behaviour of Cu during the annealing step using a hard contact model (HCM) approach. This

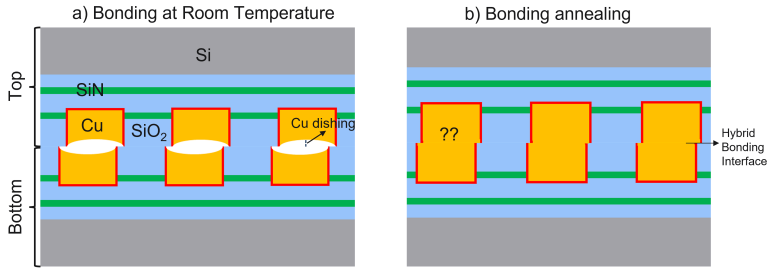

Figure 4: Schematic illustrations of the hybrid bonding process with a) after CMP and bonding at room temperature and b) after bonding annealing.

model is based on thermal strain to close the initial gap after bonding by the thermal expansion and elasto-plastic behaviour of Cu with or without an additional role of creep [22] [23] [24].

2. The second is based on cohesive zone model (CZM) while simulating Cu-Cu interface closure mechanism. This model proposes that the cohesive interactions combined with the thermal expansion of Cu are the main mechanics of Cu bonding with an initial dishing.

Whatever the approach used, it is clear that the Cu dishing specifications for interface closure are more restricted with the reduction of the Cu pad width. This is driven by the lower thermal strain with pad width reduction during the annealing step [25]. The Cu mechanical properties usually considered in the numerical simulations are the bulk ones that might be adequate for micrometric Cu pads. However, it is now well established that materials at small scales, especially with grain size between 100-1000 nm, present much different properties (thermomechanical, electrical...) than the bulk one [26] [27] [28]. Hence, the main challenge is the correct understanding of the Cu thermomechanical properties with the reduction of the Cu pad size below 1 μm, which is key whatever the approach used for Cu-Cu interface closure. In the present thesis, the Cu thermomechanical properties in the sub-micron region will be studied. This will give access to the correct dishing specifications to be set with the reduction of the hybrid bonding pitch.

Understanding the thermomechanical behaviour of Cu might not be sufficient alone to guarantee Cu-Cu electrical connections at the interface. An important parameter that is usually used for Cu-Cu electrical qualification at the interface is the contact resistivity. As defined by Berger, the contact resistance is the additional resistance between an ideal contact and the practical one [29]. In the case of Cu/Cu bonding, an ideal contact corresponds to a perfectly reconstructed bonding interface where the contact resistivity approaches the Cu grain boundary one. Many parameters were found to deviate the contact resistivity from its ideal value. For instance, Taibi evidenced a contact resistivity that decreases from 1.4×10^{-9} to 2.25×10^{-10} $\Omega.cm^2$ when increasing the bonding annealing temperature from 200 °C to 400 °C for a 3×3 μm^2 contact area [30]. This behaviour can be explained by the presence of Cu oxide layer. At 200 °C, this layer might still be existing at the Cu/Cu interface contributing to the increase in the contact resistivity. Even at 400 °C, the Cu/Cu contact resistivity is still two orders of magnitude above the theoretical grain boundary contact resistivity reported in the order of 10^{-12} $\Omega.cm^2$ [31]. Another important parameter that can contribute to the increase in contact resistivity is

the presence of cavities or Cu oxide nodules at the interface. Their existence has been highlighted in the case of Cu/Cu direct bonding [32] as well as Cu/SiO_2 hybrid bonding [33][34].

Jourdon proposed an explanation of the increase in contact resistivity due to the presence of voids at the Cu/Cu interface. It is based on the fact that these voids reduce the conductive section of bonding pads. The contact resistivity, due the presence of voids, can be defined as [35]:

$$\rho_{c,eq} = (R_{void} - R_{novoid}) \times w^2 \quad (1)$$

where R_{void} and R_{novoid} are the resistances of single Daisy Chain (DC) interconnects with or without void and w is the width of the bonding pad. Jourdon found that the interconnects resistance is negligibly impacted by bonding voids presence ($<$ 10 % resistance increase) as long as their occupation remains smaller than 90 % of the Cu/Cu contact area. This observation is valid for Cu pad of 3 μm in width.

The main challenge that was also highlighted by Jourdon is the lack of experimental methods capable of quantifying a contact resistivity below 10^{-9} $\Omega.cm^2$. For Cu pads above 3 μm, this was not of a main concern since the contribution of the contact resistivity of 10^{-9} $\Omega.cm^2$ to the interconnect resistance was below 10 %. However, this has a critical impact with pad size reduction because the contact resistivity depends on the contact surface between the top and bottom Cu pads with $\rho_c = R_c \times A_c$. Reducing the contact surface (due to Cu pad size reduction) leads to an increase in contact resistance for a given contact resistivity. Especially for Cu pad below 1 μm in width, the 10^{-9} $\Omega.cm^2$ criterion leads to a significant increase of the interconnect resistance (>50 %). Even though the degree of importance of the resistance increase depends on the specific type of application, we aim to define in the present PhD work the correct process specifications to have the lowest possible contact resistivity at the interface. In other words, we aim to achieve a contact resistivity close to the grain boundary one. To do that, the main challenge is the development of new test methods and structures for accurate quantification of contact resistivity at the Cu-Cu interface with pitch reduction.

W2W overlay impact on electric yield

Another parameter that may impact the electrical yield with pitch reduction is W2W overlay. This challenge arises from the specific process of the hybrid bonding technology. During the bonding step, the two wafers are aligned with respect to each other by using special alignment marks. A misalignment can occur that is the sum of the translation, rotation and scaling (run out) as schematically illustrated in figure 5 [36] [37]. The presence of misalignment leads to a reduction of the contact surface between the top and bottom Cu pads. Currently, the standard bonding tool performance accuracy is ± 200 nm. This is sufficient to achieve a 100 % electric yield for pitches above 1 μm. However, important question arises if any yield loss can take place in the sub micron pitch region.

For the integration of interest in my PhD, with a via+pad configuration at interface (HBV-HBM), Jourdon defined the minimum pitch limit that can be achieved to be equal to 0.976 μm assuming a misalignment of 200 nm [34]. This assumption is based on the

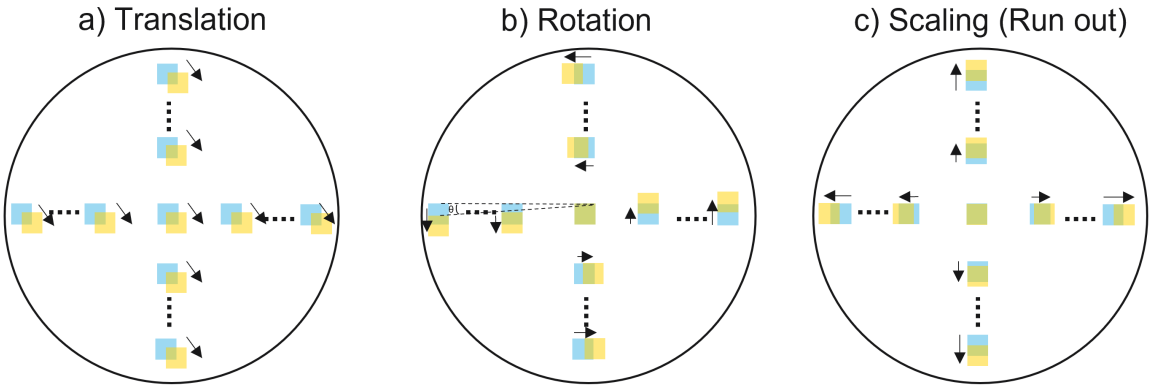

Figure 5: Schematic illustrations of the misalignment that can occur during the bonding step with a) translation, b) rotation and c) scaling (run out). The yellow and blue squares are used to illustrate Cu pads from the top and bottom wafers.

hypothesis that electrical connections issues might occur when the contact surface at the Cu-Cu interface is below the critical surface of the HBV. In the present PhD work, we aim to study the validity of this hypothesis for hybrid bonding pitch below 1 μm. If validated, new solutions should be proposed to mitigate any potential yield loss.

In addition, beside its impact on the electric yield, W2W overlay leads to an increase in the interconnection electrical resistance. Its impact on the electrical resistance increases with the reduction of the hybrid bonding pitch [36]. The acceptable overlay limits should be set depending on different criteria with respect to the electrical resistance. Moreover, interactions are expected between the W2W overlay and the contact resistivity since both parameters are directly related to the contact surface. Any interaction should be understood and clearly defined to achieve high electrical yield.

III.2 Assessing the reliability of the hybrid bonding level

The hybrid bonding level is usually treated as a BEoL technology. The main reliability challenges studied for a BEoL level directly apply for the hybrid bonding level. The main risks that have been studied in the literature includes the mechanical stability of the interface, the stress induced voiding (SiV) phenomenon, the electromigration (EM) failure mechanism, Cu diffusion in the dielectric as well as the time dependent dielectric breakdown (TDDB) mechanism.

Until this day, no major failure has been reported with respect to the mechanical stability of the interface and the thermally activated mechanisms (such as the SiV) down to 1 μm pitch [38]. For the integration of interest in my PhD, the robustness of the hybrid bonding level was previously studied down to 1.44 μm bonding pitch showing a good robustness [21]. With the reduction of the hybrid bonding pitch, Cu pads are closer to each other that lead to higher thermomechanical constraints and interactions at the interface. Therefore, the mechanical stability of the interface and the thermally activated phenomena (namely SiV) should be studied with pitch reduction below 1.44 μm to ensure

the robustness of the hybrid bonding level.

The EM mechanism can be defined as an atomic flow driven by the electrons and enhanced by temperature and mechanical stresses [39]. The EM failure mechanism is a major concern for interconnections in BEoL level due to the continuous shrink of their dimensions that leads to an increase in the electrical current densities [40]. Moreau introduced a detailed electromigration study for hybrid bonding based integration technology with a via+pad configuration [39]. The studied integration is similar to the one of interest in my PhD with Cu/SiO_2 hybrid bonding and a level containing HBV and HBM. For pitches above 6 μm, the electromigration killer void was always reported to take place at the BEoL level, in the top or bottom metal lines depending on the electrons flow direction [39] [41]. With the reduction of the pitch, important concern arises on the immunity of the hybrid bonding level to EM killer void occurrence. A study reported by IMEC with Cu/SiCN integration and a top pad smaller than the bottom pad showed an EM killer void at the hybrid bonding level for pitch around 3.42 μm. If similar change in the killer void location is validated for our integration with HBV and HBM, it might lead to lower performances at use conditions. Hence, it is important to study if any change in the electromigration failure mode for pitches below 6 μm could degrade the projected performances at use conditions.

Moving to the Cu diffusion reliability risk, it is a major concern for the hybrid bonding integration, particularly the Cu/SiO_2 one. This potential risk is the main motivation to adapt hybrid bonding configuration with a dielectric barrier type at interface, such as the SiCN adapted by IMEC [25]. During the bonding step, a misalignment between the top and bottom wafers is expected. This leads that part of Cu pads will directly faces the SiO_2 dielectric. Cu was well reported to highly diffuse in SiO_2 in the literature under atomic and ionic forms for the BEoL cases [42] [43]. Any presence of Cu diffusion for the Cu/SiO_2 hybrid bonding case could seriously degrade the properties of SiO_2. For the configuration of interest in my PhD, with Cu/SiO_2 hybrid bonding and for pitches above 6 μm, many studies have been done by Moreau and Jourdon where no Cu ionic or atomic diffusion were identified [44] [45]. A hypothesis was put in place based on the presence of a self-formed Cu_2O layer at the interface in the area where Cu is directly facing SiO_2, which could act as a potential barrier to Cu diffusion. The validity of the hypothesis of Cu_2O as a barrier to Cu diffusion at the Cu/SiO_2 hybrid bonding interface should be investigated for sub micron pitches.

The last reliability risk that is extensively studied for BEoL level and could be a concern for the hybrid bonding technology is Time Dependent Dielectric Breakdown. As defined by McPherson, TDDB refers to the physical process whereby a dielectric stored under a constant electric field, less than the materials breakdown strength, will breakdown upon time aging [46]. For the Cu/SiO_2 hybrid bonding integration, TDDB is critical arising from a potential misalignment between the top and bottom wafers will eventually lead that part of the Cu pad is directly facing SiO_2. Any Cu ionic or atomic diffusion could degrade the dielectric insulation properties leading to lower failure times. The only TDDB study was reported by Kagawa from Sony for a Cu/SiO_2 hybrid bonding integration (similar architecture design (Cu/SiO_2) to the one of interest in my PhD) and for pitches down to 3 μm. The author guaranteed the 10 years performance at use condi-

tions [20] [47]. The TDDB performance highly depends on the characteristics of Cu and SiO_2 that are unique to each integration. Hence, it is critical to investigate the TDDB failure mechanism for our integration with Cu/SiO_2 hybrid bonding. The reliability under TDDB with pitch reduction is a critical concern since Cu pads are closer. This might lead to modified conduction mechanisms with pitch reduction and should be targeted.

Now that the main challenges of pitch reduction for the hybrid bonding technology have been defined, we will present in the following sections the thesis methodology.

IV Thesis methodology

In an earlier work by the teams at STMicroelectronics, CEA-LETI and IMS, a hybrid bonding pitch down to 1.44 μm has been demonstrated that can allow an interconnection density with Cu/SiO_2 hybrid bonding in the order of 10^7 interconnections/cm^2. As discussed earlier, a hybrid bonding pitch limit of around 1 μm was concluded by the study of Jourdon that depends on the standard bonding tool performance (± 200 nm). The main objective of this thesis is to study the lowest achievable hybrid bonding pitch for our hybrid bonding integration that maintains acceptable electrical and performance characteristics and responds well to the device reliabilities criteria. Our main objective embeds all the key elements that will be studied in the following chapters including the electrical, performance and reliability aspects with the reduction of the hybrid bonding pitch.

Chapter 1: Hybrid Bonding Mechanism and Process

In this chapter, the Cu/SiO_2 hybrid bonding mechanism will be resumed based on the reported previous studies in the literature. A focus is done on the SiO_2/SiO_2 and Cu/Cu direct bonding mechanisms. The different hybrid bonding architectures will be presented as well as the different types of applications. The main test vehicles and structures that will be used to assess and characterize the hybrid bonding level with pitch reduction will then be presented.

Chapter 2: Hybrid Bonding Level Characterization with Hybrid Bonding Pitch Reduction

As discussed in section III.1, one of the main challenges with the reduction of the hybrid bonding pitch is the achievement of the electrical connections at the Cu-Cu interface. In the first part of this chapter, we will study the thermomechanical behaviour of individuals Cu pads with decreasing width down to 0.32 μm. For that, in-situ measurements with temperature using the Laue microdiffraction technique at the European Synchrotron Radiation Facility (ESRF) have been conducted. The objective is to study any change of the mechanical properties of Cu that may influence the Cu-Cu interface closure mechanism with the reduction of the Cu pad width. We will use the output of these measurements to define the theoretical dishing threshold, from a pure thermomechanical point of view, which is needed to establish Cu-Cu connections at the interface.

In the second part of this chapter, we will move to the study of the electrical behaviour with the reduction of the hybrid bonding pitch. The approach that will be adapted for pitch reduction is the shrink of the pad size while maintaining a spacing equal to the pad width. The via size will remain intact. We will study how the electrical resistance and capacitance, that are the main parameters defining the performance of the interconnects, vary with the reduction of the pitch. We will also define if any pitch limit exists for the current hybrid bonding configuration. In addition, we will define if the current bonding tool performance is sufficient to achieve high electric yield in sub-micron pitch region. Furthermore, discussions will include the role of contact resistivity at the interface with size reduction, which is the main parameter used for electrical qualifications. We will develop new test structures and methods adapted for the hybrid bonding configuration. Our main objective here is to define the dishing limit, from an electrical point of view, that guarantees a contact resistivity at the Cu-Cu interface close to the Cu grain boundary one. Achieving this implies a perfectly reconstructed Cu-Cu interface.

Chapter 3: Cu/SiO_2 Hybrid Bonding Level Reliability with Pitch Reduction

The third chapter will focus on extensive reliability studies at the hybrid bonding level with the reduction of the hybrid bonding pitch. We will focus on the following reliability risks, from the least to the most critical one as deduced from previous studies, which are: the mechanical stability of the hybrid bonding interface, the thermally activated phenomena (mainly SiV), the electromigration failure mechanism, Cu diffusion at the interface and the TDDB failure mechanism.

Higher thermomechanical interactions are expected with the reduction of the hybrid bonding pitch due to reduced spacing between adjacent pads. Hence, the robustness of the hybrid bonding level will be studied by thermal cycling (TC) and high temperature storage (HTS) tests. The objective is to study any robustness failure in the sub-micron pitch region.

For the EM failure mechanism, the objective is to study if the hybrid bonding level remains immune to the EM induced voiding, which was the case for pitches above 7 μm. Any change of the killer void location could have a direct consequence on the EM performances at use conditions. We aim to study any change in the failure mode under EM with hybrid bonding pitch reduction, which may possibly degrade the EM performance. This will be achieved by performing EM tests at different temperatures and stress current densities using specific test structures dedicated for the electromigration study.

The Cu diffusion in SiO_2 reliability risk, which is a major concern for the Cu/SiO_2 hybrid bonding configuration, will be also investigated in the third chapter. In the present work, our objective is to validate the hypothesis of a Cu_2O layer as a barrier to Cu diffusion with the reduction of the hybrid bonding pitch. We aim to understand the origin of the Cu_2O layer formation as well as its thermal stability under aging tests. For that, we will use the total x-ray fluorescence (TXRF) and liquid phase decomposition inductively coupled plasma mass spectroscopy (LPD-ICPMS) techniques for chemical investigation of Cu atomic diffusion that offer high precision limit as well as bias temperature stress

(BTS) coupled with triangular voltage sweep (TVS) for Cu ionic diffusion. In addition, the electron energy loss spectroscopy (EELS) technique will be used to chemically analyze the hybrid bonding interface state after thermal aging.

The last reliability risk that will be investigated in this chapter is the TDDB failure mechanism that occurs at the dielectric SiO_2 level. Our objective is to understand the degradation mode under TDDB and if there is any major role of Cu diffusion assisting breakdown. In addition, we aim to understand how does the hybrid bonding configuration with Cu/SiO_2 behave under TDDB as compared to BEoL typical interfaces with Cu and SiN/SiCN passivation layers. In other words, is the Cu_2O layer efficient in decelerating Cu diffusion under TDDB as compared to SiN and SiCN? This understanding will provide important recommendations for the future of the Cu/SiO_2 hybrid bonding technology in the sub-micron pitch region. To achieve this, a new test methodology will be developed and TDDB tests will be performed at different electric fields and temperatures.

At the end of this chapter, we will define the most critical reliability risks that should be studied in the sub-micron pitch region.

Chapter 4: Toward New Hybrid Bonding Configurations

Many barriers might emerge on two parallel aspects that may decelerate further hybrid pitch reduction and adaption of sub-micron pitches in actual applications. The first barrier is the existence of a pitch limit from a process point of view. This limit seems to be attained by Sony with their 1 μm hybrid bonding pitch, in which HBV and HBM have continuous shapes [48]. For our integration, with HBV and HBM, the presence of a similar pitch limit would require shrinking the HBV size to further reduce the hybrid bonding pitch. This leads to a significant increase in the interconnect electrical resistance since HBV is the most resistive part of all the hybrid bonding elements. In the first part of this chapter, we aim to overcome this potential barrier by adapting an alternative approach for pitch reduction through a decrease of the spacing between adjacent pads. Our objective is to study the impact of adapting such approach on the electrical behaviour of the hybrid bonding level as well as on its robustness.

Another barrier that might emerge with pitch reduction is the RC interconnect delay increase. The RC interconnect delay from the hybrid bonding level, as it is the case for any BEoL level, will increase while shrinking the width and spacing of the interconnections. Depending on each type of application, this might be a roadblock for adapting sub-micron pitches. To target this problematic, in the second part of chapter 4, we will study and propose new hybrid bonding configurations to mitigate the expected RC interconnect delay increase with pitch reduction. These solutions will be based, mainly, on reducing the thickness of the hybrid bonding level. Many challenges might arise such as the compatibility of the process with such configurations as well as any robustness issues. Studying the feasibility of the process, the electrical behaviour and the robustness of these new configurations as well as their pertinence for the sub-micron pitch applications are the main objectives of this section.

Finally, based on all the cumulated findings from the current work and by considering

the latest advancement related to the hybrid bonding field, we will define a new theoretical pitch limit that can be attained using the hybrid bonding technology.

Chapter 1

Hybrid Bonding Mechanism and Process

This chapter aims to briefly describe the hybrid bonding process and mechanism. It will include the state of the art of the different hybrid bonding architectures reported in the literature as well as the main fields of applications. Finally, the main test vehicles and structures will be presented.

1.1 Cu/SiO_2 hybrid bonding mechanism

The Cu/SiO_2 hybrid bonding mechanism involves two distinct bonding mechanisms that are SiO_2/SiO_2 and Cu/Cu direct bonding. In the following sections, we will introduce the different bonding mechanisms involved as reported in the literature. This will be useful especially to better understand the the electrical behaviour as well as the thermodynamical stability of the interface with hybrid bonding pitch reduction.

1.1.1 General principle

The direct bonding or hybrid bonding in the case of two materials is the spontaneous adhesion between two surfaces, without the need of an intermediate material (polymer, metal), at ambient temperature and atmospheric pressure. In general, the two main conditions are required that are surface cleaning and activation. These two steps make the surfaces smooth and eliminate the organic and inorganic contaminants that might create defects at the bonding interface.

First, the two wafers to be bonded are positioned facing each others. Adhesion can then be initiated at the center or edge of two wafers by a pin pressing the two wafers into contact. This leads to the formation and propagation of a bonding wave chasing the air present in between. This step takes no more than few seconds as illustrated by Beilliard for the case of quartz/Si direct bonding [49]. The energy required to separate the two wafers is defined as the bonding energy. Its value depends on the hydrophilic or hydrophobic nature of the two surfaces. The hydrophilic bonding leads to high bonding energy while offering several integration options [50].

When bonding at ambient temperature, the bonded wafers adhere to each other sufficiently enough to be handled without deteriorating the alignment precision. However, the two wafers can be easily separated due to the low bonding energy. Therefore, a thermal annealing step is needed to strengthen the interface interactions and hence the bonding energy.

1.1.2 $SiO2/SiO_2$ direct bonding

The first mechanism of SiO_2/SiO_2 direct bonding goes back to the year of 1989 and was developed by Stengel [51] and revisited by Tong and Gösele in 1998 [52]. This chemical model was based on the hydrophilic nature of the two surfaces to be bonded and is illustrated schematically in figure 1.1. In the Gösele model, Van der Waals forces based on hydrogen bond networks between oxygen and hydrogen atoms dominates SiO_2/SiO_2 direct bonding through absorbed water layers in which water molecules form a water cluster at temperature below 100 °C. As the temperature goes up above 100 °C, the water can diffuse around the bonding interface, resulting in hydrogen bonds between silanol groups on the surface of top and bottom wafers. Then, covalent bonds of siloxane are formed at the SiO_2/SiO_2 bonding interface at temperatures ranging from 200 °C to 700 °C. The nanogaps are closed when the temperature is increased above 700 °C (figure 1.1 (d)).

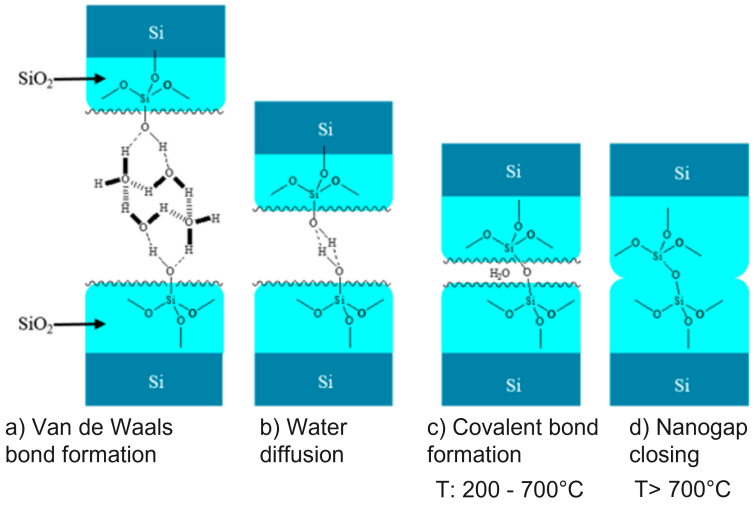

Figure 1.1: Schematic illustrations of SiO_2/SiO_2 direct bonding as developed by Stengel and revisited by Tong and Gösele [53].

In 2001, the accuracy of this model was questioned by Rieutord [54]. The author showed with the help of the bonding interface characterization by X-Ray reflectivity method that the bonding interface width (corresponding to the distance between the highest asperities of each surface) is constant up to 900 °C and decreases after. In addition, the role of water molecules absorbed at the surface of each wafer was put in evidence. In fact, for the bonding anneal temperatures below 150 °C, the presence of water limits the growth of asperities and thus the reinforcement of the interface. The full closure of the bonding interface is done at temperature higher than 900 °C thanks to material diffusion

activated at this high temperature.

Rieutord proposed a second mechanism of SiO_2/SiO_2 direct bonding [55]. This time, the nanometric roughness between the two surfaces to bond is considered and a model based on the contact of asperities is proposed. In this case, the contact between the two SiO_2 surfaces is produced at the highest asperity level. After bonding at ambient temperature, the adherence between the two surfaces is only due to the equilibrium between the attractive and repulsive forces present at the bonding interface. During the bonding anneal, the asperity contact areas become wider and adhesive leading to the formation of covalent bonds at the bonding interface and thus an increase in the bonding energy [56].

Furthermore, in 2015, Fournel reported an SiO_2/SiO_2 direct bonding mechanism with N_2 plasma activation. Fournel proposed that the asperity roughness evolves with internal water stress corrosion. The SiO_2/SiO_2 interface prevent the interfacial water from diffusion through the SiO_2. The remaining water between the asperities in contact penetrates in the tensile SiO_2 regions induced by compression forces. The bonding mechanism proposed can be assumed the same as the chemical model, but bonding can be achieved at lower temperatures thanks to the plasma activation [57].

A typical bonding energy between the SiO_2 surfaces after room temperature bonding is in the order of 0.1 J/m^2 [58]. This bonding energy increases with increasing temperature and reaches around 2.2 J/m^2 at 400 °C [58]. The use of N_2 plasma activation can lead to much higher bonding energy to around 7 J/m^2 at 400 °C [57].

1.1.3 Cu/Cu direct bonding

In this section, we will go through the details of Cu/Cu metal bonding mechanism that is the bonding between two blanket Cu wafers at room temperature and followed by thermal treatment [59] [60].

The prerequisite for Cu/Cu metal bonding is surface preparation and activation using a special chemical mechanical polishing step. The high hydrophilic nature of the surfaces to be bonded leads to the absorption of several water monolayers. The formation of a native oxide Cu_2O in the order of 1 to 2 nanometers of thickness preserve the hydrophilic character of the two wafers to be bonded. At ambient temperature, Cu/Cu adhesion is possible through Van der Waals and hydrogen forces due to the presence of the Cu_2O layer at the interface. An increase of the Cu/Cu bonding energy was evidenced by Di Cioccio from around 0.7 J/m^2 (after room temperature bonding) to 2.5 J/m^2 (after storage up to 140 days) [61]. This increase in bonding energy was linked to the evolution of the Cu_2O oxide thickness where a layer between 4 to 5 nm in thickness was evidence at the Cu/Cu interface after room temperature (RT) storage as shown in figure 1.2 [61].

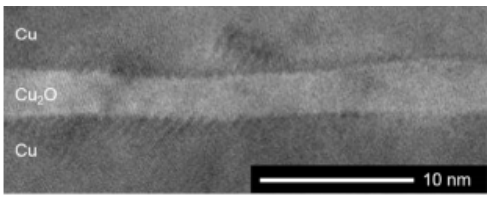

Figure 1.2: High resolution transmission electron microscopy (TEM) image showing the presence of Cu_2O of a thickness of 4 nm at the bonding interface. The Cu/Cu direct bonding was done at ambient temperature and the image was taken after several weeks of storage at RT [61].

Several experiments have been conducted to investigate the evolution of the Cu-Cu bonding interface during the annealing process. Studies done by Gueguen and Di Cioccio using transmission electron microscopy (TEM) inspections at different annealing temperatures have put in evidence two main phenomena: the dewetting or dissolution of the copper oxide layer and Cu/Cu interface reconstruction. The dewetting phenomenon can be linked to the competition between two energies: the interface energy between Cu and Cu_20 (γ_{Cu/Cu_2O}) and the grain boundary energy (γ_{gb}). From a purely thermodynamic point of view, the condition for a stable oxide layer between two metal layers (in our case Cu) is when $\gamma_{gb} > 2\gamma_{Cu/Cu_2}$. Between room temperature and 150 °C, the dewetting of the copper oxide takes place along the bonding interface and Cu oxide nodules can be formed. Above 150 °C, Cu grain boundaries are formed through the reorganization of the Cu/Cu interface with voids appearing at the interface. The illustration of the different stages in Cu/Cu bonding as a function of temperature is shown in figure 1.3 [62].

Furthermore, Martinez gave additional details on the Cu-Cu bonding mechanism during the annealing step. Using in-situ and quantitative TEM analysis, the authors showed that the Cu/Cu interface reconstruction during the annealing step is initiated by the apparition of diffusion wedges [63]. These wedges can be formed when annealing above 350 °C. Further annealing up to 400 °C leads to the growth of these wedges at the interface and assists to a fully reconstructed grain boundary zigzag shapes at the Cu/Cu interface (see figure 1.3, bottom schematics).

The Cu/Cu interface bonding energy strongly increases with temperature and can reach up to 3 J/m^2 after an annealing temperature of 100 °C [61] [64]. This high bonding energy makes extremely difficult the estimation of its value with higher temperature using typical destructive methods (such as four-point bending) because of sample breakage.

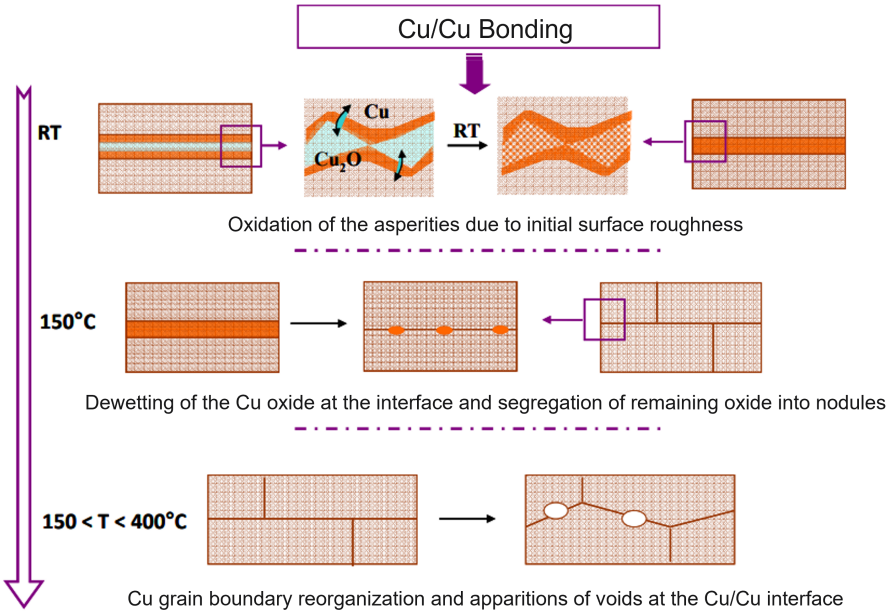

Figure 1.3: Schematic illustrations of the different stages in Cu/Cu bonding as a function of temperature [62].

1.1.4 Cu/SiO_2 hybrid bonding

Cu/SiO_2 hybrid bonding is the combination of the Cu/Cu and SiO_2/SiO_2 bonding mechanisms described in sections 1.1.3 & 1.1.2 respectively. The Cu bonding pads ensure the electrical connection between the top and bottom wafers as well as part of the mechanical adhesion. Direct bonding with SiO_2 assists the adhesion between the two wafers and serves as an insulation material between adjacent Cu pads.

Prior to hybrid bonding at room temperature, a critical step is needed that is the preparation of the two surfaces to be bonded through a specific CMP step. The CMP process should ensure low surface roughness that is essential to achieve Cu/SiO_2 hybrid bonding. It is possible to achieve enhanced surface activation through plasma activation coupled or not with bonding at ultra-high vacuum [65].

After the CMP step, several surface profiles can be obtained depending on the removal rate between Cu and SiO_2 as reported by Di Cioccio [61]. These can be summarized as following:

1. Flat surface between Cu and SiO_2 as shown in figure 1.4 (a). After bonding at room temperature, it is supposed that the Cu/Cu and SiO_2/SiO_2 surfaces are in contact. This represents the ideal scenario.

2. Cu pad in protrusion with respect to SiO_2 that takes places when the removal rate of SiO_2 is higher than Cu. After bonding at room temperature, voids can appear at the SiO_2/SiO_2 interface as shown in figure 1.4 (b).

3. Cu pad in recess with respect to SiO_2, referred as dishing as shown in 1.4 (c). After bonding, depending on the Cu dishing level and the presence or not of cohesive

forces at interface, only the SiO_2/SiO_2 surfaces are in contact. Therefore, at this stage, no Cu-Cu connections are established.

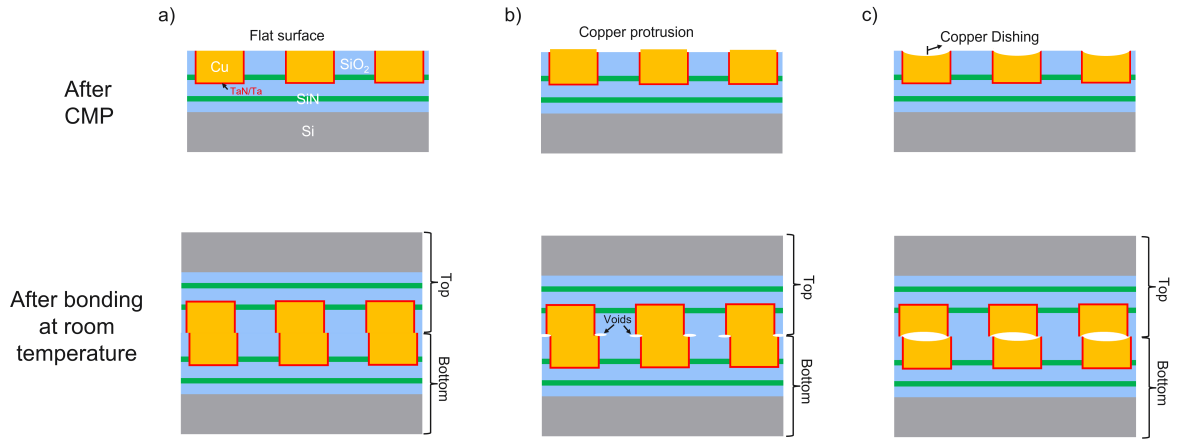

Figure 1.4: Schematic illustrations of the hybrid bonding scenarios depending on the surface profile with a) flat Cu and SiO_2 surface, b) Cu in protrusion and c) Cu pad in recess with respect to SiO_2 (dishing).

It can occur that three bonding scenarios are present in the same wafer, depending on the maturity of the CMP process. For the different cases, an annealing step is needed to reinforce the bonding energy at the interface. Even for the cases where Cu pads are already in contact (flat surfaces or pad in protrusion), an annealing step is needed to ensure the Cu_2O dissolution and interface reconstruction. In these specific cases, careful attention should be made regarding the protrusion level in order to avoid interface delamination during the thermal annealing step. In fact, due to the difference in the coefficient of thermal expansion (CTE) between Cu and SiO_2, a peeling stress could take place at the SiO_2/SiO_2 interface that could ultimately lead to interface delamination [23]. For the case with dishing at the Cu pad level, which is the approach adapted for the integration in this thesis, the annealing step is even more critical as it is needed to establish Cu-Cu connections between Cu pads. This is made possible through the thermal expansion of Cu. With the reduction of the Cu pad size width, more restricted Cu dishing levels are imposed for Cu-Cu connections establishments [22].

A mix between two surface profiles (dishing and protrusion) depending on wafer was also reported in [25]. IMEC, adapting a top pad smaller than the bottom one, uses a different slurry and polishing pad during the CMP step between the top and bottom wafers to generate protrusion at the top level and dishing on the bottom wafer. This strategy seems to be interesting especially when bonding with sub 1 μm Cu pads due to the limited thermal expansion of Cu.

For the Cu/SiO_2 hybrid bonding case, the bonding energy was reported around 1.14 J/m^2 after annealing at 200 °C and increases to 6.6 J/m^2 after thermal treatment at 400 °C for 2 hours [66].

1.2 State of the art on the hybrid bonding technology

There exists many hybrid bonding process variants that depends first on the type of metal and dielectric used at the interface and second the design and number of the metal pads.

Regarding the type of the metal material, the use of Cu is dominant [67] [20] [25]. Some studies investigated hybrid bonding with other metals such Al [68]), Au [69] and Ni [70]. However, most of these studies reported poor electrical connections at the interface. In addition, the use of Cu is compatible with the standard BEoL tools and processes that makes it the only material adapted in mass production.

Regarding the type of the dielectric material, the use of inorganic dielectrics, mainly silicon dioxyde (SiO_2) and in some cases SiCN, is dominant. Some studies used organic dielectrics such as polymer [71]. The use of polymer is beneficial especially for memory applications requiring low bonding annealing temperatures below 250 °C [72]. However, this process is not yet mature and challenges such as interface delamination and the establishment of Cu-Cu connections at interface need further study [72] [73].

Two designs exist with respect to the number and architecture of Cu levels at the interface. The first design is a hybrid bonding level composed of via (named hybrid bonding via HBV- in our study) and pad (referred as hybrid bonding metal HBM - in our study) at the top and bottom wafers. The Cu-Cu connections at the hybrid bonding interface is through HBM. The HBV is used to connect between the HBM and either the top or bottom metal lines. This design is referred in the following sections as via+pad. The second design is composed of only Cu pads (referred in the following sections as pad only) at the hybrid bonding level that ensures the Cu-Cu connections at the interface and with the metal lines. These two designs can be differentiated in figure 1.5 by comparing, for example, the integration of Sony (via+pad) and IMEC (pad only).

The first published articles with a Cu/SiO_2 hybrid bonding date back to 2006 (by Ziptronix society), with a technology called the direct bonding interconnect (DBI®) and an 8 μm interconnection pitch [74].

Sony introduced, in 2016, a Cu/SiO_2 hybrid bonding with a via+pad design and 4 μm hybrid bonding pitch for 3D stacked image sensors [20]. Lower pitches at 3 μm were reported in 2019 [47]. The latest achievement is a hybrid bonding pitch of 1 μm in 2020 [48]. Although not yet introduced in mass production of image sensors, it seems that the 1 μm pitch might be pertinent in a three-layered stacked system with a pixel parallel digitization architecture [75].

In 2017, Gambino presented the developments done by ON Semiconductor who also adapted the Cu/SiO_2 hybrid bonding technology with a pad only design. In their approach, a two steps bonding annealing is adapted with SiO_2/SiO_2 bonding at 100 °C followed by a bonding anneal at 300 °C for Cu-Cu bonding establishment. The hybrid bonding pitch reported is 8 μm with 3 μm wide Cu pads with an electric yield above 90 %.

IMEC has developed the Cu/SiCN hybrid bonding configuration with a pad only de-

sign. A size mismatch between the top and bottom pads is adapted to have some overlay tolerance during the bonding step. The use of SiCN can act as a barrier to Cu diffusion in the dielectric in the case of misalignment between the top and bottom wafers. Two steps annealing process is adapted: the first one at 250 °C to strengthen the SiCN/SiCN bonding interface followed by a second anneal at 350 °C to obtain Cu/Cu bonds. IMEC holds the lowest hybrid bonding pitch near 700 nm. This pitch was first reported back in 2017 but with an electrical yield loss around 50 %. In 2022, IMEC showed updated results of the 700 nm pitch with an electric yield of 90 % [76]. The origin of this continuing yield loss was not fully understood and may be related to a possible impact of misalignment or due to the thermomechanical behaviour of Cu, with Cu-Cu connections not established. The lowest reported pitch by IMEC with a 100 % electric yield is 1.08 μm back in 2020 [77].

The Yangtze Memory Technologies Co. (YMTC) company has developed its technology by using a size mismatch between the top and bottom Cu pads with a via+pad approach and a cap layer as dielectric at the interface (properties not reported) [38]. This technology was introduced for the 3D NAND memory stacking. The hybrid bonding pitch reported is around 1 μm with a 100 % electric yield and a smallest pad width at interface of 350 nm. The strategy adapted by YMTC for pitch reduction seems to be based on shrinking both the via and pad. YMTC have embedded the 1 μm pitch technology in their product ¨$Xtacking$ 2.0¨ making it the lowest hybrid bonding pitch present in consumer products [78].

CEA-LETI and STMicroelectronics started to develop the hybrid bonding process with Cu/SiO_2 with first published results dating back to 2008. The first interconnections had only 2 metal levels with an interconnection pitch of 14 μm. These structures permitted a complete study including the morphological, electrical and reliability characterizations [30]. In 2016, an interconnection pitch of 7.2 μm with the via+pad approach and 100 % electrical yield was reported [67]. The latest achievement is a 3D stacked image sensor with a hybrid bonding pitch of 1.44 μm in 2018 [21].

The main reported results on the hybrid bonding technology for pitch below 3 μm that were discussed in this section are summarized in figure 1.5. Examples of some applications integrating the hybrid bonding technology are shown in table 1.1.

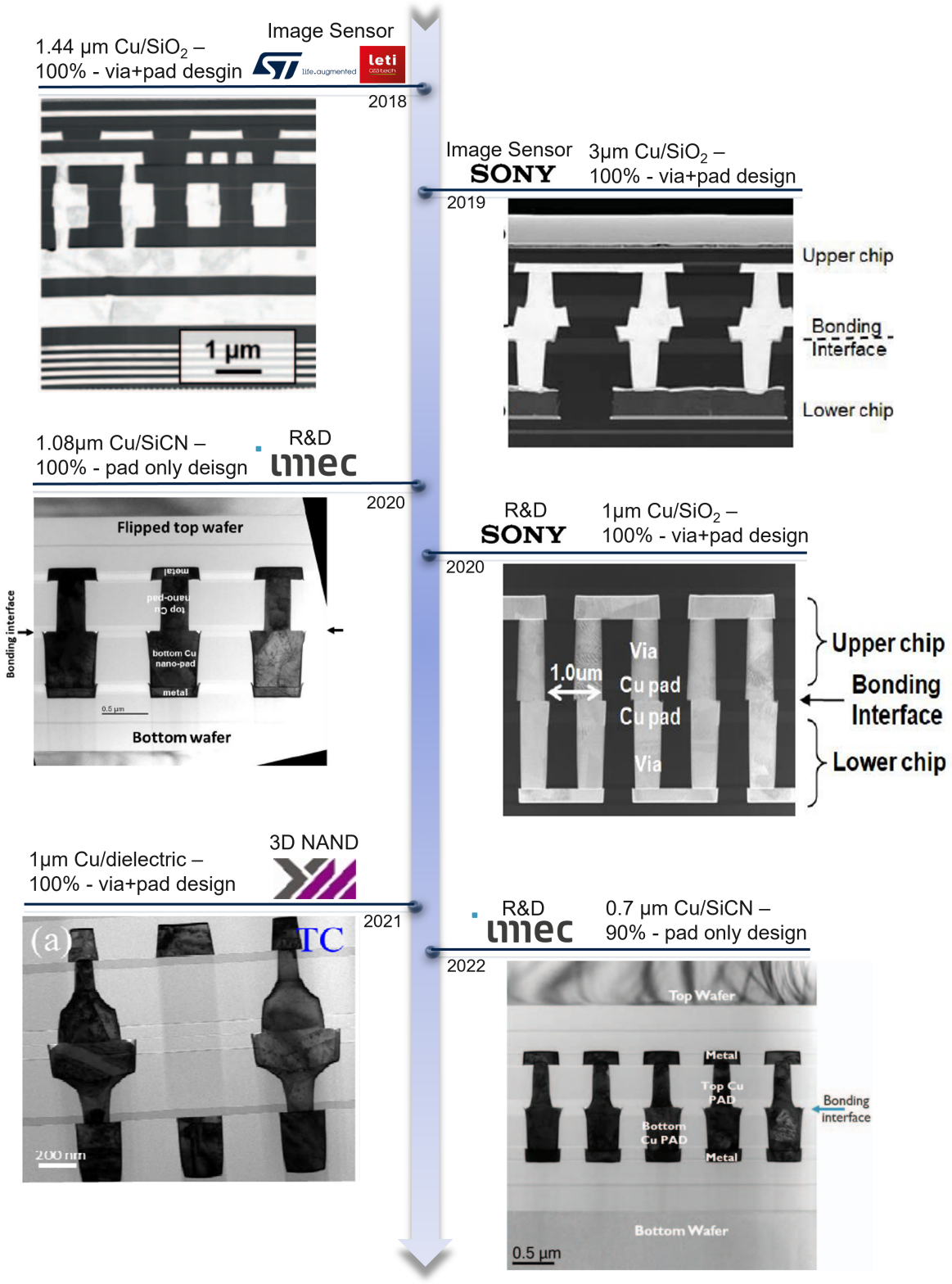

Figure 1.5: State of the art on hybrid bonding configurations for pitches below 3 μm. The configuration architecture, electric yield, application type/maturity level are indicated.

Table 1.1: Examples of some applications using hybrid bonding as the 3D stacking technology.

Year	Application Details	Stacking Technology	Hybrid Bonding Pitch	Company	Reference
2016	8 Mpixel 1.12 μm 65nm CIS 65nm 7 MLs CMOS logic	$Cu/dielectric$	-	Toshiba	[79]
2016	65nm SPAD CIS 40nm CMOS logic	Cu/SiO_2	7.83 μm	STMicroelectronics Uni of Edinburgh	[80]
2016	2 2.5 Mpixel 1.1 μm CIS 40 nm CMOS logic	Cu/SiO_2	4 μm	Sony	[20]
2017	16 Mpixel 1 μm CIS on logic wafer	$Cu/dielectric$	-	OmniVision	[81]
2018	14 Mpixel 1.5 μm 4 MLs CIS 7 MLs CMOS logic	Cu/SiO_2	8.8/1.44 μm	STMicroelectronics CEA-LETI Univ. of Bordeaux	[21]
2019	1.33 Mpixel 5 μm InGaAs/InP on silicon ROIC SWIR applications	Cu/SiO_2	5 μm	Sony	[82]
2021	25nm 3 MLs DRAM process 55nm 7 MLs logic process DRAM applications	$Cu/dielectric$	3 μm	Xi'an UniIC Semiconductors Co.	[83]
2021	Memory NAND die logic die NAND applications	$Cu/dielectric$	-	YMTC	[78]

1.3 Hybrid bonding pitch reduction: a need for many applications

In this section, we will discuss the importance of hybrid bonding pitch reduction down to sub-micron by considering the different types of applications that are currently integrating the hybrid bonding technology as a solution for 3D stacking.

1.3.1 Image sensor

With the reduction of the pixel pitch in image sensors and the need for higher 3D stacking interconnect density, the hybrid bonding technology is more and more adapted as compared to the TSV integration. In fact, one of the first and main application using the hybrid bonding technology was the CIS. Beside allowing direct vertical interconnection between the pixel and ISP chips, the hybrid bonding technology is beneficial in a three-layers stacked architectures where a memory chip can be inserted in between the pixel and the ISP tiers. In high volume production of image sensors, the lowest hybrid bonding pitch is around 1.4 μm and embedded by the ams OSRAM company with their product ¨Mira220¨ [84].

From 2010, the pixel pitch scaling slowed down because of the lower sensitivity for pixel pitches around 1 μm. Lately, since 2018, the pixel shrink has been accelerated again to meet market demands of multi-camera systems and digital zoom capabilities [85] [86] [87] [88] [89]. In 2022, a pixel pitch of 0.56 μm has been demonstrated [90]. The pixel parallel digitization architecture in image sensor, like Sony's design, could benefit from the reduction of the hybrid bonding pitch [91]. In fact, for this specific architecture, the hybrid bonding pitch should be equal to the pixel pitch.

More generally, hybrid bonding pitch reduction would allow the possibility to 3D stack

image sensors with higher interconnect density and offers the flexibility to design more efficient architectures. For instance, recent architectures by Sony in 2019 involve the use of Cu/SiO_2 hybrid bonding technology to 3D stack an InGaAs image sensor that is composed of III-V photodiode array (PDA) on a read-out integrated circuits allowing SWIR image sensor applications [82]. The design of such architectures was not possible without the hybrid bonding technology. Hybrid bonding pitch reduction down to sub micron could be also beneficial for intelligent vision sensor (IVS) that involves integrating AI processor [92]. To sum up, it is of no doubt that future demands for a variety of image sensor applications will involve the need of sub micron hybrid bonding pitches.

1.3.2 Memory applications

The hybrid bonding technology has recently emerged in many memory type devices such as the dynamic random access memory (DRAM) devices, 3D NAND and high performance computing (HPC) devices. For the memory applications, an annealing budget below 250 °C is needed. A lower thermal budget implies additional developments to achieve good electrical yield and Cu-Cu connections, which might explain the only recent adaption of hybrid bonding in these applications. One type of architecture for DRAM is the high-bandwidth memory. These devices traditionally use TSVs and micro bumps to increase the number of Input/Output (I/O) connections of logic-to-memory interface to provide high bandwidth at high data rate. With the increasing number of I/O, TSV connections will accumulate larger resistance and capacitance that can lead to high power consumption. In 2020, Xi'an UniIC Semiconductors adapted the hybrid bonding technology for DRAM by stacking the logic die (including control and I/O) above a DRAM array die with 3 μm hybrid bonding pitch [93]. The maturity of sub-micron hybrid bonding pitches is extremely beneficial for these type of devices to allow increased I/O number to provide higher bandwidth and data rate.

As for the 3D NAND, devices in mass production already embed hybrid bonding pitch of 1 μm by YMTC [78] [38]. The use of the hybrid bonding technology achieved faster I/O speed and higher bit density [94]. The rapid data volume growth for Artificial Intelligence (AI) and big data applications will require even higher I/O density that can only be achieved using the hybrid bonding technology with sub-micron pitch.

As for the HPC, it refers to computing systems with extremely high computational power that can solve complex and demanding problems. It is not until 2022 that the hybrid bonding technology has been adapted to HPC domain with the AMD 3D $V-Cache^{TM}$ product fabricated by TSMC with the 7 nm technolog [95]. The product announced by AMD company embeds hybrid bonding pitch of 9 μm that is driven by the TSV minimum pitch. Hybrid bonding pitches below 3 μm are to be adapted by Intel in their processors as announced in 2022 [96]. Ultra-high interconnect density 3D architectures, with hybrid bonding pitch below 1 μm, is a need to fit future computing and AI needs [96].

In conclusion of this section, it is clear the hybrid bonding technology is emerging as the main solution for 3D stacked ICs in many applications such as image sensors, HPC and memory devices. Based on the discussions made, sub-micron hybrid bonding pitch is a need for a wide range of devices allowing new architecture of 3D stacked systems.

1.4 Test vehicles and structures

This section aims to introduce the bonding process flow for the different test vehicles with a single metal level and a full flow electrical vehicle. We will also introduce the different generations of test vehicles used for the different studies in the present thesis work. The structures used for the electrical resistance and capacitance qualifications will be presented. The remaining structures will be introduced before their corresponding parts in their respective chapter.

1.4.1 Single metal level test vehicle

The bonding process flow with a single metal level is shown in figure 1.6. All the steps are done in the production fab of STMicroelectronics. Several successive layers of SiO_2/SiN are first deposited on the Si substrate. The different Cu patterns are then defined inside the dielectric by the lithography and etch steps (figure 1.6 (2)). The Ta/TaN barrier is deposited followed by Cu seed deposition by physical vapor deposition (PVD) technique. The patterns are then filled with Cu by electrochemical deposition (ECD) technique as illustrated in figure 1.6 (3). A chemical mechanical polishing (CMP) step is needed and processed to remove the excess of Cu and the Ta/TaN layers and to prepare the two surfaces to be bonded. After CMP, the Cu pads are in slight recess with respect to SiO_2 that is known as Cu dishing as illustrated in 1.6 (4). The two wafers are then aligned and bonded at room temperature. An annealing step is done at 380 °C for 2 hours to establish the Cu-Cu connections and to reinforce the bonding energy. The scanning acoustic microscopy (SAM) inspection is then done to study the presence of bonding defects at the wafer level. If no bonding defect is present, the top Si can be grinded and thinned down by wet process. For the Cu diffusion analysis, which will be presented in chapter 3, the top Si is thinned down to 3 μm. For the different TEM observations, the top Si is thinned completely by grinding process while stopping on the first SiN layer deposited in front side.

The different masks for single metal level processing are referred as the CPMX masks with ¨X¨ donating the corresponding generation. The different single metal level test vehicles used in the present thesis are the following:

1. CPM3: this test vehicle is composed of Cu matrices with HBM width of 3.3, 3.6, 4.4 and 5.4 μm and a pitch twice the HBM width. The samples processed with the CPM3 test vehicle are used for the Cu diffusion analysis that will be presented in chapter 3.

2. CPM6: this is composed of Cu matrices with HBM width of 3, 2, 1, 0.5 and 0.3 μm and a pitch twice the HBM width. This test vehicle will be used for hybrid bonding demonstration down to 600 nm in pitch. The samples processed with this test vehicle will be used for the different Laue microdiffraction studies performed at the ESRF and that will be present in chapter 2.

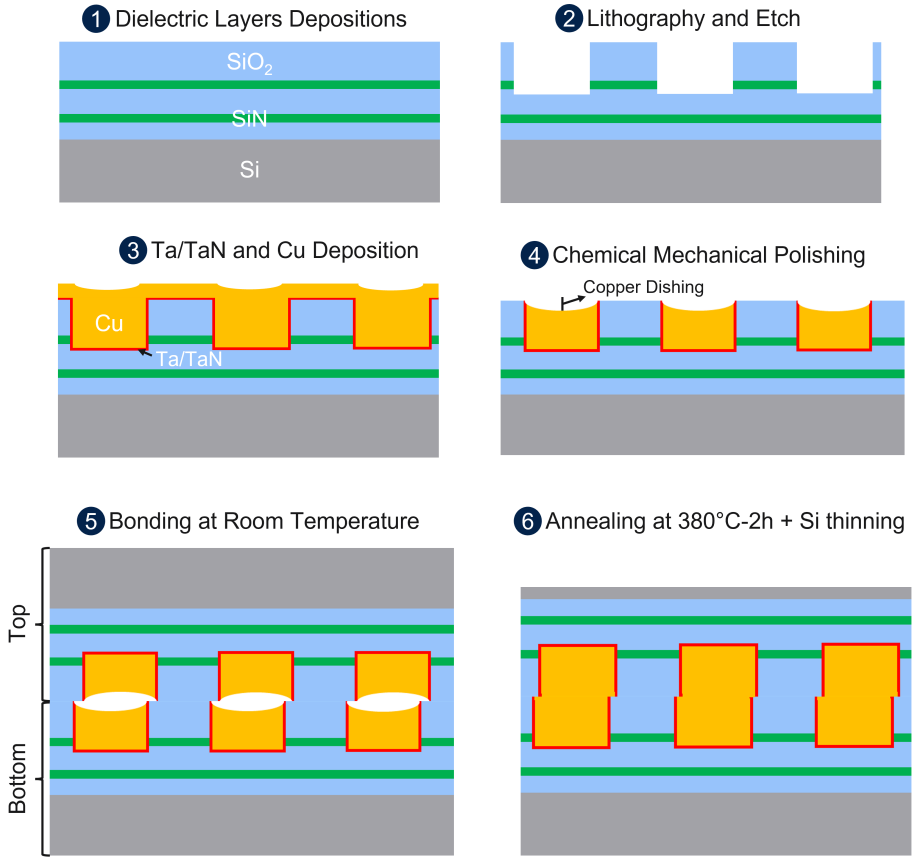

Figure 1.6: Process flow description for hybrid bonding with a single metal level (ML).

1.4.2 Full flow electrical test vehicle

The fabrication process of the electrical test vehicles is presented hereafter. All the steps are done in the production fab of STMicroelectronics. The different process steps are shown in figure 1.7. After processing the different metal levels, in our case 4 on top wafer and 7 on bottom wafer, successive dielectric SiN/SiO_2 layers are deposited as shown in figure 1.7 (1). The hybrid bonding via (HBV) and hybrid bonding metal (HBM) levels are then processed and etched by a double damascene process. After etching, the Ta/TaN barrier is deposited followed by Cu seed deposition by PVD. The patterns are filled with Cu by ECD. A CMP step is processed to remove the excess Cu and Ta/TaN layers and to reach the topography level required for the hybrid bonding process. Bonding is done at room temperature followed by an annealing step at 380 °C for 2 hours. After bonding annealing, the SAM inspection is performed to identify the presence of any bonding defects at the wafer level. The top Si can be thinned down only if no bonding defects are detected. The back side illuminated (BSI) process can then be done until the Al pad formation. Electrical measurements of the different hybrid bonded structures can then be performed.

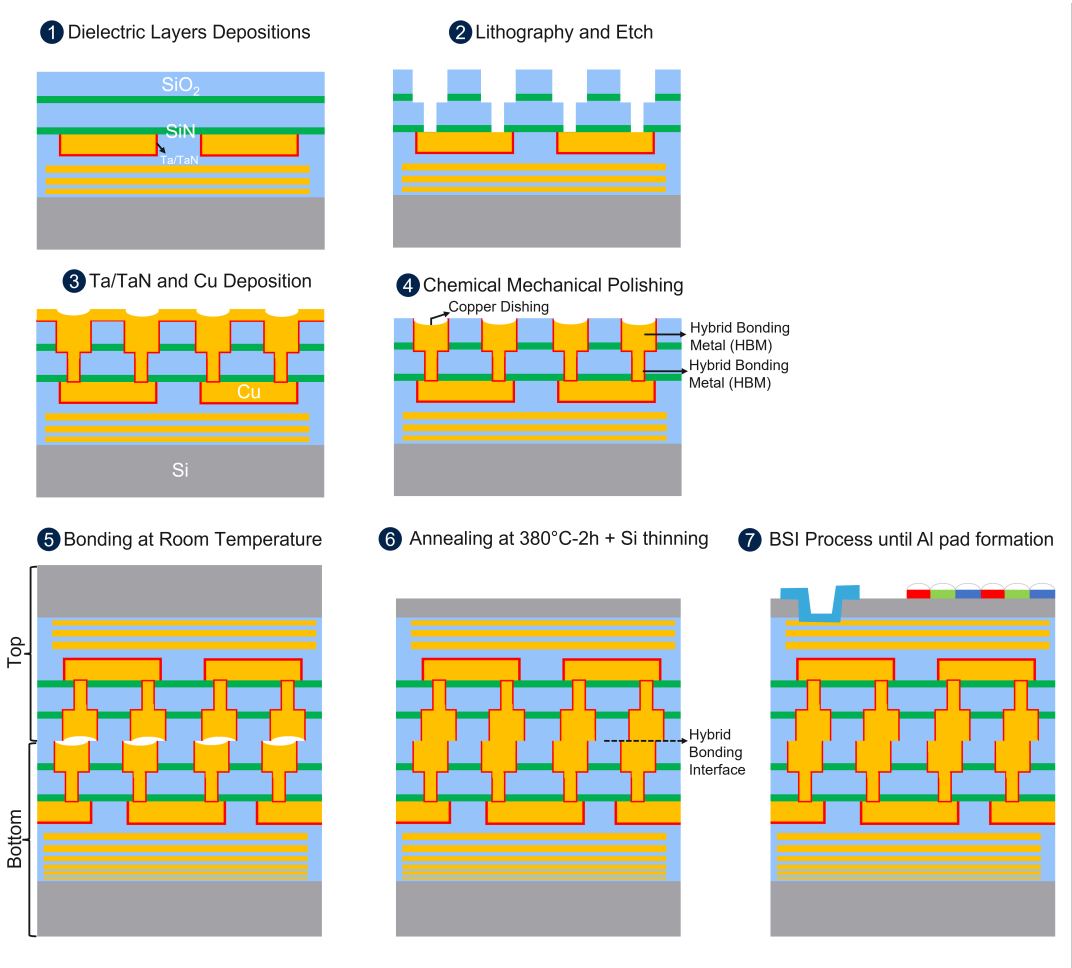

Figure 1.7: Hybrid bonding process flow description for the electrical test vehicles.

Three different electrical test vehicles, with different names assigned to ease referring later on in this manuscript, are used for electrical assessment that are the following:

1. Starsky and Hutch (S&H) that consists of electrical structures with pitch ranging from 6.84 down to 1.44 μm. The structures in this test vehicle were designed by Jourdon during his PhD thesis [34]. The S&H test vehicle serves as a reference with the 1.44 μm pitch. Most of the failure mechanisms studies (TDDB, Cu diffusion and electromigration) that will be presented in Chapter 3 are performed on samples from the S&H vehicle since wafers were available at the beginning of my PhD thesis.

2. TEDDY-Fine Pitch (FP) that consists of electrical pitch down to 1.44 μm. The test structures embedded in this test vehicle were mainly dedicated to the study of contact resistivity at 1.44 μm pitch. The aim was to evaluate their precision and relevance. In addition, the TEDDY-FP test vehicle is used to demonstrate new hybrid bonding configurations that will be presented in chapter 4.

3. TEDDY-Ultra Fine Pitch (UFP) that contains the structures designed in the present PhD work with the following electrical pitches: 1.44, 1.08, 0.9 and 0.81 μm. Pitch reduction is done by shrinking the size of the hybrid bonding metal (HBM) pad while keeping the hybrid bonding via (HBV) size constant. The choice of the lowest pitch (0.81 μm) is driven by the size and shape of the HBV as we expect for this

lowest pitch to have pad and via of continuous shapes. The reference structures in TEDDY-UFP test vehicle have an equal spacing and HBM width. Structures with spacing lower than the HBM width were also embedded and will be represented in chapter 4. The TEDDY-UFP test vehicle embeds structures for the contact resistivity evaluation down to 0.81 μm pitch. Most of the experimental electrical results presented in chapter 2 are based on the TEDDY-UFP test vehicle. Structures with pitch below 1 μm are also used to investigate any Cu diffusion in chapter 3.

The general electrical structures that are used to study the electrical behaviour with pitch reduction are the following:

1. Daisy chain (DC) structures with interconnection links of 100, 5k and 30k, which are used to study the electrical resistance behaviour with pitch reduction (figure 1.8 (a)).

2. Comb-comb structures with 57k interconnections used for leakage current and capacitance study with pitch reduction (figure 1.8 (b)). These structures were designed with comb legs along both X and Y directions to study the impact of overlay in X and Y.

The remaining electrical structures, for example the new designs for the contact resistivity evaluation and for Cu diffusion analysis, will be presented in their respective sections.

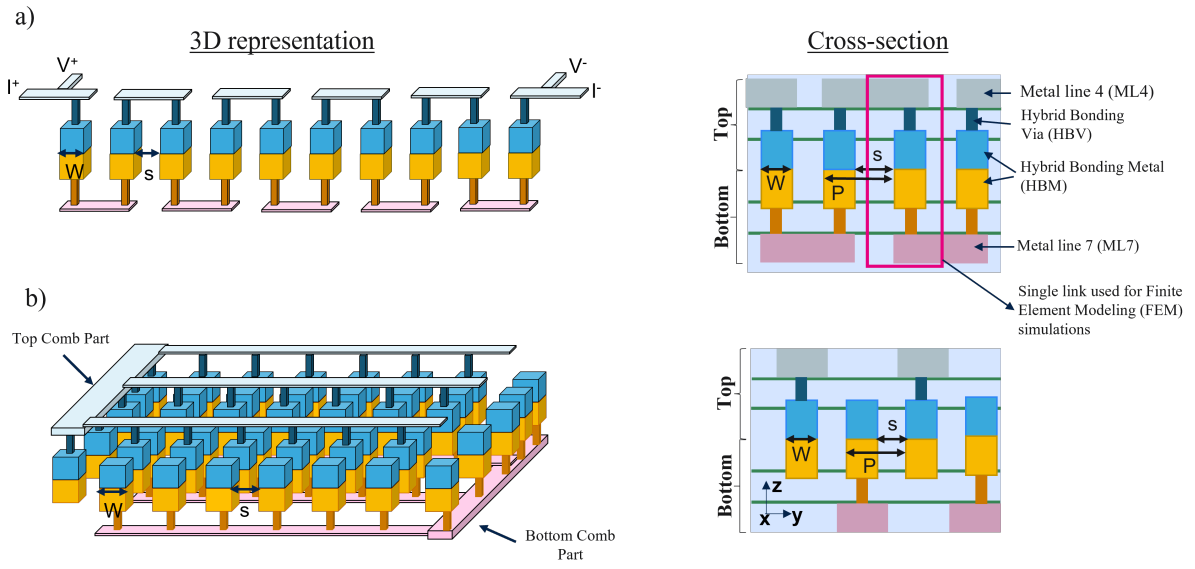

Figure 1.8: 3D (left) and cross section (right) representations of a) the daisy chain structure used for electrical resistance study and b) comb-comb structure used for leakage current and capacitance monitoring. W is the HBM width, s the spacing between adjacent pads and P is the hybrid bonding pitch.

A summary of the single metal and full flow test vehicles used in the present work is shown in table 1.2.

Table 1.2: Summary of the different test vehicles used for the hybrid bonding pitch reduction studies. Full Flow (FL) represents the electrical test vehicle and 1 Metal Level (ML) refers to the test vehicle with a single metal level at hybrid bonding level.

Test Vehicle	Full Flow (FL) / 1 Metal Level (ML)	HBM Width (μm)	Hybrid Bonding Pitch (μm)
CPM8	1ML	5.4	10.8
		4.4	8.8
		3.6	7.2
		3.3	6.6
CPM6	1ML	3	6
		2	4
		1	2
		0.5	1
		0.3	0.6
S&H	FL	3.42	6.84
		1.71	3.24
		0.72	1.44
TEDDY-FP	FL	0.72	1.44
TEDDY-UFP	FL	0.72	1.44
		0.54	1.08
		0.45	0.9
			0.85
			0.8
			0.75
		0.405	0.81
			0.755
			0.71
			0.675

Chapter 2

Hybrid Bonding Level Characterization with Hybrid Bonding Pitch Reduction

This chapter focuses on the thermomechanical and electrical characterizations of the hybrid bonding level with pitch reduction. The main objective is to study the bonding mechanism and the existence of any pitch limit from a thermomechanical and electrical point of views. To achieve this, we will focus on studying and understanding the requirements that drive successful hybrid bonding with pitch reduction.

The first key requirement with the reduction of the hybrid bonding pitch is the Cu-Cu interface closure after annealing. In fact, during the CMP step, Cu dishing is produced (see figure 2.1) and an annealing step is needed to achieve Cu-Cu connections. The establishment of Cu-Cu connections is directly driven by the thermomechanical behaviour of individual Cu pads during the annealing step. The thermomechanical behaviour includes thermal expansion, elasto-plastic behaviour, and Cu creep. The strain part based on the thermal expansion is believed not to significantly change from the bulk one for Cu pads with grains above 100 nm [97]. Hence, the main objective is to study the elasto-plastic properties and any role of Cu creep assisting interface closure with Cu pad width down to 0.32 μm. The main challenge of achieving this is the capability of the experimental methods to characterize Cu grains with dimensions down to 0.32 μm that justifies the need of synchrotron based measurements. In the first section of this chapter, the ultimate objective is to study if the Cu-Cu interface closure mechanism changes with the reduction of Cu pad size and to define any pitch limit from the thermomechanical point of view.

Characterizing the electrical behaviour, represented by the electrical resistance and capacitance, is the second key requirement with the reduction of the hybrid bonding pitch. In fact, important consideration with the reduction of the hybrid bonding pitch down to sub-micron pitch is the chip performance which is mainly affected by the resistance-capacitance delay (RC product) induced by interconnects. Hence, a focus is done in this chapter to understand the electrical behaviour of all elements of the hybrid bonding level both from the electrical resistance and capacitance aspects. Moreover, important parameter that can impact the electric yield with pitch reduction is wafer-to-wafer (W2W) overlay, which is solely driven by the bonding tool performance. With the standard

bonding tool equipment, W2W accuracy in the range of ±200 nm can be achieved. In this section, the W2W overlay limits to achieve 100 % electrical yield in the sub-micron pitch region will be defined. A specific challenge for the hybrid bonding integration is the qualification of Cu-Cu electrical connections at the interface. For that, we will define the contact resistivity as the criterion. The main challenge here is the precise estimation of the contact resistivity with the reduction of the hybrid bonding pitch. This is because the resolution of the methods that are conventionally used to assess the contact resistivity at the interface are not adapted for Cu pad width below 3 μm (this point will be detailed in section 2.2.1.2). Developing new methods for contact resistivity measurements allow the correct definition of the dishing threshold needed to secure Cu-Cu electrical connections. In the second section of this chapter, the ultimate objective is to define if any pitch limit exists below which Cu-Cu electrical connections at the interface are no longer guaranteed.

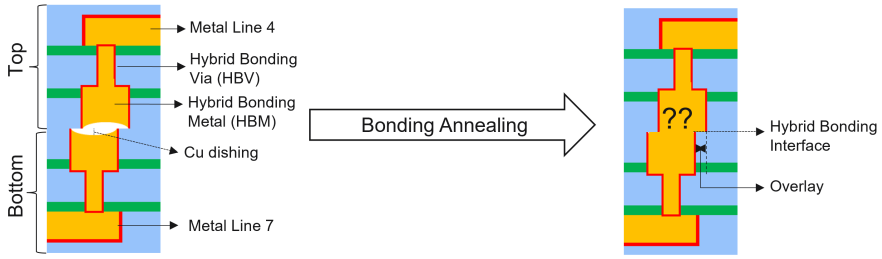

Figure 2.1: Schematic illustrations of the hybrid bonding level after bonding at room temperature (left) and after bonding annealing (right). The main challenge is the achievement of Cu-Cu connections with pitch reduction.

2.1 Thermomechanical characterization with Cu pad size reduction

Materials at small scales, especially in which the grain size is in the 100-1000 nm, have much different thermomechanical and electrical properties than the bulk one [26] [27] [28]. Hence, with the reduction of the hybrid bonding pitch driven by smaller Cu pad size at interface, fundamental questions arise that are key for sub micron pitch achievement:

1. How does the Cu properties vary from the bulk one with the reduction of the Cu pad width below 1 μm?

2. How does the microstructure, represented by the grain size, number and orientation, evolve with the reduction of the Cu pad size?

3. Is there any correlation between the grain orientation and grain size with their respective thermomechanical behaviour?

4. Especially for the hybrid bonding case, is there any Cu orientation favorizing Cu-Cu interface closure after annealing at the hybrid bonding interface?

Answering these questions is the key to understand the thermomechanical behaviour with Cu pad size reduction to sub micron dimensions. Therefore, in this section, we

will study experimentally the microstructure of Cu pads with decreasing width from 3 to 0.32 μm. In-situ measurements are performed to understand the mechanical behaviour of Cu with temperature (to mimic the bonding annealing step). Finite element modeling (FEM) simulations based on the experimental findings are then done to get the full picture on the behaviour of the 0.32 μm Cu pads and to define the dishing threshold needed to establish Cu-Cu connections.

2.1.1 State of the art: models for Cu-Cu hybrid bonding interface closure mechanism

In this section, we will focus on the hard contact model that considers that Cu-Cu interface closure is driven by the thermomechanical behaviour of Cu during the annealing step. Two approaches are reported in the literature based on this model: the first one is driven by deformation based on the thermal expansion and elasto-plastic behaviors of Cu while the second proposes an additional role of Cu creep.

For the first approach, Sart used 2D numerical simulations to study the most important parameters that drives interface closure after annealing [22]. For constant Cu pad width of 5 μm, the author found that the dishing depth will strongly influence the critical temperature, which is the temperature of full Cu-Cu bonding. Higher dishing depths will require higher bonding annealing temperatures to achieve full Cu-Cu connections. In addition, accounting Cu plasticity using a Ludwik power-law hardening rule allows to achieve lower critical temperatures as compared to the elastic behaviour. Most importantly, the author found that for a constant dishing and with decreased Cu pad size, the critical temperature increases exponentially when the interconnect Cu width is below 1 μm. Hence, the dishing threshold should be well defined, especially for sub 1 μm Cu pads, to achieve successful bonding of the interface. Moreover, Jin reported in 2022 a study on the Cu-Cu interface by thermomechanical 3D simulations for Cu pads of 5 μm without any role of creep [23]. The author found that the Cu bonding area increases both with higher annealing temperatures and lower dishing depth that is consistent with the findings of Sart. The author goes further by studying the peeling stress at the SiO_2/SiO_2 interface. Higher peeling stresses are found with decreasing dishing depth. The choice of dishing depth should not only rely on the achievement of Cu connections but careful attention should be made to avoid high peeling stress in the SiO_2/SiO_2 areas and prevent interface delamination after annealing.

For the approach including a role of Cu creep, Wlanis reported 2D and 3D numerical models including the surface roughness of the Cu pad measured using atomic-force microscopy (AFM) [24]. The author found that the 2D model underestimates the contact area ratio between the top and bottom pads as compared to the 3D model. The author showed that the roughness profile has an impact on the contact area formation after annealing. In addition, the author proposes that the creep mechanism can contribute to interface closure even at low annealing temperature of 200 °C. In addition, the Cu creep role is mentioned in several articles but without any details [98] [99].

Generally, there is a lack of experimental thermomechanical characterizations dedicated to hybrid bonding. Important considerations such as Cu anisotropy are not ac-

counted for in the numerical simulations. With decreasing Cu size width below 1 μm, we can suspect the appearance of one dominant grain at the pad level [100]. Any relation between the thermomechanical behaviour and the grain orientation could therefore impact the choice of the dishing threshold in the sub micron region. In the following section, we will study experimentally the thermomechanical behaviour with decreasing Cu pad width by focusing mainly on (a) characterizing the elastic-plastic properties with Cu pad size reduction and (b) assessing any role of Cu creep assisting interface closure. For the experimental measurements, the Laue microdiffraction technique at European Synchrotron Radiation Facility (ESRF) in Grenoble is used. FEM simulations are also performed to correlate with the experimental findings to conclude on the thermomechanical behaviour.

2.1.2 Experimental procedure

2.1.2.1 Experimental technique: Laue microdiffraction

The Laue microdiffraction technique with a synchrotron source is used to access the microstructure of Cu pads with decreasing size [101] for the main following reasons:

1. To analyze the microstructure of Cu pad width down to 0.32 μm, a technique with high resolution is needed. The Laue microdiffraction technique at the ESRF is a suitable technique since it allows to identify grain size down to 100 nm.

2. To study the thermomechanical behaviour of individual Cu pads while simulating the bonding annealing budget, an in-situ analysis is needed. Such analysis is possible in parallel with Laue microdiffraction measurements. Most importantly, by analyzing the Laue patterns, the state of deformation of the crystal lattice versus the theoretical or experimental reference could be assessed. This gives access to the deviatoric part of the deformation. This deviatoric part of the strain is related to the change of grain shape. Accessing the deviatoric part of the strain gives information on the presence of any plastic or creep behaviour during annealing, which is critical to understand the thermomechanical behaviour of Cu pads. To find the total strain in annealing, one should also consider the hydrostatic part which accounts the volume change. The geometry of experimental measurements (displacement of the beam) being very well controlled, it allows to reach a relative precision of 10^{-4} on the deviatoric strain tensor component [102]. This is not accessible by any other technique.

3. The employment of X rays to study the local orientation present many advantages as the surface preparation is much less demanding than other techniques, for instance electron backscatter diffraction (EBSD).

The main limitation when studying the behaviour of Cu grains with temperature using Laue microdiffraction is that any grain growth could not be precisely quantified. The EBSD technique allows for instance access to this information [103].

2.1.2.2 Experimental samples and studies

The samples used for this study are schematically represented in figure 2.2. The process flow was detailed in section 1.4.1. For the non bonded samples and after the CMP step,

a 60 nm layer of SiN is deposited on the top surface to avoid a possible Cu oxidation. For the bonded sample, the top Si substrate is thinned completely until the first SiN layer as shown in figure 2.2 (b). The different types of studies are detailed as following:

1. The first study is the analysis at room temperature of non bonded samples.

2. The second is an in-situ analysis with temperature up to 400 °C with the aim of simulating the thermomechanical behaviour of Cu pads during the bonding annealing step. For an ideal study, this analysis should be done on hybrid bonded samples directly after bonding at room temperature. This study is not feasible since bonded wafers without any annealing have low bonding energy. Cutting small samples for the in-situ analysis without de-bonding the wafers is not possible. For the same reason, thinning down the Si substrate at least to 3 μm to be able to localize the different structures is not achievable without de-bonding the wafers. Instead, the in-situ analysis with temperature is conducted on non bonded samples that can allow to conclude on the thermomechanical behaviour of Cu.

3. The third study is the analysis after bonding on bonded samples having the standard annealing step. The top Si is fully removed to easily localize the different structures. Preliminary numerical simulations were performed and showed that there is no impact of the top Si thickness on the stress/strain states at the Cu pad level.

Table 2.1 summarizes the characteristics of the different structures used for the different types of studies. Structures with 3, 2, 1 and 0.32 μm in Cu pad width are studied. For the in-situ analysis with temperature, only two extreme structures (3 and 0.32 μm) are analyzed. The thickness of the Cu pads is around 0.85 μm. Careful attention is made to the spacing between adjacent pads to avoid interference of diffraction signals. As a rule, the spacing of the Cu pads should always be higher than the pad thickness.

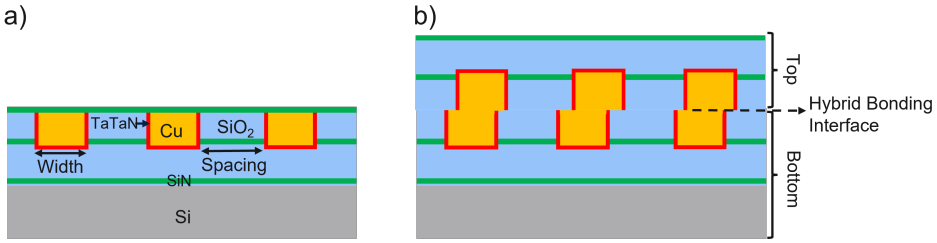

Figure 2.2: Schematic illustrations of a) non-bonded sample and b) bonded samples after top Si removal used for the analysis with the Laue microdiffraction technique.

2.1.2.3 Experimental set-up

The experimental set-up is schematically illustrated in figure 2.3. The measurements were performed at the BM32 beamline of the ESRF (Grenoble, France) in strong collaboration with the IM2NP (Institut Materiaux Microelectronique Nanosciences de Provence) laboratory. The polychromatic x-ray beam with an energy bandwidth from 5 to 25 keV is focused down to a size of 500 nm (H) × 500 nm (V) on the sample surface (which is inclined by 40° with respect to the incident beam) using a pair of Kirkpatrick-Baez mirrors. The diffracted x-rays are then recorded by a sCMOS detector (Photonic Science) with

Table 2.1: Description of the different structures used for the experimental study using the Laue microdiffraction technique.

Structure	Pad width (μm)	Spacing (μm)	Type of study Before bonding	In-situ with temperature	After bonding
A	3	3	X	X	X
B	2	2	X	-	X
C	1	2.1	X	-	X
D	0.32	2.5	X	X	X

2018 $\times$ 2016 pixels and a pixel size of 73.4 μm $\times$ 73.4 μm that is installed at an angle of 90° with respect to the incident x-ray beam at 77 mm from the sample position. An Anton Paar furnace was used for in-situ annealing experiments which were conducted at room temperature, at 100 °C and, then in steps of 50 °C up to 400 °C. The heating rate was 15 °C/min with a stabilization time of 5 minutes at each temperature step. At the highest temperature, three acquisitions were recorded to simulate the effective bonding annealing duration of 2 hours. The microstructure and deformation are further monitored while cooling down to ambient temperature with a step of 100 °C without controlled cooling rate. A cartography of Laue patterns acquisition is performed on the sample surface to cover 10 Cu pads for the 0.32 μm wide pad or 5 Cu pads for the 3 μm wide pad.

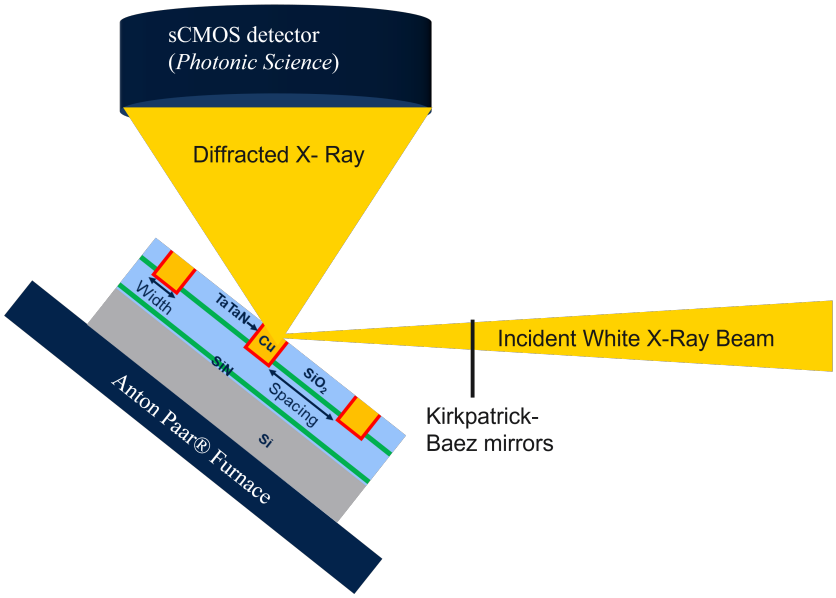

Figure 2.3: Schematic illustration of the experimental set-up for the Laue microdiffraction measurements. The non bonded sample is used for illustration.

2.1.2.4 Laue patterns analysis technique

The output of the measurements described previously is Laue patterns (example shown in figure 2.4), which corresponds to a single acquisition with both the Si and Cu elements. The ¨Lauetools¨ software that was developed by Micha at ESRF is then used to analyze the Laue patterns [104].

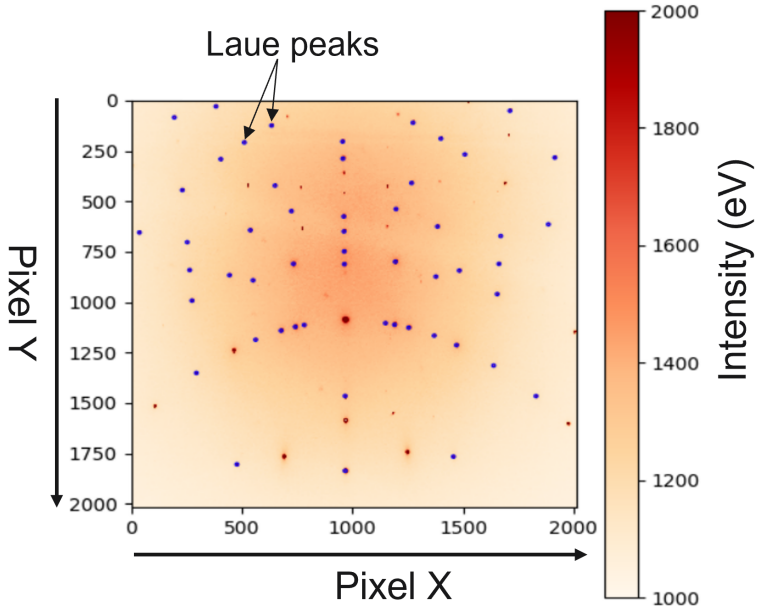

Figure 2.4: Example of Laue image output after acquisition for the non-bonded sample with 3 μm wide Cu pad and after background removal.

Below we describe briefly the analysis process:

1. Each Laue image contains peaks corresponding to the Si substrate and crystalline Cu. The first step consists of calibrating the detector parameters using the peaks of the Si crystal with known orientation of [001]. The calibration step is crucial as it can impact the accuracy of the found deviatoric strain. The calibration step is done at every temperature for the in-situ analysis.

2. After calibration, a peak search is launched to identify the different Laue peaks corresponding to both Si and Cu. The peak search can be launched automatically on a series of Laue images using the ¨peaksearch¨ module.

3. Each peak is then indexed with its respective match of material and crystal orientation. The comparison between the experimental and theoretical peaks allows to deduce the deviatoric strain tensor of each grain. This can also be launched automatically using the ¨Indexrefine¨ module.

4. To visualize the results, two modules are used: (a) ¨buildsummary¨ to classify the different data obtained (orientation, deformation...) and (b) ¨plotmap¨ which is an interface allowing to graphically visualize the results.

The main limitation of the ¨Lauetools¨ software is that the visual interface do not enable inverse pole figure (IFP) orientation map plot within a respective direction. Instead, the hkl Miller indices can be only visualized.

More recently, a neural-network based hkl recognition of the Laue spots was developed which is the ¨LaueNN¨ software [105]. The main advantage of this new software is the rapidity and accuracy of analyzing Laue patterns. By analyzing the image with

¨LaueNN¨, an output script is made available with the Euler angles of the different Laue images. Combining it with the MTEX software in Matlab, accurate IFP figures can be visualized [106]. Therefore, for the analysis of the grain orientation, the ¨LaueNN¨ software is used. For the deviatoric strain analysis, we will rely on the classical ¨Lauetools¨ software.

2.1.3 Experimental results

In this section, we will discuss the experimental results issued from the Laue microdiffraction measurements at ESRF. In our study, we will focus on the orientation and deviatoric strain perpendicular to the pad surface (i.e., Z direction) since it is directly related to Cu-Cu interface closure.

2.1.3.1 Results of non bonded single Cu pads at 30 °C

Microstructure dependence on Cu pad width

The IFP orientation maps, perpendicular to the Cu pad surface, are shown in figure 2.5 (a) for the 3, 2, 1 and 0.32 μm wide non-bonded Cu pads. The grain orientation varies between [001] to [111] and no dominant orientation can be highlighted for the different pad width. The average grain number is extracted from the IFP map as shown in figure 2.5 (b). The grain number decreases from 9 on average for the 3 μm wide Cu pad down to a single grain for the 0.32 μm Cu pads. We can therefore suspect the existence of a monocrystalline microstructure for the 0.32 μm wide Cu pads. We cannot eliminate the hypothesis of a dominant grain since, with the Laue microdiffraction technique, grains lower than 100 nm in size cannot be detected. Previously, Panchenko reported 12 grains on average for 4 μm wide Cu pads before bonding [103]. In addition, Kim studied the microstructure of Cu pads with 2, 1.2 and 0.8 μm width by EBSD before bonding and found that grain number decreases to few grains for the 0.8 μm with the appearance of one dominant grain [100]. In either case, no preferential or dominant orientation is identified that is consistent with our findings.

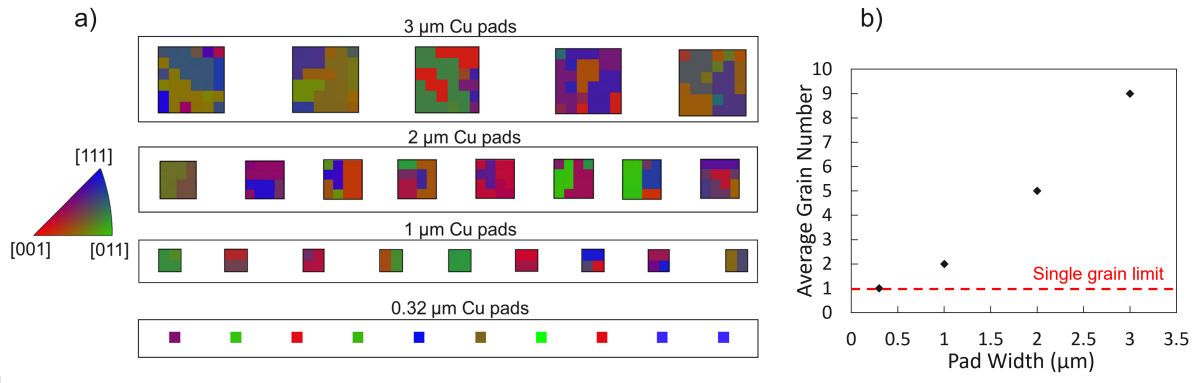

Figure 2.5: a) Inverse pole figure (IPF) orientation map perpendicular to the Cu pad surface for the 3, 2, 1 and 0.3 μm wide Cu pads from top to bottom respectively and b) the average grain with Cu pad width reduction.

The decreasing number of grains, for the specific Cu recipe used in our study, could have an impact on the thermomechanical behaviour under annealing, which could therefore alter the Cu-Cu interface closure mechanism. In addition, because copper is a very elastically anisotropic material (Zener ratio of 3.2 [107]), this spread in orientation could have direct consequences on the elastic behavior of different pads. In the following paragraph, we aim to study any dependence between the grain deviatoric strain at 30 °C and its respective crystalline orientation.

Deviatoric strain dependence on grain orientation

Each grain orientation is characterized by its respective Young's modulus. Hence, the Young's modulus is used to represent the grain orientation and to study any correlation with the deviatoric strain along the Z direction (ϵ'_{zz}). The Young's modulus is calculated using equation 2.1 [108]:

$$\frac{1}{E_{hkl}} = \frac{C_{11}+C_{22}}{(C_{11}-C_{12})(C_{11}+2C_{12})} - 2\left[\frac{1}{(C_{11}-C_{12}} - \frac{1}{2C_{44}}\right]\left(u^2v^2+v^2w^2+w^2u^2\right) \quad (2.1)$$

where $C_{11} = 168.4$ GPa, $C_{12} = 121.4$ GPa, and $C_{44} = 75.4$ GPa are the elastic constants of Cu taken based on literature from ref. [109]. u, v, and w are the direction cosines of the investigated direction calculated using the hkl Miller indices in the Z direction as following:

$$u = \frac{h^2}{(\sqrt{h^2+k^2+l^2})}, v = \frac{k^2}{\sqrt{(h^2+k^2+l^2)}}, w = \frac{l^2}{\sqrt{(h^2+k^2+l^2)}} \quad (2.2)$$

The deviatoric strain calculation of each grain differs with respect to its size. For the 0.32 μm wide Cu pads, each grain is represented by a single pixel, and the deviatoric strain is the single value of each pixel. However, for the 3 μm wide Cu pads, several pixels define a single grain. Therefore, when calculating the deviatoric strain, an average value is taken between the different pixels corresponding to the same grain. In addition, for the 3 μm wide Cu pads, only grains with pixel number higher than 10 are considered.

The deviatoric strains results measured at 30 °C are shown in figure 2.6 for the two extreme Cu pad widths. At 30 °C, a negative deviatoric strain is observed for all pads whatever their size. No clear correlation can be found between the deviatoric strain and Young's modulus. The absolute deviatoric strain level ($|\epsilon'_{zz}|$) is always higher for the 0.32 μm wide Cu pads as compared to the 3 μm polycrystalline wide Cu pads of similar orientation. This could be related to an impact of grain-grain interaction inside the 3 μm wide Cu pads limiting the ϵ'_{zz} strain contrary to the single or dominant grain inside the 0.32 μm pads.

The results of the analysis of non-bonded Cu pads at 30 °C, especially the dependence between the average grain number and the Cu pad width, arise several questions: (a) is there any relation between the grain size and its respective thermomechanical properties? (b) how does the grain orientation change with the bonding annealing budget, depending on its size? (c) focusing on the monocrystalline grains, how does the grain thermomechanical behaviour vary depending on its crystalline orientation? and what are

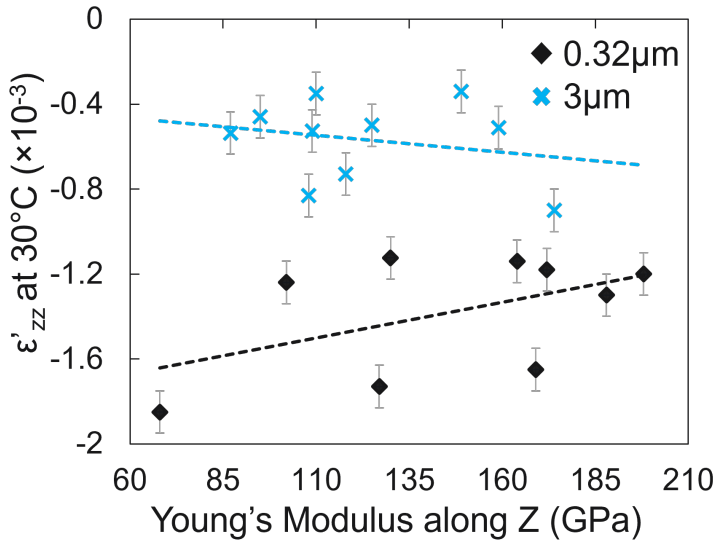

Figure 2.6: Grains deviatoric strains at 30 °C vs. Young's modulus for the 3 and 0.32 μm wide non-bonded Cu pads. Vertical bars represent the experimental uncertainty.

the consequences on the dishing specifications to be set with decreasing pad width?

To answer these questions, an in-situ analysis with temperature is needed and performed on the two extremes Cu pad width (the 3 and 0.32 μm Cu pads). This is presented in the following section.

2.1.3.2 Results of in-situ analysis with temperature on non bonded Cu pads

The in-situ analysis with temperature is performed on non bonded samples (schematic shown in figure 2.2) for the 3 and 0.32 μm wide Cu pads with the orientations reported in section 2.1.3.1. When annealing up to 400 °C and cooling down to 30 °C, no grain orientation evolution with temperature is found for the different pads. Possible explanation could be related to the fact that the grain orientation is directly driven by the post deposition anneal temperature. The bonding annealing budget up to 400 °C is not expected to impact the grain orientation. In the following paragraph, we will study the thermomechanical behaviour of the different grains by focusing on the deviatoric strain evolution with temperature as a function of the grain size/orientation.

Deviatoric strain evolution with temperature

For the sake of comparison, we choose to represent two grains selected between the 3 μm and 0.32 μm wide Cu pads with orientations close to either [111] or [001] and having a close calculated Young's modulus.

The results for the two grains with orientation close to [111] and high Young's modulus of 173 GPa are shown in figure 2.7 (a). The deviatoric strain after annealing time of 2 hours at 400 °C is presented. In heating, we observe the same tendency in deviatoric strain increase between the two grains of different size. The linear increase is especially respected for the grain inside the 0.32 μm wide Cu pad since it is formed mostly of a

single grain contrary to the grain inside the 3 μm Cu pad where interactions between adjacent grains can play a role. In addition, the assumption made when calculating the deviatoric strain as an average value between the different pixels could also lead to higher errors when presenting the 3 μm wide Cu pads. In cooling, a similar tendency is also observed but the single grain cooling curve is above the heating one contrary to the 3 μm grain. If plastic deformation occurs at 400 °C, we suspect to have the cooling behaviour above the heating one similarly to single grain result. The cooling behaviour observed for the grain inside the 3 μm wide Cu pad could be linked to a modified plastic behaviour as a results of interaction between adjacent grains with different crystalline orientation.

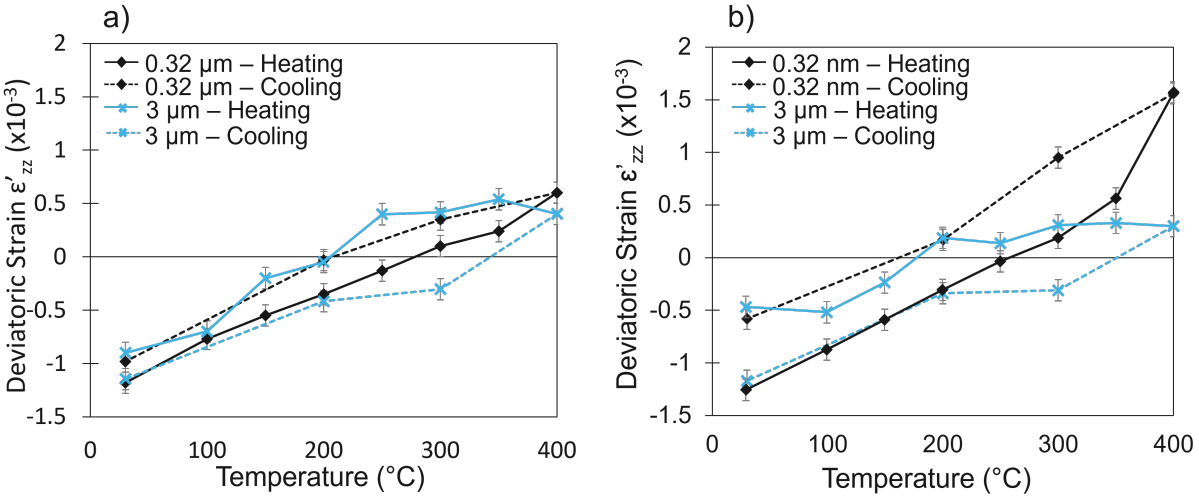

Figure 2.7: Deviatoric strain evolution with temperature for two grains selected between the 3 μm and 0.32 μm non-bonded Cu pads of orientation close to a) [111] and b) [001]. Vertical bars represent the experimental uncertainty.

In figure 2.7 (b), the result of two grains selected between the 3 μm and 0.32 μm wide Cu pads with orientation close to [001] and Young's modulus of 96 GPa is represented. Single grain inside the 0.32 μm wide Cu pad exhibits larger deviatoric strain at T > 350 °C which could be related to an impact of plasticity or creep. One might also relate this to the impact of Young's modulus evolution with temperature. We think this hypothesis is less probable since any Young's modulus evolution should have been refracted into an orientation change, which was not the case. Similar conclusion for the behaviour in cooling is obtained as for the two grains of orientation close to [111].

By analyzing the deviatoric strain vs. temperature curves for all the different grains, the following conclusions can be made:

1. For the 0.32 μm wide Cu grains, the closer the orientation to [001], hence lower Young's modulus, the higher the deviatoric strain at temperature above 350 °C.

2. By fitting a linear curve in the heating phase for the deviatoric strain between 30 °C and 350 °C, the strain free temperature (SFT) is found to lie between 200 and 300 °C for the 0.32 μm Cu grains. For the Cu grains of 3 μm pads, it is found to be between 150 and 250 °C that can explain the difference levels of deviatoric strains observed at 30 °C in figure 2.6.

3. For Cu grains of the 3 μm Cu pads, a stabilization of the deviatoric strain at temperature above of 350 °C can be observed. This behaviour could be verified by measurements above 400 °C, which were not covered during our experimental measurements. In addition, more grains should be studied for more statistics.

Important consideration for the hybrid bonding process is the Cu pad deformation during annealing since it will impact the Cu-Cu interface closure. To investigate this, depending on the Cu grains with different size and orientation, the delta of deviatoric strain between 30 °C and 400 °C - 2h is calculated and represented in figure 2.8. For the monocrystalline Cu grains, a clear correlation exists between the delta of deviatoric strain, and the grain orientation represented by the Young's modulus. Inside the 0.32 μm wide Cu pads, the grain with an orientation that has a smaller elastic constant along Z, i.e. closer to the [001] orientation, exhibits a larger deformation. When bonding with Cu pads containing a monocrystalline or a dominant Cu grain, the specifications for the maximum allowed Cu dishing depends on orientation and should therefore be set with respect to the grain orientation having the lowest deformation, in this case close to [111].

As for the larger Cu grains inside the 3 μm wide Cu pads, no correlation exists between the delta of deviatoric strain between 30 °C and 400 °C - 2h with the Young's modulus. In addition, lower delta is generally observed for the 3 μm Cu pads as compared to the 0.32 μm grains.

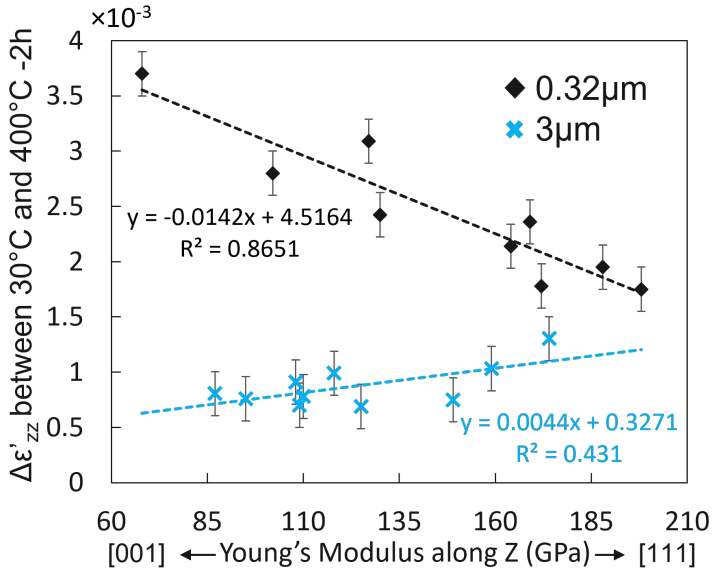

Figure 2.8: The delta of deviatoric strain between 30 °C and 400 °C - 2h vs. Young's modulus for the 3 and 0.32 μm non-bonded Cu pads. Vertical bars represent the experimental uncertainty.

In this section, we found that the deviatoric strain evolution with temperature depends on grain orientation for the pads with a single dominant orientation (0.32 μm wide pads) and on grain interaction for larger Cu pads (3 μm wide pads). The 0.32 μm wide Cu pads exhibit larger deviatoric strain under the annealing process as compared to grains with similar orientation inside the 3 μm wide polycrystalline Cu pads. Possible explanation could be related to: (a) different plastic behaviour and (b) the impact of grain-grain

interaction for polycrystalline 3 μm wide Cu pads. As mentioned earlier, this deviatoric part of the strain is related to the change of grain shape. However, to find the total deformation in annealing, we should be able to estimate the hydrostatic part that accounts the volume change and therefore can be seen as the major deformation part. One can take the hypothesis of a no stress perpendicular to the free surface (σ_{zz}) to move from the deviatoric to the full strain tensor. The hydrostatic strain can be estimated using the Hooke's law by mathematically solving a single equation. However, this approach might underestimate the total strain tensor leading to inconclusive results. To conclude on the thermomechanical behaviour, numerical simulations are needed to fit the experimental findings. Simulations for the 3 μm wide Cu pads should include Cu microstructure modeling and high simulation times of grain-grain interactions. This action was launched but could not be completed in my PhD. As for the 0.32 μm wide Cu pads, the modeling task is much simpler as there is only a single or a dominant grain. In section 2.1.4, the thermomechanical behaviour study of the 0.32 μm non bonded wide Cu pads will be presented.

2.1.3.3 Results of bonded Cu pads

Bonded samples with Cu pad width ranging between 3 and 0.32 μm wide were analyzed using the Laue microdiffraction technique. The analysis task using the LaueTools software could not be completed for the 2 and 1 μm wide bonded Cu pads. For these two samples, the spacing between adjacent bonded Cu pads is around 1.3 μm considering that the W2W overlay was around 0.7 μm. The total thickness of the two bonded pads is 1.5 μm that is higher than the spacing between pads. This led to interference of Laue microdiffraction signals from Cu pads leading to inconclusive results. This problem is not present for the 3 and 0.32 μm Cu pads.

The analysis using the LaueTools software is generally more difficult for the bonded Cu pads as compared to the non bonded ones. In fact, it is not possible to conclude on the origin of the Laue peaks with respect to either the top or bottom pads. TEM cross sections of bonded samples with 3 μm and 0.32 μm wide Cu pads are shown in figure 2.9 (a) and (b) respectively. For the 0.32 μm wide Cu pads, there is no Cu-Cu bonding taking place since the W2W overlay is higher than the pad width. As shown in figure 2.9 (b), Cu is bonded to SiO_2 that should be considered when analyzing the results. For this particular case, it is possible to separate the Laue microdiffraction signal coming from top and bottom Cu pads.

The deviatoric strain results of bonded Cu pads are shown in figures 2.10 (a) and (b) for the 3 μm and 0.32 μm wide Cu pads respectively. For comparison, the results of the non bonded Cu pads that have undergone the bonding annealing step are shown with their deviatoric state after cooling at 30 °C. For the 3 μm wide Cu pads (results shown in figure 2.10 (a)), the deviatoric strain results of the bonded and non bonded Cu pads that has undergone the same bonding annealing budget lie between -0.5 and -2$\times$ 10^{-3}. There is no clear impact of the hybrid bonding process on the deviatoric strain state. Similarly, for the 0.32 μm wide Cu pads with results shown in figure 2.10 (b), no clear tendency exists between the deviatoric strain and the orientation represented in our case by the Young's modulus. The difference between the bonded and non bonded Cu pads deviatoric

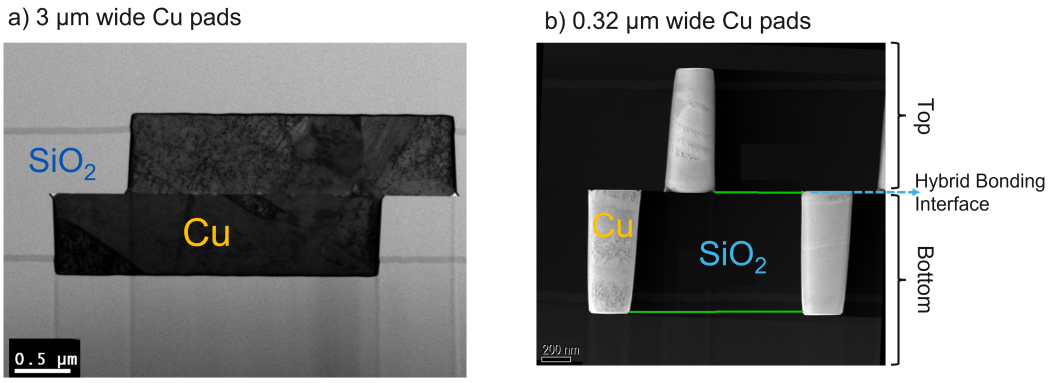

Figure 2.9: TEM cross sections of the bonded samples used for the Laue microdiffraction analysis with a) 3 μm wide Cu pads and b) 0.32 μm wide Cu pads. The overlay on the 0.32 μm wide Cu pads samples is higher than the pad width leading to Cu to SiO_2 bonding.

state is mainly for the grains with Young's modulus below 130 Gpa. This might be related to the restricted thermal strain in the case of bonded Cu pads where Cu is facing SiO_2 as compared to non-bonded Cu pads.

The accuracy of this comparison and observation is related to the initial state of the bonded Cu pads before any annealing. In fact, it is probable that grains with similar crystalline orientation might have different initial state of deviatoric strain that is related to the strain free temperature characteristic. It seems that, for this specific case study, the in-situ analysis with temperature is the only study capable of giving understanding on the thermomechanical behaviour of individual Cu pads during the bonding annealing step.

In the following section, the thermomechanical behaviour of individual non bonded Cu pads will be investigated numerically by fitting the in-situ experimental results in order to conclude on the individual Cu pads thermomechanical properties.

2.1.4 FEM study: 0.32 μm wide Cu pads

While Laue microdiffraction gives access only to the deviatoric strain, the full strain tensor is computed for the 0.32 μm wide Cu pads using FEM simulations. The results are discussed in the following sections.

2.1.4.1 3D-model description and material properties

COMSOL Multiphysics ® is used to study the thermomechanical behaviour of single non bonded Cu pads. The 3D model is based on a 0.32 μm wide Cu pad embedded in a SiO_2 matrix with 750 μm Si substrate as showed in figure 2.11. The thicknesses of Cu pads and SiO_2 were extracted from TEM images on the samples analyzed at the ESRF. Symmetric boundary conditions are applied as shown in figure 2.11. A fixed constraint is applied at the bottom Si side to avoid rigid body motion.

Regarding the material properties, a linear isotropic behavior is used for both Si and

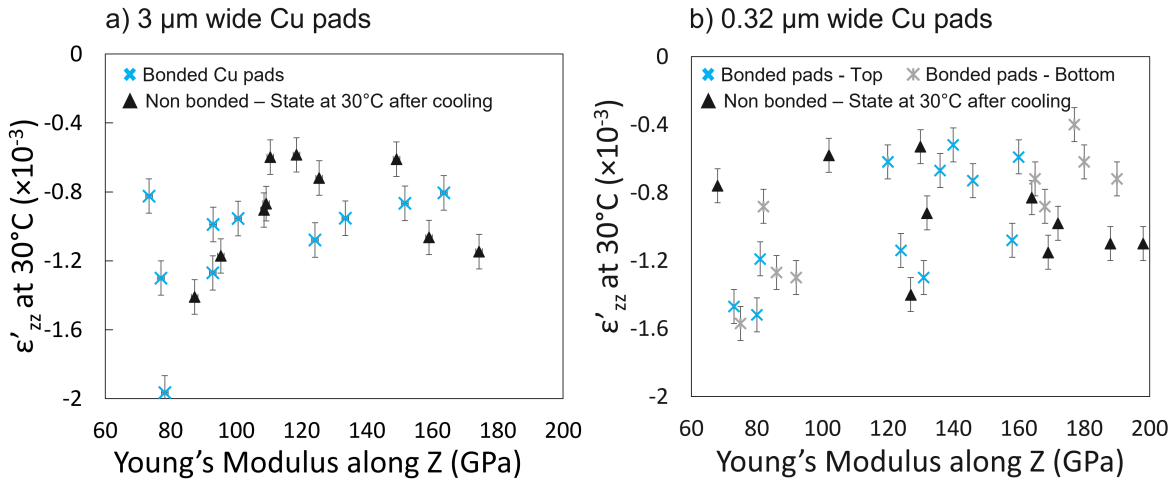

Figure 2.10: Comparison of deviatoric strain between bonded Cu pad and non bonded Cu pads at 30 °C (after annealing and cooling) vs. Young's modulus for the different grains inside the a) 3 and b) 0.32 μm wide Cu pads.

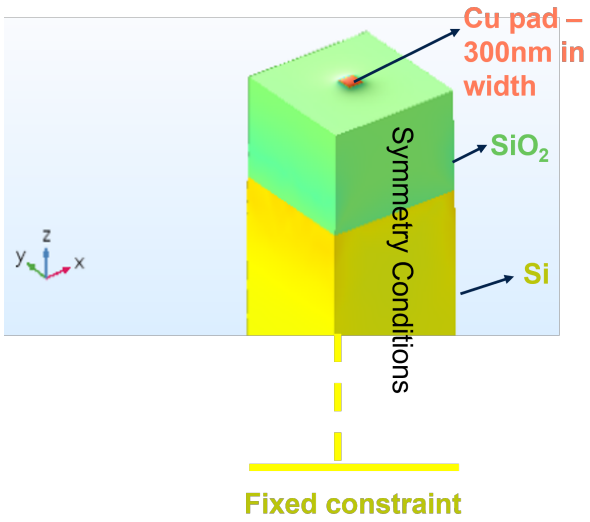

Figure 2.11: Description of the 3D model used for the FEM simulations of the 0.32 μm non-bonded Cu pads.

SiO_2. Their corresponding thermoelastic constants (E, ν and CTE) were taken from literature at ambient temperature as shown in table 2.2 [110] [111] [112]. As for Cu, we started by including the elastic anisotropy using the elastic constants previously defined. Most importantly, the rotation matrix was defined by taking the Euler angles inferred from Laue microdiffraction of each single pad. Each pad with its given material properties inferred from Laue microdiffraction was investigated separately by FEM. The CTE of Cu used is $16.5 \times 10^{-6}\ C^{-1}$ that corresponds to the bulk value [113]. An important parameter to define is the temperature at which the pad does not exhibit any thermal strain. The SFT was deduced for each single pad from the experimental curves.

Table 2.2: Material properties taken into account for the 3D numerical simulations for the 0.32 μm non-bonded Cu pads.

Material	Si	SiO_2
Young's Modulus E (GPa)	130	70
Coefficient of Thermal Expansion CTE (1/°C)	2.6×10^{-6}	0.5×10^{-6}
Poisson's ration ν	0.28	0.17

2.1.4.2 FEM results

The 3D numerical simulations results for the 0.32 μm wide Cu pads with the lowest and highest Young's modulus are shown hereafter. The behaviour in heating is solely studied and a comparison is performed with the experimental findings. As shown in figure 2.12 (a), for a pad with a high Young's modulus (orientation close to [111]), the simulations reproduce the linear experimental trend and fit well the experimental results at all temperatures. Similar behaviour is observed for all the Cu pads with an E > 130 GPa. However, for pads with E < 130 GPa, the fully elastic simulation fails to reproduce the nonlinear experimental behavior for T<150 °C and for T > 350 °C. This mismatch is shown exemplarily in 2.12 (b) for the pad with the lowest Young's modulus (orientation close to [001]). This observation clearly indicates the need to include additional behaviour other than the elastic one, which could be related to a plastic or any creep behaviour. In the following section, we start by studying any impact of plasticity.

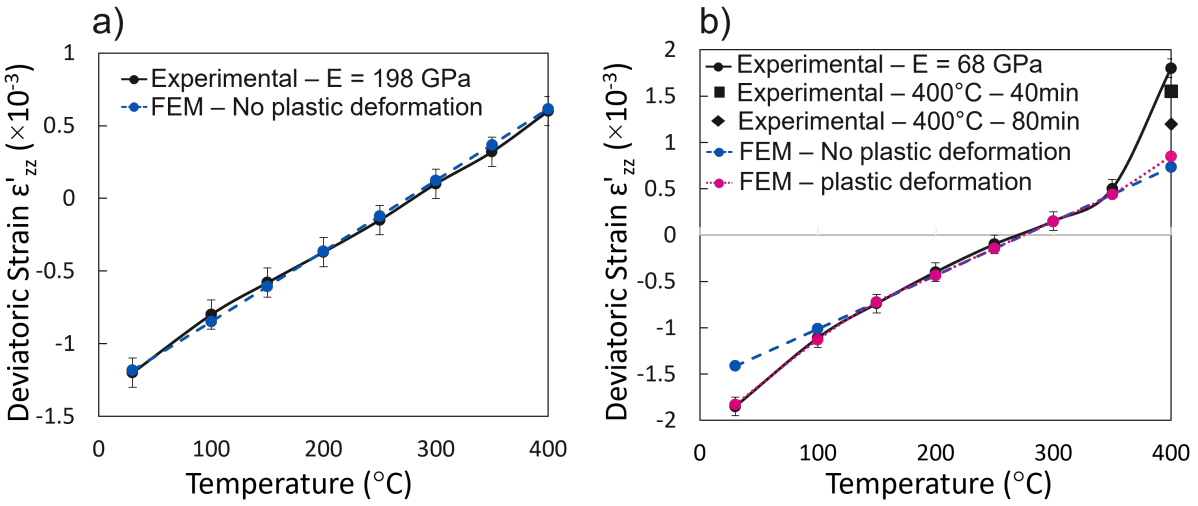

Figure 2.12: Comparison between experimental and FEM simulations results for the 0.32 μm wide non-bonded Cu pads with (a) the lowest E value (orientation close to [001]) and (b) the highest E value (orientation close to [111]). Vertical bars represent the experimental uncertainty.

Fitting the plastic behaviour

In order to account for plasticity within the FEM simulations, we adapted a Ludwik power law model that is given by equation 2.3 [114]:

$$\sigma = \sigma_y + K\epsilon_p^N \tag{2.3}$$

Where σ_y is the yield stress in MPa, K is the strength coefficient in MPa, ϵ_p is the plastic strain and N is the stress exponent. A nanoindentation study done by Sart on Cu with 1 μm thickness deposited on fullsheet Si wafer and grains with a size of 1 μm revealed a strength coefficient K of 1600 MPa, a yield strength σ_y ranging from 200 to 300 MPa, and N between 0.2-0.3 [22]. As we are dealing with much lower grain size, we expect to have different plastic behaviour and a dependence with the grain orientation. Therefore, a design of computer experiments (DoCE) mixing face-centered central composite design (FC-CCD) [115] and latin hypercube sampling (LHS) [116] is designed using Design Expert software with the range of variations for three variables shown in table 2.3. A total of 70 simulations are performed. This DoCE is applied at two different temperatures (30 °C and 100 °C) for each pad exhibiting a shift between numerical and experimental trends. The response of each simulation (run) for the DoCE is the deviatoric strain ($\epsilon_{zz}^{'}$).

Table 2.3: Input parameters with their range of variations for the design of computer experiments for plastic model fitting of the 0.32 μm wide non-bonded Cu pads.

Variable	Minimum	Maximum
Yield stress σ_y in MPa	100	400
Strength coefficient K in MPa	100	3000
Stress exponent N	0.1	0.9

After running the simulations, a two-factor interaction (2FI) response is selected that includes direct factor interactions and gives an adjusted and predicted R^2 greater than 95 %. For a given pad and temperature, numerous combinations of parameters exist giving the same deviatoric strain response as the experimental one. However, the number and range of combinations can be strongly restricted by fitting the complete range from room temperature to 100 °C. The results of fitting the plastic model variables are shown in table 2.4 for all the Cu pads exhibiting plastic deformation.

When adding plasticity to the computations, excellent agreement of the simulated behavior with the experimental behavior is obtained at 30 °C and 100 °C as shown in figure 2.12 (b) for the pad with the lowest Young's modulus. However, the model cannot reproduce the deviatoric strain evolution at 400 °C. The deviatoric strain evolution was experimentally monitored at 400 °C by consecutive Laue microdiffraction during the 2h annealing period revealing an increasing $\epsilon_{zz}^{'}$ with increasing time as shown in 2.12 (b). This behavior is observed only for the two Cu pads with E $<$ 120 GPa and can be linked to a role of Cu creep. In general, creep typically occurs for metals at temperatures on the order of half of the melting temperature (for Cu the creep temperature is around 500 °C which is below the annealing budget in this study). Considering the limited number of Cu grains studied experimentally, the exact parameters and the exact creep behavior

Table 2.4: Interval of the plastic model parameter's variations after fitting between 30 °C and 100 °C for the 0.32 μm wide non-bonded Cu pads.

Pad Young's Modulus (GPa)	Variables variations after fitting between 30 and 100 °C					
	σ_y (MPa)		K (MPa)		N	
	Min	Max	Min	Max	Min	Max
127	180	190	650	670	0.35	0.4
130	185	189	670	720	0.3	0.37
63	140	146	650	700	0.65	0.72
102	160	170	700	720	0.55	0.6

(Nabarro-Herring, Norton, Garofalo...) cannot be determined. In addition, creep also plays a role on the hydrostatic part of the strain. This means that the deviatoric part obtained experimentally is not sufficient to estimate the full strain tensor. In either case, we believe that creep does not significantly impact the total deformation since accounting the plastic deformation could fit the experimental results for most of the Cu pads.

Plastic behaviour dependence on grain orientation

The average results presented in table 2.4 are schematically represented in figure 2.13. We observe a decrease in the yield strength for the Cu pads with low Young's modulus. This could be explained by the Schmid factor which decreases when tending to the [111] orientation, therefore leading to higher yield stress [117]. This explains why no plastic deformation is observed on Cu pads with E > 130 GPa. Previous experiments performed on single micrometric Cu crystals clearly evidenced a relation between orientation and yield strength with the [111] orientation having much higher values [118]. As for the stress exponent N, we can observe an increase with decreasing Young's modulus. These results clearly show that the plastic behaviour of each monocrystalline Cu pad is directly driven by its crystalline orientation. Therefore, in the following paragraph, we will study the total deformation dependence on the grain orientation which is key for interface closure during the hybrid bonding process.

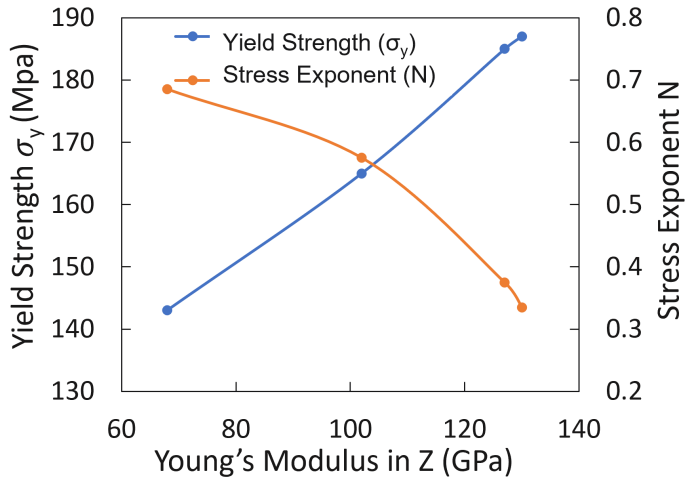

Figure 2.13: Average yield strength (σ_y) and stress exponent (N) as a function of the Young's modulus as found by the DoCE analysis for the 0.32 μm wide non-bonded Cu pads.

2.1.4.3 Extraction of the total deformation during annealing

Based on the agreement between the numerical and experimental results, one can rely on the numerical simulations to find the total deformation in the annealing step. The total displacement (hydrostatic + deviatoric) is computed by FEM simulations as shown in figure 2.14. It should be noted that these results are based on anisotropic-plastic behavior for Cu and does not account for creep. Therefore, the deformation for the two Cu pads possibly exhibiting creep (with E < 120 GPa) may be underestimated. A clear correlation exists between E and the total deformation where Cu pads with lower E exhibit larger deformation. Since the thermal expansion is independent of orientation in cubic systems, the difference in deformation along Z (out of plane direction) arises from the difference in deviatoric strain level that was found experimentally and confirmed by FEM simulations.

The results of figure 2.14 show that, depending on the orientation, a difference of 2 nm in displacement can be found for single 0.32 μm wide Cu pads that gives a total of 4 nm in bonding. At this level of Cu pad width, the 4 nm gap is significant. The specifications for Cu dishing should therefore be based on the [111] orientation (largest Young's modulus E and minimum deformation) to secure full interface closure after hybrid bonding.

2.1.5 Hybrid bonding demonstration with single metal level

To verify experimentally the findings of the theoretical dishing threshold detailed in section 2.1.4.3, a hybrid bonding demonstration is done with single metal level. The wafers are processed with the CPM6 mask that was presented in section 1.4.1 and composed of Cu matrices with HBM widths of 3, 2, 1, 0.5 and 0.3 μm and a pitch twice the HBM width. The process flow with a single metal level was detailed in section 1.4.1.

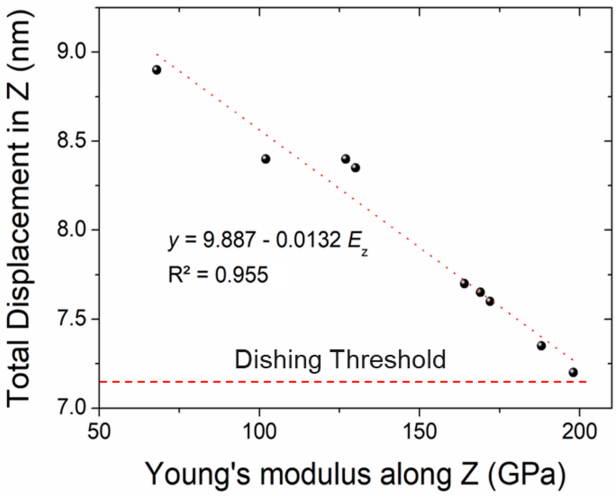

Figure 2.14: Total displacement in normal direction to the pad plane vs. Young's modulus as found by FEM simulations for the 0.32 μm wide non-bonded Cu pads.

After bonding and annealing at 380 °C for 2 hours, the scanning acoustic microscope (SAM) is used to check the presence of any bonding defects at the wafer level. A SAM example after bonding with the CPM6 test vehicle is shown in figure 2.15 (a).

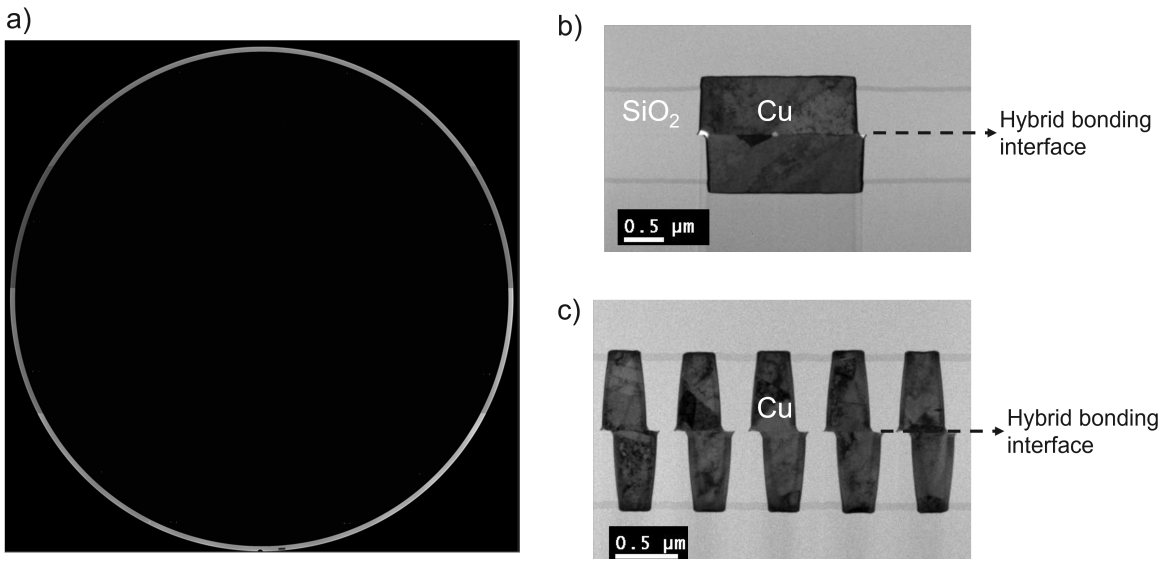

Figure 2.15: a) SAM image after bonding annealing of 300 mm wafer with the CPM6 single metal level test vehicle with pad width down to 0.3 μm. Cross section images by transmission electron microscope of bonded structure with b) 2 μm wide Cu pad and c) 0.3 μm Cu pads.

No bonding defect can be seen at the wafer level using SAM with a 50 μm resolution. TEM imaging is then performed on structures with different Cu pads width to check the interface closure after annealing. The results are shown in figure 2.15 (b) and (c) for the 2 μm and 0.3 μm wide Cu pads respectively. Whatever the Cu pad width, we observe good closure of the hybrid bonding interface. We conclude that on multipitch test vehicles, with Cu width down to 0.3 μm, the compliance with the dishing threshold for the smallest pad guarantees Cu-Cu connections for larger Cu pads.

2.1.6 Discussion

In this section, we have investigated the thermomechanical behaviour of individual Cu pads with the reduction of the pad size down to 0.32 μm using the Laue microdiffraction technique at the ESRF. We considered the hypothesis that the thermomechanical behaviour plays the major role and define the Cu-Cu interface closure mechanism with the reduction of the hybrid bonding pitch. Based on our studies, the following main discussions can be made:

- **Cu microstructure with size reduction:** with the reduction of Cu pad width from 3 μm down to 0.32 μm, and for the specific Cu deposition recipe used in our study, the number of Cu grain decreases from 9 on average for the 3 μm wide Cu pads down to single grain for the 0.32 μm Cu pads. Based on this result, we suspect the presence of a dominant grain for Cu pads with width below 1 μm. We believe that for further Cu pad width size reduction below 300 nm, a single grain presence is probable. These observations do not necessarily apply for Cu pads processed with different recipes. In fact, the Cu microstructure and grain size are highly driven by the Cu process conditions. For example, lower grain size can be obtained by the reduction of the post deposition annealing budget [119] [120]. Polycrystalline sub 1 μm Cu pads could be achieved by the use of fine-grain Cu [99]. Therefore, when studying the Cu thermomechanical behaviour, we should consider both the dependence on the grain size and number. Polycrystalline micrometric Cu pads do not necessarily behave as polycrystalline sub micron pads. In the following discussions, we will propose possible explanation based on the Cu grain size and number.

- **Cu microstructure with temperature:** based on our studies, we found that the Cu orientation does not change after annealing up to 400 °C, whatever the grain size. Possible Cu orientation control could be done at the deposition step to achieve lower variation in orientation. For instance, some studies in the literature reported processes that can achieve one dominant orientation (the [111] orientation in their case) [98] [99]. We also believe that aging tests, such thermal cycling and high temperature storage that are usually performed at temperature below 200 °C, should not have an impact on the Cu microstructure whatever the Cu pad and grain size. Previous study in the literature done on 4 μm polycrystalline Cu pads showed a small refinement of the grain structure after thermal aging tests and intergrowth of Cu grains at the interface after annealing above 300 °C [103]. No conclusion was made on grain orientation. The intergrowth above 300 °C reported in [103] could be related to the specific Cu recipe as compared to our present study.

- **Thermomechanical behaviour of polycrystalline Cu pads:** for 3 μm Cu pads with polycrystalline Cu grains, no clear conclusion could be made on the thermomechanical behaviour based only on the experimental findings. The experimental data were analyzed in terms of deviatoric strain and Young's modulus extraction. Complementary simulations are needed with microstructure modeling to get the full strain matrix (including the hydrostatic strain part) and to study the grain-grain interactions, which were not modeled during my PhD. Based on the experimental measurements done by Sart on micrometric Cu grains [22], we think that Cu bulk properties could be considered for polycrystalline micrometric Cu pads.

- **Thermomechanical behaviour of monocrystalline Cu pads:** for the 0.32 μm monocrystalline Cu pads, it is no longer correct to assume the Cu bulk properties. Based on the correlation between the numerical and experimental findings, the following main aspects should be considered:

  - Cu anisotropy should be added when simulating the thermomechanical behaviour of Cu pads with one dominant grain. The Young's modulus dependence on on orientation should be adapted. In fact, Cu is a very elastically anisotropic material (Zener ratio of 3.2). The Young's modulus in the [111] orientation is three times higher than along the [001] orientation. This dependence has direct consequences on the elastic behavior of the different pads.

  - For the integration studied with the 0.32 μm wide Cu pads, the plastic behaviour depends on the grain orientation. We found that grains with orientations close to [001] have lower yield strength, leading to higher plastic deformation at the annealing temperature as compared to grains with orientation close to [111]. This plastic deformation is a positive contributor to the hybrid bonding mechanism as it gives higher total strain for the same thermomechanical stress. The dependence between the grain orientation and the plastic behaviour is also existent for micrometric single crystals [118]. Hence, we believe that the elastic-plastic dependence on orientation should also be considered when studying micrometric Cu pads with a single dominant grain.

  - We believe that the model including the thermal expansion and elastic-plastic behaviour of Cu is the most adequate to describe Cu-Cu interface closure for the 0.32 μm wide Cu pads. In fact, for most of the Cu pads, no role of creep was seen when fitting the experimental findings with numerical simulations. Since the CTE of Cu down to 0.32 μm Cu width is believed to depend neither on the grain size nor on the grain orientation, it is therefore the elastic-plastic behaviour that is the main contributor to the Cu-Cu interface closure with reduction of the hybrid bonding pitch.

- **Preferred orientation for Cu-Cu interface closure:**

  - For the 0.32 μm monocrystalline Cu pads, we found that grains with orientation close to [001] favorize the hybrid bonding interface closure after annealing. The higher deformation for the [001] grain orientation is related to the impact of plastic deformation, which has a positive contribution to the total deformation under annealing. For our process, random monocrystalline grain orientation was found. Therefore, the dishing threshold should be set with respect to the grain with orientation of [111] that has the lowest deformation.

  - Some studies in the literature report that the [111] orientation could favorize the interface reconstruction after annealing since it is the orientation with high surface creep [98] [99]. However, the authors are not clear if this mechanical behaviour assists the interface closure or only to grain ¨diffusion¨ once the pads are in contact. The Cu creep role could be related to the specific Cu recipe used and to a possible impact of the size of the Cu pad studied which are at 8 μm.

- **Bonding mechanism down to 100 nm wide Cu pads:** with further pad size reduction down to 100 nm, the CTE is also expected not to vary from the bulk one [97]. A possible impact of creep should be studied since the creep rate is believed to increase with decreasing grain size [121] [122]. Depending on the stress state associated with Cu creep, this could have a positive contribution to Cu-Cu interface closure by leading to higher strain deformation. Future studies are needed to investigate if any role of Cu creep is present for Cu pads below 0.32 μm in width.

- **Bonding mechanism with Cu pads below 100 nm in width:** for Cu pad size below 100 nm, the bonding mechanism is more complicated as the CTE will be dependent on the grain size. Experimental and numerical studies report an expected increase in the CTE of Cu with the decreasing grain size [97] [123]. If validated for our specific recipe on sub 100 nm Cu pads, this will also have a positive contribution to Cu-Cu interface closure during the hybrid bonding process. We hence believe that, from a thermomechanical point of view, the achievement of the Cu-Cu interface closure even with Cu pads below 100 nm should not be a roadblock for pitch reduction.

2.1.7 Conclusion

In this section, we presented the thermomechanical behaviour study done using synchrotron based Laue microdiffraction measurements and FEM simulations. Several key finding for sub micron pitch achievement can be concluded based on these studies:

1. The grain number is directly driven by the width of Cu pad. Based on our findings and for the specific Cu recipe in our study, we expect to have a monoscrystalline or a single dominant grain for Cu pads with width below 1 μm. The grain orientation, on the other side, does not depend on the pad width and no dominant orientation neither an orientation evolution with temperature is expected for width down to 0.32 μm.

2. By combining FEM and the experimental findings, it is found that the monocrystalline grains inside the 0.32 μm Cu pads exhibit different plastic behaviors depending on the grain orientation. The Ludwick power law model was able to describe the plastic behaviour. The difference in the elasto-plastic behaviour between the different grains greatly impacts the total grain deformation expected during the annealing step.

3. We found that the Cu-Cu interface closure mechanism for the monocrystalline 0.32 μm wide Cu pads is dependent mainly on the elastic-plastic deformation. This is because the deformation based on CTE is not believed to change with grain size down to 0.1 μm and no major creep effect was identified when comparing the experimental behaviour with the numerical one for most of the pads. The dishing specifications should be set with respect to the grain having the lowest deformation. In this case, it is the grain with the orientation of [111].

The results of thermomechanical behaviour were used to demonstrate the feasibility of the hybrid bonding process with single metal level down to bonding with 0.3 μm wide Cu pads. This also serves as a reference for bonding on electrical test vehicles. In the

following section, we will discuss the electrical behaviour of the hybrid bonding level with the reduction of the pitch.

2.2 Electrical characterizations with pitch reduction

In section 2.1, we have studied the thermomechanical behaviour of single non-bonded Cu pads. This allowed to define the theoretical dishing threshold to guarantee Cu-Cu connections. The objective of this section is to understand the electrical behaviour of the hybrid bonding level with pitch reduction that is represented by the electrical resistance and capacitance. Furthermore, due to the critical impact of contact resistivity with pitch reduction, new test methods are explored to quantify low Cu-Cu contact resistivity at the hybrid bonding interface. The ultimate objective is to adapt the dishing threshold with pitch reduction found in section 2.1.4.3 to secure Cu-Cu electrical connections. The insulation properties of the dielectric could degrade with pitch reduction due to lower distance between adjacent pads. This will be verified in addition to any potential impact of pitch reduction on the electrical capacitance. The electrical resistance is studied on daisy chain structures with interconnection links ranging from 100 to 30k (see figure 1.8 (a)). The leakage current and capacitance variations are studied on comb-comb structures with 57k interconnections that were shown in figure 1.8 (b).

2.2.1 Electrical resistance

In this section, a focus is done on the electrical resistance behaviour with pitch reduction. A study on the key parameters that influence the resistance is first presented and discussed. Based on this study, we will study the contact resistivity with the aim of exploring new test structures and studying any correlation with dishing. We will then move to study the single interconnect resistance behaviour with pitch reduction and discuss the overlay limits that should be respected to guarantee a 100 % electrical yield in the sub micron pitch region.

2.2.1.1 Impact of process variations parameters

Since process parameters can vary between different locations on the wafer, the aim of this study is to define the key parameters that impact the electrical resistance with pitch reduction. The electrical resistance of a simple metal line is dependent on its geometry and on the material resistivity. Therefore, several material and geometric based parameters should be considered. To conclude on the geometric parameters to be studied, we will take as a reference the 1.44 μm pitch. A TEM cross section for the 1.44 μm reference pitch from the S&H test vehicle is shown in figure 2.16. The HBV and HBM have trapezoidal shapes. From a sensibility study, we found that HBM shape and thickness have a negligible impact on the electrical resistance in the range of variations found (below 1 %). Only the trapezoidal form of the HBV is considered for our study.

The complete list of parameters and ranges considered for the study is shown in table 2.5. For all the material and geometric based parameters, we kept the same ranges with pitch reduction. The variation range for Cu resistivity is extracted from 4-point measurements on samples with different thicknesses from 0.5 to 1.44 μm. The TaN/Ta resistivity is taken equal to the one reported by Jourdon [35] while assuming a ± 5 % variation. A $\pm$ 10% variation of the TaNTa theoretical 13 nm thickness is considered in the simulations. The trapezoidal form of the HBV (see figure 2.16) is considered in the simulations with the diameter D that is at the HBV/HBM intersection and α which is equal to d/D with d being the small diameter of intersection between HBV and the metal lines. The

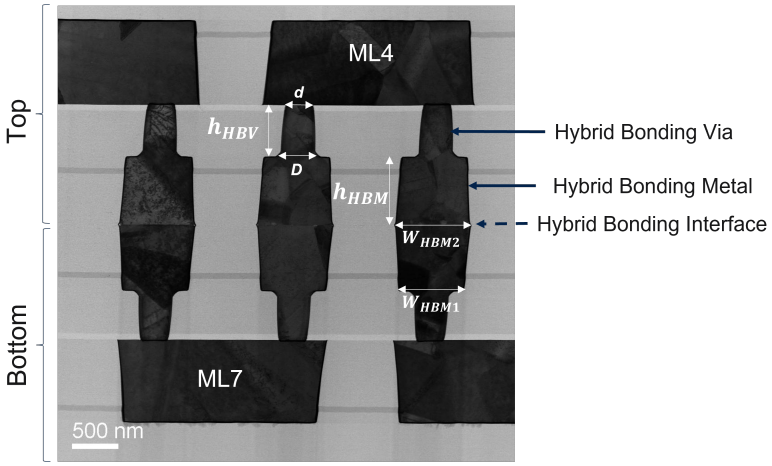

Figure 2.16: TEM cross section picture imaging of a daisy chain structure with 1 HBV per HBM with 1.44 μm hybrid bonding pitch from the S&H test vehicle.

variations of the HBV diameter are based on TEM cross sections at different locations inside the wafer and the range is defined based on scanning electron microscope (SEM) diameter measurements post etch. For the thickness, it is based on full map thickness measurements allowing to conclude on the range of variations. Moving to the contact resistivity, as no precise information is present for this variable, we have chosen a wide range between 10^{-11}-10^{-9} $\Omega.cm^2$ based on what has been reported in the literature [30]. The maximum overlay in X and Y directions varies depending on the studied pitch. The aim is to have the lowest contact surface area of 15 %, which is an arbitrary criterion, respected as a lower bound between the different studied hybrid bonding pitches. This leads to a maximum overlay of 450, 325, 270 and 245 nm for the 1.44, 1.08, 0.9 and 0.81 μm pitches respectively.

A DoCE is then conducted using the 9 factors previously defined. A mixed model of FC-CCD and LHS is modeled with 557 runs in total. COMSOL Multiphysics® is used to perform the FEM numerical simulations. Since the interconnects inside the DC are in series, only a single interconnect is modeled for the analysis and covers one top/bottom HBM and HBV along with half-length of metal lines 7 and 4 (ML7 and ML4) as shown by the red rectangle in figure 1.8 (a).

After running the FEM electrical simulations, the 2FI response model is selected which gives the best fit with an R^2 value higher than 98 %. The impact weight of each parameter is shown in figure 2.17. The presented values are used to assess the degree of importance for each parameter. The impact of the material and geometric based parameters on the electrical resistance is similar with hybrid bonding pitch reduction. As for the contact resistivity and overlay, these parameters are the most significant and their degrees of importance increase with hybrid bonding pitch reduction. This is related to the overlay limits set with respect to the 15 % criterion lower bound of contact area with HBM size reduction. For the 1.44 μm pitch, with the maximum overlay of 450 nm, the lowest contact surface is 0.0729 μm^2 as compared to 0.0256 μm^2 for 0.81 μm pitch even with lowest overlay of 245 nm. In addition, the contact resistivity is defined as the resistance of a unit area and expressed in equation 2.4 [29]:

Table 2.5: Input parameters of the DoCE for the electrical resistance analysis with pitch reduction.

Coded Factor	Parameter	unit	Minimum	Maximum
A	Copper resistivity	$\mu\Omega.cm$	1.81	2
B	TaN/Ta resistivity	$\mu\Omega.cm$	67.33	74.42
C	TaN/Ta thickness	nm	11.7	14.3
D	HBV diameter D	nm	340	380
E	alpha (d/D)	-	0.8	0.93
F	Via height (h_{HBV})	nm	530	570
G	Contact resistivity	$\Omega.cm^2$	10^{-11}	10^{-9}
H	Overlay X	nm	0	Variable
K	Overlay Y	nm	0	Variable

$$\rho_c = R_c A_c \tag{2.4}$$

where R_c is the resistance encountered by the electrical current when crossing the bonding interface. The contribution of R_c to the total structure electrical resistance increases with lower contact surfaces for a constant contact resistivity. This explains the increased degree of importance of ρ_c with decreasing pitch where the contact surfaces decrease.

The lower bound contact area criterion can be defined to get identical contact surfaces with HBM size reduction. However, this approach is unrealistic since it will lead to tight overlay ranges with pitch reduction. Instead, we think that the correct criterion to use is an identical overlay limits with pitch reduction, for instance corresponding the standard bonding tool performance of $\pm$200 nm. This is expected to lead to the same conclusion deduced from our study.

Based on the DoCE results presented in this section, we found that the HBV related parameters (d and α) have a high impact on the electrical resistance but constant with pitch reduction. This is because the HBV parameters do not change with size reduction. The material related parameters (Cu and TaN/Ta) as well as the HBV and TaN/Ta thickness variations have a negligible impact on the electrical resistance. The major impact on electrical resistance is attributed to both overlay and contact resistivity. Their corresponding impacts significantly increase with pitch reduction. These are the main parameters which are studied in the following sections.

Although the overlay parameter is driven by the bonding tool performance, the limits will be defined in section 2.2.1.3.3 with pitch reduction by defining several criteria. As for contact resistivity, that represents the electrical quality of the hybrid bonding interface, it should be precisely characterized. Hence, we will focus in section 2.2.1.2 on quantifying the contact resistivity by exploring new precise methods and studying any correlation

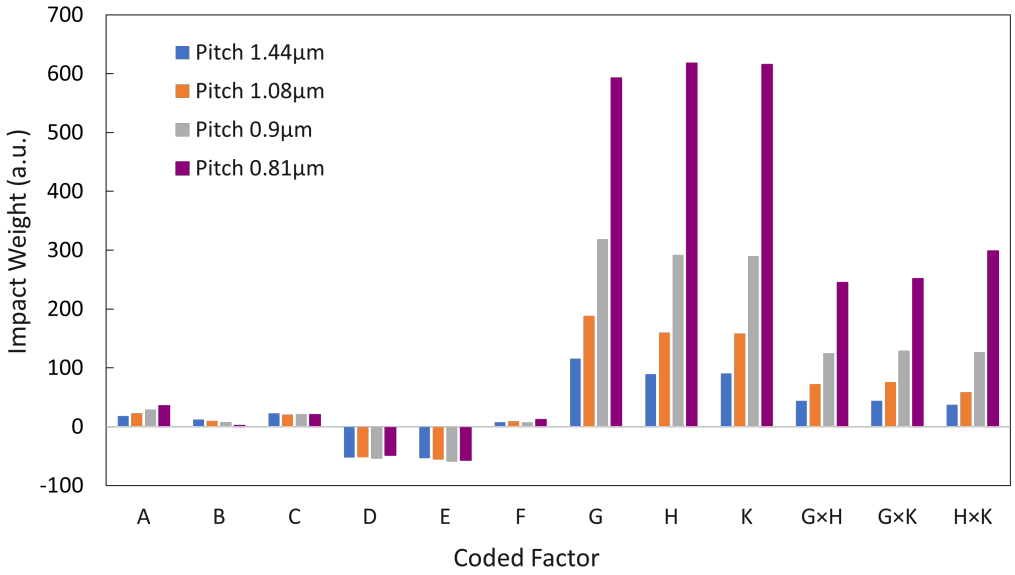

Figure 2.17: Impact weight of the most important parameters and their interactions on resistance for a single link interconnection with 1 HBV/1HBM for the 1.44, 1.08, 0.9 and 0.81 μm pitches.

with the dishing.

2.2.1.2 Contact reisitivity evaluation with pitch reduction

2.2.1.2.1 State of the art: methods and limitations

The contact resistivity is an active topic of investigation that has been well studied in the literature as it is an indication of the electrical quality of the Cu-Cu connections at the hybrid bonding interface [30] [35] [124]. During his PhD thesis, Taibi proposed a method to estimate the contact resisitivity for a hybrid bonding structure with a simple damascene process (two metal levels in total) by comparing the theoretical and experimental electrical resistances of a daisy chain. This method consists on decomposing the structure in elementary parts. The resistance of each element is calculated as a function of its dimensions and its material resistivity leading to the calculation of the theoretical resistance of the interconnection (R_{th}). The contact resistance is then found by subtracting the theoretical resistance from the experimental one (R_{exp}) as represented in equation 2.5 [30]:

$$R_c = R_{exp} - R_{th} \tag{2.5}$$

The contact resistivity can then be estimated using the contact area and the calculated contact resistance ($\rho_c = R_c \times A_c$). Based on this method, Taibi evidenced a contact resistivity that decreases from 1.4×10^{-9} to 2.25×10^{-10} $\Omega.cm^2$ when increasing the bonding annealing temperature from 200 °C to 400 °C [30] for a 3×3 μm^2 contact area.

This method was further studied by Jourdon for dual damascene hybrid bonding configurations, in which an HBV and HBM are used at the hybrid bonding level identical to the configuration studied in my PhD [35]. Jourdon showed that calculating the electrical resistance analytically leads to higher value than the experimental one, therefore

an inconclusive result on the contact resistance estimation. This is linked to the fact that interconnects are complex assemblies of various dimensions and materials. Simplifying them as a bundle of resistance sub-elements is not precise and affects the overall resistance. The author then used 3D FEM modeling to find the electrical resistance and found a closer but still a higher resistance than the experimental result. This was linked to the impact of process variations parameters on the FEM results (for instance, the HBV shape) and a perfect fit would require to exactly know the geometry of an interconnect. Therefore, this method is not suitable to study contact resistivity for interconnects containing several levels of metallization.

Jourdon followed these studies by exploring 3D cross kelvin resistor (CKR) structures adapted to the hybrid bonding configuration. These structures are only sensible if the contact resistivity is higher than 10^{-9} $\Omega.cm^2$. This corresponds to a density of bonding voids occupying more than 90 % of the Cu-Cu contact surface [35]. Chen also reported with CKR a Cu-Cu contact resistivity between 1.2-1.7 10^{-9} $\Omega.cm^2$ with Cu pad width ranging from 5 to 15 μm [124] that seems lie in the lowest precision of these structures. Therefore, we can conclude that no reported test structure is able to precisely quantify interface resistance with contact resistivity below 10^{-9} $\Omega.cm^2$. Until today, the 10^{-9} $\Omega.cm^2$ limit was sufficient for Cu-Cu electrical interface qualification since it was assumed negligible as compared to other elements such as the barrier resistivity. For instance, the TaN barrier resistivity is 100 higher than the Cu electrical one.

The precision limit of 10^{-9} $\Omega.cm^2$ is indeed critical with hybrid bonding pitch reduction. As shown in figure 2.18 and using the 10^{-9} $\Omega.cm^2$ precision limit, the lowest contact resistance than can be precisely estimated with pitch reduction increases that is related to the decreasing contact surface area between the top and bottom Cu pads. As an example, for the 1 μm pitch (HBM pad width of 500 nm), any contact resistance below 400 $m\Omega$ cannot be precisely quantified.

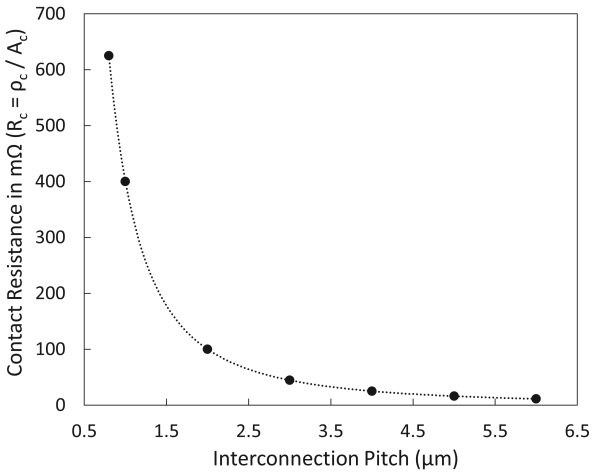

Figure 2.18: The lowest contact resistance that can be measured with pitch reduction using the 10^{-9} $\Omega.cm^2$ precision limit and with the assumption of full contact at the interface (no W2W overlay).

Hence, it is of much importance to explore new structures to quantify contact resistiv-

ity at the Cu-Cu interface below 10^{-9} $\Omega.cm^2$ as it has the main impact on the electrical resistance deduced from the DoCE study in section 2.2.1.1. In the following sections, we will discuss new structures developed during my PhD for precise estimation of low contact resistivity at the hybrid bonding interface.

2.2.1.2.2 Cross bridge kelvin resistor like structure

Structure description and precision limit

The cross bridge kelvin resistor (CBKR) structures have been widely used to characterize the metal-semiconductor contacts [125] [126]. An adaptation of the CBKR test structure to the HB integration is developed as shown in figure 2.19. The main particularity of this structure is that the sensing locations of the electric potential (V^+ and V^-) are directly on the HBM surface.

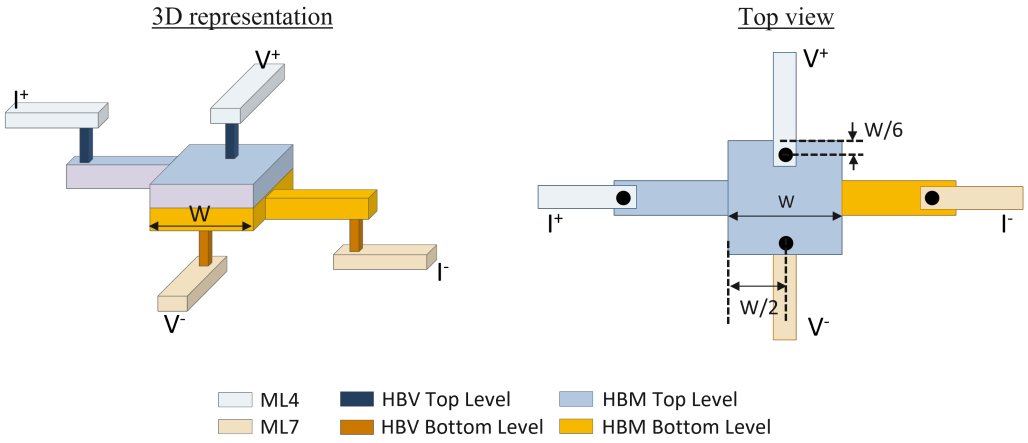

Figure 2.19: Schematic illustration of the cross bridge kelvin resistor like structure adapted to hybrid bonding.

A preliminary analysis using FEM allows us to make to following main conclusions:

- The precision limit is dependent on the V^+ and V^- sensing locations at the HBM surface as presented in appendix A.2. The highest precision is achieved when the sensing locations are in the middle of the HBM pads as presented in figure 2.19.
- The CBKR is not adapted to study Cu-Cu contact resistance at the hybrid bonding interface with an HBM width below 1 μm (appendix A.3). In fact, with decreasing HBM width, the precision limit decreases. Therefore, this structure is only designed in our TEDDY-UFP test vehicle with an HBM width down to 1.215 μm.
- The precision limit is dependent on overlay, and decreases when the overlay increases. Therefore, when studying the experimental results, only the structures with an overlay lower than ± 50 nm are considered.

For the optimized structure, FEM simulation is used to study the correlation between the imposed contact resistivity at the interface and the one calculated using the extracted potential difference as shown in figure 2.20 for the 2.16 μm wide pad width. We can clearly see that a good correlation exists down to the contact resistivity of 10^{-10} $\Omega.cm^2$. Below this limit, a deviation from the linear curve (calculated = imposed) starts occurring. Therefore, this structure allows to precisely estimate contact resistivity down to 10^{-10} $\Omega.cm^2$, which is one order of magnitude gain as compared to the 3D CKR [35].

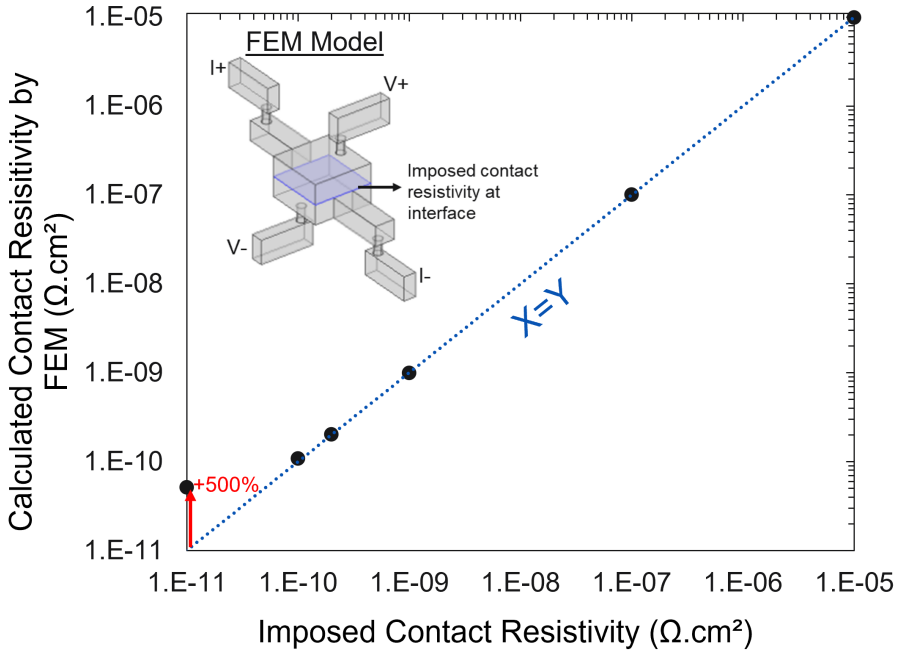

Figure 2.20: Correlation between imposed contact resistivity at the interface and the one calculated by FEM for the CBKR structure with 2.16 μm wide HBM.

As we need to quantify low contact resistance, careful attention is made to the applied electrical current so as to get the best compromise between the measurement errors and Joule heating. Issued from the study presented in Appendix A.1, an applied electrical current of 10 mA is used for the experimental measurements.

Experimental Results

The experimental results of contact resistances obtained by CBKRs are shown in figure 2.21 for the structures with different HBM width from 2.16 to 1.215 μm on the TEDDY-UFP test vehicle. The results clearly show that the detected contact resistance increases with decreasing HBM width. This structure is sensitive to the contact area in contrary to the CKR structures studied by Jourdon, which is mostly related to the higher precision limit of the CBKR structures [35].

The maximum and minimum contact resistivities with decreasing HBM width are calculated and shown in table 2.6. The estimated values are always below 10^{-10} $\Omega.cm^2$ whatever the HBM width. This is below the precision limit found for the CBKR. We can

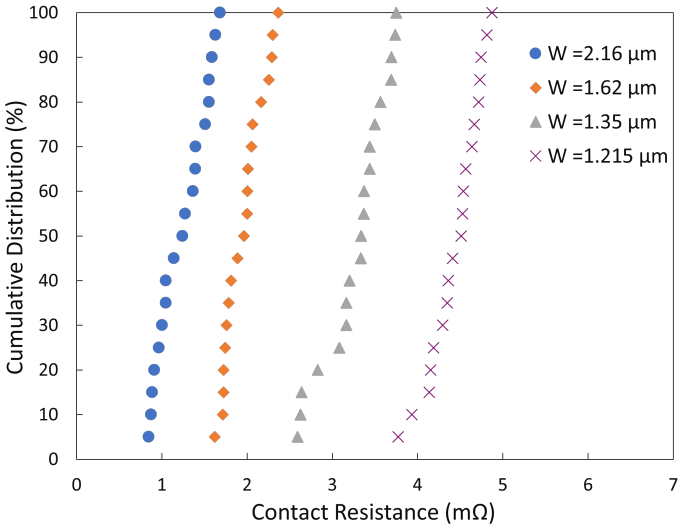

Figure 2.21: Cumulative distributions of the experimental contact resistance obtained by CBKR for the different HBM width on the TEDDY-UFP test vehicle.

conclude that in this study, whatever the HBM size width (from 2.16 to 1.215 μm), the contact resistivity at the interface is always below 10^{-10} $\Omega.cm^2$.

Table 2.6: The maximum and minimum contact resistivities using the CBKR structures extracted from figure 2.21 for the different HBM width.

HBM width W (μm)	Contact resistivity ($\Omega.cm^2$)	
	Minimum	Maximum
2.16	3.9×10^{-11}	7.8×10^{-11}
1.62	4.2×10^{-11}	6.2×10^{-11}
1.35	4.7×10^{-11}	6.8×10^{-11}
1.215	5.5×10^{-11}	7.1×10^{-11}

The CBKR design was studied as a potential new structure capable of detecting contact resistivity down to 10^{-10} $\Omega.cm^2$. Even though the new design allows one order of magnitude grain in precision with respect to the CKRs, it seems not be sufficient to detect the real contact resistivity since the measured results are below the detection limit.

2.2.1.2.3 Extraction of contact resistivity through numerical fitting of experimental resistances at varying contact surfaces

Structures and method description

The proposed methodology to quantify the contact resistivity at the interface is based on studying a new test structure to fit the experimental electrical resistance using FEM simulations. The additional requirement is the need of electrical resistance at different

contact area ratios. In fact, with decreasing contact surfaces between the top and bottom HBM pads, the impact of contact resistivity increases. It is therefore possible to extract the contact resistivity by studying numerically the electrical resistance deviation at reduced contact surfaces.

For the experimental data, specific structures are needed to apply this method as shown in figure 2.22. It consists of a daisy chain structure through the hybrid bonding interface with 100 links and where an imposed misalignment at the design is applied to control the contact area between the top and bottom pads. 4 structures are designed with 100, 50, 40 and 30 % theoretical contact areas between the top and bottom HBMs. The effective contact area that we will use to exploit the experimental resistances considers the W2W overlay induced at the bonding step. These structures are embedded in the TEDDY-UFP test vehicle and designed with the following 4 hybrid bonding pitches: 1.44, 1.08, 0.9 and 0.81 μm.

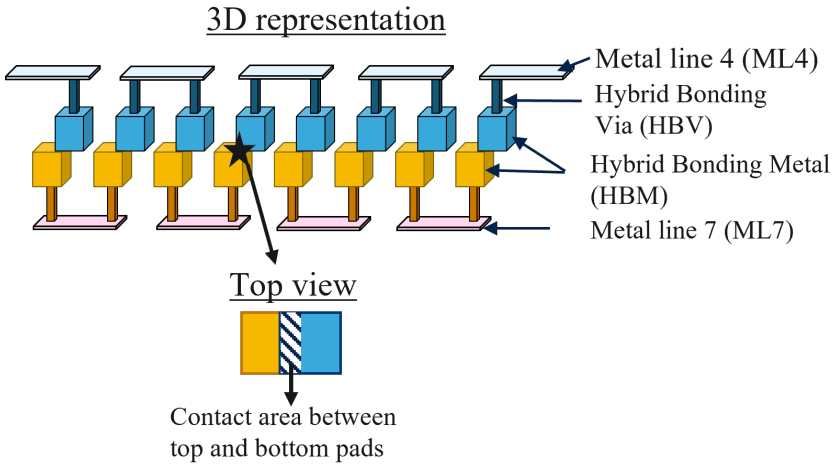

Figure 2.22: Schematic illustration of the daisy chain structure with misalignment used for the contact resistivity estimation. The contact area between the top and bottom pads is controlled.

The prediction model issued from the DoCE presented in section 2.2.1.1 is used to predict a set of geometric/material based parameters at a 100 % contact area. Many combinations of parameters could exist leading to the same experimental electrical resistance. Any combination could be selected to build the 3D numerical model of a single interconnection as no interaction was found between the contact resistivity and either of the geometric and material-based parameters (check figure 2.17).

The experimental results at the different contact areas are then fitted with the built numerical model while varying the contact resistivity at the HBM Cu-Cu contact. An illustration of the method for contact resistivity estimation is shown in figure 2.23 for the 720 nm wide HBM width (1.44 μm pitch). The contact resistivity at the Cu-Cu interface for this particular case is 5.10^{-11} $\Omega.cm^2$. The proposed methodology can precisely quantify contact resistivities down to 10^{-11} $\Omega.cm^2$.

This method is used in the following section to study any impact of dishing on contact resistivity while aiming to define the dishing limit with pitch reduction to get negligible

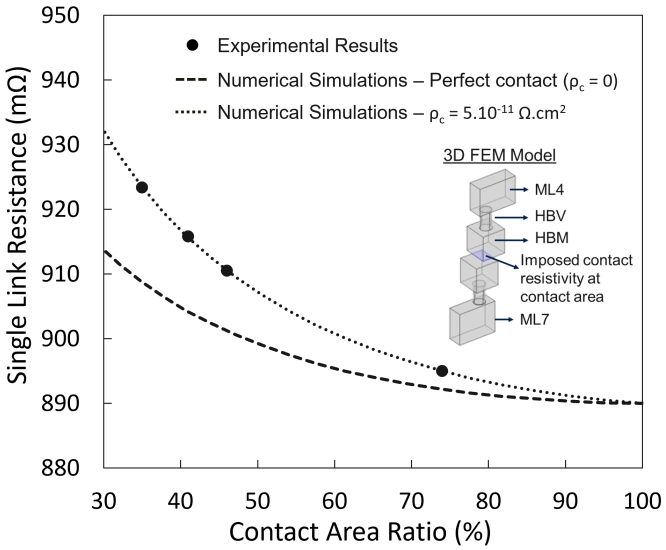

Figure 2.23: Illustration of the estimation method of contact resistivity at the Cu-Cu interface with HBM width of 720 nm (1.44 μm pitch).

contribution of contact resistivity.

2.2.1.3 Experimental results with pitch reduction

The objective of this section is to define the key parameters for 100 % electrical yield achievement in the sub-micron pitch region. The structures for study in this section were embedded in the TEDDY-UFP test vehicle with an equal spacing and HBM width. We will start by studying the dishing specifications that should be respected with decreasing pad width. A discussion on the overlay limits is then presented. Finally, we will study the experimental resistance behaviour of a single interconnect with pitch reduction.

2.2.1.3.1 Dishing specifications for electrical connections

To set the specifications of Cu dishing with pitch reduction, a set of wafers was processed with different levels of Cu dishing in the Cu HBM pads. After bonding annealing, SAM images are performed to check the appearance of any bonding voids at the wafer level. With dishing increase, no bonding defects appear by SAM with a resolution of 50 μm as shown in figure 2.24. Based on the study reported in the literature using GHz-SAM with a resolution of 1 μm [127], it is probable that the SAM technique in our case cannot identify bonding defects at Cu pad width down to 0.405 μm. Since no bonding defects were detected, the complete backside process was done on all wafers that allows us to verify experimentally the presence of Cu-Cu electrical connections with increased dishing.

The method described in section 2.2.1.2.3 is used to study any correlation between the dishing and contact resistivity on TEDDY-UFP test vehicle. The results are shown in figure 2.25. The average dishing values between the top and bottom pads found by atomic

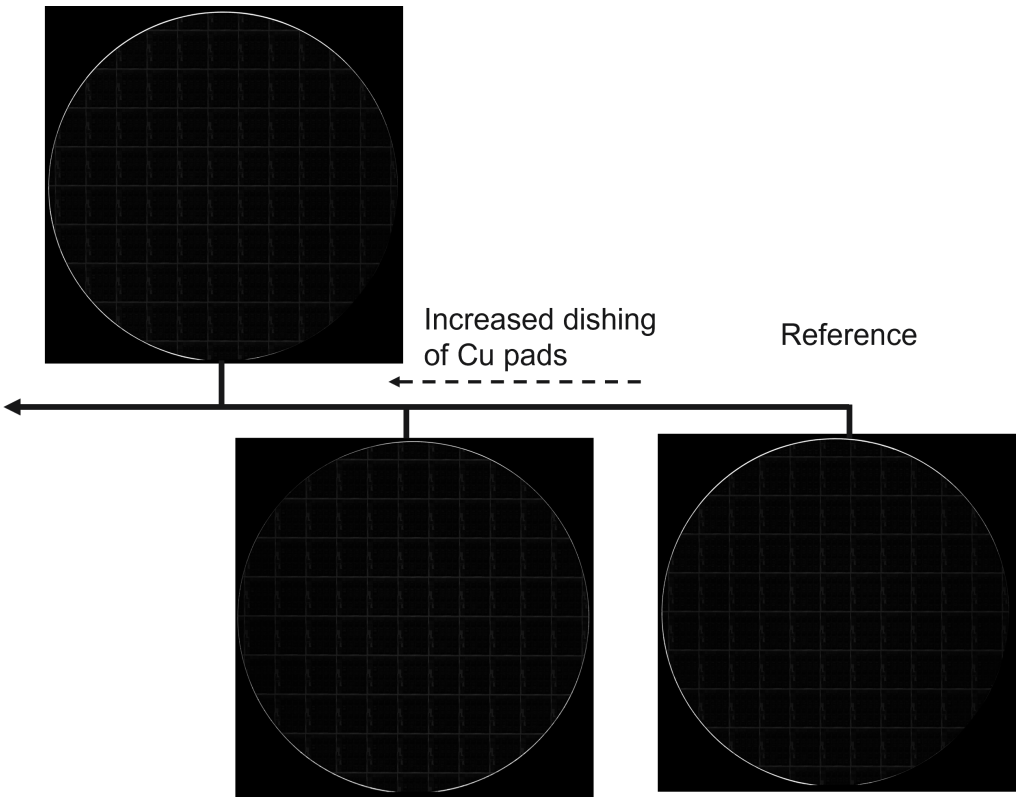

Figure 2.24: SAM results after bonding annealing at 380 °C - 2h with different levels of dishing induced at the Cu pad level for the TEDDY-UPF test vehicle.

force microscopy (AFM) measurements before bonding annealing at different specified locations inside the wafer are used for the correlation.

If we focus first on the 1.44 μm pitch, three regions could be identified depending on the dishing level:

1. A region below a dishing value where the contact resistivity is below 10^{-11} $\Omega.cm^2$. This corresponds to the precision limit of the method used in our study. Assuming that the lowest contact resistivity that can be achieved at the interface is the grain boundary resistivity, this was reported between 0.15 - 4 10^{-12} $\Omega.cm^2$ for the case of Cu grain boundary [128] [31]. Any contact resitivity below 10^{-11} $\Omega.cm^2$ signifies that the Cu-Cu interface reconstruction is close to the ideal case, which is driven by the Cu grain boundary resistivity and no more related to the impact of the hybrid bonding process such as voids.

2. A second region where the contact resistivity increases exponentially with increased dishing until reaching a value of 10^{-9} $\Omega.cm^2$. The origin of this exponential increase will be discussed later.

3. A region where no Cu-Cu electrical connections are established that is an indication of an open circuit. Above a certain dishing, the thermal expansion of Cu is not sufficient to close the Cu-Cu interface after thermal annealing leading to an open circuit. Based on this result, We can validate that a black SAM signal with a resolution higher than the Cu pad width does not necessarily imply the presence of Cu-Cu electrical connections, which can only be validated using electrical measurements.

These results clearly highlight a major impact of dishing on the Cu-Cu contact resistivity at the interface. Similar behaviors are observed with pitch reduction down to 0.81 μm as shown in figure 2.25. The following observations can be made:

- The slope of the exponential correlation between the contact resistivity and dishing increases from 5.82 to 7.27 for the 1.44 and 0.81 μm pitch respectively. For a given level of Cu dishing, higher contact resistivity is obtained with HBM size reduction.
- The dishing leading to open circuits decreases with HBM size reduction. Therefore, in a multipitch test vehicle, the dishing limit should be set with respect to the deformation of the lowest pad size.

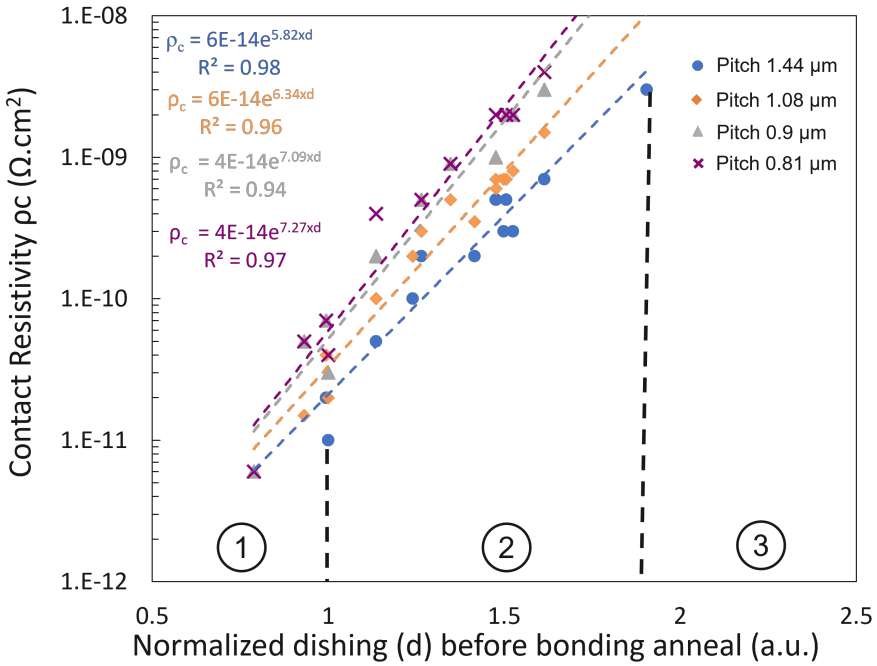

Figure 2.25: Contact resistivity vs. normalized dishing before bonding anneal for the structures with HBM width of 720 nm, 540, 450 and 405 nm (1.44, 1.08, 0.9 and 0.81 μm pitch respectively) on the TEDDY-UFP test vehicle. The dishing giving 10^{-11} $\Omega.cm^2$ for the 720 nm structure is used for normalization.

The contact resistivity is therefore dependent on the dishing level as well as the HBM size. The dishing threshold can be defined with respect to an acceptable contribution of contact resistance with respect to the total interconnect resistance. This depends on the requirements of each type of application and the resistance increase impact on the chip performance. For our case, and in order to secure excellent Cu-Cu connections, the dishing threshold is defined to get negligible contribution of contact resistivity (< 1 % impact on the electrical resistance for the 0.81 μm), i.e. to be in the region (1) of figure 2.25.

To understand the exponential relationship between the contact resistivity and dishing, we will rely on FEM simulations. Sart found by FEM that the gap lateral extent after annealing at a given temperature increases as a ¨ln¨ function of the dishing depth as shown in figure 2.26.

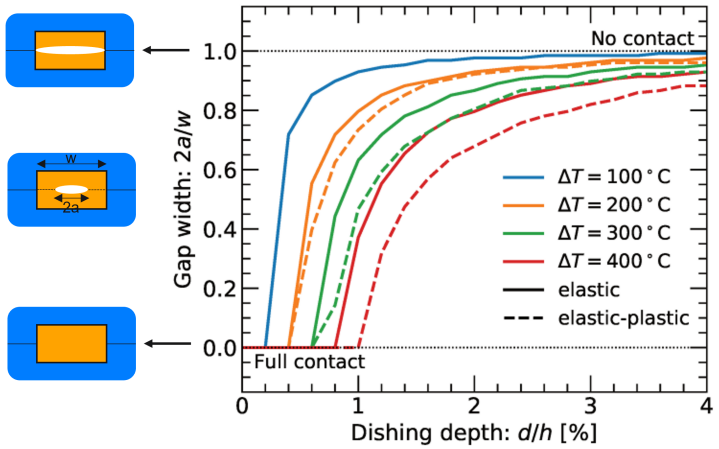

Figure 2.26: Computed gap lateral extent as a function of dishing depth for several temperature variations [22].

To study any correlation between the lateral gap after annealing and contact resistivity, we perform FEM electrical simulations using COMSOL. The model is presented in figure 2.27 (a) for the 1.44 μm pitch structure (720 nm wide HBM) by assuming a varying gap width of $2a$ at the Cu-Cu interface. The height of the gap is constant (20 nm) while varying the width. We use the same nomenclature used by Sart for consistency. The electrical resistance is computed with varying gap width between 10 and 710 nm. The contact resistivity is then deduced using the found electrical resistance increase. The result of contact resistivity as a function of the gap width is shown in 2.27 (b). An exponential correlation clearly exists between contact resistivity and the increasing gap width. The contact resistivity obtained just before open circuit is around 10^{-9} $\Omega.cm^2$ that is consistent with the experimental findings from figure 2.25. Based on the correlation found in figure 2.27 between the contact resistivity and the gap width, and the one reported in figure 2.26 between the dishing depth and the gap width, the exponential correlation found experimentally between the contact resistivity and dishing is validated. Based on these results, we therefore think that the increase in contact resistivity is due to the reduction of the effective bonding area after the annealing step. The decrease in the effective bonding area could originate from dispersed voids at the interface as studied by Jourdon [35] or from a localized gap after annealing as the hypothesis taken in our study. The same exponential correlation between the contact resistivity and the bonding void density is expected irrespective of the hypothesis used (localized or dispersed voids at the interface).

In the following sections, the electrical results based on the adapted dishing threshold for a contact resistivity below $10^{-}11$ $\Omega.cm^2$ are presented and discussed. We will focus on the overlay limit problematic as well as understanding the electrical resistance behaviour with pitch reduction.

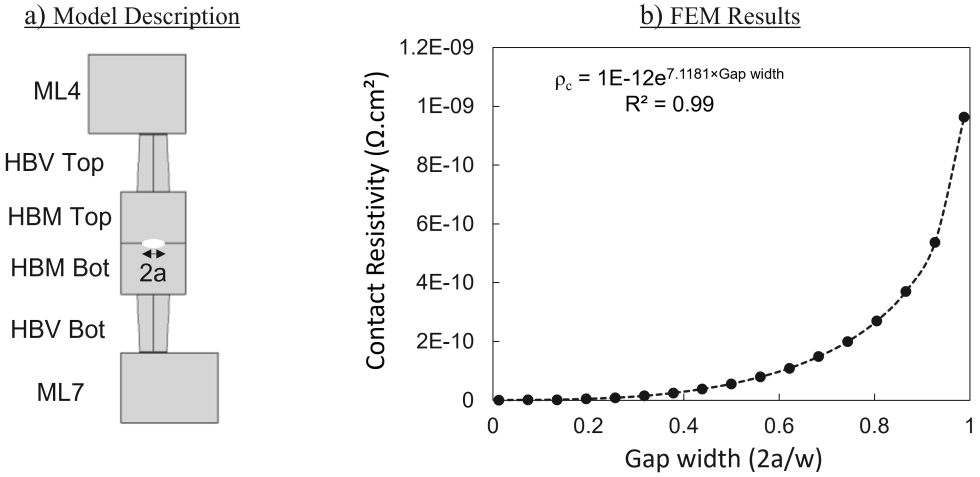

Figure 2.27: a) FEM model description with a gap at the interface and b) found contact resistivity using FEM as a function of $2a/w$ for the structure with 720 nm wide HBM Cu pads.

2.2.1.3.2 HB level characterization by TEM

Four pairs of wafers of the TEDDY-UFP test vehicle are processed while respecting the dishing specifications issued from the previous section to get a contribution of contact resistivity below $10^{-}11\ \Omega.cm^2$. The hybrid bonding level is characterized with pitch reduction by TEM analysis. The results are shown in figure 2.28. Whatever the pitch, we can highlight some voids present at the interface with width up to 20 nm (white arrows). These voids are regularly present at the Cu-Cu hybrid bonding interface and are attributed to the voids created by the dewetting of the Cu oxide present at the interface along the grain boundaries [64]. An important observation is that for pitch below 0.9 μm, the HBV and HBM have continuous shapes and they can no longer be differentiated. This observation validates our choice of the lowest pitch of 0.81 μm for the HBV/HBM configuration when the HBV size is kept constant. The hybrid bonding pitch around 0.8 μm is the pitch limit for the HBV/HBM configuration that is achieved by the reduction of the HBM size while maintaining a constant width of HBV.

2.2.1.3.3 Overlay limit definition with pitch reduction

An example of the W2W overlay mapping for wafer 04 of the TEDDY-UFP test vehicle is shown in figure 2.29. The misalignment is the sum of the translation, distortion, and scaling (run out) [37]. In our study and when calculating the contact surface between the top and bottom pads, the misalignment vector is decomposed into a misalignment in X (M_X) and Y (M_Y) directions.

The box plot results of M_X and M_Y for the set of the 4 wafers of the TEDDY-UFP test vehicle are shown in figure 2.30 (a) and (b) respectively. The misalignment vector that is defined as the $\sqrt{M_X^2 + M_Y^2}$ is also represented in figure 2.30 (c). In average, the misalignment vector is equal to 187, 112, 155 and 35 nm for wafers 01, 02, 03 and 04 respectively. The first three pairs of wafers were used for bonding recipe optimization. The results of wafer 04 correspond to the real capability of the bonding equipment where a W2W overlay below 150 nm can be obtained.

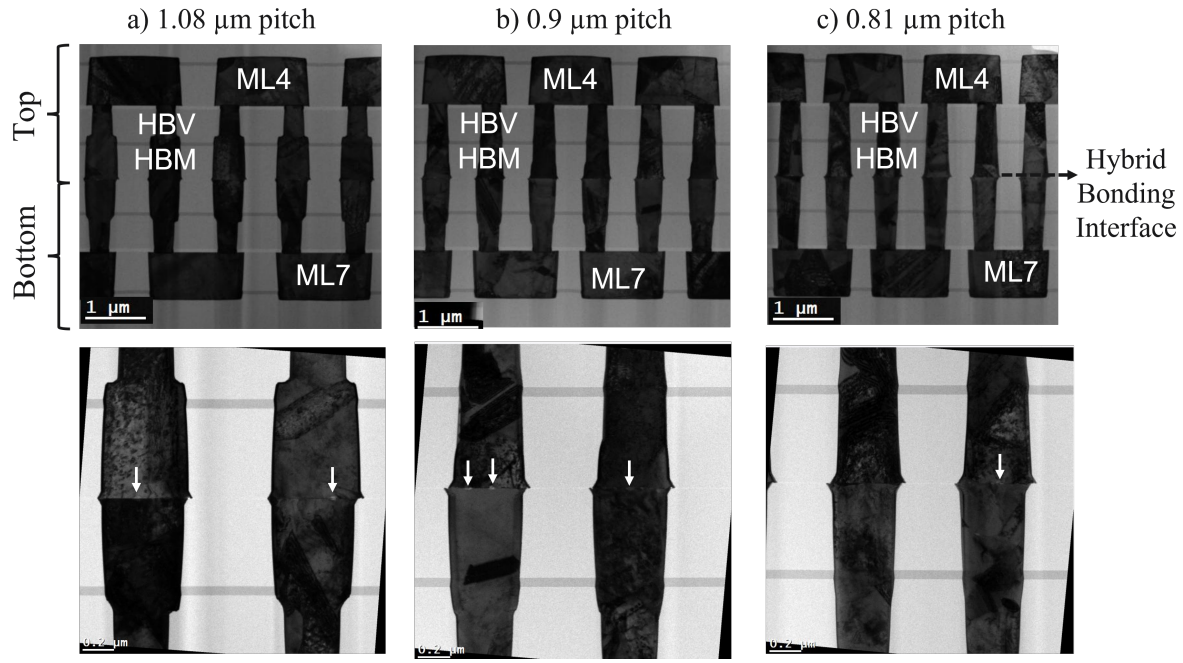

Figure 2.28: TEM cross sections imaging inside daisy chain structures with a) 1.08 μm, b) 0.9 μm and c) 0.81 μm hybrid bonding pitch on the TEDDY-UFP test vehicle. White arrows illustrate bonding voids at the interface.

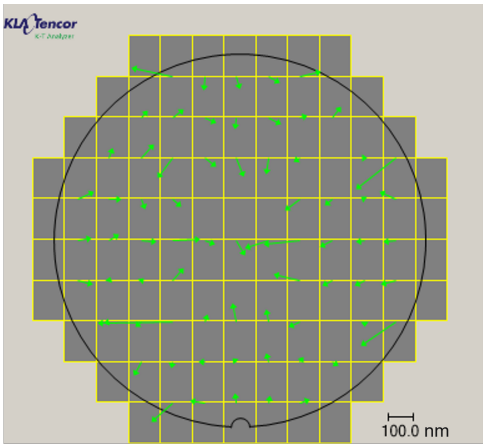

Figure 2.29: W2W overlay mapping for wafer 04 of TEDDY-UFP test vehicle. The green arrows represent the misalignment vectors based on IR measurements.

Using the electrical results of the wafer with the highest overlay up to 400 nm (wafer 01 in figure 2.30), the single link resistance of a DC with 5k interconnections is studied as a function of the contact area ratio for the different pitches as shown in figure 2.31.

From the general trend of the different distributions, we can see an increase in the electrical with decreasing contact area. However, it is not possible to establish a clear correlation between the contact area and the electrical resistance, since each electrical resistance result corresponds to a structure with its own combination of the geometric and material based parameters (for example HBV and HBM width and height...). Electrical failures are only observed for the lowest pitch (0.81 μm) when the contact area

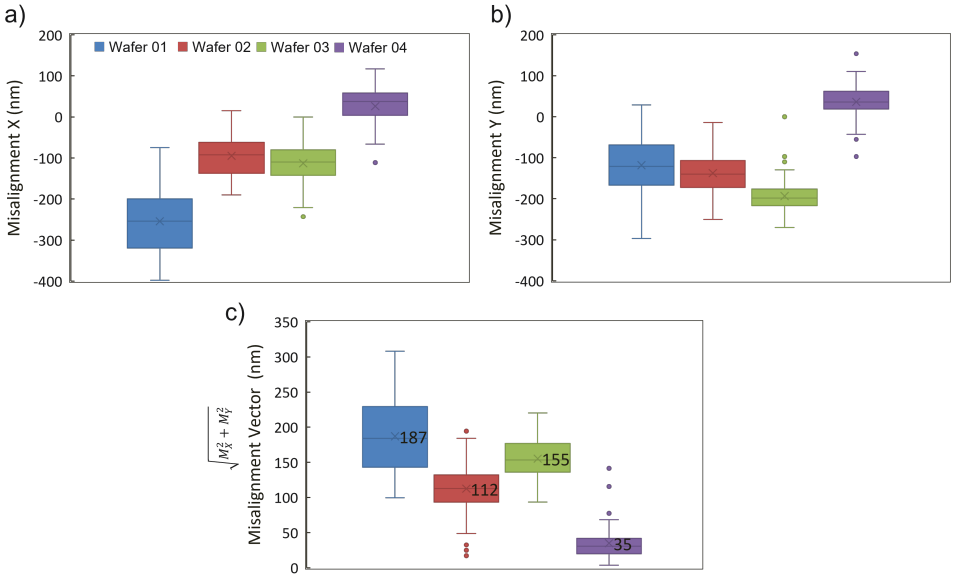

Figure 2.30: Box plots of a) misalignment in X b) misalignment in Y and c) misalignment vector $\left(\sqrt{M_X^2 + M_Y^2}\right)$ for a set of 4 wafers of TEDDY-UFP test vehicle. The average misalignment vector for each wafer is indicated in the box plots.

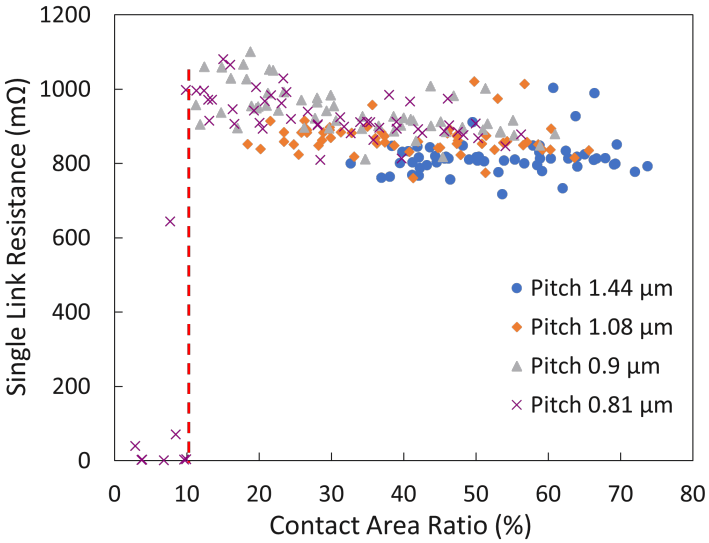

Figure 2.31: Single link resistance of a DC with 5k-links as a function of the contact area ratio for the different pitches inside the TEDDY-UFP test vehicle.

ratio between the top and bottom pads is below 10 %. Mostly, these electrical failures are characterized by a drop in the electrical resistance caused probably by a short circuit (detailed explanation will be given in the following paragraphs). A single open circuit is evidenced at a contact area ratio of 3.5 % for the 0.81 μm pitch (not presented in the figure 2.31).

For pitches above 1.44 μm, Jourdon defined the overlay limits when the contact area between the top and bottom pads is equal to the critical section of the HBV [34]. This hypothesis is studied by taking the theoretical diameter of the HBV (0.32 μm) and by calculating the contact area ratio between the HBV section and the HBM pads. This is

found to be at 15, 28, 40 and 50 % for the 1.44, 1.08, 0.9 and 0.81 μm pitch respectively. Based on the results of figure 2.31, this hypothesis is not valid since electrical resistance connections are well established for 1.08, 0.9 and 0.81 μm pitch way below their respective calculated critical area ratios.

The overlay limits are instead defined based on either of the following criteria:

1. An increase in the total interconnect resistance caused by overlay, which is set at an arbitrary value of 10 %.
2. The occurrence of electrical failures found experimentally in figure 2.31 that are only present for the 0.81 μm pitch.

Overlay limit based on electrical resistance increase

The response model from section 2.2.1.1 is used to define the overlay limits based on the criterion of 10 % increase in electrical resistance. The choice of the geometric/material based parameters does not impact our result since no interaction was found between overlay and these parameters (figure 2.17). The only important parameter is the contact resistivity that is first taken at 10^{-11} $\Omega.cm^2$ since the dishing was defined to get a negligible contribution of contact resistivity. The results of resistance increase as a function of the contact area are shown in figure 2.32. Using the defined 10 % criterion increase, the corresponding contact area can be extracted. The overlay limits for the different pitches are calculated and summarized in table 2.7. The overlay tolerance is ±450 nm for the 1.44 μm and decreases to ±205 nm for the 0.81 μm pitch.

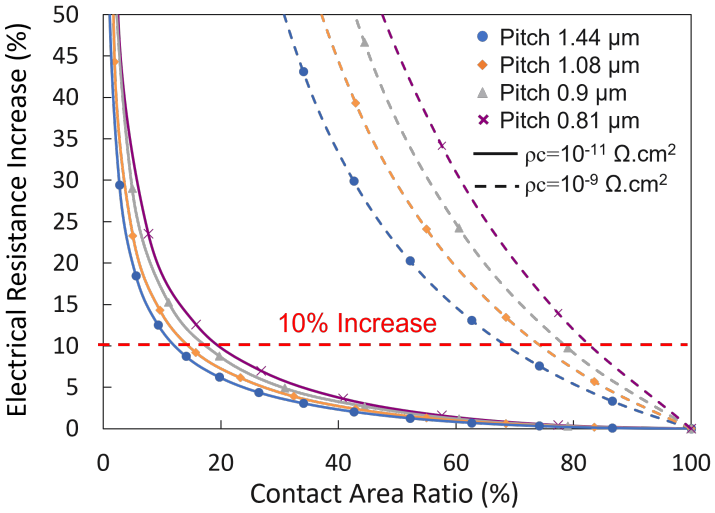

Figure 2.32: Resistance increase (%) as a function of the contact area ratio for the different pitches as found by FEM simulations assuming a contact resistivity of 10^{-11} $\Omega.cm^2$ (straight lines) and 10^{-9} $\Omega.cm^2$ (dotted lines).

Since the contact resistivity can vary depending on the dishing specifications, it is critical to study how the contact resistivity will influence the overlay limits. The DoCE response model is used while varying the contact resistivity. As shown in figure 2.33, to

Table 2.7: The overlay limits with pitch reduction as found by FEM simulations with respect to a 10 % increase of the interconnect resistance and a contact resistivity of 10^{-11} $\Omega.cm^2$.

Interconnect pitch (μm)	Overlay limit (nm)
1.44	± 450 nm
1.08	± 340 nm
0.91	± 240 nm
0.81	± 205 nm

keep with the 10 % increase criterion, the overlay limit decreases with increasing contact resistivity for a given pitch. Taking the contact resistivity of 10^{-9} $\Omega.cm^2$ (see figure 2.32, the overlay limit corresponding to a 10 % increase in interconnection resistance is only ±35 nm for the 0.81 μm pitch. This results evidences the importance of maintaining good Cu-Cu electrical connections by respecting the dishing specifications put in place to get negligible impact of contact resistivity.

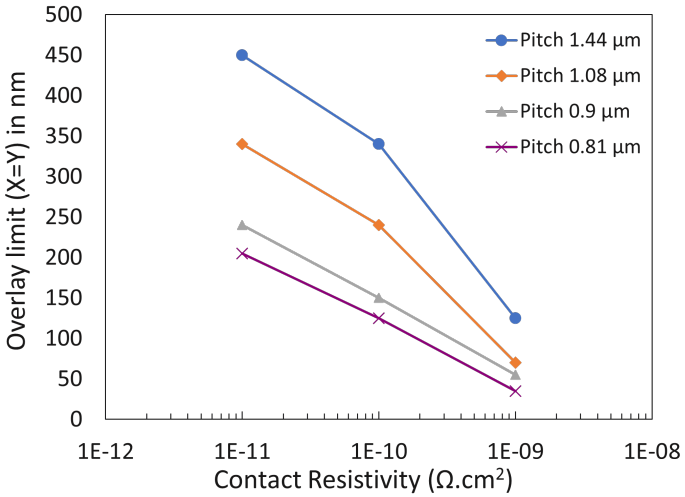

Figure 2.33: Overlay limit (X=Y) simulated with increasing contact resistivity at interface for the different hybrid bonding pitches. The 10 % increase criterion is used to define the limits.

Overlay limit based on electrical failure occurrence

To define the overlay limits based on the presence of electrical failures, one should understand first the origin of these failures. In figure 2.28 (c), we can see that the pad width at the hybrid bonding interface is larger than the theoretical one leading to lower spacing between adjacent HBM pads. When the overlay in one direction is higher that the spacing and lower than the HBM width, a contact could occur between adjacent pads. This might be the origin of the resistance drop and therefore short circuits observed for the 0.81 μm pitch. This hypothesis is studied using FEM simulations. Several interconnects should be modeled to simulate possible contact between adjacent pads. The pad width is taken at 440 nm that leaves a spacing of 370 nm between adjacent pads. The 3D and cross section representations of the FEM model are shown in figure 2.34.

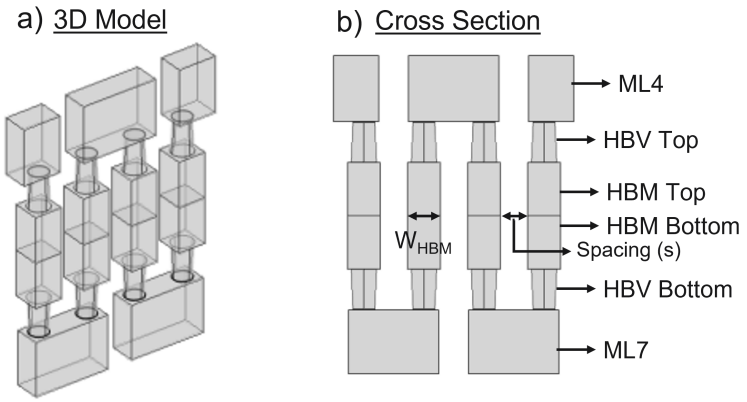

Figure 2.34: a) 3D and b) cross section representations of the FEM model used to study the electrical resistance failure for the 0.81 μm pitch.

Simulations are run by varying the overlay in one direction (in this example, X direction) between 0 and 440 nm. The electrical resistance results of the 4 interconnects are shown in figure 2.35 (a). The electrical resistance increases up to overlay of 360 nm as expected. When the overlay reaches 370 nm, the resistance drops by a factor of 2.3 and remains approximately constant until 440 nm above which open circuit is detected. The drop in resistance is linked to the connection between adjacent pads. The current will take short circuits as shown exemplary in figure 2.35 (b) for an overlay of 410 nm.

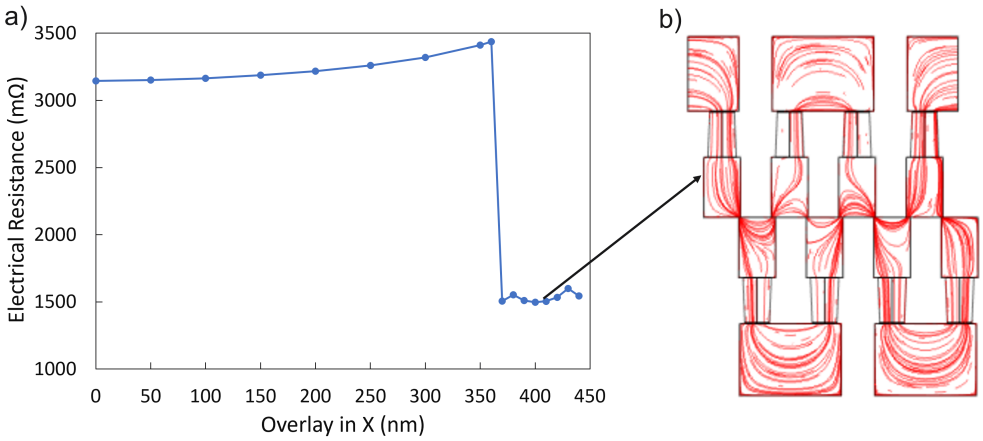

Figure 2.35: a) Electrical resistance variations with overlay in X for the structure with 4 interconnects and 0.81 μm pitch and b) cross section illustration of the current streamlines showing the short circuits when adjacent pads are connected.

This behaviour is verified by checking the overlay results of the structures in short circuits in figure 2.31 for the 0.81 μm pitch. This phenomenon starts occurring when the overlay in either direction exceeds 350 nm. The drop in resistance is higher than the predicted FEM simulations. This originates mostly that only 4 interconnects are modeled in FEM. Predicting the correct experimental resistance requires modeling the full structure (with 5k interconnections) that requires high simulation resources. We can validate

the hypothesis on the electrical failure origin that is induced by electrical shorts between adjacent HBMs at the interface. Defining the overlay limits based on the electrical failure occurrence and irrespective of the resistance increase leads a limit of ±350 nm for the 0.81 μm pitch. This limit is much more relaxed as compared to the one imposed by the 10 % resistance increase criterion for the same pitch level (±220 nm).

2.2.1.3.4 Electrical resistance with pitch reduction

The electrical resistance with pitch reduction is studied on daisy chain structures (see figure 1.8 (a)) with different link sizes from 100 to 30k interconnections. The cumulative distributions of a single link resistance for wafers 2, 3 and 4 are shown in figure 2.36. The single link resistance is simply obtained by dividing the total chain resistance by the total number of links. A 100 % yield is obtained down to 0.81 μm pitch with an overlay between ±250 nm.

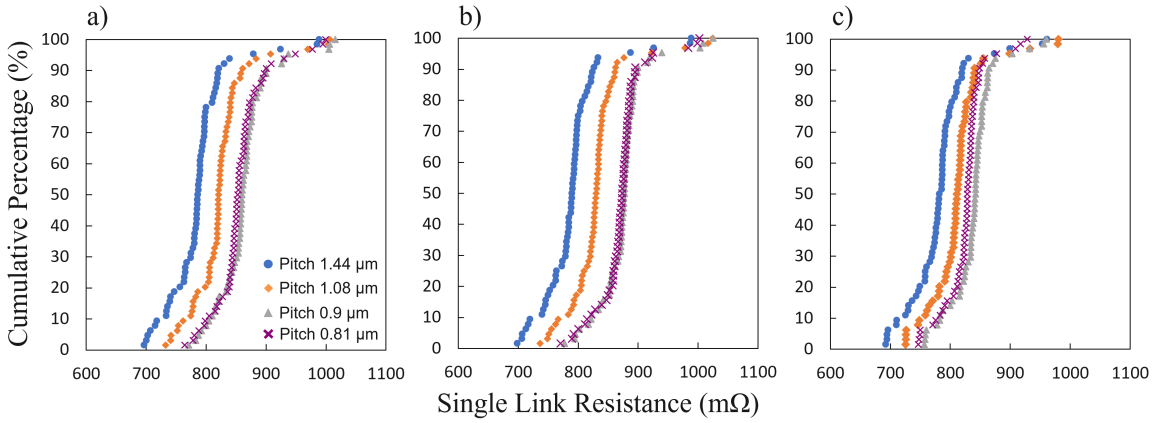

Figure 2.36: Cumulative percentage distributions of a single link resistance of a 5k-link daisy chain structure for the different pitches for a) wafer 02, b) wafer 03 and c) wafer 04 of the TEDDY-UFP test vehicle.

The mean experimental value with pitch reduction is calculated for the different wafers as shown in figure 2.37. We can observe higher variations of the mean value between the different wafers with pitch reduction. This is attributed in majority to the impact of overlay. With pitch reduction and for a given overlay, lower contact surfaces are obtained with decreasing HBM size and higher impact on the electrical resistance is expected. For instance, wafer 03 with the highest mean electrical resistance results has an average misalignment vector of 155 nm as compared to 35 nm for wafer 04 with the lowest electrical resistance results (figure 2.30 (c)). We can therefore conclude that the variations between the different wafers are in majority attributed to the impact of overlay.

The mean experimental resistance increases with pitch reduction down to 0.9 μm and then decreases for the 0.81 μm pitch, which is confirmed on the three studied wafers. To understand this behaviour, FEM simulations are performed. We will take for comparison the mean experimental values of wafer 04 (wafer with the lowest overlay) so that to keep

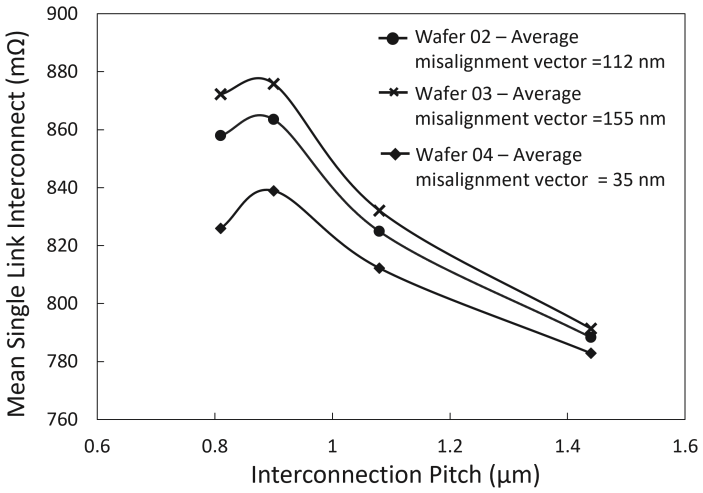

Figure 2.37: Mean experimental single link resistance with pitch reduction for the different wafers of TEDDY-UFP test vehicle.

the impact of overlay at its minimum. In the 3D models, we will first assume that the trapezoidal shape and size of the HBV do not change with pitch reduction. The diameter D is taken at 330 nm with an alpha (d/D) of 0.9 taken from TEM images. Based on full map thickness measurements, the mean experimental value is taken for the heights of HBV and HBM. The trapezoidal form of HBM is not considered and its width is issued from width HBM measurements post etch. The average overlay values of wafer 04 are also considered in the simulations that are found at 40 and 30 nm in X and Y directions respectively. The results are shown in figure 2.38 where a good correlation exists between simulations and experimental down to 0.9 μm pitch. For the 0.81 μm pitch, the predicted value is greater than the experimental one. From TEM cross sections (figure 2.28 (c)), we found that for the 0.81 μm pitch, the HBV and HBM have continuous shapes. This is then taken into consideration in our FEM by adjusting the 3D model. The diameter (d) of the HBV and the width of the HBM at the interface are kept constant and a conical shape is build containing a continuous HBV and HBM levels as illustrated in figure 2.38. By adjusting the 3D model, a closer numerical value to the experimental one is obtained. By accounting a continuous conical shape for HBV and HBM, the size of HBV is directly driven by the size of the HBM and no electrical current crowding takes place at the HBV/HBM intersection that could explain the decrease in resistance with respect to the reference 3D model. It might be pertinent for further pitch reduction to maintain a similar size of HBV/HBM to achieve good interconnect electrical resistance.

Now that the electrical resistance behaviour is pretty much understood and the limits are well defined, we will focus in the following sections on the insulation and capacitance aspects with pitch reduction.

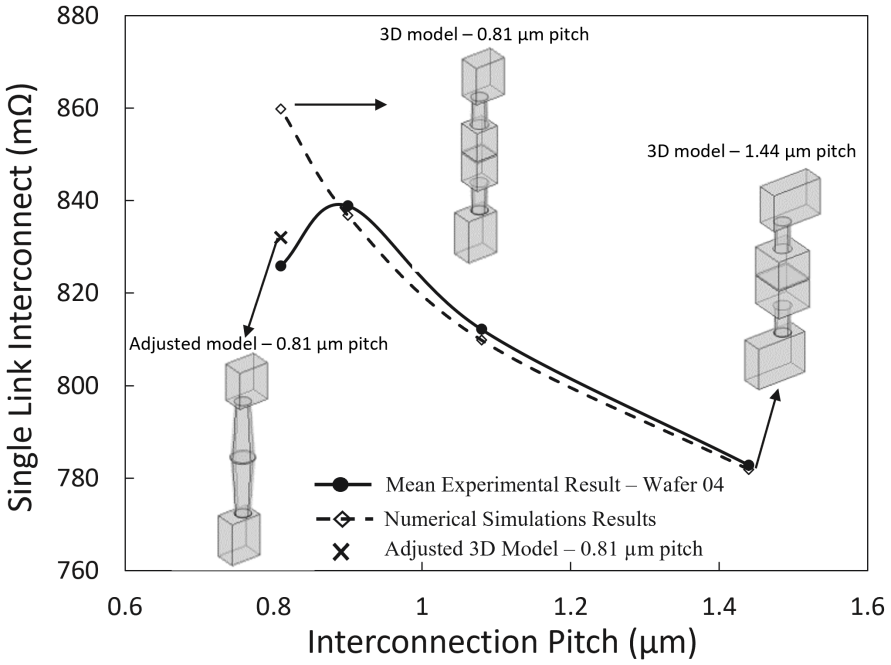

Figure 2.38: Comparison between the mean experimental value of wafer 04 and FEM simulations with pitch reduction of the TEDDY-UFP test vehicle.

2.2.2 Electrical insulation properties with pitch reduction

In order to verify the dielectric insulation properties with pitch reduction, parametric tests with a low potential difference of 3.3 V is applied between the top and bottom combs of the comb-comb structures with 57k interconnections (figure 1.8 (b)). The objective is to check the presence of any electrical shorts with pitch reduction.

The results are shown in figure 2.39 for the different pitches where the leakage current is plotted as a function of the calculated spacing between the 3D combs. This is found by subtracting the overlay from the theoretical/designed spacing (s). The leakage current is independent of the spacing and varies between 3 to 5×10^{-12} A whatever the pitch.

We can conclude that the interconnects remain insulated with pitch reduction down to 0.81 μm. In the next chapter, electrical characterizations are performed to study the dielectric behaviour under higher voltages until breakdown.

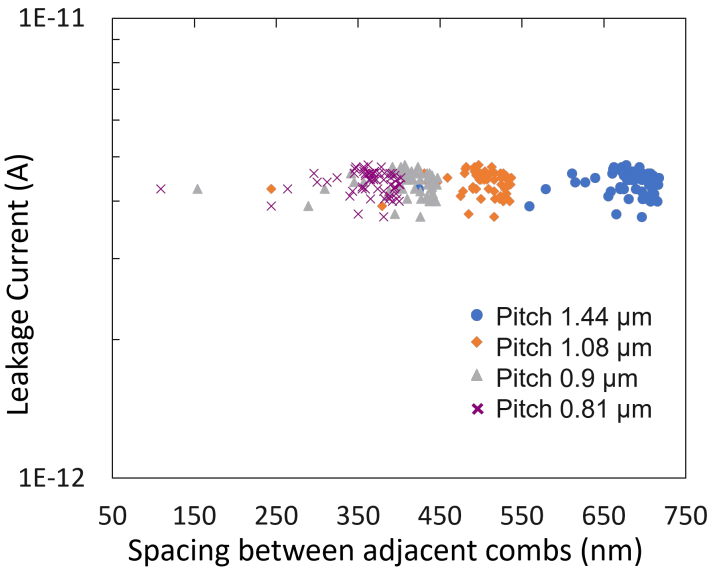

Figure 2.39: Leakage current as a function of the calculated spacing between adjacent combs for the 3D comb-combs structures with different hybrid bonding pitches of the TEDDY-UFP test vehicle.

2.2.3 Electrical capacitance

In this section, we will focus on the electrical capacitance behaviour with pitch reduction. The aim is to identify the important parameters that affect the capacitance when reducing the pitch and to study numerically the experimental behaviour.

2.2.3.1 Impact of process variations parameters

The simple capacitance of a dielectric between two metal lines is given by equation 2.6:

$$C = \epsilon \frac{Lt}{s} \tag{2.6}$$

where ϵ is the absolute permittivity of the dielectric, L and t are respectively the length and thickness of the metal line and s the spacing between metal lines.

By analyzing equation 2.6 and applying it to the case of hybrid bonded structure, the process variations of h_{HBM}, W_{HBM1}, W_{HBM2}, D, d, and h_{HBV} are identified for possible impact on the capacitance (figure 2.40 (b)). The distance s for our HB case is directly related to W2W overlay and width/form of the structure. The variation in absolute permittivity is assumed to be negligible. Capacitance estimation is obtained using silicon process modeling software that is SEMulator3D®. The 3D and cross section model representations are shown respectively in figure 2.40 (a) and (b). Since the structure is an arrangement of parallel capacitance, a comb-comb structure of 100 interconnections is modeled for simulation. The total structure capacitance can be estimated by multiplying the obtained result by a size factor to 57k interconnections. A sensitivity pre-analysis study allows us to conclude that the HBV's related parameters (D, d, h_{HBV}) have a negligible impact on the capacitance. Therefore, these will not be considered in the simulations.

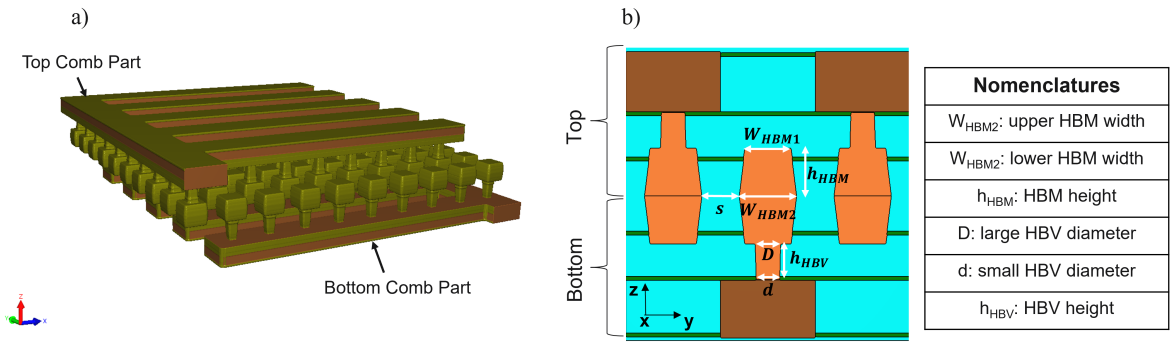

Figure 2.40: a) 3D model representation and b) cross section scheme of the comb-comb structure as seen in SEMulator3D® (Conventor). The nomenclature is also given.

To study the importance of remaining parameters on capacitance, a DoCE approach was adapted using Design-Expert® software. A mixed model of FC-CCD and LHS is created with a total number of 50 runs. The variation ranges for the entry parameters (list shown in table 2.8) were extracted from TEM images as well as post etch HBM width and thickness measurements. For this analysis, the limit is set at 250 nm for overlay-related parameters. We choose to study the structures with legs along the X directions leading that the structures are more sensible to overlay in Y.

Table 2.8: Input parameters for the design of computer experiments for capacitance analysis. Their variation ranges are given with respect to the mean experimental measurements.

Coded Factor	Parameter	Unit	Range
A	Pad width W_{HBM1}	nm	± 4 %
B	Pad width W_{HBM1}	nm	± 5 %
C	Pad height h_{HBM}	nm	± 5 %
D	Overlay X	nm	250
E	Overlay Y	nm	250

After running the simulations for the four pitches of 1.44, 1.08, 0.9 and 0.81 μm, a quadratic response model is selected that gives the best fit with an R^2 above 98 %. The relative impact of the different parameters on capacitance with pitch reduction is shown in figure 2.41. The highest relative impact from the 5 parameters is found to be the overlay in Y whatever the pitch. In addition, with pith reduction, its relative impact increases. This is mostly related to the reduced spacing between pads with lower pitch. The lowest impact on capacitance is the overlay in X due to the structure specific design that is more sensible to Y misalignment. All the parameter relative coefficients have positive values meaning that increasing them will give higher capacitance. This is consistent with the analysis of the simple capacitance equation 2.6. Moreover, we can observe a quadratic relation between capacitance and overlay Y as illustrated by the high relative impact of $E \times E$. All the other interactions have negligible effect.

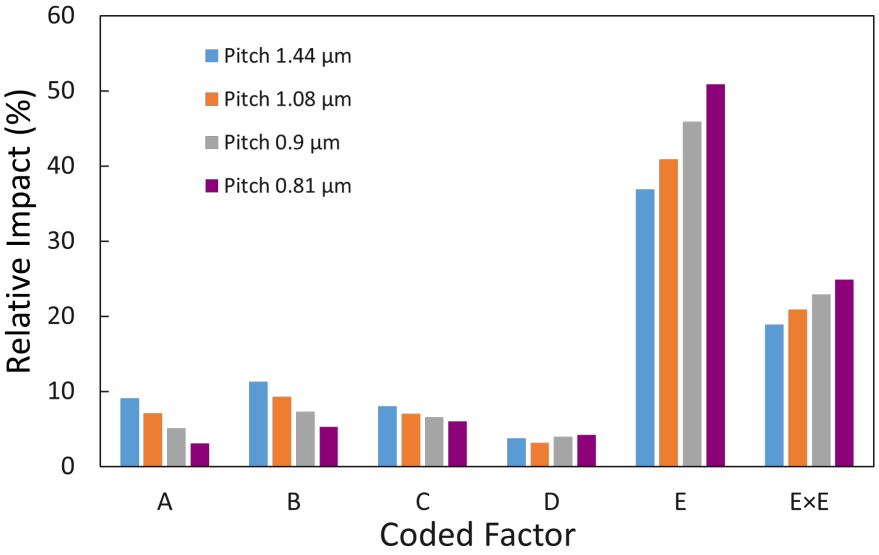

Figure 2.41: Relative impact of the most important parameters on the capacitance for the 1.44, 1.08, 0.9 and 0.81 μm pitches.

Based on the DoCE study presented in this section, we can conclude that with pitch reduction, all the factors that impact the spacing between adjacent pads (such as HBM shape, overlay) should be well controlled to reduce the capacitance variations. It is clear that the overlay, in the 250 nm range taken for the study, is the main factor that will impact the capacitance with pitch reduction. In the following section, we will focus on the experimental capacitance results, and we will study if our numerical model can explain well the experimental variations.

2.2.3.2 Experimental results with pitch reduction

To study experimentally the capacitance variations with pitch reduction, the comb-comb structures with 57k interconnections are used (figure 1.8 (b)). Since we kept the same interconnections number with pitch reduction, the capacitance per area is used for the study. The results are shown in figure 2.42 where the capacitance per area is plotted as a function of overlay in Y. To check if the numerical modeling matches the experimental results, the quadratic response from the DoCE study of each pitch (section 2.2.3.1) is used to plot the upper and lower limits of capacitance as a function of overlay in Y. The upper and lower limits are obtained by setting all the parameters at their extreme levels and calculating the response at a given Y overlay. It can be clearly seen that all the experimental values lie within the limits of numerical results for all the studied pitches. In addition, the general trend or curvature is also respected.

The mean experimental value is then compared with FEM simulations. We use wafer 04 that has the lowest overlay variations (average misalignment vector of 35 nm) so that to keep the impact of overlay at its minimum. The numerical simulations results are concluded from the prediction model of the DoCE study in section 2.2.3.1 by taking the average values of the different parameters and assuming no overlay. As shown in figure 2.43, the numerical simulations explains well the mean experimental increase trend. There is a small systematic gap (less than 3 %) between the experimental and simulations that is

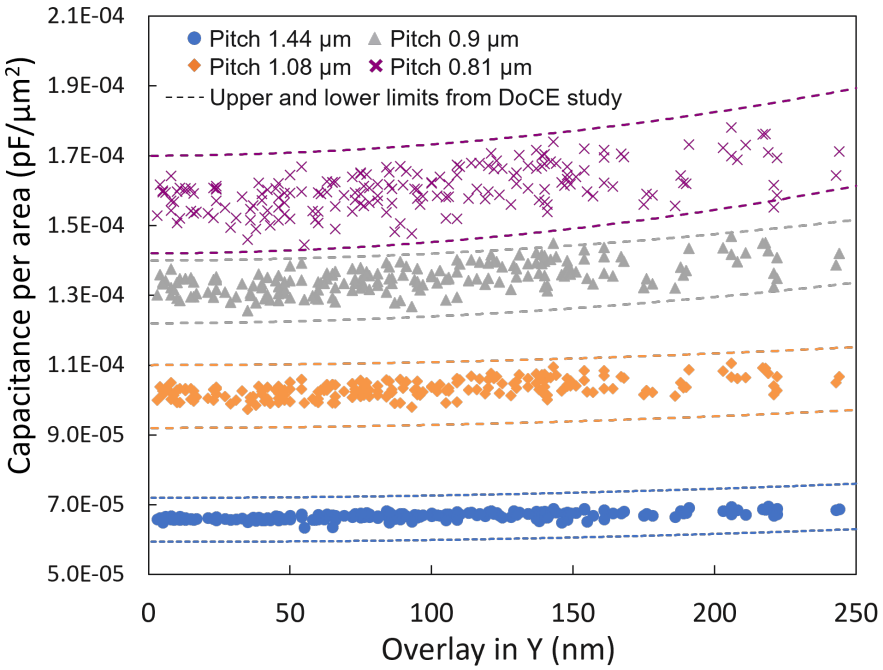

Figure 2.42: The capacitance per unit area as a function of overlay in Y for the comb-comb structures with different pitches on the TEDDY-UFP test vehicle. The dotted lines represent the upper and lower limits for each pitch as found by the DoCE study in section 2.2.3.1.

mostly related to the simplifications made for the 3D-model and the fact that no overlay was considered when predicting the numerical results.

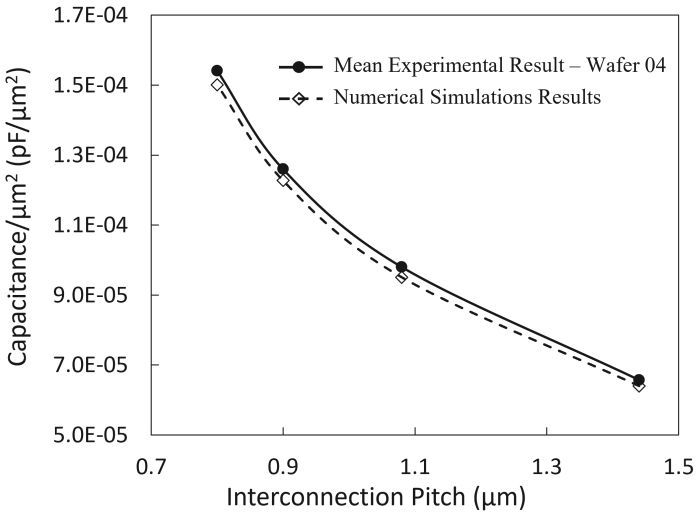

Figure 2.43: Comparison between the mean experimental and numerical simulation results of the capacitance/μm^2 for wafer 05 of the TEDDY-UFP test vehicle.

Based on the experimental results presented in this section, we expect more than 130 % increase in capacitance per area with pitch reduction from 1.44 to 0.81 μm when keeping the same configuration with HBV and HBM. The experimental increase in the capacitance per area is line with FEM simulations and is in majority due to the reduced

spacing between adjacent pads. In Chapter 4, we will focus on new configurations to achieve lower capacitance for a given pitch and which could be a solution to compensate the capacitance increase with pitch reduction.

2.2.4 Discussion

In this chapter, we have investigated the electrical behaviour of the hybrid bonding level with the reduction of the pitch down to 0.81 μm. The main objective was to study the pitch limit from an electrical point of view. Our studies focused on the electrical characterization of the hybrid bonding level and most importantly to the bonding interface through numerical and experimental investigations. The main following discussions can be made:

- **Pitch limit for our via+pad (HBV-HBM) configuration:**

  - For the studied HBV-HBM configuration, pitch reduction is achieved by shrinking the HBM size while keeping the HBV size constant. Based on our studies, we found that 0.81 μm is close to the pitch limit for our current configuration since HBV and HBM will have continuous shapes. Further pitch reduction would require the shrink of the HBV size thus increasing the total interconnect resistance because the HBV is the most resistive part of all the hybrid bonding elements. The strategy of having small HBV size is adapted by YMTC with an HBV size close to 100 nm (1 μm via pitch) [38]. In chapter 4, we will discuss designs to reduce the pitch below 0.81 μm by reducing the spacing between adjacent pads.

  - In the literature, pitch down to 1 μm with 100 % electrical yield has been well reported [75] [38] [77]. Hybrid bonding pitch of 0.7 μm is reported by IMEC, but with configurations having a pad only at the interface and a top pad smaller than the bottom one to achieve better insensitivity to overlay [25] [76]. However, with this design and below 1 μm pitch, around 10 % yield loss is seen that could be related to the impact of overlay.

- **W2W overlay specifications:** we found that the current standard bonding tool performance between ±200 nm is sufficient to achieve 100 % yield down to 0.81 μm pitch. This is true for our specific configuration with top and bottom HBM pads of identical dimensions. We think that the configuration with smaller top pads (reported by IMEC [76] and YMTC [38]) is not necessarily efficient for pitch below 1 μm when considering the actual standard bonding tool performance.

- **Key findings with pitch reduction:** based on a preliminary DoCE analysis, we found that contact resistivity has a major impact on the electrical resistance with pitch reduction, which was not the case for pad width above 3 μm. This parameter defines the electrical quality at the Cu-Cu interface.

  - **Method for contact resistivity characterization:** a new method for estimation of contact resistivity down to 10^{-11} $\Omega.cm^2$ was developed, which is based on experimental and numerical comparison of electrical resistances at different contact surfaces. This method allows two orders of magnitude gain in precision as compared to the conventional contact resistivity measurement methods such as 3D CKR [35].

- **Dishing threshold with pitch reduction:** When fitting the total deformation obtained from the thermomechanical study of the 0.32 μm wide pad (orientation [111]) with the dishing limits from the electrical study (not shown hereafter), we can conclude that the dishing limit based on the thermomechanical behaviour is equal to the limit for open circuit. This implies that the thermomechanical analysis solely does not guarantee the establishment of Cu-Cu connections. The dishing limit should be refined based on the electrical study, which is discussed in the following paragraph.

- **Impact of dishing on contact resistivity:** we found that the dishing before bonding annealing has a major impact on the contact resistivity at the Cu-Cu interface. Above a certain dishing, an exponential increase of contact resistivity is expected until an open circuit occurs. We believe that the origin of this exponential increase is related to a decreased effective bonding area after the annealing step. For polycrystalline Cu pads, the reduced effective bonding area is due to dispersed voids along the hybrid bonding interface [35]. For sub micron Cu pads, where a single dominant grain is expected, we think that the decrease in the contact area is due to a localized non bonded area like the hypothesis of a gap after annealing proposed by Sart [22]. However, we believe that the localized non bonded area will mostly be at the edges of the HBM pads. This is because it is the area with lowest deformation due to contact with the TaTaN barrier, which has much lower CTE than Cu [24].

- **Contact resistivity criterion with pitch reduction:**

  - The 10^{-9} $\Omega.cm^2$ contact resistivity criterion that was used as an indication of excellent electrical quality at the interface for pads with width larger than 3 μm [129] [130] could no longer be the criterion for sub 1 μm Cu pads. Taking the example of the 0.405 μm wide Cu pads (0.81 μm pitch), we found that the average interconnect resistance with a perfect contact is 825 $m\Omega$. The 10^{-9} $\Omega.cm^2$ contact resistivity means 600 $m\Omega$ as additional contact resistance which is an increase by more than 70 % of the total interconnect resistance. For the 3 μm wide Cu pads, the 10^{-9} $\Omega.cm^2$ contact resistivity was only 11 $m\Omega$ in contact resistance.

  - We highly recommend that for sub micron Cu pads, the contact resistivity criterion should be set at 10^{-11} $\Omega.cm^2$. For the 0.81 μm pitch, this corresponds to a contact resistance below 6 $m\Omega$ that is less than 1 % of the total interconnect resistance. The respect of this criterion guarantees a Cu-Cu interface that is perfectly reconstructed and a contact resistivity close to the Cu grain boundary one. Since the contact resistivity depends on the HBM width, the dishing threshold should be defined with respect to lowest Cu pad size on a multipitch test vehicle, which guarantees excellent electrical connections for all the range of pad sizes. Further pitch reduction with Cu pads below 0.405 μm in width requires adjusting the contact resistivity criterion by studying the dependence between the dishing and contact resistivity.

- **Electrical resistance with pitch reduction:**

  - An increase in the total interconnect resistance by 7% was found with decreasing pitch from 1.44 down to 0.9 μm which is related to the shrink of pad size.

For the hybrid bonding pitch of 0.81 μm, with a continuous HBV and HBM shapes, a decrease in the interconnect resistance was detected experimentally which could be related to lower current crowding at the HBV-HBM intersections. For further pitch reduction below 0.81 μm, configurations with continuous HBV and HBM shapes could be adapted.

- Pitch reduction below 0.81 μm will eventually require to reduce the thickness of the hybrid bonding level to have lower aspect ratio. Important parameter that should be considered when reducing the thickness is Cu resistivity. This parameter is believed to increase but only below 200 nm of Cu thickness [131].

- **Electrical capacitance with pitch reduction:** the capacitance per unit area increases significantly by more than 130 % with pitch reduction from 1.44 down to 0.81 μm, while keeping the same HBV-HBM configuration. This increase is mainly related to the decreased spacing between adjacent Cu pads. With further pitch reduction keeping the same configuration, a significant increase is expected as an inverse function of the spacing. Possible solutions could be summarized as following:

  - The use of dielectrics at the interface with lower k constants than the SiO_2 (k=3.9). Adapting this solution could possibly change the bonding mechanism, which may justify that hybrid bonding configuration with low-k dielectric is not strongly studied until today.

  - The geometric parameter adaptation at the hybrid bonding level that includes decreasing the thickness and/or increasing the spacing between HBM pads for the same pitch level. This solution will be explored in this thesis.

Taking into consideration the latest overlay developments with a precision of ± 50 nm [132], we believe that further pitch reduction down to 200 nm (100 nm wide Cu pads) is possible from an electric point of view, as long as the dishing is adapted to get good Cu-Cu electrical connections at the interface.

2.2.5 Conclusion

In this section, the electrical behaviour of the hybrid bonding level was characterized and understood with pitch reduction from 1.44 down to 0.81 μm. We were able to develop new methods capable of quantifying contact resistivity with at least two orders of magnitude gain in precision with respect to the state of the art methods. Several key parameters should be respected that are crucial to obtain electrical connections with pitch reduction.

1. For the electrical resistance, the contact resistivity and overlay are the parameters with the highest impact with pitch reduction. By adapting the dishing threshold with respect to the lowest Cu pad size, negligible impact of contact resistivity can be secured. As for overlay, even for the 0.81 μm pitch, the ± 350 nm limits are sufficient to achieve 100 % yield. The overlay limits should be defined based on an acceptable increase of the interconnect resistance, depending on each product specification.

2. For the electrical capacitance, the overlay parameter has the major impact with pitch reduction. The overlay limits, as for the case of the electrical resistance, can be defined with respect to an acceptable increase of the capacitance based on using the DoCE model. Pitch reduction while keeping the HBV/HBM configuration leads to capacitance increases as validated both experimentally and by simulations.

Issued from this section, we confirm an increase of the interconnect RC delay with pitch reduction mainly due to the capacitance increase. Depending on the type of application and each product specifications, this RC interconnect could impact the overall performance and can be seen as a roadblock for pitch reduction adaptation. Possible solutions could be envisaged to reduce the RC interconnect delay by simply reducing the hybrid bonding stack thickness.

2.3 Chapter 2 conclusion

In this chapter, we investigated into the thermomechanical and electrical behaviors of the hybrid bonding level with the reduction of the Cu pad size width down 0.32 μm. The objective being to define any pitch limit for successful Cu-Cu interface closure from the thermomechanical and electrical point of views. The following key conclusions can be made:

- When bonding with sub-micron Cu pads down to 0.32 μm, the Cu-Cu interface closure depends mainly on the elastic-plastic behaviour of Cu. When studying the thermomechanical behaviour, the plastic properties dependence on Cu orientation should be considered for Cu pads with a single or dominant grain. Grains with orientation close to [001] favorize the Cu-Cu interface closure by exhibiting higher total deformation when annealing mainly due to the plastic part of the deformation. The dishing threshold, on the other side, should be defined with respect to the Cu grains with orientation [111], having the lowest total deformation. We believe that Cu-Cu interface closure from a thermomechanical point of view is still possible down to at least bonding with 100 nm wide Cu pads.

- The dishing threshold defined from the thermomechanical study based on the total deformation under annealing corresponds to the dishing threshold for electrical open circuit. The dishing threshold should be refined with respect to a specific criterion of contact resistivity adapted to each product specifications. Dishing adaption with respect to a contact resistivity criterion of 10^{-11} $\Omega.cm^2$ guarantees negligible impact on the total interconnect resistance down to 0.81 μm pitch. On a multipitch test vehicle, to achieve high electrical yield, the dishing specifications should be set based on the contact resistivity criterion for the lowest Cu pad size.

- The current standard bonding tool performance ($\pm$200 nm) is sufficient to achieve 100 % electric yield down to 0.81 μm. The overlay limits could be set according to an acceptable increase in either the electrical resistance or capacitance according to the specifications of each product/application. From the electrical behaviour perspective and with the latest overlay development in W2W bonding down to $\pm$50 nm [132], hybrid bonding pitch reduction down to 200 nm is possible, if the dishing threshold could be controlled to get negligible contact resistivity at the Cu-Cu interface.

Depending on the type of application, a potential roadblock to further reduce and adapt sub-micron hybrid bonding pitches is the increased RC interconnect delay. Even though adapting hybrid bonding configurations with continuous HBV and HBM shapes could be beneficial from the electrical resistance side, this is believed to have little impact on the electrical performance as no gain is expected to the capacitance that is the main RC contributor. In chapter 4, we will study new hybrid bonding configurations that could solve this problematic and can achieve a better performance for a given pitch.

Chapter 3

Cu/SiO_2 Hybrid Bonding Level Reliability with Pitch Reduction

To begin with this third chapter, and before discussing the main reliability risks at the hybrid bonding level, it is crucial to clarify the signification of several important words to avoid misunderstanding about the results that will be presented in this chapter. For instance, what is the difference between reliability and robustness? On one side, and by definition, the reliability is the "probability that a product (system) will perform its intended function for a specific time period when operating under normal (or stated) environmental conditions" [133]. The robustness, on the other side, is the "capability of functioning correctly or not failing under varying application and production conditions" [134]. This is verified by the process of ¨qualification¨, which includes all the activities that ensure that the nominal design and the manufacturing will meet or exceed the reliability targets [134]. On one hand, robustness qualifications include pass or fail tests, while reliability include lifetime tests (time-to-failure, lifetime extrapolation...).

Under qualification tests, failure could occur that is the inability of the product to perform its defined mission. Here, we should differentiate between the failure mechanism and mode. The failure mechanism is the physical, chemical, electrical or other process that cause device degradation or failure. Whereas, the failure mode, is simply the observable failure event (short circuit, open circuit...). Hence, for a single failure mechanism, several failure modes could be associated. In an integrated circuit, failure could occur at different levels (transistor, interconnection, package...) with diverse origins (electrical, mechanical, chemical...). At the hybrid bonding level, the failure mechanisms expected are, in majority, similar to the BEoL level. In my PhD thesis, we will focus on the main failure mechanisms shown in table 3.1.

The main objective of this chapter is to study and understand the failure mechanisms stated in table 3.1 and any possible variation with pitch reduction. Below, we briefly explain the importance to study each failure mechanism at the hybrid bonding level. We choose to present the failure mechanism results depending on their critical importance to the hybrid bonding level (from the least to the most critical).

Interface Mechanical Stability

During their lifetimes, interconnects are subject to repetitive thermomechanical stresses that could lead to fatigue induced failures. At the hybrid bonding level, this could eventually lead to interface delamination. In addition, with pitch reduction, higher thermomechanical interactions are expected due to the reduced spacing between neighboring pads [21]. Therefore, in the first part of this chapter, the objective is to study the mechanical stability of the hybrid bonding interface with pitch reduction down to 0.81 μm by Thermal Cycling (TC) tests.

Stress induced Voiding

The stress induced voiding (SiV) is a failure mechanism that takes place at the metallization levels of the IC. It is driven by the Cu/dielectric interface quality, the residual stresses at the interface as well as by the grain microstructure [135] under the application of a thermal budget. In the previous chapter, for our specific integration, we showed that the grain number decreases with Cu width reduction where a single or dominant grain is expected when the Cu pad width is below 1 μm. This could impact the failure occurrence under SiV. In the second part of this chapter, the objective is to study any impact of the reduction of the HBM size on the SiV failure mechanism by the mean of High Temperature Storage (HTS) Tests.

Electromigration

The electromigration (EM) failure mechanism takes place at the metallization level (similar to SiV) and is defined as the matter displacement activated by the application of temperature and electrical current. Until today, and for the hybrid bonding configuration with an HBV/HBM, failure by electromigration always occurs at the BEoL level, inside the top or bottom metal lines depending on the current flow direction [39]. Important questions arise with the reduction of the pitch namely: (a) what are the implications of hybrid bonding pitch reduction on the time-to-failure under EM? (b) As the HBM and HBV tend toward similar sizes, is there any implication on the killer void location? In the third section of this chapter, our main objective is to study any change in the failure mode with hybrid bonding pitch reduction that could degrade the EM performance.

Cu Diffusion at the Cu/SiO_2 Interface

Cu diffusion is a major concern for the hybrid bonding integration, particularity the Cu/SiO_2 one. During the bonding step, a misalignment is expected leading that part of Cu HBM will directly faces the SiO_2. Cu diffusion, under the atomic and ionic forms, could degrade the insulation properties of SiO_2. Many studies have been done by Moreau and Jourdon, where no Cu ionic or atomic diffusion is identified [44] [45]. A hypothesis was put in place where a self-formed Cu_2O layer is present at the interface, in the area where Cu is directly facing SiO_2, which could act as a barrier to Cu diffusion. In the fourth part of this chapter, the objective is to study the validity of the hypothesis of Cu_2O as a barrier to Cu diffusion at the Cu/SiO_2 hybrid bonding interface and whether it remains immune to Cu diffusion with the reduction of the hybrid bonding pitch. To

achieve this, we will study separately both the atomic and ionic diffusion mechanisms by new characterization methods. Discussions will include possible explanation on the Cu_2O formation at the hybrid bonding interface.

Time Dependent Dielectric Breakdown

The Time dependent dielectric breakdown (TDDB) occurs at the SiO_2 level and refers to the physical process whereby a dielectric stored under a constant electric field, less than the materials breakdown strength, will breakdown with time. The TDDB is seen as the most critical failure mechanism for the hybrid bonding interface since any presence of Cu diffusion could degrade the performances under TDDB. In addition, the reduction of the pitch and distance between neighboring pads could lead to serious implications on the failure mode under TDDB. In the last section of this chapter, as no detailed TDDB study does exist for the hybrid bonding, the main objective is to understand the TDDB failure mechanism and mode for our Cu/SiO_2 hybrid bonding integration.

Table 3.1: Potential reliability risks at the hybrid bonding level and the tests used to assess each risk.

Potential reliability risk	Consequence	Tests used to assess the risk
Interface mechanical stability	Higher resistance and leakage current, open circuit	Thermal cycling (TC) test
Stress induced voiding (SiV)	Higher resistance until open circuit	High temperature storage (HTS)
Electromigration (EM)	Higher resistance until open circuit	EM tests (temperature, stress current densities)
Copper diffusion	High leakage current and dielectric properties degradation	Bias temperature stress (BTS)/ Triangular voltage sweep (TVS) and BTS/capacitance-voltage (C-V)
Time dependent dielectric breakdown (TDDB)	Dielectric breakdown	Constant voltage stress (CVS) at different temperatures and electric fields

3.1 Study of interface mechanical stability

3.1.1 Failure physics

Interconnects are subject during their lifetimes to thermal cycles due to current and power cycling (Joule heating-related aspects) and environmental changes. During these cycles, thermomechanical stresses are generated due to the different coefficients of thermal expansion (CTE) of the (different) materials comprising the interconnect levels. The general equation that targets the generated thermal stress σ_{th} in the case of a thin film deposited on a substrate depends on the temperature and the type of material, and is expressed by the following formula [136]:

$$\sigma_{th} = \frac{E_f}{1-\nu_f}(T - T_0)(\alpha_s - \alpha_f) \tag{3.1}$$

where E_f is the Young's modulus (GPa), ν_f is the Poisson's ratio, α_f and α_s are the CTE of the thin film and substrate respectively (1/K) and T_0, T are the stress free temperature and the test temperature in K respectively.

If we focus at the materials used at the BEoL level, and similarly the hybrid bonding interface, it consists mainly of Cu and dielectrics. Therefore, high thermal stresses is expected to be generated under the application of temperature stress due to the CTE difference between Cu and the dielectric material. Such repetitive stresses can eventually lead to fatigue damage like ruptures leading to larger leakage current and/or high-resistance interconnects and, ultimately open circuits [137] [138] [139].

At the hybrid bonding level, we are interested in studying any impact of the repetitive thermomechanical stresses at the hybrid bonding level. A possible consequence on the interface level could be interface delamination since it is constituted of alternation of Cu and SiO_2 materials.

3.1.2 Previous studies at the hybrid bonding level

Table 3.2 summarizes the previous results of TC tests performed at the hybrid bonding level. The integration type is also mentioned with respect to pad-only or via+pad designs and the type of dielectric used at the interface. We can see that, whatever the integration type, no robustness issues are reported. The only failures are attributed to a package issue. It should be mentioned that these results include mainly tests done on W2W integration (ST/CEA-LETI, Xperi, IMEC, YMTC) and only one result on D2W qualification (Xperi). This suggests that the hybrid bonding interface has similar robustness as compared to a standard Cu/dielectric passivation BEoL interface. For the integration of interest for my PhD, at STMicroelectronics, CEA-LETI and IMS, the robustness was evaluated down to 1.44 μm bonding (electrical pitch of 7.2 μm) while reporting no failures [21]. In the following sections, a focus is done on the 1.44 μm electric pitch that will also serve as a reference for our study with pitch reduction. The robustness of the hybrid bonding interface with pitch reduction down to 0.81 μm is also studied.

Table 3.2: Summary of the reported TC tests results from literature at the hybrid bonding level.

Company/Research Institution	TC Conditions	Interconnection Pitch	Integration Type	Fail/No Fail	Ref
ON Semiconductor	-40 °C to 85 °C, 1000 cycles	8 μm	pad only - Cu/SiO_2	One fail (package issue)	[140]
ST/CEA-LETI	-50 °C to +150 °C, 1000 cycles	7.2 μm	via+pad - Cu/SiO_2	No fail	[67]
	-65 °C to +150 °C, 500 cycles	7.6 μm	via+pad - Cu/SiO_2	No fail	[21]
	-55 °C to +150 °C, 500 cycles	1.44 μm	via+pad - Cu/SiO_2	No fail	[21]
IMEC	-40 °C to +125 °C, 1000 cycles	10 μm	via+pad - Cu/SiO_x	No fail	[141]
Xperi	-40 °C to +150 °C, 1000 cycles	10 μm	pad only - Cu/SiO_2	No fail	[142]
	-55 °C to +125 °C, 1000 cycles	3.8 μm	pad only - Cu/SiO_2	No fail	[143]
Global Foundaries	-65 °C to +150 °C, 1350 cycles	5.76 μm	via+pad - $Cu/diel$ (not detailed)	One fail	[144]
Yangtze Memory Technologies Co.	-65 °C t +150 °C, 15000 cycles	1 μm	via+pad - $Cu/diel$ (not detailed)	No fail	[38]

3.1.3 Experimental results

3.1.3.1 Structures of interest and test conditions

The test structure used to monitor the resistance variations after thermal cycling tests is a daisy chain (see figure 1.8 (a)). The failure criterion is set at a 10 % increase in the chain resistance that is an arbitrary criterion frequently used. Similarly, the leakage current is monitored on a comb-comb structures with 57k links adapted to hybrid bonding (see figure 1.8 (b)). The leakage current failure criterion is set when $I_{final}/I_{initial}$ is 100, which is an arbitrary criterion. TC tests are performed with the temperature range of -65 °C and +150 °C according to JEDEC standard JESD22-A104 corresponding to the consumer domain [145].

3.1.3.2 1.44 μm pitch

The resistance variations for the DC with 30k links and 1.44 μm pitch after the different TC tests are shown in figure 3.1. After 500 cycles, the resistance increases between 0.1 and 0.2 % with respect to the initial chain resistance. The resistance variations correspond to all the dies on a single wafer. The resistance variations on the control structures without any aging are below 0.003 %. This means that the variations observed after 500 cycles are a real indication of an interconnect resistance increase. These variations are still very low with respect to the arbitrary criterion of 10% increase. To check if resistance continues to increase, TC tests were conducted until 2000 cycles with a reading every 500 cycles. As shown in figure 3.1 (a), after 1000 cycles, the resistance decreases returning close to their initial values. It is then hard to deduce any resistance evolution up to 2000 cycles considering the variations on the reference structures without any aging. After 2000 cycles, the resistance variations are between -0.2 and 0.1% that are well below the failure criterion of 10 %. We can conclude that the Cu/SiO_2 hybrid bonding level with 1.44 μm pitch is robust. This is true for all levels including the HBV, HBM, hybrid bonding interface as well as the top and bottom metal lines.

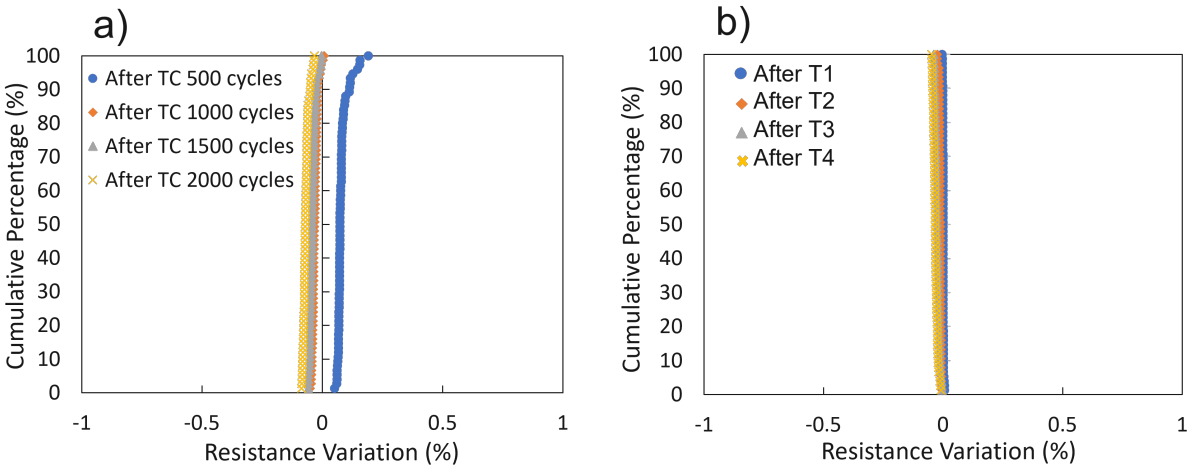

Figure 3.1: Resistance variations for the DC-30k links with 1.44 μm pitch from the $S\&H$ test vehicle on a) the sample after thermal cycles and b) the control sample without any aging. T1, T2, T3 and T4 represent variations on reference sample with measurements done with the same tester equipment as after TC 500, 1000, 1500 and 2000 cycles respectively.

To check any potential impact of thermal cycling on the dielectric side, the leakage current variations on the comb-comb with 57k links and 1.44 μm are studied. The results are shown in figure 3.2. The variations observed on the stressed structures are similar to the ones obtained on the reference sample without any aging. In fact, the leakage current measurements are sensible to the probe positions on the Al pads. In addition, some corrosion degradation of the Al pads was observed after TC that might explain these variations. In any case, the leakage current ratio stays well below the failure criterion of 100 advising no detectable impact of thermal cycling on the 1.44 μm pitch hybrid bonding level.

In the following section, the behaviour of hybrid bonding level under thermal cycling is studied on electrical test vehicles with pitch down to 0.81 μm.

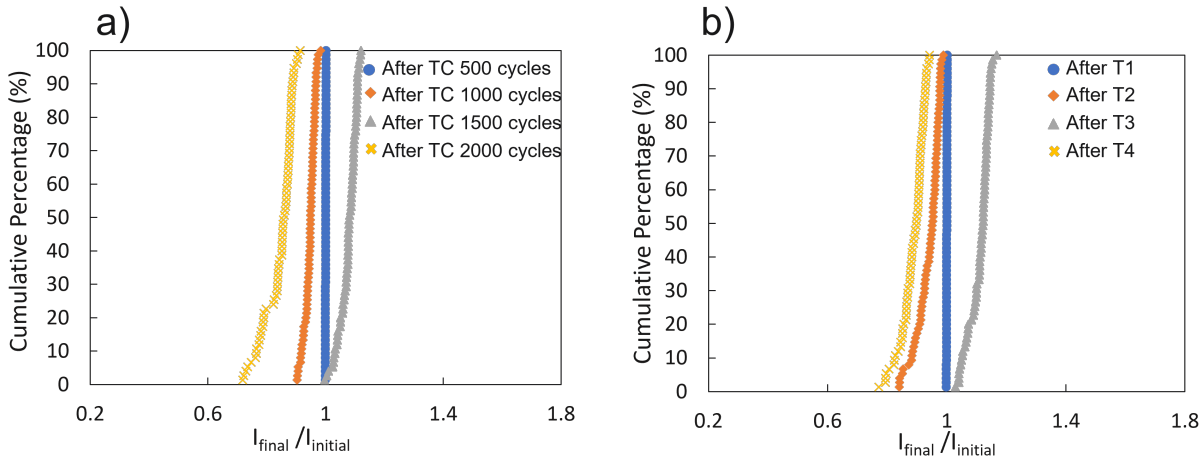

Figure 3.2: Leakage current variations for the comb-comb 57k links with 1.44 μm pitch on the *S&H* test vehicle on a) samples after TC test with intermediate readouts and b) on control samples without any aging.

3.1.3.3 Hybrid bonding level mechanical stability with pitch reduction

With hybrid bonding pitch reduction, lower spacing between adjacent pad is present. As previously shown by Jourdon using numerical simulations down to 1.44 μm, this lower spacing leads to an interface highly stressed and to interactions between adjacent pads. This behaviour is believed to be even more critical for pitch below 1 μm due to even lower spacing that can lead to high risk of delamination. TC test, with the same condition previously described, is performed on a TEDDY-UFP wafer that embeds hybrid bonding pitch down to 0.81 μm. The electrical resistance variations results are shown in figure 3.3 (a). After 500 cycles, the electrical resistance variations are in the range of ± 0.1 % for the different hybrid bonding pitches down to 0.81 μm, which are well below the 10 % resistance increase failure criterion. We can conclude that the Cu/Cu interface is mechanically stable down to 0.81 μm for the range of TC test conditions done.

To study any impact of TC on the dielectric side, the leakage current is tracked on comb-comb structures with 57k interconnection links with pitch reduction. The results are shown in figure 3.3 (b). The leakage current variations down to 0.81 μm pitch observed after the TC test were similar to the variations on the reference wafer without any aging as it was the case for the 1.44 μm pitch (see figure 3.2). This suggests that there the Cu/SiO_2 and SiO_2/SiO_2 interfaces are also stable after thermal cycling. The observations should be confirmed by performing different TEM cross sections to study the dielectric interface state after the thermal cycling test.

3.1.4 Conclusion

In this section, we have studied the mechanical stability of the hybrid bonding with pitch reduction down to 0.81 μm. The risk of interface delamination increases with pitch reduction due to lower spacing between adjacent pads leading to highly stressed interface and higher mechanical interactions between pads. This risk was evaluated using thermal cycling test with the temperature range of -65 °C and +150 °C. For the 1.44 μm pitch

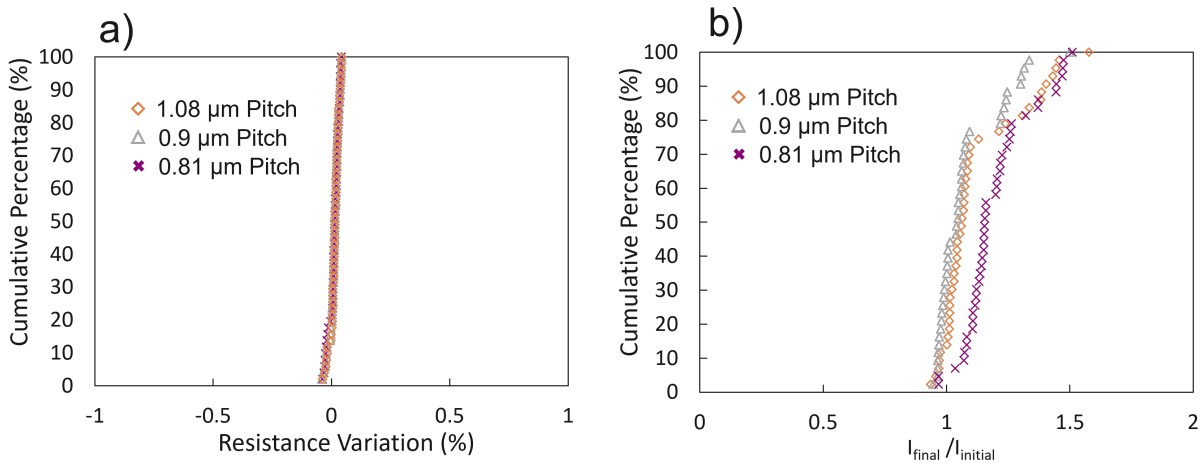

Figure 3.3: a) Resistance variations for the DC 30k interconnection links with pitch reduction down to 0.81 μm on the TEDDY-UFP test vehicle and b) leakage current variations for the comb-comb 57k links with pitch reduction after the TC test with the temperature range of -65 °C and +150 °C for 500 cycles.

and even after 2000 cycles, no sign of any interface delamination was observed both on the Cu and dielectric sides. The same conclusion applies with pitch reduction down to 0.81 μm pitch after 500 cycles of tests. Based on these findings, we can conclude that the hybrid bonding level is mechanically stable down to pitch of 0.81 μm and any risk of interface delamination can be neglected. We think that the mechanical stability of the interface is driven by the good bonding energy at the Cu/SiO_2 hybrid bonding interface. Therefore, further pitch reduction below 0.81 μm should not rise any particular concern as long as the materials used at the interface are similar.

3.2 Stress induced Voiding

3.2.1 Failure physics and degradation model

The stress induced voiding (SiV) is a failure mechanism that takes place in the metallization levels of the integrated circuit (IC). The SiV phenomenon is driven by the residual stresses present at the Cu/dielectric levels that are unique to each specific process. The SiV can be accelerated with the application of a thermal budget. The SiV failure mechanism can be summarized in two phases. The first phase is observable with void propagation at the grain boundaries. This process is mainly driven by the micro-structure inhomogeneity. At high temperature and in the absence of an electrical current, the grain expands intrinsically causing cavities in the structure. The second phase can be summarized by the migration and accumulation of voids in the zones where the stress is lower. This will lead to an increase in the interconnect electrical resistance until a failure by an open circuit occurs. The characteristic of SiV is that it occurs without electric current flowing through the interconnect. For the SiV phenomenon study, constant temperature is used. The generalized expression for the SiV time to failure can be expressed by the equation 3.2 [146]:

$$t_F = A_0(T - T_0)^{-n} exp\left(\frac{Q}{k_B T}\right) \tag{3.2}$$

where A_0 is a constant which depends on the particular geometry, n is the stress migration exponent which depends on the material type and microstructures of the interconnects, Q is the activation energy for void creation in eV, k_B is the Boltzmann constant ($8.617 \times 10^{-5}\ eV\ K^{-1}$), T_0 and T are respectively the stress free temperature and the applied temperature. When the SiV test is carried out at temperature close to stress free temperature, the tensile stress in the metal line is low, so that the void growth rate is low and the SiV phenomenon is hardly activated. When the temperature is close to ambient one, there exists high tensile stresses, but the mobility or diffusivity is low. As temperature increases, the diffusivity increases exponentially and the SiV lifetime will decrease consequently until reaching the critical temperature (T_{crit}). Therefore, to accelerate the SiV phenomenon, the test should be carried at T_{crit} that was reported to lie in between 150-200 °C for Cu interconnects [146] [147]. The failure time reported in the back end of line (BEoL) Cu case, on via+metal line structures, is in the range of few hundreds to 5000 h hours depending on the Cu width and testing temperature [148] [149]. For Cu dual damascene processes, the SiV failure rate was found to increase with increasing line width that is opposite to what has been observed for AL line [150].

3.2.2 Previous SiV studies at hybrid bonding level

Table 3.3 summarizes the reported SiV studies in the literature performed at the hybrid bonding level by HTS. No major failure behaviour has been reported and the only failures do not confirm if it is a hybrid bonding related one [144]. For the integration of interest for my PhD, the robustness of the hybrid bonding level was evaluated down to 7.6 μm interconnection pitch. In the following section, a focus is done on the SiV study for the 1.44 μm pitch by HTS test at 175 °C according to JEDEC (JESD22-A103 - consumer domain) [151], and by going beyond the 1000 h standard annealing time (up to 4000 h). In addition, the robustness of the hybrid bonding interface with pitch reduction down to 0.81 μm will be studied.

3.2.3 SiV experimental results

3.2.3.1 1.44 μm pitch

The resistance variations are monitored on the DC structure (figure 1.8 (a)) with 30k links and 1.44 μm pitch after the different HTS tests at 175 °C as shown in figure 3.4 (a). A resistance decrease can be observed after the first 1000 h (between 0.15 and 0.22 %) that is well below the 10 % failure criterion. To inspect if these variations come from the measurement errors, the resistance variations are tracked on a reference sample (without any aging) by measurements done at the same time and using the same tester as the sample enduring HTS. The resistance variations on the reference structures are below 0.003 %. This indicates that the variations observed after 1000 h are a real indication of a decrease in the interconnect resistance. This could be related to the interface, HBV, HBM or metal line resistance decrease. The specific structures for contact resistivity evaluation could be beneficial to study if the resistance variations after HTS are attributed to the Cu/Cu interface. This is not possible for this particular study since these structures are

Table 3.3: Summary of previous HTS tests results reported in the literature at the hybrid bonding interface.

Company/Research Institution	HTS Conditions	Interconnection Pitch	Integration Type	Fail/ No fail	Ref
Sony	175 °C, 1000 h	4 μm	via+pad - Cu/SiO_2	No fail	[20]
	175 °C, 1000 h	3 μm	via+pad - Cu/SiO_2	No fail	[152]
ON Semiconductor	200 °C, 500 h	8 μm	pad only - Cu/SiO_2	No fail	[140]
ST/CEA-LETI	175 °C, 2000 h	7.6 μm	via+pad - Cu/SiO_2	No fail	[67]
Xperi	225 °C, 2000 h	10 μm	pad only - Cu/SiO_2	No fail	[142]
Global Foundaries	225 °C, 1000 h	5.76 μm	via+pad - $Cu-diel$ (not detailed)	3% failed structures	[144]
Yangtze Memory Technologies Co.	200 °C, 7000 h	1 μm	via+pad - $Cu-diel$ (not detailed)	No fail	[38]

not embedded in the $S\&H$ test vehicle. For the SiV studies with pitch reduction down to 0.81 μm, the contact resistivity evaluation after HTS will be conducted if seen necessary.

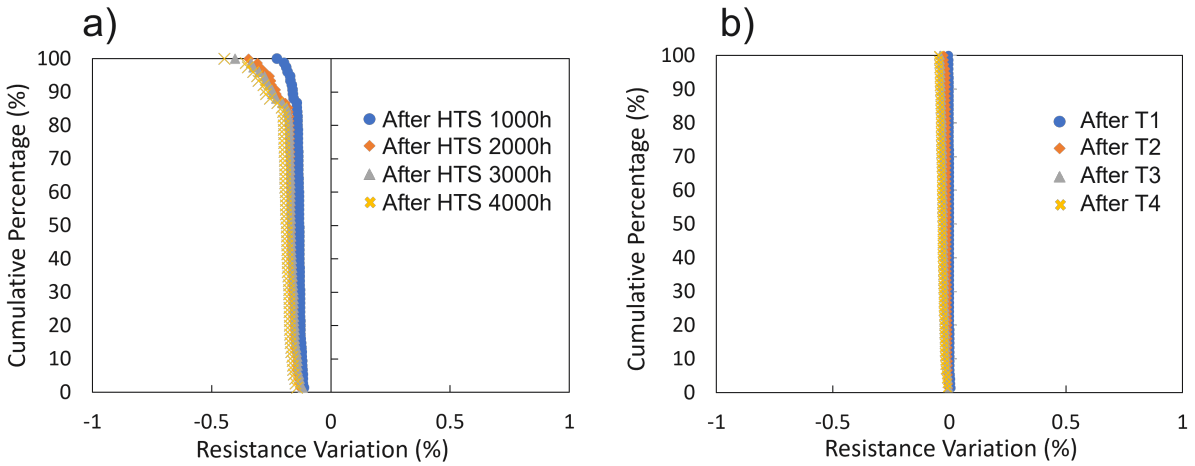

Figure 3.4: Resistance variations for the DC-30k link with 1.44 μm pitch on the $S\&H$ test vehicle after a) the different HTS tests and b) on reference sample without any aging. T1, T2, T3 and T4 represent measurements done on the reference sample at the same time/tester as after HTS 1000, 2000, 3000 and 4000 h respectively.

Since for the BEoL case, the SiV failure time could go up 5000 h [148] [149], the HTS tests were continued until a total time of 4000 h with a resistance measurement

each 1000 h. As shown in figure 3.4 (a), the resistance did not change with increasing HTS time for the cumulative distribution up to 85 % of the population, taking into account the variations observed on the reference sample. For the population higher than 85% of cumulative distribution, the resistance decreases with higher HTS time. In both cases, the resistance variations are below 0.5 % that are well below the set failure criterion.

Although in the literature, SiV could occur at lower times than 4000 h, this is dependent on the Cu properties, interconnection design and surrounding materials that vary with different integrations. In addition, we question if the stress temperature used at 175 °C is the critical one to accelerate the SiV phenomenon for the hybrid bonding integration. For future studies, it will be interesting to perform HTS tests in the temperature range of 150-250 °C to calibrate the critical temperature of test. Based on the results reported in this section, we can conclude that the SiV failure mechanism is not really activated for the 1.44 μm even when testing up to 4000 h.

In the following section, the hybrid bonding level robustness under HTS will be evaluated with pitch reduction down to 0.81 μm.

3.2.3.2 SiV with pitch reduction

The SiV study with pitch reduction is conducted on a wafer from TEDDY-UFP test vehicle that embeds hybrid bonding pitch down to 0.81 μm. The resistance variations after HTS on DC structures with 30k link interconnections are shown in figure 3.5. Whatever the hybrid bonding pitch, with 1.08, 0.9 and 0.81 μm, the electrical resistance variations lie in between ±0.1 %. We can conclude that the hybrid bonding level is immune to the SiV phenomenon despite the shrinking size and spacing between adjacent pads. In addition, considering the low variations in the electrical resistance, any Cu/Cu interface contact resistivity evaluation after HTS is not possible.

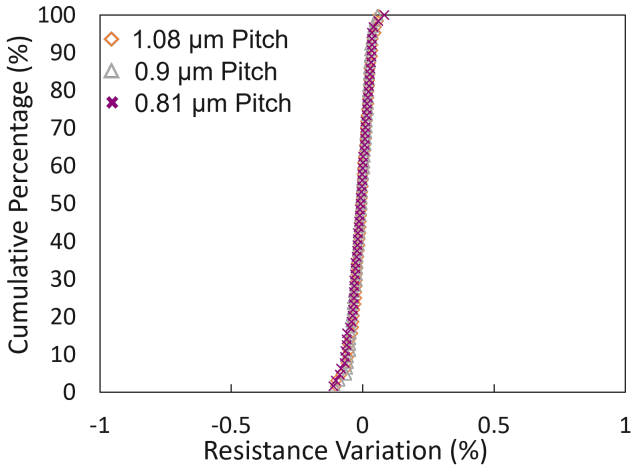

Figure 3.5: Resistance variations for the DC-30k links structures with pitch reduction down to 0.81 μm on the TEDDY-UFP test vehicle after HTS test at 175 °C for 1000 h.

3.2.4 Conclusion

In this section, the stress induced voiding failure mechanism was evaluated at the hybrid bonding level with pitch reduction down to 0.81 μm under high temperature storage tests. No SiV failures were depicted after 4000 h of storage for the 1.44 μm pitch. Only small resistance variations (< 0.5 %) were found that can be attributed to any of the different elements forming the interconnection such as the HBV, HBM and metal lines. Any role of Cu/Cu interface reconstruction could not be concluded in the present study, which can only be tracked by quantifying the contact resistivity. Moreover, even with pitch reduction down 0.81 μm, the hybrid bonding level remains immune to SiV and no failures take place after 1000 h of HTS. Therefore, the hybrid bonding level is robust down to 0.81 μm pitch with the specific test conditions used. For future studies, it would be pertinent to continue the HTS tests beyond 1000 h on sub micron pitches to study any possible SiV failure. Moreover, it is important to perform HTS tests with the temperature conditions range of 150-250 °C that might give more insights on the critical temperature for test to accelerate the SiV failure mechanism.

3.3 Electromigration

For the hybrid bonding configuration of interest for my PhD, with HBV and HBM, studies done by the team at CEA-LETI/STMicroelectronics showed that electromigration related voids always occur at the BEoL level (top or bottom metal line depending on the electron flow) [39]. There is no HB-related failure down to 7.2 μm pitch, suggesting that the hybrid bonding interface is immune to electromigration irrespective of the electron flow direction. However, with further reduction of the hybrid bonding pitch, several crucial questions on the EM behaviour arise:

1. Does the hybrid bonding interface stay immune to EM related failure? In fact, a study done by IMEC with a 3.42 μm hybrid bonding pitch reported a killer void at the hybrid bonding level depending on the current flow direction [153].

2. In the previous chapter, we showed that with pitch reduction, HBV and HBM will tend toward continuous shapes and we expect a single dominant grain for Cu pads below 1 μm width. Are there any implications on the time-to-failure (TTF)?

In this section, the objective is to study any change of the EM failure mechanism and performance with the reduction the hybrid bonding pitch down to 1.44 μm.

3.3.1 Failure physics and degradation models

The electromigration failure mechanism can be defined as the matter displacement observed inside a metallic material. It is activated by temperature and induced by the flow of electrical current and can be accelerated by thermomechanical stresses. On one side, this displacement results in the formation and growth of cavities until the electrical rupture of the structure. On the other side, extrusion could be observed. This phenomenon is much important with higher current densities inside the interconnections.

One of the important parameters that drives the matter displacement is the diffusion coefficient. It defines the electromigration performance. It is written as an effective diffusion coefficient that is decomposed by equation 3.3 [154], [155]:

$$D_{EFF} = D_l + D_d.f_d + D_i.f_i + D_{gb}.f_{gb} \tag{3.3}$$

The subscripts in the above equation donate various diffusion paths as follows: l: lattice (or bulk), d: dislocation core, i: interface, gb: grain boundary and f_r (r = d, i, gb) as the fraction of atoms diffusing through a given pathway.

The semi-empirical equation for median time to failure of a group of identical conductors which had same EM stressing is known as generalized Black's equation and expressed by equation 3.4 [156]:

$$t_{50} = Aj^{-n}exp(\frac{E_a}{k_BT}) \tag{3.4}$$

where t_{50} is the median time to failure, A is a constant which contains a factor involving the cross-sectional area of the film and material properties, j the current density in the conductor (MA/cm^2), k_B the Boltzmann constant, T is the temperature in K, n and

E_a are respectively the stress current exponent and the activation energy (eV) which are also known as the Black's parameters. E_a and n are independent variables obtained by varying the test conditions: one while fixing the current and varying the temperature and inversely for the second. This is further detailed by the following equations:

$$E_a = \left(\frac{-d(ln(MTTF))}{d(\frac{1}{kT})} \right)_{jcsnt} \tag{3.5}$$

$$n = \left(\frac{-d(ln(MTTF))}{d(j)} \right)_{Tcsnt} \tag{3.6}$$

Originally, Black's derivation resulted in n = 2 [157]. This was the source of a debate until showing that the value of the n parameter is generally between 1 and 2, which is directly related to the importance of the nucleation time for cavities with respect to the growth time [158]. For the case of Cu, where the nucleation phase is very short, n is close to 1 [159]. n close to 2 is associated with a failure dominated by the void nucleation time that was mostly reported for Al interconnects [160]. The activation energy for each diffusion path for the Cu interconnect are shown in table 3.4. As shown, the lattice or bulk diffusion has the highest activation energy, being the slowest path for mass transport. The interface diffusion between Cu and the surrounding layers dominates the diffusivity path having the lowest activation energy.

Table 3.4: Activation energy (E_a) associated with each diffusion path for the Cu interconnect.

Diffusion path	E_a (eV)	Reference
Bulk Cu	2.3	[161]
Dislocations	1.2-1.5	[162]
Grain boundary	0.8-0.85	[163]
Interface Cu/passivation	0.8	[164]

Alternatives to the Black's formula have been proposed lately. Lloyd proposed a model that takes into account both the nucleation and growth phases [165]:

$$MTTF = \left(\frac{A.k.T}{j} + \frac{B(T)}{j^2} \right) exp \left(\frac{E_A}{k_B T} \right) \tag{3.7}$$

Where A and B are constants which contains geometric information, such as the size of the void required for failure. $B(T)$ also has a temperature dependence that depends on which failure model is chosen. Because of its simplicity, the Black's formula is still actually widely used.

3.3.2 State of the art of electromigration studies at hybrid bonding level

Starting by previous studies done by the team at CEA-LETI/STMicroelectronics for identical integration as my PhD study (HBV and HBM configuration with Cu/SiO_2), Moreau gave a detailed EM study with HBM width down to 3.6 μm and also a potential effect of the HBV redundancy and positioning [39]. The stress temperature was set to 350 °C and

a variable stress current between 5 and 30 mA (Joule heating less than 5 °C). Physical failure after EM tests showed that the weakest link is either the top or bottom metal line depending on the electron flow. Therefore, the failure is always situated at the BEoL level with an immune hybrid bonding interface. This study also concluded that the HBV positioning does not have an impact from an EM point of view, most probably due the HBM size. In addition, during his PhD thesis, Jourdon extracted the Black's parameters (activation energy and current exponent) from EM tests on samples with HBM width of 3.6 μm [41]. The temperature range of the study was between 290 and 350 °C and a stress current between 7.5 and 40 mA (Joule effect less than 10 °C). The activation energy was estimated at 0.99 eV $\pm$ 0.034 eV that is close from the BEoL activation energy for the grain boundary and metal/capping interface. The current exponent was found at 1.36 ± 0.11, which is higher than the expected value of 1 for growth time dominant failure.

For the pad only configuration, De Messemaeker at IMEC studied the EM performance with Cu/SiCN hybrid bonding and with the pitch of 3.24 μm (the top pad size is 540 nm while the bottom pad size is 1620 nm) [153]. For the upstream electron flow study, EM tests were conducted at 200 and 240 °C with current densities between 8.2 and 13.7 MA/cm^2. The activation energy is found at 0.93 eV that is close to the one found for the HBV-HBM configuration. Here also, the current exponent is found at 1.9, which can be a signature of a mixture between two EM models: void nucleation and void growth. Physical failure analysis showed that voids formation and failure occurred at the BEoL top metal line. This is linked to the electron wind through the top metal, carrying Cu atoms away from the top pad, until a critical vacancy concentration is reached and a void is nucleated and subsequently grows. As for the tests with electron flow down, these were conducted at a temperature of 240 °C and a stress current density of 13.7 MA/cm^2. The lifetime is significantly increased relative to the electron flow up test with the same temperature and current stress. This could be explained by the wider bottom line. Physical failure analysis showed large void at the hybrid bonding interface in addition to the BEoL bottom line location. Physical analysis on sample which has not yet failed showed that voids at the hybrid bonding interface are collected in a large void and moving up. This suggests that in EM, the empty volume behaves as a pre-existing void and will become a dominant contributor when scaling down the pad size. This result evidences, for the first time, a change of the EM failure mode at the hybrid bonding interface.

Based on what is reported, the main objective of our analysis is to study any failure mode change for the HBV-HBM configuration when scaling down the pad size down to 720 nm (pitch of 1.44 μm) and if any change of mode could degrade the projected lifetime at use conditions.

3.3.3 Electromigration results with pitch reduction

3.3.3.1 Structure of interest and test conditions

The test structure used for the EM failure mechanism and mode investigation is an asymmetric NIST-like structure adapted to the hybrid bonding integration as shown in figure 3.6. The main interest of this structure is that when a current is flown, it is first divided by 4 so that the highest current stress is guaranteed at the single link side. This will simplify the failure analysis. The studied pad dimensions are either 1.72 or 0.72 μm (pitch

of 3.42 and 1.44 μm respectively). There is one HBV per HBM for the different pitches. The metal line width is 3.42 and 1.44 μm for the 3.42 and 1.44 μm pitch structures respectively. As for the reservoir length, it is 0.72 μm for the 3.42 μm pitch compared to 0.2 μm for the 1.44 μm pitch.

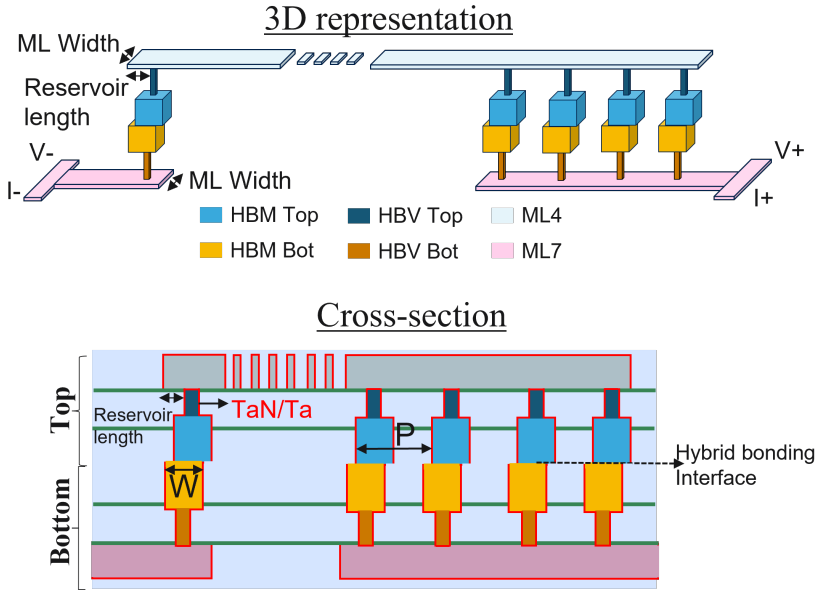

Figure 3.6: 3D (top) and cross-section (bottom) schematic representations of the NIST-like structure used for the electromigration study with pitch reduction. W is the HBM pad width and P is the interconnection pitch.

EM tests are performed at the package level with the temperature and current stress conditions in table 3.5. All the EM tests and physical failure analysis were performed at CEA-LETI by *Stéphane Moreau* and *David Bouchu*. The testing temperature is fixed at 350 °C and the maximum current stress is limited to 20 mA to keep the Joule effect below 10 °C. Having high Joule heating could over-accelerate the EM phenomenon leading to false results when extrapolating to use conditions. Most importantly, Joule effect should be kept low to limit possible interaction between E_a and n through the temperature and the current stress. The failure criterion is set at a 10 % increase in the interconnect resistance, which is an arbitrary criterion.

Table 3.5: EM tests conditions.

Structure	Temperature (°C)	Stress Current (mA)
NIST - 3.42 μm pitch	350	18.5
NIST - 1.44 μm pitch	350	15
		18.5
		20

3.3.3.2 EM Time to failure with pitch reduction

The EM time-to-failure (TTF) distributions at 350 °C and 18.5 mA for the 3.42 and 1.44 μm pitch NIST-like structures are shown in figure 3.7. The slope is similar between

the different pitches suggesting the same failure mechanism. For either pitch, the highest stress current is 22.4 MV/cm^2 obtained at the HBV level and calculated as the ratio between the applied stress current (18.5 mA) and the HBV area (πR^2 with R being the theoretical radius of HBV around 162 nm). Higher EM TTFs are obtained for the 3.42 μm pitch. If the failure position is still at the BEoL level, possible explanations could be related to the higher metal line width for the 3.42 μm pitch structure and most importantly higher reservoir length (0.72 vs. 0.2 μm in reservoir length for the 3.42 and 1.44 μm pitch structures respectively). The reservoir length is defined as an extended region of metal line that hardly carries any current because its area is not the path of current flow. For the BEoL Cu interconnects, higher reservoir length led to an enhanced EM performance [166] [167]. If it is a hybrid bonding related EM failure, the impact of the HBM width could be the source of higher EM TTF for the 3.42 μm wide HBM. This will be further studied is section 3.3.3.3.

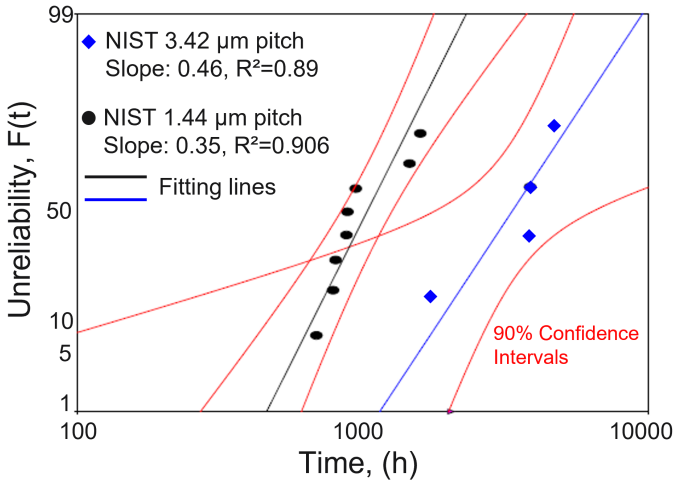

Figure 3.7: Probability plot (lognormal distribution) after EM test at 350 °C and 18.5 mA for the 3.42 and 1.44 μm pitch NIST-like structures on the $S\&H$ test vehicle.

Focusing on the 1.44 μm pitch, the EM results after tests at different stress conditions are shown in figure 3.8. Lower TTFs are obtained with increasing stress current between 15 and 18.5 mA. A much higher slope is obtained for the 20 mA condition. Possible explanations could be related to a different degradation mode or a possible over-acceleration phenomenon. Hence, the results at 20 mA are not taken into consideration when calculating the stress exponent. The stress exponent is calculated using equation 3.6 and is found close to 7.3 taking into account t_{50} for the 15 and 18.5 mA test conditions. This is much higher than the n value between 1-2 which is usually found for BEoL Cu and also from the previous studies [41] [153]. The deviation of the current exponent is a typical phenomenon that is mostly be related to local Joule heating effect and EM induced plasticity [168] [169].

To understand the root cause of the different performances with pitch reduction and to study any change in killer void location, a focus is done in the following section on the physical failure analysis.

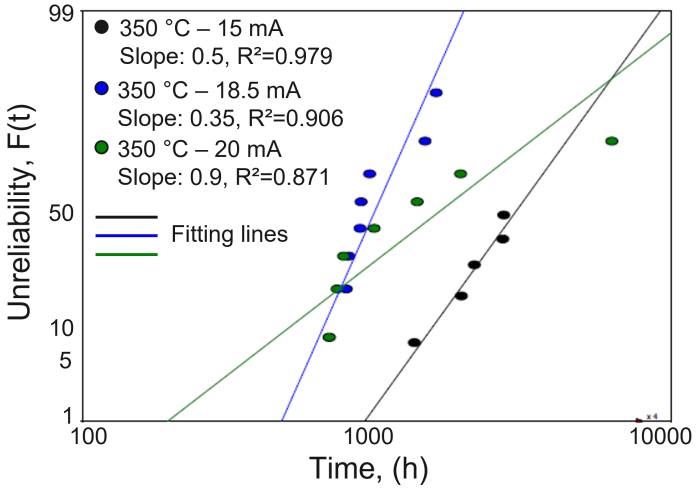

Figure 3.8: Probability plot (lognormal distribution) after EM test at 350 °C and for different stress current conditions for the 1.44 μm pitch NIST-like structure on $S\&H$ test vehicle.

3.3.3.3 Physical failure analysis

Failure localization is usually not needed for the NIST-like structure that is due to its particular design: the failure is always expected to be localized on the single link side (figure 3.6). Therefore, when analyzing the failure structures, cross sections are performed on the single link side.

For the 3.42 μm pitch case (HBM width of 1.72 μm), different cross sections imaging were performed for different failed structures and at different positions alongside the HBM length as shown in figure 3.9. We suspect that voids first occur at the HBM level caused by the low activation energy at the Cu/SiO_2 interface. This is the result of the misalignment between the top and bottom wafers (figure 3.9 (1)). Indeed, Moreau found lower EM activation energy when higher surface of Cu is in contact with SiO_2 [170]. In a second phase, voids nucleate at the HBV level due to the flux divergence resulting from the presence of the barrier between the top metal line and HBV and driven or not by the presence of a grain with low EM resistance (figure 3.9 (3)). This is also the location where the stress current density is the highest. The killer void is present at the HBV level and might sometimes lead to local melting due to Joule heating in the high resistance area. This study highlights a change in EM failure mechanism as compared to pitches higher than 6 μm when the killer EM void was present at the BEoL metal line level.

For the 1.44 μm pitch structures, a difference was observed when analyzing structure with different times to failures. For the beginning of the TTF statistics, the killer void is observed at bottom metal line due to the flux divergence resulting at the barrier (TaN/Ta) between the HBV and the bottom metal line as shown in figure 3.10 (a). This is attributed to an early failure due to a slit-like void [171]. Analysis of failed structure at the middle of TTF statistics highlights the same failure mode identified for the 3.42 μm pitch structure (figure 3.10 (b)). The killer void is observed at the top HBV level and similarly voids were identified at the Cu/SiO_2 interface.

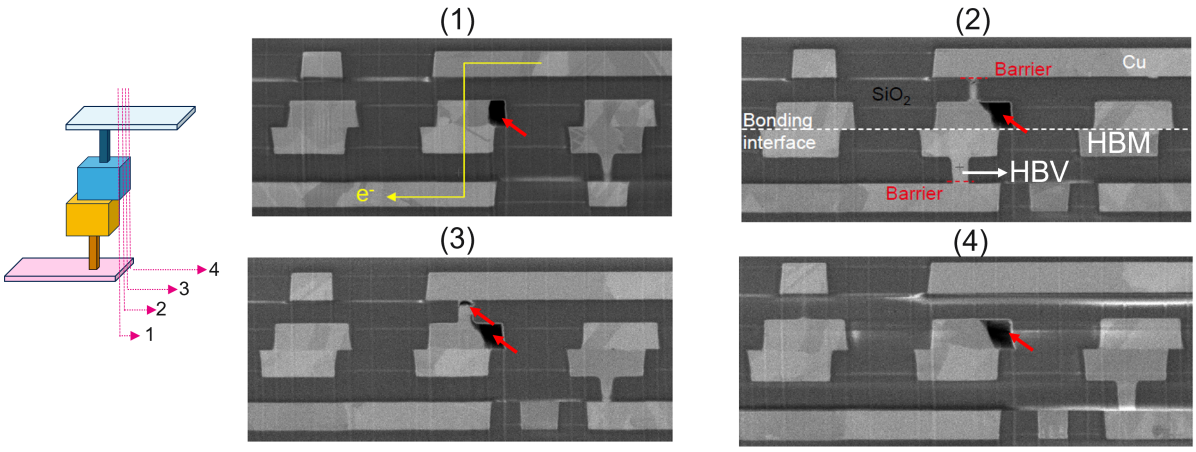

Figure 3.9: Electronic cross section imaging of failed test structure after EM test (350 °C, 18.5 mA, middle of the TTF statistics) for the 3.42 μm pitch structure on the $S\&H$ test vehicle. Voids are clearly identified at the HBV and HBM levels (red arrows).

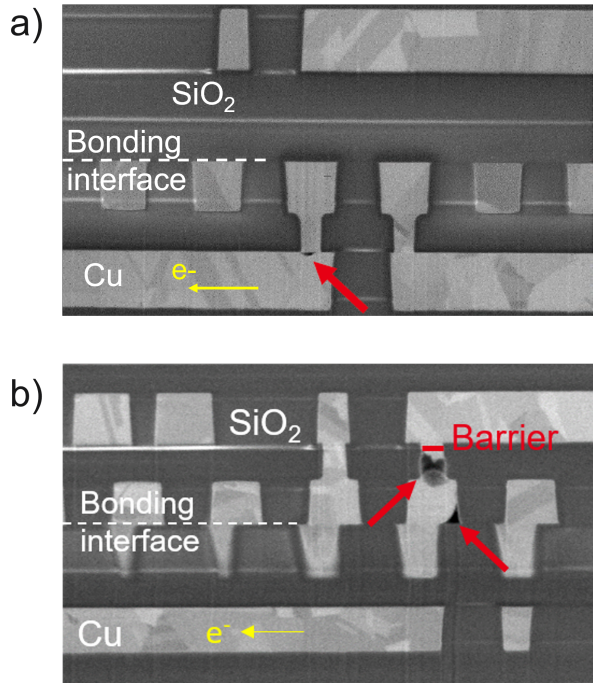

Figure 3.10: Electronic imaging of failed test structure with 1.44 μm pitch on the $S\&H$ test vehicle after EM tests at 350 °C, 15 mA for a) beginning of the TTF statistics and b) middle of the TTF statistics. Only the cross section with the EM related void is shown and highlighted by red arrows.

The results of the physical failure analysis evidence a change in the electromigration failure mode for pitch lower than 6 μm where the killer void is switched from the BEoL level to the HBV level. Since the failure is present at the interface, an explanation of the lower TTFs obtained for the 1.44 μm as compared to the 3.42 μm pitch could be related to an impact of the HBM width, acting as a reservoir length. In the following section, estimations at use conditions are performed for the 1.44 μm pitch to study any possible impact of the failure mode change.

3.3.3.4 Prediction for use conditions

In order to study any possible impact of the change in failure mode on the EM performance, extrapolation at operating conditions using the EM results at 350 °C - 15 mA for the 1.44 μm pitch is done using equation 3.8 [172]:

$$TTF_{oper} = MTTF_{stress} \left(\frac{I_{stress}}{I_{oper}}^{n} \right) \times exp \left[\frac{E_a}{k_B} \left(\frac{1}{T_{oper}} - \frac{1}{T - stress} \right) + NSD \times \sigma \right] \quad (3.8)$$

where NSD is the number of standard deviations related to the chosen percentage of failure and σ is the lognormal standard deviation. The subscripts ¨stress¨ and ¨oper¨ donate to EM testing and use/normal operating conditions respectively. Using equation 3.8, an estimation of the I_{use} to sustain specific life characteristics can be interpreted as shown in equation 3.9:

$$I_{oper} = I_{stress} \sqrt[n]{\frac{MTTF_{stress}}{TTF_{oper}} \times exp \left[\frac{E_a}{k_B} \left(\frac{1}{T_{oper}} - \frac{1}{T - stress} \right) + NSD \times \sigma \right]} \quad (3.9)$$

Since no precise extractions of the activation energy and stress exponent were possible for the 1.44 μm pitch, we will rely on the values reported in the literature. The activation energy is assumed at 0.7 eV that is the lowest activation energy reported for diffusion along the interface and a stress exponent n of 1 is taken (conservative case). The MTTF of stress at 15 mA and 350 °C is used for calculation. The projected current I_{oper} under use conditions for a consumer type application (10 years, 0.01 %, 125 °C) is 123 mA. Taking the fact that failure occurs inside the HBV, the current density is around 1.5×10^2 MA/cm^2. We can confidently conclude that the change of failure mode does not degrade the projected EM performances at operating conditions.

3.3.4 Conclusion

In this section, the electromigration failure mechanism for the Cu/SiO_2 hybrid bonding integration was investigated down to 1.44 μm pitch. A potential EM degradation scenario can be concluded as shown in figure 3.11. For pitch above 6 μm, the killer void is present at the metal line level. With hybrid bonding pitch reduction, the EM killer void is shifted to the hybrid bonding level. It is not possible to precisely estimate at which pitch the transition occurs since no EM data exists between 6.84 and 3.42 μm. For pitch below 3.5 μm, the first void occurs at the Cu/SiO_2 interface, probably due to low activation energy originated from the misalignment between the top and bottom wafers. In a second phase, void appears at the HBV level which could be caused by the flux divergence due to the presence of the barrier between the top metal line and HBV. A coalescence between these voids can occur leading to degradation. In addition, for the 1.44 μm pitch, we found a more complex scenario as low TTFs may be related to slit-like voids. Based on these results, it is no more valid to say that the HB level is immune to electromigration. However, despite the change of the killer void location, the projected performances under use conditions for the 1.44 μm pitch are not affected.

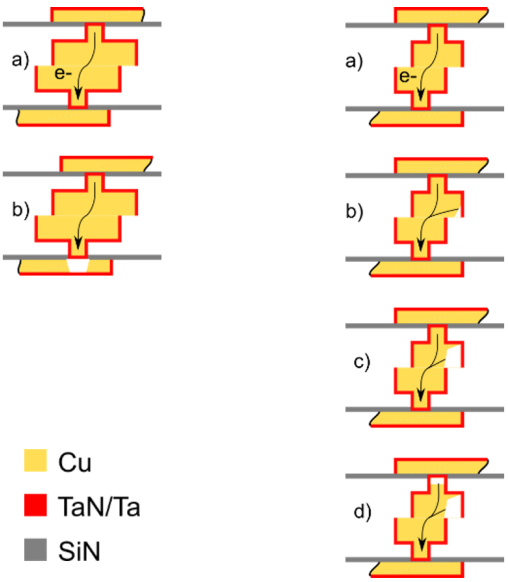

Figure 3.11: Illustration of the failure modes dependent on the hybrid bonding pitch: left) above 6 µm and right) below 3.5 µm (side view) for a downstream electromigration test [Moreau et al., IRPS 2023].

We believe that the EM failure mechanism is of critical concern with further hybrid bonding pitch reduction if the killer void is found to stay at the HBV/HBM level. Hence, EM studies on NIST structures with pitch reduction down to 0.81 μm should be done to understand the EM behaviour in the sub micron pitch region.

3.4 Cu diffusion at the Cu/SiO_2 interface

The critical degree of Cu diffusion at the hybrid bonding interface is directly related to the dielectric type used at the interface. Since we are dealing with Cu/SiO_2 hybrid bonding integration, Cu diffusion is one of our major concern. This is because misalignment could occur at the bonding step leading to part of Cu pad faces directly the SiO_2 as shown exemplary in figure 3.12. Cu has been well identified to highly diffuse into SiO_2 for the BEoL cases [42] [43] [173]. There are two main mechanisms by which metal species and particularly Cu can migrate into the dielectric:

- Thermal diffusion of metal atoms at ¨elevated¨ temperature, which is mainly driven by the metal concentration gradient
- Ionic diffusion of metal ions, which is driven by an applied external electric field

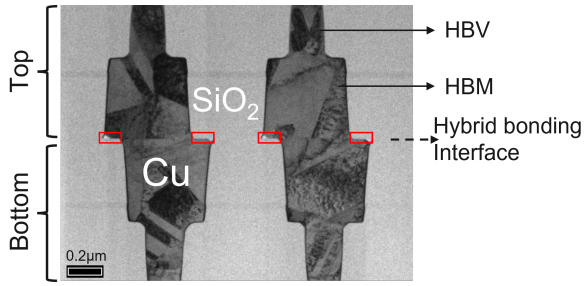

Figure 3.12: TEM cross section at the hybrid bonding interface inside a structure with 1.44 μm pitch showing the zones (red rectangles) where part of Cu HBM is in direct contact of SiO_2 due to misalignment from the bonding step.

Studies done by the team at CEA-LETI/STMicroelectronics identified by TEM-EELS a 3 nm of cuprous oxide (Cu_20) in the region of misalignment where Cu is facing SiO_2 (Cu/SiO_2 of red zones in figure 3.12) [45]. The EELS results are shown in figure 3.13. For the O-K ionization edge, and at positions (2) and (3), a pre-peak is identified highlighting a modification of O atoms, which is typically related to a metallic oxide as shown in figure 3.13 (b) (black arrow) [174]. As for the Cu EELS spectra at the interface (figure 3.13 (c)), a signal of Cu oxidation is observed at positions (2) and (3). The study concluded the presence of a Cu_2O layer with 3 nm thickness and the hypothesis that Cu_2O is acting as a barrier to Cu diffusion.

The main objective of the study in the section is to validate the hypothesis of a self-formed Cu_2O layer acting as a barrier to Cu diffusion and confirm it with pitch reduction. This is achieved by studying separately both atomic and ionic diffusion using new electro-chemical characterizations. In addition, a focus is done on the thermal stability of the Cu_2O layer after thermal aging. Several EELS measurements will be conducted to study the presence of the Cu_2O layer after different test conditions.

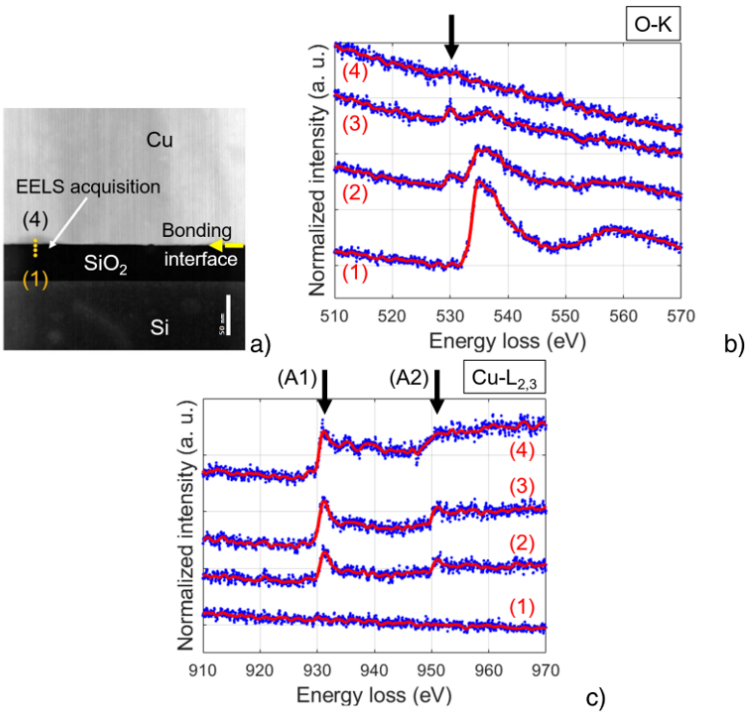

Figure 3.13: STEM picture illustrating the Cu/SiO_2 hybrid bonding interface along with the 4 positions used to perform EELS spectra acquisition. b) O-K ionization edge collected at the 4 sites, evidence of a pre-peak (black arrow). c) $Cu - L_{2,3}$ ionization edge at the 4 sites. [45]

3.4.1 Thermal diffusion

3.4.1.1 Preliminary analysis on Cu atomic diffusion: case of SiO_2 deposited on Cu

From BEoL studies, the diffusion coefficient of Cu in SiO_2 at 380 °C (corresponding to the bonding anneal temperature) varies between 2.2×10^{-20} and 2.8×10^{-18} $m^2.s^{-1}$ [43] [173]. This variation is related to the characteristics of the Cu/SiO_2 interface that vary depending on the specific material properties used (for example, the dopants used in Cu, the deposition technique of SiO_2...). Hence, a preliminary study is first done to check any Cu atomic diffusion when SiO_2 is deposited on Cu pads for the specific material used in our Cu/SiO_2 hybrid bonding process. The schematic description of the sample used for this study is shown in figure 3.14. The sample is composed of 300 mm wafer with patterned Cu pads (1 metal level of CPM8 mask) with width between 3.3 and 5.4 μm. After the CMP step, an 80 nm of SiO_2 is directly deposited on the Cu pads. The sample is annealed at 380 °C - 2 h to simulate the hybrid bonding annealing budget.

After bonding annealing, a TEM-EELS mapping is performed to study (a) any Cu diffusion at the Cu/SiO_2 interface and (b) the presence of a Cu oxide layer. The results are shown in figure 3.15. In figure 3.15 (a), the TEM analysis highlights a bump above the Cu pad and a gap separating the Cu pads from the bump. The EELS mapping for the different elements indicates a compound of SiCuO, which is formed mainly from Cu diffused into SiO_2. After the bonding annealing budget, the Cu/SiO_2 interface is thermally unstable and a delamination is seen at the interface. By SEM inspections, we

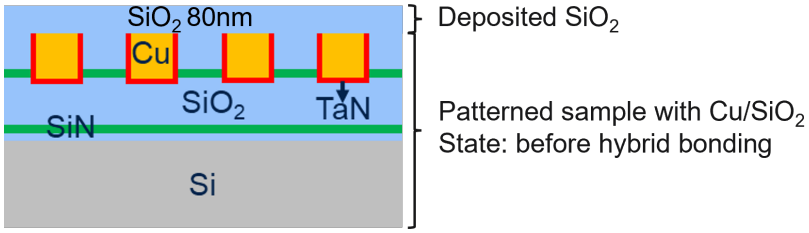

Figure 3.14: Schematic cross section of the sample used for preliminary evaluation of Cu diffusion when SiO_2 is directly deposited on Cu pads.

confirmed that this delamination behaviour is representative on other pads. No similar behaviour of interface delamination was reported in the literature when studying Cu diffusion into SiO_2 [43] [173]. Possible explanation could be related to the size of the Cu pads as well as the thickness of SiO_2 used for our study (80nm). Usually, the studies reported in the literature include $Cu/SiO_2/Si$ stacks, which are different from our current study with a free SiO_2 surface to deform. It is most probable that interface delamination occurred during the thermal annealing step. Beside the fact that Cu diffuses in SiO_2, a thermal stress is generated due to the different CTE between Cu and SiO_2, which could explain the presence of the delamination.

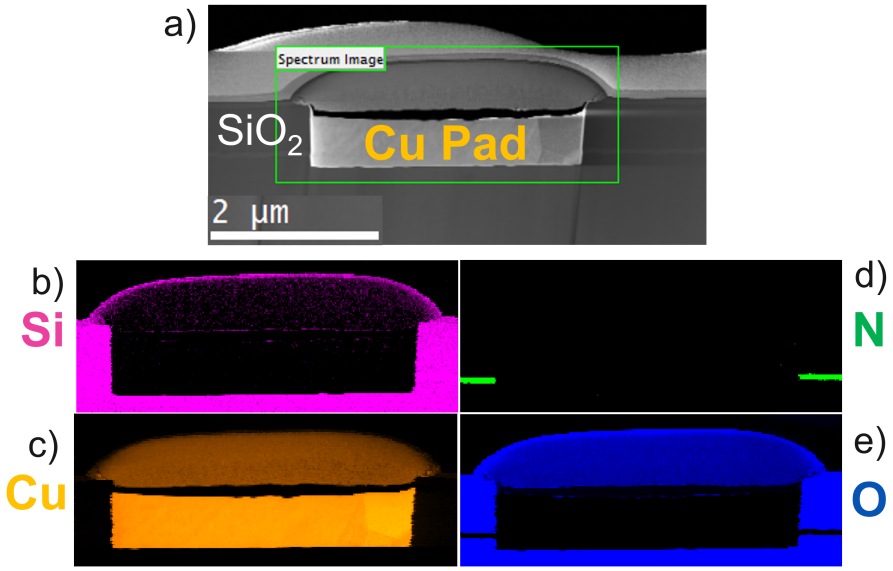

Figure 3.15: a) TEM image at the Cu/SiO_2 interface when SiO_2 is deposited on Cu pads showing a gap between Cu pads and SiO_2 and a bump. EELS mapping results for the following element: b) silicon (Si), c) copper (Cu), d) nitrogen (N) and e) oxygen (O) after annealing at 380 °C - 2 h.

Based on our preliminary study, it is confirmed that Cu does diffuse in SiO_2 for the specific materials used in our hybrid bonding process when it is directly deposited on SiO_2 similar to the reported studies in the literature for BEoL cases. In the following section, we will go through the physics of atomic diffusion.

3.4.1.2 Physics of atomic diffusion

In this section, we will present the physics of atomic diffusion into the dielectric as reported in the literature. We will rely on the one dimensional equation in order to define the most adequate characteristics for experimental samples and thermal budgets for the hybrid bonding study. In one dimension, Fick's first law is given to describe the net flux of metal atoms from a metallic source (our case: Cu) inside a dielectric (our case: SiO_2) [175]:

$$f(x,t) = -D\frac{\partial \rho(x,t)}{\partial x} \tag{3.10}$$

where f is the flux, defined as the number of metal atoms passing through a unit area and per unit time, ρ is the concentration of metal atoms in cm^{-3}, $\frac{\partial \rho(x,t)}{\partial x}$ is the concentration gradient that is the driving force for diffusion and D is the diffusion coefficient in cm^2/s.

The diffusion coefficient can be written as an Arrhenius form:

$$D = D_0\ exp\left(\frac{E_a}{kT}\right) \tag{3.11}$$

Where D_0 is the pre-exponential factor, E_a is the activation energy for atom motion inside the dielectric (eV), k is the Boltzmann constant and T is the temperature (K). The diffusion coefficient is therefore dependent on temperature.

To satisfy the mass balance requirements gives Fick's second law:

$$\frac{\partial \rho(x,t)}{\partial t} = -\frac{\partial f(x,t)}{\partial x} = \frac{\partial}{\partial x}\left(D\frac{\partial \rho(x,t)}{\partial t}\right) \tag{3.12}$$

The equation 3.12 can be simplified assuming that D is independent of x to the following form:

$$\frac{\partial \rho(x,t)}{\partial t} = D\frac{\partial^2 \rho(x,t)}{\partial^2 x} \tag{3.13}$$

The higher the diffusion term is, the faster an atom can migrate and accumulate inside a dielectric. An analytical solution can be derived from equation 3.13, assuming the below boundary conditions, which is called the predeposition diffusion:

$$\rho(x, t=0) = 0 \quad \rho(x=0,t) = \rho_s \quad \rho(x=d,t) = 0 \tag{3.14}$$

where ρ_s is the fixed metal concentration at the metal-dielectric interface and d is the dielectric thickness. ρ_s is usually assumed to be the maximum solubility of metal inside the dielectric. So, for the case of Cu in SiO_2, ρ_s is $10^{18}\ at.cm^{-3}$ [176]. Solving equation 3.13 with the above boundary conditions gives equation 3.15:

$$\frac{\rho(x,t)}{\rho_s} = 1 - erf\left(\frac{x}{2\sqrt{Dt}}\right) \tag{3.15}$$

In the above equation, $\sqrt{Dt}$ is the characteristic diffusion depth and erf is the error function. To get the sample characteristics for our hybrid bonded samples, equation 3.15 will be used to estimate the relative concentration $\frac{\rho(x,t)}{\rho_s}$ based on the known diffusion coefficient of Cu in SiO_2 reported in the literature.

3.4.1.3 Previous Cu thermal diffusion studies at the hybrid bonding level

Cu thermal diffusion studies are only reported for the Cu/SiO_2 hybrid bonding configuration by the team at STMicroelectronics/CEA-LETI/IMS, which is identical to the integration studied in my PhD. In fact, Jourdon used the ToF-SIMS technique to identify any Cu atomic diffusion with a concentration as low as 10^{17} $at.cm^{-3}$ [44]. The analysis was performed on samples where the bottom Cu patterned wafer is bonded to a full sheet SiO_2 top wafer. The top wafer is composed of successive SiN/SiO_2 layers. Two thermal budgets were studied: 400 °C-2 h and 400 °C-16 h. This study concluded that no Cu thermal diffusion occurs at the Cu/SiO_2 hybrid bonding interface with a concentration higher than 10^{17} $at.cm^{-3}$. Although Cu was observed on the surface of the sample, this was assessed to a probable Cu contamination when handling the samples.

In the following section, the potential risk of Cu thermal diffusion at the Cu/SiO_2 interface is studied in details using characterization techniques having higher precision than ToF-SIMS.

3.4.1.4 Results of Cu atomic diffusion

Test conditions and structures of interest

Two thermal budgets are defined: the first corresponding to the bonding annealing condition for the electrical test vehicle (380 °C-2 h) while the second is excessive annealing at 400 °C-16 h to be in line with the previous study [44]. Using the lowest and highest diffusion coefficients of Cu in SiO_2 found in the literature for the two stress conditions, the relative concentration ($\frac{\rho(x,t)}{\rho_s}$) is calculated along the SiO_2 depth as shown in figure 3.16.

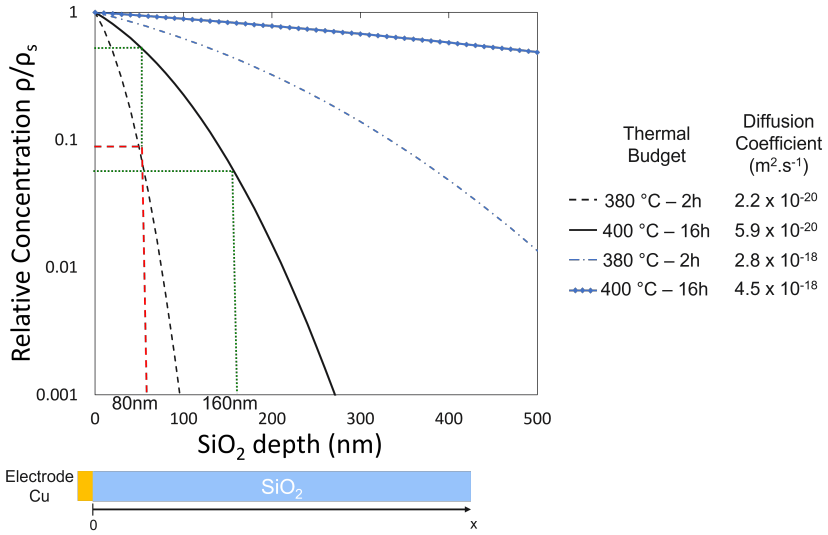

Figure 3.16: Relative concentration profiles of Cu in SiO_2 depth calculated using the lowest and highest diffusion coefficients found in the literature for the different annealing conditions [43] [173]. 0 corresponds to the Cu/SiO_2 interface position.

Based on the calculations shown in figure 3.16, we can clearly conclude that any Cu diffusion in an SiO_2 layer with a relative concentration higher than 0.1 would be notice-

able under the lowest thermal budget of 380 °C-2h for SiO_2 thickness thinner than 80 nm. This is shown by the red dotted lines in figure 3.16. The relative concentration of 0.1 is used as the criterion to get a concentration of Cu in SiO_2 higher than 10^{17} $at.cm^{-3}$. This result allows to define the SiO_2 thickness at the hybrid bonding interface above the HBM Cu pads and that should not exceed 80 nm. If there any Cu diffusion at the interface to the SiO_2 top layer, Cu will rapidly diffuse through the Si layer and reach the top surface since the diffusion coefficient of Cu in Si is as high as 2.2×10^{-10} $m^2.s^{-1}$ at 380 °C [177] [42].

The process of the samples used for the Cu atomic diffusion study consists in bonding two 300 mm wafers. A schematic description is shown in figure 3.17. The bottom wafer is Cu patterned with 1 metal line with the CPM8 mask with pad width between 3.3 and 5.4 μm. The top wafer is composed of either 80 nm of SiO_2 (figure 3.17 (a)) or three layers combining SiO_2 (80 nm) – SiN (60 nm) – SiO_2 (80 nm) as shown in figure 3.17 (b). The sample with SiN will serve as a BEoL reference since SiN has been shown to be an excellent barrier to Cu diffusion for standard BEoL configuration [178] [179]. Specific surface preparation are done to ensure successful bonding of a hybrid wafer with a full sheet SiO_2 one.

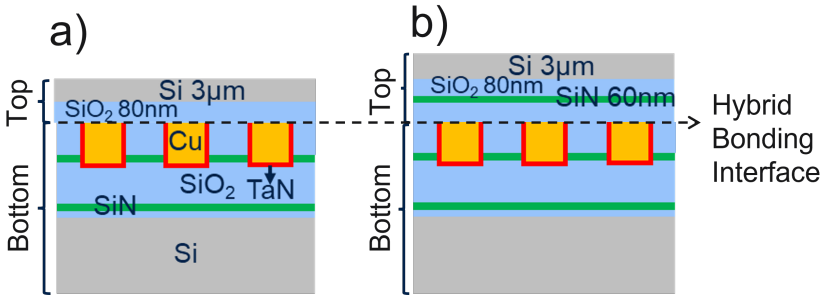

Figure 3.17: Schematic cross sections of the hybrid bonded samples used for the thermal analysis study: a) with 80 nm of SiO_2 on top and b) with three layers of SiO_2-SiN-SiO_2 on top (to be used as a BEoL reference).

After hybrid bonding and bonding anneal at 380 °C-2 h, the top wafer is thinned down to 3 μm to simulate the residual Si thickness for some image sensors developed at STMicroelectronics. After thinning, to simulate the final anneal of the image sensor integration, an additional budget of 380 °C-2 h is applied. At this stage, all the samples have undergone a total thermal anneal of 380 °C-4 h. Additional high aging budget of 400 °C-16 h is performed on some samples to be in line with the previous study by Jourdon [44].

Experimental methods

Two methods are used to quantify any Cu diffusion through the hybrid bonding interface that are total X-ray fluorescence (TXRF) and liquid phase decomposition – inductively coupled plasma mass spectroscopy (LPD-ICPMS). By these techniques, the Si surface of the top thinned wafer is analyzed.

For the TXRF method, an X-ray beam irradiates the surface to be analyzed with a low incident angle ($< 0.1°$), below the critical angle. Incident X-rays excite atoms of the

sample. These excited atoms go back in an equilibrium state with an electronic transition emitting X-ray photons. X-rays are totally reflected with a material penetration of only $\sim 4\ nm$. Therefore, this technique allows principally the characterization of the near wafer surface. The detection limit for Cu is around $10^{10}\ at.cm^{-2}$ for the average value [180].

LPD-ICPMS is a technique used to identify ¨any¨ wafer contaminants. For this technique, a special chemical solution based on HF/HNO_3 is poured on the top of the wafer. Different Si thicknesses can be etched depending on the exposure duration. In this study, LPD-ICPMS analysis was done for 1 μm depth under the Si surface. The collected solution is then analyzed by ICPMS [181]. LPD-ICPMS gives an average of contamination in Si thickness with a detection limit of $3 \times 10^{10}\ at.cm^{-2}$, lower than the TXRF technique.

The two methods used are complementary since TXRF allows measurements over the surface while LPD-ICPMS gives an average concentration along the 1 μm Si depth. One sample is used per anneal condition and by analysis technique.

Experimental results of Cu atomic diffusion

The average results of Cu concentration obtained by TXRF and LPD-ICPMS are shown in table 3.6. The analysis of the results is done at two levels: (a) on the global level of Cu concentration found and (b) on a comparison between hybrid bonded samples and reference ones with SiN.

The Cu level lies between $0.15 \times 10^{12}\ at.cm^{-2}$ and $0.27 \times 10^{11}\ at.cm^{-2}$, which is at least one order of magnitude higher than the detection level of these characterization methods. Those results must be compared to the classical Cu level measured on backside Si substrate for backend samples at STMicroelectronics fab that is around $10^{11}\ at.cm^{-2}$. The concentrations obtained on the hybrid bonded samples are nearly one decade higher indicating the presence of Cu diffusion across the hybrid bonding interface. Whatever the split conditions, the $10^{12}\ at.cm^{-2}$ Cu concentration level is in tolerable amount as it should have a limited impact on performance as showed by Gonella who used TDDB to study the impact of different levels of Cu contamination on the dielectric lifetime [182] [183].

Table 3.6: TXRF and LPD-ICPMS average Cu concentration results obtained on the hybrid bonded samples after the different test conditions.

Top Sample		SiO_2 only		$SiO_2 - SiN - SiO_2$	
Total anneal conditions		380 °C-4h	380 °C-4h + 400 °C-16h	380 °C-4h	380 °C-4h + 400 °C-16h
Results of Cu concentration ($\times 10^{12}\ at.cm^{-2}$)	TXRF	1.03	2.72	0.9	0.95
	LPD-ICPMS	0.18	1.7	0.15	0.19

Moving into details, after annealing at 380 °C-4h, the Cu concentration obtained on the samples with SiO_2 only and with SiN are similar. This suggests that Cu in direct contact of SiO_2 at the hybrid bonding interface does not produce more Cu diffusion as compared to the sample with the 60 nm SiN. Previous study at the BEoL interconnect highlighted a level of Cu concentration by TXRF around 4×10^{12} $at.cm^{-2}$ through a 50 nm SiN after annealing up to 400 °C-1h that is consistent with our results [179]. For additional stress conditions of 400 °C-16h, the Cu concentration obtained on the sample with only SiO_2 is higher than the sample with SiN. The lower Cu concentration on the sample with SiN can be explained by its twice higher SiO_2 thickness. From figure 3.16 and for the 400 °C-16h condition, we can observe that increasing the SiO_2 thickness from 80 to 160 nm can decrease the relative concentration at surface up to one order of magnitude particularly with the lowest diffusion coefficient. This is illustrated by the green dotted lines. It would be pertinent to conduct atomic diffusion studies with the same total height of dielectric (including SiN) for the two samples with and without the dielectric barrier to verify this hypothesis.

For the case of SiO_2 directly deposited on Cu pads, a Cu/SiO_2 interface delamination was observed in addition to the presence of Cu diffusion diffusion in SiO_2 (check section 3.4.1.1). In order to study the Cu/SiO_2 interface state for the hybrid bonding case, TEM cross section is done on the sample having only SiO_2 on the top wafer and that has been annealed at 400 °C for 16 h. The results are shown in figure 3.18. In figure 3.18 (b), a zoom at the Cu/SiO_2 hybrid bonding interface (red rectangle in figure 3.18 (a)) shows no sign of any interface delamination. It is clear that the Cu/SiO_2 hybrid bonding interface is thermodynamically stable even after annealing at 400 °C for 16 hours.

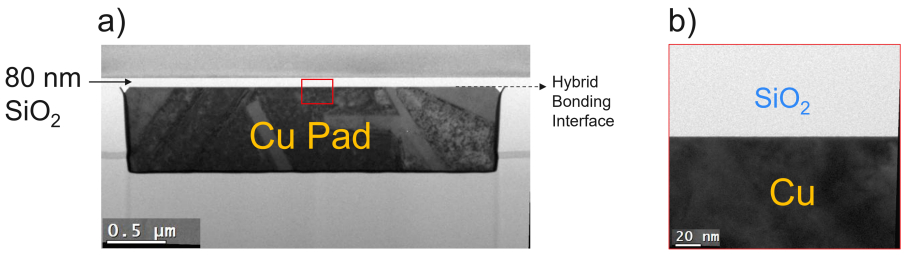

Figure 3.18: a) TEM cross section on the hybrid bonded sample having only SiO_2 on top wafer from the CPM8 test vehicle after thermal annealing at 400 °C for 16 h and b) zoom at the Cu/SiO_2 interface (red rectangle).

The results of the experimental characterizations by TXRF and LPD-ICPMS prove that the Cu/SiO_2 hybrid bonding has similar ¨Cu contamination¨ after thermal annealing as compared to the sample with SiN dielectric barrier. In addition, the Cu/SiO_2 hybrid bonding interface is thermodynamically stable after annealing at 400 °C for 16 hours. As mentioned earlier, a 3 nm Cu_2O layer was evidenced in the region where Cu is facing SiO_2 which could act as a barrier to Cu diffusion in SiO_2. The results obtained in this section go in the favor of validating the barrier characteristics of the Cu_2O present at Cu/SiO_2 hybrid bonding interface. We think that the 3 nm Cu_2O layer is at least of similar characteristics to suppress Cu thermal diffusion as the 60 nm SiN layer.

3.4.1.5 Discussion on the Cu_2O formation hypotheses

The Cu_2O formation could be explained by the following possible hypotheses:

1. The first hypothesis could be related to the fact that after bonding, part of the HBM pad will be in contact of SiO_2 due to the presence of misalignment. SiO_2 can be the source of oxygen element that might lead to the formation of Cu oxide. The negative enthalpy of formation ($-\Delta H_f$) for the CuO and Cu_2O oxides per oxygen atom are 155.2 $kJ/mole$ and 167.4 $kJ/mole$ respectively, which is much smaller than that of SiO_2 (910.4 $kJ/mole$) [184]. Therefore, from the thermodynamic point of view, Cu should not reduce the SiO_2 to form a Cu oxide when SiO_2 is deposited on Cu. Similarly for the hybrid bonding process, we expect that Cu in direct contact of SiO_2 should not reduce the oxygen from SiO_2 to form a Cu oxide layer. The hypothesis of Cu_2O formation originated from oxygen in SiO_2 is less probable. This also suggests that the Cu_2O/SiO_2 interface present at the hybrid bonding interface will be thermodynamically stable as no interaction is expected between these layers.

2. Another hypothesis could be linked to that after CMP and before bonding, HBM pads are exposed to the ambient atmosphere and in particular oxygen, which could lead to Cu oxidation. The Cu_2O was previously observed in the case of blanket Cu/Cu bonding [185]. This interfacial copper oxide present at the Cu-Cu interface diffuses along the Cu-Cu bonding interface after annealing that allows Cu-Cu contact [185]. In the case of Cu/SiO_2 hybrid bonding, and in the region where Cu HBM is facing SiO_2, we think that the Cu_2O is still present after bonding annealing. The Cu_2O thickness reported at the Cu-Cu interface is around 4 nm [185], which is close the thickness illustrated at the Cu/SiO_2 hybrid bonding interface by EELS [45]. Although in the literature the Cu oxide phase at Cu/Cu interface was concluded based on the electron density drop, we think that EELS is the adequate technique to use to conclude on the Cu oxide phase with a thickness of several manometers.

Having all this in mind, we think that the formation of the Cu_2O layer is linked to the second hypothesis particularly to Cu oxidation after CMP and before bonding. In the misalignment region, where Cu HBM is facing SiO_2, we believe that the Cu_2O layer is still present as identified by the EELS analysis [45].

One might suspect the instability of the Cu oxide layer as some studies on the oxidation of Cu thin film showed that Cu_2O is thermally unstable above 300 °C where a CuO phase should exist after several hours of annealing [186]. This phase transition can be mediated by equation 3.16 [187]:

$$Cu_2O + \frac{1}{2}O_2 \rightarrow 2CuO \tag{3.16}$$

In our specific case, even after bonding annealing at 380 °C, the Cu_2O is present. A possible explanation is that, after the hybrid bonding step, no oxygen rich environment is present in contrary to the studies previously reported in the literature [186] [187]. The Cu_2O will be thermally stable when no interaction exists with an oxygen rich environment. This further validates that SiO_2 does not behave as a source of oxygen element, which is in line with the reported enthalpy of formation between Cu_2O and SiO_2.

3.4.2 Field-enhanced ion diffusion

3.4.2.1 Physics of ionic diffusion

After evaluating the atomic thermal diffusion, it is important to study the field-enhanced ionic diffusion that have the major impact on the device lifetime. In the presence of an electric field, an additional driving force for ion migration inside the dielectric will occur. The one-dimension flux of atomic/ionic diffusion at a position x, after a time of annealing t is given by equation 3.17 [188]:

$$f(x,t) = -D\frac{\partial \rho(x,t)}{\partial x} + \frac{qDE(x,t)\rho(x,t)}{kT} \tag{3.17}$$

Where the left part is the thermal diffusion term previously presented, q is the electric charge, E(x,t) is the effective electric field that includes both the external field and the ionic field from the penetrated ions, D represents the metal-ion diffusivity, k is the Boltzmann constant and T is the temperature. At low electrical testing temperature below 250 °C, the atomic diffusion coefficient of Cu in SiO_2 is below 2×10^{-23} $m^2.s^{-1}$ and we can expect that the ionic diffusion dominates the thermal diffusivity term. Therefore, the stress conditions for the ionic diffusion studies will be at temperatures below 250 °C.

3.4.2.2 Previous studies on Cu ionic diffusion at the hybrid bonding interface

Cu ionic diffusion has been studied for both configurations with a barrier dielectric (SiCN) and an oxide dielectric (SiO_2) at the hybrid bonding level. For a dielectric barrier at the interface with SiCN, Hou reported a Poole-Frenkel conduction mechanism using a comb-comb like structures [189]. In addition, by plotting the current density vs. temperature at electrical fields of 1.5 and 2.5 MV/cm, the author showed a deviation from the expected linear relationship when the electrical field and temperature are higher than 1.5 MV/cm and 200 °C respectively. This indicates the presence of Cu drift under these conditions. Nevertheless, the study concluded that the hybrid bonding process using SiCN as bonding dielectric material is robust.

Meanwhile, previous studies of Cu field enhanced diffusion for the Cu/SiO_2 configuration, which is identical to the integration in my PhD, showed no sign of Cu ionic diffusion up to a stress of 20 V - 30 min and temperature of 250 °C for a 6.84 μm pitch [45]. Moreau performed bias temperature stress (BTS) coupled with triangular voltage sweep (TVS) measurements on a MIS-like structure adapted to hybrid bonding with a 3.42 μm wide HBM pads. No particular peak or hump could be identified whatever the BTS/TVS conditions used suggesting no diffusion of any ionic species (Cu^+, Na^+, $K^+ \dots$). The author linked the lack of ionic diffusion to the presence of a $\sim$ 3 nm Cu_2O layer at the Cu/SiO_2 interface identified by EELS, and that is believed to act as a barrier to Cu diffusion.

In the following section, new electrical characterizations are performed for the Cu/SiO_2 hybrid bonding configuration with pitch down to 1.44 μm (720 nm HBM width). The aim is to validate the observations made on the Cu ionic diffusion at the Cu/SiO_2 hybrid bonding interface with the reduction of the HBM size. Most importantly, products are subject during their lifetime to thermal stresses. Any thermal instability of the Cu_2O layer could lead to serious degradation of the insulation properties of dielectric. Hence,

a study is performed in the following section on the stability of the Cu_2O layer after thermal aging in response to Cu ionic diffusion.

3.4.2.3 Results of Cu field-enhanced ionic diffusion

3.4.2.3.1 Structures of interest

MIS-like structure

The hybrid bonded metal insulator semiconductor (MIS) test structure adapted to hybrid bonding is illustrated in figure 3.19, that is identical to the structure presented in [45]. It consists of bonding two 300 mm wafers. The top wafer is composed of 4 metal layers excluding the hybrid bonding level (HBV and HBM) from the $S\&H$ test vehicle. The bottom wafer is made of full sheet 40 nm SiO_2 layer deposited on a Si substrate. The main interests of this structure summarize as following:

1. The maximized contact area between Cu and SiO_2 at the hybrid bonding interface that makes it suitable to Cu diffusion analysis. The Cu pad width at the HBM level ranges from 3.42 down to 0.72 μm. For our study, we will focus on the 0.72 μm wide HBM width.

2. This structure is not affected by overlay since breakdown should always occur in the 40 nm SiO_2.

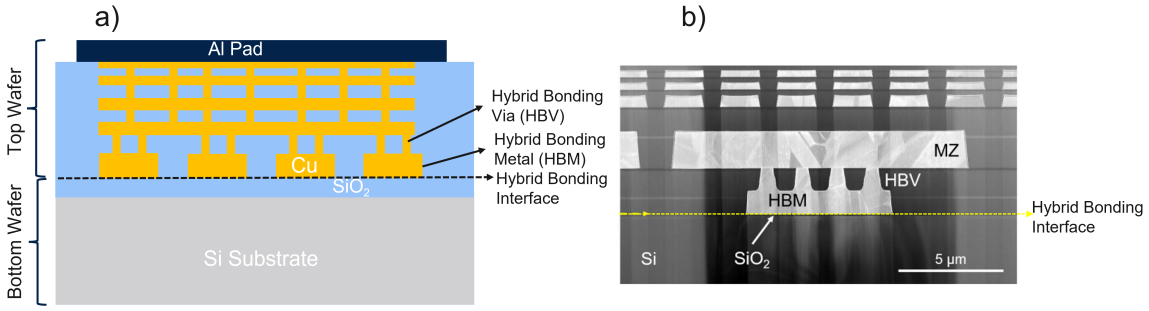

Figure 3.19: (a) Schematic view and b) STEM cross section of the hybrid bonded MIS structure. The SiO_2 thickness at the bottom wafer is 40 nm [45].

The main limitation of this structure is a possible impact of the Si substrate when studying Cu diffusion.

Comb-serpentine structure

The second structure used for Cu ionic diffusion is the comb-serpentine as shown in figure 3.20. The HBM width is 720 nm. This structure is similar to a Metal Insulator Metal (MIM) design. This design also maximizes the Cu/SiO_2 contact area at the hybrid bonding interface [44]. Previous studies by Jourdon showed the pertinence of the comb-serpentine structure for breakdown analysis at hybrid bonding interface as compared to

the comb-comb structure. In fact, for the comb-comb structure, the most critical distance is at the dielectric layer at the Al pad level and not between both combs. This leads to a dielectric breakdown at Al pad level instead of the hybrid bonding interface [44].

The theoretical distance between the comb and serpentine (d) is 252 nm. During the bonding step, misalignment could occur that should be considered to calibrate the d value as following:

$$d = 252 - x \tag{3.18}$$

where x is the overlay in X direction due to the particular design of this structure. The main limitation of this structure is the correct estimation of the distance taking into account the overlay measurements errors, which could lead to errors when applying the electrical field.

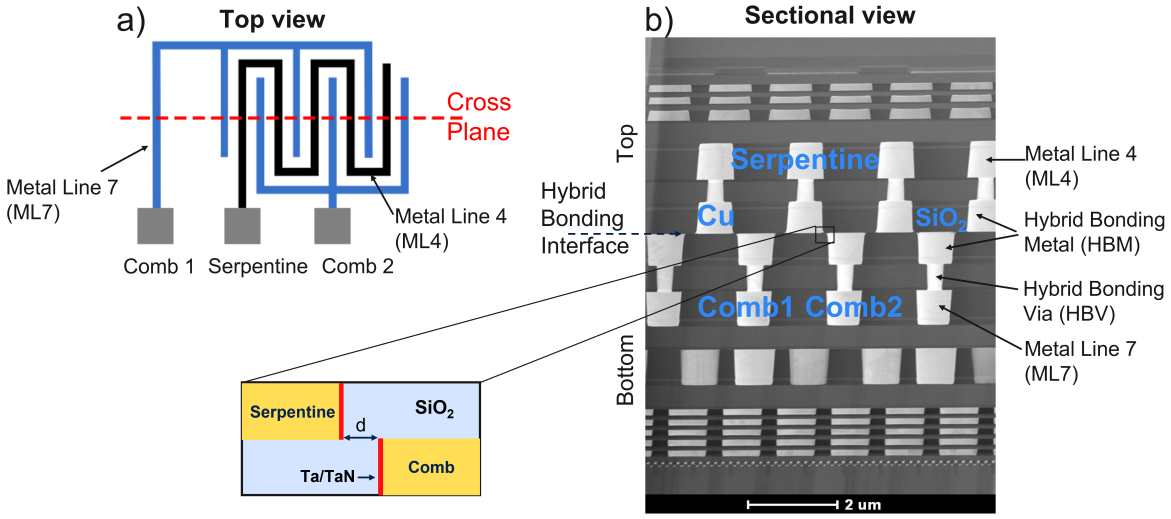

Figure 3.20: (a) Top schematic view and b) TEM cross section of the hybrid bonded comb-serpentine test vehicle with pad width of 720 nm. The theoretical distance d is 252 nm.

3.4.2.3.2 Experimental methods and test conditions

BTS/C-V

The first experimental method consists of combining BTS with capacitance voltage (C-V) measurements. This experimental method only applies to the MIS structure reported in section 3.4.2.3.1, figure 3.19. C-V measurements are performed at a first step by applying a polarization between -10 and +10 V, which will serve as a reference. Then, a BTS is applied to force Cu ion diffusion into the dielectric. After that, a C-V measurement is again performed to track any ion drift. The presence of diffused ions would produce a shift in the flat band voltage V_{FB}, which is the voltage at which the surface charge density at the SiO_2/Si is equal to zero [190] [173]. This technique can possibly be used to conclude on the Cu diffusion coefficient for the Cu/SiO_2 integration when

comparing between the experimental and numerical results [173].

BTS/TVS

The second technique is a combination between BTS and TVS, which was used by Moreau in his study [45]. This method is applied to the comb-serpentine structure with HBM width of 720 nm shown in figure 3.20. First, TVS measurements are performed for reference. Then, a BTS is applied to force Cu ion diffusion into the dielectric. If any Cu diffusion takes place during BTS, this will be directly evidenced by ionic peaks on I-V recorded during TVS. BTS/TVS method can detect metallic diffusion densities as low as about $10^9\ cm^{-2}$ [191].

The test conditions are shown in table 3.7.

Table 3.7: BTS, TVS and C-V test conditions for Cu ionic diffusion studies.

Structure	MIS-like Structure		Comb-Serpentine Structure	
Test	BTS	C-V	BTS	TVS
Test Sequence	Test 1	Test 2	Test 1	Test 2
Temperature	200 $°C$	200 $°C$	200 $°C$	200 $°C$
Bias	±10 V	up to 15 V	±15 V	up to 2.67 MV/cm
Duration	-	up to 50 min	-	up to 30 min
Ramp rate	100 mV	-	250/125 mV/s	-
Sweep direction	-10 → 10 V	-	-15 → 15 → -15 V	-

3.4.2.3.3 Results of Cu ionic diffusion: 1.44 μm pitch

BTS/C-V results

BTS/C-V measurements are performed on MIS structures with a volume of 12 samples to check the shift of the flat band voltage after the different stress conditions. A typical result example is shown in figure 3.21 on structure with HBM width of 720 nm. A shift of V_{FB} is clearly observed with increasing BTS time from the C-V curves (figure 3.22 (a)).

To study if these variations come from the ionic charges trapped into the dielectric, the leakage current variations with BTS is studied in figure 3.22 (b). No leakage current increase can be seen with the different stresses. This leads to the conclusion that the V_{FB} shift is mostly not related to ionic diffusion inside the dielectric. Possible explanation of the shift is the polarization of the dielectric that is a typical behavior when an electric field is applied leading to the reorientation of the positive and negative charges inside the dielectric [192]. Similar behaviour of V_{FB} shift not related to Cu diffusion was for example reported in [193]. The application of higher stress time may lead to abnormal C-V characteristics and to the dielectric breakdown phenomenon, therefore inconclusive results on the impact of Cu diffusion.

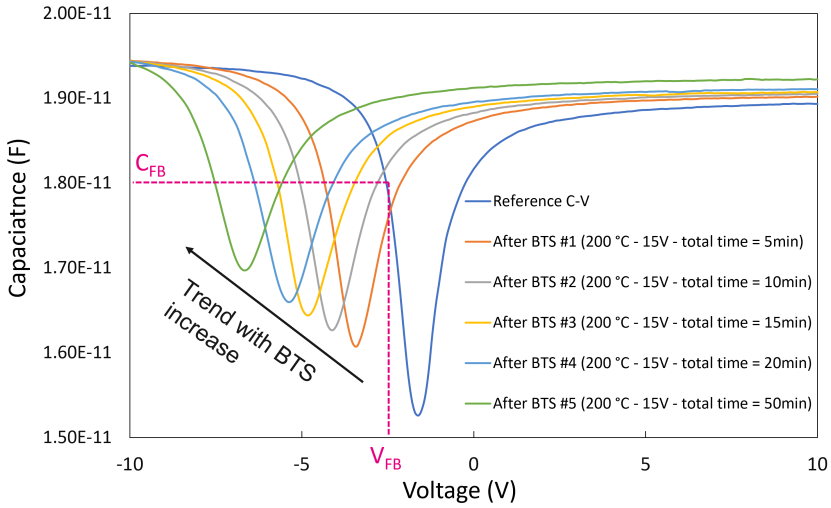

Figure 3.21: C-V results between -10 and +10 V after the different BTS tests at 15 V, 200 °C and up to 50 min on the MIS type structure with HBM width of 720 nm.

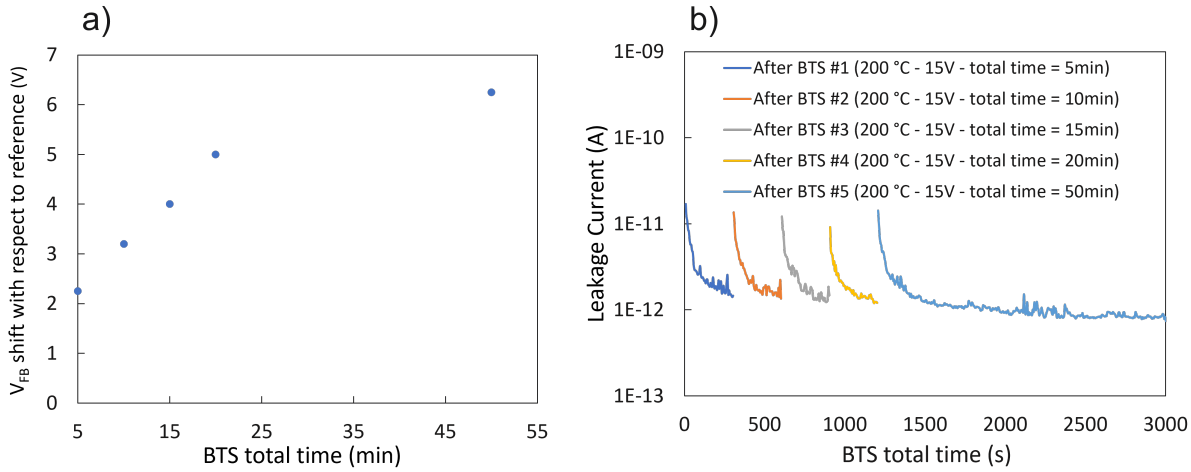

Figure 3.22: a) V_{FB} shift from the C-V curves presented figure 3.21 and b) leakage current variations with increasing BTS times with stress at +15V and 200 °C.

For our hybrid bonding integration, the BTS/C-V method does not allow to conclude on a possible Cu ionic diffusion at the Cu/SiO_2 interface. In fact, it is not possible to separate the V_{FB} shift linked to dielectric polarization from Cu diffusion. In the following section, the BTS/TVS method is on the MIM structure is studied.

BTS/TVS results

BTS/TVS characterizations are performed on a volume of 12 samples with MIM structure (comb-serpentine structure shown in figure 3.20 with HBM width of 720 nm) that involves studying the Cu ionic drift between adjacent HBMs at the hybrid bonding interface. A typical example is shown in figure 3.23. No particular ionic peak can be identified whatever the BTS/TVS conditions which signifies no diffusion of any ionic species (Cu included). This result is in line with the electrical demonstration of the lack of Cu ionic diffusion done on MIS structure with much higher HBM width (3.42 μm) [45]. We can

conclude that, with pitch reduction down to 1.44 μm pitch, the Cu/SiO_2 hybrid bonding configuration is still immune to Cu ionic diffusion.

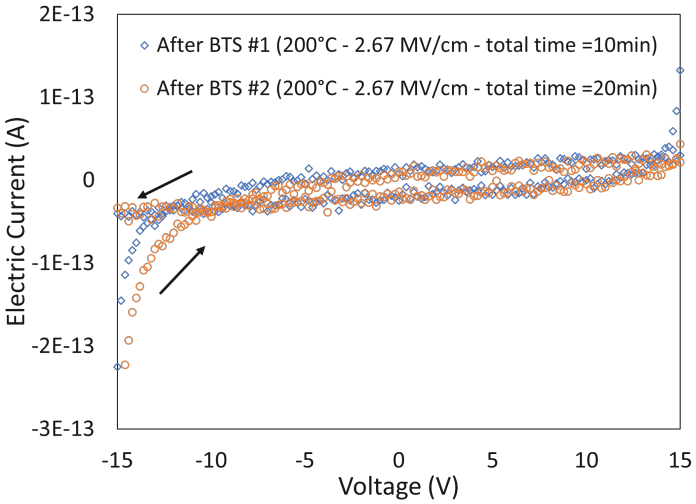

Figure 3.23: Typical TVS results on the comb-serpentine structure after different BTS tests at 200 °C and 2.67 MV/cm up to 20 min using a sweep rate of 250 mV/s for the 720 nm wide HBM on the $S\&H$ test vehicle. Reference data (before any BTS) has been subtracted from each TVS data after the different BTS tests in order to highlight a potential ionic diffusion after the different stresses.

No Cu ionic diffusion occurs at the Cu/SiO_2 hybrid bonding interface up to stress of 2.67 MV/cm with HBM width down to 720 nm using the BTS/TVS method, which can detect metallic diffusion densities as low as 10^9 cm^{-2}. The presence or not of Cu ionic diffusion at the interface is related to the barrier characteristics of either the Cu_2O or the dielectric barrier, for instance SiCN. Previous observation for the $Cu/SiCN$ hybrid bonding configuration showed an increase in the leakage current at 200 °C and for fields above 1.5 MV/cm that was linked to a Cu ionic drift [189]. Therefore, we believe that the self-formed 3 nm Cu_2O layer at the Cu/SiO_2 hybrid bonding interface is at least as efficient as the SiCN in decelerating the Cu ionic diffusion at the hybrid bonding interface.

3.4.2.4 Discussion on Cu ionic diffusion with pitch reduction

To study possible impact on the integrity of the Cu/SiO_2 hybrid bonding interface with pitch reduction, BTS/TVS characterizations are performed. The structures used for this analysis are similar to the one in figure 3.20, but with lower HBM width and lower spacing (d) between the comb and serpentine as shown in figure 3.24. Two structures are designed and used for this analysis that were embedded in the TEDDY-UFP electrical test vehicle: the first with an HBM width of 0.45 μm and a spacing of 0.18 μm and the second with an HBM width of 0.405 μm and a spacing of 0.16 μm. The TVS results using a sweep rate of 125 mV/s after BTS at 200 °C, 2.67 MV/cm and up to 30 min are shown in figure 3.24.

For the structure with HBM width of 0.45 μm, a small shift of the electrical current (see red dotted zone in figure 3.24 (a)) is evidenced after the third BTS in the region of low

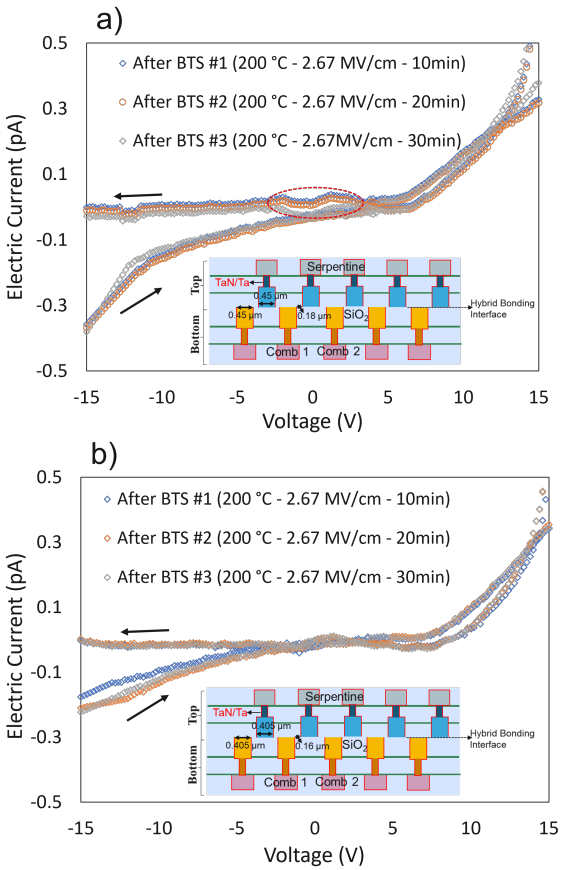

Figure 3.24: Typical TVS results using a sweep rate of 125 mV/s after BTS test at 200 °C, 2.67 MV/cm and up to 30 min done one comb-serpentine structure with a) HBM width of 0.45 μm and b) HBM width of 0.405 μm on the TEDDY-UFP test vehicle. Reference data (before any BTS) has been subtracted from each TVS data after the different BTS tests to highlight a potential ionic diffusion after the different stresses.

electric potentials (between ±3 V). The electric current deviation being below 0.01 pA, we think it is not linked to the presence of ionic diffusion since any Cu ionic diffusion is usually associated with much higher peaks [194] [195]. The cause of this deviation remains unclear and it might be related to the measurement errors. Moreover, this particular behaviour was only observed on a single sample between the 12 tested samples with 0.45 μm wide HBM width. For the samples with HBM width of 0.405 μm, no ionic peaks can be identified after the different BTS times, promoting that no Cu ionic diffusion takes place as shown exemplary in figure 3.24 (b). The Cu/SiO_2 hybrid bonding interface remains immune to ionic diffusion even with HBM size reduction down to 0.405 μm. We believe that the mechanism of barrier formation for such small possibly monocrystalline Cu pads is identical to larger polycrystalline ones. Therefore, this suggests that the formation of the Cu_2O barrier layer at the interface is independent of the HBM size and microstructure.

In the following section, a study is done on the stability of Cu_2O as a barrier to Cu diffusion after thermal aging for the 1.44 μm pitch samples.

3.4.2.5 Thermal stability of the Cu_2O layer

The cuprous oxide was found previously to be thermally unstable when annealing above 300 °C for several hours where the cupric oxide (CuO) could form [186] [196]. It is therefore of much importance to study whether any thermal instability of the Cu_2O layer present at the Cu/SiO_2 hybrid bonding interface after long-term storage might cause reliability issues. The wafer which was placed at HTS at 175 °C for 4000 h is used for this analysis. Typical TVS results after BTS on the comb-serpentine structure with HBM width of 720 nm are shown in figure 3.25 (a) and (b) for the 250 and 125 mV/s sweep rates respectively. No particular peak can be identified after the different stress conditions whatever the voltage sweep rate. This means that there is no ionic diffusion between two pads across the hybrid bonding interface. Thus, there is no ionic Cu diffusion across the interface between adjacent Cu pads. These results are identical to our electrical characterizations done on samples before storage suggesting the same barrier characteristics of the Cu_2O layer before storage.

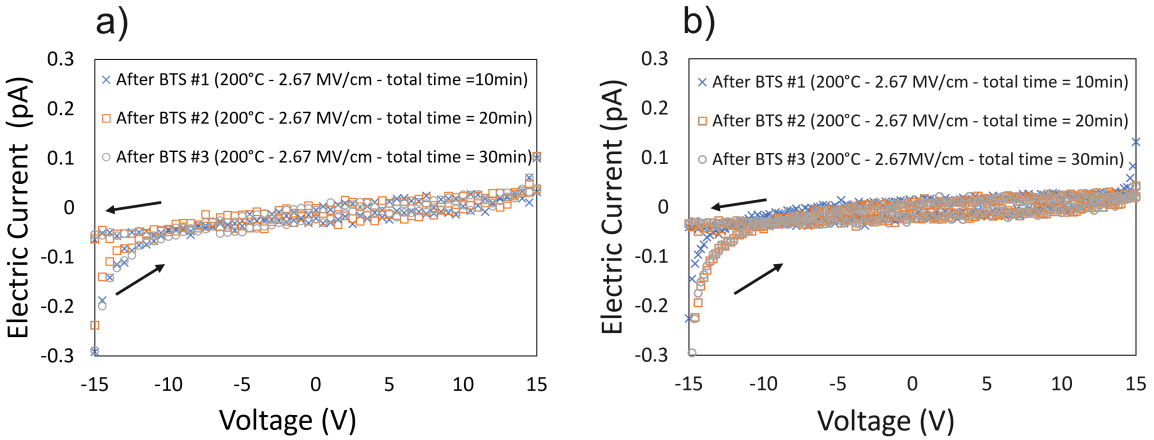

Figure 3.25: Typical TVS results on the comb-serpentine structure with 720 nm wide HBM on the $S\&H$ test vehicle having HTS for 4000 h after different bias temperature stress (BTS) tests at 200 °C and 2.67 MV/cm up to 30 min using a sweep rate of a) 250 mV/s and b) 125 mV/s.

In order to study any change of the Cu_2O phase identified before storage, EELS is used to chemically analyze the hybrid bonding interface state after long term storage of the device. The EELS results after HTS at 175 °C during 4000 h are shown hereafter. In figure 3.26 (a), a TEM cross section picture at the Cu/SiO_2 interface is presented along with the line scan (green line) performed for the EELS analysis. Two sites are extracted from this line scan: (1) inside Cu pads and (2) at Cu/SiO_2 interface. In figure 3.26 (b), the $Cu-L_{2,3}$ ionization edge for the 2 sites is given. The EELS Cu spectrum at position 1 corresponds to reported Cu crystalline. At the interface, the Cu spectrum exhibits a small white line around 936 and 955 eV, which is typical of an oxidation state. The positions of the peaks are linked to a typical cuprous oxide phase (Cu_2O). Using a digital micrograph (Gatan©) software, a multiple linear least squares (MLLS) fitting routine is used to map the different spectra phases along the EELS line profile using the two identified signals of metallic Cu and Cu_2O at positions 1 and 2 respectively [197]. The results are shown in figure 3.26 (c). The blue line describes the intensity of Cu_2O across the Cu/SiO_2 hybrid bonding interface while the orange line profile is the Cu metal. A clear peak of Cu_2O

is observed at the interface. Measuring the full-width half-maximum (FWHM) of Cu_2O profile leads to the identification of a homogeneous layer of Cu_2O with a thickness around 3.29 nm. Thanks to the previous study on sample without aging [45] and this result, we can conclude that there is no evolution in the Cu oxide phase or thickness when a Cu oxide endures long-term storage conditions at 175 °C.

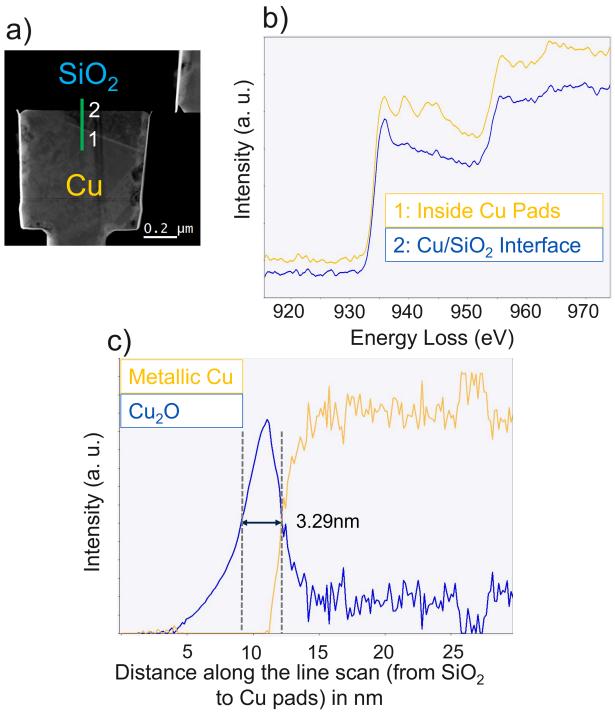

Figure 3.26: a) STEM picture illustrating the Cu/SiO_2 interface of the comb-serpentine structure with 720 nm wide HBM on the $S\&H$ test vehicle after HTS at 175 °C for 4000 h with the line scan (green) and the two sites extracted for study, b) $Cu - L_{2,3}$ ionization edge for the 2 sites and c) calculated Cu oxide thickness by using the two identified Cu_2O and metallic Cu references.

3.4.3 Conclusion

In this section, the major reliability concern of Cu diffusion at the Cu/SiO_2 hybrid bonding interface was profoundly investigated. In fact, during the bonding step and due to misalignment between top and bottom wafers, a part of Cu HBM is in direct contact of SiO_2. Cu can diffuse in SiO_2 under two forms, atomic and ionic, which could degrade the insulation properties of the dielectric. Based on our findings, we believe that Cu/SiO_2 hybrid bonding integration with a self-formed 3 nm Cu_2O is robust in response to Cu diffusion. Our analysis showed that the Cu_2O layer is at least as effective in suppressing Cu atomic diffusion as a 60 nm SiN dielectric barrier included in a BEoL stack. As for Cu ionic diffusion, a methodology with new test structures and electric characterizations methods allowed us to conclude that no Cu ionic diffusion occurs at the Cu/SiO_2 hybrid bonding interface with the reduction of the HBM width down to 405 nm. The 3 nm Cu_2O layer is efficient in suppressing Cu ionic diffusion and we believe that its formation is independent of the HBM size and the area ratio between Cu and SiO_2. Moreover, the Cu_2O layer present at the Cu/SiO_2 interface is thermally stable after aging the sample for long duration both in its oxide phase (no evolution to CuO) and thickness. All these results validate the hypothesis of the barrier characteristics of the Cu_2O layer. Hence, we believe that Cu diffusion should not be of a major concern with further pitch reduction if the Cu_2O barrier is still present at the Cu/SiO_2 hybrid bonding interface.

3.5 Time dependent dielectric breakdown

In this section, a focus is done on the time dependent dielectric breakdown (TDDB) failure mechanism study for our Cu/SiO_2 hybrid bonding integration. In section 3.4.1, we showed that low levels of Cu atomic concentration (around 10^{12} $at.cm^2$) is expected at the dielectric level due to the bonding and final annealing steps at 380 °C. Important question arises here on any impact on the performance under TDDB. In addition, even though no Cu ionic diffusion has been identified in section 3.4.2, the tests were done for a limited stress time. It is crucial to study any impact or presence of Cu diffusion on the failure behaviour under TDDB. The study in this section concentrates principally on verifying if the finding of the Cu_2O barrier layer is still valid under TDDB, which is the most critical test to project performance at use conditions. Secondly, since device with hybrid bonding integration is subject during his lifetime to thermal aging, we aim to study any performance loss under TDDB when the hybrid bonded structures are subject to these stresses.

3.5.1 Failure physics and degradation models

TDDB is a common failure mechanism at the BEoL as well as the front end of line (FEoL) levels. In the case of BEoL, the dielectric breakdown failure mechanism is usually associated with the inter-metallic dielectric (IMD) or inter-layer dielectric (ILD) oxides that separate metal lines. Due to the propagation of different signals, residual electrical charges can accumulate at the interface of the metallization layers. Under the application of an electrical field, these charges can migrate toward a metal line of lower potential by crossing the dielectric. With time aging, these electrical charges can lead to an effective delay ($\tau = RC$) to signal propagation. Leakage current can thus be formed between the lines, depending on the integration and increasing with lower distance between the metal lines. These leakage currents can lead eventually to the breakdown of the dielectric in an irreversible manner by the loss of its insulation properties.

Several degradation models have been proposed in the literature that could explain the aging of the dielectric under the application of an electric field. Here are the most reported ones:

1. The E-model, also known as the thermomechanical model, is proposed both for gate oxide and BEoL dielectrics [198] [199] [200]. Theoretical justifications for this model are based on the assumption that the application of an electric field will break weak bonds in the dielectric that will form leakage passages and will eventually result in breakdown.

2. The $\sqrt{E} - model$ is motivated by assuming dielectric degradation due to Cu-ion drift through the dielectric and on the observation that the two main conduction mechanisms (Poole-Frenkel and Schottky Emission) have a $\sqrt{E}$-dependency of the leakage current [201] [202]. The traps present in the material are ionized and will cause an increase in the local electric field, which lead to breakdown.

3. The 1/E model is based on the assumption that breakdown is caused by entrapment positive charges at the dielectric on the cathode side by Fowler-Nordheim tunnel-

ing [203]. This model does not embed a clear role of metallic diffusion assisting breakdown as compared to the $\sqrt{E}$ model.

The acceleration models associated with each of three models are as follow:

- E-model: TTF $\propto$ exp(-γE)
- $\sqrt{E}$-model: TTF $\propto$ exp(-2β $\sqrt{E}$)
- 1/E model: TTF $\propto$ exp(G/E)

Where γ, β and G are the acceleration parameters.

Other models have been proposed in the literature such as the impact damage (ID) model and the power law (PL) model [204] [205]. Our study is first limited to the three widely reported acceleration models.

3.5.2 Previous TDDB studies at hybrid bonding interface

Even though TDDB has been widely studied in the case of BEoL integration [206] [207] [208], very few studies have been done at the hybrid bonding interface. For instance, Hou calculated the field acceleration factor (γ) for the Cu/SiCN hybrid bonding configuration by measuring the breakdown voltage of the dielectric using several voltage ramp-up rates [189]. Three different ramp rates were applied (1.15, 0.26 and 0.06 V/s) at temperatures between 100 and 200 °C. The voltage ramp was found to affect the breakdown voltage V_{BD} since the voltage increments take time to induce TDDB stress effects leading to a lower V_{BD} for the lower ramp rates. The field acceleration parameter γ was found between 11-13 between 100 and 175 °C and decreases down to 9 at 200 °C, which could be linked to an impact of the Cu drift in the SiCN layer. The author then assumed a power law model to estimate V_{max} at use conditions and to conclude that the 10 years performance is guaranteed. We question if additional tests have been done to confirm this hypothesis.

As for the Cu/SiO_2 hybrid bonding integration, TDDB is even more critical since a potential misalignment between the top and bottom wafers will eventually lead that part of the Cu pad is directly facing SiO_2. Kagawa from Sony presented TDDB tests for the Cu/SiO_2 hybrid bonding integration (similar architecture design (Cu/SiO_2) to the one of interest for my PhD) but Black's parameter are used instead of the dependence on the electric fields [209] [152]. The author guarantees the 10 years performance at use conditions. Several crucial questions are kept vague. For example, what is the dependence between TTF and the electric field? Is there any role of Cu diffusion assisting breakdown? In addition, the TDDB performance highly depends on the characteristics of Cu and SiO_2 (deposition temperature, dopants used...), which are unique to each integration.

Since no actual TDDB details are given for the hybrid bonding integration, we will go through the main TDDB findings at the BEoL level. For instance, even with SiN or SiCN passivation layer, Cu diffusion was found to degrade the dielectric performance in TDDB [206] [210]. Cu diffusion into the dielectric during TDDB can take two forms [211]: (a) through the dielectric passivation layer known as interfacial diffusion as shown in figure 3.27 (a) and (b) through the metal barriers that is defined as bulk diffusion

(figure 3.27 (b)). The dielectric breakdown usually takes place at the interface between adjacent pads so that interfacial diffusion is the dominant path [201]. The interface is expected to have a higher trap density than the bulk dielectrics due to the bond mismatch between the different materials. Cu diffusion during TDDB will alter the TDDB electric field acceleration model that is used to determine the failure rate or the lifetime at use conditions. The $\sqrt{E}$-model is the most appropriate to describe the TDDB behaviour when Cu diffusion plays a major role in degrading the dielectric lifetime as shown by studies at BEoL level with dielectrics with k constant below 3.7 [201] [212].

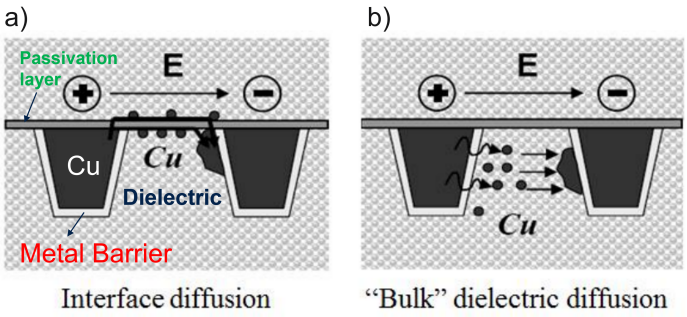

Figure 3.27: Schematic illustrations of the two possible failure modes for TDDB under the assumption that Cu diffusion through the dielectrics control the TDDB lifetime with a) interface diffusion and b) bulk diffusion.

In section 3.4.2, a conclusion was made that no Cu ionic diffusion is present at the Cu/SiO_2 interface when stressing the device. It is therefore expected to get a different failure mode under TDDB for our Cu/SiO_2 hybrid bonding integration than the $\sqrt{E}$-model if a negligible role of Cu drift assisting breakdown is found. A detailed study on the TDDB behaviour for the Cu/SiO_2 integration is conducted and presented hereafter.

3.5.3 TDDB results

3.5.3.1 Preliminary analysis: linear ramp voltage sweep (LRVS) measurements

We will start by studying the conduction mechanisms and the V_{bd} dependence on the distance between comb-serpentine (d) where d is adjusted with respect to the overlay found by Infra Red (IR) measurements (eq. 3.18). Several linear ramped voltage sweep (LRVS) measurements were done at 30 °C on the comb-serpentine structure (figure 3.20) where a potential difference is applied between the serpentine and either comb with a step of 1 V. The current compliance is 10^{-2} A. A total of 20 samples are tested. As shown figure 3.28, we can clearly distinguish two different behaviors of leakage current increase with voltage: the first one, associated with slow leakage current increase and the second, evidenced by high slope of leakage current increase just before the breakdown. For the structures with low V_{bd} (<40 V), the second behaviour is dominant. In fact, at constant voltage condition, much higher electric field will be reached on the structures with higher misalignment. These observations are in line with previous studies done with the 1.71 μm wide HBM that suggests that the conduction mechanisms do not change with HBM size

reduction from 1.71 to 0.72 μm [44].

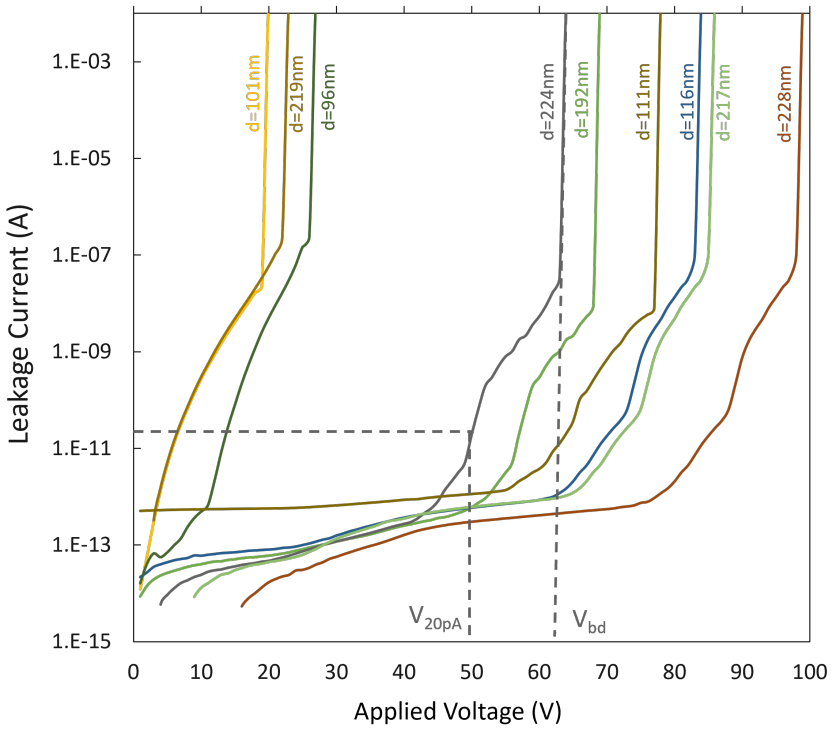

Figure 3.28: Examples of LRVS measurements done on comb-serpentine structures with 720 nm wide HBM on the *S&H* test vehicle at 30 °C with a step of 1 V. For each structure, the calculated d is indicated.

From the LRVS measurements and taking the hypothesis of planar capacitance ($E_{bd} = V_{bd}/d$), V_{bd} should change linearly with d. As shown in figure 3.29, where V_{bd} is plotted against the distance between the comb and serpentine, a poor R^2 of 0.01 is obtained. The estimation of E_{bd} from the linear fit gives a value of 0.4 MV/cm that is much lower than the breakdown strength reported in the literature for the SiO_2 case (up to 10 MV/cm) [213] [214].

The underestimation of the breakdown strength for our case could be related to the errors induced when calculating the d value. The errors can be summarized as follow:

1. The imprecisions induced from overlay measurements estimated for our case: ±30 nm.

2. The errors related to the HBM shape at the hybrid bonding interface. In fact, the theoretical HBM width at the interface is 720 nm whereas our analysis based on TEM cross sections showed that we can have up to ±55 nm variation of the HBM width. This will directly impact the estimated distance d.

To test these last hypotheses, TEM cross sections were performed on several structures tested under LRVS with different breakdown voltages to measure the distance d between the comb and serpentine. The results for two structures are shown in figure 3.30. Important observation is related to Ta/TaN barrier form at the interface. This form is induced during the CMP step and should also be considered when estimating the critical distance between adjacent pads. For structure 1 with V_{bd} of 31 V (figure 3.30 (a)),

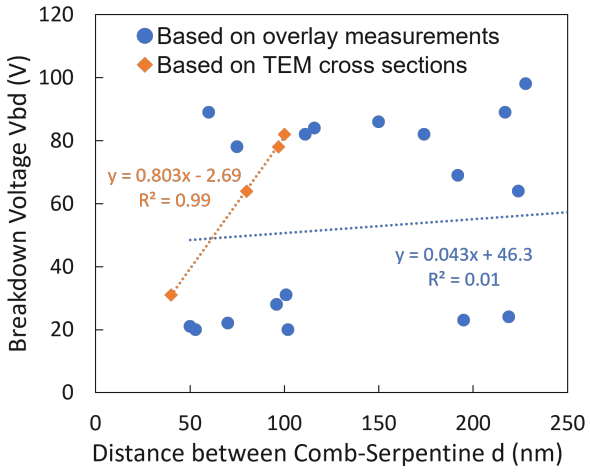

Figure 3.29: The breakdown voltage V_{bd} vs. the distance between comb and serpentine (d) based on overlay measurements and on TEM cross sections.

the measured distance d on TEM is 40 nm vs. 101 nm based on overlay measurements. Similarly, for structure 2 with V_{bd} of 82 V (figure 3.30 (b)), the distance between comb and serpentine based on TEM is 100 nm vs. 174 nm based on overlay measurements. The prediction of the breakdown strength based on several TEM measurement leads to a value of 8±0.2 MV/cm as shown in figure 3.29, which is more in agreement with the reported breakdown field of SiO_2 [203].

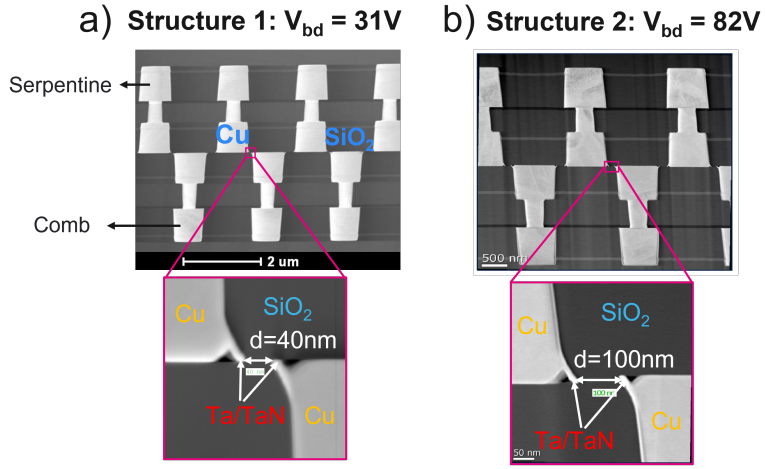

Figure 3.30: TEM cross sections for (a) structure 1 with V_{bd} of 31 V showing a distance between comb and serpentine of 40 nm and (b) structure 2 with V_{bd} of 82 V showing a distance between comb and serpentine of 100 nm on the $S\&H$ test vehicle.

We can conclude that a precise TDDB analysis based on W2W overlay measurements is not possible when the distance between adjacent pads is lower than 200 nm. In fact, for a given electric field for test, more than 100 % uncertainty is expected due to the variables impacting d (overlay measurements imprecision and pad shape variations at hybrid bonding interface). Therefore, a method is needed to precisely predict the distance d without cutting the structure or even harming it electrically.

3.5.3.2 TDDB testing method and conditions

To get a precise TDDB analysis, the LRVS curves in figure 3.28 are studied in order to predict V_{bd}. Based on the observation made previously on the high slope of leakage current increase for all the structures whatever the distance d, we define the 20 pA current point to report its respective voltage (check example in figure 3.28). The 20 pA current is an arbitrary criterion and another point of reference could be defined as long as it is present in the high leakage increase part of the curve. It is mandatory to stay in the reversible zone i.e., without degradation if the electric potential is lowered that justifies the choice of the 20 pA point. The difference between V_{bd} and V_{20pA} is calculated for all the structures. The probability density function (PDF) distribution shown in figure 3.31 indicates that the results are well centered at 14 V and the variations of ΔV are distributed between 11 and 17 V. This implies that the behavior in this region of electric fields is very similar.

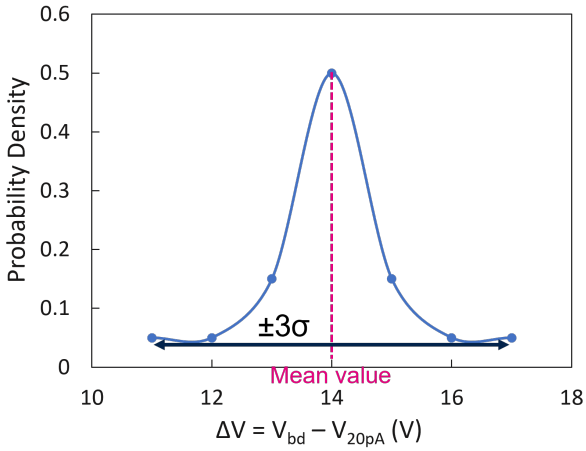

Figure 3.31: Probability density function (PDF) of ΔV (V_{bd}-V_{20pA}) showing results varying between 11 and 16 V and well centered at 14 V.

This allows to define the methodology for TDDB testing at the hybrid bonding interface as following:

1. LRVS measurements are performed on the structures to be tested in TDDB with a stop condition at 20 pA. The V_{20pA} is then found without harming the structure.

2. 14 V is added to V_{20pA} in order to finely estimate V_{bd}. The distance between comb and serpentine is classically calculated as d = V_{bd}/E_{bd} where E_{bd} is equal to 8 MV/cm as found experimentally.

3. Structures with an estimated $V_{bd} > 40$ V are only tested under TDDB. When limited to structures with an estimated $V_{bd} > 40$ V, the error of V_{bd} estimation by this method is restricted to $\pm$7.5 % for the worst case scenario (estimation error = $\pm$3V/40V).

Application of the described method is done using the comb-serpentine structure with an HBM width of 720 nm presented in figure 3.20 at the different test conditions shown in table 3.8. TDDB measurements are done at the wafer level of the S&H test vehicle. Three temperature test conditions are defined: 155, 170 and 195 °C. 12 samples are tested per

each stress and temperature conditions. The failure criterion is set at an absolute leakage current level of 1 mA, which is an arbitrary criterion that critically affects the chip performance.

Table 3.8: TDDB test conditions performed on the comb-serpentine structure with HBM width of 720 nm on the *S&H* test vehicle.

Electric Field (MV/cm)	Temperature (°C)	Volume
6	170	12 samples each
4	155 - 170 - 195	
2.67	155 - 170 - 195	
2.1	155 - 170 - 195	
1.6	195	

In the following section, the results of TDDB study using the described method are presented for the Cu/SiO_2 hybrid bonding configuration with 1.44 μm pitch.

3.5.3.3 Time-to-failure dependence on the electric field

An example of TDDB results for the tested temperature of 155 °C is shown in figure 3.32 (a). Initially, a decrease in the leakage current is observed that can be linked to several mechanisms in relation with the dielectric's nature such as trapping. Then, the SiO_2 degradation leads to an increase in the leakage current until it increases significantly and reaches the failure criterion (1 mA). From the TDDB results, the Weibull distribution are plotted in figure 3.32 (b). There is no significant change in the shape parameter/Weibull slope (β) between the different testing conditions indicating that the active failure mechanism stays identical. This observation is valid for the tested temperatures of 170 °C and 195 °C as documented in appendix B, section B. 1.

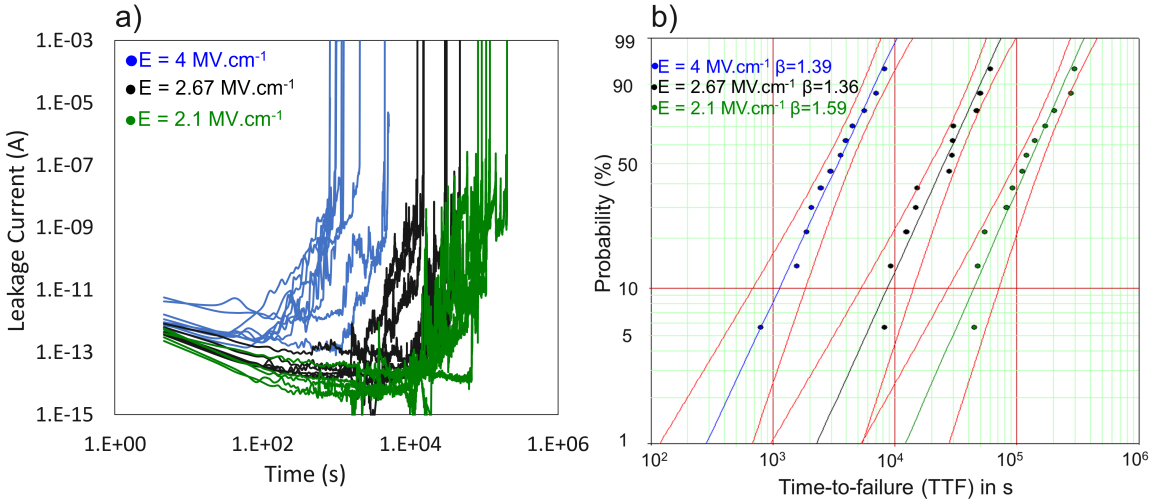

Figure 3.32: Example of a) TDDB results and b) Weibull distribution at the tested temperature of 155 °C on the comb-serpentine structures with 720 nm wide HBM on the *S&H* test vehicle.

From the Weibull distributions, the 63.2 % TTF is extracted to study the dependence on the electric fields. The three field-acceleration models previously presented (E, $\sqrt{E}$

and 1/E) are first used to fit the experimental data. The results of fitting the different models are shown in figure 3.33 (a), where the results at 4 and 2.67 MV/cm are considered to build the different acceleration models. It is clear that the 1/E model is the only model capable of fitting the experimental data at all tested temperature for electric fields below 2.5 MV/cm. Important observation is at the temperature of 170 °C, the TTF at 6 MV/cm mostly fits the $\sqrt{E}$-model. The electric field of 6 MV/cm being close to the breakdown field (8 MV/cm), we question if this is caused by a change in the failure mode. This observation could not be validated at the temperature conditions of 195 and 155 °C. Since at no time will the product be subjected to such high electric field of 6 MV/cm even with the lowest tested critical distance of 50 nm between adjacent pads, we will focus on the 1/E dependence in the following sections. The 1/E model is the most adequate to project performances at use conditions. The fitting of the 1/E model at lower field of 1.6 MV/cm is validated for the temperature of 195 °C. This leads to the conclusion that, at electric fields below 2.67 MV/cm, the failure mode in TDDB at the hybrid bonding level is different from the standard Cu BEoL interconnects where a clear $\sqrt{E}$ dependence was reported. This can be attributed to the role of Cu assumed negligible in the dielectric breakdown mechanism for the Cu/SiO_2 hybrid bonding integration leading to higher TTF at lower electric fields (check explanations in section 3.5.1).

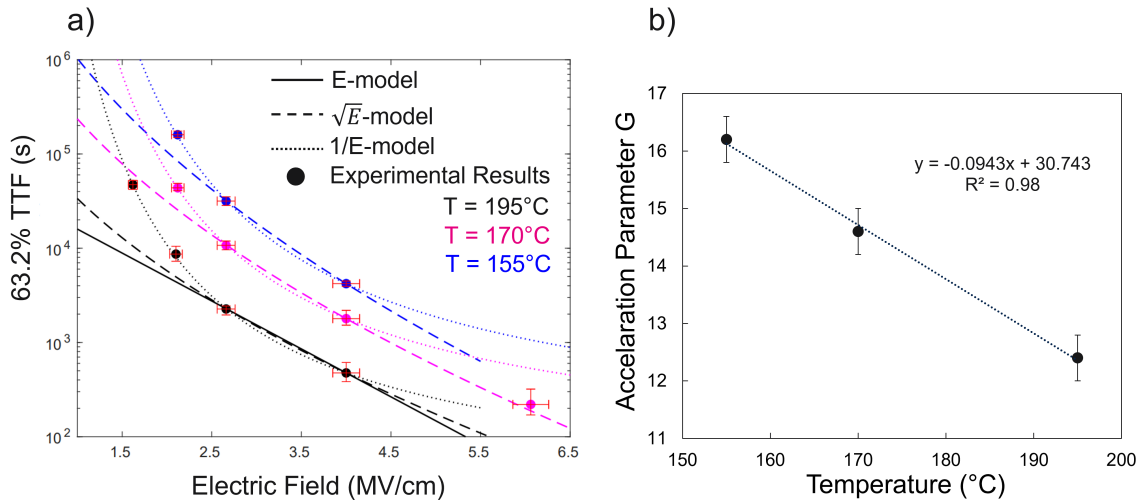

Figure 3.33: a) Results of fitting the different models with TTF obtained at 63.2 % of Weibull distribution at all tested temperatures as obtained from TDDB tests on comb-serpentine structures with 720 nm wide HBM on the *S&H* test vehicle. Vertical bars are 90 % confidence bounds and horizontal bars are the ±7 % of uncertainty on the electric field. b) Acceleration parameter G dependence on temperature.

For each temperature, the result of extracting the acceleration parameter G is represented in figure 3.33 (b) showing a temperature dependency. The field-acceleration parameter increased by more than 35 % with temperature decrease from 195 to 155 °C. The temperature dependency of the acceleration parameter was also reported in the literature for the case of E-dependency and for ultra-thin oxide study at the FEoL level [215].

Based on these results, we think that for the Cu/SiO_2 hybrid bonding configuration, the role of Cu assisting is negligible. In the following section, to validate this hypothesis, the activation energy dependence on electric field is studied.

3.5.3.4 Activation energy dependence on the electric field

The activation energy E_a is calculated using the Arrhenius equation that states the following:

$$TTF = Aexp^{\frac{E_a}{KT}} \tag{3.19}$$

where TTF is taken at 63.2 %, A is pre-exponential factor assumed to be temperature independent, K is the Boltzmann constant and T is the temperature. The activation energy is found, for each tested electric field, by fitting between the different temperatures as detailed in appendix B, section B. 2. The activation energies are summarized in table 3.9 and are found to increase from 0.95 to 1.26 eV for the electric field of 4 and 2.1 MV/cm respectively.

Table 3.9: Results of activation energies found at the different studied electric fields.

Electric Field (MV/cm)	Activation Energy (eV)
4	0.95 ± 0.07
2.67	1.14 ± 0.07
2.1	1.26 ± 0.07

Exclusively for TDDB, a dependency between the activation energy (E_a) and electric field was previously found and studied for gate and BEoL oxides. Below, we briefly analyze the physics of this dependence and possible impact of any Cu diffusion on the activation energy based on the study done by McPherson in the case of thermomechanical E model. The relation between the activation energy and the electric field is given by equation 3.20 [198]:

$$E_a^* = E_a - pE_{loc} - \frac{1}{2}\alpha E_{loc}^2 \tag{3.20}$$

where E_a^* (eV) is the effective activation energy for bond breakage in the presence of a field, E_a (eV) is the intrinsic activation energy for bond breakage in the absence of a field, p (C.m) is the permanent dipole moment of SiO_2, E_{loc} (V/m) is the local electric field at the molecular level and α ($e.m^2/V$) is the molecular polarizability of SiO_2. The applied electric field E is embedded inside E_{loc}. In fact, each molecule inside the SiO_2 dielectric will experience the applied electric field E plus a dipolar field due to the polarization. This implies a local electric field E_{loc} (which distorts the Si–O bonds) which can be nearly twice the magnitude of the applied electric field [198].

For the case of no metallic diffusion assisting breakdown, the activation energy is dependent on the strength or weakness of the dielectric bond and therefore, the quadratic term's (αE_{loc}^2) impact is negligible. This led to a direct relationship between the activation energy and E. For model when metallic ionic diffusion assists breakdown, for instance the $\sqrt{E}$ model, the quadratic term should be taken into account and the activation energy at low fields will tend to lower values than the linear relation. The molecular polarizability, which is a measure of the molecular distortion which occurs, is given by:

$$\alpha = \frac{3\epsilon_0 \times (\epsilon_r - 1)}{N_V \times (\epsilon_r + 1)} \tag{3.21}$$

where ϵ_0 ($= 5.52 \times 10^{-4}$ e/Vnm) is the permittivity of free space, ϵ_r (=3.9) is the relative dielectric constant for SiO_2 and N_V ($= 2.3 \times 10^{22}$ $/cm^3$) is the number of molecules per unit volume. This gives a molecular polarizability for the SiO_2 molecule of 3.54×10^{-13} $e.m^2/V$. Two parameters can play a role in modifying the molecular polarizability when metallic diffusion assists breakdown: the relative dielectric constant which will increase with metal accumulation inside the dielectric and the number of molecules per unit volume. The increase in the dielectric constant will increase α until reaching a limit value of 7.19×10^{-13} $e.m^2/V$. Even though α have doubled, this will have a negligible impact on the quadratic term with respect to the pE_{loc} term (even at high fields, for example E = 10 MV/cm, and with $\alpha = 7.19 \times 10^{-13}$ $e.m^2/V$, $\frac{1}{2}\alpha E_{loc}^2/pE_{loc} < 0.01$) [198].

We can therefore suspect that the main contributor to the increase in α (and thus the quadratic term) is N_V. The presence of metallic ion drift will tend to reduce the number of molecules per unit volume leading to lower activation energies at low fields. This behavior was previously reported in the case of Cu diffusion assisting breakdown [216].

For our case, a dependence between the activation energy with either E and 1/E can be established as shown in figure 3.34 (a) and (b) respectively. The activation energy dependence on E is expected for the case of the thermomechanical E model and is not in line with the TTF dependence on 1/E previously discussed. Although no clear physical explanation exists until this day for the activation energy dependence on 1/E, we think it is the correct correlation taking into consideration the found TTF dependence on 1/E.

In either case, there is no sign of any reduced E_a at electric field below 3 MV/cm, which suggests that the role of metallic diffusion assisting breakdown is negligible.

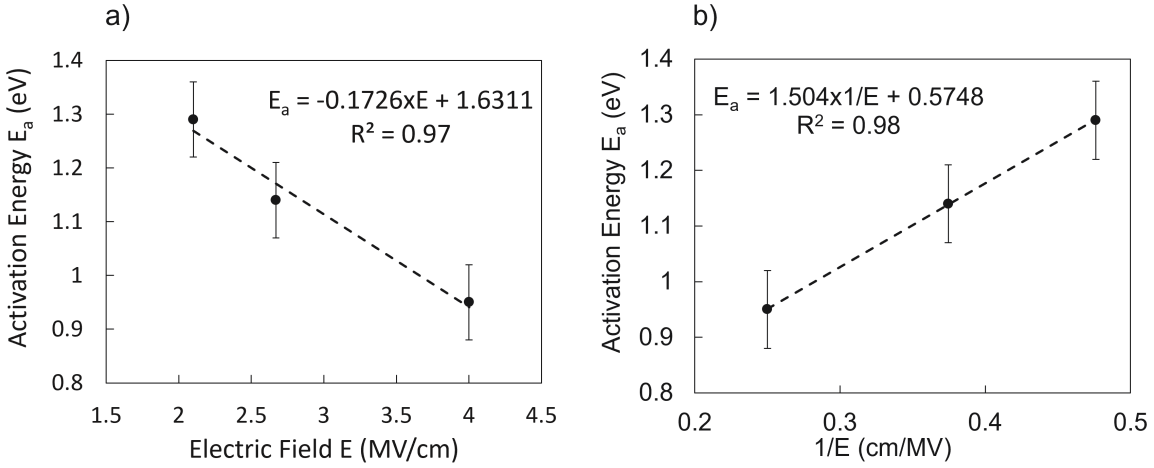

Figure 3.34: Activation energy dependence on a) the electric field (E) and b) the inverse of the electric field (1/E). Vertical bars represent the imprecision in estimation of the activation energy.

A comparison is made between the found activation energy at the Cu/SiO_2 hybrid bonding interface with different BEoL dielectrics from the literature cases as shown in table 3.10. Some values were interpolated with respect to the relations between the activation energy and electric fields found by the authors [217] [201]. The activation energies are higher for the hybrid bonding case as compared to BEoL even though a passivation layer (SiN or SiCN) is used to limit Cu diffusion. For the reported BEoL studies, a $\sqrt{E}$ dependence is reported which is a sign of Cu diffusion assisting breakdown.

Table 3.10: Comparison between the activation energies obtained at the different electric fields for our hybrid bonding with SiO_2 (720 nm wide HBM) vs. BEoL cases with either SiN or SiCN passivation layers.*Interpolated values.

Electric Field (MV/cm)	Activation Energy E_a (eV)		
	Our SiO_2 (k=3.9) Hybrid Bonding - No passivation layer	FSG (k=3.7) BEoL - SiN passivation [201]	SiOC (k=3) BEoL - SiCN passivation [217]
4	0.95	0.7	0.6
2.67	1.14	1.01*	0.9*
2.1	1.29	1.1*	0.95*

Based on the activation energy results, we believe that any Cu diffusion does not play a significant role assisting TDDB for the Cu/SiO_2 hybrid bonding integration. Higher activation energies as compared to BEoL interconnects with SiN and SiCN dielectrics barriers as passivation are observed for similar electric fields. Even though the original equation of activation energy dependence on E (equation 3.20) does not take into account a possible role of a barrier-like layer, the results of activation energies do reflect the role of a possible barrier. Hence, we believe that the higher activation energies obtained for the Cu/SiO_2 hybrid bonding case could be related to the Cu_2O layer present at the Cu/SiO_2 interface and acting as a barrier to Cu diffusion even under TDDB.

3.5.3.5 Discussion on the role of Cu_2O

As previously stated, a 3 nm layer of Cu_2O was evidenced by EELS in the region when Cu is in direct contact of SiO_2. The efficiency of this layer to act as a barrier to Cu diffusion under the application of electric fields was studied by TVS/BTS characterizations. We therefore believe that this layer remains a barrier to Cu diffusion under TDDB leading to the 1/E dependence and that no reduced activation energy was found at lower fields. McPherson showed that the 1/E model is valid when the initial bond breakage energy is strong, leading that the current induced hole-capture rate is dominant with respect to field-enhanced bond breakage rate [203]. Moreover, Lloyd found that the 1/E dependence is based on the assumption that the failure time is proportional to the rate at which damage is created in the dielectric by high energy electrons [218]. In any case, this model does not embed a clear or major role of metallic ion drift in the failure mechanism, which indicates that the role of Cu in TDDB is negligible. This is in line with our observations and strengthens our hypothesis that cuprous oxide (Cu_2O) can act as a barrier against Cu diffusion in SiO_2 for the Cu/SiO_2 hybrid bonding integration.

One can also suspect the presence of the Cu_2O layer at the Cu/passivation interface that could make our conclusion on the role of Cu_2O at the hybrid bonding interface incorrect. Since the Cu/SiCN hybrid bonding process is not available in the scope of my PhD, we will limit the study to the case of SiN deposited on Cu pads, which is typical to a standard BEoL interface. This study could also help us to understand the different failure modes observed in TDDB between our hybrid bonding case with respect to the BEoL studies with SiN. To study the presence of the Cu_2O layer at the Cu/SiN standard BEoL interface, the EELS technique is used. A sample was processed for study as shown in figure 3.35 (a) where a 60 nm SiN layer was deposited on top surface after CMP. The bonding annealing step of 380 °C-2 h is applied. In figure 3.35 (b), a zoomed TEM picture at the Cu/SiN interface is shown along with the line scan (green line) performed for the EELS analysis. Two sites are extracted: (1) Cu/SiN interface and (2) inside Cu pads. In figure 3.35 (c), the $Cu - L_{2,3}$ ionization edges for the 2 sites are given. Both results are similar that correspond to reported Cu crystalline spectra with no white line [219]. There is no sign of an oxide copper at the interface. This suggest that cuprous oxide highlighted at Cu/SiO_2 hybrid bonding interface does not exist at the standard BEoL interface. Cu_2O seems to be a hybrid bonding characteristic. This could explain the different acceleration model observed for the TDDB failure mechanism ($1/E$ vs. $\sqrt{E}$) between our hybrid bonding case and BEoL one. We can confidently conclude that, for the Cu/SiO_2 hybrid bonding interface even without a passivation layer, the Cu_2O layer is efficient to provide reliable configuration under TDDB.

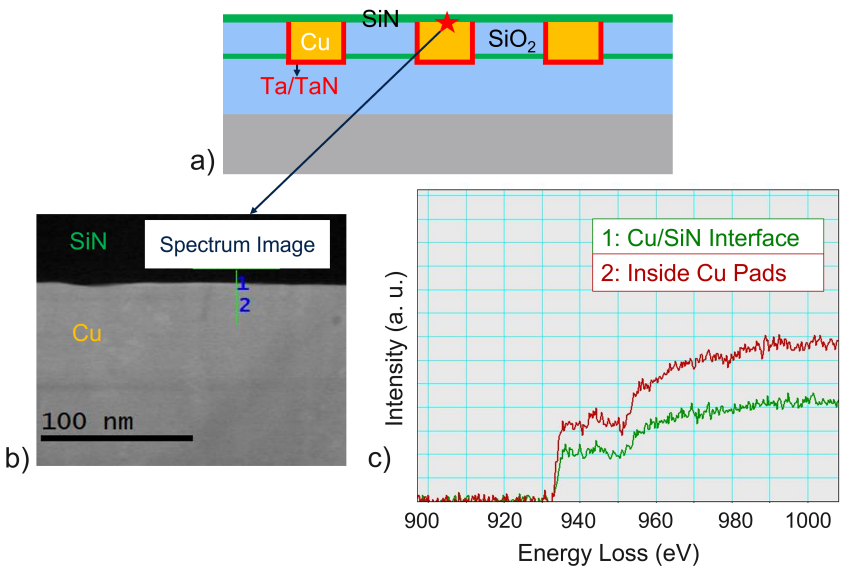

Figure 3.35: a) Schematic representation for the structure used for EELS analysis. b) TEM picture illustrating the Cu/SiN interface with the line scan (green) and the two sites extracted for study. c) $Cu - L_{2,3}$ ionization edge for the 2 sites.

Furthermore, we think it is of great interest to study the presence of the Cu_2O layer in the case of the Cu/SiCN hybrid bonding configuration. If its presence is validated, this will lead to hybrid bonding configuration with a double barrier, including both Cu_2O and SiCN.

3.5.3.6 Predictive TDDB model

Important consideration for TDDB is the estimation of the electric fields at use conditions. One possible method to extrapolate the TDDB performances to use conditions is to use the relations found previously between TTF and temperature at each electric field (figure B.2) to estimate the TTF either at 63.2 or 0.1 % at the temperature of 125 °C for each electric field. After that, one can take the hypothesis that the time-to-failure is still dependent on 1/E with decreasing temperature. A 1/E model can then be fitted using the extrapolated values to predict the performance at use conditions.

More generally, we can propose a generalized equation for TTF prediction based on the study reported by Kimura who presented the time to breakdown dependence on 1/E by equation 3.22 [220]:

$$TTF(T) = \tau_0(T) exp\left(\frac{G(T)}{E}\right) \tag{3.22}$$

τ_0 is the pre-exponential factor that depends on the temperature. The acceleration parameter G was reported in figure 3.33 and can be written as following:

$$G(T) = -0.0943 \times T + 30.743 \tag{3.23}$$

In the same way, and using the relations found in figure 3.33, it is possible to establish a correlation between τ_0 and the temperature. However, this correlation depends on the TTF percentage taken for calculations. Considering the TTF at 0.1 %, the following equation describes the dependence between τ_0 and the temperature (T in °C):

$$\tau_0(T) = -0.21 \times T + 46.18 \tag{3.24}$$

Equation 3.22 can then be written as following:

$$0.1\%\ TTF = (-0.21 \times T + 46.18) exp\left(\frac{-0.0943 \times T + 30.743}{E}\right) \tag{3.25}$$

Using equation 3.25, it is possible to project the TDDB performance for a given temperature and applied electrical field depending on the type of application.

3.5.3.7 TDDB failure localization analysis

To physically check the failure mode for our 1/E dependence, failure analyses were performed to localize the failures triggered by different stress conditions. Optical beam induced resistance change (OBIRCH) technique is used for failure localization. A 1340 nm laser is used, and a potential difference of 700 mV is applied between the serpentine and comb. Several failed structure under different TDDB test conditions were analyzed. An example is shown in figure 3.36. Defects (red and green spots) are clearly located within the test structure footprint. The result indicates that the electrical failure is the sum of multiple defective zones. As the structure is buried under several metal layers, the failure analysis is challenging despite the use of a computer-aided design (CAD) alignment solution. In fact, TEM images performed inside the OBIRCH spots failed to highlight any short or failure at the interface. One possible solution could be the consideration of the delayering before the OBIRCH analysis to be able to perform a better CAD alignment,

directly on the test structure and not on the test pads. This action was launched but it is very challenging as stopping the delayering process at the correct level is very tricky. At the moment of writing the PhD thesis, no conclusive results were available.

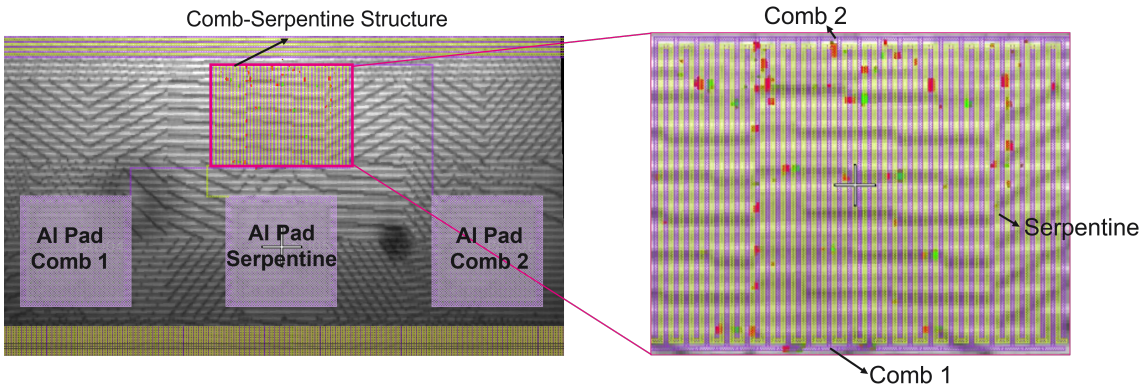

Figure 3.36: Example of the result of an OBIRCH analysis of a comb-serpentine structure with 720 nm wide HBM on the *S&H* test vehicle after TDDB breakdown at 155 °C and 2.1 MV/cm (top view). The test structure layout design is superimposed (violet and yellow colors). Defects, red and green spots, are identified within the test structure footprint.

3.5.4 Impact of thermal aging on TDDB performance

Devices are subject during their lifetimes to thermal cycles and aging. Thermal aging could degrade the insulator properties of the dielectric leading to lower breakdown strength and lower performance under TDDB [221]. Even though BTS/TVS did not show any Cu ionic diffusion after long thermal aging at 175 °C for 4000 h, it is of critical interest to study any impact of thermal aging on the TDDB performance. Therefore, TDDB tests are performed at 170 °C on comb-serpentine (figure 3.20) structures after a total thermal aging of 4000 h at 175 °C. At the three electric fields previously studied (2.1, 2.67 and 4 MV/cm), the Weibull distributions are shown in figure 3.37 (a) along with the shape parameter/Weibull slope (β). No significant change in β is observed between the different testing conditions indicating that the active failure mechanism stays identical. The results of fitting the TTF dependence on the electric field is shown in figure 3.37 (b).

The 1/E model fits best the experimental data, in particular, at electric fields below 2.5 MV/cm. The acceleration parameter G is found to be equal to 14.2 as compared to 14.6 on samples without any aging. Similar TTFs are obtained before and after thermal aging at 175 °C for 4000 h suggesting that the dielectric keeps its insulator properties and that no major role of Cu assisting breakdown is present. This conclusion is in line with the BTS/TVS characterizations results and with the Cu_2O stability after thermal aging.

3.5.5 Discussion on TDDB behaviour and impact of pitch reduction

Based on the TDDB results presented in this section, we can propose the following discussion with respect to its behaviour and the expected performance with pitch reduction.

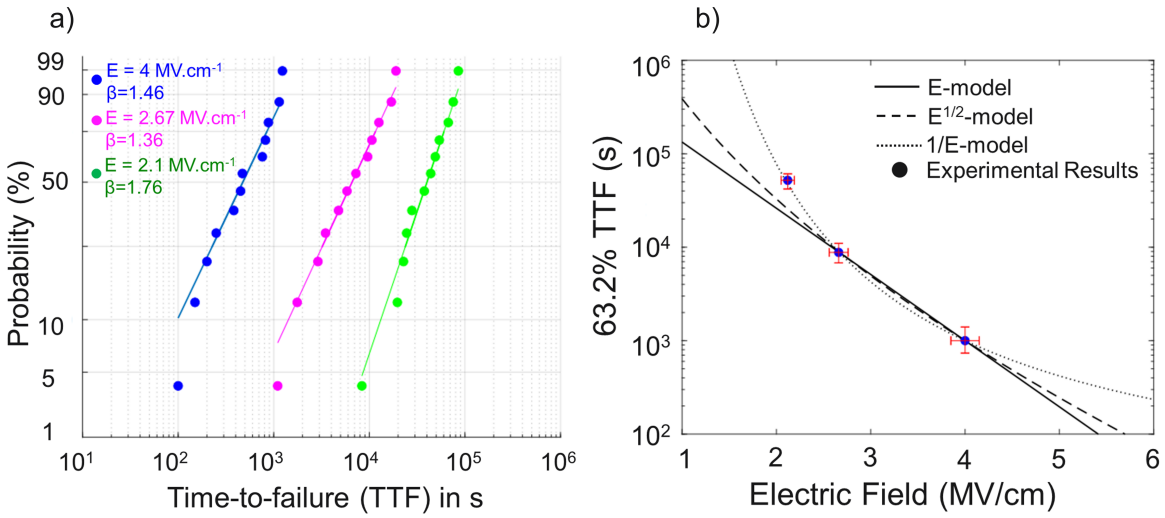

Figure 3.37: a) Weibull distributions (solid lines) of times-to-failure for the 3 electric fields at temperature of 170 °C done on the comb-serpentine structures with 720 nm wide HBM on the *S&H* test vehicle and the sample after a total thermal aging of 4000 h at 175 °C and b) Results of fitting the different models with TTFs obtained at 63.2 % of the Weibull distributions.

First, we should define the critical distance location at the hybrid bonding level where dielectric breakdown is expected to take place. This critical distance is illustrated in figure 3.38. It is always expected to be at the hybrid bonding interface even when there is no misalignment (figure 3.38 (a)). This is driven by: (1) the trapezoidal shape of the HBM with higher width at the interface and (2) the Ta/TaN barrier shape at the interface (check figure 3.38) that is induced from the CMP step. Due to this last effect, usually known as galvanic corrosion, a void is supposed to be present at the Cu/TaTaN intersection on the interface. This behaviour is not a unique characteristic of our hybrid bonding integration since it is seen also on other hybrid bonding integration such as IMEC's configuration [25] [76].

In the case of no misalignment (figure 3.38 (a)), there is no Cu in direct contact of SiO_2. For this particular case, we expect that the TDDB conduction mechanism is dominant by ¨bulk diffusion¨. If any Cu diffusion occurs, it will be through the Ta/TaN barrier. Due to the well controlled quality barrier between the Cu and SiO_2, ¨bulk diffusion¨ requires extremely high stressing time. In a device with several Cu/passivation dielectric interfaces and low k dielectrics at the BEoL level, we expect that TDDB occurs first at the BEoL level rather than the hybrid bonding interface.

Once a misalignment between the top and bottom wafers occurs, Cu will face SiO_2. In this particular region, a self-formed Cu_2O layer is present as shown schematically in figure 3.38 (b). The critical distance is also the one at the hybrid bonding interface between adjacent pads. At electric fields above 6 MV/cm, the conduction mechanism might be driven by the $\sqrt{E}$-model based on the reported finding in our study. However, at no time will the product be subject to such high electric fields even when the critical distance is 50 nm. For electric fields below 4 MV/cm and based on the 1/E dependence found in our TDDB studies, we believe that the Cu_2O acts as a good barrier to Cu diffusion, therefore decelerating or potentially suppressing any impact of Cu diffusion during TDDB. One

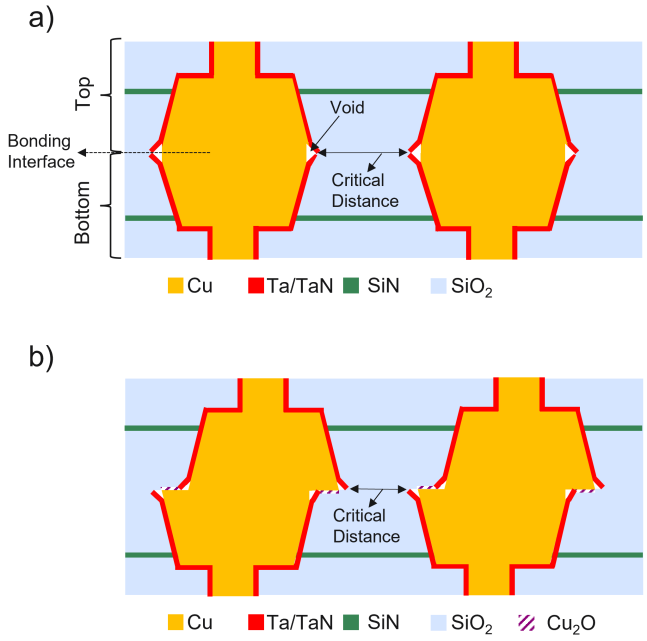

Figure 3.38: Schematic representation of the hybrid bonding configuration illustrating the critical distance where TDDB is expected to take place for a) case with no W2W overlay and b) with misalignment.

can expect that, with increasing stressing time, the Cu_2O layer might lose some of its barrier characteristics leading to Cu ions generation in SiO_2 until breakdown. If this phenomenon does actually take place, it will occur after much higher stressing times than the BEoL failure time, which is based on the higher activation energy found and the 1/E field acceleration dependence as compared to the $\sqrt{E}$ one.

Moving to the TDDB behaviour with pitch reduction, we have assessed in the present study structures under TDDB with a distance between adjacent pads down to 50 nm. We believe that the same TDDB behaviour is expected when the distance is higher than 50 nm irrespective of the HBM width. This is because we think that the Cu_2O formation is independent of the pad width. If we take into consideration the latest W2W development allowing an accuracy down to ±50 nm [132], we predict that the hybrid bonding configuration is reliable from a TDDB point of view down to 200 nm pitch (100 nm wide HBM pads). When the distance between adjacent pads is below 50 nm, a TDDB assessment is needed to evaluate any change in the conduction mode.

3.5.6 Conclusion

In this section, the dielectric breakdown failure mechanism at the Cu/SiO_2 hybrid bonding level was investigated. A new TTDB testing method was developed, based on the analysis of preliminary LRVS measurements, allowing to conduct precise TDDB measurements. This new method can also be applied to any other BEoL level that include overlay between via and metal lines, induced from lithography step for instance, to achieve higher precision under TDDB analysis. Based on this method, a 1/E dependence under TDDB

for the Cu/SiO_2 hybrid bonding is found, which is a different acceleration model as compared to the $\sqrt{E}$-model for the standard BEoL interconnects. Higher activation energies are found as compared to BEoL dielectrics with either SiN or SiCN passivation layer at the Cu/dielectric interface. We believe that the origin of this difference is the presence of the Cu_2O barrier, which is a characteristic of the Cu/SiO_2 hybrid bonding process. In our studies, we showed that no ionic diffusion takes place with HBM size down to 0.405 μm. In addition, we covered TDDB studies with a spacing between pads down to 50 nm. We can confidently conclude that the Cu/SiO_2 hybrid bonding level is reliable under TDDB down to a pitch of 200 nm, as we also believe that the Cu_2O layer formation is independent of the HBM width.

3.6 Chapter 3 conclusion

In this chapter, we have investigated the main reliability risks for the Cu/SiO_2 hybrid bonding level with the reduction of the pitch. These include the mechanical stability of the bonding interface, the stress induced voiding (SiV) mechanism, the electromigration (EM) failure mechanism, the risk of Cu diffusion in SiO_2 and the time dependent dielectric breakdown (TDDB) failure mechanism.

From a mechanical stability and SiV point of views, no failures were identified with hybrid bonding pitch reduction down to 0.81 μm. We can confirm that these reliability risks continue as the least critical failures even in the sub micron pitch region indicating that the Cu/SiO_2 hybrid bonding interface is robust. For future studies on the mechanical stability of the hybrid bonding level, we suggest to perform thermal cycling on the samples having contact resistivity at interface above 10^{-11} $\Omega.cm^2$. We believe this should allow better understanding on the existence of any correlation between the mechanical and electrical qualities of the hybrid bonding level. For the SiV failure mechanism, it would be interesting to perform high temperature storage tests at different temperatures in the range of 150-250 °C. This should allow better understanding on the critical temperature for the SiV accelerating tests and provide a more profound understanding of this failure mechanism for future studies.

For the electromigration failure mechanism, we evidenced a change in the killer void location from the top or bottom metal lines (pitch > 7 μm) to the HBV level for pitch below 3.5 μm. Even though projections under use conditions are not affected by this change of failure mode for the 1.44 μm pitch, the hybrid bonding level is no longer immune to electromigration. A potential degradation scenario could be concluded for these lower pitches. Void occurs first at the HBM level, more precisely at the Cu/SiO_2 interface, due to the low activation energy at the $Cu/SiO2_2$ region. In a second phase, the void at the HBV level nucleates caused by flux divergence due to the presence of the TaN/Ta barrier. Failure by electromigration occurs at the HBV, which is the region with the highest current density. We believe that electromigration failure mechanism could potentially become the principal concern with further pitch reduction especially if the degradation scenario is kept identical. We therefore expect lower TTF with the reduction of the hybrid bonding pitch due to lower HBM volume acting as a reservoir effect. In addition, as shown in the previous chapter for the 0.81 μm pitch, HBV and HBM have continuous shape. We think this could have a possible impact on the killer void location that could be shifted to the HBM level or a competition between two distinct failure modes under electromigration. Hence, EM studies are of critical interest in the sub micron pitch region to inspect that it satisfies to the product specification at use conditions.

Cu diffusion at the interface, which is the major reliability concern for the Cu/SiO_2 configuration, was also investigated in depth. During the bonding step, a possible misalignment could take place between the top and bottom wafers leading that part of the Cu HBM is in direct contact of SiO_2. Cu atomic or ionic diffusion could seriously degrade the SiO_2 dielectric insulation properties. In the region where Cu is facing SiO_2, a 3 nm of Cu_2O layer is formed. We believe that the Cu_2O layer formation is related to the Cu oxidation after CMP and before bonding. After bonding annealing, in the Cu-Cu region,

the Cu_2O layer diffuses along the Cu-Cu bonding interface allowing Cu-Cu contact [185]. In the region where Cu HBM is facing SiO_2, we think that the Cu_2O remains stable after bonding annealing explaining its presence evidenced by EELS analysis. The Cu_2O is thermally stable even after very long thermal aging (4000 h) at 175 °C. Our studies on Cu thermal and ionic diffusion concluded the following: (a) the 3 nm Cu_2O layer is at least as efficient in minimizing Cu atomic diffusion as the 60 nm SiN dielectric barrier, (b) no Cu ionic diffusion takes place at the Cu/SiO_2 hybrid bonding interface even after thermal aging suggesting the Cu_2O has better characteristics in suppressing Cu ion drift into SiO_2 than the SiN or SiCN with much higher thicknesses. The Cu/SiO_2 hybrid bonding configuration, with the self-formed Cu_2O barrier, is reliable in response to Cu diffusion. We believe this will still be valid with further pitch reduction since we think that Cu_2O formation is independent of the Cu pad size at the hybrid bonding interface.

Time dependent dielectric breakdown analysis on comb-serpentine with HBM width of 720 nm evidenced TTF dependence of 1/E for electric fields below 2.6 MV/cm. Our results evidenced a different acceleration mode in TDDB compared to the one constantly reported at the BEoL level ($\sqrt{E} - model$) with SiN/SiCN passivation layers. These results are further assisted by the higher activation energies found for the Cu/SiO_2 hybrid bonding interface as compared to BEoL cases. This modified behaviour is attributed to the negligible role of Cu assisting breakdown at the Cu/SiO_2 hybrid bonding interface. The 3 nm Cu_2O, which presence is unique to the Cu/SiO_2 hybrid bonding interface, is also efficient in decelerating or even eliminating Cu ionic diffusion under TDDB. Based on our detailed studies, a predictive TDDB model was proposed that could be used to extrapolate the TDDB performance for future applications with sub-micron pitches. We expect to have the same TDDB performance with hybrid bonding pitch reduction down to 200 nm pitch. We can conclude that the current Cu/SiO_2 hybrid bonding configuration is reliable from a TDDB point of view and does not present any road block for further pitch reduction, as long as the Cu_2O barrier is present at the interface.

We started this chapter by placing Cu diffusion and TDDB failure mechanisms as the major concerns for the Cu/SiO_2 hybrid bonding configuration with pitch reduction. The presence of the self-formed Cu_2O barrier strongly eliminates the importance of theses failure mechanisms and we believe to get the same reliable performance down to 200 nm of hybrid bonding pitch. We think, on the other side, that electromigration failure mechanism is the most critical with hybrid bonding pitch reduction due to the change of the killer void location to the hybrid bonding level. Hence, future studies should focus on assessing the EM failure with pitch reduction.

Chapter 4

Toward New Hybrid Bonding Configurations

This chapter focuses on exploring new hybrid bonding configurations with the aim of (a) studying further pitch reduction below 0.81 μm and (b) proposing solutions for the resistance-capacitance (RC) interconnect delay increase evidenced with pitch reduction for the current via+pad (HBV-HBM) standard configuration.

In chapter 2, we showed that 0.81 μm is close to the pitch limit for the via+pad (HBV-HBM) configuration since HBV and HBM have continuous shapes at those dimensions. Pitch reduction below 0.81 μm is no longer possible by only shrinking the HBM as the HBV size should also be reduced. This approach was not accessible for our study because of the design rules implemented for the specific technology node and for a thick metal level case. In addition, this approach would increase the total interconnect resistance since the HBV is the most resistive part of all the hybrid bonding elements. An alternative approach for pitch reduction below 0.81 μm is through spacing reduction between adjacent pads while keeping the HBM width constant (figure 4.1 (b)). This design will be evaluated in the first section of this chapter. Lower spacing between adjacent pads implies higher thermomechanical interactions, which might alter the electrical resistance behaviour of the hybrid bonding level. Hence, in the first section of this chapter, we aim to study the electrical behaviour of the hybrid bonding level with pitch reduction by adapting the approach of spacing reduction for a constant HBM size.

In the second section of this chapter, we aim to study new hybrid bonding configurations allowing RC delay reduction with hybrid bonding pitch reduction. Important consideration for the sub-micron pitch is the chip performance, which is mainly affected by the RC induced by interconnects. In chapter 2, we evidenced that pitch reduction by the HBV-HBM configuration leads to an increase in the RC interconnect delay, mainly driven by the capacitance increase. Even though assessing the degree of importance of the hybrid bonding level RC interconnect delay depends on the type of application, our objective is to study new designs allowing reduction of the RC delay. In the scope of my PhD, this problematic is targeted by adapting the geometric parameters of the hybrid bonding level, mainly by reducing the total thickness to achieve better RC. These new designs are referred afterwards as the HBV on HBM (figure 4.1 (c)) and the HBV only (figure 4.1 (d)) configurations that are processed mainly by eliminating the HBM level

from one or two wafers respectively. The main challenge of adapting these solutions is the establishment of Cu-Cu connections when bonding with HBV (theoretical width of 0.32 μm).

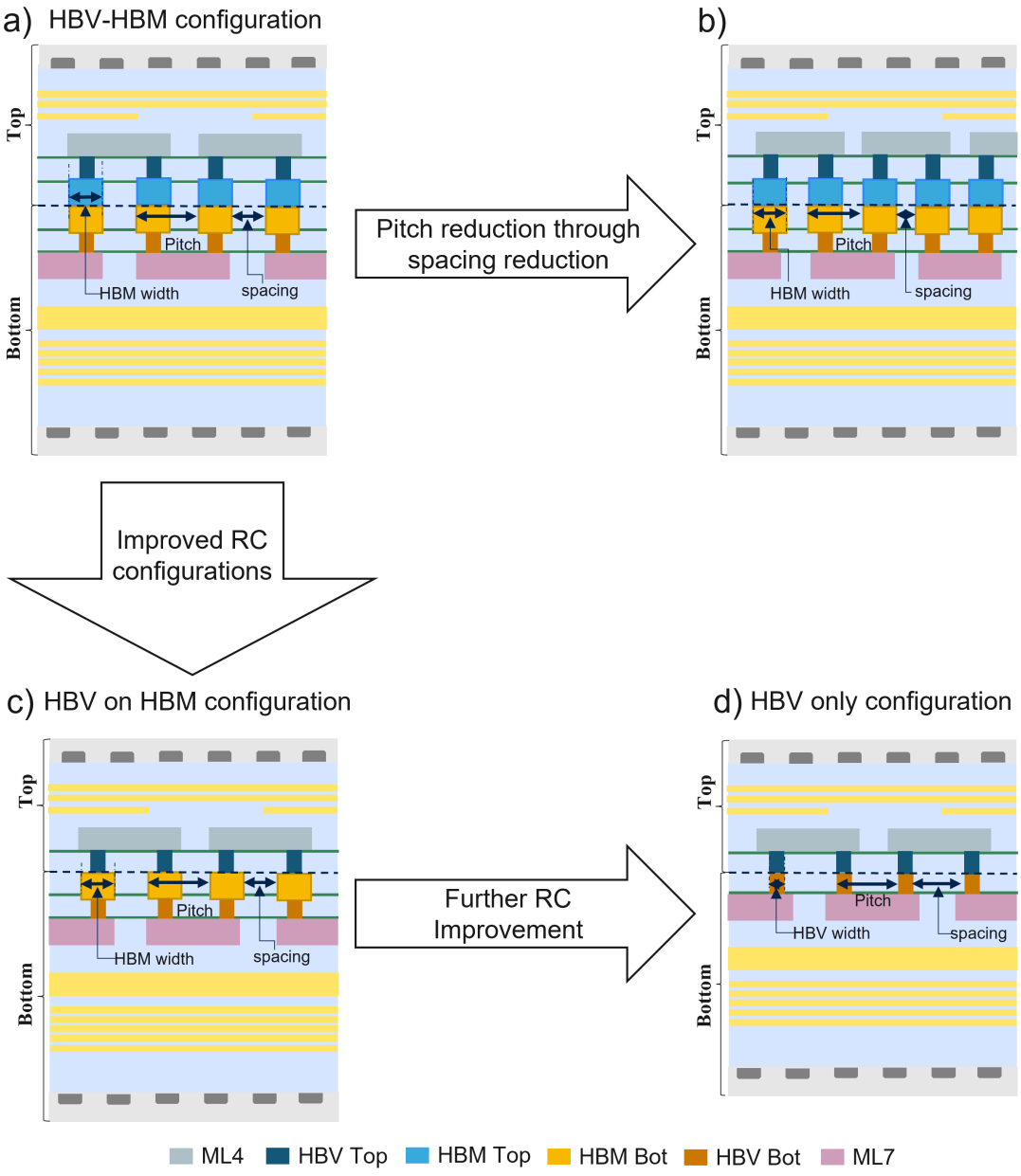

Figure 4.1: Schematic illustrations of a) standard HBV-HBM configuration (spacing = HBM width), b) HBV-HBM configuration with lower spacing (spacing < HBM width), c) HBV on HBM configuration and d) HBV only configuration.

4.1 Pitch reduction through spacing shrinkage

In this section, pitch reduction below 0.81 μm is explored by reducing the spacing between adjacent pads while keeping the HBM width constant.

This approach was reported in the literature by IMEC with a pad only configuration at interface and a top pad smaller than the bottom one. The author showed by SAM that bonding voids start occurring when the spacing is reduced between adjacent pads and especially when it leads to a Cu density above 30 % [77]. The structures with lower spacing between neighboring pads become weaker against interface voids that cause an increase in the unbonded area. The bonding voids in the high density regions could be attributed to the dielectric surface profile, in their case SiCN, near the Cu pads regions.

Moreover, the impact of reducing the spacing between adjacent pads on interface closure was investigated numerically by Sart [22]. The author showed that, for a given pad width and dishing, decreasing the spacing leads to a more difficult bonding. This was attributed to the vanishing vertical stress at the periphery of the interconnects. With decreasing spacing between adjacent pads, and under the annealing step, more compressive stresses are present at the pad edge, attenuating the expansion difference between the center and the edge of the pad and thus hindering dishing compensation.

In addition, one can suspect also that the dishing state at the Cu pad level is dependent on the Cu density for given CMP specifications. This observation was concluded by a study done by the Institute of Microelectronics (IME) in which they showed by AFM inspections, that the step height varies with the density in the case of Cu/SiO_2 interface [222]. Careful attention should therefore be made to the optimization of the CMP step to be adapted with a multi-density test vehicle.

Having all this in mind, adapting pitch reduction through reducing spacing between adjacent pads arises several challenges that need to be targeted:

1. What are the consequences of decreasing the spacing between adjacent pads on the electrical behaviour of the hybrid bonding level, namely the electrical resistance and capacitance?

2. With reduced spacing between adjacent pads, higher thermomechanical interactions are expected at the interface as shown by numerical simulations in [21]. Does the hybrid bonding interface remain mechanically stable after aging tests?

In the following sections, we will study the electrical behaviour and the robustness of the hybrid bonding level with pitch reduction below 0.81 μm.

4.1.1 Range of studied pitches

The electrical behaviour is studied with pitch reduction down to 0.675 μm. The structures are embedded in the TEDDY-UFP electrical test vehicle and are designed with the two HBM widths: 0.45 and 0.405 μm. The details are shown in table 4.1. The specific structures used to study the electrical behaviour with pitch reduction were presented in

figure 1.8. They consist of: (a) daisy chain (DC) structures with reduced spacing between adjacent pads for electric resistance study and (b) comb-comb structures for capacitance and leakage current study. The lengths of the structures are 100 links for the case of DC and at 1k interconnections for the com-comb case. The DC structure with the lowest pitch (0.675 μm) was not embedded in the electric test vehicle due to the design rule limit specifications at the metal lines level. The reference structures (with an equal spacing and HBM width) were presented in chapter 2 and will be used for comparison.

Table 4.1: Description of the structures used for pitch reduction study with spacing reduction on the TEDDY-UFP test vehicle.

Structure	Pad width 0.45 μm		Pad width 0.405 μm	
	Spacing s (μm)	Pitch P (μm)	Spacing s (μm)	Pitch P (μm)
A (reference)	0.45	0.9	0.405	0.81
B	0.4	0.85	0.35	0.755
C	0.35	0.8	0.305	0.71
D	0.3	0.75	0.27	0.675

4.1.2 Bonding results

For the structures with reduced spacing and constant HBM size, the dishing specifications were defined with respect to the reference structures (of equal spacing and HBM width) so as to keep a contact resistivity at the Cu-Cu interface below 10^{-11} $\Omega.cm^2$. The bonding results were presented in chapter 2. No bonding defects were evidenced by SAM with a resolution of 50 μm in the area of these structures. The overlay results of the 4 bonded pairs of the TEDDY-UFP test vehicle were also presented in chapter 2. In what follows, the wafer with the highest misalignment vector of 189 nm in average (wafer 01) is used to study the overlay limits with decreased spacing and pitch. The wafer with the lowest misalignment vector of 35 nm in average (wafer 04) will be used to study the electrical behaviour with pitch reduction.

4.1.3 Electrical characterization results

4.1.3.1 Overlay limit definition with pitch reduction

In chapter 2, we defined the overlay limits based on two criteria: the first limit corresponding to the 10 % increase in the interconnect resistance and the second is based on the occurrence of electric failures.

The 10 % increase criterion is dependent only on the HBM size and is not affected by the reduced spacing. Hence, the same overlay limits are applicable with reduced spacing as the reference structures with 0.9 and 0.81 μm pitches (0.45 and 0.405 μm of equal spacing and HBM size). This leads to overlay limits of $\pm$270 and $\pm$220 nm for the structures with HBM width of 0.45 and 0.405 μm respectively irrespective of the spacing.

As for the overlay limits based on electrical failure occurrence with reduced spacing/pitch, the comb-comb structure is used instead of the DC one. This is because the DC structures with decreased spacing have only 100 HBMs along one direction (Y direction). The highest misalignment values are along the X direction that makes incomplete the conclusions on the overlay limits when using the DC structures. The comb-comb structures embed HBMs along the X and Y directions. Therefore, these structures are sensible to both overlay directions. The results are shown in figure 4.2 (a) for the structures with HBM width of 0.405 μm. When the capacitance is at the 10^{21} pF level, this means that adjacent pads of the top and bottom combs are connected. We will take this criterion as an indication of the presence of electrical failure. We can see that, with pitch reduction by keeping the same HBM size, the overlay limits decrease. This is expected due to the reduced spacing between adjacent pads. The overlay limits are summarized in figure 4.2 (b) for the structures with HBM width of the 0.45 and 0.405 μm. For a given HBM width, the overlay limit decreases linearly with pitch reduction meaning that the electric failure is solely related to the decreased spacing between adjacent pads. For the structure with the lowest pitch at 0.675 μm, the overlay limits are at $\pm$210 nm. Even with a standard bonding tool performance ($\pm$200 nm), electric failures due to overlay should not be of a concern for the range of reduced pitches presented in our study. The advancement in W2W overlay accuracy down to $\pm$50 nm allows future possibilities to pitch reduction using the reduced spacing approach down to 0.5 μm pitch [223].

In the following sections, we will focus on the electrical resistance and capacitance with pitch reduction.

4.1.3.2 Electrical resistance behaviour

The cumulative distributions of a single interconnect resistance of a 100-link daisy chain structure with decreasing pitch are shown in figure 4.3 (a) for the HBM width of 0.45 μm and (b) HBM width of 0.405 μm. A 100 % electrical yield is observed with decreasing pitch down to 0.71 μm when the W2W overlay is below $\pm$200 nm. For a given HBM width of 0.45 and 0.405 μm, we can observe a slight decrease (< 2 %) in the single interconnect resistance for the different structures with decreasing pitch. We link the decrease in the electrical resistance to shorter metal lines. For instance, for the structures with HBM width of 0.45 μm, the corresponding length of the top/bottom metal lines is 1.368, 1.323, 1.161 and 1.116 μm for the 0.9, 0.85, 0.8 and 0.85 μm hybrid bonding pitch respectively. 3D FEM electrical simulations using COMSOL Multiphysics® are performed to verify this hypothesis.

A comparison between the mean experimental electrical resistance value with the numerical simulation results is shown in figure 4.4 for the case of HBM width of 0.45 μm. The FEM results match the mean experimental decrease trend with pitch reduction. We can therefore validate that the decrease in the electrical resistance observed with pitch reduction for a given HBM width is attributed to the decreased length of the top and bottom metal lines.

The above observation proposes that the contact resistivity at the Cu/Cu interface does not vary with pitch reduction through reduced spacing. In chapter 2, we found that the contact resistivity for the reference structures with an equal spacing and HBM width

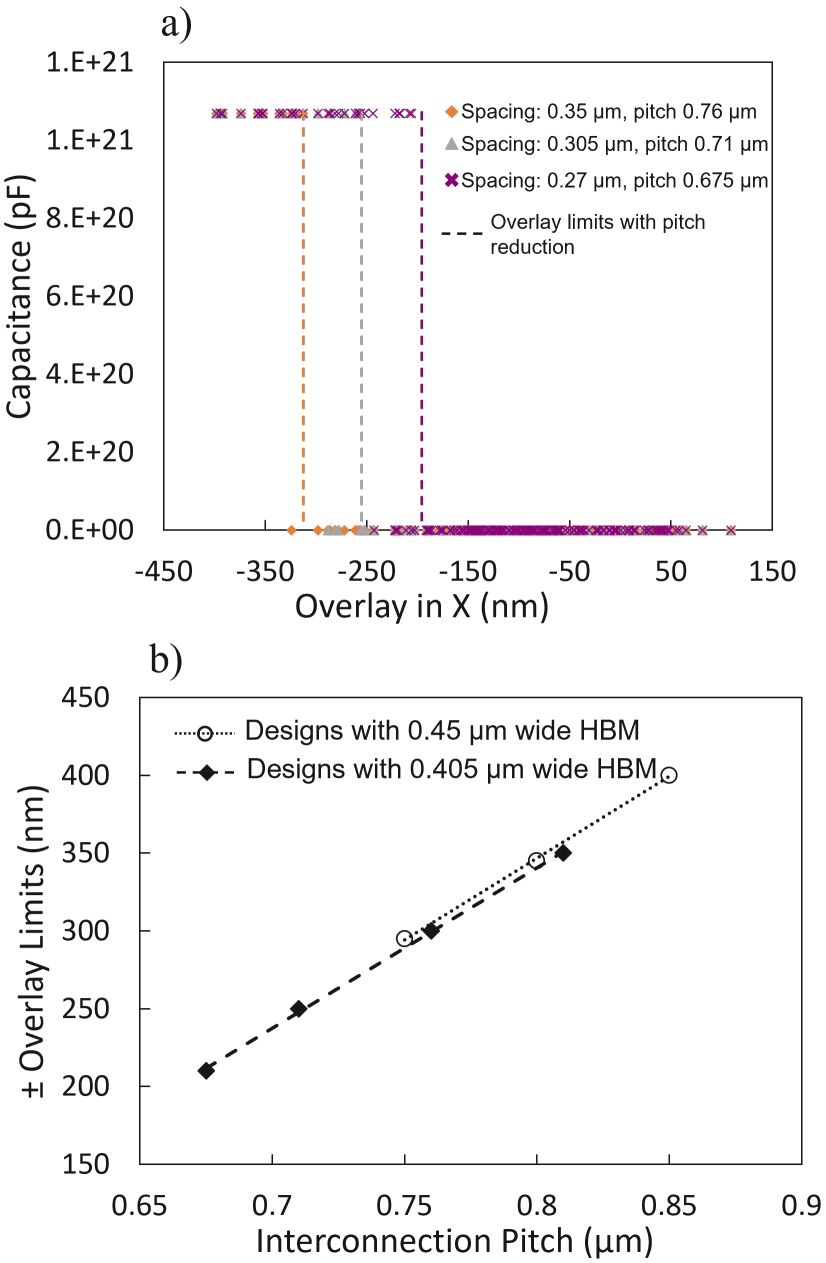

Figure 4.2: (a) Capacitance vs. overlay in X with reducing spacing/pitch for the comb-comb structures with 1k interconnections on the TEDDY-UFP test vehicle and HBM width of 0.405 μm. (b) Summary of the overlay limits vs. interconnection pitch for the different structures with HBM width of 0.45 and 0.405 μm.

is below 10^{-11} $\Omega.cm^2$ when bonding with HBM width of 0.45 and 0.405 μm. We can conclude that the electrical quality at the Cu/Cu interface is not affected in the studied ranges of Cu pads width and pitches. Pitch reduction down to 0.71 μm is validated from an electrical resistance point of view. This observation should be assigned on much larger structures in future studies.

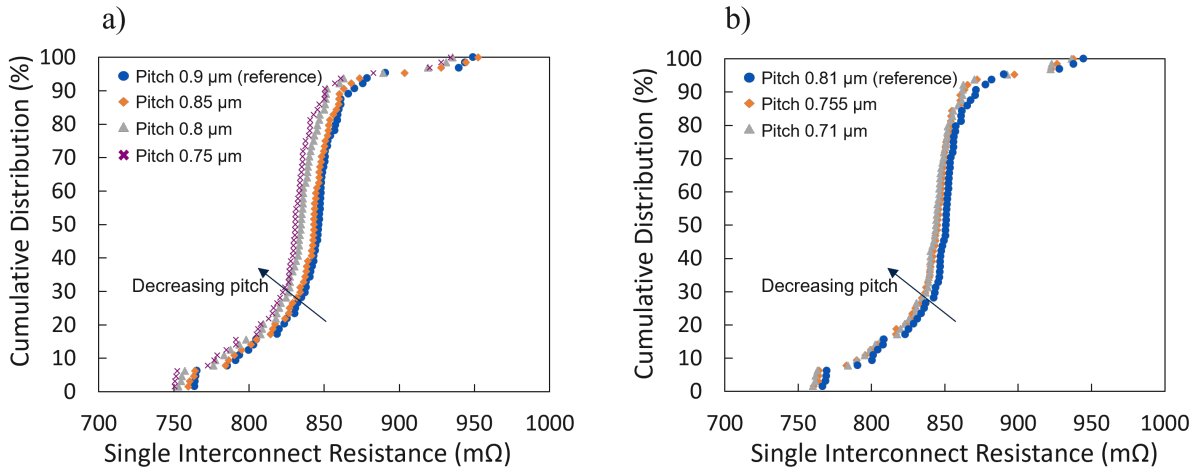

Figure 4.3: Cumulative distributions of a single link resistance of a 100-link daisy chain structure with decreasing pitch for a) HBM width of 0.45 μm and b) HBM width of 0.405 μm on the wafer with a misalignment vector of 35 nm in average of the TEDDY-UFP test vehicle (wafer 04).

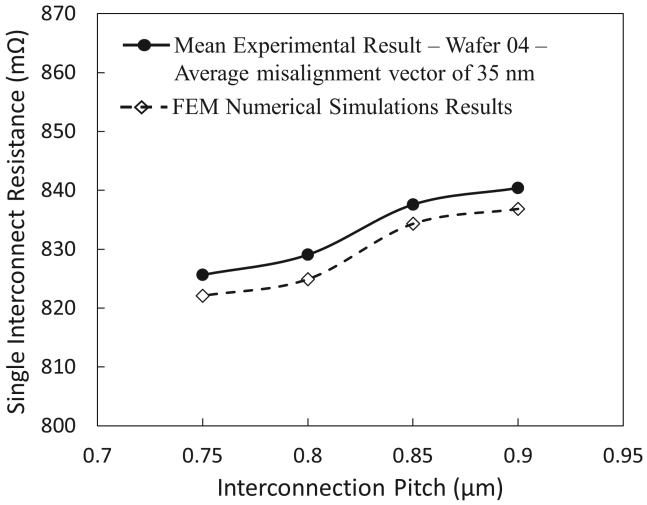

Figure 4.4: Comparison between the mean experimental electrical resistance results of wafer 4 (average misalignment vector of 34 nm) of TEDDY-UFP test vehicle with the ones obtained by FEM simulations for the DC structures with HBM width of 0.45 μm as a function of the interconnection pitch.

4.1.3.3 Electrical insulation properties

In order to verify the dielectric insulation properties with pitch reduction through reducing spacing between adjacent pads, parametric tests with a low potential difference of 3.3 V is applied between the top and bottom combs of the comb-comb structures with 1k interconnections (figure 1.8 (b)). The objective is to check the presence of electrical shorts with pitch reduction and not to breakdown.

The results are shown in figure 4.5 for the different comb-comb structures with a) HBM width of 0.45 μm and b) HBM width of 0.405 μm. The leakage current is plotted as a function of the calculated spacing between the 3D combs with the latter found by subtracting the overlay from the theoretical spacing. The leakage current is independent

of the spacing and varies between 3 to 6 $\times 10^{-12}$ A whatever the pitch. The interconnects remain well insulated with pitch reduction through reducing spacing down to 0.675 μm pitch, when the applied voltage is 3.3 V. We therefore believe that the strategy of pitch reduction through reducing spacing between adjacent pads does not harm the dielectric insulation properties.

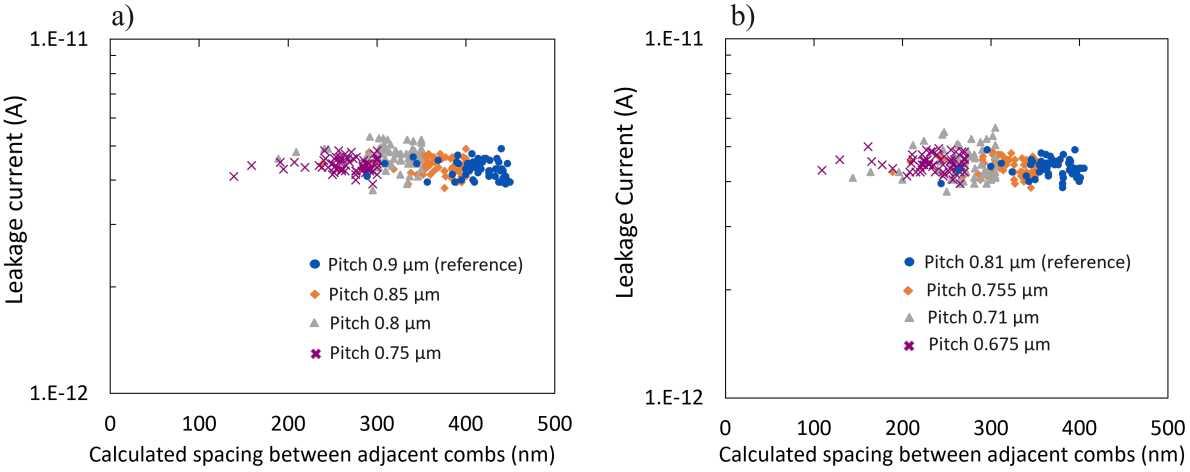

Figure 4.5: Leakage current as a function of the calculated spacing between adjacent combs for the 3D comb-comb structures with pitch reduction for a) HBM width of 0.45 μm and b) HBM width of 0.405 μm for the TEDDY-UFP wafer with an average misalignment vector of 35 nm (wafer 04).

4.1.3.4 Electrical capacitance behaviour

Since the pitch is reduced through decreased spacing between adjacent HBM pads while keeping the thickness of the hybrid bonding level constant, an increase in the capacitance is expected with pitch reduction. This is studied experimentally using the comb-comb structures with 1k interconnections. The cumulative distributions of the capacitance per area (pF/μm^2) are shown in figure 4.6 for the different structures with pitch reduction. For a given HBM width, pitch reduction through decrease spacing leads to an increase in the capacitance that is in line with the theory in equation 2.6. In addition, we can clearly see that the capacitance variations increase with pitch reduction through reduced spacing. The mean values and standard deviations are summarized in table 4.2.

For the 0.405 μm HBM width case, the mean capacitance per area increased by 199 % (almost the double) when decreasing the theoretical spacing from 0.405 μm (0.81 μm pitch) down to 0.27 μm (0.675 μm pitch). Moreover, the standard deviation increases with reduced spacing and pitch whatever the HBM width. We think this is linked to the process parameters variations such as HBM width and overlay. In chapter 2, we showed that the impact of the different process parameters increases with pitch reduction down to 0.81 μm. The impact of these process parameters, including overlay, is expected to continue increasing with further pitch reduction by reduced spacing. This can explain the higher standard deviations observed. It is possible to confirm these observations by extending the range of the DoCE models presented in chapter 2 to study the pitch ranges through reducing spacing. This subject was not addressed during my PhD and should be

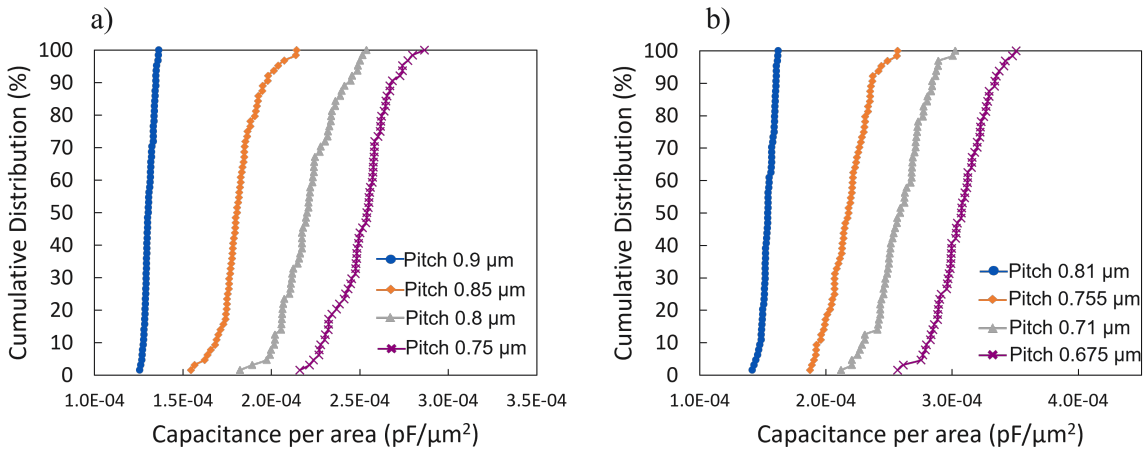

Figure 4.6: Cumulative distributions of the capacitance per area (pF/μm^2) for the different 3D comb-comb structures with pitch reduction with a) HBM width of 0.45 μm and b) HBM width of 0.405 μm for wafer 04 of the TEDDY-UFP test vehicle.

targeted in future studies.

Table 4.2: Mean experimental value and standard deviation of the capacitance per area of the comb-comb structures with different HBM width and pitches on the TEDDY-UFP test vehicle.

Structures with pad width 0.45 μm				Structures with pad width 0.405 μm			
Spacing s (μm)	Pitch P (μm)	Mean value $\times 10^{-4}$ (pF/μm^2)	standard deviation $\times 10^{-5}$ (pF/μm^2)	Spacing s (μm)	Pitch P (μm)	Mean value $\times 10^{-4}$ (pF/μm^2)	standard deviation $\times 10^{-5}$ (pF/μm^2)
0.45	0.9	1.31	0.26	0.405	0.81	1.54	0.48
0.4	0.85	1.82	1.17	0.35	0.76	2.17	1.62
0.35	0.8	2.21	1.56	0.305	0.71	2.59	1.99
0.3	0.75	2.51	1.59	0.27	0.675	3.07	2.02

4.1.3.5 Robustness of the hybrid bonding level

With the reduction of the spacing between adjacent pads, higher pad to pad interactions are expected with higher thermomechanical stresses at the hybrid bonding interface. This increases the risk of delamination and thermally activated phenomena such as the stress induced voiding mechanism. The robustness of the structures with reduced pitch through spacing reduction at a constant HBM width are studied by the following aging tests:

1. Thermal cycling (TC) test with the temperature range of -65 °C and +150 °C according to JEDEC standard JESD22-A104 [145].

2. High temperature storage (HTS) tests at 175°C for 1000 hours according to JEDEC JESD22-A103 [151].

For clarity, we will represent the variations of the structures with the lowest pitch for each HBM width. The resistance variations after TC and HTS tests are shown in figure 4.7 (a) as studied on DC structures with 100 interconnection links. With pitch reduction down to 0.71 μm though reduced spacing, the resistance variations after both tests in the range of ± 0.1 %. First, these results are well below the ± 10 % failure criterion. Second, these variations are identical to the reference structures with an equal spacing and HBM width presented in chapter 3. This clearly indicates that the hybrid bonding level is robust with pitch reduction down 0.71 μm and the approach of pitch reduction through spacing does not rise any particular risk from a mechanical stability and SiV point of views within the performed aging test conditions.

Moreover, to study if the dielectric insulation properties are altered with reduced spacing after both aging tests, the leakage current is tracked on comb-comb structures with 1k interconnections. A voltage difference up to 40 V is applied between the top and bottom combs to study the behaviour under elevated electric fields. The leakage current variations ($\frac{I_{final}}{I_{initial}}$) are shown in figure 4.7 (b). The leakage current variations are well below the 100 defined failure criterion. In addition, the observed variations are within the same range of the leakage variations tracked on reference samples with no aging performed on identical test bench and same measurement times as the samples after tests. Therefore, we can attribute the leakage variations observed in 4.7 (b) to measurement errors. We can conclude that with pitch reduction down to 0.675 μm through reduced spacing, the dielectric properties remain intact after aging tests even under high voltage conditions of 40 V.

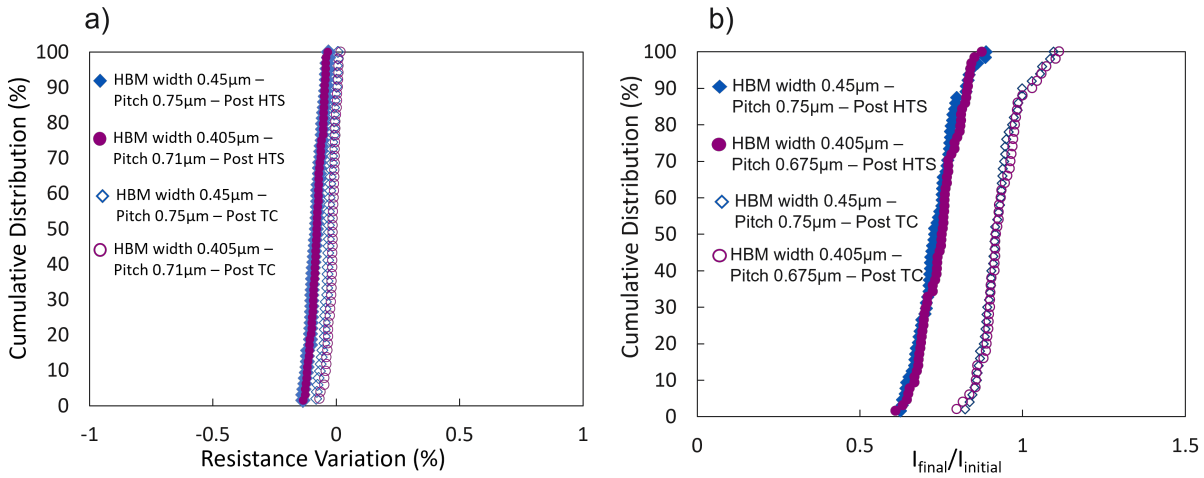

Figure 4.7: Cumulative distributions of a) resistance variations and b) leakage current variations for the structures with HBM width of 0.45 and 0.405 μm and lowest pitch on the TEDDY-UFP test vehicle after TC and HTS aging tests.

For future studies, we propose to further push the TC cycles and HTS hours beyond the standard conditions that can give more insights on the robustness of the hybrid bonding level for the approach of pitch reduction through reduced spacing. This would allow to validate or not the activation of any failure mechanism.

4.1.4 Discussion

In this section, we focused on studying pitch reduction for the via+pad (HBV-HBM) hybrid bonding configuration through reduced spacing between adjacent pads while keeping the HBM width constant. The following main discussions can be made:

1. **Bonding feasibility:** structures with reduced spacing/pitch and a surface below 10^{-3} mm^2 were embedded in the TEDDY-UFP test vehicle for the HBM widths of 0.45 and 0.405 μm. No local bonding defect was evidenced by SAM in contrary to a previous study done by IMEC where bonding voids start occurring when the Cu density is above 30 % [77]. This could be related to a difference in the surface characteristics before bonding as compared to our present study.

2. **Overlay limit definition:** reducing the spacing between HBM restricts the acceptable overlay limits. Based on our results, for the lowest pitch studied of 0.675 μm, the overlay limit is around ±210 nm. This accuracy in W2W overlay is achievable with the standard bonding tool performance. From the overlay perspective, and for the HBM size of 0.405 μm, pitch reduction through reduced spacing is theoretically possible down to 0.5 μm pitch, taking into consideration the latest W2W overlay development with an accuracy of ±50 nm [223].

3. **Electrical behaviour with reduced spacing:**

   - **Electrical resistance**: based on our studies with the HBM width of 0.45 and 0.405 μm, we found that reducing the spacing between adjacent pads while keeping the HBM size constant does not impact the electrical resistance behaviour. For a given HBM width, the same electrical resistance behaviour was obtained with pitch reduction down to 0.71 μm pitch. No modification of the Cu-Cu interface resistance is seen despite the calculations made by Sart who reported that reducing the spacing makes interface closure more difficult [22]. We believe this is linked to the adequate dishing specifications defined with respect to the contact resistivity criterion below 10^{-11} $\Omega.cm^2$. In addition, we question if the bonding voids seen by IMEC in their study might be related to their specific dishing specifications, making interface closure with increased Cu density not possible. We therefore recommend to adapt the dishing threshold leading to a contact resistivity below 10^{-11} $\Omega.cm^2$, to secure interface closure after annealing even with pitch reduction down to 0.71 μm.

   - **Electrical capacitance**: as expected, the capacitance increases with the reduced spacing taking into account that the thickness of the hybrid bonding level is kept constant. Depending on the application, this increase in capacitance might significantly increase the total IC RC interconnect delay and can have a negative impact on the overall performance. This could be a roadblock for adapting these configurations with reduced pitch. A simple solution is possible by reducing the thickness of the hybrid bonding level leading to lower capacitance. On the other side, with reducing spacing between pads, the dielectric keeps its insulation properties.

4. **Reliability risks:** pitch reduction through reduced spacing could rises specific challenge with regard to the time dependent dielectric breakdown failure mechanism, which can alter the conduction mode under time with the application of electric

field. This can also affect the projected performances at use conditions. Taking the example of a BEoL study with low-k dielectric, it was found that the failure time under TDDB reduces with decreased spacing between adjacent Cu pads [224]. For our hybrid bonding case, we have studied in chapter 3 the TDDB failure mechanism at the interface on structures having spacing between pads down to 50 nm. Hence, we believe that adapting the range of the hybrid bonding pitches studied in this section should not rise any particular risk in TDDB as we expect to have the same performance and conduction mechanism. Regarding the electromigration failure mechanism, we believe that pitch reduction through reduced spacing should not alter the performance with respect to the reference structures with equal spacing and HBM width mainly because the HBM width is unchanged.

Based on the results of our study, pitch reduction through reduced spacing opens the door for 3D stacking with an interconnect density above 2.10^8 $interconnects/cm^2$ as shown in figure 4.8. This is the most advanced interconnect density reported until this day using the hybrid bonding technology [225].

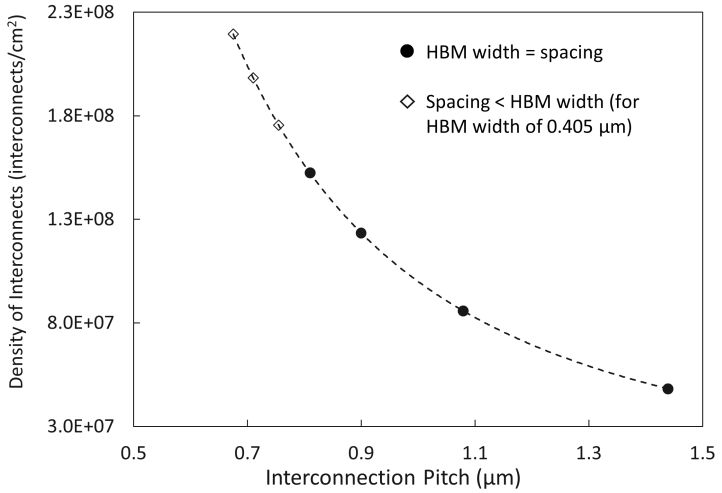

Figure 4.8: The interconnect density (in $interconnects/cm^2$) vs. interconnection pitch based on the different results in this thesis.

4.1.5 Conclusion

In this section, we studied the approach of reducing the hybrid bonding pitch below 0.81 μm by reducing the spacing between adjacent pads. The same electrical resistance behaviour was evidenced down to 0.71 μm despite the reduced spacing that theoretically induces more difficult bonding. This is attributed to the adequate dishing specifications that allow to secure a contact resistivity at the interface below 10^{-11} $\Omega.cm^2$, even with reduced spacing. High electric yield is also guaranteed even with the standard bonding tool performance. The robustness of the hybrid bonding level with pitch reduction through reduced spacing was validated by aging tests. The hybrid bonding interface, despite the higher thermomechanical stresses at the hybrid bonding level due to reduced spacing, seems to remain mechanically stable. This could be attributed to the high bonding energy at the Cu/SiO_2 hybrid bonding interface. The hybrid bonding pitch limit with

this approach is directly driven by the specific design rules for each technological node and depending on the metal line level. In our case, the design rules are with respect to a thick metal level. Further pitch reduction is only possible by switching to thin metal layers with less restricted design rules for a given technological node. This study was launched for demonstration on a single metal level but could not be completed within the scope of my PhD. Furthermore, depending on the application type, a possible roadblock to adapt pitch reduction through reduced spacing could be linked to the increased capacitance. Possible solutions could be envisaged to compensate this increase by simply reducing the thickness of the hybrid bonding level.

4.2 Hybrid bonding configurations for RC delay reduction

Two new hybrid bonding configurations are studied in the next sections as shown in figure 4.9. For these configurations, the TEDDY-FP test vehicle is used. These are based on reducing the hybrid bonding stack total thickness to reduce the RC delay. The lowest hybrid bonding pitch is 1.44 μm. The two configurations are described as following:

1. The HBV on HBM configuration: a schematic illustration is shown in figure 4.9 (b). On the top wafer, only the via (HBV) level is processed while keeping the process of the bottom wafer identical to the standard via+pad (HBV-HBM) configuration (figure 4.9 (a)). The hybrid bonding level thickness of the top wafer (HBV+HBM) is reduced from 1.2 down to 0.5 μm so a decrease in the capacitance is expected. A decrease in the electrical resistance is also theoretically expected since the resistance of the top HBM is eliminated. In addition, since the Cu pads at the hybrid bonding interface have dissimilar sizes, we expect an overlay tolerance between $\pm 250nm$ for the 1.44 μm pitch in which the electrical resistance in independent on the W2W overlay.

2. The via (HBV) only configuration as shown schematically in figure 4.9 (c). The top and bottom wafer levels are processed with the HBV level only. A significant decrease in the total thickness of the hybrid bonding stack is expected from 2.4 μm down to 1 μm, leading to even more decrease in the capacitance as compared to the HBV on HBM configuration. Since the top and bottom HBMs are not processed, a decrease in the electrical resistance is theoretically expected. The sensibility of the HBV only configuration to W2W overlay should be studied since bonding is done with Cu pads of 0.32 μm of theoretical size.

In the following sections, the bonding results and electrical characterizations of these new configurations are presented. Discussions will include the robustness studies of the hybrid bonding level under aging tests as well as the pertinence of adapting these configurations in the sub micron pitch region.

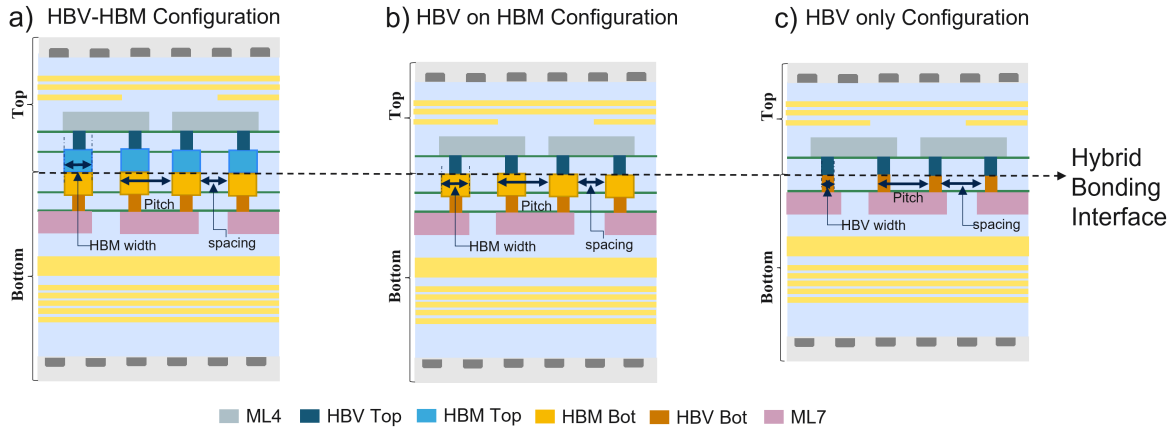

Figure 4.9: Schematic illustrations of a) the HBV-HBM standard configuration, b) the HBV on HBM configuration and c) HBV only configuration.

4.2.1 HBV on HBM configuration

4.2.1.1 Bonding process and results

The process of the electrical test vehicles done with the HBV on HBM configuration is detailed in Appendix C, section C.1. The process of the bottom wafer is identical to the HBV-HBM configuration. As for the top wafer, a single damascene process is adapted to process the HBV level only. Four pairs of wafers with the TEDDY-FP test vehicle are used to study the feasibility of this design. The overlay results of the 4 bonded wafers are detailed in Appendix C, section C.2. After bonding and annealing at 380 °C for 2 hours, SAM is used to check the presence of any bonding defects at the wafer level. A SAM example after bonding for the HBV on HBM configuration with the TEDDY-FP test vehicle is shown in figure 4.10 (a). No bonding defect can be seen at the wafer level using SAM with a 50 μm resolution. As discussed in chapter 2, a black signal of SAM does not necessarily imply the presence of Cu-Cu contacts, which can only be confirmed by electrical measurements.

To physically characterize the interface, a TEM cross section is performed inside a daisy chain structure with 1.44 μm pitch as shown in figure 4.10 (b). No gap exists at the interface between the HBV and HBM after annealing, for this particular location. From the TEM cross section, important observation can be made regarding the trapezoidal shape of the HBV between the top and bottom wafers (represented by d and D that are the small and large diameters respectively). For the bottom wafer with the dual damascene process, the HBV parameters d and D are 310 and 380 nm respectively as compared to 270 and 350 nm of the HBV of the top wafer with the single damascene process. Smaller HBV sizes are obtained on the top wafer that should be considered when analyzing the electrical results. The ratio between d and D ($\alpha = \frac{d}{D}$) is similar between the top and bottom wafers. The HBV size variations are induced by the change from the dual to the single damascene process.

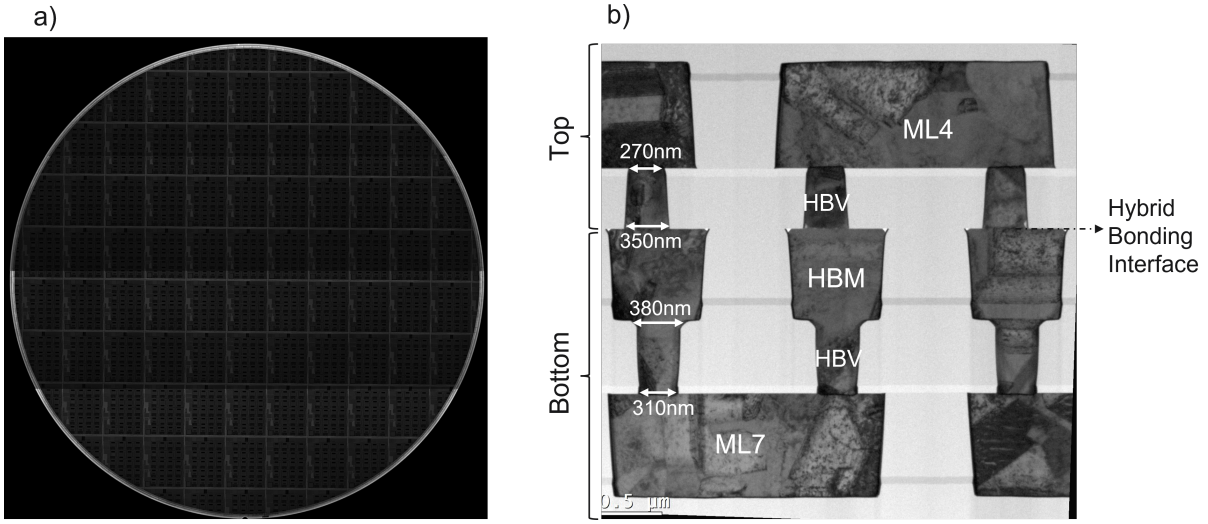

Figure 4.10: a) SAM image after bonding annealing of 300 mm wafer with the HBV on HBM configuration with TEDDY-FP test vehicle and b) cross section image by TEM of bonded structure inside a daisy chain with 1.44 μm pitch.

In the following sections, we will present the electrical characterizations results with the aim of studying the Cu-Cu connections and the status on the RC characteristic.

4.2.1.2 Electrical characterization results

Electrical resistance

The cumulative distribution of a single link resistance of a 5k-links daisy chain structure with 1.44 μm pitch is shown in figure 4.11 for the four wafers processed with the HBV on HBM configuration. The result of a single wafer processed with the HBV-HBM standard configuration on TEDDY-FP test vehicle with the same pitch is added for comparison. A 100 % electrical yield is obtained on all wafers with W2W overlay below $\pm$250 nm. Higher electrical resistance (up to 7 % on average) are obtained on the wafers with the HBV on HBM configuration as compared to the HBV-HBM one. We believe that this is linked to smaller shape of HBV on the top wafer (check figure 4.10 (b)). The results of the mean electrical resistance values along with the standard deviations are summarized in table 4.3. The variations observed between the 4 wafers of the HBV on HBM configurations are mostly not attributed to the impact of W2W overlay. This is because the HBV on HBM configuration is independent of overlay in the range $\pm$250 nm. In addition, wafer 04 with the lowest electrical resistance values is the one with the highest W2W overlay (check figure C.2).

To study the origin of these variations and the increase in electrical resistance as compared to the HBV-HBM configuration, FEM is used. The mean values of the shape and height of the different elements in the stack are considered in the simulations as issued from the width dimensions after etching and thickness measurements. We will assume that the parameters of the bottom wafer are similar between the two configurations, taking into consideration that the process of the HBV-HBM configuration on TEDDY-FP is robust. The details of the 3D models used in the FEM simulations for the HBV-HBM and the HBV on HBM configurations (for wafer 04) are available in appendix C, section C.3. The FEM results are included in table 4.3. The increase in electrical resistance observed experimentally is also predicted by simulations. This is mainly linked to the smaller HBV shape on the top wafer from the single damascene process, leading to higher electrical resistance. The wafer-to-wafer variations for the HBV on HBM configuration are attributed to the process parameters variations mainly the shape and height of the HBV of the top wafer.

Lower standard deviations are obtained on the wafers with the HBV on HBM configuration as compared to the standard one (see table (4.3). Possible reasons include:

1. Lower HBV size variations of the top wafer: even though the top wafer has smaller HBV as compared to the bottom one, the variations in diameter at the wafer level are tighter that could explain the lower standard deviations obtained for the wafers with the HBV on HBM design. In other words, the simple damascene process induces lower variation of the HBV diameter at the wafer level as compared the double damascene process.

2. Impact of overlay: the configuration with HBV on HBM design is not sensible to

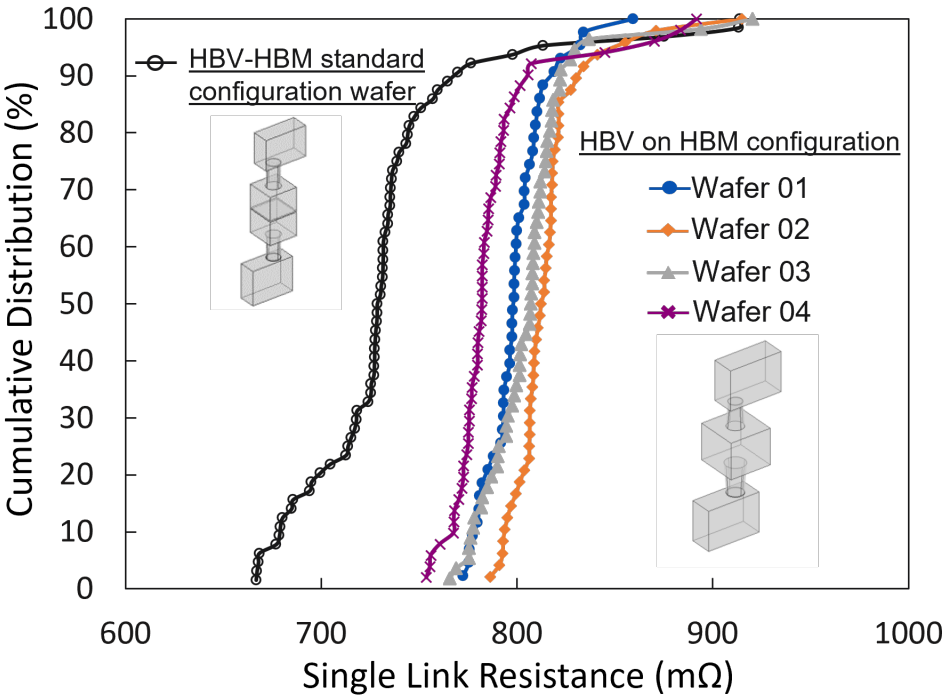

Figure 4.11: Cumulative distributions of the single link resistance of a 5k-links DC structure with 1.44 μm pitch for the different wafers processed with the TEDDY-FP test vehicle with the HBV on HBM configuration. The result of a single wafer processed with the HBV-HBM standard configuration on TEDDY-FP with the same pitch is shown for comparison.

overlay up to ±250 nm in which the same contact area is obtained. For the HBV-HBM configuration, the ±250 nm range of overlay could induce up to 5 % variation of the electrical resistance. This could explain in a part the lower standard deviation obtained for the HBV on HBM configuration.

Table 4.3: Summary of the experimental electrical resistance results of the single link resistance of a 5k-links DC structure and 1.44 μm pitch on the wafers with HBV-HBM standard configuration and the HBV on HBM one processed with the TEDDY-FP test vehicle. The FEM result is also included

Configuration type	HBV-HBM standard configuration	HBV on HBM configuration			
Wafer number	-	01	02	03	04
Mean electrical resistance ($m\Omega$)	733.5	799.6	815.5	806.2	787.9
Std deviation ($m\Omega$)	47.3	16.6	20.9	25.1	27.6
FEM Result ($m\Omega$)	731.2	795.2	810.5	803.12	782.92

Electrical capacitance

Moving to the electrical capacitance of the HBV on HBM configuration, this is studied on comb-comb structures with 57k interconnections and 1.44 μm pitch. The cumulative

distributions of the capacitance per area are shown in figure 4.12. A single wafer with the HBV on HBM design is only shown. For the 1.44 μm pitch, a 30 % decrease of the capacitance per area for the configuration with the HBV on HBM design is obtained. This is mainly linked to the reduced stack thickness by suppressing the HBM level on the top wafer. Even though the mean electrical resistance increased up to 7 % with the new HBV on HBM configuration, an RC delay reduction is expected due to the decrease in the capacitance.

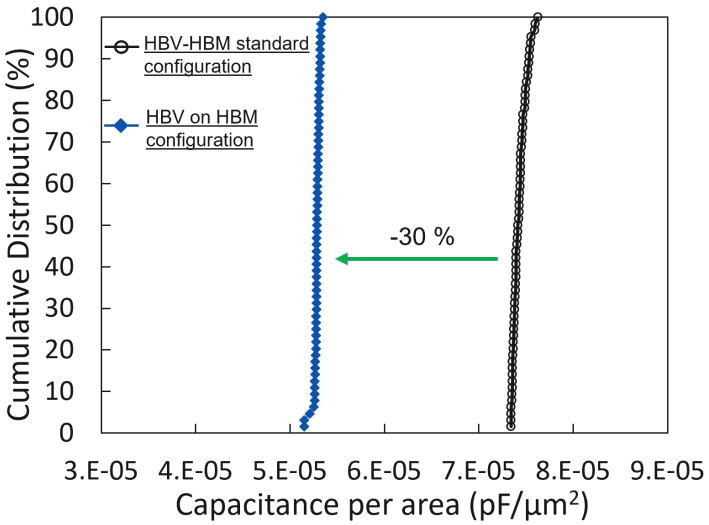

Figure 4.12: Cumulative distribution of the capacitance per area of comb-comb strcutures with 57k interconnections and 1.44 μm pitch processed with the TEDDY-FP test vehicle for standard HBV-HBM and HBV on HBM configurations.

Important question arises on the pertinence of this configuration with the reduction of the hybrid bonding pitch below 1.44 μm. To answer this, RC projections with pitch reduction are presented in the following section.

Projection with pitch reduction

Numerical simulations are used to study the pertinence of the HBV on HBM configuration with the reduction of the hybrid bonding pitch. For comparison, the mean experimental electrical resistance and capacitance results of the TEDDY-UFP presented in chapter 2 are used. For the electrical resistance, the numerical simulations results of the HBV on HBM configuration are adjusted with respect to the mean experimental result over the 4 wafers with 1.44 μm pitch. As shown in figure 4.13 (a), the electrical resistance of the HBV on HBM configuration with pitch reduction is closer to the HBV-HBM one. This can be explained by the fact that the electrical resistance increase linked the shrink of the HBM size with pitch reduction is lower for the HBV on HBM configuration that has only one HBM. For the 0.81 μm pitch, the expected electrical resistance increase is only 2.7 %. For the capacitance aspect, as shown in figure 4.13 (b), the expected capacitance decrease for the HBV on HBM configuration is higher with pitch reduction and is around 36 % for the 0.81 μm pitch as compared to the HBV-HBM configuration. We hence believe that the pertinence of the HBV on HBM design is greater with the reduction of the

hybrid bonding pitch. For the 0.81 μm pitch, the RC interconnect delay from the hybrid bonding level is reduced by more than 30 % with respect to the HBV-HBM configuration.

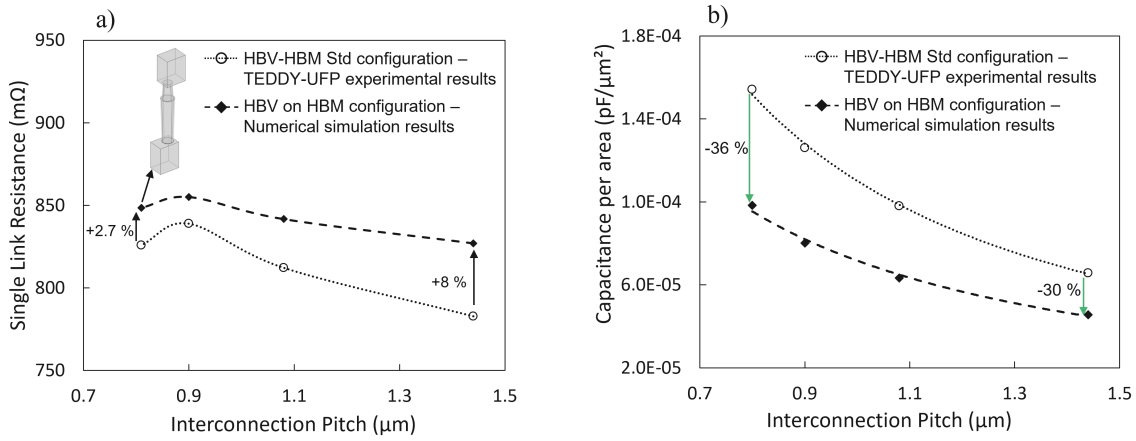

Figure 4.13: Projected electrical behaviour with pitch reduction for the HBV on HBM configuration using numerical simulations for a) the electrical resistance and b) the capacitance per area. The experimental results of the TEDDY-UFP test vehicle with the HBV-HBM configuration are presented for comparison.

4.2.1.3 Robustness of the HBV on HBM configuration

Due to the size mismatch of the Cu pads between the top and bottom wafers, important concerns arise on the mechanical stability of the HBV on HBM configuration. The robustness of the HBV on HBM configuration with 1.44 μm pitch is studied by the mean of the TC and HTS aging tests with conditions presented in section 4.1.3.5.

The resistance variations are studied on daisy chain structures with 5k interconnections and 1.44 μm pitch. The results are shown in figure 4.14 (a). All the structures passed the ± 10 % failure criterion and the resistance variations after both tests are below ± 1 %. In addition, a negligible leakage current variation is observed on the comb-comb structures with 57k interconnections and 1.44 μm pitch after both aging tests as shown in figure 4.14 (b). All the structures passed the leakage current $\frac{I_{final}}{I_{initial}}$ failure criterion of 100.

We can conclude that adapting the HBV on HBM configuration with 1.44 μm pitch does not raise any particular risk from a mechanical stability and Stress induced Voiding (SiV) point of views in the range of TC and HTS tests conditions performed. Future studies should target the mechanical stability of the interface by going beyond the standard JEDEC conditions to assess the presence of any failure.

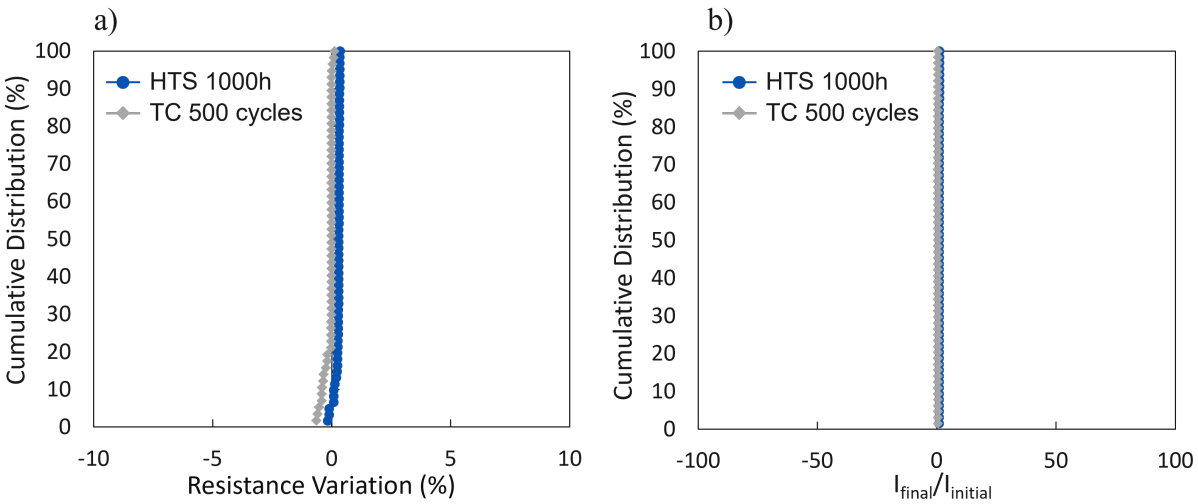

Figure 4.14: a) resistance variations after TC and HTS tests on DC structures with 1.44 μm pitch and b) leakage current ratio $\frac{I_{final}}{I_{initial}}$ variations on comb-comb structures with 57k interconnections and 1.44 μm pitch for wafer processed with the HBV on HBM configuration on the TEDDY-FP test vehicle.

4.2.2 HBV only configuration

After evaluating the HBV on HBM design, this section focuses on studying the HBV only configuration in which hybrid bonding is performed with the HBV level.

4.2.2.1 Bonding process and results

The process of the electrical test vehicles done with the HBV only configuration is detailed in Appendix D, section D.1. The process is identical between the top and bottom wafers and consists of processing the HBV level only of the TEDDY-FP test vehicle with a single damascene process. When bonding with ~0.32 μm wide Cu pads, careful attention should be made to the dishing level in order to secure Cu-Cu connections. A specific CMP is developed and adapted to induce dishing that lies below the 10^{-11} $\Omega.cm^2$ contact resitivity criterion defined in chapter 2. Seven pairs of wafers of the TEDDY-FP test vehicle are used to study the feasibility of the HBV only design. The overlay results of the 7 bonded wafers are detailed in Appendix D, section D.2 (check figure D.2). W2W overlay below ±250 nm is obtained on all wafers both in X and Y directions, which is typical to the standard bonding tool alignment performance. After bonding and annealing at 380 °C for 2 hours, SAM is used to check the presence of any bonding defects at the wafer level. A SAM example after bonding for the HBV only configuration with the TEDDY-FP test vehicle is shown in figure 4.15 (a) where no bonding defects can be seen at the wafer level with a 50 μm spatial resolution.

To physically characterize the interface, a TEM cross section is performed inside a daisy chain structure with 1.44 μm pitch as shown in figure 4.15 (b). We can clearly see that no gap exists between the top and bottom HBV after annealing. However, this does not confirm the presence of Cu-Cu electrical connections at the interface that can only be assessed by electrical measurements. From the TEM cross section, we can confirm the observations made on the HBV shapes for the single damascene process where smaller

HBVs are obtained as compared to the dual damascene HBV-HBM process. It should be mentioned that the design HBV diameter is 0.32 μm. By taking the average between d and D, the single damascene process seems to produce HBV diameters that are closer to the design HBV diameter as compared to the dual damascene process.

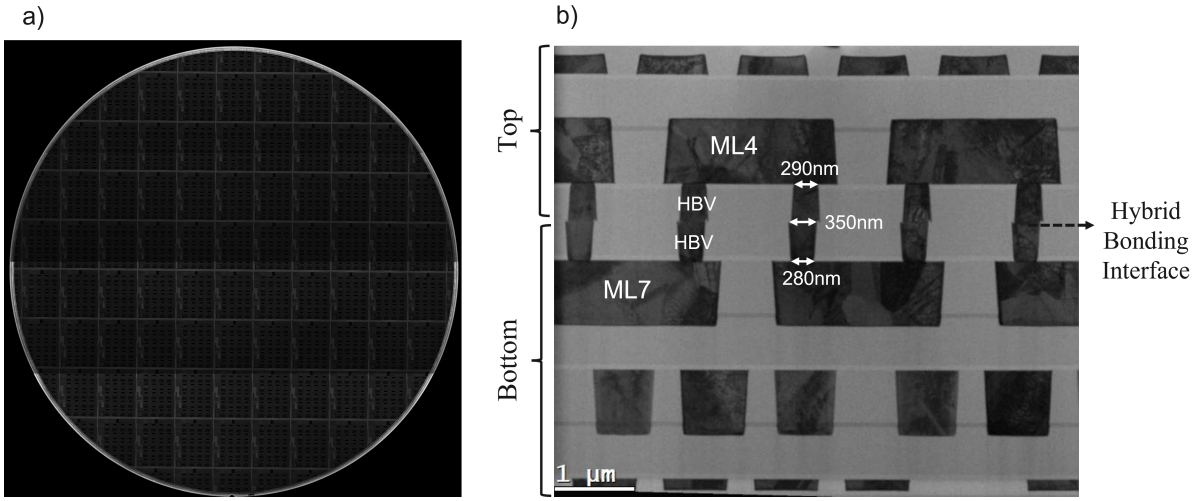

Figure 4.15: a) SAM image after bonding annealing of 300 mm wafer of the HBV only configuration with the TEDDY-FP test vehicle and b) cross section image by TEM of bonded structure inside a daisy chain with 1.44 μm pitch.

In the following sections, we will present the electrical characterizations results with the aim of studying the Cu-Cu electrical connections at the interface and any improvement on the RC interconnect delay.

4.2.2.2 Electrical characterizations

Electrical resistance

The electrical resistance behaviour of the HBV only configuration is studied on DC structures with 5k-links and 1.44 μm pitch. The cumulative distributions of a single link resistance for the different wafers are shown in figure 4.16. The result of a single wafer processed with the HBV-HBM standard configuration on TEDDY-FP test vehicle with the same pitch is added for comparison. Electrical resistance increase of 15 % as compared to HBV-HBM configuration is evidenced. As compared to the HBV on HBM design presented in section 4.2.1.2, an additional 8 % increase in electrical resistance can be deduced. Hence, the HBV on HBM design that has the top wafer processed with the single damascene process lies in between the HBV-HBM and HBV only configurations. The electrical increase observed in figure 4.16 can also linked to the smaller size of the HBV when processed with the single damascene process and will be verified later on by numerical simulations.

The variations in the electrical resistance between the 7 different wafers could be linked to a possible impact of process variations parameters, including W2W overlay. When bonding with the HBV level only, higher sensibility to overlay is obtained as shown in figure 4.17 with the help of numerical simulations. Assuming an ideal contact at

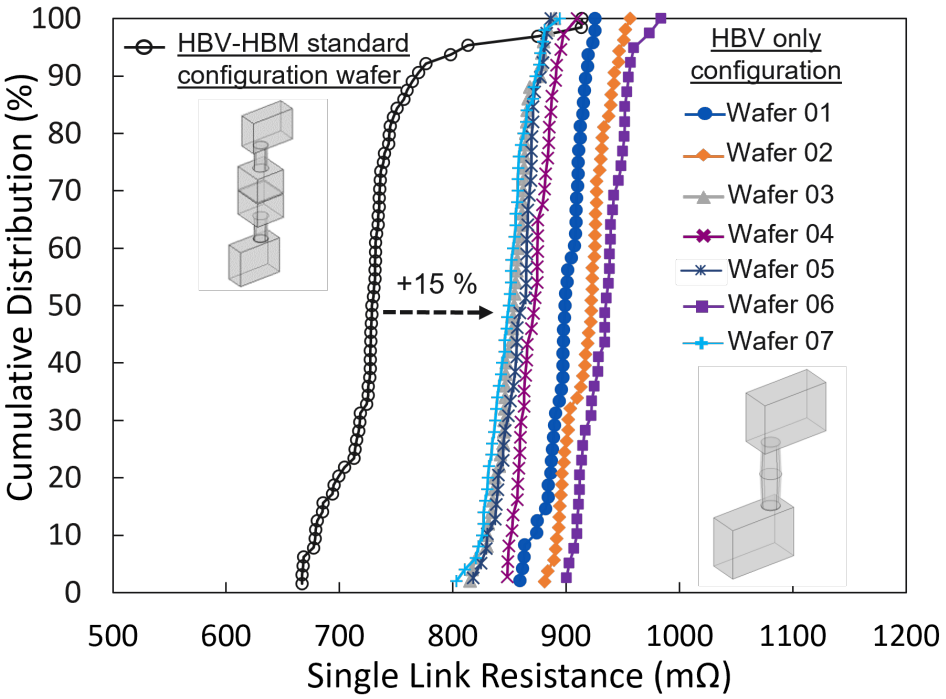

Figure 4.16: Cumulative distributions of the single link resistance of a 5k-links DC structure with 1.44 μm pitch for the different wafers processed with the TEDDY-FP test vehicle and the HBV only configuration. The result of a single wafer processed with the HBV-HBM standard configuration on TEDDY-FP with the same pitch is shown for comparison.

the interface, the electrical resistance increases by more than 40 % with an overlay of 200 nm in both directions. The overlay limit based on the 10 % resistance increase criterion defined in chapter 2 leads to a limit of ±135 nm. This overlay limit is, however, independent of the hybrid bonding pitch down to 0.81 μm, since the HBV size is constant.

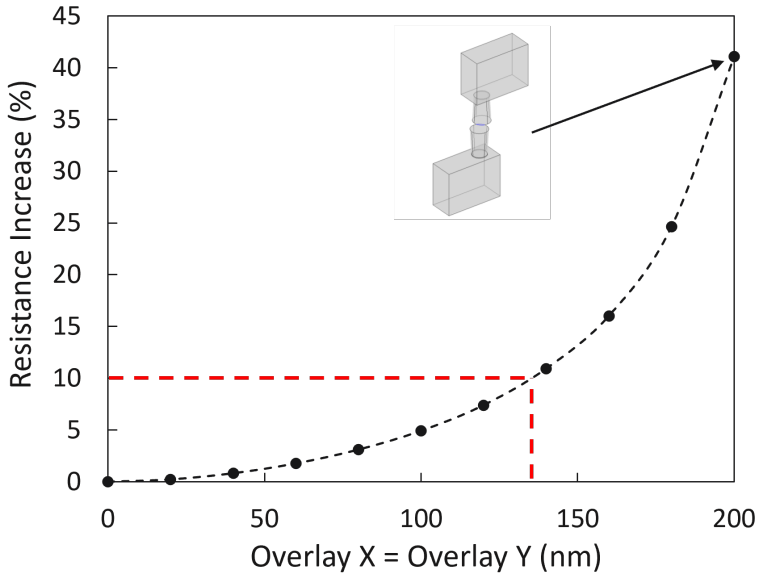

Figure 4.17: FEM results of the electrical resistance increase vs. overlay for the HBV only configuration with 1.44 μm pitch.

The results of the mean electrical resistance values along with the standard deviations for the different studied wafers are summarized in table 4.4. FEM is used to study the origin of the electrical resistance variations between the different wafers and the increase in electrical resistance as compared to the HBV-HBM configuration. The mean values of the shape and height of the different elements are considered in the simulations. In addition, since the impact of the W2W overlay is significant, the mean values in X and Y directions for each wafer are also considered. The details on the 3D model used for the FEM simulations for the HBV only configuration (wafer 07) are presented in appendix D, section D.3. The results of FEM simulations are shown in table 4.4. The FEM electrical resistance result is always lower than the mean experimental. Taking the hypothesis that the difference between the experimental and numerical resistance is attributed to the contact resistance impact, the calculation leads to a contact resistivity at the Cu-Cu interface below 4×10^{-12} $\Omega.cm^2$ for all wafers. In addition, the same increase trend between FEM and measurements is observed between the different wafers. We can confirm that the electrical resistance increase of the HBV only configuration with respect to the HBV-HBM one is mainly linked to the smaller HBV shape on the top and bottom wafers from the single damascene process. The wafer-to-wafer variations for the HBV only configuration are attributed to the process variation parameters: mainly the shape and height of the HBV of the top and bottom wafer as well as the impact of W2W overlay.

Table 4.4: Summary of the experimental electrical resistance results of a single link resistance of a 5k-links DC structure and 1.44 μm pitch of the wafers with HBV only configuration along with the result of one wafer with the HBV-HBM standard configuration processed with the TEDDY-PF test vehicle. The FEM simulation results are also included.

Configuration type	HBV-HBM standard configuration	HBV only configuration						
Wafer number	-	01	02	03	04	05	06	07
Mean electrical resistance ($m\Omega$)	733.5	898.8	918.4	853	872	857.7	934.2	848.6
Std deviation ($m\Omega$)	47.3	16.8	19.1	16.5	15	16.5	19.4	18.7
FEM Result ($m\Omega$)	731.2	892.7	912.5	846.8	864.6	850.2	928.4	840.03

In addition, lower standard deviations are obtained on the wafers with the HBV only configuration as compared to the standard one. We think it is related to lower HBV shape variations: even though the top wafer has smaller HBV as compared to the bottom one, the variations in diameter at the wafer level are tighter as compared to the HBV-HBM configuration.

Hybrid bonding with the HBV level only is possible by respecting the dishing specifications to get a negligible impact of contact resistivity. Higher electrical resistance ($\sim$15 %) was evidenced as compared to the HBV-HBM configuration that is mainly linked to the smaller size of the HBV, and is not attributed to the electrical quality of the Cu-Cu connections at the interface that is below 10^{-11} $\Omega.cm^2$.

Electrical capacitance

The capacitance of the HBV only configuration is studied on comb-comb structures with 57k interconnections and 1.44 μm pitch. The cumulative distributions of the capacitance per area are shown in figure 4.18 for one wafer processed with the HBV only configuration as compared to the standard HBV-HBM configuration with 1.44 μm pitch. A significant decrease by around 66 % is observed for the HBV only configuration. This can be explained by (a) the height of the hybrid bonding stack reduced from 2.4 μm for the HBV-HBM configuration down to $\sim$ 1 μm for the HBV only configuration and (b) the higher spacing between adjacent HBVs (1.12 μm) as compared to a spacing of 0.72 μm between adjacent HBMs for the HBV-HBM configuration. Despite the increase in electrical resistance, the overall RC interconnect delay of the hybrid bonding level is reduced by around 60 % for the HBV only configuration at the 1.44 μm pitch.

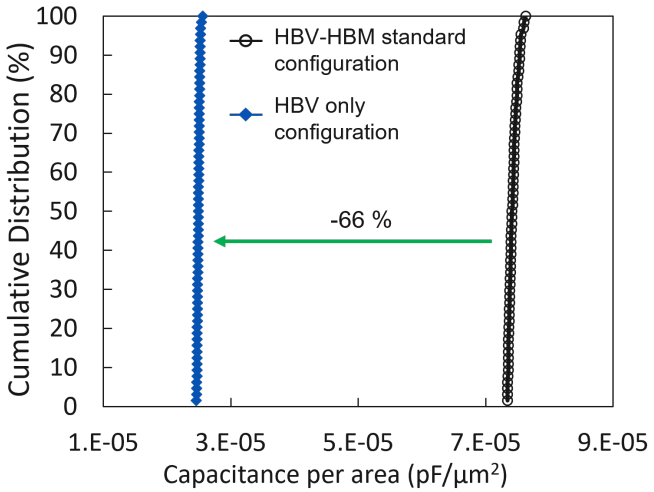

Figure 4.18: Cumulative distributions of the capacitance per area of the comb-comb strcutures with 57k interconnections and 1.44 μm pitch processed with the HBV-HBM and HBV only configurations with the TEDDY-PF test vehicle.

Here again, we question the pertinence of adapting the HBV only configuration for sub micron pitches. That's why, in the following section, numerical simulations are used to project the RC interconnect delay with pitch reduction down to 0.81 μm.

RC projection with pitch reduction

In order to study the pertinence of adapting the HBV only configuration with pitch reduction below 1.44 μm, we will use FEM to predict the electrical resistance and capacitance with pitch down to 0.81 μm. The mean experimental results of the TEDDY-UFP presented in chapter 2 are used for comparison. For the electrical resistance, the numerical simulations results of the HBV only configuration are adjusted to reflect the mean experimental result of the 7 wafers with 1.44 μm pitch. Assuming the same process is

adapted with pitch reduction, we expect reduced electrical resistance for the HBV only configuration as shown in figure 4.19 (a). The resistance increase with HBM shrink is not present for the HBV only configuration. The resistance decrease is attributed to the decreased lengths of the top and bottom metal lines. At 1.44 μm pitch, the electrical resistance is 15 % higher for the HBV only configuration as compared to the HBV-HBM one. For the 0.81 μm pitch, the electrical resistance difference is only around 3 %. The capacitance gain for the HBV only configuration increases with pitch reduction and is around 75 % for the 0.81 μm pitch as compared to HBV-HBM configuration.

Adapting the HBV only configuration is an effective solution to compensate the RC interconnect delay increase with pitch reduction obtained with the standard HBV-HBM configuration. In fact, adapting this new design with 0.81 μm pitch guarantees a hybrid bonding level RC delay reduction by more than 70 % as compared to the HBV-HBM configuration with similar pitch.

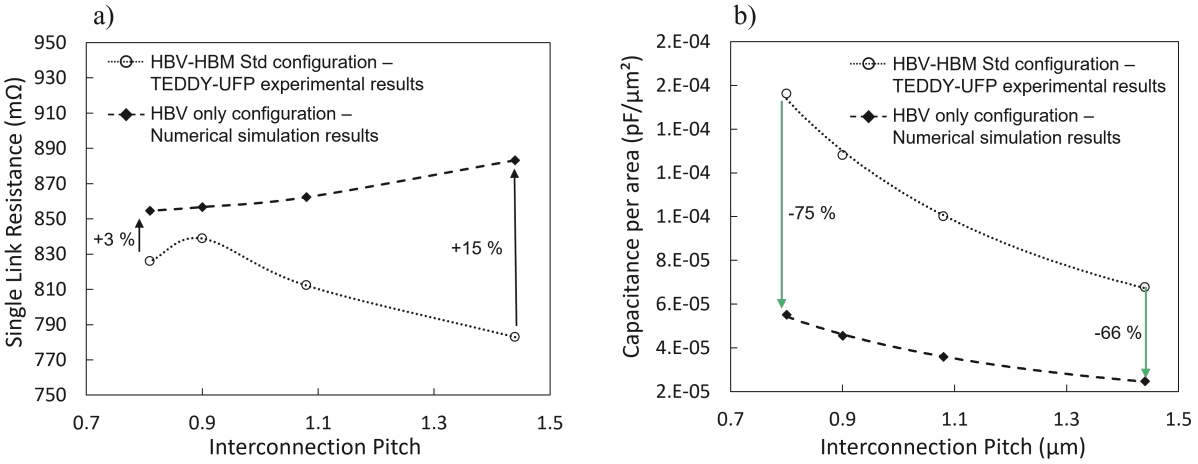

Figure 4.19: Projected electrical behaviour with pitch reduction for the HBV only configuration using numerical simulations for a) the electrical resistance and b) the capacitance per area. The experimental results of the TEDDY-UFP test vehicle with the HBV-HBM configuration are presented for comparison.

4.2.2.3 Robustness of the HBV only configuration

A critical concern for the HBV only configuration is the robustness of the hybrid bonding level. The overall Cu-Cu bonding area with respect to the SiO_2/SiO_2 one is reduced. In addition, for the studied pitch of 1.44 μm, the distance between adjacent pads at interface is increased meaning that the local Cu density is reduced. This might lower the bonding energy at the hybrid bonding interface. The integrity and mechanical stability of the Cu-Cu interface could therefore be in risk. In addition, due to the low contact area, initial voids present at the hybrid bonding interface could evolve toward killer voids at the HBV level. In fact, an electromigration study done by IMEC with a pad only configuration and a size mismatch between top and bottom showed that initial voids at the interface affects the EM performance. We question if any voids present for our hybrid bonding case could also assist the SiV phenomenon and therefore should be verified.

The robustness of the hybrid bonding level with the HBV only configuration is studied by TC and HTS tests with the conditions presented in section 4.2.1.3. The resistance variation is studied on a daisy chain structures with 5k-links and 1.44 μm pitch. The results are shown in figure 4.20 (a). All the structures passed ± 10 % failure criterion and the resistance variations after both tests are below ± 1 %. We can conclude that the Cu-Cu interface is mechanically stable even when bonding with pads as small as 300 nm in width. Moreover, a negligible leakage current variation is observed on the comb-comb structures with 57k interconnections after both aging tests. All the structures passed the leakage current $\frac{I_{final}}{I_{initial}}$ failure criterion of 100 as shown in figure 4.20 (b).

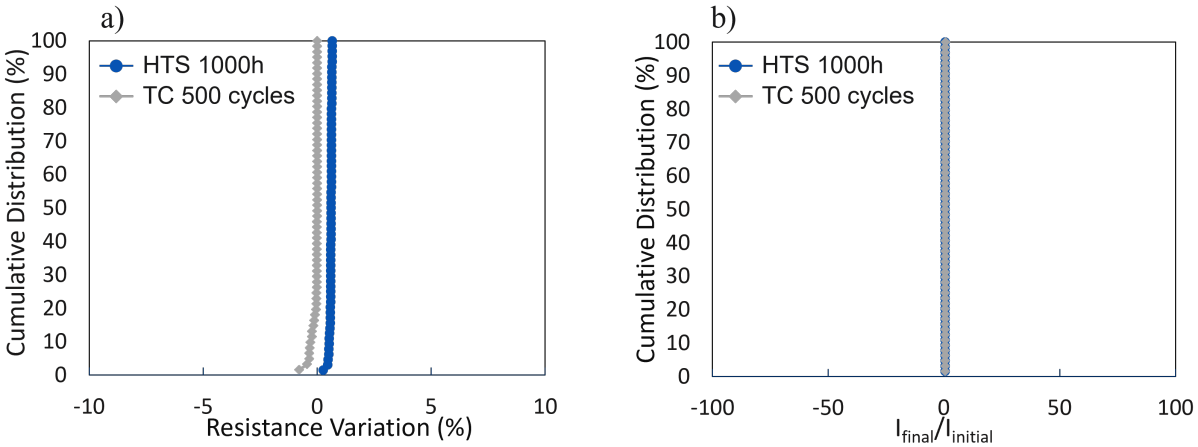

Figure 4.20: a) resistance variations after TC and HTS tests on DC structures with 1.44 μm pitch and b) leakage current ratio $\frac{I_{final}}{I_{initial}}$ variations on comb-comb structures with 57k-links and 1.44 μm pitch for wafer processed with the HBV on HBM configuration with the TEDDY-PF test vehicle.

We can conclude that the hybrid bonding level with the HBV only design, in which hybrid bonding is done with 0.32 μm wide Cu pads, is mechanically stable and does not rise any particular risk when aging with the standard TC and HTS JEDEC conditions. We recommend to push forward the TC and HTS conditions to confirm the robustness at high aging conditions.

4.2.3 Discussion

In this section, new hybrid bonding configurations were explored with the aim of reducing the RC interconnect delay from the hybrid bonding level with the reduction of the hybrid bonding pitch. The following main discussions can be made:

1. **HBV on HBM design:** this configuration is obtained by bonding the HBV level only of the top wafer to a bottom wafer processed with the HBV-HBM levels. This design is close to the one adapted by IMEC, which uses a pad only at the interface with a width mismatch between the top and bottom Cu pads [226]. This approach is also adapted by YMTC that uses the via+pad (HBV-HBM) configuration [38]. In their case, the HBV size varies between the top and bottom wafers. Within the scope of my PhD, this configuration was explored with the main objective of

reducing the thickness of the hybrid bonding level, to improve both the electrical resistance and capacitance. Based on our studies, the following observations can be made:

- **Electrical resistance behaviour**: up to 8 % increase in the electrical resistance of the HBV on HBM design was evidenced as compared to the HBV-HBM one for the 1.44 μm pitch, which is directly linked to the smaller size of the HBV with the single damascene process. This configuration allows an overlay tolerance of $\pm$250 nm for the 1.44 μm pitch in which the electrical resistance is independent of overlay. With pitch reduction, lower overlay tolerances are expected. For instance, for the 0.81 μm pitch, the theoretical overlay tolerance is only $\pm$40 nm. Adapting this approach would not to be of a major interest with the standard bonding tool performance of $\pm$200 nm. However, this configuration could be beneficial with the advancing bonding tool accuracy, with the latest developments allowing the achieve an overlay accuracy of $\pm$50 nm [223].

- **Electrical capacitance behaviour** : for the 1.44 μm pitch, adapting the HBV on HBM design allows 30 % reduction in capacitance as compared to the HBV-HBM configuration. The same capacitance gain is expected by adapting the HBV on HBM configuration down to 0.81 μm. We therefore believe that the pertinence of this configuration is much higher with sub micron pitches and could lead to a 30 % reduction of the RC delay from the hybrid bonding level for the 0.81 μm pitch.

- **Robustness of the HBV on HBM configuration**: Based on our aging studies, we found that the HBV on HBM configuration with a width mismatch between the top and bottom Cu pads is mechanically stable for the 1.44 μm pitch, within the standard JEDEC TC and HTS test conditions. We expect to get the same behaviour with pitch reduction down to 0.81 μm.

- **Reliability of the HBV on HBM configuration:**

- A possible risk of adapting the HBV on HBM configuration could be linked to the electromigration failure mechanism. We question if the killer void location will stay at the hybrid bonding level or will return back to the metal line levels. This concern originates for the results of the EM study done by IMEC with a size mismatch between the top and bottom pads who showed that the EM killer location depends on the electrons flow directions [153]. A competition between two different EM degradation modes could take place at the hybrid bonding level. In light of the EM results for HBV-HBM configuration with 1.44 μm pitch presented in chapter 3, having only the HBV level at the top wafer could influence the time-to-failures under electromigration since the top HBM was believed to act as a reservoir effect. We therefore believe that the electromigration failure mechanism could be a potential concern for adapting the HBV on HBM configuration and should be evaluated especially in the sub micron pitch region.

- Adapting the HBV on HBM configuration does not pose any risk in regard of TDDB failure mechanism despite the fact the higher surface of Cu is in direct contact of SiO_2. The Cu_2O layer is believed to be present at the Cu/SiO_2 interface, acting as barrier to Cu diffusion. Moreover, the HBV on HBM configuration allows

higher spacing between adjacent pads at the top wafer level. The HBV on HBM configuration is believed to be reliable down to 0.81 μm pitch from the TDDB and interface stability to Cu diffusion point of views.

2. **HBV only configuration:** this configuration is obtained by hybrid bonding with the HBV level only on the top and bottom wafers. The bonding is done with a Cu via width of $\sim$0.32 μm. This design is similar to the one adapted, for example, by ON Semiconductor [140] and IMEC [226] but in our case the top and bottom Cu pads are of similar sizes. Based on our studies, the following observations can be made:

   - **Electrical resistance behaviour:** for the 1.44 μm pitch, a 15 % increase in the mean electrical resistance of the HBV only design was evidenced as compared to the HBV-HBM one, which is also directly linked to the smaller size of the HBV processed with the single damascene step. The main challenge of the HBV only configuration is with respect to its sensibility to W2W overlay. In order to maintain the 10 % increase criterion, the overlay should not exceed $\pm$130 nm, even with the 0.81 μm pitch. With the latest advancements in W2W down to an accuracy of $\pm$50 nm, this problematic can be ¨neglected¨.

   - **Electrical capacitance behaviour:** for the 1.44 μm pitch, adapting the HBV only configuration allows 66 % reduction in capacitance as compared to the HBV-HBM design with the same pitch level. This is linked to the decreased hybrid bonding level thickness of the top and bottom wafers. By numerical simulations, we expect to get the same capacitance gain with the HBV only configuration down to 0.81 μm pitch. The pertinence of adapting this configuration is much higher with sub micron pitches and can lead to more than 70 % decrease of the RC delay from the hybrid bonding level for the 0.81 μm pitch.

   - **Robustness of the HBV only configuration**: based on our aging studies, we found that the HBV only configuration that embeds hybrid bonding with 0.32 μm wide Cu pads is mechanically stable for the 1.44 μm pitch, for the standard JEDEC TC and HTS test conditions. Based on the good robustness evidenced in chapter 3 for the HBV-HBM configuration down to 0.81 μm pitch, we believe that the HBV only configuration will remain robust with pitch reduction down to 0.81 μm. This is also linked to the constant pad size at the interface for the HBV only design, independent of the pitch down to 0.81 μm.

   - **Reliability of the HBV only configuration:**

   - Adapting the HBV only configuration rises concerns with respect to the EM failure mechanism, similarly to the HBV on HBM design. In addition, for the HBV only design and because of low contact area when bonding with 0.32 μm wide Cu pads, any cavities present at the hybrid bonding interface could impact the EM performance. Hence, the EM failure mechanism should be evaluated for the HBV only design.

   - The HBV only design does not rise any particular risk from the TDDB aspect. This is because for a given pitch, the distance between adjacent HBVs is higher than

the spacing between neighboring HBMs in the case of the HBV-HBM configuration. We think that the HBV only design is reliable down to 0.81 μm pitch from the TDDB and interface stability to Cu diffusion point of views.

If proven to satisfy the electromigration requirements at use conditions, we believe that the HBV only configuration will be of great interest taking into account the latest W2W advancements [223]. We highly recommend adapting this configuration with pitch reduction down to 0.81 μm. This will have a significant positive impact by improving the overall integrated circuit RC interconnect delay.

4.2.4 Conclusion

In this section, we have studied two new hybrid bonding configurations with the aim of achieving an improved electrical resistance and capacitance behaviours with pitch reduction. The explored hybrid bonding configurations are the HBV on HBM and the HBV only designs which consist of eliminating the HBM level from one or two wafers respectively. A slight increase in the electrical resistance was obtained experimentally for the 1.44 μm pitch as compared to the HBV-HBM design. This increase is only linked to the smaller size of the HBV from the specific single damascene process and does not reflect any issue of the electrical connections at the Cu-Cu interface. Adjusting the etch process to get larger HBVs and lower electrical resistance with the single damascene process is possible. This is, however, of a minor interest since we expect to get closer electrical resistance of the two new configurations to the HBV-HBM design with reduction down to 0.81 μm. For the 1.44 μm, a significant improvement of the hybrid bonding level capacitance by adapting the HBV on HBM and HBV only designs is obtained corresponding respectively to 30 and 60 % reduction with respect to the HBV-HBM design. The hybrid bonding levels of the two studied configurations with 1.44 μm are mechanically stable, and no particular risks were evidenced after standard aging tests conditions. In conclusion, the two new configurations do improve the hybrid bonding RC interconnect delay for a given pitch as compared to the standard HBV-HBM design. We think that the HBV only design is the most adequate to adapt with the connection pad size reduction that allow a significant decrease of the RC interconnect delay.

4.3 Chapter 4 conclusion

In this chapter, we focused on exploring new hybrid bonding designs with the aim (a) achieving further reduction below 0.81 μm and (b) improving the hybrid bonding RC interconnect delay with pitch reduction.

For the first objective, we adapted the approach of decreasing the spacing between neighboring pads while keeping the HBM width constant. With the 0.45 and 0.405 μm wide HBMs, pitch reduction down to 0.71 μm do not alter the electrical resistance behaviour and especially the Cu-Cu electrical connections at the hybrid bonding interface. This was made possible by respecting the dishing threshold to get a negligible contribution of contact resistivity. Pitch reduction down to 0.675 μm is possible from an overlay perspective even with the standard bonding tool accuracy ($\pm$200 nm). This could open the door to 3D stacking by Cu/SiO_2 hybrid bonding with an interconnect density up to 2.10^8 $interconnects/cm^2$. A possible roadblock of adapting this approach could be attributed to the capacitance increase originated from the reduced spacing which could negatively impact the total RC delay. Possible solution could be achieved by simply reducing the total hybrid bonding level thickness.

The problematic of capacitance increase was also evidenced when reducing the hybrid bonding pitch by keeping an equal size of HBM width and spacing. In order to mitigate the RC increase from the hybrid bonding level, we studied new hybrid bonding configuration designs to achieve our second objective. The solution was based on reducing the hybrid bonding level thickness by processing the HBV level only on either one or two wafers to be bonded. The HBV on HBM design allows a 26 % RC reduction for the 1.44 μm pitch while allowing an overlay tolerance by $\pm$250 nm. By simulations, this design keeps its pertinence with pitch reduction down to 0.81 μm. The HBV only design allows even more hybrid bonding level RC delay reduction by more than 60 % for the 1.44 μm pitch with respect to the HBV-HBM standard design. This latter design allows higher RC delay reduction with pitch reduction down to 0.81 μm. The two new explored designs are mechanically stable after the standard TC and HTS tests, for the 1.44 μm. Based on these results, and if proven to satisfy the required electromigration performances under use conditions, we think it is of great interest to directly adapt the HBV only design in the production process of consumer products. Beside its benefits on the RC delay improvement, adapting this design will lower both the product's production cost and time.

General Conclusion and Perspectives

General Conclusion

The hybrid bonding integration has emerged in the last decade as a key process solution for the 3D integration technology, which allows vertical stacking of multi-functional and technological chips. In an earlier work, a hybrid bonding pitch down to 1.44 μm has been demonstrated by the teams at STMicroelectronics, CEA-LETI and IMS, which can allow an interconnection density with Cu/SiO_2 hybrid bonding in the order of 10^7 $interconnections/cm^2$. Interconnection pitch reduction below sub-micron is a need for many applications such as image sensors and memory devices and can allow the design of more efficient architectures. In the present work, the goal was to study the lowest achievable hybrid bonding pitch that maintains acceptable electrical performance characteristics and responds well to the device reliability criteria.

To target these objectives, we investigated the following key points: (a) Cu-Cu interface closure mechanism with the reduction of the Cu pad size, (b) electrical behaviour of the hybrid bonding level, (c) failure mechanisms evaluation and (d) new architectures for further pitch reduction and enhanced chip performance.

In the first part of the thesis, we studied a possible change in the Cu interface closure mechanism with the reduction of the Cu pad width at the interface. We considered the hypothesis that Cu interface closure is mainly driven by the thermomechanical behaviour of individual Cu pads during the annealing step. Synchrotron-based in-situ measurements (Laue microdiffraction technique) with temperature were conducted on non-bonded and bonded Cu pad down to 0.32 μm in width. We evidenced that, for Cu pad below 1 μm in width, one dominant grain is expected to be present at the pad level. The hypothesis of Cu pad behaviour as Cu bulk properties is still valid. In this case, the thermomechanical behaviour of each single pad, especially elasto-plastic properties, is driven by its crystalline orientation. The bonding mechanism, based on Cu interface closure by thermal strain deformation, is still applicable for Cu pad width down to 0.32 μm while creep having no major role. The dishing specifications were defined according to the pad having the lowest displacement under annealing, in our case it is the grain of [111] crystalline orientation.

After evaluating the Cu interface closure mechanism, we focused on the electrical study of the hybrid bonding level with the reduction of the pitch. The approach adapted for pitch reduction for the hybrid bonding configuration with a hybrid bonding via (HBV) and hybrid bonding metal pad (HBM) at the interface was based on shrinking the HBM size. The HBV size was fixed. Important consideration here is the electrical chip performance that is mainly driven by the resistance-capacitance (RC) delay induced by the

interconnects. The RC delay was found to increase with pitch reduction down to 0.81 μm, mainly driven by the capacitance increase due to spacing reduction. 0.81 μm is close to the pitch limit since HBV and HBM have then continuous shapes. Further pitch reduction by shrinking only the pad size is not possible and requires shrinking the size of the via and metal lines. Furthermore, an important concern for sub-micron pitch is wafer-to-wafer (W2W) overlay. We evidenced that, with the standard bonding tool accuracy of $\pm$200 nm, a 100 % electrical yield can be achieved with pitch down to 0.81 μm. To qualify the Cu-Cu electrical connections at the interface, we took the contact resistivity at Cu-Cu interface as the main parameter with pitch reduction. **New and innovative methods** were developed for contact resistivity characterization with an accuracy down to 10^{-11} $\Omega.cm^2$, which is at least two orders of magnitude higher in accuracy referring to the state of the art methods. Based on this methodology, we have put in evidence for the first time a dishing range where electrical connections are established at the interface but with an exponential increase of Cu-Cu contact resistivity up 10^{-9} $\Omega.cm^2$. This major finding gives the flexibility to set a dishing threshold according to an acceptable increase in contact resistivity with respect to the total interconnect resistance, which is to be defined to each product and application specifications. Nevertheless, we recommended the 10^{-11} $\Omega.cm^2$ contact resistivity criterion that guarantees an impact on the electrical resistance below 1 % down to 0.81 μm pitch. In this case, the contact resistivity at the interface will be close to the Cu grain boundary one suggesting a perfect Cu-Cu interface reconstruction. With further pitch reduction below 0.81μm, W2W overlay should no longer be seen as a roadblock with the latest developments allowing an overlay accuracy of $\pm$50 nm. Instead, the establishment of Cu-Cu electrical connections at the interface should be the main point of study. The contact resistivity study with dishing is a critical need to achieve a 100 % electrical yield with pitch reduction below 0.81 μm and should be considered for future studies.

The second part of the thesis was dedicated to the study of the failure mechanisms with the reduction of the hybrid bonding pitch. The different studied reliability risks include: (1) the mechanical stability of the interface, (2) the stress induced voiding (SiV), (3) the electromigration (EM) failure mechanism, (4) the Cu diffusion risk at the Cu/SiO_2 hybrid bonding interface and (5) the time dependent dielectric breakdown (TDDB) mechanism. We pointed out that the Cu/SiO_2 hybrid bonding with pitch reduction down to 0.81 μm does not cause any particular risk from a mechanical stability and SiV phenomena and that the Cu/SiO_2 hybrid bonding integration is robust in the sub-micron pitch region. The mechanical stability of the hybrid bonding level is mainly driven by the high bonding energy for the case of Cu/SiO_2 hybrid bonding. Further pitch reduction while keeping the same materials, in this case Cu and SiO_2, should not rise any particular concern.

From an EM point of view, we have put in evidence a change in the EM killer void location from the top or bottom metal lines (pitch $>$ 6 μm) to the HBV level for pitch below 3.5 μm. Even though projections under use conditions are not affected by this change of failure mode for the 1.44 μm pitch, the hybrid bonding level is no longer immune to electromigration. A potential degradation scenario was concluded where void occurs first at the HBM level, more precisely at the Cu/SiO_2 interface, due to the low activation energy in this region. In a second phase, the void at the HBV level nucleates caused by flux divergence due to the presence of the TaN/Ta barrier. Failure by EM occurs at the HBV that is the region with the highest current density. The EM failure mechanism

could potentially become the principal concern in the sub-micron pitch especially if the degradation scenario is similar.

Moving to the risk of Cu diffusion at the Cu/SiO_2 hybrid bonding interface, it originates from a potential misalignment during the bonding step leading that a part of Cu pad will be in direct contact with the SiO_2 dielectric. Any Cu atomic or ionic diffusion could seriously degrade the dielectric degradation properties leading to lower product lifetime. In a previous study by the ST/CEA/IMS teams, a ∼3 nm cuprous oxide (Cu_2O) layer was evidenced in this critical region with the hypothesis that the Cu_2O can act as a barrier to Cu diffusion. We believe that the Cu_2O layer formation originates from Cu oxidation after CMP and before bonding. Our studies from physical-chemical to electrical characterizations showed that (1) the Cu_2O layer is efficient as barrier to Cu atomic diffusion as compared to a 60 nm SiN dielectric barrier layer usually used at the BEoL level interconnects and (2) the 3 nm Cu_2O layer suppress any Cu ionic diffusion in SiO_2 even with pitch reduction down to 0.81 μm and after higher thermal aging conditions. The hypothesis of a Cu_2O as an effective barrier to Cu diffusion was validated that renders the Cu/SiO_2 hybrid bonding configuration reliable from a Cu diffusion point of view. The same behaviour is expected for pitches below 0.81 μm if the Cu_2O barrier remains present.

As for the TDDB failure mechanism, and after developing a **new methodology** for testing, the performance under TDDB was evaluated. Our studies have put in evidence a different acceleration model than the one regularly observed in standard BEoL interconnect. A 1/E dependence between the time-to-failure and the electric field was evidenced in compared to standard $\sqrt{E}$-model for BEoL interconnects having SiN and SiCN as dielectric passivation layers. This was attributed to the negligible impact of Cu diffusion assisting dielectric breakdown due to the presence of the Cu_2O barrier at the Cu/SiO_2 interface. This hypothesis was further assisted by the higher activation energies found our Cu/SiO_2 hybrid bonding integration at the different electric fields as compared to the BEoL dielectrics. The detailed study allowed us to propose a **complete TDDB predictive model** that can be used to project the TDDB performances for given use conditions depending on the targeted application. The same TDDB performance is expected down to 200 nm pitch, assuming the latest developments in W2W overlay (accuracy of ±50 nm). TDDB with spacing lower than 50 nm should be investigated for a possible change in the TDDB degradation model.

In the third part of the thesis, we have investigated **new hybrid bonding architectures** to answer to the problematics of pitch limit and RC delay increase when only shrinking the pad.

Here, a different approach was adapted for pitch shrinkage below 0.81 μm by reducing the spacing between adjacent pads. We found that a 100 % electrical yield behaviour is guaranteed with pitch down to 0.675 μm with the standard bonding tool accuracy (±200 nm) for small structures' surfaces. The robustness of the hybrid bonding level remained intact with the reduced spacing with no impact of potential higher thermomechanical stress at the hybrid bonding level. Adapting this approach for pitch reduction led to increased capacitance due to reduced spacing. Hence, this method allows higher interconnexion density, but it is not the most appropriate from an electrical performance point of view.

New configurations with the aim of hybrid bonding level RC delay reduction were

studied by reducing the hybrid bonding level thickness. These were based on eliminating the HBM level from one or two wafers leading respectively to the HBV on HBM and HBV only configurations. The first configuration, HBV on HBM, allowed a decrease in the RC delay by a factor of 1.4 for the 1.44 μm pitch as compared to the HBV-HBM configuration. The HBV only configuration allowed even more RC reduction by a factor close to 3. The contact resistivity remained below 10^{-11} $\Omega.cm^2$ by respecting the defined dishing threshold even when bonding with 0.32 μm wide Cu pads. By simulations, these new configurations are believed to provide a huge interest to mitigate the RC increase with pitch reduction observed for the HBV-HBM configuration especially in the sub-micron pitch region. This is supported by the good robustness of this design validated after standard qualification tests. The reliability of the HBV only design, especially from an EM point of view, should be studied to confirm that it satisfies the required performances under use conditions.

In this thesis, we have demonstrated hybrid bonding pitch down to 0.675 μm, which can allow 3D stacking with an interconnect density up to 10^8 $interconnects/cm^2$. We have developed new methodologies for TDDB testing and contact resistivity evaluation that are transferable and applicable to any BEoL level. We have proposed design solutions that can be adapted to mitigate any electrical performance concerns with pitch reduction. In addition, we have defined the dishing limits with pitch reduction from a thermomechanical and electrical point of views to guarantee Cu-Cu connections. Based on our findings and considering the latest W2W overlay development with an accuracy of 50 nm, hybrid bonding down to 200 nm pitch (100 nm wide Cu pads) is theoretically achievable. The capability of achieving pitch below 200 nm depends on future W2W overlay development for accuracy below 50 nm, which is not clearly stated for the moment in the roadmaps.

Perspectives

In this thesis, the electrical performance and reliability of the hybrid bonding level was adressed with pitch reduction. The presented studies allowed to identify the key parameters for successful bonding in the sub-micron pitch region as well as to understand the behaviour with respect to the different failure mechanisms. Several important questions remain to be investigated. We can propose the following recommendations for future studies:

Cu-Cu contact resistivity: in chapter 2, we said that it is possible to set the dishing threshold according to an acceptable increase of contact resistivity, between $10^{-11} - 10^{-9}$ $\Omega.cm^2$, with respect to the total interconnect resistance. This criterion is purely based on the electric performance needed depending on the application type. It is important to assess the robustness and the reliability of these structures especially if the contact resistivity is higher than 10^{-10} $\Omega.cm^2$. In fact, structures with contact resistivity above 10^{-10} $\Omega.cm^2$ are expected to have high void density at the interface. The hybrid bonding interface might be in risk especially from the mechanical stability, stress induced voiding and electromigration point of views. It was previously found that voids present at the Cu-Cu interface assists the electromigration degradation mechanism (study by IMEC [153]). Hence, it is important to extend the validity of the different regions of contact resistivity to include the robustness/reliability aspects by performing thermal cycling, high temperature storage and electromigration tests on the sample with contact resistivity $> 10^{-11}$ $\Omega.cm^2$.

Electromigration: based on the change of the EM killer void location with pitch reduction observed for the via+pad (HBV-HBM) configuration, the EM failure could potentially become the main reliability concern for sub-micron hybrid bonding pitch. Therefore, EM tests should be performed on the sub-micron pitch structures embedded in the TEDDY-UFP test vehicle to study the failure mode under EM and if it satisfies the required performances under use conditions. In addition, to understand the change of the EM killer void location observed, it will be possible to conduct thermoelectrical simulations to identify the weakest regions to EM induced failures [227]. EM tests are also of a critical need for the HBV on HBM and the HBV only configurations presented in chapter 4. For these configurations, it is important to study a possible change in the degradation mode depending on the electrons flow direction.

Time dependent dielectric breakdown: TDDB tests should be performed on comb-serpetine structures with Cu pad width down to 0.405 μm to highlight any change in the failure mode. It is also important to extend the validity of the dielectric breakdown study to include structures where the spacing between adjacent pads is below 50 nm that was not included in the present study. The main challenge here is that the testing methodology developed in chapter 3 is not precise for estimation of breakdown voltages when the spacing is below 50 nm. To target this, two adjacent comb-serpentine structures were embedded in the new electrical test vehicle (TEDDY-UFP). One structure should be used for linear ramped voltage sweep measurement to conclude on the breakdown voltage while the second structure could be used for TDDB testing. In this way, a precise TDDB study could be conducted even when the spacing between adjacent pads is below 50 nm

and the study of any change of the failure mode will be possible.

Cu_2O **barrier characteristics:** in chapter 3, we validated experimentally that the Cu_2O layer acts as a barrier to Cu diffusion in SiO_2. To go one step further on the understating of the Cu_2O barrier characteristics, it is possible to apply the density functional theory (DFT) using numerical tools such as Quantum Espresso or VASP [228] [229]. This approach was used in the literature to study the barrier properties of silicon nitride and carbide, with respect to Cu diffusion, as compared to silicon oxide [230]. In our case, it is important to simulate both Cu/SiO_2 (reference) and Cu_2O/SiO_2 interfaces. As a first step, DFT should be used to simulate the activation energy it takes to excite Cu atoms from cubic Cu and Cu atoms from Cu_2O into the SiO_2. This could give a first understanding of the barrier characteristics of Cu_2O before adding the impact of temperature and electric fields in the ab-initio simulations. The main challenge here, beside the heavy simulation times, is the correct modeling of Cu_2O since no information exists on its crystalline or amorphous structure. As a first assumption, it would be possible to simulate the cuprous oxide as a face-centered cubic (FCC) system as reported in the literature [231].

Pitch reduction below 0.81 μm**:** the hybrid bonding pitch limit evidenced in chapter 2 for the via+pad configuration is related to the design rule limitations of the HBV, HBM and metal lines levels that depend on the technological node as well as the thick metal line specifications. To further reduce the pitch, it is possible to switch the hybrid bonding process to thin metal lines levels that have less restricted design rules for the same technological node. It will be pertinent to directly adapt the pad only configuration. One advantage of adapting the thin metal specifications is the reduced stack thickness that can allow better RC performance. However, the main challenge is mostly related to the modified Cu mechanical properties that can impact the Cu-Cu interface closure mechanism. To target this, the thermomechanical behaviour of Cu pads between 100-300 nm in width with thickness below 200 nm, that is a typical thickness of thin metal line level, should be studied. In-situ measurements using the Laue-microdiffraction technique at ESRF like the one presented in chapter 2 should be capable of understanding the behaviour down to 100 nm in grain size.

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Appendix A

Cross Bridge Kelvin Resistor Like Structures

In this appendix is presented the studies done on the cross bridge kelvin resistor (CBKR) like structures that cover the applied electrical current calculation, the sensibility to sensing locations and to Cu pad size reduction.

A.1 Applied electric current calculation

Since we are expecting a very low potential difference when measuring the contact resistance using CBKR, we should understand the specifications of the voltmeter used and the measurements errors. The measurements are calibrated based on the CBKR with an HBM width of 2.16 μm and contact resistivity at the interface of 10^{-11} $\Omega.cm^2$. For this special case, a potential difference of 2.2 μV is expected when applying an electric current of 1 mA. According to the documentation of our multimeter (Agilent 3458A), the maximum resolution for the most precise calibration is 10 nV, which is sufficient for our study. The measurement accuracy is given as a function of reading and range and increases with increased functioning time of the multimeter. Taking the worst case scenario (accuracy after 2 years), we can estimate the measurements errors with applied electric current to detect the potential difference of a 10^{-11} $\Omega.cm^2$ contact resistivity at interface. This is shown in figure A.1.

With increasing current, lower measurements errors are expected that is attributed to higher potential difference. However, Joule heating with increased electric current should be checked for possible impact on the electrical resistance results.

To check Joule heating, experimental electric resistance measurements with an applied current between 0.1 and 35 mA are performed on several daisy chain structures with 100 links to extract the temperature coefficient of resistance (TCR). The measurements are performed at 4 different temperatures of 30, 100, 150 and 195 °C. The TCR value in our case is found to be equal to 0.002±0.0001 /°C. The increase in temperature due to Joule heating can then be estimated using equation A.1:

$$\Delta T = \frac{\Delta R}{R_0} \times \frac{1}{TCR} = B \times I^2 \tag{A.1}$$

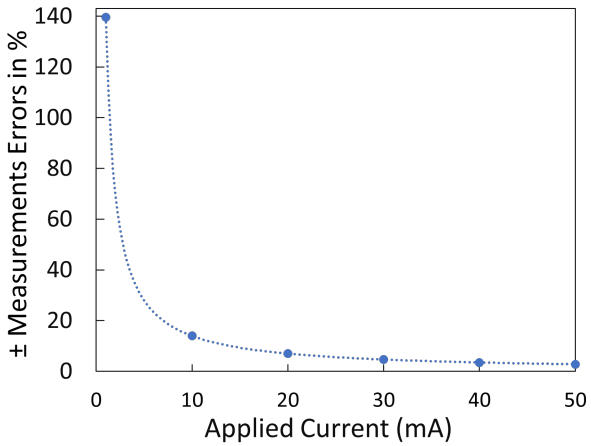


Figure A.1: Calculated measurement errors as a function of the applied electric current corresponding to the potential difference of a contact resistivity at interface of 10^{-11} $\Omega.cm^2$.

where $\frac{\Delta R}{R_0}$ is the resistance shift, I is the current and B is a constant containing thermal conductivity, resistivity, and metal/dielectric dimensions. The temperature increase (ΔT) with increasing applied electric current is shown in figure A.2. The choice of 1 mA as an applied current will have a negligible Joule heating effect but measurements errors above 140 %. The applied current of 10 mA gives the best compromise: Joule heating below 10°C and measurements errors below 10%. Therefore, experimental measurements on the CBKR structures are performed with an applied electric current of 10 mA.

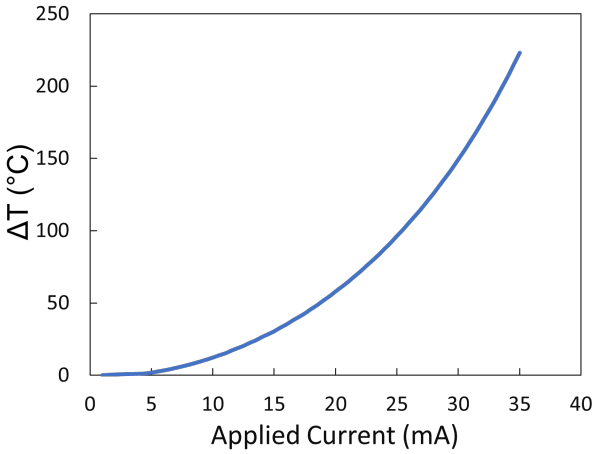


Figure A.2: Results of increase in temperature due to Joule heating as a function of the applied current.

A.2 Sensibility of CBKR to electric potential sensing locations

To study the sensibility of the CBKR structure to the electric potential sensing locations, simulations were done using the CBKR structure with the HBM width of 2.16 μm to predict V^+ and V^- when placed at different locations on the pad surface. We set an imposed contact resistvity of 10^{-10} $\Omega.cm^2$. The theoretical voltage drop expected for this

contact resistivity is 24 μV. As shown in figure A.3, the voltage drop is the closest to the theoretical one when the sensing locations are at the center. This could be understood by plotting the electrical potential streamline, which are mostly stable at the center as compared to the corners. Therefore, the CBKR structures with Cu pad size reduction are designed with the potential sensing locations at the center.

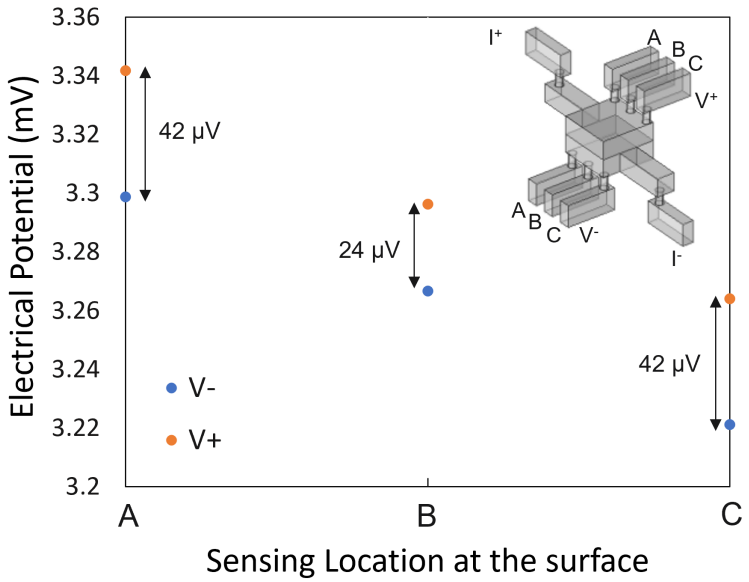


Figure A.3: Electrical potentials V^+ and V^- at different sensing locations where the applied current I is 10 mA for the CBKR structure with HBM width of 2.16 μm

A.3 Sensibility of CBKR with size reduction

The sensibility of the CBKR structures to detect low contact resistivity with the reduction of the HBM width is studied by FEM simulations performed with HBM width from 2.16 to 1 μm. The sensing locations have the positions issued from section A.2 and indicated in figure 2.19. The results are shown in figure A.4. For the CBKR with HBM width of 2.16 and 1.215 μm, the precision limit is around 10^{-10} $\Omega.cm^2$. However, for the 1 μm HBM width, we start observing a deviation around 10^{-9} $\Omega.cm^2$ of imposed contact resistivity at the interface. At 10^{-10} $\Omega.cm^2$, 110% deviation is observed between the calculated contact resistivity by FEM and the imposed one. We can observe a reduction in the precision limit with the HBM size reduction, which will tend toward the state of the art methods [35]. Therefore, CBKR structures for experimental evaluation of contact resistance are only designed with HBM width larger than 1.215 μm.

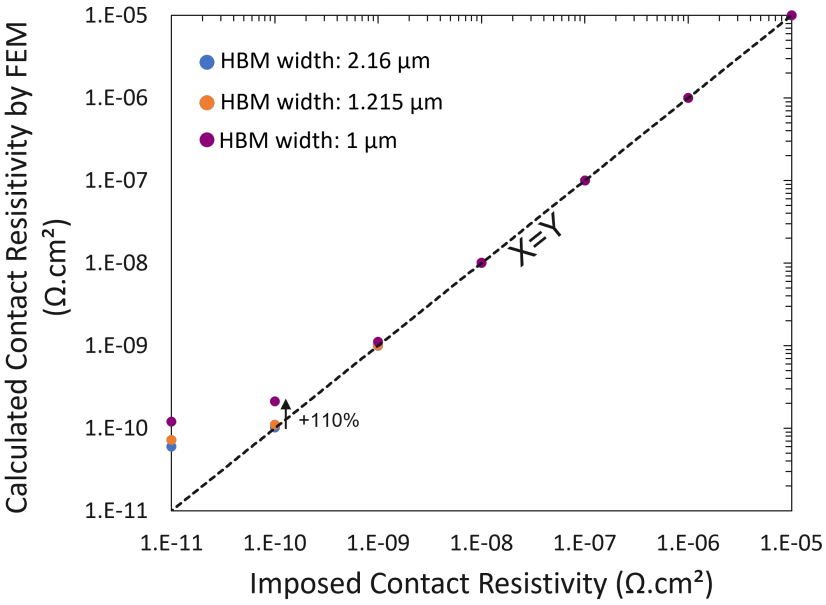


Figure A.4: Correlation between imposed contact resistivity at the interface and the one calculated by FEM for the CBKR structures with HBM width reduction from 2.16 to 1 μm.

Appendix B

Time Dependent Dielectric Breakdown

B. 1 Weibull distributions

The Weibull distributions for all the tested electric fields at the temperature of 195 °C and 170 °C are shown in figure B.1 (a) and (b) respectively. At the temperature of 170 °C, the Weibull slope β is slightly different for the highest electric field of 6 MV/cm, which might be an indication of a different degradation mode than the tested electric fields between 4-2.1 MV/cm.

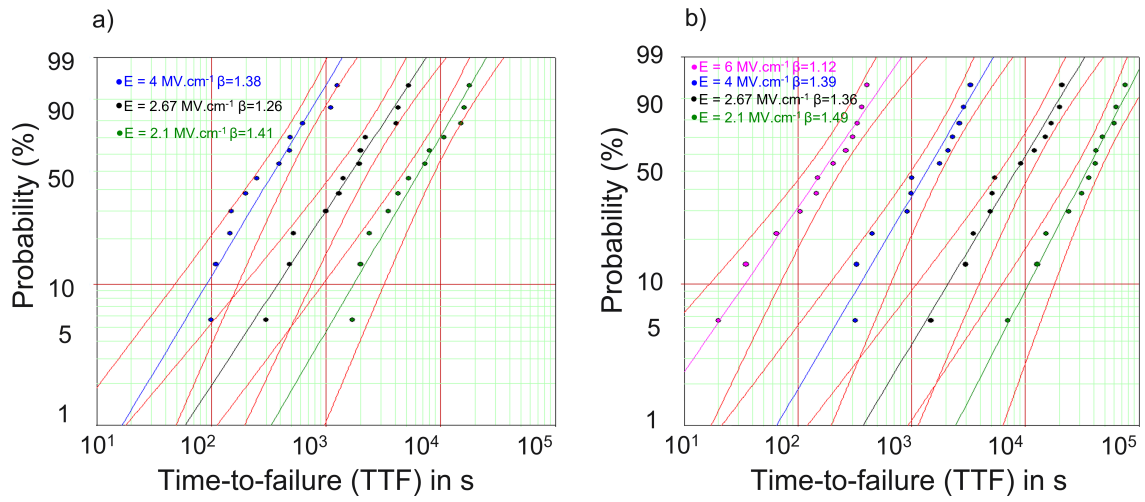


Figure B.1: Weibull distributions for the different tested electric fields on comb-serpentine structures with 720 nm wide HBM on the *S&H* test vehicle for the temperature of a) 195 °C and b) 170 °C.

B. 2 Arrhenius plots

Using equation 3.19, the Arrhenius plots for the different tested electric fields can be extracted as shown in figure B.2. The slope of each curve at each electric field is the respective activation energy. The TTF at 63.2 % and 0.1 % were used for activation energy extraction as shown respectively in figure B.2 (a) and (b), which give similar results.

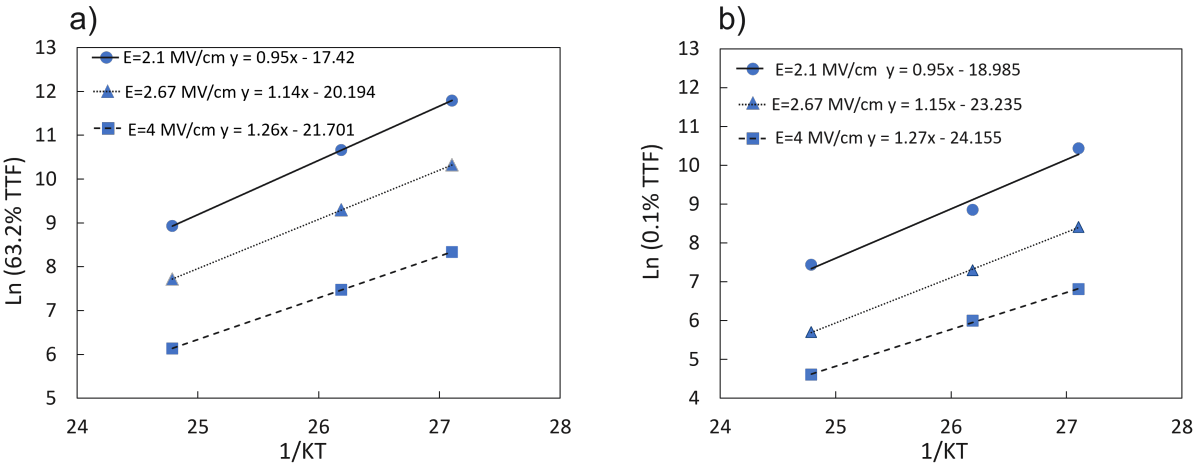


Figure B.2: The Arrhenius plots at different tested electric fields using a) 63.2% TTF and b) 0.1% TTF. The activation energy is the slope of the curve. An $R^2 > 0.97$ is obtained for the different curves.

Appendix C

HBV on HBM Configuration

C.1 Process flow description

The fabrication process of the electrical test vehicle with the HBV on HBM configuration is presented in figure C.1. The process of the bottom wafer is identical to the one showed in the previous chapter. We will focus on the process of the top wafer with the HBV level only. After processing the different metal levels, i.e. 4 for top wafer, two dielectric layers of SiN and SiO_2 are deposited as shown in figure C.1 (b) (1). The hybrid bonding via (HBV) are defined by the lithography step followed by a single damascene etch process (figure C.1 (b) (2)). After etching, the Ta/TaN barrier is deposited followed by Cu seed deposition by PVD. The patterns are filled with Cu by ECD. A specific CMP step adapted to the process of only HBV on the top wader is the done to remove the excess Cu and Ta/TaN layers and to activate the two surfaces to be bonded. Bonding is done between the top wafer with only the HBV level and the bottom wafer with the standard levels at room temperature followed by an annealing step at 380 °C for 2 hours. After bonding annealing, the top Si is thinned down and the back side illuminated (BSI) process is done until the Al pad formation. Electrical measurements can then be performed to characterize the hybrid bonding level.

C.2 Overlay results

Four pairs of wafers are used for the HBV on HBM study on the TEDDY-FP test vehicle (lowest hybrid bonding pitch is 1.44 μm). The W2W overlay boxplots in X and Y directions are shown in figure C.2.

C.3 Finite element modeling description

The 3D models of the HBV-HBM configuration and the HBV on HBM one are detailed in figure C.3 (a) and (b) respectively. The hybrid bonding elements of the bottom wafer are kept constant between the two configurations considering that the HBV-HBM process on TEDDY-FP test vehicle is robust. The smaller HBV shape on the top wafer is considered based on SEM-critical dimensions (CD) measurements. The mean parameters values which are shown correspond to wafer 04 with the HBV on HBM design.

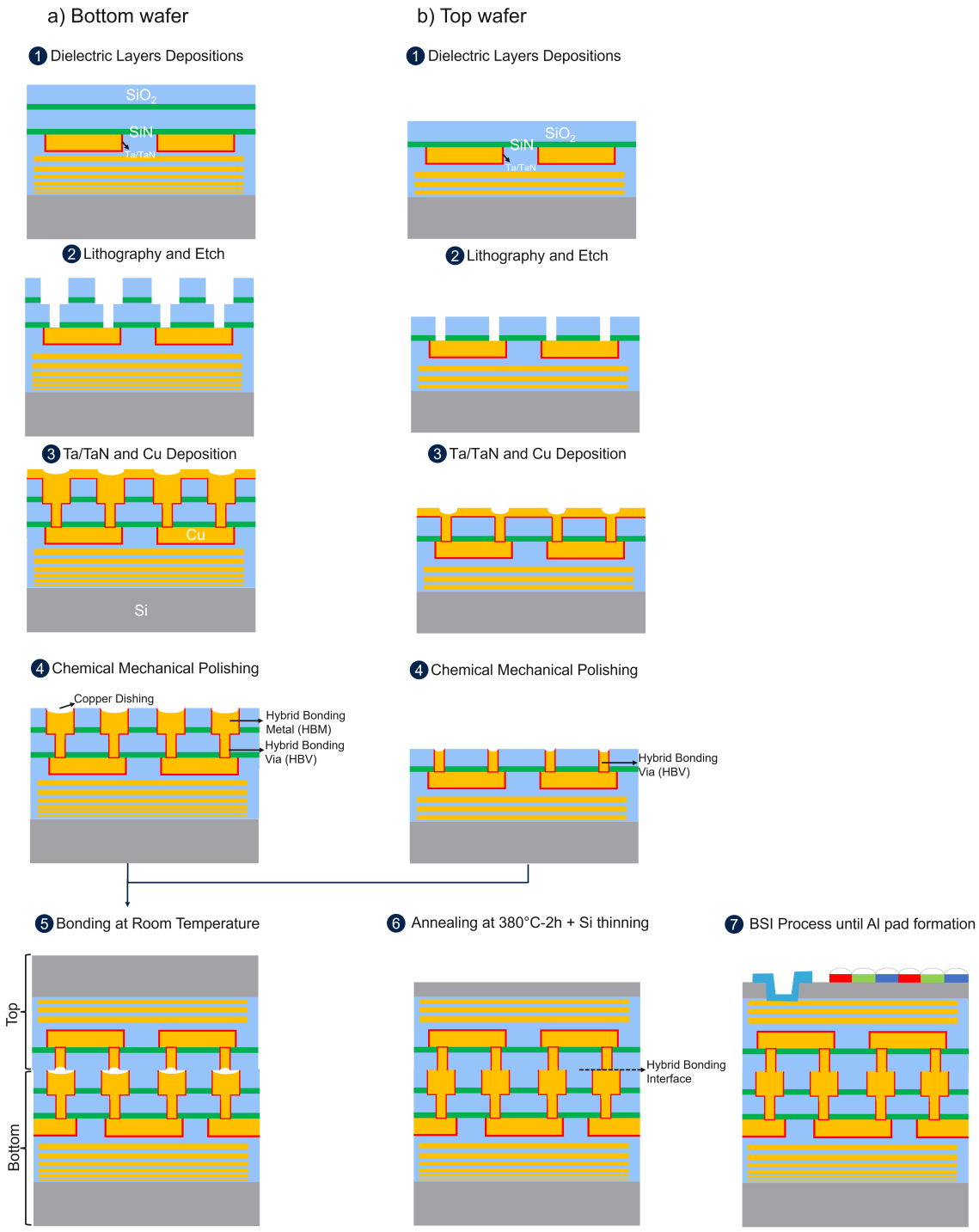


Figure C.1: Process flow description for the electrical test vehicle with the HBV on HBM configuration on the TEDDY-FP test vehicle.

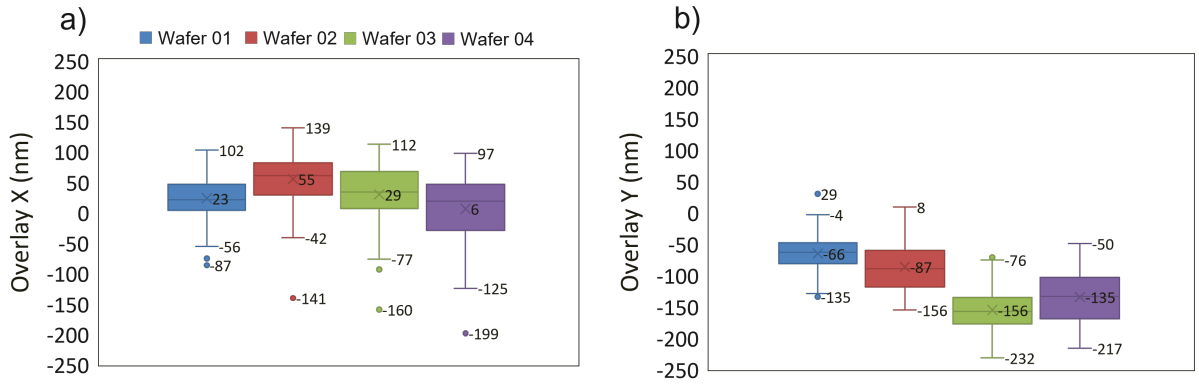
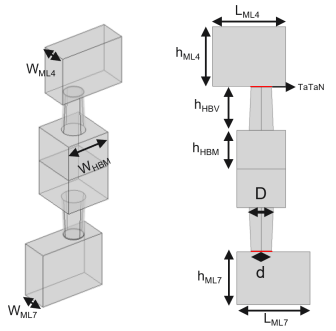


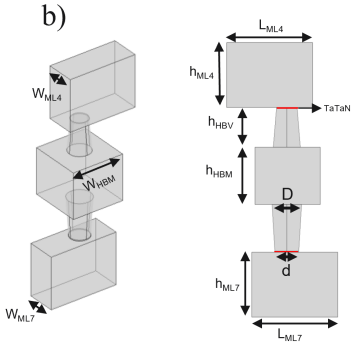
Figure C.2: W2W overlay boxplots in X and Y directions for a set of 4 wafers of TEDDY-FP test vehicle processed with the HBV on HBM design. The mean, minimum and maximum values for each wafer are indicated on the box plots.

a)



Parameter	Dimensions (µm)	
Metal line 4 (ML4)	L_{ML4}= 1.08, h_{ML4} = 0.82, W_{ML4}= 0.45	Top
Barrier TaN/Ta	$t_{TaN/Ta}$ = 0.014	Top
Hybrid Bonding Via (HBV) Top	D = 0.36, d = 0.31, h_{HBV} = 0.6	Top
Hybrid Bonding Metal (HBM)	W_{HBM} = 0.82, h_{HBM} = 0.72	Top
Hybrid Bonding Metal (HBM)	W_{HBM} = 0.82, h_{HBM} = 0.72	Bottom
Hybrid Bonding Via (HBV) Bot	D = 0.365, d = 0.31, h_{HBV} = 0.6	Bottom
Barrier TaN/Ta	$t_{TaN/Ta}$ = 0.014	Bottom
Metal line 7 (ML7)	L_{ML7}= 1.08, h_{ML7} = 0.81, W_{ML7}= 0.45	Bottom

b)



Parameter	Dimensions (µm)	
Metal line 4 (ML4)	L_{ML4}= 1.08, h_{ML4} = 0.82, W_{ML4}= 0.45	Top
Barrier TaN/Ta	$t_{TaN/Ta}$ = 0.014	Top
Hybrid Bonding Via (HBV) Top	D = 0.33, d = 0.26, h_{HBV} = 0.52	Top
Hybrid Bonding Metal (HBM)	W_{HBM} = 0.82, h_{HBM} = 0.72	Bottom
Hybrid Bonding Via (HBV) Bot	D = 0.365, d = 0.31, h_{HBV} = 0.6	Bottom
Barrier TaN/Ta	$t_{TaN/Ta}$ = 0.014	Bottom
Metal line 7 (ML7)	L_{ML7}= 1.08, h_{ML7} = 0.81, W_{ML7}= 0.45	Bottom

Figure C.3: 3D models parameters details taken into the FEM simulations for a) the HBV-HBM configurations and b) the HBV on HBM configuration for wafer 04. The hybrid bonding pitch is 1.44 μm. These dimensions are based on a full map in-line width/critical dimension (CD) and thickness measurements. The mean value is considered in the numerical simulations.

Appendix D

HBV only Configuration

D.1 Process flow description

The fabrication process of the electrical test vehicle with the HBV only configuration is presented hereafter. The different process steps are shown in figure D.1. For this configuration, the process of the bottom and top wafers is identical. After processing the different metal levels, i.e. 4 on top wafer and 7 on bottom wafer, two dielectric layers of SiN and SiO_2 are deposited as shown in figure D.1 (1). The HBV are defined by the lithography step followed by a single damascene etch process (figure D.1 (2)). After etching, the Ta/TaN barrier is deposited followed by Cu seed deposition by PVD. The patterns are filled with Cu by ECD. A specific CMP step adapted to the process of wafer with only HBV level is then done to remove the excess Cu and Ta/TaN layers and to activate the two surfaces to be bonded. Bonding is done at room temperature followed by an annealing step at 380 °C for 2 hours. After bonding annealing, the top Si is thinned down and the BSI process is done until the Al pad formation. Electrical measurements can then be performed to characterize the hybrid bonding level.

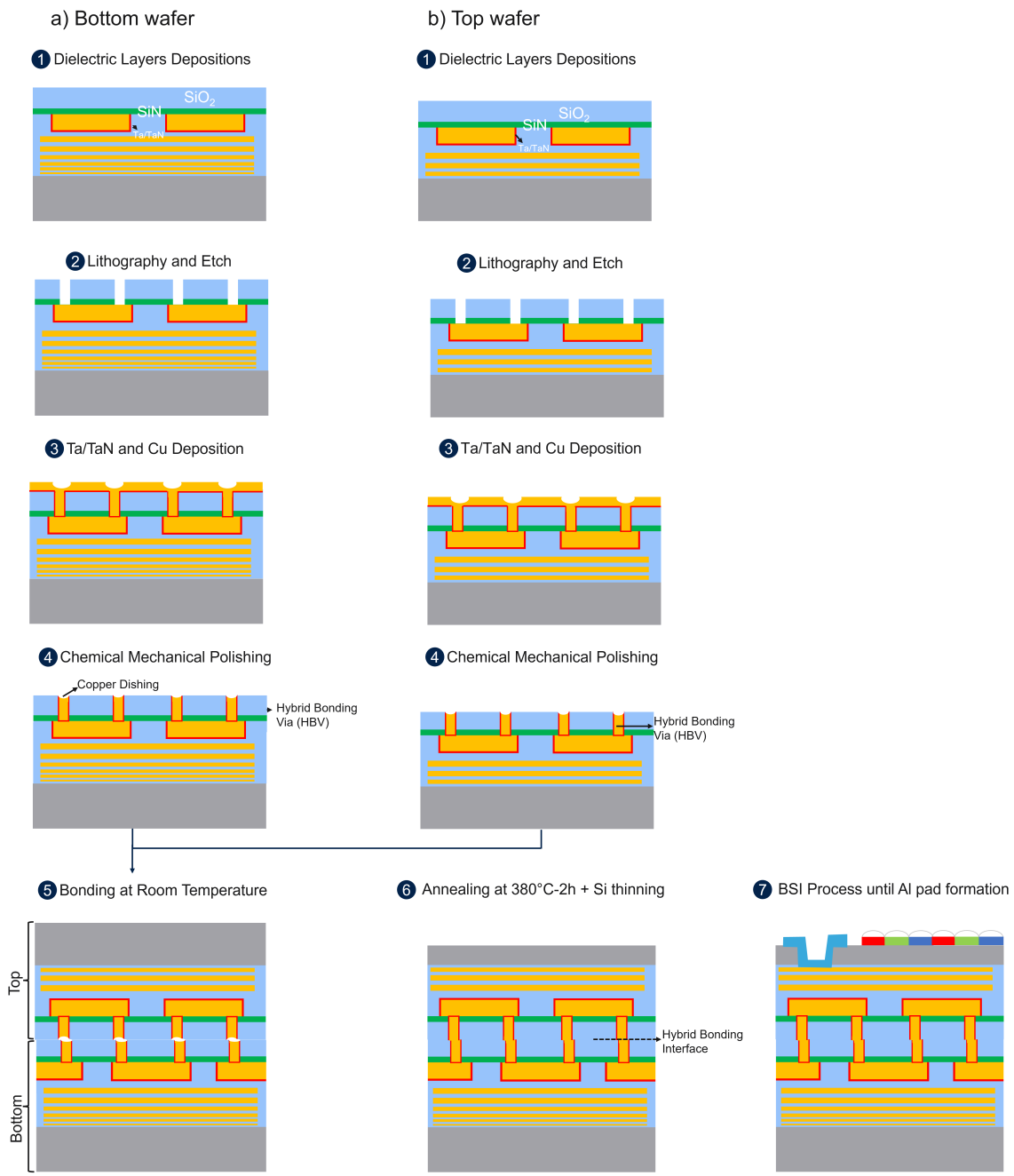


Figure D.1: Process flow description for the electrical test vehicle with the HBV only configuration processed with the TEDDY-FP test vehicle.

D.2 Overlay results

Seven pairs of wafers are used for the HBV only study on the TEDDY-FP test vehicle (lowest hybrid bonding pitch is 1.44 μm). The W2W overlay results in X and Y directions are showed in figure D.2.

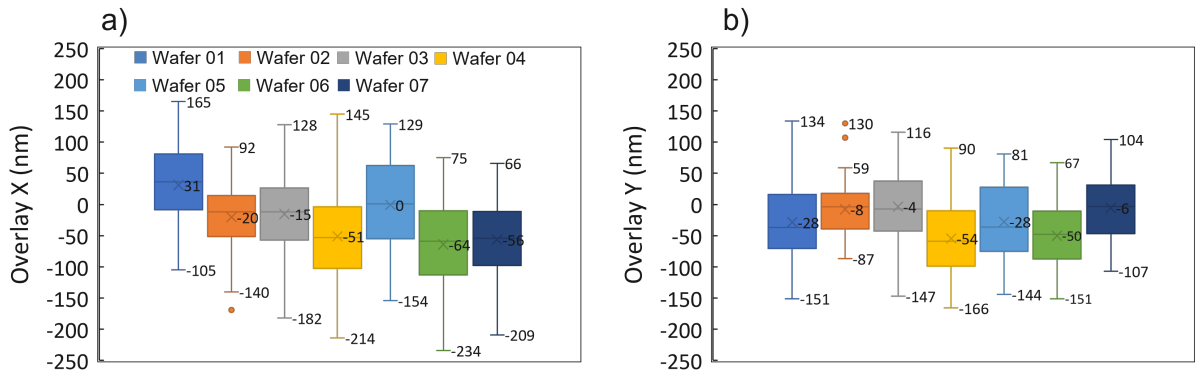
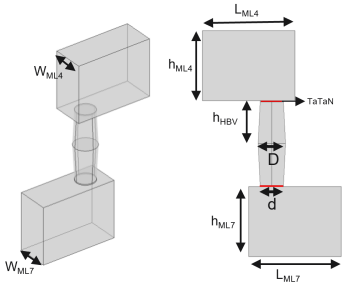


Figure D.2: W2W overlay box plots in X and Y directions for a set of 7 wafers of TEDDY-FP electrical test vehicle processed with the HBV only configuration. The mean, minimum and maximum values for each wafer are indicated on the box plots.

D.3 Finite element modeling description

The 3D model of the HBV only configuration is detailed in figure D.3. The HBV shape and thickness on the top and bottom wafers are based on SEM-CD measurements after the etch step and dielectric thickness measurements after the CMP step. The mean parameters values that are shown in figure D.3 correspond to wafer 07 processed with the HBV only configuration. It should be noted that the mean W2W measurements in X and Y directions are considered when simulating the mean electrical resistance value of each wafer.



Parameter	Dimensions (µm)	
Metal line 4 (ML4)	L_{ML4}= 1.08, h_{ML4} = 0.82, W_{ML4}= 0.45	Top
Barrier TaN/Ta	$t_{TaN/Ta}$ = 0.014	Top
Hybrid Bonding Via (HBV) Top	D = 0.33, d = 0.27, h_{HBV} = 0.5	Top
Hybrid Bonding Via (HBV) Bot	D = 0.325, d = 0.26, h_{HBV} = 0.51	Bottom
Barrier TaN/Ta	$t_{TaN/Ta}$ = 0.014	Bottom
Metal line 7 (ML7)	L_{ML7}= 1.08, h_{ML7} = 0.81, W_{ML7}= 0.45	Bottom

Figure D.3: 3D model parameters details taken into the FEM simulations for the HBV only configuration for wafer 07 with a pitch of 1.44 μm. These dimensions are based on a full map in-line width/critical dimension and thickness measurements. The mean value is considered in the numerical simulations.

Scientific Contributions

Publications in international journals

1. **B. Ayoub**, S. Lhostis, S. Moreau, J.G. Mattei, A. Mukhtarov, H. Frémont, "Investigation into Cu diffusion at the Cu/SiO2 hybrid bonding interface of 3D stacked integrated circuits", Microelectronics Reliability, 2023. doi: 10.1016/j.microrel.2023.114934.

2. **B. Ayoub**, S. Moreau, S. Lhostis, H. Frémont, S. Mermoz, E. Souchier, E. Deloffre, S. Escoubas, T. Cornelius, O. Thomas. "In-situ characterization of thermomechanical behavior of copper nano-interconnect for 3D integration", Microelectronic Engineering, Elsevier, 261, pp.111809, 2022. doi: 10.1016/j.mee.2022.111809

3. S. Moreau, J. Jourdon, S. Lhostis, D. Bouchu, **B. Ayoub**, L. Arnaud, H Frémont "Review: Hybrid Bonding-Based Interconnects: A Status on the Last Robustness and Reliability Achievements", ECS Journal of Solid State Science and Technology 11, 024001, 2022. doi: 10.1149/2162-8777/ac4ffe.

International conferences with proceedings

1. **B. Ayoub**, Lhostis, S., Moreau, S., Perez, E. L., Jourdon, J., Lamontagne, P., ... and Frémont, H. "Impact of Process Variations on the Capacitance and Electrical Resistance down to 1.44 μm Hybrid Bonding Interconnects", 2020 IEEE 22nd Electronics Packaging Technology Conference (EPTC), 2020.

2. **B. Ayoub**, S. Moreau, S. Lhostis, P. Lamontagne, H. Frémont et al. "New Method to Perform TDDB Tests for Hybrid Bonding Interconnects", IEEE International Reliability Physics Symposium (IRPS), 2022, USA.

3. **B. Ayoub**, Lhostis S., Moreau S., Souchier E., Deloffre E., Mermoz S., Gusmão Cacho M. , S. Norah, Rey C, Aybeke E., Gredy V., Lamontagne P., Thomas O., Frémont H. "Sub 1 μm Pitch Achievement for Cu/SiO_2 Hybrid Bonding", 24th Electronics Packaging Technology Conference (EPTC). Singapore December, 2022.

4. S. Moreau, D. Bouchu, J. Jourdon, **B. Ayoub**, S. Lhostis, H. Frémont, P. Lamontagne. "Recent Advances on Electromigration in Cu/SiO2 to Cu/SiO2 Hybrid Bonds for 3D Integrated Circuits", International Reliability Physics Symposium (IRPS), 2023.

5. J.G. Mattei, R. Bon, **B. Ayoub**, S. lhostis, L.R. Clement. "Advanced Electron Energy Loss Spectroscopy investigation of microelectronic devices", 2023 IEEE International Interconnect Technology Conference (IITC). Dresden, 2023.

6. S. Moreau, J. Jourdon, S. Lhostis, D. Bouchu, **B. Ayoub**, L. Arnaud, H. Frémont "Hybrid Bonding-Based Interconnects: A Status on the Last Robustness and Reliability Achievements", 240th ECS Meeting Orlando, USA October, 2021.

International conferences without proceedings

1. **B. Ayoub**, S. Moreau, S. Lhostis, P. Lamontagne, H. Frémont, O. Thomas. "Thermomechanical Behaviour of Copper at Nanoscale by Laue Microdiffraction". European School for Young Scientists on Microscopy and Materials Characterization. Dresden, 2022.

2. S. Lhostis, **B. Ayoub**, S. Moreau, P. Lamontagne, H. Frémont. "New reliability challenges for 3D integration stacking using hybrid bonding". 17th International Conference Reliability and Stress-Related Phenomena in Nanoelectronics. Dresden, 2022.

Patent

1. S. Lhostis, **B. Ayoub**, L. Frey. "New method for the integration of metal/dielectric stacks". Patent ID 83148951. Filled. 2022