Degradation and Lifetime Reliability Models to Assess the Electromagnetic Compatibility Performance of Integrated Circuits Under Environmental Constraints

Md Jaber Al Rashid

▶ **To cite this version:**

Md Jaber Al Rashid. Degradation and Lifetime Reliability Models to Assess the Electromagnetic Compatibility Performance of Integrated Circuits Under Environmental Constraints. Other. Université d'Angers, 2023. English. NNT : 2023ANGE0028 . tel-04470767

HAL Id: tel-04470767

https://theses.hal.science/tel-04470767v1

Submitted on 21 Feb 2024

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

DOCTORAT BRETAGNE SCIENCES LOIRE POUR L'INGENIEUR

université angers

THÈSE DE DOCTORAT DE

L'UNIVERSITÉ D'ANGERS

ÉCOLE DOCTORALE N° 602
Sciences de l'Ingénierie et des Systèmes
Spécialité : *« Électronique, signal, génie industriel »*

Par

« Md Jaber Al Rashid »

Degradation and Lifetime Reliability Models to Assess the EMC Performance of Integrated Circuits Under Environmental Constraints

Thèse présentée et soutenue à Angers, le « November 13, 2023 »
Unité de recherche : Laboratoire LARIS, IETR de Rennes, ESEO Angers
Thèse N° : « si pertinent »

Rapporteurs avant soutenance :

Ghaleb HOBLOS Professeur, ESIGELEC, IRSEEM
Tristan DUBOIS Maître de conférence HDR, Université de Bordeaux

Composition du Jury :

Président :	Bruno Castanier	Professeur, Université d'Angers d'exercice *(à préciser après la soutenance)*
Examinateurs :	Ghaleb HOBLOS	Professeur, ESIGELEC, IRSEEM
	Tristan DUBOIS	Maître de conférence HDR, Université de Bordeaux
	Bruno Castanier	Professeur, Université d'Angers
	Philippe Besnier	Directeur de recherche, CNRS
Dir. de thèse :	Mihaela Barreau	Maître de conférences HDR, Université d'Angers
Co-encadrant de thèse :	Mohsen Koohestani	Enseignant-Chercheur HDR, ESEO, Angers

Invité(s) :

	Richard Perdriau	Enseignant-Chercheur HDR, ESEO, Angers
	Frédéric Lafon	Ingénieur EMC Master Expert, VALEO-GEES, Paris
Co-encadrant. de thèse :	Laurent Saintis	Maître de conférences, Université d'Angers

ACKNOWLEDGEMENT

First and foreost, my sincere appreciation is expressed for the assistance, unwavering affection, support, and prayers that my parents, Harun Or Rashid and Shahnaz Rashid, have bestowed upon me during the course of my PhD studies. They have always believed in me and have been with me despite the distance. My sister and brother are also deserving of my gratitude for their unwavering support, affection, and confidence in me. It is not possible for me to be the person I am today without you all. I dedicate the entirety of my doctoral accomplishment to my family.

My deepest gratitude is extended to my three supervisors—Dr. Mohsen Koohestani from ESEO Engineering School, Dr. Mihaela Barreau, and Dr. Laurent Saintis from the LARIS, Polytech Angers—for their invaluable guidance, encouragement, and support throughout the completion of this dissertation, as well as for generating numerous ideas that formed the basis of this work. I would like to extend my heartfelt appreciation to Dr. Laurent Saintis and Dr. Mohsen Koohestani for their unwavering fortitude, encouragement, and inspiration during the years it took me to complete my PhD. These significant milestones that I have attained throughout my PhD journey are wholly at their disposal. Additionally, I appreciate Dr. Richard Perdriau's assistance and constructive criticism regarding the work I produced while at ESEO.

I would like to express my sincere appreciation to the evaluators of my doctoral dissertation, Dr. Tristan Dubois (University of Bordeaux) and Prof. Ghaleb Hoblos (ESIGELEC), for their meticulous examination of the manuscript and valuable comments and recommendations concerning the research endeavors detailed in the dissertation report. Moreover, I would like to express my gratitude for the insightful feedback and contributions made by two CSI members—Professor Bruno Castanier from the University of Angers—and Dr. Frederic Lafon—during the three years I spent pursuing my doctorate. Their review of the ongoing thesis work significantly enhanced the dissertation's quality. Additionally, I would like to express my gratitude to the remaining members of the doctoral examination committee for attending the defense of my thesis and offering their invaluable counsel and feedback regarding the thesis that was presented.

I express my sincere gratitude to the funding agency, Pays de la Loire Region, An-

gers Metropole, University of Angers, and ESEO Engineering School for granting me the opportunity to participate in this pioneering endeavor that characterizes the long-term evolution of electromagnetic compatibility (EMC) performance degradation at the IC component level in order to model the predictive reliability of integrated circuits. I express my gratitude to the LARIS laboratory affiliated with Polytech Angers and the RF-EMC laboratory featured in the ESEO Engineering School for furnishing me with cutting-edge facilities, including contemporary engineering components and apparatus that facilitated the execution of essential experiments and measurements essential to complete the dissertation.

Finally, I would like to extend my sincere appreciation and pleasure to all my PhD colleagues and closest friends, with a special mention to Mohammed Salim Bidou, Sabrine Dachraoui, and Faitma-Ezahra, whom I met during my doctoral studies at the LARIS laboratory in Polytech Angers. Their unwavering support, inspiration, and the countless pleasant moments we have shared together have been invaluable to me throughout this endeavor. All of these memories would be cherished for the remainder of my life. It was a delight to interact with each of you at multiple social gatherings and excursions. Furthermore, I would like to express my gratitude to my ESEO Engineering School companions, specifically Qazi MashaaI and Mokhtarul, for the invaluable moments we have shared. could remember each of you for the remainder of my existence.

Table of Contents

List of Acronyms

TABLE DES FIGURES

Liste des tableaux

INTRODUCTION

This general introduction highlights a brief overview of the background and motivation for conducting the research on the reliability study that involves developing degradation and lifetime reliability models of analog and digital circuits at the Integrated Circuit (IC) chip level developed by manufacturers, with regards to assessing the Electromagnetic Compatibility (EMC) performance, in particular, the conducted immunity to the electromagnetic (EM) disturbances due to the influence of different specified environmental stress conditions (i.e., thermal and electrical voltage overstress). It is then followed by providing research objectives aligned with the title of the thesis report. Afterwards, the organization of the thesis report is presented, prior to mentioning a list of associated publications, in scientific journals and conferences. Note that all the figures, tables and results provided in this report are produced by the author, unless specified otherwise.

Motivation for EMC and Reliability Study of ICs

Over the past few decades, electronic products have become increasingly pervasive in everyday life. The semiconductor industry simultaneously incorporates more and more circuits onto Printed Circuit Board (PCB)s in an effort to provide more functionality at lower power consumption, higher speed, and smaller dimensions. Not only have their complexities increased, but they are also increasingly exposed to EM contamination sources, particularly as a result of the heavy congestion of ubiquitous wireless systems emitting EM signals across a broad spectrum of frequencies. Therefore, the ability to operate these devices without interfering with one another is of the utmost importance. Particularly, their EM conduction/emission must be regulated, and they must be sufficiently immune to other Electromagnetic Interference (EMI). EM disturbances in Integrated Circuits (ICs) can originate either (1) from the external environment (external immunity issues) : they are generated by other devices and propagate through PCB tracks and harnesses (conducted mode) or as EM waves (radiated mode), or (2) from within the IC itself (internal immunity, auto-immunity issues) : for instance, a million-transistor digital block can generate current spikes flowing through the power supply network, whixh is likely to

disturb an analog, digital or mixed signal block located on the same die. Within a given frequency range, the conducted or radiated emission level of an IC (the "aggressor") can reach and even exceed the susceptibility level of the other (the "victim").

The rapid speed of invention, as well as the industrial EMC trend, support the massive need for downsizing of ICs with ever-increasing functionality. According to the International Technology Roadmap for Semiconductors (ITRS), reduction of the geometric size or dimention of the IC enables the integration of an increasing number of functional logic gates and transistors on an IC, but at the expense of power consumption and peak current. With peak currents of several hundreds of amperes, aPCB and system designer cannot rely solely on 'classical' PCB-level EMI reduction techniques to ensure that their product complies with standard EMC regulations. As a result, IC designers must consider the necessity for EMI suppression at their own level. Such efforts to create a modern IC chip, which governs certain processes in electronic embedded systems, not only make the IC more prone to partial or complete failure in the presence of an EM disturbance, but also make maintaining acceptable EMC characteristics much more difficult that distinguishes competitors in the IC manufacturing industry. The susceptibility to EM disturbances has resulted in growing safety and robustness to EMC specifications concerns, necessitating the development of techniques to reduce undesirable EM susceptibility to EMI. This explains why there are a number of international EMC/EMI guidelines and standards (such as IEC, IEEE, and CISPR) that specify essential requirements not only for military, medical, and automotive applications, but also for commercial products.

Every IC package (including pins) possesses conducted immunity levels, and its failure is susceptible to exposure to either electric or magnetic field. Depending on the IC's internal architecture and pin couplings, EM disturbance can affect the IC's performance to the point where it exceeds the immunity levels to electric and magnetic field (e.g., all ICs are sensitive to both fields with varying frequency responses). Furthermore, as the clock frequency of digital sequential circuit blocks embedded in modern micro-controller IC chips increases, EMI shifts to the thousands of megahertz or gigahertz range, which requires an extension of currently available immunity characterization methods to this frequency band. As a result, determining those EMC values allows engineers to analyze the IC while also knowing its conducted immunity/emission levels.

In addition, when an electronic product is designed for mass production, the functional behavior of each function is tested and validated under environmental conditions to ensure that the product will not malfunction when subjected to particular types of

stress. Typically, thermal conditions, aging, humidity, and vibration are considered when evaluating such objectives. In the EMC domain, PCBs are typically designed for nominal and ambient conditions ; however, the issue arises as to how the EMC performance will evolve as a result of these parameters. This demands not only evaluating the drifts of EMC levels of an electronic circuit throughout its lifespan in a given environment, but also determining sufficient margins to ensure compliance with EMC limits throughout the product's lifetime. Those accelerated aging tests make it possible to evaluate only the EMC degradation variations after aging under specified stress conditions, whereas the long-term EMC prediction under such conditions cannot be estimated without developing an accurate reliability model. The latter permits the prediction of EMC conducted immunity performance throughout the product's lifecycle, which is of great assistance to IC manufacturers in evaluating the trade-off between device performance and fabrication cost prior to manufacturing ICs.

Exposure to various environmental stress conditions can have a severe impact on the conducted immunity profile of an IC level, leading to operational failures with different failure modes (i.e., soft and hard) associated with different failure mechanisms. Those failures occur due to the coupling of EM disturbance signal on the IC pin, causing temporary and/or permanent malfunction due to exceeding the acceptable EMC limit. Aging can have a considerable impact on the degradation of the EMC performance of the analog and digital circuit components in an IC chip. As a result, the appropriate operation of the electrical performance of those ICs is also compromised, reducing the intended lifetime, reliability, and durability of an electronic component or electronic system. Maintaining the desirable long-term EMC robustness of the analog and digital circuit components embedded in an IC chip is therefore essential for ensuring the durability of an electronic component over its lifetime. In order to minimize re-design and production costs, it is necessary, during the design phase of an IC, to ensure its optimum reliability and durability while adhering to the industry standards for long-term EMC qualification. Therefore, it is essential to ensure that the ICs operating in an electronic system generate as few EM disturbances as feasible and exhibit less susceptibility to the EMI caused by other disturbance sources over the course of their entire service life.

The predicted operational lifetime of analog and digital ICs designed and developed by manufacturers for various purposes (e.g., medical, aviation, automotive, and so on) may be several months or years. Accurate assessment of the lifetime reliability of ICs can be difficult, and it is critical to consider how its functionality varies due to changing external

factors such as environmental operating conditions (i.e., thermal, humidity, pressure, vibration, mechanical shock, electrical voltage overstress) over the course of its operational life. Throughout the life cycle of an IC in an EM environment, it is essential to characterize its long-term evolution of the EMC robustness by analyzing the variations of the conducted immunity level in both the transient and frequency domains due to exposure in harsh environmental stress (temperature and/or humidity variations), which may also be incorporated to estimate its lifetime reliability.

This thesis work aims to investigate and evaluate the impact of accelerated ageing on the long-term evolution of the EM robustness of both analog and digital circuits at the IC level. Consequently, the primary goal of the research work is to develop predictive degradation and lifetime reliability models to estimate unknown degradation model and lifetime reliability metrics (i.e., Instantaneous Failure Rate, Acceleration Factor, Mean Time-to-Failure, Probability of Failure) of the tested ICs in nominal as well as other tested or untested accelerated environmental stress conditions, while considering that the IC is robust and maintains the EMC compliance level within the whole lifetime of the equipment in an electronic system which they belong to. Eventually, those developed models should be validated and to become the part of the EMC performance evolution data that should be supplied by the IC manufacturers, in order to facilitate the design of functional and durable electronic products.

Objectives of the Thesis

The manuscript aims to propose and develop degradation and reliability models for the industry representative manufactured analog and digital IC samples by assessing the long-term evolution of the EMC conducted immunity performance under the influence environmental constraints. Those developed models enabled to predict the unknown degradation and lifetime reliability parameters, depending on characterizing the conducted immunity measurements performed in accordance to the designed Accelerated Degradation Test (ADT) plan. In addition, those developed models would enable to predict the reliability parameters in nominal as well as tested or untested different environmental stress conditions, while estimating the conducted immunity performance by developing the Integrated Circuit Immunity Modeling-Conducted Immunity (ICIM-CI) models of the tested Device Under Test (DUT) samples. The objectives of the research work presented in this report can be summarized as follows :

1. Conduct a comprehensive state-of-the-art review on developing the ICIM-CI models of various analog circuits, and compare the simulation model results with the conducted immunity performance measurement results obtained by performing various EMC tests (i.e., EFT and DPI).
2. Investigate and analyze the evolution of the EM robustness of analog ICs under the influence of multiple ageing stress conditions (i.e., thermal and electric overstress voltage).
3. Develop and couple accelerated degradation test model to predict the lifetime reliability parameters based on the functional performance of the designed low voltage dropout analog circuit with adjustable output in 180 nm CMOS technology.
4. Conduct a comparative study to evaluate the conducted immunity of functionally identical analog ICs by integrating different obsolescence and the impact of different thermal stress conditions.
5. Investigate the influence of applying thermal step-stress ADTs combined with constant electrical overstress conditions on the developed ICIM-CI models of the studied analog ICs.
6. Develop degradation and accelerated life test reliability models to predict the desired parameters based on the variation of the long-term EM robustness of both analog and digital circuits, depending on the defined multiple external stress conditions applied while performing different types of ADTs.

Thesis Organization

According to the general concepts on the need to conduct the research study on the reliability modeling of ICs based on the Electromagnetic Robustness (EMR) under the influence of external environmental stress conditions, the thesis report is organized in five chapters, excluding the present and the main conclusion and perspective chapter of the thesis report.

Chapter 1 provides an overview of the existing literature available on how to propose and develop different kinds of EMC simulation models (i.e. ICIM-CI, ICIM-CPI, ICIM-CE, ICEM-CE and so on) to compare with that of the measured conducted immunity and emission of various analog and digital circuits, in accordance to the current international electrotechnical commission (IEC) standards (i.e., IEC 62433-4 and IEC 62433-2).

Furthermore, the effect of continuous aging on the evolution of the EMC performance of various analog and digital circuits (e.g. operational amplifier and oscillator) is explored. Furthermore, the DPI and EFT experimental techniques required for performing and characterizing the conducted immunity of ICs in the time and frequency domains are discussed, followed by providing an overview of the basic terminologies, concepts, and general principles focusing on the IC-EMC reliability study.

Chapter 2 presents a case study of an analog Complementary Metal-Oxide-Semiconductor (CMOS) voltage regulator circuit designed in 180 nm analog-mixed signal (AMS) bulk technology with the goal of proposing and developing the degradation model based on the functional performance degradation data of the developed electrical simulation model, subjected to multiple accelerated temperature and electrical overstress conditions. Furthermore, an Accelerated Life Test (ALT) was proposed and developed with the help of the Maximum Likelihood Estimation (MLE) method for predicting model constant parameters and required reliability characteristics under the effect of applied accelerated stress conditions.

Chapter 3 investigates the conducted immunity of identical pin-compatible analog ICs developed by different manufacturers under the influence of the specified different temperature stress conditions, while integrating the obsolescence or the second-source in life-long systems. Moreover, the impact of applying extreme high and low thermal environmental stress on the developed Passive Distribution Network (PDN) and Immunity behavioral (IB) blocks of the developed ICIM-CI models of the studied analog ICs is also compared and analyzed.

Chapter 4 highlights the influence of ageing on the currently available ICIM-CI models to predict the EMC performance at the IC level. The influence of performing ADT on the observed conducted immunity drifts of different analog tested ICs with similar functionality is explored and analyzed. The ICIM-CI models, with and without considering the accelerated ageing impact, are developed and compared by analyzing the effect on both the developed PDN and IB models of the fresh and aged IC samples. This study emphasize on the importance of including versions of those available EMC model standards.

Chapter 5 investigates the effect of applying multiple accelerated stress factors (i.e. thermal and electrical voltage), while performing the thermal step-stress ADTs on the evolutions of the long-term EMR of the tested analog ICs and constant stress ADTs on the digital circuit embedded within the Attiny85 micro-controller IC chip samples, followed by developing and constructing the suitable EMC performance degradation models and

the ALT reliability models to predict the necessary model parameters.

Publications

The conducted research study presented in this thesis has resulted in the following peer-reviewed journal articles and conference proceedings. Figures and Tables illustrate the results of those publications, which have been referenced and cited within the chapters to demonstrate the originality of the author's own work. The list of peer-reviewed journal articles and conference proceedings are mentioned as follows :

1. **Jaber Al Rashid**, Mohsen Koohsestani, Laurent Saintis, and Mihaela Barreau. Lifetime reliability modeling of digital ICs influenced by the environmental and aging constraints : A case study. *IEEE Transactions on Device and Materials Reliability*, 2023, (under review).
2. **Jaber Al Rashid**, Mohsen Koohsestani, Laurent Saintis, and Mihaela Barreau. Degradation and reliability modeling of EM robustness of voltage regulators based on ADT : An approach and a case study. *IEEE Transactions on Device and Materials Reliability*, 2023 (major revision).
3. **Jaber Al Rashid**, Mohsen Koohsestani, Richard Perdriau, Laurent Saintis, and Mihaela Barreau. Combining obsolescence and temperature stress to evaluate the immunity of voltage regulators to direct power injection in long lifespan systems. *IEEE Letters on EM Compatibility Practice and Applications*, 5(1) : 27-32, 2023, doi : 10.1109/LEMCPA.2023.3240621.
4. **Jaber Al Rashid**, Mohsen Koohsestani, Laurent Saintis, and Mihaela Barreau. High temperature accelerated ageing influence on the conducted immunity modelling of the commonly used voltage regulator ICs. *In 2023 International Symposium on EM Compatibility (EMC Europe)*, pages 1–6, Krakow, Poland, 2023. IEEE Xplore (paper id 119).
5. **Jaber Al Rashid**, Laurent Saintis, Mohsen Koohsestani, and Mihaela Barreau. Coupling simulation and accelerated degradation model for reliability estimation : Application to a voltage regulator. *Microelectronics Reliability*, 138 :114682, 2022, doi : 10.1016/j.microrel.2022.114682.
6. **Jaber Al Rashid**, Mohsen Koohsestani, Laurent Saintis, and Mihaela Barreau. A state-of-the-art review on IC-EMC reliability. *In Proceedings of the 31st European*

Safety and Reliability Conference, pages 1850–1857, Angers, France, 2021. Research Publishing Services, doi : 10.3850/978-981-18-2016-8-154-cd.

Chapitre 1

A State-Of-The-Art on IC-EMC Reliability : Methodology, Modeling and aging Impact on the EMC of ICs

EMC is the ability of an IC to function satisfactorily in its EM environment without introducing intolerable EM disturbance to anything operating in that environment. In order to guarantee the functional safety of electronic applications and the simultaneous operation of all nearby electronic devices or other ICs in a given EM environment, the EMC performance operating in an EM system should be within the desired level. Different EMC standards (such as, IEC 61963 and IEC 62132) for ICs are now available for a variety of applications, including automotive, avionics transport, medical, and telecommunications.

Although the size and dimension issue of an IC is usually considered, the EMC issues are not considered by IC designers during the design stage because it was only addressed at the system and PCB levels. ICs are the sources of noise emission and sensitivity, so they are the source of several EMC constraints and issues related to the conducted immunity or susceptibility to external EM disturbance signals. Due to the ongoing development of CMOS technology trends related to an increase in clock speed, an increase in IC design complexity, and a decrease in the size of the transistors within ICs operating in nanoscale electronic circuits or devices, ICs are becoming more sensitive to noise [1]. Furthermore, the integration of Deep Sub-Micron (DSM) circuits in EM environments under harsh external environmental conditions implies evolution of functional electrical characteristics and/or performances of the ICs as well as continuation of the internal physical degradation or failure mechanisms, which affects the functional safety of the EM devices [2]. Considering the EMC issues of ICs and their evolution in critical environments, the

study of IC-EMC, along with the lifetime reliability of ICs, is essential to characterize the long-term evolution of the EM robustness at different external operating conditions (e.g., temperature, humidity, electrical voltage and vibration) [3].

In this first chapter, the objective is to conduct a comprehensive review of literature works and their research findings on developing accurate immunity and emission models of ICs, with a particular emphasis on quantitative evaluation of experimental characterization based on various IC-EMC measurement methods under various ALTs. The subsequent sections of this chapter presents a few recent researches on the methodology to develop, extract and validate various types of the EMC models, such as ICIM-CI, Integrated Circuit Immunity Modeling- Conducted Pulse Immunity (ICIM-CPI) and Integrated Circuit Emission Modeling-Conducted Emission (ICEM-CE) based on the IEC modeling standards, proposed for predicting and analyzing the EMC performance of various types of analog and digital circuits designed within a test chip. Those developed models were simulated and compared with the DPI conducted immunity measurements performed on different pins of the tested IC samples. In addition, literature studies on investigating the evolution of the EMR of ICs have been discussed ; these existing research studies provide an overview of how applying various types of stress factors (i.e., thermal and electrical overstress) with specified magnitude and stress duration could influence the conducted EMC performance of ICs. In addition, an overview of the general principle on reliability study of electronic components at the IC level is presented to highlight the need to incorporate and integrate the environmental impact on the EMC performance for developing the degradation and reliability model. Those modes would allow to predict various reliability matrices taking into account of the conducted immunity EMC performance evolution of the tested ICs subjected to the aging caused by extreme stress conditions.

1.1 EMC of ICs : Conducted Immunity Measurement and Analysis

The conducted immunity level of ICs should be within the desirable range for maintaining the functional safety and reliability of electronic systems in various complex applications such as automotive and aeronautic. Throughout the operational lifetime of ICs, harsh environmental conditions, such as, extreme high or low temperature, humidity, shock, and stress tend to cause intrinsic physical degradation, resulting in significant variations in the lifelong EMC performance of IC device [4], [5]. Therefore, predicting the

lifetime reliability under the external environmental stress conditions and maintaining their long-term EMR, while operating within a system in any application is a critical issue that needs to be addressed.

According to IS0 11451, "EMC" is "the ability of a device, equipment or system to function satisfactorily in its EM environment, without introducing EM disturbances that could interfere with the proper operation of the devices or systems located in its environment" [6]. Since EMC difficulties emerge in an EM environment (EM) from three elements, the source or aggressor, the victim, and the coupling mechanism [7]. The term "source" refers to the source of the EM energy that creates the disturbances, whether natural (i.e., lightning or man-made (for example, electrostatic discharge). The term "victim" refers to an IC or electronic equipment that receives the EM disturbance from the aggressor and has its electrical properties impaired as a result of EM interference operating on the electronic component. The term "coupling path" refers to the manner of coupling (cable, parasitic inductance, power rails, ground, parasitic capacitance, traces on a printed circuit board (PCB), and antenna) that causes harmonic disturbances to be transmitted from the source to the victim.

Characterizing and determining complex EM immunity and emission issues of ICs under complex EM environment is essential for accurate evaluation of EMC and reliability of ICs. The IC-EMC lifetime reliability metric refers to the function that can be expressed in terms of parameters to indicate or predict how long the system would be performing before exhibiting various EMC failures under different external operational conditions [8]. Adopting realistic and accurate model construction with precise model validation to predict EM immunity and emission performance of ICs have attained significant importance to IC designers and manufacturers. Evaluation of predictive EMC simulation results would be necessary to IC chip designers and manufacturers for reduction of time, number of prototype cycles and fabrication cost prior to manufacturing various kinds of ICs [8].

Simulating immunity and emission models can help IC designers to understand and anticipate EMC levels to conducted harmonic disturbance when applied to IC pins, which in turn enable IC manufacturers to provide conclusive statement on whether IC would be EMC compliant prior to manufacturing. Moreover, EMC model construction and obtaining EMC results by simulations in various CAD software are considered very useful and easy to analyze compared to that of performing various EMC performance characterization tests in accordance to the existing IEC standards (IEC 62132-4, IEC 61967-4). Developing and constructing the conducted immunity and emission models to predict the

EMC performance of ICs at the device or component level would enable the determination of different induced failure mechanisms and their origin caused by injecting conducted EFT pulses into different IC pins as well as by coupling high frequency RF signals to induce noise by causing EMI onto different analog and digital input and/or output as well as power supply pins of the IC chip.

1.1.1 Transient EM conducted immunity measurement of ICs

Several studies have been conducted to characterize the immunity profile of various analog and circuits embedded in an IC chip based on the IEC standard tests (i.e., EFT, DPI).

In accordance with the IEC 61000-4-4 standard [9]-[10], the EFT/Burst testing method is commonly used to evaluate the EM conducted immunity of ICs to the transient-conducted interference. The generator generates an EFT signal consisting of a sequence of bursts in transient mode that may be injected directly to either functional or power supply pins of ICs via magnetic or electric coupling. Hence, EMI causes temporary malfunction or even permanent damage to the integrated circuit [11]. EFT generator can generate interference pulses with high repetitive frequency (MHz), amplitude (U), short rising time (t_r), pulse duration (t_d) and pulse width (t_w). The characteristics of the waveform of a single Langer probe that emits EFT injection pulse that complies with the IEC standard 61000-4-4 is presented the Figure 1.1 [11], which was injected into different IC pins (i.e., I/O, V_{dd} and GND) using the voltage injection probe (P200). The injection probe was connected to the EFT generator, which could generate the EFT pulse with t_r, t_d, EFT burst or pulse frequency and burst duration of 1.5 ns, 5 ns, 10 kHz and 6.5535 s, respectively. Moreover, the standardized waveform of the EFT pulse has an exponential shape with rapid rising and falling slope.

Table 1.1 shows the various parameters of the EFT pulse, whose magnitude can be varied within a certain range and conforms to the IEC 6100-4-4 standard [12]. With the voltage probe (P301), this EFT burst of pulses can be injected into different IC pins, triggering various forms of failure (i.e. soft and hard failure).

The EFT testing method is a destructive method due to injecting the EFT voltage above a certain voltage limit to different pins of the IC under test, which can affect its functionality in terms of current or voltage fluctuations. The block diagram for the EFT test setup used to evaluate the immunity of the several I/O pins, power supply (VDD) and ground (VSS) pins in the time-domain or transient mode is shown in the Figure 1.2

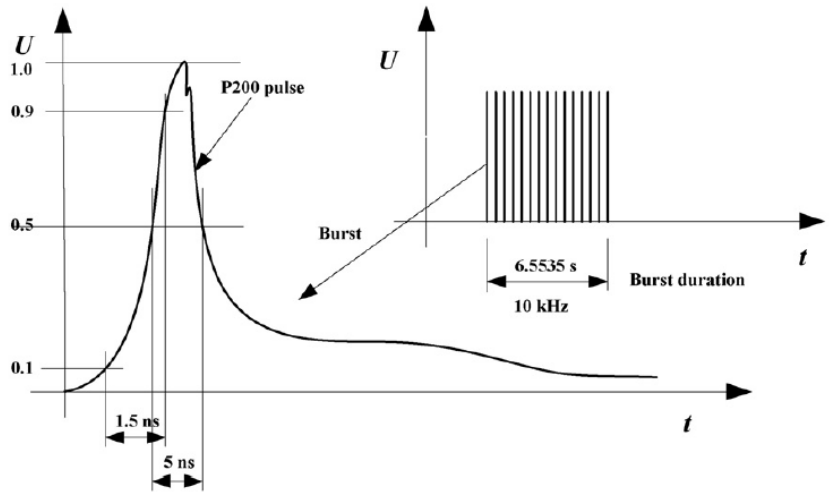


FIGURE 1.1 – EFT pulse waveform injected into the IC pins using the P200 probe [11].

TABLE 1.1 – Parameters of the burst for the EFT test [12].

Set voltage	**Output voltage peak values and repetition frequencies**		
	U_S *(open circuit)*	U_S *(50Ω)*	***Repetition frequency***
kV	kV	kV	kHz
0.25	0.25	0.125	5 or 100
0.5	0.5	0.25	5 or 100
1	1	0.5	5 or 100
2	2	1	5 or 100
4	*4*	*2*	*5 or 100*
Wave shape into a 50 Ω load:			
rise time t_r	(5± 1.5) ns		
pulse width t_w	(50 ± 15) ns		
peak voltage	U_S ± 2 %		

[13]. The EFT test bench was consisted of the EFT source integrated with the control software for generating the EFT signal with fixed parameters, the DUT mounted on the EMC test board, DC power supply, ground plane, injection probe (P250) for injecting the EFT pulse into the IC pins and the oscilloscope for the EFT source to monitor the EFT measurement results.

In [14], researchers injected the EFT pulse into the VDD, GND and several I/0 pins

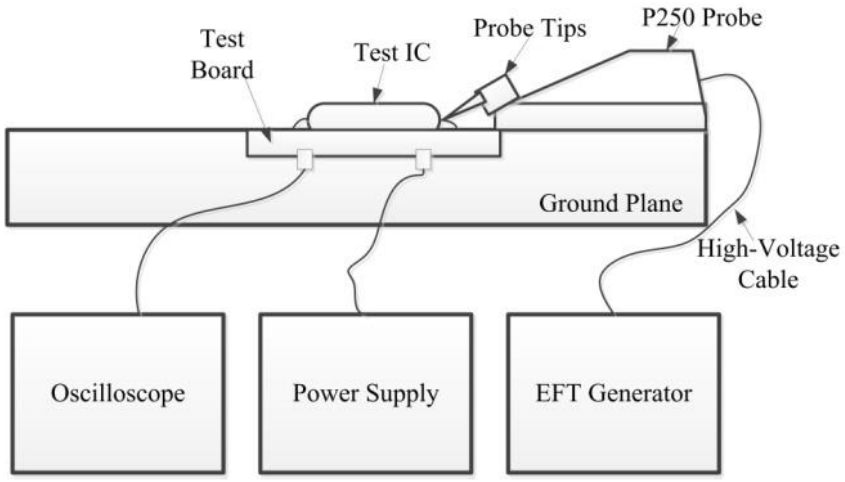


FIGURE 1.2 – EFT pulse waveform injected into the IC pins using the P200 probe [13]

TABLE 1.2 – Classification of different failure modes observed during the EFT test [11], [14].

States	Description
No failure (A)	DUT performs as designed during and after EFT injection
Self-recovering (B)	DUT doesn't perform as designed during exposure, but can return to normal operation after EFT-Burst is removed
Soft failure (C)	DUT doesn't perform as designed during exposure. DUT doesn't return to normal until exposure is removed and reset pin is asserted
Repower-recovering (D)	DUT doesn't perform as designed during exposure. DUT doesn't return to normal until exposure is removed and power to DUT is cycled
Damaged (E)	DUT can't return to normal due to physical damage or other permanent performance degradation

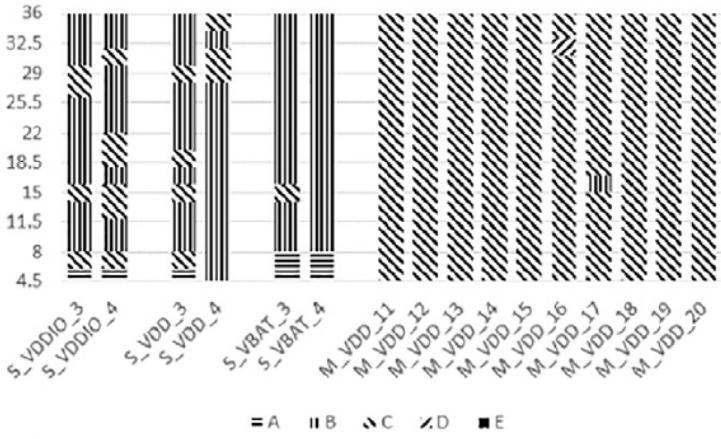
of the DUT in order to investigate the immunity of different pins of the DUT. Different types of failure modes or error states (A, B, C, D and E) were identified due to the injection of the EFT voltage on these pins under test (PUT). The immunity criterion to the EFT disturbance was detected and evaluated by observing these different kinds of failure modes on the tested IC pins. Table 1.2 shows four failure modes identified during the EFT immunity test conducted on the IC DUT [11], [14]. These observed failure modes can be categorized into three different types of failure mechanisms (e.g. soft failure, power recycling and self-recovering failure). Soft-failure (C) could be observed when the normal operation of the micro-controller IC under test would be interrupted due to the injection

of the EFT pulse on its pins and the DUT would only resume its normal functionality due to the removal of the EFT pulse and upon the activation of reset pin. This failure mechanism would be observed due to the wrong switching of the logic gates resulting in an unexpected storage of data in the flash memory or register [11], [14].

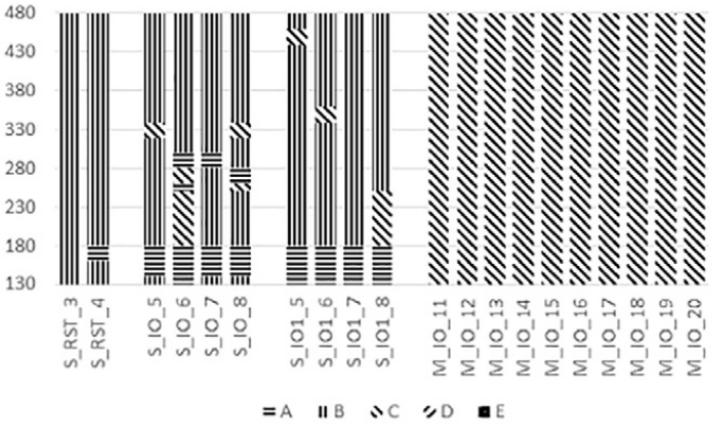
Power recycling failure is caused by the error state D as shown in the Table 1.2 due to the latch-up of the CMOS devices within the DUT, which can be detected by observing a large spike of the current or EFT voltage injected on the PUT. This phenomenon would occur due to the switching of the internal transistors (i.e., NPN and PNP) into the on-state above a certain EFT voltage injection on the PUT, generating a significantly large current to flow through the low resistance conducting path developed between the VDD and the VSS pin of the DUT [13]. Self recovering failure mode or error state B would occur when the microcontroller is disturbed due to different failure mechanisms, such as, power-on reset (POR), watchdog reset (WDOG), external pin reset (PIN), loss of clock (LOC), and low-voltage detect (LVD). If the VDD voltage would be lower than the reset voltage of the DUT, then the POR is triggered. LVD would be activated for protecting the data stored in the register of the microcontroller DUT, when the VDD is reduced below the lowest permitted detected voltage (LVDL). In order to prevent this failure mechanism, the DUT might be equipped with the low voltage prevention circuit, which would ensure the IC to remain in the reset state until its VDD would become greater than the VLDL after the EFT pulse is removed [11].

In [14], the EFT test conducted to evaluate the conducted immunity of the the VDD and I/O pins of two different micro-controllers. The IC with 8051 architecture was denoted by 'S', and the other IC was labelled as 'M' due to having the ARM architecture. Different error states (i.e. A, B, C and D) or permanent malfunction induced by the EFT pulse were considered as the immunity criterion for assessing the conducted immunity of the tested ICs to the transient disturbance. The EFT voltage injected to the power and IO pins on the two DUTs is shown in the Figure 1.3, and different error states were observed on the pins under tests (PUTs), depending on the magnitude of the injected EFT voltage prior to causing the tested ICs to malfunction permanently. Due to the injection of the positive polarity EFT voltage on the power pins of the DUTs, the Figure 1.3a showed that the immunity of the IC chip (i.e., 'M') was less compared to the other IC as the error state C was observed due to injection of higher EFT voltage on its VDD pins. However, the 'S' chip showed error state A upto low EFT voltage, followed by observing the mode B failure due to injecting high EFT voltage on its VDD pins. Similarly, the Figure 1.3b

illustrates that the IO pins of the 'S' chip was more immune to the EFT disturbances compared to the other tested IC. The IO pins of the 'S' could withstand higher EFT voltage injection than that of the 'M'. Besides, the 'M' chip showed higher degree of failure modes (i.e., state C), while the 'S' chip could only demonstrated failure mode B [14]. While comparing the EFT results depicted in the Figures 1.3a and 1.3b, it was found that the IO pins required higher EFT voltage (indicated in the y-axis) injection than those VDD pins for observing different failure modes, and causing permanent degradation of the IC functionality induced by the EFT disturbance.



(a)



(b)

FIGURE 1.3 – EFT voltage injection on DUTs with different error states observed (a) VDD ; (b) IO pins [14].

1.1.2 Conducted immunity measurement of ICs in frequency domain

The DPI conducted immunity testing method is regarded as one of the most effective techniques for characterizing the conducted immunity of ICs in the presence of radio frequency (RF) continuous-wave single-tone EM disturbances. The RF signal at a specific frequency (f) with conducted forward power is injected into various IC pins via the cable harness or PCB traces to ensure an efficient coupling mechanism during the conduction mode propagation of the RF signal power [15]. The DPI immunity test can be conducted in accordance to the IEC 62132-4 standard [16]. The DPI test-bench setup consists of the different electrical components to characterize the effect of inducing the conducted EM disturbance on the functionality of an IC sample under test. In general, the DPI test bench is composed of radio-frequency (RF) signal generator, RF power amplifier, bi-directional coupler, decoupling network, power meters, oscilloscope and a control computer to monitor the relevant output data [2].

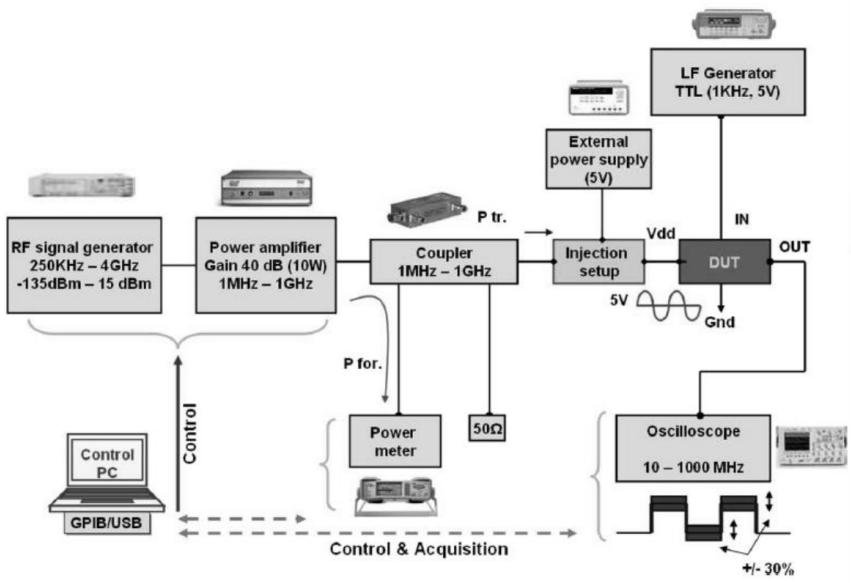


FIGURE 1.4 – DPI test setup for characterizing the conducted immunity of an IC under test [17].

In [17], the DPI test setup used for characterizing the conducted immunity of an inverter circuit between the DPI frequency range between 1 MHz and 1 GHz is shown in Figure 1.4. The injection setup refers to the decoupling network, which consist of a 47 pF

coupling capacitor or the bias tee connected in series. The RF signal generator is used as an interference source to send continuous-wave harmonic disturbance signal at a specific signal power, which is then amplified by the RF amplifier. The use of the wideband bias tee is crucial for allowing the continuous sinusoidal RF signal generated by the RF signal generator to superimpose on the DC signal of the power supply pin of the DUT, whereas one end of the inductor is connected to the external power supply and the other end to the coupling capacitor. The RF power amplifier is used to amplify the power of the RF signal, which is then injected to the PUT of the IC through the injection capacitor that blocks the DC signal provided by an external power supply, after flowing through the bi-directional coupler. A bi-directional coupler is connected with two different power meters for measuring the RF signal forward and reflected power, respectively. The DPI failure criterion is considered depending on the DUT specifications, sensitivity of the circuit, functionality in nominal condition and the applications where the IC usually operates.

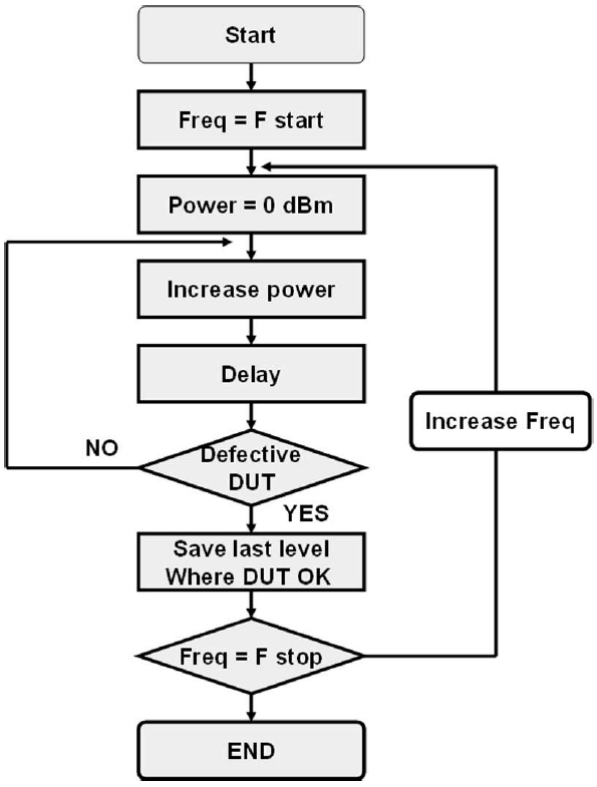


FIGURE 1.5 – Proposed flowchart for the DPI test algorithm to characterize the conducted immunity level of an IC under test [17].

DPI test algorithm was implemented according to the IEC 62132-4 standard for evaluating the conducted immunity level of the DUT, which is shown in the Figure 1.5 [17]. The amplitude of the RF signal power was incremented linearly, while varying the DPI frequency between 50 and 1000 MHz with a linear step size of 50 MHz. If the measured RF signal power at any corresponding DPI frequency would exceed the considered failure criterion, that minimum power injected on the DUT the DPI failure should be recorded at each corresponding frequency for causing the DPI failure.

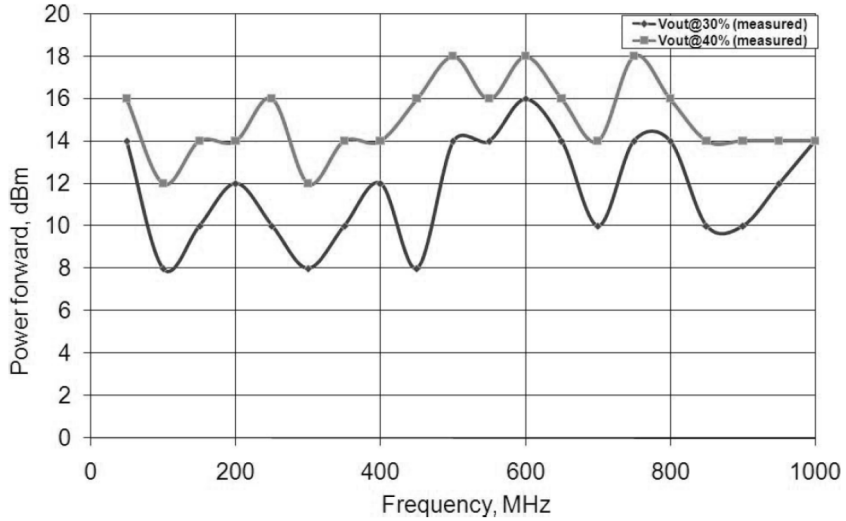


FIGURE 1.6 – DPI test result for evaluating the conducted immunity level of an IC under test at different failure criterion [17].

Different failure threshold criterion (i.e., ±20%, ±30% and ±40%) variations of the nominal output voltage level and a ±10% jitter variation were considered [17]. Figure 1.6 plots two different conducted immunity waveforms of the DPI measurement data (i.e. forward power and frequency) for a CMOS inverter circuit at different failure criterion. It was found that greater amount of forward power was needed to exceed the +40% failure criterion compared to that of the +30% variations considered on the nominal output voltage. Hence, the tested CMOS inverter circuit showed higher conducted immunity profile throughout the entire DPI range due to considering higher criterion (i.e. +40% against +30%).

The DPI simulation algorithm was proposed in [15] based on the DPI test measurement procedure established in accordance to the IEC 62132-4 standard [16]. Figure 1.7 demonstrates the DPI flowchart based on the DPI measurement performed on the digital

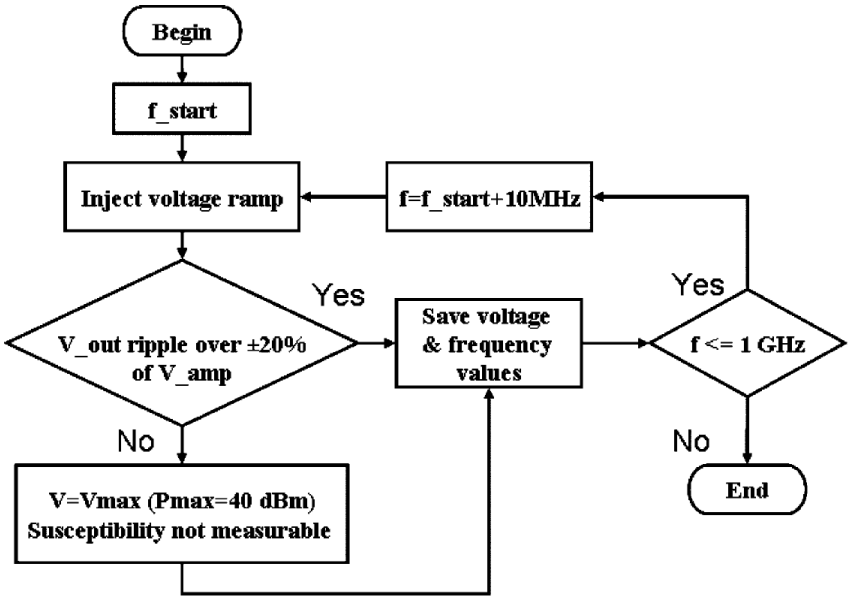


FIGURE 1.7 – DPI test algorithm setup for evaluating the conducted immunity level of an IC under test [15].

core of the custom-made CESAME IC chip fabricated in 0.18 um CMOS technology. The flowchart shows that DPI frequency of the disturbance signal was considered to vary between 10 MHz and 1 GHz with a linear step size of 10 MHz. The simulation was conducted in the time-domain at each DPI frequency. Moreover, considering a fixed DPI frequency, the generated RF signal power was incremented linearly with a small step-size from a minimum value (e.g., −30 dBm) to the maximum power limit (40 dBm) until the DPI failure would be observed. The DUT was considered to fail if the considered failure criterion (i.e., ±20% variation on the voltage of the output data and a jitter more than ±10% of the data output edges) was exceeded due to injecting the amplified RF disturbance signal on the power supply pin of the NORM digital core of the DUT.

The exact injected power into the IC PUT at each corresponding DPI frequency was recorded when the failure criterion condition was achieved. Figure 1.8 plots both the measurement and simulated data of the injected power versus the DPI frequency ranging between 10 and 1000 MHz [15]. The proposed DPI simulation model could be validated as the simulation results was found to be comparable to that of the experimental measurements due to observing similar frequency matching locations at the high and low conducted immunity data points (i.e., injected power). However, a significant difference

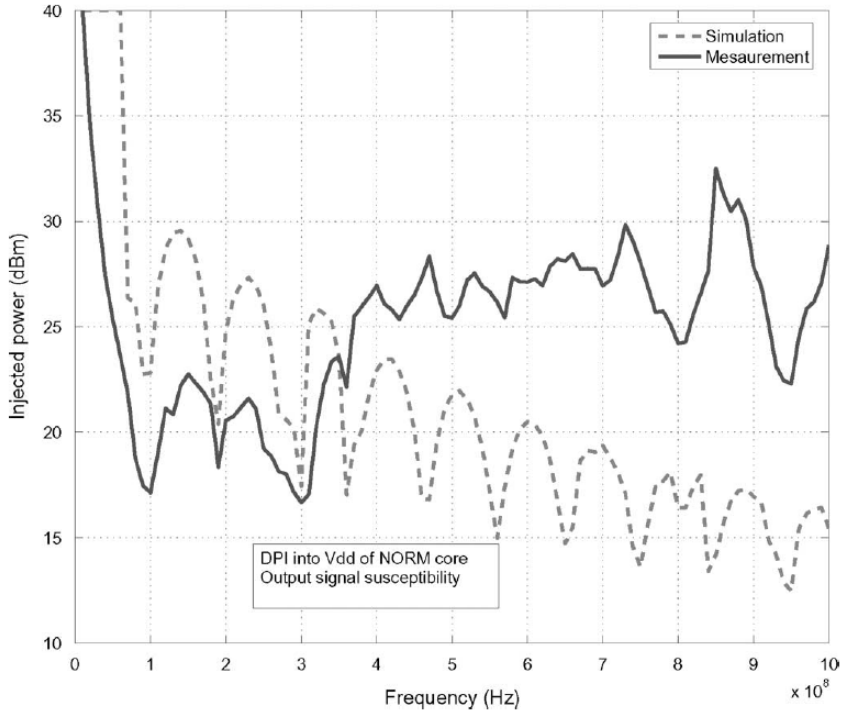


FIGURE 1.8 – Simulation and the measurement result for evaluating the conducted immunity level the DUT [15].

of around 20 dBm injected power between the measurement and simulation curves could be observed above 360 MHz due to the ripples, without taking into account of the the power losses within the DPI system in the proposed model.

1.1.3 Conducted immunity and emission modeling techniques of ICs

Producing accurate EMC models enables to predict the conducted immunity and emission levels ICs accurately in both time and frequency domain, as well as allows determination of various failure modes and mechanisms activated due to either injecting the EFT signal or coupling of a continuous sinusoidal disturbance signal with a single-tone frequency to both analog and digital circuit structures (i.e., oscillator, regulator, micro-controller and so on) embedded within different IC model [8].

Numerous researches were conducted on developing EM immunity and emission models. Different types of immunity models for low dropout regulator (LDO) were proposed

and designed and fabricated in CMOS 90 nm technology [18]. Those immunity models were compared to experimental results for highlighting importance of including PCB track model, on-chip package, decoupling and parasitic components network to design the IC model with greater accuracy. Moreover, immunity behavior of digital cores embedded in an IC designed in 0.18 μm CMOS technology was studied and evaluated using the developed immunity model involved construction and extraction of different components including PCB track model, IC package and lead model, DPI immunity test setup model and transistor based model for digital cores [15].

The basic ICIM-CI structure of an IC chip to coupling of conducted harmonic disturbance on various input/output pins, VDD and ground (GND) pins is based on readily available ICIM-CI standard proposal based on standard IEC 62433-4 [19]. The dual port ICIM-CI model structure was proposed in [20] for conducted transient EFT pulse applied on different IC pins shown in Figure 1.9. That model composed of PDN that consists of passive lumped resistive, inductive and capacitive components for modeling the path way of EM interference injected at different disturbance input (DI1 and DI2) terminals of IC. It consists of IB that represent different circuit schematic embedded in the IC. Applying failure criterion to different observable outputs (OO) pins of the IB blocks would allow identifying the IC failure types and immunity level to conducted interference associated to different output waveform observed at those output pins. The conducted immunity model construction and extraction measurement techniques have been discussed in this section along with the model validation results and analysis on the IC immunity modeling.

In [21], the ICIM-CPI model was proposed for a 32-bit micro-controller that included EFT test bench setup model to characterize immunity behavior according to the standard (IEC 61000-4-4). The block diagram was proposed to represent the overall ICIM-CPI model construction of the micro-controller, as shown in Figure 1.10. The overall immunity model structure is composed of PDN block that is be used to represent overall impedance between the EFT injected pulse terminals (T1 and T2) and reference ground terminals (GND1 and GND2) [21]. PDN model was designed and constructed using linear passive components (resistors, inductors and capacitors) in series-parallel connections to model IC package and lead, on-chip interconnections and IC bonding wires to connect between VDD and GND pins.

The purpose of designing the PDN block is to model conducted disturbance coupling path from the external EFT model environment to the internal IC pin. Non Linear Block (NLB) model design was performed with non-linear active electronic components such as

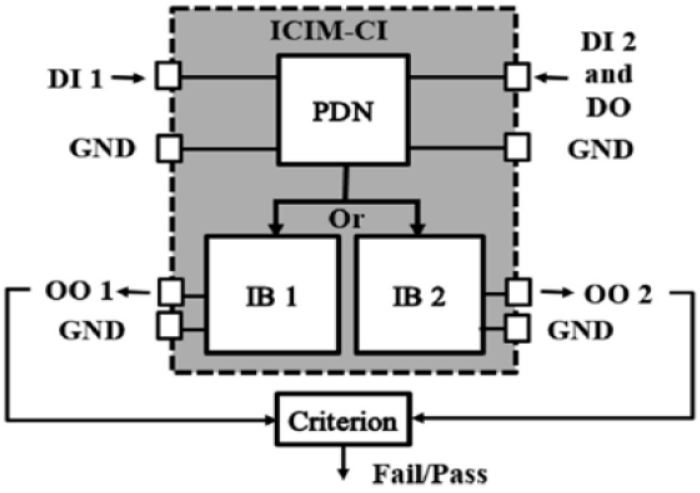


FIGURE 1.9 – Dual port ICIM-CI model structure of an IC [20].

diodes to protect the IC from the permanent failure or damage due ESD coupling and EFT pulse injection to IO, VDD and VSS pins. NLB model is essential to describe non-linear characteristics of the EFT pulse propagation pathway into the IC and was linked with PDN model through internal terminals (i.e., IT1) and to connect VDD with input terminals of IC as shown in Figure 1.10. The output waveform was monitored at the OO IC pin due to the EFT pulse injection at T1 terminal. The failure block contains files or computed data or results obtained at OO terminal, which allows detecting the failure types due to injected harmonic disturbance depending on the failure criterion defined at the associated output pin.

The conducted immunity model of an 8-bit micro-controller was developed for simulating immunity behavior in time-domain based on experimental characterization of EFT test setup [22]. The overall IC immunity model considering EFT test setup model, PDN, IO model and EFT or ESD protection model within the IC package and die (Figure 1.11) [22]. The overall IC immunity model construction involved modeling EFT test bench using transient voltage source with a 50-Ω series resistance for producing standard EFT pulse, followed by a voltage amplifier to amplify EFT generated voltage up to 2 kV. In order to model the EFT disturbance between the EFT source and IC pins, coupling paths were modeled using injection capacitor (C_{inj}) and DC power supply feed inductors as shown in Figure 1.11. The high impedance between the VDD/VSS pins and IO pins was modeled using resistors (R2, R3) and capacitors (C2 and C3), respectively. PDN model was

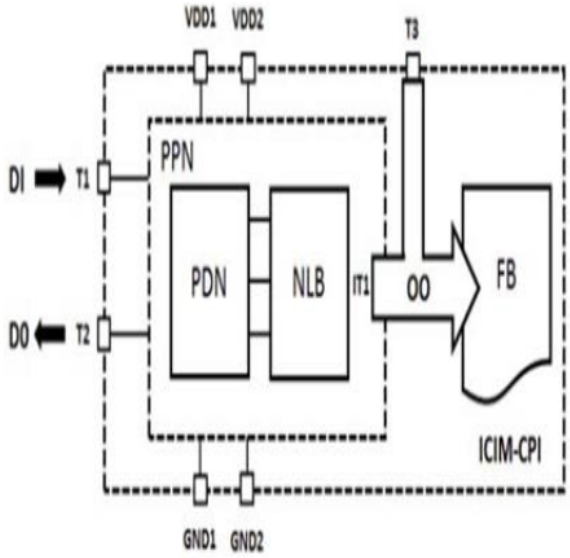


FIGURE 1.10 – Structure of the proposed ICIM-CPI model [21].

constructed using linear passive RC components connected in series-parallel networks for linear coupling between VDD/VSS pins and some non-linear active diodes for non-linear coupling between power and ground rails. PDN model, on-chip package model, IO model and ESD protection model was developed from the IC immunity experimental characterization, basic knowledge of IC layout structure and IC manufacturer provided data could be obtained from for EFT protection structures [23]. EFT protection model could be obtained based on the IC layout design from the IC manufacturer that consist of diodes that should function as trigger, nFET and pFET power clamps.

This IO protection model circuitry was implemented with each IO pad or pin to allow diverting large currents from the VDD pins to the GND during EFT events and to prevent rapid or sharp rise or change in voltage of VDD under coupling of EFT pulse [22]. The transistor-netlist based circuit model for the IO cell in Figure 1.12 [22] is composed of nFET and pFET transistors so that the IO cell can be used both as high or low enabled input and output. Different measurement techniques are involved to extract parameters of constructed PDN, IO and lumped parasitic components of series-parallel network on-die package model is mentioned below.

Research study was also conducted to construct conducted immunity model of the phase locked loop (PLL) circuit embedded within the IC fabricated in 90 nm CMOS technology in order to estimate the long-term conducted susceptibility of the PLL in frequency

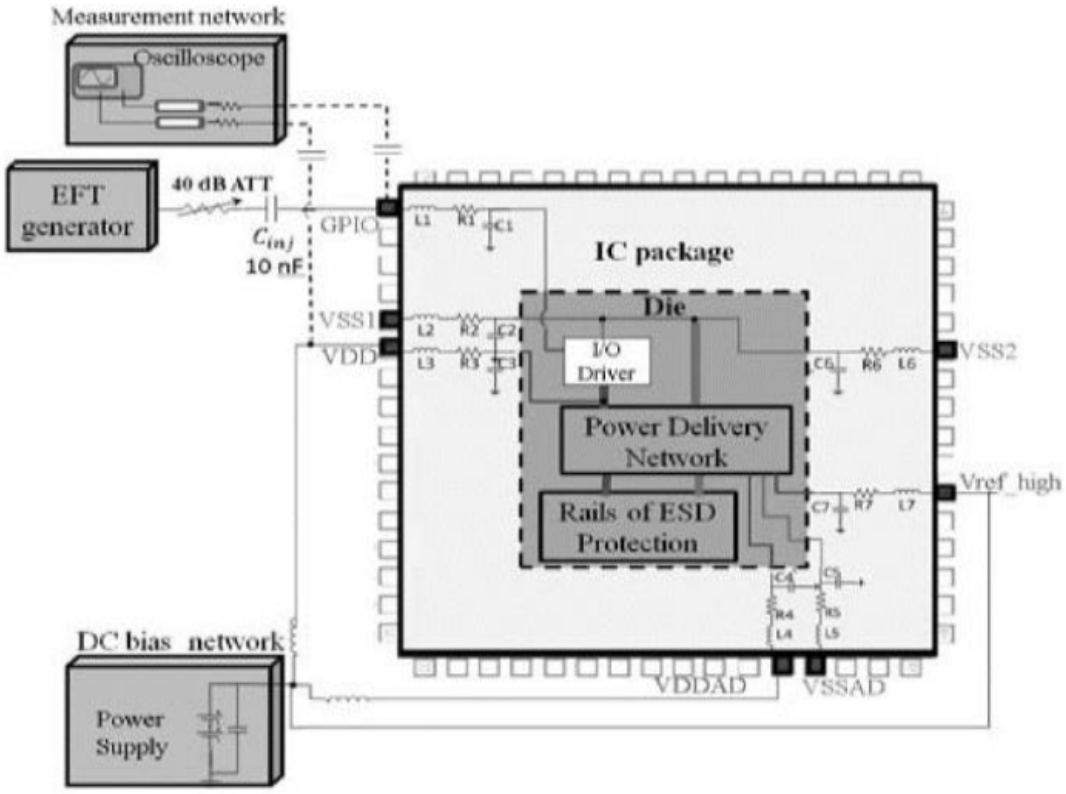


FIGURE 1.11 – IC model structure with EFT setup [22].

domain due to the injection of conducted harmonic disturbance power to the VDD pin of the IC [24]. The simplified IC susceptibility model diagram for predicting the PLL immunity with DPI setup is presented in Figure 1.13 [24]. The proposed susceptibility model for the PLL include model construction two main blocks. PDN model for the PLL circuit structure was designed with passive linear R, L and C components to demonstrate the overall equivalent impedance network between the VDD and GND pins for each different sub-blocks of the PLL. The PDN model included on-chip interconnection, parasitic inductance for the IC package along with the DPI test bench model and EMC test board model for explaining exact EMI coupling paths to different pins of PLL structure. The objective of the IB model construction for the PLL is to explain and understand the PLL circuit response to the conducted harmonic disturbance coupled on the VDD pins of different sub-circuit blocks (i.e. frequency divider, voltage controlled oscillator and phase detector). IB block model was constructed from using the transistor based SPICE model to design the complete PLL circuit schematic in bulk CMOS technology. Accurate IB block

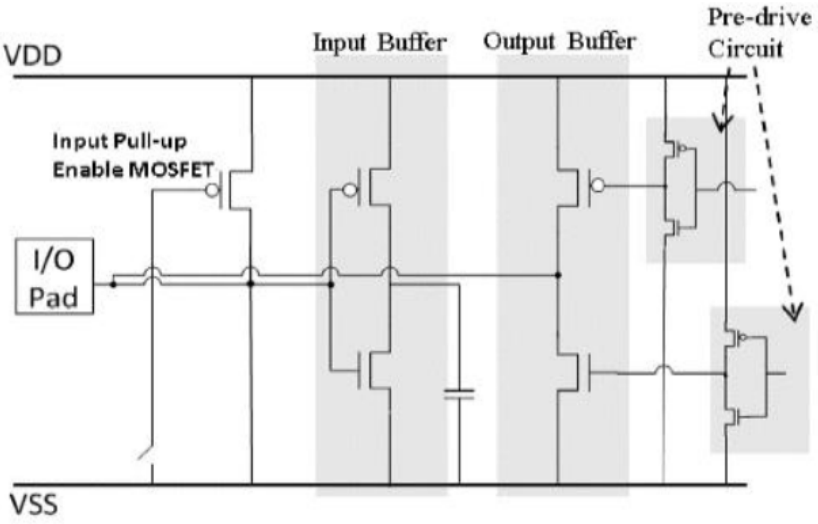


FIGURE 1.12 – IO model protection circuitry of IC model [22].

model description could enable to detect the failures induced by the EMI coupling on the VDD pins, which results in validating the immunity model by producing the simulated immunity curve comparable to the experimental results.

The conducted immunity model extraction of an IC involves determining parametric values of different linear and non-linear components that has been used to construct different parts of the model. The research study presented in [24] extracted PDN block model for the PLL circuit from impedance measurements by S-parameter experimental characterization using 2-port Vector Network Analyzer (VNA) and high frequency probes. Different types of impedance measurements between the VDD and VSS pins of the PLL circuit enabled to extract exact component values for the package inductance, equivalent capacitance and determine substrate-coupling measurement values.

Similarly, *S*-parameter experimental measurement technique was also used for impedance measurements between each VDD and VSS pins to extract both on-chip package lumped parasitic component values and passive linear components of the on-die PDN model constructed for an 8-bit microcontroller. EFT/ESD protection network model could be extracted from the I-V graphs produced by the experimental measurements of current (I) and voltage (V) for non-linear active EFT and ESD protection diodes. IO cell model extraction, which depends on the type of cell configuration (logic high or low output), could be achieved by certain experimental test setup for obtaining nFET and pFET parameters, including gain, voltage and current values [22]. For determining the package

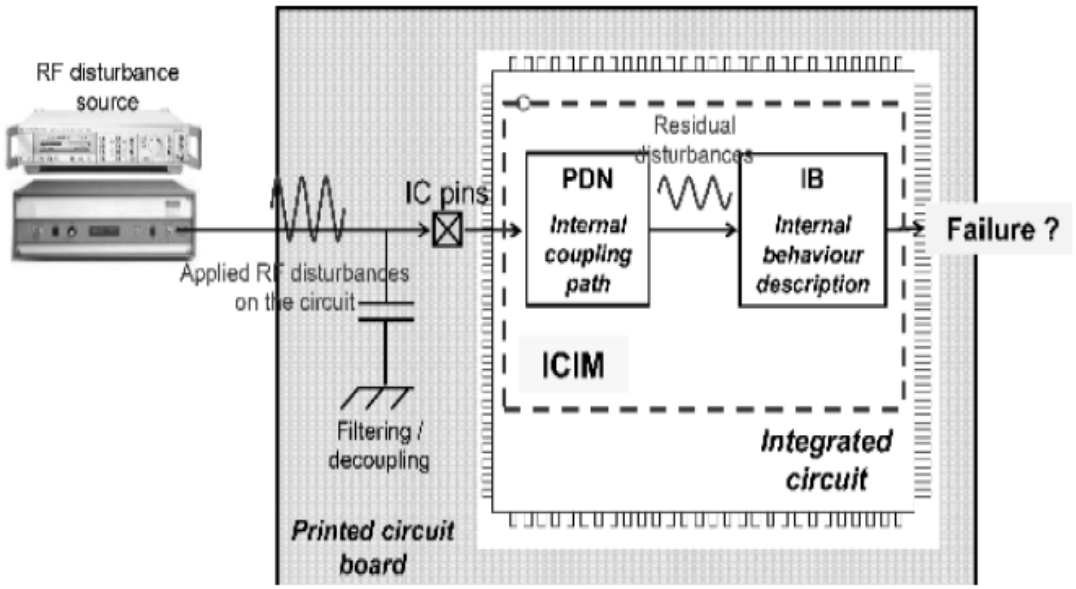


FIGURE 1.13 – IC immunity model for the PLL component including the direct power injection test setup [24].

inductance and capacitance values, various methods for determining impedance between the IC ports using S-parameter measurements were proposed. Figure 1.14 shows one of the possible measurement technique for determining the impedance between the power rails of IC and package inductance of bonding wires [25]. This measurement method allows to measure S_{11} parameter, which could be used to determine the input impedance and hence extract the R6, C6 values as indicated by the arrows marked the on-die PDN model as shown in Figure 1.14.

The study conducted in [25] suggested another S-parameter measurement method using VNA was proposed for determining capacitances between IC package, die and VDD/VSS planes. That measurement method involved connecting one port of the VNA to any one pin and the other port to the GND for measuring S_{11} parameters while other IC pins remain disconnected as depicted in Figure 1.15 [25]. This measurement method allows to obtain L1, C1 and R1 values. Hence, experimental characterization are necessary to compute and extract the parameters of different components used to develop the immunity model. The NLB, consisting of active diodes and I/O ESD/EFT protection models, could be developed and extracted either from the IBIS file or by simulation using a circuit simulator based on the knowledge of the specific IC modeled by the user. The

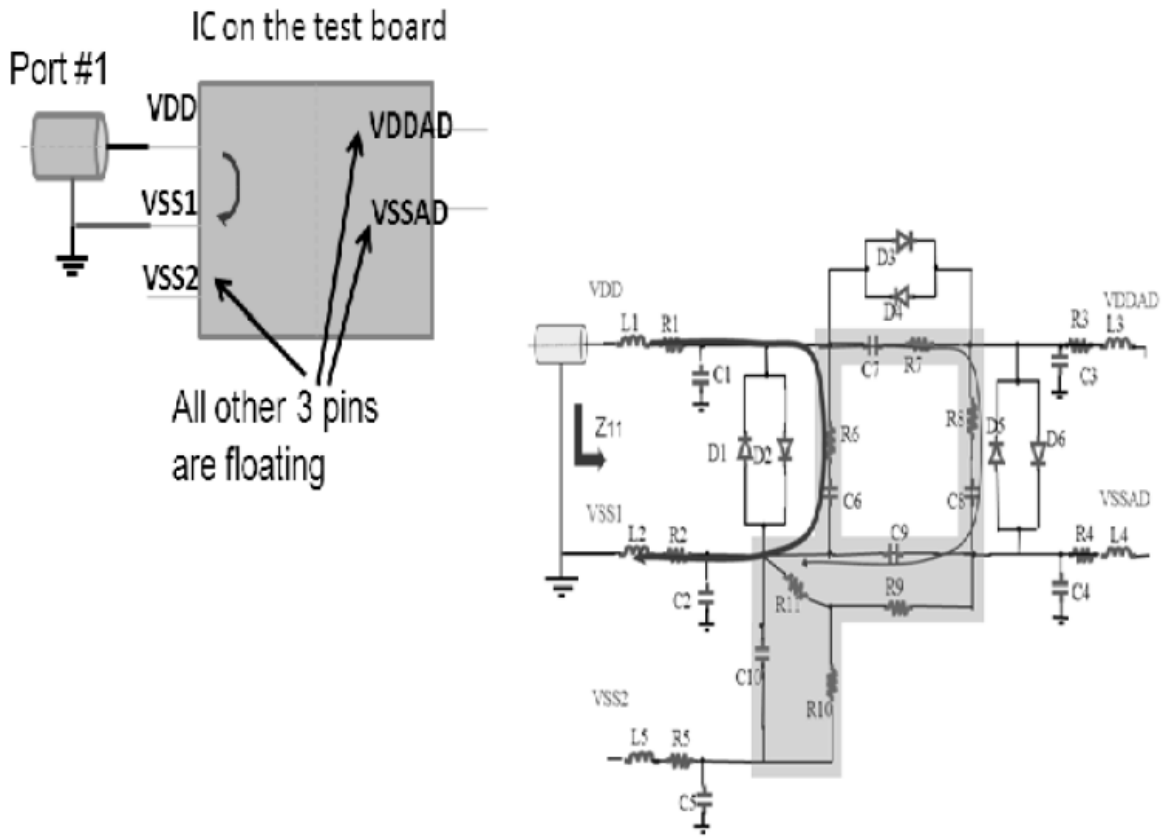


FIGURE 1.14 – Measurement method for the IC PDN model extraction [25].

Transmission Line Pulse (TLP) measurement approach is performed using the TLP generator based on the IEC 62615 standard for obtaining I-V measurements to extract the NLB components model [21]. Injection of the TLP pulse at different input terminals and measuring voltage and current values at these terminals would allow characterizing active diodes connected between GND and input terminals.

After completion of the PDN and IB block model design, construction and extraction steps, conducted ICIM-CI validation is very crucial to proof accuracy of the developed immunity model. Model validation step involves conducting EMC performance simulations in different CAD software so that the simulation results of predictive EM susceptibility level can be comparable to actual measurements obtained from available experimental immunity characterization tests. The developed conducted immunity model of an 8-bit micro-controller was simulated and the results were compared with experimental data.

Figure 1.16a illustrates the simulated curve for the predicted voltage variation wa-

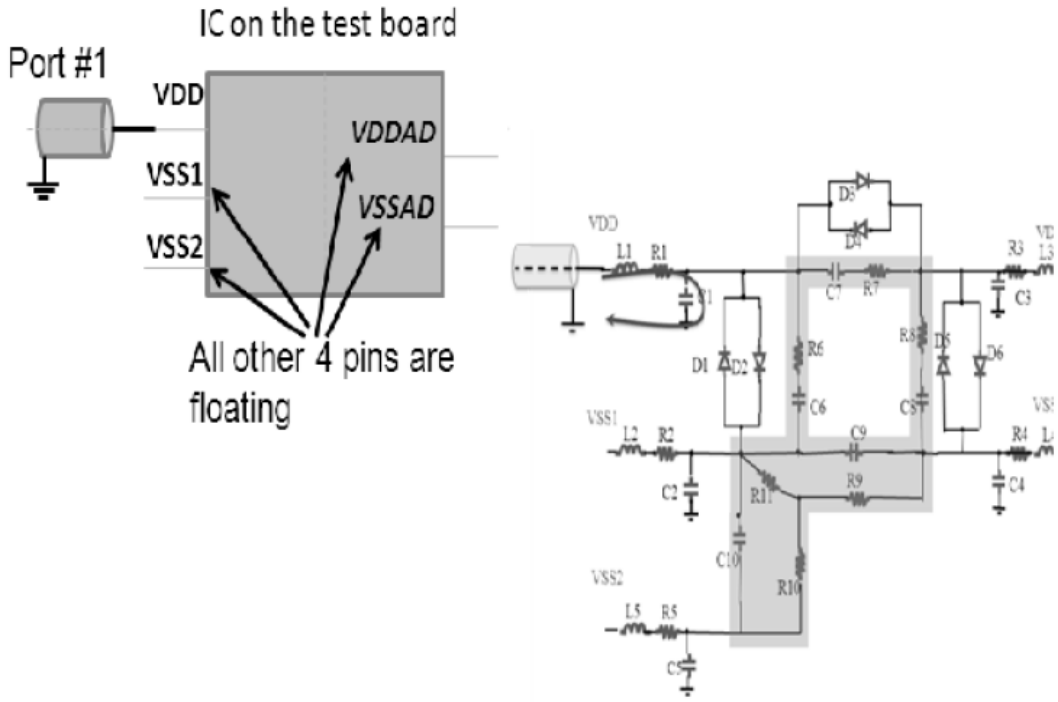
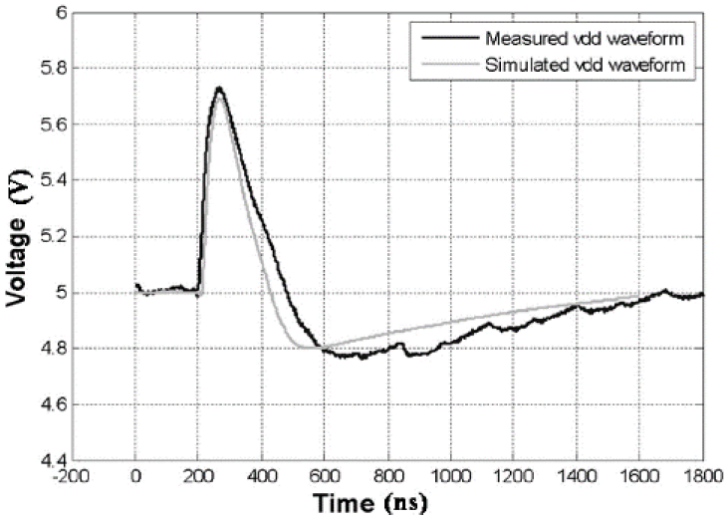


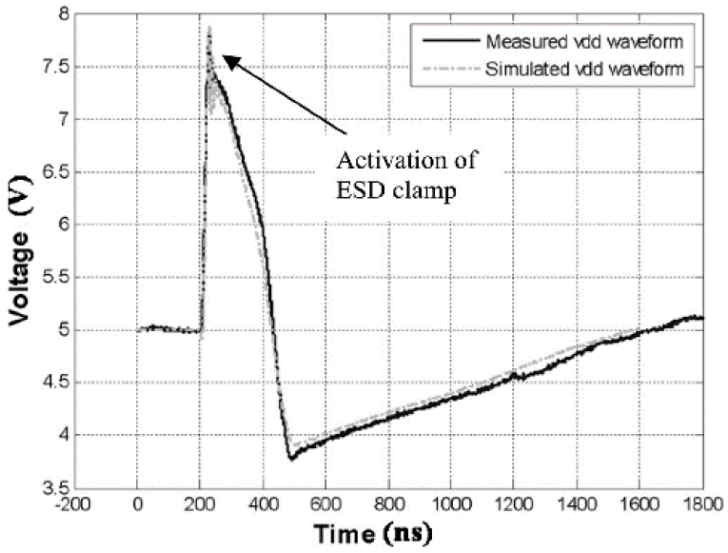
FIGURE 1.15 – Measurement method for the IC package model extraction [25].

veform and actual measurement waveform when an EFT voltage of 200 V was injected into VDD pins of the IC [22]. The EM conducted immunity characteristic behavior of both simulated and measured curves in the transient domain demonstrate similar trend in the VDD variation with minimal difference, which proves the validity of the proposed model for estimating and understanding IC immunity issues. The developed model was further analyzed with ESD diode model by changing the VDD waveform due to coupling of 1600 V EFT voltage into the VDD pin. Figure 1.16b demonstrates a sharp rise in the VDD voltage in the form of a spike followed by rapid decline of the supply voltage within very short time interval. The peak value is directly related to the applied EFT voltage leads to trigger the non-linear active diode so that the high current generated on the VDD pin could be diverted through the diodes from the VDD to the GND for ensuring protection of the IC pins from permanent damage.

The conducted immunity model for the PLL was constructed, extracted and simulated for S-parameter measurements to proof that the equivalent input impedance of the extracted PDN block is similar to that of experimental measurements over the whole frequency range. Impedance (Z_{11}) comparison profile diagram for the VCO sub-circuit block



(a)



(b)

FIGURE 1.16 – Model validation result (a) EFT voltage 200 V ; (b) EFT voltage 1600 V applied to the VDD pin [22].

of the PLL circuit is shown in Figure 1.17 [24]. By comparing the Z_{11} magnitudes of the measured and simulated curves, accurate matching between the measured Z_{11} and the simulated results with minor deviations was obtained over the entire simulated frequency range of up to 1 GHz

Followed by the validation of the PDN model extraction, the complete PLL immunity model was simulated in transient condition to obtain power supply voltage fluctuation

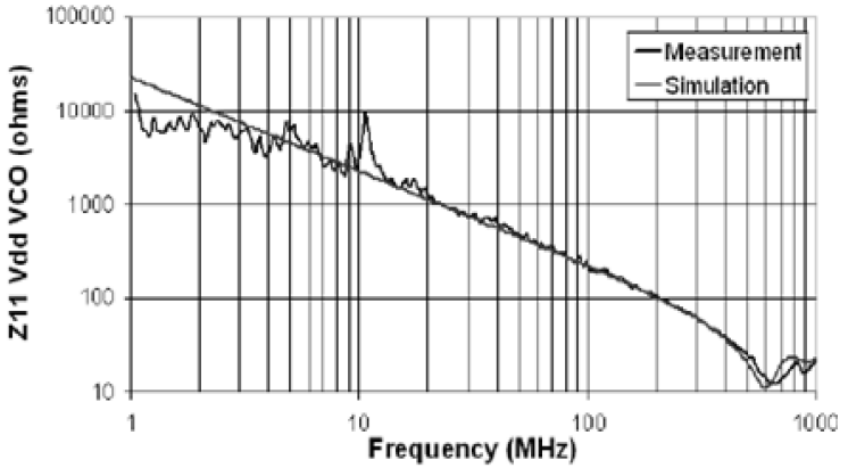


FIGURE 1.17 – Impedance measurement from VDD VCO pin [24].

at different incident RF power and frequency induced by the EMI coupling on the VDD pins. Considering the immunity failure criterion (e.g. 10% voltage variation of the nominal VDD supply) applied at the output of the developed model, minimum threshold injected power (in dBm) and corresponding frequency (in MHz) could be recorded over the entire frequency range between 1 MHz to 1 GHz. The immunity curve of the power injected against the incident frequency of the harmonic disturbance causing the immunity failure is presented in Figure 1.18 [24]. Comparing the estimated immunity curve in frequency domain with the experimental measurement of susceptibility level show that the model accurately predicted the susceptibility level over the entire frequency range. Figure 1.18 also demonstrates that the developed model could predict higher susceptibility to EMI compared to those measurements performed in different frequency values of 400 and 800 MHz, with slight overestimation of immunity level in the low frequency range [24].

EM emission model of an IC can be produced and developed by relying on the simple standard ICEM-CE modeling approach (i.e., IEC 62433-2). The conducted EM emission model for the digital core circuit embedded in the IC was developed [26]. The emission model consisted of the PDN block model construction that is similar to the immunity model. However, unlike the IBblock model, the Internal Activity (IA) block should be constructed and included to develop the ICEM-CE model. In order to develop the IA block model, two current sources were used in parallel connection for quantifying the current generated from the digital core circuit activity during the EM emission (Figure 1.19) [26].

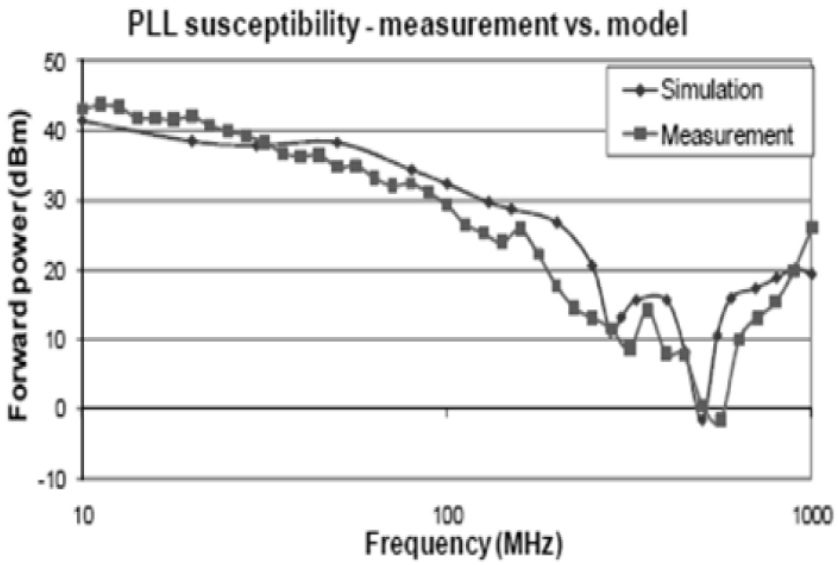


FIGURE 1.18 – Immunity profile comparison between the model and measurements [24].

Two current sources were used to represent the IA block model that could produce triangular waveform during simulations. The IA model parameters include rise time, fall time and peak current that could be extracted from the SPICE transient simulation of the digital core circuit by tuning or optimizing the parameter values for obtaining the best-fit simulated current waveform with respect to the actual current waveform. The proposed PDN network is composed of package inductance and resistances between the VDD and VSS pins as well as the decoupling capacitance for the digital core that could be extracted using the S-parameter measurements prior to estimating the linear passive R, L and C component values to ensure the best fitting of the impedance profile produced by conducting the required measurements between the VDD and VSS pins of the digital core.

The emission model validation produced simulation results on the VDD supply voltage fluctuations of the digital core activity during the EM emission, which was compared to the measured values, as shown in Figure 1.20 [26]. Analyzing and evaluating the simulation results depict similar change in the VDD core voltage fluctuations due to the EM emission, resulting comparable peak-to-peak voltage and oscillating time period.

The EM model was simulated to produce the emission level curve as illustrated in Figure 1.21 in frequency domain [26]. The simulated EM emission level is comparable to measured results and follows similar decreasing trend with increasing frequency of the

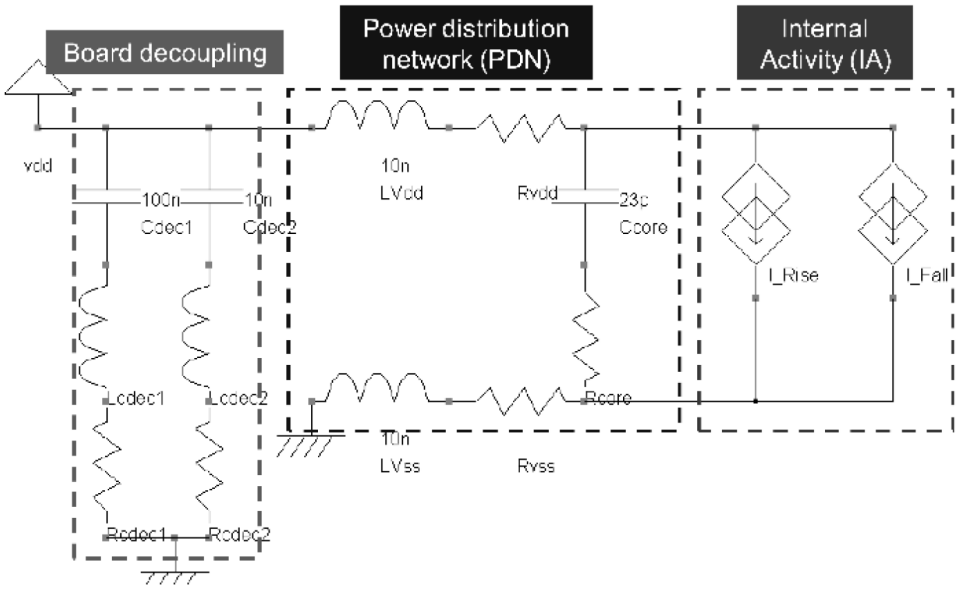


FIGURE 1.19 – Emission model for the digital core circuit embedded in the IC [26].

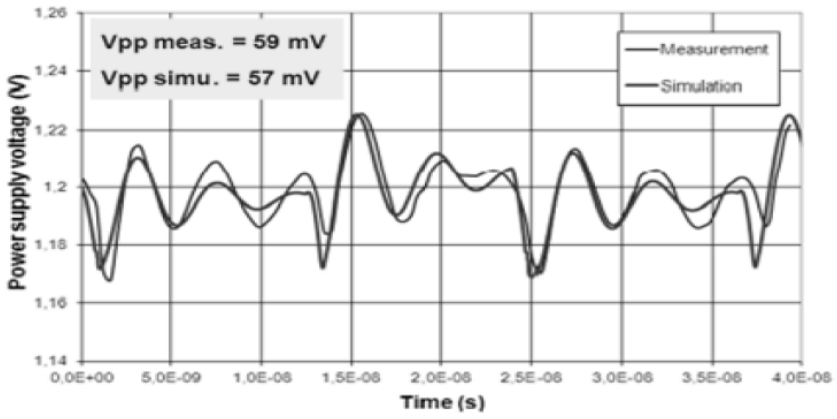


FIGURE 1.20 – Simulated and measured digital core power supply voltage fluctuation [26].

applied harmonic disturbance. However, slight mismatch in the emission level at high frequency between the measured and simulated results was noticed. Improving and minimizing the difference between the simulated and measured results require designing and constructing the complex PCB board and substrate coupling models together with the extraction of complex triangular waveform from the IA block using precise power consumption analysis of the digital core.

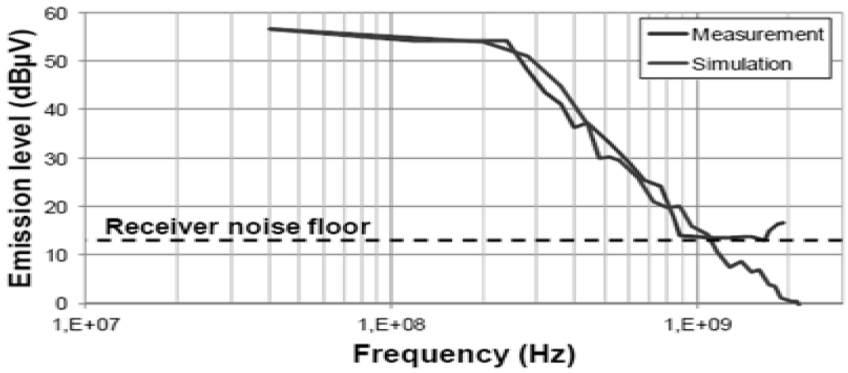


FIGURE 1.21 – Simulated and measured conducted EM emission level from the digital core [26].

1.2 General Principles on EMR of ICs

The study of the EMR of ICs involve evaluating and analyzing the impact of aging stress conditions on the conducted immunity level of the ICs under test. The study aimed to compute the immunity drift by contrasting the conducted immunity measured before and after accelerated overstress conditions, based on the defined stress types, conditions, and duration applied to the DUTs [1] [4]. The EMR methodology was proposed in [4] for characterizing the EMC performance of ICs as shown in Figure 1.22. The flowchart presented in the Figure 1.22 shows different steps involved for characterizing the EM immunity drift after performing the conducted immunity tests (i.e., EFT and DPI) on different pins of the DUTs. The initial step is to create an optimized test plan for both the conducted EMC performance tests and the accelerated test. The optimal test design for EMC depends on several aspects of EMC level measurements, including test samples, cost, time, precision, and repeatability. In addition, the accelerated test plan includes the selection of stress parameters (i.e., stress magnitude and duration) to accelerate the rate of intrinsic wear-out degradation mechanisms and trigger or activate different failure modes of the DUTs [1].

The EMC test measurement procedure should be validated by ensuring that the EMC results obtained are repeatable with little variation among the DUTs. The measurement uncertainty of EMC test components must be reduced through accurate optimization of the EMC test bench and EMC test board or PCB on which the IC under test is mounted, as well as other necessary components, inductors, capacitors and resistors. Furthermore, the test procedure should be validated by subjecting all samples to identical stress condi-

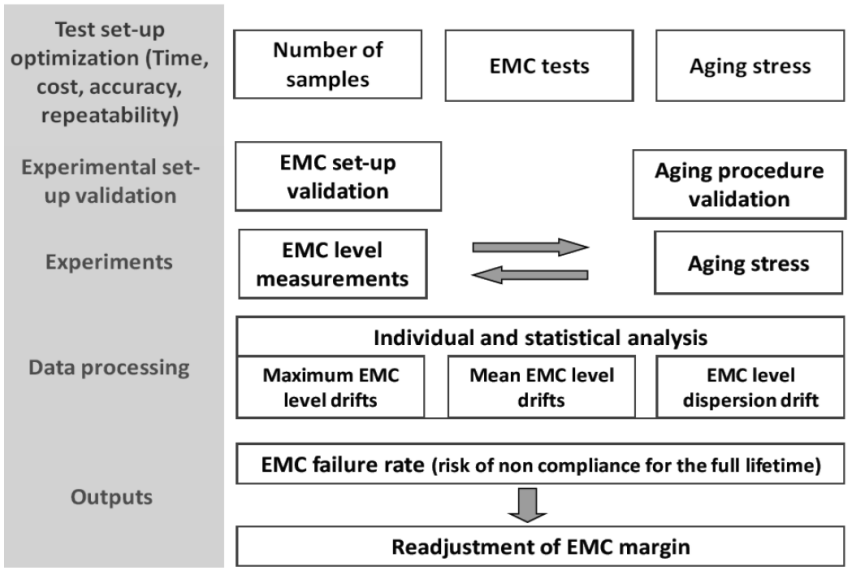


FIGURE 1.22 – Experimental methodology for characterizing EMR of ICs [1], [4].

tions (stress duration, stress magnitude). As a result, it is critical to monitor and maintain the selected stress conditions for all the tested N samples for the total stress duration (T) to ensure that all ICs degrade properly in a controlled environment.Prior to performing the test to accelerate the EMC performance degradation of the DUTs caused by either single or multiple stress types (i.e., temperature, electrical overstress, and humidity) at the selected stress magnitude and duration inside the climatic chamber, the EMC test measurement should be carried out in the nominal conditions as specified by the IEC 62132-4 standard [16]. Depending on the selected stress magnitude and duration, the test should be conducted on N number of test samples. After the test has been conducted for the required duration, the N samples should be removed from the climatic chamber and the EMC measurement test should be conducted in either the time or frequency domain to obtain the conducted immunity data under the influence of various stress conditions.

This measurement setup should be repeated several times in order to investigate the evolution of the EMC performance of aged ICs at different stress duration until the end of the total stress period. Those EMC measurement data of each individual aged IC sample should be recorded for statistical data processing, so that the impact of aging on the EMC performance of the DUTs can be predicted. Various EMC statistically computed drift parameters (i.e. maximum, mean, and standard deviation) can be calculated for N samples following each EMC experiment by subtracting the EMC measured data of each

fresh sample from that of the corresponding aged DUT samples. The statistically measured data would enable to investigate the gradual variations in the EMC performance of the tested ICs as a result of different aging stress conditions. The final step of the EMR methodology entails predicting the EMC failure rate based on the observed EMC performance degradation resulting from the application of highly accelerated aging conditions. This is essential for determining whether the DUT operating within a system is likely to exhibit EMC non-compliance throughout its entire lifetime when subjected to severe environmental conditions. If the EMC performance of the tested ICs falls below the expected and desirable limit during its operational lifetime, the EMC margin must be readjusted by the manufacturers by modifying the EMC test board with EFT protection components or by designing the IC with on-chip EMC protection devices, such as a diode, MOSFET, or filter circuit [1].

While considering the effect of aging on the EMR of the IC, it is essential to investigate if the degradation of the DUT reduces or improves the robustness to the EMI [3]. This can be assessed by evaluating the conducted immunity or susceptibility drift or variations at regular intervals after a fixed aging stress duration, which would also enable the IC designers and manufacturers to identify the EMC non-compliance risk associated with the DUT. The influence of aging on the degradation of the DUT robustness to the EMI is shown in the Figure 1.23 [3]. The fresh DUTs can be considered as an EMC compliant if its initial susceptibility level (ISL) provided by the manufacturer is greater than the required customer's specified limit (CSL) for any particular application (i.e. automotive, medical and aeronautics).

This ISL for any fresh DUT can be determined by comparing with the CSL of that component. Under the influence of aging, the DUT robustness can be categorized into three types (i.e. safe margin, unsafe margin and high-risk margin). The IC can be considered as an EMC non-compliant for a specific application if its final susceptibility level (FSL) determined at the end of the aging test is found to be lower than that of both the ISL and CSL, resulting the IC to become less robust as its conducted immunity level changes from safe to unsafe margin. Similarly, the aged IC immunity level would be considered within a high-risk margin if its FSL is slightly higher than the CSL and lower compared to the ISL [3]. However, the robustness of some of the aged analog and digital ICs (e.g., regulator, micro-controller, operational amplifier and so on) can also remain in the safe margin due to observing an increasing trend in the conducted immunity level, causing the FSL to be larger than that of both the ISL and CSL as depicted in the Fi-

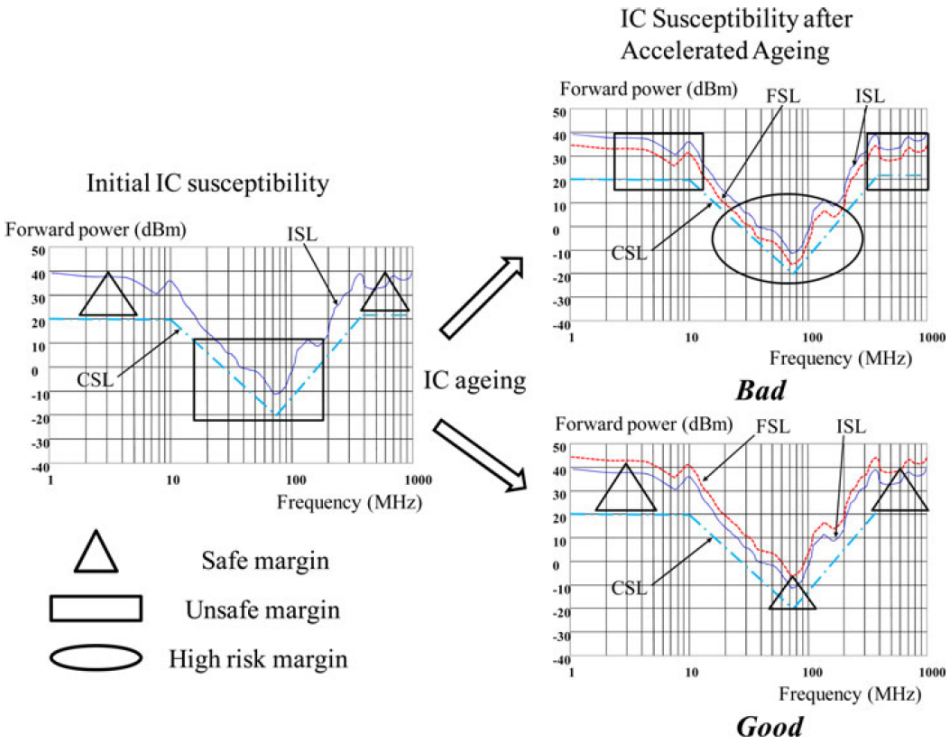


FIGURE 1.23 – Characterizing the EMR of the DUT under the influence of aging [3].

gure 1.23. Thus, the EMR immunity issues for the ICs should be considered during the designing and manufacturing phase for any specific application.

Time-dependent accelerated aging methodology was proposed in [11] to study the combined effect of the aging and the EFT test for assessing the EMR on the conducted immunity of the DUT as shown in the Figure 1.24. This methodology was proposed to measure the immunity drift during the continuous aging process by applying the temperature stress on the IC under test for a certain period of time. In order to study the evolution of the conducted immunity of the tested IC, the EFT measurement was performed on both the fresh and aged IC sample. The fresh sample was aged prior to performing the aging test inside a climatic chamber under constant thermal stress of 130 °C and electrical overstress of 5 V for a fixed aging stress time ($T = 24$ hours). After the completion of the aging test for T hours, the applied stress conditions were removed for very short period of time t. The EFT injection test was performed on the DUT pins within this short time in nominal condition. This EFT injection testing time t should be short compared to the aging test duration for ensuring the permanent degradation induced by aging would not be recove-

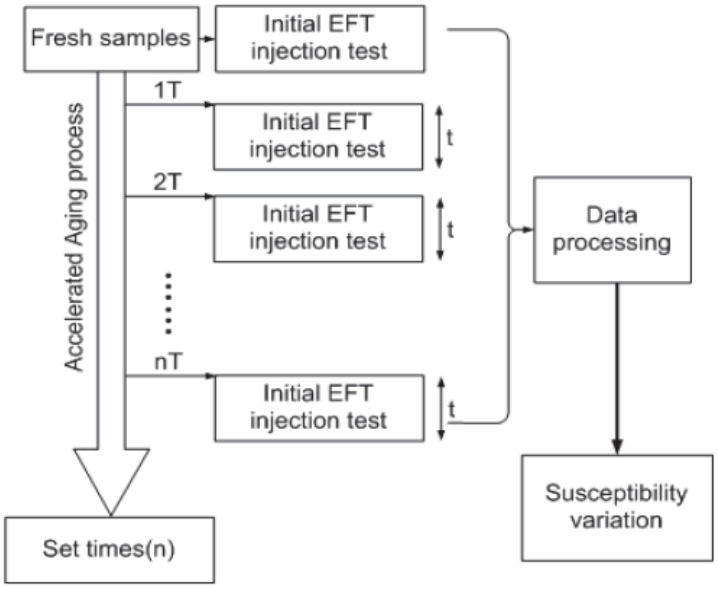


FIGURE 1.24 – Time-dependent EMR methodology under accelerated aging conditions [11].

red. The accelerated aging test resumed and the aging process continued for another T hours, followed by performing the EFT test on the tested ICs for another ($t = 1$ hour) under the nominal temperature conditions. This measurement-stress-measurement continuous test flow method was conducted for n times until the total stress duration reached. Finally, the EMC performance degradation data were processed to obtain the conducted immunity variation after each aging stress T duration.

In [11], the susceptibility variation was observed on both fresh and aged IC under test due to injection of both the positive and negative polarity EFT pulse on the IC PUTs as shown in the Figure 1.25. As observed, the EMR capability of the tested pins varied due to accelerated aging. It was found that the power supply pin showed least EMR capability than other tested pins due to wide variation of the EFT failure voltage throughout the aging period. Moreover, slight degradation in the EFT voltage injected to induce failure was also observed for both ground and reset pins under test. Hence, the micro-controller tested under the influence of both high temperature and electrical overstress aging was found to be less robust to the EFT test. The EMR study revealed that the conducted susceptibility degradation to EMI increased upon the EFT injection on the tested IC pins.

The effect of aging on the EM immunity or emission level of ICs at device or com-

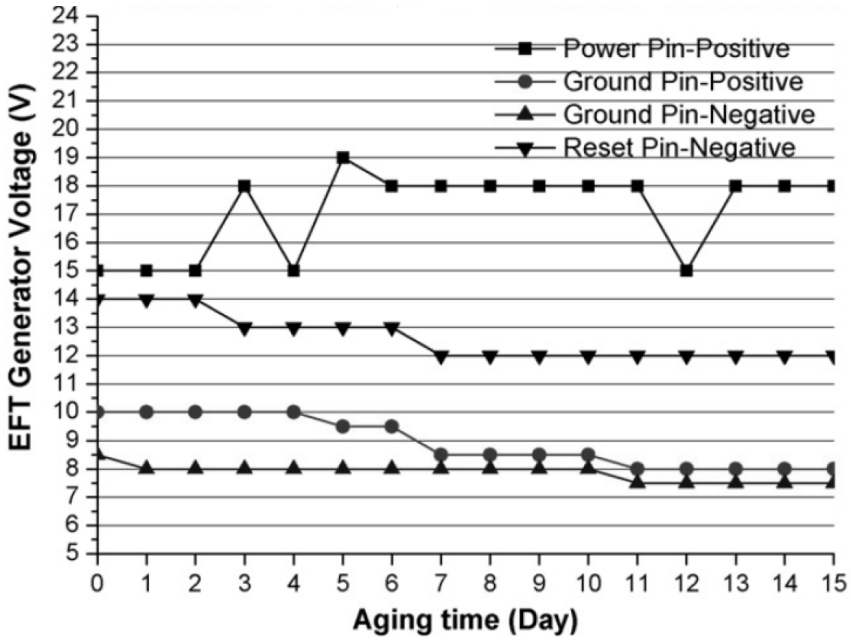


FIGURE 1.25 – EFT failure injection voltage on IC both fresh and aged IC pins[11].

ponent level under influence of different external factors (electrical stress, high or low temperatures) applied for certain stress duration can be modeled to analyze, predict and evaluate long-term evolution of EMC performance. Figure 1.26 presents the proposed block diagram with external environment model integrated into the standard conducted ICIM-CI model for conducting aging analysis to evaluate variations of EM immunity levels of electronic components [27]. Thermal stress is one of the external factor considered in the environment model, which acts as the aging stress factor for the operational amplifier at the component level. The environment model was introduced in the ICIM-CI model to study the aging impact on the EM susceptibility level.

Introducing the aging effect into the immunity or emission model enables to understand and analyze the origin of aging impact on the EMC performance evolution and detect causes of different failure types. In order to predict the long-term immunity of an IC under the influence of aging, the flowchart presented in Figure1.27 describes the methodology to develop the aging model taking into account different aging stress conditions and how this simulation-based aging model should be incorporated with the developed immunity model to simulate the influence of aging on the EMC performance of the tested IC's transistor model [8]. The first required step for identifying aged transistors is to conduct transient simulation on the SPICE transistor model under aging conditions. This is due to the

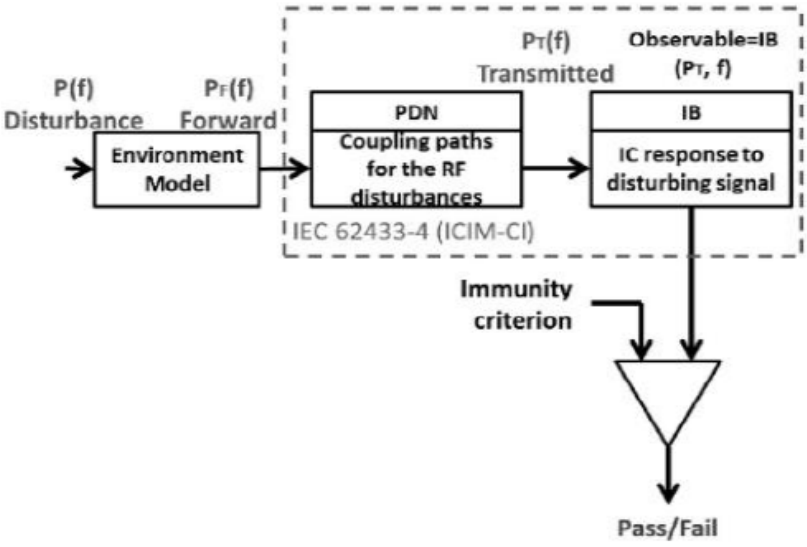


FIGURE 1.26 – Block diagram for the ICIM-CI model with integrated external environmental model for aging [27].

intrinsic degradation mechanisms followed by the computation of aged transistors' internal parameters (i.e., μ_{eff} and Threshold Voltage (V_{th})). Following the identification of aged transistors, the aged transistor model is created and extracted using either physical device characterization or by adding the new electrical parameter values estimated analytically during aging [24]. Aged transistor model netlist needs to be included in the simulation library to construct the immunity model containing aged transistor model. Performing simulation on the conducted immunity model would generate EM immunity curves, while taking into account of the considered aging conditions.

In [28], the simplified block diagram of the conducted susceptibility model was developed for an operational amplifier in the negative feedback configuration with unity gain to conduct aging analysis (Figure 1.28). The simplified EM susceptibility model includes aged transistor netlists for the IB block model in order to evaluate the effect of the applied aging conditions (electrical overstress supply voltage and stress duration). Before including aged transistor netlist in the developed model, variation of the threshold voltages and mobility were experimentally characterized for transistors when electrical stress voltage was applied to the biasing voltage stress duration. Acceleration of transistor degradation mechanisms (i.e., Hot Carrier Injection (HCI), Negative Bias Transistor Instability (NBTI)) due to aging was considered as the main reason for variations of these

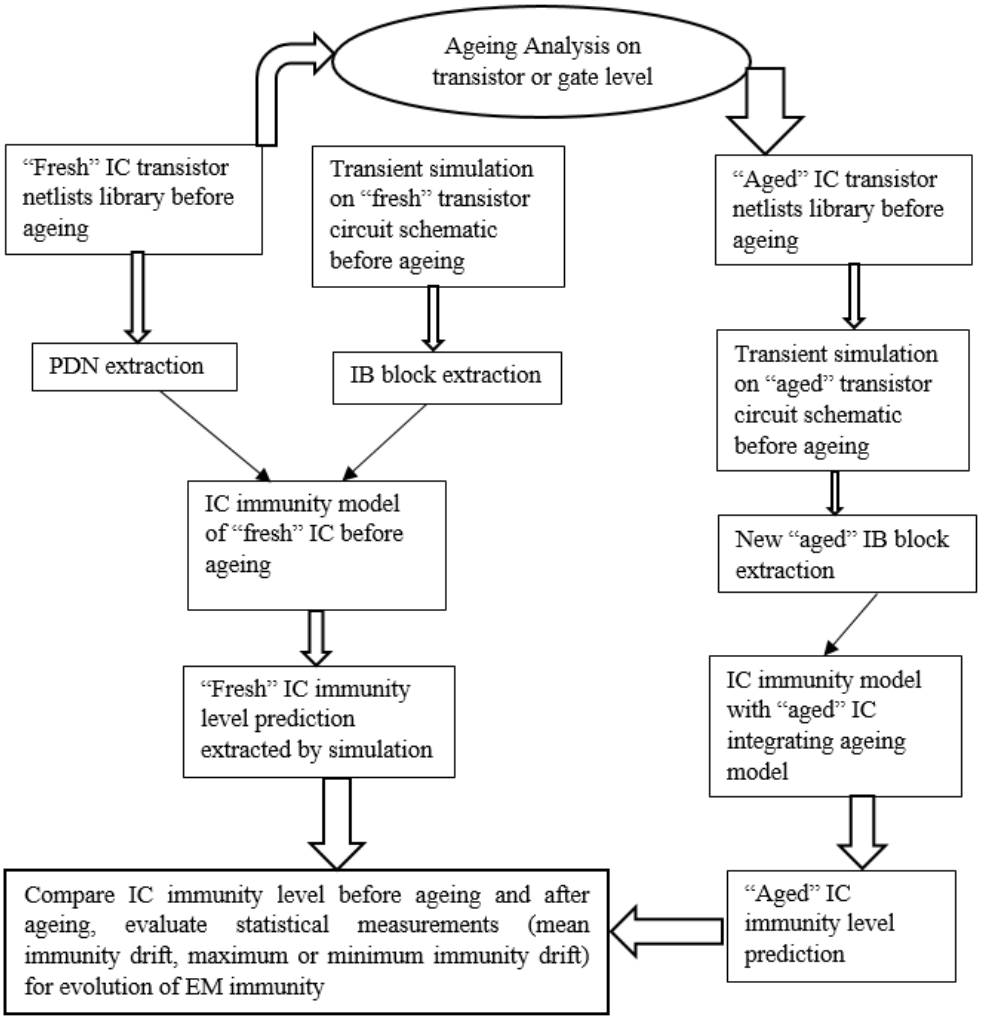


FIGURE 1.27 – Proposed aging-aware ICIM model methodology [8].

electrical parameters.

Offset voltage output induced by the conducted EM interference at a constant injected frequency of 200 MHz and injected RF power increasing from 2 to 5 dBm at different aged time duration is depicted in Figure 1.29. The graphical results in [28] show an increase of DC offset output voltage with the increasing stress time. Moreover, predicted EM susceptibility also increases with the increasing stress duration and injected RF power. The reason for such trend could be explained due to the acceleration of the intrinsic degradation mechanisms that can be responsible to increment the V_{th} according to stress magnitude and duration.

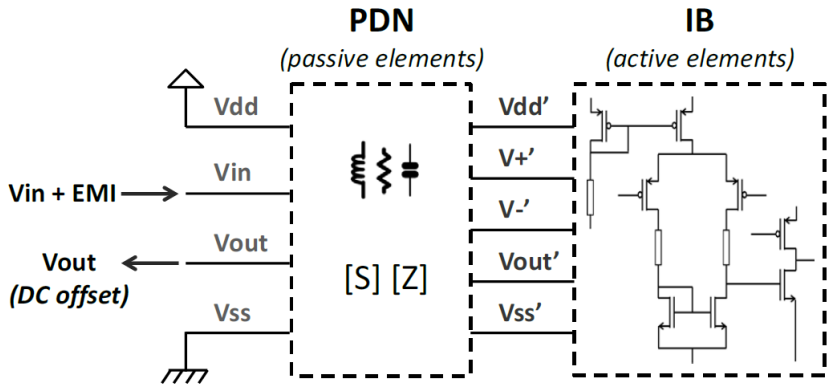


FIGURE 1.28 – Proposed aging-aware EM susceptibility model structure of the operational amplifier [28].

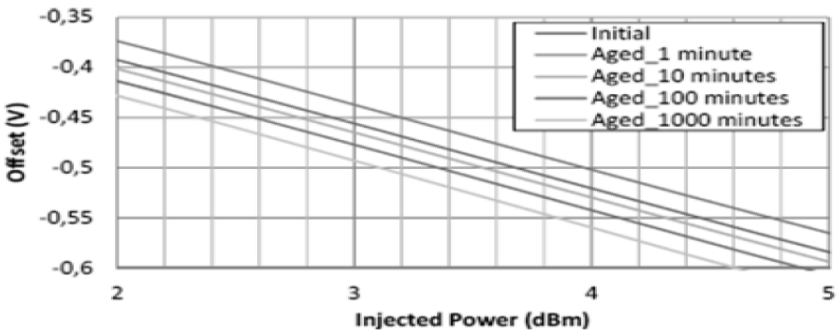


FIGURE 1.29 – Aging impact on the DC offset voltage as a function of the RF power at 200 MHz [28].

Emission model developed for the digital circuit designed in 90 nm CMOS technology was electrically stressed up to a given stress time. Aging-aware emission model produced after determining the analytical relationship between V_{th} variation and stress duration for different applied stress voltage. In [26], the V_{th} variations of the proposed emission model is shown in the Figure 1.30. The graph shows the best-fit curve for the model on the experimentally characterized measured value and increase of the V_{th} would be acceptable according to the n_{th} power MOSFET law [26]. Because of the increase in the threshold voltage with the stress duration, the current consumption modeled by the IA block parameters for the digital core activity could also vary.

Consequently, the aged IA block included new parameters (i.e., rise time, fall time, peak current) while considering the V_{th} variations with aging stress conditions. The evo-

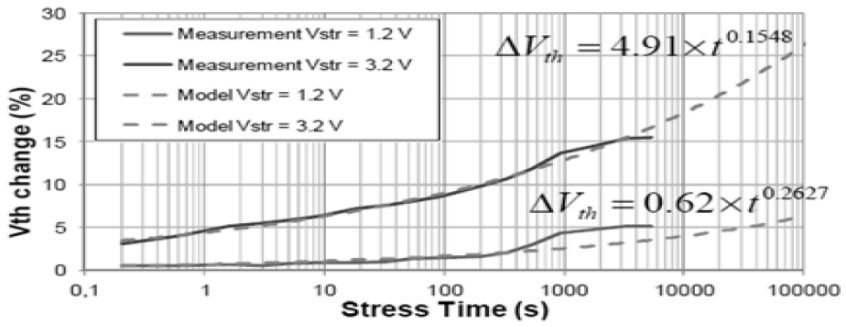


FIGURE 1.30 – Threshold voltage variations depending on the different aging conditions [26].

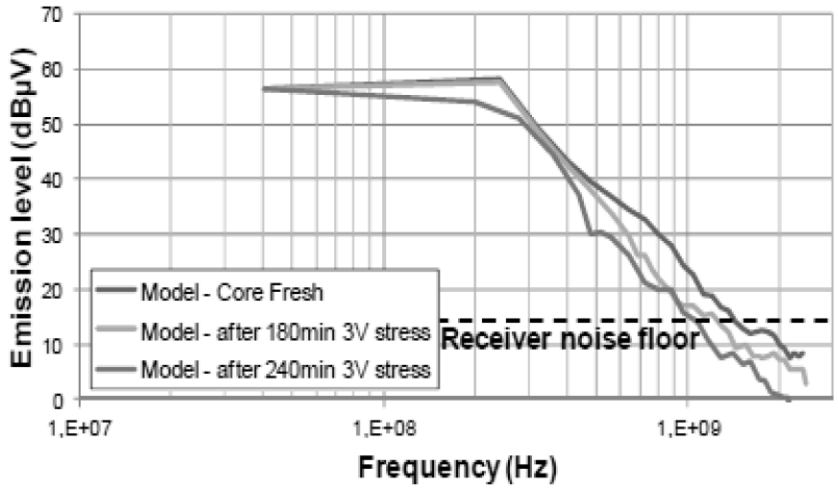


FIGURE 1.31 – Evolution of the EM emission level of the digital core circuit due to aging stress [29].

lution of the EM emission level after aging is provided in Figure 1.31 [29] after applying 3.6 V electrical stress voltage applied on the V_{DD} pin for 120 minutes. Emission level declines with the increase of the injected RF frequency after aging, which was likely due to the decline of the internal current generated from the digital core circuit switching activity and increase of the V_{th} of the aged transistors due to the activation and acceleration of the NBTI degradation mechanism. The NBTI degradation mechanism is activated under aged conditions when negative bias voltage at the gate-source terminal of the transistors and high RF voltage amplitude is applied on the V_{DD} supply voltage.

1.3 General Principles on the Reliability of ICs

The IC-EMC lifetime reliability refers to the functionality that can be expressed in terms of parameters (such as voltage, current, and power) to indicate or predict how long the system would perform before exhibiting various EMC failures under different external operational aging conditions [8], [30].

The Reliability function ($R(t)$) of an electronic component and/or an electrical system is defined as the probability that the component or system remains operational from time t_0 to t, such that it's functionality started at t_0 under the influence of nominal condition [30]. The relationship between the Cumulative Distribution Function (CDF), denoted by $F(t)$, and $R(t)$ is regarded to be opposite, indicating those two parameters refer to the non-failure and/or failure probability function with time. The $R(t)$, which is usually regarded as the survival time t duration elapsed with a specified non-failure probability for a specified population or sample size, can be expressed mathematically in (1.3) where $f(t)$ represents the Probability Density Function (PDF) and the CDF is denoted by $F(t)$.

$$R(t) = Pr(T \geq t) = 1 - F(t) = \int_t^{\infty} f(t)\, dt \tag{1.1}$$

Both the PDF and CDF are essential to develop the reliability model for deriving different reliability metrics (i.e., Time-to-Failure (TTF), Acceleration Factor (AF), Mean Time-to-Failure (MTTF), Instantaneous Failure Rate (IFR)) of an electronic component. The mathematical expression between the $f(t)$ and $F(t)$ is provided in (1.3), which is obtained by taking the derivative of the $F(t)$. The derived $f(t)$ indicates the distribution of failure across the entire operational time range, which represents the failure speed of an electronic component or product.

$$f(t) = \frac{d}{dt} F(t) \tag{1.2}$$

IFR is defined as instantaneous failure rate at time t, denoted $\lambda(t)$. The value $\lambda(t)dt$ represents the probability of having a failure in the time interval $[t; t + dt]$, knowing that there has been no failure in the time interval $[0; t]$ [30].In other words, therefore, it can

also be referred as the ratio of the number of failures during the time period Δt, for the devices that were healthy at the beginning of testing (operation) to the time period Δt.

Thus, by applying the conditional probability theorem, then the total probability theorem, $\lambda(t)$ is written :

$$\begin{aligned} \lambda(t)dt &= \frac{Prob(failure\,on\,[t;t+dt]\,without\,failure\,on\,[0;t])}{Prob(no\,failure\,on\,[0;t])} \\ \lambda(t)dt &= \frac{Prob(failure\,on\,[0;t+dt]) - Prob(failure\,on\,[0;t])}{Prob(no\,failure\,on\,[0;t])} \end{aligned}$$

and finaly

$$\lambda(t) = \frac{f(t)}{R(t)} = -\frac{1}{R(t)} \cdot \frac{dR(t)}{dt} \tag{1.3}$$

It can also be noted that :

$$\begin{aligned} \lambda(t) &= -\frac{d\ln[R(t)]}{dt} \\ \text{hence : } \ln[R(t)] &= -\int_0^t \lambda(u)du \\ \text{and : } R(t) &= \exp\left[-\int_0^t \lambda(u)du\right] \end{aligned} \tag{1.4}$$

Failure rate is commonly used as a reliability metric to quantify the reliability of electronic devices (i.e., ICs, MOSFET and other electronic components). The unit of measurement for the failure rate is expressed in Failure in Time (FIT), i.e., 1 FIT is equivalent to 1 failure in every 10^9 hours of device or a product operation [31]. The physical significance of FIT is that a higher value implies lower reliability of a component due to higher number of failures observed within a specific period of time. Probability of failure and/or non-failure estimated data can be obtained when the accelerated aging on the DUT samples due to the High Accelerated Life Test (HALT) causes functional performance degradation over a specified short duration, which can be modeled by applying various distribution models, including exponential, Weibull, normal, and log-normal distributions on various types of existing life-stress ALT analytical models (i.e., Eyring, Arrhenius, and many more).

A general form of reliability functions is described by the standard lifetime model. The

random variable T, time to first failure, which is considered to follow the $R(t)$, provided that it represents the probability that T is greater than t. The probability that the lifetime is greater than t, $R(t)$, is continuous to the right at all points. The $R(t)$ is assumed to belong to a class of functions that depend only on the parameters of scale, shape and offset :

$$R(t) = R\left(\left(\frac{t-\omega}{\eta}\right)^{\beta}\right), (\eta, \beta > 0) \tag{1.5}$$

with $\theta = \{\eta, \beta, \omega\}$ vector of unknown parameters (η, β and ω respectively the scale, shape and position (or offset) parameters).

If $\omega \neq 0$, then this term represents the lifetime consumed by over-aggressive burn-in ($\omega > 0$) or start-up delay ($\omega < 0$). In the case of testing, this situation does not arise because the equipment or the component under test is produced for the testing purpose, burn-in is controlled and aging is considered negligible. Thus, only those scenario where $\omega = 0$ is considered to be significant and would be deal with.

The statistical distributions (weibull, log-logistic, exponential and log-normal) for probability of failure distribution that are commonly used in reliability belong to this family of models. In the following, we will focus solely on the weibull distribution [30].

Weibull distribution Considering $R(t) = e^{-t}$ in equation 1.5, we obtain the Weibull reliability function class with :

$$R(t) = e^{-\left(\frac{t}{\eta}\right)^{\beta}} \tag{1.6}$$

and PDF :

$$f(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} e^{\left(-\frac{t}{\eta}\right)^{\beta}} \tag{1.7}$$

The service life of ICs can typically be described using a 'Bathtub' curve : infant mortality, normal life, and wear out period of an IC device [3]. The wear-out period is indicated by the deterioration at the end of a device's useful life, induced by a variety of failure mechanisms. The 'Bathtub' curve which represents the life-cycle of an IC that includes three different stages, which are : infant failure period, stable or operational period and wear-out period as shown in the Figure 1.32 [30]. Internal tensions, identified as stressOr parameters, are accountable for the wear-out failure rate (Weibull shape $\beta > 1$).

There are only four varieties of applied and imposed stress conditions : voltage, current, power dissipation, and input signal can be static, dynamic, transient, or surge. Those can be quantified in terms of the level of stress administered relative to their instantaneous mode of failure due to burnout. However, for the sake of uniformity and normalization, they are constrained by the technology's maximum values. Figure 1.32 also demonstrates the mathematical expression for the IFR which remains constant during the normal operational period of a product, depending on the shape β parameter value which differs compared to both the intrinsic and extrinsic failure period of that component.

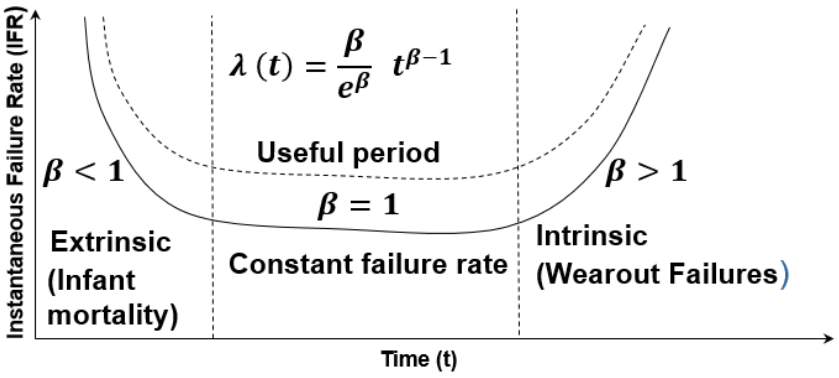


FIGURE 1.32 – Bathtub curve showing the Weibull distribution of the electronic component operating lifetime period [30].

An IC failure during the infant failure period is usually filtered out before usage. However, for newly manufactured ICs, survival of the fittest can eliminate the influence of infant mortality. In the stable period, an IC can operate normally and has good immunity to EMI [11]. Different failure mechanisms coexist, but they have different failure rates and different sensitivities to operation conditions. Their failure rates are related to the type of failure mechanism, internal design parameters such as activation energy, and external environmental conditions such as temperature, thermal cycling, humidity etc. After a long operational period, electronic components begin to wear-out because of intrinsic effects, such as HCI, NBTI and Time Dependent Dielectric Breakdown (TDDB) [4], [32]. Those intrinsic failure mechanisms are induced by applying different external stress factors (i.e., temperature, electrical overstress) on ICs, causing permanent or wear-out degradation of the internal CMOS transistors within the tested ICs due to mostly formation of cracks and holes in gate oxide and change in the physical parameters (i.e. V_{th} and μ_{eff}) of both NMOS and PMOS transistors [32]. Table 1.3 shows different failure modes, causes of

these failure mechanisms which occurs due to applying some external stress factors that are responsible for accelerating the rate of the wear-out period of an IC, hence affecting its EMC performance and lifetime reliability.

TABLE 1.3 – Intrinsic failure mechanisms of an IC induced by accelerated aging [32]

Failure mechanism	**Cause of failure**	**Failure modes**	**Acceleration factor**
Time dependent dielectric breakdown (TDDB)	Cracks and holes in gate oxide.	Gate leakage.	High temp. Electrical field.
Hot carrier injection (HCI)	Trapped carrier in gate oxide due to the effect of ionization of channel carriers near the drain region.	Threshold voltage shift and mobility degradation. Serious issue in short channel NMOS transistor.	Low temp. High drain-source voltage. Radiation exposure.
Negative Bias Temperature Instability (NBTI)	Formation of fixed-oxide charge in PMOS gate oxide.	Threshold drift with partial recovery phenomenon. Serious issue in thin oxide PMOS transistor.	High temp. High negative gate voltage.

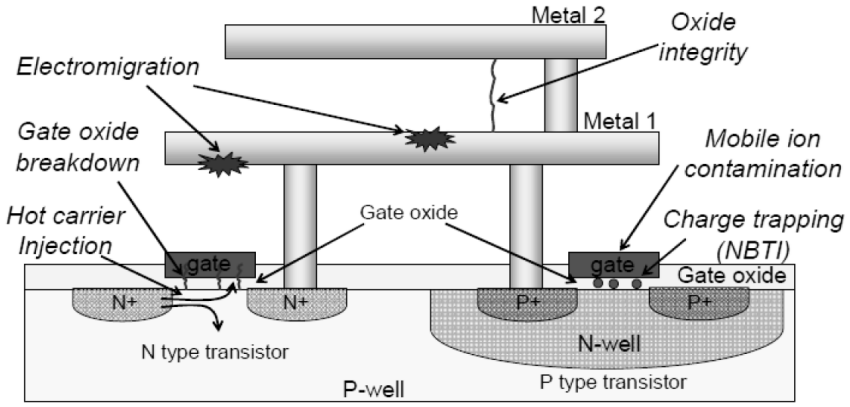


FIGURE 1.33 – Intrinsic failure mechanisms induced in CMOS transistor of an IC [33].

Those intrinsic failure mechanisms (i.e., HCI and NBTI) are considered to be the two most common intrinsic wear-out failure mechanisms that can be activated by exposing the

electronic components to harsh environmental conditions (i.e. humidity, extreme high or low temperatures and electrical overstress). Both the HCI and NBTI failure mechanisms results in the formation of cracks due to the gate oxide defect and the trapping of charge carriers within the gate oxide of the transistor as demonstrated in the Figure 1.33. Those external extreme conditions accelerate the rate of degradation of various intrinsic failure mechanisms which can cause significant modification of the internal parameters (i.e., V_{th} and charge carrier mobility) of the CMOS transistors of these electronic components [33]. Hence, the circuit's functionality or electrical characteristics (i.e, current consumption, operating frequency, voltage, gate oxide resistance) are also affected or modified due to undergoing noticeable permanent degradation, affecting the lifetime reliability throughout the operational period of these degraded electronic devices or IC.

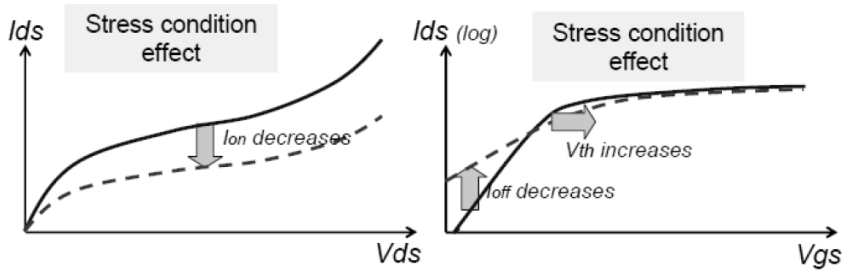


FIGURE 1.34 – CMOS transistor parameter variations induced by intrinsic failure mechanisms from an EMC point of view [33].

The effect of the these relevant wear-out failure mechanisms is responsible for causing degradation of CMOS transistors electrical characteristic parameters within an IC as shown in the Figure 1.34. Depending on the type of the failure modes caused by different external stress factors, stress magnitude and the stress duration, those internal,parameters of CMOS transistors would drift significantly. It can also be observed that the CMOS characteristic curve presented in the Figure 1.34 moves downward as the drain-source current (Drain-source Current (I_{ds})) decreases with increasing the drain-source voltage (Drain-source Voltage (V_{ds})) of the CMOS transistor due to observing significant reduction of its saturation current (Saturation Current (I_{on})) parameter. Moreover, the V_{th} parameter of CMOS transistors would also increase when an IC is subjected to a high temperature stress for certain stress duration. Hence, modifications of CMOS parameters within an IC is responsible for observing quantitative EMC performance degradation, in terms of both conducted emission and immunity to the harmonic disturbance injected on both analog

and digital circuits.

1.4 Conclusion

This chapter has provided a general overview on the characterization and analyzing the EMC performance of ICs, both without and with the influence of external factors (i.e. temperature, electrical voltage and so on). The main purpose of this extensive review based chapter is to conduct a detail study on how to conduct EMC design, extract and produce conducted immunity and emission models that would be based on the IC functionality and its applications.

Several case studies were investigated to explain the modeling methodology for conducted model construction and extraction while considering conducted harmonic EMI applied on the IC pins. These developed immunity and emission models were validated up to a greater accuracy by comparing quantitative predicted EMC simulated results to that of experimental measurements. Moreover, a comparative analysis between the EMC model and measurements results could provide research insight on the importance of proposing complex IC EMCmodels, which include both PCB and the substrate coupling model for accurately predicting the susceptibility level over the higher frequency range greater than 1 GHz. It was also demonstrated how to conduct aging simulations on conducted immunity and emission models to predict origin of the EMC performance degradation due to the intrinsic failure mechanism of ICs. However, those existing research works were only able to demonstrate final conducted immunity EMC level after certain aging period, without showcasing the variation of the evolution of the observed EM conducted immunity degradation at various stress duration in real-time to investigate the aging impact on the EMC behavior of an IC.

Previous research study was conducted on the FPGA device to predict its lifetime reliability based on its functionality and EMC performance, particularly the conducted emission when subjected to the M-HTOL (Multiple High Temperature Operating Lifetime) accelerated aging test. Based on the experimental measurements obtained from the M-HTOL test, the predictive M-STORM (Multi-physics MulTi-Stressors Predictive Reliability Model) was proposed for identifying different possible failure modes and the conducted EM emission from the tested FPGA devices throughout its lifetime [34]. Prior knowledge of these previously conducted research works would allow to understand the complexity in the immunity modeling techniques and helps to analyze the EMC simulated

results both in time-and frequency-domain.

Based on the experimental measurements on the conducted immunity of the tested ICs, the long-term evolution of the EMR of the DUTs under different accelerated aging tests would be highlighted in the next chapters to investigate the influence of accelerated degradation tests on the conducted EM immunity performance of the ICs by determining the immunity drift against the degradation time induced by both constant and step-stress multiple aging stress factors (i.e., temperature and electrical voltage). The following chapters of the conducted research work presented in this report would also include developing the ICIM-CI models (i.e., PDN and IB) for the ICs under the influence of the defined environmental stress conditions and the accelerated aging tests. Based on the conducted EMC measurements obtained on both the fresh and aged DUTs, the latter chapters of the conducted research study would include proposing and developing the degradation model followed by the predictive reliability model that could be integrated with the ICIM-CI model for addressing aging induced EMC variations with time and predicting the conducted EM immunity performance throughout the lifetime of the tested ICs under both tested and untested conditions.

Chapitre 2

Coupling Simulation and Accelerated Degradation Model for Reliability Estimation of an Analog CMOS Circuit

---

This chapter demonstrates the use of numerical simulation data, depending on the functional behavior of an analog IC voltage regulator, for assessing the reliability performance estimation based on the accelerated degradation test data. The CMOS analog circuit was designed using Cadence Virtuoso software in 180 nm analog-mixed signal (AMS) CMOS technology, and simulated to evaluate its output voltage variations to both temperature and input voltage. The output voltage (V_{out}) degradation data were generated according to environmental parameters (input voltage and temperature) constraints, which makes it possible to define failure thresholds under accelerated conditions, making use of the numerical simulation model along with the proposed degradation model. Degradation path model has been adopted to determine the pseudo failure time under the specified failure criterion (5%). Acceleration law model has then been derived to estimate the reliability model parameters by performing maximum likelihood estimation method not only to analyse but also to predict lifetime data distribution of the regulator under different voltage and temperature stress conditions. The main objectives highlighted in this chapter are as follows :

1. Defining the failure criterion of a regulator chip in accelerated test conditions.
2. Developing the electrical simulation model of an analog regulator chip.
3. Proposing and developing the degradation model from accelerated degradation data.
4. Applying the MLE method to assess the reliability parameters.

2.1 Introduction

Reliability prediction of ICs embedded in electronic components is essential for manufacturers to estimate the functionality and probability of failure while operating under extreme external operational conditions (e.g., high or low temperature, humidity, voltage or current stress). Moreover, advanced reliability model (i.e., Multi-stressor Predictive Reliability Model (M-STORM) needs to be developed and integrated with the ICIM-CI for predicting long-term evolution of EMC on CMOS ICs operating at external environmental constraints [34]. Study of the reliability modelling is generally proposed based on traditional existing standards available in MIL-HDBK-217F [35] and the FIDES standard providing an overview on the methodology to assess reliability of electronic systems. High Temperature Operating Life Test (HTOL) and Low Temperature Operating Life Test (LTOL) standard ageing measurements are usually conducted on ICs to induce and accelerate different types of intrinsic degradation mechanisms [34]. Depending on the ageing stress types (high or low temperature, voltage, and so on), different failure degradation mechanisms are activated in CMOS circuits, which vary charge carrier mobility (μ_{eff}) and V_{th} parameters of the MOS transistors in deep sub-micron CMOS technology depending on ageing stress magnitude and duration [36].

Degradation mechanisms (i.e., NBTI and HCI) degradation mechanisms are activated when HTOL test is conducted on MOS devices under high temperature, electric field and high negative gate bias voltage, while TDDB is observed due to applying low temperature and low drain-source voltage on MOS transistors during LTOL test [32]. In [37], NBTI degradation on VDMOSFET was investigated under external magnetic field that identified formation of paramagnetic defects at the interface between silicon and the oxide layer. In [38], stress-induced NBTI effect was characterized in p-channel power VDMOSFET to investigate V_{th} drift at high temperature stress conditions for predicting the device lifetime reliability by applying different linear extrapolation models to fit experimental degradation data. Previous studies on extracting accurate reliability modelling for ICs have considered multiple failure mechanisms by conducting Multiple Temperature Operating Lifetime (MTOL) method under multiple simultaneous stress conditions [39]. The M-STORM is developed considering different combinations of temperature and voltage stresses applied on Field Programmable Gate Array (FPGA) circuits to accurately evaluate and predict the IC failure rate and TTF under any specified operating conditions [34],[40]. Depending on the multiple stress conditions, the MTOL method enables to dis-

tinguish and identify different failure degradation mechanisms inducing on the CMOS circuits during accelerated ageing tests [31],[41].

In [42], the usage of MTOL testing method was demonstrated to predict Probability of Failure (PoF) and compute the FIT of multiple failure mechanisms for reliability prediction of FPGA devices fabricated on 45 nm and 28 nm CMOS technology. In [43], degradation data generated during measurements was used to develop accurate predictive reliability model by combining FIT of multiple failure mechanisms. The reliability matrix method, which involves predicting failure rates of each different failure mechanisms using corresponding mathematical models, followed by evaluation of accelerated factors were adopted for each failure types based on ageing test data [39]. Hence, the system reliability predicted accurately by the matrix solution method at any operational conditions that were not specified during the ageing test [39],[42]. Failure threshold is generally required for an IC to define the TTF under nominal conditions. However, this criterion is indeed essential for defined accelerated life test conditions. The goal of this section involves conducting reliability study solely based on the development of electrical design model follows by the use of reliability software tools to estimate reliability model parameters.

This chapter is outlined in different following sections. Section 2.2 describes the low droput CMOS adjustable output voltage regulator circuit design in Cadence Virtuoso software using 180 nm CMOS technology as well as discussing the simulation results to analyse both temperature and voltage sensitivity. That section also includes mathematical and curve fitting simulation model to assess the output voltage (V_{out}) for varying combinations of temperature and input voltage variations before degradation. Section 2.3 summarizes methods to produce degradation path model based on generated aged degradation data to compute pseudo lifetime for specified failure threshold criterion. This section also provides the reliability modelling and estimation analysis taking into account the degradation data and pseudo lifetime based on the developed simulation model for accurate prediction of its lifetime parameters under different ageing stress conditions. The main highlights of this chapter along with the concluding contributions of the reliability study are provided in Section 2.4.

2.2 Circuit Design and Simulation

Figure 2.1 shows the internal structure of the designed low dropout voltage regulator using Cadence Virtuoso software in AMS 180 nm technology. It consists of the opera-

tional amplifier (error amplifier), power Metal Oxide Semiconductor Field Effect Transistor (MOSFET), voltage divider circuit formed with resistors ($R0$ and $R1$) and load ($Cload$ and $Rload$). A two-stage cascaded trans-conductance operational amplifier was designed using both p- and n-type MOSFETs with the required aspect ratio width (w)/length (l) to obtain desirable output voltage and current. Power MOSFET (i.e. $TP0$) was designed as a pass element with large aspect ratio (w/l) to drive a high current into the voltage regulator circuit block. The series connected resistive voltage divider circuit acts as a negative feedback for the amplifier to compare the output voltage of the amplifier with the 1.2 V bandgap voltage reference (V_{ref}) value provided at the negative input terminal of the amplifier. The difference between these two voltages is adjusted to obtain V_{out} of the regulator.

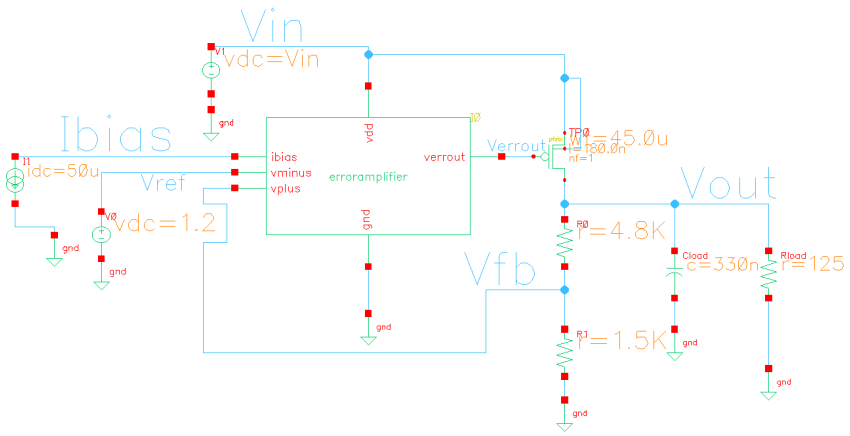


FIGURE 2.1 – Circuit design schematic of the studied regulator.

Table 2.1 provides a list of electronic components with their respective numerical values selected to design the overall circuit test bench of the studied regulator (Figure 2.1). These electrical components, with the specific parameters were selected using the software, were connected with the error amplifier circuit designed with specific combination of n-type and p-type MOSFET at required aspect ratio of width and length to obtain the desired output performance in nominal condition. Notably, one of the voltage sources was used as a supply input voltage (V_{in}) for the internal MOSFETs of the error amplifier circuit block, which could be modified to examine the performance of the designed electrical model under varying thermal and voltage condition.

TABLE 2.1 – External electronic components utilized to design the test bench circuit of the studied regulators

Electrical components	Symbol	Parameters
DC voltage source	vdc	Vin
DC current source	Ibias	50 µA
DC voltage source	Vref	1.2 V
Resistors	R0, R1 & Rload	4.8 kΩ, 1.5 kΩ & 125 Ω
MOSFET	TP0	45 µm/ 180 nm
Capacitor	Cload	330 nF

2.2.1 Simulation results : temperature and voltage sensitivity analysis

The designed electrical circuit was simulated in Spectre to analyse both temperature and voltage sensitivity. The V_{out} variations were monitored for operating temperature between −40 °C and +120 °C, while keeping the input V_{in} unchanged at a nominal value of 7 V. The output voltage increased non-linearly at lower temperature and vice versa. Hence, the regulator was found to be sensitive to temperature variations, with minimal temperature sensitivity of 0.000406 V/°C (Fig 2.2). Voltage sensitivity simulation was conducted by varying V_{in} within a range of 6.5 V to 8 V at constant nominal temperature of 27 °C. Results demonstrated the linear variation of V_{out} for changing V_{in}, with a relatively higher sensitivity of 0.64.

Both the V_{in} and operating temperature were varied simultaneously to observe the combined impact of these parameters on the overall V_{out}. The effect of varying both temperature and V_{in} on the V_{out} is shown in Figure 2.2.

2.2.2 Electrical simulation model

Based on the circuit design model developed in Cadence software, simulation data obtained from the set of curves in Figure 2.2, the output voltage dependency of the regulator on temperature and V_{in} can be modelled mathematically. Non-linear relationship between V_{out} and temperature was observed at constant V_{in}, which can be modelled separately in terms of polynomial function. On the other hand, V_{out} behaves linearly due to changing V_{in} for a fixed temperature, which can also be expressed mathematically.

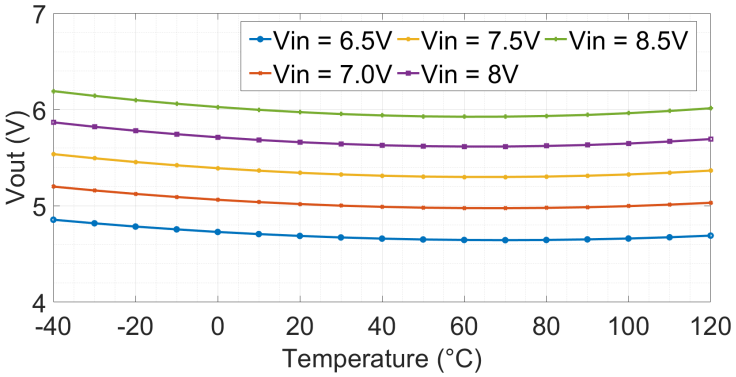


FIGURE 2.2 – Output voltage as a function of temperature and input voltage variation.

Overall, those two mathematical functions can be combined as shown in (2.1), forming a single mathematical simulation model for V_{out} as a function of both dependent variables (temperature and V_{in}), where T and V_{in} represent temperature and input voltage applied to the regulator, respectively. The output characteristics of the proposed electrical simulation model for the regulator was investigated at low input voltage range (6.5 V–8.5 V) along with varying operating temperature between −40 °C and +120 °C for developing the mathematical simulation model provided in (2.1) at degradation time (t = 0), prior to applying accelerated degradation for high aging voltage (12 V and 18 V) and high temperature stress conditions.

$$V_{\text{out}}(T, V_{\text{in}}) = (aT^2 + bT + c)(dT + e)(V_{\text{in}} + e) \tag{2.1}$$

Results in Figure 2.2 were used to demonstrate the best curve fitting polynomial model to determine the constant values of the unknown variables (i.e. a, b, c, d and e). Figure 2.3 illustrates graphically the developed simulation model. The graph in Figure 2.3 displays distribution of simulated data points close to the surface of the polynomial due to applying the best suitable curve fitting modelling technique. As observed, it is possible to obtain the V_{out} at any operating temperature and corresponding V_{in} by substituting known values of curve fitting constants substituted in (2.1). It is worth mentioning that the proposed model is likely to be appropriate for other types of technologies, where the electrical simulation model for the design kit could be developed in other CMOS technology. Note that no further efforts have been carried out in simulation to make the regulator set the

output voltage to 5 V.

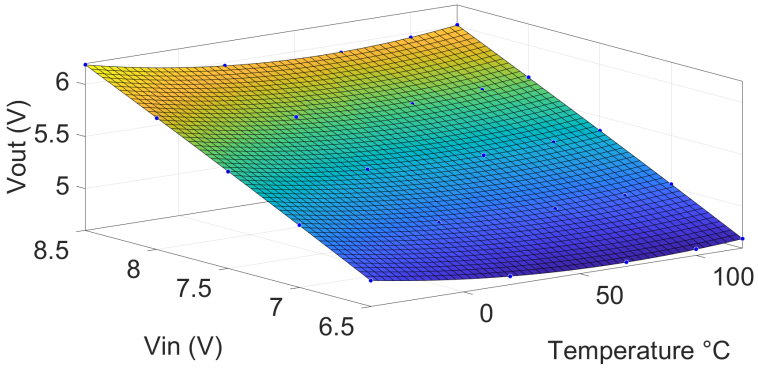


FIGURE 2.3 – Simulation curve fitting model of the output voltage.

2.3 Degradation Path and ALT Modeling

Electrical simulation model for the regulator developed with the aid of schematic design in cadence allowed to obtain simulation data before the aging degradation time. Simulated test data were used to demonstrate the purpose of this methodological approach. The V_{out} degradation data was considered for the total ageing duration of 1000 hours with a span of every 200 hours. Degradation data was generated for the specified ageing stress conditions, which include combination of both different ageing input voltage and temperature stress level at 12 V and 18 V for corresponding temperature stress of 80 °C and 120 °C, respectively. A methodological approach was applied to obtain degradation data at different ageing stress time, based on some specific simulation procedures that have been mentioned as follows :

1. Obtain relevant reliability parameters (i.e. Π_{th}) for the IC regulator using the FIDES predictive reliability analysis standard to compute failure rates (λ) corresponding to different failure modes.
2. Apply the FIDES standard to separately compute the acceleration factors (A_{F_T}) due to temperature stress by defining the Arrhenius law model and A_{F_V} due to voltage stress using the model according to the standard defined for the regulator.
3. Generate failure times at different ageing stress time for different combinations of voltage (12 V and 18 V) and temperature stress (80 °C and 120 °C), while

considering A_{F_T}, A_{F_V} and the Weibull distribution for the degradation process.

4. Define the failure criterion for the regulator to determine the corresponding V_{th} drift from the nominal V_{out} data at specified ageing stress condition.
5. Propose and develop the degradation model in the simulation step and obtain the values of unknown parameters of the model for different combinations of stress levels defined at the initial stage of the simulation procedure. The unknown parameters (γ and D) were evaluated using the simulation test data, while the unknown variable μ was obtained using the computed failure time and V_{th} drift data.
6. Finally, V_{out} degradation data at different stress time intervals was generated from the proposed degradation model with known values of degradation model parameters.

2.3.1 Degradation model estimation

The output voltage as a function of ageing stress time for different temperature and voltage stress is plotted in Figure 2.4. In order to fit sets of voltage degradation data for specified ageing stress conditions, the mathematical degradation model was proposed in (2.2), where V_{out} depends on stress time duration, stress magnitude (V_{in} and T), unknown parameters μ and γ are functions of V_{in} and temperature ($T/°\mathrm{C}$) and unknown coefficient D is linear function of V_{in} and T.

$$V_{\mathrm{out}}(t, V_{\mathrm{in}}, T) = \mu t^{\gamma} + D \tag{2.2}$$

The expression in (2.2) refers to the degradation model for the regulator, indicating how V_{out} link to ageing stress time ($t > 0$) at any specified combination of V_{in} and T. Therefore, equation (2.2) provides an insight to understand the impact of t on V_{out}, with T and V_{in} applied simultaneously. The proposed degradation model might vary, and hence, the acceleration law model might differ for different technology because of different associated failure modes or degradation mechanisms.

Figure 2.4 illustrates four different V_{out} degradation paths were generated for each corresponding different stress level (12 V and 18 V) at different temperatures, which fits the V_{out} degradation data with greater accuracy. Plotting the best fits of the degradation model to the data indicates that the model is adequate for estimating the unknown

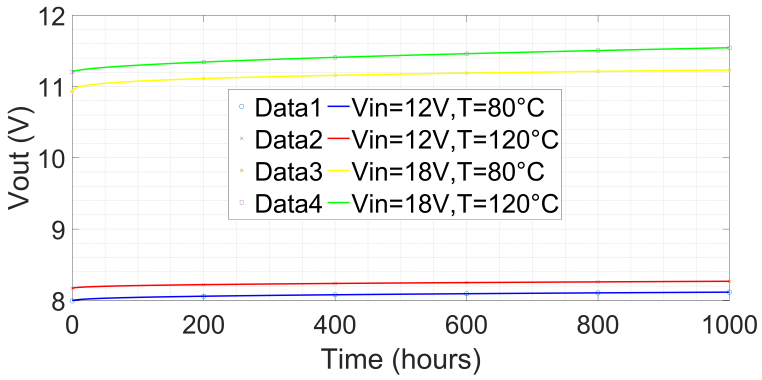


FIGURE 2.4 – Degradation path model fitted to the output voltage data of the regulator at different stress conditions.

parameters (μ, γ and D) of the model. The graph demonstrates that the degradation level increases with stress duration, with more pronounced V_{out} degradation observed for higher stress conditions (18 V and 120 °C). Considering a fixed failure criterion of 5%, corresponding V_{th} was defined as the minimum degraded output voltage above the nominal voltage at which the regulator was considered to fail. The regulator's performance ratings (maximum current and voltage) from the specification mentioned in the datasheet was taken into account, while a fixed failure criterion was chosen with an arbitrary value in order to ensure that the regulator would not undergo into permanent failure mode while assessing its performance degradation throughout the total specified stress duration of 1000 hours. Thus, the TTF was determined at the defined V_{th} for corresponding 5% failure criterion at the specified ageing stress conditions. Interpolating the degradation curve to reach the minimum V_{th} (5% higher than nominal V_{out}) value after degradation would lead to obtain the pseudo failure time. It is also possible to calculate the failure time using the (2.3), after determining unknown parameters of the degradation model.

$$TTF = \left(\frac{V_{\text{th}} - D}{\mu}\right)^{\frac{1}{\gamma}} \tag{2.3}$$

Table 2.2 summarizes the numerical values of the degradation model parameters and failure time computed for each unit of the regulator at different ageing stress conditions. The tabular data for highest applied stress voltage (18 V) and maximum temperature (120 °C) indicates least TTF in hours is needed to reach failure criterion compared to

TABLE 2.2 – Degradation model parameters and TTF under different stress conditions

Parameters	12 V, 80°C	12 V, 120°C	18 V, 80 °C	18 V , 120 °C
μ	0.01	0.045	0.007	0.008
ϒ	0.372	0.285	0.453	0548
D	7.988	10.91	8.132	11.20
TTF/hours	22392	6846	13536	2490

that of other lower ageing stress conditions.

2.4 Reliability Estimation : Life Data Analysis

The relationship between the life−time dependency denoted by L for electronic components and temperature stress only for accelerated life tests can be modeled by applying Arrhenius law as shown in (2.4) [30], where T is the temperature stress, E_A is the activation energy, k refers to the Boltzmann constant and A is the constant that depends on failure criteria, product design and so on.

$$L = A \exp\left(-\frac{E_a}{kT}\right) \tag{2.4}$$

The inverse power relationship can be used to model the life−voltage relationship of electronic components, such as, capacitor, IC, transformer and microelectronic circuits to investigate the effect of voltage as an accelerating stress factor on its L as shown in (2.5) [30], where V is the voltage stress, L is the nominal life, A and B are constants that also depends on component properties, design and failure criteria.

$$L = \frac{A}{{V_{\text{in}}}^B} \tag{2.5}$$

Life data analysis was used to predict the lifetime distribution of the regulator and estimate the required reliability parameters at the applied stress conditions and defined

threshold level. Stress parameters (e.g., voltage and temperature) were applied simultaneously to increase acceleration factor and performance degradation of the regulator. Hence, the L relying on these stress parameters is modelled by combining Arrhenius relationship and inverse power law model for temperature and voltage stress respectively as provided in (2.6), which describes the mathematical modeling relationship between the Life and the combined temperature and voltage stresses discussed in [30].

$$L = \frac{A}{V_{\text{in}}^{B}} \cdot \exp\left(\frac{E_a}{kT}\right) \cdot \exp\left(\frac{C\log(V_{\text{in}})}{kT}\right) \tag{2.6}$$

The expression in (2.6) consist of several unknown parameters, where L is the nominal life that can be represented as characteristic life of the Weibull distribution, A, B and C are the stress dependent constants that depends on failure criterion and product design. Besides the activation energy (Ea) with a value of 0.75 eV is considered for the studied regulator, k corresponds to Boltzmann constant expressed in J/K or eV/°C, and the T refers to the thermal stress denoted by kelvin (K). The relationship between L and both stress parameters (T and V_{in}) is expressed in (2.6), where the last term $C\ln(V_{in})$ or $C\log(V_{in})$ inside the exponential has been provided to indicate that the interaction between T and V_{in} is strongly evident [30]. The resulting expression can be simplified by assuming that this last term is non-existent if significant effect of both T and V_{in} on L is not evident. Consequently, the simplified expression would account for the relationship between L and (T and V_{in}) to be modeled individually or independently by the Arrhenius and inverse power relationship.

MLE method, with the aid of Weibull distributions, was applied using the quantified sets of TTF data under specific threshold and stress conditions, enabled to obtain reliability estimation parameters, including β and η using Weibull++ software [ref15]. The CDF for the Weibull distribution expressed in (2.7), was considered to determine the unknown parameters, where $F(t)$ refers to the probability of failure, β is the shape parameter of the distribution and η is the scale parameter and t is the arbitrary time. The analytical expression provided in (2.8) refers to the generalized log-linear (GLL) that considers the Arrhenius life-stress relationship for temperature stress and inverse power life-stress relationship for voltage stress, where α_0, α_1 and α_2 refers to the GLL-Weibull model parameters and η is represented by the natural logarithm applied on the lifetime data L.

$$F(t) = 1 - \left[\exp\left(-\frac{t}{\eta}\right)\right]^{\beta}, \quad t > 0 \tag{2.7}$$

$$\eta = e^{\alpha_0} e^{\alpha_1(\frac{1}{T})} e^{\alpha_2 \log(V_{\text{in}})} \tag{2.8}$$

It is worth mentioning the difficulty of establishing the direct correspondence between the GLL–Weibull model parameters (i.e., α_0, α_1 and α_2) and stress-parameter constants (i.e., A, B, and C), since (2.6) is not expressed as a generalized log-linear expression, rather it shows the combined life-temperature and voltage stress relationship between L and the simultaneous impact of T and V. The analytical expression for the GLL expression could be derived by applying natural logarithm in (2.6) as shown in (2.9), where $\log L$ refers to the $\log \eta$. The GLL–Weibull model was applied using the Weibull++ software to estimate approximate values of the model parameters (i.e. α_0, α_1 and α_2). The mathematical expressions of these estimated parameters could be derived by considering some assumptions in order to evaluate the unknown A, B and C model constants mentioned in (2.6).

$$\log(L) = \log(A - B\log(V_{\text{in}}) + \frac{E_a + C\log(V_{\text{in}})}{kT}) \tag{2.9}$$

Comparing and equating both (2.9) and (2.8), while considering negligible impact of both V_{in} and T on the L, the A can be computed using (2.12). Both the unknown constants (i.e. B and C) could be determined using the predicted numerical values of α_1 and α_2. The expression in (2.9) can be simplified to obtain (2.10) and (2.11), where X and Y refer to the constant variables that could also be computed using the known values of V_{in}, A and B constants. Note that the (2.10) and (2.11) considered the constant V_{in} and T stress factors, respectively that impacts on the L in nominal conditions.

$$\log L = X + \frac{E_a + C\log(V_{in})}{k} \cdot \frac{1}{T} \tag{2.10}$$
$$\text{where,} \quad X = \log A - B\log(V_{in})$$

$$\log L = Y + \left(\frac{C}{kT} - B\right)\log(V_{in}) \tag{2.11}$$
$$\text{where,} \quad Y = \log A + \frac{E_a}{kT}$$

Thus, (2.13) refers to the mathematical expression for α_1 that is derived by substituting (2.8) in (2.10), while taking into account of the impact of T stress only on the L due to considering constant V_{in} stress in nominal condition (i.e. $V_{in} = 7$ V). Similarly, α_2 is derived from (2.11) as shown in (2.14), considering the influence of V_{in} stress only on the L and assuming negligible influence of T use-stress level in nominal condition (i.e. $T = 298.1$ K) at the defined threshold. Thus, the stress-dependent constants denoted by A, B and C were evaluated using the derived expressions provided in (2.12), (2.13) and (2.14) respectively, with the known values of k, T, V_{in} as well as the estimated α_0, α_1 and α_2 parameters of the GLL–Weibull model in use-level or nominal condition.

$$\alpha_0 = \log(A) \tag{2.12}$$

$$\alpha_1 = \frac{E_a + C\log(V_{in})}{k} \tag{2.13}$$

$$\alpha_2 = \frac{C}{kT} - B \tag{2.14}$$

Table 2.3 provides numerical values of the accelerated life test analysis. These estimated parameters would enable to determine lifetime data for failure under any operating conditions. It shows that the estimated parameters of the developed GLL-Weibull model could be used determine lifetime stress dependent constants mentioned in (2.6). Moreover, the Table 2.3 shows the value of the β parameter is constant and >1 ($\beta > 1$), which means that the regulator degraded with increasing non–constant λ in the wear-out phase demonstrated in the bathtub curve.

The life data (probability of failure) expressed in percentile at corresponding failure time for different stress combinations is plotted in Figure 2.5. The data plotted on the

TABLE 2.3 – Reliability model estimation parameters under different accelerated stress conditions

Parameters	Data (Value)
shape (β)	1.34
scale (η)	7.08E+06
A	5.02E-05
B	-1.13
C	-42.10
α_0	-9.90
α_1	8701.19
α_2	-1.71

logarithmic graph corresponds to the pseudo lifetime (hours) failure on x-axis for different voltage and temperature stress level. Nominal condition refers to the nominal temperature at 25 °C. The parallel lines for the logarithmic fits produced by applying the Weibull distribution display β parameter is independent of voltage and temperature stress, while the scale parameter η is dependent on different stress levels at defined threshold criterion. It is worth to mention that the failure mode remained unchanged for the different stress levels' unreliability curve demonstrated in the Figure 2.5 with an assumption that the β remained unchanged at different stress conditions. Higher lifetime reliability of the regulator was predicted (around 9000 hours at 12 V, 12 °C against 5000 hours at 18 V and 120 °C) for 99% failure probability. The Weibull distribution plot presented in Figure 2.5 allows the linear interpolation of the plotted data to the specified degradation criterion (5% V_{out} drift from nominal value).

The application of Weibull's distribution was found to more suitable for applying linear regression model to best fit the degradation data. The construction of reliability models based on Weibull's distribution has enabled to extract and estimate reliability parameters, including pseudo TTF for different stress conditions only in the wear-out stage of the regulator's bathtub curve. Weibull distribution was considered as one of the most suitable than other statistical distributions (e.g., log-normal, exponential) because of its simplicity, less complexity to develop the reliability model of the studied regulator and has got only one unknown parameter to provide the failure information. This kind of statistical distribution was applied to the degradation behavior of the regulator due to

being more suitable compared to other statistical distributions (i.e., exponential and log-normal) for characterizing both the useful life period and wear–out phase in the bathtub curve of this device. This could be possible by extracting shape parameter value from the Weibull reliability curve plotted against the stress time. However, other types of statistical distribution (i.e., exponential and log-normal) could characterize the TTF data of the device with non-constant increasing failure rate in the wear-out phase of the bathtub curve. The shape parameter β of this distribution allows obtaining valuable information on failure modes or mechanisms at different phases of the bathtub curve. The shape parameter β value is < 1, indicates that the device demonstrates random degradation with constant failure rate λ in the useful phase of the bathtub curve and the component would undergo into hard failure.

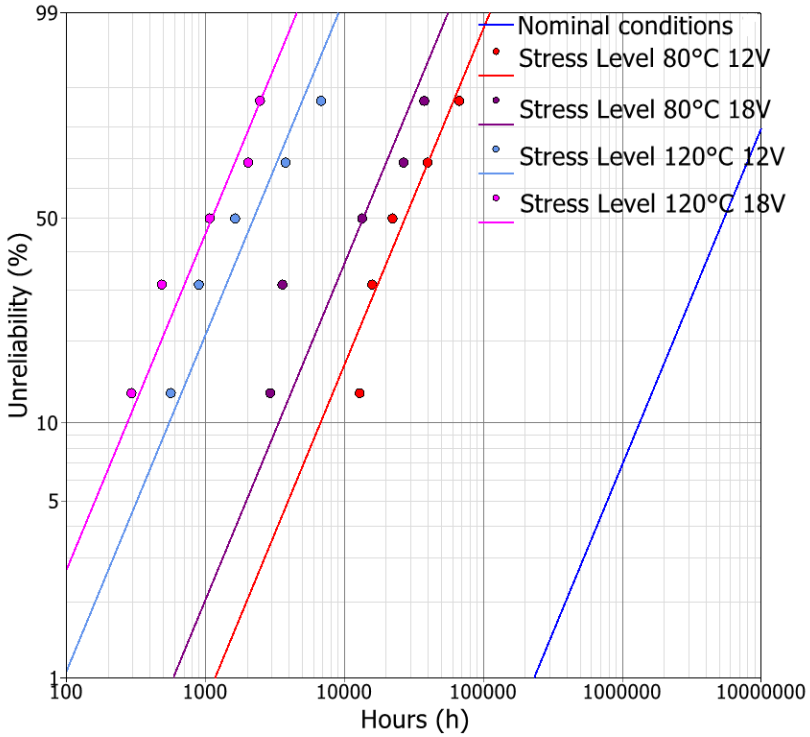


FIGURE 2.5 – Weibull distribution fits to pseudo failure time at different stress conditions.

Data measurements from experiments are usually preferable prior to applying the Weibull distribution or log-normal distribution methods to evaluate or accurately predict reliability parameters (such as, FIT, TTF, AF and IFR) from using the degradation data, when the DUTs are subjected to specified stress conditions. However, the limitation or

the weakest−link property of this type of distributions, lies mostly on the difficulty of computing accurate estimation of reliability parameters, i.e. the pseudo TTF, FIT, PoF and so on, for any untested or undefined accelerated aging stress environmental operating conditions.

2.5 Conclusion

The importance of employing a simulation model of the designed low dropout CMOS adjustable voltage regulator to evaluate the estimation of reliability based on accelerated degradation data has been illustrated in this chapter. The objective was achieved by developing the numerical model for extracting the output voltage as a function of temperature and input voltage. Moreover, a methodological approach was proposed to generate the output voltage degradation data under accelerated conditions based on the knowledge of predictive reliability analysis for the regulator in accordance to the the FIDES standard. The defined failure threshold criterion was extracted at two different voltage and temperature stress conditions to estimate the pseudo failure lifetime from the degradation data. With the use of simulated test data, a suitable acceleration law model was then adopted to predict the reliability parameters of the regulator under accelerated conditions.

It was also shown that the estimated lifetime reliability of the proposed design of the regulator is significantly higher at lower accelerated ageing conditions (around 90,000 hours at 12 V, 80 °C against 5000 hours at 18 V, 120 °C) for 99% failure probability. Hence, the regulator was found to have significantly higher pseudo TTF, depending on the magnitude of ageing stress type (voltage and temperature) conditions.

Developing accurate degradation path model under HALT conditions would enable to produce improved reliability model for estimating the lifetime failure probability of IC components while operating under specified ALT conditions. The perspective of the presented study would involve conducting the accelerated ageing life tests and the measurement ALT results would be utilized for statistical analysis prior to developing an accurate reliability model to predict EMC performance of the regulator, and integrate the impact of ageing tests to develop the ICIM-CI model of the commercially available regulator ICs from different manufacturers. These research studies have been provided in next chapters.

Chapitre 3

Conducted Immunity Evaluation of Analog ICs Integrating Obsolescence and Temperature Stress in Long Lifespan Systems

---

This chapter compares the EMC performance of three different voltage regulator ICs (i.e., UA78L05, L78L05 and MC78L05) developed by three different manufacturers, with similar functionality and pin compatibility, under the influence of low and high temperature stress conditions (i.e., −30 °C and +100 °C). The DPI conducted immunity test was performed on these ICs to analyze the impact of applying thermal stress on the conducted immunity to the injection of single-tone RF disturbance signal. The DPI immunity parameters were measured and recorded in real-time for an incident amplified power, while the ICs were exposed to low and high thermal stress conditions. It was demonstrated that the minimum injected power required to reach the defined failure voltage threshold criterion (±4%) varied over a certain frequency range depending on the ICs. Moreover, these functionally identical ICs showed significant evolution of their conducted immunity in all the considered temperatures, depending on their manufacturer. Input impedance curves were monitored at low, high and nominal temperature, showing noticeable decline of impedance at high frequency. Moreover, the equivalent *RLC* values of the lumped elements (i.e., resistor, inductor and capacitor) were extracted and compared at these aforementioned temperature conditions to model the PDN impedance for the selected ICs. The immunity behaviour of these ICs was further investigated by generating look up table data from the DPI measurements. The major findings of the conducted experimental study are mentioned as follows :

1. A DPI test was conducted on three pin compatible functionally identical voltage regulator ICs under nominal conditions, manufactured by three different compa-

nies, demonstrating significant variations in the conducted immunity in different frequency ranges.

2. The impact of exposing those ICs to low and high temperatures was found to alter the conducted immunity characterized during the DPI measurement, with the aim to investigate the combined effect of obsolescence (or second-source) management and thermal stress.
3. Whatever the IC manufacturers, the DPI characterization results conducted at nominal, extreme low and high thermal stress conditions, revealed a higher immunity of those ICs in extreme temperatures, with marginal difference in magnitude of the minimum injected power (below +5 dB) in high frequency (above 700 MHz).
4. The PDN model developed for the considered ICs demonstrated limited information to determine the immunity of the ICs, and the need for an IB block was shown to be necessary.

3.1 Introduction

IC manufacturers face key challenges on assessing and analyzing obsolescence (or second-source) related to the EMC performance of an IC under the influence of the thermal stress conditions. The term "obsolescence" refers to replacing an IC developed by a manufacturer with another functionally identical or pin-to-pin compatible IC (i.e., second-source) of another manufacturer based on the conducted immunity characterized by conducting different types of EMC performance evaluation measurement techniques (i.e., DPI, EFT and so on) experimental tests under the specified low and high external thermal stress conditions. The evolution of the EMC behavior of an IC subjected to external temperature stresses should be taken into consideration to ensure proper functionality and EMC compliance during the obsolescence management within the life-cycle of that product. Voltage regulator ICs, which are ubiquitous in almost any electronic application, are likely to be sensitive to EMI [3]. The conducted immunity of these ICs to EMI can be evaluated by performing testing methods according to the defined EMC standards. DPI is considered a suitable method to characterize the immunity of ICs with respect to unmodulated RF sinusoidal signals [44]. According to the IEC 62132-4 standard [16], the DPI test is carried out by injecting single-tone signal disturbances up to 1 GHz into the IC pin in order to record the forward power causing IC failure or malfunction as a function of frequency [45].

Previous research works published on the immunity of low-dropout voltage (LDO) regulator circuits mainly focused on developing a conducted immunity model to predict their EMC performance and validate the developed model by comparing with DPI measurements. In [18], an immunity modeling methodology, compliant with the ICIM-CI standard [46], was proposed for an entire LDO voltage regulator circuit. In [20], a multiport modeling methodology based on ICIM-CI was proposed and implemented for predicting the conducted immunity of a micro-power voltage bandgap (i.e., LTC1798–2.5) circuit. The proposed model was simulated and the results were compared with the DPI and S-parameter measurements to validate the accuracy of the model. In [47], an on-chip voltage sensor was introduced inside the regulator IC to measure DPI immunity results, and demonstrated the construction of an accurate electrical simulation model based on both off-chip and on-chip measurement data, together with the internal circuit information of the regulator. Figure 3.1 illustrates the overall block diagram of the visual summary presented in this chapter, including the temperature-controlled thermal chamber to illustrate that the studied ICs placed inside this chamber was subjected to both low and high thermal stress conditions, while simultaneously conducting the DPI experiment on each of the three considered ICs, separately. Moreover, few additional information (i.e., PDN and IB) have been mentioned to highlight that both the PDN and the IB models have been developed as part of the ICIM-CI model for evaluating the conducted immunity of these considered analog ICs under the influence of environmental stress conditions.

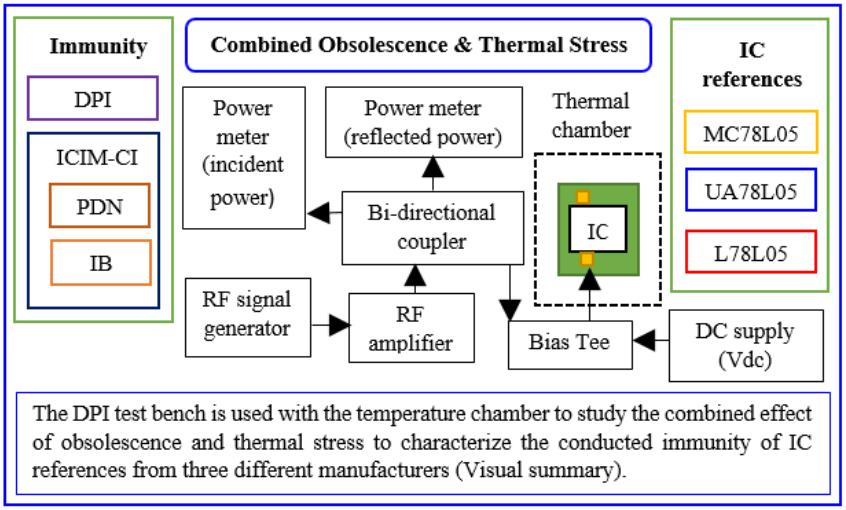


FIGURE 3.1 – Visual representation of the research study.

External thermal stress factors, such as temperature and humidity, can affect the EMC robustness of ICs throughout their entire lifetime. In [48], the reliability parameters determined from the coupling of the developed simulation and acceleration model for the designed voltage regulator could be compared with the accelerated life test results. Previous research studies intended to address the impact of electrical stress on the evolution of conducted immunity of electronic components [3]. The latter was investigated in [49] for the low-dropout voltage regulator to understand the link between its EMC performance evolution and electrical characteristics. However, combining the simultaneous evolution of conducted immunity as functions of obsolescence and environmental thermal stress has not been yet been explored. This chapter aims to investigate the impact of applying thermal stress conditions (i.e., temperature) on the EMC performance of three functionally identical regulator ICs from different manufacturers, in order to come to a sensible envelope of the conducted immunity of those ICs at different temperatures, when considering component changes due to obsolescence, or second-sources.

Considering the study presented in this chapter, the term "obsolescence" has been used to focus in the context of a system obsolescence instead of only on IC obsolescence,where the term "obsolescence" refers to the possible replacement of an IC within a system by another functionally identical and pin-compatible IC of another manufacturer with different EMC behavior under the influence of external environmental characteristics (i.e., temperature). This chapter is divided into the following sections as listed below. Section 3.2 describes the experimental procedures for performing the DPI test to characterize the conducted immunity on selected ICs from various manufacturers under various thermal stress conditions. Section 3.3 investigates the effect of thermal stress (high and low) temperatures on the conducted immunity of the selected DUT. Section 3.4 presents the development and construction of the ICIM-CI model of the tested sample under the influence of external environmental conditions, as well as a comparative analysis of both the developed PDN and IB blocks. Section 3.5 concludes the findings of the conducted immunity study performed on the tested ICs of different manufacturers to investigate the combined impact of obsolescence and thermal conditions.

3.2 Materials and Methodology

This section addresses the functionality of the voltage regulator ICs as well as the specific DPI test setup used to perform conducted immunity tests under the thermal stress

on three functionally identical and pin-to-pin compatible voltage regulator ICs developed by three different manufacturers.

3.2.1 Devices under test

Three different types of commercially available voltage regulator IC fabricated by three different manufacturers, with comparable pin configurations, similar packaging and identical functionality (i.e., output voltage V_{out} of +5 V), were chosen for the purpose of the study to compare conducted immunity level in continuous wave (CW) mode by conducting DPI experiment. Those selected ICs with corresponding part or model (i.e., UA78L05, L78L05 and MC78L05) are manufactured by Texas Instruments, STMicroelectronics and On-Semiconductor, respectively.

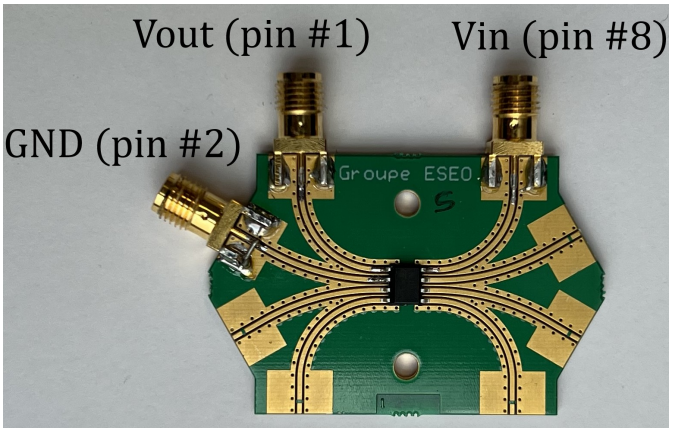


FIGURE 3.2 – Voltage regulator IC mounted on a custom DPI test board.

Figure 3.2 shows one of the tested regulator ICs mounted on a generic SOIC8 extraction test board designed in [50]. The 4-layer FR4 PCB design consists of a ground plane for providing ground reference with minimum impedance, short traces with identical length from pads to the board edge connectors to ensure low power loss and low crosstalk during immunity testing of the IC. The following IC pins, i.e., output voltage (pin 1), input voltage (pin 8) and ground (pin 2), were soldered on the PCB traces and SMA connectors were fitted onto the pads corresponding to these pins under test (PUT). Note that, although the internal connections are the same for all those ICs where other grounded pins were internally connected, pins 3, 6 and 7 are not connected to the PCB ground for the ease of experiments, which makes the connection between the die and the

PCB ground more resistive and inductive, the main objective being the comparison of the thermal stress impact on the conducted immunity of those ICs. It can be noted that internal connections are the same for all those ICs, thus making the comparison sensible. The generic SOIC8 extraction test board design was preferred for the DPI experiment, considering the IC DUT has also got the same package, which is also frequently used in ICs for automotive applications.

The functionally identical regulator ICs with exactly similar operational parameters were selected to assess potential obsolescence related EMC issues. Those regulator ICs provide an output voltage of +5 V with an average output current of around 40 mA when a minimum of +7 V input voltage is applied, and can operate within a wide temperature range (i.e., between −40 °C and +120 °C). Note that nominal values are the same for all manufacturers.

3.2.2 Experimental setup

The DPI test bench setup is used with the temperature chamber to investigate the combined effect of obsolescence and temperature stress by evaluating the conducted immunity of the selected ICs (Figure 3.1). It consists of a RF signal generator to generate the RF signals with desired power level in the considered frequency range (i.e., 10 MHz−1 GHz with 10 MHz step), a +43 dB gain RF power amplifier with bi-directional coupler, and a wideband external bias tee. The sinusoidal voltage waveform with a single-tone frequency that is electromagnetic radio wave in nature with a constant frequency (ranging between hundred and thousands of MHz range) could be generated by a RF generator. The purpose of producing the RF signal is to ensure conducted coupling of the EMI on a specific IC pin for dealing with obsolescence management related to the EMC issues of an IC due to the injection of the analog RF signal disturbance under the influence of external thermal stress conditions.

The incident power at the output of amplifier was varied from +3 to +33 dBm before injecting into the DUT V_{in} pin. The bi-directional coupler is connected to a power meter to measure both the incident power of the amplified RF signals and the reflected power. The bias tee (ZX85-12G-S+), which is used to provide an injection path for the RF signal to couple into the IC pin, includes the coupling capacitor and inductor in a certain configuration such that one end of the inductor is connected to the DC power supply (+12 V) and the other end to the capacitor. Due to its wide bandwidth extending up to 30 GHz, the PCB has a constant impedance over the injection frequency range. Moreover,

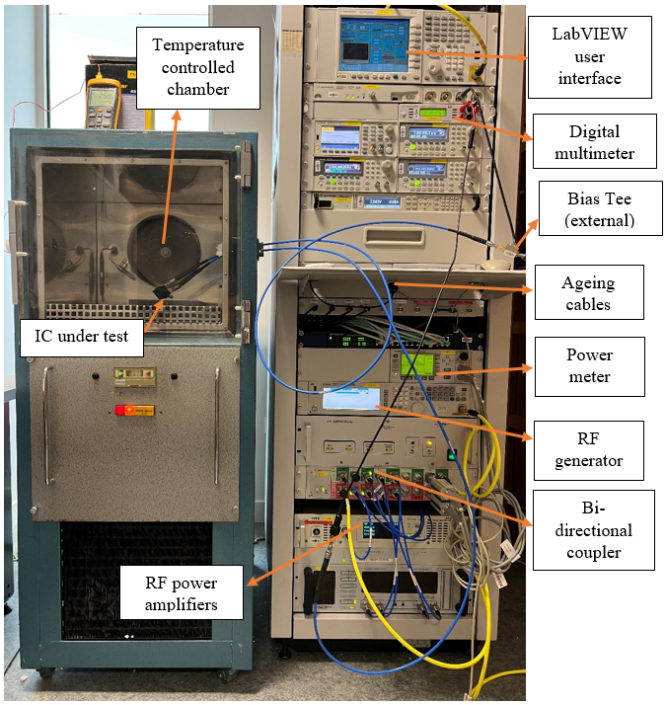


FIGURE 3.3 – DPI test bench setup with temperature controlled chamber.

this wideband bias tee used for the DPI experiment has a low insertion loss of +0.6 dB in nominal condition and high current capacity of 400 mA. Hence, the output of the bias tee provides the RF disturbance signal coupled to the DC analog voltage signal, which is injected into the DC power supply V_{in} pin of the regulator IC. The corresponding DC V_{out} at the IC pin 1 caused by this disturbance is monitored from pin 1 using a digital oscilloscope. A ±4% criterion on the DC V_{out} was considered for positive or negative DPI failure modes. Positive failure mode could be indicated when the positive deviation of +0.2 V (+4%) from the nominal DC output is observed at each DPI frequency values and negative failure mode could be resulted due to the −0.2 V (−4%) variation from the nominal DC output.

Figure 3.3 shows the DPI test bench setup for performing conducted immunity experiments at both considered low and high temperatures. The DPI test was conducted in accordance to the IEC 62132-4 standard [16]. The RF source was stepped across the frequency range between 10 MHz and 1000 MHz. The step size of the generated RF signal was varied linearly at 10 MHz across the entire frequency range to ensure EMC compliance in according to the IEC standard [16]. The temperature controlled chamber

is used to maintain nominal conditions (+25 °C) or a constant thermal stress (−30 °C and +100 °C) environment. During the DPI experiment, the ICs are placed inside the chamber, and all DPI parameters (i.e., forward power, reflected power, injected power, and frequency) responsible for causing failure are measured and recorded in real-time under all the three aforementioned conditions. Note that, the cables connected with the SMA connectors of the PCB were chosen to withstand extreme high and low temperature [51].

Since the aim is to assess the conducted immunity performance of the tested DUTs under different thermal stress conditions, the numerical data presented in the immunity curves (i.e., Figures 3.4 to 3.6) indicate injected power at the DUTs pin measured against each corresponding, when the DUTs have exceeded the defined failure threshold or immunity criterion (±4%). Hence, presenting the injected power data seemed a more logical approach to achieve the objective of the study presented in this chapter. The algorithm used for conducting the DPI immunity test has been programmed to measure and extract forward power, reflected power and the minimum injected power at each corresponding frequency causing the DPI failure, depending on the immunity or failure threshold defined at the start of the DPI experiment. The conducted immunity curves (i.e., Figures 3.4 to 3.6) indicate injected power at the DUTs pin measured against each corresponding frequency, when the DUTs have exceeded the defined DPI immunity failure threshold criterion.

3.3 Results and Findings

This section presents the experimental characterization on the conducted immunity due to applying RF signal disturbance on the IC V_{in} supply (pin 8) in nominal and thermal stress conditions. The goal is to compare and highlight the impact of applying extreme thermal stress conditions on the conducted immunity of three different functionally identical IC references manufactured by different manufacturers.

3.3.1 Conducted immunity of ICs under nominal conditions

Every IC was tested with an RF signal coupled to the V_{in} (pin 8) under nominal conditions. Figure 3.4 shows the minimum power injected to the V_{in} pin of the tested ICs (i.e., UA78L05, L78L05 and MC78L05) causing a DPI failure at different frequencies. The immunity profile of the tested ICs demonstrated significant deviation of the injected

power throughout the entire frequency range. A comparative study highlighted that the V_{in} pin of L78L05 is the most immune to RF disturbances up to 150 MHz. This study was conducted to compare and assess the immunity profile of these ICs, subjected to both nominal and external thermal stresses. Conversely, the V_{in} pin of MC78L05 was found to be more immune between 300 MHz and 1000 MHz compared to the other two ICs (i.e., UA78L05 and L78L05). Moreover, the DPI immunity profile curve of MC78L05 shows that the measured injected power reached at its peak (i.e., beyond +30 dBm) at 930 MHz, which means this IC could withstand highest injected power causing the DPI failure.

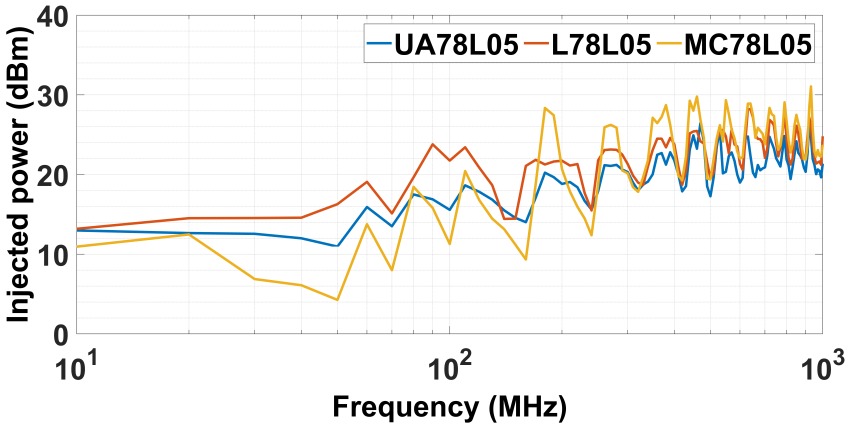


FIGURE 3.4 – Incident RF power as a function of frequency at +25 °C.

3.3.2 Conducted immunity of ICs under thermal stress conditions

Experiments were performed on the regulator ICs to investigate the influence of temperature extrema (i.e., −30 °C and +100 °C) on the conducted immunity of the V_{in} pin. The different ICs were first exposed to a temperature stress of −30 °C. Figure 3.5 compares the impact of the low thermal stress on the three ICs. The MC78L05 was found to be less immune in the low frequency range (from 10–70 MHz). However, this IC was found to be robust and immune to RF disturbances both in the middle and high frequency ranges (from 200–800 MHz). This is because the measured injected power was higher at both high and low immunity points in almost all the corresponding frequency values, except at 550 MHz and 400–450 MHz. Moreover, applying low thermal stress on the UA78L05

resulted to improve the immunity to RF perturbations at low frequency (i.e., +21.6 dBm against +18 dBm at 100 MHz). However, the MC78L05 was found to be more immune than the other two tested IC samples in higher frequency range (i.e., 700-1000 MHz).

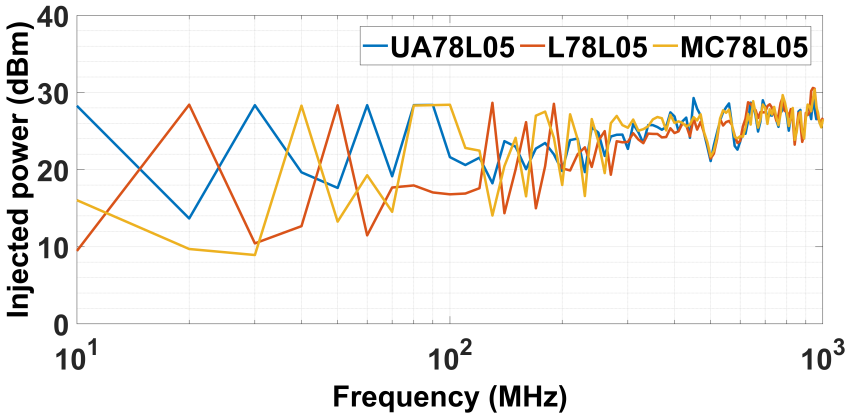


FIGURE 3.5 – Incident RF power as a function of frequency at −30 °C.

A similar experimental approach was then followed under the influence of high temperature stress. The recorded injected power to the V_{in} pin of different ICs at different RF signal frequency is plotted in Figure 3.6. Under the influence of high temperature stress, when compared to that of L78L05 and UA78L05 ICs, the V_{in} pin of the MC78L05 showed a significant decrease in immunity to the RF disturbance throughout the entire frequency range.

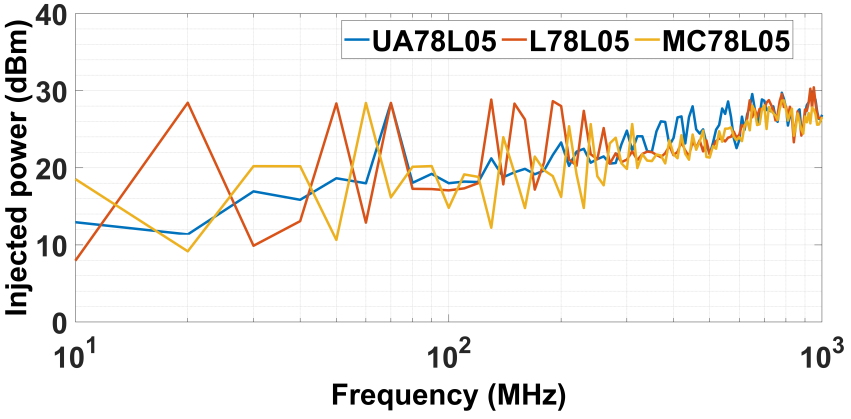


FIGURE 3.6 – Incident RF power as a function of frequency at +100 °C.

The following observations based on the results of the immunity curves displayed in

Figures. 3.5 and 3.6 can be made :

1. Within a specific frequency range, each of the selected DUTs demonstrated higher DPI immunity both at the low and high temperature stresses when comparing to that of under nominal condition. UA78L05 showed higher immunity both at low and high thermal stress condition throughout the entire frequency range between 10 and 1000 MHz, except at few frequencies (i.e., 20 MHz, 110 MHz and 280 MHz). Between 600 MHz and 1000 MHz, the DPI immunity of L78L05 was found to be greater at both low and high thermal stress scenario. MC78L05 demonstrated higher conducted immunity both at low and high thermal stress conditions than that of nominal condition between 10 MHz and 170 MHz, excluding only few frequency values (i.e., 20 MHz and 110 MHz). These aforementioned observations could also be exhibited and validated by plotting the immunity curves at different thermal stress conditions on the same axes for the tested DUT references (i.e., UA78L05, L78L05 and MC78L05).
2. Under the influence of low and high thermal stresses applied only on the tested IC samples, the V_{in} pin of all ICs demonstrated higher immunity in the upper frequency range (i.e., 700−1000 MHz).
3. All ICs were found to be more immune at low thermal stress than at high thermal stress condition.
4. The reason for observing higher DPI immunity both at low and high temperature stress condition could be more likely due to activating and accelerating degradation mechanisms. At high temperature stress condition, negative bias temperature instability failure mechanism would likely accelerate during the DPI measurements. Hence, the increase in threshold voltage and reduction of charge carrier mobility of transistors might be responsible for the significant variation in the DPI behavior of the ICs. This corroborates the results observed in [32] for different ICs.
5. Figures 3.7, 3.8 and 3.9 demonstrate the effect of applying lowest and greatest thermal stress conditions on the studied ICs (i.e.„ UA78L05, MC78L05, and L78L05). When compared to the nominal temperature, it was discovered that higher injected power was required at −30°C than at +100°C for all of the studied ICs. As a result, the conducted immunity behavior of these evaluated DUTs improved at low thermal stress compared to high thermal stress.

Figure 3.10 shows the minimum power injected into the V_{in} pin which induces a fai-

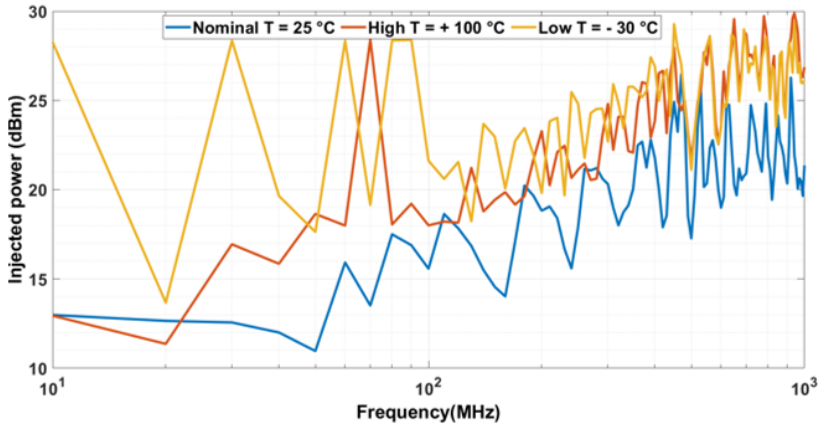


FIGURE 3.7 – Conducted immunity of UA78L05 as a function of different thermal stress conditions.

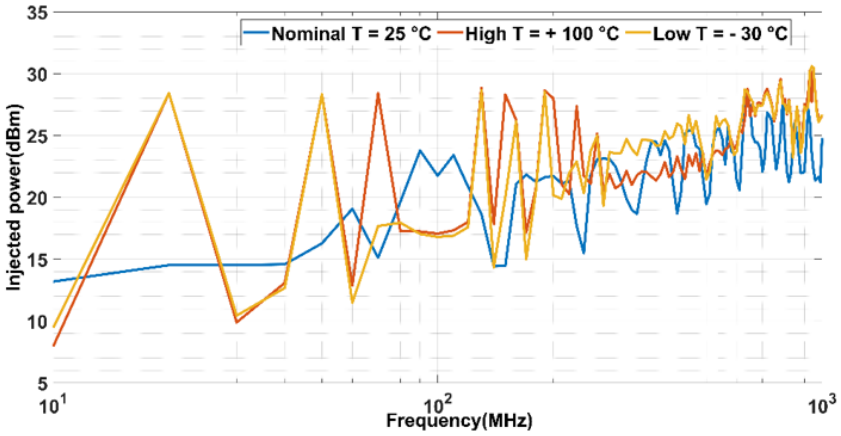


FIGURE 3.8 – Conducted immunity of L78L05 as a function of different thermal stress conditions.

lure in all three temperature conditions regardless of the manufacturers. As can be seen, except below 25 MHz, the immunity seems to be lower in nominal temperature conditions than in both extreme temperatures. Moreover, above 200 MHz, a low temperature stress increases immunity compared to the other conditions. However, even if immunity tends to increase with frequency in all temperature conditions, there are significant differences among the considered ICs (up to +20 dBm at 20 MHz and below 50 MHz for high and low temperatures, respectively). This highlights the need for characterization of second source ICs in obsolescence studies. This is because even though the considered IC sample functionality is taken into account according to the specification provided by the manufacturer,

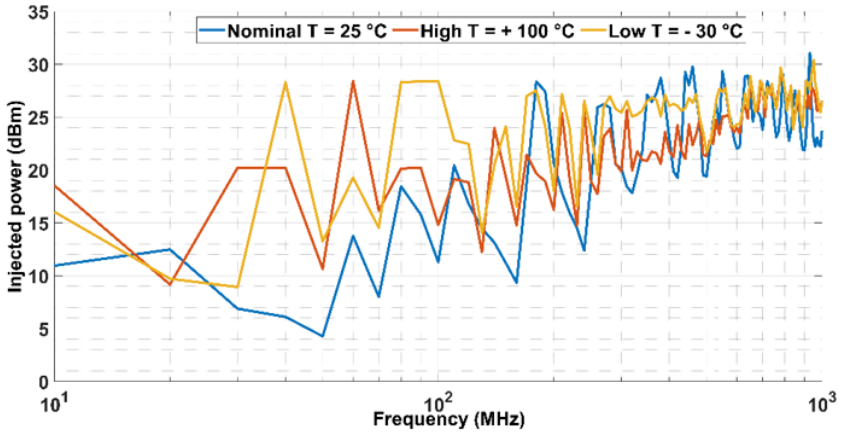


FIGURE 3.9 – Conducted immunity of MC78L05 as a function of different thermal stress conditions.

the EMC performance analysis of the IC and its EMC specification for any application is not provided in the datasheet. Hence, this unavailability of the necessary EMC data could made it difficult to conclude that the whole EMC performance of a system is independent from the EMC behavior of all ICs in that system.

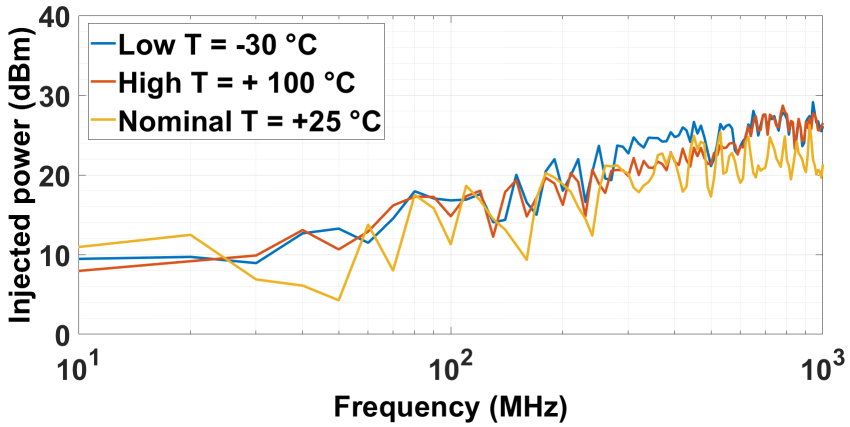


FIGURE 3.10 – Minimum immunity of the three regulators under the considered thermal stresses.

3.4 S-parameter Measurement and Impedance Extraction

In order to verify the obsolescence of the selected ICs and explain possible reasons for significant variations on the EMC performance obtained under nominal conditions, S-parameters were measured using VNA at nominal temperature to extract the corresponding input impedance observed at the V_{in} (pin 8). The equivalent input Impedance (Z_{11}) of these ICs were also compared at both lowest and highest temperature (Figure 3.11). The reflection coefficient denoted by S_{11} parameter was directly measured using the VNA equipment. This measured data was then converted to the Z_{11} using the mathematical expression expressed in equation (3.1), where S_{11} refers to the reflection coefficient measured in decibel (dB) unit and Z_0 refers to the characteristic impedance whose magnitude is 50 Ω [52].

$$Z_{11} = Z_0 \cdot \frac{1 + |(S_{11})|}{1 - |(S_{11})|} \tag{3.1}$$

Figure 3.11a shows the Z_{11} curves observed at the V_{in} pin extracted from the S_{11} parameter. A resonance is observed above 400 MHz for both MC78L05 and L78L05 as the Z_{11} curves follows a decreasing trend, reaching the minimum magnitude of the Z_{11} beyond the aforementioned frequency value. However, the UA78L05 showed resonance at around 350 MHz with relatively higher impedance compared to that of MC78L05. The PDN model of these IC consists of resistance (R), package inductance (L) and on-chip capacitance (C) between the V_{in} and ground pins of these ICs [8]. Due to the presence of the wideband bias tee, the interaction with on-chip PDN model is expected to occur at frequencies above the tested DPI frequency range.

Note that, the Z_{11} curves in Figure 3.11 were produced using the measured data obtained from the VNA instrument, which was configured with logarithmic frequency steps. Hence, those Z_{11} curves of the tested ICs at different thermal conditions appears to be smooth compare to that of the Figures 3.4 to 3.6, which was produced in the linear frequency steps using the measurement data in accordance to the DPI measurement test standard. Moreover, it is also worth mentioning that the resonant behavior which has been visible in those Z_{11} plots might not be clearly evident in the observed power injected plots (Figures 3.4 to 3.6), which was due to the fact that the reflected power at the resonance,

having the input impedance magnitude of 20 Ω, did not differ from that observed at frequencies with the impedance magnitude of 80 Ω. Therefore, the observed resonance was not related to the input power plots.

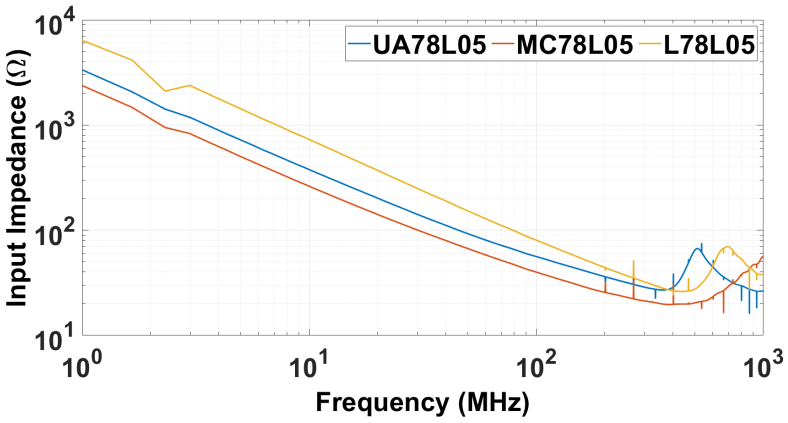
The equivalent R, L and C values of the PDN model for each individual IC can be extracted analytically from the corresponding Z_{11} profile curve. The equivalent RLC values required for the PDN block could be extracted graphically using Figure 3.11. The mathematical expression for extracting the L value is provided in (3.2), where Z_L corresponds to the magnitude of the Z_{11} at the frequency denoted by f_L. This mathematical expression has been considered based on the theoretical conception that the parasitic L could be obtained from the Z_{11} curve at the high frequency range, beyond the resonant frequency (f_r) due to the fact that the L plays a dominating role contributing to the overall equivalent Z_{11} [52]. Hence, L could be extracted graphically by determining the Z_L magnitude corresponding to the f_L at the high frequency region of the Z_{11} curves demonstrated in the Figure 3.11, where the Z_{11} magnitude at the y-axis of the curve increases at the rate of +20 dB/decade.

$$L = \frac{Z_L}{2\pi f_L} \tag{3.2}$$

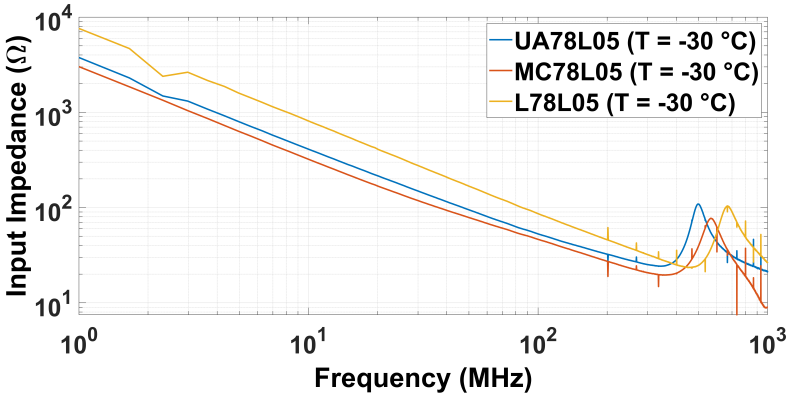
$$C = \frac{1}{Z_c \cdot (2\pi f_c)} \tag{3.3}$$

However, the equivalent C could be derived from the Z_{11} curve at low frequencies below f_r. The mathematical equation to extract C is depicted in (3.3), where Z_c corresponds to the magnitude of Z_{11} at a lower frequency f_c than f_r. Hence, the equivalent C could be extracted from the Figure 3.11 at the low frequency region, where the Z_{11} magnitude decreases by −20 dB/decade. Determining the magnitude of C at low frequencies is necessary because C is a significant contributor to the overall Z_{11} obtained between the V_{in} and the GND (pin2) of the tested ICs. The equivalent R required to develop the PDN model of the tested ICs was extracted from the Figure 3.11. Figures 3.11a to 3.11c show that the Z_{11} magnitude is minimum at the f_r. Hence, the R correspond to the minimum Z_{11} at the corresponding f_r in Figure 3.11.

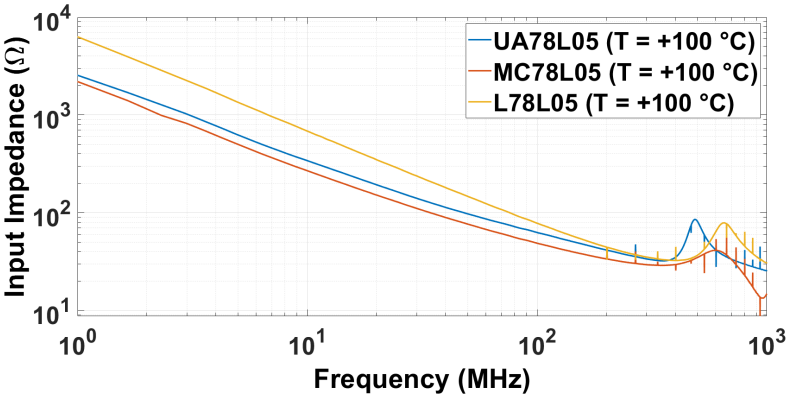
Table 3.1 compares the equivalent RLC values extracted for the PDN models of the selected ICs at low, nominal and high temperature. Those equivalent RLC values were ex-



(a)



(b)



(c)

FIGURE 3.11 – Input impedance of the tested ICs at different temperatures : (a) +25 °C ; (b) −30 °C ; (c) +100 °C.

tracted using (3.2) and (3.3), depending on the required parameters obtained graphically by taking into account of the Figure 3.11. At the nominal temperature (i.e., T = +25 °C), the smallest equivalent capacitance for the L78L05 causes lower internal decoupling at low frequencies compared to the other two MC78L05 and UA78L05 ICs. However, the L78L05 shows more immunity to RF disturbances in low frequency (Figure 3.4), which means that the IB of the active part of the chip should be also considered for a proper evaluation of the IC's immunity. Besides, the package inductance values for the input voltage pin of UA78L05 was found to be higher by 135% and 31.1% compared to that of the MC78L05 and L78L05, respectively, which mainly results in obtaining high input impedance in high frequency. The MC78L05 has the lowest inductance and the highest capacitance at the nominal temperature. Hence, it can be concluded that it is likely to have a larger die, a higher minimum gate length and a smaller bond wire length compared to UA78L05 and L78L05. Likewise, the UA78L05 is not the most immune in high frequency thus requesting a further analysis of the IB model.

TABLE 3.1 – PDN Model Extraction for the Considered ICs as a Function of Temperature

Temperature (T)	**T = -30 °C**			**T = +25 °C**			**T = +100 °C**		
IC reference	**R (Ω)**	**L (µH)**	**C (pF)**	**R (Ω)**	**L (µH)**	**C (pF)**	**R (Ω)**	**L (µH)**	**C (pF)**
UA78L05	24.3	20.3	38.7	27.1	15.6	42.1	32.1	21.01	46.5
MC78L05	19.5	13.8	49.4	19.7	6.63	60.6	28.9	11.1	59.0
L78L05	23.1	13.6	19.6	27.3	11.9	21.8	32.9	15.6	23.3

The transmitted power was further used to assess the IB block table. The IB model information presented in the form of look-up table is considered a valid criterion to validate the EMC performance of these ICs. Table 3.2 compares the threshold actual transmitted power (P_t) among the selected ICs at nominal temperature for different frequencies ranging from 100 to 1000 MHz. The P_t to the IB block was evaluated as accurately as possible using the DPI and S_{11} measurements, while taking into consideration of the power loss (P_{loss}) due to the DPI injection path (i.e., bias tee, coupling capacitor, cable and PCB trace). The mathematical relationship between the P_t and the injected power to the V_{in} pin of the tested IC denoted by P_{inj} is expressed in equation (3.4).

$$P_t = (1 - |S_{11}|^2) \cdot (P_{\text{inj}} - P_{\text{loss}}) \tag{3.4}$$

Results provided in Table 3.2 shows that P_t is the lowest for the UA78L05 within the considered frequency except at 100 MHz, which validates that the UA78L05 is the least immune to the RF disturbances in that range. However, the L78L05, despite having lower inductance and capacitance values in its PDN, is found to have higher P_t than the UA78L05. This clearly demonstrates that the PDN is not the only block determining the immunity of the whole IC, and that the IB plays an important role. Besides, the MC78L05, with the smallest inductance value, was found to have the highest P_t causing a failure above 200 MHz. Therefore, the IB block determined at the nominal temperature plays significant role to figure out origin of the IC's immunity to the RF disturbances.

TABLE 3.2 – IB Look up Table for Tested ICs at Nominal Temperature

IC reference	UA78L05	MC78L05	L78L05
frequency (MHz)	Transmitted power (dBm)	Transmitted power (dBm)	Transmitted power (dBm)
100	7.45	3.28	10.76
150	6.88	3.44	4.81
200	11.3	13.0	12.78
250	10.51	11.2	13.29
300	13.02	12.75	13.18
350	12.91	19.83	15.24
400	14.91	15.96	16.32
450	18.41	21.29	18.3
500	11.11	13.06	12.78
550	14.24	23.27	18.48
600	12.26	15.64	15.28
650	12.59	20.37	20.99
700	12.66	16.33	15.31
750	13.62	17.14	16.4
800	13.48	19.23	16.53
850	15.93	20.17	17.98
900	12.32	14.76	14.09
950	13.46	16.05	14.41
1000	13.88	17.09	17.26

In order to investigate the impact of both extreme low and high temperatures on the PDN model of the selected ICs, in terms of their equivalent RLC values, the input impedance curves were computed from the S-parameters measurements as shown in Figures 3.11b and 3.11c, respectively. Figure 3.11b depicts that the Z_{11} of the ICs increase in low frequency at the lowest temperature compared to those at the nominal temperature. Besides, the magnitude of the Z_{11} of these ICs is found to be lower in high frequency at the highest temperature. Moreover, the Z_{11} curves showed similar decreasing trend throughout the entire frequency range as shown in Figures 3.11b and 3.11c, respectively. The equivalent RLC values extracted at the low and high temperature from the corres-

ponding input impedance curves were found to be comparable and varied considerably as shown in Table 3.1. Based on the Z_{11} curves plotted at −30 °C and +100 °C, the computed inductance values of UA78L05, MC78L05 and L78L05 increased considerably from its nominal value by 30.1%, 108.1% and 14.3% at −30 °C, respectively. Besides, the inductance values evaluated at +100 °C was also incremented for UA78L05, MC78L05 and L78L05 by 34.7%, 67.4% and 31.1%, respectively.

The overall equivalent resistance R values computed from the Z_{11} profile at −30 °C were declined from its nominal value by 10.3%, 1% and 15.4% for UA78L05, MC78L05 and L78L05, respectively. On the other hand, the R values extracted at the high temperature were increased by 18.5%, 46.7% and 20.5% in comparison to that of at the nominal temperature for UA78L05, MC78L05 and L78L05, respectively. Under the influence of the lowest temperature, the capacitance value of UA78L05, MC78L05 and L78L05 was reduced from its nominal value by 8.1%, 18.5% and 10.1%, respectively. However, with an exception of MC78L05, whose capacitance value declined by 2.7% at high temperature, UA78L05 and L78L05 demonstrated 10.5% and 6.9% increase of its capacitance from its nominal value, respectively. Hence, these findings suggest that the PDN model plays considerable contribution to characterize the conducted immunity of these PDN at extreme temperatures. Considering the variations of the RLC values from their nominal ones as well as the measured injected power presented in Figures 3.5 and 3.6, the IB block look-up tabular data for MC78L05 also showed similar decreasing trend at the lowest and highest temperature in high frequencies compared to that of UA78L05 and L78L05. The IB model was determined to investigate its role and contribution to the overall immunity of the ICs, along with its PDN model. This assessment was established under the nominal temperature only, while considering little importance of including the IB look-up table at extreme temperatures.

3.5 Conclusion

This chapter demonstrated the combined impact of thermal stress and obsolescence by conducting DPI experiments on three functionally identical and pin compatible regulator ICs from three different manufacturers. The selected ICs were exposed to nominal temperature, low and high external temperature conditions (i.e., −30 °C and +100 °C) during the DPI measurements by injecting the RF disturbance on the input pin of the IC. Based on the defined immunity criterion (±4%), all the ICs under test were measured,

yielding either a positive or negative offset voltage at the V_{out} pin.

Under the nominal conditions, experimental results demonstrated that, compared to the other two ICs, the MC78L05 had the highest immunity in high frequency. However, that regulator model was found to be less immune to DPI injection when exposed to both low and high thermal stresses. Moreover, regardless of the IC manufacturers, it was observed that the DPI immunity tends to be increased significantly (around +30 dBm at 1000 MHz against almost +10 dBm at 10 MHz) with the increase of frequency at both high and low environmental stress conditions compared to that of the nominal temperatures. These results indicate that it would be essential to verify IC's conducted immunity when replacing by a second-source or a more recent EMC compliant functionally identical IC device.

Input impedance curves were also compared for all the considered ICs at low, high and nominal temperatures. With the increase of frequency, the impedance curves followed a similar trend but with significant level differences. Package inductance value for UA78L05 was found to be higher than the other two ICs, and the lowest capacitance value was obtained for L78L05. Hence, these RLC variations made it possible to conclude that the UA78L05 was the least immune in high frequency, while the L78L05 showed a high conducted immunity in low frequency. The IB block tabular data of exact transmitted power against frequency was further generated in nominal temperature from the DPI measurements for all the selected ICs. The concluded outcome of observing the highest conducted immunity for MC78L05 compared to the other two ICs was confirmed in high frequency. Hence, the comparative analysis of the conducted immunity performance of the considered ICs of different manufacturers would be essential to verify the electromagnetic compliance of an IC within a system, when replacing by a second-source or a more recent IC component.

In this study, the term "Obsolescence" refers to the drop-in replacement of an IC from a second source of another manufacturer, which is pin-to-pin compatible with similar functionality and specifications. If an IC is replaced by a second-source, it is thus important to make sure that its EMC behavior keeps the system within the EMC limit. It is also important to consider external thermal stress conditions for all second-sources in order to take into account of the environmental conditions of the system in its lifetime. This is also essential to highlight if the IC with similar functionality and specifications of another manufacturer is EMC compatible and can replace the existing EMC non-compatible IC in the system in order to meet the EMC compatibility requirement issue

for any particular applications. Future perspective of this ongoing research work would involve developing, constructing and integrating accelerated ageing stress conditions applied on these regulator ICs with the conducted immunity models the the to investigate the impact of ageing on the standard ICIM-CI model. Moreover, numerous samples of these selected analog ICs would be allowed to undergo ageing by conducting step-stress ADTs to characterize ageing phenomenon under the influence of multiple stress factors, including thermal and voltage overstress conditions for specified stress duration. Based on the evolution of the conducted EMC performance, statistical computation would be presented followed by developing degradation and reliability models to be able to predict the long-term electromagnetic evolution of the immunity parameters as functions of ageing and/or obsolescence. The above aforementioned studies would be presented in the next chapters.

Chapitre 4

Investigate and Analyze the Influence of High Temperature Accelerated Aging on the Conducted Immunity Modelling of the Analog ICs

This chapter aims to develop and compare ICIM-CI models of two different voltage regulator ICs with similar functionality (i.e., UA78L05 and L78L05) under the combined influence of two different electrical overstress (i.e., 9 and 12 V) and high temperature (i.e., 70–110 °C) stresses aging conditions for a total stress duration of 950 hours for ensuring EMC degradation within this short accelerated stress duration, while taking into account of the fact that these tested ICs would not go into permanent failure. Step-stress ADTs are performed on two samples of UA78L05 (i.e., T1 and T2) and L78L08 (i.e., S1 and S2) manufactured by Texas Instrument and STMicroelectronics, respectively. DPI test was conducted in nominal conditions (i.e., 7.5 V and 25 $°C$) on these selected ICs according to IEC 62132-4 standard before and after the accelerated aging test. For the studied cases, it was found that the PDN models extracted at nominal temperature before and after aging test for the ICIM-CI model of UA78L05 and L78L05 remained unaffected. However, the aging process affected the IB block of the ICIM-CI model significantly due to noticeable reduction in the conducted immunity level characterized by the extracted IB look-up table data in terms of power transmitted and frequency. It was demonstrated that both fresh and aged samples of L78L05 demonstrated higher conducted immunity profile compared to those of UA78L05. Moreover, the aged S1 and S2 samples showed lower immunity drift than those of the aged T1 and T2 respectively throughout the whole DPI frequencies, ranging between 10 and 1000 MHz. While applying the same thermal

step-stress on all the test samples inside the climatic chamber, DUT samples S2 and T2 aged at high electrical overstress (i.e., 12 V) conditions demonstrated higher mean drift of immunity level compared to that of the other two aged samples S1 and T1 under low electrical voltage (i.e., 9 V) stress conditions.

4.1 Introduction

The EMR of ICs is usually affected due to aging under the influence of harsh external environmental stress conditions (i.e., high temperature and electrical overstress) [4]. The various ALTs can be performed on ICs by applying stress conditions to activate and accelerate the rate of degradation due to intrinsic failure mechanisms induced by aging [53]. For example, HCI and NBTI are known to degrade the EMC performance of ICs [33]. Those internal degradation mechanisms modify different transistor parameters by lowering the electron mobility and increasing the V_{th} of the aged ICs, causing significant impact on electromagnetic emission under the applied electrical stress conditions [32]. Likewise, the influence of aging can also affect the functionality (i.e., noise, saturation current, signal propagation delay) due to the variation of the physical parameters of the transistors in both digital and analog ICs, resulting significant reduction in the conducted immunity to EMI [54] [1].

ALT methods, such as, HTOL and low LTOL, are usually performed on the ICs to evaluate the influence of aging on the conducted immunity to EMI. According to the AEC-Q100-Rev-H standard [55], HTOL test is performed by applying constant thermal stress at 150 °C for 450 hours, whereas LTOL test requires applying thermal stress at −40 °C upto the same stress period. In [53], both standard HTOL and LTOL tests were performed on the low-power 65 nm CMOS IC to characterize the influence of aging on the conducted emission and immunity levels of several input and output (I/O) pins of the ICs structures under test. The conducted immunity variation induced by aging was evaluated by performing the DPI test by injecting harmonic disturbance signal on the power supply and digital pins according to the IEC 62132-4 standard, but at 25 °C in both before and after the ALTs.

In [1], the HTOL aging test was performed to characterize the evolution of the aging induced immunity drift of analog circuit structure (i.e., variable controlled oscillator) designed in 0.25 μm CMOS technology. In [56], accelerated aging conditions (i.e., electrical overstress) was applied for a specific stress period on the regulator circuit implemented

on a test IC chip to accelerate relevant wear-out degradation mechanisms until the tested chip fails. The changes in the LDO immunity was characterized during the aging process using the DPI measurements according to the IEC 62132-4 standard [16] by measuring the conducted immunity parameters prior and after the ALTs, which showed an increase in the electromagnetic immunity drift [56]. Moreover, the long-term conducted immunity of different analog circuit blocks of the PLL circuit was analyzed by performing the ALTs, and the results revealed that the aging reduced the immunity profiles of the tested structures across the whole DPI frequency range [24].

The IC designers and manufacturers need to predict the the conducted immunity of ICs prior to the manufacturing phase. The ICIM-CI model has been proposed and published in the IEC 62433-4 standard [57]. This standard model can be extracted from simulations based on the knowledge about the internal structure of the IC under test. In [58], the effect of aging and external thermal stress conditions on the proposed ICIM-CI model of a custom-designed integrated oscillator was studied, demonstrating significant reduction of the conducted immunity level with better accuracy that can be taken into account in the future revised version of the ICIM-CI standard. In [20], multi-port conducted immunity model was proposed and compared with the measurements to validate accuracy of the simulation model to estimate the EMC performance of the bandgap reference circuit designed and implemented in the test chip. In [47], the LDO susceptibility model was proposed based on the MOSFET models to extract the ICIM-CI model, which was then validated using the DPI measurements. In [59], the ICIM-CI modeling process was presented by extracting individual models for both linear passive and non-linear active elements of the LDO regulator in order to compare the conducted EFT immunity measurement to the proposed simulation model. In [18], a white-box modeling approach was presented for the LDO regulator mounted on a test chip to demonstrate the methodology required to extract the ICIM-CI model. The model was then validated by comparing the simulation results to the DPI measurements. However, the impact of aging on the ICIM-CI models of ICs should be investigated in order to predict long-term EMR and lifetime reliability. In [48], an electrical simulation model for the voltage regulator as well as an accelerated degradation model were proposed to predict various reliability parameters based on functional performance under different thermal and electrical overstress conditions.

Overall, high aging temperature was incorporated into the development of the ICIM-CI model of the studied regulator ICs to investigate the impact of extreme external environmental conditions on the conducted immunity models of DUTs.This chapter is divided

into following sections. Section 4.2 provides description of the accelerated aging plan and experimental procedures to conduct both aging and DPI test to characterize the conducted immunity before and after the completion of the aging test. Section 4.3 illustrates the measurement results and findings of the experimental study conducted on both fresh and aged ICs, followed by comparing the EMC performance of both the tested L78L05 and UA78L05 DUT. Section 4.4 outlines the aging impact on the developed ICIM-CI model of the tested ICs, demonstrating significant changes between the fresh and aged IB lookup tabular data and insignificant effect of aging on the developed PDN model. Hence, the main outcome demonstrated refers to the fact that the standard ICIM-CI model might be updated and modified to analyze the EMC performance, while taking into account of the influence of accelerated aging on the conducted immunity model of ICs.

4.2 Materials and Methods

This section presents the test conditions for accelerated aging applied to the chosen voltage regulator ICs. Furthermore, it also introduces the experimental test setup used to conduct high temperature step-stress ADT as well as the DPI test on the ICs to characterize the aging impact on the developed ICIM-CI models.

4.2.1 Accelerated aging test plan

The accelerated aging test plan was designed to investigate and compare the high temperature aging impact on the EMC performance degradation and the ICIM-CI models of the selected ICs (i.e., UA78L05 and L78L05). Table 4.1 provides information on the accelerated aging test plan, which includes the number of IC test samples, total aging stress duration, electrical overstress and thermal stress conditions applied on the samples.

Table 4.1 demonstrates that identical thermal step-stress conditions were applied to each of the four DUT samples. Two samples (i.e., T1 and S1) of UA78L05 and L78L05, were respectively subjected to a low arbitrary electrical overstress voltage of 9 V (20% higher than nominal voltage). In contrast, high supply voltage stress condition (60% greater than nominal voltage) was chosen for the T2 and S2 samples, ensuring the aged samples remain operational at the end of the aging test. It is worth to mention that these DUT samples with similar functionality and pin compatibility, manufactured by different companies, were selected to compare their conducted immunity performance based on the

TABLE 4.1 – Design Of The Accelerated aging Test Plan

IC reference	Samples	Thermal stress (°C)	Electrical overstress (V)	Total stress duration (hours)
UA78L05	T 1	70-110 °C	9 V	950 hours
	T 2	70-110 °C	12 V	950 hours
L78L05	S 1	70-110 °C	9 V	950 hours
	S 2	70-110 °C	12 V	950 hours

applied aging test plan.

4.2.2 Measurement test setup and procedures

Four fresh DUT samples were placed inside the climatic chamber (Climat2) to perform high temperature accelerated aging test for 950 hours. The accelerated aging test setup is shown in Figure 4.1. The test setup consists of high temperature cables (Amphenol-RF 095-902-466-004) to withstand high temperature within the climatic chamber (Figure 4.1b) as well as external DC power supply sources for providing electrical overstress above the nominal voltage (i.e., 7.5 V) into the V_{in} pin 8 (Figure 4.1a) of the tested ICs. Those temperature cables are used to inject the DC input voltage signal to the V_{in} pin of these ICs. The Spirale V software interface integrated with the climatic chamber was used to develop a program for regulating and maintaining the thermal step-stress conditions inside the chamber. The latter consisted of varying the temperature from 70 °C to 110 °C with a linear step increment of 10 °C after every 200 hours, reaching the maximum aging temperature at 800 hours, and the step-stress ADT was continued for the remaining 150 hours. It should be noted that the maximum temperature stress and total stress duration were chosen based on the operational characteristics of the selected ICs so that the aged samples remain functional avoiding permanent failure throughout the step-stress ADT.

The above-mentioned aging plan was applied to all the four DUTs in the controlled environment condition for the complete duration of the step-stress ADT induced aging. The aged samples were removed from the thermal aging climatic chamber at the end of the process, and the DPI immunity test was performed at the nominal condition (i.e., 7.5 V and 25 °C) in accordance to the IEC 62132-4 standard [16]. The standard DPI test

bench was used to perform the DPI experiment, and the relevant measurement data (i.e., power injected and frequency) were recorded on both fresh and aged IC samples in order to analyze the influence of the aging process on the conducted immunity of the tested ICs.

(a)

(b)

FIGURE 4.1 – Accelerated aging test set-up (a) outside view ; (b) inside view of the climatic chamber.

The DPI measurement setup is similar to that in [60]. The harmonic disturbance signal was injected into the V_{in} pin of each considered sample ICs. Continuous sinusoidal electromagnetic (EM) disturbance signal was generated by the signal generator (Agilent N5183A) and injected on the V_{in} pin of the IC after signal propagation through the bi-directional coupler, while performing the DPI test before and after the accelerated aging test. The disturbance signal was amplified by the RF amplifier (Prana AP32DT120) and allowed to superimpose over the nominal 7.5 V DC biasing voltage provided by an external power supply source through the decoupling network (i.e., wideband bias-tee and capacitor) into the V_{in} pin of the IC. With a linear step-size of 10 MHz, the injected signal's amplified signal power was linearly varied between 3 and 30 dBm over the RF frequency range of 10 to 1000 MHz.

Two independent power meters were utilized to record relevant measurement data (i.e., forward power and reflected power). The LabView interface, which is incorporated with the DPI test bench, is programmed to measure the P_{inj} when the defined failure threshold criterion is observed at various frequency values. Based on the forward and reflected power measured from the power meters, the minimum P_{inj} required to cause IC malfunction was recorded at each corresponding frequency values over the entire tested DPI frequency values. The DPI failure threshold criterion of ±4% deviation from the nominal DC V_{out} was considered on all the test samples, resulting a DC offset voltage (i.e., ±0.2 V) variation from the nominal V_{out} at the pin 1 (Figure 4.1a) of those DUT samples. The DPI failure threshold was chosen with a fixed arbitrary value to ensure the ICs remained operational throughout the step-stress ADT, taking into account of various functional performance parameters (i.e., maximum operating temperature, maximum current and operating voltage) of the regulator ICs. It is worth to mention that the input current remained unchanged during the aging process.

4.3 Results and Discussion

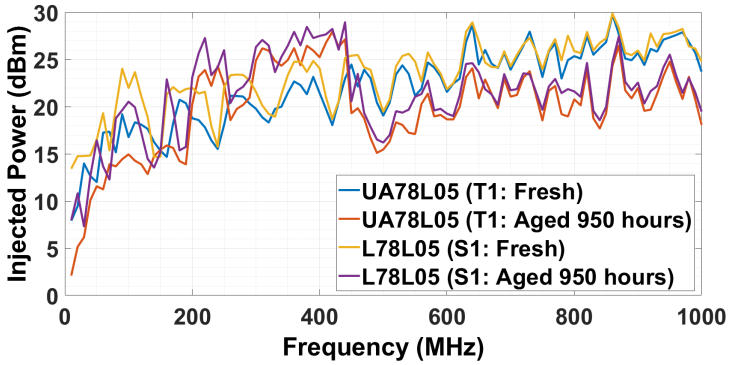
This section presents the experimental results to analyze the combined effect of applying thermal and electrical aging stress conditions on the conducted immunity to EMI. Moreover, several aging-induced immunity drift parameters (i.e., mean power injection drift, maximum and lowest aging drift, and standard deviation) for these tested samples were analyzed and compared based on those EMC measurements recorded before and after aging.

4.3.1 Accelerated aging impact on conducted immunity

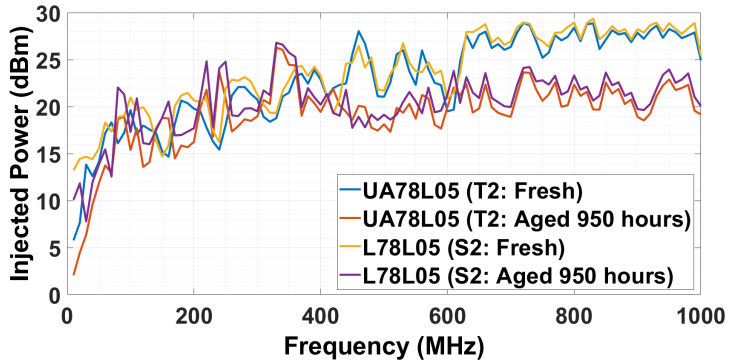
The conducted immunity profile for both fresh and aged ICs under two different electrical overstress (i.e., 9 V and 12 V) and identical thermal stress conditions is depicted in Figure 4.2. The aging impact on the conducted immunity of the samples S1 and T1 subjected to low electrical overstress and high thermal step-stress conditions is displayed in Figure 4.2a. Across the whole DPI frequency range, it was found that the fresh L78L05 sample (i.e., S1) was more immune than that of UA78L05 (i.e., T1). Although the conducted immunity profiles for both of these fresh DUT samples showed a gradual increasing trend, the P_{inj} into the V_{in} pin of the S1 sample varied from 12.5 to 25 dBm between 10 and 1000 MHz, while the T1 required lower P_{inj} (i.e., 8 dBm at 10 MHz and 24 dBm at 1000 MHz) to induce the DPI failure. The influence of aging caused by high temperature and low electrical overstress (i.e., 9 V) conditions resulted in a significant degradation of the conducted immunity level of the tested samples S1 and T1 at both low and high frequency values, ranging from 10 MHz to 200 MHz and 450-1000 MHz, respectively. Conversely, aging induced by the step-stress ADT and electrical overstress (i.e., 9 V) improved the conducted immunity level of both the aged samples (S1 and T1) in the mid frequency range (i.e., 200-450 MHz). Furthermore, it could be observed that the immunity profile waveform produced for the aged S1 sample needed larger P_{inj} throughout the whole DPI test frequency spectrum than that of the aged T1 sample.

Figure 4.2b illustrates the effect of aging on the conducted immunity level of the test samples (S2 and T2) for the L78L05 and UA78L05, respectively, subjected to both high electrical overstress (i.e., 12 V) and identical thermal stress conditions as outlined in the Table 4.1. Under the effect of the high electrical overstress, both the tested S2 and T2 samples demonstrated a significantly higher difference in the P_{inj} between the aged and fresh states at each corresponding DPI frequencies compared to those of the S1 and T1 samples depicted in Figure 4.2a. Between 10 and 1000 MHz, the sample S2, both in fresh and aged states, could endure greater P_{inj} compared to that of the fresh and aged T2 sample. As a result of this immunity behaviour, it was possible to conclude that the S2 was more immune to the harmonic disturbances than that of the the considered T2 sample.

It is worth mentioning that the observed change of the conducted immunity level could be due to the degradation of the associated CMOS transistors within the tested ICs. Depending on the stress magnitude and duration, the step-stress ADT would activate and accelerate intrinsic degradation mechanisms that could modify the electrical properties (i.e., V_{th} and charge carrier mobility) of several aged CMOS transistors. Numerous internal



(a)



(b)

FIGURE 4.2 – Aging impact on the conducted immunity profile of IC samples under same thermal stress and (a) low electrical overstress (i.e., 9 V); (b) high electrical overstress conditions (i.e., 12 V).

CMOS transistors of the aged DUTs could be degraded due to high positive biasing voltage and the biasing current caused by the electrical overstress condition, which would increase the V_{th} and reduce the charge carrier (i.e., holes and electrons) mobility [4]. Thus, a clear relationship between the variations of the physical features of CMOS transistors induced by aging and the conducted immunity level could be established. The influence of aging on the observed dispersion of the conducted immunity level between the fresh and aged states of the tested samples under the DPI measurements can be a result of the variability of the DUT characteristics and the measurement uncertainty of the DPI test bench equipment.

4.3.2 Aging induced conducted immunity drift of ICs

The P_{inj} measured for both fresh and aged ICs (i.e., L78L05 and UA78L05) under the nominal conditions were used to evaluate the aging induced immunity drift threshold, also

known as the power injected drift (ΔP_{inj}), by subtracting the measured injected power $P_{inj_{AGED}}$ of the aged sample from that of the recorded $P_{inj_{FRESH}}$ of the fresh sample. The aging induced immunity drift of the test samples at each corresponding frequency value Figure 4.3. Negative EMC immunity drift was observed for both aged samples of L78L05 and UA78L05 at the high frequency range (i.e., 650-1000 MHz). Throughout the whole DPI frequency range, both the aged T1 and T2 samples showed slightly higher mean immunity drift than those of the aged S1 and S2. Moreover, positive ΔP_{inj} of the immunity threshold was observed within the specific frequency range (i.e., 250-450 MHz) due to the fact that the measured P_{inj} of the aged sample was higher than that of the fresh IC, highlighting an improvement in the conducted immunity level of all the tested samples. The impact of the high electrical overstress condition on the aged S2 and T2 samples could be noticed in their respective aging immunity drift waveform, which is shown in the Figure 4.3. The aged S2 sample showed greater ΔP_{inj} immunity drift than the aged S1, indicating higher conducted immunity drift due to the significant influence of the electrical stress observed on the EM immunity of the aged DUT. Likewise, the aged sample T2 demonstrated higher conducted immunity drift level compared to that of the T1 due to observing noticeable difference in the ΔP_{inj} evaluated throughout the whole frequency range.

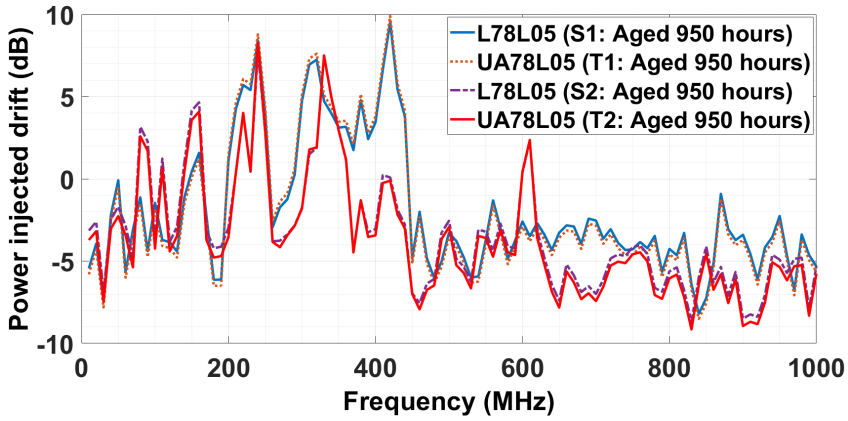


FIGURE 4.3 – Influence of the aging on the conducted immunity drift of the tested ICs.

Table 4.2 summarizes aging induced EMC drift parameters computed for all the distinct samples of ICs (i.e., L78L05 and UA78L05). The absolute mean EMC aging drift (ΔMP_{inj}) over the entire frequency range is evaluated as the ΔP_{inj} for both the UA78L05 and L78L05 varied at every corresponding frequency value. The ΔMP_{inj} for the aged S1

and S2 samples of was 6.97% and 6.4% lower than those of the aged T1 and T2, respectively. Thus, the L78L05 showed more EM robustness and immunity than the UA78L05 under the indicated accelerated aging conditions. Due to the effect of the high electrical overstress and the defined identical thermal step-stress external factors, the aged S2 and T2 samples exhibited greater immunity drift than the other two aged (S1 and T1) samples. The ΔMP_{inj} of the S2 sample was found to be 9.2% greater than the other DUT of the same IC (i.e., L78L05), with a higher mean standard deviation (σ) of the immunity drift. Similar immunity behaviour was observed for the aged samples of UA78L05, with a 7.9% increase in ΔMP_{inj} for the T2 sample and an 18% higher σ compared to the other aged T1 sample. From an EMC point of view, the computed minimum and maximum power injected drift level for those tested IC samples were found in each corresponding DPI frequency values at which the negative and positive drift had occurred, respectively.

TABLE 4.2 – Aging Induced Immunity Drift Parameters

IC reference	Samples	Absolute mean EMC ageing drift (ΔMP_{inj}) [dB]	Minimum EMC ageing drift ($P_{inj_{MIN}}$) [dB]	Maximum EMC ageing drift ($P_{inj_{MAX}}$) [dB]	Mean standard deviation over all the frequency range (σ) [dB]
UA78L05	T 1	4.31	-8.51	9.90	1.88
	T 2	4.68	-9.15	8.28	2.22
L78L05	S 1	4.01	-8.19	9.54	1.83
	S 2	4.38	-8.72	7.85	2.09

The evolution of the EMC robustness of a tested sample could also be measured and compared by evaluating both ΔMP_{inj} and σ for the aged UA78L05 and L78L05 tested sample using the following mathematical expressions as shown in (4.1), where $P_{inj}X_f$ refers to the power injected after aging, P_{injY_f} refers to the power injected at each DPI frequencies before aging, f_a and f_b represent the minimum and maximum DPI frequency value respectively, varying between 10 and 1000 MHz with a step-size of 10 MHz between each frequency point, and $n_{frequency}$ represents the total number of frequency values. As the accelerated aging can affect the variability between the pin-to-pin compatible with identical functionality tested ICs (i.e., UA78L05 and L78L05), the σ of the immunity levels needs to be computed over the entire DPI frequency range for the aged DUT samples. The mathematical expression to evaluate σ of both the aged UA78L05 and L78L05 across the entire DPI frequency range is shown in (4.2). It is worth to mention

that observed variation in the conducted immunity drift between UA78L05 and L78L05 might also be impacted by the measurement repeatability issues due to the uncertainties of the DPI measurement components. Nevertheless, the latter caused by the DPI test bench variation is independent of the tested ICs, ensuring insignificant impact on the evolution of the observed conducted immunity drift induced by aging [33].

$$\Delta MP_{\text{inj}} = \frac{1}{n_{\text{frequency}}} \sum_{f=f_a}^{f_b} |P_{\text{inj}X_f} - P_{\text{inj}Y_f}| \quad \text{for } f_a \le f \le f_b \tag{4.1}$$

$$\sigma = \sqrt{\frac{\sum_{f=f_a}^{f_b} (P_{\text{inj}X_f} - \Delta MP_{\text{inj}})^2}{n_{\text{frequency}} - 1}} \quad \text{for } f_a \le f \le f_b \tag{4.2}$$

4.4 Effect of Aging on the ICIM-CI Model of ICs

The ICIM-CI was developed for both fresh and aged DUT samples in order to compare and analyze the effect of aging on the conducted immunity of the selected ICs(i.e., UA78L05 and L78L05). To investigate influence of aging on these ICIM-CI models, both the PDN and IB models were extracted from the experimental results obtained before and after accelerated aging tests for each individual DUT of L78L05 and UA78L05. The passive PDN block for each DUT was developed by S-parameter measurements using the VNA similar to that in [8]. The measured reflected coefficient S_{11} was used to determined the input impedance Z_{11} between the V_{in} and ground (GND) pins of the IC samples before and after accelerated aging. The PDN block was then modeled by extracting the unknown parameters of the lumped passive components (e.g., resistor, inductor and capacitor) from the Z_{11} profile to investigate the contribution of the aging effect on the PDN block of the ICIM-CI model. Figure 4.4 displays the Z_{11} profile curves versus frequency (i.e., 1–1000 MHz) for both the fresh and aged S1 and T1 test samples. It was found that the impedance profiles of both new and aged ICs remained comparable, with the exception of the aged L78L08 sample (i.e., S1), which exhibited a higher impedance compared to the UA78L05 below and above the resonant frequency, that could be due to higher resistance (R2), lower coupling capacitance (C2), and parasitic inductance (L2) values. As observed in Figure 4.4, the extracted RLC values of the PDN model for the aged T1 sample were 35.5 Ω, 19.8 μH and 41.2 pF, whereas the overall RLC values for the aged

L78L05 were found to be 49.2 Ω, 21.6 pF and 16.8μH. The conducted immunity could be similar for both of these tested IC at high frequency due to the small difference in the Z_{11} values dominated by the extracted $L1$ and $L2$ values of the PDN block. Note that, the input impedance profiles of the other two IC samples remained constant after being aged at high electrical overstress condition. Thus, it can be concluded that the PDN block of these studied IC samples was unaffected by aging.

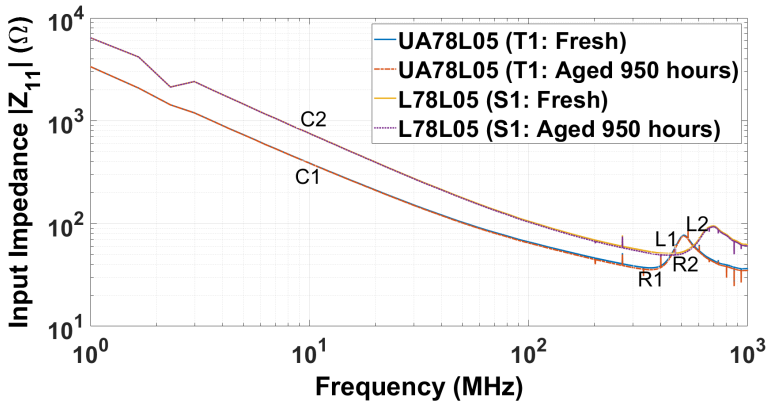
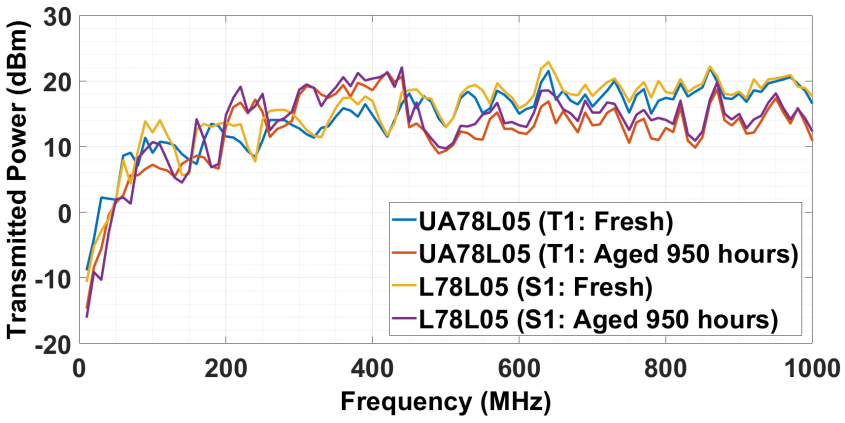


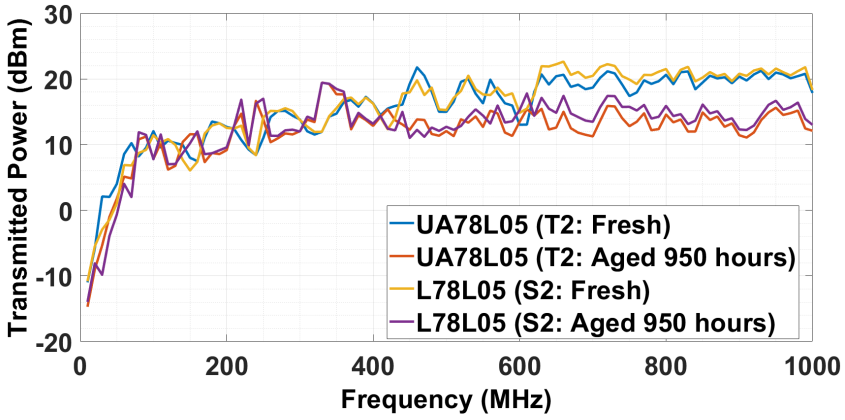
FIGURE 4.4 – Influence of the aging on the input impedance profile of V_{in} of the selected ICs.

The black box approach was considered to produce the IB block for each individual samples of both UA78L05 and L78L05 by extracting the look-up table from the DPI measurement data. The look-up table data include the actual P_t to the V_{in} pin at each corresponding DPI frequency value, causing the DPI failure on the considered IC samples. This P_t corresponds to the actual power that couples into the pin of the IC mounted on the PCB, and it is considered as the relevant parameter for analyzing the conducted immunity level under the influence of aging. The P_t was evaluated by using the P_{inj} measurement data recorded from the DPI measurements, S_{11} measured using the VNA and insertion loss owing to the cables and PCB trace. The mathematical expression to evaluate the actual P_t to the pin of the IC samples under test is provided in (3.4).

The data from the look-up table, which corresponds to the IB blocks of the ICIM-CI models of L78L05 and UA78L05, was extracted and plotted against the DPI frequency range, as can be seen in the Figure 4.5. Figure 4.5a shows that the P_{trans} of the aged T1 sample decreased by a mean deviation of 4.3 dB and 4 dB for the aged S1 over the whole frequency range. Besides, the maximum P_{trans} deviation between the aged and fresh samples of UA78L05 and L78L05 is 9.9 dB and 9.5 dB, respectively.



(a)



(b)

FIGURE 4.5 – Influence of aging on the IB block of the ICIM-CI model of ICs under same thermal stress and (a) low electrical overstress (i.e., 9 V) ; (b) high electrical overstress conditions (i.e., 12 V).

Similar to the Figure 4.5a, Figure 4.5b demonstrates that the P_t level of the aged test samples is lower than that of the fresh ones at each corresponding frequency, with the exception between 200 and 400 MHz, which is due to the improvement of the conducted immunity profile due to aging. Furthermore, the average P_t drift of the aged samples owing to aging under high electrical stress was 4.4 dB and 4.7 dB for the S2 and T2, respectively. As a result, the reduced P_t level observed in both Figures. 4.5a and 4.5b depict that the accelerated aging impacts the extracted IB blocks of the ICIM-CI models of both UA78L05 and L78L05. In order to account for the effect of aging on the developed ICIM-CI models of the tested IC samples, it is essential to readjust the IB look-up tables with the modified and updated P_t and corresponding frequencies.

4.5 Conclusion

The objective of the study was to integrate the aging impact caused by elevated temperature and voltage overstress into the developed standardized ICIM-CI model of the tested ICs for investigating the effect of aging on the conducted immunity model of the studied regulator ICs. A comparative study was conducted using measurements on the two pin-to-pin compatible voltage regulator ICs (i.e., L78L05 and UA78L05) to examine the effect of thermal and electrical overstress aging stresses on the developed ICIM-CI models. The DPI experiments were carried out on both fresh and aged ICs. Two different samples of both L78L05 and UA78L05 were aged inside the climatic chamber to accelerate the rate of internal degradation mechanisms (i.e., HCI or/and NBTI) under the combined impact of the defined thermal step-stress and electrical overstress conditions.

The PDN model was developed using the S-parameter measurement and the corresponding Z_{11} profile of each considered fresh and aged samples. It was found that the PDN model was unaffected by aging due to observing no variation in the R, L, and C values of the passive elements included in the model. Before and after the accelerated aging of the ICs, DPI tests were performed in nominal conditions and measurements were recorded in nominal conditions to extract the look-up table for constructing the IB blocks of individual samples. It was discovered that the aging reduces the P_t level, resulting in a significant impact on the IB block of both L78L05 and UA78L05 examined samples. Hence, aging caused by performing the step-stress ADT at the defined stress conditions decreased the conducted immunity of the considered ICs in a given frequency range, with UA78L05 having a higher mean standard deviation of the P_t between fresh and aged samples than the L78L05. In order to take into account of the effect of aging on the IB blocks of the ICIM-CI models of the IC samples under test, the modified P_t values as a function of frequency should be updated in the look-up tables by applying statistical deviations of the aging immunity drift.

The future perspective of the conducted experimental case study would be to implement the same research methodology on numerous IC samples for both UA78L05 and L78L05 and perform statistical computations based on the measurement data to draw a general conclusion on the influence of integrating external aging stress conditions on the developed ICIM-CI model, particularly taking into account of the required changes in the IB model, demonstrating the non-negligible contribution of applying multiple aging stress conditions on the EMC performance evolution on the tested IC samples.

The following chapter presents development of degradation and reliability models of these selected IC regulators to predict lifetime reliability parameters (i.e., TTF, PoF) and unknown model parameters based on the observed degradation of the conducted EM immunity test results as a function of DPI frequencies at different aging stress time intervals, while performing the thermal aging step-stress ADTs on numerous DUTs of both UA78L05 and L78L05 under constant electrical overstress conditions.

Chapitre 5

Degradation and Reliability Modeling Approaches to Assess the Long-Term EM Robustness of ICs

5.1 Introduction

This chapter presents an approach to develop degradation and reliability models of analog and digital IC based on the long-term evolution of the EMC performance degradation due to the stress time-dependent ADT. The proposed log-linear ALT model is combined with the Weibull unreliability distribution function model to estimate the failure lifetime data against the applied voltage stress at three different failure threshold criterion. At various constant voltage overstress and threshold constraints, the lifetime reliability performance parameters (i.e., TTF, PoF, model constants) of the tested DUTs were evaluated based on the measured degradation data.

The physics-based modeling approach is utilized to develop the model for the degradation paths based on the observed monotonic degradation of the measured degradation data as well as the conditions of the thermal stress ADT. In order to estimate the unknown parameters of the developed degradation model, the MLE method is combined with a genetic optimisation algorithm. The ADT plan is designed and conducted on six samples of both UA78L05 and L78L05 ICs placed inside a climatic chamber combining both the thermal step-stress (i.e., 70-110 °C) and constant electrical overstress (i.e., 9 and 12 V) conditions for a total stress duration of 950 hours. All the selected UA78L05 and L78L05 samples are subjected to the direct DPI measurement test under nominal conditions in order to characterize their conducted immunity to EMI. The statistical degradation data (i.e., the average injected power) of the aged samples is computed across

the entire DPI frequency range for a variety of stress time duration. In addition, this chapter also compares and analyzes the long-term conducted immunity degradation of a digital circuit, embedded within the tested Attiny85 micro-controller IC samples developed by Atmel, due to applying multiple accelerated aging stress (i.e., temperature and electrical voltage) conditions based on the designed constant-stress ADT plan, prior to developing the degradation and lifetime reliability models. Depending on the observed EMC performance degradation data, the aforementioned developed models allowed for the estimation of various model parameters in both tested and untested environmental conditions. This chapter is divided into following sections. The first section 5.2 is dedicated a state-of-the-art on ALT and ADT to modeling and estimation of degradation performances and reliability metrics. Section 5.3 presents the design of the thermal step-stress ADT plan and the measurement test setup for performing this accelerated aging test on the selected L78L05 and UA78L05 regulator DUTs. Furthermore, this section discusses the experimental approach and methodology used to characterize the evolution of the EMC performance degradation of the chosen DUTs under the effect of different stress conditions (high temperature and electrical voltage). Section 5.4 demonstrates the measurement algorithm and procedure followed to conduct the DPI test on the selected DUTs to characterize the conducted immunity evolution at different stress duration. Section 5.5 analyzes the observed EMC degradation of the tested analog IC samples caused of the accelerated aging, prior to estimating various unknown degradation model parameters. Section 5.6 demonstrates the construction of the ALT reliability models and compares the predictive reliability model parameters for the tested samples, subjected to the defined threshold criterion and multiple stress conditions. Section 5.7 presents the ADT modeling approach by applying the physics-based degradation model based on the measured ADT data recorded for both L78L05 and UA78L05 tested samples. Section 5.8 provides detail discussion on the procedures involved for developing the degradation and reliability model of the Attiny85 micro-controller IC based on investigating and analyzing the conducted immunity degradation of the digital circuits within the tested IC samples, subjected to combined influence of both thermal and electrical voltage overstress conditions defined in the designed ADT plan.

5.2 State-of-the-Art on ALT and ADT

Analog ICs in electronic systems demonstrate significant evolution of their EMC performance when subjected to external environmental (i.e., temperature, humidity, electrical overstress) conditions. Considering the accelerated aging of IC-level electric circuits, reliability analysis is essential for estimating the lifetime of a device. During the operational lifetime of the ICs in nominal environmental conditions, these electronic components experience various internal failure mechanisms in extreme environments (i.e., gate oxide defect, electromigration, HCI, bias transistor instability, and mobile ion contamination) due to high or low temperature, humidity, and positive or negative biasing electrical overstress, resulting in the formation of cracks, holes and trapping of charge carriers in the gate oxide layer [61], [62]. Consequently, the aging of an IC's internal metal-oxide semiconductor transistors (i.e., threshold voltage, drain-saturation current, and electron mobility) may alter its operational characteristics (noise, leakage current, propagation delay, operating frequency, and gate oxide capacitance) [33]. During the accelerated aging process, degradation or intrinsic failure mechanisms are activated, resulting considerable distortion in the functional performance characteristics causing significant impact on the conducted immunity and emission of the ICs, operating within the electronic system. Multiple stress factors accelerate the aging process, allowing the acceleration rate of the relevant wear-out processes to rise depending on the size and duration of the stresses [53], [63].

Different types of ALTs can be performed to extract reduced lifetime failure data after the component fails permanently due to the application of external stress factors of varying magnitude for a fixed duration [30]. ADTs can be conducted to compute pseudo lifetime failure data based on a predefined degradation criterion without enduring permanent or hard failure. The goal of these elevated stress tests is to determine the DUT's lifetime reliability, failure rate, and other functional parameters or characteristics under normal operating conditions [64]. The AF associated with a degradation mechanism induced by a known ageing stress condition can be computed using reduced lifetime failure data obtained during the short duration of the test, and the extracted data of the DUT can be extrapolated for any defined environmental condition [33]. Acceleration law models (i.e., Arrhenius, Eyring) are required for extrapolating the computed failure time data obtained from the accelerated ageing tests so that the long-term lifetime reliability of the tested components can be predicted for any tested or untested conditions [65]. Moreover,

these reliability acceleration tests enable the development of various reliability modeling functions for each corresponding ageing stress levels depending on the defined stress conditions. Considering the fact that acceleration laws due to various stress types can be computed from the trend of the reliability functions at different stress conditions, the ALTs are performced for the short duration which lead to the determination of the tested component's reliability parameters quantitatively at the nominal operational condition [66].

ADT is regarded as a suitable method for estimating the lifetime reliability parameters of electronic components. Considering the difficulty to determine the reliability assessment of highly reliable components operating in nominal environmental conditions, the degradation test should be designed and conducted at high stress levels to accelerate performance degradation metrics (i.e., voltage, current and power), thereby enabling the prediction of lifetime reliability data in nominal or other environmental conditions [67]. Various types of degradation modeling approaches (i.e., general path and stochastic process) were employed in prior research to examine ADT data. In [68], a stochastic process was used to develop the best fitting degradation path model using ADT measurement data for DC thin-film capacitors subjected to specified humidity stress conditions.

Different kinds of degradation modeling approaches, with specific limitations and advantages, as a function of stress magnitude and duration, can be considered to assess the deterioration of functional performance, reliability prediction and life span of electronic component [69]. Stochastic degradation process (e.g., Markovian), which include the inverse Gaussian method was applied to develop degradation model, considering the random behaviour of the degradation data [70]. Such random behavior of the observed degradation path was modeled by adopting Markovian stochastic process, which includes the inverse Gaussian method. In [71], the degradation of a light-emitting diode was investigated by developing a random-effect Wiener process model that took measurement errors into account. In [72], a non-Markovian process involving degradation modeling approach was used to examine the random degradation and predict the remaining useful lifetime of lithium ion batteries. The Tweedie exponential dispersion process model was developed to demonstrate that the multi-level step-stress ADT plan could be transformed into a simple step-stress ADT plan by taking into account of the D-optimality and V-optimality criterion [73]. This proposed ADT design plan was implemented to obtain numerical degradation data of the tested LEDs, followed by conducting a simulation study to compare the efficiency of the proposed optimum test design plan to that of the other step-stress

ADT plans presented in the previous literature studies. The Bayesian Markov chain Monte Carlo method was applied to these analytical models in order to effectively estimate the MLE model's parameters and analyze the computed results of the measured data [74]. In [75], a multivariate general degradation path model was developed to investigate the general trend in the degradation data with multiple degradation characteristics of the tested sample by incorporating covariance and integrating random effects that consider variation among the observed non-linear degradation paths. The unknown model parameters of the proposed model were predicted by integrating an expectation maximization algorithm with the Markov chain Monte Carlo simulation method for predicting system reliability using a closed-form reliability function. A prognostic method was applied based on the proposed generalized extreme value distribution to fit the developed model accurately to the contact resistance degradation data of electrical connectors subjected to thermal cycling ALT [76]. This data driven method was implemented by applying this statistical degradation process enabled to predict the failure in time rate and failure probability of the tested connectors for both short and long duration of ALT.

Assessing the traditional reliability life testing on some highly reliable components may not be suitable by observing hard or soft failure within the tested duration due to minimal or negligible performance degradation under the specified stress conditions [77]. Due to the rising demand for dependable and long-lasting products, reliability analysis have emerged as essential elements in the design and development of electronic systems. Previous research studies demonstrated different methods for proposing and analyzing usefulness of these developed models. In [78], an alternative degradation modeling approach is introduced to analyze measured fatigue crack degradation data by employing Weibull distribution with a time-dependent shape parameter *beta* and estimating the model's unknown parameters using the MLE method. On the basis of the right-censored measured degradation data generated by the rocket engine trials, the MLE method was used to estimate the unknown parameters of the Weibull distribution [79]. In [80], degradation model was proposed with standard deviation function and random regression coefficients based on the observed linear deviation of the semiconductor's V_{th} over time. In addition, statistical methods were developed to estimate the failure time distribution for a variety of degradation models [81], including the non-linear mixed effects model to introduce Monte Carlo simulation-based methods for determining point estimates and confidence intervals prior to assessing the component's reliability.

To develop an accurate degradation path modeling is essential before predicting re-

liability parameters of electronic components in an electronic system. In [82], the developed reliability tool was used to predict the reliability of an static random access memory (SRAM) digital IC (i.e., 6 transistors) as a function of time. Mean Time-to-Failure (MTTF) was evaluated prior to the fabrication of the IC, using reliability test data obtained from the wafer fabrication technology. To predict the SRAM's reliability, a quantitative reliability modeling approach was developed, taking into consideration an extended building-in-reliability (BIR) methodology and the wafer-level reliability system [83]. This methodology was utilized to show that there are strong relationships between wear-out and package level SRAM degradation. In [84], the commonly used physics-of-failure lifetime models for wire bond interconnects, available in power electronic modules, were studied to investigate the effect of high-temperature stress on the wire bonds. Electrical simulation model for the low voltage regulator was developed and coupled to the degradation model in order to predict pseudo failure time and the related developed reliability model parameters, when subjected to the defined constant multiple stress (i.e., high thermal and electrical overstress) conditions [85].

Numerous research studies were conducted to examine the EMC performance before and after the aging process performed on both analog and digital ICs. In [8], construction and validation of the developed conducted immunity and emission models of various aged ICs (i.e., operational amplifier, micro-controller) were studied. The long-term immunity of an aged phase-locked loop was accurately predicted and validated by developing a simulation model and comparing it to DPI measurements [24]. In accordance with the IEC 62132-4 standard [16], the DPI experiment was performed on different blocks of the phase-locked loop circuit to characterize the conducted immunity in frequency domain. In accordance to following the reliability standards (AEC-Q-100-Rev-H) [55], the impact of performing accelerated ageing tests on the electromagnetic robustness of ICs was investigated and simulation model was developed and compared to the measurement data to investigate the ageing impact [4]. The influence of ageing is integrated on the developed ICIM-CI of the tested voltage regulator ICs were investigated [86]. In [87], the impact of aging on the EMC performance of a Spartan6 Xilinx FPGA digital circuit device was studied to predict the long-term conducted emission level by proposing a new methodology, which involved constructing the conducted emission model for the tested FPGA, while accounting for accelerated ageing using the predictive multi-stressors reliability model (M-STORM) [88].

Prior research studies have focused on predicting the lifetime reliability based on the

conducted emission of the digital ICs. However, to the best of our knowledge, the development of both degradation and reliability models based on the conducted immunity performance degradation of ICs have not yet been investigated. The use of combined thermal and electrical voltage overstress conditions to characterize the conducted immunity of analog and digital ICs for accurately estimating their degradation and reliability model parameters have not yet been studied. Thus, the current study aims to demonstrate the ALT and ADT modeling approach by combining the life-stress acceleration laws with various statistical distributions (i.e., Weibull, Log-normal and Exponential) to determine the lifetime reliability and predict the EMC performance degradation of analog voltage regulator ICs under the combined influence of both the constant electrical overstress and thermal step-stress conditions. Thus, coupling of the conducted immunity or emission tests with the ageing accelerated life tests (i.e., HTOL, temperature cycling and LTOL) is essential to investigate the long-term electromagnetic robustness of ICs in real-life harsh environmental conditions. Thus, the major highlights of this chapter is to compare the EMC performance of two functionally identical voltage regulator ICs (i.e., L78L05 and MC78L05) family, followed by developing degradation and reliability models based on the evolution of the observed conducted immunity measurement data to predict lifetime reliability parameters of the tested analog voltage regulator IC samples, subjected to the combined constant electrical overstress and thermal step-stress ADTs.

5.3 Materials and Methods : EMR Assessment of Analog ICs

This section deals with the design of the ADT plan as well as the measurement setup used to perform the accelerated aging test on the selected functionally identical and pin-to-pin compatible voltage regulator ICs developed by two different manufacturers (i.e., STMicroelectronics L78L05 and Texas Instruments UA78L05). The test samples were mounted on a generic SOIC8 extraction test board made of a 4-layer FR4 PCB (Figure 5.2b).

5.3.1 The thermal step-stress ADT plan

The step-stress ADT plan was designed to accelerate the aging process of the ICs depending on the choice of multiple stress types (i.e., thermal and electrical voltage),

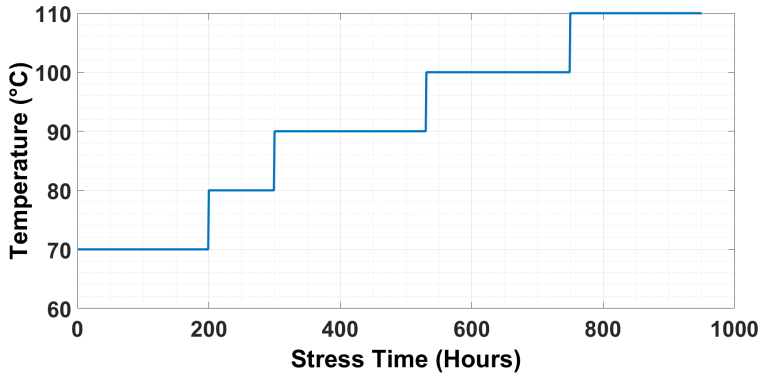


FIGURE 5.1 – The step-stress ADT plan.

magnitude and total stress duration. Figure. 5.1 depicts the considered high temperature step-stress ADT, whereas Table 5.1 provides information on the number of IC samples under the influence of both temperature and electrical overstress conditions. It is worth mentioning that the stress duration differed for various thermal stress magnitude to assess, if any, the impact of stress duration on the EMC degradation evolution of the tested samples.

TABLE 5.1 – Aging stress conditions to perform the ADTs on the ICs

IC reference	Samples	Electrical voltage stress	Temperature stress	Total stress duration
L78L05	S1, S2 and S3	9 V	70 – 110 °C	950 hours
	S4, S5 and S6	12 V	70 – 110 °C	950 hours
UA78L05	T1, T2 and T3	9 V	70 – 110 °C	950 hours
	T4, T5 and T6	12 V	70 – 110 °C	950 hours

The magnitude of the temperature stress is incremented between 70 and 110 °C with a linear step-size of 10 °C for a total stress time duration of 950 hours. Figure 5.1 shows that both the lowest and highest temperature stress is kept constant applied for 200 hours. However, from 80 °C to 110 °C, the thermal step-stress was observed at different stress time (i.e., 300, 531 and 645 hours, respectively). A total of twelve test samples (i.e., T1-T6 and S1-S6) were considered to obtain an accurate enough estimation of the EMC performance degradation caused by the accelerated aging process. Both L78L05 and UA78L05 were selected to compare the lifetime reliability based on the drift observed on the conducted EMC measurement degradation due to the aging impact maintained during the ADTs. Hence, sufficient number of IC components (i.e., 6 units) for both L78L05 and UA78L05

analog devices were selected instead of a single sample for observing EMC level dispersion between the tested samples, which could provide a clear reflection on the EMR characteristics of the DUTs that belongs to the entire family of the L78L05 and UA78L05.

Table 5.1 shows a similar thermal stress magnitude and duration with two different constant electrical overstresses voltage levels (i.e., 9 V and 12 V) applied on the IC samples. Among the six L7805 samples, S1, S2 and S3 were selected for aging at 9 V, and the rest of the three IC samples (i.e., S4, S5 and S6) were subjected to aging at constant 12 V electrical overstress condition. Similarly, three samples (i.e., T1, T2 and T3) of UA78L05 were subjected to low electrical overstress, while the rest of the UA78L05 samples (i.e., T4, T5 and T6) were allowed to undergo through the accelerated aging process under high electrical overstress condition during the ADT performed inside the thermal climatic chamber. Note that, temperature stress of same magnitude was applied continuously to all these selected DUTs for the same stress time according to the step-stress ADT plan demonstrated in the Figure 5.1. It should be stated that since for input voltages within the range of 15 to 20 V all the IC samples were crashed after 200 hours of aging under the first thermal stress magnitude (i.e., 70 °C), V_{in} stress of 20% and 60% higher than the selected 7.5 V applied voltage in nominal operating condition was considered in the ADT plan. It is worth mentioning that the repeatability of the measured EMC performance results of the tested DUTs samples was also considered during the design of the ADT plan.

5.3.2 Measurement setup and procedure

The experimental setup to perform the ADT on the selected IC samples is displayed in Figure 5.2. The high temperature stress was applied on the DUTs inside the climatic chamber. The host computer was used to program the temperature-controlled Spiral V software integrated with the climatic chamber (Figure 5.2a) to implement the designed ADT plan. Multi-channel DC analog voltage power supplies were utilized to provide constant electrical voltage stress into the DC V_{in} pin of the tested ICs. High temperature aging cables (i.e., Amperol RF 095−902−466−004) [51] were connected to the external DC power supply cables outside the climatic chamber via the connectors as shown in the Figure 5.2a. These thermal resistant aging cables [51] were connected to the tested samples inside the climatic chamber to inject both low and high electrical overstress voltage levels into the V_{in} pin 8 of the tested DUTs (Figure 5.2b). This aging cable differ from the DC power supply cable in terms of their ability to withstand very high temperature maintai-

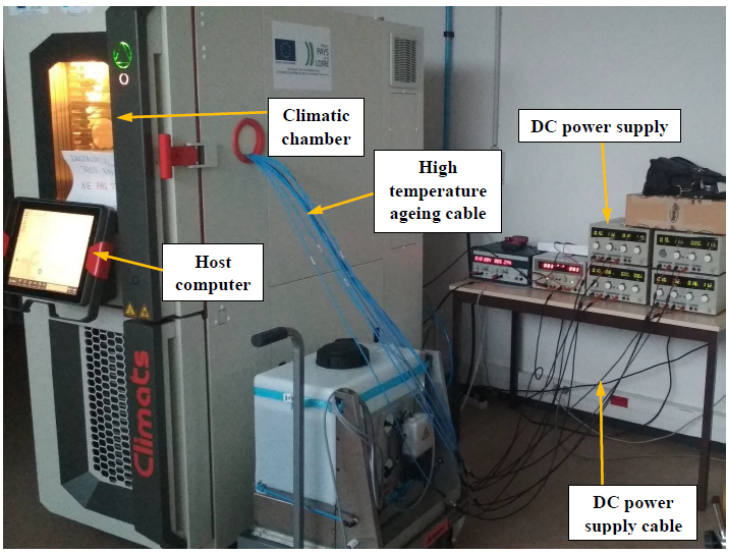
ned inside the climatic chamber without undergoing into corrosion or any other kind of physical damage. These high temperature cables were chosen for the purpose of maintaining extreme temperatures inside the climatic chamber, while performing the ADTs on the tested IC samples.

5.3.3 Experimental methodology

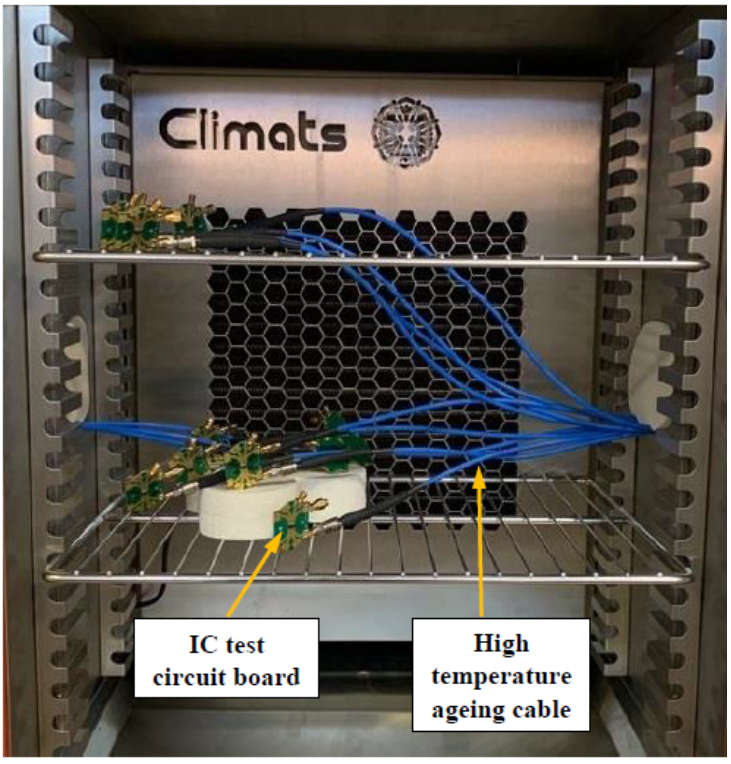
The aging stress time-dependent ADTs was conducted on the DUTs inside the climatic chamber to ensure permanent degradation induced by the applied stress conditions. During the accelerated aging process, after a certain stress duration according to the methodology shown in Figure 5.3, the process was paused and DPI tests were performed on all the fresh and aged DUTs to evaluate the conducted immunity variations. The process was then resumed until the completion of the ADT plan.

Stress-measurement-stress refers to the repetitive cycle of applying both thermal and electrical aging stress on the IC samples inside the climatic chamber during the ADT for a fixed aging stress-time (T'), followed by removing the stress and performing the DPI test on these aged samples outside the climatic chamber under the nominal conditions (i.e., 25 °C and 7.5 V) for a very short t period. Note that, little time duration of t was maintained compared to that of the T' hours in order to ensure that the aged ICs would not undergo into partial recovery from the permanent degradation induced by the ADTs. Prior to simultaneously applying the thermal step-stress and electrical overstress in the climatic chamber, the DPI experiments were performed separately on each individual L78L05 and UA78L05 fresh samples.

This conducted immunity measurement test was conducted for t duration, and the measurement data (i.e., P_{inj} and frequency) were recorded prior to resuming the aging process of those DUTs. The EMC capacity of the aged IC samples were characterized at different stress duration (i.e., 100, 200, 300, 531, 645, 750, 850 and 950 hours) as shown in Figure 5.3. The recorded DPI measurement data of those aged samples were then processed statistically to compute and compare with the fresh ones to investigate the long-term EMC robustness of these tested ICs by analyzing and modeling the conducted immunity performance degradation at different aging stress magnitude and time intervals. It is worth mentioning that all of the tested DUTs of UA78L05 and L78L05 remained operational and did not exhibit permanent failures after the ADTs were completed.



(a)



(b)

FIGURE 5.2 – Experimental test setup : (a) outside and (b) inside views of the climatic chamber.

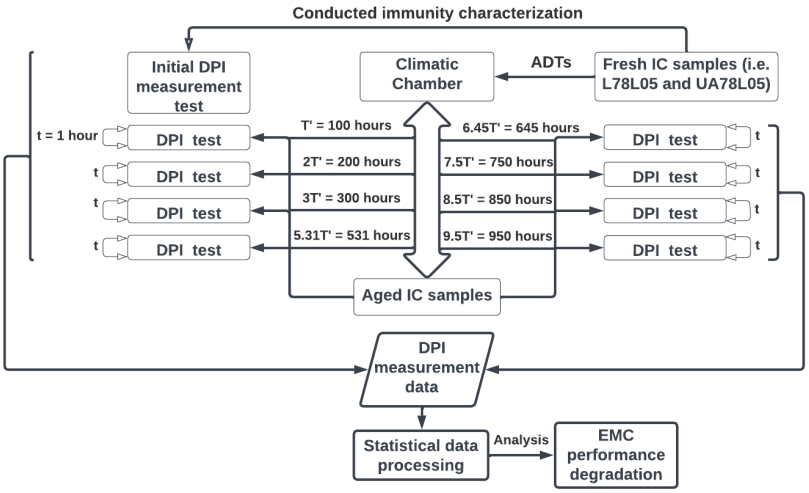


FIGURE 5.3 – Time-dependent accelerated aging methodology.

5.3.4 DPI test procedure and measurement algorithm

The DPI test measurement setup is similar to that presented in [60] is implemented with the measurement algorithm shown in Figure 5.4b. Figure 5.4a shows the standard DPI test-bench setup consisting of the DPI equipments for characterizing the conducted immunity of the DUT. The standard DPI test bench setup consist of the RF signal generator, RF amplifier integrated with the bi-directional coupler, power meters and the bias tee (i.e., inductor with decoupling capacitor) to form the injection network to couple RF signal on the DC power supply line of the DUT (Figure 5.4a). This injection network provides an efficient coupling mechanism with the pin under test (PUT) of the tested sample by the use of bias-tee with high impedance inductance connection in series with the coupling capacitor. The standard DPI experimental methodology was performed in accordance to the IEC 62132-4 standard [16].

The LabVIEW software, which is integrated with the DPI test bench, has been programmed based on the DPI algorithm to measure and record the relevant DPI data (i.e., P_{inj}) at different corresponding DPI frequencies. The flowchart of the DPI measurement algorithm is displayed in Figure 5.4b. The step-by-step procedures required to implement this algorithm is mentioned as follows :

1. choose the minimum and the maximum generated power of the RF signal, which is denoted by P_{min} and P_{max}, respectively.

2. select both the initial and final frequency of the amplified RF signal, ranging between 10 and 1000 MHz.
3. define the DPI failure criterion (i.e., ±4%) deviation from the nominal output voltage (V_{out}) on all the DUTs.
4. considering a fixed DPI frequency, vary the generated power of the RF signal between −40 dBm and +13 dBm with a linear increment of 1 dBm.
5. check if the defined failure threshold criterion is reached for any specific generated power and the DPI frequency value.
6. when the DPI failure occurs due to the DC offset (i.e., ±0.2 V) variation at the V_{out} pin 1 of the tested samples occurs, measure and record the forward power, reflected power using the power meters, and the minimum P_{inj} coupled to the V_{in} pin 8 of the DPI at the corresponding frequency.
7. vary the DPI frequency (f) between the initial and final value with a linear step-size of 10 MHz. Repeat the above measurement steps to record the computed P_{inj} at each corresponding DPI frequency values.

5.4 Experimental Results and Analysis of Analog ICs

This section presents the DPI measurement results performed on the tested DUTs before and after the accelerated aging at different stress duration. The evolution of the conducted immunity drift under the influence of aging induced by the defined stress conditions applied on the 6 samples of L78L05 and UA78L05 at various stress duration has been discussed.

5.4.1 Conducted immunity characterization of the analog DUTs

The conducted immunity data (i.e., P_{inj}) at each corresponding DPI frequency f values of both L78L05 and UA78L05 tested samples, aged at different stress time durations, were measured and compared with the fresh ones to observe evolution of the conducted immunity level under the influence of the defined accelerated aging multiple stress conditions. Fig 5.5 compares the variation of the conducted immunity level of T3 and T6 samples aged under low and high electrical overstress, while maintaining the same thermal step-stress condition. The minimum P_{inj} required on the V_{in} pin to cause DPI

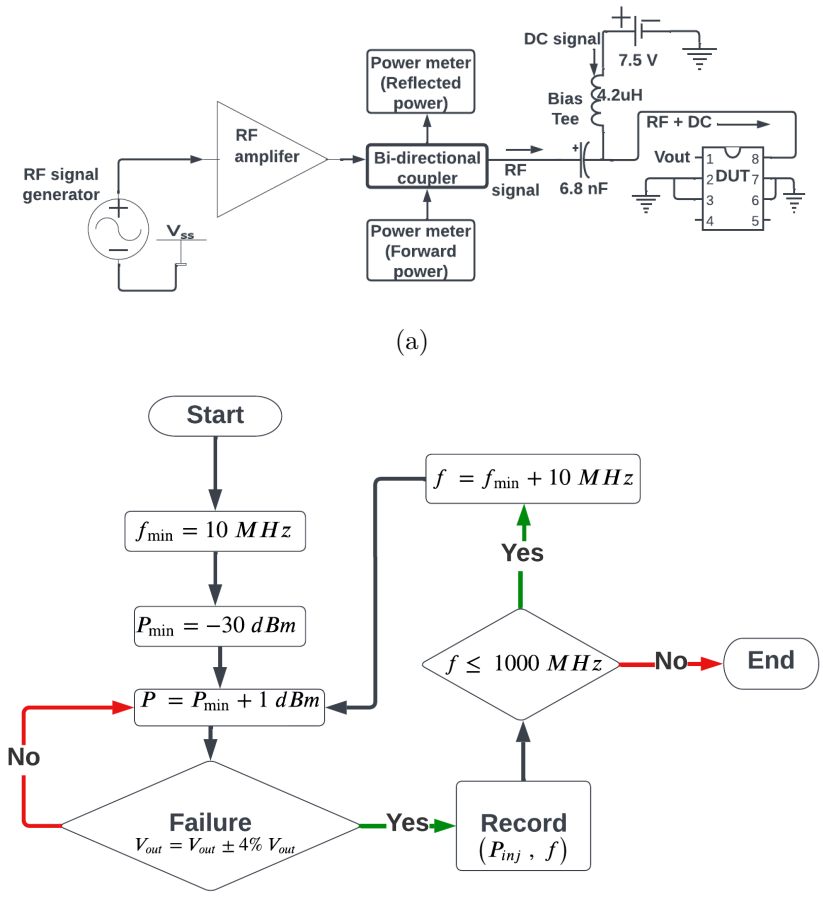
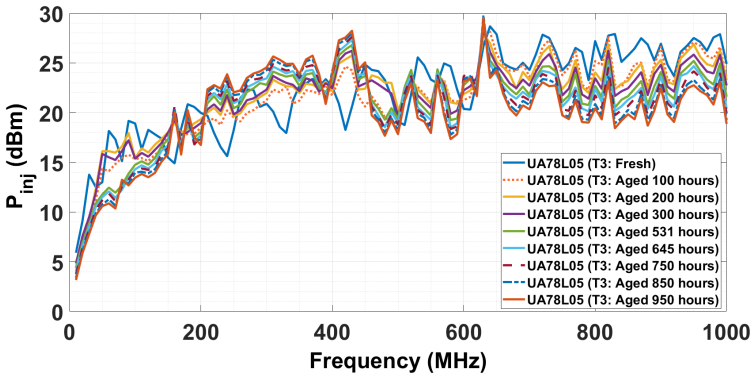


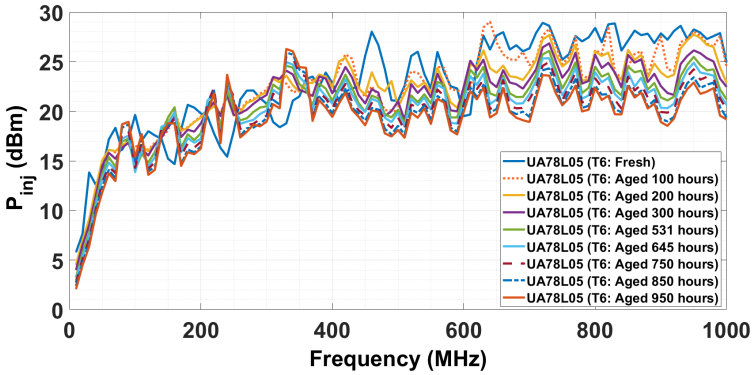
FIGURE 5.4 – (a) DPI test bench setup, (b) flowchart of the DPI measurement algorithm.

failure varied with DPI frequency at different aging stress intervals. At the high DPI frequency range (600-1000 MHz), both aged T3 and T6 samples demonstrated a monotonic decline in the level of conducted immunity compared to the fresh samples. This is because both the aged T3 and T6 samples required less P_{inj} to reach the defined failure threshold criterion than their fresh ones.

Figures 5.5a and 5.5b depict a set of conducted immunity curves in the frequency domain that exhibit a similar trend based on the magnitude and duration of stress. As aging stress time increased, the measured P_{inj} values for both aged T3 and T6 declined at all corresponding frequencies between 600 and 1000 MHz. Nonetheless, the T6 sample aged at high electrical overstress (i.e., 12 V) demonstrated weaker immunity to harmonic disturbance injection than the T3 sample aged at low electrical overstress (i.e., 9 V). After



(a)



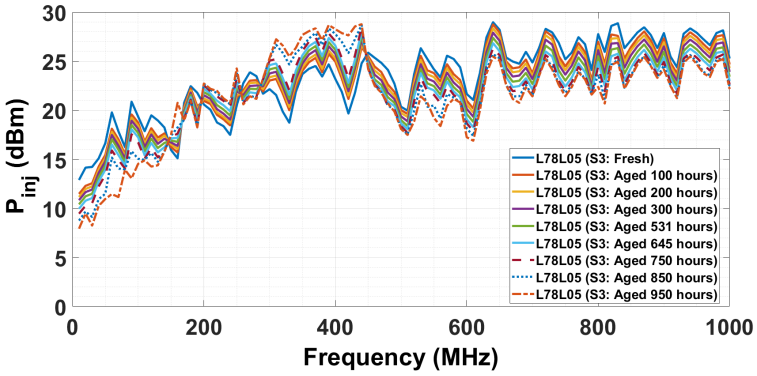
(b)

FIGURE 5.5 – Evolution of the conducted immunity level of UA78L05 samples at various stress duration caused by the identical thermal step-stress and (a) low ; (b) high voltage overstress.

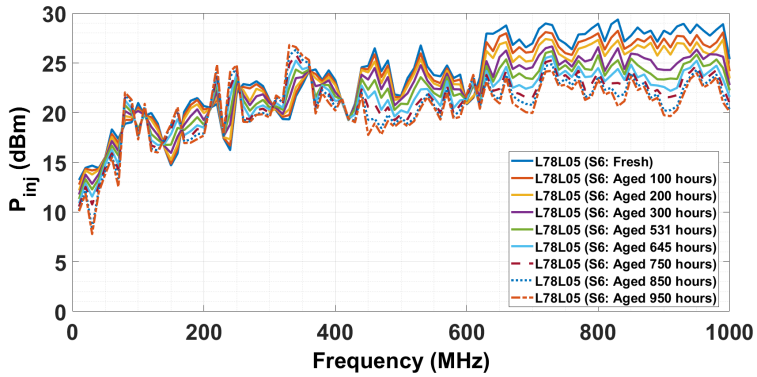
950 hours of cumulative stress, the absolute mean P_inj of the aged T6 DUT decreased by 4.7 dB over the entire DPI frequency range, compared to 4.3 dB for the aged T3 sample. It should be noted that the evolution of EMC performance is affected by both the aging stress time and the f values. Since it was determined that the P_inj of the fresh state was lower than that of the aged state depending on the f range at various stress times, the conducted immunity of the aged T3 improved at low frequencies (i.e., 200-480MHz).

The aforementioned effect of aging on the EMC level was also observed in samples S3 and S6 as shown in Figure 5.6, which illustrates the variation of the P_{inj} across the entire DPI frequency range (i.e., 10-1000 MHz). Both the Figures 5.6a and 5.6b illustrate an increasing and decreasing trend in the conducted immunity level in the low frequency bands (i.e., 10-440 MHz) for the aged S3 and S6 samples. As a function of stress duration,

the P_{inj} of aged S3 and S6 declined at each f values between 450 and 1000 MHz. The aged S3 sample, on the other hand, displayed higher EMC robustness than the aged S6 sample. When the S3 was aged at 9 V for 950 hours compared to that of the 12 V electrical stress applied to the S6, the average P_{inj} of the fresh S3 and S6 samples fell by 3.9 dB and 4.4 dB throughout the whole DPI frequency range, respectively.



(a)



(b)

FIGURE 5.6 – Evolution of the conducted immunity level of L78L05 samples at various stress duration caused by the identical thermal step-stress and (a) low ; (b) high voltage overstress.

Both the fresh and aged L78L05 samples were found to be more immune to the harmonic disturbance signal compared to those UA78L05 tested samples. Prior to the start of the ADT, the fresh S3 and S6 samples were able to withstand greater P_{inj} at each DPI frequencies than the T3 and T6 samples, respectively. Moreover, when compared to the T3 and T6 samples, the aged S3 and S6 DUTs exhibited 9.3% and 6.4% smaller variation in the mean P_{inj} measured from 10 MHz to 1000 MHz between 100 and 950 hours. The

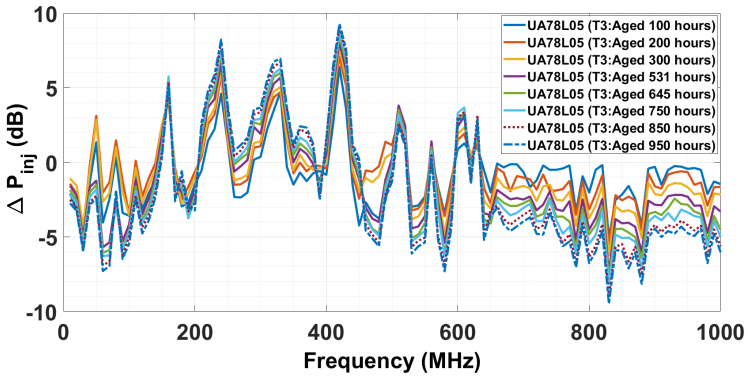
conducted immunity of the aged IC samples (T3, T6, S3, and S6) improved compared to those before ageing, as evaluated by the P_{inj} at corresponding f values within the low frequency band (i.e., 10–400 MHz). It is worth noting that all of the other examined UA78L05 and L78L05 samples showed a comparable variation of the measured P_inj as a function of both the f and the stress time duration. Consequently, all the tested DUTs exhibited comparable EMC performance degradation as a result of the global aging impact caused by the permanent intrinsic degradation effects.

This observed variation in the EMC performance level between the samples of the UA78L05 and L78L05 could be attributed to process variations among these tested samples (Figures 5.5 and 5.6), as a result of the different length, width, and types of internal identical CMOS transistors used in the designing stage. In addition, the use of different packaging and fabrication techniques during the manufacturing and production phase of these IC samples might play a significant role in the process dispersion, allowing numerical deviations in the internal parameters (i.e., I_{on}, V_{th}, μ_{eff}, gain) of these internal transistors due to aging.

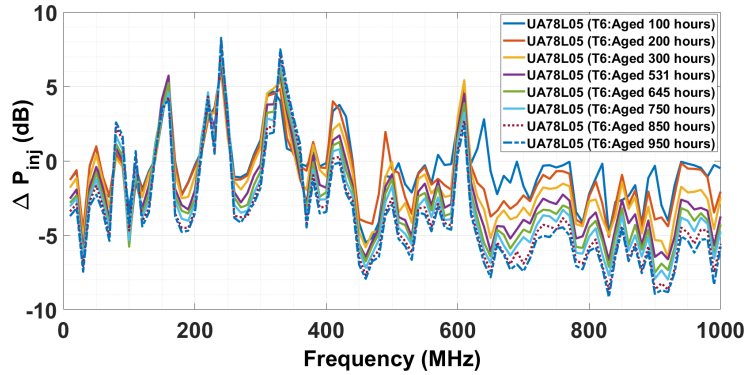
5.4.2 Conducted immunity drift of the aged analog ICs

The DPI measurement tests were performed on all the selected fresh and aged DUT samples of UA78L05 and L78L05 to measure the P_{inj} data at each corresponding DPI frequency value. Power injected drift (ΔP_{inj}) caused by accelerated aging was calculated for each DPI frequency value ranging from 10 to 1000 MHz to investigate the impact of aging on the deviation of the conducted immunity level at different aging stress times. The corresponding ΔP_{inj} data was extracted at each tested frequency by subtracting the measured P_{inj} of the fresh sample from that of the aged state.

Figure 5.7 compares the ΔP_{inj} as a function of DPI frequency at different thermal step-stress time intervals. A negative (positive) drift implies reduction (improvement) in the conducted immunity level of the aged samples. At different frequencies ranging from 10 to 630 MHz, both positive and negative ΔP_{inj} values were obtained, whereas only negative ΔP_{inj} values were obtained for the remaining tested frequency values up to 1000 MHz. These observations are evident in both Figures. 5.7a and 5.7b, which is a result of the decline in the conducted immunity level of the aged samples of UA78L05. Positive ΔP_{inj} data was extracted in the low DPI frequencies, implying that the conducted immunity level of both the T3 and T6 samples improved significantly after aging. Similarly, at various aging stress time periods, negative ΔP_{inj} values were calculated because the



(a)

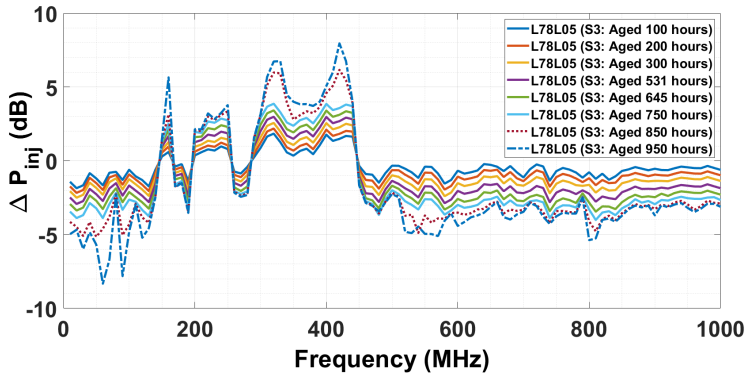


(b)

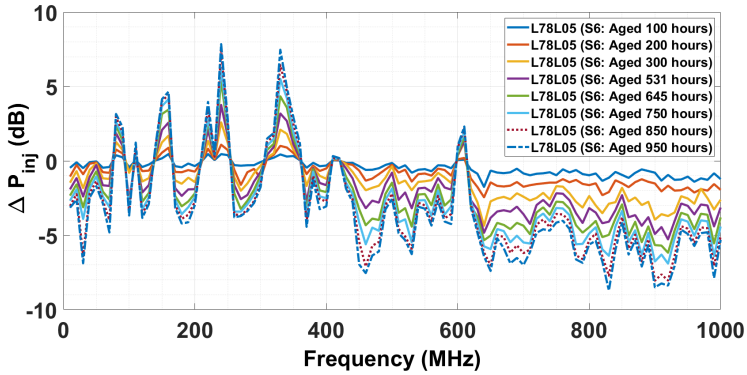
FIGURE 5.7 – Conducted immunity level drift of UA78L05 samples at various stress duration caused by the thermal step-stress as well as (a) low and (b) high voltage overstress.

measured P_{inj} of fresh T3 and T6 samples was found to be higher than those of aged states, indicating that the conducted immunity level of these DUTs degraded over the duration of the thermal step-stess ADT.

Figure 5.7a illustrates that the absolute mean ΔP_{inj} of the aged T3 sample increased between 1.7 and 4.3 dB over the whole frequency range, while the absolute average ΔP_{inj} for the T6 reached from 1.8 dB to 4.7 dB between 100 and 950 hours as shown in the Figure 5.7b. It should be noted that, depending on the magnitude and duration of the stress, all of the other tested UA78L05 samples showed a comparable evolution on the ΔP_{inj} across the whole measured frequency range. Figure 5.8a demonstrates a lower mean immunity level drift at every stress duration, reaching an absolute value of 3.9 dB at the end of the thermal step-stress ADT compared to the 4.4 dB extracted over the entire frequency range of interest as shown in Figure 5.8b. Hence, the S6 was



(a)



(b)

FIGURE 5.8 – Conducted immunity level drift of L78L05 samples at various stress duration caused by the thermal step-stress as well as (a) low and (b) high electrical overstress.

found to be less immune than that of the tested S3 after the accelerated aging test. It is worth mentioning that all the other selected tested samples of both UA78L05 and L78L05 showed similar evolution on the conducted ΔP_{inj} data across the entire tested frequency domain, depending on the applied magnitude and duration of the stress. Hence, these samples demonstrated considerable EMC performance degradation with noticeable computed mean EMC conducted immunity deviation between the DUTs. This observed dispersion in the EMC performance level among the DUTs of the tested ICs can be due to the process variations between these tested samples, which leads to the numerical variations of the internal transistor parameters (i.e., I_{on}, length, width, current gain) of the identical CMOS transistors with similar functionality but different references used in the design phase. Moreover, the origin of the observed EMC degradation behavior can be either due to the modification of the internal NMOS and PMOS transistor's electrical

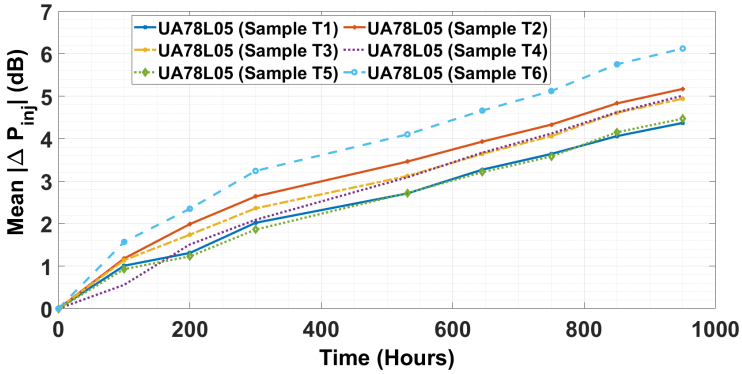
parameters (i.e., V_{th} and μ_{eff}), different manufacturing date, or different physical failure mechanisms (i.e., gate oxide defect, electromigration, and mobile ion contamination) leading to cracks and holes in their internal structure (e.g., gate oxide and metal layers) [33] [58]. Therefore, those prevalent intrinsic failures of CMOS circuit transistors within the tested ICs are responsible for the internal parametric drift, resulting in a significant EMC level drift caused by aging. The influence of higher number of samples was confirmed to have no impact on the EMC dispersion between the tested samples. Nevertheless, an increase in the number of DUTs, on the other hand, would allow for more measurement data on EMC degradation and lifetime failures, which might further improve the accuracy of predicting the proposed reliability model's unknown parameters and widen its confidence interval to predict the failure probability distribution of the developed model.

5.5 Degradation Path Modeling and Pseudo Lifetime Estimation of Analog ICs

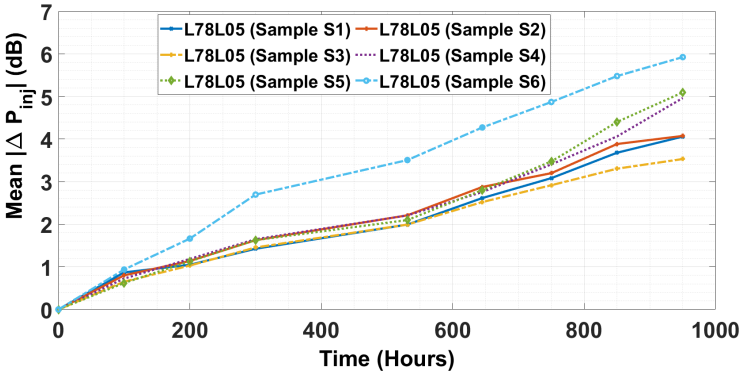
This section presents the evolution of the EMC performance degradation paths of both the tested analog ICs samples as a function of time. Besides, depending on the trend in the observed degradation of the conducted immunity of these aged DUTs under the influence of the applied ADTs plan, degradation path model have been developed to fit the measured degradation data. Linear regression analysis is applied to obtain the mathematical relationship between the selected degradation parameter and stress time. It is worth to mention that the unique degradation paths could be produced for each individual tested analog and digital circuit samples. The behaviour of these degradation paths could be modeled mathematically. The unknown parameters of the defined mathematical model for each degradation paths were estimated, prior to determining the pseudo failure time. The pseudo TTF was determined for all the considered analog and digital DUTs based on the user-defined degradation failure criterion. Note that, degradation failure criterion or the failure threshold is expressed in percentile that refers to the deviation of the selected EMC degradation parameter (i.e., ΔP_{inj}) from that of the actual power injected before ageing.

Figure 5.9 depicts the EMC performance degradation curves of all the tested samples as a function of the aging stress time. Since the ΔP_{inj} of the aged DUTs was dependent on both frequency and stress time, mean absolute injected power drift ($|\Delta P_{inj}|$), computed at various stress time by taking the average of the absolute ΔP_{inj} data for every corres-

ponding frequency, was considered the suitable EMC performance degradation indicator parameter. At each thermal and voltage stress magnitude and duration, the corresponding EMC degradation data was characterized by evaluating the magnitude of the mean $|\Delta P_{inj}|$ over the high frequency range (i.e., 600-1000 MHz). The latter band was chosen due to the continuous monotonic immunity degradation (Figures 5.7 and 5.8), which leads to model the EMC degradation behavior of the DUTs with higher accuracy.



(a)



(b)

FIGURE 5.9 – Conducted immunity degradation as a function of the stress time on the tested samples of (a) UA78L05, (b) L78L05.

Figures 5.9a and 5.9b show significant increment of the mean $|\Delta P_{inj}|$ (having a higher positive slope in UA78L05 compared to L78L05 samples) with increasing stress duration under the defined ADT plan. The immunity degradation of both UA78L05 and L78L05 could be compared by highlighting the noticeable difference in the mean $|\Delta P_{inj}|$ depending on the applied stress time. The aged T6 showed highest variation in the mean $|\Delta P_{inj}|$ compared to the other tested samples in every stress time intervals, reaching a maximum

value of 6.12 dB at 950 hours (Figure 5.9a). However, lower mean $|\Delta P_{inj}|$ values over the high desired frequency range could be observed for the L78L05 sample ICs (Figure 5.9b). After the completion of 950 hours, the aged L78L05 samples S3 and S6 demonstrated a 28.5% and 3.26% lower immunity degradation compared to those of the aged UA78L05 T3 and T6, respectively.

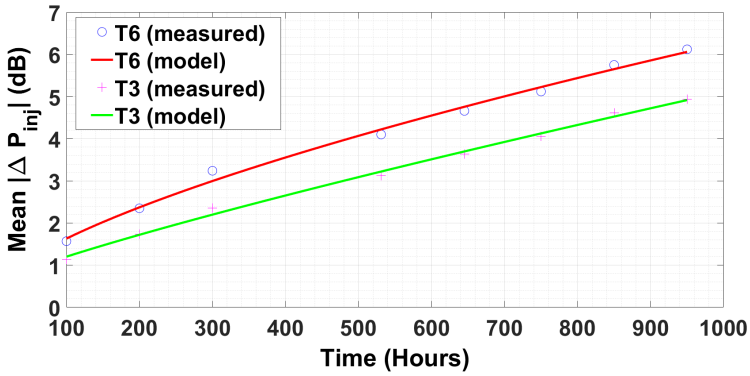
Figure 5.10 showcases the good agreement between the generated degradation paths fitted to the measured EMC degradation data by performing linear regression technique as shown in Figure 5.9 for two samples of UA78L05 and L78L05 at different stress duration. The degradation paths generated for T3 and T6 differ from each other depending on the computed mean $|\Delta P_{inj}|$ data based on the applied step-stress ADT conditions (Figure 5.10a). The similar monotonic degradation increasing with stress duration trend implies that the same degradation model could be employed for both UA78L05 and L78L05 ICs to estimate the unknown relevant parameters of the model, predicting the conducted immunity degradation. The simplified proposed mathematical model representing the monotonic degradation observed in Figure 5.10 is expressed in equation (5.1), where $g_{ikl}(t)$ corresponds to the degradation function of stress magnitude and duration (t) for component i, level of input voltage k and level of temperature l, A_{ikl} and γ are the stress dependent unknown coefficients. Note that the similar mathematical expression was also found in [26], which considered the power MOSFET law to explain behaviour of the stress-dependent degradation path.

$$g_{ikl}(t) = A_{ikl} \times t^{\gamma} \tag{5.1}$$

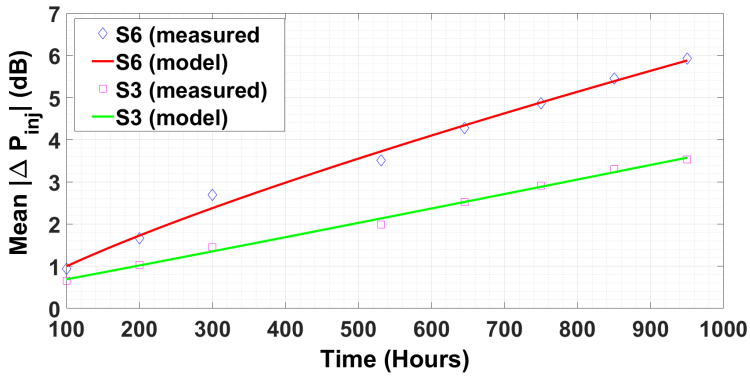
Applying the linear regression analysis to generate the best-fit degradation path curves (Figure 5.10) allowed for the determination of the mathematical relationship between the absolute mean ΔP_{inj} and stress time (t), with a time exponent stress-dependent (γ) variable used in (5.1). The typical numerical value for the γ parameter was found to be 0.64 and 0.51 for T3 and T6, respectively (Figure 5.10a). On the other hand, the γ parameter for L78L05 (i.e., S3 and S6) degradation path curves were 0.75 and 0.80, respectively (Figure 5.10b. Hence, these above aforementioned numerical values could be considered to be comparable to that of stated in [26]. It is worth mentioning that the typical value of the defined time exponent γ parameter varies depending on the specified stress conditions.

It is worth mentioning that all the other tested analog regulator ICs were observed to show such increasing trend in their corresponding degradation paths as observed for

UA78L05 (i.e., T6 and T3) and L78L05 (i.e., S6 and S3), depending on the applied multiple ageing stress conditions. The unknown parameters (i.e., γ and A_{ikl}) of each corresponding degradation paths were estimated by applying the linear curve fitting method. When the observed EMC degradation path reaches the defined failure threshold G criterion (i.e., 15%) in the nominal condition (Figure 5.10), the corresponding pseudo TTF of the tested DUTs could be determined by considering the G as the ratio of mean $|\Delta P_{inj}|$ to that of mean P_{inj} at different DPI measurement time.



(a)



(b)

FIGURE 5.10 – Degradation path fitted to the EMC degradation data of ICs samples (a) UA78L05, (b) L78L05.

5.6 Accelerated Life Test (ALT) Modeling and Analysis of Analog ICs

This section presents the ALT modeling methodology based on the EMC performance degradation data obtained on the tested DUTs. This developed ALT model is used to estimate unknown ALT model parameters and predict the lifetime reliability of the aged IC regulators under the influence of different constant electrical overstress conditions and the failure G criterion considered on the conducted immunity degradation of the tested IC samples.

5.6.1 ALT reliability modeling and parameter estimation

Inverse-power voltage (IPV) law and the temperature dependent Eyring ALT models were used to develop a quantifiable life-stress model to predict the lifetime stress data [30]. The Eyring model is the modified Arrhenius ALT model, which can be mathematically expressed as a function of the temperature stress only, as can be seen in (5.2), where $L(T)$ refers to the lifetime data that can be computed as a function of single stress T, A_x and B_x are the stress-dependent unknown model constants. The IPV acceleration law model due the voltage stress only can be expressed in (5.3), where $L(V)$ represents the lifetime of a component as a function of voltage stress only that increases the acceleration factor and performance degradation of the DUT, C and n refers to the model parameters that can be determined analytically by using different statistical PoF distribution (i.e., exponential, log-normal and Weibull) function. Applying the Weibull failure probability distribution function on the degradation is considered to be suitable for obtaining useful information on the failure trend due to various failure mechanisms and for characterizing both the useful life and wear-out phase in the bathtub curve of the tested samples [85]. Equation (5.4), natural logarithmic form in (5.4), is the combination of equations (5.2) and (5.3) to develop a mathematical model for the lifetime multiple stress parameters dependent acceleration model. The analytical expression in (5.4) also contains unknown model constants (C_x, n and B_x), which can be estimated with high precision depending on the accuracy of the model.

$$L(T) = \frac{1}{T} e^{-(A_x - \frac{B_x}{T})} \tag{5.2}$$

$$L(V) = \frac{1}{C_x V^n} \tag{5.3}$$

$$L(T,V) = \frac{A_x}{V^n} e^{\frac{B_x}{T}} \tag{5.4}$$

Equation (5.5) is considered the location parameter (μ_x), which refers to the mean TTF of the tested sample. Thus, equation (5.5) was modified, and the proposed lifetime acceleration model was developed as expressed in (5.6), where $\mu_x(V,T,G)$ is a function of three independent variables, i.e., voltage V and temperature T stresses while considering G as the failure threshold constraint, and α_{x_0}, α_{x_1}, α_{x_2} and α_{x_3} are the stress-dependent model constants. According to Figure 5.10, the influence of V stress can be seen to be more significant compared to T, hence, equation (5.6) can be further simplified to (5.7) for a fixed G criterion.

$$\mu_x(V,T,G) = \ln L(T,V) = \ln A_x - n \ln V + \frac{B_x}{T} \tag{5.5}$$

$$\begin{aligned} \mu_x(V,T,G) &= \ln L(T,V,G) \\ &= \alpha_{x_0} + \alpha_{x_1} \ln(V) + \alpha_{x_2} G + \alpha_{x_3} \frac{1}{T} \end{aligned} \tag{5.6}$$

$$\mu_x(V,G) = \alpha_{x_0} + \alpha_{x_1} \ln(V) + \alpha_{x_2} G \tag{5.7}$$

In order to construct the reliability model of the DUTs, the combination of applying the Weibull's distribution on the proposed lifetime ALT model expressed in (5.7) for extracting the relevant ALT model constants and estimating reliability parameters with good accuracy for the defined accelerated tested conditions were considered. The expressions for the CDF, PDF, and natural logarithmic form of the PDF of the Weibull distribution are respectively given in (5.8), (5.9) and (5.10), where η and β_w refer to the scale and

shape parameters, respectively. The overall combination of the proposed ALT−Weibull reliability model can be then expressed by substituting the ALT proposed model for the applied V and G mentioned in (5.7) into the term $\ln\eta$ in (5.10). Hence, the simplified analytical expression for the developed ALT−Weibull reliability model is given in (5.11), with unknown model parameters of α_{x_0}, α_{x_1}, α_{x_2}, β_w and η.

$$F_w(t) = 1 - e^{-(t/\eta)^{\beta_w}} \tag{5.8}$$

$$f_w(t) = \frac{\beta_w}{\eta} \cdot \left(\frac{t}{\eta}\right)^{\beta_w - 1} \cdot e^{-\left(\frac{t}{\eta}\right)^{\beta_w}} \tag{5.9}$$

$$\ln f_w(t) = \ln\beta_w - \ln\eta + (\beta_w - 1)(\ln t - \ln\eta) - \left(\frac{t}{\eta}\right)^{\beta_w} \tag{5.10}$$

$$\ln f_w(t) = \ln\beta_w - \mu(V,G) + (\beta_w - 1)[\ln t - \mu(V,G)] - \left(\frac{t}{\eta}\right)^{\beta_w} \tag{5.11}$$

TABLE 5.2 – ALT Reliability Model Parameters for both L78L05 and UA78L05

Model parameters	**IC reference**	
	UA78L05	**L78L05**
$\boldsymbol{\alpha_{x0}}$	3.46	6.04
$\boldsymbol{\alpha_{x1}}$	0.16	0.14
$\boldsymbol{\alpha_{x2}}$	0.41	-0.57
$\boldsymbol{\beta_w}$	4.60	6.83
$\boldsymbol{\eta}$	694.85	1074.17
$\boldsymbol{L_f}$	-105.69	-102.30

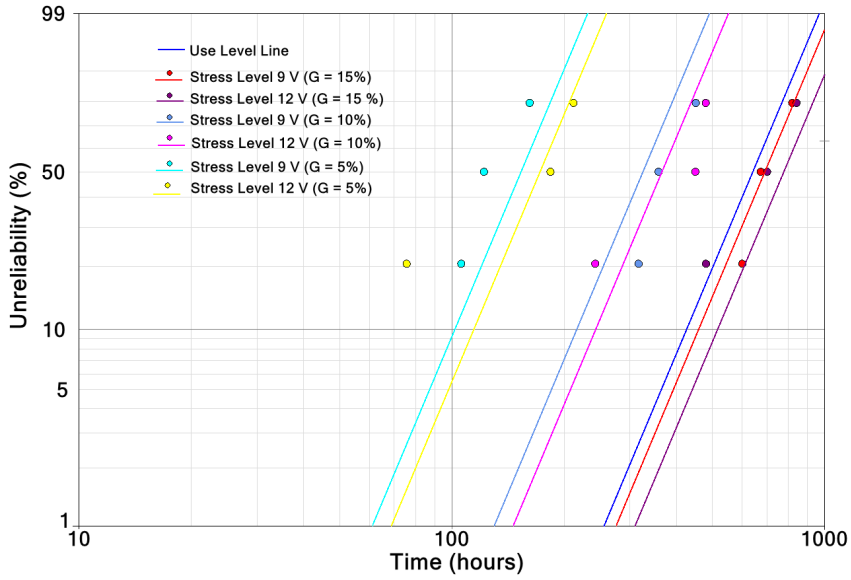
Considering the EMC performance for all the tested sample size of both UA78L05 and L78L05, those unknown parameters were obtained for both DUTs by applying the MLE method on the developed ALT−Weibull model (5.11). With the help of the Weibull distribution, which is applied on the pseudo TTF data obtained from the degradation

data measurements under the specified G and V conditions, the MLE method allows to estimate these reliability model parameters. Table 5.2 provides the estimated values for the proposed reliability model parameters under the nominal conditions of 7.5 V and 15% criteria on the evaluated EMC degradation data for the tested samples of both L78L05 and UA78L05. The almost close L_f values for both L78L05 and UA78L05 regulators implies that the model fits to the data measurements of the tested ICs. Moreover, significant difference in the scale parameter η of the Weibull distribution might be due to the different model constants obtained by Weibull++ software under the defined accelerated life test conditions. The positive and greater than one β_w value indicates that both L78L05 and UA78L05 DUTs were degraded in the bathtub curve's wear-out phase with increasing failure rate.

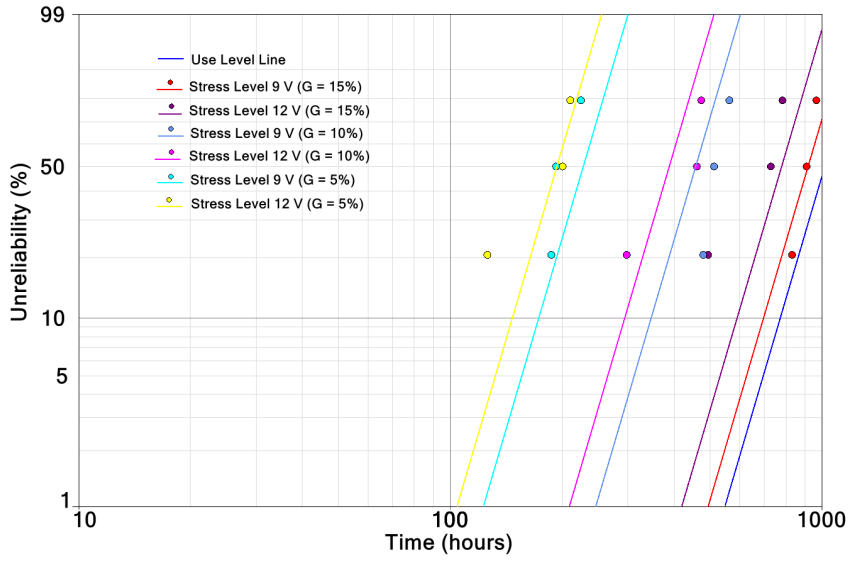
5.6.2 Reliability and life-data analysis of analog DUTs

The lifetime reliability of the tested samples is characterized under the impact of applying two different constant electrical voltage stresses (i.e., 9 V and 12 V) on both UA78L05 and L78L05 based on the EMC degradation observed during the ADTs. Figure 5.11 demonstrates the Weibull distribution plots of the unreliability function, which fits to the pseudo TTF degradation data of UA78L05 and L78L05 IC DUTs for two different stress conditions at three different G criterion (i.e., 5%, 10% and 15%). Time on the x-axis refers to the computed pseudo TTF based on the EMC degradation data under the specified threshold criterion, whereas the data points in the y-axis corresponds to the predicted unreliability (probability of failure). The logarithmic fits to these data points is represented by the parallel lines, which are produced due to applying the Weibull distribution on the proposed lifetime reliability model. This type of distribution displays the shape β_w parameter which is independent of the applied V stress levels and G constraints, and the scale η parameter that is dependent on both the considered different stress levels and G criterion. Note that the limited number of tested IC samples could be responsible for observing the mismatch between these parallel lines and the pseudo TTF data points as shown in Figures 5.11a and 5.11b. Figures 5.11a and 5.11b illustrate that higher lifetime unreliability is obtained at higher G criterion and lower V stress level. The best fit parallel lines were plotted in Figure 5.11 for different stress levels, considering the β_w parameter is fixed irrespective of the stress magnitude unlike the η parameter, but depends on the stress types applied on the tested IC samples. This limitation might be resolved by increasing the number of tested IC samples, which would minimize the observed discre-

pancy between a large number of TTF data points and logarithmic best-fit parallel lines, and the developed ALT model's precision could be enhanced.



(a)



(b)

FIGURE 5.11 – lifetime reliability Weibull distribution fits to pseudo failure time at different stress conditions applied on (a) UA78L05, (b) L78L05.

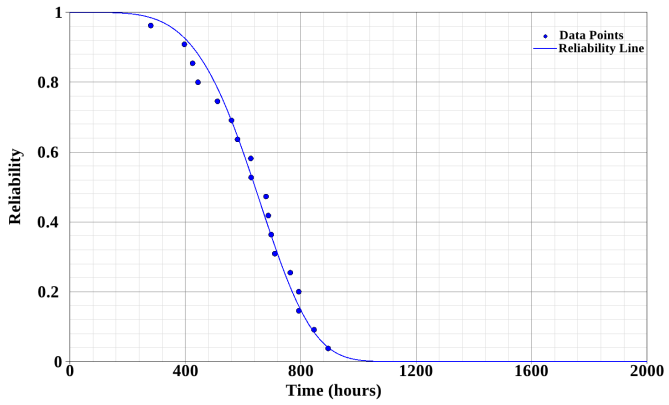
Figure 5.11a demonstrates the unreliability with corresponding pseudo TTF when all six samples were subjected to the defined G for both 9 V and 12 V stress levels above the

use level, which refers to the nominal conditions (i.e., 7.5 V and 25°C at 15% criterion). It can be observed that the unreliability of all tested samples varies from 20% to 80%, with a larger pseudo TTF for the 10% criterion (485 hours at 12 V with 80% unreliability) compared to the 5% (220 hours at 12 V with 80% unreliability). For a fixed G criterion, an inverse relationship between the considered voltage stress and pseudo TTF was noticed for samples of L78L05 compared to UA78L05 (Figure 5.11), which is due to the noticeable difference in the conducted immunity degradation of the tested DUTs.

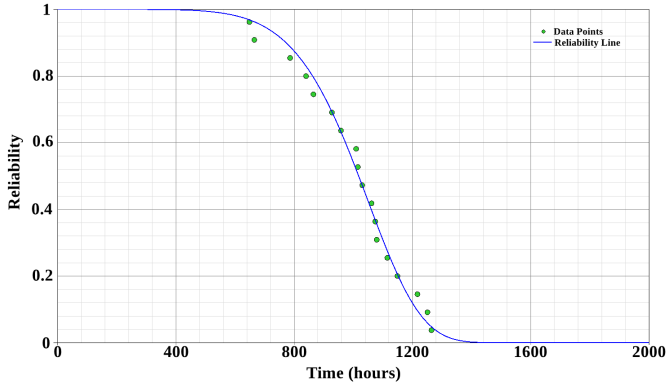
Figure 5.11b shows that at a fixed G criterion, the pseudo TTF of the majority of L78L05 samples is found to be greater at 12 V than that if at 9 V applied stress. Applying the proposed lifetime reliability model to the tested samples of L78L05, the greatest unreliability is observed at approximately 478 hours when a 10% failure criterion is applied to the EMC performance degradation of a single aged unit under 12 V overstress conditions. On the other hand, when applying the lower voltage stress level and G criterion, the sample is considered unreliable after 300 hours with the least unreliability. These observations in the unreliability plots would be due to the noticeable difference in the conducted immunity degradation of the tested UA78L05 and L78L05 DUTs.

Figure 5.12 shows the reliability (or survival probability) line best fits to the pseudo TTF data based on the EMC degradation of the tested samples under the influence of the defined failure G criterion and voltage stress conditions in nominal thermal condition. The reliability values on the y-axis corresponds to the non-failure probability for each data points against the pseudo TTF on the x-axis. Considering three different G criteria and applying two different voltage overstress levels, a total of 18 degradation data points were plotted for both UA78L05 and L78L05 samples. Considering 10% criterion at 12 V applied stress level, the 96% reliability and unreliability model functions for a tested sample occur at 245 and 850 pseudo TTF hours, respectively (Figure 5.12a). Thus, all the tested samples of UA78L05 subjected to different constraints would fail within the total applied stress duration. However, as observed in Figure 5.12b, unlike the UA78L05, in nominal condition, few tested L78L05 samples would fail beyond 1200 hours with a lifetime unreliability of around 84%. Hence, those samples would have the remaining life of only 16% having the survival probability of 0.16 while the constant stress is maintained and a fixed G threshold is defined on the degradation data.

Figure 5.12b shows similar behaviour of the proposed reliability model function, which decreases with increasing failure time expressed in hours and this reliability curve best fits to the degradation data points of the DUTs at 9 and 12 V stress magnitude. It is predicted



(a)



(b)

FIGURE 5.12 – Reliability function based on the proposed ALT model fits to the degradation data of (a) UA78L05, (b) L78L05.

that all the tested aged L78L05 samples would survive upto 100% until 400 hours, and the highest reliability or the lowest probability of failure is observed at 640 hours when the degradation data crosses or reaches the defined failure G level under the impact of applying a constant stress. Overall, the developed reliability model with an acceptable modeling accuracy can be validated by observing the best fitting of the reliability function curve to the measured lifetime to failure data points as illustrated in both Figs. 5.12a and 5.12b.

5.7 Step-stress ADT Modeling of Analog DUTs

Due to performing the step-stress ADT on a tested unit, the degradation path function at any stress time could be considered to be dependent only on the current accelerated

stress level applied for the specified time intervals and the observed cumulative degradation accumulated due to applying previous stress levels, but independent of the failure mechanisms, which are consistent under both accelerated and nominal stress conditions [73]. A physics-based approach for degradation modeling was used to estimate the unknown parameters of the selected degradation model and to depict the degradation path caused by the evolution of the monotonic degradation observed at different stress duration over the high frequency range (i.e., 600-1000 MHz) as shown in Figure 5.10.

The evolution of the degradation paths caused by the step-stress ADT was modeled by applying the logarithm in equation (5.1) that provides the expression for the $d_{ikl}(t)$ which is expressed as the logarithm of the ratio between the variation of the evaluated mean $|\Delta P_{inj}|$ and the computed nominal mean P_{inj} across the DPI frequency range for the fresh unit tested sample (i) before aging, voltage level (k) and temperature stress level (l) as shown in equation (5.12).

$$d_{ikl}(t) = \ln\left(\frac{\Delta P_{inj}}{P_{inj}}\right) = \ln(A_{ikl}) + \gamma \ln(t) \tag{5.12}$$

Considering the combined aging impact of the multiple stress factors (voltage and temperature), the term A_{ikl} can be expressed using the accelerated aging life-stress (i.e., Eyring) model as shown in equation 5.13.

$$\ln(A_{ikl}) = \ln(\alpha_i) - B \ln(V) + \frac{E_a}{KT} \tag{5.13}$$

considering component i, level of input voltage k and level of temperature l.

Equation (5.13) can be modified by substituting the expression of A_{ikl} to obtain the expression as shown in (5.14), which represents degradation path modeling under the combined influence of temperature T and electrical voltage V stress on the accelerated aging process.

$$d_{ikl}(t) = \ln\left(\frac{\Delta P_{inj}}{P_{inj}}\right) = \ln(\alpha_i) - B \ln(V) + \frac{E_a}{KT} + \gamma \ln(t) \tag{5.14}$$

Consequently, the proposed physics-based model for the degradation path $d_{ikl}(t)$ is expressed in (5.15), with unknown degradation parameters (i.e., β_1, β_2, β_3 and β_4).

$$d_{ikl}(t) = \beta_1 + \beta_2 \ln(V) + \beta_3 \frac{1}{T} + \beta_4 \ln(t) \tag{5.15}$$

By comparing and equating both equations (5.14) and (5.15), these unknown parameters can be determined as shown in (5.16), where β_1 is found by the normal distribution of μ_α and σ_α, E_a is the activation energy expressed in eV, K is the Boltzmann constant measured in eV/°C or eV/K. The best fits of this proposed degradation model to the EMC degradation data indicate that the modeling methodology is adequate enough to estimate the unknown variables B, α_i and γ.

$$\beta = \begin{cases} \beta_1 = \ln(\alpha_i), \text{where } \alpha_i \sim \ln(\mu, \sigma) \Rightarrow \ \beta_1 \sim \mathcal{N}(\mu_\alpha, \sigma_\alpha) \\ \beta_2 = -B \\ \beta_3 = \frac{E_a}{K} \\ \beta_4 = \gamma \end{cases} \tag{5.16}$$

Since thermal step-stress ADT was applied to the DUTs, the cumulative degradation path function for a tested sample unit due to thermal step-stress, denoted by $D_{ik}(t)$, can be represented by a series of mathematical expressions as shown in (5.17), where the term τ_m (m=1, 2, ..., 5) refers to the pseudo virtual time needed to obtain the step-stress ADT degradation path value due to the specified T stress level, and t_m refers to the time after which the T stress level increases linearly according to the step-stress ADT plan illustrated in Figure. 5.1.

$$D_{ik}(t) = \begin{cases} d_{ikl_1}(t) & \text{if } 0 \le t < t_1 \text{ at } 0 < t \le 200 \\ d_{ikl_2}(\tau_2 + t - t_1) & \text{if } t_1 \le t < t_2 \text{ at } 200 < t \le 300 \\ d_{ikl_3}(\tau_3 + t - t_2) & \text{if } t_2 \le t < t_3 \text{ at } 300 < t \le 531 \\ d_{ikl_4}(\tau_4 + t - t_3) & \text{if } t_3 \le t < t_4 \text{ at } 531 < t \le 750 \\ d_{ikl_5}(\tau_5 + t - t_4) & \text{if } t_4 \le t < t_5 \text{ at } 750 < t \le 950 \\ \vdots & \\ d_{ikl_{m-1}}(\tau_{m-1} + t_{m-1} - t_{m-2}) & \text{if } t_{m-1} < t <\le t_m \end{cases} \tag{5.17}$$

The pseudo virtual time τ_m can be derived by the general relationship between each degradation path functions at different time intervals as shown in equation (5.18). The

latter can be used to obtain τ_2 to τ_5 at different intervals of time and T.

$$\tau_m = \begin{cases} t_1 \quad m = 1 \\ (\tau_{m-1} + t_{m-1} - t_{m-2}) \exp\left(\frac{\beta_3}{\beta_4}\left(\frac{1}{T_{m-1}} - \frac{1}{T_m}\right)\right) \quad 2 \le m \le 5 \end{cases} \tag{5.18}$$

where,

$$\begin{aligned} \tau_2 &= \tau_1 \exp\left(\frac{\beta_3}{\beta_4}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) \quad \text{if } t_1 < t \le t_2 \text{ at } 200 < t \le 300 \\ \tau_3 &= (\tau_2 + t_2 - t_1) \exp\left(\frac{\beta_3}{\beta_4}\left(\frac{1}{T_2} - \frac{1}{T_3}\right)\right) \quad \text{if } t_2 < t \le t_3 \text{ at } 300 < t \le 531 \\ \tau_4 &= (\tau_3 + t_3 - t_2) \exp\left(\frac{\beta_3}{\beta_4}\left(\frac{1}{T_3} - \frac{1}{T_4}\right)\right) \quad \text{if } t_3 < t \le t_4 \text{ at } 531 < t \le 750 \\ \tau_5 &= (\tau_4 + t_4 - t_5) \exp\left(\frac{\beta_3}{\beta_4}\left(\frac{1}{T_4} - \frac{1}{T_5}\right)\right) \quad \text{if } t_4 < t \le t_5 \text{ at } 750 < t \le 950 \end{aligned}$$

In order to obtain the unknown parameters of the proposed degradation model, the analytic expression for the CDF was derived for one value of the applied thermal and electrical stress level as shown in (5.19), where theCDF is denoted by F_{ik}, and ϕ refers to the standard normal distribution of the CDF. This expression was determined based on the condition that the tested sample fail if the proposed $g_{ikl}(t)$, which is a function of t and T, reaches or exceeds the user-defined threshold (G) criterion based on the functionality outlined in the specifications, and the applications. The latter was considered the ratio of the mean $|\Delta P_{inj}|$ to that of the nominal mean P_{inj} of the fresh sample before the step-stress ADT. The performed immunity performance degradation data for all of the tested DUTs at various measurement time duration were taken into account (Figure 5.9). Consequently, for the purposes of this ADT modeling, G was calculated for each of the tested DUTs at different duration of stress time, taking the EMC degradation data into consideration. When the observed EMC performance degradation $d_{ikl}(t)$ reached the critical horizontal degradation level (D_v) at the defined G, the pseudo TTF was determined.

$$\begin{aligned} F_{ik}(t) &= P\big(d_{ikl}(t) \ge G\big) \\ &= \Phi\left(\frac{\ln(G) - \beta_2 \ln(V) - \beta_3 \frac{1}{T} - \beta_4 \ln(t) - \mu_\alpha}{\sigma_\alpha}\right) \quad \text{if } 0 < t \le 200 \text{ at } T = 70\ ^\circ C \end{aligned} \tag{5.19}$$

Equation (5.20) shows the set of equations for each stress between 70 °C and 110 °C maintained at specific stress time intervals according to the step-stress ADT design plan illustrated in Figure 5.1.

$$F_{ik}(t) = \begin{cases} \Phi\left(\frac{\ln(G)-\beta_2\ln(V)-\beta_3\frac{1}{T_1}-\beta_4\ln(t)-\mu_\alpha}{\sigma_\alpha}\right) & \text{if } 0 < t \le 200 \text{ at } T = 70\ ^\circ C \\ \Phi\left(\frac{\ln(G)-\beta_2\ln(V)-\beta_3\frac{1}{T_2}-\beta_4\ln(\tau_2+t-200)-\mu_\alpha}{\sigma_\alpha}\right) & \text{if } 200 < t \le 300 \text{ at } T = 80\ ^\circ C \\ \Phi\left(\frac{\ln(G)-\beta_2\ln(V)-\beta_3\frac{1}{T_3}-\beta_4\ln(\tau_3+t-400)-\mu_\alpha}{\sigma_\alpha}\right) & \text{if } 300 < t \le 531 \text{ at } T = 90\ ^\circ C \\ \Phi\left(\frac{\ln(G)-\beta_2\ln(V)-\beta_3\frac{1}{T_4}-\beta_4\ln(\tau_4+t-531)-\mu_\alpha}{\sigma_\alpha}\right) & \text{if } 531 < t \le 750 \text{ at } T = 100\ ^\circ C \\ \Phi\left(\frac{\ln(G)-\beta_2\ln(V)-\beta_3\frac{1}{T_5}-\beta_4\ln(\tau_5+t-750)-\mu_\alpha}{\sigma_\alpha}\right) & \text{if } 750 < t \le 950 \text{ at } T = 110\ ^\circ C \end{cases} \tag{5.20}$$

The mathematical expression for the PDF, denoted by $f_{ik}(t)$, was obtained for one stress level at 70 °C for the initial stress duration of 200 hours as shown in (5.21) by taking the derivative of the CDF expression presented in (5.19).

$$f_{ik}(t) = \begin{cases} D\exp\left(-\frac{1}{2}\left(\frac{\ln(G)-\beta_2\ln(V)-\beta_3/T-\beta_4\ln(t)-\mu_\alpha}{\sigma_\alpha}\right)^2\right) & \text{if } 0 < t \le 200 \text{ at } T = 70\ ^\circ C \\ \text{where } D = \frac{1}{\sigma_\alpha\sqrt{2\pi}} \end{cases} \tag{5.21}$$

Similarly, the overall PDF expression for the applied thermal step-stress levels, $f_{ik}(t)$, can be obtained by applying the natural logarithm of the PDF as shown in (5.22).

$$\ln(f_{ik}(t)) = \begin{cases} Z - \frac{1}{2}\left(\frac{\ln(G)-\beta_2\ln(V)-\beta_3\frac{1}{T_1}-\beta_4\ln(t)-\mu_\alpha}{\sigma_\alpha}\right)^2 & \text{if } 0 < t \le 200 \text{ at } T = 70\ ^\circ C \\ Z - \frac{1}{2}\left(\frac{\ln(G)-\beta_2\ln(V)-\beta_3\frac{1}{T_2}-\beta_4\ln(\tau_2+t-t_1)-\mu_\alpha}{\sigma_\alpha}\right)^2 & \text{if } 200 < t \le 300 \text{ at } T = 80\ ^\circ C \\ Z - \frac{1}{2}\left(\frac{\ln(G)-\beta_2\ln(V)-\beta_3\frac{1}{T_3}-\beta_4\ln(\tau_3+t-t_2)-\mu_\alpha}{\sigma_\alpha}\right)^2 & \text{if } 300 < t \le 531 \text{ at } T = 90\ ^\circ \\ Z - \frac{1}{2}\left(\frac{\ln(G)-\beta_2\ln(V)-\beta_3\frac{1}{T_4}-\beta_4\ln(\tau_4+t-t_3)-\mu_\alpha}{\sigma_\alpha}\right)^2 & \text{if } 531 < t \le 750 \text{ at } T = 100\ ^\circ C \\ Z - \frac{1}{2}\left(\frac{\ln(G)-\beta_2\ln(V)-\beta_3\frac{1}{T_5}-\beta_4\ln(\tau_5+t-t_4)-\mu_\alpha}{\sigma_\alpha}\right)^2 & \text{if } 750 < t \le 950 \text{ at } T = 110\ ^\circ C \\ \text{where } Z = -\ln(\sigma_\alpha/\sqrt{2\pi}) \end{cases} \tag{5.22}$$

The likelihood function L_f, (5.23) or in natural logarithm form in (5.24), for the tested samples at different stress level can be then expressed as the multiplication of the PDF

function at specific time intervals, where t_i represents the different EMC performance degradation measurement time at which the EMC degradation data were computed for the tested IC samples (Figure 5.10), k refers to the two different voltage stress level, n_k is the number of samples tested at each stress level. The derivative of the analytical expression in (5.24) with respect to the unknown parameters of the degradation model is essential prior to applying the MLE method. Considering the complexity of the proposed model with multiple unknown parameters, the genetic algorithm was considered for the optimization purposes to predict the unknown parameters. Table 5.3 provides the estimated values of the degradation model parameters for both UA78L05 and L78L05 tested DUTs. Consequently, the generalized EMC performance degradation model, developed by the ADT modeling approach, would allow to predict the conducted immunity degradation behavior of the the tested IC samples at any known or unknown multiple stress conditions.

$$L_f(t|\mu_\alpha, \sigma_\alpha, \beta_2, \beta_3, \beta_4) = \prod_{k=1}^{2} \prod_{i=1}^{n_k} f_{ik}(t_i) \tag{5.23}$$

$$\ln\left(L_f(t|\mu_\alpha, \sigma_\alpha, \beta_2, \beta_3, \beta_4)\right) = \sum_{k=1}^{2} \sum_{i=1}^{n_k} \ln(f_{ik}(t_i)) \tag{5.24}$$

TABLE 5.3 – Degradation Model Parameters for both L78L05 and UA78L05

Degradation model parameters	**IC reference**	
	UA78L05	**L78L05**
σ_α	-1.55	-3.43
μ_α	0.54	0.61
β_2	-1.01	-0.22
β_3	116.05	116.04
β_4	0.23	0.20
$L_f(t\|\sigma_\alpha, \mu_\alpha, \beta_2, \beta_3, \beta_4)$	0.04	0.03

5.8 Degradation and lifetime Reliability Modeling of Digital ICs Influenced by the CSADT Ageing Constraints

This section aims to develop degradation and reliability models, depending on the conducted measurements and analysis of the conducted immunity performance degradation of the digital circuits embedded within the Attiny85 micro-controller IC developed by Atmel, under the influence of multiple constant ageing stress factors (i.e., thermal and electrical overstress) conditions.

5.8.1 Constant stress ADT plan

The constant stress ADT plan was designed to activate the relevant failure modes and mechanisms by accelerating the aging of the digital circuit embedded within the Attiny85 micro-controller ICs based on the selection of multiple stress factors (i.e., temperature and electrical voltage), stress magnitude, and total duration. The number of IC samples selected for ADTs under the influence of both temperature and electrical overstress is detailed in Table 5.4. A total of 24 DUTs IC samples (i.e., AT1−AT24) were considered to obtain an accurate and desirable enough estimation of the observed conducted immunity performance degradation caused by simultaneously applying two different constant temperature (i.e., 110 °C and 70 °C) and electrical overstress levels (i.e., 4 V and 5 V). Among the tested IC samples, the 12 DUTs samples (i.e., AT1−AT12) were subjected to the highest constant temperature stress with two distinct constant electrical voltage stress magnitudes. For the remaining acIC samples (i.e., AT13-AT24), a similar constant stress ADT was developed, taking into account similar electrical voltage overstress conditions but employing a lower constant temperature stress level (70°C).

5.8.2 Attiny85 IC under test

The Attiny85 IC chip is a low power and high performance 8-bit micro-controller, designed and developed by the Atmel Corporation, can be reprogrammed In-System through a Serial Programming Interface (SPI) either by a conventional non-volatile memory programmer or using an On-chip boot code running on the integrated Central Processing Unit (CPU) core. According to the datasheet of the selected IC chip, the selected At-

TABLE 5.4 – Accelerated ageing conditions to perform the constant stress ADTs on the ICs

IC model reference	Samples	Thermal stress	Electrical voltage stress	Total stress duration
Attiny85	AT1-AT6	110 °C	4 V	1000 hours
	AT7-AT12	110 °C	5 V	
	AT13-AT18	70 °C	4 V	
	AT19-AT24	70 °C	5 V	

tiny85 sample has been manufactured with various functional specifications (i.e., 32 general purpose instruction registers, 8 kB in-system programmable flash memory, 256-bytes Static Random Access Memory (SRAM), 8-bit counter, Arithmetic Logic Unit (ALU), analog comparator and Analog-to-Digital Converter (ADC) circuit and 6 general-purpose input/output (I/O) lines [89]. The internal block diagram of the Attiny85 IC chip is equipped with analog and digital circuit blocks (i.e., flip-flops, timer, counter) as shown in Figure 5.13. Using the analog and/or digital I/O pins, these circuit blocks can be programmed to perform various functions in various applications, including wearable electronic components, battery-powered devices and internet of things (IoT), controlling the speed and direction of different types of motors, reading and transmitting sensor data, and communicating with other devices using the SPI protocol.

According to the specifications [89], Figure 5.14 shows the pin configuration of the selected IC associated to different physical pin numbers. Those pins are assigned to execute various functional tasks based on the program stored into the IC's internal memory. In order to turn on the chip, the physical pins 4 and 8 should be connected to the DC power supply and the PCB ground, respectively. The remaining I/O pins can be used as analog and/or digital pins to operate the integrated analog and/or digital circuits integrated within the IC chip.

This micro-controller IC chip was programmed using the Arduino IDE software tool compatible to the Arduino UNO embedded system device for performing the required functionality of the digital circuit embedded within the IC chip. The developed program was uploaded and/or burned into the flash programmable memory of the IC by choosing the Arduino UNO development board as the in-system programming (ISP) programmer. The latter could be performed by following some necessary steps mentioned as follows :

1. Upload the Arduino ISP code to the 'Arduino UNO' development board.

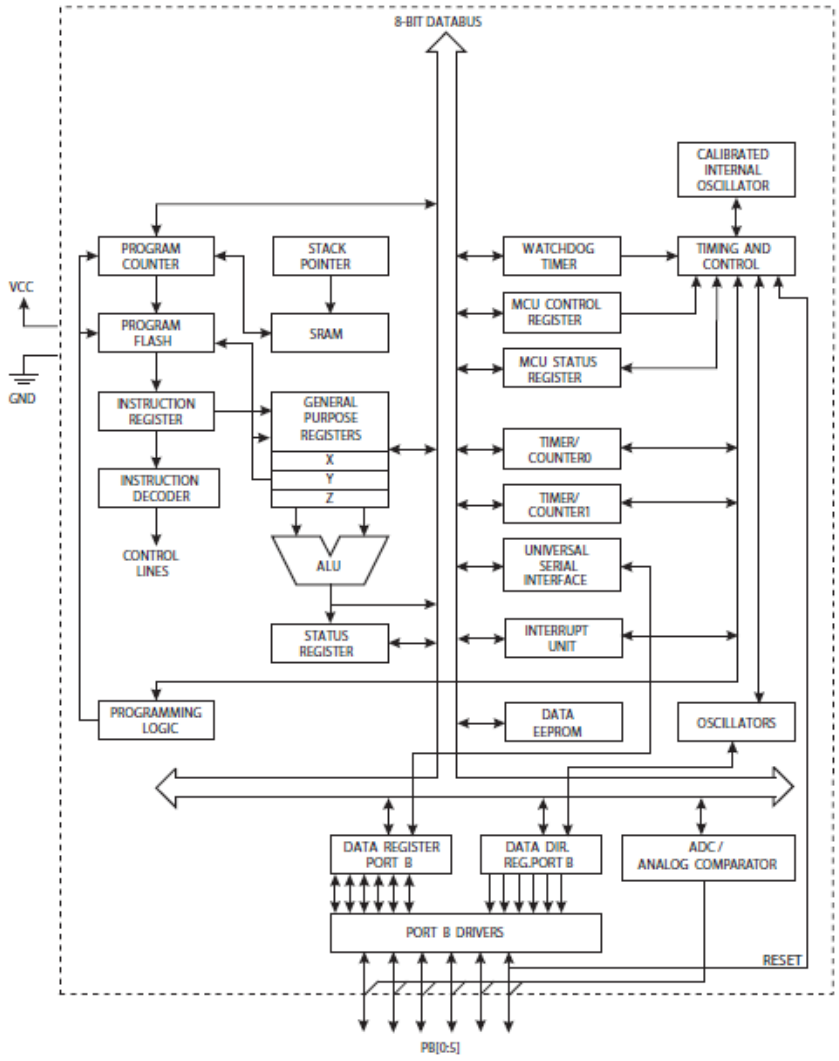


FIGURE 5.13 – Internal block diagram of the Attiny85 micro-controller IC chip [89].

2. Interfacing between the Attiny85 micro-controller chip and the Arduino UNO board by connecting the IC pins to the required appropriate pins of the Arduino UNO. Figure 5.15 shows the connection between the SPI pins of the IC and the Arduino UNO physical hardware pins (i.e., MOSI, MISO, Reset, SCK), prior to uploading the program code into the IC chip using the Arduino UNO as a programmer.

3. Install the required driver and package for the Attiny85 compatible micro-controller processor and choose required parameters, internal clock frequency of 8 MHz.

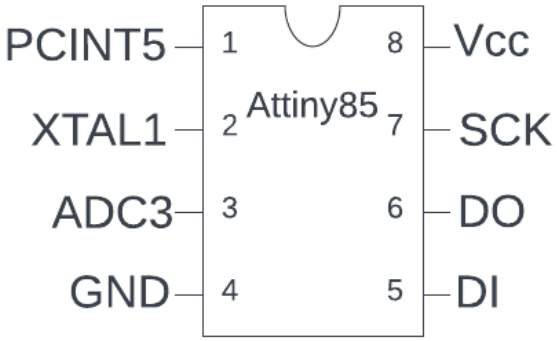
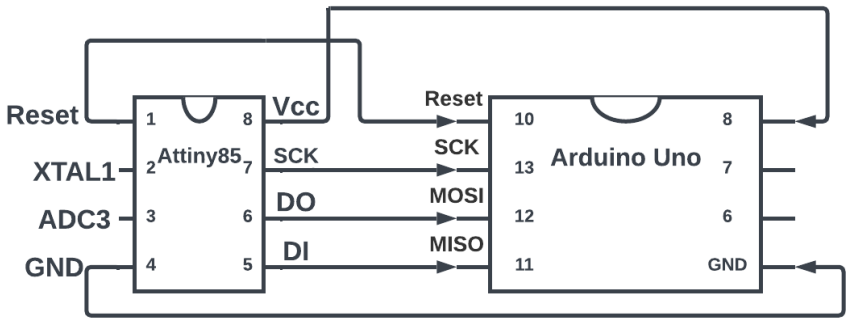


FIGURE 5.14 – Pin configuration of the Attiny85 micro-controller IC chip [89].

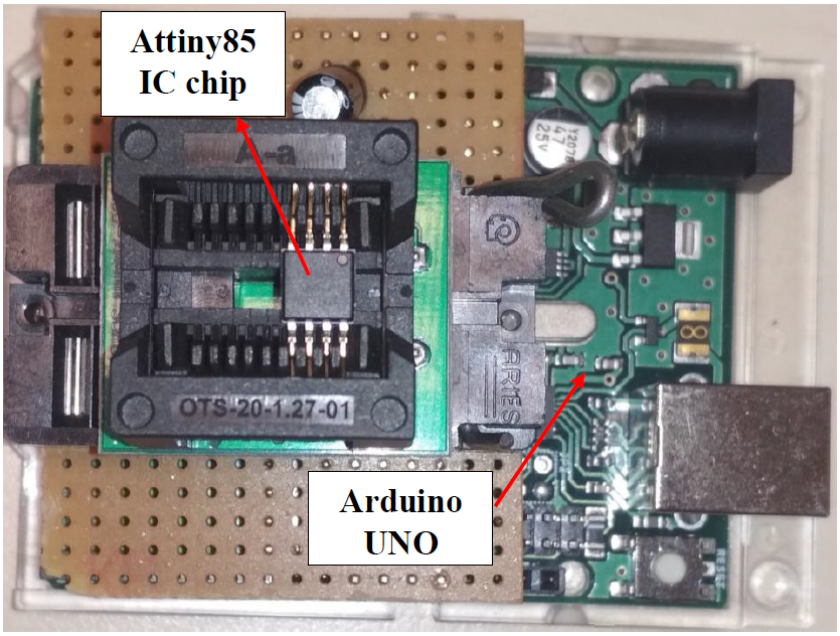
4. Prior to uploading the developed program into the IC, choose the Arduino UNO as the "Arduino as ISP" programmer using the Arduino IDE software, followed by selecting the "Burn Bootloader" option available in the software platform.
5. Finally, use the software platform's "Upload Using Programmer" command to upload the produced code to the IC re-programmable memory.

The micro-controller IC was programmed by implementing the algorithm necessary to acquire the desired functionality of the integrated digital circuit on the chip. The following are the step-by-step techniques for implementing this algorithm to construct the program for executing the digital circuit of the micro-controller in nominal settings (i.e., 25 °C and 3 V).

1. Initialize various input and output ports of the Attiny85 micro-controller. The digital input (DI) and serial clock (SCK) pins are configured as inputs to receive the square wave signal from an external functional signal generator, while the digital output (DO) pin is set as an output to observe the digital output signal. Set the initial state of both the DI and DO pin at the digital logic low (0) level.
2. Within the code's 'void loop()' method, the program allows you to wait until the digital clock signal attached to the SCK pin changes from logic low to high level (rising edge), ensuring synchronization with the clock signal.
3. Read the initial logic state of the digital input signal on the DI pin and store the



(a)



(b)

FIGURE 5.15 – Interfacing the Attiny85 IC pins with the Arduino UNO (a) schematic ; (b) component.

value (logic high or low) in the data variable, which then sends the data to the DO pin so that the state of the DO pin corresponds to that of the DI pin state (i.e., if the DI bit is 1, the DO pin also sets to high).

4. Using the 'while()' loop function in the code, check and wait for detecting for the rising edge of the external clock signal on the SCK pin.
5. Record the previous state value of the DO pin at the rising edge of the clock pulse.
6. Wait for detecting the next falling edge followed by the rising edge of the clock signal applied to the SCK pin.

7. At the rising edge of the clock signal, check if the previous state of the DO pin is at logic low or high voltage level. If the previous state of the DO pin was at the digital logic high (1) bit, set it to the low and vice versa, while considering the current state of the DI signal that latched into the DO pin.
8. Check the previous state of the DO signal at the falling edge of the clock pulse. The output signal would would remain unchanged irrespective of the DI signal state, until the next rising edge at the SCK pin is detected

Overall, this developed algorithm was designed and implemented in the program to enable the Attiny85 to demonstrate a specific output functionality of the digital logic circuit, such that such that the DO signal changes from logic low to high and vice versa on the rising edge of the clock signal on the SCK pin, depending on the state of the DI pin. In addition, the output signal at the DO pin would remain unchanged until the next ascending edge of the clock pulse to the SCK pin is detected. Note that the developed algorithm was implemented to guarantee proper timing and synchronization between the DI and clock signals in order to obtain an accurate micro-controller output signal at the DO pin.

5.8.3 Experimental methods and measurement procedures

The accelerated aging time-dependent experimental test setup used to implement the designed constant stress ADTs plan on the selected IC samples (i.e., AT1-AT24) is similar to that of in Figure 5.2 displayed in the sub-section 5.3.3. However, the selected DUTs samples (i.e., AT1-AT12) were subjected to the highest thermal aging stress magnitude (i.e., 110 °C) inside the climatic chamber for a total stress duration of 1000 hours. Those fresh sample ICs, were subjected to the two different DC electrical voltage overstress levels (i.e., 4 V and 5 V) applied into the V_{cc} (pin 8) using the high temperature thermal resistant aging cables [51]. Similarly, the remaining 12 fresh DUTs samples (i.e., AT13-AT24) were aged simultaneously according to the designed constant stress ADT plan discussed in the sub-section 5.8.1. Those constant multiple stress aging conditions were applied simultaneously on all the fresh DUTs for ensuring permanent intrinsic degradation caused by activating and accelerating the relevant failure mechanisms induced by the high temperature and electrical voltage stress factors. induced the failure mechanisms (i.e., HCI and NBTI).

The evolution of the long-term EMR of the ICs, depending on the applied aging

stress magnitude and time duration, was investigated by implementing the repetitive method of applying the "Stress-Measurement-Stress" technique till the completion of the intended ADT plan mentioned in the Table 5.4, which is similar to that of illustrated in the Figure 5.3. However, this experimental methodology involved pausing the accelerated ageing process after every 200 hours of stress duration, followed by removing all the tested IC samples from the climatic chamber, and performing the DPI conducted immunity tests in nominal condition (i.e., 25 °C and 3 V) on all the fresh and aged ICs to assess and analyze the accelerated aging impact on the measured EMC performance variation at different stress time. The aged DUTs were then reintroduced to the climatic chamber prior to resuming the accelerated aging process outlined in the ADT plan. Hence, the above aforementioned cycle was repeated after every fixed aging stress duration of 200 hours for the total stress duration of 1000 hours.

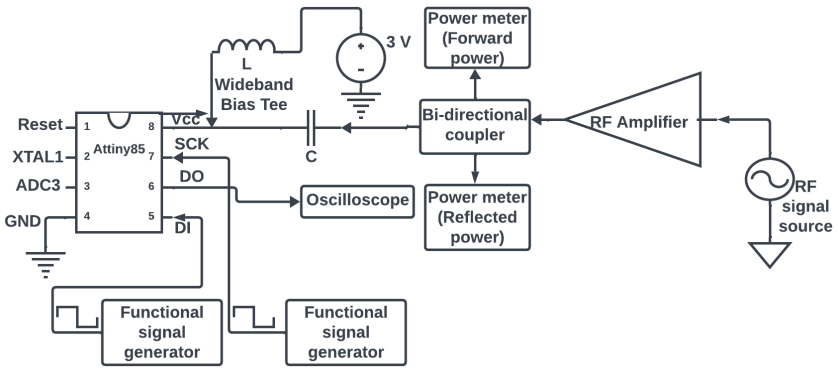


FIGURE 5.16 – Measurement test setup for evaluating the conducted immunity of the DUTs

The conducted EMC performance of the tested ICs was evaluated by performing the non-destructive DPI test in accordance to the IEC 62132-4 standard [16]. The DPI test measurement setup is similar to that discussed in sub-section 3.2.2. However, the conducted immunity variation of these aged Attiny85 IC chip micro-controller, mounted on the custom-designed with SOIC8 package PCB, required applying the square-wave pulse for the clock signal into the SCK (pin 7) as well as injecting another square-wave digital signal into the DI (pin 5) using an external multi-channel functional signal generator. The experimental test setup was utilized to characterize the conducted immunity parameters (i.e., P_{inj} and f). Figure 5.16 displays the overall experimental test bench for performing the DPI test on both the fresh and aged micro-controller IC samples.

Figure 5.16 shows that the digital square-wave signal was generated using the functional signal generator and injected to the DI (pin 5) of the tested IC at the DI signal frequency (f_{DI}) of 50 KHz and a duty cycle of 50%. In addition, another external square-wave clock signal, with the clock frequency (f_{sck}) of 100 KHz and a 50% duty cycle, allowing it to remain at the logic high voltage level for half the total time period, was produced by another functional signal source and introduced to the SCK (pin 7). This square-wave clock signal was generated with a positive rising edge, changing from the logic low voltage (V_L) level (i.e., 0.3 V) to the logic high voltage (V_H) level (i.e., 2.8 V). It is worth mentioning that the same magnitude of both the V_L and V_H were selected for the DI signal. Since the micro-controller IC was turned on by applying 3 V into the V_{cc} (pin 8) in the nominal condition, hence, both the V_H and the V_L magnitude were arbitrary selected to be slightly lower to the V_{cc} voltage and higher to the reference GND (i.e., 0 V). Note that, the magnitude of these generated digital signal were selected by taking into account of the IC's datasheet for considering relevant specifications, including the operating temperature, manufacturing tolerance and the tested IC chip physical and electrical characteristics (i.e., maximum operating current, supply voltage). It is also worth mentioning that the f_{sck} was chosen to be double of the f_{DI} so that the DI signal could be synchronized to the SCK pulse at the rising edge, enabling to avoid any synchronization or signal propagation delay that might affect the DO signal from aligning with the clock signal.

Depending on the program uploaded to the tested DUTs, it reads the DI signal on every cycle of the clock signal at the SCK pin. At the rising edge of the clock signal, the DI signal data was send out to the DO pin. According to the algorithm of the program, the output signal at the DO pin would only change its previous state (i.e., logic low to high and vice versa) depending on the present state of the DI pin. Consequently, at the falling edge of the clock signal, the output signal would remain the same as the previous state until the next clock rising edge at the SCK pin is detected. Thus, the DO signal produced with the rising edge corresponds to the clock signal's rising edge and the falling edge depending on the previous logic state of the DO (pin 6). As a result, at the nominal condition, the digital circuit embedded within the IC was allowed to perform with this specific functionality, producing a DO square voltage waveform that could be monitored in the digital oscilloscope. The DO square-wave signal produced at the DO pin with a frequency (f_{DO}), which is identical to that of f_{DI}.

The experimental test bench presented in Figure 5.16 was utilized to perform the

DPI test by implementing the developed DPI algorithm similar to that in Figure 5.4b. However, the DPI failure criterion defined for the tested Attiny85 micro-controller IC chip would differ compared to that discussed in subsection 5.3.4. Considering the IEC 62132-4 standard for defining the DPI immunity criterion, the digital circuit was considered to fail, while characterizing the EMC performance, if the following defined perturbations criteria would be obtained as mentioned below,

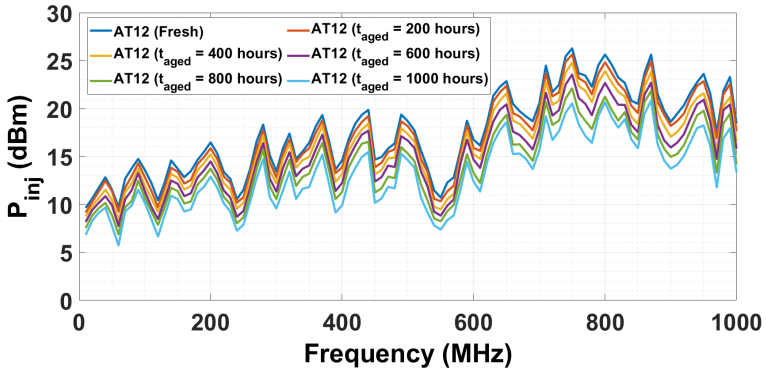
1. either the nominal V_L or V_H level of the DO signal exceeds the 10% boundary limit, resulting in the positive or negative failure mode due to the injection of the RF disturbance into the V_{cc} pin.
2. either the timing variation observed in the rising or falling edges of the expected DO signal due to the noise induced by the EMI should not exceed the 10% limit. This phenomenon could be observed in the DO signal due to the noise induced to the V_{cc} pin of the IC, which affects its signal integrity causing significant implication in its functional performance.

The DPI measurement data (i.e., P_{inj}) on the V_{cc} pin to induce the DPI failure on the tested ICs were recorded at each corresponding RF frequency, ranging from 10 MHz to 1000 MHz with a step-size of 10 MHz. The later section compares and analyzes the conducted immunity variation of some of the IC samples (i.e.,, AT6, AT12, AT18 and AT24), under the influence of different constant thermal and electrical voltage overstress conditions taking into account of the ADT plan, as a function of aging stress time (t_{aged}) and DPI frequencies.

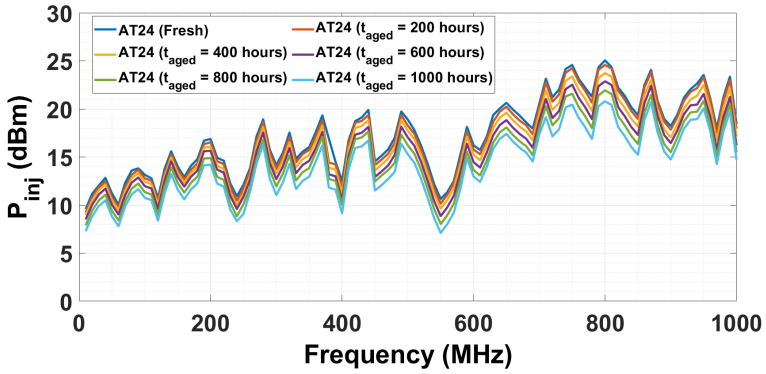
5.8.4 Conducted immunity performance of the aged DUTs : results and analysis

Figure 5.17 illustrates the EMC performance evolution of the tested fresh and aged AT12 and AT24 IC sample observed at different stress t_{aged} duration, subjected to the same electrical overstress voltage (i.e., 5 V) but different thermal stress conditions (i.e., 110 °C and 70 °C). While considering an increase of the t_{aged} intervals, the EMC performance of the tested IC samples, characterized by both the high and low immunity points, degraded at each corresponding frequencies, ranging between 10 and 1000 MHz (Figures 5.17a and 5.17b). Although the P_{inj} was found to be comparable for the AT24 and AT12 ICs, Figure 5.17a shows that the mean P_{inj} of the fresh AT12 decreased from 18.43 dBm to 13.35 dBm between 10 MHz and 1000 MHz. Consequently, the Figure 5.17b displays a

smaller reduction of an average P_{inj} from 18.44 dBm to 14.71 dBm across the same tested DPI frequency range, after the completion of the total ageing t_{aged}. Thus, the AT24 was found to be more immune compared to the AT12 due to applying 30 °C higher temperature stress magnitude for 1000 hours.



(a)

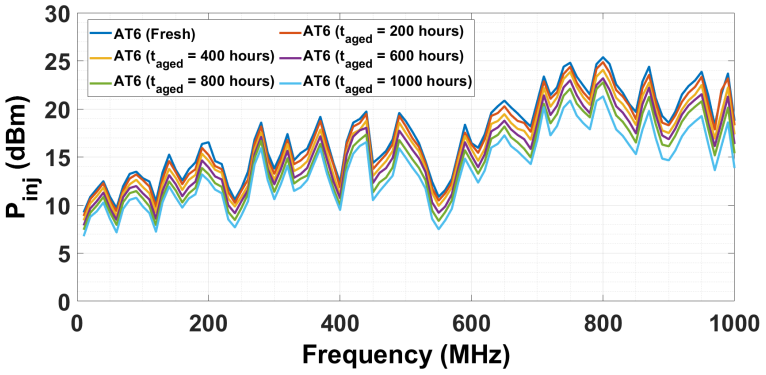


(b)

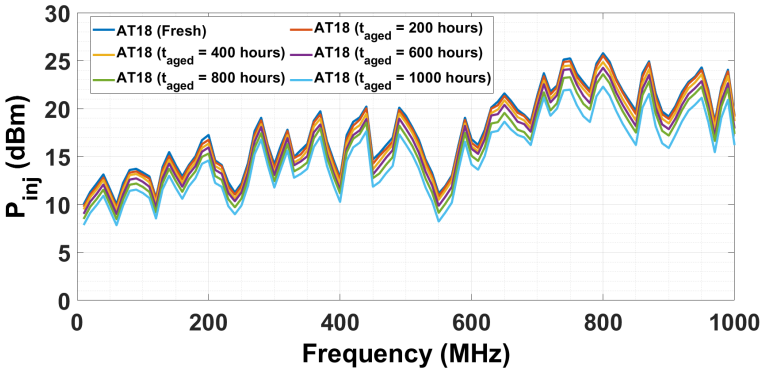
FIGURE 5.17 – Evolution of the conducted immunity level of Attiny85 samples at various aging stress duration caused by the identical 5 V electrical voltage overstress and constant (a) high ; (b) low thermal stress conditions.

The similar evolution of the EMC characteristics was also observed for both the tested AT6 and AT18 IC samples in Figure 5.18. However, Figure 5.18 demonstrates little impact on the conducted immunity degradation of the DUTs compared to those tested sample's EMC performance observed in Figure 5.17. This is because both the AT6 and AT18 were subjected to a 7.3% lower electrical voltage overstress magnitude compared to those AT12 and AT24 IC DUT samples, respectively. It is worth to mention that the similar EMC performance was also obtained for the remaining 20 IC samples tested in accordance to

the designed multiple constant stress ADT plan.



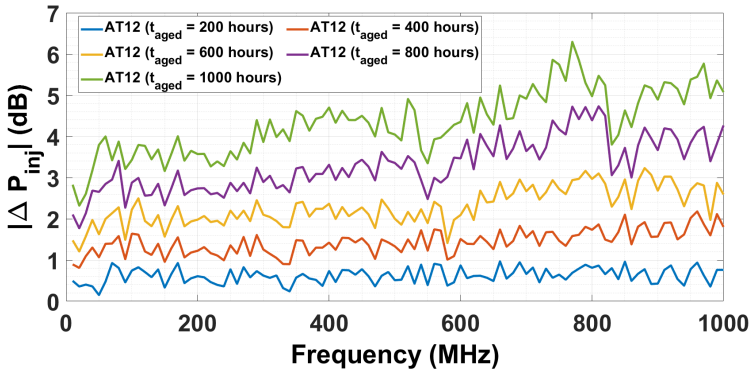
(a)



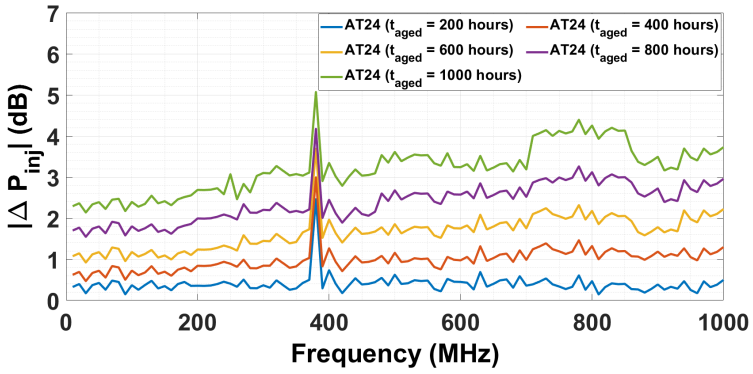
(b)

FIGURE 5.18 – Evolution of the conducted immunity level of Attiny85 samples at various aging stress duration caused by the identical 4 V electrical voltage overstress and constant (a) high ; (b) low thermal stress conditions.

The effect of applying constant multiple stress factors (i.e., temperature and electrical voltage) on the EMC fluctuation of the recorded P_{inj} level between the fresh sample and the aged state at different aging t_{aged} duration was analyzed by computing the absolute ΔP_{inj} at each DPI frequency values between 10 and 1000 MHz. Figures 5.19 and 5.20 compares the variation of the extracted $|\Delta P_{inj}|$ data computed as a function of tested frequency at different aging t_{aged} intervals. The significant reduction in the EMC performance of all the tested ICs was observed at different t_{aged} intervals, due to obtaining negative statistical computation of the ΔP_{inj} data extracted for each corresponding DPI frequency values. The $|\Delta P_{inj}|$ data was considered as a suitable parameter to observe the evolution of the conducted immunity performance degradation at different stress duration.



(a)



(b)

FIGURE 5.19 – Conducted immunity level drift of Attiny85 samples at various aging stress time caused by the identical 5 V electrical voltage overstress as well as constant (a) high ; and (b) low thermal stress conditions.

The observed increasing degradation of the conducted immunity level drift, characterized by the ΔP_{inj}, could be due to the increasing failure rate of the accelerated intrinsic failure mechanisms (i.e., HCI and NBTI) induced by applying multiple accelerated aging stress conditions. These failure mechanisms could change the intrinsic parameters of the internal transistors of the digital circuit within the tested Attiny85 samples, increasing the V_{th} and reducing the charge carrier (i.e., electrons and holes) mobility of the internal NMOS and PMOS transistors. Moreover, these induced failure mechanisms may apply large V_{ds} between the drain and source terminals of the aged internal CMOS transistors, resulting in a substantial reduction of I_{ds} propagating across these terminals.

This phenomenon could be validated using the mathematical relationship between I_{ds} and V_{th} expressed in (5.25), where I_{ds} refers to the biasing current flowing between the

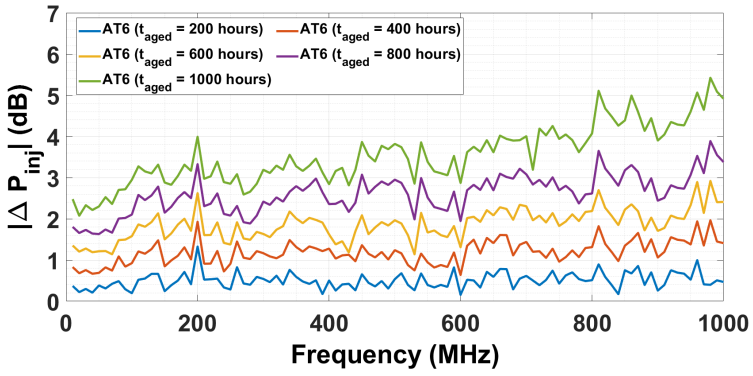
drain and source terminal of internal aged transistors within the tested IC chip, μ_n is the electron mobility of NMOS transistor, C_{ox} is denoted by the gate-oxide capacitance and (w/L) is the geometric ratio of internal aged transistors [90]. Therefore, lower transconductance g_m parameter of the aged transistor could be demonstrated mathematically in (5.26) [26]. Finally, the switching speed of the aging internal transistors of the digital circuit embedded within the DUT could decrease, thereby increasing the signal propagation delay through the internal logic gates of the tested ICs [91]. Therefore, adequate timing and clock synchronization between the DI and clock signal at the SCK pin could no longer be guaranteed, resulting in DO signal distortion in the aged DUT and a reduction in its conducted immunity performance.

$$I_{ds} = \left(\frac{\mu_n C_{ox}}{2}\right) \cdot \left(\frac{w}{L}\right) \cdot (V_{gs} - V_{th})^2 \tag{5.25}$$

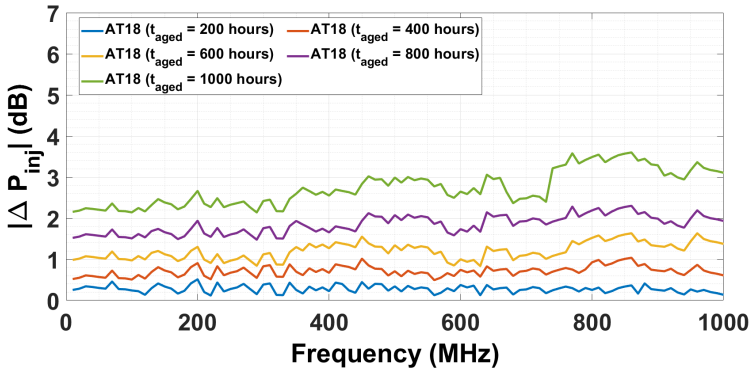
$$g_m = \sqrt{I_{ds} \cdot \mu_n \cdot C_{ox} \cdot \left(\frac{w}{L}\right)} \tag{5.26}$$

5.8.5 EMC degradation modeling and parameter estimation of the aged DUTs

Figure 5.21 illustrates an increasing conducted immunity performance curves for each of the selected tested IC samples (i.e., AT6, A12, AT18 and AT24), characterized by the mean $|\Delta P_{inj}|$ data plotted on the y-axis against the aging stress duration of time on the x-axis. Since the measured P_{inj} data of the tested DUTs was dependent on both the DPI frequency and aging stress duration, consequently the extracted ΔP_{inj} data also varied depending on both the frequencies and aging stress t_{aged} duration. Hence, mean $|\Delta P_{inj}|$ was considered for representing the aging stress time-dependent evolution of the EMC performance degradation on the tested ICs. At each stress intervals of t_{aged}, mean $|\Delta P_{inj}|$ was computed by taking the sum of all the ΔP_{inj} extracted for each corresponding tested DPI frequency followed by dividing the evaluated total ΔP_{inj} by the total number of the considered frequency values. This statistical computation of the absolute mean ΔP_{inj} for the tested digital IC samples could be represented by a mathematical expression similar to that of mentioned in equation 4.1. Figure 5.21 demonstrates significant increment



(a)



(b)

FIGURE 5.20 – Conducted immunity level drift of Attiny85 samples at various aging stress time caused by the identical 4 V electrical voltage overstress as well as constant (a) high ; and (b) low thermal stress conditions.

of the the mean $|\Delta P_{inj}|$ with increasing stress duration for all the tested IC samples, depending on the applied accelerated multiple stress conditions defined by the designed constant stress ADT plan. The conducted immunity performance degradation of these tested IC samples could be compared by noticing significant difference in the mean $|\Delta P_{inj}|$ at various stress times. At the end of the conducted ADTs, the aged AT12 DUT showed the highest conducted immunity degradation, demonstrating a mean $|\Delta P_{inj}|$ of 4.33 dB over the whole frequency range, compared the rest of the tested IC samples. Under the influence of the identical thermal stress but different electrical overstress conditions, the aged AT6 sample showed a total of 22.3% lower immunity degradation compared to the aged AT12 DUT. In addition, the AT24 sample IC aged at the low thermal (i.e., 70 °C) and high electrical voltage (i.e., 5 V) overstress condition for 1000 hours exhibited a 17.2%

greater conducted immunity performance degradation compared to that of the aged AT18 sample DUT with the similar accelerated thermal stress and a lower electrical overstress conditions (Figure 5.21).

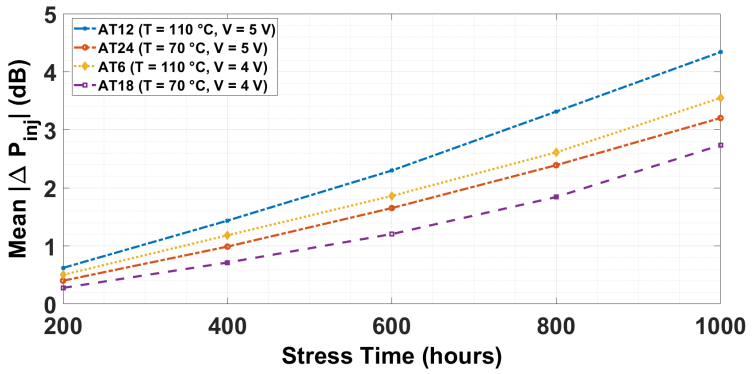


FIGURE 5.21 – Conducted immunity degradation as a function of stress time under the influence of accelerated aging conditions on the tested IC samples.

Figure 5.22 depicts the monotonic evolution of the monotonic degradation of the tested IC samples at different stress time over the whole tested DPI frequency range (i.e., 10-1000 MHz). For a fixed aging stress time measured in hours, both the computed $|\Delta P_{inj}|$ and the measured nominal P_{inj} data of the fresh DUTs before aging varied in each frequency points over the entire tested frequency range, ratio of the $|\Delta P_{inj}|$ to that of the P_{inj} data of the fresh sample was evaluated which is denoted by G. At various stress times, mean G was computed by taking the average of the evaluated G for every corresponding frequency, and was considered as the suitable stress time dependent EMC degradation path modeling indicator parameter for the tested ICs, as illustrated in Figure 5.22. In addition, Figure 5.22 shows that the similar increasing monotonic degradation trend over the total stress duration is observed for all the DUT samples tested at different combinations of applied thermal (T) and electrical voltage (V) overstress conditions. Those non-linear best-fit degradation paths were generated by extrapolation technique, which follows a suitable agreement with the computed mean G data points (Figure 5.22).

The simplified mathematical expression to model those generated monotonic degradation paths at various stress duration and magnitudes is provided in equation (5.27), where $y_{ikl}(t)$ represents the mean G (denoted by %), A and γ are the stress-dependent degradation unknown model constants, i is the sample unit, k refers to the V stress level and l is the T constant stress level. Applying the regression analysis on the developed model

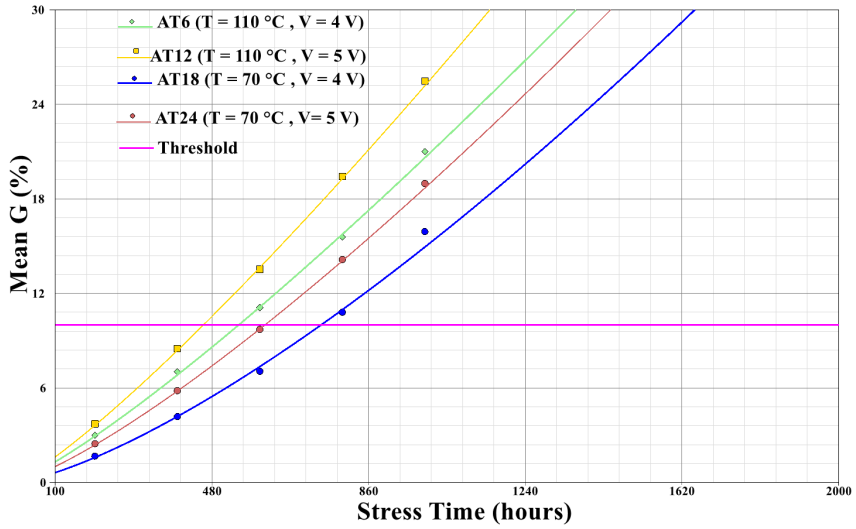


FIGURE 5.22 – Degradation paths fitted to the computed EMC degradation of the tested IC samples.

expressed in (5.27) allowed to estimate those relevant unknown model constants (i.e., A and γ). Determining the model constants would enable to predict the EMC degradation data based on the known values of stress duration for any tested or untested accelerated stress conditions. Moreover, the proposed model could also allow to predict the future conducted immunity degradation in nominal condition after a certain operational time period of ICs.

$$y_{ikl}(t) = A_{ikl} t^{\gamma} \tag{5.27}$$

$$\log(y_{ikl}(t)) = \log\left(\frac{\overline{\Delta P_{inj}}}{P_{inj}}\right) = \log(A_{ikl}) + \gamma \log(t) \tag{5.28}$$

$$t_{\text{failure}} = \exp\left(\frac{\log(y_{ikl}(t)) - \log(A_{ikl})}{\gamma}\right) \tag{5.29}$$

Non-destructive EMC degradation path modeling analysis was performed to determine the pseudo TTF data that could be determined both graphically and mathematically,

depending on the defined failure threshold. A failure threshold of 10% on the observed EMC degradation datawas considered which is shown by the horizontal line in Figure 5.23. Applying the logarithm on both sides of the equation (5.27) provide for the $y_{ikl(t)}$ that is referred as logarithmic mean ratio of the variation of $|\Delta P_{inj}|$ from that of the nominal P_{inj} before aging of the tested IC as shown in equation (5.28).

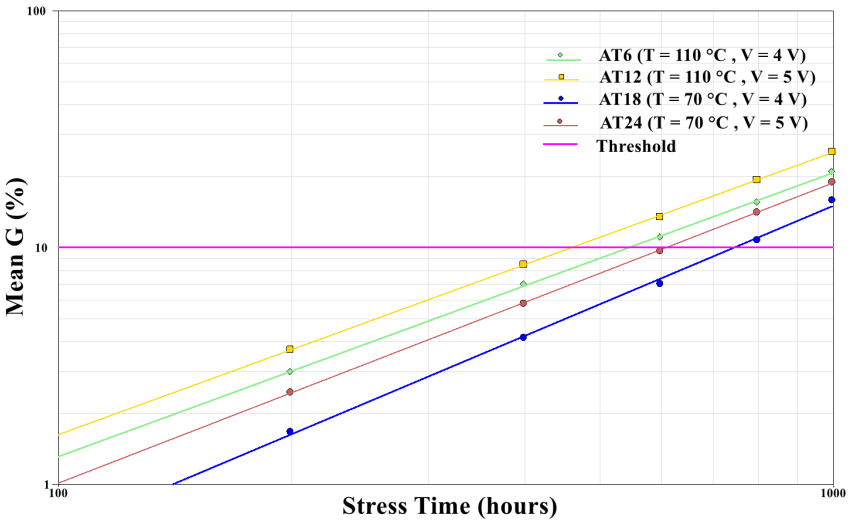


FIGURE 5.23 – Log-linear degradation paths generated at different constant multiple stress conditions to estimation of the failure time data.

TABLE 5.5 – EMC degradation path modeling parameters and TTF data of various tested IC samples

IC references	Parameters		
	A	ϒ	TTF/ (hours)
AT6	0.0052	1.1988	549
AT12	0.0072	1.1593	514
AT18	0.0011	1.3801	739
AT24	0.0029	1.2683	616

The mathematical expression for determining the estimated failure time $t_{failure}$ based on the considered degradation over the stress time is expressed in equation (5.29), using the predicted values of the model constants A and γ. Table 5.5 shows the model parameters and the computed TTF data of IC samples tested at multiple constant multiple stress factors with different stress magnitude. It is worth to mention that this developed

degradation path model was employed for the rest of the samples for determining their corresponding $t_{failure}$ and other relevant model parameters.

5.8.6 ALT modeling and reliability analysis of the tested ICs

Since both temperature T and voltage V stress factors were applied simultaneously on the DUT samples that resulted to obtain the EMC performance degradation data, the generalized Eyring ALT model to express the relationship between the quantifiable lifetime (L) and both T and V stresses in (5.30), where the $L(T,V)$ refers to the life-data relationship with the applied T and V stress factors on the tested IC samples, unknown model constants (i.e., A, B and C) depends on sample design and properties that was estimated by combining this model with the two-parameter Weibull distribution and applying the MLE method to estimate those model parameters. Unlike the simplified Eyring ALT model that takes into account of the impact of T stress only on the lifetime L of a tested sample, the developed mathematical life-stress model is an extension of the simplified Eyring ALT model. This model takes into account of any strong interaction between the thermal T and non-thermal (i.e., electrical voltage) stress factors using the last exponential term using the model constant C as shown in (5.30), allowing to predict the effect of varying one of the individual stress factors on the lifetime L stress data is dependent on the stress level of the other stress factor. In the other words, it can also be implied that the impact caused by the acceleration factor due to the T would depend on the stress magnitude of the V stress and vice versa [30]. The two parameters Weibull PDF expression is provided in (5.9), where the scale η is equivalent to the $L(T,V)$ and expressed in (5.31). The generalized Eyring-Weibull PDF expression can be obtained by substituting the (5.31) in (5.9). Thus, the mathematical expression for the combined generalized-Weibull PDF is provided in equation (5.32). The derived mathematical expression for the developed reliability model is expressed in (5.33). Applying the MLE method after substituting the (5.32) in the generalized form that represents the L_f log-likelihood function provided in (5.24). Applying the minimum function optimization technique using the $t_{failure}$ data allows obtain the unknown ALT reliability model and Weibull distribution parameters β_w and η are provided in Table 5.6.

$$L(T,V) = \frac{A}{T}\exp\left(\frac{E_a}{kT}\right)\exp(BV)\exp\left(\frac{CV}{kT}\right) \tag{5.30}$$

$$\frac{1}{\eta} = \frac{1}{L(T,V)} = \frac{T}{A}\exp\left(-\frac{E_a}{kT}\right)\exp(-BV)\exp\left(-\frac{CV}{kT}\right) \tag{5.31}$$

$$f_w(t,T,V) = \frac{\beta_w}{L(T,V)}\left(\frac{1}{L(T,V)}\cdot t^{\beta_w-1}\right)\cdot\exp\left(-\frac{t}{L(T,V)}\right)^{\beta_w} \tag{5.32}$$

$$R(t,T,V) = \exp\left[-t\left(\frac{A}{T}\exp\left(-\frac{E_a}{kT}\right)\exp\left(-BV\right)\exp\left(-\frac{CV}{kT}\right)\right)^{\beta}\right] \tag{5.33}$$

TABLE 5.6 – ALT reliability modeling parameters for the tested IC samples

Model parameters	Data
A	9.24
B	1327.86
C	0.30
E_a	-0.11
L_f	-106.09
β_w	32.68
η	1507.44

The developed generalized Eyring-Weibull life-stress relationship was employed to characterize lifetime reliability model parameters of the IC samples tested under the influence of applying multiple stress factors with different constant stress magnitudes for a fixed stress duration. Figure 5.24 illustrates a set of parallel lines, produced by applying the Weibull distribution on the developed reliability model, which fits to the computed pseudo TTF data for each DUT samples. Those sets of parallel lines is a representation of the predicted unreliability, which corresponds to the combined influence of both thermal and electrical voltage stress factors with different stress magnitudes. In addition, those pseudo TTF data points evaluated based on the defined failure threshold considered on the observed EMC degradation data. The developed model could predict the unreliability (or failure probability) for all the tested samples with a very acceptable accuracy as little difference between the Weibull distribution plots of the unreliability function and those

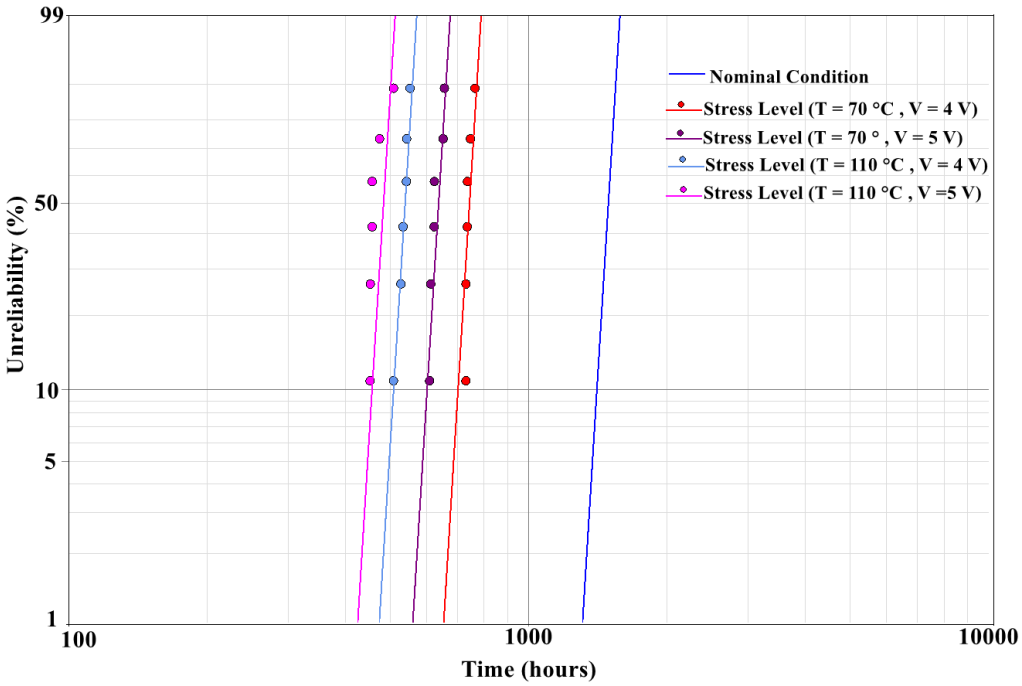


FIGURE 5.24 – Lifetime unreliability distribution of the logarithmic fits to the pseudo TTF data for each tested IC samples at different accelerated stress conditions.

TTF data points is depicted in Figure 5.24.

Figure 5.24 shows the unreliability (expressed in percentile) for all the six selected DUT samples tested at different combinations of accelerated aging stress conditions above the nominal conditions (i.e., 25 °C and 5 V). The unreliability of all the tested 24 samples, indicated as the dotted points on the logarithmic plot, shows a linear increasing tend, varying from 10% to 90% on the y-axis against the increasing pseudo TTF data points (between 450 and 850 hours respectively) on the x-axis. The tested AT12 IC sample, under the combined impact of multiple stress factors at the constant stress magnitude of 110 °C and 5 V, showed the least pseudo TTF (514 hours with 90% unreliability) compared to the AT24 (616 hours with 10% unreliability) sample aged at 70 °C and 5 V. Likewise, the AT6 sample aged at 4 V and 110 °C took 549 hours to fail with 90% unreliability, while the AT18 sample survived for 749 hours prior to reaching the similar failure probability. Similarly, the effect of applying various electrical voltage V stress only on the lifetime reliability of the tested ICs, while maintaining the magnitude of the temperature stress, was also observed in Figure 5.24.

While comparing the pseudo TTF data between the AT6 and AT12 samples, it can

be observed that the failure time data for those two DUTs differed by 35 hours for reaching the maximum 90% unreliability. On the other hand, both the tested AT18 and AT24 samples, aged at a similar lower thermal stress (i.e., 70 °C) compared to that of the other two selected tested samples, took longer pseudo TTF based on the observed EMC degradation data. Comparing the unreliability of both these two samples, the AT18 would survive upto 739 hours until reaching the 90% failure probability compared to the other sample AT24 (10% unreliability at 649 hours). Hence, it can be concluded that the unreliability is the minimum for applying the lowest stress magnitude of thermal and electrical voltage stress factors simultaneously on the selected DUTs, as a result it would allow those ICs to survive for longer period of time. Moreover, the developed reliability model also allows to predict the failure time in nominal condition as shown in Figure 5.24. It is observed that the reliability model would plot the predicted unreliability in nominal condition, implying that all those tested samples predicted lifetime would be between 1100 and 1600 hours.

Figure 5.25 showcases the reliability (or non-failure probability) curve that best fits to the estimated lifetime extrapolating data of all the DUT samples in nominal thermal condition. The non-linear decreasing trend of the reliability curve implies that the predicted non-failure or survival probability of the considered DUTs operating in nominal condition would decrease with an increase of operational time. The reliability function $R(t)$ representing this curve is derived based on the developed reliability model, and can be expressed using the mathematical expression provided in (5.33).

Moreover, Figure 5.25 shows that the reliability value on the y-axis remained 1 till 1200 hours, predicting all the 24 selected DUTs would survive in nominal condition upto this time period. In addition, all the 24 data points correspond to the predicted lifetime reliability parameters were plotted on the x-axis against the reliability and/or survival probability values on the y-axis. The reliability curve predicts that the AT12 would fail at around 1150 hours with the 10% survival probability On the other hand, the predicted lifetime reliability of 90% reliability would be observed for the AT24 sample that would fail at around 1350 hours. Thus, it is observed that all the 24 DUT samples would fail beyond the total applied accelerated stress duration. Overall, the developed ALT reliability model could estimate the failure data points which corresponds to those tested IC samples with an acceptable good accuracy, based on the conducted immunity degradation data obtained as a result of accelerated aging due to performing the designed ADT for a specified stress duration. It can be concluded that the tested samples would take longer time to fail with

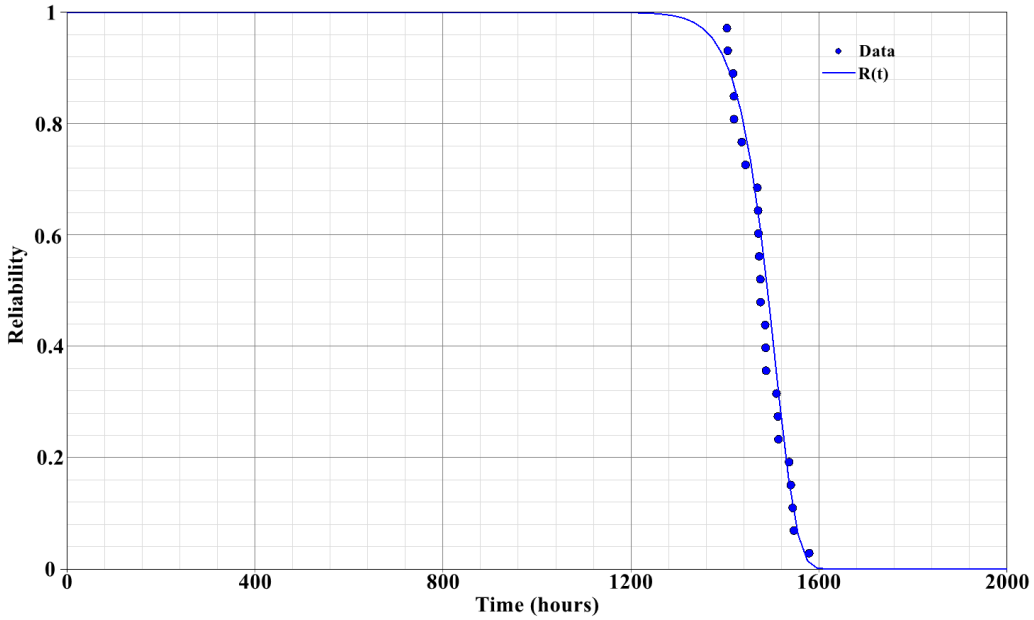


FIGURE 5.25 – Reliability function curve fits to the estimated lifetime data based on the developed ALT reliability model for the tested ICs.

lower predicted lifetime reliability (or non-failure probability).

5.9 Conclusion

Following a new proposed approach on characterizing the EMC performance capacity and its degradation of the tested ICs under various multiple stress conditions, this chapter focused on developing both the degradation and reliability models based on the long-term EMC conducted immunity degradation performance of two types of IC : the selected pin-to-pin compatible functionally identical L78L05 and UA78L05 voltage regulators during the step-stress time-dependent ADTs, and Attiny85 micro-controller IC developed by Atmel, under constant stress ADT plan.

This chapter highlighted on the experimental and measurement procedures applied on The tested IC samples that were subjected to multiple stress factors (thermal and electrical voltage) to maintain accelerated aging throughout the duration of the defined ADT plan. It has also studied the impact of applying constant multiple stress conditions defined by the constant stress ADT plan to characterize the EMC conducted immunity performance degradation of the digital circuit embedded within the studied Attiny85

micro-controller samples.

The long-term evolution of the conducted immunity to the EMI was characterized by performing the DPI tests on both fresh and aged DUTs under nominal conditions, after interrupting for a short time period, the ADT aging process at various stress magnitude and duration. The EMC perfromance measurement data were recorded before and after the ADTs to compare the impact of accelerated aging on the conducted immunity to the harmonic disturbance signal injected into the V_{in} pin of the DUTs. Statistical evaluation of the EMC measurement data was carried out to investigate variation of the mean ΔP_{inj} across the DPI frequencies at different stress time duration.

The ALT-Weibull reliability modeling approach was considered to develop the reliability model as a function of different G and V stress constraints applied on the analog IC regulator samples. The developed ALT model was utilized to predict the unknown model constants of both L78L05 and UA78L05 as well as determine the unreliability of all the tested samples under the combined effect of different user-defined G and V stress conditions. Considering the two different reduced fixed G (i.e., 5% and 10% criteria) compared to the nominal G criterion, it was discovered that pseudo acTTF is reduced at lower G, thereby increasing the probability of failure or unreliability for a specified stress condition. Unreliability showed a decreasing trend with increasing G criterion at fixed V overstress level for both L78L05 and UA78L05 tested samples. However, at a higher G criterion level, higher lifetime reliability (i.e., pseudo TTF) was obtained for both UA78L05 and L78L05 samples. Unlike the tested samples of the UA78L05, L78L05 samples exhibited a lower TTF at higher V stress levels, when a fixed G criterion was applied to the EMC degradation data.

It was found that the pseudo TTF of one of the tested sample of L78L05 for the 10% criterion was (around 362 hours at 9 V with 50% unreliability) compared to the tested UA78L05 IC (around 465 hours with 50% failure probability) at the same threshold criterion and voltage stress level. Moreover, under the influence of 12 V and 10% criterion with 50% unreliability, higher pseudo TTF (around 518 hours) was computed for one of the L78L05 sample compared to that of the UA78L05 sample, whose TTF was 454 hours with the identical predicted unreliability at the same applied V and G constraints. Hence, considering the use of limited sample size, an accurate estimation of the developed ALT-Weibull model could be used to assess and compare the lifetime reliability of both L78L05 and UA78L05 regulator ICs based on the variation in EMC performance at nominal condition as well as under any known or unknown stress conditions.

A physics-based degradation modeling approach was applied to model the monotonic EMC performance degradation at different stress duration to compute pseudo TTF as well as predicting the degradation path model parameters as a function of environmental stress conditions specified in the ADT plan. Estimating the unknown model constants of the developed degradation path model would allow to investigate the gradual conducted immunity degradation behavior of the DUTs under any tested or untested conditions.

It is worth mentioning that the EMC performance degradation data was collected under both thermal step-stress and voltage overstress conditions. Nevertheless, the observed degradation demonstrated that the acceleration factor due to the applied voltage stress level could play a more significant role in the degradation of the tested ICs than thermal stress. Although the developed reliability model allows to assess the lifetime reliability of both UA78L05 and L78l05 tested ICs for any defined threshold and voltage stress level, the limitation of such a model is the possibility to independently estimate the acceleration factor due to temperature stress only (Arrhenius model).

Overall, the presented study's highlights was to characterize and investigate the evolution of the conducted immunity performance of those tested analog ICs caused by the influence of applying external multiple stress conditions, prior to developing the degradation path model to estimate the EMC performance degradation based on the step-stress ADTs measurement data, and followed by integrating the acceleration model with the Weibull distribution to develop the predictive ALT−Webull reliability model for estimating the long-term reliability parameters for the whole lifetime of an electronic component.

It is demonstrated that, for a limited number of samples under the combined influence of thermal step-stress with voltage overstress conditions, the proposed reliability model predicts with a very acceptable accuracy the lifetime reliability of both UA78L05 and L78L05 tested ICs, developed based on the conducted immunity degradation data. Those similar observations were made for all the Attiny85 micro-controller DUTs samples, which were subjected to multiple stress factors (i.e., thermal and electrical voltage) with different combination of constant stress magnitude for a specified stress duration defined in the constant stress ADT plan.

A total of 24 Attiny85 micro-controller ICs were tested under the influence of the designed constant stress ADT plan to analyze the impact of applying multiple stress conditions with four different stress levels. Those selected IC samples were programmed to perform a specified function of digital logic circuits in nominal condition. A similar stress time-dependent accelerated aging methodology presented for the analog ICs was

also implemented for those DUTs to investigate the long-term evolution of the EMR. The conducted immunity variation was also computed to obtain the degradation data for the selected samples, demonstrating significant $|\Delta P_{inj}|$ for AT12 compared to those AT6, AT18 and AT24 samples. Based on the observed monotonic EMC degradation over the entire DPI frequency range, the physics-based model for developing the degradation model was employed, followed by estimating those unknown degradation model constants and determining pseudo TTF data. The generalized Eyring life-stress model combined with the Weibull distribution enabled to develop the reliability model, showcasing acceptable accuracy of the model with the statistically computed TTF data points. Analyzing the reliability modeling results for the tested DUT samples revealed higher unreliability (or failure probability) for the AT12 sample with least TTF data compared to the other tested samples. Hence, it can be concluded that those samples tested at highest aging stress conditions would require least TTF with highest PoF and vice versa.

It is essential to build degradation and predictive reliability models to assess the lifetime reliability of an electronic component over its entire operational lifetime based on the evolution of the EMC degradation observed under the defined accelerated stress conditions. The future perspective of the study would involve proposing and developing the degradation and the ALT reliability models of digital ICs based on the designed ADT plan, which involves combining both constant extreme thermal and voltage overstress conditions for a fixed stress duration. Hence, the implication of the study would enable the IC manufacturers to forecast the lifespan dependability of the tested ICs before exceeding the specified EMC margin or limit. Depending on the applications, the reliability assessment of an DUT based on its conducted immunity performance would allow the system's reliability to be determined. This would enable designers to redesign ICs to improve their lifetime reliability by considering their long-term EMC robustness into account, as well as ensuring the system's compliance with EMC requirements and safety standards. The study's future implications would allow manufacturers to anticipate the functioning of both analog and digital circuits during the lifetime of a system based on EMC requirements, depending on the applications, for estimating the electromagnetic reliability of the electronic system.

General Conclusion and Perspectives

The EMC performance of both analog and digital ICs can have significant impact due to exposure to the harsh environmental conditions. In addition, an IC is expected to operate consistently in an electromagnetic environment, without any failures for an extended period of its lifetime. However, in real-life applications, different failure modes and intrinsic failure mechanisms may be activated by several extreme operational conditions (i.e., temperature, humidity, electrical voltage and so on), causing significant degradation of its conducted immunity level and thus reducing the useful operational life period. Thus, conducting the reliability study of both analog and digital circuits at the IC level is essential for ensuring the proper functionality and maintaining desirable lifetime in an electronic system or product, while taking into account of the EMC behavior of those ICs operating under diverse environmental conditions (i.e., temperature, humidity, atmospheric pressure, electrical voltage and so on).

An extensive literature review was conducted to investigate the aging impact on the conducted immunity and emission performance level of both analog and digital circuits at the IC level. The outcome of those previous research studies demonstrated significant degradation in the conducted immunity and emission levels for both analog and digital ICs, after performing the traditionally available accelerated aging tests (i.e., HTOL and LTOL) in accordance to the defined standard for choosing the stress magnitude and duration. Those aging tests could only compare the EMC performance variation between a fresh and an aged IC after the completion of the aging process. Hence, the time-dependent variation of the EMC immunity and emission performance under the accelerated ageing conditions was not studied in details.

Both constant and step-stress ADT plans were designed and conducted for the selected analog and digital ICs, followed by characterizing the conducted immunity performance evolution in the frequency-domain at different stress time duration. Degradation path model was developed with fairly acceptable accuracy to estimate the EMC performance degradation at any tested or/and any untested accelerated aging stress conditions.

Since commercially available analog and digital IC samples were selected to develop the degradation and lifetime reliability models based on their conducted immunity performance evolution under the influence of harsh environmental stress conditions defined in the ADT plans, the black-box approach is deemed appropriate, as the IC's internal circuit designed with various electronic components are not included in those samples' specifications. Therefore, employing a white-box approach may not be regarded as a suitable technique, as it would necessitate sufficient knowledge on the internal circuit design along with the internal components used to fabricate and manufacture the selected ICs, prior to designing the identical circuit in any simulation software.

The black-box approach was implemented to develop the ICIM-CI model, which required performing the designed ADTs on the selected fresh commercially available IC samples and characterizing the impact of aging on the conducted immunity levels at the IC level. Multiple accelerated ageing stress factors (i.e., thermal and electrical voltage) overstress conditions were applied on the DUTs to investigate and validate the aging influence on the observed EMC performance, resulting significant and/or insignificant variations in the PDN and/or IB blocks of the standard conducted immunity models developed in accordance with the IEC 62433-4 standard. The influence of accelerated aging on the studied IC samples was investigated and their EMC performance degradation was considered to include in the active and/or passive block of the developed ICIM-CI model.

1 - ***Summary of the PhD contributions***

In this document, the overall contributions and findings are divided into four parts, which are briefly summarized below..

In the second chapter, the desirability of employing a simulation model of the designed analog voltage regulator is demonstrated to evaluate the estimation of reliability based on accelerated degradation data. By devising a numerical model to extract the output voltage as a function of temperature and input voltage, the goal was accomplished. In addition, a methodological approach was devised to generate output voltage degradation data under accelerated conditions based on the predictive reliability analysis for the regulator according to the FIDES standard. Using simulated test data, a suitable acceleration law model was adopted to determine the regulator's reliability parameters under accelerated conditions. It has been demonstrated that the estimated lifetime reliability of the proposed regulator design is substantially greater under accelerated aging conditions with a lower failure probability. In accordance with the magnitude of ageing stress type (voltage and temperature) conditions, it was found that the regulator's pseudo TTF was

substantially higher.

In the third chapter, the combined impact of thermal stress and obsolescence is investigated and analyzed by conducting DPI experiments on three functionally identical and pin compatible regulator ICs from three different manufacturers. Under the nominal conditions, experimental results demonstrated that, compared to the other two ICs, the MC78L05 had the highest immunity in high frequency. However, when exposed to both low and high thermal stress magnitudes, that regulator IC model reference was found to be more susceptible to DPI injection. Furthermore, regardless of the IC manufacturer, it was discovered that the DPI immunity increases dramatically with frequency under both high and low environmental stress conditions when compared to the nominal temperatures. These results indicate that it would be essential to confirm IC immunity when replacing a device with one from a second source or one manufactured more recently.

The Z_{11} curves for all of the investigated IC sample references were also compared at low, high, and nominal temperatures. These curves followed a similar trend as frequency increased, albeit with considerable level variances. UA78L05 was found to have a higher package inductance value than the other two ICs, while L78L05 had the lowest capacitance value. As a result of these *RLC* differences, it was feasible to deduce that the UA78L05 was the least immune in high frequency, whereas the L78L05 had high conducted immunity in low frequency.

From the DPI measurements for each of the selected ICs, the IB block tabular data of precise transmitted power versus frequency was then generated at the nominal temperature for each of the ICs. Thus, the conclusion that MC78L05 exhibited the highest conducted immunity relative to the other two ICs was confirmed at high frequency. Consequently, a comparative analysis of the conducted immunity performance of the considered ICs from various manufacturers would be required to verify the electromagnetic compliance of an IC within a system when replacing it with a second-source or a more recent device.

In the fourth chapter, the ICIM-CI models were developed for the selected fresh UA78L05 and L78L05 IC samples. The impact of applying environmental accelerated aging stress conditions on the developed ICIM-CI models was investigated. The ageing impact caused by elevated temperature and voltage overstress was taken into account and incorporated into the developed standardized ICIM-CI model of the tested ICs for analyzing and assessing the effect of ageing on the conducted immunity model of the studied analog ICs.

The DPI measurements were performed on the two pin-to-pin compatible voltage regulator ICs (i.e., L78L05 and UA78L05) to compare and examine the effect of applying different accelerated ageing stresses on their respective developed ICIM-CI models. The PDN block was shown to be unaffected by ageing due to no variation in the overall extracted R, L and C values of the passive lumped electrical components that can be included to represent the PDN block of the developed model.

The DPI immunity test results conducted on the examined aged L78L05 and UA78L05 samples revealed that aging decreases the computed P_trans within the tested DPI frequency range, resulting in a significant impact on the IB block of the developed conducted immunity models for the respective tested L78L05 and UA78L05 samples. As a result of executing the thermal step-stress ADT at the specified stress conditions, while simultaneously applying the constant elevated electrical overstress voltage on the tested samples, aging decreased the electromagnetic conducted immunity levels of the studied ICs samples within a particular frequency range, with UA78L05 exhibiting a greater mean standard deviation of the P_{trans} observed between fresh and aged samples than the L78L05 tested ICs. To take into account for the effect of aging on the IB blocks of the developed ICIM-CI models of the DUT samples as a result of implementing the designed ADT plan, the modified P_{trans} values as a function of frequency should be updated in the power look-up tables by using the statistical deviations of the ageing immunity drift.

Finally, **in the fith chapter**, following a new approach proposed to characterize the EMC performance capability and its degradation of ICs tested under various multiple stress conditions, the final chapter focused on the development of IC degradation and reliability models. This approach was applied to functionally identical and pin-to-pin compatible L78L05 and UA78L05 voltage regulators, and to the Attiny85 micro-controller. The analysis focused on the long-term degradation performance of EMC conducted immunity during ADTs. After defining accelerated test plans following multiple stress factors (i.e., thermal and electrical overstress), experimental and measurement procedures applied to the tested IC samples, a physics-based degradation modeling approach was applied to model the monotonic degradation of EMC performance at different stress duration. This made it possible to calculate the pseudo TTF and predict the model parameters of the degradation path as a function of the environmental stress conditions specified in the ADT plan. Estimation of the unknown parameters of the developed degradation model provides the progressive degradation behavior of DUT conducted immunity under any tested or untested conditions.

It is demonstrated that under the combined influence of thermal step-stress with voltage overstress conditions, the proposed reliability model predicts with a very acceptable accuracy the lifetime reliability of both UA78L05 and L78L05 tested ICs, developed based on the conducted immunity degradation data. This developed ALT reliability model is validated by illustrating the Weibull reliability function curves against time for the tested analog IC samples (L78L05 and UA78L05), which best fits the pseudo TTF data points with good accuracy. The similar outcome was also achieved for testing the digital logic circuit of the Attiny85 micro-controller under the combined influence of both thermal and electrical overstress conditions defined in the constant stress ADT plan, leading to obtain relevant unknown reliability model parameters as well as the degradation path parameters, which would allow to predict the conducted immunity degradation performance as well as predict the unreliability (or survival probability) in both nominal as well as for any tested or untested accelerated conditions. The conducted study on the Attiny85 micro-controller ICs revealed that the developed generalized Eyring-Weibull reliability model could predict the lifetime reliability in nominal condition, demonstrating higher pseudo TTF for those tested samples (i.e., AT12), aged at 110 °C and 5 V, with lower failure probability or unreliability compared to the other tested samples (i.e., AT6, AT18 and AT24) based on the observed EMC degradation data computed at various stress duration. It is worth to mention that the rest of the tested samples showed similar trend in the conducted immunity level degradation, thus validating the above aforementioned outcome and demonstrating acceptable accuracy of the developed degradation and reliability models.

This study demonstrated the characterization and study of the evolution of the conducted immunity performance of tested ICs caused by the influence of the application of multiple external stress conditions. The development of the method provided a degradation path model to estimate the degradation of EMC performance based on measurement data from progressively stressed ADTs, and followed by the integration of the acceleration model with the Weibull distribution to develop the ALT-Webull predictive reliability model to estimate long-term reliability parameters for the entire lifetime of an electronic component.

2 - ***Research prospects***

It is essential to build degradation and predictive reliability models to assess the reliability of an electronic component throughout its operational life, based on the evolution of EMC degradation observed under defined accelerated stress conditions. Depending on the application, assessing the reliability of a DUT on the basis of its conducted immu-

nity performance would enable system reliability to be determined. This would enable designers to redesign ICs to improve their lifetime reliability by considering their long-term EMC robustness, while assuring system compliance with the EMC requirements and safety standards.

Some of the perspectives of the presented research study may also be accounted for various industrial applications, including communication, automotive, can be envisaged.

1. Chapter 2 showed the importance of using analog and digital circuit design and simulation software (i.e., Cadence Virtuoso, LTSpice, Ansys) to model their functional performance as a function of environmental stress conditions. Consideration of this study's model of EMC performance degradation as a function of time would enable manufacturers to predict the operation of analog and digital circuits over the lifetime of a system based on EMC requirements, depending on application, in order to estimate the electromagnetic reliability of the electronic system. This would also help IC designers to apply EMC mitigation techniques on the ICs so that their EMC compliance limit would be maintained throughout the operational lifetime.
2. In this report, a black-box approach to developing degradation and reliability models based on acEMC immunity measurement data was considered. Various simulation programs, including IC-EMC, Cadence Virtuoso, and Ansys, can be used to design CMOS-based analog and digital circuits, followed by simulations of conducted emission and immunity under thermal stress and/or aging conditions. The simulation results can then be used to develop predictive models, which can be compared to reliability models developed using measured data. By comparing the simulation model to the developed measurement model, the applied methodology for integrating the conducted immunity and reliability models can be validated. In addition, the fundamental causes of the observed EMC degradation can be determined by simulating the CMOS transistors affected by the application of accelerated aging conditions in order to identify those affected. This would enable the IC designers and manufacturers to forecast the lifetime reliability of various analog and digital circuit blocks embedded in an electronic system.
3. The IEC 62132-4 standard defines DPI the immunity criterion. Based on the results of this study, the standard could be modified to take into account of changes in performance over time.

In this manuscript, degradation and reliability modeling approaches have been presen-

ted to investigate the long-term EMR of the studied analog and digital ICs. Nevertheless, further developments and issues with various future aspects can be considered for conducting further research in the field of integrating IC-EMC reliability. Some of the promising aspects for emphasizing on the future development in this field of research have been identified as mentioned below ;

1. The DPI test bench configuration consists of numerous components with a specified degree of measurement uncertainty, which may have a significant impact on creating some measurement inaccuracy. The average or mean value of the measurement data allowed us to limit the influence of such inaccuracy in our method. The measurement error, on the other hand, can be included in the construction of a stochastic deterioration process, such as the Wiener process. When quality control procedures are applied to test data, it is feasible to discern between normal measurement errors caused by experimental equipment and those caused by human error.
2. Throughout the report, conducted immunity performance degradation was investigated by performing the DPI test in the frequency domain. Degradation modeling followed by the lifetime reliability was demonstrated based on the observed EMC degradation data computed by performing this non-destructive mode of experiments. However, characterizing the conducted immunity performance of both analog and digital ICs in the time-domain by performing the EFT, as discussed in the first chapter, is also an important aspect of investigating the EMC performance of ICs. In this case, the development of degradation models requires a method of taking into account the cumulative damage caused by EFT injection causing different types of failure.
3. Since EFT is a destructive method of assessing the conducted immunity of the tested ICs, prior to exploring the conducted immunity variation of the selected ICs under the influence of accelerated ageing conditions, ICs test samples with sufficient ESD protection networks can be selected or designed along with the custom-designed PCB by following proper EMC compliance design rules. This is essential so that the EFT measurement data can performed properly on both fresh and aged ICs at various stress times and different kinds of failure modes can be observed.
4. In this report, analog and digital ICs, with a significant number of samples were tested to identify the statistical variation of the EMC data for developing ac-

curate reliability models. Applying statistical computations to develop the EMC degradation data of all those samples individually is time-consuming. Machine learning techniques can be employed to train the surrogate model for large number of samples. This would allow to develop reliability models with large number of samples for any ICs with similar functionality, design and applications.

BIBLIOGRAPHIE

[1] B. Li, A. Boyer, S. Bendhia et C. Lemoine, « Ageing effect on electromagnetic susceptibility of a phase locked loop », en, *Microelectronics Reliability*, t. 50, *9-11*, p. 1304-1308, sept. 2010, ISSN : 00262714. DOI : 10.1016/j.microrel.2010.07.100. adresse : https://linkinghub.elsevier.com/retrieve/pii/S0026271410003732 (visité le 26/01/2022).

[2] B. Li, A. Boyer, S. B. Dhia et C. Lemoine, « Ageing effect on immunity of a mixed signal IC », en, in *2010 Asia-Pacific International Symposium on Electromagnetic Compatibility*, Beijing, China : IEEE, 2010, p. 1024-1027, ISBN : 978-1-4244-5621-5. DOI : 10.1109/APEMC.2010.5475532.

[3] J. Wu, A. Boyer, J. Li, S. B. Dhia et R. Shen, « Characterization of Changes in LDO Susceptibility After Electrical Stress », en, *IEEE Transactions on Electromagnetic Compatibility*, t. 55, *5*, p. 883-890, oct. 2013, ISSN : 0018-9375, 1558-187X. DOI : 10.1109/TEMC.2013.2242471.

[4] S. Ben Dhia et A. Boyer, « Electro-magnetic robustness of integrated circuits : from statement to prediction », en, in *2013 9th International Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, Nara, Japan : IEEE, déc. 2013, p. 208-213, ISBN : 978-1-4799-2315-1. DOI : 10.1109/EMCCompo.2013.6735202.

[5] S. Ben Dhia et A. Boyer, « A review of research on the effect of aging on the EMC of integrated circuits », en, in *2016 Asia-Pacific International Symposium on Electromagnetic Compatibility (APEMC)*, Shenzhen, China : IEEE, mai 2016, p. 1153-1155, ISBN : 978-1-4673-9494-9. DOI : 10.1109/APEMC.2016.7522971.

[6] M. Ramdani, E. Sicard, A. Boyer et al., « The Electromagnetic Compatibility of Integrated Circuits—Past, Present, and Future », en, *IEEE Transactions on Electromagnetic Compatibility*, t. 51, *1*, p. 78-100, fév. 2009, ISSN : 0018-9375. DOI : 10.1109/TEMC.2008.2008907.

[7] R. B. Keller, *Design for Electromagnetic Compatibility–In a Nutshell : Theory and Practice*, en. Cham : Springer International Publishing, 2023, isbn : 978-3-031-14186-7. doi : 10.1007/978-3-031-14186-7.

[8] J. A. Rashid, M. Koohestani, L. Saintis et M. Barreau, « A State-of-the-Art Review on IC EMC Reliability », en, in *Proceedings of the 31st European Safety and Reliability Conference (ESREL 2021)*, Research Publishing Services, 2021, p. 1850-1857, isbn : 978-981-18201-6-8. doi : 10.3850/978-981-18-2016-8_154-cd. (visité le 12/02/2023).

[9] H. Kunkel et S. Klezar, « Electric fast transients (EFT) : The revision of IEC 61000-4-4 », in *8th International Conference on Electromagnetic Interference and Compatibility*, IEEE, 2003, p. 403-408.

[10] « IEC 61000-4-4 :2012 », en, International Electrotechnical Commission (IEC), International standard, avr. 2012, p. 87. adresse : https://webstore.iec.ch/publication/4222.

[11] J. Wu, C. Li, B. Li, W. Zhu et H. Wang, « Microcontroller susceptibility variations to EFT burst during accelerated aging », en, *Microelectronics Reliability*, t. 64, p. 210-214, sept. 2016, issn : 00262714. doi : 10.1016/j.microrel.2016.07.099.

[12] S. Bauer, B. Deutschmann et G. Winkler, « Prediction of the robustness of integrated circuits against EFT/BURST », en, in *2015 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, Dresden, Germany : IEEE, août 2015, p. 45-49, isbn : 978-1-4799-6616-5. doi : 10.1109/ISEMC.2015.7256130.

[13] J. Nie, X. Chen, W. Shao et W. Fang, « Susceptibility of a microcontroller against electrical fast transients disturbances », en, *Journal of Physics : Conference Series*, t. 1074, p. 012 117, sept. 2018, issn : 1742-6588, 1742-6596. doi : 10.1088/1742-6596/1074/1/012117.

[14] J. Wu, B. Li, W. Zhu, H. Wang et L. Zheng, « Investigations on the EFT immunity of microcontrollers with different architectures », en, *Microelectronics Reliability*, t. 76-77, p. 708-713, sept. 2017, issn : 00262714. doi : 10.1016/j.microrel.2017.06.078.

[15] A. Alaeldine, R. Perdriau, M. Ramdani, J.-L. Levant et M. Drissi, « A Direct Power Injection Model for Immunity Prediction in Integrated Circuits », en,

IEEE Transactions on Electromagnetic Compatibility, t. 50, *1*, p. 52-62, 2008, ISSN : 0018-9375. DOI : 10.1109/TEMC.2007.911920.

[16] « IEC 62132-4 : Integrated Circuits, Measurement of Electromagnetic Immunity – Part 4 : Direct RF Power Injection Method », IEC, Geneva, Switzerland, International standard, 2003.

[17] I. Chahine, M. Kadi, E. Gaboriaud, A. Louis et B. Mazari, « Characterization and Modeling of the Susceptibility of Integrated Circuits to Conducted Electromagnetic Disturbances Up to 1 GHz », en, *IEEE Transactions on Electromagnetic Compatibility*, t. 50, *2*, p. 285-293, mai 2008, ISSN : 0018-9375, 1558-187X. DOI : 10.1109/TEMC.2008.918983.

[18] J. Wu, A. Boyer, J. Li et al., « Modeling and Simulation of LDO Voltage Regulator Susceptibility to Conducted EMI », en, *IEEE Transactions on Electromagnetic Compatibility*, t. 56, *3*, p. 726-735, juin 2014, ISSN : 0018-9375, 1558-187X. DOI : 10.1109/TEMC.2013.2294951. adresse : http://ieeexplore.ieee.org/document/6695801/.

[19] J.-l. Levant, M. Ramdani et R. Perdriau, « Power- Supply Network Modeling », en, p. 5,

[20] S. H. Airieau, T. Dubois, G. Duchamp et A. Durier, « Multiport ICIM-CI modeling approach applied to a bandgap voltage reference », en, in *2016 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, Wroclaw, Poland : IEEE, sept. 2016, p. 526-531, ISBN : 978-1-5090-1416-3. DOI : 10.1109/EMCEurope.2016.7739248. adresse : http://ieeexplore.ieee.org/document/7739248/ (visité le 26/01/2022).

[21] A. Durier, P. Fernandez-Lopez, J.-L. Levant et C. Marot, « ICIM-CPI : Integrated circuits immunity model : Conducted pulse immunity : Description, extraction and example », en, in *2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC)*, Singapore : IEEE, mai 2018, p. 695-700, ISBN : 978-1-5090-5997-3. DOI : 10.1109/ISEMC.2018.8393871.

[22] J. Zhang, J. Koo, R. Moseley et al., « Modeling Injection of Electrical Fast Transients Into Power and IO Pins of ICs », en, *IEEE Transactions on Electromagnetic Compatibility*, t. 56, *6*, p. 1576-1584, déc. 2014, ISSN : 0018-9375, 1558-187X.

DOI : 10.1109/TEMC.2014.2332499. adresse : https://ieeexplore.ieee.org/document/6863668 (visité le 21/02/2022).

[23] M. Stockinger, J. W. Miller, M. G. Khazhinsky et al., « Boosted and Distributed Rail Clamp Networks for ESD Protection in Advanced CMOS Technologies », en,

[24] A. Boyer, S. Ben Dhia, B. Li, C. Lemoine et B. Vrignon, « Prediction of Long-term Immunity of a Phase-Locked Loop », en, *Journal of Electronic Testing*, t. 28, *6*, p. 791-802, déc. 2012, ISSN : 0923-8174, 1573-0727. DOI : 10.1007/s10836-012-5335-y.

[25] Ji Zhang, Jayong Koo, D. G. Beetner, R. Moseley, S. Herrin et D. Pommerenke, « Modeling of the immunity of ICs to EFTs », en, in *2010 IEEE International Symposium on Electromagnetic Compatibility*, Fort Lauderdale, FL : IEEE, juill. 2010, p. 484-489, ISBN : 978-1-4244-6305-3. DOI : 10.1109/ISEMC.2010.5711323. adresse : http://ieeexplore.ieee.org/document/5711323/ (visité le 21/02/2022).

[26] A. Boyer et S. Ben Dhia, « Characterization and modeling of electrical stresses on digital integrated circuits power integrity and conducted emission », en, in *2013 9th International Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, Nara, Japan : IEEE, déc. 2013, p. 190-195, ISBN : 978-1-4799-2315-1. DOI : 10.1109/EMCCompo.2013.6735199. adresse : http://ieeexplore.ieee.org/document/6735199/ (visité le 02/03/2022).

[27] T. Dubois, S. Hairoud, M. Gomes de Oliveira, H. Frémont et G. Duchamp, « Characterization and model of temperature effect on the conducted immunity of Op-Amp », en, *Microelectronics Reliability*, t. 55, *9-10*, p. 2055-2060, août 2015, ISSN : 00262714. DOI : 10.1016/j.microrel.2015.06.018.

[28] H. Huang, A. Boyer, S. Ben Dhia et B. Vrignon, « Prediction of aging impact on electromagnetic susceptibility of an operational amplifier », en, in *2015 Asia-Pacific Symposium on Electromagnetic Compatibility (APEMC)*, Taipei, Taiwan : IEEE, mai 2015, p. 86-89, ISBN : 978-1-4799-6668-4 978-1-4799-6670-7. DOI : 10.1109/APEMC.2015.7175235.

[29] A. Boyer et S. B. Dhia, « Effect of Aging on Power Integrity and Conducted Emission of Digital Integrated Circuits », en, *Journal of Low Power Electronics*, t. 10, *1*, p. 165-172, mars 2014, ISSN : 15461998. DOI : 10.1166/jolpe.2014.1307.

[30] G. Yang, *Life Cycle Reliability Engineering*, en. Wiley, fév. 2007, isbn : 978-0-471-71529-0.

[31] A. Bensoussan, « M-STORM reliability model applied to DSM technologies », en, in *2016 IEEE Nanotechnology Materials and Devices Conference (NMDC)*, Toulouse, France : IEEE, oct. 2016, p. 1-2, isbn : 978-1-5090-4352-1. doi : 10.1109/NMDC.2016.7777115. adresse : http://ieeexplore.ieee.org/document/7777115/ (visité le 16/03/2022).

[32] A. Boyer, S. B. Dhia, B. Li, N. Berbel et R. Fernandez-Garcia, « Experimental Investigations into the Effects of Electrical Stress on Electromagnetic Emission from Integrated Circuits », en, *IEEE Transactions on Electromagnetic Compatibility*, t. 56, *1*, p. 44-50, fév. 2014, issn : 0018-9375, 1558-187X. doi : 10.1109/TEMC.2013.2272195.

[33] A. Boyer, A. C. Ndoye, S. Ben Dhia, L. Guillot et B. Vrignon, « Characterization of the Evolution of IC Emissions After Accelerated Aging », en, *IEEE Transactions on Electromagnetic Compatibility*, t. 51, *4*, p. 892-900, nov. 2009, issn : 0018-9375, 1558-187X. doi : 10.1109/TEMC.2009.2033577.

[34] C. Ghfiri, A. Boyer, A. Bensoussan, A. Durier et S. Ben Dhia, « A New Methodology for EMC Prediction of Integrated Circuits After Aging », en, *IEEE Transactions on Electromagnetic Compatibility*, p. 1-10, 2018, issn : 0018-9375, 1558-187X. doi : 10.1109/TEMC.2018.2819722.

[35] « MIL-HDBK-217F, MILITARY HANDBOOK : RELIABILITY PREDICTION OF ELECTRONIC EQUIPMENT », rapp. tech., déc. 1991.

[36] V. Huard, M. Denais, F. Perrier et al., « A thorough investigation of MOSFETs NBTI degradation », *Microelectronics Reliability*, t. 45, *1*, p. 83-98, 2005.

[37] H. Tahi, C. Tahanout, M. Boubaaya et al., « Experimental investigation of NBTI degradation in power VDMOS transistors under low magnetic field », *IEEE Transactions on Device and Materials Reliability*, t. 17, *1*, p. 99-105, 2017.

[38] N. Stojadinovic, D. Dankovic, I. Manic, V. Davidovic, S. Djoric-Veljkovic et S. Golubovic, « Impact of negative bias temperature instabilities on lifetime in p-channel power VDMOSFETs », in *2007 8th International Conference on Telecommunications in Modern Satellite, Cable and Broadcasting Services*, IEEE, 2007, p. 275-282.

[39] J. B. Bernstein, M. Gabbay et O. Delly, « Reliability matrix solution to multiple mechanism prediction », en, *Microelectronics Reliability*, t. 54, *12*, p. 2951-2955, déc. 2014, issn : 00262714. doi : 10.1016/j.microrel.2014.07.115. adresse : https://linkinghub.elsevier.com/retrieve/pii/S0026271414003114 (visité le 16/03/2022).

[40] A. Bensoussan, « Microelectronic reliability models for more than moore nanotechnology products », *Facta Universitatis, Series : Electronics and Energetics*, t. 30, *1*, p. 1-25, 2016.

[41] E. Bender, J. Bernstein et A. Bensoussan, « Reliability prediction of FinFET FPGAs by MTOL », en, *Microelectronics Reliability*, t. 114, p. 113 809, nov. 2020, issn : 00262714. doi : 10.1016/j.microrel.2020.113809. adresse : https://linkinghub.elsevier.com/retrieve/pii/S002627142030408X (visité le 16/03/2022).

[42] J. B. Bernstein, A. Bensoussan et E. Bender, « Reliability prediction with MTOL », en, *Microelectronics Reliability*, t. 68, p. 91-97, jan. 2017, issn : 00262714. doi : 10.1016/j.microrel.2016.09.005.

[43] J. B. Bernstein, « Reliability Prediction for Aerospace Electronics : » en, Defense Technical Information Center, Fort Belvoir, VA, rapp. tech., avr. 2015. doi : 10.21236/ADA621707.

[44] Y.-C. Chang, S. S. Hsu, Y.-T. Chang, C.-K. Chen, H.-C. Cheng et D.-C. Chang, « The direct RF power injection method up to 18 GHz for investigating IC's susceptibility », in *2013 9th International Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, IEEE, 2013, p. 167-170.

[45] F. Lafon, F. de Daran, M. Ramdani, R. Perdriau et M. Drissi, « Extending the frequency range of the direct power injection test : Uncertainty considerations and modeling approach », in *7th International Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC COMPO 09)*, 2009.

[46] « Integrated Circuit Immunity Modelling Beyond [1]GHz », en,

[47] J.-f. Wu, J.-c. Li, A. Boyer, H.-y. Wang, X.-c. Gu et R.-j. Shen, « LDO EMC susceptibility modeling with on-chip sensor measurements », in *2012 6th Asia-Pacific Conference on Environmental Electromagnetics (CEEM)*, IEEE, 2012, p. 270-273.

[48] J. A. Rashid, L. Saintis, M. Koohestani et M. Barreau, « Coupling simulation and accelerated degradation model for reliability estimation : Application to a voltage regulator », *Microelectronics Reliability*, p. 114 682, 2022, issn : 0026-2714. doi : https://doi.org/10.1016/j.microrel.2022.114682.

[49] S. Hairoud-Airieau, G. Duchamp, T. Dubois, J.-Y. Delétage, A. Durier et H. Frémont, « Effects of ageing on the conducted immunity of a voltage reference : Experimental study and modelling approach », en, *Microelectronics Reliability*, t. 76-77, p. 674-679, sept. 2017, issn : 00262714. doi : 10.1016/j.microrel.2017.07.030. adresse : https://linkinghub.elsevier.com/retrieve/pii/S0026271417303141.

[50] S. T. OP 'T LAND, « Integrated Circuit immunity modelling beyond 1 GHz" », Univ. of INSA Rennes 1, Rennes, France, pHd DISSERTATION, 2014.

[51] A. R. 7029-3531, *Amphenol RF 7029-3531, ATC-PS TEST CBL SMA(M)X2 6FT, Mouser Electronics [Online]*. adresse : https://www.mouser.fr/ProductDetail/Amphenol-SV-Microwave/7029-3531?qs=DRkmTr78QATPXgEuvstMmg%3D%3D.

[52] F. LAFON, « Techniques and methodologies development to take into account EMC constraints in Automotive equipment design », France, PhD dISSERTATION, 2011.

[53] S. Ben Dhia, A. Boyer, B. Li et A. Cisse Ndoye, « Characterisation of electromagnetic compatibility drifts of nanoscale integrated circuit after accelerated life tests », en, *Electronics Letters*, t. 46, *4*, p. 278, 2010, issn : 00135194. doi : 10.1049/el.2010.2885.

[54] R. Fernández, R. Rodri, M. Nafri, X. Aymerich et al., « Effect of oxide breakdown on RS latches », *Microelectronics Reliability*, t. 47, *4-5*, p. 581-584, 2007.

[55] *Failure Mechanism Based Stress Test Qualification for Integrated Circuits*, sept. 2014.

[56] J. Wu, A. Boyer, J. Li, S. B. Dhia et R. Shen, « Characterization of changes in LDO susceptibility after electrical stress », *IEEE transactions on electromagnetic compatibility*, t. 55, *5*, p. 883-890, 2013.

[57] *"EMC IC modelling — part 4 : models of integrated circuits for EMI behavioural simulation, conducted immunity modeling (ICIM-CI)", IEC 62433-4 ;* 2016. adresse : https://standards.iteh.ai/catalog/standards/iec/ed29d356-6ef1-4dff-8659-a79887c09dea/iec-62433-4-2016.

[58] Q. M. Khan, M. Koohestani, J.-L. Levant, M. Ramdani et R. Perdriau, « Validation of IC Conducted Emission and Immunity Models Including Aging and Thermal Stress », en, *IEEE Transactions on Electromagnetic Compatibility*, p. 1-14, 2023, issn : 0018-9375, 1558-187X. doi : 10.1109/TEMC.2023.3253385.

[59] Y. Huang, J. Wu, Chuangwei Li et Wei Zhu, « Investigation on EFT effects in a low dropout voltage regulator », en, in *2016 Asia-Pacific International Symposium on Electromagnetic Compatibility (APEMC)*, Shenzhen, China : IEEE, mai 2016, p. 214-217, isbn : 978-1-4673-9494-9. doi : 10.1109/APEMC.2016.7523013. adresse : http://ieeexplore.ieee.org/document/7523013/ (visité le 21/02/2022).

[60] J. Al Rashid, M. Koohestani, R. Perdriau, L. Saintis et M. Barreau, « Combining Obsolescence and Temperature Stress to Evaluate the Immunity of Voltage Regulators to Direct Power Injection in Long-Lifespan Systems », *IEEE Letters on Electromagnetic Compatibility Practice and Applications*, t. 5, p. 27-32, mars 2023, issn : 2637-6423. doi : 10.1109/LEMCPA.2023.3240621.

[61] J. B. Bernstein et J. Qin, « Physics based reliability qualification », in *IEEE International Reliability Physics Symposium*, 2007.

[62] M. White, « Microelectronics reliability : physics-of-failure based modeling and lifetime evaluation », 2008.

[63] F. JENSEN, « ELECTRONIC COMPONENT RELIABILITY », 1995.

[64] W. Q. Meeker, L. A. Escobar et C. J. Lu, « Accelerated degradation tests : modeling and analysis », *Technometrics*, t. 40, *2*, p. 89-99, 1998.

[65] A. Bensoussan Alain, *State of the art of the predictive approach to reliability," Deliverable L1.1, Robustness project, IRT Saint-Exup´ery*, 2014.

[66] F. Guérin, M. Barreau, A. Charki, A. Todoskoff, S. Cloupet et D. Bigaud, « Reliability Estimation of Mechanical Components Using Accelerated Life Testing Models », 2010. adresse : https://api.semanticscholar.org/CorpusID:115623298.

[67] N. Balakrishnan, E. Castilla et M. H. Ling, « Optimal designs of constant-stress accelerated life-tests for one-shot devices with model misspecification analysis », *Quality and Reliability Engineering International*, t. 38, *2*, p. 989-1012, 2022.

[68] S. Zhao, S. Chen et H. Wang, « Degradation modeling for reliability estimation of DC film capacitors subject to humidity acceleration », *Microelectronics Reliability*, t. 100, p. 113 401, 2019.

[69] N. Gorjian, L. Ma, M. Mittinty, P. Yarlagadda et Y. Sun, « A review on degradation models in reliability analysis », en, in *Engineering Asset Lifecycle Management*, D. Kiritsis, C. Emmanouilidis, A. Koronios et J. Mathew, éd., London : Springer London, 2010, p. 369-384, isbn : 978-0-85729-321-3 978-0-85729-320-6. doi : 10.1007/978-0-85729-320-6_42. (visité le 01/06/2023).

[70] Z.-S. Ye et N. Chen, « The inverse Gaussian process as a degradation model », *Technometrics*, t. 56, *3*, p. 302-311, 2014.

[71] Z.-S. Ye, Y. Wang, K.-L. Tsui et M. Pecht, « Degradation data analysis using Wiener processes with measurement errors », *IEEE Transactions on Reliability*, t. 62, *4*, p. 772-780, 2013.

[72] Y. Zhou et M. Huang, « Lithium-ion batteries remaining useful life prediction based on a mixture of empirical mode decomposition and ARIMA model », *Microelectronics Reliability*, t. 65, p. 265-273, 2016.

[73] W. Yan, X. Xu, D. Bigaud et W. Cao, « Optimal design of step-stress accelerated degradation tests based on the Tweedie exponential dispersion process », *Reliability Engineering & System Safety*, t. 230, p. 108 917, 2023.

[74] Z. Pan et N. Balakrishnan*, « Multiple-steps step-stress accelerated degradation modeling based on Wiener and gamma processes », *Communications in Statistics-Simulation and Computation*, t. 39, *7*, p. 1384-1402, 2010.

[75] L. Lu, B. Wang, Y. Hong et Z. Ye, « General path models for degradation data with multiple characteristics and covariates », *Technometrics*, t. 63, *3*, p. 354-369, 2021.

[76] J. Song, A. Shukla et R. Probst, « Prediction of failure in time (FIT) of electrical connectors with short term tests », *Microelectronics Reliability*, t. 138, p. 114 684, 2022.

[77] P. Jiang, B. Wang, X. Wang et Z. Zhou, « Inverse Gaussian process based reliability analysis for constant-stress accelerated degradation data », *Applied Mathematical Modelling*, t. 105, p. 137-148, 2022.

[78] W. Huang et D. L. Dietrich, « An alternative degradation reliability modeling approach using maximum likelihood estimation », *IEEE transactions on reliability*, t. 54, *2*, p. 310-317, 2005.

[79] H. Li, Z. Zhang, Y. Hu et D. Zheng, « Maximum likelihood estimation of weibull distribution based on random censored data and its application », in *2009 8th International Conference on Reliability, Maintainability and Safety*, IEEE, 2009, p. 302-304.

[80] J.-C. Lu, J. Park et Q. Yang, « Statistical inference of a time-to-failure distribution derived from linear degradation data », *Technometrics*, t. 39, *4*, p. 391-400, 1997.

[81] C. J. Lu et W. O. Meeker, « Using degradation measures to estimate a time-to-failure distribution », *Technometrics*, t. 35, *2*, p. 161-174, 1993.

[82] C. M. Tan et F. He, « Predicting integrated circuit reliability from wafer fabrication technology reliability data », in *2007 International Symposium on Integrated Circuits*, IEEE, 2007, p. 267-270.

[83] W.-T. K. Chien et F. Hao, « An extended building-in reliability methodology on evaluating SRAM reliability by wafer-level reliability systems », *IEEE Transactions on Device and Materials Reliability*, t. 20, *1*, p. 106-118, 2020.

[84] L. Yang, P. A. Agyakwa et C. M. Johnson, « Physics-of-failure lifetime prediction models for wire bond interconnects in power electronic modules », *IEEE Transactions on Device and Materials Reliability*, t. 13, *1*, p. 9-17, 2012.

[85] J. Al Rashid, L. Saintis, M. Koohestani et M. Barreau, « Coupling simulation and accelerated degradation model for reliability estimation : Application to a voltage regulator », en, *Microelectronics Reliability*, 33rd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, p. 5, sept. 2022, issn : 0026-2714. doi : 10.1016/j.microrel.2022.114682.

[86] J. A. Rashid, M. Koohestani, L. Saintins et M. Barreau, « High Temperature Accelerated Ageing Influence on the Conducted Immunity Modelling of the Commonly Used Voltage Regulator ICs », in *in International Symposium and Exhibition on Electromagnetic Compatibility*, IEEE Xplore, sept. 2023.

[87] C. Ghfiri, A. Boyer, A. Bensoussan, A. Durier et S. Ben Dhia, « A New Methodology for EMC Prediction of Integrated Circuits After Aging », en, *IEEE Transactions on Electromagnetic Compatibility*, p. 1-10, 2018, issn : 0018-9375, 1558-187X. doi : 10.1109/TEMC.2018.2819722.

[88] Ghfiri, A. Durier, A. Boyer et S. Ben Dhia, « A new methodology to extract the ICEM-CE internal activity block of a FPGA », en, in *2017 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, Angers : IEEE, sept. 2017, p. 1-6, isbn : 978-1-5386-0689-6. doi : 10.1109/EMCEurope.2017.8094792.

[89] « ATtiny25/ATtiny45/ATtiny85, Appendix B - Automotive Specification at 1.8V », en,

[90] A. Boyer, S. B. Dhia, B. Li, N. Berbel et R. Fernandez-Garcia, « Experimental investigations into the effects of electrical stress on electromagnetic emission from integrated circuits », *IEEE transactions on electromagnetic compatibility*, t. 56, *1*, p. 44-50, 2013.

[91] A. Boyer et S. Ben Dhia, « Effect of electrical stresses on digital integrated circuits power integrity », en, in *2013 17th IEEE Workshop on Signal and Power Integrity*, Paris, France : IEEE, mai 2013, p. 1-4, isbn : 978-1-4673-5679-4 978-1-4673-5678-7 978-1-4673-5677-0. doi : 10.1109/SaPIW.2013.6558327.

DOCTORAT BRETAGNE SCIENCES LOIRE POUR L'INGENIEUR

université angers

Titre : Modèles de dégradation et de fiabilité pour évaluer les performances de compatibilité électromagnétique des circuits intégrés sous contraintes environnementales

Mot clés : compatibilité électromagnétique, injection directe de puissance, immunité conduite, test de durée de vie accélérée, modélisation de la fiabilité, modèle de dégradation basé sur la physique

Résumé : Les conditions environnementales sévères peuvent avoir un effet significatif sur les performances en compatibilité électromagnétique (CEM) des circuits intégrés analogiques et numériques. En outre, un circuit intégré doit fonctionner de manière fiable dans un environnement électromagnétique. Dans cette thèse, des plans d'essai de dégradation accélérée sous contraintes constantes et échelonnées ont été mis en oeuvre pour les circuits intégrés analogiques et numériques sélectionnés, suivis par la caractérisation de l'évolution de la performance de l'immunité conduite dans le domaine fréquentielle sous différentes durées de contrainte. Pour estimer la dégradation des performances CEM dans des conditions de vieillissement accéléré testées ou non, un modèle de dégradation basé sur la physique est combiné à un modèle de durée de vie accélérée pour prédire les métriques de fiabilité. L'approche boîte noire a été utilisée pour construire le modèle d'immunité conduite, qui a nécessité la caractérisation de l'effet du vieillissement au niveau du circuit intégré. L'influence du vieillissement accéléré sur dégradation des performances CEM a été incluse dans les blocs actifs et/ou passifs du modèle d'immunité.

Title: Degradation and Lifetime Reliability Models to Assess the Electromagnetic Compatibility Performance of Integrated Circuits Under Environmental Constraints

Keywords: electromagnetic compatibility, direct power injection, conducted immunity, accelerated degradation test, reliability modeling, physics-based degradation model

Abstract: The severe environmental conditions can have a significant effect on the electromagnetic compatibility (EMC) performance of both analog and digital integrated circuits (IC). In addition, an IC is expected to operate reliably in an electromagnetic environment. In this thesis, both constant and step-stress accelerated degradation test plans were implemented on selected analog and digital ICs, followed by the characterization of the conducted immunity performance evolution in the frequency-domain at various stress time duration. To estimate the EMC performance degradation under any tested or untested accelerated aging stress conditions, a physics-based degradation path model was combined with accelerated lifetime model to predict reliability metrics. The black-box approach was used to construct the conducted immunity model, which required characterizing the effect of aging at IC level. The influence of accelerated aging on EMC performance degradation was included in the active and/or passive blocks of the immunity model.