Optimization of dielectric/GaN interface for MIS gate power devices

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THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ GRENOBLE ALPES

École doctorale : EEATS - Electronique, Electrotechnique, Automatique, Traitement du Signal (EEATS)
Spécialité : Nano électronique et Nano technologies
Unité de recherche : Laboratoire d'Electronique et de Technologie de l'Information (LETI)

Optimisation de l'interface diélectrique/GaN pour la grille MIS des transistors de puissance

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Thèse soutenue publiquement le **28 novembre 2023**, devant le jury composé de :

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"The interface is the device"
- Herbert Kroemer

Résumé

L'augmentation de la consommation électrique est un phénomène exponentiel depuis les années 1970 dans tous les secteurs concernées. De plus, face au réchauffement climatique, le mouvement actuel vers l'électrification massive ainsi que l'augmentation des sources d'énergies renouvelables amènent des nouvelles exigences en matière de gestion et de distribution d'énergie. Notamment, une conversion d'énergie électrique plus efficace pour différentes applications serait bénéfique afin de limiter les pertes d'énergies. Une telle conversion consiste à convertir le courant alternatif (AC) ou le courant continu (DC) à différents niveaux de tension, fréquences ou types de courant. Cette tâche est assurée par l'électronique de puissance, où la conversion d'énergie est effectuée par des modules de puissance composés de composants passifs tels que des condensateurs ou des inductances, et de composants actifs tels que des transistors. Initialement basés sur des composants en silicium, ces derniers ne sont pas en mesure de répondre aux nouvelles demandes (e.g. puissance transmise, fréquence de commutation, efficacité) en raison de leurs limitations physiques. Cela a incité l'industrie et les instituts de recherche à développer de nouveaux composants de puissance basés sur des matériaux à large bande interdite (WBG) tels que le carbure de silicium (SiC) et le nitrure de gallium (GaN). En effet, ces matériaux présentent de meilleures propriétés physiques que le silicium telles qu'une tension de claquage et une vitesse de saturation des électrons plus élevée, tout comme des meilleurs propriétés thermiques. Par conséquent, les composants basés sur les WBG peuvent convertir une plus grande quantité d'énergie ou à une fréquence plus élevée, le tout avec plus d'efficacité grâce à la réduction des pertes en conduction et en commutation.

Concernant le GaN, si des applications en optoélectronique et en Radio-Fréquence sont déjà possible ou améliorées par l'utilisation du GaN par rapport au Si, son utilisation en électronique de puissance constitue une perspective prometteuse pour ce domaine. Grâce à sa large bande interdite et sa vitesse de saturation des électrons élevée, l'utilisation du GaN permet de fabriquer des composants avec une fréquence de commutation plus élevée que ceux à base de Si. Ainsi, les modules de puissance avec des composants à base de GaN sont plus efficace tout en ayant une taille réduite. Ceci est notamment le cas de l'hétérojonction AlGaN/GaN dans laquelle se forme à l'interface un gaz électronique bidimensionnel (2DEG) à haute mobilité électronique. Avec cette structure, les transistors à haute mobilité électronique, dit « HEMT », peuvent être fabriqués avec l'avantage d'avoir une résistance à l'état passant (R_{ON}) plus faible et une fréquence de commutation plus élevée. Néanmoins, ces transistors ont un comportement dit « Normally-ON », ce qui signifie qu'ils ont une tension de seuil négative (V_{TH}<0). Ceci est préjudiciable en électronique de puissance car cela pose des problèmes de sécurité tout comme cela complexifie le design du convertisseur. Par conséquent, les HEMTs « Normally-OFF » (V_{TH}>0) sont hautement souhaitables et recherchés. Différentes architectures existent pour obtenir ce comportement, le HEMT avec une grille p-GaN étant celle largement adopté dans l'industrie. Cependant, cette architecture limite la polyvalence des dispositifs de puissance avec sa plage de tension de grille limitée et ses fuites de grille importantes à des tensions de grille élevées.

Pour résoudre ce problème, les HEMT à canal MOS, dit « MOSc-HEMT », développés au CEA-Leti constituent une solution intéressante pour les HEMTs Normally-OFF. En effet, la présence de l'empilement de grille MOS permet d'augmenter la plage de tension de grille et de réduire les fuites de grille, le tout en

maintenant un V_{TH} positif. Ce dernier est obtenu en gravant complètement la couche d'AlGaN au niveau de la grille, déplétant ainsi le 2DEG, et formant une cavité dans le GaN. La conduction entre la source et le drain est ensuite assurée par un canal MOS. Malgré l'avantage d'une grille MOS, les MOSc-HEMTs ne sont pas encore adoptés sur le marché de l'électronique de puissance. En effet, l'empilement de grille MOS et en particulier l'interface diélectrique/GaN présente les problèmes suivants :

- Le canal MOS a une mobilité réduite par rapport à celui du 2DEG, réduisant ainsi la mobilité du transistor, et donc augmentant le R_{ON}.
- La rugosité de la surface réduit en partie la mobilité des électrons.
- Les défauts d'interface affectent le V_{TH} et le R_{ON}, ces derniers peuvent être introduits par la gravure et le dépôt du diélectrique.
- Les défauts dans le diélectrique et proche de l'interface avec le GaN induisent une instabilité du V_{TH}.
- La surface du GaN est sujette à une oxydation rapide, tout en ayant une réactivité élevée envers les impuretés, affectant ainsi le V_{TH} et son instabilité.

Par conséquent, pour consolider définitivement le MOSc-HEMT, l'interface diélectrique/GaN doit être optimisée. Pour ce faire, l'impact des différentes étapes de fabrication doit être étudié. Dans ce projet de thèse mené en collaboration entre le CEA-Leti et le LTM, les principaux objectifs sont d'une part de développer des techniques de caractérisation physico-chimique en complément de véhicules de test électriques simplifiés, et d'autre part d'utiliser ces méthodologies pour étudier l'impact de différents procédés sur la grille MIS afin de l'optimiser. En particulier, différents diélectriques et leur recuit post-dépôt ont été étudiés.

Dans le premier chapitre de ce manuscrit, le contexte général de l'électronique de puissance et l'intérêt des composants basés sur du GaN seront présentés. Une comparaison entre le GaN et d'autres matériaux sera détaillée afin de démontrer son avantage en électronique de puissance. Ensuite, les propriétés des matériaux GaN et AlGaN seront présentées, amenant ensuite à la description de la formation du 2DEG dans l'hétérojonction AlGaN/GaN tout comme ses propriétés. La différence entre les composants Normally-ON et Normally-OFF sera brièvement présentée, avec ensuite une présentation des différentes architectures possibles pour obtenir un comportement Normally-OFF. Ensuite, le MOSc-HEMT avec ses avantages et ses processus de fabrication seront décrits et argumentés en mettant l'accent sur l'impact des procédés sur l'empilement diélectrique/GaN tout comme sur l'empreinte environnementale du MOSc-HEMT final. Enfin, les différentes voies d'optimisation vers un empilement MIS optimisé seront présentées et détaillées conjointement avec les objectifs de cette thèse.

Au chapitre 2, la méthodologie avec les différentes techniques de caractérisation sera présentée. Dans un premier temps, toutes les structures étudiées seront décrites et comparées afin d'argumenter sur les différentes informations qui peuvent être extraites de chacune d'elles et le choix du véhicule de test adapté suivant le paramètre que l'on cherche à étudier. Ensuite toutes les caractérisations électriques seront présentées avec leur méthodologie et hypothèses. Notamment, les paramètres électriques seront

présentées tels que la tension de bande plate (V_{FB}) et son hystérésis (ΔV_{FB}) utilisés pour étudier la fiabilité de l'empilement de grille, et la densité des états d'interface (D_{it}) utilisée pour analyser la qualité de l'interface. Dans un troisième et dernier temps, les caractérisations physico-chimiques utilisées dans ce travail de thèse seront décrites, en particulier l'analyse chimique des interfaces enterrées par spectrométrie photoélectronique à rayons X de haute énergie (HAXPES) et l'analyse de la rugosité de surface par microscopie à force atomique (AFM). La méthodologie présentée dans son ensemble mise sur la corrélation entre les paramètres électriques observés avec les caractérisations physico-chimiques afin de comprendre l'impact d'un processus et de l'optimiser.

Dans le chapitre 3, l'empilement de référence Al_2O_3/GaN gravé sera étudié. Dans une première section, l'impact de la gravure sur la rugosité latérale de surface et la mobilité électronique sera étudié avec l'utilisation du « Power Spectral Density » (PSD) sur les images AFM. En particulier, la variabilité et la différence entre la moyenne quadratique de la rugosité (RMS) et le PSD seront discutées. A l'aide du PSD, une comparaison de différentes gravures sera effectuée et comparée avec la mobilité électronique afin de déterminer si la rugosité de surface est un facteur limitant pour la mobilité électronique. Pour cela, une extraction de mobilité développée dans notre groupe sera utilisée pour extraire la contribution de chaque région de la grille. Dans une deuxième section, l'étude de l'impact du recuit post-dépôt (PDA) pour l'Al_2O_3 sera présentée. En combinant l'extraction de paramètres *C-V* et des caractérisations physico-chimiques telles que l'HAXPES, le ToF-SIMS et le FTIR, une température PDA optimale de 500°C sera mise en évidence. L'extraction de la densité des états d'interface, au moins sur la région de la bande interdite du GaN proche de la bande de conduction, indiquera également que la gravure et la préparation de surface sont déjà optimales en termes de faibles création de défauts lors de la fabrication du MOSc-HEMT. Cependant, au-dessus de cette température optimale de PDA, l'Al_2O_3 commence à se dégrader tant électriquement que physico-chimiquement. Par conséquent, ce chapitre met en évidence la faible stabilité thermique de l'Al_2O_3 déposé sur du GaN gravé.

Dans le chapitre 4, l'$Al_{0.5}Si_{0.5}O_x$ sera étudié comme une alternative à l'Al_2O_3 afin d'augmenter la stabilité thermique et de réduire la quantité de pièges dans le diélectrique déposé. La meilleure stabilité thermique de l'AlSiO et son hystérésis plus faible seront mises en évidence ainsi que ses limites en termes de stabilité morphologique et d'interface avec le GaN. En effet, par corrélation conjointe de TEM, d'HAXPES et de ToF-SIMS, la limite supérieure de recuit de l'$Al_{0.5}Si_{0.5}O_x$ sera discutée. Pour augmenter la stabilité thermique de l'AlSiO, l'introduction d'une couche de SiO_2 entre l'AlSiO et le GaN sera présentée. Tandis que la stabilité thermique est augmentée, les paramètres électriques seront dégradés. Toutefois, pour optimiser l'empilement $Al_{0.5}Si_{0.5}O_x/SiO_2$, un PDA à 950°C doit être appliquée afin de réduire les impuretés carbonées présentes dans le SiO_2. Enfin, la présence d'impuretés sera étudiée afin de comprendre l'hystérésis anormale observée et mise en évidence par des mesures à haute température (150°C).

Enfin, dans le chapitre 5, l'AlON sera également étudié comme alternative à l'Al_2O_3 dans la même intention que l'AlSiO. Dans une première section, l'approche supercycle par « Plasma-Enhanced Atomic Layer Deposition » (PE-ALD) pour déposer de l'AlON sera décrite et argumentée, mettant en évidence les conditions optimales pour obtenir un AlON uniforme et avec une teneur en azote contrôlée. Avec l'AlON uniforme obtenu, l'impact de l'azote et du PDA sera étudié. En accord avec la littéra-

ture, l'augmentation du V_{FB} avec la concentration d'azote sera présentée tandis que l'augmentation de l'hystérésis sera expliquée par des analyses ToF-SIMS. L'impact bénéfique du PDA sera présenté, avec une comparaison avec l'Al_2O_3 mettant en évidence les meilleures propriétés électriques de l'AlON, notamment à hautes températures de mesure. À partir de ces résultats, une concentration d'azote et une température de PDA optimales seront détaillées pour l'empilement AlON/GaN gravé.

Remerciements

Ce projet de thèse a été riche d'expérience et d'échange au CEA-Leti et LTM. Il n'aurait pas été possible sans l'aide, l'appui et la contribution de plusieurs personnes.

Tout d'abord je remercie les membres du jury d'avoir accepté d'évaluer et relever les limites de ce travail de thèse. Notamment je remercie Daniel ALQUIER et Marie-Paul BESLAND d'avoir accepté la lourde tâche de rapporteurs. Merci pour vos commentaires et suggestions. Je remercie également Sylvain BOLLAERT et Aurore CONSTANT d'avoir fait l'honneur d'examiner cette thèse. J'adresse aussi mes remerciements à Ahmad BSIESY pour avoir présidé le jury.

Dans un deuxième temps, je tiens à remercier mon encadrement de thèse qui a été très formateur. Un grand merci à Bassem SALEM, mon directeur de thèse, qui a été toujours présent depuis le premier jour, tant à m'orienter sur le plan scientifique qu'à me motiver et me redonner confiance. Je remercie grandement Laura VAUCHE pour son encadrement et sa patience sans faille. Tu as toujours su me pousser au-delà de mes sentiers battus, tout en gardant une bienveillance envers moi en me rappelant qu'une thèse n'est pas une course mais un marathon ! Je remercie également Eugénie MARTINEZ et William VANDENDAELE pour leur encadrement et pour tout ce que j'ai pu apprendre tant en XPS qu'en caractérisation électrique. Un grand merci à vous !

Je remercie également l'équipe du LAPS pour leur accueil, leur bonne humeur et leurs conseils. Je remercie Véronique SOUSA pour son accueil et sa bienveillance au sein du laboratoire. Un grand merci à Blend MOHAMAD qui a toujours été disponible pour répondre à toutes mes questions concernant le GaN et les HEMTs. Merci à Cyril LE ROYER pour tous les retours sur nos productions scientifiques et pour m'avoir appris à bien illustrer et présenter mes résultats. Je remercie aussi Julien BUCKLEY, René ESCOFFIER, Jérôme BISCARRAT, Etienne NOWAK, Sophie ROLLET, Aurélien OLIVIER, Rémi RIAT, Stéphane BECU, Murielle FAYOLLE-LECOCQ, Florent GRECO et Charlotte GILLOT pour avoir contribué de loin ou de près à ces travaux et pour les différents échanges pendant ou hors pauses cafés.

J'adresse aussi mes remerciements aux membres du LTM pour leur accueil et contributions. En particulier, je remercie Bernard PELISSIER et Sébastien LABAU pour l'aide et les échanges concernant l'XPS. Merci aussi à Sarah BOUBENIAH et Mohammed ZEGHOUANE sans qui beaucoup de travaux n'auraient pas été possible.

Je remercie également les membres de la PFNC/DPFT et du LCRF pour leur contributions. Merci à Marc VEILLEROT, Denis MARIOLLE, Christophe LECOUVEY, Pierre FRANÇOIS, Nicolas GAUTHIER, Gauthier LEFÈVRE et Névine ROCHAT pour leur caractérisation mais aussi pour le temps pris pour me faire découvrir leur expertise. Merci aussi à Alexis KRAKOVINSKY pour sa disponibilité et son aide lors des mesures électriques. Merci aux graveurs, Simon RUEL et Patricia PIMENTA-BARROS, pour les différentes gravures réalisées dans cette thèse mais principalement pour les discussions autour de cette thématique. Je remercie aussi Messaoud BEDJAOUI, Stéphane CADOT et Helen GRAMPEIX pour le dépôt et recuit d'oxyde, mais également pour vos retours et conseils sur la grille MIS.

Je souhaite aussi remercier mes camarades de thèse du LAPS, LTM et PFNC/DPFT qui ont rendu ces années plus amusantes et agréables. Je pense à Florian, Vishwajeet, Clémentine, Ahmad, Mohammed,

Timothée, Thomas, Tarek, Roman, Manuel, Valentin et David.

Un grand grand merci à mes amis qui m'ont soutenu durant ces années, à distance ou autour d'un verre. Je pense à Quentin, Sam, Aloïs, Cyril, Benjamin, Élie, Eléa, Mathias et Elena.

Finalement, les mots me manquent pour décrire ma reconnaissance envers ma famille et belle-famille. Merci à mes parents, grand-parents et sœurs qui m'ont motivé à venir en France pour les études et dont le soutien a été sans faille. Merci aussi à mes beaux-parents, beaux-frères et belles-sœurs pour leur jovialité et leur appui depuis le début de cette thèse.

Merci à ma merveilleuse épouse, Léa, d'avoir accepté de courir ce marathon avec moi. Sans toi je n'aurais pas eu le courage de me lancer. Ton soutien a été de tous les jours, d'autant plus durant ces derniers mois de thèse. Merci pour ta patience, tes encouragements et ta joie qui ont ensoleillé ces années, même les jours les plus difficiles.

SDG

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Abbreviations

2DEG Two-Dimensional Electron Gas

V_{FB} Flat-Band Voltage

ΔV_{FB} Flat-Band Voltage hysteresis

V_{TH} Threshold Voltage

ΔV_{TH} Threshold Voltage hysteresis

Λ_{SR} Correlation length

AES Auger Electron Spectroscopy

AFM Atomic Force Microscopy

Al_i Aluminium Interstitial

ALD Atomic Layer Deposition

ALE Atomic Layer Etching

AR-HAXPES Angle-Resolved Hard X-ray Photoelectron Spectroscopy

BB Band Bending

BDEAS Bis(diethylamino)silane

BTS Bias-Temperature Stress

C-V Capacitance-Voltage

CBO Conduction Band-Offset

CMOS Complementary Metal Oxide Semiconductor

D_{it} Interface states density

DFT Density Functional Theory

DOS Density of States

EDX Energy-dispersive X-ray spectroscopy

FEOL Front-End Of Line

FIB Focused Ion-Beam

FOM Figure of Merit

FTIR Fourier Transformed Infrared Spectroscopy

FWHM Full Width at Half Maximum

GIXRD Grazing Incidence X-ray Diffraction

G_m/ω Normalized conductance

HAXPES Hard X-ray Photoelectron Spectroscopy

HEMT High Electron Mobility Transistor

HHCF Height-Height Correlation function

I-V Current-Voltage

ICP-RIE Inductively Coupled-Plasma Reactive Ion Etching

ID Information Depth

IGBT Insulated Gate Bipolar Transistor

IMFP Inelastic Mean Free-Path

LCA Life Cycle Analysis

MOCVD Metal-Organic Chemical Vapor Deposition

MOS/MIS Metal-Oxide-Semiconductor/Metal-Insulator-Semiconductor

MOSc-HEMT Metal-Oxide-Semiconductor-channel High Electron Mobility Transistor

MOSCAP MOS capacitor

MOSFET Metal-Oxide-Semiconductor Field Effect Transistor

MSM Measure-Stress-Measure

NIL Nitridated Inter-Layer

pAR-XPS Parallel Angle-Resolved X-ray Photoelectron Spectroscopy

PBTI Positive Bias Temperature Instability

PDA Post Deposition Annealing

PE-ALD Plasma-Enhanced Atomic Layer Deposition

PE-CVD Plasma-Enhanced Chemical Vapor Deposition

PMA Post Metallization Annealing

POR Process of Reference

PSD Power Spectral Density

PVD Physical Vapor Deposition

R_{ON} ON-Resistance

RMS Root Mean Square roughness

RPP Remote Plasma Pretreatment

RSF Relative Sensitivity Factor

RTP Rapid Thermal Processing

SE *In-Situ* Spectroscopic Ellipsometry

SRH Shockley–Read–Hall

TDMAS tris(dimethylamino)silane

TEM Transmission Electron Microscopy

TLM Transmission Line Method

TMA Trimethylaluminum

TMGa Trimethylgallium

ToF-SIMS Time-of-Flight Secondary Ion Mass Spectrometry

UID UnIntentionally Doped

V_N Nitrogen Vacancies

V_O Oxygen Vacancies

VBM Valence Band Maximum

VBO Valence Band-Offset

WBG Wide Bang Gap

XPS X-ray Photoelectron Spectroscopy

Work done in conjunction with others

The work presented in this thesis was carried out by the author, with the following exceptions:

Process

1. Substrates: All the GaN substrates were grown at CEA-Leti by Matthew Charles and Simona Torrengo. The dicing of the substrate were performed by the author.

2. Etching: All the dry etching steps were performed at CEA-Leti by Simon Ruel and Patricia Pimenta-Barros (Chapter 3 and 5).

3. Cleaning: At CEA-Leti, the wet cleaning using the Process Of Reference (POR) was performed by Thomas Philippe (Chapter 3 and 4). At the PTA, the wet cleaning using HCl was performed by Mohammed Zeghouane and Bassem Salem (Chapter 5) from LTM.

4. Deposition: At CEA-Leti, the dielectric deposition by Atomic Layer Deposition (ALD) was performed by Eric Nguyen Gia Can for Al_2O_3 (Chapter 3) and by Stéphane Cadot (Chapter 4) for $Al_{0.5}Si_{0.5}O_x$. At the PTA, the dielectric deposition of AlON by Plasma-Enhanced ALD (PE-ALD) was performed Mohammed Zeghouane (from LTM) and the author (Chapter 5).

5. RTP annealing: At CEA-Leti, the annealing was performed by Helen Grampeix (Chapter 3 and 4). At the PTA, the annealing was performed by the author (Chapter 3) and Mohammed Zeghouane (from LTM) (Chapter 5).

6. Metal-Oxide-Semiconductor Capacitor (MOSCAP) fabrication: At CEA-Leti, the MOS-2 MOSCAP were fabricated according the flow developed at CEA-Leti (Chapter 3). At the PTA, the MOS-1 MOSCAP were fabricated by the author (Chapter 3 and 4) and Mohammed Zeghouane (from LTM) (Chapter 5).

7. GaNG transistor in Chapter 3 were fabricated at CEA-Leti by the clean room staff.

Characterization

1. Electrical measurements from MOSCAP: *C-V* for MOS-1 MOSCAP were performed by the author (Chapter 3, 4 and 5), similarly for the G_m/ω measurement at different temperatures (Chapter 3). The interface states abacus (Chapter 2) was calculated by William Vandendaele and Marie-Anne Jaud from CEA-Leti. The *C-V* for MOS-2 MOSCAP were performed by Rémi Capron and William Vandendaele from CEA-Leti. The BTS and MSM measurement in Chapter 4 and Chapter 5 respectively were performed by the author.

2. Electrical measurement from transistor: The *C-V* and I_D-V_G from GaNG transistors were performed by Arnaud Anotta while the data treament was carried out by Cyrille Le Royer from CEA-Leti (Chapter 3). The mobility extraction methodology and data analysis code was defined by

Clémentine Piotrowicz from CEA-Leti (Chapter 2 and 3).

3. The ToF-SIMS analysis were performed at CEA-Leti by Marc Veillerot (Chapter 3 and 5), François Pierre and Nicolas Gauthier (Chapter 4).
4. All the XPS and HAXPES was performed by the author and the AES (Chapter 5) was carried out by Mohammed Zeghouane from LTM.
5. All AFM images in Chapter 3 were acquired at CEA-Leti by Christophe Lecouvey for in-line measurements (in the clean room), and by either Denis Mariolle or Thomas Jalabert for off-line measurements (out of the clean room).
6. All the TEM/EDX (Chapter 4 and 5) was performed by Gauthier Lefèvre from LTM, and the GIXRD was performed by the author.
7. The FTIR in Chapter 3 was carried out by Névine Rochat from CEA-Leti.

The evaluation of all the results was carried out by the author

General introduction

The increase in electrical consumption has been a exponential phenomena since the 1970's for all involved sectors. Moreover, in the wake of global warming, the movement towards massive electrification and the adoption of renewable energies sources have been challenging the demands in power management and distribution. Notably, more efficient electrical power conversion for different applications would be beneficial in order to limit energy losses. Such conversion consist in converting alternating current (AC) or direct current (DC) at different voltage levels, frequencies or current types. This task is ensured by power electronics, where the conversion is performed by power modules composed of passive components such as capacitors or inductances, and actives components such as transistors. Initially based on silicon devices, the latter are unable to support the new demands (e.g. output power, switching frequency, efficiency) due to their physical limitations. This prompted the industry and research institutes to develop new power devices based on wide band gap (WBG) materials such as silicon carbide (SiC) and gallium nitride (GaN). In fact, these materials present better physical properties than silicon such as a higher breakdown voltage, a higher electron mobility and a higher thermal properties. Therefore, WBG-based devices can convert higher amount of power or at a higher frequency with more efficiency due to the reduced conduction and switching losses.

Considering GaN, if applications in optoelectronic and Radio-Frequency are already possible or improved by the use of GaN, its use in power application is a promising outlook for that field. With its high band gap, high electron mobility and good thermal properties, the use of GaN allows to fabricate devices with higher switching frequency than Si-based. Power modules with GaN converters are hence more efficient and their size are reduced. This is particularly the case of AlGaN/GaN heterojunction in which a two-dimensional electron gas (2DEG) with high electron mobility is formed at the interface. With this structure, High Electron Mobility Transistors (HEMTs) are fabricated with the advantage of having a lower ON-state resistance (R_{ON}) and a higher switching frequency. Nonetheless, these transistors have a Normally-ON behavior, which means that they have a negative threshold voltage (V_{TH}<0). This is detrimental for power electronics due to safety issues and complex driver design. Therefore, Normally-OFF HEMTs (V_{TH}>0) are highly desirable. Different architectures exist to achieve this behavior, the p-GaN gate HEMT being the one widely adopted in the industry. However, this architecture limits the versatility of power devices with its limited voltage swing and large gate leakage at high gate voltages.

To solve this issue, the MOS-channel HEMT (MOSc-HEMT) developed at CEA-Leti is an interesting solution for Normally-OFF HEMTs, the latter being designed for a voltage application of 650V. In fact, the presence of the MOS gate stack allows to increase the voltage swing and reduce the gate leakage while maintaining a positive V_{TH}. The latter is obtained by fully recessing the AlGaN layer at the gate region, depleting the 2DEG. The conduction between the source and the drain is ensured by a MOS channel. Despite the advantage of a MOS gate, MOSc-HEMTs are not yet adopted by the power market. Indeed, the MOS gate stack and in particular the Dielectric/GaN interface has the following issues:

- The MOS channel has a reduced mobility compared to the 2DEG mobility, reducing the overall transistor mobility, and therefore increasing R_{ON}.
- The surface roughness partly reduces the electron mobility.
- Interface defects affect V_{TH} and R_{ON}, and can be introduced by the etching and the dielectric deposition.
- Defects in the dielectric induce V_{TH} instability.
- The GaN surface is prone to rapid oxidation and reactive towards impurities, affecting V_{TH} and its instability.

Consequently, to definitely consolidate the MOSc-HEMT, the Dielectric/GaN interface and stack need to be optimized. To do so, the impact of different fabrication steps needs to be understood. In this PhD project carried out in collaboration between CEA-Leti and LTM, the main objectives are first to develop physical-chemical characterization techniques as a complement of simple electric test vehicles, and secondly to use this methodology to study the impact of different processes on the MIS gate in order to optimize it. In particular the different dielectrics and the post-deposition annealing were investigated.

In the first chapter of this work, a general context of power electronics and the interest in GaN-based devices will be presented. A comparison between GaN and other materials will be provided in order to discuss its advantages in power electronics. Then, the GaN and AlGaN material properties will be provided, leading to the description of the 2DEG formation in the AlGaN/GaN heterojunction and its properties. The difference between Normally-ON and Normally-OFF devices will be shortly presented, with then a presentation of the different possible architectures to obtain a Normally-OFF. Then the MOSc-HEMT with its advantages and fabrication processes will be described and discussed with a focus on the impact of processes on the Dielectric/GaN stack and on the environmental footprint of the final MOSc-HEMT. Lastly, the different optimization paths towards an optimized MIS gate stack will be presented and argued together with this PhD project objectives.

In Chapter 2, the methodology with the different characterization techniques will be presented. In a first step, all the structures studied will be described and compared in order to argue the different information that can be extracted from each one of them, and which test vehicle is adapted to study a given parameter. Then all the electrical characterizations will be presented with their methodology and assumptions. In particular, the electrical parameters will be presented such as the Flat-Band Voltage (V_{FB}) and its hysteresis (ΔV_{FB}) to analyze the reliability of the gate stack, and the interface states density (D_{it}) to analyze the interface quality. In a third step and final step, the physical-chemical characterizations used in this PhD work will be described with an emphasis on buried interface chemical analysis with Hard X-ray Photoelectron Spectroscopy (HAXPES) and surface roughness analysis with Atomic Force Microscopy (AFM). The overall presented methodology emphasizes the correlation between the observed electrical parameters and physical-chemical characterizations in order to understand the impact of a process and optimize it.

In Chapter 3, the reference Al_2O_3/etched GaN gate stack will be studied. In the first section, the impact

of etching on lateral surface morphology and electron mobility will be investigated with the use of Power Spectral Density (PSD) on AFM images. In particular, the variability and the difference between the Root Mean Square roughness (RMS) and PSD will be discussed. Using the PSD, a comparison of different etchings will be performed and compared with the electron mobility in order to determine whether the surface roughness is a limiting factor for the electron mobility. For that, a mobility extraction developed in our group will be used to extract the contribution of each region in the gate cavity. In a second section, the study of the impact of Post-Deposition Anneal (PDA) on Al_2O_3 will be presented. By combining the extraction of *C-V* parameters and physical-chemical characterization such as HAXPES, ToF-SIMS, and FTIR, an optimal PDA temperature of 500°C will be highlighted. The extraction of interface states density will also indicate, at least on the upper band gap of GaN, that the etching and surface preparation processes employed in the MOSc-HEMT fabrication are already optimal in terms of low defect formation. However, over this optimal PDA temperature, the Al_2O_3 starts to degrade in terms of electrical and physical-chemical parameters. Therefore, this chapter highlights the low thermal stability of Al_2O_3 deposited on etched GaN.

In Chapter 4, the $Al_{0.5}Si_{0.5}O_x$ will be studied as an Al_2O_3 alternative in order to increase the thermal stability and reduce the amount of traps in the deposited dielectric. The superior thermal stability of AlSiO and lower hysteresis will be highlighted together with its limitation in terms of structural stability and interface with GaN. In fact, by joined correlation of TEM, HAXPES and ToF-SIMS, the upper limit for annealing the $Al_{0.5}Si_{0.5}O_x$ will be discussed. To increase the thermal stability of AlSiO, the introduction of an SiO_2 layer between AlSiO and GaN will be presented. While the thermal stability is increased, the electrical parameters will be degraded. To optimize the stack however, a high PDA temperature needs to be applied. Lastly, the presence of impurities will be investigated in order to understand the abnormal hysteresis observed at a high measuring temperature (150°C).

Finally, in Chapter 5, the AlON will also be studied as an alternative for Al_2O_3 with the same intention of AlSiO. In the first section, the Plasma-Enhanced Atomic Layer Deposition (PE-ALD) supercycle approach to deposit AlON will be described and discussed, highlighting the optimal conditions for uniform AlON and controlled nitrogen content. With the obtained uniform AlON, the impact of nitrogen and PDA will be studied. In agreement with the literature, the increasing V_{FB} with nitrogen concentration will be presented while the increased hysteresis will be explained by ToF-SIMS analyses. The beneficial impact of PDA will be presented, with a comparison with Al_2O_3 highlighting the better electrical properties of AlON, particularly at high measuring temperatures (150°C). From the results, an optimal nitrogen concentration and PDA temperature will be drawn for the AlON/etched GaN stack.

1

General context and state of the art

This chapter aims to present the context for MOSc-HEMT devices in power electronics and the different challenges that the MIS gate faces. First, the context and the market of power electronics will be briefly presented. Then the physical properties of GaN and AlGaN will be described as well as the AlGaN/GaN heterojunction used to fabricate High Electron Mobility Transistors. After that, the fabrication of MOSc-HEMTs at CEA-Leti will be presented alongside the impact of fabrication processes on the MIS gate. Finally, the different optimization paths for the MIS gate will be discussed, and the objectives of the thesis presented.

Contents

1.1 Context

Ever since the 1970s, the world's electrical consumption continues to rise reaching 22 848 TWh in 2019 as shown in **Figure 1.1** [1]. Such a rise can be explained by the increase in residential consumption in OECD countries (e.g. USA, Europe) and industrial consumption in non-OECD countries (e.g. China, India). Recently, in response to climate change, a push towards electrification of some sectors such as transportation is starting to drive the electrical consumption. 62% of CO_2 emissions can indeed be related to electricity and transport sectors [2]. Renewable energy sources have also increased in the energy mix in order to tackle the emission of greenhouse gases.

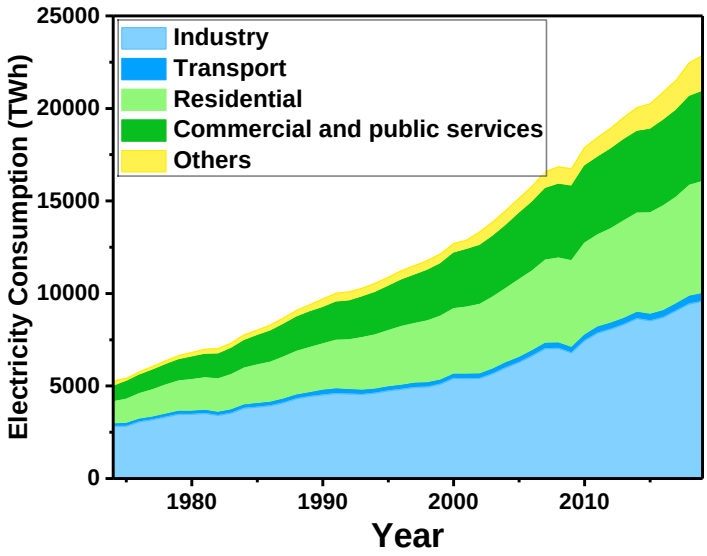


Figure 1.1: World's electricity consumption by sector between 1974 and 2019 [1].

It is therefore essential to efficiently transfer and convert the electrical energy. This task is carried out by Power Electronics which ensures different types of conversions (current type, voltage level, and/or frequency) from source to consumption. For instance, the electrical grid carries the energy through a high voltage-alternating current (AC) and is converted to a lower voltage-direct current (DC) used in consumption (e.g. phone charger). Inversely, in the case of photovoltaic cells, power electronic circuits convert the DC-generated current into AC in order to inject it into the traditional AC electrical grid. To perform these tasks, power electronics is composed of passive components such as capacitors and inductors allowing for the conversion of the voltage level and the current type, and of active components in the form of diodes and transistors transferring the power in a switching mode (cf. **Figure 1.2**).

The switching consists in alternating between ON and OFF states at a given frequency to convert a given power. Until the 2010s, active components were based on silicon components such as the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) used for low power at high frequencies (10-100 kHz) and the Insulated Gate Bipolar Transistor (IGBT) used for higher power and lower frequencies. However, due to the non-ideality of power components, power losses related to the conduction (ON-Resistance (R_{ON})) and switching mitigate their efficiency. Another issue is the size of power modules based on Si which are usually bulky. Although continuous efforts have been employed in optimizing Si-based components, Si physical properties hinder further optimization in terms of breakdown voltage, ON-state resistance, thermal conductivity (i.e. heat dissipation), and frequency.

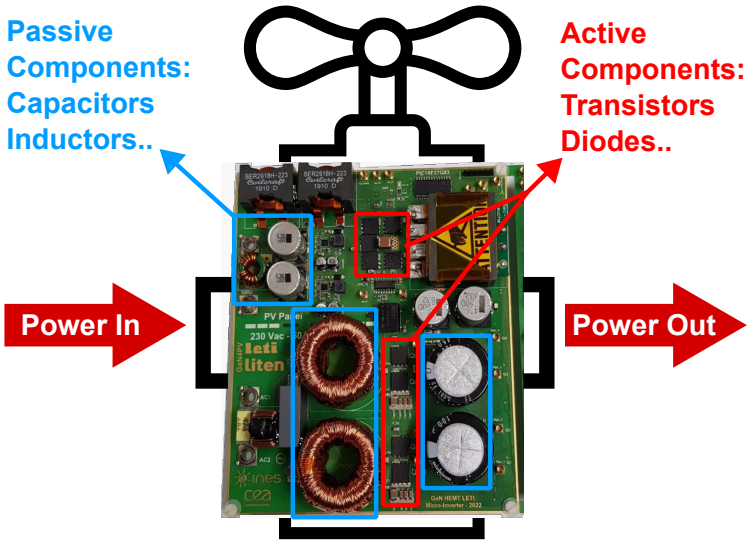


Figure 1.2: Micro-inverter for a PV application at CEA-Leti and Liten [3].

In that regard, Wide Bang Gap (WBG) materials such as Gallium Nitride (GaN) and Silicon Carbide (SiC) offer new possibilities in terms of power, frequency, compactness and efficiency. In fact, replacing Si with WBG components in different applications has the potential to considerably save energy due to their improved efficiency (e.g. up to 28.7 TWh/year in data centers in 2018) [4]. Such improvement can be traced back to the higher band gap, electron mobility, and critical electric field. Coming from optoelectronics and RF applications, GaN-based devices hold the promise of faster and more efficient power converters. Indeed, the role of GaN and SiC components are more complementary than conflicting as shown in **Figure 1.3**. SiC components focus more on higher power applications and higher frequencies than IGBTs, and GaN components focus on higher frequency operations. The applications for GaN-based devices are low-power PV, data centers and consumer applications such as fast chargers, all of that being in the low voltage range (<900 V). This range represents a market share of 68% [5] while the GaN power market is expected to grow from 126 million dollars in 2021 to 2 billion dollars in 2027, with a strong increase in the consumer and datacom sectors [6].

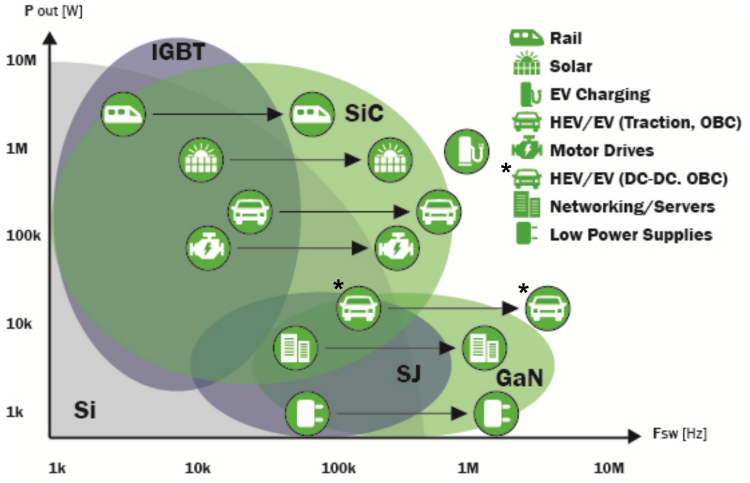


Figure 1.3: Classification of Si, SiC and GaN based on output power and operating frequency with their respective power applications, taken from [7].

In the next section, GaN and Aluminium Gallium Nitride alloy (AlGaN) materials properties will be presented. The addition of an AlGaN barrier allowing the fabrication of lateral transistors with high electron mobility will be presented and both its advantages and drawbacks for power devices will be discussed.

1.2 GaN and AlGaN properties

1.2.1 GaN: a Wide Band gap material for power applications

As stated previously, GaN is a Wide Band Gap semiconductor (3.4 eV) with interesting properties for power devices. The WBG group is composed of semiconductors with a band gap larger than 2 eV such as 4H-SiC (3.23 eV), β-Ga_2O_3 (4.8-4.9 eV) and diamond (5.47 eV) [8], [9]. For power electronics, the important properties represented in **Figure 1.4** are:

- High band gap, allowing to lower the generation of carriers at elevated temperatures (e.g. 150°C) and therefore reducing leakage current at such temperatures reached in some power applications.
- High critical electric field (proportional to the band gap, $E_{crit} \propto E_G^{2.3}$ [10]), which corresponds to the amount of electric field that the material can withstand without breaking.
- High electron saturation velocity, allowing to increase the switching frequency. It is related to the maximum velocity of electrons under high voltage.
- High electron mobility, allowing to reduce conduction losses with a lower R_{ON}.
- High thermal conductivity, in order to dissipate the self-heating effect during operation.
- High melting point, in order to withstand high temperature operations.

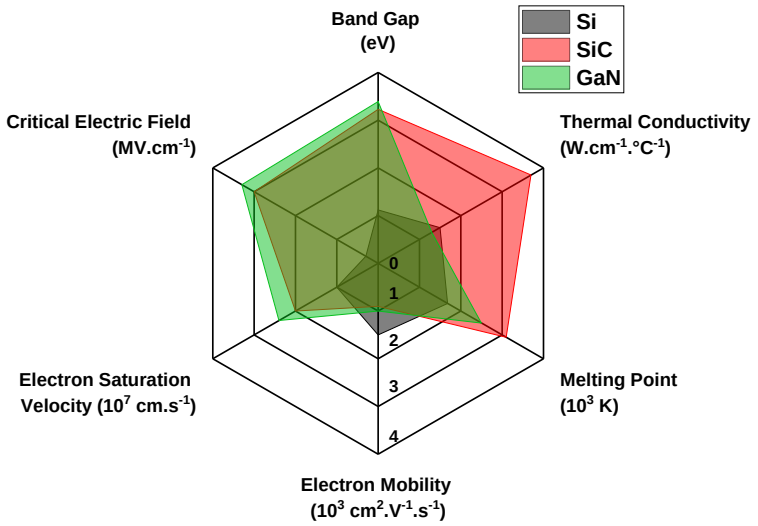


Figure 1.4: Diagram of different materials properties of Si, SiC and GaN at 300 K in the scope of power electronics. Based on [8], [9].

GaN is superior to Si for all considered properties except for thermal conductivity and electron mobility. It is indeed interesting in terms of band gap, critical electric field and electron saturation velocity, but it lacks the thermal properties attributed to SiC. A Figure of Merit (FOM) is usually used to describe the benefits of these material properties, the two main FOM being the Baliga's figure of merit (BFOM) for power applications and the Johnson's figure of merit (JFOM) for high-speed devices [10]. Specifically for the BFOM, it's based on a ratio between breakdown voltage and ON-resistance considering a vertical unilateral and abrupt p/n junction, which is not the case for lateral devices.

$$BFOM = \mu\varepsilon E_{crit}^3 \;\; ; \;\; JFOM = \frac{E_{crit} v_s}{2\pi} \tag{1.1}$$

Where μ is the electron mobility, ε the permittivity, v_s the electron saturation velocity. The values for Si, SiC and GaN are reported in the table below. Both BFOM and JFOM are favorable towards GaN due to its higher critical electric field and high electron saturation velocity. GaN-based devices can then be more compact and switch at high frequencies. Nonetheless, as stated before, the value obtained for BFOM is mainly true for GaN vertical devices. In the case of GaN lateral devices, Gaska et al. have proposed a new but more complex relationship between breakdown voltage and ON-resistance, which still highlights a good advantage for GaN in power devices [11].

Figure of Merit	Si	SiC	GaN
BFOM ($TW.m^{-2}$)	0.43	207.74	302.14
JFOM (THz.V)	0.48	9.55	12.61

Table 1.1: Figures of Merit for Si, SiC and GaN using values in [8], [9].

1.2.2 Crystal structure

GaN is a III-V material, meaning that is composed of atoms from the 3rd and the 5th column of the periodic table, i.e. gallium (Ga) and nitrogen (N). It has three possible crystal structures: a face-centered cubic (Rock Salt), a cubic (Zinc Blend), and a hexagonal (Wurtzite). The two cubic structures can be obtained in some specific conditions (pressure, temperature, substrate) but the hexagonal is the most stable structure and the most used in power electronics [12]. It is formed by two hexagonal closed-packed lattices, one by Ga atoms and the other by N atoms. Each III atom is surrounded by four V atoms and vice versa, as represented in **Figure 1.5**.

The hexagonal crystal structure is defined by the edge length of the hexagonal base (a), the height of the unit cell (c), and the distance of the Ga-N bond along the [0001] direction (u). A closer look along the c-axis reveals an asymmetric configuration, i.e. the [0001] and [000$\bar{1}$] directions are not identical. Therefore, when GaN is grown in the [0001] direction, the surface is terminated by Ga atoms (Ga-face), and when GaN is grown in the [000$\bar{1}$] direction, the surface is terminated by N atoms (N-face). The terms Ga-face or N-face refer specifically to the direction of growth and not the last layer of atoms on the top surface. For instance, if a Ga-face GaN with a Ga-terminated surface is etched and the surface becomes terminated by N atoms, the GaN is still Ga-face.

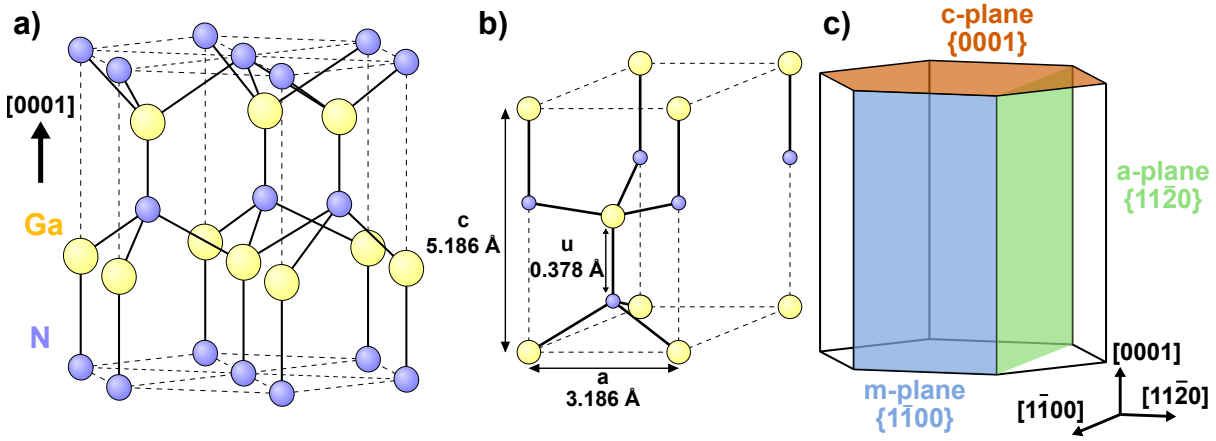


Figure 1.5: a) Ga-face GaN Wurtzite crystal structure; b) the cell unit with the different parameters, with values taken from [8], [13]; c) the different plans from the GaN crystal structure.

Three particular plans in the Wurtzite GaN structure are also to be considered (cf. **Figure 1.5**): the c-plane $\{0001\}$, the a-plane $\{11\bar{2}0\}$ and the m-plane $\{1\bar{1}00\}$. Their contribution will be further discussed in the next sections.

Similarly to GaN, AlN and the ternary alloy $Al_xGa_{1-x}N$ have a hexagonal Wurtzite structure with an asymmetrical configuration along the c-axis. a and c for $Al_xGa_{1-x}N$ follow the Vegard's law, whereas u follows quadratic relationship [14]:

$$a^{Al_xGa_{1-x}N}(x) = a^{AlN}x + a^{GaN}(1-x) \tag{1.2}$$

$$c^{Al_xGa_{1-x}N}(x) = c^{AlN}x + c^{GaN}(1-x) \tag{1.3}$$

$$u^{Al_xGa_{1-x}N}(x) = u^{AlN}x + c^{GaN}(1-x) + b_u x(1-x) \tag{1.4}$$

Where b_u, equal to -0.0032, is a bowing parameter. The lattice parameters for GaN and AlN are summarized in **Table 1.2**:

Material	a (Å)	c (Å)	u (Å)
GaN	3.186	5.186	0.378
AlN	3.112	4.982	0.3825

Table 1.2: Lattice parameters for GaN and AlN [8], [13].

1.2.3 Spontaneous polarization

The nature of the Ga-N bond is ionic, nitrogen being more electronegative than gallium (i.e. N^{3-} and Ga^{3+}). Coupled with the asymmetric configuration along the c-axis, a spontaneous polarization ($\overrightarrow{P}_{SP}^{GaN}$) appears in the material without any strain. In other words, a polarization exists without any electric field applied. This is explained by the non-overlap of positive and negative charge barycenters along the c-

axis, creating an ensemble of sheet charges compensated in the bulk, but creating at the c-plan surface negative charges on the oriented Ga-face and positive charges in the oriented N-face (cf. **Figure 1.6**). Therefore, the orientation of the polarization vector depends on the direction of growth. Materials having this property are qualified as pyroelectric since their polarization changes with temperature due to crystal dilatation. The asymmetry not being found perpendicularly to the c-axis, the m and a-planes (cf. **Figure 1.5.c)**) are non-polar.

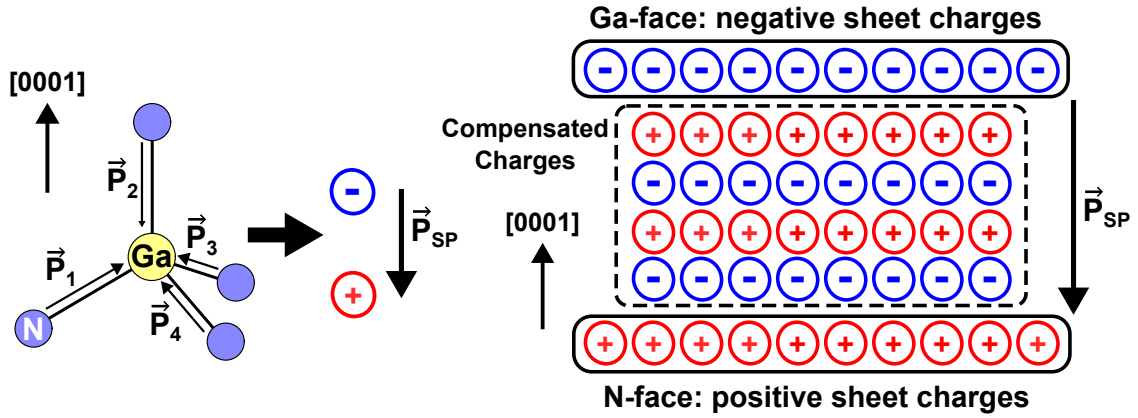


Figure 1.6: On the left, schematic representation of GaN tetrahedron with its different polarizations, leading to the appearance of the spontaneous polarization; On the right, the dipole sheet representation in Wurzite GaN, resulting in the spontaneous polarization and sheet charges on the surface.

The polarization in GaN is calculated to be equal to -0.034 C.m^{-2} [14], leading to a positive sheet charge equaled to $1.8-2.1\times10^{13}$ cm^{-2} [15]. This would lead to a surface potential in the order of -420 eV, higher than GaN's band gap (3.4 eV) [15]. However, experimental values of surface potential are reported to be around -0.3 to -1.5 eV, meaning that the sheet charges at the surfaces are compensated by both ionized donors and surface states (extrinsic such as gallium oxide and surface donors) [15]. Therefore, a large amount of surface states is expected at the GaN surface.

Having the Wurtzite structure, the same spontaneous polarization phenomena is observed for AlN and $Al_xGa_{1-x}N$. The direction of the polarization vector also depends on the growth direction. For AlN, the polarization is higher than GaN's polarization ($\overrightarrow{P}_{SP}^{AlN}=-0.090\,C.m^{-2}$ and $\overrightarrow{P}_{SP}^{GaN}=-0.034\,C.m^{-2}$). Since the relationship of u in $Al_xGa_{1-x}N$ is quadratic (cf. **Equation 1.4**), its spontaneous polarization as a function of Al molar fraction (x) can be also expressed with a quadratic equation [14]:

$$\overrightarrow{P}_{SP}^{Al_xGa_{1-x}N}(x)=\overrightarrow{P}_{SP}^{AlN}x+\overrightarrow{P}_{SP}^{GaN}(1-x)+bx(1-x) \tag{1.5}$$

Where $\overrightarrow{P}_{SP}^{AlN}=-0.090$ C.m^{-2}, $\overrightarrow{P}_{SP}^{GaN}=-0.034$ C.m^{-2} and $b=0.0021$ C.m^{-2}.

1.2.4 Piezoelectric polarization

GaN and AlGaN being pyroelectric, they are also piezoelectric. In fact, if GaN or AlGaN is under a given strain along the c-plane, the crystal deformation further moves the charge barycenters along the c-axis (cf. **Figure 1.6, left**), changing the polarization in the material. The added polarization is qualified as piezoelectric polarization ($\overrightarrow{P}_{PE}$). For an AlGaN/GaN heterojunction, strain is observed due to lattice

mismatch of a between AlGaN and GaN (cf. **Equation 1.2**), with a^{AlGaN} being smaller than a^{GaN}. This mismatch induces a tensile strain in AlGaN and a compressive strain in GaN, ultimately inducing a piezoelectric polarization (cf. **Figure 1.7, left**).

Considering that the AlGaN layer in the AlGaN/GaN heterojunction used in power devices is thinner than the GaN layer, the AlGaN layer is the only layer impacted by the strain while the GaN layer has no strain (i.e. pseudomorphic). In that configuration, by considering that the strain and the stress in the c-plane are isotropic (same along the x and y direction), the piezoelectric polarization of an $Al_xGa_{1-x}N$ as a function of the Al molar fraction (x) can be expressed using the strain with the piezoelectric constant (d_{31}) and the elastic constants (C_{11}, C_{12}, C_{13}, and C_{33}) [10]:

$$\overrightarrow{P}_{PE}^{Al_xGa_{1-x}N}(x) = 2d_{31}\left(\frac{a^{Al_xGa_{1-x}N}(x) - a^{GaN}}{a^{GaN}}\right)\left(C_{11}(x) + C_{12}(x) - 2\frac{C_{13}(x)^2}{C_{33}(x)}\right) \tag{1.6}$$

The direction of the polarization vector in the AlGaN layer is identical to the existing spontaneous polarization in the case of Ga-face. Therefore, the two polarizations are added as represented in **Figure 1.7, right**.

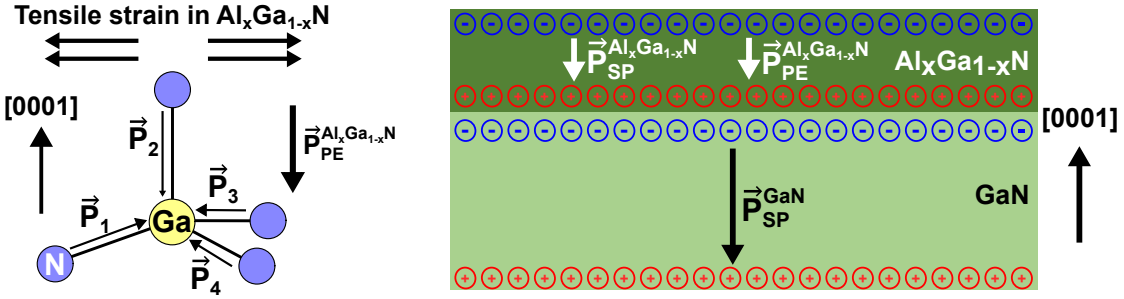


Figure 1.7: On the left, schematic representation of the effect of tensile strain in $Al_xGa_{1-x}N$ leading to the appearance of the piezoelectric polarization; On the right, the different polarization in the AlGaN/GaN heterojunction considering that the layer is thick enough to be pseudomorphic (without strain).

1.2.5 AlGaN/GaN heterojunction: 2D-Electron Gas

The sum of polarization in $Al_xGa_{1-x}N$ (spontaneous and piezoelectric) is not equal to the spontaneous polarization in GaN, leading to the presence of an interfacial charge. The polarization charge can be calculated using the gradient of the polarization ($\sigma_p = \nabla \overrightarrow{P}$). Consequently, the polarization charges at the $Al_xGa_{1-x}N$/GaN interface as function of the Al molar fraction (x) can be described as:

$$\sigma_{int}^{Al_xGa_{1-x}N/GaN}(x) = \sigma_{SP}^{GaN} - \left(\sigma_{SP}^{Al_xGa_{1-x}N}(x) + \sigma_{PE}^{Al_xGa_{1-x}N}(x)\right) \tag{1.7}$$

For a molar fraction above 0.2, a positive interface charge up to 1×10^{13} cm^{-2} is obtained. However increasing x over 0.3 induces a partial relaxation of the $Al_xGa_{1-x}N$ layer, reducing $\overrightarrow{P}_{PE}^{Al_xGa_{1-x}N}$ and ultimately limiting the increase of interfacial charges [16]. The positive interface charges are then compensated by the creation of a Two-Dimensional Electron Gas (2DEG) at the AlGaN/GaN interface with similar electron density (1×10^{13} cm^{-2}) without any doping or electric field applied [16]. This 2DEG still appears when the GaN layer is unintentionally n-doped (UID), which is the case for GaN grown

for the heterojunction used in power devices (cf. further discussion in **Section 1.4.1.2**). The 2DEG is situated on the GaN side due to the lower conduction band in GaN (cf. **Figure 1.8**). Other than the Al molar fraction, the 2DEG density is also modulated by the AlGaN thickness, with saturation around 20-30 nm but decreasing electron density with lower AlGaN thickness [17].

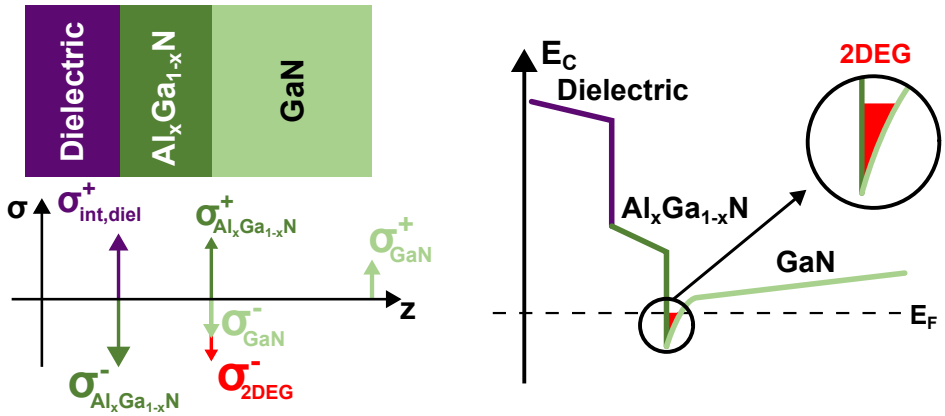


Figure 1.8: On the left, schematic representation of the different charges in the Dielectric/$Al_xGa_{1-x}N$/GaN stack leading to the appearance of the 2DEG; On the right, the band diagram of the dielectric/$Al_xGa_{1-x}N$/GaN stack with the 2DEG.

The origin of electrons in the 2DEG has been a debated topic as presented by Bakeroot et al. [18]. Ibbetson et al. [17] proposed that the electron origin in the case of Metal/AlGaN interface is mainly surface donor states on the AlGaN surface with an energy level of 1.65 eV from the conduction band. Other groups highlighted defects at similar energy levels as an origin [19], [20]. In the case of the Dielectric/AlGaN interface, Bakeroot et al. [18] proposed instead that the donor states are in the dielectric but close to the interface.

Since the 2DEG is present without doping and it is confined at the AlGaN/GaN interface, the electron gas can reach mobility at room temperature in the order of 1000 to 2000 $cm^2.V^{-1}.s^{-1}$ [21], [22]. This high mobility is also possible due to a sharp AlGaN/GaN interface. Adding a thin AlN interfacial layer increases the mobility by further confining the 2DEG on the GaN side [23].

1.3 AlGaN/GaN based power transistors

From the 2DEG obtained with the AlGaN/GaN heterojunction, lateral High Electron Mobility Transistor (HEMT) can be fabricated in order to reduce the conduction losses linked to R_{ON} and the switching losses linked to the switching frequency. The two kinds of HEMT classified according to the voltage applied to turn on the transistor or the Threshold Voltage (V_{TH}) will be presented in the next sections. At CEA-Leti, V_{TH} is defined as the gate voltage where a drain current of 10^{-5} A/mm is obtained.

1.3.1 Normally-ON (D-mode)

The first kind is the Normally-ON or D-mode (Depletion mode) transistor. It's a HEMT with a Schottky gate contact on the AlGaN layer, the source and the drain being fabricated on the GaN layer in order to contact the 2DEG (cf. **Figure 1.9**).

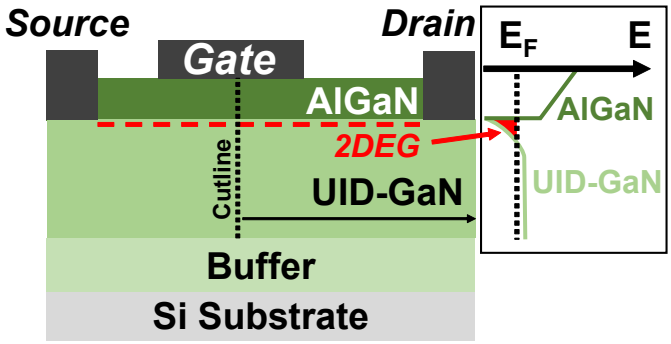


Figure 1.9: Schematic representation of Normally-ON GaN HEMT with its associated energy band diagram.

Since the latter exists without any large doping and electric field, if a voltage is applied at the drain without any bias at the gate, a current can flow between the source and the drain as in the "ON" state (i.e. Normally-ON). To reach the "OFF" state, a negative voltage needs to be applied at the gate in order to deplete the 2DEG under the gate (i.e. Depletion Mode). Thus, their threshold voltage is negative. If Normally-ON devices can be interesting for RF applications, devices with a positive threshold voltage, i.e. Normally-OFF or E-mode (Enhance-mode), are more desirable for power devices. In fact, having a positive V_{TH} allows safer operations and less complex driver design [10].

1.3.2 Normally-OFF (E-mode)

To obtain a Normally-OFF AlGaN/GaN HEMT, different architectures proposed in the literature and commercialized will be presented, with at last the Metal-Oxide-Semiconductor-channel High Electron Mobility Transistor (MOSc-HEMT) presented.

1.3.2.1 Cascode configuration

A first solution to obtain a Normally-OFF AlGaN/GaN HEMT is the cascode configuration, in which a Normally-OFF low voltage Si n-MOSFET is connected in series at the drain with a Normally-ON AlGaN/GaN HEMT (cf. **Figure 1.10**) [24]. Thus, the Si n-MOSFET having a positive V_{TH} controls the current going through the AlGaN/GaN HEMT. However, the package size and cost are increased while the series connection induces large parasitic inductance limiting the switching frequency. The presence of the Si n-MOSFET also restricts operations at high temperatures [10]. For its advantages, the Cascode configuration is commercialized by Transform and Nexperia with a voltage range of 650 V.

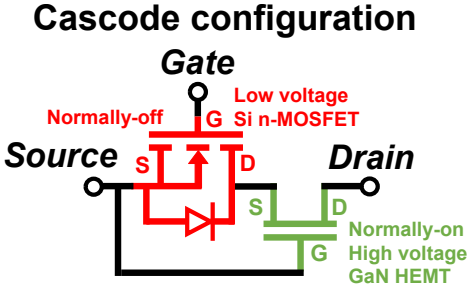


Figure 1.10: Schematic representation of the Cascode configuration with a AlGaN/GaN HEMT.

1.3.2.2 p-GaN gate

The other solution largely adopted by the industry is the p-GaN gate, commercialized by Infineon, EPC and Panasonic. As its name suggests, the positive V_{TH} is obtained by a p-doped GaN layer situated between the gate metal and the AlGaN barrier, as represented in **Figure 1.11, left**. The p-doping lifts the conduction band depleting the 2DEG while maintaining its presence and high mobility during the ON state. The doping is in the order of $10^{18} - 10^{19}$ cm^{-3} using Mg as a "shallow" acceptor at 0.13-0.2 eV from GaN's valence band.

As described in **Section 1.2.5**, the Al molar fraction and the thickness of the AlGaN layer can be used to optimize the effect of the p-GaN layer [25]. In fact, increasing the Al molar fraction or the barrier thickness can lead to a Normally-OFF behavior and cancel out the effect of the p-GaN layer. On that same logic, the barrier at the gate region can be etched to obtain a thinner layer, which increases V_{TH} while maintaining a high 2DEG density between the gate and the drain [26].

Nonetheless, this architecture has a limitation which is the gate leakage current when the gate voltage is higher than V_{TH}. Indeed, the p-GaN/AlGaN/GaN stack behaves as a p-i-n junction. Although the leakage can be limited by using some specific gate metals such as TiN in order to have a high Schottky barrier [27], the voltage swing or the maximum voltage range that can be applied at the gate is still limited.

1.3.2.3 Fluorine gate

Fluorine-based gate is another topology used to obtain a Normally-OFF AlGaN/GaN HEMT. It is based on implanted negative Fluorine ions (F^-) at the AlGaN gate region depleting the 2DEG without losing its high mobility (cf. **Figure 1.11, right**)[28]–[30]. It can be combined with a Metal-Oxide-Semiconductor/Metal-Insulator-Semiconductor (MOS/MIS) stack to reduce the gate leakage current [31]. A similar effect can be obtained with direct *in-situ* fluorine doping in the oxide (i.e. dielectric) layer of the MOS stack [32]–[34]. If the Normally-OFF behavior is achieved, concerns rise on the stability of the V_{TH} with trapping at the AlGaN and/or oxide layer [31], [35].

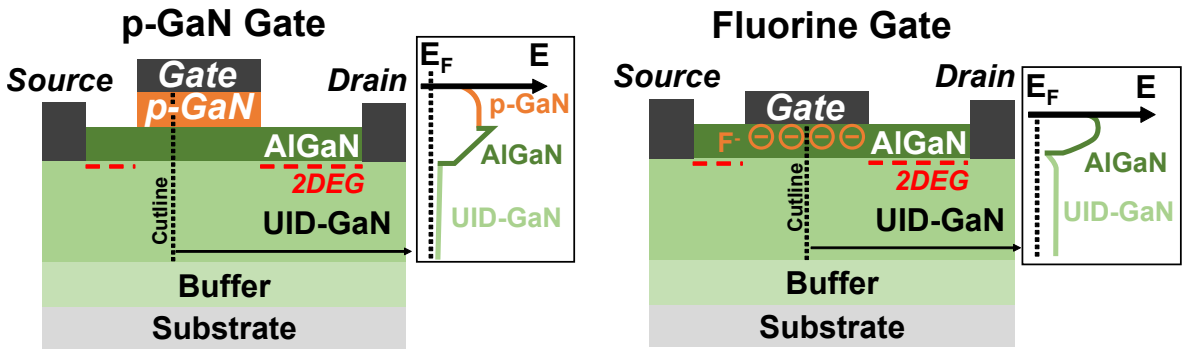


Figure 1.11: Schematic representation on the left of a p-GaN gate HEMT and on the right of a Fluorine gate HEMT with their associated energy band diagrams.

1.3.2.4 Partially-recessed MIS gate

As described in **Section 1.2.5**, reducing the AlGaN thickness reduces the 2DEG density to the point where a Normally-OFF behavior can be obtained. This thickness is generally under 5 nm depending on the Al molar fraction [17], [36]. However, in order to keep a high 2DEG density outside of the gate region, only the AlGaN gate region is etched [36], [37]. If a Schottky gate contact can be used, a MOS gate stack is preferred as it reduces the gate leakage and increases the voltage swing [38]–[40]. This approach is described as Partially-recessed MIS gate (cf. **Figure 1.12, left**). Similarly to the p-GaN gate and the fluorine gate, the partial AlGaN recess allows to keep a high 2DEG mobility during the ON-state. However, the variation in the etching process can induce V_{TH} variation from one device to another, limiting its industrialization [41].

1.3.2.5 MOS-channel HEMT: fully-recessed MIS gate

The Metal-Oxide-Semiconductor-channel High Electron Mobility Transistor (MOSc-HEMT) is another approach to obtain a Normally-OFF AlGaN/GaN HEMT [42]–[44]. It's the architecture adopted at CEA-Leti, designed to withstand 650 V and deliver 30 A [45]. Different than the partially-recessed MIS gate, the MOSc-HEMT has a fully recessed AlGaN layer in order to deplete the 2DEG under the gate, stabilizing the V_{TH} variation from one device to another. After recess, a dielectric layer is deposited to isolate the gate, while the 2DEG at the source and drain side are intact, as represented in **Figure 1.12, right**. At the ON state, the conduction under the gate is ensured by a MOS channel formed between the source and drain sides. However, the MOS channel mobility is significantly lower than the 2DEG (i.e. 10 times), increasing the overall R_{ON}. The etching also reveals non-polar gate sidewalls, such as m-planes or a-planes (cf. **Figure 1.5, c)**) depending on the device orientation in the case of perfectly perpendicular sidewalls. Actual sidewalls are not vertical and are based on semi-polar planes, which still will have different contributions in V_{TH} and R_{ON} [46]. Compared to a p-GaN gate, the MOSc-HEMT allows smaller R_{ON} variation with temperature and better switching characteristics [45].

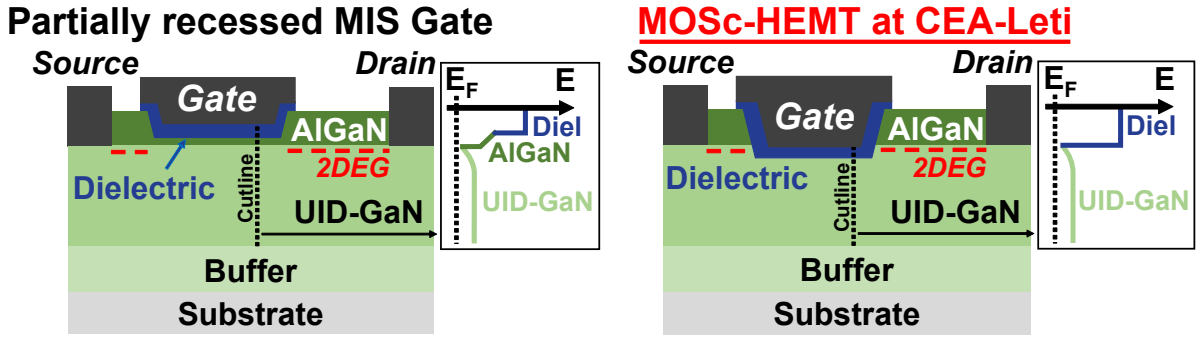


Figure 1.12: Schematic representation on the left of a Partially-recessed MIS gate and on the right of a Fully-recessed MIS gate HEMT (MOSc-HEMT) with their associated energy band diagrams.

Still, one critical aspect to ensure its use is the optimization of the Dielectric/GaN interface in order to have stable V_{TH}/R_{ON} [10]. In fact, this interface presents many challenges in terms of defects and surface preparation that need to be addressed. To understand these challenges, the fabrication process, its impact on the Dielectric/GaN stack, and the different optimizations will be presented in the following sections.

1.4 MOSc-HEMT fabrication and challenges for the MIS gate

The Front-End Of Line (FEOL) fabrication of the MOSc-HEMT is comprised of 48-60 different steps, from epitaxy to the fabrication of the first level of metallization (including field plates). If GaN-based power converters are more efficient and allow to reduce the impact of the use phase, the environmental impacts of the sourcing and each fabrication step based on Life Cycle Analysis (LCA) methodology are also important to consider and will be shortly presented based on internal reports.

1.4.1 Fabrication processes

1.4.1.1 Gallium origin and sourcing

GaN is a synthetic material grown from gallium and nitrogen. Nitrogen is not a critical element, used in different fabrication steps under different gas forms and solutions. Gallium instead is an element found in different ores, mainly in bauxite[1], zinc ores and coals [47]. Bauxite is the ore having the most Ga with only a Ga average content of 50 ppm in mass (or 0.0005%), which means that Ga is a by-product of bauxite and zinc ores processing [47]. China is the main producer of Ga with 98% of the worldwide production of low purity Ga (99.99%) [48]. Higher levels of purity (>99.9999%) are needed for the semiconductor industry and are obtained by refining techniques [49]. With increasing demand in gallium-related applications (RF, optoelectronics and now power) but critical outsourcing, gallium has been considered by the EU as a Critical Raw Material[2] since 2020 [50]. This qualification has been recently exemplified by restricted exports of gallium in the context of the chip war between China and the US [51].

1.4.1.2 Epitaxy

As described in the previous section, GaN is not found in bulk substrates and needs to be grown from Ga and N by epitaxy on substrates. Epitaxy corresponds to the growth of a thin crystalline single layer on a substrate in which the crystal order of the grown layer is dictated by the substrate. Epitaxy is usually performed by Metal-Organic Chemical Vapor Deposition (MOCVD) using metal-organic molecules as precursors. For GaN, the precursors are usually Trimethylgallium (TMGa) for Ga and ammonia for N. The layer is grown by the gaseous precursors reacting near the surface, being absorbed and diffusing on the substrate surface, the by-products being rejected afterward (cf. **Figure 1.13**). The temperature of deposition is around 1000°C.

The choice of substrate is also essential since the lattice and thermal expansion coefficient mismatch between the grown layer and substrate induces strain, the latter creating dislocation and point defects in the grown layer [53]. These defects can reduce or affect the device breakdown voltage [54]. Four different substrates can be used: Si, Sapphire (Al_2O_3), SiC and GaN. The **Table 1.3** summarizes the different properties of the cited substrates. GaN substrate is the best option in terms of mismatch due

[1] Mainly composed of aluminium oxide, it's the main ore used to extract aluminium

[2] "Those raw materials that are most important economically and have a high supply risk are called critical raw materials." p.1 in [50]

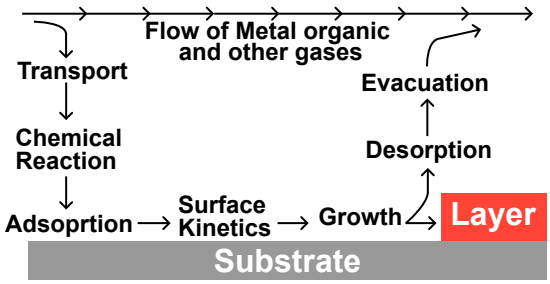


Figure 1.13: Principle of MOCVD based on a scheme found in [52].

to reduced defects and no mismatch, but the cost is very high making it commercially unsuitable. SiC is the best foreign substrate due to lower mismatch and defects, but similarly to GaN substrates, the cost is high. Although sapphire is more suitable in terms of mismatch, Si is more advantageous for its cost considering that 200/300 mm wafer can be used, but also due to the possibility of integration in the Complementary Metal Oxide Semiconductor (CMOS) process used in the industry. This is why most of the GaN-based power devices use a Si substrate. At CEA-Leti, the used Si diameter is 200 mm.

	Si	Sapphire	SiC	GaN
Lattice mismatch (%)	-17	16	0.31	0
Thermal expansion coefficient mismatch (% compared to GaN)	53.6	-33.9	21.4	0
Thermal conductivity ($W.cm^{-1}.K^{-1}$)	1.6	0.25	4.9	2.3
Dislocation density (cm^{-2})	10^8	10^8	10^8	$10^4 - 10^8$
Wafer size (mm)	200-300	50-100	50-150	50-100
Cost	Cheap	Cheap	Expensive	Very expensive

Table 1.3: Properties for different substrates used for GaN epitaxy, from [30].

Still, using Si presents a challenge for GaN epitaxy with its high mismatch with GaN. To make it possible and reduce the amount of strain, defects, and bowing of the wafer during cooling after MOCVD, buffer layers are grown before the GaN layer. They consist of a 200-300 nm AlN nucleation layer (NL) and 1-2 µm transitions layers [53]. The AlN nucleation layer is used to prevent the strong reaction between Ga and Si happening at high temperatures. The NL also reduces the mismatch between the Si substrate and the upper layers by providing a compressive strain. After the NL, the transition layers are grown layers to manage the strain during cooling after MOCVD. These transition layers can be: graded $Al_xGa_{1-X}N$ layers with x going from 1 to 0 from the NL to the GaN layer, AlN/GaN super-lattice, AlN interlayers with GaN, and two to three $Al_xGa_{1-X}N$ layers with x increasing gradually from 1 to 0 [30]. To deposit the AlN and $Al_xGa_{1-X}N$ layers, the precursor for Al is Trimethylaluminum (TMA).

Then a GaN layer is grown with a higher thickness in order to withstand a high electric field and allow for high-voltage vertical breakdown. It is composed of a carbon-doped layer (GaN:C) allowing to improve the breakdown voltage and reduce lateral/vertical leakages, and of an unintentionally n-doped (UID) GaN layer that is the channel layer. The latter is doped due to the intentional presence of defects and/or impurities such as Si rendering a n-type doping of $\leq 10^{15} cm^{-3}$ [30]. The 2DEG is formed by growing around 25 nm of $Al_xGa_{1-X}N$ with an Al molar fraction of 25%. Lastly, a capping layer of SiN is grown to protect the wafer surface. The overall epitaxy structure is represented in **Figure 1.14**:

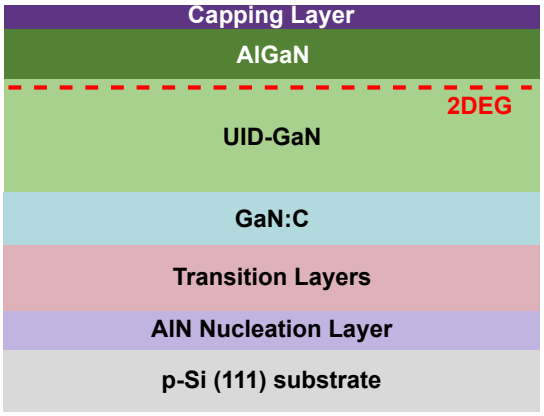


Figure 1.14: Schematic representation of III-V epitaxial layers on Si used to fabricate MOSc-HEMT.

In terms of environmental footprint, the impact of MOCVD is mainly the process in itself which is demanding in electrical power and can last several hours at high temperatures (1000°C) [55], [56]. Potential ways to reduce this impact are to reduce the processing time, increase the energy efficiency of the MOCVD equipment, and favor energy mix with low carbon emission [56].

1.4.1.3 Etching

After epitaxy, the AlGaN gate region is recessed to obtain the Normally-OFF behavior. For that, Inductively Coupled-Plasma Reactive Ion Etching (ICP-RIE) is the process frequently used to obtain an anisotropic and selective dry etching on WBG materials [57]. A plasma is generated by the Inductively Coupled Plasma reactor and directed towards the substrate with a bias. The use of ICP reactors is notably interesting due to the tunable plasma density. The etching has both a physical and chemical component that can be tuned accordingly to obtain the desired profile. For GaN etching, the plasma is based on a mixture of BCl_3 and Cl_2. With this plasma, the GaN etching cannot be only a chemical etching due to the high ebullition temperature of reaction by-products. The BCl_3 /Cl_2 radicals react with GaN (AlGaN) forming gallium (aluminium) chlorides byproducts ($GaCl_3$ and $AlCl_3$). Moreover, using BCl_3 is effective in reducing the defective native gallium oxide (GaO_x) [58]. Therefore, ICP-RIE is a fast and effective way to etch the AlGaN/GaN heterojunction. Nonetheless, the plasma etching induces damage on the surface that needs to be addressed as follows:

- Surface roughness [59].
- Higher presence of native oxide after etching [60].
- Lattice defects from ion bombardment. They can be either shallow or deep defects producing doping compensation or trapping. The most notable defect is Nitrogen Vacancies (V_N) which acts as a shallow donor [61] and reduces V_{TH} [62], [63]. The damage can be measured as deep as 100 nm from the surface, although the projected range of the ions is only <1 nm [64].
- Deposition of polymeric film composed of CH_x species in the plasma chemistry or after reacting with the photoresist mask [64].
- Nonstoichiometric surface due to selective etching/removal of species, such as in preferential sput-

tering of lighter elements leading to an enrichment of heavier elements [64].

Therefore, to remove the ICP-RIE damaged layer on the surface, Atomic Layer Etching (ALE) is performed. The ALE is an isotropic etching process consisting of two sequential steps [65]:

- (Reaction A) Surface modification.
- (Reaction B) Removal of the modified surface layer.

There are different ways to perform the reaction A, but the one used at CEA-Leti is the chlorination of the GaN surface with a mixture of BCl_3 /Cl_2 plasma. The difference with ICP-RIE is that no bias is applied at the surface to etch it, the plasma only reacts with the surface. Reaction B is then performed by sputtering the modified surface layer at low bias [66]. The etching per cycle is around 5 Å, with a couple of cycles used to etch a few nanometers. The ALE process is summarized in **Figure 1.15** :

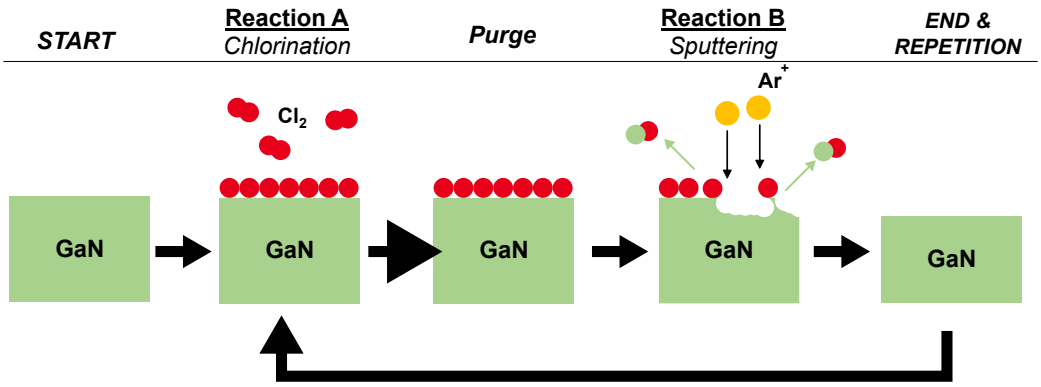
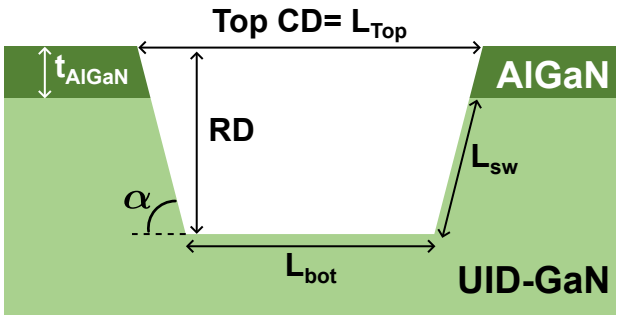


Figure 1.15: Principle of ALE applied to the GaN surface.

After etching, the gate has a trench shape, with a bottom and sidewalls regions as represented in **Figure 1.16**. The etching is not fully vertical, with a sidewall angle appearing and reducing the bottom gate length. To measure the angle and therefore the gate bottom length, a CD-SEM equipment is used to measure the recess depth (RD) and the sidewall angle (α) [45]. From the top gate length (L_{Top}), the sidewall angle, and the AlGaN thickness (t_{AlGaN}), the gate bottom (L_{bot}) and sidewall (L_{sw}) length in GaN can be expressed as:



$$L_{bot} = L_{Top} - 2\frac{RD}{\tan(\alpha)} \tag{1.8}$$

$$L_{sw} = \frac{RD - t_{AlGaN}}{\sin(\alpha)} \tag{1.9}$$

Figure 1.16: Schematic representation of the gate cavity after recess with the different associated parameters.

The overall ICP-RIE and ALE etching processes have a high impact on climate change when using fluorinated gases in the process (e.g. SF_6 for etching of SiN capping layer, NF_3 for cleaning the chamber).

This impact can be reduced with the addition of an abatement system which eliminates the fluorinated gases by combustion and water scrubbing [55].

1.4.1.4 Surface treatment

After etching, some remaining by-products still remain on the surface such as the polymeric film coming from the photoresist mask. To remove them, a stripping sequence consisting of an exposure to a dry O_2 and a EKC265™ wet stripper is used. The O_2 plasma oxidizes the remaining photoresist (mostly carbon and hydrogen) forming volatile CO, CO_2 and H_2O. It also allows to oxidize any GaN etching by-products. The EKC265™ wet stripper solution removes oxides created by the plasma [67].

The stripping still leaves some residual carbon, oxygen and other impurities. Therefore, before dielectric deposition, the surface is cleaned with a wet solution. This can be a challenging task since the Wurtzite GaN surface with its dangling bonds is very reactive towards the adsorption of oxygen [15], but also to a wide range of impurities, resulting in a higher impurity concentration on a GaN surface than on a Si surface [68]. Therefore choosing the appropriate wet solution is important since the MOSc-HEMT V_{TH} is dependent on it, primarily due to the reduction of a defective GaO_x [60]. The Process of Reference (POR) sequence at CEA-Leti has an ending sequence containing HF known to reduce GaO_x and passivate the surface [69], [70].

The large number of stripping and wet steps used in the overall FEOL fabrication flow can lead to environmental impacts due to the production of chemicals and emissions of volatile organics into the air [55].

1.4.1.5 Dielectric deposition by Atomic Layer Deposition

With the surface prepared by stripping and wet cleaning sequences, the dielectric is deposited by Atomic Layer Deposition (ALD). It is a cyclic layer-by-layer deposition technique used to deposit thin and conformal layers, in which a precursor and a reactant react to form one layer of the desired material at each ALD cycle (cf. Similarly to ALE, one ALD cycle is composed of sequential steps [71], [72]) as illustrated in **Figure 1.17**:

1. (Reaction A) The precursor is injected in the chamber to react with active sites on the substrate (or the monolayer), until a monolayer of precursor is adsorbed.
2. (Reaction B) The reactant is injected into the chamber and reacts with the precursor monolayer to form a monolayer of the desired material.

Between each reaction, a purge of the remaining precursor or reactant is performed with an inert gas (e.g. Ar) in order to avoid any reaction between the unabsorbed precursor and reactant, and to remove the reaction by-products.

For oxides and nitrides, the precursor in ALD is typically a metalorganic compound carrying the metal element while the reactant is the oxidizing or nitrogenous element. A temperature around 300°C is used to favor the chemisorption of both the precursor and the reactant. Moreover, a plasma can be used as a

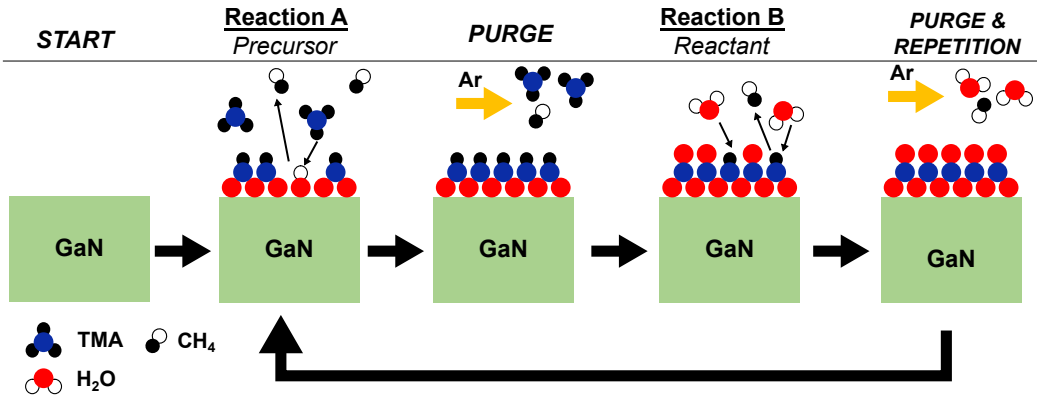


Figure 1.17: Principle of ALD applied to Al_2O_3 deposition on a GaN surface.

reactant to increase its chemisorption and reduce the deposition temperature, this technique referred as Plasma-Enhanced Atomic Layer Deposition (PE-ALD).

The dielectric deposited for the gate is Al_2O_3 with a thickness of 30 nm. For the CEA-Leti MOSc-HEMT, the precursor for Al is Trimethylaluminum (TMA) and the reactant is H_2O, with a temperature deposition of 300°C [60]. The reaction between TMA and H_2O can be written as follow:

$$(A)\ Al-OH^* + Al(CH_3)_3 \rightarrow Al-O-Al(CH_3)_2^* + CH_4 \tag{1.10}$$

$$(B)\ Al-CH_3^* + H_2O \rightarrow Al-OH^* + CH_4 \tag{1.11}$$

However, the reaction can be incomplete with H_2O leaving defective Al-Al and Al-O-H bonds. Other reactants can be used such as ozone (O_3) and O_2 plasma to increase the reactivity between the precursor and the reactant [38], [73], [74]. For ozone, the amount of Al-Al and Al-O-H bonds are reduced [38], but still the amount of carbon and oxidation at the GaN surface increases [73]. O_2 plasma also reduces -OH groups [75], [76], but the GaN oxidation is increased [76], [77]. To avoid the damage caused by the ozone or O_2 plasma, a thin H_2O-based Al_2O_3 can be deposited before [73], [76], but concerns remain in terms of reliability. That is why the H_2O-based Al_2O_3 was chosen for the MOSc-HEMT.

In terms of environmental footprint, similarly to MOCVD, the impact of ALD is mainly due to the demanding electrical power for the process and its long process time [56]. The same conclusion for MOCVD can be drawn to reduce the ALD process impact.

1.4.1.6 Gate metal deposition and contact fabrication

After dielectric deposition, a W/TiN metal stack is deposited by Plasma-Enhanced Chemical Vapor Deposition (PE-CVD) for W and Physical Vapor Deposition (PVD) for TiN in order to form the metal gate. The TiN is firstly deposited to have a higher V_{TH} due to the higher metal work function, while W is deposited after to reduce the gate metal resistivity and to fill the gate cavity. In fact, the TiN deposition is not very conformal leading to gaps at the corner of the gate cavity if the thickness is too high.

After the MIS gate is fabricated, the source and drain contact are fabricated by etching the AlGaN barrier and depositing a Ti/Al bilayer. After deposition, a contact annealing is performed between 400 to 650°C for 2 min under N_2 to improve the contact. The fabrication is continued with the metallic vias being

fabricated, and at last a final annealing for several hours at low temperature is performed to reduce the variability of transistor characteristics as represented in **Figure 1.18**.

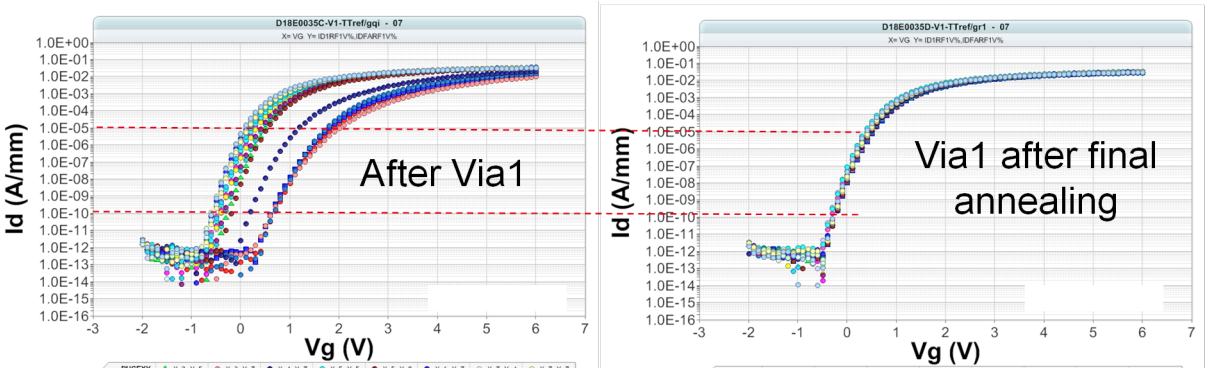


Figure 1.18: I_D-V_G for MOSc-HEMT before and after the final annealing.

1.4.2 MIS gate optimization

After fabrication, the Dielectric/GaN stack and interface are impacted mainly by the etching, the surface preparation and the dielectric deposition with defects and roughness as represented in **Figure 1.19**, mitigating the adoption of the MOSc-HEMT.

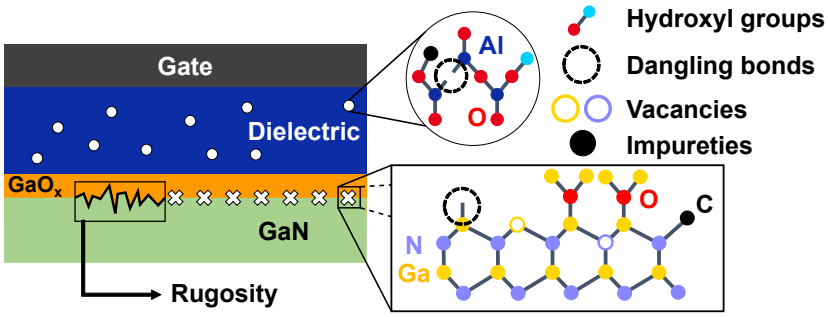


Figure 1.19: Schematic representation of defects that can be encountered in Dielectric/GaN stack and interface.

In fact, as described, etching can damage the surface, impacting the device with a lower mobility [78], an increased amount of interface states impacting the mobility, V_{TH} and the subthreshold slope [62], [63], [78], [79]. ALE allows to partially restore the damage [80], but the roughness is still present.

Surface preparation and dielectric deposition are also a concern with the presence of impurities both at the interface and in the dielectric, but also with the presence of an interfacial GaO_x [60]. In fact, this GaO_x is difficult to remove [81] and can induce V_{TH} instability by electron trapping [75], [82] and/or V_{TH} reduction [60]. Impurities such as -OH groups present in the dielectric as discussed in the **Section 1.4.1.5** can induce electron trapping leading to V_{TH} instability [38], [73], [75], [83]. It is therefore essential to optimize the dielectric/GaN stack and interface.

The overall studies in the literature have been performed on transistors or planar capacitors. For the transistor, mainly the Threshold Voltage (V_{TH}), the Threshold Voltage hysteresis (ΔV_{TH}) and the electron mobility were considered. For capacitors, the Flat-Band Voltage (V_{FB}), the Flat-Band Voltage hysteresis (ΔV_{FB}) and the Interface states density (D_{it}) were evaluated to study the Dielectric/GaN interface. The correspondence between the two devices can be made for planar devices, but the presence of the gate

cavity adds the impact of sidewalls which needs to be taken into account. Having that in mind, the different possible paths to optimize the MIS stack will be presented in the following section, from the etching to the dielectric deposition and post-processing.

1.4.2.1 Etching and surface treatments

To minimize the damage from the ICP-RIE etching, different approaches are possible:

1. Elimination or reduction of the plasma-induced damage using etching methods without plasma or low ICP bias power.
2. Recovery of the damaged layer.
3. Removal of the damaged layer.

Etching

The etching without plasma is possible with Photoelectrochemical (PEC) etching with photo-assisted oxidation since typical wet etchings have a lower impact on GaN [84]. The process is based on the generation of holes at the Electrolyte/GaN interface, the latter breaking down GaN into Ga^{+3} ions. The ions react with the electrolyte resulting in Ga_2O_3 that can latter be dissolved by acid or basic solutions such as H_3PO_4 and KOH [85] or H_2SO_4/H_3PO_4 [86]. This etching technique was reported to present a better sub-threshold slope (SS) indicating a better Dielectric/etched GaN interface [84]. Etching with low ICP bias power is possible by the presented ALE approach in **Section 1.4.1.3**.

Another technique without or with little impact of the recess to form the gate cavity is the Selective Area Growth (SAG) in which either the AlGaN (or GaN) region is not grown [87] or a GaN layer is regrown on the recessed GaN [88]. In the case of the recessed GaN, SAG faces the same challenges with the negative impact of etching and exposure to air. The exposure to air before dielectric deposition is also a challenge for SAG without recess. Still, this technique is promising due to the lower impact than ICP-RIE etching [87]. It can also be followed by an *in-situ* dielectric deposition which increases the electron mobility [89].

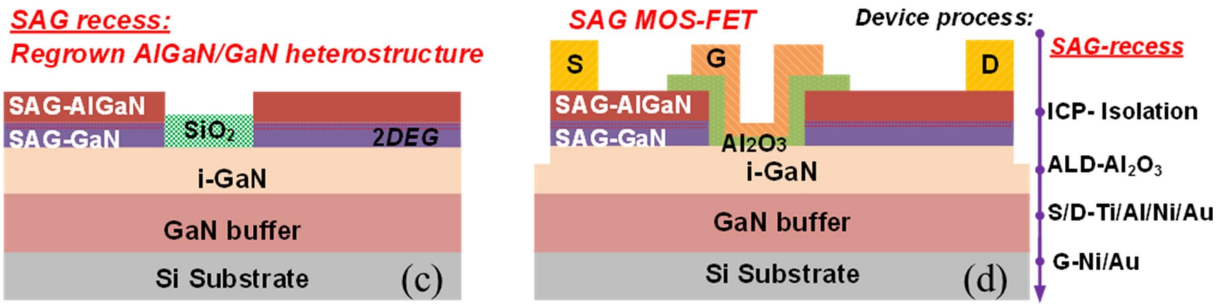


Figure 1.20: Schematic representation of the Selective Area Growth process without gate recess [87] [3].

Other than the presented ALE procedure, the digital etching approach is another way to reduce the etching damage. It is based on the oxidation of the GaN surface and subsequent removal of the formed gallium oxide. The oxidation can done by a low power O_2 plasma [37], [90]–[92], a N_2O plasma [93] or

wet solutions such as H_2SO_4/H_3PO_4 [94]. The removal of the gallium oxide can done by a low power plasma BCl_3 [91], which acts as a self-limiting process due to the fact that BCl_3 etching of GaN is lower than gallium oxide. The removal can also be performed with wet HCl [37], [90], [93], [94]. Moreover, with the difference in oxidation between AlGaN and GaN, TMAH and KOH can be used to selectively etch the oxidized AlGaN and stop at the GaN layer [95]–[97].

Surface treatments

To recover or remove the damaged layer, different surface treatments can be performed. Extensive treatments have been studied for the GaN surface, as reported in the excellent review of Bermudez [98]. A particular issue that remains after wet cleaning is the presence of GaO_x after dielectric/oxide deposition. In fact, Duan et al. [99] reported a reoxidation forming a GaO_x layer with a thickness of 0.5 Å during the surface exposure to ambient air before XPS measurement or during the wet treatments (HF and/or DI water rinse). To remove it before dielectric deposition, an *in-situ* $NH_3/Ar/N_2$ plasma sequence called Remote Plasma Pretreatment (RPP) can be performed to remove GaO_x and form a Nitridated Inter-Layer (NIL) [82]. The NH_3/Ar sequence removes GaO_x while the N_2 sequence nitrides the surface, passivating V_N defects [82], [100], [101]. Other plasma sequences such as H_2/NH_3 cycles [102], a sequence of NH_3/N_2 or N_2/H_2 [103][104] can be used before ALD of AlN, SiN_x, or even epitaxy, allowing to decrease the hysteresis, reduce the R_{ON}, but decrease V_{TH}. Therefore, combining different treatments seems to be a good approach to achieve the desired surface preparation [105].

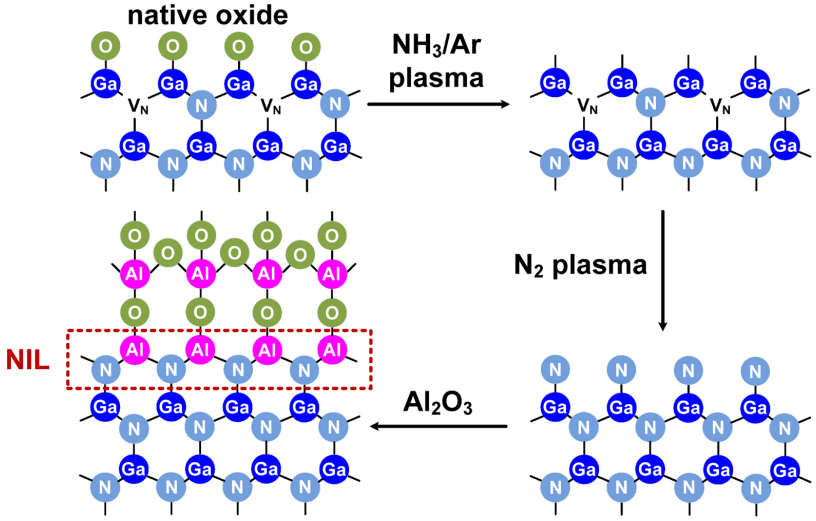


Figure 1.21: Schematic representation of the RPP process for GaN surface treatment prior to Al_2O_3 deposition, forming an NIL at the interface [101](©IOP Publishing. Reproduced with permission. All rights reserved).

Considering the gate cavity with polar and non-polar plans, few studies demonstrate the GaN crystallographic orientation impact on the effectiveness of surface treatments and on electrical characteristics of the device [106]–[109]. In particular, sidewall formation has been reported to significantly impact the device performance [79].

[3]Reprinted from *Correlating device behaviors with semiconductor lattice damage at MOS interface by comparing plasma-etching and regrown recessed-gate Al_2O_3/GaN MOS-FETs*, 546, Liang He, Liuan Li, Fan Yang, Yue Zheng, Jialin Zhang, Taotao Que, Zhenxing Liu, Jinwei Zhang, Qianshu Wu, Yang Liu, p. 3, Copyright (2021), with permission from Elsevier.

1.4.2.2 Interfacial layer and dielectrics

Interfacial layer

The growth of a thick native gallium oxide is difficult [110], meaning that a dielectric layer needs to be deposited in order to form a MIS gate. At the Dielectric/GaN interface however, the presence of an interfacial gallium oxide layer GaO_x and the lattice mismatch between the dielectric layer and the GaN substrate have to be controlled to optimize the device parameters (V_{TH}, D_{it}, and mobility...).

Reducing the gallium oxide (GaO_x) with wet cleaning and plasma treatments is a solution as presented in the previous section. Improving the GaO_x is another approach by creating a high-quality interfacial GaO_x. For instance, using the chamber of a Low-Pressure Chemical Vapor Deposition (LPCVD) prior to SiN_x deposition, the formation of high-quality GaON layer was reported by oxidizing the etched GaN surface with an O_2 plasma and subsequently annealing the surface at a high temperature under N_2 [90], [111], [112]. The introduction of the GaON layer was proven to induce a V_{TH} of 1.15 V and a reduced hysteresis of 0.2 V [90]. Under negative stress, hole injection was also limited thanks to the higher valence band offset between the interfacial GaON and the GaN substrate [111], [112]. In terms of moblity, GaON formed by N_2O plasma allows to increase the electron mobility [113], possibly from the reduced damage caused by the SiN_x LPCVD [114].

Another solution other than improving or reducing the interfacial GaO_x is to deposit a thin interfacial AlN layer since AlN has a lower lattice mismatch with GaN than other dielectrics (SiN_x,SiO_2, and Al_2O_3) [115]. Nonetheless, AlN can be easily oxidized, even at ambient air, requiring the subsequent *in-situ* deposition of the upper dielectric layer. Such oxidation property can be however useful to prevent the GaN surface oxidation during oxide deposition such as with SiO_2 or Al_2O_3. In terms of electrical properties, AlN deposited before Al_2O_3 on c-plane (0001) and m-plane ($1\bar{1}00$) GaN present a reduced ΔV_{FB} and D_{it}, with better results on m-plane [116]. In a MOSc-HEMT, 2 nm PEALD AlN deposited before Al_2O_3 improves ΔV_{TH} from 800 mV to 65 mV and reduces D_{it} [43]. For a Al_2O_3/AlN/etched GaN stack, Liu et al. have also reported a reduction of hysteresis and D_{it} when AlN is deposited after the NIL process, the improvement being explained by a greater separation from Al_2O_3 defects [44], [117]. For AlSiO, AlN increases the electron mobility thanks to confined electrons at the AlN/GaN interface [118] while reducing the diffusion of Ga into AlSiO for Post-Deposition Anneal (PDA) at high temperature (i.e. 950°C) [119].

Therefore, GaO_x can be either removed by cleaning/plasma steps or improved by oxidation and annealing steps in order to produce a GaO_x with less defects. AlN can also be deposited before the dielectric to protect the GaN surface, to improve V_{TH} and its hysteresis, the D_{it}, and the electron mobility.

Dielectrics

Regarding the dielectric deposited to form a MIS gate, the desired properties are :

- A Band gap larger than GaN to have a conduction band offset higher than 1 eV.

- A dielectric layer without grain boundaries to avoid large leakage current, and with high chemical/thermal stability.
- A high permittivity to increase the transconductance, the channel mobility, and consequently R_{ON}.
- A high breakdown voltage to withstand high voltages.

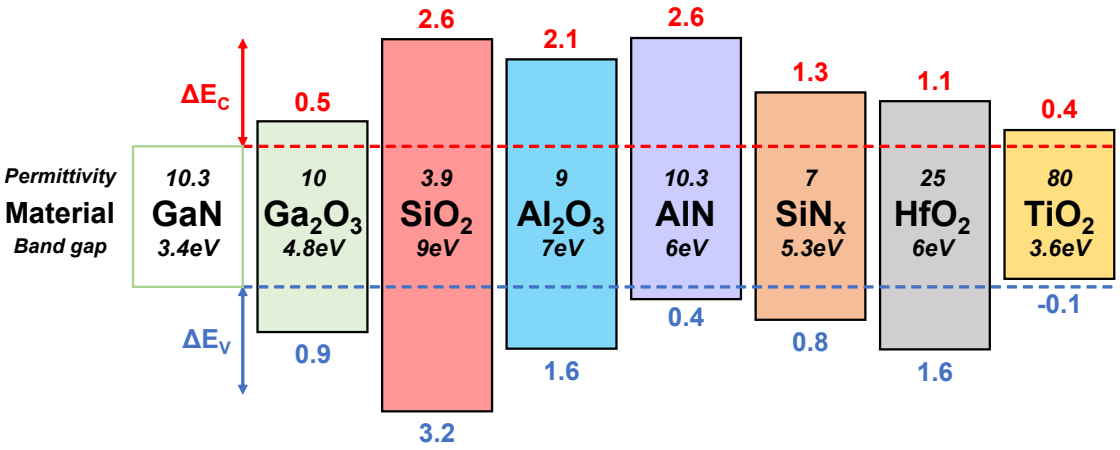


Figure 1.22: Schematic representation of reported band alignments between different dielectrics and GaN. Their respective band gap and permittivity are represented [120]–[123].

Various dielectric candidates with material properties and band alignments with GaN are represented in **Figure 1.22**. Having both a high permittivity and a high band gap is not possible since both properties are inversely proportional. This limits the choice to SiO_2, SiN_x, Al_2O_3 and HfO_2. From the mentioned dielectrics, only HfO_2 is not commonly used as a gate dielectric in the literature.

SiO_2 is a good candidate with a high gap (∼9 eV) but a low relative permittivity (∼3.9) [124], [125], and high thermal stability on GaN (>800°C). The large gap reduces the gate leakage current and the high thermal stability enables high thermal budgets during the fabrication process. Still, the high thermal stability does not prevent the diffusion of Ga into SiO_2 for annealing higher than 800°C, causing a reduction of breakdown voltage and a rise of leakage current [126]. Moreover, after annealing at 800°C, a negative shift of V_{FB} was reported and attributed to Oxygen Vacancies (V_O) induced by hydrogen reduction in GaO_x [127].

SiN_x has a lower gap (5∼7 eV) but a high permittivity (7.5), and is often used as a capping layer to prevent current collapse between the gate and the drain [128], [129]. For the gate, SiN_x was reported to passivate Nitrogen Vacancies (V_N) for AlGaN/GaN heterojunctions [39], [130]. A large disadvantage for SiN_x is the small band gap leading to leakage current from both electrons and holes [111], [131]

As described in **Section 1.4.1.5**, Al_2O_3 is the dielectric used in the MOSc-HEMT fabricated at CEA-Leti. In fact, ALD Al_2O_3 has a band gap of 6.8∼7 eV [132], [133] with permittivity varying between 8 to 10 [124], [125]. Various D_{it} were reported with values ranging from 10^{11} to 10^{13} $eV^{-1}.cm^{-2}$ with treatments before or after Al_2O_3 deposition [132], [134], [135].

One way to optimize the Al_2O_3/GaN gate stack is to perform Post Deposition Annealing (PDA) and/or Post Metallization Annealing (PMA). For PDA, usually between 400 and 800°C, V_{TH}/V_{FB} increases [136]–[139], ΔV_{TH} reduces [140], and electron mobility increases [81], [136], [139]. Such improvement

was explained by a reduction of positive charges in GaO_x [139], [141], in Al_2O_3 [138], and/or the reduction of D_{it} [137], [140], [142]. The PDA atmosphere is also important with forming gas (N_2/H_2) being reported to reduce D_{it} [135] while O_2 was reported to also reduce D_{it} [135] and increase V_{FB} [74], potentially by reducing V_O in Al_2O_3 [138]. Still, for O_2, an increased GaO_x is also noticed [74], potentially harming the interface, as well as an increased hysteresis [135]. Using N_2 is commonly observed in the literature, but with Winzer et al. [135] reporting an increased D_{it} although a lower hysteresis is found. For PMA, which can be related to contact fabrication and annealing, it was reported to also reduce positive charges [139], [143]–[145] and to reduce D_{it} [144], [146].

Nonetheless, both for PDA and PMA, a disadvantage is the low thermal stability of Al_2O_3 when deposited on GaN, with crystallization at 800°C when deposited on as-grown GaN surfaces [132], [147]. Such limitation is necessary to take into account where the gate is fabricated before the contacts as demonstrated by Hori et al. [132], when the PDA and or PMA is applied (i.e. maximal annealing temperature) but also in regard to the whole thermal budget associated to the MOSc-HEMT fabrication.

Consequently considering the limitations of each dielectric, an interesting solution is to combine each dielectric into alternative dielectrics such as AlSiO and AlON. To do so different approaches exist. For AlSiO, the ternary alloy formed from Al_2O_3 and SiO_2 can be deposited by:

- Sputtering aluminium target doped with silicon [148], [149].
- MOCVD [150]–[152].
- Nanolaminates of Al_2O_3 and SiO_2 deposited by ALD [153], [154].

Combining the properties of Al_2O_3 and SiO_2, AlSiO has larger band gap than Al_2O_3 and higher permittivity than SiO_2, the values between SiO_2 and Al_2O_3 depending on the ratio Si/Al [154]. Therefore, for higher Si content, the leakage current is reduced due to an increased conduction band offset with GaN [153], [154]. Hysteresis ($\Delta V_{TH}/\Delta V_{FB}$) is reported to reduce compared to Al_2O_3 [149]–[151]. By varying the percentage of Si of MOCVD AlSiO, Sayed et al. also notice a reduced ΔV_{FB} with Si content up to 46%, a higher concentration leading to counterclockwise hysteresis or reversed hysteresis due to possibly mobile charges [152].

However, for V_{TH}/V_{FB}, different values are reported regarding the Si content, probably because of the different deposition methods [118], [149], [151], [153]. Nonetheless, Smith et al. [118] observed an increasing V_{TH} with increasing Si content, the latter being amplified by an interfacial AlN layer. This seems to be in agreement with Density Functional Theory (DFT) simulation proposed by Chokawa et al. [155] in which neutral V_O defects observed in SiO_2 are favored to positive V_O defects observed in Al_2O_3 [156], [157]. Still, such defects in Al_2O_3 have the (2+/0) transition energy level (1.9∼3.5 eV from GaN's valence band for an Al_2O_3 valence band offset of 0.9 eV) under the Fermi level for both n-GaN and UID-GaN substrates, leading to a neutral charge state. Concerning the interface between AlSiO and (0001) GaN, Chokawa et al. [158] reported by DFT simulation the absence of dangling bonds due to the oxygen bonds from AlSiO. Low D_{it} have indeed been observed [150], [151].

With the incorporation of Si, the thermal stability of AlSiO is higher than Al_2O_3 [150], [159]. With in-

creasing PDA temperature (650°C-1050°C), ΔV_{FB} is reduced with an I-V plateau related to electron traps disappearing at 850°C [159]. However, for a PDA at 950°C, a crystallized region close to the GaN interface was observed [160]. Moreover, Sayed et al. [161] reported by atom probe microscopy the diffusion of Ga from the (0001) GaN surface, forming an AlGaSiO interfacial layer and increasing the D_{it}. Such observation was made for AlSiO deposited by MOCVD at a high temperature (700°C), this temperature possibly explaining the diffusion of Ga. To avoid crystallization, a thin SiO_2 can be deposited [160], the interfacial layer increasing the field effect mobility by 50% (i.e. 27.7 to 58.6 $cm^2.V^{-1}.s^{-1}$).

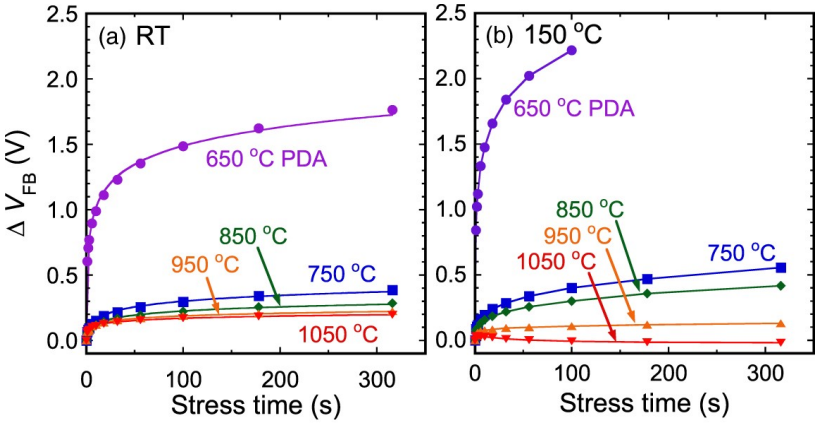


Figure 1.23: V_{FB} shift under a positive bias stress at both (a) room temperature and (b) 150°C for AlSiO with 21%Si for n-GaN MOSCAPs. Different PDA temperatures were tested [159](©The Japan Society of Applied Physics. Reproduced by permission of IOP Publishing Ltd. All rights reserved).

Regarding AlON, similar to AlSiO, it combines the properties of Al_2O_3 and AlN. It can be deposited by:

- Sputtering of an Al target with a flow of N_2 and O_2 [162].
- Nitriding an ALD Al_2O_3 with a N_2 plasma [163], [164].
- ALD by using N_2/O_2 precursors together with TMA [165].
- ALD with nanolaminates of Al_2O_3 and AlN [166], [167].
- Oxidizing an AlN layer [133], [168].

The introduction of nitrogen in Al_2O_3 reduces the band gap and should increase the permittivity [131], but lower permittivity has been reported [133]. In terms of hysteresis, AlON is reported to have a lower hysteresis than Al_2O_3 [133], [162], [164], [166], [169], explained by passivated V_O defects in the dielectric [170] but also a higher conduction band offset [133], [162], [164]. In fact, Nozaki et al. [133] observed a reduction of electron injection with increasing nitrogen content. Moreover, using a MOSc-HEMT, Kang et al. [164] have reported a lower V_{TH} shift under a positive stress for AlON compared to Al_2O_3 (cf. **Figure 1.24, left**). Nonetheless, if the electron injection is reduced with AlON, Hosoi et al. have observed a hole injection which can be an issue for negative stress. The hole leakage might be explained by defective N2p orbitals near AlON's valence band [171].

Nitrogen also seems to induce the presence of negative charges, increasing the V_{FB} [163], [166]. Still, a recent report for AlON in a MOSc-HEMT gate does not highlight a higher V_{TH} than Al_2O_3 [164]. Moreover, contradictory DFT simulations are reported regarding the effect of nitrogen in Al_2O_3, with

Choi et al. [172] reporting the presence of negative charges, and Guo et al. [83] reporting the absence of any charge states. In terms of interface with GaN, AlON is reported to have a lower D_{it} mostly for energy levels higher than 0.35 eV from GaN's conduction band, possibly by a reduced interfacial GaO_x [162], [164], [166], [169]. With such an improved interface, the use of AlON improves the field effect mobility of MOSc-HEMTs by 19% (235 $cm^2.V^{-1}.s^{-1}$) compared to using Al_2O_3 (cf. **Figure 1.24, right**) [164].

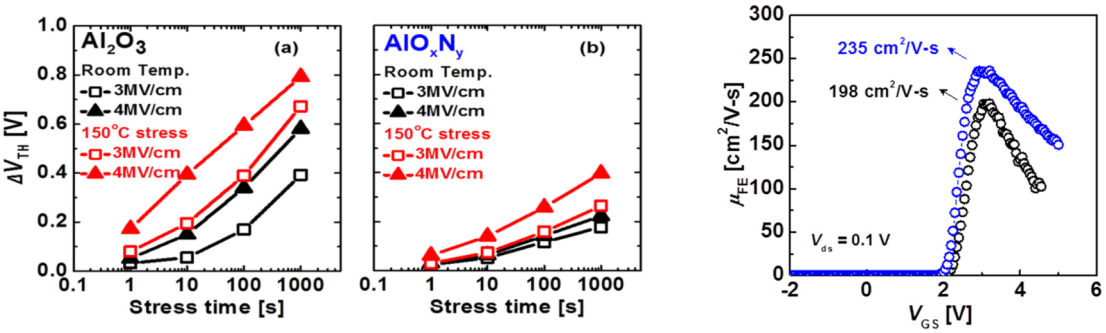


Figure 1.24: For a MOSc-HEMT with Al_2O_3 or AlON: on the left, V_{TH} shift under a positive bias stress at both room temperature and 150°C; on the right, the field effect mobility extracted using a drain voltage of 0.1 V [164](©IOP Publishing. Reproduced with permission. All rights reserved).

Similarly to AlSiO, the presence of nitrogen increases the thermal stability of AlON up to 800°C on AlGaN [162]. High PDA or PMA temperature can therefore be used, with reported higher V_{FB} and reduced ΔV_{FB} [163], [169]. However, no further studies of the impact of annealing are reported for AlON, more specifically for AlON on etched GaN.

The following table (**Table 5.5**) summarizes the advantages and drawbacks of the discussed dielectrics. From the table, it is clear that the alternative dielectrics have interesting properties compared to Al_2O_3 and SiO_2 but they still have drawbacks to consider.

	SiO_2	Al_2O_3	AlSiO	AlON
Band gap (eV)	9	6.8	6.8 to 9 for increasing Si content	6.5 to 7
Permittivity	3.9	8-10	8 to 3.9 for increasing Si content	7.4 (8%N)
Crystallization T°C on GaN (°C)	>800	<800	950	>800
Advantages	High band gap High T°C stability	Sufficient band gap High permittivity	High T°C stability High band gap Medium permittivity Lower defects and D_{it}	High T°C stability High permittivity V_{FB} modulable with %N Low defects and D_{it} Higher mobility
Drawbacks	Diffusion of Ga for T°C at 800°C = leakage current Lower V_{FB}	Low T°C stability Defects	Ga intermixing at interface	Hole traps

Table 1.4: Summary of properties for the discussed dielectrics, with their advantages and drawbacks [112], [125], [127], [132], [133], [153], [154], [161], [167], [171].

1.5 Objectives of the PhD project

As demonstrated, the Dielectric/GaN stack and interface is a critical component of the MOSc-HEMT, causing reliability issues and hindering the adoption of the MOSc-HEMT. The etching, the surface preparation and the dielectric deposition are the most impacting steps in the fabrication flow and need to be addressed to control and optimize the MIS gate stack. Different paths can be found in the literature, but properly characterizing the impact of different fabrication steps is relevant to understand the possible ways to optimize the Dielectric/GaN stack.

This work takes place in the context of further optimizing MOSc-HEMT gate stack fabricated and developed at CEA-Leti. Recent efforts have been made towards optimizing the etching [66], [80] and the surface preparation [60], [67] before dielectric deposition. This PhD project aims to :

- Expand the understanding on the impact of etching and dielectric deposition by developing physico-chemical characterization methods (HAXPES/AFM) as a complement of planar capacitors.
- Study with the developed methodology the impact of different dielectrics and post-deposition annealing in order to increase V_{FB}, reduce its associated hysteresis ($\Delta V_{FB} < 100$ mV), and reduce the interface states density ($D_{it} < 10^{11}$)

These studies were therefore based on the comparison and correlation of physical-chemical analyses with electrical measurements performed on simplified MOS capacitor structures. Therefore, my work as a PhD student dealt with preparing and fabricating the coupons and analyzing them with HAXPES, GIXRD and C-V measurements. Complementary analyses were performed by TEM, ToF-SIMS and FTIR. As far as possible, samples were prepared using the same steps used in the MOSc-HEMT prior to the dielectric deposition.

1.6 Conclusion of this chapter

The increasing demand for reliable and efficient power devices is pushing the development of WBG-based power devices over Si-based power devices. In fact, GaN offers faster and more efficient power converters. Combining AlGaN and GaN in a heterojunction allows to form an electron gas with high mobility in order to fabricate High Electron Mobility Transistors (HEMTs). In the context of power electronics, HEMT reduces the conduction and switching losses associated with the reduced ON-state resistance (R_{ON}) and the increased switching frequency.

Nonetheless, AlGaN/GaN HEMTs are Normally-ON with a negative threshold voltage (V_{TH}), which causes safety issues and complexifies the driver design. Hence, Normally-OFF devices are highly desirable. Different architectures are proposed to obtain the Normally-OFF behavior, the p-GaN being the architecture widely adopted in the industry. However, it still suffers from gate leakage and limited gate voltage swing.

MOS-channel HEMTs (or MOSc-HEMTs) have the potential to solve these issues while maintaining a Normally-OFF behavior. The positive voltage is obtained by recessing the AlGaN layer at the gate

region and fabricating a MIS gate in order to reduce the gate leakage. Still, the Dielectric/GaN interface is a critical component of the MOSc-HEMT inducing reliability issues and limiting the adoption of the MOSc-HEMT.

Therefore, the aim of this PhD project is to optimize the Dielectic/GaN interface by characterization the impact of different fabrication steps, and by expanding on recent works performed at CEA-Leti with studies mainly directed towards the impact of different dielectrics and post-deposition annealing. To do so, physical-chemical characterization methodologies were developed and used alongside simplified electric vehicle tests.

2

Methodology and experimental set-up

This chapter aims to present the different structures and their fabrication alongside the different characterization techniques used in this thesis. A complementary approach with dedicated structures for electrical and physical-chemical characterization is necessary to understand the impact of different processes on the Dielectric/GaN gate stack and interface.

Contents

2.1 Fabricated structures

The study of the dielectric/GaN interface and MIS gate requires different test structures and devices in order to extract complementary information. Small and simplified coupons allow to easily access both physical-chemical and electrical information of the gate stack, and rapidly evaluate the impact of different processes. The electrical measurements together with some physical-chemical measurements (TEM/HAXPES) are performed on fabricated MOS capacitors (MOSCAPs). For the rest of the physical-chemical measurements, dedicated Dielectric/GaN coupons are fabricated. They consist only of planar MOS or OS structures simulating the bottom gate region. To access the sidewalls and the desired transistor parameters to be optimized, MOSc-HEMTs are used. Notably, the impact of sidewalls is not to be neglected since its contribution in a MOSc-HEMT is not negligible, as demonstrated by the gate morphology impacting the MOSc-HEMT parameters such as V_{TH} and the electron mobility [46]. The different structures are then:

- **Samples**: In the form of a Dielectric/GaN stack, physical-chemical characterization can be easily performed on them.
- **MOS-1**: They are capacitors fabricated on coupons with fewer and simpler steps as real devices. It allows to scan multiple processes with fewer resources and wafers. However, it does not follow all the processes used in the fabrication of a MOSc-HEMT, mostly the metallization.
- **MOS-2**: They are capacitors fabricated on 200 mm wafers with fabrication steps as close as possible to a MOSc-HEMT. More MOSCAP per process being tested can be fabricated but in order to evaluate different processes, multiple wafers are required contrary to MOS-1 devices.
- **Simplified MOSc-HEMT (GaNG)**: They are transistors with fewer fabrication steps (mainly gate and contact). GaNG layout has multiple layout variations, essential for the R_{ON}/mobility extraction. However, Their simplified process flow without field plates hinders their characterization at high voltages.
- **MOSc-HEMT**: The full MOSc-HEMT transistor allowing full electrical characterization, but with longer fabrication and thus limited variation of process steps.

For both MOSCAPs, the GaN substrate was n-doped with Si in the order of 5×10^{17} cm^{-3}, which is different from the UID-GaN substrate used in MOSc-HEMT. Without the 2DEG, the GaN substrate needs to be doped to have a sufficient amount of free carriers, allowing characterizations such as C-V measurements. **Table 2.1** summarizes all the differences, advantages, and limitations of each structure.

Considering all structures, it is clear that each one is important to understand the Dielectric/GaN stack and to optimize it. Still, their own limitations are also important to consider while using them. In this thesis, samples and MOSCAP structures were mainly used due to their accessibility and versatility, but GaNG transistors were also employed to characterize the electron mobility. In the following sections, the different structures process flow will be presented.

Capabilities	Samples	MOS-1	MOS-2	GaNG	MOSc-HEMT only FEOL (Section 1.4.1)
Minimum fabrication steps	**2-5**	**7**	**10**	**26**	**48-60**
Lithography steps	**0**	**1**	**1**	**5**	**11**
Dimension	**Coupon**	**Coupon**	**200 mm**	**200 mm**	**200 mm**
GaN Doping under the gate (UID/n-type)	**Both**	**n-type**	**n-type**	**UID**	**UID**
Gate region studied	**Bottom**	**Bottom**	**Bottom**	**Bottom & Sidewalls**	**Bottom & Sidewalls**
$V_{FB}/\Delta V_{FB}$	✗	✓	✓	✗	✗
$V_{TH}/\Delta V_{TH}$	✗	✗	✗	✓	✓
Measure-Stress-Measure for Bias Temperature Instability degradation	✗	✓	✓	✓	✓
R_{ON}	✗	✗	✗	✓	✓
Mobility extraction μ	✗	✗	✗	✓	✓
Full transistor / High Voltage characterization	✗	✗	✗	✗	✓
Oxidation at Diel/GaN interface (XPS/HAXPES)	✓	✗ (XPS) ✓ (HAXPES)	✗ (XPS) ✓ (HAXPES)	✗	✗
Atomic distribution in Diel/GaN stack (ToF-SIMS)	✓	✓	✓	✗	✗
Dielectric structure/ crystallization (GIXRD/TEM)	✓(GIXRD) ✓(TEM)	✓ (TEM)	✓ (TEM)	✓ (TEM)	✓ (TEM)
Gate morphology (TEM/SEM)	✗	✗	✗	✓	✓

Table 2.1: Summary of the different test structures in order to study different processes or obtain a specific information on the MOSc-HEMT gate.

2.1.1 Samples for physical-chemical characterizations

The samples for physical-chemical characterization were fabricated both at the CEA-Leti clean room and at the Plateforme Technologique Amont (PTA) with surface areas ranging from 1×1 cm^2 to 4×6 cm^2. The samples can be cut from bigger samples or 200 mm wafers before or after dielectric deposition, allowing for instance to etch the GaN surface with the same process used for MOSc-HEMT in a 200 mm tool and then to deposit the dielectric layers at the PTA. These samples are useful for the characterization of the Dielectric/GaN interface or the full gate stack with X-ray Photoelectron Spectroscopy (XPS), Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS), and Grazing Incidence X-ray Diffraction (GIXRD).

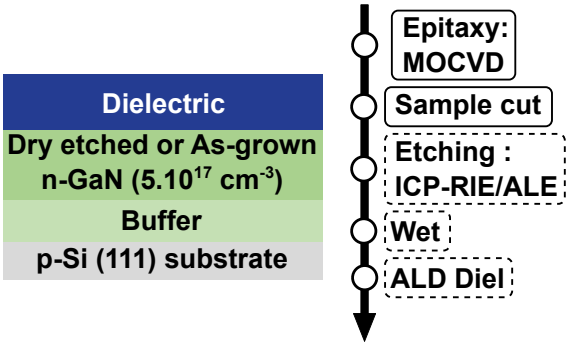


Figure 2.1: The sample process flow. Process in dashed boxes are used depending on the study.

2.1.2 MOS-1: MOSCAP on coupons

These MOS capacitors fabricated at the Plateforme Technologique Amont (PTA) on 1.5×1.5 cm^2 coupons were also diced either before or after dielectric deposition following the MOSc-HEMT process flow. The dielectric deposition by ALD and/or PE-ALD is also possible at the PTA through a Flexal from Oxford Instruments. In that case, the surface preparation used in the MOSc-HEMT cannot be applied just before deposition (manual transfer from a clean room to another one). As a substitute, the samples were cleaned with HCl for 3 min. This wet treatment is used since it's more accessible and less dangerous than a wet treatment with HF. Moreover, HCl is found to reduce GaN native oxide, passivating the surface with Cl atoms [67], [173]–[176]. In the case of a dielectric deposited at the CEA-Leti clean room, the same surface preparation used in MOSc-HEMTs can be applied for as-grown or etched n-GaN samples. An example of MOSCAP and the process flow at the PTA after dielectric deposition is represented in **Figure 2.2**. The process consists only in the fabrication of the metal contacts, as follows:

- Lithography step in a positive resin (AZ1512 HS) to form circular gap rings.
- Metal deposition of gold and nickel (100 and 30 nm respectively) with e-beam evaporation. The nickel is used as an adhesion layer for gold.
- Lift-off process with acetone and isopropanol.

The inner contact is used as a "gate" and the side as a lateral contact. The inner contact diameter ranges from 100 to 1500 µm. The gap is defined to be equal to 150 µm. For annealing, a Rapid Thermal Processing (RTP) oven with either N_2 or O_2 is also available. The gas atmosphere can influence the

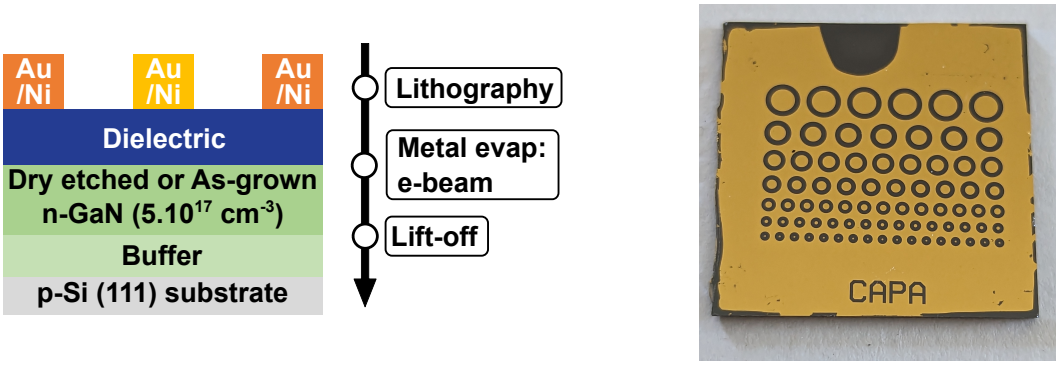


Figure 2.2: On the left, the PTA process flow; on the right, the final MOS capacitor.

annealing effect on the gate stack, but in order to only have the impact of temperature, N_2 was always used as ambient gas.

As mentioned in **Section 2.1**, the advantage of MOS-1 devices is the possibility to rapidly carry out many process variations. It also allows to use less GaN wafers which are costly and long to epitaxiate. Nonetheless, in terms of environmental footprint [177], the use of gold as a contact metal has a strong impact. Considering the amount of gold and nickel deposited, the gold is 10^4-10^5 times more detrimental than nickel (**Table 2.2**). In this thesis, this metal stack was kept but in perspective, it will be important to change the top metal contact by another metal less detrimental such as TiN or Al. As described in **Table 2.2**, by substituting all the Au and Ni by Al, the environmental impact is divided by a 10^5-10^7 factor.

Metal	Mass used (g)	Climate change (CO2-Eq)	Ecotoxicity, freshwater (CTUe)	Resource use, minerals and metals (Sb-Eq)
Gold (Au)	4.34×10^{-7}	2.10×10^{-2}	5.5	2.82×10^{-5}
Nickel (Ni)	6.01×10^{-8}	1.08×10^{-6}	1.24×10^{-4}	1.36×10^{-6}
Aluminium (Al)	7.90×10^{-8}	7.77×10^{-7}	1.73×10^{-5}	1.39×10^{-12}

Table 2.2: The Environmental footprint impact of different gate metals for different criteria, considering the mass of metal used in a 1.5×1.5 cm^2 coupon.

2.1.3 MOS-2: MOSCAP on 200 mm wafers

These MOS capacitors are fabricated on the whole 200 mm wafer with a similar process flow used for the MOSc-HEMTs' gate (i.e. etching and surface preparation) with either as-grown or etched n-GaN surfaces (cf. **Section 1.4.1**). Nonetheless, they differ from the real MOSc-HEMTs' gate by two things:

- The dielectric and the gate metal are deposited on the whole wafer, typically with 30 nm of Al_2O_3, 60 nm of TiN and 300 nm of W.
- The inner metal pad ("gate") and the side ring are fabricated by etching the gate metal until the etching reaches the dielectric layer.

In this configuration, a large number of devices can be tested allowing to have a large statistics. The annealing can also be performed after dielectric deposition with a RTP oven. The MOSc-HEMT final

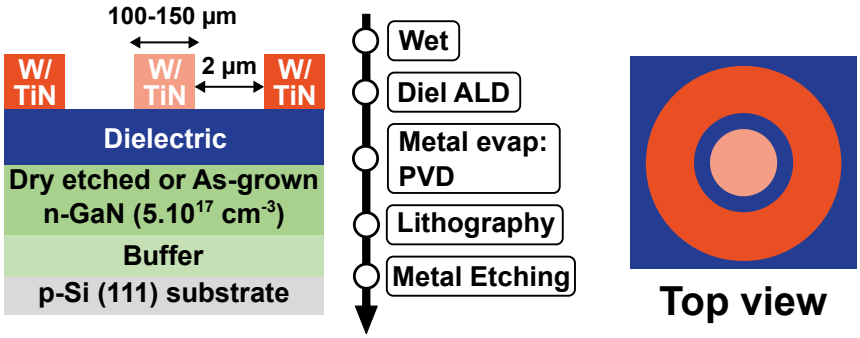


Figure 2.3: On the left, the MOS-2 process flow; on the right, a schematic top view.

thermal budget can also be performed in another RTP oven and thermal furnace, for contact annealing and a long annealing.

2.1.4 GaNG: fast fabricated MOSc-HEMT gate module

MOSc-HEMTs process flow have multiple process steps, turning the fabrication into a lengthy procedure and limiting the number of process variations being tested. To address this issue, a simplified MOSc-HEMT process flow with fewer fabrication steps was developed at CEA-Leti. The main focus is the gate and contact fabrication with multiple layout variations, allowing to test different designs and to perform the R_{ON} and mobility partioning. However, it does not contain the Back-End Of Line fabrication part nor the field plates necessary to manage the electric field at high voltages, thus limiting the characterization of GaNG transistors to low voltages.

2.2 Electrical analyses

2.2.1 Capacitance-Voltage measurements

With the MOS capacitor, Capacitance-Voltage (C-V) measurements were primarily conducted with an Agilent 4284A LCR meter at 1 kHz with an AC signal of 50 mV. This frequency was applied in order to observe both the interfaces and the traps in the dielectric. At the same time, the Normalized conductance (G_m/ω) was measured by acquiring the conductance and then normalizing it with the pulsation ω ($\omega = f \times 2\pi$; f = Frequency). Both C-V and G_m/ω were normalized to the gate surface area. A schematic representation of the contact used to do such measurements is represented in **Figure 2.4**.

Since both MOSCAPs do not have a direct ohmic contact between the side contact and the GaN substrate, two different solutions were considered according to each structure. For MOS-1 devices, since the side contact has a larger area than the inner circular contact, the capacitance associated with the side contact is large and can be neglected with respect to the gate capacitance. Therefore, when measuring, only the gate capacitance is observed.

$$\frac{1}{C_{Total}} = \frac{1}{C_{Gate}} + \frac{1}{C_{Side}} \approx \frac{1}{C_{Gate}} \tag{2.1}$$

In the case of MOS-2 devices, an ohmic contact through the dielectric layer is created by breaking down

the dielectric layer at the side/ring contact. To do so, a Current-Voltage (I-V) measurement is performed between the Si substrate and the side ring with a voltage sweep between 0 to 50 V.

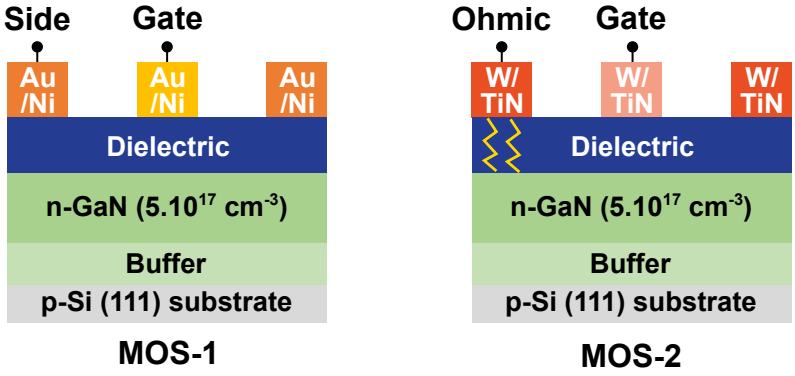


Figure 2.4: On the left, C-V contact for MOS-1 devices; on the right, C-V contact for MOS-2 devices with an ohmic path through the dielectric layer.

2.2.1.1 Flat-band voltage extraction

From *C-V*, the Flat-Band Voltage (V_{FB}) can be extracted, which corresponds to the gate potential applied to flatten GaN's energy bands. It can be calculated using the theoretical C_{FB} as follows [178]:

$$C_{FB} = \frac{C_{ox}C_D}{C_{ox}+C_D} \quad with \quad C_D = \sqrt{\frac{kT\varepsilon_{GaN}\varepsilon_0}{q^2 N_D}} \tag{2.2}$$

Where C_{ox}, k, T, ε_{GaN}, ε_0, and q are respectively the oxide capacitance, the Boltzmann constant, the temperature in Kelvin, the relative GaN permittivity, the vacuum permittivity and the electron elementary charge. The extraction of V_{FB} is interesting due to the fact that it's linked to different sources of charges in the MOS structure. In fact, V_{FB} can be expressed as [178]:

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(\phi_s)}{C_{ox}} - \frac{1}{C_{ox}}\int_0^{t_{ox}} \frac{x}{t_{ox}}\rho_{ot}(x)dx - \frac{1}{C_{ox}}\int_0^{t_{ox}} \frac{x}{t_{ox}}\rho_{mob.}(x)dx \tag{2.3}$$

Where ϕ_{MS} is the difference of work function between the metal and the GaN substrate, Q_f (C.cm^{-2}) is the fixed charges at the Dielectric/GaN interface, Q_{it} (C.cm^{-2}) is the interface charges associated with interface states, ρ_{ot} (cm^{-3}) is the density of traps in the dielectric and $\rho_{mob.}$ (cm^{-3}) is the density of mobile charges in the dielectric. For a given ϕ_{MS}, all these charges impact V_{FB}, and subsequently the gate voltage needed to be applied in order to accumulate electrons at the dielectric/GaN interface. Considering the GaN doping, the gate metal for MOS-1 devices (i.e. nickel), and the absence of charges in the gate stack, the ideal V_{FB} is equal to roughly 1 V. Since V_{TH} is also linked to the accumulation of electrons from the 2DEG at the dielectric/GaN interface, controlling the presence of these charges is essential to increase V_{TH}. To do so, Q_{it}, ρ_{ot}, and $\rho_{mob.}$ need to be reduced, while Q_f can either be reduced or negative charges be implemented. Therefore, V_{FB} can be studied as a first parameter towards a higher V_{TH}.

2.2.1.2 Flat-band hysteresis

Likewise, V_{TH} hysteresis can be partially studied through V_{FB} hysteresis after a voltage sweep back and forth between depletion and accumulation regimes. V_{FB} hysteresis or ΔV_{FB} is the difference between the

V_{FB} for a reverse sweep and a forward sweep:

$$\Delta V_{FB} = V_{FB}^{Reverse} - V_{FB}^{Forward} \tag{2.4}$$

In that case, the charges involved in ΔV_{FB} are mainly ρ_{ot} and $\rho_{mob.}$. In fact, for ρ_{ot}, the electron trapped with a long time constant in a dielectric will remain "fixed" during the measurement, introducing a ΔQ in the MOS structure and increasing V_{FB}. It is only after a given time that this charge is emitted and V_{FB} recovers its former value. This hysteresis will be qualified as clockwise. For oxides, these traps are typically Oxygen Vacancies (V_O) [156]. Concerning $\rho_{mob.}$, these mobile charges in the form of ions (mostly positive) drift across the dielectric layer if enough thermal energy is given to them. Their movement during the measurement affects the distribution of charges in the dielectric layer and consequently impacts V_{FB}. Therefore, instead of having a clockwise hysteresis, a counter-clockwise hysteresis can be observed. An example of C-V characteristics with V_{FB} and ΔV_{FB} extracted is represented in **Figure 2.5**.

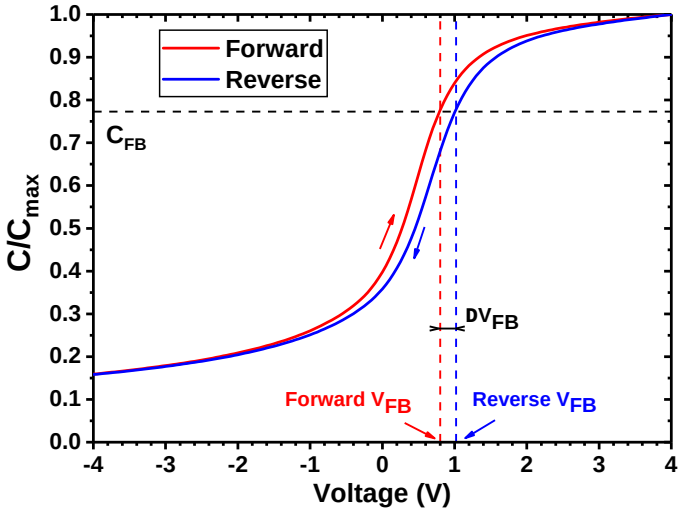


Figure 2.5: Example of C-V characteristics for the Al_2O_3/GaN stack at 1 kHz.

When comparing different dielectrics, it is important to compare the hysteresis for a similar applied electric field. In fact, if a similar capacitance can be obtained for different dielectrics by adjusting their thickness, the maximum gate voltage applied on the thinnest dielectric will lead to a higher electric field and more electron trapping in the dielectric (cf. **Equation 2.6**). Finally, a higher measuring temperature can be used to enhance electron trapping and verify the quality of the dielectric. Defects in a dielectric can indeed be represented by harmonic oscillators in which the transition between the trapped state and the empty one requires an energy barrier to overcome. Increasing the temperature gives enough energy to enable this transition [179].

2.2.1.3 Dielectric constant and dielectric thickness

Other parameters that can be extracted from C-V are the dielectric constant and the dielectric thickness. The dielectric constant is important since a high permittivity for a given thickness allows to increase the transconductance, the channel mobility, and consequently R_{ON}. It also allows for a thicker dielectric layer with the same capacitance as a thinner dielectric layer with lower permittivity. The dielectric constant or

the dielectric thickness can be extracted from the dielectric capacitance:

$$\varepsilon_{Diel} = \frac{C_{ox} t_{ox}}{\varepsilon_0} \mid t_{ox} = \frac{\varepsilon_{Diel} \varepsilon_0}{C_{ox}} \tag{2.5}$$

2.2.2 I-V measurements

I-V measurements can also be performed on both MOSCAP structures. For MOS-1 devices, an ohmic contact can be created on the side contact similar to the method used for MOS-2 devices (cf. **Figure 2.4**) in order to ground it with the body. At the gate contact, a voltage sweep between 0 to 60 V is performed and the gate current is measured. *I-V* characteristics are represented in terms of the electric field in the dielectric and can be calculated as:

$$E = \frac{V_G - V_{FB}}{t_{ox}} \; or \; for \; simplicity \; E = \frac{V_G}{t_{ox}} \tag{2.6}$$

From *I-V*, the breakdown field (E_{BD}) can be extracted and used as an indicator of the dielectric reliability. It corresponds to the electric field where the dielectric has a hard breakdown and an ohmic current is observed. A large number of *I-V* characteristics for MOSCAPs on 200 mm wafers is possible, allowing to reduce the uncertainty. However, due to the limited number of structures available and the difficult body contact caused by the small coupon area, MOSCAPs on coupons presented large variability and discrepancy with *I-V* measurements. Therefore, *I-V* measurements were only considered for the MOSCAPs on 200 mm wafers.

2.2.3 Extraction of Interface states density

2.2.3.1 Conductance method

Other than impacting V_{FB}/V_{TH}, the Interface states density (D_{it}) impacts the channel mobility and consequently R_{ON}. It can be extracted through various ways with transistors and MOS capacitors. In the case of MOSCAPs, the mostly used methods are the Terman method [180] and the conductance method [181]. Both are based on the study of different elements in the MOS equivalent circuit. The Terman method is based on the analysis of the semiconductor capacitance (cf. **Figure 2.6.a)**) at high frequency with interface states capturing and emitting carriers, with a sensibility of 10^{10} $eV^{-1}.cm^{-2}$. However, this method requires a perfect knowledge of the doping and an accurate measurement of the semiconductor capacitance [178]. Moreover, in the case of GaN, the large band gap limits the generation of holes consequently limiting the extraction to D_{it} close to GaN's conduction band [182]. On the contrary, the conductance method does not require to access the semiconductor capacitance. It is based on the direct analysis of interface states through the capture/emission mechanism with a time constant $\tau_{it} = C_{it} R_{it}$ at depletion or weak inversion regimes. It can measure D_{it} in the order of 10^9 $eV^{-1}.cm^{-2}$. The equivalent circuit can be simplified as represented in **Figure 2.6.b)** with parallel capacitance (C_p) and conductance (G_p). G_p normalized by the pulsation ω is related to D_{it} by the following equations. For continuously distributed energy levels:

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1 + (\omega\tau_{it})^2\right] \tag{2.7}$$

To extract the D_{it}, G_p/ω as a function of ω for a given voltage has a maximum at $\omega_{it} \approx 2/\tau_{it}$ and the maximum value is equal to:

$$D_{it} = \frac{\alpha}{q}\left(\frac{G_p}{\omega}\right)_{max} \tag{2.8}$$

Where α is a constant, equal to 2.5 for the SiO_2/Si interface. The ω_{it} is associated with the trap energy level with respect to GaN's conduction band by the following equation:

$$E_C - E_T = kT \ln\left(\frac{2\upsilon_{th}\sigma_s N_C}{\omega_{it}}\right) \tag{2.9}$$

Where υ_{th} is the electron thermal velocity, σ_s the capture cross-section of D_{it}, and N_C the effective density of states at the GaN's conduction band edge. σ_s can be assigned to 10^{-14} cm^{-2} [117] and υ_{th} to $\sqrt{3kT/m_e}$ where m_e is the effective electron mass in GaN. To extract D_{it} as a function of $E_C - E_T$, *C-V* measurements can be performed at different frequencies and $G_p/\omega = f(\omega)$ plotted for different voltages at depletion or weak inversion. However, when *C-V* measurements are performed, the equivalent circuit is different (cf. **Figure 2.6.c)**). Considering the series resistance R_s, G_p/ω is expressed as a function of C_m and G_m as [183]:

$$\frac{G_p}{\omega} = \frac{\omega G_c C_{ox}^2}{G_c^2 + \omega^2(C_{ox} - C_c)^2} \tag{2.10}$$

Where:

$$R_s = \frac{G_{m,acc}}{G_{m,acc}^2 + \omega^2 C_{m,acc}^2} \tag{2.11}$$

$$C_c = \frac{C_m}{(1 - R_s G_m)^2 + (\omega R_s C_m)^2} \tag{2.12}$$

$$G_c = \frac{\omega^2 R_s C_m C_c - G_m}{R_s G_m - 1} \tag{2.13}$$

And where $C_{m,acc}$ and $G_{m,acc}$ are the capacitance and conductance in the accumulation regime, C_c and G_c are the corrected capacitance and conductance with respect to R_s.

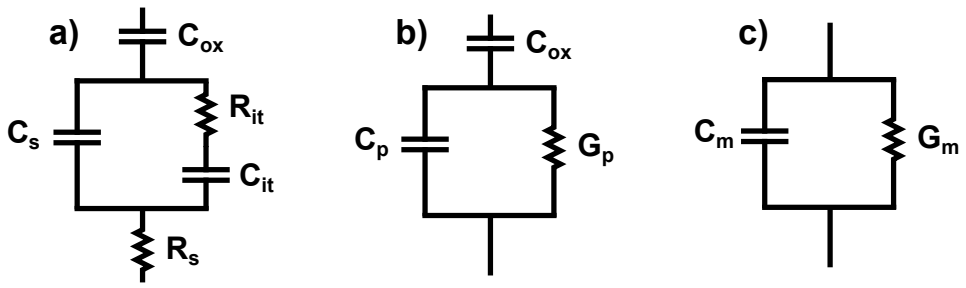


Figure 2.6: Equivalent circuit of a MOS structure: a) with R_s the sheet resistance, C_{it} and R_{it} both the capacitance and the resistance associated with interface traps, and C_s the capacitance associated with the semiconductor; b) simplified circuit with parallel capacitance (C_p) and conductance (G_p); c) circuit measured by C-V measurements.

If the conductance method is one of the most precise methods to extract D_{it}, its use in a dielectric/GaN interface can be troublesome, mostly for UID-GaN substrate. In fact, as demonstrated by Vandendaele et al. [184], this interface can present a resistive component associated with the UID-GaN substrate which

increases the extracted conductance with increasing frequency. This leads to an overestimation of D_{it} close to GaN's conduction band. For the n-GaN substrate, the extrapolation is reduced compared to the UID-GaN substrate but for high frequency, an increase in resistivity cannot be neglected. Moreover, similarly to the Terman method, only the energy levels close to the conduction band are accessible at room temperature (typically under 0.4 eV [141]).

2.2.3.2 Conductance method at different temperatures

Consequently in order to extract accurate D_{it} for dielectric/GaN interfaces, a mixed of Technology Computer Aided Design (TCAD) and analytical models can be applied. Measuring at different temperatures also increase the range of energy levels that can be analyzed. The model developed by Vandendaele et al. [184] consists of a 1D modeling of Al_2O_3/GaN stack where a total admittance (Y_{Total}) is calculated with the semiconductor capacitance, a given D_{it} population and a gate potential dependent resistance. $Y_T$otal is then used to simulate the associated C-V characteristic such as G_m/ω-V. Therefore, for a given D_{it} population, C_{ox} and doping (N_D), a abacus of D_{it} as a function of $(G_m/\omega)_{max}$ can be calculated. An example for $C_{ox} = 2.655 \times 10^{-7}$ F.cm^{-2} is represented in **Figure 2.7**.

A linear relationship between D_{it} and $(G_m/\omega)_{max}$ is observed for a low D_{it}, but with an increasing $(G_m/\omega)_{max}$, D_{it} starts to saturate due to the fact that the associated C_{it} ($= qD_{it}$) is higher than C_{ox}. Consequently, in the linear part, an experimental $(G_m/\omega)_{max}$ peak as a function of gate voltage (preferably $(G_c/\omega)_{max}$ in order to take into account R_s) can be used to extract the associated D_{it} value. Knowing D_{it}, the associated energy level can be calculated using **Equation 2.9** by replacing ω_{it} with $2\pi f$, where f is the measuring frequency. Hence for C-V measurements at room temperature or other temperatures, this abacus allows to have an idea of D_{it} at a given energy level.

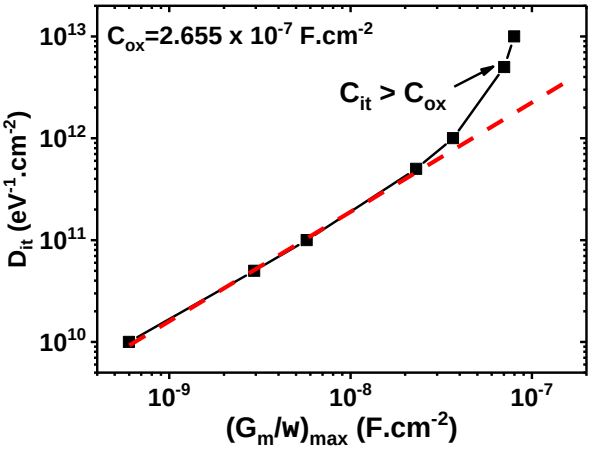


Figure 2.7: D_{it} abacus as a function of the maximum of G_m/ω for $C_{ox} = 2.655 \times 10^{-7}$ F.cm^{-2}.

To have a large $E_C - E_T$ range, the C-V measurements can be performed between 20 K and 500 K. This allows to scan between 0.02 to 0.86 eV below GaN's conduction band (E_c) with f = 1 kHz. Combining different temperatures with different frequencies allows to check if the extraction is valid. Indeed, $E_C - E_T$ can be accessed by different couples of T/f. If a discrepancy is observed by combining different measuring temperatures and frequencies, the analysis is not entirely accurate.

To reach deeper levels up to GaN mid-gap (1.2 eV) with frequencies around 1 kHz, the temperature

needs to be raised around 925 K (652°C), which could potentially crystallize high-κ dielectrics such as Al_2O_3. Therefore, with this technique, only an upper fraction of the GaN gap can be analyzed. p-GaN substrate could potentially allow to extract D_{it} close to the valence band but the low activated free holes concentration with Mg doping hinders such analysis.

2.2.3.3 Electrochemical analysis for surfaces states

Another interesting analysis to access defects at the GaN surface before the dielectric deposition is the Electrochemical-Voltage method (ECV) based on a Mott-Schottky plot. It is based on the measurement of the depletion capacitance similarly to a Schottky contact, but instead of having a metal contact, the contact is made with an electrolyte. Primarily used to extract the semiconductor doping concentration, the Mott-Schottky plot also allows to extract a V_{FB} and barrier height $\phi_{barrier}$ which corresponds to the difference in energy between the bulk Fermi level and the surface conduction band of the semiconductor.

According to Winnerl et al. [185], [186], this $\phi_{barrier}$ can be associated with surface defects after etching with HCl. Monitoring the $\phi_{barrier}$ for different etchings with an as-grown reference surface can allow to access whether the etching creates more or less surface states. This was done by Pernel et al. [187] and the POR etching process was found to have a $\phi_{barrier}$ closer to the as-grown reference $\phi_{barrier}$. If ECV was not used in this thesis, this technique is interesting to rapidly access the surface states before dielectric deposition and without MOSCAPs. Moreover, an interesting perspective would be to access deeper interface states with a thin dielectric/GaN stack thanks to lower frequency measurements but further work needs to be done to achieve this measurement.

2.2.4 Other analyses

2.2.4.1 Mobility extraction by R_{ON} partitioning at different gate voltages

As described in **Section 1.4.1**, the gate has a gate bottom region composed by a c-plane GaN and the gate sidewalls regions with polar or semi-polar plans (cf. **Figure 1.5,c)**). Each region has its own contribution to the MOSc-HEMT performances in terms of V_{TH}, R_{ON}, and electron mobility at the gate channel [46]. Specifically for R_{ON}, the contribution of each region can be calculated with a MOSc-HEMT by a method called R_{ON} partitioning thanks to GaNG transistors since they have different gate length transistors (cf. **Figure 2.8**) [45], [188]:

$$R_{ON} = 2R_c + R_{2DEG,S+D} + 2R_t + R_{channel} \tag{2.14}$$

Where $2R_c$ is the contact resistance measured with the Transmission Line Method (TLM) structures [189]. $R_{2DEG,S+D}$ is the 2DEG resistance, equaled to $R_{sh,2DEG} \times L_{GD}L_{GS}$ where $R_{sh,2DEG}$ is measured with Van der Pauw structures [190] and L_{GD}/L_{GS} are respectively the gate-drain and gate-source length. $R_{channel}$ and R_t are the bottom and the sidewall resistances respectively. Both resistances are extracted by plotting R_{ON} at a given V_G for different gate lengths (cf. **Figure 2.8**). The slope directly gives the channel sheet resistance $R_{sh,chan}$ ($R_{channel} = R_{sh,chan} \times L_G$). The intercept ($R_{intercept}$) is related to R_t and is

equal to:

$$R_{intercept} = 2R_c + R_{2DEG,S+D} + 2R_t \Rightarrow R_t = \frac{R_{intercept} - R_{2DEG,S+D} - 2R_c}{2} \tag{2.15}$$

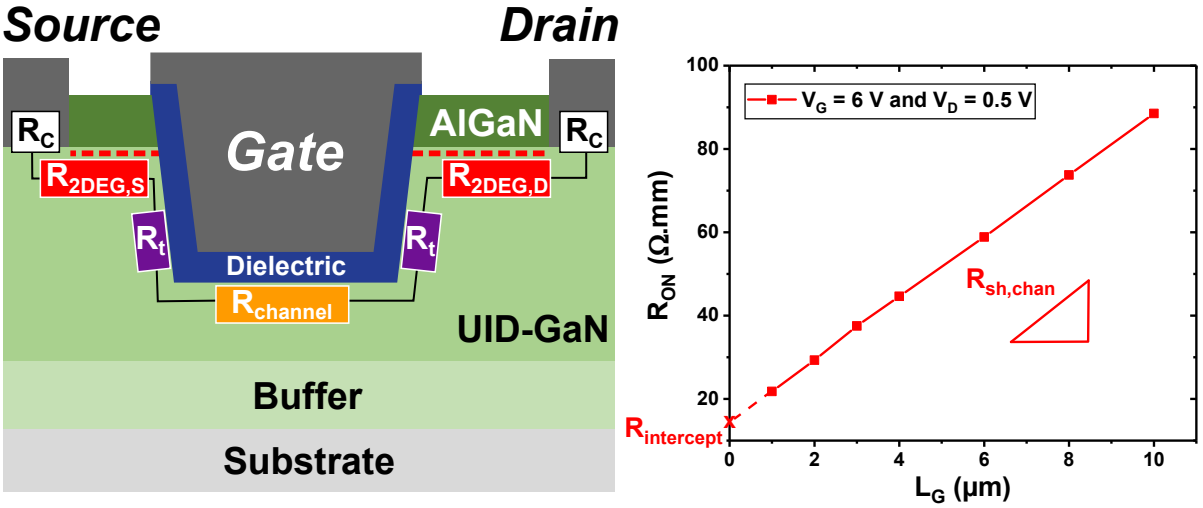


Figure 2.8: On the left, a schematic representation of the different resistances contributing to R_{ON} for a MOSc-HEMT; on the right, R_{ON} for different corrected gate lengths for V_G = 6 V. The slope of the curve gives the channel sheet resistance $R_{sh,chan}$ and the intercept gives a $R_{intercept}$ related to R_t.

As described in **Section 1.4.1.3**, since the gate bottom length is not equal to the top CD, the corrected bottom L_G is used in the $R_{ON}(L_G)$ plot. Having defined the contribution of each gate region on R_{ON}, the recent work of C. Piotrowicz [46] has demonstrated that the use of R_{ON} partitioning is relevant to evaluate the mobility contribution of each gate region. It consists in extracting $R_{channel}$ and R_t at different V_G from $R_{ON}(L_G)$ for different V_G. The electron density $N_{channel}(V_G)$ is then extracted by *C-V* measurements with a 200 µm gated Van der Pauw structure representing the gate bottom region. Assuming that $N_{channel}(V_G)$ is uniform across the gate cavity, the mobility associated with the gate bottom (μ_{bot}) and the sidewall regions (μ_{sw}) can be calculated with $R_{channel}(V_G)$ and $R_t(V_G)$ [46]:

$$\mu_{bot} = \frac{1}{qN_{channel}(V_G)R_{sh,chan}(V_G)} \quad | \quad \mu_{sw} = \frac{L_{sw}}{qN_{channel}(V_G)R_t(V_G)} \tag{2.16}$$

Where L_{sw} is the sidewall length calculated from the sidewall angle and the recess depth.

2.2.4.2 Bias-Temperature Stress

Mobile charges described in **Section 2.2.1.2** can be measured by Bias-Temperature Stress (BTS) measurements with *C-V*. Since mobile ions have an enhanced drift at elevated temperatures, the sample is heated at 200°C and the gate is stressed at an electric field lower than 1 MV.cm^{-1} for a given time (here 10 min). This step allows the mobile charges to drift while limiting electron trapping in the dielectric. After the given time, the stress is maintained to fix the mobile charges, and the temperature is lowered to room temperature. A *C-V* characteristic is then performed and V_{FB} is extracted. The procedure is then repeated by stressing the gate with the opposite bias. The total procedure is summarized in **Figure 2.9**. By considering that the mobile charges can be expressed as sheet charges, the difference in V_{FB} between the two stresses gives the density of mobile charges [178]:

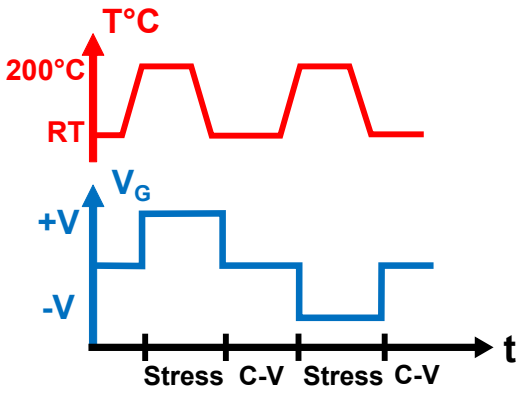


Figure 2.9: Schematic representation of the BTS measurement procedure.

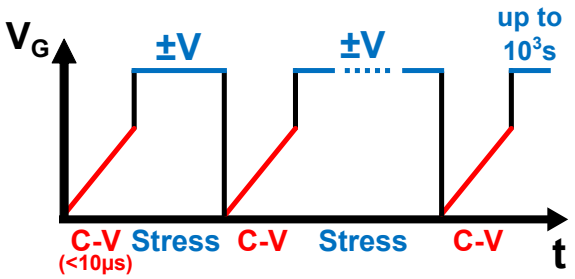
$$N_{mob.} = \frac{-C_{ox}\left(V_{FB}^{+} - V_{FB}^{-}\right)}{q} \tag{2.17}$$

Where V_{FB}^{+} and V_{FB}^{-} are the extracted flat band voltages after the positive and negative bias respectively.

2.2.4.3 Measurement-Stress-Measurement method

In terms of reliability, the use of ΔV_{FB} can be limited due to the fact that the hysteresis depends on the sweep rate (which is slow for *C-V*), the sweep direction, and the voltage range. Moreover, fast traps that could affect the MOSc-HEMT are difficult to characterize in this configuration. However, the Measure-Stress-Measure (MSM) method is a method allowing the characterization of fast traps in the Dielectric/GaN gate stack while ensuring stable stress conditions.

It consists in sequences of measurements and stress steps. The stress is maintained for a given time and then a fast measurement is performed (<10 µs) to not affect the stress conditions, and finally the stress is applied again for a given time (cf. **Figure 2.10**). In the case of *C-V* measurements, in order to have a fast acquisition, the gate current I_G is measured instead after the fast gate voltage ramp [191]. I_G is composed of the leakage current $I_{leak.}$ and the displacement current $I_{disp.}$. With a dielectric thick enough (<15 nm), the leakage current can be considered negligible and I_G equal to $I_{disp.}$. With $I_{disp.}$, it is possible to obtain the gate capacitance as:



$$I_G \approx I_{dis.} = C\frac{dV}{dt} \Rightarrow C = \frac{I_{dis.}}{dV/dt} \tag{2.18}$$

Figure 2.10: Schematic representation of the MSM measurement procedure.

Where dV/dt is the voltage ramp applied at the gate. The measurements are made with an Agilent B1500 by using a Wave Generator / Fast Measurement Unit (WGFMU). Two contacts are used, the gate contact and the side/ohmic contact of the MOSCAP.

2.3 Physical-chemical analyses

With mostly samples but also with some MOSCAPs, different physical-chemical characterizations were used to characterize the gate stack and the Dielectric/GaN interface. In this section, the different techniques used in this thesis will be presented and discussed.

2.3.1 X-Ray Photoelectron Spectroscopy (XPS) and Hard X-Ray Photoelectron Spectroscopy (HAXPES)

2.3.1.1 Principle and equipment

X-ray Photoelectron Spectroscopy (XPS) is a characterization technique sensible to the surface and interface chemical composition, environment, and surface band structure. It is based on the analysis of photoelectrons generated after excitation by an X-ray beam. When an X-ray photon interacts with an atom, if the photon energy (hν) is higher than the electron binding energy (BE) of a core level, the electron can absorb the photon energy and be ejected, as represented in **Figure 2.11**.

Alongside this photoelectric effect, the Auger effect can also occur. As represented in **Figure 2.11**, when the electron of a deeper level is ejected, the atom is ionized and in an excited state. To stabilize it, an upper electron can fill the generated hole. The excess of energy is either evacuated by an X-ray photon (i.e. X-ray Fluorescence) or by a second ejected electron, the Auger electron.

The generated photoelectron can be collected, and its kinetic energy (KE) analyzed. Since there is no energy loss during this process, the photoelectron binding energy can be deduced from the kinetic energy as follows:

$$BE = h\nu - KE - \phi_{Spectr.} \tag{2.19}$$

Where $\phi_{Spectr.}$ is the calibrated work function of the spectrometer. The spectrometer work function is measured with a clean Cu reference sample in order to set the reference level to the Fermi level (i.e. the zero in the energy scale corresponds to the Fermi level). As represented in **Figure 2.12**, an XPS spectrum is characterized by photoelectric peaks measured at specific binding energies and Auger lines.

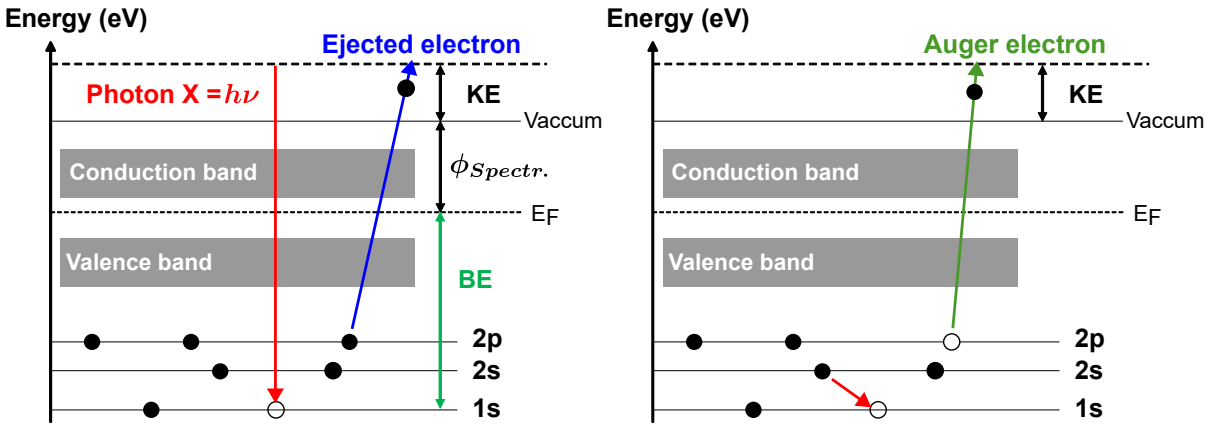


Figure 2.11: On the left, the XPS principle based on the photoelectric effect; on the right, the Auger effect. Based on [192].

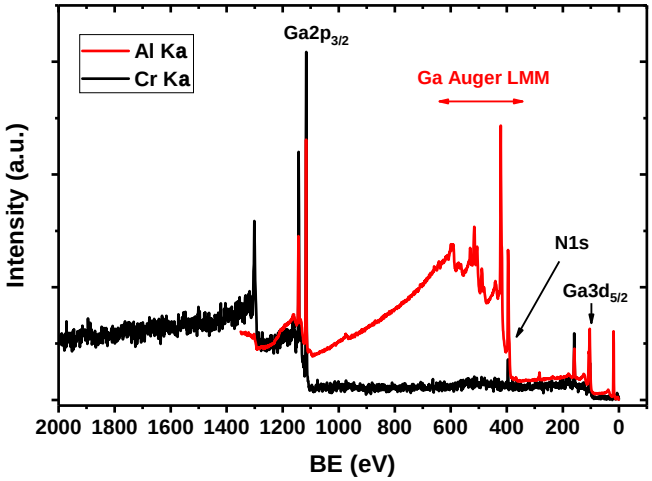


Figure 2.12: XPS survey spectrum on as-grown GaN for the Al and Cr Kα sources.

A typical XPS setup is represented in **Figure 2.13**. It is composed of an x-ray source, a monochromator, a hemispherical energy analyzer with a characteristic pass energy, and a detector. Measurements are performed under ultra-high vacuum (UHV) (P $\simeq 10^{-9}$ mbar). Different X-ray sources are possible. The typical X-ray source is Al Kα (h$\nu = 1486.7$ eV), but higher energy sources such as Cr Kα (h$\nu = 5414.7$ eV) exist. The use of high X-ray energy sources is denominated Hard X-ray Photoelectron Spectroscopy (HAXPES). Historically linked to synchrotron facilities, the commercialization of laboratory HAXPES has increased the accessibility of this technique [193]. HAXPES presents some advantages with respect to standard XPS, such as a higher probing depth (from 10 to 30 nm) and, in the case of GaN, the shift to higher energies of Ga Auger lines coinciding with the N1s spectrum with XPS (cf. **Figure 2.12**). One of the XPS systems used in this thesis was a PHI Quantes equipped with both Al Kα and Cr Kα X-ray sources. Parallel Angle-Resolved X-ray Photoelectron Spectroscopy (pAR-XPS) is another XPS related technique used in this thesis. Measurements were done with a customized Thermo Fisher Scientific Theta 300 instrument with an Al Kα X-ray source. Compared to XPS, pAR-XPS allows collecting different take-off angles at the same time with a large angle collecting magnetic lens and a 2D electron detector.

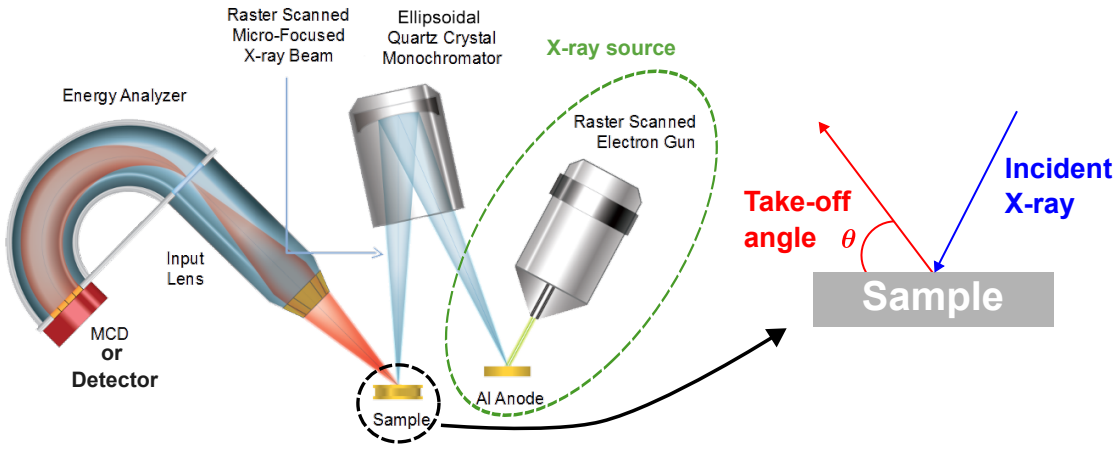


Figure 2.13: Different components of a XPS equipment, here the energy source is an Al Kα source, based on [194].

2.3.1.2 Chemical analyses on dielectric/GaN stack

Since each atom has specific binding energies linked to electronic core levels (e.g. 1s, 2s, $2p_{3/2}$, $3d_{5/2}$ ...), XPS can be used to identify chemical species. The binding energy is also influenced by the chemical environment. For instance, for electronegative bonds such as oxygen bonds, the binding energy tends to increase since more energy is needed to eject electrons engaged in these bonds [195]. Consequently, XPS is also a powerful tool to study chemical environments.

For aluminium-based oxides, the used spectra are O1s and either Al2p or Al1s for respectively Al or Cr Kα sources. For GaN, the used spectra are Ga3d and $Ga2p_{3/2}$, with $Ga2p_{3/2}$ being more surface sensitive than Ga3d. However, the photoelectric scattering cross-section (σ_i) representing the probability of a photoelectron for a given binding energy being ejected with a given X-ray energy source is strongly reduced for Ga3d for a high X-ray energy [196]. Therefore, the $Ga2p_{3/2}$ spectrum is preferred in HAXPES.

Fitting models for XPS spectra are used to decompose the different binding states contributions. An XPS peak has mainly three major parameters: the lineshape expressed by a Gaussian/Lorentzian ratio (G/L), the Full Width at Half Maximum (FWHM), and the binding energy. In order to compare different samples and because of small differences between the $Ga2p_{3/2}$ peaks, a model with fixed binding energy differences between the components was used. The different components for $Ga2p_{3/2}$ were defined with both literature and reference samples. For instance, the FWHM and G/L were defined according to the nature of the bonds [197]. Finally, the chemical shift between Ga-N and Ga-O bonds was set according to the difference between the Ga-O bond of a Ga_2O_3 sample and the Ga-N bond of a GaN sample [198]. The parameters for $Ga2p_{3/2}$ are summarized in the table below.

Parameter	$Ga2p_{3/2}$			O1s	
	Ga-N	Ga-O	Ga-Ga	O-Al	Al-O-H
G/L (%)	80	100	40	100	100
FWHM (eV)	1.5 ± 0.1	≤ 2.6	≤ 2.6	≤ 2.6	≤ 2.6
Binding energy (eV)	/	$BE_{Ga-N} + 0.7$ [198]	$BE_{Ga-N} - 1.3$ [199], [200]	/	$BE_{Al-O} + 1.2$ [199]–[201]

Table 2.3: Fitting parameters for $Ga2p_{3/2}$ and O1s spectra. The G/L and FWHM were defined according to the nature of the bonds [197].

2.3.1.3 Analysis Depth and HAXPES

As described before, XPS is a surface technique since most of the signal comes from a few nanometers (i.e. 3$\sim$5 nm). The XPS intensity coming from a given thickness t follows the Beer-Lambert relationship:

$$I = I_0 \exp\left(-\frac{t}{\lambda_i \sin(\theta)}\right) \tag{2.20}$$

Where I_0 is the intensity at the surface, λ_i the photoelectron Inelastic Mean Free-Path (IMFP) for a given kinetic energy, and θ the take-off angle. From **Equation 2.20**, the Information Depth (ID), i.e. the depth in which useful information is obtained, can be defined as the thickness where the signal at the surface

drops by a given percentage such as 95%:

$$ID = \lambda_i \sin(\theta) \ln\left(\frac{1}{1-(95/100))}\right) \simeq 3\lambda_i \sin(\theta) \tag{2.21}$$

ID depends on the IMFP and thus on the photoelectron kinetic energy, which in turn is correlated to the energy of the X-ray source. Now considering a dielectric/GaN interface, the ID needs to take into account the dielectric thickness (t_{Diel}) and the IMFP in this dielectric ($\lambda_{i,Diel}$). Since the refraction index at dielectric/GaN interface for X-ray is close to one [202], from **Equation 2.20** the intensity at a given depth in GaN (t_{GaN}) is:

$$I_{GaN} = I_0 \exp\left(-\frac{t_{Diel}}{\lambda_{i,Diel}\sin(\theta)}\right) \exp\left(-\frac{t_{GaN}}{\lambda_{i,GaN}\sin(\theta)}\right) \tag{2.22}$$

The information depth in GaN for a drop of 95% of signal at the dielectric surface for the Dielectric/GaN stack can then be calculated as follows:

$$\exp\left(-\frac{t_{Diel}}{\lambda_{i,Diel}\sin(\theta)}\right) \times \exp\left(-\frac{ID_{GaN}}{\lambda_{i,GaN}\sin(\theta)}\right) = 1 - 0.95 \tag{2.23}$$

$$ID_{GaN} = \lambda_{i,GaN}\sin(\theta)\ln\left(\frac{1}{1-(95/100))}\right) - \frac{\lambda_{i,GaN}t_{Diel}}{\lambda_{i,Diel}} \tag{2.24}$$

As represented in **Figure 2.14.a)**, with an Al Kα source, the information depth in GaN for an Al_2O_3/GaN stack is under 2 nm with an Al_2O_3 thickness between 2 to 5 nm, and this for $Ga2p_{3/2}$ and Ga3d spectra respectively. With HAXPES, deeper interfaces can be studied with a dielectric thickness higher than 5 nm (cf. **Figure 2.14.b)**). Hence, it enables to have a dielectric thickness closer to the Al_2O_3 thickness used in the MOSc-HEMT gate (i.e. 30 nm). Such advantage will be discussed in the next section.

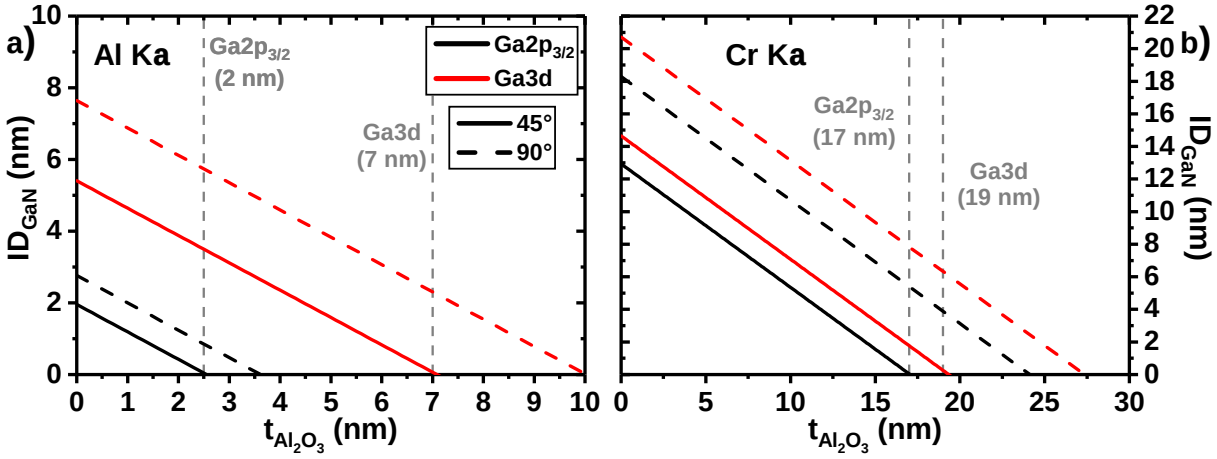


Figure 2.14: ID(P=95%) in GaN for commonly used Ga core levels as a function of Al_2O_3 deposited thickness for a) Al Kα and b) Cr Kα X-ray sources.

2.3.1.4 Advantage of HAXPES over XPS: analysis of burried interfacial gallium oxide

As described in the previous section, the analysis depth for XPS is significantly lower than HAXPES, requiring a dielectric thickness lower than 5 nm for the Dielectric/GaN interface analysis. To avoid the study of thin dielectrics, the use of HAXPES was preferred in this work. In order to find an adequate

dielectric thickness for HAXPES, the presence of Ga-O bonds in the $Ga2p_{3/2}$ spectra for increasing Al_2O_3 thickness (3 to 20 nm) is represented in **Figure 2.15**. It reveals an increasing Ga-O contribution with dielectric thickness seemingly confirming an increasing interface oxidation with a thicker dielectric. This is contrary to the results reported by Duan et al. [203] in which the GaO_x is stabilized after dielectric deposition. However the thickest dielectric layer analyzed was 5 nm thick. Another possibility for the increased Ga-O contribution is the lower sampling depth in GaN with higher dielectric thickness. However, a ToF-SIMS study performed in our group also highlights an increasing GaO_x with thicker dielectric layer [204]. Therefore, HAXPES is an appropriate technique for buried interfaces compared to XPS.

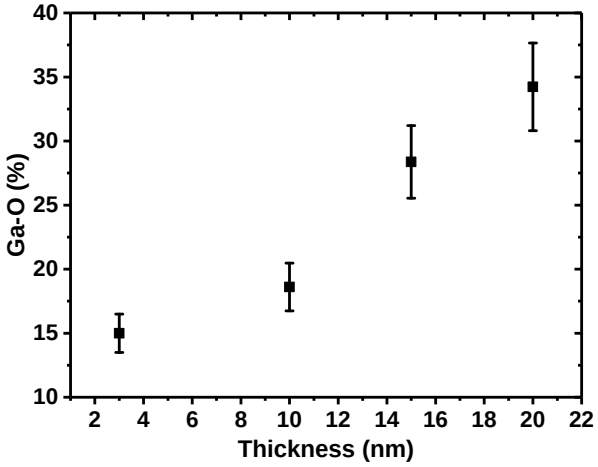


Figure 2.15: Ga-O% extracted from $Ga2p_{3/2}$ using HAXPES at the take-off angle equal to 45°, for different Al_2O_3 thicknesses deposited on etched GaN

2.3.1.5 Binding energy calibration: an issue for HAXPES

During XPS analysis on insulating materials and wide band gap semiconductors, the photoelectric effect leaves positive charges that cannot be evacuated by the material. The positive charges will then slow down the subsequent photoelectrons, increasing their associated binding energies, with a potential distortion of the spectrum. To compensate for the charging effect, a flux of electrons called a "flood gun" is used during the analysis. Nonetheless, it is common to obtain a shift of the spectrum towards lower binding energies due to an overcompensation. To calibrate the binding energies when using the flood gun, the advantageous carbon C1s position originating from surface contamination is used (i.e. 284.8 eV) [205]. If this technique is useful for Al Kα sources, the high probing depth of HAXPES and the decreased photoelectron cross sections reduce strongly the C1s signal, rendering difficult this technique. Therefore, other solutions need to be employed.

One interesting solution is the use of O KLL auger electrons. Since their shift between XPS and HAXPES depends on the energy source differences, it is possible to calibrate the O KLL in XPS with the C1s and then use the position of O KLL in HAXPES as a reference and take into account the energy source differences [206]. This method can be performed in the PHI-Quantes but is troublesome and long since the O KLL emission rate is low. Another solution is to use simply one of the spectra as a reference, such as Al1s for aluminium-based oxides, with binding energy references in the literature. The latter was the technique used in this thesis, with Al1s set at 1562 eV [207].

2.3.1.6 Quantification

Quantification is possible with XPS but only on a relative scale since some parameters such as the photon flux are difficult to know [208]. Indeed, the intensity of a spectral line is equal to:

$$A_i = JN_i\sigma_i T\lambda_i a\sin(\theta) \tag{2.25}$$

Where J is the X-ray photon flux, N_i is the atomic concentration of an element, T is the analyzer transmission function, and a is the analyzed area. We can define a quantity called Relative Sensitive Factor (RSF or S_i here), which in the case of the PHI Quantes equipment is estimated at the take-off of 54.7° (i.e. the magic angle):

$$S_i = \sigma_i T\lambda_i \tag{2.26}$$

For a different take-off angle, the RSF is corrected accordingly to a factor (f), taking into account the effect of the angle on the photoelectric cross-section:

$$S_i^{cor} = \sigma_i f \tag{2.27}$$

In order to remove the dependency on unknown parameters, the atomic concentration is hence calculated with respect to all other detected elements:

$$C_i = \frac{\frac{A_i}{S_i^{cor}}}{\sum_k \frac{A_k}{S_k^{cor}}} \times 100 \tag{2.28}$$

Where C_i is the atomic concentration relative to other detected elements. The uncertainty is around 10% for each element.

2.3.1.7 Thickness extraction (AR-HAXPES)

As presented in **Section 2.3.1.3** for a dielectric/GaN stack, the XPS intensity is modulated by the dielectric thickness and the take-off angles (cf. **Equation 2.20**). By performing angle-resolved XPS (i.e. varying θ angle), the thickness of a layer (dielectric or interfacial) can be calculated, such as the interfacial GaO_x thickness [209]:

$$\ln\left(1+\frac{R}{R_0}\right) = \frac{t_{layer}}{\lambda_{layer}\sin(\theta)} \tag{2.29}$$

Where:

$$R = \frac{I_{layer}}{I_{sub.}}; R_0 = \frac{I^{\infty}_{layer}}{I^{\infty}_{sub.}} \tag{2.30}$$

R is the intensity ratio between the layer signal and the substrate, and R_0 is the intensity ratio between the reference layer and the reference substrate measurements. Note that by using this two layers model, we ensure that the attenuation coefficient through the top dielectric layer is similar for both Ga_2O_3 and

GaN layers, and thus vanishes when calculating intensity ratios. For more information on this, see the **Annex A**.

The linear extrapolation between the logarithm function and the inverse of the $\sin(\theta)$ function gives a slope with the layer thickness divided by the IMFP in the layer. This technique is really interesting and fast with pAR-XPS but for thicker deposited dielectrics, Angle-Resolved Hard X-ray Photoelectron Spectroscopy (AR-HAXPES) is needed. Hence for calculating the GaO_x thickness with AR-HAXPES, R/R_0 was calculated with the Ga_2O_3 and GaN reference samples, the value being 1.1455. The IMFP for $Ga2p_{3/2}$ photoelectron through Ga_2O_3 was calculated to be equal to 5.831 nm.

2.3.1.8 Band alignments

Finally, the band alignments for a dielectric/GaN stack are available with XPS. The method is mainly based on the measurement of the Valence Band Maximum (VBM) or the variation of it, defined as the distance of the first signal onset from the Fermi level. The first parameter to be defined is the GaN Band Bending (BB). It can be accessed by two methods, one by direct measurement of VBM at the surface/interface and the other related to the Kraut method based on the measurement of a full XPS GaN spectrum [98]:

$$BB = VBM_{bulk} - VBM_{surf} = E_G^{GaN} - \phi_f - VBM_{surf} \tag{2.31}$$

$$BB = E_G^{GaN} - \phi_f - BE_i^{surf/interf} + \left(BE_i^{bulk} - VBM_{bulk}\right) \tag{2.32}$$

Where E_G^{GaN} is the GaN band gap, ϕ_f the difference between GaN's conduction band and the Fermi level, VBM_{surf} the VBM measured at the surface, $BE_i^{surf/interf}$ the BE for a spectrum of GaN either at the surface or at the interface, $BE_i^{bulk} - VBM_{bulk}$ the difference between the binding energy of the GaN spectrum and the VBM in the bulk such as in measurements at θ equal to 90°. However, in the case of the Al Kα source, this difference is not really a bulk measurement, due to the low information depth in GaN, thus introducing some possible errors. Moreover, for both methods, the extraction of VBM is associated to some uncertainties [210].

In general, as represented in **Figure 2.16.a)**, the VBM is extracted at the intersection between the extrapolated linear part of the spectrum with the baseline. However, due to XPS broadening of the valence band Density of States (DOS), the real value of VBM will be underestimated by roughly 0.4 eV [210]. That is why Kraut et al. [211] proposed to simulate the XPS broadening of the valence band DOS. This method is more precise but requires more work than the simple VBM extrapolation. Another challenge is the sampling depth. In fact, the VBM spectrum is a sum of the contributions from different sampling depths, leading to a VBM binding energy not being representative of the surface but of a sub-surface [203], [210]. This sub-surface region might also have a different BB. Nonetheless, regarding this effect related to the doping concentration, Huang et al. [210] have found only a correction of 0.09 eV for a GaN doping of 8.10^{17} cm^{-3}. Considering both challenges, VBM extraction can be troublesome but in our case, the corrections and uncertainties are lower than 0.5 eV. Therefore, both methods were used in this thesis.

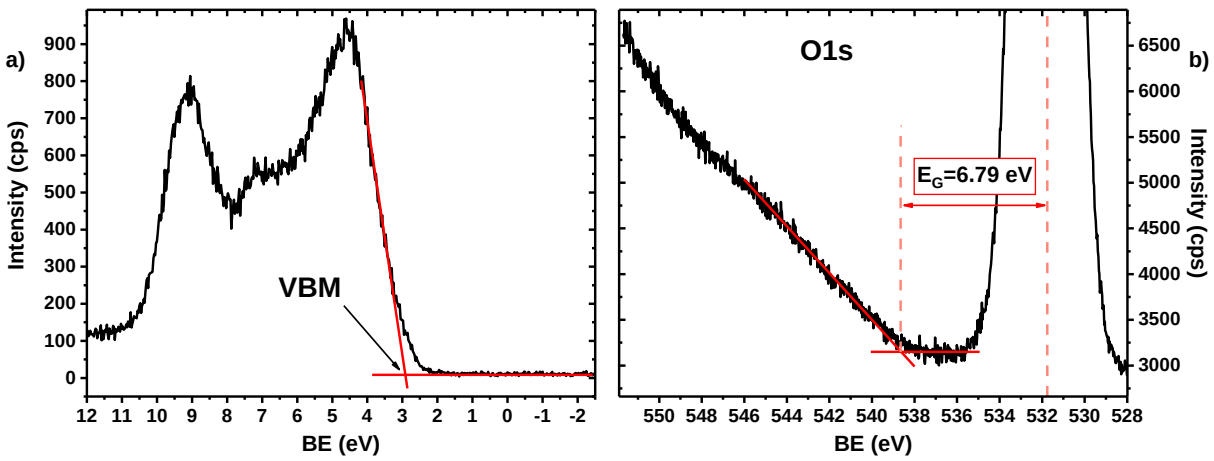


Figure 2.16: With an Al Kα source: a) VBM spectrum of etched GaN and b) O1s electron loss spectrum of ALD Al_2O_3 with the extracted band gap.

With the band bending, it is possible to calculate the net amount of charges at the interface $\sigma_{interf.}^{net}$:

$$\sigma_{interf.}^{net} = \pm\frac{\varepsilon_{GaN}}{q}\sqrt{\frac{2q}{\varepsilon_{GaN}}\left(\frac{N_C \times kT}{q}\exp\left(-\frac{q(BB+\phi_{bulk})}{kT}\right)+N_D\times(BB+\phi_{bulk})\right)+D} \tag{2.33}$$

Where ε_{GaN} is GaN's permittivity, k the Boltzmann's constant, T the temperature in Kelvin, N_D the donor doping concentration, ϕ_{bulk} the difference between GaN's conduction band and the Fermi level ($\phi_{bulk} = 0.039$ eV) and D the integration constant. For an interface free of charges, $\sigma_{interf.}^{net}$ and BB are equal to zero, allowing D to be equal to -1.12×10^{12} eV.F^{-1}.cm^{-2}. Since GaN has a spontaneous polarization induced charge of 1.8×10^{13} cm^{-2} at the interface, the added charges can be calculated as:

$$\sigma_{added} = \sigma_{interf.}^{net} + 1.8\times10^{13} \tag{2.34}$$

After defining the band bending, the Valence Band-Offset (VBO) and the Conduction Band-Offset (CBO) can be defined as:

$$VBO = VBM_{bulk}^{Diel} - VBM_{bulk}^{GaN} \tag{2.35}$$

$$CBO = E_G^{Diel} - E_G^{GaN} - VBO \tag{2.36}$$

Considering the band bending, the VBO expression can be redefined as [212]:

$$VBO = VBM_{bulk}^{Diel} - VBM_{bulk}^{GaN} + \left(BE_i^{interf} - BE_i^{bulk}\right) \tag{2.37}$$

Where BE_i^{interf} is the binding energy for a spectrum of GaN at the interface. The last parameter to extract if unknown is the dielectric band gap. For oxides, the band gap can be measured from the difference between the O1s electron loss spectrum intercept with the baseline and the O1s peak position (cf. **Figure 2.16.b**)).

Between XPS and HAXPES, XPS was used to obtain the band alignment of the Dielectric/GaN stack. Although the interfacial oxidation can be different for thicker dielectric layers, the time and the sensibility

of some spectra such as VBM is a limiting factor for HAXPES. Results concerning the band bending needs therefore to be taken with hindsight. Further results and discussion are present in **Section 3.2.2.1**.

2.3.2 Atomic Force Microscopy and Power Spectral Density

2.3.2.1 Principle

Atomic Force Microscopy (AFM) is a microscopy technique used to characterize surface topography thanks to a tip in the nanometer size. Through interactions between the tip and the surface, the cantilever deflection is recorded by a reflected laser beam on a photo-detector, ultimately recording the surface height (cf. **Figure 2.17**). In the context of studying the dielectric/GaN interface, AFM is used to characterize the roughness of the GaN surface which can affect the electron mobility under the gate and ultimately the R_{ON} of a MOSc-HEMT.

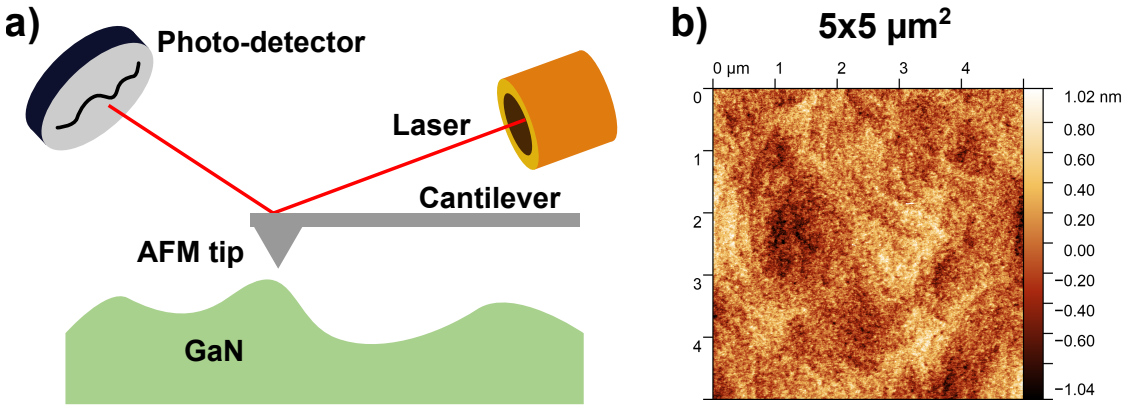


Figure 2.17: a) Schematic representation of the AFM principle, based on [213]; b) example of an AFM image on etched GaN.

There are different modes in AFM. The most commonly used in *in-line* metrology is the Tapping mode due to its fast acquisition speed. In this mode, the tip touches the surface with an oscillation close to its resonance frequency at a constant amplitude phase and distance d from the surface [214]. However, it requires a significant pre-setting step and the aging of the tip is unknown. Another mode is the Peak Force Tapping, which contrary to the tapping mode, is off-resonance [215]. The maximum interaction force is kept under 10 pF, allowing for a more resolved AFM tip. Another advantage of this mode is that the tip degradation is more easily monitored. In this thesis, for large AFM scans and *in-line* AFM, the tapping mode was used, whereas for smaller scan areas (500×500 nm^2) and *off-line* AFM, the Peak Force tapping was used.

2.3.2.2 Roughness parameters and functions

From the AFM image, Root Mean Square roughness (RMS) or Δ_{SR} can be calculated. It corresponds to the root mean square average of height deviation from the mean height value:

$$\Delta_{SR} = \sqrt{\frac{1}{NM}\sum_{n=1}^{N}\sum_{m=1}^{M}(z(n,m)-\bar{z})^2} \tag{2.38}$$

Where $\bar{z}$ is the average height, N and M are the number of pixels. Δ_{SR} is usually the parameter used to describe the roughness and its impact on surface-roughness limited mobility μ_{SR}. However, for a given Δ_{SR}, different height distributions are possible. To better describe this distribution, two functions can be used, with both being related to the autocorrelation function (ACF): the Power Spectral Density (PSD) and the Height-Height Correlation function (HHCF). The PSD describes the height distribution in spatial frequencies by applying a Fourier transform on the ACF. Initially in 2D, the function can be expressed with a 1D function as [216]:

$$PSD(k) = \frac{2\pi}{NMh} \sum_{j=0}^{M-1} |\widehat{P}_j(k)|^2 \;\; with \;\; \widehat{P}_j(k) = \frac{h}{2\pi} \sum_{n=0}^{N-1} z_{nj} \exp(-iknh) \tag{2.39}$$

Where h is the pixel dimension. The PSD is really interesting for μ_{SR} since μ_{SR} is inversely proportional to PSD. Therefore, the function in itself is interesting to have a view on the impact of roughness on μ_{SR}. The HHCF also describes the height distribution but in physical length and is instead linked to the ACF by [216]:

$$H(\tau) = \frac{1}{N(M-m)} \sum_{l=1}^{N} \sum_{n=1}^{M-m} (z_{n+m,l} - z_{n,l})^2 \tag{2.40}$$

Where $m = \tau_x/\Delta x$. From both functions, the Correlation length (Λ_{SR}) can be extracted, corresponding to the length in which there is no correlation between different heights on the surface. This parameter is also used to describe μ_{SR} as [217]–[221]:

$$\begin{aligned} \mu_{SR} &\propto \frac{1}{\Delta_{SR}^2 \Lambda_{SR}^2} \;\; for \; n_s > 1/(\pi \Lambda_{SR})^2 \\ \mu_{SR} &\propto \Lambda_{SR} \;\; for \; n_s < 1/(\pi \Lambda_{SR})^2 \end{aligned} \tag{2.41}$$

Where n_s is the electron density at the MOS channel. To extract Λ_{SR}, two models for the PSD and one model for the HHCF can be used. For PSD, we have the exponential model based on the exponential expression of the ACF and the k-correlated model [216]:

Exponential:

$$PSD(k) = \frac{\Delta_{SR}^2 \Lambda_{SR}}{\pi \left(1 + k^2 \Lambda_{SR}^2\right)} \tag{2.42}$$

k-correlated:

$$PSD(k) = \frac{\Delta_{SR}^2 \Lambda_{SR}}{\left(1 + k^2 \Lambda_{SR}^2\right)^{C/2}} \tag{2.43}$$

Where C is a fitting parameter. For HHCF, similarly to the PSD, the exponential model can be used [216]:

$$H(\tau) = 2\Delta_{SR}^2 \left[1 - \exp\left(-\frac{\tau}{\Lambda_{SR}^2}\right)\right] \tag{2.44}$$

2.3.2.3 AFM procedure

In order to obtain these functions and their fitting, the Gwyddion software was used for the analysis of AFM images. The procedure for AFM acquisition and data treatment in Gwyddion is described in **Figure 2.18**.

Different sizes of scan areas were used, ranging from 500×500 nm^2 to 5×5 μm^2. The number of pixels for each scan area was chosen accordingly in order to have a pixel size close to the tip curvature ($\backsim$4-5

nm for Tapping mode, ∽1-2 nm for Peak force tapping).

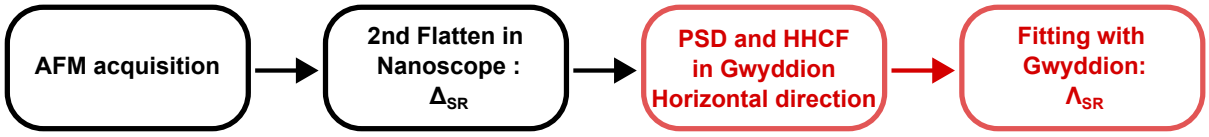


Figure 2.18: Schematic representation of the AFM procedure to extract the Δ_{SR}, the functions, and Λ_{SR}.

2.3.3 Other analyses

2.3.3.1 AES: Electron Auger Spectroscopy

Together with XPS, Auger Electron Spectroscopy (AES) is a characterization technique sensible to the surface allowing the analysis of the elements and chemical states, and their quantification [192]. As explained in **Section 2.3.1.1**, the Auger effect needs three electrons which can be influenced by the chemical bonding states. The number of Auger lines also increases with the atomic number allowing the identification of all elements except for H and He. By identifying the elements and their Auger peaks, a depth profile can be performed by sputtering the sample with an Ar^+ ion gun (at an incident energy of 500 eV) and analyzing the etched surface. Only the elements which are selected are quantified. Depth profiling with AES can be a first good approach to verify the atomic composition of a material. However, the preferential sputtering of light elements such as oxygen and the use of tabulated Relative Sensitivity Factor (RSF) that do not take into account matrix effects can lead to erroneous atomic profiles and quantification. Therefore, for quantification and depth profiling respectively, XPS and ToF-SIMS are preferable.

2.3.3.2 ToF-SIMS

Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) is a destructive surface analysis technique in which a sample is bombarded with a primary ion beam, causing the emission of secondary ions from an analysis crater, after progressive removal of the material with the sputtering beam [222]. The emission of secondary ions comes from the first or second monolayers. Thanks to an applied difference of potential (V), the secondary ions are collected and analyzed by a Time-of-Flight mass analyzer. Since the flight time in the detector depends on the ion mass, the secondary ions can be identified with their flight time and a high mass resolution. The equation linking the mass of the secondary ion and its flight time can be written as:

$$t_{ion} = L\sqrt{\frac{m}{2qV}} \tag{2.45}$$

Where, L is the length of the drift region in the mass analyzer. Contrary to magnetic SIMS where the analysis of ions is sequential, in ToF-SIMS all incoming ions are detected and analyzed in parallel. With ToF-SIMS, depth profiling is also possible. For that, a sputtering ion beam is used to create an abrasion crater ($\sim 130\ \mu m^2$) bigger than the analysis crater ($\sim 90\ \mu m^2$) (cf. **Figure 2.19**). The depth resolution is around 1 nm while the surface sensibility can be down to 1 ppm (particles per million). Thus, to

complement XPS and AES analyses, ToF-SIMS depth profiling allows to analyze the depth distribution of atoms or chemical species (such as impurities) that normally will not be detected by XPS/HAXPES.

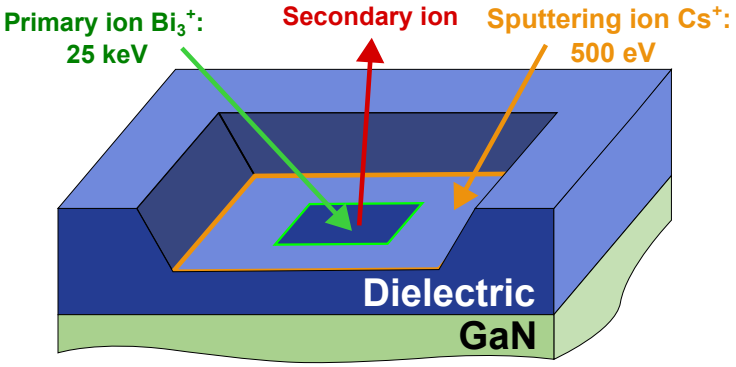


Figure 2.19: Schematic representation of the ToF-SIMS depth profiling for the Dielectric/GaN stack.

In this thesis, the primary ion beam used is Bi_3^+ with an energy of 25 keV and the sputtering ion is Cs^+ with an energy of 500 eV, all with an angle of 45°. Both negative and positive ions can be analyzed, but in the case of sputtering by Cs^+, the ion yield for electronegative element increases. For instance, chlorine or fluorine profiles can have a large intensity while the real amount of these species is negligible to other less electronegative species (i.e. Al or Ga). On the contrary, the ion yield for some species such as, H, C, and N is low. To study these species, their association between them or with O allows to increase the ion yield.

If all ions can be analyzed, quantification is only possible by using a reference for both the dielectric and the GaN substrate, where quantification is precisely known. However, relative quantification is possible by normalizing all signals by a reference signal. In the case of the Dielectric/GaN stack, the GaN^- and $^{71}Ga^+$ profiles in the bulk are used as a reference for the analysis of respectively negative and positive ions. The sputtering time where the reference signal drops by 50% is set to be the interface.

It is also important to consider the matrix effect at the Dielectric/GaN interface. In fact, due to the change of materials at the interface, the ion yield changes and can create a peak that can be considered as an artifact [223]. Nonetheless, a comparison of the peak at the interface for different samples can be used to evaluate any relative changes in the analyzed ion from one sample to another. The MCs^+ mode (M being the species associated with Cs) is also a possibility to reduce the matrix effect and verify the presence of these peaks [223].

Finally, since different ions can have the same mass, mass interferences can be a problem for some analyzed species. This is the case for GaO^- having the same mass as $CH_2^{71}Ga^-$, $GaNH_2^-$ or $^{71}GaN^-$. Thus, to analyze the gallium oxide profile, the $^{71}GaO^-$ is studied instead.

2.3.3.3 TEM/EDX

Transmission Electron Microscopy (TEM) is a technique allowing to image complex structures at the nanometric scale. The sample being thinned by a Focused Ion-Beam (FIB) is analyzed by an electron beam transmitted through the sample. The transmitted electrons are then collected and an image is obtained [224]. During the acquisition, secondary electrons can be emitted by the sample leaving empty core levels. The recombination between valence electrons and these empty levels produces x-rays, which

can be analyzed by Energy-dispersive X-ray spectroscopy (EDX) to obtain chemical information on the sample.

For the study of the Dielectric/GaN stack and interface, both TEM and EDX are helpful in identifying the presence of interfacial layers, crystallized regions, the deposited dielectric thickness, and controlling the atomic distribution in the stack. However, at high incident energy (300 keV), the electron beam tends to crystallize aluminium oxides [225]–[227]. This *in-situ* crystallization makes the EDX analysis unreliable. Therefore, special care needs to be taken while acquiring the image. One way to confirm the presence of crystallized regions at the aluminium oxide is to acquire an image with a larger field of view.

2.3.3.4 GIXRD

In the scope of structural analysis, Grazing Incidence X-ray Diffraction (GIXRD) is a characterization technique used to characterize thin deposited layers. Using the principle of X-Ray diffraction (XRD), a small incident X-ray angle (α) with the sample is kept in order to increase the path of X-rays in the thin layer. This increases the structural information obtained from the thin layer with X-ray diffraction patterns. The diffractogram is recorded by moving the detector along the 2θ circle, 2θ being the angle between the diffracted X-rays and the sample [228]. In the case of the Dielectric/GaN stack, GIXRD was used to identify signs of dielectric crystallization after annealing. However, the absence of peaks does not allow ultimately to conclude on the absence of crystallization. TEM imaging is then interesting to confirm the GIXRD analysis. In this thesis, α was kept at 2° [229].

2.3.3.5 FTIR

Finally, Fourier Transformed Infrared Spectroscopy (FTIR) is a complementary technique used in this thesis to detect hydroxyl groups (-OH). It is based on the absorption of infrared photons by chemical bonds at their specific vibration modes. This absorption can be represented as peaks of absorbance as a function of wavelength [230]. For instance, for -OH groups, the peaks appear at around 3500 cm^{-1}. The analysis of thin films can be enhanced by the use of multiple internal reflections (MIR). The idea is to trap infrared photons in the layer by using two prisms as represented in **Figure 2.20**.

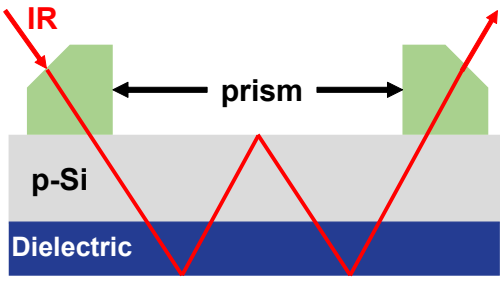


Figure 2.20: Schematic representation of the MIR-FTIR for the Dielectric/Si stack.

The multiple reflections in the layer consequently increase the analysis sensibility. However, the usual Dielectric/GaN stack can't be analyzed due to the presence of multiple layers in the GaN buffer interfering with the infrared photons. Thus, to study the presence of -OH groups in the dielectric layer, the latter had to be deposited on a silicon substrate. The signal substrate was measured and removed from the Dielectric/Si signal thanks to a reference silicon substrate.

2.4 Conclusion of this chapter

The different characterization techniques used in this PhD project were presented, based on the comparison between electrical and physical-chemical characterizations. For electrical characterization, MOS capacitors were fabricated and analyzed by *C-V* and G_m/ω measurements in order to simulate the gate bottom cavity and have a first understanding on the impact of different fabrication steps. D_{it} measurements at room temperature or different temperatures were used to finely characterize the interface states. Nonetheless, the results with MOS capacitors still need to be confirmed with transistors since the gate sidewalls are not characterized. Transistors were used to measure the electron mobility.

For physical-chemical characterizations, HAXPES allows to analyze burried interfaces, allowing to simulate as far as possible the real gate stack. The PSD enables the characterization of the lateral roughness, which is absent in typical RMS value, in the idea of understanding the morphological impact of etching. Complementary but important measurements such as ToF-SIMS and TEM/GIXRD also allow to analyze the presence of impurities and the structure of the dielectric respectively.

In the next chapter, this methodology will be employed in order to study the Al_2O_3/etched GaN gate stack from etching to post-deposition annealing.

3

Study of Al_2O_3/GaN gate stack : from etching to Post-Deposition anneal

This chapter aims to present the study of the Al_2O_3/etched GaN gate stack by analyzing the impact of etching on the GaN surface and the electron mobility, and by studying the impact of the Post-Deposition Anneal (PDA). In the first section, the use of the Power Spectral Density (PSD) was evaluated to characterize the lateral GaN surface roughness. The methodology was applied to the study of different etchings and revealed no significant differences between them, indicating a limited impact of the Surface-Roughness limited mobility (μ_{SR}). This is further confirmed by extracted gate bottom mobility being not impacted by μ_{SR}. In the second section, an optimal PDA temperature is found for 500°C in which the ΔV_{FB} is minimal and V_{FB} is not further reduced. Over that PDA temperature, ΔV_{FB} increases, and an onset of crystallization happening only with the Al_2O_3/etched GaN gate stack is observed. Both the POR etching process and the optimal PDA temperature allow to have a minimal interface states density.

Contents

3.1 Characterization of the etched surface roughness

In this section, the characterization of GaN surfaces after etching will be discussed by employing AFM images and subsequent analyses in spatial wavelength in order to complete the use of Root Mean Square roughness (RMS) or Δ_{SR} in the analysis of etched GaN surfaces. In fact, a large difference in Δ_{SR} impacts the MOSc-HEMT electrical performances by increasing R_{ON} and reducing electron mobility [87], [219]. However, surfaces with similar or close Δ_{SR} can be visually different due their height distributions [231], [232] and lead to different R_{ON} and electron mobility [46]. Therefore, another parameter or function is needed alongside Δ_{SR} to characterize the etched GaN surface in order to optimize the etching process and minimize its impact on the MOSc-HEMT mobility. As described in **Section 2.3.2**, the Power Spectral Density (PSD) is a second-order statistical analysis inversely proportional to the Surface-Roughness limited mobility (μ_{SR}) and in which the Correlation length (Λ_{SR}) can be obtained to describe the lateral distribution of the roughness [231], [232]. The etched GaN surface was recently integrated into the calculation of MOSc-HEMT mobility at different temperatures by analyzing the surface with PSD [221]. However, it was not yet applied to study the etching of a GaN surface and the impact of different etching processes. In the following sections, the variability of the PSD method, the of etching on as-grown surfaces and the influence of different etchings will be discussed.

3.1.1 Experimental details

Three different AFM studies were carried out in order to :

1. Evaluate the variability of the PSD function at the same and different locations of a GaN substrate.
2. Evaluate the impact of etching by comparing as-grown and etched surfaces.
3. Use the developed methodology to study the impact of different etching processes on the GaN surface and on the MOSc-HEMT electrical parameters (R_{ON}, μ).

For the first study, an (0001) oriented n-GaN buffer layer with a Si doping concentration of 5×10^{17} cm^{-3} grown on 200 mm p-Si (111) substrates by MOCVD was etched with the Process of Reference (POR) etching process (**Q1** = ICP-RIE high bias + ALE) as described in **Section 1.4.1.3**. No strip and wet steps were performed. The AFM measurements were performed with the Fast-scan tip. 10 scans were performed on the same position (cf. point A in **Figure 3.1.a)**) and 10 scans were performed on different positions as represented in **Figure 3.1.a)**. For both types of measurements, the scan areas were 2×2 μm^2 and 5×5 μm^2.

For the second study, in order to have a physical point of reference, a 2×4 cm^2 GaN coupon was glued on a Si wafer as a support with a thermal paste (cf. **Figure 3.1.b)**). The GaN substrate is identical to the first study due to the fact that the as-grown surface of the n-GaN wafer is a GaN layer, contrary to the UID-GaN wafer used for MOSc-HEMTs where the first layer is a SiN capping layer. Two etching processes were studied: the POR etching process (**Q1** = ICP-RIE high bias + ALE) and an etching process in which the ALE step was replaced by an ICP-RIE step with lower bias (**Q2** = ICP-RIE high bias - low bias). No strip and wet steps were also performed. The AFM measurements were performed

with the Fast-scan tip, before and after etching using the corner of the coupon as a reference point. The scan areas were 1×1, 2×2 and 5×5 μm^2.

For the third study, four quarters of a UID-GaN substrate were etched with four different etching processes. The GaN buffer layer was grown by MOCVD on a 200 mm p-Si (111) substrate and was similar to the buffer layer of a MOSc-HEMT (cf. **Section 1.4.1.2**) in order to compare with roughness results with the MOSc-HEMT electrical performances. A quarter was etched thanks to Si patches covering 3/4 of the wafer (cf. **Figure 3.1.c)**). The other quarters were etched with the three other etchings by moving the Si patches. The different etching processes were :

- **Q1** = POR process (ICP-RIE + ALE)
- **Q2** = ICP-RIE high bias - low bias
- **Q3** = Confidential 1#
- **Q4** = Confidential 2#

After etching, the wafer was stripped and cleaned with a wet sequence ending with HF, in order to reproduce the MOSc-HEMT process flow. A first AFM measurement was performed with the Fast-scan tip but little difference was observed between the etchings. Therefore, to have better control of the tip degradation, the Peak Force tapping was used. The scan area was fixed to 500×500 nm^2 and five measurements were performed on each quarter. Alongside the AFM measurements, GaNG transistors described in **Section 2.1.4** were fabricated using the different etching processes to etch the AlGaN/GaN stack. With these transistors, mobilities extracted for the gate bottom region and on the gate sidewall region were estimated using the methodology explained in **Section 2.2**. For that, I_D-V_G were performed between -2 V to 6 V for gate lengths ranging from 1 to 10 µm.

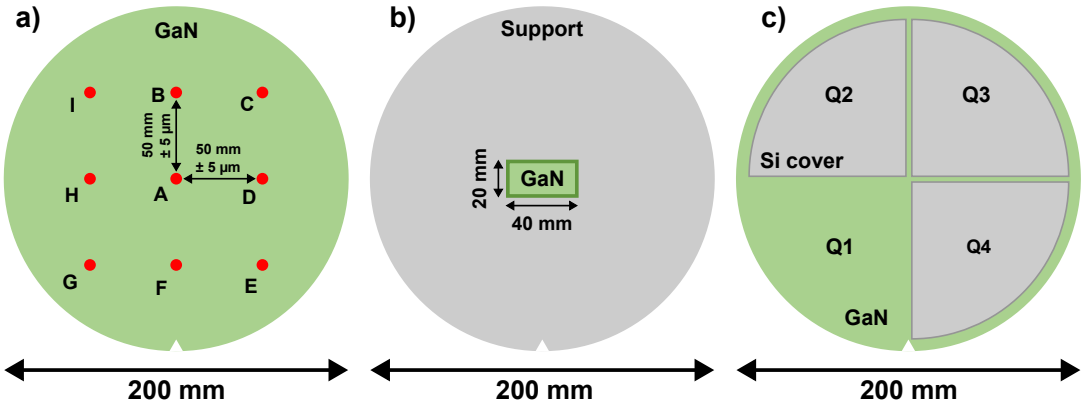


Figure 3.1: The experimental settings for a) the variability study, b) the comparison as-grown and etched, and c) the impact of different etchings.

3.1.2 Results and discussion

3.1.2.1 Variability of the PSD method

The variability of the PSD for measurements on the same area is represented in **Figure 3.2**. Little variability is observed for both scan areas. For smaller scan areas (i.e. 2×2 μm^2), the variability slightly

increases with the spatial frequency but is stable for $5 \times 5\ \mu m^2$ scan areas. The mean extracted RMS (Δ_{SR}) for the $2 \times 2\ \mu m^2$ scan area is 0.389 ± 0.005 nm and for the $5 \times 5\ \mu m^2$ scan area, it is 0.815 ± 0.001 nm.

Regarding the variability in different areas of the wafer, the PSD is represented in **Figure 3.3**. The PSD has again a variability affecting the higher frequencies for the $2 \times 2\ \mu m^2$, but the PSD is relatively stable at the different locations on the wafer for both scan areas. This could also indicate a low variability on the GaN surface after etching. The mean extracted Δ_{SR} for $2 \times 2\ \mu m^2$ is 0.316 ± 0.004 nm and 0.412 ± 0.018 nm for $5 \times 5\ \mu m^2$.

The correlation lengths (Λ_{SR}) extracted with either the K-correlated model or the exponential model are represented in **Figure 3.4** and **Table 3.1**. The variability of Λ_{SR} is small for measurements on the same location for both scan areas but increases for different locations, especially for the K-correlated model on a $2 \times 2\ \mu m^2$ scan area. Therefore, the K-correlated model seems to induce more variability on Λ_{SR}. The extracted values are around 14 nm at the same location for both models and at different locations, the length is between 18.8 and 20.3 nm. These lengths are similar to the correlation length extracted on etched GaN by Fiorenza et al. ($\sim$ 20 nm) [221], but higher than values used in mobility simulation ($\sim$ 1.5 nm) [233]. The lower Λ_{SR} in simulation can be explained by the fact that it is often used as a fitting parameter rather than a physical one. Nonetheless, if the electron density n_s is higher than $1/(\pi\Lambda_{SR})^2$ (for $\Lambda_{SR} = 20\ nm \Rightarrow n_s = 2.53 \times 10^{10}\ cm^{-2}$), the relationship between the Surface-Roughness limited mobility (μ_{SR}) and Λ_{SR} (cf. **Equation 2.41**) switches from being proportional to Λ_{SR}^{-2} to being proportional to Λ_{SR} [217], [218], [234]. Considering the obtained Λ_{SR}, this second relationship ($\mu_{SR} \propto \Lambda_{SR}$) is therefore obtained for low electron densities and can lead to different mobility values at high n_s [234].

Model	Correlation length Λ_{SR} (nm)			
	Same location		Different locations	
	$2 \times 2\ \mu m^2$	$5 \times 5\ \mu m^2$	$2 \times 2\ \mu m^2$	$5 \times 5\ \mu m^2$
Exponential	14.4 ± 0.1	14.0 ± 0.1	18.8 ± 0.8	20.3 ± 0.7
K-correlated	14.7 ± 0.3	14.2 ± 0.2	19.6 ± 1.9	17.1 ± 0.8

Table 3.1: Mean extracted correlation length Λ_{SR} for $2 \times 2\ \mu m^2$ and $5 \times 5\ \mu m^2$ scan area after multiple measurements at the same or different locations.

Comparing the two scan areas, little difference is observed both directly in the PSD function and with the extracted Λ_{SR}. Nonetheless, the lower scan area allows faster acquisition than the higher scan area if the pixel size remains close to the tip curvature ($\sim$ 4-5 nm). Consequently, in the next section, a lower scan area of $1 \times 1\ \mu m^2$ is also tested.

3.1.2.2 Comparison between as-grown and etched GaN surfaces

The difference between before and after etching for two etchings (Q1 = ICP-RIE high bias + ALE and Q2 = ICP-RIE high bias - low bias) were considered. In **Figure 3.5**, the AFM images before and after etching with the Q1 etching process are represented. Terraces and dislocation holes can be observed on as-grown surfaces while etching removes most of the terraces and induces roughness [67]. An increased

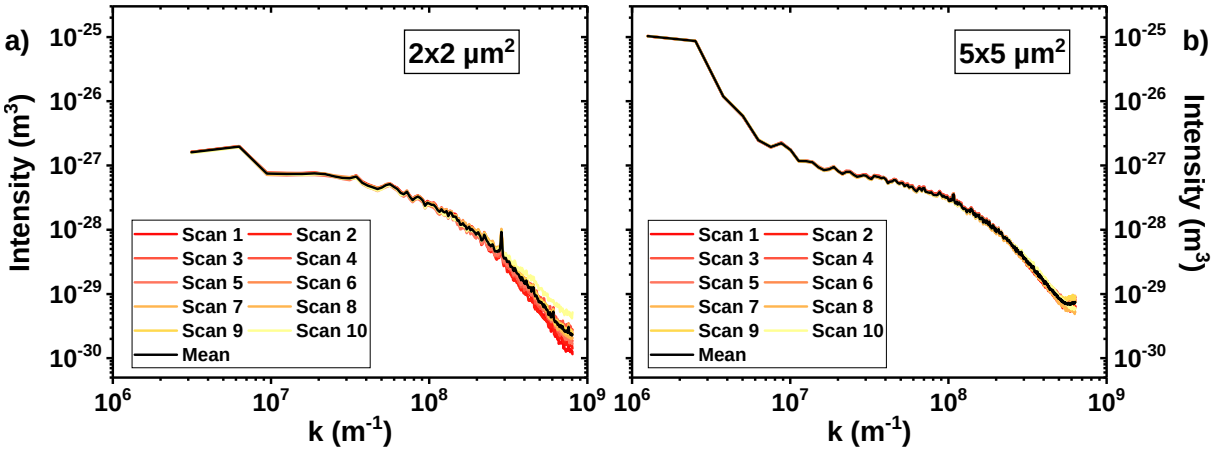


Figure 3.2: Variability of PSD for AFM measurements on the same location on the wafer.

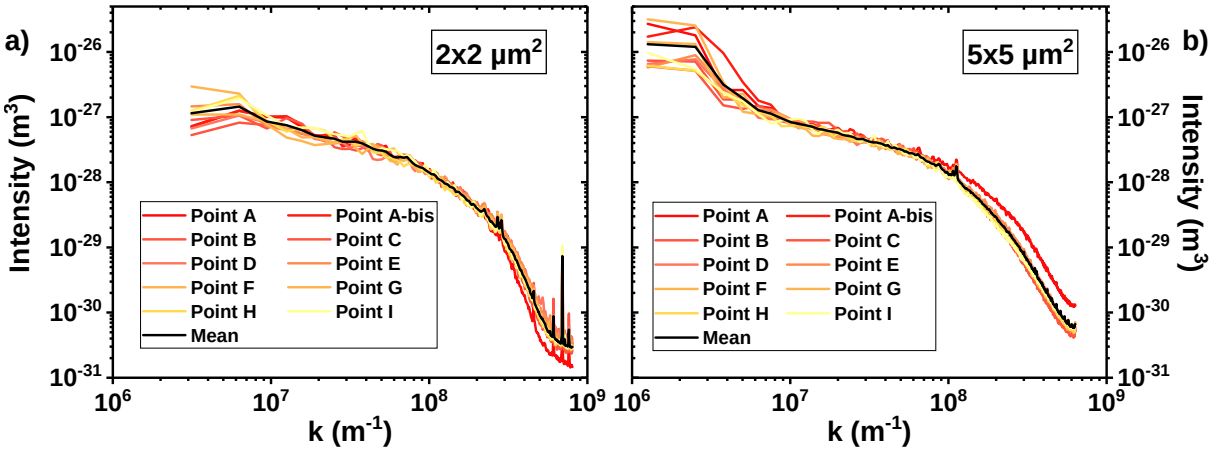


Figure 3.3: Variability of PSD for AFM measurements on different locations on the wafer.

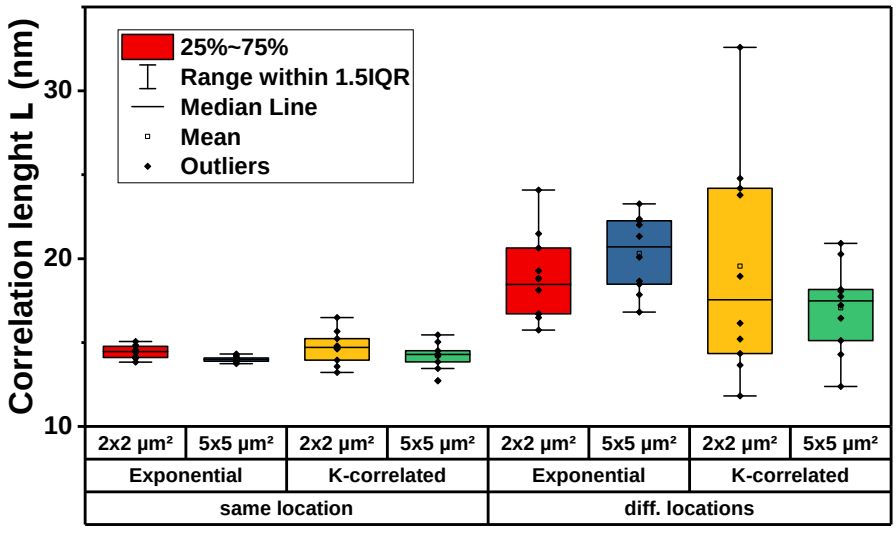


Figure 3.4: Variability of extracted correlation lengths Λ_{SR} on the same location or different locations on the wafer.

Δ_{SR} is observed after etching for both Q1 and Q2 etching processes (cf. **Table 3.2**), in agreement with results reported by He et al. [87], the difference being 0.1 nm. With μ_{SR} being proportional to Δ^{-2} [218], [234], the higher Δ_{SR} after etching can indicate a degradation of mobility. A lower Δ_{SR} is therefore important. The difference in Δ_{SR} is more predominant with a lower scan area, with a difference of around 0.1 to 0.2 nm for the 1×1 μm^2 scan area. As the scan area increases, more terraces and steps can be observed before etching (cf. **Figure 3.5**). These steps would then contribute to the Δ_{SR} extracted in larger scan areas, with even sometimes Δ_{SR} for an as-grown surface being higher than an etched surface as observed by our group [59]. Whereas on a smaller scan area, these steps are more difficult to observe and don't increase the Δ_{SR}. Therefore, to see a difference in Δ_{SR} between before and after etching, it seems important to reduce the scan area. Moreover, the small difference in Δ_{SR} (0.1 nm) seems to not properly describe the observed visual changes after etching (i.e. removed terraces). The use of PSD can help to describe these visual changes. Comparing both etchings, the Q1 process (POR etching process) has only a slightly higher Δ_{SR} than the Q2 process and it is difficult to differentiate the two etchings in terms of Δ_{SR}. Still, reducing the scan area also allows to improve the difference in Δ_{SR} between etching processes.

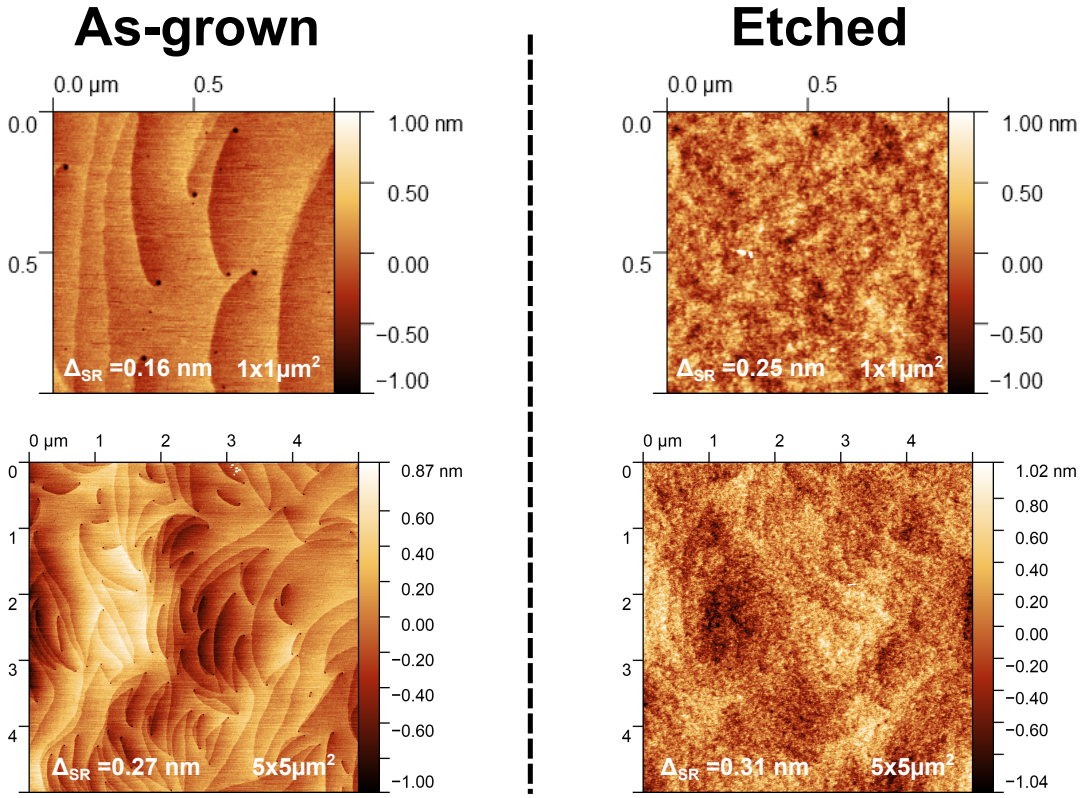


Figure 3.5: AFM images before and after etching with the Q1 process.

The PSD of 1×1 μm^2 and 5×5 μm^2 scan areas for a surface before etching and after the Q1 etching are represented in **Figure 3.6**. If the difference of Δ_{SR} can be little between as-grown and etched surfaces (<0.2 nm), the PSD allows to observe in spatial wavelength the impact of etching, as demonstrated by a large difference in PSD before and after Q1 etching process for the scan area of 5×5 μm^2, whereas the difference in Δ_{SR} is only 0.04 nm. The same observation can be made for GaN surfaces before and after the Q2 etching process. The PSD for the as-grown surface has almost a linear trend in the log-log scale.

Scan area	RMS or Δ_{SR} (nm)			
	Q1 = ICP-RIE high bias + ALE		Q2 = ICP-RIE high bias - low bias	
	Before etch	After etch	Before etch	After etch
$1 \times 1\ \mu m^2$	0.16	0.25	0.09	0.21
$2 \times 2\ \mu m^2$	0.17	0.27	0.13	0.25
$5 \times 5\ \mu m^2$	0.27	0.31	0.30	0.31

Table 3.2: RMS or Δ_{SR} for Q1 and Q2 etchings before and after etching at different scan area.

The intensity is also lower, as expected by the lower Δ_{SR} extracted before etching. On the contrary, the PSD intensity after etching increases, and a knee can be observed, related to Λ_{SR}. Since μ_{SR} is inversely proportional to the PSD [218], [233], the overall lower PSD intensity for an as-grown surface could also indicate a better μ_{SR}. By doing the difference between the PSD before and after etching for both etching processes, the PSD increases by 45∼80% after etching.

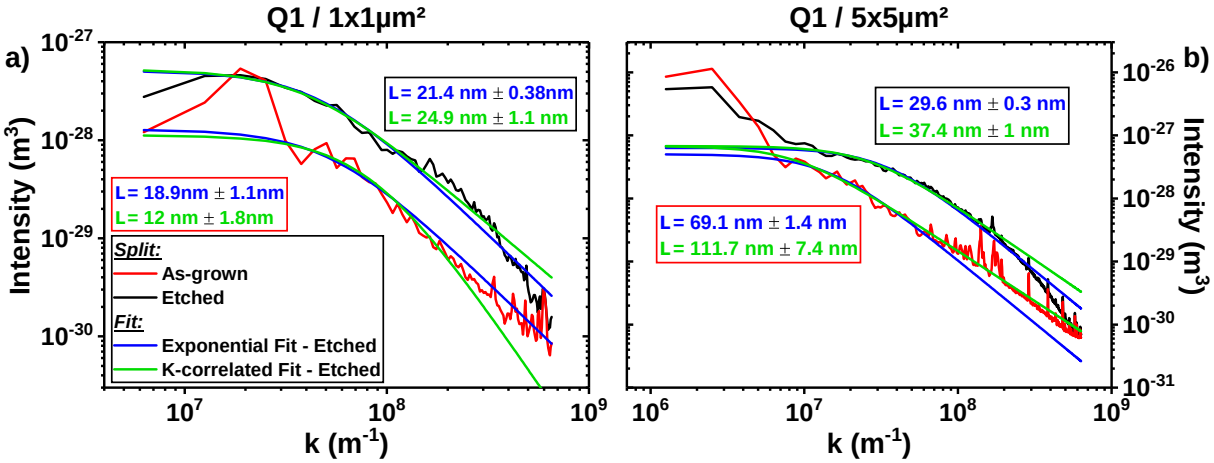


Figure 3.6: PSD before and after with the Q1 etching process on a) 1×1 and b) $5 \times 5\ \mu m^2$ scan areas, fitted with the exponential and K-correlated model.

Using both the exponential and K-correlated models, the difference in Λ_{SR} before and after etching is described in **Figure 3.7**. For higher scan areas, it is clear that Λ_{SR} is higher for as-grown surfaces and that etching reduces Λ_{SR} with the formation of the knee in PSD intensity. For $1 \times 1\ \mu m^2$, the extraction can be difficult for an as-grown surface as shown in **Figure 3.6.a)** and a Λ_{SR} close to the one extracted for etched surfaces can be obtained.

Comparing the PSD for the two etching processes (cf. **Figure 3.8**), little difference is revealed between the two etchings, especially for a $5 \times 5\ \mu m^2$ scan area. But for $1 \times 1\ \mu m^2$, Q2 reveals a lower PSD intensity similar to the lower Δ_{SR} extracted with the AFM image (0.21 vs 0.25 nm). Consequently, the PSD for Q2 could indicate a better μ_{SR}. The extracted Λ_{SR} in **Figure 3.9** also shows little difference between the two etchings. However, for all scan areas and both fitting models, the Q1 process has a higher correlation length. The relationship between correlation length and mobility will be further discussed in the next section with mobility extracted from a transistor. Consequently, in the next section, the impact of different etchings and their related mobility will be discussed.

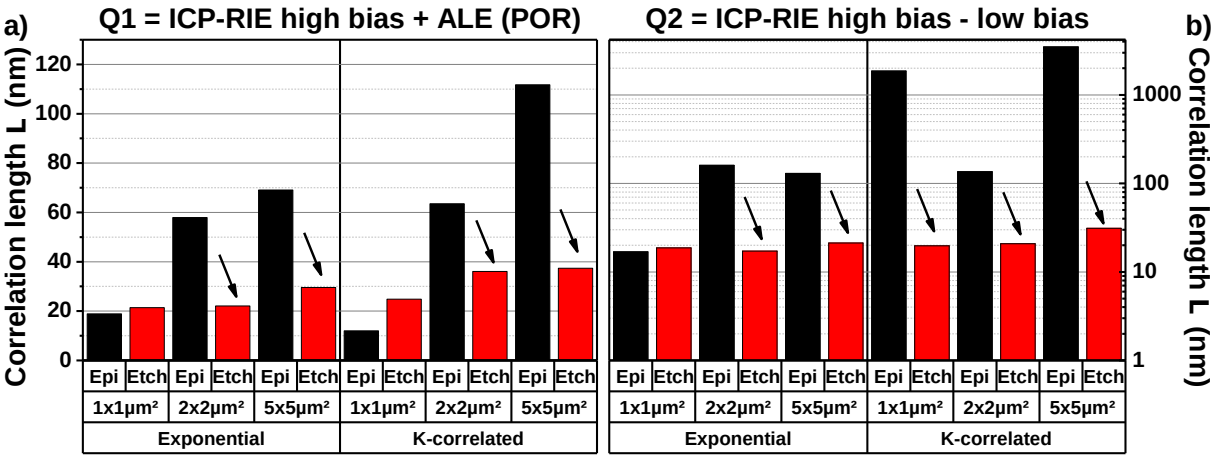


Figure 3.7: Extracted correlation length Λ_{SR} for both a) Q1 and b) Q2 etching processes, before and after etching. Both the exponential and the K-correlated model were used for the different scan areas.

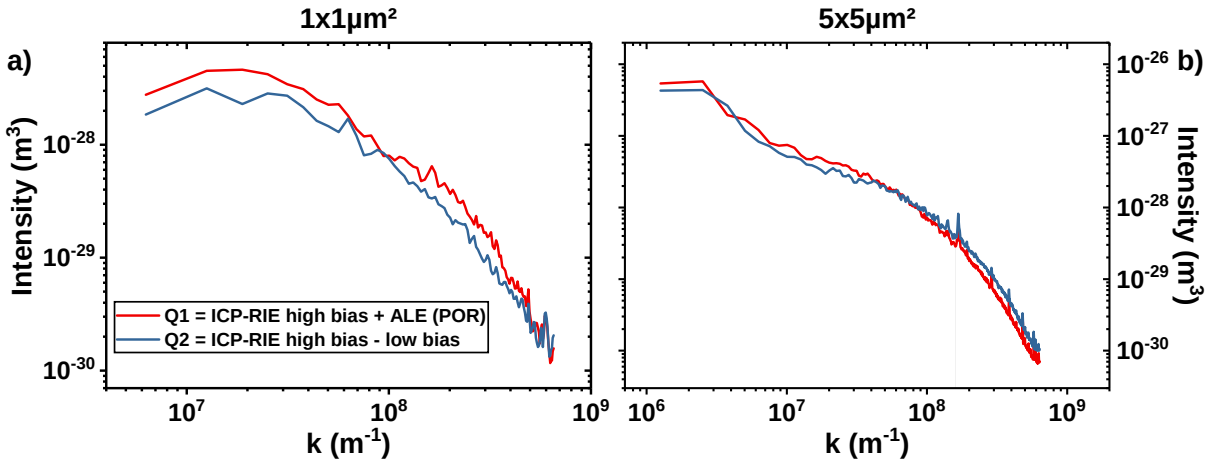


Figure 3.8: PSD after the Q1 and Q2 etching processes on a) 1×1 µ and b) 5×5 μm^2 scan areas

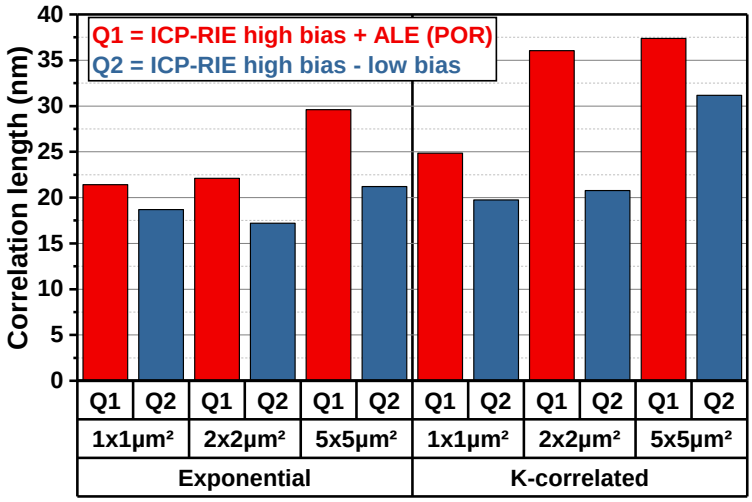


Figure 3.9: Extracted correlation lengths Λ_{SR} for both a) Q1 and b) Q2 etching processes with the exponential and the K-correlated models on different scan areas.

3.1.2.3 Impact of different etchings and comparison with mobility

Alongside the Q1 and Q2 etching processes, the Q3 (Confidential 1#) and Q4 (Confidential 2#) etching processes were also studied on quarters of a GaN wafer (**Section 3.1.1**). Since the difference between etchings was more clearly observed with lower scan areas, a scan area of 500×500 nm^2 was used. The Peak Force tapping mode was also used to have better control on the tip degradation and also have the finest possible tip. The AFM images are represented in **Figure 3.10** for a 500×500 nm^2 scan area. Visually, there is no significant difference between the different etchings. In terms of Δ_{SR}, the Q3 process presents a slightly higher value as described in **Figure 3.11**, but the difference is not striking.

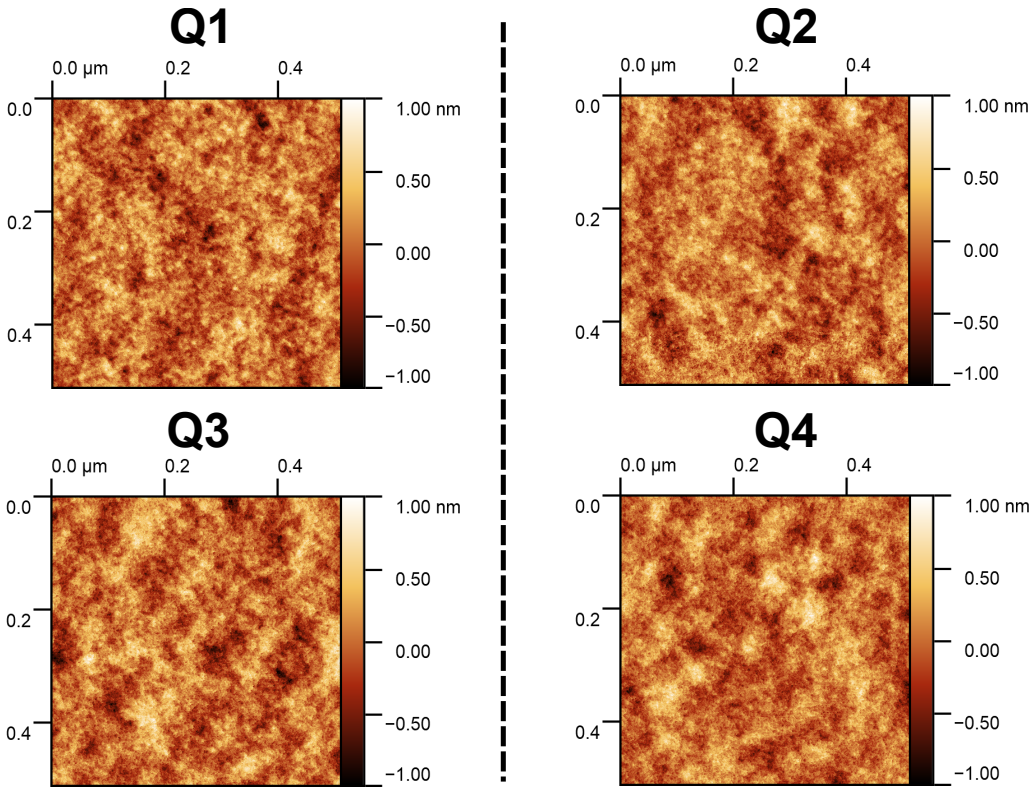


Figure 3.10: AFM images after etching with all studied etching processes.

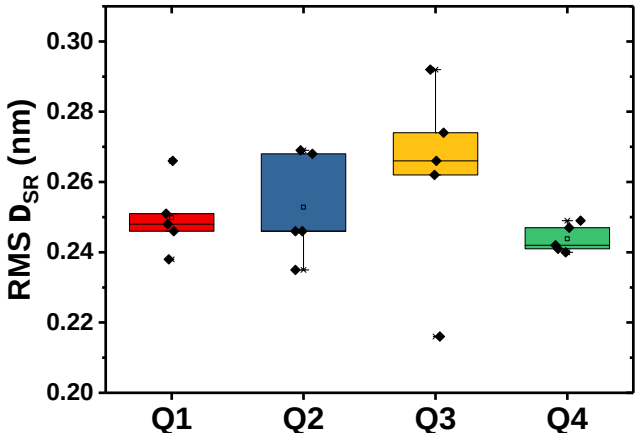


Figure 3.11: RMS Δ_{SR} directly extracted from the AFM images for the different etching processes.

With PSD, the difference is even more difficult to observe with the mean PSD for each etching having identical intensity along the spatial length (cf. **Figure 3.12.a)**). Consequently, μ_{SR} seems not to be impacted by the etching process. The Height-Height Correlation function (HHCF) was also tested to try to observe differences (cf. **Figure 3.12.b)**). In that case, again the Q3 shows a higher plateau, this result being related to Δ_{SR}. By extracting Λ_{SR} with both the PSD and HHCF described in **Figure 3.13**, it is possible to see that the K-correlated function gives lower Λ_{SR} while the exponential for PSD and HHCF gives higher Λ_{SR}. The difference could be ascribed to better fitting with the exponential model for both PSD and HHCF (cf. **Figure 3.12.c) and d)**). Considering the exponential fitting, the Δ_{SR} increases from Q1 to Q4, the values ranging between 11 to 16 nm. Again Λ_{SR} values higher than 10 nm are observed (cf. **Section 3.1.2.1**).

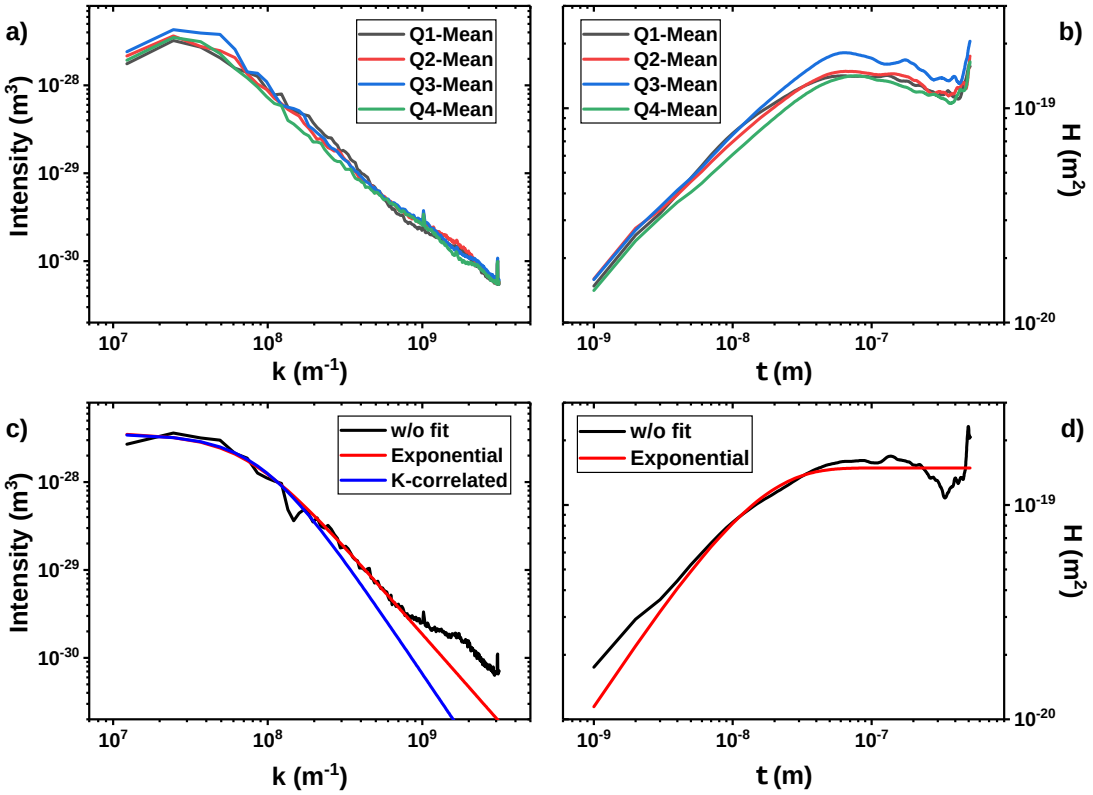


Figure 3.12: Mean a)PSD and b) HHCF for the different etching processes on a 500×500 nm^2 *scan area. Fitting of c) PSD with K-correlated and exponential models, and of d) HHCF with the exponential model.*

Taking into account both Δ_{SR} and Λ_{SR}, two ratios related to mobility can be calculated according to different definitions and assumptions. For the first ratio, μ_{SR} is proportional to $1/(\Delta_{SR} \times \Lambda_{SR})^2$ (cf. **Equation 2.41**) [217]–[220]. The second ratio considers the fact that Λ_{SR} is equal to or higher than the electron wavelength ($\sim$ 10 nm), leading to μ_{SR} being proportional to $\Lambda_{SR}/\Delta_{SR}^2$ (cf. **Equation 2.41**)[218], [221]. For the first ratio (cf. **Figure 3.14.a)**), using Λ_{SR} fitted with the K-correlated model leads to a higher ratio due to the lower Λ_{SR} but for the other fitting method for PSD and HHCF, the differences between the different etchings are small. Similarly, using the second ratio (which is more in accordance with the higher extracted Λ_{SR}) the ratio is smaller for Q3 using the K-correlated fitted Λ_{SR} and doesn't vary significantly for all etchings with the other fitting method for PSD and HHCF (only a slightly higher for Q4). Considering that the K-correlated model does not fit properly the high-frequency range,

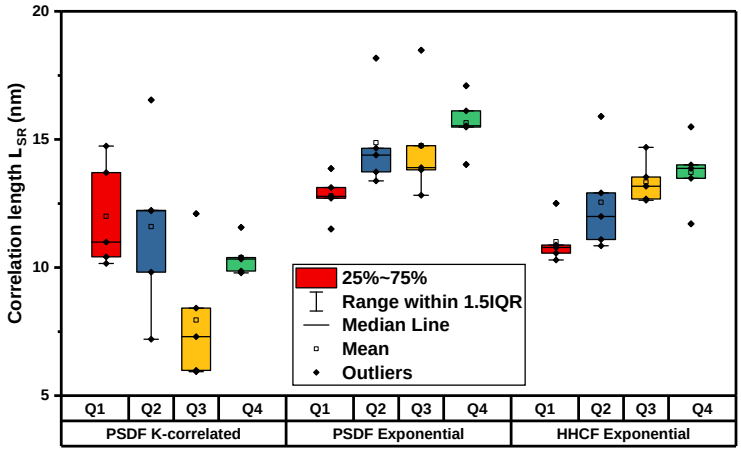


Figure 3.13: Correlation lengths Λ_{SR} extracted from both PSD and HHCF with the K-correlated model and the exponential model.

the differences observed with the K-correlated model for both ratio can not be fully trusted. Therefore, regarding the extracted PSD function and both ratios for the exponential model in PSD and HHCF, it is possible to conclude that little difference in μ_{SR} could be observed for the different etchings.

To confirm this observation, the mobility of both the bottom channel and the sidewalls for the different etchings were extracted with GaNG transistors. The I_D-V_G measured with $V_D = 0.5$ V in **Figure 3.15** for the different etching processes indicate a degraded characteristic for Q3 inducing a higher ON-resistance (R_{ON}), whereas the other etchings are similar to the POR Q1 process. Plotting $R_{ON}(L_G)$ for a given V_G (cf. **Figure 3.15.b)**) allows to extract from the slope the bottom channel resistance, and from the intercept the sidewall resistance [46] (cf. **Section 2.2.4.1**). These resistances are then used in the mobility partitioning and extraction. **Figure 3.16** represents the electron mobility extracted for both the bottom region (μ_{bot}) and the sidewall region (μ_{sw}) as a function of the electron channel density ($\mathrm{n_{Channel}}$). Similar to the I_D-V_G, the bottom channel is strongly degraded by the Q3 etching process with a reduction of 50% along the electron density. However, for the sidewall mobility, all etching processes have similar behavior, with the Q4 process showing only slightly higher mobility.

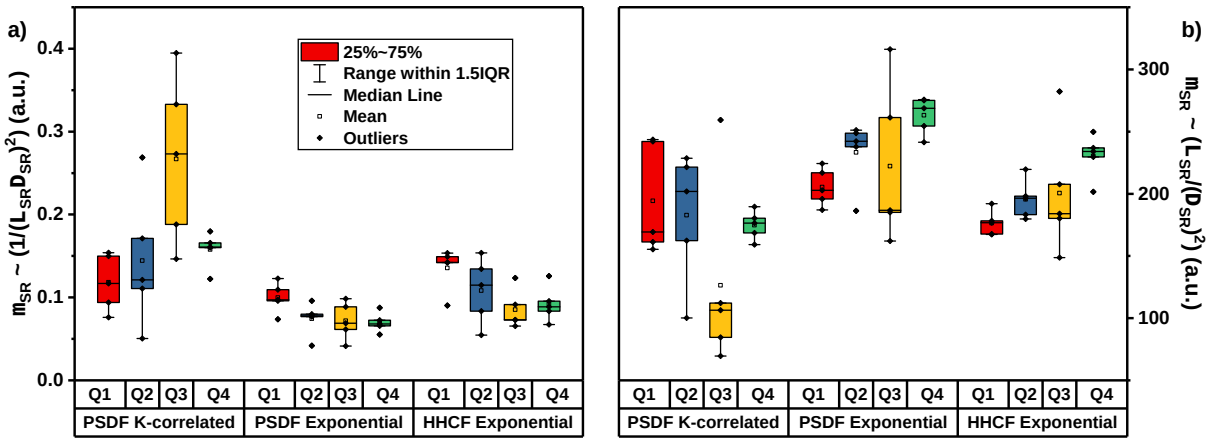


*Figure 3.14: Ratios of roughness parameters proportional to μ_{SR}: a) $1/(\Delta_{SR} \times \Lambda_{SR})^2$ and b) $\Lambda_{SR}/\Delta_{SR}^2$. The Δ_{SR} values correspond to **Figure 3.11** and the Λ_{SR} to **Figure 3.13**.*

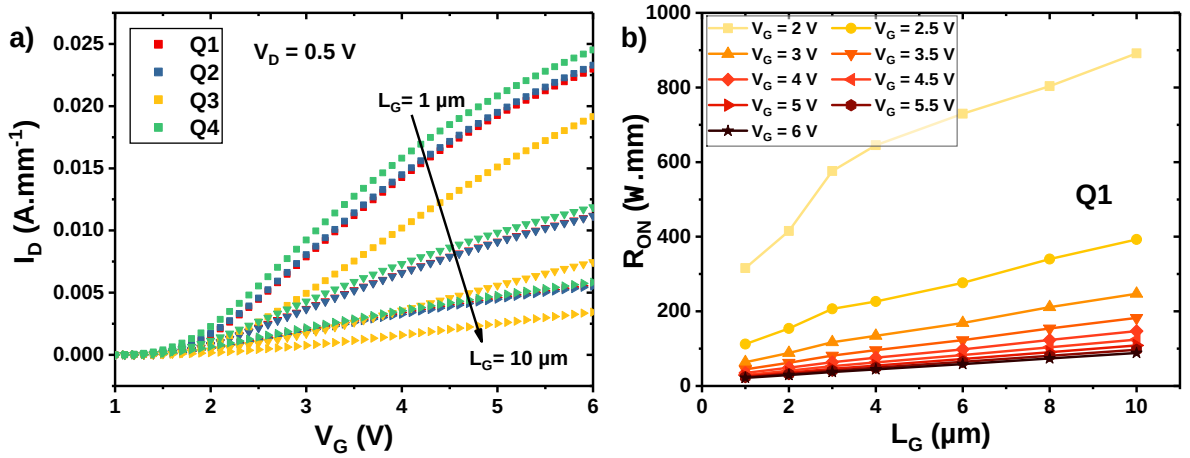


Figure 3.15: a)I_D-V_G of the different etchings processes for different gate length (median of 21 measurements); b) R_ON for different gate lengths and different V_G for the POR etching process (Q1) (median of 21 measurements).

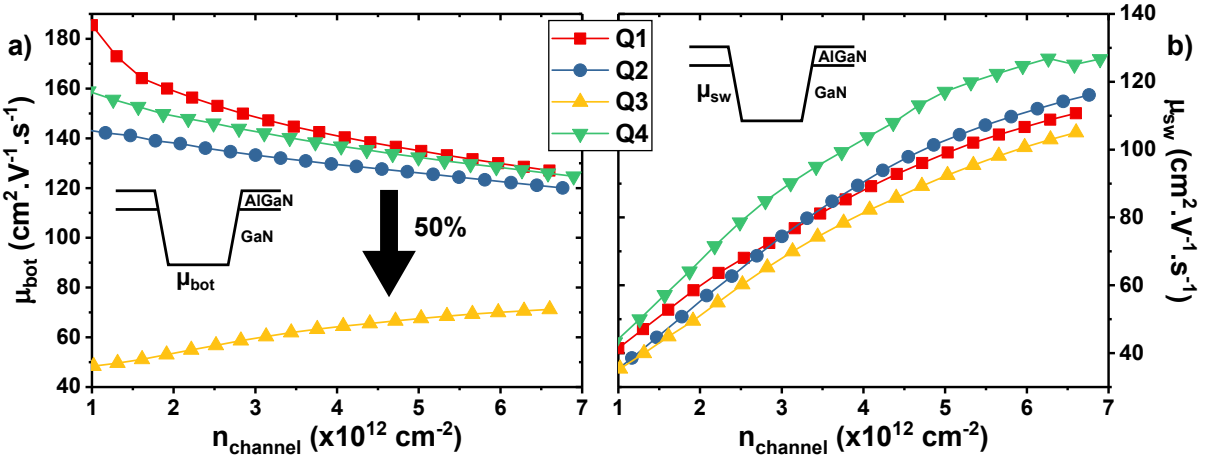


Figure 3.16: Extracted a)bottom mobility and b) sidewall mobility for the different etching processes (median of 21 measurements).

Consequently, the degraded I_D-V_G for Q3 can be mainly associated with degraded mobility at the gate bottom. By analogy, this gate bottom is precisely the region that is analyzed with AFM. Since little difference in terms of roughness parameters and their ratio proportional to μ_{SR} is observed for the different etchings, the extracted μ_{bot} confirms that μ_{SR} is not the main limiting factor. In fact, if it was the case, μ_{bot} should be impacted by surface scattering at higher electron density (10^{13} cm^{-2}). However, μ_{bot} is already lower for Q3 at low electron density (10^{12} cm^{-2}). The low mobility at low $n_{Channel}$ could be related to other scattering phenomena, such as Coulomb scattering and/or neutral impurities scattering [219], [221], [235]. Therefore, Q3 seems to affect the surface mainly by introducing defects such as interface charges and/or neutral impurities, rather than by increasing the roughness.

3.1.3 Conclusions

In this section, the Power Spectral Density (PSD) was studied in order to characterize the impact of the etching process on GaN surface roughness. The PSD suffers from little variations when measured in the same position but increases slightly when measuring at different positions demonstrating a little non uniform GaN roughness across the 200 mm wafer. In fact, for a 2×2 μm^2 scan area, the standard deviation at different positions for Δ_{SR} and $\Lambda_{SR}^{Exponential}$ are 0.11 and 2.6 nm respectively, instead of 0.02 and 0.4 nm at the same position. Comparing before and after etching reveals that etching removes the terraces, increases RMS (Δ_{SR}) by roughly 0.1 nm, and reduces the correlation length (Λ_{SR}) by 20 to 40 nm for scan areas larger than 2×2 μm^2. Moreover, the PSD provides a detailed description of the difference between before and after etching, more precise than only using Δ_{SR}, with etched surfaces having a PSD higher by 45$\sim$80% than as-grown surfaces (lower Δ_{SR} and higher Λ_{SR} for as-grown GaN) instead of only 3$\sim$57% for Δ_{SR}. This difference seems to indicate that the etching process can degrade μ_{SR}. Reducing the scan area is also important in order to enhance the differences in Δ_{SR} and Λ_{SR} before and after etching but also between etching processes.

With the difference between as-grown and etched being defined, this methodology with a small scan area was applied for comparing different etching processes. While Δ_{SR} has a higher value for the Q3 process, the differences between all the etchings are rather small. Comparing their respective PSD also reveals little difference, indicating a low impact of the tested etching processes on the GaN surface roughness and a similar μ_{SR}. The Height-Height Correlation function (HHCF) was also tested in order to observed possible changes between the etched surfaces. However, other than the HHCF plateau linked to Δ_{SR} being higher for Q3, the extracted correlation lengths are also similar. Even considering different ratios proportional to μ_{SR}, a little difference is observed between the etched surfaces, confirming the observed PSD. By extracting the respective gate bottom mobility and sidewall mobility from MOSc-HEMTs, the Q3 process is shown to degrade the bottom mobility starting at a low electron density (10^{12} cm^{-2}). Since the mobility is already affected at a low electron density, other scattering mechanisms such as Coulomb and neutral impurities seem to be responsible for the lower mobility with the Q3 process.

Therefore, this confirms that the gate bottom μ_{SR} does not contribute significantly to the mobility degradation of MOSc-HEMTs for the studied etchings processes, as observed with the PSD and the related extracted parameters. This confirms the overall stable surface roughness obtained with the different etchings and the limited impact of μ_{SR}. Nonetheless, the study of interface states by the conductance

technique can be interesting to understand the impact of the Q3 process on Coulomb scattering. The PSD methodology could be interesting in the study of etching with more surface roughness degradation affecting the MOSc-HEMT electron mobility, such as ICP-RIE etching without ALE and with a higher bias. Therefore, for the MOSc-HEMT process of reference and the 3 other etching variations, the roughness induced by etching is not a limiting factor to the device performance. The thesis work will now focus on the impact of MOSc-HEMT processing on V_{FB} instability studied through MOS capacitors.

3.2 Impact of Post-Deposition Anneal on Al_2O_3/GaN gate stack

After etching, the GaN surface is cleaned with a wet solution in order to reduce the presence of impurities, etching residues and GaO_x formed during the O_2 plasma strip. Depending on this surface preparation, the Al_2O_3/etched GaN interface and gate stack will induce variation in electrical parameters such as V_{FB}/V_{TH} and its hysteresis [60], [70], [236], [237]. In the case of the MOSc-HEMT developed at CEA-Leti, an optimal cleaning sequence ending with HF was selected. Post Deposition Annealing (PDA) can further optimized the Al_2O_3/etched GaN gate stack by improving the interface and reducing defects in the dielectric, resulting in higher V_{TH} and reduced ΔV_{TH} [139], [140]. Except for Kim et al. [42], most of the reports on PDA for Al_2O_3/GaN gate stack are on Al_2O_3 deposited on as-grown GaN [81], [134], [135], [137], [142], [199] or on etched GaN with the fabrication of drain and source contacts before gate fabrication [132], [139]. Since fabricating the source and drain after the gate stack can degrade it [132], the impact of PDA on the Al_2O_3/etched GaN gate is necessary in order to optimized it accordingly to the MOSc-HEMT process flow. Therefore, in the next section, different PDA temperatures will be investigated without or with the MOSc-HEMT final thermal annealing.

3.2.1 Experimental details

30 nm Al_2O_3 layers were deposited by ALD on (0001) oriented n-GaN buffer layers with a Si doping concentration of 5×10^{17} cm^{-3}. The n-GaN buffer layers were grown on 200 mm p-Si (111) substrates by MOCVD. Before Al_2O_3 deposition, the substrates were etched by ICP-RIE and ALE and cleaned with a wet sequence containing HF. The Al_2O_3 precursors were Trimethylaluminum and H_2O for Al and O sources, and the deposition temperature was 300°C. After deposition, PDA was performed under N_2 1) for 4 min at 400, 500, or 600°C on $1.5 \times$ 1.5 cm^2 samples or 2) for 5 min at 400, 500, or 550°C on 200 mm wafers. This duration of PDA was chosen since minor consensus is found for PDA's duration, with durations ranging from 30 s to 90 min in the literature [81], [138]. The temperature range was chosen to be lower than alumina's crystallization temperature, and higher than the deposition temperature. Initially, a PDA at 600°C for the 200 mm wafers was planned but the wafer broke during the fabrication process. MOSCAPs test structures were consequently fabricated: 1) on the $1.5 \times$ 1.5 cm^2 samples with Au/Ni metal contacts deposited by e-beam evaporation (MOS-1; cf. MOSCAPs on coupon **Section 2.1.2**) and 2) on the 200 mm wafers with TiN metal contacts deposited by Physical Vapor Deposition (MOS-2; cf. MOSCAPs on 200 mm wafers **Section 2.1.3**). MOS-1 were fabricated to investigate rapidly the impact of PDA without the MOSc-HEMT final thermal budget whereas MOS-2 were also annealed after metallization in order to simulate the MOSc-HEMT process flow and final thermal budget. The final thermal budget consists in the ohmic contact annealing at 400-650°C for 2 min under N_2 and the final

annealing at low temperature (300- 550°C) for several hours. The process flow for both MOS devices is summarized in **Figure 3.17**.

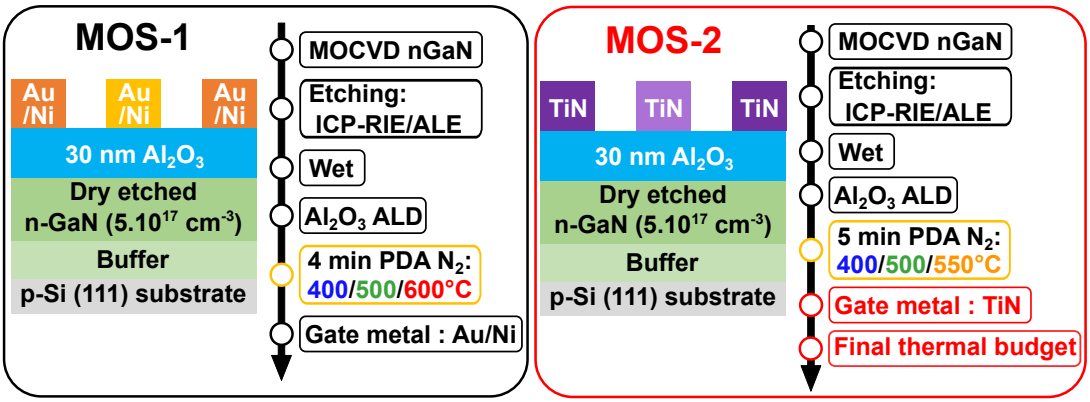


Figure 3.17: MOS-1 and MOS-2 process flows with different PDA temperatures.

C-V and G_m/ω measurements were performed on these samples at 1 kHz with a forward voltage sweep between -4 V and 6 V and a backward voltage sweep between 6 V and -4 V. Interface states density (D_{it}) of MOS-1 devices were extracted by the conductance method at different temperatures explained in **Section 2.2.3.2**. Simple extraction of D_{it} at room temperature for MOS-1 and MOS-2 devices was also performed using the abacus in **Section 2.2.3.2**. Current density-Voltage (*J-V*) measurements were performed between 0 to 50 V for MOS-2.

In parallel, 15 nm Al_2O_3 were deposited on etched n-GaN substrates following the process of MOS-1 devices, in order to perform physical and chemical characterizations. These samples were analyzed using HAXPES, ToF-SIMS, and GIXRD. The HAXPES analyses were conducted on the PHI Quantes equipped with a Cr Kα ($h\nu = 5414.7\ eV$) X-Ray source. The photoelectron take-off angles were set at 45° for Ga2p$_{3/2}$ analysis and 90° O1s analysis respectively, yielding to integrated sampling depths of approximately 16.6 and 24 nm considering the IMFP of photoelectrons in Al_2O_3. The fitting models for both Ga2p$_{3/2}$ and O1s are presented in **Section 2.3.1.2**. GaN oxidation at the interface was analyzed with the Ga-O area percentage in Ga2p$_{3/2}$ peak, and the presence of O-H groups was deduced from the area of O-H bonds in O1s peak. ToF-SIMS analyses were performed by detecting negative ions. GIXRD was performed with a 2θ angle between 20° and 60°. Finally, for FTIR with multiple internal reflection, dedicated 30 nm ALD Al_2O_3 on p-Si samples were analyzed to investigate the variation of OH groups with PDA temperatures.

3.2.2 Results and discussion

3.2.2.1 Without final thermal budget

The *C-V* and G_m/ω measurements for MOS-1 devices are reported in **Figure 3.18**, with V_{FB} and ΔV_{FB} being extracted and shown in **Figure 3.19**. A small reduction of V_{FB} up to 500°C and a strong decrease for a PDA over 500°C is noticed for MOS-1 devices, going from -220 mV to -350 mV between the reference and the PDA at 500°C and down to -700 mV for a PDA at 600°C. The decrease of V_{FB} could be detrimental to our MOSc-HEMT, leading to a lower V_{TH} as explained in **Section 2.2.1.1**. This reduction is contrary to commonly reported increased V_{FB} or V_{TH} after PDA [137]–[139]. For hysteresis, ΔV_{FB} is

reduced with increasing PDA temperature and reaches a minimum at 500°C, with a reduction from 108 mV to 56 mV between the reference and a PDA at 500°C. The reduction of ΔV_{FB} with PDA temperature was similarly observed in previous reports [139], [140], [238]. However, for a PDA over 500°C, an small increase of ΔV_{FB} is observed.

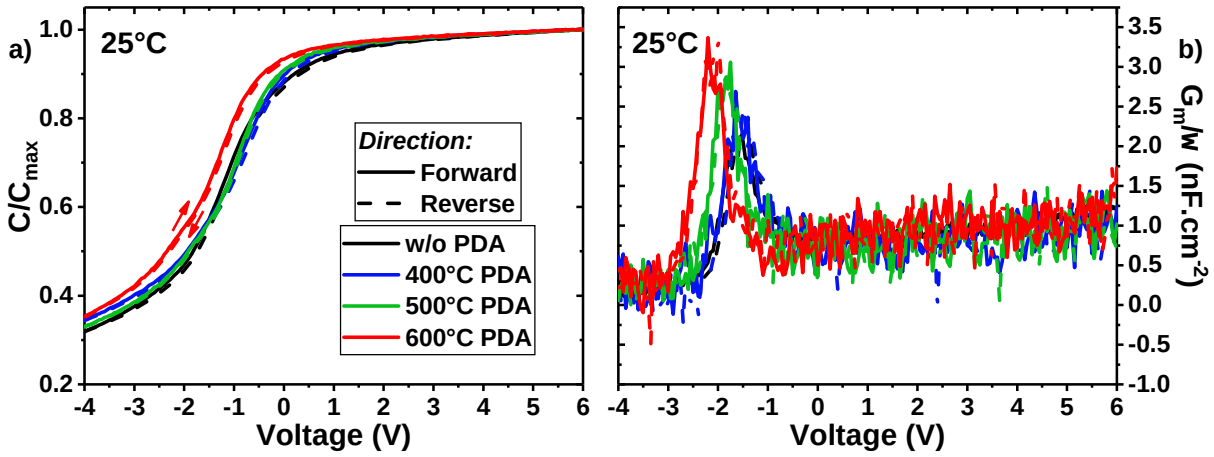


Figure 3.18: Normalized a) C-V (median of five measurements) and b) G_m/ω measurements (single measurement) for MOS-1 devices.

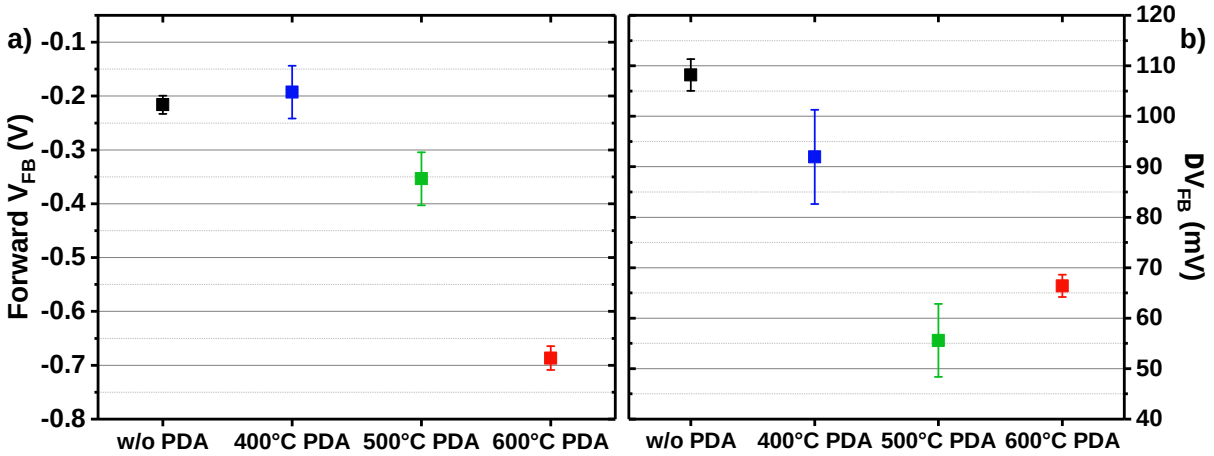


Figure 3.19: a) V_{FB} and b) ΔV_{FB} for MOS-1 devices extracted from the C-V measurements (median of five measurements).

$E_C - E_T$ (eV)	D_{it} $(10^{10} eV^{-1}.cm^{-2})$			
	w/o PDA	*w/ 400°C PDA*	*w/ 500°C PDA*	*w/ 600°C PDA*
0.49 $(25°C)$	3.47 ± 0.03	3.91 ± 0.08	4.83 ± 0.21	5.23 ± 0.21

Table 3.3: Interface states density extracted for MOS-1 devices from normalized G_m/ω peaks at 1 kHz and at 25°C (median of five measurements).

Concerning the interface, a peak of conductance can be observed in **Figure 3.18.b)** for all PDA samples. It is linked with the small bump in **Figure 3.18.a)** and can be related to the presence of interface states induced at the etched GaN surface. With increasing PDA temperature, the peak slightly increases. As represented in **Table 3.3**, by using the interface states density abacus in **Section 2.2.3.2 Figure 2.7**, D_{it} at 0.49 eV from GaN's conduction band increases from 3.47x10^{10} to 5.23x10^{10} $eV^{-1}.cm^{-2}$ between the reference and PDA at 600°C.

Further characterizations were performed using the conductance method at different temperatures. As represented in **Figure 3.20.a)**, the D_{it} is extracted between 0 to 0.9 eV from GaN's conduction band. It slightly decreases with trap energy approaching GaN's conduction band. This is contrary to the typically U-shaped or increased D_{it} towards GaN's conduction band reported on GaN [117], [141], [236], [239], [240]. Still, a similar observation was recently reported by our group [184]. Moreover, the D_{it} extraction is proven reliable due to the good overlap between the D_{it} extracted at both different temperatures and frequencies.

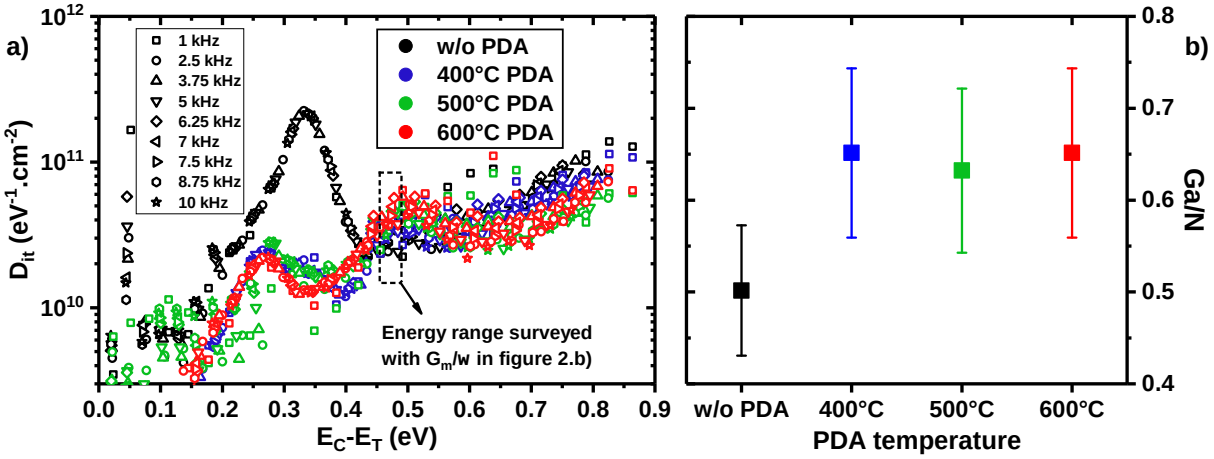


Figure 3.20: a) Interface states density using the temperature method at frequencies between 1 kHz and 10 kHz, for different PDA temperatures; b) relative Ga/N ratio for different PDA temperatures using HAXPES quantification (cf. ***Section 2.3.1.6****).*

In the energy range surveyed by the G_m/ω measurements in **Figure 3.18.b)**, the D_{it} values follow the same trend as reported in **Table 3.3**, with values ranging from 2 to $6 \times 10^{10} \text{eV}^{-1}.\text{cm}^{-2}$. However, the major impact of annealing is found at 0.33 eV where a peak of D_{it} is reduced with PDA. Similarly in the case of a MOSc-HEMT, Ferrandis et al. [241] reported by Deep Level Transient Spectroscopy (DLTS) the presence a trap at 0.31 eV related to ICP-RIE etching. Fang et al. [242] also reported by DLTS the presence of a surface defect at 0.25 eV after ICP-RIE etching and assigned it to the complex V_N-V_{Ga}. In terms of D_{it} similar peak at 0.5 eV was found using the Terman method and was associated to Nitrogen Vacancies (V_N) on a SiN/GaN gate stack with a NH_4OH wet treatment and a H_2 plasma treatment [243]. Finally, Bisi et al. have also reviewed defects in GaN where V_N are reported between 0.09 to 0.27 eV from GaN's conduction band [244]. Other reported defects in the same range are Mg impurities in n-GaN (0.355 eV), the Si dopant in it-self (Si_{Ga} = 0.37-0.4 eV) and impurities such as C, O or H in nitrogen substitutional position [244]–[246].

In parallel, extracting the Ga/N stoichiometry from HAXPES measurements for the different PDA temperatures, reveals a ratio closer to one after PDA (cf. **Figure 3.20.b)**). This better stoichiometry could be an explanation for the reduced D_{it} peak with fewer native defects at the interface such as V_N. In fact, Hashizume et al. observed a relaxed and better organized Al_2O_3/GaN interface after annealing [145]. However, decreasing the V_N density with temperature would result in a lower Ga/N ratio, which is the opposite of what is observed in **Figure 3.20.b)**. As a result, it is challenging to link the improved GaN stoichiometry at the interface to a reduced number of V_N defects. Moreover, the Ga/N ratio lower than unity cannot be assigned to a rearranged interface, since as proposed by our group, the difference in

probing death between the $Ga2p_{3/2}$ and N1s photoelectrons [59]. The reduction of V_N-V_{Ga} complexes could be another possibility. Concerning the presence of carbon related defects, the ToF-SIMS analyses did not reveal any specific changes in C carbon content in the gate stack. Finally, regarding the presence oxygen at the interface, **Figure 3.22** indicates a reduced Ga-O bonds, related to GaO_x, after annealing. Such reduction could also explain the reduced D_{it} peak. Nonetheless the most probable origin for the D_{it} peak is an etching induced defect that reduces with the annealing. Other than the peak, the D_{it} values for all samples are under $1x10^{11}$ $eV^{-1}.cm^{-2}$, highlighting an optimized interface thanks to the etching and wet processes as previously reported by our group [184]. Therefore, contrary to Tadmor et al. [146], annealing does not introduce interface states.

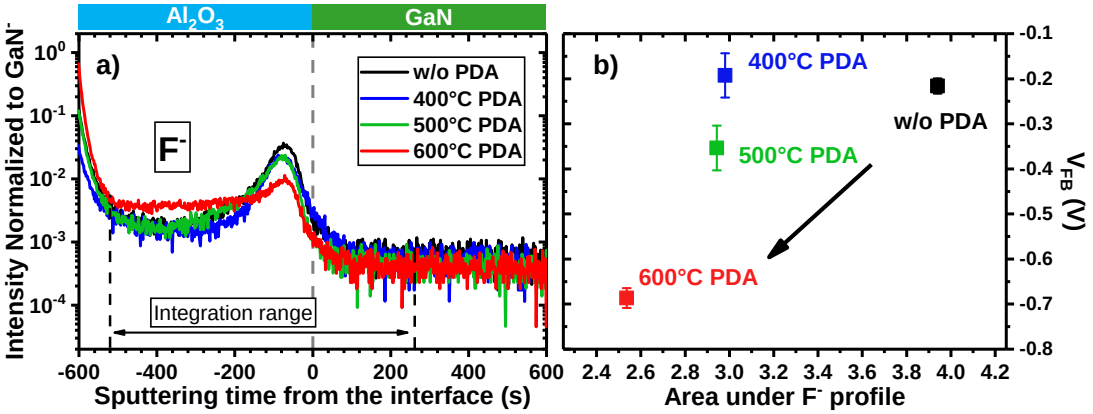


Figure 3.21: a) Normalized Fluorine depth profiles obtained by ToF-SIMS for different PDA temperatures; b) Integrated area under fluorine profiles for a defined range as a function of V_{FB} for MOS-1 devices.

In order to understand the reduction of V_{FB}, the fluorine depth profile was analyzed by ToF-SIMS (cf. **Figure 3.21.a)**). This V_{FB} reduction seems to follow the trend of fluorine reduction at the interface. In fact, the fluorine profile at the interface reduces with the PDA temperature, with a strong decrease for 600°C PDA. Likewise, the content of fluorine represented by the integrated area under the fluorine profile reduces with PDA temperature (cf. **Figure 3.21.b)**). A diffusion of fluorine towards the Al_2O_3 bulk region is also observed for a PDA higher than 500°C. The stretch of fluorine in the GaN substrate for 400°C can be attributed to an increased surface roughness. The origin of fluorine contamination could be attributed to the wet cleaning containing HF [69], [229], [236], but internal reports at CEA-Leti have described the presence of fluorine without a HF wet cleaning step, therefore it is possible that the fluorine comes from different sources before or during the dielectric deposition. Therefore, more work on this issue needs to be done understand the fluorine presence. Since fluorine doping of Al_2O_3 is also used to increase V_{TH} by introducing negative charges [32], [34], the reduction of fluorine could explain the reduction of V_{FB} for MOS-1 devices. Nonetheless, the reduction of V_{FB} could also be explained by the increase of positives charges in Al_2O_3 such as V_O^{+2} or Al_i^{+3} or the decrease of negatives charges such as O_i^{-2} or V_{Al}^{-3} [143], [156]. Similar reduction of V_{FB} with annealing temperature was already reported in the literature, the main hypothesis being the reduction of negative charges introduced during the fabrication process [146]. Another possibility is the increase of GaO_x at the interface inducing positive charges [60].

However, as observed by HAXPES, the Ga-O bonds related to the presence of interfacial GaO_x reaches a minimum after a PDA at 500°C (cf. **Figure 3.22.a), left**). Since GaO_x is reduced after annealing, this

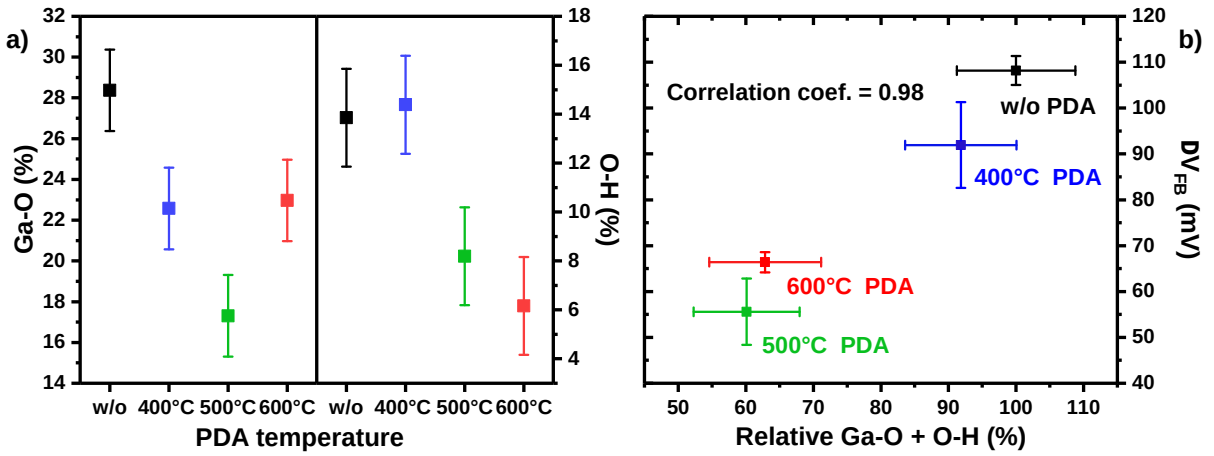


Figure 3.22: a) Ga-O and O-H bonds percentages extracted by HAXPES from respectively $Ga2p_{3/2}$ and O1s spectra for different PDA temperatures and without final thermal budget ; b) correlation between hysteresis and relative Ga-O + O-H percentage.

means that GaO_x is not responsible for the V_{FB} reduction. Nonetheless, the trend observed for GaO_x is similar to the decrease of hysteresis with temperature, with a minimum observed at 500°C PDA. The reduction of GaO_x could consequently explain the reduction of hysteresis. This correlation is plausible since GaO_x reduction was reported to reduce hysteresis [69], [75], [82]. But after a PDA at 600°C, the Ga-O bond percentage is found to be equal to the percentage observed after a 400°C PDA. Whereas in terms of hysteresis, a lower ΔV_{FB} after a PDA at 600°C than after a PDA at 400°C is observed. The presence of GaO_x can't alone explain the observed hysteresis. Other than Ga-O bonds, hydroxyl groups' reduction is equally noticed in Al_2O_3 with increasing PDA temperature. Indeed, O-H bonds reduction after PDA is confirmed by HAXPES analyses (cf. **Figure 3.22.a), right**) as also previously observed by Zhu et al. [247] but with standard XPS. Contrary to Ga-O, O-H bonds are further reduced at 600°C, possibly explaining the hysteresis difference between a PDA at 400°C and 600°C. Similarly to GaO_x, the reduction of OH groups was associated with a reduction of hysteresis [75]. Interstitial hydrogen defect energy levels in amorphous Al_2O_3 were indeed reported to be close to the GaN conduction band [83], this proximity to the conduction band leading to electron trapping and hysteresis. Therefore, to analyze the combined effect of GaO_x and hydroxyl groups, their combined relative variation was calculated using the equation below and plotted with respect to hysteresis in **Figure 3.22.b)**.

$$R_{GaO-OH} = 50 \times \left(\frac{GaO}{GaO_{w/oPDA}} + \frac{OH}{OH_{w/oPDA}} \right) \tag{3.1}$$

As represented, the combined impact of GaO_x and OH groups seems to explain the observed hysteresis with the different PDA temperatures with a correlation coefficient of 0.98, instead of 0.88 and 0.87 for respectively GaO_x and OH groups. Hence it is essential to reduce both the interfacial GaO_x and the OH groups in order to reduce the hysteresis.

The observed trend of OH reduction was also confirmed both by FTIR and ToF-SIMS analyses (cf. **Figure 3.23**). With FTIR, the absorbance spectrum associated to OH bonds reduces and reaches a minimum at 500°C. Through ToF-SIMS, the OH reduction is seen to occur mainly in Al_2O_3 bulk, little reduction at the interface being observed. More specifically, the stretch of OH profile in the GaN substrate for

400°C was also observed for other elements from Al_2O_3 and could be attributed to the impact of surface roughness.

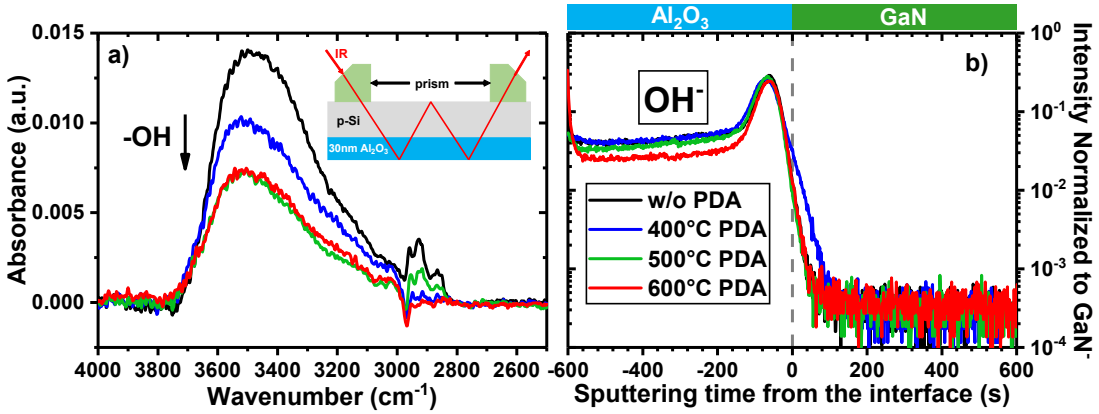


Figure 3.23: a) FTIR O-H absorbance spectrum for 30 nm Al_2O_3 on p-Si with different PDA temperatures and without final thermal budget. A manual correction of base line was performed; b) OH profiles by ToF-SIMS for different PDA temperatures.

Finally, the Al_2O_3 band gap and band alignment with GaN were surveyed with XPS by analyzing the O1s energy loss spectrum (cf. in **Annex B**, **Figure A.1**) and the Ga3d spectra at 45°, for 3 nm Al_2O_3/etched GaN samples with or without PDA at 500°C. As represented in **Figure 3.24**, the band gap is around 6.8∽7 eV, these values being in agreement with literature for ALD Al_2O_3 [132], [133]. The annealing here increases the Al_2O_3 band gap by 0.2 eV with still an amorphous structure. Regarding the band offsets, they were extracted using **Equation 2.37** in **Section 2.3.1.8**. Both samples have relatively high CBO with values around 2.4 eV, allowing to reduce electron leakage through the gate but equally to reduce electron trapping. On the opposite, the VBO are low and close to 1 eV, and could be a problem for hole leakage. Nonetheless, both CBO and VBO values are also close to some values reported in the literature [15], [123], [164], [248]–[250], despite variation in the order of 1 eV in both CBO and VBO values due to different processing prior Al_2O_3 deposition or different deposition techniques in itself [212], [251], [252].

Concerning the GaN's band bending for both samples calculated using **Equation 2.31** in **Section 2.3.1.8**, the band bending is upward and around 0.8 eV. The annealing therefore seems not to change the band bending. Yang et al. [252] have also reported an upward band bending at 0.9 eV without annealing and 0.3 eV after annealing at 650°C in vacuum for 1 nm PE-ALD Al_2O_3/GaN. By using **Equation 2.33** in **Section 2.3.1.8**, the charges at the interface associated to the band banding are negative and around $-2.1 \times 10^{10}\text{cm}^{-2}$ (cf. **Table 3.4**). This upward band bending and consequently interface charges are contrary to the observed negative V_{FB} and reduction of V_{FB} with PDA in **Figure 3.19.a)**, but also to the positive interface charges reported in the literature [143], [253], [254]. One possible explanation is that the 3 nm and 30 nm Al_2O_3 samples have different amounts of interface charges. Gong et al. [250] have indeed reported a reducing upward band bending with increasing ALD cycles. Their hypothesis follows the theory proposed by Esposto et al. [253] where ionized donor charges situated between Al_2O_3 and GaN conduction band starts to form with increasing the thickness of deposited Al_2O_3 (or higher ALD cycles). The thicker Al_2O_3 would have a different band structure, which would provide these donor charges. Wang et al. recently proposed that these positive interfacial charges are Aluminium Interstitial

(Al_i) defects formed during the initial ALD cycles, notably by the use of TMA as precursor [254]. Al_i can indeed have a positive charge according to Density Functional Theory (DFT) calculations for amorphous Al_2O_3 [156]. Therefore, it is possible that charges inversion at the interface would happen with Al_2O_3 thicker than 3 nm. This hypothesis could also explained the reason for an upward band bending obtained by Yang et al. [252]. Another possibility is the higher interface oxidation observed with higher thicknesses of Al_2O_3 on etched GaN described in **Section 2.3.1.4**. Considering that GaO_x was reported to introduce positive charges [60], [255], [256], a higher amount of GaO_x could potentially increase these positive charges and induce downward band bending. However, this hypothesis is incongruent with the fact that the variation in Ga-O bonds with PDA does not follow the trend observed in V_{FB}. Therefore, the most suitable hypothesis is the presence of positive charges in Al_2O_3 such as Al_i.

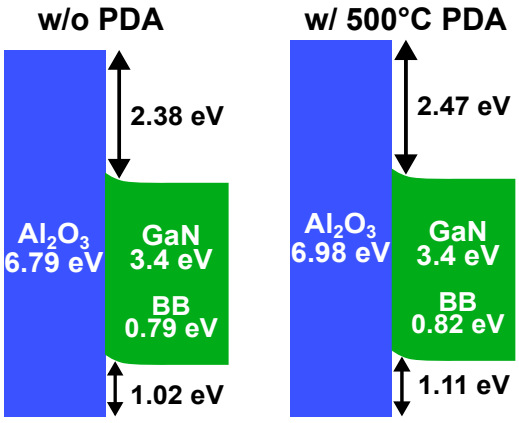


Figure 3.24: Band offsets and band bendings for the Al_2O_3/etched GaN without and with a PDA at 500°C. The Ga3d spectra were analyzed at the take-off angle of 45°.

Sample	w/o PDA	w/ 500 °C PDA
Band bending (eV)	1.02	0.82
$\sigma^{net}_{interf.}$ cm^{-2}	-2.10×10^{12}	-2.13×10^{12}
$\sigma^{positive}_{added.}$ cm^{-2}	1.59×10^{13}	1.59×10^{13}

Table 3.4: Extracted GaN's band bending using the $Ga2p_{3/2}$ spectrum at the take-off angle of 45°. The net interface charges are calculated from the band bending. The added positive interface charges are calculated by subtracting the net surface charges by GaN's spontaneous-polarization-induced negative charges (-1.8×10^{13} cm^{-2})

Considering the obtained results without the final thermal budget, an optimal PDA temperature is found at 500°C in which ΔV_{FB} is minimal and the reduction of V_{FB} is limited. The interface is also found to be optimized thanks to the etching and wet processes combined with PDA (reduction of GaO_x). In the next section, the impact of the final thermal budget will be discussed.

3.2.2.2 With final thermal budget

The MOS-2 devices (cf. **Figure 3.17**) have a final thermal annealing in order to simulate the overall thermal budget associated to the source and drain ohmic contacts. Their C-V and G_m/ω measurements are reported in **Figure 3.25**, with the extracted ΔV_{FB} and V_{FB} shown in **Figure 3.26**. With the final thermal budget, the different PDA temperatures have a reduced impact on V_{FB} with values around 1.2 V.

This means that the pre-existing fixed charges in Al_2O_3 were reduced with the final thermal budget and/or due to the different fabrication process between MOS-1 and MOS-2. With increasing PDA temperature, they seem to slightly vary. By precisely extracting the hysteresis, a low value around 20 mV is found until PDA at 500°C. However, over a 500°C PDA, the hysteresis increases around 42.5 mV, highlighting the slightly higher electron traps in Al_2O_3 after a 550°C PDA. By analyzing both the V_{FB} and ΔV_{FB} trends, the final annealing without PDA already presents a low hysteresis, whereas applying a PDA does not change significantly V_{FB} but can increase hysteresis, especially after a 550°C PDA.

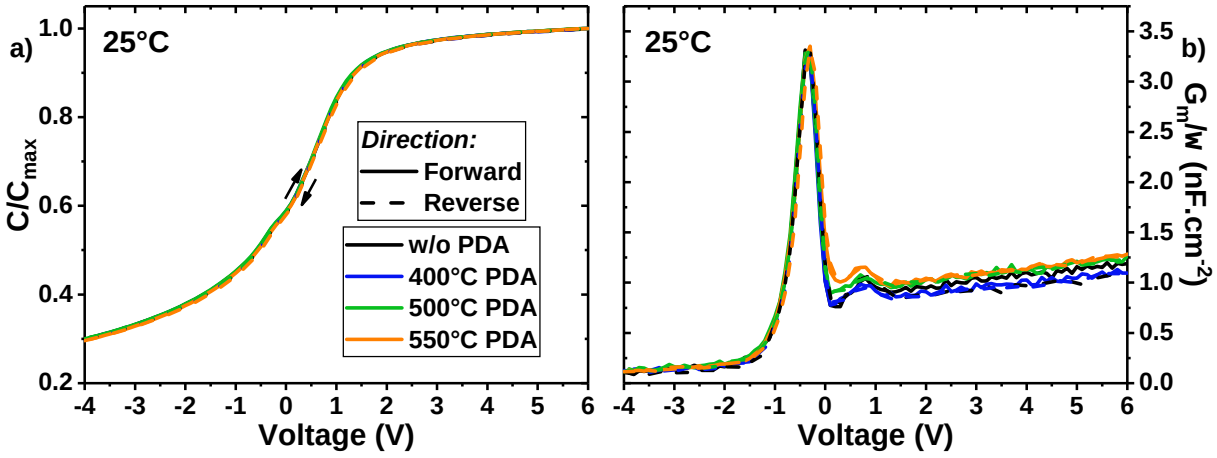


Figure 3.25: Normalized a) C-V (median of nineteen measurements) and b) G_m/ω measurements (median of nineteen measurements) for MOS-2 devices.

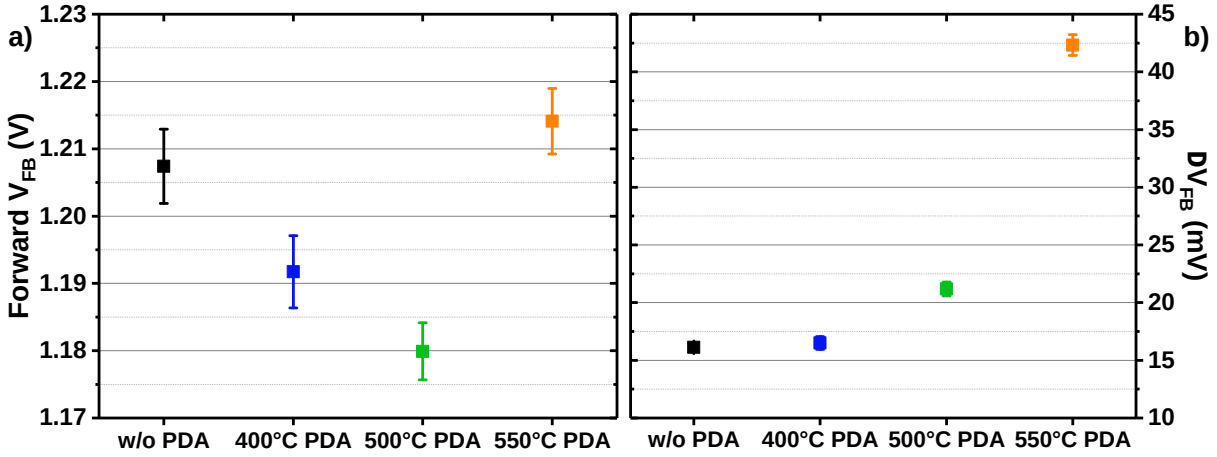


Figure 3.26: a) V_{FB} and b) ΔV_{FB} for MOS-2 devices extracted from the C-V measurements (median of nineteen measurements).

$E_C - E_T$ (eV)	D_{it} $(10^{10} eV^{-1}.cm^{-2})$			
	w/o PDA	*w/ 400°C PDA*	*w/ 500°C PDA*	*w/ 550°C PDA*
0.49 (25°C)	5.70 ± 0.33	5.56 ± 0.31	5.64 ± 0.04	5.72 ± 0.03

Table 3.5: Interface states density extracted for MOS-2 devices from normalized G_m/ω peaks at 1 kHz and at 25°C (median of nineteen measurements).

Analyzing the interface with G_m/ω peaks reveals a similar amount of D_{it} for all PDA samples (cf. **Table 3.5**). These values are close to the ones extracted in **Table 3.3** without the final thermal budget or those from the reference [184] ($\backsim 2 \times 10^{10}$ $eV^{-1}.cm^{-2}$). Therefore, the final thermal budget combined with PDA does not affect the interface, the latter being already optimized by the etching and wet pro-

cesses, but a comparison with MOS-2 devices before the final thermal budget is necessary to affirm this hypothesis.

Concerning V_{FB} and ΔV_{FB}, by comparing them with the results obtained for MOS-1 (cf. **Figure 3.18**), a beneficial contribution of the final thermal budget is observed in MOS-2 devices. In fact without PDA, the V_{FB} increases from -0.2 to 1.2 V and hysteresis reduces from 110 to 20 mV with the final thermal budget. Moreover, as stated previously, PDA has a limited impact on MOS-2 devices resulting in a overall stable V_{FB} and ΔV_{FB} until a PDA at 500°C. This difference can be explained by the fact that the final thermal budget acts as a Post Metallization Annealing (PMA), the latter being reported as beneficial [143], [144], [146]. Another possibility is the gate material and/or deposition technique. E-beam evaporation was indeed reported to introduce positive charge [257], reducing V_{FB} in MOS-devices. Nonetheless, for both types of devices, a PDA over 500°C is detrimental to the gate stack with increased hysteresis.

Moreover, this degradation is equally observed in MOS-2 devices with *J-E* measurements and extracted breakdown field. In **Figure 3.27.a)**, some devices with a PDA at 550°C have an earlier breakdown. The extracted breakdown field further confirms the presence of two populations (cf. **Figure 3.27.b)**), one with hard breakdown at 11 MV.cm^{-1} and the second with a soft breakdown at 5 MV.cm^{-1}. The devices without PDA or with a lower PDA temperature present instead a hard breakdown between 10 to 13 MV.cm^{-1}. The soft breakdown at 550°C indicates the onset of degradation at such PDA temperature with the final thermal budget.

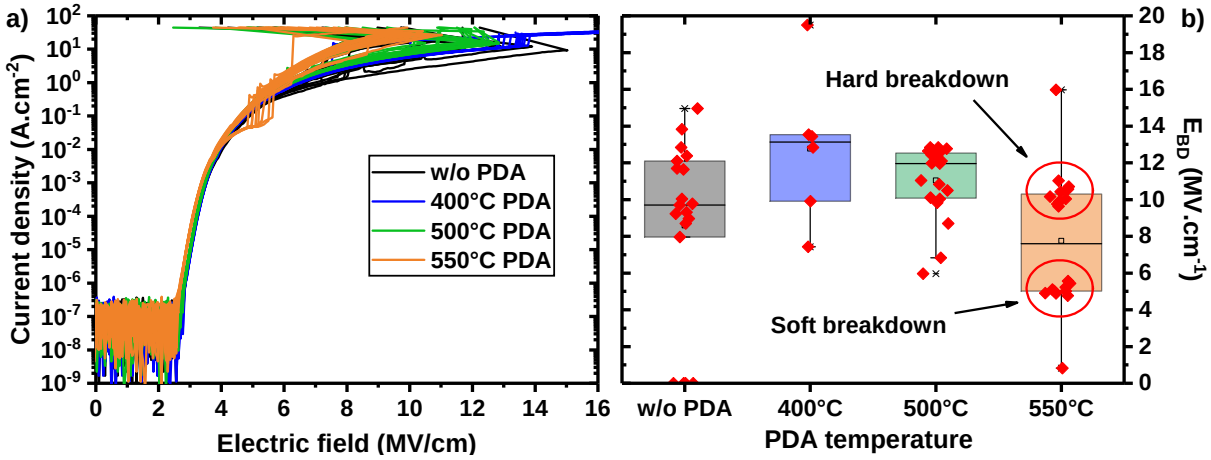


Figure 3.27: a) J-E measurements of MOS-2 devices after the final thermal budget; b) Breakdown field obtained from J-E measurements of MOS-2 devices after the final thermal budget.

This onset of degradation can be partially explained by the onset of crystallization observed for Al_2O_3 deposited on etched GaN with a PDA at 600°C. GIXRD analyses in **Figure 3.28** in fact highlight the presence of a small orthorhombic κ-Al_2O_3 peak attributed to the (122) plan, indicating an onset of crystallization. Moreover, the absence of this peak for both Al_2O_3 deposited on as-grown GaN with a PDA at 600°C and Al_2O_3 deposited on etched GaN with a PDA at 500°C indicates that the onset of crystallization occurs above 500°C when the GaN substrate is etched. This crystallization onset is unexpectedly low compared to the literature for ALD Al_2O_3 [42], [140], [146]. The difference could be attributed to the different etching process, wet sequence (such as TMAH) and/or oxidant precursor in Al_2O_3 deposition (for instance O_2 plasma). Interestingly, Tadmor et al. [146] have reported a change in Al_2O_3 surface roughness after a PMA at 600°C, which they correlate to an onset of degradation in the

dielectric layer. Nonetheless, taking into account the obtained results, the etched GaN surface seems to be the main reason for the earlier onset of crystallization. This further consolidates the need to perform studies on etched GaN substrates in order to optimize the dielectric/GaN gate stack for MOSc-HEMTs, with processes close to the actual transistor process flow.

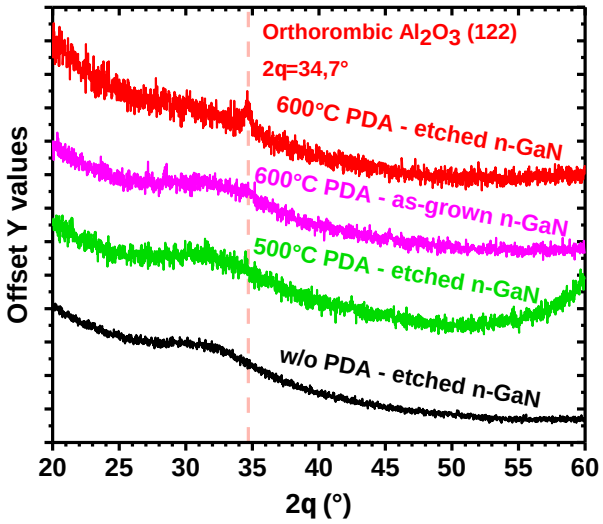


Figure 3.28: GIXRD analyses with grazing angle of 2° for 15 nm Al_2O_3 on etched GaN without PDA, with 500°C and 600°C PDA, and for 15 nm Al_2O_3 on as-grown GaN with a 600°C PDA. All the samples have no final thermal budget.

The onset of crystallization for a PDA above 500°C can explain the lower breakdown field. The presence of grain boundaries can contribute as current paths leading to lower breakdown field. Therefore, these observations further reinforce the detrimental effect of PDA above 500°C for Al_2O_3/etched GaN gate stack.

3.2.3 Conclusions

The impact of PDA for Al_2O_3 on etched GaN substrates was investigated with both electrical and physical-chemical characterizations. First without the final thermal budget, for a PDA below 500°C, the beneficial reduction of hysteresis is observed which could be correlated to the reduction of GaO_x at the Al_2O_3/GaN interface and OH groups in Al_2O_3. V_{FB} is equally reduced, following the trend of fluorine reduction in Al_2O_3. However, increasing the PDA temperature over 500°C strongly reduces V_{FB} and increases hysteresis, the latter being linked to an increase of interfacial GaO_x. Regarding interfacial defects, PDA reduces an interface peak at 0.33 eV from GaN's conduction band, but increasing the PDA temperature does not further reduce the interface states density. The band alignment between Al_2O_3 and the etched GaN substrate highlights a conduction band offset higher than 2 eV, with little impact of annealing. Secondly with the final thermal budget, the impact of PDA on V_{FB} is reduced. Nonetheless, for a PDA over 500°C, a degradation of hysteresis is noticed. Similarly, the breakdown field is reduced, explained by the onset of crystallization for Al_2O_3 deposited on etched GaN for a PDA higher than 500°C.

Consequently, both the thermal budget and the fabrication processes before Al_2O_3 deposition influence the impact of PDA. This study further consolidates the need to take into account these factors when

optimizing the PDA process. Considering both fabricated devices, the optimal PDA temperature with a N_2 atmosphere for the Al_2O_3/etched GaN gate stack is 500°C.

3.3 Conclusion of this chapter

The impact of process steps going from the etching process to the Post-Deposition Anneal (PDA) was studied for the Al_2O_3/etched GaN gate stack. With AFM measurements, the Power Spectral Density (PSD) was used to describe the impact of etching with different scan areas and etching recipes. If a clear difference can be observed between as-grown surfaces and etched surfaces with PSD, its use for describing the impact of different etchings can be limited. Moreover, other than the RMS (Δ_{SR}), the use of the correlation length (Λ_{SR}) as a roughness parameter can be difficult since its extraction can be troublesome and the relationship between Surface-Roughness limited mobility (μ_{SR}) is difficult to define.

Nonetheless, the PSD in itself can be a good indicator of μ_{SR} as observed in the study of different etchings and the extracted mobility. In fact, the gate bottom mobility indicates a mobility impacted more by Coulomb and/or neutral impurities scattering rather than by Surface-Roughness scattering, as suspected from the absence of PSD variation for the different etchings. This also confirms the overall stable roughness obtained with the different etching processes used in the MOSc-HEMT fabrication and their limited effect on R_{ON} and mobility. Therefore, PSD can be helpful to screen rapidly rather the etching will have a strong impact on the surface and the mobility.

After analyzing the surface roughness, the impact of PDA was considered for Al_2O_3/etched GaN. An optimal PDA temperature of 500°C was found when performed under N_2, in which hysteresis is minimal and V_{FB} is not further reduced. Hysteresis is correlated to the reduction of hydroxyl groups and GaO_x whereas V_{FB} is correlated to the fluorine reduction. However, over 500°C in PDA, Al_2O_3 starts to degrade with an increased hysteresis and an onset of crystallization is noticed only for the Al_2O_3/etched GaN. With both the POR etching process (Q1) and the optimal PDA temperature, the interface states density is minimal. In terms of integration in the fabrication flow, the low thermal stability of Al_2O_3 limits the thermal budget of subsequent steps such as contact fabrication. That is why the contact annealing is kept at a temperature below 600°C.

In perspective, it would be interesting to integrate the analysis of the interface states using the conductance method with the extracted gate bottom and sidewall mobility in order to understand the impact of etching on the Coulomb scattering.

The low thermal stability of Al_2O_3 and the impact of the etched substrate motivates the study of alternative dielectrics such as AlSiO and AlON in order to increase the thermal stability and reach lower electron trapping. These alternative dielectrics will be discussed in the following chapters.

4

Study of AlSiO for high-temperature Post-Deposition Anneal on GaN : Benefits and challenges

This chapter aims to present the study of $Al_{0.5}Si_{0.5}O_x$ with or without interfacial SiO_2 for high-temperature Post-Deposition Anneal. In the first section, the electrical and physical-chemical properties of $Al_{0.5}Si_{0.5}O_x$ for the different PDA temperatures are discussed. A higher thermal stability than Al_2O_3 is observed. The optimal temperature is found at 750°C in which both stable AlSiO layer and interface are maintained while the hysteresis is reduced. Over 750°C, the AlSiO starts to crystallize and interfacial GaO_x is noticed. In the second section, the introduction of an interfacial SiO_2 layer is investigated in order to further increase the thermal stability of AlSiO. Annealing at 950°C is found to be the optimal temperature in which the hysteresis is the lowest when compared to AlSiO without SiO_2 while maintaining a higher V_{FB}. Nonetheless, both the AlSiO and the AlSiO/SiO_2 stack suffer from reversed hysteresis linked to mobile charges in the form of Na^+/K^+ impurities.

Contents

4.1 $Al_{0.5}Si_{0.5}O_x$/GaN stack

Considering the limited thermal budget that can be applied on Al_2O_3 and how it hinders further reduction of defects with annealing, AlSiO is a promising alternative for Al_2O_3. In fact, as described in **Section 1.4.2.2**, AlSiO is interesting for two main reasons: the reported lower defect at the interface and in the dielectric [149]–[151] and the higher thermal stability allowing higher temperature processes [150], [159].

Moreover, increasing the Si content in AlSiO was reported to further reduce hysteresis and increase the conduction band offset [152], [153]. If the beneficial impact of PDA was studied for low Si content (21%) [159], the same was not performed on higher Si concentration. Therefore, in this section, the study of $Al_{0.5}Si_{0.5}O_x$ with different PDA temperatures will be discussed in comparison with Al_2O_3 without annealing. An optimal PDA temperature is found at 750°C.

4.1.1 Experimental details

19 nm AlSiO layers and 30 nm Al_2O_3 were deposited by ALD on as-grown (0001) oriented n-GaN buffer layers with a Si doping concentration of 5×10^{17} cm $-$ 3. The n-GaN buffer layers were grown on p-Si (111) substrates by MOCVD. The Al_2O_3 reference sample was also deposited on an as-grown GaN substrate in order to exclude the impact of GaN etching. Before dielectric deposition, the GaN surface was cleaned with a wet sequence containing HF. For deposition, the ALD precursors for AlSiO were TMA, tris(dimethylamino)silane (TDMAS), and ozone, while for Al_2O_3 the precursors were TMA and H_2O. For AlSiO, 50% of Si content with respect to Al was obtained with a supercycle approach in which thin layers of SiO_2 and Al_2O_3 were deposited alternatively. The thicknesses of AlSiO and Al_2O_3 were selected in order to have the same oxide capacitance and the deposition temperature was 300°C. After deposition, the wafer was cut into 1.5×1.5 cm^2 samples which underwent PDA in an RTP oven for 3 min under N_2 at 650°C, 750°C, 850°C, or 950°C. These temperatures were selected in order to compare with the work of Kikuta et al. [159] and validate the AlSiO deposition and annealing. Then, circular MOSCAP structures on coupons presented in **Section 2.1.2** were fabricated, the process flow being summarized in **Figure 4.1**.

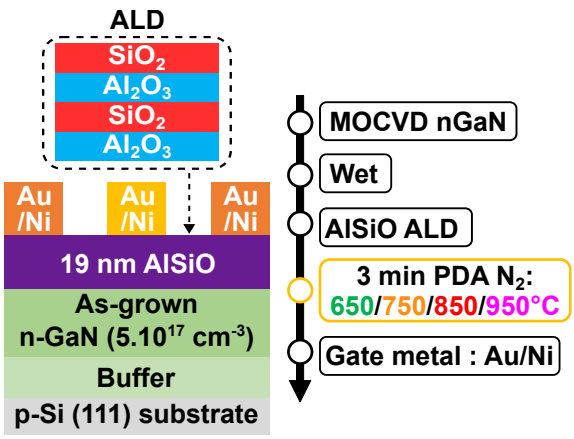


Figure 4.1: AlSiO MOSCAPs process flow with different PDA temperatures

C-V measurements were performed on these samples at 1 kHz with a forward voltage sweep between -4 V and 6 V and a backward voltage sweep between 6 V and -4 V. They were measured at 25°C, 150°C and 200°C. BTS measurements were carried out by stressing the gate with ± 1.8 V at 200°C for 10 min, as described in **Section 2.2.4.2**. The AlSiO layers were analyzed by TEM, Energy-dispersive X-ray spectroscopy (EDX) and ToF-SIMS. The AlSiO's interface with GaN was also analyzed by ToF-SIMS and Angle-Resolved Hard X-ray Photoelectron Spectroscopy (AR-HAXPES) (cf. spectra for AR-HAXPES in **Annex C**, **Figure A.3**). Both negative and positive ions were analyzed by ToF-SIMS. The 50% Si with respect to Al was confirmed with HAXPES quantification at the take-off angle of 75°, as shown in **Table 4.1**.

PDA temperature	O (at%)	Al (at%)	Si (at%)	$100 \times Si/(Al+Si)$ (%)
w/o PDA	64.8	17.7	17.5	50
650°C	65.8	16.9	17.4	49
750°C	64.7	17.7	17.6	50
850°C	64.4	17.6	18.1	49
950°C	65.3	16.1	18.6	46

Table 4.1: Atomic percentage for O, Al, Si, and Si ratio with respect to Al by using quantification with HAXPES. The silicon content stays around 50%.

4.1.2 Results and discussion

Two trends regarding the PDA temperatures were observed on the AlSiO samples. For a PDA temperature under 750°C, a stable AlSiO with reduced hysteresis is noticed, whereas, for a PDA temperature over 750°C, a degraded AlSiO/GaN stack is observed.

4.1.2.1 Annealing under 750°C: reduced hysteresis

For a measuring temperature of 25°C, the *C-V* and G_m/ω characteristics for the Al_2O_3 reference sample and for the AlSiO samples with a PDA under 750°C are represented in **Figure 4.2**. No significant conductance peak associated with interface states is observed, which is in accordance with the absence of etching on the GaN surface as observed with Al_2O_3/etched GaN gate stack (cf. **Section 3.2**). Thus the interface states density is under 10^{10} $eV^{-1}.cm^{-2}$.

In **Figure 4.3**, the extracted V_{FB} and hysteresis are represented. AlSiO has a lower V_{FB} than Al_2O_3 and it is further reduced with the PDA. Concerning hysteresis, all samples present a clockwise hysteresis, with AlSiO without PDA having a slightly lower hysteresis than the Al_2O_3 reference sample. The hysteresis is reduced with increasing PDA temperature, reaching a minimum of 78 mV. This minimum is higher than the minimum of 56 mV found for Al_2O_3 on etched GaN after annealing at 500°C (cf. **Section 3.2.2.1**). Considering that etching increases the hysteresis [63] and that both the Al_2O_3/etched GaN and the AlSiO/as-grown GaN gate stack have the same wet cleaning, the higher hysteresis for the AlSiO after a PDA at 750°C seems to indicate that more electron traps are present in AlSiO even after a high-temperature PDA. However, this difference can be explained by a higher electric field applied on the AlSiO samples due to AlSiO's lower thickness.

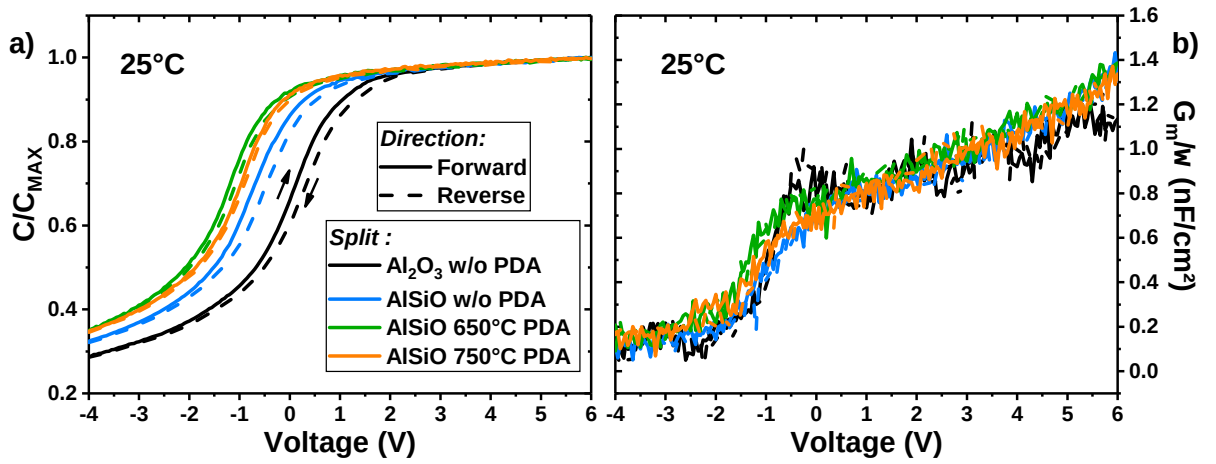


Figure 4.2: a) Normalized C-V measurements (median of five measurements) and b) G_m/ω measurements (single measurement) of Al_2O_3 without PDA, AlSiO without PDA, with 650°C and 750°C PDA.

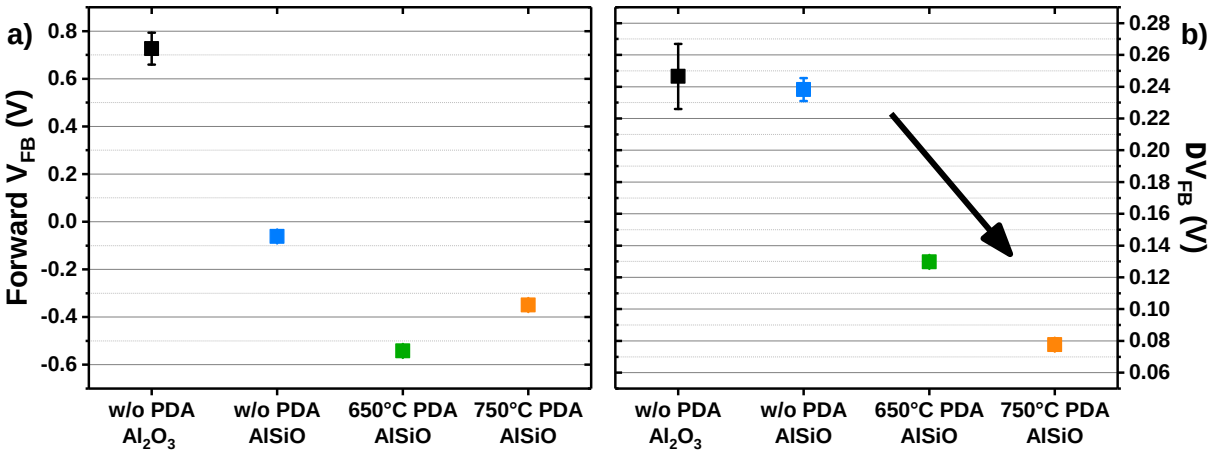


Figure 4.3: Extracted a) V_{FB} and b) ΔV_{FB} (median of five measurements) at 25°C for Al_2O_3 without PDA, AlSiO without PDA, with 650°C and 750°C PDA.

As represented in the **Table 4.2**, the extracted permittivity is around 5.6∼5.9, which is coherent with the values reported by Kikuta et al. [153] for Si content close to 50%. This value is as expected between the Al_2O_3 (8∼10) and SiO_2 (3.9).

Al_2O_3	$Al_{0.5}Si_{0.5}O_x$		
w/o PDA	w/o PDA	650°C	750°C
9.39±0.08	5.9±0.03	5.71±0.05	5.61±0.03

Table 4.2: Relative permittivity for Al_2O_3 and $Al_{0.5}Si_{0.5}O_x$ at different PDA temperatures (median of five measurements).

As for PDA on Al_2O_3/etched GaN, the trend of V_{FB} can be partially explained by the presence of fluorine in the gate stack. In **Figure 4.4.a)**, the F^- depth profile is reduced and increases slightly after a PDA at 750°C. By integrating the depth profile over the gate stack, the content of fluorine was qualitatively extracted and represented as a function of V_{FB} (cf. **Figure 4.4.b)**).

The reduction of hysteresis with PDA for AlSiO can be partially explained by the decrease of hydroxyl groups [75]. The OH^- profile intensity in **Figure 4.5.a)** is reduced with increasing PDA temperature.

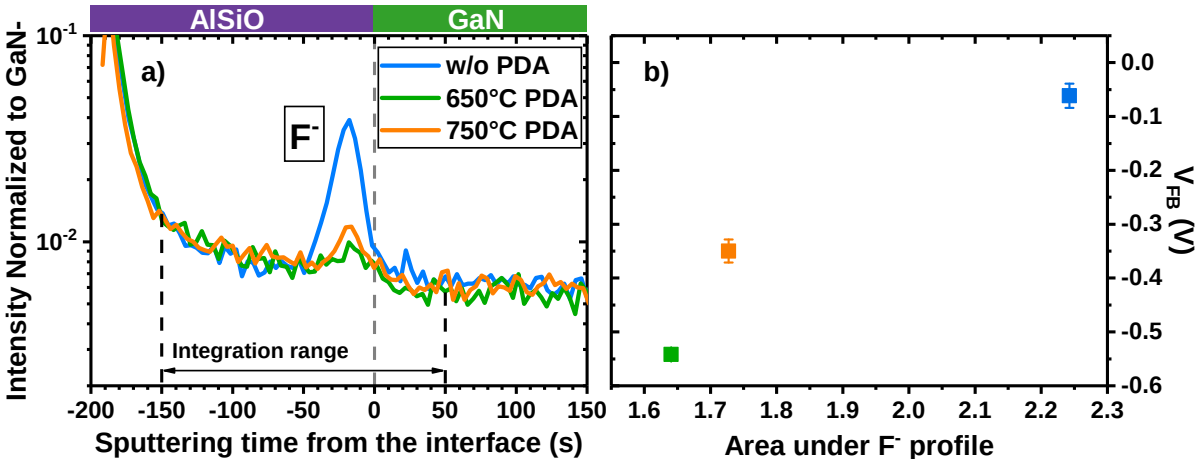


Figure 4.4: a) Normalized ToF-SIMS depth profiles of F^- for AlSiO without PDA, with 650°C and 750°C PDA; b) Integrated area under fluorine profiles for a defined range as a function of V_{FB}.

As stated in the previous chapter, hydroxyl groups have a +1/-1 transition level in Al_2O_3 that is close to GaN's conduction band [83]. Other defects could also be reduced such as Oxygen Vacancies (V_O) commonly found in oxides. Chokawa et al. have indeed reported by ab-initio calculation the neutralization of the charge state for V_O in AlSiO after annealing, by incorporating them within a SiO_2 configuration [155]. PDA could also reduce different border traps [140][135]. Contrary to Al_2O_3 on etched GaN, the trend observed for hysteresis cannot be associated with a reduction of GaO_x since the interface is relatively stable even at 750°C, as observed with the non-variation of $^{71}Ga^-$ profile with PDA temperature in **Figure 4.5.b)**. The ToF-SIMS analyses also highlight a uniform and stable Si distribution throughout the AlSiO layer at the different PDA temperatures (cf. **Figure 4.5.a)**). Consequently, this study demonstrates that AlSiO has a thermal stability higher than Al_2O_3 since the layer does not present a degradation even after a PDA at 750°C [140].

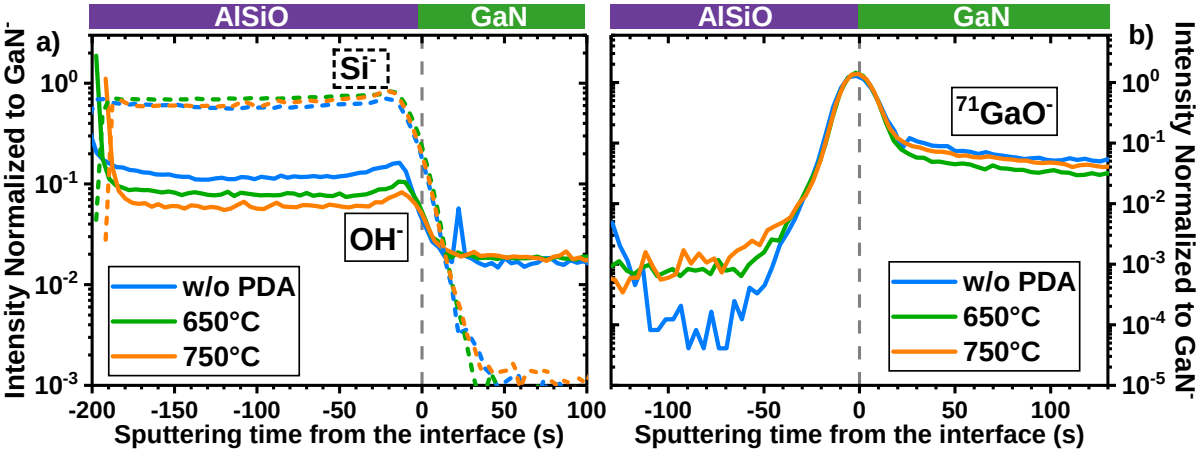


Figure 4.5: Normalized a) ToF-SIMS depth profiles of OH^- and Si^-, and b) ToF-SIMS depth profiles of $^{71}GaO^-$ for AlSiO without PDA, with 650°C and 750°C PDA. Reduced hydroxyl groups are noticed with increasing PDA temperature, while the interface and the layer stay stable.

4.1.2.2 Annealing over 750°C: Degraded AlSiO/GaN stack

However, with a PDA temperature over 750°C, the AlSiO/GaN stack starts to be degraded. In **Figure 4.6**, the presence of a reversed hysteresis is observed on the *C-V* characteristic measured for the 850°C PDA

sample. This will be further discussed in the following subsection. Moreover, no specific conductance peak is observed after an 850°C PDA. Concerning the 950°C PDA sample, no *C-V* measurement could be done because of a large leakage current induced by crystallization.

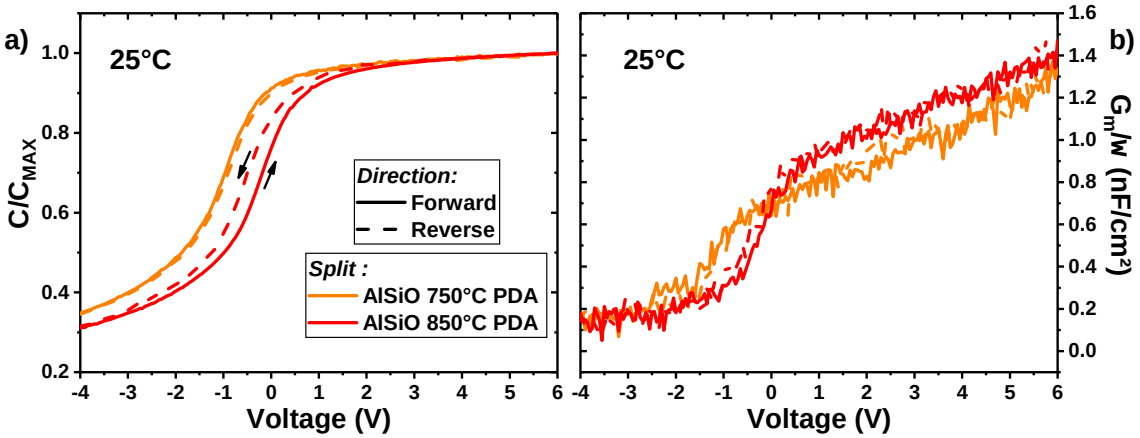


Figure 4.6: a) Normalized C-V measurements (median of five measurements) and b) G_m/ω measurements (single measurement) of AlSiO with 750°C and 850°C PDA. No C-V measurements are shown for 950°C PDA because of the large leakage current, due to crystallization of AlSiO (cf. ***Figure 4.7****).*

While crystallization is not observed in GIXRD analysis after 950°C PDA (cf. in **Annex C**, **Figure A.2**), crystallized regions in the AlSiO layer can be observed in the TEM images (cf. **Figure 4.7**) in the 950°C PDA sample. The boundaries between these large crystallized regions would constitute leakage current paths in the oxide, making the extraction of *C-V* characteristics difficult. Nonetheless, crystallization starts at 850°C with fewer and smaller crystallized regions being observed in the TEM images (cf. **Figure 4.7**). This onset of crystallization however does not induce large leakage current. Since the TEM images were performed to understand the degradation for a PDA temperature higher than 750°C, only the 850°C and 950°C PDA samples were analyzed together with the reference sample. Compared to the literature, our onset of crystallization is lower than the onset observed by Kikuta et al. and Ito et al. found at 950°C [159], [160]. The difference could be associated with a different oxygen source (for them: O_2 plasma) leading to lower oxygen content in our case (O_3). In fact, for HfO_2 on Si, an excess of Hf in the oxide (lower O content) was associated with a lower crystallization temperature [258]. The excess of Hf would lead to higher sources of energy stored in the dielectric, leading to its lower crystallization temperature. Another possibility for earlier crystallization could be the surface preparation or the metal deposition.

The onset of degradation at 850°C is also observed in terms of Si segregation. As represented in **Figure 4.8.a)**, the Si starts to accumulate at the AlSiO/GaN interface after an 850°C PDA. This accumulation is confirmed by EDX analyses in **Figure 4.8.b)** for 950°C PDA in which Si accumulates at both Ni/AlSiO and AlSiO/GaN interfaces, while Al depletes from both interfaces. Since the 950°C PDA sample is crystallized, the EDX analyses do not further degrade the layer and a comprehensive analysis is possible, even though the resolution is lower with EDX. This Si segregation at both sides of the AlSiO is also observed in the Si^- ToF-SIMS depth profile.

As the layer starts to degrade at 850°C, the interface is also affected by this PDA temperature range. As observed in **Figure 4.7**, an interfacial layer appears after an 850°C PDA and further grows at higher PDA

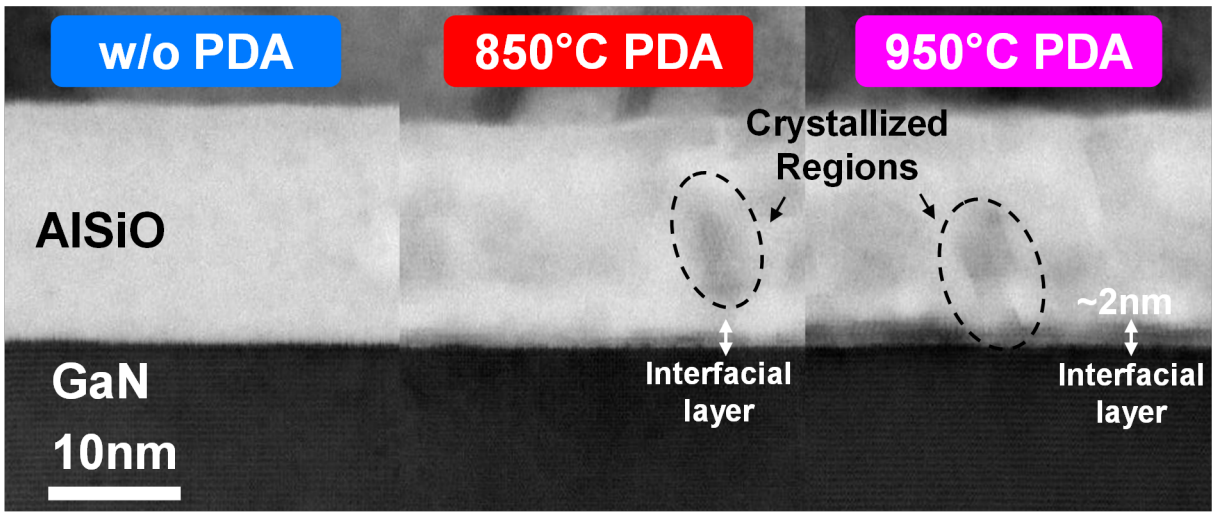


Figure 4.7: TEM images for AlSiO samples without and with PDA at 850°C and 950°C. Both PDA samples present crystallized regions and interfacial layers. The 950°C PDA sample has a thicker interfacial layer and more crystallized regions than the 850°C sample.

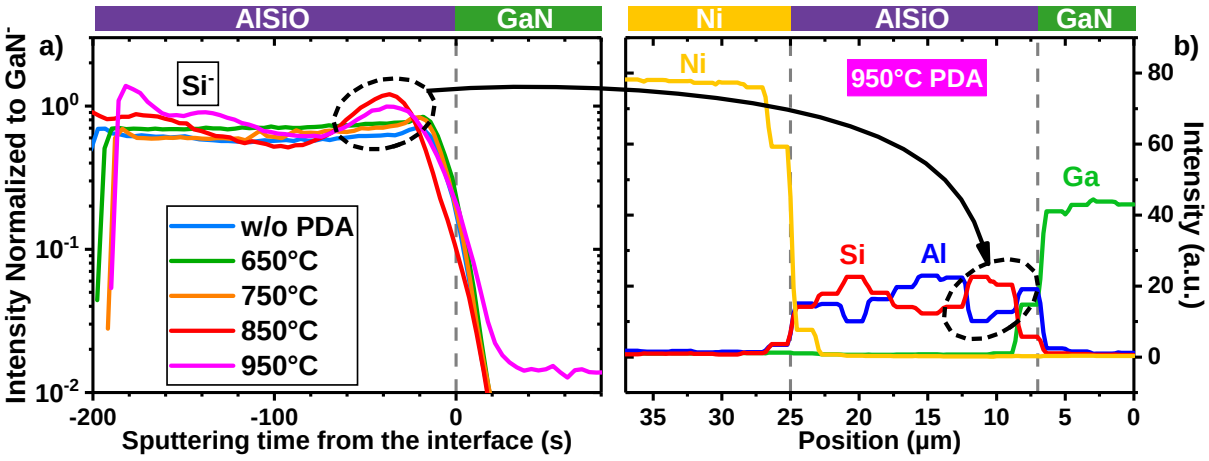


Figure 4.8: a) ToF-SIMS depth profiles of OH- and b) EDX analyses for AlSiO with 950°C PDA. The silicon accumulates at the AlSiO/GaN similarly to the accumulation observed in the EDX analyses.

temperatures up to 2 nm. This layer can be associated with GaO_x or $SiGaO_x$ observed both in ToF-SIMS and AR-HAXPES analyses. The $^{71}GaO^-$ profile in **Figure 4.9** starts to widen towards the AlSiO layer at 850°C. With AR-HAXPES, the extracted GaO_x thickness (cf. **Figure 4.10**) also starts to increase at 850°C PDA, with a thickness higher than 1 nm and reaching 2.5 nm at 950°C. A similar onset of GaO_x growth is observed for thermally oxidized GaN when the annealing temperature is over 750°C [110]. Likewise for SiO_2 and $HfSiO_x$ [259], [260], AlSiO does not prevent GaO_x growth at the interface that inevitably starts after an annealing at 750°C. Moreover, GaN's orientation could also influence oxidation. In fact, Sayed et al. have reported an intermixing between Ga and the gate oxide for AlSiO deposited by MOCVD at 700°C and only on (0001) oriented GaN substrates [161], similarly to our GaN substrate surface orientation. This reported intermixing could also confirm a possible intermixing between Si and GaO_x since Si is segregated at the AlSiO/GaN interface.

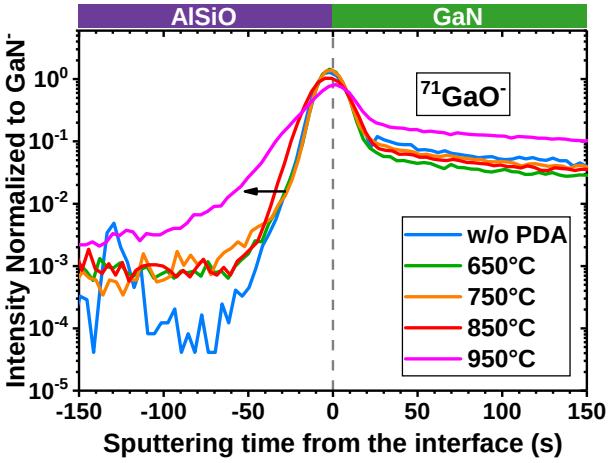


Figure 4.9: Normalized ToF-SIMS depth profiles of $^{71}GaO^-$. The profile extends towards AlSiO for PDA temperatures higher than 750°C.

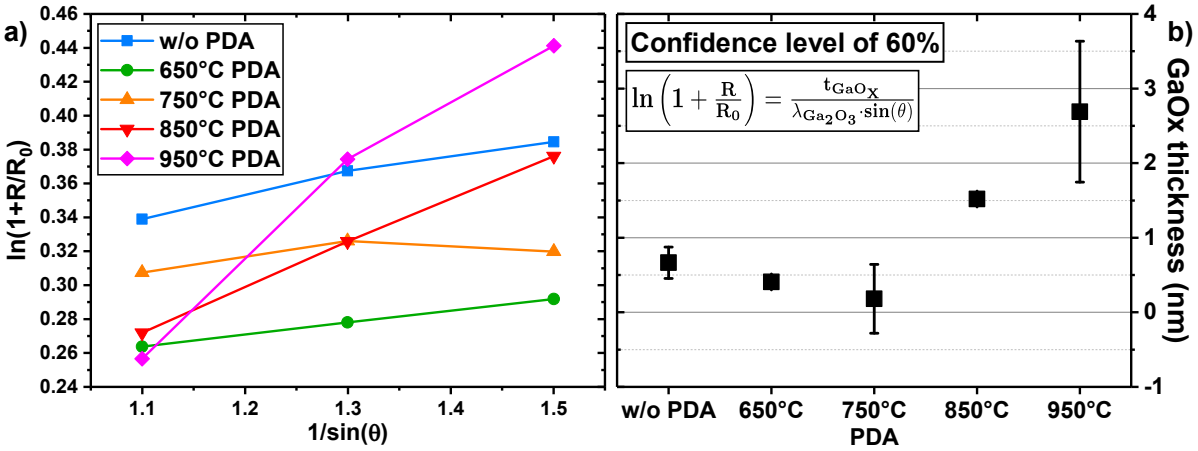


*Figure 4.10: a) $ln(1+R/R_0)$ as a function of $1/sin(\theta)$ and b) GaO_x thickness extracted from varying the HAXPES take-off angle between 42/50/65°. The increased GaO_x thickness after 750°C PDA correlates to the extended $^{71}GaO^-$ profile in **Figure 4.9**.*

Therefore, for a PDA over 750°C, the AlSiO/GaN stack starts to be degraded with an onset of crystallization at 850°C, an atomic Si segregation at the AlSiO/GaN interface, and an interfacial GaO_x growth. Electrically, the 950°C PDA sample has a large leakage current impeding proper *C-V* measurements whereas for the 850°C PDA sample a reversed hysteresis is observed.

4.1.2.3 Reversed hysteresis

To understand the origin of the reversed hysteresis observed in **Figure 4.6**, *C-V* characteristics were measured at higher temperatures such as 150°C and 200°C. As represented in **Figure 4.11** and in the extracted hysteresis in **Figure 4.12.a)**, the reversed hysteresis is increased for the 850°C PDA sample when the measuring temperature increases from 150 to 200°C. But the other AlSiO samples have a reversed hysteresis when the measuring temperature is increased, until it becomes negative for all samples at 200°C. For the reference Al_2O_3 without PDA, the hysteresis is increased with the measuring temperature due to increased electron trapping at the higher measuring temperature. Therefore, the reversed hysteresis is only observed in the AlSiO samples.

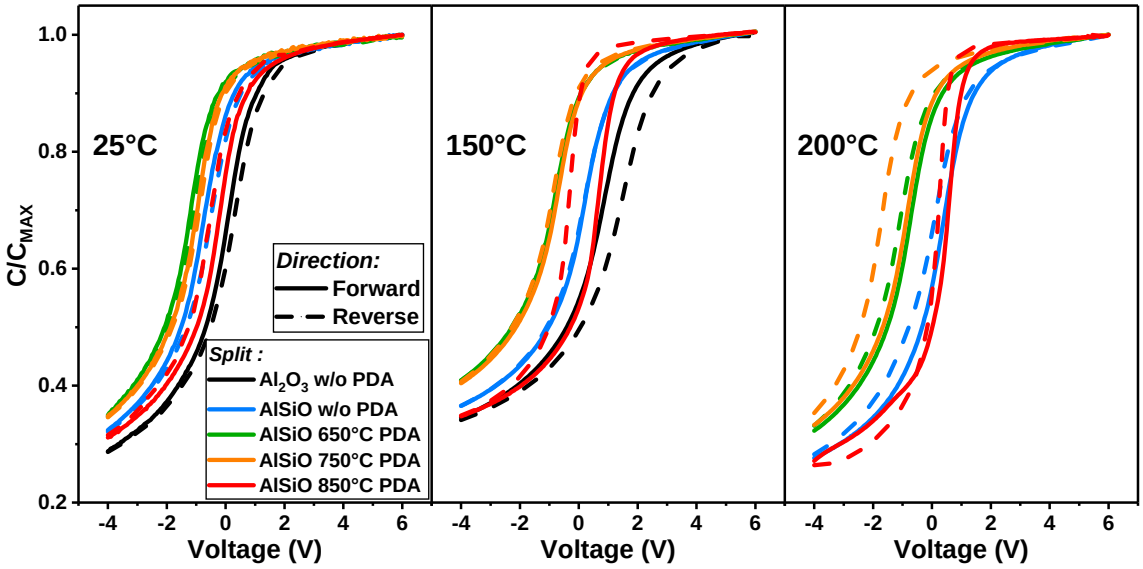


Figure 4.11: C-V measurements (median of five measurements) at 25°C, 150°C and 200°C measuring temperatures.

Since this phenomenon is thermally activated, one possible explanation is the presence of positive mobile charges. These charges are typically associated with positive alkaline species (e.g. H^+, Li^+, Na^+, and K^+), and their drift inside the oxide is increased with the measuring temperature [183]. At room temperature, their movement is hindered and an absence of reversed hysteresis is observed for all AlSiO samples with a PDA under 750°C. However, for the 850°C PDA samples, the presence of a reversed hysteresis for all measuring temperatures, especially at room temperature, seems to be partially explained by the small crystallized regions observed in **Figure 4.7**. These regions could increase the drift of mobile ions at room temperature, allowing the presence of reversed hysteresis [261]. The presence of reversed hysteresis in AlSiO was also reported by Sayed et al. for a Si content of 76%, without PDA, and deposited by MOCVD on a $(000\bar{1})$ oriented n-GaN [152]. Interestingly, the reversed hysteresis is observed at room temperature, with the authors also mentioning the possible presence of mobile charges.

To quantify the amount of mobile charges, BTS measurements were performed on the samples without PDA (stable AlSiO) and with a PDA at 850°C (degraded AlSiO). As represented in **Figure 4.12.b)**, similar amounts of mobile charges in the order of 2.3×10^{12} cm^{-2} were extracted. Thus, a similar origin of mobile charges is expected to be found in both stable (from no PDA to PDA up to 750°C) and degraded AlSiO samples (PDA over 850°C). Moreover, the annealing does not reduce the amount of

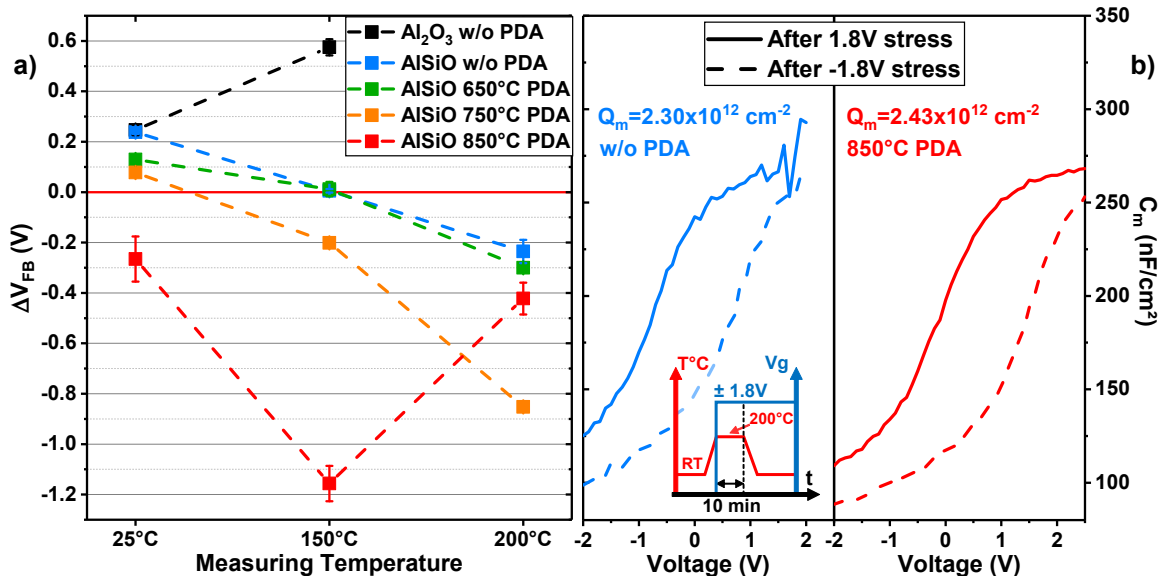


Figure 4.12: a) Extracted ΔV_{FB} (median of five measurements) from C-V measurements. Increasing the measuring temperature reveals reversed hysteresis for all AlSiO samples; b) BTS measurements on AlSiO samples without PDA and with 850°C PDA. A similar amount of mobile charges is calculated for the AlSiO samples without PDA and with 850°C PDA.

mobile charges, but rather reveals a more significant reversed hysteresis, e.g. for the 750°C PDA sample. One hypothesis to explain this impact of PDA temperature is the reduction of electron traps discussed in **Section 3.2.2.1**. By reducing the amount of electron traps, lower negative charges in the form of trapped electrons can counterbalance the positive mobile charges. Therefore, at the measuring temperature of 200°C, the higher negative hysteresis for higher PDA temperatures could be associated with electron traps being reduced with a higher PDA temperature.

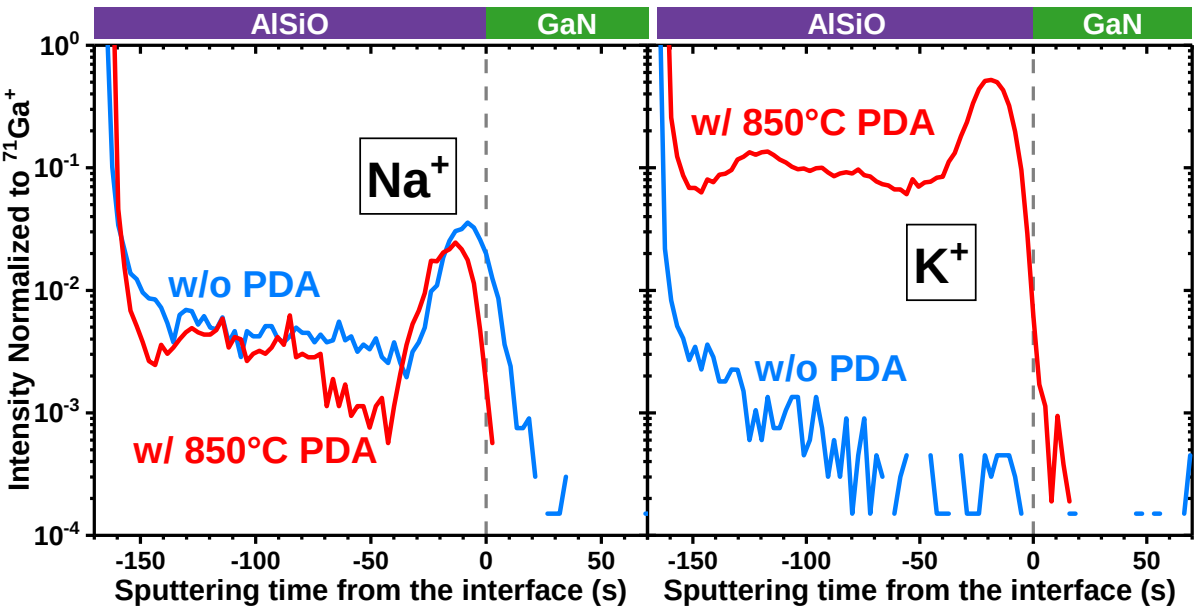


Figure 4.13: Normalized ToF-SIMS depth profiles of K^+ and Na^+ on AlSiO samples without and with 850°C PDA. Both samples have Na^+ and K^+ contamination.

Finally, positive ions were analyzed by ToF-SIMS analysis in order to find a possible origin for the mobile charges, typically alkaline ions. The results represented in **Figure 4.13** highlight the presence of both Na^+ and K^+ impurities in the AlSiO samples without PDA and with a PDA at 850°C. For Na^+, the PDA does not affect the profile, with Na^+ being found even without PDA. This seems to indicate that the sample is contaminated with Na^+ before or during deposition. On the contrary, K^+ is not found before PDA but present after a high-temperature PDA, meaning that the source of K^+ could be found during or after the annealing. Since both Na^+ and K^+ ions have a similar secondary ion yield and that similar amounts of mobile charges are observed in the samples, K^+ seems to not be the primary cause for mobiles charges. Otherwise, the increase in K^+ after a 850°C PDA would lead to an increase in the amount of mobile charges. Therefore, the most probable explanation for reversed hysteresis in AlSiO is the presence of mobile charges in the form of Na^+ and K^+ impurities. Their source is associated to the process environment, such as the handling of the samples or other steps [183]. But in particular, the wet sequence can be ruled out since it does not contain Na and/or K species. A more clean process environment, such as in fabrication, is necessary to address this issue.

4.1.3 Conclusions

The impact of Post-Deposition Anneal on AlSiO with 50% of Si content with respect to Al was evaluated. A thermally stable AlSiO layer and interface with GaN is observed up to 750°C, which is higher than Al_2O_3 on etched (cf. **Section 3.2**) and as-grown GaN [140]. Moreover, the increase in PDA temperature also reduced V_{FB} hysteresis until 750°C thanks partially to the reduction of hydroxyl groups and other defects. Similar hysteresis is observed between AlSiO and Al_2O_3 without annealing, but compared to the Al_2O_3/etched GaN with a 500°C PDA (cf. **Section 3.2**) AlSiO with a 750°C PDA has a slightly higher hysteresis. A decrease of V_{FB} is also observed compared to Al_2O_3 and further reduces with increasing PDA temperature partially due to the reduction of fluorine. Over 850°C in PDA temperature, a degraded AlSiO/GaN stack is noticed, with both the onset of crystallization for AlSiO and interfacial GaO_x growth. Consequently, an optimal PDA temperature for AlSiO with 50% Si deposited on as-grown GaN is found for 750°C. Nonetheless, the presence of mobile charges in the form of Na^+/K^+ needs to be addressed. As proposed by Ito et al. [160], the introduction of a thin SiO_2 interfacial layer in order to increase AlSiO thermal stability will be discussed in the next section.

4.2 Introduction of SiO_2 interfacial layer

In this section, the introduction of a SiO_2 layer between the AlSiO layer and the GaN substrate will be presented for different PDA temperatures. Thanks to the increased thermal stability of AlSiO with SiO_2 [160], an optimal PDA temperature is found at 950°C with a lower hysteresis and a higher V_{FB} than the optimal PDA temperature without SiO_2 (750°C).

4.2.1 Experimental details

15 nm AlSiO layers (50 %Si) with a 2 nm interfacial layer of SiO_2 were deposited by ALD and PE-ALD respectively on the same as-grown substrate as in the previous section. The fabrication is in every aspect

similar to the previous section, the difference being the introduction of SiO_2 at the AlSiO/GaN interface. Concerning the SiO_2 deposition, the PE-ALD precursors for Si and O were Bis(diethylamino)silane (BDEAS) and an O_2 plasma respectively, and the deposition temperature was 50°C. This precursor and low temperature deposition were chosen to avoid GaN oxidation during the deposition, as observed in Ge [262]. The process flow is summarized in **Figure 4.14**. *C-V* measurements were performed on these samples at 1 kHz with a forward voltage sweep between -4 V and 6 V and a backward voltage sweep between 6 V and -4 V. They were measured at 25°C and 150°C. Interface states densities were extracted at both measuring temperatures using the abacus used for the conductance method presented in **Section 2.2.3.2**. ToF-SIMS analyses were performed with both negative and positive ions collected. To have the same ToF-SIMS analyses conditions, AlSiO samples were again measured alongside the AlSiO/SiO2 samples.

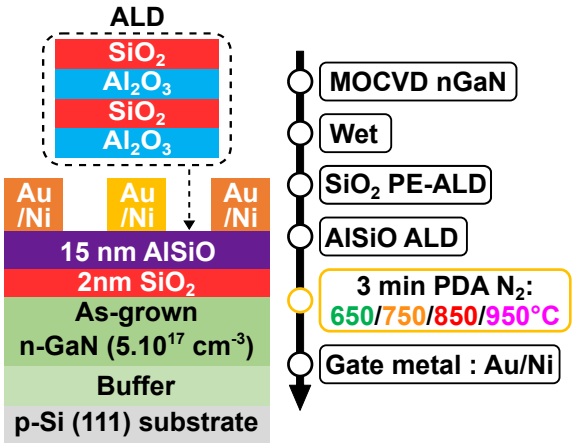


Figure 4.14: AlSiO/SiO_2 MOSCAPs process flow with different PDA temperatures

4.2.2 Results and discussion

Figure 4.15 reports the *C-V* and G_m/ω characteristics at 25°C and 150°C for the AlSiO/SiO_2 samples at different PDA temperatures, alongside the reference Al_2O_3. A first observation is the presence of *C-V* for the sample annealed at 950°C. This means that the introduction of SiO_2 either avoids the formation of a leakage path through the gate stack, probably by reducing the crystallization of AlSiO as reported by Ito et al. [160]. The introduction of SiO_2 deposited at a low temperature also introduces interface states, represented by the presence of conductance peaks for the samples without or with a PDA under 750°C. Further increasing of the PDA temperatures reduces these peaks. For a PDA temperature over 750°C, negative hysteresis is noticed for the AlSiO/SiO_2 when the measuring temperature is raised to 150°C. Interestingly, the hysteresis is increased for the samples with a PDA temperature under 750°C.

By considering the extracted V_{FB} and its hysteresis in **Figure 4.16**, increasing the PDA temperature reduces V_{FB} and ΔV_{FB} for all AlSiO/SiO_2 samples, revealing a negative hysteresis at 150°C for both 850 and 950°C samples. AlSiO/SiO_2 samples generally have a higher V_{FB} than the Al_2O_3 and AlSiO samples. However, this is also observed for hysteresis, in which an annealing of 850°C is necessary to reduce it down to the Al_2O_3 hysteresis. The higher amount of traps is further confirmed with hysteresis increase when extracted at 150°C. Therefore, on one hand, the introduction of interfacial SiO_2 improves the thermal stability and increases V_{FB}, but on the other hand, it introduces interface states and traps in

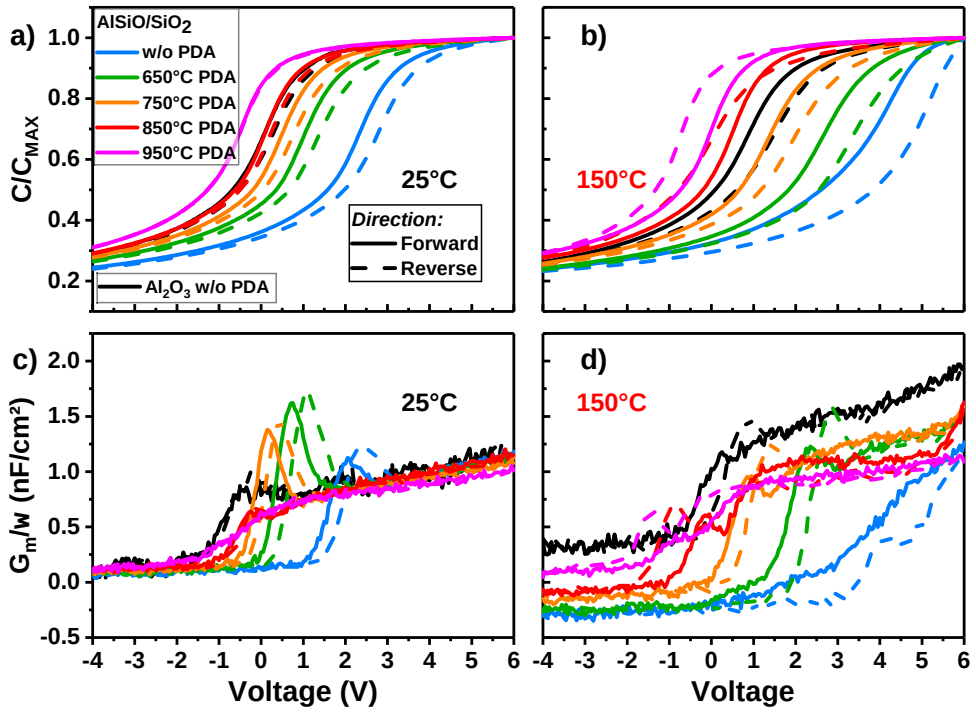


Figure 4.15: Normalized C-V characteristics for Al_2O_3 without PDA and $AlSiO/SiO_2$ samples on as-grown GaN with PDA at the measuring temperatures of a) 25°C and b) 150°C (median of five measurements); G_m/ω characteristics at c) 25°C and d) 150°C (single measurement).

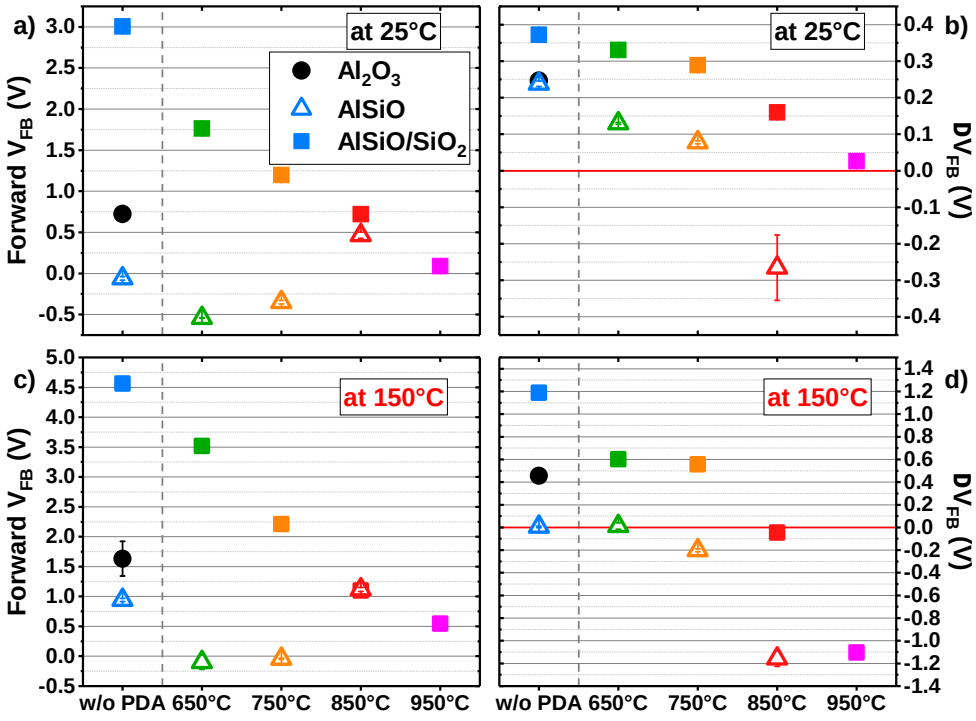


Figure 4.16: For the different PDA temperatures on AlSiO and $AlSiO/SiO_2$: a,b) Extracted forward V_{FB} and ΔV_{FB} (median of five measurements) at 25°C; c,d) Extracted forward V_{FB} and ΔV_{FB} (median of five measurements) at 150°C.

the gate oxide increasing the hysteresis. Nonetheless, disregarding the negative hysteresis at 150°C, the PDA at 950°C is an interesting temperature to consider since it leads a lower hysteresis and higher V_{FB} than for AlSiO with a PDA temperature of 750°C (26 mV and 78 mV respectively). Moreover, at this PDA temperature of 950°C, the conductance peak is further reduced.

Thanks to ToF-SIMS analyses in **Figure 4.17.a)**, the reduction of hydroxyl groups with PDA temperature is also observed for AlSiO/SiO_2 when increasing the PDA temperature, partially explaining the reduction of ΔV_{FB}. In addition, the amount of hydroxyl groups is higher than for the AlSiO samples, the latter having a lower hysteresis. However, at 950°C, an increase of OH^- is observed for the AlSiO/SiO_2, which is not correlated to the lower ΔV_{FB}. Therefore, as discussed previously in **Section 4.1.2.1**, other sources of electron traps being reduced after PDA could be responsible for the decrease in hysteresis. One possibility is the presence of carbon impurities in the SiO_2. As represented in **Figure 4.17.b)**, the C^- profile in the SiO_2 layer is strongly reduced after a PDA at 950°C. Moreover, this C^- peak's intensity follows the trend observed for the conductance peaks in **Figure 4.15** in which the PDA at 650°C and 750°C lead to an increase of conductance peaks. Thus, the presence of carbon could lead to the formation of interface states at the SiO_2/GaN interface.

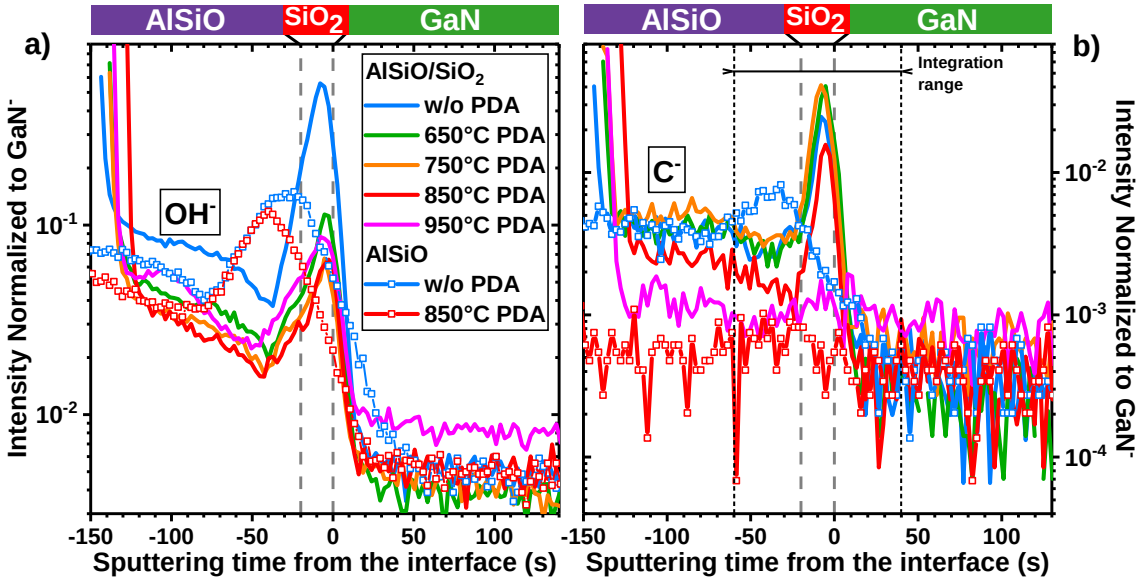


Figure 4.17: Normalized ToF-SIMS depth profiles of a) OH^- and b) C^- for AlSiO/SiO_2 at different PDA temperatures and AlSiO without and with a 850°C PDA. PDA reduces the hydroxyl groups whereas C^- in SiO_2 is reduced only after a 850°C PDA.

To have a better understanding of the amount of carbon in the SiO_2 layer and its impact on the conductance peaks, the C^- profile was integrated within the range represented in **Figure 4.17.b)**, while the conductance peaks at 25°C and 150°C were associated to D_{it} values using the abacus used for the conductance method. Their combination in the semi-log scale is represented in **Figure 4.18**. The high uncertainty with the sample without PDA at 150°C can be explained by a high G_m/ω peak variation among the sample and leakage current covering the peaks. A correlation is found between the increase of carbon and the increase of D_{it}, leading to the understanding that the carbon impurities in SiO_2 deteriorate the SiO_2/GaN interface. A similar observation was made by Shibata et al. where the increase of the carbon concentration in Al_2O_3 was linked to an increase of D_{it} for an Al_2O_3/AlGaN/GaN stack [263]. The presence of carbon in the interfacial SiO_2 layer could be explained by the low deposition

temperature of 50°C and/or the presence of amino ligands (nitrogen bonds with carbon) in the BDEAS precursor [262]. At this temperature, the oxidation rate is reduced compared to depositions at 250°C and 300°C. Nonetheless, annealing at 950°C allows to completely reduce the presence of carbon and the presence of interface states at 25°C. Another possibility to reduce the presence of carbon impurities would be to use a NH_3 plasma before the O_2 [262]. In fact, the NH_3 plasma allows to remove the amino ligands, reducing the presence of carbon impurities.

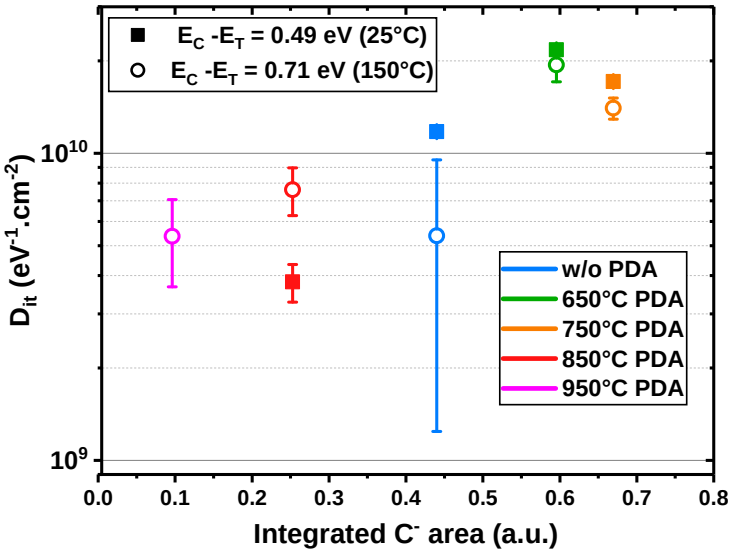


*Figure 4.18: Interface states density extracted at 25°C and 150°C by using the abacus used for the conductance method, with respect to the integrated C^- area within the integration range shown in **Figure 4.17.b)**. Reducing the amount of carbon impurities allows to reduce the amount of D_{it}.*

Another important aspect to evaluate is the stability of the AlSiO layer and interface with GaN after the introduction of SiO_2. In the TEM images of **Figure 4.19**, the SiO_2 has a thickness of 3∼4 nm, which is higher than expected, an AlSiO thickness of around 13 nm. The crystallized regions are only observed for the 950°C PDA sample. This means that the presence of *C-V* characteristics for this sample could be explained only by the presence of the non-crystallized SiO_2, and that the SiO_2 layer indeed increases the AlSiO's thermal stability [160]. **Figure 4.19** also reveals the either the absence or a very thin interfacial layer between SiO_2 and GaN, highlighting a stable interface.

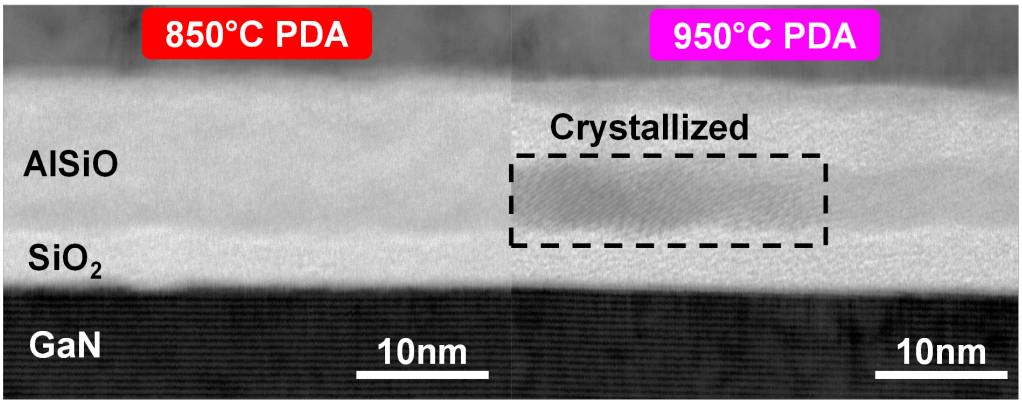


Figure 4.19: TEM images for AlSiO/SiO_2 samples with PDA at 850°C and 950°C. The presence of SiO_2 induces an absence of AlSiO crystallization for the 850°C PDA sample, whereas for the 950°C PDA sample a crystallized region is still present. No interfacial layer is observed.

ToF-SIMS analyses further confirm the previous observations. For Si^- depth profiles represented in **Figure 4.20.a)**, the presence of SiO_2 allows to increase the onset of Si^- segregation from 850°C for AlSiO to 950°C with SiO_2 interfacial layer. Indeed, the peak of Si^- close to the GaN interface is related to SiO_2, but at 950°C the Si^- profile at the AlSiO/SiO_2 interface has a stronger decrease (cf. circle in **Figure 4.20.a)**) than for the lower PDA temperatures. Concerning the SiO_2/GaN interface, the $^{71}GaO^-$ profiles represented in **Figure 4.20.b)** do not highlight a significant widening towards the AlSiO layer, even at 950°C. AlSiO/GaN interface exhibit a broader GaO^- profile than the SiO_2/GaN interface which can be understood as higher oxidation being observed, as supported by the TEM images in **Figure 4.19**. Thus, the introduction of SiO_2 increases the stability of the AlSiO layer and interface with GaN.

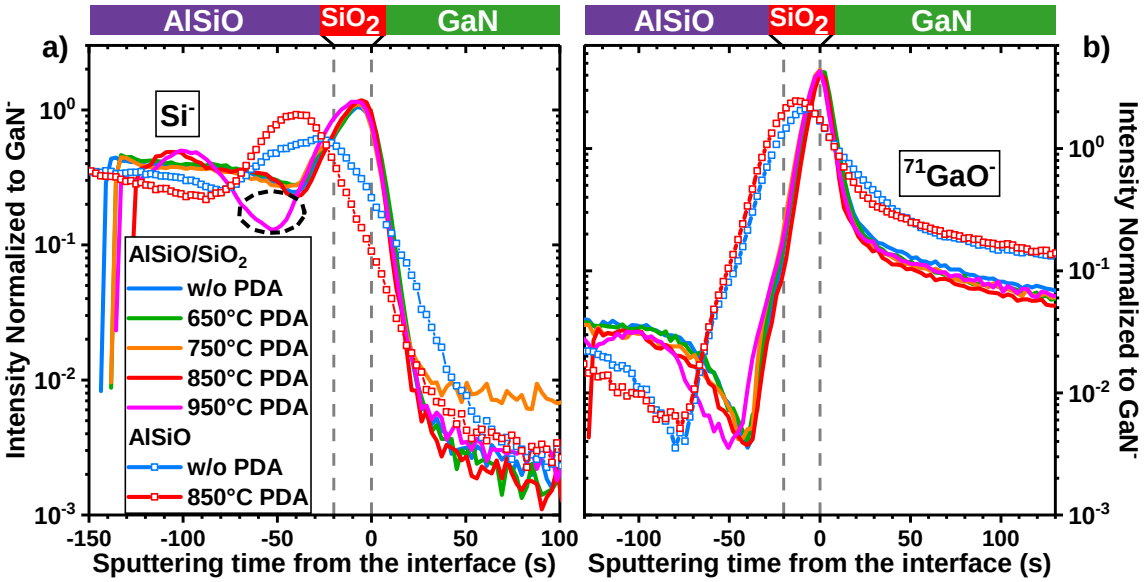


Figure 4.20: Normalized ToF-SIMS depth profiles of a) Si^- and b) $^{71}GaO^-$ for AlSiO/SiO_2 at different PDA temperatures and AlSiO without and with a 850°C PDA. The introduction of interfacial SiO_2 increasse by 100°C the Si stability, while the GaN's interface oxidation is drastically reduced.

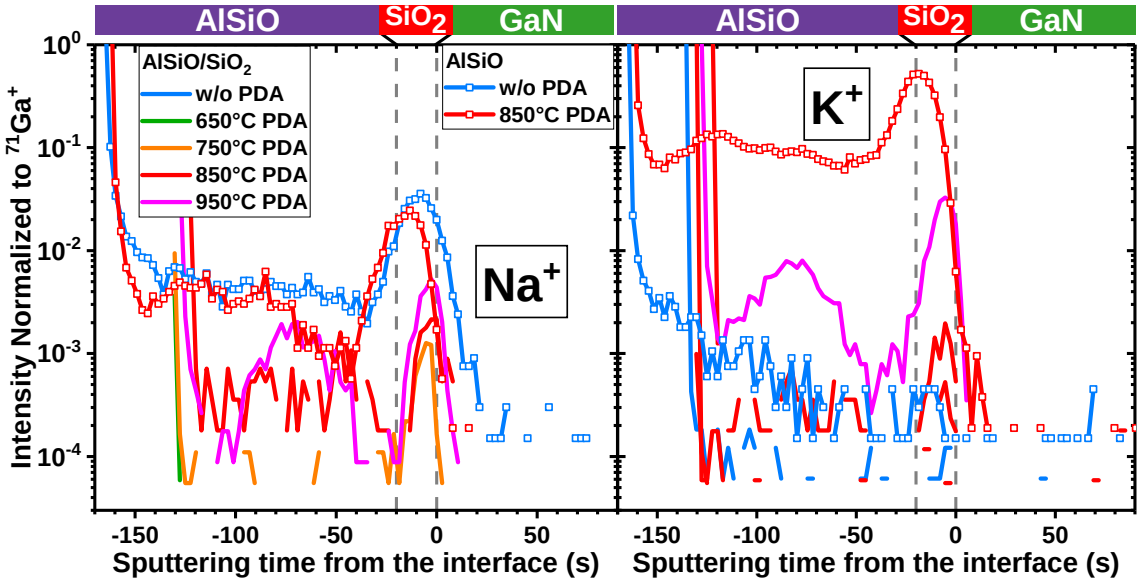


Figure 4.21: ToF-SIMS depth profiles of K+ and Na+ for AlSiO/SiO2 at different PDA temperatures and AlSiO without and with 850°C PDA. Normalized ToF-SIMS depth profiles of K^+ and Na^+ for AlSiO/SiO_2 at different PDA temperatures and AlSiO without and with a 850°C PDA.

Finally, in order to understand the presence of reversed hysteresis for the 850°C and 950°C PDA samples, the Na^+ and K^+ profiles were analyzed by ToF-SIMS analysis (cf. **Figure 4.21**). Na^+ presence is observed after annealing at 850°C and 950°C but at a lower level than for the AlSiO samples. For both samples, the intensity is relatively small (detection limit around 10^{-4}) and it is not clear whether it affects or not the *C-V* measurement with reversed hysteresis. The same observation can be made for K^+ in which the contamination is observed clearly only after a 950°C PDA. Therefore, in the case of the $AlSiO/SiO_2$ samples, the reversed hysteresis could be partially explained by the presence of Na^+ and/or K^+, mostly for the 950°C PDA sample where the presence of these contaminants is slightly higher than for 850°C PDA.

4.2.3 Conclusions

The introduction of a 2 nm interfacial PE-ALD SiO_2 layer to improve the stability of the AlSiO layer was investigated for different PDA temperatures. The higher thermal stability of the dielectric/GaN is confirmed thanks to the addition of SiO_2 with an onset of Si segregation (+100°C) at higher PDA temperature and a lower oxidation at the GaN interface. With MOSCAPs on coupons, at both 25°C and 150°C, the presence of SiO_2 increases both V_{FB} and ΔV_{FB} with respect to Al_2O_3 and AlSiO, with higher hysteresis than 289 mV after a PDA at 750°C. The interface is also electrically degraded with an increase of D_{it} after a PDA at 650°C or 750°C. These poor electrical parameters can be partially explained by a higher amount of traps and the presence of carbon impurities in SiO_2 due to the low deposition temperature of 50°C. However, with PDA above 850°C, hysteresis is reduced and reaches similar values to Al_2O_3 and AlSiO. Moreover, the PDA at 950°C leads to lower hysteresis and higher V_{FB} than the optimal PDA temperature for AlSiO (750°C). However, at this temperature of 950°C, AlSiO still crystallizes. It means that 950°C PDA allows for a good SiO_2/GaN interface quality but that this temperature is too high to preserve AlSiO amorphous properties. Finally, reversed hysteresis is also observed at 150°C for the 850°C and 950°C PDA samples, equally explained by the presence of Na^+ and/or K^+, but in smaller amounts.

4.3 Conclusion of this chapter

The electrical and physical-chemical properties of $Al_{0.5}Si_{0.5}O_x$ with or without an interfacial SiO_2 were investigated at different Post-Deposition temperatures. Without SiO_2, two trends are observed when the PDA temperature is increased. For a PDA under 750°C, the hysteresis is reduced while the AlSiO layer and interface with GaN remain stable with no Si segregation or GaO_x growth. Over a PDA at 750°C, the AlSiO layer and its interface with GaN start to degrade. This is illustrated by an onset of crystallization for AlSiO, a phase separation in AlSiO, and GaO_x growth.

The introduction of SiO_2 increases the AlSiO's thermal stability with an increased temperature onset of Si segregation and no GaO_x growth. However, the low deposition temperature of SiO_2 introduces defects such as carbon impurities, which increases hysteresis and introduces interface states. Annealing above 850°C solves these issues by strongly reducing hysteresis and interface states.

Therefore, on one hand, the optimal PDA temperature for AlSiO is 750°C, and on the other hand, the

optimal temperature for AlSiO/SiO_2 is between 850 and 950°C. Nonetheless, Na^+/K^+ contamination affects the gate stack with reversed hysteresis at high measuring temperatures, especially for high PDA temperatures. Removing them is essential in order to have reliable AlSiO and AlSiO/SiO_2 gate stacks.

In perspective, it would be important to study the influence of Si content in the AlSiO layer with different PDA temperatures. This would help to understand whether the presence of mobile charges is linked to the Si concentration and to assess which Si concentration is more suitable for the gate stack. The 50°C 2 nm PE-ALD SiO_2 interfacial layer can also be very interesting in combination with another upper dielectric layer withstanding PDA temperature of 950°C without crystallization (AlSiO with different Si content, or other alternative), since this study demonstrated good SiO_2/GaN interface properties after annealing at 950°C. The SiO_2 layer could be improved by depositing at a higher temperature or with an NH_3 plasma step in order to reduce the PDA temperature. It would be also interesting to repeat the same study on etched GaN.

5

Development and analysis of AlON for improved Dielectric/GaN interface

This chapter aims to present the development of AlON thin layer deposition by PE-ALD and the analysis of both its electrical and chemical-physical properties, as well as the quality of the AlON/GaN interface. In the first section, the supercycle approach for AlON deposition on etched GaN substrates will be discussed in order to obtain a uniform layer and controllable nitrogen concentration between 1.5 to 7.1 %. Then in the second section, AlON's electrical and chemical-physical properties will be argued for different nitrogen concentrations and as a function of PDA at different temperatures. An optimal AlON/etched GaN for V_{FB} hysteresis and interface states density at both measuring temperatures of 25 and 150°C is found for a nitrogen concentration around $1.5 \backsim 2.6$ *% annealed above 600°C.*

Contents

5.1 Development of AlON by PE-ALD

Similarly to AlSiO, another dielectric that can be an alternative to Al_2O_3 in order to have a higher thermal stability and less electron traps is AlON. As described in **Section 1.4.2.2**, AlON is reported to have lower traps and a better interface with GaN than Al_2O_3 [133], [162], [164], [166], [169], while possibly introducing negative charges that could increase V_{TH}/V_{FB} [163], [166]. The introduction of nitrogen also increases the thermal stability of AlON [162] allowing to use high-temperature annealings.

AlON has been deposited mainly by ALD with different approaches. In the following section, a new PE-ALD approach with AlN oxidation for AlON deposition will be described. This approach could improve the reactivity in the AlN oxidation process, reducing defects in the final AlON layer, while controlling the amount of nitrogen in AlON and maintaining an unoxidized GaN interface. In the second section, the impact of different nitrogen concentrations in AlON will be presented in a first time, and then the impact of annealing for these different nitrogen concentrations will be discussed in order to find the optimization configuration for the AlON/GaN stack.

5.1.1 Experimental details

15 nm AlON layers were deposited by Plasma-Enhanced Atomic Layer Deposition (PE-ALD) with a FlexAL reactor on (0001) oriented n-GaN buffer layers with a Si doping concentration of 5×10^{17} cm^{-3}. The n-GaN buffer layers were grown on p-Si (111) substrates by MOCVD). Before AlON deposition, the substrates were etched by ICP-RIE and ALE and cleaved into 1.5×1.5 cm^2 samples. The GaN surface was etched in order to access directly the impact of etching as for the Al_2O_3/etched GaN gate stack. The samples were then cleaned with HCl for 3 min, rinsed in deionized water, and dried with N_2. As stated in **Section 2.1.2**, the goal of HCl wet cleaning is to reduce the GaO_x before dielectric deposition but HF is preferable due its possible combined reduction of GaO_x and carbon impurities. The PE-ALD precursors for Al, N, and O were TMA, N_2 plasma, and O_2 plasma, respectively. The AlON deposition consists in a supercycle approach where thin AlN layers are oxidized with an O_2 plasma. The PE-ALD cycle for AlN deposition is based on a previous report [264] and consists of a TMA injection step (0.05 s), a purging step with Ar (3 s), an N_2 plasma step (15 s), and a purging step with Ar (3 s). After a given number of AlN cycles (or a given AlN thickness being deposited), an oxidation cycle is performed, consisting of an O_2 plasma step (15 s) and a purging step with Ar (3 s). This oxidation process allows to form an AlON layer. The supercycles sequence and AlON/etched GaN stack are detailed in the figure below. The plasma power was set to 300 W with a chamber pressure of 10 mTorr and the deposition temperature was fixed at 300°C. The PE-ALD sequence and process flow is summarized in **Figure 5.1**.

To study the influence of the AlN thickness on AlON, the total number of AlN cycles was fixed at 240 for all samples and the number of AlN cycles before one oxidation step was set to 60, 30, 15, 12, 8, and 4. To distinguish the different AlON supercycles, the following nomenclature is used : (**X AlN cycles + 1 plasma O_2 cycle)**) × **Y supercycles**. Hence, the corresponding supercycles were **60**x**4**, **30**x**8**, **15**x**16**, **12**x**20**, **8**x**30** and **4**x**60**. In addition to AlON, an AlN reference sample was also deposited by PE-ALD based on a previous report [264].

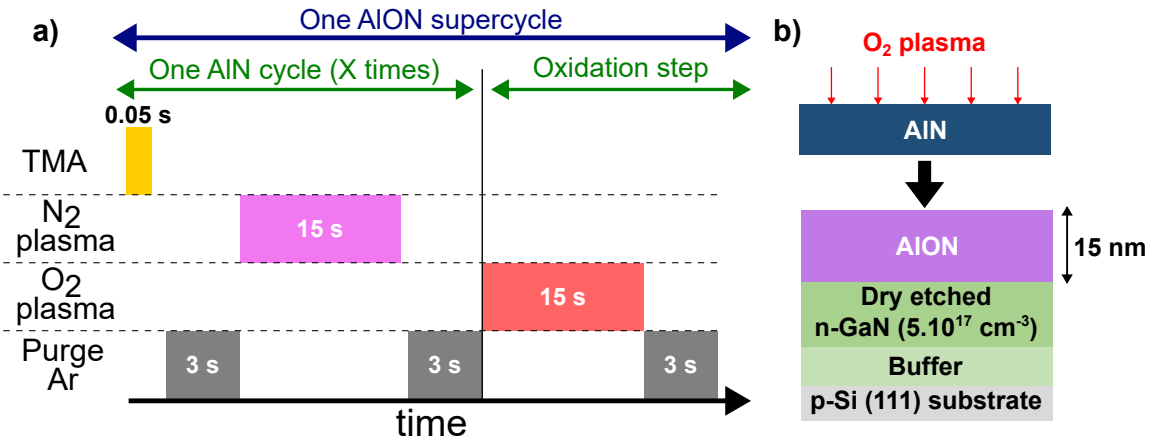


Figure 5.1: Schematic representation of a) the PE-ALD sequence used to deposit AlON and of b) AlON/etched GaN stack

To monitor the film growth, *In-Situ* Spectroscopic Ellipsometry (SE) with four wavelengths (463 nm, 524 nm, 596 nm, and 634 nm) was used. The thickness was measured by fitting a nonlinear regression algorithm (Marquardt-Levenberg) with Film Sense Software. More information on the fitting parameters is presented in reference [264]. The structural properties of AlON films were analyzed using TEM, after Focused Ion-Beam (FIB) with a Helios Nanolab 450S from FEI. The chemical composition was analyzed by Parallel Angle-Resolved X-ray Photoelectron Spectroscopy (pAR-XPS) on the Theta 300 tool from Thermo Scientific, with the incident angle varying from 23.75° to 76.25°. The X-ray energy source was a monochromatic Al Kα (hν = 1486.7 eV), the pass energy was fixed at 100 eV and the energy resolution was fixed at 0.1 eV. Finally, the chemical composition and the in-depth composition profiles were analyzed by Auger Electron Spectroscopy (AES) and ToF-SIMS analyses. The AES analyses were performed with a PHI 700Xi Auger nanoprobe using a 20 keV incident electron beam energy. The atomic concentration profiles were obtained by sputtering the deposited layer with a 500 eV Ar^+ ion beam. The AES spectra were collected after each 30 s sputtering step. For the ToF-SIMS analyses, negative ions were collected and analyzed.

5.1.2 Results and discussion: towards an uniformed and controlled layer

The thicknesses of AlN layers deposited within X AlN cycles and of the final AlON layers, measured with in-situ Spectroscopic Ellipsometry, are summarized in **Table 5.1**. The maximum and the minimum AlN thicknesses before an oxidation step are respectively 3.8 and 0.25 nm. The AlN's Growth Per Cycle (GPC) for each supercycle is around 0.63 Å/cycle, close to our AlN reference [264]. The final thickness is 15 $\pm$ 1 nm for all supercycles, meaning that the oxidation step doesn't influence the growth rate.

To understand the chemical environment of the different AlON supercycles, the N1s spectra (cf. **Figure 5.3**) were analyzed and the nitrogen atomic concentration was calculated (cf. **Figure 5.2**). From the N1s spectra, four different chemical bonds are identified and resumed here: N-Al at 397 eV [163], [164], [265], N-Al-O at 398.3eV [265], [266], O-N-Al at 399.7 eV [163], [164], [266] and N-O at 403 eV [133], [163], [164], [265]. However, the strongly oxidized N-O bond is noted only for supercycles with a number of AlN cycles per oxidation lower than 15 ($t_{AlN}^{oxid.} \leq 0.96$ nm). The other three chemical bonds are observed for all the others supercycles.

Supercycles	60x4	30x8	15x16	12x20	8x30	4x60
AlN cycles per oxidization step	60	30	15	12	8	4
Average thickness or $t_{AlN}^{oxid.}$ (nm)	3.8	1.92	0.96	0.76	0.51	0.25
Growth Per Cycle (GPC) (Å/cycle)	0.63	0.64	0.64	0.63	0.64	0.63
Final sample thickness (nm)			$\backsim$ **15** $\pm$ **1**			

Table 5.1: Summary of AlON supercycles and their respective AlN thickness per oxidation step

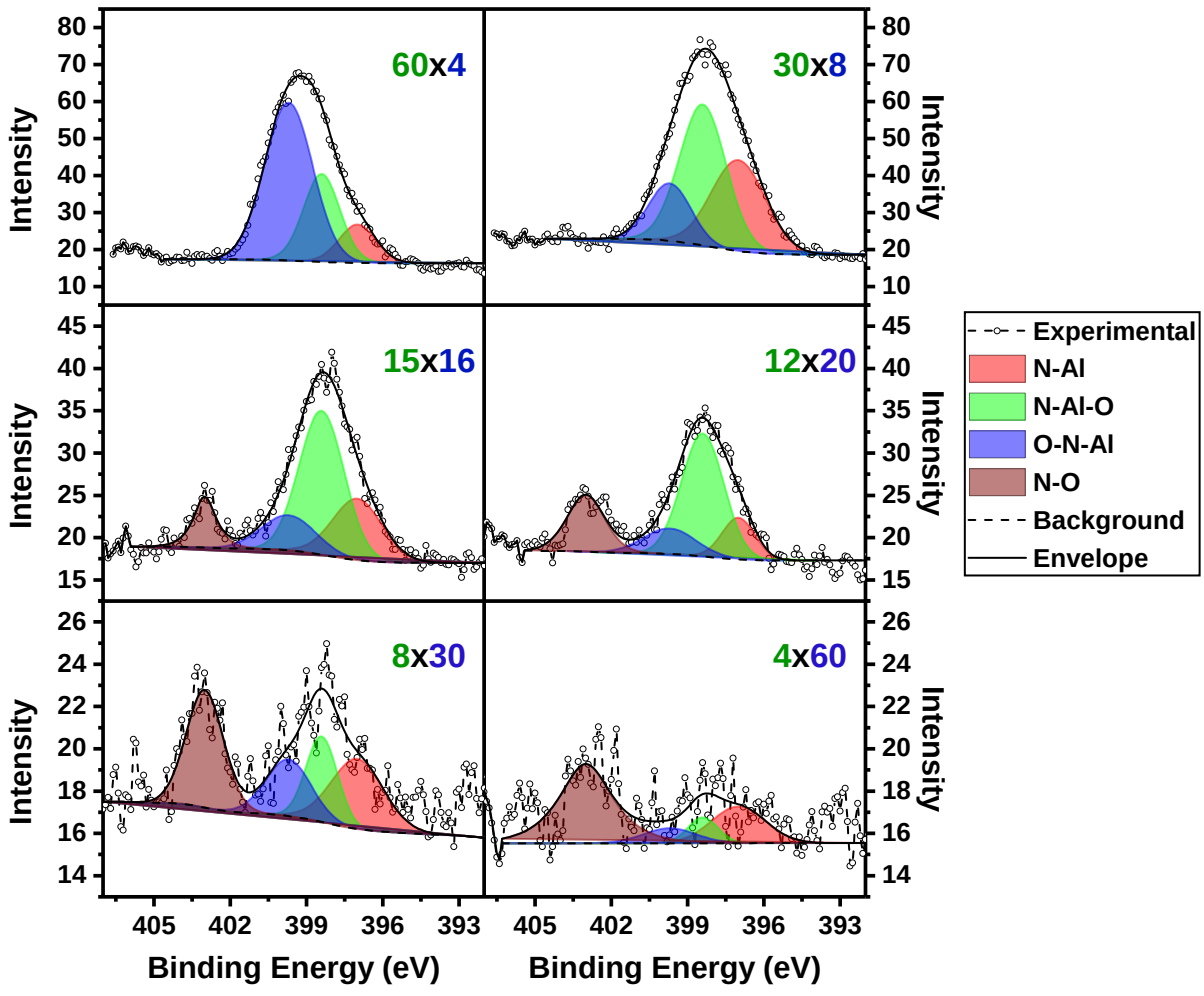


Figure 5.2: N1s spectra obtained by pAR-XPS for different AlON supercycles.

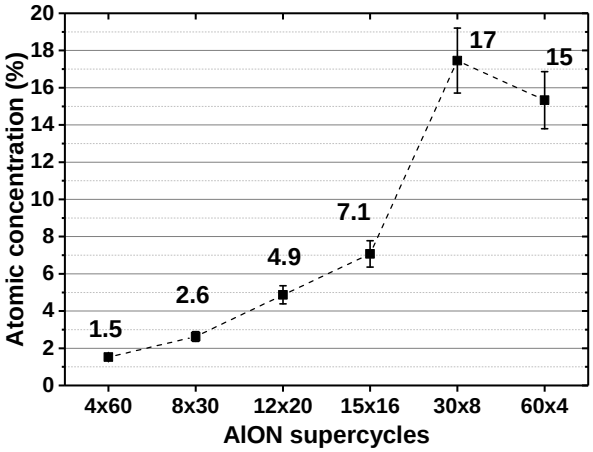


Figure 5.3: Nitrogen atomic concentration in percentage for different AlON supercycles obtained from pAR-XPS quantification.

From XPS quantification, a higher nitrogen content is related to a thicker AlN being oxidized (or thicker $t_{AlN}^{oxid.}$), with the lowest and the highest nitrogen concentration being respectively 1.5 and 17 %. Hence, by adjusting $t_{AlN}^{oxid.}$ with the number of AlN cycles, it is possible to control the nitrogen content. These observations are in agreement with results reported by Nozaki et al. [133] for AlON deposition by oxidation with ozone (O_3).

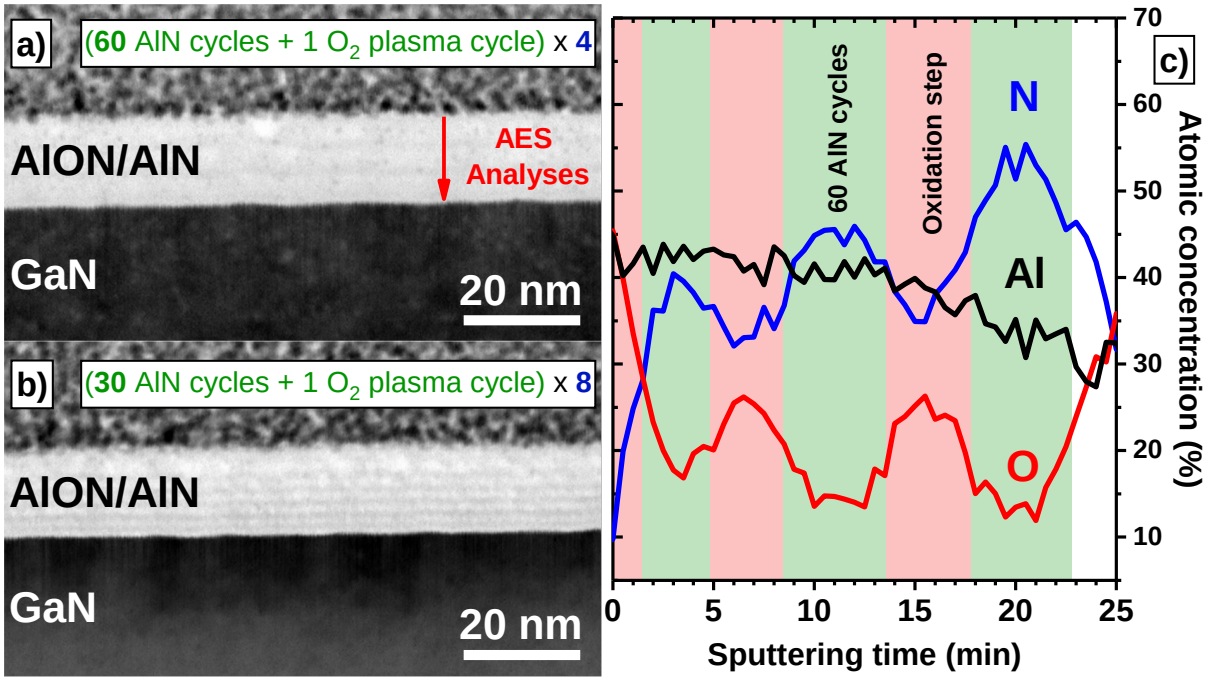


Figure 5.4: On the left, TEM images for a) 60x4 and b) 30x8 AlON supercycles. On the right, c) AES atomic concentration profile of N, Al, O for 60x4 AlON supercycle.

When analyzing the TEM images of 60x4 and 30x8 supercycles in **Figure 5.4.a) and b)**, a non-uniform dielectric layer is noticed for both layers. More specifically, dark regions in the number of supercycles (or oxidation step) can be observed for both AlON supercycles, meaning that the whole layer is partially oxidized and that both AlON and AlN are present. To confirm this observation, AES atomic concentration profiles for the 60x4 sample were measured and are represented in **Figure 5.4.c)**. Cyclical peaks of nitro-

gen and oxygen appear alternatively, while the aluminium profile remains constant throughout the layer. It can be noted that the nitrogen contents found by AES are probably less accurate than those obtained by XPS, due to the use of tabulated Relative Sensitivity Factors (RSFs) that do not take into account matrix effects. Moreover, when comparing the TEM image and the AES profiles for 60x4 supercycles, the dark regions correspond to AlON thin layers whereas the bright regions can be associated with AlN layers. Therefore, the limiting factor for the full AlN layer oxidation is the diffusion of oxidizing species through a $t_{AlN}^{oxid.}$ thicker than 1.92 nm. Increasing the plasma step time and/or the plasma power could oxidize the AlN layer, but it might require specific parameters for each supercycle having a $t_{AlN}^{oxid.}$ higher than 1.92 nm. Other than film uniformity, a quick survey of C-V measurements on these supercycles (not shown here) revealed large leakage current, further demonstrating that these films cannot be used for a MOS gate.

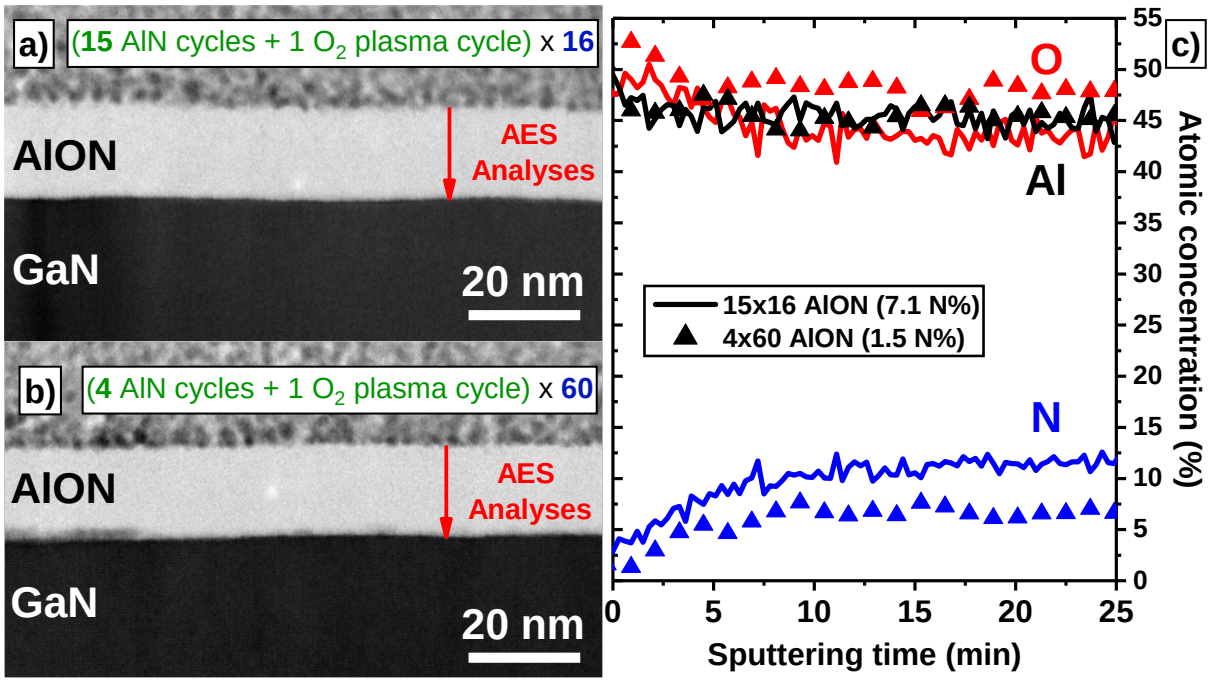


Figure 5.5: On the left, TEM images for a) 15x16 and b) 4x60 AlON supercycles. On the right, c) AES atomic concentration profile of N, Al, O for 15x16 and 4x60 AlON supercycle.

On the other hand, for the 15x16 and 4x60 supercycles ($t_{AlN}^{oxid.}$ = 0.96 and 0.25 nm respectively), their respective TEM images in **Figure 5.5.a) and b)** reveal a uniform amorphous layer. The latter implies that their corresponding AlN's $t_{AlN}^{oxid.}$ were thin enough for the oxidizing species to diffuse and oxidize the AlN layer at each oxidation step. AES atomic concentration profiles in **Figure 5.5.c**)) confirms this observation, in which both oxygen and nitrogen are uniformly distributed in the layer. Furthermore, since N-O bonds are also notified only for supercycles with a number of AlN cycles lower than 15 (**Figure 5.2**), it seems that the presence of these bonds is an indicator of a uniformly oxidized layer. The AES depth profiles also confirm the lower nitrogen content expected for the 4x60 AlON supercycle. Consequently, with our O_2 plasma setting, the supercycles with AlN $t_{AlN}^{oxid.}$ lower than 1 nm lead to a uniform AlON layer. For the rest of the study, 15x16, 12x20, 8x30 and 4x60 supercycles will be considered since only these supercycles form uniform AlON and can be electrically viable.

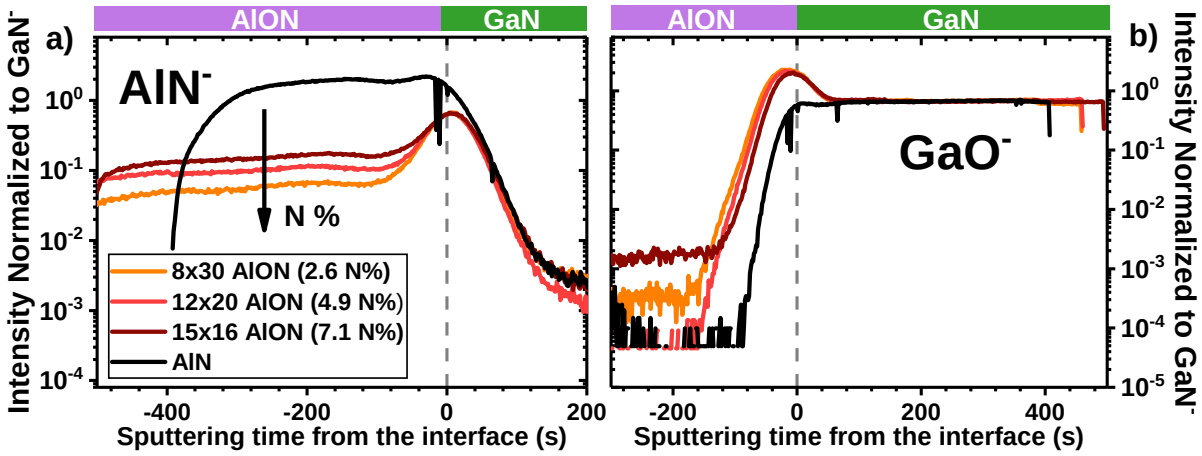


Figure 5.6: ToF-SIMS analyses of a) AlN^- and b) GaO^- depth profiles for reference AlN sample, 8x30 (2.6 N%), 12x20 (4.9 N%) and 15x16 (7.1 N%) AlON samples.

To confirm the overall uniform distribution of nitrogen and study the presence of gallium oxide at the interface, ToF-SIMS depth profiles of AlN^- and GaO^- were analyzed and are represented in **Figure 5.6.a) and b)**. The AlN^- profiles confirm the uniform AlON distribution throughout the different AlON samples, and their reduction is in agreement with their respective nitrogen content. Once more, the profiles demonstrate full nitrogen incorporation in the AlON layer without regions with depleted nitrogen content as in the AES depth profiles for 60x4 AlON supercycle (cf. **Figure 5.4.c**)). By analyzing the GaO^- depth profiles (cf. **Figure 5.6.b**)), a slight increase of GaN oxidation can be noticed at the AlON/etched GaN interface with a lower number of AlN cycles (thinner $t_{AlN}^{oxid.}$) being oxidized, probably because the O_2 plasma can more easily oxidize the GaN surface with a thinner deposited AlN layer. Nonetheless, the increase in GaO^- is small when the number of AlN cycles is reduced, meaning that our deposition process has a small impact on interface oxidation. Regarding the 4x60 AlON supercycle, the TEM image in (cf. **Figure 5.5.b**)) seems to indicate GaN oxidation and it will be investigated in the next section.

5.1.3 Conclusions

AlON layers with a 15 nm thickness were deposited by PE-ALD with different nitrogen concentrations by combining a thin PE-ALD AlN and an oxidation step with an O_2 plasma. The nitrogen content is controlled by the AlN thickness per oxidation step. For an AlN thickness per oxidation ($t_{AlN}^{oxid.}$) step higher than $\backsim$1 nm, an AlON/AlN multilayer is deposited and observed by TEM and AES. On the other hand, a uniform AlON film is obtained for an AlN thickness per oxidation step lower than $\backsim$1 nm, with characteristic N-O bonds observed in pAR-XPS. Moreover, the GaN substrate is slightly oxidized by the O_2 plasma step, even for a low $t_{AlN}^{oxid.}$ equal to 0.51 nm. Hence, the deposition step has only a slight impact on interface oxidation.

5.2 PDA with different Nitrogen concentrations

In this section, electrical properties the uniform deposited AlON (15x16, 12x20, 8x30 and 4x60 supercycles) will be investigated as a function of the nitrogen content. Then the impact of different PDA temperatures on the AlON material and electrical properties will be discussed. A nitrogen concentra-

tion from 1.5 to 2.6% with an annealing at 800°C is found to be optimal in terms of MOS capacitances electrical parameters.

5.2.1 Experimental details

15 nm of AlON with different nitrogen concentrations were deposited on the same substrates from the previous section. The GaN etching, cleaning, and AlON deposition were the same as described in **Section 5.1.2**. The nitrogen concentrations were 1.5%, 2.6%, 4.9%, and 7.1% in atomic concentration. Similarly, 15 nm of Al_2O_3 was deposited by ALD for reference, with TMA and H_2O as precursors. After deposition, PDA was performed under N_2 for 5 min at 400, 600, or 800°C for both AlON and Al_2O_3 samples in an RTP furnace. These 3 temperatures were selected to probe a large temperature range for the 4 different nitrogen concentrations. Circular MOSCAP structures were then fabricated (cf. **Figure 5.7**) and *C-V* measurements were carried out at 1 kHz with a forward voltage sweep between -4 V and 4 V, and a backward voltage sweep between 4 V and -4 V. Two measuring temperatures were selected, 25°C and 150°C, to analyze the electron trapping in the dielectric at elevated temperature but also to analyze deeper interface states. Measure-Stress-Measure (MSM) measurements were performed by stressing the gate at 4 V until 1000 s as described in **Section 2.2.4.3**, in order to have a view on the Positive Bias Temperature Instability (PBTI). The instability was monitored by calculating the V_T shift with respect to the measurement before stress, V_T being defined as $(C_{OX}\text{-}C_{min})/2+C_{min}$. The interface states density was extracted using the abacus used for the conductance method presented in **Section 2.2.3.2**.

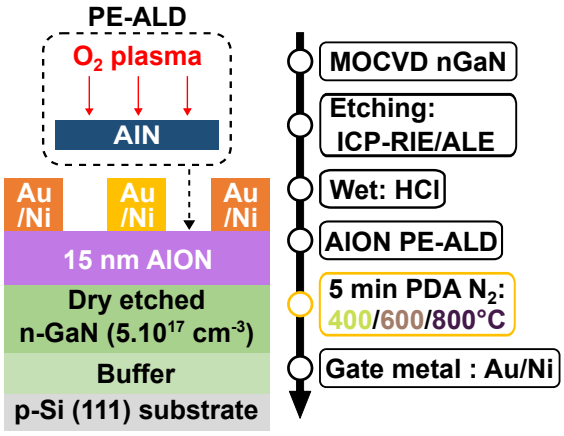


Figure 5.7: AlON MOSCAPs process flow with different PDA temperatures

The nitrogen atomic concentration and the interfacial gallium oxide thickness at different PDA temperatures were analyzed by HAXPES and Angle-Resolved Hard X-ray Photoelectron Spectroscopy (AR-HAXPES) respectively. These analyses were performed on the PHI Quantes. Interface oxidation was also analyzed by XPS with the PHI Quantes equally equipped with a monochromatic Al Kα (hν = 1486.7 eV), together with AlON's energy band gap, band offset and band bending. The band gap was extracted using the O1s energy loss spectrum whereas the band bending and the band offset were calculated as explained in **Section 2.3.1.8**. Specifically for band bending and band offset measurements, 3 nm AlON deposited on etched GaN were analyzed. For the latter, the analyzed spectra were O1s, and Ga3d. The nitrogen distribution and impurities were analyzed by ToF-SIMS analyses by detecting negative ions. Similarly to the previous section, the same AlN reference was analyzed by ToF-SIMS.

GIXRD was equally performed on 2.6 N%, 4.9 N%, and 7.1 N% AlON samples without metallization and after a PDA at 900°C.

5.2.2 Results and discussion

5.2.2.1 Impact of Nitrogen incorporation without annealing

The impact of the different nitrogen concentrations on the AlON/etched GaN electrical performances was investigated without PDA. **Figure 5.8** shows the *C-V* and G_m/ω characteristics measured at 25°C and 150°C for the reference Al_2O_3 and the AlON samples. For AlON, *C-V* characteristics are shifted positively with higher nitrogen concentration as previously reported [163], [166], but the shift does not go beyond Al_2O_3 for both measuring temperatures. A double slope at AlON's *C-V* characteristics is also observed at 25°C, but it disappears at 150°C. This slope can be related to interface states since conductance peaks are observed close to the slope. Increasing the temperature allows deeper interface states to respond to the *C-V* measurement while their emission time is reduced according to the Shockley–Read–Hall (SRH) model. This could lead to the disappearance of the slope at 150°C. All studied samples present clockwise hysteresis, with the latter increasing at 150°C compared to 25°C due to electron trapping in the oxide and at the interface being enhanced by the elevated temperature. Interestingly, Al_2O_3 has the highest hysteresis at 150°C.

The V_{FB} and ΔV_{FB} are extracted from the *C-V* characteristics as shown in **Figure 5.9**. As mentioned before for AlON, the increased V_{FB} with higher nitrogen concentration is noticed for both measuring temperatures. Hysteresis seems to be slightly impacted by nitrogen concentration as ΔV_{FB} increases for nitrogen concentration above 1.5%. However, no clear trend with nitrogen concentration can be observed at both measuring temperatures. Nonetheless, at both measuring temperatures and for the different nitrogen contents, the lower hysteresis of AlON compared to Al_2O_3 indicate that nitrogen incorporation in AlON reduces electron trapping, especially for higher measuring temperatures as 150°C. The lower electron trapping for AlON could be explained by the reduction of traps such as Oxygen Vacancies (V_O) [170] and/or the increase of conduction band offset between AlON and GaN [164], although AlON's slightly lower band gap than Al_2O_3's one [133], [162].

By using the interface states density abacus, D_{it} values were extracted and summarized in **Table 5.2**. The associated energy levels are calculated with the measuring temperature and frequency using the equation in **Section 2.2.3.2**. It reveals an overall better interface for the AlON/GaN interface with lower D_{it} when nitrogen concentration is reduced. Interestingly, D_{it} for 7.1 N% AlON is close to Al_2O_3. As such, it seems that the increase in nitrogen concentration induces a small degradation of the AlON/GaN interface.

The insertion of nitrogen at low concentration (<5%) seems to improve the quality of both the dielectric (less electron trapping) and the interface (less hysteresis and interfacial states), when compared to Al_2O_3. This is contrary to the reported literature, where an increase in nitrogen incorporation leads to lower electron trapping [133].

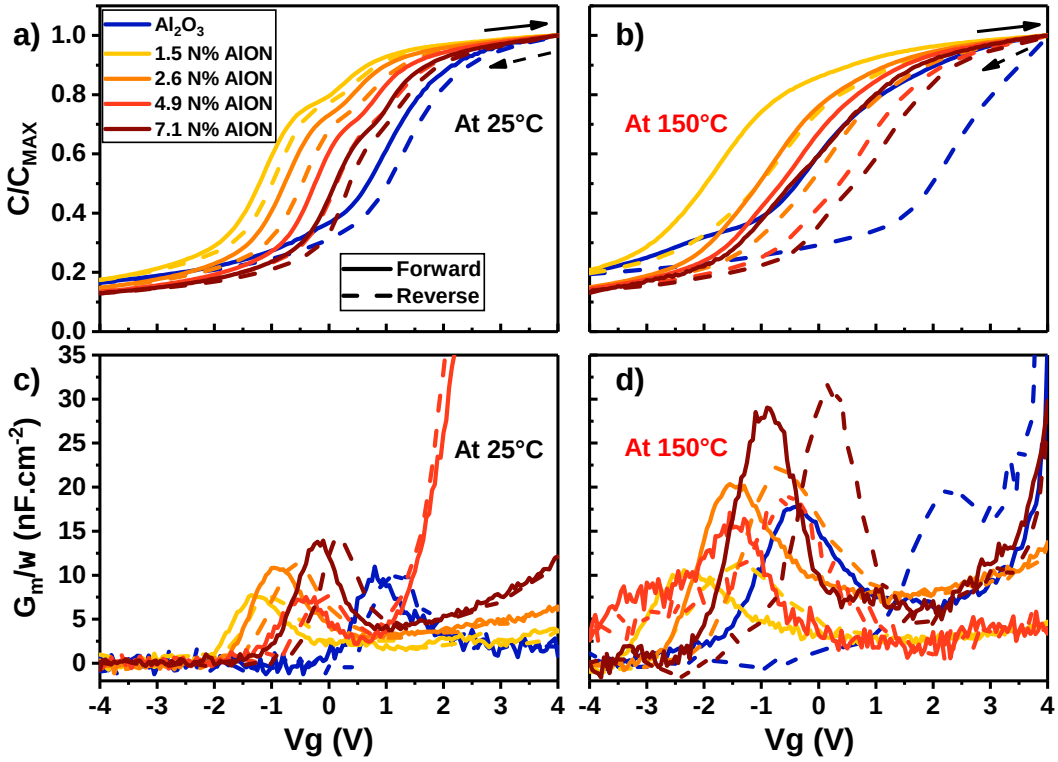


Figure 5.8: Normalized C-V characteristics for Al_2O_3 and AlON samples without annealing at the measuring temperatures of a) 25°C and b) 150°C (median of three measurements); G_m/ω characteristics at c) 25°C and d) 150°C (single measurement).

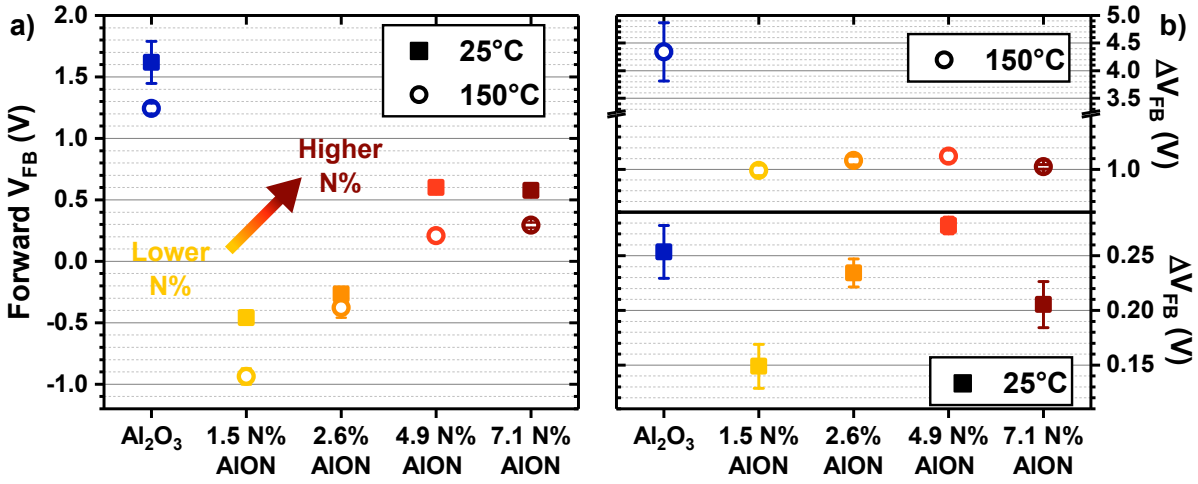


Figure 5.9: a) Extracted forward V_{FB} (median of three measurements) at the measuring temperatures of 25°C and 150°C; b) extracted V_{FB} hysteresis (median of three measurements) at 25°C and 150°C.

$E_C - E_T$ (eV)	D_{it} $(10^{11} eV^{-1}.cm^{-2})$				
	Al_2O_3	$1.5N\%$	$2.6N\%$	$4.9N\%$	$7.1N\%$
$0.49(25°C)$	2.50 ± 0.35	0.95 ± 0.08	1.82 ± 0.11	1.33 ± 0.01	2.25 ± 0.11
$0.72(150°C)$	4.98 ± 0.74	1.86 ± 0.05	2.82 ± 0.16	2.73 ± 0.07	5.72 ± 0.54

Table 5.2: Interface states density (median of three measurements) extracted from normalized G_m/ω peaks at 1 kHz for both 25°C and 150°C.

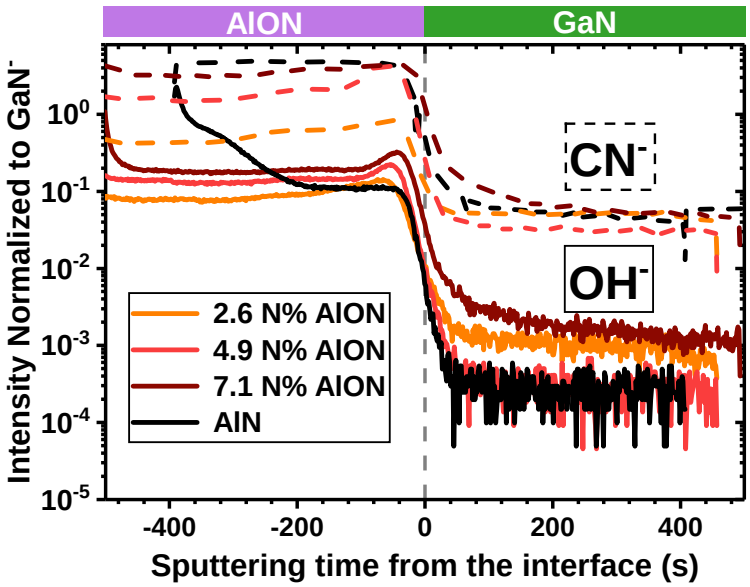


Figure 5.10: Normalized ToF-SIMS depth profiles of CN^- and OH^- profiles for a reference AlN sample, 2.6 N%, 4.9 N%, and 7.1 N% AlON samples.

To further understand the impact of nitrogen on the V_{FB} hysteresis and D_{it}, ToF-SIMS analyses were carried out on the 2.6 N%, 4.9 N%, and 7.1 N% AlON samples. As shown in **Figure 5.10**, ToF-SIMS analyses reveal an increase in hydroxyl groups and carbon impurities with higher nitrogen content. The deteriorated hysteresis and D_{it} with increasing nitrogen concentration could be then related to the increase of hydroxyl groups and carbon impurities, as previously reported [75], [267] and observed **Section 3.2.2.1**. The increase of these impurities seems not to be directly related to the nitrogen concentration but mostly to the deposition technique, especially for carbon impurities found in the AlN reference sample. Since to obtain lower nitrogen concentration, thinner AlN layers have to be oxidized, it means that fewer carbon impurities from AlN deposition remain in the AlON layer. Regarding hydroxyl groups, no particular explanation was found for their increase with respect to nitrogen concentration, since the reference AlN sample has the lowest amount of hydroxyl groups close to the GaN interface. Thus, in comparison with Al_2O_3, the introduction of nitrogen for all concentrations is more advantageous specifically for higher operating temperatures, but within AlON samples, lower nitrogen concentrations have lower electron trapping due to the lower presence of impurities.

5.2.2.2 Impact of annealing

After Post-deposition Annealing, the nitrogen content and distribution in the AlON were analyzed by HAXPES and ToF-SIMS using the 4.9 N% AlON sample for its intermediary nitrogen content. As shown in **Table 5.3**, a stable nitrogen concentration is found for the different PDA temperatures, highlighting stable nitrogen incorporation within AlON even after 800°C PDA, similar to AlON deposited by Nozaki et al. after 800°C PDA [133]. The difference in nitrogen content from the expected value of 4.9 N% can be associated with the uncertainty of the fitting process used to take away the N-Ga contribution from the GaN substrate (cf. in **Annex D**, **Figure A.4**).

In **Figure 5.11**, the ToF-SIMS analyses of AlN^- profiles reveal the absence of a degraded layer or inhomogeneous nitrogen distribution with increasing PDA temperatures. GIXRD analyses of annealed

PDA temperature	N (at%)	Al (at%)	O (at%)
w/o PDA	4.1	33.7	62.2
400°C	4.8	32.8	62.4
600°C	4.4	33.5	62.2
800°C	4.2	33.3	62.5

Table 5.3: Atomic percentage for N, Al and O in 4.9 N% AlON by using quantification with HAXPES. Results are given with an uncertainty of ±10%

AlON samples at 900°C (cf. **Figure 5.12**) shows no sign of crystallization for a PDA at 900°C but TEM images are necessary to confirm the absence of crystallized regions. For a PDA at 800°C, the TEM images in **Figure 5.12** show no crystallization, confirming the high thermal stability of AlON compared to Al_2O_3 [42].

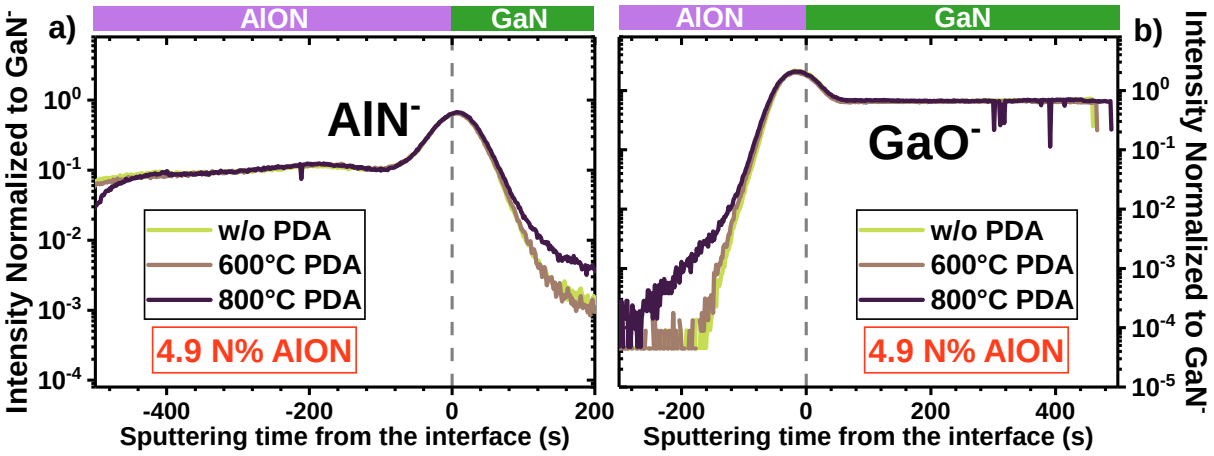


Figure 5.11: Normalized ToF-SIMS depth profile of a) AlN^- and b) GaO^- profiles for 4.9 N% AlON samples without PDA and with respectively 600°C and 800°C PDA.

The higher crystallization temperature is explained by the incorporation of nitrogen. The oxidant precursors is also different between AlON and Al_2O_3 (O_2 and H_2O respectively), but in the literature peaks related to crystallization in GIXRD analyses where observed for Al_2O_3 deposited with O_2 plasma after a 800°C PDA [42], whereas in **Figure 5.12** no peaks are observed after a 900°C PDA and no crystallized regions appear in the TEM images after a 800°C PDA. Concerning the interface stability, ToF-SIMS analyses of GaO^- profiles show no specific growth of GaO_x or Gallium diffusion with increasing PDA temperature, thus revealing a stable interface under high PDA temperature.

Low GaO_x growth was also observed with AR-HAXPES for the 1.5 N% AlON sample, shown in **Figure 5.13**, with GaO_x thickness remaining below 1 nm ($Ga2p_{3/2}$ fitted spectra in **Annex D**, **Figure A.5**). However, for this 1.5 N% sample, a trend of increasing GaO_x thickness with increasing PDA T°C is observed, as expected from the results in **Section 5.1.2**, where a slight increase of GaN oxidation was noticed at the AlON/GaN interface with a lower number of AlN cycles. The results in **Figure 5.13** seem to show that 1.5 N% AlON has a thicker interfacial GaO_x than Al_2O_3 sample, but the uncertainty is rather high. Still, compared to the thickness extracted for the AlSiO study, AlON seems to prevent further oxidation, probably due to its affinity for oxygen and therefore acting as a sponge for oxygen.

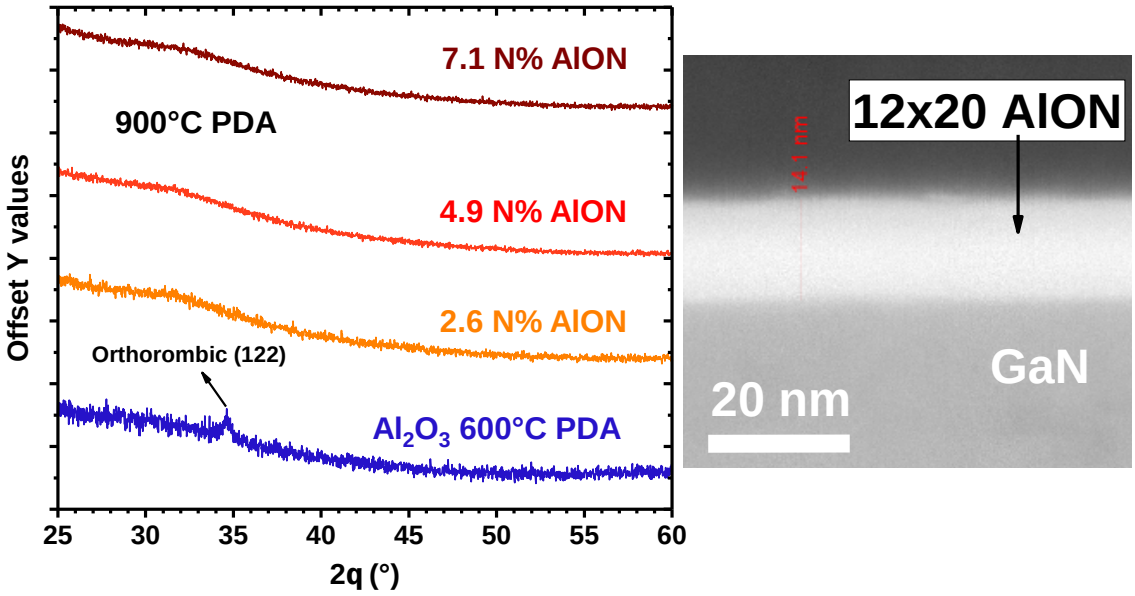


Figure 5.12: On the left, GIXRD analyses of 2.6 N%, 4.9 N% and 7.1 N% AlON annealed at 900°C under N_2 for 5 min. Incident angle was 2°. On the right, TEM image for 12x20 AlON after a 800°C PDA

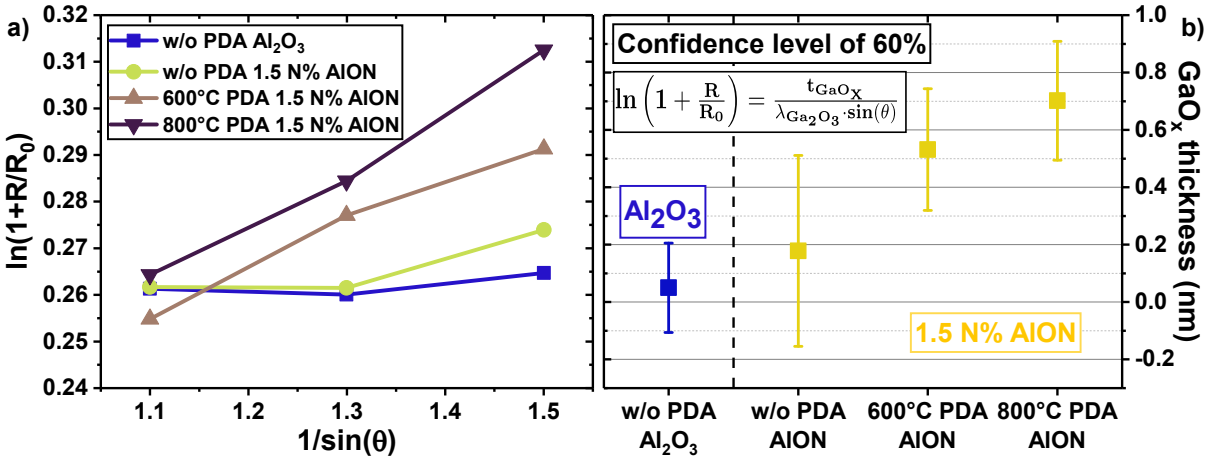


Figure 5.13: a) ln(1+R/R_0) as a function of 1/sin(θ) and b) extracted interfacial GaO_x thickness obtained by AR-HAXPES using 3 take-off angles (42/50/65°) for Al_2O_3 and with 1.5 N% AlON without PDA, with 600°C and 800°C PDA.

Figure 5.14 shows the *C-V* and G_m/ω characteristics for different AlON after PDA at 800°C. The Al_2O_3 characteristics were not measured due to the large leakage current from crystallization after 800°C PDA. The presence of *C-V* characteristics for AlON reassures the higher thermal stability of AlON over Al_2O_3 thanks to the introduction of nitrogen. Moreover, the positive shift of *C-V* curves with higher nitrogen concentration (cf. **Section 5.2.2.1**) is also noticed after PDA, and at both measuring temperatures. Hysteresis reduces with a 800°C PDA in comparison with no PDA (cf. **Figure 5.8**), as previously reported for a PDA under forming gas (N_2/H_2) or O_2 [163], [169]. Concerning the interface, conductance peaks are also reduced for all nitrogen concentrations and at both measuring temperatures in comparison with no PDA (cf. **Figure 5.8**), leading to the disappearance of the second slope observed for the AlON samples without PDA. In terms of permittivity at 800°C, it varies with N% as follow: 8.7, 9.2, 10.5, 9.3 for 1.5, 2.6, 4.9, 7.1 N% respectively. The high permittivity is in the range of reported permittivity for Al_2O_3 [124], [125].

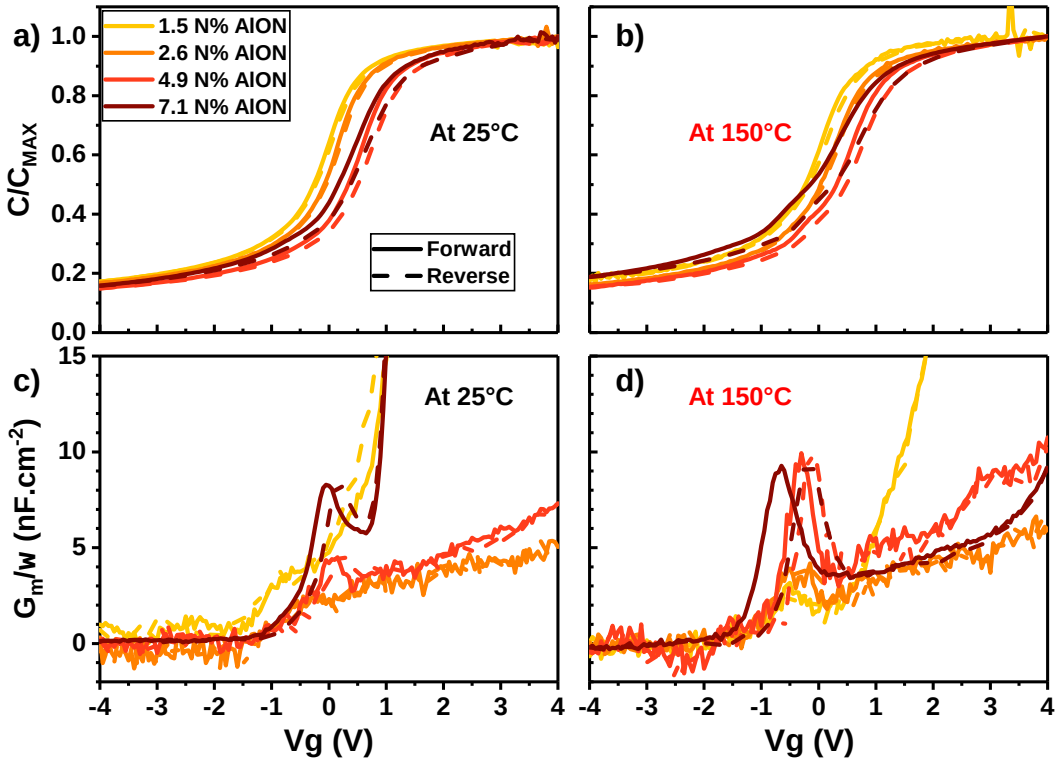


Figure 5.14: Normalized C-V characteristics for AlON samples with 800°C PDA at the measuring temperatures of a) 25°C and b) 150°C (median of three measurements); G_m/ω characteristics at c) 25°C and d) 150°C (single measurement).

The extracted V_{FB} and hysteresis at both measuring temperatures and for different PDA temperatures are shown in **Figure 5.15**. While the nitrogen incorporation increases the V_{FB}, PDA also increases V_{FB} as previously reported for PDA under O_2 on AlON [169]. In our case, PDA increases and stabilizes V_{FB} throughout the different PDA temperatures, especially for nitrogen concentrations under 4.9%. On the other side, V_{FB} for Al_2O_3 is strongly reduced with increasing PDA temperature, with a V_{FB} being lower than AlON for a 600°C PDA. This trend is similar to one observed in **Section 3.2.2.1** but with different wet treatments (here HCl, there ending with HF). As mentioned, hysteresis for all samples reduces for both measuring temperatures. At 25°C, ΔV_{FB} reduction follows a similar trend for Al_2O_3, 1.5 N%, and

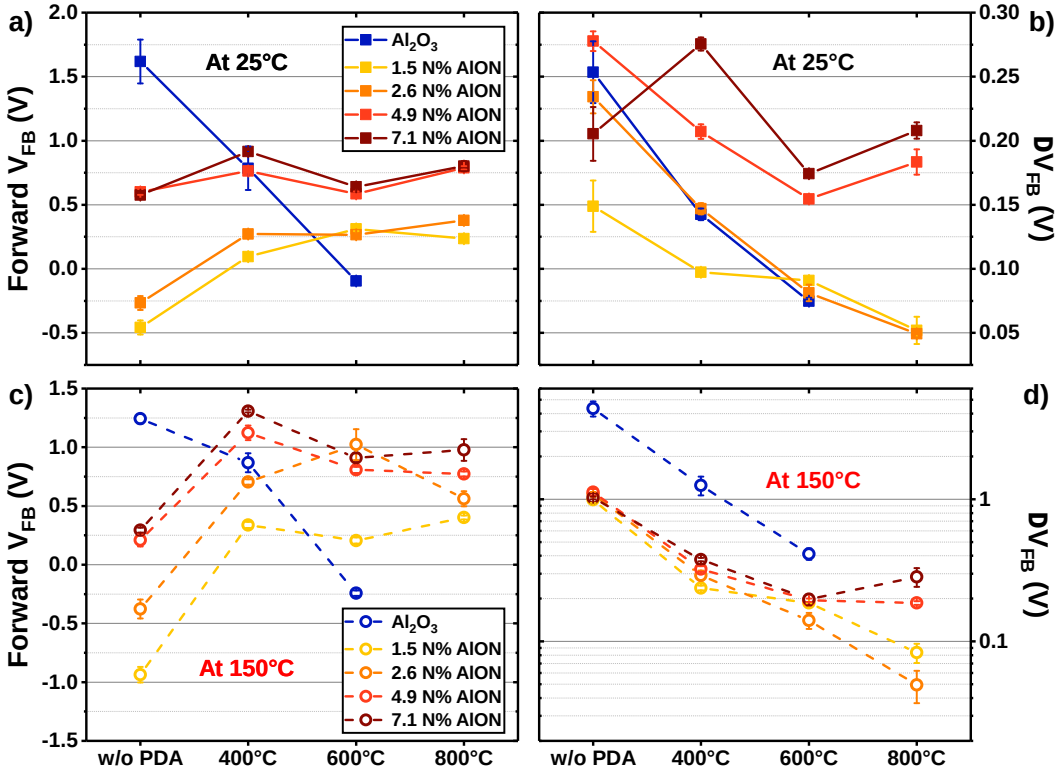


Figure 5.15: For the different PDA temperatures: a,b) Extracted forward V_{FB} and ΔV_{FB} (median of three measurements) at 25°C; c,d) Extracted forward V_{FB} and ΔV_{FB} (median of three measurements) at 150 °C

2.6 N% AlON samples, reaching values below 4.9 N% and 7.1 N% AlON samples. However, at 150°C, a more pronounced hysteresis is observed for Al_2O_3, while all AlON samples have a lower hysteresis. This observation further confirms the reduction of electron trapping by nitrogen incorporation. Interestingly, hysteresis for 1.5 N% and 2.6 N% are strongly reduced even at 150°C, with a low hysteresis for both measuring temperatures. With respect to nitrogen content, a higher hysteresis for a concentration higher than 2.6 % is relatively maintained for each PDA temperature.

The observed trend for hysteresis at both 25 and 150°C is confirmed by MSM measurements at 4 V for AlON samples annealed at 800°C and Al_2O_3 annealed at 600°C represented in **Figure 5.16**. For 4.9 and 7.1 N% AlON, stressing at both 25 and 150°C reveals a large trapping, the 7.1 N% sample presenting the highest shift. The trapping starts to stabilize after around 100 s. For 1.5 and 2.8 N% AlON at room temperature, the V_T shift is higher than for Al_2O_3, similarly to the hysteresis extracted in **Figure 5.15.d)**. Nonetheless at 150°C, the V_T shift for 1.5 and 2.6 %N increases but stays lower than Al_2O_3 for which ΔV_T increases rapidly to the point of being higher than the 7.1 N% AlON sample after 1000 s. Therefore, this highlights the better reliability of AlON with 1.5∼2.6 N% annealed at 800°C compared to the other nitrogen concentrations and more importantly to Al_2O_3.

The reduction of hysteresis or electron trapping with PDA temperature could be explained partly by the reduction of hydroxyl groups [75]. This is confirmed by ToF-SIMS analyses (cf. **Figure 5.17**) showing reduced hydroxyl groups with PDA temperature. Possible other defects such as border traps in the dielectric layer [135], [140] could also be reduced by the PDA process. However, the carbon impurities do not reduce with PDA (cf. **Figure 5.17**). This means that they are well incorporated within the AlON

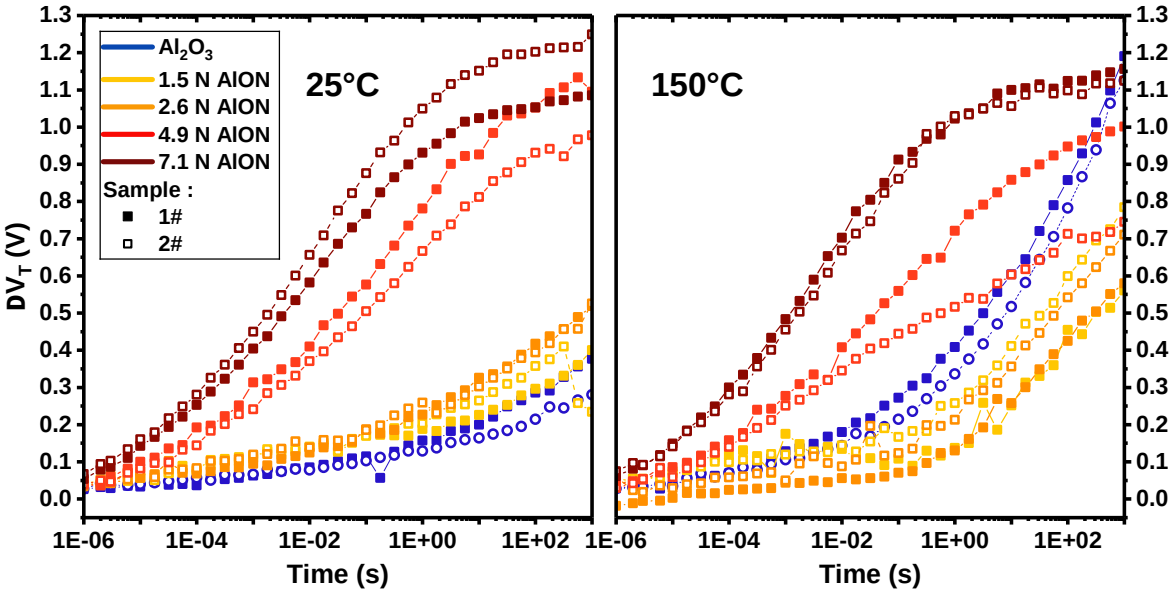


Figure 5.16: ΔV_T after stress at 4 V for the Al_2O_3 sample with a 600°C PDA and for the different AlON samples with a PDA 800°C PDA

layer and cannot explain the ΔV_{FB} reduction with PDA temperature. Assuming that the carbon content for the other nitrogen concentrations has the same behavior, this assumption could explain the difference observed between the different AlON samples even after PDA, since increasing amounts of carbon impurities could lead to increasing hysteresis [267]. Moreover, contrary to what has been observed in **Section 3.2.2.1**, the increase of GaN oxidation with lower nitrogen content does not explain the difference in hysteresis for the different nitrogen concentrations.

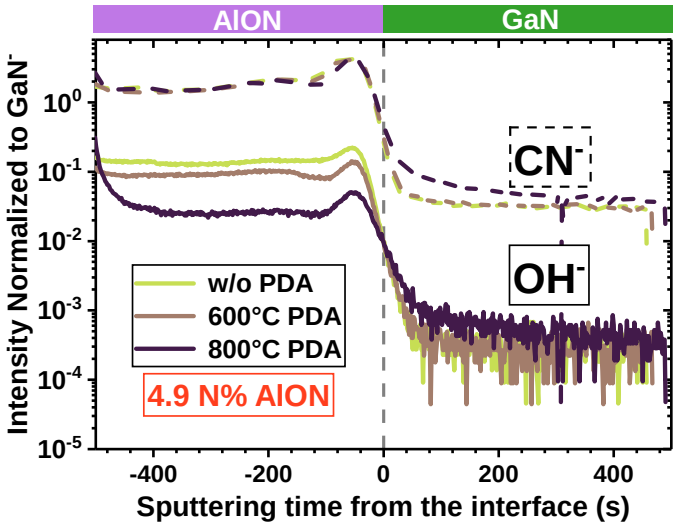


Figure 5.17: Normalized ToF-SIMS depth profiles of CN^- and OH^- profiles for 4.9 N% AlON samples without PDA and with respectively 600°C and 800°C PDA

Finally, concerning the AlON/GaN interface electrical properties, a reduction of D_{it} is observed for AlON samples in comparison with Al_2O_3. D_{it} is only reduced for Al_2O_3 after a 400°C PDA (cf. **Figure 5.18**). At the defect energy level of 0.49 eV (T_{meas}=25°C), little difference is noticed between the AlON samples. But for 800°C PDA, a lower interface states density is found for 1.5 N% AlON. The same observation is made at 0.72 eV (T_{meas}=150°C) where D_{it} is lower for 1.5 N% and 2.6 N% AlON. Hence,

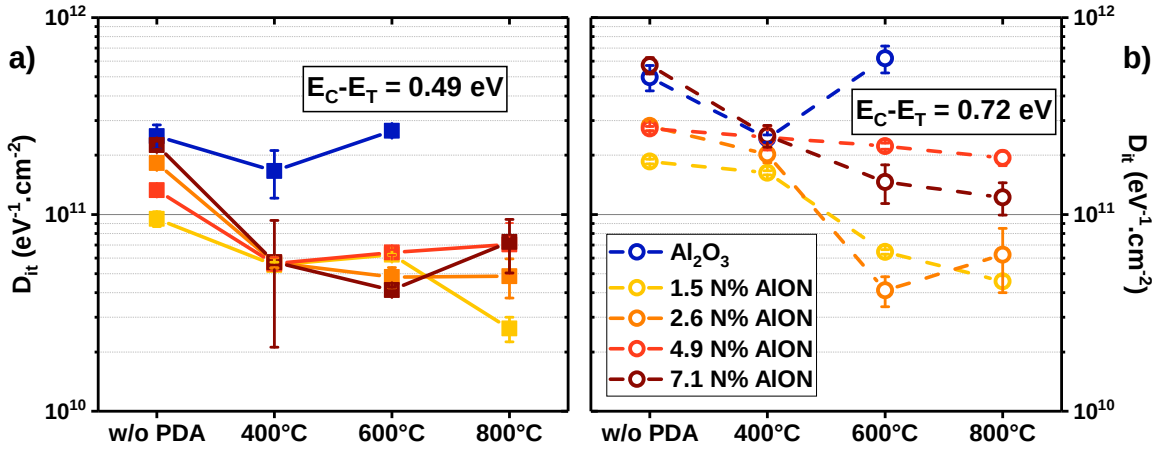


Figure 5.18: Density of interface states extracted from G_m/ω peaks at 1kHz at both measuring temperatures of a) 25°C and b) 150°C for Al_2O_3 and AlON samples with different PDA temperatures.

a better interface is obtained with a lower nitrogen concentration, and a PDA temperature higher than 600°C. This stable and improved interface correlates to the absence of significant growth of interfacial gallium oxide discussed previously.

Considering the hysteresis and the extracted D_{it}, the optimal nitrogen concentration and PDA temperature are 1.5-2.6 N% and a PDA at 600-800°C.

5.2.2.3 Band gap and band-offset for optimal PDA temperature

With the optimal PDA temperature found for 800°C, the band gap and band offset were extracted for different nitrogen concentrations. With the analysis of the O1s electron loss spectrum in **Figure 5.19.a)**, the band gap was extracted and represented in **Figure 5.19.b)**. It shows a parabolic relationship with nitrogen content, with the higher nitrogen content leading to a lower band gap. The extracted AlON band gap is close to the experimental value for ALD Al_2O_3 (6.7 eV [132]), and larger than the theoretical value for AlN (6 eV [124]), which is reasonable since AlON nitrogen content is low, leading to a band gap closer to Al_2O_3. Consequently, the gap is sufficiently large for a dielectric/GaN stack. The extracted band gap is slightly lower than 6.9 7 eV reported by Nozaki et al. [133] for a similar range of nitrogen content after annealing at 800°C and close to 6.8 eV reported by Wang et al. [167] for an AlON annealed at 600°C for 30 s but with an unknown nitrogen content.

With the extracted band gap, the band offsets for both the valence and the conduction band were calculated alongside GaN's band bending **Equation 2.37** and **Equation 2.31** in **Section 2.3.1.8**. **Figure 5.20** represents the band diagram with the extracted values by using the Ga3d spectra at the take-off angle of 45° from the 3 nm AlON/etched GaN samples. As shown in the figure below, the Conduction Band-Offset (CBO) is relatively high for all AlON samples, with little variation with the nitrogen content, and close to the value extracted by Kang et al. with a Fowler-Nordheim plot (2.64 eV) [164]. Hence, AlON has a high barrier for electrons. Inversely, the Valence Band-Offset (VBO) is low for 1.5 N% and can present a problem in hole injection for that sample. These observations are in relative accordance with the band alignment extracted by Wang et al. [167] on AlON/AlGaN stack, with the reported alignment having simultaneously a CBO and a VBO higher than 1 eV. The different values however could be explained by the different substrate (AlGaN has a gap of 4 eV). Compared to the optimal Al_2O_3/etched GaN gate

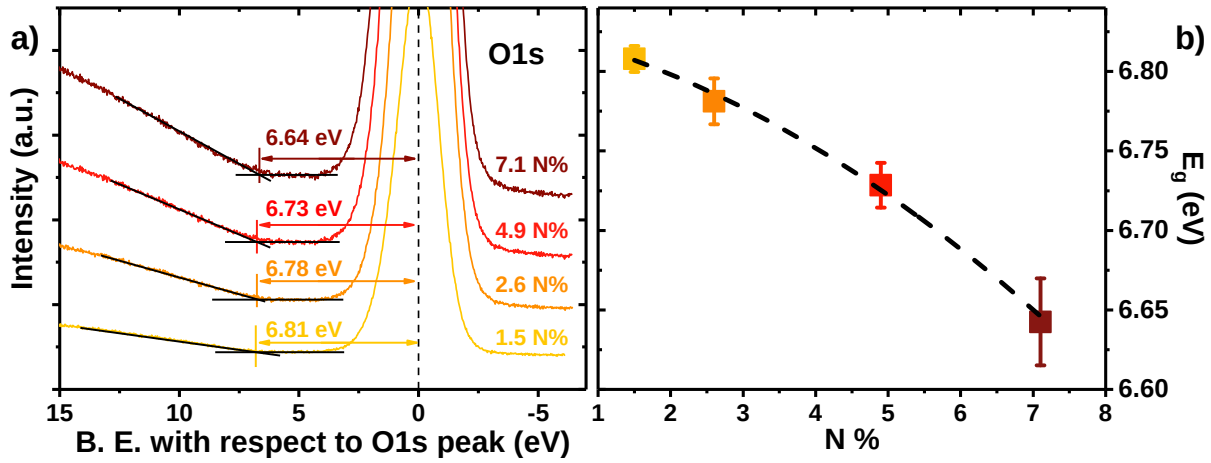


Figure 5.19: a) O1s electron loss spectra and b) corresponding extracted band gap for different nitrogen concentration annealed at 800°C

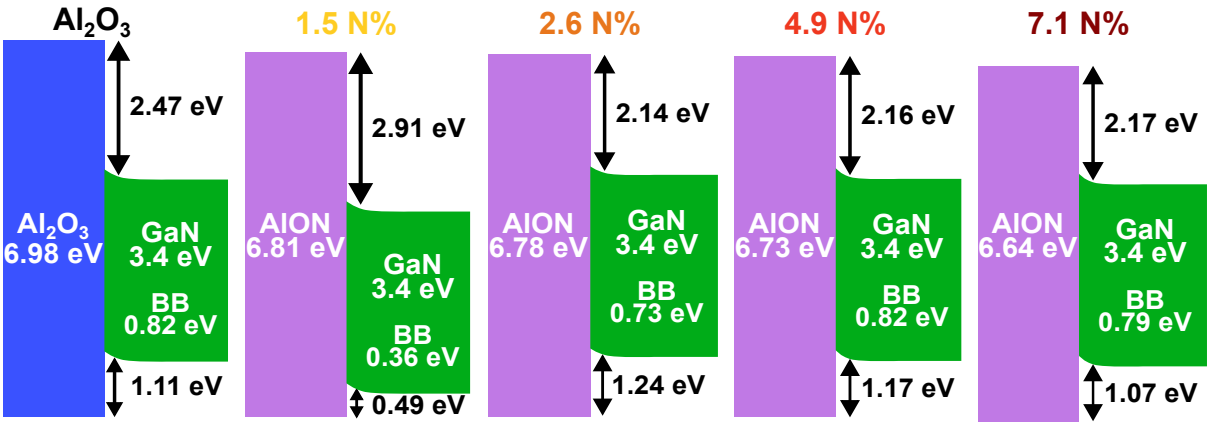


*Figure 5.20: Al_2O_3/etched GaN from **Chapter3** with a PDA at 500°C and AlON/etched GaN stack at different nitrogen concentrations with a PDA at 800°C. The Ga3d spectra were analyzed at the take-off angle of 45°.*

stack from **Chapter 3** (with a PDA at 500°C), AlON for most of the different nitrogen concentrations have a similar band alignment, as represented in **Figure 5.20**.

Concerning GaN's band bending demonstrated in **Figure 5.20** and summarized in **Table 5.4**, it reveals an upward band bending for all AlON samples in the order of 0.3 0.8 eV, meaning that the net interface charges is positive. By using **Equation 2.33** in **Section 2.3.1.8**, these charges are in the order of -1×10^{12} cm^{-2}, with added positive interface charge in the range of 1.7×10^{13} cm^{-2}. This value is close to the value extracted for the optimal Al_2O_3/etched GaN stack (1.59×10^{13} cm^{-2}) but lower to the reported value of 2.27×10^{13} cm^{-2} for Al_2O_3/GaN extracted with *C-V* measurements [253]. The upward band bending slightly increases with nitrogen concentration, but especially after 1.5 N%. Therefore, as deduced from XPS measurements, there's a slight different amount of interface charges between 1.5 N% and the other AlON samples. Nonetheless, this difference is not observed with the extracted V_{FB}. The origin for the charges can be both the oxide at the interface since it reduces with increasing nitrogen content, or any donor defect in AlON and/or GaN.

Sample	1.5 %N	2.6 %N	4.9 %N	7.1 %N
Band bending (eV)	0.36	0.73	0.82	0.79
$\sigma^{net}_{interf.}$ cm^{-2}	$-.38 \times 10^{12}$	-2.01×10^{12}	-2.13×10^{12}	-2.09×10^{12}
$\sigma^{positive}_{added}$ cm^{-2}	1.66×10^{13}	1.60×10^{13}	1.59×10^{13}	1.59×10^{13}

Table 5.4: Extracted GaN's band bending using the Ga3d spectra at the take-off angle of 45°. The net interface charges are calculated from the band bending. The added positive interface charges are calculated by subtracting the net surface charges by GaN's spontaneous-polarization-induced negative charges (-1.8×10^{13} cm^{-2}).

5.2.3 Conclusions

The impacts of different nitrogen concentrations in AlON and of Post-Deposition Anneal on the MOS capacitances AlON/etched GaN electrical performances were investigated and compared to Al_2O_3. Without annealing, an increase of V_{FB} with nitrogen content was observed in line with the literature. Hysteresis is well improved by the presence of nitrogen when compared to Al_2O_3, especially for a measuring temperature of 150°C. The increase of electron trapping with nitrogen seems to originate from the presence of impurities related to the deposition process.

With annealing, stable AlON layers and interfaces with etched GaN were observed for a PDA up to 800°C. When combined with low nitrogen content, V_{FB} was increased and stabilized, whereas the hysteresis or electron trapping was strongly reduced by the PDA for AlON and Al_2O_3 samples thanks partly to hydroxyl groups' reduction. Moreover, AlON has a lower hysteresis than Al_2O_3 at 150°C while having a lower D_{it}, highlighting the superior MOS electrical properties of AlON/etched GaN in comparison with Al_2O_3/GaN.

Finally, the energy band gap for the different nitrogen concentrations with PDA at 800°C is comprised between that of Al_2O_3 and that of AlN, with higher nitrogen concentration leading to a lower energy band gap. The extracted band alignments highlight a high barrier for electrons ($\backsim$2-2.9 eV) whereas the barrier for holes is around 0.5$\backsim$1 eV.

5.3 Conclusion of this chapter

AlON deposition was developed with a supercycle approach by alternating thin AlN PE-ALD and oxidation with an O_2 plasma. By this process, a suitable range of 1.5 to 7.6 % in nitrogen concentration is obtained and controlled by the deposited AlN thickness. A uniform layer and stable interface are also observed while the extracted energy band gap is sufficiently high for the MIS gate. Although a mechanism with the AlN deposited thickness is proposed to explained the formation of a uniform AlON with a controlled nitrogen content, a kinetic study of the proposed AlON deposition could further

As expected, the increase in nitrogen increases the V_{FB} of the AlON/GaN MOS capacitors. The electron trapping is reduced compared to Al_2O_3, especially at the higher measuring temperature of 150°C. With annealing, AlON thermal stability is confirmed to be higher than 600°C, allowing it to undergo PDA temperatures of 800°C. The latter allows to further decrease the electron trapping by reducing the presence of defects in the AlON layer and at the interface. V_{FB} is equally stabilized in comparison with Al_2O_3 after PDA. Considering the hysteresis and the interface quality at both measuring temperatures, the more suitable nitrogen concentrations are around 1.5 and 2.6 % with annealing between 600 and 800°C.

In perspective, it would be interesting to study the presence of interfacial and/or bulk charges for the different nitrogen concentrations through the different PDA temperatures. This would allow to understand which charges are driving the electrostatic control of our gate and further optimize the AlON/etched GaN stack. Moreover, although a mechanism with the AlN deposited thickness is proposed to explained the formation of a uniform AlON with a controlled nitrogen content, a kinetic study of the proposed AlON deposition could be interesting to better comprehend the deposition process and perhaps optimize it further. If employed in a MOSc-HEMT, these results seem to indicate that AlON would have better performance than Al_2O_3 as a gate dielectric.

General conclusion and perspectives

General conclusion

With increasing demand for efficient power devices, AlGaN/GaN-based MOSc-HEMT is an interesting solution for Normally-OFF low-voltage power devices (650 V). However, the Dielectric/GaN interface at the MIS or MOS gate is a critical device aspect preventing the MOSc-HEMT from entering the power market. Thus, the aim of this PhD project was to understand the impact of fabrication steps on the MIS gate by comparing physical-chemical and electrical characterizations and to optimize the Dielectric/GaN stack. Different paths of optimization are possible from reduction of the etching damage, use of an efficient surface preparation and deposition of a reliable dielectric. In this work, the focus was mainly on the study of different dielectrics layers and tuning their properties (bulk and interface) through Post-Deposition Annealings.

Different characterization techniques were used or specifically developed to study the MIS gate stack. Planar MOS capacitors were fabricated to easily study different gate stack processing. Flat-Band Voltage (V_{FB}) and its hysteresis (ΔV_{FB}) were employed to have insight on the transistor threshold voltage and its hysteresis, while conductance measurements allowed to extract information on the interface states density. The desired properties are low V_{FB} hysteresis (<100 mV), high V_{FB} and low D_{it} ($< 10^{11}$). Combined with the electrical measurements, physical-chemical measurements were performed to understand the impact of fabrication steps on the electrical parameters. HAXPES and ToF-SIMS are useful techniques to finely analyze the chemistry of both the stack and the interface, while the use of Power Spectral Density (PSD) on AFM images allows to characterize the lateral GaN surface roughness and have an idea of the impact of roughness on the Surface-Roughness limited mobility (μ_{SR}).

First, the Al_2O_3/etched GaN gate stack process of reference for the MOSc-HEMT fabrication was studied with a focus on the impact of etching roughness and of an additional Post-Deposition Anneal of Al_2O_3. The use of PSD was evaluated, revealing a small variation of the intensity extracted with the method. This method highlights clear differences between an as-grown and etched surface in terms of PSD intensity distribution, while these differences are observed with difficulty when using RMS as a roughness parameter. Four different etching processes were analyzed with PSD. No significant differences between the processes was observed implying a limited impact of roughness on μ_{SR}. This is confirmed by the measurements of the gate bottom mobility which is already reduced for some processes at a low electron density due to other scattering mechanisms ($\mu_{bot} \approx 160\ cm^2.V^{-1}.s^{-1}$). Therefore, for the MOSc-HEMT process of reference and the 3 other etching variations, the roughness induced by etching is not a limiting factor to the device performance. The study of PDA revealed an optimal temperature of 500°C in which ΔV_{FB} is minimal (56 mV) due to the reduction of GaO_x and -OH groups. V_{FB} is reduced, due to the reduction of fluorine presence in the stack. Moreover, the extraction of interface states density (D_{it}) highlights low density in the order of 5×10^{10} $eV^{-1}.cm^{-2}$, probably because the etching process and the wet cleaning sequence are already optimized and leave few interface states. Applying an annealing after deposition reduces a D_{it} peak at 0.3 eV. However, over 500°C in PDA, hysteresis rises again and an

onset of crystallization is observed. Such degradation is still observed when the final thermal budget is applied. Therefore, while the etching and the wet processes enable an optimized Al_2O_3/GaN interface, the low thermal stability of Al_2O_3 hinders further reduction of defects in the dielectric and the overall thermal budget that can be applied during the fabrication of the MOSc-HEMT.

To increase the thermal stability of the deposited dielectric, alternatives such as AlSiO and AlON were studied. An AlSiO with 50% in Si content deposited on as-grown GaN by Al_2O_3 and SiO_2 ALD nanolaminates was investigated for different different PDA temperatures. The higher thermal stability of AlSiO is confirmed. An optimal PDA temperature of 750°C is observed in which the hysteresis is reduced and both the AlSiO layer and the interface are kept stable. At 850°C, the AlSiO layer starts to crystallize and a GaO_x growth is noticed. The introduction of a low temperature SiO_2 interfacial layer increases the thermal stability by 100°C but introduces interface states and electron traps increasing D_{it} and ΔV_{FB}. If at 950°C AlSiO starts to crystallize, both the hysteresis and interface states are strongly reduced with values lower than the observed for the 750°C PDA without interfacial SiO_2. However, both the AlSiO and the AlSiO/SiO_2 stacks suffer from reversed hysteresis linked to mobile charges, possibly explained by Na^+/K^+ impurities. Such property is not desirable for MOS gates in power devices since it induces V_{TH} instability when the operating temperature is high (i.e. 150°C). Therefore, in order to employ the AlSiO/SiO_2, this issue needs to be tackled with cleaner processes.

The AlON deposited on etched GaN by a PE-ALD supercycle approach was described and studied for different PDA temperatures. By controlling the thickness (or the number of cycles) of PE-ALD AlN being oxidized by an O_2 plasma, the nitrogen content was controlled in a range between 1.5 to 7.1%N while maintaining a uniform AlON layer. An increased V_{FB} and ΔV_{FB} is observed for an increasing nitrogen, in correlation with increasing -OH groups and carbon with nitrogen content. With increasing PDA temperature, the hysteresis is reduced partly explained by the reduction of -OH groups while V_{FB} remains in overall stable. The higher thermal stability for AlON is also confirmed together with a stable interface with etched GaN. In comparison with Al_2O_3, AlON offers a significantly reduced hysteresis and interface states density for a N content of 1.5 or 2.6%. This is especially observed at a high measuring temperature. Therefore, optimal AlON/etched GaN stack and interface can be obtained with a nitrogen content between 1.5 to 2.6%N and annealed above 600°C.

The following table summarizes the obtained results for each dielectrics with both electrical and material properties:

	30 nm Al_2O_3 on etched GaN	19nm $Al_{0.5}Si_{0.5}O$	15 nm AlON (1.5% N) on etched GaN
V_{FB}	-0.35 V (PDA 500°C)	-0.37 V (PDA 750°C)	0.24 V (PDA 800°C)
V_{FB} hysteresis	56 mV (PDA 500°C)	76 mV (PDA 750°C)	50 mV (PDA 800°C)
D_{it} at 0.49 eV ($10^{10} eV^{-1}.cm^{-2}$)	4.83±0.21 (PDA 500°C)	/ (PDA 750°C)	2.63 ± 0.38 (PDA 800°C)
Crystallization T°C on GaN	around 600°C	850	>800
Advantages	High band gap Low GaN oxidation	Highest band gap	Lower hysteresis at 150°C High band gap Low GaN oxidation
Drawbacks	Low T°C stability	GaO_x growth after 750°C Mobile charges	Low hole barrier

Table 5.5: Summary of properties observed for the optimal PDA temperature of each studied dielectric.

Considering the different performed studies, the following conclusions can be made:

- The etching and the cleaning sequences used in the MOSc-HEMT process flow is already optimized with both limited impact on dielectric/GaN interface roughness and interface states.
- Al_2O_3 is a good candidate as a dielectric for the MOS gate, with reduced ΔV_{FB} and interface states after an annealing at 500°C. But its thermal stability limited at 600°C hinders the use of higher annealing temperature used to reduces defects in the dielectric, but also limits the overall thermal budget applied in the MOSc-HEMT fabrication process. Other dielectrics with higher thermal stability are necessary.
- Alternative such as AlSiO and AlON are promissing with higher thermal stability and lower V_{FB} instability. More work is needed to optimize the AlSiO/GaN stack in terms of ΔV_{FB}. AlON present interesting properties when annealed at 800°C, both physical (higher thermal stability) and electrical (lower ΔV_{FB} and D_{it} at room and at 150°C). The later could replace Al_2O_3 or be used as an interfacial layer.
- To make a reliable recessed MOS gate, the interface oxidation needs to be controlled, the etching damage can be reduce with low etching process and cleaning sequences (mostly with sequences with HF), the dielectric layer has to be controlled and its defects reduced as much as possible.

Limits of this work and perspectives

Although a number of additional information on the Dielectric/GaN interface and stack was obtained with this PhD project alongside the study of alternative dielectrics, some elements still need to be answered and pondered:

- All the presented studies were performed on planar MOS capacitances, simulating the gate bottom cavity for simplicity, while the sidewalls are omitted. However, a recent work in our group highlights the impact of sidewall morphology on the transistor parameters such as V_{TH} and mobility

[46]. Therefore, until which point is the simple gate bottom model valid? According to Hirai et al. [106], m-plane have a higher V_{FB} than a-plane but similar D_{it}. No comparison was performed with c-plane. Hence, it would be interesting to compare m-planes with c-planes.

- The surface roughness is not the limiting factor on the gate bottom, this observation seems to be also applied to the sidewalls when the extracted mobility for the four etching process are compared. Nonetheless, the strong degradation for the confidential 1# etching process could be explained by another limit factor. As stated, the interface states could be responsible. Therefore, are interface state density at the gate bottom related to this degradation? Moreover, if the POR etching and cleaning sequence is proven to reduce D_{it} in the limited energy range probed by the conductance method ($E_C - E_T = 0.05 - 0.85$), D_{it} affecting the interface could also be presented close to the valence band. How can this band gap portion be analyzed? Some groups have reported the use of DLOS (Deep Level Optical Spectroscopy) for such analyses [239], which could be a solution.
- For AlSiO and AlSiO/SiO_2, where do the Na^+/K^+ impurities come from and are they related to the Si concentration as reported by Sayed et al. [152]? What is the trade-off between Si content and $V_{FB}/\Delta V_{FB}$?
- For AlON, is the increase of V_{FB} related to interfacial charges or bulk charges in the dielectric?

With its limitations, the presented methodology allowed to have a comprehensive view of the Dielectric/GaN interface. Further work on the deposition and annealing of AlSiO layers can be made with different Si% content while the SiO_2 layer can be optimized by increasing the deposition temperature. Such developments are expected to be carried out by a new PhD project at CEA-Leti. For AlON, while it's an interesting substitute to Al_2O_3 for MOSc-HEMT, this dielectric could also be applied to vertical GaN trench-MOSFET as expected to be performed on a PhD project at CEA-Leti and LTM. As described in the introduction, an interfacial layer such as AlN can be introduced alongside an *in-situ* plasma cleaning in another to minimize the surface oxidation during oxide deposition [44], [82], [117]. Such process could be introduce in the MOSc-HEMT process flow to improve V_{TH} subthreshold slope linked partially to D_{it}. AlON could also be used as an interfacial layer and be combined with Al_2O_3 or AlSiO for instance. To further take into account the sidewalls' contribution, dedicated MOS capacitors on the sidewalls could be a great contribution to the study of the MOSc-HEMT gate cavity, with new challenges arising in terms of physical-chemical characterizations for such 3D configuration. Likewise, while the conductance method on p-GaN or DLOS can be performed to extract D_{it} for the gap portion close to GaN's valence band, the use of ECV could be an interesting method to analyze the surface states with p-GaN (or interface states when a dielectric is deposited) as already explored for n-GaN [187]. Finally, ab-initio studies on amorphous dielectric/GaN interface could be performed to further understand the defects and their nature at or close to the interface.

Annexes

A Annex Chapter 2

Thickness extraction by AR-HAXPES

The XPS intensity from GaN can be expressed in function of the upper dielectric and the interfacial gallium oxide as:

$$I_{GaN} = I^{\infty}_{GaN} \exp\left(\frac{-d_{GaO_x}}{\lambda_{GaO_x}\sin(\theta)}\right)\exp\left(\frac{-t_{diel}}{\lambda_{diel}\sin(\theta)}\right) \tag{1}$$

Similarly, the intensity coming from GaO_x is:

$$I_{GaO_x} = I^{\infty}_{GaO_x}\left(1-\exp\left(\frac{-d_{GaO_x}}{\lambda_{GaO_x}\sin(\theta)}\right)\right)\exp\left(\frac{-t_{diel}}{\lambda_{diel}\sin(\theta)}\right) \tag{2}$$

The ratio R of GaO_x and GaN XPS intensity can then be written as:

$$R = \frac{I_{GaO_x}}{I_{GaN}} = \frac{I^{\infty}_{GaO_x}\left(1-\exp\left(\frac{-d_{GaO_x}}{\lambda_{GaO_x}\sin(\theta)}\right)\right)\exp\left(\frac{-t_{diel}}{\lambda_{diel}\sin(\theta)}\right)}{I^{\infty}_{GaN}\exp\left(\frac{-d_{GaO_x}}{\lambda_{GaO_x}\sin(\theta)}\right)\exp\left(\frac{-t_{diel}}{\lambda_{diel}\sin(\theta)}\right)} \tag{3}$$

$$R = R_0\frac{\left(1-\exp\left(\frac{-d_{GaO_x}}{\lambda_{GaO_x}\sin(\theta)}\right)\right)}{\exp\left(\frac{-d_{GaO_x}}{\lambda_{GaO_x}\sin(\theta)}\right)} \tag{4}$$

$$R = R_0\left(\exp\left(\frac{d_{GaO_x}}{\lambda_{GaO_x}\sin(\theta)}\right)-1\right) \tag{5}$$

$$\tag{6}$$

With $R_0 = I^{\infty}_{GaO_x}/I^{\infty}_{GaN}$. From the expression of R, the following expression can be written:

$$\ln\left(1+\frac{R}{R_0}\right) = \frac{d_{GaO_x}}{\lambda_{GaO_x}\sin(\theta)} \tag{7}$$

B Annex Chapter 3

Without final thermal budget

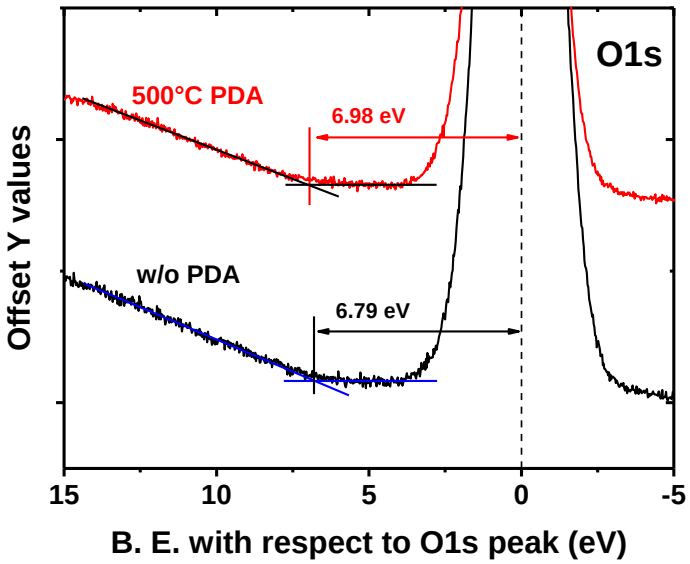


Figure A.1: O1s electron loss spectra for the Al_2O_3/etched GaN without and with a PDA at 500°C.

C Annex Chapter 4

Annealing over 750°C: Degraded AlSiO/GaN stack

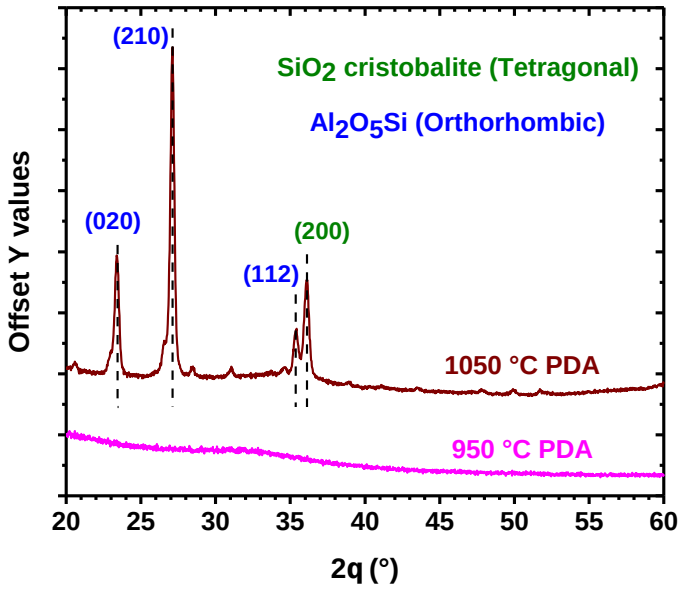


Figure A.2: GIXRD analyses for AlSiO samples with PDA at 950°C and 1050°C with incident angle being 2°. The diffraction patterns are observed after 1050°C PDA, with both crystallized Al_2O_5Si and SiO_2 being observed.

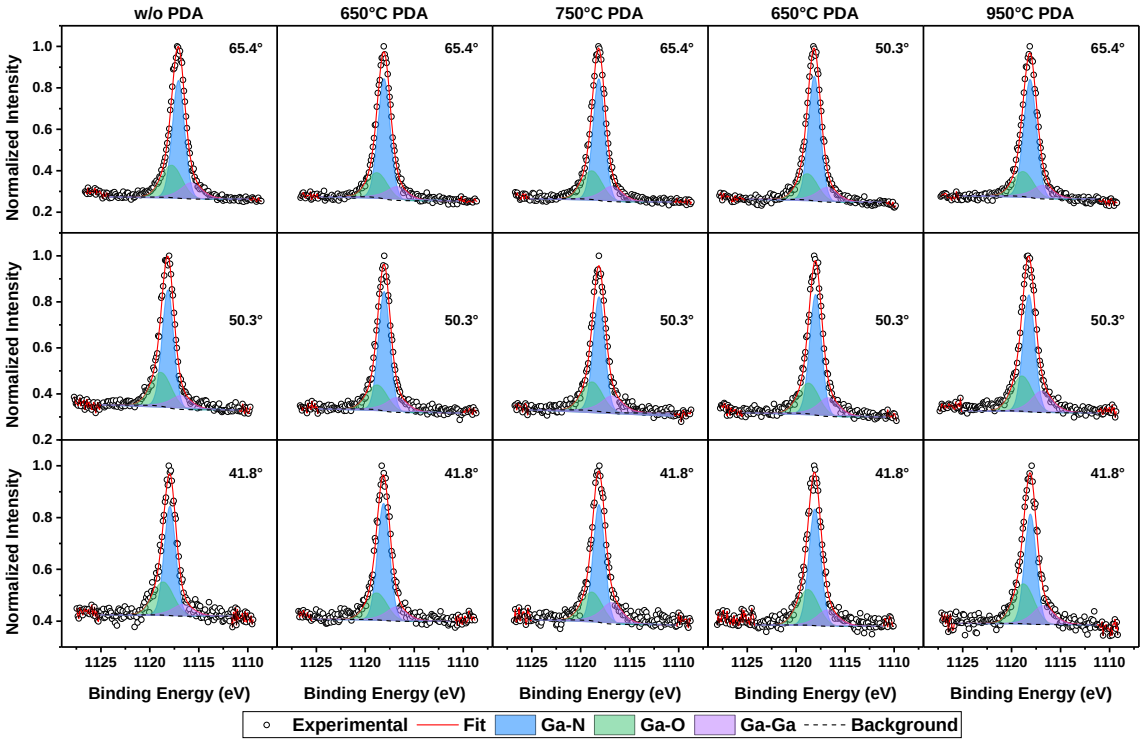


Figure A.3: AR-HAXPES analysis of $Al_{0.5}Si_{O.5}O_x$ for different PDA temperatures. The intensity is normalized by the experimental peak value.

D Annex Chapter 5

Impact of annealing

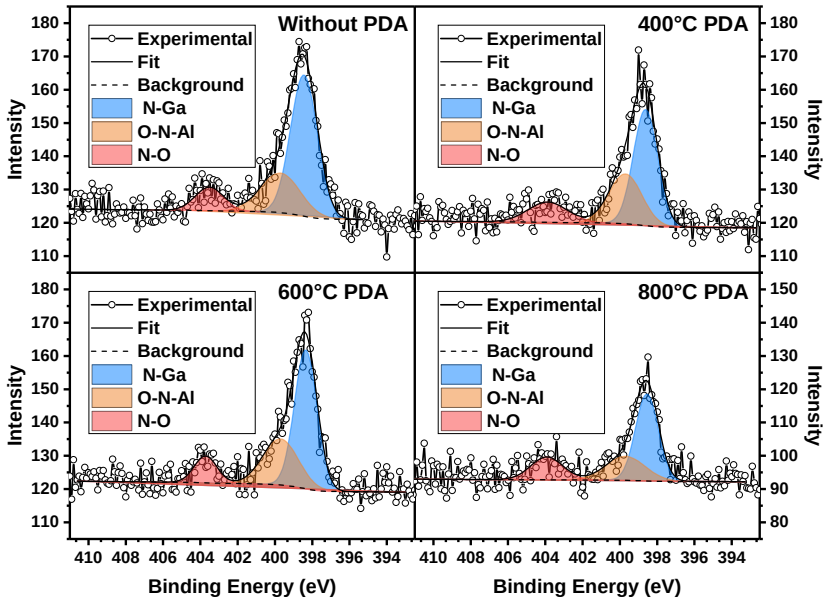


Figure A.4: HAXPES analysis of N1s spectrum for 4.9N% AlON with different PDA temperatures.

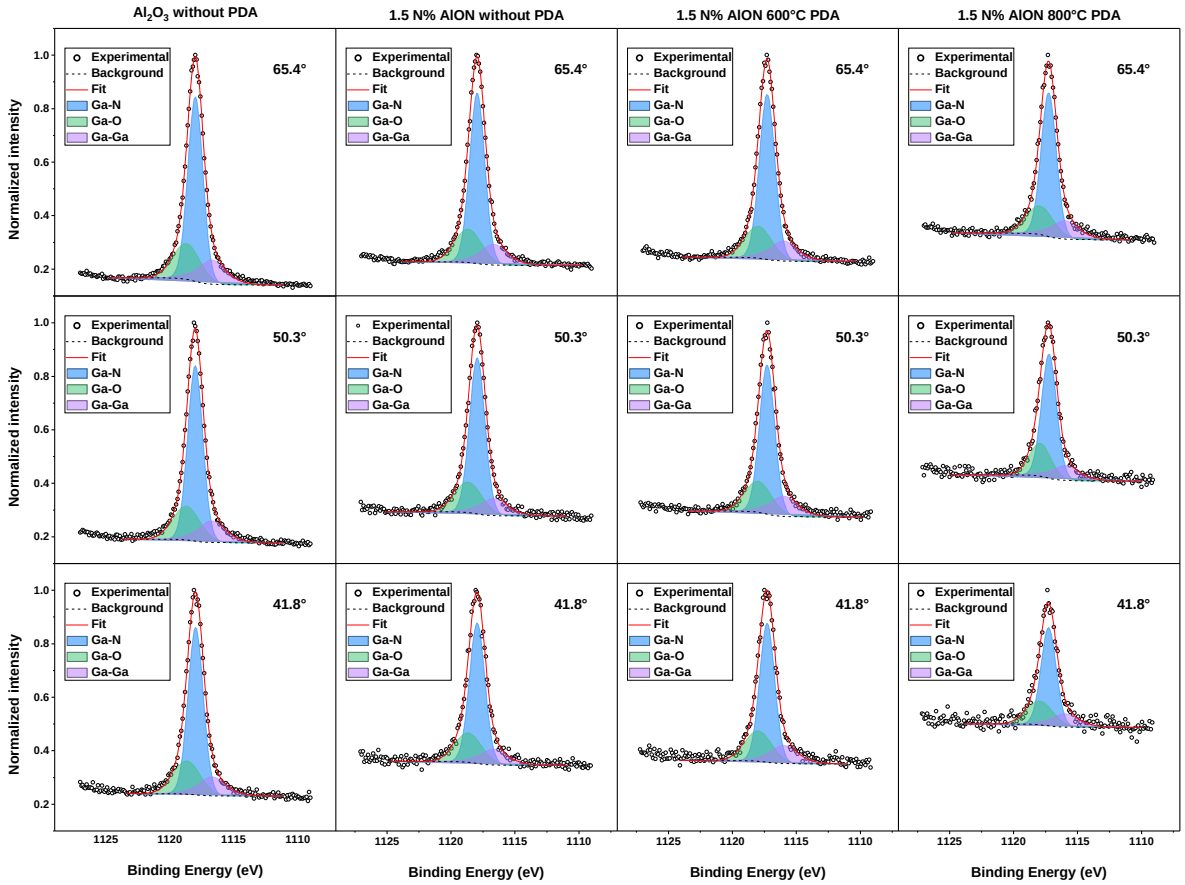


Figure A.5: AR-HAXPES analysis of Al_2O_3 without PDA, 1.5 N% AlON without, with 600°C and 800°C PDA. The intensity is normalized by the experimental peak value.

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- **P. Fernandes Paes Pinto Rocha**, L. Vauche, P. Pimenta-Barros, S. Ruel, R. Escoffier, and J. Buckley, "Recent Developments and Prospects of Fully Recessed MIS Gate Structures for GaN on Si Power Transistors" In: *Energies* 16.7 (March 24 2023), p. 2978. DOI: 1996-1073/16/7/2978.
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- T. Spelta, M. Veillerot, E. Martinez, D. Mariolle, N. Chevalier, **P. Fernandes Paes Pinto Rocha**, B. Salem, L. Vauche and B. Hyot, "Impact of etching process on Al_2O_3/GaN interface for MOSc-HEMT devices combining ToF-SIMS, HAXPES and AFM", In: EuroSOI-ULIS 2023, *Solid-State Electronics* 208 (Aug. 2023), p. 108743. DOI: 10.1016/j.sse.2023.108743
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Optimisation de l'interface diélectrique/GaN pour la grille MIS des transistors de puissance

Résumé

Pour atteindre les objectifs de l'Accord de Paris sur le climat, il est crucial de diminuer la consommation énergétique mondiale. Un levier de diminution est la réduction des pertes lors des étapes de conversion d'énergie électrique via des composants de puissance GaN sur Si plus petits et plus efficaces. L'architecture MOSc-HEMT («MOS-channel High Electron Mobility Transistor ») à tension de seuil V_{TH} positive (ou Normally-OFF) est en développement au CEA-Leti afin d'adresser ces besoins pour des convertisseurs de basse tension (< 900 V). Contrairement à la grille p-GaN, le caractère Normally-OFF est obtenu en gravant la barrière AlGaN puis en fabriquant une grille MIS en utilisant l'Al_2O_3 comme diélectrique de grille. Toutefois, la présence de rugosité et de pièges à l'interface diélectrique/GaN est critique pour la fiabilité du transistor, pouvant réduire le V_{TH}, introduire des instabilités du V_{TH} et dégrader la mobilité des électrons. Il est ainsi essentiel d'optimiser l'empilement diélectrique/GaN afin de viabiliser la fabrication des MOSc-HEMTs. Ainsi, l'objectif de cette thèse est d'optimiser l'interface diélectrique/GaN en développant des méthodes de caractérisation physico-chimique en complément de véhicules de test électrique simplifiés, et en utilisant ces méthodes pour étudier l'impact de différents procédés de fabrication. Cela a permis dans un premier temps d'étudier l'empilement Al_2O_3/GaN gravé en : 1) analysant l'impact de la gravure sur la mobilité des électrons ; 2) étudiant l'impact des recuits après dépôt (PDA). Dans un deuxième temps, des diélectriques alternatifs à l'Al_2O_3 tels que l'AlSiO et l'AlON ont été développés et caractérisés en vue d'augmenter la stabilité thermique du diélectrique et de réduire les instabilités de V_{TH}. Ces travaux ont permis d'obtenir des informations sur l'interface diélectrique/GaN et de proposer des alternatives à l'Al_2O_3, comme l'AlON accompagné d'un recuit à haute température.

Mots-clés: Puissance, Grille, Interface, GaN, Transistors

Optimization of dielectric/GaN interface for MIS gate power devices

Abstract

To achieve the Paris Climate Agreement objectives, it is crucial to reduce the global energy consumption. One solution is the reduction of energy losses during power conversion by using smaller and more efficient GaN-on-Si power converters. The MOSc-HEMT ("MOS-channel High Electron Mobility Transistor") architecture with positive threshold voltage V_{TH} (or Normally-OFF) is currently under development at CEA-Leti to address these needs for low-voltage converters (< 900 V). Unlike p-GaN gate, the Normally-OFF behavior is achieved by etching the AlGaN barrier and then fabricating a MIS gate using Al_2O_3 as the gate dielectric. However, the presence of roughness and traps at the dielectric/GaN interface is critical to the transistor reliability, potentially reducing V_{TH}, introducing V_{TH} instabilities and degrading the electron mobility. It is therefore essential to optimize the dielectric/GaN stack in order to fabricate reliable MOSc-HEMTs. Thus, the aim of this thesis is to optimize the dielectric/GaN interface by developing physico-chemical characterization methods as a complement of simplified electrical test vehicles, and using these methods to study the impact of different fabrication processes. At first, the etched Al_2O_3/GaN stack was studied by: 1) analyzing the impact of etching on the electron mobility; 2) studying the impact of Post-Deposition Annealing (PDA). Secondly, alternative dielectrics to Al_2O_3 such as AlSiO and AlON were developed and characterized in order to increase the dielectric's thermal stability and to reduce V_{TH} instabilities. This work provided information on the dielectric/GaN interface and led to the proposal of alternatives to Al_2O_3, such as AlON followed by high-temperature annealing.

Keywords: Power, Gate, Interface, GaN, Transistors