Condition and Health Monitoring of Modular Multilevel Converter for HVDC grids

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Du diagnostic au pronostic de l'état de santé des IGBT dans un convertisseur modulaire multiniveaux pour les réseaux HVDC

Devant le jury composé de :

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Condition and Health Monitoring of Modular Multilevel Converter for HVDC Grids

A Dissertation submitted to
UNIVERSITE CLAUDE BERNARD LYON 1

In partial fulfillment of the requirements for the degree of
DOCTOR OF PHILOSOFY

Presented by:

Diego Alejandro VELAZCO NAVARRO

Supervised by: Prof. Guy Clerc
Co-supervised by: Dr. Emmanuel Boutleux
2023

A mis papás Franz y Patricia
por su esfuerzo y su apoyo incondicional

A mi hermano Alvaro
mi compañero de la vida

y a mi abuela María Paz
donde quiera que estés...

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Abstract

The growing power and energy demand, as well as the integration of new renewable sources into the electrical system and the long distances between electrical consumers and producers are pushing the actual AC grid to evolve. Hence, HVDC has emerged as a promising solution for upgrading the power transmission infrastructure and meet the demanding requirements and future needs of the electrical grid. Moreover, HVDC is nowadays the preferred technology for bulk power transmission and the integration of large-scale renewable sources such as offshore windfarms.

One fundamental component of HVDC systems is the converter station. At the ends of an HVDC line, the converter station is responsible for interfacing the DC link with the AC grid. Among the different types of technology for converter stations VSC have gained in relevance in the last few decades, as they provide improved functionalities when compared to the traditional converters employed for HVDC applications. Concerning VSC topologies, the MMC has emerged as the most advantageous topology and the main candidate for future HVDC projects.

The MMC is a scalable converter composed mainly of stacks of SMs that allow its operation. Each SM is composed itself by a large storage capacitor and IGBT modules used for the insertion or the bypass of the capacitor. As power transmission is a critical application, HVDC systems are subjected to very demanding reliability and availability requirements and the MMC is not the exception. This thesis addresses the condition monitoring and the prognosis of the remaining useful life of IGBT modules in a HVDC-MMC application, as these elements were identified as one of the weakest components present in converter applications.

A physics-of-failure approach is chosen for the prognosis scheme. This scheme uses the thermal loading of the semiconductor devices of a HB-SM for making computations of the lifetime consumption in the evaluated period. Then, from this lifetime estimation the remaining useful life can be inferred. Additionally, the prognosis scheme allows the calculation of the reliability of the HB-SM by considering the reliability functions of its composing elements. Consequently, this calculation is used for computing the redundancy needed for attaining the target availability values with the help of a Markov Chain and Monte Carlo simulations.

Another important subject addressed in this thesis is the condition monitoring of IGBT modules. For this purpose, a Power Cycling testbench was developed. The $V_{CE(on)}$ was chosen as the parameter for tracking the evolution of the degradation state of the power device throughout the cycling tests. Consequently, an online $V_{CE(on)}$ measurement board was conceived and developed. In order to get more relevant insights of the cycling protocol applied, a strategy for the online estimation of the junction temperature of IGBT devices was developed and it is based on the use of a Kalman filter. This strategy also enables to perform an estimation of the degradation of the state-of-health of the IGBT by analyzing the Thermo-Sensitive Electrical Parameters.

Résumé

Les réseaux de transport d'électricité doivent s'adapter pour faire face aux défis de la croissance de la demande d'énergie, de la rapide expansion des moyens de production des énergies renouvelables et de l'éloignement des centres de production et consommation. Dans ce contexte, la transmission d'énergie en courant continu à très haute tension (HVDC) commence à s'imposer comme la technologie privilégiée pour les applications de forte puissance.

Dans les systèmes de transmission HVDC, le convertisseur de puissance joue un rôle majeur. Cet équipement réalise la conversion du courant continu (DC) en courant alternatif (AC), pour pouvoir interfacer le lien HVDC au réseau de puissance existant en AC. Parmi les différents types des technologies des convertisseurs pour les réseaux HVDC, les convertisseurs à source de tension (VSC) supplantent peu à peu les convertisseurs à source de courant (LCC) car ils fournissent des fonctionnalités améliorées comme un meilleur encombrement et une meilleure compatibilité avec un futur réseau maillé HVDC.

En ce qui concerne les topologies VSC, le convertisseur MMC est aujourd'hui la topologie de référence. Il s'agit d'une structure modulaire, composée principalement de piles de sous-modules (SMs). Chaque SM est composé en lui-même d'un condensateur et de modules IGBT utilisés pour l'insertion ou le bypass du condensateur.

Etant donné que le transport d'énergie est une application critique, les systèmes HVDC sont soumis à des normes de fiabilité et de disponibilité très exigeantes et le MMC ne fait pas l'exception. C'est pourquoi ce travail aborde la surveillance de l'état de santé et le pronostic de la durée de vie restante des IGBT présents dans les SMs du convertisseur. Ce travail se focalise sur les IGBT car ils ont été identifiés comme l'un des composants les plus fragiles dans les convertisseurs de puissance.

Une approche par analyse de la physique de la défaillance a été choisie pour mettre au point une méthodologie de pronostic de la vie restante du convertisseur. Cette démarche utilise le profil thermique subi par les semiconducteurs pour calculer la consommation de la durée de vie écoulée dans la période évaluée et en déduire la durée restante. Par ailleurs, cette démarche permet de faire des calculs de la fiabilité des SMs en considérant la consommation de la durée de vie et la fonction de fiabilité des éléments qui le composent. En outre, des calculs des niveaux de redondance à installer, pour atteindre aux besoins de disponibilité, sont réalisés grâce à cette méthodologie.

Un autre sujet important abordé dans cette recherche est le suivi de la dégradation des modules IGBT. Pour étudier cela, un banc de cyclage actif a été développé. La tension $V_{CE(on)}$ a été choisie comme paramètre de surveillance pour suivre la dégradation du module tout au long des tests de cyclage. Par conséquent, une carte de mesure de cette tension a été développée et cette carte a permis de développer une méthode pour estimer la température de jonction des IGBT. Elle se base sur un filtre de Kalman, dont le réglage est réalisé en utilisant la méthode ALS qui permet d'obtenir le réglage optimal du filtre. Les essais ont aussi permis de tracer l'évolution d'autres paramètres sensibles à la dégradation.

Resumen

Las redes de transporte de energía eléctrica deben adaptarse a los desafíos que conlleva el incremento de la demanda de energía, la expansión de las fuentes de energías renovables y al alejamiento de los centros de producción de los centros de consumo. Es bajo este contexto, que los sistemas de transporte de electricidad en corriente continua y alta tensión (HVDC) han surgido como una solución prometedora para mejorar la infraestructura de los sistemas de transmisión en corriente alterna y cumplir con los exigentes requisitos de las futuras redes eléctricas.

En los sistemas de transmisión HVDC, el convertidor de potencia juega un rol fundamental. Éste último realiza la conversión de corriente continua (CC) en corriente alterna (CA), para poder interconectar una línea HVDC al sistema de potencia existente. Entre las diferentes tecnologías para redes HVDC, los convertidores a fuente de tensión (VSC) están remplazando progresivamente a los convertidores a fuente de corriente (LCC). En efecto, los convertidores VSC otorgan nuevas funcionalidades que facilitarían la implementación de redes multiterminales en CC.

Dentro de las topologías VSC, el convertidor modular multinivel (MMC) es hoy en día, la topología predilecta para nuevas líneas HVDC. Se trata de una estructura modular compuesta de submódulos (SMs). Cada SM está compuesto de un condensador y de módulos IGBT que son utilizados para la inserción o el bypass del condensador.

Dado que el transporte de energía es una aplicación critica, los sistemas HVDC se rigen por estrictas normas de fiabilidad y disponibilidad. Es por este motivo que este trabajo aborda la supervisión del estado de salud y el pronóstico de la vida restante de los IGBTs presentes en los SMs del convertidor MMC. Esta tesis hace énfasis en los IGBTs, puesto que éstos han sido identificados como uno de los componentes más frágiles dentro de los convertidores de potencia.

Un enfoque basado en el análisis de las causas físicas de la degradación ha sido adoptado para diagnosticar la vida restante de los SMs. Este enfoque utiliza el perfil térmico experimentado por los IGBTs para calcular el consumo de la duración de vida en el periodo evaluado y deducir la vida restante. Además, este método permite calcular la fiabilidad de los SMs tomando en cuenta el perfil de carga y los indicadores de fiabilidad de sus elementos. También, el cálculo de niveles de redundancia es posible gracias a este enfoque.

Otro aspecto fundamental abordado en este trabajo es la supervisión de la degradación de los módulos IGBT. Un banco de envejecimiento basado en variaciones térmicas ha sido desarrollado para este fin. La tensión $V_{CE(on)}$ ha sido escogida como un parámetro para el monitoreo de la degradación del módulo durante las pruebas de envejecimiento. Consecuentemente, una tarjeta electrónica para medir este parámetro ha sido desarrollada y ha permitido la implementación de un método de estimación de la temperatura del IGBT. Dicha metodología utiliza un filtro de Kalman que es parametrizado gracias al algoritmo ALS, lo cual asegura un funcionamiento optimo del filtro y una estimación precisa de la temperatura del IGBT. Finalmente, las pruebas de envejecimiento han permitido monitorear la evolución de otros parámetros sensibles a la degradación.

Contents

List of abbreviations

AC	Alternating Current
ACM	Autocovariance Matrix
ADC	Analog to Digital Converter
ALS	Autocovariance Least-Squares Method
ANFIS	Adaptative Neuro-Fuzzy Inference System
ANN	Artificial Neural Network
AVM	Average Value Models
BCA	Balancing Control Algorithm
CDF	Cumulative Distribution Function
CHB	Cascaded H-Bridge Converter
CIGRE	Conseil international des grands réseaux électriques
CM	Condition Monitoring
CSC	Current-Source Converter
CTE	Coefficient of Thermal Expansion
DBC	Direct Bonded-Copper Layer
DC	Direct Current
DSEP	Damage-Sensitive Electrical Parameter
DUT	Device Under Test
EMI	Electromagnetic Interference
ENTSO-E	European Network of Transmission System Operators for Electricity
EOL	End-of-Life
EOS	Electrical Overstress
FB-SM	Full-Bridge Submodule
FC	Flying Capacitor Converter
FEA	Finite Element Analysis
FIT	Failures In Time (number of failures per 10^9 hours)
FMMEA	Failure Mode, Mechanism and Effect Analysis
FWD	Free-Wheeling Diode
GD	Gate Driver
GPIO	General Purpose Input/Output ports
GPR	Gaussian Process Regression
H3TRB	High Humidity High Temperature Reverse Bias
HB-SM	Half-Bridge Submodule
HCI	Hot Carrier Injection
HS	High-Side Switch
HTGS	High Temperature Gate Bias
HTRB	High Temperature Reverse Bias
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
IEC	International Electrotechnical Commission
IGBT	Insulated-Gate Bipolar Transistor
KBA	Knowledge-Based Agent
KF	Kalman Filter

LCC	Line Commutated Converter
LS	Low-Side Switch
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTDC	Multi Terminal DC grids
MTOE	Millions of Tons of Oil Equivalent
MVDC	Medium Voltage Direct Current
NLM	Nearest Level Modulation
NPC	Neutral-Point Clamped Converter
NTC	Negative Temperature Coefficient
OHL	Overhead Lines
OWF	Offshore Windfarm
P2P	Point-to-Point HVDC link
PC	Power Cycling
PCA	Principal Component Analysis
PCB	Printed Circuit Board
PDF	Probability Density Function
PF	Power Factor
PI	Proportional-Integral (PI) Controller
PLL	Phase-Locked Loop
PoF	Physics-of-Failure
PTC	Positive Temperature Coefficient
PWM	Pulse Width Modulation
RMS	Root Mean Square
RTD	Resistance Temperature Detector
RUL	Remaining Useful Life
SEM	Scanning Electron Microscope
SM	Submodule
SMU	Source Meter Unit
SOA	Safe Operating Area
SOH	State-of-Health
SSBP	Simple State-Based Prognostics
TDDB	Time Dependent Dielectric Breakdown
TDNN	Time-Delay Neural Network
TIM	Thermal Interface Material
TRB	Temperature Reverse Bias
TSEP	Temperature Sensitive Electrical Parameters
TSO	Transmission System Operator
UART	Universal Asynchronous Receiver/Transmitter
VSC	Voltage-Source Converter

General Introduction

Background

The energy demands around the world are growing, in fact they have been growing at an accelerated pace since the industrial revolution in the early 1800s. Moreover, modern societies have evolved under a strongly energy-dependent model where energy consumption is ever-growing [1]. Given this high energy demand, fossil fuels have played a major role since they are easily available, and they have low production costs. An evolution of the primary energy sources can be seen in Figure i.1.

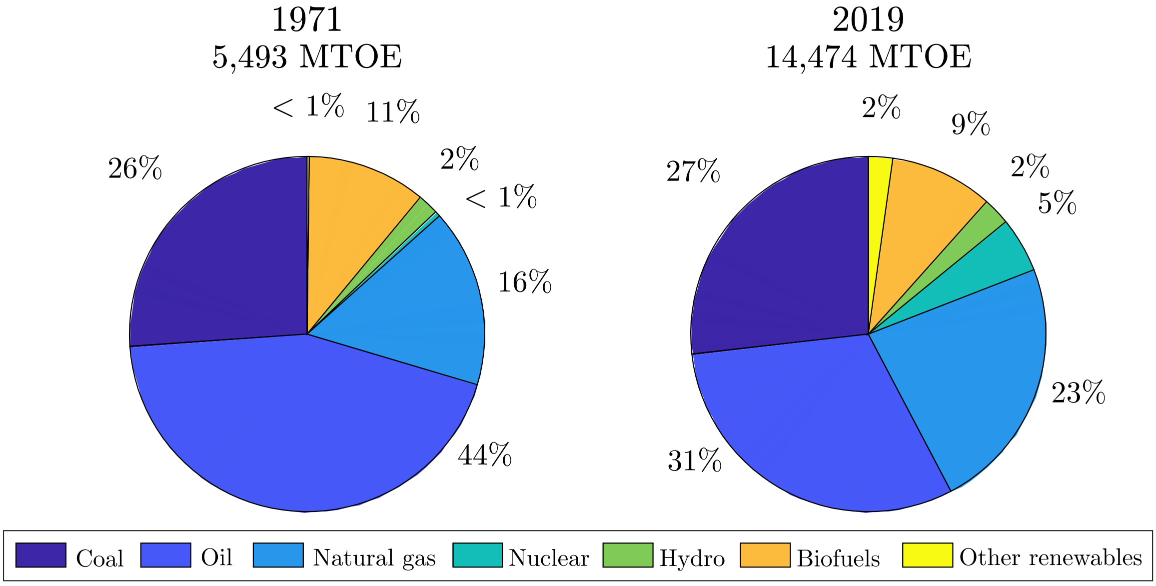


Figure i.1. Global primary energy sources in 1973 and 2019 in Millions of tons of oil equivalent (MTOE) [2]

Even though fossil fuels have allowed for a rapid development of society, they pose nowadays a major problematic related to CO_2 emissions and its contribution to the greenhouse effect. It is in this climatic context, that newer energy sources have seen a major development in the past few decades. First, nuclear energy was seen as a viable solution regarding its climactic impact, however, nuclear fuel waste management proved to be a blocking point, as well as its highly demanding safety requirements. Subsequently, renewable energies have soared as the most viable technologies for emission-free energy production. Therefore, new climatic policies have placed renewable energies at the heart of coming energy projects and initiatives.

Not only has energy production seen the impact of the high energy demands. Power transmission must also deal with this constraint. The growing energy demands on power transmission systems are pushing towards the rapid development of High Voltage Direct Current (HVDC) technologies. As an example of this trend towards HVDC, the European commission, in partnership with the European Network of Transmission System Operators for Electricity (ENTSO-E), has set its first objective of increasing the number of interconnections by 15% until 2030, with, in particular, the integration of tens of thousands of kilometers of HVDC lines [3], [4].

HVDC has been recognized as a major contender for performing long-distance bulk-power transmission, asynchronous AC systems interconnections, interconnection of different regions requiring submarine and/or underground cables, and transmission of offshore wind power to shore [5], [6].

Some of the advantages of HVDC are the lower conduction losses on the DC lines compared to its AC counterparts as there is no skin effect, nor proximity effect on DC. In addition, DC has the advantage of the absence of losses due to reactive current [7].

Despite all the advantages of DC over AC, a major drawback for HVDC systems is the cost of the power conversion stations needed to interface DC links to the existing AC infrastructure. The tradeoff between the cost of AC/DC converter stations and the attractive characteristics of DC transmission are suitable beyond a critical distance, otherwise known as break-even distance [6]–[9]. An illustration of the costs of high voltage AC and DC transmission systems as a function of the distance of the interconnections can be seen in Figure i.2. Depending on the type of transmission line the break-even distance can be different. In the case of overhead lines (OHL) this distance is estimated at around 500-800 km, while cable transmission systems become economically more attractive at distances longer than 60-80 km [8], [9].

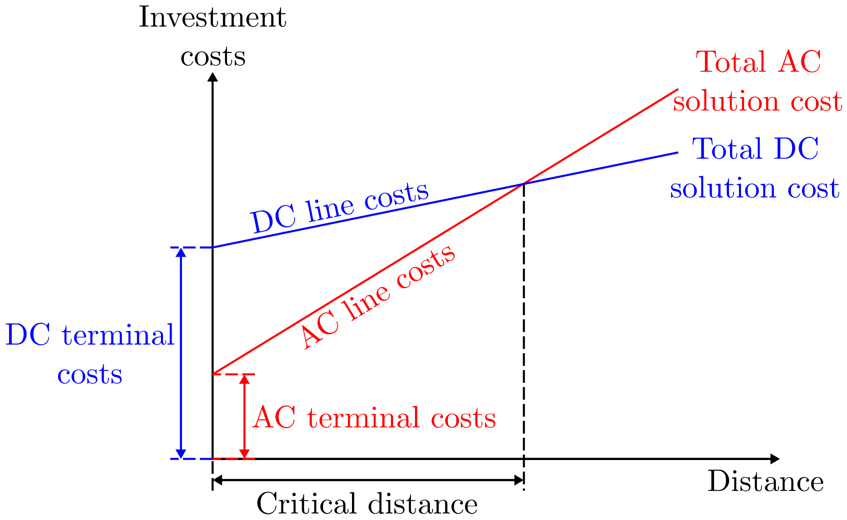
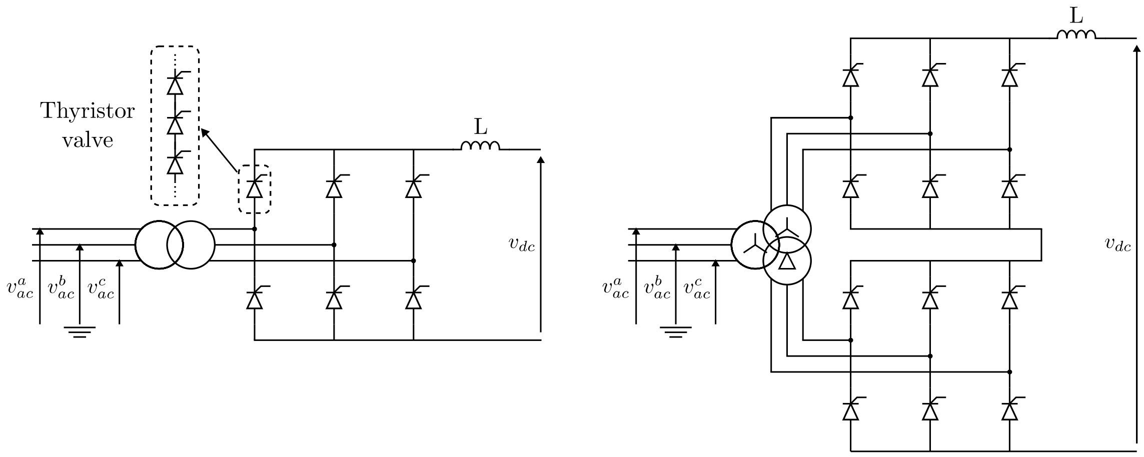


Figure i.2. HVAC and HVDC transmission comparison

In this research work, the subject of the study will be the AC/DC converter station at the ends of the DC power transmission line. There are several examples of efforts for developing DC conversion stages in the first part of the 1900s [10], [11]. However, the main technological milestone that has allowed the development of AC/DC conversion is the emergence of Silicon-based power semiconductors [7]. The first example of AC/DC power converters for high voltage is the Line Commutated Converter (LCC). It is categorized as a current-source converter (CSC), as it behaves as a current source on the AC side. This converter topology reposes on the use of thyristors, as illustrated in Figure i.3.



(a) (b)

Figure i.3. (a) Simplified schematic of a Line Commutated Converter, (b) Twelve-pulse converter

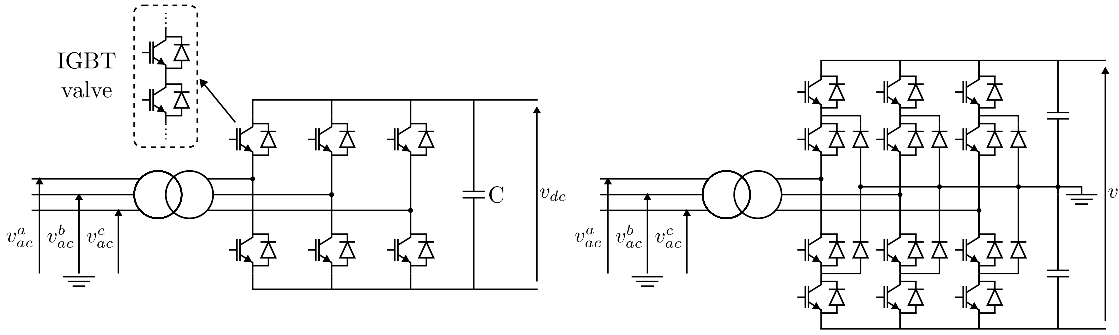
The thyristors used in LCC have ratings of 8.5kV - 5kA [7]. Therefore, it is necessary to connect the semiconductors in series, in order to withstand the high voltages corresponding to HVDC applications. The series association of semiconductor devices is known as a valve.

Thyristors can be switched on; however, they need the current to pass through zero in order to switch off. This characteristic impacts the performance of the converter as the converter relies on the AC side network for the turn-off of the semiconductors and cannot be used as the only power source. This also implies that the active power P and the reactive power Q cannot be controlled independently in this topology. Hence, the converter requires the use of large filters for reactive energy compensation. Filters are not only used for this purpose, but also for reducing the current swing on the AC side and suppress the important harmonic content. In order to address the latter issue, the twelve-pulse topology seen in Figure i.3 can be used. Moreover, with this technology the DC current cannot change direction, as it flows through a large inductance as depicted in Figure i.3. Thus, power reversals are achieved by changing the polarity of the DC voltage.

In order to address the issues of current-source converters, the voltage-source converter (VSC) technology has gained in relevance since the late 1990s [12]. VSC technologies rely on the use of semiconductors such as the Insulated-Gate Bipolar Transistor (IGBT), that can be controlled at both turn-on and turn-off. This allows for an additional degree of freedom, which enables the independent control of the active and reactive power. This characteristic also allows converters to no longer rely on the AC grid for its operation and gives them “black-start” capabilities [9]. Since the turn-off of the devices can be controlled in VSCs, they can switch much faster than CSCs and improve the harmonic performance, which can result in the elimination of filters [13].

In contrast to CSC, VSC allows for power reversals by maintaining the voltage polarity and changing the direction of the current. This makes VSCs much easier to connect into a Multi-terminal HVDC system of DC-Grid [14].

There are several VSC topologies. The first VSC topology introduced for HVDC applications is the 2-level converter, which can be seen in Figure i.4 (a). Current IGBT technology for HVDC has ratings of 3.3kV to 6.5kV and 1kA to 2 kA [15]. It is therefore necessary to assemble these components in series to withstand the voltage levels of HVDC applications. Similar to thyristors in LCC, IGBTs are assembled in "IGBT valves" that make up a single switching element. A major drawback of this structure is that components inside an IGBT valve need to be perfectly synchronized during the switching actions. Otherwise, some of the individual IGBTs will experience overvoltages that can lead to the destruction of the power module and can lead to catastrophic scenarios. In order to attain a better voltage distribution among the components inside a valve, snubber circuits are employed. These elements lead to higher power losses during normal operation and will impact the volume and the weight of the converter station, which can be of particular interest for some applications.



(a) (b)

Figure i.4. VSC topologies: (a) 2-level converter, (b) 3-level converter, NPC topology

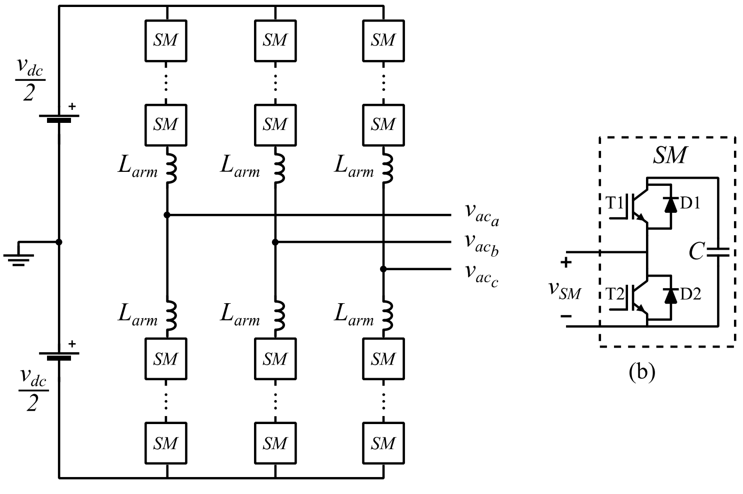
In order to deal with the issues concerning the series assembly of components and the nonnegligible switching losses for reducing the AC harmonic content, different VSC topologies have emerged. Among some of them the Floating Capacitor Converter (FC), or the Cascaded H-Bridges Converter (CHB) can be mentioned [16]–[18]. However, one of the most widely used in HVDC applications is the Neutral-Point Clamped Converter (NPC) seen in Figure i.4 (b). It is a 3-level converter, which can generate output levels of $+v_{dc}/2$, 0 and $-v_{dc}/2$. The IGBT valves in this topology withstand only half the voltage when compared with the 2-level topology. The zero-voltage level output can be obtained with the use of the clamping diodes present in this topology.

This structure allows a decrease in losses and reduced harmonic content to the detriment of higher system complexity and control strategy. There are other issues concerning the NPC. For instance, the number of diodes present in this topology is quite important. Also, the voltages across the capacitors need to be balanced, hence they may require the use of additional circuits. Given these characteristics, this topology in practical HVDC applications is limited to three levels, contrary to the theoretical multilevel capabilities inherent to the NPC building block.

The series assembly of elements for obtaining switching "valves" and the higher switching frequencies are the principal downsides of the VSC topologies mentioned previously. A multilevel architecture can help overcome the limitations of the classical VSC circuits. Thus, the Modular Multilevel Converter (MMC) topology arose as a viable alternative for HVDC applications. This topology will thus be the subject of this thesis and will be discussed in more detail in the following paragraph.

Modular Multilevel Converter

A major technological advance for VSC technologies is the Modular Multilevel Converter (MMC) seen on Figure i.5. It was first introduced in 2003 by German professor R. Marquardt [19], [20]. This topology is considered the most promising for HVDC transmission applications, as it has the main advantages of other VSC structures but without the drawbacks. Additionally, the MMC is scalable, its modular structure allows an improved output quality and the topology is more efficient as it has reduced switching losses [21].



(b)

(a)

Figure i.5. (a) Three-phase Modular Multilevel Converter, (b) Half-bridge submodule

The MMC topology shown in Figure i.5 (a) has three phases, otherwise known as a converter leg. Each leg is composed of an upper and lower arm, which are composed themselves of an arm inductor L_{arm} and a stack of submodules. The submodules are connected in series for generating the output voltage levels of the HVDC system. Multiple submodule configurations are proposed in the literature [22], but the two most popular are the half-bridge (HB-SM) and full-bridge (FB-SM) configurations. In practical applications today, the HB-SM is the most used due to cost considerations.

A HB-SM topology can be seen in Figure i.5 (b). It consists of a storage capacitor and two IGBT modules. Each IGBT module has an IGBT device and its antiparallel diode, in order to perform three-quadrant operation. The IGBT modules allow the insertion or the bypass of the storage capacitor. The output voltage of an MMC arm can be controlled by inserting/bypassing submodules in order to obtain the desired waveforms. An illustration of the output voltage of an arm and of a converter leg can be seen in Figure i.6.

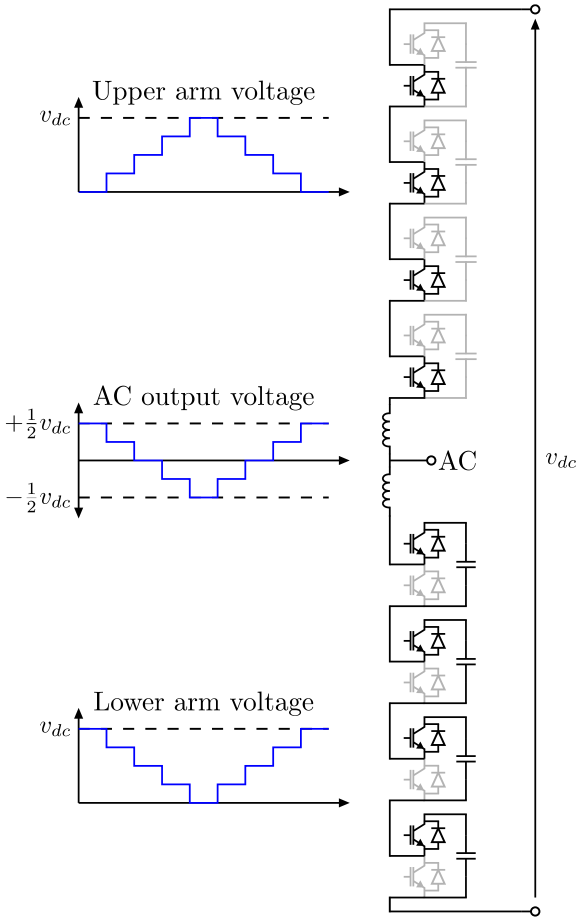


Figure i.6. Working principle of a single phase of an MMC

Problem statement and thesis scope

According to the ENTSO-E, TSOs and other end-users of HVDC should consider that improved reliability (e.g. decreasing 1-2 trips per year on average) and improved availability (e.g. decreasing 1-2 outages days per year on average) can bring significant cost savings to TSOs and/or society [23].

The scope of this work is limited to the power converter, in this case the Modular Multilevel Converter. It was seen that the MMC topology consists mainly of the submodules HB-SMs, which are basically composed of IGBT modules and storage capacitors. According to a survey on the reliability of power converters [24], both these elements are considered critical and among the weakest links that define the reliability of the circuits in which they are present.

This work will focus more particularly on the IGBT devices, as studying both elements deem to be a rather long and difficult task. Moreover, IGBT devices according to [24], are the weakest components in the power conversion chain and several works have been reported for addressing the state-of-health (SOH) of the storage capacitor in the MMC application [25]–[27]. Therefore, this work intends to understand the main failure modes and mechanisms of the IGBT device in an HVDC-MMC application and to select an appropriate strategy for assessing its state-of-health and determine its remaining useful life (RUL) while in online operation.

There are several strategies for enhancing the reliability and availability of power converters. Among them, Condition Monitoring (CM) has gained in relevance in the last few decades [28] and will be the chosen strategy for the rest of this thesis. The CM approach consists of tracking the evolution of a particular parameter indicative of the state of degradation of an element, in order to assess its degradation. From this method, additional efforts can be made in order to prognose the expected end-of-life (EOL) of the studied element and determine its RUL.

A particular point of interest in this study is the thermal loading of the IGBT components. This is a crucial subject for deploying a prognosis methodology as it will be seen in the body of this work.

Thesis outline

The organization of this thesis is as follows:

- Chapter 1 deals with the IGBT modules used in an HVDC-MMC application, subsequently it covers the main failure modes and mechanisms they can experience. Finally, a comprehensive review on the techniques for the condition monitoring and the prognosis of the remaining useful life of these devices is presented.
- Chapter 2 describes the modelling of a MMC. This model will be employed for obtaining the electrical waveforms and the loading conditions of the IGBT devices to be studied in this application.
- Chapter 3 presents a methodology for the estimation of the lifetime of the semiconductors present in a HB-SM. This methodology considers the mission profile experienced by the semiconductors and translates it to a thermal profile. The computed thermal profile is used for the calculation of the lifetime consumption experienced in the evaluated period. Additionally, this chapter presents a methodology for evaluating the reliability of a MMC arm and consequently computing the redundancy requirements for attaining a target converter availability.
- Chapter 4 presents a power cycling testbench developed for studying the degradation process of the IGBT devices. The online surveillance of the collector-emitter voltage is also addressed in this chapter. Additionally, the estimation of the junction temperature of the IGBTs is covered. Finally, the results of the power cycling tests are presented in this chapter.

Main contributions

The main contributions of this thesis to the scientific community are:

- A thorough overview of the typical failure modes and mechanisms of IGBT modules suited for a HVDC-MMC application.

- A review of the state-of-the-art on the prognosis and condition monitoring of IGBT modules.
- A hybrid averaged-detailed model of the MMC for obtaining the electrical waveforms of the elements of a HB-SM.
- A methodology for the estimation of the lifetime consumption of semiconductor devices considering the mission profile of the converter. This topic was the subject of a conference paper [29].
- A novel model-based interpolation/extrapolation method, for the calculation of the lifetime consumption based on thermal profiles.
- Reliability predictions of the semiconductors inside a HB-SM. These predictions consider the mission profile experienced by the semiconductors and the manufacturer lifetime models.
- A methodology for computing the number of required SMs based on the reliability of its composing elements. This methodology considers the target availability of the HVDC application as well as the mission profile of the semiconductors. Correspondingly, this work was the subject of a conference paper [30].
- An AC Power Cycling testbench was developed in this thesis, along with all the instrumentation required for performing a condition monitoring scheme for IGBT devices.
- An upgraded circuit for the online measurement of $V_{CE(on)}$ was proposed. Moreover, this circuit is not only suitable for IGBT devices, but also for faster semiconductor devices.
- A methodology for the estimation of the junction temperature of IGBT devices based on the online measurement of $V_{CE(on)}$ and a Kalman filter.

List of publications

- D. Velazco, G. Clerc, E. Boutleux, F. Wallart, and L. Chédot, “IGBT Lifetime Estimation in a Modular Multilevel Converter for bidirectional point-to-point HVDC application,” in *2020 22nd European Conference on Power Electronics and Applications (EPE’20 ECCE Europe)*, Sep. 2020, pp. 1–10. doi: 10.23919/EPE20ECCEEurope43536.2020.9215880.
- D. Velazco, G. Clerc, E. Boutleux, and F. Wallart, “Comparison of Redundancy Requirements for Modular Multilevel Converter Considering Manufacturer Reliability Inputs and Mission Profile,” in *2022 24th European Conference on Power Electronics and Applications (EPE’22 ECCE Europe)*, Sep. 2022, pp. 1–10

1. State of the art on CM and prognosis techniques for IGBT modules

1.1. Introduction

From the general introduction it was seen that the IGBT is one of the main elements of the Modular Multilevel Converter. Additionally, in the survey reported in [24], it was mentioned that the most fragile component in power converters is the semiconductor. Hence, this thesis will focus on the reliability of the IGBT in the context of the MMC application. This work will intend to set a basis for a prognosis of the lifetime of these devices, as well as performing other relevant reliability-related computations.

This chapter starts with a background description on the IGBT module. More detail on the different types of modules employed in VSC-HVDC applications will be discussed.

Additionally, the failure mechanisms of the IGBT devices will be presented. The main stressors, failure modes and the parameters that can help the monitoring of the different failure types will be introduced.

Subsequently, a thorough state of the art on the approaches for the prognosis of the state of health of these elements will be made. The prognosis approaches will be discussed and the main advantages and disadvantages of each of them will be mentioned.

In the last section of this chapter some of the more relevant works on the Condition Monitoring of the IGBT devices will be presented. A critical summary on the applied methods will be made at the end of this paragraph.

1.2. Background on IGBT modules

Insulated Gate Bipolar Transistors (IGBTs) are a mature technology of semiconductors that has been under continuous improvement [31] since its introduction in the early 1980s [32], [33]. This type of semiconductor has a wide variety of applications such as wind energy generation, hybrid vehicles, high speed rails, energy transmission and distribution.

This family of semiconductor can address broad voltage ranges from 300 V to 6.5 kV and current handling capabilities larger than power MOSFETs [34]–[36]. These characteristics make IGBTs a suitable technology for HVDC applications such as the MMC [19], [20]. In HVDC-MMC it is reported that 84% of converter failures are due to valve device failures [37]. As the IGBT module is one of the main elements of the valves, it is important to perform reliability evaluations of this type of device.

In the case of HVDC applications, there is an interest in using the highest voltage-rated devices in order to decrease the number of stages required for achieving AC-DC conversion at high voltages. Semiconductor manufacturers have developed specific IGBT packaging technologies addressed to this type of usage. The relevant packaging technologies for high-power transmission are press-pack and wire-bonded (flat-pack) modules, which will be discussed later in this chapter.

Regardless of the packaging technology used by the modules, the semiconductors inside them are composed by elementary semiconductor cells, which are arranged in such a way that they constitute a semiconductor chip [38]. A cell corresponding to a typical IGBT design can be seen in Figure 1.1.

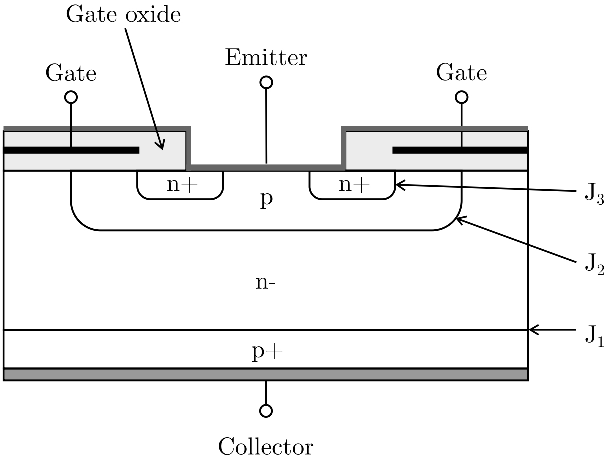


Figure 1.1. Layered schematic of an IGBT cell [39]

In Figure 1.1, the three electrical terminals of the cell (collector, emitter, gate) and the different junctions inside the device can be seen. Depending on the voltage applied between the gate and the emitter the pn junctions J_1, J_2 and J_3 will either be conducting or in a blocked state, which will eventually turn the IGBT on (positive gate-emitter voltage) or off (0V or negative gate-emitter voltage). The gate connections are encapsulated in electrically insulated gate oxide.

The IGBT structure is placed on a silicon chip, but in order to be able to connect the chip to the circuit it is necessary to use an external packaging. Thus, the power component is composed of one or more semiconductor chips in a package. The package and its connection technology are just as important as the characteristics of the semiconductor regarding the reliability of the whole component [40].

A power module has an internal circuit topology, composed of several power semiconductor components and packaging interconnections [41]. In order to increase the power rating of the module, it is necessary to provide a similar loss repartition on each of its internal components. In IGBT power modules, it is a common practice to install IGBT chips as well as diode chips, for free-wheeling purposes and for allowing three quadrant operation.

High-power IGBTs generally have low on-state voltages, which reduce the conduction losses. The total losses experienced by high-power devices can reach several kilowatts. Hence, the package must be conceived in such a manner that the heat generated by the losses can be dissipated away from the chips, for ensuring that the thermal limits of the silicon chips are not met. The packaging must therefore have a high reliability and a high durability under alternating load conditions [42]. Moreover, the package must provide high electrical conductivity for avoiding undesirable electrical properties like parasitic resistance, parasitic capacitance and parasitic inductance [42].

The main packaging technologies for high-power applications such as the HVDC-MMC will be described in the following lines.

1.2.1. Press-pack modules

Press-pack technology has proved to be a robust and reliable packaging method for devices like thyristors and diodes in high-power applications [43]. It is a solderless packaging structure, which achieves thermal and electrical contacts by pressuring components from one device to another. Recently, this technology has been adapted for high-power rated IGBT devices. In Figure 1.2 some examples of press-pack modules can be seen as well as the internal structure of a monolithic press-pack device.

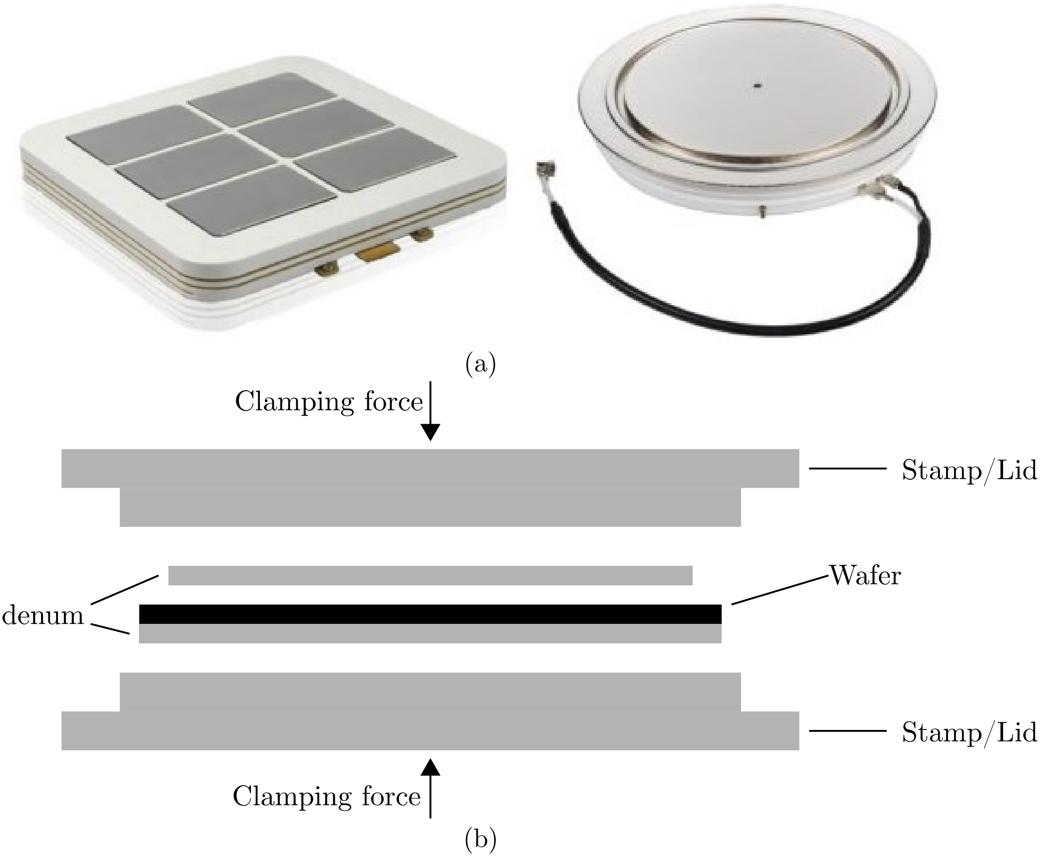
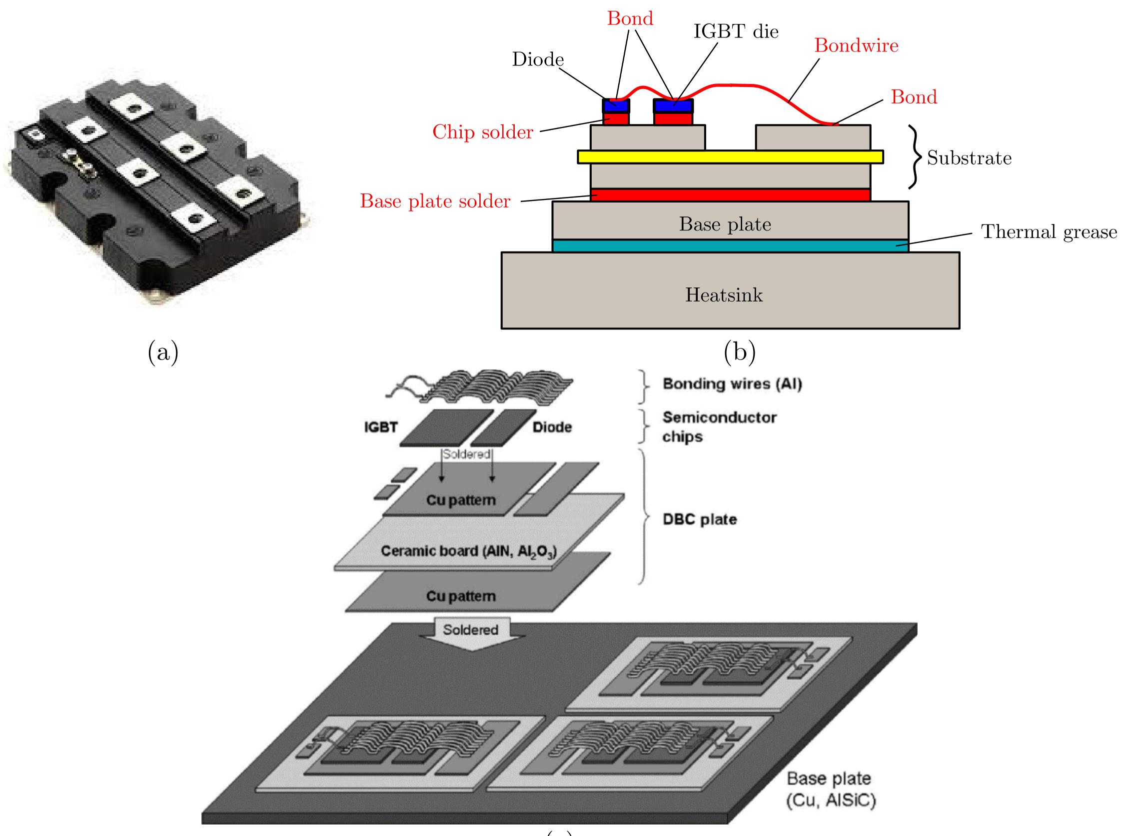


Figure 1.2. IGBT press-pack modules (a) Example modules [44], [45], (b) Internal structure [43]

From Figure 1.2 (b) it can be seen that, this packaging technology has a molybdenum plate and a metal lid on either side of the Si wafer. These elements provide the electrical and thermal contact between stacks of similar devices. Additionally, the packages are hermetically sealed. Molybdenum is used as it has a similar CTE to that of silicone, also its hardness properties make this metal a desired choice for its placement between the metal lids and the chips.

1.2.2. Wire-bonded (Flat-Pack) modules

The most widely used packaging technology corresponds to the wire-bonded modules. A high-power wire-bonded module, as well as its internal structure can be seen in Figure 1.3 [40], [42], [46].



(a) (b)

(c)

Figure 1.3. IGBT wire-bonded modules (a) Example module [40], (b) Internal structure [40], [42], [46], (c) Exploded view of IGBT module structure [47]

In this type of packaging technology bonding pads are used for connecting the different gate and emitter electrical terminals to the semiconductor dies. Metallization layers are employed for performing electrical connections to the bonding pads. The metallization layers on the chips are made from aluminum alloys for aluminum wire-bonding the die with the power terminals of the device. In most emitter metallization designs, the bonding pads are disposed in a matrix array for preventing the formation of hotspots as seen on Figure 1.4 [48].

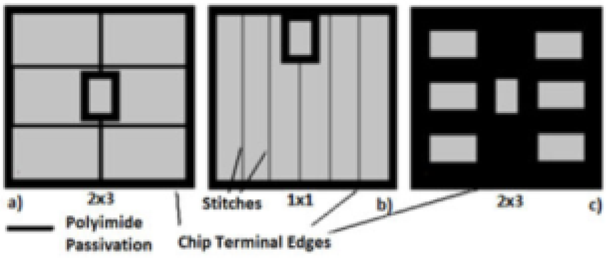


Figure 1.4. Common emitter metallization layouts [48]

The collector and its metallization layers are located on the other side of the chips. The collector metallization has 3 roles: First, it works as an electrical connection between the collector and the package. Second, it acts as a thermal interface between the chip and the package [40]. Third, it functions as an adhesion layer between the die and the solder layer used for attaching the die to the package. In some cases, extra metallization layers are added to the backside metallization to protect the semiconductor from contamination [40].

The wire-bonded modules have a direct bonded copper layer (DBC) as shown in Figure 1.3 (b) and Figure 1.3 (c). The metallization layers on top of the IGBT/free-wheeling diodes (FWD) dies are connected to the top copper layer of the DBC through aluminum bond wires. This top copper layer is used as a power track to connect devices to each other and to module terminals [49].

The metallization layers on the bottom side of the chips are soldered to the top copper layer of DBC. These solder layers are also known as die attaches or chip attaches and can also be seen in red below the semiconductor chips on Figure 1.3 (b). They also serve three functions: First, they conduct current from the dies to the top layer of the DBC. Second, they transfer heat from chips to DBC. Third, they fix the dies to the DBC [49].

The DBC consists of two copper layers sandwiching a ceramic layer that provides electrical isolation between the chips and the baseplate. The DBC is generally soldered to a copper baseplate. The solder layer between the DBC and the baseplate is called DBC attach, and it performs two functions: First, it transfers heat from the DBC to the baseplate that is mounted on a heatsink. Second, it fixes the DBC to the baseplate that is mounted on the heatsink [40], [46], [48], [50].

1.2.3. Comparison between module packaging technologies

Both packaging technologies, are currently being used in HVDC applications. In Table 1.1 [51] a comparison between both technologies can be seen. From Table 1.1, it can be seen that press-pack technology is more reliable from a power/thermal cycling perspective [52]. Thus, this technology is being pushed for high-power applications. However, wire-bonded technology is still more widely used than press-packed technology in most applications and several MMC manufacturers still use wire-bonded devices for this sort of purpose. Thus, for the rest of this study, the focus will be made on wire-bonded devices as this is the weakest technology for high-power IGBT modules.

1.3. Failure mechanisms of power modules

As mentioned previously, the packaging technology for this research work corresponds to wire-bonded modules. This type of technology is more susceptible to failures than the more recent press-pack technology. But the former is still being widely employed and there are still many reliability-related aspects to address for wire-bonded technologies.

Failures in wire-bonded modules can be categorized according to different criteria. In [53] the different failure mechanisms were categorized by the nature of the fault. Hence, failure mechanisms can be classified as intrinsic and extrinsic [54], [55]. Intrinsic failure mechanisms are due to natural degradation of materials and show wear-out behavior. Extrinsic failure mechanisms are due to unintended defects of product deviations. They are random in nature and show early-life failures and random failures [41].

Feature	Wire-bonded modules	Press-pack modules
Thermal and power cycling reliability	Mismatch in CTE can lead to fatigue failure	The possibility of fatigue failure is reduced since wire bond and solder interconnect are substituted with bondless pressure contact [52]
Single die failure susceptibility	The state (open- or short-circuit) after a single die failure is not defined. It can lead to catastrophic failure of the whole module	With a redundant design, the module can continuously operate with a single die failure. A failed die can be replaced during planned system services
Explosion safety	An explosion was observed when short-circuit conditions were met [56], [57]	The plasma formed by a short-circuit can be confined inside the module through proper designing
Cooling system	Simple: a heatsink with cooling fans or liquid cold plates can be used	Complicated: deionized water is used
Heat dissipation	Large temperature differences between individual chips can occur due to inherent variability in thermal resistance of their solder interconnects and substrates	Uneven heat dissipation is reduced by sharing common heatsink blocks: the temperature difference between the hottest and coldest dies were 6°C during the heating phase of a power cycle [58]
Current distribution	Current flow in individual dies can be uneven due to their temperature differences	Current flow in individual dies is “quite homogeneous” between individual dies [58]
Die mounting	Conventional (inexpensive)	Unique (expensive)
Electrical insulation	A ceramic layer itself in the DBC substrate provides the internal insulation	A die carrier subassembly requires housing for the insulation
Transient voltage at high switching frequency	Transient voltage of individual dies varies unless their electrical circuits are perfectly identical	Differences in transient voltage of individual dies are reduced since a common inductive path is shared

Table 1.1 Comparison between press-pack and wire-bond packaging technologies [59]–[62]

Also, failure mechanisms in IGBT modules can be classified by the location at which the failure is originated [49], [63]. According to this criterion, they can be categorized in chip-related failures and package-related failures. A comprehensive diagram depicting the origin of the failure mechanisms in IGBT modules can be seen in Figure 1.5 [41], [63]. Additionally, Table 1.2 [49] shows more details on the different failure modes and gives an insight on the effect of the failures on the system.

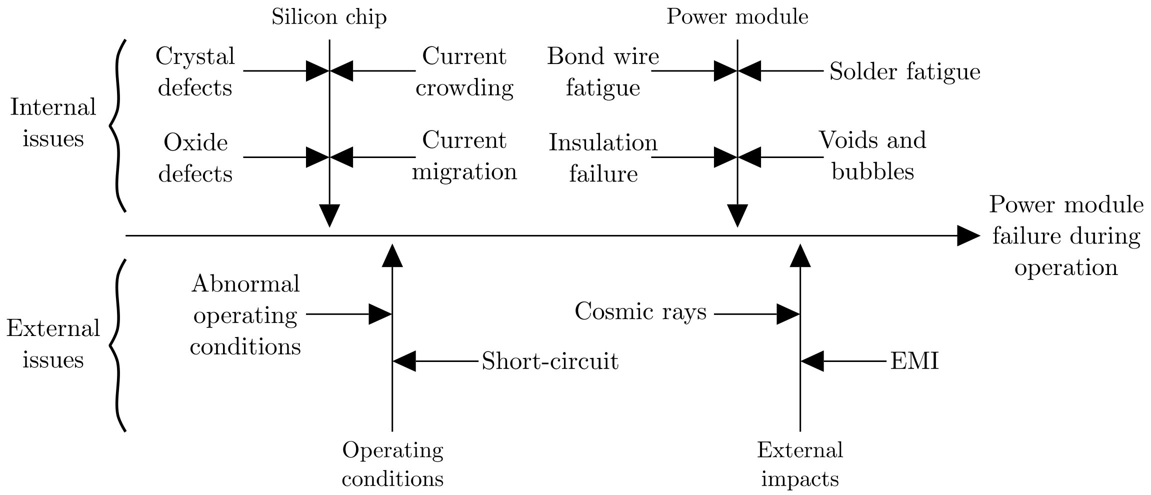


Figure 1.5. Potential failure types in power modules [41], [63]

Mode	Type	Failure	Effect
Chip-related	Overstress [40], [42], [55], [64], [65]	Gate overvoltage (voltage breakdown)	-Open-circuit faults -Short-circuit faults (most of the cases)
		Overvoltage (voltage breakdown)	
		Overcurrent	
		Cosmic rays burn out	
	Wear-out [40], [66]–[71]	Time dependent dielectric breakdown (TDDB)	-Mal-operation of gate drivers & switches -Loss of chip's voltage blocking capability
		Hot Carrier Injection (HCI)	
		Electrochemical migration	
Package-related	Overstress [40], [72]	Mechanical shock and stresses	-Open or short-circuit faults -Accelerate wear-out -Melting and burnouts (more common in harsh environments)
		Thermal shock	
		Thermal runaway & flashovers	
	Wear-out [40], [67]–[72]	Thermomechanical fatigue	-Thermal losses (most of the cases) -Stray (leakage) current issues -Loss of module's voltage blocking capability
		Thermomechanical creep	
		Electro & electro-chemical migration	
		Insulation degradation	

Table 1.2 Failure mode classification in power modules [49]

A brief description of the main failure mechanisms of IGBT modules will be made in the following paragraph. The failure mechanisms will be categorized by the location at which they take place.

1.3.1. Chip-related failure mechanisms

1.3.1.1. Overstress failure mechanisms

The main overstress failure mechanisms are due to electrical overstress (EOS), and burnout [42], [72].

In the case of electrical overstress, overvoltages can lead to secondary breakdown under high-voltage and excessive heating [65], [73]–[76]. In order to prevent this issue, it is necessary to ensure that the safe operating area (SOA) for the device is suited to the application and that proper cooling of the semiconductor is achieved [77].

As for burnout failures, they are observed either at the final phase of wear out or because of random events. These failures are associated with short-circuit conditions, where a large current flows through the device while blocking the full line voltage [72]. These conditions lead to the thermal runaway and the destruction of the device.

Latch-up is a failure mechanism inherent to IGBT devices. It happens when a big dv/dt is produced during the turn-off and can trigger the parasitic thyristor in the IGBT structure [72], [77]. The latch-up is a burnout failure as the triggering of the parasitic component leads to the thermal destruction of the device. Another catastrophic burnout of an IGBT chip can be originated from cosmic ray collision on the device [78].

Although in some cases the overstress failures of chips show up as an open-circuit, in most of the cases they manifest as short-circuit of the device [40], [65], [75], [76].

1.3.1.2. Wear-out failure mechanisms

The most common wear-out failures for IGBT dies are Time Dependent Dielectric Breakdown (TDDB) and Hot Carrier Injection (HCI) [66], [72].

The dielectric breakdown is caused by gate degradation due to accumulated defects [79]. In [80], three defect generation mechanisms are identified: impact ionization, anode hole injection and trap creation. Catastrophic breakdown occurs when the device experiences severe electrical or thermal stress.

Regarding HCI, two mechanisms are distinguished. The first is the electric field distortion due to accumulation of ionic contaminants in the passivation of the high-field region. The second is the growth of defects in the gate oxide [81]. During high temperature operation, hot carriers can be injected into the gate oxide when carriers attain high energy. These mechanisms lead to shifts in the device characteristics, such as threshold voltage, leakage current, transconductance, or saturation, and eventually to device degradation [73], [82], [83].

Finally, another relevant wear-out failure mechanism is electrochemical migration. In presence of the appropriate conditions (high humidity, high temperature and high voltage), electrical migration at chip passivation layer and terminal structure lead to an increase in leakage currents and loss of blocking capabilities [67]–[71], [84].

1.3.2. Package-related failure mechanisms

1.3.2.1. Overstress failure mechanisms

The main causes for overstress failures at package level are thermal shocks, thermal runaways, mechanical shocks and stresses [49]. The result of a mechanical shock can damage the internal structure of the IGBT module and compromise its voltage blocking capability. This in turn, will lead to voltage breakdown [85].

Thermal runaway happens under high temperature and it leads to the melting of the connections inside the package [40], [72]. Another possible cause for package-related overstress are flashover-generated burnouts [40], [49].

1.3.2.2. Wear-out failure mechanisms

For package-related failures, the principal failure mechanisms are thermomechanical fatigue, thermomechanical creep, electromigration and corrosion [72], [86].

Electromigration is originated in bond wires and metallization layers in the presence of high currents. This phenomenon leads to the creation of voids and hot spots [49], [72].

As for corrosion, it is reported that humidity and corrosive chemicals existing in various industrial applications can be a very important source of packaging degradation [67], [72], [87]. Additionally, humidity degrades the insulation characteristics of module encapsulation materials such as Si-gel [49], [67].

Concerning thermomechanical creep, it is caused by high operating temperatures that lead to the weakening of the mechanical strength of the package layers, which eventually can result in the formation of cracks [72], [88].

Among all the package-related failure mechanisms the more relevant are those related to thermomechanical fatigue [49]. The cause behind these mechanisms is the mismatch of the coefficients of thermal expansion (CTE) of the different layers of the IGBT module [72]. Additionally, temperature gradients are produced in the thermal path because of the difference in the thermal characteristics of the different module layers [89]. In Table 1.3 the typical thermal properties of a wire-bonded package can be seen.

IGBT module manufacturers have made efforts for reducing the stress induced by thermomechanical cycling. They have produced modules with materials that reduce the stress in the adjacent layers such as Al_2O_3 for the ceramic layer and copper baseplates [90]. Other notable improvements in packaging thermal performances were reported in [91]–[98].

The main failure mechanisms resulting from the thermomechanical fatigue are bond-wire degradation, solder layer degradation and degradation of metallization layers. These mechanisms, being the more relevant, will be discussed separately and in more detail.

Layer	Material	Conductivity (W/m/K)	Capacity (J/kg/K)	CTE (10^{-6}/K)
Bond wire	Al-alloy	220	896	23
Metallization				
Chip/Die	Si	100	741	3
Die attach	Solder SnAg (96.5/3.5)	28	-	57
DBC attach				
DBC layer 1	Cu	380	381	17
DBC layer 2				
Baseplate				
DBC ceramic	Al_2O_3	25	850-1k	8
	AlN	180	700-760	5

Table 1.3 Thermal properties of standard IGBT wire-bonded package [40]

1.3.2.2.1. Bond wire degradation

Bond wire failures are mainly caused by crack growth at the bond wire/chip interface due to temperature swings and the different CTEs between Si and Al [99]. Stress is produced at this interface as both layers experience different strains. The resulting stress is dependent on the temperature [73].

Cracks are generally initiated at the boundaries of the bonded area of the wire, since the expansion of the wire is restricted at the edges of the bond pad [100]. Therefore, cracks propagate from the edges towards the center of the bonded area through the pad between the wire and the metallization or through the body of the wire [101] as seen on Figure 1.6. When cracks reach the center of the Al wire, bond wire lift-off is produced and the connection between the wire and the chip is lost. An example of bond wire lift-off can be seen in Figure 1.7 (a). Another site where cracks initiate and propagate is the wire heel, however, this mechanism is less frequent. If the cracks at the wire heel reach the center of the wire heel cracking is produced and the electrical connection is compromised. In Figure 1.7 (b) an example of bond wire heel crack can be seen.

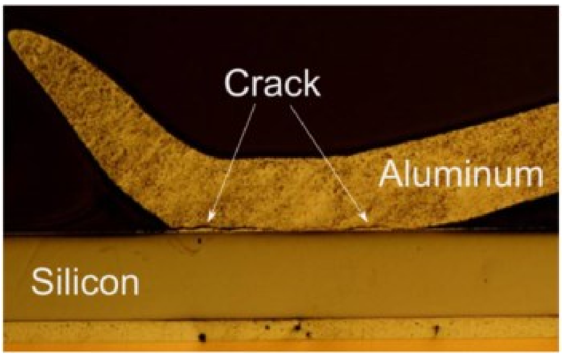
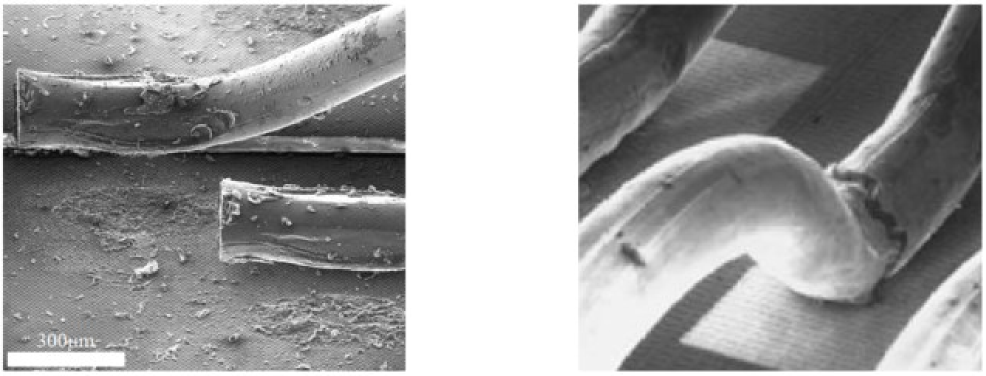


Figure 1.6. Cracking of the bonded pad between the Si chip and the Al bond wire [101]

It is worth mentioning that both failure mechanisms happen when the module is submitted to power cycling. Once a wire has failed, the current is redistributed through the remaining wires. This results in an increase in current and hence in temperature of the remaining bond wires, which accelerates its degradation. The loss of electrical contact between the wire and the chip results in the increase of the on-state resistance of the module, which will lead to higher conduction losses.



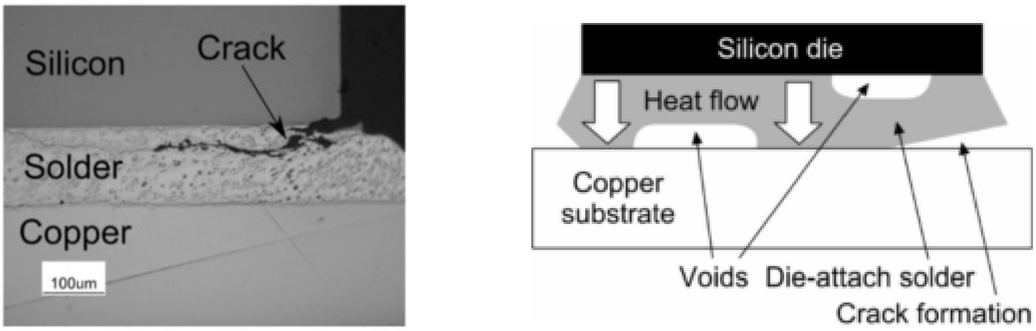
(a) (b)

Figure 1.7. SEM images of bond wire degradation [72], [102]: (a) lift-off, (b) heel cracking

1.3.2.2.2. Solder layer degradation

Similar to wire bond degradation, the solder layer is affected by the CTE mismatch between adjacent layers, between the solder and the silicon for the die attach and between the solder and the copper for the DBC attach. The cyclic thermal loading produces mechanical stresses to the solder layers [103], [104], which are more important at its corners due to restricted elongation [105]. Thus, cracking will initiate at the corners and will propagate towards the center of solder layers as evidenced in Figure 1.8 (a). Additionally, voids present in the solder layer, as result of the manufacturing process, will constitute high mechanical stress locations where cracks can initiate and propagate [101]. It is thus possible that voids expand producing even larger voids inside the solder layers. This phenomenon can be verified in Figure 1.8 (b).

As solder layers constitute an element along the thermal cooling path, any defect on it will have thermal impacts on the module [106]. The contact area between the solder and its adjacent layers will be reduced due to solder degradation, hence obstructing the heat flow from the chip towards the heatsink. This leads to an increase in the thermal resistance, which consequently raises the temperature of the module. Once again, the temperature increase will accelerate all other temperature-dependent failure mechanisms.



(a) (b)

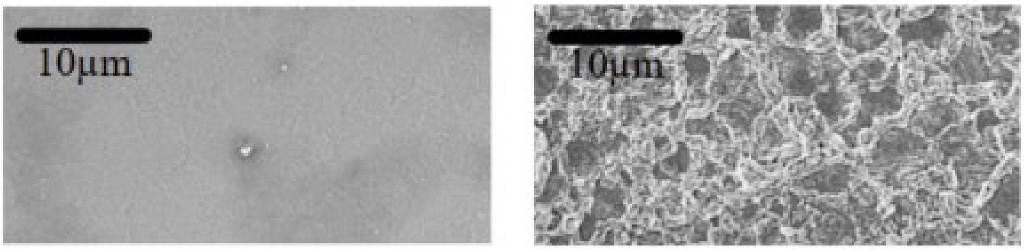
Figure 1.8. Solder layer degradation [73], [101], [107]: (a) Cracking, (b) Void formation

1.3.2.2.3. Metallization layer degradation

As it was mentioned previously in section 1.2.2, metallization layers are necessary for performing the electrical connections on the top side of the chip. These layers are fixed by adding a film of Al through physical vapor deposition combined with thermal annealing, thus creating a polycrystalline structure with grain diameter below 1μm (see Figure 1.9 (a)) [42].

Once again, the CTE mismatch between the Al and the Si from the chips creates high degrees of stress in the interface of both materials due to temperature oscillations. From the CTEs seen in Table 1.3, it is possible to infer that during the heating phases, the metallization layer suffers from compressive stress and vice versa for the chip [102]. From these stresses it was verified that the chips only suffer from elastic strain due to the high yield strength of Si. However, Al relaxation does not occur directly in the interface, even though the stress is highest at this region. Instead, metallization surface effects are observed through grain extrusion or general reconstruction due to plastic deformation of the Al [108] (Figure 1.9 (b)).

In general, reconstruction is more evident at the center of the chip, as junction temperatures are more elevated in this region [72]. In [109] it was demonstrated that surface reconstruction is negligible in the peripheral regions of the chip. Nonetheless, aluminum reconstruction reduces the cross-section of the metallization, and the Al sheet resistance is increased consequently. This effect produces the increase of the on-state voltage, which will lead to the increase of the power losses and of the junction temperature, thus, leading to the acceleration of temperature dependent failure mechanisms.



(a) (b)

Figure 1.9. Metallization layer surfaces [41]: (a) new semiconductor, (b) after reconstruction

1.3.3. Summary on failure mechanisms

The main failure mechanisms experienced by wire-bonded modules were seen in previous lines. They were categorized mainly as chip-related and package-related. It was also seen that failure mechanisms for both chip and package can be classified as overstress and wear-out failures. A complete summary of the IGBT module failure sites, stresses, modes and mechanisms can be seen in Table 1.4 [51].

Failure sites		Stresses	Modes	Mechanisms
Die-level	Die	EOS with/without thermal stress	Short circuit, burnout, loss of gain control	Latch-up and secondary breakdown
		Electrical stress	High leakage current	Hot carrier injection
		EOS	Short circuit, loss of gate control	Gate oxide breakdown
		Electrical stress	Burnout	Dynamic avalanche breakdown
		EOS	Burnout	Electrostatic discharge
		Electromagnetic stress	Burnout, gate rupture	Radiation-induced effect
		Mechanical or thermomechanical overstress	Die crack	Fracture
Package-level	Bond pad	Thermal overstress, electrical stress	Open circuit	Metallization reconstruction
	Bonding wire: bond	Thermomechanical stress	Bond wire lift-off	Fatigue
	Bonding wire: heel	Thermomechanical stress	Bond wire heel cracking	Fatigue
	Bonding wire: body	Thermomechanical stress	Open wire	Electromigration
		Thermal, chemical and mechanical stresses	Open wire	Stress corrosion
		Thermal, chemical, mechanical and/or electrical overstress	Wire burnout	Joule heating
	Solder joint	Thermomechanical stress	Solder joint cracks	Fatigue or grain growth
	Ceramic substrate	Mechanical stress	Shell-like fracture pattern	Brittle fracture
		Thermomechanical stress	Delamination	Delamination of metallization
		Electrical overstress	Electrical short	Partial discharge

Table 1.4 Failure sites, stresses, modes and mechanisms

One important conclusion of the work presented in [73] is that thermomechanical fatigue is the dominant wear-out mechanism in IGBT-based power converters. Failures induced by overstress mechanisms can happen suddenly and have catastrophic consequences. Hence, they cannot be the subject of study for a condition monitoring framework. As it was seen in Table 1.2, thermomechanical fatigue is a type of failure mechanism that affects the package of IGBT modules. Hence, the focus for the rest of this work will be made on package-related degradation of the IGBT modules. Special efforts will be made on determining the state-of-health (SOH) and the estimation of the remaining useful life (RUL) of the power modules by analyzing the thermal loading of the power module.

In order to produce the thermal loading profile for activating the main package-related failure mechanisms and assessing the long-term reliability of IGBT modules, dedicated thermal cycling tests are required. This topic will be covered in thorough detail in chapter 4 of this thesis.

1.4. Notions related to prognosis and Condition Monitoring

Some definitions need to be considered for understanding the concepts related to prognosis and Condition Monitoring (CM) [73].

- Diagnosis: Given that a fault has occurred, diagnosis is to identify the root cause of the fault
- Prognosis: Assess the current health level and predict the health of the component at some point in the future
- Condition Monitoring: Perform real-time measurements of the condition of a component, such that actions can be taken depending on its health status

Having reviewed the previous definitions it is now clear to state that CM is different from prognosis. CM is to assess the current health condition of a component/system, while prognosis is to predict the health condition at some point in the future. CM techniques alone cannot determine the remaining time before the failure of a component/system occurs [51].

According to [51], the application of CM and prognosis techniques for IGBT modules is still limited. This is because many challenges need to be addressed such as:

- Performing measurements of physical quantities related to the health conditions of the devices without interrupting their normal operation
- Correlate health indicators directly or indirectly estimated from physical measurements to the real condition of devices
- Project health indicators to the future with adequate failure criteria, managing uncertainties related to the prediction of the remaining useful life (RUL)

The following lines will give a comprehensive review on the main CM and prognosis techniques for IGBT modules.

1.5. Condition Monitoring for IGBT modules

The technology advancements have allowed for improved reliability of IGBT modules. However, in critical applications such as bulk power transmission, reliability assessment during the manufacturing stage might be insufficient to attain the availability requirements of the application [51]. According to [24], the failure/cost ratio of power conversion systems is very high. These failures can have catastrophic and unrecoverable consequences. Hence, it is necessary to implement strategies for improving the reliability of its more vulnerable elements.

The condition monitoring (CM) approach can be a suitable alternative for assuring the target availability requirements of critical applications. CM was originally developed for systems such as rotating machines and electrical equipment and has been adopted and implemented in power converters deployed on the field to be able to prevent failures [51].

CM provides a continuous monitoring and assessment of the module reliability in its work environment. Therefore, it relies on real-time measurements to detect any deviations from healthy characteristics during normal operating conditions, such that maintenance interventions can be performed [73].

In the case of IGBT power modules, the CM approach will aim to detect changes in parameters that are indicative of die and pack degradation during operation [51]. These parameters are also known as failure precursors or damage sensitive electrical parameters (DSEPs). In Table 1.5 [51], an excellent summary of the IGBT DSEPs associated with the failure modes and mechanisms was presented. It is also worth remarking that a CM parameter can be affected by multiple failure mechanisms. Hence, not a single parameter can be necessary and sufficient to monitor the individual failure mechanisms in IGBT modules.

As it was mentioned previously in section 1.3.3, this work will focus on the package-related degradation related to thermomechanical fatigue. Thus, the following literature review was focused on CM techniques covering the failure mechanisms of interest and its corresponding DSEPs.

1.5.1. Bond wire CM techniques

Bond wires are a major failure site in wire-bonded modules [72], [105]. In [110], a methodology for CM of these elements was presented. The considered approach consisted in observing the evolution of the $V_{CE(on)}$ throughout power cycling (PC) tests. The proposed scheme for performing the measurement of $V_{CE(on)}$ can be seen in Figure 1.10 [110]. The strategy employed in that work consisted in performing the measurements under constant temperature and current conditions.

Failure sites		**Failure modes**	**Failure mechanisms**	**DSEPs**
Die-level	Die	Short circuit, burnout, loss of gate control	Latch-up and secondary breakdown	$V_{CE(on)}$ t_{off} $V_{GE(th)}$
		Short circuit, loss of gate control	Time dependent dielectric breakdown	V_{GE} $V_{GE(th)}$
Package-level	Bonding wire: bond	Bond wire lift off	Fatigue and/or reconstruction	t_{on} t_{off} $V_{CE(on)}$ V_{GE}
	Bonding wire: heel	Bond wire heel cracking	Fatigue	
	Bonding wire: body	Open wire, wire burnout	Stress corrosion Joule heating	
	Solder joint	Solder joint cracks	Fatigue or grain growth	R_{th} $V_{CE(on)}$ t_{off} Low-order harmonics

Table 1.5 Failure sites, modes, mechanisms and DSEPs [51], [110]–[119]

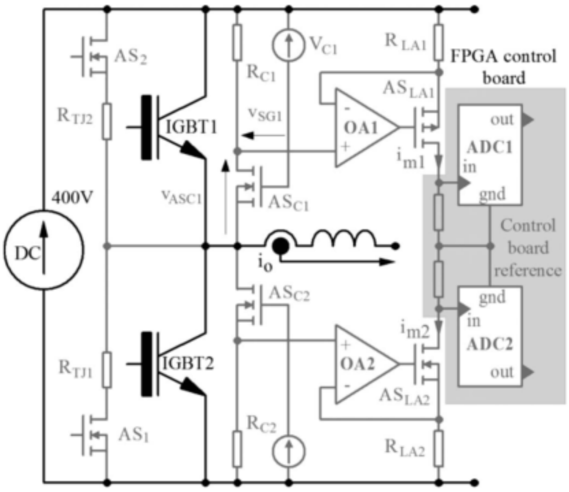


Figure 1.10. $V_{CE(on)}$ measurement scheme [110]

One of the main drawbacks of this work is that in the presence of noise, the estimations of the degradation can be uncertain. Uncertainties larger than 1% can lead to significant error in characterizing the health condition of a degraded module, if the failure criterion is as small as 5% [51].

In light of these issues, [120] proposed an improved method for the measurement of $V_{CE(on)}$. It consists in the use of an advanced CM algorithm along with a multiplexer circuit. With this new scheme uncertainties of less than 0.1% were reported. It is worth noting that a relay network was necessary to perform the measurements during the periods where the converter is at rest as seen on Figure 1.11. The $V_{CE(on)}$ measurements are compared with a healthy value of this parameter at a fixed current and temperature. Any difference between the measured value and the corresponding healthy value indicates a degradation of bond wires.

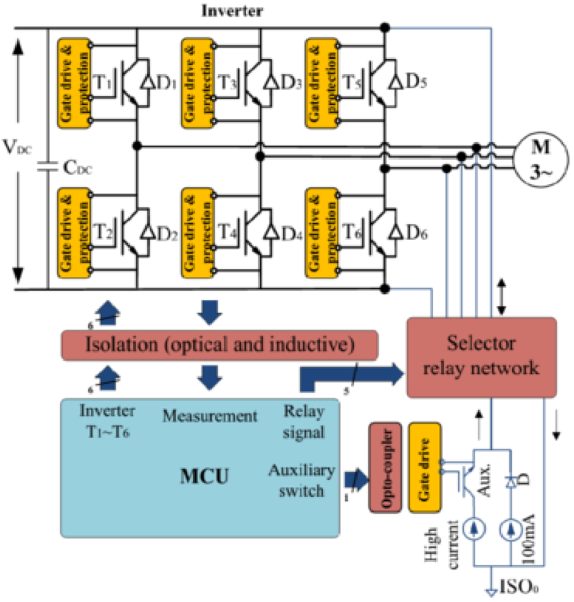


Figure 1.11. Health-monitoring system for power converter [120]

In [101] the measurement of $V_{CE(on)}$ was also employed for the estimation of the degradation of bond wires. The circuit employed in that work can be seen in Figure 1.12.

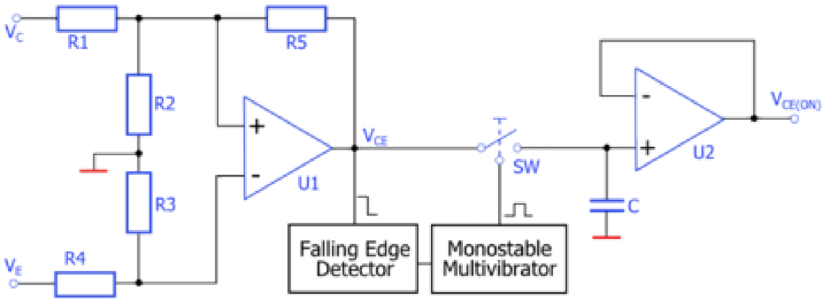
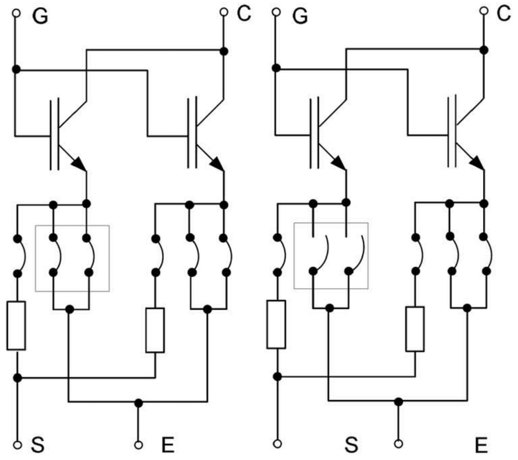


Figure 1.12. A simplified schematic of the $V_{CE(on)}$ measurement circuit [101]

Since $V_{CE(on)}$ depend on the temperature and the health conditions of IGBT modules, it is necessary to decouple them when performing $V_{CE(on)}$ measurements. In order to do so, [115] proposed a warning system in an electrical vehicle (EV) application. The system consisted of hardware architecture and an adaptive-algorithm-based software architecture. The software architecture enables each individual vehicle to generate its own look-up table about the junction temperature and the corresponding $V_{CE(on)}$. The voltage measurement was compared to a reference value in look-up tables.

Another CM method was proposed in [121] for monitoring the degradation of bond wires. The packaging is modified to include additional sensing wires bonded to the emitter contact on the chip as seen on Figure 1.13. These wires are connected to a resistor to increase its impedance and preventing the current from flowing through them. When there is a voltage change between the sense contact and the emitter contact terminals its indicative of bond wire failure.



(a) (b)

Figure 1.13. Bond wire lift-off detection scheme [121]: (a) No fault, (b) Fault

In the works performed in [116], [117] the evaluation of the SOH of the bond wires was evaluated by analyzing the change of waveforms during turn-on. The waveforms evaluated were V_{GE} and I_{GE}. In a component where bond wire degradation has been identified a faster increasing rate of V_{GE} can be noticed, as seen on Figure 1.14.

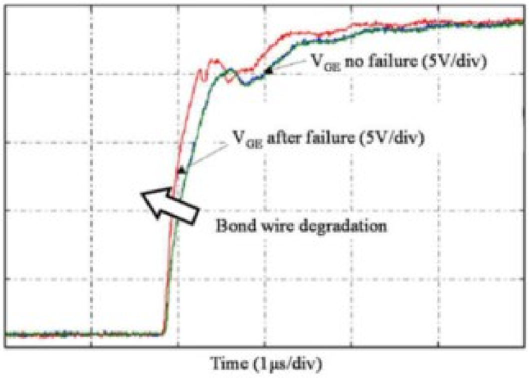


Figure 1.14. Gate-emitter voltage waveforms during turn-on [117]

1.5.2. Solder layer CM techniques

In the research carried out in [110], in addition to the CM of bond wires, it is possible to perform the CM of the solder layers of the module. This is possible by performing measurements of the junction temperature T_j and the case temperature T_c. This allows for the estimation of the thermal resistance R_{th} at a fixed current of 100 A with the help of Eq. (1.1). As it was indicated in Table 1.5, this parameter can be used for monitoring the degradation of the solder layers of the IGBT module.

$$R_{th_{jc}} = \frac{(T_j - T_c)}{V_{CE(on)100\mathrm{A}} \cdot 100\mathrm{A}} \tag{1.1}$$

Another method for assessing the SOH of solder layers of IGBT modules was proposed in [118]. The methodology proposed in that research can be seen in Figure 1.15. It is based on the measurement of T_c and the use of a thermal model and a power loss model to estimate the value of the thermal resistance R_{th}. Any variation from the initial R_{th} estimate might be indicative of degradation of the solder layers that constitute the thermal cooling path. The variation in the R_{th} is deduced from the differences in the initial loss model and an updated loss calculation.

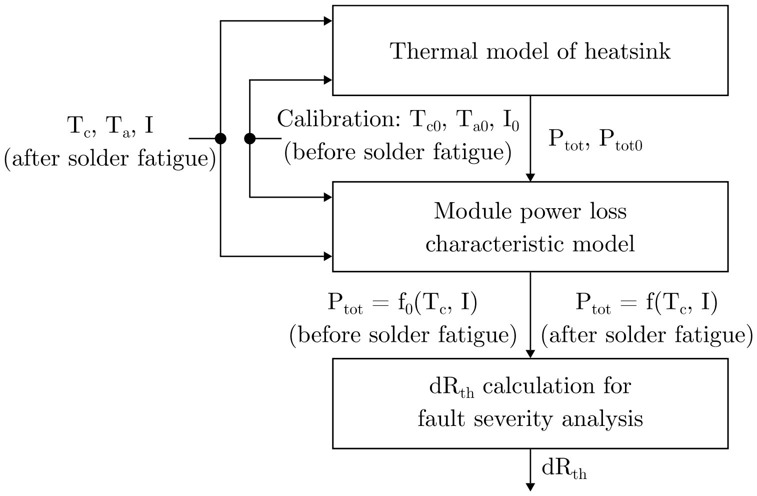


Figure 1.15. CM methodology for solder layers of power module [118]

Another work [119], proposed a methodology for the assessment of the degradation of the solder layers of IGBT modules based on the use of low-harmonics injection. The amplitude of the harmonics is correlated with the temperature. When an issue on the thermal path arises variations in the temperature readings are associated with degradation of the solder layer. This CM technique needs to use two control loops as seen in Figure 1.16. The inner loop is in charge of generating the harmonic content, while the outer loop suppresses the harmonics. The control signal of the outer loop reflects the degradation state of the solder layer.

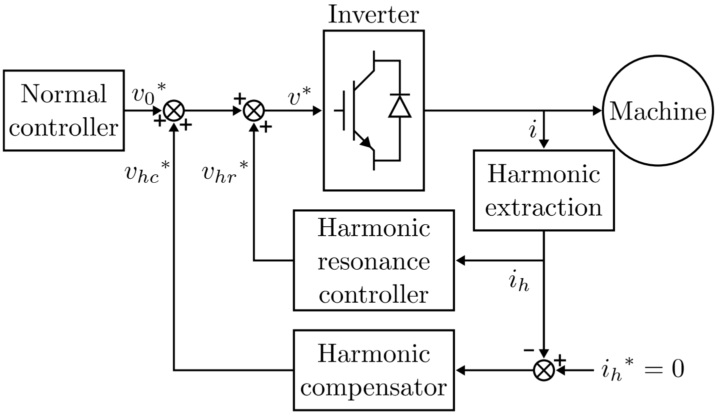


Figure 1.16. Solder fatigue CM scheme with harmonic injection [119]

In [122] the principal component analysis (PCA) technique was used for the detection of solder layer fatigue. In that research $V_{CE(on)}$, I_C and T_c were monitored to extract a vector of features. These features are compared with predetermined healthy features and the residuals between them are indicative of degradation of the thermal path. The CM scheme employed can be seen in Figure 1.17.

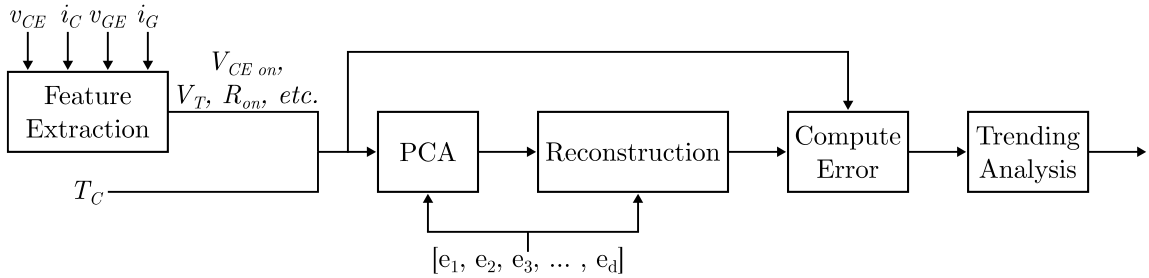


Figure 1.17. CM scheme for solder fatigue analysis with PCA [122]

The research work presented in [123] used a model estimate of the T_j for assessing the degradation state of the solder layers of IGBT modules. Additionally, a measurement of the real T_j was performed with the help of an infrared camera. The CM technique consisted in comparing the model estimates with the measurements issued with the IR camera. The model describes the healthy behavior of an IGBT module, so if any differences arise between the measurement and the estimate, it can be inferred that the solder layer is suffering of a degradation process.

Other works that used the estimation of the junction temperature T_j for the assessment of the SOH of IGBT modules were presented in [124]–[126]. $V_{CE(on)}$ measurements were employed for the estimation of T_j thanks to previous offline characterizations in [124]. The voltage measurement circuit used in this research can be seen in Figure 1.18.

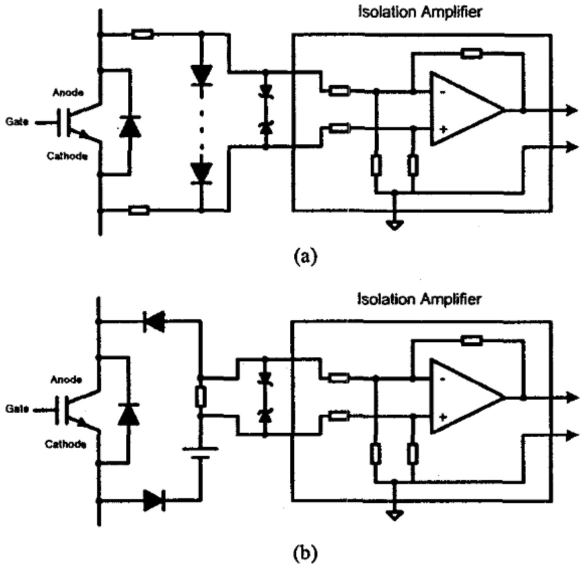


Figure 1.18. Circuit for measuring $V_{CE(on)}$ [124]: (a) For voltages 0V-600V, (b) For voltages 600V-2000V

Another CM strategy for solder layers was proposed in [127]. The method consisted in the use of a Kalman filter for T_j estimation. Afterwards, residual generation is employed for determining the state of the solder layers. The residuals are the difference between the estimate provided by the Kalman filter and T_j measurements thanks to the circuit seen in Figure 1.12. The residuals will become relevant when changes in the thermal path appear. In this work the Kalman filter acts as a fusion method that incorporates measurement data and a pre-calibrated model. The CM scheme employed in this work can be seen in Figure 1.19.

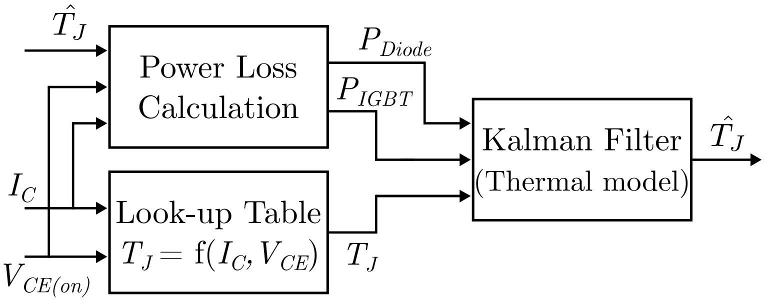


Figure 1.19. CM scheme employing a Kalman filter for T_j estimation [127]

The same author of the work in [127], proposed an alternative in [101] where the T_j measurement based on $V_{CE(on)}$ can be replaced by a measurement based on $V_{GE(th)}$. This can allegedly improve the performance of the Kalman filter scheme seen in Figure 1.19. The $V_{GE(th)}$ circuit proposed in that work can be seen in Figure 1.20.

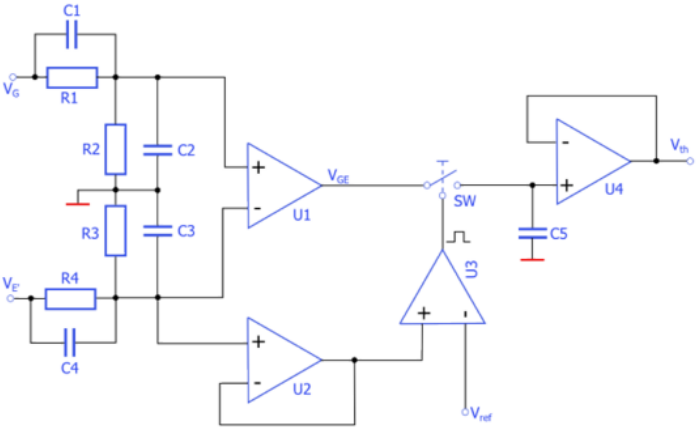


Figure 1.20. Circuit for measuring $V_{GE(th)}$ in the CM scheme proposed in [101]

1.6. Prognosis of IGBT modules

Extensive literature on different prognosis techniques and approaches was carried out. Two main approaches for performing prognosis were distinguished: The approach based on Physics-of-Failure (POF) methods and the Data-based approach. approaches will be discussed in the following lines.

1.6.1. Physics-of-Failure methods

Physics-of-Failure methods describe the physical process of a failure mechanism [101], [128]. These methods focus mainly on the wear-out mechanisms experienced by the studied component. These methods apply the knowledge of the physical characteristics of the element such as geometries, material properties, environmental and operational stresses to produce an estimate of component lifetime [101]. Additionally, the PoF-based assessment during the design process has been widely accepted as an efficient and cost-effective way for ensuring reliability [129], [130].

The PoF approach on IGBT modules was used to describe the electromigration mechanism of bond wires [131]. Soon, more PoF methods were developed for describing other failure mechanisms such as HCI [132] and TDDB [133]. Subsequently, the PoF approach started gaining relevance for addressing package-related failure mechanisms. The principal PoF models for addressing package-level issues are based on cyclic fatigue and fracture mechanics [134].

There is still room for improvement concerning the PoF approach. For instance, in the presence of different failure mechanisms, they can be mutually affected and lead to an accelerated degradation [135], [136]. The multi-stressor failure mechanisms are starting to be addressed by this approach. However, this field is still immature. Additionally, lifetime estimates obtained with PoF methods may have large uncertainties. This can happen due to the uncertainties behind manufacturing processes [101]. Another challenge that PoF methods are starting to deal with is the real-time implementation. This will allow for a more efficient and accurate reliability prediction as the actual stresses (environmental and operational) will be considered.

According to [137], [138], the implementation of a PoF methodology requires several steps as seen on Figure 1.21. The first step in this methodology must deal with the understanding of the potential failure mechanisms in the target application. Then, a stage ensues where the dominant failure mechanisms, the required environmental and operational variables are identified with the help of a virtual reliability assessment. The identified parameters will be used for performing in-situ monitoring [101]. Once the monitored parameters have been acquired, the relevant data will be simplified for its usage with PoF models.

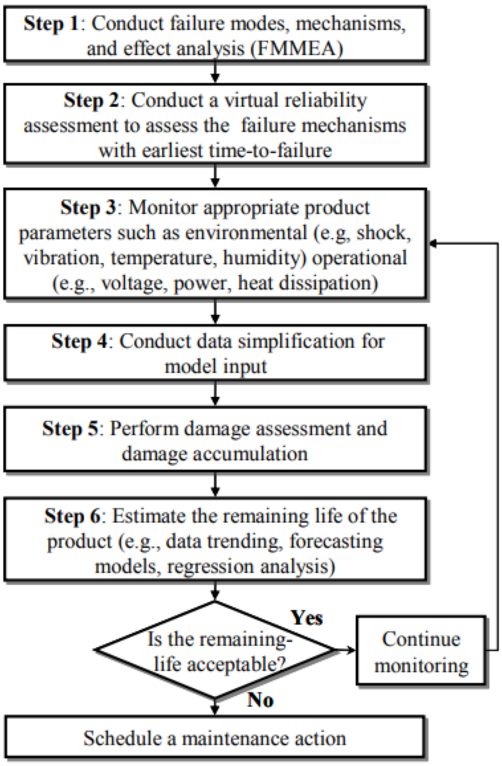


Figure 1.21. Framework for performing PoF-based life-consumption monitoring [138]

The Failure Mode, Mechanism and Effect Analysis (FMMEA) is conducted for identifying failure mechanisms and models for all failure modes and prioritizing failure mechanisms [139]. But as it was mentioned previously, the main failure mechanisms for IGBT modules were already identified and are related to the temperature loading of the components. Thus, for these elements, the necessary tools to be used for performing a PoF-based prognosis are data reduction methods and the PoF models. The following lines will describe the tools employed in the PoF methods for prognosis of IGBT module lifetime.

1.6.1.1. Lifetime models

This following section introduces the relationships between stress-strain and the number of cycles to failure N_f. Each strain swing (rise and fall) of the same amplitude causes a closed hysteresis loop (Figure 1.22) and is considered as a cycle (Figure 1.23) [140]. The total degradation for a given load profile is calculated by considering the cumulative effect of each hysteresis loop. In such case, cycle counting is necessary in order to be able to obtain stresses and also count the number of hysteresis loops in a given profile. The counting algorithms will be discussed in a different section.

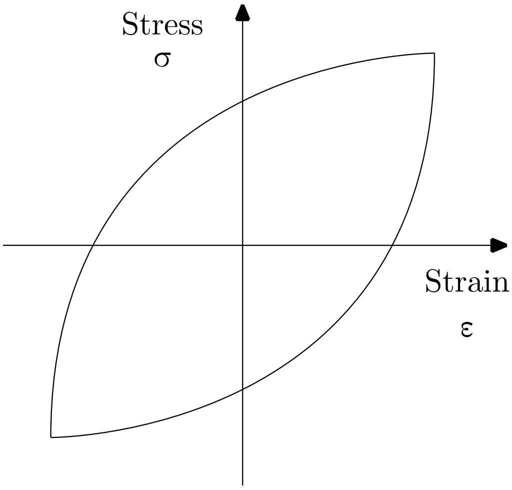


Figure 1.22. Hysteresis stress-strain loop of a material

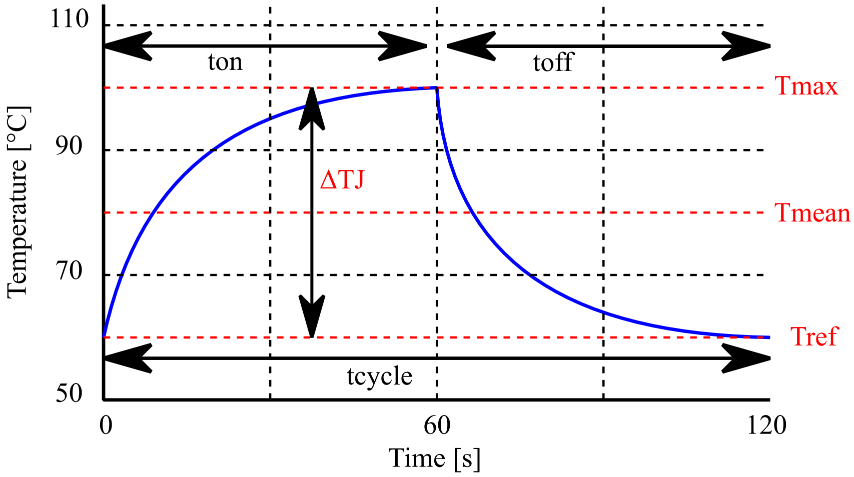


Figure 1.23. Example of thermal cycle for lifetime models

Two of the main failure mechanisms of wire bonded semiconductor packs are wire-bonds lift-off and solder cracking [72]. These failures are temperature related. Hence, from the temperature profiles, both types of failures have to be modeled to estimate their respective lifetime and the IGBT lifetime.

The failure mechanisms are associated with a mismatch of thermal expansion coefficients of the different layers of the power semiconductors [28]. The ratio of increase in length to the original length of a material is known as strain ε. There are two types of strain: elastic and plastic. On the one hand the elastic strain is the portion of strain which can be recovered upon unloading. On the other hand, the plastic strain is the portion of strain that cannot be recovered upon unloading and is the main cause of permanent damage. Both strain types cause stress σ to the material.

The lifetime models aim to translate the strain from the temperature profile and obtain the equivalent stress applied to the different layers of the semiconductors. They also aim to express the critical stress for a given thermal condition in terms of the number of cycles to failure N_f that a semiconductor can withstand under the applied thermal conditions. The models can be further classified into analytical and physical modelling methods. The former gives the relation between the experienced thermal cycles and N_f. The latter methods are based on finite-element (FE) analysis. As FE simulation tend to have high computational requirements, this thesis makes use of analytical lifetime prediction models.

1.6.1.1.1. Analytical lifetime models

In the literature many different types of analytical lifetime models can be found [72], [99], [141]–[144] and the more popular are described in Table 1.6 [145].

Model name	Model for cycles to failure N_f	Constants	Variables
Coffin-Manson	$A \cdot \Delta T_j^{\beta_1}$	A, β_1	Temperature swing (ΔT)
Coffin-Manson-Arrhenius	$A \cdot \Delta T_j^{\beta_1} \cdot \exp\left(\frac{E_a}{k \cdot T_m}\right)$	A, β_1, k, E_a	ΔT, mean temperature (T_m)
Norris-Landzberg	$A \cdot f^{\beta_2} \cdot \Delta T_j^{\beta_1} \cdot \exp\left(\frac{E_a}{k \cdot T_m}\right)$	A, β_1, β_2, k, E_a	ΔT, T_m, frequency (f)
Bayerer	$A \cdot \Delta T_j^{\beta_1} \cdot \exp\left(\frac{\beta_2}{T_{j_{min}} + 273}\right) \cdot {t_{on}}^{\beta_3} \cdot {I_B}^{\beta_4} \cdot {V_C}^{\beta_5} \cdot D^{\beta_6}$	A, β_1, β_2, β_3, β_4, β_5, β_6	Minimum junction temperature ($T_{j_{min}}$), heating time (t_{on}), current per bond foot (I_B), bond wire diameter (D) and voltage class (V_C)
Held	$0.5\left[\frac{L \cdot \Delta\alpha \cdot \Delta T}{\gamma \cdot \chi}\right]^{1/c}$	CTE mismatch between the two surfaces near solder joint ($\Delta\alpha$), fatigue exponent (c)	Typical lateral size of the solder joint (L), thickness of the solder layer (χ) and ductility factor of the solder (γ)
Black	$A \cdot I^2 \cdot \exp\left(\frac{E_a}{k \cdot T_m}\right)$	A, k, E_a	Current (I), T_m

Table 1.6 Popular lifetime models for various design parameters and variables [145]

Among the lifetime prediction models presented in Table 1.6, the simplest is the Coffin-Manson model [72], [141]. This model only makes use of the temperature swings ΔT_j experienced by the semiconductor devices. It also makes use of constants that depend on the semiconductor characteristics. The values of these constants can be obtained by numerical simulations or experimental measurements. The formulation of this model can be seen in Eq. (1.2):

$$N_f = A \cdot \Delta T_j^{\beta_1} \tag{1.2}$$

An improved version of the Coffin-Manson model was presented in [142] and can be seen in Eq. (1.3). This model also considers an Arrhenius term that considers the medium temperature T_m on the considered thermal cycle. Additionally, the model requires the Boltzmann constant k and the activation energy E_a that can be determined experimentally.

$$N_f = A \cdot \Delta T_j^{\beta_1} \cdot \exp\left(\frac{E_a}{k \cdot T_m}\right) \tag{1.3}$$

A more complete lifetime prediction model derived from Eq. (3.6) is the Norris-Landzberg model [143] and is presented in Eq. (1.4). This model considers the same parameters as the improved Coffin-Manson-Arrhenius model and also the frequency parameter f of the experienced thermal cycles.

$$N_f = A \cdot f^{\beta_2} \cdot \Delta T_j^{\beta_1} \cdot \exp\left(\frac{E_a}{k \cdot T_m}\right) \tag{1.4}$$

Another analytical model derived from the Coffin-Manson model is the Bayerer model [144]. This model can be seen in Eq. (1.5) and is considered the more complete lifetime prediction model as it considers several parameters such as the heating time t_{on} of the thermal cycles, the minimum junction temperature $T_{j_{min}}$, the current per bond foot I_B, the voltage class of the semiconductor V_C and the bond wire diameter D.

$$N_f = A \cdot \Delta T_j^{\beta_1} \cdot \exp\left(\frac{\beta_2}{T_{j_{min}} + 273}\right) \cdot {t_{on}}^{\beta_3} \cdot {I_B}^{\beta_4} \cdot {V_C}^{\beta_5} \cdot D^{\beta_6} \tag{1.5}$$

Another model that is also derived from the Coffin-Manson law is the Held (large solder joint) model seen in Eq. (1.6). This model considers the geometry of the solder joint as well as the material characteristics to effectively compute the number of cycles to failure.

$$N_f = 0.5\left[\frac{L \cdot \Delta\alpha \cdot \Delta T}{\gamma \cdot \chi}\right]^{1/c} \tag{1.6}$$

1.6.1.1.2. Physical lifetime models

These models can be categorized in stress-, strain-, energy-, and damage-based models. Among these, energy-based models are the most convenient and produce more accurate results as they reproduce test conditions more accurately [146]. These models are used to predict fatigue failures on the basis of a hysteresis energy term or type of volume-weighted average stress-strain history [147]. Fatigue energy is calculated from some correlation to the energy under the stress–strain hysteresis loop [148].

1.6.1.1.2.1. Solder joint models

In [149] a model (Eq. (1.7)) is presented based on the total strain energy ΔW_{total}, the rest of the values are fatigue coefficients derived from experiments.

$$N_f = \left(\frac{\Delta W_{total}}{W_0}\right)^{1/k} \tag{1.7}$$

In [148] a model (Eq. (1.8)) based on the stress-strain hysteresis energy density W_{SS} the other parameters are temperature-dependent material constants derived from fatigue tests.

$$N_f = C(W_{ss})^{-m} \tag{1.8}$$

In [150] a model (Eq. (1.9)) based on the critical strain energy is presented, where C is the critical value attained, E_p and E_c are the creep and elastic energies calculated thanks to finite element analysis.

$$C = N_f\left(a\, E_p + b\, E_c\right) \tag{1.9}$$

1.6.1.1.2.2. Bond wire models

The model in [151] (Eq. (1.10)) employs Coffin-Manson relationship between N_f to the plastic strain induced per cycle (ϵ_{pl}). C_1 and C_2 are constants obtained from stress experiments.

$$N_f = C_1\left(\Delta\epsilon_{pl}\right)^{C_2} \tag{1.10}$$

When the bond wire is below the yield stress the lifetime can be obtained with Eq. (1.11) [152]. It employs the stress range instead of the strain amplitude, the other constants are obtained by means of FEA.

$$N_f = C_3(\Delta\sigma)^{C_4} \tag{1.11}$$

Finally, a model based on the energy density [153] can be seen in Eq. (1.12). The number of N_f is associated to the current of the wire-bond. w_{pl} is the dissipated energy in one ribbon corresponding to the current I and w_{pl}^{cr} is the accumulated plastic strain energy density for the lifetime of the ribbon.

$$N_{f(I)} = \frac{w_{pl}^{cr}}{w_{pl(I)}} \tag{1.12}$$

1.6.1.2. Cycle counting methods

The PoF prognosis approach for IGBT modules consists in the evaluation of the thermal loading profiles experienced by the semiconductors. The raw thermal loading cannot be exploited by PoF lifetime models. Hence, a preprocessing stage is required. This preprocessing consists of the identification of thermal cycles, which will generate closed stress-strain hysteresis loops [154].

Several different counting algorithms exist in the literature. The more commonly used methods can be seen in Figure 1.24 [155], they are the half-cycle, the maximum edge, the rising edge and the rainflow algorithm. Among the counting algorithms the rainflow counting method has gained in popularity as it has little relative error when compared to other cycle counting methods [155]. Thus, this method will be covered in more detail, since it will be the counting method used in this thesis.

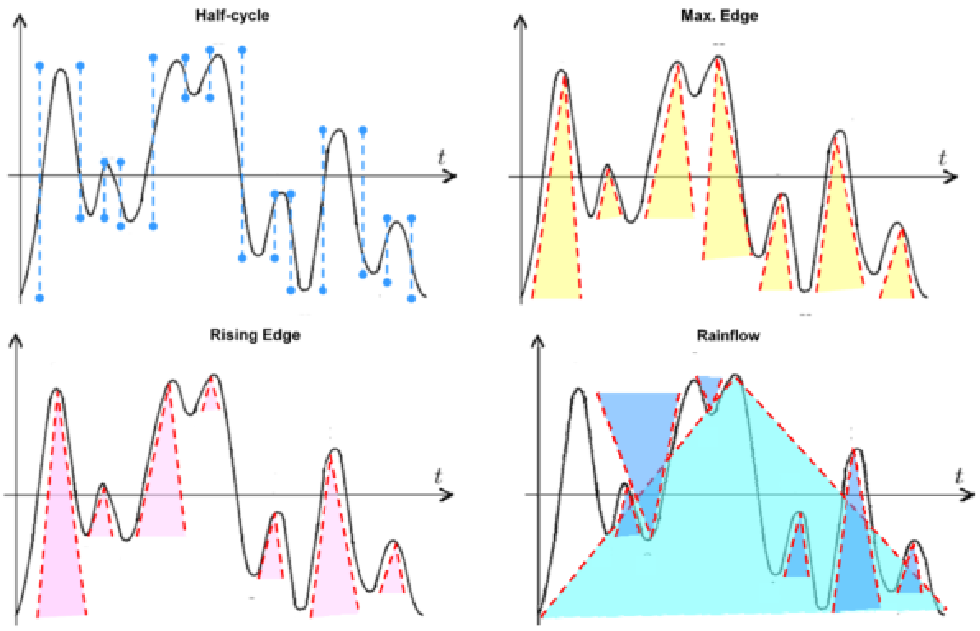


Figure 1.24. Graphical illustration of different counting algorithms [155]

1.6.1.2.1. Rainflow Counting Algorithm

This methodology was first described by Matsuishi and Endo [156] and is inspired by the form of rain flows dripping from pagoda roofs as evidenced by Figure 1.25 (a). As mentioned previously, this method maps the different stress-strain hysteresis loops (Figure 1.25 (b)) issued from the loading profile.

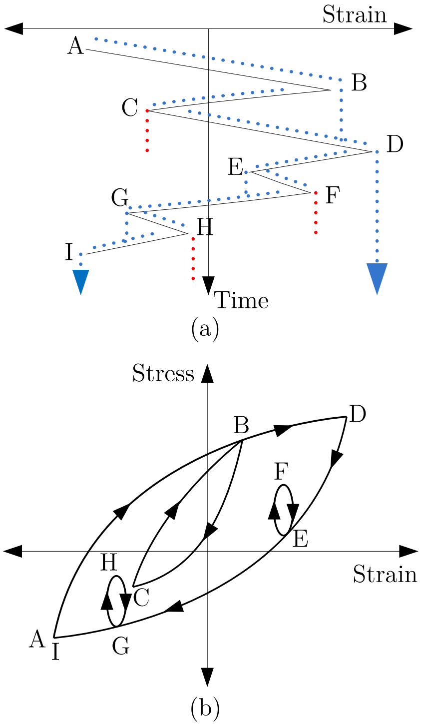


Figure 1.25. Rainflow on: (a) a load sequence, (b) stress-strain plot [140]

1.6.1.3. Cumulative Damage models

After having organized the different thermal models with a counting method and obtaining the number of cycles to failure N_f with the lifetime models, the damage suffered by the device can be calculated. This is possible by using cumulative damage models. In Table 1.7 [49], the more important cumulative damage models in the literature are presented.

Cumulative Damage model	Characteristics	Equations
Linear damage rule (Miner's)	- LDE, nLLD, nLSC, nLIC - Analytic - Many applications - Popular in IGBT lifetime - Simple	$D = \sum \frac{n}{N_f} = 1$
Double linear damage rule	- LDE, LLD, LSC, nLIC - Analytic - Many applications - Simple	$D_l = \sum \frac{n}{N_l} = 1$ $D_{ll} = \sum \frac{n}{N_{ll}} = 1$ $N_l = f(N_f)$ $N_{ll} = N_f - N_l$
Non-linear damage rule	- nLDE, LLD, LSC, nLIC - Analytic - Some applications	$D = \left(\frac{n}{N_f}\right)^{\dot{g}(\Delta T_j)} = 1$
Crack growth[1]	- nLDE, LLD, LSC, nLIC - Some applications - Complex	$\frac{da}{dN} = g(a, \Delta T_j, T_{jmax})$ $D = \frac{a}{a_c} = 1$
Crack growth and retardation[2]	- nLDE, LLD, LSC, nLIC - Some applications - Complex	$\frac{da}{dN} = C(\Delta T_j) \cdot g(a, \Delta T_j, T_{jmax})$ $D = \frac{a}{a_c} = 1$
LDE: linear damage evolution; LLD: load level dependent LSC: load sequence considered; LIC: load interaction considered nX: X is not considered or concerned [1] Damage is modeled as growth of a hypothetical crack [2] Damage retardation due to load interaction effect		

Table 1.7 Analytical cumulative damage models [49]

Miner's rule is the most popular out of the bunch of cumulative damage models. It assumes that degradation caused by the contribution of each thermal cycle can be added linearly. However, non-linear relationships between cycle magnitude and damage, interaction between cycles and non-linear damage evolution can limit the accuracy of prediction [49]. To deal with this issue some other cumulative damage models exist as seen on Table 1.7. Nevertheless, linear degradation with simple rainflow counting are still the preferred techniques for IGBT lifetime estimation.

Lifetime estimation only considers the thermal loading as the damaging agent of power modules. However, other parameters such as humidity, corrosive environments and cosmic ray can lead to an even lower lifetime. Hence, lifetime estimation based just on thermal loading represents the upper bound for lifetime estimation in a particular application [42].

1.6.1.4. Examples of PoF methods

In [157], a real-time PoF approach for IGBTs was presented. The thermal loading is computed with the help of a reduced thermal model. Afterwards the rainflow counting algorithm extracts the relevant information from the thermal profile. These extracted features are translated to mechanical stress with the help of a finite element analysis (FEA) simulation [158]. Then a Coffin-Manson lifetime model is used along with linear damage accumulation rule to calculate life consumption of weak elements of IGBT modules. The methodology can be seen in Figure 1.26.

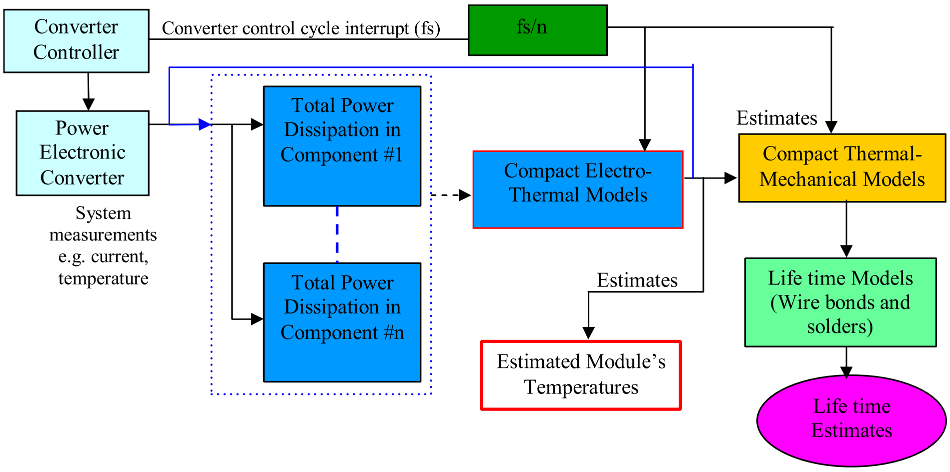


Figure 1.26. PoF approach for prognosis of IGBT modules in [157]

The work presented in [159] made a more practical prognostic computation for voltage source inverters for wind turbine applications, assuming solder joint fatigue to be the dominant failure mechanism.

In the work presented in [160], a similar approach was considered. However, in this work three different timescales were considered for the evaluation of the lifetime consumption in an offshore wind application. Additionally, instead of using analytical lifetime models, this work used manufacturer cycling information for performing the lifetime consumption computations.

Other examples of PoF approaches for prognosis were reported in [29], [30]. The prognosis was done considering two different timescales for a HVDC-MMC application. In addition, a model-based extrapolation method was proposed for using manufacturer power cycling information. The model-based extrapolation is based on the Norris-Landzberg equation [143].

There are several other examples of PoF in the literature [83], [111], [120], [129], [157], [161]–[164], which make this approach the more popular for the prognosis of the lifetime of IGBT power modules.

1.6.2. Data-based methods

Data-based methods for prognosis do not require specific knowledge about the studied component/system [165]. The information to assess health state is obtained from historical data. The main data-driven methods employed for prognosis are machine-learning techniques and statistics and probability theory [51].

These methods are advantageous compared to PoF techniques if the studied systems are hard to model [166]. The primary strength of these approaches is the ability to transform high-dimensional noisy data into lower dimensional information for prognostic decisions [167], [168]. Finally, the deployment of these techniques is quick and cheap and has a larger scope of applications than model-based methods.

The weakness of this approach is that its performance is highly dependent on the analyzed data, both in quantity and in quality [167]. Another difficulty comes from the fact that it is difficult to obtain run-to-failure data, particularly for new systems, since they are conceived to have longer lifespans.

According to [101], data-based methods use in-situ measurements of parameters that are correlated to failures. Measured data changes its statistical characteristics over time as a result of degradation. Hence, detection of changing trends allows for the estimation of the remaining time before a failure happens [169].

The main failure precursors for IGBT modules were presented in Table 1.5. The estimates obtained with data-based methods use the DSEPs as inputs. Then black-box non-physical models are used to learn the time behavior of the historical data. The models are then used to predict the evolution of the failure precursors and obtain an estimate of the modules remaining useful life (RUL). In order to be able to apply these techniques, threshold values must be defined for the failure precursors. If these values are exceeded, it means that the module has already reached the end of its functionality. Some of the failure criteria found on the literature for the failure precursors can be seen on Table 1.8.

Parameter	Symbol	Failure criteria deviation
Collector-emitter saturation voltage	$V_{CE(sat)}$	5%
Gate-emitter threshold voltage	$V_{GE(th)}$	20%
Collector current	I_C	20%
Junction temperature	T_j	20%
Gate saturation current	$I_{G(sat)}$	20%
Thermal impedance	Z_{th}	20%

Table 1.8 Failure criteria of the different DSEPs of an IGBT module [170], [171]

1.6.2.1. Examples of Data-based methods

The research presented in [172] proposes a data-based scheme for the prognosis of the state-of-health of IGBTs. The scheme is depicted in Figure 1.27, it is based on the use of $V_{CE(on)}$ as the failure indicator. A healthy data base of the failure indicator is used as the training data. Any deviation measured online from the healthy dataset is computed with the Mahalanobis Distance (MD). The measurements are performed at constant temperature and current conditions for isolating the loading conditions. Finally, a particle filter is used for predicting the evolution of $V_{CE(on)}$.

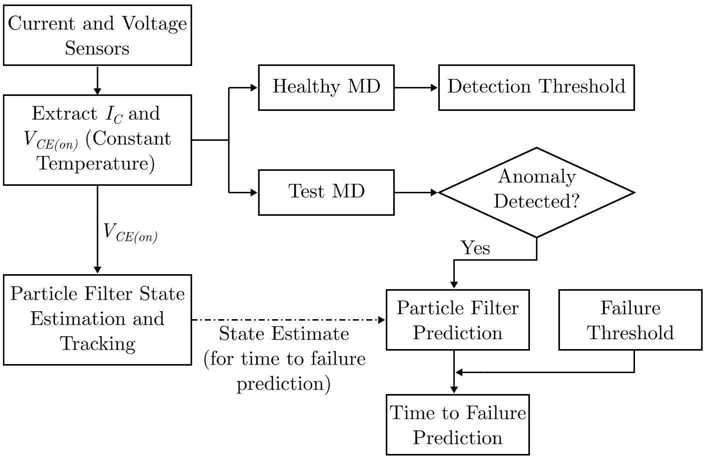


Figure 1.27. Prognostic scheme proposed in [172]

In [173]–[175] the scheme seen in Figure 1.28 was proposed. This scheme is valid for both MOSFETs and IGBT devices.

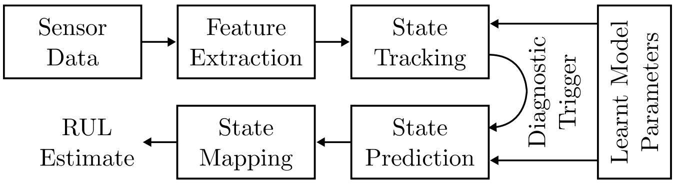


Figure 1.28. Prognostic scheme proposed in [173]–[175]

An example of a dataset used on a data-driven prognosis scheme can be seen in Figure 1.29 [176]. In this work the failure precursors monitored were the T_j and $V_{CE(on)}$. Two different classes of training data were used. One describes brand-new IGBT modules whereas the other describes aged modules. In Figure 1.29 the training data can be seen as well as the boundary between both classes.

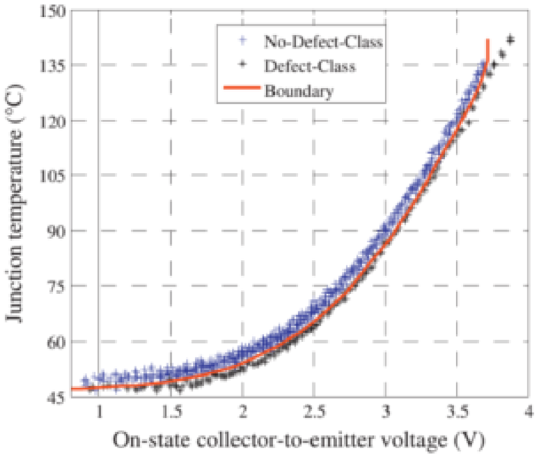


Figure 1.29. Healthy and aged data of T_j and $V_{CE(on)}$ [176]

In [177], a probabilistic Monte Carlo framework is presented for the calculation of the RUL. This framework can be seen in Figure 1.30. This approach uses the $V_{CE(on)}$ as the monitored failure precursor along with Monte Carlo simulations to evaluate several degradation paths into the future. The RUL can be either the mean or the median of the multiple propagated paths. The propagated paths are based on probability distributions fitted to the aged data after performing power cycling tests.

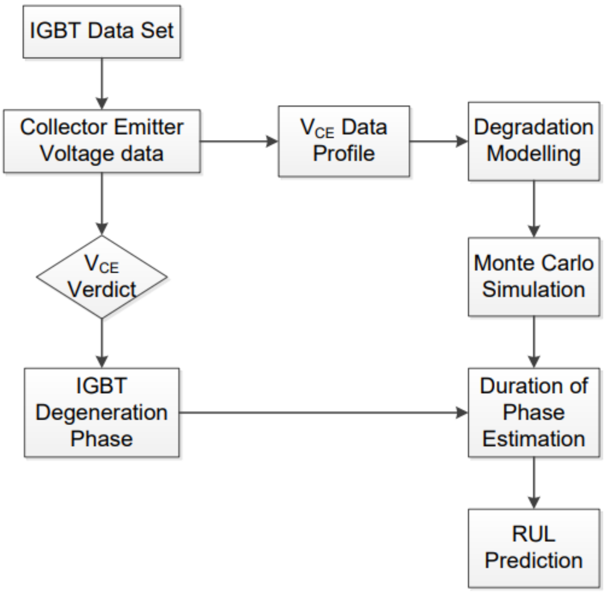


Figure 1.30. Data-driven scheme for RUL estimation [177]

Another work using a simpler data-driven approach was reported in [178]. This work uses the simple state-based prognostics (SSBP) method for the estimation of the RUL of IGBT devices. The SSBP model evaluates a finite number of discrete states for statistical evaluation of the evolution of the failure mode. Three stages are required for performing the RUL computation: clustering, cluster evaluation and RUL computation as seen on Figure 1.31.

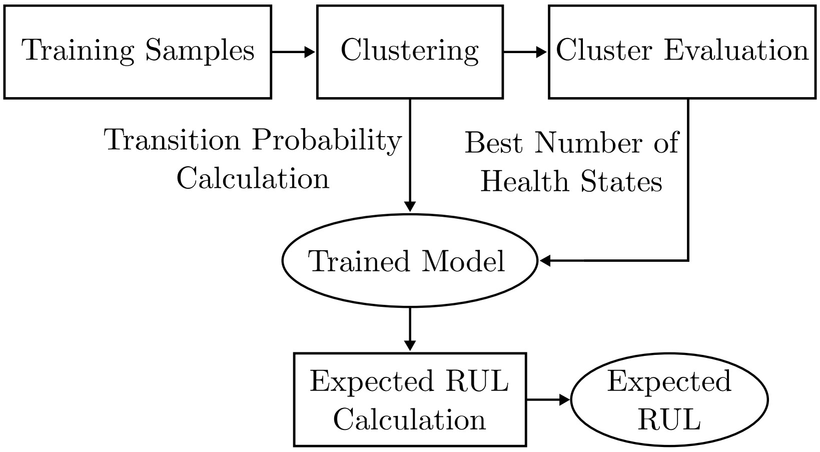


Figure 1.31. Steps of the SSBP method for RUL computation [178]

In [111], an empirical degradation model was proposed. It is based on the evolution of the on-state resistance of a component and represents die-attach failures. It uses a linear discrete model for Bayesian tracking algorithms like extended Kalman filter (eKF).

The use of a particle filter along with second-order least squares regression was used in [179]. This approach used once again $V_{CE(on)}$ as the DSEP for the implementation of the prognosis scheme. The RUL estimation was simulated with boundary levels calculated with a Gaussian probability distribution of the particles by the end-of-life estimation.

A Gaussian Process Regression (GPR) technique was proposed in [173] for assessing the RUL of MOSFET devices based on its on-state resistance. A mean function is used to describe the RUL prediction. The computation of the uncertainties is done by the use of a covariance function.

Also, a computation-efficient statistical method was presented in [180], This method tracks the evolution of $V_{CE(on)}$ over discrete phases throughout the useful life of the module. The duration of each phase provides the basis for the calculation of a probability model.

In prognosis, artificial neural networks (ANN) are reputed for being able to model non-linear trends, like the degradation trend present in power module devices [54]. The structure of a classical ANN can be seen in Figure 1.32. The complexity of ANN methods resides in the fact that the number of hidden layers and nodes become critical issues in the training process [54].

An example of ANN being used for prognosis of IGBT modules was reported in [181]. In this work a particular architecture of ANN was chosen, the Time-Delay neural network (TDNN). This architecture is similar to the traditional feed-forward neural network but the input signals are augmented by using a time-delay varying activation on the inputs, and propagates through in a similar way to feed-forward fashion connection [54]. Along with the TDNN (Figure 1.33), a statistical approach was used for modelling the RUL.

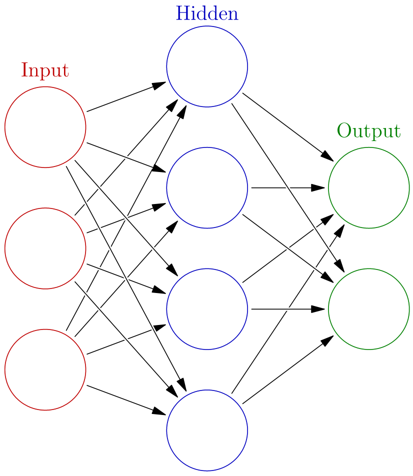


Figure 1.32. Traditional structure of an ANN

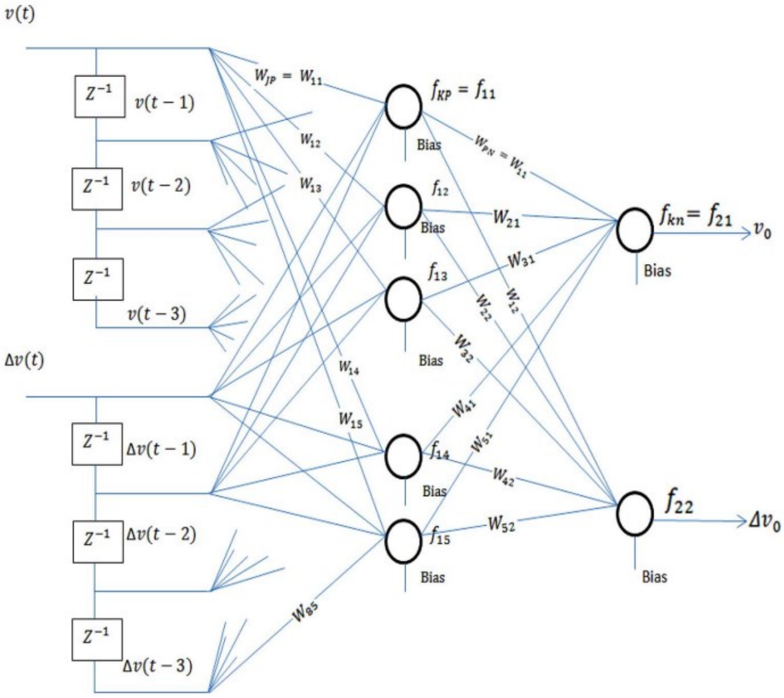


Figure 1.33. TDNN proposed in [181]

Also, knowledge-based models (KBA) can be used for the prognosis of the RUL of the devices. They use graphical models, such as Bayesian networks and rule-based reasoning. These models are simpler than classical PoF or other data-driven models where end-of-life data is required. Expert systems and fuzzy logics are some of the most traditional KBA [182].

An example of KBA on the prognosis of lifetime of IGBT modules was reported in [183]. In this work the chosen KBA technique was the adaptive neuro-fuzzy inference system (ANFIS). Two parameters were monitored T_j and $V_{CE(on)}$, which were used to train a fuzzy Sugeno model (FSM) for mapping the membership function from input to output.

1.6.3. Fusion methods

These methods combine the benefits of both PoF and Data-based methods, while overcoming the disadvantages of each of them. These methods make the most of the available information, such as failure precursors, loading profiles, lifetime models, material properties, geometries, in order to compute a lifetime estimate with improved accuracy. It is considered to be an open research field [184].

According to [185], fusion can happen at different levels of the CM/prognosis framework (see Figure 1.34). The easiest fusion would be sensor fusion. It combines the readings of multiple sensors to improve the accuracy of feature extraction. The next level has to deal with feature fusion. It means that the data extracted from different sources is combined and processed (e.g. weighting techniques). The final and highest level for fusion techniques is that of knowledge fusion, where different lifetime estimates coming from different techniques such as PoF or data-based approaches are combined [101].

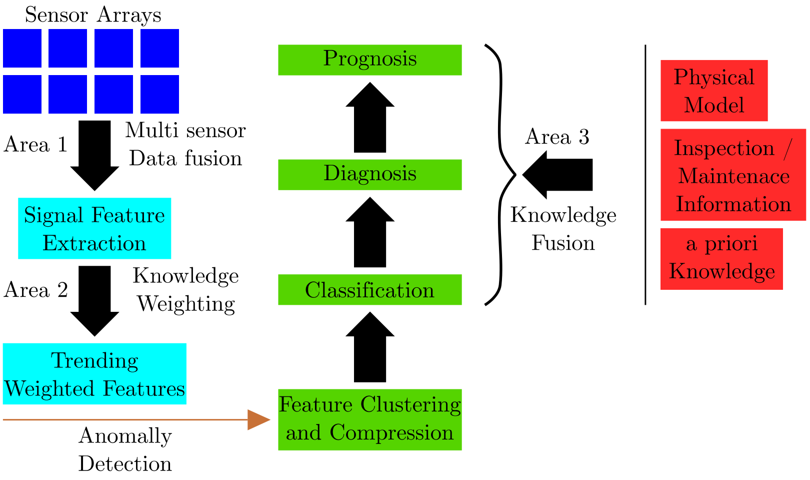


Figure 1.34. Levels for performing fusion techniques [185]

1.6.3.1. Examples of Fusion methods

A knowledge fusion strategy was proposed in [186]. A healthy baseline data is compared with online measurements to detect any changing trends indicative of degradation. Parameters that exhibit progressive degradation are isolated and used as inputs for the prognosis of lifetime. The chosen parameters are indicative of different failure mechanisms, thus individual PoF models can be used accordingly. The strategy also uses the historical loading using failure models. Finally, two RUL computations coming from different sources are combined. The fusion strategy scheme can be seen in Figure 1.35.

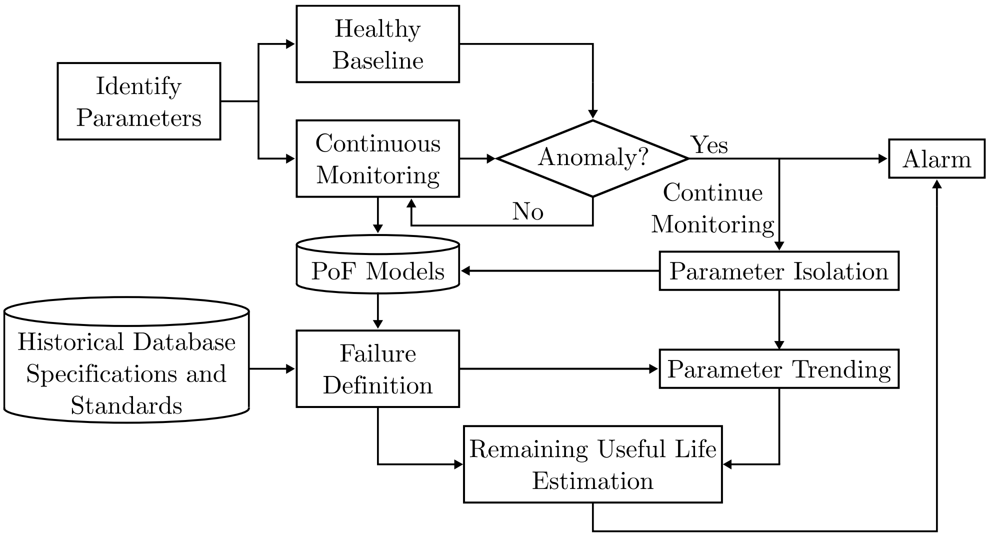


Figure 1.35. Fusion prognosis approach presented in [186]

Another example at the highest fusion-level was proposed in [187]. In this work a mathematical model of the system was used. A real degradation profile was induced on the real system and measurement of inputs and output quantities such as voltages and currents were acquired. The input/output impedances and admittances are calculated to get a transfer function of the system. A damage model is finally fused with energy relaxation from the system, its attenuation and the loading profile. Then a fuzzy RUL estimator computes the RUL.

Some other examples of fusion methods were reported: In [188], a transferable belief model fused the RUL estimates of two different prognosis algorithms. The fused estimate proved more accurate, and more reliable than the individual prognosis algorithms employed.

In [101], a strategy for calculating the RUL of IGBT modules was proposed. It mixed data measurement for tracking the evolution of $V_{CE(on)}$ as the bond wires degrade due to cycling conditions. In addition, a model-based approach is also applied in the form of a Kalman filter to track the evolution of T_j and infer degradations to the solder layer of IGBTs. Mixing the data tracking of the DSEP with the model-based estimation can improve the accuracy of the life prognosis.

The time-delay neural network proposed in [181] (Figure 1.33) makes part of a larger prognosis scheme. The complete approach uses a model-based lifetime estimation and measured-data as well as the TDNN for computing the IGBT lifetime [54]. The complete fusion prognosis scheme can be seen in Figure 1.36.

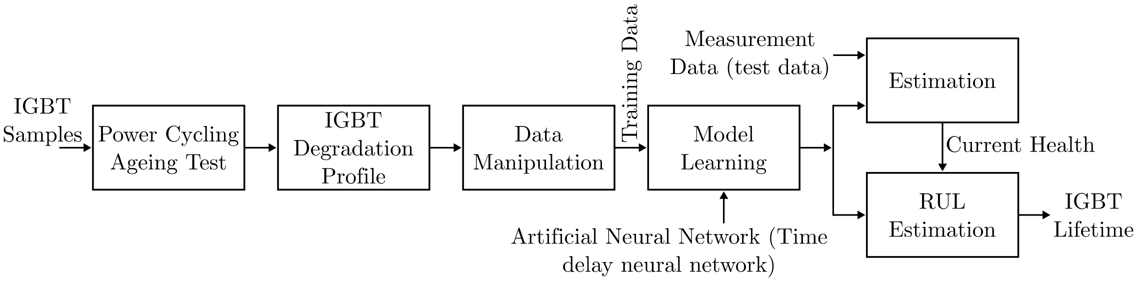


Figure 1.36. Data-mining prognosis approach proposed in [54]

1.7. Chapter conclusion

In this chapter, a thorough review of the relevant literature on IGBT modules was made. The technologies of IGBT modules suited for high-power applications were presented. It was also mentioned that for the rest of this study the focus will be made on wire-bonded (Flat-Pack) technology for IGBT modules.

Subsequently, a major review on the different failure mechanisms for wire-bonded modules was performed. It was concluded that even if IGBT modules can suffer from die-related issues, the more relevant issues to this type of component are packaging-related. Moreover, it was seen that there are failure mechanisms activated due to overstresses and wear-out processes. Only wear-out failures can be subjected to condition monitoring schemes. Therefore, this work will focus on wear-out failures.

Afterwards, some of the parameters used for monitoring the degradation of IGBT modules were presented. Additionally, the more relevant condition monitoring techniques for package-related issues of IGBT modules were presented. The reviewed techniques are the ones useful for detecting the degradation of the bond wires or the solder layers of power modules.

Finally, this chapter introduced the basic notions for the prognosis of the state-of-health of IGBT modules. The prognosis techniques can be grouped into PoF and data-based approaches. The PoF approach uses a deep understanding of the physics behind the main failure mechanisms. On the other hand, the data-based approach relies on the use of historical data combined with machine-learning techniques as well as statistics and probability theory. Also, some examples of fusion approaches were introduced. The fusion methods try to exploit the strengths in both PoF and data-driven techniques without having to deal with its basic limitations.

Before being able to test any prognosis and CM approaches it is necessary to understand the environment and the loading conditions that the power module will experience in the target application. Therefore Chapter 2 of this thesis will focus on the modelling of the environment and loading conditions to be experienced by the IGBT module in an HVDC-MMC application.

In this thesis, a methodology for the prognosis of the lifetime of an IGBT module inside a submodule of an MMC is presented in Chapter 3. The approach employed for the lifetime estimation is PoF based. From this methodology, some reliability metrics will be evaluated and the calculation of the required redundancy for the converter can be obtained.

As for the condition monitoring it is first necessary to activate the failure mechanisms in order to see an evolution of the DSEPs. Thus, this requires for the use of a power cycling testbench that activates the relevant temperature-dependent failure mechanisms. Chapter 4 of this work will deal in further detail on the design and deployment of a power cycling testbench and the chosen CM approach to track the degradation of IGBT modules.

2. MMC modelling for lifetime estimation and reliability analysis

2.1. Introduction

The Modular Multilevel Converter topology was previously presented. It was already mentioned that this topology is one if the main enablers of VSC-HVDC systems and is the most promising topologies for Multi Terminal DC (MTDC) grids [7], [9].

It is in this perspective that the reliability of the elements of the MMC is of crucial importance. In order to make reliability studies, first is necessary to get a more thorough understanding of the MMC topology and its functioning. It is important to notice that the purpose of the MMC modelling is to obtain the necessary inputs for carrying out reliability studies at component level.

In this chapter, the principles for the modelling of a MMC will be presented. Consequently, a mixed modelling technique enabling the analysis of component level characteristics will be performed.

Afterwards, the mathematical description of the topology will be proposed. Then, the control strategy required for an accurate functioning of the converter will be briefly discussed. Finally, the simulation results of a MMC will be presented in order to validate the modelling approach and the control strategy.

2.2. Modelling background

Several types of models can be found in the literature to describe the operation of modular multilevel converters [189]–[194]. The models are often categorized according to different criteria such as the number of state variables, the time or frequency domain, the control laws or the implementation techniques [195]. According to the CIGRE [196], there are 7 types of models for HVDC converters.

- Type 1, Full Physics-Based Models: the semiconductors are represented by their own sets of differential equations
- Type 2, Full Detailed Models: employs simplified nonlinear semiconductor models based on I/V curves
- Type 3, Simplified Switchable Resistance Models: the semiconductors are represented by two-value resistances, representing the ON and OFF states
- Type 4, Detailed Equivalent Circuit Models: based on type 3 models, but reductions (Thevenin/Norton) are performed to reduce the number of nodes
- Type 5, Average Value Models (AVM) based on switching functions: state variables and inputs are represented by their average values. The AC and DC side characteristics are modelled as controlled current and voltage sources
- Type 6, Simplified Average Value Models: similar to type 5 models, but the sources are represented in the phasor domain

- Type 7, RMS Load-Flow Models: they are employed for representing the steady-state converter outputs

As mentioned previously, there are different criteria for selecting a particular type of modelling technique [197]. The lifetime estimation methodology developed in this thesis focuses on the semiconductors of a single submodule (SM) among the 2400 (6 arms × 400 SMs/arm) necessary for converter operation.

In order to be able to simulate the electrical behavior of a single submodule Type 4 and Type 5 models will be retained. Afterwards, a mixed averaged-detailed model was developed for studying the MMC topology.

To understand the functioning of the averaged-detailed model, first a more detailed description of Type 4 and Type 5 models is required. Thus, these models will be presented in the following paragraphs.

2.2.1. Type 5 model – Reduced order average model

This model is valid if the voltages across the capacitors of a SM in one arm are balanced and all the SM capacitors are identical. If the previous conditions are met, then the number of state values associated with the SM capacitor voltages can be reduced to one per arm [189]. Similarly, the switching function variables, i.e. the bypass/insertion orders for the individual SMs, can be averaged to one control variable [195].

The aforementioned simplifications allow the modelling of a converter arm as one equivalent voltage source which represents the voltage generated by the inserted SMs, one equivalent current source to represent the charging dynamics of the SM capacitors and one equivalent capacitor. This model can be seen in Figure 2.1. The controlled voltage and current sources are regulated with the modulation index m.

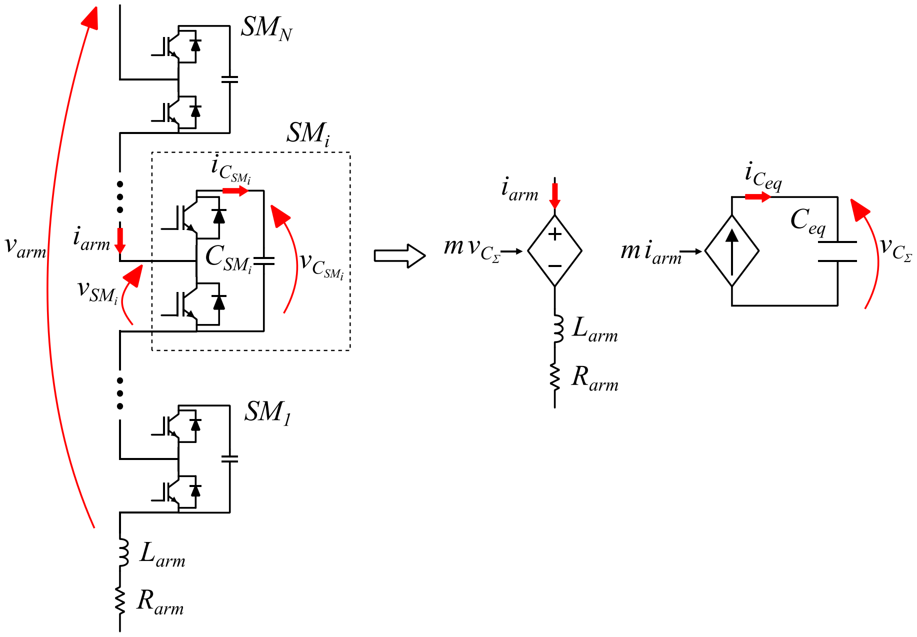


Figure 2.1. Converter arm and its reduced order average model

The derivation of this model is described in Appendix A.1. From that analysis, the expressions describing the reduced order average model are Eqs. (2.1)-(2.4), where N_{SM} is the number of SMs in the arm and n the number of SM capacitors being inserted.

$$v_{arm} = m\, v_{C_\Sigma} \tag{2.1}$$

$$i_{Ceq} = m\, i_{arm} \tag{2.2}$$

$$m = \frac{n}{N_{SM}} \tag{2.3}$$

$$Ceq = \frac{C_{SM}}{N_{SM}} \tag{2.4}$$

Additionally, the charging/discharging dynamics of the equivalent capacitor Ceq can be calculated thanks to Eq. (2.5).

$$\frac{d}{dt} v_{C_\Sigma} = \frac{1}{Ceq} \cdot (m\, i_{arm}) \tag{2.5}$$

This model is used for describing the converter operation under normal operation, i.e. each SM in the arm is in insertion or bypass state. Both states are achieved in the HB-SM by turning ON one of the SM transistors as seen in Figure 2.2.

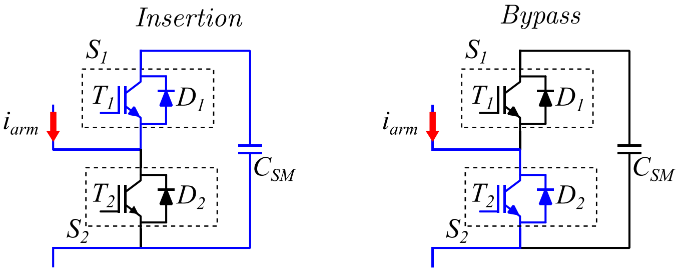


Figure 2.2. HB-SM states

As previously seen in Figure 2.1, during normal operation the arm current flows through the equivalent voltage source of the model, charging or discharging the equivalent capacitor Ceq. Depending on the polarity of the arm current, one of the different semiconductor devices present in the HB-SM will be active. It can also be seen from Eq. (2.1), that the arm voltage is proportional to the equivalent capacitor voltage v_{C_Σ} affected by the modulation index m, which is calculated by the converter control algorithm. Table 2.1 makes a comparison of the characteristics of a real arm and the reduced order average model. In Table 2.1, u represents the insertion or bypass state of the i^{th} HB-SM.

Current Polarity	Real Arm		Model
	Conducting Device	Arm Voltage	Arm Voltage
$i_{arm} < 0$	D_2 or T_1	$\sum_{i=1}^{N_{SM}} v_{C_{SM_i}}(t) u_i(t)$	$m\, v_{C_\Sigma}$
$i_{arm} > 0$	D_1 or T_2		

Table 2.1 Comparison between real arm and reduced average arm model

2.2.2. Type 4 model – Semi-analytic detailed model

Type 5 models developed in the previous section are well suited for analyzing the converter operation when performing system level studies. However, this type of model does not provide much information about component level behavior. Thus, detailed models are implemented for a more comprehensive component-level analysis.

Given the large amount of SMs in a High Voltage structure such as a MMC, an exact model describing IGBT-diode dynamics is prohibited [189]. However, semi-analytic detailed models reported in the literature [195], [198], can address SM-level dynamics such as semiconductor losses and the charging dynamics of the storage capacitor without compromising simulation time and performance.

The model presented in [198] utilizes an equivalent circuit and a set of equations to describe the dynamics of each SM. Figure 2.3 depicts this type of model. When comparing this model to the reduced order average model seen in the previous section, the equivalent capacitor is replaced by a set of equations that determine the relations between an arm and each individual SM.

The set of equations required for the model are defined as proposed in [198]. For an i^{th} SM in the stack, the capacitor voltage is given by the solution of Eq. (2.6). Where u_i is a binary signal representing the SM control signal. When $u_i = 1$ the SM is in the insertion state and when $u_i = 0$ the SM is in the bypass state, as previously seen in Figure 2.2.

The equivalent voltage source on Figure 2.3 is the sum of all the capacitor voltages of the inserted SMs as described in Eq. (2.7).

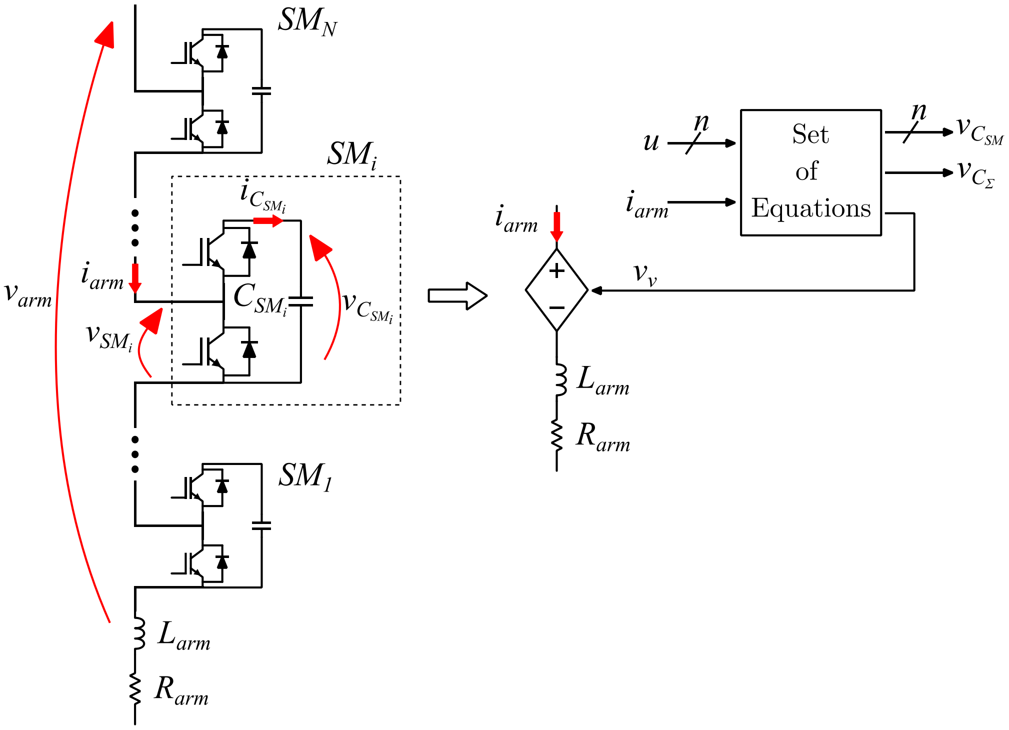


Figure 2.3. Semi-analytic detailed model of a SM arm [198]

$$\frac{dv_{C_{SM_i}}(t)}{dt} = \frac{1}{C_{SM}}\left(u_i \,.\, i_{arm}(t)\right) \tag{2.6}$$

$$v_v(t) = \sum_{i=1}^{N_{SM}} \left(v_{C_{SM_i}}(t) \,.\, u_i(t)\right) \tag{2.7}$$

Finally, the sum of all capacitor voltages in the stack is:

$$v_{C_\Sigma}(t) = \sum_{i=1}^{N_{SM}} v_{C_{SM_i}}(t) \tag{2.8}$$

In Eq. (2.8), $v_{C_\Sigma}(t)$ is the voltage on the equivalent arm capacitor of the reduced order average model under the assumption of all SMs having the same capacitor value (see Appendix A.1 for more details on the average model deduction).

2.2.3. Averaged – Detailed model

The resulting averaged-detailed model employed for this study can be seen in Figure 2.4. It uses a reduced order average model for 2 phases of the MMC topology. Both upper and lower arms follow the same principle for its modelling.

The remaining phase was modelled using a semi-analytic detailed model, which allows to obtain more information about the electrical behavior of the submodules of the remaining phase. It is worth mentioning that both upper and lower arms in the remaining phase were modelled in the same way.

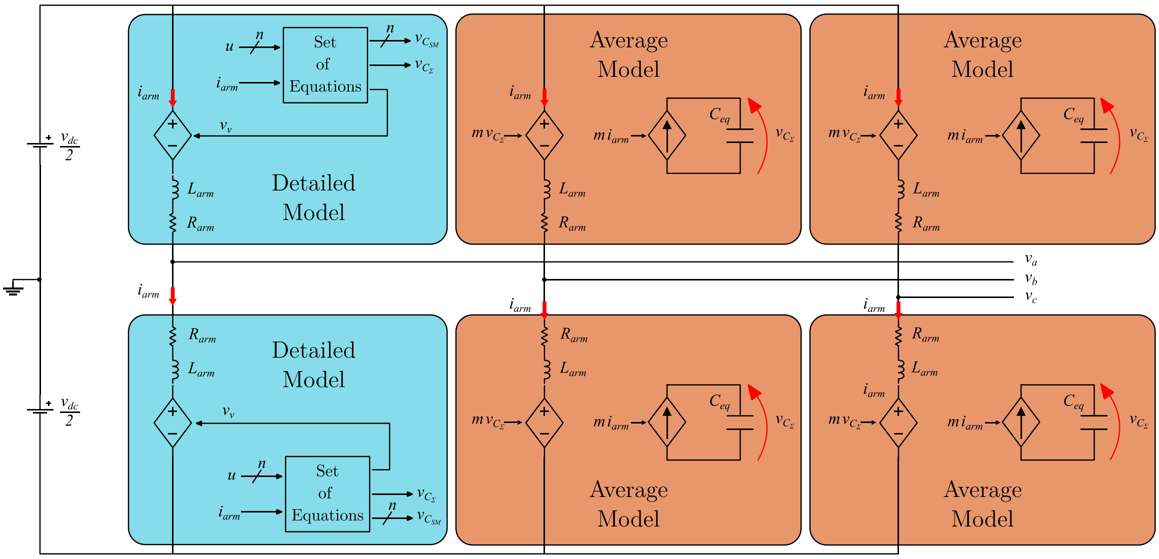


Figure 2.4. Averaged – Detailed model

2.3. Mathematical description

The fundamental laws describing the behavior of a phase of the averaged-detailed model (Figure 2.5) can be seen in Eq. (2.9). In this expression, the u and l superscripts represent, respectively, the upper and lower arms.

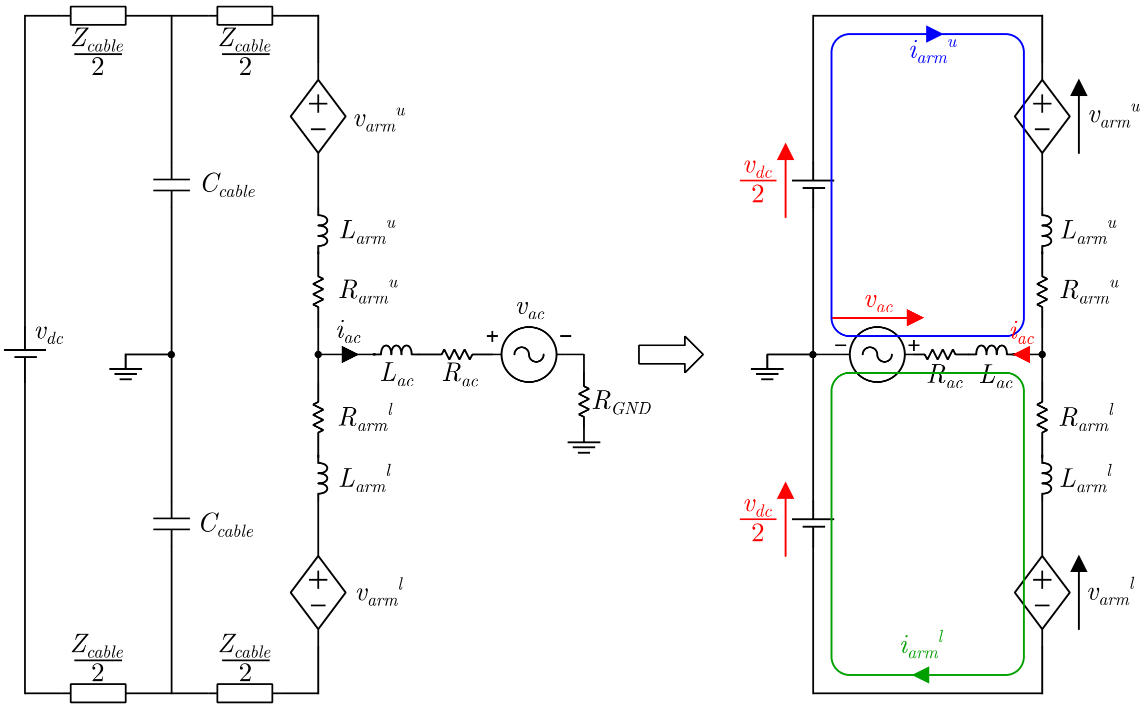


Figure 2.5. Mesh analysis of a phase of the averaged-detailed model

$$\begin{bmatrix} L_{arm}{}^{u}+L_{ac} & -L_{ac} \\ -L_{ac} & L_{arm}{}^{l}+L_{ac}\end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_{arm}{}^{u}(t)\\ i_{arm}{}^{l}(t)\end{bmatrix} = \begin{bmatrix}\frac{v_{dc}}{2}-v_{ac}(t)\\ \frac{v_{dc}}{2}+v_{ac}(t)\end{bmatrix} - \begin{bmatrix}1&0\\0&1\end{bmatrix}\begin{bmatrix}v_{arm}{}^{u}(t)\\ v_{arm}{}^{l}(t)\end{bmatrix} + \begin{bmatrix}-R_{arm}{}^{u}-R_{ac} & R_{ac}\\ R_{ac} & -R_{arm}{}^{l}-R_{ac}\end{bmatrix}\begin{bmatrix}i_{arm}{}^{u}(t)\\ i_{arm}{}^{l}(t)\end{bmatrix} \tag{2.9}$$

If the phase currents of the MMC are balanced, there will be no current flowing through the ground resistor R_{GND} of Figure 2.5. Thus, it can be removed from a single-phase schematic. Moreover, if the voltages across the upper and lower C_{cable} are unbalanced, a homopolar current will appear and will circulate across R_{GND} and will simultaneously discharge the C_{cable} with the highest voltage and charge the C_{cable} with the lowest voltage. Hence, both voltages will naturally reach an equilibrium. Therefore, the single-phase model can be simplified as seen on the right-hand side of Figure 2.5.

It is worth noting that the arm voltages $v_{arm}(t)$ in Eq. (2.9) can take different forms depending on the type of model employed for each phase. For the phases employing the reduced order average model, $v_{arm} = m\, v_{C_\Sigma}$ as expressed in Eq. (2.1), whereas in the phase using the semi-analytic detailed model v_{arm} will take the form of $v_v(t)$ expressed in Eq. (2.7).

Up until this point, the different equations describing the dynamics of an MMC arm were described. However, as it can be shown by Eq. (2.9), there is a strong coupling between the outputs of the system $i_{arm}{}^{u}$ and $i_{arm}{}^{l}$. Moreover, it is a common practice in the literature to separate the AC and DC components for simplifying the control strategy [189], [195], [199]–[201]. In order to accomplish this decoupling, the arm voltages and currents of Eq. (2.9) are expressed in a new coordinate system thanks to a sigma-delta ($\Sigma\Delta$) transformation that represents the sum and differences of the evaluated quantities of the same phase as seen on Eqs. (2.10) and (2.11).

$$\begin{bmatrix} i_\Sigma(t) \\ i_\Delta(t) \end{bmatrix} = \begin{bmatrix} 0.5 & 0.5 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} i_{arm}{}^u(t) \\ i_{arm}{}^l(t) \end{bmatrix} \tag{2.10}$$

$$\begin{bmatrix} v_\Sigma(t) \\ v_\Delta(t) \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ -0.5 & 0.5 \end{bmatrix} \begin{bmatrix} v_{arm}{}^u(t) \\ v_{arm}{}^l(t) \end{bmatrix} \tag{2.11}$$

The inverse transformations are:

$$\begin{bmatrix} i_{arm}{}^u(t) \\ i_{arm}{}^l(t) \end{bmatrix} = \begin{bmatrix} 1 & 0.5 \\ 1 & -0.5 \end{bmatrix} \begin{bmatrix} i_\Sigma(t) \\ i_\Delta(t) \end{bmatrix} \tag{2.12}$$

$$\begin{bmatrix} v_{arm}{}^u(t) \\ v_{arm}{}^l(t) \end{bmatrix} = \begin{bmatrix} 0.5 & -1 \\ 0.5 & 1 \end{bmatrix} \begin{bmatrix} v_\Sigma(t) \\ v_\Delta(t) \end{bmatrix} \tag{2.13}$$

By careful inspection of Eq. (2.10) and Figure 2.5, it can be inferred that the difference of arm currents i_Δ is equivalent to the line current i_{ac}. Additionally, the sum of the arm currents of a same phase i_Σ is in part given by the DC current i_{dc} coming from the DC network. This current will be denoted $i_{\Sigma_{dc}}$ ($i_{\Sigma_{dc}} = i_{dc}/3$). The other component of i_Σ comes from the circulating currents i_{circ}, internal to the MMC converter (see Eq. (2.14)). This component represents the current exchanges between the phases of the converter. A more comprehensible illustration of the currents i_Δ and i_Σ can be seen in Figure 2.6.

$$i_\Sigma{}^i = i_{\Sigma_{dc}}{}^i + i_{circ}{}^i \text{ with } i = a, b, c \tag{2.14}$$

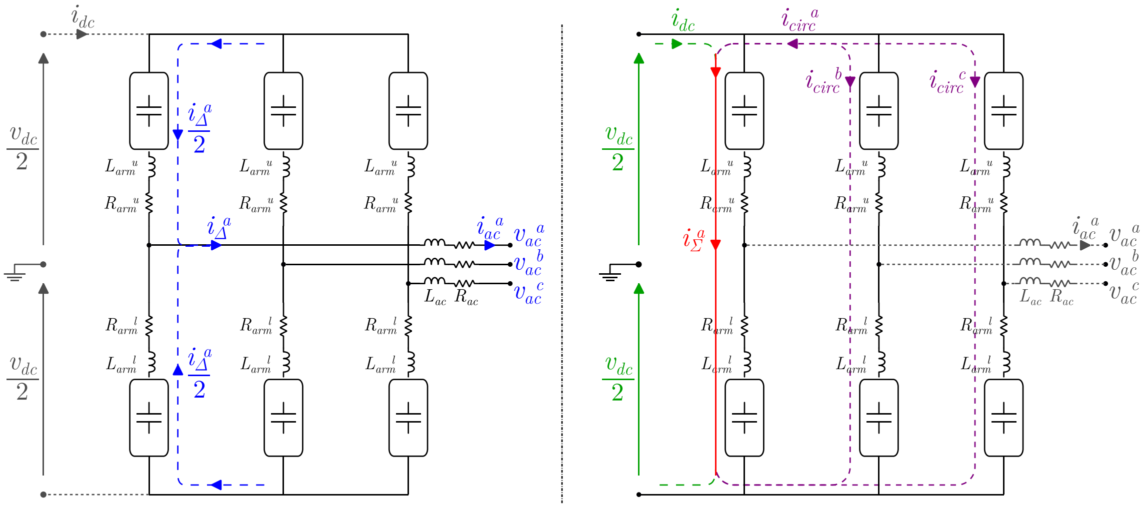


Figure 2.6. Interpretation of currents i_Δ and i_Σ for one MMC phase

After applying the base transformations of Eqs. (2.10) and (2.11) to Eq. (2.9), the behavior of one MMC phase can be described as:

$$\frac{d}{dt}\begin{bmatrix} i_{\Sigma}(t) \\ i_{\Delta}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R_{arm}{}^{u,l}}{L_{arm}{}^{u,l}} & 0 \\ 0 & -\frac{R_{eq}}{L_{eq}} \end{bmatrix}\begin{bmatrix} i_{\Sigma}(t) \\ i_{\Delta}(t) \end{bmatrix} + \begin{bmatrix} -\frac{1}{2L_{arm}{}^{u,l}} & 0 \\ 0 & \frac{1}{L_{eq}} \end{bmatrix}\begin{bmatrix} v_{\Sigma}(t) \\ v_{\Delta}(t) \end{bmatrix} + \begin{bmatrix} \frac{v_{dc}}{2L_{arm}{}^{u,l}} \\ -\frac{v_{ac}(t)}{L_{eq}} \end{bmatrix} \tag{2.15}$$

Where the equivalent resistance R_{eq} and equivalent inductance L_{eq} are given by:

$$R_{eq} = \frac{R_{arm}{}^{u,l}}{2} + R_{ac} \tag{2.16}$$

$$L_{eq} = \frac{L_{arm}{}^{u,l}}{2} + L_{ac} \tag{2.17}$$

In order to design the controller of the converter it is necessary to use the reduced order average model and to consider the evolution of the voltage on the equivalent arm capacitor $v_{C_{\Sigma}}$. Thus, from Eq. (2.5) and Eq. (2.10), the Eq. (2.18) can be obtained.

$$\frac{d}{dt}\begin{bmatrix} v_{C_{\Sigma}}{}^{u}(t) \\ v_{C_{\Sigma}}{}^{l}(t) \end{bmatrix} = \frac{1}{Ceq^{u,l}}\begin{bmatrix} m^{u} & \frac{m^{u}}{2} \\ m^{l} & -\frac{m^{l}}{2} \end{bmatrix}\begin{bmatrix} i_{\Sigma}(t) \\ i_{\Delta}(t) \end{bmatrix} \tag{2.18}$$

Finally, the relation between the equivalent capacitor voltage $v_{C_{\Sigma}}$ and the $\Sigma\Delta$ transformations of the arm voltages can be obtained with Eq. (2.19).

$$\begin{bmatrix} v_{\Sigma}(t) \\ v_{\Delta}(t) \end{bmatrix} = \begin{bmatrix} m^{u}(t) & m^{l}(t) \\ -\frac{m^{u}(t)}{2} & \frac{m^{l}(t)}{2} \end{bmatrix}\begin{bmatrix} v_{C_{\Sigma}}{}^{u}(t) \\ v_{C_{\Sigma}}{}^{l}(t) \end{bmatrix} \tag{2.19}$$

Eq. (2.15) demonstrates that a decoupling can be achieved by performing the $\Sigma\Delta$ transformations. Moreover, the dynamics of the Σ and Δ components of the currents are independent. Hence, an equivalent circuit seen on Figure 2.7 can be used for describing the functioning of one MMC phase. Figure 2.7 also illustrates that the AC and DC currents can be independently regulated inside an MMC contrarily to VSC standards [201]. However, a coupling between AC and DC networks is still present and can be evidenced in the dynamics of the MMC capacitors seen on Eq. (2.18) and Figure 2.7.

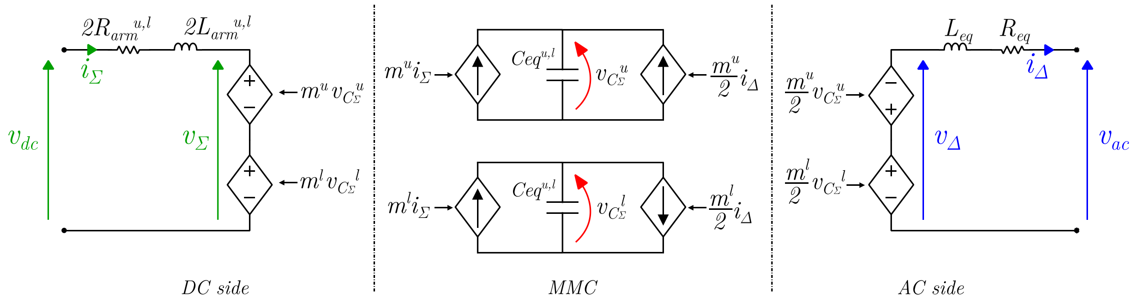


Figure 2.7. One MMC phase equivalent circuit in the reference frame $\Sigma\Delta$

As seen on Figure 2.7, the AC line current i_Δ can be controlled by imposing a voltage difference between the phase voltage v_{ac} and the alternative voltage source v_Δ. On the other hand, the current i_Σ can be controlled by imposing a voltage difference between the DC grid voltage v_{dc} and v_Σ. Consequently, a power difference between both DC and AC entities will result in a variation of the stored energy inside the capacitors of the MMC.

Furthermore, the equivalent capacitors are being permanently charged and discharged. This action is performed by the modulated currents $m^{u,l} i_\Delta$ and $m^{u,l} i_\Sigma$. Considering Eqs. (2.1) and (2.11), it can be demonstrated that the modulation indexes $m^{u,l}$ have alternative and continuous components. Hence the modulated currents $m^{u,l} i_\Delta$ and $m^{u,l} i_\Sigma$ are themselves a sum of products of continuous components (DC-DC), alternative components (AC-AC) and even of mixed continuous-alternative components (AC-DC). The continuous and alternative components of the modulated currents have an impact on the mean voltage across the equivalent capacitors. The mixed continuous-alternative component has an influence on the voltage swings experienced by the equivalent capacitors.

The proper functioning of the MMC is based on the fact that the equivalent capacitor voltages must be controlled to stay within acceptable limits. This allows the converter to stock a sufficient amount of internal energy in its arms and allows each arm to generate the desired voltage outputs for normal operation.

Likewise, the MMC can perform DC to AC conversion and vice versa by means of the storage capacitors it has in its arms. The energy balance must be maintained at all times for steady-state operation. The following paragraph gives a more detailed insight of converter operation at steady-state.

2.4. Steady-state analysis

2.4.1. Calculation of arm currents and voltages

The steady-state behavior can be deduced from the dynamic Eqs. (2.15) and (2.18) developed in section 2.3. From the Eqs (2.14), (2.15) as well as from Figure 2.6, it has been shown that i_Σ partially corresponds to a DC current coming from the DC grid into the leg of the converter (ignoring the circulating current i_{circ}). If the phases of the converter are balanced, this value corresponds to the DC grid current divided by the number of phases of the converter (in this case, the MMC has three phases). The DC components of i_Σ in steady-state can be obtained from Eq. (2.15) considering that $(\frac{d}{dt} = 0)$:

$$i_\Sigma(t) = \frac{v_{dc} - v_\Sigma(t)}{2{R_{arm}}^{u,l}} \simeq \frac{i_{dc}}{3} = i_{\Sigma_{dc}} \tag{2.20}$$

Since the arm resistances have small values, as losses need to be reduced, there is only need of a small voltage difference to impose the DC currents. Hence, in steady-state the value of v_Σ is quite similar to the DC grid voltage.

$$v_\Sigma(\mathrm{t}) \simeq v_{dc} \tag{2.21}$$

It was seen in Figure 2.7 that the power flow on the AC side can be controlled by imposing a voltage difference between the AC grid voltage v_{ac} and the alternative modulated voltage source v_{Δ}.

Additionally, MMCs composed of HB-SMs are not able to generate arm voltages bigger than pole-to-pole voltages. This is mainly due to the fact that the HB-SMs can't produce negative voltages. Then the modulation factor K can be defined as the ratio of the peak voltage of the AC grid and the DC grid voltage as seen in Eq. (2.22). This implies that this factor will be comprised between 0 and 1.

$$K = \frac{\widehat{V_{ac}}}{\left(\frac{v_{dc}}{2}\right)} \tag{2.22}$$

Normally the K factor should be fixed at the highest possible value. However, a small margin must be kept for dynamic purposes. Considering a sinusoidal modulation [17], and using the peak AC voltage as a reference, the AC variables can be written as:

$$v_{\Delta}(t) = K\frac{v_{dc}}{2}\sin(\omega t) = \widehat{V_{ac}}\sin(\omega t) \tag{2.23}$$

$$i_{\Delta}(t) = \widehat{I_{ac}}\sin(\omega t - \phi) \tag{2.24}$$

Applying the ΣΔ transformations from Eqs. (2.10) and (2.11) to Eqs. (2.20), (2.21), (2.23) and (2.24) yields the current and voltage expressions in steady state:

$$i_{arm}{}^{u}(t) = \frac{i_{dc}}{3} + \frac{\widehat{I_{ac}}}{2}\sin(\omega t - \phi) \tag{2.25}$$

$$i_{arm}{}^{l}(t) = \frac{i_{dc}}{3} - \frac{\widehat{I_{ac}}}{2}\sin(\omega t - \phi) \tag{2.26}$$

$$v_{arm}{}^{u}(t) = \frac{v_{dc}}{2} - \widehat{V_{ac}}\sin(\omega t) \tag{2.27}$$

$$v_{arm}{}^{l}(t) = \frac{v_{dc}}{2} + \widehat{V_{ac}}\sin(\omega t) \tag{2.28}$$

2.4.2. Study of capacitor dynamics

The expression depicting the dynamics of the equivalent capacitor of an arm (Eq. (2.5)) with the reduced order average model will be used as the base for pursuing this section. Additionally, the energy stored inside this element must be considered:

$$W_{arm}{}^{u,l}(t) = \frac{1}{2}Ceq^{u,l}\left(v_{C_{\Sigma}}{}^{u,l}(t)\right)^{2} \tag{2.29}$$

It is also known that the evolution of this energy depends on the power exchange in each arm. This power exchange $p_{arm}{}^{u,l}(t)$ is the result of the product of the arm voltage and arm current as depicted in Eq. (2.30).

$$\begin{bmatrix} p_{arm}{}^{u}(t) \\ p_{arm}{}^{l}(t) \end{bmatrix} = \begin{bmatrix} i_{arm}{}^{u}(t) & 0 \\ 0 & i_{arm}{}^{l}(t) \end{bmatrix} \begin{bmatrix} v_{arm}{}^{u}(t) \\ v_{arm}{}^{l}(t) \end{bmatrix} \tag{2.30}$$

Replacing Eqs. (2.25)-(2.28) in Eq. (2.30) yields:

$$p_{arm}{}^{u}(t) = \frac{v_{dc}i_{dc}}{6} - \frac{\widehat{V_{ac}}\widehat{I_{ac}}\cos(\phi)}{4} + \frac{v_{dc}\widehat{I_{ac}}\sin(\omega t - \phi)}{4} - \frac{\widehat{V_{ac}}i_{dc}\sin(\omega t)}{3} + \frac{\widehat{V_{ac}}\widehat{I_{ac}}\cos(2\omega t - \phi)}{4} \tag{2.31}$$

$$p_{arm}{}^{l}(t) = \frac{v_{dc}i_{dc}}{6} - \frac{\widehat{V_{ac}}\widehat{I_{ac}}\cos(\phi)}{4} - \frac{v_{dc}\widehat{I_{ac}}\sin(\omega t - \phi)}{4} + \frac{\widehat{V_{ac}}i_{dc}\sin(\omega t)}{3} + \frac{\widehat{V_{ac}}\widehat{I_{ac}}\cos(2\omega t - \phi)}{4} \tag{2.32}$$

The first two terms of Eqs. (2.31) and (2.32) represent the power transmitted by the arms, coming from the DC grid P_{dc} and from the AC grid P_{ac}. The remaining terms represent the inherent power swings inside an arm. These fluctuations are responsible for the charging and discharging of the capacitors. By careful inspection of Eqs. (2.31) and (2.32) a term introducing oscillations at two times the line frequency can be identified. Consequently, the energy dynamics can be obtained by integrating Eqs. (2.31) and (2.32):

$$W_{arm}{}^{u}(t) = \int_{t_0}^{t} p_{arm}{}^{u}(t)dt + W_{arm_0}{}^{u} = \int_{t_0}^{t} \frac{dW_{arm}{}^{u}(t)}{dt} + W_{arm_0}{}^{u} \tag{2.33}$$

$$W_{arm}{}^{l}(t) = \int_{t_0}^{t} p_{arm}{}^{l}(t)dt + W_{arm_0}{}^{l} = \int_{t_0}^{t} \frac{dW_{arm}{}^{l}(t)}{dt} + W_{arm_0}{}^{l} \tag{2.34}$$

In Eqs. (2.33) and (2.34) $W_{arm_0}{}^{u,l}$ symbolizes the initial energy stocked inside the arms. Another important aspect to consider is the average power inside an arm:

$$p_{arm}{}^{u,l}(t) = \overline{\frac{dW_{arm}{}^{u,l}(t)}{dt}} = \frac{v_{dc}i_{dc}}{6} - \frac{\widehat{V_{ac}}\widehat{I_{ac}}\cos(\phi)}{4} = \frac{P_{dc}}{6} - \frac{P_{ac}}{6} \tag{2.35}$$

The analysis of Eqs. (2.33), (2.34) and (2.35) helps to understand that in order to have a constant amount of energy inside an arm $W_{arm_0}{}^{u,l}$, the equilibrium between AC and DC power must be guaranteed. Otherwise, the capacitors inside the converter will attain energy levels that are not compatible with the nominal operation of the converter, thus losing the station due to energy imbalance inside the converter.

Finally, the voltage on the equivalent capacitors in steady state must remain controlled to assure a stable energy level inside the converter. The time evolution of this voltage can be obtained by replacing Eqs. (2.33) and (2.34) in Eq. (2.29):

$$v_{C_\Sigma}{}^{u,l}(t) = \sqrt{\frac{2}{Ceq^{u,l}}\left(\int_{t_0}^{t} p_{arm}{}^{u,l}(t)dt + W_{arm_0}{}^{u,l}\right)} \tag{2.36}$$

From (2.36) it can be concluded that an energy variation will have an impact on the voltage $v_{C_\Sigma}{}^{u,l}$, which represents the sum of all the voltages of the SM capacitors of an arm. In any case, this voltage must always be kept below a limit expressed in Eq. (2.37) where $v_{C_{sm}}{}^{max}$ is the maximum admissible voltage on a SM capacitor.

$$v_{C_\Sigma}{}^{u,l}(t) \leq v_{C_{sm}}{}^{max} N_{sm} \tag{2.37}$$

Moreover, the arm voltage $v_{arm}{}^{u,l}$ is a modulated voltage that is proportional to the available equivalent capacitor voltage $v_{C_\Sigma}{}^{u,l}$(See Eq. (2.1)). This means that the arm voltage can't be higher than the voltage across all the inserted SM capacitors. This holds to be true in the particular case where $m = 1$.

$$v_{arm}{}^{u,l} \leq v_{C_\Sigma}{}^{u,l}(t) \tag{2.38}$$

In order to make a synthesis of this paragraph, Figure 2.8 depicts the expected waveforms for an MMC arm in steady state. The superposition of DC and AC components can be clearly distinguished for the arm voltages and currents. Additionally, the equivalent capacitor average value is kept constant as expected from the power balance of Eq. (2.35). Moreover, the oscillation on this voltage is given by the terms on Eqs. (2.31) and (2.32). Finally, the proportionality between the modulation index and the arm voltage can be observed.

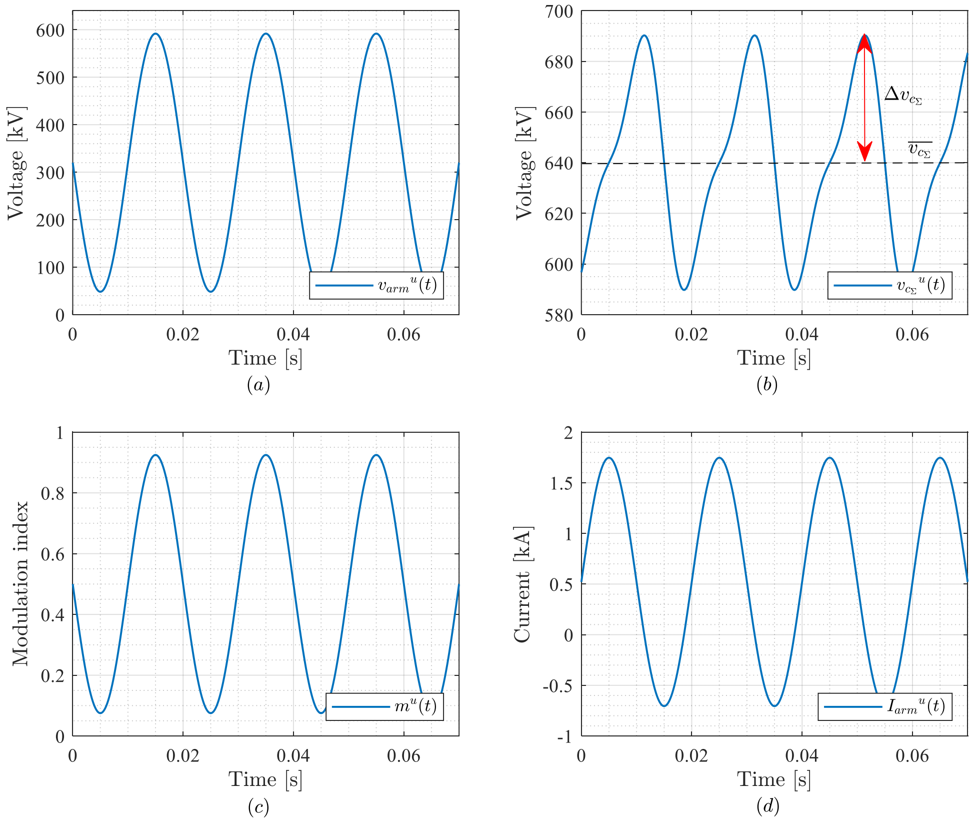


Figure 2.8. Steady-state waveforms of an MMC arm: (a) Arm voltage $v_{arm}{}^u(t)$ (b) Equivalent capacitor voltage $v_{C_\Sigma}{}^u(t)$ (c) Modulation index $m^u(t)$ (d) Arm current $i_{arm}{}^u(t)$

From the steady-state analysis it can be concluded that the DC and AC power exchanges must be meticulously controlled for assuring the correct functioning of the MMC. Thus, the control strategy must fulfill three main objectives [189]:

- Control the DC currents circulation

- Control the AC currents circulation
- Control the converter energy to satisfy Eq. (2.35) on all converter arms, for guarantying a nominal energy ${W_{arm}}_0{}^{u,l}$ in steady state. The nominal energy should be sufficient to have a ${v_{C}}_{\Sigma}{}^{u,l}$ greater than the arm voltage to be generated.

In addition to those objectives, the control must be able to balance the voltage on each of the SM capacitors present in an arm. Therefore, the next section will deal with the control of the MMC topology.

2.5. Modular multilevel converter control

As mentioned in [189], the control of the MMC topology can be divided into two control stages as depicted in Figure 2.9. The first one, otherwise known as high-level control, is dedicated to the control of the converter currents and energies. The second one, otherwise known as low-level control, assures the balancing of the individual SM voltages on each arm.

For the arms modeled employing the reduced order average model, only the first type of control is required. However, for the arms modeled employing the detailed model, high-level and low-level control are necessary for performing the converter simulation.

The high-level control stage needs the measurements of both AC and DC grid voltages and currents, arm currents and arm equivalent capacitor voltages. It outputs the modulation index for each arm. If an average model is used, the control outputs act directly into the model. If a detailed model is used, the arm voltage references are transferred to the low-level control stage that calculates how many SMs per arm must be inserted to achieve the desired arm voltage and decides which ones to insert in order to maintain their voltages inside a specified range. This control stage needs the voltage measurement of all SMs in an arm. This control is referred as Balancing Control Algorithm (BCA). The outputs of this stage are the control signals for each SM [189]. Both control stages will be detailed in the following lines.

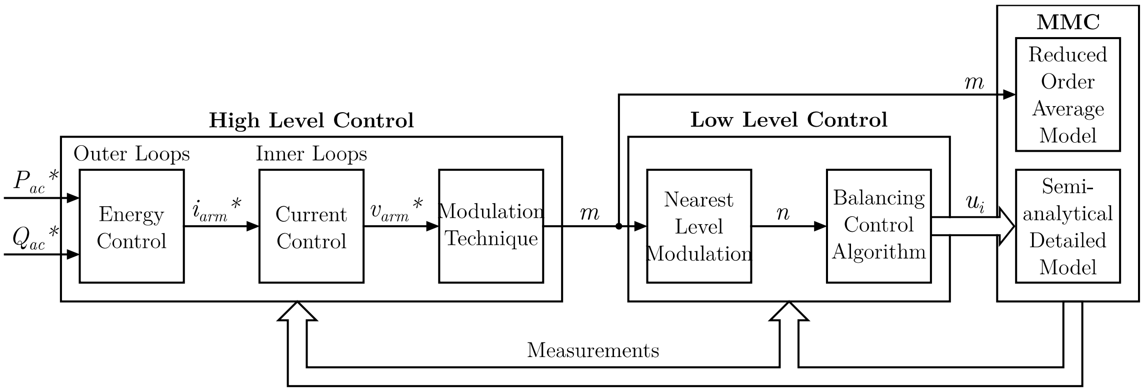


Figure 2.9. Control scheme of a Modular Multilevel Converter

2.5.1. Low level control

As it was previously discussed, the low-level control must ensure that a certain number of SMs is inserted for having a correct arm voltage. Also, this control stage deals with the balancing of the SM capacitor voltages. In order to accomplish both tasks, low level controllers make use of a modulation block and a sorting algorithm known as BCA. The modulation block will address the first topic, whereas the BCA will keep SM-capacitors charged at reasonable levels. Along with an appropriate switching strategy, this control layer will directly send the command signals to all the IGBTs present in the converter to effectively insert or bypass a target SM capacitor.

In the literature numerous modulation techniques are proposed. Among the most popular, are pulse width modulation techniques with its main variants. Phase-Shifted PWM and Level-Shifted PWM are the most popular PWM techniques [202], [203]. Also, vectorial modulation techniques, such as space vector PWM [20], are among the most used in practical applications. Nevertheless, these techniques are hard to deploy in an application such as an HVDC-MMC. The main challenge for the traditional modulating techniques is that they are not well suited for dealing with such high number of stages.

In response to this issue, a particular modulation technique more suited to the MMC application will be considered in this thesis. This technique is known as Nearest Level Modulation (NLM) [204]. This modulation scheme computes the number of SMs to be inserted according to the required arm voltage and the individual voltages on each SM capacitor. The NLM scheme rounds the number of SMs to be inserted to the nearest highest integer as described in Eq. (2.39). This modulation technique requires that the dispersion of SM capacitor voltages remain low.

$$\begin{aligned} n^{u,l}(t) &= \mathrm{round}\left(\frac{{v_{arm}}^{u,l^*}(t)}{\frac{\sum_{i=1}^{N_{SM}} v_{C_{SM_i}}(t)}{N_{SM}}}\right) = \mathrm{round}\left(\frac{{v_{arm}}^{u,l^*}(t)}{{v_{C_\Sigma}}^{u,l}(t)} N_{SM}\right) \\ &= \mathrm{round}\left(m^{u,l}(t) N_{SM}\right) \end{aligned} \tag{2.39}$$

Similarly, there are many available schemes for performing the balancing of SM capacitors in the literature [205]–[208]. It was seen in [205] that the balancing algorithms can be sorted into two different categories. The first one aims to reduce the switching frequency of the power semiconductors, while the other aims to reduce the voltage ripple experienced by the SM capacitor. The later will be considered in this study. This method was presented in [208] and it is known as the average band algorithm. The principle of this method can be seen in Figure 2.10.

The basic operation of this BCA resides in the sorting of a list that contains all the SM capacitor voltages in an arm in a descending direction. This action is performed at each time a SM capacitor voltage reaches a tolerance value measured from the average value of all SM capacitor voltages. Consequently, the choice of the SMs to be inserted $n^{u,l}(t)$ issued from the NLM scheme will be decided based on the arm current polarity. The $n^{u,l}(t)$ highest modules will be inserted in presence of a negative current, as a mean for discharging its capacitors. Contrarily, the $n^{u,l}(t)$ lowest modules will be inserted in the presence of a positive current, as a way of charging its corresponding SM capacitors.

This algorithm ensures that all SM capacitor voltages are kept inside a tolerance band V_{tol}, measured around the average value of all the SM capacitor voltages within an arm as expressed in Eq. (2.40).

$$\frac{\sum_{i=1}^{N_{SM}} v_{C_{SM_i}}}{N_{SM}} - V_{tol} < v_{C_{SM_i}} < \frac{\sum_{i=1}^{N_{SM}} v_{C_{SM_i}}}{N_{SM}} + V_{tol} \quad \textbf{(2.40)}$$

Moreover, Eq. (2.40) can be expressed as a function of the average value of the equivalent capacitor voltage v_{C_Σ} and its voltage ripple ΔV_{C_Σ}:

$$\frac{\left(\overline{v_{C_\Sigma}} - \Delta V_{C_\Sigma}\right)}{N_{SM}} - V_{tol} < v_{C_{SM_i}} < \frac{\left(\overline{v_{C_\Sigma}} + \Delta V_{C_\Sigma}\right)}{N_{SM}} + V_{tol} \quad \textbf{(2.41)}$$

Finally, Eq. (2.41) can be interpreted considering the average SM behavior:

$$(\overline{V_{SM}} - \Delta V_{SM}) - V_{tol} < v_{C_{SM_{avg}}} < (\overline{V_{SM}} + \Delta V_{SM}) + V_{tol} \quad \textbf{(2.42)}$$

The typical waveforms after employing the NLM modulation and the BCA are depicted in Figure 2.11.

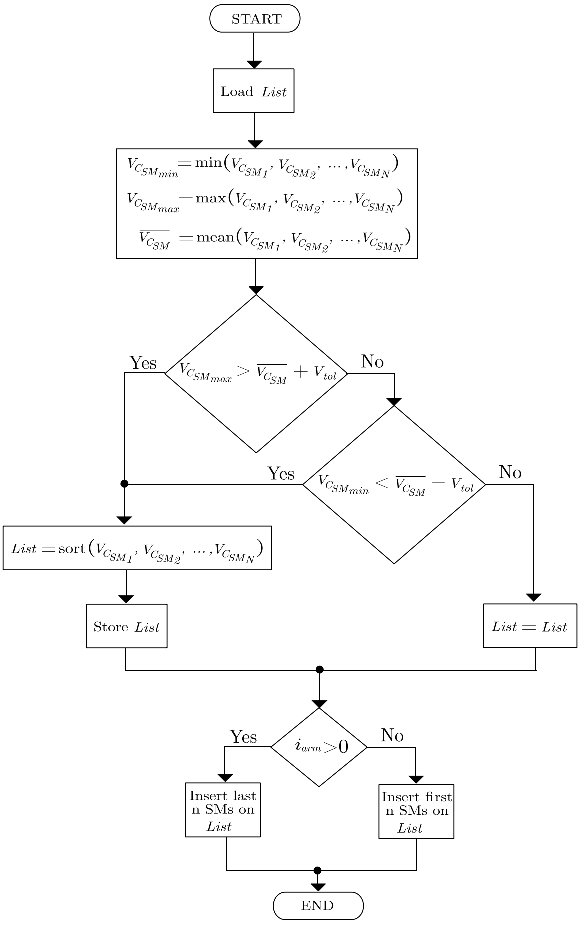


Figure 2.10. Average tolerance band scheme [208]

The choice of the V_{tol} parameter can have a strong impact on the converter. On the one hand, if this value is too low the SM capacitor voltages will be more prone to reach the tolerance band limits, thus incurring in more switching events, which can lead to an increase of the switching losses experienced by the semiconductors. On the other hand, if the tolerance voltage is set too high, there would be a need to increase the value of the capacitor in order to reduce the voltage ripple and keep the SM capacitor voltages below the maximal SM voltage rating.

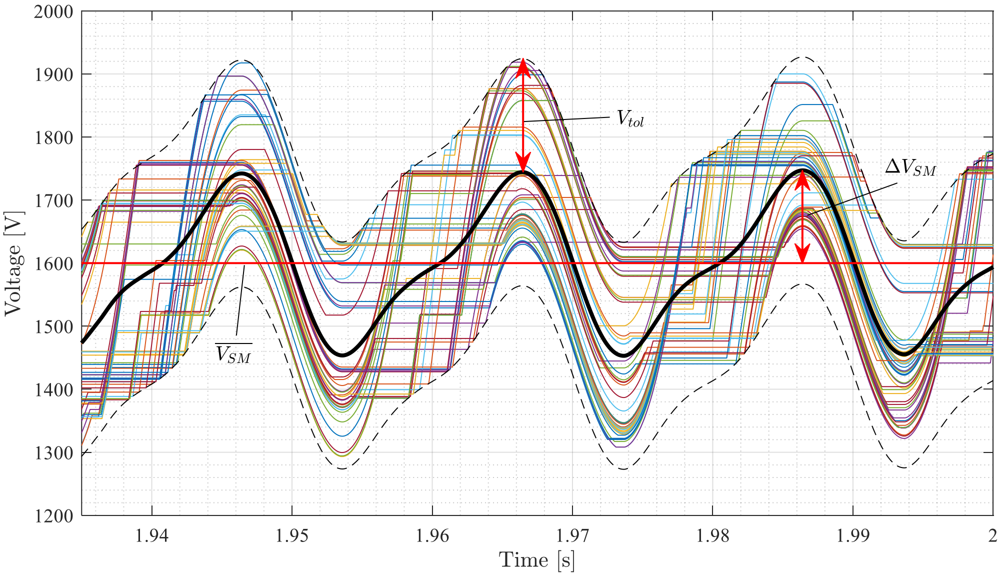


Figure 2.11. SM capacitor voltages in an MMC arm

2.5.2. High level control

The high-level control scheme can be depicted in Figure 2.12. The control strategy is performed employing the ΣΔ transformations, previously described in section 2.3, allowing the successful decoupling of AC and DC powers. As it was previously established, the goals of the high-level control are to regulate the AC and DC currents and the energy in the MMC arms. In order to achieve these goals, nested control loops are used.

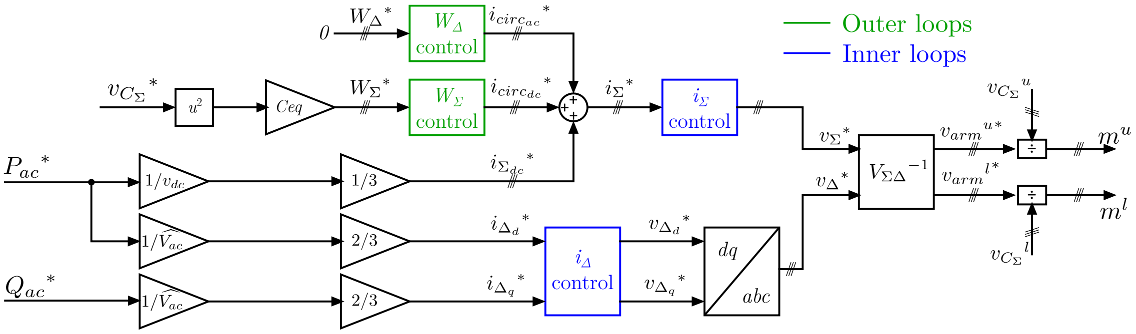


Figure 2.12. High-level control scheme

The outermost loops deal with the regulation of the total energy inside the MMC W_{MMC} and its distribution along its legs and arms (W_Σ and W_Δ). Complementarily, the innermost regulation loops deal with the control of AC and DC currents.

The outer control layer is much slower compared to the innermost control layers. Hence, the outputs of the external control layers compute the references for the inner control loops. As the inner loops have much faster dynamics, they appear as a unitary gain for the outer controllers as depicted in Figure 2.13. In order to achieve this performance, the time constants of the control loops must allow different dynamics. It has been verified that imposing response times at least three times faster for the inner controllers yield satisfactory results.

$$\tau_{inner} \ll \tau_{outer} \tag{2.43}$$

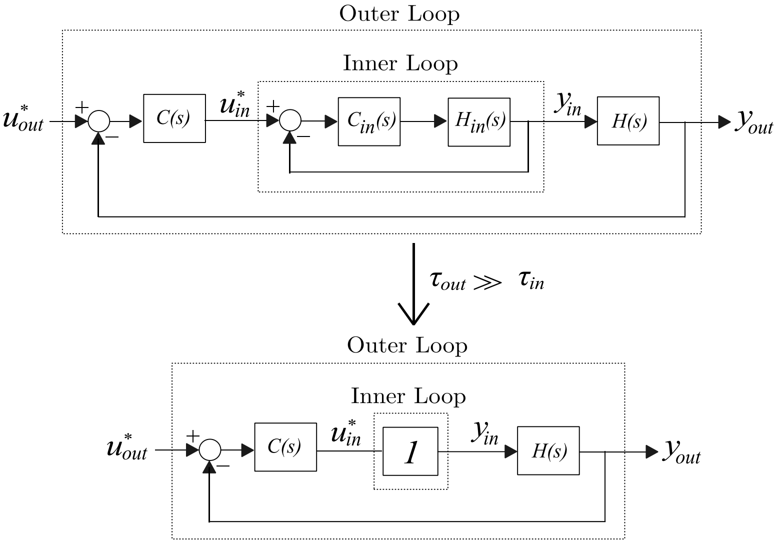


Figure 2.13. Control layers under the assumption that $\tau_{inner} \ll \tau_{outer}$

The final output of the high-level control is the modulation index (m^u, m^l) to be applied to each arm. For the reduced-order average models, this output will be passed directly to the arm models. However, the semi-analytic detailed models will require the low-level controller to treat the modulation index issued from the high-level control and process it to send the gate signals to all the semiconductors present in the MMC structure.

It is also worth mentioning that the regulation of the control variables will be possible by using proportional-integral (PI) controllers. The transfer function of these controllers can be seen in Eq. (2.44).

$$C(s) = K_p\left(1 + \frac{1}{\tau_i\, s}\right) \tag{2.44}$$

2.5.2.1. Outer control loops

It was already evidenced in Eq. (2.35) that the MMC behaves as a mean for transforming AC to DC power. Additionally, it was explained that any unbalances between DC and AC power will result in an energy swing inside the converter as described in Eq. (2.45).

$$\overline{\frac{dW_{MMC}(t)}{dt}} = P_{dc} - P_{ac} = \Delta P_{MMC} \tag{2.45}$$

In this study, the AC grid imposes fixed power references to the MMC controller. This is normally done in real applications since TSOs set the references for the overlaying AC grids. Consequently, the DC power should perform the regulation of the energy by means of acting on the currents i_{Σ}. However, it is also possible to regulate any energy unbalances through the adjustment of the AC power (currents i_{Δ}) and fixing the DC power reference [199]. Thus, a coefficient α can be introduced as a way to distribute the regulation of energy unbalances between the AC and DC power [195]:

$$P_{dc} = {P_{MMC}}^{*} + \alpha \Delta P_{MMC} \tag{2.46}$$

$$P_{ac} = {P_{MMC}}^{*} + (1 - \alpha) \Delta P_{MMC} \tag{2.47}$$

Where ${P_{MMC}}^{*}$ represents the operating point of the converter.

As mentioned previously, it is a common practice that TSOs set the references for AC grids. Consequently, all the power disparities will be dealt by acting on the DC grid. This means that the coefficient $\alpha = 1$ in Eqs. (2.46) and (2.47). Thus, the control of the converter will aim to not disturb the AC grid and make all adjustments by changing the DC power reference, as a way to deal with the variations of the converter internal energy.

Additionally, the energy inside the arms of the converter is proportional to the squared voltage of the equivalent capacitor voltage ${v_{C_{\Sigma}}}^{u,l}(t)$. As this voltage is subjected to line frequency and twice the line frequency harmonics, a filter must be implemented before applying the energy controllers. Similar to the nested control loops strategy, the effectiveness of the filtering for energy control resides on the assumption that the low-pass filter has a much smaller time constant τ_{LPF} than the closed loop response of the energy controllers $\tau_{W_{CL}}$ as seen on Eq. (2.48).

$$\tau_{LPF} \ll \tau_{W_{CL}} \tag{2.48}$$

It is also known that the goal of the outer loops is to control the energy balance between the phases and arms of the converter. In this regard, two controllers will be employed.

The first one assures a horizontal balancing inside the converter. This means that all the phases of the converter will share the same energy W_{Σ}. This energy corresponds to the sum of the energies of the upper and lower arms belonging to the same phase. Evidently, the sum of all the energies W_{Σ} in all the phases of the converter amounts to the total energy of the MMC W_{MMC}.

The second controller assures the vertical balance inside the converter. This means that the second controller will act on the balancing of the arms corresponding to a same phase. This differential energy W_{Δ} corresponds to the difference between the upper and lower arm energies.

The sum and difference energies for a single converter phase can be expressed in the following way:

$$\begin{bmatrix} W_{\Sigma}(t) \\ W_{\Delta}(t) \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} W_{arm}{}^{u}(t) \\ W_{arm}{}^{l}(t) \end{bmatrix} = \frac{1}{2}\, Ceq^{u,l} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} \left(v_{C_{\Sigma}}{}^{u}(t)\right)^2 \\ \left(v_{C_{\Sigma}}{}^{l}(t)\right)^2 \end{bmatrix} \tag{2.49}$$

The main mechanism for controlling W_{Σ} and W_{Δ} is the use of the circulating currents previously evoked in Eq. (2.14). The circulating currents do not have an impact on the DC or AC grids if Eq. (2.50) is verified.

$$i_{circ_a}(t) + i_{circ_b}(t) + i_{circ_c}(t) = 0 \tag{2.50}$$

Moreover, the circulating currents in each phase can have DC and AC components as seen on Figure 2.12 and described in Eq. (2.51):

$$i_{circ}(t) = i_{circ_{dc}}(t) + i_{circ_{ac}}(t) = i_{circ_{dc}}(t) + \widehat{I_{circ_{ac}}} \sin(\omega t - \psi) \tag{2.51}$$

The DC component $i_{circ_{dc}}$ will be responsible for controlling W_{Σ}. Its main goal will be to have all the phases of the converter share similar amounts of energy. In the case of a three phase MMC, W_{Σ} should be a third of the total converter energy.

Finally, the AC component $i_{circ_{ac}}$ will be employed for controlling the energy difference W_{Δ} for all the phases of the converter. It can easily be concluded that an energy imbalance among the arms corresponding to a same converter phase is undesired. Thus, the reference set for the W_{Δ} controller is 0.

2.5.2.1.1. Energy sum (W_{Σ}) control

By applying the ΣΔ transformations of Eqs. (2.10) and (2.11) to Eq. (2.30) the instant power on a converter phase in the ΣΔ reference frame can be obtained:

$$\frac{dW_{\Sigma}(t)}{dt} = v_{\Sigma}(t) i_{\Sigma}(t) - v_{\Delta}(t) i_{\Delta}(t) \tag{2.52}$$

In Eq. (2.35) the average power inside an arm was illustrated. This expression can also be used for determining the average power sum of a converter phase:

$$\overline{\frac{dW_{\Sigma}(t)}{dt}} = \frac{v_{dc} i_{dc}}{3} - \frac{\widehat{V_{ac}}\widehat{I_{ac}} \cos(\phi)}{2} = \frac{P_{dc}}{3} - \frac{P_{ac}}{3} \tag{2.53}$$

From Eq. (2.53), it can be seen that the regulation of W_{Σ} can be achieved by acting on either DC or AC power. But, as it was explained earlier, P_{ac} will be treated as a fixed reference. Then, all the regulation will be dealt on the DC power. This will prevent any unbalance on the AC quantities [195]. Figure 2.14 presents the control loop of W_{Σ} per phase. The blocks $C(s)$ and $F(s)$ represent the controller and the filter transfer functions.

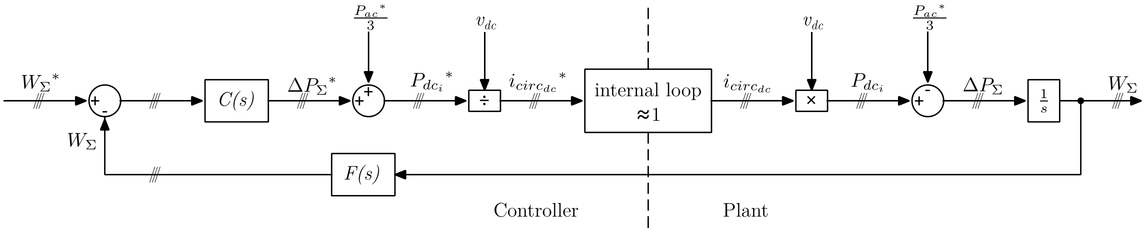


Figure 2.14. Control loop of W_{Σ}

The reference $W_\Sigma{}^*$ is fixed so that each leg of the converter shares an equal amount of energy. The output of the controller is a power variation ΔP_Σ to be added to the AC power reference $P_{ac}{}^*$ corresponding to each phase of the converter, this way the DC power reference $P_{dc}{}^*$ will respond to any perturbations on W_Σ.

The synthesis of the controller seen in Figure 2.14 requires a different interpretation of Eq. (2.52) as the AC power P_{ac} will now be treated as a reference:

$$\frac{dW_\Sigma(t)}{dt} = v_\Sigma(t)i_\Sigma(t) - \frac{P_{ac}{}^*}{3} \tag{2.54}$$

Applying the Laplace transformation yields:

$$W_\Sigma(s) = \frac{1}{s}\left(v_\Sigma(s)i_\Sigma(s) - \frac{P_{ac}{}^*}{3}\right) \tag{2.55}$$

2.5.2.1.2. Energy difference (W_Δ) control

The energy difference between the arms of a same converter leg can be obtained from the instantaneous power expression in Eq. (2.30) as well as applying the ΣΔ transformations in Eqs. (2.10) and (2.11):

$$\frac{dW_\Delta(t)}{dt} = \frac{v_\Sigma(t)i_\Delta(t)}{2} - 2v_\Delta(t)i_\Sigma(t) \tag{2.56}$$

Ideally this energy variation must be null, meaning that upper and lower arm energies have similar energy changes. However, it can be appreciated in Eq. (2.56), that the energy variation between the arms of a same leg corresponds to two products of AC and DC quantities. This means that if the continuous quantities v_Σ and i_Σ are "purely continuous", then there wouldn't be any power variation between upper and lower arms. In real applications, the physical differences between the elements of the circuit could lead to an energy imbalance between arms of a same phase. Thus, there is a strong need for applying this controller.

It was seen in Eq. (2.14), that the sum current i_Σ is composed of a purely DC component $i_{\Sigma_{dc}}$ and a circulation current i_{circ}. Additionally, it was explained in Eq. (2.51) that the circulating currents have both continuous and alternative components.

For the purpose of the regulation of the variations of W_Δ, only the alternative component of the circulating current $i_{circ_{ac}}$ will be utilized. Then, the product $v_\Delta i_\Sigma$, will become a product of two alternative components, which has an average value:

$$\overline{\frac{dW_\Delta(t)}{dt}} = \overline{-2v_\Delta(t)i_{circ_{ac}}(t)} = -\widehat{V_{ac}}\widehat{I_{circ_{ac}}}\cos(\psi) \tag{2.57}$$

The synthesis of the controller is performed by applying the Laplace transformation to Eq. (2.56):

$$W_\Delta(s) = \frac{1}{s}\left(-2v_\Delta(s)i_{circ_{ac}}(s)\right) \tag{2.58}$$

Additionally, this controller must ensure that the condition described in Eq. (2.50) is fulfilled for guaranteeing that i_{circ} will not perturb the AC or DC grids. For achieving this purpose [209] proposes the use of a matrix M_Δ that will be multiplied to the new $i_{circ_{ac}}$ references for calculating new circulating currents i'_{circ} whose sum is equal to 0.

$$\begin{bmatrix} i'_{circ_a} \\ i'_{circ_b} \\ i'_{circ_c} \end{bmatrix} = M_\Delta \begin{bmatrix} i_{circ_a} \\ i_{circ_b} \\ i_{circ_c} \end{bmatrix} = \begin{bmatrix} 1 & -0.5 & -0.5 \\ -0.5 & 1 & -0.5 \\ -0.5 & -0.5 & 1 \end{bmatrix} \begin{bmatrix} i_{circ_a} \\ i_{circ_b} \\ i_{circ_c} \end{bmatrix} \tag{2.59}$$

The overall schema of the W_Δ controller can be seen in Figure 2.15.

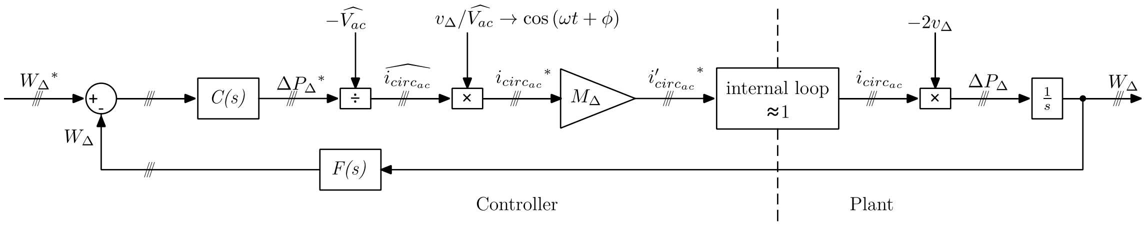


Figure 2.15. Control loop of W_Δ

2.5.2.2. Inner control loops

2.5.2.2.1. DC current control

It was already seen that ΣΔ transformations allow for an independent control of the AC and DC currents. This was clearly depicted in Figure 2.7. If only the DC component of Eq. (2.14) is considered, then the DC current $i_{\Sigma_{dc}}$from Eq. (2.15) can be expressed in the Laplace domain as follows:

$$i_\Sigma(s) = \frac{1}{2L_{arm}{}^{u,l}s + 2R_{arm}{}^{u,l}}(v_{dc} - v_\Sigma(s)) \tag{2.60}$$

Eq. (2.60) is then used for the synthesis of the PI controller to be implemented. Each phase requires a controller for assuring an equivalent current repartition among the different legs of the MMC. The choice of the parameters of the PI controller are based on the pole placement strategy as well as the choice of a reasonable closed-loop time response. The overall structure of the control loop can be seen on Figure 2.16.

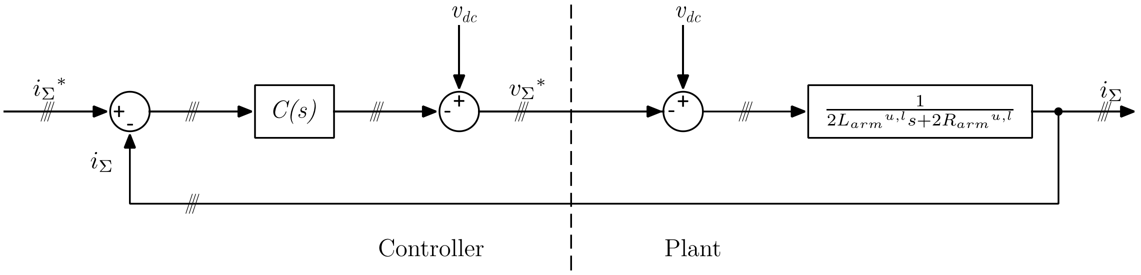


Figure 2.16. Control loop for the DC current i_Σ

2.5.2.2.2. AC current control

In order to control the AC current i_Δ, a Park transformation can be used for changing the three-phase reference frame into a direct-quadrature-zero sequence reference frame. As the three-phase current system is perfectly balanced at steady-state, the zero-sequence component will be null. Hence, a two-coordinate reference frame dq will be employed. This method requires the use of a phase-locked-loop PLL for the identification of the angle and the frequency of the system. The d axis will be aligned with the AC voltage v_{ac}.

This strategy will allow an independent control of the active and reactive power by means of the currents i_d and i_q as expressed in Eqs. (2.61) and (2.62).

$$P_{ac} = v_{\Delta_d} i_{\Delta_d} \tag{2.61}$$

$$Q_{ac} = -v_{\Delta_q} i_{\Delta_q} \tag{2.62}$$

If the Park transformation is applied to the AC current i_Δ in Eq. (2.15) on phases a, b and c, then Eq. (2.63) can be obtained. This expression will then be employed for the synthesis of the AC current controller seen on Figure 2.17.

$$\frac{d}{dt}\begin{bmatrix} i_{\Delta_d} \\ i_{\Delta_q} \end{bmatrix} = \begin{bmatrix} -\frac{R_{eq}}{L_{eq}} & \omega \\ -\omega & -\frac{R_{eq}}{L_{eq}} \end{bmatrix} \begin{bmatrix} i_{\Delta_d} \\ i_{\Delta_q} \end{bmatrix} + \frac{1}{L_{eq}} \begin{bmatrix} v_{\Delta_d} \\ v_{\Delta_q} \end{bmatrix} - \frac{1}{L_{eq}} \begin{bmatrix} v_{ac_d} \\ 0 \end{bmatrix} \tag{2.63}$$

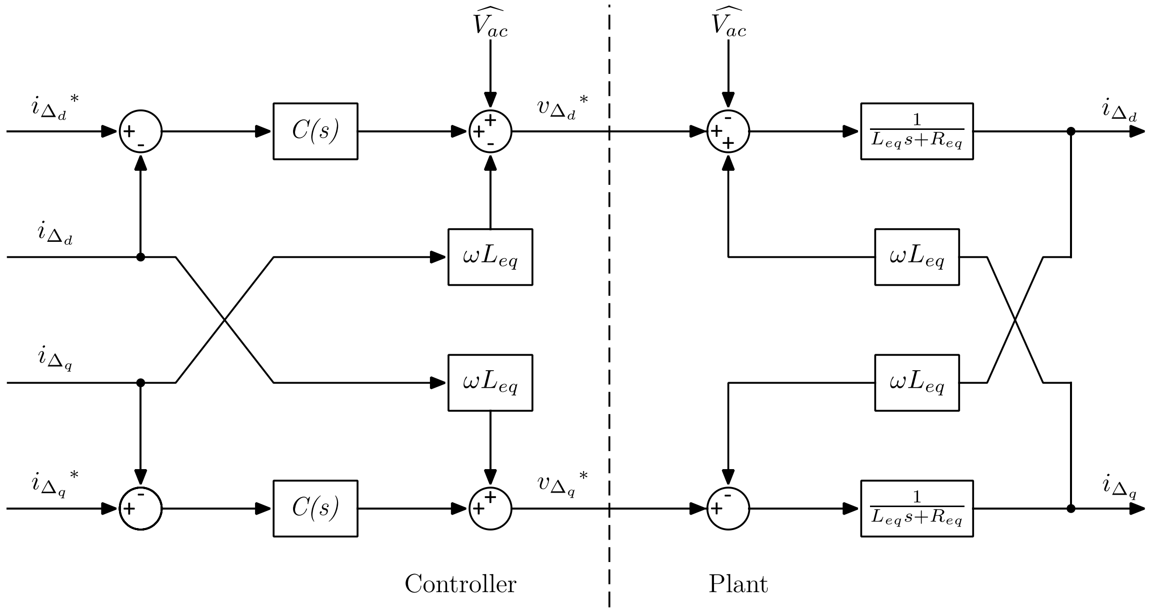


Figure 2.17. AC current control loop

2.6. Simulation results of converter operation

In order to validate the converter model employed in the previous paragraphs, as well as the control strategy, a Modular Multilevel Controller with the characteristics described in Table 2.2 was simulated. Additionally, the time response of the different controllers and the filter for the energy loops can be seen in Table 2.3. The waveforms corresponding to the simulated MMC are depicted in Figure 2.18. The waveforms seen on Figure 2.18 correspond to the legs simulated employing the reduced-order average model. These waveforms show the proper functioning of the high-level control loops.

Moreover, and since the subject of this study are the semiconductors inside an HB-SM, the main waveforms of a single SM can be appreciated in Figure 2.19. The single SM waveforms were issued from the legs simulated with the semi-analytic detailed model and require the use of the low-level controllers in order to be obtained.

Parameter	Variable	Value	Unit
Rated power	P	1	GW
AC grid voltage	$U_{ac_{rms}}$	333	kV
DC grid voltage	v_{dc}	640	kV
AC grid frequency	f	50	Hz
Average switching frequency	f_{sw}	150	Hz
Arm inductor	${L_{arm}}^{u,l}$	50	mH
Number of SMs per arm	N_{SM}	400	-
SM capacitor	C_{SM}	10	mF
Average capacitor voltage	$v_{C_{SM}}$	1.6	kV

Table 2.2 MMC parameters

Control Loop	Closed-loop time constant τ_{CL}
Energy sum W_Σ	100 ms
Energy difference W_Δ	100 ms
Low-pass filter τ_{LPF}	13 ms
DC current i_Σ	0.1 ms
AC current i_Δ	0.1 ms

Table 2.3 Closed-loop time constants for control validation

In Figure 2.18, different power references and the measured AC and DC powers can be seen. At the start of the simulation the power reference P^* is set to zero. At $t = 0.5\ s$, P^* is set to 1 GW. Then at $t = 1\ s$ the P^* is set to 0.7 GW and finally at $t = 2.5\ s$ the P^* is set to -1 GW. It can be clearly seen that the measured AC and DC powers follow the reference. In this figure the waveforms of the AC and DC grid currents can be seen. Both currents are proportional to the set points given by P^* and Q^*. It is also worth mentioning that the reactive energy reference Q^* was set to different setpoints for the validation of the control strategy, as verified on Figure 2.18. Finally, some waveforms internal to the MMC can be seen. The arm currents and the equivalent capacitor voltages are depicted to show the performance of the high-level control loops.

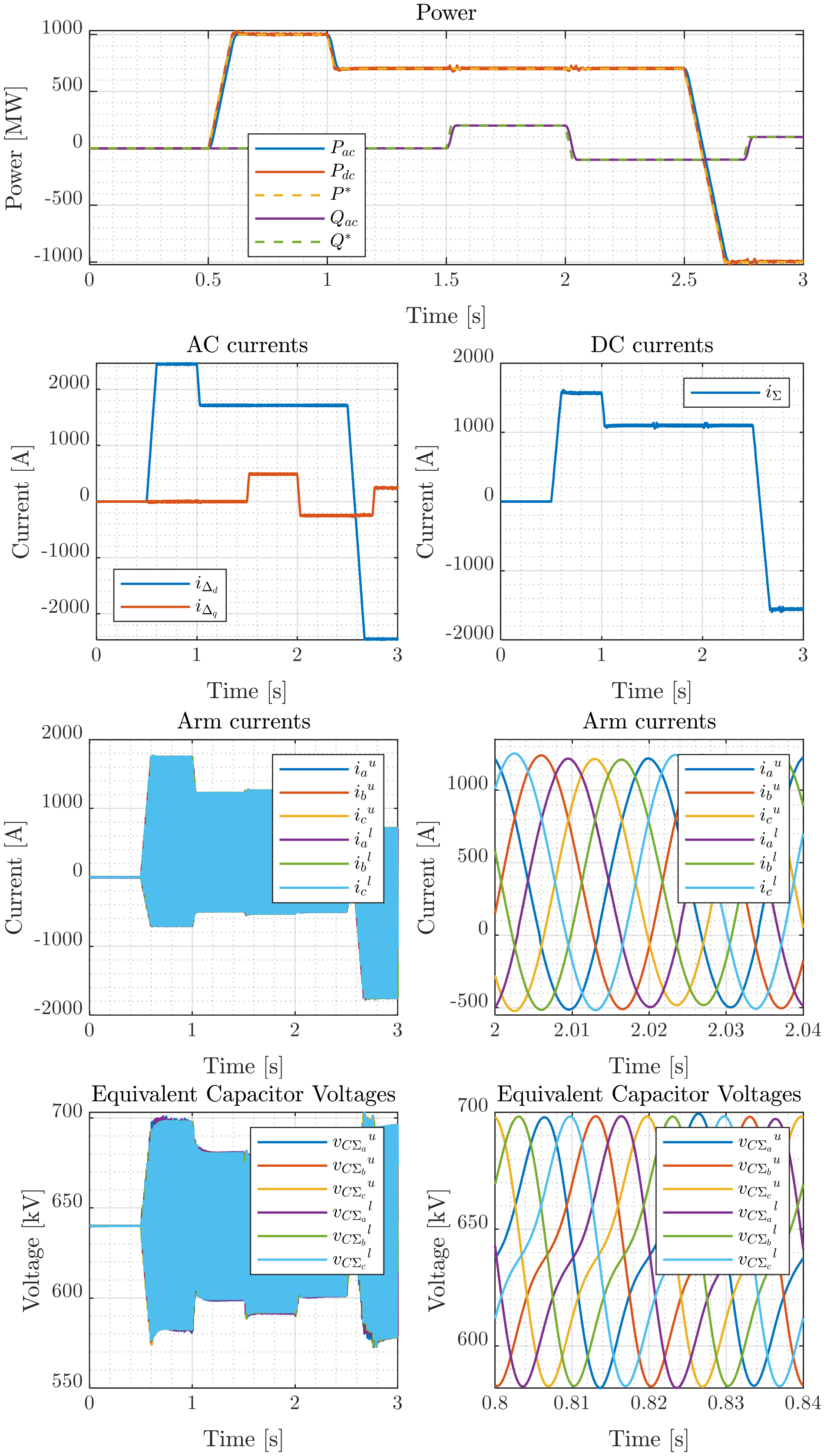


Figure 2.18. Reduced-order model waveforms, high-level control validation

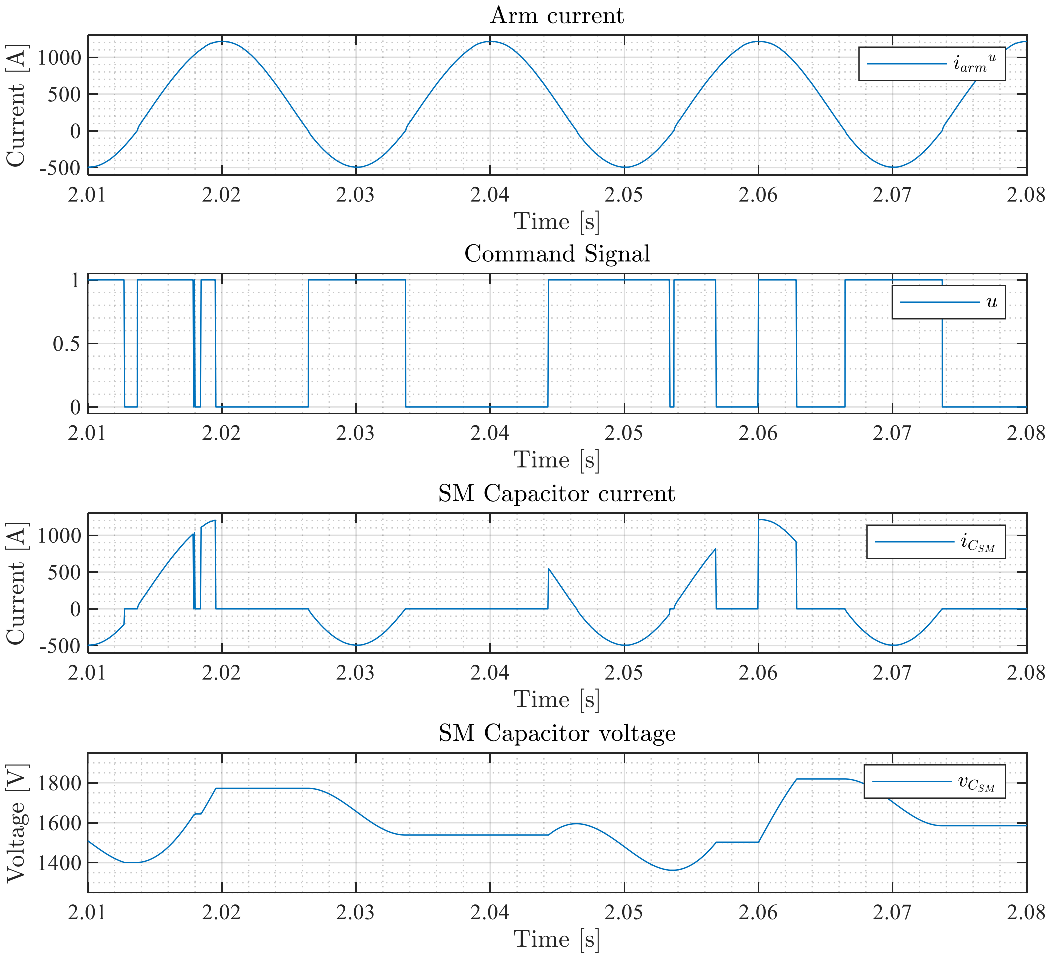


Figure 2.19. Single SM waveforms issued from detailed model, low-level control validation

In Figure 2.19 the waveforms corresponding to a single SM can be seen. From this figure, it is clear that the current entering the SM capacitor $i_{C_{SM}}$ is proportional to the product $u\, i_{arm}$. This current will be responsible for charging and discharging the SM capacitor. The voltage across the capacitor $v_{C_{SM}}$ can also be seen on Figure 2.19. It is worth noting that $v_{C_{SM}}$ stays within the limits set by the low-level control, thus validating the modulation and BCA deployed.

The waveforms seen on Figure 2.19 are the main output of the converter modeling stage. These waveforms will then be employed for the development of the lifetime estimation methodology. This lifetime estimation approach will only consider the electrical behavior of a single SM of a MMC and will focus on the lifetime estimation of the semiconductors composing the SM. The results of the lifetime estimation can then be generalized for the rest of the semiconductors inside the converter.

2.7. Chapter conclusion

This chapter dealt with the modelling of a modular multilevel converter. The work developed in this thesis makes use of two different modelling techniques for the different arms of the topology.

It was also seen in this chapter that the ΣΔ transformations allow for a decoupling of the DC and AC quantities present in the MMC. The mathematical description permits the understanding of the current dynamics that allow the control of the internal energy of the converter.

The reduced-order average model leads to determine the main mathematical laws concerning the general functioning of the converter. It is also this model that allows the verification of the high-level control strategy developed.

The semi-analytic detailed model permits the verification of the low-level control techniques, more particularly the balancing algorithm that is crucial for guaranteeing a safe operation of the converter.

The semi-analytic detailed model is the main resource employed for acquiring the HB-SM waveforms that will be used in the following chapters for developing the methodologies for lifetime estimation and reliability related analysis.

3. Methodologies for Lifetime Estimation, Reliability Predictions and Redundancy Computations

3.1. Introduction

In previous chapters, the importance of Modular Multilevel Converters for the development of HVDC links was discussed. Additionally, the benefits of the improved reliability of HVDC links was also addressed [23]. In light of these facts, a thorough study of the reliability of the MMC topology was conducted.

In this chapter the MMC was used as the subject for developing three different reliability related methodologies.

The first one concerns the lifetime estimation of the converter. This methodology is broken down into different stages that will be discussed in detail in section 3.2.

The second one deals with the reliability predictions of the MMC. This method makes use of component level reliability indicators, consequently determining system level reliability predictions.

The third methodology aims to make redundancy computations for determining the number of redundant submodules required by the converter. This computation is necessary for guaranteeing the availability standards imposed by the HVDC grids requirements.

Finally, this chapter makes a comparison between different case studies, each one employing different inputs for performing reliability predictions and redundancy computations.

3.2. Methodology for lifetime estimation based on mission profile

The methodology for lifetime estimation developed in this chapter is based on the analysis of the thermal loading experienced by the semiconductors of the studied converter as performed in [29], [160], [210]–[214]. In order to compute the thermal profiles of the semiconductor devices, the mission profile of the MMC is considered. Once the thermal profiles are obtained, they are translated to a lifetime consumption for the evaluated period, which finally allows an estimation of the lifetime consumption.

Additionally, the lifetime estimation methodology developed in this work will analyze the thermal loading of the semiconductors at different timescales as performed in [29], [160]. In [160] three different timescales are evaluated, each having different time constants. The identified scales were: Long-term, with time steps in the range of hours. Medium-term, with time steps in the range of seconds. Finally, the short-term with time steps in the range of milliseconds since it is performed for observing thermal variations caused by the line and switching frequency.

In this work, the first two timescales will be considered as performed in [29]. The short-term timescale will not be considered in this thesis. This is justified since the lifetime models provided by the manufacturer of the semiconductors [215] consider that thermal loading in the short-term time range will incur in almost negligible lifetime consumption.

Besides dealing with two different timescales, the approach for lifetime estimation in both cases is identical, but with some particularities to be considered for the different stages of the procedure.

The different stages employed throughout the lifetime estimation methodology can be seen in Figure 3.1. It consists of 5 different stages: the modeling of the converter, the calculation of the losses of the semiconductor devices, the calculation of the thermal loading, the use of the rain flow counting algorithm [156] for organizing the thermal profiles and finally, the use of the lifetime models provided by the manufacturer as well as the Miners rule [216] for estimating the lifetime consumption. All the stages were developed following the considerations in [217] and will be described in the following sections.

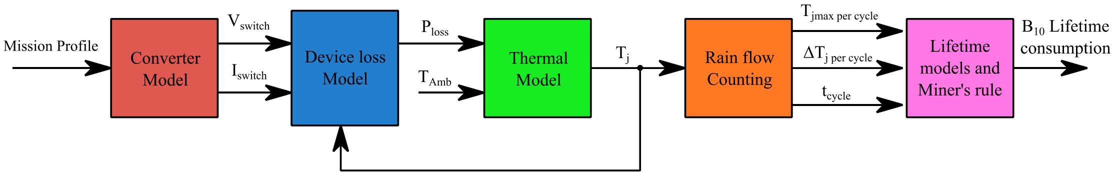


Figure 3.1. Lifetime Estimation Methodology

3.2.1. Estimation of power losses

In order to estimate the power losses, it is first necessary to identify the current and voltage across the different semiconductors composing a HB-SM. The current going through the semiconductors will be dependent on the command signal u of the SM and on the direction of the arm current i_{arm}. Figure 3.2 depicts the conducting device inside a HB-SM based on the different operational modes. An example of the current across the different semiconductors is depicted in Figure 3.3. The operating modes of a HB-SM are based on the state of the SM and the current direction. This information is also shown on Table 3.1, which gives information on the capacitor current and the output voltage of a HB-SM.

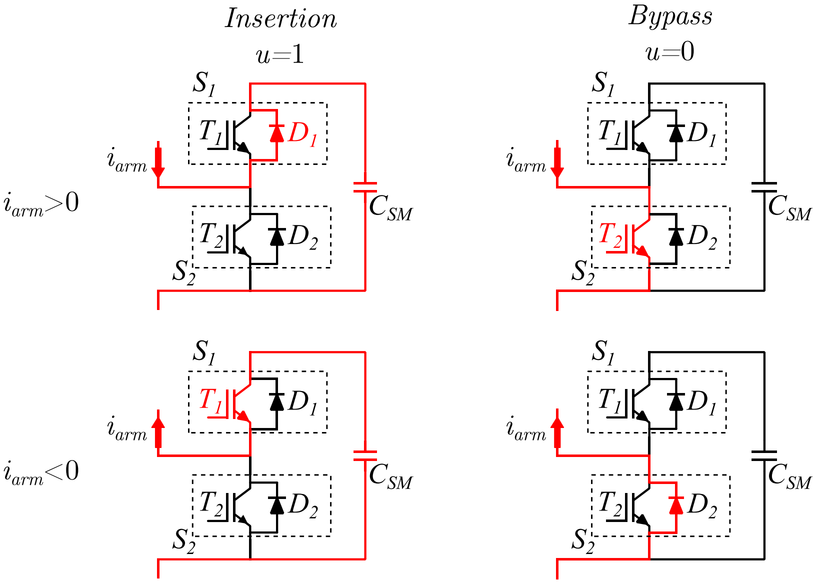


Figure 3.2. Conducting device on a HB-SM

Mode	Command signal	Current direction	SM output voltage	Capacitor current	Conducting device
1	$u = 1$	$i_{arm} > 0$	$v_{C_{SM}}$	i_{arm}	D_1
2	$u = 1$	$i_{arm} < 0$	$v_{C_{SM}}$	i_{arm}	T_1
3	$u = 0$	$i_{arm} > 0$	0	0	T_2
4	$u = 0$	$i_{arm} < 0$	0	0	D_2

Table 3.1 HB-SM operation modes

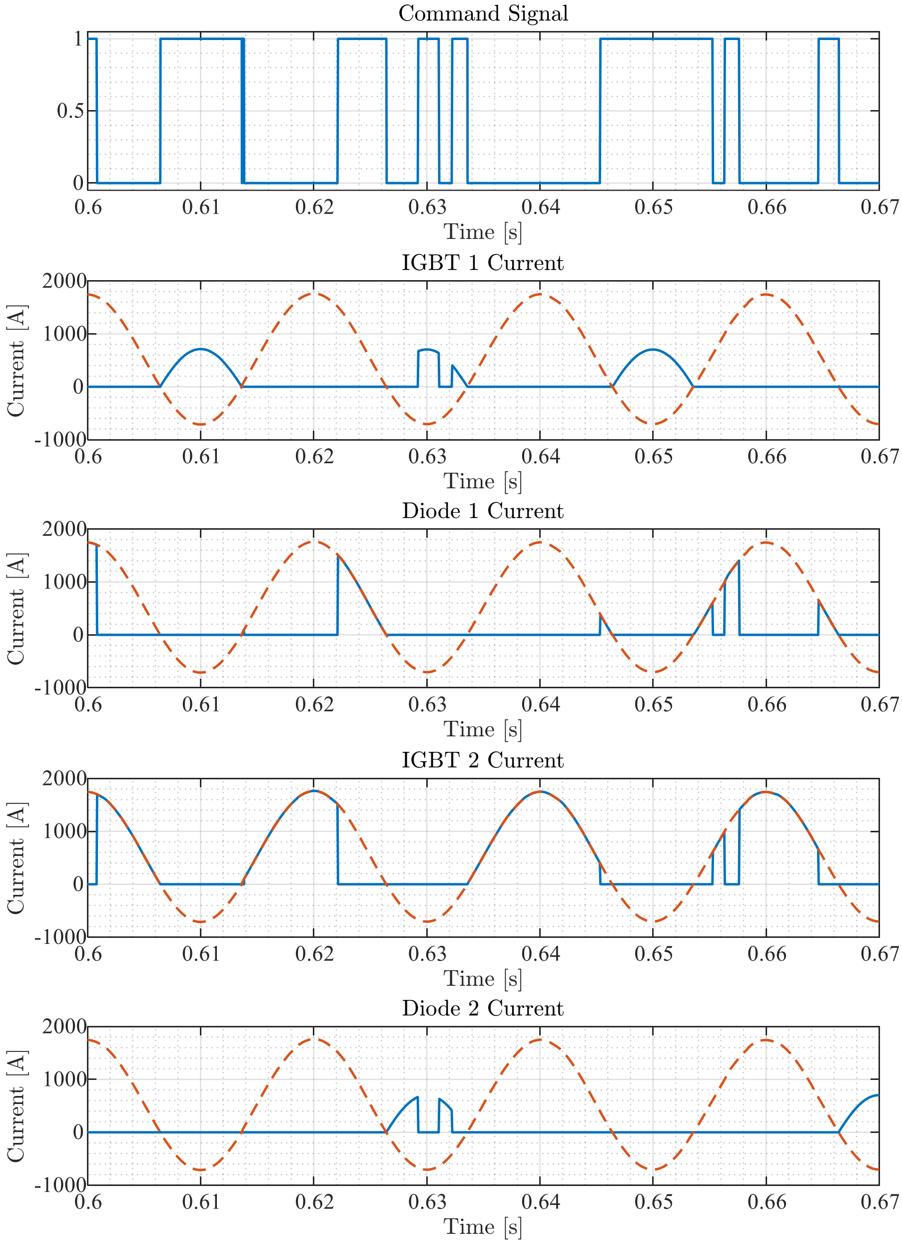
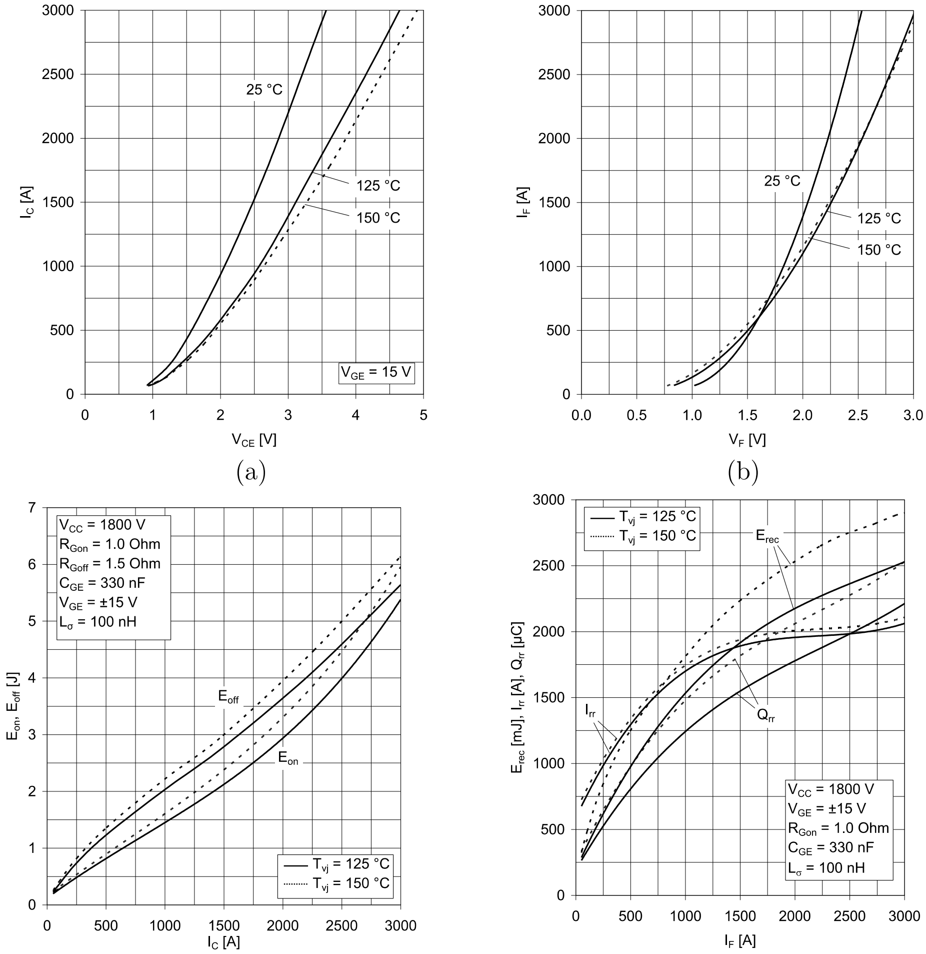


Figure 3.3. Example of semiconductors currents

Once the current and voltage across each semiconductor is identified, the methodology for calculating the power losses can be developed. The methodology uses the information provided by the manufacturer and presented in the semiconductors datasheet [218]. The losses experienced by the power devices are separated in conduction and switching losses. The information provided on the data sheet allows for the calculation of both. The curves allowing the power losses estimation of the IGBTs of a HB-SM are depicted in Figure 3.4.



(a) (b)

(c) (d)

Figure 3.4. Datasheet information for the calculation of semiconductor losses [218]: (a) IGBT On-state characteristics (b) Diode Forward characteristics (c) IGBT Switching energies per pulse vs. collector current (d) Diode Recovery characteristics vs. forward current

In order to reduce the computation time, the datasheet information was converted to look-up tables that allow for a faster calculation of the power losses experienced by the devices as carried out in [29], [160]. The look-up tables consider the converter power setpoint as an input. Subsequently, for each operating point, the nominal voltages and currents are calculated for a single HB-SM and its semiconductors. In order to obtain a realistic value of currents and voltages, the converter simulation was carried out for several seconds. The final current and voltage values of the semiconductors of a HB-SM were used as inputs to the look-up tables that contain the datasheet information. The process for the calculation of the losses of an IGBT is depicted in Figure 3.5. The losses were averaged over a period of converter operation for obtaining the average losses over a period.

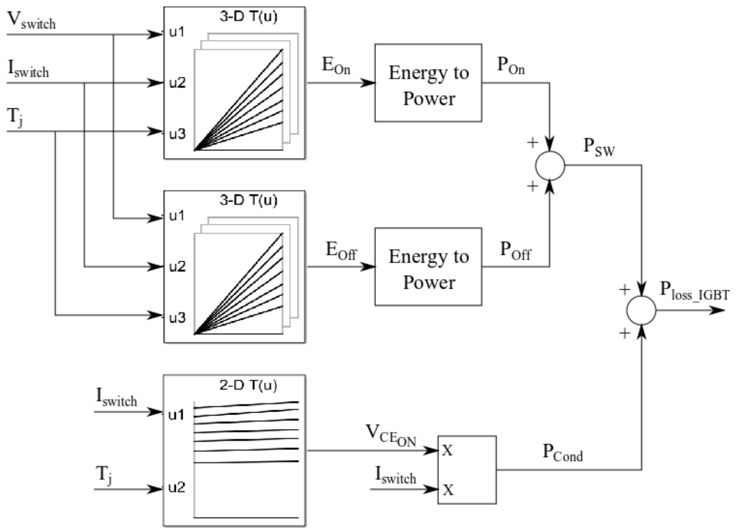


Figure 3.5. Procedure for calculating the losses of an IGBT

Additionally, the look-up tables employ the semiconductors junction temperature for the calculation of the power losses. The different look-up tables employed for the loss estimation stage can be seen in Figure 3.6.

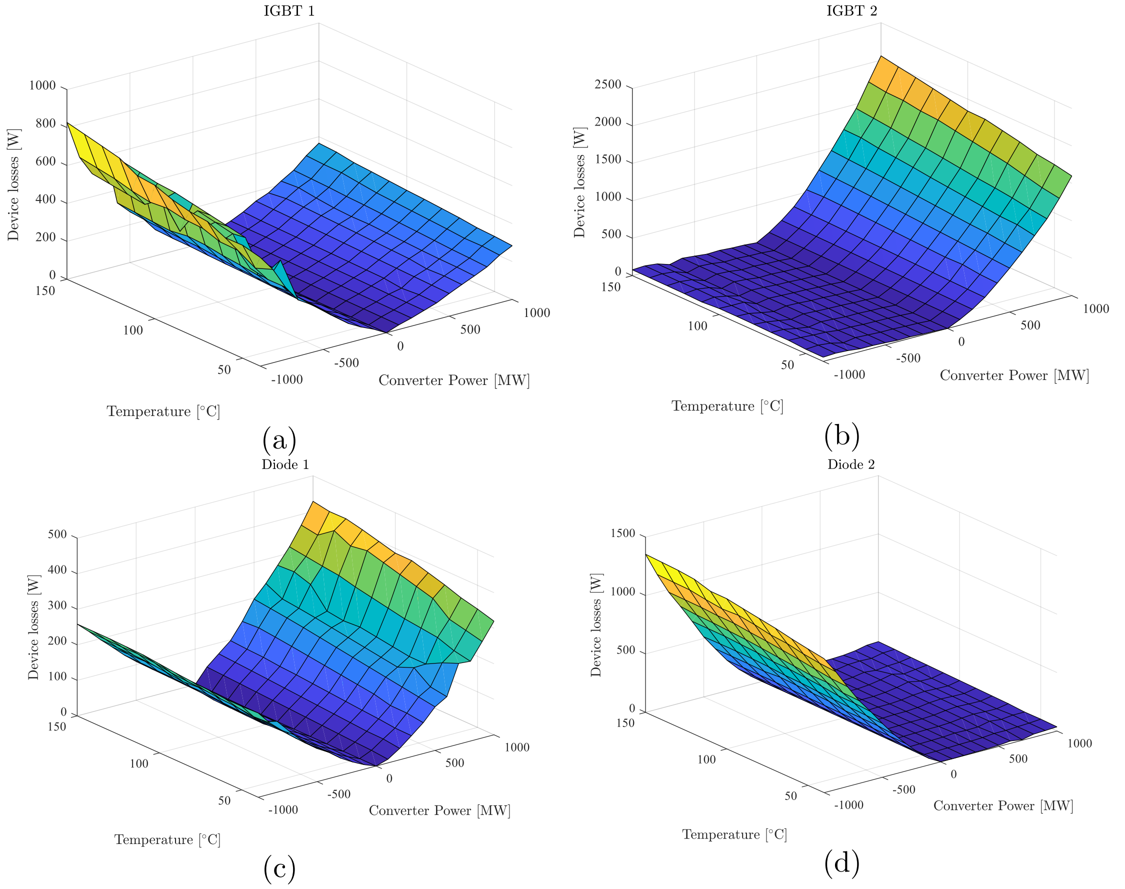


Figure 3.6. Look-up tables for losses estimation: (a) IGBT 1 (b) IGBT 2 (c) Diode 1 (d) Diode 2

3.2.2. Thermal modelling

It was previously mentioned that the lifetime estimation methodology based on the evaluation of the mission profile experienced by the converter is carried out considering two different time scales.

In the case of the long-term time scale, the time span of the evaluated profiles is of one year of operation. Given this timespan, the time-step chosen for evaluating the thermal loading is of one-hour. Additionally, most of the data found on mission profiles considering different applications give hourly inputs [219] [220], which will be more easily exploited by the thermal model developed for the long-term timescale.

In the case of the medium-term time scale, the approach considered in [29] was implemented. The medium-term profiles are generated for the studied applications. The generation of medium-term profiles will be further discussed on the evaluation of the case-studies. Nevertheless, it is worth mentioning that the time-step employed for evaluating the medium-term thermal loading is 1 second.

Up until this point on the lifetime estimation methodology, the same model of the converter and the same modelling of the power losses will be used for the different timescales. However, two different thermal models will be employed as a way to consider the differences between the studied timescales as done in [29].

Both thermal models employed are based on the semiconductor information provided by the manufacturer and presented in the datasheet [218]. The information to be exploited by the thermal models is presented in the form of the thermal impedance curves shown in Figure 3.7. Additionally, the manufacturer provides a mathematical approximation of the transient thermal impedance. This mathematical approximation is presented in the form of a fourth order Foster thermal network seen on Figure 3.8. These parameters are an approximation of the transient thermal impedance of the semiconductor from the junction to the case $Z_{th_{jc}}$. Additionally, the manufacturer provides information on the case to heatsink thermal resistance $R_{th_{ch}}$ of the different semiconductors. The parameters for the considered module are presented in Table 3.2.

Device	Parameter	Unit	Variables			
IGBT	$R_{th_{jc}}$	K/kW	5.854	1.375	0.641	0.632
	$\tau_{th_{jc}}$	ms	207.4	30.1	7.55	1.57
	$R_{th_{ch}}$	K/kW	9	-	-	-
Diode	$R_{th_{jc}}$	K/kW	11.54	2.887	1.229	1.295
	$\tau_{th_{jc}}$	ms	203.6	30.1	7.53	1.57
	$R_{th_{ch}}$	K/kW	18	-	-	-

Table 3.2 Thermal parameters of the considered semiconductors [218]

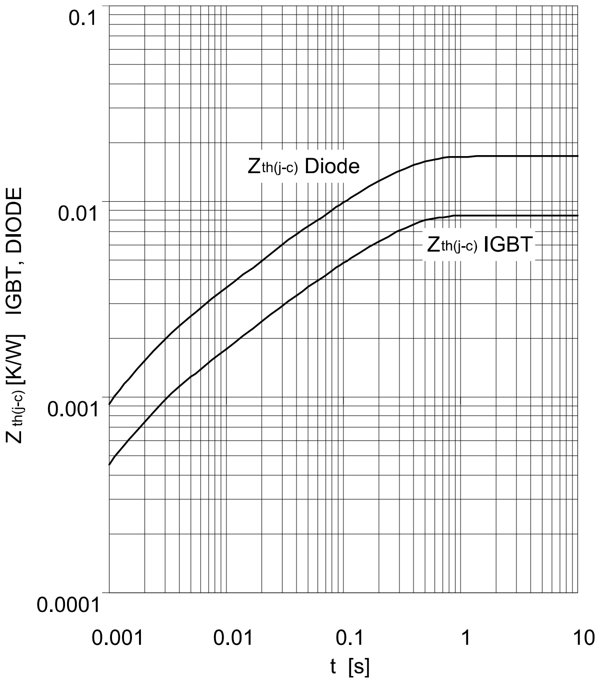


Figure 3.7. Transient thermal impedance vs time of the studied semiconductors [218]

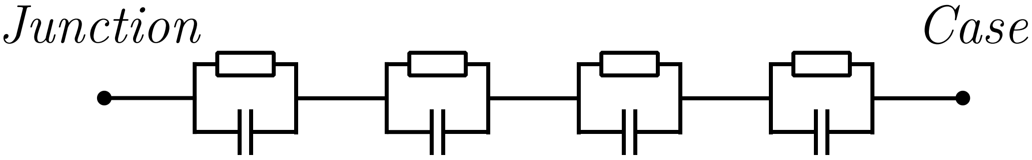


Figure 3.8. Foster thermal network

Both thermal models will be explained in the next lines. The model employed for long-term analysis is known as a static thermal model and the model employed for medium-term analysis is known as a dynamic thermal model.

3.2.2.1. Static thermal model

As the long-term timescale has a time step of one hour, the time constants of the semiconductors have no significant impact on the thermal profiles in this time scale. This can be clearly seen in Table 3.2, since the time constants of both IGBT and diode have a maximum value in the range of some hundreds of milliseconds.

The semiconductor manufacturer presents the thermal behavior as a Foster network. In this particular case the information is presented as a series of junction-to-case thermal resistances $R_{th_{jc}}$ and as a series of time constants $\tau_{th_{jc}}$ for each of the approximated layers. A thermal capacitance for each layer can also be simply deduced from this information.

Moreover, a thermal heatsink is also necessary for completing the thermal model. The heatsink also has a particular thermal resistance and capacitance that need to be calculated accordingly to the application.

The static thermal model will only consider the thermal resistances of the different layers. Therefore the time constants, and the thermal capacitances, will not have a significant impact on the final thermal loading profiles in this timescale [29], [160]. This model can be seen in Figure 3.9.

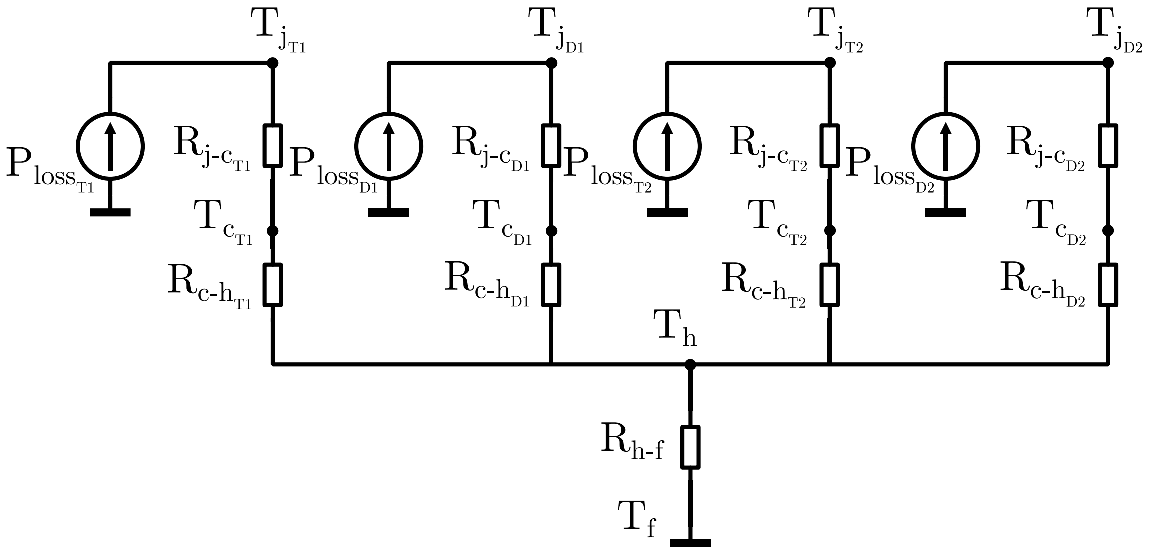


Figure 3.9. Static thermal model

From Figure 3.9 it can be seen that all the semiconductors present in a HB-SM share a common heatsink. This allows the cooling of the power devices and creates a heating path between the heating sources (semiconductors) and a cold source (thermal cooling fluid). This also means that the heatsink will see the losses experienced by all the semiconductors.

The thermal resistance of the heatsink $R_{th_{hf}}$ must be dimensioned to guarantee that the maximum junction temperature of every semiconductor connected to it is not exceeded. Hence, this static thermal model is not only employed for calculating the long-term thermal loading. It is also employed for dimensioning the thermal resistance $R_{th_{hf}}$ of the cooling system.

For the dimensioning of $R_{th_{hf}}$ the power-losses look-up tables can be directly employed. It can be seen on Figure 3.6 that the elements with the bigger losses are the lower devices (IGBT 2 and Diode 2). This is probably due to the fact that the HB-SM is in the bypassed state longer than it is inserted. It can also be seen on Figure 3.6 that when the converter power is positive the element that experiences the bigger losses is the IGBT 2. Whereas in the case of negative powers, the element that experiences bigger losses is the Diode 2. However, it can be clearly distinguished that IGBT 2 experiences much important losses than Diode 2. Therefore, the dimensioning of $R_{th_{hf}}$ will be performed for assuring that the maximum junction temperature of IGBT 2 is not exceeded. Eq. (3.1) shows the criteria for dimensioning $R_{th_{hf}}$.

$$T_{j_{max}} = T_f + R_{th_{hf}} \sum P_{loss} + \left(R_{th_{jc}} + R_{th_{ch}}\right) P_{loss_{T2}} \tag{3.1}$$

Where T_f is the cooling fluid temperature, $\sum P_{loss}$ corresponds to the sum of power losses in all the semiconductors. $R_{th_{jc}}$ and $R_{th_{ch}}$ are the thermal resistances of the IGBT and $P_{loss_{T2}}$ corresponds to the losses experienced by the IGBT 2.

From Eq. (3.2), the expression for $R_{th_{hf}}$ can be deduced:

$$R_{th_{hf}} = \frac{\left(T_{j_{max}} - T_f\right) - \left(R_{th_{jc}} + R_{th_{ch}}\right) P_{loss_{T2}}}{\sum P_{loss}} \tag{3.2}$$

It is crucial that the thermal resistances present in the SM cooling scheme be minimized. This allows for an increase in the power density of the converter [211].

It should be noted that within the semiconductors, the layers that contribute the most to the thermal resistance $R_{th_{jc}}$ are the solder and ceramic isolation [211]. To address this issue and improve the thermal performances of semiconductor devices, especially those employed for higher voltages and powers, new materials with higher thermal conductivities such as aluminum nitride (AlN) for the ceramic isolation and 95Pb-5Sn or 96Sn-4Ag for the solder have been introduced [211], [221].

The thermal resistance of the thermal interface material (TIM) $R_{th_{ch}}$, must also be minimized or eliminated if possible. The most typical TIM employed are thermal pastes applied between the baseplate of the modules and the surface of the heatsink to improve the thermal contact conductance by replacing the air, which has a lower thermal conductivity [211].

Finally, the thermal resistance of the cooling solution $R_{th_{hf}}$ depends on many factors such as the type of cooling medium, type of convection, the geometry of the heatsink, the characteristics of the fans or pumps employed, etc. All these characteristics must be considered on the design stage as they impact on the cost, volume, weight and reliability of the cooling solution [211].

3.2.2.2. Dynamic thermal model

Contrarily to what was assumed for the static thermal model, the thermal constants and capacitances of the different layers of the semiconductors and the cooling solutions can no longer be ignored. Since, the time-step employed for the medium-term analysis is of 1 second, the capacitances will play a major role on the performance of the thermal model.

As it was already presented, the manufacturer provides fourth order Foster networks for describing the thermal behavior of the semiconductors. But for a complete thermal model, the TIM and the heatsink need to be considered.

According to [222], the series connection of Foster models can lead to inaccurate results, especially in the lower time regime. Therefore, the dynamic thermal model is based on the use of Cauer thermal networks as the one seen on Figure 3.10.

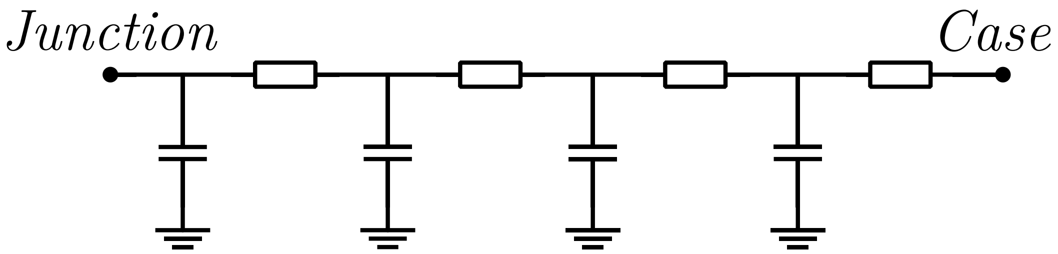
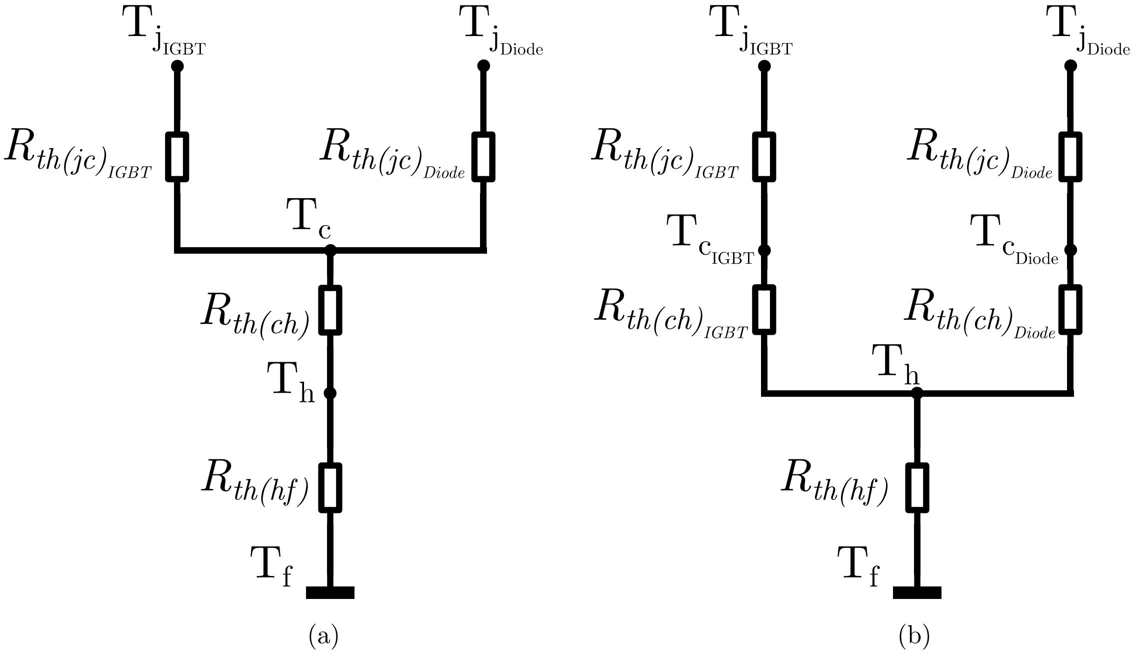


Figure 3.10. Cauer thermal network

The use of Cauer thermal networks for the different semiconductors present in the HB-SM requires a mathematical transformation to convert the data provided by the manufacturer. The Foster to Cauer conversion is based on [223]. Subsequently, the TIM and heatsink Cauer thermal models will be connected in series to the Cauer networks corresponding to the different power devices.

According to the manufacturer of semiconductors, there are two possible ways of modelling the thermal interface as seen on Figure 3.11. On the one hand, in the model seen on Figure 3.11 (a) the IGBT and diode of a single switch share the same thermal interface resistance. On the other hand, Figure 3.11 (b) depicts a model where each element, IGBT and diode have their own individual thermal resistance. According to [222], the latter modeling technique provides a more realistic simplification.



(a) (b)

Figure 3.11. Modelling of the thermal interface

Thus, after performing the Foster to Cauer transformations and employing the thermal interface modelling where each semiconductor has its own individual TIM, a new thermal network for the HB-SM can be obtained. This thermal network corresponds to the dynamic thermal model employed in this thesis, which can be seen on Figure 3.12.

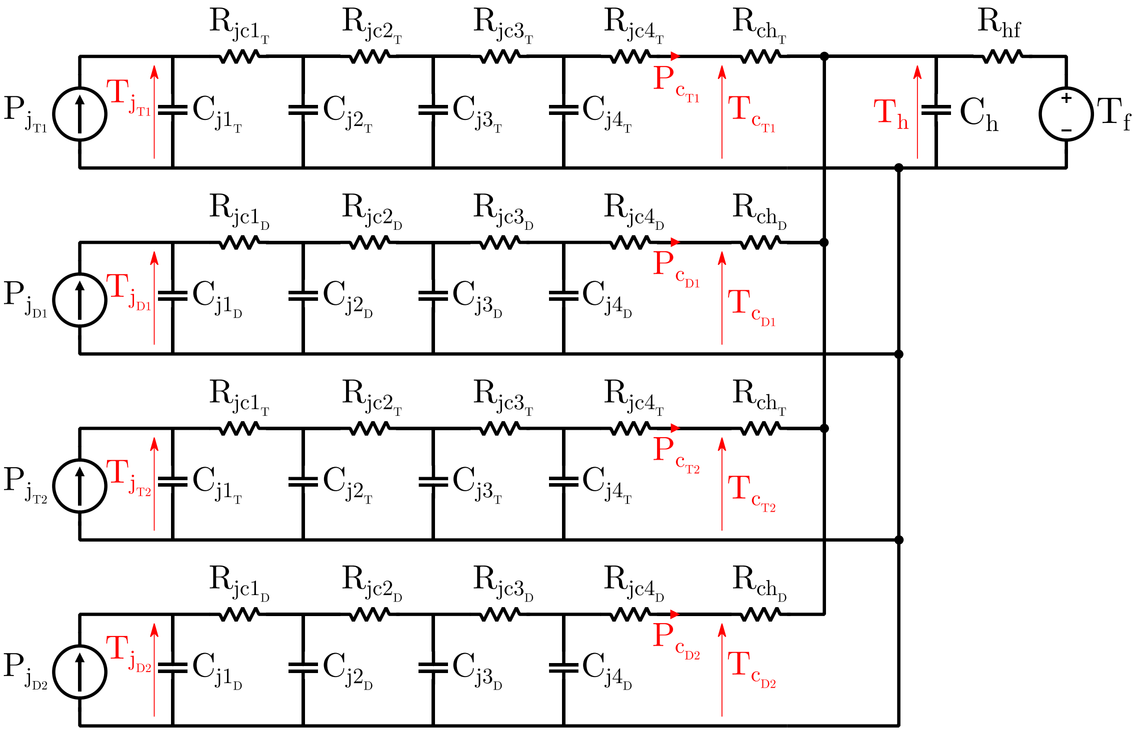


Figure 3.12. Dynamic thermal model

The dynamic thermal model developed allows for the calculation of the heatsink temperature as well as the case and junction temperatures for all the power devices present in a HB-SM. The dynamic thermal model can also be expressed as a set of state-space representations that will allow the calculation of the thermal loading of the different layers. In order to have a simplified state-space representation, each semiconductor will have its own state-space model and the heatsink will be subjected to the same modelling approach.

The simplified thermal model for the semiconductors is depicted in Figure 3.13. The expression describing the state-space representation for the semiconductors can be seen on Eq. (3.3). It must be noted that T_1 in Eq. (3.3) corresponds to the junction temperature of the semiconductor T_{j_k}, where $k = \{T1, D1, T2, D2\}$.

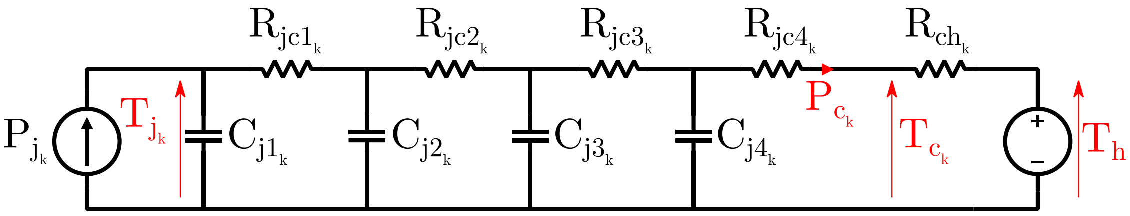


Figure 3.13. Simplified dynamic thermal model for the semiconductors

$$\frac{d}{dt}\begin{bmatrix}T_1\\T_2\\T_3\\T_4\end{bmatrix}=\begin{bmatrix}-\frac{1}{R_1C_1} & \frac{1}{R_1C_1} & 0 & 0\\ \frac{1}{R_1C_2} & -\frac{1}{C_2}\left(\frac{1}{R_1}+\frac{1}{R_2}\right) & \frac{1}{R_2C_2} & 0\\ 0 & \frac{1}{R_2C_3} & -\frac{1}{C_3}\left(\frac{1}{R_2}+\frac{1}{R_3}\right) & \frac{1}{R_3C_3}\\ 0 & 0 & \frac{1}{R_3C_4} & -\frac{1}{C_4}\left(\frac{1}{R_3}+\frac{1}{R_4+R_{ch}}\right)\end{bmatrix}\begin{bmatrix}T_1\\T_2\\T_3\\T_4\end{bmatrix}+\begin{bmatrix}\frac{1}{C_1} & 0\\ 0 & 0\\ 0 & 0\\ 0 & \frac{1}{C_4(R_4+R_{ch})}\end{bmatrix}\begin{bmatrix}P_{j_k}\\T_h\end{bmatrix} \tag{3.3}$$

The model seen on Figure 3.13 and on Eq. (3.3) allows the calculation of the temperatures in all the internal layers of the fourth order Cauer network. However, the actual junction temperature is represented by the first layer of this model. One particularity of this model is that the TIM does not have a thermal capacitance. This can also be reflected on Eq. (3.3). In order to calculate the rate of change of the last layer of every semiconductor $\dot{T}_4$, the last term of the state matrix adds the last Cauer thermal resistance R_4 and the case-to-heatsink thermal resistance R_{ch}.

The thermal model of the heatsink is depicted on Figure 3.14 and the state-space representation of the heatsink can be seen on Eq. (3.4).

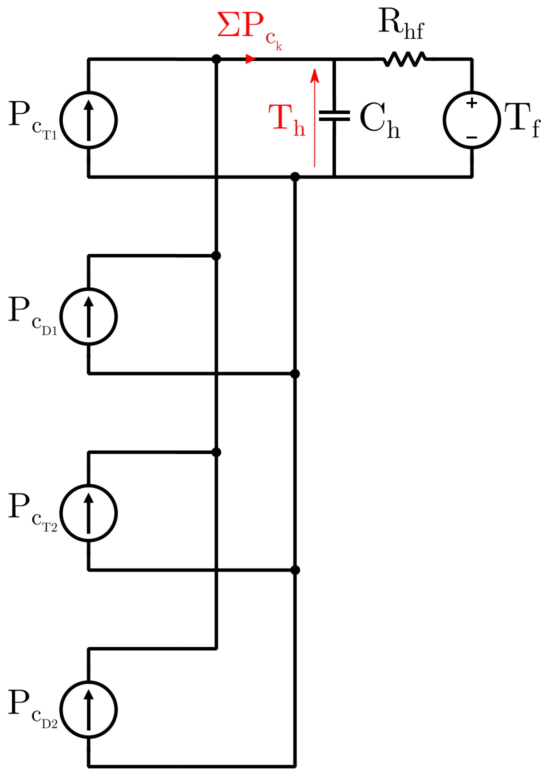


Figure 3.14. Simplified thermal model of the heatsink

$$\frac{d}{dt}[T_h] = \left[-\frac{1}{R_{hf}C_h}\right][T_h] + \left[\frac{1}{C_h} \quad \frac{1}{R_{hf}C_h}\right]\begin{bmatrix}\sum\limits_{k}^{T_1,D_1,T_2,D_2} P_{c_k}\\ T_f\end{bmatrix} \tag{3.4}$$

As it can be evidenced by both Figure 3.14 and Eq. (3.4), all the losses going through the case-to-heatsink resistance R_{ch} of every power device are added and they are all fed to the heatsink thermal model.

The thermal model of the heatsink is composed of the heatsink-to-cooling fluid thermal resistance $R_{th_{hf}}$ and its thermal capacitance C_{th_h}. It was previously discussed on section 3.2.2.1 that the static-thermal model permits the calculation of $R_{th_{hf}}$. However, the choice of the thermal capacitance can be made by choosing a type of cooling mechanism and verifying the typical thermal capacitances of such cooling elements. An example of the typical thermal time constants for different cooling methods can be seen on Figure 3.15.

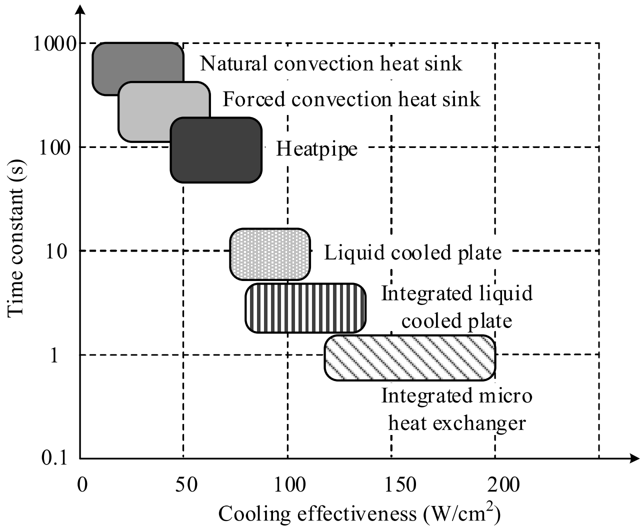


Figure 3.15. Comparison of cooling solutions in terms of cooling effectiveness and thermal time constant [211]

In regular HVDC-MMC applications the cooling of the elements of the HB-SM is done with a liquid cooled plate. From Figure 3.15, it can be appreciated that such a cooling solution has a thermal time constant in the range of 10 s.

This information would be applicable to the HB-SM if the volume of the cooling fluid would be used only for cooling one particular SM. However, in the case of a real HVDC-MMC, the cooling system is mutualized for all the HB-SMs present in an arm. Under this particular condition, it can be assumed that the total volume and mass of the cooling fluid are no longer negligible. Having such a large thermal mass in the form of the thermal fluid used for the cooling of the elements of a converter arm, it can also be inferred that the thermal inertia provided by this cooling system is quite important. As a way of reflecting the impact of the thermal inertia provided by the cooling system, a thermal time constant in the range of some hundred seconds will be considered for the rest of the study.

For concluding this paragraph, the performances of the dynamic thermal model can be appreciated in Figure 3.16 and Figure 3.17.

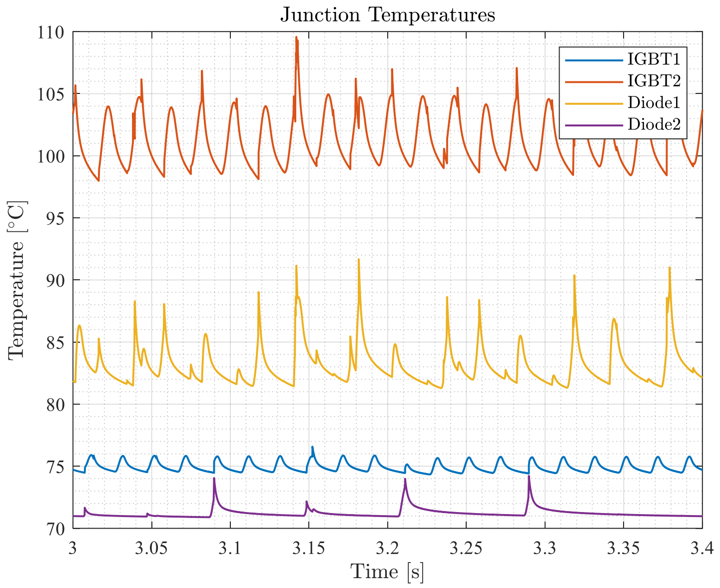


Figure 3.16. Junction temperature of the semiconductors in a HB-SM (Inverter mode)

The thermal profiles seen on Figure 3.16 are obtained from a simulation of a 1 GW MMC operating at its rated power. It can be clearly evidenced that the different power devices are subjected to different thermal stresses for a given operating point of the converter.

From Figure 3.16 it can also be concluded that when operating in inverter mode, the lower IGBT (IGBT 2) presents a higher thermal stress, which is consistent with the losses in the look-up tables seen in Figure 3.6. Hence, it is logic to assume that when operating in rectifier mode, the element that will have a bigger thermal stress is the lower diode (Diode 2) as hinted by Figure 3.6 and confirmed in Figure 3.17.

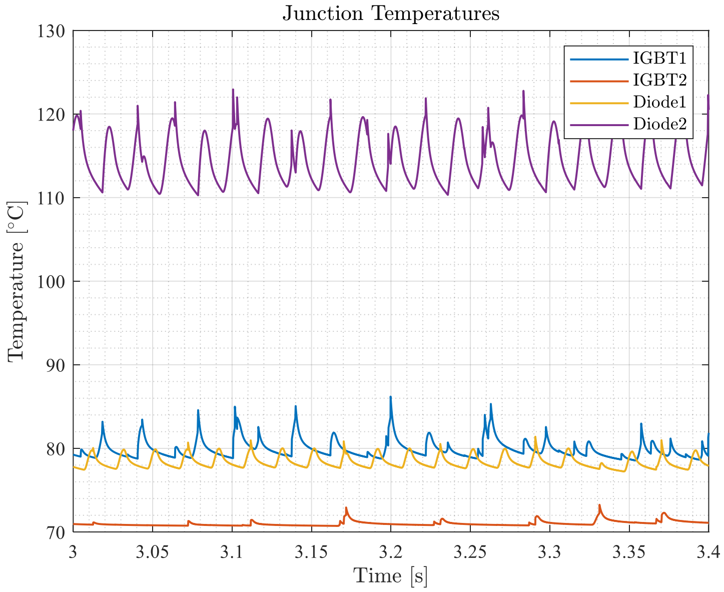


Figure 3.17. Junction temperature of the semiconductors in a HB-SM (Rectifier mode)

3.2.3. Calculation of lifetime consumption and remaining useful life

The calculation of the lifetime consumption of semiconductor devices based on the thermal profiles they experienced is possible thanks to the use of lifetime models, cycle counting algorithms and the Miner's rule. Each of these topics will be addressed in the next paragraphs.

3.2.3.1. Lifetime models

Even if there is extensive literature concerning analytical lifetime prediction models, such as the ones already covered in section 1.6.1.1, some semiconductor manufacturers also provide their own lifetime prediction models based on empirical data obtained after performing cycling tests [215]. In this study, the lifetime model of the manufacturer will be employed for performing the lifetime estimation methodology. The model employed is presented in the form of cycling curves seen on Figure 3.18.

In the particular case of ABB, this manufacturer presents the lifetime models as B_{10} lifetime curves. These curves represent the estimated number of cycles to failure for a 10% failure rate or the number of cycles during which 10% of the modules' population fails under the given thermal conditions.

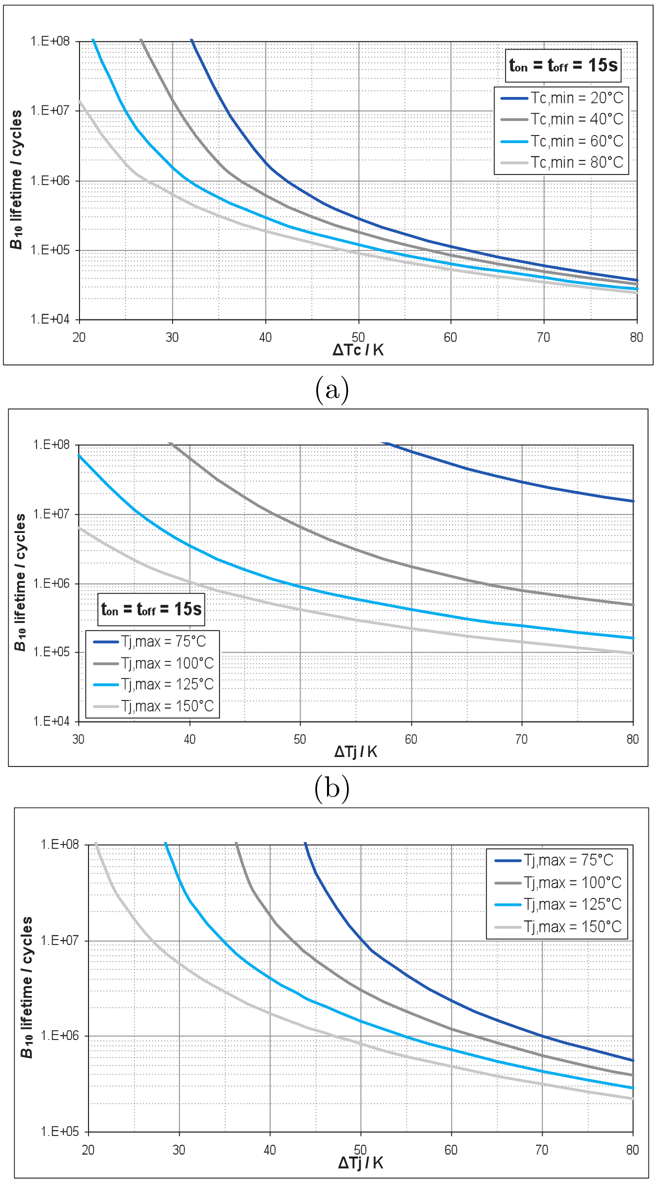
Moreover, the lifetime models provided by ABB are based on the Coffin-Manson law and fatigue of the joints due to plastic deformation [215]. Additionally, the manufacturer provides different lifetime models for the different elements of the semiconductor modules as evidenced in Figure 3.18. Three different lifetime models are presented in [215], they describe the lifetime of the substrate solder joints, the chip solder joints and the bond wires.

As it can be seen on Figure 3.18 (a) the model for the substrate solder joints is dependent on the case temperature T_c of the modules. Also, the lifetime of substrate solder joints is dependent on the duration of the thermal cycle applied, in Figure 3.18 (a) some lifetime curves for a t_{cycle} of 30 seconds can be seen. Curves for different t_{cycle} can be found in [215].

Figure 3.18 (b) depicts the lifetime model of the chip solder joints. This model is dependent on the junction temperature of the semiconductors T_j as well as the duration of the thermal cycles t_{cycle}. In Figure 3.18 (b) some lifetime curves for a t_{cycle} of 30 seconds can be seen. Curves for different t_{cycle} can be found in [215].

Finally, the lifetime model of the bond wires seen on Figure 3.18 (c). This model is also dependent on the junction temperature of the semiconductors T_j. However, the lifetime of the bond wires is independent on the duration of t_{cycle}.

The use of the manufacturer lifetime models is limited to the specified input ranges described in [215]. Hence, in order to generalize the manufacturer data a method for extrapolating the ageing data based on a physical law was developed and will be described in the following lines.



(c)

Figure 3.18. Lifetime model of the different elements of an IGBT module [215]: (a) substrate solder joints (b) chip solder joints (c) bond wires

3.2.3.1.1. Model-based extrapolation method

As mentioned previously, the lifetime models provided by the manufacturer of the power devices is only applicable if the inputs are within the specified ranges expressed in [215]. Thus, in order to extend the applicability and to accurately calculate the N_f under a given thermal condition a special model-based extrapolation method was developed.

This extrapolation method is based on the Norris-Landzberg lifetime prediction model described in Eq. (3.5). Under two different cycling conditions, the N_{f_2} for a new cycling condition can be computed from the N_{f_1} of a previous thermal condition and the new thermal constraints applied to the newer test. This relationship is expressed in Eq. (3.5).

$$N_{f_2} = N_{f_1} \left(\frac{\Delta T_2}{\Delta T_1}\right)^{\alpha} \left(\frac{f_2}{f_1}\right)^{\beta} \exp\left(\frac{E_a}{k}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right) \tag{3.5}$$

This expression considers the frequency at which the thermal cycles of both cycling conditions are fixed. Nonetheless, this expression can also be formulated based on the duration of the thermal cycles as seen on Eq. (3.6).

$$N_{f_2} = N_{f_1} \left(\frac{\Delta T_2}{\Delta T_1}\right)^{\alpha} \left(\frac{t_1}{t_2}\right)^{\beta} \exp\left(\frac{E_a}{k}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right) \tag{3.6}$$

The model-based method allows to simply interpolate the ageing data by calculating the α, β, and γ coefficients between two different cycling conditions as expressed in Eq. (3.7), Eq. (3.8) and Eq. (3.9) [29], [30]. Those expressions assume that only a single thermal condition is different between two different ageing protocols. This allows to compute a 3D grid (Figure 3.19) for calculating the estimated lifetime for any combination of thermal cycling conditions. The α, β and γ coefficients for each mesh in Figure 3.19 are computed employing a least-squares algorithm considering the vertices data of each mesh. The coefficients α, β and γ computed for the outer meshes are employed for the extrapolations.

$$\alpha = \frac{\log\left(\frac{N_{f_2}}{N_{f_1}}\right)}{\log\left(\frac{\Delta T_2}{\Delta T_1}\right)} \tag{3.7}$$

$$\beta = \frac{\log\left(\frac{N_{f_2}}{N_{f_1}}\right)}{\log\left(\frac{t_1}{t_2}\right)} \tag{3.8}$$

$$\gamma = \frac{E_a}{k} = \frac{\log\left(\frac{N_{f_2}}{N_{f_1}}\right)}{\left(\frac{1}{T_2} - \frac{1}{T_1}\right)} \tag{3.9}$$

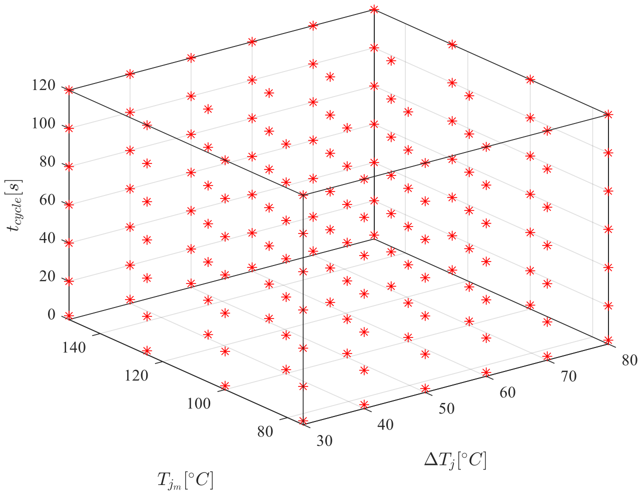


Figure 3.19. 3D grid for interpolation/extrapolation of ageing coefficients

In order to be able to employ the lifetime models of the semiconductor manufacturer along with the extrapolation method, there is a need to organize the thermal loading profile experienced by the power devices. Cycle counting methods are employed for this kind of task. Among the different counting algorithms present in the literature [154], [155], the one that has shown the most accurate results is the rainflow counting algorithm [155]. This method will be further explained in the next section.

3.2.3.2. Rainflow counting algorithm

To predict the life of a component subjected to a variable load history, it is necessary to reduce the complex history to a number of events which can be compared to available constant amplitude test data. The process of reducing the loading history to a number of constant amplitude events involves cycle counting [140]. The more popular cycling counting methods were presented in section 1.6.1.2.

It was previously mentioned that the counting method to be employed in this thesis is the rainflow counting method. Thus section 1.6.1.2.1 already covered the working principle of this method.

The outputs of the rainflow counting method are a tabularized series of events of different amplitudes. This data is normally given as a table containing the extracted cycles information or in the form of a histogram. An example can be seen on Figure 3.20, corresponding to the temperature of a semiconductor inside a HB-SM. In this example the mean junction temperature T_m of the semiconductors is employed for organizing the thermal profile.

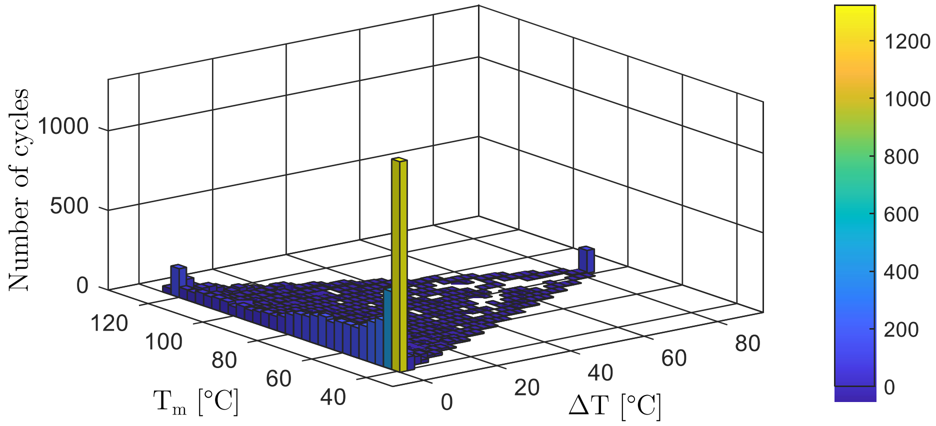


Figure 3.20. Histogram of the extracted thermal cycles with the rainflow counting algorithm

3.2.3.3. Miner's rule, lifetime consumption and RUL computation

Once the thermal loading of the semiconductors is obtained and organized in thermal cycles thanks to the rainflow counting algorithm, the lifetime models along with the model-based extrapolation method are employed for calculating the number of cycles to failure N_f for each of the identified thermal cycles. This information allows for the calculation of the lifetime consumption CL of each individual cycle as seen on Eq. (3.10):

$$CL_{i,k} = \frac{nb_i}{N_{fi,k}}, k \in \{\text{chip solder, dbc solder, bondwire}\} \tag{3.10}$$

In Eq. (3.10), nb_i represents the number of experienced thermal cycles under a given thermal cycling condition $(\Delta T_i, T_i)$. It can also be seen on the same expression that the lifetime consumption for the different elements of the semiconductor can be calculated in this way. This is possible, as the manufacturer provides different lifetime models for the composing elements of a semiconductor as seen on section 3.2.3.1.

Once the individual lifetime consumption of all the thermal cycles is calculated the total lifetime consumption in the evaluated period is calculated with the help of the Miner's rule [216]. This rule states that the lifetime consumption of a material is linear. Therefore, the total lifetime consumption CL_Σ can be computed by adding all the individual lifetime consumptions of any particular thermal condition, as expressed in Eq. (3.11). This is performed for all the elements composing the power device.

$$CL_{\Sigma,k} = \sum_i CL_{i,k}\,, k \in \{\text{chip solder, dbc solder, bondwire}\} \tag{3.11}$$

Finally, a lifetime estimation LF can be made for all the elements of a semiconductor thanks to Eq. (3.12) if a mission profile of one-year is evaluated:

$$LF_k = \frac{1}{CL_{\Sigma,k}}, k \in \{\text{chip solder, dbc solder, bondwire}\} \tag{3.12}$$

3.2.4. Case studies

The profile-based lifetime estimation methodology developed in previous lines was employed for two different case studies. The first one concerns a Point-to-Point HVDC link (P2P). The second case concerns an offshore windfarm (OWF) application. The methodology for lifetime estimation remains the same for both case studies, as shown in Figure 3.21.

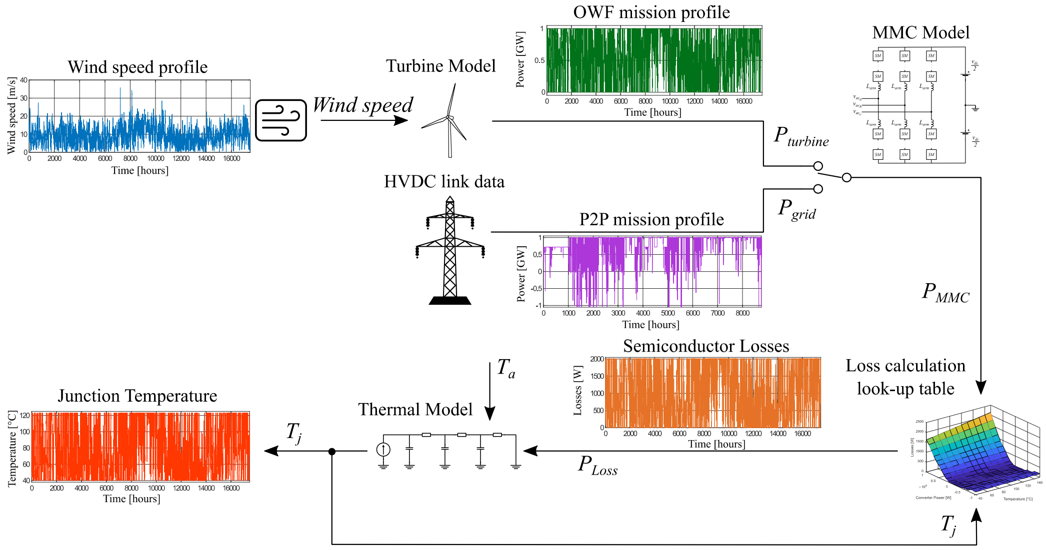


Figure 3.21. Lifetime estimation methodology applied to both case studies

The case studies were chosen as they have radically different mission profiles. The different profiles will be discussed in the following lines.

3.2.4.1. P2P application

One of the main characteristics of the chosen P2P link, is that it allows power reversals. The chosen P2P link in this study corresponds to the NordNed link between Norway and the Netherlands. In spite of the fact that this HVDC link uses Line Commutated Converter (LCC) technology, the power exchange data was adapted to a 1 GW MMC based link in order to perform the study. This approach was adopted due to lack of public information on mission profiles for MMC based HVDC links, as it was done previously in [29].

3.2.4.1.1. Long-term mission profile

The data concerning the long-term mission profile for the P2P application was extracted from the ENTSO-E Transparency Platform [219]. It corresponds to a 1-year power exchange with intervals of one hour. Figure 3.22 depicts the long-term mission profile for the P2P link addressed in this study.

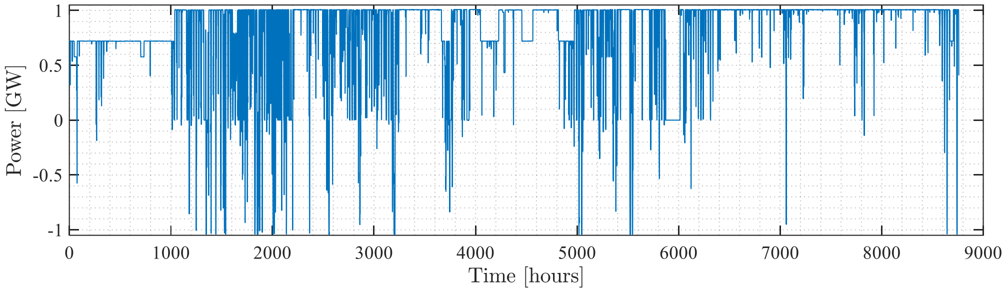


Figure 3.22. Long-term mission profile for P2P link

3.2.4.1.2. Medium-term mission profile

The data corresponding to the medium-term mission profile for the P2P link was employed following the same approach as carried out in [29] and inspired from [160]. This approach consists of generating 1-hour power profiles. The profiles generated will range from -1 GW to 1 GW by steps of 0.1 GW. The profiles will be obtained with the help of a normal distribution to simulate the power fluctuations. The normal distribution will be centered around each of the evaluated powers and the variance is set for a maximum variation of 40MW around the average power. Figure 3.23 presents an example of a power profile centered around 1 GW.

Similar to what was done in [29], [160], it is necessary to consider the frequency of occurrence of all the “average powers” evaluated in the long-term profile.to be able to calculate the medium-term lifetime consumption. The histogram illustrating this frequency of occurrence can be seen in Figure 3.24. The yearly medium-term lifetime consumption for the P2P link CL_{MT-P2P} will be calculated following Eq. (3.13). In this expression the weights of all the average powers (W_{-1GW} to W_{1GW}) as well as the lifetime consumptions (CL_{-1GW} to CL_{1GW}) are considered. It is worth noting that the sum of all the weights is equal to one as they represent the probability of occurrence of an operating point.

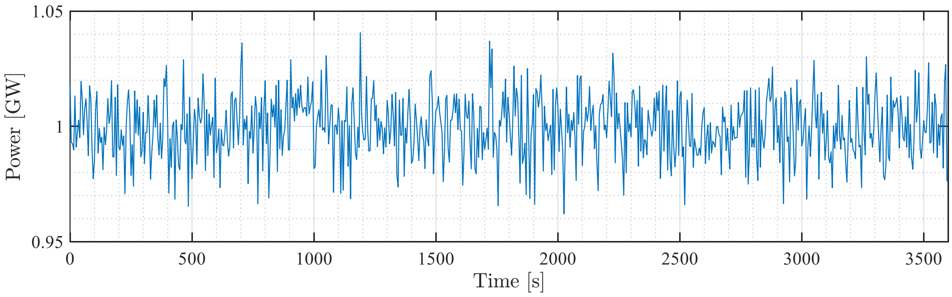


Figure 3.23. Generated profile (1 GW) for medium-term analysis of a P2P link

$$CL_{MT-P2P} = 365 \cdot 24 \cdot (W_{-1GW} \cdot CL_{-1GW} + \cdots + W_{1GW} \cdot CL_{1GW}) \tag{3.13}$$

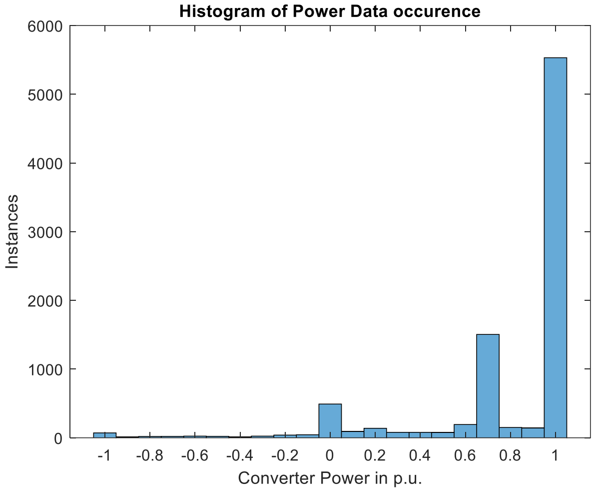


Figure 3.24. Frequency of occurrence of long-term operating points for P2P application

3.2.4.2. OWF application

For the OWF application, an additional stage must be made since the retrieved data for this case study are wind profiles from the Lidar located at the Anholt (ANH) offshore wind farm [220]. The wind profiles are then translated to power operating points for the MMC, by considering the mechanics of the wind turbine system [160].

It should be noted that a whole wind farm was approximated to a model of a single equivalent turbine of 1 GW in order to reduce the complexity of the simulations in this case study. Additionally, some particularities need to be considered for the timescales studied and they will be described in their corresponding sections.

3.2.4.2.1. Long-term mission profile

The data retrieved from the Anholt windfarm was acquired every 10 minutes over two years as depicted in Figure 3.25. Afterwards, this data is fed to a wind turbine model. Since the wind data is sampled at 10 minutes and only long-term thermal characteristics are examined in this timescale, the dynamics of the wind turbine are ignored as done in [160]. Thus, the wind profile is simply translated to the power operating point by using the power curve of the turbine. The main characteristics of the power curve of the turbine employed are described in Table 3.3. The resulting mission profile for the converter is depicted in Figure 3.26.

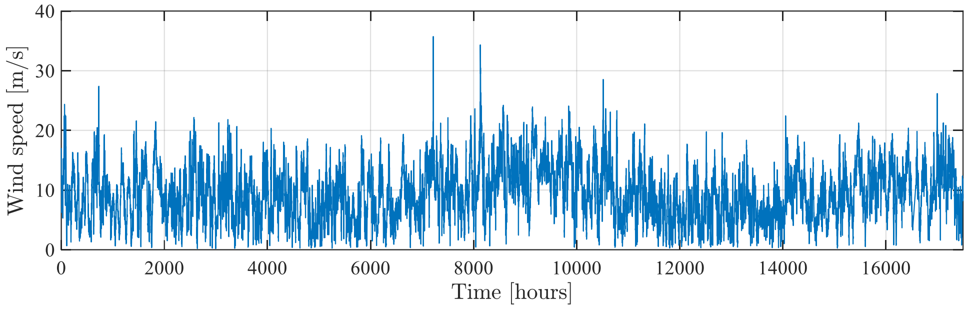


Figure 3.25. Wind profile for long-term analysis

Cut-in speed [m/s]	Cut-out speed [m/s]	Rated wind speed [m/s]	Recut-in wind speed [m/s]
4	25	12	24*

Table 3.3 Power-curve characteristics of the employed turbine
*The recut-in wind speed has a delay of 30 minutes to simulate the start-up process

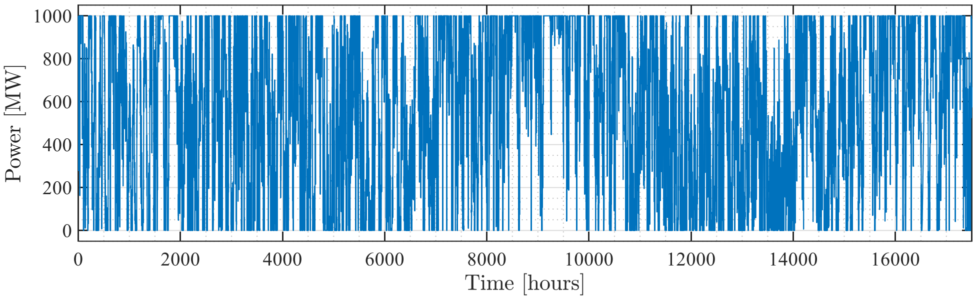


Figure 3.26. Long-term mission profile for MMC in OWF application

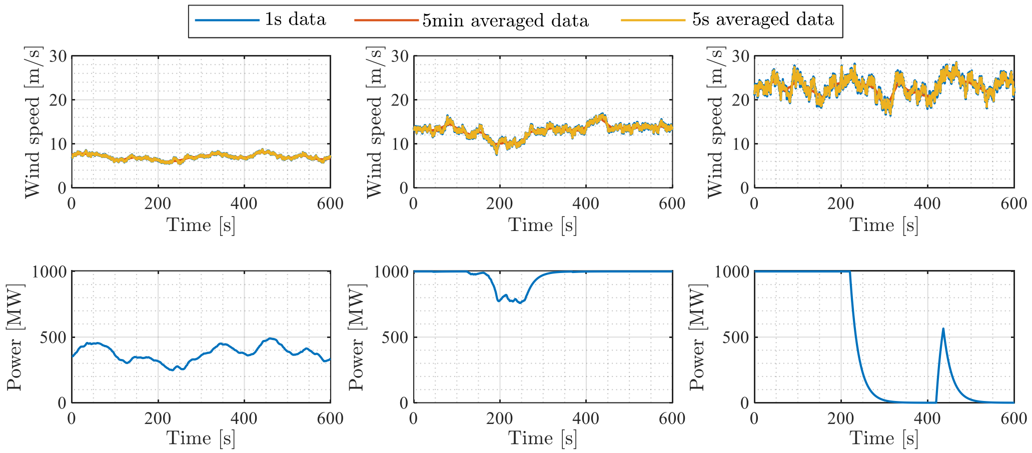
3.2.4.2.2. Medium-term mission profile

Concerning the medium-term mission profile a similar approach to the one in [160] was considered. In this timescale the thermal loading of the semiconductors will also be influenced by the dynamics of the wind turbine system such as the pitch control, to limit the generated power and speed control to maximize the power production. As the long-term data was sampled at 10 minutes, this time span will be used for this timescale. Also, a one-second time step was considered for this analysis.

For performing this study, 10-minute wind profiles were generated with the help of the Kaimal spectra [224]. A turbulence of 18% was considered, as it corresponds to Class A wind turbulence. Several wind speeds were considered for the generation of the profiles. The wind speeds employed range from 1 m/s to 29 m/s by steps of 2 m/s. The Kaimal spectra is be centered around the wind speeds.

Afterwards, the wind profiles are used for calculating the output power of the turbine, which will be the operating point for the MMC associated to the windfarm. In order to perform the calculation of the operating point, the turbine characteristics seen in Table

3.3 are considered. Additionally, some detailed considerations need to be applied for applying the power curve characteristics. The cut-in speed is set at 4 m/s with 5 min average, the cut-out speed is 25 m/s with 5 min average or 32 m/s with 5 s average. Additionally, the recut-in wind speed is set at 24 m/s with a delay of 30 min to simulate the startup process of the system. Moreover, since the dynamics of the wind turbine are considered in this study, a time constant of 20 seconds is used to simulate the inertia of the power generation chain of elements (wind turbine, drive train and generator). Some examples of the generated wind profiles and their corresponding converter power can be seen in Figure 3.27.



(a) (b) (c)

Figure 3.27. Generated wind speeds (instantaneous, 5-min averaged and 5s averaged) and their corresponding output power. (a) V_{avg} = 7 m/s, (b) V_{avg} = 13 m/s, (c) V_{avg} = 23 m/s

As it was performed in [160], the means by which the 10-minute generated profiles are translated to full-year lifetime consumptions is to weight the lifetime consumption of each profile. The weight applied to the 10-minute operating conditions can be obtained from the density of wind speed distribution seen in Figure 3.28. The yearly medium-term lifetime consumption for the OWF application CL_{MT-OWF} is computed from Eq. (3.14). In this expression the weighting factors of all the wind speeds ($W_{1m/s}$ to $W_{29m/s}$) i.e. the frequency of occurrence of the wind speeds as well as the lifetime consumptions ($CL_{1m/s}$ to $CL_{29m/s}$) computed from the powers associated to these wind speeds are considered.

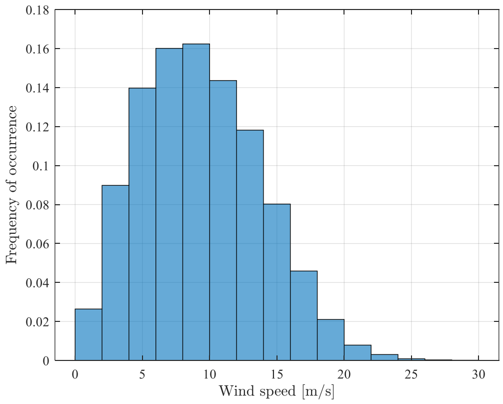


Figure 3.28. Frequency of occurrence of wind speeds throughout the evaluated period

$$CL_{MT-OWF} = 365 \cdot 24 \cdot 6 \cdot (W_{1m/s} \cdot CL_{1m/s} + \cdots + W_{29m/s} \cdot CL_{29m/s}) \qquad \textbf{(3.14)}$$

3.2.5. Results

As the lifetime estimation methodology is based on the analysis of the thermal loading of power semiconductors, it is necessary to first compute the thermal profiles for both timescales covered in this study.

3.2.5.1. Thermal loading

The resulting thermal profiles for the long-term period were obtained thanks to the static thermal model developed in section 3.2.2.1. The cooling system characteristics were dimensioned so that a maximum junction temperature of 90°C is reached for the most stressed component at rated power. Figure 3.29 depicts the thermal loading of IGBT 2 corresponding to the profile seen in Figure 3.22 for the P2P link. Similarly, Figure 3.30 shows the thermal profile of IGBT 2 corresponding to the OWF profile seen in Figure 3.25.

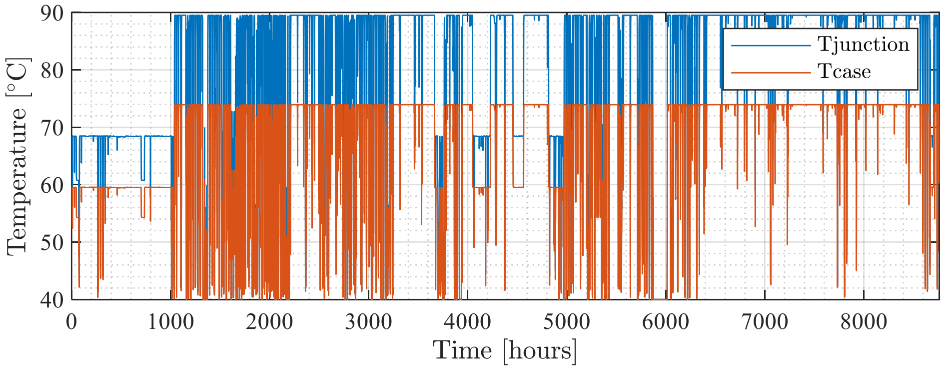


Figure 3.29. Thermal profile of IGBT 2 over the long-term period, P2P application

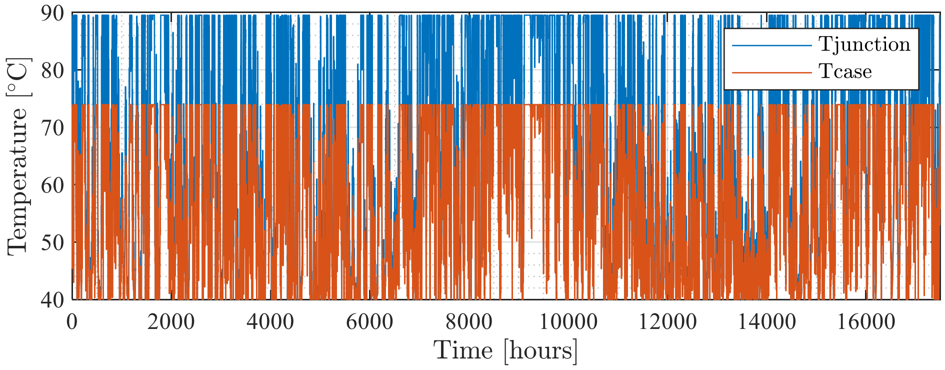


Figure 3.30. Thermal profile of IGBT 2 over the long-term period, OWF application

Concerning medium-term analysis, the results were obtained with the help of the dynamic thermal model from Figure 3.12. In the case of the P2P application an example of a thermal profile for the one of the generated medium term power profiles (Figure 3.23), can be seen in Figure 3.31. Additionally, the thermal profiles corresponding to the wind term profiles seen in Figure 3.27 are illustrated in Figure 3.32.

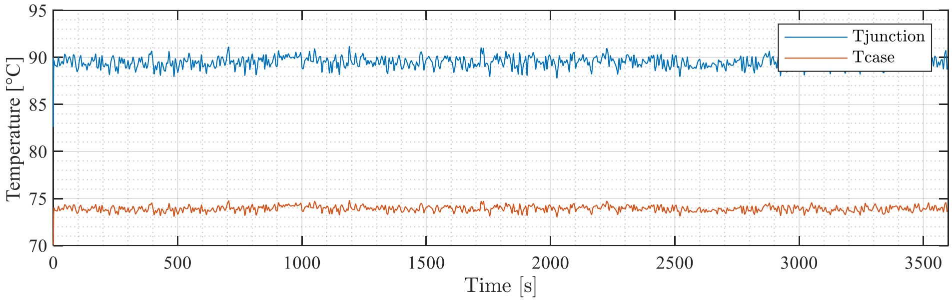


Figure 3.31. Thermal profile of IGBT 2 (1GW) over the medium-term period, P2P application

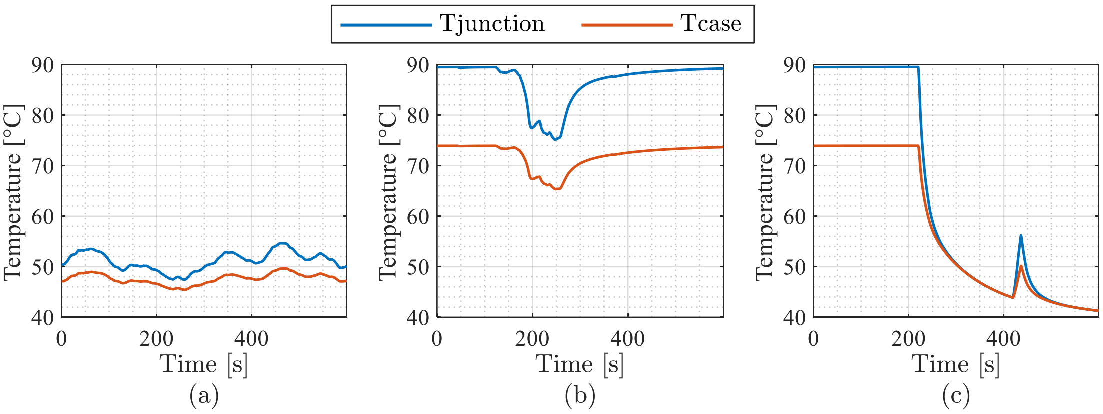


Figure 3.32. Thermal profile of IGBT 2 over the medium-term period for different wind speeds (a) $\boldsymbol{V_{avg}} = 7$ m/s, (b) $\boldsymbol{V_{avg}} = 13$ m/s, (c) $\boldsymbol{V_{avg}} = 23$ m/s

The medium-term thermal profile obtained for the P2P application, of Figure 3.31, indicates that there are several small thermal cycles for this particular case study. The results will be similar for the other medium-term profiles generated around different "average powers" for the P2P application, since the criteria for the generation of these power profiles was a steady maximum variation of 40 MW.

For the OWF application, Figure 3.32 shows that the thermal loading of the semiconductor can be quite different under various wind conditions. From Figure 3.32 (a) it can be seen that at wind speeds below the rated wind speed the temperature profiles have some fluctuations. These fluctuations will increase as the wind speed increases but remains below the rated wind speed. In Figure 3.32 (b) it can be seen that when the rated wind speed is reached, the temperature remains stable as the power-curve of the turbine fixes the power production to the rated capacity. However, when the wind speed decreases, it will generate a big fluctuation to the thermal profile as evidenced on Figure 3.33 (c).

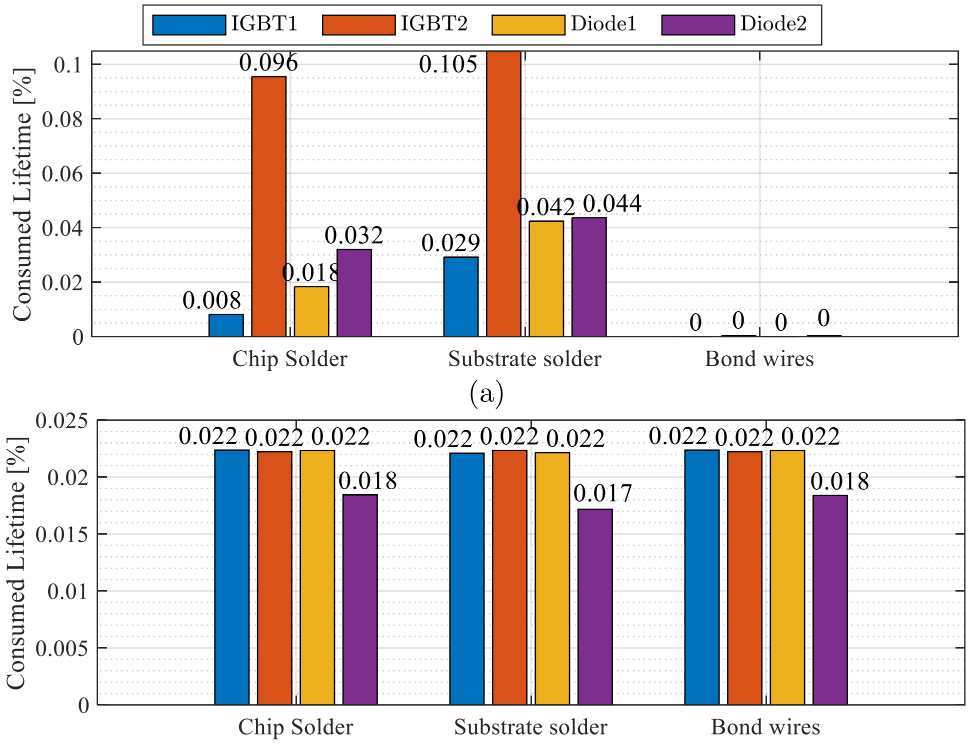
3.2.5.2. Lifetime Consumption and Remaining Useful Life

From the thermal profiles obtained in section 3.2.5.1 the lifetime consumption of all the different elements of the semiconductors of a HB-SM can be obtained by employing the stages previously described on this chapter: the rainflow counting algorithm, the manufacturer lifetime models, the model-based extrapolation method and the Miners' rule.

The results concerning the lifetime consumption experienced in the P2P application can be seen in Figure 3.33 and Figure 3.34. The results depicted in both figures show the lifetime consumption for the individual elements of the semiconductor: the chip solder, the substrate solder and the bond wires.

Figure 3.33 depicts the lifetime consumption in the two studied timescales. Figure 3.33 (a) depicts the lifetime consumption in the long-term timescale, whereas Figure 3.33 (b) shows the lifetime consumption on the medium-term timscale. From Figure 3.33 (a) it can be seen that the lifetime consumption for the substrate solder is more significant than the other elements in the long-term timescale. Moreover, from Figure 3.33 (a) it can be seen that the semiconductor that has the higher lifetime consumption is IGBT 2. From Figure 3.33 (b) it can be seen that the lifetime consumption is quite similar between all the elements of the semiconductors and also, the lifetime consumption is similar between the different semiconductors of the HB-SM.

By comparing the results of both timescales, it can be seen that the total lifetime consumption in the P2P application (Figure 3.34) is mostly dominated by the long-term thermal cycles. However, for the bond wires, the lifetime consumption is more important in the medium-term timescale.



(a)

(b)

Figure 3.33. Lifetime consumption for the P2P application: (a) Long-term, (b) Medium-term

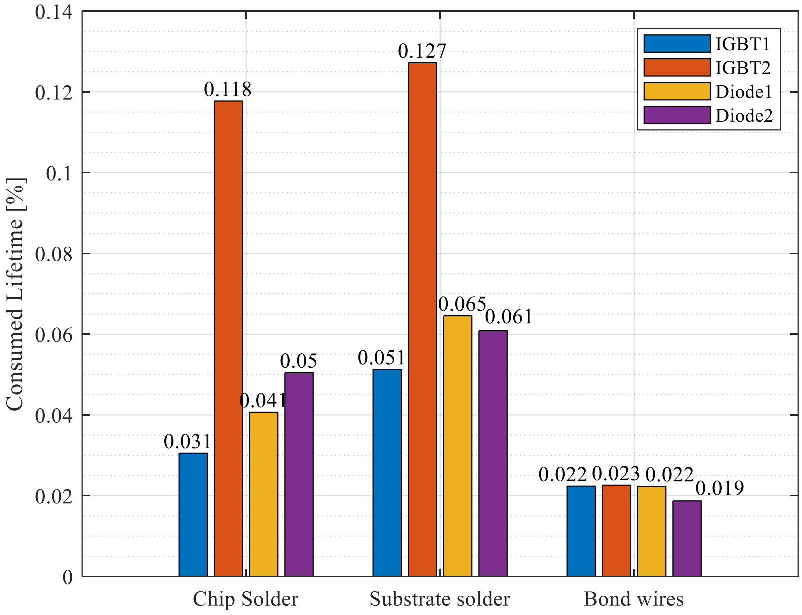


Figure 3.34. Total lifetime consumption for the P2P application

From the lifetime consumptions computed for the different elements of the semiconductors, the expected B_{10} lifetime can be calculated thanks to Eq. (3.12). This is possible as the lifetime curves employed indicate the B_{10} lifetime. This parameter indicates the time by which 10% of the elements of a population experiencing the same stress will fail. Another interpretation of this result is the time at which a single component has a 10% probability of failure. The results for the B_{10} lifetime of the semiconductors and its composing elements for the P2P application can be seen in Table 3.4.

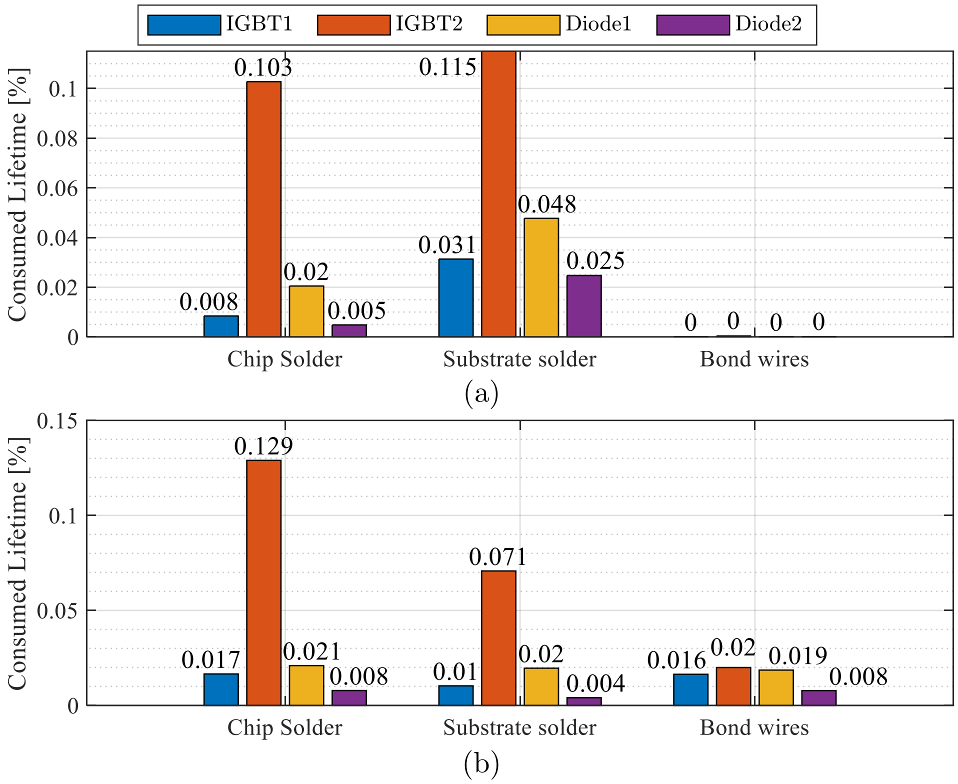
Device	Chip solder B_{10} life end [years]	DBC solder B_{10} life end [years]	Wire bond B_{10} life end [years]
IGBT 1	3275	1949	4470
IGBT 2	849	786	4423
Diode 1	2458	1549	4478
Diode 2	1981	1643	5343

Table 3.4 B_{10} lifetime estimation for the P2P application

In the case of the OWF application, the results concerning the lifetime consumption for the composing elements of the power devices in a HB-SM can be appreciated in Figure 3.35 and Figure 3.36.

In Figure 3.35 the results for both studied timescales can be seen. It can be concluded from Figure 3.35 (a) that the lifetime consumption of the substrate solder is more important in the long-term timescale, however the lifetime consumption of the chip solder is quite close. Figure 3.35 (b) depicts the results for the medium-term timescale. It can be seen on Figure 3.35 (b) that the chip solder is the most stressed element in the power devices.

Again, it can be evidenced that in both timescales the semiconductor that has a bigger lifetime consumption is the IGBT 2. As for the total lifetime consumption (Figure 3.36), it can be seen that the chip solder is more stressed under the medium-term profiles. The substrate solder is more stressed under long-term mission profiles and the bond wires are more stressed under the medium-term profiles. These behaviors can be explained since the lifetime models of the chip solder and the bond wires depend on the junction temperature, whereas the lifetime model of the substrate solder is dependent on the case temperature.



(a)

(b)

Figure 3.35. Lifetime consumption for the OWF application: (a) Long-term, (b) Medium-term

With the lifetime consumptions for the OWF application in both timescales, the total lifetime consumption was computed and then the B_{10} lifetime for the power devices in the OWF application was calculated. The results can be seen in Table 3.5.

Device	**Chip solder B_{10} life end** [years]	**DBC solder B_{10} life end** [years]	**Wire bond B_{10} life end** [years]
IGBT 1	3999	2400	6072
IGBT 2	431	538	4916
Diode 1	2411	1485	5355
Diode 2	7887	3473	1.26e4

Table 3.5 B_{10} lifetime estimation for the OWF application

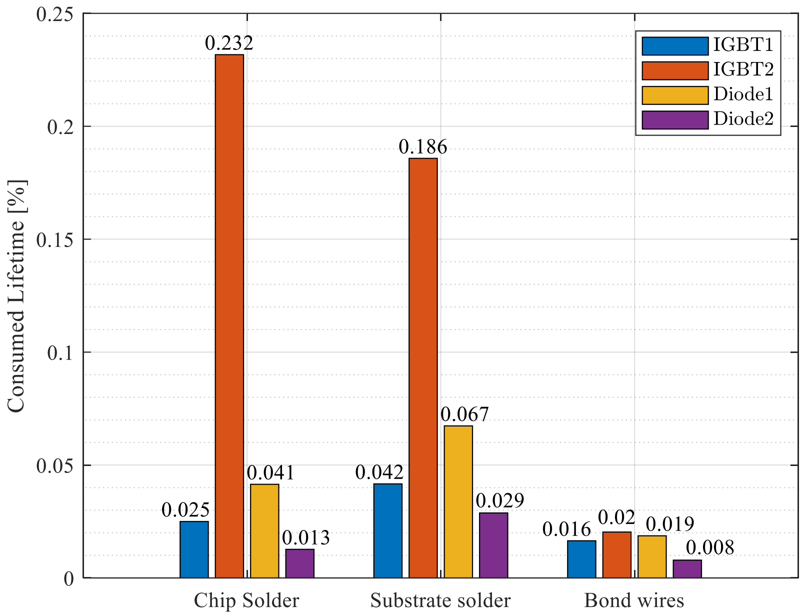


Figure 3.36. Total lifetime consumption for the OWF application

From the results seen in Table 3.4 and Table 3.5, it can be deduced that the lifetime consumption for the most stressed component (IGBT 2) is more important in the OWF application (lifetime consumption of chip solder and substrate solder). Another interesting conclusion by comparing Figure 3.36 and Figure 3.34 is that the Diode 2 is more stressed in the P2P application. This happens since the P2P application has some power reversals as seen on Figure 3.22, and during the stage where the reversals occur, the most solicited semiconductor is the Diode 2. The impact can be seen also on the B_{10} lifetime results from Table 3.4 and Table 3.5. What can be inferred from this behavior is that a larger lifetime consumption for Diode 2 can be expected if the mission profile for the P2P application has more instances of power reversals.

Finally, it is important to mention that the results depicted in this section are greatly influenced by the thermal conditions used for this study. The choice of the dimensioning of the heatsink parameters guaranteed a maximum junction temperature of 90°C for the most stressed component. In other works such as [29], [140], [160], [210], [211], higher junction temperatures are allowed for the semiconductors and since the lifetime models are also dependent on this parameter, the lifetime consumption can greatly differ. The choice of a maximum junction temperature of 90°C is more optimistic in terms of lifetime consumption and seems to be more realistic than higher junction temperatures for MMCs deployed in HVDC applications.

3.3. Methodology for reliability predictions

Reliability is defined as the ability of a system or component to perform its required functions under stated conditions for a specified time.

Reliability prediction is a major topic surrounding power electronics. These predictions are vital in the design phase, as the reliability requirements are strongly dependent on the application on which a converter is deployed.

In the case of HVDC applications, where the reliability aspect is of primary importance, the reliability of its composing elements has to be taken with the utmost care. Thus, in this section the reliability prediction of a MMC will be considered.

Two different approaches will be considered for performing the reliability predictions. In the first one, only off-the-shelf reliability indicators, provided by the manufacturers of power electronics components, will be used. In the second approach, the mission profile experienced by the converter will also be considered for performing the reliability predictions.

The probabilistic background behind the reliability predictions will be described in the next section.

3.3.1. Probability analysis

It is necessary to understand the basic functions for probability analysis in order to perform reliability predictions. These functions are described in Eqs. (3.15)-(3.18).

$$F(t) = P(T \leq t) = \int_0^t f(t)dt \tag{3.15}$$

$$f(t) = \frac{dF(t)}{dt} \tag{3.16}$$

$$R(t) = 1 - F(t) \tag{3.17}$$

$$h(t) = \frac{f(t)}{R(t)} \tag{3.18}$$

In Eq. (3.15), the expression for the calculation of the cumulative distribution function (cdf) $F(t)$ can be seen. It represents the probability that the studied element fails before some time t. The probability density function (pdf) $f(t)$ shown in Eq. (3.16), is the derivative of $F(t)$ and it represents the likelihood that a component will fail at some time t. The reliability function $R(t)$ can be seen in Eq. (3.17). It represents the probability of survival of a given element until a time t. It can also represent the availability [225].

The number of failures occurring per unit time is given by the failure rate function, otherwise known as hazard function $h(t)$ seen in Eq. (3.18). This function follows the characteristics of the bathtub curve seen in Figure 3.37. During the first portion of the bathtub curve $h(t)$ decreases, this period represents the infant mortality of the studied component. During the second portion of the curve, $h(t)$ remains constant, this is the phase of maturity of the element where only random failures can occur. The last portion of the bathtub curve shows an increasing $h(t)$, and it represents the end-of-life phase where the wear-out becomes the preponderant cause of failures. It is important to note that the hazard function $h(t)$ is not a probability.

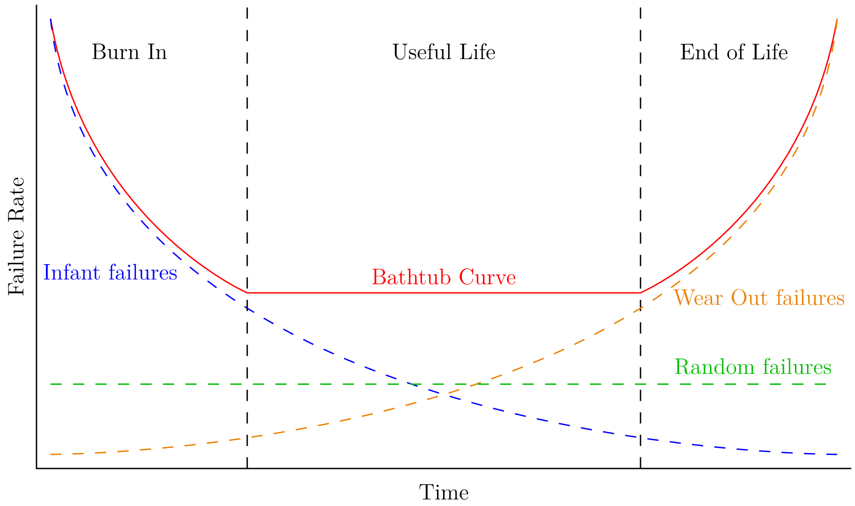


Figure 3.37. Bathtub curve

The methodology for computing system-level reliability predictions in this thesis consists of using component-level reliability functions and computing system-level reliability. This methodology is independent of the type of case study. This methodology can be depicted in Figure 3.38 and can further be expressed in Eq. (3.19). In this expression the cumulative distribution function of the system $F_{sys}(t)$ is obtained employing the individual cumulative failure distributions $F_i(t)$ of all the i^{th} elements.

$$F_{sys}(t) = 1 - \prod(1 - F_i(t)) \tag{3.19}$$

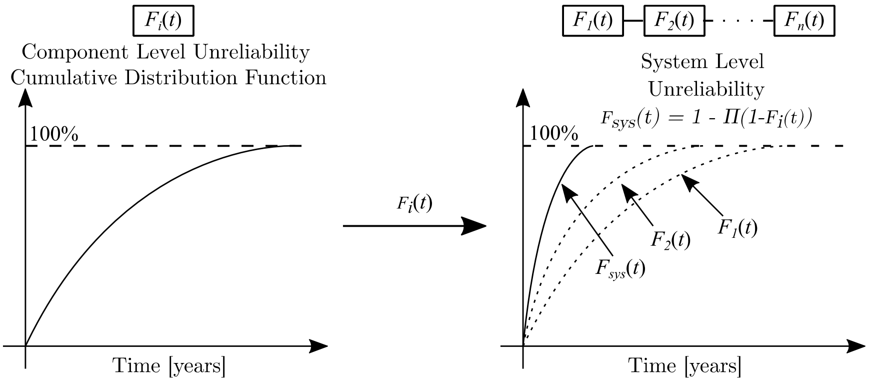


Figure 3.38. Methodology for the computation of system-level reliability

3.3.2. Reliability based on manufacturer off-the-shelf reliability inputs

In general, the manufacturers of components for power electronic systems provide reliability indicators for their products. These indicators will be useful for the end-user for making system-level reliability predictions. With these results, the design of a system can be validated and go further to the development stage.

For the MMC application, the reliability of the converter can be computed by considering the reliability of a HB-SM, which is calculated with the reliability of its composing elements (Figure 2.2). The manufacturer provides the reliability indicator in the form of the constant failure rate λ of the component. It can be expressed in Failures In Time (FIT), which is the number of failures per billion (10^9) hours as seen on Eq. (3.20).

$$\lambda = \frac{\sum FIT}{10^9} \tag{3.20}$$

The constant failure rates of the elements of a HB-SM expressed in FIT can be seen in Table 3.6 [225]. These elements include the power semiconductors, the storage capacitor and the electronic board that drives the HB-SM.

Component	FIT
IGBT	100
Capacitor	300
Electronic Board	1200

Table 3.6 Failure rates of the elements of a HB-SM [225]

Since the manufacturer only provides the constant failure rate λ of the elements as a reliability indicator, the reliability function will be calculated considering only the constant random failure portion of the bathtub curve from Figure 3.37. Thus, the Eqs. (3.15)-(3.18) can be expressed in the following form:

$$F(t) = 1 - e^{-\lambda t} \tag{3.21}$$

$$f(t) = \lambda e^{-\lambda t} \tag{3.22}$$

$$R(t) = e^{-\lambda t} \tag{3.23}$$

$$h(t) = \frac{\lambda e^{-\lambda t}}{e^{-\lambda t}} = \lambda \tag{3.24}$$

It can be seen from Eq. (3.23), that the reliability function $R(t)$ considering only constant random failures corresponds to an exponential distribution. It can also be evidenced from Eq. (3.24), that the hazard rate remains constant for this analysis and is given by the parameter λ.

When all the elements of a system are modelled employing the exponential distribution, the failure rate of the system can be computed by adding the failure rates of its composing elements. In the case of a HB-SM, its failure rate λ_{SM} will be obtained with Eq. (3.25). Consequently, the reliability of the HB-SM $R_{SM}(t)$ can be calculated with Eq. (3.26).

$$\lambda_{SM} = 2\lambda_{IGBT} + \lambda_{capa} + \lambda_{board} \tag{3.25}$$

$$R_{SM}(t) = e^{-\lambda_{SM} t} \tag{3.26}$$

The reliability of the HB-SM and its composing elements is depicted in Figure 3.39. This information will then be used for performing reliability calculations at converter level and also for performing redundancy computations.

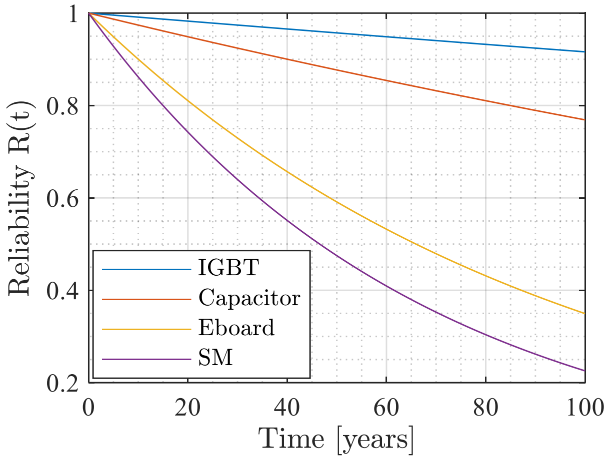


Figure 3.39. Reliability of a HB-SM and its composing elements considering off-the-shelf reliability indicators

3.3.3. Reliability based on experienced mission profile

In this thesis the results from the profile-based lifetime estimation will be used for estimating the reliability functions of the semiconductors of a HB-SM. The approach developed in this research is a more simplified approach than the one traditionally employed for performing reliability predictions, where Monte Carlo simulations need to be employed and variations to the lifetime models and load profiles are required for making approximations to a Weibull distribution [213], [226].

As it was seen in section 3.2.5.2, the lifetime consumption for the most stressed component was more important in the case of the OWF application. Therefore, only the OWF application will be considered for the reliability calculations performed in this section. Then, the reliability of the whole SM will be calculated by considering the reliability functions of the remaining components of the SM (capacitor and electronic board) as it was seen on Figure 3.38.

Since the storage capacitor and the electronic board were not subjects for the lifetime estimation study, the reliability functions corresponding to these elements will be the exponential reliability functions calculated for the constant random failure portion of the bathtub curve of Figure 3.37.

As it was mentioned previously, the calculation of the reliability functions of the semiconductors will be performed employing the results of the lifetime estimation methodology. Since the B_{10} lifetime for the different parts of a semiconductor device were calculated, this information can be used for making an approximation to an element cumulative distribution function $F_k(t)$. Consequently the CDF of all the k elements composing the devices (chip solder, substrate solder and bond wires) will be employed to calculate the device unreliability function $F_{dev}(t)$ as expressed in Eq. (3.27) and as depicted in Figure 3.40.

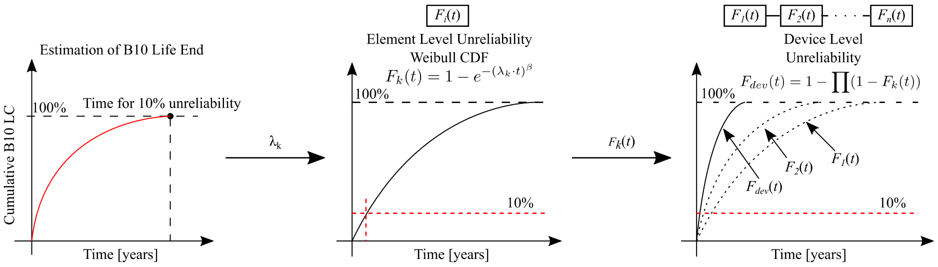


Figure 3.40. Methodology for calculating device level unreliability $F_{dev}(t)$

$$F_{dev}(t) = 1 - \prod\left(1 - F_k(t)\right), k \ \in \{\text{chip solder, dbc solder, bond wire}\}, \quad dev \ \in \{\text{T1, T2, D1, D2}\} \tag{3.27}$$

Since the models [215] employed for the calculation of the B_{10} lifetime of the semiconductors are fitted employing the two parameter Weibull distribution [227] the reliability related functions described in section 3.3.1 will be expressed according to Eqs. (3.28)-(3.31) for the k elements of the power devices. In this case, the parameter λ no longer represents a constant failure rate but a fitting parameter. Eqs. (3.28)-(3.31) can also be expressed in terms of the scale parameter σ of the Weibull distribution.

$$F_k(t) = 1 - e^{-(\lambda_k t)^\beta} = 1 - e^{-(t/\sigma_k)^\beta} \tag{3.28}$$

$$f_k(t) = \beta e^{-(\lambda_k t)^\beta} {\lambda_k}^\beta t^{\beta-1} = \beta e^{-(t/\sigma_k)^\beta} {\sigma_k}^{-\beta} t^{\beta-1} \tag{3.29}$$

$$R_k(t) = e^{-(\lambda_k t)^\beta} = e^{-(t/\sigma_k)^\beta} \tag{3.30}$$

$$h_k(t) = \frac{\beta e^{-(\lambda_k t)^\beta} {\lambda_k}^\beta t^{\beta-1}}{e^{-(\lambda_k t)^\beta}} = \beta {\lambda_k}^\beta t^{\beta-1} = \beta {\sigma_k}^{-\beta} t^{\beta-1} \tag{3.31}$$

In order to fully calculate the reliability of each k element of the device the only information available is the B_{10} lifetime or LF_k, which is the time at which the CDF is equal to 10% as expressed in Eq. (3.32).

$$F_k(LF_k) = 0.1 \tag{3.32}$$

Thus, it is necessary to calculate the fitting parameter λ_k as well as the shape parameter β to fully be able to map the reliability of each element and consequently of each device. As the shape parameter β is an indication of the variance of the Weibull distribution and also represents the current stage on the bathtub curve (e.g. $\beta < 1$ corresponds to the burn in stage, $\beta = 1$ corresponds to the useful life stage and $\beta > 1$ corresponds to the wear out phase), several shape factors β will be tested as carried out in [30]. Therefore, with the LF_k information and the values of β, a corresponding λ_k can be computed with Eq. (3.33) for each β evaluated.

$$\lambda_k = -\frac{\left[\ln\left(1 - F_k(LF_k)\right)\right]^{\frac{1}{\beta}}}{LF_k} = -\frac{\left[\ln(1 - 0.1)\right]^{\frac{1}{\beta}}}{LF_k} = -\frac{\left[\ln(0.9)\right]^{\frac{1}{\beta}}}{LF_k} \tag{3.33}$$

Finally, once the CDF $F_k(t)$ is computed for all the internal elements of a semiconductor, the CDF of each device $F_{dev}(t)$ is obtained with Eq. (3.27). This will eventually allow the calculation of the CDF of the HB-SM $F_{SM}(t)$ with Eq. (3.34). Consequently, the reliability of the SM $R_{SM}(t)$ is calculated with Eq. (3.35).

$$F_{SM}(t) = 1 - \prod\left(1 - F_m(t)\right), m \in \{\mathrm{T1, T2, D1, D2, Capacitor, Eboard}\} \tag{3.34}$$

$$R_{SM}(t) = 1 - F_{SM}(t) \tag{3.35}$$

The results corresponding to a shape factor $\beta = 2.5$ for all the elements of the most stressed semiconductor device can be seen in Figure 3.41 (a). Figure 3.41 (b) depicts the reliability of the semiconductors using the same shape factor. Figure 3.41 (c) shows the reliability functions of the remaining elements of a HB-SM, as well as the reliability of the SM itself.

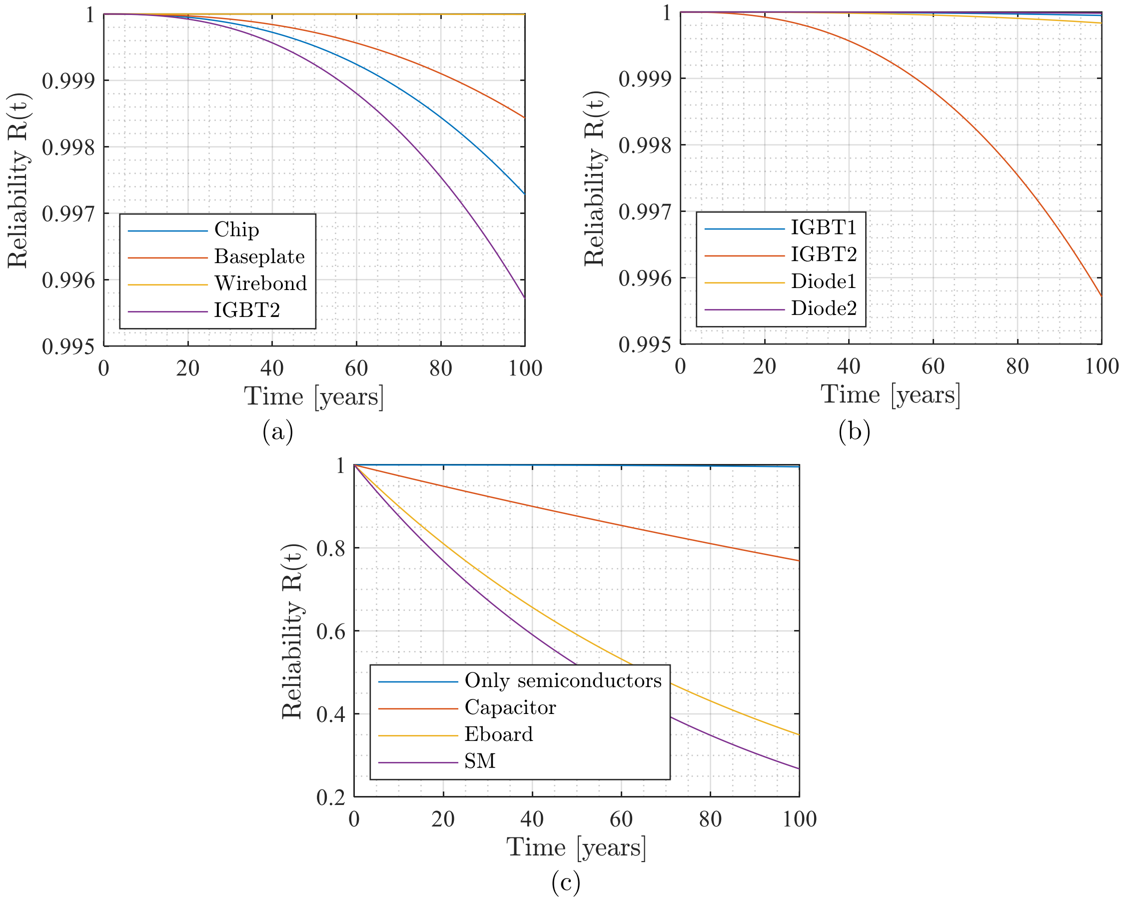


Figure 3.41. Reliability functions with a shape factor $\beta = 2.5$: (a) Inner elements of IGBT 2, (b) Semiconductors, (c) Components of a HB-SM

It was mentioned previously that many β parameters were tested in this thesis. As a shape factor below 1 coincides with the infant-failure period of semiconductors, values below 1 weren't employed in this study. This was done since it is the role of the semiconductor manufacturers to solve the causes leading to infant failures. The β values considered in this study are 1, 1.5, 2, 2.5, 5 and 10. The reliability functions for the HB-SM corresponding to these β values are depicted in Figure 3.42.

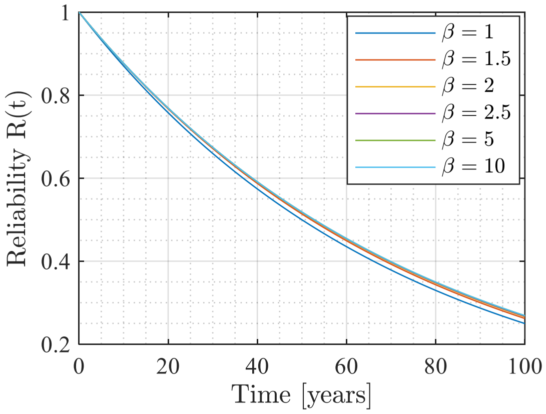


Figure 3.42. Reliability functions of a HB-SM for different shape parameters β

3.4. Methodology for redundancy computations

As HVDC systems are one of the main enablers of bulk-power transmission over long distances [5], [228], power transmission systems are pushing towards the rapid development of suitable technologies for uninterrupted service. According to the ENTSO-E [23], TSOs and other end-users of HVDC should consider that improved reliability (e.g. decreasing 1-2 trips per year on average) and improved availability (e.g. decreasing 1-2 outage days per year on average) can bring significant cost savings to TSOs and/or society. The availability of the HVDC system depends on the individual availabilities of all the assets comprised in the power transmission chain, as well as any planned of unplanned outages of the system for maintenance [225]. One of the assets with the biggest impact on the overall availability of the system is the converter station. Hence, it is important to accurately determine its availability.

Moreover, in the case of offshore substations the cost of maintenance is much more elevated than in onshore substations. This is mainly due to the fact that specialized repair vessels are needed for offshore maintenance [229], [230]. An additional problem concerns the high demand of the repair vessels, consequently planned maintenance is favored in order to keep low operational costs [231].

The preferred topology for the connection of the offshore wind farms to onshore substations are VSC-HVDC and more particularly MMC. One of the main advantages of the MMC is its modularity. This modularity is necessary for the normal operation of the converter. Having several conversion stages per arm allows to have less distortions on the AC waveforms and reduce the size of filters, thus allowing a diminution of the footprint of the converter [232].

Another crucial advantage of the modularity, is the possibility to employ additional redundant stages or redundant submodules. These stages will assure that the converter remains operational between maintenance interventions [233]. Concerning the control of the redundant SMs, two strategies have been found in the literature [232]–[234].

In the first strategy, the redundant SMs are in a standby state, where they are electronically bypassed and only become active when another SM fails [225]. This type of redundancy is otherwise known as cold redundancy. The other strategy for redundancy management is known as hot redundancy. In this method all SMs are involved during the converter operation. This method has the additional advantage of avoiding the operation of a mechanical switch for the insertion of a SM and the charging of its corresponding capacitor. Hence, hot redundancy is widely adopted in MMCs [235], [236], and it will be the only approach for redundancy considered in this study.

The methodology for computing the redundancy requirements of an MMC arm is based on the calculation of the availability of the arm by the end of the expected lifetime of the converter. In this study a target useful life of 40 years is considered, as this is the life expectancy of VSC-HVDC transmission links [237].

Given the criticality of the application, the availability requirement for an offshore link is set to 98% [225]. In order to attain this target HVDC system availability, a target availability of 99.5% is set for an MMC arm. Additionally, a fixed period of two years will be considered between maintenance operations.

The arm availability is calculated considering the reliability of the individual HB-SMs composing the arm, which was the main result of section 3.3. It is also worth mentioning that two approaches were considered for performing redundancy computations. They will be described in the following lines.

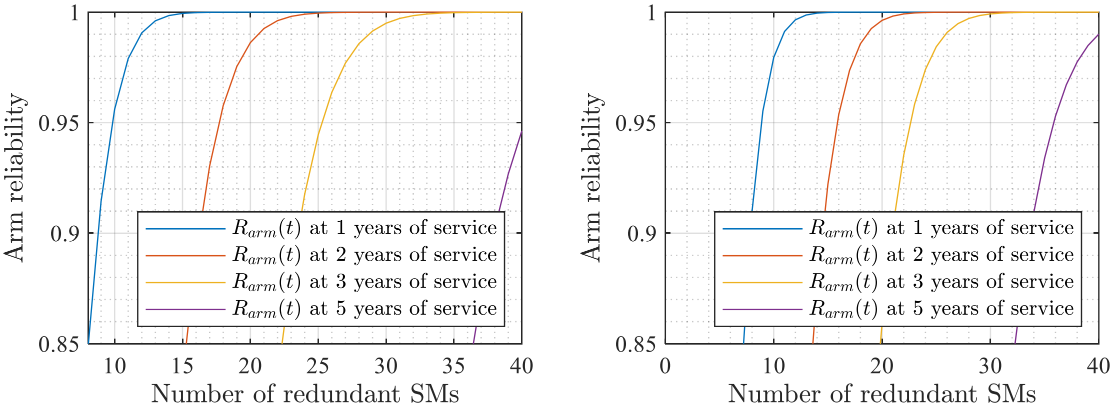
3.4.1. Analytical approach for redundancy computations

The first approach for performing the redundancy computations is an analytical approach that employs the binomial distribution (k-out-of-n model) [238] seen in Eq. (3.36). It is also worth considering that the availability of the arm can be approximated to the reliability calculated with Eq. (3.36) as the binomial distribution represents a discrete probability evaluated at each maintenance interval.

$$R_{arm}(t) = \sum_{k=0}^{N_{red}} \frac{(N_{min} + N_{red})!}{k!\,(N_{min} + N_{red} - k)!} [1 - R_{SM}(t)]^k [R_{SM}(t)]^{N_{min}+N_{red}-k} \tag{3.36}$$

In Eq. (3.36) N_{min} represents the minimum number of HB-SM required for arm operation, N_{red} represents the number of redundant SMs evaluated. This expression can be understood as all the possible combinations that yield a maximum number of failed SMs equal to N_{red}, but assuring that at least N_{min} SMs will survive, thus still allowing the MMC arm to work.

Applying Eq. (3.36) to the HB-SMs reliability distributions $R_{SM}(t)$ from Figure 3.39 and Figure 3.42 yields the results for the arm reliability $R_{arm}(t)$. The results are depicted in Figure 3.43. Figure 3.43 (a) shows the $R_{arm}(t)$ when using manufacturer reliability indicators and Figure 3.43 (b) shows the results when using the profile-based methodology and $\beta = 2.5$. The calculations were performed for an MMC that requires at least 400 HB-SMs to guarantee its operation.



(a) (b)

Figure 3.43. Arm reliability $R_{arm}(t)$ using: (a) Manufacturer information, (b) OWF mission profile, $\beta = 2.5$

The results from Figure 3.43 depict $R_{arm}(t)$ at 1, 2, 3 and 5 years of service. As the interval chosen for the maintenance interventions was chosen to be 2 years, only the results at 2 years of service need to be considered. The results using manufacturer information and the profile-based methodology can be synthesized in Table 3.7.

Case Study	Manuf. Data	OWF profile $\beta = 1$	OWF profile $\beta = 1.5$	OWF profile $\beta = 2$	OWF profile $\beta = 2.5$	OWF profile $\beta = 5$	OWF profile $\beta = 10$
N_{red}	22	21	20	20	20	20	20

Table 3.7 Number of redundant SMs for a target availability of 99.5%

This method gives a first hint on the number of redundant SMs required for achieving the target arm availability throughout the operating life of the MMC. However, this method has a critical drawback. The binomial approach cannot be employed when the SMs have different probabilities of survival. In other words, the replacement of out-of-order SMs during the maintenance operations pose a major conflict for the calculation of the redundancy requirements with the binomial approach.

Moreover, this method approximates the minimum redundancy required to the redundancy needed at the first maintenance intervention (e.g. 2 years). Thus, this method neglects the effect of further ageing of HB-SMs (wear-out), and does not take into account the reliability of SMs by the end of the useful life of the converter (e.g. 40 years).

3.4.2. Markov Chain approach for redundancy computations

In order to circumvent the problems of the binomial approach, such as the replacement of faulty HB-SMs during maintenance operations and verifying the arm availability by the end of its target lifetime, a method based on the use of a Markov chain shown in Figure 3.44 was developed. This method also makes use of Monte Carlo simulations to emulate the lifetime of the MMC arm.

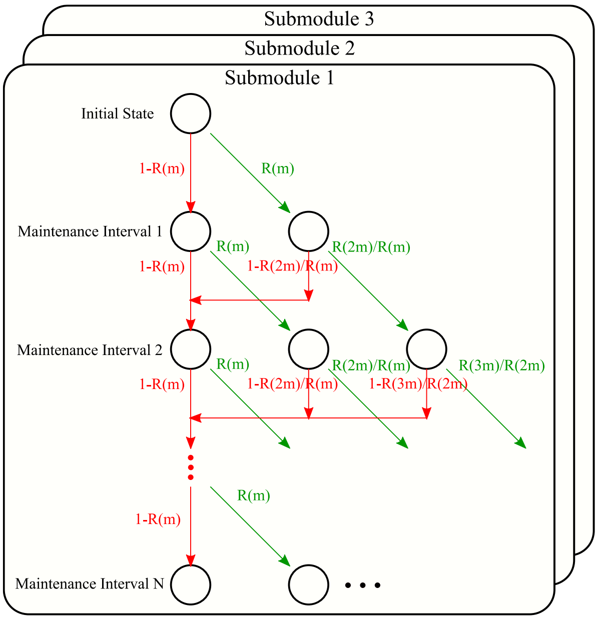


Figure 3.44. Markov chain for calculation of $R_{arm}(t)$ for a target mission time of 40 years

In the Markov chain shown in Figure 3.44, m represents the time between maintenance interventions. If a SM has survived two maintenance stops, the probability of survival/failure for the next maintenance operation, considers the fact that the SM has already survived to two previous maintenance intervals as expressed by the subscript $2m$. Equally, if the SM has survived to more maintenance stops (green branches), this is considered for further calculations. If a SM fails (red branches) its probability of survival R is reset to 1, which is similar to replace the SM by a new one.

With the Markov Chain from Figure 3.44 different redundancy levels were tested. For each redundancy level 1000 arm lifetimes were simulated. The minimum number of redundant SMs to be installed in an arm should guarantee an availability of 99.5% by the end of the target mission life of the arm (i.e. 40 years).

The time interval for the maintenance is set to two years. At each maintenance period, a random value between 0 and 1 is used to describe the failure/survival of each SM in the arm, the random value follows a uniform distribution. If this value is below the probability of survival of the SM, then it can be considered that the SM has survived the period before the maintenance intervention. However, if this value is bigger than the probability of survival, the SM has failed between maintenance interventions.

If the number of failed SMs during the maintenance stop is smaller than the number of redundant SMs installed, the arm has survived that particular interval and the failed SMs are replaced with new ones. This process is carried out at each maintenance intervention and is stopped if the arm survives until its target mission life. If by any chance the number of failed SMs is bigger than the number of redundant SMs installed at a given maintenance period, the arm has failed the ongoing simulation. Finally, the availability is approximated to the number of arm survivals for each redundancy level tested. Figure 3.45 illustrates the results obtained with the Markov Chain approach. The results depicted in Figure 3.45 can be resumed in Table 3.8.

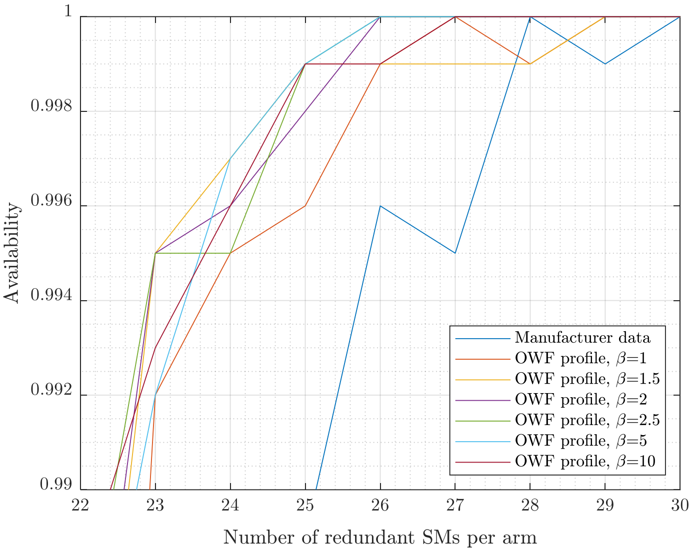


Figure 3.45. Availability of an MMC arm vs. Number of redundant SMs

Case Study	Manuf. Data	OWF profile $\beta = 1$	OWF profile $\beta = 1.5$	OWF profile $\beta = 2$	OWF profile $\beta = 2.5$	OWF profile $\beta = 5$	OWF profile $\beta = 10$
N_{red}	26	24	23	24	23	24	24

Table 3.8 Number of redundant SMs for a target availability of 99.5%

3.4.3. Discussion on the redundancy computation methodology

The results of the redundancy computation methodology reflect the results for the reliability predictions from section 3.3. It can be clearly evidenced from Table 3.7 and Table 3.8 that the redundancy requirements when employing the manufacturer reliability indicators yields the worst-case scenario. As it was mentioned in section 3.2.5.2, the thermal conditions imposed to the profile-based methodology greatly affect the calculations for the reliability of a SM and consequently for the arm availability computations.

It can also be seen from Table 3.7 and Table 3.8, that the shape factor β has almost no impact on the final redundancy estimations. This can be explained as the failure rates of the other elements of the HB-SM (storage capacitor and electronic board), are much higher compared to the failure rates of the semiconductors in both case studies.

It was also mentioned previously that when employing the Weibull distribution, the shape parameter β allows the mapping of the stage on the bathtub curve of the studied element. It was also indicated that only shape parameters bigger or equal to one were evaluated in this study. The main reason behind the lack of a noticeable loss of reliability in spite of the different β evaluated is that the acceleration in the reliability decline happens much after the target mission time of the converter. An example concerning the reliability of the chip solder of IGBT 2 can be seen in Figure 3.46.

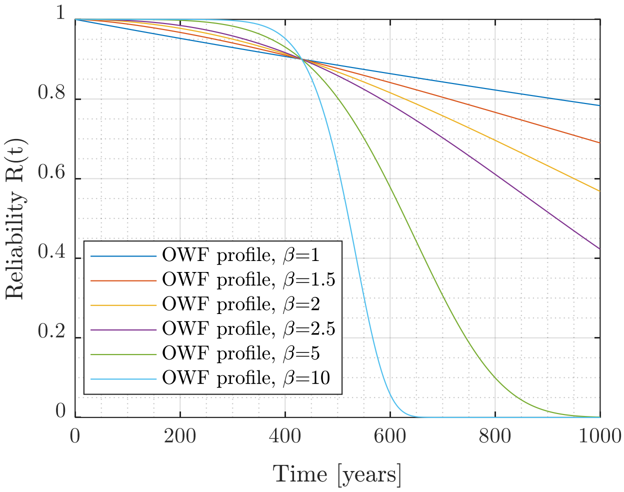
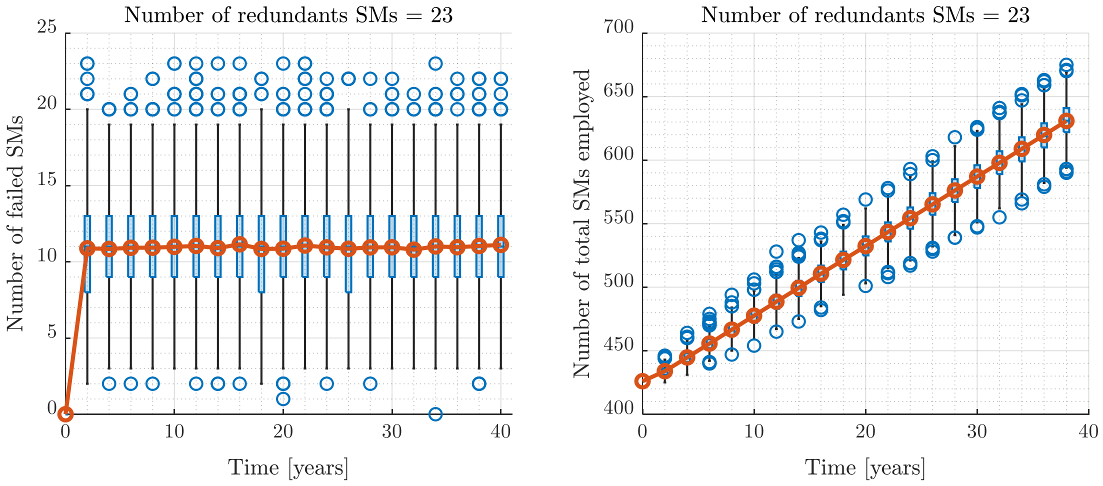


Figure 3.46. Reliability of the chip solder of IGBT 2 for different β

The reliability functions seen on Figure 3.46 are obtained considering a fixed time span for a loss of reliability of 10%, which corresponds to the B_{10} lifetime definition in [215]. The fixed time span for the loss of reliability was obtained with Eq. (3.12) described in section 3.2.3.3.

Another noticeable result from the redundancy computations based on the Markov Chain and the Monte Carlo simulations is the estimation of the number of failed SMs at each maintenance period. This result allows for the calculation of the total number of SMs employed throughout the target mission time of the converter (i.e. 40 years). The results depicting the average number of failed SMs at each maintenance period can be seen in Figure 3.47 (a) and the approximated number of SMs employed during the operating life of the converter can be seen in Figure 3.47 (b). Both results correspond to the profile-based inputs when employing a $\beta = 2.5$.



(a) (b)

Figure 3.47. (a) Number of failed SMs per arm at each maintenance intervention, (b) Number of total SMs employed during the operating life of the arm (OWF profile, $\beta = 2.5$)

In Figure 3.47 (a) the average number of failed SMs per maintenance intervention can be seen. It is important to notice that the maximum value is equal to the number of installed redundant SMs (i.e. 23 SMs). If this number would have been higher, the MMC arm wouldn't have survived and the whole converter would have stopped working. Also, from Figure 3.47 (a), it can be seen that the average number of SMs failed per maintenance period is 11, but the results can have a large variance.

In Figure 3.47 (b) the evolution of the total number of employed SMs in an arm can be noticed. The total number of SMs per arm employed is indeed much higher than the initial number of SMs per arm installed at the beginning of converter operation. The studied MMC arm requires only 400 SMs to operate, it requires an additional 23 SMs for accomplishing an availability of 99.5% throughout its operating life. However, the total number of SMs employed by the arm will be somewhere around 630 SMs. This means that the arm requires more than 200 additional SMs than the ones with which started its operation. This result is not negligible by any means and can have a major impact on the operating costs of the conversion station. Moreover, as the MMC has six arms, the total number of SMs employed in the whole converter during its operational life can ascend to 3800 SMs in average. This number is much larger to the initial 2400 SMs required for MMC operation. A comparison between the total number of SMs employed in the studied cases can be seen in Figure 3.48.

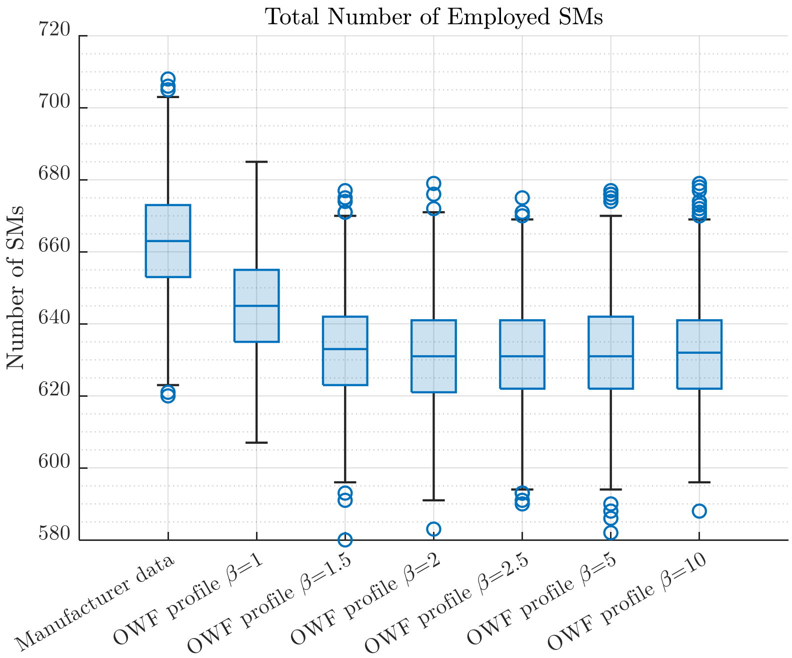


Figure 3.48. Comparison between the number of employed SMs for different case studies

As mentioned previously in this section, the shape parameter β employed for the profile-based redundancy calculations does not notably affect the number of redundant SMs as seen on Figure 3.45 and Table 3.8. However, when $\beta = 1$ a slight impact on the total number of employed SMs can be noticed in Figure 3.48. The average number of employed SMs in this case is 645 compared to the 631 SMs when employing the profile-based inputs where $\beta > 1$. It is worth reminding that when $\beta = 1$, the Weibull distribution behaves as an exponential distribution. It was previously shown in Figure 3.46 that with a higher value of β, the acceleration in the decline of reliability is much steeper, but it happens much after the target mission time for the converter. This means that before this sudden decline in the reliability distributions, the distributions with higher β values will have higher reliability values, thus impacting the redundancy computations as evidenced in Figure 3.48.

Finally, the results shown in Figure 3.48 indicate that the manufacturer off-the-shelf reliability indicators yield the worse results in terms of total number of SMs employed. A simple exponential distribution is used to model the SM reliability in this particular case. This information correlates with the results for the calculation of $R_{SM}(t)$ in section 3.3, since the reliability distribution employing off-the-shelf reliability indicators is more pessimistic than the reliability of a SM employing the profile-based methodology.

3.5. Chapter conclusion

In this chapter three different methodologies were presented.

The first methodology developed is the lifetime estimation methodology. All the required stages for performing the lifetime estimations were detailed in section 3.2. A particular contribution developed in this methodology concerns the use of a model-based extrapolation technique. This technique showed to be very useful for performing lifetime consumption calculations after running the semiconductors thermal profiles through the rainflow counting algorithm and for employing the manufacturer lifetime models. Subsequently, the methodology was employed for studying 2 different types of mission profiles. The lifetime consumption proved to be more important in the OWF application than in the P2P application when analyzing the lifetime consumption of the most stressed component.

The second methodology developed in this chapter concerns the reliability predictions of a HB-SM. These predictions were performed by employing two different types of inputs: manufacturer off-the-shelf indicators and profile-based lifetime consumptions issued from the lifetime estimation methodology.

In the predictions using manufacturer off-the-shelf indicators a traditional straightforward technique was used for calculating the HB-SM failure rate λ_{SM} by adding the individual failure rates λ_i of the composing elements of the SM. Additionally, when using this type of input an exponential distribution was employed to model the reliability functions of all the elements of the SM and the SM itself.

In the reliability predictions using profile-based lifetime consumptions as inputs, only the results of the OWF application were retained. This methodology proposes a simplified approach compared to the existing methods in the literature. Several shape factors were evaluated to map the reliability of the semiconductor devices, but the exponential distribution was retained for performing the calculation of the reliability of the remaining elements of the HB-SM.

The third methodology developed in this chapter concerns the redundancy computations for attaining a target availability value. Once again, the off-the-shelf inputs and the profile-based inputs for the OWF application were used for developing this analysis. The redundancy computations were performed using two different types of approaches. The first approach gives analytical results for the computation of redundant SMs required. However, these results can only be considered as initial approximations as they don't consider the wear-out of the SMs nor its replacement.

In order to have a more realistic method to compute the redundancy levels required a methodology based on a discrete Markov Chain and Monte Carlo simulations. The results with this newly developed methodology are logical as the number of redundant SMs obtained is slightly higher than the number of redundant SMs employing the analytical approach based on the binomial distribution.

Moreover, the Markov-based approach allowed for the calculation of the number of failed SMs before each maintenance intervention and allowed the simulation of its replacement by brand new SMs, which cannot be made with the analytical method. An approximated total number of SMs used per arm can also be computed thanks to this methodology.

It is worth mentioning that the study of the number of failed SMs and total employed SMs opens many perspectives for future research. Some might involve the choice of alternative maintenance strategies concerning the replacements of healthier SMs in order to optimize the number of redundant SMs installed or reducing the total number of SMs employed throughout the active life of the converter.

It can also be concluded in this chapter that the lifetime estimation methodology and the reliability prediction can be applied to different types of topologies.

Finally, it is worth mentioning that the results in which a mission profile was employed can be greatly influenced by the thermal conditions fixed for the converter. It can easily be inferred that if higher junction temperatures are allowed for the semiconductors, they will have a shorter expected lifetime. Consequently, this result will impact the reliability predictions as well as the redundancy computations.

The results obtained in this chapter are merely based on theoretical information, it is thus necessary to perform real tests for addressing the reliability of semiconductors and validating the results obtained in this chapter. It is for this reason that the next chapter will deal with the practical implementation of a test bench for performing real reliability assessments of IGBT devices.

4. Power Cycling Test

4.1. Introduction

In the previous chapter several methodologies have been developed. However, in order to be able to validate those results, an experimental setup must be conceived and implemented testing IGBT modules under various thermal conditions. The experimental setup must be able to activate the more representative failure mechanisms of the semiconductor modules and more particularly those that are characteristic of the studied application (HVDC-MMC). The test bench will also serve for validating the use of temperature sensitive electrical parameters (TSEPs) for tracking the ageing process of IGBTs and will also help validate the ageing laws used in the determination of the RUL.

In this chapter, a brief review on experimental setups concerning the ageing of IGBT modules is carried out. Consequently, the choice of an ageing test bench topology is chosen.

Afterwards, this chapter describes the development of the ageing test bench. The development process involves several simulations, which are used for the validation of the thermal constraints imposed to the semiconductor devices.

A central topic developed in this chapter is the instrumentation required for monitoring the experimental set up. In particular, the emphasis has been put on the development of measurement means for the estimation of the junction temperature, as well as for determining the state of health (SOH) of the device. This is an essential step for monitoring the ageing process of the device.

Finally, the integration of all the elements of the ageing test bench will be shown as well as some experimental results validating the correct behavior of the cycling test bench as well as the instrumentation and the health monitoring approaches.

4.2. Motivation for performing power cycling tests

Several different tests exist for assessing the reliability of semiconductor devices. Each of those tests activates a very particular stressor [239] and there are some that allow the analysis of multi-stressor inputs for semiconductor reliability [240]. Some of the most well-known tests for semiconductor reliability can be seen on Table 4.1 [241], [242]. The tests seen on Table 4.1, correspond to the qualification tests performed by a major IGBT module manufacturer.

As it was seen on previous chapters, the main failure mechanisms for IGBT modules are related to the thermal stress experienced by the semiconductor device. In this context, the most pertinent reliability tests are the temperature and power cycling tests [239], [243]–[245].

The temperature cycling test, otherwise known as thermal cycling test, deals with the temperature excursions experienced by the baseplate of the IGBT modules. This particular type of test mainly puts stress on the soldered joints between the DBC substrate and the module baseplate [246]. The duration of the cycles experienced in this type of test can last several minutes as seen on Figure 4.1.

	Qualification	Test Method	Test Conditions	Qualification Standard
Environmental Assessment	Passive Cycling	IEC60068-2-14	$\Delta T = 80K$ $T_{min} = 25°C\ (\pm 5)$ $2\ min < t_{cycle} < 6\ min$	20000 cycles for MMC base plate 5000 cycles for copper base plate
	Temperature Cycling	IEC60068-2-14	$T_{stg\ min}$ to $T_{stg\ max}$ $T_{dwell} \geq 1\ hour$ Transfer time = $30\ s$	100 cycles
	Vibration	IEC60068-2-6	$f = 55$ to $500\ Hz$ Acceleration = $10g$	6 hours total 2 hours in each of 3 mutually perpendicular axes
	Mechanical Shock	IEC60068-2-27	Acceleration = $20g$ Pulse width = $20\ ms$, half sine	5 shocks in both positive and negative direction of 3 axes
	Salt Mist	IEC60068-2-11	Ka Test	168 hours
	Low Temperature Storage	IEC60068-2-1	$T_{amb} = T_{stg\ min}$	1000 hours
	High Temperature Storage	IEC60068-2-1	$T_{amb} = T_{stg\ max}$	1000 hours
	High Humidity High Temperature (H3TRB)	IEC60749-5	$T_{amb} = 85°C$ Relative Humidity $= 85\%$ $V_{ce} = 80\ V$ $V_{ge} = 0\ V$	1000 hours
Electrical Assessment	High Temperature Gate Bias (HTGS)	-	$T_j = T_{max}$ $V_{ge} = 20\ V$ V_{ce} = short	1000 hours
	High Temperature Reverse Bias (HTRB)	-	$T_j = T_{max}$ $V_{ce} = 0.8 \cdot V_{ce\ max}$ V_{ge} = short	1000 hours
	Power Cycling	-	$\Delta T = 60/50K$ $T_{max} = Tj_{max}$ $2\ s < t_{cycle} < 6\ s$	1M cycles for $\Delta T = 50K$ 400k cycles for $\Delta T = 60K$

Table 4.1 IGBT qualification tests [241]

On the other hand, power cycling tests deals with the temperature variations experienced by the chip-junction temperature at relatively short intervals in a timeframe of seconds [246]. This type of test activates the main failure mechanisms surrounding the chip connections such as the bonding wires and the die attach. A typical power cycling test protocol can be seen on Figure 4.1.

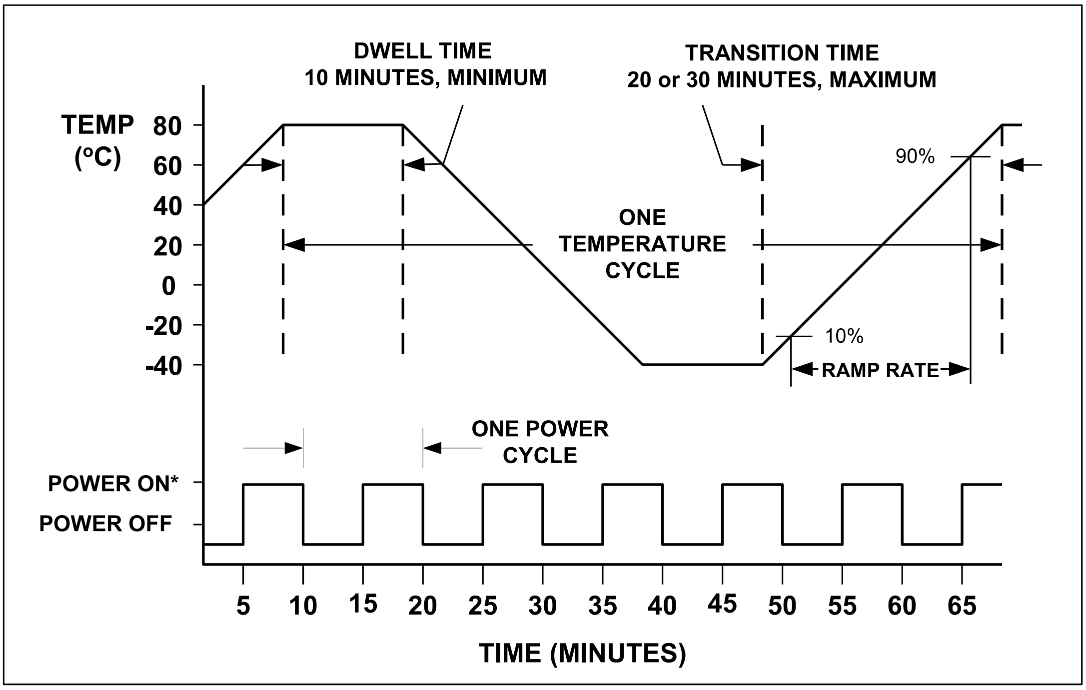


Figure 4.1. Typical power and temperature cycle test condition [243]

Another important characteristic to consider concerning the cycling tests is that, in thermal cycling, the heating source is external (heating plate or other) [247] and that, at all moments during this test, the case temperature T_c is equal to the junction temperature T_j. In the case of the power cycling test, the heating source is the semiconductor device. In the power cycling test a current is applied to the component, this current produces internal losses in the device [247] and finally the losses are translated to a rise in the device temperature. During the power cycling test, the junction temperature T_j can be different from the case temperature T_c.

As the power cycling test includes the thermal fluctuations originated by the conduction of the semiconductor devices, this test is more representative of the nominal operation of power converters. The thermal cycling test is relevant to converter operation when there are start/stop cycles or when there are environmental conditions that heavily impact the case temperature of the semiconductor.

In real-life HVDC MMC applications, the MMC valve halls are subjected to controlled environmental conditions. For instance, the thermal cooling fluid employed in the cooling system has a fixed temperature and the average heatsink temperature of all the HB-SMs is controlled [248]. Given these operating conditions, a power cycling test is more relevant to the studied application, since the cycling in this application is mainly due to load variations. Hence, this chapter will only focus on the implementation of power cycling tests for assessing the reliability of IGBT modules.

4.3. Review of power cycling testing methods

As mentioned in [249], the power cycling (PC) test is an important and efficient method to assess the reliability performance of semiconductor modules related to packaging technology with respect to thermal stress [42], [247], [250].

The PC test allows the study of the different failure mechanisms due to thermal stress, experienced by the power device modules [62], [108], [251]. Moreover, the PC test is a cornerstone for the development of new designs and packaging materials for power device modules [250], [252]–[254]. Additionally, the PC test can be employed for developing lifetime models based on its results [215], [144], [99], [255], [163], [256], [257] and it can finally be used for design for reliability by performing lifetime estimations of power modules under real-life converter mission profiles [154], [159], [160], [258]–[260].

In order to have relevant PC test results, it is necessary that tests are performed in realistic operating conditions of a device under test (DUT) and that the monitoring of the state-of-health (SOH) is conducted [249]. These requirements demand the implementation of measurement circuits and schemes for the tracking of precursor parameters or damage sensitive electrical parameters (DSEPs) [170], [249], [261]. The most relevant failure precursors and their failure criteria were already seen in Table 1.8. By implementing the online monitoring of the failure precursors, PC tests can run continuously, without the need for start/stop sequences. Moreover, online monitoring allows for the stoppage of the PC testing before the occurrence of failures, which can lead to the destruction of the PC test bench [249].

Several studies involving PC test circuits can be found in the literature [62], [99], [108], [170], [171], [262]–[270]. Moreover, all of the testing circuits can be classified into two different schemes [49], [170], [249], [261], [271], [272]: DC and AC power cycling. Both power cycling schemes will be detailed in the following paragraphs.

4.3.1. DC power cycling

Several research works have dealt with the study of reliability of semiconductor devices with the help of DC power cycling circuits [42], [271], [273]–[275]. This type of test is considered as the simplest for practical implementations, since the monitoring of the failure precursors is easier to carry out [49]. This is the main reason why semiconductor manufacturers adopt DC PC test platforms. Also, most of the work on lifetime testing and degradation analysis have been performed on DC test benches [40], [42].

Figure 4.2 (a) gives an insight at the circuit setup employed for this type of test. In this type of setup, the gate of the DUT is always polarized by applying of a constant DC voltage (e.g. 15 V) with the help of an external voltage source. This setup also uses a current source, which provides a constant DC current, responsible for the DUT's temperature increase by its conduction losses. Once the target junction temperature is reached, the current injection is stopped, this action can be achieved by using an external switch. The power device is cooled back to the reference temperature, when the load current source is disconnected. The cooling task can be performed with the help of an external cooling system. Once the reference temperature for the PC protocol is reached, the load current is reconnected to repeat the heating cycle. The whole heating and cooling sequence will intuitively have a period t_{cycle} with duty cycle t_{on}/t_{cycle}, where t_{on} is the load pulse duration. Figure 4.2 (b) depicts the waveforms corresponding to the working sequence of the DC PC setup.

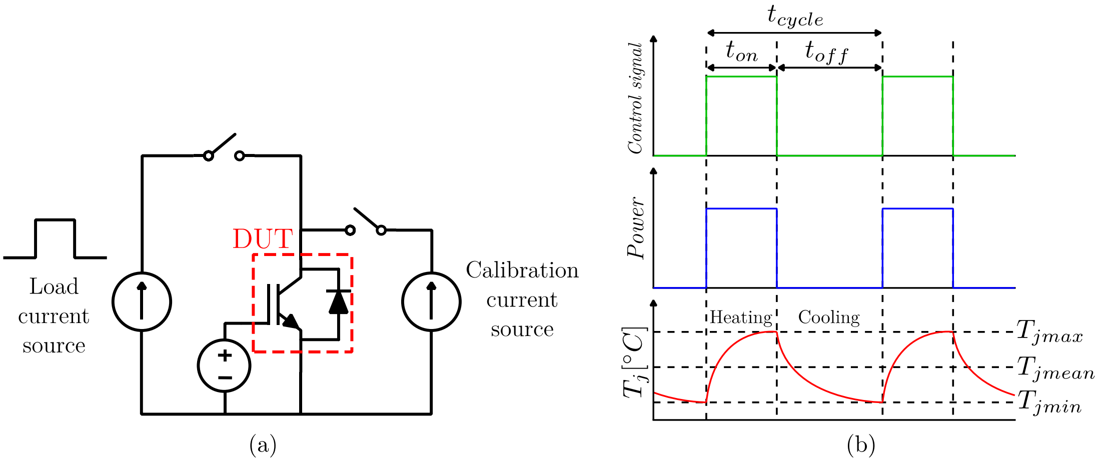


Figure 4.2. Conventional DC power cycling test: (a) DC power cycling circuit, (b) Control signal, injected power and temperature profile applied to the DUT [249]

It is also a common practice to make a junction temperature estimation, once the main load current is disconnected from the DUT [49], [274]. In order to perform this estimation, a calibration current source is employed in this setup as seen on Figure 4.2 (a). This additional current source is responsible for applying a small current, in the range of milliampere, for achieving an accurate junction temperature estimation. The estimation process will be dealt in detail later in this chapter.

The DC power cycling setup can have several extended configurations. There are configurations that allow the testing of multiple DUT devices [275] (Figure 4.3 (a)). Another type of configuration for performing DC power cycling consists of the use of the DUT in linear mode [249] (Figure 4.3 (b)). In this particular configuration, the gate-emitter voltage V_{GE} of the DUT is controlled so that a target collector current I_C can be obtained. The feedback of the collector current is often carried-out with an op-amp integrator. This configuration has an additional control parameter V_{DC} for the generation of power losses, and thus can work at reduced current when compared to the traditional DC PC circuit.

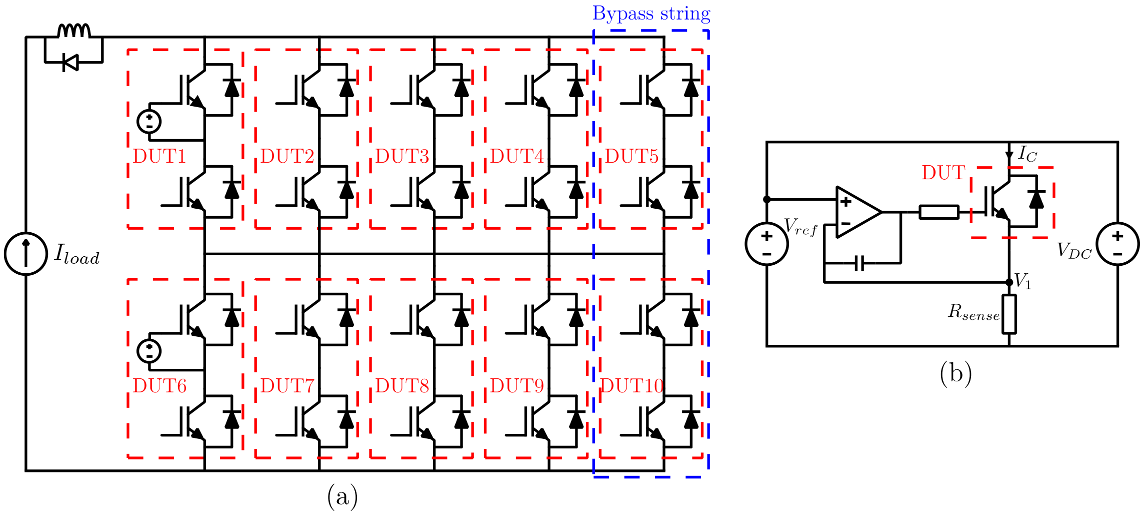


Figure 4.3. Extended configurations of DC power cycling test: (a) multiple device setup [275], (b) DUT in saturation mode [249]

4.3.2. AC power cycling

One of the main issues concerning DC power cycling tests is that the DUT is subjected only to conduction losses for the cycling protocol. This condition is unrealistic as the DUT is submitted to switching actions in real converter applications. Moreover, in the traditional DC PC setup, there is not a blocking voltage applied to the DUT. Given this set of particular conditions for DC PC tests, it is possible to activate failure mechanisms different than the ones experienced in real applications.

Several strategies have been explored in previous works for imitating, more closely, the real-life behavior of IGBT modules. A noteworthy synthesis of these strategies was presented in [261] and [249]. All the PC strategies that rely on the switching of the semiconductor devices can be considered as AC power cycling schemes.

The first type of AC PC test circuits developed, were meant to study semiconductor reliability in the context of traction applications. Hence, the first circuits employed for AC PC tests consisted in motor drive inverters or inverter with inductive loads [112], [276]–[280]. However, this test setting presents several disadvantages. Among the difficulties of this setup, it is worth mentioning that it is quite expensive, as the loads consume large powers during prolonged test periods [249].

In order to overcome the main problems experienced by the previous type of tests, several advanced circuits were proposed in the literature [108], [126], [170], [269], [271], [281]–[284]. The advanced circuits are mainly based on a full H-bridge inverter topology with inductive load, as depicted on Figure 4.4. This circuit is quite advantageous because of its simplicity, the inclusion of switching losses, as well as the involvement of the antiparallel diodes thanks to the inductive loads. This also allows the analysis of the thermal cross-coupling between diode and IGBT dies as reported in [101]. Also, this scheme is cost-efficient, as the power circulates between the phase legs thanks to a phase-shift control strategy. It is thanks to this control approach, that the power supply used in the circuit delivers only the power losses [108], [269], [285]. Finally, this setup and its control strategy allows for an independent control of the power factor PF.

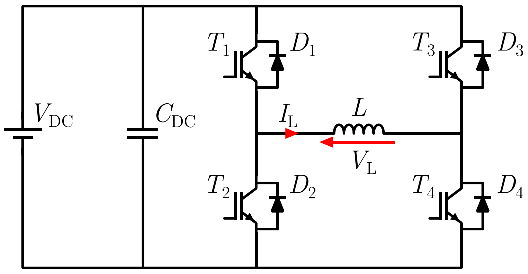
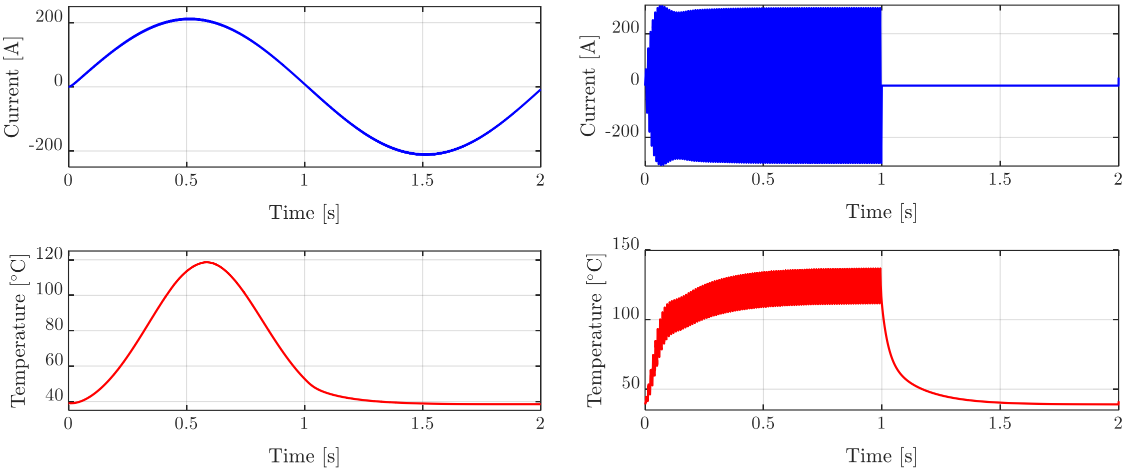


Figure 4.4. AC power cycling test circuit

It is possible to perform two types of power cycling protocols with the advanced AC PC test circuit.

The first approach, seen on Figure 4.5 (a), consists on applying sinusoidal currents with low output frequencies in the range of a few Hz (less than 10 Hz). During the application of the current to the corresponding semiconductor, a thermal variation is obtained thanks to the losses experienced by the semiconductor device. This approach allows for high thermal variations ΔT_j in a relatively short cycle period t_{cycle} [269]. The parameters of the heating cycles such as its amplitude and its duration can be controlled by changing the output frequency, switching frequency, the magnitudes of output current and voltage and the reference temperature. The power factor can also be used as an extra degree of freedom for this type of test.

The second approach, seen on Figure 4.5 (b), makes use of an output current at a much higher frequency than the former approach. The output frequency in this case is in the range of hundreds of Hz. Sinusoidal waveforms are applied to the DUT at the output frequency mentioned previously. The DUT slowly heats by the application of the current, until reaching the target maximum junction temperature T_{jmax} required for the test. Once this temperature is reached the current injection is stopped, similarly to the DC PC test. The junction temperature is slowly cooled down back to the reference temperature by means of an external cooling system. In this cycling approach, longer thermal cycles can be applied to the DUT whilst applying high thermal variations ΔT_j. The thermal cycles can be managed by acting on the magnitude of the output current, the power injection time, the switching frequency, etc.



(a) (b)

Figure 4.5. Strategies for different PC protocols: (a) temperature swing by low-frequency sinusoidal current [269], (b) temperature swing by high frequency current injection [108]

The AC PC test can introduce some modifications to its basic topology, depending on the parameters and the resources available for performing the ageing experiments. For example, cycling protocols were carried out in single phase converters [108], [271] and three phase converters [269]. Another interesting variant, is the one reported in [284], which was used for testing high power semiconductor modules. However, the basic operating principle for these circuit variations remains the same as the one previously described for the generic AC PC test circuit.

A synopsis on the DC and AC power cycling methods can be seen in Table 4.2. From this summary a choice on the type of test bench to be developed for this thesis was made. The AC PC test bench was chosen since it makes a more realistic assessment of the power losses. Thus theoretically, the failure mechanisms will be more similar to the ones experienced in the real application.

Criteria	DC platforms	AC platforms
Type of losses	Conduction losses	Conduction and switching losses
Cost	Low	High
Complexity	Low (Moderate)	High
Controllable parameters	I, t_{on}, V_{GE} (V_{DC})	I, t_{on}, V_{GE}, V_{DC}, V_{out}, f_{out}, f_{sw}, PF
Advantages	- Simplicity in operation and monitoring of precursors - Possible to test multiple DUTs	- DUT exposed to realistic conditions - More variety of PC test conditions
Disadvantages	- DUT not subjected to realistic conditions - High current is required - Limitation on the PC test conditions	- Complexity in operation and monitoring of precursors - Relatively expensive

Table 4.2 Summary on the power cycling test methods [249]

4.4. Power cycling test setup

As mentioned in the previous paragraph, the AC PC circuit was chosen for performing reliability tests on the studied IGBT power modules. The details on the test bench setup will be described in the following lines.

4.4.1. Configuration of the AC power cycling test setup

Figure 4.6 depicts the configuration of the chosen AC power cycling test setup. The topology of the setup is a single-phase full H-bridge circuit. Similar to what was done in [269], [286], each half-bridge converter behaves as an individual converter. One of the half-bridge modules is used as the device under test DUT, whereas the other half-bridge module, is a higher rated power module, which will be called the load module. This is done so that the higher rated module withstands the power cycling tests performed with this setup, without the need of changing the power devices.

Both half-bridge modules are connected to an inductive charge which allows the power circulation between both phase legs. The test circuit also uses a DC-link capacitor for providing the transient energy required for the power exchange between both phase legs. Also, the circuit uses a DC voltage source, that will deliver the power losses. The aforementioned elements are the basic elements of the generic AC power cycling test benches reported in the literature (Figure 4.4). However, this new enhanced setup has several other elements.

The enhanced test circuit uses bleeding resistors R_{disch} for assuring a safe capacitor discharge, once the test sequence is stopped, thus improving the overall safety of the circuit. Also, an input resistor R is employed. This resistor has two main functions: The first one consists of limiting the current when charging the DC-link capacitor. The second function consists of filtering the current delivered by the source, since this resistor and the DC-link capacitor behave as a low-pass RC filter, which will be beneficial when using several AC PC test circuits in parallel. Additionally, the test circuit uses protection diodes in parallel to the DUT devices. The role of these elements will be described in more detail in section 4.4.4.3. All the power elements employed in this setup are placed over a liquid cold plate, which will set the temperature reference for the DUT. The testbench also employs a contactor switch responsible for the connection of each inverter to the DC voltage source.

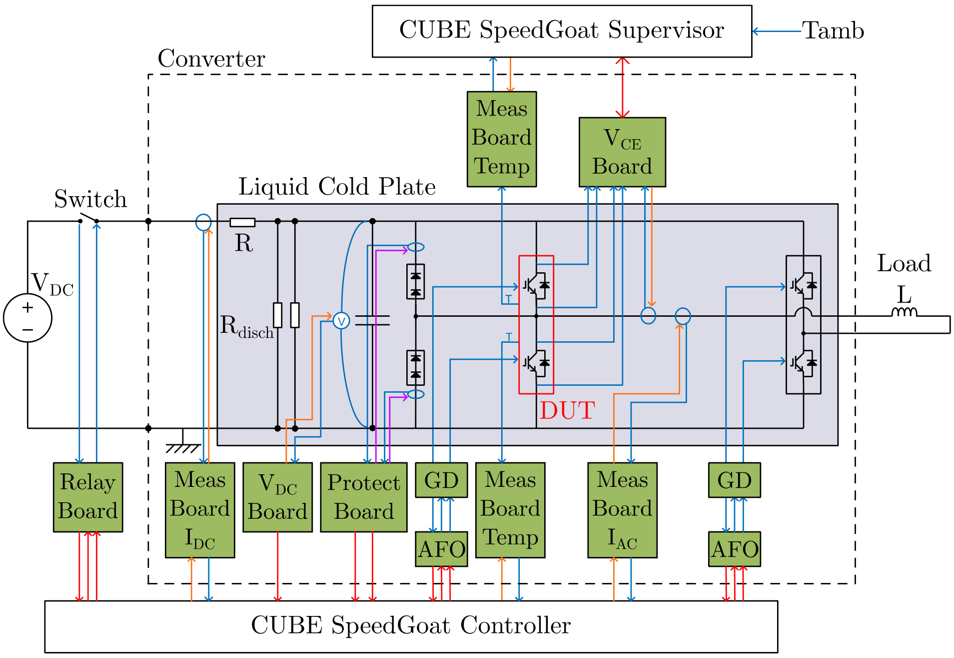


Figure 4.6. Configuration of power cycling test setup

Last but not least, this setup uses several electronic boards for assuring the circuit proper operation and monitoring of the cycling protocol. In Figure 4.6 the commercial gate drivers (GD) and fiber optic adapters (AFO) for interfacing the GDs to the controller can be seen. The remaining electronic boards were developed specifically for the PC test bench. More details on these electronic boards will be given in section 4.4.4.

Concerning the control and the supervision of the testbench, two customized Speedgoat real-time target machines are employed. One of the Speedgoat machines employed can be seen on Figure 4.7. From Figure 4.7, it can be seen that the Speedgoat machines employed have several interfaces that allow to receive and send analog or digital signals.

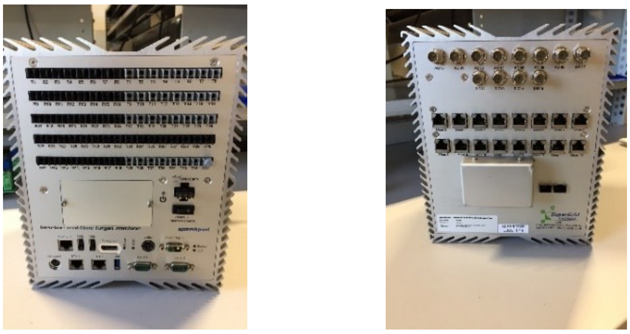


Figure 4.7. Customized Speedgoat real-time target machine

One of the Speedgoat machines is used as the controller for the test bench which consists of 5 identical AC PC test circuits in parallel as seen on Figure 4.8. The other Speedgoat machine oversees all the acquisitions related to the monitoring of the health state of the DUT and the estimation of the junction temperature. The Speedgoat machines use MATLAB and Simulink as their interface.

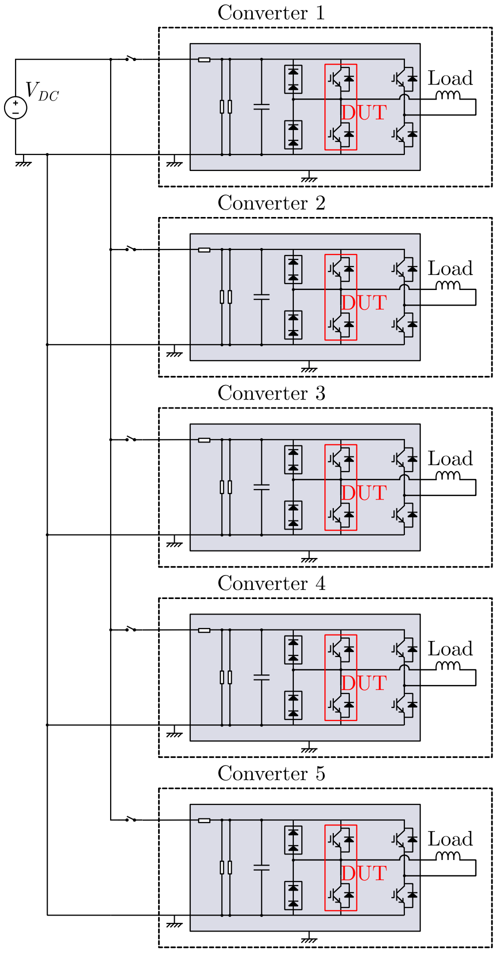


Figure 4.8. Complete testbench diagram

The Speedgoat controller not only sends the drive signals for the IGBT modules and regulates the load current, but it is also responsible of assuring the safe operation of the test bench. Among the protections implemented, a verification of the capacitor voltage is done for detecting any overvoltages and for assuring that the voltage is high enough for the normal operation of the converter. Other protections include an overcurrent protection, a protection against cold plate overheating, also the return signal from the gate drivers is linked to the controller, as the drivers are able to detect faults. In case of any type of fault, the controller stops the functioning of the concerned converter, and it opens the contactor switch that connects it to the DC power supply.

On the other hand, the Speedgoat supervisor receives the readings of the collector-emitter voltages from the DUT, as well as the load current for health monitoring purposes. It performs 10 s acquisitions every 10 minutes at a sampling rate of 1.25 µs for each converter. All the data is then sent to a server for performing computations such as the junction temperature estimation.

An external chiller is used for providing the water required by the liquid cold plates. The chiller can control the water temperature which will set a reference for the heatsink temperature, according to the desired test condition and keep the cold plate temperature as constant as possible throughout the duration of the PC test.

Figure 4.9 shows the AC power cycling test circuit with all its composing elements. It can be seen from Figure 4.9 that the DUT power module can be easily accessed. The power connections are achieved by employing conductive bars for ease of installation and replacement of the DUT, as this element will often be changed when performing the power cycling tests. Hence, the AC PC testbench was conceived with a plug-and-play concept, for easy replacement of the tested DUT modules, as well as the electronic boards required for converter operation. The complete power cycling testbench scheme can be seen in Figure 4.10.

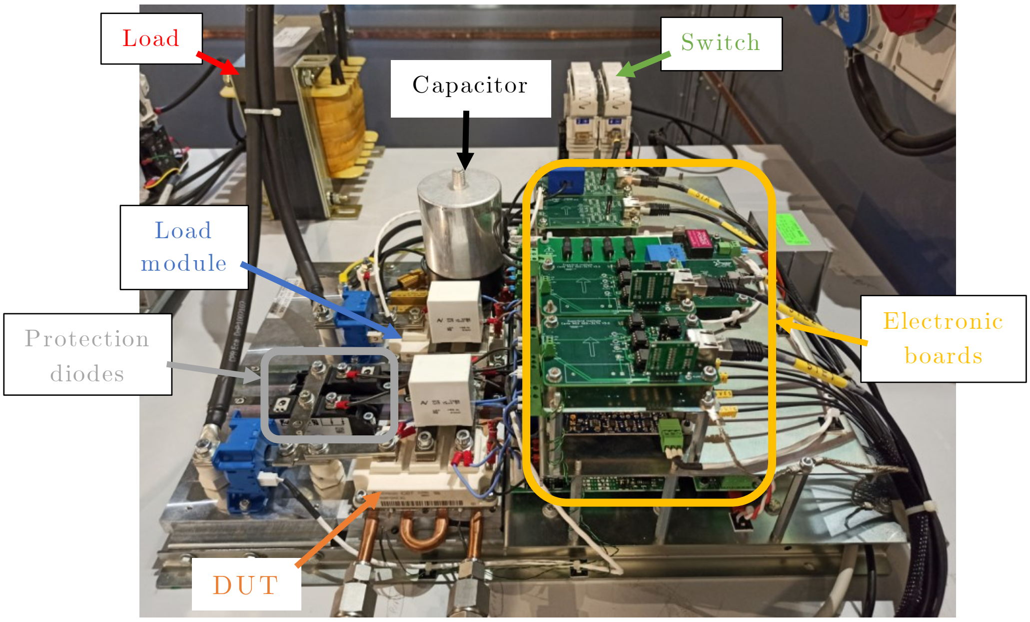


Figure 4.9. Prototype for the AC PC test setup

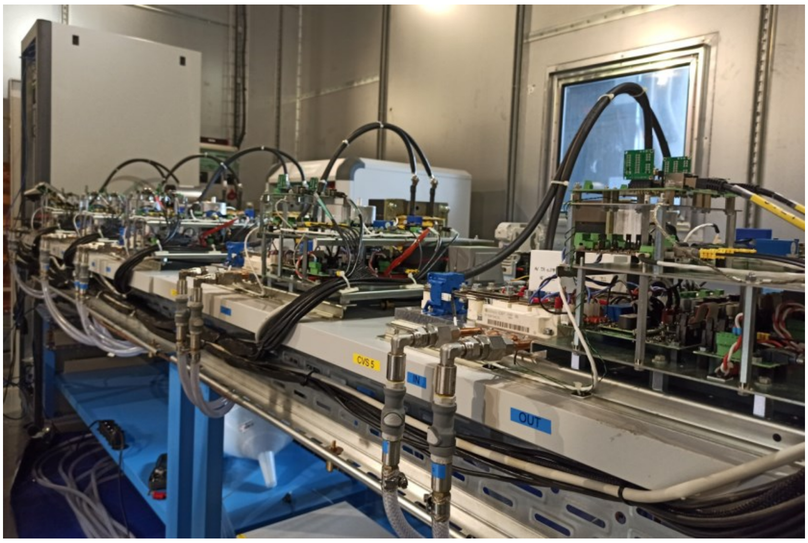


Figure 4.10. Power Cycling testbench

4.4.2. Choice of device under test

In order to be able to obtain substantial results and being able to make statistical analysis, it is necessary to test multiple devices. Hence, a smaller power module than the one used in the real MMC application was chosen. This is done mainly for economic reasons. since the power modules used in real HVDC-MMC applications can be quite costly.

A power module that would be suited for an HVDC-MMC applications is the single switch IGBT module FZ1500R33HL3 [287]. This device uses Trench/Fieldstop IGBT3 technology, thus a smaller module using the same semiconductor technology was chosen as the device under test. The reference of the power module used for the power cycling tests is the dual IGBT module FF150R12KE3G [288], seen on Figure 4.11.

Figure 4.11. IGBT dual module FF150R12KE3G typical appearance

The chosen DUT module is a 1200 V, 150 A power device compared to the 3300 V 1500 A device used in the real application. As it was first mentioned in section 4.4.1, the load module is a higher rated module than the DUT module. The chosen load module is the dual IGBT module FF450R12KT4 [289], which can withstand 1200 V and 450 A, which is a current rating three times higher than the current rating of the DUT. The load module has the same housing as the DUT module (Figure 4.11), thus this module was chosen for ease of integration in the AC PC converter. Additionally, the load module has fast Trench/Fieldstop IGBT4 technology, which according to the manufacturer can enhance the lifetime expectation when compared to IGBT3 technology at equal output power [290].

4.4.3. Operating principle of the setup

In the chosen setup the DUT module and the load module are linked via the inductive charge as shown in Figure 4.6. The basic principle of the converter follows the opposition method described in [285]. The DUT module is controlled using an open-loop controller, which sets an output voltage reference V_1, which fulfills the required cycling conditions such as magnitude, output frequency and switching frequency. The complimentary module is controlled with the help of a closed-loop controller, which sets the output voltage V_2 in the load branch. The V_2 voltage reference is calculated in order to generate a current reference I_L across the load inductor with the desired magnitude, output frequency and power factor. The control scheme employed can be seen on Figure 4.12.

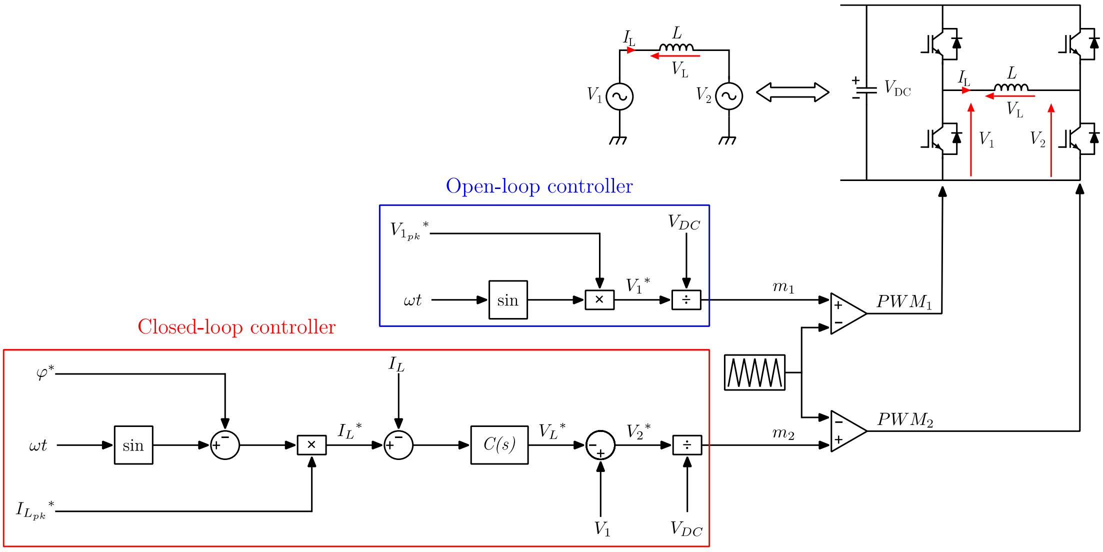


Figure 4.12. Control strategy for the AC power cycling test circuit

A Proportional-Integral (PI) controller is used for the closed-loop controller seen in Figure 4.12. The output of this current controller is the voltage reference across the load inductor, which is the voltage difference between the DUT and the load branch as seen on Figure 4.13. The application of a voltage across the inductor will generate a current variation across the inductor. Thanks to the control strategy employed, a small load inductor can be used for obtaining a low current ripple. As explained in [269], the power factor of the output current can be modified for imposing different power cycling conditions. With a PF=1, the IGBT losses are dominant on the DUT branch and the diode losses on the load module. On the contrary, with a PF=-1, the diodes are submitted to higher stresses on the DUT module and the IGBTs on the load branch.

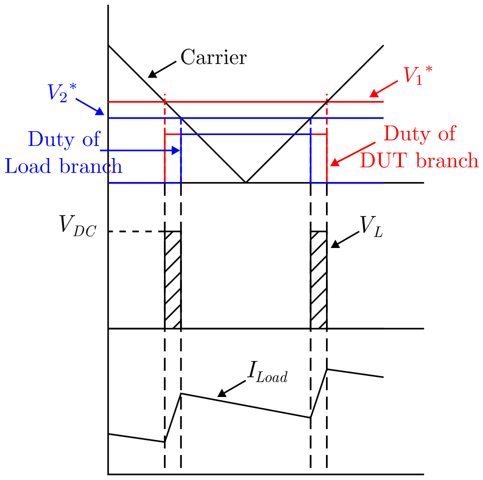
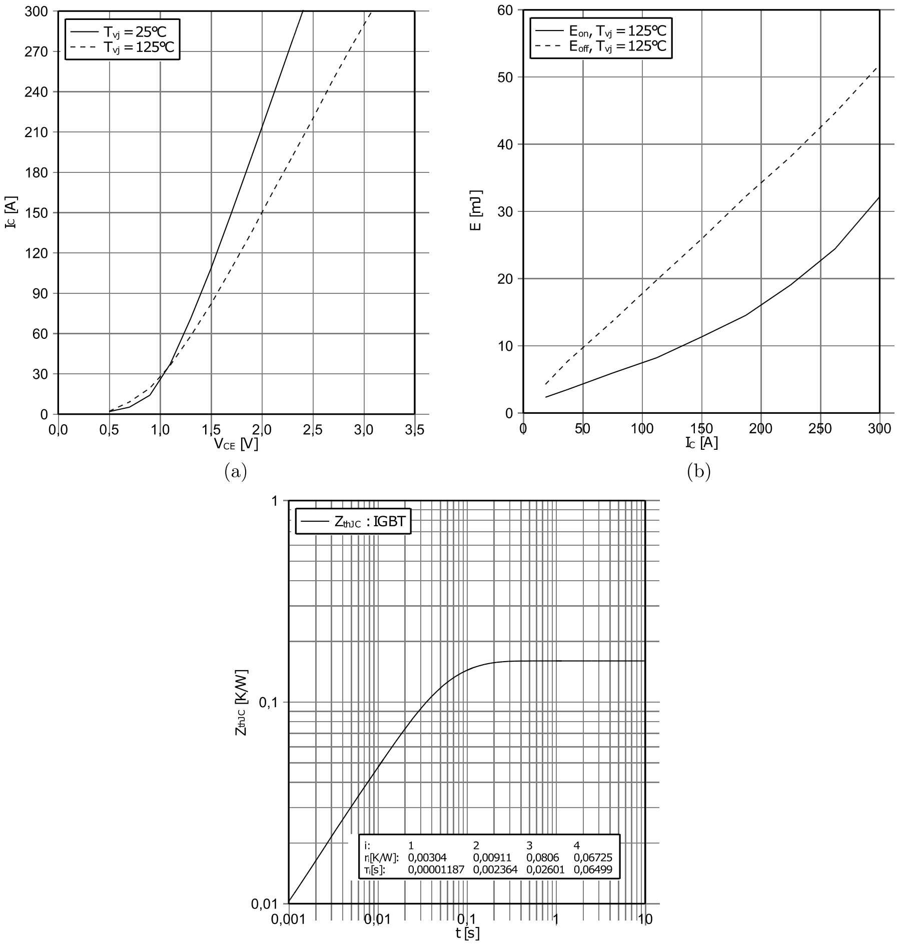


Figure 4.13. Reference voltages for the DUT and load module, reference inductor voltage and output current [269]

The sinusoidal current applied to the load, also passes through the power modules. This current flow leads to power losses inside the semiconductor devices, which leads to the temperature increase for performing the PC test. The DUT datasheet information provided by the manufacturer [288] and seen on Figure 4.14 is used for computing the temperature profile corresponding to a given current reference as seen on Figure 4.15.



(a) (b)

(c)

Figure 4.14. DUT Datasheet information for computation of power losses and thermal profile [288]: (a) IGBT On-state characteristics, (b) IGBT Switching energies per pulse vs. collector current, (c) IGBT Transient thermal impedance

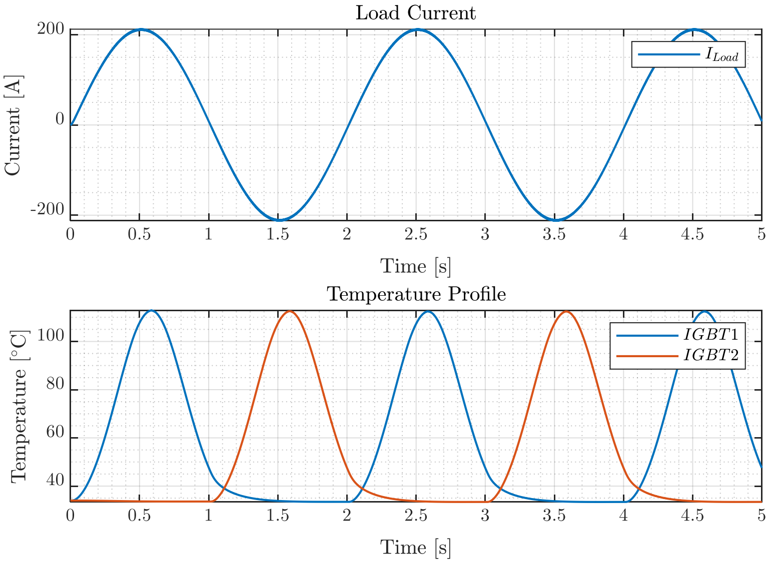
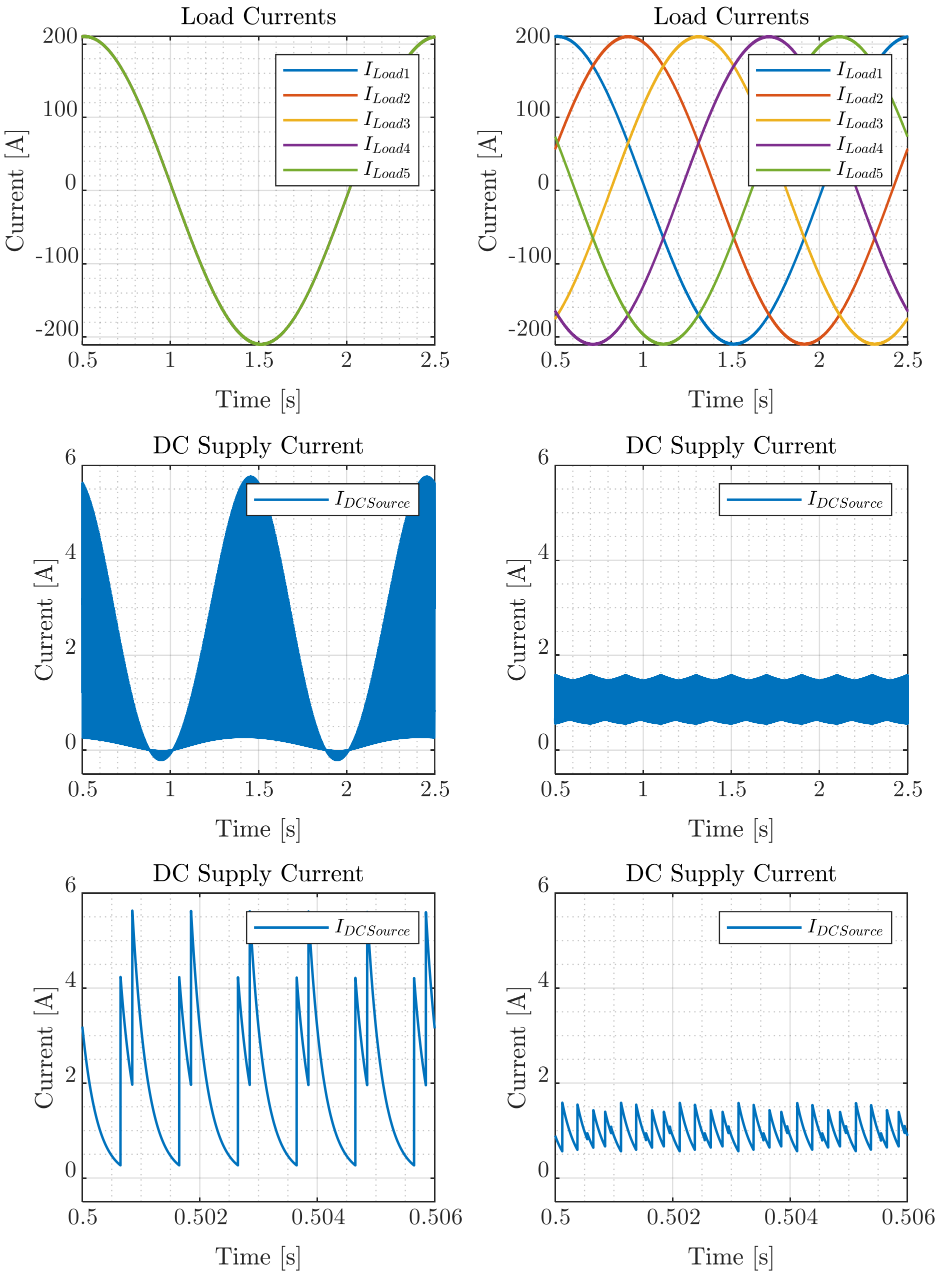


Figure 4.15. Current reference and corresponding junction temperature across the DUT devices

Since there are 5 identical converters in the overall AC PC test setup, it is necessary to make an efficient management of the power demanded to the DC voltage source. This is achieved by introducing different phase angles ωt to each individual converter. As there are 5 converters, the different voltage and current references must be shifted by 72°, in order to have the lowest current inrush from the DC voltage source. This could also enable a lower rating of the DC source. If this phase shift is not performed, the testbench will still work, however, the DC supply will be more stressed during the PC protocol. Figure 4.16 shows the load currents and the DC voltage source current under the best condition (with phase shift), and under the worst condition (without phase shift).



(a) (b)

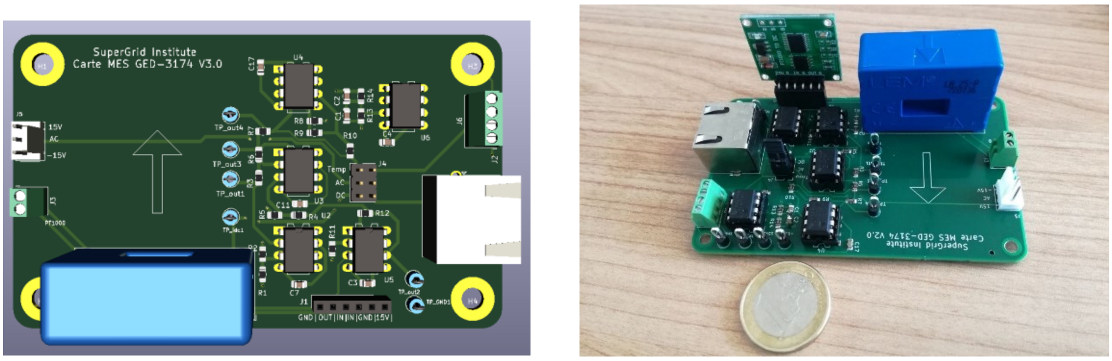
Figure 4.16. Load currents and DC Voltage source current inrush: (a) without phase shift, (b) with phase shift

4.4.4. Electronic boards

The PC testbench requires a large number of measurements and data treatment in order to be able to operate. Moreover, data needs to be acquired and treated for following the evolution of the different failure precursors in order to be able to determine the state of health and the remaining useful life of the DUT devices. Hence the development of electronic boards was a crucial stage in the development of the PC test setup. In the following lines the different electronic boards developed for the testbench will be described.

4.4.4.1. Measurement board

The measurement board is a multipurpose electronic board, which can be configured in three different ways, depending on the desired function. This board has a common PCB layout for its different functions and it is interfaced with the analog ports of the Speedgoat real-time machines. The layout and the real measurement board can be seen on Figure 4.17. However, more or less components will be soldered onto the PCB, based on the board configuration. The different measurement board configurations will be developed in this section.



(a) (b)

Figure 4.17. Multipurpose measurement board (a) concept, (b) final board

4.4.4.1.1. Temperature measurement

It is necessary to have a proper measurement of the reference temperature for performing the PC tests. In the case of the developed PC test circuit, Pt1000 resistance temperature detectors (RTDs), as the one seen on Figure 4.18 were employed for carrying out temperature measurements T_c at the interface of the liquid cold plate and the DUT baseplate. In order to be able to place these probes, grooves have been machined on the liquid cold plate surface as depicted on Figure 4.19. It must also be noted that the placement of the Pt1000 probes and the grooves is done so that the semiconductor dies are vertically aligned with the RTDs, for obtaining a correct acquisition.

Figure 4.18. Pt1000 P_1K0.161.1E.A.040

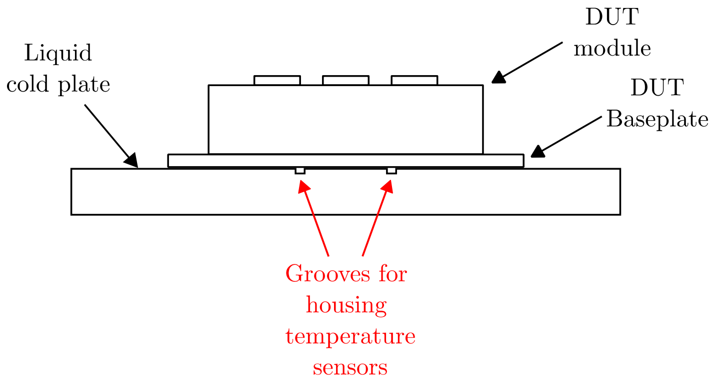


Figure 4.19. Groove placement for heatsink temperature measurement

The voltage across the RTD is proportional to the temperature at the interface between the cold plate and the DUT baseplate. Hence, an effective method for translating the voltage measurement into a temperature reading must be employed for treating the temperature measurements. In order to simplify this task, a commercial transmitter module was acquired. This module can be seen on Figure 4.20 and can be configured for delivering an output voltage between 0-10 V or 0-5 V. Finally, this voltage measurement signal must be transformed to an analog current signal compatible with the analog ports of the Speedgoat real-time machine. For being able to carry out this mission, a circuit for adapting the voltage output of the transmitter module to the required analogic current signal was developed and can be seen on Appendix A.2. An example of the temperature measurements performed with this board can be seen on Figure 4.21.

Figure 4.20. NGW thermal resistance to voltage Pt1000 to 0-5V 0-10V linear conversion temperature transmitter module

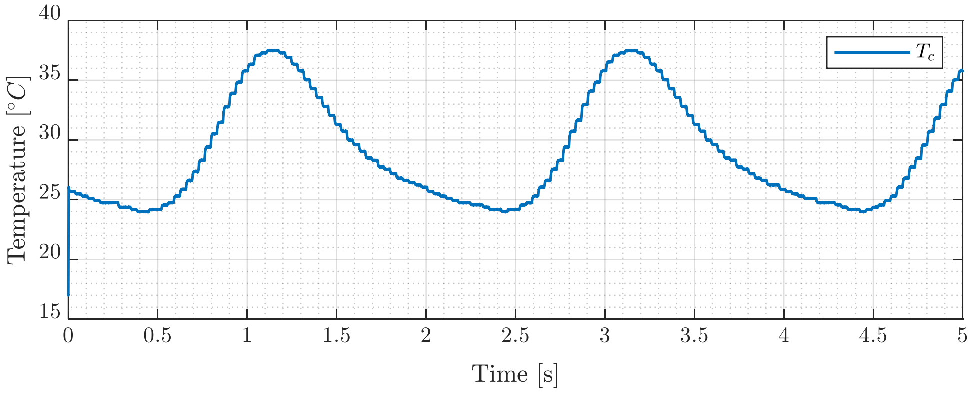


Figure 4.21. Temperature measurement at the interface of the cold-plate and the DUT baseplate with the multipurpose board

These temperature measurements are then treated by the supervision dedicated Speedgoat machine. This data will be used for the development of the junction temperature estimation algorithm, as well as for the protection of the overall circuit. If the measured cold-plate temperature exceeds a safety threshold, an alarm signal will be sent to the controller, which will eventually launch an emergency stop sequence to the converter.

4.4.4.1.2. I_{ac} measurement

A very important function for an appropriate operation of the PC test setup is the measurement of the load current. Firstly, this measurement is used for the control strategy of the circuit, which will compute the command signals of the power devices, in order to generate the load current reference for achieving the desired PC condition. Secondly, the current measurement will be employed for the estimation of the junction temperature. This measurement can be associated with look-up tables for calculating the collector-emitter saturation voltage $V_{CE(sat)}$ of the IGBT devices, which can then be employed for performing a calculation of the losses experienced by the power semiconductors.

Therefore, an accurate sensor must be used for performing the current readings. The chosen sensor for this mission is the LEM LF 210-S seen on Figure 4.22. It is a closed loop Hall effect current transducer. This current probe is fed through the multipurpose measurement board and its analogic readings are also transmitted to the Speedgoat controller via this circuit.

Figure 4.22. LEM LF 210-S for load current measurement

4.4.4.1.3. I_{dc} measurement

It is necessary to have a correct measurement of the current delivered by the DC voltage source to each individual PC test circuit. This is necessary for safety purposes, as a large current inrush could indicate a DC bus short-circuit. For accomplishing this assignment, a current probe between the connecting switch and the input resistor of each individual PC converter is used. As it was previously explained, the DC voltage source will only deliver the power losses experienced by the semiconductor devices. This translates to a low current value, when compared to the current experienced by the loads. Thus, the DC current measurement is mainly used for safety reasons, when a certain threshold value is met, the testbench controller will start a turn-off sequency to the converter which has experienced the overcurrent. The current transducer LEM LA 25-P, seen on Figure 4.23, was chosen for performing these readings. This sensor is also fed through the multipurpose board and uses this circuit as a mean for communicating with the Speedgoat controller.

Figure 4.23. LEM LA 25-P for DC input current measurement

4.4.4.2. V_{dc} measurement board

It is necessary to have a correct measurement of the DC link voltage, as it can be dangerous to have an overvoltage at the capacitor terminals. It is also necessary to have a proper DC link voltage to generate the required current reference, as if this voltage is not big enough the current reference will not be achieved as there is not sufficient energy in the capacitor to feed the load inductor. Hence, the controller makes use of this measurement for the correct functioning of the controller. If there is an overvoltage or a very low DC link voltage, the PC sequence will be stopped by the controller.

This type of measurement requires special attention. Firstly, since a high voltage is being measured at the DC link (i.e. 600 V), some isolation requirements must be met for assuring a safe operation of this circuit. Secondly, since the analog ports of the Speedgoat controller are already being used by the multipurpose measurement boards, this signal must be digitized and sent through a fiber optic interface to the Speedgoat real-time machine.

In order to meet the special requirements for this measurement, the main components used for this board are: a LEM voltage transducer LV-25P/SP (Figure 4.24), an analog to digital converter (ADC) AMC130505 with ΣΔ architecture (Figure 4.25) and a fiber optic transmitter AFBR-1624Z (Figure 4.26). The overall concept for this measurement can be seen in Figure 4.27.

Figure 4.24. LV-25P/SP voltage transducer for DC-link voltage measurement

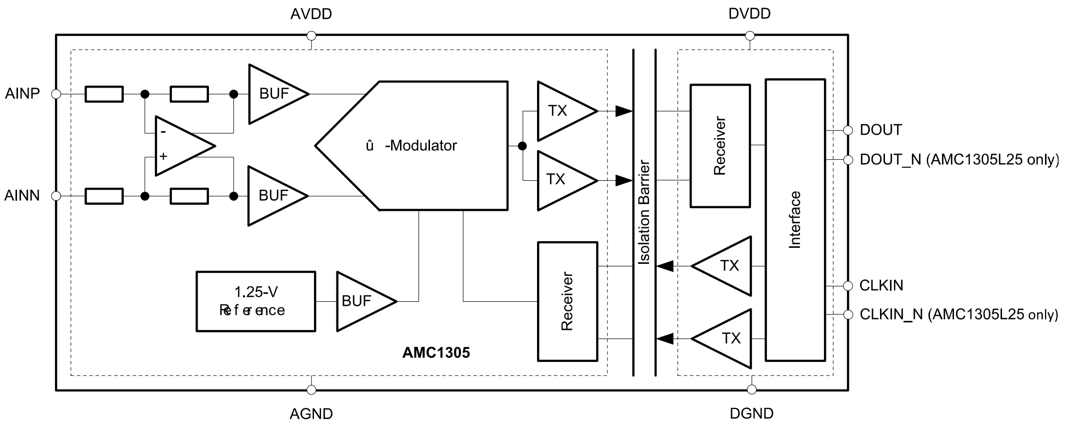


Figure 4.25. ADC AMC130505 internal structure [291]

Figure 4.26. AFBR-1624Z fiber optic transmitter

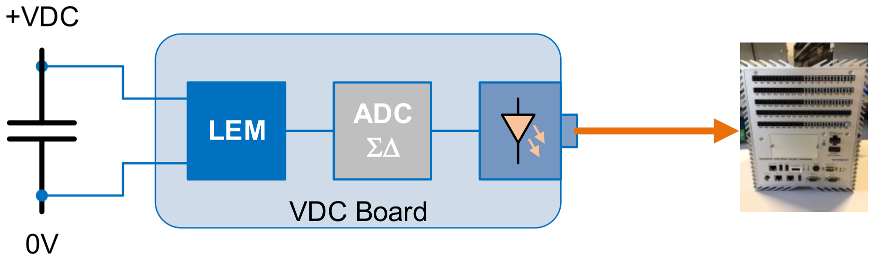
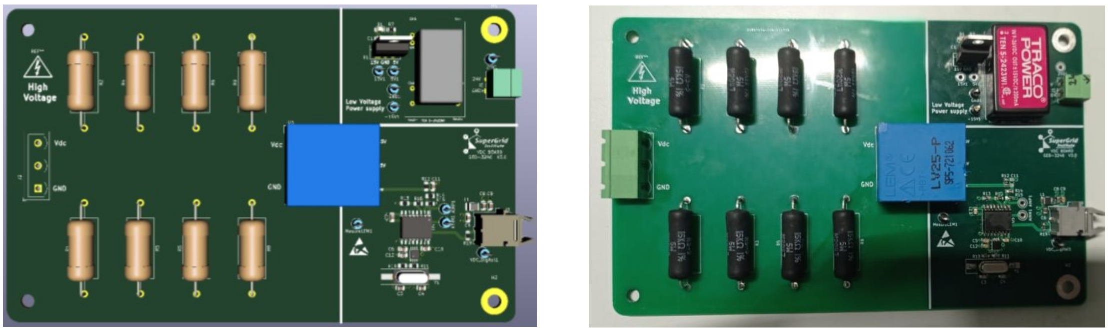


Figure 4.27. Overall concept for the V_{dc} board

More details concerning the V_{dc} board layout and the dimensioning of the different stages for conditioning the analog input signal to the digital signal transmitted to the controller are available on Appendix A.3, also the validation of the circuit can be seen on the same appendix. The V_{dc} board is finally depicted on Figure 4.28.



(a) (b)

Figure 4.28. V_{dc} board: (a) concept, (b) final board

4.4.4.3. Protection diodes and protection board

As it was seen on Figure 4.6 and depicted in greater detail in Figure 4.29 the PC test circuit has a protection branch made of 2 series diodes in parallel with the higher and lower devices of the DUT module.

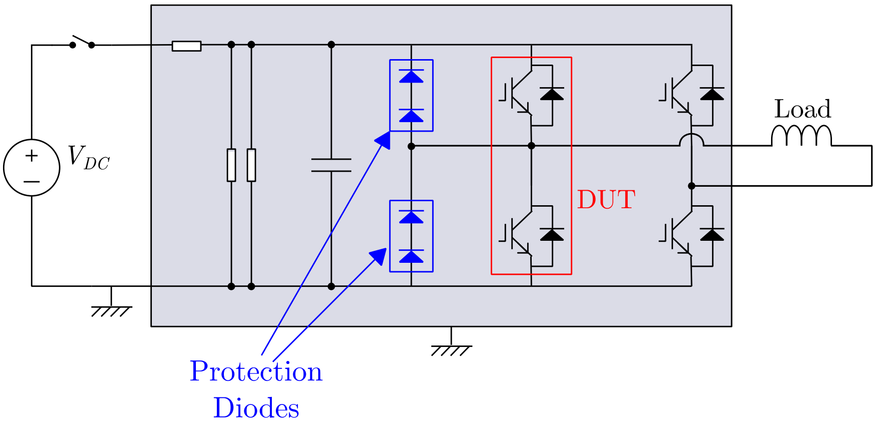


Figure 4.29. Protection diodes for open-circuit fault detection

The PC test circuit is able to apply thermal stress to both IGBT and diode devices on the DUT module. In this study only the IGBT semiconductors will be submitted to the PC conditions. Nonetheless, this testbench was conceived for testing also the diode devices in further studies. In case of any short-circuit fault in either IGBTs or diodes, the gate drivers associated with the DUT module will send a signal to the controller, that will launch the stop sequence of the converter. Concerning open circuit faults, if an IGBT device experiences this condition, the complementary side diode will start conducting as depicted in Figure 4.30. When this condition happens, the controller will get a return on this condition and will stop its normal operation.

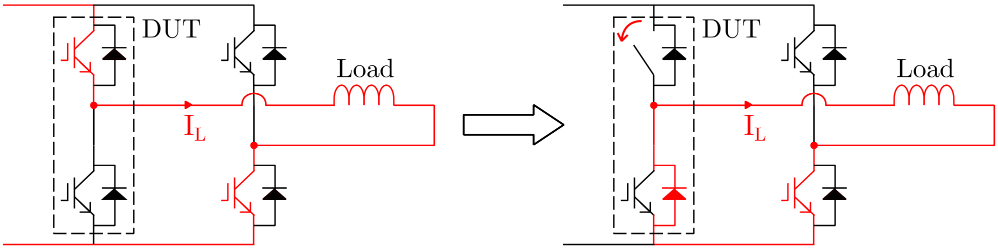
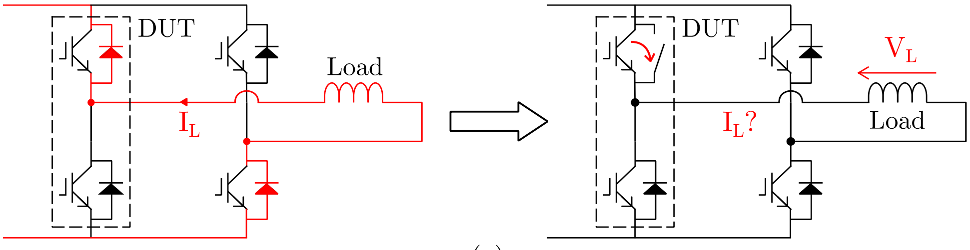
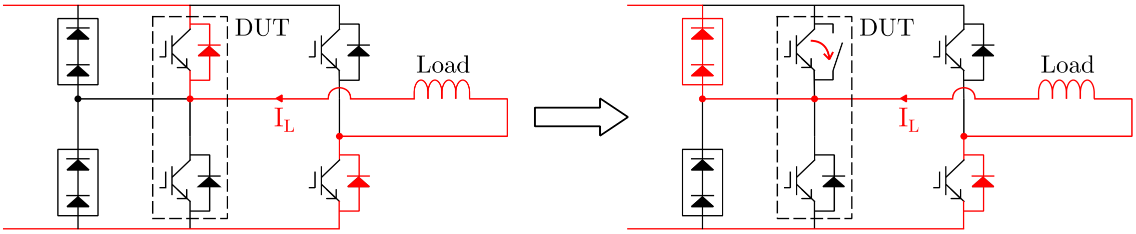


Figure 4.30. IGBT open-circuit fault

However, in case of any open-circuit faults in the diodes, the current path will be interrupted, and a high voltage will appear at the load terminals as a result of the sudden current halt as depicted in Figure 4.31 (a). It is under this particular condition that the protection diodes installed in a parallel branch will become active and will ensure the current conduction as depicted on Figure 4.31 (b). The protection diodes won't be active during the normal operation of the converter, as the threshold voltage V_{th} of the protection diodes is much higher than the threshold voltage of the diode of the DUT. Two diodes were used in series for guaranteeing a higher threshold voltage on the protection branch. The reference for the diodes installed in the protection branch is IXYS MEE75-12DA, these elements can be seen on Figure 4.32.



(a)



(b)

Figure 4.31. Diode open-circuit fault: (a) without protection diodes, (b) with protection diodes

Figure 4.32. Diodes IXYS MEE75-12DA

It is finally necessary to detect the presence of any current on the protection branch, since this means that a diode on the DUT branch has already failed and the cycling protocol must be stopped. For achieving this mission, a current probe is placed on the protection branch and a special board was conceived. The current probe chosen for this current measurement is the LEM transducer HASS 50-S seen on Figure 4.33. It is a hall effect open loop transducer. This sensor is fed through the protection board, which also sends an alert signal to the controller once a threshold current is reached. The circuit for detecting the current on the protection diodes employs open collector comparators LT1011.

Figure 4.33. LEM transducer HASS 50-S

The current threshold for sending the alert signal to the controller can be configured by regulating a potentiometer installed on the protection board. The protection board communicates with the controller via the digital ports of the Speedgoat real-time machine, thanks to fiber optic transmitters AFBR-1624Z as the one seen on Figure 4.26. For safety concerns, this circuit was conceived with a reverse-logic approach. This means that the circuit sends a signal at high state if there is no current on the protection diodes. Complimentary, once a current is detected on the protection branch and becomes higher than the set threshold, the protection board sends a low voltage signal to the controller. The final circuit for the protection board can be seen on Figure 4.34.


(a) (b)

Figure 4.34. Protection board (a) concept, (b) final board

4.4.4.4. Relay board

The switches that connect each converter to the DC voltage supply, seen on Figure 4.6 and Figure 4.8, must be able to withstand the current coming from the voltage source and they need to operate at the DC-link voltage (600 V). The switch LTC002501*A02 from Microelettrica Scientifica and seen on Figure 4.35, was chosen due to its electrical characteristics.

However, the chosen switch requires an important power consumption for closing its main contacts. Unfortunately, the controller does not have high power ports for interfacing directly with the switch. Hence, an additional interface is required for accomplishing this connection. This interface must be able to send the necessary command signals to the switch, and also to receive a reading of the state of the switch. Moreover, this interface must be able to control all the switches of the converter and be able to open and close the switches according to the established procedures for a correct operation of the PC testbench. Hence, this interface will require a special architecture. The concept and the elements chosen for this board can be seen on Figure 4.36 and will be called relay board.

Figure 4.35. Switch LTC002501*A02 for connection of the converters to the voltage source

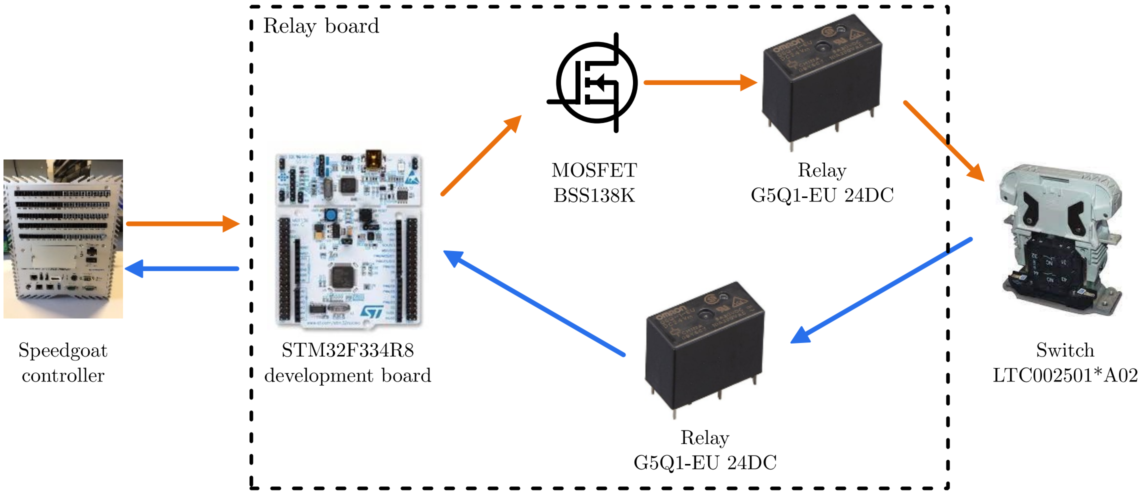


Figure 4.36. Relay board concept

The relay board uses relay elements as a mean for interfacing the power supply necessary for closing the main contacts of the power switch. The relays chosen for this particular interface have the reference G5Q-1-EU 24DC from Omron Electronics and can be seen in Figure 4.36. These relays are also used for reading the state of the switch with the help of its auxiliary contact. The relay board also has a STM32 development board as seen on Figure 4.36. The general-purpose input/output ports (GPIOs) of the development board are used for sending the command signals to the different power switches and for reading its states. Some of the GPIOs of the development board are also used for establishing the exchange with the Speedgoat controller by using UART (Universal Asynchronous Receiver/Transmitter) communication thanks to a RS-232 serial protocol. Finally, the circuit requires the use of BSS138K power MOSFETs for linking the development board and the relays, hence allowing the actioning of the power switches.

More details on this board and its additional circuitry can be found on Appendix A.4. The resulting circuit for the relay board can be seen on Figure 4.37.

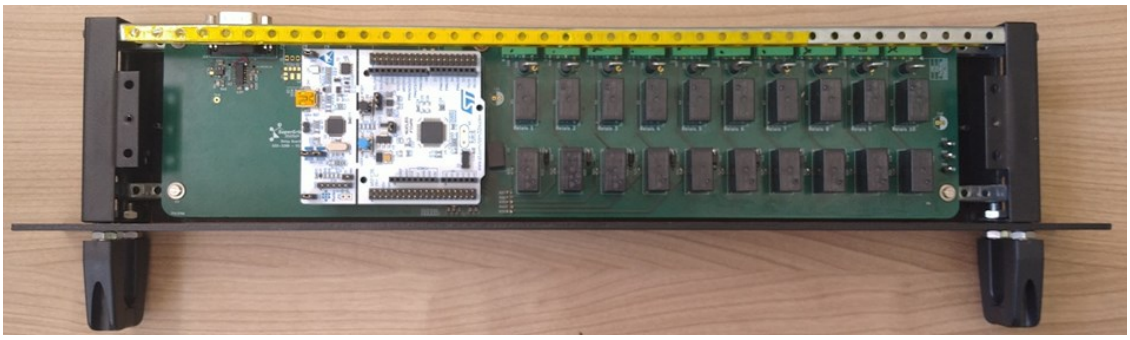


Figure 4.37. Relay board

4.4.4.5. V_{CE} measurement board

The electronic boards described in previous lines were necessary for the nominal operation of the converter as well as for safety reasons. The last electronic board developed for the PC testbench does not have the same purpose. Instead, this board will track the evolution of one of the main failure precursors of the IGBT devices, the collector-emitter saturation voltage $V_{CE(sat)}$. This board will also be able to measure the diode forward voltage V_F, which is one of the main failure precursors corresponding to this type of semiconductor. As it was mentioned previously in section 4.3 the tracking of the failure precursors allows for an estimation of the state-of-health of the semiconductor device. Therefore, an accurate method for the measurement of this failure precursor must be implemented.

A literature review was conducted on the main measurement methods for the $V_{CE(sat)}$ and the V_F. There are two important categories concerning this subject: offline and online measurement schemes.

Offline measurement schemes are quite common in the context of PC tests, because they provide a high degree of accuracy and high voltage input range [292]. One of the most employed circuits for this type of measurement was reported in [120], [293]. However, offline methods only serve the purpose of evaluating the degradation of the DUT, they do not provide more advanced functionalities to the supervision of the PC protocol.

Online measurements are more challenging to achieve, as they are carried out during normal operation, while the DUT is connected to the main power source. However, they can contribute to a deeper analysis on the state of degradation of the DUT. Because of this reason, this type of measurement will be considered for the PC testbench deployed for this thesis.

One of the most common online measurement schemes is the one proposed in [292]. This circuit employs a similar technique than the one used for protecting the semiconductors against short-circuits and overload currents. The sensing technique is based on the use of two thermally coupled diodes as seen on Figure 4.38.

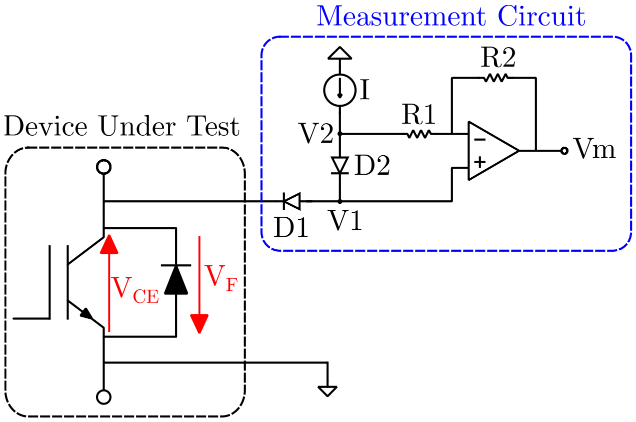


Figure 4.38. V_{CE} measurement circuit proposed in [292]

The working principle of the measurement circuit can be described by the following expressions:

$$V_+ = V_1 = V_{CE} + V_{D1} \tag{4.1}$$

$$V_m = V_- - \frac{R2}{R1}(V_2 - V_-) \tag{4.2}$$

If $R2 = R1$ and assuming that the op-amp works on a linear state ($V_+ = V_-$), then replacing Eq. (4.1) in Eq. (4.2) yields:

$$V_m = V_{CE} + V_{D1} - (V_2 - V_1) = V_{CE} + V_{D1} - V_{D2} \tag{4.3}$$

If both diodes experience the same voltage drop ($V_{D1} = V_{D2}$), then Eq. (4.3) becomes:

$$V_m = V_{CE} + V_{D1} - V_{D1} = V_{CE} \tag{4.4}$$

The output of the measurement circuit will be equal to the V_{CE} during the on state of the DUT, when the low current source I polarizes the sensing diodes D1 and D2. However, this sensing principle will only work if the voltage drop across both diodes is identical. In order to guarantee this condition, both diodes were thermically coupled in [292]. When the DUT is at the off state, the diode D1 will block the high voltage and the output of the measurement will be different from V_{CE}. According to [292], if the amplifier is supplied with a bipolar voltage, the circuit can operate for measuring both V_{CE} and V_F.

In [294], it is stated that the previous measurement circuit is not well suited for fast switching semiconductors. The PC testbench developed in this thesis was conceived not only for testing IGBT devices, but it is also intended to be used for testing wide band gap devices in future studies. In the same research work [294], the measurement circuit from Figure 4.39 was proposed.

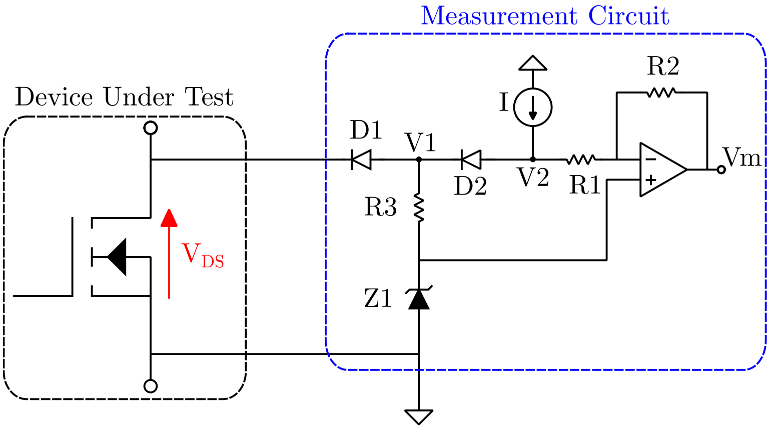


Figure 4.39. On-state voltage measurement circuit from [294]

The basic operation principle of the measurement circuit of Figure 4.39 is the same described in Eqs. (4.1)–(4.4). An important difference between the circuit from Figure 4.39 and the one from Figure 4.38 is the presence of the Zener diode, that will fix the output voltage of the measurement circuit. This new on-state voltage measurement scheme was not intended to measure the voltage across the body diode of the DUT. However, this circuit can measure voltages lower than the voltage drop of Z1 when it is forward biased. Hence, it can measure small V_F voltages (lower than 1V). This V_F range of measurement is adequate for fast switching semiconductors, as they have smaller voltage drops than IGBT devices, but is not adequate for IGBT semiconductors.

In order to keep the advantages of both measurement circuits: High V_F measuring capacity from the circuit in Figure 4.38 [292] and on-state voltage measurement at high switching speeds from the circuit in Figure 4.39 [294], a new on-state voltage measurement circuit was developed in this study. This new circuit can be seen on Figure 4.40.

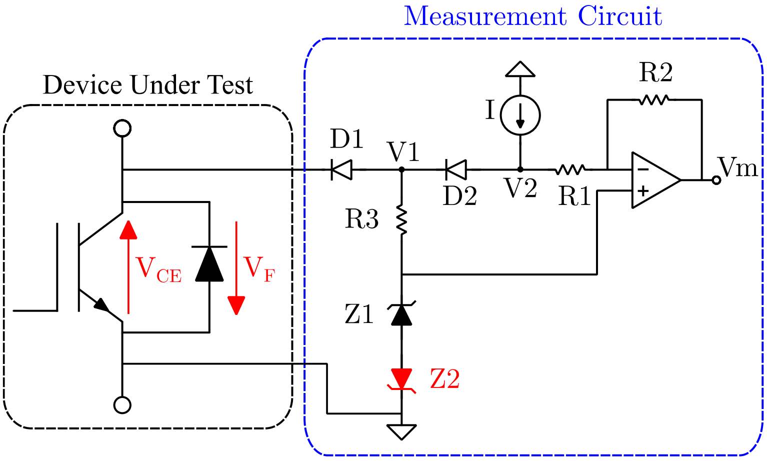


Figure 4.40. Proposed on-state voltage measurement circuit

The addition of Zener diode D2 in the proposed measurement circuit, allows for the sensing of higher range V_F voltages. Moreover, the performances of the circuit in terms of dynamic response are similar to the ones from the circuit in Figure 4.39. Hence, this new measurement circuit is well suited for IGBT devices, as well as for fast switching semiconductors.

The main components for this measurement circuit are the sensing diodes D1 and D2 with reference STTH112, which are ultrafast diodes from STMicroelectronics. The Zener diodes used in this circuit have the reference BZX84B8V2L from ROHM and the operational amplifier AD8065.

Besides measuring V_{CE} this board is also intended to perform the measurement of the current across the load I_{Load}. By performing V_{CE} and I_{Load} measurements, this circuit can be used for the online estimation of the junction temperature T_j of the semiconductor devices. This subject will be described in more detail in section 4.5. The concept for this measurement circuit is shown in Figure 4.41.

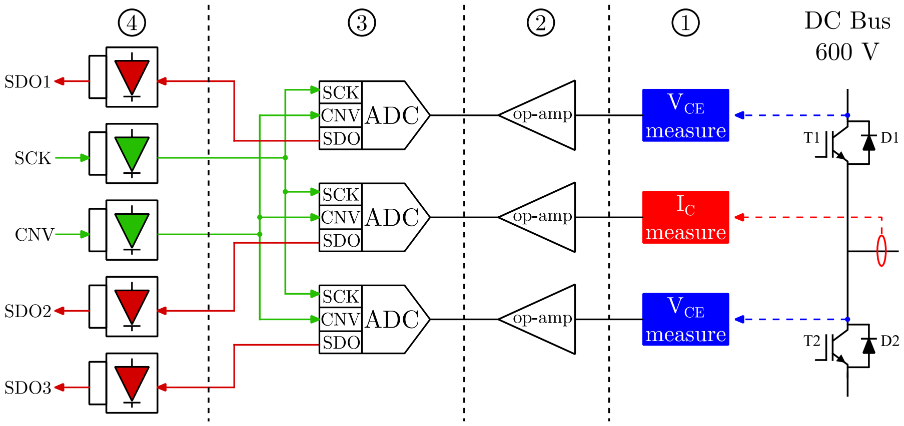
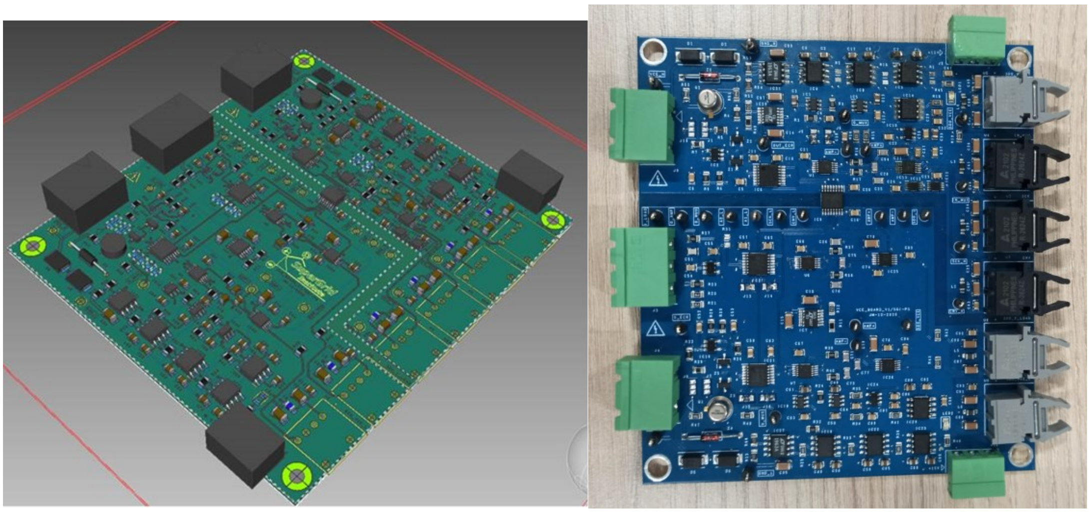


Figure 4.41. Concept for the V_{CE} measurement board

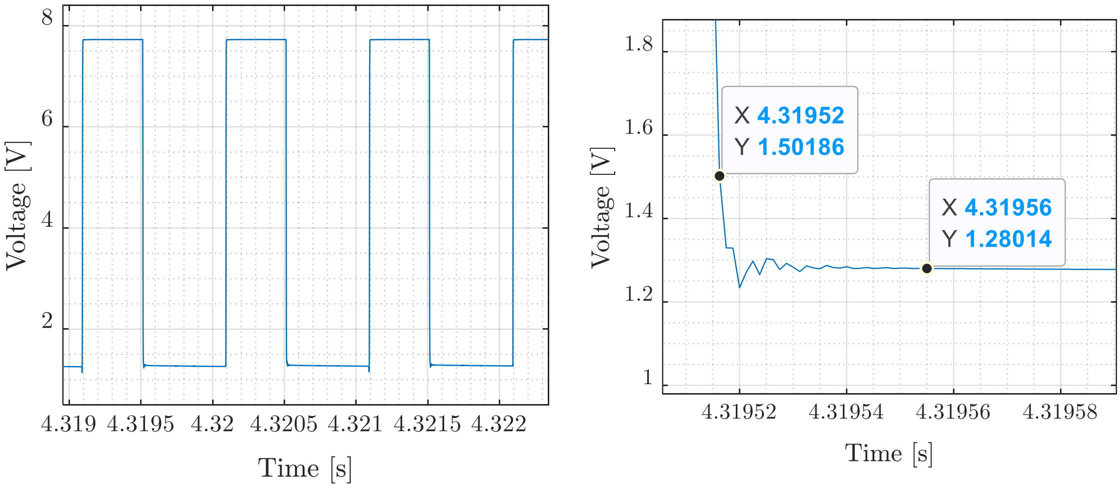
The circuit shown in Figure 4.40 is employed for the measurement of $V_{CE(sat)}$ and V_F. A LEM sensor LF 210-S like the one from Figure 4.22 is interfaced with the measurement board. From Figure 4.41 it can be seen that the measures are sent via an operational amplifier to 18-bit ADCs of reference AD7982BRMZ. The ADCs are then interfaced with fiber optic connectors that transmit the signals to the Speedgoat machine that deals with the supervision and the estimation of the junction temperature. The implemented circuit can be seen in Figure 4.42.



(a) (b)

Figure 4.42. V_{CE} board: (a) concept circuit, (b) final board

Some of the measurements performed with the V_{CE} board can be seen in Figure 4.43. In Figure 4.43 (a) the measured on-state voltage is approximate to 1.28 V. The higher voltage (near 7.7 V) shown in Figure 4.43 (a), corresponds to the saturated voltage output that the board generates when the concerned IGBT is turned off. Hence, this information will be used by the supervision machine for disregarding high-state voltage readings. In Figure 4.43 (b) it can be seen that the measurements are not accurate immediately after the switching actions. Therefore, the readings will only be used after a delay (300 µs) in order to avoid the transient region and obtain correct V_{CE} measurements.



(a) (b)

Figure 4.43. (a) V_{CE} measurements, (b) Zoom on measurements

4.5. Junction temperature estimation

As it was described previously the V_{CE} measurement board allows for the measure of $V_{CE(sat)}$ as well as I_{Load}. From these two inputs the current across each semiconductor device can be deduced. As the $V_{CE(sat)}$ is dependent on the collector current I_C and the junction temperature T_j of the device, the device temperature can be inferred from the readings of $V_{CE(sat)}$ and I_C. The procedure for the estimation of this temperature will be described in this section.

4.5.1. I-V Characterization

The direct characteristics of the IGBT semiconductors can be recovered from the device datasheet [288]. They were already depicted in Figure 4.14 (a). However, the data from Figure 4.14 (a) only has information relevant to two temperatures. The PLECs model of the DUT has greater information concerning the output characteristics of the DUT, as it has data from 6 different temperatures, from 25°C to 150° and by steps of 25°C. Nonetheless, for the sake of precision and discrepancy between modules, it was decided to perform static characterizations of the DUTs to be used. The characterizations of these devices were performed with the help of the power device analyzer B1506A from Keysight seen on Figure 4.44. The results of the characterizations of a DUT performed with the measurement equipment can be seen on Figure 4.45.

Figure 4.44. Power device analyzer B1506A

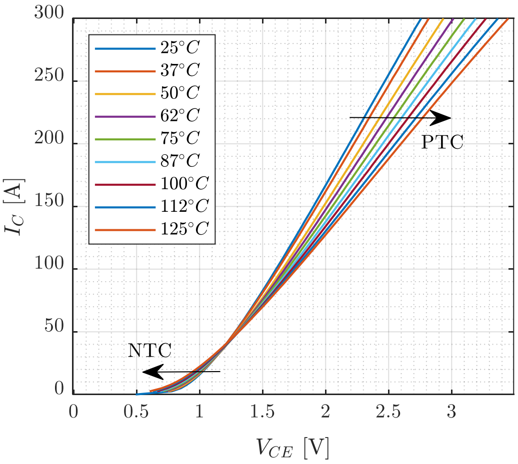


Figure 4.45. Output characteristics FF150R12KE3G, obtained with B1506A

As it can be seen from Figure 4.45, more temperature points were considered for having a more accurate database for performing junction temperature estimations considering the output characteristics of the DUT. Also, it is worth noting that the voltage was measured between the collector and the kelvin emitter terminal for improved accuracy.

4.5.2. Preliminary T_j estimation from I-V characterization

With the help from the I-V characterization, a method employing 2 stages of linear interpolations was developed for performing junction temperature estimations. This method consists in a first time, to perform a linear interpolation for calculating the $V_{CE(sat)}$ for all the temperatures of the database at the measured current I_C. This first stage can be better illustrated in Figure 4.46.

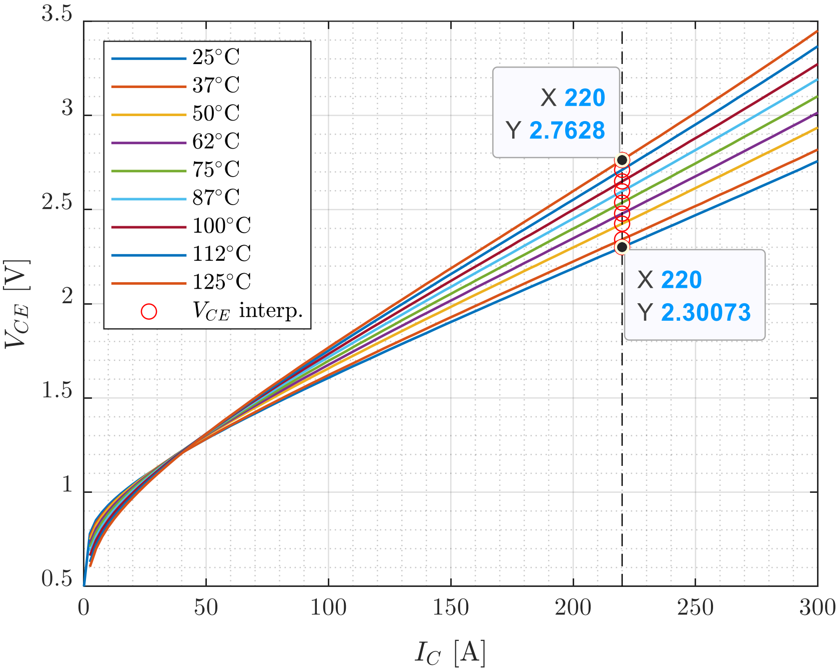


Figure 4.46. First stage of linear interpolations for calculation of $V_{CE(sat)}$ at different T_j and at the measured I_C

In Figure 4.46 the values of $V_{CE(sat)}$ for all the temperatures of the database at a measured collector current I_{meas} can be seen. In the previous example the measured current $I_{meas} = 220\,A$. The voltage values were computed employing a linear interpolant. Subsequently, the $V_{CE(sat)}$ values will be used for calculating the junction temperature corresponding to a measured collector-emitter voltage $V_{CE\,meas}$, this process is depicted in Figure 4.47.

In Figure 4.47 a quasi-linear dependency of T_j from the voltage V_{CE} at a fixed current I_C can be appreciated. The linear behavior is more noticeable at higher currents and facilitates the calculation of the device temperature. In the example from Figure 4.47, the $V_{CE\,meas} = 2.5\ V$. Then the corresponding junction temperature is calculated with a linear interpolation, in this example, the estimated junction temperature $T_j = 66.8\,°\mathrm{C}$.

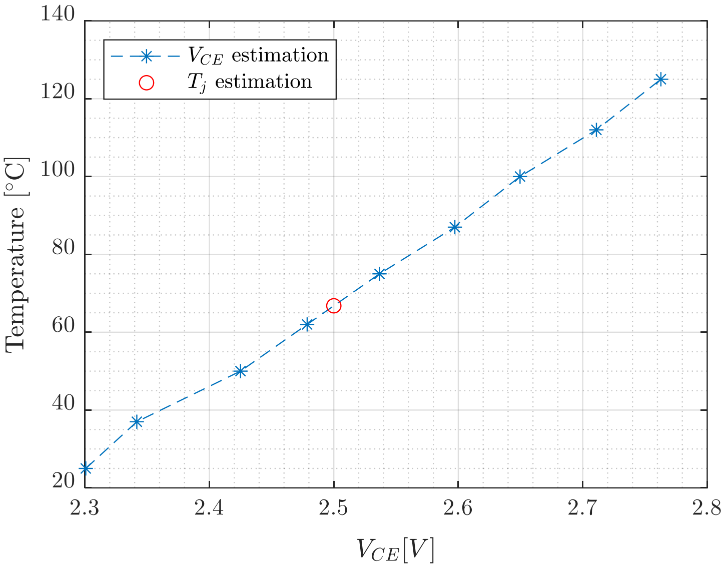


Figure 4.47. Second stage of linear interpolations for calculation of T_j at the measured voltage $V_{CE\ meas}$

From Figure 4.47 it can also be noticed that the linearity in the dependency of T_j from the V_{CE} voltage is not perfect, which might come from some measurement noise. Moreover, from Figure 4.45 and Figure 4.46 a singularity in the output characteristic curves can be seen. At this particular point, there can be many solutions for the junction temperatures corresponding to the measured I_C and V_{CE} pair. The singularity occurs at lower I_C currents, thus the estimations performed at low currents and at currents close to the singularity will lack in accuracy. However, at higher currents the T_j estimations will have improved accuracy.

4.5.2.1. V_{CE} calibration

In order to improve the accuracy of the V_{CE} measurements, as well as the estimation of the junction temperature T_j a correction gain $k_{V_{CE}}$ on the V_{CE} readings from coming from the V_{CE} board was implemented. This correction gain considers the singularity or cross-over point at which the IGBT characteristic changes from a negative temperature coefficient (NTC) to a positive temperature coefficient (PTC) (Figure 4.45). This was done for limiting the influence of the temperature on the measurements.

In order to calculate the correction gain $k_{V_{CE}}$, the cross-over point on the output characteristics seen in Figure 4.45 is used. It is worth reminding that these characteristic curves were obtained with the help of a high-precision B1506 curve tracer from Keysight. The cross-over point is found by verifying the value of $V_{CEmax} - V_{CEmin}$ at any given current. Then, the cross-over current is the current at which this difference is the lowest. Also, the mean value of V_{CE} at the cross-over current is retained and is considered as the theorical cross-over voltage $V_{CEcross-th}$. In Figure 4.46 the value of $V_{CEmax} - V_{CEmin}$ at a collector current of 220 A is 0.462 V. Therefore, the cross-over point will be found at a lower current.

Once the cross-over point is found on the characterization curves, the $k_{V_{CE}}$ is obtained thanks to Eq. (4.5).

$$k_{V_{CE}} = \frac{V_{CEcross-th}}{V_{CEcross-meas}} \tag{4.5}$$

In Eq. (4.5), $V_{CEcross-meas}$ is the V_{CE} measured with the V_{CE} board at the cross-over current obtained from the characterization curves. By applying the correction gain $k_{V_{CE}}$ to the readings from the V_{CE} board, they will match the output characteristics obtained with a high-precision curve tracer. Moreover, the calculation of this gain considers the cross-over point for eliminating any temperature dependency. Also, the correction gain is only applied to the voltage as $V_{CE} = f(I_C, T_j)$, since in this application, the collector current is imposed by the external circuit and is measured by a commercial LEM current transducer (Figure 4.22).

It is also worth mentioning that before applying the correction gain $k_{V_{CE}}$, the readings from the V_{CE} board were already calibrated. The calibration was performed with the help of the source meter unit (SMU) Keithley 2612B seen on Figure 4.48, in order to correct any internal gains and offsets internal to the V_{CE} board.

Figure 4.48. Source Meter Unit Keithley 2612B

4.5.3. Kalman filter for final T_j estimation

The method described in section 4.5.2 is not fully reliable for the whole current range of the power device. Hence, a Kalman filter was used as a mean to improve the accuracy of the previous T_j computation, particularly at low current values. A similar approach was undertaken in [101], where a Kalman filter was used for eliminating the noise from the online measurement of a TSEP.

The probabilistic background for using the Kalman filter was described in previous works [101], [127]. The Kalman filter is an optimal state estimator, which uses the information coming from a measurement y and from the prediction of a state x to compute a corrected estimation of the same state. It is a discrete tool that computes the optimal estimation of the states in two different stages: prediction and correction.

4.5.3.1. Thermal modeling

Before introducing the equations of the different stages of the Kalman filter algorithm, it is first necessary to develop the model of the studied process. The continuous state-space representation of a process can be seen in Eqs. (4.6)–(4.7).

$$\frac{dx}{dt} = Ax + Bu \tag{4.6}$$

$$y = Cx + Du \tag{4.7}$$

With:

- $x \in \mathbb{R}^n$: state vector
- $u \in \mathbb{R}^m$: input vector
- $y \in \mathbb{R}^p$: output vector
- A: state matrix
- B: input matrix
- C: output matrix
- D: feedforward matrix

The process to be modeled is the thermal behavior of the semiconductors of the DUT. As it was previously seen in section 3.2.2, there are two ways of representing the thermal network of a semiconductor device. For deploying the Kalman filter algorithm it is crucial to optimize the computation time, hence the Foster (Figure 3.8) representation was chosen. In this representation the number of operations is reduced since the state matrix A is diagonal.

In [127] not only the self-heating path of the IGBTs was considered, but also the thermal cross-coupling of the diodes antiparallel to the IGBTs. However, in this research, the cross-coupling will not be considered, especially since its influence at low currents is almost negligible. In Figure 4.49 an internal layout of the module depicting the IGBT chip and its corresponding antiparallel diode chip can be seen.

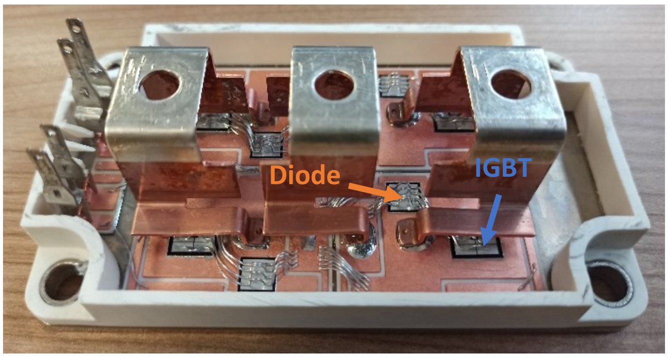


Figure 4.49. Internal layout of the DUT

The datasheet provides information about the self-heating thermal path (Figure 4.14 (c)). However, it was chosen to perform characterizations of the thermal path of the semiconductors with the thermal impedance analyzer Phase 12 from Analysis Tech, seen on Figure 4.50. These characterizations were carried out to account for the disparities between the datasheet and the measured behavior of each individual component. The Phase 12 analyzer was used for characterizing both the self-heating path and the cross-coupling path with the antiparallel diode, as seen on Figure 4.51.

Figure 4.50. Phase 12 Thermal Impedance Analyzer

It can be seen on Figure 4.51, that there is a noticeable difference between the datasheet information and the characterizations corresponding to the thermal impedance of the self-heating path. It can also be seen that the cross-coupling thermal impedance is not as relevant as the self-heating thermal impedance. Thus, this information will not be considered in the model employed for the Kalman filter algorithm.

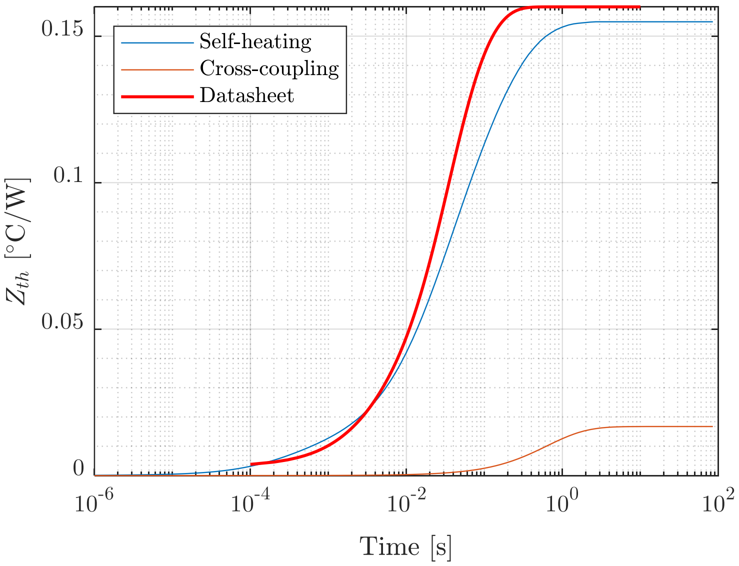


Figure 4.51. Thermal impedance characterizations

As it was mentioned previously, Foster networks were employed for the thermal model to be used in the Kalman filter. Hence, the characterization data seen on Figure 4.51 was fitted to a fourth order ($n = 4$) Foster thermal network conforming with the expression in Eq. (4.8).

$$Z_{th} = \sum_{i=1}^{n} R_{th,i}\left(1 - e^{-\frac{t}{R_{th,i}\cdot C_{th,i}}}\right) = \sum_{i=1}^{n} R_{th,i}\left(1 - e^{-\frac{t}{\tau_{th,i}}}\right) \quad \mathbf{(4.8)}$$

Where:

- Z_{th}: thermal impedance
- R_{th}: thermal resistance
- C_{th}: thermal capacitance
- τ_{th}: thermal time constant

The fitted data for the fourth order Foster thermal model for the thermal impedance curves seen on Figure 4.51 can be seen on Table 4.3. The fitting was performed employing the least-squares regression model.

Thermal impedance	**Parameter**	**Unit**	**Values for the Foster layers**			
Self-heating	R_{th}	°C/W	9.43e-3	3.47e-2	6.77e-2	4.30e-2
	C_{th}	$J/°C$	3.58e-2	0.332	0.827	6.467

Table 4.3 Fitted values for a fourth order Foster thermal network

With the fitted data, the state-space representation from Eqs. (4.6) and (4.7) can be expressed as:

$$\frac{d}{dt}\begin{bmatrix}\Delta T_1\\ \Delta T_2\\ \Delta T_3\\ \Delta T_4\end{bmatrix} = \begin{bmatrix}\frac{-1}{R_{th,1}\cdot C_{th,1}} & 0 & 0 & 0\\ 0 & \frac{-1}{R_{th,2}\cdot C_{th,2}} & 0 & 0\\ 0 & 0 & \frac{-1}{R_{th,3}\cdot C_{th,3}} & 0\\ 0 & 0 & 0 & \frac{-1}{R_{th,4}\cdot C_{th,4}}\end{bmatrix}\begin{bmatrix}\Delta T_1\\ \Delta T_2\\ \Delta T_3\\ \Delta T_4\end{bmatrix} + \begin{bmatrix}\frac{1}{C_{th,1}} & 0\\ \frac{1}{C_{th,2}} & 0\\ \frac{1}{C_{th,3}} & 0\\ \frac{1}{C_{th,4}} & 0\end{bmatrix}\begin{bmatrix}\Phi_{IGBT}\\ T_c\end{bmatrix} \tag{4.9}$$

$$y = T_{j,IGBT} = \begin{bmatrix}1 & 1 & 1 & 1\end{bmatrix}\begin{bmatrix}\Delta T_1\\ \Delta T_2\\ \Delta T_3\\ \Delta T_4\end{bmatrix} + \begin{bmatrix}0 & 1\end{bmatrix}\begin{bmatrix}\Phi_{IGBT}\\ T_c\end{bmatrix} \tag{4.10}$$

With:

State vector: $x = \begin{bmatrix}\Delta T_1\\ \Delta T_2\\ \Delta T_3\\ \Delta T_4\end{bmatrix}$; Input vector: $u = \begin{bmatrix}\Phi_{IGBT}\\ T_c\end{bmatrix}$; Output vector: $y = [T_{j,IGBT}]$

- $\Delta T \in \mathbb{R}^4$: thermal increase in the Foster layers of the thermal network corresponding to the IGBT self-heating path
- $\Phi_{IGBT} \in \mathbb{R}$: power losses originated in the IGBT
- $T_c \in \mathbb{R}$: temperature measured with PT1000 sensors at the interface of the cold-plate and the DUT case
- $T_{j,IGBT} \in \mathbb{R}$: junction temperature of the IGBT
- $R_{th}, C_{th}, \tau_{th} \in \mathbb{R}^4$: thermal resistances, capacitances and time-constants corresponding to the IGBT self-heating path

In order to be able to use the Kalman filter, the state space model from Eqs. (4.6) and (4.7) has to be discretized, yielding Eqs. (4.11) and (4.12):

$$x_{k+1} = A_d x_k + B_d u_k \tag{4.11}$$

$$y_k = C_d x_k + D_d u_k \tag{4.12}$$

With:

- $x_k \in \mathbb{R}^4$: discretized state vector at the current iteration
- $x_{k+1} \in \mathbb{R}^4$: discretized state vector at the next iteration
- $u_k \in \mathbb{R}^2$: discretized input vector at the current iteration
- $y_k \in \mathbb{R}^1$: discretized output vector at the current iteration
- $A_d \in \mathbb{R}^{4\times4}$: discretized state matrix
- $B_d \in \mathbb{R}^{4\times2}$: discretized input matrix
- $C_d \in \mathbb{R}^{1\times4}$: discretized output matrix
- $D_d \in \mathbb{R}^{1\times2}$: discretized feedforward matrix

The discretized model was obtained with the help of the MATLAB function c2d() with the zero-order hold method. This model will be employed in the Kalman filter algorithm.

4.5.3.2. Kalman filter background

Even though a process can be modeled with great precision, it will always be subject to perturbations and noises that might have not been considered at the modeling stage. Similarly, the measurement of a physical quantity is subjected to a measurement noise. Thus, the measurement will be different from the real output of the process. Therefore, it is necessary to consider the noises in both the process and in the measurement for the modeling of the Kalman filter as seen on Eqs. (4.13) and (4.14).

$$x_{k+1} = A_d x_k + B_d u_k + G w_k \tag{4.13}$$

$$y_k = C_d x_k + D_d u_k + v_k \tag{4.14}$$

In Eq. (4.13), the process noise is considered in the vector w as well as in the G matrix, that maps how the noise affects the system. In Eq. (4.14), the measurement noise is considered in the v vector.

Assuming that the process and measurement noises are Gaussian in nature with null mean value, it is possible to use the Kalman filter for obtaining an estimation $\widehat{T_j}$ of the junction temperature T_j of the IGBT. The basic principle behind the Kalman filter in this particular application, is to complement the measurement of T_j issued from the preliminary estimation from section 4.5.2 with the theoretical output of the model from Eqs. (4.11) and (4.12). Hence, the Kalman filter will combine a portion of both types of inputs to perform an optimal estimation of the real value of T_j.

The Kalman filter is chosen as to minimize the cost function seen on Eq. (4.15). In Eq. (4.15) x are the states of the system and $\hat{x}$ the state estimates.

$$J = E[(x-\hat{x})(x-\hat{x})^T] \tag{4.15}$$

By introducing the statistical information about the process noise w and the measurement noise v, the Kalman filter will make the calculations of the state estimate. Considering null expected values for both types of noises, the information required for the algorithm are the noise variances. As there are four states in the model from Eq. (4.11), the process noise w will be given by a four-element column vector. The variances of the process noises must be considered, but equally the covariances between each noise element. This information is expressed in a covariance matrix Q as seen on Eq. (4.16):

$$Q = E[ww^T] = \begin{bmatrix} V[w_1] & \cdots & cov[w_1, w_4] \\ \vdots & \ddots & \vdots \\ cov[w_4, w_1] & \cdots & V[w_4] \end{bmatrix} \tag{4.16}$$

Similarly, the variance of the measurement noise must be employed by the Kalman filter algorithm. This information is expressed in the covariance matrix R seen on Eq. (4.17). As there is only a single measurement, the covariance matrix R will be of dimension 1×1, hence a scalar value as seen on Eq. (4.17).

$$R = E[vv^T] = V[v] \tag{4.17}$$

4.5.3.3. Kalman filter algorithm

It was previously mentioned that the Kalman filter algorithm consists of two stages: prediction and correction. Both stages will be described in the following lines.

4.5.3.3.1. Prediction stage

This stage corresponds to the estimation based solely on the theoretical model. Hence, the obtained values are the expected theoretical values. The main expressions describing this stage are seen on Eqs. (4.18)-(4.20):

$$\hat{x}_{k|k-1} = A_d x_{k-1|k-1} + B_d u_k \tag{4.18}$$

$$P_{k|k-1} = A_d P_{k-1|k-1} {A_d}^T + Q_k \tag{4.19}$$

$$y_{k|k-1} = C_d \hat{x}_{k|k-1} + D_d u_k \tag{4.20}$$

With:

- $\hat{x}_{k|k-1} \in \mathbb{R}^4$: predicted a priori state estimate for the current iteration
- $x_{k-1|k-1} \in \mathbb{R}^4$: corrected a posteriori state estimate of the previous iteration
- $P_{k|k-1} \in \mathbb{R}^{4\times4}$: predicted covariance matrix of the a priori state error $e_k = x_k - \hat{x}_{k|k-1}$
- $P_{k-1|k-1} \in \mathbb{R}^{4\times4}$: corrected a posteriori covariance matrix for the previous iteration of the state error $\epsilon_{k-1} = x_{k-1} - x_{k-1|k-1}$
- $y_{k|k-1} \in \mathbb{R}^1$: prediction at the current iteration
- $u_k \in \mathbb{R}^2$: system inputs for the current iteration

4.5.3.3.2. Correction stage

This second stage aims to improve the prediction by considering the measurement of T_j issued from the preliminary estimation. The calculations performed in this stage intend to find the optimal proportion or the degree of confidence to be attributed to the measurement and the prediction. This degree of confidence is expressed in the Kalman gain K. On the one hand, if the gain is equal to 0, it means that the output of the filter will be based only in the theoretical model. On the other hand, if the value of the Kalman gain is different to 0, it means that the output of the filter considers the measurement for the final estimation. The values of the Q and R matrices are used to determine the Kalman gain as seen on the expressions corresponding to the correction stage (Eqs. (4.21)-(4.25)).

$$\varepsilon_k = y_k - y_{k|k-1} = y_k - \left(C_d\hat{x}_{k|k-1} + D_d u_k\right) \tag{4.21}$$

$$S_k = C_d P_{k|k-1} {C_d}^T + R_k \tag{4.22}$$

$$K_k = P_{k|k-1} {C_d}^T {S_k}^{-1} \tag{4.23}$$

$$\hat{x}_{k|k} = \hat{x}_{k|k-1} + K_k \varepsilon_k \tag{4.24}$$

$$P_{k|k} = (I - K_k C_d) P_{k|k-1} \tag{4.25}$$

With:

- $\varepsilon_k \in \mathbb{R}^1$: residual at the current iteration between the measurement and the prediction
- $y_k \in \mathbb{R}^1$: measurement at the iteration k issued from the preliminary estimation
- $\hat{x}_{k|k} \in \mathbb{R}^4$: a posteriori state estimate at the current iteration

This stage is also known as the update stage, since the estate estimation is updated by considering the measurements.

4.5.3.4. Simplified Kalman filter algorithm

In the chosen model for describing the heating process of the IGBT semiconductors, there is not a noticeable evolution of the matrices defining the dynamics of the system. It is for this reason that the error covariance matrix $P_{k|k}$ converges to a steady-state value and the Kalman filter K_k will also converge to a constant value as seen on Figure 4.52.

Therefore, it is possible to simplify the calculations for the Kalman filter algorithm. The Kalman gain can be calculated in a previous offline stage, and the algorithm will still be able to function online for the estimation of the junction temperature.

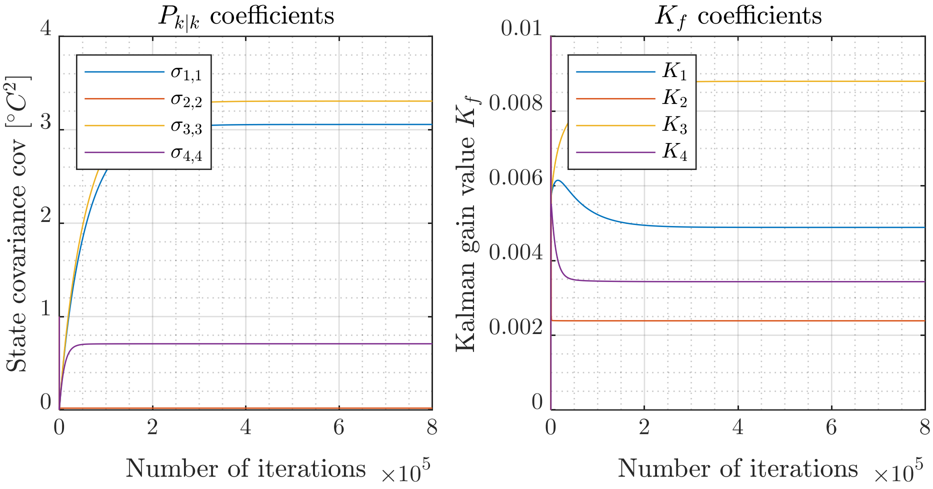


Figure 4.52. Evolution of the coefficients of the error covariance matrix $P_{k|k}$ and the Kalman gain K (Q and R values were chosen arbitrarily in this calculation)

4.5.3.4.1. Prediction stage

$$\hat{x}_{k|k-1} = A_d x_{k-1|k-1} + B_d u_k \tag{4.26}$$

$$y_{k|k-1} = C_d \hat{x}_{k|k-1} + D_d u_k \tag{4.27}$$

Differently from the calculations seen on section 4.5.3.3.1, the covariance matrix of the state error was calculated offline to determine the Kalman gain.

4.5.3.4.2. Correction stage

$$\hat{x}_{k|k} = \hat{x}_{k|k-1} + a \cdot K_f \left(y_k - y_{k|k-1}\right) \tag{4.28}$$

$$y_{k|k} = C_d \hat{x}_{k|k} + D_d u_k \tag{4.29}$$

With:

- $K_f \in \mathbb{R}^{4\times1}$: steady-state Kalman gain values calculated offline
- $a \in \mathbb{B}$: Boolean variable for determining the use of the measurement in the Kalman filter algorithm

It was seen on section 4.5.2, that the preliminary estimation of T_j with the linear interpolations based on the readings of V_{CE} and I_C did not yield satisfactory results for the complete range of currents. It was already mentioned that this preliminary estimation will be more accurate at higher I_C values. Therefore, the variable a seen in Eq. (4.28), allows to incorporate the measurement into the algorithm, only once a certain current threshold is met. Since there is a high sensibility of T_j in respect to the pair (V_{CE}, I_C), the variable a will allow the algorithm to consider the measurements, only if they allow for a better estimation of T_j. Below the current threshold, only the model prediction will be considered. Having simplified the Kalman filter algorithm the resulting block diagram can be seen in Figure 4.53.

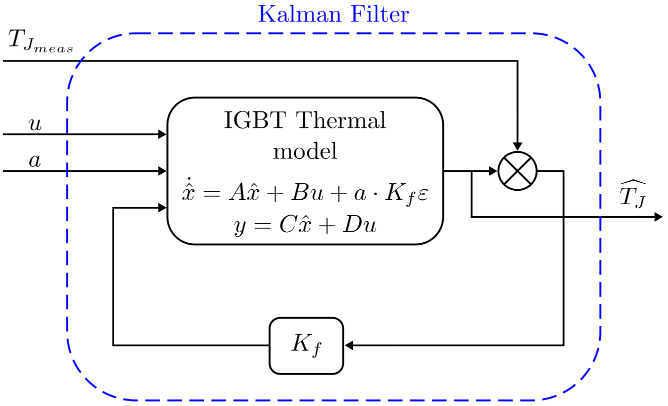


Figure 4.53. Simplified Kalman filter block diagram

4.5.4. Autocovariance Least-Squares method

It was seen in the previous paragraph that the noise covariance matrices Q and R play a fundamental role in the calculation of the Kalman gain as expressed in Eqs. (4.19), (4.22) and (4.23). This supposes that a previous knowledge on the nature of the noises present in the system and in the measurement acquisition chain must be known, for having an effective calculation of the Kalman gain and thus an accurate state estimation.

In most applications, these matrices are unknown to the end-user of the Kalman filter. Hence, the values employed in the covariance matrices are guessed by making assumptions on the characteristics of the process and on the noise present in the observations. If close enough assumptions are made, the Kalman filter will converge to the optimal estimation. However, this convergence can happen after several time intervals or never happen, if the initial assumptions are far from the real Q and R values. This work intends to improve the accuracy of the Kalman filter for T_j estimation by correctly identifying the covariance matrices with the help of the Autocovariance Least-Squares (ALS) method [295], [296].

The ALS method is an empirical method which allows to obtain an estimate of the covariance matrices Q and R. The main principle behind this method is to obtain residuals from a Kalman filter parametrized with an arbitrary Kalman gain L. Afterwards, an optimization problem must be solved to provide the values of Q and R. It is based on the notion that the outputs of the system contain information on both observation and process noise, when being compared to the predicted outputs.

If Eq. (4.28) is simplified and expressed in terms of the residuals and the arbitrary gain L, when the measurements are available, it yields:

$$\hat{x}_{k|k} = \hat{x}_{k|k-1} + L\left(y_k - y_{k|k-1}\right) = \hat{x}_{k|k-1} + L\,\varepsilon_k \tag{4.30}$$

Then, the residuals can be calculated for a certain number of iterations N_d. A sufficient large value of N_d, is required to guarantee a zero mean prediction error when using the ALS method. Then, it is possible to construct the vector ε which contains the residuals ε_k with $k \in \{0; \dots; N_d\}$. Subsequently, the expected value of ε_k with a lagged version of itself can be calculated as an intermediate step of the method. This calculation is expressed in Eq. (4.31).

$$\mathcal{C}_{(j)} = E\left[\varepsilon_k \, \varepsilon_{k+j}{}^T\right] \tag{4.31}$$

In Eq. (4.31) j represents the number of lagged iterations. Also, N is a user defined variable for the maximum number of lags to be evaluated. Hence, if $\mathcal{C}_{(j)}$ is evaluated between $j = 0$ and $j = N - 1$, it can be calculated from its own residuals by means of Eq. (4.32). Practically, the expected value from Eq. (4.31) can be computed using the time average seen on Eq. (4.32).

$$\mathcal{C}_{(j)} = \frac{1}{N_d - j} \sum_{i=1}^{N_d - j} \varepsilon_i \, \varepsilon_{i+j}{}^T \tag{4.32}$$

Subsequently, the ALS method demands that all the $\mathcal{C}_{(j)}$ coefficients to be arranged in the form of the autocovariance matrix (ACM) $\mathcal{R}(N)$ expressed in Eq. (4.33).

$$\mathcal{R}(N) = \begin{bmatrix} \mathcal{C}_0 & \cdots & \mathcal{C}_{N-1} \\ \vdots & \ddots & \vdots \\ \mathcal{C}_{N-1}{}^T & \cdots & \mathcal{C}_0 \end{bmatrix} \tag{4.33}$$

Then, the ACM is reorganized in a column vector b as expressed in Eq. (4.34). In MATLAB the command reshape() is used for stacking the columns of a matrix.

$$b = \operatorname{vec}\big(\mathcal{R}(N)\big) \tag{4.34}$$

In [295] it is explained that the covariance matrices Q and R are present in the expression given by Eq. (4.35).

$$M \begin{bmatrix} Q_{1,1} \\ Q_{2,1} \\ \vdots \\ Q_{4,4} \\ R_{1,1} \end{bmatrix} = b \tag{4.35}$$

In Eq. (4.35) the matrix M is constructed as specified in [295]. The computation of this matrix can be a long procedure, which is detailed in Appendix A.5. It can be seen that in Eq. (4.35) that the terms of the covariance matrices are arranged in a column vector. This expression can also be written as Eq. (4.36), where $\theta \in \mathbb{R}^{17\times 1}$.

$$M\theta = b \tag{4.36}$$

Therefore, the solution vector reduces the problem of the estimation of Q and R to a least-squares problem expressed in Eq. (4.37).

$$\hat{\theta} = \underset{\theta}{arg_{min}} \, \|M\theta - b\|_2{}^2 \tag{4.37}$$

Where the solution vector contains the optimal estimations of the matrices Q and R respectively, as indicated in Eq. (4.38). In this expression $\big(\hat{Q}\big)_s$ and $\big(\hat{R}\big)_s$ are the vectorized forms of the estimated covariance matrices.

$$\hat{\theta} = \left[\big(\hat{Q}\big)_s^T \, \big(\hat{R}\big)_s^T\right]^T \tag{4.38}$$

4.5.4.1. Conditions for applying the ALS method

The ALS method can be applied only if three conditions are met [295], [296].

Condition 1: The thermal model must be detectable

A system is detectable if its non-observable states are stable. In the case of the model used for the Kalman filter, it can be noticed that all the poles in Eq. (4.9) are stable. This is the case since all of them are negative.

Condition 2: The state estimate expected value must converge

The state estimate error can be expressed as Eq. (4.39). In this expression x_k are the states real values at iteration k, whereas $\hat{x}_{k|k-1}$ represents the predicted a priori state estimations at iteration k.

$$e_k = x_k - \hat{x}_{k|k-1} \tag{4.39}$$

When substituting Eqs. (4.13), (4.14) corresponding to the original model, Eqs. (4.18), (4.24) corresponding to the Kalman algorithm, and using a non-optimal gain L, into Eq. (4.39), then Eq. (4.40) can be obtained.

$$e_{k+1} = (A_d - A_d L C_d) e_k + G w_k - A_d L v_k \tag{4.40}$$

The ALS method requires that $E[e_k] \to 0$, so that the coefficients in matrix $P_{k|k}$ stabilize. Therefore, the expression of the expected value of the state estimate error is given by Eq. (4.41).

$$E[e_{k+1}] = E[(A_d - A_d L C_d) e_k + G w_k - A_d L v_k] \tag{4.41}$$

Developing Eq. (4.41) yields:

$$E[e_{k+1}] = (A_d - A_d L C_d)\, E[e_k] + G\, E[w_k] - A_d L\, E[v_k] \tag{4.42}$$

Since the noise have a null mean value, then Eq. (4.43) can be obtained.

$$E[e_{k+1}] = (A_d - A_d L C_d)\, E[e_k] \tag{4.43}$$

Consequently from Eq. (4.43), Eq. (4.44) can be finally deduced:

$$E[e_k] = (A_d - A_d L C_d)^k\, E[e_0] \tag{4.44}$$

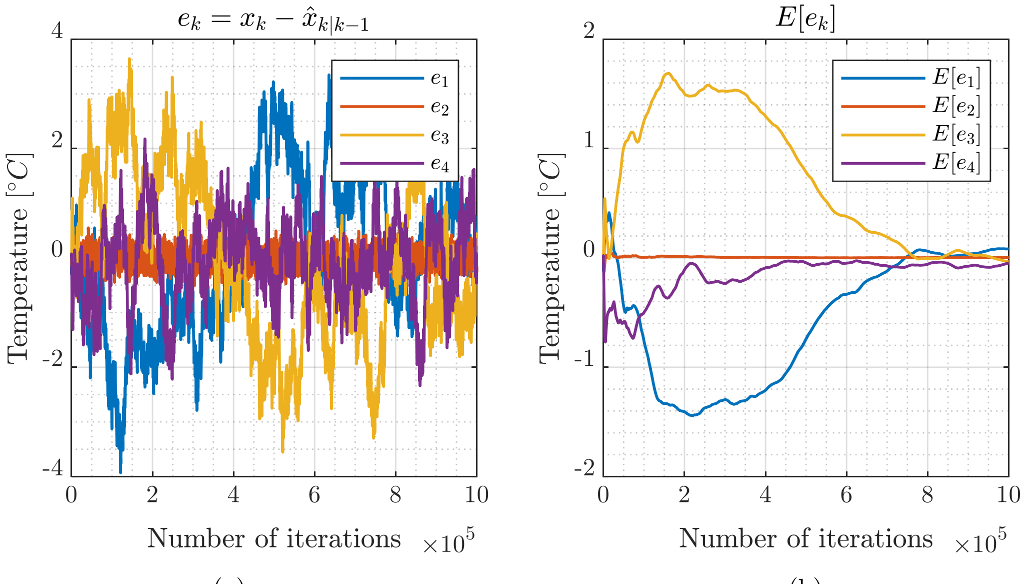
This implies that in order to have a convergent e_k, the eigenvalues of $(A_d - A_d L C_d)$ must be stable. Or expressed otherwise in Eq. (4.45).

$$\mathrm{eig}(A_d - A_d L C_d) < 0 \tag{4.45}$$

Condition 3: A large number of iterations must be considered

The number of iterations N_d for constructing the residual vector $\varepsilon = \begin{bmatrix} \varepsilon_0 \\ \varepsilon_1 \\ \vdots \\ \varepsilon_{N_d} \end{bmatrix}$ must be large enough, so that $E[e_k] \to 0$. If this condition is met, the coefficients of the covariance matrix $P_{k|k}$ will have a steady-state value. The number of iterations N_d to consider depends on the eigenvalues of $(A_d - A_d L C_d)$. Poles with large time constants will take a greater number of iterations to converge.

A more graphic illustration of the convergence of the expected value of the state estimates can be appreciated in Figure 4.54.



(a) (b)

Figure 4.54. (a) State estimate error, (b) Expected value of state estimate error

From Figure 4.54 (b) it can be seen that the expected value of the error $E[e_k]$ approaches 0 after nearly 800 000 iterations. Some of the coefficients take longer to converge, since there are different dynamics for the poles of $(A_d - A_d L C_d)$.

4.5.4.2. Validation of the ALS method

In order to validate the accuracy improvement provided by the use of the ALS method a simulation was carried out. The response of the Kalman filter when submitted to a step excitation was analyzed. The process for this validation is as follows:

First, the process and measurement noises w_k and v_k were synthetically simulated and added to the model in accordance with Eqs. (4.13) and (4.14). The fictive noise vectors are created from arbitrarily defined covariance matrices Q and R such that:

$$w_k \sim \mathcal{N}(0, Q) \tag{4.46}$$

$$v_k \sim \mathcal{N}(0, R) \tag{4.47}$$

In Eqs. (4.46) and (4.47) $\mathcal{N}$ represents the normal distribution. It can be seen that the mean value is null for both noise vectors. The covariance matrices used for the generation of the noise vectors are:

$$Q = 2 \cdot 10^{-4} \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}, R = 2.5$$

The aim of this validation is to recalculate the covariance matrices Q and R. The ALS method estates that these matrices can be obtained even when a non-optimal Kalman gain L is used for the generation of residuals. In order to calculate the non-optimal gain L, different matrices from the original ones were used. The values of the wrong matrices are:

$$Q = 200 \cdot 10^{-4} \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}, R = 0.005$$

The gain L is calculated by using Eq. (4.23), with the wrong Q and R matrices. Hence, K_k in Eq. (4.23) will be replaced by L, since it is not the optimal gain. In Figure 4.55, the performance of the Kalman filter can be seen when using the non-optimal gain.

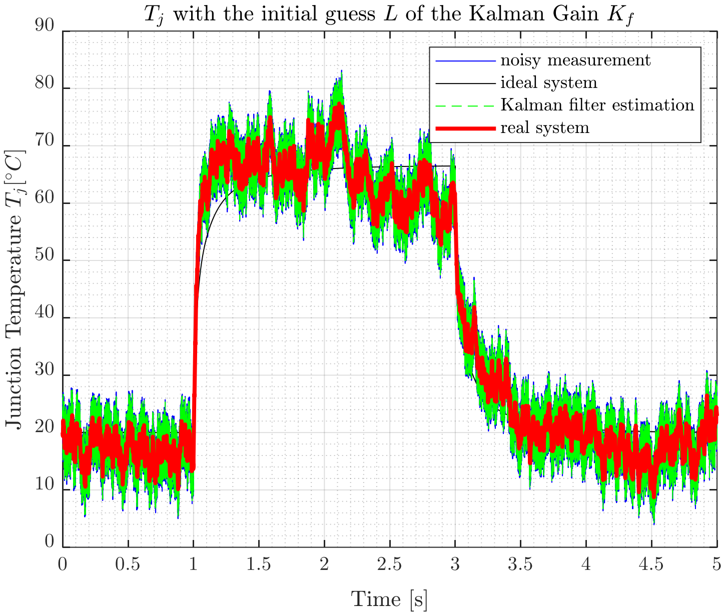


Figure 4.55. Kalman filter performance when using a non-optimal gain

After performing 4M iterations the residual vector ε is obtained and the ALS algorithm should return the correct Q and R matrices. However, the estimated noise covariance matrices $\hat{Q}$ and $\hat{R}$ obtained are:

$$\hat{Q} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0.0020 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}, \hat{R} = 2.4956$$

At a first regard, the estimated noise covariance matrices are incorrect and should result in a poor performance of the Kalman filter. However, when using $\hat{Q}$ and $\hat{R}$ the response of the Kalman filter is satisfactory, as evidenced in Figure 4.56. The filter built with $\hat{Q}$ and $\hat{R}$ has a much superior performance than the one built with a non-optimal gain as verified in Figure 4.55. The good performance of the method can be attributed to the fact that several noise configurations can lead to the same distortion of the output of the system. Moreover, a response of the Kalman filter when using the known Q and R covariance matrices can be seen in Figure 4.57. By comparison of Figure 4.56 and Figure 4.57, it can be seen that the performance of the filter is almost identical, even if different

Q and R values were used for the synthesis of the filter. Therefore, the ALS method can compute different configurations of $\hat{Q}$ and $\hat{R}$ that give satisfactory results when used with the Kalman algorithm.

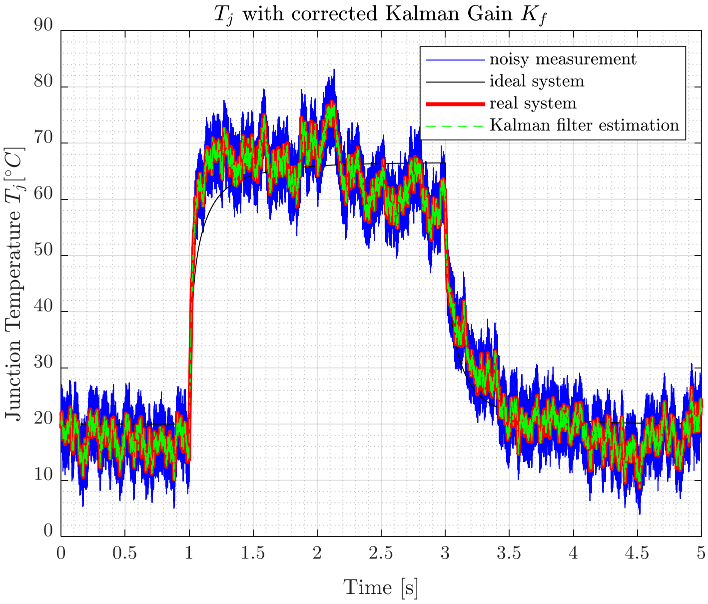


Figure 4.56. Kalman filter performance when using $\hat{Q}$ and $\hat{R}$

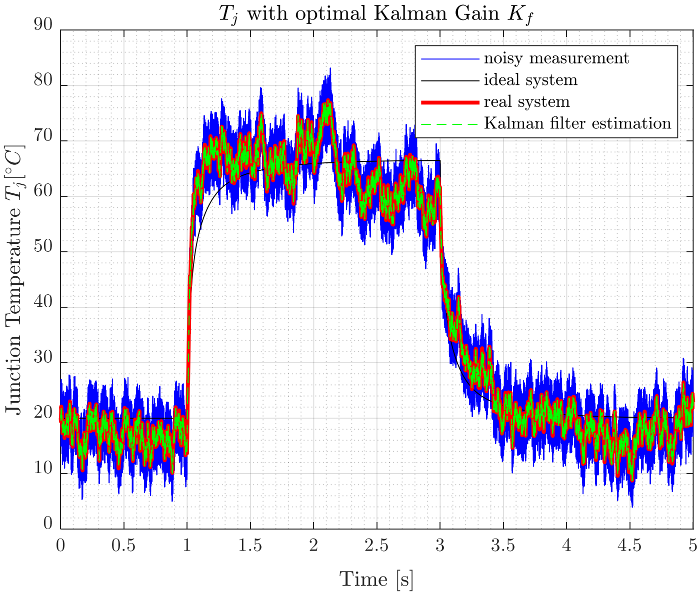


Figure 4.57. Kalman filter performance with known Q and R matrices

4.5.5. Validation of T_j estimation with fiber optics measurement

In order to validate the methodology for the estimation of T_j a similar approach to the one considered in [297] was performed. This approach is based on the use of fiber optics sensors for the measurement of T_j. In this work a CoreSens signal conditioner from OpSens is used, as well as the fiber optics sensors OTG-F, which can be seen in Figure 4.58.

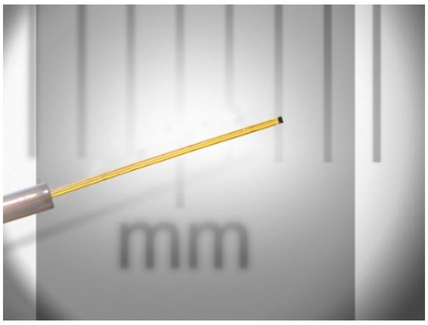


Figure 4.58. OpSens fiber optic sensor OTG-F

The sensor from Figure 4.58 employs a technique based on temperature-dependent bandgap of GaAs crystal as the temperature transduction mechanism. This mechanism provides the sensor with a high accuracy and repeatability and most important EMI immunity, which makes it ideal for switching converter applications. Additionally, this measurement technique is electrically isolated and has a bandwidth of 1 kHz.

For the implementation of the measurement, the crystal at the tip of the sensor must make contact with the element to be measured. Hence, it was required to perform perforations to the DUT for the installation of the sensors. Additionally, ceramic tube guides were used for assuring that the sensors reach the junction of the semiconductor and fixing the sensor placement. This implementation can be seen in Figure 4.59.

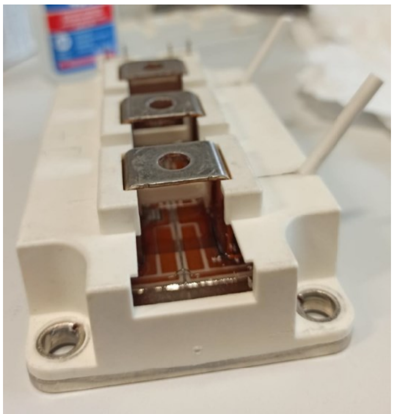


Figure 4.59. Implementation of fiber optics measurement of T_j

The placement of the sensor is of the outmost importance. In order to have a correct placement, static and dynamic tests were performed. The static and dynamic measurements were compared against characterization results obtained with the Phase 12 thermal impedance analyzer from Figure 4.50. The fiber optic sensor is moved until its performance approaches the results of the measurement with the thermal impedance analyzer. Consequently, the position of the sensor is fixed. The results comparing the dynamic characteristics of both measurements can be shown on Figure 4.60.

Some differences between the performance of both systems are evidenced in Figure 4.60. There is a static error on the one side and a difference in the dynamics of both systems. These differences can be explained as different cooling systems (chiller and cold-plate) are associated with each of the measurement devices. The measurements seen in Figure 4.60 use the water temperature as the reference for the measurements.

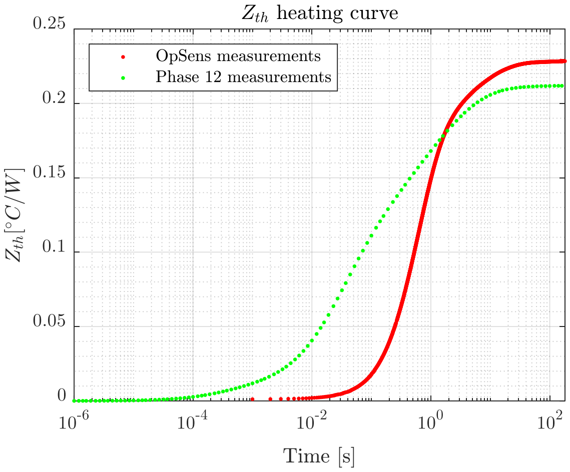
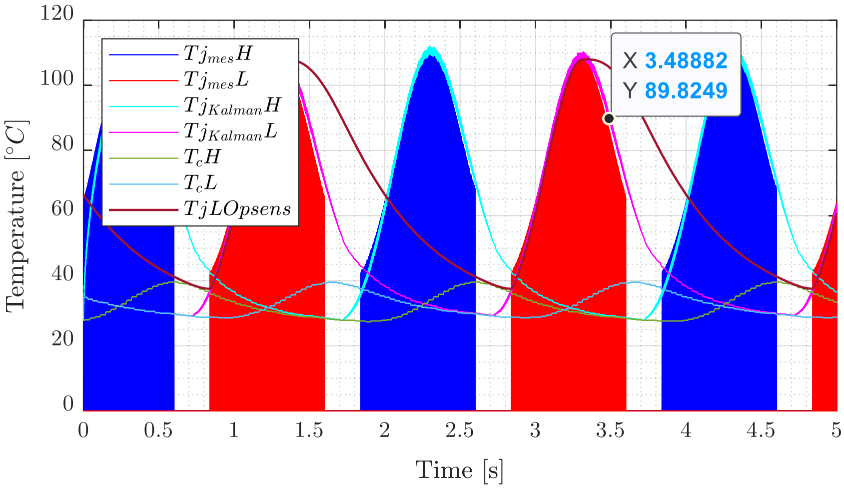
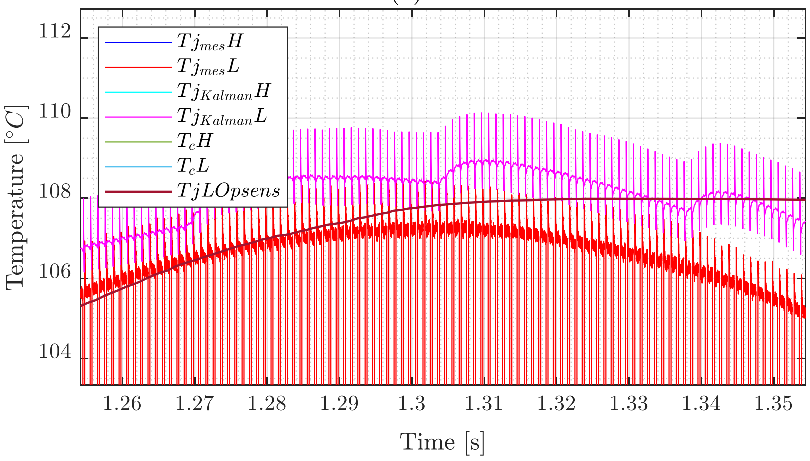


Figure 4.60. Comparison of the thermal response of OpSens fiber optic system against Phase 12 thermal impedance analyzer

Once the positioning of the fiber optic sensors is defined, this measurement is employed for the validation of the T_j estimations obtained with the Kalman filter discussed in section 4.5.3. The resulting measurements can be seen in Figure 4.61.



(a)



(b)

Figure 4.61. Resulting T_j measurements

In Figure 4.61 it can be appreciated that the estimation T_j is really similar to the measured temperature with the fiber optic sensors. This is especially true when heating the device (Figure 4.61 (a)). At the cooling phase, there is a slight difference. This can be attributed to the fact that the sensor performs differently at the cooling phase. However, it can be seen that the maximum value estimated, and the measured maximum temperature are nearly identical as evidenced on Figure 4.61 (b). Therefore, this measurement has validated the approach for the estimation of T_j.

4.6. Power cycling experiments

As it was already mentioned, the AC PC test circuit allows for the testing of both IGBT and diode devices. It was also mentioned that the power factor allows for controlling the repartition of the losses among the different semiconductors. In this particular case a $PF = 1$ will be employed so that most of the power losses, and hence, thermal stress is applied to the IGBT devices.

However, before applying the cycling protocols it is necessary to define a statistical background for deciding the number of tests to perform. It is also necessary, to calculate the estimated duration of the different cycling conditions to be imposed to the semiconductors. These calculations will be described in the following paragraphs.

4.6.1. Statistical background for cycling tests

The main statistical tool for describing the end-of-life phenomena is the Weibull distribution. This distribution was already described in Eq. (3.28) and it has been popularized in reliability engineering for analyzing life data [257]. However, some other statistical considerations must be considered for determining the conditions for the power cycling protocol. They will be mentioned in the following lines.

4.6.1.1. Median Rank

The calculation of this parameter was presented in [257], [298] for helping determine the number of samples to be considered per cycling condition applied. This parameter indicates the cumulative probability of failure corresponding to the k^{th} failure out of a sample of N units at the 50% confidence level [299]. The approximations done by the Median Rank correspond to a binomial distribution. This value can be obtained by employing the Benard's approximation seen on Eq. (4.48).

$$MR = \frac{k - 0.3}{N + 0.4} \tag{4.48}$$

The medium rank was computed for several sample sizes, the results expressed in percentages can be seen in Table 4.4.

k^{th} failure	Sample size N									
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
1	50.00	29.17	20.59	15.91	12.96	10.94	9.46	8.33	7.45	6.73
2		70.83	50.00	38.64	31.48	26.56	22.97	20.24	18.09	16.35
3			79.41	61.36	50.00	42.19	36.49	32.14	28.72	25.96
4				84.09	68.52	57.81	50.00	44.05	39.36	35.58
5					87.04	73.44	63.51	55.95	50.00	45.19
6						89.06	77.03	67.86	60.64	54.81
7							90.54	79.76	71.28	64.42
8								91.67	81.91	74.04
9									92.55	83.65
10										93.27

Table 4.4 Median Rank for each failure according to sample size (in percentage) [257]

4.6.1.2. Sample size estimation

Testing a large number of samples gives more accurate results. However, having a large sample size can be quite costly and time consuming. Therefore, it is crucial to make an accurate estimation of the correct sample size for performing reliability tests.

An indicator for calculating the sample size is the uncertainty. It can be calculated from the median ranks calculations [257], [298], performed in Table 4.4. The formulation of the uncertainty based on the median ranks calculation can be seen in Eq. (4.49).

$$Uncertainty = 1 - \left(MR_{highest} - MR_{lowest}\right) \tag{4.49}$$

Figure 4.62 depicts the calculation of the uncertainty for different sample sizes. From Figure 4.62 it can be seen that for large sample sizes, as the number of sample increases, the decrease in uncertainty is not as relevant as for small sample sizes. The region of interest for choosing the number of samples is the knee of the curve (between 6 and 12 samples). The minimum number of samples, 6 is chosen for testing several PC conditions.

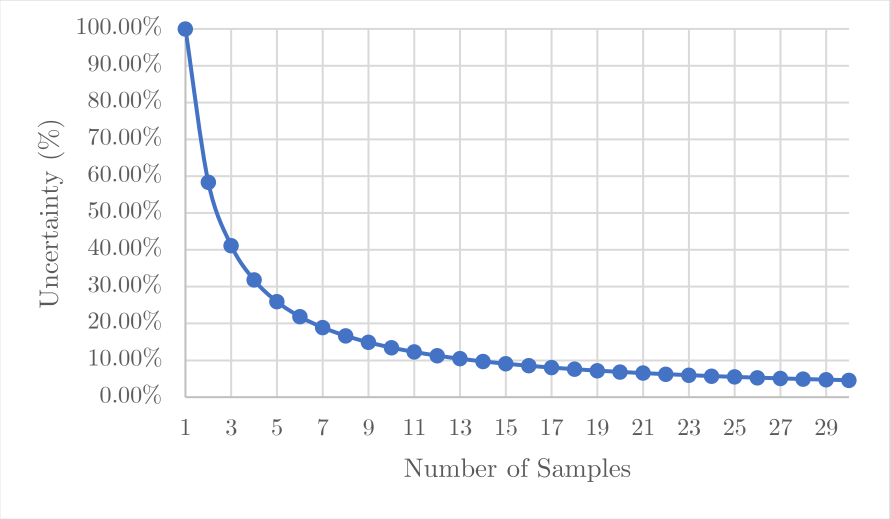


Figure 4.62. Uncertainty calculation according to sample size

4.6.2. Calculation of power cycling conditions

The principal lifetime models of IGBT power devices were presented in Table 1.6. In these lifetime models the main stressors are temperature dependent. Perhaps the more important stressor in the existing lifetime models, is the temperature swing ΔT_j experienced by the device. Other relevant parameters are the duration of the thermal cycles t_{cycle} and the reference temperature at which the cycling protocol was undertaken. This temperature reference can be either the mean temperature T_{mean}, the highest junction temperature $T_{j_{max}}$ or the minimum junction temperature $T_{j_{min}}$.

The Bayerer lifetime model shown in Eq. (1.5), is dependent on all the previous stressors. Moreover, this model depends on other characteristics of the studied device, which makes it the preferred model for performing reliability tests. Thus, this lifetime model was considered as the basis for the determination of the PC conditions.

The proposed cycling protocols to be implemented aim to evaluate the influence of the main temperature dependent stressors of the Bayerer model: ΔT_j, $T_{j_{min}}$and t_{on}, which represents the heating time. In this particular study, the ΔT_j will be controlled by the amplitude of the sinusoidal current $I(t)$ to be applied to the load. The $T_{j_{min}}$ will be imposed by the reference temperature set with the external chiller, as the power device will be cooled until reaching the cold plate temperature. Finally, the t_{on} will be controlled thanks to the output frequency of the load current. Additionally, a constant switching frequency f_{sw} of 1 kHz will be used. The test conditions and its estimated duration can be seen on Table 4.5. The coefficients of the Bayerer model for the calculation of the duration of the tests can be seen in Table 4.6 [144].

Condition	$\boldsymbol{\Delta T_j}$ [°C]	$\boldsymbol{T_{j_{min}}}$ [°C]	$\boldsymbol{t_{on}}$ [s]	Estimated Cycles to failure $\boldsymbol{N_f}$	Estimated Days to failure
1	80	40	1	3.85E+05	8.9
2	90	40	1	2.29E+05	5.3
3	70	40	1	6.95E+05	16.1
4	90	40	5	1.09E+05	12.6
5	90	40	10	7.89E+04	18.3
6	70	60	1	5.43E+05	12.6
7	70	50	1	6.12E+05	14.2
8	70/80/90	40/50/60	1/5/10	4.37E+05	12.1
Total					100.1

Table 4.5 Power cycling conditions and the estimated duration of the tests

Coefficient	$\boldsymbol{A}$	$\boldsymbol{\beta_1}$	$\boldsymbol{\beta_2}$	$\boldsymbol{\beta_3}$	$\boldsymbol{\beta_4}$	$\boldsymbol{\beta_5}$	$\boldsymbol{\beta_6}$
Value	2.03E+14	-4.416	1285	-0.463	-0.716	-0.761	-0.5

Table 4.6 Coefficients of the Bayerer lifetime model [144]

4.6.3. Protocol for PC tests

Even though the power cycling conditions to be applied were defined in section 4.6.2, several different tests are going to be performed throughout the PC protocol. The different tests aim to track the evolution of some of the failure precursors seen on Table 1.8. Additionally, some of the tests to be performed will be employed for recalibrating the junction temperature estimation methodology.

An overview of the timeline of a power cycling test can be seen on Figure 4.63. It also depicts the moment at which the different calibration and surveillance tests will take place. The tests performed throughout the PC protocol will be described in the following lines.

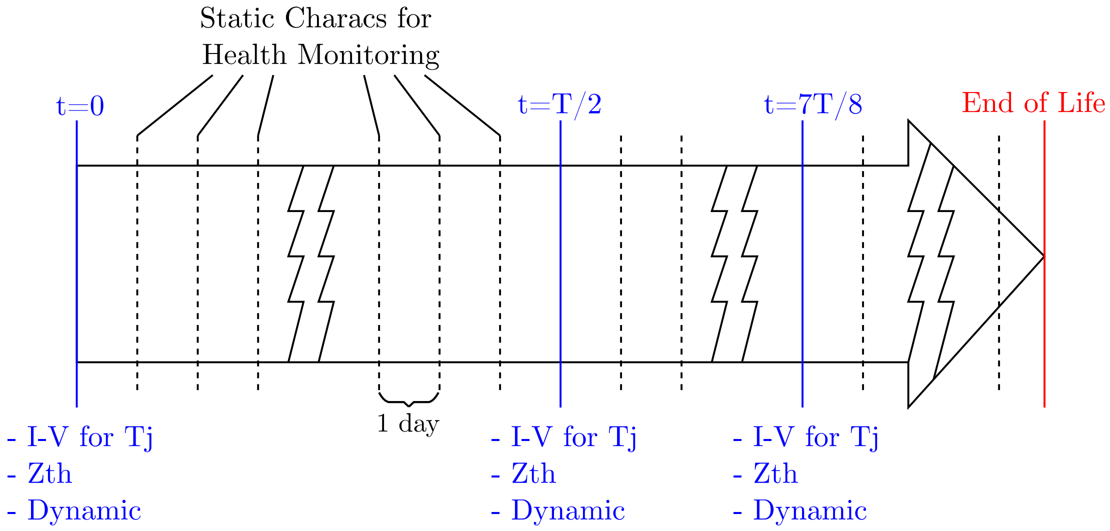


Figure 4.63. Timeline of a PC test

4.6.3.1. I-V Characterization for T_j estimation

This process was previously described in section 4.5.1. For performing this characterization, the power device analyzer B1506A from Figure 4.44 is used. The output characteristics of the IGBT device at several different temperatures are obtained as shown in Figure 4.45. The goal of this test is to obtain look-up tables for computing T_j.

This type of test is performed at three different moments of the PC test, as seen on Figure 4.63. This is done as a mean to consider the degradation of the power device and account for its effect on the estimation of the junction temperature. This test is first performed before the ageing protocol or at $t = 0$. Then, this test is repeated at $t = T/2$ or half the expected duration of the particular cycling condition. Finally, this test is performed around the expected end of life of the DUT at $t = \frac{7}{8} \cdot T$.

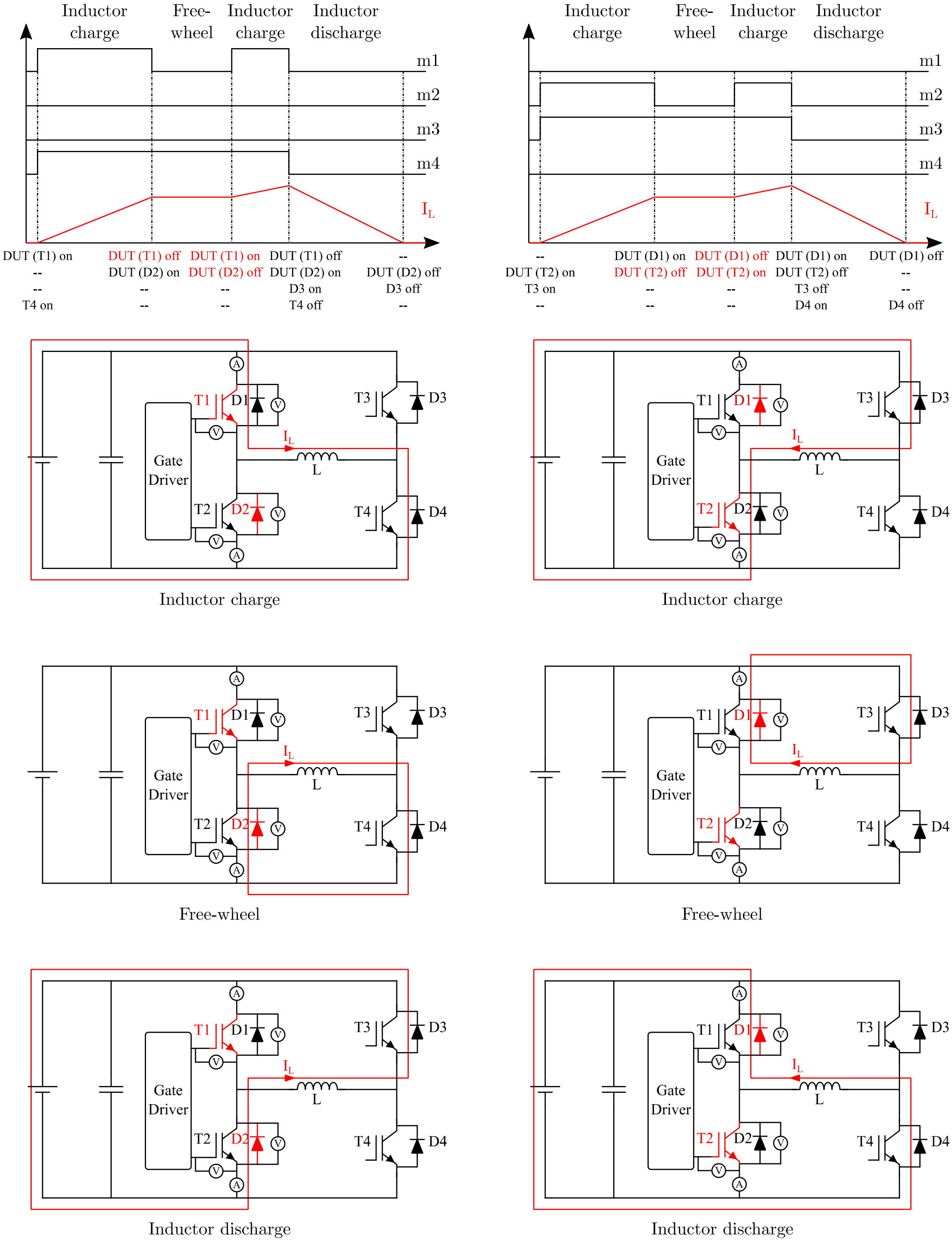
4.6.3.2. Z_{th} characterization for Health Monitoring

This test aims to track the degradation of the thermal path of the DUT. It will track the degradation of both the thermal resistance R_{th} and the thermal impedance Z_{th} of the semiconductor. This test will be performed with the help of the thermal impedance analyzer from Figure 4.50. Some of the expected Z_{th} curves can be seen on Figure 4.51.

This test will be performed at the same time intervals described for the characterization of section 4.6.3.1. Additionally, this result could be used to update the Kalman filter model for the estimation of the junction temperature. However, due to time constraints this was not carried out.

4.6.3.3. Dynamic characterization for Health Monitoring

In order to inspect the switching characteristics of semiconductors it is a common practice to perform the double pulse test [300]. This test allows to perform a turn-off switching action on the DUT, followed by a turn-on action. More details on the sequence for performing this test can be seen on Figure 4.64.



(a) (b)

Figure 4.64. Double pulse test sequence: (a) HS IGBT, (b) LS IGBT

For being able to perform this type of test it is necessary to have a large enough capacitor to provide the energy during the switching actions. In the original PC test circuit, the DC link capacitor alone cannot provide the sufficient energy. Therefore, external capacitors as the ones seen on Figure 4.65, are connected to the DC bus of the test circuit (Figure 4.66) for being able to perform the double pulse test. Some of the switching waveforms obtained with this test can be seen on Figure 4.67.

The degradation of the DUT can induce a degradation of the dynamic characteristics of the power semiconductor [301]. The main dynamic failure precursors of the IGBT devices are the turn-on and turn-off time (t_{on} and t_{off} respectively). Additionally, some other dynamic characteristics, such as the Miller plateau length can be inspected for asserting the level of degradation of the device. The dynamic characterizations will not only be useful for assessing the degradation of the devices, but also for the estimation of the junction temperature. The Kalman filter used for the estimation of T_j requires the use of the losses experienced by the semiconductors as one of its inputs. Hence, the calculation of the switching losses will use the switching energies obtained with the double pulse tests. The calculation of the switching energies was performed as indicated in [302], and the resulting switching energies can be seen in Figure 4.68.

Similar to the testing protocols of sections 4.6.3.1 and 4.6.3.2 this test can be performed at different points throughout the cycling protocol.

Figure 4.65. External capacitors for performing double pulse tests

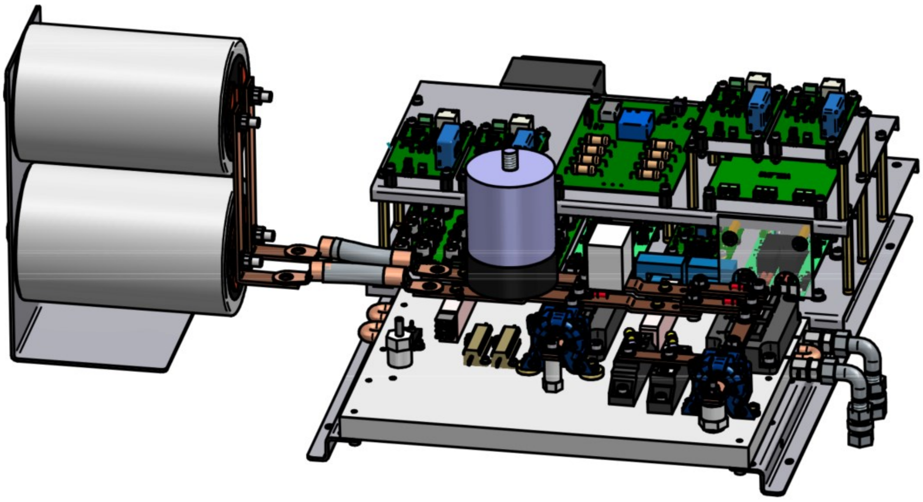


Figure 4.66. Connection of external capacitors

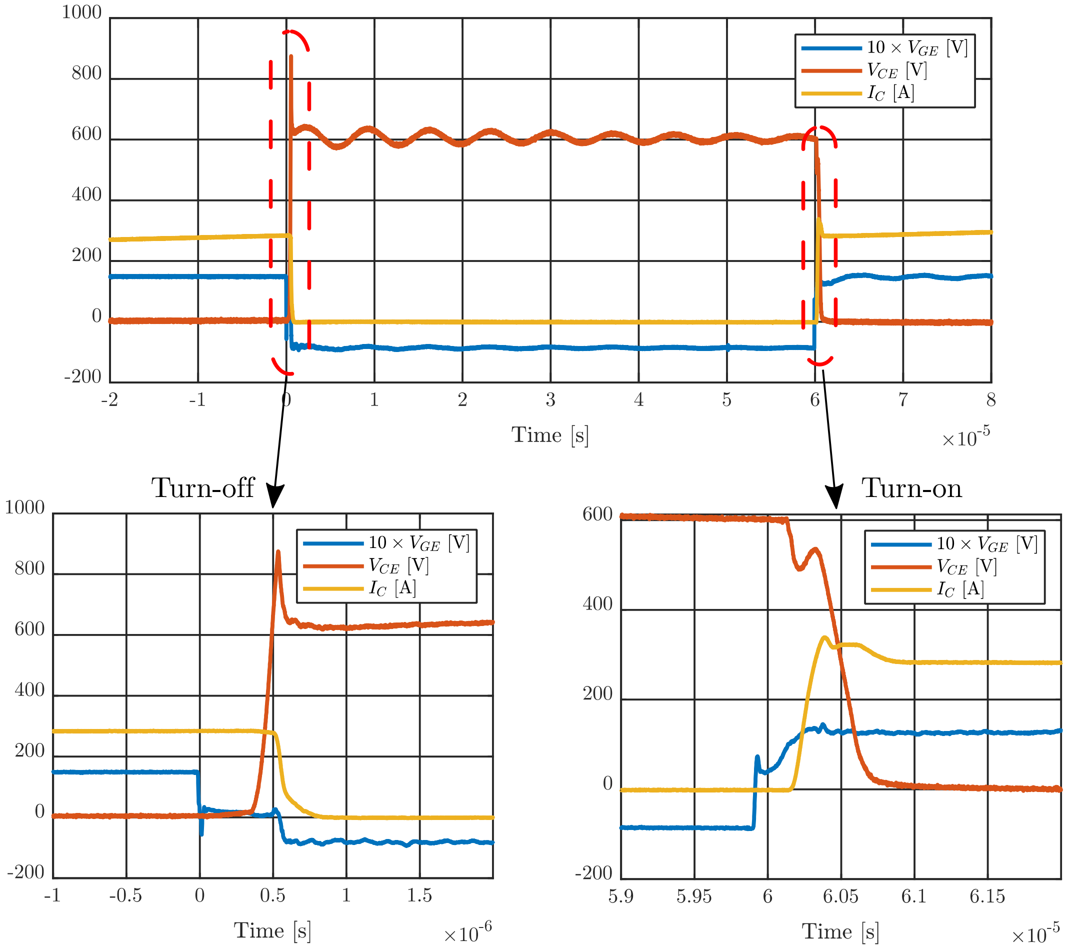


Figure 4.67. Switching waveforms at Turn-off and Turn-on

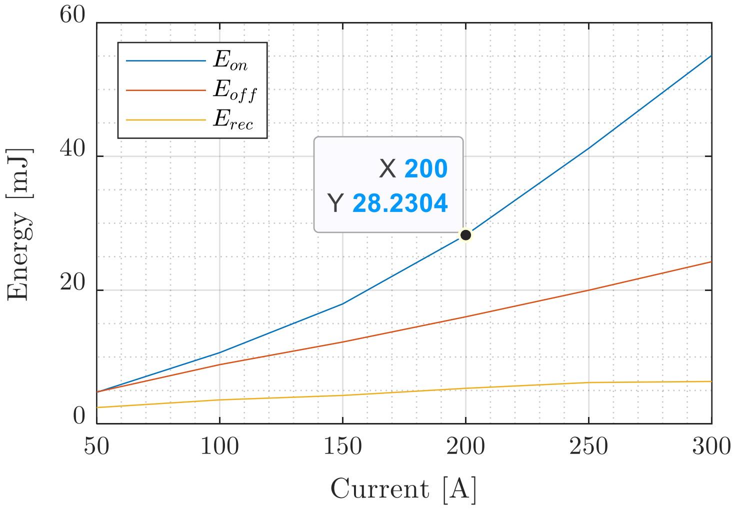


Figure 4.68. Switching energies obtained with the double pulse tests

4.6.3.4. Static characterizations for Health Monitoring

Differently from the tests performed in the previous sections, the tests for tracking the evolution of the simplified static characteristics of the device will be performed in a more periodic way. The tests performed in the previous sections are more time consuming or require the use of external equipment for being performed, hence the previous tests cannot be performed as often. The static characterizations for health monitoring will be performed every day. In the following lines the simplified static characterizations will be described.

4.6.3.4.1. I-V characterization

It is well known that the $V_{CE(sat)}$ is dependent on I_C, T_j and also on the degradation of the device ($V_{CE(sat)} = f\big(I_C, T_j, \text{degradation}\big)$). In order to assess the effect of the degradation on the $V_{CE(sat)}$ it is necessary to remove the influence of the I_C and T_j. Thus, the output characteristics of the DUT will be acquired at a very low current, and fixed reference temperature. Using a small enough current guarantees that the semiconductor device does not produce self-heating and the device remains at the fixed temperature reference. The chosen current for performing this test is 100 mA, similarly, this test will be performed at a fixed temperature reference of 15°C.

For performing this test, the temperature will be set with the help of the cold plate and the external chiller. The equipment employed for performing the current injection of the calibration current and measuring the $V_{CE(sat)}$ value is the source meter unit (SMU) Keithley 2612B seen on Figure 4.48.

4.6.3.4.2. V_{th} characterization

Another failure precursor found in the literature is the gate-emitter threshold voltage $V_{GE(th)}$ as evidenced in Table 1.8. Similar to the test described in section 4.6.3.4.1, this measurement will be performed at a fixed current and reference temperature for assessing the evolution of this quantity in regard to the ageing of the power device. The SMU Keithley 2612B from Figure 4.48, will also be employed for performing this characterization.

4.7. Measurements and test results

Up until this point, this chapter described the experimental setup and the methods employed for the monitoring of the DUT and the complete test bench. This section will present the main results obtained with the PC test bench.

4.7.1. Real-time measurements

In section 4.4.4.5 the V_{CE} board was introduced, and it was mentioned that this will be the main tool for assessing the health-state of the IGBT module. In Figure 4.43 it was seen that the V_{CE} readings obtained with the board, must be correctly interpreted in order to get valid measurements. Therefore, after considering the necessary delays for avoiding transient voltage measurements, the valid real-time V_{CE} and I_{Load} measurements obtained with the V_{CE} board can be seen in Figure 4.69.

The measurements of the on-state voltages for both IGBT devices (high-side and low-side) inside the DUT can be seen in Figure 4.69. It is obvious that the high-side IGBT will be conducting in the presence of positive currents on the load, whereas the low-side IGBT will conduct in the presence of a negative current on the load. In this regard, it is of crucial importance that the measurements of the on-state voltages and the load current are perfectly synchronized, as evidenced on Figure 4.69. The computation of the losses experienced by the semiconductors as well as the temperature estimation are dependent on these measurements and if these quantities are not synchronized, it can lead to incorrect computations of the losses and the temperature of the power devices.

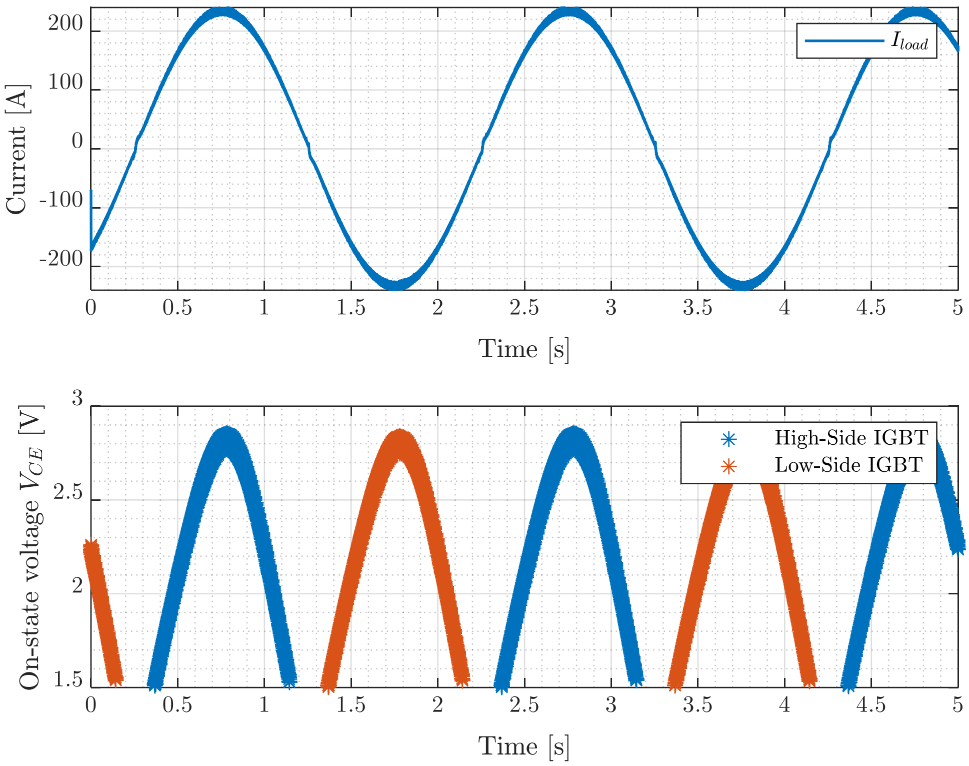
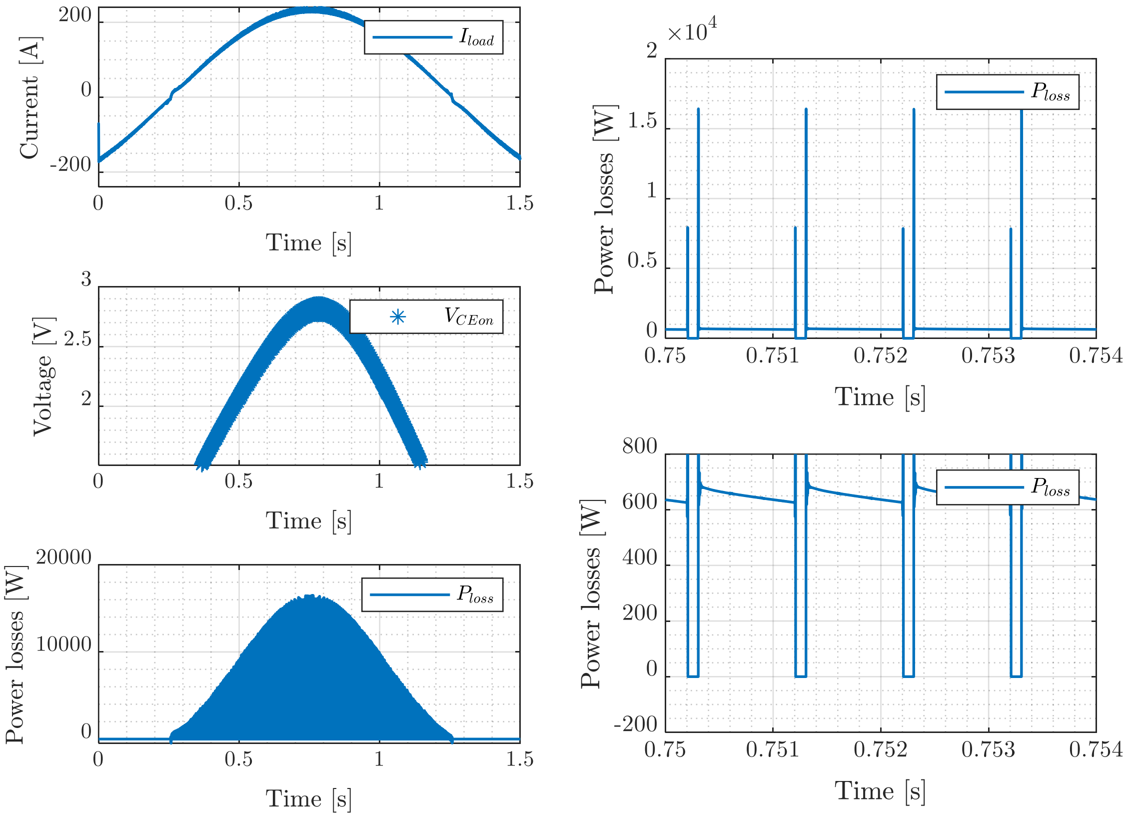


Figure 4.69. Real-time measurements performed with the V_{CE} board

From the measurements obtained with the V_{CE} board seen in Figure 4.69, it is possible to perform the calculation of the power losses on the semiconductors. On Figure 4.70 the losses experienced by the high-side IGBT can be seen. From a simple inspection of Figure 4.70 (a) it could be concluded that the computation of the losses is incorrect as values in the range of 16 kW can be appreciated. However, if inspected more carefully (Figure 4.70 (b)), it can be appreciated that there are peaks in the power loss computation that correspond to the switching losses experienced by the device. The computation of the switching losses was done by interpolating the switching energies (Figure 4.68) obtained with the double pulse test from section 4.6.3.3. Once the switching energy is obtained, it is converted to a power pulse by dividing the interpolated energy by the time that takes the switching action. This procedure was depicted on Figure 3.5. As the switching times for the DUT are in the range of a few µs, the resulting power pulses can have such large values as the ones shown in Figure 4.70. Even if the switching losses can have very large peak values, they are applied during short periods. In the experimental setup developed in this chapter, the vast majority of losses come from the conduction losses. In Figure 4.70

(b) the conduction losses can be seen more clearly on the lower section. In this example the conduction losses reach values superior to 600 W. These losses are obtained by multiplying the values of the V_{CE} and I_C present on the device.

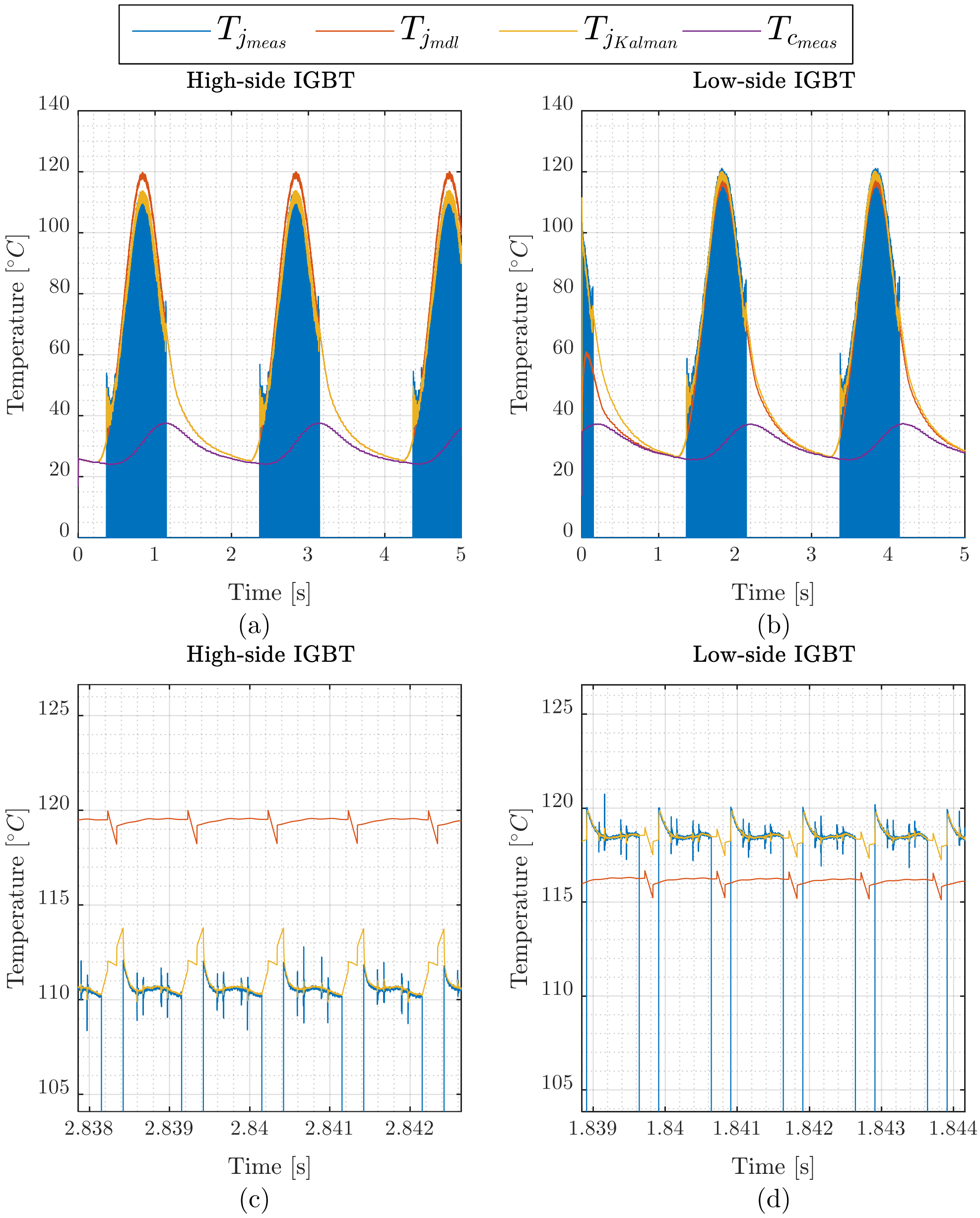


(a) (b)

Figure 4.70. (a) Computation of power losses (High-side switch), (b) Zoom on power losses

4.7.2. Junction temperature estimation

A large portion of this chapter deals with the hardware and the methodology for the estimation of the junction temperature of the IGBT devices. Finally, these estimations can be seen on Figure 4.71, in which the junction temperatures for the high-side and low-side IGBTs can be distinguished. Different temperatures can be seen in Figure 4.71, such as the temperature at the interface of the heatsink and the baseplate of the device ($T_{c_{meas}}$), but more importantly, the junction temperature issued from the preliminary estimation ($T_{j_{meas}}$), from the thermal model used for the synthesis of the Kalman filter ($T_{j_{mdl}}$) and the output of the Kalman filter ($T_{j_{Kalman}}$).



(a) (b) (c) (d)

Figure 4.71. Estimation of junction temperature T_j

The Kalman gains computed for the estimation of T_j of the semiconductor devices are:

$$K_{f,HS} = \begin{bmatrix} 1.94 \times 10^{-7} \\ 0.2425 \\ 7.66 \times 10^{-6} \\ 4.50 \times 10^{-16} \end{bmatrix}, K_{f,LS} = \begin{bmatrix} -6.12 \times 10^{-20} \\ 1.04 \times 10^{-322} \\ -2.45 \times 10^{-12} \\ 0.2401 \end{bmatrix}$$

These gains indicate that the Kalman output will follow more closely the model employed for the synthesis of the filter, as explained in section 4.5.3.3.2. It is worth noting that the Kalman gains were obtained with the covariance matrices computed with the ALS method. The covariance matrices that were used for the computations of K_f are:

$$Q_{HS} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0.0064 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}, R_{HS} = [0.0811];\ Q_{LS} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0.0081 \end{bmatrix}, R_{LS} = [0.1065]$$

The covariance matrices also help understand why the computed Kalman gains are so small. It can be seen that the coefficients for the measurement noise R are at least one order of magnitude more important than the non-null coefficient of the process covariance matrix Q. Therefore, the model is more reliable than the measurement in this application.

It is worth noting that a Foster representation was chosen for modeling the Kalman filter. Hence, there is not a physical interpretation of the layers composing the thermal network. In this case, the ALS method assigns all the variance to one of the layers of the model. This interpretation will also lead to satisfactory estimates as the junction temperature from the Foster model is obtained as the sum of all the temperatures of its composing layers as expressed on matrix C from the state representation seen in Eq. (4.10).

It was not possible to determine the layer to which the variance is attributed. A look on the continuous state matrices of both switches is necessary:

$$A_{HS} = 1\text{e}-3 \begin{bmatrix} -0.0099 & 0 & 0 & 0 \\ 0 & -1.9450 & 0 & 0 \\ 0 & 0 & -0.0025 & 0 \\ 0 & 0 & 0 & -0.0497 \end{bmatrix},$$

$$A_{LS} = 1\text{e}-3 \begin{bmatrix} -0.0475 & 0 & 0 & 0 \\ 0 & -1.7485 & 0 & 0 \\ 0 & 0 & -0.0125 & 0 \\ 0 & 0 & 0 & -0.0041 \end{bmatrix}$$

In the case of the HS switch the variance is attributed to the second layer which according to its state matrix has the smallest time constant. On the other hand, for the LS switch the variance is attributed to the fourth layer which has the biggest time constant.

In Figure 4.71 (c) and Figure 4.71 (d) it can be seen that when the measure is available the Kalman output will approach the measured values as the Kalman gains are not 0 for one of its layers. Some interesting phenomena can be distinguished in Figure 4.71. It can be seen that the junction temperature of the high-side switch is smaller than that of the low-side IGBT. At first glance, this result seems incorrect as the devices are subjected to the same current and should dissipate almost the same losses. However, the upper IGBT is closely located to the water inlet of the heatsink, which means that this device will be cooled more efficiently than the other semiconductor. A difference of almost 8°C between both devices can be evidenced due to this characteristic.

4.7.3. Degradation assessment

Having verified the measurements that can be performed with the hardware developed for the experimental setup, it is important to track the degradation of the DUT. In order to do so, the evolution of the on-state voltage V_{CE} is a standard practice. In many research works [108], [271], this measurement is performed with the use of a calibrated current sources in the range of milliamps in order to have accurate results. Thus, it is a common practice to interrupt the cycling protocol for carrying out this measurement.

The V_{CE} board delivers accurate measurements and since it provides synchronized measures of V_{CE} and I_C, it was chosen to perform a quasi-online degradation assessment. The cycling protocol does not need to be stopped in order for this analysis to be carried out. The Speedgoat supervisor periodically streams the measurements obtained with the V_{CE} board. It streams measurements performed during 10 s of converter operation and the data is sampled at 1.25 µs. This data is sent to an external computer and the junction temperature is estimated offline. Then, it was chosen to track the evolution at a fixed current and fixed junction temperature, as a mean for having the same frame of reference for all the streamed data. An example of a streamed dataset for tracking V_{CE} can be seen in Figure 4.72.

It was chosen to perform the measurements of V_{CE} at different current and temperature pairs. A measurement was taken at a current value below the cross-over point (10 A), another measurement at a current superior to the cross-over current (180 A) and finally a measurement at the cross-over current (specific to each device). The values of the T_j for the acquisitions were chosen by inspection of the estimated temperature at the chosen currents with a tolerance of some degrees.

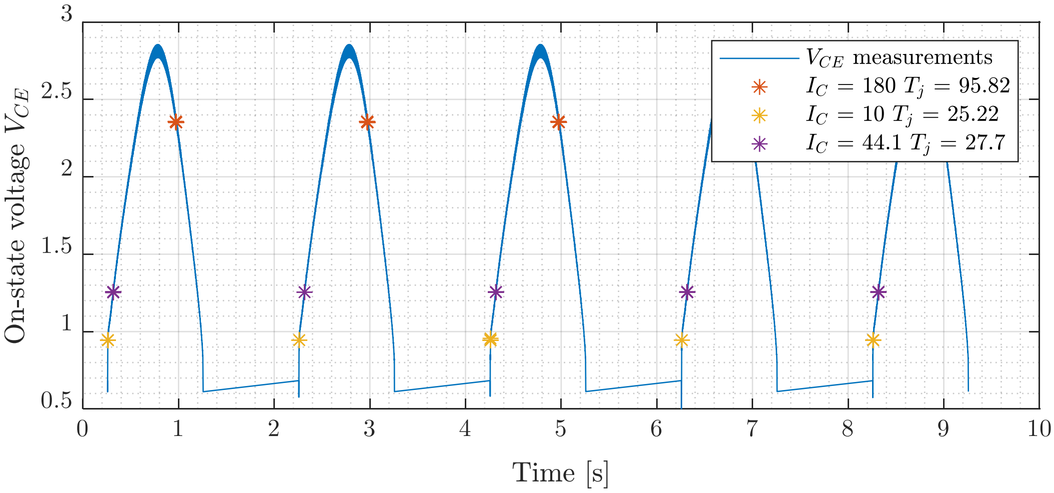
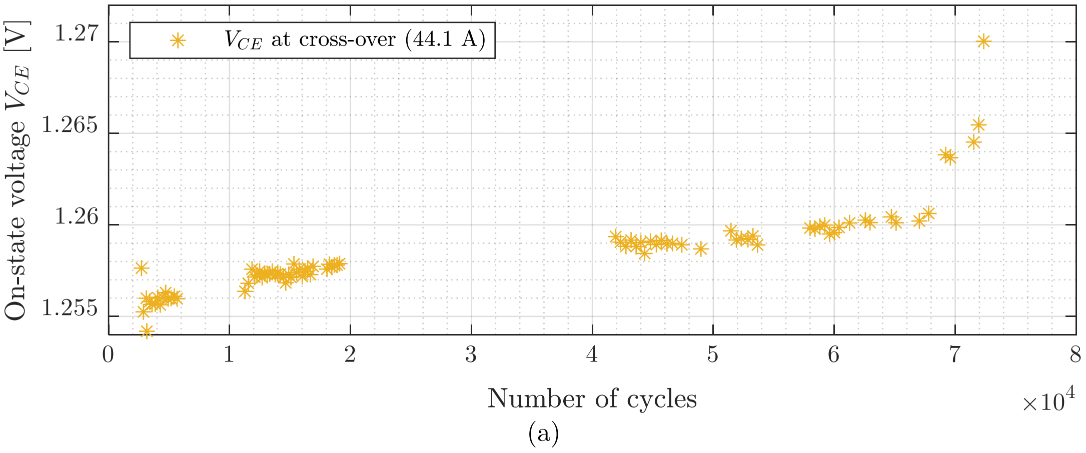
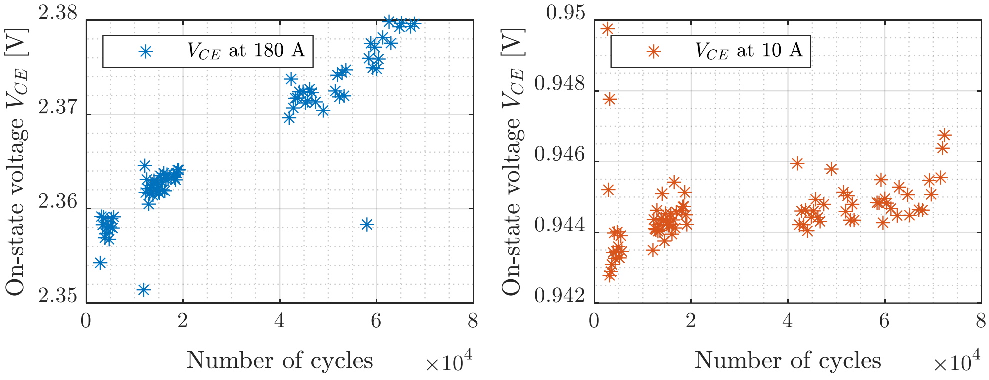


Figure 4.72. V_{CE} measurements at different (I_C, T_j) pairs

The acquisitions are taken at different stages of the cycling protocol, and the V_{CE} measurements are evaluated for tracking the degradation on the IGBT devices. The results concerning one DUT can be seen on Figure 4.73.



(a)



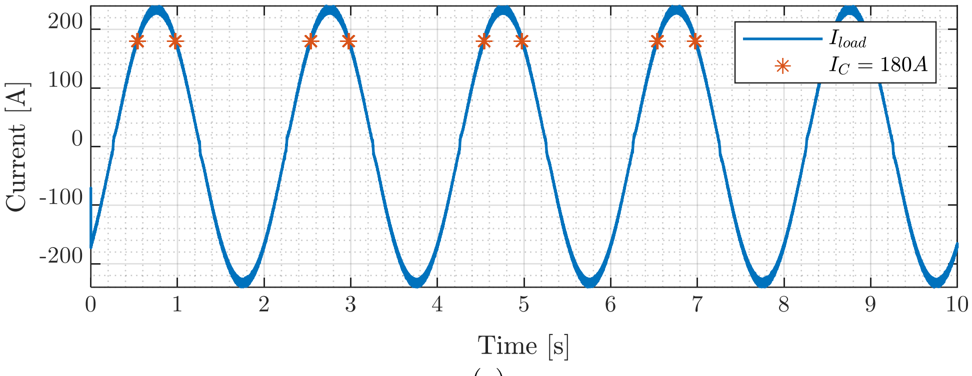
(b) (c)

Figure 4.73. Evolution of on-state voltage

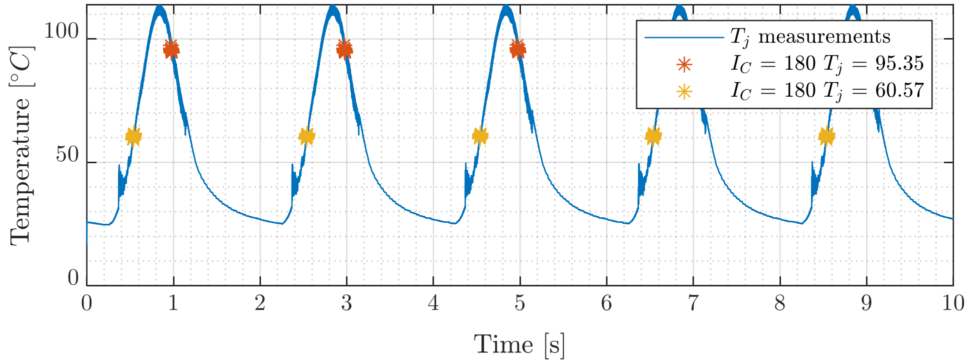
It is important to highlight that there were issues with the streaming of the data somewhere around 20k cycles into the ageing protocol, but they were solved as evidenced on Figure 4.73. Due to time considerations the assessment of the degradation was still carried out. The results are satisfactory even with a lack of acquisitions between 20k and 40k cycles. A slight increase on V_{CE} can be distinguished at the all the chosen I_C and T_j pairs.

A more detailed analysis can be performed by inspection of Figure 4.73 (a). A noticeable increase of V_{CE} can be identified after 67808 cycles. After this cycle, the increase in V_{CE} is more accelerated until another sudden increase happens after 71946 cycles. The last streaming for this DUT happened at 72361 cycles. At which the final value of V_{CE} is 1.27003 V, which represents an increase of 1.18% of its initial value. The last registered cycle before the detection of a fault on the testbench assigned to the DUT happened at 76081 cycles. Unfortunately, there is no data stream at this stage, so it is possible that subsequent jumps in the V_{CE} readings might have happened after the last acquisition.

Additionally, other ageing indicators were chosen such as the junction temperature at a fixed collector current measurement. This value was chosen arbitrarily to 180 A, however this indicator can be tracked at any I_C value. An example of this indicator can be seen on Figure 4.74. It can be noticed on Figure 4.74 (b) that for the chosen current, two possible T_j values can be retained. The first at a lower temperature happens during the current rise, while the second at a higher temperature happens at the current fall.



(a)



(b)

Figure 4.74. T_j measurements at fixed I_C

The T_j readings at current rise and current fall were retained and used as an ageing indicator as depicted on Figure 4.75.

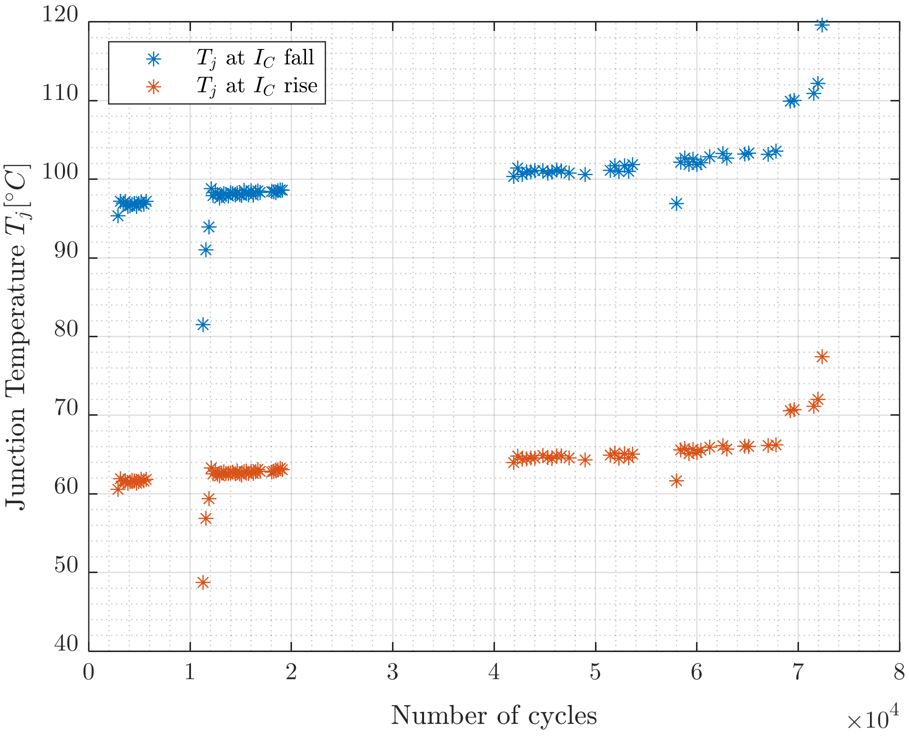
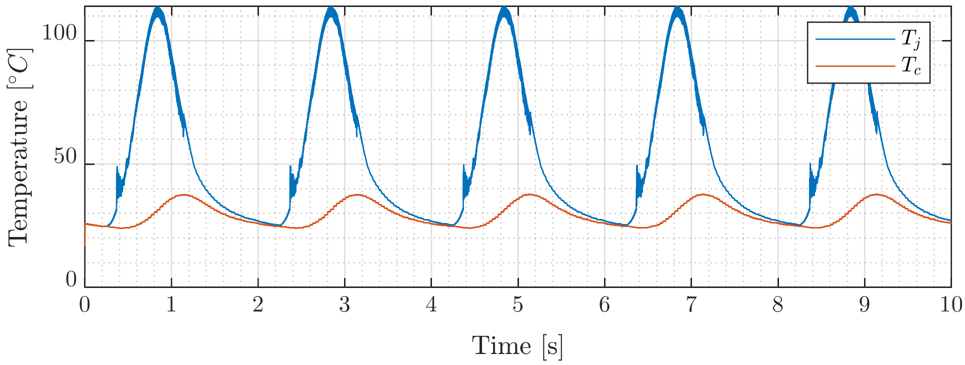


Figure 4.75. Evolution of T_j measurements

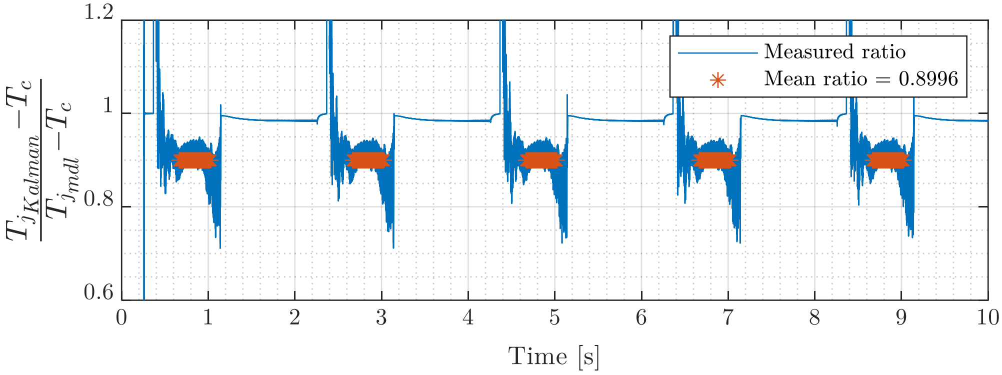
It can be seen on Figure 4.75 that this indicator gives more accurate insights than V_{CE} for the assessment of the degradation of the device. Again, a slight increase in the registered temperatures can be seen for most of the cycling protocol, until a sudden increase happens after 67808 cycles as seen previously on Figure 4.73 (a). In the case of T_j at current fall it can be noticed that the final registered temperature is 119.6°C and its initial value was 95.3°C. Which means that the temperature increase throughout the cycling tests was of 24.3°C. It is worth noting that the water temperature was fixed during the test. In the case of T_j at current rise, the initial registered value was 60.6°C, its final value 77.4°C giving an increase of 16.8°C.

The final ageing indicator chosen for the assessment of the degradation of the DUT is the ratio between the $\Delta T_{Kalman}/\Delta T_{mdl}$. The temperature variation ΔT is the difference of the junction temperature and the temperature of the baseplate. This quantity is proportional to the thermal resistance R_{th} of the module, thus is an appropriate indicator of the degradation of the device. This indicator was chosen as it compares the temperature variation obtained with a model at the start of the ageing protocol against a variation influenced by the measurements that are considered in the Kalman algorithm.

An example of the measurement of this ratio is shown in Figure 4.76. For a better illustration of this indicator the T_j issued from the Kalman filter and the T_c are depicted in Figure 4.76 (a). This ratio only makes sense when there is an available measurement of the junction temperature. It was seen that the measurements are only considered when the current is above a defined threshold and is represented by a binary variable a in Eq. (4.28).



(a)



(b)

Figure 4.76. Measurement of ratio $\Delta T_{Kalman}/\Delta T_{mdl}$

It was also verified when computing this indicator, that its value is subjected to big transients around the moments where the measurement is enabled/disabled. Thus, an additional current threshold was used for computing this parameter. Once the new threshold is reached the mean ratio of $\Delta T_{Kalman}/\Delta T_{mdl}$ is computed for the streamed data, as seen on Figure 4.76 (b).

Consequently, the evolution of this ratio was computed for all the streamed files and the resulting curve can be seen on Figure 4.77. As this value is proportional to R_{th} the variation of this indicator proves that there is a degradation of the internal layers present in the semiconductor. The initial value registered for this parameter is 0.9 and its final value 1.12, which represents an increase of 24%. This value is congruent with the end-of-life criteria seen on Table 1.8.

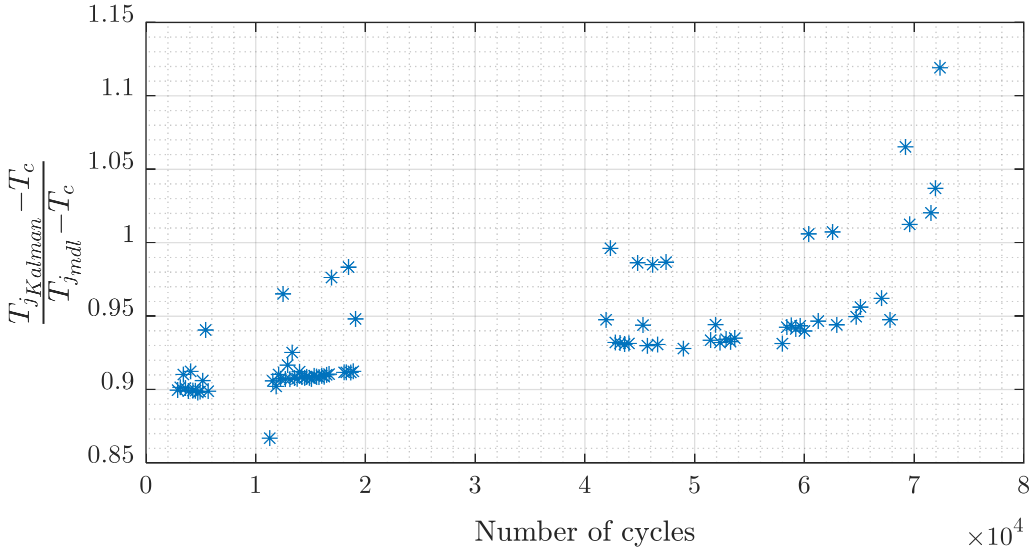


Figure 4.77. Evolution of ratio $\Delta T_{Kalman}/\Delta T_{mdl}$

4.7.4. Discussion on the power cycling experiments

It is worth reminding that the results depicted in section 4.7.3 were supposed to represent condition 2 of the ageing protocols presented in Table 4.5. However, the actual cycling condition imposed has the parameters depicted in Table 4.7. Those parameters can be verified from Figure 4.71.

Condition	ΔT_j [°C]	$T_{j_{min}}$ [°C]	t_{on} [s]	**Estimated Cycles to failure N_f**	**Estimated Days to failure**
New	87	25	0.6	414573	5.8

Table 4.7 Cycling conditions applied in real protocol

In Table 4.7 the estimated number of cycles to failure for the condition imposed is 414573 cycles, whereas the real number of cycles to failure of the DUT is 76081 cycles. There is quite a substantial difference between the estimated value and the real one. This difference can be attributed to the fact that the estimation was carried out using the default coefficients of the Bayerer lifetime model presented in Table 4.6. It is therefore necessary to perform a statistical analysis for correcting the coefficients of the model to describe the lifetime of the DUT. Due to time constraints this analysis was not carried out in this thesis. Also, additional cycling conditions need to be put to test for validating the new coefficients of the lifetime model.

It is also important to perform a post-mortem analysis to better interpret the results and detect the failure mechanisms activated through the cycling tests. The only type of post-mortem analysis performed in this work consists of the visual inspection of the DUT. Even if a visual inspection seems a rather simple verification, in this case it demanded a great effort. The cycled DUT was opened by machining the external plastic case. Then, the insulating gel was removed in two stages, the first by hand, and the second with the help of an industrial silicon remover product. This was necessary as the gel wouldn't allow for a visual verification of the state of the semiconductors.

The studied module without the external casing and without the insulating gel can be seen on Figure 4.78. Moreover, Figure 4.78 depicts one of the root causes of the failure of the device wire bond lift-off. It was verified that 3 out of 4 emitter bond wires were completely detached from the metallization pads on one of the two chips that make the high-side switch of the DUT. Unfortunately, this type of inspection cannot lead to a complete understanding of the failure mechanisms experienced by the IGBT. More advanced techniques, such as electronic microscopy, need to be employed for performing a proper post-mortem analysis.

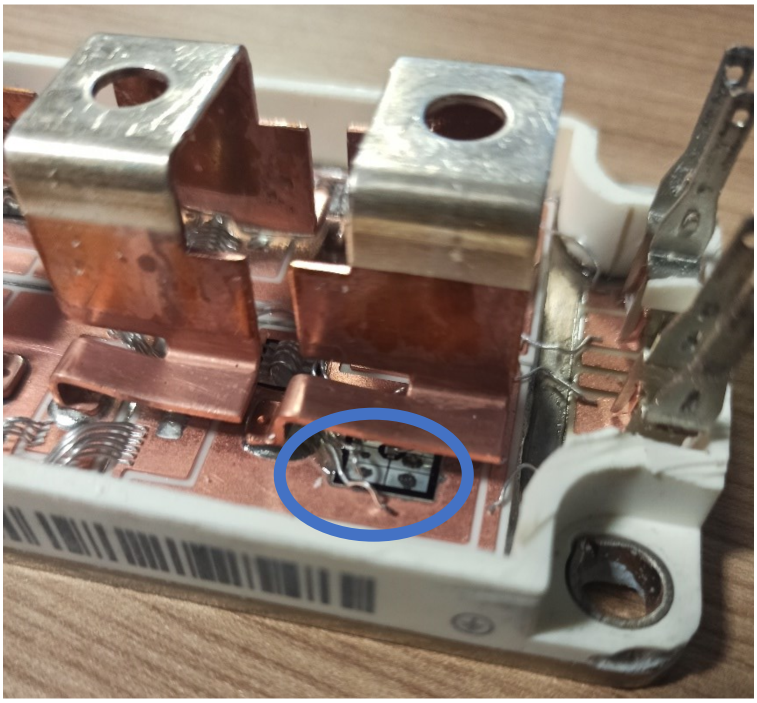


Figure 4.78. Wire bond lift-off on the DUT

4.8. Chapter conclusion

This chapter dealt with the power cycling test, from its development stage until the obtention of cycling results for a single DUT.

On the first section a review on the existing cycling methods and topologies was presented. This review led to the choice of an AC power cycling topology for the experimental setup developed in this thesis.

Subsequently, the test setup was presented with all of its composing elements. Insights were given on the software developed for the operation of the test bench, but a more detailed description of the hardware was done. Besides the elements composing the power circuit of the ageing setup, a great effort was put into the development of electronic boards. Among the electronic boards developed, a particular attention was given to the V_{CE} board, as this board will be instrumental in the assessment of the degradation of the power semiconductors.

It was seen that the upgraded V_{CE} measurement circuit can perform accurate measurements but is also capable of added functionalities when compared to existing boards dedicated to this purpose. The V_{CE} board can be used with fast switching devices, and it can also provide bipolar outputs for measuring the V_F of antiparallel diodes.

A great portion of this chapter was dedicated to the estimation of the junction temperature of the DUT. It was seen that the V_{CE} board played a major role in this task, since it delivers synchronized readings of the on-state voltages and the collector currents. However, the preliminary T_j estimation by use of the output characteristics of the IGBT was proven insufficient for a correct estimation of the junction temperature. This is attributed to the fact that for currents near the cross-over point the preliminary estimations yield poor results. Therefore, an additional technique was proposed for giving a more accurate junction temperature estimation.

The chosen technique for improving the junction temperature estimation is a Kalman filter. This tool is very well known and its performance on this type of application was already proved in previous research works. This technique combines the temperature measurements obtained with the preliminary T_j estimation and a thermal model that was parametrized by using accurate characterization inputs.

A novelty introduced for improving the performance of the Kalman filter was the use of the autocovariance least-squares method. This method was employed for determining the noise covariance matrices Q and R that will have a direct impact on the performance of the filter as they are used for the computation of the Kalman gain K_f.

The T_j estimations where afterwards validated with the help of a fiber optic measurement equipment.

All the background for performing a statistical analysis of the degradation/lifetime of the DUT was discussed. It was seen that the sample size for assuring low levels of uncertainty must be of 6 elements per condition to be tested. Different cycling conditions were proposed for addressing the main stressors involved in the lifetime models of semiconductors (ΔT_j, $T_{j_{ref}}$ and t_{on}). Due to time considerations, the statistical analysis was not performed and only a cycling condition was evaluated.

Then, the cycling protocol was discussed. This protocol involves several characterizations throughout the power cycling test, some of them are required for the computation of the junction temperature and other ones are used for evaluating the state of degradation of the power device. Again, due to time considerations only the characterizations at the start of the cycling tests were carried out. This were mainly used for the estimation of T_j. The characterizations for addressing the degradation were not performed, as they would require stopping the converter and time constraints pushed to finish the cycling test in a short amount of time.

In the last section of this chapter the main results of the V_{CE} measurements and T_j estimations are shown. The accuracy of the V_{CE} was proven as the measurements seem to give realistic values for T_j. It was demonstrated that the Kalman filter has a satisfactory performance as it reduces the noise in the measurements. It was also seen that the Kalman output relies more on the model, but it approaches the measurement when it is available.

Afterwards three indicators were chosen for tracking the state-of-health of the semiconductors. These indicators are:

- V_{CE} at fixed I_C and T_j (above, below and at cross-over point)
- T_j at fixed I_C (at current rise an at current fall)
- Ratio $\Delta T_{Kalman}/\Delta T_{mdl}$ (proportional to R_{th})

The assessment of the degradation was performed in a quasi-online manner as it was not necessary to interrupt the cycling tests, but the computations were carried out offline. Due to time considerations, only one module was subjected to the cycling protocol.

Also, a visual inspection of the cycled module was performed. In this analysis it was verified that the bond wires of the high-side switch of the device were damaged. They were detached from the emitter pads.

Finally, it can be said that the experimental setup developed in this work was able to perform its intended goal, which was to apply harsh thermal conditions to power semiconductors. The main stressor in power cycling tests is the ΔT_j excursion experienced by the power devices. Hence, a big challenge was to be able to generate large variations in a short amount of time. This goal was achieved, as verified on the cycling curves concerning T_j estimation. Moreover, the test bench successfully allowed for a module to experience a fault due to degradation of its internal structure by means of power cycling.

Conclusions and Perspectives

Conclusions

HVDC systems have very demanding reliability and availability requirements, since electrical outages can have severe economical and societal consequences. The MMC, being a pivotal technology for the development of HVDC systems, needs to be the subject of strategies for having its availability improved. Therefore, condition monitoring was identified as a potential methodology to enhance the performance of this type of converter. In this work, the focus was made on the IGBT modules present in the HB-SMs.

In Chapter 1 an introduction to the IGBT module technology for HVDC applications was presented. Even though, the more modern Press-pack IGBTs are quickly imposing themselves in HVDC applications, the more mature flat-pack technology is still relevant and present in HVDC-MMCs. Hence, this work focuses on wire bonded IGBT modules. Subsequently in Chapter 1, a literature review was made on the failure mechanisms affecting wire bonded IGBT modules. From the literature review, it was concluded that packaging related issues are more relevant in IGBT modules and that they are activated mainly through wear-out processes. Since packaging-related failure mechanisms are caused by wear-out processes, the failure precursors indicative of this type of failures can be tracked for assessing the state-of-health of the component. It was also seen from the literature review on failure mechanisms, that thermal loading is the major cause of the packaging-related failures.

Also in Chapter 1, an extensive state-of-the-art on the prognosis and CM techniques for IGBT modules was presented. It was seen that the PoF approaches for IGBT prognosis use the thermal loading as the input for lifetime models. It was also seen that other approaches based on historic data can be employed for the prognosis of the RUL of IGBT devices. Concerning CM, it was seen that there are already several works that addressed the weakest parts of IGBT power modules: the bond wires and the solder layers.

In Chapter 2, a hybrid model of the MMC was presented. This model allows for the obtention of the electrical waveforms of a single HB-SM, which were later employed in the lifetime estimation methodology. In Chapter 2 a comprehensive mathematical background for the averaged-detailed model was given. Additionally, an insight into the control strategies required for assuring the operation of the converter was given in Chapter 2.

In Chapter 3, the electrical outputs of the averaged-detailed model from Chapter 2 were used as the first step for performing the lifetime estimation of the semiconductors present in a HB-SM. The electrical waveforms were first translated to power losses experienced by the semiconductors. Then, thermal models allowed for the computation of the resulting thermal profile of each power device. A major output of the research on the lifetime estimation of IGBT devices was a model-based extrapolation technique which is based on the Norris-Landzberg model for the extrapolation of data inside the lifetime models provided by semiconductor manufacturers. The rainflow counting algorithm along with the Miner's cumulative damage model was finally used for obtaining the lifetime consumption of the semiconductors.

Also, Chapter 3 dealt with the reliability prediction of a HB-SM. It was seen that this computation can be made employing the reliability distribution of the composing elements of a SM. Moreover, the lifetime estimation for the semiconductors can be simply translated to a Weibull reliability distribution, which allows to consider the mission profile in the reliability predictions. Finally, Chapter 3 presented a methodology for performing redundancy computations. It uses the reliability predictions of the HB-SM along with a Markov Chain that considers the updated probability of survival of the SMs, while considering the previous maintenance interventions. Then, Monte Carlo simulations allow to test different redundancy levels for achieving a target availability.

Chapter 4 dealt in its first sections with the review of power cycling protocols and testbenches. This type of experimental setup is required for assessing the reliability of IGBT devices by subjecting them to stresses that resemble those experienced in real applications. From the review on PC topologies, the AC power cycling was retained as it applies more realistic stresses to the IGBT devices, due to the presence of switching losses. Subsequently in Chapter 4 a detailed insight on the design of an ageing testbench was given. First, the DUT devices were presented and the basic hardware for performing the cycling protocols. Also, the control strategy for the testbench was discussed. The chosen strategy allows for large temperature excursions that allow for obtaining power cycling results in a reasonable amount of time.

A great part of Chapter 4 dealt with the instrumentation required for the functioning of the testbench. Several electronic boards were developed for this goal. Since the CM scheme employed in this thesis reposes on the monitoring of the collector-emitter on-state voltage $V_{CE(on)}$, a particular circuit was proposed in this work. The circuit can be considered as an upgrade of similar circuits used for the same purpose, as it allows for full-range bipolar measurements and fast enough operation in order to be compatible with wide-band gap devices. The V_{CE} measurement circuit was deployed in an electronic board that allows for the real time measurement of both high-side and low-side devices along with the load current in a synchronized manner.

With the online measurements of the V_{CE} board, a crucial topic was confronted: the estimation of the junction temperature T_j of the IGBT components. The method for the estimation of T_j it is based on the use of a preliminary estimation using only the measurement of the pair I_C and $V_{CE(on)}$, which can be obtained with the V_{CE} board. For improving the estimation, a Kalman filter was developed.

The model employed in the Kalman filter, along with its residues allows to track any drift in the parameters of the semiconductor thermal network, which is also indicative of the degradation of the IGBT device. Moreover, in order to improve the performance of the Kalman filter the autocovariance least-square methods was used for computing the covariance matrices used with the Kalman filter.

Finally, Chapter 4 gives the results of the power cycling tests, along with the results of the real-time estimation of the temperature of the semiconductor devices. The evolution of the $V_{CE(on)}$ of the cycled modules can be seen. Additionally, some other ageing indicators were presented. These results can be applied for giving a prediction of the remaining useful life of the components.

Perspectives

It is worth reminding that the main goal of this research work was to assess the state of health of IGBT devices for a HB-SM in a HVDC-MMC application. The experimental setup developed in Chapter 4 was conceived in order to carry out tests that will help validate lifetime models and develop more advanced algorithms for predicting the RUL of the devices in this type of application.

Due to time constraints the experimental results were used only to verify the drift in parameters due to degradation and validate the concept of the power cycling test with all its hardware and methodologies for a practical assessment of the reliability of IGBTs. Therefore, subsequent studies must be made for using the experimental setup to validate the results obtained with the lifetime estimation methodology developed in Chapter 3 and assess the reliability of IGBTs in the context of a HVDC-MMC.

Due to the discrepancies concerning the evolution of the $V_{CE(on)}$ with the degradation of the module [110], [111], [115], [120], it was concluded that basing a CM strategy solely on the measurement of this parameter can yield unsatisfactory results when different failure mechanisms compete against each other [51]. It will therefore be necessary, to develop measurement circuits of other failure precursors (Table 1.8), such as the one shown in Figure 1.20. This will allow to have a richer database and will allow to develop data-based techniques for identifying the current state-of-health and predict the end-of-life of the studied devices.

A possible approach for a prognosis methodology could combine the information from the thermal profile using an online rainflow counting algorithm [303], along with information from the drift of DSEPs to have a better estimation of the RUL of the IGBTs. The online rainflow counting algorithm is a PoF method, whereas the extrapolation of the drift in DSEPs could be obtained using data-based techniques such as fuzzy logic or artificial neural networks.

Concerning the cycling protocols, the characterizations for health monitoring were not performed due to time constraints. However, these characterizations will be made for further ageing tests. Moreover, the execution of these characterizations needs to be automized and the sequences need to be coded and interfaced with the supervision Speedgoat machine.

The experimental setup developed in this thesis will be a valuable asset for performing reliability studies of semiconductor devices. In future works, the degradation of the diodes can be addressed with the use of the AC PC test circuit. Additionally, the setup can be used for testing different semiconductor technologies (wide-band devices). The model-based extrapolation technique developed in section 3.2.3.1.1 can also be put to test with the help of the experimental setup.

An important tool for reliability of semiconductors are lifetime models. The lifetime models proposed in the literature can be tested with the help of the ageing test bench, and they can be adapted for a particular type of semiconductor to be tested. Additionally, the power cycling circuit can be fundamental for verifying if the lifetime models developed using DC power cycling are still valid in the context of AC power cycling.

Additionally, the cycling test bench can be useful for determining the pertinence of the use of the Miners rule that considers linear damage accumulation for the estimation of lifetime consumption.

As it was mentioned on Chapter 4, a complete post-mortem analysis will also be helpful for determining the failure mechanisms activated when performing the power cycling tests.

Concerning the redundancy computations developed in Chapter 3, the analysis of the total number of SMs employed allows for evaluating different type of maintenance strategies. It is a standard practice to replace only the failed SMs. However, replacing additional SMs might have a positive impact in the long term. Thus, new maintenance strategies can be tested with the redundancy computation methodology developed in this thesis, along with economic considerations for evaluating the optimal predictive maintenance approach.

The strategies developed in Chapter 3 can be used in other type of contexts such as MMC in MVDC applications or to different topologies. As the reliability predictions are based on the thermal loading of the devices, the only requirement for using the methodologies from chapter 3 on other applications is to use a valid mission profile and obtain the corresponding temperature profiles on the semiconductors. Moreover, the use of the mission profile can be used for obtaining reliability predictions on the capacitor present in the HB-SM and produce more accurate reliability predictions for the MMC.

Another subject that could be further investigated is the use of adaptive control strategies for prolonging the life of the semiconductors in the MMC application. This could be done by developing new balancing control algorithms that consider the state-of-health of the SM.

Finally, this thesis addressed the effects of thermal stresses to the state of health of the semiconductors. In recent years there has been an interest in performing multidimensional stress analysis. This type of analysis aims to study the impact of different stressors on the lifetime of semiconductor devices. In order to carry out this type of analysis one type of stressor should be addressed at a time, in order to fully understand its effect. Consequently, the effect of simultaneously applying different stressors should be addressed to fully understand how they can interact between each other. As this thesis dealt with thermal stress, future studies should consider the effects of other types of stress, such as the ones induced by the presence of humidity.

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Appendices

A.1. Derivation of the reduced average model

To obtain the reduced average model of a single arm, the energy stored in one HB-SM is considered:

$$W_{C_{SM}} = \frac{1}{2} C_{SM} v_{C_{SM}}^{2} \tag{A.1}$$

Where C_{SM} is the SM capacitance and $v_{C_{SM}}$ is the capacitor voltage. Hence the total energy stored in an arm composed by N_{SM} HB-SMs is the sum of all SM energies:

$$W_{C_\Sigma} = \sum_{i=1}^{N_{SM}} \frac{1}{2} C_{SM_i} v_{C_{SM_i}}^{2} \tag{A.2}$$

If all the SMs are identical, i.e. all capacitors have the same value C_{SM} and assuming a proper balancing of the capacitor voltages. Also, it must be considered that all SM voltages $v_{C_{SM}}$ are similar, then Eq. (A.2) becomes:

$$W_{C_\Sigma} = N_{SM} \times \frac{1}{2} C_{SM} {v_{C_{SM}}}^{2} \tag{A.3}$$

Additionally, the sum of all the voltages of the capacitors in an arm is:

$$v_{C_\Sigma} = \sum_{i=1}^{N_{SM}} v_{C_{SM_i}} \tag{A.4}$$

Again, if the capacitors are correctly balanced, the sum of all SM voltages yields:

$$v_{C_\Sigma} = N_{SM} v_{C_{SM}} \tag{A.5}$$

Then, Eq. (A.3) can be expressed differently by using Eq. (A.5):

$$W_{C_\Sigma} = \frac{1}{2} C_{SM} \frac{1}{N_{SM}} {v_{C_\Sigma}}^{2} \tag{A.6}$$

This equation can be interpreted as the equivalent energy stored in one equivalent capacitor Ceq with a total voltage of v_{C_Σ}. The value of the equivalent capacitor is:

$$Ceq = \frac{C_{SM}}{N_{SM}} \tag{A.7}$$

Equally, the current through the equivalent capacitor can be expressed as:

$$i_{Ceq} = Ceq \frac{d}{dt} v_{C_\Sigma} \tag{A.8}$$

Replacing Eq. (A.4) and Eq. (A.7) in Eq. (A.8) yields:

$$i_{Ceq} = \frac{C_{SM}}{N_{SM}} \sum_{i=1}^{N_{SM}} \frac{d}{dt} v_{C_{SM}}{}_i \qquad \textbf{(A.9)}$$

The current across the equivalent capacitor can also be expressed as:

$$i_{Ceq} = \frac{1}{N_{SM}} \sum_{i=1}^{N_{SM}} i_{C_{SM}i} \qquad \textbf{(A.10)}$$

Now, the current of one SM capacitor is equal to the arm current if the SM is inserted or zero if the SM is bypassed. If there are n inserted SM capacitors, then Eq. (A.10) becomes:

$$i_{Ceq} = \frac{n}{N_{SM}} i_{arm} \qquad \textbf{(A.11)}$$

Also, the voltage of an arm is the sum of all the SM voltages:

$$v_{arm} = \sum_{i=1}^{N_{SM}} v_{SM\,i} \qquad \textbf{(A.12)}$$

The voltage of one SM is equal to the voltage across its capacitor $v_{C_{SM}}$ if it is inserted or zero if it is bypassed. Then for n inserted SMs, Eq. (A.12) becomes:

$$v_{arm} = n \times v_{C_{SM}} \qquad \textbf{(A.13)}$$

Replacing the value of $v_{C_{SM}}$ from Eq. (A.5) into Eq. (A.13) yields:

$$v_{arm} = \frac{n}{N_{SM}} v_{C_\Sigma} \qquad \textbf{(A.14)}$$

Also, the modulation index can be expressed as:

$$m = \frac{n}{N_{SM}} \qquad \textbf{(A.15)}$$

Finally, the arm voltage can be expressed in terms of the modulation index:

$$v_{arm} = m \times v_{C_\Sigma} \qquad \textbf{(A.16)}$$

Eqs. (A.7), (A.11), (A.14) and Eq. (A.15) represent the reduced order average model of a single arm. Any converter using arm structures can be modelled with the use of the reduced order average model. This is also valid for the Modular Multilevel Converter.

A.2. Voltage to current adapting circuit for RTD measurement

The whole acquisition chain for performing temperature measurements with the multipurpose measurement board can be seen in Figure A.1. It uses the commercial NGW board for polarizing the Pt1000 sensor. In Figure A.1, V_{RTD} represents the voltage measured on the terminals of the Pt1000 sensor, V_{NGW} represents the output voltage of the NGW board and $V_{out_{calib}}$ is the voltage read by the Speedgoat machine.

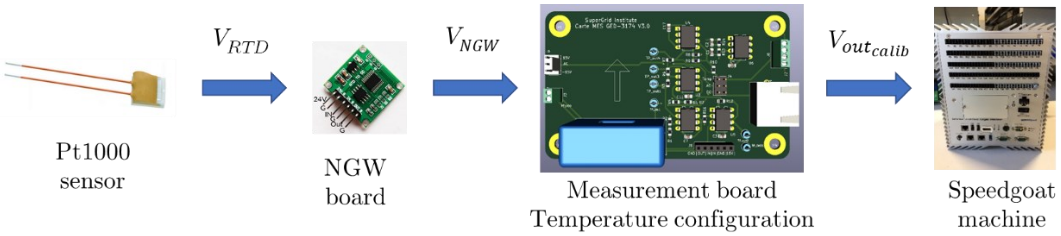


Figure A.1. Acquisition chain for temperature measurement

The allowable voltage across the shunt resistors of the Speedgoat machine is equal to ±1V. However, in order to be immune to any EMI perturbations and noises, it was decided to transmit the measurement information in the form of analog current signals. The chosen range for the current measurement is between -10 mA and 10 mA.

It is important to maximize the range of measurements. Hence, the lowest current will be sent when a temperature of 0°C is read by the Pt1000 RTD sensor. On the other hand, the maximum current will be read when the temperature is equal to 100°C.

Considering the allowable voltage range and the chosen current range for transmitting the information, the shunt resistors should have a value of 100 Ω. After characterizing the op-amp THS4551 used in the measurement circuit, a current offset of 1 mA was noticed. Thus, the circuit should be dimensioned so that $-11\text{mA} \rightarrow 0°\text{C}$ and $9\text{mA} \rightarrow 100°\text{C}$, which implies that $-1.1\text{V} \rightarrow 0°\text{C}$ and $0.9\text{V} \rightarrow 100°\text{C}$ across R_{shunt}.

The desired calibrated voltage in terms of the measured voltage is given by Eq. (A.17).

$$V_{out_{Calib}} = \frac{V_{max} - (V_{min})}{T_{max}} T_{meas} + b = \frac{0.9 - (-1.1)}{100} T_{meas} + b \tag{A.17}$$

At $T_{meas} = 100°\text{C} \rightarrow V_{out_{Calib}} = 0.9\text{V}$, therefore b yields:

$$b = V_{out_{Calib}} - \frac{V_{max} - (V_{min})}{R_{shunt}} T_{max} = 0.9\text{V} - \frac{0.9\text{V} - (-1.1\text{V})}{100°\text{C}} 100°\text{C} = -1.1$$

From the NGW measurement board datasheet, Eqs. (A.18), (A.19):

$$V_{NGW} = \frac{5.073}{350} T_{meas} + \frac{5.073 \times 50}{350} \tag{A.18}$$

$$T_{meas} = V_{RTD} \frac{350}{5.073} - 50 \tag{A.19}$$

After replacing the value of b in Eq. (A.17) yields:

$$V_{out_{Calib}} = \frac{2}{100} T_{meas} - 1.1 \qquad \textbf{(A.20)}$$

If Eq. (A.19) is replaced in Eq. (A.20), Eq. (A.21) is obtained.

$$V_{out_{Calib}} = \frac{2}{100}\left(V_{RTD}\frac{350}{5.073} - 50\right) - 1.1 = 1.38V_{RTD} - 2.1 \qquad \textbf{(A.21)}$$

It will be therefore practical to apply a gain of 1.38 and an offset of 2.1 V to the output signal of the NGW measurement board for obtaining the desired analog signal. Thus, the desired block diagram for the voltage to current adapting circuit can be seen in Figure A.2.

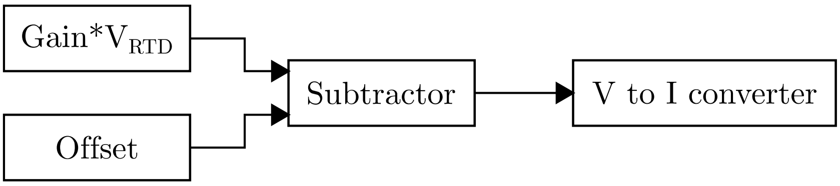


Figure A.2. Block diagram for RTD adapting circuit

For the gain stage an op-amp was used in a non--inverting configuration. The transfer function of this circuit will be given by Eq. (A.22).

$$V_{gain} = \left(1 + \frac{R_4}{R_3}\right) V_{RTD} \qquad \textbf{(A.22)}$$

With $R_4 = 1k\Omega$ and $R_3 = 2.6k\Omega$ the desired voltage will be obtained.

For the offset stage a voltage divider as well as a voltage follower circuit will be used. The offset voltage is obtained with Eq. (A.23) that represents the voltage divider equation.

$$V_{off} = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{1.2k}{7.3k + 1.2k} 5\text{V} = 2.11\text{V} \qquad \textbf{(A.23)}$$

The subtractor stage is also implemented with an op-amp circuit. Its transfer function is given by Eq. (A.24).

$$V_{sub} = \left(V_{gain} - V_{off}\right)\frac{R_8}{R_7} \qquad \textbf{(A.24)}$$

However, the same value was chosen for resistors R_8 and R_7, as well as for R_5 and R_6. Hence, the output of the subtractor stage is expressed in Eq. (A.25).

$$V_{sub} = 1.38V_{RTD} - 2.1 \qquad \textbf{(A.25)}$$

It is worth noting that $R = R_{10} = R_{11} = R_{12} = R_9$, then the following expressions characterize the V to I conversion stage:

$$I_{shunt} = I_1 + I_2 = \frac{V_{sub} - V_+}{R} + \frac{V_{aux} - V_+}{R} \qquad \textbf{(A.26)}$$

$$V_- = \frac{R_{10}}{R_{10} + R_{11}} V_{aux} \qquad \textbf{(A.27)}$$

Knowing that $V_- = V_+$ yields Eq. (A.28):

$$V_{sub} = R \times I_{shunt} \tag{A.28}$$

Therefore, the schematic of the adapting circuit implemented on the measurement board can be seen in Figure A.3

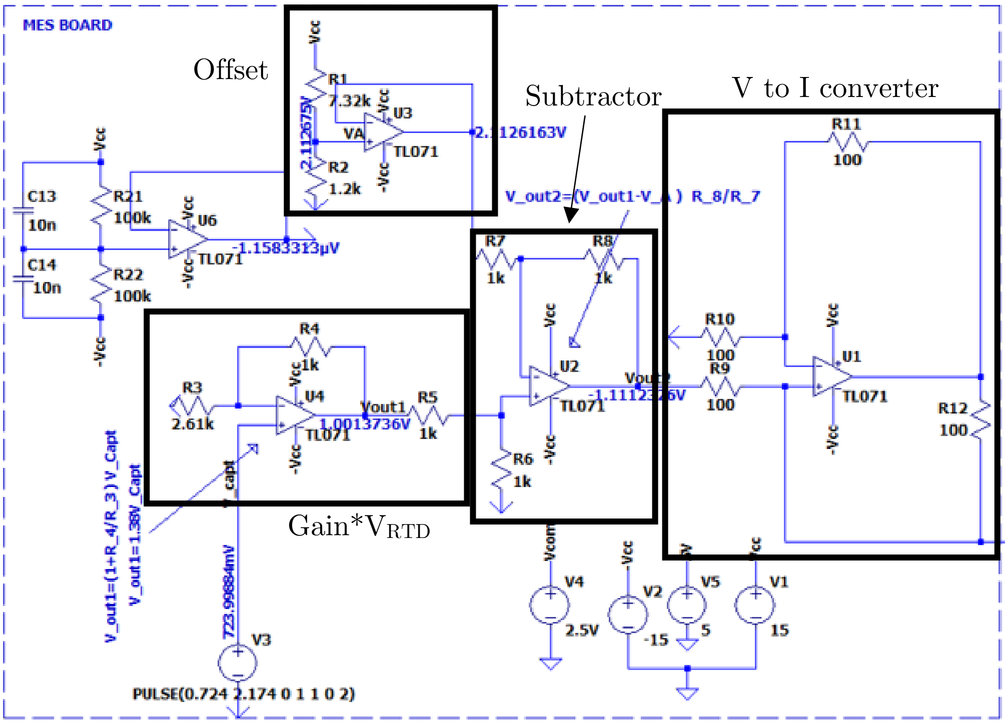


Figure A.3. Schematic of adapting circuit

A.3. Dimensioning of the V_{dc} board

The voltage transducer LEM LV-25P/SP must have a current on the primary $I_P = 10mA$. Since the DC voltage V_{DC} to be measured can be as high as 1200V it is necessary to distribute the current among many resistors as indicated on Figure A.4.

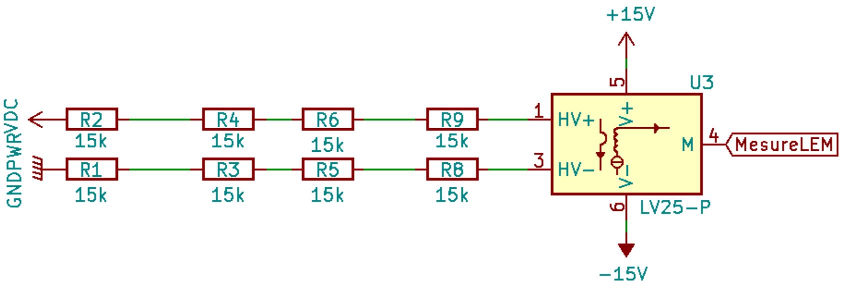


Figure A.4. Schema for the LEM voltage transducer

As it can be seen from Figure A.4, the chosen resistor value $R_{in} = 15k\Omega$. Therefore, the current on the primary can be obtained with Eq. (A.29).

$$I_P = \frac{V_{DC}}{8R_{in}} \tag{A.29}$$

From which $I_P \in [0mA\ 10mA]$, as the transformation ratio $k = 2500/1000$, the current on the secondary I_S will be given by Eq. (A.30). Therefore, $I_S \in [0mA\ 25mA]$

$$I_S = k\ I_P \tag{A.30}$$

A complete schematic of the elements of the V_{dc} board can be seen in Figure A.5.

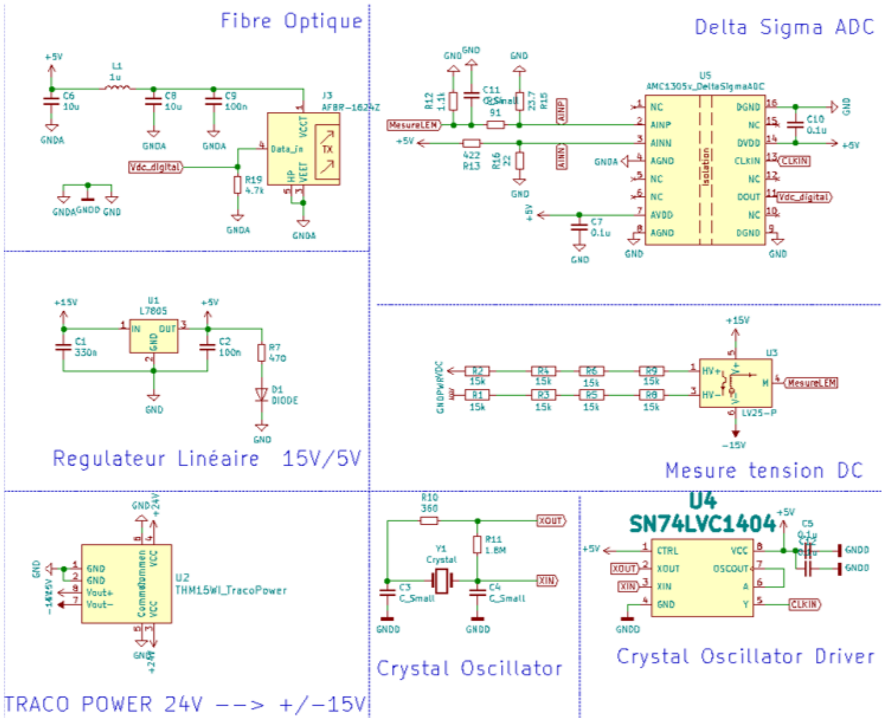


Figure A.5. Schematic V_{dc} board

Particular attention must be put to the charge resistor to be used at the nominal current, according to the datasheet of the LEM $R_{CHARGE} \in [100\Omega\ 340\Omega]$. The value of this resistor will be influenced by the impedance of the ΣΔ converter. In Figure A.6 the equivalent circuit of the ΣΔ ADC can be seen.

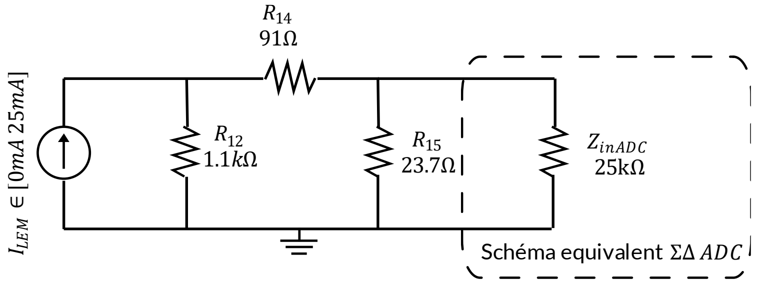


Figure A.6. Equivalent circuit of ΣΔ ADC

Therefore, the charge resistor can be calculated as:

$$R_{CHARGE} = [(R_{15}//Z_{inADC}) + R_{14}]//R_{12} = 103.85\Omega \tag{A.31}$$

Which verifies the required condition imposed by the LEM transducer.

The conditioning stage for the ΣΔ converter can be seen in Figure A.7.

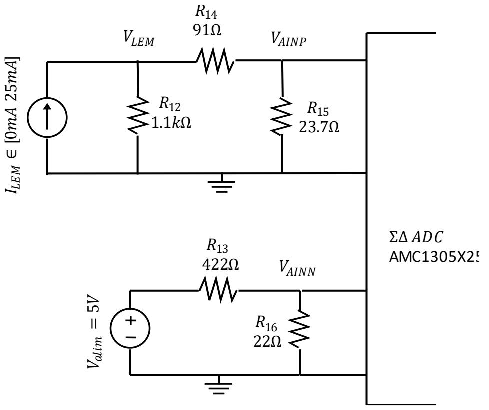


Figure A.7. Conditioning stage transfer equivalent circuit

For benefitting from the maximum range of the ADC it is desired to have:

$$\Delta V_{inADC} = V_{AINP} - V_{AINN} = 500mV$$

According to the datasheet of the ADC:

$$\frac{V_{AINP} + V_{AINN}}{2} \in [-0.16V\ ;\ 3V]$$

It was desired to fix the negative input voltage to: $V_{AINN} = \frac{R_{16}}{R_{16}+R_{13}} 5V \cong 0.25V$

From an inspection of the circuit depicted in Figure A.5, the voltage given by the current transducer is inferred:

$$V_{LEM} = I_S \times \frac{R_{12}(R_{14} + R_{15})}{R_{12} + R_{14} + R_{15}} \tag{A.32}$$

The voltage of the positive input of the ADC is dependent on the LEM voltage as expressed by Eq. (A.33).

$$V_{AINP} = \frac{R_{15}}{R_{15} + R_{14}} V_{LEM} \tag{A.33}$$

By replacing Eqs. (A.29)-(A.32) in Eq. (A.33) it can be obtained:

$$V_{AINP} = \frac{R_{15}}{R_{15} + R_{14}} \times \frac{R_{12}(R_{14} + R_{15})}{R_{12} + R_{14} + R_{15}} \times k \times \frac{V_{DC}}{8 * R_{in}} \tag{A.34}$$

Therefore:

$$\begin{cases} V_{DC} \in [0V; 1200V] \Rightarrow V_{AINP} \in [0V; 0.5V] \\ V_{AINN} = 0.25V \end{cases}$$

Which gives a differential voltage according to the specified conditions.

A.4. Additional information on the Relay board

The coil of the switches LTC002501*A02 will be fed through a voltage source of 24V. Knowing its power consumption the equivalent resistor can be calculated with Eq. (A.35).

$$R = \frac{U^2}{P} = \frac{24^2}{32} = 18\Omega \tag{A.35}$$

Then, the inductance of the coil can be inferred from its time constant with Eq. (A.36).

$$L = \tau \times R = 50ms \times 18 = 900m\text{H} \tag{A.36}$$

Subsequently, the current across its inductance is given by Eq. (A.37).

$$I = \frac{U}{R} = \frac{24}{18} = 1.33\text{A} \tag{A.37}$$

With this information the energy stored in the coil can be calculated with Eq. (A.38).

$$E = \frac{1}{2}LI^2 = \frac{1}{2}900 \times 10^{-3} \times (1.33)^2 = 796m\text{J} \tag{A.38}$$

This energy must be dissipated in some element during the opening of the circuit. In the case of this circuit diodes TVS were chosen for this purpose as seen on the schematic of Figure A.8, which corresponds to the hardware used for handling one relay.

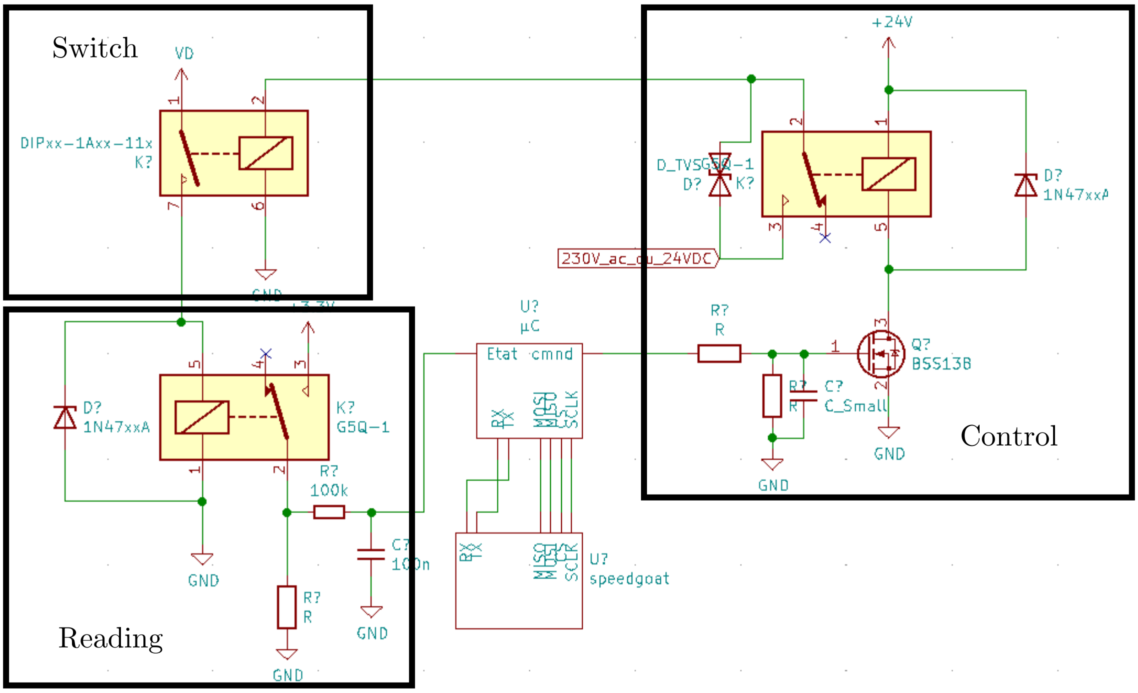


Figure A.8. Schematic for piloting one relay

A.4.1. Structure of the code for communication

The messages for commanding the relays and for reading its current state have the structure depicted on Figure A.9.

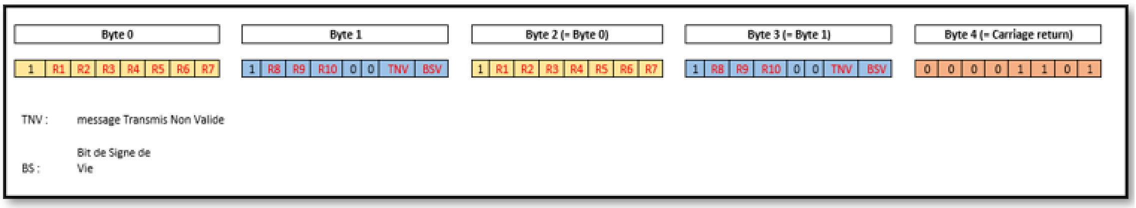


Figure A.9. Structure of a message

The byte 0 is equal to byte 2, and byte 1 is equal to byte 3. This was done for detecting any errors in the communication. Byte 4 has a constant value of 13 for identifying the end of a message. Once a message is valid bytes 0 and 1 transfer the information, in these messages R_x represents the state of a particular relay. Additionally, a health state bit (BSV) is used. Its state changes every 10ms and helps detect problems in the communication of the information. Finally, there is a bit that validates the structure of the received message (TNV).

The reception of the information is carried out with a FIFO buffer.

A.5. Construction of matrix *M* for the ALS method

The computation of matrix M was presented in [295]. For its calculation it is first necessary to consider the usual linear, time-invariant, discrete-time model defined by Eqs. (A.39), (A.40).

$$x_{k+1} = Ax_k + Bu_k + Gw_k \tag{A.39}$$

$$y_k = Cx_k + v_k \tag{A.40}$$

In which $A \in \mathbb{R}^{nxn}$, $B \in \mathbb{R}^{n\times m}$, $G \in \mathbb{R}^{n\times g}$, $C \in \mathbb{R}^{p\times n}$ and $w_k \sim \mathcal{N}(0, Q)$ and $v_k \sim \mathcal{N}(0, R)$. The state estimates of this model can be computed with the linear, time-invariant state estimator from Eqs. (A.41), (A.42).

$$\hat{x}_{k+1|k} = A\hat{x}_{k|k} + Bu_k \tag{A.41}$$

$$\hat{x}_{k|k} = \hat{x}_{k|k-1} + L\big[y_k - C\hat{x}_{k|k-1}\big] \tag{A.42}$$

Where L is the estimator gain, which is not necessarily the optimal gain. With the estimator, the state estimation error $e_k = x_k - \hat{x}_{k|k-1}$ evolves according to

$$e_{k+1} = (A - ALC)\, e_k + [G, -AL] \begin{bmatrix} w_k \\ v_k \end{bmatrix} \tag{A.43}$$

In Eq. (A.43) $\bar{A} = (A - ALC)$, $\bar{G} = [G, -AL]$ and $\overline{w}_k = \begin{bmatrix} w_k \\ v_k \end{bmatrix}$. Which yields:

$$e_{k+1} = \bar{A}\, e_k + \bar{G}\, \overline{w}_k \tag{A.44}$$

With knowledge of the state estimator and the evolution of the state estimation error the following terms can be defined

$$\mathcal{O} = \begin{bmatrix} C \\ C\bar{A} \\ \vdots \\ C\bar{A}^{N-1} \end{bmatrix}, \Gamma = \begin{bmatrix} 0 & 0 & 0 & 0 \\ C & 0 & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots \\ C\bar{A}^{N-2} & \cdots & C & 0 \end{bmatrix}, \Psi = \Gamma\big[\oplus_{j=1}^{N}(-AL)\big]$$

Where N represents a number of lags used in the autocovariance matrix seen in Eq. (4.33). Also $\oplus_{j=1}^{N}$ represents the matrix direct sum operator evaluated from $j = 1$ to N i.e $\oplus_{j=1}^{N}\mathbf{A}_i = \mathrm{diag}(\mathbf{A}_1, \mathbf{A}_2, \dots, \mathbf{A}_N)$.

It is necessary to remind that the noise covariance matrix of the measurement R determines the variation of the measurement noise v_k for each k iteration. Also, it is worth reminding that $(R)_s$ is a vectorized representation of the matrix R, in which all its columns are stacked.

Consequently, an operator $\mathscr{I}_{p,N}$ can be defined, where p is the number of rows of matrix C. It represents a permutation matrix that allows the conversion of the direct sum to a vector, i.e. $\mathscr{I}_{p,N}$ is the $(pN)^2 \times p^2$ matrix of zeros and ones satisfying:

$$\left(\oplus_{j=1}^{N} R\right)_s = \mathscr{I}_{p,N}(R)_s$$

Then an intermediate term D can be calculated as seen on Eq. (A.45).

$$D = \left[(\mathcal{O} \otimes \mathcal{O})(I_{n^2} - \bar{A} \otimes \bar{A})^{-1} + (\Gamma \otimes \Gamma)\not{\mathcal{I}}_{p,N}\right] \tag{A.45}$$

In Eq. (A.45) the $\otimes$ operator represents the Kronecker product i.e. $\mathbf{A} \otimes \mathbf{B} = \begin{bmatrix} a_{11}\mathbf{B} & \cdots & a_{1n}\mathbf{B} \\ \vdots & \ddots & \vdots \\ a_{m1}\mathbf{B} & \cdots & a_{mn}\mathbf{B} \end{bmatrix}$, if $\mathbf{A}$ and $\mathbf{B}$ are arbitrary matrices.

Finally, the M matrix required for the computation of the noise covariance matrices can be obtained with Eq. (A.46).

$$M = \left[D(G \otimes G) \,\middle|\, \begin{matrix} D(AL \otimes AL) \\ +[\Psi \oplus \Psi + I_{p^2N^2}]\not{\mathcal{I}}_{p,N} \end{matrix} \right] \tag{A.46}$$

In which the operator $\oplus$ represents the Kronecker sum i.e. $\mathbf{A} \oplus \mathbf{B} = \mathbf{A} \otimes I_g + I_m \otimes \mathbf{B}$, where $\mathbf{A}$ is a matrix of size $m \times p$ and $\mathbf{B}$ a matrix of size $g \times h$ and the $\otimes$ operator represents the Kronecker product.

A.6. Résumé étendu en Français

A.6.1. Introduction générale

A.6.1.1. Contexte

Les réseaux de transport d'électricité ont dû s'adapter pour faire face aux défis de la croissance de la demande d'énergie, la rapide expansion des moyens de production des énergies renouvelables et l'éloignement des centres de production et des centres de consommation. Dans ce contexte, la transmission d'énergie en courant continu à très haute tension (HVDC) commence à s'imposer comme la technologie privilégiée pour les applications de forte puissance [5]–[7].

Dans les systèmes de transmission HVDC, le convertisseur de puissance joue un rôle majeur. Cet équipement réalise la conversion du courant continu (DC) en courant alternatif (AC), pour pouvoir interfacer le lien HVDC au réseau de puissance existant en AC. De plus, le convertisseur de puissance peut fournir des services supplémentaires au système electrique.

Il existe 2 grandes familles de convertisseurs utilisées dans les systèmes HVDC : les convertisseurs à source de courant (CSC) et les convertisseurs à source de tension (VSC). Aux terminaux AC, les convertisseurs de chacune de ces familles se comportent respectivement comme une source de courant ou une source de tension.

Dans le cas des CSC, la topologie « Line Commutated Converter » (LCC) est la plus utilisée. Ce type de convertisseur utilise des thyristors comme éléments de commutation. Ces composants ont un amorçage commandé, alors que le retour à l'état bloqué se fait lors d'un passage à zéro de courant. C'est la raison pour laquelle ces convertisseurs dépendent d'un circuit extérieur pour fonctionner. Ceci implique une connexion a un réseau alternatif fort. Par ailleurs, la topologie LCC nécessite des filtres pour la compensation d'énergie réactive ainsi que pour réduire les ondulations de courant aux terminaux AC du convertisseur. Il est important de remarquer que pour réaliser des inversions du sens de puissance, les convertisseurs LCC doivent inverser la polarité de la tension continue, caractéristique qui complexifie grandement leur utilisation dans le cadre de réseaux maillés.

Afin de surmonter les inconvénients des convertisseurs CSC, la technologie VSC est apparue et a gagné en importance à partir des années 1990s [11]. Les convertisseurs VSC utilisent des transistors bipolaires à grille isolée (IGBT) comme éléments de commutation. Ces composants nécessitent une commande en tension. Ils conjuguent les avantages des transistors à effet de champ et des transistors bipolaires. Ainsi, ils sont capables de réaliser des commutations rapides avec des chutes de tension à l'état passant très faibles. Ces composants sont commandables à l'ouverture et à la fermeture, ce qui rend le processus de commutation indépendant du circuit extérieur auquel le convertisseur se connecte. Comme l'ouverture des IGBTs est commandée, les convertisseurs VSC peuvent avoir des fréquences de commutation plus élevées que les CSC. De ce fait, les exigences du filtrage harmonique, aussi bien en taille qu'en nombre, pour les VSC se trouvent réduites [13].

La première topologie de type CVS apparue pour des applications HVDC est le convertisseur 2 niveaux. Cette topologie nécessite la mise en série d'un grand nombre d'IGBT pour former un seul interrupteur. Par conséquent, elle requiert une synchronisation parfaite lors de la commutation des composants. De même, ce type de convertisseur doit utiliser des dispositifs d'équilibrage, actifs ou passifs, causant des pertes additionnelles, afin d'égaliser les tensions aux bornes de chaque IGBT.

Pour pallier ces problématiques, une première approche a été d'augmenter le nombre de niveaux de tension. Donc, des nouvelles topologies sont apparues telles que le convertisseur à capacités flottantes (FC), le convertisseur cascadé en pont en H (CHB) ou les topologies 3 niveaux, parmi lesquelles le « Neutral Point Clamped » (NPC) est la plus répandue. Néanmoins, le problème de la mise en série des composants persiste dans les topologies citées. Raison pour laquelle une solution modulaire s'avère plus pertinente.

A.6.1.2. Convertisseur Modulaire Multiniveaux

Une avancée technique majeure dans le domaine des convertisseurs VSC a eu lieu avec l'introduction du convertisseur modulaire multiniveaux (MMC) [19]–[21]. Cette topologie est présentée sur la Figure A.10 (a). Outre les avantages fournis par les topologies VSC, la structure modulaire du MMC permet une meilleure qualité des formes d'onde en sortie, et un meilleur rendement grâce à une réduction des pertes de commutation permise par le nombre élevé des étages de conversion.

Cette topologie se compose de trois bras identiques, un pour chaque phase du réseau. Chaque bras, en lui-même, est constitué d'un demi-bras supérieur et inférieur. Ces derniers sont connectés avec le pôle positif et négatif de la tension DC. Chaque demi-bras est constitué d'une inductance de bras L_{arm} et de la mise en série de N modules de puissance élémentaires, appelés sous-modules (SMs). Plusieurs types des configurations des SM existent [22], cependant, seules les topologies demi-pont (HB-SM) et pont-complet (FB-SM) sont utilisées en pratique. La topologie HB-SM (cf. Figure A.10 (b)) est la plus utilisée aujourd'hui, compte tenu du prix de cette solution et de son meilleur rendement.

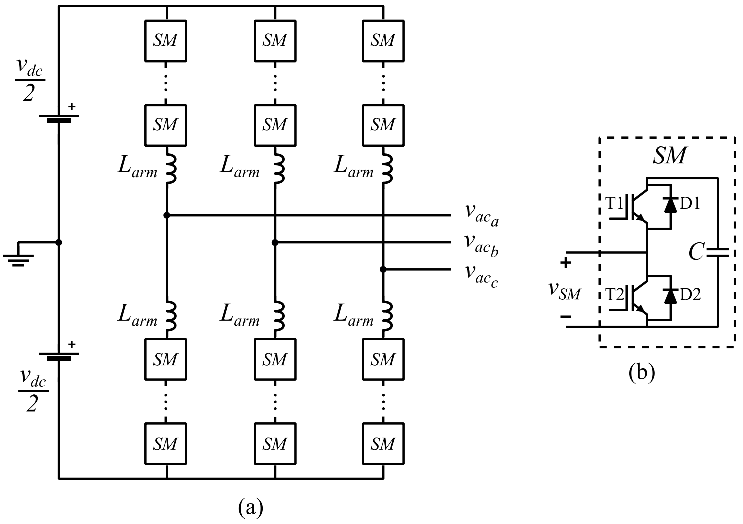


Figure A.10. (a) Convertisseur Modulaire Multiniveaux, (b) Sous-module half-bridge

Le module HB-SM est constitué d'un condensateur et de 2 interrupteurs de puissance. Chaque interrupteur est composé d'un IGBT et d'une diode en antiparallèle, permettant de conduire les courants négatifs. Les interrupteurs permettent l'insertion ou le bypass du condensateur. La tension en sortie d'un demi-bras est contrôlée en générant des paliers de tension. Chaque HB-SM apporte un échelon de tension si le SM est inséré. En revanche, l'apport en tension d'un SM sera nul si le SM est bypassé. La tension du réseau AC en sortie est proportionnelle à la différence des tensions entre les demi-bras d'une même phase, tandis que la somme des tensions des demi-bras donne la tension du bus DC. Ce principe de fonctionnement est illustré dans la Figure A.11.

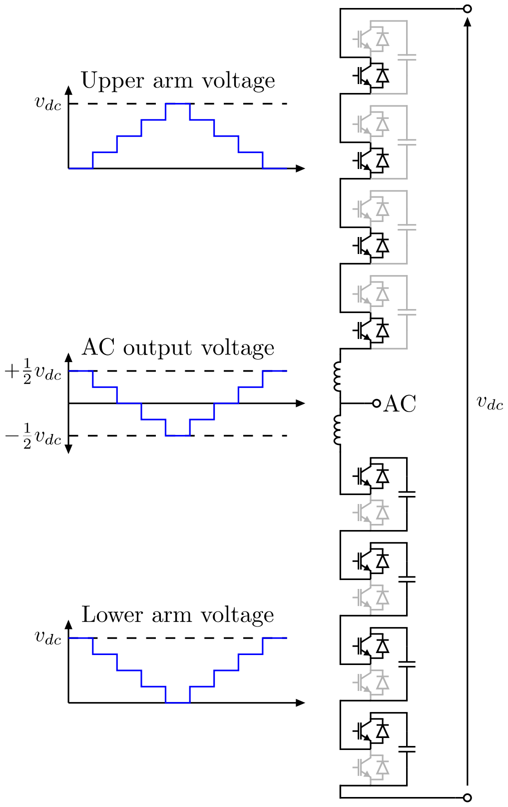


Figure A.11. Principe de fonctionnement d'un bras du MMC

A.6.1.3. Énoncé du problème et portée de la thèse

D'après le réseau européen des gestionnaires de réseau de transport d'électricité (ENTSO-E) les gestionnaires des réseaux de transport (GRT) ainsi que les utilisateurs des systèmes HVDC doivent améliorer la fiabilité (par exemple, réduire 1 à 2 déclenchements par an en moyenne) et la disponibilité (par exemple, réduire 1 à 2 jours d'interruption par an en moyenne) des réseaux. Ces améliorations auront un impact positif pour les GRT et la société [23].

Ce travail vise à contribuer à l'amélioration de la fiabilité et de la disponibilité du convertisseur MMC. Comme mentionnée précédemment, le SM est la brique de base du convertisseur. C'est pour cette raison que cette recherche se limitera à l'étude de la fiabilité des SMs. Plus particulièrement, cette thèse abordera la fiabilité des transistors IGBT car d'après des enquêtes [24], les semiconducteurs sont les éléments les plus fragiles au sein des convertisseurs de puissance.

L'analyse du profil thermique des IGBT sera utilisé pour évaluer la consommation de durée de vie de ces éléments et pour réaliser des calculs de fiabilité. Par ailleurs, cette thèse abordera la surveillance de l'état de santé des IGBT en suivant des grandeurs électriques sensibles à la dégradation.

Ce manuscrit de thèse est organisé en quatre chapitres.

Dans le premier chapitre, l'état de l'art des mécanismes de défaillances des IGBT, ainsi que des techniques pour le suivi de l'état de santé et le pronostic de la durée de vie restante des IGBT sont présentés.

Dans le chapitre deux, la modélisation d'un convertisseur MMC, ayant pour but des analyses de fiabilité, est réalisée.

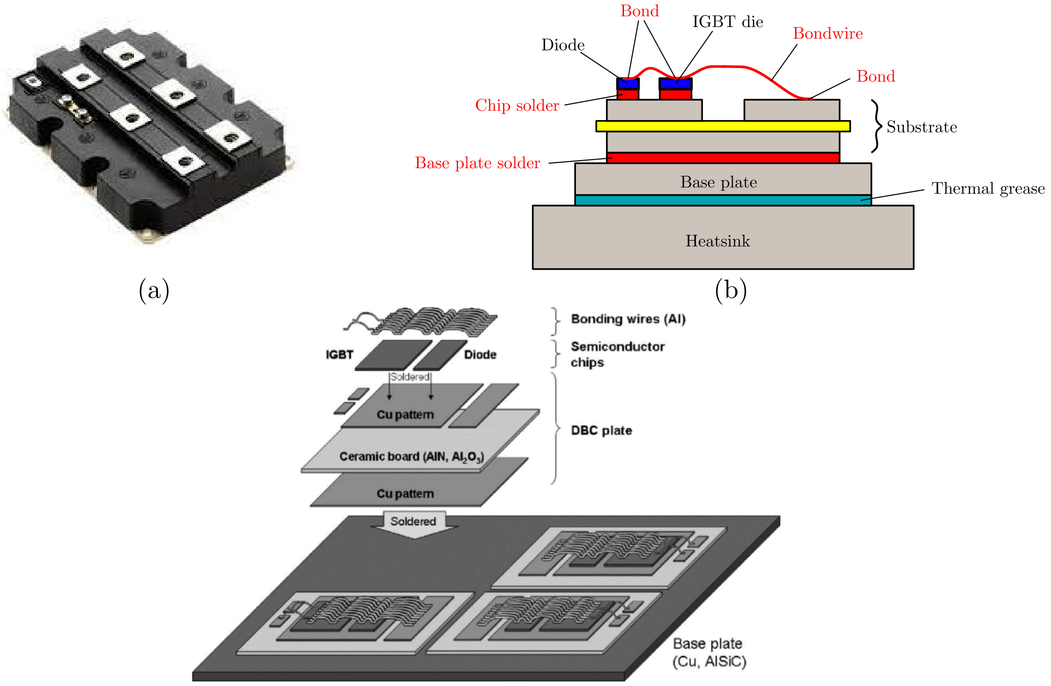
Le chapitre trois aborde les calculs de consommation de durée de vie des IGBT d'un MMC, compte tenu du profil de mission subi par les semiconducteurs. Ce chapitre développe également des calculs de fiabilité du convertisseur.

Finalement, le chapitre quatre présente la réalisation des tests de cyclages actifs, nécessaires pour valider les calculs de fiabilité et pour faire le suivi des paramètres électriques pour la surveillance de l'état de santé des IGBT.

A.6.2. Chapitre 1 : Etat de l'art

A.6.2.1. Le module IGBT et ses mécanismes de défaillance

Un module IGBT pour des applications de forte puissance, ainsi que sa structure interne peuvent être observés dans la Figure A.12.



(a) (b)

(c)

Figure A.12. Module IGBT : (a) boitier de puissance [40], (b) structure interne du module [40], [42], [46], (c) vue en détail des couches de la structure interne [47]

La littérature distingue les mécanismes de défaillance des modules IGBT selon le lieu où la défaillance commence à se manifester. Ainsi, ces mécanismes peuvent être liés à des problèmes dans la puce semiconducteur ou packaging [49]. Des travaux de recherche précédents, affirment que, pour les modules de puissance, les défauts liés à des problèmes de packaging sont les plus courants [49].

Il est aussi nécessaire de pouvoir suivre la dégradation des modules pour pouvoir développer des moyens de surveillance de l'état de santé. Dans le cas des défauts liés au semiconducteur, la majorité des défaillances sont dues à des conditions de stress soudains et imprévisibles qui ne peuvent pas être suivies. Cependant, les défauts liés au packaging sont de nature progressive, donc ils peuvent être monitorés.

Les mécanismes de défaillance progressifs des boitiers de puissance sont : la fatigue thermomécanique, le fluage thermomécanique, l'électromigration et la corrosion [72], [86]. Cependant, ce sont les mécanismes de défaillance liés à la fatigue thermomécanique les plus importants [49]. Aussi, ils seront abordés plus en détail.

La cause principale des problèmes de fatigue thermomécanique est la différence entre les coefficients d'expansion thermique (CTE) des différentes couches à l'intérieur du module [72]. La dégradation des fils de bonding, la dégradation des couches de soudure et la dégradation des couches de métallisation, sont les principales conséquences de la fatigue thermomécanique des modules IGBT.

A.6.2.2. Surveillance de l'état de santé des IGBT

La surveillance de l'état de santé est connue sous le nom de « Condition Monitoring » (CM) en anglais. Cette technique consiste à réaliser des mesures en temps réel des grandeurs qui donnent une indication de l'état de santé du système étudié. Le but du CM est de prendre des actions en tenant compte de l'état actuel du système.

Dans le cas des IGBT, il existe de nombreux paramètres électriques dont la dérive est une indication de la dégradation du module. Dans la Table A.1, les paramètres sensibles à la dégradation (DSEPs) et les modes et mécanismes de défaillance associés peuvent être observés.

Dans la Table A.1, il est possible de voir que la tension collecteur-émetteur pendant la phase de conduction $V_{CE(on)}$ est un paramètre qui permet de suivre l'évolution de plusieurs mécanismes de défaillance. C'est pour cette raison que ce paramètre a été beaucoup utilisé pour la surveillance de l'état de santé des IGBT dans des travaux précédents [51], [110]–[119]. Un travail approfondi sur les circuits de mesure de cette grandeur sera évoqué dans le chapitre quatre. Il est important de remarquer qu'une variation de 5% sur la valeur de $V_{CE(on)}$ indique la fin de la durée de vie du semiconducteur [171].

Le suivi de la résistance thermique R_{th} est très utilisé pour la surveillance de l'état de santé des joints de soudure entre les couches présentes dans la structure des IGBT. Une augmentation de la résistance thermique est indicatrice de la dégradation du chemin de refroidissement et une variation de 20% sur la valeur initiale de R_{th} est indicatrice de la fin de la durée de vie de l'IGBT [171].

Localisation de la défaillance		Modes de défaillance	Mécanismes de défaillance	DSEPs
Au niveau de la puce	Puce	Court-circuit, perte de contrôle de la grille	Latch-up et panne secondaire	$V_{CE(on)}$ t_{off} $V_{GE(th)}$
		Court-circuit, perte de contrôle de la grille	Rupture diélectrique dépendante du temps	V_{GE} $V_{GE(th)}$
Au niveau du boitier	Fils de bonding : liaison	Détachement du fil	Fatigue et/ou reconstruction	t_{on} t_{off} $V_{CE(on)}$ V_{GE}
	Fils de bonding : talon	Casse du talon	Fatigue	
	Fils de bonding : corps	Fil ouvert, fil brulé	Corrosion, échauffement	
	Joint de soudure	Fissures du joint de soudure	Fatigue ou croissance des grains	R_{th} $V_{CE(on)}$ t_{off} Harmoniques faibles

Table A.1 Localisation, modes et mécanismes de défaillance associés aux DSEPs respectifs [51]

A.6.2.3. Pronostic de la durée de vie restante des IGBT

La bibliographie distingue deux approches pour la prédiction de la durée de vie restante des IGBT. Les méthodes basées sur l'étude de la physique de la défaillance « Physics-of-Failure » (PoF), et les méthodes basées sur l'exploitation des données « Data-based ».

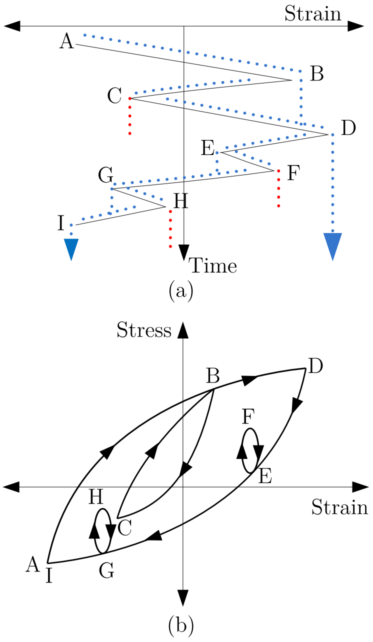
A.6.2.3.1. Méthodes PoF

Les méthodes de pronostic utilisant des méthodes PoF analysent les causes physiques de la défaillance en tenant compte des géométries, des propriétés des matériaux et des conditions d'opération et de l'environnement pour donner une estimation de la durée de vie restante. Un des résultats majeurs issue de l'utilisation des méthodes PoF sont les modèles de durée de vie des semiconducteurs.

Les modèles de durée de vie les plus utilisés, considèrent le profil thermique pour réaliser une estimation de la consommation de la durée de vie. En général, ce type de modèle se focalise sur des cycles thermiques caractérisés par une température de référence T_{ref}, une variation de température ΔT_j et la durée du cycle thermique appliqué t_{cycle}. Un exemple est la loi de Bayerer [144] (Eq. (A.47)). Cette loi considère d'autres paramètres pour l'estimation d'un nombre de cycles jusqu'à la défaillance N_f selon la condition thermique appliquée. Différents coefficients β_i sont appliqués aux paramètres du modèle pour mieux décrire l'influence de chaque paramètre sur la durée de vie.

$$N_f = A \cdot \Delta T_j^{\beta_1} \cdot \exp\left(\frac{\beta_2}{T_{j_{min}} + 273}\right) \cdot t_{on}{}^{\beta_3} \cdot I_B{}^{\beta_4} \cdot V_C{}^{\beta_5} \cdot D^{\beta_6} \tag{A.47}$$

Ensuite, il est nécessaire de pouvoir identifier les cycles thermiques subis par les semiconducteurs dans des applications réelles. Il faut donc, décomposer les profils thermiques dans des cycles élémentaires à l'aide des méthodes de comptage des cycles thermiques. La méthode de comptage la plus précise, selon la littérature, est l'algorithme rainflow [156]. Cette méthode est illustrée dans la Figure A.13.



(a)

(b)

Figure A.13. Algorithme rainflow : (a) séquence de charge, (b) diagramme contrainte-déformation [140]

Finalement, l'estimation de la durée de vie D se fait en utilisant les modèles de dommages cumulés. Parmi ces modèles, la règle de Miner [49] (Eq. (A.48)) est la plus répandue. Elle suppose une contribution linéaire de toutes les cycles thermiques n subis par l'IGBT.

$$D = \sum \frac{n}{N_f} = 1 \tag{A.48}$$

A.6.2.3.2. Méthodes basées sur les données

Ce type de méthode n'a pas besoin d'une connaissance approfondie des phénomènes qui donnent lieu à la défaillance. Ces méthodes utilisent l'historique des paramètres sensibles à la dégradation. Les techniques basées sur les données les plus utilisées sont l'apprentissage automatique « machine learning » et des méthodes statistiques [51].

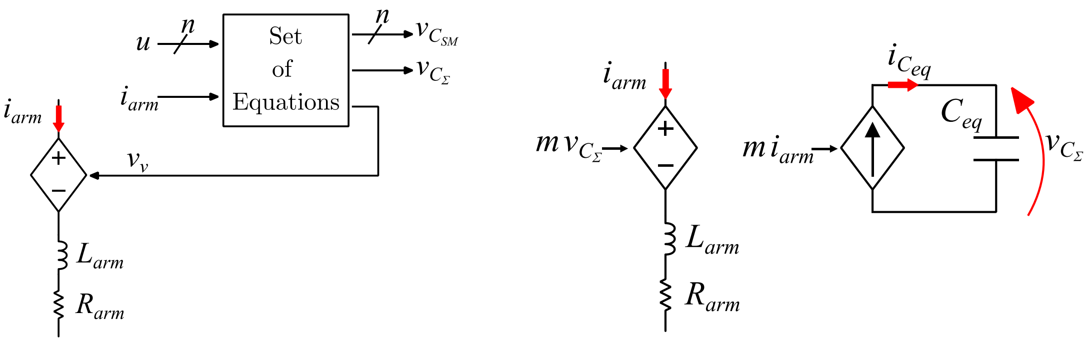
A.6.2.3.3. Méthodes de fusion

Il existe également des méthodes qui combinent les avantages des méthodes PoF et des méthodes basées sur les données. Ils utilisent la connaissance de la physique de la dégradation ainsi que l'historique des paramètres sensibles au vieillissement pour donner des estimations plus précises de la durée de vie restante des IGBT.

A.6.3. Chapitre 2 : Modélisation d'un convertisseur modulaire multiniveau pour l'analyse de fiabilité

Avant de pouvoir tester des méthodes de pronostic de la durée de vie ou faire la surveillance de l'état de santé des semiconducteurs, il est nécessaire de connaître les conditions d'opération et le profil de charge des IGBT dans l'application étudiée. Dans ce travail de thèse, l'application visée est celle d'un convertisseur MMC pour des applications HVDC. C'est pour cette raison qu'il faut développer un modèle du convertisseur MMC adapté aux études de fiabilité d'un HB-SM.

Il est important d'obtenir des formes d'onde pertinentes pour un seul HB-SM du convertisseur. Il est alors nécessaire de faire un modèle détaillé d'un sous-module. Cela est possible grâce aux modèles dits semi-analytiques [198] (cf. Figure A.14 (a)). Par ailleurs, il est important de voir l'influence du système environnant sur les formes d'onde du SM étudié. C'est pour cela que le reste du convertisseur est modélisé en utilisant un modèle moyen [189] (cf. Figure A.14 (b)). Ainsi, une approche de modélisation par demi-bras est adoptée pour représenter le convertisseur. Deux demi-bras d'une même phase de MMC sont modélisés en utilisant un modèle détaillé semi-analytique et les quatre demi-bras restants sont modélisés à l'aide d'un modèle moyen (cf. Figure A.15).



(a) (b)

Figure A.14. Modèles d'un demi-bras : (a) modèle détaillé semi-analytique, (b) modèle moyen

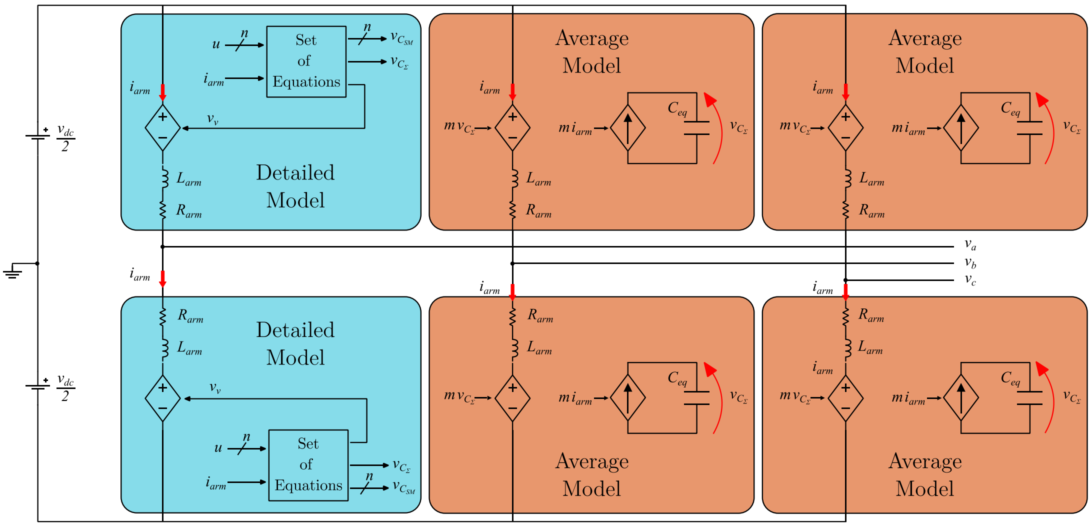


Figure A.15. Modèle mixte moyenné - détaillé d'un convertisseur MMC

Ensuite, le principe de fonctionnement du modèle mixte et l'approche générale du contrôle du convertisseur sont présentés. Dans la Figure A.16, le schéma du contrôle est exposé en identifiant deux étages principaux : contrôles de haut et de bas niveaux.

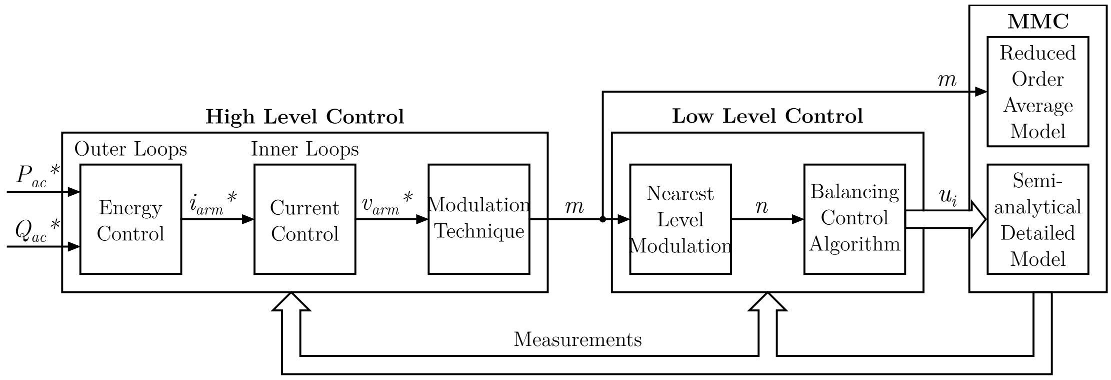


Figure A.16. Principe de contrôle du modèle mixte d'un convertisseur MMC

Le contrôle du haut niveau a pour but de calculer l'indice de modulation m de chaque demi-bras. Pour pouvoir réaliser ces calculs, des transformations $\Sigma\Delta$ sont utilisées et permettent le découplage des grandeurs AC et des grandeurs DC [189]. Le schéma du contrôle de haut niveau est présenté dans la Figure A.17.

Dans le schéma du contrôle haut niveau, il y a deux types de boucles de commande. La boucle externe contrôle l'énergie à l'intérieur du convertisseur pour garder un équilibrage énergétique entre phases et entre demi-bras. Les boucles externes donneront les consignes de courant de chaque demi-bras aux boucles internes. Ensuite, les boucles internes sont chargées de calculer les références des tensions pour chaque demi-bras afin de pouvoir faire les échanges de puissance souhaités. Finalement, les consignes en tension permettent de calculer l'indice de modulation m correspondant à chaque demi-bras. Il est important d'indiquer que pour garantir le bon fonctionnement du contrôle haut niveau, il faut que les boucles internes soient plus rapides que les boucles externes.

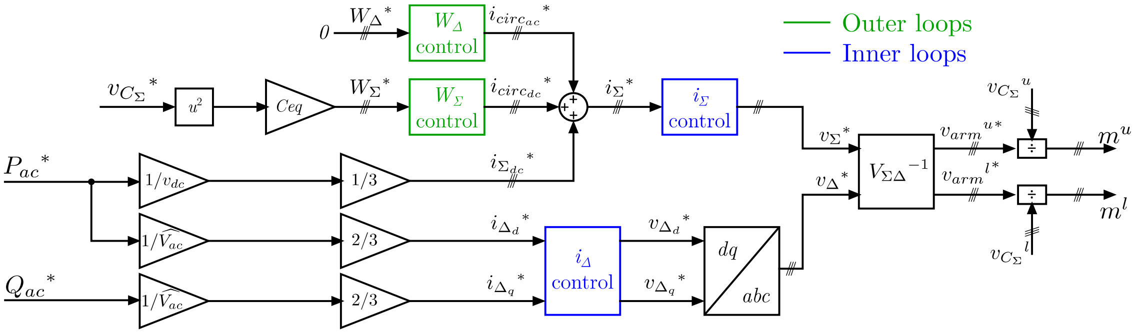


Figure A.17. Schéma du contrôle haut niveau d'une phase du MMC

Le contrôle de bas niveau consiste en une modulation dite du « niveau le plus proche » ou « Nearest Level Modulation » (NLM) [204] en anglais et en un algorithme d'équilibrage de la tension des condensateurs « Balancing Control Algorithm » (BCA) [208]. L'étage NLM détermine le nombre de sous-modules à insérer en fonction de l'indice de modulation m. Le BCA détermine quels SMs doivent être insérés en fonction de leur niveau de tension et du sens du courant du bras. Le contrôle bas niveau est appliqué aux demi-bras modélisés en utilisant le modèle détaillé semi-analytique.

Quelques résultats de simulation du fonctionnement du convertisseur sont illustrés à la Figure A.18. Ces résultats valident les stratégies de contrôle haut niveau implémentés. De plus, la Figure A.19 montre les formes d'onde d'un seul SM, ce qui permet de valider le contrôle du bas niveau.

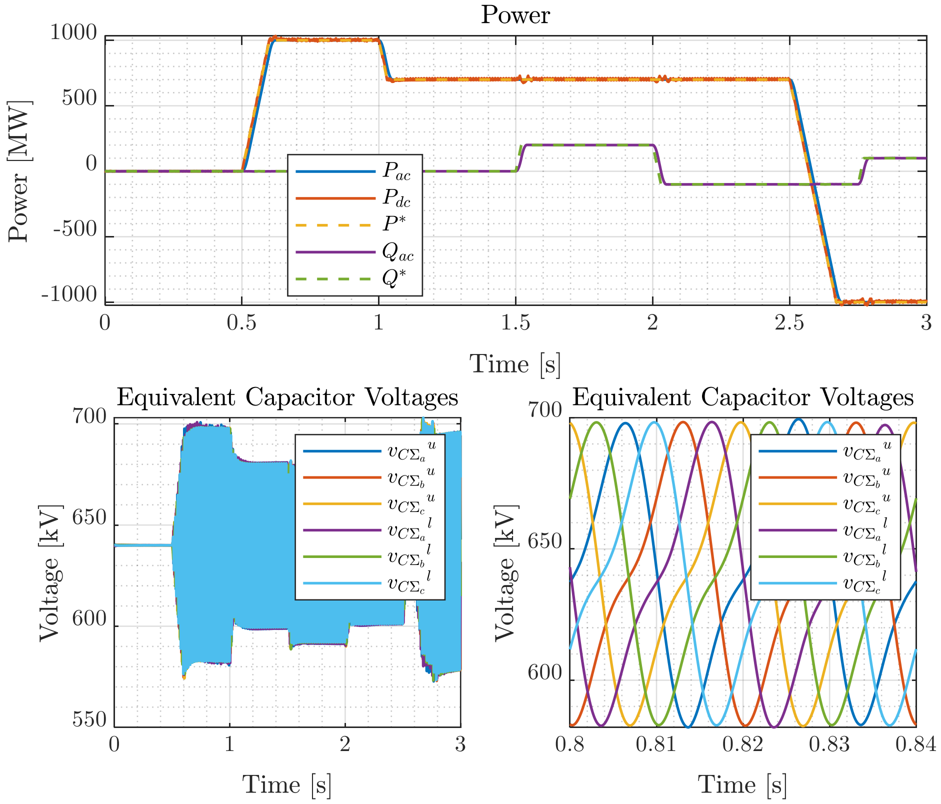


Figure A.18. Formes d'onde du convertisseur pour validation du contrôle haut niveau

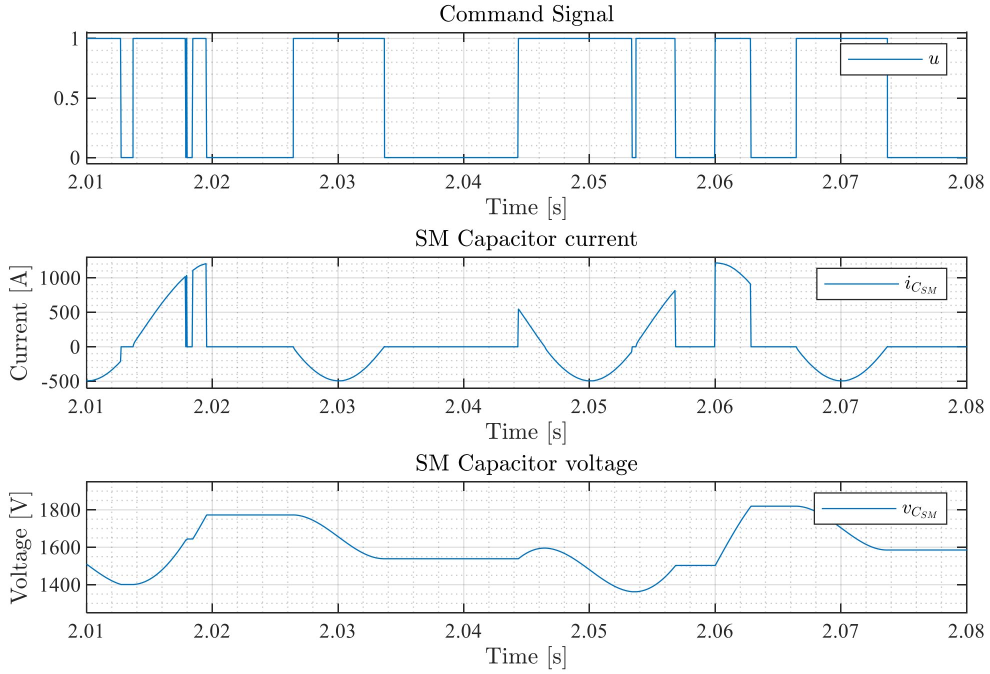


Figure A.19. Formes d'onde d'un SM pour validation du contrôle bas niveau

A.6.4. Chapitre 3 : Méthodes pour l'estimation de la durée de vie, des calculs de fiabilité et des niveaux de redondance

A.6.4.1. Estimation de la durée de vie des IGBT d'un HB-SM

La méthodologie utilisée pour l'estimation de la durée de vie des IGBT est présentée dans la Figure A.20. Elle se décompose en cinq étapes.

La première étape a été abordée dans le chapitre deux : elle consiste en la modélisation du convertisseur. Cette étape est nécessaire pour obtenir les formes d'onde électriques des semiconducteurs à l'intérieur d'un HB-SM. Ensuite, la deuxième étape consiste à faire une estimation des pertes dans les semiconducteurs en utilisant les tensions et courants des semiconducteurs ainsi que leur température de jonction T_j. La troisième étape adresse la modélisation thermique des semiconducteurs afin d'obtenir le profil thermique correspondant au profil de mission du convertisseur. Elle utilise les pertes comme donnée d'entrée pour calculer les profils thermiques. La quatrième étape consiste à organiser les profils thermiques des semiconducteurs en utilisant l'algorithme rainflow présenté dans le chapitre un. Finalement, la cinquième étape réalise un calcul de la consommation de la durée de vie dans la période évaluée, en utilisant les histogrammes fournis par l'algorithme rainflow avec des modèles de durée de vie existants et en appliquant la règle de Miner.

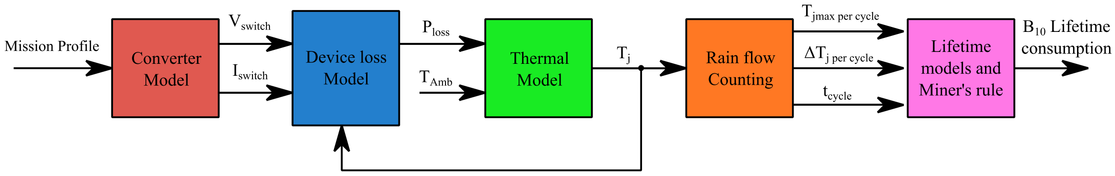


Figure A.20. Méthodologie pour l'estimation de la durée de vie des IGBT d'un HB-SM

Dans la deuxième étape, correspondant à l'estimation des pertes, des tableaux des données calculant les pertes dans les semiconducteurs ont été utilisés. Ces tableaux ont été remplis en utilisant le point de fonctionnement du convertisseur, la température de jonction et les données de la feuille de données (datasheet) [218]. Ils permettent aussi, d'améliorer la vitesse d'exécution des calculs. Un tableau des données utilisé dans cette étape est montré dans la Figure A.21.

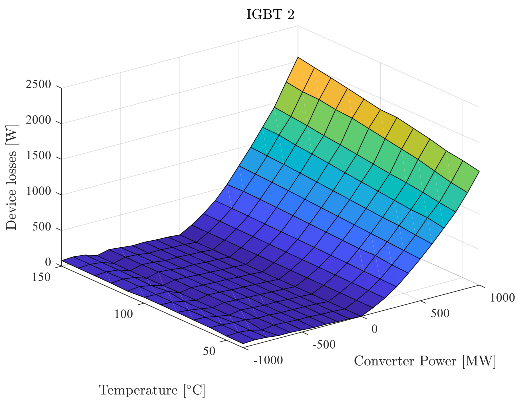
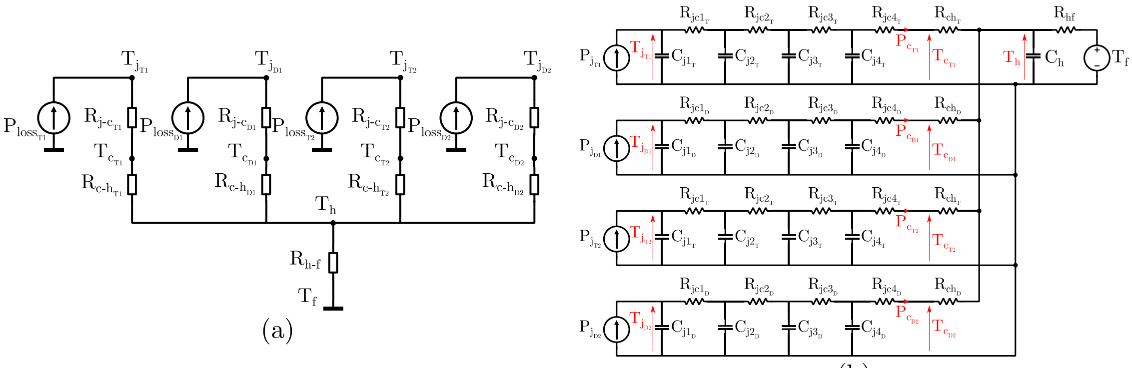


Figure A.21. Représentation graphique des données pour le calcul des pertes de l'IGBT 2

L'étape de modélisation thermique utilise aussi des données de la datasheet [218] pour construire deux modèles thermiques. Le premier est un modèle statique pour l'estimation de durée de vie sur des données avec un temps d'échantillonnage supérieur à dix minutes. Le deuxième type de modèle est un modèle dynamique qui prend en considération les constantes de temps pour le calcul des profils thermiques avec des données échantillonnées sur des durées inferieures à dix minutes. Les modèles développés correspondent à une représentation Cauer et peuvent être analysés dans la Figure A.22.



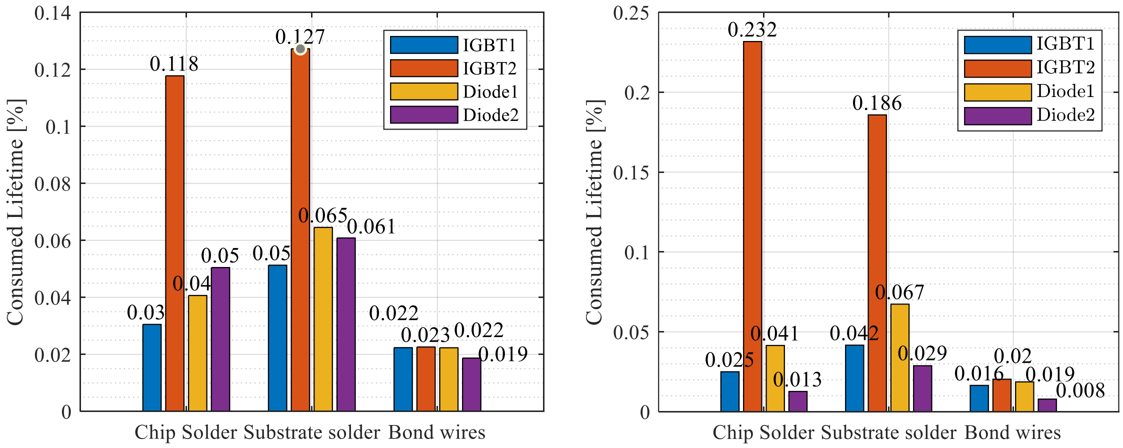
(a) (b)

Figure A.22. Modèles thermiques : (a) modèle statique, (b) modèle dynamique

Des données de cyclage thermique des fabricants [215] ont été utilisées pour calculer la consommation de durée de vie avec une probabilité de défaillance de 10% « B_{10} lifetime ». Ces modèles adressent des éléments internes des IGBT comme les fils de bonding et les couches des soudures. Ensuite, une méthode pour l'extrapolation de ces données a été développée. Elle est basée sur la loi de Norris-Landzberg (cf. Eq. (A.49)) pour réaliser les calculs des coefficients α, β et γ correspondants à un profil thermique donné.

$$N_{f_2} = N_{f_1}\left(\frac{\Delta T_2}{\Delta T_1}\right)^{\alpha}\left(\frac{t_1}{t_2}\right)^{\beta}\exp\left(\frac{E_a}{k}\left(\frac{1}{T_2}-\frac{1}{T_1}\right)\right) \qquad \textbf{(A.49)}$$

Deux types de profil de mission ont été évalués dans cette étude. Un profil correspondant à un lien HVDC (P2P) et un profil du vent correspondant à une application de ferme éolienne offshore (OWF). La consommation de durée de vie pour les deux applications est présentée dans la Figure A.23.



(a) (b)

Figure A.23. Consommation de la durée de vie (a) P2P, (b) OWF

A.6.4.2. Prédictions de la fiabilité d'un HB-SM

Les estimations de la consommation de durée de vie sont utilisées pour calculer des indicateurs de fiabilité des SM. Dans le cas d'un SM, sa fiabilité dépend de la fiabilité des éléments qui le composent. D'un point de vue de la fiabilité, tous ses éléments sont associés en série, puisque la casse d'un d'entre eux entraîne la casse d'un HB-SM. La probabilité de défaillance cumulée (CDF) d'un système dont ses éléments sont associés en série est donnée par l'Eq. (A.50) et représentée graphiquement dans la Figure A.24.

$$F_{sys}(t) = 1 - \prod(1 - F_i(t)) \tag{A.50}$$

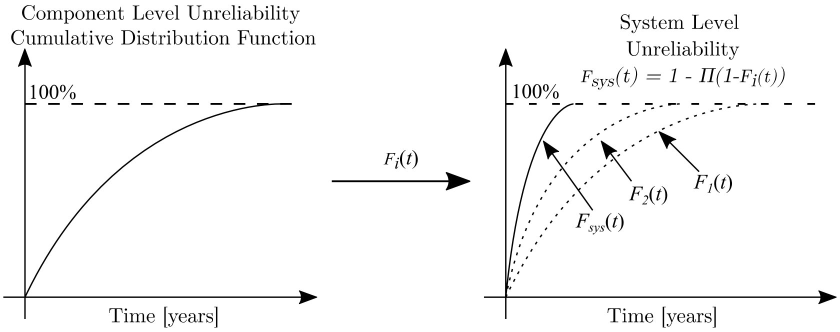


Figure A.24. Calcul de la probabilité de défaillance cumulée au niveau système

Avec la consommation de durée de vie, le temps jusqu'à une valeur de CDF de 10% est calculée pour chaque élément d'un SM. Avec cette information, il est possible de déterminer la CDF de cet élément à tout instant selon l'Eq. (A.51), elle correspond à la CDF de la distribution de Weibull [227]. Il est important de remarquer que le facteur de forme β n'est pas connu. Plusieurs valeurs de β seront donc évaluées.

$$F_k(t) = 1 - e^{-(\lambda_k t)^{\beta}} \tag{A.51}$$

Pour calculer la fiabilité d'un SM, le condensateur et la carte électronique du SM sont considérés. La CDF du SM et sa fonction de fiabilité R_{SM} sont données respectivement par l'Eq. (A.52) et l'Eq. (A.53). La R_{SM} est montrée dans la Figure A.25.

$$F_{SM}(t) = 1 - \prod\left(1 - F_m(t)\right), m \in \{\mathrm{T1, T2, D1, D2, Capacitor, Eboard}\} \tag{A.52}$$

$$R_{SM}(t) = 1 - F_{SM}(t) \tag{A.53}$$

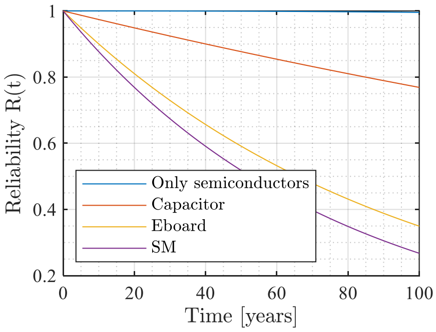


Figure A.25. Fiabilité d'un HB-SM et ses éléments, $\beta = 2.5$

A.6.4.3. Calcul de la redondance pour un demi-bras de MMC

Un des avantages du convertisseur MMC est la possibilité de rajouter des SMs redondants pour atteindre des niveaux de disponibilité compatibles avec les standards imposés par les GRT [225]. Cette disponibilité peut être calculée à partir des données de fiabilité d'un SM. Dans ce travail, il a été choisi de considérer une stratégie de redondance active [235], [236], car elle est la plus utilisée pour le MMC.

Dans un premier temps, une approche analytique a été considérée pour calculer le nombre des SMs redondants. Cette approche utilise la distribution binomiale pour calculer la fiabilité d'un demi-bras R_{arm} (cf. Eq. (A.54)). Ce résultat peut être interprété comme la probabilité de survie d'un demi-bras jusqu'à une première intervention de maintenance. Autrement dit, la probabilité qu'il y'ait au moins N_{min} SMs opérationnels, étant donné qu'il y a N_{red} SMs installés en plus. Plusieurs intervalles entre maintenances et plusieurs niveaux de redondance ont été évalués. Les résultats pour un MMC dans une application OWF et des résultats utilisant des indicateurs de fiabilité du fabricant sont présentées dans la Figure A.26.

$$R_{arm}(t) = \sum_{k=0}^{N_{red}} \frac{(N_{min}+N_{red})!}{k!\,(N_{min}+N_{red}-k)!}[1-R_{SM}(t)]^k[R_{SM}(t)]^{N_{min}+N_{red}-k} \qquad \text{(A.54)}$$

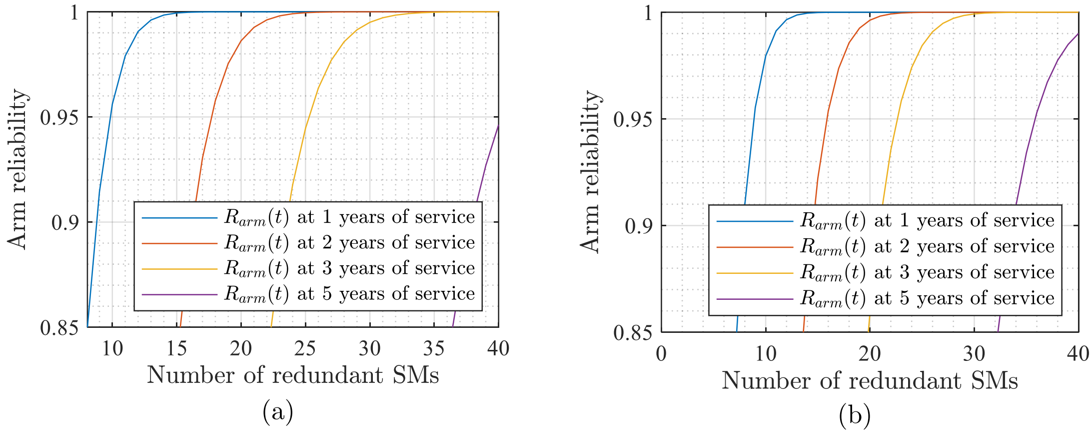


Figure A.26. Fiabilité d'un demi-bras : (a) données fabricant, (b) application OWF, $\beta = 2.5$

L'inconvénient de l'approche analytique est que la disponibilité sera approximée à la valeur de la fiabilité au moment de la première maintenance et il ne tient pas compte du vieillissement du système. Par ailleurs, la méthode analytique ne considère pas le remplacement des SMs défaillants entre deux maintenances. C'est pour cette raison qu'une approche différente a été conçue pour tenir compte de ces contraintes. Elle utilise des chaînes de Markov (cf. Figure A.27) et des simulations de Monte Carlo pour les calculs de la disponibilité en fonction du nombre des SMs redondants installés. Dans cette démarche, si un SM survit durant la période entre deux maintenances, sa fiabilité continue à se dégrader. Aussi, à chaque maintenance il est vérifié que le nombre de SMs défaillants soit inférieur à N_{red}. Si cela est le cas, les SMs défaillants sont remplacés par des nouveaux SMs ($R_{SM} = 1$). Si le nombre de SMs défaillants est supérieur à N_{red}, le demi-bras n'a pas survécu durant ce test particulier. Dix mille tests ont été réalisés pour chaque niveau de redondance et la disponibilité est approximée par la proportion des tests où les demi-bras ont survécu à la fin de la durée de service (40 ans). Les résultats sont présentés dans la Figure A.28.

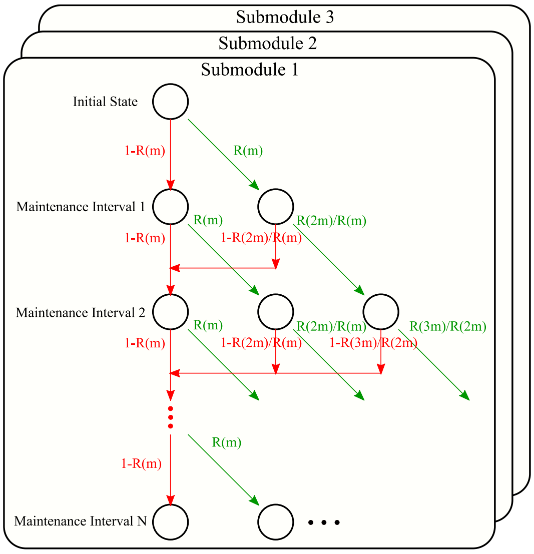


Figure A.27. Chaîne de Markov pour le calcul de la disponibilité d'un demi-bras

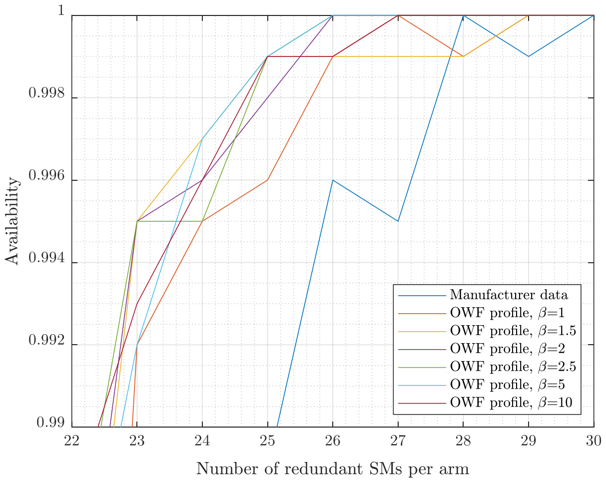
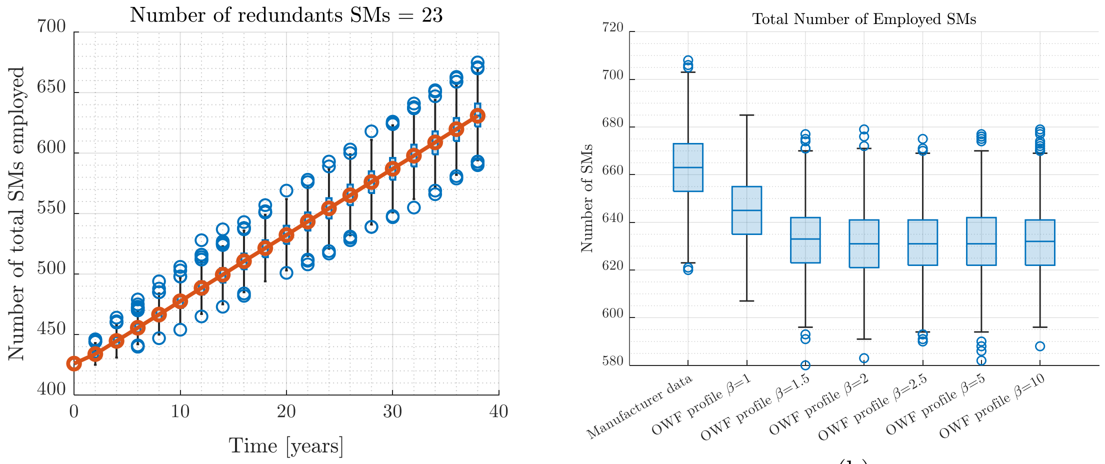


Figure A.28. Disponibilité d'un bras avec la chaine de Markov

Il est important de remarquer que l'approche avec la chaîne de Markov et les simulations de Monte Carlo, permet d'estimer le nombre total des SMs utilisés pendant la durée de service du convertisseur (cf. Figure A.29 (a)). De plus, une comparaison du nombre des SMs en utilisant les données du fabricant ou en évaluant les prédictions de fiabilité issues de la méthodologie pour l'estimation de la durée de vie peut être observée à la Figure A.29 (b). Seule l'application OWF a été évaluée car selon les résultats de consommation de durée de vie, ce scenario est le plus pessimiste.

Il est important de remarquer que les résultats obtenus pour l'estimation de la durée de vie, pour les prédictions de fiabilité et l'estimation de la redondance sont fortement dépendants des hypothèses prises. Une limite supérieure de $T_j = 90°C$ a été fixée pour les semiconducteurs, pour avoir des conditions d'opération réalistes pour un MMC dans une application HVDC. Si la limite de T_j est fixée à des valeurs supérieures, les résultats seront plus pessimistes.



(a) (b)

Figure A.29. (a) Nombre de SMs total au cours de la période de service, (b) Comparaison du nombre de SMs total dans les différents cas d'étude

A.6.5. Chapitre 4 : Test de cyclage actif

Il est nécessaire de valider les méthodologies développées dans le chapitre trois. Ainsi, un moyen expérimental pour imposer des conditions de cyclage thermique s'avère pertinent. De plus, il permettra d'activer les principaux mécanismes de défaillance des IGBT, de vérifier l'évolution des paramètres sensibles à la dégradation et de valider les modèles de durée de vie vus dans la littérature.

Dans cette thèse il a été choisi de réaliser des protocoles de cyclage actif. Dans ce type de cyclage, les semiconducteurs sont la source de l'échauffement pour réaliser les essais de fiabilité [239]. Il y a deux types de méthodes de cyclage actif, le cyclage DC et le cyclage AC. La Table A.2 fait une comparaison entre les deux méthodes.

Critère	Cyclage DC	Cyclage AC
Type de pertes	Conduction	Conduction et commutation
Coût	Faible	Elevé
Complexité	Faible (Modérée)	Grande
Paramètres de contrôle	I, t_{on}, V_{GE} (V_{DC})	I, t_{on}, V_{GE}, V_{DC}, V_{out}, f_{out}, f_{sw}, PF
Avantages	- Simplicité en opération et surveillance des paramètres - Possible de tester plusieurs DUTs	- Le DUT est soumis a des conditions réalistes de cyclage - Plus de variété sur les conditions des tests
Inconvénients	- Conditions non-réalistes de cyclage - Besoin de courants élevés - Limitation sur les conditions des tests	- Operation et surveillance complexes - Solution onéreuse

Table A.2 Comparaison méthodes de cyclage actif [249]

Finalement, il a été choisi de développer un banc de cyclage AC, puisque les conditions de vieillissement sont plus réalistes dans ce type de protocole.

A.6.5.1. Banc de cyclage

La topologie standard des bancs de cyclage AC consiste en un pont en H et une charge inductive. Cependant, le banc développé pour cette thèse, compte plusieurs éléments additionnels pour la surveillance et la sécurité du banc. Un schéma des éléments d'un convertisseur est présenté dans la Figure A.30. La maquette complète est constituée de cinq convertisseurs identiques (cf. Figure A.31).

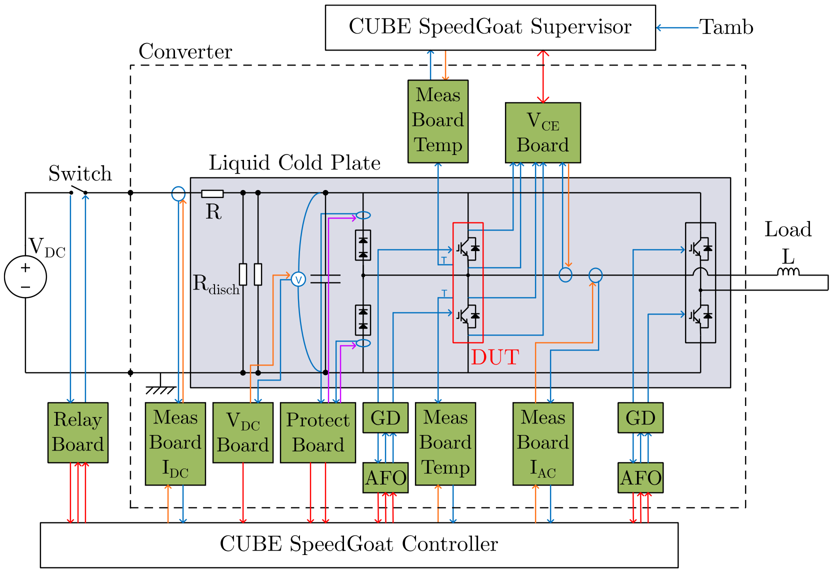


Figure A.30. Schéma des éléments d'un convertisseur pour le cyclage AC

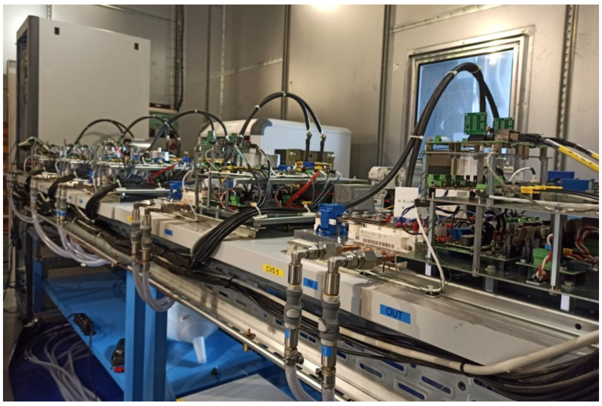


Figure A.31. Banc de cyclage AC

Un des bras du pont en H sera l'élément de test appelé « Device Under Test » (DUT). L'autre bras servira à réguler le courant nécessaire pour imposer les conditions de cyclage souhaitées. Le principe du contrôle du banc est montré dans la Figure A.32. La tension du DUT sera imposée en boucle ouverte, tandis que l'asservissement en courant se fera en boucle fermée. L'amplitude du courant, la fréquence du courant, et le facteur de puissance permettront de contrôler les conditions de cyclage thermique. Il est important de remarquer qu'en imposant des courants avec une fréquence fondamentale basse (ex. 0.5 Hz), il sera possible d'avoir des cycles thermiques rapides (de l'ordre de quelques secondes).

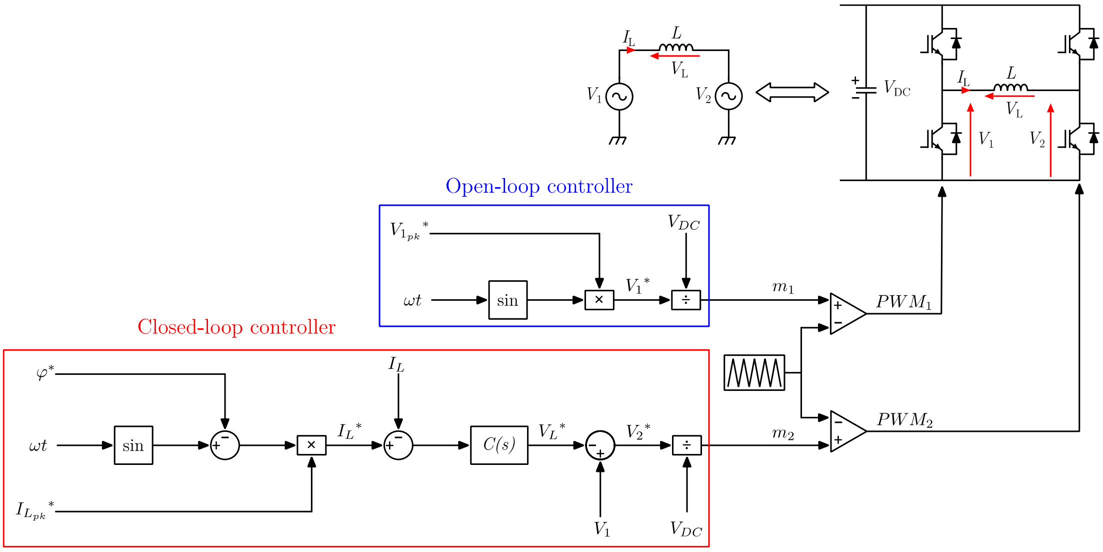
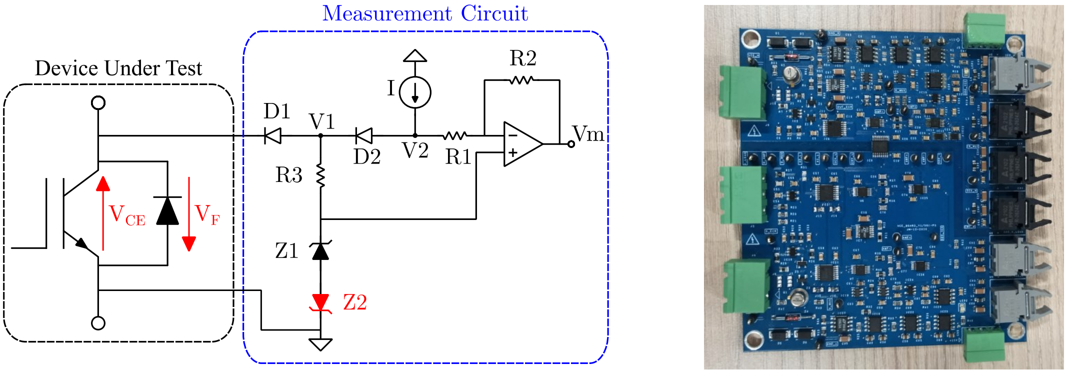


Figure A.32. Stratégie de contrôle d'un convertisseur

Deux machines Speedgoat sont utilisées pour le fonctionnement du banc. Une machine est utilisée pour le contrôle du banc et l'autre est chargée de sa surveillance. Plusieurs cartes électroniques ont été développées pour le fonctionnement du banc. Cependant la carte qui permettra la surveillance de l'état de santé du DUT est la carte « V_{CE} board ».

A.6.5.2. Mesure du V_{CE}, carte V_{CE} board

Le principe de mesure de V_{CE} a été déjà présenté dans [292], et une amélioration à ce circuit a été présentée en [294]. Le circuit développé dans cette thèse a les avantages des deux circuits précédents : mesure des tensions négatives pour la surveillance des diodes et temps de réponse rapide pour surveiller des éléments à large bande interdite. Un schéma du circuit de mesure et la carte finale sont montrés dans la Figure A.33.



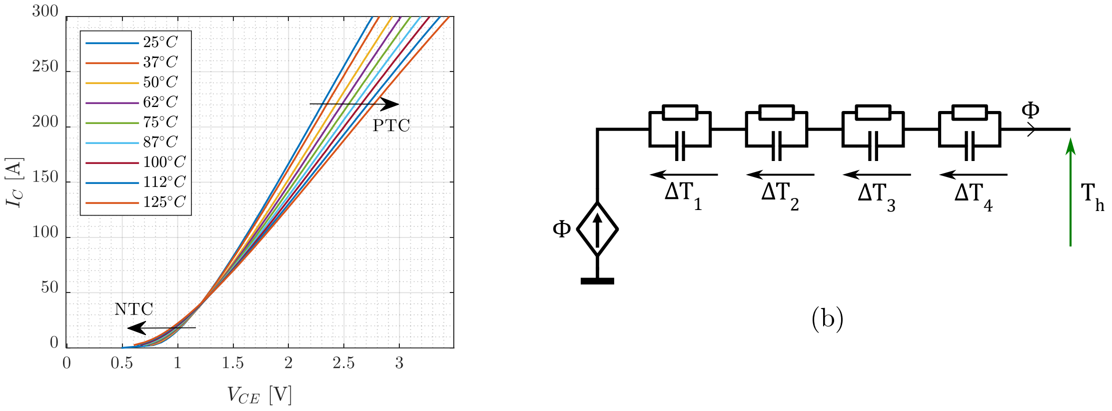
(a) (b)

Figure A.33. Carte V_{CE} : (a) Circuit de mesure, (b) Réalisation finale de la carte

A.6.5.3. Estimation de la temperature de jonction T_j

Dans ce travail, un filtre de Kalman a été proposé pour faire l'estimation de la température de jonction. Le filtre de Kalman combinera l'information d'une estimation préliminaire de T_j avec l'information d'un modèle thermique représenté par un réseau Foster. L'estimation préliminaire de T_j est obtenue à partir des mesures de V_{CE} et de I_C.

Un exemple des courbes pour l'estimation préliminaire de T_j est présenté dans la Figure A.34 (a). Également, dans la Figure A.34 (b) le réseau Foster utilisé pour la modélisation de l'impédance thermique entre la jonction de l'IGBT et la semelle du pack.



(a) (b)

Figure A.34. (a) Courbes pour l'estimation de T_j, (b) Réseau Foster pour la modélisation de l'impédance thermique

Par ailleurs, la méthode « Autocovariance Least-Squares » (ALS), a été utilisée dans cette thèse pour améliorer les performances du filtre de Kalman. Cette méthode sert à identifier les matrices de covariance du bruit Q et R du système. La performance du filtre est fortement dépendante de ces paramètres, parce qu'ils interviennent dans le calcul du gain de Kalman K_f, comme exprimé dans les Eqs. (A.55)-(A.56).

$$P_{k|k-1} = A_d P_{k-1|k-1} {A_d}^T + Q \tag{A.55}$$

$$K_f = P_{k|k-1} {C_d}^T \left(C_d P_{k|k-1} {C_d}^T + R \right)^{-1} \tag{A.56}$$

Dans lesquels :

- $P_{k|k-1} \in \mathbb{R}^{4\times4}$: Matrice de covariance de l'erreur d'état à priori $e_k = x_k - \hat{x}_{k|k-1}$
- $P_{k-1|k-1} \in \mathbb{R}^{4\times4}$: Matrice de covariance de l'erreur d'état corrigée de l'itération précédente
- $A_d \in \mathbb{R}^{4\times4}$: Matrice d'état du système
- $C_d \in \mathbb{R}^{1\times4}$: Matrice de sortie du système
- $Q \in \mathbb{R}^{4\times4}$: Matrice de covariance du bruit du process
- $R \in \mathbb{R}^{1\times1}$: Matrice de covariance du bruit de mesure

La méthode ALS consiste donc à construire une matrice d'autocovariance à partir des résidus ε d'un filtre paramétré avec un gain non-optimal L et du calcul de l'espérance mathématique des résidus avec une version retardée d'eux-mêmes. Le calcul des coefficients de la matrice d'autocovariance est montré dans l'Eq. (A.57) et la construction de la matrice d'autocovariance $\mathcal{R}(N)$ est présentée dans l'Eq. (A.58).

$$\mathcal{C}_{(j)} = \frac{1}{N_d - j} \sum_{i=1}^{N_d - j} \varepsilon_i \, {\varepsilon_{i+j}}^T \tag{A.57}$$

$$\mathcal{R}(N) = \begin{bmatrix} \mathcal{C}_0 & \cdots & \mathcal{C}_{N-1} \\ \vdots & \ddots & \vdots \\ {\mathcal{C}_{N-1}}^T & \cdots & \mathcal{C}_0 \end{bmatrix} \tag{A.58}$$

Dans lesquels :

- j : Nombre d'itérations retardées à considérer
- N_d : longueur du vecteur des résidus
- N : Nombre maximal des retards à évaluer

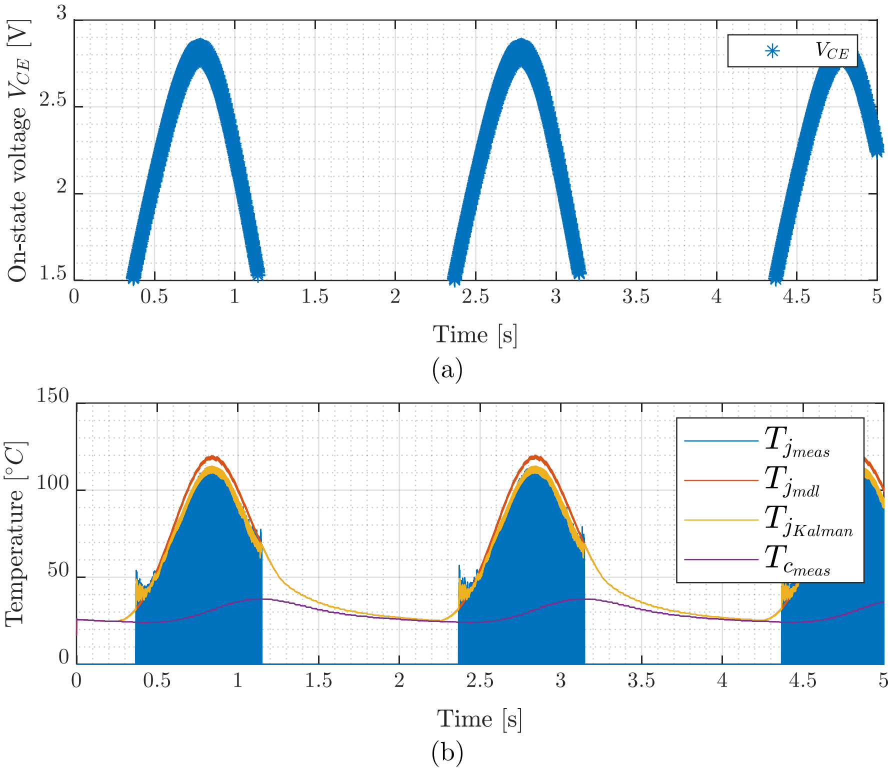
Après avoir obtenu la matrice d'autocovariance, il est possible d'obtenir des estimations $\hat{Q}$ et $\hat{R}$ en calculant la solution du système exprimé dans l'Eq. (A.59).

$$M\theta = b \tag{A.59}$$

Où θ est la forme vectorisée et concaténée dans un vecteur colonne des matrices $\hat{Q}$ et $\hat{R}$. Le paramètre b est la forme vectorisée de la matrice d'autocovariance $\mathcal{R}(N)$. La construction de la matrice M est réalisée à partir des caractéristiques du système d'état comme indiqué dans l'annexe A.5.

A.6.5.4. Résultats et évaluation de la dégradation

Les mesures de tension avec la carte V_{CE} sont présentées dans la Figure A.35 (a). Les résultats de l'estimation de T_j sont observés dans la Figure A.35 (b). Il est important de remarquer que les estimations de T_j ont été validées avec l'aide des capteurs de mesure de température par fibre optique.



(a)

(b)

Figure A.35. (a) Mesures de V_{CE}, (b) Estimations de T_j

Une fois les mesures de V_{CE} et les estimations de T_j disponibles, il est possible de calculer à partir de ces informations, le processus de dégradation du DUT en faisant un suivi de ces paramètres. De plus, un troisième paramètre a été proposé pour avoir une vision plus complète de la dégradation du module. Il s'agit du ratio entre la variation de température issue du filtre de Kalman et celle issue du modèle du réseau Foster. Ce ratio permet d'obtenir une estimation de la résistance thermique entre la jonction et la semelle. Les résultats sont présentés dans la Figure A.36.

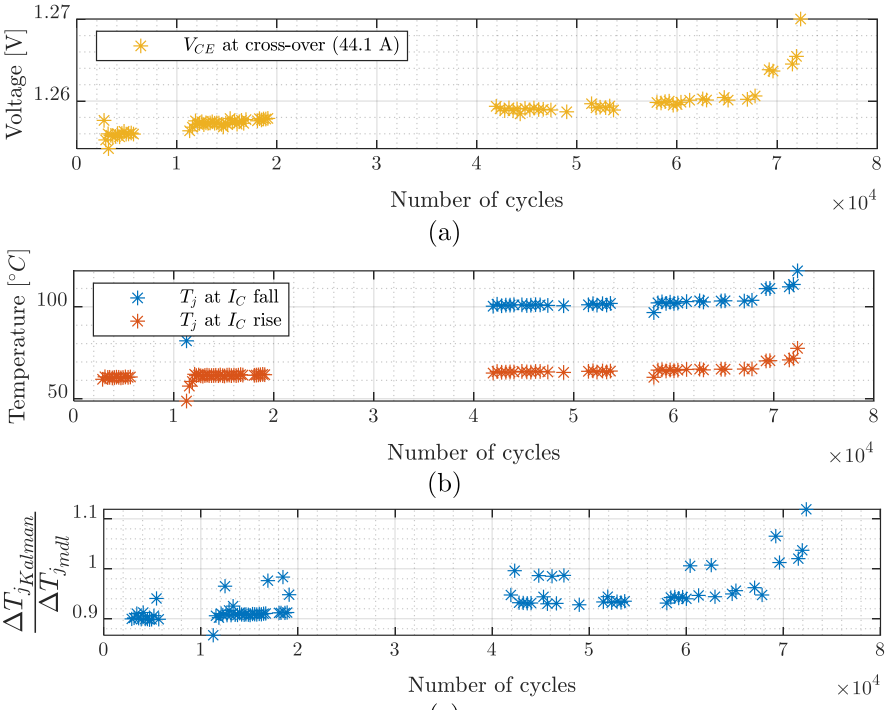


Figure A.36. Evolution des paramètres sensibles à la dégradation

Il y a eu un problème avec le système d'acquisition entre les vingt millièmes et quarante millièmes cycles thermiques. Cependant, durant cette phase, les paramètres suivent une évolution très lente, alors qu'autour de 70000 cycles ils présentent des variations importantes. Après inspection du module vieilli, il a été constaté que les fils de bonding se sont détachés des pads de puissance (cf. Figure A.37).

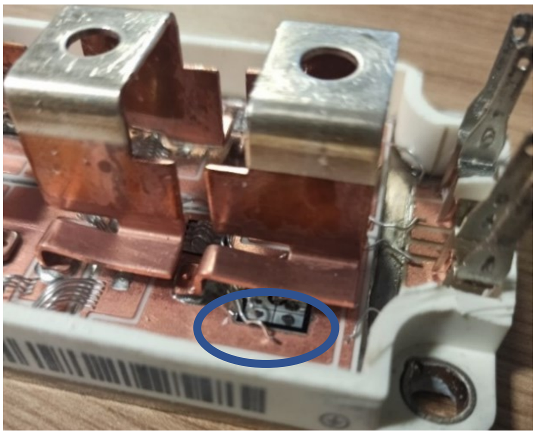


Figure A.37. Analyse post-mortem du module

En raison du manque de temps, il n'a pas été possible de faire plus de tests de cyclage. Il a toutefois été constaté aussi que le temps de casse avec le banc de vieillissement est différent du résultat attendu en utilisant la loi de Bayerer. C'est pour cette raison qu'il faudra réaliser plusieurs tests de cyclage pour faire des analyses statistiques et paramétrer une loi de vieillissement adéquate pour les modules testés avec la méthode de cyclage AC.

A.6.6. Conclusions

Les systèmes HVDC ont des besoins très exigeants en termes de fiabilité et disponibilité. Le convertisseur MMC est une brique fondamentale des systèmes HVDC. Aussi des stratégies pour l'amélioration de la fiabilité/disponibilité du convertisseur ont été abordées. Ce travail s'est intéressé notamment à l'étude de la fiabilité des IGBT présents dans les SMs du convertisseur MMC.

Dans le chapitre 1, les technologies des modules IGBT pertinentes pour des applications HVDC ont été citées. La technologie « flat-pack » a été choisie comme sujet d'étude pour cette thèse, car cette technologie est la plus utilisée dans les convertisseurs MMC actuellement. Dans ce chapitre, une revue des mécanismes de défaillance de ce type de module a été réalisée. Par ailleurs, un état de l'art des techniques pour la surveillance de l'état de santé et pour la prédiction de la durée de vie restante des IGBT a été effectué.

Pour analyser la dégradation des IGBT dans le contexte d'une application HVDC, il a été nécessaire de modéliser le convertisseur. Cette tâche a été effectuée dans le chapitre 2 de cette thèse. Le modèle mixte moyenné-détaillé a permis d'obtenir des formes d'onde caractéristiques d'un convertisseur, et les grandeurs électriques expérimentées par les éléments d'un SM.

Ensuite, avec la connaissance des tensions et courants subis par les semiconducteurs d'un SM, une méthodologie pour l'estimation de la durée de vie a été développée dans le chapitre 3. Cette méthodologie repose sur l'étude du profil thermique des semiconducteurs, puisque les modèles de prédiction de durée de vie se basent principalement sur la notion du cyclage thermique. A l'issue de cette méthodologie pour l'estimation de la durée de vie, une approche pour la prédiction de la fiabilité des SMs et pour le dimensionnement de la redondance d'un demi-bras du convertisseur MMC a été développée.

Ensuite, un moyen expérimental a été conçu pour tester la fiabilité des IGBT dans un contexte permettant de reproduire des mécanismes de défaillance similaires à ceux rencontrés dans des applications réelles. Pour cette raison un banc de cyclage AC a été développé. Il a été nécessaire de développer des moyens physiques et numériques pour le fonctionnement du banc. Un point d'intérêt est celui de la surveillance de l'évolution de l'état de santé du DUT. Aussi, une carte électronique spécialement dédiée à cette tâche a été conçue et développée. Les performances de cette carte ont permis de déployer des méthodes d'estimation de température de jonction et de suivi de la dégradation de l'IGBT. Un autre point d'importance évoqué dans le chapitre 4 a été la méthodologie de l'estimation de la température de jonction. Bien que la technique du filtre de Kalman ait été déjà utilisée dans ce type de contexte, l'utilisation d'un algorithme ALS a permis d'améliorer les performances du filtre de Kalman utilisé, ce qui s'est traduit par des estimations plus précises. Avec, la mesure de la tension V_{CE} et les estimations de la température T_j, il a été possible d'observer l'évolution des paramètres sensibles au vieillissement au cours d'un test de cyclage thermique. Etant donné la différence entre le temps de test attendu et celui vérifié lors de la réalisation du test de cyclage, il s'avère nécessaire de réaliser plusieurs tests pour faire des analyses statistiques et paramétrer des lois de vieillissement. Finalement, il est important de remarquer que le banc réalisé a bien permis d'imposer des conditions de vieillissement accéléré dû au cyclage thermique et constitue donc un outil important dans la perspective du développement de nouvelles méthodes de diagnostic et de pronostic de la durée de vie restante des semiconducteurs.