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Optimal Design Methodology for Static Converters - Application to the Aeronautical Context

Jérémy Bourdon

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Jérémy Bourdon. Optimal Design Methodology for Static Converters - Application to the Aeronautical Context. Electric power. Institut National Polytechnique de Toulouse - INPT, 2018. English. NNT : 2018INPT0020 . tel-04513496

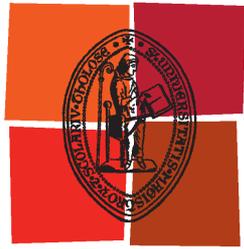
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Université
de Toulouse

THÈSE

En vue de l'obtention du

DOCTORAT DE L'UNIVERSITÉ DE TOULOUSE

Délivré par :

Institut National Polytechnique de Toulouse (Toulouse INP)

Discipline ou spécialité :

Génie Electrique

Présentée et soutenue par :

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le mercredi 23 mai 2018

Titre :

Méthodologie de conception de convertisseurs-statistiques-application à
un contexte aéronautique

École doctorale :

Génie Electrique, Electronique, Télécommunications (GEETS)

Unité de recherche :

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Acknowledgements

Abstract

Nowadays, the electrification of on-board functions on planes is growing inevitably, intensified by the study of new programs such as the More Electric Airplane (MEA). This concept - studied by Airbus - involves both improving the device performance and reliability, and lowering operation and maintenance costs. This growing electrification will significantly reduce gas emissions to meet the new energy and environmental challenges of our society. However, in order to achieve these goals, electrical engineering of aircraft should be dramatically improved. Indeed, design requirements have changed due to new architectures and technological constraints. In this context, power electronics have become a key factor to supply, treat and transport electrical energy with efficiency in our embedded networks and systems. The equipment related to this area will be more affordable, efficient, ecological and integrated in order to create the MEA.

This thesis proposes a new way to design and optimize the power equipment, taking into account the many challenges of the MEA. This is possible thanks to the computer-aided and optimal design, also called virtual prototyping. This new approach in power electronics is a digital revolution in our methods of design and sizing. Indeed, virtual prototyping provides easier and quicker fully optimized systems, while meeting the objectives and specific constraints of an application. This software also dramatically improves the pre-design phase of a converter by simplifying complex decisions on technological compromise, materials, shapes and sizes, as well as internal parameters of a converter - switching frequency filtering, regulation, etc. In other words, the optimal design will become an indispensable step to reach quickly and more effectively new levels of performance. Furthermore, although this approach is driven by the aviation industry, it has to remain flexible enough to be extended to any field of study and any industry.

A full software platform methodology of an electrical engineering optimization is presented in this manuscript. The power component sizes up the complete chain of conversion, while going through related issues such as EMC filtering. This methodology is carried out in particular through the creation of appropriate models of the main power devices of a static converter. A complete ecosystem is also proposed, including communication with time and frequency multi-physics solvers. Finally, we focus on applications related to the development of More Electric Aircraft. Thus, we propose several use examples of this tool, taking into account the needs and constraints of this very demanding environment.

Key-words

Power Electronics, Virtual Prototyping, Optimal Design, Optimization, Isolated DC/DC power converter, Multilevel converters, Wide Band-gap, SiC, GaN, More electric aircraft, Power converter sizing, Filter sizing, EMC

Résumé

L'électrification croissante des fonctions à bord des avions est inévitable et s'intensifie avec l'étude de nouveaux programmes tel que l'Avion Plus Electrique (MEA). Ce concept étudié par Airbus implique l'amélioration de la performance des appareils et de leur fiabilité, ainsi que la diminution des frais d'opération et de maintenance. Il permettra de réduire considérablement les émissions de gaz afin de répondre aux nouveaux défis énergétiques et écologiques de notre société. Cependant, pour atteindre ces objectifs, l'état de l'art en génie électrique doit être amélioré. En effet les exigences en terme de conception ont changé, en raison des nouvelles architectures et contraintes technologiques. Dans ce contexte, l'électronique de puissance est devenu un facteur clé pour alimenter, traiter et transporter l'énergie électrique avec efficacité dans nos réseaux et systèmes embarqués. Les équipements relatifs à ce domaine devront donc être plus abordables, performants, écologiques et intégrés afin d'aboutir à la création du MEA.

Pour y parvenir, le but de cette thèse est de proposer une nouvelle façon de concevoir et d'optimiser ces équipements de puissance, tout en prenant en compte les nombreux défis du MEA. Cela est possible grâce à la conception optimale informatisée, aussi appelée prototypage virtuel. Cette nouvelle approche en électronique de puissance promet une révolution numérique de nos méthodes de conception et de dimensionnement. En effet, le prototypage virtuel fournira plus facilement et rapidement des systèmes entièrement optimisés, tout en répondant aux objectifs et aux contraintes spécifiques d'une application. Ces logiciels permettront aussi d'améliorer drastiquement la phase de pré-dimensionnement d'un convertisseur en simplifiant la prise de décisions complexes sur des compromis technologiques, de matériaux, formes et dimensions, ainsi que de paramètres internes à l'utilisation d'un convertisseur - fréquence de découpage, filtrage, régulation, etc. En d'autres termes, la conception optimale deviendra une étape indispensable pour atteindre plus efficacement et rapidement de nouveaux niveaux de performances. De plus, bien que cette approche soit poussée par le milieu aéronautique, elle reste suffisamment flexible pour être étendue à n'importe quel domaine d'étude et d'industrie.

Une méthodologie complète de plate-forme logicielle d'optimisation en génie électrique est présentée dans ce manuscrit, du dimensionnement du composant de puissance jusqu'à la chaîne complète de conversion, tout en passant par des problématiques connexes tel que le filtrage CEM. Cette méthodologie est réalisée notamment grâce à la création de modèles adaptés des principaux dispositifs de puissance présents à l'intérieur d'un convertisseur statique. Un écosystème complet est aussi proposé, comprenant la communication avec des solveurs multi-physiques temporels et fréquentiels. Finalement, nous nous concentrons sur des applications relatives au développement de l'avion plus électrique. Ainsi, nous proposons plusieurs exemples d'utilisation de cet outil, prenant en compte les besoins et contraintes de ce milieu très exigeant.

Mots-clés : *Electronique de Puissance, Prototypage Virtuel, Conception Optimale, Optimisation, Convertisseur isolé DC/DC, multiniveaux, semi-conducteurs grand gap, SiC, GaN, Avion Plus Electrique, Dimensionnement, Filtres, CEM*

ETHAER Project

Advanced power electronic for aeronautical applications

The ETHAER project is at the border of basic research and applied research. It addresses the field of Power Electronics within the frame of the more electrical aircraft that has generated many research over the past five years. The specific aim of this project is to help defining the power electronic converters for the next generation of airplanes (2015-2020). With this aim in view, the project focuses on the interconnection of the LV and HV networks (resp. 28 and 540V) which is definitely a very demanding function. This project includes technological aspects that require experimental check and must be pushed up to the full prototype stage. However, more theoretical aspects aiming at the design and optimisation are also included; dedicated tools aiding the design and the technological choices to be made in order to build the power systems for future aircrafts will also be developed.

Electronique de puissance à Très Hautes performances pour l'AERonautique

Le projet ETHAER se situe à l'interface recherche amont/recherche industrielle. Il relève du domaine de l'Electronique de puissance et se situe dans le contexte applicatif de l'avion plus électrique sur lequel se focalisent de nombreuses recherches depuis 5 ans. Il a pour ambition de contribuer à la définition de convertisseurs de puissance électroniques pour les avions de future génération (2015-2025). Pour atteindre cet objectif global, le projet se focalise sur une fonction électrique particulière très contraignante, l'interconnexion réversible et isolée entre les réseaux de bord 28V et +/-270V, ces derniers étant d'ores et déjà définis. Il contient donc un important volet expérimental et technologique qui doit déboucher sur la réalisation de démonstrateurs. Mais il va plus loin, en visant la synthèse de méthodes de conception/optimisation, la construction d'outils associés et la définition de technologies d'intégration susceptibles d'être exploitées dans les autres fonctions de conversion électriques qui vont se multiplier dans les aéronefs.

Partners/Partenaires

- AIRBUS OPERATIONS SAS
- IES INSTITUT D'ELECTRONIQUE DU SUD
- AMPERE LABORATOIRE AMPERE
- GEEPS GENIE ELECTRIQUE ET ELECTRONIQUE DE PARIS
- LAPLACE LABORATOIRE PLASMA ET CONVERSION D'ENERGIE

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List of Abbreviations

AC	Alternating Current
A/C	Aircraft
ATA	Air Transport Association
BBCU	Buck Boost Converter Unit
CAD	Computer-Aided Design
DBC	Direct-Bonded Copper
DC	Direct Current
DF	Dissipation Factor
EMC	Electro Magnetic Compatibility
EMI	Electro Magnetic Interference
FEM	Finite Element Method
FOM	Figure of Merit
HV	High Voltage
LV	Low Voltage
MEA	More Electrical Aircraft
OOP	Object-oriented Programming
PCB	Print Circuit Board
SC	Semiconductor
UI	User Interface

Chapter 1

1. Introduction

Power electronics is a scientific and technical discipline whose purpose is to convert the electric power from one form to another. As a computer processes information, a power electronics equipment processes power (Figure 1). To realize this conversion, we design static converters which are connected to their sources and must provide processed and suitable electrical power according to demanding specifications and be immune to perturbations like EMC or heat stress. Today the most common approach of designing a converter remains the use of pre-studies with more or less assumptions, the design experience or even the method of “trial-error”. However, more and more design tools are available on the market to minimize the conception cycles before getting a final functional product. Yet, no current tools or methods give directly a design accurate enough to define the best topologies, technologies or ideal sizing of components. In addition, this optimization practice has been used for many years in other areas such as mechanics, with for instance the design of the aircraft structures [1] [2], and is called "preliminary design" or “computer-aided optimal design”. Consequently, this thesis aims to propose a methodology to perform a similar task in the field of power electronics. Then, this optimal design approach will be used on a challenging application dedicated to new embedded aeronautical converter, like the BBCU. This converter is a centrepiece of the electrical architecture of a future commercial aircraft, called the More Electrical Aircraft.

In this introductory chapter, the context of this study and the problematic of the computer-aided optimal design are developed. First of all, the “More Electrical Aircraft” concept and the implementation of power electronics in commercial aircraft will be exposed, leading to the creation of new converters that require to be optimized, especially from preliminary studies. Then, we will explain the objectives and expectations of the assisted design used to optimize any kind of power converter. Finally, and before revealing the axes of research developed all along this thesis, figure of improvements in power electronics through the optimal design will be introduced.

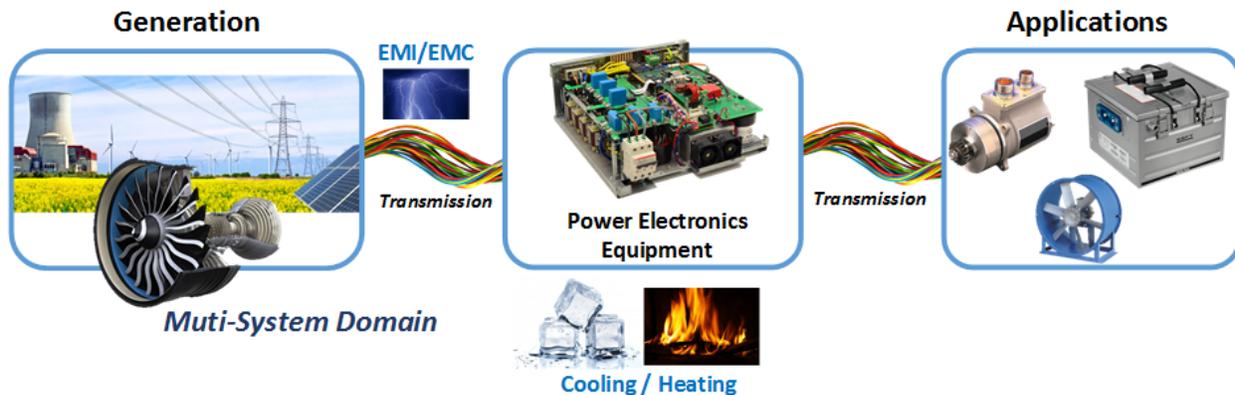


Figure 1: Power electronics principle schematic

1.1. The More Electrical Aircraft (MEA)

1.1.1. Review of the MEA

In the last decades, some important steps have already been achieved towards a more electrical airplane, particularly with the increasing role of the electrical energy in aviation board networks. At the beginning, its use was limited to navigation and flight instruments, and then it was gradually increase to improve the comfort and In-Flight Entertainment (lighting, kitchen, video equipment). New applications have emerged to optimize the aircraft operation, such as power management of the flight controls on the Airbus A320 in the 1980s (Fly-by-wire). The development of the Airbus A380 was a further step of innovation in electrical technologies: free AC grid frequency (360-800Hz), electrical emergency system, new electro-hydraulic actuators for flight controls and Solid State Power Controllers for low current ratings.

Nowadays, the More Electrical Aircraft (MEA) concept offers high potential for future air transport and is one step towards more efficient planes. Four secondary vectors of energy dedicated to the system servitudes are used on aircraft and are mainly obtained from propulsion engines: mechanical, hydraulic, electrical and pneumatic energy. The MEA aims to replace hydraulic and pneumatic systems by electrical ones, called respectively “Hydraulicless “or “Bleedless” architectures [3] [4], reducing overall system weight and offering an easier maintenance. Moreover, these new architectures imply new propulsion engines that improved the overall efficiency and the implementation of new desirable characteristics of electrical systems, and so increases their number. Indeed, the “MEA” label relates to the potential improvement that could offer electrical systems compared to the other energy forms. In fact, conventional solutions are already optimized and do not indicate significant changes in a close future. Therefore, many technological, industrial, functional and structural improvements are expected for the equipment. As it is connected to electrical networks, the term “Power-by-wire” is then used. Because of all these changes, the global electrical power of the aircraft is continuously increasing (Figure 2).

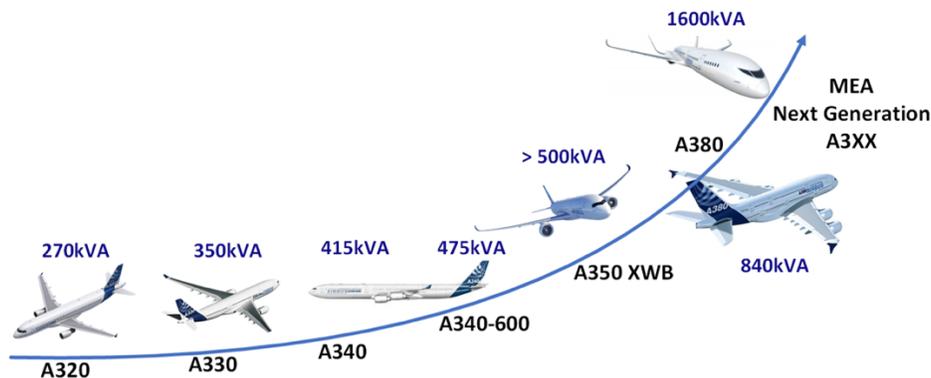


Figure 2: Electrical generation capacity installed on Airbus A/Cs

For the next generation of Airbus aircraft (Boeing has already used electrical concepts in the 787 [5]), other functions may be performed electrically, such as wheel braking, air conditioning and engine start (Figure 3). Some examples of characteristics of the electrical systems can be exposed:

- **Controllability** implying the power on demand
- **Re-configurability**, maintaining the functionality during faults
- **Advanced diagnostics** and prognostics, which is a more intelligent maintenance to increase the aircraft availability
- **Homogeneous interface** between the different components: electrical, power electronics, electronics types
- Easier replacement of the systems

Moreover, simulations should be more efficient to study the design optimization and get more facts and knowledge for engineering design. In addition, the change to more electrification covering both the aerospace and automotive industries [6] [7], should lead to an equipment standardization, which will reduce the assembly cost and time. The aircraft manufacturing is also facilitated by the greater flexibility of the electrical installation compared to the hydraulic and pneumatic systems. For instance, the installation of pipes and ducts is more restrictive and electrical wiring brings additional degrees of freedom. In a few words, this technical rupture will enhance the aircraft design, whose main purpose is to reduce dramatically the total aircraft weight in order to reduce fuel consumption, operating costs and environmental impact. However, it requires an advanced work on the different electrical and power electronics systems, which are present everywhere in the aircraft.

1.1.2. Power Electronics Integration

In order to better understand the impact of power electronics in the MEA, it is important to present systems powered and/or controlled by those means. Indeed, current and future developments of electrical architectures are necessarily linked to the development of power electronics applications (Figure 3). In the latest generation of commercial aircraft, the presence of static converters in the network was limited to a reduced amount of systems: food commercial expenses (galleys), rectifiers (115V-400Hz/28V) and emergency inverters (28V/115V-400Hz). With the energy management evolution in the MEA and the increasing power demand, the number of classical AC/DC and DC/AC converters have increased. In other words, power electronics have been identified as a key success factor for the future aircraft generation, and conquer more various systems of the aircraft. These systems are classified in ATA or Air Transport Association [8], a common referencing standard for all commercial aircraft, detailing the different systems of the aircraft. The ATA impacted are listed in Table 1. More information about embedded systems and ATA's using power electronics can be found in [9] [10] [11]. In the context of this thesis, we focused on the ATA 24, i.e. the electrical power generation and distribution, with the emergence of a HDVC network [12] [3] in the aircraft due to the new MEA architecture.

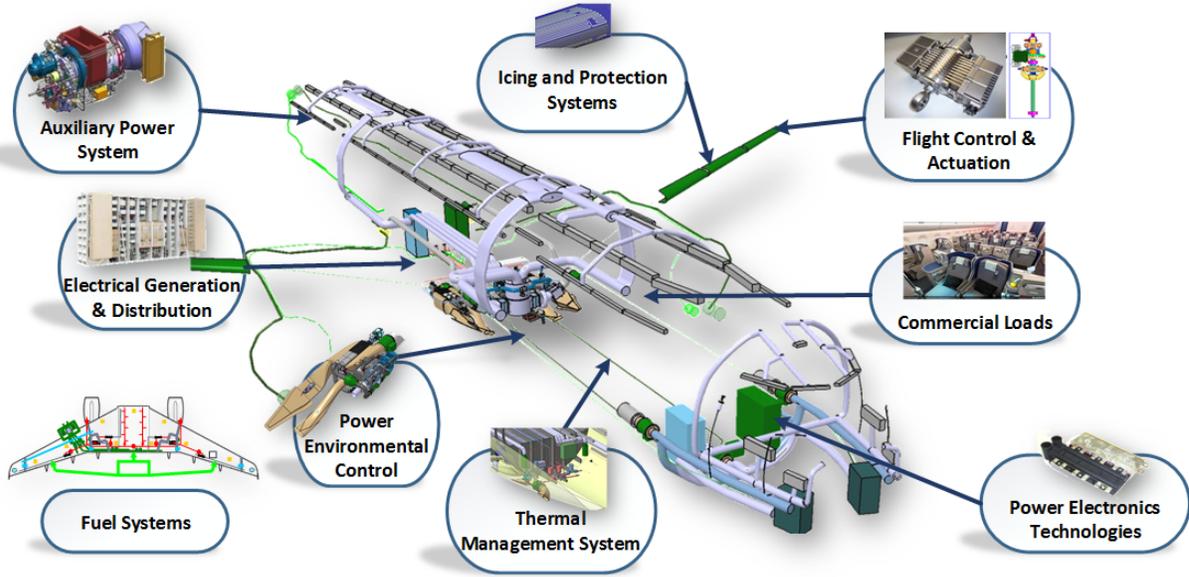


Figure 3: Opportunities of Power Electronics on Systems

	Definition	Example
ATA 21	Air conditioning & pressurization system	Fans supplied with high power until 9.8 kVA
ATA 24	Electrical Power Generation and Distribution	Variable Frequency Generator (VFG), Solid-State Power Control (SSPC), new HVDC network
ATA 27	Flight Control system	Increase of electrical systems, electrical actuators
ATA 28	Fuel system	Supply by power converters on free frequency networks
ATA 29	Hydraulic System	Each hydraulic circuit includes an electrical pump
ATA 32	Landing Gear Systems	Actuators for the extension, retraction and orientation of systems, doors, the front wheel etc.
ATA 78	Thrust reversers	Require high power for a short time through an all-electric system (until 25kVA).

Table 1: Examples of power electronics use within different A/C systems

1.1.3. Impact of the new HVDC network

As discussed in previous sections, the number of loads and electrical equipment in commercial aircraft is increasing exponentially. One of the possible answers to this problematic is the creation of an ‘HVDC network’ [12]. For Airbus, ‘HVDC network’ means a DC network composed of two rails with potentials equal to respectively +270V and -270V, the reference of potential being the plane structure. Indeed, it allows to not integrate many AC/DC rectifiers as currently done on aircraft embedding an AC network. It obviously implies a significant gain in the global weight of electrical systems [13]. The ‘Bleedless’ architecture represented in Figure 4 is one of the propositions offering new electrical energy management in the aircraft, including an HVDC network and other

innovations [3]. This network requires the creation of numerous new power converters, and among them one that links the HVDC 540V network to the LVDC (or DC) 28V network. It is the Buck Boost Converter Unit or BBCU, one study case of this thesis introduced in Chapter 5.

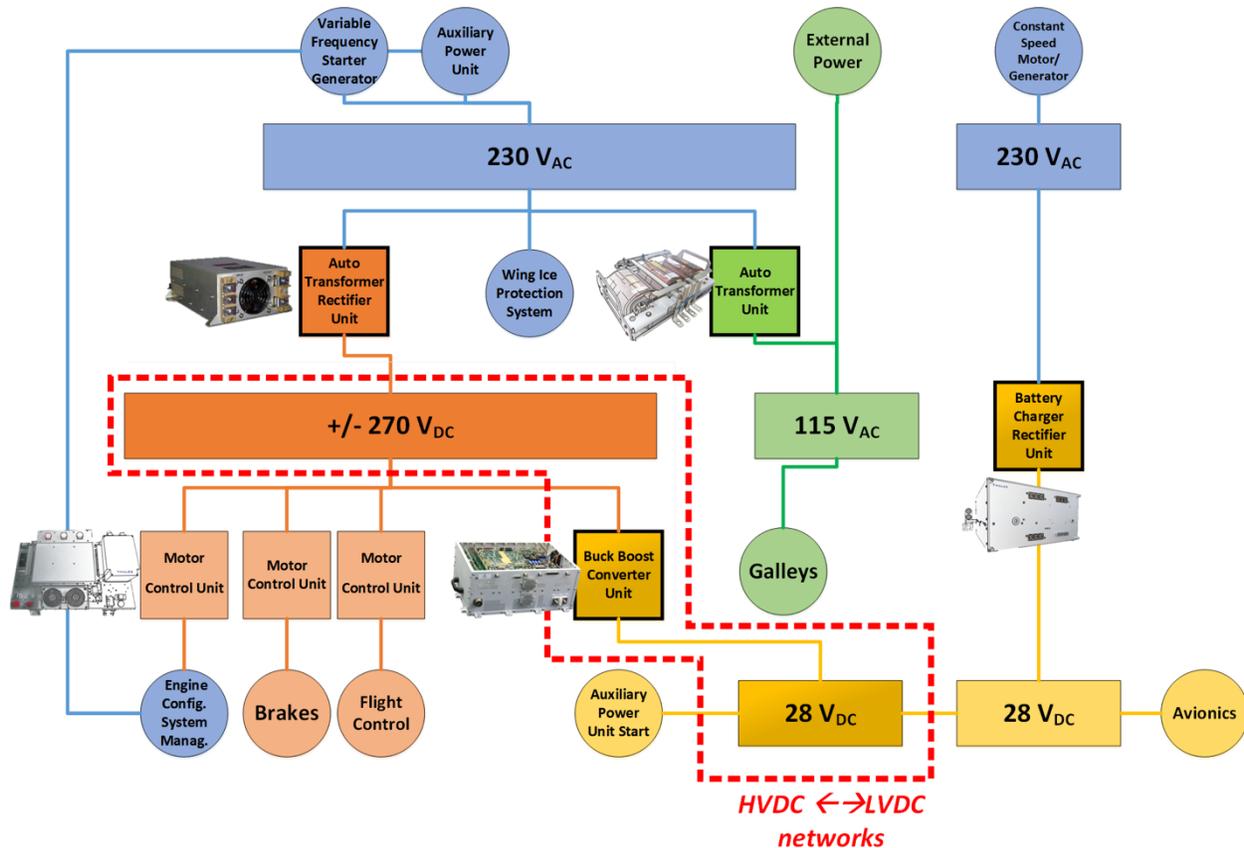


Figure 4: Example of a Bleedless architecture with the implementation of the BBCU functions [14]

However, there are high expectations on the converter power density and efficiency because of the ambition to board them in the MEA (**Erreur ! Nous n'avons pas trouvé la source du renvoi.**). Therefore, a new approach is proposed in this thesis in order to optimize the converter design and sizing. Indeed, a new methodology in power electronics is used here: the computer-aided and optimal design of static converters, also called virtual prototyping. As a conclusion, beyond the HVDC requirements in the MEA, the power converters will have to reach new level of integration and efficiency in order to be compliant with the new expectations, efficiency and higher constraints. Thus, a new global problematic arises in the power electronics field in order to design the most appropriate converters: how to define the best and more appropriate technologies and get the optimal sizing of each component related to a specific application? This optimal design can only be reached thanks the help of computational tools and optimization routines, which is generally referred to as computer-aided design and optimal design.

1.2. Computer-aided design in Power Electronics

To face these new challenges, specific tools allowing a more efficient and faster design of power converters are needed and this requires working at two different levels;

- **Component-level multi-physic models** describing the different interactions between the components of a converter that all need to be taken into account in the design process. This includes electrical, thermal, magnetics, and fluid mechanics models. Concerning the electrical model, it should be noted that the losses in each component, though very small compared to the total power flowing through the converter, have a critical influence on design trade-offs and on the performances of the converter. These losses are generally governed by second order phenomena involving complicated physics; (physics ruling conduction and switching losses in semiconductors, physics ruling core losses in magnetic cores, physics ruling AC current distribution and losses in conductors...). Easier but important as well, weight models are also needed since the weight of the converter is important to the user.
- **Converter-level formulation and tools** to describe the interactions between the components (solver, or solvers for the different physics), the evolution of performances (weight, efficiency...) as a function of design parameters (converter topology, and components values, dimensions, materials or shape...). The trade-offs between performances result of complex interactions between many design parameters (including continuous and discrete variables) and the problems is generally complex enough to give many different local minima. As a consequence, optimization routines are generally needed to address such a problem, and convergence depends widely on the problem formulation and type of algorithm used.

The purpose of this section is to provide definitions and identify the new expectations of the computer-aided optimal design. The aim is to get in a minimum of time a solution that matches all requirements and is close to the best design. It is generally very difficult to guarantee that a global optimum is reached, so although optimization routines are used, it would be better to speak of automated design than optimal design. In future work, a first step would be to switch to algorithm providing boundaries of the objective function in subsets of the design space, which allows deriving an upper bound of the difference between the current objective function and its absolute minimum.

The aim of the present work is to build models and establish formulations giving at least a solution matching all requirements, the requirements being in the way that is most convenient to the designer

Previous studies have been realized on individual components in the Laplace laboratory:

- Optimization of magnetics components [15]
- Design of a DC-DC converter with a succession of local optimizations on the different parts of the converter [16].

These works are used as a basis of this thesis, but they never considered a strategy to create a direct optimization of a global converter, including EMI studies. Thus, the methods have been thoroughly reconsidered.

1.2.1. New expectations in Power Electronics

First of all, we need to identify the new expectations on power electronics systems, as demonstrated in [17]. They are used in a wide range of applications, such as industry automation, processes, communication, transportation and lighting. The current static converters are quite mature and design criteria include cost reductions or improved reliability. In order to measure these needs, numerous **performance indices** (Figure 5) are often stated:

- Power density [kW/dm³]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/\$] or [kW/€]
- Relative losses [%]
- Failure Rate [h⁻¹]
- Environmental Impact from metal [Kg_{material}/kW] or silicon [cm_{Si}/kW]

It should be noted that the global cost of a converter is generally the criterium that is the most important, but it is also the most difficult to evaluate since it derives from parameters that depend on time, market, customer/retailer agreements, number of items produced, etc... Academic research is likely to produce design tools handling physics-based phenomena and performances, but only industry seems to be able to produce relevant cost models. To this extent collaboration between both worlds is a must.

Moreover, in a converter design we rarely consider only one criteria of improvement. Therefore, trade-offs are needed in order to create the best trade-off thanks to multi-objective optimization (Figure 5).

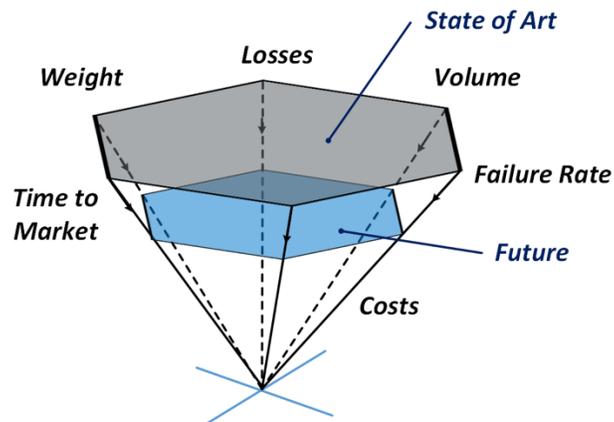


Figure 5: Current and Future Requirements in Power Electronics, extracted from [17]

However, all **Performance Indices** cannot be maximized independently (Figure 6). Therefore, designers need to make choices and if advanced design tools a certain flexibility must be provided to allow guiding the design in a given direction, prioritizing a given set of performances or using a ponderated sum of basic criteria.

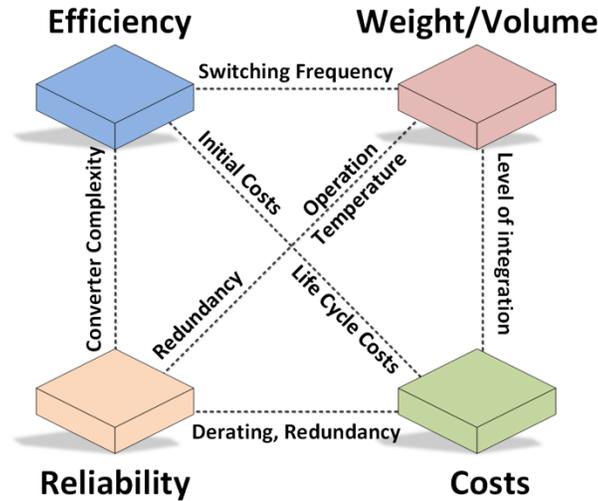


Figure 6: Example of opposite objectives in a power electronic equipment, extracted from [17]

Depending on the field of application, the market to be addressed, or company-specific design rules, different weights of the criteria can be used and quite different solutions can be found (Figure 7). As a conclusion, advanced modelling tools are required to calculate these specific performance profiles quickly and accurately, but also to switch easily from one to another.

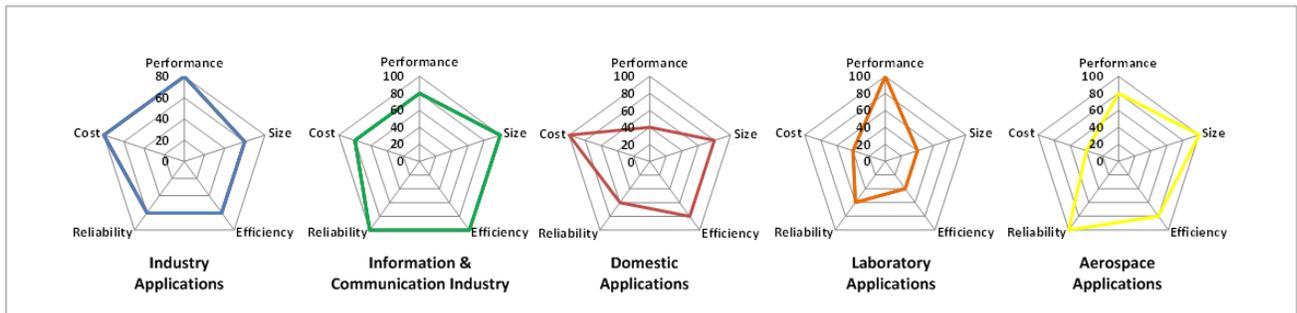


Figure 7: Weight repartition on performance indices as a function of the domain application, extracted from [17]

1.2.2. Digitalization & Virtual Prototyping

In order to meet previous expectations and performances (1.2.1), new tools such as multi-domain modelling and simulation, optimization and virtual prototyping are required. The transition from hardware prototyping to multi-domain modelling, simulation and optimization has started in R&D laboratories [17] and this is sometimes referred to as “Digitalization” (Figure 8).

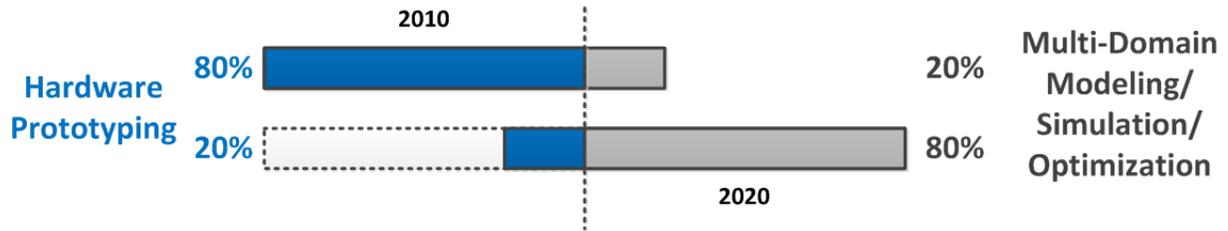


Figure 8: The digitalization transition in power electronics thanks to the virtual prototyping, extracted from [17]

In Power Electronics, this digitalization aims at providing software that can improve the converters corresponding to any type of conversion (DC/DC, DC/AC...). The expected features to be included in the computer-aided tool are:

Design Optimizations:

- Advanced Simulations that allow multi-objective optimization and identify performance limits results, such as “Pareto Fronts “or comparisons. The multiple objectives have to be easily switchable (optimization of different goals) and tuneable if weight are applied on them (each objective has a definite weight).
- Detailed component sizing in terms of shape, dimensions, material, etc. and their operation parameters (frequency, temperature, duty cycle)
- Trade-off Analysis by successive optimizations, with a variation of study parameter like topologies, technologies and key parameters or even sensitivity studies to evaluate the technology advancements and understand possible mutual dependencies of performances
 - Solvers and Simulations

Models Library:

- New models creation of power components dedicated to virtual prototyping, covering the wide range of custom and COTS (Components-Off-The-Shelf) devices
- Application of specific solutions, like devices (e.g. PCB, Power Module, Chips)
- Comprehensive modelling and physical phenomena (e.g. Cost, EMI, Reliability)
 - Minimization of the simulation time with new solvers or strategies like model order reduction, simplification and granularity

Posteriori Verification:

- Interactive features with commercial and specialized software, such as post-treatment validation (solvers, FEM (Finite Element Modelling), CAD (Computer-Aided Design) etc.)

From the equipment to systems:

- Ease of integration into systems to extend gradually the spectrum of the equipment design for a more global optimization. For instance, two systems that have been optimized individually, are not necessarily the optimum when put together. Maybe they can lose all of their assets calculated during their sizing once interconnected, because of negative coupled effects?

- Simulation of what cannot (anymore?) be measured in real systems (High Integration Level), e.g. current in a fast switching semiconductor: inserting a current sensor may modify the switching waveforms

Big Data:

- Database management, analysis of this data (devices, tests, issues, quality etc.), obsolescence treatment

Efficiency:

- Low Complexity to keep the tool accessible, and modularity / scalability to make it evolve
- Robustness, quickness and reliability of results
- Accessible UI (User Interface) and tools for any user, processing all the points of this list

From previous expectations, we can now deduce what should be the degree of freedom left to the user (or to the tool?), in order to get a relevant design and realize any sort of project (Figure 9). Thus, a designer could use and compose with these “objects”:

- Devices
- Topologies
- Modulation and Control
- Design Procedure
- Modularization / Standardization / Economy of Scale
- Manufacturing
- New/Custom applications

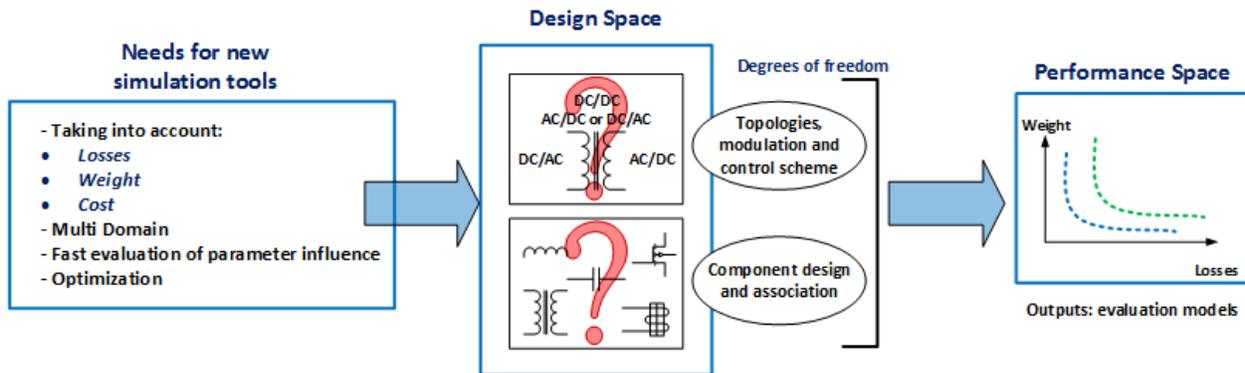


Figure 9: Requirements for new simulation tools in Power Electronics

Due to the digitalization of the design process, some engineering and scientific fields are more and more correlated. For instance, in order to realize multi-objective optimizations, we require some expertise from computer sciences, mathematics and electrical engineering. In addition, numerous domains have to be considered when creating power electronics models, in order to represent the different physics or interesting aspects included in a static converter:

- **Electric**, the most obvious in a power electronics converter, which simulates the waveforms of voltage and current.

- **Magnetic**, in order to simulate an advanced physics inside the magnetic components such as inductors and transformers
- **Thermal**, to evaluate the heat stress imposed to the component to avoid their destruction
- **Mechanical**, to get an idea of a 3D representation and physical parameters such as the weight and volume
- **Fluidic**, especially for the cooling system where constraints such as pressure drop or maximum flow are sizing the converter
- **Economical considerations**, which are definitely outside of physics but at least as complex, should also be included. Some of the complexity here is related to the fact that cost can be different for one player or the other... (quantity-dependant prices) as previously introduced.

As a conclusion, the Pre-Design still has some “Remaining Challenge” ahead and numerous functions to build in order to provide an efficient high-level decision-making tool. It should be a pre-design and multi-domain software realizing high level decisions, in addition of the current specialized software. Its aim should not be to substitute the role of current electrical solvers or dedicated physical software such as FEM. However, bridges between predesign, and design software are considered as mandatory in the future to accelerate the designs. Another important point will be to change the habits of Power Electronics designers; it might take some time for these tools to become mature and be accepted by the industry. We can mention “Gecko” as an example, which is an emergent software suite used as an advanced Power Electronics Design Platform. It includes Modelling & design (circuit simulation, thermal simulation, FEM Simulation) [18]. In addition, the virtual prototyping requires a new way to create models, which will be detailed in this thesis. Indeed, components, systems, topologies and controls are concerned by this modelling and need to be quick to compute, with a control on the assumptions and the inaccuracy they may create.

1.2.3. Pre-design VS Detailed-Design

Once the needs for computer-aided design in power electronics have been exposed, it is interesting to redefine the difference between detailed design and pre-design. In fact, the detailed design is the final design that will be implemented physically in the equipment, in order to perform a specific function. This phase takes into account all the very specific characteristics of each component. However, it is complicated to get these final characteristics directly in the pre-design phase. The subject of this manuscript is the creation of a tool and a method for the pre-design. The tool should do the same work, but it involves simplified models that are much more simple but less accurate. They involve assumptions – more or less strong -, include a description of only the phenomena that are assumed to be predominant. The final pre-design may need different types of post-processing and checks:

- it must match all requirements, at least within the limits of the accuracy of the models. This basic check is inherent in most optimization routines and expressed as a simple output flag.

- The proposed pre-design might not be the optimal design (global minimum of objective function) but it should at least be a “good” design; a strict formulation of “good” design would be that for this design the objective function is for example less than $x\%$ above the global minimum of the objective function. Today we are not able to give such a guarantee, but tools giving such an indication have been identified and they might be used in the future to better evaluate our results. This optimality is also related to the models used to formulate the problem.
- Another type of post processing is to check that the simplified models are still valid in the conditions of the pre-design. This can be done using more sophisticated models at this point only. For example, 3D finite elements simulation can be used to check the losses at the nominal point in a magnetic component that was designed using optimization routine and a much simpler model of magnetic component.

1.2.4. Problematics for sizing a Power Converter

New requirements on the methodology, expected results and functions were presented in the previous part. We can now express in terms of electrical engineering formalism our expectations in resolving an optimal design problem on a power converter. Indeed, the resolution of the design problem must answer to the global and recurrent issues met during a converter sizing. These issues are related to the design (e.g. topology, control) and choice of components (e.g. material, technology) among the whole possibilities, part number and combinations available on the market, where the main ones are defined hereafter. The aim of this approach is to revisit current design methods of power systems. Today manual or local optimizations are realized individually on each component, setting assumptions without knowing the real impact on the global system. On the contrary, the optimal design addresses directly all parameters, components and their combinations in the converter. It leads to the best design by realizing a global trade-off according to one or several objectives. Thus, a global optimum is reached with a well-tuned computational tool. To illustrate this problematic, we have raised open questions. They formulate the different challenges that the optimal design has to solve in order to become an essential design tool for power electronics systems.

- Which material, technology and geometry should be used to create the different components? Increasing the frequency of the passive components implies the use of components suitable for high frequency [19]. However, it is difficult to find large magnetic cores capable of operating at high power/high frequency (tens of kW, tens or hundreds of kHz), most capacitors also have resonance frequencies around 1 MHz and a simple conductor becomes worse when frequency increases because of skin and proximity effects. Furthermore, a more sophisticated technology is used to switch at higher frequency (stray inductance, gate drivers...) and now that power devices are switching so fast, the calculation time of digital controllers can also be responsible for calculation time limitations. The implementation of the commutation cell becomes more complex and of the regulators switching at higher frequency and even the control technique demands for the semiconductors also rise in terms of speed; thus, the integration becomes an inevitable solution to overcome all these problems [20].

- What is the best conversion topology to be used? And should we use the multilevel concept? If so, how many levels should be used?

Nowadays, making a trade-off between several topologies for a same application is still a time-consuming task. Assumptions and simplification are made in order to design a converter and it must be checked that these assumptions are valid in the conditions imposed by final design [21]. Employing multilevel topologies should be explored since it increases the degrees of freedom but it may lead to not so standard conditions and bring unusual design trade-offs [22] [23]. For example, in two-level converter, the trade-off between heatsink and filter weight is governed by switching losses and filter design that depend on the same parameter, the switching frequency; but in multilevel design, the frequency seen by the filters is the switching frequency multiplied by the number of cells and this may change the game. These topologies also allow distributing the voltage and current among several switches and commutation cells. Thus, the use of more efficient semiconductors with reduced sizes is possible, which is in line with a reduction of the size of cooling system and passive components. However, a large number of cells involves more control circuits and therefore a greater complexity of the circuit [24], and it must be checked that voltage and current are respectively balanced between the different series/parallel cells [25].

- How far should the switching frequency to be increased to reduce the overall size of the converter?

Passives components are often the bulkiest components in a converter, and a widespread idea is to increase the switching frequency of the semiconductors to reduce their volume [26]. This is relevant for components such as isolation transformers, DC bus capacitors, and in general internal filters or filters designed for ripple only, but the behaviour can be quite different when a frequency-domain standard with a salient point is the main criteria (typ. at 150kHz...)the behaviour can be quite different [27].

- How to design filters to reach the application standards?

In recent years, the speed of semiconductors has increased, allowing less switching losses thanks to faster switching transitions. However, these faster transitions increase the level of EMC perturbation at high frequency and may put more stress on the EMC filter. In addition, a recent expectation in aeronautics is to relax the current standards so as to reduce the impact of the standard on the global sizing and weight of the systems, and analyse if a better referential exists for our equipment.

- Is it better to use semiconductors with low conduction, low switching or a trade-off between both?

New semiconductors can be faster with less switching losses. This makes it possible decreasing total losses and using smaller or different cooling systems. On the other hand, increasing the switching frequency may reduce the weight of the filters so there is a trade-off between the weight of filters and cooling system. Another possibility is to employ high temperature components, which accept a higher junction temperature and reduce the requirements on the cooling system. In general increasing the temperature affects reliability, so it should be checked that the technology of high temperature components is mature enough to maintain reliability at an acceptable level [28] [29].

- Has my design reached a global optimum? Is there an easier, more efficient or less expensive solution?

From the previous questioning, it is clear here that a global trade-off has to be calculated. However, it is not easy to perform it theoretically. This is the reason why the construction of a computer-aided tool is required. Optimization techniques are a good approach to play automatically with the degrees of freedom and obtain designs that match given requirements; example of such studies can be found in the literature:

- In [30], the author proposes a study of several topologies in order to reduce the overall cost of the system.
- In [31], cost models are proposed for the main components of SMPS in a power range from 5 to 50kW with the objective to integrate them in cost optimization routines.
- In [32] the authors take into account the influence of the weight and volume of passive components to build an optimized converter. They show that the cooling system has a predominant effect on sizing.
- In [33], a converter design platform is provided for the production of integrated system.
- Finally, in [34], the authors present the limits of power electronics by reviewing various options for reducing the mass and volume of converters.

Nevertheless, realizing a complete study from these different papers remains difficult because of the lack of information. Therefore, a new methodology must be created to answer all these problems.

From previous questions, we can establish a synthesis on different axes to take into account in our models and optimization for the virtual prototyping development. We conclude that the optimal design and the computer-aided tools have to follow these factors driving power electronics and innovations. These three vectors of improvement have been studied during the ETHAER project, in different thesis and laboratories, as already introduced earlier in the first pages of this manuscript. We link each topic to the main current publications and partners:

- Evaluation of current/future opportunities in power electronics such as new components and technologies (This thesis, Laplace/Airbus Operations SAS)
- Comparison of the numerous topologies and possible evolutions or improvements with additional circuits or components (This thesis & IES [35])
- **Emergence of integration techniques and their simulation** (GEEPS & Ampere [36] [37])

Addressing these three bullets, should make it possible to optimize volume, weight and efficiency of static converters. A review of emerging innovations and future developments in power electronics and aeronautics is necessary to define the models to be created in future computational tools.

1.3. Vector of improvements in Power Electronics

1.3.1. Components and Technologies

It is mandatory to know precisely what the main types of components are in power electronics to find the optimal design. The most relevant technologies have to be modelled and integrated in the optimization tool. It is natural to think that the last technical concepts will bring benefits on one or some of the chosen objectives. However, they are not always mature enough and the limited possible progress of the coming decades must be taken into account to establish a feasible perspective [38]. Therefore, it is very interesting to measure possible improvements between the current and future solutions and have a glimpse on the perspectives. As a result, the current questioning is to know what are the technologies to be modelled in the optimal design. We have already answered this question in [39]. However, a shortlist of the technologies mentioned in the paper is summarized in Figure 10.

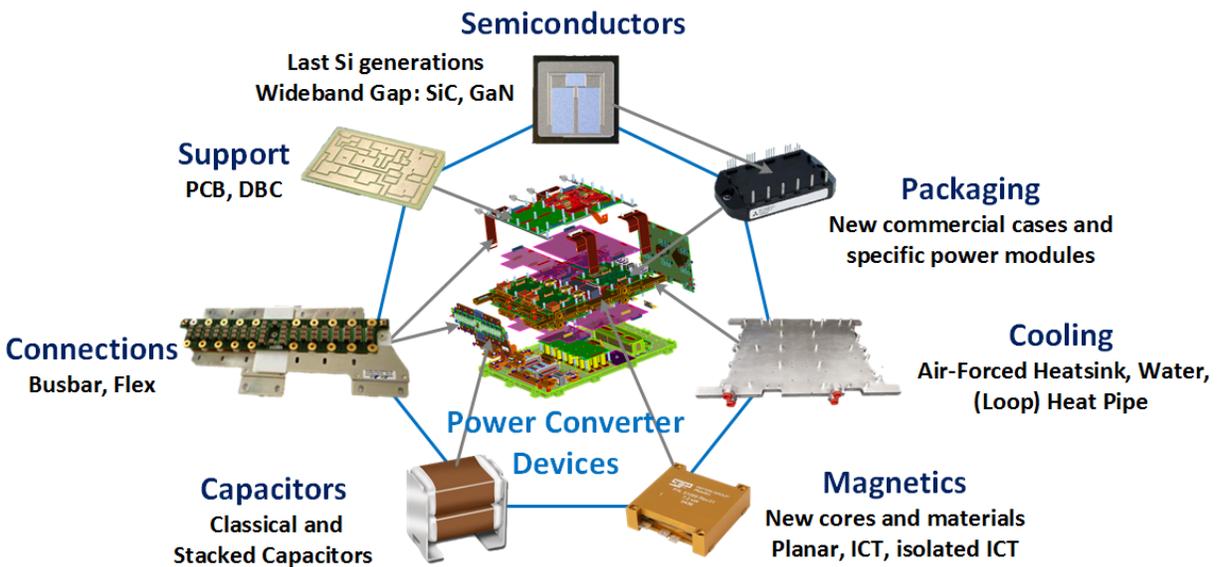


Figure 10: Examples of current and new technologies to be modelled in the computer-aided design tool

1.3.2. Topologies

Nowadays the global study of the different topologies has been made and only small innovations can occur in the field of energy conversion. However, choosing the best topology for a given set of specifications is still a very difficult task. Indeed, many variations and strategies on a same topology exist that keep pushing the improvements limits, and based on key factors such as performance, reliability, integration, weight and cost. Classification of these different structures and evolutions must be done in order to make a pre-selection and then use the optimal design approach to compare them. However, it is impossible to choose the best one directly without making a deep study. Now it is clear that a tool computing directly different combinations can make the work of the designer

faster and easier while ensuring the relevance of the solution. Such an example is given in chapter 5 and a survey of BBCU topologies in Appendix.

1.3.3. Integration

In this memoir the word “integration” means all processes, machines and techniques that can help building smaller and better power converters. Optimizing constructing and assembly can be a way to save weight, but it can be also an absolute requirement to make the system work; for example, with fast switching semiconductors stray inductance can be a killer, and sophisticated assembly techniques can be required to allow safe operation of a commutation cell. In recent years construction techniques have radically evolved, for instance with the Bus Bar and Flex technologies [40]. Other examples are the elimination of packaging creating parasitic inductances [41] and the reduction of the circuit size allowing better electrical performance, eliminating soldering and increasing the reliability [42]. Another approach is to use power modules to increase the level of integration of all active and passive components. The term 'integrated power module' refers to the fact that several components share a single substrate and case. The power modules are the best example of this trend. For instance, the driver commands and possible protections systems are directly incorporated in the module [43]. A demonstrator of a multilevel application with an integrated capacitor is realized in [44] and shows the benefits of power module - reducing the volume, easing the assembly of the converter and improving the thermal management. The last example we can give is the components buried in a PCB (Print Circuit Board) or a DBC (Direct-Bonded Copper). The purpose there is the same as for power modules. As a conclusion, more and more studies consider the integration of methodologies using 3D considerations in order to optimize the integration [45]. More classical techniques and prototypes accepts passives components inside the PCB more easily, like planar capacitors [46]. We can also mention the work of the ETHAER project, to which this thesis belongs. It is a study mainly focused on the semiconductor, package and driver integrations (Figure 11). As an example, several thermal management techniques for GaN transistors have been investigated, with a Wafer-Level Packaging (WLP), mount on DBC ceramic substrates to detail the manufacturing process and get thermal simulations and experimental results. More information are detailed in [36] [37].

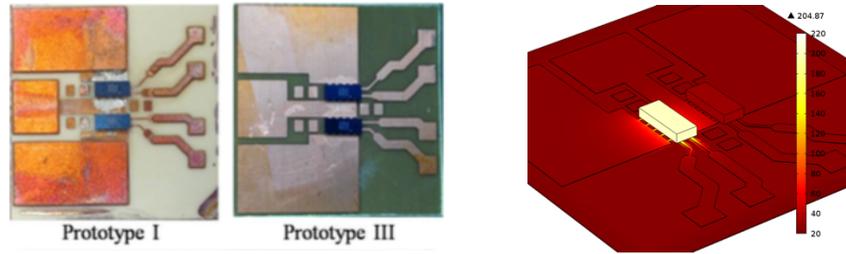


Figure 11: Photographs of integrated switching cell prototypes and related temperature simulation

1.4. Conclusion and Axes of research

1.4.1. Chapter 1 – General Introduction

As a conclusion, this introductory chapter has presented the context of the More Electrical Aircraft. It explains why power electronics is a key factor for future aircrafts and how it is integrated into the electrical architecture. With the increasing power demand and number of power converters, new problematics arise. Therefore, new methods to address them more efficiently are required, especially in relation to digitalization. In this context, new converters have been created due to the emergence of a new HVDC network. Because of the numerous new challenges arising from these designs, this thesis is aiming at creating both a methodology and a computer-aided design tool. It aims at designing automatically whole static converters, for any kind of application. In addition, a review of design issues in power electronics has been reviewed in order to identify the technological locks that the optimal conception has to address. Then, the relevant technologies, topologies and integration processes have been reviewed in order to list the different aspects to be modelled in the final design tool. During this thesis, different axes will be explored and can be presented in four other chapters.

1.4.2. Chapter 2 - Optimal Design Methodology

The optimal design in power electronics requires a global methodology to optimize the sizing of a converter. This chapter aims to explain how to set an optimization problem on a power system and how to create the different parts of the virtual prototyping platform (presented in 1.2.2). In other words, it is the backbone of our optimization software dedicated to the power conversion. In addition, rules, pattern and strategies will be presented on the different computational objects that are parts of our libraries: components, composite (assembly of components) and topologies.

1.4.3. Chapter 3 & 4: Models of Power Devices

These chapters explain how to create all the main multi-domain models of power devices in a converter, which is useful for the optimization and pre-sizing methodology. For each component, a technological review is done with performance factors allowing to select the best ones in a design. Then, continuous and analytical models are proposed according to different granularities in order to incorporate them in an optimization. To finish, some experimentations have been realized to

assess the pertinence of our models in the final study case. The chapter 3 deals with the “active part” of a power converter, gathering the switching semiconductors and their associated cooling systems. The chapter 4 deals with the “passive part:” capacitors and magnetic components, including inductors, isolated transformers or not isolated inter-cell transformers (ICT). In addition, the filter sizing is introduced, gathering both previous device families. In each chapter, geometrical, thermal, electrical, cost and losses models are proposed to answer to the needs of the computer-aided optimal design. Different shapes, geometries and materials are considered in order to cover all the possibilities of the current technologies used in a static converter.

1.4.4. Chapter 5: Optimization of Power Devices, Topologies and Converter

The chapter 5 proposes to optimize several case studies extracted from the power devices constituting the global converter. Firstly, we propose local optimizations of the classical power devices that require a “custom” design, such as heatsinks and magnetic components. Secondly, we demonstrate how we can optimize an assembly of several devices with a filter topology thanks to our methodology and models. Finally, we propose several converter optimizations. We will focus especially on the BBCU converter in order to highlight the limits of our current work on the optimal pre-sizing in power electronics and how to improve it. Concluding remarks are exposed then in order to provide a global overview on this thesis work, but also to provide an outlook and directions for possible future research.

Chapter 2

2. Methodology for the Optimal Design of Power Converters

Optimal and aided design in Power Electronics is a problem as old as the discipline itself. It is also obvious that the virtual prototyping of converters is less advanced than in other fields such as mechanics [1] [2] or electrical machine [47] [48]. Among numerous topologies (multiple converters architectures) and technologies (diversity in terms of components and materials), the optimal choice of a conversion structure dedicated to a specification remains a difficult exercise. Therefore, solving physical problems thanks to optimization algorithms is critical to take decisions more easily and analyse the physical systems in more depth. The purpose here is to find the minimum value of mathematical functions among the set of all feasible solutions, answering to certain conditions or constraints (1).

$$\min_{x \in R^n} f(x) \text{ subject to } c(x) \geq 0 \quad (1)$$

To set the problem in the Electrical Engineering context, the computation has to find an optimal design and assess trade-offs of components and static converters. In addition, the current analysis and resolution power of computational tools – such as circuit simulators, finite element methods (FEM) and, solvers of all kinds – offer considerable potential that we can no longer ignore. Thus, it is essential to define the needs of computer aided-design in the field of power electronics. In our case, the virtual prototyping is a way to reduce the time needed to design and test prototypes, but mainly centred on the simulation of electric models. Although these simulations are essential to predict the interactions of different circuit elements, they are not sufficient to provide their elementary characteristics such as the mass and volume of the converter. However, some computer-aided design (CAD) software dedicated to printed circuit board or mechanical manufacturing systems can provide this information. Thus, this chapter proposes a new approach to fill in this lack in electrical engineering.

This chapter presents the different steps that have been realized in this thesis to set an optimization problem dedicated to the power electronics systems. First, the global architecture built in order to create a coherent hierarchy in the different elements of the proposed methodology is presented. Then, the strategy is chosen and detailed to solve an optimization problem dedicated to the energy conversion. A definition is also proposed that describes the components, allowing a 3D virtual prototyping based on a direct-model description. Thirdly, a way to assembly these different elements in sub-systems is created, called topologies, in order to perform local optimizations and to size the parts of the converter such as filters or semiconductors and their associated cooling systems. To finish, the environment to compute the models, solvers and optimization algorithms has been

created, resolving any sort of local or global optimizations in power electronics, with a graphical interface (GUI).

2.1. Software Architecture

2.1.1. Topology, Device and Material

First, a global architecture describing the building blocks of a power converter under a computing formalism has been defined. In this thesis, it is proposed to describe the converters as computational elements, often called « objects » according to the Oriented Object Programming (OOP) term [49]. These objects have intrinsic properties, such as their shapes, sizes and materials, and there are methods that calculate their weight, size but also their electric models, magnetic, thermal, losses etc. The integration of these models in a solver then allows the simulation of the physical object in a given environment, and makes it possible to optimize a full converter. To organize this process, a decreasing hierarchy of elements constituting a static power converter has been established: 1) topologies, 2) devices, 3) materials (Figure 12).

From the composition feature of OOP, a static converter is composed of different levels of *elements*. The analysis shows that the highest one concerns the *topologies*, which are sub-systems gathering several *devices* and designed to perform a specific function inside the converter. Three main items have been identified:

- *Active Topologies* realize the switching conversion thanks to semiconductor devices and switch the current and voltage waveforms to produce an electrical setting or process the power.
- *Passive topologies* mainly surround the active part and are composed of inductors and capacitors in order to realize the smoothing of voltage waveforms and/or current at the input and output of the converter. Thus, EMC disturbances are attenuated with differential and common mode filters in order to comply with different standards. Transformers are also considered, and in some cases their influence on filtering may also be included in addition of the isolation/conversion feature. Passive elements can also be used to build resonant tanks to create new converter topologies.
- *Cooling systems* collect and evacuate the heat losses in order to ensure an acceptable temperature rise inside the converter or devices. They are often integrated with a fluid like water, air or oils, in order to increase their efficiency but also to add systems to manage them like fans or pumps.

Moreover, *Topologies* are themselves composed of *devices* such as inductors, capacitors, semiconductors, heat exchangers, fans, pumps etc. Finally, each device is composed of one or several *materials*, which can be conductive, magnetic, or dielectric. All these elements have been analysed and will be detailed in this chapter in order to provide their modelling philosophy.

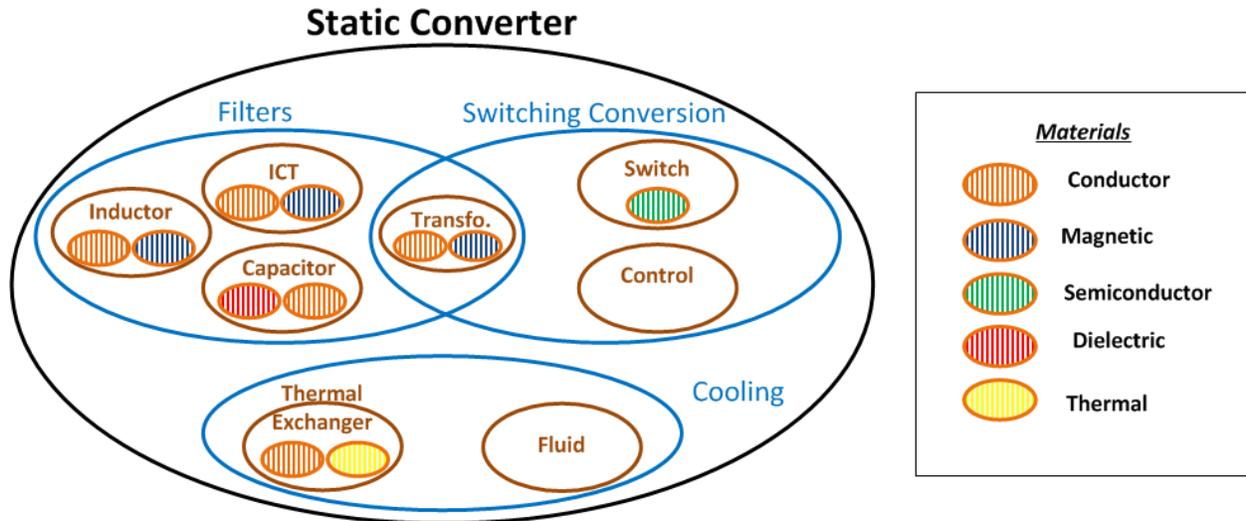


Figure 12: Global architecture of the predesign tool, already presented in [16]

2.1.2. Design pattern

Thanks to the “bottom-up” approach of the different elements constituting a converter and the OOP programming that has been created in the previous section, a new IT concept was introduced: **the design pattern of the virtual prototyping platform** (Figure 13). This completely new approach includes all the construction rules that were applied for the model library of this thesis under a computing formalism.

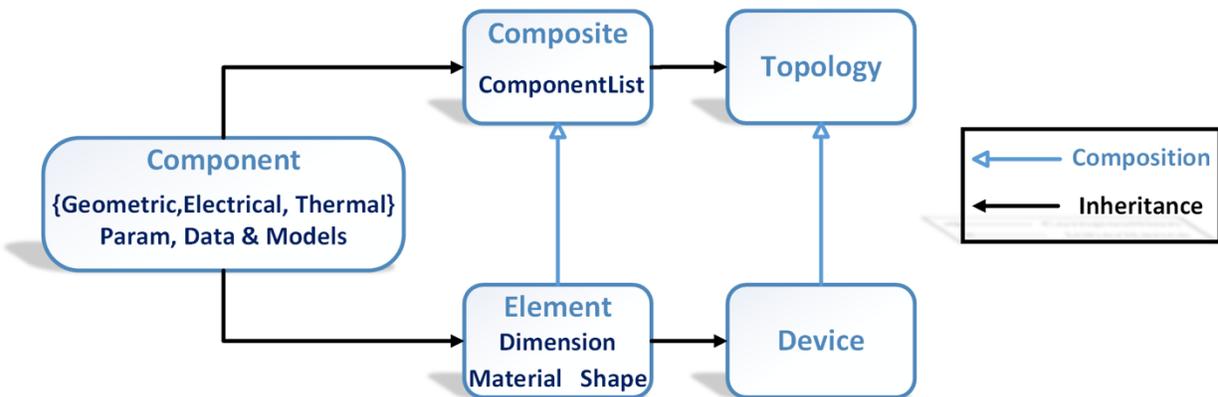


Figure 13: Class diagram for the different objects used in the new methodology created

Indeed, another useful feature of the OOP, also visible in the design pattern, relates to the inheritance of elements. These elements share common properties and methods of a more global element, which helps classifying models and physical objects dedicated to specific uses. Thus, inheritance and composition properties of each component family simplify and reduce the amount of code and library creation.

Figure 14 presents these principles followed by the library of components created. It is also listing the main modelling work realized during this thesis. However, before providing the details of each element models, a global optimization strategy has been decided in order to orientate the modelling process.

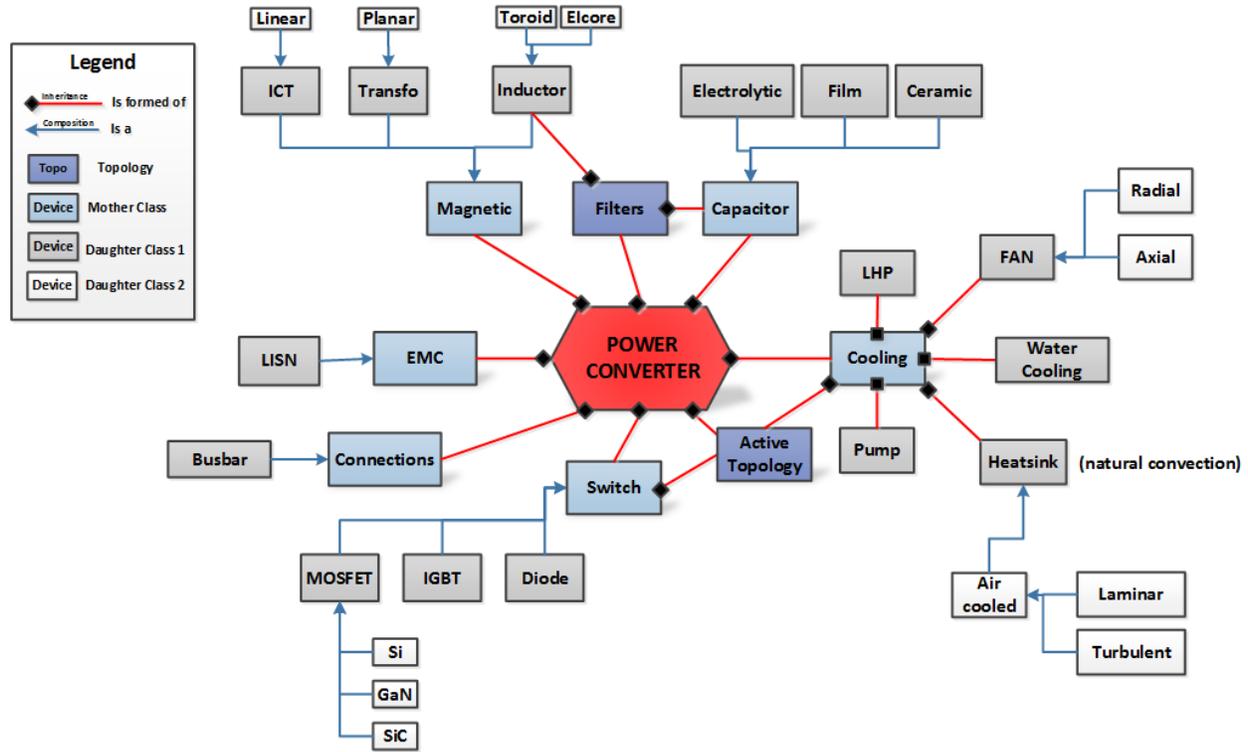


Figure 14: Example of a global pattern to sort the different models involved in a power converter, using inheritance and composition assets

2.2. Optimization Definition and Process

2.2.1. Strategy of Optimization

Many opportunities are available to describe an optimization problem and condition the way our models are made. However, a strategy has been chosen in order to get a relevant optimization tool. The first step was to identify and build an appropriate type of models to express the relevant physics used in the applications, i.e. to formulate the physical world under a relevant mathematical formalism. Different techniques exist in the optimization domain, and three main notions are used to characterize them: **variables, objectives and constraints**.

Firstly, **objectives and constraints** concepts have been developed and determined in the first chapter. As a reminder, the virtual prototyping in power electronics requires mono and multi-objectives computations, with multi-domains constraints guaranteeing the physical and system integration feasibility of the power converter. Thus, objectives and constraints have been integrated

as functions in the models of the library. A whole analysis of these functions has been conducted; it will be detailed in Chapter 3 and 4 for each type of device.

Secondly, the type of **variable** needs to be defined. Variables are the main components of the optimization system and are bound within an allowed interval, large enough to make sure that the optimal combination lies in the allowed space. Two types of variables exist: **continuous and discrete**. The discrete type is the natural standard used by designers in Power Electronics – for instance, with a precise selection of a component in a database, or a finite number of turn in for magnetic component. However, this approach is combinatorial and is difficult to apply to large systems like a static converter (up to 50 variables in our case). Therefore, the “continuous type” was chosen; it tends to make the system easier to solve because of its smoothness, derivability and deterministic assets and has reputation to be fast and easy to converge with relatively basic gradient-based algorithms [50]. Nevertheless, it may not be possible to differentiate a global or a local optimum without using particular strategies. In addition, it requires new kinds of continuous and physical models of power converter elements, containing new problematics like unrealistic results translating the continuous result in the discrete and real world. For instance, a number of 2.5 switches can be found as the result of an optimization with a continuous model. But in reality, is the best discrete solution obtained with 2 or 3? And does it still verify the optimum? (Figure 15).

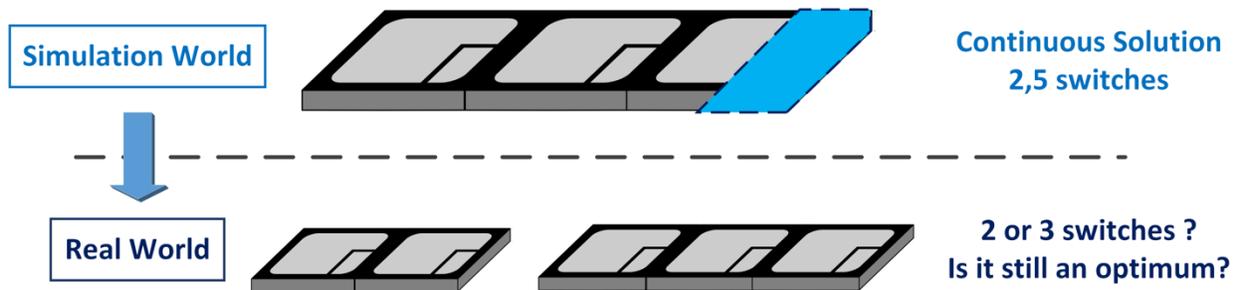


Figure 15: One challenge of the continuous formalism: the translation of the optimized results on a real solution

Thirdly, numerous optimization algorithms are now available, that have been analysed for this thesis. With the continuous strategy, **deterministic algorithms** such as gradient descent can be used, as well as **stochastic descent**, like the well-known genetic algorithm [51]. Determinism means that every time a gradient descent is run for a given training set, the same optimum is reached in the same number of iterations. Using this method in the case of minimization problems, the algorithm computes the direction that decreases the objective function the most. Some alternatives based on gradient descent exist to try to avoid local minima, like the multi start or global search techniques [52]. On the contrary, stochastic means that we obtain a different optimum and a unique cost as a function of the iteration history, by the computation of an approximation to the descent direction at every step thanks to random variables. Although stochastic ones are empirically often better and offer a better convergence on global results [50], they are also more complex to tune and longer in terms of resolution. Thus, **both will be used in this manuscript, but with a preference for the deterministic ones.**

Finally, and from our point of view, the electrical designer does not have to develop optimization tools, but have to know how to use it. Therefore, the Matlab software was chosen, as it proposes pre-made toolboxes on local and global optimizations [52] and allows coding our own developments, such as optimization algorithms, physical models representing the power converters and devices, methods, pre- and post-processing, and user interfaces. Moreover, the coupling with numerous commercial and physical solvers is today possible and is very interesting to perform multi physics simulations, like the FEM software, and magnetic and thermal simulations. As a conclusion of the strategy setting to compute optimization in power electronics, the choices that were explored during this thesis and their consequences are summarized in Table 2.

	Strategy	Resulting Actions
Variables	Continuous Variables	New library of physical models are required to perform a continuous description of power electronics elements
Objectives	Mono and Multi-Objectives	Calculation and combination of integration properties (weight, volume, cost)
Constraints	Constraint problems	Multiphysics constraints sizing the converters must be calculated, such as thermal, electrical or magnetic ones
Algorithm	Deterministic (Heuristic in a second time)	Creation of tools allowing the use of advanced optimization, communication between models and physical solvers
Platform Development	Matlab	Compile all the work done in a complete software suite, providing a simple experience and tools, with a Graphic User Interface

Table 2: Synthesis of the strategies of this thesis to create a computational tool optimizing static converters

2.2.2. Continuous Modelling

The philosophy of continuous models that have been selected in this thesis to answer the optimization context is very simple. The component chosen by the optimizer has to possess the ability to inform whether its design is viable or not. Because operating temperatures are considered as the main critical constraints in an operating converter, it is essential to control its calculation. The models required and created in the tool should allow estimating a temperature vector based on a geometric vector. In addition, models and parameters used should be representative of the state of the industrial state and limitations (discretization of data). They have to be adapted to technological developments. These models could be integrated into local optimization procedures (optimize the component) or global optimization procedures (optimize all the components of the converter. In an optimization under constraints, the optimization algorithm will minimize an "objective" function respecting a set of constraints. Once the models are created, it should be possible to incorporate any physical parameter except the specifications used in the objective function or in the vector constraints. To address this issue, the concept of "Comp3D" has been created; it is basically a mother class used to build a library of power components. This concept is explained hereafter.

2.2.3. Indirect and Direct Modelling

Because continuous variables have been chosen as an optimization strategy, a specific methodology of modelling is required to describe the devices, sharing properties and methods. Two classical methods of description used in engineering have been analysed and developed: the indirect and direct modelling.

The **Indirect Model**, mainly used in electrical engineering, has been investigated first. From behavioural parameters (electrical and thermal), integration outputs have been obtained (weight and volume) without knowing the precise geometry of a device. As an example, weight and volume of a capacitor can be defined from a dimensional relation using its stored energy. Because the indirect modelling does not take into account the structural or internal description of the component, there is no direct link with the geometry of a “real object”. From a sole integration output (volume, weight) an infinity of solutions can be found in terms of geometrical results (dimensions, shapes, number of layers etc.). Therefore, this way of modelling cannot be used for accurate virtual prototyping of components but can be useful as a first and quick method because of the ease to create models and the low number of variables.

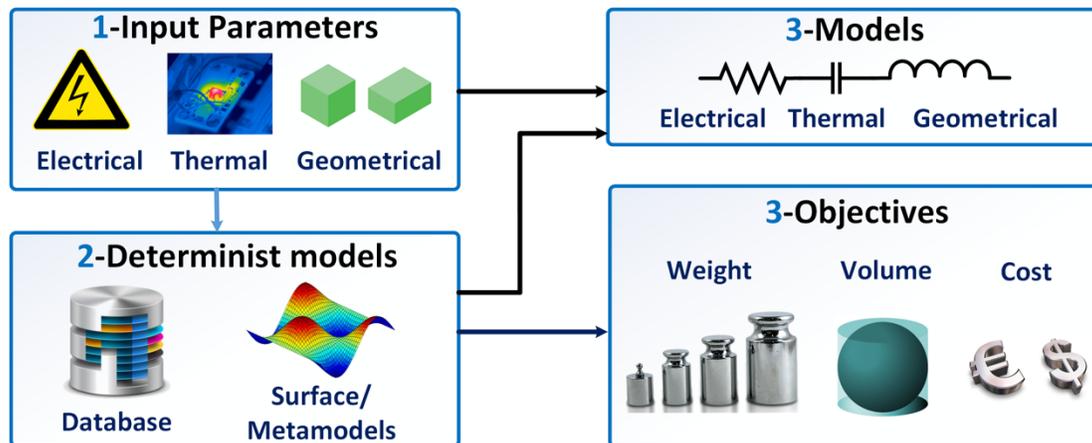


Figure 16: Indirect Modelling Principle

On the contrary, the **Direct Model** has been studied for accurate virtual prototyping, resolving the problems related to the non-unicity of solutions of the direct modelling. It is based on the real world description of physical objects from their shapes, dimensions and material descriptions. Once these features are described, integration (weight and volume) and behavioural (electrical, thermal and magnetic) properties have been obtained. This principle is extendable to any component (Figure 17). Thus, the optimization has to stretch and compress the component in any direction, making the different physical models vary in order to find the best geometrical dimension of each component.

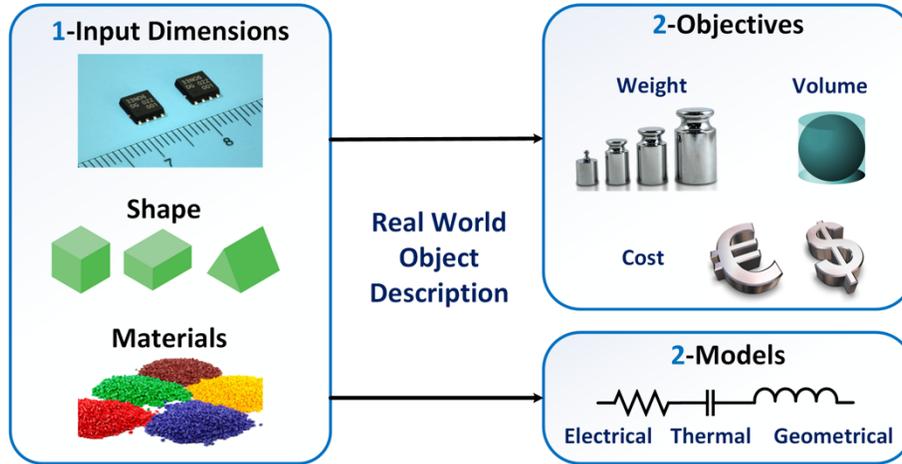


Figure 17: Direct Modelling Principle, called COMP3D (2.2.2)

This thesis has contributed to develop direct models of components adapted to the power electronics field. These models are detailed in the chapters 3 and 4. Once these models are established, a global resolution method to compute them is required [53] [54], and has been specifically adapted for power electronics problems as displayed in Figure 18:

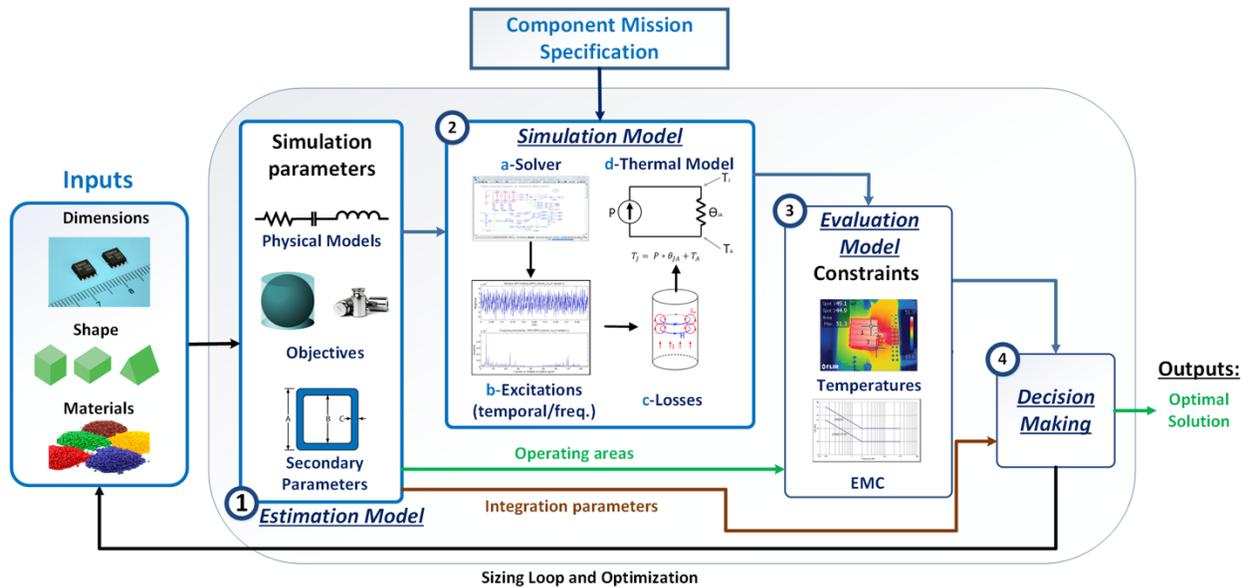


Figure 18: Comp3d steps methodology

- An **Estimation Model** calculates the problem objectives in terms of integration values – mass, volume or cost – and create physical and behavioural models (electrical/magnetic and thermal model) from the dimensions, shape and materials of the device. It has to minimize the number of parameters to process in order to simplify the sizing and the optimization.
- A **Simulation Model** computes the different physical models based on converter specification, computing the mission profile thanks to electrical, magnetic and thermal circuits. As a result, it provides excitations for the thermal model, and finally the device

behaviour to compare to the problem constraints. An electrical resolution followed by a thermal one has been used.

- An **Evaluation Model** checks the dimensioning of each component in terms of constraints (usually the maximal temperature) and validates the operating areas calculated in the estimation models.
- The **Decision Making** step accepts or refuses the current set of variable solution.

2.2.4. Direct vs Inverse Model

As already partially explained previously, it is important to highlight the difference between direct vs inverse models. Direct models are models able to represent the physics of an object. The inputs are the characteristics that define the physical structure of the object: shape, dimensions and materials. Based on these inputs, the direct model is able to predict the behavior of the object when external constraints are applied. For example, if a certain voltage is applied, the model should determine the current that will flow, and other useful physics can be included; thermal, magnetics, aerodynamic, etc. In our case, direct models deliver a nodal model for each physics, so that models can be connected to each other and used to simulate the behavior at a system level. In the real world, the inputs of a direct model fully determine all characteristics of an object, so from a theoretical point of view, there should be only one direct model. In practice, an object can have various direct models corresponding to various levels of accuracy.

An inverse model is a design model. Its inputs are the parameters and point of operation that we want to achieve (value of the inductance and allowed RMS current for example) and the outputs are the shape, dimensions and materials of an object that give these characteristics and allows this point of operation. Secondary outputs of an indirect model are typically the volume and weight. By nature, there is an infinity of objects that match the specifications, which implies that there is an infinity of possible indirect models.

Inverse models may seem to be more powerful since they tell how to construct the object we need to perform a given task. In fact, it is not so and inverse models suffer from various drawbacks:

- inverse models are generally obtained by inverting the equations governing a direct model, and this direct model must be a low accuracy model to make the inversion possible, (for example, neglect the fringing effect of the magnetic flux in the airgap),
- inversion generally requires strong assumptions or arbitrary choices to reduce degrees of freedom and make the system invertible (for example assume homogenous induction in a magnetic core or impose homothetic shapes to limit the number of dimensions),
- applied constraints are generally not defined at the component level, but at the system level (for example, assume that “we know that 20% current ripple in an inductor is the right choice”)

These remarks show that using inverse models limits the accuracy of the results and eliminates arbitrarily some degrees of freedom. It is therefore important to develop system-level design methods

that allow using direct models to explore a wider space of solutions, obtain more accurate results and allow finding improved designs.

2.2.5. Model Granularity

Ways used to model a device or a physical object in engineering are numerous and can take into account multiple physical and mathematical aspects, depending on the assumptions of the designer. Therefore, a new referential has been created in order to group and organize the different manner and describe our continuous models under a same formalism. It will be presented in this section. Different levels of description for a same device have been grouped and chosen, promoting either the time of computation or the accuracy: it is what we called granularity in this study. Thus, the models have been organized by precision with four levels (Figure 19). If one level is not available for some items, a substitution rule was defined:

- The **Level 0 or System Level** has the lowest granularity and offers a fast computation by considering a macroscopic physics, not using any materials and completing a wide range of exploration. The number of variables is minimized, with models based either on dimensional equations deduced from direct fitting of databases (response Surfaces). Either on a scaling approach and homothetic assumptions from a pre-chosen sample or model. A sole and global losses model is enough for this level.
- The **Level 1 or Converter Level** is a good compromise between speed and precision, with a rough description of the geometry and virtual material (best properties of a family range). Simplified physics-based models like 1D or 2D approximations are typically used, like the famous Area product for magnetic components [55]. Advanced response surfaces with several inputs, interpolations or Meta models are also considered [53]; these response surfaces are based on dimensional and physical analysis in order to provide a simple analytical equation. Here, DC and AC losses in models have to be separated for instance, in order to bring more details in the modelling work (rather than consider a more global loss model, less accurate).
- The **Level 2 or Component Level** favours the precision rather than the rapidity. The number of variables has been maximized to represent specific technologies. Different models of losses have to be as detailed as possible, with the choice of different models referring to the literature.
- The **Discrete Level** considers only discrete components extracted from databases or FEM simulations. This level is meant to be used when the highest accuracy is desired: post-convergence verification, refinement or correction of previous models.

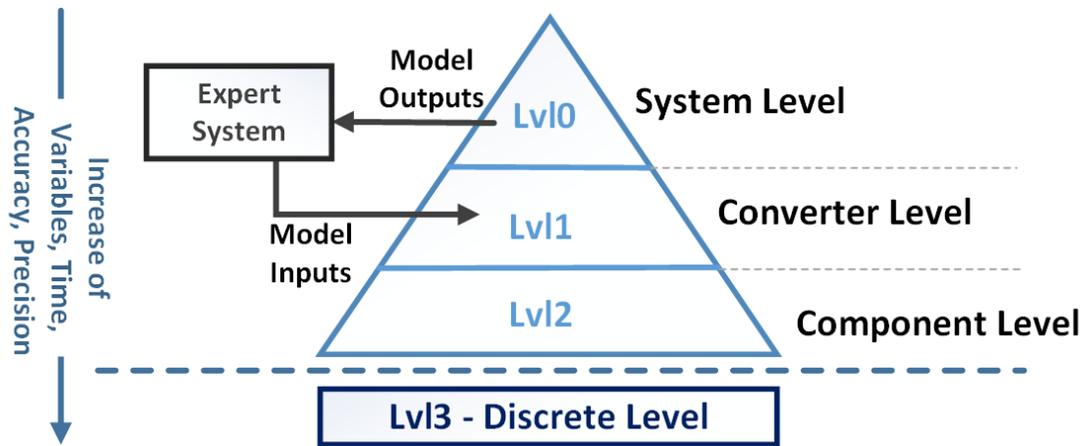


Figure 19: Models Granularity Architecture

Table 3 has been created to sum up the different granularities, and detail the key properties of each stage. An example was performed on a heatsink model, providing an estimation of the time computing on a sole iteration.

	Name of the level	Number variables	Average Error	Type of Model	Computation time (Heatsink object example)
Level 0	System	1-2	<50%	homothetic equations response surface dimensional equations	0.01 sec
Level 1	Converter	3-6	<20%	Simplified physics-based models like 1D or 2D approximations	0.09 sec
Level 2	Component	>6	<10%	Detailed physics	0.55 sec
Level 3	Discrete	Depending on the database or FEM software	Depending on the database or FEM software	Exact physics	FEM: Depending on the mesh, > 10 min

Table 3: Synthesis of the different levels of granularity used in the context of the optimal design

However, in some cases the designer does not want to specify the level of granularity of its model or describe precisely a component. Some reasons can explain this situation: either he wants to explore new possibilities during the optimization process, or he has no idea on what is the best parameter for its application. In this situation, he can use an expert system. This approach allows accelerating the whole optimization process by tightening step by step the possibilities and range of exploration, as well as avoiding the discrete parameters. Simple strategies have been developed by direct descent between levels, based on obvious deductions. This option is left open for future research in the direction of system expert functions.

2.3. Solvers and Excitations computation

As explained previously (2.2.2), objects that have been created require solvers in order to compute their physical models, (electrical, magnetic and thermal). They have to be able to translate their definitions expressed under different formalisms such as node list or analytical definitions. Thus, these solvers compute the excitations that are essential to the calculation of signals and quantities compared to the physical and system constraints (such as losses and EMC disturbances). In our case, different kinds of solvers are available, adapted to specific problems and more or less suitable for the virtual prototyping. Because the thermal models can be expressed with an electrical formalism (source, resistance, ground etc.), only electrical solvers have been explored and developed in this part.

2.3.1. Solver Simulation

To perform the electrical simulation, two solutions are available:

- Temporal simulation, with a possible transformation into the frequency domain
- Frequency simulation

a. Temporal Simulation

The first method to simulate an electrical topology, concerns the temporal simulation. It is the usual method for simulating a circuit, establishing fine simulations and verifying the validity of objects. It is easily feasible because each component has at least one or several electrical models expressed as node lists that are switchable with different granularity descriptions. Thus, the different components can easily be interconnected and create an overall power converter model. Then, we just need to use a classical solver on a global electrical circuit. Commercial usual solvers have been tested (PSpice, PSIM, SABER, Simulink, Plecs, etc.), to get the right excitations in a sole simulation at each bound of components. These excitations are then used to calculate losses and temperature, or to compare it with the physical and system constraints (Figure 20). About their operation, these temporal solvers perform a numerical integration through differential equations, derived from the interpretation of a circuit, while respecting a time definition of the system. They realize a good accuracy of the waveforms, particularly in complex cases of discontinuous conduction. Nevertheless, for a relevant frequency analysis, it is necessary that the number of samples is large enough, and that the steady state is established [56]. In our case, shooting methods have been used to obtain directly the steady states values and avoid problems of convergence due to non-physical aspects. In addition, the presence of reactive elements of strong values (filtering, monitoring port etc.) significantly extends the transitional phases of the signals and can bring difficulties with these solvers [57]. These factors combined with very low values of the calculation step make the simulation time very significant (from sec to dozens of sec for one simulation). Therefore, the "computing power" is here one of the limiting factors. Thus, this approach has to be avoided if possible for optimization computation. As an example of a commercial solver used in optimization, thesis [16] uses vector

simulations adapted to the study of multilevel topologies. Thus, from a single circuit model, it is possible to simulate multiple combinations of topologies in series and in parallel.

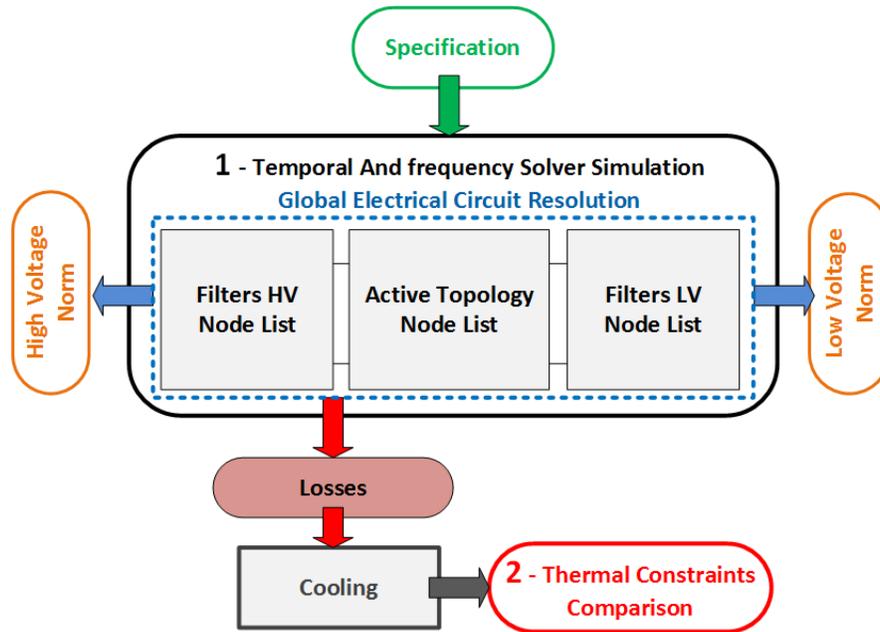


Figure 20: Solver Simulation, using a global electrical circuit

b. Indirect Frequency Simulation

From these classical solvers, it is easy to get temporal vectors, but we often prefer to use frequency data to design the different elements of our library, in order to get more accuracy on the losses calculation or EMC comparisons. Thus, Fast Fourier Transform (FFT) operation is required on temporal vectors. Although it is well managed by engineering tools (it has been tested with Matlab in this this thesis, or directly with integrated options in solvers), it extends the time of computation. The complete classical protocol is detailed in [58], explaining that the calculation steps must be small enough to meet the properties related to the sampling of signals. From our experience, time and frequency (via FFT) methods of simulation are not well suited for optimization resolution with our standard computers. The simplest optimization problems take hours or days to be solved with advanced algorithms. In addition, many problems can occur during the simulation because of non-physical values of components, the variables exploration, and the method of getting the steady state by shooting methods. Therefore, we need another method to get our frequency operation vectors.

c. Direct Frequency Simulation

To avoid this intermediate step of FFT computation, an alternative exists. A direct frequency solver called OOTEE has been used. It has been created with a collaboration between the Laplace laboratory and Liebherr Aerospace and means “Oriented Object Tool for Electrical Engineering”. It is a steady state frequency solver used to solve classical problems related to electric power supply and high power electronics. A part of the work related to this solver that has been realized was to

debug it as beta users. Then others extensions have been added among which a library of models, a design method and optimization functions. In addition, special functions and resolution methods have been analysed to optimize filters (Chapter 4). It is important to notice that this solver is not built like most electrical solvers; its speed is a first choice for optimizations because of the fast simulation of steady state waveforms (temporal and frequency), which is less than a second. A comparison with the temporal solver PLECS is shown in Figure 21. In addition, it can simulate “Configurable” power converter in terms of multilevel topology, associate different conversions and use several modulation schemes. However, only topologies whose architecture are based on classical switching cells are available for now, such as inverters and non-isolated DC-DC conversion. In order to extend its use to other topologies, an analytical resolution method explained in the next part has been realized.

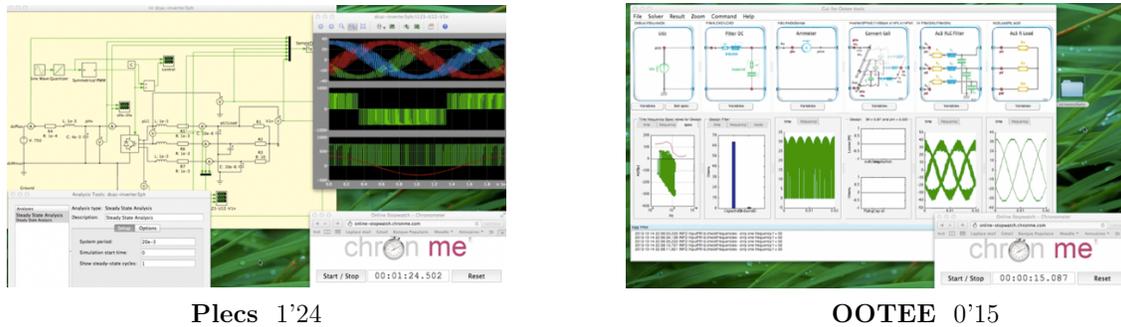


Figure 21: Example of a time comparison between the OOTE and PLECS solver computation

2.3.2. Analytical Resolution

To avoid using real-time or frequency simulations on the whole or part of the converter, a method based on analytical resolutions has been proposed. The main asset is to accelerate the computing time compared with classical temporal/frequency solvers, which is very important for optimization routines. In addition, the analytical definition allows describing specific converters, which is not possible with the solvers. In our case, we used the analytical representation for the switching conversion of isolated DC-DC topologies that we coupled to the OOTE solver. Thus, the rapidity and accuracy of the frequency solver are maintained, even on very specific topologies. In addition, this methodology saves time to set the problem and improve the capability and versatility of filter objects. A global process can be formulated to explain the analytical resolution. From the specifications (voltage, power, ambient temperature etc.), the topologies are successively excited with the following steps (Figure 22).

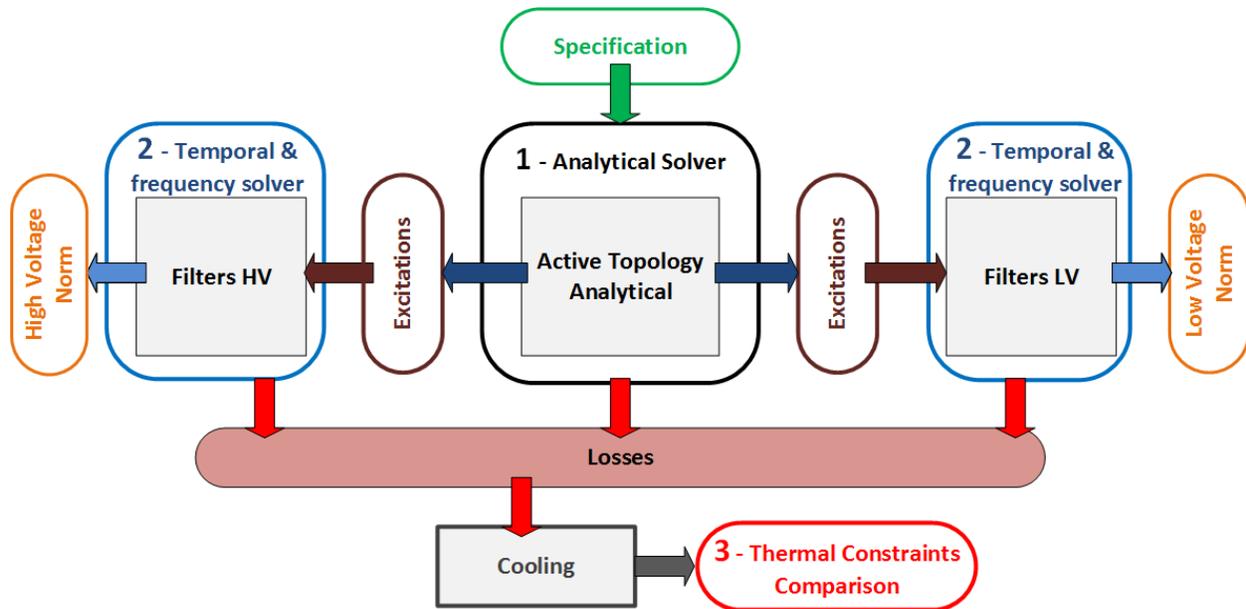


Figure 22: Analytical and Solver assembly for an optimal converter sizing

- 1) Operation points of the active topology (peak, average or rms values) are calculated thanks to an analytical representation of the static converter. A library of analytical topologies has been built in order to provide a wide range of topologies such as classical and bidirectional DC-DC, interleaved or not (Figure 23). In this step, the influence of filters and cooling systems are neglected.
- 2) Previous operation points are injected in filter objects on the Low and High voltage side. They allow recreating an equivalent source of excitation at inputs of each filter, in order to compute an AC study. Thanks to a simulation, current ripples at the output of both filters are then calculated. **Here, the assumptions are that both filters are fully independent and have no influence on each other.**
- 3) From previous calculations and simulations, losses can be extracted and applied to the thermal model of the converter, and so make the temperature rise, as well as other variables. For instance, the power dissipated in the semiconductor and/or passive components is conducted to the cooling system, and the heatsink temperature rise can be calculated and compared to the thermal constraints.

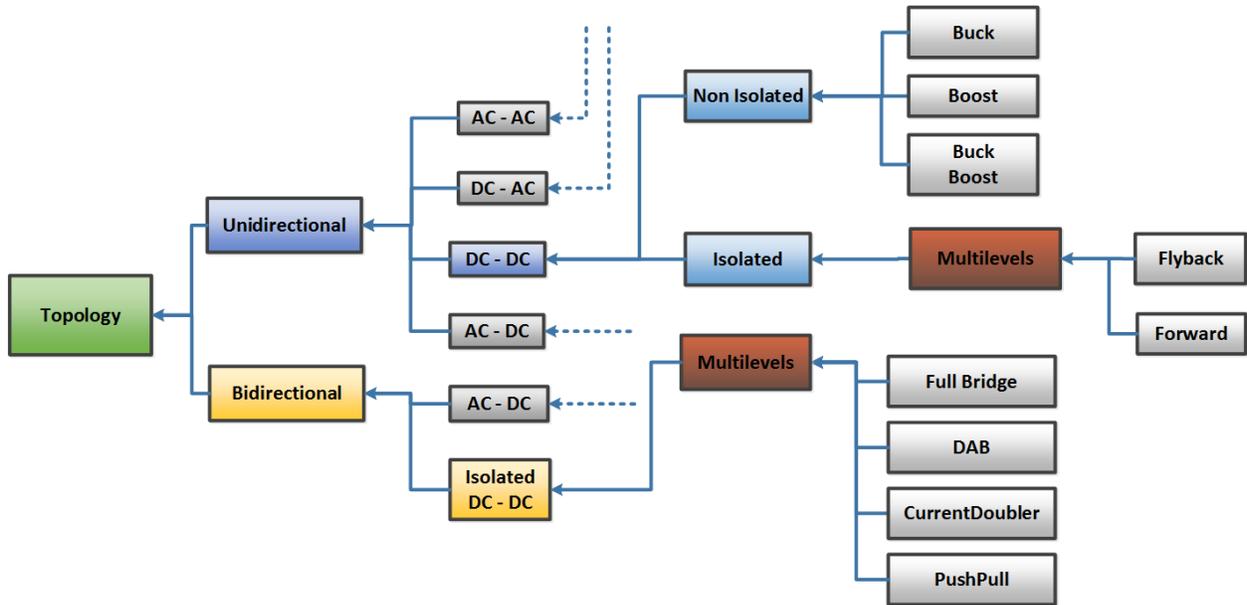


Figure 23: Analytical topologies library and hierarchy

This method of analytical and solver resolution mix is very interesting because of its speed and flexibility. A complete analytical resolution methodology without using temporal or frequency solvers was also explored. In other words, solver models of filters are replaced by analytical models to size and comply with the standards. Thus, we gain in speed, but some assumptions made us lose in accuracy (Table 4). These analytical representations of filters were realized from different methods as explained in thesis [58]: Transfer functions, State Representation and Matrix approach. However, this kind of description is not flexible and requires a longer work to debug and make reliable models for a specific topology. In the end, it is less attractive than the previous method explained.

To conclude this review of electrical solvers for the optimal design of power converters, pros and cons of each type have been summarized in Table 4.

	Pros	Cons	Iteration time order
Temporal solver	Global, accurate, secure, graphical interface or node lists definition, libraries, computes any sort of topologies	Very slow, discrete variables, convergence problem, needs FFT, adds of shooting methods for steady state	10sec
Analytical Solver	Very fast, applicable to any topologies, continuous variables, gets direct operating points	Strong assumptions on electrical phenomenon, difficult and long to create, limitation in regards with the complexity of the circuit, possible bugs and errors on theoretical equations	msec
Ootee, a Frequency solver	Average to fast speed, direct frequency vectors calculation, numerous options, linked to the thesis libraries	Limited to classical converters (choppers, inverters etc.), only discrete variables, not so easy to set up, time to understand how to use the solver	sec
Mix Frequency & Analytical solver	Fast, applicable to any topologies, continuous variables	Needs to master and connect analytical and frequency methods	10 msec

Table 4: Proposition of solver use for different simulation granularity studies

2.4. IT development and outlook

Although the previous points are the most evident works of our sizing methodology, numerous IT tools and functions are required to provide designers an accessible and efficient software platform. They are numerous but they have a poor scientific interest in this manuscript. However, because they are crucial to run our work, we will enumerate them. Indeed, designers have to consider this very important aspect in virtual prototyping; it may simplify and improve the user experience, and it will allow spreading this new methodology in electrical engineering. Some examples of tools developed during this thesis are now presented.

2.4.1. Process Management and libraries

In order to manage the optimization process between the different objects (models, solvers, optimization algorithms etc.) of the virtual prototyping software created in this thesis, libraries have been built and filled in to organize the whole process and simplify the coding and user interaction. A non-exhaustive list of these methods and objects is proposed:

- +Comp3D: devices and topologies library as shown in Figure 12
- +Topology: analytical solvers of different topologies presented in Figure 23
- +OptimAlgo: specific optimization algorithms that have been created as an alternative to the ones proposed in the Matlab Software:
 - AGNEOptim
 - APSOOptim
 - ESOptim

- +OptimDesign: library of models that are not devices, topologies or solvers. In other words, it gathers mainly utilities, such as a function to couple semiconductors and cooling systems.
- +OptimProblem: local or global optimization problems related to a power converter. Thus, pre-made scripts of device, topologies and converters optimization on a single or multiple operation points have been proposed. Moreover, direct functions such as sensitivity studies, multi-objectives or Pareto front are available.
- +OptimTools: library of parsers and methods to establish a communication between models/solvers and the optimizer. In addition, tools to visualize information during and after the optimization are available, which are mainly used during debug phases.
- +Unit Tests: library of unit tests in order to maintain a robust version of the software

Then, numerous methods available in the platform have also been created, grouped by their functions:

- Configuration Files: adapt and configure any computer and OS in order to use our software,
- Database Manager: utilities around the management of material, devices, and fluid databases,
- Data & Excitations: possibility to stock external files; internal files and data that are called during the design process,
- IHM: this part is developed in the next section,
- Standards: files to store the different electrical standards, used in the design and compared as constraints,
- Post Processing: link the different functions of post processing such as communication with external solvers (FEM, electrical). It also calls the database manager to compare the result with real samples,
- Pre-processing: functions to create our models from the database manager and other software,
- Script: examples on the whole range of models listed in the previous files and libraries,
- Tools: all the other scripts, such as graphical option for the plots,
- Results: Files to store the results of the different computations.

2.4.2. Graphical User Interfaces

All the previous files and scripts relate to the back-end part of the software i.e. that is the hidden part for the user. Therefore, a prototype of front-end interfaces was developed, in order to ease the user experience but also to propose something more accessible and configurable. The first example relates to data management and handling, which represent several challenges by their big variety, size and origins. Indeed, database management is a mandatory step in virtual prototyping. The continuous models that have been created are intrinsically defined by their materials, and some meta-models are built from a list of components. Eventually, specific sample can even be selected in our optimization to replace a model. Thus, a management function is available to sort and compute references of material and component databases: it is the database manager function.

Regarding the materials, four different families have been considered: Conductor, Dielectric, Insulators and Magnetic materials. The main characteristics listed in the database are the density for the mass, thermal or electrical conductivity for their respective models, or the “tangent delta” for loss calculation. Databases have also been created for the different fluids that are used in cooling systems such as air, water, or oil. On the other side, five families of components have been listed: Semiconductors, Capacitors, Heatsink, Fans and Geometry of Magnetic Cores. A deep work has been realized to get information on different sources (internet, catalogues, constructors, X-ray, studies, simulations, and assumptions) and unify them under a single formalism. A tool has been developed to create continuous models in a pre-processing phase, with regression or interpolation to fit in virtual models (Figure 24). Moreover, the component manager can choose discrete samples rather than using a model, and then apply a scaling law if the option is enabled. It is also possible to use this kind of GUI to treat the obsolescence of components for instance. In addition, FOM (Figure of Merit) (Figure of Merit) have been used to differentiate materials and devices for pre-studies (Chapters 3 & 4).

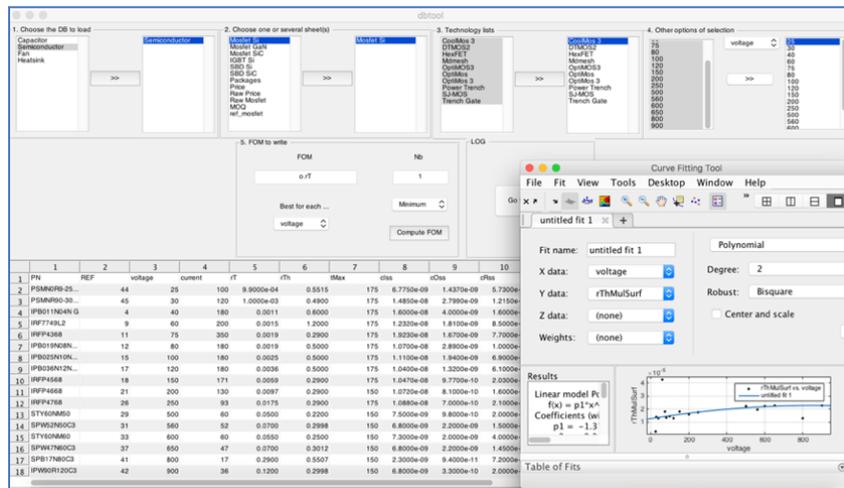


Figure 24: Database Tool and Curve Fitting tool used to create continuous models from our databases

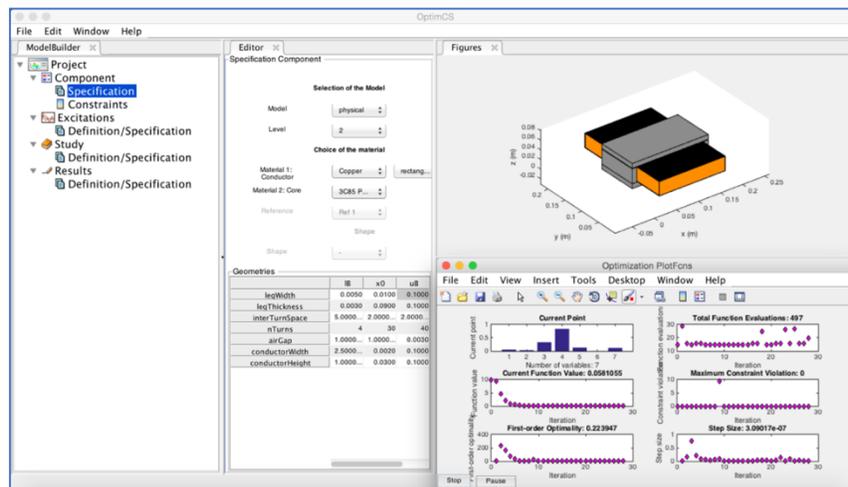


Figure 25: Proposed User Interface for predesign in power electronics

Another example relates to the purpose in making the pre-design methodology accessible, and propose a full demonstration of the thesis work. In this domain, a complete software with a GUI (graphic User interface) has been designed. This interface gathers all the methods and models described in this manuscript. In addition, it allows optimizing any component, composite, or topology according to numerous options entirely settable by users. A screenshot of the software is presented in Figure 25. An interesting evolution, which is under study at the laboratory, is to mix the proposed approach with an electrical circuit software construction, in order to create a WYSIWYG experience (What You See Is What You Get).

2.4.3. Outlook

An overview of what is and should be a virtual prototyping software and a power electronics optimization can now be given. Figure 26 shows the various models and design features presented throughout this chapter. The contribution of this thesis has been to give a backbone to this software, create the first elementary functions, and make the first step towards the global and local optimization of static converters. In the future, each part will be more developed and mastered in order to propose a final version that any designer in power electronics could use. In addition, with the increasing use and power of computers, new heavier methods such as FEM modelling could be directly implemented in the optimization in the coming years, in order to get results finer and easier.

2.5. Conclusion

In this chapter, the different methodologies to perform the optimization of a power converter have been analysed, and a specific strategy was established. Firstly, a software architecture that sorts out the different elements of a static converter at several levels has been proposed. An IT design pattern that follows the inheritance and composition features of the OOP programming and aiming at easy programming has been created, as well as a consistent library of devices and topology models. Secondly, a strategy in order to solve efficiently an optimization problem dedicated to power electronics has been developed. The aim is to use continuous variables in order to run deterministic algorithms, which are easier to compute because they are quicker and give a better convergence. However, it means that the device models created and their physics have to be described with continuous equations. Therefore, the methodology to create and compute models has been defined and presented. It has especially been used for direct modelling that allows getting the objectives and physical models of every device under a continuous form, based on inputs that are its material, shape and dimensions. Then, we proposed different ways to solve the models and a classification to choose the most suitable solver as a function of the optimization problem to treat. The purpose was to get new methods to avoid the use of classical and commercial electrical solvers, which can bring some recurrent problems in optimization. The use of a frequency solver has been explored, which is more suitable for the loss estimation, EMC calculation and comparison in our systems. However, this solver is limited in terms of variety of conversion topology. A proposition that mixes analytical

resolution of the operation point of converters with the frequency resolution of the filters has been presented; it is used to get the speed, accuracy and flexibility of the frequency solver. Finally, a review of the software tools and methods has been made to demonstrate the quantity of work to be realized in order to provide a final version of the software that could be used by anyone. The graphical user interfaces are exposed, which aim to propose something simple and configurable to users. To finish, an overview of the global software backbone is presented, explaining that a long way is still to be made before getting a final and absolute virtual prototyping tool.

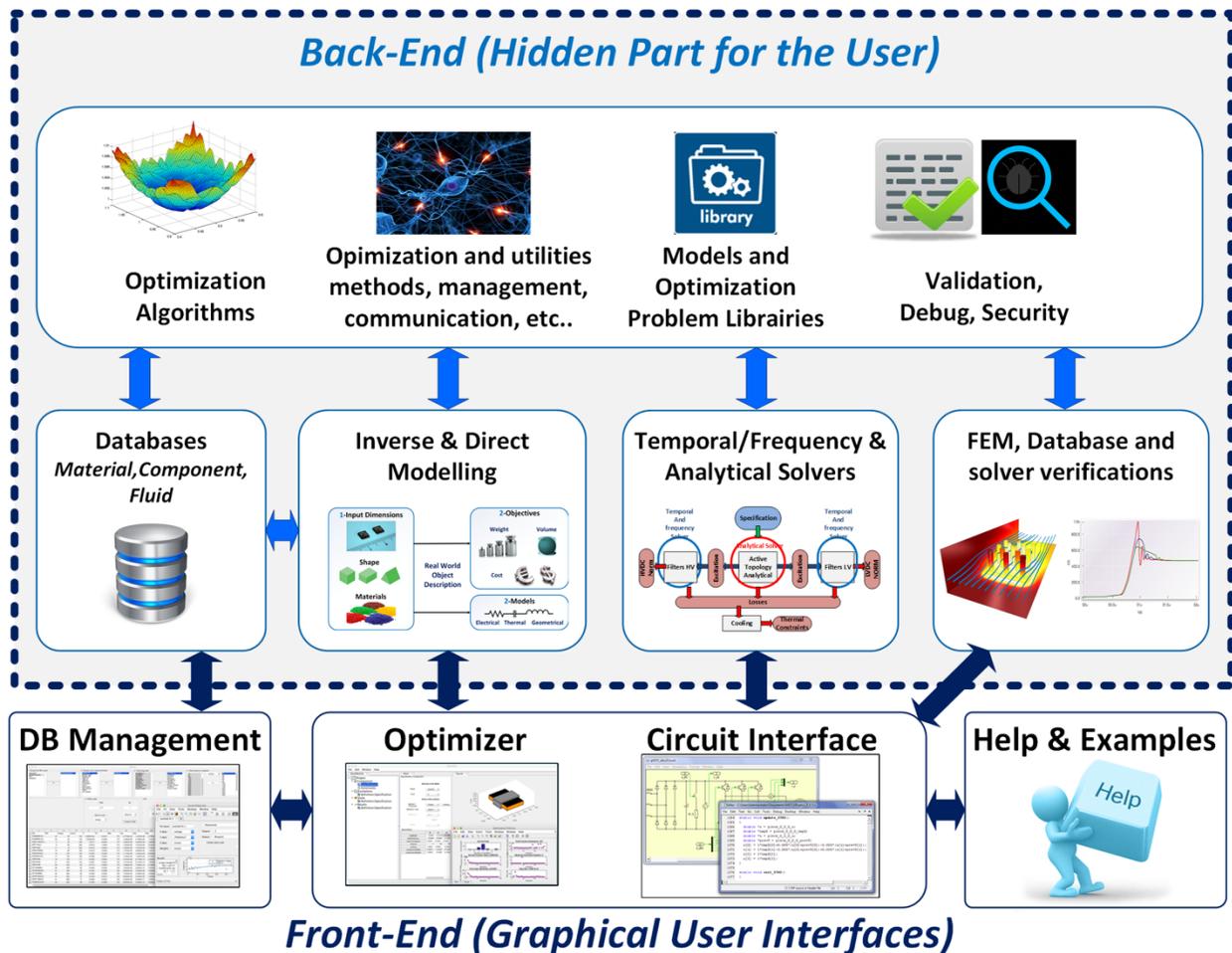


Figure 26: Global architecture of a complete virtual prototyping software dedicated to Power Electronics

Chapter 3

3. Active Part: Analytical models of Semiconductors and Cooling

The purpose of this chapter is to provide relevant continuous models to design and optimize the pair semiconductors (SC)/cooling device. The demonstration is split into two parts, in order to present individually each device.

Part A: Semiconductors

The main purpose of semiconductor models is to evaluate their conduction and switching losses because losses greatly influences the design of a power converter; combined with the switching frequency, loss models govern the trade-off between the weight of the filters and the weight of the heatsinks. In addition, semiconductor losses are generally the dominant losses, so they greatly affect converter efficiency. For both these reasons, semiconductor loss models are a key point in converter design and it is important to predict accurately the losses generated by a given switching device for a given point of operation defined by the voltage and current applied to the commutation cell, the temperature of the switching device, the gate resistance, etc.

A second aim of this chapter is to provide models helping the designer to select the right device at a very early stage of the process. This is especially helpful when multicell conversion is allowed: components with voltage and current ratings smaller than the voltage and current of the commutation cell become eligible, and this increases drastically the number of designs to be investigated. The brute force solution would be to run one design with each semiconductor in the database and select the best design at the end.

The ‘continuous semiconductor model’ that we try to develop in the second part of this chapter would be, in its ultimate version, a model with limited inputs (point of operation and voltage and current ratings of the device, for example) and would calculate the losses obtained with the best existing device with these ratings. Depending on the voltage and current ratings selected, the best device would be an IGBT or a MOSFET, for example, so this model could help an inexperienced designer to select the right technology.

In a less ambitious version, we could have different models for different classes or technologies (MOSFETs, super junction MOSFETs, IGBTs, and IGCTs for example), and these models could be used to reflect the influence of the number of series and parallel cells. To avoid the brute force design process described previously, these models could be used in an optimization routine so that

the best voltage and current ratings are automatically found; the same process would also indicate which topology should be used (how many cells in series and parallel)

However, discrete variables are difficult to handle in optimization routines, so such a model should be made continuous. For example, the voltage rating of an IGBT should not be only 600V or 1200V or 1700V; any value in between should be allowed so that the routine can slide from one rating to the other within the same optimization run and help selecting a likely-best voltage rating in one single optimization.

3.1. Review of Technologies

3.1.1. Semiconductor Technologies

Nowadays, the number of models required to represent all the semiconductors technologies is huge. Silicon semiconductors (Si) have evolved in the last decades to propose an important panel of efficient components: PIN or Schottky diodes, Mosfets [59] and IGBTs [60]. A few years ago, semiconductors design entered in a transition phase with the emergence of Wide Band Gap (WBG) devices such as Gallium Nitride with voltage rating up to 600V) and Silicon Carbide up to 1700V. They offer lower losses and higher thermal, power and frequency capabilities, leading to a better integration and size of passives components (Figure 27). Nevertheless, because of this integration, the electrical system requires special design layouts and advanced cooling considerations. Many comparisons have been made to compare locally WBG and Si devices [61] [62] and consider these technologies in the aeronautical context [63].

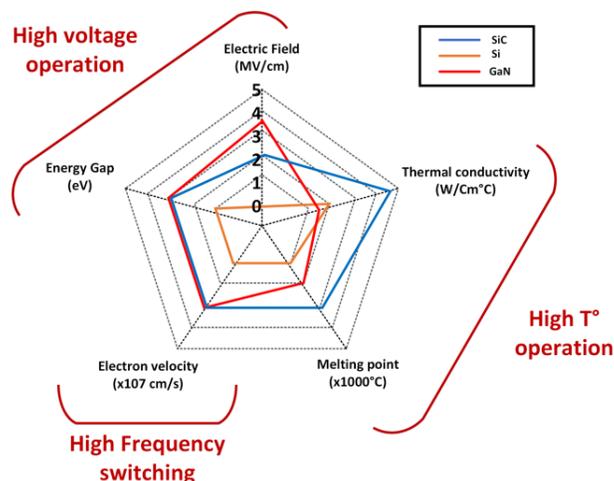


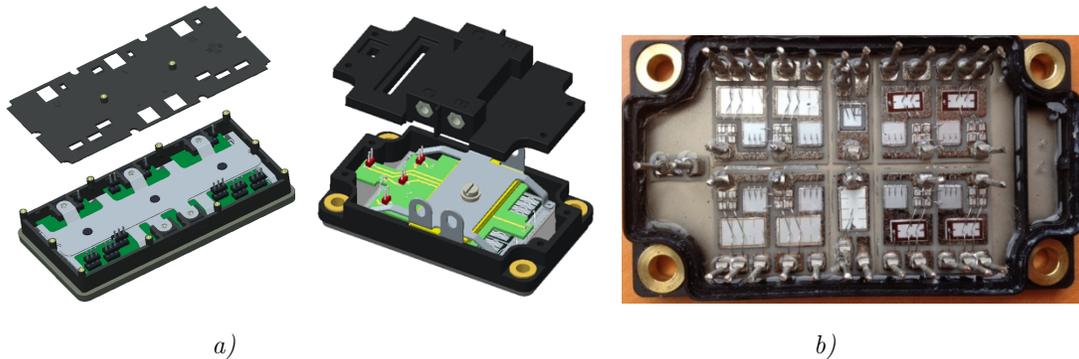
Figure 27: Comparison semiconductors technologies on 3 axes: breakdown voltage, operating temperature, switching frequency [64]

3.1.2. Semiconductor Packaging

Numerous types, technologies and sizes of discrete packages exist to encapsulate power chips [65] [66]. Recently, significant progress on recurrent limitations has been noticed on these commercial cases, such as parasitic inductance, capacitance or thermal impedance [67], [68], [69] and [70].

Despite cases improvements, discrete packages tend not to be used in high power applications. Aeronautics and space applications contribute to the miniaturization and system integration in power electronics, with severe installation space and weight restrictions. To reach higher performances and power in a smaller space, we use power modules accepting numerous chips inside the same package (Figure 28). The aim is to obtain a higher integration and less parasitic inductors with internal busbars or flex technologies, and to ensure that the drivers and decoupling capacitors are closer to the switch dies. In addition, EMI are reduced and probes or sensors can be added inside the module. However, such modules are quite high tech devices, and the cost of development and production can sometimes remain high.

Another problem is the concentration of hot spots, which requires an advanced cooling system to extract calories. An alternative is to bury directly the chips and driver into the PCB or DBC as shown in Figure 11 (1.3.3). This technology may bring improvements on electrical and thermal aspects, such as reduction of the thermal impedance, electrical unbalance and parasitic elements.



*Figure 28: Power Modules examples
a) with low inductance planar busbar (SEMELAB) – b) custom (Airbus)*

3.1.1. Basics of semiconductor modelling

First of all, foundations of loss calculation in semiconductors have to be introduced. These losses can be separated into two types: conduction and switching.

The conduction losses are generally defined by an on-state resistance R_{DSon} and a voltage drop U_{Drop} (2). The on-state resistance is always provided for Mosfet, but it has to be deduced from the U_{CE-I_c} characteristics [6] [71] for IGBT technologies.

$$Losses_{conduction} = R_{DSon} * I_{RMS}^2 + U_{Drop} * I_{average} \quad (2)$$

The switching losses at a specific voltage, depend on the switching frequency and the switched current. In many cases, choosing a larger semiconductor in order to reduce the conduction losses increases the switching losses and thus brings back the previous loss savings to zero. The switching energies are often discussed in the literature. They are dissipated during turn-on/turn off phases, and denoted respectively E_{on} and E_{off} . In [71], advanced equations have been written to calculate the switching losses from the switching energies and datasheets.

It is possible to identify three main sources of switching losses. However, these sources cannot be easily explained on a macroscopic plan. As a result, the proposition here is to use three coefficients (A, B and C) that are specific to each semiconductor technology [4]. The equation is detailed in (3) for the turn-on phase (the equation is similar for the turn-off phase).

$$E_{on}(i) = (A_{on} + B_{on} \cdot i + C_{on} \cdot i^2) \quad (3)$$

- **Coefficient A**, represents the losses that are independent of the current. These are typically the losses associated with stored charges in the output capacitor.
- **Coefficient B**, represents the losses that are proportional with the current. This includes losses induced by the crossing of current and voltage waveforms.
- **Coefficient C**, represents the losses proportional with the square of the current. This includes the dissipation of the energy stored in the inductances of the switching loop.

Finally, the switching losses are expressed as a function of the switching energies and frequency (4).

$$Losses_{switching} = (E_{on} + E_{off}) \cdot F_{switching} \quad (4)$$

3.1.2. Figures of Merit

Semiconductor manufacturers propose a wide range of devices, of which main specifications have been stored in a database of more than 8,000 references, gathering devices from various companies and technologies. In addition, these data can be classified by standard or user-defined features. Thus, in order to help selecting these references, two types of Figure of Merits (FOM) have been used: related to a single technology of semiconductors or several ones.

On the one hand, we consider the FOMs **related to a specific technology**.

For example in MOSFETs, R_{dsOn} can be used to identify samples with the lowest conduction losses, and $R_{dsOn} \times Q_g$ [72] can be used when a trade-off is needed between switching and conduction losses (Figure 29-a). Some variants of FOMs for Mosfet exist for high-density application [73] and for low voltage rating [74]. Other examples of FOMs related to a specific technology can be found for IGBT, GaN [75] and diodes/unipolar devices [76]. A graphical approach is also proposed in [77]. Similarly, COTS (Component-Off-the-Shelf) cases can be compared with a thermal FOM like in [78], in order to select the right thermal package depending on the application.

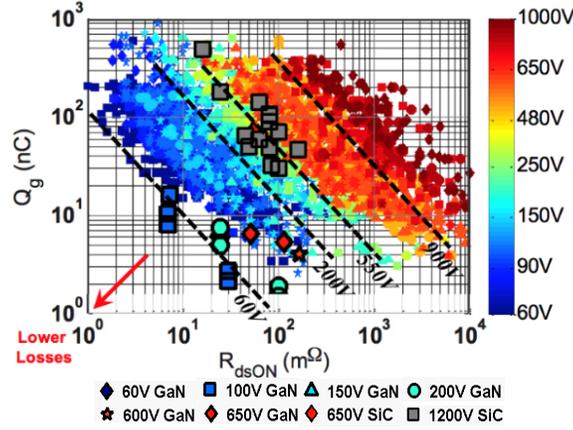


Figure 29: Mosfet comparison with the R_{dsOn}, Q_g FOM for different breakdown voltages [79]

On the other hand, the FOMs that include **several technologies** have been considered.

The aim is to compare different families of semiconductors thanks to a same criterion. In [16], a loss coefficient is proposed as the ratio of the dissipated and switched powers. It estimates the maximum conversion efficiency for a design with an imposed frequency and temperature elevation. The switched power (P_{sw}) is the maximal power transferred by a commutation cell. It is theoretically reached when the duty cycle is equal to 1. It is defined as the product of the high-voltage (V_{HV}) and the current of the low-voltage side (I_{LV}) (5).

$$P_{sw} = V_{sw} \cdot I_{sw} = V_{HV} \cdot I_{LV} \quad (5)$$

Thus we can obtain the global loss coefficient, with α the duty cycle of the switch and η the global efficiency (6):

$$\chi = \frac{P_{losses}}{P_{sw}} = \frac{P_{HV} - \eta \cdot P_{HV}}{V_{HV} \cdot I_{LV}} = \frac{(1 - \eta) \cdot (V_{HV} \cdot I_{HV})}{V_{HV} \cdot I_{LV}} \approx (1 - \eta) \cdot \alpha \quad (6)$$

Using the thermal and packaging parameters, the maximum power dissipated by an active device is given by the increase of the temperature ($\Delta\theta$), divided by the thermal resistance between the junction of the device and the ambient air (R_{th}). With f_{sw} , being the switching frequency, we get (7):

$$P_{Losses} = Losses_{cond}(\alpha) + Losses_{sw}(f_{sw}) = \frac{\Delta\theta}{R_{th}} \quad (7)$$

Thus, a maximal loss coefficient χ_{max} can be obtained from the previous definitions (8):

$$\chi_{max} = \frac{\Delta\theta}{P_{Losses} \cdot R_{th}} \quad (8)$$

Another approach is to consider the **SC surface**. Indeed, it is a common parameter to all SC technologies, and is directly linked to the current rating and thermal capability. Thus, a relevant FOM comes from the maximal allowed current density, called J_{max} . This FOM also depends on the switching frequency and thermal aspects of the packaging, as presented in (9)(10). As a result, and

using the losses equation expressed in (3.1.1), and from (7), J_{max} is deduced by extracting the current caliber of the SC, divided by its chip area.

$$J_{max}(f_{sw}) = \frac{-[\alpha \cdot V_t + (B_{on} + B_{off}) \cdot f_{sw}] \pm \sqrt{\Delta_{Discriminant}}}{A_{chip} \cdot (2[D \cdot R_T + (C_{on} + C_{off}) \cdot f_{sw}]}) \quad (9)$$

$$\begin{aligned} \sqrt{\Delta_{Discriminant}} = & [\alpha \cdot V_t + (B_{on} + B_{off}) \cdot f_{sw}]^2 \\ & - 4 \cdot [D \cdot R_T + (C_{on} + C_{off}) \cdot f_{sw}] \cdot \left[(A_{on} + A_{off}) \cdot f_{sw} - \frac{\Delta\theta}{R_{th}} \right] \end{aligned} \quad (10)$$

In addition, a ‘‘cut off’’ frequency is deduced from (9), to evaluate the predominance of conduction or switching losses in the frequency plane (11).

$$F_{cutOff} = \frac{[\alpha \cdot (V_t \cdot I + R_t \cdot I^2)]}{[(A_{on} + A_{off}) + (B_{on} + B_{off}) \cdot I + (C_{on} + C_{off}) \cdot I^2]} \quad (11)$$

3.2. Semiconductor Modelling

3.2.1. Different approaches

Different modelling approaches can be found in the literature to model the SC object.

The first modelling approach focuses on the internal architecture and uses the Finite Element Methods (FEM) to model physically the transistor based on its geometry, doping density and distribution of holes and electrons. Some software exist, such as GSS, MEDICI and SYNOPSIS, which can be a first way to estimate losses. These models require knowing in detail each material layer constituting the device, which is impossible on a wide range of samples. In addition, big adjustments efforts are needed on the model and it is very time consuming. And, last but not least, with this approach, the complexity of the model of the semiconductor itself may be so complicated that the external circuit (the commutation cell) may be represented as a very simple circuit. The influence of parameters such as stray inductance or damping resulting of eddy currents may significantly affect losses and other important features like voltage overshoot, so in the end it is not obvious that the most sophisticated semiconductor model is enough to obtain good prediction of the switching behaviour. Therefore, this first approach is probably not the best option for optimization.

The second option is to use an equivalent circuit to represent the behaviour of the semiconductor; this model can be linear or nonlinear, typically to represent the variation of capacitances with the applied voltage. As a nodal model, it can be used to derive analytic equations of characteristic quantities or to be connected to a nodal model of the commutation cell and obtain waveforms accounting for all the elements in a switching cell with a standard simulation software: Spice, PSIM, Saber, PLECS etc. [71], [80], [144] [145]. These methods are widely used for loss analysis because they correspond to a good balance between semiconductor and external circuit, and represent a good

trade-off between results accuracy and simulation time. In addition, other external influences can be added such as parasitic resistances and capacitances, drivers, control or routing [80]. However, and in spite of manufacturer efforts to provide these component models, they are not always available.

Our proposition, explained hereafter, is to simplify as much as possible the semiconductor definition by considering a virtual chip and by using database extrapolation and linear models. In this version, the voltage rating and the chip size can be continuously varied between the discrete values of existing devices to create virtual devices with realistic parameters (e.g. R_{dsOn} , C_{oss} , etc.). (fig 31.a).

The idea behind this concept of virtual device is to guide the optimization of multicell converters. Let's assume that we have analytic formulations of the different characteristics of a converter (envelope of the input/output spectrum, for example) involving n_S and n_P , the discrete number of cells in series and in parallel. From a purely mathematical point of view, it is possible to allow non-integer values of n_S and n_P which makes the formulation compatible with gradient-based optimization routines. Allowing continuous variation of the voltage rating and of the surface device appears as the next step to make the system 100% continuous and allow full design in a single optimization run. The aim of this approach is not to provide an accurate solution, but to give a fast estimate that can be used as a first guess for a more realistic optimization, or to address large-scale problems and provide macroscopic sensitivity models (for example, impact of the EMC standard on the weight of filters aboard an aircraft).

3.2.2. Formulation

The geometrical description to define the virtual and continuous models of semiconductors, based on the surface chip and database explorations, is summarized in (12):

$$Parameter_n(\text{Type}, \text{Technology}, \text{FOM}, \text{Voltage}, \text{Surface}_{chip}, \text{Packaging}) = Equation_n \quad (12)$$

With parameters 'Type' to 'Packaging' defined as:

- **Type** of semiconductors influences the way to operate the component, such as for instance the different (i-v) characteristics of different segment of operations between a Mosfet and a Diode [81].
- **Technology** defines the specific loss model, dependant on specific granularity and coefficient deduced from databases, as represented in the granularity diagram (Figure 34) and Chapter 2.
- **FOM** that selects the best components according to different criteria (3.1.2).
- **Breakdown Voltage**, which is somehow related to the thickness of the active region. However, modifying the breakdown voltage of a device requires a complete modification of the design (thickness of different layers, doping profiles, etc.) and it is very difficult to know how this will affect the parameters of the model.
- **Chip Surface**, which is the main geometrical information but is rarely mentioned by manufacturers. Therefore, we conducted an identification work on interesting samples by

destructive (abrasion) and non-destructive (X-rays) ways (Figure 30). An alternative is to consider the package area, with or without a filling coefficient representing the ratio between the surface chip and the case area that is derived from the identification study. For a given device, it is quite easy to determine how the chip area influences the main characteristics of the model; direct proportionality for capacitances (to apply on C_{oss} , C_{iss} , C_{rss}) (14), inverse proportionality for on-state resistance and thermal resistance (13), for example.

$$R = \frac{Coeff_R}{Surface} \quad (13) \quad C = Coeff_C \cdot Surface \quad (14)$$

- **Packaging**, calculates the specific thermal model of the semiconductor (3.3.3). We can also determine if the technology is isolated or not [82] [83].

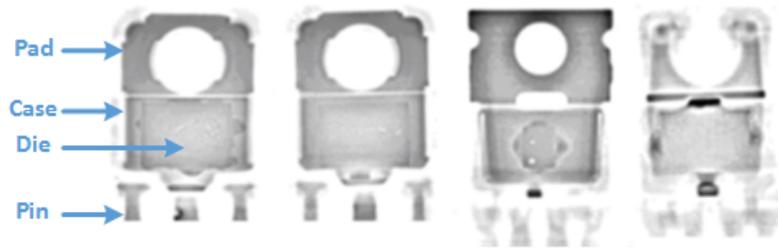


Figure 30: X-ray visualization of surface dies for different TO-220 Mosfet packages

3.2.3. Macro-Switch Object

When continuous models are not available for a specific SC technology, the “macro-switch” object can be used to provide a continuous definition of a discrete SC device (from a part number of the database). To indirectly vary the global SC voltage and surface, the “macro-switch” object proposes an assembly of “steady” chips in serial and parallel, by replacing old inputs by two new ones: n_{Ser} and n_{Par} . Thus, the definition (12) becomes (15), where both models realize the same computational operation in the end.

$$Parameter_n(Part\ Number, nPar, nSer) = Equation_n \quad (15)$$

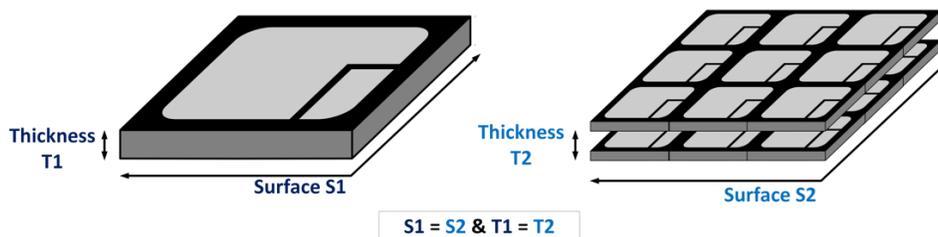


Figure 31: Main inputs parameters for a same SC object and a Macro-switch association, where the thickness is replaced by the voltage calibre in our definition

3.2.1. Benefits of this approach

There are many advantages when using continuous surface and breakdown voltages of SC devices. An assembly of devices with a lower voltage rating can give better performance than using a single device with a higher voltage rating. For example, assuming the R_{dsOn} of a Mosfet to vary as $V_{CEmax}^\alpha / Surf$ it can be seen that series connection of 2 voltage devices with half the voltage rating and half the surface gives the same total surface (2.0.5) and an equivalent ‘ON’ resistance of $2.(0.5^\alpha / 0.5) = 2.0.5^{\alpha-1} = 0.5^{\alpha-2}$. This means that if α is greater than 2 the series connection of 2 devices with half the voltage rating and half the surface is better than a single device. For low voltage MOSFETs, device physics governing the channel resistance often lead to $\alpha > 2$ [84]. In our case, we found for low voltage calibre $\alpha \approx 2.4$ (Figure 32).

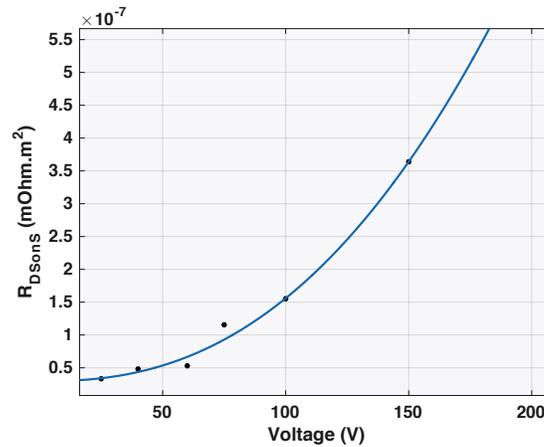


Figure 32: Calculation of the coefficient α for low calibres Hexfet Mosfets (Here $\alpha = 2.4$)

For Mosfets with higher voltage rating the bulk resistance modifies this behaviour and for other components such as IGBTs it is also more complicated; for all these cases the conclusion is not straightforward and a database approach is a better option to obtain unbiased conclusions for actual components. Parallel chips are used to increase the effective surface and so the current rating of a device. An alternative to parallel chips is to use parallel switching-cells by means of multi-level topologies. However, the switching energies in parallel circuits are directly impacted by the size of the switching circuit loop, which plays a major role in the losses of rapid components [114]. Indeed, based on the switching energy equation of (3.3.1.b), the losses are higher at low current because of the multiplication of the constant term. On the other hand, the losses are lower at high current with the division of the quadratic term. This is shown in (16) for the switching energy equation. In addition, the thermal boundaries are increased in a parallelization and the component get a higher current rating, as in (17) for the thermal resistance junction to air.

$$E_{sw}(Npar) = A.Npar + B.I + \frac{C.I^2}{Npar} \quad (16) \quad R_{th}(Npar) = \frac{R_{th}}{Npar} \quad (17)$$

Similarly, the chips of serial semiconductors allow increasing the breakdown voltage. An alternative to these chips is to use serial switching cells in multi-level topologies (8.c). Indeed, the

semiconductors of low ratings offer better conduction features and lower switching losses, which allows improving the global conversion efficiency. Nevertheless, their use can be complex because of the high number of chips (control, unbalance). An example of the macro switch model that has been created in the device library is presented in Figure 33.

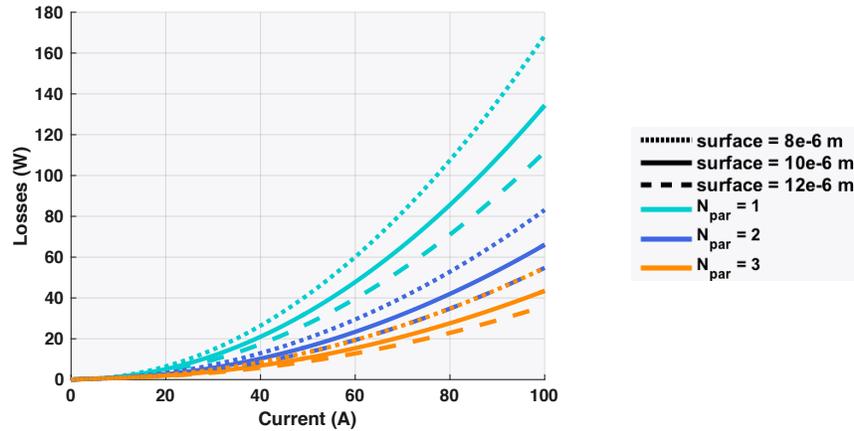


Figure 33: Calculation of semiconductor losses in a Chopper Topology ($V_{hv} = 100$ - $V_{lv} = 50$ V)
Hexfet Mosfet model level 2 as defined in the granularity (3.2.2)

3.2.2. Models Granularity

A granularity system has been established to describe the models of the SC object with more or less precision (i.e. electrical, losses and thermal models). As discussed in Chapter 2, the purpose of this work is to offer to the designers three degrees of freedom in the choice of different levels of models, from fast to accurate simulations, and a trade-off of both.

The SC granularity system, is based on a hierarchy between the different SC families and their technologies (Figure 34). The more granular the level is, the more restraint around technological similarities the selection of samples is. This system makes the model more accurate, because of the common behaviours of similar materials and internal architectures. Finally, the system created makes the transition between the different levels of precision easy, and thus simplifies the choice of the best device at the end of an optimization.

This granularity pattern (Figure 34), has been extended to the discrete SC packaging, based on their different families and technologies. It makes different descriptions of the thermal models available, regardless of the SC technology (3.3.3).

Active Part: Analytical models of Semiconductors and Cooling

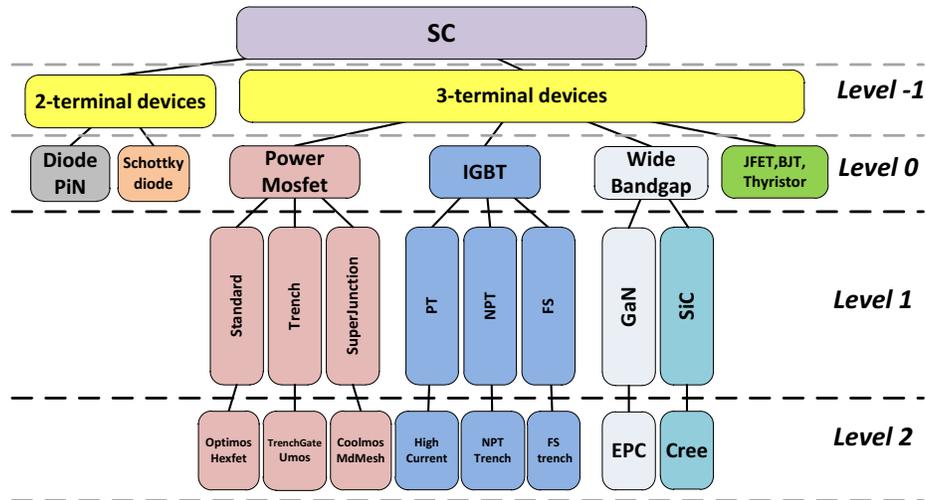


Figure 34: Granularity levels for the SC objects

Based on technological families, the different granularity levels that we propose for the SC objects are detailed below:

- **Level -1** represents the “type” in the SC definition (3.2.2). It indicates if we use a 3-terminal or a 2-terminal device, i.e. a transistor or a diode.
 - **Level 0 (System level)** considers a whole SC family (e.g. Mosfet, IGBT, WBG).
 - **Level 1 (Converter level)**, considers an entire SC sub-family (e.g. GaN or SiC for Wide Band Gap SC). Other virtual sub-families can also be used, such as groups of low and high voltage semiconductors.
 - **Level 2 (Device level)** is the most accurate family of SC. It is defined by very specific technology names (e.g. Optimos, CoolMos for Mosfets).
 - **Discrete level** uses the databases created, in order to select one or several devices. It allows to replace in an optimization the continuous models with discrete samples, or to verify the final results with real devices.

For each granularity level, we propose a related technological sorting for the current semiconductors technologies: Figure 35 for the Mosfets and Figure 36 for IGBTs.

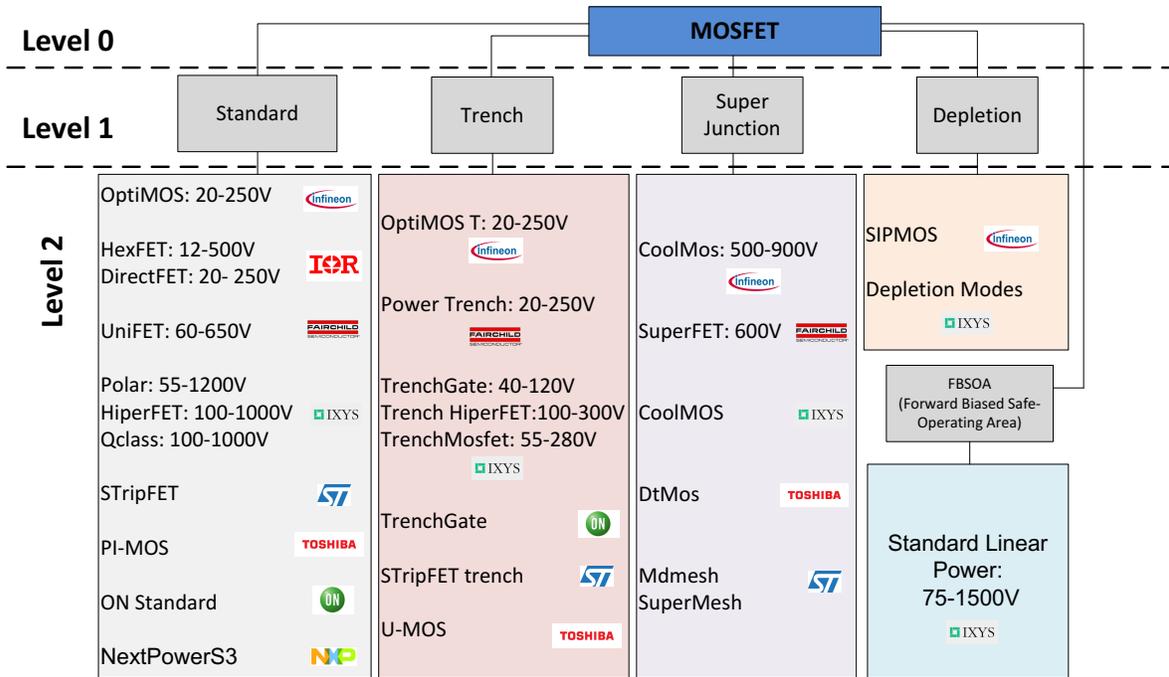


Figure 35: Classification of the N-Channel MOSFETs by constructor and commercial name (Each commercial name includes several generations)

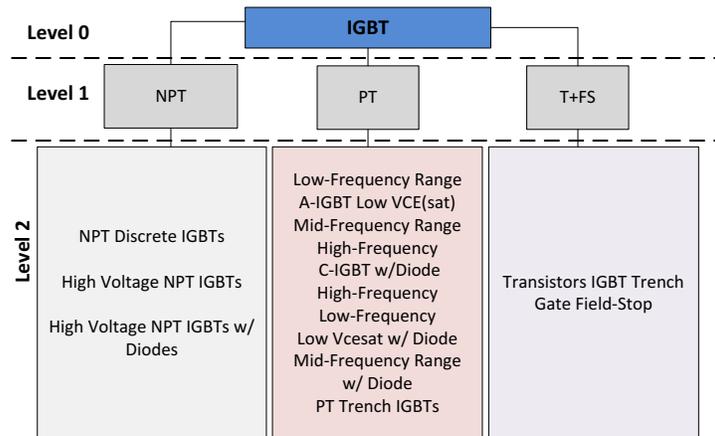


Figure 36: Classification of the IGBTs by constructor and their commercial name

3.2.3. Operation Modes

The SC model considers different internal operations, with two ways of power transfer: forward and backward. It allows considering either the transistor or the (body) diode operation (Figure 37) in order to study recovery losses. Moreover, an additional diode can be integrated in parallel in the switching cell. This diode can show better internal characteristics than the natural body diode. This principle has been made automatic to select the right loss models depending on the current direction when the macro-switch model is coupled with a solver.

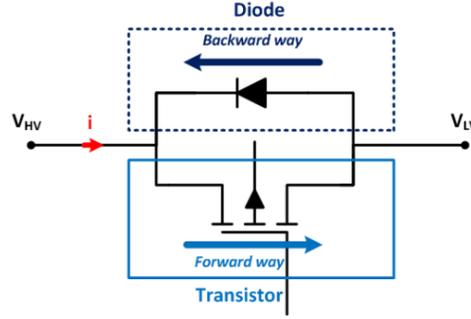


Figure 37: The two directions of operation modes in the macro-switch model: forward and backward

3.3. Multi-domain Models

Active topologies are composed of switches that control a power flow. For instance, they can adjust a voltage level by acting on the duty cycle, or even create an alternative signal. Two models are essential to represent the behavior of the switches in a pre-design approach: the loss and thermal models. We implicitly consider that the electrical model is already implemented in the electrical solver, and need not be defined here.

N.B.: Loss calculation in semiconductors has been already introduced in (3.1.1).

3.3.1. Loss Models

The first approach to create a continuous SC object, is to characterize **globally** the losses thanks to the scaling laws or dimensional equations methods [85]. These methods can be perfectly fitted for low granularity levels of SC objects. For instance, the loss can be approximated as a function of the chip area thanks to a scaling law using a sample of a database (18). Thus, when the SC losses are already known, it is possible to derive the losses of new SC objects with new surfaces. However, this kind of model is limited because it does only consider a fixed switching frequency, that is a main parameter of the converter sizing.

$$Losses^* = S^* \Leftrightarrow \frac{Losses}{Losses_{Ref}} = \frac{S}{S_{ref}} \quad (18)$$

The second approach is more accurate. It **splits** the conduction and the switching losses of the device in two different models.

a. Conduction Losses

As already stated, conduction losses of MOSFETs are mainly caused by the on-state resistance. This resistance is inversely proportional to the size of the die: the larger the transistor, the lower the R_{DSon} , and so the lower the conduction losses are [86]. The continuous model is obtained in this way, where R_{DSonS} is the specific resistance, i.e. the product $R_{DSon} \cdot Surface_{chip}$ that we need to approximate analytically (19).

$$R_{D_{SonS}}(V, Surface_{chip}) = R_{D_{Son}} \cdot Surface_{chip} \quad (19)$$

To illustrate this model, a Mosfet example has been chosen (Figure 38). It represents the best samples from the RdsOn.Qg FOM. This “conduction” model is easy to set, offers good results, and a low relative error (<5%). A dimensional equation can also be derived for lower granularity models (20).

$$R_{D_{Son}}(V) = a + b \cdot V^2 \quad (20)$$

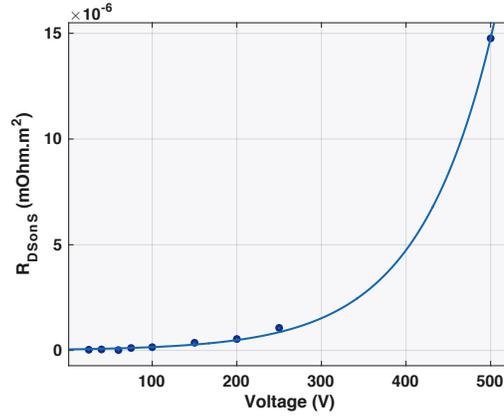


Figure 38: Specific resistance model for the best Hexfet Mosfet according to the R_{dsOn}.Q_g FOM

b. Switching Losses

Numerous equations exist in the literature to estimate the switching losses (mainly in the application notes of the SC manufacturers). An example is given in (21), with I_{dOn} - I_{dOff}, being the current of the turn-on and turn-off phases, and T_{on} and T_{off} being the commutation time of rise and fall of the drain source voltage V_{DS} (Figure 39). These equations are useful when no other information is available in datasheets, and are widely used in the industry.

$$P_{sw} = \frac{1}{2} V F_{sw} \cdot (I_{dOn} \cdot (t_{1On} + t_{2On}) + I_{dOff} \cdot (t_{1Off} + t_{2Off})) \quad (21)$$

With,

$$t_{1On} = R_g \cdot C_{iss} \cdot \ln \left(\frac{V_{gsmax} - V_{gs(th)}}{V_{gsmax} - V_{gs(p)}} \right)$$

$$t_{2On} = \frac{R_g \cdot C_{rss} \cdot V_{ds}}{V_{gsmax} - V_{gs(p)}}$$

$$t_{1Off} = \frac{R_g \cdot C_{rss} \cdot V_{ds}}{V_{gs(p)}}$$

$$t_{2Off} = R_g \cdot C_{iss} \cdot \ln \left(\frac{V_{gs(p)}}{V_{gs(th)}} \right)$$

R_g, gate resistor

C_{iss}, input capacitance of the MOS

C_{rss}, reverse transfer capacitance of the MOS

V_{gs(th)}, gate to source threshold voltage

V_{gs(p)}, Miller plateau voltage

V_{gs max}, Voltage of the driver of the MOS

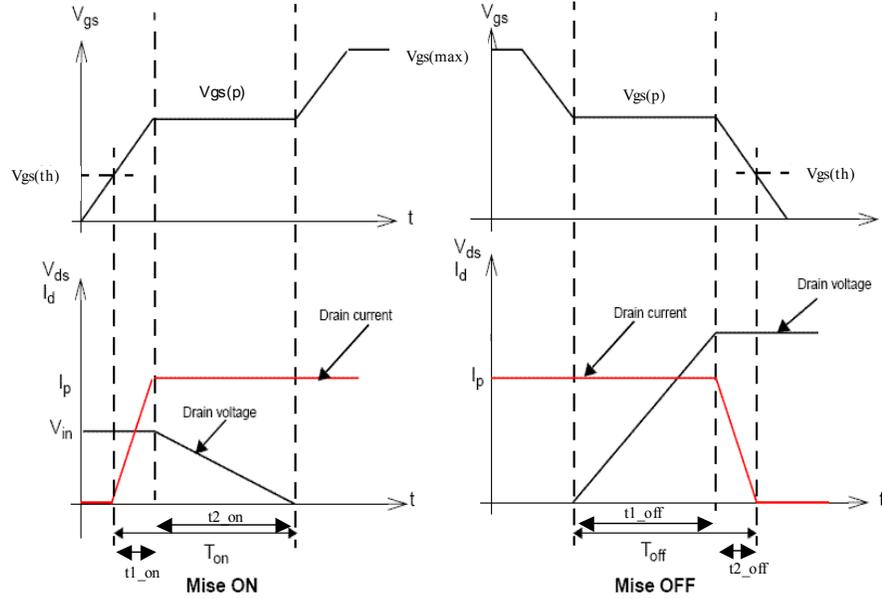


Figure 39: Commutation times of a Mosfet

In our case, these equations can be used for low granularity models with scaling laws, because they use the information of the databases, without pre-processing. However, apart from this case, we prefer to use the switching energies and their coefficients A, B and C to perform accurate loss computation, as already stated in (3.1.1).

The first approach is to create a switching loss model from the global switching energies. It has been realized with a direct multi-dimensional fit, i.e. a “response surface” of the turn-on (E_{on}) and turn-off (E_{off}) energies. Three inputs define this surface: the surface, voltage and current (22).

$$Losses_{sw}(S, V, I) = (E_{on}(S, V, I) + E_{off}(S, V, I)) \cdot f_{sw} \quad (22)$$

Indeed, for models representing wide families of samples (e.g. the granularity level 1), this approach is completely suitable, providing a better behaviour and final results than the second method explained hereafter: it is not recommended to create a switching definition too accurate for a high-level object (gathering different SC technologies). Indeed, the distribution of the switching coefficients A, B and C can be very different for different kinds of SC, which makes impossible the creation of a relevant model at this granularity.

The second approach to create a continuous model, is to link the coefficients A, B and C to the chip area, called the “switching coefficient method”. It can be done thanks to basic analytical equations based on the macro switch formulation as represented in (23) and (24). It is possible to derive from a loss analysis how the coefficients vary with the die area: coefficient A is proportional, B is constant and C is inversely proportional.

$$A_{onS}(V) = \frac{A_{on}}{A_{chip}} \quad (23)$$

$$C_{onS}(V) = C_{on} \cdot A_{chip} \quad (24)$$

Finally, the switching losses are represented as a function of the die area (with the “surface” term S) (25).

$$Losses_{sw}(V, S) = \left[(A_{ons}(V) \cdot S_{chip} + B_{on}(V) \cdot I + \frac{C_{ons}(V)}{S_{chip}} \cdot I^2) + (A_{offs}(V) \cdot S_{chip} + B_{off}(V) \cdot I + \frac{C_{offs}(V)}{S_{chip}} \cdot I^2) \right] \cdot f_{sw} \quad (25)$$

Some examples of coefficients following a direct dependency to the voltage and surface of the chip have been studied, as given in Figure 40. This approach has then been extended to the parasitic capacitances C_{oss} , C_{rss} and C_{iss} , parameters proportional to the surface and as a function of the breakdown voltage.

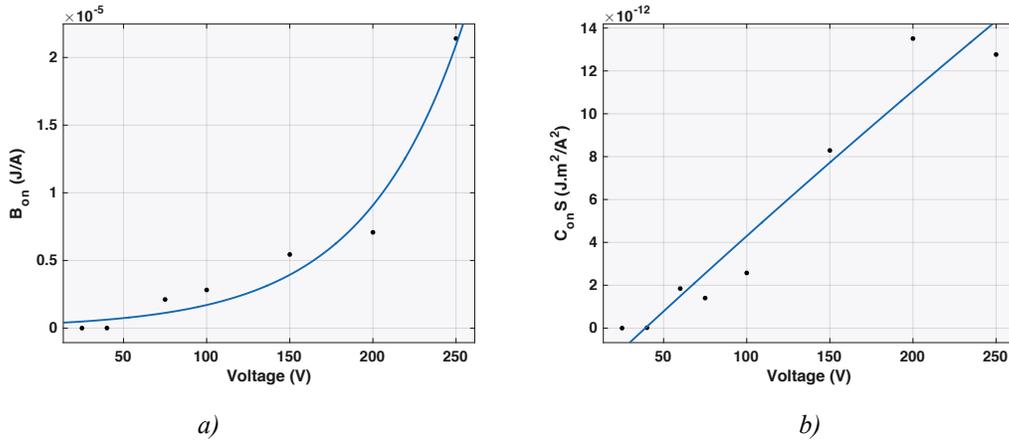


Figure 40: Example of switching coefficients regressions for Hexfet Mosfet: a) B_{on} – b) C_{on}

An example of the final switching loss model created thanks to the “switching coefficient method” is shown in Figure 41.

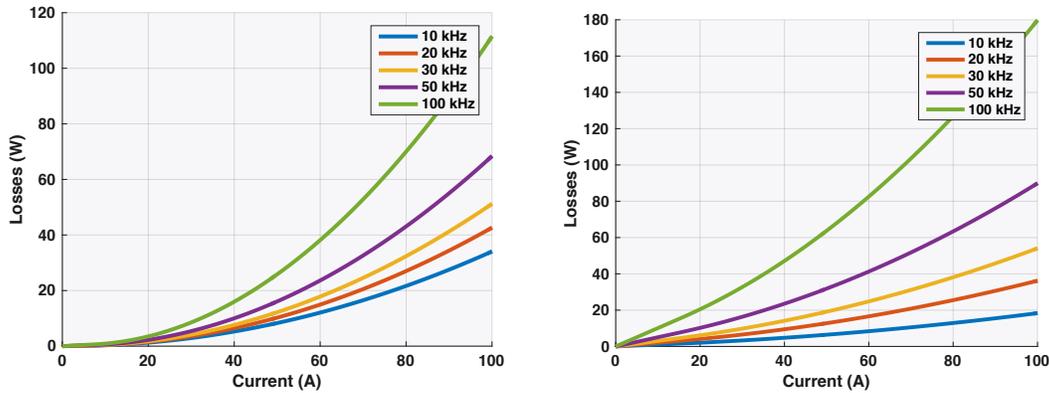


Figure 41: Example of the model behaviour for different frequencies a) GaN 60V b) SiC1200 V

To conclude, it is sometimes difficult and not obvious to find a relationship between the chip surface and the different available “switching parameters”. For instance, some samples must be rejected to build a relevant average continuous model. In addition, the “coefficients method” (25) only works for a unique family of components, or at least for very close technologies. For more general models,

we must use the method of the switching energies “response surfaces” (22), less accurate but allowing a more physical model.

In addition, the main error on the loss estimations of the SC object comes from this switching loss model. Therefore, it is very important to make the good choices of methods and samples during the creation of this model. However, it remains performing enough for the pre-design phase, as will be proven later in the global validation (3.3.2).

c. Switching energy extraction and validation

Switching energies can be found directly in datasheets for IGBT. However, they are not provided for Mosfets. To solve this problem, a simulation tool called AMIGO has been created in the laboratory to characterize the switching energy thanks to PSIM simulations and models of the parasitic elements. This tool has already been presented in [87]. This computation has been extended in this thesis to include the influence of the recovery losses of body diodes in our loss models. An example of simulations is shown in Figure 42, under the “simulation” label.

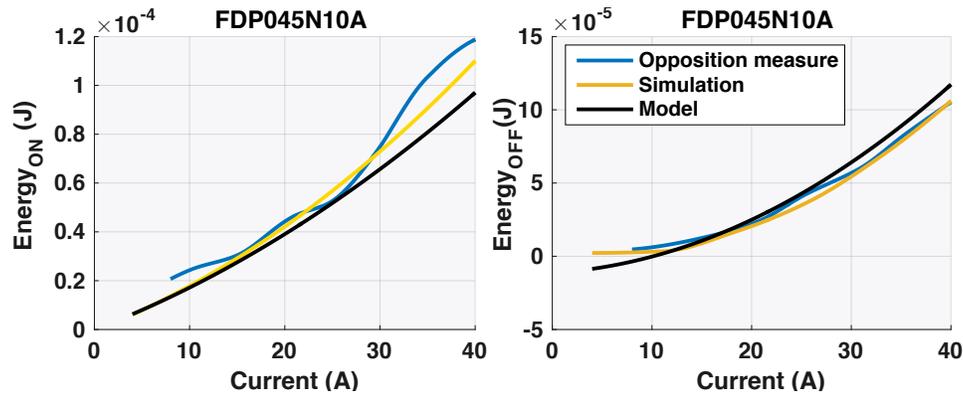


Figure 42: Simulation tool results compared to the experimental opposition method on FDP045N10A samples; $Opposition = real\ measurements - Simulation = AMIGO\ software\ computation - Model = Continuous \ \& \ analytical\ equation\ for\ the\ switching\ losses$

To validate the results of this simulation, two methods were available: the double-pulse method and the opposition method. A comparison of these methods is detailed in [79] and [88]. Because of its advantages (theoretically sound, non-invasive, easy to set up, no need of specific probes, etc.), the opposition method has been chosen here.

Some of the best Mosfets of our database have been tested in the Opposition bench (Figure 43). The aim was to characterise the Mosfets, to integrate the best ones in a converter prototype, but also to evaluate the accuracy of the simulation-based approach. One example of measurements is given in Figure 42 (other samples are already presented in [16]), with the “opposition” label. The results of this comparison are very positive as the simulations match experimental tests on a wide operating range (until 40A). More details and validations of the opposition method have also been presented in [5] and in [89] for GaN technologies, where the experimentation also validates this

approach. In addition, there is a good correlation between the continuous model presented in Figure 42, under the “model” label, and the measurements and simulations.

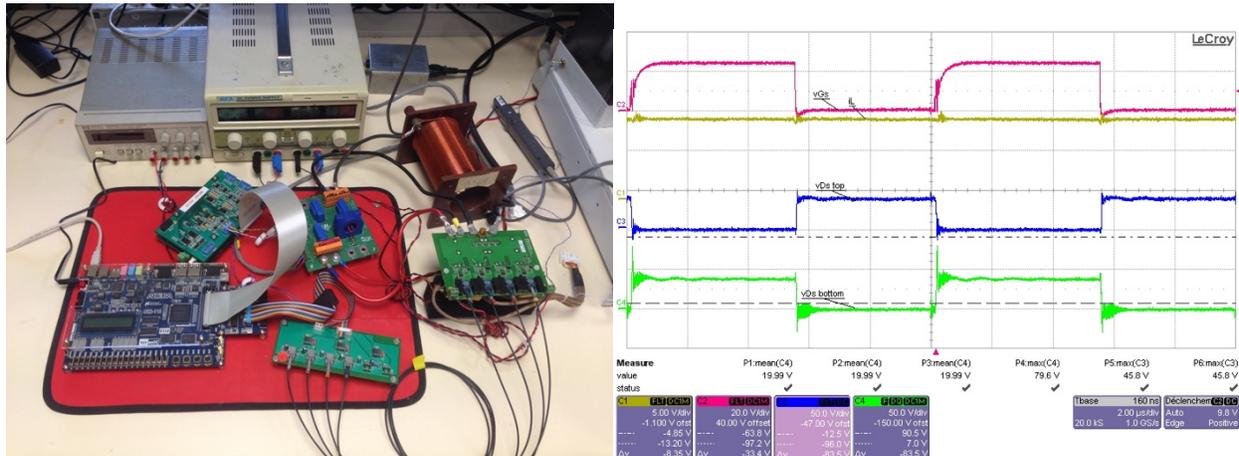


Figure 43: Opposition methods experimentation

3.3.2. Global Validation of the losses models

The purpose of this section is to validate a complete loss model by comparison with the database devices. We have chosen the global Mosfet model (Granularity Level 1) for this demonstration. Two methods are available to fit the physical models with our computational tools: the **interpolation** and the **regression methods**.

Because the SC data (e.g. the required parameters for the models such as specific R_{dsOnS} or the specific switching coefficients) are mainly increasing or decreasing as a function of the voltage during the curve fitting of the model parameters (i.e. when we want to find equations of the SC behaviour) the **interpolation** approach can be used to create the analytical model. The interpolation is linear by part, which allows creating “continuous by part” models, **without error** when the final model is compared to the original samples selected for the curve fitting. In our classical gradient algorithms, these models propose a very interesting alternative to minimize the errors of models, with a good and quick convergence. Indeed, we did not see any problem during the computations, compared to classical continuous and linear models. In addition, this approach is very well-managed to build models thanks to the Matlab software functions.

However, it is not always possible to use this approach, because of the possible bad data distribution during the curve fitting (according to us, a bad distribution is when the data is not linearly increasing, with many discontinuities in the data due to the chosen samples). Therefore, we need to validate the regression approach in this demonstration. However, in the case of the global Mosfet object that has been chosen here, the interpolation method remains available to create a highly accurate loss model from the database (error is null).

Thus, the second approach to create continuous models is the **regression**. Contrary to the interpolation, the regression proposes an average continuous model among the selected samples, implying a **relative error** that needs to be quantified.

To perform a relevant curve fitting on the selected samples from our whole Mosfet database, (no matter what fit method is used), the best two Mosfets have been selected on the most representative voltage ratings, according to the $R_{dsOn} \times Q_g$ FOM (Figure 44). Here, we arbitrary decided that a representative family have to reach the criterion of 400 samples/voltage calibre. The main identified families are the Hexfet, Optimos, MdMesh and CoolMos technologies, because of the database we created. This selection by “most representative” voltage calibres allows to avoid the minor families and devices that are not common on the market because they are less performing or lack of industrial interest. Thus, the data distribution of the physical characteristics during the fit (as a function of the chip surface and voltage in our case) obtains a better quality to create the different average model we need to model a semiconductor device.

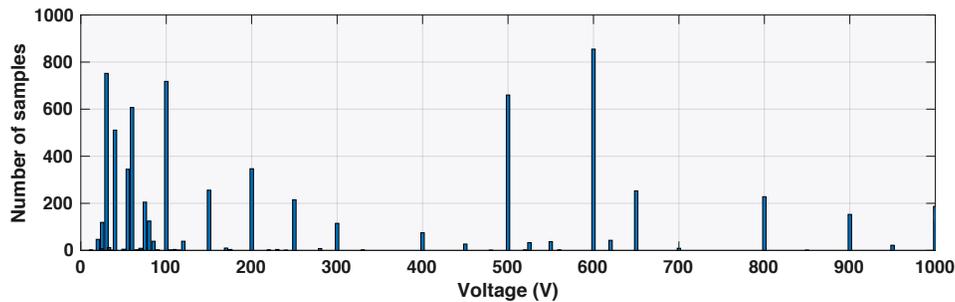


Figure 44 : Mosfet repartition in our database as a function of the breakdown voltage

Finally, once the regression model has been created for the best Mosfets of our database, a sensitivity study has been processed on the loss models created by changing the duty cycle (for conduction losses), the frequency (for switching losses) and the handled current (Figure 45), to finally obtain a maximum relative error of roughly 20%. By creating a global object of the GaN technology (Granularity level 1) and performing the same study, we got equivalent results, slightly better due to a narrower range of the SC samples studied. From the previous and individual validation of the conduction and switching losses presented in the chapter, these figures illustrate the sum of the relative errors for these both loss models.

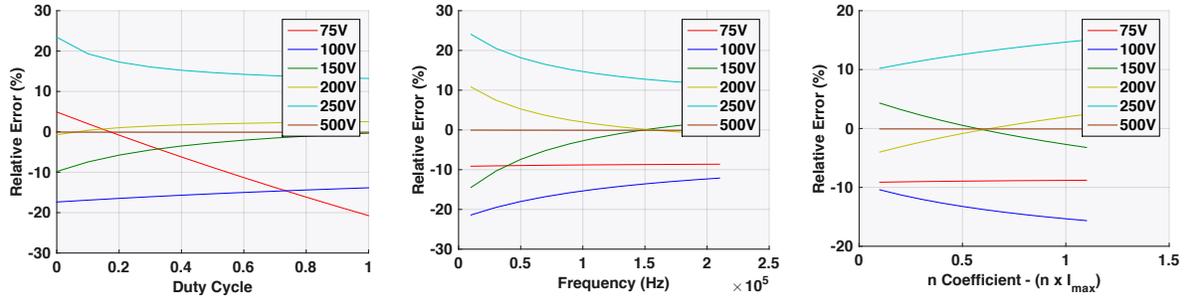


Figure 45 : Sensitivity study on the relative error of the model 1) Duty cycle Impact @ I_{max} and $F_{sw} = 100^{\circ}3$ - 2) Frequency Impact @ I_{max} and $D = 0.5$ - 3) Current Impact $D = 0.5$ and $F_{sw} = 100^{\circ}3$

As a conclusion, these global loss results have an acceptable relative error to compute a pre-design and allow fast explorations in terms of topology and ratings. In addition, the more reduced the selection in terms of technologies and characteristics, the lower the error of the regression. Thus, when samples are well selected thanks to technological sorts, figure of merits, main devices of the market selection, the error reached is less than 20% for an object with a level 2 granularity.

3.3.3. Thermal Model

As presented in the introduction, numerous packages of SC exist in power electronics (Figure 46). Their different performances [65] [66] have to be evaluated in our designs. Thus, the objective of this section is to build a continuous model to evaluate these different packages. The thermal model of SC described here relates to the physical description of the package (dimensions, material, layers, etc.), and then to the definition of its thermal resistance(s). Numerous approaches are possible to create this model, and we consider two distinct situations:

- Either a single chip in a discrete package (COTS devices). Such models are described hereafter;
- Or several dies integrated in the same substrate (power modules). Such models are exposed in part B of this chapter (Cooling – Part B).

DPAK (TO-252)		Reverse DPAK (Rev. TO-252)		DPAK 5pin (TO-252 5pin)		D ² PAK (TO-263)		D ² PAK 2pin (TO-263-2)		D ² PAK 7pin (TO-263 7pin)	
3	9.9 x 6.5 x 2.3	3	9.7 x 6.6 x 2.34	5	9.9 x 6.5 x 2.3	3	15.0 x 10.0 x 4.4	2	15.0 x 10.0 x 4.4	7	15.0 x 10.0 x 4.4
											
SO-8/SO-8 dual		SO-16/12		SO-14		SO-16		SO-18		SO-19	
8	5.0 x 6.0 x 1.75	12	10.0 x 6.0 x 1.75	14	8.75 x 6.0 x 1.75	16	10.0 x 6.0 x 1.75	18	12.8 x 10.3 x 2.65	19	12.8 x 10.3 x 2.65
											
SO-20		SC59		SOT-23		SOT-89		SOT-223		SOT-323	
20	12.8 x 10.3 x 2.65	3	3.0 x 2.8 x 1.1	3	2.9 x 2.4 x 1.0	3	4.5 x 4.0 x 1.5	4	6.5 x 7.0 x 1.6	3	2.0 x 2.1 x 0.9
											
SOT-363		TSOP-6		S308		TISON (power stage 5x6)		WISON (power stage 3x3)		SuperSO8	
6	2.0 x 2.1 x 0.9	6	2.9 x 2.5 x 1.1	8	3.3 x 3.3 x 1.0	8	5.0 x 6.0 x 1.0	8	3.0 x 3.0 x 0.8	8	5.15 x 6.15 x 1.0
											
SuperSO8 dual		SuperSO8 fused leads		VSON (ThinPAK)		CanPAK™ S-Size		CanPAK™ M-Size		TDSON-10	
8	5.15 x 6.15 x 1.0	8	5.15 x 6.15 x 1.0	4	8.0 x 8.0 x 1.0	6	4.8 x 3.8 x 0.65	7	6.3 x 4.9 x 0.65	10	3.0 x 3.0 x 0.9
											

Figure 46 : Example of some main external packages for the Mosfet semiconductors
(Source: Coolmos Infineon – Application Note 600VCoolMOS)

a. Physical Approach

Firstly, a “physical equation” has to be written, that defines the thermal model thanks to the geometry of the case and its material description. The thermal model of discrete packages can be simplified by the calculation of two main equivalent resistances to estimate the thermal conduction: the junction to case resistance R_{thJC} and the junction to ambient resistance R_{thJA} . These thermal conduction phenomena, are easily computable thanks to simplified physical equations using 1-D or 2-D heat directions in a flat support. These equations use different granularities depending on the hypothesis:

- Firstly, when the distance travelled by the heat flow “L” is very small, a 1-D thermal resistance can approximate the simplest model (26), with k being the thermal conductivity and S the chip surface.
- Then, when “L” becomes not negligible, the model must consider edge effects by means of a 2-D thermal propagation model. One classical approach is to assume that the heat flux spreads linearly, in a uniform section area, and that it is characterized by a cone angle α . and a surface = $a.b$, with $a < b$. (27)
- The third representation is certainly the closest to the semiconductors behaviour in a conductive support. It considers that the heat flow does not spread linearly from the heat source, but radially thanks to a spreading resistance (28). This spreading resistance description is largely developed in part B of this chapter (Cooling – Part B).

$$R = \frac{L}{k.S} w \quad (26) \quad R_{th} = \frac{1}{2k(b-a)} \cdot \ln\left(\frac{b}{a} \cdot \frac{a + 2w \cdot \tan \alpha}{b + 2w \cdot \tan \alpha}\right) \quad (27) \quad R_{th} = \frac{1}{4\pi \cdot k \cdot L} \ln\left(\frac{S'}{S}\right) \quad (28)$$

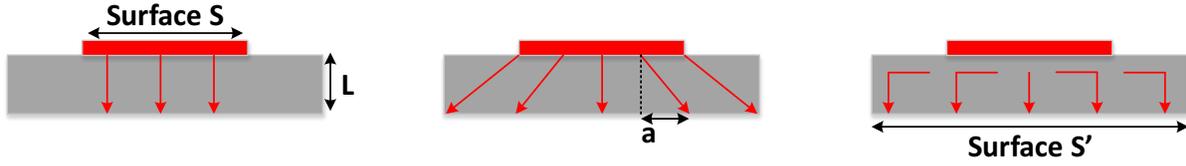


Figure 47: Physical models representing the thermal resistance of a discrete semiconductor package

The last solution to get a thermal model through a physical approach is to calculate the resistance of each layer of the package (Figure 48). The aim is to create a nodal model that can then be solved with any nodal network solver. Nevertheless, it is often difficult to find all the architectural information of the SC devices, which limits the use of this method.

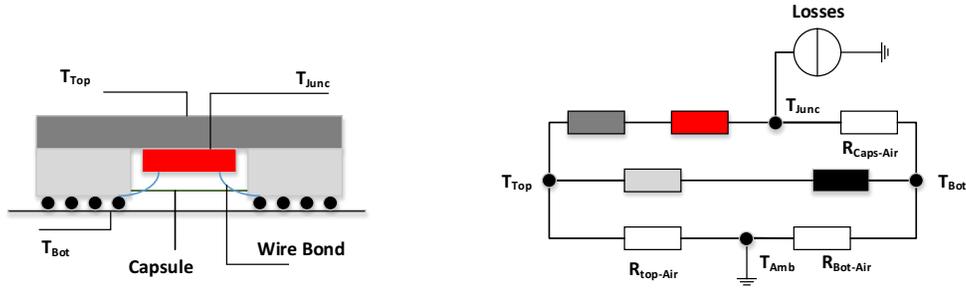


Figure 48: BGA package model represented as under an electrical formalism

To conclude on the physical definitions, these models imply numerous hypothesis of the internal architecture and effects of the thermal packages. As a result, a high number of relative errors may occur (up to 50% for TO-220 when compared to our database). Therefore, they are only used in low granularity models or when data is missing in the database. In other cases, the database approach has been preferred because of its equivalent simplicity and higher accuracy.

b. Database Approach

Discrete SC packages are very diverse and possess technological specificities that the previous “physical models” cannot represent. Thus, with an approach like the loss model (including a granularity), models of the thermal resistances as a function of the chip surface (or package surface) have been created. It is also based on a scaling approach (29).

$$R_{TH}(Surface_{chip\ or\ case}, V) = \frac{R_{THSpe}}{Surface_{chip\ or\ case}} \quad (29)$$

Firstly, models based on the **package area** have been tested, because this data can easily be extracted from the database when the name of the discrete package is known. Indeed, packaging dimensions are always mentioned in datasheets. The hypothesis is that the SC chip fills in all the package. This method provides good first estimations for pre-design studies, as shown in Figure 49

for different examples of Mosfet packaging. For instance, an average error of 3,2% has been obtained for the Mosfet packed in TO263 and 3,4% in TO-247.

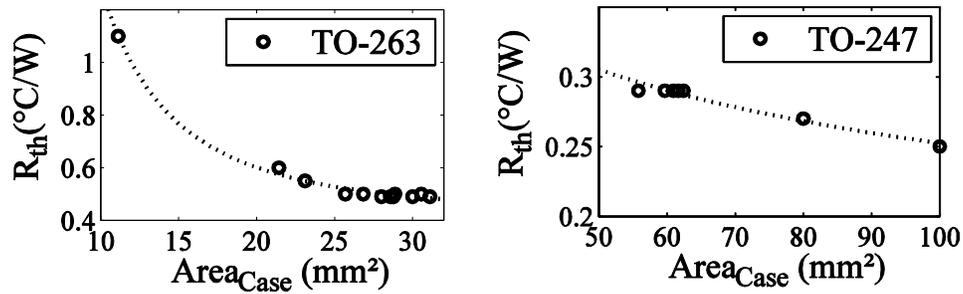


Figure 49: Examples global thermal resistance models of our Mosfet database, as a function of their packaging type and package surface

However, in order to improve the accuracy of the results, the **chip area** has to be considered in this thermal model (and if possible, the ratio between the chip area and the package area, as it influences directly the heat flow in semiconductors devices (3.3.3.a) (Figure 50)).

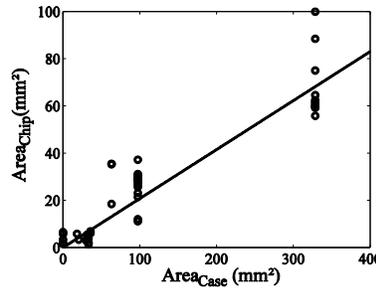


Figure 50: Average evolution of the Area Chip as a function of the Area Case for a selection of the best SC with the criterion $R_{son} \cdot Q_g$

Thermal models have also been created, directly based on the SC technologies, by mixing different technologies of packages for a same SC type. The purpose was to get relevant thermal models for the specific families of semiconductors that are integrated in different packages, as for the global Mosfets model in Figure 51.

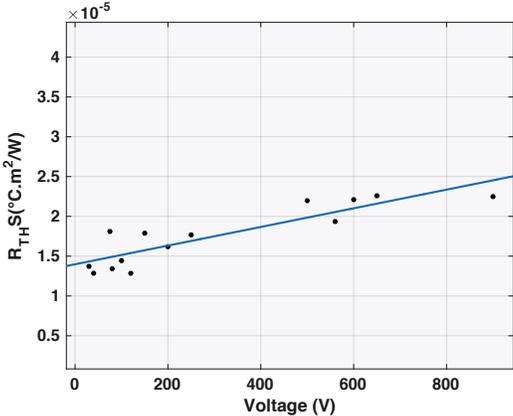


Figure 51 : Specific thermal resistance for the best Mosfet as a function of the voltage according to the FOM $R_{dsOn}\cdot Q_g$

Or on the contrary, we can also consider only the packaging technologies, and create different families as shown in Figure 52 for the Mosfets or our database.

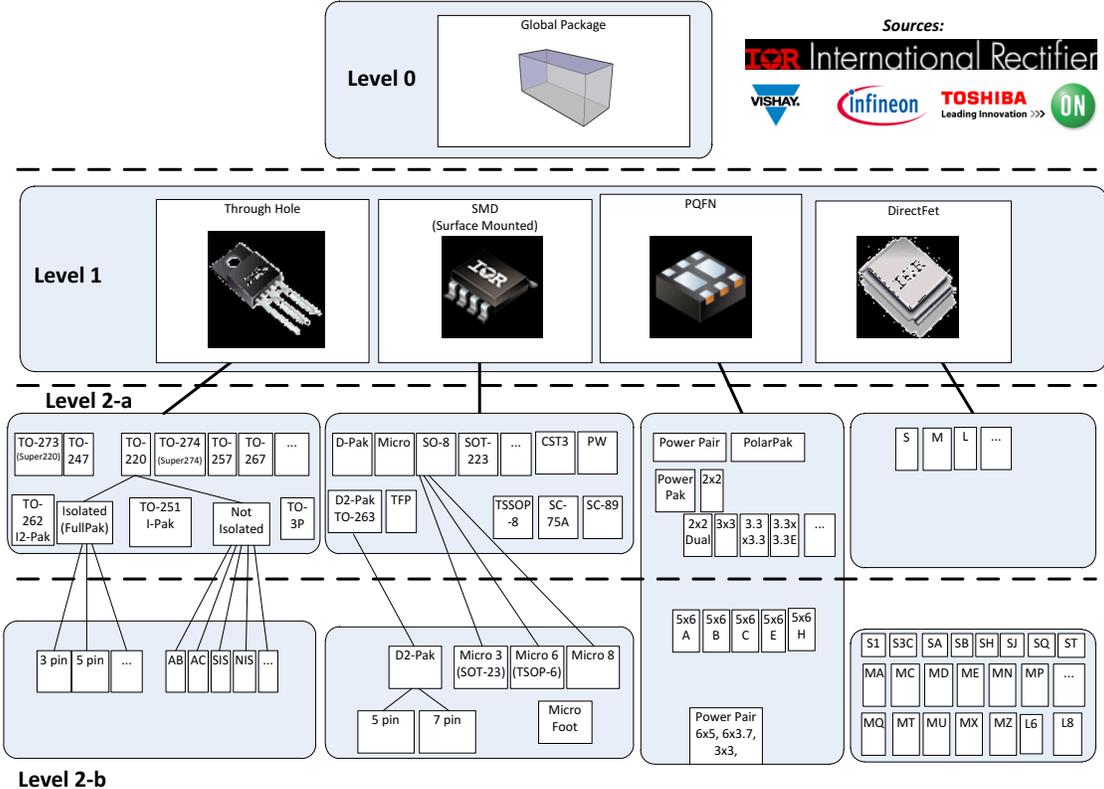


Figure 52: Proposition of a classification for the main Mosfet packages

As examples, we can consider a precise family of thermal packages, like the Though Hole Family (gathering all the TO 2XX references, and equivalent to a level 1 granularity for the thermal model) as shown in Figure 53-a ; or to consider a very precise reference of thermal package, like the TO-263 as shown in Figure 53-b.

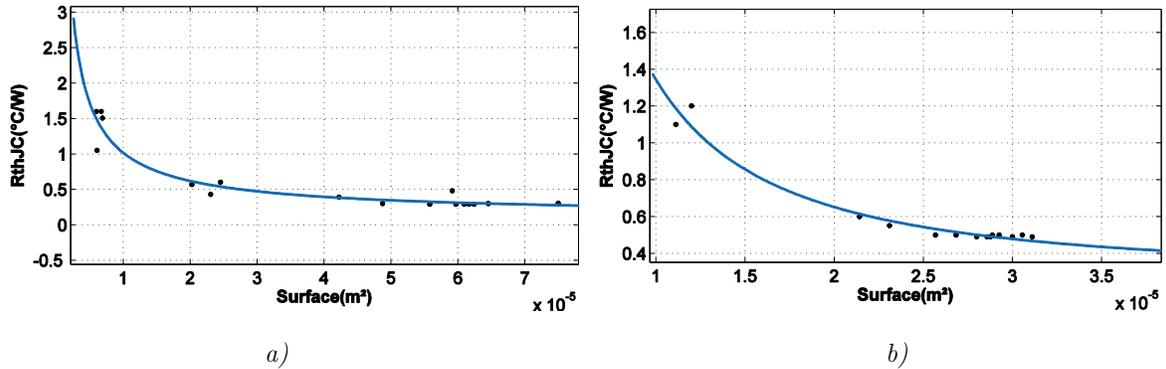


Figure 53: a) Thermal resistance of the Through hole package family as a function of the chip surface
 b) Thermal resistance of the TO-263 package family as a function of the chip surface

For isolated packages [82] [83], this model can be extended as a function of the breakdown voltage, sustained by the SC. This voltage is proportional to the thickness of isolation, and so to the thermal conductivity (Average error for TO-220FP: 8.5% and for ISOPLUS247: 4.1% with details in Table 5). Finally, the thermal model of the SC is achievable from database regressions. It presents good results, regardless of the hypothesis taken. Once again, an interpolation is possible when a good selection of samples is selected, to get a highly accurate and linear-by-part model.

Voltage (V)	TO220 Rth _{datasheet}	TO220 Rth _{computed}	Relative Error (%)	Voltage (V)	TO247 Rth _{datasheet}	TO247 Rth _{computed}	Relative Error (%)
100	1,6	1,76	10	75	0,29	0,28	-2
100	0,57	0,52	-8	100	0,29	0,30	3
120	0,43	0,46	7	150	0,29	0,29	-1
500	1,6	1,84	15	200	0,29	0,32	10
560	0,601	0,57	-5	250	0,29	0,29	1
800	3,6	3,40	-6	560	0,2998	0,31	2
				650	0,3012	0,28	-8
				900	0,2998	0,32	8
				1200	0,51	0,50	-2

Table 5: Validation of the Isolated package models for the TO-220FP and ISOPLUS247

To conclude, we prefer to use the database approach to create our models, because it is easier to set and gets more accurate results. As a notice, the results that can be here obtained are similar to the conduction loss model (close to 5% of relative error), also based on a resistance model (i.e. the on-state conduction resistance – (Part 3.3.1)).

3.3.4. Cost Model

The SC cost model comes from a combination of manufacturing processing steps and R&D efforts. However, the raw material has a negligible influence on the final price [90] and different methods exist to create cost models based on database extrapolation [91]. Numerous studies present the linear increase of the semiconductor price as a function of the chip size (Figure 54).

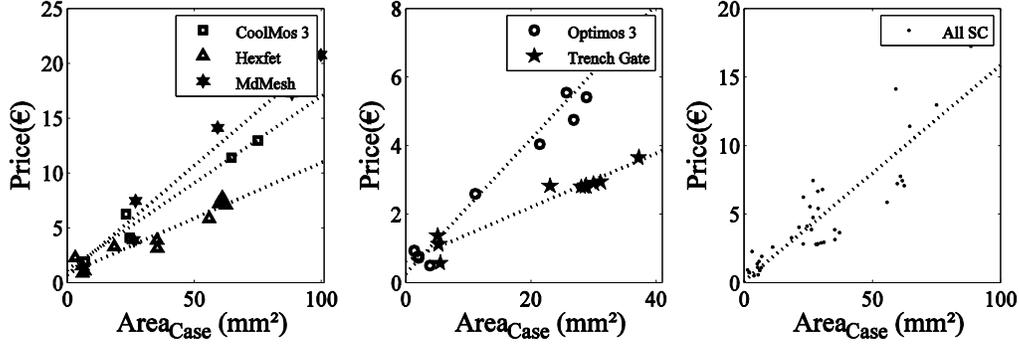


Figure 54: Price as the function of surface area for specific technologies of semiconductors in a same range of voltage

In our model, two factors determine the cost of the semiconductors: the chip size and the packaging price. A first equation has been written, using on the one side the specific price per chip area, and on the other side, the R&D, production costs, and global packaging price (bonding, soldering, integration) (30).

$$Price_{SC} = Price_{chips} + Price_{pack/R\&D} = \sum (Price_{speChip(x)} \cdot Area_{chip(x)}) + Price_{pack/R\&D} \quad (30)$$

Usually, the chip price is linearly proportional to its size. In our case, we have used data from internet sellers (MOUSER). Through regression, the average error found is 20% for the global Mosfet data and 30% for the GaN data.

Moreover, the Minimum Order Quantity set by the industry had to be considered, even though it is a non-physical factor based on commercial considerations. Thus, a proposition has been to add on the previous equations a global factor k_{MOQ} representing this MOQ (31) (Figure 55-b).

$$Price_{Final\ SC} = k_{MOQ} \cdot Price_{SC} \quad (31)$$

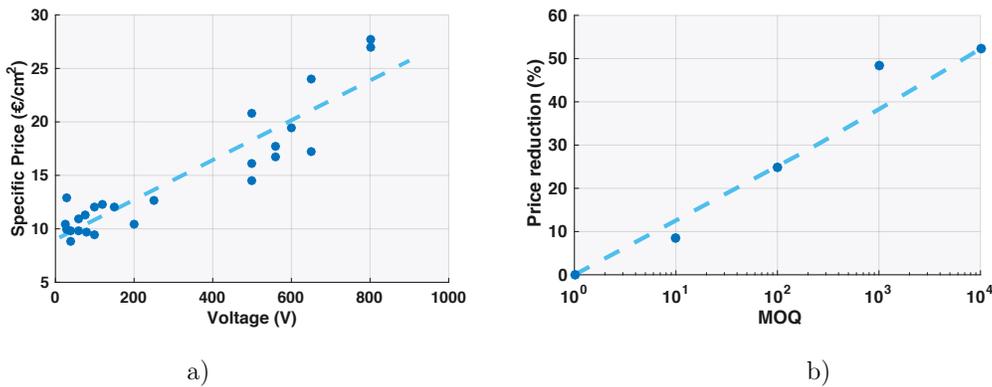


Figure 55: a) SC Specific price model as a function of the voltage
b) % of the SC price reduction as a function of the MOQ (from MOUSER data)

Another input that is interesting in the virtual prototyping is the year of release. Indeed, some studies give us projections of the future prices for different technologies, which helps designers to

take decisions and guide their work. In addition to the performance results, the price can be approximated for a period of up to 10 years, which is a precious information in the industry to get projections (Figure 56). As a conclusion, a cost model has been created with simplified and macroscopic equations on the semiconductors.

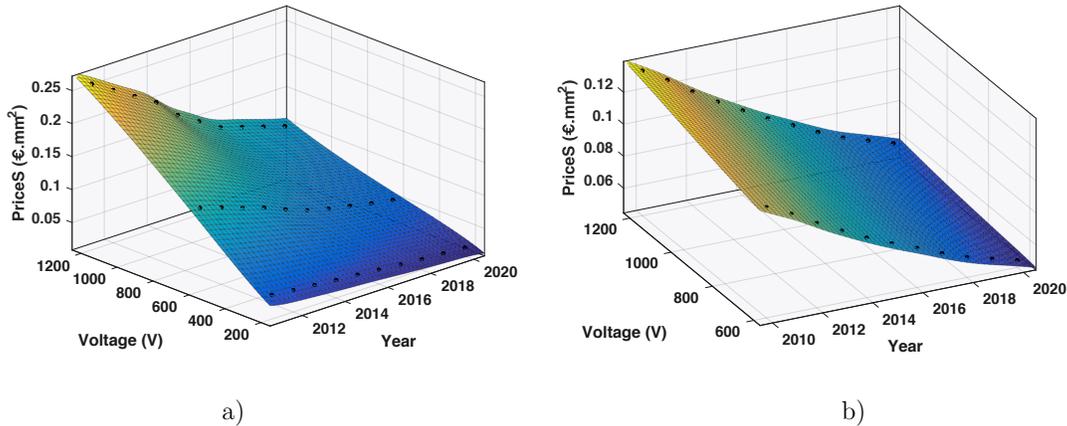


Figure 56: SC Specific price as a function of the voltage and year of release
 a) GaN b) Mosfet SiC (from Airbus data)

3.4. Conclusion

In this chapter, a global method has been proposed, aiming at creating analytical and continuous models of any type of semiconductors, according to different granularities and packaging. These models are mainly based on the chip area, as it defines the main electrical, loss and thermal parameters of a semiconductor device. Nevertheless, this method requires the creation and update of huge databases, which is a difficult work because of the variety of parameters provided by each manufacturer, rarely well standardized in datasheets, and because of the frequent technological evolutions and commercial updates.

Another challenge is to select the best components in the database, in order to create the most suitable model dedicated to converters optimizations. Thus, several FOM have been created, including some that match with our work as they consider the chip surface and thermal parameters.

Moreover, information is missing most of the time (chip area, on-state resistances for IGBT, switching energies for Mosfets, etc.). Therefore, substitution methods have to be found. As an example, an X-Ray investigation has been realized to measure the chip surfaces. Similarly, the switching energies of Mosfets have been simulated based on datasheet information. Thus, the database has been completed, relevant curve fittings have been created, and so the analytical equations for the SC object have been obtained. However, filling in the data can induce errors, and this work has to be as accurate as possible and standardized in order to optimize the modelling.

Although the proposed modelling method depends directly on the quality of the database used, it shows that a very simple and quick approach is possible to create and maintain semiconductor

models in the pre-design phase. Finally, good results are obtained on the global loss and thermal models, which has a direct impact on the sizing of the cooling system, discusses in the following part. To keep improving the encouraging results of our study, larger databases should be investigated to refine the proposed models by studying more types and families of components.

Part B: Cooling

Losses in a static converter are mainly generated by semiconductors. They imply two main consequences: they define the performance of the converter topology in terms of efficiency, and they generate local heating. Thus, the losses have to be transported and evacuated by a cooling equipment in order to maintain an acceptable temperature in the system and avoid thermal damages. In addition, with the increase of the power densities in power electronics, these losses are more and more concentrated on small areas. As a result, new devices are required to evacuate the losses efficiently. Therefore, the cooling system becomes a dimensioning element of the converter that has to be wisely selected and optimized. In most cases, the cooling systems are limited to the SC devices, but they can also be applied to more elements like magnetics components (sometimes a main source of heating). Moreover, many solutions are available to cool down a converter, depending on the amount of power to cool, the domain of use (industry, aeronautics, domestic, etc.), or the converter's own specification. Therefore, it is important to get a performing modelling of the cooling, in order to choose the right devices and optimize them, to finally improve the system power density.

Firstly, this chapter presents the cooling technologies applied in power electronics, and details their limits in the aeronautical context. Secondly, the thermal model principle of a cooling system and its formulation are exposed. This approach is shared by any cooling device, in order to transport and evacuate the thermal calories outside the power conversion. In addition, the method is created for one or several heat sources (e.g. one or many SC chips on a same base plate). Then, a criterion of comparison (FOM) is proposed to evaluate the performance of the cooling and select them in a database. Thirdly, the details of the thermal models of a classical straight-fin heatsink are provided, in natural and air-forced convections. Some granularities are created to define the models, from a global definition of the device to the modelling of its parts by different models (i.e. base plate + array of fins). To finish, some validations have been led to illustrate these models through empirical tests and simulations, before concluding on the global modelling work and its validity

3.5. Technological Review

Different technologies exist to cool down the hot spots generated during the static converter operation. A study has been created to identify the main technologies of cooling devices that are available in power electronics, especially for high power applications. They have been and classified by the type of physical media used (air, liquid and two-phases).

3.5.1. Air Cooling

The air cooling solutions are represented in power electronics by the use of heatsinks. These devices gather a base plate and an array of plates (or pins), in order to increase the exchange surface and maximize the power transfer between the heat source and the air. The heatsinks have different shapes, as shown in Figure 57, which possess their own advantages and drawbacks, as detailed in [92], [93] and [94]. Hence, a design trade-off is required to select the best geometry according to the

application. Indeed, the fins (or pins) may be in-line or staggered, with different shapes (square, circular, elliptical) and different form factors (straight or cross-cut). As an example, curved fins help to guide the flow and improve the heat transfer, while straight fins increase considerably the airflow inside the internal channels. On the other side, pin fins increase the surface area. But they also increase the mass of the heatsink with the risk of a fin oversizing, which may cause an important pressure drop [95]. To break the boundary layers and increase the heat exchange, it is also possible to pierce the fins or create surface imperfections. Moreover, by threading the bottom of the fins (U-shaped), the heat to exhaust can be considerably increased.

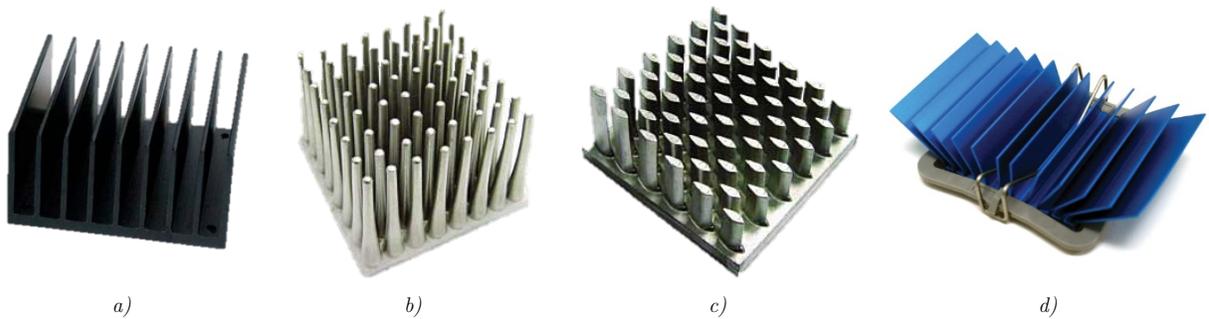


Figure 57: Main air cooling heatsink form factors: a) straight parallel fins b) Cross-cut inline round pin fins c) Staggered elliptical pin fins d) Curved parallel fins

In power electronics, these heatsinks are mainly used in a forced convection, while the natural convection is applied to low power applications. However, the forced convection can cool down a limited amount of power, and some requirements can limit its efficiency, like its maximal flow rate or pressure drop in avionic systems. Therefore, the forced solution may be excluded for some high-power applications and so, other cooling systems have to be considered, such as the liquid cooling.

3.5.2. Liquid Cooling

A liquid-cooling system is often composed of a cold plate crossed over by a specific liquid optimizing the thermal exchange – usually glycol (Figure 58) – through a hydraulic network composed of a pump, valves and a deported exchanger. Other new integrated solutions can also be directly implemented in power modules, such as a liquid-cooler with plates and coolant flows [96].



Figure 58: Airbus Water Cold Plate, optimized for the cooling of 10 power modules including two loops of folded fin technology

Although the liquid solution offers more efficient perspectives in terms of thermal management, it is interesting to note that actual studies in aeronautics focus on air-forced solutions (coupled with Heat Pipes or not). Indeed, the high promises of the new wide band-gap semiconductors (less losses, more integration,) reduce the need of very efficient cooling systems. However, these chips are smaller and smaller, involving more concentrated hot spots. Thus, new spreader technologies could be required to evacuate the concentrated calories (like heat pipes), which can be coupled with heatsinks. With these new devices, it will be possible to remove the classical hydraulic networks in aircraft, as expected in the MEA concept (Chapter 1). As a reminder, air systems remain less heavy and costly, have more reliability, are easy to install, and require less maintenance. Nowadays in aeronautics, trade-offs at a system levels are required to choose between liquid and air solutions (with or without spreaders).

3.5.1. Two-Phases Cooling

The last alternative relates to the Heat Pipes (HP) and Loop Heat Pipes (LHP). Their goal is to spread more efficiently the hot spots in the power electronics systems. They are also named “two-phase” exchangers because a two-phase flow is present under various forms in the device. As an example, an external heating may cause transient flows to transition from pure liquid to vapour flows. This flow optimizes the transfer of calories from one point to another, but requires a thermal exchanger to evacuate these calories. In addition, these systems mostly run in close loops, with or without a pump, and can be totally autonomous.

These devices have been successfully used in the last decades for the thermal management of a variety of applications in aerospace [97]. Their main benefits are the mass effectiveness and the stability in high temperatures. They can transport considerably more heat per fluid mass, resulting in lower system mass and smaller cooling tubes. Their main disadvantages are that they need to evacuate losses somewhere (and so an exchanger like a heatsink has to be used), their gravity dependence, the inflexibility of their evaporator [98] and their price. Other innovative developments derive from classical (L)HP, such as the pulse-LHP, or integrated thermoelectric effects leading to energy harvesting.

3.5.1. Choice for the modelling work

The three previous cooling strategies are very interesting in the pre-design scheme. In the aeronautical context especially, their analysis allows to establish comparisons and trade-offs on specific electrical systems. Thus, they should all be modelled in a library.

However for now, our modelling work has only focused on the air solution, and more precisely on the parallel and straight fins heatsink geometries (Figure 57-a). It is the simplest form to implement and describe physically in a modelling work. Thus, it is a good basis to start the creation of thermal models and objects in our optimization platform. In addition, this solution is favoured in the More Electrical Aircraft, and thus has to be our priority. Nevertheless, the straight-fin heatsinks do not necessarily dissipate the highest powers when they are bought on shelves. They have to be

customized and optimized, mainly with an optimal ratio (fin height/channel width) at a given pressure drop. Thus, a complete model has been created to entirely custom this thermal device.

Nevertheless, some other models are available in our library, describing a liquid-cooling base plate and a loop heat-pipe spreader and aiming at estimating their thermal models. However, no validation and no use of these models have been developed. Therefore, we will not present this work here.

3.6. Cooling Modelling

In this section, we propose to develop the theoretical foundation of the cooling model. The objective is to build step by step the different models of cooling, by stating the thermal principles, figures of merit and device geometries.

3.6.1. Problem Setting

In our pre-design approach, the cooling object is mainly defined by its thermal model. This model is built by calculating the global thermal resistance of the device, or of a resistance network, from its architecture and external perturbations (like an air flow for the heatsink). Then, when a heat source is applied to this model, a temperature elevation of the system (ΔT) is calculated and compared to a critical constraint (ΔT_{max}), which should not be reached or exceeded (32).

$$\Delta T(x, y, z) = Losses(x, y, z) * R_{TH}(x, y, z) < \Delta T_{max}(x, y, z) \quad (32)$$

This thermal model can be more or less complex depending on the assumptions on the heat propagation in one or several of the 3D directions (x, y, z). It can also consider one or several heat sources. Heat transfer coefficients can be used instead of resistances, in order to simplify some well-known problems with the use of empirical data and well-known coefficients. In addition, the thermal model is often coupled with fluidic models in order to limit secondary parameters like the air flow or pressure drop, especially when fans or pump systems are used in the system.

For example, in the case of the heatsink, three thermal resistances can be considered (Figure 59) in order to form the thermal model of a heatsink:

- R_{JC} , the "junction to case" resistance of the power semiconductor (supplied by the manufacturer)
- R_{CH} , the heat resistance "case to heatsink" which is based on the material and thickness of the thermal interface
- R_{HA} , the thermal resistance "heatsink to ambient" which corresponds to the sink performance. This chapter mainly develops this type of resistance.

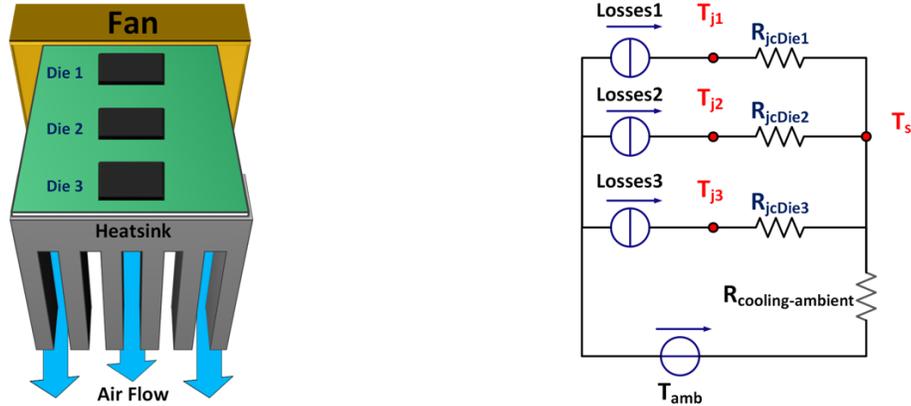


Figure 59: Example of a classical thermal model of an air-forced convection heatsink, with different chips on a same support

3.6.2. Figure of Merit

Some Figures Of Merit (FOM) exist in order to assess the performance of cooling devices. In the industry, designers often use the global thermal resistance (R_{th}) in order to select their COTS devices (Components Off The Shelf). Although this hypothesis to use the thermal resistance is very simple and quite efficient, it remains insufficient to choose the cooling device in an optimized system, as aimed in current power electronics applications.

Thus, another available criterion is the CSPI (Cooling System Performance Index). This value reflects the performance obtained by the volume (33) or mass (34) of a thermal assembly [99] [100].

$$CSPI_{Mass} = \frac{1}{R_{th} \cdot Masse} \quad (33)$$

$$CSPI_{Volume} = \frac{1}{R_{th} \cdot Volume} \quad (34)$$

It allows designers to systematically quantify the performance level achieved by a given system and if it is optimized, thanks to a rapid approach and a single number. As an example, we can see in Figure 60 that even if R_{th} is the lowest for a fin length of 22 cm, the heatsink is oversized (not optimized as a function of its weight). This index can also be evaluated for different parameters, such as the length of the sink or different fan models. To provide a general idea, a good $CSPI_{Volume}$ today is between 18 and 20W/K.L.

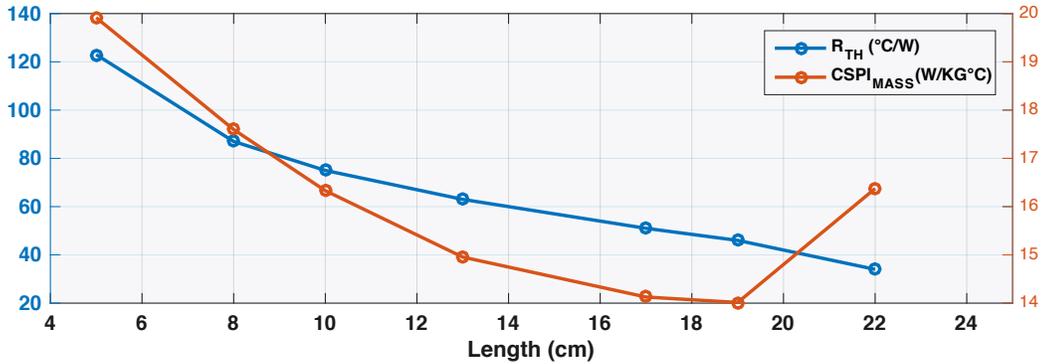


Figure 60: Comparison between the CSPI and R_{th} criteria for the CK SMD family heatsink from Fisher Electronik (aluminum, height = 4.8 cm, width = 6,3 cm)

3.6.3. Geometrical and Material description

As already stated, the focus here is on the straight-fin heatsink. Its geometry can easily be modelled by adding the different dimensions of each element constituting the device, i.e. the base plate and the fins. As a notice, the geometry parameters exposed in Figure 61 will be used in this whole thesis to define the thermal models and write equations. The dimensions of the heatsink are:

- b , the gap space between two consecutive fins
- t , the fin thickness
- L , the length of the heatsink
- W , the width of the heatsink
- H , the height of the heatsink. It is the sum of H_{fin} and H_{base} , i.e. the base plate height and the fin height.

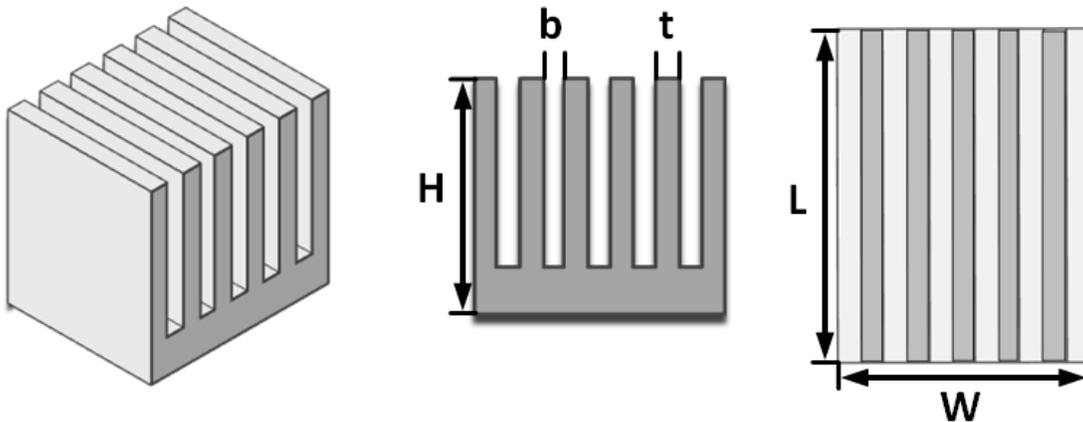


Figure 61: Geometrical definition of a straight-fin heatsink

Three materials of our database can be considered: Aluminum, Copper and Zinc (Table 6). However, some treatments can be added on these materials in order to limit the amount of heat transferred by radiation. For example, the surface emissivity of anodized aluminum is 0.77, compared to 0.07 for rough aluminum (Table 6). From the geometrical definition and based on the precise dimensions

of each part of the heatsink, the volume can be calculated easily and precisely. In addition, by knowing the weight of materials and the volume (Table 6), it is possible to get the final device weight. Compared with the database information, this approach on the weight brings less than 5% of relative error.

	Specific weight(kg/m ³)	K - Thermal conductivity(W/mK)	Emissivity Coefficient (ϵ)
Rough Aluminum	2700	210	0.07
Anodized Aluminum			0.77
Copper (polished)	8930	380	0.023 – 0.052
Zink (polished)	2800	116	0.045
Iron (polished)	7200	79.5	0.14 – 0.38

Table 6: Thermal characteristics of the available heatsink materials in our database

3.7. Multi-domain Models

In order to present the thermal models of the heatsink, the device has been split in two parts: the base plate and the array of fins. It allows a better description of the cooling device as it considers the thermal effects occurring in each individual portion.

3.7.1. Base-Plate

Firstly, the modelling of the base plate is studied. A granularity has been built in order to establish a hierarchy between the thermal descriptions of the base-plate, based on different description of the heat flow dispersion and the number of loss sources to handle in the model. The three main thermal effects have to be considered in this model: The Conduction, Convection and Radiation.

a. Conduction – Analytical definitions

One of the most common way to define the conduction in a flat support is the use of analytical equations that are easy to set and quick to compute. Indeed, vertical 1-D and 2-D conduction models through a rectilinear support have already been developed in Part A for discrete packages of semiconductors (3.3.3.a). These models can be applied here by considering the base plate as a flat support (26) (27) (28). However, this approach is very simplistic and has only to be used for low granularity models.

To be more accurate on the thermal phenomena occurring in the base plate, we consider that the heat flux rarely spreads on the heat source axis, but spreads on a radial direction. To represent this phenomenon, a “spreading resistance” is used. It occurs when the heatsink surface S' is bigger than the chip surface S (Figure 65). A simple definition is proposed in (35). The opposite phenomenon can also appear when $S' > S$. It is called the constriction phenomenon, and so a “constriction resistance” model has to be used.

$$R_{th\ Spreading} = \frac{1}{4 \cdot \pi \cdot K \cdot L} \ln\left(\frac{S'}{S}\right) \quad (35)$$

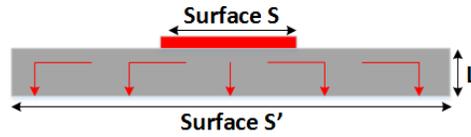


Figure 62: Simplified spreading resistance model reflecting the heat flow dispersion into a flat support

For a higher granularity, numerous definitions of the spreading resistance can be found in the literature, often based on empirical data. These definitions are more detailed and accurate than the previous models, and many of them have been tested during this thesis. From experience and many simulations (that have not always been satisfying), the most accurate model on a wide range of validity have been selected. It is an improved analytical definition of the thermal spreading, based on the placement and dimensions of one or several square sources located on a finite support. The complete study is detailed in [101]. This model estimates average temperatures and solves the sums of Fourier equations for the three dimensions, taking into account the exchange by conduction in the plate and by convection with the air.

A modelling work on this approach has been carried out at the laboratory, in order to implement and improve these definitions in our model library (cf. Anne Castelan work). Comparisons with FEM simulations have been realized for different ratios of chip/support surfaces (Figure 63), in order to validate the model again. The relative error obtained is less than 1% for one and two sources, which validates this efficient approach of this methodology to describe precisely the spreading effect.

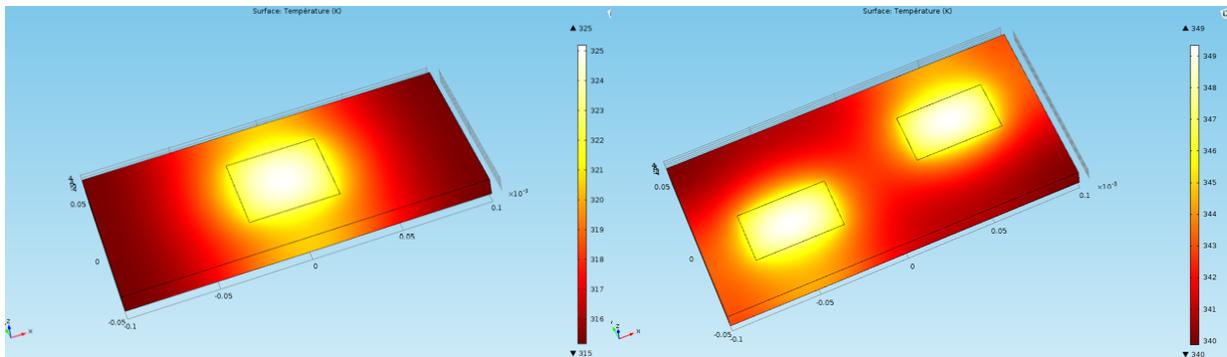


Figure 63: Spreading resistance FEM simulation (COMSOL) for different size and source number configurations on a finite support

b. Conduction – “Meshed” network

Rather than using an analytical formulation to estimate the thermal spreading phenomenon in a flat plate, a discretization with a “meshed” network is also possible [102]. It has been achieved thanks to the definition of several elementary thermal resistances per unit area (Figure 64-a), and

the estimation of the heat flow direction in each node of the 3D plan (x, y, z) . The thermal dissipation in the support provides efficient isothermal lines in the system studied (Figure 64-b). The more precise the thermal analysis of the support is (depending on L , the unit length of the network), the more reliable the discretization is, but at the expense of calculation time. Moreover, the step size of the mesh represents a form of granularity. Three types of thermal resistances are used in this model:

- R_{xy} , coplanar to the support (horizontal conduction)
- R_z along the z -axis and perpendicular to the support plan (vertical conduction)
- R_{CONV} linked to the convection phenomena between the support and the external environment

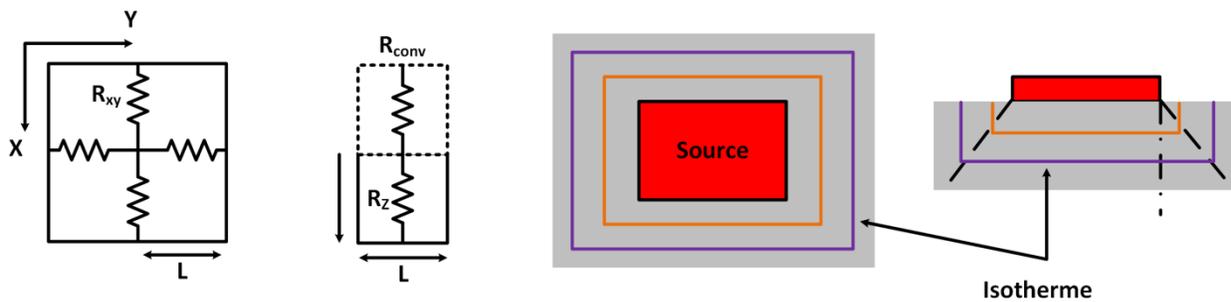


Figure 64: Elementary thermal network of a meshed model for one thermal source

Usually, the support is considered as infinite because of the low dimensions of the sources compared to the support. However, to be closer to the reality, the devices in power electronics are more and more integrated. Therefore, the assessment of the thermal model must comply with the new boundaries conditions: the four physical borders around the chip and its placement on the support (Figure 65). These boundaries are represented by a new heat resistance R_E , imposed by the border of the external environment. In addition, interactions between different types of materials are possible and have to be considered (isolation layers for instance).

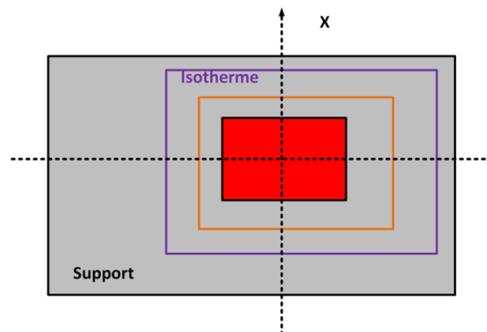


Figure 65: Boundaries conditions of an advanced meshed thermal model of a chip placed on a plan support

In the case of **multiple heat sources**, a first rough thermal estimation can be considered as a sole and global “one heat source”, which is the addition of all separate sources. It can be used for low granularity models.

However, a better alternative is to use the **superposition principle** and the meshed network to characterize the thermal interaction between different sources on the same material support (P_n). At first, each source is studied individually. Then, by superposition of the results of the different sources, it is possible to evaluate the total temperature distribution (36). This principle is illustrated in Figure 66. The hypothesis is that the lower the distance separating the two sources is, the higher the global temperature is.

$$P_{tot}(x, y, z) = P_1(x, y, z) + \dots + P_n(x, y, z) \quad (36)$$

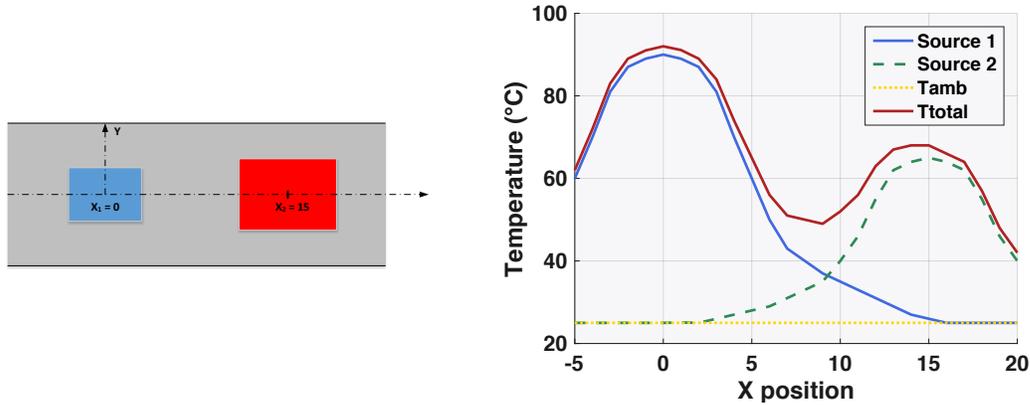


Figure 66: Superposition principle for several sources on a same support

c. Convection

The convective heat transfer or “convection” is the transfer of heat from one place to another by the movement of fluids. It is usually the main form of heat transfer in liquids and gases. In our base plate model, the convection is expressed by a heat transfer coefficient h_{conv} , associated with the related exchange surface S between the solid and the fluid, where the thermal flux q occurs (37). The convection can also be expressed as a thermal resistor R_{conv} (38).

$$q = h_{conv} \cdot S \cdot \Delta T \quad (37) \quad R_{conv} = \frac{1}{h_{conv} \cdot S} \quad (38)$$

This coefficient h_{conv} depends on the surface temperature, which is unknown in most cases and has to be approximated thanks to analytical empirical equations [103] or found in databases (Table 7). It also depends on the type (gas or liquid), velocity, viscosity, and temperature properties of the media.

	Fluid	h_{conv} (W/m ² K)
Free Convection	Air, gases and dry vapours	0.5 - 1000
	Water and liquids	50 - 3000
Forced Convection	Air, gases and dry vapours	10 - 1000
	Water and liquids	50 - 10000
	Liquid metals	5000 - 4000

Table 7: Typical convective heat transfer for main heatsink fluids

Two types of convection are considered to create the thermal model of the base plate:

- **Forced Convection:** The air-forced h_{convFC} is approximated directly by empirical equations like (39), with v being the relative speed from 2 to 20 m/s. Another model found in [104] proposes a formulation of the forced convection as a function of the length of the case L (in m) (40).

$$h_{convFC} = 10.45 - v + 10^{0.5} \quad (39)$$

$$h_{convFC} = 3.768 \sqrt{\frac{v}{L}} \quad (40)$$

- **Natural Convection:** Here again, simplified formula are available for the natural air convection h_{convNC} based on empirical studies and for different configurations (Table 8). However, contrary to the forced convection, a recurrent problem occurs. Indeed, we do not know a priori the temperature of the exchange surface, although it is required to obtain the air properties essential to the calculation of h_{convNC} . Thus, the ΔT has to be “guessed” (41).

$$h_{convNC} = C \left(\frac{\Delta T}{L} \right)^n = \left(\frac{T_{surface} - T_{amb}}{L} \right)^n \quad (41)$$

Simplified formula exist to solve this problem [105], as exposed in (42). The coefficients that are used in the previous equations are shown in Table 8, with S being the surface of the plate and T_{amb} the ambient temperature.

$$T_s = \frac{\left(\frac{q}{CS} \right)^{\frac{1}{n+1}}}{n} \cdot L^{\frac{1}{n+1}} + T_{amb} \quad (42)$$

Numerous other equivalent models are available in the literature, proposing different ranges of validity and hypothesis. As an example, [104] proposes three other empirical formulations that are (43) (44) (45)(the coefficients are exposed in Table 8). Little information are given on the validity domain of these models, but according to the author (43) is the preferred expression:

$$h_{convNC} = 2,79 \cdot f \left(\frac{\Delta T}{0,0254 \cdot p} \right)^n \quad (43)$$

$$h_{convNC} = 0,0005 \cdot f \left(\frac{\Delta T}{L} \right)^{0.25} \quad (44)$$

$$h_{convNC} = 0,944 \cdot \left(\frac{\Delta T}{L}\right)^{0.35} \quad (45)$$

	Length solid (inch)		Empirical Factor		
	p	f	n	C	n
Vertical Plate	Thickness	1,22	0,35	1.42	.25
Horizontal Plate (heat to the top)	$0.5 \frac{W \cdot L}{W + L}$	1	0,33	1.32	.25
Horizontal Plate (heat to the bottom)		0,5	0,33	.59	.25

Table 8: Typical convective heat transfer coefficients

d. Radiation

Thermal radiations can become significant in some configurations, especially for large objects and high power designs. This heat transfer takes the form of electromagnetic waves (mainly in the infrared region), and can be described by reference to the 'black body', sometimes called 'gray body'. The Stefan-Boltzmann law, which depends on the 4th order of the temperature T , defines radiations as in (46), with ϵ being the emissivity coefficient (1 for a black body), T the absolute temperature (K), S the body area (m^2), and σ the Stefan-Boltzmann Constant. Table 6 proposes some radiation constants for the main heatsink materials, with more references in [106].

$$P = \epsilon \sigma T^4 S \quad (46)$$

A radiative heat transfer coefficient can also be approximated between two gray object thanks to analytical equations depending on the surface temperatures (47).

$$h_{Rad} = \epsilon \sigma (T_1^2 + T_2^2)(T_1 + T_2) \quad (47)$$

In addition, the radiation effect is often combined with the convection, and can be represented by a sole effective and global heat transfer coefficient h_E (48). It includes h_{NC} (Natural convection), h_{Rad} (Radiation) and h_{FC} (Forced Convection). This effective coefficient can also be estimated by analytical and empirical equations available in the literature or abacus.

$$h_E = h_{conv} + h_{Rad} = (h_{convNC} + h_{convFC}) + h_{Rad} \quad (48)$$

3.7.2. Parallel-fins

The models to define the heatsink base plate have been presented in the previous section. However, the array of fins still has to be described. Indeed, the heat dissipation that is generated by a solid in any fluid can be improved by increasing the surface area of the solid. By thermal convection, the heat flow is proportional to the contact surface between the two medias. By adding fins on the solid,

i.e. by increasing the heat exchange area, more heat is dissipated and a thermal resistance is added because of the blades length.

a. Nomenclature & Fluidic Definitions

First, we need to precise the nomenclature that is used in this section, especially the physical constants and variables:

- c_p , fluid specific heat at a defined pressure
- λ_{fluid} , fluid thermal conductivity
- μ , fluid dynamic viscosity
- ρ , fluid density
- \mathbf{g}_c , gravitational acceleration
- β , coefficient of thermal expansion for the fluid
- h , heat transfer coefficient
- η , fin efficiency
- δ , thermal conductivity
- v , mean speed of the fluid
- ΔT , temperature difference between the surface and the air
- h , heat transfer coefficient

As a reminder, geometrical variables have already been defined in (3.6.3). In addition, new geometrical parameters are used:

- d , hydraulic diameter inside the fins
- S_{fin} , surface of the side of each fin
- k , ratio of the fin thickness/gap between two fins

Then, we need to precise the fluidic notions that are used to define advanced thermal convection equations. Three coefficients are used here:

- The **Prandtl number** (49), a momentum diffusivity ratio related to the fluid characteristics.

$$P_r = \frac{\mu \cdot c_p}{\lambda_{fluid}} \quad (49)$$

- The **Reynolds number** (50), a normalized heat flow coefficient, which predicts similar flow patterns in different fluid flow situations.

$$R_E = \frac{\rho \cdot v \cdot d}{\mu} \quad (50)$$

- The **Nusselt number** (51), a convective to conductive heat transfer ratio across the surfaces studied. These coefficients aim at refining the calculation of the thermal resistance thanks to assumptions. The formulation is based on a heat transfer mixed model, which is deduced by comparing numerical simulations, as presented in [107].

$$N_u = \left(\frac{1}{\left(Re \cdot \frac{b}{L} \cdot \frac{Pr}{2}\right)^3} + \frac{1}{\left(0.664 \cdot \sqrt[3]{Pr} \cdot \sqrt{Re \cdot \frac{b}{L} + 3.65 \cdot \sqrt{Re \cdot \frac{b}{L}}}\right)^3} \right)^{-\frac{1}{3}} \quad (51)$$

b. Natural Convection

On the one side, we can formulate the natural convection of a heatsink with simple and low granularity definitions:

- A global thermal resistance can be considered for the natural convection of heatsinks (including the base plate and fins), as specified in datasheets. It is formulated under a volumetric resistance (e.g. by realizing a regression on samples extracted from a database) (Figure 67).
- Empirical equations based on physical equations allow to estimate with precision this global resistance from the geometrical dimensions [108] [109].
- In [54], Meta-models are used to create interesting scaling laws, based on physical equations or non-linear regression methods.

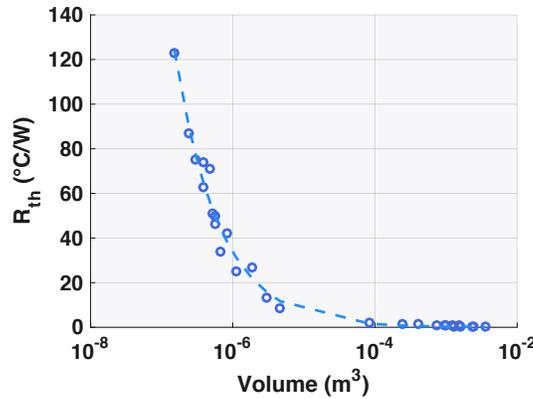


Figure 67: Thermal resistance evolution as a function of a straight fin heatsink family (Fisher Elektronik ICK)

On the other side and as previously discussed, a more accurate definition can be provided, by splitting the problem in two parts: the base plate, already detailed in (3.7.1), and the fins thermal models, presented hereafter.

For the fin model, a heat transfer can easily be estimated in the case of arrays of vertical parallel fins, considering a vertically mounted natural convection. If there is enough space between the fins, there is no interference on the thermal convection effect, and the heat transfer coefficients are the same as for a single flat plate. However, it is rarely the case as optimized heatsinks have very close

plates. Thus, the boundary layers of the thermal model will merge and the heat transfer coefficient for the natural convection will fall below the single plate coefficient value. By using the equation (52) and knowing Nu and Ra , the heat transfer coefficient of the convection can be estimated for arrays of closed fins [110].

$$Nu = \frac{h \cdot b}{k} = \frac{Ra}{24} \left(1 - e^{-\frac{35}{Ra}}\right)^{0.75} \quad (52) \quad Ra = \frac{\rho^2 \cdot g_c \cdot \beta \cdot c_p \cdot b^4 \cdot \Delta T}{\mu \cdot k \cdot L} \quad (53)$$

These relationships may then be used to estimate the optimum spacing between fins b_{opt} , as given by (54).

$$b_{opt} = 2.659 \left(\frac{\mu L k}{\beta g_c \Delta T c_p} \right)^{0.25} \rho^{-0.5} \quad (54)$$

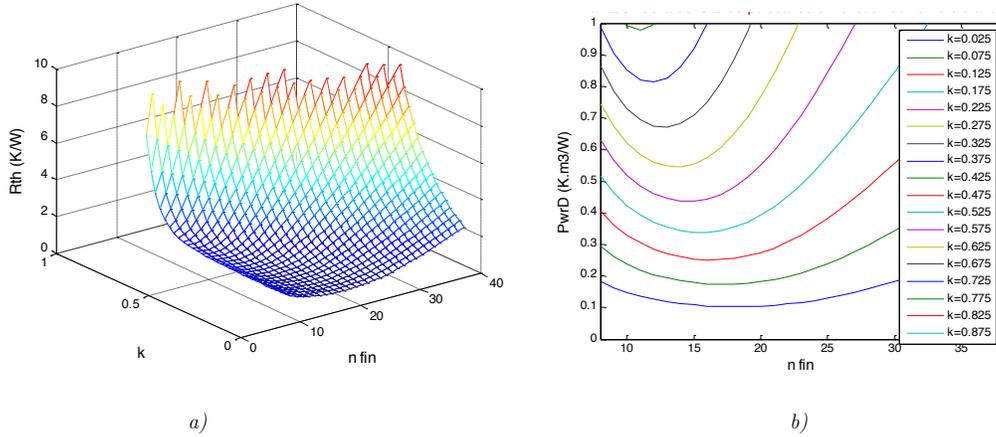
The objective here is to estimate the global heat transfer transported and evacuated by the array of plates. This quantity depends not only on the heat transfer coefficient previously calculated, but also on the number of fins, as shown in (55).

$$q = \eta \cdot h \cdot Area \cdot \Delta T = h \cdot (N \cdot 2 \cdot H \cdot L \cdot \eta) \cdot (T_{surface} - T_{ambient}) \quad (55)$$

In addition, since the temperature varies along a fin, the surface will not dissipate the heat evenly. Therefore, a fin efficiency η can be defined as the ratio of Q_{real} (heat flow actually dissipated by the fin) and Q_{ideal} (heat flow dissipated if the temperature was uniform and equal to the temperature of the solid, i.e. the base of the fin). Each shape of fins is associated with a particular efficiency and its calculation can become quickly very complex. Therefore, in the case of a straight fin, a simplified equation is proposed in (56), with h being the heat transfer coefficient detailed in [111].

$$\eta = \frac{Q_{real}}{Q_{ideal}} = \frac{\tanh(m \cdot H)}{m \cdot H} \text{ with } m = \sqrt{\frac{2 \cdot h}{t \cdot \delta}} \quad (56)$$

To simplify, a fin efficiency of 1 can be used, i.e. the efficiency is considered as perfect. Examples of global models of the array of fins is presented in Figure 68, showing that a global minimum is possible in terms of geometry and number of fins.



a) b)

Figure 68: Examples of the natural convection heatsink models

- a) R_{th} variation as a function of N_{fin} and k , the ratio fin thickness/fin gap
 b) Power density capability variation as a function of N_{fin} and k

c. Air-forced Convection

The thermal models of the natural convection phenomena have been presented previously. This section focuses now on the air-forced convection in a fin array.

d. Fin Model

A first approach for low granularity models is to consider a global and simple equation, defining directly the volumetric resistance as a function of the airflow [112] (57). An example of well-known coefficients is exposed in Table 8 for the volumetric resistances.

$$Volume_{heatsink} = \frac{R_{volumetric}}{R_{thermal}} \quad (57)$$

Available Airflow (LFM)	Volumetric Resistance ($Cm^3 \text{ } ^\circ C/W$)
Natural Convection	500 – 800
200	150 – 250
500	80 – 150
1000	50 - 80

Table 9: Approximate range of volumetric resistances as a function of the airflow

Secondly, a more accurate fin model in air-forced conditions uses the fluidic coefficients introduced in (3.7.2.a). It considers a global thermal resistance (58) composed of the thermal resistances of the base plate and the fins (N being the number of fins) – with a factor of $\frac{1}{2}$ because the two lateral sides are taken into account.

$$R_{heatsink} = R_{BasePlate} + \frac{R_{fin}}{2.N} \quad (58)$$

The base plate model is estimated in (3.7.1). The fin resistance has been modelled thanks to a

resistance network, [113] [114]. It increases significantly the accuracy of the thermal model, especially for thin fins that are more common in optimized heatsinks (Figure 69).

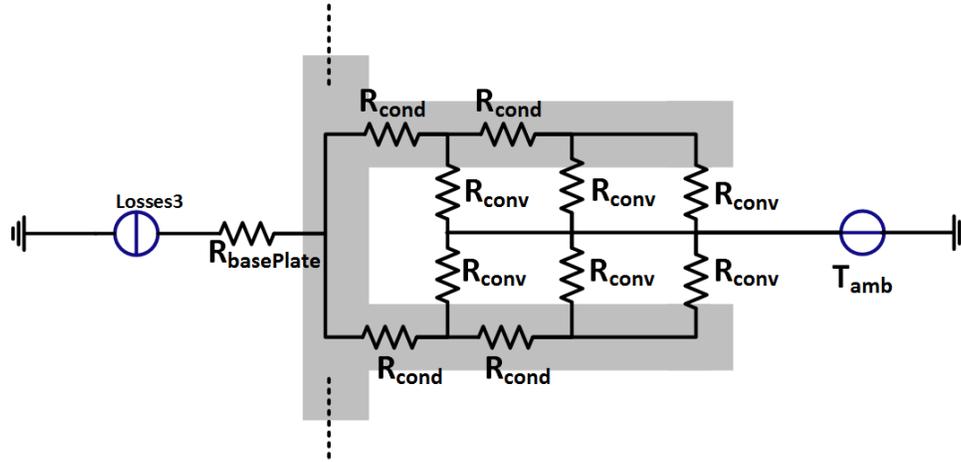


Figure 69: Air-forced fin thermal model

We obtained (59), with y being the number of modules in the thermal network, composed of the conduction resistances R_{cond} , parallel to the convection resistances R_{conv} :

$$R_{fin} = -\frac{1}{2} \frac{A \cdot (-B)^y \cdot -R_{cond} \cdot (-B)^y + A \cdot C^y + R_{cond}}{(-B)^y - C^y} \quad (59)$$

The internal coefficients A, B and C are calculated as follows:

$$A = \sqrt{R_{cond} \cdot (R_{cond} + 4 \cdot R_{conv})} \quad (60) \quad B = \sqrt{\frac{-2 \cdot R_{conv} - R_{cond} + A}{R_{conv}}} \quad (61) \quad C = \frac{2 \cdot R_{conv} + R_{cond} + A}{R_{conv}} \quad (62)$$

Regarding the elementary resistances of conduction and convection, the equations (63) and (64) have to be considered:

$$R_{cond} = \frac{1}{y} \cdot \frac{H_{Fin}}{\lambda_{fin} \cdot t \cdot L} \quad (63) \quad R_{conv} = y \cdot \frac{1}{h \cdot S_{fin} \cdot \eta_{fin}} \quad (64)$$

η_{fin} is the fin efficiency (65) and h the heat transfer (66).

$$h = Nu_b \cdot \frac{\lambda_{fluid}}{b} \quad (65) \quad \eta_{fin} = \frac{\tanh\left(\sqrt{\frac{2 \cdot h \cdot H_{Fin}}{\lambda_{fin} \cdot S_{fin}}}\right) \cdot \sqrt{\lambda_{fin} \cdot S_{fin}}}{H_{Fin} \cdot \sqrt{2 \cdot h}} \quad (66)$$

These calculations assume that the air flow regime is laminar in the sink, which is true for the majority of cases. As a first validation, the "Cool Air" sizing tool developed at ETH Zurich has been used in order to compare the models results. It provides equivalent results. Two examples of the model behaviour are presented in Figure 70 and Figure 71, which show that a global minimum of the design is possible in terms of geometry, number of fins, air flow and pressure drop.

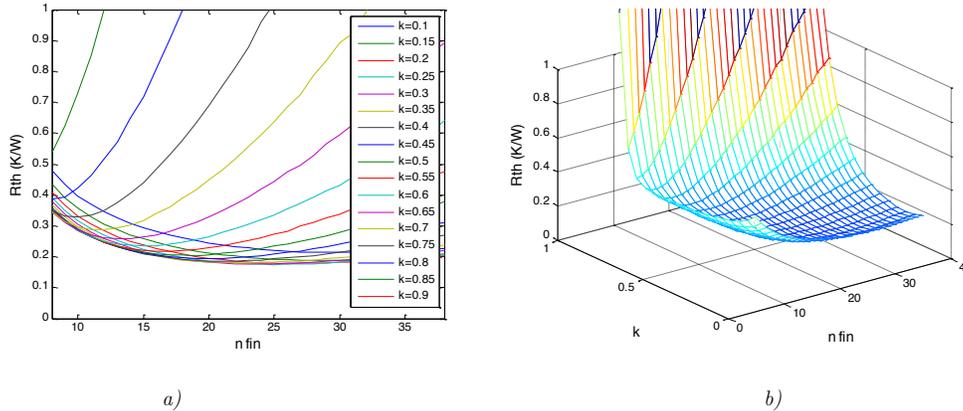


Figure 70: Examples of the air-forced convection heatsink models

- a) R_{th} variation as a function of N_{fin}
 b) R_{th} variation as a function of N_{fin} and k , the ratio fin thickness/fin gap

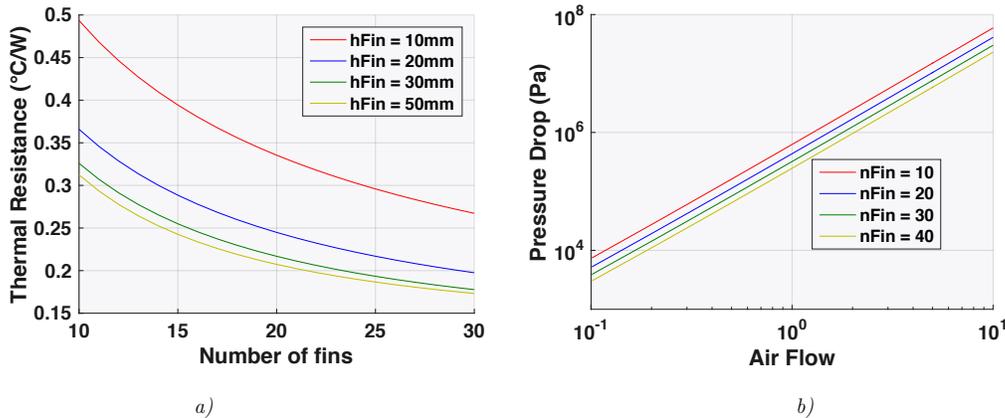


Figure 71: Examples of the air-forced convection heatsink models

- a) R_{th} variation as a function of N_{fin}
 b) Pressure Drop variation as a function of the airflow

3.7.3. Pressure Drop Model

In order to predict the performances of the heatsinks in air-forced mode, it is necessary to estimate the average speed of the air flow inside the fins (in m/s), depending on the pressure drop. The pressure drop is the difference in pressure between the inlet and the outlet of the cooling component. This phenomena appears when frictional forces act on a fluid as it flows through the tube, which is caused by the resistance to flow. Indeed, by knowing this effective air flow and coupling it to the fans and blowers' static pressure characteristics, it is possible to deduce the pressure drop occurring in the system. This pressure drop is a main constraint in an embedded equipment.

Different methods are proposed, and compared to empirical and simulation results in [111]. The most accurate model that we have tested is coming from [115]. It expresses the pressure drop ΔP in Pa (67) and the air channel speed $v_{channel}$ in (m/s) (68) – the average velocity of the air flowing through the channel – and the effective speed blows to the heatsink v_{eff} :

$$\Delta P = \left(\frac{v_{channel}^2}{2} \cdot \rho \right) \cdot \left(K_c + K_e + \frac{f_{app} N (2HL + bL)}{HW} \right) \quad (67) \quad v_{channel} = v_{eff} \cdot \left(1 + \frac{t_f}{b} \right) \quad (68)$$

The coefficients K_c and K_e represent the pressure losses due to the sudden contraction and expansion of the flow entering and leaving the heat sink flow channel between the fins:

$$K_c = 0.42 \cdot \left(1 - \left(1 - \frac{t \cdot N}{W} \right)^2 \right) \quad (69) \quad K_e = \left(1 - \left(1 - \frac{t \cdot N}{W} \right)^2 \right) \quad (70)$$

f_{app} is the apparent friction factor for hydro dynamically developing laminar flow. It is related to the friction factor for fully developed flows f .

$$f_{app} = \frac{L}{Re \cdot b} \cdot \sqrt{\frac{47.33 \cdot B \cdot Re}{L} + (2 \cdot f)^2} \quad (71)$$

$$f = 24 - 32.527 \cdot \psi + 46.721 \cdot \psi^2 - 40.829 \cdot \psi^3 + 22.954 \cdot \psi^4 - 6.089 \cdot \psi^5 \quad (72)$$

The models have been compared to the experimentations proposed in [115]. Three real heatsinks with various geometries and air characteristics have been tested, and then compared with the FLOWTHERM simulations. The models match with the experimentations for different cases detailed in this paper (Figure 72). The pressure drop models have also been tested with the COMSOL software, in order to validate our Matlab models (Figure 73). In several cases, the maximal relative error is inferior to 20%.

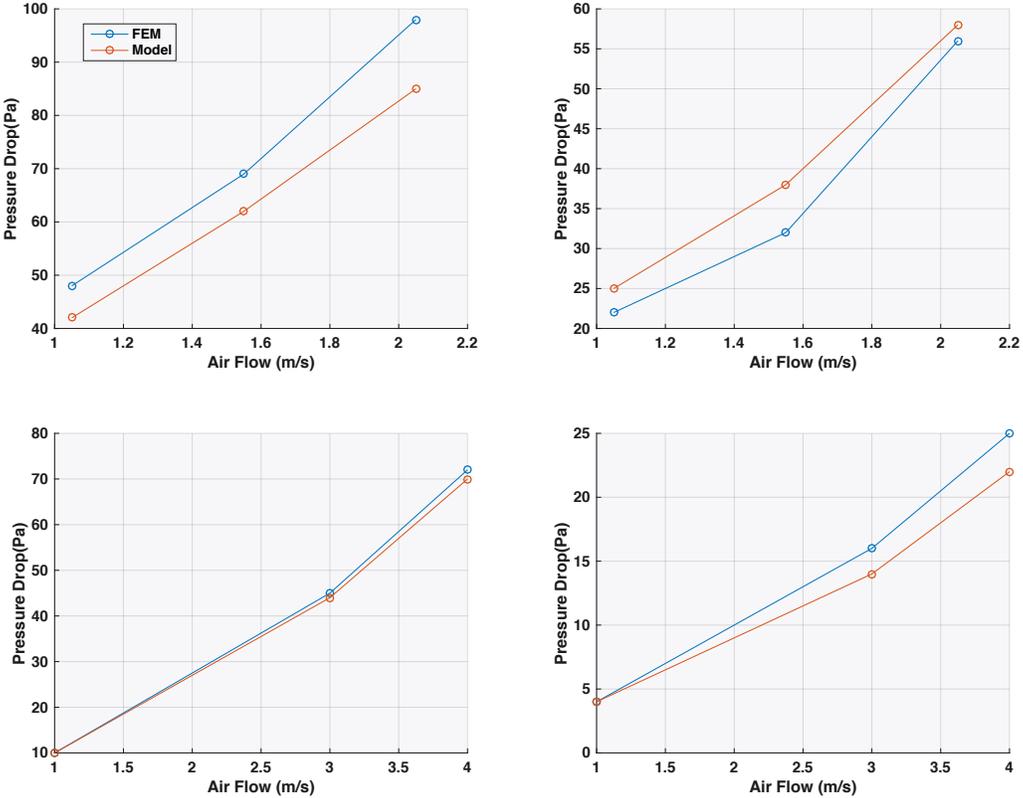


Figure 72 : Heatsink pressure drop model validation compared to experimental data from [115]

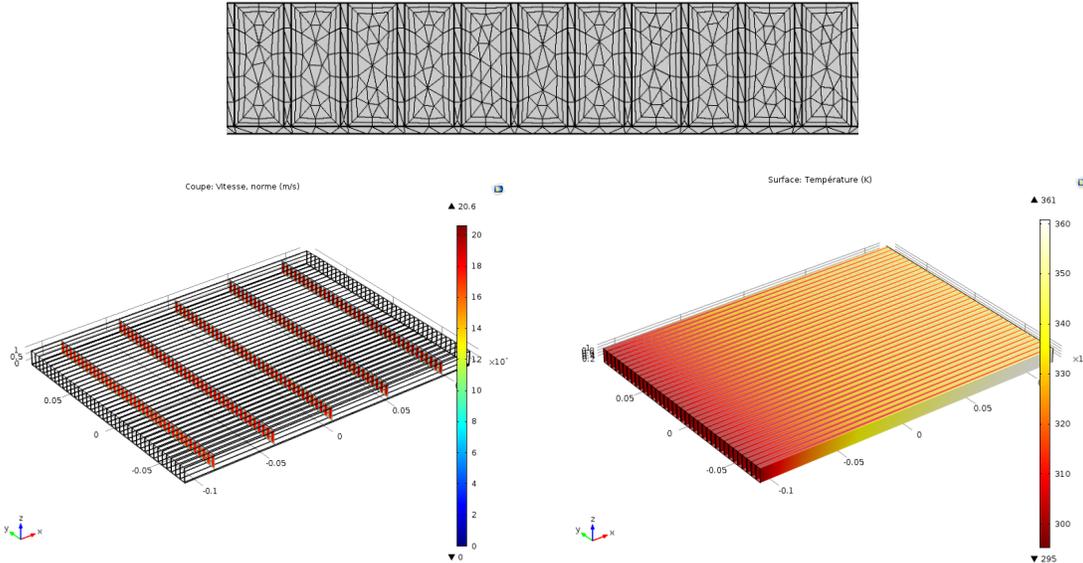


Figure 73 : Pressure drop and thermal dissipation simulations with COMSOL

3.7.4. Cost models

The final cost of heatsinks depends on two main factors:

- The material, which cost is directly proportional to the volume (or weight) of the heatsink.
- The manufacturing and labour cost of production, including the engineering cost.

Considering the market price of aluminum, the heatsink cost is not always proportional to its weight (or volume) for all types of devices. For instance, the hollow-fin type is light but expensive. Thus, we have to consider only the classical geometries in order to create a pertinent model. For the straight-fin heatsinks, the distributor prices show that the cost is quite linear as a function of the volume, as shown in (Figure 74-a) thanks to Farnell's website data. The cost model equation created is given in (73), and confirmed by [91].

$$Price_{Hsink} = k_{MOQ} \cdot (SpecPrice_{material} \cdot V_{Hsink} + Price_{manufacturing}) \quad (73)$$

A Minimum Order Quantity (MOQ) coefficient (k_{MOQ}) has also been added in order to link the unit price model to this commercial factor. As an example, Figure 74-b shows the price reduction coefficient as a function of the MOQ. This figure is based on the available data extracted from our database of aluminum heatsinks.

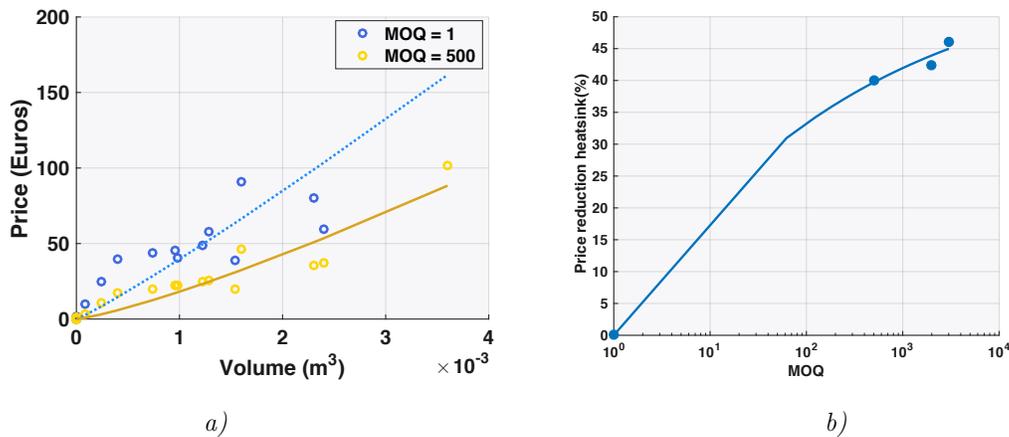


Figure 74: a) Specific price for aluminium straight heatsinks as a function of the volume
b) Price reduction vs MOQ of the Heatsink from MOUSER website partnumbers

3.8. Fan Model

In aeronautical applications, converters that require an air-forced cooling are often connected directly to a pneumatic network. This network provides an airflow to the inlet of the thermal exchanger. Thus, the injection of air is not managed by the power electronics equipment and no additional cooling equipment has to be considered in the modelling. In this case, additional information such as fluidic constraints (e.g. pressure drop) are specified to size the power equipment.

However, in some cases, a fan or a blower has to be added for thermal reasons or to build an independent system. Therefore, a fan object is required in our model library. Fans are generally described by a characteristic showing their pressure drop Δp_{fan} [Pa], dependent on the flow rate of the air \dot{v} [m³/s] (Figure 75-a) [116] [117]. The main principle of the fan is to supply a precise flow rate to the thermal exchanger, which is a function of its external characteristics like its geometry and power consumption. There are two possibilities to model this fan object:

- It is possible to propose a continuous model of a fan based on its geometry, in order to estimate the air and pressure characteristics [118].
- A more common approach is to consider a discrete fan that has been pre-selected in a database, and use on it some well-known scaling laws [119]. It allows to modify the fan dimensions and speed in order to get the new air-flow, pressure and power characteristics (Table 10).

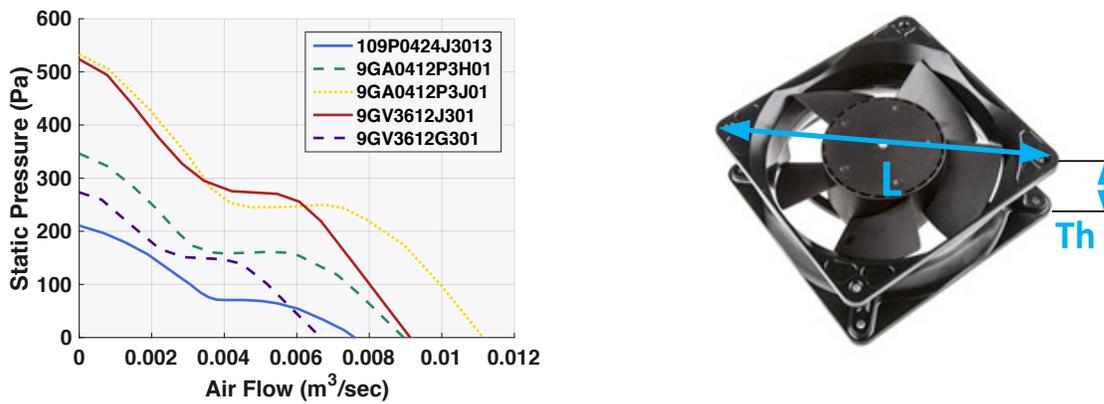


Figure 75: SANYO axial Fan samples characteristics and input dimensions of the model

	Fan scaling laws		
Flow \propto Speed	$\frac{Q_A}{Q_B} = \left(\frac{N_A}{N_B}\right)^1$	Flow \propto (Diameter) ³	$\frac{Q_A}{Q_B} = \left(\frac{D_A}{D_B}\right)^3$
Pressure \propto (Speed) ²	$\frac{SP_A}{SP_B} = \left(\frac{N_A}{N_B}\right)^2$	Pressure \propto (Diameter) ²	$\frac{SP_A}{SP_B} = \left(\frac{D_A}{D_B}\right)^2$
Power \propto (Speed) ³	$\frac{P_A}{P_B} = \left(\frac{N_A}{N_B}\right)^3$	Power \propto (Diameter) ⁵	$\frac{P_A}{P_B} = \left(\frac{D_A}{D_B}\right)^5$

Table 10: Scaling Fan Laws

Other quantities can be calculated as optimization constraints of a fan sizing: the **noise** and the **vibrations**. Indeed, the specifications of a converter often set of limit to these quantities, with for instance the purpose of not disturbing potential users and of increasing the system reliability. Many empirical formulas are available in [120]. They are specific to the form-factors or the fans (e.g. axial, radial, etc.). As an example, from the empirical data given in [121], the noise can be formulated thanks to (74). The noise is expressed in dB, K_W being an empirical specific sound, Q the low rate in cfm, P the total pressure in inches, BFI the Blade Frequency in bpf, and CN an efficiency correction coefficient.

$$Noise = K_w + 10 \log_{10} Q + 20 \log_{10} P + BFI + C_N \quad (74)$$

3.9. Experimental Validation

Some experimental validations have been achieved in order to ensure the efficiency of our cooling models in different applications. These experimentations have been compared to the most accurate models we have created (i.e. for the highest granularity that have been presented previously).

3.9.1. Forced Convection

Firstly, some forced convection tests have been realized on different heatsinks and fans. The aim was to compare the global thermal resistance of our virtual object with these real devices (i.e. the thermal model between the base plate where the heat source and the ambient air are applied). Our hypothesis considers a heat source distributed on all the base plate, as it is often the case in real applications since the heatsink is normally customized to fit perfectly the semiconductors space, and so to limit the spreading phenomena

Thus, the set-up of this experimentation is to mount a power resistor on the flat base, in order to generate the equivalent of the semiconductor distributed losses on the thermal interface (Figure 76). In addition, a support attaching the fan to the radiator has been added to ensure that the forced air flows well over the whole sink section. Different thermocouples have been used to measure the temperatures efficiently, with some of them placed inside the base plates.

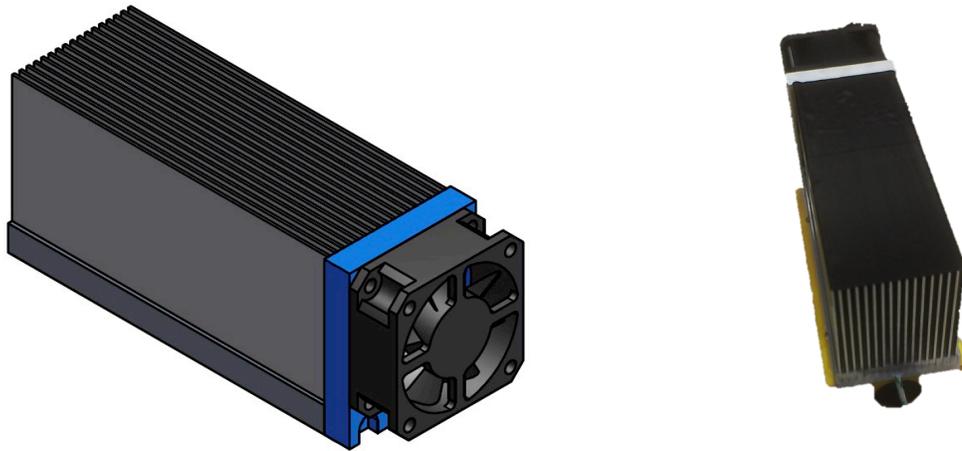


Figure 76 : Fan/heatsink mounting for the validation of models

The results of this empirical validation give a mass of 230 g for 233 g in theory, which means a relative error of 1,3%. The measures of the thermal resistances have been realized for power ratings from 40W to 110W. The 100W measures have been summed up in Table 11 as an example. They

provide a maximal relative error inferior to 6%. To finish, the air velocity measured is about 20% lower than the "theoretical" speed in all the cases.

Fan	Experimental Measurement		Model	Validation
	P (W)	Rth (°C/W)	Rth (°C/W)	Relative Error (%)
SANYO 9GA0412P3H01		0,237	0,25	-5,20%
SANYO 109P0424J3013	100	0,265	0,28	-5,36%
SANYO 9GA0412P3J01		0,217	0,23	-5,65%

Table 11: Results of the heatsink validation in forced convection

Thus, the forced convection models demonstrate good results in this configuration, especially for the thermal model of the fin array. However, this set-up does not validate empirically the possible spreading phenomena that can occur in the base plate. As a reminder, it has already been verified by the FEM simulation in (3.7.1).

3.9.1. Natural Convection

Secondly, validations have been realized in natural convection. The validations are easier for this natural mode since the global thermal resistance R_{th} is either characterized in datasheet or easily deducted from an experimentation. Thus, this global thermal resistance R_{th} has to be compared directly to the thermal model. However, we consider as a hypothesis that we use the models in the same environment as the one used to characterize the device, which is not true in many cases (e.g. an ambient temperature of 25°C, etc.).

On the one hand, the heatsink models are compared to a real device that is specified and customized for an Airbus power electronics application and generates 30W of losses. The heatsink geometry is presented in Figure 77. The relative difference on the thermal resistance with its thermal characterization (i.e. the global thermal resistance) is 6% and 1% for its weight estimation.



Figure 77: Natural Convection device for the Cooling Evaluation

On the other hand, we have extended this comparison thanks to a short database filled in with samples extracted from the Farnell website. By only comparing the global R_{th} , the relative error of the thermal model is always inferior to 14%, which confirms the previous results.

Thus, from these simple comparisons, the natural convection model built is accurate, and can be used in pre-design.

3.9.1. Aeronautical Environment

Thirdly, a cooling experimentation has been realized in an avionic context. The purpose was to characterize the thermal aspect of a full-bridge topology using GaN semiconductors under natural and forced convections that comply with the Airbus requirements. Thus, we used this experimentation to do a first rough validate of our heatsink thermal model in both modes. Indeed, the set-up is not dedicated to the thermal characterization, but can provide interesting information to know if our models are close to the reality.

The set-up is composed of four switches that are coupled with a custom straight-fin heatsink (almost equivalent to our model in terms of geometry), and specially optimized for the wide-band gap devices (Figure 78). The board is placed in an avionic rack and cooled by a laminar airflow under a pressure of 300 Pa, which corresponds to the ground pressure of the standard avionic programs. We have characterized the global thermal resistance with one chip in conduction at first, then with two chips.

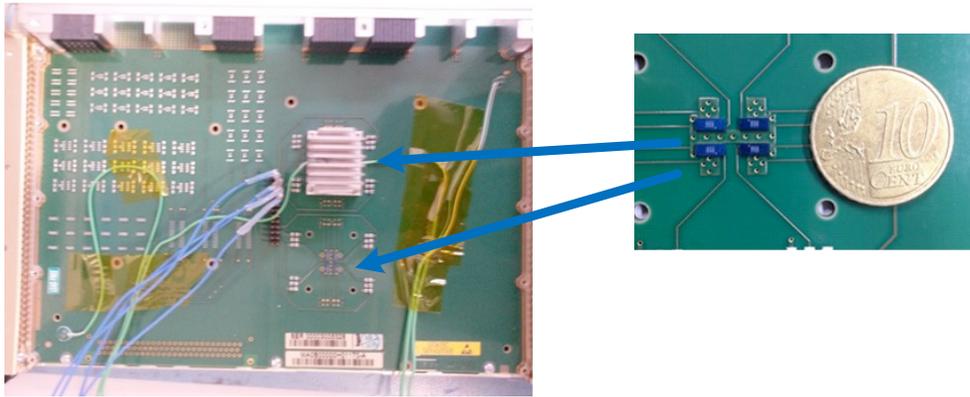


Figure 78: Circuit board and Heatsink used in the experience

The maximal error of global thermal resistance is 20% between the empirical and the simulation results (Table 12), which is acceptable for a pre-design. This error value is higher than the previous results, which may be explained by a slightly different geometry between the simulation and the reality (the fin length is not totally constant all along the plate), by the fact that the heating conduction spread in the PCB or in the thermal grease has been neglected; or because the air flow was not entirely driven into the sink section.

Thus, limits can be established on this kind of thermal comparison. An order of magnitude can be validated: here the model built is close to the reality. As a reminder, the first aim of this experimentation was to test the thermal behaviour of the GaN devices, and not to validate precisely a thermal model which is much more complex.

Chip Conduction	Dissipated Power	Convection Type	Relative Error (%)
1 chip	2W	Natural	-20
		Forced	18
	4W	Natural	-17
		Forced	15
2 chips	2W	Natural	-15
		Forced	12
	4W	Natural	-14
		Forced	11
	6W	Natural	-16
		Forced	10

Table 12: Comparison results between the models and the experimentation

3.10. Conclusion

An entire method has been proposed to create analytical and continuous models of heatsinks in natural and air-forced convections, according to different granularities and hypothesis. The different thermal phenomenon occurring in a power converter have been approached, including the thermal models of the global heatsink, base plate and parallel fins. These models allow fine representations of physical effects, such as the spreading phenomena, and provide accurate results that have been validated by databases, FEM simulation and experimental prototypes. As a conclusion, the thermal modelling part of the optimal design in power electronics - represented by the straight-fin heatsink - is well mastered for different granularities and can be efficiently optimized and prove the potential of this new way to design power electronics devices.

However, only heatsink models have been developed, and on a precise fin form-factor. It is thus too limited for the actual applications and study requirements. Indeed, the current problematics in the MEA require to make design trade-offs between the air, water and LHP technologies, which is still not possible with the work achieved. Thus, as a future work, it is essential to keep developing new form-factors of heatsinks, and to improve the current models of the other cooling devices in order to get a representative library of models. They should allow to perform efficient comparisons between the different cooling medias and providing relevant trade-offs for electrical systems, that is too few available in the current literature.

Chapter 4

4. Passive Part: Analytical models of Magnetics, Capacitors and EMC Filters

The purpose of this chapter is to provide relevant continuous models to design and optimize the passive devices, especially to realize the galvanic isolation with transformers and EMC filters composed of inductors and capacitors. The demonstration is separated in three parts, in order to present individually each device, i.e. magnetics and capacitors. Then a filter design method integrating these devices is presented.

Part A: Magnetic Devices

The objective of this part is to propose a model that allows full design of magnetic devices, taking into account each of its parts, such as magnetic cores, conductors and insulators. A description of the different physical effects playing a role in its construction are presented first. It is essential to remember that this work was initiated several years ago in the Laplace laboratory, with previous studies on the pre-design of Transformers and Inter Cell transformers [122] [123] [16] [124]. This chapter proposes a global synthesis of the different techniques used in the magnetic component design and dedicated to multi-objective design. In a first section, we propose an overview of the device we want to model in pre-design studies. Secondly, a review of the material and their assessment is proposed for the core component and conductors. Thirdly, we define the different models of magnetic devices, before proposing their different multi-domain design, especially for the inductor that is more difficult to define than classical transformers. Finally, the next steps to validate our approach and future work are discussed.

4.1. Magnetics Objects Overview

The magnetic objects exist under numerous devices and forms in power electronics. On the one side, **inductors** are usually found under different types of core materials:

- **E- or U-type ferrite cores** with possible air gap, which allow different winding variations (Figure 79). It implies either a better heat surface exchange (a) or a better channelling of the magnetic field (b). The E-type is preferred for high current ripple and alternative applications because the whole winding is included in the core. Using an airgap stabilizes the inductance for the DC current levels while devices without any airgap are directly

impacted by the material properties variations. However, more perturbations and losses are produced because of the magnetic field, which is indeed less guided (fringing effect) [125].

- **Toroidal cores** in powder with a distributed airgap or in Nano-crystalline material with no airgap and no possibility of airgap. Thus these cores propose less freedom in the inductor design. Their use of this geometry/materials in our converters remain exclusive to the filtering applications, especially for the coupling inductors.
- **Other shapes** like pot cores, EE- and L-type cores.

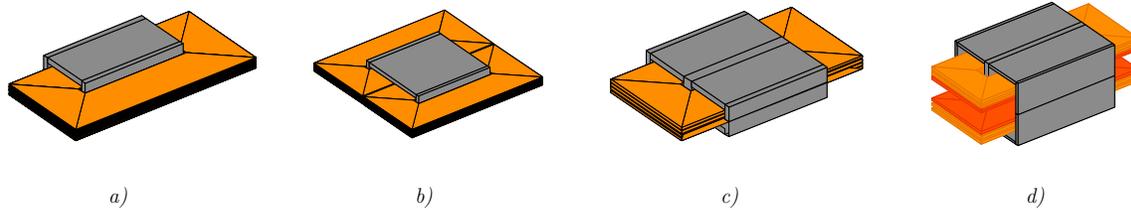


Figure 79: Some inductor shapes

a) U-core 1 winding - b) U-core two windings - c) E-core one winding - d) E core transformer sample

On the other hand, **transformers** are the main elements of isolated converters, as they ensure galvanic isolation and power transfer between the primary and secondary sides. Planar cores are the preferred type for high frequency and high power applications because of their low profile easing the integration and increasing the heat surface exchange. The leakage inductances must be minimized while the power transfer efficiency is optimized. They are indeed usually contained in an E-core, and they possess two different conductors stacked or interleaved. Nowadays, conductors are directly integrated as stacked PCB or busbar. Other conventional transformers with round conductors and cores have also developed in the inductor part. They basically use the same principles as the planar type.

Another interesting component is the **Inter Cell Transformer (ICT)**, composed of monolithic or separate cores. A two-phase ICT is a coupled inductor based on the transformer pattern, with the only difference that the AC component of the two voltages across the two pairs of terminals of the ICT are imposed by the external circuit. The leakage inductance must be maximized with a separation of the conductors in order to guarantee an efficient filtering behaviour. Indeed, ICTs are usually implemented in parallel and multi-cell topologies, as phase-interleaving offers a more efficient filtering. ICT normally reduces the current ripple in the windings and the total induction because of the decoupling of the common and differential mode flux. Thus, the equipment obtained is more compact and lighter. Various ICT topologies exist thanks to different methods of coupling and interleaving of conductors [16] [123]. However, the ICT is not always an ideal choice because of poor improvements in the global sizing of the power converter, a high sensitivity to current unbalance implying a possible saturation, and even a lack of robustness to the disconnection of a phase. Nevertheless, an oversizing of the ICT can accept this kind of failures, though we lose the advantage of the compactness [124]. We can also create **Isolated InterCell Transformers**, that are the direct mix between a transformer and an ICT. The simplest isolated Inter Cell Transformer is

Filters

composed of four phases. The primary and secondary windings of a given phase are wound on the same leg so that primary-secondary leakage is minimized; otherwise, the geometry is similar to that of a non-isolated ICT. Like transformers, isolated ICTs are often built with E-type cores that better contain the magnetic fields in the core, with less electro-magnetic field outside since all the conductors are inside the core. However, they possess less exchange surfaces. It seems that this configuration is more suitable for high current ripple, where the alternating field is higher. Different ICT topologies are displayed in Figure 80.

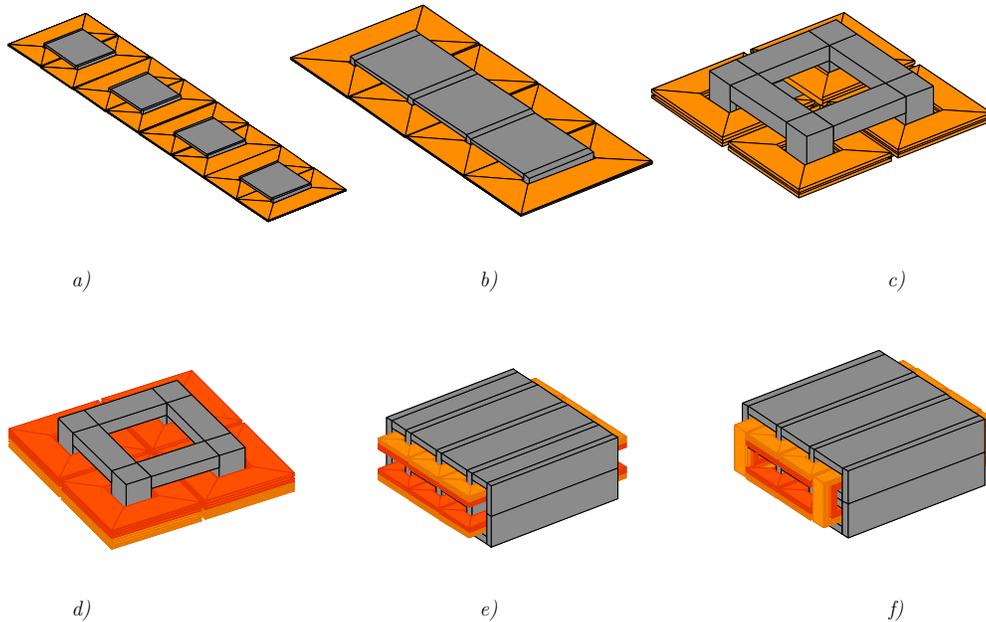


Figure 80: Different examples of ICT (a,b,c) and isolated ICT devices (d,e,f)
 For isolated ICTs, primary winding in orange, secondary in red

4.2. Materials

4.2.1. Core Materials

The role of a magnetic circuit is to guide the magnetic field lines and to reduce the reluctance along this path. The objective of magnetic design is to obtain the best trade-off between a high permeability, a high saturation induction, and a low level of losses in a given frequency range. When aiming at optimal design of power converters, only the main high frequency materials are investigated (Table 13).

Material	Ferrosilicon alloy(Fe-Si)	Iron-nickel alloy (Fe-Ni)	Ferrites
Frequency domain	[0;10e3] Hz	[10e3;10e5] Hz	[10e4;10e8] Hz
Material	Nanocrystalline	Amorpheous	Low permeability
Frequency domain	[10e4;10e7] Hz	[10e4;10e5] Hz	[10e4;10e7] Hz

Table 13: Frequency domain for the main families of core materials

Thorough reviews of these materials can be found in the literature [126]. Indeed, they possess particular restrictions on various criteria (operating frequency, permeability, induction temperature, losses, geometry, stability...) that must be taken into consideration during the sizing of the component. The design of a magnetic component is mainly guided by two parameters: B_{max} , the maximal induction imposed by the material and F_{sw} , the switching frequency. B_{max} is the amplitude of the induction that can be admitted by the material; at low frequency it is equal to the saturation induction, but when the switching frequency increases, it must be decreased to limit the losses generated inside the material at an acceptable level. A high B_{max} and a high f_{sw} both contribute to make the magnetic component small, but because B_{max} decreases non linearly with increasing f_{sw} , there is for each material an optimal frequency range, giving a maximum of $B_{max} \cdot f_{sw}$. When the switching frequency is imposed, it is also possible to select the material giving the highest $f_{sw} \cdot B_{max}$ product; this material should give the smallest magnetic component.

The product $f_{sw} \cdot B_{max}(f_{sw})$ is usually used to follow these rules and compare different materials at a given loss density level, as it reflects the variation of loss density (Figure 81). At a given frequency, the most interesting material is the one with the highest figure of merit [127]. At low frequency, the induction is limited by the saturation and in high frequency by the loss density.

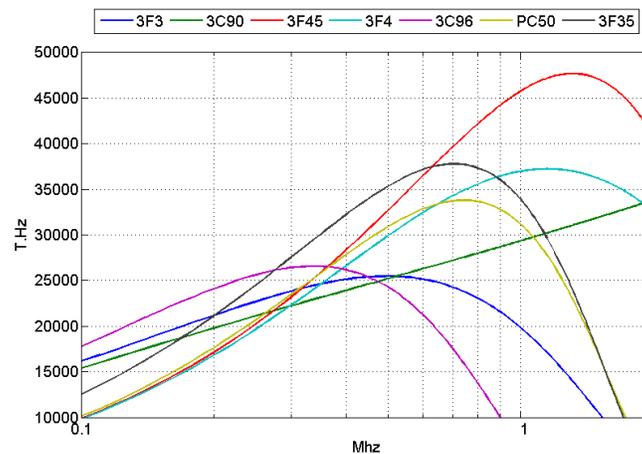


Figure 81 : Performance factor evolution $f_{sw} \cdot B_{max}$ for different materials as a function of the switching frequency from manufacturer data [128]

In addition, it is possible to create a virtual material based on this FOM by tracing the overall limit of the different materials. This can be done for all materials, or for a family of materials of the same type. In order to do so, we use our loss models and database presented below. This virtual material

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presents at each frequency the characteristics of the best material of the family. Thus, a single surface is obtained, which avoids testing different discrete materials. However, such a surface comprises many local minima and its derivative has many discontinuities that can cause convergence problem if used in optimization routines. A smooth response surface approximating this surface can be generated to represent a virtual material that will be referred to as “current-best material”. In the context of a deterministic optimization, this material should help and accelerate the convergence of gradient-based algorithms. However, a second run has to be used to define the closest and most appropriate material.

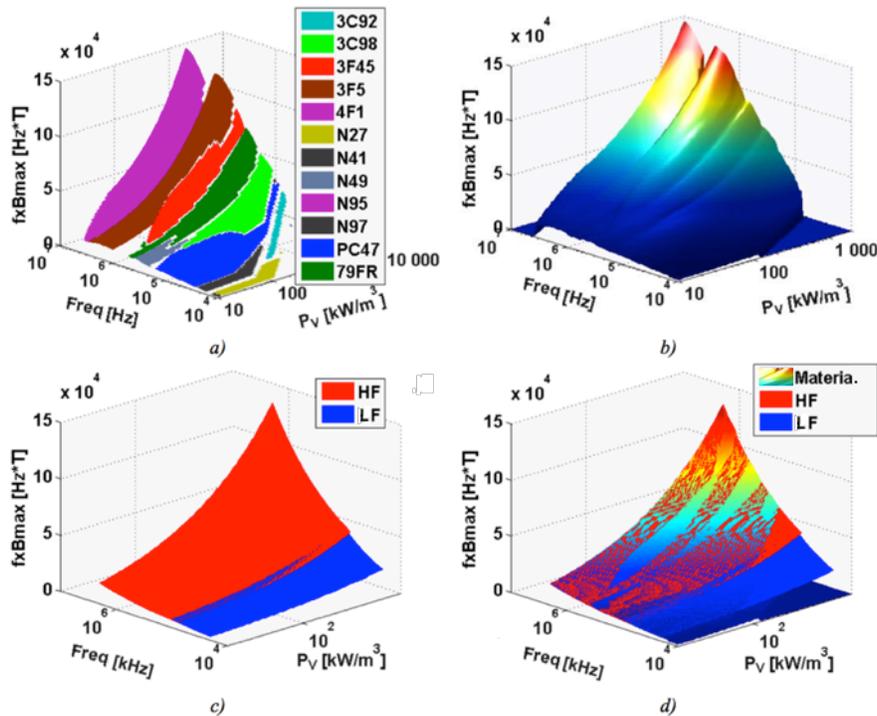


Figure 82: Performance factor $f_{sw} \cdot B_{max}$ for the technological limits of ferrites as a function of the power density (P_v) and the switching frequency (Freq) [16]

- a) Best performant materials for a given frequency and loss density
- b) Best Range of use for the ferrite materials as a real and sole surface
- c) “Current-best material” from a linearization of b) as smooth surfaces and divided in two families: High (HF) and Low Frequencies (LF)
- d) Comparison between response surface (c) and real surface (b)

4.2.2. Conductor Materials

The materials and shapes of conductors must be chosen to limit copper losses, composed of skin and proximity effects. Two materials are usually considered: copper that has a high current conductivity, and aluminium that is lighter and possesses a high thermal conductivity. Copper is generally preferred in power electronics, but its rising cost now makes aluminium a very good challenger [123]. Round conductor is the most common shape, however flat and square wires also exist and may be

preferred for some applications; flat wires may reduce high frequency AC resistance and square wires may help increase the fill factor.

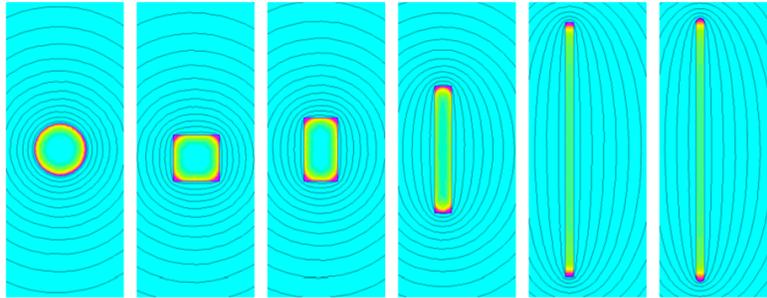


Figure 83: Skin effect simulation in different shapes of conductors (extracted from [123])

Another technique can be used to limit the increase of AC resistance at high frequency: The Litz wires. They are made of thin conductors individually insulated and connected in parallel, which are twisted to successively occupy the same position in the field. Different types of Litz wires are shown in Figure 84 [129].

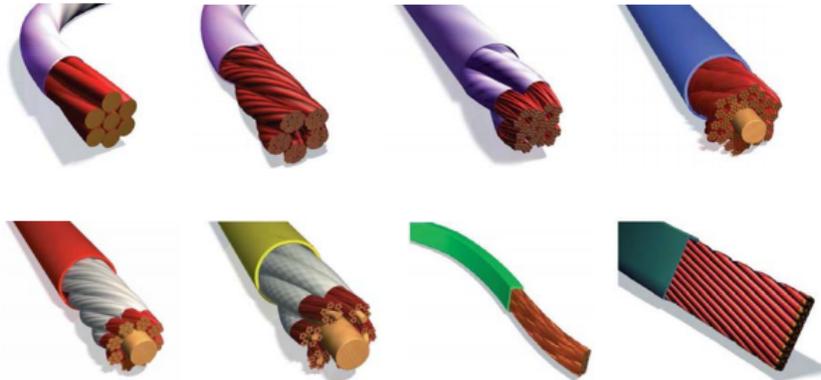


Figure 84: Variety of commercial Litz Wires

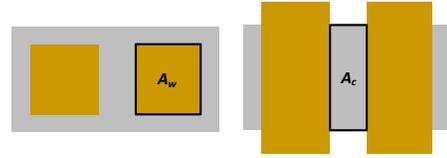
4.3. Principle of the model

4.3.1. Formulation of the problem

To introduce the modelling principles and to consider the different aspects of the magnetic component, it is convenient to rely on the product areas. This idea has been introduced by many publications such as [55] and is represented in Figure 85 for transformers (75) and inductors (76) with q windings. The maximum induction and the current densities are dependent on the frequency and size, and they are particularly limited by the core and conductor losses and the allowed temperature of materials.

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$$Cte. (Vol)^{\frac{4}{3}} = A_w \cdot A_c = P \frac{\sum_{i=1}^q K_{Pi} \frac{K_{wi}}{J_{iRMS}(T, F, Aw)}}{B_M(T, F, A_c)F} \quad (75)$$



$$Cte. (Vol)^{\frac{4}{3}} = A_w \cdot A_c = W_L \frac{\sum_{i=1}^q K_{wLi} \frac{K_{wi}}{J_{iRMS}(T, F, Aw)}}{B_M(T, F, A_c)F} \quad (76)$$

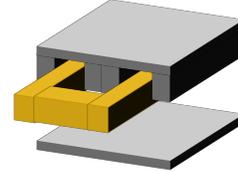


Figure 85: Principle of the product area for magnetic devices

The variables involved are:

- Geometric parameters
- A_w , window available for drivers
- A_c , effective area of the magnetic circuit
- K_{Pi} and K_{wi} , factors that are dependent on the geometry and shape of the electrical excitation
- K_{wi} , fill factors of the winding window (form of drivers, isolation)
- System specifications
- P in the case of power transformers and couplers
- W_L , in the case of power inductors
- F , operating frequency
- Main constraint
- T , operating temperature
- Internal variables
- B_M , peak value of induction in the magnetic circuit
- J_{iRMS} effective current density in the winding

4.3.2. Granularity

For each core shape (E-Core, Toroid, etc.), magnetic components can be described with models of increasing complexity levels. Simple models are to be used in large scale problems or pre-design studies, and it is therefore interesting to limit the number of input parameters (optimization variables) i.e. dimensions and material (Figure 86). As an example, the number of dimensions can be reduced by using homothetic shapes, [55] and the number of possible materials can be limited by using one or several “current-best material”.

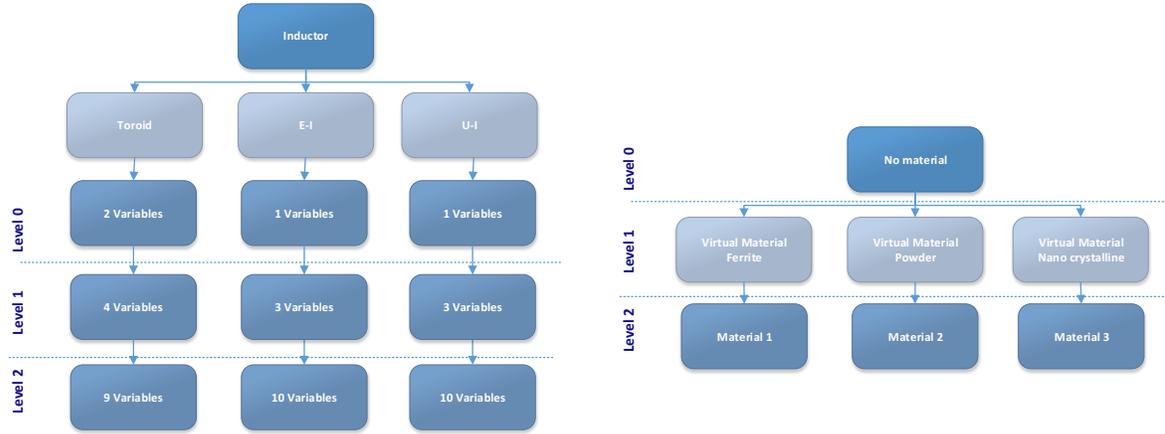


Figure 86: Inductor Granularity for the geometry and material

4.3.3. Model Definition

The geometrical representation is the same for all magnetic components and use the same inputs in our methodology (Table 14). It requires defining the different dimensions of the winding (square, round, Litz, etc. (4.2.2)), core(4.2.1), insulation layers and airgaps. For instance, there are different functions of calculation defined inside the magnetic object, depending on the conductor geometry. Examples of precise representations of E-type (a) and toroid (b) cores are given in Figure 87.

D_w : winding diameter	N_l : number of layers
n_s : number of strands (Litz wire)	d_{it} : distance between consecutive turns
l_w : core leg width	d_{il} : distance between consecutive layers
l : core leg thickness	ag : air gap distance
N : number of turns	al : air length

Table 14: Example of the inputs for the models of magnetic devices

In addition, many different placements of conductors in the winding are possible according to the type of application. Globally, only two cases are highlighted in terms of electrical performance: horizontal or vertical placements [123]. Geometrical outputs (e. g. conductor lengths, exchange surface, core volume, ...) can be derived from the different dimensions (weight, volume, surface...) and when the material properties are known, weight is easily derived as well. The precision of the geometrical model depends on the granularity of the geometry but remains very exact and reliable for the highest granularities when they are compared to manufacturer datasheets [130] or seller data.

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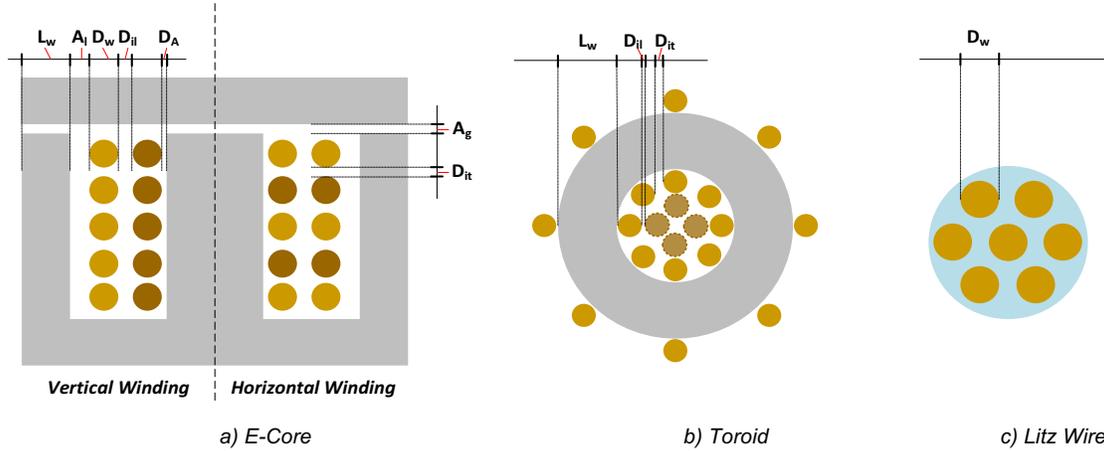


Figure 87: a) E-core b) Toroid Inductors Models, c) Litz Wire definition

4.4. Multi-Domain Models

The multi-domain models discussed in details in this section are the electric, loss, thermal and cost ones.

4.4.1. Reluctance model

Numerous electrical models can be found in the literature for different design requirements. The general representations considered for our optimal design are those that consider a perfect magnetic component, simple DC losses, AC losses, saturation or leakage as a function of the granularity. The calculations of the classical electrical parameters are directly linked to the device geometry, and are described in basic electrical engineering books [131] [132]. However, a more advanced representation is preferred in this thesis. Indeed, the assessment of the evolution of magnetic phenomena, such as the saturation current, is necessary to find the best design. However, it is difficult to apply the integral formulation of Maxwell on complex objects. In order to simplify this model, an analogy with the laws of Kirchhoff is possible based on the Reluctance, Capacitors and Inductors Permeance models [133] [79], as represented in (77) and Figure 88.

$$R(B) = \frac{\text{length}}{\mu_0 \mu_r(B) k_{fill} \cdot \text{Area}} = \frac{1}{P} \quad (77)$$

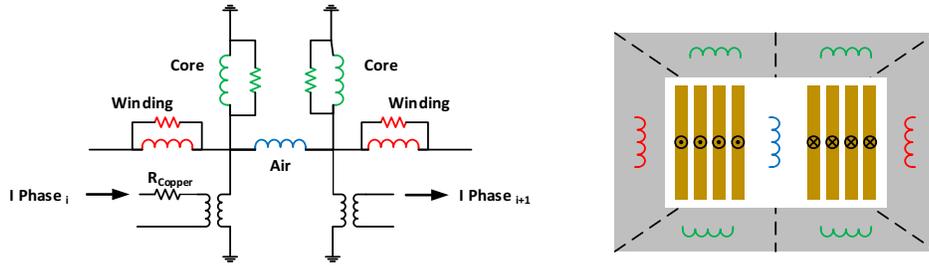


Figure 88: Equivalent reluctance models example

Indeed, with a simple interfacing between the electric and magnetic fields, it is easy to build this model from the device geometry. Each conductor is represented by a transformer, which is polarized in the direction of the current flow transit. This model can also combine various magnetic cores, which makes the definition of complex components more flexible (Figure 88). An example for an insulated ICT transformer similar to the one used in an isolated DC-DC converter such as the BBCU is given in Figure 89.

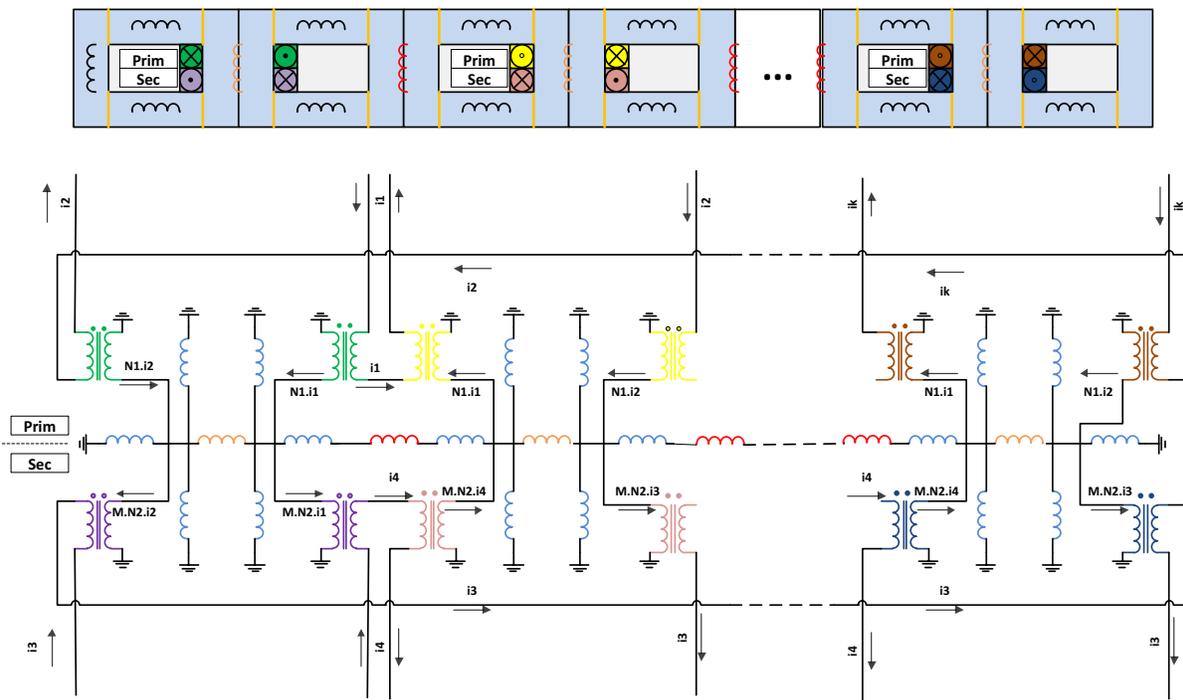


Figure 89: Example of a isolated transformers dedicated to multilevel DC-DC converter with the permeance model

In order to validate our reluctance approach created thanks the OOTEE frequency solver (Chapter 2), we have compared our output electrical signals with commercial solvers. An example is shown in Figure 90 for the electrical model of parallel inverters, whose phases are matched using coupled inductors [134].

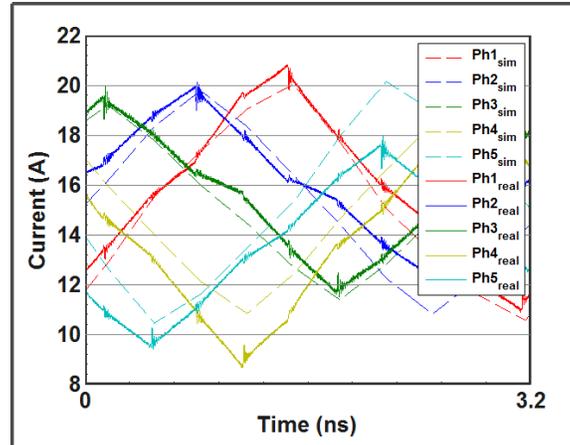


Figure 90: Comparison between Ootee and commercial solvers for interleaved inverters

4.4.2. Losses

a. Magnetic Losses

In the case of magnetic devices, an analytical model cannot estimate core losses. The losses of magnetic materials mainly vary depending on the frequency, maximum induction and temperature. The two best-known sources of losses in magnetic materials are hysteresis and eddy current losses. In [135], the author suggests adding the ferromagnetic resonance and the inter-granular barrier losses. The empirical model usually used is the Steinmetz model [136] [137], which is based on a sinusoidal regime. However, it is not broadband and more coefficients should be used to cover a wide frequency range. Similarly, it gives a monotonous evolution of the $f \cdot \hat{B}$ performance factor provided by manufacturers [138], while in practice this product presents a maximum. For these reasons, other empirical models with a wider domain of validity were developed. Analytical expressions are established in Table 15 [139]. The FF method has the advantage of being compatible with the use of loss models taking into account non-sinusoidal waveforms and only using the Steinmetz coefficients of the formulation, as described in [140] for the IGSE method. The second and more complete method offers a better accuracy but will be less flexible to use. These models match with the curves of the $f \cdot \hat{B}$ factor provided by the manufacturers with an average error of 5%, at an operating temperature of 100 ° C. It allows describing the behavior of the material with a low error margin and over a wide frequency range. Derivatives and more accurate calculation methods [140] are possible, for instance for ferrite core loss with non-sinusoidal waveforms, loss maps, gap losses or non-linearity [141] (Figure 91).

	Formulas	
Steinmetz	$L = Vol . k_1 . f^{\alpha_s} . B^\beta$	(78)
Oliver	$L = Vol . (k_1 . f^2 . B^2 + k_2)$	(79)
Tan Delta	$L = Vol . (f^2 . B^2 . e^{k_1} + k_2)$	(80)
FF	$L = Vol . k_1 . (t + s . f^{\alpha_s} + u . f^{\alpha_u} + v . f^{\alpha_v}) . B^\beta$	(81)
PC	$L = Vol . k_1 . (t + s . f^{\alpha_s} + u . f^{\alpha_u} + v . f^{\alpha_v}) . B^{w.f\beta_w+x.f\beta_x+z.f\beta_z+y}$	(82)

With $k_1, k_2, s, u, v, w, \alpha_s, \alpha_u, \alpha_v, \beta, \beta_x, \beta_w, \beta_z$ coefficient to calculate for each material, f the frequency [Hz], B the magnetic induction [T], Vol the core volume [m³] and L the iron losses [W].

Table 15: Different core loss formulas, adjusted by manufacturing data

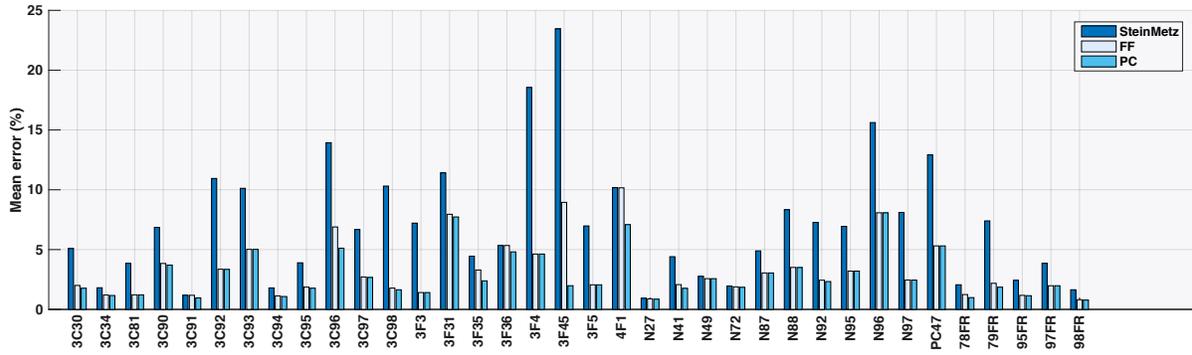


Figure 91: Error on the adjustment of manufacturing data with analytical models for the ferrite materials

Finally, the iron losses are calculated using the sum of all the harmonics. Indeed, this method provides a good approximation of the losses (83).

$$P_{Iron} = [k_1 f + k_2 f^2] . V_{Iron} \approx [k f^b] . V_{Iron} \quad (83)$$

From these equations, a scaling law can be deduced in order to extrapolate the losses in low granularity (84).

$$P_{Iron}^* = f^{*b} l^{*3} \quad (84)$$

b. Joules Losses

Joule losses represent a significant part of the total losses of a magnetic component. They are usually represented thanks to serial resistances and take into account the DC effect (85). However, AC loss calculation must also be made, and the case of inductors and transformers have to be handled in a different way, because of different characteristics of the magnetic field in the window, resulting in different assumptions for the creation of the models.

$$R_{dc} = \frac{\rho_w \cdot length}{S_w} \quad (85)$$

c. Transformer

In order to provide the AC behaviour of transformers, a one-dimension assumption on the distribution of the magnetic field can be established. The calculation of the Joule losses - including the skin effect - can then be performed in a purely analytical manner with a satisfactory accuracy [139]. The author of [142] solves the problem by calculating the AC resistance of conductors in a transformer for sinusoidal current. He explains the proximity effect mathematically by solving the Maxwell's equations for 1D models of transformers. Originally, his work only considers rectangular-section conductors. Currently, some adjustments are proposed to address the problem of round wires and conductors that do not fill the entire core window, or for other devices such as inductors [123]. An example of this ratio is presented in (86), with Q being the ratio between the conductor thickness and the skin depth Figure 92.

$$F_r = \frac{R_{ac}}{R_{dc}} = Q \frac{\sinh(2Q) + \sin(2Q)}{\cosh(2Q) - \cos(2Q)} + 2Q \frac{m^2 - 1}{3} \frac{\sinh Q - \sin Q}{\cosh(Q) + \cos(Q)} \quad (86)$$

A more advanced formula from [123] can be used in order to estimate the losses value for each layer of the winding (F_{rp}). For instance from this formula, it is recommended in the winding design that the most central layers (in the core window) get the smallest length since they have the highest F_{rp} value (87).

$$F_{rp} = \frac{R_{ac}}{R_{dc}} = Q \left(\frac{(p^2 + (p-1)^2)(\sinh 2Q + \sin 2Q) - 4p(p-1)(\sinh Q \cos Q + \cosh Q \sin Q)}{\cosh(2Q) - \cos(2Q)} \right) \quad (87)$$

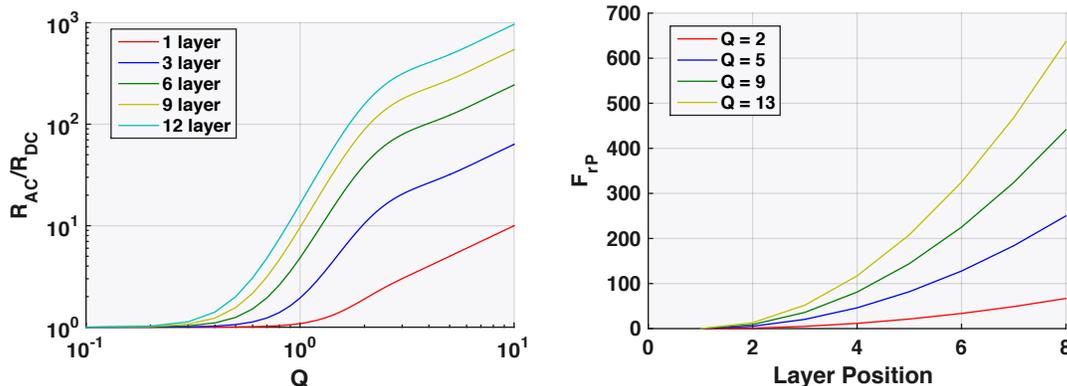


Figure 92: a) Variation of the AC resistance with Q factor b) FEM simulation of the current distribution in the winding

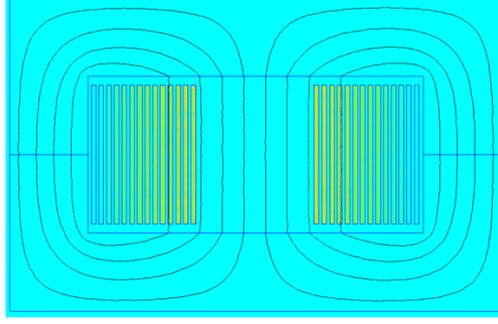


Figure 93: FEM simulation of the current distribution in the winding

Validation are performed with the FEMM software. In addition, empirical approximations for low granularity have been computed, such as the Levasseur formula [132] with (88) for round, and (89) for rectangular conductors. We can also find in [35], a complete methodology to design a transformer thanks to the area product.

$$F_{round} = \frac{R_{ac}}{R_{dc}} = 0,25 + \sqrt[6]{0,18 + \left[\frac{S}{\text{perimeter} \cdot \delta} \right]} \quad (88)$$

$$F_{plate} = \frac{R_{ac}}{R_{dc}} = \sqrt[8]{1 + \left[\frac{\alpha_{smallSide}}{2\delta} \right]^8} \quad (89)$$

d. Inductor

In the case of inductors, the problem is more difficult because the previous assumptions are no longer applicable and because of the presence of airgaps. However, we can propose several models depending on the conductor shape. Global winding losses can be expressed under (90) [143], with ξ being the function of the copper diameter and skin losses (91). Winding losses must be calculated for each winding turn and with a distinction between the inside and outside parts of the window [144]. An approximation of \hat{I}_L^2 [145] can be realized or simulations can be used.

$$P_{wdg} = R_{DC} \cdot X^{shape}(\xi) \cdot \hat{I}_L^2 \quad (90)$$

$$\xi = \frac{\text{diameter}_{cop}}{\sqrt{2}\delta_{cop}} \quad (91)$$

- Round and Litz: Well-known analytical solutions based on 1-D field approximation are available. They distinguish the skin and proximity effects called E_{skin} and E_{prox} (92). Their calculations are detailed in [146] [147]. The normalized field amplitude $H_{ext(f)}$, is expressed in [144].

$$X^{Round/Litz} = [E_{skin}(\xi) + E_{prox}(\xi)] \cdot \overline{H_{ext(f)}}^2 \quad (92)$$

- Foil and flat: Approximating an analytical equation for these geometries is very complicated because the 1-D assumption of a 2-D phenomenon implies many errors. Consequently, we used a more pragmatic approach and realized FEM simulations interpolated as surfaces [146] [147]. They are function of the frequency and the geometrical dimensions, with results that are stored in databases and called by our models. This work will be described in other

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following thesis of the laboratory, that have specially work on this point. In our case, we have only use the stored results.

4.4.3. Thermal Model

The temperature calculation of the magnetic components is achieved using simple models directly extracted from the literature. Only a global review is made here, since the aim were not to develop a model for this section. Deeper explanations can be found in [143] in order to understand the hypothesis, implementations et limitations of these models.

The first one assumes the same temperature is reached over both the core and the windings and a single exchange coefficient is used to describe both the radiation and the convection. As a result, he temperature difference between surrounding air and the magnetic components may be expressed as:

$$\Delta T = \frac{P_w + P_c}{h \cdot A_{TH}} \quad (93)$$

also propose a more advanced model that considers the hot spot calculation. It involves a model of coupling between windings and core and takes into account internal conduction effects (93) (Figure 94). In addition, the convection exchange coefficients are calculated using semi-empirical equations [144]. 2D and 3D models have been created to verify these hypotheses and the assumptions with a good accuracy (Figure 94). A relative error of -1,18% was found between the equivalent global thermal resistances.

$$R_{thCond} = \frac{l}{\lambda_{th} \cdot A_{TH}} \quad (94)$$

In addition, we calculate the radiated heat with ϵ_1 the emissivity and σ the Boltzmann constant and the convection, like in (95)(96), where the different elements of the equations and models are explained in [143].

$$R_{thRad} = \frac{l}{h_{rad} \cdot A_{TH}} = \frac{T_1 - T_2}{\epsilon_1 \sigma (T_1^4 - T_2^4) A_{TH}} \quad (95) \quad R_{thConv} = C_v \left(\frac{P}{P_{ref}} \right)^{0.477} \left(\frac{T_{amb}}{T_{ref}} \right)^{-0.218} \left(\frac{T - T_{amb}}{L^{0.285}} \right)^{0.225} \quad (96)$$

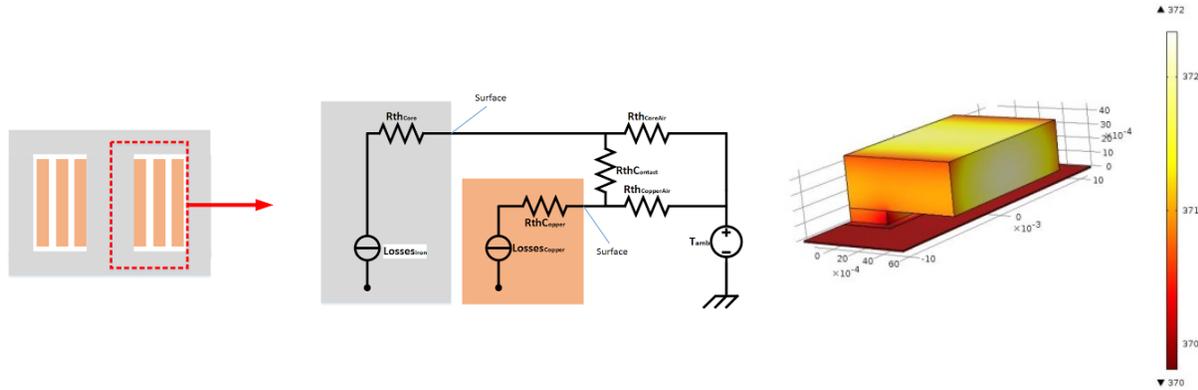


Figure 94: Simplified Thermal Model for a Magnetic Component

In order to validate the previous model, and in spite of the difficulty to obtain accurate thermal measurements via infrared devices, we only wanted to consider if our thermal models were in the right order of magnitude. Thus, by injecting an increasing power (20,35,50,75,90,100W), we have the temperatures on the surface of our transformer and compared it to our thermal models. Indeed, thanks to a Rogowski current probe, we have recorded very precisely the vector across our magnetic component, in order to inject it into our model and estimate the losses (Figure 95).

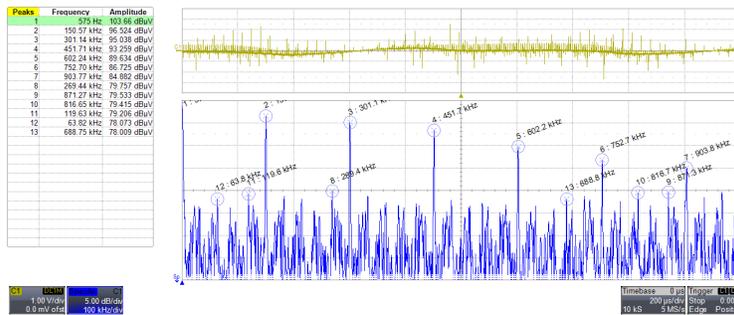


Figure 95 : Input transformer current measurement @50W

The experiment is presented in Figure 96.

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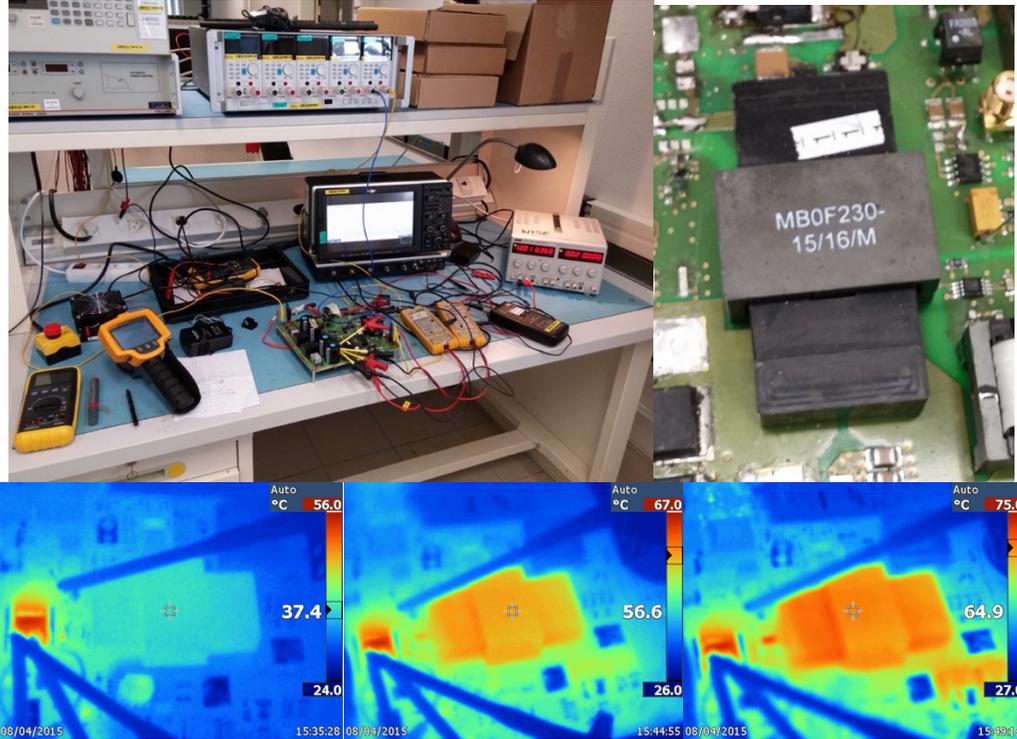


Figure 96 : Estimation of the surface temperature of a power transformer thanks to an infra-red camera

We obtained for the whole range of tested powers (6 cases) an average error of 21%, with a peak at 29% on the surface temperature estimation, which confirms the consistency of the model. However, at this point it is complicated to conclude. Indeed, a sole geometry has been tested, and we do not know if the remaining error is due to the losses estimations, the thermal model or even the measurement of our experience. Other more accurate thermal experimentations should be necessary to refine these results and bring a final validation.

4.4.4. Cost Model

The price of magnetic devices depends on the material quantity, i.e. on the volume of conductors and core, but also on the manufacturing process that allows assembling both parts of the device (97). Some coefficients for this equation, comprising the manufacturing cost, are proposed in [91] [144].

$$Price_{mag} = Price_{spe}^{Core} \cdot Vol_{core} + Price_{spe}^{Cond} \cdot Vol_{cond} + Manufacturing \quad (97)$$

We have studied the specific cost (as a function of the volume) of different core materials, i.e. ferrites, amorphous, Nanocrystalline and Si steel. From many internet seller websites, a database has been created in order to know the price of equivalent cores having different dimensions to deduce the cost models of Figure 97-a.

Regarding the copper material, we took into account the linear price as a function of the section area, or the diameter for round conductors (Figure 97-b). From the internet website seller, we have

found that the linear price is not linear as the function of the diameter. We suspect that this non-intuitive result is due to manufacturing/commercial problematics.

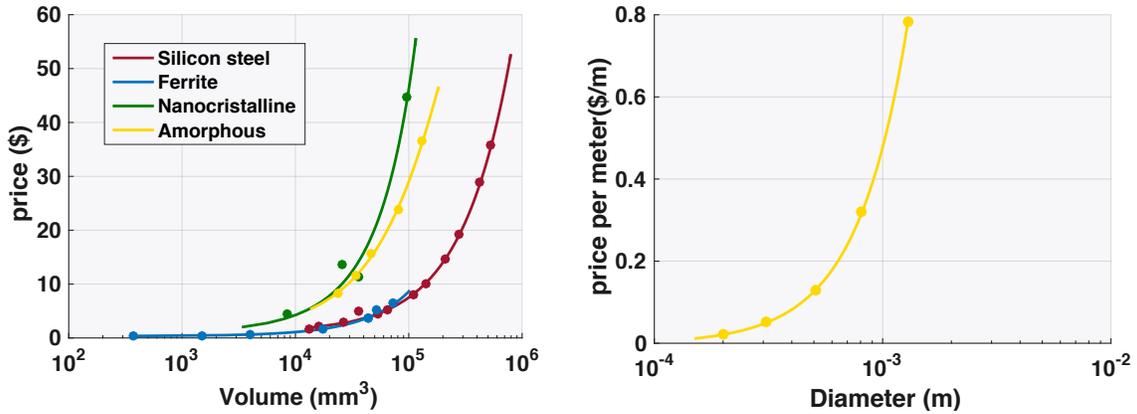


Figure 97: Cost models of the magnetic objects from diverse internet-seller references
 a) Prices of magnetic cores under quadratic polynomial forms as a function of their volumes
 b) Prices of a round copper material as a function of its diameter

A MOQ (Minimum Order Quantity) model for magnetics cores has been created thanks our price databases, that we have created thanks to internet and different seller sources, in order to find the reduction percentage. The following plot has been obtained (Figure 98).

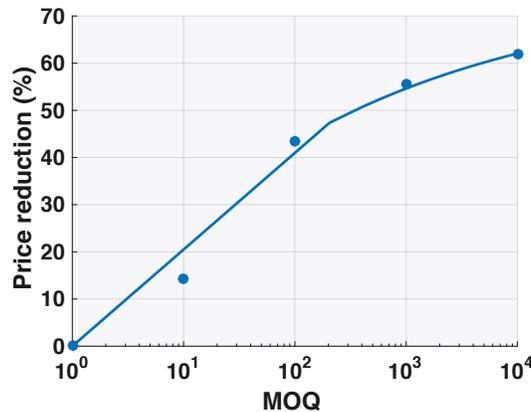


Figure 98: Mean price reduction for previous cores, as a function of the MOQ

4.5. Validation and Conclusion

Our continuous approach to create models of magnetics devices has been validated in different projects but in a restricted family part of magnetic components. We can provide as examples a HF transformer for low power supplies [148], isolated couplers for boost conversions in embedded networks, and not isolated couplers for DC-DC high power converters [149] [150]. Reference [144] provides the inductor designs for 3-ph PWM converters. In each case, a good correlation between

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the initial design and the final performance of the magnetic component has been obtained. Thus, a synthetic approach for magnetic components is available, with specific calculations depending on the geometries and on the operation point imposed to the device. The inductor requires more attention than other devices that are better known in the literature. For instance, the inductor requires more attention than transformers because Dowell's model for AC resistance in the windings cannot be used for inductors.

Part B: Capacitor devices

The purpose of this part is to propose modelling principles that allow designers to define continuous models of virtual capacitors. Then the geometry of these representative capacitors will vary in order to deduce their internal characteristics. From this theoretical device, it will be possible to find real or close samples in the standard production. These models must be adaptable to the main technologies, material, geometries and packages available on the market. First, we introduce the different technologies of capacitor on the market and their figure of merit in order to highlight the most appropriate capacitor for some applications and model creation. Second, we expose the principle of the continuous models, with different definitions of their geometry and granularities. Third, we propose different physical models to represent the behaviour of the capacitor model in our optimization software, before presenting validations and conclusions.

4.6. Capacitor Overview

4.6.1. Technologies

Capacitors are part of the family of passive components. They are mainly used for decoupling, energy storage, filtering and snubbers. To be adapted to a specific environment and application, a capacitor is mainly defined by its internal characteristics (e.g. nominal capacity, voltage breakdown, ESR), and so by its material composition, geometry and packaging. The main constraints applied to capacitors are related to the converter switching, which can generate high RMS currents, high-order current harmonics (tens of kHz in high power, hundreds of kHz or even above 1MHz for mower power application) and fast current variations (several hundreds of A/ μ sec. From these facts, an accurate model reflecting the behaviour of the capacitor is required for the optimal design of a power converter. Usually, the type of dielectric material defines the application domain. Several types of capacitors exist in the industry answering to the electrical, thermal or mechanical requirements. Very complete reviews of capacitors can be easily found in literature. The main types used by the industry in power electronics in 2012 are Ceramic (54%), Electrolytic (40%) and Plastic Films (6%), as represented in Figure 99 [151]. For each of these types, the geometry is different and Figure 100 shows the two main: square and round.

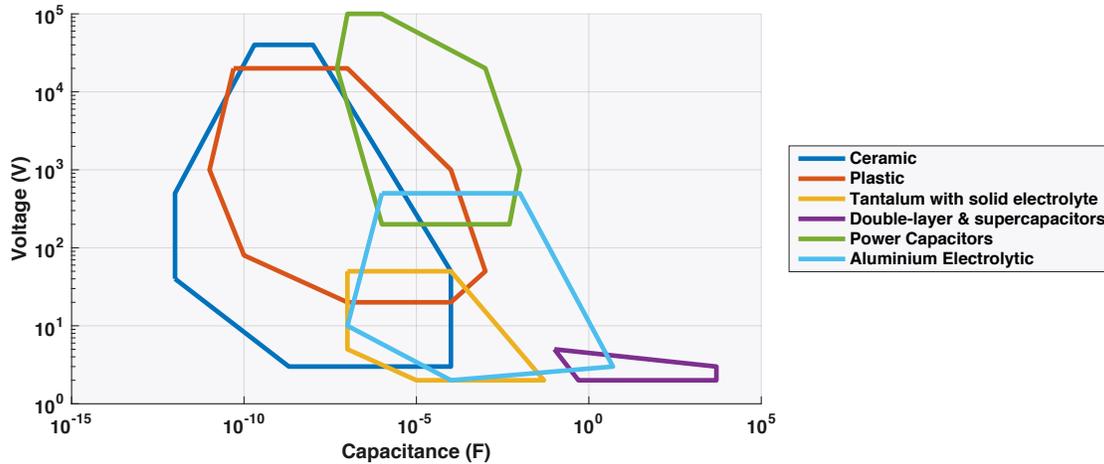


Figure 99: Voltage/Capacitance distribution for different technologies of capacitors (source : [152])

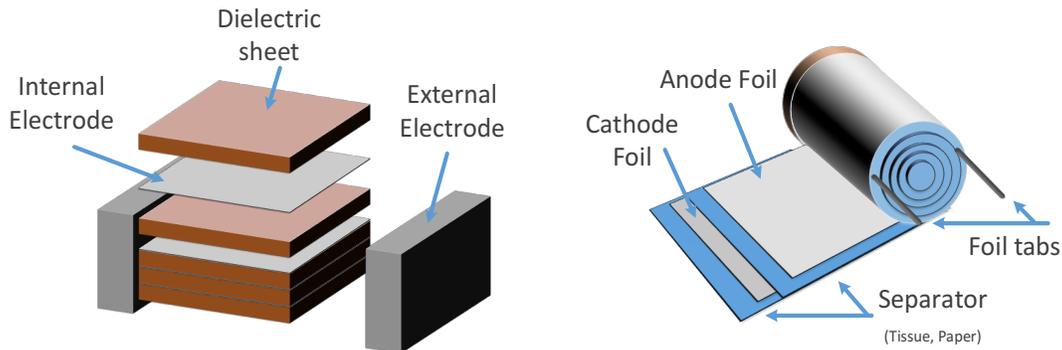


Figure 100: Typical construction of capacitors
a) Ceramic b) Electrolytic or Film

4.6.2. Figures of Merit

Among the huge database of samples provided by manufacturers, designers require criteria or Figure of Merit (FOM) to compare the different references. It allows them to find the most appropriate component for their application. In our case, FOM are useful to select samples to create our continuous models by regression analysis. Thus, five main factors exist to compare the capacitors:

- Capacitance
- Rms current
- Breakdown voltage
- Resonance frequency
- Secondary parameters: global volume, weight, cost, etc.

In order to take into account all of these criteria in one quantity and compare the capacitors, two FOM have been developed [16]. The first factor shows the evolution of the volume as a function of

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stored energy (98) while the second shows the evolution of the volume as a function of the admissible current (99). By combining both, we obtain the figure of merit used in Figure 101.

$$FOM_1 = C.V^2/Vol \tag{98}$$

$$FOM_2 = V.\frac{I}{Vol} \tag{99}$$

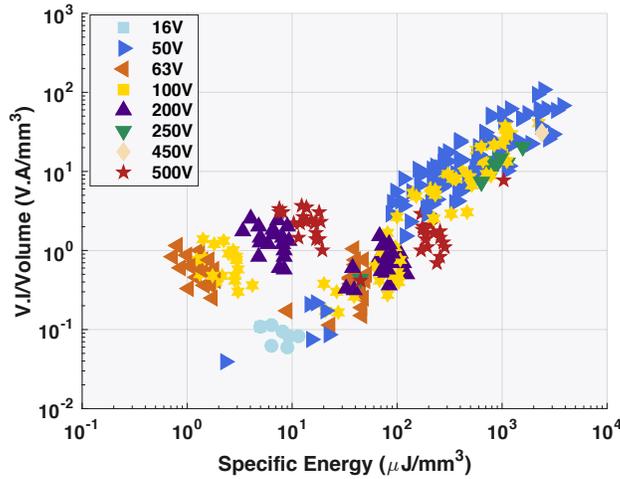


Figure 101: Figure of merit for ceramic capacitor

4.7. Principle of the model

4.7.1. Problem Setting

To introduce model of virtual capacitor and to consider its different aspects, it is convenient to establish the definition using a single equation. It is the “area product”: a famous principle often used for the design of magnetic components [55]. It leads to the following formulation:

$$Cte. (Vol)^{\frac{4}{3}} = A_{elec} \cdot A_{di} = W_C \frac{K_{WC} K_{elec}}{J_{RMS}(T, F, A_{elec}) \epsilon E_M(T, H, e) F} \tag{100}$$

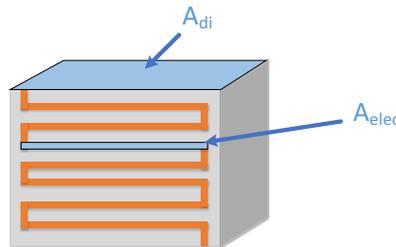


Figure 102: Figure of merit for Capacitor a) Ceramic b) Film

The different variables involved in this formulation are:

- Dimensions
- A_{di} developed surface of the dielectric, assumed as the surface of the capacitor
- A_{elec} , total electrode area
- E_M , dielectric thickness
- K_{WC} and K_{elec} , fill factor of the “winding window” for the dielectric and electrode layers (*shape of the conductors, insulation*)
- System specification
- W_c , stored energy
- F , operating frequency
- Main constraint
- T , operating temperature
- Internal Variables
- E_M , peak value of the electric field in the dielectric
- J_{RMS} effective current density in the electrodes

The description of the area product is applicable to different shapes such as rectangular or cylindrical capacitors. The proposed definition shows that the problem can be formulated according to the “direct modelling” explained in previous chapters (Chapter 2) and subject to the availability of loss models. The results of different modelling are available in the literature and provide a solid basis to address the subject of main technologies of capacitor, which we will explain hereafter.

4.7.2. Granularity

In order to propose different levels of description for capacitors in a pre-design scheme, we developed the following model with 4 levels:

- **Level 0** represents a global capacitor and includes all the types and technologies existing on the market. The simplest representation is required for this model, with no material or shape consideration. It can be achieved thanks to dimensional equations or scaling laws.
- **Level 1** represents a defined type of capacitor, i.e. Film, Electrolytic or Ceramic. A material for each type of dielectric can be considered in this case, as well as different shapes. Analytical equations based on a simple architecture are sufficient to obtain satisfying results with minimal computation resources.
- **Level 2** represents a specified technology of dielectric. For instance, PP, PET or PETS dielectrics are available for the “Film” type. A deep representation of its geometry and parameters is required to perform the most accurate simulation of this component.
- **Level 3 or discrete level** loads sample references from databases and can use scaling laws on specific device if required.

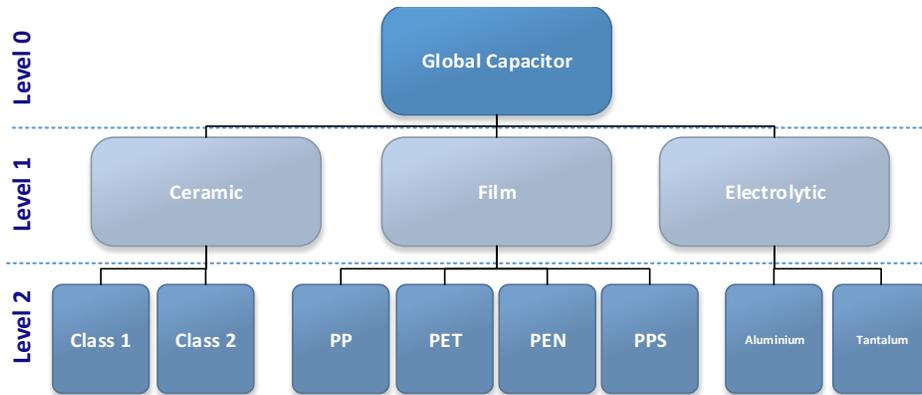


Figure 103: Granularity of the capacitor models

4.8. Model Definitions

4.8.1. Inverse Model

When the designer thinks he knows what capacitance is required and what maximum voltage will be applied, he may use the inverse model to determine the size and weight of the capacitor. These parameters determine the energy that must be stored in the capacitor, and this can be linked to the volume and weight of the device (101). Such a model is proposed in [153] and illustrated in Figure 104.

$$Weight_{direct} = a + b \cdot (Energy_{stored})^c = a + b \cdot \left(\frac{1}{2} CV^2\right)^c \quad (101)$$

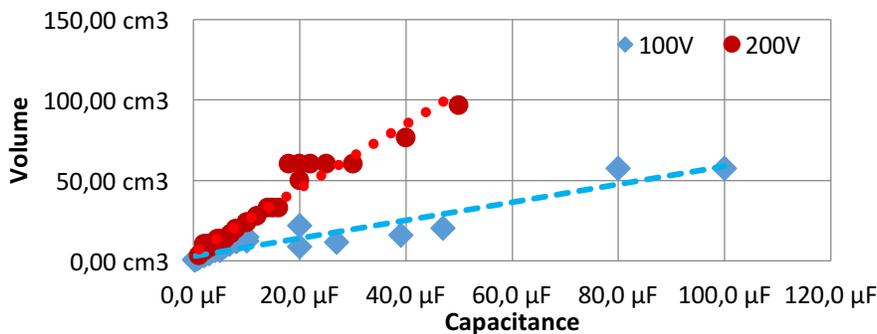


Figure 104: Estimation of the volume of film-square capacitors extracted from our database (several manufacturers), as a function of two electrical characteristics: the capacitance and voltage (100 and 200V)

4.8.2. Direct Model

There are two ways to build a direct model of capacitor: it can use as inputs either the internal or the external dimensions defining its geometry (Figure 105). In order to reduce the number of inputs of the model, form factors can also be imposed by creating ratios between the different dimensions.

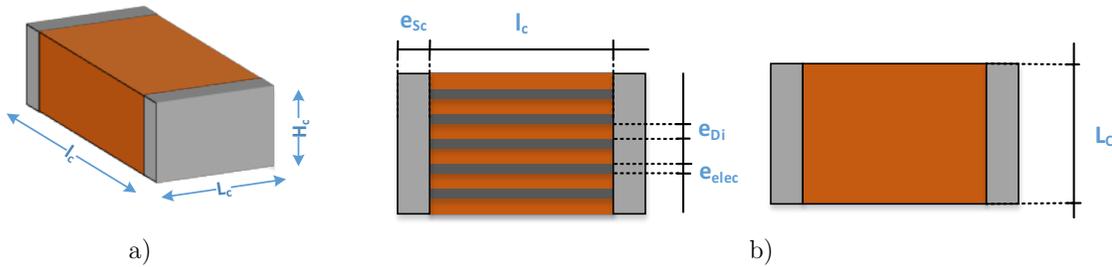


Figure 105: Basic pattern of the elementary capacitor
 a) external geometry definition b) internal geometry definition

a. External definition

The datasheets often define the capacitor by its external dimensions, i.e. lengths, width, and height for a rectangular capacitor (diameter and height for a cylinder form) (Figure 105-a). Although we need to know the internal structure of a capacitor to define its behaviour thanks to physical equations, here we only want to use the external dimensions to approximate a relevant model. This representation assumes that all the studied capacitors possess an equivalent internal architecture. It is very convenient, as it allows handling wide ranges of capacitors extracted from databases and creating response surfaces with a very good accuracy. Indeed, physical characteristics can be directly linked to the external dimensions of the capacitors, as summarized in Table 16. The inputs to define this model based on its external dimensions and depending on the available data are:

- **Surface or Volume**, dimensions that are proportional to the capacitance,
- **Thickness or Voltage** that represents the breakdown voltage of the device,
- **Shape**: round or square, described by different calculation methods,
- **Type**: technological family (e.g. film, ceramic, electrolytic),
- Dielectric material, (e.g. PP, PET),
- **Metallization**, (e.g. aluminum),
- **Level**, definition of the granularity (4.7.2).

	Physical Equations	Scaling laws
C	$C = \frac{Area}{thickness}$	# $\frac{Area}{thickness}$
ESR	$ESR = \frac{\sigma}{\epsilon' \omega^2 C}$	# $\frac{thickness}{Area}$
$R_{electrode}$	$Re = \rho \frac{length}{Width \cdot thickness_{elec} n_{elec}}$	# $\frac{length}{Width \cdot thickness}$
ESL	$L_{flat} = k_1 \cdot l \left[\ln \left(\frac{2l}{w+t} \right) + k_2 + k_3 \left(\frac{w+t}{l} \right) \right]$	#length
R_{th}	$R_{th} = \frac{1}{k} \frac{length}{Area}$	# $\frac{length}{Area}$
Weight	$weight = k \cdot volume$	#volume

Table 16: Main physical relations between the dimensions and internal characteristics of a capacitor

b. Internal definition

The idea here is to define the internal architecture of the capacitor, i.e. precise each element and layer constituting it (Figure 105-b). This approach is equivalent to the methodology exposed in the magnetics section, that provides very good results. Instead of using databases, we describe real physical equations by knowing each detail of the geometry. In practice, it is often impossible to know precisely the internal architecture of a given device. There are too many different topologies to generalize an accurate definition on a wide range of samples (Figure 106). Therefore, to overcome this problem, we consider a capacitor constituted of a simple assembly of successive dielectric and electrode layers. Additional correction factors can be applied, in order to get closer of specific technologies and reality, with a database calibration. This calibration is realized thanks to chosen real samples of our database, to get the minimal mean error on the different main physical parameters of the model compared to the real devices.

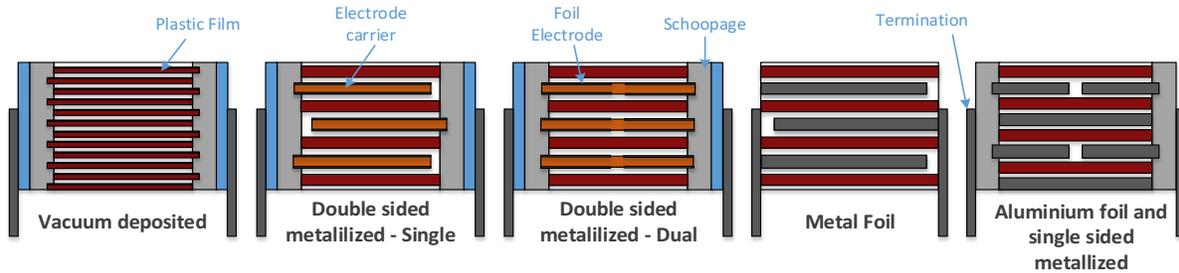


Figure 106: Main different internal architecture of capacitor devices

The study of different capacitor geometries has been realized through an equivalent cuboid capacitor based on [35]. Thus, the inputs based on its internal dimension are:

- **Length, Width or Surface**, dimensions that are proportional to the capacitance
- **Dielectric thickness**, dimension defining the voltage breakdown
- **Thickness internal/external electrodes**, dimension of the electrodes inside or outside the device, mainly responsible of the joule losses
- Number of layers
- **Shape**: round or square, with different calculation methods
- **Type**: film, ceramic or electrolytic, representing each main technology (e.g. Film, Ceramic)
- **Material**, to precise a specific material to gain in precision (e.g. PP, PET)
- **Level**, definition of the granularity (4.7.2)

4.8.3. Macro-Capacitors and Database selection

Assembling capacitors in series or parallel allows creating macro-capacitors with improved physical characteristics (Figure 107). For instance, and based on simple electrical equations (Table 17), series connection of capacitors can be used to increase the breakdown voltage. On the other side, assembling capacitors in parallel can increase the capacitance value, the effective current capability and the equivalent thermal resistance. Mixing both associations can also be considered in order to form new macro-devices, called multi-stacked capacitors on the market (only for parallel

configuration). They confirm their advantages (gain of space), but also show lower ESR, and equivalent ESL for higher capacitances values [154]. Moreover, with this principle and a reference capacitor, it is easy to find the optimal combination of parallel devices that satisfies the expected parameters of an application (greater or equal to V_{min} , C_{min} , I_{min} for instance), in terms of objectives such as weight or cost.

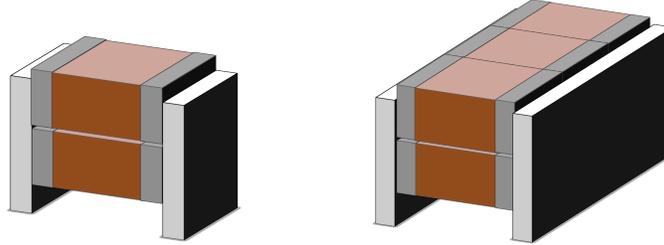


Figure 107: Macro capacitors, with parallel associations

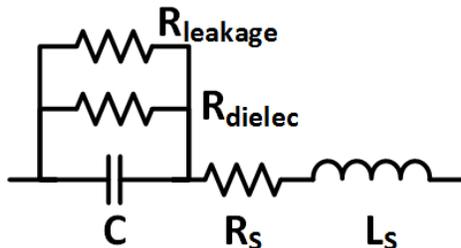
Equivalent parameter	Physical Equations
V_{eq}	$V_{eq} = V_{capa} \cdot n_{ser}$
$ESR_{eq}/R_{th_{eq}}$	$R_{eq} = \frac{R}{n_p}$
C_{eq}	$C_{eq} = n_p \cdot \frac{C}{n_s}$
I_{eq}	$I_{eq} = n_p \cdot I$
$Weight_{eq}/Volume_{eq}$	$Vol_{eq} = Vol \cdot n_{ser} \cdot n_{par}$

Table 17: Equivalent parameter for multi-stacked capacitors

4.9. Multi-Domain Models

4.9.1. Electrical

The electrical model has to translate the different imperfections of the capacitor. It is commonly composed of an RLC circuit composed of L_s the serial inductance, R_s resistance of the electrodes and C the proper capacitance. A most advanced representation [4], adds two resistors simulating the losses of the dielectric R_{dielec} and leakage $R_{leakage}$, as shown in Figure 108. More complete models can be found in literature, representing very specific technologies [7], temperature dependence, DC bias [5], or aging time [6].



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Figure 108: Classical advanced electrical model for a capacitor

Electrical parameters of a capacitor are directly connected to the dimensions of the device. Thus, it is easy to calculate these parameters from dimensions. We can remind the expression of the main electrical quantities (resistance equations are developed below):

- **Capacitance**, with ϵ_o the electric constant and ϵ_r the relative static permittivity (102).

$$C = \epsilon_o \epsilon_r \frac{\text{Surface}}{\text{thickness}_{\text{dielectric}}} \quad (102)$$

- **Breakdown voltage**, with E_{rupt} the dielectric strength and K_{Margin} a margin coefficient (103).

$$V = \text{thickness}_{\text{dielectric}} \cdot E_{rupt} \cdot K_{Margin} \quad (103)$$

- **Stray inductance**, derived from the length of external connections through an empirical equation ($1e^{-6}$ H/m)

4.9.2. Losses Models

a. Losses Calculation

Loss calculation can be approached by different manners: separately by detailing the different loss phenomena, useful when the object is describe internally, for each layer and describe by physical equations (4.8.2.b); or globally, that is useful when we describe the capacitor object with its external dimensions and extracted from datasheets (4.8.2.a);

In the first case, we separate the two types of losses where the total losses are the simple sum of both phenomena:

- **Dielectric losses** due to an applied AC electric field on a dielectric material
- **Joule losses** caused by the current flowing through the electrode layers and metallic connections

To formulate the sum of these two types of losses, a practical approach often used in the industry is to characterize materials by their respective resistances or dissipation factors (DF or $\tan \delta$). Thus, the global DF is expressed by (104) or formulated as a serial resistance when the capacitance and the frequency is known, and conversely.

$$\tan \delta_{\text{total}} = ESR \cdot C \cdot w = \tan \delta_{\text{Dielec}} + \tan \delta_{\text{Electrode}} \quad (104)$$

By considering that the current flowing in the capacitor is rarely sinusoidal (it means to take into account the harmonics of this current), we reach a final expression of the total losses (105), with the total factor losses $tg\delta_{\text{total}(h)}$ and an order of harmonic h . This approach is really useful when we describe by its internal architecture the capacitor.

$$L_{tot} = \sum_{h=0}^{\infty} [P_j(f) + P_{dielec}(f)] = \sum_{h=0}^{\infty} \frac{tg\delta_{total(h)}}{C2\pi hF} I_{heff}^2 = \quad (105)$$

In the second case, to simplify the loss models, a common way is to neglect the dielectric losses by only considering a global *ESR*, depending or not on the frequency and often extracted from datasheets (106). This method is used when we describe the capacitor object thanks to its external dimensions. At low frequencies, this *ESR* is close to the serial resistance *Rs*, the resistance of the electrode, but it increases at higher frequency because of skin effect. The *ESR* is generally higher for devices with a higher rated voltage (Figure 109).

$$L_{tot} = \sum_{h=0}^{\infty} ESR(f_h) \cdot I_{eff}^2(f_h) \quad (106)$$

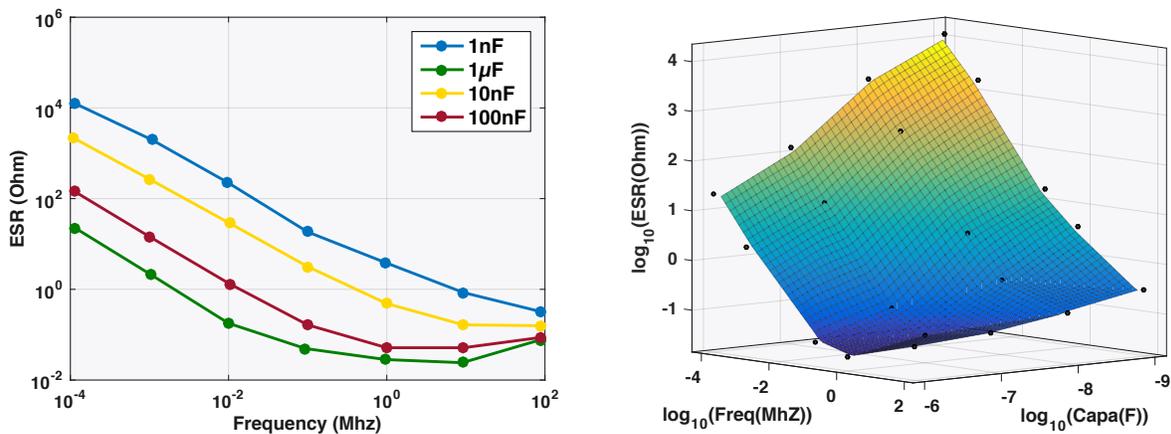


Figure 109: ESR evolution for Ceramic Capacitors

a) X7R capacitors as a function the frequency, for different capacitances

b) X7R capacitors as a function the frequency and the capacitance

b. Current-Best Dielectric

As expressed previously, we need to model the dissipation factor of the best dielectric materials. Dielectric losses relate to the intrinsic properties of the dielectric material used and are very difficult to determine analytically. The curves of dissipation factors ($tg \delta_{Dielec}$) vs frequency – provided by manufacturers for the main materials – are approximated by analytical expressions (Figure 110) for frequencies between 1kHz and 1Mhz. A virtual material gathering the best properties of each type of material, is also possible. It is also interesting to notice that in decoupling applications with an almost constant voltage, the dielectric losses are negligible that allow to not consider them in the loss model.

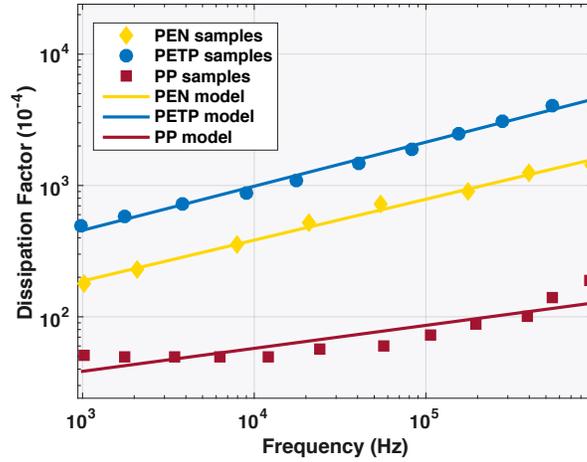


Figure 110: DF approximation by linear models.

c. Joule Losses

The current flow in the electrodes and metallic interconnections creates joule losses, which can be significant because of the large RMS currents associated with the typical power electronics applications. Numerous Joules losses expressions exist in literature, especially with the association of a dissipation factor $tg\delta_{elec}$. The consideration of these losses requires a fine analysis. However, we need a simple enough model to be used in the predesign context, for cylindrical and rectangular geometries. In [155] and simplified in [35], the author proposes a loss model based on the study of the electrical potential along an electrode. He deduces the expression of the active and reactive power per unit area on the electrode, and so finally calculates the final joules losses. Thus, we obtain a DF that exclusively depends on the geometrical configuration of the capacitor. The most advanced mathematical forms involve Bessel functions. However, a simplification gives close results for frequency up to the MHz [156]. For a given geometry (our elementary square capacitor for instance) we have as analytical expression the DF $tg\delta_{elec}(F)$ (107), with L_{capa} the length of the elementary capacitor, k a coefficient, ρ_{elec} the electrode resistivity, e_{elec} and e_{dielec} the thickness of electrode and dielectric layers, f the frequency and m_i the isolation margin thickness.

$$tg\delta_j = L_{capa} \frac{\sinh(kL_{capa}) - \sin(kL_{capa}) + k \left(1 + \frac{4m_i}{L_{capa}}\right) \cdot [\cosh(kL_{capa}) - \cos(kL_{capa})]}{\sinh(kL_{capa}) + \sin(kL_{capa})} \quad (107)$$

$$\text{with } k = \sqrt{\frac{4\pi f \epsilon_0 \epsilon_r \rho_{elec}}{e_{dielec} e_{elec}}}$$

Finally, we can present the behaviour of a global ESR calculation, including the dielectric and joule losses definition (Figure 111).

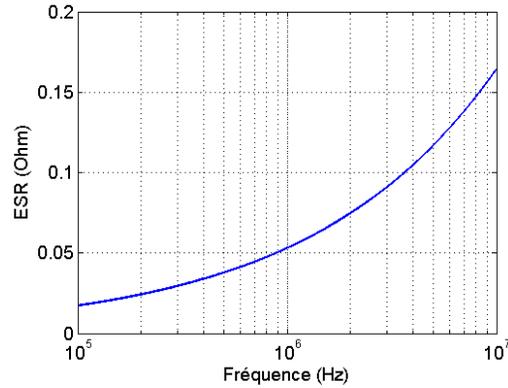
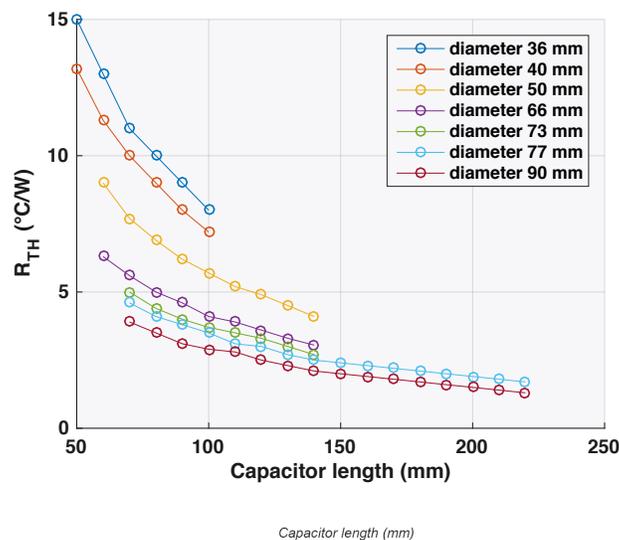


Figure 111 : Example of theoretical calculation of a global ESR for an elementary film square capacitor from previous equations [156]

4.9.3. Thermal Model

Whatever technology is considered, the maximum operation temperatures of capacitors are relatively low ($\approx 85^\circ\text{C}$). Moreover, additional effects occur with the temperature rise, for example an aging effect of the dielectric. Losses are responsible for this temperature increase and can be approximated thanks to an equivalent thermal model. We can consider the three main heat transfer modes: conduction between the different architectural layers, convection with the surrounding air, and radiation exchange with the environment. The thermal model of the capacitor has to express the evolution of the temperature to guarantee its operability under maximal constraints. It can be realized thanks to different methods:

- **Regression:** a thermal resistance R_{th} is obtained directly by regression from databases in order to provide a thermal model as a function of the dimensions (Figure 116).



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Figure 112: Thermal resistance as a function of the length of cylindrical electrolytic capacitor, for different diameters

- **Meta Model:** we introduced an analytical meta-model of an electrolytic capacitor, realized in partnership with INSA Toulouse. This approach is based on a dimensional analysis of the problem, that is finally expressed as in (108) with associated coefficients (Table 18). This method is called SLAWMM [157]. More information can be found in relative thesis works such as [158] [159] [160] to find all the details of this calculation and example exposed hereafter.

$$R_{th} = k_0(k_1 + k_2\pi_1 + k_3\pi_1^2) \cdot (\pi_4^{k_4} Gr^{k_5}) D^{(a_0+a_1Gr+a_2\pi_1+a_3\pi_1^2+a_4\pi_4)} \quad (108)$$

k_0	k_1	k_2	k_3	k_4	k_5
-2.04-2	0.9226	-58.5757	22.697	-0.239	-0.01959
a_0	a_1	a_2	a_3	a_4	
-1.329	1.99E-9	0.077	-0.06997	-3E-4	

Table 18: Numerical values for the thermal meta-model ($T_{inf} = 100^\circ C$) with $\pi_1 = \frac{Diameter}{Length}$, the thermal conductivity ratio $\pi_4 = \frac{\lambda_z}{\lambda}$ and the number of Grashof (Gr)

After validation with the finite element COMSOL software (Figure 113), we observed that the analytical laws provide a good estimation of the thermal resistance, with an error between 5% to 20%.

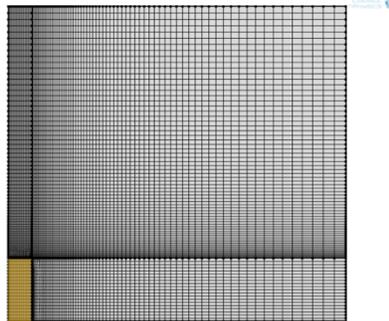


Figure 113: Numerical model simplified for the COMSOL study of a capacitor cut, assuming that the capacitor is composed of a single material that the losses will be dissipated in the whole volume and not localized on the electrodes only.

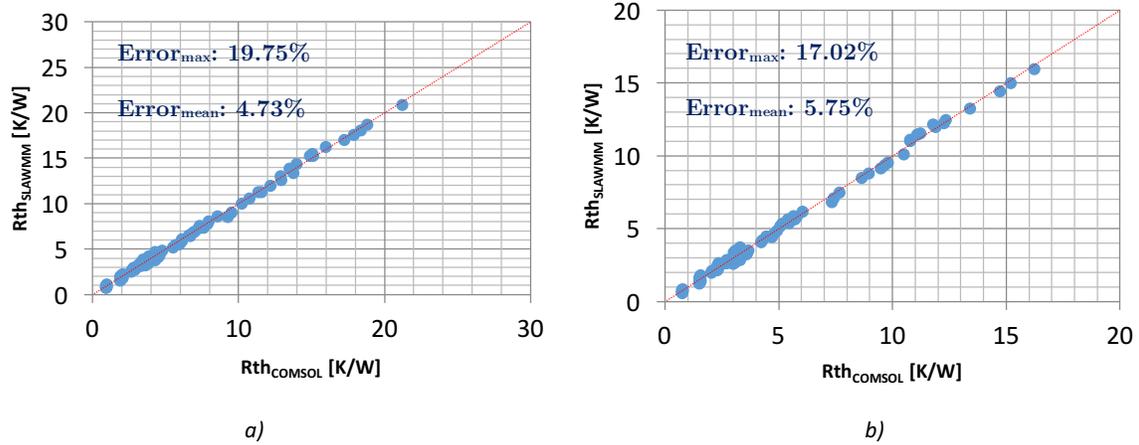


Figure 9 : Comparison of the heat resistance obtained by the scaling law after non-linear regression with the thermal resistance evaluated on COMSOL for two external temperatures

a) $T_1 = 25^{\circ}\text{C}$. b) $T_2 = 100^{\circ}\text{C}$.

- **Exchange coefficients:** they allow simple analytical equations for the estimation of surface temperature elevations between the capacitor and a fluid. First, we consider a total homogeneous surface temperature calculated from previous losses, and a global heat transfer coefficient based on radiation and convection. Second, we achieve a more advanced representation by considering different convection coefficients, depending on the surface location on the capacitor [161] (Figure 114). The radiative coefficient is considered as a constant on the studied temperature range (20° to 85°). Finally, we obtain equations (109).

$$\Delta T_{CA} = \frac{P_{totalC}}{h \cdot A_{TH}} = \frac{P_{totalC}}{h1 \cdot A_{TH1} + h2 \cdot A_{TH2} + h3 \cdot A_{TH3} + R \cdot A_{th}} \quad (109)$$

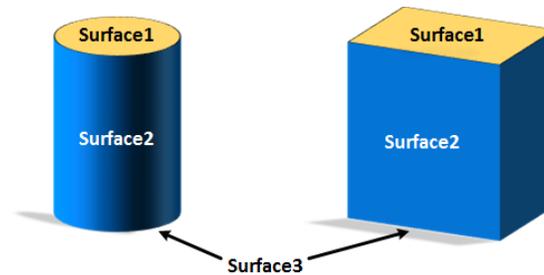


Figure 114: Location of the different exchange surfaces for two capacitor geometries

- **Nodal network:** Unlike the previous cases, a method of temperature estimation of the hot spot is introduced. The hypothesis chosen is to consider the multi-layer capacitor as a quasi-homogeneous material (but with an anisotropic thermal conductivity), allowing a general formulation more accessible compared to hybrid systems like magnetic components (Figure 111). In order to ensure the compatibility with a low computational cost, the chosen path is to "mesh" the capacitor and to assign a thermal equivalent network to each area created.

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The network is excited by a source of local losses with supposedly constant volume losses. Moreover, we place this 3D problem into a 2D representation. The thermal resistances associated are determined from the dimensions of the corresponding area and from two factors:

- a radial conductivity λ_{Radial} corresponding to the thermal conductivity of the association of the dielectric series and armature (110).

$$\lambda_{\text{Radial}} = \frac{e_{\text{Electrode}} + e_{\text{Dielec}}}{\frac{e_{\text{Dielec}}}{\lambda_{\text{Dielec}}} + \frac{e_{\text{Elec}}}{\lambda_{\text{Elec}}}} \quad (110)$$

- an axial conductivity λ_{Axial} corresponding to the thermal conductivity of the dielectric series parallel association and armature (111).

$$\lambda_{\text{Axial}} = \frac{e_{\text{Electrode}} \lambda_{\text{Elec}} + e_{\text{Dielec}} \lambda_{\text{Dielec}}}{e_{\text{Electrode}} + e_{\text{Dielec}}} \quad (111)$$

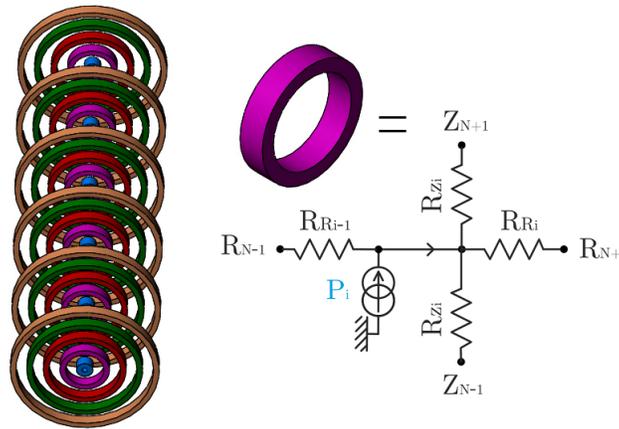


Figure 115: Equivalent local nodal network for the thermal model of a multi-stacked capacitor [156]

The resolution of the complete network is relatively simple – even with hundreds of nodes – and more economical than the numerical solution of the Fourier equation [9]. The results of this approach have been compared with those obtained by a digital resolution. Figure 116 shows this comparison for different capacitor dimensions and the quite good agreement between the two methods.

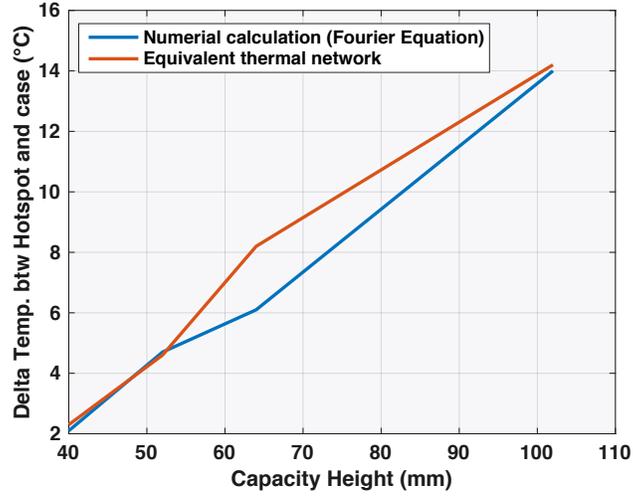


Figure 116: Validation of the nodal thermal network thanks to a finite element simulation

4.9.4. Cost Model

The price of capacitors varies depending on their specifications. We created a cost model for all types of capacitors (ceramic, film and electrolytic), based on data from 2015 and using separate databases with different Minimum Order Quantities (MOQ). As already stated in [91], the price of the film and ceramic components scale linearly with the rated capacitance C_r and the Voltage V_r , but the energy stored becomes cheaper for higher rated voltages because of the voltage quadratic term. It is partly due to low manufacturing cost of thicker dielectrics, which are used for higher rated voltages around 2-3kV. Equation for the capacitors considering both film and ceramic material is given by (112).

$$Price_{capa}^{Film} = a_{capa}^{Film} + b_{capa}^{Film} \cdot V_r + c_{capa}^{Film} \cdot C_r = a_{capa}^{Film'} + b_{capa}^{Film'} \cdot V_r + c_{capa}^{Film'} \cdot S_r \quad (112)$$

For the electrolytic devices, the price scales with the energy stored as shown in the equation below (113).

$$Price_{capa}^{Elec} = b_{capa}^{Elec} \cdot V_r + c_{capa}^{Elec} \cdot C_r V_r^2 = b_{capa}^{Elec'} \cdot V_r + c_{capa}^{Elec'} \cdot S_r V_r^2 \quad (113)$$

In our case, we have created models based on a direct modelling, i.e. by using as inputs the voltage, the image of the dielectric thickness and the surface of the stacked layers. We show both approaches in Figure 117 for ceramic and electrolytic capacitors.

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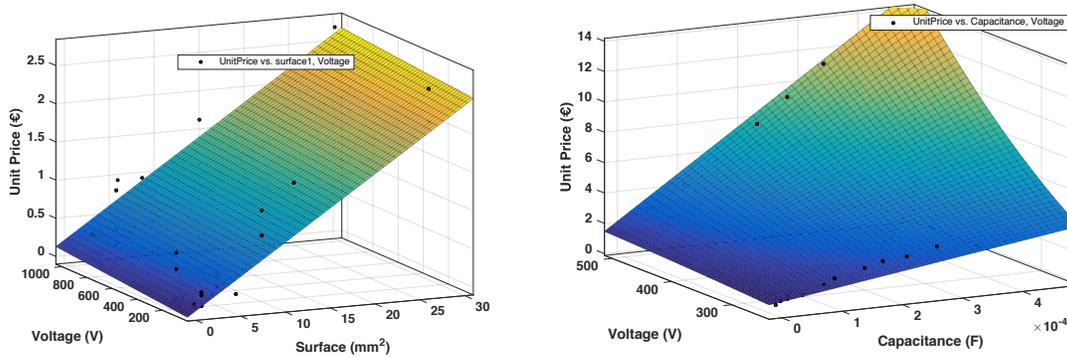


Figure 117: Cost model of capacitors from MOUSER website partnumbers with as evaluating goodness of fit: the SSE the Error Sum of Squares, R-square the coefficient of determination and RMSE the root-mean-square error

- a) Ceramic (SSE: 1.672 -R-square: 0.8946- RMSE: 0.2639)
- b) Electrolytic (SSE: 2.801- R-square: 0.9908- RMSE: 0.4184)

In addition, we provide a MOQ using our price databases, in order to create a global factor to apply on the unit cost. Then, we calculate a price reduction as a function of the order quantity, as shown in Figure 118 for electrolytic capacitors.

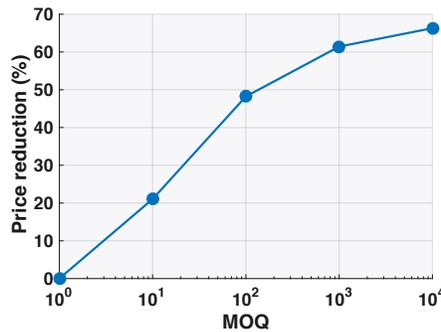


Figure 118: Minimum Order Quantity model (MOQ) for electrolytic capacitors from MOUSER website partnumbers

4.10. Validation

The model validation defined by its external dimensions depends on the quality of the regression curves. From our experience, the average error margin is often lower for the highest granularity at 10%. We give an example of the capacitance and loss model as a function of the volume in Figure 119.

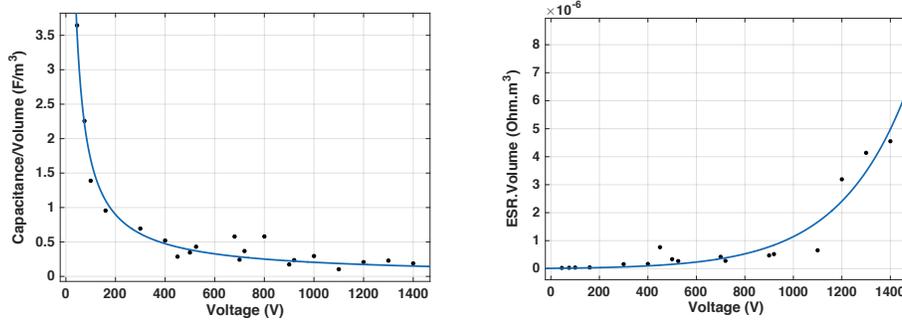


Figure 119: Example of film Capacitors regression a) Capacitance model (SSE: 0.389 - R-square: 0.972 - Adjusted R-square: 0.9709 - RMSE: 0.1471) - b) ESR model (SSE: 2.944e-12- R-square: 0.9155 - Adjusted R-square: 0.896 - RMSE: 4.759e-07)

In order to define the model by its internal architecture, we used the most precise physical equations developed in this chapter, and then tested them on reduced family of components for cylindrical and rectangular capacitors. In addition, we added correction factors to fill our lack of knowledge about the internal architecture of the samples chosen. The calculation of these coefficients is performed automatically in order to obtain the smallest average error. We got the Figure 120 and Figure 121. Thus, we see that the weight error of models is very low. However, electrical (capacitance), thermal (Rth) and loss models (global ESR including joule and dielectric phenomena) have a maximum of 25% error. This is more than the external model. As a conclusion and knowing that we put strong hypothesis on the internal architecture, the results are finally quite good. All the models are available and commented in the library Comp3d of the laboratory.

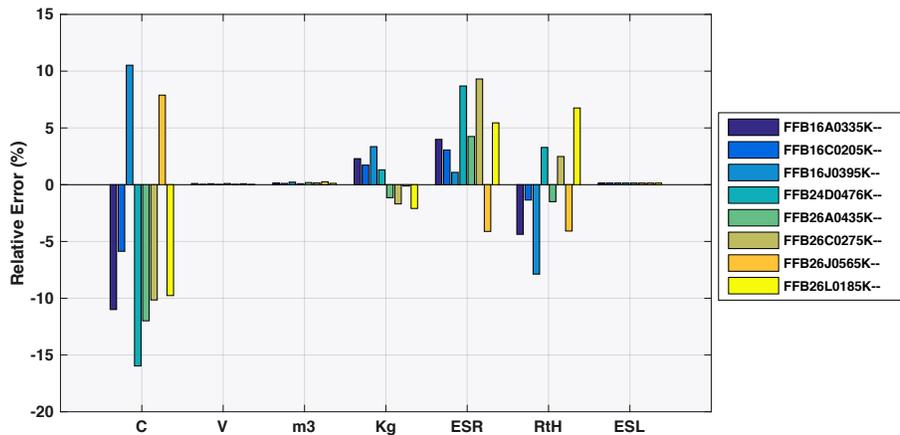


Figure 120: Validation of the “internal geometry” definition model on film rectangular capacitors (AVX) (C the capacitance, V the voltage calibre, m3 the volume, Kg the weight, ESR the serial resistance, Rth the thermal model, ESL the serial inductor).

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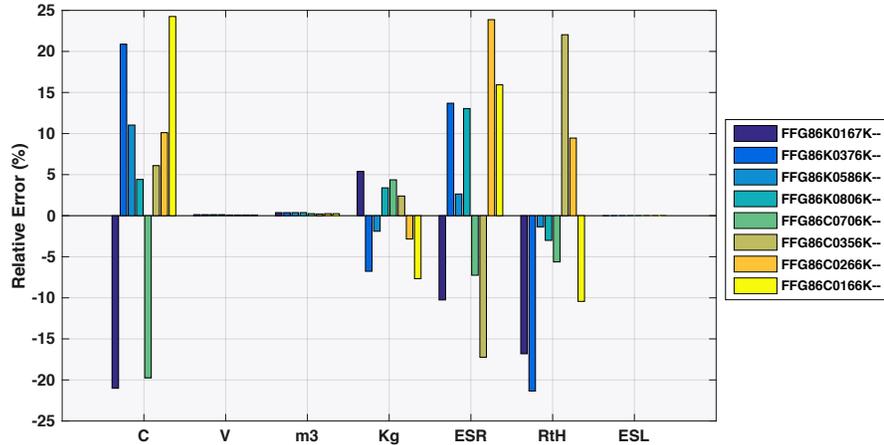


Figure 121: Validation of the “internal geometry” definition model on film cylindrical capacitors (AVX) (C the capacitance, V the voltage calibre, m^3 the volume, Kg the weight, ESR the serial resistance, R_{th} the thermal model, ESL the serial inductor).

4.11. Conclusion

A direct modelling of capacitors has been presented in this chapter according to two axes: an external definition of its geometry based on database regressions or response surfaces; and an internal definition based on physical equation and a simplified geometry, in order to describe the physics inside a power converter. Our models are meant to represent the industrial reality. But this reality is complex because of the number of manufacturers and the variety of technological variants and proprietary manufacturing methods. These models may only be representative of an average representation in each technology. Because these components are selected on the shelf (COTS), we cannot show a design example. Nevertheless, different polypropylene film capacitors calculated by the corresponding procedure have been compared with samples of the same "capacity / voltage" characteristics. Volumes and admissible current observed remain in a range of 20% for the internal definition, and under 10% for the external one for our built models.

Part C: EMC Filters

Switching converters produce high-frequency noise that is propagated on power lines and can affect other electronic equipment connected to the same network. This noise energy produced by the switching function of a power supply is predominant at the fundamental frequency and its harmonics (a few tens of kHz to 30 MHz). At these frequencies, the classical standards impose maximum levels not to be exceeded (150kHz to 30MHz). Filters are a crucial part of a converter preliminary design since they are a major contributor to total weight, and their design mainly results of constraints imposed by the standard to be respected. Thus, a good estimation differential and common mode models is required to check standard-compliance at an early stage of the design. We first recall the different types of EMI in embedded systems. Their standards and methods of measurement are then developed. Second, we propose methods to create equivalent sources to represent these interferences, and explain how to design filters to attenuate and isolate EMI, with an extension to the multilevel converters. To conclude, our models are compared with simulations and experimentations to validate our approach.

4.12. Perturbations, Standards and Measurement

4.12.1. Types of EMI in embedded systems

An EMC problem exists when a noisy system (the source) generates interferences that are transported via a coupling path towards a susceptible system (the victim). The different types of disturbance or noise source encountered in an embedded equipment for A/C (Aircraft) are (Figure 122):

- Conducted disturbances on power and signal lines, based on two principles (Figure 123):
- **Differential-mode**: perturbation in opposite ways,
- **Common-mode**: perturbation in parallel ways.
- Radiated disturbances
- Electromagnetic disturbances from lightning, HIRF (High Intensity Radiated Fields), internal radio-frequency sources and PEDs (Portable Electronic Devices)

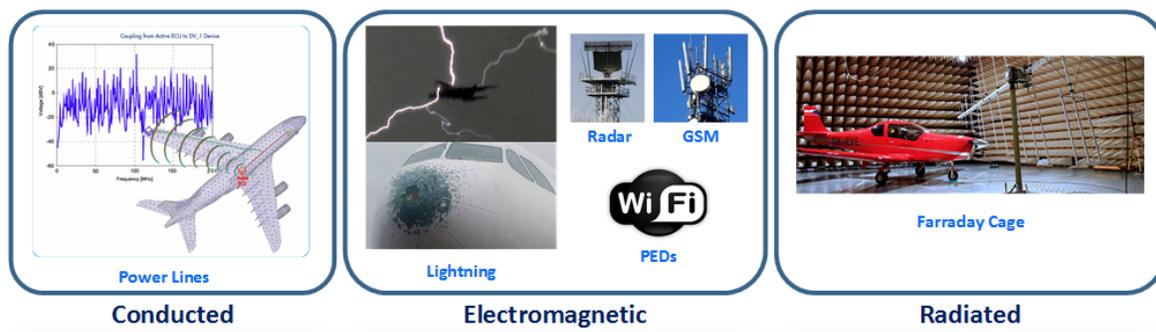


Figure 122: Synthesis of EMC perturbations in an A/C

In power electronics pre-design, only conducted disturbances under 30 MHz are considered, because they are the most stringent and predictable problems in static converters. Although models exist (SEISME project [162]), it is difficult to estimate the radiations because it is an empirical science that is specific to each design. Regarding lightning, external and generic devices are automatically added to protect the system, like serial switch or TVS (Transient Voltage Suppressor) that limit the lightning current. Therefore, it is not necessary to take them into account during the pre-design of a converter.

4.12.2. Conducted Disturbances in a Converter

Due to the high switching frequencies, conducted electromagnetic disturbances appear in the converter and are the most prominent disturbances to consider. They are classified in two classes, the differential and common modes (Figure 123) [163]. Often, detailed circuits containing numerous parasitic components representing imperfections and connections of components [164] [165], are used to represent the path between the victim and the source. However, in a pre-design scheme, it is impossible to consider this level of details. Thus, simple schematics must be used to estimate the magnitude of the perturbations, as well as paths and ways to filter them. Four main conducted perturbations are classified for the virtual prototyping (Figure 123):

- **Common Mode** - Input to Heatsink potential (1)
- **Common Mode** - Input to Output (2)
- Differential Mode – Inputs (3)
- Differential Mode – Outputs (4)

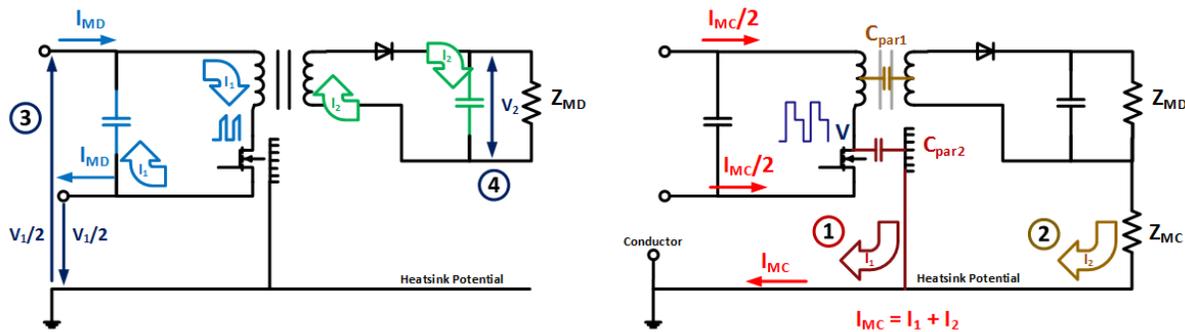


Figure 123: Localisation of the 4 main conducted EMI a) Differential mode – b) Common Mode

On the one hand, the differential mode is directly caused by the current and voltage waveforms (quasi-square) generated by the switching cell. On the other hand, the common mode noise is essentially due to the switching voltage associated to the parasitic capacitance between the midpoint of the switching cell (potential between the MOSFET and a diode for a buck-type) and the mechanical ground. These perturbations are due to the high dV/dT generated by the switches transitions. The main parasitic capacitance is of the one between the switching cell and the heatsink (Figure 124). It allows high frequency currents to flow through the entrance of the converter and the ground connector. The need to electrically isolate the devices from the heatsink, or even the

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equipment chassis, comes from three main reasons: **safety**, **reduction of electromagnetic interference** by reducing stray capacitance junction-to-ground and **the cooling of many devices** on the same heatsink frame. The normal method of isolation is to use an isolated material between the semiconductor device and the heatsink (4.13.4) (Figure 124-a). Another possible path to consider in an EMC pre-design study is the housing/shielding of the global power converter (Figure 124-b). Thus, an approximation of this conduction line can be approximated with arbitrary/empirical values in order to evaluate the impact of the converter shielding.

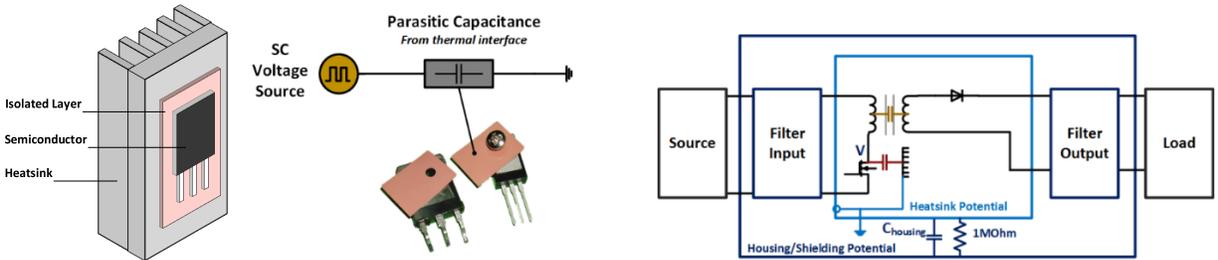


Figure 124: Schematic of the principle for the common mode perturbation and Simplified Housing/shielding electrical path in a power converter

4.12.3. Standards

To accept the conducted disturbances in an embedded equipment, different standards exist in the industry, in order to characterize the magnetic susceptibility levels (Figure 126). It is important to notice that the respect of these standards can generate highly functional improvements (Figure 125-a).

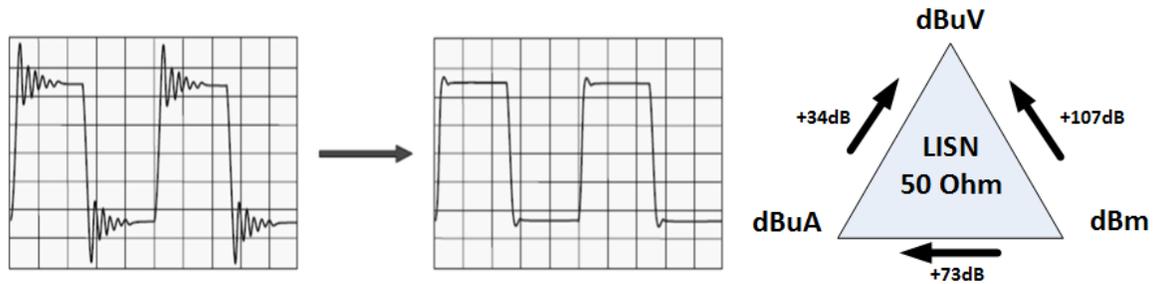


Figure 125: a) Functional improvement with the EMC filtering on power waveforms b) EMC triangle of conversion between common standards units

In our case, we only consider four standard documents. As a notice, the airbus standards are represented in Figure 126 because of industrial property. :

- RTCA/DO-160G (Figure 126, with the labels B and L explained hereafter) or EUROCAE/ED-14G
- Airbus HVDC directives, related to the new HVDC network in the MEA (270 or 540V).
- ABD100.1.2, (Airbus Directives), related to the EMC aspects up to 150kHz
- ABD100.1.8, (Airbus Directives), related to the Network aspects from 150kHz to 200 MHz

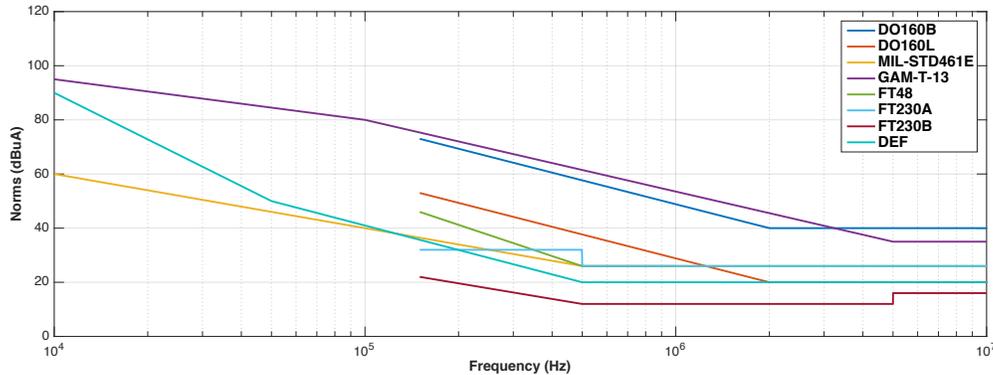


Figure 126: Example of EMC standards in the electrical industry

Because of the different units exposed by the previous standards, it is convenient to use the “conversion triangle” in EMC, in order to get a unique comparison basis (Figure 125-b). There are different categories of equipment, which are defined in terms of location and separation between the equipment and aircraft radio antennas. Different susceptibilities levels are allocated to these categories:

- **Category B:** equipment where interference should be controlled to tolerable levels.
- **Category L:** equipment in areas far from the aircraft apertures (such as windows) and far from the radio receiver’s antenna (in the electronic bay of an aircraft).
- **Category M:** equipment to which apertures are electro-magnetically significant and that is not directly in view of the radio receiver’s antenna (passenger cabin or cockpit)
- **Category H:** equipment located in areas that are in direct view of a radio receiver’s antenna (typically applicable for equipment located outside the aircraft).

In addition to these standards, practical design rules are commonly used at Airbus, for instance to ensure a security margin of 6dB on the conducted susceptibility (10dB for radiated). They are created to compare the theoretical design and avoid problems in practice. It is also known from experience, that previous standards are sometimes no longer adapted to current application in aircraft. This is the reason why some ongoing studies have been launched that aim at refreshing the susceptibility levels. Although frequency standards are a key point of the filters sizing, they are not the only ones (stability, overshoots or voltage collapse, settling time and inrush currents must also be considered (4.13.3.)).

4.12.4. Measurements

Usually, common-mode (CM) and differential mode (DM) currents are measured thanks to current probes and depend on the impedance of the line it is connected to. To avoid this dependence, standards are defined for a specific impedance which is realized thanks to a LISN (Line Impedance Stabilization Network). In aeronautics, measurements and comparisons of conducted electromagnetic emissions are carried out using a normalized LISN at 50 Ohms. In simulation, it can easily be replaced by a simpler circuit (Figure 127). The interference measured by the LISN

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have a common-mode and a differential-mode component but EMC standards define current disturbance limits for the sum of these two components, as it is difficult to separate their contributions. In [166], the authors propose a method to separate their measurements. The current simulation method is to perform two iterative simulations for each mode, in order to determine successively the different filters.

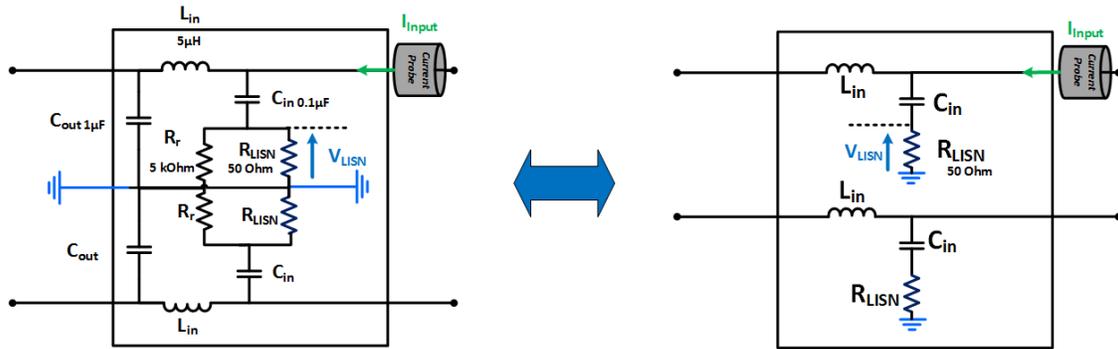


Figure 127: LISN circuit normalized @ 50 Ohm and its simplification for simulations

A LISN is a low-pass filter, typically placed between an AC or DC power source and the Equipment Under Test (EUT). It creates a known impedance and provides an RF noise measurement port (Figure 128). The values obtained are typically converted into dBμV, dBμA or dBm. It is good to know that in practice, we accept +/- 1 dB over the repeatability of EMC testing with LISN, depending on parasitic elements such as wiring, deviation setup tools or measurement accuracy. Thus, we should reach this precision in our simulation to get a pertinent sizing. To finish, the measurement can be made at two different locations around or inside the LISN, depending on the test specification and the equipment domain. For instance, aeronautic standards impose to measure the input current at the LISN bounds (Figure 127). At the opposite, other specifications impose measuring the current/voltage through/across the 50 Ohm resistor.

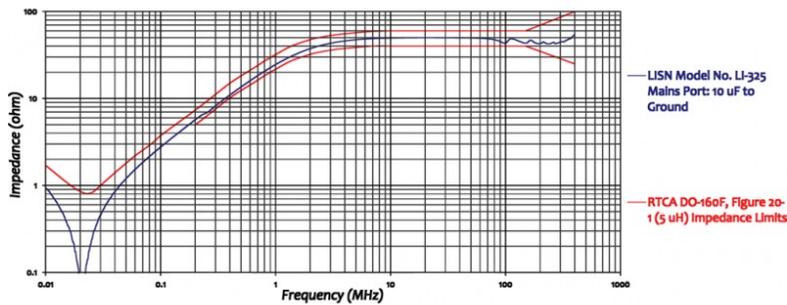


Figure 128: LISN circuit and its impedance normalized @ 50 Ohm

4.13. EMI and Filter Models

Due to the high switching frequencies, conducted electromagnetic disturbances appear in the converter. To protect the networks, EMC (electromagnetic compatibility) filters are required that comply with the harmonic standards defined in the industry. At Airbus, we estimated that 30-40% of the converter weight and volume is caused by filtering. Our purpose here is to establish a method to design them efficiently. Generally, designers think that increasing the frequency improves the converter compactness. Indeed, the passive components are smaller for a same ripple peak to peak. But, the standards become more constraining for higher frequencies, and increasing the frequency does not reduce automatically the filter size [167]. In addition, losses become higher and so a global thermal/EMC trade-off has to be found. Therefore, it is clear that we need an optimization to deduce the ideal compromise in regards with a specification.

4.13.1. Filter Topology

a. Topology Object

To automate this process, we propose to create a **topology object** composed of passive devices in our library (Figure 129), on which we add EMI sources and network/load/LISN objects. Different scenarios are available for the filter object of our library, depending on the converter configuration:

- Common-mode Filter, Differential-mode Filter or Both inside the same composite
- Location: Input/output, HV/LV, AC/DC, etc.
- Insulated Equipment or Chassis ground connections
- Specific Filter Order (second, fourth, etc.)
- Choice of technologies, shapes, material, constraints, etc.
- Standards to comply with (Figure 126)

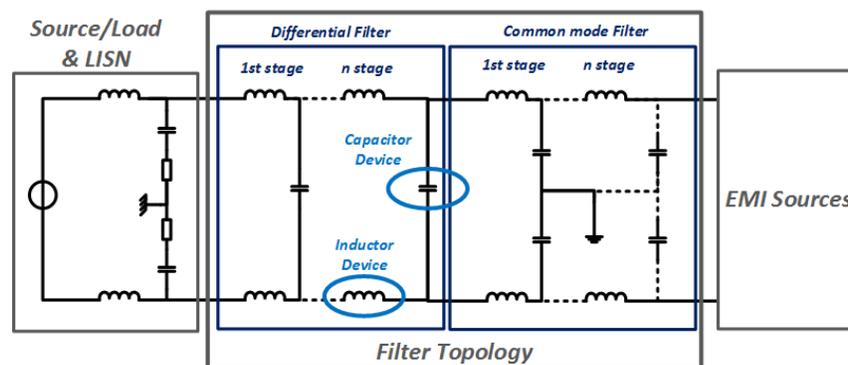


Figure 129: Schematic of Filter Topology Object Configuration

b. Principle of the topology

Numerous approaches exist for the filter design. The one proposed in this thesis is based on the different functions of the passive components:

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- Limit the impact of **the converter on the external world**, i.e. limit the current ripple on the HV side, and the voltage ripple on the LV side, based on the steady state analysis (I_{ripple}^{HV} , V_{ripple}^{LV}).
- Limit the impact of **the converter on itself**, i.e. limit the LV current ripple and the HV current ripple, based on the steady state analysis (I_{ripple}^{LV} , V_{ripple}^{HV}).
- Limit the impact of **the external world on the converter**, i.e. limit the HV and LV voltage variations induced by loads steps, based on the transient response (I_{dip}^{LV} , $V_{overshoot}^{HV}$).

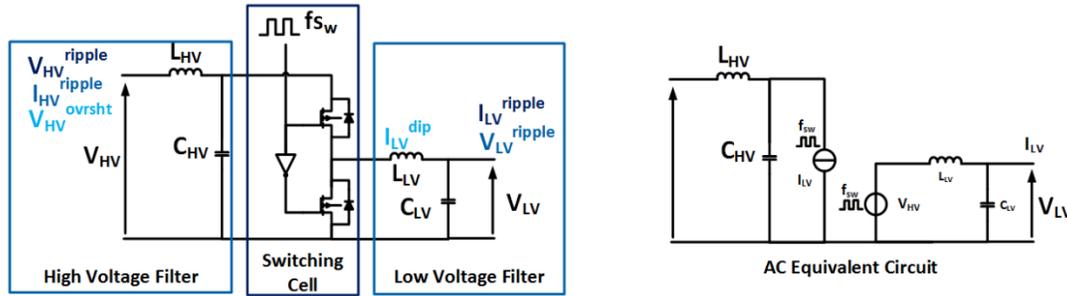


Figure 130: Sizing quantities in a power converter and its AC equivalent model in order to simulate them

These different aspects are represented in Figure 130 with its equivalent AC circuit, including the simplified perturbations sources that are developed in our next section. This equivalent circuit is used to assess the filter efficiency compared to the standards and specifications.

4.13.1. Perturbation source Models

The purpose of EMC modelling is to approach the spectrum of interference signals. Therefore, it is advisable to work directly in the frequency domain. The methods to simulate these sources have been proposed in the chapter 2 and 3 on a direct and indirect approach. As a reminder, we proposed:

- **Indirect frequency methods** using a time-domain solver coupled to FFT calculations.
- **Direct methods** with analytical equations or the direct frequency solver OOTEE.

Hereafter, we detail our direct simulation of these sources inside the frequency solver.

a. Direct Simulation

We have use “simplified” disturbance sources based on a linearization of the structure as already used in [165]. This “simplified” approach consists in replacing the switching cell by equivalent generators of square waveforms (Figure 130), to generate the differential and common mode currents. These elementary generators contain the necessary information about the power and switching to transcribe in a pre-design tool, allowing the sizing of a switching cell, and so a complete power converter. Indeed, this simplified degree of realism is sufficient to represent the phenomena that generate researched currents perturbations. The equivalent circuit of a buck and a 3-phase inverter are exposed in Figure 131. For the buck, the HV DM is generated by the current absorption of the network; therefore, it is naturally represented by a harmonic current generator. On the

opposite, the LV DM&CM are represented by an equivalent harmonic voltage generator, which pictures the switching cell behaviour. These sources finally replace the cell switching and the network power supply.

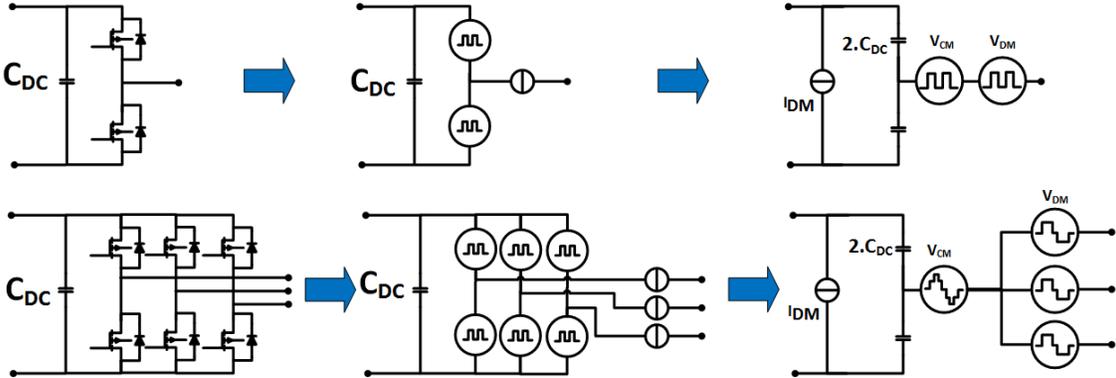


Figure 131: AC equivalent circuit for a single- 3-phases switching cells

For several years, a simplified approach has been used in EMC, which helps to understand phenomena. It is based on the **decomposition** of the different interference sources and propagation paths. The possible sources are divided into those of differential mode (current for HV/DC side and voltage sources for LV/AC side, for respectively Buck and Inverter topologies) and those of common mode (voltage sources) (Figure 132). This dissociation of effects in currents and voltages allows a phenomenon logical analysis, which is easier and faster. Though this method is entirely based on a "Source-Path-victim" approach, it requires a good knowledge of the power structure.

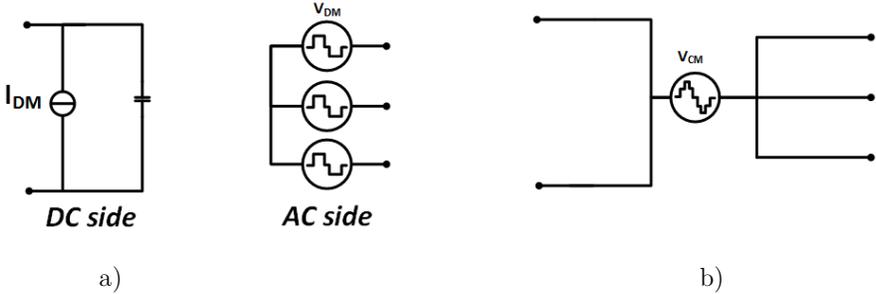


Figure 132: Dissociation of the different perturbation sources of the inverter from Figure 131 a) Differential Mode b) Common Mode

4.13.2. Source-Path-Victim Description

To describe the "Source-Path-victim" circuit, different methods are available. The easiest one is to create a node list, and then use an appropriate solver to simulate the electrical behaviour. It allows describing with precision and flexibility any different EMC models. In our case, we chose this solution with the direct frequency solver OOTEE (Chapter 2) that is developed in the next section (a). However, other quicker approaches are possible, as developed in several theses such as [164] [165] [168]. Although these methods are limited to assumptions and simplifications, and are unique

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on a specific topology, they can be very useful in the optimization processes. We can classify them in three types:

- Transfer Function
- Matrix approach
- State Representation

In our case, we used the models and propositions of the thesis [168] [164] [165] and contributed to this pure analytical method with a multilevel common mode model (Appendix).

a. Multi-level equivalent Circuit Approach

Some AC equivalent circuits for classical topologies (buck, inverter) have been presented in Figure 131 and Figure 132. They can be extended to multicell converters with any number of cells through a generic approach. A classical buck converter, with a 2-level serial interleaving is shown in Figure 133. It considers that the LV amplitude is divided by the number of serial level (N_{ser}), while the switching frequency is multiplied by this same coefficient (N_{ser}). The HV side is unchanged.

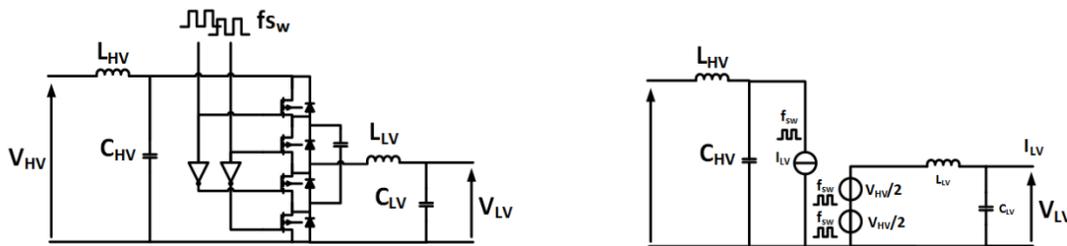


Figure 133: Series multicell buck converter, with its equivalent circuit

For a 2-level parallel interleaving (Figure 134), the amplitudes of the LV and HV sides are divided by N_{par} and their switching frequencies are multiplied by N_{par} .

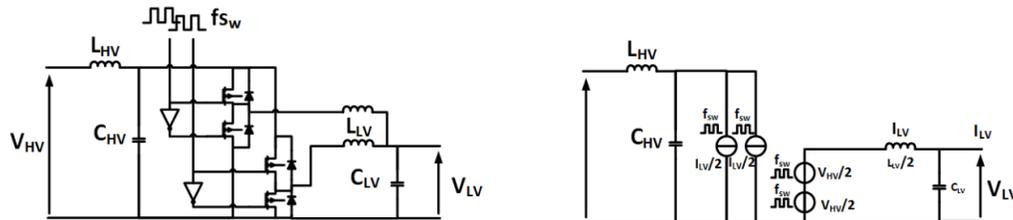


Figure 134: Parallel multicell buck converter, with its equivalent circuit

Finally, for a mix of serial/parallel interleaving, we obtained the Figure 135, which superposes the previous design rules to create an AC equivalent circuit of multilevel converters.

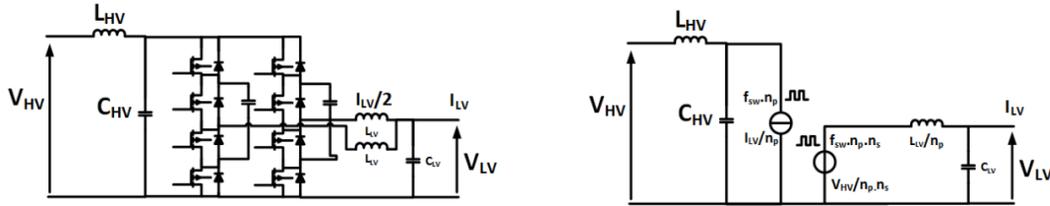


Figure 135: Series-parallel multicell buck converter, with its equivalent circuit

As already done in the previous example for the LV inductor, we can extend this “equivalent” method to the different passive components decoupling the switching cell before connecting filters. Thus, with this new stage of decoupling, we only need to connect a classical filter, without managing the multilevel aspect of the switching cell. Three configurations are possible for the DM:

- **Serial Current-sources:** The decoupling stage is composed of N serial capacitors. Thus, the equivalent capacitance is C/N . (Figure 137a)

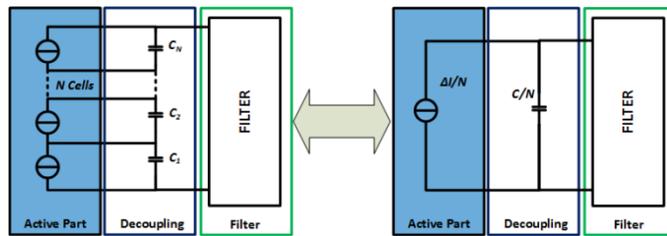


Figure 136: Equivalent Multicellular topology in a Serial Configuration

- **Parallel Voltage-sources:** The decoupling stage is composed of N parallel inductors. Thus, the equivalent inductance is L/N . (Figure 137b)

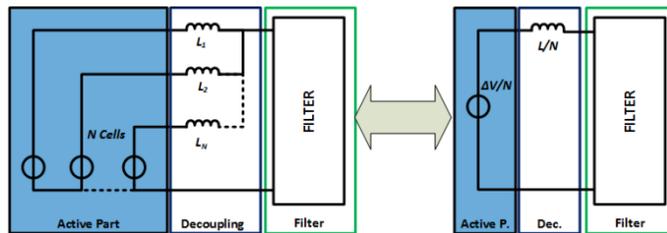


Figure 137: Equivalent Multicellular topology in a Parallel Configuration

- **Mixed interleaving:** It is the combination of both previous points.

Regarding the common mode, we use the same voltage source definition as the one on the LV side. However, we add the electrical common path, linked to the ground by a parasitic impedance (Figure 138). We assume that passive devices for the common mode have no effect in the differential filter model. On the contrary, we include differential mode components in our common-mode simulation.

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Thus, we obtain differential and common mode filter circuits easily for any multilevel converter disposition. It should be noted that we can easily simplify the common mode circuit, by only considering one branch of the perturbation with a hypothesis of symmetry and balanced currents. Thus, the filter study is simplified with less devices to study, which accelerates our simulations and optimizations.

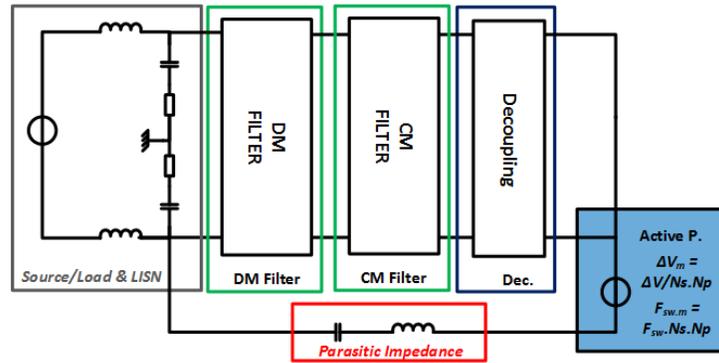


Figure 138: Equivalent Multicellular common mode AC circuit

b. Transfer Function Approach

In Appendix, a transfer Function approach is proposed to treat the Multilevel-converters analytically

c. Resolution

Different methods exist to verify if the filter design is compliant with a standard. A current simplification is to only consider the first harmonic calculation, which is in most cases the greatest. The assumption is that if the first harmonic is compliant, the rest of the spectrum is compliant too. In [3], the author explains this method according to the slope of the standard to comply with: in some cases, if the slope is too steep, we should not assess the first harmonic but a specific point called the 'salient point'. In our case, the method to perform the filter optimization is simpler. It is directly based on the vector computation and comparison with the standard, which is very efficient using current engineering tools like Matlab.

Figure 139 illustrates the different steps:

- 1) Computation of the EMC perturbation from a direct or indirect frequency method, in order to get a vector containing the amplitudes of this disturbance.
- 2) Interpolation of the disturbance vector and standard as a function of the frequency, in order to calculate the difference of magnitude. Then, we select the maximal value in this vector.
- 3) If this maximum is negative, the filter is compliant. If not, we try a new design of the filter.

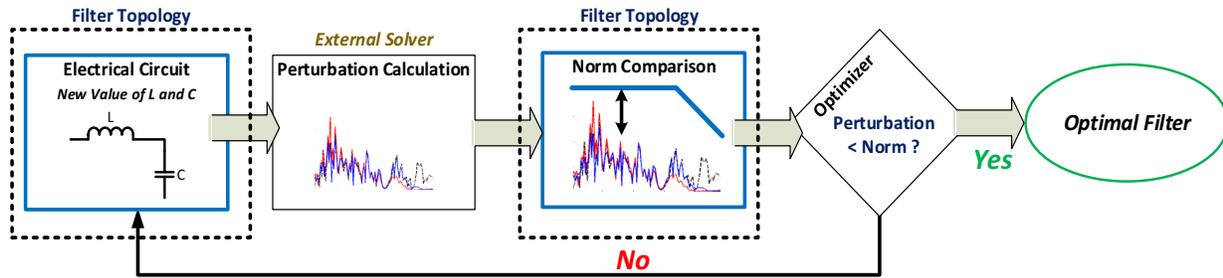


Figure 139: Principle of the filtering sizing steps

This resolution method includes others mechanism that avoid common filter design problems during the computation (e.g. under formalism of options and/or constraints in the optimization scheme), such as:

- Choosing the adequate filter topology
- Selecting the inductance and capacitance values to verify that the cut-off frequency $f_0 < f_{sw}$ the switching frequency
- Verifying the magnetic saturation
- Limiting the leakage inductances in the magnetic components, if required
- Adding a margin to take into account the dispersion of components (ESR)

4.13.3. Temporal consideration

As introduced before, the EMC frequency considerations are a key point of filter design, but they are not the only ones. Other criteria are also important for the dips design, such as stability, voltage overshoot and dips in presence of load steps, settling time and inrush current during the charge and discharge of filters. As an example, the work in [169] uses optimization algorithms to reduce the energy stored in the passive elements by combining the stability criteria, the filtering and the damping. In our case, we can perform simulations during or after the optimization loops to validate these criteria, or we can directly put constraints on the values of the electric filter with these two simple hypotheses [170]:

- When voltage is passing from a full load to an empty load, the faster response of the topology is obtained by imposing a zero-duty cycle. Thus, the inductor current charges the capacitor. The voltage overshoot is given by an equation that allows us to finally limit the overshoot on the high voltage during our optimizations (114).
- When the power of the circuit is turned on, an inrush current occurs to charge the capacitors. This inrush current must be limited. For the low-voltage filter, the network inductor helps to limit the inrush current (or is saturated if too much current, it is why the maximum inrush is specified in standards) but imposes a limitation on the capacitance. For the high-voltage filter, the filter inductance limits the inrush current. Another method is to limit the use of a pre-load resistor [171]. It allows limiting the voltage dip on the low voltage side (115).

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$$V_{overshoot} < \sqrt{\frac{L}{C}} \cdot I_{max} \quad (114)$$

$$I_{dip} < \sqrt{\frac{C}{L}} \cdot V \sqrt{n_p} \quad (115)$$

A common representation used in the laboratory expresses this principle limiting the possible values of L and C (Figure 140).

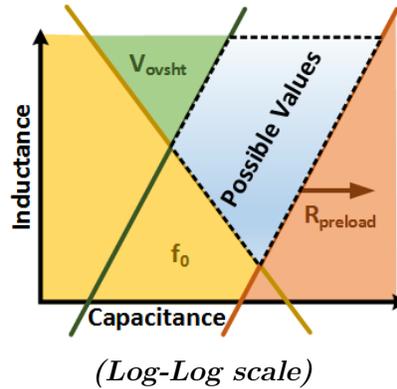


Figure 140: Satisfying values of capacitance and inductance in a LC filter

4.13.4. Parasitic capacitance Model

a. Physical origin of the parasitic capacitance

The common-mode model considers a parasitic impedance between the semiconductors and the heatsink potential, which has to be electrically isolated for different reasons (4.12.2). This isolation is often realized in our application with a thermal interface like a Sil-Pad (Figure 124). Sil-Pads are thermally conductive insulators. They are a cleaner, cheaper, more durable and efficient alternative to mica or ceramics and present excellent thermal performance. Nowadays, an alternative exists with semiconductor packages that directly embed this isolation (Figure 141) (Chapter 3). Thus, it is interesting to know how to evaluate the parasitic impedance of these isolators. Numerous analytical equations exist to approximate these values, with more or less accuracy, configurations and hypothesis. But in the pre-design phase, we prefer to fix a worst case arbitrary value of the parasitic capacitance of a power module, often estimated between 1e-9 and 1e-12F. Therefore, we need to measure and validate these values on real power modules.

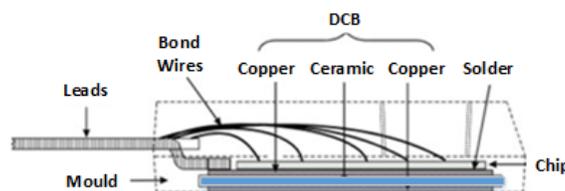


Figure 141: Example of an isolated discrete packaging of semiconductor: ISOPLUS 247 cross-section

b. Parasitic Capacitor measurement

In order to design the best filtering devices to meet the standards, it is necessary to characterize the elements generating noise. In our case, it is the measurement of the parasitic capacitance C_{mc} , present in our switching cell model. We determine it by measuring the intrinsic capacitance of the power module between the midpoint and the ground (mechanical mass / radiator). The common mode impedance measurements are made between the midpoint of a bridge and the base of the module on these IGBT samples: *SEMIKRON SK25GD065ET*, *EUPEC FS50R12KT3* and *MICROSEMI APTGT150A120TG*. These measures allow us to get an order of magnitude of the common mode impedance value of different power modules voltages and power (Figure 143).

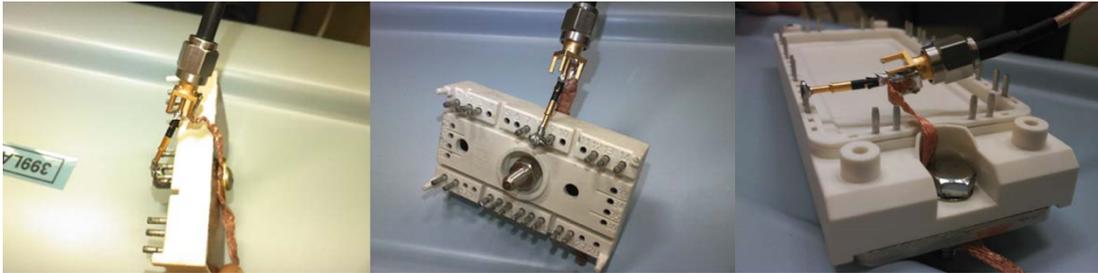


Figure 142: Photograph of the tested IGBT modules

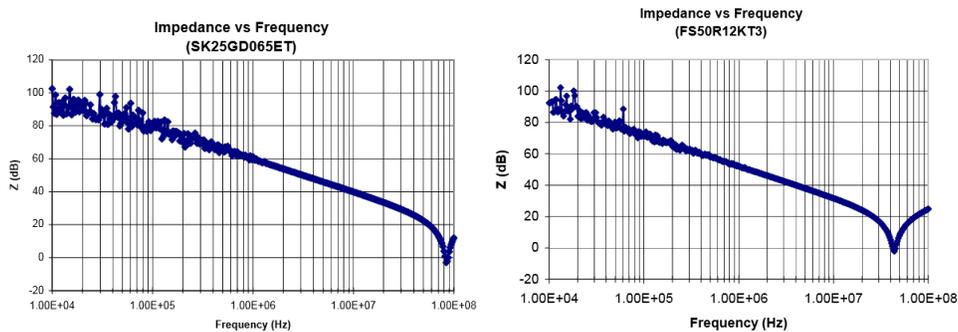


Figure 143: Impedance measure on power modules

The impedance acts as a plan capacity for a maximum frequency of 50MHz. Up to this frequency, an inductive effect appears. From the experience, it is certainly due to the parasitic elements of the measurement setup. We can easily deduce the value of C which equals to the following equation (for the SK25GD065ET module) (116):

$$Z = \frac{1}{jC\omega} \rightarrow C = \frac{1}{jZ\omega} = \frac{1}{98.1 \times 2\pi \times 10 \times 10^6} = 162.2 \text{ pF} \quad (116)$$

Final results are exposed in Table 19. Because housing sizes are very different between a 600V IGBT and a 1200V IGBT, we find that the parasitic capacitance is much higher for a 1200V IGBT. The facing surfaces are also larger. Given the impedance curves, we see that the behaviour of the impedance is purely capacitive up to 30 MHz (or 50 MHz). We can therefore use a 'simple' capacitance to model our source of disturbance (Max simulation of 30MHz frequency, as per Max

Filters

DO160 standard). In the case where a high frequency modelling should be carried out ($> 30\text{MHz}$), a series RLC model should replace the 'simple' capacity, but we suspect that is the consequence of the measurement set up and that normally this parasitic capacitance must to be “perfect”.

<i>References</i>	<i>Manufacturer</i>	<i>Features</i>	<i>Cmc</i>	<i>Frequency Validity</i>
<i>SK25GD065ET</i>	<i>Semikron</i>	<i>600V / 30A L x I(*) : 55mm x 31mm</i>	<i>162 pF</i>	<i>50 MHz</i>
<i>FS50R12KT3</i>	<i>Eupec</i>	<i>1200V / 50A L x I(*) : 100mm x 45mm</i>	<i>385 pF</i>	<i>30 MHz</i>
<i>APTGT150A120TG</i>	<i>Microsemi</i>	<i>1200V / 150A L x I(*) : 93mm x 41mm</i>	<i>419 pF</i>	<i>30 MHz</i>

Table 19: Impedance values corresponding to the circuit of Figure 177

4.13.5. Validation

Because the differential-mode in EMC has been well mastered for decades in power electronics, no specific validations of models are required for our methodology and models. Only their integration in our platform was verified. Indeed, the majority of literature references proposed in this part, have already validate differential-mode models. Nevertheless, the common-mode models are rarely investigated or taken into account to size the filter of static converters. Although their principle is studied in some cases, a validation is expected to be sure of our hypothesis.

a. Comparison with SABER

Firstly, we compared a classical inverter topology comprising a LC input filter SABER simulation with our methodology using the frequency solver OOTEE and simplified sources. We tested to get the current common-mode measurement at two different locations: at the input of the LISN and at the 50-ohm resistance of the LISN. As a notice, the OOTEE solver provide only relevant results for the odd harmonics, contrary to SABER. We can also see that the OOTEE solver provides close results in a shorter time than the SABER solver (seconds for the OOTEE rather than tens of seconds/minutes for SABER), so it is more suitable for the optimal sizing of filters. However, it exists a difference of results (e.g. $\approx 10\text{dB}$ @ 5,9,11th harmonics), that can be partially explained by the fact that the trapezoidal shapes used to represent the common mode perturbations in both solvers are not exactly similar (the Saber simulation uses an almost trapezoidal shape, slightly rounded). Thus, the conclusion here, is that exists a difference of results with a traditional solver (SABER) and our new simplified frequency solver (OOTEE), but they both provide a same global order of magnitude for the majority of the odd harmonics.

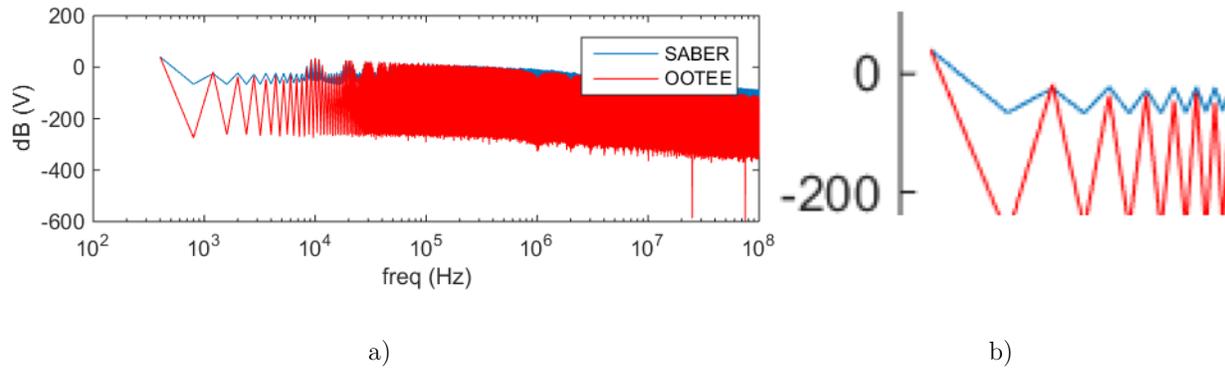


Figure 144: a) EMC comparisons between SABER and OOTEE simulations at the input of an inverter
 b) Zoom on the first harmonics of a)

b. Comparison on a real inverter measurement

An experimental prototype was made at Airbus and Laplace a few years ago in a previous research thesis [172]. It was dedicated to the measurement of conducted emissions of an aeronautical inverter. Its aim was to comply the power lines with the DO160 standard, and to compare several strategies of filtering. We reuse the results of this experience to validate our own common-mode model. Different configurations of filtering have been tested, based on a single 10kW inverter module, using a carrier-based modulation. Incremental elements proposing different configurations, and acting on the common mode circuit were added as shown in Figure 145. More details are in the thesis [172]:

- 1) Common mode capacitors (4x150nF) operating @ 15.6 kHz with a 30A peak level
- 2) 1) + Common mode inductance (13mH) with LC filter cut-off frequency @ 1800Hz
- 3) 1) + 2) + filter input and output inductors with two different common modes.

The impedances of all components have been characterized and inserted in our frequency simulation model. The envelope of the experimental spectrum has been fitted to ease the final comparison with Matlab simulations, as shown in Figure 146.

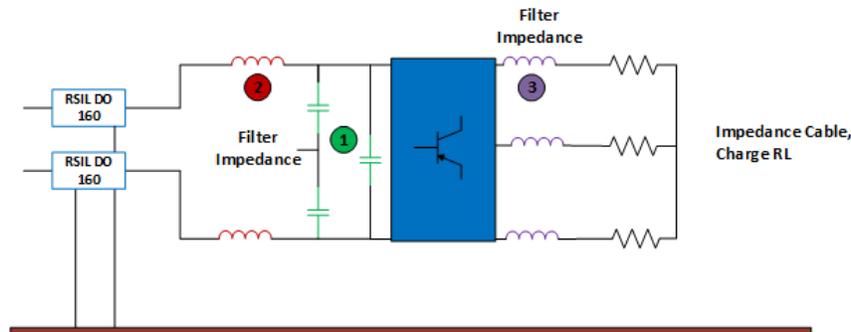


Figure 145: Different configuration tested on the 10kW inverter prototype
 Input $L_{mc} = 13\text{mH}$ - Output $L_{mc} = 8.5\text{mH}$ - Load + Cable = 5 m

Filters

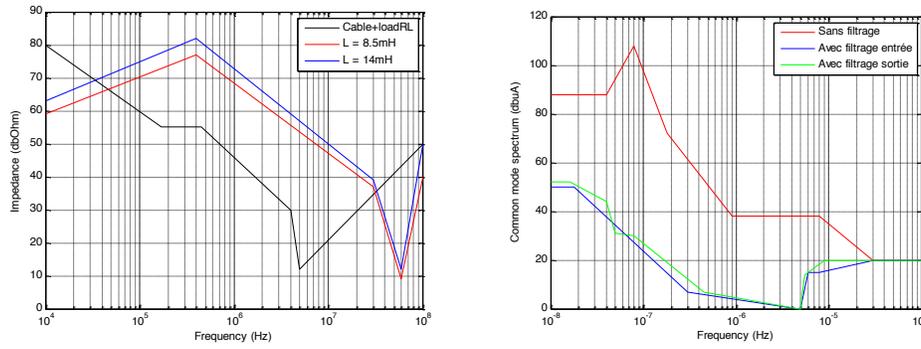
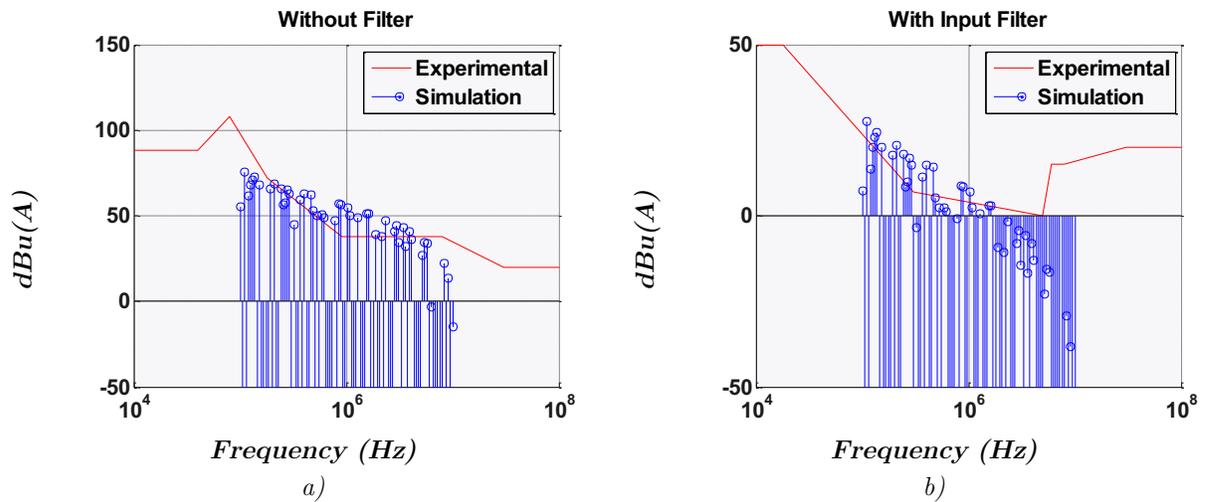


Figure 146: Fitted envelopes from thesis results [172]

a) Impedances of the different elements of the prototype b) Experimental measurements

Finally, we can now compare our common-mode models to that experience from thesis [172] (Figure 147). The experimental curves are the envelop of the real frequency results, under a continuous representation of the different harmonics to better show the results with our own simulations. The results are close to experimental results and can prove the validity of our common-mode hypothesis, particularly in the context of optimal pre-design and virtual prototyping. The difference can be explained by the fact that is a comparison between experimental and simulation data, but also by the fact that it is approximated data extracted from a paper thesis for the experimental part. In addition, we do not know all the configuration of the experience.



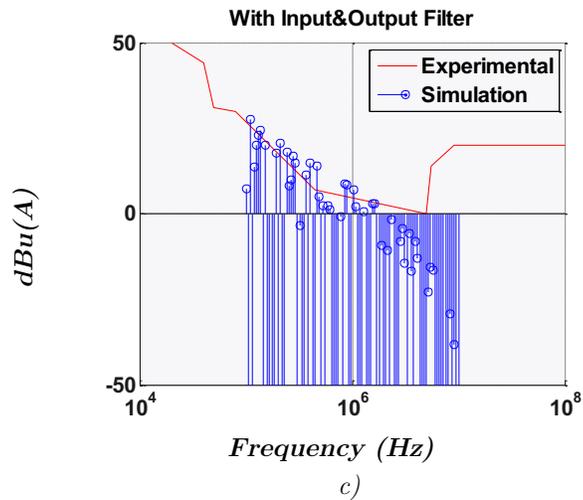


Figure 147: Comparison between simulation and experimentation: spectrum of common mode current as a function of the frequency @ the LISN

a) Without Filter – b) With Input Filter – c) With output Filter

4.14. Conclusion

First, a reminder on the EMC phenomena in embedded systems has been proposed, including the frequency standards and measurements that characterize them. Then, sources and models have been proposed to allow optimization-based design of the differential and common mode filters. Finally, because the differential mode modelling is well mastered, validation via experimental measurement and simulation have been proposed for the common-mode model. For the moment, they are not totally convincing in this state, because relevant difference exists during our validations, mainly because of our simplifications and the use of the frequency solver OOTEE. However, our proposition provides a magnitude of results complying with a pre-design work, and so can be used as a first proposition in our virtual platform even if this part requires to be improved in order to better simulate the EMC problematics in a power converter. In addition, an evaluation of the parasitic capacitances within our power modules has been realized. Thus, a good correlation between models and real phenomena has been obtained in spite of the simplicity of the models. This work finally enables to properly design the filter in a pre-design context.

Chapter 5

5. Optimizations Examples of power devices, topologies and converters

The purpose of this chapter is to present a list of pre-design applications in power electronics. This list is non-exhaustive and has been computed thanks to the multi-physics models presented in this thesis. The objective of this work is to demonstrate the potential and assets of our computer-aided approach, but also to identify its limits and possible improvements.

The pre-design is organized in three optimization levels, as stated in Chapter 2 for our platform and GUI (Graphical User Interface). Each of these levels is illustrated by examples, which have been chosen to show the different kinds of studies available. The three optimization levels are:

- Single Device Optimization
- Topology Optimization
- Converter Optimization

For the **Single Device Optimizations**, a custom straight-fin heatsink has been chosen to demonstrate how to optimize a single device. This heatsink optimization is a main challenge to design the active part of a converter. The pre-design is achieved in two different studies, by considering the natural convection and the air-forced convection.

The **Topology level** deals with the optimizations of the assembly of some basic devices, as defined in Chapter 2. Topologies are divided in two distinct families, in order to build a whole converter. They either contain the active topologies as defined in Chapter 3 (semiconductors + cooling devices), or the passive topologies i.e. the Filters as stated in Chapter 4 (Magnetics and Capacitors). We present examples for both cases:

- **Passive Topology**

An example of a topology pre-design is proposed for the assembly of passive devices through a filter application. This filter is applied to a classical chopper conversion and designed according to the aeronautic standards. It demonstrates the simultaneous optimization of passive components (a capacitor and inductors that form a classical LC filter), while respecting the EMC and thermal considerations defined by the system specification.

- **Active Topology**

Two examples of active topology optimizations have been chosen; they focus on two DC-DC applications.

- The first example compares different isolated topologies, in order to find the most efficient and lightest DC-DC conversion for a 400W specification. A low granularity is used to define the multi-physic models in order to accelerate and improve the convergence of the optimizations, but also to demonstrate how trade-offs can be quickly made in a pre-design scheme. This method allows taking high level decisions rapidly and with a limited precision of results. The objective here is to identify major trends, not to get a detailed design of the devices, as it can be reached with a higher granularity (Chapter 2).
- The second example deals with the optimization of the Buck Boost Converter Unit (BBCU), an isolated and bidirectional 12kW converter. It includes the modelling work of continuous and analytical solvers of very different topologies, and takes into account a multi-level and continuous description of the BBCU architecture.

The final level concerns the **Converter Optimizations**, that is the gathering of the active and passive **topologies**. No results on this level have been reached at the end of this thesis. It seems that the results obtained from each individual topology are not mature enough to ensure robust optimization of a whole converter. The scripts and models to launch a converter optimization are available, but the relevance of the result cannot be guaranteed. Therefore, this part will only be introduced in the conclusion of this chapter, as part of future work and perspectives.

***Notice:** In this chapter unless specified different, the following options are used:*

- *highest level of modelling,*
- *bounds and initialization of each optimization parameter as defined in the Comp3d library.*

5.1. Optimizations of a Single Device

5.1.1. Straight-fin Heatsink in Natural Convection

In this first example, we consider the optimization of a straight-fin heatsink. The purpose is to evaluate the evolution of its weight in natural convection as a function of the losses to evacuate.

The optimization problem can be summed in these different points.

- Function objective: Weight
- Constraints:
 - ΔT_{\max} (between the heatsink and ambient), this difference of temperature is a common limitation in a pneumatic network applied to embedded systems (Chapter 3 – Part B).
 - Technological consideration to create an industrial heatsink (thickness of the fins/baseplate for instance)
- Fixed parameters: Width and Length of the base plate, in order to fit a power board

Optimizations Examples of power devices, topologies and converters

- Degrees of Freedom: Fins (Length, width, number, air gap (Chapter 3))
- Parametric study: Material, Power to dissipate, Length and width of the base plate, different function objectives etc.

This evaluation has been realized thanks to sensitivity analyses, in order to see the dependency and impact of different parameters on the final weight. Different set-ups have been tested by applying small modifications on the heatsink initial specification and parameters, in order to establish relevant comparisons and deduce the best way to improve the heatsink design, such as the materials, maximal temperature acceptance, objective or the initial imposed geometry. The basic specification of the device is presented in Table 20.

Equivalent parameter	Physical Equations
Losses	5-30 W
Material	Aluminum
Width	30cm
Length	20 cm
ΔT_{\max} (between the heatsink and ambient)	55°C

Table 20: Main specifications of the Natural Convection Heatsink

Once the optimizations have been computed for the different set-ups and operation points, the curves of Figure 148 have been obtained. For information, roughly four hours of computation have been required to get these four figures, once everything had been well instantiated and parameterized. This kind of device optimization is the first brick of our software platform, as it is purely analytical and does not use external solvers. Thus, it is a good basis to illustrate the minimum computation time that is required today to perform pre-design studies in on a single object.

Finally, these figures (Figure 148) allow to assess the impact of changing the parameters compared to the initial specification, and evaluate which parameter is the most interesting to improve. As examples:

- The bigger the losses are, the heavier the optimized device is
- Aluminium is the lighter material
- The lower the allowed temperature delta is, i.e. the more constrained by losses and the heavier the device is
- To reach a difference of temperature of 60°C on the system rather than 55°C (@ 20W of power dissipation), the weight increases of almost 1kg.

We can also point to some doubts about the final results of our methods:

- The initial surface of the baseplate, imposed by the specification (Table 20), implies clearly an oversizing for low power (5 and 10 W). We can see that the difference of weight is very

small at these powers, almost equal. That maybe indicates that the computation has reached the minimal bounds of the optimization parameters during the optimal sizing of the heatsink.

- Weight and Volume objectives provide different solutions (Figure 148-c). Indeed, the “volume” objective consider the external volume of the device. On the contrary, the weight considers the exact volume of the device (i.e. by excluding the air-gap between fins).
- The variation of the base plate surface (Figure 148-d) provide “non-linear” results, that maybe points on a problem or difficulties of convergence during the optimization.

Other similar results and questions can be deduced by analysing the curves. As a conclusion, this kind of information is valuable for achieving high level system trade-offs, provide figures that are easily understandable and sharable, and take design decisions. However, remaining questions are still unresolved at this step, that should require more additional work on post-treatment functions to better analyze the results.

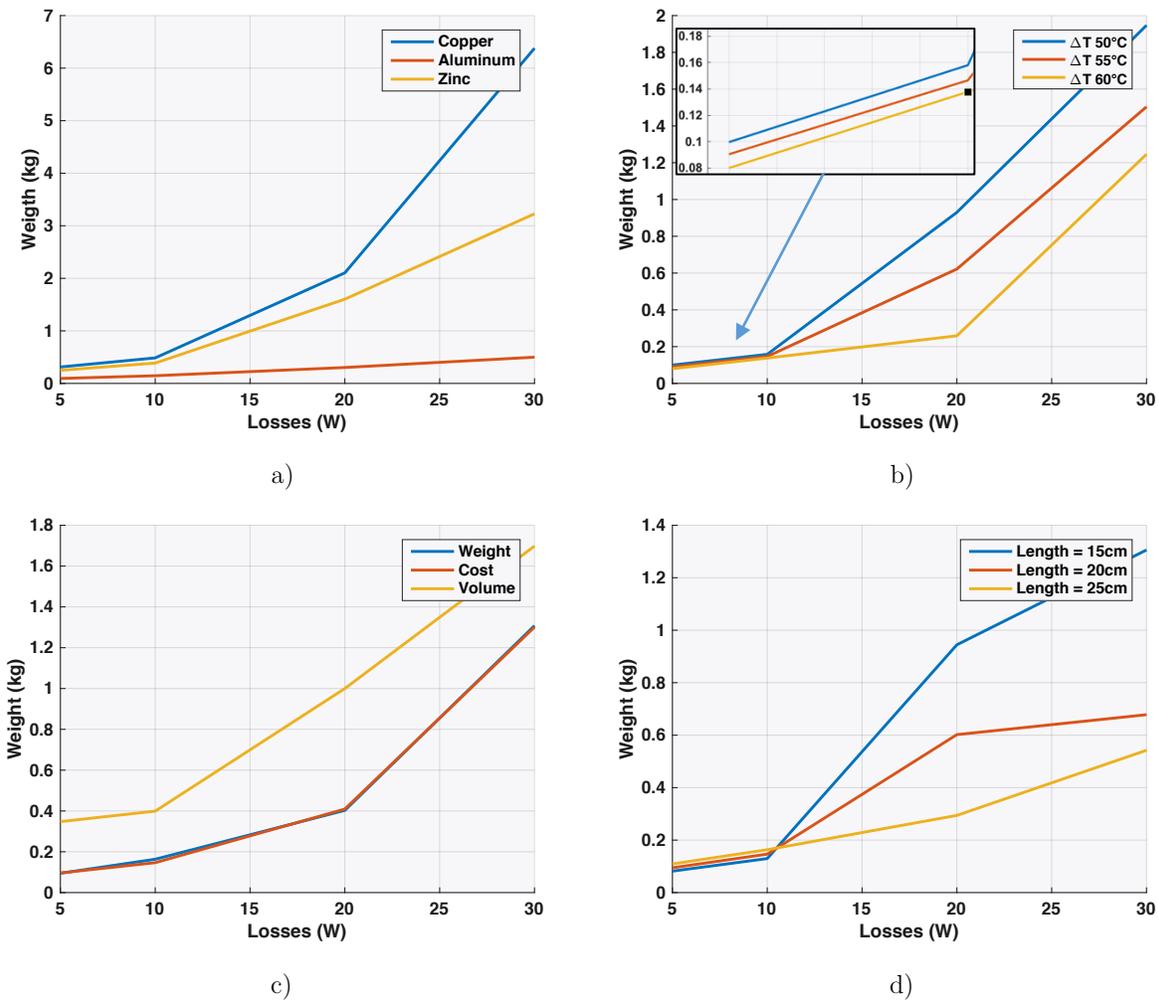


Figure 148: Evolution of the weight of a natural convection heatsink vs losses for different parameters
 a) Material b) Difference of Temperature c) Objectives d) Geometry

5.1.2. Straight-fin Heatsink in Air-Forced Convection

A similar study has been conducted for another straight-fin heatsink in air-forced convection. Here, new models and phenomena have been observed, that must be considered in our trade-off, like the pressure drop, the air flow and the difference of temperature between the inlet and the outlet of the heatsink. Indeed, the aeronautical context implies a set up for the cooling system: presence of an air stream, including an imposed air flow and limited pressure drop. As a result, there is no bypass around the heatsink, all the air from the air system (a blower for instance) passes through the heatsink, since the delta of pressure is calculated from the heatsink geometry (Figure 149).



Figure 149: a) The chosen heatsink geometry and air-flow configuration - b) another common example of configuration which is not used in our study

The optimization problem can be summed in these different points.

- Function objective: Weight
- Constraints:
 - ΔT_{\max} (between the heatsink and ambient), this difference of temperature is a common limitation in a pneumatic network applied to embedded systems (Chapter 3 – Part B).
 - Speed of the forced air flow (g/sec)
 - Difference between the Input/output temperature of the air flow ($^{\circ}\text{C}$)
 - Maximal delta of pressure (Pa)
 - Technological consideration to create an industrial heatsink (thickness of the fins/baseplate for instance)
- Fixed parameters: Width and Length of the base plate, in order to fit a power board
- Degrees of Freedom: Fins (Length, width, number, air gap (Chapter 3))
- Parametric study: Material, Power to dissipate, ΔT_{\max} , Length and width of the base plate, air speed, pressure drop, different function objectives etc.

Parameters	Values
Material	Aluminum
Losses	200-1200 W
Width	30cm
Length	30 cm
Air Flow (Imposed forced air flow)	55 g/sec
ΔT_{\max} (between the heatsink and ambient)	55°C
ΔP_{\max}	600 Pa
T_{inlet} (Incoming air temperature)	65°C
T_{outlet} (Outgoing air temperature)	85°C

Table 21: Specification of the Air-Forced Convection Heatsink

The results of the sensitivity analysis are presented in Figure 150. Some of the conclusions deduced are:

- the bigger the losses, the heavier the optimized device,
- aluminium is the lighter material
- the lower the allowed difference of temperature delta, the heavier the device
- a variation of the heatsink length has a bigger impact on the final weight than the variation of its width; the temperature constraint has more impact on the final weight than the pressure drop
- the air flow has little influence; it maybe indicates an over-sizing of this quantity.

Other similar results can be deduced very easily by analysing direct reading of the curves.

Optimizations Examples of power devices, topologies and converters

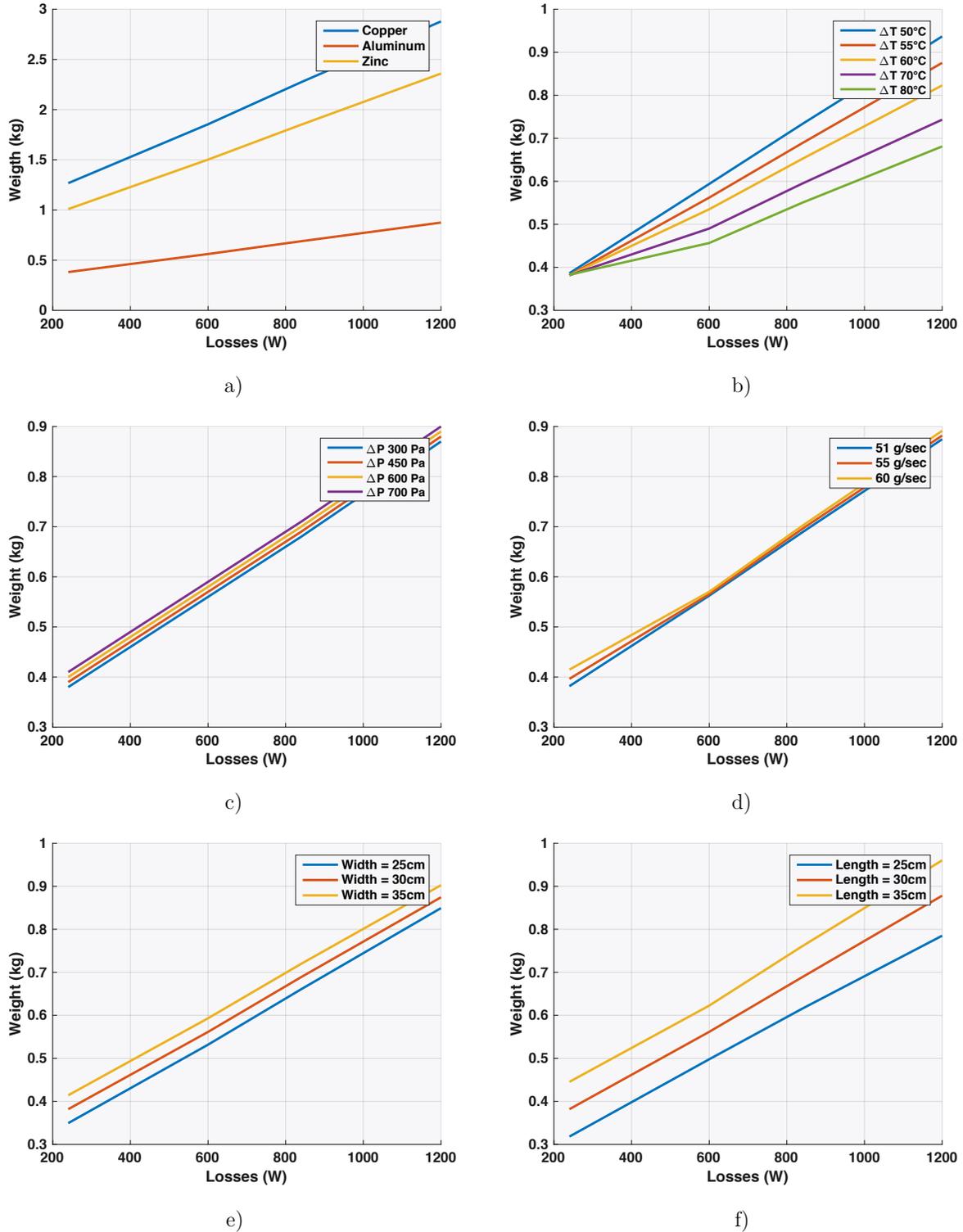


Figure 150: Evolution of the heatsink weight as a function of several parameters for an air-forced convection
 4 points in abscissa (250, 600, 850, 1200W)

a) Material b) Delta of Temperature c) Pressure Drop d) Air Flow e) Width f) Length

Following these two demonstrations on heatsinks, we can conclude on the optimization of single devices.

First, it is easy to get relevant and global optimums on single-device problems by using the traditional optimization algorithms such as the gradient descent (here with Multi-Starts (MS)). Indeed, they are well defined, use few variables, and are most of the time under a perfect continuous and analytical formalism, which allows a good convergence of the optimizer. Thus, getting the results on a single operation point is quick (some minutes without MS). Moreover, they propose very robust solutions when coupled with an advanced algorithm such as the MS or the GS (Global search) (Chapter 2). The MS & GS solutions have been favoured in our case. In addition, this conclusion can be extended to the other types of individual devices that we have in our library (magnetics, semiconductors, capacitors...) because they have the same properties and models as the heatsink.

Second, some efficient options are available to realize more advanced optimization studies, such as the multi-objective studies & Pareto fronts, or the sensitivity studies that have been presented in this section. Indeed, very interesting to get these graphical and automated curves, that can be finally analysed and contribute to design trade-offs. They allow to get the technological tendency in our equipment and systems, and help engineers to take design decisions. Moreover, this simulation remains quick (roughly 1 hour to get a relevant figure in our examples).

Finally, these tools have been used for a few industrial projects at Airbus, to give pre-design information, to design individual devices and to create system specifications. These optimizations have been validated thanks to FEM, and their results have been compared to other existing studies to ensure their accuracy. It shows that the industry is ready to accept this kind of study - at least in a Research & Development phase - and that we are encouraged to continue such a development (complete the libraries of models and their accuracy, develop the solvers etc.) and the one of computer-aided platforms.

However, at this step, it is important to note that is impossible for us to completely ensure that the final results are perfect, have reached a real global optimum, or have not suffered of recurrent problematics of convergence/calculation with our models or algorithms during the optimization. More real projects and studies are needed to be entirely confident with our optimization platform.

5.2. Optimizations of Topologies

5.2.1. Optimizations of a Differential Filter

Topology

The optimization of topologies is the second level of studies available in our computer-aided platform, where the first level concerned individual devices. Our first demonstration to optimize topologies thanks our tools is based on a passive topology, and more precisely on a differential LC

filter (2nd order). This filter includes basic capacitor and inductor objects, similarly to the single devices optimized in the previous section. It is connected to a classical chopper topology on its high voltage side. As shown in Figure 151, this side contains a HVDC Bus of 540V and a LISN (Line Impedance Stabilization Network). On the low voltage side of the chopper, the output load is a pure resistive impedance.

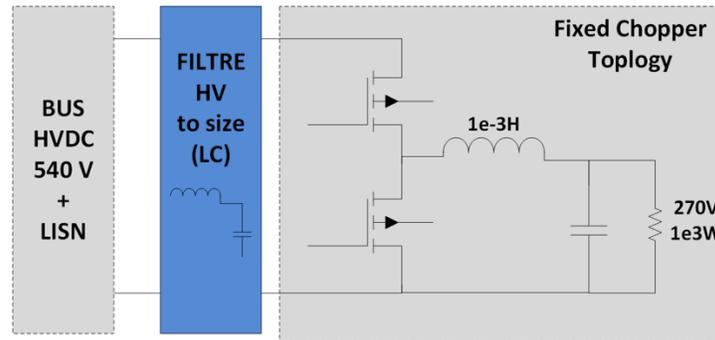


Figure 151: Schematic for the HV differential filter of a classical chopper topology

In order to design the filter, the EMC standards have to be defined. Here, the Airbus HVDC directives have been chosen. The global tendency of this standard level is introduced in Figure 153, and the main parameters of the chopper and filter are presented in Table 22.

Parameters	Values
EMC standard	HVDC Directive Airbus
Chopper	540V to 270V
Filter	LC – 2nd order
Power	1 kW

Table 22: Main parameters of the Filter and Chopper Specification

In a filter optimization, several analyses are possible to estimate the performance of the passive topology. These analyses mainly focus on the restrictions imposed by the system (through its specifications and EMC standards) and on the converter and filter topologies chosen. Thus, three axes will be developed for the sensitivity analysis (i.e. to vary each parameter to evaluate its own impact on the final objective), in order to test and estimate different design scenarios and allow to get the maximum information during the design process:

- the power of the converter,
- the EMC susceptibility level,
- the interleaving of the multi-level chopper topology; we consider that the simple topology described in Figure 151 can be replaced by a multi-level converter.

Other cases have been studied; they are also available in the software platform. However, it was not possible to present all of them in this memoir, such as:

- choice of material, technology, shape of the inductors and capacitors,
- order and topology of the filter,
- choice of converter topology,
- choice of the EMC standards,
- choice of objectives (mono, multi) and constraints (such as the thermal ones, e.g. the maximum elevation of temperature for the filter),
- choice to use a cooling device or not, and of which technology.

a. EMC Standard sensitivity analysis

In this first example, the study focus on the susceptibility level of an Airbus EMC standard: the HVDC standard. The aim is to know how this standard impacts the final weight of the filter. Thus, three magnitudes of susceptibility level have been considered:

- the normal EMC standard level,
- the EMC standard level + 10dbA, i.e. less constrained,
- the EMC standard level - 10dbA, i.e. more constrained.

As expected, the filter is heavier with a high constrained standard (and inversely) - the more, the better (Figure 152).

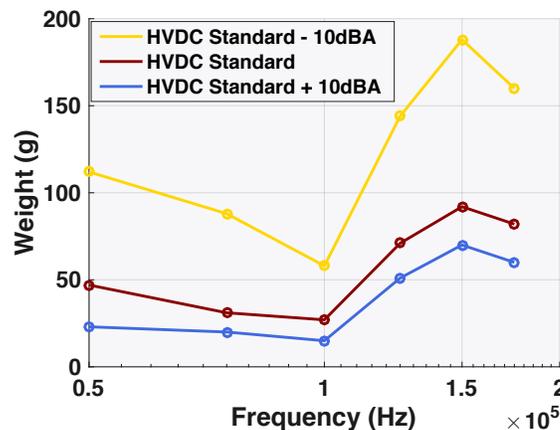


Figure 152: Weight evolution of the filter as a function of the switching frequency and for different levels of susceptibility related to the Airbus HVDC directives

Regarding the shape of the weight curve as a function of the switching frequency, different phenomena have been analyzed:

- in the low frequency range (up to $1e5$ Hz), the filter weight is lower for higher switching frequencies – the more, the better,
- it could be expected as it is commonly admitted that reducing the passive devices can be achieved thanks to a higher switching frequency in a converter. By analysing the results of the filter sizing problem around this low frequency range, the thermal losses are not the

dominant constraints to design the filter. Here it is rather the EMC perturbations that are the most constraining and so, size the filter as expected.

- At a frequency between 100kHz and 150kHz, the weight increases with the switching frequency. At this frequency range, the EMC standard is collapsing (roughly -80dB/dec) (Figure 153). Thus, a simple LC filter (i.e. a second order of -40dB/dec) can only help to pass this constraining slope by shifting its cut-off frequency on lower frequency, which increases the mass of its passive devices.
- At more than 150 kHz, the susceptibility level of the EMC standard is flat again (Figure 153), which allows a slight decrease of the filter mass because the harmonics are less constrained by this flat standard rather than the previous slope.
- For high frequencies (around 200kHz), the weight of the filter increases again because of quick increase of the losses. Indeed, the thermal model normally dominates the EMC constraints for very high switching frequencies.

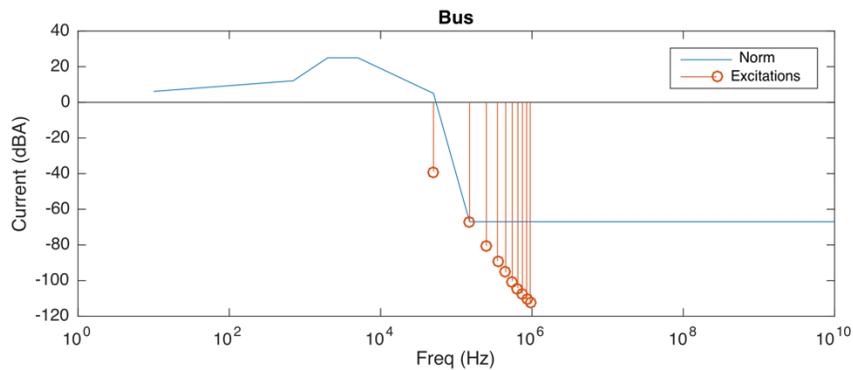


Figure 153: Example of a standard comparison with the Airbus HVDC standard, during an optimization iteration

Regarding the time of computation, roughly 8 hours of work have been required to get the sole Figure 152 presented in Several factors allow to explain this increasing computing time:

- Two devices are now optimized instead of one. Thus, once they are coupled as a topology, it increases the number of optimization variables and constraints to handle in the optimal problem. Moreover, the topology object imposes additional constraints, like the EMC considerations (frequency susceptibility levels, temporal limits, etc.)
- An external solver is used to compute the electrical models and then compare the frequency signals with the EMC constraints (the solver used is Ootee, the frequency solver presented in Chapter 2).

Because of the two previous points, it is less easy to converge towards a global minimum because of a higher global complexity. Therefore, more robust optimization methods have to be used in order to get reliable solutions. In our case, we have selected the MS algorithms with 100 random starting points. Finally, this algorithm is more efficient, although they take more time to converge.

b. Power Sensitivity Analysis

In this second example, three different powers are considered for the converter: 1kW, 3kW and 5kW. Once again, the aim is to evaluate the impact of these power changes on the filter weight.

The results obtained show that the shape of the weight curves is equivalent to the one obtained in the previous analysis. However, the weight results are different. As expected, the higher the power, the heavier the weight of the filter (Figure 154).

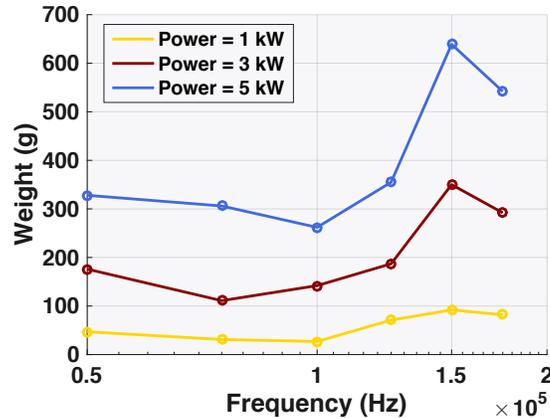


Figure 154: Evolution of the filter weight as a function of the switching frequency for different powers of converters

c. Multilevel Sensitivity Analysis

In our last example, we consider the interleaving variation of a multilevel chopper. As can be seen from the equivalent circuit in Chapter 4 used to represent the multi-level commutation cell, the HV side is only impacted by the parallel configuration, and not by the serial one. Four interleaving cases have been considered, from 1 to 4 cells in parallel.

This analysis shows that the higher the parallelization, the lower the weight of the filter. The global shape of the weight curves is similar to those observed in the previous studies.

However, there is a frequency translation of the weight increase depending on an even (2, 4) or odd (1, 3) interleaving level. This translation can be explained because the EMC standard limits the optimal solution. According to the apparent switching frequency - which depends on the parallelization of the topology since the frequency is multiplied by the interleaving coefficient - the first or the second harmonic constrains the filter design. Indeed they “reach” the EMC constraint (as shown in Figure 153 for the second harmonic). Thus, for odd values, the standard limits the switching frequency to around 125kHz, and for even values around 150kHz (Figure 155).

For the moment, no more explanations or results are available to provide a better explanation of this phenomenon. A deeper analysis is required to really understand what is hidden behind these results.

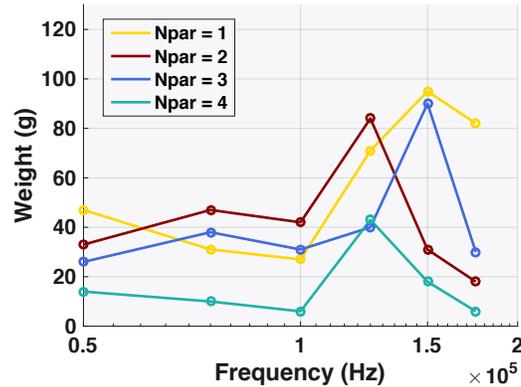


Figure 155: Filter weight evolution as a function of the switching frequency, for different parallel levels and in a multilevel chopper topology

5.2.2. Optimizations of Active Topologies

In the previous example concerning the design of a passive topology, a frequency solver has been used to define the source of perturbation, which is finally an “active topology”. This approach thanks to an external solver allows describing automatically the global electrical circuit of the active topologies. However, this solver is inherently limited in terms of topology and the current status is that it is limited to classical and non-isolated DCDC-conversion. Today, it is very interesting to explore the DC-DC isolated conversion. To do it, we proposed to create analytical solver of these conversion, in order to couple it with the frequency solver that manage the filtering part efficiently. Thus, this chapter concerns the work on these active and analytical topologies through 2 examples: the first deals with a quick and relative comparison of topologies thanks to low granularity levels, in order to show how get quick information for high level studies. In a second time, we now consider a detailed design of topology, through the BBCU application.

a. Isolated DC-DC Converter

To address the optimization of active topologies, a comparison of various classical and isolated DC-DC topologies has been conducted, in order to find the lightest and most efficient one. For this study, no detailed or absolute solution is required on the design of each component. Indeed, only a relative and global evaluation of the converter weight and efficiency is needed. Thus, in order to ensure an easy and quick convergence, the models with a low granularity are the most suitable for this application. The specification of the DC-DC conversion is presented in Table 23.

Parameters	Values
VHV	270 Vdc
VLV	28 Vdc
Power	400W
Standards & Constraints	Airbus Directives

Table 23: Main specifications of the power converter studied

topologies have been identified as interesting candidates (Figure 156). In order to create their electrical models, the Ootee frequency solver cannot be used. Indeed, it does not accept the isolated DC-DC topologies yet (Chapter 2). Thus, analytical solvers for each topology have been created to represent their physical behaviour. This modelling work is based on [173]. It provides the main analytical equations describing the operations of the converter, but also the limitations on the duty cycle values and on the continuous mode.

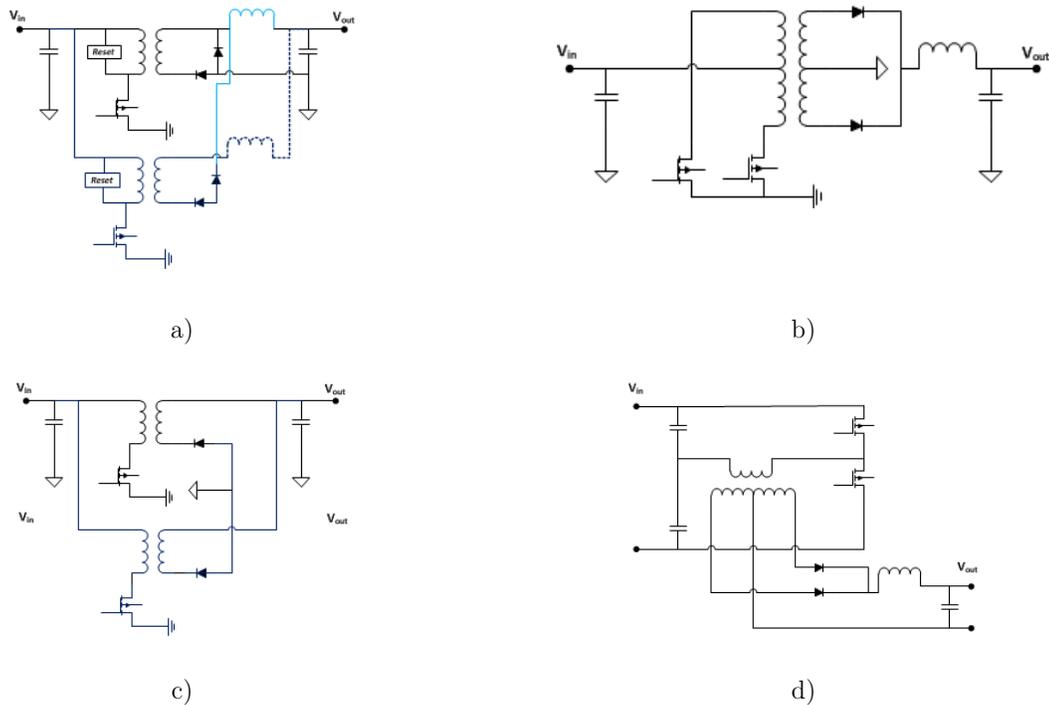


Figure 156: Identified DC-DC topologies

a) Forward (*Interleaved with 2L – with 1 L*) b) Push Pull c) Flyback Interleaved d) Half-bridge

Some of these topologies use a centre-tapped transformer (Figure 156). However, no model of this object has been developed in our device library. Therefore, a classical transformer model is used as a temporary alternative, considering as assumptions that the design and loss evaluations are oversized compared to a real centre-tapped transformer.

Finally, the design results are presented in Table 24 and Table 25 for defined operation points (from green for the best results to Red for the worst ones). Regarding the aeronautical constraints and

Optimizations Examples of power devices, topologies and converters

specifications and according to the optimizations and different operations points, the half-bridge topology is the most suitable for the application studied.

Weight (kg*)	Topology DC-DC 400W						
	Forward	2-level Forward-1L	2-level Forward-2L	Push-Pull	Half-Bridge	Flyback	Flyback 2L
Isolation Stage	0,02	0,02	0,05	0,03	0,02	0,06	0,11
Non-isolated Part	0,24	0,30	0,49	0,15	0,20	0,21	0,12
Heatsink Natural Convection	0,44	0,57	0,44	0,69	0,18	1,74	1,66
Total Weight	0,71	0,89	0,98	0,87	0,40	2,00	1,88

Table 24: Weight analysis with main parameters: $\alpha = 0.35$, $\Delta T = 55^\circ C$, $F_{sw} = 100e3Hz$

Losses (W*)	Topology DC-DC 400W						
	Forward	2-level Forward-1L	2-level Forward-2L	Push-Pull	Half-Bridge	Flyback	Flyback2L
Isolation Stage	0,02	0,76	0,01	0,01	0,31	1,30	0,11
Switches	41,51	49,82	41,25	56,84	21,62	110,28	106,60
Inductor	4,21	0,42	2,44	1,79	0,80	0,00	0,00
Total Losses	45,73	51,00	43,69	58,64	22,73	111,58	106,71
Total Efficiency (%)	88,57	87,25	89,08	85,34	94,32	72,11	73,32

Table 25: Losses analysis with main parameters: $\alpha = 0.35$, $\Delta T = 55^\circ C$, $F_{sw} = 100e3Hz$

As a conclusion, the low granularity models are very useful in the optimization process, because they are quick, they converge well (only a few minutes of computation) and the results are quite easy to analyse. Because of their limited accuracy, the final solutions must be considered with caution (e.g. the final weight is too much minimized and far from the state of art).

However, it was not the goal of this exercise. The key here is to get relative results, enable to set relevant and easy comparisons that we have done.

However, in order to fully realize this kind of quick and rough comparison, the topological and device model's description still has to be improved. For instance, the frequency solver is currently replaced by analytical equations (including high assumptions), and the transformer object used is not accurate.

In addition, it would be very interesting to add a filtering to this optimization problem, thanks to the connection of a passive topology. It will allow to get the real power density under an aeronautical "meaning". This addition of filters on the active topology to form a complete converter has been realized in this thesis by using the methods 'mixed' explained in chapter 2. However, no relevant results have been obtained, due to the increasing complexity of the optimization problem.

A deeper analysis of the inaccuracy or lack of results is given in the last conclusive chapter, in order to provide more information and ways of improvements for the next users and developers of this software platform.

Thus, much progress to achieve remain on each individual part (models, solvers, convergence), before allowing a complete converter optimization.

b. BBCU

This part is focused on the work realized to answer at a specific Airbus application: The Buck Boost Converter Unit (BBCU). The objective of this study is to find an active topology that minimizes the embedded weight into the aircraft.

c. Specification

The BBCU is a bidirectional and isolated DC-DC converter, dedicated to the energy conversion between a new embedded network +/- 270 VDC and a 28 VDC network. The +/- 270 VDC embedded network is currently studied for a possible implementation in the MEA (Chapter 1). The BBCU must transfer up to 12 kW, which makes its design quite challenging, particularly for the low-voltage side because of very high current (up to 500 A). Figure 157 shows how it is used in an aircraft. In addition, numerous operation modes answer to the mission profiles of the aircraft, including a wide range of input and output voltages. That implies major difficulties for the design and the control scheme. The main problematics to design the BBCU in regards to power electronics, is summed up in Appendix. The Airbus specification [174] gives more details on the BBCU background and specificities. To sum up the specifications of the BBCU, the main points are:

BBCU nominal points in the Boost mode are:

- Nominal LV voltage: 28V
- Nominal HV voltage: 540 V. The converter must work on a range of 340V to 650V
- Nominal Power: 12 kW
- Efficiency > 85%

BBCU nominal points in the Buck Mode are:

- Nominal LV voltage: between 24,5 and 31,7 V
- Nominal HV voltage: 540 V or +/- 270 V, for a range of 450V to 650V
- Nominal Power: 12 kW
- Efficiency > 90%

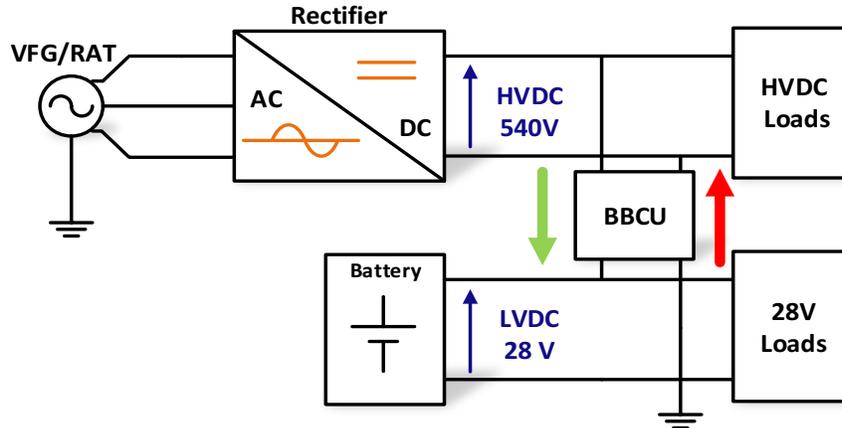


Figure 157: Schematic of the BBCU Principle

The document [175] exposes the details about the different mission profiles and operation modes. Nevertheless, it can be summarized with critical operation points for the converter design as a function of the “Buck” or “Boost” power transfer mode (Table 26). Of course, specifications of both modes must be matched with the same design. Therefore, an option to compute several operation modes sequentially in a same loop of optimization has been created.

Mode	Boost				Buck			
Points	1	2	3	4	5	6	7	8
LV (V)	24,5	31,7	18	24,5	27	29	24,5	31
HV (V)	540	340	540	320	720	400	760	720
Power (kW)	12							
EFFICIENCY (%)	> 85				> 90			
I_{min} (A)	-	-	-	-	-	-	-	-

Table 26: BBCU Critical operation points

More information is available in Appendices about the BBCU specifications. Concerning the equipment **constraints**, coming from the aircraft standards, the main ones are summarized up in Table 27.

Constraints	Value
Delta T amb-jc	55°C
Pressure DROP	6000 Pa
Delta T inlet-outlet	20°C
Number Max channels multilevel	10

Table 27: Main system constraints for the BBCU sizing

d. Topological Overview of Bidirectional and Isolated DC-DC converters

A first step was required to enumerate the possible topologies to apply for the BBCU application. Today, a few revolutions are long-awaited on the topologies of static converters. In most cases, a literature study is enough to list the various candidates dedicated to a specific conversion and highlight the potential best ones. However, their comparisons, in order to select the best structure suited to a specification, is often realized thanks to assumptions, approximation or self-experience. In addition, these calculations are often made successively on the individual devices (i.e. component by component) of the converter and do not take into account a global and optimal approach.

On the other side, the selection of structures could be conditioned by different factors or combination (performance, reliability, integration, mass, cost), making different relative “best” topologies. Thus, a multi-objective approach is often required with the most accurate calculation to design each component. In our case, we consider that a mass mono-objective also implies an indirect optimization of the efficiency in order to maximize the power density of the converter.

Finally, the BBCU study is only focused on the family of reversible DC-DC converters with a galvanic isolation. A complete **topological survey** has been realized and presented in Appendices, including topics like multistage or multilevel topologies and snubbers to improve the initial topologies. Thus, this survey allows establishing a shortlist of promising BBCU topologies to optimize and compare thanks our pre-design methodology (Figure 158 & Figure 159). The candidates are:

- Dual Full-Bridge topology
 - with the inductor on the LV side
 - with the inductor on the HV side
- Dual Active Bridge (DAB) converter
- Push-pull current doubler interleaved rectifier
- Push-pull centre tapped rectifier

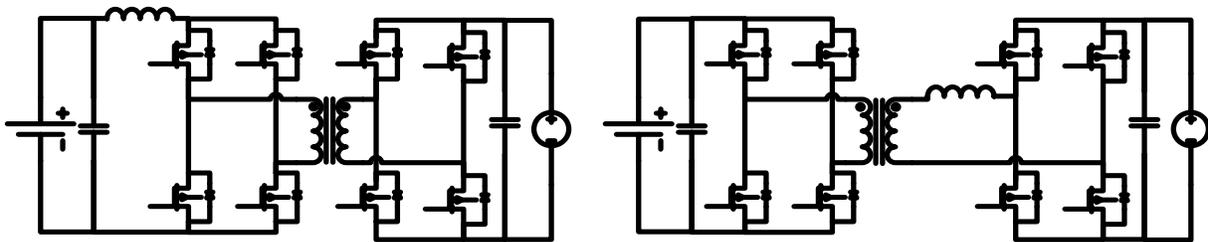


Figure 158: a) Full-bridge Converter Voltage and Current Sourced
b) Dual Active Bridge, a two-voltage sources full-bridge

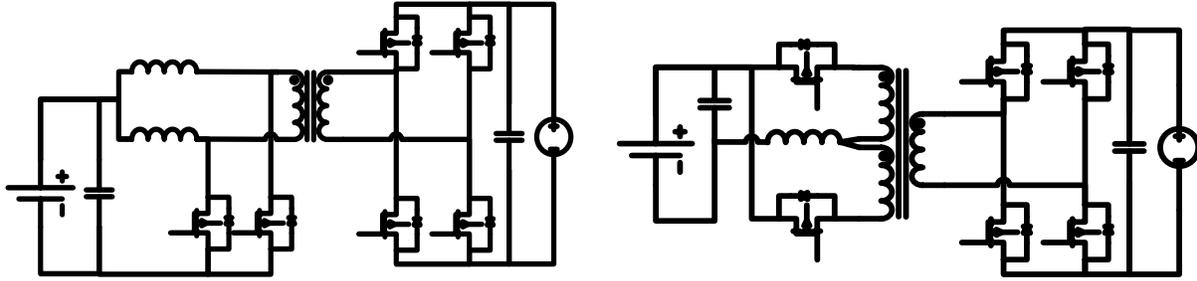


Figure 159: a) Bidirectional and isolated converter with a current doubler
 b) Bidirectional and isolated converter with a push-pull circuit

e. Analytical solver

To compute the optimal problem, analytical and continuous models of “active topologies” have been created in order to build an “analytical solver” for the BBCU candidates. To realize it, equations of [35] have been totally readapted, to propose a solver that defines and computes the electrical behaviour of multilevel, isolated and bidirectional DC-DC converters in a **direct way**. The main steps of the direct way for an active topology are:

- The geometry/shape/dimensions of devices allow defining their own electrical values
- These electrical values are injected into the electrical circuits, i.e. in our case the analytical solver
- Then, thanks to the analytical equations, we can describe the converter behaviour and provide operation points useful for the design. Indeed, this analytical solver directly approximates the time and frequency vectors that will be applied at the bounds of the different devices of the converter
- Finally, the objectives and constraints of the converter and devices (specially losses and thermal constraints) are calculated and compared until an optimal solution is found

On the contrary, another solver and a User Interface presents these models also for an inverse modelling [35], i.e. from the converter specification to the electrical values of devices (Figure 160).

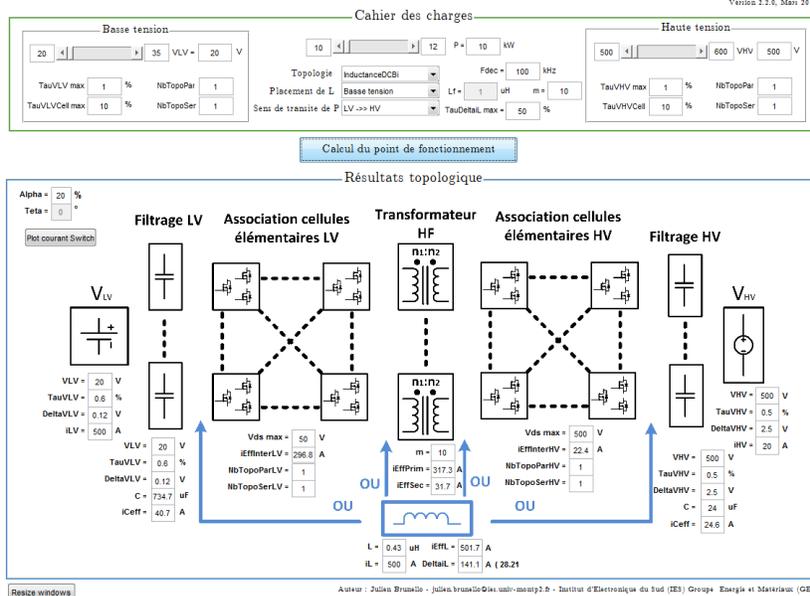


Figure 160: User Interface (UI) computing in an inverse way the analytical equations of the different BBCU candidates [35]

This direct modelling has been completely verified through PSIM simulations and this includes multi-level configurations. As an example of this verification, Figure 161 shows a comparison of temporal waveforms for the current-doubler topology.

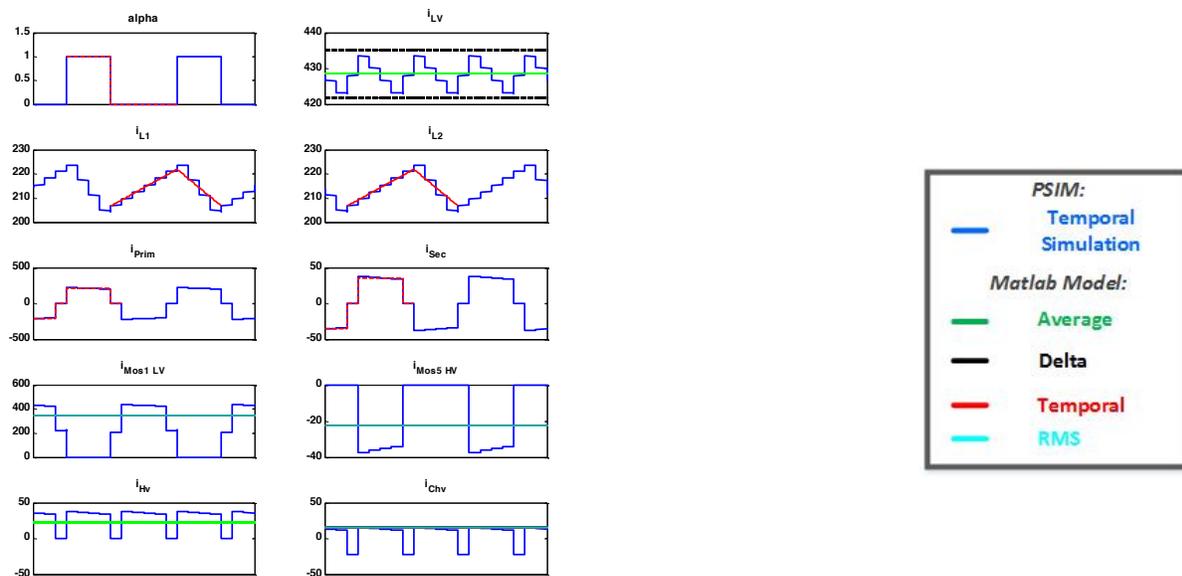


Figure 161: Current-doubler validation of the analytical model thanks the PSIM simulations @100kHz, $L_1 = L_2 = 10e-6$ H, $CLV = 1e-6$ F, $CHV = 2e-6$ F $m=6$, $v_{Hv} = 540$ V, $v_{Lv} = 28$ V, $\alpha = 0,4$, $P = 12e3$ W ; Transit Way: V_{Lv} to v_{Hv}

However, this verification has only been made on a limited set of operation points. The lack of this approach was to not ensure a complete validation, especially on a wide range of operation points as

it is the case in optimization computations. Indeed, the electrical definition of [35], including multilevel and continuous variables seems to not be robust during the variable exploration of an optimization (e.g. non-physical results are obtained on outputs for some devices, when non-obvious parameters are proposed by the optimizer as inputs). A solution to avoid this problem is, either to limit arbitrarily the range of exploration, but we limit the final results; either to constrain (and so refuse) the non-physical output values directly in the optimization problem. Nevertheless, it increases the complexity of the problem and causes convergence problems. The allowable intervals of the different inputs (or the non-physical output values) are easily identifiable by using the graphical interface of the indirect modelling (interface represented in Figure 160). For instance, an input which create a non-physical output values could be a lower or higher inductance value.

As a conclusion, the solution to use analytical solvers of topologies in order to replace the missing definitions in the frequency solver, stays a good approach. It is quick to execute and represents very precisely the physics inside the devices and the converter (as the PSIM validations have proved it). However, the method proposed here for the solver with the continuous description has to be rethought, in order to make it more robust. It is required to better know its domain of validity to be finally directly used in optimization (without using tips that temporarily correct the problems as it is realized today, inserting a bias in the result).

Another important point is the methodology of validation. In the future, a more global and automatic approach has to be applied rather than a limited set of points to validate models. However, it is often complicated to check everything, as encountered for many cases in this thesis. Testing, checking, detecting bugs, is time consuming and many design projects will be needed to determine the domain of validity.

f. Comparison with a prototype

Thanks to the creation of a first BBCU prototype [35] in the ETHAER project, it was possible to assess the different models involved in the optimization problem, (i.e. the analytical solver and devices models through a loss comparison). Indeed, data about the global losses of the converter has been communicated to us at different operation points. It has been measured thanks to the water cooling system exchanger. However, the precision is not known, therefore precautions have to be taken on this evaluation, and we consider that only the global coherence of models with reality can be compared here.

The prototype is a two-cell version, constituted of a 3kW brick of the current doubler topology (1/4 of the final 12kW demonstrator). The transformer has a serial interleaving for the HV side and two parallel cells for the LV side (Figure 162). This configuration has been recreated thanks to the model library. As an example, Figure 163 presents the specific model of the planar transformer used. All other functions (auxiliary circuits, decoupling capacitors, snubbers) are present in the prototype and its implementation prefigures precisely the future converter, as explained in [35].

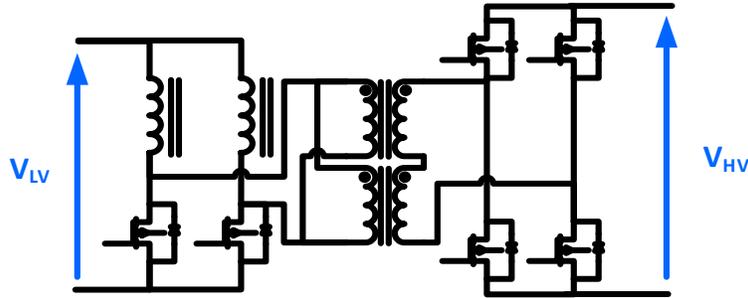


Figure 162: Schematic of the 3kW BBCU Prototype

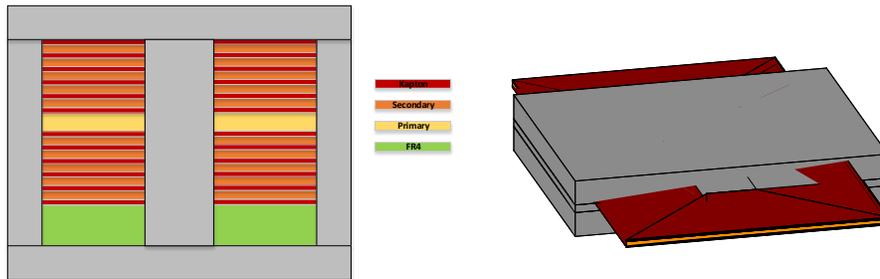


Figure 163: Schematic of the planar transformer used in the 3kW prototype, with its model representation from Matlab

However, the real prototype contains snubber circuits to optimize the semiconductor losses (active limiter or active clamp). They cannot be simulated by the analytical solver yet. Thus, our hypothesis is that we over-evaluate the losses thanks to the models. To conclude, the results of this comparison (Figure 164), provides a mean average rough error of close to 20% (with peaks up to 40%).

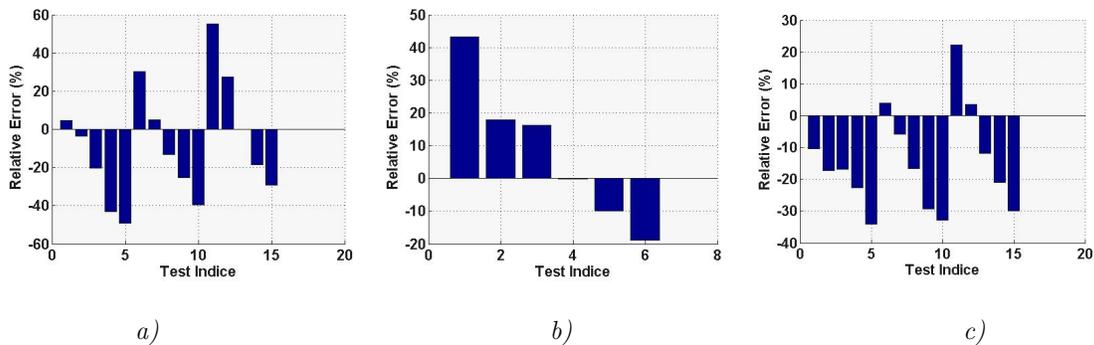


Figure 164: Relative error of the topology global losses between our models and measurement on the real prototype (from [35]) - Boost mode @18(a), 19(b), 20(c)V to 540V - (the test indices indicates different operation points of the high voltage side between the available range of the specification)

It is finally difficult to conclude on these results. We can only say that the modelling is not so bad, because output values stay “physical” in spite of their inaccuracy to describe a detailed design. Some points can be highlighted to explain some potential sources of errors versus the real world:

- The individual errors of the different models of device are added, implying a potential higher global difference if they are all contributing to maximize the final error of the system
- The precision of the experimental measurement is not known, that can be sometimes important, especially on thermal set ups
- The little difference of definition between the simulation and the prototype (e.g. snubbers, simplification of the transformer). Our library does not contain all the models and put assumptions in some models to ease the calculation of physical phenomena.
- Other bugs or problems of conception that have not been detected for now

The conclusion is that it is difficult to compare exactly our models compared to the reality yet. Indeed, the library is not complete and must be completed with new phenomena (e.g. snubbers, ZVS/ZCS switching, resonance). In addition, we had no other opportunities to compare our models with real prototypes.

In the future, it is very important not to stay at the computing level to assess the models through simulation and FEM validations. More time must be spending on real designs and projects to debug all the possible problems that are not detected yet. A final experimental work and design would bring a very interesting feedback on the optimizations.

g. BBCU Topology Optimization

Some BBCU optimizations have been realized on the candidate topologies, for different switching frequencies and for different multilevel configurations (in serial and parallel). The aim was to assess how is working the computer-aided platform on an active and analytical topology, and then to discuss its current efficiency. The objective function of the BBCU optimization was the weight, and its constraints have been explained previously in this section in addition of the own internal constraints related to each component and composite (as explained all along this chapter).

We will first consider the current-doubler topology. The Figure 165 presents its optimized weight results for three different switching frequencies, as a function of the losses. Only the highest granularity available has been used for each device in order to simulate and optimize the most precise power converter.

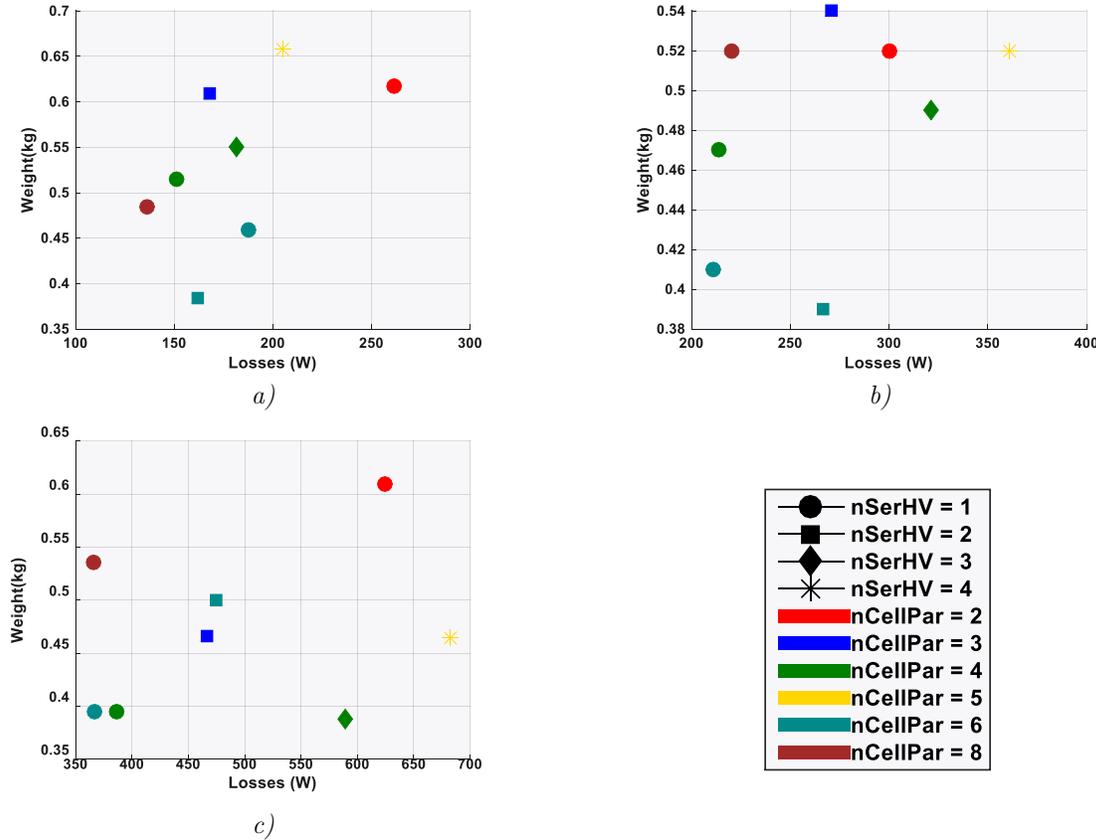


Figure 165: Current-doubler topology weight optimization as a function of losses at various switching frequencies 50 kHz(a), 100 kHz(b) and 150 kHz(c) and multi-level configurations

Although the optimization problem is well running and propose a final solution for each configuration, some obvious blocking points appear in the solutions at the end:

- A low global weight is obtained compared to the state of art for DC-DC conversion (1kW/Kg), even by adding an approximated weight of mechanics, filters and other missing part in the converter description.
- As already explained, the topological object is bounded by arbitrary values to avoid the non-robustness of the analytical solver. That limits its exploration domain, since the problem is more constrained by these values during each iteration rather than real “physical constraints” like thermal or electrical ones. In these conditions, it is here very complicated to ensure that a real optimum is found.
- Another point is the non-physical coherence of results. It is normally expected that more there is losses inside a same configuration, more the weight has to be high. And it is clearly not the case.

To conclude, some non-visible bugs occur either on the convergence of the problem, either inside the models of devices. Same results and problems can be extended to the other BBCU topologies, available inside different optimization problem inside the platform. Although, the global

optimization problem is running, now the main work is to locate and fix local bugs in order to really provide relevant solutions, and so a real optimal design. Indeed, validations of components have been well verified and domain of validity have been fixed, but now we need to enter in a global debug phase, by using this code in numerous design project, but also and mainly compare it with real conceptions.

About the debug, it would be judicious to add and create debugging functions, more automatic to locate the problems in order to fix them more efficiently in the future. Finally, this thesis is only supplying a methodology, models and tools allowing the whole topology optimization, but the results cannot be exploited for now in the case of pre-design.

Another temporary solution would be to use the PSIM simulations files and couple them with the optimization platform. Even if the continuous interleaving is lost with this approach, it could be a better assessment to debug only the device models, by isolating the analytical solver bugs, or even assess if the convergence is ensured.

5.3. Conclusion

It is time to conclude on the global effectiveness of the different types of available optimization types exposed in this chapter. Only a review on the process and results is here proposed, since a more global survey englobing all the thesis parts is proposed in Chapter 6. Thus, it consists by listing the successes and fails obtained for the moment during the computation. But also, to analyse the remaining work to achieve a powerful design tool providing real optimum on a global converter design.

5.3.1. Success

From previous examples, several successes can be highlighted:

- Device Optimizations:
The optimization of a single device is today well-realized, even with the most accurate models that imply more complexity in the optimization problem. Thus, on a sole operation point, this computation takes only a few minutes, depending on the resolution methods.
- Filter Topology Optimizations:
On the same way, the optimization of a single filter topology in its different modes is also well-realized, but takes more time to tune the problem to get relevant results, always in a few minutes of computation.
- Sensitivity analysis:
The single optimization can be extended to sensitivity analyses, as presented in some figures of this chapter. That consists into generate optimizations from a set of input variables, by varying parameters or objectives. Its aim is to demonstrate the dependency of different

variables between each other. Nevertheless, sensitivity studies multiply the computation time by the number of required points. To improve it – when the power of classical laptops are limited or to get draft and quick results - it is possible to degrade models thanks to the granularity, but the results accuracy is impacted.

- Multi-objective studies:

Multi-objective studies & Pareto Front can also be envisaged with the software platform, even if examples have been focused on single “weight objective” in chapter because of the aeronautics goals.

- Application to some pre-design project:

Majority of computations provide relevant results and have been applied to some industrial pre-project on single device optimizations. They have been validated by state of art, FEM, and databases, and mainly used for pre-designs, trade-offs, call of tenders or specification definitions. But never for a real design, that stay a problem (this point is developed in the next part).

- **Solvers coupling:**

The coupling with the frequency solver Ootee, and other commercial or analytical solver is fully operational, allowing more easily the creation of many applications (especially for the filtering applications in this Chapter).

- **Efficient UI:**

The creation of a UI has greatly facilitated the creation of optimization problems. Indeed, it is more intuitive and it is possible to visualize directly all the tuneable parameters, without forgetting some that can be hidden in scripts. It also helps to be a showcase or a demonstration of the pre-design work in power electronics.

5.3.2. Missing part

Some missing parts and failures are still present in this final work. These points require to be investigated in order to solve remaining bugs:

- **Lack of low granularity levels in models:**

When sensitivity studies are used, it can spend days to get the final curves (depending on the number of points and granularity of the models used). That is often too long in contrast of the awaited results, that are only general tendencies instead of precise results. It can be explained by the fact that for some devices the low granularity models that are quicker and better adapted to this kind of study have not been maintained. A main focus was on the high granularity ones. We chose to privilege higher accuracy in order to get better results.

From experience, it is finally a big lack in our platform, because low granularity is perfect to debug and set new optimal problem because of their low complexity and more easy aspect to

investigate and understand occurring problems. In addition, it would have been simpler to begin our work with low granularity models to create and build the platform, debug all the problems, and then progressively increase the complexity of model to gain in accuracy.

- **Robustness of the Analytical solvers:**

The analytical solver for the isolated and bidirectional DC-DC conversion is not totally achieved. Although it works well and was validated for pre-defined operation points, it is not the case when it is inserted in an optimization, as explained previously (5.2.2.e). The temporary solutions used to correct this problem have to be improved, because it highly increases the complexity of the resolution or bias the final solution, that is not good to ensure an optimal design for the converter.

- **Global Converter optimization**

- **Coupling (filter topology + analytical solver):**

Because of the lack of relevant results on the BBCU optimizations, it is impossible to conclude on the strategy to couple filter topologies (using the frequency solver) with an active topology (using the analytical solver). However, scripts defining this architecture are available, are running and could be tested if the previous problems are solved.

- **OOTE solver (filters + active topologies in the frequency solver):**

Optimisations on a global chopper with filters on the low and high voltage side has been tried. However, not enough time has been accorded to this study and few results have been obtained. The fact to assembly all these elements increase the complexity of the convergence, but supply an output. However, before concluding on this part, more validations are required on a simple filter, with the creation of a prototype for instance to ensure the optimum.

- **No validation through the design of real prototype**

No real design has been realized using the final results of an optimization. Indeed, we did not get opportunities to lead a complete design with the pre-design tool in order to validate the real efficiency of this approach. However, this step is essential to continue to develop this kind of computational platform. Only the real design experience can confirm if this strategy goes into the right direction.

- **User Interface**

No complete “converter” optimization is available in the UI, that is stopping at the filtering definition. The next step is to extend the UI in order to propose a complete visual tool.

- **Not enough debugging functions**

Something that could be very interesting for future work and development, is the creation of debugging function or more visualization in order to detect bugs and errors in the solutions, especially in the UI.

Chapter 6

6. Conclusion and Future Work

In this memoir, we have explained how to conceive a new computer-aided platform, in order to design and optimize power electronics equipment dedicated to any industry or application. In this context, methodologies, tools and models have been created to contribute to the virtual prototyping research in electrical engineering. This work has been tested on some applications, mostly using the aeronautical requirements and constraints. However, from the results obtained, it is evident that much improvement remains to be accomplished before releasing a final software. Indeed, the final aim that is to allow the direct optimization of global converters from an electrical specification is not entirely reached yet. Therefore, we propose in this chapter some concluding remarks to provide an overview of the manuscript. And then, a feedback and analysis of our work is proposed, as well as new ways of research and improvement for the future.

6.1. Conclusive summary

In Chapter 1, the context of the thesis has been presented, introducing the aeronautical industry and a focus on the More Electrical Aircraft (MEA). This context implies the development of a new HVDC electrical network, and so of new power electronics systems. These systems have to be more integrated and efficient to overpass the current technological locks. To address this problematic, we have proposed the “digitalization” of the design process: i.e. the creation of a computer-aided software, based on a new pre-design methodology. It should allow to optimize directly the design process of the components of a power system, in order to provide very good design solutions and global trade-offs. As an introduction to this quite new application field in power electronics, we have realized a survey of the required design problematics and challenges to design a power converter. The aim is to synthetize the requirement, elements and specification essential to include in the design platform.

In Chapter 2, we have exposed our complete methodology to create the global development platform. It details how to model, simulate and optimize the principal devices and topologies that constitute a power converter. The main ideas regarding the modelling of devices, are to use the Object-oriented programming (OOP), continuous modelling and granularity levels in order to create and organize a wide range of models in a library, with different ranges of validity. We have also chosen to favor the deterministic algorithm of optimization in our strategy, with one or several objectives to ease the convergence. Moreover, the frequency solver ‘Ootee’ has been preferred to reduce the time computing of each simulation. However, it stays limited in terms of topology. Therefore, we also added other solvers – temporal, analytical and FEM – in order to extend the possibilities and flexibility of our platform. Other IT features have been coded to ease the creation of the optimization

problem, its resolution and the communication between the different objects of the converter. It is important to note that this work has represented one of the main parts of the coding work, especially to ensure a pleasant user experience. In addition, a User interface (UI) has been created to demonstrate a first user experience for the pre-design software in power electronics. It changes the classical way of designing the electrical applications and gathers all the options and models exposed in this dissertation.

In Chapters 3 and 4, we have presented our multi-physic and continuous models (electrical, magnetic, thermal and fluidic) of power devices. On the one hand, the converter has devices acting in its active part: semiconductors and cooling systems. On the other hand, it has passive devices: capacitors, magnetics that can be assembled as filters. For each object, the direct modeling has been highlighted, i.e. we can deduce all the internal parameters required to the physical solvers and optimization from the geometry, shape and material. In addition, several equations have been proposed for each physical phenomenon occurring in devices, in order to let the designers establish a coherent granularity. Finally, the domains of validity, limitations and missing parts of each model have been highlighted to provide a pertinent feedback and let ways of improvement for future modeling works.

In Chapter 5, we have proposed a review of some applications realized with the optimization platform in the aeronautical context. Thus, we have proposed sensitivity studies on single devices, but also on passive and active topologies of converter and filters. It allowed to demonstrate the benefits of a pre-design tool and how to make choices and trade-offs in electrical engineering. We have also approached the global optimization of an HVDC-DC power converter, which helps us to demonstrate the limits of our research and the remaining work before releasing an efficient and global commercial tool.

Finally, in this conclusive chapter we propose a general feedback on this research work and new fields of research in optimal design for power electronics, and more generally in electrical engineering.

6.2. Feedback and Future Fields of research

In order to discuss future areas of development for our optimization platform, different topics are proposed that have represented important locks during the development. These points have been worked and improved all along the thesis and have now to be the subject of feedbacks. Thus, propositions to extend new research and directions are developed, in order to keep improving the engineering field of the pre-design in power electronics.

6.2.1. Collect and Store Data

A primordial aspect to create some physical models, and that has been minimized at first, was the construction and extrapolation of databases. Excel sheets have been built progressively, as a function of the requirement of new parameters, and in parallel of the methodology construction. Indeed, this

Conclusion and Future Work

solution has been used for the flexibility it offers to fill in, modify and organize data. However, it is not tailored to handle thousands of references with reliability and efficiency.

Now the needs and database patterns have been well identified. Thus, a way of improvement could be to switch to more “professional” solutions, like real SQL databases in order to treat, sort and interpret them more efficiently, especially during the extrapolation stage.

Another issue was the human interpretation while adding new part numbers in bases. Indeed, some points occur:

- Different users have filled in the bases and have applied their own assumptions and interpretations. As an example, different methods have been used for the discretization of datasheet curves to fill in some electrical parameters, or have mixed typical and maximal values. Therefore, some of these parameters can be misinterpreted or are missing, which creates a global lack of coherence in the database and so, impacts some errors or inaccuracy in the final extrapolated physical models for the power devices. A solution should be to establish a more detailed nomenclature and identified specific methods/tools to fill this database in.
- Data collection from different manufacturers/dealers is sometime complicated, because there is not a common formalism. Thus, they do not provide the same parameters and do not use the same measurement conditions. It should be interesting to identify the problematic parameters and rearrange them in the bases for the main manufacturers.
- This way to fill manually the databases is very time-consuming and does not allow an easy refreshing when new products are released. Thus, either we find how to get more unified information from the manufacturers to consolidate the bases more easily. Either with the emergence of the digitalization and big data, it could be interesting to create new automatic computing methods to get the information automatically and with more efficiency. It would also secure the process to avoid human errors as in the first point.

Secondary data are also deduced to complete some parameters of bases thanks to external simulation software, like the switching coefficients for semiconductors by using PSIM simulations. It could be very interesting to automate and mutualize these processes in the future inside a same global tool that should manage collection, simulation and modelling of the parameters.

The final aim is to get very clear, reliable, up-to-date and easy-to-sort databases in order to extract interesting references for applications or even to use them discretely. Thus, we could obtain more efficient and accurate models.

6.2.2. Domain of Validity

The domain of validity for physical models is essential to compute optimizations. Very wide range of inputs (e.g. from the mm to the m for the dimensions of device) are wanted in the modelling, in order to cover a maximum of cases during an optimization. In this context, it is difficult to propose a unique model validating this complete range. Indeed, it often includes components with different technologies, materials and internal architectures, which do not match with a same model

description. Also, the more we increase the model validity, the more the accuracy decreases because of higher assumptions. Thus, new strategies have to be found to answer to this problematic and keep working on models with open domains of validity.

The proposition of this thesis is to insert a granularity level in models as an input, considering a more or less precise physical description of the devices. It allows designers to explore solutions from a global and large description to a very precise and detailed modelling. In addition, switching between these levels needs to be easily established. However, it requires to propose a very complete library of models, proportional to the number of levels. In addition, the idea of using a computing expert system was introduced in Chapter 2, in order to automatically evolve between the different granularities to find the best solution for the optimization according to what the designer is looking for. Thus, it could automatically answer to the validity range problem by choosing the most appropriate levels for the current problem, and step by step identify the real need for the system. However, this system still needs to be entirely developed and the model library has to be completed in order to match the 3 granularities that we defined: system, converter, device.

6.2.3. Validations of Models

In order to analyse and validate the optimization results, we need to evaluate the mean error of each physical model, especially for the objective quantities (e.g. weight and losses). However, this task is very complicated and rigorous to perform it on each model of each device and each topology. Because of lack of time and capability, we have not been able to do so in details for all the models that have been created. Therefore, further work is needed to define a generic way to validate each model more easily. Three axes of validation have been used during the thesis:

- About COTS devices, the comparison with databases is easily feasible, to calculate an average error, especially with the curve fitting tools present in the Matlab software. However, it is important to select a wide range of devices, in order to improve the domain of validity of our models. Another approach, is to use the literature and perform comparisons with existing studies, but it is limited and must only be used as a temporary solution.
- In this thesis, when it was possible and available, experimental validations have been preferred with specific test benches. However, few opportunities have been possible. Important future work has to be realized on real prototypes and benches, to really assess the modelling work, in order to know if this pre-design approach is going in the right direction. However, it is often long, complex and expensive to set up.
- Because of the complexity of real validation, it has been often replaced with FEM simulations in this thesis. Indeed, once they are well initialized, they propose relevant results very quickly. FEM simulations can also be automated to directly validate optimization results and refine them if needed. Nevertheless, they are not so easy to create and require experience to converge to a relevant solution.

Thus, several approaches have been explored as far as possible. But a work is still required to perform automatic tests on models and particularly the need to achieve validation with real prototypes. In addition, it is very important to save these validations as “unit tests” in a specific library, in order to know if the models are still correct when modification are introduced in the platform software. As a conclusion, this validation part in the pre-design of power electronics has to be highly improved in a close future.

6.2.4. Electrical Solvers

Several electrical solvers have been tried in order to find the best tailored one for a pre-design study. As explained in the memoir, the frequency solver has been privileged, that proposes very quick simulations and a relevant accuracy in spite of its simplifications. However, today this solver is still limited in terms of topology and features. For instance, only chopper and inverter topologies are available to run with our optimization package. It is essential to extend the frequency solver features to other essential topologies in power electronics – galvanic insulation, resonant switching, snubbers, etc. Thus, a huge improvement of the tool is feasible, but temporary solutions are possible to fill in this gap:

- The first one is to use the classical temporal solvers, which are less efficient for optimization computation but allow to simulate all the topologies. A solution should be to use a computing power higher than the one of our current laptops, by using servers for instance. Thus, we could use easily these solvers, but also more demanding algorithms and get better solutions and so unblock many convergence problems. These solvers are accessible from our optimization platform, but have not been tested in this thesis. Thus an interesting work would be to perform comparison between the different solvers.
- The second point is the creation of analytical solvers that has been tried in this memoir. They can be easily found in literature, are quick to code and compute, and they bring new advantages like the consideration of a continuous interleaving for multilevel converters. Nevertheless, this solution is not flexible, presents approximations and can provide non-physical solutions because of a validity domain that is not well mastered. Thus, this approach is not a complete success, and work has remained to prove its complete efficiency, especially from the definition of the equations. In addition, we can consider the analytical solvers as a temporary solution that will be replaced by more flexible solver in the end to provide a better user experience.

6.2.5. Model Integration

The integration of models in the optimization platform requires a complete methodology to call and compute these objects. Indeed, during a computation, the physical models of power devices need to interact together, but also to communicate with the optimizer, the graphical interfaces and solvers, in order to share data and results as explained in Chapter 2.

A pattern to organize these different classes of objects (i.e. the Comp3d pattern: device, topology, converter) has been proposed to answer to this problematic. But also to create generic functions to compute the different variables and data, called at various stages of the computation and the optimization.

This methodology has to be established from the beginning of the modeling work, because it determines the architecture of each model and object representing a device, topology or a converter. These computations and exchange functions require a considerable work and influence directly the efficiency of the tool. Therefore, this part has not to be underestimated, and must be considered and planned as an important part of the modelling work.

In addition, a methodology and library of “integration” functions have been created that is now complete and well-suited to the models and objects presented in this manuscript. However, this proposition could be modified, if new objects are added. Indeed, it has been built on demand, in parallel of the modelling work. Thus, it would be wise to analyze whether this generic method is always efficient – especially for a complete electrical chain of conversion – and readjust if necessary.

6.2.6. Convergence of the Solution

The convergence of an optimization problem to a global and optimal solution has been a main concern to create our strategy and methodology. Therefore, the development of continuous models has been chosen, with the use of deterministic algorithms. It works well today for single devices and individual topologies as shown in Chapter 6. Nevertheless, even with this “simplified” approach, many convergence problems can appear when very detailed models are used in the optimizations, with a large number of optimization variables. Thus, it is still complicated to converge directly and at a first try to a satisfying solution for a whole power converter (i.e. an active topology and its filters) because the problem is too complex today.

Moreover, the simple gradient descent is often blocked in local minimums, and advanced algorithm of optimization are always required, including random aspects (Multi-start, GS) or heuristic algorithms to get a global solution. In some cases, we fail in converging at all, or it was too long to compute (up to days). It means that something has been missed in the methodology, that bugs or discontinuities are present in objects and models, or even that the assembly of the object/solver/optimizer induces a hidden problem. Therefore, it is essential to continue to improve this angle (methodology, modelling, algorithms etc.).

An immediate solution may be to consider this problem under a more mathematical aspect, by developing specific algorithms and functions dedicated to the power converters. Another one would be to use more powerful calculation units in order to remove the computation time constraint and launch more efficient computations with more frontal algorithms. Only by resolving these current locks, it would be able to optimize complete electrical chains or complete converters implying the complete filtering of the equipment, that today do not provide pertinent enough solutions.

6.2.7. Software Considerations

Matlab has been chosen to create the optimization functions, models, and to prototype the global software because of its ease of coding, scientists' packages (e.g. optimization and UI) and the community. However, although this solution is very useful at first, it is expensive in term of licence, not free of rights and is depending on its own libraries.

One question to ask for the future is whether it is appropriate to stay on this platform. Or if it is better to switch to other ones also possessing strong scientific libraries such as Python or Java. They would allow designers to get more control on the code, models and computation and be more efficient. But also to be able to share and/or sell this pre-design software more easily. However, good IT skills and experience are required to build a proper architecture, as well as to maintain and develop the different packages required for this kind of business. Thus, people with strong computer sciences skills will be required to improve the electrical engineering field in this case.

6.2.8. User Interface and User Experience

A Graphical User Interface (UI) is proposed to deliver a first version of that could be an optimal user experience for a pre-design software in power electronics. This interface allows to identify the best design opportunities thanks to simulations, optimizations and trade-offs. Its aim is to approximate easily the objectives driving today the power electronics from a specification (e.g. power density, efficiency, cost).

Today, this interface is limited to the optimization of power devices and filters. It does not consider a complete topology and a dynamic circuit creation, with free component placement. However, this graphical part is being developed on another project in the laboratory, and should be presented soon. Thanks to this GUI, we have proved that our methodology is suitable to be released to new users as it offers an 'intuitive experience'. However, it has to be completed and improved in order to propose more features and libraries of options, models and devices, like the whole definition of a power converter.

6.2.9. Results Exploitation

Regarding the exploitation of the results obtained, we can easily make relative, multi-objective and sensitivity studies to compare and establish trade-offs of technologies and architectures thanks to the UI and pre-made scripts. However, considering an absolute analysis on results remains complicated because we still have problems to evaluate the accuracy of models on the big range of dimensions that are used to define the optimization problems.

In addition, it is very complicated to know how to consider the cumulative errors of the models we have today quantified. Indeed, errors may be added or balanced. Furthermore, current results cannot be compared with real equipment, which makes the validations and conclusions complex. For example, on a weight study, we have only optimized the internal components of the power converter, but we have no idea of the mechanics, drivers, PCB influence etc., which can be up to

25% of the device global weight (from Airbus designs). Thus, a great avenue of progress remains to refine results and better quantify the error margins, especially on a global design.

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References

8. Appendix 1 - Electrical Model SC

a. Switching-cell Model

First, a simple classical active topology containing a single switching cell of two interrupters (buck or boost topology) is considered. This switching cell has been simplified with a generalized model, i.e. controlled and ideal voltage/current sources (Figure 64). It means that we get square-waveforms (or trapezoidal, closer to the real magnitude) signals, whose amplitude and frequency vary. In addition, and to calculate operation points of the switching cell, equivalent conduction resistances can be added. In the case of a classical switching cell, these resistances are estimated during the respective conductions of the top and bottom switches. A proposed formulation is given in (1). This average representation has been used in the OOTEE solver (chapter 2) in order to create our equivalent sources of current and voltage. Another option is to replace controlled sources by resistances with infinite or adaptable values, in order to improve the accuracy of the resolution. However, the compute time is increased, that is less attractive for optimization resolutions.

$$R_{eq} = \alpha \cdot R_{onTop} + (1 - \alpha) \cdot R_{onBottom} \quad (1)$$

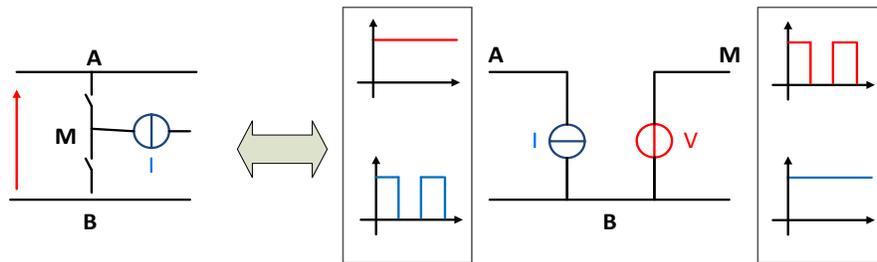


Figure 166: Representation of a classical commutation cell with controlled sources

b. Analytical EMI Sources

The square waveform (or trapezoidal) representation has also a big advantage. Because of its linear and analytical formulation, there is no need to use an external solver. Indeed, it is simple enough to establish the analytical expressions of the frequency domain thanks to a linearization hypothesis. This method has first been preferred to calculate losses and compare standards in electrical engineering. Indeed, it has to be privileged for the EMC studies to define the different EMI sources in a power converter. It is called a “direct method” or calculation, compared to the solvers which are called “indirect”. Different techniques are available to calculate square and trapezoidal waveforms, as detailed in [58] [176] [177]. Some examples from this cited literature are presented in Table 28 and a comparison is given in Figure 167. These examples are only a synthesis for this kind of models. The parameters are explained in detail in references, with more figures and explanations in order to understand them.

Appendix 1 - Electrical Model SC

Fourier-simplified	$F_{square}(x) = \frac{4}{\pi} \sum_{n=1,3,5,\dots}^{\infty} \frac{1}{n} \sin\left(\frac{n \pi x}{L}\right) \quad (2)$
Fourier	$F_{trap}(n) = A \left[\frac{(\text{sinc}(t_r \cdot \pi \cdot n \cdot F_0)) \cdot e^{-1j \cdot \pi \cdot n \cdot F_0 \cdot t_r}}{1j \cdot \pi \cdot n} - \frac{(\text{sinc}(t_d \cdot \pi \cdot n \cdot F_0)) \cdot e^{-1j \cdot \pi \cdot n \cdot F_0 \cdot (2t_w + t_r)}}{1j \cdot \pi \cdot n} \right] \quad (3)$
Envelop	$E_{trap}(n) = \frac{2 \cdot A \cdot t_w \cdot F_0 \cdot P1 \cdot P2}{(p+P1) \cdot (p+P2)} \quad \text{with } P1 = \frac{2}{t_w} \text{ and } P2 = \frac{2}{t_r} \quad (4)$
Laplace	$F_{trap}(v_n) = A \frac{t_w}{T_{dec}} \left[\frac{\text{sinc}(t_r \cdot \pi \cdot v_n) \cdot e^{j t_w \pi v_n} - \text{sinc}(t_f \cdot \pi \cdot v_n) \cdot e^{-j t_w \pi v_n}}{t_w(j \cdot \pi \cdot v_n)} \right] \cdot e^{-j(2 \cdot t_{delay} + t_r + t_w) \pi \cdot v_n} \quad (5)$
Convolution	$F_{\overline{trap}}(v) = F_{trap}(v) \cdot S_w(v) \quad \text{with } S_w(v) = \text{sinc}(\pi \cdot \tau v) e^{-j \pi \tau v} \quad (6)$

Table 28: Analytical EMI sources calculation by direct methods

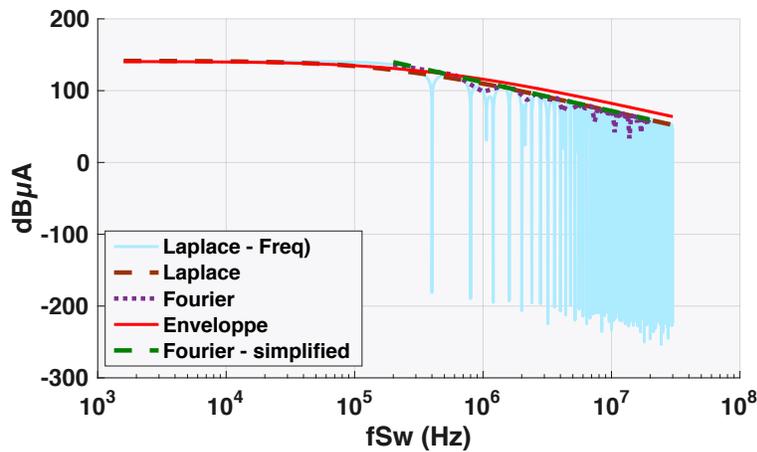


Figure 167: Comparison of the different EMI sources models from a direct definition

These relatively ideal waveforms, allow an acceptable frequency representation for a range of medium frequencies. In addition, new devices like wide band gap present less switching losses and are often faster, involving steeper dv/dt s and di/dt s, and so closer to the square representation. In addition, more realism can be brought to the sources by taking into account some critical phenomena such as oscillations, overvoltage, or recovery phase during the switching. Only new equations are needed, also defined by Laplace transforms [57].

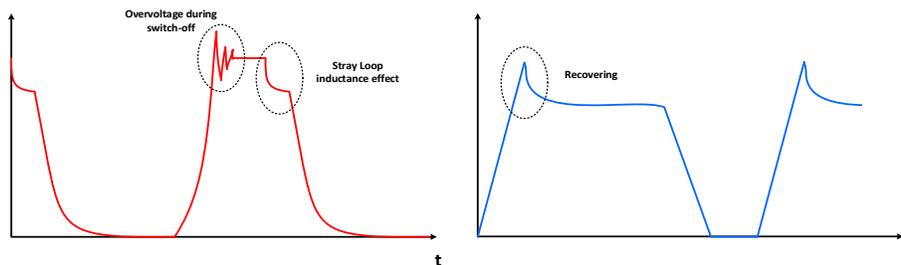


Figure 168: More realistic switching waveforms to be considered

c. Multi-level switching cells

As said previously, rather than using macro-switches, we can use a multi-level conversion (3.2.3), that has been used in the optimal problems. The increasing number of cells is beneficial in high voltage or current applications, since it allows a voltage and current distribution between multiple semiconductors or switching cells. Thus, using higher-performance semiconductor with reduced sizes is possible. The multilevel principle has already been presented in numerous thesis [178]. In a few words, the nP cells of a parallel multilevel converter are controlled by the same duty ratio and a phase of $2\pi/k$. If the system is balanced, the current in each phase is equal to the current of the low voltage divided by the number of phases. By analogy, in serial converters the voltage is divided by nS . Both serial and parallel interleaving can be used simultaneously, and so we obtained the equations below for a buck converter as explained in [179]:

$$\Delta V_{LV} = \frac{V_{HV}}{n_s \cdot n_p} \quad (7)$$

$$\Delta I_{HV} = \frac{I_{LV}}{n_p} \quad (8)$$

The frequency is multiplied by the number of phases on each side as follows:

$$F_{appLV} = F_{sw} \cdot n_p \cdot n_s \quad (9)$$

$$F_{appHV} = F_{sw} \cdot n_p \quad (10)$$

As a conclusion, an AC equivalent model is represented in Figure 169 for a mix of serial and parallel interleaving. This principle is re-used and developed in more details in Chapter 4 regarding the filters.

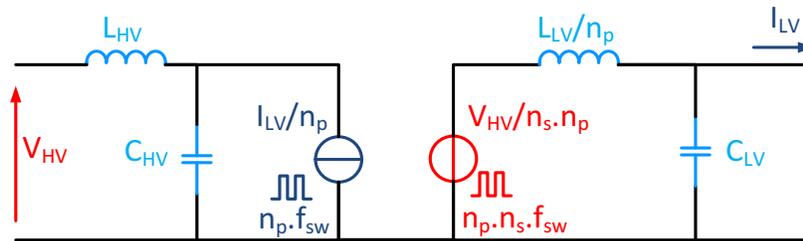


Figure 169: AC equivalent model for a multilevel conversion

9. Appendix 2 –Cooling Validation

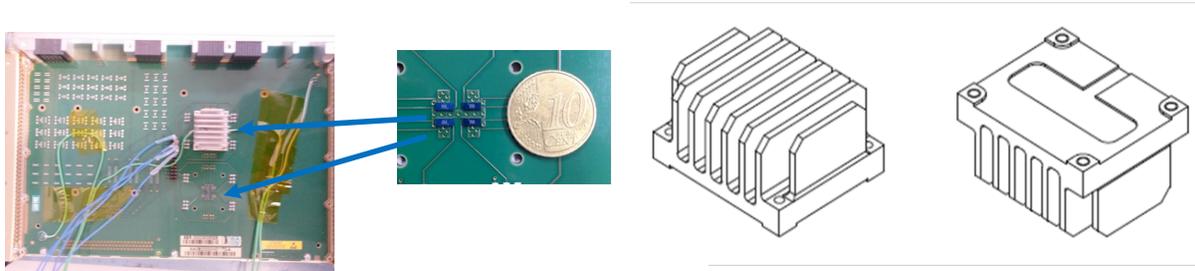


Figure 170: Circuit board and Heatsink used in the experience

The board is placed in an avionic rack and cooled by a laminar airflow. Measurements are carried out under the conduction mode of SC, without ventilation at first and then with a pressure of 300 Pa corresponding to the ground pressure of the IDEE5 program. From the pressure drop curve measurement, the airflow characteristic is estimated with precision.

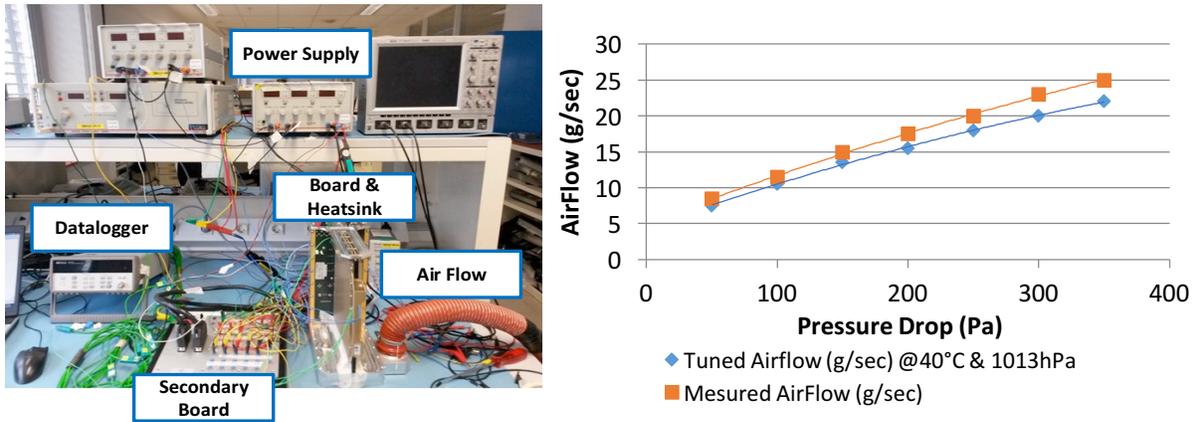


Figure 171: Experience set-up and Air Flow vs. Pressure Drop measurements during the experience

A few examples of thermal measurements are exposed hereafter. They have been realized for convections on one or two devices under conduction modes, and for different semiconductors powers. In addition, several thermocouples have been put at the closest hot spots and interesting locations, to deduce the different thermal resistances.

Appendix 2 –Cooling Validation

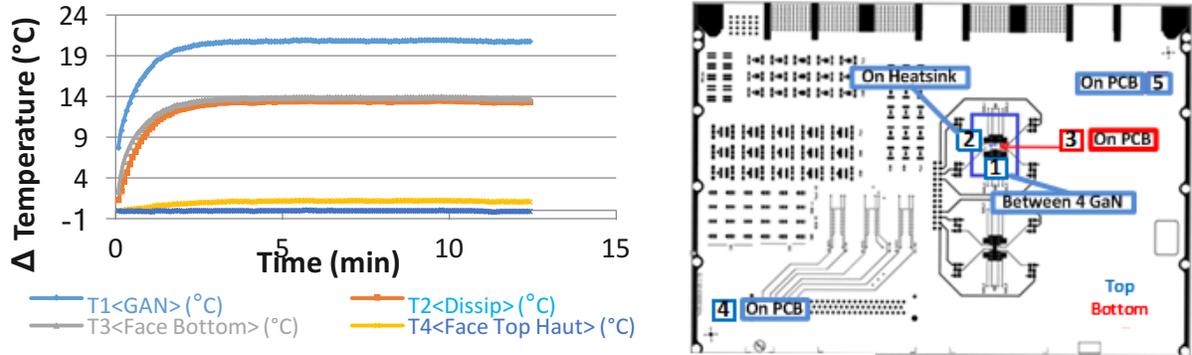


Figure 172: Thermal measurement for the 2dies x3 Watt configuration - with air cooling $T_{amb} = 18, 2^{\circ}\text{C}$; $P_{GaN1} = 2,95\text{W}$; $P_{GaN2} = 2,98\text{W}$ $\Delta T1 = 20, 7^{\circ}\text{C}$; $\Delta T2 = 13, 3^{\circ}\text{C}$; $\Delta T3 = 13, 7^{\circ}\text{C}$;

From previous measurement, it is easy to deduce the different global thermal resistances of the system, as a function of the power.

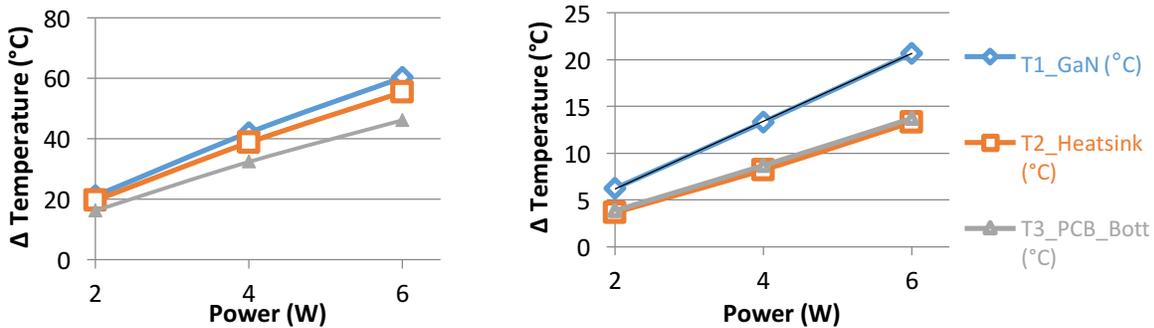


Figure 173: Global thermal impedance results e: (a) Without Air Cooling – (b) with Air Cooling

Then, we approximated a thermal model using the models explained in this chapter, in order to compare our modelling to the reality and following the principle of Chapter 3 . Relative errors in different configurations are showed hereafter.

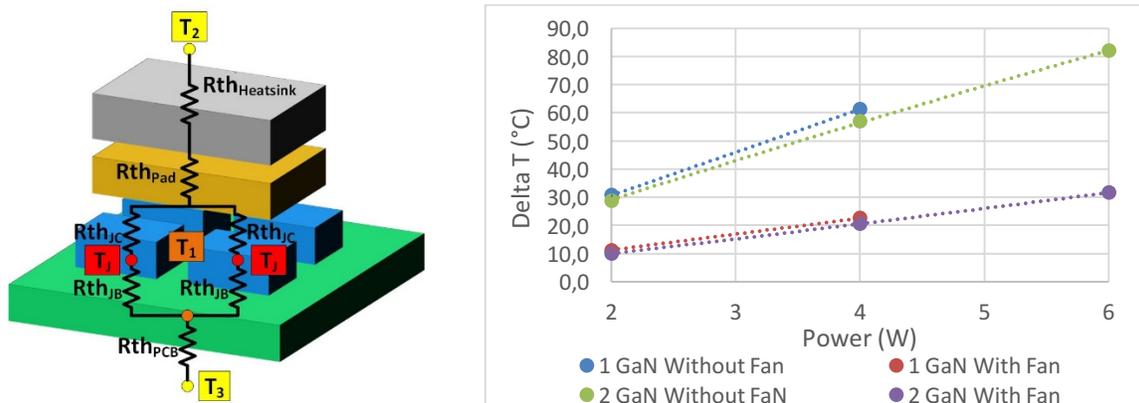


Figure 174: Thermal model circuit hypothesis and results of the model

Feedback and Future Fields of research

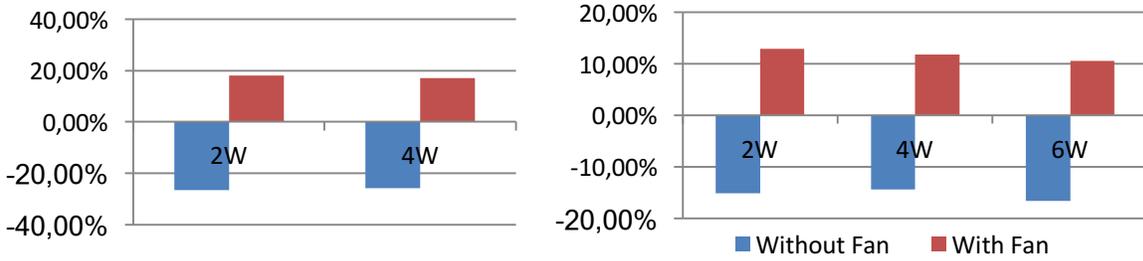


Figure 175: Relative error between measurement and simulation a) 1 chip b) 2 chips

As a conclusion, models are quite accurate with a maximal error of 20%. Thus, we can estimate with an analytical model the maximum power as input for this switches in the considered environment. As an example, if we take a maximal temperature of 105°C for the die, we get the temperatures displayed in the table below.

T _{max} possible	Power	T _{calculated}	T _{max}
Without Cooling	8	105,1	105
With Air Cooling	17,5	105,3	105

Table 29: Junction temperature model as a function of the power

Appendix 2 –Cooling Validation

10. Appendix 3 – Transfer function approach for the EMC perturbations – Common Mode

We propose an analytical common-mode model for multi-level converters based on a transfer function approach. We consider a simplified LISN as a simple RLC circuit, with R_{LISN} being the normed resistance at 50 ohms, C_{Par} the parasitic capacitance and L_{LISN} the loop stray inductance. Then, once the LC filter is chosen among a 0, 2nd or 4th order (Figure 176), a global transfer function is calculated.

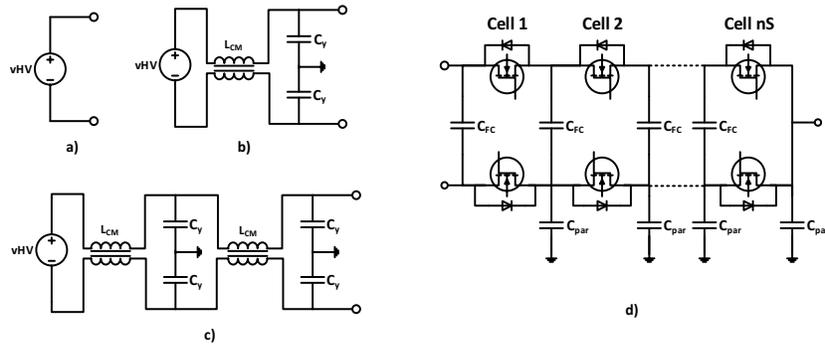


Figure 176: Multilevel common-mode model a) 0 order b) 2nd order c) 4th order d) real representation

As we can see, a parasitic capacitor is dedicated to each stage, i.e. to each switching cell. The problem is easily simplified thanks to the representation of the impedance of each component in equivalent impedance (Figure 177 and Table 30). Although formulas are available for parallel legs, only the transfer function of the n_S series cells of 1 leg are calculated here. If n_P legs are connected in parallel, the transfer functions are simply multiplied by a n_P factor. This hypothesis is correct when working with envelopes of in-phase spectra with phase-shifted and interleaved legs in parallel. However, it does not allow tricky designs using harmonic cancellation of specific components.

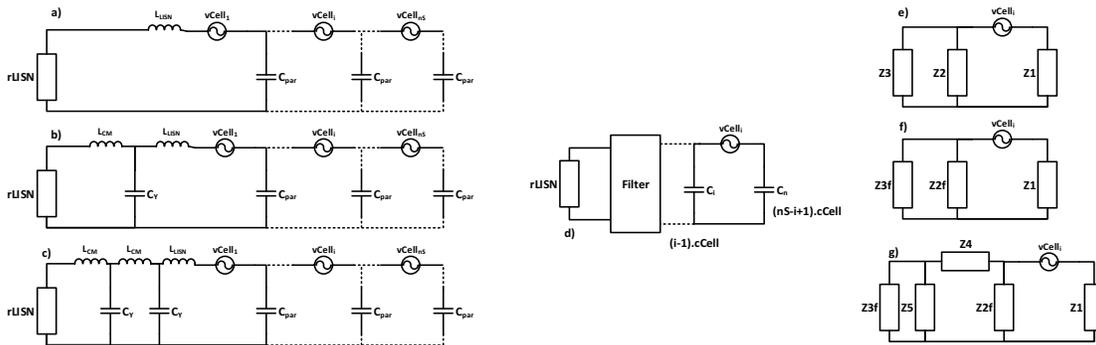


Figure 177: Simplified model of multilevel common-mode through transfer function calculations

Appendix 3 – Transfer function approach for the EMC perturbations –

Common Mode

	Formulas				
Z1	$1/(nS + 1)/cCell/s$	(1)	Z3f	$rLISN + (lLISN + lCM(3)).s$	(2)
Z2	$1/(i - 1)/cCell/s$	(3)	Z4	$lCM(2).s$	(4)
Z3	$rLISN + lLISN.s$	(5)	Z5	$1/Cy(3)/s$	(6)
Z2f	$1/((i - 1).cCell + cY)/s$	(7)			

Table 30: Impedance values corresponding to the circuit of Figure 177

11. Appendix 4 – BBCU Design Challenges

11.1. Specifications

From the specification, it is possible to directly identify the conversion principle required to realize the BBCU function. It is divided in three parts and represented in Figure 178:

- A chopper to generate a high frequency AC voltage
- A transformer providing galvanic isolation
- A rectifier to provide DC voltage output

From this simplified definition of the BBCU operation, it can be established some evident design challenges and technological locks to solve.

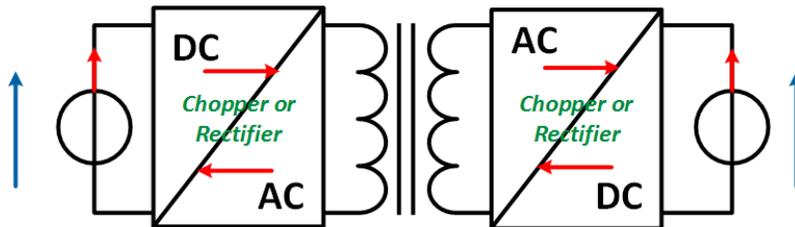


Figure 178: Bidirectional and isolated DC-DC Converter Principle

Despite the improvements and profits brought by the new BBCU concept, numerous challenges appear to entirely design the converter in terms of electrical and aeronautical considerations. A non-exhaustive list of technological locks has been identified and presented hereafter.

11.2. Design Challenges for the BBCU

- **What is the best topology for this application?**

The great difference between high and low voltage prohibits the use of non-isolated structures. Indeed, isolated structures necessarily imply a double conversion AC/DC/AC and so an increase of the weight because of the addition of magnetic components. This principle covers a wide range of isolated DC-DC converter, with one or two stages of conversion (addition of a buck/boost for instance), and the use of multilevel converters. In addition, different ways to operate the switching losses are possible, including better efficiency but more components.

- **How to handle the reversibility of the power transfer?**

The bi-directional function increases inevitably the structure complexity. Therefore, the design must minimize the design intricacy to be totally compliant and reliable in the aeronautical context. Different ways are possible to realize this function, like two unidirectional converters or a sole

bidirectional converter for instance. In addition, we can use one or many transformers depending on the topology or directly integrate filtering aspect thanks to isolated Intercell transformers [16].

- **How to increase the converter density?**

To be efficient and integrated in regards of the global system of the aircraft, the BBCU density must be optimized in terms of power/mass and power/volume. In addition, the cohabitation between high voltage and high current adds difficulty to build a compact system: high voltage requires thick insulation and installations against partial discharge problems while high current causes an increase of the conductor weight.

- **How to comply with the constraining standards and the safety requirement of the aeronautic industry?**

The quest for compactness and efficiency usually results in increasing the perturbations and so overpassing the aircraft standards. Thus, a compromise will be compulsory to be compliant with the standards. In addition, filters are often designed after the construction of the converter, which sometimes implies bad or not integrated solutions. Thus, we lost the gain realized on the converter design because this work was not included in the primary design. It is why, a direct optimization of the converter and its filters would be a big advantage to consider a global optimum.

- **How to guarantee an efficient high transformation ratio and optimize the volume and weight of the magnetic component?**

Through a galvanic isolation, the high and low voltage difference has to drive various modes of operations. It implies many challenges letting few degree of freedom in the design. In addition, the mission profile of the converter due to the aircraft and the different modes of operation have to be included in the optimization in order to provide the best ration in spite of these limitations and huge ranges of operation. In addition, the high power and low voltage requirement implies very high currents (up to 500A). As a result, these key components have to be particularly well designed. As said previously, some routines exist do realize optimal design of magnetic components. The fact to link them to the optimization of the whole converter will allows to optimize this touchy component in term of mass and integration or even cost.

- **How to reduce the recurrent cost while guaranteeing the quality of the converter?**

The price of a new development can make the recurrent cost of the converter explode because of the creation of specific components or the lack of control on the design, which lead to buy inappropriate components. However, an acceptable compromise certainly exists in order to reach a minimum cost with good performances in regard to the specification.

11.3. Annexe 4 – Bidirectional and Isolated DC-DC Converter Review

11.3.1. Principles

a. Bidirectionality

Before beginning our overview of topologies, we need to introduce the reversibility concept of a DC-DC converter. In fact, a bidirectional converter between two voltage sources can be very simply achieved via two unidirectional converters. The first conversion uses a “forward” power transfer, from V_1 to V_2 , while the second carries out a “backward” conversion from V_2 to V_1 (Figure 179a). For an isolated topology, we usually combine two converters by inserting on each side an inverter and rectifier stage (Figure 179b). It allows to gain in integration and avoids doubling the number of components, although it implies a design trade-off on component shared by both directions. This principle is deeply presented in [180] with some examples and electrical definitions.

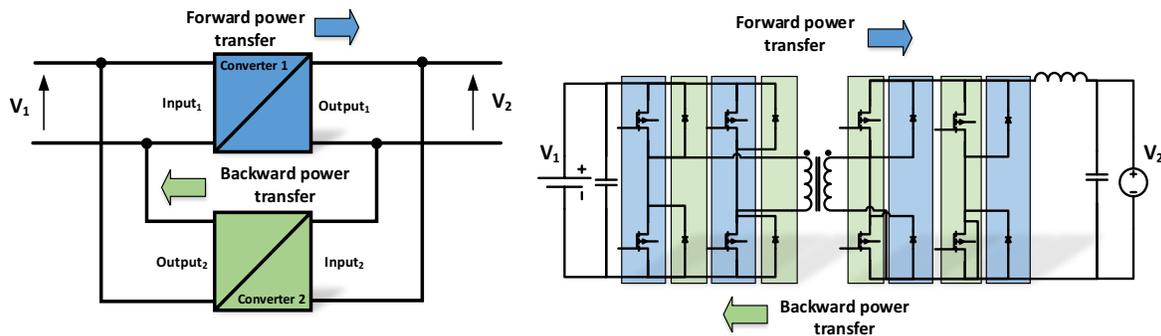


Figure 179: a) Principle construction of a bidirectional DC-DC converter using two unidirectional DC-DC converters - b) Classical bidirectional DC-DC converter with a DC/AC double conversion

b. Architecture

The literature proposes many candidates for isolated DC-DC converters. Most of these converters can be described by a common architecture, divided into four parts (Figure 180):

- **Input and output filter networks**, at least represented by a single capacitor or inductor and required to provide smooth terminal voltages and currents.
- **DC-AC converter** provides AC power to the transformer and then **AC-DC converter** supplies DC power to the receiving port, with a bidirectional power transfer. Typically, full-bridge circuits, half bridge circuits, and push-pull circuits are employed. However, different solutions are possible, like a single switch network used in a bidirectional flyback converter [122];
- **Reactive High Frequency Networks** provide energy storage capability within AC part and are used to modify the shapes of the switch current waveforms in order to achieve low switching losses. Even though, these parts are not necessarily required for a fully functional

bidirectional DC–DC converter, they will always be present in practice due to the parasitic components (e.g. stray and magnetizing inductances, parasitic capacitances).

- **High Frequency Transformer** is required in order to achieve electric isolation; it further enables large voltage and current transfer ratios.

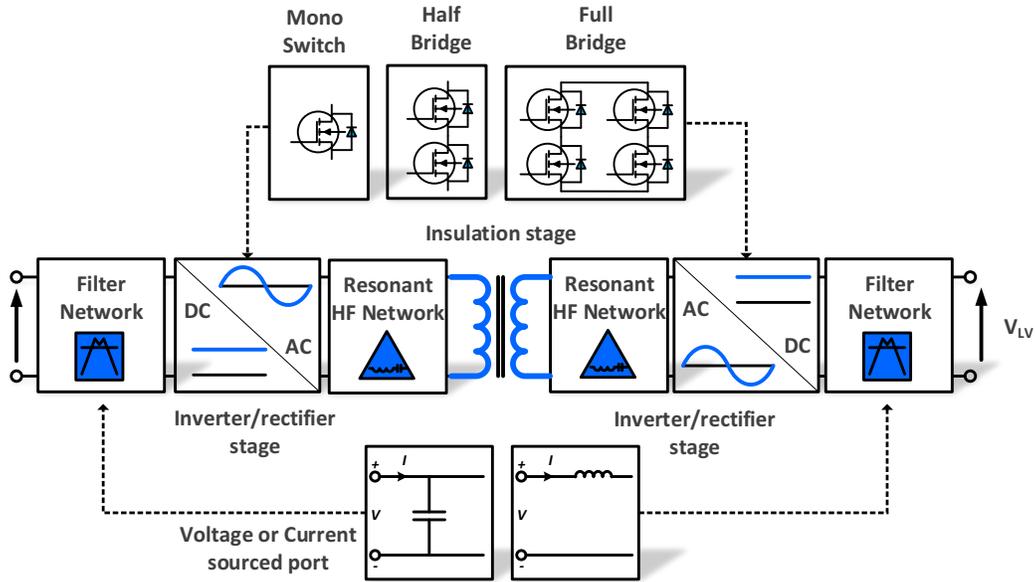


Figure 180: Generic architecture of a bidirectional DC-DC converter with a galvanic isolation

11.3.2. Topologies of Conversion

In order to choose the conversion topologies, we can rely on an extensive literature, which provides this inventory work [181] [182] [35], numerous information, pros & cons, references and equations. Therefore, we only propose a non-exhaustive list of topologies without analysis. Indeed, the purpose of this thesis is to compare directly this list by performing a global optimization, without realizing previous estimations. The single stage topologies is made of three families (

Figure 181). In fact, we only consider non-resonant Dual Bridge converters, containing DC–AC and AC–DC stages, and realizing higher efficiency conversion for high power applications – as explained in 11.3.3. Regarding other families, we will not consider the topologies with few switches and discontinuous operation, normally employed for low voltage and low and medium power applications (flyback, forward and Ćuk). Nevertheless, some work on these topologies exist. For instance, [122] proposes a 12kw flyback converter (270/28V), with eight parallel cells using an Intercell Transformer for the filtering, coupling and galvanic isolation.

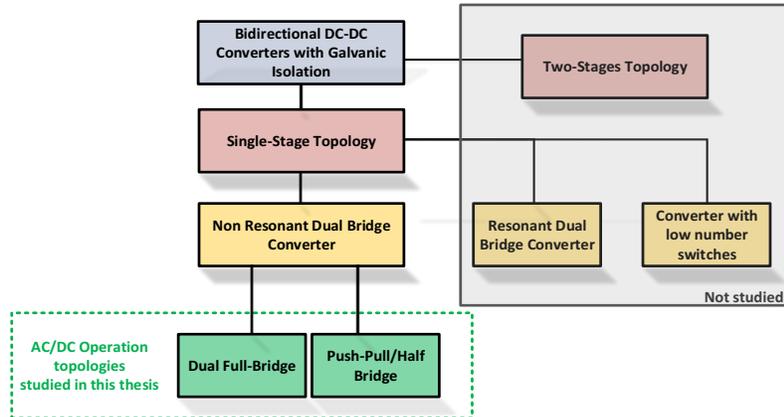


Figure 181: Topological Overview of bidirectional DC-DC converters with a galvanic insulation

The last family contains DC–DC converters with resonant HF networks (Figure 182), which offer in particular increased capabilities regarding the utilization of the semiconductor switches [183]. Many topologies of resonant tank exist in the literature, and it would be too long to all enumerate them. Even though converters with unidirectional power flow are thoroughly described in literature, only a few on bidirectional converters can be found. One of the reasons might be that the converter is more complex and that they require additional HF components. The main advantages and drawbacks of the most common unidirectional resonant converters are summarized in [184]. In addition, we have decided not to study them for several reasons. One of them is that due to the experience of the ETHAER project partners [185] we prefer to develop hard switching conversions that reach equivalent or better efficiency without additional components or more complex structure and control. Another indication of the last decades is to consider the lack of interest in R&D for these topologies, with no development of commercial products.

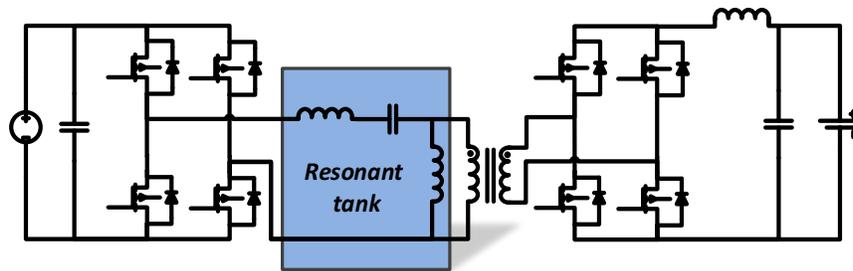


Figure 182: Bi-directional resonant converter, with a LLC resonant HF network

11.3.3. Non Resonant Dual Bridge Converters

As explained previously, our topologies comparison only considers the non-resonant dual Bridge converters, containing DC–AC and AC–DC stages (11.3.1.b). They are usually composed of full-bridges or half-bridges and push-pull converters, which allow us to divide them in subfamilies.

a. Dual Full-Bridge converters

One characteristic of the **dual Full-Bridge** conversion is that semiconductor switches can be operated with soft switching, implying low semiconductor losses and so a possible high power density. We identified two usual structures depending on its non-resonant high frequency network location (a simple inductor or the transformer stray inductance itself):

- **Before the switching stage** on the LV or HV side (Figure 183-a), called voltage and current sourced converters. Two subcategories are possible: the current-fed where the inductor is located at the input of the converter [186], [187], [188], and the voltage-fed where it is located at the output [189], [190]. A three-phase version can be found in [191]. Other interesting information can be found in [192], [193], [194], [195].
- **Between the switching stages** on the LV or HV side (Figure 183-b), called two voltage sources converters. When an inductor is located between both active arms, we generally call the topology Dual Active Bridge (DAB) [196], [197], [198], [199]. Other interesting information can be found in [200], [201], [202], [203], [204].

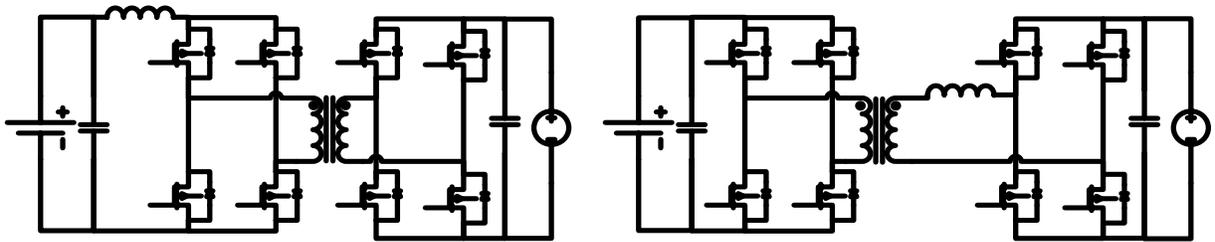


Figure 183: a) Full-bridge Converter Voltage and Current Sourced – b) Dual Active Bridge, a two-voltage sources full-bridge

b. Push-Pull/ Full-Bridge converters

Instead of a full-bridge on the LV side of the converter, different AC–DC configurations can be used like half-bridges or single switch topologies. To better understand the difference, [205] presents a comparison between full-bridges vs. push-pull topologies in low voltage and high power DC-DC converter. The converters of this family are:

- The **push-pull current doubler interleaved rectifier** topology (Figure 184-a), composed of separate inductors and single switches on the low voltage side [206], [207], [208], [209], [210], [211] [212]. This topology also exists in three-phase versions [213], [214], [215].
- The **push-pull centre tapped rectifier** topology (Figure 184-b), with a single inductor on the LV side [216], [217] [218], [219], [220], [221]. We also found three-phase version [222], [223], [224].

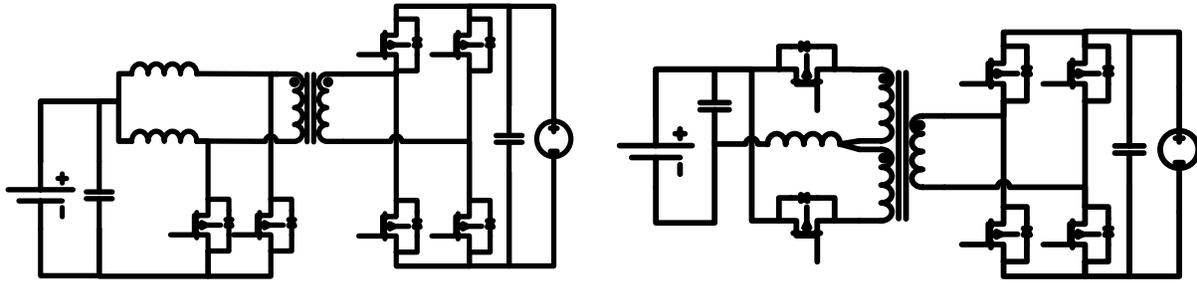


Figure 184: a) Bidirectional and isolated converter with a current doubler – b) Bidirectional and isolated converter with a push-pull circuit

11.3.4. Topology Improvements

a. Multi-Stage Topologies

The topologies enumerated previously (Figure 180) are called Single-Stage converters, since they contain a unique conversion stage. However, their wide-range voltage operations can sometimes make transformers and switches ineffective. An improved utilization of these elements is achieved thanks to a multi-stage topology, containing an additional power converter in order to adjust voltage and current levels (Figure 185). Indeed, the topologies are operated more efficiently and evenly if the input to output voltage ratio is close to the transformer turns ratio. Thus, a two-stage solution allows a more evenly distributed converter efficiency. Indeed, it employs an additional buck and/or boost converter without galvanic isolation, in order to adjust the voltage applied to the converter stage. However, the total number of components is higher. Thus, the additional DC-DC converter needs to be highly efficient in order to achieve a higher global efficiency. The classical arrangements (Figure 185) are composed with bidirectional buck or boost converters, which allows both way power transfers.

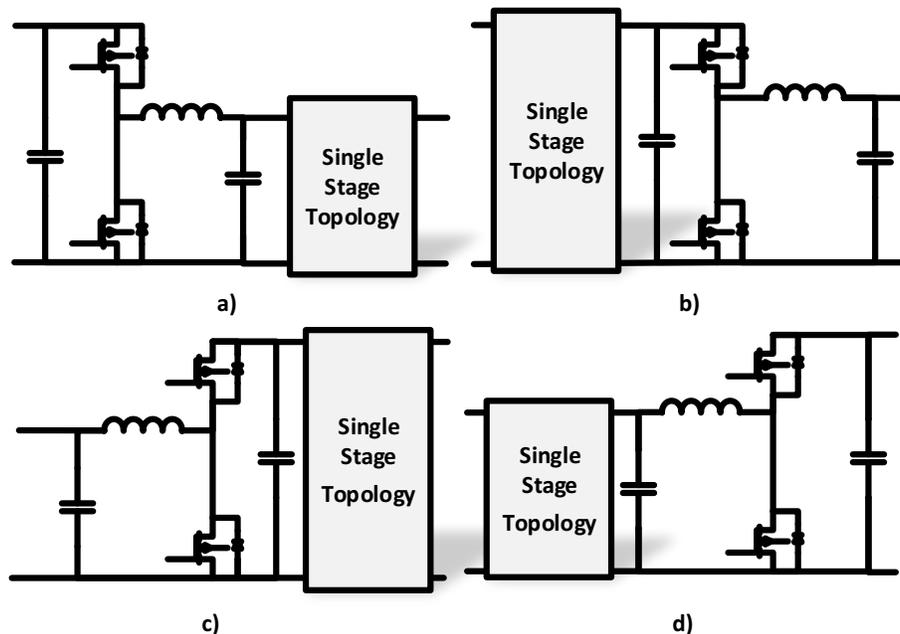


Figure 185: 2-stage converters a) HV side buck converter - b) HV side boost converter c) V side buck converter d) LV side boost converter – As a notice a) is the topology for the first BBCU prototype at Airbus

In [180], for a Dual Active Bridge (DAB) topology with specifications close to the ones of the BBCU, four different two-stage configurations are investigated. The aim of the study was to determine which structure is the most efficient. At a defined output power (2 kW), the efficiency distribution obtained for two-stage solutions are more balanced than a single-stage converter. However, the average values ($92.7\% \leq \eta \leq 93.0\%$) are less than in the single-stage (93.5%). Thus, with a more complex hardware setup required, the proposed two-stage solutions are less attractive than the single-stage. Therefore, in this thesis, we assume that optimizing a single-stage converter with an appropriate topology is more integrated, reliable and efficient than a 2-stage configuration.

11.3.5. Multi-level Topologies

To improve the conversion of high power applications, serial and parallel multilevel converters are used to get significant gains on reactive elements and transformer sizing. However, an optimum on the cell number is often found arbitrarily. Therefore, this concept has to be generalized thanks to analytical definitions of our considered topologies [35].

- The ***Parallel interleaving*** divides the total power of a converter into several lower ones. It has a big interest in high current applications. It is achieved by parallel elementary cells (**Figure 160**), whose nominal equations are modified by a parallel factor (Table 31). Thus, the cell voltage is still equal to the source, while the global power and capacitors values decrease. Nevertheless, the total volume of inductors and transformers are unchanged while the number of components increases.

- The ***Serial interleaving*** separates the voltage into equal parts of same value. That has a big interest in high voltage applications (**Figure 160**). The voltage is divided by the number of serial elementary cells, as represented by a serial factor (Table 31). The voltage stress and power reduction on switches and transformer allow to choose switches with smaller rating and that possess better performance, which affect the total volume of inductors and transformers. However, the main disadvantages are the increased number of components, especially capacitors, in order to ensure the proper functioning. As a result, it directly impacts the volume and weight of the converter.

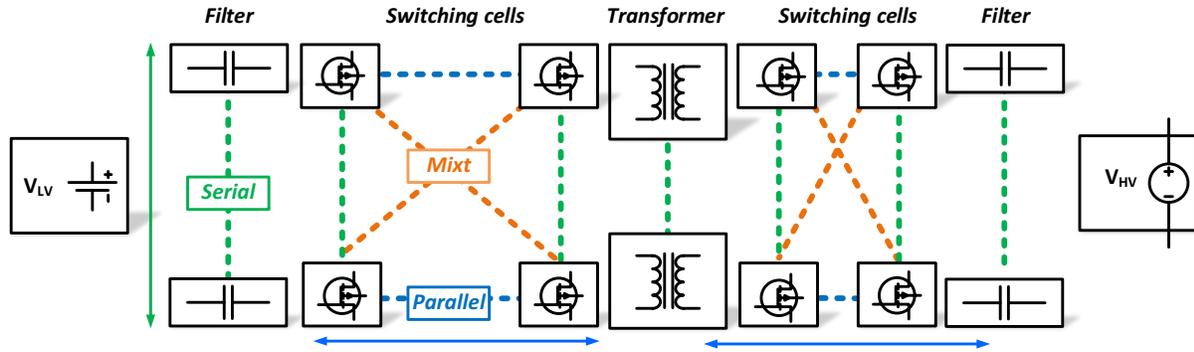


Figure 186: Main Properties of Serial and Parallel Interleaving

- The **Serial/Parallel or Mixt Interleaving** can occur when a large voltage difference between the LV and HV sides is required in high power converter (**Figure 160**). Indeed, the advantages of interleaving can highly improve the conversion efficiency, but it requires finding the optimum number of cells for each configuration. However, in order to ensure proper operation, the number of elementary cells on both sides must be equal: $N_{CellSerLV} N_{CellParLV} = N_{CellSerHV} N_{CellParHV}$.

	SERIAL	PARALLEL
V_{HV}	$V_{HVCell} = \frac{V_{HV}}{N_{ser}}$	$V_{HVCell} = V_{HV}$
V_{LV}	$V_{LVCell} = \frac{V_{LV}}{N_{ser}}$	$V_{LVCell} = V_{LV}$
Power	$P_{cell} = \frac{P}{N_{ser}}$	$P_{cell} = \frac{P}{N_{par}}$
Inductor	$N_{Induc} = 2N_{CellSer}$	$N_{Induc} = N_{CellPar} \times N_{Lcell}$
C_{LV}	$N_{CLV} = N_{LVCellLV}$	C_{LV}
C_{LV}	$N_{CHV} = N_{LVCellHV}$	C_{LV}
Switch _{LV}	$N_{MosLV} = N_{LVCellSer} \times N_{mosLVCell}$	$N_{MosLV} = N_{LVCellPar} \times N_{mosLVCell}$
Switch _{HV}	$N_{MosHV} = N_{HVCellSer} \times N_{mosHVCell}$	$N_{MosHV} = N_{HVCellPar} \times N_{mosHVCell}$
Transformer	$N_{Trasfo} = N_{CellSer}$	$N_{Trasfo} = N_{CellP}$

Table 31: Main Properties of Serial and Parallel Interleaving

To conclude on the BBCU study case, we logically expect a parallel interleaving on the LV side (high current). For the HV part (low current), it is less obvious. Indeed, it would be quite interesting to make a serial interleaving to reduce the switches voltage rating, while decreasing the power of each elementary converter. However, parallel interleaving would also reduce the elementary power dedicated to each sub converter while maintaining a reasonable number of capacitors. Thus, a series-parallel association is possible but need to be optimized to define the best optimum.

12. Annexe 5 – Prototypes Review

In recent years, several prototypes like the BBCU converter have appeared in the industry and literature. A comparison with our optimal design is interesting to conclude about the feasibility of the BBCU application, but also on our optimal sizing methodology. A global comparative table is proposed with the available data we have.

12.1.1. Industrial Converters

a. Airbus BBCU prototype – Gen 1 (2015)

This section presents the complete design of the first BBCU converter. This Airbus prototype has been developed in a research activity to demonstrate the feasibility of this concept in the new electrical architecture of the MEA. The work started in 2013 with the aim to optimize individually the different embedded technologies. We have already presented a part of this work in [1]. The first BBCU generation is based on a 2-stage architecture, with a buck-boost topology combined to a push-pull converter. The active part is composed of low profile power modules integrating last generation of high speed Mosfet & IGBT (42 dies) and passive components. The inductors use new materials allowing a reduction of 50% of the form factor compared to classical material and for equivalent performance. Planar transformers carry out the isolation, and the bus bar technology has been used to integrate stacked capacitors. The cooling is realized thanks to a water cold plate, specially designed for the mechanical package. This first prototype was achieved in 2015. It respects all the standards, is compliant to the different aeronautic challenges (electrical, EMC, mechanical, thermal) and complies with an aircraft mission profile requiring a suitable control. This first prototype had been tested in an aircraft bench, meaning that the concept is totally demonstrated with a high maturity (Technology Readiness Level (TRL) 5)), proving the possibility of implementation in future Airbus programs. The key information of this converter are a weight of 25kg for 12kW. It means a power density of 0,5 kW/kg with an efficiency of 85% (Figure 187), whose weight repartition is expressed below.

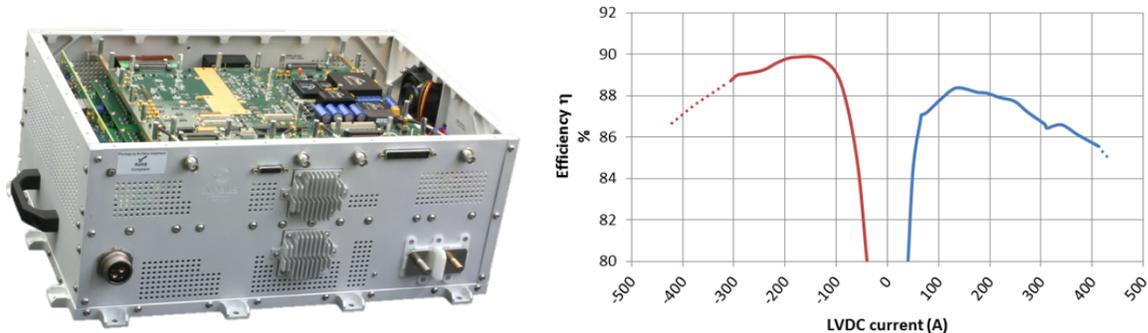


Figure 187: BBCU v1.0 picture with its efficiency curve as a function of operation modes

b. Automotive: BRUSA BSC618-24V (2015)

An automotive bidirectional converter close to the BBCU specification can be found from BRUSA [225]. It covers a large HV range (400 – 900 VDC), for a LV value equals to 24V and a power of 3kW. The BSC618-24V is based on a 2-stage architecture with a transformer stage working in a serial-resonant manner. In addition, two buck-boost converters work in a geared mode to reduce output ripples. The resonant topology realizes a current zero-crossing switching (ZCS), and an auto-commutation of the buck-boost converter is achieved (soft commuting of the bridge point). Therefore, losses can be limited to a minimum. Normally, due to the significantly slow changes of current and voltage, EMC faults are reduced in comparison with hard-switching topologies. The water-cooling is used in this converter and mechanics ensure a compact, light and vibration-resistant construction for mobile usage. Very high power and efficiency levels are reached (Figure 188). However, we have no idea of the considered constraints for this prototype, in terms of environment and EMC (certainly automotive and not aeronautics). It can explain some differences of design efficiency with the BBCU.

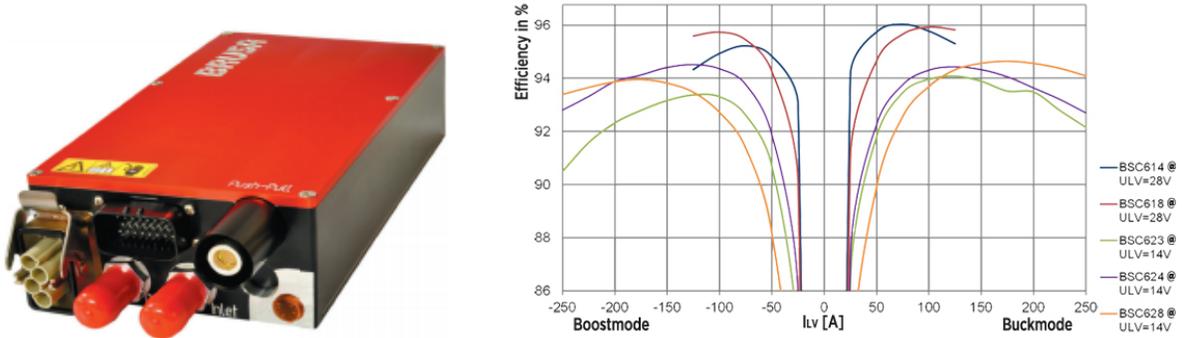


Figure 188: BRUSA BSC618-24V picture with its efficiency curve as a function of operation modes

12.1.2. Research Laboratory Converters

a. Laplace prototype (2015)

A DC-DC converter prototype was developed under the "MOET" project in the Laplace Laboratory. This converter answers to a specification equivalent to a 10 kW BBCU. The topology is based on a bi-directional push-pull converter [182] and possesses eight parallel switching cells. It contains GaN (LV side) and SiC (HV side) semiconductors, with a GaN energy recovery system. The cooling system is based on a forced-air heatsink with straight-fins. The inductive filtering is integrated inside coupled transformers, to gain in integration. The final prototype is shown in Figure 189. However, it should be noted that the model has a 13% saturation imbalance, which caused problems during the converter operation. In addition, filter cuts below the required frequency imposed by the EMC standard (20dB μ V of difference). Finally, an efficiency up to 92% can be achieved (Figure 189).

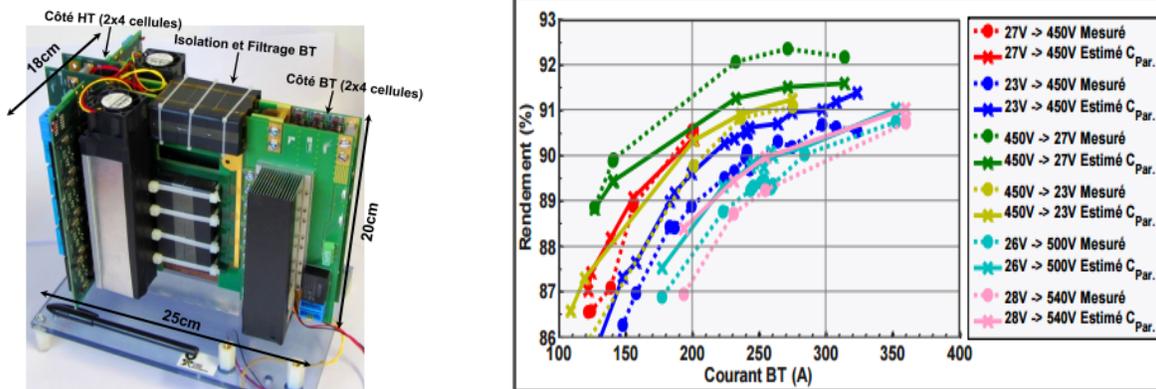


Figure 189: Laplace prototype picture with its efficiency curve as a function of operation modes

b. IES prototype – 3kW (2015)

A 3kW brick of DC/DC converter was developed by the IES laboratory for the "ETHAER" project and was already described in 5.2.2.f.

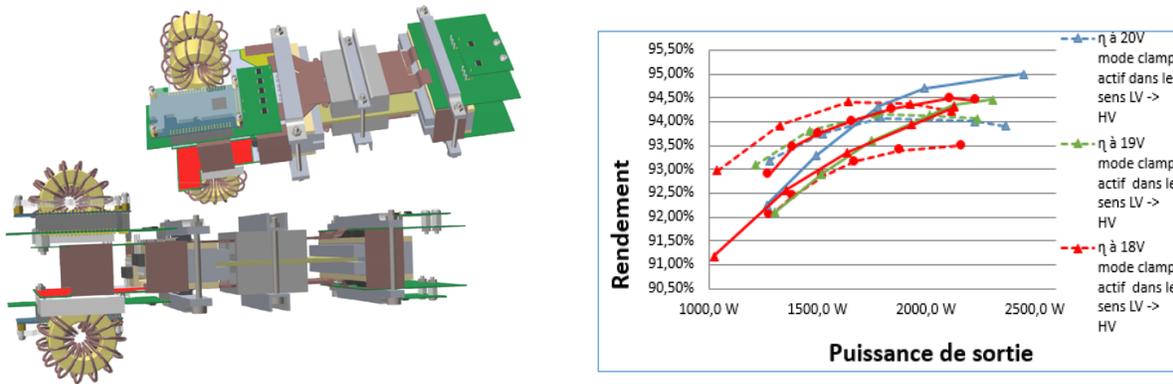


Figure 190: IES prototype picture with its efficiency curve as a function of operation modes

12.1.3. Summary of the prototypes and comparison

To compare the different solutions, we have just extrapolated some “integration” values thanks to precise measurements realized on the first BBCU converter. About the 10kW Laplace prototype, we performed a simple proportionality rule to consider a 12kW conversion. Thus, from the same basis, we can now perform an analysis on the different solutions and parts of a converter to realize a new version of the BBCU. Some data are still unavailable at the time of the writing of this memoir.

Annexe 5 – Prototypes Review

Elements/Proto		Airbus		Laplace		IES		BRUSA		Optimization	
		12kW		12kW		12kW		12kW		12kW	
		%	Kg	%	Kg	%	Kg	%	Kg	%	Kg
Measured Weight		-	-	-	5,16			100	19.4		
Electrical	HV	21	5,24	20	1,03						
	LV			5	0.26						
	Low level	9,5	2,33	-	-						
	Magnetics	-	-	42	2,17						
Cooling	HV			18	0,93						
	LV	14,4	3,53	13	0,67						
Mechanics	Packaging	28,1	6,89	-	1,45						
	Bus Bar & PCB	27	6,54	-	1,39						
	Screw	-	-	3	0,15						
Real Industrial Weight		-	24,5	-	8			-	19,4		
Ext. power Density (kW/kg)		0,49		1,5				0,61			
Total volume (L)		-		9				12,6			
Ext. power Density (kW/L)		-		1,32				0,95			
Efficiency		85%		92%				95%			

13. Synthèse en Français

Méthodologie de dimensionnement des convertisseurs statiques - Application à un contexte aéronautique

15.1 Chapitre 1: Contexte de la thèse

L'électronique de puissance est un domaine technique et scientifique dont le but est de convertir la puissance électrique d'une forme à une autre. Pour réaliser cette opération, on conçoit des convertisseurs statiques qui sont connectés à une ou plusieurs sources prédéfinies. Ces convertisseurs doivent ensuite fournir une puissance électrique traitée et adaptée, selon un cahier des charges précis et exigeant, mais aussi être immunisé aux perturbations comme des stress CEM ou thermiques (Figure 191).

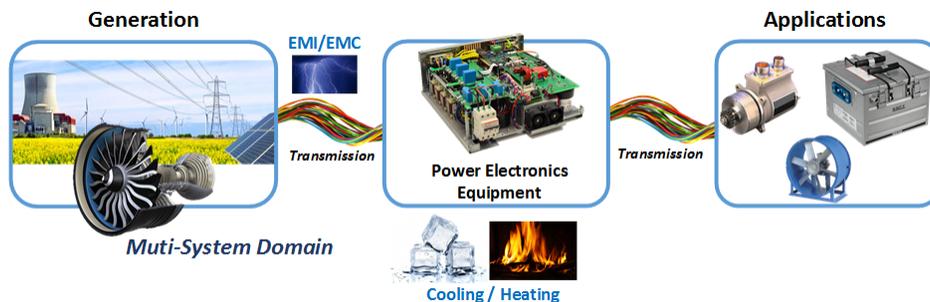


Figure 191: Schéma de principe de l'Electronique de Puissance

Aujourd'hui, les méthodes communes utilisées pour concevoir ces convertisseurs, sont des études préliminaires locales (avec plus ou moins d'hypothèses et d'approximations sur chacun des composants), l'essai/erreur (que l'on cherche à éviter en des solutions viables dès la première itération) ou encore leurs propres expériences. Or, de plus en plus d'outils et de logiciels sont disponibles sur le marché pour minimiser les cycles de conception avant l'obtention d'un produit final performant. Mais aucun d'entre eux n'est encore assez performant pour identifier directement la meilleure topologie, ou dimensionner de façon optimale un composant de puissance via sa technologie ou ses matériaux.

Cependant, nous pouvons faire le constat que ce concept d'optimisation existe depuis plusieurs décennies dans d'autres domaines comme la mécanique, les machines électriques ou la micro-électronique par exemple. On appelle cela 'design préliminaire' ou 'conception optimale', et cela fait globalement partie du domaine de la conception assistée par ordinateur (CAO). Par conséquent le but de cette thèse est de proposer une méthodologie afin de réaliser l'optimisation d'équipements et de dispositifs en électronique de puissance. De plus, cette méthodologie aura à intégrer les contraintes

et exigences du domaine aéronautique, dans le but de répondre aux futures problématique liées au systèmes embarqués dans les futurs avions, tel que le 'More Electrique Aircraft' ou avion plus électrique.

15.1.1 L'Avion Plus Electrique (MEA)

Dans les dernière décennies, d'importantes étapes ont été franchies tendant vers un avion plus électrique (MEA), particulièrement avec la forte croissance du rôle de l'énergie électrique embarquée dans les avions. De nos jours, cette évolution semble majeure pour le futur du transport aérien, et est identifiée comme la prochaine étape clé pour des avions plus économiques et écologiques. Actuellement, quatre vecteurs secondaires d'énergie dédiés à la servitude sont utilisés dans les avions : mécanique, hydraulique, électrique et pneumatique, principalement obtenus par les réacteurs de propulsion. Le MEA a pour but de remplacer ces énergies hydrauliques et pneumatiques par des systèmes électriques, que l'on appelle respectivement des architectures « Hydraulicless » ou « Bleedless », réduisant le poids global des systèmes et offrant une maintenance facilitée par exemple. Cependant, pour arriver à de telles architectures, cela nécessite un travail avancé sur les différents systèmes électriques et équipements d'électronique de puissance, présents partout dans l'avion (Figure 192). Ainsi, le but de cette thèse est de fournir des outils et un environnement permettant d'optimiser ces systèmes.

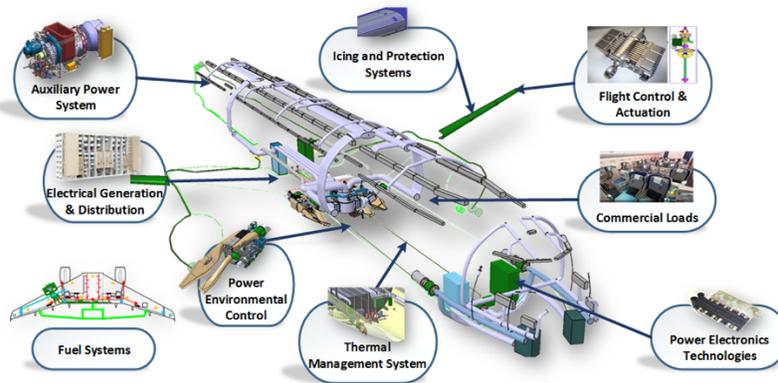


Figure 192: Opportunités de l'Electronique de puissance dans différents systèmes embarqués

15.1.2 La conception assistée par ordinateur en électronique de puissance

Pour faire face à ces nouveaux challenges, des outils spécifiques d'aide à la conception permettant un design plus efficace et rapide de convertisseurs de puissance sont nécessaires et requièrent un travail sur deux niveaux :

- **Modèles multi-physiques au niveau du composant**, décrivant les différentes interactions entre les composants d'un convertisseur.

- **Formulation et outils au niveau du convertisseur**, pour décrire les interactions entre les composants (solveurs), et l'évolution de la performance (poids, rendement, etc.) en fonction des paramètres.

Dans le but de mesurer les besoins de conception actuels des convertisseurs statiques, nous pouvons utiliser de nombreux indices de performances qui seront aussi les objectifs de nos optimisations, tels que: **Densité de Puissance** [kW/dm^3], **Puissance par unité de poids** [kW/kg], **Cout relatif** [$\text{kW}/\text{\$}$] or [$\text{kW}/\text{€}$], **Pertes Relatives** [%], **Taux de panne** [h^{-1}], **Impacts environnementaux**, pour le métal [$\text{Kg}_{\text{material}}/\text{kW}$] ou le silicium [$\text{cm}_{\text{Si}}/\text{kW}$].

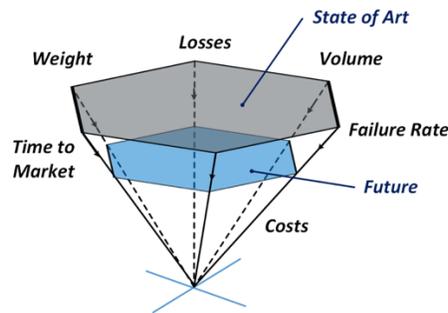


Figure 193: Actuelles et futures exigences en Electronique de Puissance, extrait de [17]

Pour atteindre ces performances, une transition de “digitalisation” s’effectue dans les laboratoires et industries en électronique de puissance, consistant à passer d’un travail de conception dit de “prototypage hardware” vers 2010, à la modélisation et simulation multi-physique aux alentours de 2020. Cette digitalisation a pour but de fournir des logiciels qui amélioreront les performances des convertisseurs de n’importe quelle type (DC/DC, DC/AC...), avec comme fonctionnalités principales: **Optimisation de la conception**, **Librairies de modèles multi-physiques**, **Vérification à posteriori**, **Simulation allant du composant, à l’équipement voire même jusqu’au système**, **Big Data et bases de données**, **Rendement de l’outil en terme de temps/précision**.

De plus, les degrés de liberté que l’utilisateur doit avoir à disposition (ou le logiciel ?), dans ce type de logiciel peuvent être résumés grâce à ces « objets » : **Composants**, **Topologies**, **Modulation et Contrôle**, **Procédure de Design**, **Modules/Normes/Economie**, **Industrialisation**, **Applications Nouvelles/Spécifiques**.

Avec cette digitalisation du processus de conception, plusieurs domaines scientifiques et de l’ingénierie deviennent corrélés. Par exemple pour une optimisation multi-objectifs, nous avons besoin d’une expertise en informatique, mathématiques et génie électrique. De plus de nombreuses physiques sont considérées durant la création des modèles d’objets utilisés en électronique de puissance : **Electrique**, **Magnétique**, **Thermique**, **Mécanique**, **Fluidique**, **Economique**

Finalement, nous pouvons aussi exprimer dans un jargon « électrique » nos attentes principales à résoudre dans le cadre du pré-dimensionnement d’un convertisseur : **Quel matériel**, **technologie**

et géométrie doit être utilisée pour construire les composants ? Quel est la meilleure topologie de conversion ? Faut-il utiliser une structure de conversion multiniveaux ? A quelle fréquence de découpage ? Comment concevoir les filtres ? Est-ce que mon résultat est global ou y a-t-il une meilleure façon de le faire ? etc. Ainsi, nous pouvons regrouper toutes ces questions et besoins dans 3 axes principaux, énumérés dans la section suivante.

15.1.3 Vecteurs d'amélioration en Electronique de puissance

Trois vecteurs d'amélioration principaux en électronique de puissance ont été identifié dans le projet ETHAER, présenté au début de ce manuscrit. Cette thèse fait partie de ce projet, et nous avons traités deux de ces problématiques à intégrer dans un outil de pré-dimensionnement. La liste des axes d'amélioration en électronique de puissance, classée par les projets de recherche et laboratoires partenaires peut être dressée ainsi :

- **Evaluation des opportunités actuelles et future en électronique de puissance**, comme les nouveaux composants et technologies (Cette thèse, Laboratoire Laplace Toulouse/Airbus Operations SAS)
- **Comparaison de topologies**, et possibles améliorations comme des circuits d'aide à la commutation (Cette thèse & Laboratoire IES Montpellier [35])
- **Emergence de technique d'intégration et leurs simulations** (Laboratoires GEEPS (Paris) & Ampère (Lyon) [36] [37])

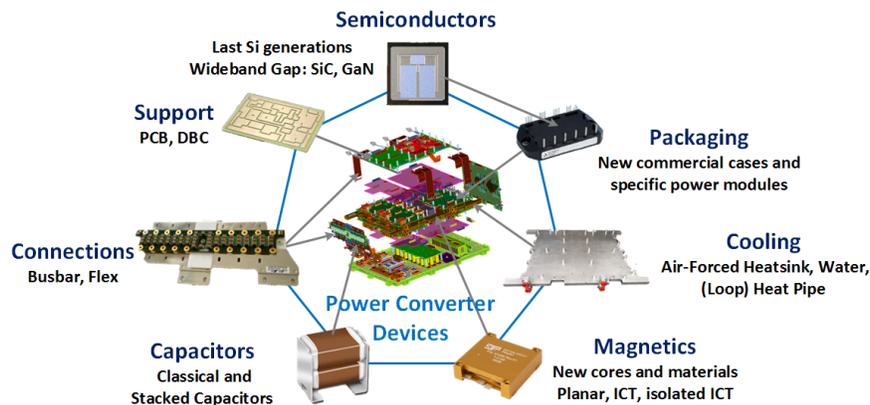


Figure 194: Actuelles et futures technologies en Electronique de Puissance à insérer dans l'outil de dimensionnement et d'optimisation

15.2 Chapitre 2: Méthodologie de design optimal

Le design optimal et assisté par ordinateur en électronique de puissance est un problème aussi vieux que la discipline. Mais le prototypage virtuel est moins avancé en Electronique de Puissance que dans d'autres domaines comme la mécanique ou les machines électriques. Parmi de nombreuses

topologies (de multiples architectures de convertisseurs) et technologies (diversité de composant et matériaux), le choix optimal d'une structure de conversion dédiée à un cahier des charges reste un exercice difficile. C'est pourquoi, résoudre les problèmes physiques grâce un algorithme d'optimisation est important pour prendre des décisions plus facilement et analyser les systèmes physiques plus en profondeur. Le but ici est finalement de trouver une valeur minimale (ou maximale) d'une fonction mathématique parmi un ensemble de solutions possibles, répondant à certaines conditions et contraintes. Ainsi ce chapitre a pour mission de présenter les stratégies et méthodologies pour créer une plateforme d'optimisation dédiée à l'électronique de puissance.

15.2.1 Architecture des modèles

Pour créer une organisation hiérarchique des éléments composant un convertisseur, nous avons utilisé la programmation dite 'orientée objet' (OOP). Les éléments de plus hauts niveaux sont des *convertisseurs*, utilisant des *topologies* qui rassemblent plusieurs *composants*. Trois objets ont été identifiés en tant que topologie :

Topologie active, étant la cellule de commutation essentiellement composée de composants à semi-conducteurs ; **Topologie Passive**, étant les filtres ; et la **Topologie Cooling**, qui est là pour refroidir les pertes dans les deux topologies précédentes. En dessous de ces topologies, nous retrouvons les composants de puissance, eux-mêmes constitués de matériaux définis et caractérisés dans nos bases de données. La hiérarchie complète est présentée dans la Figure 195.

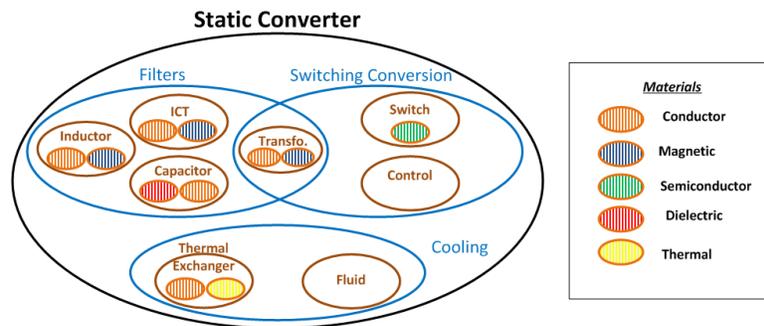


Figure 195: Architecture globale des modèles multi-physiques

Ainsi grâce à cette hiérarchisation (Figure 195), une bibliothèque complète de modèle multi-physiques a été créée pour l'ensemble des composants et topologies définies précédemment (Figure 196).

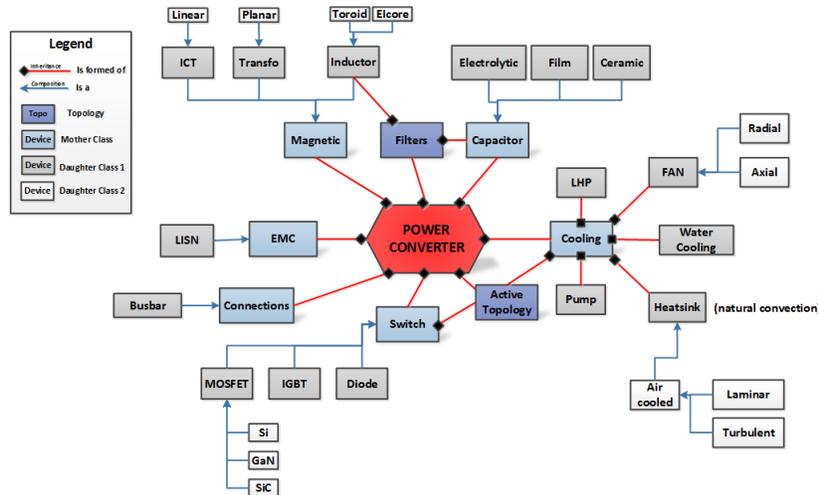


Figure 196: Vue d'ensemble de notre bibliothèque complète de modèles multi-physiques

Différentes techniques existent en optimisation, et trois notions principales sont utilisés pour les caractériser : **variables**, **objectifs** et **contraintes**.

Dans cette thèse nous proposons d'utiliser des **variables continues**, et donc de créer des modèles multi-physiques continus de composants et topologies (Figure 197), afin d'utiliser des algorithmes déterministes, censés être plus simple à utiliser que leurs concurrents, les heuristiques. Cela est censé faciliter la convergence de nos résultats. Au niveau des objectifs, nous utiliserons du **mono et multi-objectifs** afin de répondre aux indices de performance présentés dans le chapitre 1. De plus nous proposons des techniques avancées de multi-objectifs, telles que des études de sensibilités ou des fronts de Pareto. Au niveau des **contraintes**, elles seront essentiellement liées à la **physique du composant**, telles que sa température maximale avant destruction, ou encore issues de **normes** et du **cahier des charges** lui-même.

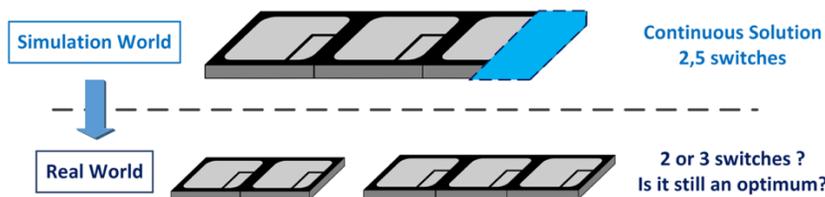


Figure 197: Un challenge de notre formalisme utilisant des variables continues pour nos modèle multi-physiques de composants: la transition entre les résultats optimisés continus et le monde réel discret

Pour réaliser la modélisation continue de nos composants, nous utiliserons une méthode dite de **modélisation directe**. Son avantage est de décrire un composant comme dans le monde réel, couche par couche, à partir de sa géométrie, forme et matériaux (Figure 198). Grâce à ces trois entrées dans le modèle, il est très facile d'obtenir une solution unique des objectifs à atteindre en électronique de puissance à travers une optimisation, tel que le poids, volume, coût etc. ; Mais aussi d'établir les modèles multi physiques du composant (électrique, thermique, etc.), en calculant des valeurs élémentaires de divers éléments physiques (résistances, capacitances, reluctance etc.).

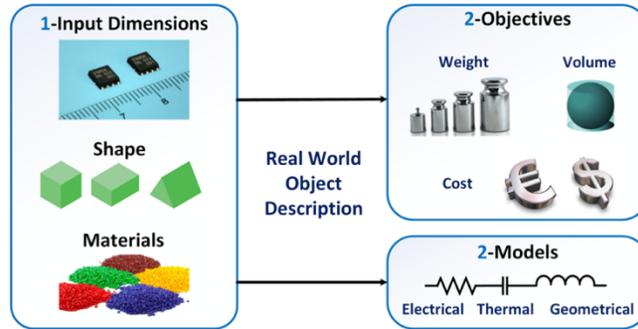


Figure 198: Principe de la modélisation dite “Directe”

De plus, dans notre librairie de composants, nous proposons à l'utilisateur de choisir entre plusieurs modèles, afin qu'il choisisse la façon de traiter le problème et le temps/précision qu'il veut y investir. On propose une hiérarchie de trois niveaux, à partir de modèles rapides mais grossier en terme de précision ; jusqu'à des modèles très rigoureux et fiables, mais plus long à calculer. De plus, cette granularité intègre une notion de « physique des composants », via un classement des technologies/matériaux existant sur le marché. Par exemple, les modèles simples englobent un maximum de technologie/matériaux afin d'avoir un modèle « généraliste » mais peu précis, jusqu'à une technologie/matériaux très précis pour les modèles de forte précision. Ces 3 niveaux (Figure 199) seront appelés **niveaux Système, Convertisseur et Composants**.

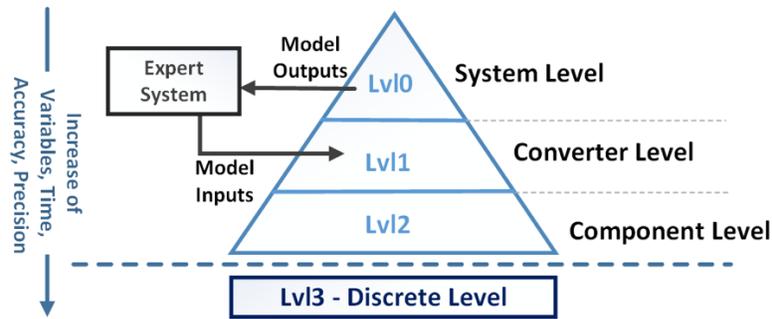


Figure 199: Hiérarchie de la granularité présente dans notre bibliothèque de modèles multi-physiques

15.2.2 Solveurs Electriques

Les précédentes sections de ce chapitre ont montrées comment créer une stratégie pour les modèle multi-physiques de composants. Maintenant nous devons nous pencher sur la façon de résoudre les modèles nodaux, principalement électriques et plus précisément les topologies actives réalisant l'opération de découpage dans les convertisseurs à l'aide de solveurs dédiés. Pour cela, nous avons identifié deux types de solveur électrique.

Les premiers réalisent une simulation directe et globale du circuit du convertisseur, incluant les filtres si besoin ; et de type temporels ou fréquentiels. Dans cette thèse nous avons favorisé un solveur fréquentiel issu du laboratoire Laplace, appelé Ootee, spécialement développé pour obtenir

des résultats acceptables en un minimum de temps en utilisant une représentation simplifiée de la cellule de commutation.

Cependant, ce solveur fréquentiel ne prend en compte que des topologies basiques de type DC/AC ou DC/DC non isolé. Pour combler ce manque sur les topologies DC/DC isolées, nous avons décidé d'utiliser dans un deuxième temps une approche analytique pour les topologies actives, et continue si possible, afin de coller à notre stratégie initiale d'optimisation. Cette partie analytique a ensuite été couplée au solveur de 1^{er} type (temporel/fréquentiel), notamment pour dimensionner la partie filtrage. En effet, le solveur fréquentiel se prête bien à l'évaluation du respect des normes, souvent exprimées dans le domaine fréquentiel. Ainsi, ce couplage « hybride » permet de garder une flexibilité sur la définition filtrage, mais avec une partie fixe sur la topologie active analytique. Finalement, une bibliothèque de topologie active analytique a été créée et validée (Figure 200).

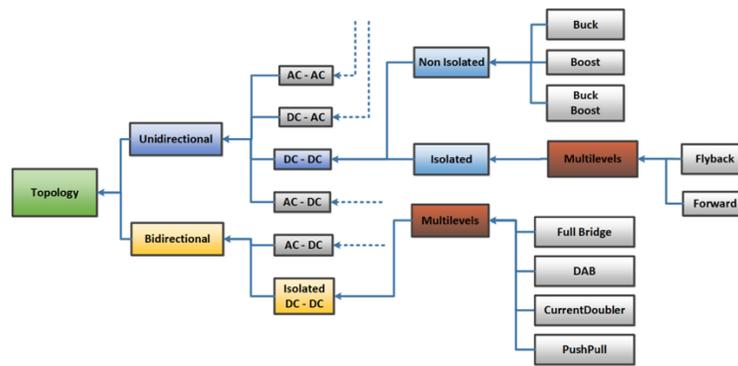


Figure 200: Hiérarchie de la bibliothèque des topologies actives analytiques

15.2.3 Développement informatique & Interface graphique

De nombreuses fonctions de développement informatiques ont été créées afin de faire communiquer l'ensemble des objets nécessaires à la plateforme d'optimisation, comme principalement des fonctions de communication entre les solveurs, modèles multi-physique, optimiseur et les interfaces avec l'utilisateur et les librairies. Cela a représenté beaucoup de travail, mais ne sera pas présenté dans cette thèse par manque d'intérêt "scientifique". Elles seront juste énumérées afin de présenter un plan global du travail réalisé.

De plus, pour faciliter la prise en main de la plateforme pour un utilisateur lambda, nous avons créé une interface graphique facilitant l'initialisation et la mise en place de problèmes d'optimisation sur des composants et topologies en électronique de puissance (Figure 201). Cette interface permet de visualiser toutes les possibilités de l'outil et des modèles/solveurs, mais aussi de gagner en flexibilité lors de l'étude de problèmes préliminaires et optimaux sur un convertisseur statique ou sur les éléments le constituant. Cette approche a aussi été étendue à la gestion de nos bases de données de composants, afin de créer des modèles multi-physiques continus par exemple.

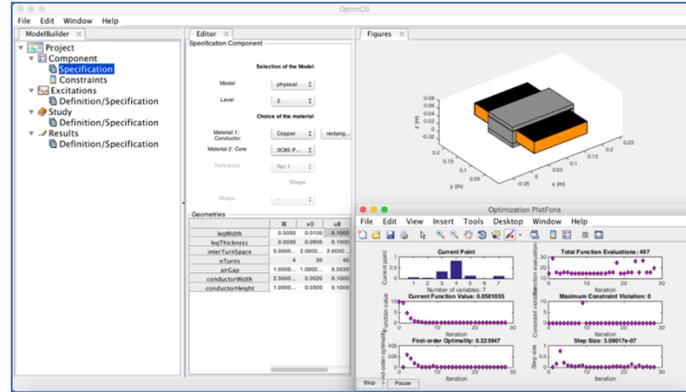


Figure 201: Interface graphique proposée pour la conception optimale en Electronique de Puissance

15.3 Chapitre 3: Modèles simplifiés des composants actifs

Les composants actifs sont représentés par deux dispositifs : les composants à semi-conducteurs et les moyens de refroidissement, qui sont dans notre cas les dissipateurs.

15.3.1 Semi-conducteurs

Le but principal de ce chapitre est d'évaluer les pertes par conduction et commutation des composants à semi-conducteurs qui influencent fortement la conception d'un convertisseur statique. Combiné avec la fréquence de découpage, les modèles de perte gouvernent le compromis entre le poids du filtre et celui du dissipateur. De plus, les pertes du semi-conducteur sont généralement dominantes, et donc affectent grandement le rendement du convertisseur. Pour toutes ces raisons, le modèle de pertes du semi-conducteur est un point central dans la conception d'un équipement de puissance, notamment pour préciser les pertes générées à une fréquence spécifique d'un point de fonctionnement.

Le second objectif de ce chapitre est de fournir les modèles aidant le concepteur à sélectionner le bon composant lors d'une étape préliminaire. Ceci est particulièrement utile pour de la conversion multicellulaire : des composants avec des calibres en tension et courant plus petits que ceux de la cellule de commutation deviennent admissibles, et cela augmente considérablement le nombre de modèles à étudier (Figure 202). Une solution dite 'force brute' serait de tester une conception avec chacun des semi-conducteurs présents dans une base de données et sélectionner la meilleure solution à la fin de ce balayage.

Chapitre 3: Modèles simplifiés des composants actifs

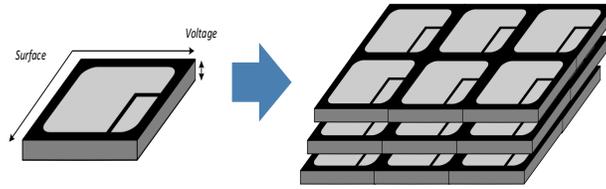


Figure 202: Illustration du modèle continu de composant à semi-conducteur

Finalement, le modèle de « semi-conducteur continu » que nous essayons de développer dans la deuxième partie de ce chapitre serait, dans sa version ultime, un modèle avec des entrées limitées (point de fonctionnement de la tension et du courant du dispositif, par exemple) et calculerait les pertes obtenues avec le meilleur composant existant avec ces entrées. En fonction de la tension et de courant sélectionné, le meilleur dispositif serait un IGBT ou MOSFET par exemple, et ce modèle pourrait aider un concepteur inexpérimenté à choisir la bonne technologie pour son application. De plus, nous définirions différents niveaux de granularité, comme expliqué dans le chapitre 2, suivant une logique technologique, permettant étape par étape de définir la meilleure technologie en un minimum de temps, tout en maximisant la précision des modèles (Figure 204)

Dans une version moins ambitieuse, nous pourrions avoir différents modèles pour différentes classes ou technologies (MOSFET, MOSFET super-jonction, IGBT et IGCT par exemple), et ces modèles pourraient être utilisés pour tenir compte de l'influence du nombre de cellules en série et en parallèle. Pour éviter le processus de conception de force brute décrite précédemment, ces modèles pourraient être aussi utilisés dans une routine d'optimisation afin que la meilleure tension et le meilleur courant se calcule automatiquement ; le même processus pourrait également indiquer quelle topologie doit être utilisée (nombre de cellules en série et parallèle). Nous pouvons voir dans la Figure 204 des illustrations des modèles continus et de commutation abordée dans cette thèse.

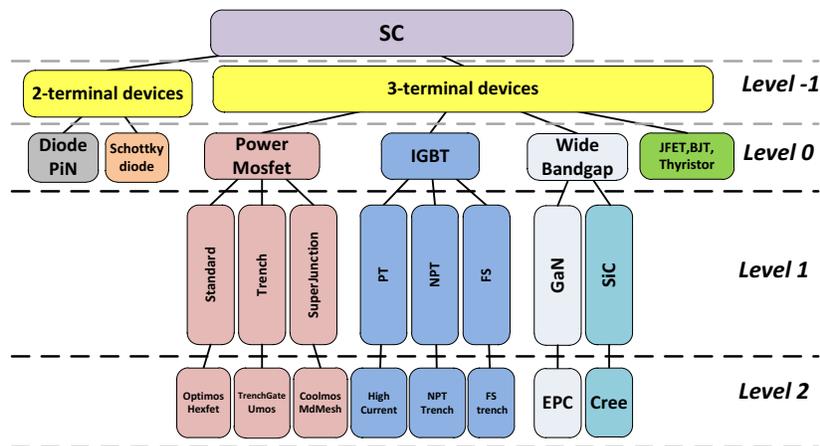


Figure 203: Granularité technologique pour les modèles de composant à semi-conducteur

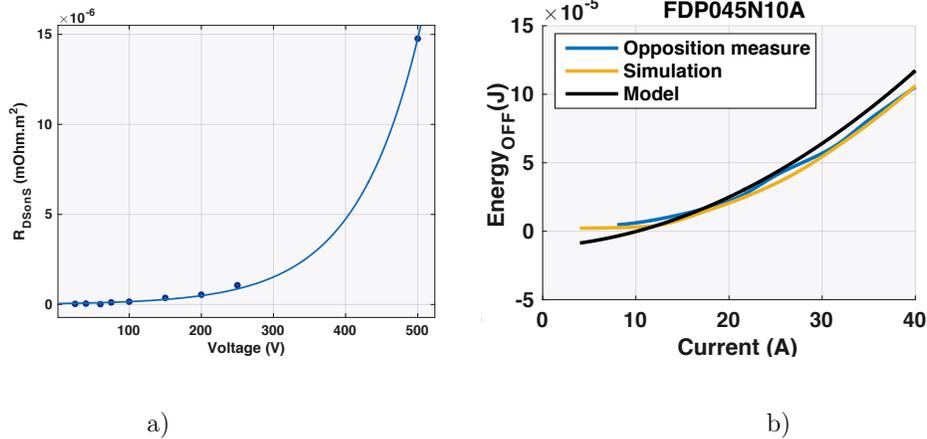


Figure 204: Modèles de pertes continus étudiés dans cette thèse

a) Modèle analytique de résistance surfacique en fonction du calibre en tension (Mosfet Hexfet) – b) Modèles de pertes par commutation (mesures par opposition, simulations détaillées AMIGO, modèle analytique de cette thèse)

Cependant, les variables discrètes sont difficiles à manipuler dans des routines d'optimisation, de sorte qu'un tel modèle doit être effectué en continu. Par exemple, la tension nominale d'un IGBT ne doit pas être seulement 600V ou 1200V ou 1700V ; toutes valeurs intermédiaires devraient être autorisées de sorte que la routine puisse glisser d'une valeur à l'autre dans le même cycle d'optimisation.

15.3.2 Dissipateurs

Comme évoqué précédemment, les pertes dans un convertisseur statique sont principalement générées par les composants à semi-conducteurs. Cela a deux conséquences : ces composants définissent en grande partie le rendement du ; de plus, ces composants génèrent un échauffement local important. Ainsi, ces pertes doivent être transportées et évacuées par un dispositif de refroidissement pour maintenir une température acceptable dans le système et éviter des dommages thermiques. Ce chapitre a donc pour but de concevoir des composants « de refroidissement et d'évacuation thermique » ; ils constituent une part significative de la masse du convertisseur et nécessitent d'être judicieusement choisis et optimisés.

Dans la majorité des cas, les systèmes de refroidissement n'agissent directement que sur les semi-conducteurs, mais ils peuvent également être utilisés pour refroidir d'autres éléments tels que les composants magnétiques. En outre, de nombreuses solutions sont disponibles pour refroidir un convertisseur, en fonction de la quantité de chaleur à évacuer, du domaine d'utilisation (industrie, aéronautique, domestique, etc.) ou du cahier des charges. Lorsque c'est possible, on se contente généralement d'un dissipateur à ailettes (Figure 205), mais si c'est nécessaire, en particulier pour les fortes puissances, nous avons recours au refroidissement liquide. Mais, avec l'augmentation des densités de puissance des convertisseurs statiques, ces pertes peuvent être de plus en plus concentrées ; de nouveaux dispositifs sont alors nécessaires et on a parfois recours à des boucles

diphases. Par conséquent, il est important d'obtenir une modélisation précise de ces différents dispositifs de refroidissement, afin de choisir les meilleurs, pour finalement améliorer la densité de puissance du système.

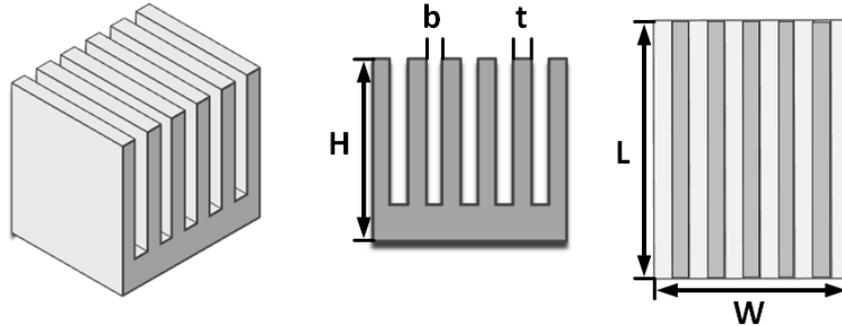


Figure 205: Géométrie d'un dissipateur à ailettes droites

Tout d'abord, nous présentons dans ce chapitre les différentes technologies de refroidissement appliquées à l'électronique de puissance, et détaillons leurs limites dans le contexte aéronautique. Le principe et la formulation du modèle thermique d'un système de refroidissement sont exposés, avec un critère de comparaison (FOM) pour évaluer les performances du système et mieux le sélectionner dans une base de données. En outre, la méthode est aussi créée pour une ou plusieurs sources de chaleur, comme présenté dans la Figure 206 pour une ou deux puces sur une même plaque froide.

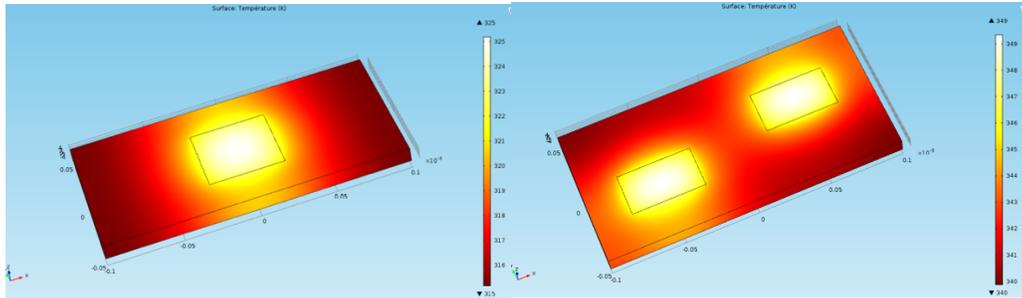


Figure 206: Simulations numériques COMSOL d'une et deux sources chaudes sur une base plane afin de calculer une résistance de « diffusion de chaleur (cf. Anne Castelan work)

Ensuite, les détails des modèles multi-physiques d'un dissipateur thermique à ailettes droites sont fournis, en convection naturelle et air forcé. Certaines granularités sont créées pour définir les différents niveaux de modèles, à partir d'une définition géométrique globale du dispositif (via un son volume par exemple), jusqu'à la modélisation précise de ses différentes parties, à savoir une base plane et un réseau d'ailettes (Figure 207).

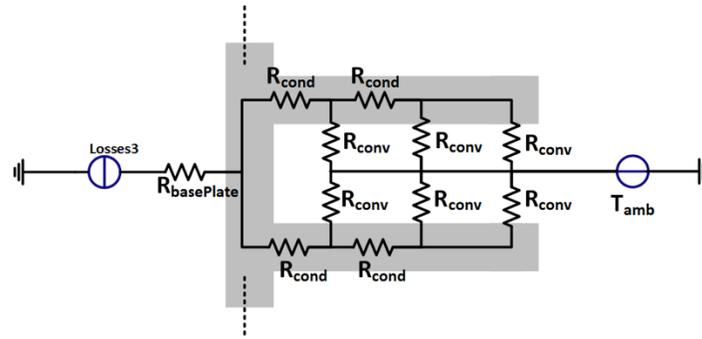


Figure 207: Exemple d'un modèle thermique de notre dissipateur à ailettes droites

Pour finir, quelques validations des différents modèles thermiques, mécanique et aérauliques ont été menées sur ces différents modèles, grâce à des tests empiriques, et des simulations numériques (Figure 208), avant de conclure sur ces travaux de modélisation et leur validité dans une plateforme d'optimisation.

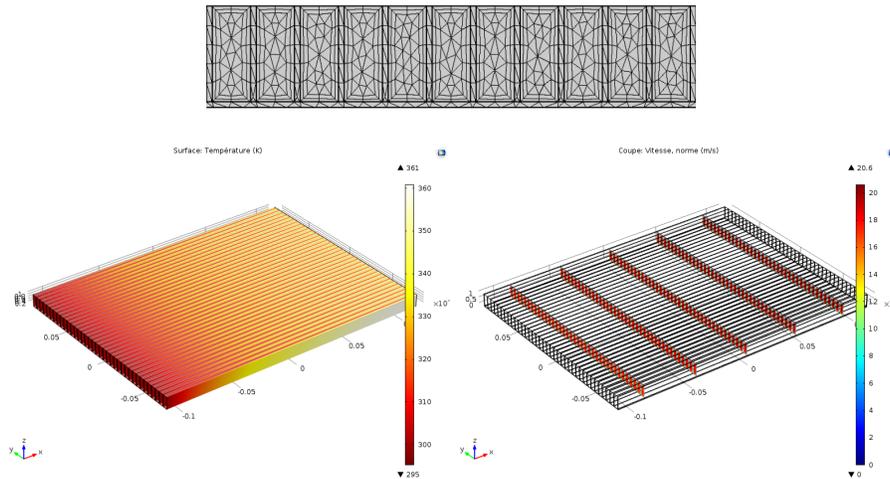


Figure 208 : Validations numériques des modèles thermiques et de chute de pression sur un dimensionnement de dissipateur

Pour information, d'autres modèles dit "secondaires" sont aussi fournis dans ce chapitre, afin de dimensionner une source d'air extérieur grâce à un ventilateur axial par exemple (Figure 209). Ces modèles sont depuis longtemps connus dans la littérature grâce à des lois d'échelle donnant de bonnes approximations. Aucune vérification n'est faite dans cette thèse, car ces travaux sont déjà réalisés dans d'autres laboratoires spécialisés. Beaucoup de publications présentent aussi de ce genre de modèles, afin d'estimer leurs précisions.

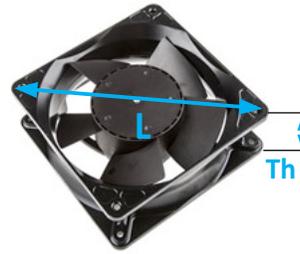
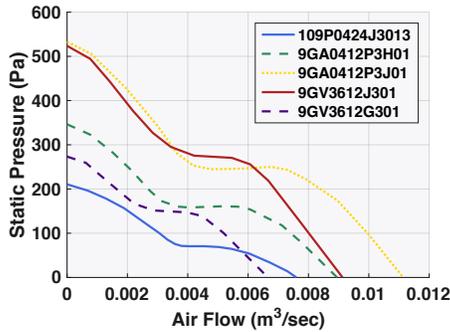


Figure 209: Modèles simplifiés de ventilateurs axiaux

15.4 Chapitre 4: Modèles simplifiés des composants passifs

Les composants passifs sont représentés par deux dispositifs : les composants magnétiques et les condensateurs, qui peuvent être assemblés pour former un objet topologique appelé filtre.

15.4.1 Composants Magnétiques

L'objectif de cette partie est de proposer un modèle qui permet la conception complète des composants magnétiques. Il s'agit alors d'utiliser la même approche que pour les objets actifs, mais en tenant compte ici de chacune des parties d'un composant magnétique : la forme, les dimensions et le matériau de son noyau, de ses conducteurs et de son isolant qui définissent les propriétés magnétiques, électriques et thermiques du composant magnétique. Précisons qu'ici « composant magnétique » désigne tous les dispositifs magnétiques, allant de l'inductance simple aux inductances couplées, aux transformateurs, en passant par des coupleurs inter-cellules (ICT). Chacune de ses familles possède une multitude de variantes, comme représenté dans la Figure 210 pour quelques exemples d'inductance et de transformateur. Dans un premier temps, nous ferons donc une synthèse de ses éléments, et nous rappellerons comment comparer ses objets grâce à des figures de mérite.

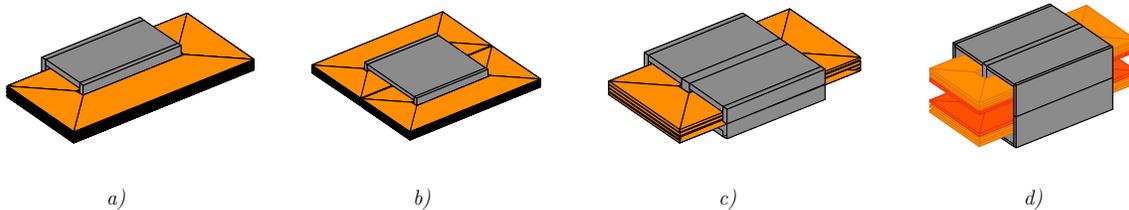


Figure 210: Echantillons d'inductances

a) U-core 1 enroulement - b) U-core two enroulements - c) E-core one enroulement- d) E-core transformateur

Dans un deuxième temps, nous exposons les différents modèles multi-physiques décrivant ces objets magnétiques : géométriques, objectifs, électriques (Figure 211), magnétiques thermique, coût etc.

Notons que ce travail a démarré il y a plusieurs années dans le laboratoire Laplace, avec des études antérieures sur les transformateurs et coupleurs inter-cellules (ICT) dans le cadre de pré-dimensionnement [121] [122] [16] [120]. Ce chapitre propose donc une synthèse globale de ces modèles, tout en complétant les parties manquantes du travail antérieur afin de créer une bibliothèque complète, en particulier pour l'inductance qui n'avait pas été traitée.

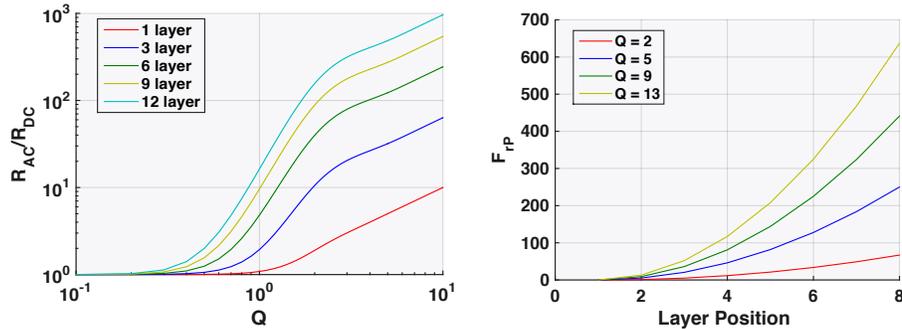


Figure 211: a) Variation de la résistance AC en fonction du facteur Q
 b) FEM simulation of the current distribution in the winding

Finalement, des simulations numériques sont réalisées afin de valider ces différents modèles (Figure 212).

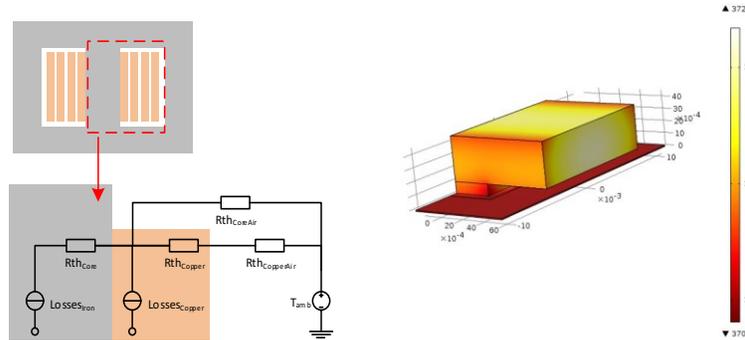


Figure 212: Modèle thermique simplifié d'un composant magnétique, avec une validation numérique 3D

15.4.2 Condensateurs

Comme pour les composants magnétiques, le but de cette partie est de proposer des principes de modélisation permettant aux concepteurs de définir des modèles continus de condensateurs. Ces modèles sont eux aussi essentiellement basés sur une description géométrique des différents éléments et matériaux composant le dispositif, définissant ses différentes caractéristiques internes multiphysiques (Figure 213). De ce dispositif théorique continu, il sera ensuite normalement possible de trouver des échantillons réels ou proches dans la production standard grâce à nos bases de données. C'est pourquoi nos modèles nécessitent d'être adaptable aux principales technologies, matériel et géométries des références disponibles sur le marché, présenté dans une synthèse. Nous introduisons

ensuite des figures de mérite, afin de mettre en évidence le condensateur la technologie la plus appropriée à l'application visée (condensateur de découplage, résonance, etc.).

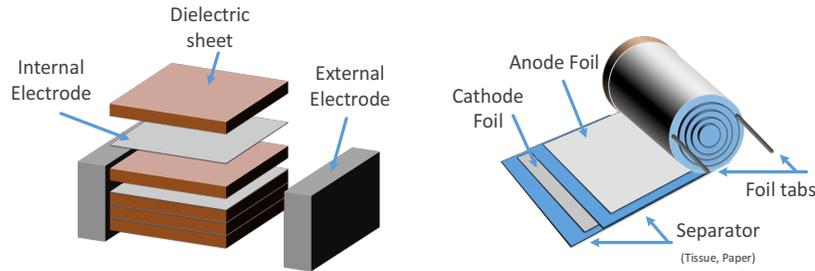


Figure 213: Architecture simplifiée d'un condensateur - a) Céramique b) Electrolytique ou Film

En second lieu, nous exposons le principe des différents modèles continus composant notre objet condensateur, et pour différentes granularités. Peu importe la géométrie initiale de ce composant, notre objet virtuel se basera toujours sur un condensateur élémentaire rectangulaire afin de faciliter l'étude multi physique (notamment avec des fonctions de passage du cylindre au parallélépipède rectangle si besoin). Ensuite deux options sont possibles : soit considérer les cotes extérieures du condensateur, soit ses dimensions internes issues de ses différentes couches diélectriques et conductrices (Figure 214). Cependant énormément de variété d'architecture internes existent, c'est pourquoi nous resterons dans le cas d'une architecture simplifiée, même si un écart important peut-être trouvé par rapport aux composants du marché.

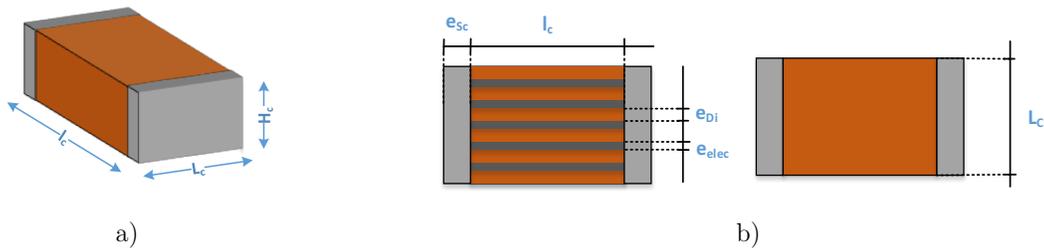


Figure 214: Descriptions géométriques de notre condensateur élémentaire
a) définition "externe" b) définition "interne"

Troisièmement, nous énumérons un à un les différents modèles physiques permettant de simuler fonctionnement d'un condensateur à travers nos solveurs et logiciel d'optimisation, avant de présenter des validations et conclusions (Figure 215). Nous présentons des modèles très satisfaisants au niveau des pertes, caractéristiques électriques et thermiques, que nous avons pu valider facilement grâce à des comparaisons avec notre base de données.

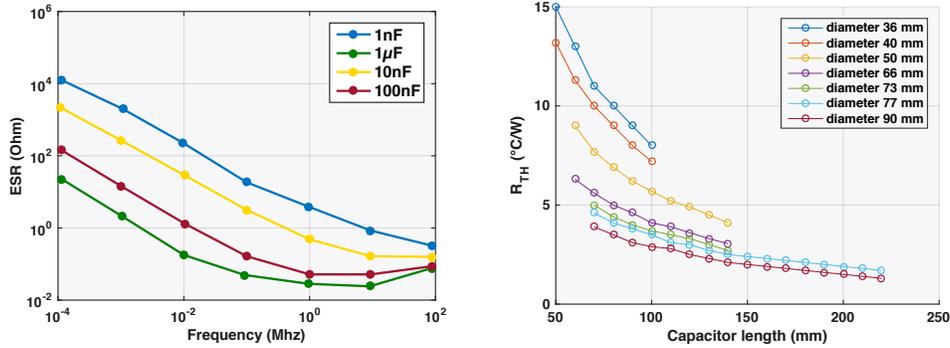


Figure 215: a) Evolution de l'ESR en fonction de la fréquence pour un modèle de condensateur céramique
 b) Résistance thermique en fonction de la longueur et du diamètre d'un condensateur cylindrique

15.4.3 Filtres

Les convertisseurs à découpage produisent du bruit à haute fréquence qui se propage sur les lignes électriques et peuvent affecter d'autres équipements électroniques connectés au même réseau. Cette énergie parasite produite par la fonction de découpage d'une alimentation électrique est prédominante à la fréquence fondamentale et ses harmoniques (quelques dizaines de kHz à 30 MHz). A ces fréquences, les normes CEM classiques imposent des niveaux de conduction maximale à ne pas dépasser (150kHz à 30MHz). Ainsi, la conception de filtres est essentielle dans le dimensionnement du convertisseur (souvent l'une des parties la plus volumineuse), en particulier par l'estimation des EMI (Interférences électromagnétiques), dont nous rappelons les différents types dans les systèmes embarqués.

Ainsi, une bonne estimation des perturbations de modes différentiel et commun est nécessaire pour être conforme aux normes CEM lors de la conception d'une alimentation embarquée. Cela est réalisé grâce à la création de la topologie dite passive, composée d'éléments magnétiques et de condensateurs (Figure 216). Cette topologie contient les dispositifs nécessaires à la simulation de test CEM cohérents avec les normes aéronautiques (ou n'importe quelle autre), tels qu'un RSIL (Réseau Stabilisateur d'Impédance de Ligne).

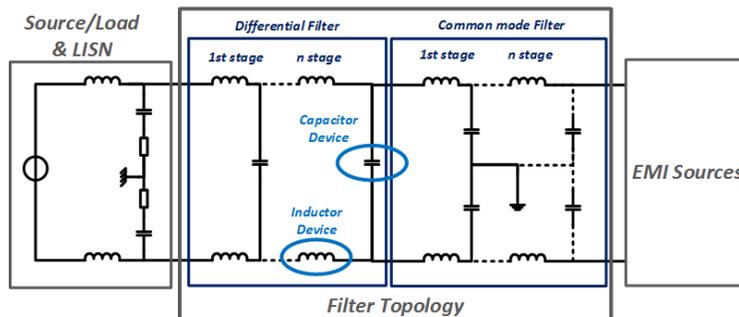


Figure 216: Principe de la topologie d'un objet "Filtre"

Deuxièmement, nous proposons des méthodes pour créer des sources équivalentes de perturbations, et expliquer comment dimensionner les filtres pour atténuer et isoler les perturbations, avec une extension aux convertisseurs multiniveaux. Pour conclure, nos modèles sont comparés à des simulations et des expérimentations pour valider notre approche. Par exemple dans le cas d'un DC-DC isolé, nous pouvons séparer les différents filtres coté basse et haute tension, et proposer des modèles multiniveaux série, parallèles ou mixtes. Finalement, ces principes de filtrages bien connus et maîtrisés pour le mode différentiel sont étendus au dimensionnement simplifié d'un filtre de mode commun, comme présenté dans la Figure 217.

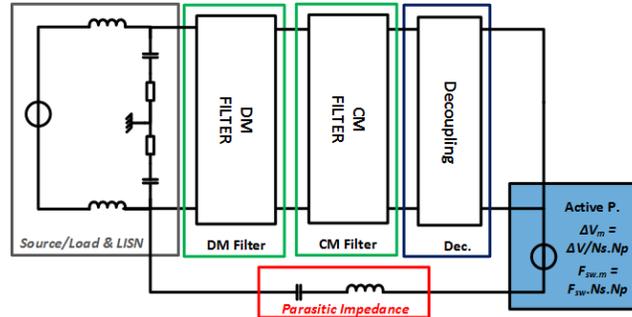


Figure 217: Circuit AC équivalent pour le mode-commun multicellulaire

15.5 Chapitre 5: Optimisation de composants et topologies dédiées aux applications aéronautiques

Le but de ce chapitre est de présenter une liste non-exhaustive d'applications utilisant le design préliminaire en électronique de puissance. Cette série d'exemples a été résolue grâce aux modèles multi-physiques exposés tout au long de cette thèse, et permet de démontrer le potentiel de notre approche utilisant notre outil de conception assistée par ordinateur, mais aussi de connaître ses limites et ses améliorations possibles. Comme exposé précédemment dans le chapitre 2, notre méthodologie de pré-dimensionnement est organisée en trois niveaux d'optimisation hiérarchisés, qui sont :

- Optimisation de Composants Individuels,
- Optimisation de Topologies, définies comme un assemblage de composants,

Optimisation de Convertisseurs, définis comme un assemblage de topologies et de composants.

15.5.1 Optimisation de composants individuels

Pour illustrer le niveau d'optimisation considérant uniquement des composants de base, nous avons choisi de présenter le dissipateur thermique à ailettes droites. Cette optimisation du radiateur peut être considérée parfois compliquée lors de la conception d'un convertisseur, vu qu'elle peut

représenter une masse importante. Ainsi, nous avons utilisé des analyses de sensibilité afin de montrer l'influence des paramètres principaux sur le dimensionnement de ce dispositif, et dans deux cas différents : en convection naturelle et en convection forcée (Figure 218).

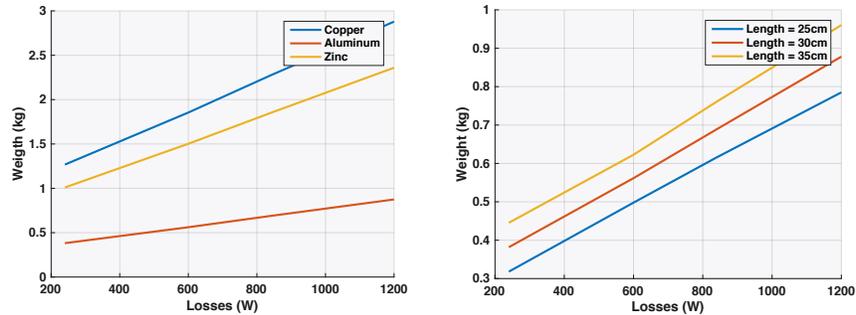


Figure 218: Evolution du poids du dissipateur en fonction du matériau et de sa longueur dans le cadre d'une convection forcée (4 points par courbe)

15.5.2 Optimisation de Topologies

L'optimisation concernant les « Topologies », qui sont divisées en deux familles distinctes, sont essentielles à la construction d'un convertisseur. Elles contiennent soit des topologies actives (Chapitre 3 : semi-conducteurs et dispositifs de refroidissement), soit des topologies passives (Chapitre 4 : Magnétiques et Condensateurs). Nous présentons des exemples d'étude de sensibilité pour les deux cas.

15.5.2.1 Passive

Pour illustrer une topologie passive, nous utiliserons un filtre différentiel appliqué à une topologie de hacheur classique, côté haute tension. Ce filtre est dimensionné selon les normes aéronautiques et démontre comment il est possible d'optimiser simultanément deux composants passifs : un condensateur et une inductance qui forment un filtre LC de 2nd ordre. Bien entendu, ce filtre imposera le respect des normes CEM avioniques et les considérations thermiques des composants et des spécifications du système. Cette résolution fait appel au solveur fréquentiel externe, qui permet de simuler la perturbation CEM du hacheur aux bornes de ce filtre. Des exemples de dimensionnement en fonction de la fréquence de découpage sont exposés dans la Figure 219.

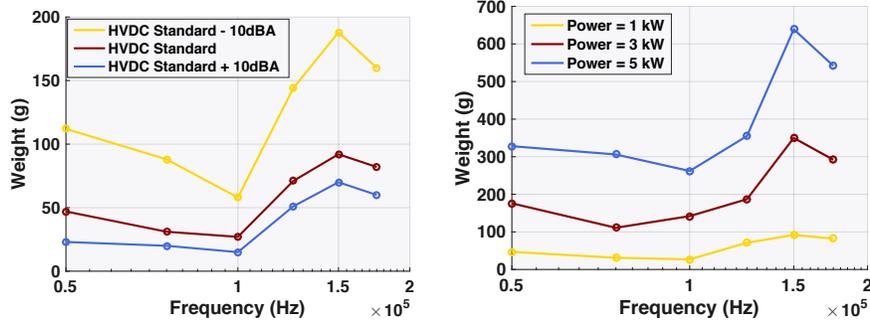


Figure 219: Evolution du poids du filtre en fonction de la fréquence de découpage, pour différents niveaux de la norme CEM HVDC et pour différentes puissances de convertisseur

15.5.2.2 Active

Pour illustrer les topologies actives, deux exemples d'optimisation ont été choisis, qui mettant l'accent sur deux applications DC-DC isolées. En effet, les applications DC-DC non isolées telles que le hacheur sont directement accessibles grâce au solveur (déjà utilisé en partie pour l'exemple du filtre, prouvant que cela fonctionne). C'est pourquoi ici les topologies analytiques sont des objets analytiques représentant des topologies précises et simulant leur fonctionnement.

a. DC-DC

Le premier exemple compare différentes topologies DC-DC isolées unidirectionnelles, afin de trouver le plus efficace et le plus léger des convertisseurs DC-DC pour une spécification de 400W. Une faible granularité est utilisée pour définir les modèles multi-physiques afin d'accélérer et d'améliorer la convergence des optimisations, mais aussi pour démontrer comment les compromis peuvent être rapidement réalisées dans un système de préconception. Cette méthode permet de prendre rapidement et sans avoir une grande précision des résultats aidant à la prise de décision de haut niveau. Pour rappel, l'objectif ici n'est pas d'obtenir un dimensionnement détaillé des dispositifs, comme il peut être atteint avec une granularité plus élevée (chapitre 2).

Poids (kg*)	Topologie DC-DC 400W						
	Forward	2-niveaux Forward-1L	2-niveaux Forward-2L	Push-Pull	Half-Bridge	Flyback	Flyback 2L
Etage d'isolation	0,02	0,02	0,05	0,03	0,02	0,06	0,11
Étages de conversion	0,24	0,30	0,49	0,15	0,20	0,21	0,12
Dissipateur	0,44	0,57	0,44	0,69	0,18	1,74	1,66
Poids total	0,71	0,89	0,98	0,87	0,40	2,00	1,88

Table 32: Analyse portant sur le poids des topologies candidates
 $\alpha = 0.35$, $\Delta T = 55^\circ C$, $F_{sw} = 100e3 Hz$

b. BBCU

Le deuxième exemple porte sur l'optimisation du Buck Boost Unit Converter (BBCU), un convertisseur de 12kW isolé et bidirectionnel. Il comprend les travaux de modélisation des solveurs continus et analytiques de très différentes topologies, et prend en compte une modélisation continue multi-niveaux de l'architecture du BBCU.

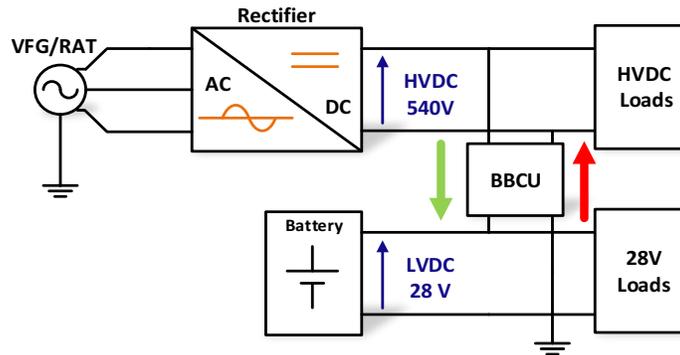


Figure 220: Schéma de principe du convertisseur DC-DC bidirectionnel et isolé 12kW, le BBCU

Une démarche complète d'optimisation est ensuite proposée jusqu'à la présentation des résultats (voir ci-dessous). Ces derniers permettent de tirer un bilan de ce qui fonctionne, mais surtout de ce qui reste à développer ou corriger.

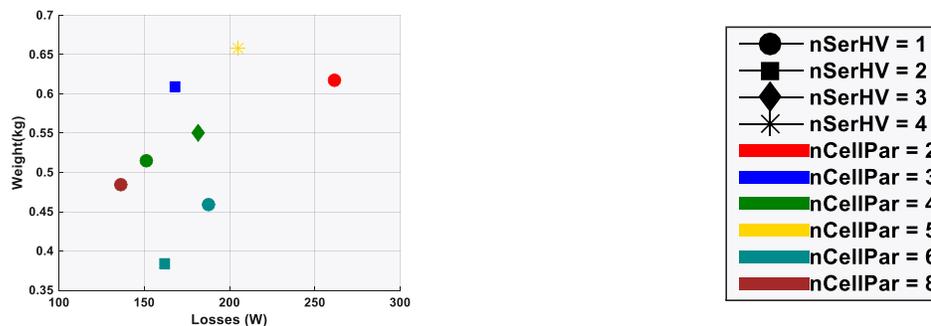


Figure 221: Résultat d'optimisation du poids de la topologie "Current-doubler", en fonction des pertes, et pour une fréquence de découpage @50 kHz et pour différentes configurations multiniveaux

15.5.2.3 Convertisseur complet

Le dernier niveau concerne les Optimisations au niveau 'Convertisseur', qui est le rassemblement des topologies actives et passives. Aucun résultat n'a été atteint à ce niveau dans le cadre de cette thèse. En effet, les résultats obtenus à partir de chaque topologie individuelle ne sont pas assez mûrs pour garantir des solutions solides et envisager leur couplage dans un convertisseur. Cependant, les scripts et les modèles pour définir une optimisation de conversion sont disponibles et les calculs peuvent être lancés. Seul le résultat final ne peut pas être garanti. Par conséquent, cette partie ne sera pas introduite dans ce chapitre, sauf dans notre conclusion pour discuter des travaux futurs.

Enfin, les avantages et les inconvénients de ces différents niveaux d'étude sont discutés. Les propositions de travaux futurs sont discutées, afin de continuer à améliorer la préconception en électronique de puissance.

15.6 Chapitre 6: Conclusion et Perspectives

Dans ce mémoire, nous avons expliqué comment concevoir une nouvelle plate-forme de conception assistée par ordinateur, afin d'optimiser n'importe quel composant ou équipement d'électronique de puissance. Dans ce contexte, des stratégies, des méthodologies, des outils et des modèles multiphysiques ont été créés, contribuant à la recherche de prototypage virtuel, de la modélisation et du pré-design en génie électrique. Ce travail a été utilisé pour répondre à certaines applications aéronautiques, et même si la route reste longue avant d'obtenir un outil finalisé et complètement robuste, il promet de devenir une aide précieuse lors du dimensionnement des convertisseurs statiques.

Cependant, à partir de nos résultats, il est nécessaire d'établir une liste d'éléments et de pistes à améliorer et compléter dans un futur proche. En effet, l'objectif final qui est de permettre une optimisation directe et efficiente des convertisseurs, à partir d'un cahier des charges électriques, n'est pas encore complètement atteint. Ainsi, une revue des axes d'amélioration et critiques de ce manuscrit est proposée dans ce chapitre en tant que conclusion générale du manuscrit.