Characterization and modelling of MOS transistors from advanced technologies (FDSOI, nanowire, GaN HEMT, LTPS...)

Donghyun Kim

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KOREA UNIVERSITY

UGA Université Grenoble Alpes

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ GRENOBLE ALPES
et de l'UNIVERSITE KOREA

École doctorale : Electronique, Electrotechnique, Automatique, Traitement du Signal (EEATS)
Spécialité : NANO ELECTRONIQUE ET NANO TECHNOLOGIES
Unité de recherche : L'Institut de Microélectronique Electromagnétisme et Photonique et le Laboratoire d'Hyperfréquences et de Caractérisation (IMEP-LAHC)

Caractérisation et modélisation des composants MOS des technologies avancées (FDSOI, nanofil, GaN HEMT, LTPS)

Characterization and modeling of MOS transistors from advanced technologies (FDSOI, nanowire, GaN HEMT, LTPS)

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Quentin RAFHAY MAITRE DE CONFERENCES HDR, Université Grenoble Alpes	Examinateur

Invités :

So Jeong PARK
DOCTEURE EN SCIENCES,
Korean Intellectual Property Office

Titre : Caractérisation et modélisation des composants MOS des technologies avancées (FDSOI, nanofil, GaN HEMT, LTPS…)

Mots clés : Microelectronique, Caracterisation, MOSFET

Résumé : Dans cette étude, la caractérisation électrique et la modélisation de divers dispositifs électroniques basés sur la structure MOSFET ont été effectuées. La caractérisation électrique des FET à nanofeuillets empilés verticalement sur FDSOI a été réalisée en utilisant une approche statistique. Ces NSFET présentaient diverses dimensions et ont été étudiés à la fois pour les NFET et les PFET. Chaque dispositif a été mesuré dans un grand nombre de matrices, totalisant plus de 170 unités. Les paramètres électriques ont été extraits au moyen de diverses méthodes, notamment la fonction Y et la fonction LW, entre autres. La corrélation entre différents paramètres électriques tels que Ion, Ioff, SS, la mobilité et les facteurs de dégradation de la mobilité a été étudiée. L'écart-type de chaque paramètre électrique a été utilisé pour interpréter la loi de Pelgrom. L'analyse des GaN HEMT jusqu'à la température cryogénique a été effectuée. Une caractérisation électrique détaillée et l'extraction des paramètres du transistor ont été réalisées sur des HEMT GaN/Si compatibles CMOS de 200 mm, même à des températures cryogéniques extrêmement basses. Les principaux paramètres du transistor, tels que la tension de seuil Vth, la mobilité à faible champ μ0, l'oscillation inférieure au seuil SS, et la résistance série source-drain Rsd, ont été extraits dans la région linéaire en utilisant les méthodes de la fonction Y et de la fonction Lambert-W, et ce, pour des longueurs de grille allant jusqu'à 0,1 μm. La méthode de la fonction Y a également été employée dans la région de saturation pour extraire la vitesse de saturation. Les résultats indiquent que ces dispositifs GaN/Si HEMT conservent leur excellent fonctionnement même à très basse température, avec une amélioration de la mobilité et de la pente inférieure au seuil. L'analyse TLM a également révélé que la résistance série source-drain Rsd est davantage limitée par la résistance de contact que par la résistance de la région d'accès 2DEG lorsque la température diminue. Les caractéristiques électriques et le profilage des pièges dans les TFT LTPS par rapport aux substrats rigides et flexibles ont été examinés. Nous avons mené une étude approfondie du transport de porteurs dans des transistors à couches minces en silicium polycristallin de type p (LTPS) sur un substrat flexible, en le comparant avec celui sur un substrat en verre, dans le but d'améliorer les performances du dispositif. Afin de comprendre l'origine du transport des porteurs sur ces substrats différents, nous avons effectué des caractérisations dépendantes de la température pour des paramètres des dispositifs électriques tels que VTH, SS, Ion et μeff. Il est bien établi que la taille des grains de poly-Si (Lgrain) et la hauteur de barrière (EB) entre les joints de grains sont les principaux facteurs déterminant le transport dans le silicium polycristallin, et ces paramètres peuvent être extraits en utilisant le modèle de mobilité polycristalline. Cependant, nos études systématiques ont montré que ce n'est pas la taille des grains, mais plutôt la hauteur de la barrière EB, qui a une plus grande influence sur la dégradation des TFT LTPS sur les substrats flexibles. La hauteur de barrière EB sur un substrat flexible est environ 18 fois plus élevée que sur un substrat en verre, tandis que la taille des grains est similaire pour les deux types de substrats. En comparaison avec les TFT LTPS sur substrat en verre, une hauteur de barrière EB plus élevée entraîne une dégradation d'environ 24 % de l'Ion, 30 % de la SS et 21 % de μeff sur le substrat flexible à température ambiante. L'analyse du bruit basse fréquence (LFN) a également révélé que la densité totale de pièges (Nt) sur un substrat flexible est jusqu'à quatre fois plus élevée que sur un substrat en verre, confirmant ainsi la valeur élevée de EB dans le dispositif fabriqué sur le substrat flexible.

Title: Characterization and modeling of MOS transistors from advanced technologies (FDSOI, nanowire, GaN HEMT, LTPS…)

Keywords: Charactertization, Microelectronics, MOSFET

Abstract: In this study, the electrical characterization and modeling of various electronic devices based on MOSFET structure were carried out. Electrical characterization of 2-vetically stacked Nanosheet FETs on FDSOI by using statistical analysis. NSFETs contained various dimensions were investigated for both NFET and PFET. Each device was measured in a lot of dies over 170 ea. Electrical parameters were extracted using various methods (Y-function and LW function, etc). The correlation of different electrical parameters (Ion, Ioff, SS, mobility, and mobility degradation factors) was investigated. The standard deviation of each electrical parameter was utilized for the interpretation of Pelgrom's law. GaN HEMT analysis down to cryogenic temperature A detailed electrical characterization and transistor parameter extraction on 200 mm CMOS compatible GaN/Si HEMTs was performed down to deep cryogenic temperatures. The main transistor parameters (threshold voltage Vth, low-field mobility μ0, subthreshold swing SS, source-drain series resistance Rsd) were extracted in linear region using the Y-function and the Lambert-W function methods for gate lengths down to 0.1 μm. The Y-function method was also employed in saturation region for the extraction of the saturation velocity. The results indicate that these GaN/Si HEMT devices demonstrate a very good functionality down to very low temperature with improvement of mobility and subthreshold slope. It was also shown by TLM analysis that the source-drain series resistance Rsd is more limited by the contact resistance than by the 2DEG access region resistance as temperature lowered. Electrical characteristics and Trap profiling in LTPS TFT comparing to on rigid and flexible substrates. The carrier transport of p-type low temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) on flexible substrate has been intensively studied and compared to that on glass substrate in order to improve device performance. To investigate the origin of carrier transport on different substrates, temperature dependent characterizations are carried out for electrical device parameters such as threshold voltage (VTH), subthreshold swing (SS), on-current (Ion) and effective carrier mobility (μeff). The poly-Si grain size Lgrain and the barrier height EB between grain boundaries are well known to be the main parameters to determine transport in polycrystalline silicon and can be extracted based on the polycrystalline mobility model. However, our systemic studies show that it is not grain size but EB that has more influence on the degradation of LTPS TFT on flexible substrates. The EB of flexible substrate is roughly 18 times higher than glass substrate whereas grain size is similar for both devices on different substrates. Compared to the LTPS TFT on glass substrate, higher EB degrades approximately 24 % of Ion, 30 % of SS and 21 % of μeff on the flexible substrate at room temperature. From low frequency noise (LFN) analysis, it is observed that the total trap density (Nt) for flexible substrate is up to four times higher than that of glass substrate, which also supports the high value of EB in the device fabricated on the flexible substrate.

Doctoral Dissertation

Characterization and modeling of MOS transistors from advanced technologies (FDSOI, nanowire, GaN HEMT, LTPS)

Donghyun KIM

Department of Electronics and Information Engineering

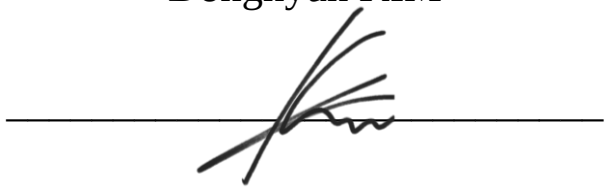
Graduate School

Korea University

February 2024

Characterization and modeling of MOS transistors from advanced technologies (FDSOI, nanowire, GaN HEMT, LTPS)

by
Donghyun KIM



under the supervision of Professor Jae Woo LEE

A dissertation submitted in partial fulfillment of
the requirements for the degree of
Doctor of Philosophy.

Department of Electronics and Information Engineering

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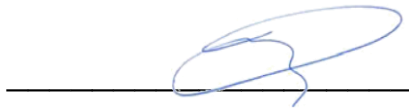
October 2023

The dissertation of Donghyun KIM has been approved by the dissertation committee in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

December 2023

Committee Chair: Jae Woo LEE



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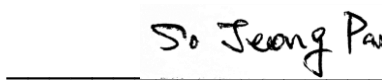
Committee Member: Hyun Suk KIM



Committee Member: So Jeong PARK

Characterization and modeling of MOS transistors from advanced technologies (FDSOI, nanowire, GaN HEMT, LTPS)

by Donghyun KIM

Department of Electronics and Information Engineering

under the supervision of Professor Jae Woo Lee

ABSTRACT

In this study, the electrical characterization and modeling of various electronic devices based on MOSFET structure were carried out. Electrical characterization of 2-vetically stacked Nanosheet FETs on FDSOI by using statistical analysis. NSFETs contained various dimensions were investigated for both NFET and PFET. Each device was measured in a lot of dies over 170 ea. Electrical parameters were extracted using various methods (Y-function and LW function, etc). The correlation of different electrical parameters (I_{on}, I_{off}, *SS*, mobility, and mobility degradation factors) was investigated. The standard deviation of each electrical parameter was utilized for the interpretation of Pelgrom's law.

A detailed electrical characterization and transistor parameter extraction on 200 mm CMOS compatible GaN/Si HEMTs was performed down to deep cryogenic temperatures. The main transistor parameters (threshold voltage V_{th}, low-field mobility μ_0, subthreshold swing *SS*, source-drain series resistance R_{sd}) were extracted in linear region using the Y-function and the Lambert-W function methods for gate lengths down to 0.1 μm. The Y-function method was also employed in saturation region for the extraction of the saturation velocity. The results indicate that these GaN/Si HEMT devices demonstrate a very good functionality down to very low temperature with improvement of mobility and subthreshold

slope. It was also shown by TLM analysis that the source-drain series resistance R_{sd} is more limited by the contact resistance than by the 2DEG access region resistance as temperature lowered.

Electrical characteristics and Trap profiling in LTPS TFT comparing to on rigid and flexible substrates. The carrier transport of p-type low temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) on flexible substrate has been intensively studied and compared to that on glass substrate in order to improve device performance. To investigate the origin of carrier transport on different substrates, temperature dependent characterizations are carried out for electrical device parameters such as threshold voltage (V_{TH}), subthreshold swing (SS), on-current (I_{on}) and effective carrier mobility (μ_{eff}). The poly-Si grain size L_{grain} and the barrier height E_B between grain boundaries are well known to be the main parameters to determine transport in polycrystalline silicon and can be extracted based on the polycrystalline mobility model. However, our systemic studies show that it is not grain size but E_B that has more influence on the degradation of LTPS TFT on flexible substrates. The E_B of flexible substrate is roughly 18 times higher than glass substrate whereas grain size is similar for both devices on different substrates. Compared to the LTPS TFT on glass substrate, higher E_B degrades approximately 24 % of I_{on}, 30 % of SS and 21 % of μ_{eff} on the flexible substrate at room temperature. From low frequency noise (LFN) analysis, it is observed that the total trap density (N_t) for flexible substrate is up to four times higher than that of glass substrate, which also supports the high value of E_B in the device fabricated on the flexible substrate.

Keywords: Electrical characterization, Low frequency noise, MOSFET, Nanowire, Nanosheet, Variability, GaN, HEMT, cryogenic, LTPS, barrier height, Seto model

최신 기술 적용 MOS 트랜지스터의 전기적 특성화 및 모델링 (FDSOI, nanowire, GaN HEMT, LTPS)

김 동 현

전자·정보공학과

지도교수: 이 재 우

Korean Abstract

본 연구에서는 MOSFET 구조를 기반으로 하는 다양한 전자소자의 전기적 특성화 및 모델링을 수행하였다. FDSOI 웨이퍼 기판에 제작된 2 개로 수직적층된 Nanosheet (NS) FET 의 전기적 특성 및 통계적 분석을 진행하였다. 다양한 게이트 면적의 NFET 과 PFET 을 이용하여 NSFET 의 분석을 진행하였다. 각 device 는 170 개가 넘는 많은 die 에서 측정되었다. 다양한 방법(Y-function, LW function 등)을 사용하여 다양한 전기적 매개변수를 추출하였다. 다양한 전기적 매개변수 (I_{on}, I_{off}, SS, effective mobility 및 mobility degradation factor)의 상관관계를 조사하였으며, 각 전기적 매개변수의 표준편차를 이용하여 Pelgrom's law 를 이용하여 해석하였다.

200mm CMOS 공정 호환 가능한 GaN/Si HEMT 에 대하여 상세한 전기적 특성화

및 트랜지스터 매개변수 추출이 극저온까지 수행하였다. 주요 트랜지스터 매개변수(V_{th}, μ_0, SS, R_{sd})는 게이트 길이가 0.1 μm 까지인 Y function 및 Lambert-W function 방법을 사용하여 선형 영역에서 추출되었다. Saturation velocity 추출을 위해 포화 영역에서도 Y function 방법을 사용하였다. 결과적으로 GaN/Si HEMT 소자가 μ_0 및 SS 의 개선과 함께 극저온까지 우수한 동작 특성을 가지는 것을 확인하였다. 또한 온도가 낮아짐에 따라 R_{sd} 이 2DEG access region resistance 보다 contact resistance 에 의해 더 크게 영향을 받는다는 것을 TLM 분석을 통해 확인하였다.

Glass 및 flexible 기판에 따라 LTPS TFT 의 전기적 특성 및 trap profiling 을 진행하였다. 소자 성능을 향상시키기 위해 flexible 기판에서 LTPS TFT 의 캐리어 이동특성에 대하여 집중적으로 분석하였으며, glass substrate 에서의 carrier transport 를 비교하였다. Glass 및 flexible 기판에서 carrier transport 의 특성 및 원리를 조사하기 위해 V_{th}, SS, I_{on} 및 μ_{eff} 와 같은 전기적 매개변수에 대해 온도에 따른 특성분석이 진행되었다. poly-Si grain 크기 L_{grain} 과 grain 경계 사이의 전기적 barrier 높이 E_B 는 다결정 실리콘의 수송을 결정하는 주요 매개 변수로 잘 알려져 있으며 다결정 이동도 모델을 기반으로 추출할 수 있습니다. 체계적인 연구에 따르면 flexible 기판에서 LTPS TFT 의 열화는 grain 크기뿐만 아니라 E_B에 크게 영향을 받는 것을 확인하였다. Flexible 기판의 E_B는 유리 기판보다 약 18 배 더 높은 반면, grain 크기는 서로 다른 기판의 두 TFT 에서 비슷한 것으로 확인되었다. Glass 기판의 LTPS TFT 와 비교하여 더 높은 E_B는 실온에서 flexible 기판 동작 특성들의 I_{on} 약 24%, SS 30%, μ_{eff} 21%를 저하시켰다.

저주파 잡음(LFN) 분석에서 Flexible 기판의 총 트랩 밀도(N_t)가 glass 기판보다 최대 4 배 더 높은 것으로 확인되었으며, 이는 또한 flexible 기판에 제작된 TFT 에서 높은 E_B 와의 상관관계를 가지고 있다.

중심어: Characterization, Low frequency noise, MOSFET, Nanowire, Nanosheet, Variability, GaN, HEMT, cryogenic, LTPS, barrier height

PREFACE

All of the work presented was conducted in IMEP-LAHC/UGA at Grenoble and AEDL with co-supervisor program between France and South Korea. All experimental materials and devices were approved by CEA-LETI (2-vertically stacked Nanosheet FET and GaN/Si HEMT) and Samsung Display Corporation (LTPS TFT).

A version of Chapter 3 has been published as two international conferences (2022 Solid State Devices and Materials [SSDM] in Japan and 2023 IEEE Electron Devices Technology and Manufacturing [EDTM] in South Korea).

A version of Chapter 4 has been published [Donghyun Kim, C. Theodorou, A. Chanuel, Y. Gobil, M. Charles, E. Morvan, Jae Woo Lee, M. Mouis, and G. Ghibaudo. "Detailed electrical characterization of 200 mm CMOS compatible GaN/Si HEMTs down to deep cryogenic temperatures." Solid-State Electronics 197 (2022): 108448.]. I was main investigator, responsible for major experiments, data collection and analysis, as well as manuscripts. A. Chanuel, Y. Gobil, M. Charles, and E. Morvan were responsible for the fabrication of GaN/Si HEMT in CEA-LETI. C. Theodorou, Jae Woo Lee, M. Mouis were responsible for co-supervisory authors for manuscript composition. G. Ghibaudo was major supervisory author and management for this project.

A version of Chapter 5 has been published [Donghyun Kim, Jungchun Kim, Haeyong Kang, Jae Won Shim, and Jae Woo Lee. "Influence of flexible substrate in low temperature polycrystalline silicon thin-film transistors: temperature dependent characteristics and low frequency noise analysis." Nanotechnology 31.43 (2020): 435201.]. I was main investigator, responsible for major experiments, data collection and analysis, as well as manuscripts. Jungchun Kim was responsible for experiments and data collection. Haeyong Kang and Jae Won Shim were responsible for co-supervisory authors for manuscript composition. Jae Woo Lee was major supervisory author and management for this project.

With regard to excellence, it is not enough to know,

But we must try to have and use it.

- Aristotle

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Chapter 1. INTRODUCTION

1.1 Semiconductor Market Trend

In the current situation, the emergence of technologically advanced devices, such as smartphones and tablet PCs, has significantly impacted the trends within the semiconductor market. The inception of these smart devices can be traced back to the IBM Simon, which was introduced in the year 1993 as the world's first-ever smart device. This revolutionary gadget served as a convergence between a mobile phone and a personal computer, offering a wide range of features such as a schedule manager, an address book, a world clock, a fax machine, various games, and a calculator, among others. Over time, smart devices have continued to evolve, resulting in the development of other notable devices like the personal digital assistant, the iPhone, and the Galaxy Tab. It is worth noting that the introduction of the iPhone and Android smartphones into the market has had a profound impact. These

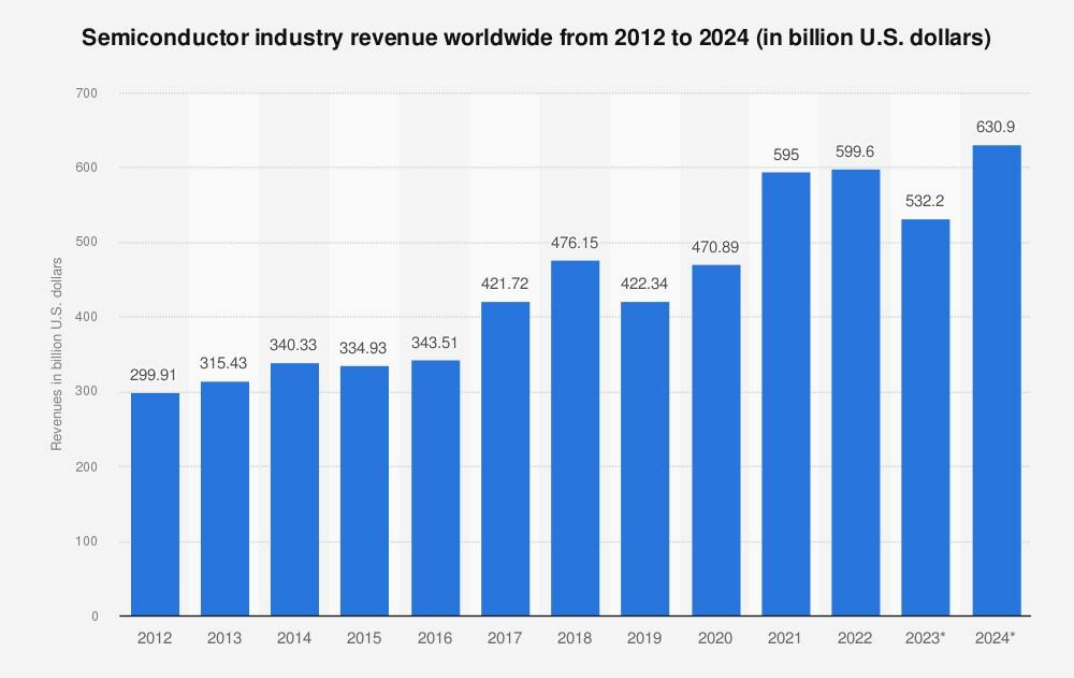


Figure 1.1 Semiconductor industry revenue worldwide from 2012 to 2024 [1]

devices have paved the way for the creation of countless smart applications that utilize a simple user interface, a global positioning system (GPS), motion sensors, and Wi-Fi capabilities, among other features. These applications play a crucial role in bridging the gap between human users and smart devices, enhancing the overall user experience, and facilitating seamless interaction.

The exponential growth of smart devices in the market is a result of the harmonious combination between applications and hardware. It has been predicted that the smartphone and tablet PC markets will experience a significant increase in growth. This increased demand for smart devices has led to changes in the trends of the semiconductor memory market. For instance, there has been a shift from PC Dynamic Random Access Memory (DRAM) to mobile DRAM and from Hard Disk Driver (HDD) to Solid-State Drives (SSDs) and NAND flash memory. A prime example of this shift is the expected growth of the market share of mobile DRAM in the DRAM market in early 2010s, which is projected to increase from 5.5% in 2010 to 7.1% in 2011, resulting in a total growth rate of over 100% [2]. In order to be utilized in mobile devices, mobile DRAM must be both cost-effective and possess high device density. Additionally, it must be developed to have high performance capabilities while maintaining low power consumption. On the other hand, the non-memory (specifically, system IC) device market is also experiencing changes due to the expansion of the smart device market.

The system IC market is experiencing growth, with a particular focus on the application processor (AP) for smart devices. In line with this trend, a strategic industrial feature known as the 'fabless company' has emerged, as shown in Tabel 1.1. This term refers to a semiconductor vendor that engages in the design, testing, and selling of chips without having its own semiconductor manufacturing facilities. Instead, it relies on other foundries to carry out the fabrication of the chips. While memory devices require an integrated device manufacturer, non-memory devices necessitate the capability to cater to customer requests through small quantity batch production. Consequently, fabless companies that prioritize chip design serve as the promising business core for the non-memory device sector.

Despite being one of the more recent trends in non-memory devices, the fabless company plays a crucial role in the research and development of device scaling down and advanced transistor technology. This includes the exploration of FinFETs, Fully Depleted Silicon-on-Insulator (FDSOI) and gate-all around (GAA) nanowires MOSFETs, such as the ones studied in the present thesis. These advancements in transistor technology remain of utmost importance as they contribute significantly to the improvement of fabrication yield, low power consumption, and overall device performance, among other factors. In essence, the fabless company's efforts in exploring these technologies and techniques are vital in driving progress in the field of non-memory devices.

Table 1.1 List of Top 10 Largest Semiconductor Companies by and Country in 2023 [3]

Rank	Company	Country
1.	Intel	United States
2.	Samsung	South Korea
3.	TSMC	Taiwan
4.	SK Hynix	South Korea
5.	Micron	United States
6.	Qualcomm	United States
7.	Broadcom	United States
8.	Nvidia	United States
9.	TI	United States
10.	Infineon	Germany

1.2 Device Scaling Down

As the dimensions of devices decrease, the task of fabricating these devices becomes more challenging. This can be observed in the case of integrated circuits, which become denser and more intricate as devices are scaled down. Consequently, various issues arise in areas such as lithography, interconnects, and processing. Scaling down the device size is

essential in order to enhance device performance, including augmented switching speed and reduced power consumption. For instance, the delay time τ of a circuit can be decreased by adjusting the gate length L, which is expressed as a function of the parameter S in Figure 1.2.

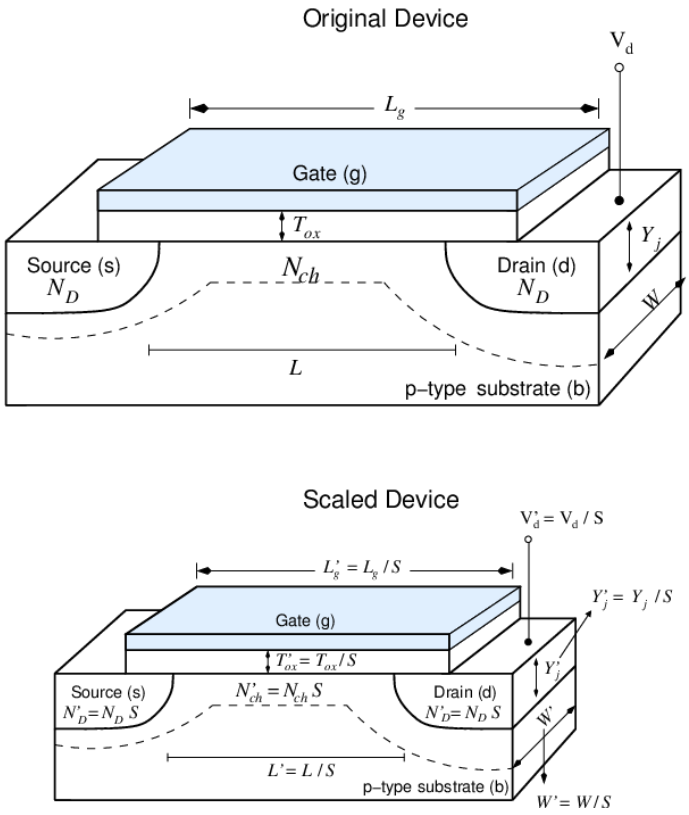


Figure 1.2 Architecture of an n-channel MOSFET and MOSFET constant electric field scaling by a factor of S [4].

There are two theories regarding the scaling of Metal-Oxide-Semiconductor (MOS) devices: Constant Electric (CE) field scaling and Constant Voltage (CV) scaling. The CE scaling theory suggests that in order to effectively manage the short channel effect, it is necessary to reduce both the horizontal and vertical dimensions of the device. Furthermore, it is proposed that the applied voltage should be decreased and the substrate doping concentration should be increased proportionally. These recommendations are summarized

in Figure 1.2, which provides a visual representation of the proposed scaling approach.

The CV theory, which is a theory that retains the same scaling down as the CE, does not alter the power supply voltage. This means that in order to maintain the charge-field, the doping densities are increased by a factor of S^2. However, it is important to note that the CV scaling inherently leads to a continuous increase of the transistor's internal electric field. This increase can potentially result in reliability problems such as electron migration, hot carrier degradation, and oxide breakdown in recent CMOS process generations. As a consequence, since the 0.5 µm MOS technology, the industry's preferred scaling methodology has been the CE.

Table 1.2 CE scaling of MOSFET device and circuit parameters [5]

Parameter	*1/S* Constant Field Scaling	30% Scaling Field Scaling
Physical Device Dimension	*1/S*	0.7
Supply and threshold voltage	*1/S*	0.7
$C_{ox}=(\varepsilon Area)/T_{ox}$	*1/S*	0.7
Gate Capacitance=WL/T_{ox}	*1/S*	0.7
Current=$(W/L)(1/T_{ox}V_{DD}^2)$	*1/S*	0.7
Propagation Delay=CV_{DD}/I	*1/S*	0.7
Frequency	*S*	1.43
Dynamic Power=$CV_{DD}^2 f_{clk}$	$1/S^2$	0.5
Leakage Power	Exponential	Exponentail
Energy	$1/S^3$	0.34

The fundamental principle underlying the CE theory is predicated upon the notion that the various physical attributes, namely the gate length, transistor width, and oxide thickness, as well as the voltages surrounding the power supply and the threshold, are accordingly and accurately adjusted and modified in accordance with a scaling factor of *1/S*, where *S* denotes a value greater than unity ($S > 1$).

Consequently, the current, gate capacitance, and propagation delay also scale by a factor of *1/S*. Hence, with a 30% reduction of all the device parameters ($1/S = 0.7$), improvements,

close to 50% in the operation frequency, are achieved for each generation. Table 1.2 lists the CE scaling rules for various device parameters and circuit performance factors. Evidently, the resulting switching energy scales by $1/S^3$, whereas the dynamic power scales by $1/S^2$. However, for a constant die size, the power dissipation due to the dynamic switching currents remains relatively constant with scaling, because the number of switching elements for the same die size increases by a factor of S^2. The negative effect of the CE is that the subthreshold current increases exponentially, as the threshold voltage scales. For example, consider a device with a V_{th} of 400 mV that is to be scaled by 0.7. For a constant die size, scaling provides around a 43% (S = 1.43) frequency improvement and doubles the number of devices. The dynamic power dissipation scales by unity, but the leakage current increases by a factor of $1.43\times10(V_{th}/S^{(1-0.7)}) = 45$.

Since the primary drivers behind the scaling of technology are mainly centered around improving performance and achieving efficient device integration, the comprehensive understanding and application of the CE scaling theory becomes a crucial and indispensable blueprint. However, with the continuous reduction in the dimensions and voltages of these devices, the emergence of leakage power as a prominent obstacle in both current and future technologies cannot be ignored. Consequently, the process of scaling VLSI technology gives rise to an array of complex and formidable challenges, encompassing power dissipation, effective management of leakage, and the adverse impacts of short channel effects. This multifaceted problem is further worsened in the context of portable energy-constrained VLSI applications, where the unnecessary drainage of battery power during extended idle periods poses a significant concern.

Gordon Moore, the co-founder of Intel, posits that the quantity of transistors present on a single chip shall increase twofold approximately every two years, a phenomenon commonly recognized as Moore's law, which has been widely acknowledged for a period of roughly 40 years, and has consequently propelled the industry forward (as depicted in Figure 1.3). This principle appears to have been effective thus far; however, it must be noted that the scaling limit of device dimensions is nearing its conclusion. At present, the Intel 7 nm

process node in 2023 has been utilized for mass production. In accordance with Moore's law, it is predicted that within several years, gate lengths on the order of a few nanometers, which represents the inherent physical constraint of the MOSFET, will be employed. Hence, the introduction of a novel conceptual framework for device scaling becomes essential in order to keep advancing in device yield and performance beyond the confines of Moore's law.

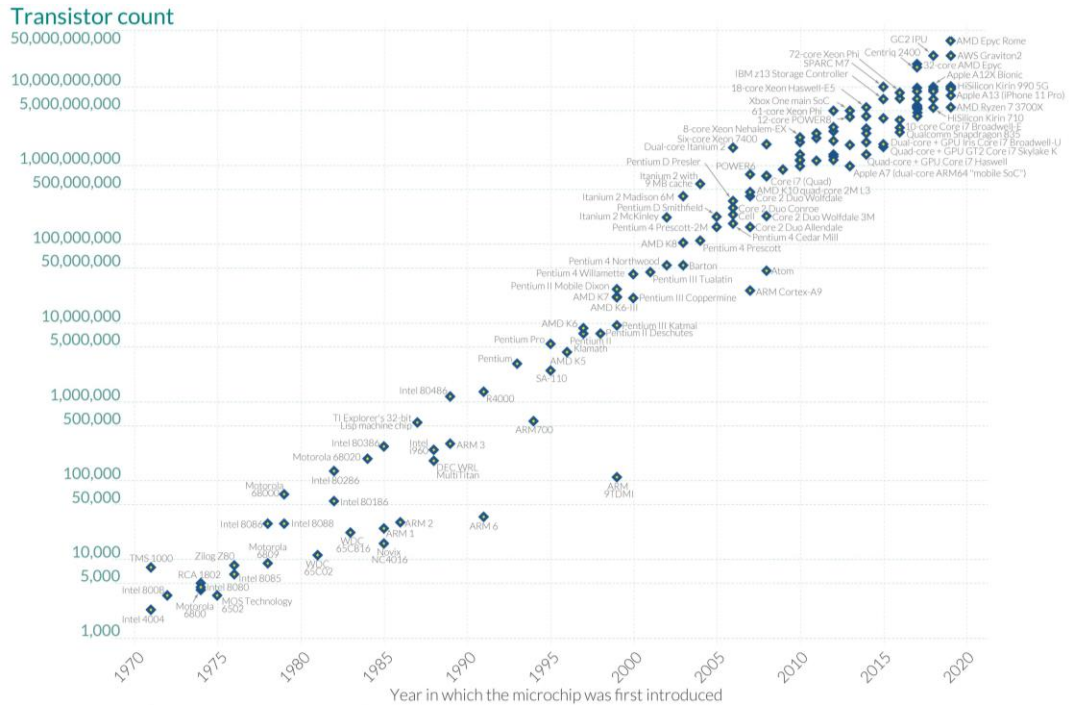


Figure 1.3 Number of transistors versus per year (Microprocessor). [6]

1.3 Fully Depleted Silicon on Insulator (FDSOI) Technology

1.3.1 State-of-the-art SOI Technology

The process of scaling bulk CMOS technology faces several significant obstacles, which has led to the exploration of alternative technologies such as FinFET, GAA nanowire

FET, and FDSOI. Among these alternatives, the FDSOI MOSFET stands out as a highly promising candidate for future technology nodes due to its potential advantages in terms of reduced variability and improved electrostatic integrity. This type of device is composed of a remarkably thin, fully depleted transistor body that is positioned on top of a buried oxide (BOX) layer, effectively sandwiched between the channel and the substrate. By employing an very lightly doped body, the floating body effect is eliminated, thereby providing immunity to variations in threshold voltage caused by random dopant fluctuations (RDF). Additionally, the body thickness (T_{si}) plays a crucial role in ensuring optimal electrostatic control by the gate.

FDSOI technology emerged as a progression of partially depleted SOI technology with the aim of eliminating the memory effect. FDSOI devices are characterized by having thin body structures, wherein the body is either rarely doped or completely undoped. Positioned beneath the channel, a BOX layer, which may be either thick (100 nm) or thin (10 nm), serves as an insulator, that also gives the possibility of bottom gate biasing to control the threshold voltage. In contemporary FDSOI processes, the source and drain regions are typically heightened and configured with facets, while the gate of the device is composed of metal gate stacks and high-k dielectric materials. Furthermore, in instances where a thin BOX is employed, doping beneath the BOX, known as ground plane (GP) doping, is sometimes implemented.

The advantages of FDSOI technology bound low variability, which related to the consistent and predictable behavior of the devices, good electrostatic control, which ensures reliable and stable operation, and the ability to integrate multiple threshold devices, allowing for enhanced flexibility in circuit design. However, any attempt aimed at enhancing the manufacturing process of FDSOI technology would be rendered meaningless if it does not coincide with improvements in circuit design, performance, and reliability. It is imperative that advancements in both the manufacturing process and circuit design are pursued in combination to fully capitalize on the potential benefits of FDSOI technology.

The current trend in the field of digital circuit design is focused on achieving maximum

performance while consuming low power. It has been previously mentioned that with FDSOI technology, high performance can be attained by reducing the threshold voltage. This reduction can be achieved through two methods: metal gate work-function engineering or back-biasing. However, it is important to note that lowering the threshold voltage poses a risk of forward biasing the diode between two adjacent ground planes, which in turn complicates the overall circuit design process.

Another potential advantage of FDSOI technology lies in its ability to have very low junction capacitances, particularly in the case of a thick BOX. However, it is worth mentioning that the raised source and drain structures introduce additional capacitance to the gate. One way to mitigate this issue is by changing the shape of the source and drain regions to a faceted shape, which aids in reducing the gate capacitance. However, it should be noted that even with this modification, the gate capacitance may still be higher compared to bulk technology. Therefore, unless the capacitance can be lowered through appropriate process engineering, there is no clear speed advantage of FDSOI over bulk technology in terms of capacitance.

Finally, it is important to consider the impact of Drain-Induced Barrier Lowering (DIBL) technology on the performance of FDSOI devices. A device with lower DIBL technology, exhibits a better subthreshold slope and consequently a higher linear current when compared to a device optimized for the same I_{ON} and I_{OFF} in a higher-DIBL technology. This suggests that the effective current in FDSOI technology has the potential to be higher compared to bulk technology, especially in scenarios involving complex gates and stacked devices.

A more apparent advantage of FDSOI technology lies in its potential applications in low-power systems. One of the primary reasons for this is the elimination of the source and drain pn-junctions, which effectively suppresses any possibility of junction leakage. In addition, the control over short-channel effects can be achieved by adjusting the body and BOX thickness. This control allows for a more conservative scaling of the gate dielectric, mitigating the concerns related to gate-induced leakage. Furthermore, the reduction in V_{th} roll-off and the utilization of light channel doping contribute to a decrease in threshold

voltage variation. Consequently, this improvement in threshold voltage variation enables the design of high-yield systems even at lower supply voltages. Consequently, the overall potential of FDSOI technology for low-power design is highly promising.

1.3.2 SOI Wafer Fabrication: Smart-Cut™ Process

UNIBOND SOI wafers are manufactured through the utilization of the Smart-Cut™ process, as mentioned in the study conducted by [7]. The fundamental aspect of this process lies in the combining of ion implantation process and wafer bonding techniques, which facilitates the successful transference of a delicate sheet of the semiconductor material onto a dielectric layer that subsequently transforms into the BOX layer. This particular technology, which was initially formed at the CEA-LETI, has gained widespread popularity and is currently employed on an industrial scale for the production of SOI wafers. The Smart-Cut™ process has undergone progressive expansion over time, enabling its utilization in the creation of different variations of SOI wafers. As a testament to its effictiveness, the process has been entrusted to SOITEC, an industry leader in the manufacturing of SOI wafers.

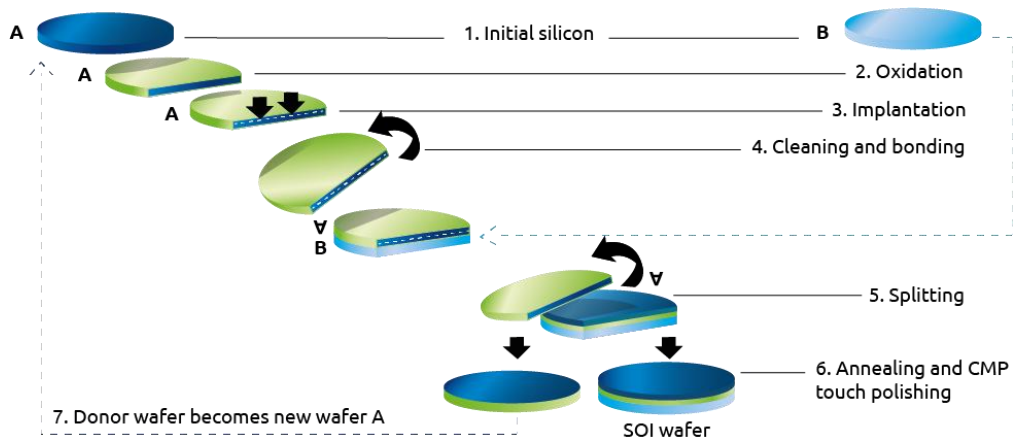


Figure 1.4 Smart-Cut™, an advanced SOI wafer fabrication technique by SOITEC Inc [7].

The Smart-Cut™ process, which is depicted in Figure 1.4 can be comprehensively

elucidated as follows: Primarily, it necessitates the utilization of two wafers, namely wafer 'A', which is referred to as the 'donor' wafer, and wafer 'B', also known as the 'handling' wafer. It is of utmost importance to note that the donor wafer 'A' is subjected to an oxidation process prior to the hydrogen implantation stage, resulting in the formation of an oxide layer on its upper surface, subsequently serving as the BOX layer. The next step entails the precise implantation of hydrogen atoms into the donor wafer 'A' at a specific depth, thereby facilitating the subsequent splitting of the two wafers. Moving on, the handling wafer 'B' can either be in its pristine state or it can be oxidized. The handling wafer plays a essential role in acting as a mechanical support for the SOI structure, ultimately aiding in the successful execution of the Smart-Cut process.

In order to initiate the direct wafer bonding, the wafer 'A' is positioned in a face-down manner onto the wafer 'B'. Subsequently, a two-phase heat treatment is meticulously carried out. During the first phase, which is conducted at an approximate temperature of 500 °C, the donor wafer 'A' undergoes a splitting process along a predetermined plane defined by the range of hydrogen ion implantation. Consequently, the thickest part of wafer 'A' is effectively separated from the bonded wafer structure. This consequential outcome gives rise to two distinct components: firstly, a thin layer consisting of single-crystalline silicon on top of the handle wafer 'B', which is underlaid by the oxide layer, and secondly, the remaining portion of the donor wafer 'A'. It is notable that this residual portion of the donor wafer can be recycled and employed once again as a donor wafer. The second phase of the heat treatment is subsequently implemented at a higher temperature, serving the purpose of strengthening the bond that exists between the Si/BOX layers and the handling wafer 'B'.

Upon the completion of the previous steps, a touch-CMP (Chemical-Mechanical Polishing) process is conducted, which is aimed at ensuring the attainment of optimal uniformity of the silicon films. It is significant to recognize that the process itself is highly

Figure 1.5 Various utilization of engineered SOI technique for specified commercialized products [8].

adaptable and can be accurately engineered in various ways in order to yield SOI wafers that are specifically tailored to cater to the exigencies of distinct applications, including but not limited to RF (Radio Frequency) switches or photonics. This versatility is vividly illustrated in Figure 1.5, thereby emphasizing the diverse possibilities offered by the Smart-Cut process.

The utilization of SOI technology exhibits significant potential in surpassing the scaling limit of CMOS technology through its distinctive characteristics. One of the key advantages of SOI technology is the ability to minimize or completely eliminate parasitic elements. Many undesired effects that are observed in bulk silicon devices arise from the interaction between the device and the substrate. It is evident that SOI devices are exempt from such interactions with the supporting substrate due to the presence of the BOX layer. Consequently, the implementation of SOI substrates ensures robustness against the latch-up phenomenon, which is commonly observed in bulk devices due to the feedback between the two inherent bipolar transistors.

The Smart-Cut^{TM} technique has emerged as the predominant method for producing standard and innovative SOI wafers. This technique is progressively being adopted within the CMOS industry. Its utilization allows for the design and fabrication of novel multi-gate

architectures, enabling the enhancement of device performance and electrical properties.

1.4 Overview of Power Electronics

Silicon has been the dominant semiconductor material ever since the advent of solid-state power conversion [9]. However, there has been a consistent rise in the need for greater power capabilities and higher frequencies. Consequently, the investigation of an alternative technology becomes vitally important in order to surpass the constraints of silicon-based electronics. Transistors fabricated from direct bandgap materials, notably III-V compounds like gallium arsenide (GaAs), indium phosphide (InP), and gallium nitride (GaN), present higher electron mobilities, sustain higher voltage magnitude, and exhibit the capability to function at higher frequencies and temperatures in contrast to silicon-based devices.

The high electron mobility transistor (HEMT), which is fabricated from III-V materials, has gathered considerable attention in recent times. In 1980, T. Mimura made the first HEMT utilizing GaAs [10]. GaN has emerged as the preferred option for HEMTs in numerous applications up to 100 GHz. This preference stems from the enhanced capabilities of GaN in delivering superior performance for high power HEMTs, owing to its high carrier density and electron mobility within the channel. Additionally, GaN exhibits higher breakdown and operating high temperature attributed to its larger bandgap [11]. These distinguished properties can make GaN HEMTs the most promising high power amplifier technology for a lot of applications ranging from mobile/wireless applications, radar systems to satellite communication and power systems [12,13,14,15]. The first report of GaN HEMTs were documented in 1993 [16], developing continuously during the last 27 years. Furthermore, during the last decade, these devices have been investigated extensively for their applicability in power electronics [17].

The material characteristics of semiconductors are presented in Table 1.3, in contrast to GaN. [18]. The parameters specified in Table 1.1 are assessed under the condition of 300 K.

The band gaps, relative dielectric constants, and breakdown fields are provided specifically for unintentionally doped (UID) bulk materials.

Table 1.3 Properties of semiconductor materials used in HEMTs at 300 K [18]

	Si	GaAs	InP	4H-SiC	GaN	SiC
Bandgap (eV)	1.12	1.43	1.34	3.2	3.44	3.26
Relative dielectric constant, ε_r	11.9	12.5	12.4	10	9.5	9.7
Breakdown electric field (MV/cm)	0.3	0.4	0.45	3.5	3.3	3
Saturation electron velocity (10^7 cm/s)	1	1	1	2	2.5	2
Electron mobility (cm^2/Vs)	1500	8500	5400	700	900	700

One of the specific benefits of GaN is its easier capacity to form the heterojunction with wider band gap materials, such as aluminium gallium nitride (AlGaN) and aluminium nitride (AlN). It generates a quantum well, commonly referred to as a two-dimensional electron gas (2DEG) channel. This channel is characterized by a significantly high electron density, exceeding $10^{13}/cm^2$, and exhibits electron mobility up to 2000 cm^2/Vs. Even though GaAs and InP own higher electron mobility, the significantly higher 2DEG density in GaN caused a lower sheet resistance which is the crucial characteristic for applications demanding high power at high frequencies. Additionally, GaN exhibits distinguished properties of higher band gap and breakdown field comparing to different semiconductor such as Si and InP, which empower high voltage operation with GaN HEMTs. Due to its ability to operate at high voltage, GaN HEMTs utilized in high line power converters as well as photovoltaic power converters. Also, with its wide band gap, GaN power electronics were applied in various industries such as automotive, military, and oil industries, etc [19].

1.5 Overview of Display Devices

1.5.1 Display devices history

The study of display is a fundamental area of research for individuals who reside in this

current era of abundant information. Simultaneously, great advancements have been made in the realm of display technology.

The Plasma Display Panel (PDP), which was once a fascinate spectacle, has its origins in the year 1964, thanks to the ingenuity of Donald B. and Jinslotto. Similar to the fluorescent lamp, the PDP operates by utilizing the concept of a phosphor being placed accurately between two glass plates, upon which a voltage is applied to stimulate the emission of visible light. Comparable to the Liquid Crystal Display (LCD) in terms of possessing a wide viewing angle and a remarkable display of colors and saturation, the PDP finds itself lagging behind in the market due to a rather unfortunate drawback - its propensity for high power consumption and the subsequent generation of heat. This fatal flaw has rendered it somewhat less attractive to consumers. Furthermore, one cannot ignore the ongoing progress and advancements being made in the realm of LCD and Organic Light Emitting Diode (OLED) technology, resulting in the recent developments witnessed in these fields.

The origin and subsequent advancement of LCDs can be attributed to the field of biology. It was in 1888 that F. Reinitzer, an esteemed researcher from Austria, made the groundbreaking discovery of liquid crystal. This crucial moment sparked a series of constant and meticulous research efforts, peaking in the creation of the world's inaugural LCD in the United States in 1971. The fundamental principle of an LCD requires the placement of a meticulously arranged panel containing liquid crystals on the front side, followed by the strategic positioning of a backlight situated behind it. As the backlight traverses through each individual liquid crystal, it undergoes refraction, resulting in an array of distinct and diverse patterns. The consequential passage of light through the color filter and polarizing filter, located at the forefront of the liquid crystal panel, yields the emergence of pixels that exhibit varying hues and intensities, contingent upon the specific refraction pattern encountered. Collectively, these pixels seamlessly amalgamate to form a cohesive and visually captivating screen. While LCDs have undoubtedly superseded CRTs in popularity and usage, it is essential to acknowledge the inherent drawbacks associated with this technology, namely its relatively limited lifespan and propensity for high power

consumption.

1.5.2 Display market trend overview

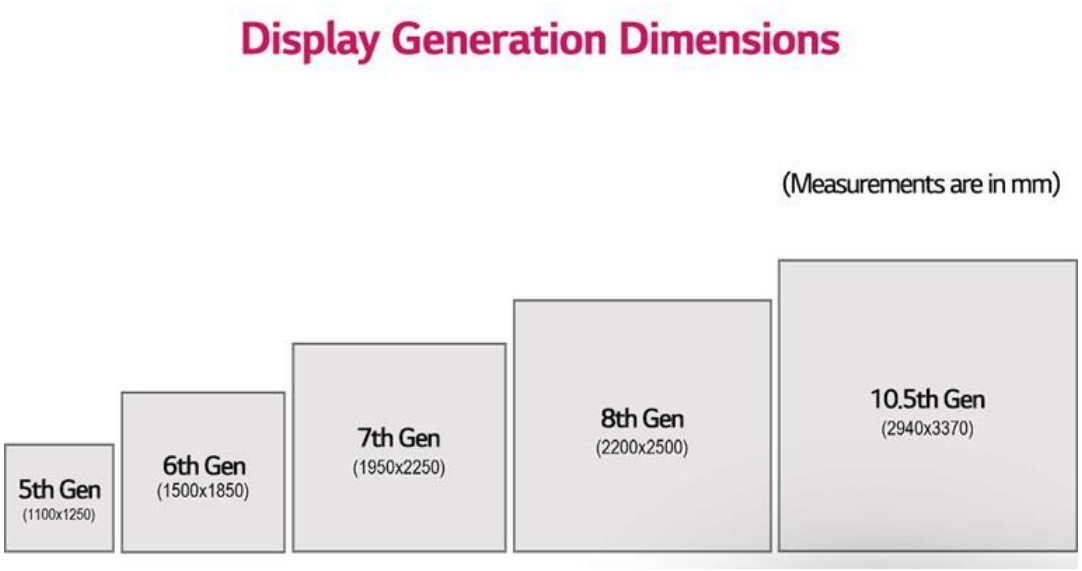


Figure 1.6 Changes in display panel's generation LG Display Inc. [20]

The Thin Film Transistor (TFT)-LCD industry has witnessed a remarkable growth trajectory due to its strategic expansion of the size of the mother glass, which is commonly referred to as the mother of the panel. This mother glass size, also known as "generation (GEN)" as depicted in Figure 1.6, plays a pivotal role in determining the dimensions of the panel itself, consequently influencing both the size and quantity of panels that can be produced. It is worth noting that, owing to the inherent differences in the panel sizes produced by individual companies, the corresponding sizes of glass substrates may exhibit slight variations across generations [20]. Consequently, it becomes evident that the entirety of display applications are merely mere fragments emanating from the mother glass. For instance, in the context of the 7th generation, we observe the existence of 42-inch panels in quantities of 8 sheets, alongside 47-inch panels in quantities of 6 sheets. Thus, it becomes

evident that the mother glass size predominantly serves as a mere indication of the essential components required for the production of panels by each respective manufacturer, while simultaneously striving to minimize the generation of discarded parts.

The commencement of LCD production in the mid-1980s resulted in a substantial growth rate of over 32% in the flat panel display market on an annual basis. During the period from 1995 to 2007, the market experienced an annual growth rate of more than 20%, with particular focus on the production of notebooks, monitors, and televisions. This growth was accompanied by fierce competition among Korea, Japan, and Taiwan, as these countries vied for dominance in the industry. Remarkably, Korea (SDC and LGD) emerged as the leading player in the global display market, attaining the largest market share since 2001, which stood at an impressive 44% in 2011. However, since 2016, the LCD market has witnessed a notable deceleration in its growth trajectory, largely attributed to the global economic downturn, an overabundance of medium and large LCD supplies leading to a

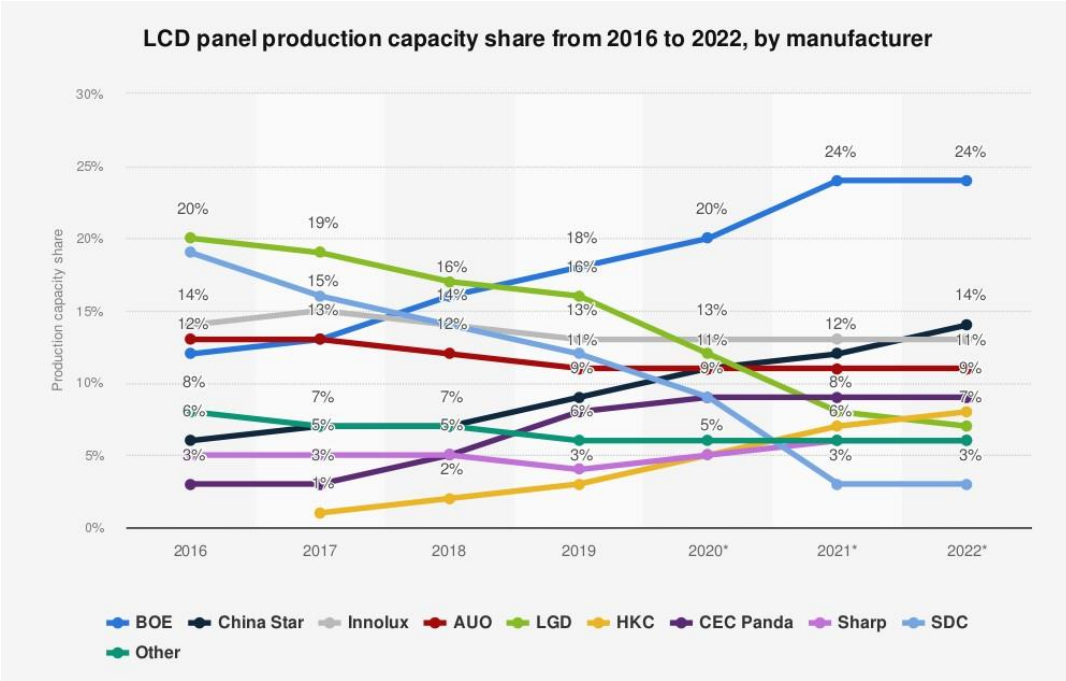


Figure 1.7 LCD production capacity by Industries [21]

decline in prices, and the rise of LCD production in China (as depicted in Figure 1.7). As a result of these factors, the LCD industry has experienced rapid stagnation since 2010. It is important to note that the slowdown in the LCD industry, which accounts for more than 93% of the overall display market, signifies a broader deceleration in the display industry as a whole. In response to this market congestion, our focus has shifted towards the development of next-generation displays, as we strive to overcome these challenges and propel the industry forward.

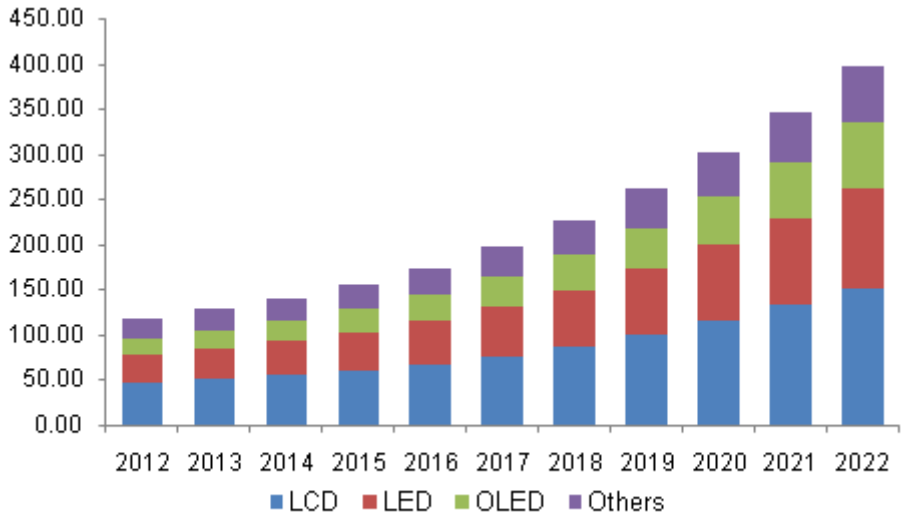


Figure 1.8 Asia-Pacific electronic display market revenue by technology [22]

Organic Light Emitting Diode (OLED) is widely considered to be a display technology that is at the forefront of the next generation of displays, capable of dominating the display market alongside LCD due to its various advantages. Since the year 2006, significant progress has been made in the development of OLED technology. In 2011, the successful production of the 5.5GEN OLED marked a turning point, leading to a rapid growth in the market, particularly in the realm of small to medium sized TVs. Efforts are now being made to penetrate the large TV market (Figure 1.8). As of 2012, the large OLED-TV market accounts for less than 10% of the overall market share, but there is a great expectation for this to increase significantly in the near future. The successful entry of large OLED-TVs into

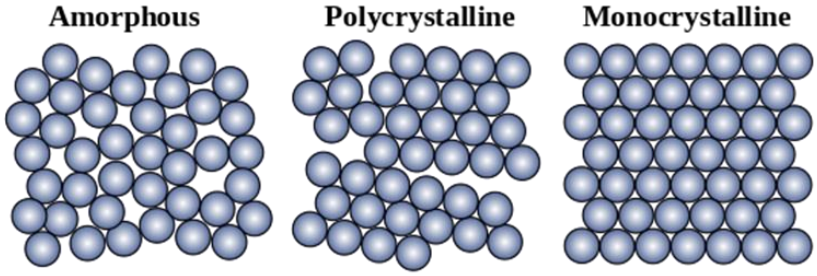
the market relies heavily on the advancement of two key technologies: the development of a large TFT backplane and the improvement of OLED pixel/encapsulation technology. The primary focus of TFT backplane technology is currently on two methods: LTPS TFT backplane and oxide TFT backplane technology. The latter, oxide TFT backplane technology, is particularly promising as it offers a simple manufacturing process and delivers excellent performance, making it an ideal choice for low-cost large OLED-TVs. On the other hand, the development of OLED pixel formation technology is largely dependent on two different approaches. The first method is based on the pattern mask technique known as SMS (Small Mask Scanning), which has been pioneered by Samsung Display. The second method, known as the white OLED + color filter method, has been developed by LG Display. Both Samsung Display and LG Display are planning to utilize these technologies to develop 55-inch OLED-TVs. In 2012, they aim to test-manufacture these TVs and subsequently announce their plans to produce them on a larger scale after 2013.

In the market for display technology, there is a growing trend towards larger panels. Consequently, there is a need to enhance the number of pixels per unit area by reducing the size of Silicon-based devices. With the increase in pixel count and the corresponding increase in the number of devices that the driving circuit must control, it becomes essential to improve the performance of the individual TFTs. However, TFTs also face challenges, such as the scaling problem encountered by Si-based devices. As a result, researchers are actively engaged in conducting studies to evaluate and compare the analysis methods of MOSFET.

1.5.3 Thin Film Transistors (TFTs)

In the realm of flat panel display, the dominant force in terms of production is attributed to amorphous Silicon TFTs. This form of display is currently undergoing a transformative process, one that is pushing it towards achieving higher levels of resolution and an overall increase in size. This evolution is visually represented in Figure 1.9. Consequently, various

alternative TFT technologies are being developed with the intention of replacing the existing amorphous Silicon TFTs. Two of the most promising contenders in this regard are Indium-Gallium-Zinc-Oxide (IGZO) and LTPS TFT.



α-Si	Poly-Si	Crystalline Si
No lattice	Different direction	One crystal
No boundary	Boundaries exists	No boundary
Low electron mobility (~>~0.5cm^2/Vs)	Relatively higher electron mobility (50~400cm^2/Vs)	High electron mobility (~>600cm^2/Vs)

Figure 1.9 The phase of silicon lattice and properties by silicon phase [23, 24]

Conventional FETs were manufactured utilizing the easily accessible material, Silicon. In the fabrication process of MOSFETs, a wafer is formed using an ingot, and subsequently, the process is initiated on this wafer. In order to produce monocrystalline silicon, also known as single crystalline silicon, a high-temperature procedure is necessary. However, due to the display panel's inability to withstand such high temperatures required for ingot manufacturing, α-Si is deposited on the channel through a relatively low-temperature process. The various properties of phase Silicon are comprehensively presented in Figure 1.9. Specifically, our attention should be directed towards electron mobility, where poly-Si exhibits a mobility rate that is approximately 100 times greater than that of α-Si. This heightened mobility plays a crucial role in determining the operational speed of TFTs.

Following this paragraph, we will delve into an exposition of the potential candidates for advanced TFTs.

The Indium-Gallium-Zinc-Oxide (IGZO) TFTs were derived from a semiconductor known as Transition Metal Oxide (TMO), which exhibits n-type conductivity as its fundamental property. In comparison to α-Si, IGZO possesses several advantages, including but not limited to higher mobility, excellent transparency, similar temperature processing capabilities, and cost-effective fabrication. Investigating the origins of binary TMO semiconductors, it can be observed that in 1990, extensive research was conducted based on the foundations of TMO. These binary TMO semiconductors were composed of a single transition metal oxide that demonstrated sufficiently high mobility and a wide bandgap of greater than 3 eV. Building upon the binary TMO platform, further advancements were made in the form of ternary and quaternary TMO semiconductors. In these advanced forms, different metals played distinct roles: Indium (In) enhanced the mobility of the channel, Zinc (Zn) exhibited a unique property of being grain boundary-free, and Gallium (Ga), when combined with InZnO, effectively suppressed the presence of oxygen vacancies, which otherwise could have disrupted the transport of charge carriers. Despite IGZO being a compound characterized by its amorphous phase, it astonishingly showcases a mobility that is 10 to 20 times greater, as illustrated in Figure 1.9 [25]. Even within the realm of amorphous states, the electron transport pathway remains consistent, thereby resulting in a relatively high mobility.

Most LCDs utilize amorphous silicon TFTs. However, in order to decrease production costs, reduce power consumption, and achieve high resolution, the development and utilization of poly-silicon TFTs is inevitable. LTPS refers to a technique for fabricating TFTs at a relatively low process temperature, which is below 500 ℃. This is in contrast to high-temperature poly-silicon, where the process temperature exceeds 900 ℃ and quartz is used as a substrate. The Poly-Si TFTs fabricated through LTPS method exhibit a current drive capability that is approximately two orders of magnitude higher compared to a-Si TFTs. By considering equivalent charging characteristics, it is possible for the TFT width to be smaller

than that of the α-Si TFT in the case of poly-Si TFTs. When the size of the TFT is reduced, the effective area increases, leading to an improvement in the aperture ratio and the possibility of achieving high resolution. Furthermore, integrating the driving circuit into the glass allows for a lighter, thinner, and more cost-effective display.

However, it should be noted that Poly-Si TFTs involve more complicated TFT processes compared to a-Si TFTs. Additionally, they have the disadvantage of lowering process margins due to circuit integration and increasing production costs as a result of the increased number of process steps and masks required compared to a-Si panels. Moreover, the non-uniformity of devices caused by the influence of grain boundaries poses a problem in the case of Poly-Si TFTs. Despite its excellent performance, Poly-Si TFTs are regarded as a next-generation display technology but are hindered by economic issues rather than performance-related drawbacks.

The fabrication of LTPS involves additional processes such as excimer laser annealing (ELA) and sequential lateral solidification (SLS) after the deposition of amorphous silicon in existing processes. ELA plays a crucial role in transforming the amorphous silicon into poly-silicon. Specifically, ELA utilizes an excimer laser to instantaneously irradiate the a-Si film for several nanoseconds, causing it to melt and recrystallize without damaging the glass substrate. However, ELA is not without its challenges. The process range is narrow, making it difficult to achieve uniformly crystalline poly-silicon, and the surface of the poly-silicon tends to be rough.

In order to implement high resolution and large area panel displays, there is a current development of faster TFT as potential candidates for replacing amorphous silicon TFT. These candidates include metal oxide (IGZO) and LTPS channels. Additionally, the development of OLEDs allows for thinner displays as the need for existing back lights is eliminated. Throughout the various generations (GEN) of panels, it is crucial to continuously improve the production processes. Moreover, the measurement and analysis of these panels becomes increasingly important as the issue of device yield arises.

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Chapter 2. MOSFET physics and characterization methodology

2.1 Introduction

In the preceding discourse, expounded upon in the first chapter of this scholarly work, the act of scaling down the dimensions of the future metal-oxide-semiconductor field-effect transistor (MOSFET) leads to an increasing deviation from the traditional planar bulk FET, which is typically equipped with a silicon dioxide (SiO_2) gate dielectric and a poly-silicon gate. Numerous approximated physical phenomena greatly influence the operation of the MOSFET as a direct consequence of this pronounced scaling down. One such phenomenon is the reduction in the dimensions of the channel, which consequently gives rise to surface roughness effects that detrimentally impact the effective mobility in the process of channel transport. The effective gate length assumes a heightened level of significance due to an augmented proportion of its presence in the overall geometrical channel length. The presence of series resistance has a twofold impact, not only affecting the drain current but also exerting an influence on the threshold voltage. Consequently, it becomes imperative to undertake a meticulous and comprehensive analysis of device characterization techniques in order to ascertain their accuracy and need for improvement.

In the progression and enhancement of sophisticated Field-Effect Transistors (FET), the reciprocal information flow between the construction of the device and its analysis is of utmost significance in achieving optimal performance. Thus, the extraction of precise parameters plays a pivotal role in the optimization of these advanced devices.

In this specific chapter, we will delve into the fundamental operation of the MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) and thoroughly explore the intricate details of its characterization. Our investigation will revolve around the measurement techniques employed, which will enable us to extract the various device parameters. Furthermore, we shall engage in a comprehensive discussion on the topic of device parameter extraction, thereby providing a comprehensive understanding of this crucial aspect.

2.2 Basic MOSFET operation

In this scholarly exposition, we shall present the fundamental equation of the MOSFET model in order to provide substantiated evidence for the subsequent extraction of the device parameters. It is imperative to note that the timeless principles and operations of the classic MOSFET, as outlined in Chapter 2.2.1 and 2.2.2, are reminiscent of the long channel device model.

2.2.1 Linear Regime (at V_D<(V_G-V_{th}))

At small bias of drain voltage V_D, the MOSFET operates in the linear regime, where the drain current I_D can be expressed as a function of various parameters as described by Eq. 2.1:

$$I_D = \frac{W}{L}\mu_{eff}C_{ox}(V_G - V_{th})V_D \quad \text{(Eq. 2.1)}$$

where W is the channel width, L the channel length, μ_{eff} the effective mobility, and the C_{ox} effective capacitance of the gate oxide. In the case of short and narrow channels, the effective gate capacitance incorporates the quantum confinement effect [1]. Through Eq. 2.1, if μ_{eff} is constant, the transconductance g_m can be described using Eq. 2.2:

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L}\mu_{eff}C_{ox}V_D \quad \text{(Eq. 2.2)}$$

2.2.2 Saturation Regime (at V_D>(V_G-V_{th}))

One of the principles of operation of a MOSFET is to regulate the gate voltage to determine how many electrons can flow through the channel. Pinch-off refers to a phenomenon in which electrons can no longer flow at a certain point in the channel. This phenomenon typically occurs when the channel length becomes short enough, and as the gate voltage increases, the channel becomes progressively thinner, eventually making it

impossible for electrons to flow.

After pinch-off, the drain current of MOSFET becomes independent of V_D and is saturated as in Eq. 2.3:

$$I_D = \frac{W}{2L}\mu_{sat}C_{ox}(V_G - V_{th})^2 \quad \text{(Eq. 2.3)}$$

$$g_m = \frac{W}{L}\mu_{sat}C_{ox}(V_G - V_{th}) = \sqrt{2\frac{W}{L}\mu_{sat}C_{ox}I_D} \quad \text{(Eq. 2.4)}$$

where μ_{sat} is the major carrier mobility in saturation regime. In an ideal situation, the drain current does not exhibit an increase as the drain bias V_D is increased. However, as the channel length is scaled down, numerous parasitic factors come into play, leading to additional effects that render the simplistic long channel current-voltage model invalid.

2.2.3 Transfer characteristics of MOSFET

2.2.3.a Threshold voltage, V_{th}

The transfer characteristic, also known as the I_D-V_G curve, is a fundamental and crucial property in the MOSFET. It plays a vital role in determining various key parameters of the MOSFET. By analyzing the transfer characteristics, significant FET parameters like the threshold voltage V_{th}, subthreshold swing *SS*, drain-induced barrier lowering DIBL, and low-field carrier mobility μ_0 can be accurately calculated. These parameters highlight the immense importance of the transfer characteristic in the characterization and analysis of FET devices.

The threshold voltage, denoted as V_{th}, holds great significance in the realm of circuit design. Its value can be utilized to derive other crucial parameters such as channel length,

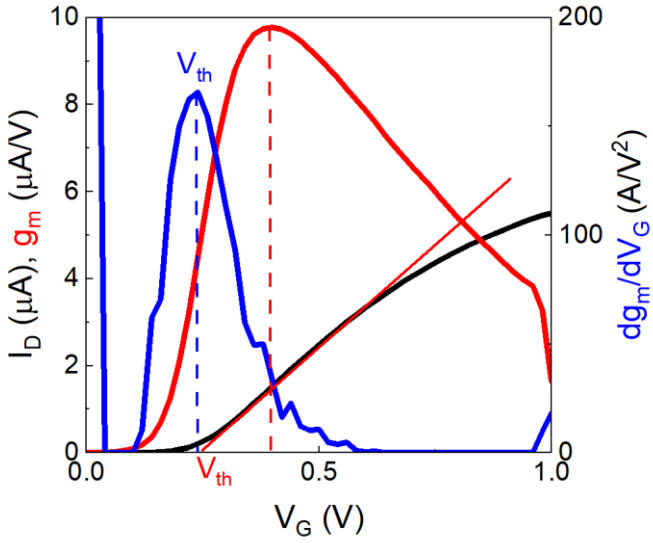

Figure 2.1 V_{th} determination by linear extrapolation method (Red) and second derivative method (Blue). Data was measured at V_D=30 mV.

channel width, and series resistance, among others. There are multiple definitions available to describe V_{th}, owing to the nonlinear nature of the transfer characteristic near this threshold voltage, which is primarily due to the presence of subthreshold current. It is also important to note that at high values of V_G, the transfer characteristics may depart from a linear pattern, primarily due to the effects of series resistance and degradation of mobility.

Linear extrapolation, a widely used method for V_{th} extraction [2], involves identifying the point on the I_D-V_G curve with the highest slope, which corresponds to the maximum value of transconductance. From this point, a linear fitting is performed on the I_D-V_G curve to extrapolate the value of V_G at zero current. However, it is crucial to note that this method can be influenced by the presence of series resistance and mobility degradation, as these factors can strongly impact the linearity of the I_D-V_G relationship [3, 4].

In the saturation regime, the calculation of V_{th} can be determined. By applying the square root operation to both sides of the equation, the transformation of Eq. 2.3 can be

implemented as follows Eq. 2.5:

$$\sqrt{I_D} = \sqrt{\frac{W}{2L}\mu_{sat}C_{ox}}(V_G - V_{th}) \quad \text{(Eq. 2.5)}$$

With Eq. 3.5 as a function of V_G, the intercept of x-axis is V_{th} through linear extrapolation. For the case of a short channel device, in which the current flow is limited by the saturation of carrier velocity, V_{th} can be easily determined by extrapolating it. Nevertheless, typically, the extraction of V_{th} is achieved by analyzing the I_D-V_G curve in the linear regime, as this approach aims to minimize any additional effects that may be induced by the presence of a high lateral electric field (which corresponds to a high V_D which is larger than V_{OV}=V_G-V_{th}).

The method of transconductance derivative utilizes the second derivative of the I_D-V_G characteristic at low V_D. It is derived from the theoretical ideal MOSFET model, where the I_D value is 0 when V_G is below V_{th}, and I_D is proportional to V_G when it is above V_{th} (as represented by Eq. 2.1). Within this model, the first derivative, $dI_D\ /\ dV_G$, is a step function, resulting in the second derivative of I_D-V_G being a delta function with an infinite value at V_G =V_{th}. Naturally, in practical cases, the maximum value of the second derivative is not truly infinite. Nevertheless, it remains a valuable tool as it is minimally influenced by series resistance and mobility degradation [2, 5].

The Y-function method, which is also known as the "drain current ratio" or "square root transconductance" method, was first proposed by G. Ghibaudo in 1988 [6]. This method combines the model of I_D-V_G and g_m-V_G characteristics in order to avoid the issue of carrier mobility degradation and parasitic series resistance. In this proposal, Ghibaudo takes into account the linear operation of the device at low drain voltage and expresses the drain current using Eq. 2.1. Additionally, the dependency of the mobility on the gate voltage is considered, which is then represented as:

$$I_D = \frac{W}{L}\frac{\mu_0}{1+\theta_1(V_G-V_{th})+\theta_2(V_G-V_{th})^2}C_{ox}(V_G - V_{th})V_D \quad \text{(Eq. 2.6)}$$

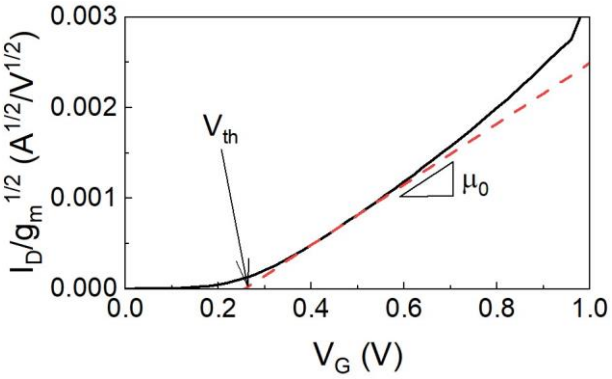

Figure 2.2 Y-function ($I_D/g_m^{1/2}$)-V_G characteristic in a n-channel Nanosheet MOSFET with a straight fitting line (red dash line)

where μ_0 is the low field mobility, and θ_1 the first order mobility attenuation coefficient which describes impurity and lattice scattering, and θ_2 the second order mobility attenuation coefficient which describes surface roughness scattering, respectively. Thus, the transconductance of Eq. 2.6 is represented by Eq. 2.7:

$$g_m = \frac{W}{L}\frac{\mu_0}{(1+\theta_1(V_G-V_{th})+\theta_2(V_G-V_{th})^2)^2}C_{ox}V_D \quad \text{(Eq. 2.7)}$$

The concept underlying the Y-function method revolves around the deliberate elimination of the mobility attenuation coefficient θ_1 and θ_2. This is achieved through a process of dividing the current I_D by the square root of the transconductance g_m. By doing so, a desired outcome is obtained, whereby the resultant value is derived as follows:

$$Y = \frac{I_D}{g_m{}^{1/2}} = \left(\frac{W}{L}\mu_0 C_{ox}V_D\right)^{1/2}(V_G - V_{th}) \quad \text{(Eq. 2.8)}$$

In Eq. 2.8, $I_D/g_m{}^{1/2}$ should be linear according to V_G with the intercept and slope which specify the V_{th} and μ_0, respectively. And then, the effective mobility attenuation coefficient θ_{eff} composed of the mobility attenuation coefficient θ_1 and θ_2 can be presented as Eq. 2.9:

$$\theta_{eff} = \frac{\left(\frac{W}{L}\mu_0 C_{ox}V_D\right)}{I_D} - \frac{1}{V_G - V_{th}} \quad \text{(Eq. 2.9)}$$

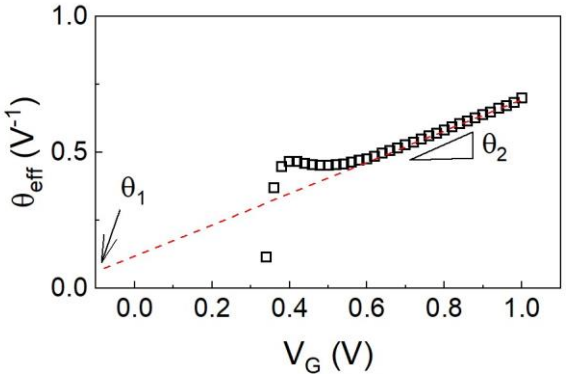

Figure 2.3 Extracted effective mobility attenuation coefficient $\boldsymbol{\theta_{eff}}$-$V_G$ from Y-function with a straight line in high inversion region

with the plot of Eq. 2.9, in the region of relative high overdrive voltage V_{ov}=V_G-V_{th}, the intercept and slope of θ_{eff} were indicated θ_1 and θ_2, respectively. In the situation of a device that has been greatly reduced in scale, such as a Gate-All-Around (GAA) or Nanosheet FET, the Y-function, which represents the device's performance, experiences a degradation due to the impact of a high gate voltage. On occasion, when it becomes imperative to extract the essential parameters from the Y-function, it becomes necessary to make modifications to the Y-function by means of employing iterations of θ_2 corrections.

2.2.3.b Subthreshold swing, *SS*

The subthreshold swing (*SS*), which refers to the change in gate voltage required to produce a tenfold increase in subthreshold drain current, is a prominent characteristic that is observed in the I_D-V_G relationship of the MOSFET. This phenomenon is particularly evident in the ideal MOSFET model, where the drain current remains at zero until the gate voltage surpasses the threshold voltage (V_{th}). However, in real devices, a diode-like behavior is observed in the drain current within the subthreshold region. This implies that even for gate voltages below the threshold voltage, there is still a small amount of drain current flowing through the device. The subthreshold drain current demonstrates an exponential behavior,

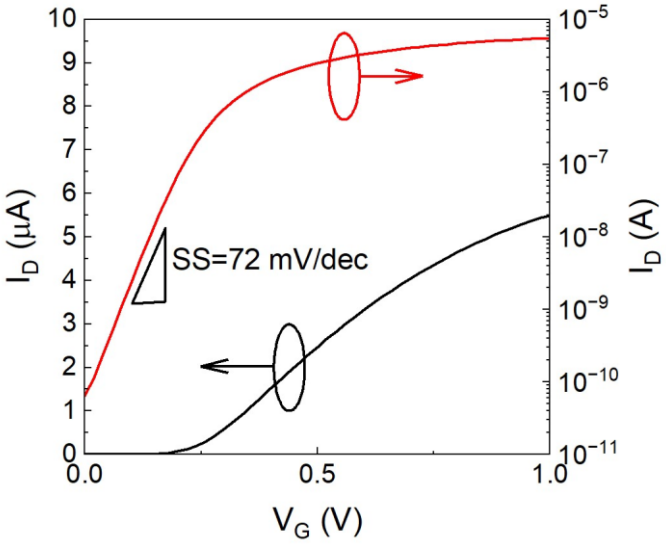

Figure 2.4 Subthreshold characteristic 2-vertical stacked Nanosheet FET (*W*=40 nm/*L*=120 nm)

which results in linearity when plotted on a logarithmic graph of the transfer characteristics.

From the reciprocal logarithmic slope of subthreshold drain current, *SS* can be defined as Eq. 2.10:

$$SS = \frac{dV_G}{dlogI_D} = 2.3(\frac{dV_G}{dlnI_D}) \quad \text{(Eq. 2.10)}$$

From diode like behavior, subthreshold drain current can be represented by Eq. 2. 11:

$$I_{D_{subV_{th}}} = I_0(\frac{q(V_G - V_{th})}{nK_BT})(1 - \exp(-\frac{qV_D}{K_BT})) \quad \text{(Eq. 2.11)}$$

The determination of I_0 is influenced by a multitude of factors, such as temperature, the effective dimension of the device and the concentration of doping, among other contributing factors. The value of n is intimately connected to the concept of ideality, which refers to the optimal conditions for capacitive coupling to occur between the interfaces of a gate stack. In situations where there is a presence of interface trap density, the value of *n* is

given by Eq. 2.12:

$$n = 1 + \frac{C_{it}}{C_{ox}} + \frac{C_d}{C_{ox}} \quad \text{(Eq. 2.12)}$$

where C_{it} is the interface trap state capacitance and C_d the channel depletion capacitance [7]. In the special case of the FDSOI, it can be observed that the concentration of C_d, which represents the depletion charge, reaches approximately a value of 0. This occurrence can be attributed to the fact that the depletion charge Q_d remains constant in relation to the voltage bias, as represented by the equation $C = dQ/dV$. By employing the Eq. 2.11 and 2.12, it becomes possible to estimate the value of *SS*, commonly known as the subthreshold swing as follows:

$$SS \approx 2.3 \frac{K_B T}{q} n \quad \text{(Eq. 2.13)}$$

where $\frac{K_B T}{q}$ is thermal voltage known as roughly 26 mV at room temperature.

For a device to exhibit desirable turn-on characteristics, it is important that the value of *SS* is minimized as much as possible. A more pronounced slope in the *SS* not only facilitates superior gate control but also leads to a decrease in the value of the subthreshold swing. It is worth noting that at ambient room temperature, the minimum value for the subthreshold swing is recorded to be about 60 mV/decade. The increase in subthreshold swing as the channel length decreases is a crucial concern in the scaling of silicon-based MOSFETs. This issue holds significant importance as it directly impacts the performance of logic circuits for low-power, high-speed applications. The subthreshold swing, being a critical parameter, plays a vital role in determining the device performance when it comes to the miniaturization of MOSFETs. A comprehensive understanding of this relationship is necessary for the successful implementation and optimization of these devices, as highlighted by previous research.

2.2.3.c Carrier Mobility

In solid-state physics, the term 'carrier mobility' commonly refers to the inherent characteristic of the carrier, be it an electron or a hole, to engage in movement within a semiconductor or metal in the presence of an electric field *E*. Depending on the specific type of carrier, the term 'carrier mobility' may also be referred to as either electron mobility or hole mobility. Upon the application of an electric field *E* across a conductor or semiconductor, the electrons or holes within the conductor or semiconductor initiate motion at an average velocity which is recognized and identified as the drift velocity v_d. So, the electron mobility μ is defined by Eq. 2.14:

$$v_d = \mu E \qquad \text{(Eq. 2.14)}$$

where μ is the carrier mobility and specified in the unit cm^2/Vs. In the case of an intrinsic semiconductor, the mobility of the charge carriers is closely affected to the various scatterings, which can include interactions with phonons, impurities, defects, or even the disorder caused by alloy composition. These different scattering processes have a direct impact on the overall drift velocity of the carriers within the semiconductor material.

In the semiconductors, the scattering mechanisms that are encountered most frequently and hold significant relevance are ionized impurity scattering and phonon scattering, more specifically, acoustic phonon scattering. When it comes to highly doped semiconductors, ionized impurity scattering plays a particularly crucial role as it involves the scattering of carriers, which are influenced by the electric field of the ionized impurities that originate from donors and/or acceptors present in the semiconductors. The scattering potential of ionized impurity scattering is assumed to be similar to Coulombic scattering, with the only difference being that the ionized impurity scattering possesses the capacity to draw in mobile carriers, who in turn act as a form of screening for the potential. In contrast, when it comes to the phonon (or lattice) scattering, the band structure of the semiconductor is subject to alteration due to variations in the lattice spacing, which can occur at any temperature higher than the absolute zero point of 0 K. The phenomenon of atoms vibrating within a crystal

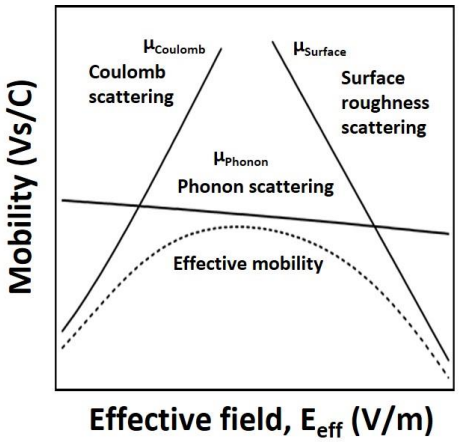

Figure 2.5 Schematic diagram to the effective field dependence of mobility by three different scattering mechanism [8]

lattice structure leads to the establishment of a precise distance between the lattice points, this vibration gives rise to the generation of pressure waves, specifically those of an acoustic nature. These pressure waves, commonly referred to as phonons, are known to have the ability to induce the scattering of carriers within the crystal lattice.

There exist two distinct categories of phonons: acoustic phonons and optical phonons. Acoustic phonons, characterized by their ability to propagate through the crystalline lattice, are directly linked to the displacement of neighboring atoms in a parallel direction. Conversely, optical phonons originate from the displacements of atoms in opposite directions [9]. In addition to the major scattering phenomena observed in semiconductors, it is essential to acknowledge the existence of several other significant scattering mechanisms, namely neutral impurity scattering, surface roughness scattering, and defect scattering. These additional scattering processes occur that is accidental upon the specific materials being utilized, the complicated structures in which they are incorporated, and the complexity of the overall manufacturing process involved.

According to the rule of Matthiessen, it is possible to combine multiple sources of scattering mechanism in Eq. 2.15:

$$\frac{1}{\mu} = \frac{1}{\mu_a} + \frac{1}{\mu_b} + \frac{1}{\mu_c} + \cdots \quad \text{(Eq. 2.15)}$$

where μ_a, μ_b, and μ_c are different mobilities affected by various scattering mechanisms above explanations (phonon or coulomb, etc) [8, 10].

Concerning the MOSFET, the mobility is not the ideal parameter for interpreting the device operation because the gate voltage can be measured experimentally not the effective electric field. Therefore, the relationship between effective mobility degradation and gate voltage is described by:

$$\mu_{eff} = \frac{\mu_0}{(1+\theta_1(V_G - V_{th}) + \theta_2(V_G - V_{th})^2)^2} \quad \text{(Eq. 2.16)}$$

using mobility attenuation coefficients from Y-function. In the long channel devices, θ_2 is negligible, but it might be significantly effective in the short channel devices [11, 12].

2.2.3.d Series Resistance

In linear regime, FET operates as a gate-controlled resistor. The resistance of FET consists of source resistance R_S, channel resistance R_{ch} and drain resistance R_D. I_D was influenced by R_S and R_D. Total series resistance R_{SD} can be representative as a superposition of R_S and R_D. R_{SD} is originated from the source and drain contact resistance, the sheet resistance of source and drain and the spreading resistance at the transition from the source diffusion to channel, etc. As device dimension reduced like FinFET and nanowire FET, bottleneck of carrier transport between low dimensional channel and source (or drain) also induce resistance. With the consideration of R_{SD}, total drain conductance g_d can be written as:

$$g_d = \frac{1}{R_{SD} + (1/g_{d0})} = \frac{g_{d0}}{1 + (R_{SD} g_{d0})} \quad \text{(Eq. 2.17)}$$

where g_d is the channel conductance. g_d can be calculated by using μ_0 and g_{d0} as follows

Eq. 2.18:

$$g_{d0} = \frac{\mu_0 W Q_n}{L} \quad \text{(Eq. 2.18)}$$

Consequently, I_D was described as Eq. 2.19:

$$I_D = G_m \frac{V_G - V_{th}}{1+\theta_1(V_G-V_{th})+\theta_2(V_G-V_{th})^2} V_D \quad \text{(Eq. 2.19)}$$

where the first order mobility attenuation factor θ_1 is $\theta_1 = \theta_{1,0} + G_m R_{SD}$, $\theta_{1,0}$ the intrinsic first order mobility degradation coefficient and G_m the low field transconductance parameter $G_m = \frac{\mu_0 W C_{ox}}{L}$.

Through Eq. 2.19, Q_n is approximately calculated by $C_{ox}(V_G - V_{th})$. Due to the presence of a total of three unidentifiable variables, namely G_m, θ_1, θ_2, and V_{th}, the process of determining the values of these unknown parameters can be accomplished by solving three distinct equations, as denoted by Eq. 2.19. From the linearity of first order mobility attenuation factor θ_1, series resistance R_{SD} can be extracted [13].

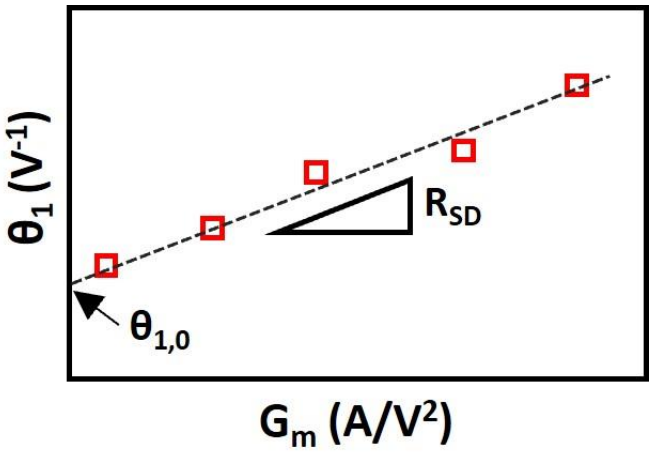

Figure 2.6 Extraction of the series resistance R_{SD} and intrinsic first order mobility degradation coefficient $\boldsymbol{\theta_{1,0}}$

2.3 Fundamental noise sources

In the device performance, noise is an unavoidable component that must be taken into consideration. From the standpoint of device operation, noise is a factor that needs to be eliminated. However, when it comes to device qualification, noise can actually serve as a valuable tool. There exist numerous origins from which noise can originate. In this chapter, we will delve into the examination of various characteristics pertaining to low frequency noise (LFN).

2.3.1 Thermal noise

Thermal noise is an extremely prevalent type of noise that arises due to the thermal motion of carriers. This thermal noise is consistently distributed across the entire frequency spectrum, hence earning the designation of 'white noise'. The generation of thermal noise is a consequence of the Brownian motion exhibited by carriers, which is heavily reliant on temperature. Consequently, even in scenarios where an electrical current is absent, thermal noise persists within the device. Power spectral Density (PSD) of thermal noise is given by Eq. 2.20:

$$S_V = 4K_BTR \qquad \text{or} \qquad S_I = \frac{4K_BT}{R} \qquad \text{(Eq. 2.20)}$$

where S_V is the PSD of thermal noise voltage, S_I the PSD of thermal noise current, R the resistance.

2.3.2 Shot noise

Shot noise is a phenomenon that arises when there is a flow of electric current across a potential barrier, which can commonly be observed in structures such as pn-junctions. This occurrence of shot noise is primarily due to the inherent discontinuity of the current flow, which arises from the discrete and quantized nature of charge carriers in the system. The discrete nature of charge carrier transports causes the current to exhibit fluctuations in its intensity, leading to the manifestation of shot noise. Shot noise is described by Eq. 2. 21:

$$S_I = 2qI \qquad \text{(Eq. 2.21)}$$

In the room temperature, shot noise is low compared to thermal noise and becomes dominant at high currents. It can be observed at low temperature.

2.3.3 Generation-recombination noise

Generation-recombination (GR) noise arises because of carriers being dynamically trapped and de-trapped during the process of transportation. The random capture of charge can lead to localized fluctuations in various carrier properties, such as mobility, diffusion coefficient, electric field, barrier height, and depletion width, among others. The origins of GR noise can be attributed to four distinct factors. Firstly, there is the recombination of free electrons and free holes. Secondly, the generation of free electrons and free holes is another source of GR noise. The combination of these aforementioned factors produces GR noise. Additionally, electron trapping and de-trapping in trap sites also contribute to the overall GR noise. Finally, the trapping and de-trapping of holes in trap sites also play a significant role in the generation of GR noise.

PSD of the carrier number fluctuation in GR noise as follows:

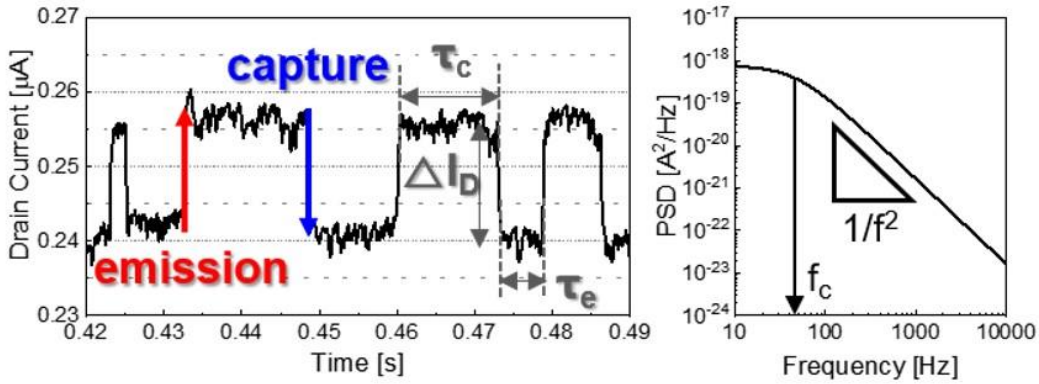

Figure 2.7 Typical RTS signal in the high-k Omega-gate MOSFET. And, schematic noise power density spectra: RTS signal described by a Lorentzian function with the corner frequency f_c, determined by the average capture and emission times of the trap [14].

$$S_N(f) = \frac{4\langle \Delta N_{trap}{}^2 \rangle \tau}{1+(2\pi\tau f)^2} \quad \text{(Eq. 2.22)}$$

where $\langle \Delta N_{trap}{}^2 \rangle$ is the variance of the total number of interface trap charges and τ the trapping time constant.

2.3.4 Random-Telegraph-Signal (RTS) noise and *1/f* noise

Random-Telegraph-Signal (RTS) noise can be considered as a special case of GR noise, which refers to the noise generated by the presence of a single trap. In situations where the number of traps is relatively low, the GR noise can present itself as RTS noise of many levels. This RTS exhibits a distinctive characteristic of having multiple quantized switching events occurring in the time domain. Furthermore, RTS noise is highly responsive to any bottlenecks that may occur in the carrier transport, such as poor contact, as well as the presence of interface states. These factors have been observed to have a significant impact on the generation and behavior of RTS noise [15].

The *1/f* noise, which is also commonly referred to as flicker noise or excess noise, is characterized by a PSD that is inversely proportional to the frequency. Although it has occasionally been labeled as low-frequency noise, this characterization is not entirely accurate, as there are other types of noise, such as GR or RTS noise, that can also be observed in the low-frequency region described as Eq. 2.23:

$$S_I = \frac{KI^\beta}{f^\gamma} \quad \text{(Eq. 2.23)}$$

where *K* is a constant, the current and frequency exponents, respectively. *1/f* noise is observed in the low frequency region (under 10^5 Hz). *1/f* noise is mainly understood through the carrier number fluctuation (CNF) model and Hooge mobility fluctuation (HMF) model.

The CNF (Carrier Number Fluctuation) model considers that 1/f noise in MOSFETs is the result of the trapping or de-trapping of carriers in the gate oxide or semiconductor channel interface. This phenomenon leads to fluctuations in the flat band voltage, which in

turn locally modulates the number of carriers and current. On top of that, the fluctuating trapped charge can induce mobility fluctuations near the trap. This modulation can be explained by combining the CNF model with the correlated mobility fluctuation model (CMF). The combined CNF+CMF model can be characterized by the normalized drain current noise.

$$\frac{S_{I_D}}{{I_D}^2} = (1 + \alpha\mu_{eff}C_{ox}\frac{I_D}{g_m})S_{Vfb}(\frac{g_m}{I_D})^2 \quad \text{(Eq. 2.24)}$$

where α is the remote Coulomb scattering parameter (Vs/C) and S_{Vfb} the flat band voltage PSD. S_{Vfb} is related to the charge fluctuation near interface, which is given as:

$$S_{Vfb} = \frac{q^2 K_B T \lambda N_t}{fWL{C_{ox}}^2} \quad \text{(Eq. 2.25)}$$

where λ is the oxide tunneling attenuation coefficient, N_t the volume trap density. CNF model is therefore sensitive to the quality of gate oxide and channel interface.

The mobility fluctuation model, proposed by Hooge in 1972 [16], is an empirical relationship that seeks to establish a correlation between the magnitude of the 1/f noise and the number of free charge carriers. This model is simply described as:

$$\frac{S_{I_D}}{{I_D}^2} = \frac{S_R}{R^2} = \frac{\alpha_H}{Nf} = \frac{q\alpha_H}{WLfQ_i} \quad \text{(Eq. 2.26)}$$

where *N* is the total number of free carriers and α_H the phenomenological parameter called as Hooge parameter, and Q_i the inversion charge density per effective device area. The Hooge parameter, initially regarded as a universally applicable constant with a value of ~2×10^{-3} for all materials, was eventually found to have large variations from case to case. Hooge, in his initial proposition, suggested a model specifically for homogeneous bulk systems. Subsequently, the Hooge mobility fluctuation model emerged as differentiating itself from mobility fluctuations caused by the scatterings arising from trapped charge carriers located at the oxide-semiconductor interface.

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Chapter 3. Current Variability in 2-vertically Stacked Nanosheet FETs on FDSOI

3.1 Introduction

The impact of fluctuations in the design and functioning of devices and circuits was not as obvious as it is now. However, as CMOS technology has progressed into the deep submicron pitch distance, these effects have become increasingly prominent. In fact, they have reached a level of significance where they are now acknowledged as a major hurdle to the further scaling of technology.

Since the inception of FinFETs, the multi-gate structure has been widely recognized as the prominent technology solution for further scaling down of integrated circuits [1]. To achieve better gate control of the channel, gate-all-around (GAA) nanowire (NW) or nanosheet (NS) FETs [2] have been developed for the next generation sub-15 nm CMOS technology for nodes, showcasing enhanced metrics of performance, including I_{on}/I_{off} ratio, and *SS* among other critical characteristics [2]. However, the aggressive scaling and the intricacy of the fabrication process have led to high levels of device-to-device variability [3], which has become a limiting factor for the performance of GAA NW-based circuits. Variability can be comprehensively categorized into two distinct classes, namely systematic variability, and random variability. The classification of variability into these two classes is contingent upon its underlying nature and the diverse sources from which it emerges. Systematic variability is a term that contains all variations in parameters that can be predicted and, as a result, can be represented and comprehended. On the contrary, random variability denotes any unexpected inconsistency caused by variations at the atomic level between indistinguishable devices. These mismatches may arise from random dopant fluctuation (RDF), line-edge roughness (LER), and variations in oxide film thickness amongst others [4]. Typically, the variability within a wafer is branched into local (intra-die variations) and global (inter-die variations). From the circuit design perspective, it is crucial to consider the

local variability (the difference between neighboring transistors of the same circuit). Nonetheless, global variability is also a crucial parameter for assessing and optimizing the process variation.

The requirement for the incorporation of a continuously growing quantity of elements, which exhibit strong efficiency in relation to driving current, power consumption, and reliability, has arisen in order to advance novel technologies and architectures. The limitations of conventional planar devices have been reached, primarily due to the impact of short channel effects (SCEs), particularly for gate lengths below 30 nm. The solution to these concerns materialized in the form of the FinFET, Gate-All-Around, Nanosheet, Nanowire structures or FDSOI, which offer better electrostatic control. Another innovative approach involves the 3D layering of devices. These techniques enable the advent of the next generation in circuits, as they fully exploit the 3rd dimension, resulting in a raising quantity of components without the need for any further reduction in area. A comprehensive study of FinFET and 3D stacking technologies has been conducted with the objective of evaluating their advantages across various fields.

In this chapter, we carried out on investigating the variability of the drain current, I_D, through measurements and model fitting in 2-vertically stacked GAA NW FETs [5]. Our primary objective is to identify the primary sources of parameter variations and their dependence on channel geometry.

3.2 Characterization of variability

Process variations are classified in two categories: intrinsic and extrinsic. Intrinsic process variation steps from atomic scaled effect like quantum-mechanical effects [6] and statistical effects in doping profile [7], typically. Extrinsic variations can be primarily attributed to any change in the conditions of the process. Such changes in process conditions can lead to fluctuations in parameters [8], resulting in a shift in the behavior of the system.

Process variations divided to: Lot to lot (L2L), Wafer to wafer (W2W) within a lot, Die to die (D2D) within a wafer, and within die. The variation occurring within a die are determined by certain parameters that exhibit significant variability across distances that are smaller in size than the overall dimensions of the die. Across a wafer, the randomly varies of parameters cause die to die variation. Because of different properties with wafers, wafer to wafer variation occurs.

The primary origins of fluctuations are associated with physical and chemical atomic-level occurrences, fabrication processes. Perhaps the primary reason for increased random fluctuations in device characteristics is the reduction of CMOS technology to sub-nm dimensions [9]. Another significant contributor can be attributed to the complicated and varied properties of the fabrication process, which consists of various steps. The process of implantation and annealing induces a stochastic distribution of dopants within the channel. Variations in the thickness of the oxide layer are given rise to the lack of uniformity in the growth process. Furthermore, the non-uniform annealing temperature can lead to additional fluctuations in V_{th}. Moreover, the presence of strain and stress engineering can apply an influence on the mobility of carriers [10]. The process of lithography and the etching effects that occur during these processes have been found to induce variations in the critical sizes of devices such as the length and width of channels. These variations are observed to be significantly narrower in comparison to the wavelength of light that is utilized in the printing of these devices.

In Table 3.1, the various sources of systematic and random variability are summarized.

Table 3.1 Systematic and random variations of MOSFET parameters and their sources

Parameter	Systematic	Random
Effective channel length	Lithography and etching	LER
Doping concentration	Non-uniformity in implantation and annealing	RDF
Mobility	Variation in strain engineering	Random strain variation
Film thickness	Non-uniformity in oxide deposition, chemical-mechanical planarization	Surface roughness

Bulk and FDSOI devices may be affected by some sources of variability like effective channel length and mobility variation due to systematic and random variations. Especially, RDF is more effective because of the variation in channel doping concentration. In the case of FDSOI, RDF changes the effective channel length in the source and drain regions. On the other hand, since surface roughness changes the silicon film thickness, variation is expected to be more notable in ultra-thin BOX FDSOI [11, 12].

3.3 Experiments and methods

2-vertically stacked NW FETs were fabricated by CEA-LETI using the state-of-the-art FDSOI technology with process steps in Figure 3.1(a). To compose of two stacked Si channel, the fabrication starts with epitaxial growth of SiGe/Si multilayers. The thickness of each sacrificial SiGe and Si film is 9 nm, respectively. Through a sidewall image transfer (SIT) technique, the pattering of multilayers used to define, and a fin pitch is 35 nm as a result. The etching of SiO_2/poly-Si dummy gate on fin is performed. After fin patterning, a

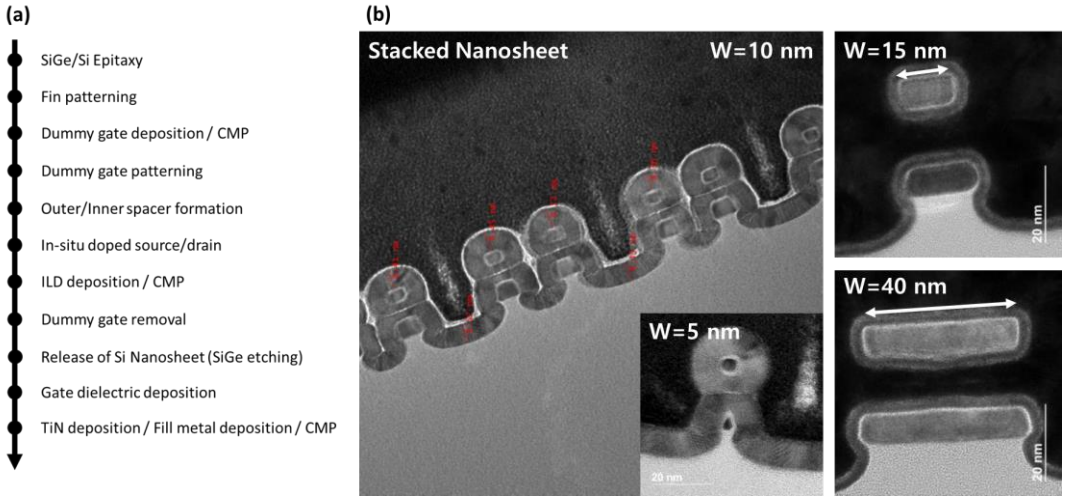

Figure 3.1 (a) The process flow of 2-vertically stacked NS FETs. (b) TEM images of GAA NS FETs with 2-vetically stacked channels: top wire has GAA structure and bottom one has Omega gate shape.

SiN spacer is fabricated prior to the anisotropic etching of the SiGe/Si fin in the source/drain regions. As a following of selective etching, the conformal deposition is carried out by a 2 nm HfO_2 dielectric, and a metal gate of TiN (2.2 nm), and Tungsten (where the equivalent oxide thickness (EOT) was 1.2 nm). Additionally, the buried oxide (BOX) thickness is 145 nm [5, 13].

Figure 3.2 Agilent B1500 semiconductor parameter analyzer and 300 mm Cascade MicroTech probe station

To exhibit the transfer characteristics, the gate voltage V_G was varied from 0 to 1 V, whereas the drain voltage V_D was kept constant at 30 mV in the linear regime. These measurements were conducted using Agilent B1500 Semiconductor Device Parameter Analyzer and Cascade MicroTech automatic probe station shown in Figure 3.2. To conduct a comprehensive statistical characterization of the global variability, static measurements were performed on over 90 dies, and problematic measurements were filtered out using I_{on}/I_{off} ratio, minimum of leakage current I_G.

3.3.1 Global variability

3.3.1.a Drain current mismatch model from linear to saturation regime

In order to validate a comprehensive model that accounts for the global variability in I_D,

it is necessary to consider the primary factors contributing to the global variability. These factors confine the sensitivity of I_D to the parameters of MOSFET, namely the threshold voltage V_{th}, the current gain factor β, and the series resistance R_{SD}. Consequently, by employing the first order Taylor approximation, the normalized fluctuation in drain current can be mathematically represented as the cumulative summation of the principal contributions as [14]:

$$\frac{dI_D}{I_D} = \left(\frac{1}{I_D}\frac{\partial I_D}{\partial V_{th}}\right) dV_{th} + \left(\frac{1}{I_D}\frac{\partial I_D}{\partial \beta}\right) d\beta + \left(\frac{1}{I_D}\frac{\partial I_D}{\partial R_{SD}}\right) dR_{SD} \qquad \text{(Eq. 3.1)}$$

The drain current mismatch in the linear regime is calculated by the summation of partial derivatives of I_D regarding V_{th}, β, and R_{SD} as follow Eq. 3.2:

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right) = \left(\frac{g_m}{I_D}\right)^2 \sigma^2(\Delta V_{th}) + (1 - G_d R_{SD})^2 \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + {G_d}^2 \sigma^2(\Delta R_{SD}) \qquad \text{(Eq. 3.2)}$$

where $\sigma^2(\Delta V_{th})$, $\sigma^2(\frac{\Delta\beta}{\beta})$, and $\sigma^2(\Delta R_{SD})$ are the variances of the threshold voltage, the gain factor, and source/drain series resistance, respectively, G_d the channel conductance in the linear region.

For the mismatch anaylsis, the methodology based on Y-function which is not affected by source/drain series resistance is useful approach in order to extract the standard deviations of V_{th} and β. According to previous research [15], the Y-function mismatch can be explained by inversion region above V_{th}:

$$\sigma^2\left(\frac{\Delta Y}{Y}\right) = \frac{\beta\sigma^2(\Delta V_{th})}{4\beta n^2\left(\frac{kT}{q}\right)^2 + Y^2} + \frac{1}{4}\sigma^2\left(\frac{\Delta\beta}{\beta}\right) \qquad \text{(Eq. 3.3)}$$

But the model in Eq. 3.3 is only valid in the linear operation regime. This methodology is functional to extract the standard deviation of V_{th} and β for using initial value to be fitting. To extend the mismatch model from linear regime to saturation regime, new assumption is required as Eq. 3.4:

$$R_S = R_D = \frac{R_{SD}}{2} \qquad \text{(Eq. 3.4)}$$

the partial derivative of I_D with respect to R_{SD} is calculated by:

$$\frac{1}{I_D}\frac{\partial I_D}{\partial R_{SD}} = \frac{g_m}{2} + g_d \quad \text{(Eq. 3.5)}$$

where g_d is the output conductance.

In consequence, by combining Eq. 3.1 and Eq. 3.5, the drain current variability in both linear regime and saturation regime is described as:

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right) = \left(\frac{g_m}{I_D}\right)^2\sigma^2(\Delta V_{th}) + \left(1 - \left(\frac{g_m}{2} + g_d\right)R_{SD}\right)^2\sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \left(\frac{g_m}{2} + g_d\right)^2\sigma^2(\Delta R_{SD}) \quad \text{(Eq. 3.6)}$$

The device channel width *W* and length *L*, which were the key parameters under investigation, spanned a considerable range of 10-20 nm and 15-200 nm, respectively. Figure 3.3 displays a representation of typical linear and logarithmic scaled plots of I_D-V_G characteristics for various geometries on PMOS at linear regime (V_D=-30 mV). It is evident that shorter *L* geometries on both of *W* (10 and 20 nm) indicate an increase in the variability of device characteristics. In particular, at *L*=15 nm device, electrical characteristics exhibit a large variation of on/off currents and threshold voltage V_{TH}, regardless of the device *W*.

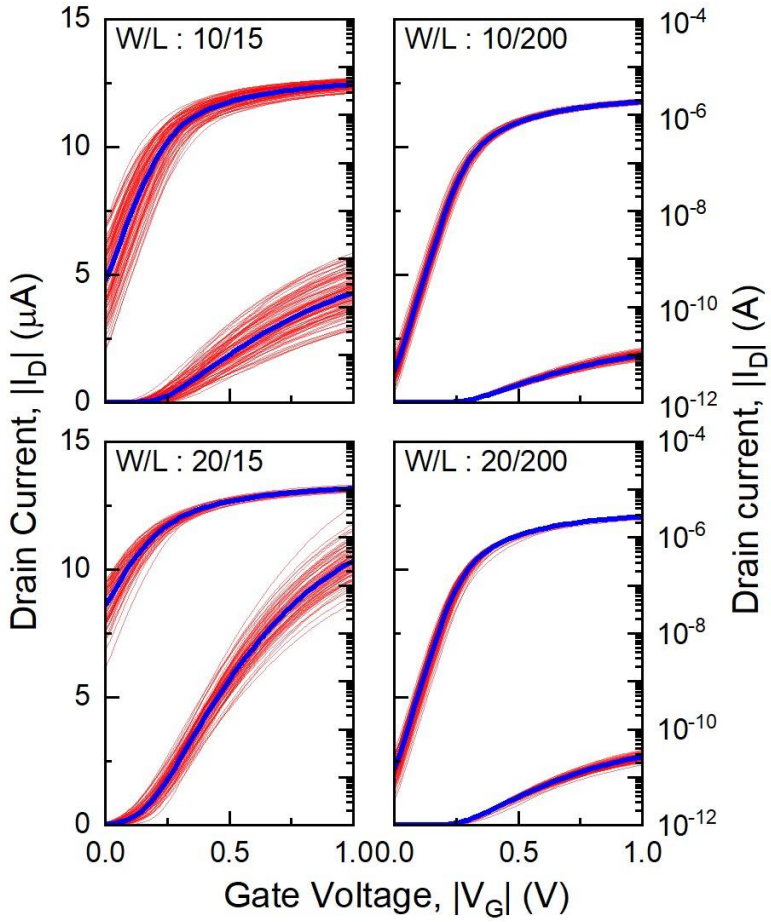

Figure 3.3 Typical I_D-V_G characteristics (red line) for various geometries on over 90 dies and average values (blue) on measured devices with W=10, 20 nm and L=15, 200 nm.

Furthermore, when comparing W=10 mm with the same device L, the W=20 mm device exhibits high off current values. It appears to be quite challenging to optimize the device fabrication processes in aggressively scaled geometries.

The calculation of the conventional intra-die local variability of I_D can be achieved by utilizing the logarithmic difference between two drain current values for the matching pair devices within the same die [15, 16]:

$$\frac{\Delta I_D}{I_D} = \ln\left(\frac{I_{D2}}{I_{D1}}\right) \quad \text{(Eq. 3.7)}$$

On the contrary, the inter-die global variability can be performed by utilizing the average value obtained from all the measure curves:

$$\frac{\Delta I_D}{I_D} = \ln\left(\frac{I_D}{I_{D,average}}\right) \quad \text{(Eq. 3.8)}$$

especially when only one current is obtained per die where $I_{D,average}$ is the average drain current across the wafer. The global variability of the shortest device with L=15 nm and W=10 nm is at least three times larger than that of the longer channel device with L=200 nm, as depicted in Figure 3.4. This is mainly due to the relatively low V_{TH} for W/L=20 nm/15 nm, which results in lower variability compared to W=10 nm. According to Pelgrom's law [17], the drain current global mismatches for larger area devices are significantly lower.

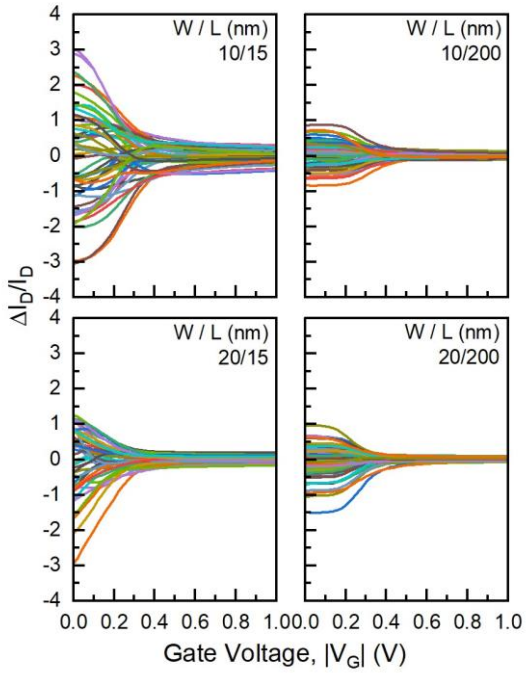

Figure 3.4 Drain current mismatch of NW FETs according to gate voltage on various geometries.

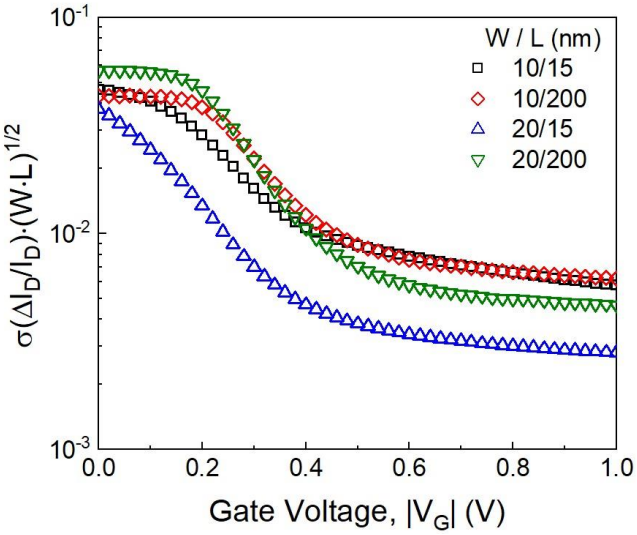

Figure 3.5 Normalized standard deviations of the drain current mismatch for different geometries in linear region.

In accordance with the visual representation delineated in Figure 3.5, the normalized standard deviations of the drain current mismatch are distinctly exhibited across an array of distinct geometries. Even though normalization has been rigorously administered in order to accommodate for variations in geometries, it is noteworthy to acknowledge that the area normalized standard deviation corresponding to the device with W/L=10 nm /15 nm is of a greater magnitude when contrasted with the standard deviations associated with the other geometries.

The variances of I_D mismatch as a function of V_G for various geometries are graphically represented in Figure 3.6. The experimental data, indicated by symbols, and the variability model (Eq. 3.6) fitting, represented by lines, exhibited a satisfactory agreement from weak to strong inversion within all cases of devices [18]. Irrespective of device W, relative I_D variances similarly decrease in the high inversion region. This phenomenon could be explicated by the terms of standard deviations with V_{TH} and β being dominant to the variability model following V_G. Furthermore, the variances of short devices L=15 nm have

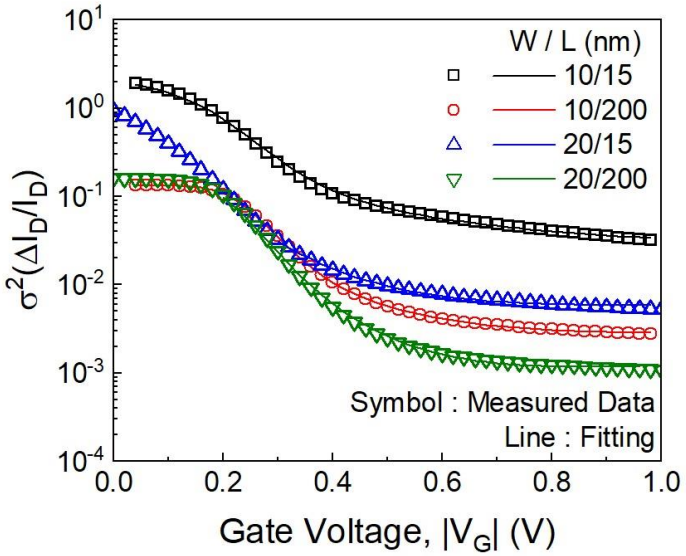

Figure 3.6 Mismatch variance versus gate voltage for different geometries. Mismatch fitting model (line) has a good agreement with experimental results (symbol)

approximately one decade larger than those of long channel devices. Furthermore, good agreement between experimental and model results indicates that the effect of ΔR_{SD} might be saturated in high inversion region regardless of device area. This phenomenon can be interpreted through the last term of Eq. 3.6, indicating that drain current in linear regime is very sensitive to R_{SD} effect where output conductance is relatively larger than transconductance.

The individual matching parameter $iA_{\Delta V_G}$ is described for various dimensions in the linear regime as Eq. 3.7. It is a way to express all area-normalized variations as gate voltage perturbations (input-referred variability).:

$$iA_{\Delta V_G} = [\sigma(\frac{\Delta I_D}{I_D})/(\frac{g_m}{I_D})] \cdot \sqrt{WL} \qquad \text{(Eq. 3.9)}$$

At low gate voltage below 0.4 V, the plateau is related to the individual matching parameters in Eq. 3.10:

$$iA_{\Delta V_{th}} = \sigma(\Delta V_{th}) \cdot \sqrt{WL} \qquad \text{(Eq. 3.10)}$$

The irregular behavior of $iA_{\Delta V_G}$ is observed in *W/L*=20/15 (nm/nm) due to relatively low threshold voltage compared to different dimensions. Below V_G= 0.3 V, the $iA_{\Delta V_G}$ drops from 1.6 to 1.1 continuously. Comparing to *W*=10 nm device with *L*=15 nm, despite gate stack composes of gate-all-around or omega-gate shape, bottom channel doesn't enclose perfectly unlike top channel. It might mean that channel of bottom nanosheet doesn't achieve volume inversion because it suffers from relatively higher short channel effect (SCE).

The standard deviations of each parameter were extracted by the variability model for the linear regime, as presented in Figure 3.8. In addition, all standard deviations have similar trends following the device area according to Pelgrom's law.

$$\sigma_{\Delta S} = \frac{A_S}{\sqrt{WL}} \qquad \text{(Eq. 3.11)}$$

where *S* is the electrical parameter of MOSFET, and A_S the Pelgrom coefficient of electrical parameter that has strong dependency on fabrication processes. Three different $A_{\Delta V_{th}}$, $A_{\Delta\beta/\beta}$, and $A_{\Delta R_{SD}/R_{SD}}$ are extracted from the standard deviation of each parameter-$(WL)^{-1/2}$

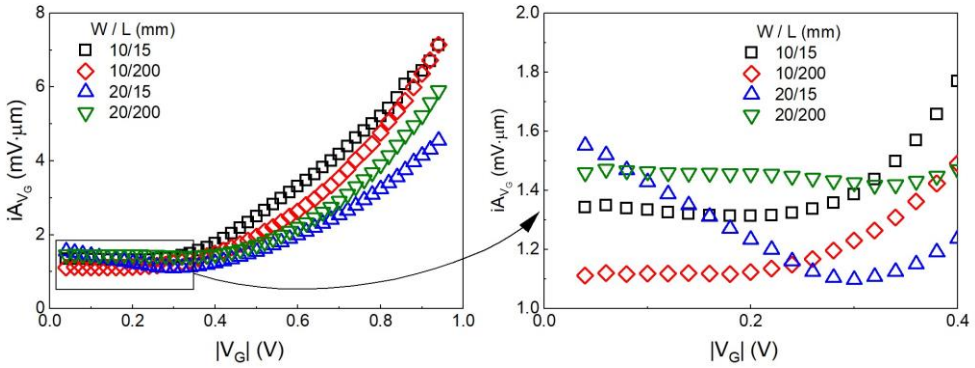

Figure 3.7 Individual matching parameter $\boldsymbol{iA_{\Delta V_G}}$ versus gate voltage V_G extracted by measured data for various geometries.

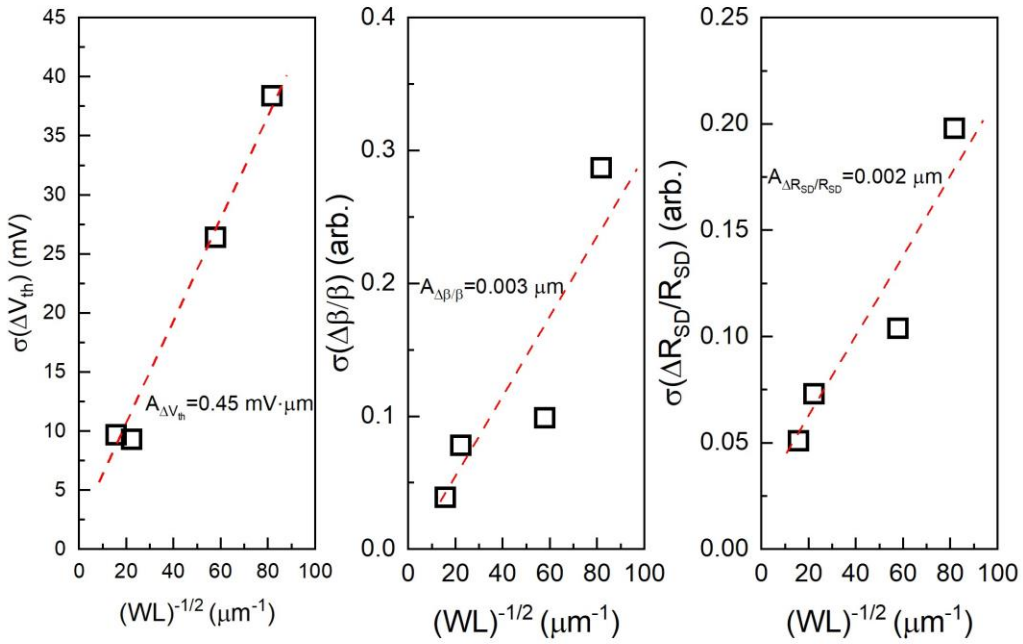

Figure 3.8 The standard deviations of each electrical parameter-$(WL)^{-1/2}$ and straight line for extracting the Pelgrom's coefficient A_s

characteristics. Especially, $A_{\Delta V_{th}}$ equal to 0.45 mV·μm is valid and relatively smaller comparing to previous research ($A_{\Delta V_{th}}$ is in the range between 2 and 6.5 mV·μm) [15, 19]. In this experiment, due to aggressive scaling down (GAA, NS, vertical stacked channel, etc) and complicated fabrication processes (difficulty of gate stack composition, effective device dimension, etc), $A_{\Delta V_{th}}$ can be increased. $A_{\Delta\beta/\beta}$ is 0.3 %·μm with a good agreement to range between 0.4 to 0.6 %·μm [20].

Figure 3.9 shows the standard deviation of ΔV_{TH} and $\Delta n/n$ for all measured devices, as extracted by the model, plotted versus the inverse square root of effective gate area, with which there should be a linear trend according to Pelgrom's law [17], if the local (die-to-die) variations are dominant. However, in the extracted data presented here, there seem to be three different slopes for $\sigma(\Delta V_{TH})$ and $\sigma(\Delta n/n)$. This can be clarified by individually plotting the same data versus the inverse square root of every dimension (W_{eff} and L) as shown in

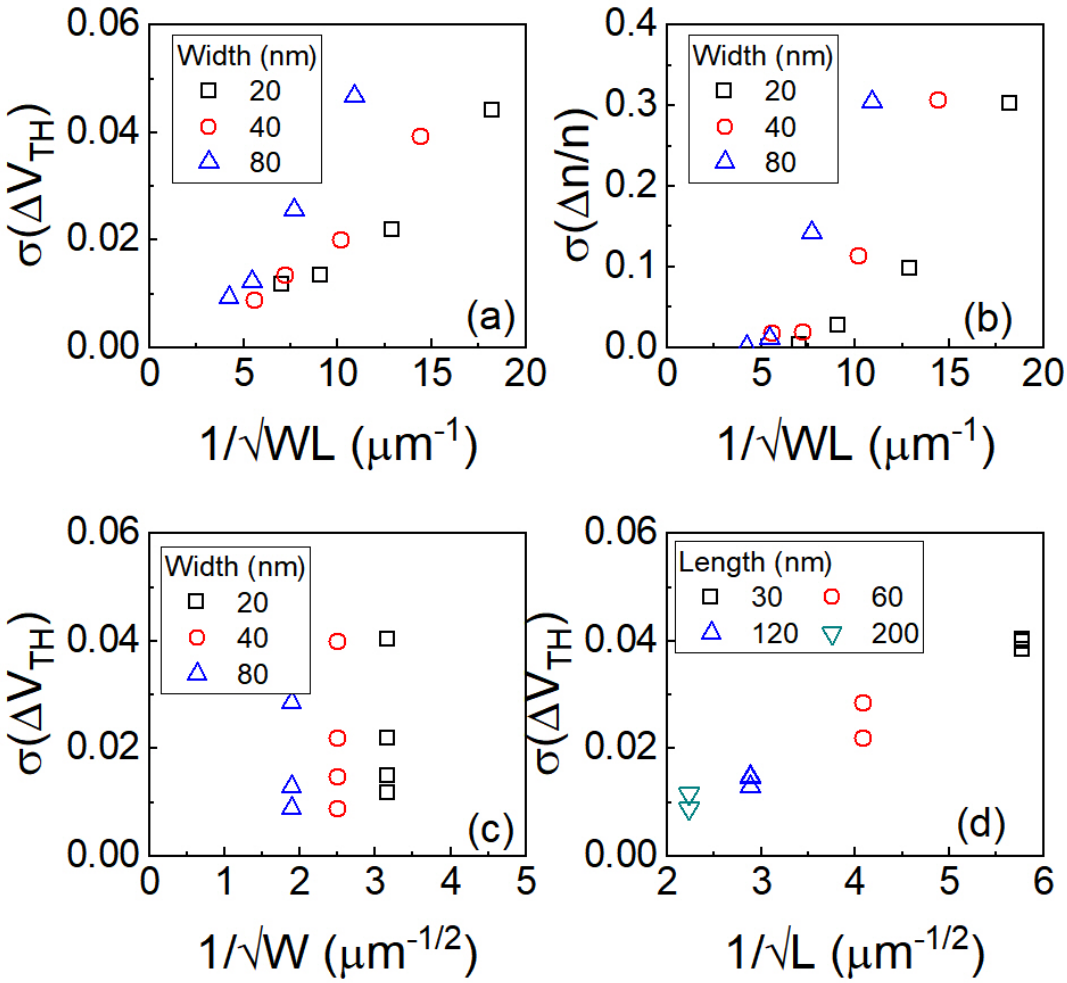

Figure 3.9 Standard deviation of Mismatch parameters versus the inverse effective area, (a) V_{TH}, and (b) ideality factor, respectively. Standard deviation of V_{TH} vs. (c) reverse of effective width, and (d) reverse of length, respectively.

Figure 3.9 (c), (d). There are four groups of nearly identical $\sigma(\Delta V_{TH})$ values which together are inversely proportional to $1/\sqrt{L}$ regardless of the variation on W_{eff}. Therefore, only the length dependence follows Pelgrom's law, meaning that the local process variations of L are the dominant source of threshold voltage and ideality factor variability [17]. Concerning the standard deviations of ΔR_{SD} and $\Delta\beta/\beta$, they were found to be negligible in these devices,

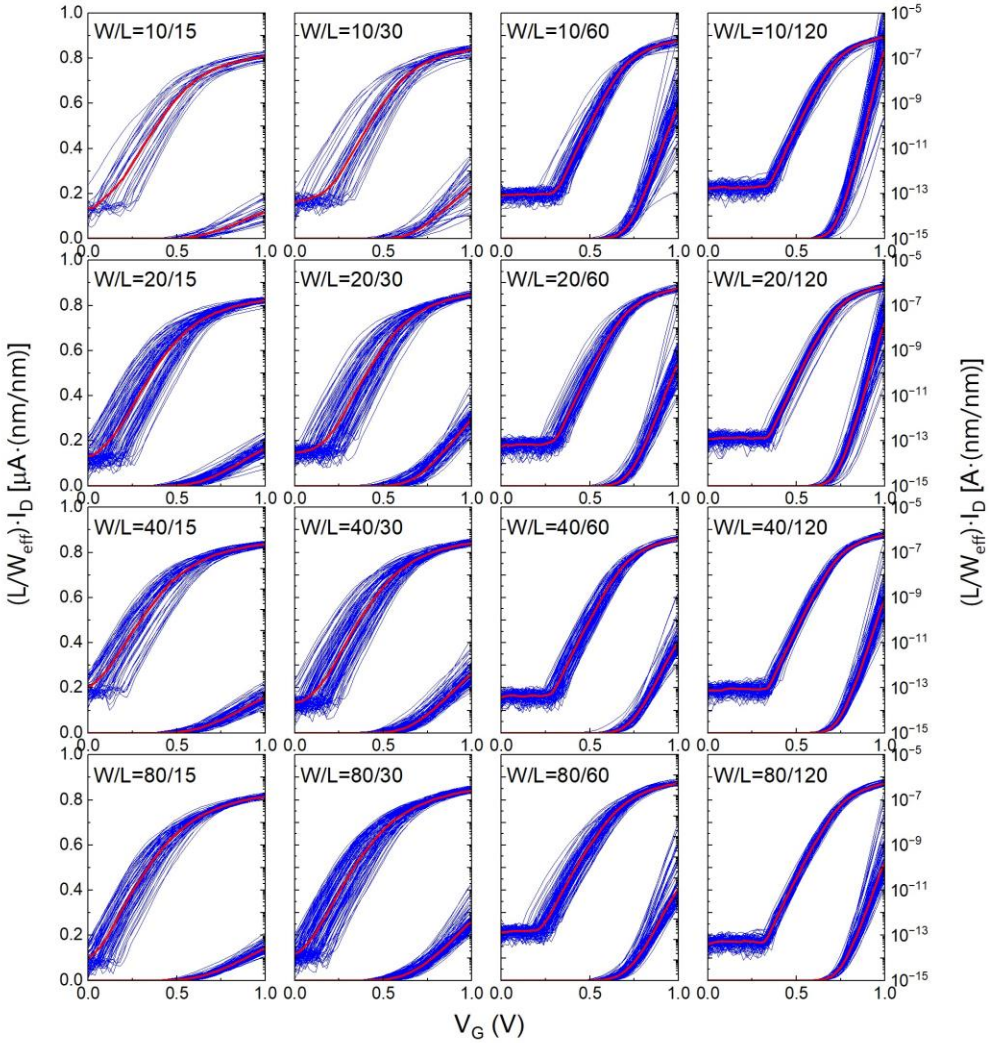

Figure 3.10 The linear and log scaled transfer characteristics of 2-vertically stacked NS MOSFETs with variations *W*=10, 20, 40, and 80 nm and *L*=15, 30, 60, and 120 nm. Drain current measurements were carried out on pairs of 165 over 300 mm whole wafer.

probably because their V_{TH} is roughly over 0.5 V and the range of measurement (0~1 V) might have been insufficient to obtain the effect of R_{SD} and mobility degradation.

3.3.1.b Drain current variability including all drain current mismatch sources

In the previous section 3.4.1, in order to validate the drain current variability model of Eq. 3.6, the partial derivatives of the drain current calculated for extracting three parameters (V_{th}, β, and R_{SD}) corresponding to I_D with PMOSFET. In the case of PMOS, because of low threshold voltage, there is no sensitivity of variability in the region of low gate voltage which is related to *SS*. Accordingly, it is required to extend the variability model including all the crucial sources of drain current:

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right) = \left(\frac{g_m}{I_D}\right)^2 \sigma^2(\Delta V_{th}) + (1 - g_d R_{SD})^2 \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + g_d{}^2 \sigma^2(\Delta R_{SD}) +$$
$$[\ln(\frac{I_D}{I_{D,th}})]^2 [\exp\left(-\frac{I_{D,th}}{I_D}\right) - 1]^2 \frac{(\sigma(\Delta n))^2}{n^2} \qquad \text{(Eq. 3.12)}$$

where $I_{D,th}$ is the constant current value near threshold voltage and n the ideal factor which the subthreshold swing variability is expressed by:

$$n = \frac{q}{kTSS} \qquad \text{(Eq. 3.13)}$$

Consequently, the electrical matching parameters ($\sigma(\Delta V_{th})$, $\sigma\left(\frac{\Delta\beta}{\beta}\right)$, $\sigma(\Delta R_{SD})$, and $\sigma(\Delta n)$) affects the variability model.

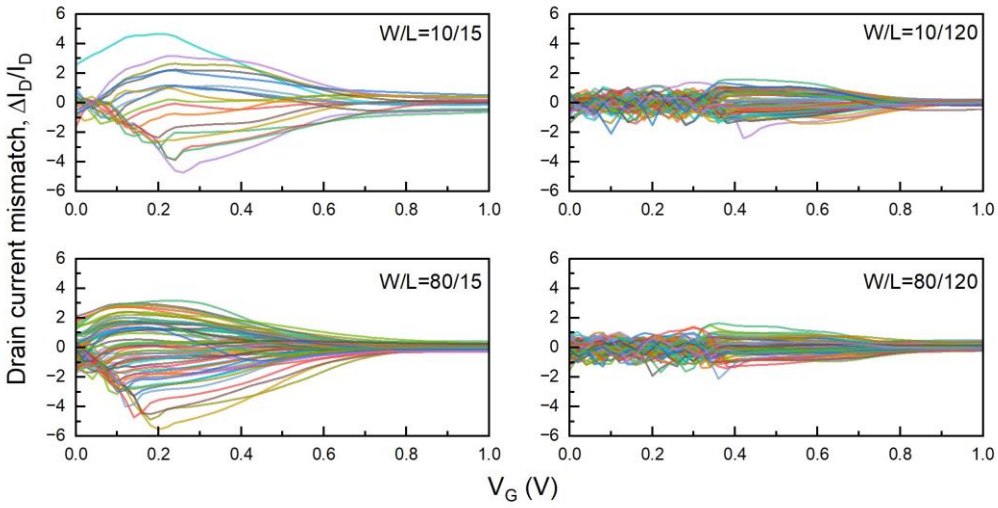

Figure 3.11 Drain current mismatch curves as a function of gate voltage with different dimensions.

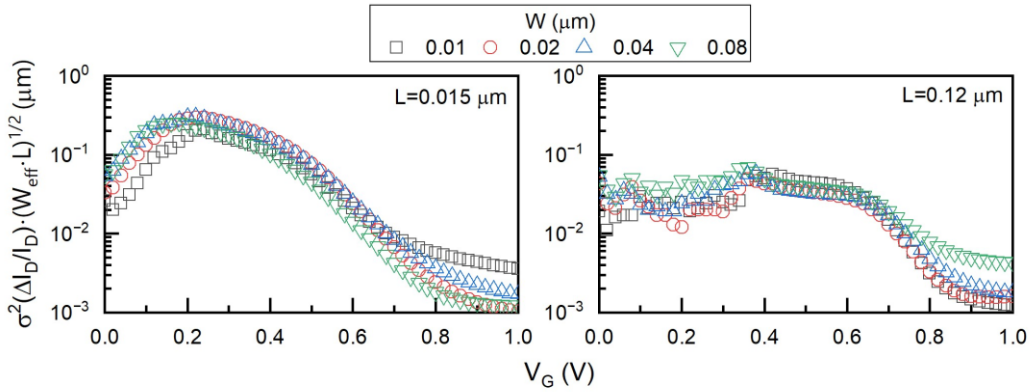

Figure 3.12 Drain current mismatch variance with normalization of effective device area as a function of gate voltage.

The transfer characteristics were measured in linear regime (V_D=30 mV) with in the range of V_G=0~1 V. The channel width has variation from 10 to 80 nm. And, the channel length varies from 15 to 200 nm. In Figure 3.10, typical transfer characteristics for various dimensions are presented. Drain current are normalized by calculated effective width W_{eff} (W_{eff}=top channel($2\cdot T_{Si}+2\cdot W$)+bottom channel($2\cdot T_{Si}+W$)) and L based on 2-vertically stacked channel structure in Figure 3.1.

The drain current mismatch is calculated by using the logarithmic difference between each drain current I_D and average drain current $I_{D,average}$ in Eq. 3.6 and presents in in Figure 3.11. The drain current variability of the short device with L=15 nm is larger than that of the longer channel device with L=200 nm with the devices W=10 and 80 nm. In the range of subthreshold below V_G=0.5 V, drain current variation increases following decreasing gate

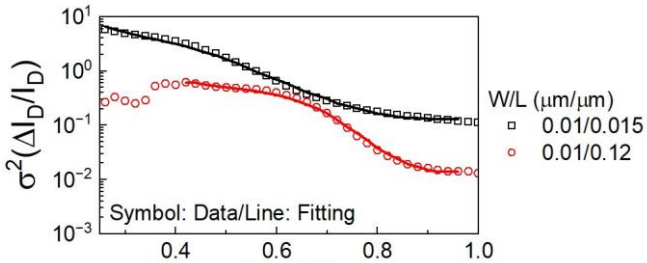

Figure 3.13 A good agreement with experimental results (Symbol) and fitting (line) with Length variation 0.015 and 0.12 μm with fixed width=0.01 μm**.**

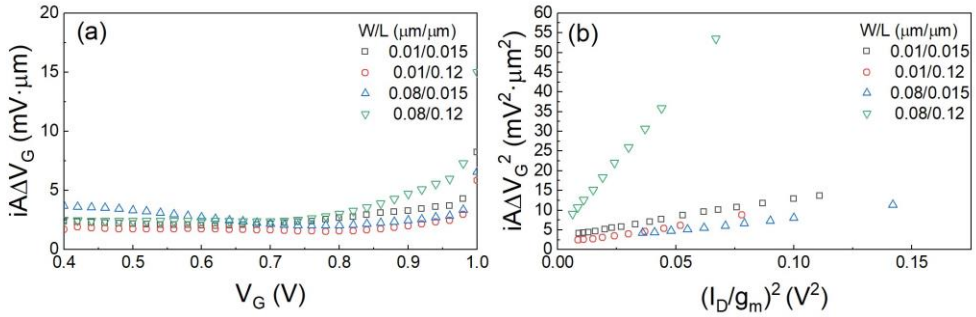

Figure 3.14 (a) the induvial matching parameter, $iA\Delta V_G^2$ as a function of gate voltage, (b) Individual matching parameter vs. extracted by experimental data, $(I_D/g_m)^2$ with various device geometries.

voltage. It might be caused by the crucial variations of threshold voltage and ideality factor. To quantify the major factors of drain current variation, the standard deviation of its mismatch was calculated with normalization effective square root device dimension $(W_{eff}\cdot L)^{1/2}$ [21]. As shown in Figure 3.12, the normalized standard deviation of the drain current mismatch as a function of gate voltage is illustrated for various devices (short and long length with narrow and relatively wide width) at linear regime (V_D=30 mV). In the range of subthreshold between 0 to roughly 0.5 V, the variances of drain current mismatch at the case of short length (L=0.015 μm) is higher than that of long length (L=0.12 μm).

In order to validate the role of electrical mismatch parameters (V_{th}, β, R_{SD}, and n) in Eq. 3.8, the experimental results were fitted in linear regime using the Levenberg-Marquardt and 4 fitting parameters. A good agreement between drain current variability model and experimental results were obtained in Figure 3.13.

The gate input referred normalized match parameter, $iA\Delta V_G^2$ extracted by Eq. 3.7, were calculated with various device dimensions. As shown in Figure 3.14(a), the properties of $iA\Delta V_G^2$ as a function of gate voltage are presented. Unlike previous PMOS trend (continuously increasing in high inversion region), in section 3.4.1, it might be difficult to observe the impact of series resistance. By using linear fitting, $iA_{\Delta Vth}$ and effective $iA_{\Delta\beta/\beta}$ can

be extracted for various device dimensions in Figure 3.14(b). It is necessary to compare the standard deviations from matching model in Eq. 3.8 to linear fitting.

The influence of individual standard deviations with four parameters (V_{th}, β, R_{SD}, and n) is calculated by using the ratio of each standard deviation. Mainly, the drain current variability can be affected by threshold voltage in all measurement region. Based on the threshold voltage, ideality factor changes dramatically, which is highly sensitive to subthreshold region. The influence of series resistance and gain increases in proportional to gate voltage as shown in Figure 3.15.

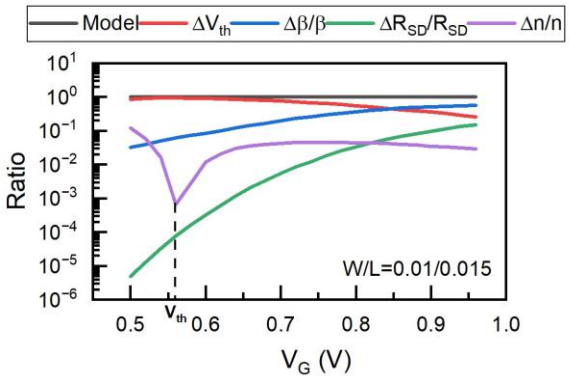

Figure 3.15 The ratio of each term in the drain variability model.

3.3.2 Low Frequency noise variability in 2-vertically stacked Nanosheet FETs

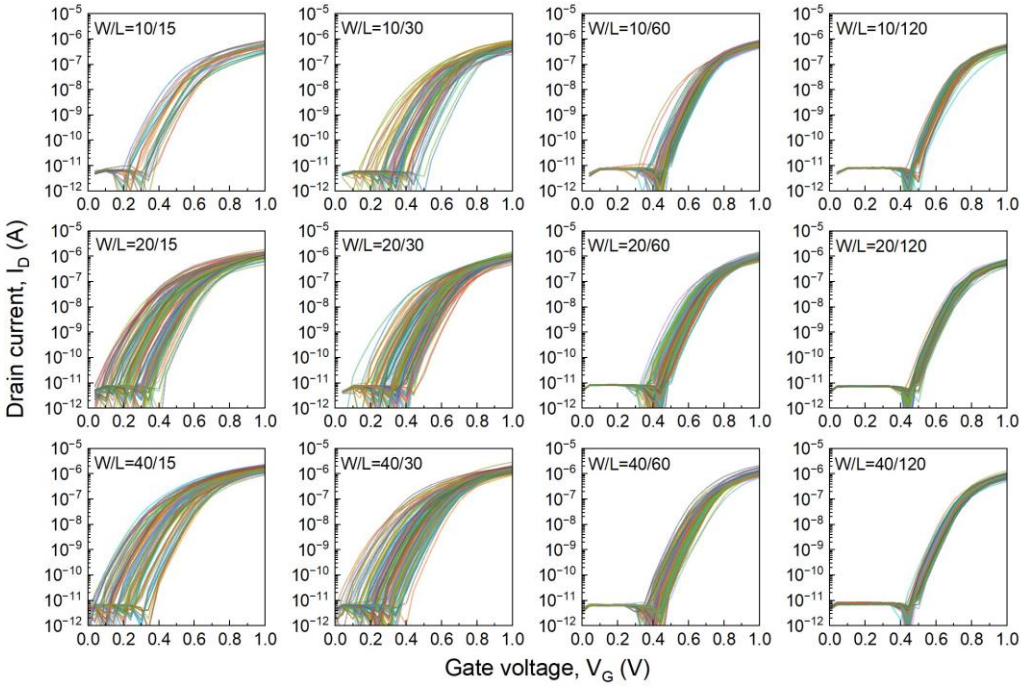

Figure 3.16 The transfer characteristics of 2-vertically stacked nanosheet FETs with various dimensions.

In this section, the Low frequency noise (LFN) characterization as a tool to evaluate 2-vertical stacked nanosheet (NS) FETs on FDSOI in terms of the quality of the gate oxide interface is investigated. Through the extraction of noise parameters (S_{vfb}, N_t and Ω) by utilizing the 1/*f*-like portion of LFN, comparative experimental investigation is carried out. Through this approach, it is possible to obtain an initial understanding of the fabrication steps that are potentially accountable for the performance degradation of the devices in relation to LFN, which could have a crucial impact on the reliable function of circuits.

3.3.2.a Experiments and methods

Drain current noise measurement were carried out on NMOS and PMOS transistors in FDSOI which is issued in chapter 3. As shown in Figure 3.16, the variation between die to die with transfer characteristics is illustrated. Because of high variations in the threshold voltage, large drain current variability is observed in the range of subthreshold.

Comparing to the drain current variations, the variation of g_m/I_D with various geometries has relatively low levels in Figure 3.17. To comprehend the source of the variability in drain current noise, it is necessary to review the prevailing model employed to elucidate the LFN in MOSFETs. Though the carrier number fluctuation (CNF) model, the normalized drain current noise $S_{I_D}/I_D{}^2$ is proportional to $(g_m/I_D)^2$ in Eq. 3.14 [22]:

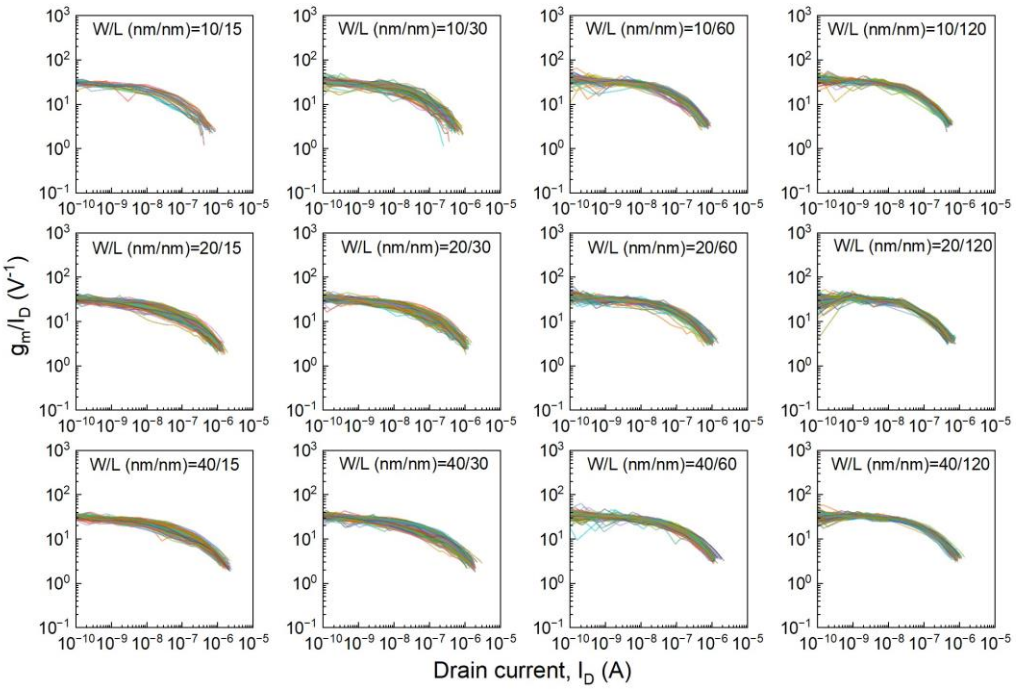

Figure 3.17 The g_m/I_D of 2-vertical stacked nanosheet FETs with various dimensions. The dispersion of g_m/I_D considers negligible comparing with drain current variation.

$$\frac{S_{I_D}}{{I_D}^2} = S_{V_{fb}} \cdot (\frac{g_m}{I_D})^2 \quad \text{(Eq. 3.14)}$$

where $S_{V_{fb}}$ is the flat-band voltage power spectral density.

The input-referred gate voltage noise, S_{V_G}, is described as:

$$S_{V_G} = \frac{{S_{I_D}}/{{I_D}^2}}{({g_m}/{I_D})^2} \quad \text{(Eq. 3.15)}$$

where S_{I_D} is the drain current power spectral density in the unit of A^2/Hz. By applying this approach, the noise variability in device-to-device is not influenced by the variation in threshold voltage, incorporated within g_m/I_D. The advantage of S_{V_G} is to utilize the noise modeling for simulation. In fact, inserting a voltage source into a gate is easier than inserting a current noise source into a drain because it can be affected by the device transconductance g_m or current I_D [22].

As shown in Figure 3.18, the input-referred gate voltage noises for dies are illustrated

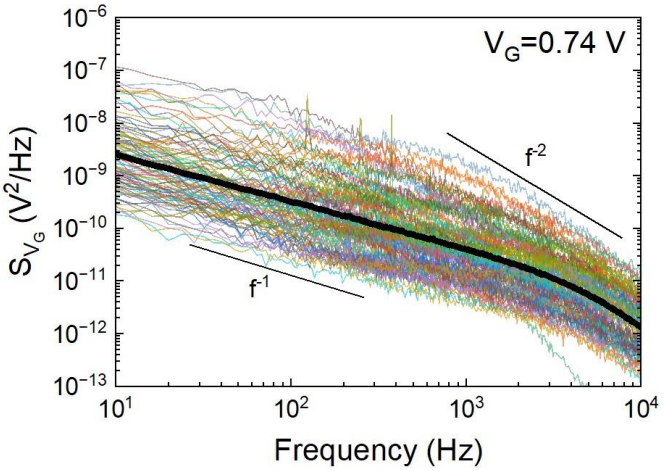

Figure 3.18 The input-referred gate voltage noises with V_G=0.74 V (various colored lines) and logarithmic average gate voltage noise (black line) in the case of device geometry (W/L=0.01/0.12 μm/μm).

as a function of frequency with gate voltage V_G=0.74 V. As the frequency increases, the variation of S_{VG} becomes smaller from 4-order at 10 Hz to approximately 2.5-order when the frequency is 10 kHz. Above the specific frequency f_c, the f^{-2} behavior is observed that typically occur in extreme scaling down device because of random telegraph noise (RTN) caused by carrier trapping and de-trapping phenomena in single trap existing interface near gate oxide and channel [23-25]. Also, it is caused by generation-recombination (GR) in the channel [26-28]. The logarithmic average noise spectrum in Figure 3.17 (blue line) behaves f^{-1} until f=2 kHz, but it follows f^{-2} behavior due to the influence of RTN or GR.

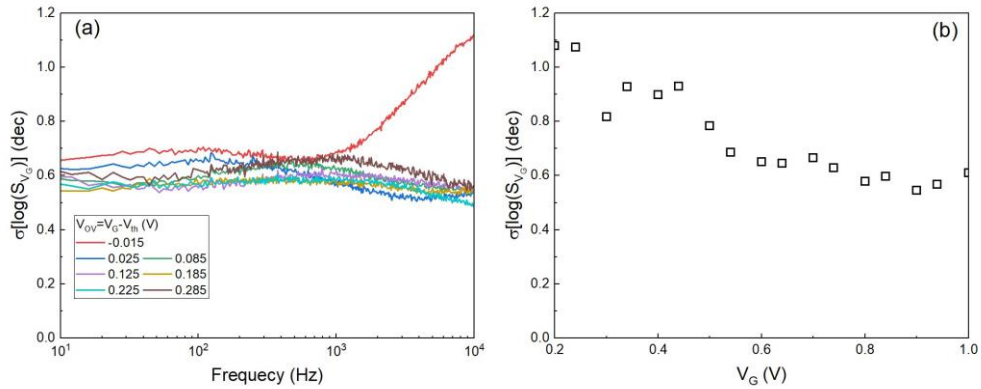

Figure 3.19 The logarithmic standard deviation of input-referred gate voltage noise vs. (a) frequency with 7 points of V_{OV}. (b) gate voltage V_G at f=10 Hz.

Figure 3.18 shows that the logarithmic standard deviation following frequency and gate voltage is calculated [29, 30]. In order to analyze the input-referred gate voltage noise variability, the logarithmic standard deviation $\sigma(\log(S_{V_G}))$ is considered in Figure 3.18(a). near threshold voltage V_{OV}=-0.015 V, the behavior of standard deviation changes dramatically above f=10 kHz. It might be caused by f^{-2} behavior due to the change of carrier transport affected by RTN or GR. The logarithmic standard deviation as a function of gate voltage is extracted at a certain frequency f=10 Hz as shown in Figure 3.18(b). As increasing of gate voltage, $\sigma(\log(S_{V_G}))$ decreases in the region of inversion, changing the value from 1.1 to approximately 0.6, almost 45 % decreasing.

The normalized $f \cdot S_{V_G}$ is illustrated in Figure 4.5 with different gate voltage in the range of inversion. The Lorentzian shaped spectra have peaks which is related to the corner (cut-off) frequency f_c of the Lorentzian as following gate volage. The correlated trap time constant τ is described by Eq. 3.16:

$$\tau = \frac{1}{2\pi f_c} \quad \text{(Eq. 3.16)}$$

$$\frac{1}{\tau} = \frac{1}{\tau_c} + \frac{1}{\tau_e} \quad \text{(Eq. 3.17)}$$

where τ_c, τ_e is the mean capture and emission time of the trap, respectively [31].

The emission and capture time of single trap rely on the carrier concentration in channel and electric field of gate oxide that is related to gate biases. Thus, the change of f_{peak} is observed in Figure 3.19. As shown in Figure 3.18(b), $\sigma(\log(S_{V_G})$ decreases with ascending of gate voltage, for the reason that as the corner frequency is in the range of high frequency, almost spectra of the input-referred gate voltage noise have closely f^{-1} behavior, it can be caused by the descending of $\sigma(\log(S_{V_G})$ as following the gate voltage [31].

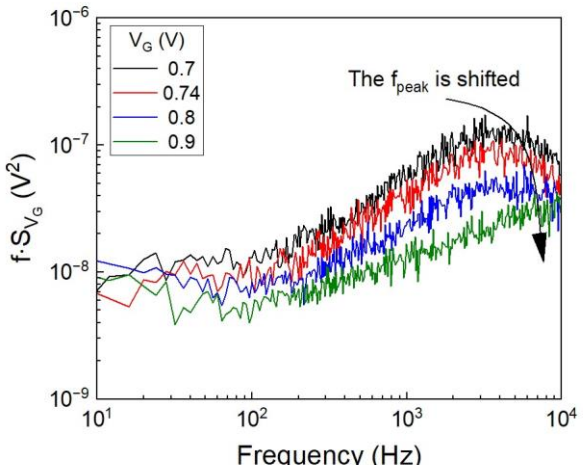

Figure 3.20 The normalization with frequency of input-referred gate voltage noise vs. frequency. There is the shift of f_{peak} following gate voltage increasing.

3.4 Conclusion

The main sources of drain current global variability have been investigated for 2-vertical stacked NS FETs on FDSOI. The main MOSFET parameters of global variability have been extracted to an analytical mismatch model in linear regime. Different model utilizes for the extraction of each standard deviation (V_{th}, β, R_{SD}, and n). At the case of PMOS, because of the insisting of low threshold voltage, ideal factor doesn't consider, which is very low sensitive in inversion region. Unlike in the case of PMOS, the global variability of NMOS confirmed the influence of the ideal factor, which changed significantly based on the threshold voltage.

The investigation of drain current mismatch in advanced GAA structure MOSFET on state-of-the-art FDSOI has been carried out. Despite extreme aggressive scaling down devices, the drain current variability model is valid and has a good agreement with experimental results. It is possible to implement in circuit simulation tools for circuit design through the drain current variability model explained by crucial parameters (V_{th}, β, R_{SD}, and n).

The investigation of the drain current noise variability is carried out with extreme scaling down devices like 2-vertically stacked nanosheet FETs on FDSOI. By using the input-referred gate voltage noise, it can be possible to analyze the noise variability which is not affected by transconductance and drain current. The average noise spectra in all range of gate voltage have f^{-1}-like behavior.

3.5 References

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Chapter 4. Detailed Electrical Characterization of 200 mm CMOS compatible GaN/Si HEMTs down to Deep Cryogenic Temperatures

4.1 Introduction

Cryogenic power electronics, which is an indispensable and pivotal technology, has been widely utilized in numerous applications such as electromechanical drives, transportation, renewable systems, and power networks [1-2]. This technology possesses immense potential to revolutionize the aforementioned fields by offering higher power density, greater efficiency, and superior performances. These superior performances can be attributed to the higher operation speed, lower power dissipation stemming from reduced voltage, better switching characteristics, shorter transmission times due to lower metal resistance, increased integration density, and better digital and analog device/circuit performances [1-2].

In recent times, GaN/AlGaN high electron mobility transistors (HEMTs) technology has emerged as a promising candidate in the field of cryogenic power electronics, especially for high frequency and high-power microwave applications, due to their high two-dimensional electron gas (2DEG) mobility when operated at very low temperatures [3-9]. However, despite the fact that several studies have already been reported about the cryogenic

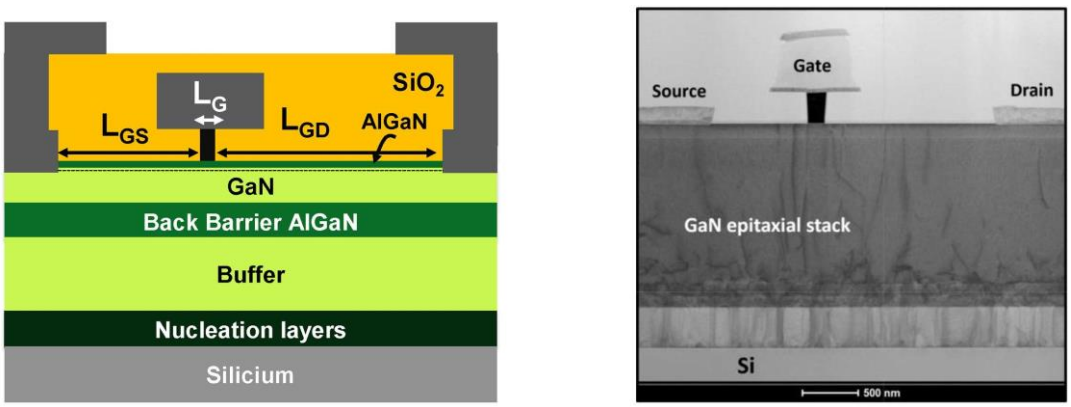

Figure 4.1 Schematic of the epitaxial stack and TEM cross section of GaN/Si HEMTs.

performances of GaN HEMT devices [10-13], there is still a lack of detailed analysis of the electronic properties of the channel and access regions under cryogenic operation. Therefore, in order to gain a more comprehensive understanding of this technology, it is imperative to conduct further research and investigation into the electronic properties of the channel and access regions under cryogenic operation.

In this present investigation, we hereby introduce, a comprehensive electrical characterization of the various transistor parameters (including, but not restricted to, mobility, saturation velocity, threshold voltage, subthreshold swing, source-drain resistance…) in relation to the gate length for gallium nitride high electron mobility transistors (HEMTs) that are operated at an frigid temperature of 10 K. Our research findings reveal that the mobility of the two-dimensional electron gas (2DEG) is escalated by the reduction of phonon scattering, and that the switching performance is substantially ameliorated at extremely low temperatures. Additionally, we propose the transmission line method (TLM) analysis of the source-drain series resistance, which is capable of distinguishing the contribution of contact and 2DEG access region resistances contingent upon the temperature.

4.2 Experiments and methods

The HEMT devices under investigation belong to a GaN technology processed on 200 mm silicon wafer designed for high frequency applications [14]. Figure 4.1 illustrates the device structure and cross section. The epitaxial stack was grown using metal organic vapor phase epitaxy (MOVPE) on a 200 mm high resistivity (111) silicon substrate. The structure consisted in transition layers and a 1.5 µm GaN carbon doped buffer layer followed by an AlGaN back barrier (300 nm) and a 150 nm unintentionally doped (UID) GaN channel. An AlN spacer (1 nm) and a thin $Al_{0.28}Ga_{0.72}N$ (7 nm) layer formed the barrier. A capping layer of 10 nm SiN was used for passivation. Ohmic contact formation began with passivation and AlGaN barrier etching before Ti/Al deposition, chemical mechanical polishing (CMP) and

annealing at 590 °C. Gate feet were patterned by e-beam lithography followed by passivation etching, TiN/W deposition and CMP. The gate head was formed by Ti/TiN/Al/TiN deposition and dry etching. Finally, vias were opened through the SiO_2 passivation and 1.4 µm Al deposition followed by lithography and dry etching formed the first level of interconnection. The test structure device gate length varied between L_g= 0.1 µm and 3 µm, the source-gate length L_{gs}=1 µm or 5.5 µm, the drain-gate length L_{gd}=1.5 µm or 5.5 µm. The device gate width was W_g=100 µm or 125 µm.

The I_d-V_g transfer characteristics were measured in linear (V_d=50 mV) and saturation (V_d=5 V) regions using an HP 4156B semiconductor parameter analyzer. The gate-to-channel capacitance C_{gc} was measured at room temperature with an HP 4284 LCR meter at a frequency of 1 MHz, providing here a maximum capacitance of about 0.9 µF/cm^2 above threshold, which is equivalent to an AlGaN/AlN thickness of about 8 nm. The cryogenic measurements were performed on a 200 mm liquid helium Susstec cryo-probe station with temperature varying between 10 and 300 K.

On one hand, the extraction of transistor parameter was carried out using the Y-function method, originally developed for Si MOSFETs [15] and recently validated on metal insulator semiconductor (MIS)-HEMT GaN devices at 300 K [16], which allows removing the influence of the source-drain series resistance R_{sd} as explained in Chapter 2 [15].

The R_{sd} is then extracted, in linear operation, from the plateau of the quantity defined below plotted in strong inversion,

$$R_{sd} = \frac{V_d}{I_d} - \frac{L_g}{W_g.C_{ox}.\mu_0.(V_g - V_{th})}, \quad \text{(Eq. 4.1)}$$

On the other hand, the transistor parameter extraction was performed using the Lambert-W function modelling approach developed for Si MOS transistors at 300 K [17] and recently extended at cryogenic temperatures [18]. In this case, the drain current in linear region including the R_{sd} influence is given by,

$$I_d = \frac{\frac{W_g}{L_g}\cdot\mu_0\cdot Q_i\cdot V_d}{1+R_{sd}\cdot\frac{W_g}{L_g}\cdot\mu_0\cdot Q_i} \qquad \text{(Eq. 4.2)}$$

where the inversion charge Q_i is modelled from weak to strong inversion as,

$$Q_i = C_{ox}\cdot\frac{n.kT}{q}\cdot LW\left(e^{\frac{V_g-V_{th}}{n\cdot kT/q}}\right) \qquad \text{(Eq. 4.3)}$$

where kT/q is the thermal voltage≈26 mV, *n* the subthreshold ideality factor and LW is the Lambert-W function [17]. This LW method presents the advantage to extract the MOSFET parameters over the full gate voltage range below and above threshold.

Finally, the Y-function method was applied in the saturation region for the extraction of the carrier saturation velocity v_{sat} as was originally demonstrated in Si MOSFETs [19]. In this case, Eq. 4.1 is used to extract the mobility degraded by the longitudinal electric field $E_l=V_d/L_g$, $\mu_{0d}=\mu_0/(1+\mu_0 V_d/(v_{sat}L_g))$, from the slope of the linear trend of $Y(V_g)$ characteristics measured in saturation, such that the saturation velocity can be obtained from [19],

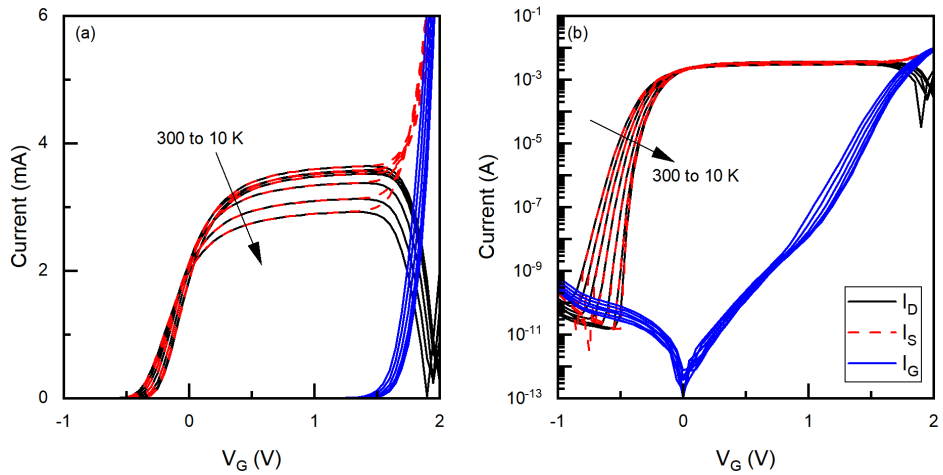

Figure 4.2. Typical I_d-V_g characteristics in linear (a) and log (b) scale as obtained on GaN/Si HEMT devices for various temperatures T=10, 50, 100, 150, 200, 250, and 300 K (V_d=50 mV, L_g=150 nm, L_{gs}=1 µm, L_{gd}=1.5 µm, W_g=100 µm).

$$v_{sat} = \frac{\mu_0 V_d}{L_g\left(\frac{\mu_0}{\mu_{0d}} - 1\right)} \quad \text{(Eq. 4.4)}$$

For comparison purpose, the saturation velocity was also extracted using the standard method based on the saturation drain current I_{dsat} and inversion charge at source terminal given by [19],

$$v_{sat} = \frac{I_{dsat}}{W_g.C_{ox}.(V_g - V_{th} - R_{sd}.I_{dsat})} \quad \text{(Eq. 4.5)}$$

where R_{sd} is the source/drain series resistance.

4.3 Results and discussion

4.3.1 Transfer characteristics

Typical drain and source current transfer characteristics I_d-V_g and I_s-V_g measured in the linear region (V_d=50 mV) are shown in Figure 4.2. They were obtained on GaN HEMT devices with a gate length of L_g=150 nm at various temperatures (10-300 K). As can be seen from the Figure 4.2, there was a strong gate current I_g for high gate voltage in such Schottky gate devices. Indeed, drain current I_d strongly differed from source current I_s for V_g>1.5 V. For this reason, the transistor parameter extraction was restricted to V_g up to 1 V in order to avoid any gate leakage influence.

Nonetheless, note that the I_d-V_g curves exhibited a very good behavior below threshold as the temperature was lowered with an improved subthreshold slope, specific of cryogenic operation. Note also that the I_d-V_g curves were saturating well above threshold due to the strong impact of the series resistance effect caused by the contact and access regions as will be discussed below.

The corresponding transconductance g_m-V_g and Y-function Y-V_g characteristics up to V_g=1 V are shown in Figure 4.3, illustrating the increase of the maximum transconductance

with temperature lowering and the linear behavior of Y-function well above threshold.

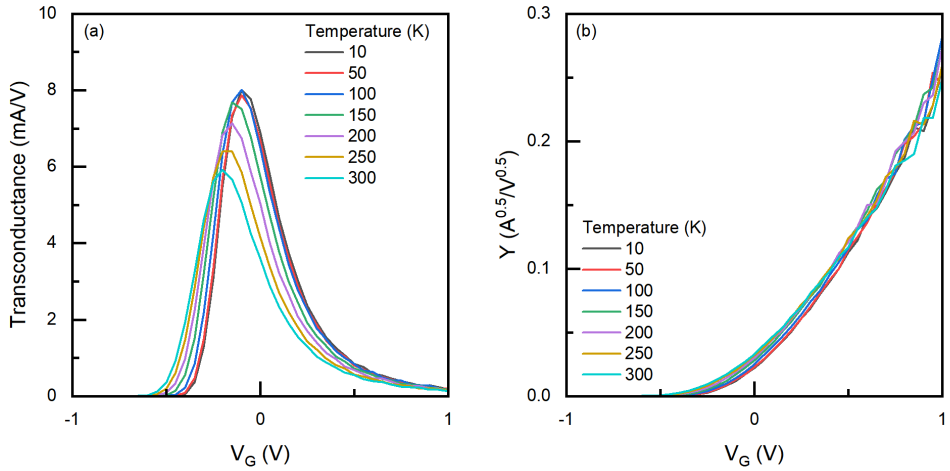

Figure 4.3. Typical g_m-V_g (a) and Y-V_g (b) characteristics as obtained on GaN/Si HEMT devices with various temperatures T=10, 50, 100, 150, 200, 250, and 300 K (V_d=50 mV, L_g=3000 nm, L_{gs}=1 µm, L_{gd}=1.5 µm, W_g=100 µm).

4.3.2 Y-function based transistor parameter extraction

Based on Eq. 2.8, the threshold voltage V_{th} and low field mobility μ_0 were extracted respectively from the x-axis intercept and slope of the Y-function linear trends above threshold [15], for each gate length and temperature. Figure 4.4 shows the variations with temperature of the obtained threshold voltage V_{th} and low field mobility μ_0 for various gate lengths. As expected from cryogenic operation, one observes a linear increase of V_{th} with

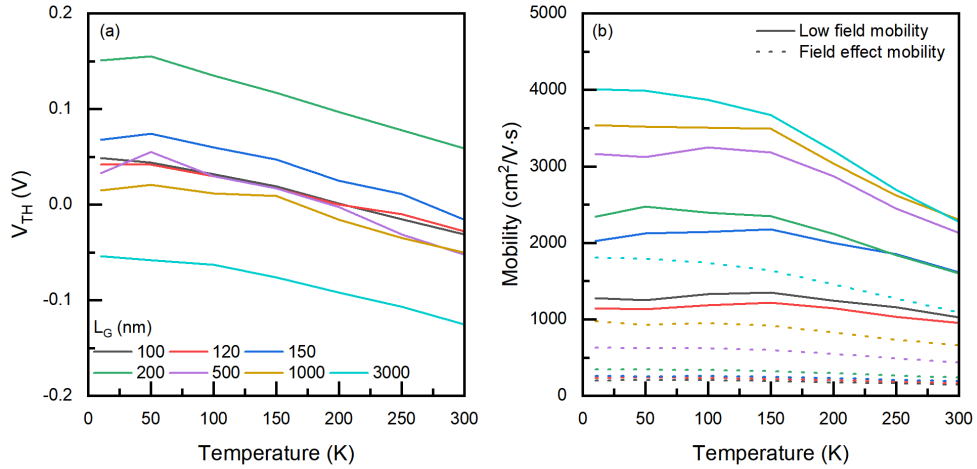

Figure 4.4. Variations with temperature of a) threshold voltage V_{th} and b) electron low field mobility μ_0 (red solid line) and μ_{femax} (blue dashed lines) as obtained on GaN/Si HEMT devices with various gate lengths L_g(nm)= 100, 120, 150, 200, 500, 1000 and 3000 (V_d=50 mV, L_{gs}=1 µm, L_{gd}=1.5 µm, and W_g= 100 µm)

temperature lowering due to carrier statistics evolution. Note also that the V_{th} roll-off versus gate length was nearly independent of temperature, as mainly arising from electrostatic-induced short channel effect as is usually observed in Si MOSFETs [20]. Moreover, the low field mobility μ_0 was also increasing with temperature reduction due to phonon scattering diminution, especially for long channel devices, where μ_0 improved from approximately 2000 $cm^2V^{-1}s^{-1}$ up to 4000 $cm^2V^{-1}s^{-1}$ for long channel, e.g. L_g=3000 nm. It should be mentioned that these mobility values are in good agreement with literature results obtained on GaN HEMTs by Hall effect or transistor parameter extraction [10, 21], pointing out the good quality of our GaN/Si technological process. In Figure 4.4(b) are also reported, for comparison purpose, the variations with temperature of the maximum field effect mobility deduced from the maximum transconductance and defined as $\mu_{femax}=g_{mmax}.L_g/(W_g.C_{ox}.V_d)$ [22], clearly revealing the huge underestimation of the mobility values obtained using this method, which is indeed inappropriate in the presence of large R_{sd} effect [23]. As can also be seen from Figure 4.4, the low field mobility μ_0 was significantly reduced as the gate length was decreased. This is better illustrated in Figure 4.5(a) where μ_0 has been plotted

versus gate length for various temperatures. It clearly appears that the low field mobility for short channel is much less temperature dependent than for long channels, revealing a clear change in scattering mechanism as reducing the gate length. Indeed, in long channels, μ_0 is likely dominated by phonon scattering explaining the mobility increase at lower *T*. Instead, in short channels, μ_0 is almost constant with temperature, which is indicative of neutral scattering domination as was observed in scaled Si MOSFETs [18]. Therefore, these low field mobility data versus temperature and gate length were tentatively modelled using the same approach employed in Si MOSFET, where the mobility can be described as [18],

$$\mu_{0,mod} = \left[\frac{1}{\mu_{ph}}.\left(\frac{T}{300}\right)^{\alpha} + \frac{1}{\mu_N}.\left(1+\frac{L_c}{L_g}\right)^{\beta}\right]^{-1} \qquad \text{(Eq. 4.6)}$$

where μ_{ph} is the phonon-limited mobility at room temperature, μ_N is the temperature independent neutral defect-limited mobility for long channel, L_c being a critical gate length

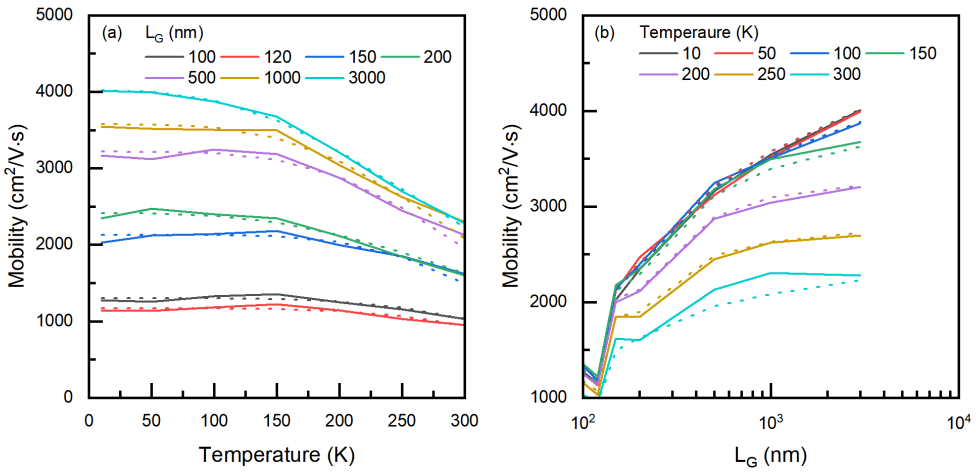

Figure 4.5. a) Experimental (solid lines) and Eq. (5.6) modeled (dashed lines) variations of electron low field mobility μ_0 with gate length L_g for various temperatures *T*=10, 50, 100, 150, 200, 250, and 300 K and b) variations of low field mobility μ_0 with temperature *T* for various gate lengths L_g= 100, 120, 150, 200, 500, 1000 and 3000 nm as obtained on GaN/Si HEMT devices (V_d=50 mV, L_{gs}=1 µm, L_{gd}=1.5 µm, W_g= 100µm). Model parameters: μ_{ph}=5000 cm^2/Vs, μ_N=4100 cm^2/Vs, L_c=160 nm, α=3, β=1.3.

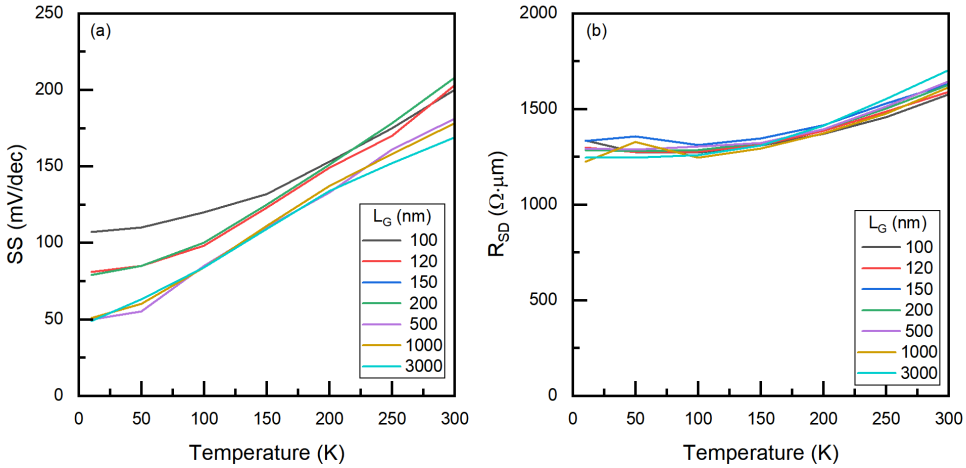

Figure 4.6. Typical variations with temperature of subthreshold swing *SS* (a) and access series resistance R_{sd} (b) as obtained on GaN/Si HEMT devices for various gate lengths L_g= 100, 120, 150, 200, 500, 1000 and 3000 nm (V_d=50 mV, L_{gs}=1 µm, L_{gd}=1.5 µm, W_g=100 µm).

and α and β fitting parameters. As can be seen from Figure 4.5, the simple model of Eq. 4.6 provided a good description of mobility variations both with gate length and with temperature. It clearly shows that the mobility degradation in short channel GaN HEMTs is also well interpreted by an increased contribution of neutral scattering defects. The latter ones should be mostly localized close to source-drain gate edges and could stem from the metal gate etching process.

The variations with temperature of the subthreshold swing $SS=dV_g/dlog(I_d)$ are shown in Figure 4.6(a) for various gate lengths. As expected from cryo-operation, the subthreshold swing *SS* mostly followed the Boltzmann linear trend vs temperature over 100 K before saturating at low temperature, likely due to some specific interface trap energy profile and/or to charge-induced-disorder potential fluctuations, as found in Si MOS devices [24, 25]. The

access series resistance R_{sd} was extracted using Eq. 4.1 at strong inversion where its impact is maximized. The variations with temperature of the series resistance R_{sd} for various gate lengths are shown in Figure 4.6(b). The access resistance R_{sd} values ranged typically around ≈1400 Ω.µm and increased linearly with temperature above 100 K, whatever the gate length,

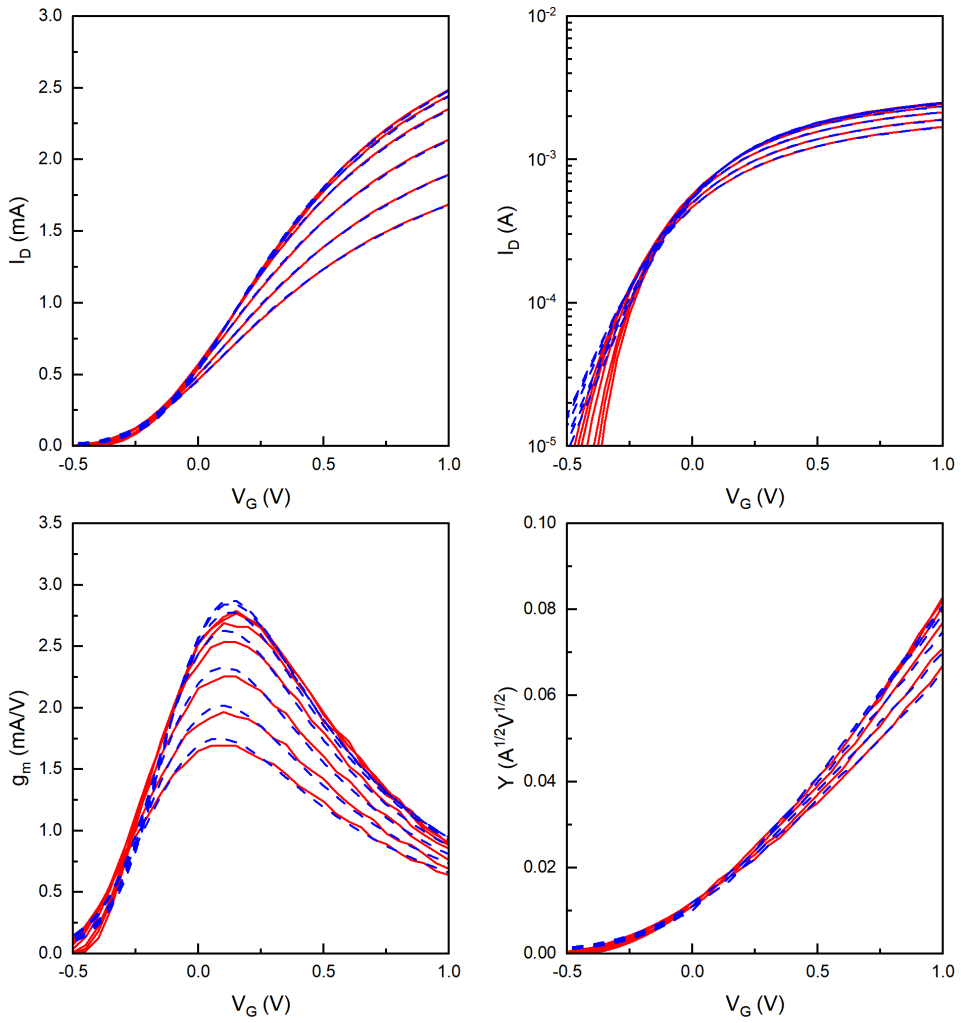

Figure 4.7. Experimental (red solid lines) and Lambert-W model fits (blue dashed lines) of the $I_d(V_g)$, $g_m(V_g)$ and $Y(V_g)$ characteristics for various temperatures T= 10, 50, 100, 150, 200, 250 and 300 K as obtained on GaN/Si HEMT devices (V_d=50 mV, L_g=3000 nm, L_{gs}=1 µm, L_{gd}=1.5 µm, W_g=100 µm).

emphasizing the R_{sd} extraction consistency against L_g. These $R_{sd}(T)$ variations are in line with the metallic degenerate behavior observed for the sheet resistance of AlGaN/AlN/GaN HEMT structures with ≈10^{13} q/cm^2 2DEG carrier density [21, 26]. These variations will be discussed in more details below.

4.3.3 Lambert-W-function based transistor parameter extraction

Lambert W function-based transistor parameter extractions were carried out using Eqs 4.2-4.3. Typical fits of the transfer characteristics obtained by LW function modelling, with optimized parameters (V_{th}, μ_0, n, R_{sd}), are illustrated in Figure 4.7 over a wide gate voltage range from below to above threshold. Note that excellent fits of the characteristics can be obtained, especially around and above threshold i.e. V_g>-0.25 V, for both $I_d(V_g)$, $g_m(V_g)$ and $Y(V_g)$ curves. In Figure 4.8 are shown the variations with temperature of the threshold

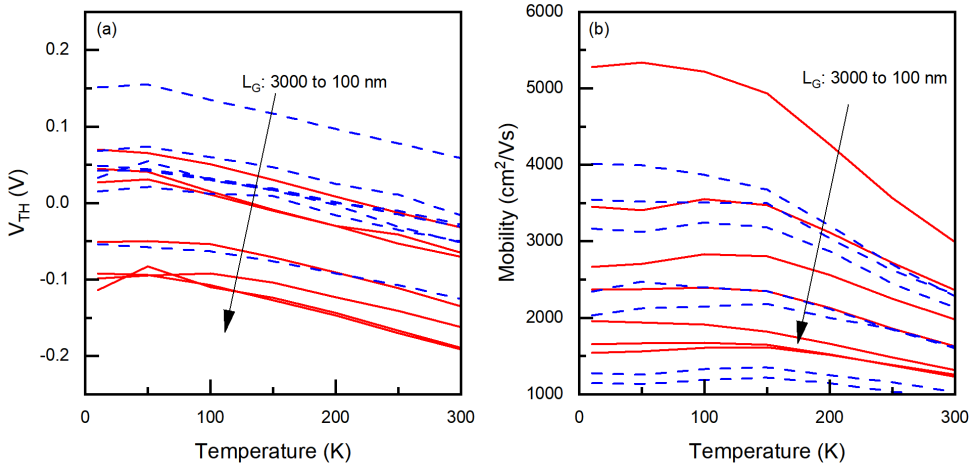

Figure 4.8. Variations with temperature of a) threshold voltage V_{th} and b) electron low field mobility μ_0, as obtained from LW function extraction (red solid line) and from Y-function method extraction (blue dashed lines) on GaN/Si HEMT devices with various gate lengths L_g= 100, 120, 150, 200, 500, 1000 and 3000 nm (V_d=50 mV, L_{gs}=1 µm, L_{gd}=1.5 µm, W_g=100 µm).

voltage V_{th} and of the low field mobility μ_0 obtained with the LW function fitting method (red solid lines) for devices with various gate lengths. For comparison purpose, the $V_{th}(T)$ and $\mu_0(T)$ curves extracted with Y-function method (blue dashed lines) are also reminded. Although slightly different, the V_{th} and μ_0 parameters extracted by both methods displayed the same behavior with temperature and gate length, which was also observed in Si MOS devices [17, 18]. The good mobility values obtained by the LW function method again confirmed the quality of such GaN/Si HEMT devices.

In Figure 4.9 are reported the variations with temperature and reciprocal temperature of the subthreshold ideality factor n_L obtained from the LW function fittings for various gate lengths (red solid lines). The ideality factor values directly deduced from the subthreshold swing *SS* (see Figure 4.9(a)), $n_{SS}=SS/(2.3\times kT)$, are also reported in blue dashed lines. As can be seen, the LW function fitting procedure tended to overestimate the ideality factor, especially at low temperature. However, this inconvenience does not alter the validity of the transistor parameter extraction just below and above threshold. It should also be noticed that

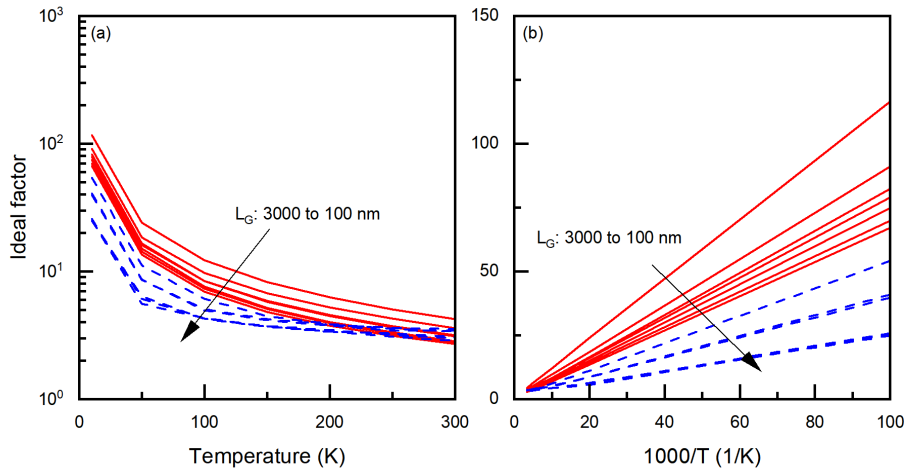

Figure 4.9. Variations of subthreshold ideality factors n_L (red solid lines) and n_{SS} (blues dashed lines) and b) with temperature (a) and reciprocal temperature (b) as obtained on GaN/Si HEMT devices for various gate lengths L_g= 100, 120, 150, 200, 500, 1000 and 3000 nm (V_d=50 mV, L_{gs}=1 µm, L_{gd}=1.5 µm, W_g=100 µm).

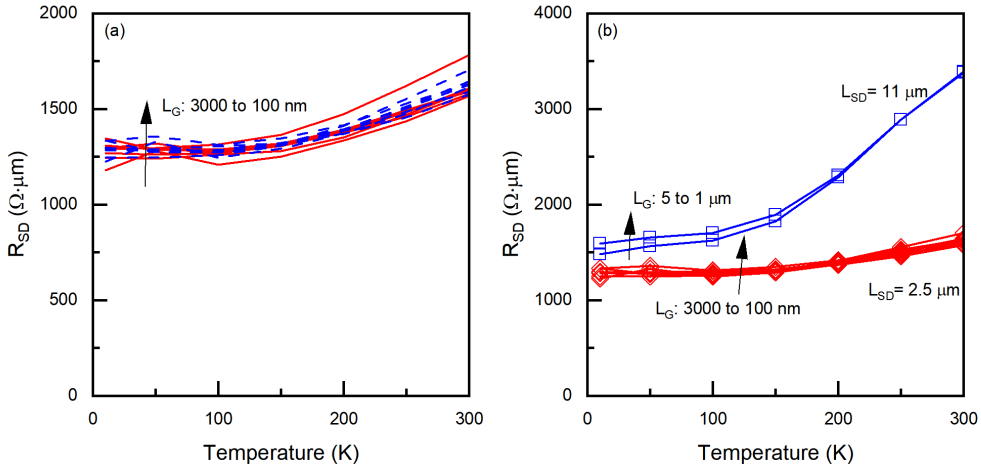

Figure 4.10. a) Variations with temperature of series resistance values R_{sd} extracted by LW function method (red solid lines) and by Y-function method (blue dashed lines) as obtained on GaN/Si HEMT devices for various gate lengths L_g= 100, 120, 150, 200, 500, 1000 and 3000 nm (V_d=50 mV, L_{gs}=1 µm, L_{gd}=1.5 µm, W_g=100 µm). b) Variations with temperature of series resistance values R_{sd} extracted by Y-function method for two access region distances L_{sd}=2.5 µm and 11 µm as obtained on GaN/Si HEMT devices for various gate lengths L_g= 1000 and 5000 nm (V_d=50 mV, L_{gs}=5.5 µm, L_{gd}=5.5 µm, W_g=125 µm).

the *1/T* dependence of the ideality factor has been previously found in Si MOSFETs and can be explained by the SS plateauing behavior at low temperature [18].

The access series resistance values R_{sd} extracted by the LW function fitting method (red solid lines) are displayed in Figure 4.10(a) along with those obtained by Y-function method (blue dashed lines) for a transistor with an access region distance $L_{sd}=L_{gs}+L_{gd}$=2.5 µm, emphasizing the consistency of the two extraction methodologies. In Figure 4.10(b), are reported the temperature dependence of the source and drain resistance R_{sd} extracted from Y-function method for two access region distances L_{sd1}= 2.5 µm and L_{sd2}=11 µm for various gate lengths. In this case, a larger temperature dependence of R_{sd} can be noticed for the devices with the longer access region distance.

In order to discriminate the contribution brought by the contact resistance R_c and by the

2DEG access region resistance $\rho_{2DEG}.L_{sd}$, ρ_{2DEG} being the 2DEG sheet resistance, a transmission line method (TLM) analysis of the source-drain series resistance R_{sd} for two L_{sd} values was carried out using Eq. 4.7,

$$R_{sd}(L_{sd}) = 2.R_c + \rho_{2DEG}.L_{sd} \qquad \text{(Eq. 4.7)}$$

By this way, ρ_{2DEG} and R_c can be obtained from,

$$\rho_{2DEG} = \frac{R_{sd}(L_{sd2}) - R_{sd}(L_{sd1})}{L_{sd2} - L_{sd1}} \qquad \text{(Eq. 4.8a)}$$

$$R_c = \frac{R_{sd}(L_{sd1}) - \rho_{2DEG}.L_{sd1}}{2} = \frac{R_{sd}(L_{sd2}) - \rho_{2DEG}.L_{sd2}}{2} \qquad \text{(Eq. 4.8b)}$$

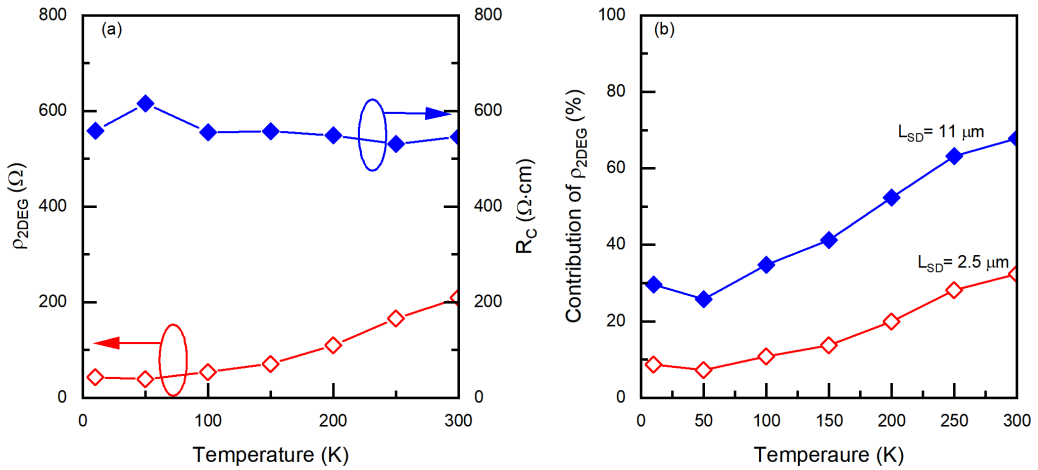

Figure 4.11. a) Variations with temperature of the 2DEG sheet resistance ρ_{2DEG} (red solid lines) and of contact resistance R_c (blue dashed lines) as obtained from R_{sd} TLM analysis on GaN/Si HEMT devices with various access region lengths L_{sd}=2.5 and 11 µm. b) Variations with temperature of percentage contribution of 2DEG access region resistance to the total source-drain resistance R_{sd} for two access region distances L_{sd}=2.5 µm and L_{sd}=11 µm as obtained from Figure 4.10(b) data.

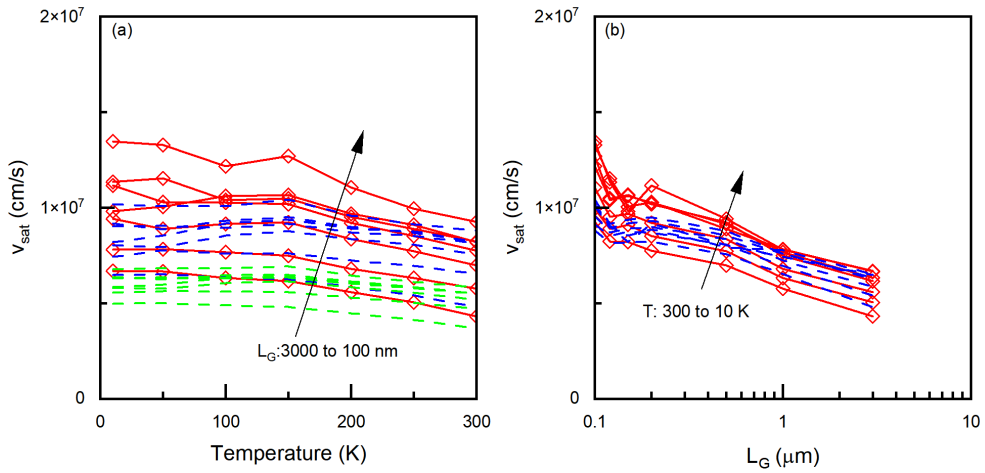

Figure 4.12. a) Variations with temperature of saturation velocity v_{sat} as extracted from Y-function (Eq. (4.4), red solid lines), or using the standard method with (blue dashed lines) or without (green dashed lines) R_{sd} correction (Eq. (6)), as obtained for various gate lengths L_g= 100, 120, 150, 200, 500, 1000 and 3000 nm (V_g=1.5 V, V_d=5 V & V_d=50 mV, W_g=100 µm). b) Variations with gate length of saturation velocity v_{sat} as extracted from Y-function (Eq. 4.4, red solid lines), or using the standard method (blue dashed lines) with R_s correction (Eq. 4.5), as obtained on GaN/Si HEMT devices for various temperatures.

In Figure 4.11(a) are displayed the variations of the contact resistance R_c and the 2DEG sheet resistance ρ_{2DEG} as obtained from Figure 10(b) data using Eq. 4.8 for L_{sd1}=2.5 µm and L_{sd2}=11 µm. As can be seen, the contact resistance R_c was rather temperature independent (≈550 Ω.µm), which reveals a quasi-metallic behavior. Instead, the 2DEG sheet resistance ρ_{2DEG} increased significantly with temperature, likely due to the mobility increase resulting from temperature lowering, as observed for long channel mobility in Figure 4.8(b), associated to a constant polarization-induced 2DEG carrier density. Since, at room temperature, ρ_{2DEG}≈200 Ω and μ_0≈2000 $cm^2V^{-1}s^{-1}$, it follows that the 2DEG electron density in the access regions is about ≈1.5x10^{13} cm^{-2}, which, for some reason, is about ≈30 % larger than the standard polarization-induced value for the AlGaN/GaN system as measured e.g. by Hall effect in devices from the same technology [26, 27]. In Figure 4.11(b) are shown the variations with temperature of the percentage contribution of the 2DEG access region

resistance to the total source-drain resistance $R_{sd}=2.R_c+\rho_{2DEG}.L_{sd}$. As can be seen, the contact resistance contribution is enhanced as the temperature is lowered and can reach up to 90 % (resp. 70 %) for an access region length L_{sd}=2.5 µm (resp. 11 µm). Finally, the saturation velocity v_{sat} was extracted using the Y-function (Eq. 4.4) and standard (Eq. 4.5) methods after having recorded the $I_d(V_g)$ characteristics in saturation region (V_d=5 V, not shown here). In Figure 4.12(a) are reported the variations with temperature of such extracted saturation velocities for various gate lengths. It should be mentioned that the value of the source resistance R_s needed in Eq. 4.5 was taken, according to Ohm's law, as a portion of the total resistance R_{sd} such as $R_s=R_c+L_{gs}.\ \rho_{2DEG}$. As can be seen from Figure 4.12(a), the v_{sat} values obtained by the standard method (Eq. 4.5) were significantly underestimated with respect to those deduced from Y-function, especially when the R_s correction was overlooked (R_s=0 in Eq. 4.5)) for short channels. It should be noted that the overall temperature dependence of v_{sat} is in a good agreement with those obtained on Si MOS transistors [20]. In Figure 4.12(b) are shown the corresponding variations of v_{sat} with gate length, revealing as is usual the increase of v_{sat} with channel length reduction, which is inherent to the extraction procedure and/or velocity overshoot effect [19, 20]. It is worth noting that these saturation velocity values, found around 10^7 cm/s, are in a good agreement with those previously reported in GaN HEMTs [28-32].

4.4 Summary and conclusion

In this study, a comprehensive electrical characterization and an extensive extraction of transistor parameters were conducted on 200mm CMOS-compatible GaN/Si HEMTs, reaching deep cryogenic temperatures. The transistor's key parameters, namely threshold voltage (V_{th}), low-field mobility (μ_0), subthreshold swing (SS), and source-drain series resistance (R_{sd}), were extracted in the linear region (V_d=50 mV) using Y-function and Lambert-W function methods for gate lengths ranging from 3 µm down to 0.1 µm. Additionally, the Y-function method was utilized in the saturation region (V_d=5 V) to extract

the saturation velocity. The findings indicate that the 200 mm CMOS-compatible GaN/Si HEMT devices exhibit excellent functionality even at extremely low temperatures (10 K) and demonstrate a significant improvement in mobility and subthreshold slope. In long channels, the low-field mobility μ_0 was observed to increase from 2000 to 4000 $cm^2V^{-1}s^{-1}$ as the temperature decreased from 300 K to 10 K, due to a reduction in phonon scattering. Conversely, in short devices, the low-field mobility remained nearly temperature independent, possibly due to the dominance of neutral defect scattering. Furthermore, the saturation velocity (v_{sat}) was found to exceed 10^7 cm^2/s at low temperatures. Through TLM analysis, the source-drain series resistance (R_{sd}) was shown to be more controlled by the contact resistance (R_c) than by the 2DEG access region resistance as the temperature decreased. Finally, it is worth noting that the Lambert-W function modeling of the drain current characteristics, which has demonstrated its effectiveness in Si MOSFETs [18], could offer a straightforward compact model for the operation of such GaN/Si HEMTs, even in deep cryogenic conditions.

4.5 References

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Chapter 5. Influence of Flexible Substrate in Low Temperature Polycrystalline Silicon Thin-Film Transistor: Temperature Dependent Characteristics and Low Frequency Noise Analysis

5.1 Introduction

Owing to the requirement of larger-scale and higher-resolution display panel, the development of display devices has been continued [1]. Especially, thin-film transistors (TFTs) are one of the key technologies to improve the operating speed of pixel array because switching transistor and driving circuits must be faster to give higher-resolution on the larger display panel compared to previous generation of display devices. To increase the driving current and carrier mobility, various research have been carried out for the material and device points of view. Low temperature polycrystalline silicon (LTPS) TFT is a successful result of such studies because it has the advantages of thermal budget during the fabrication process and high carrier mobility (several tens cm^2/Vs) [2]. Excimer laser annealing (ELA) rapidly melts and recrystallizes the amorphous layer into poly-Si at low temperature and makes grain size larger [3-5]. The large grain size of LTPS TFT enhances the carrier mobility and device performances compared to amorphous Si (a-Si).

Recently, the era of flexible display has begun. Industries have been making the products using flexible polymer (PET, polycarbonate, polypropylene, and polyimide (PI)) substrates, such as foldable display for the smart phones and flexible wallpapers using organic light emitting diodes (OLEDs). However, compared to the conventional TFTs on the rigid glass substrate, there are many issues for the TFTs on the flexible substrate in the device performance and reliability points of view. Generally, previous studies investigated poor reliability and on-off characteristics for the flexible substrates. For example, light illumination and electrical stress caused device instability, which is explained by the traps located in the insulator and channel of TFTs [6-9]. Thus, for the improvement of device performance and reliability in the LTPS TFTs on the flexible substrate, it is necessary to

understand origins of the different device properties compared to one on the typical glass substrates [10].

In this chapter, the different carrier transport induced by each substrate (flexible and glass substrate) is studied by using temperature dependent characterization and low frequency noise (LFN) analysis. Flexible substrate makes different temperature dependent behaviors of threshold voltage (V_{TH}), subthreshold swing (SS), effective carrier mobility (μ_{eff}) in I_{DS}-V_{GS} characteristics compared to the glass substrate. The effects of barrier height (E_B), grain size and traps at grain and grain boundaries have been studied by using the simulation and experimental analysis. LFN study shows the difference of noise level-frequency characteristics caused by the trap profiles depending on the kind of a substrate.

5.2 Device Fabrication

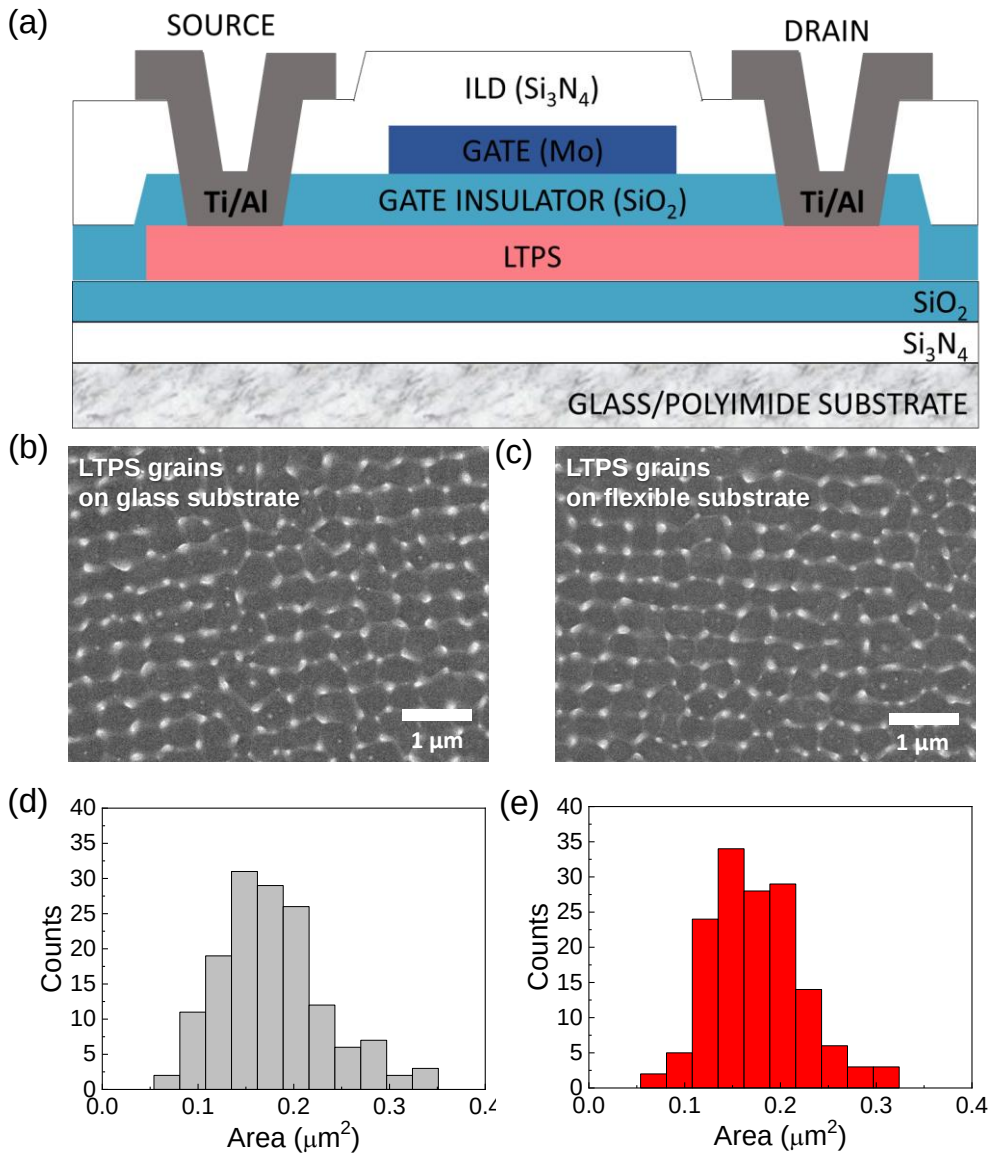

Figure 5.1. (a) Cross section of LTPS TFTs on glass and flexible substrates. FE-SEM images of LTPS films on (b) glass and (c) flexible substrate. The histogram of grains area on (d) glass and (e) flexible substrate shows that mean value is 0.178 and 0.175 μm^2, respectively.

Figure 5.1(a) presents the cross-section of p-type LTPS TFTs. A buffer layer, composed of Si_3N_4 and SiO_2, was deposited on both glass and flexible PI substrates before amorphous-Si was sputtered with 100 nm. After ELA process, amorphous-Si was recrystallized as LTPS active channel. The gate insulator (GI) was made of 100 nm SiO_2 by plasma-enhanced chemical vapor deposition (PECVD). After the formation of gate metal Mo on GI, the self-aligned boron doping was carried out for heavily doped source/drain region. After doping process, devices were annealed at 380 ℃ during 30 minutes in furnace. The interlayer dielectric (ILD) Si_3N_4 was deposited by PECVD before source/drain contacts were patterned by dry etching process. Finally, Ti/Al deposited for electrodes. The gate width W_G is 3.5 μm and the gate length L_G is 40 μm for both LTPS TFTs on different substrates. Each image of LTPS channel on glass (Figure 5.1(b)) and flexible (Figure 5.1(c)) substrates is observed by Hitachi SU8200 Field Emission-Scanning Electron Microscopy (FE-SEM), respectively. In Figure 5.1(d) and (e), the histogram of grain area is shown for LTPS film on glass and flexible substrate, respectively. Mean grain area of each film is 0.178 and 0.175 μm^2, which means that the mean grain size (the square root of mean area) is approximately same as 0.42 μm.

Table 5.1 Electrical parameters of LTPS TFTs

Parameters	on Glass Substrate	on Flexible Substrate
Threshold Voltage $\|V_{TH}\|$ (V)	2.25	4.14
Subthreshold Swing SS(V/dec)	0.7	1.0
On Current I_{ON} (μA·μm/μm)	0.86	0.65

5.3 Results and discussion

5.3.1 DC Characteristics

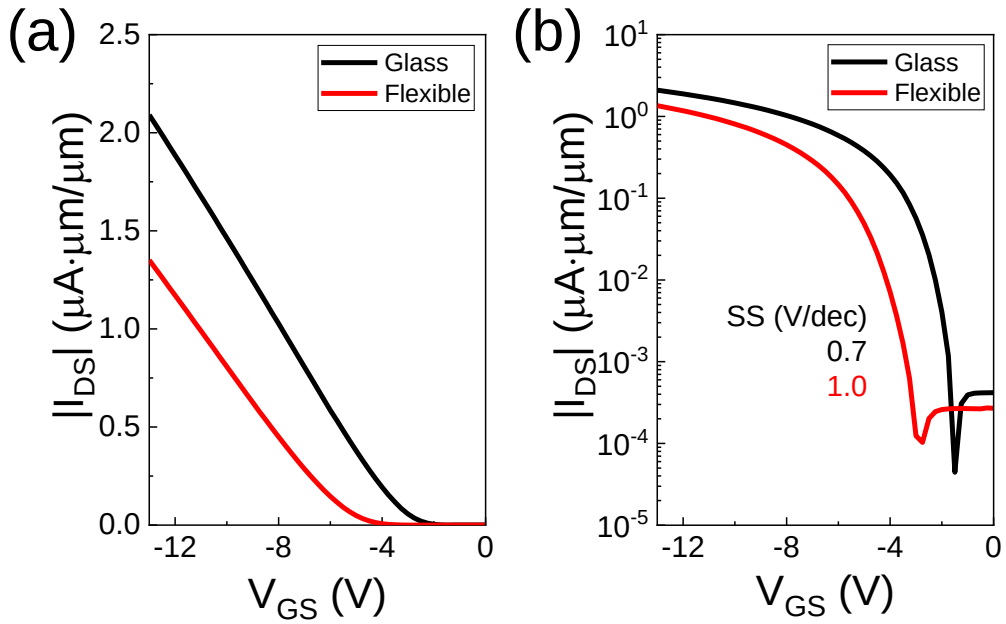

Figure 5.2. (a) Transfer curves for glass and flexible substrates at 300 K. Drain-to-source current $|I_{DS}|$ for the flexible substrate is approximately 40 % lower than that of the glass substrate. By using the flexible substrate, threshold voltage V_{TH} is negatively shifted comparing to the glass substrate. (b) Subthreshold swing *SS* of LTPS on the flexible substrate is 30 % higher than the device on the glass substrate.

The transfer characteristics of LTPS TFTs were measured by Keithley 4200 semiconductor characterization system (SCS) with the variation of gate-to-source bias V_{GS} from 0 to −13 V and with the drain-to-source voltage V_{DS}=−0.1 V for the linear region operation to prevent mobility degradation by the lateral electric field between source and drain. All DC characterization were carried out in the vacuum probe station (<10^{-5} Torr) to control other gas and water molecules which can affect device performance. Measurement temperature is controlled in the range of 300-375 K by thermal chuck. Figure 5.2(a) and (b)

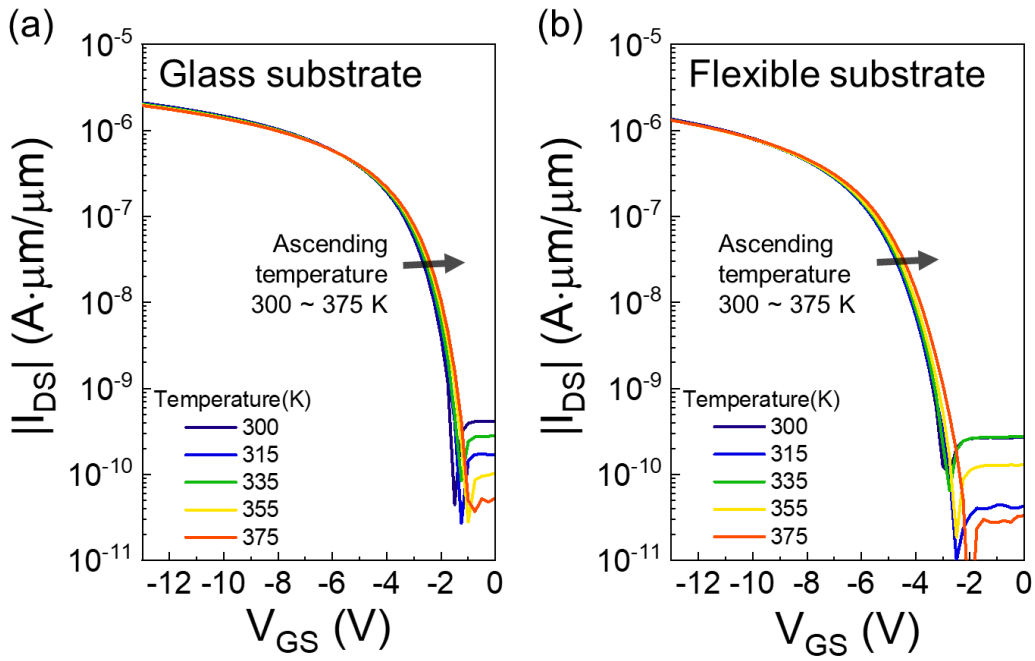

Figure 5.3. Temperature dependent transfer characteristics of LTPS TFTs on glass and flexible substrates. From 300 K to 375 K, V_{TH} changes in positive direction for both glass and flexible substrates. Higher temperature makes $|I_{DS}|$ lower and SS higher.

show the typical linear- and log-scale plots of transfer characteristics for LTPS TFTs at room temperature (300 K). The V_{TH} is extracted by constant-current method at the normalized drain-to-source current $|I_{DS}|=10^{-8}$ A·μm/μm. As shown in Table 5.1, LTPS TFT on the flexible substrate has negatively shifted V_{TH} compared to on the glass substrate. In the case of that mobile carriers (hole) are trapped in certain trap sites, more negative gate bias is needed to make channel carrier concentration high. The *SS*, an electrical parameter of gate coupling affected by the interface traps, is 0.7 V/decade for glass substrate. On the flexible substrate, *SS* is 1.0 V/decade and 30 % higher than glass substrate. On-current (I_{on}) is decided by I_{DS} at certain overdrive voltage $|V_{OV}|$ ($|V_{GS}-V_{TH}|=5$ V) and LTPS TFT on the flexible substrate shows approximately 24 % suppressed I_{on} than glass substrate's one [11-13]. As previous reports, all the parameters related to device performance in the TFT on the flexible

substrate show poor values comparing to the that on the glass. Therefore, the intensive studies to elucidate degradation factors are necessary to improve flexible display device based on LTPS.

Figure 5.3(a) and (b) show the I_{DS}-V_{GS} characteristics under the change of temperature in the range of 300-375 K. It is observable that the positive shift of V_{TH}, the degradation of *SS* and I_{on} according to ascending temperature for both glass and flexible substrates [14, 15].

The V_{TH} of TFT is given by Eq. 5.1:

$$V_{TH} = V_{FB} + 2\phi_f + \sqrt{\frac{4\varepsilon_{ch}\, q\, N \phi_f}{C_{ox}}} \qquad \text{(Eq. 5.1)}$$

where V_{FB} is the flat-band voltage, ϕ_f the difference between Fermi level and intrinsic Fermi level, ε_{ch} the permittivity of LTPS active channel, q the elementary charge, N the

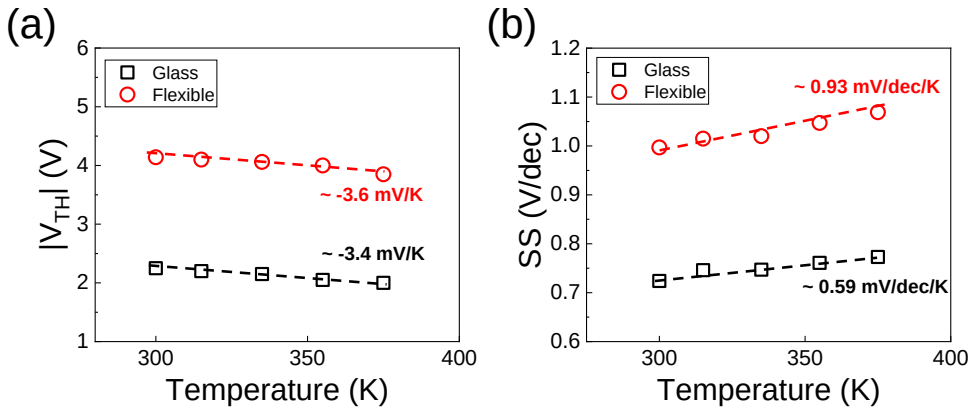

Figure 5.4. Threshold voltage V_{TH} and subthreshold swing *SS* as a function of temperature for LTPS TFTs. (a) The magnitude of $|V_{TH}|$ for the flexible substrate is higher than that of the glass substrate at each temperature condition, whereas the slope of $|V_{TH}|$−temperature is similar. (b) Higher temperature makes *SS* of LTPS TFT on the flexible substrate increase. In the case of *SS*, flexible substrate has roughly 1.5 times larger *SS*-temperature sensitivity, which means higher impact of C_{it} and C_{dep}.

doping concentration, and C_{ox} the gate insulator capacitance. Temperature dependent ϕ_f is an important factor that decides V_{TH} at given temperature, and described by Eq. 5.2 as following [15, 16]:

$$\frac{d\phi_f}{dT} = \frac{k_B}{q}\left(ln\left(\frac{N}{n_i}\right) - \frac{T}{n_i}\frac{\partial n_i}{\partial T}\right) \quad \text{(Eq. 5.2)}$$

where k_B is Boltzmann's constant, N the doping concentration, n_i the intrinsic carrier concentration proportional to $exp\left(\frac{-Eg}{2k_BT}\right)$, and T the temperature. $\frac{d\phi_f}{dT}$ is negative due to exponential increasement of $\frac{\partial n_i}{\partial T}$. Thus, $|V_{TH}|$ decreases as temperature increases. The extracted $\frac{dV_{TH}}{dT}$ values are similar for both substrates (-3.4 mV/K in glass substrate and -3.6 mV/K for flexible substrate in Figure 5.4(a)).

SS is a function of temperature and explained by Eq. 5.3 as follows [17, 18]:

$$SS = \frac{2.3k_BT}{q}\left(1 + \frac{C_{it}+C_{dep}}{C_{ox}}\right) \quad \text{(Eq. 5.3)}$$

where C_{it} is the interface trap capacitance, and C_{dep} the depletion capacitance. The thermal dependency of *SS* would be determined by C_{it} and C_{dep} related to LTPS active channel which has many grains and grain boundaries [19-21]. In Figure 5.4(b), the slope of temperature dependent *SS* for the flexible substrate shows approximately 1.6 times higher than glass substrate's one. It means that LTPS TFT on flexible substrate has higher C_{it} and C_{dep} caused by interface traps of gate insulator-to-active channel, and grain-to-grain boundaries.

The μ_{eff} of polycrystalline channel is affected by the grain size (L_{grain}) and E_B at grain-to-grain boundaries which can be described by Seto's model [22]:

$$\mu_{eff} = L_{grain}q\sqrt{\frac{1}{2\pi m^* k_B T}}e^{\frac{-E_B}{kT}} \quad \text{(Eq. 5.4)}$$

where m^* is the effective mass of carrier. In the polycrystalline channel, larger L_{grain} makes

the carrier velocity faster whereas higher E_B disturbs the carrier transport between grains [23-25]. To examine the trade-off between L_{grain} and E_B, temperature dependent μ_{eff} is simulated as a function of L_{grain} and E_B in Figure 5.5(a). At fixed grain size (0.7 μm), different E_B change the trend of the slope $\Delta=\mu_{eff}T$. For E_B=50 meV, Δ shows negative slope (-5.2 $cm^2V^{-1}s^{-1}K$). In this case, high E_B at grain-to-grain boundaries dominates the carrier transport and higher temperature increases μ_{eff}. In contrast, for small E_B (1 meV), μ_{eff} is mainly affected by L_{grain} and suppressed by phonon scattering at high temperature so that Δ is positive (10.6 $cm^2V^{-1}s^{-1}K$). From the experimental data, Δ=10.4 and 4.5 $cm^2V^{-1}s^{-1}K$ are observed for the LTPS TFTs on the glass and flexible substrates, respectively as shown in Figure 5.5(b) [26, 27]. E_B and L_{grain} are extracted by fitting of Seto's model (Table 5.2). In the flexible substrate, approximately 18 times higher E_B is observed than the glass substrate whereas the L_{grain} is similar (0.65 and 0.67 μm for glass and flexible substrate, respectively). It might describe that higher and wider barrier height between grain boundaries affect C_{it}, and also reduce μ_{eff} for the flexible substrate. Because the density of trap is as a function of energy, the mobile carrier can feel more trap sites in higher E_B. The higher barrier height, the more traps in the grain boundary interfaces exist and increase C_{it} (Figure 5.5(c)). Thus, high E_B makes the degradation of *SS* and I_{on} for LTPS TFT on the flexible substrate.

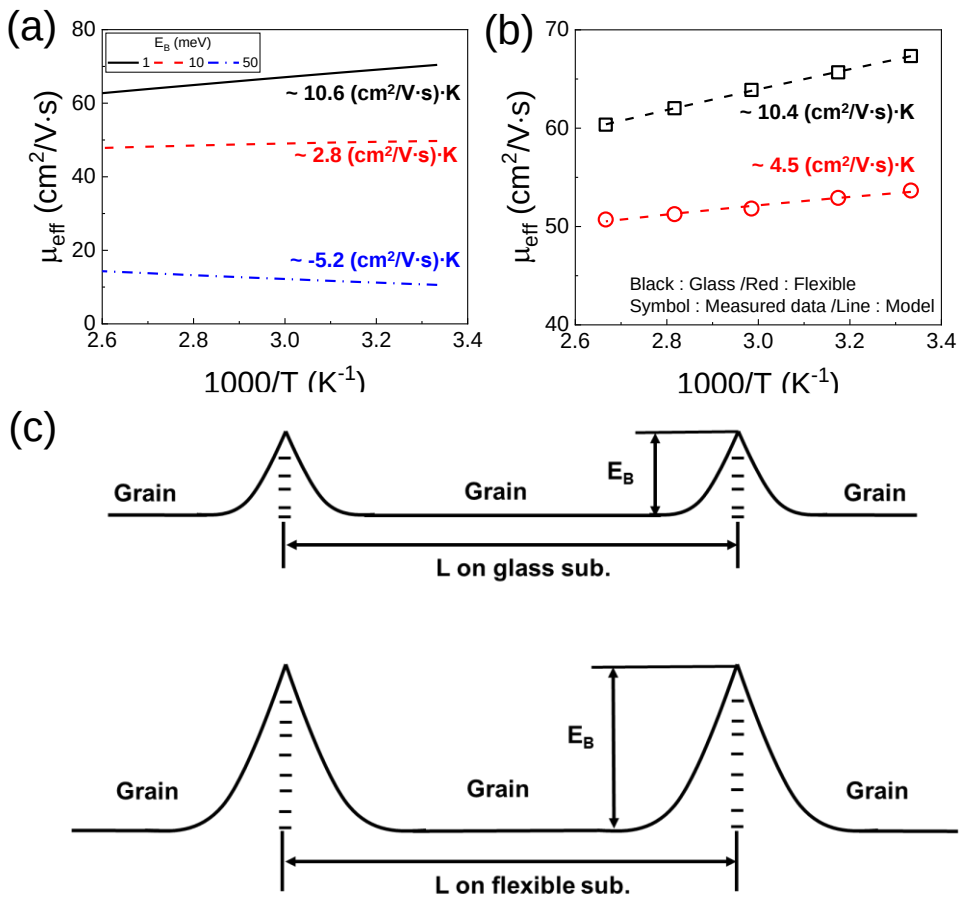

Figure 5.5. (a) Simulation of temperature dependence of effective mobility μ_{eff} under various grain boundary barrier height E_B (1, 10, and 50 meV) for fixed grain size L_{grain}=0.7 μm. (b) The experimental data which are well fitted by the model in the both cases. Less sensitive temperature dependence of μ_{eff} was shown in the lower value. (c) Illustration of LTPS active channels on both glass and flexible substrates by applying extracted E_B and L_{grain}. By fitting the measured data to model, E_B and L_{grain} can be extracted.

5.3.2 Low Frequency Noise

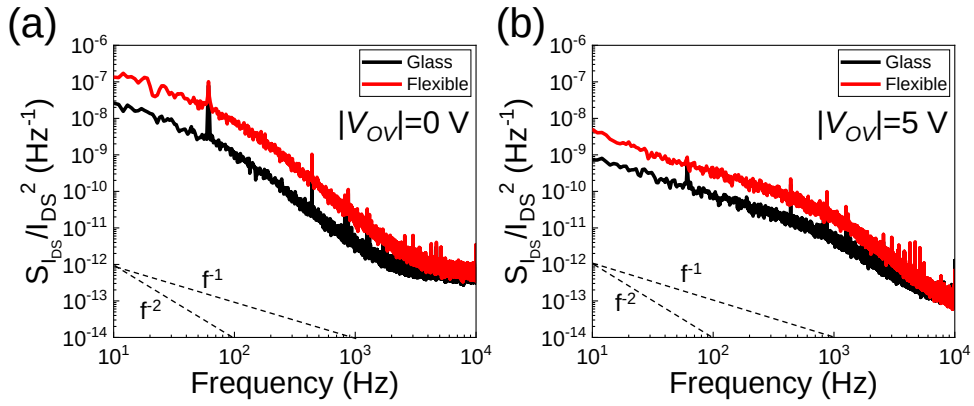

Figure 5.6. Comparisons of the normalized noise power spectral density PSD at different overdrive voltages $|V_{OV}|$ (a) 0 V and (b) 5 V. For both $|V_{OV}|$, flexible substrate shows 1-order higher noise level than that of glass substrate at 10 Hz. The corner frequencies (f_c) are observed, which is related to carrier trapping/de-trapping time.

The LFN characteristics of LTPS TFTs were measured by a Stanford SR 570 low noise current preamplifier and NI DAQ 4431 data acquisition (DAQ) with the variation of $|V_{OV}|$ in the range of 0 to 6 V and with V_{DS}=−0.1 V. Since the flux of I_{DS} is decided by the quantity of inversion charges, V_{GS} is selected in the range from V_{TH} to V_{OV} high enough. The LFN was measured as a function of frequency (f) between 10 to 10 kHz. Figure 5.6(a) and (b) show the drain current-normalized power spectral density (PSD) $S_{I_{DS}}/{I_{DS}}^2$ of LTPS TFTs on glass and flexible substrates at $|V_{OV}|$=0 and 5 V. It is shown that the magnitude of PSD for LTPS TFT on the flexible substrate is approximately 10 times higher than that of TFT on the glass substrate below the corner frequency (f_c) which related to the location information of traps for $|V_{OV}|$=0 and 5 V. Below f_c, PSD decreases with the slope of f^{-1}, whereas it drops to over f^{-2} after f_c. The f_c is observed on near 10^2 and 10^3 Hz at $|V_{OV}|$= 0 and 5 V, respectively [28-30]. The PSD at higher frequency is affected by faster trapping and de-trapping events of carriers, which means that it occurs near interface at gate insulator-to-active channel. On the

other hands, the PSD at lower frequency refers to the traps far from the interface because enough time is needed for trapping and de-trapping of carriers. When the LFN is affected by trapping and de-trapping of carriers, different slope and corner frequency of PSD as a function of $|V_{OV}|$ means that the trap profile changes according to the gate bias [31].

In conventional LFN analysis, the mechanism of the drain current-normalized PSD fluctuation is explained by the carrier number fluctuation with correlated mobility fluctuation (CNF+CMF) [32, 33]. It described in two parts: (i) carrier number fluctuation occurred by carrier of trapping/de-trapping, (ii) carrier mobility fluctuation when carrier flows under coulombic force scattering [34]:

$$\frac{S_{I_{DS}}}{{I_{DS}}^2} = S_{vfb}\left(1 + \alpha\mu_{eff}C_{ox}\frac{I_{DS}}{g_m}\right)^2\left(\frac{g_m}{I_{DS}}\right)^2 \qquad \text{(Eq. 5.5)}$$

where S_{vfb} is the PSD of flat band voltage noise, α the remote Coulomb scattering coefficient, and g_m the transconductance. As shown in Figure 5.7(a), ${S_{I_{DS}}}/{{I_{DS}}^2}$ is linearly

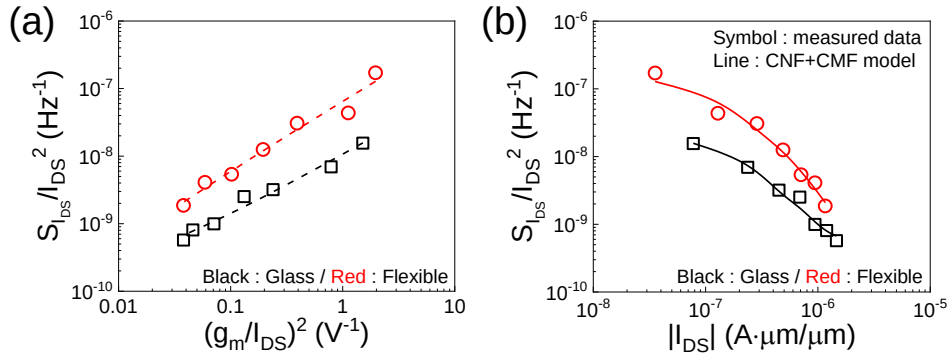

Figure 5.7. Noises spectrum of LTPS TFTs on glass (Black) and flexible (Red) substrates which were normalized by I_{DS} at frequency f=10 Hz. (a) S_{IDS}/I_{DS}^2 is proportional to $(g_m/I_{DS})^2$. The carrier number fluctuation correlated carrier mobility fluctuation CNF+CMF model is a function of $(g_m/I_{DS})^2$. (b) Measured data (black and red symbols) were well fitted by CNF+CMF model.

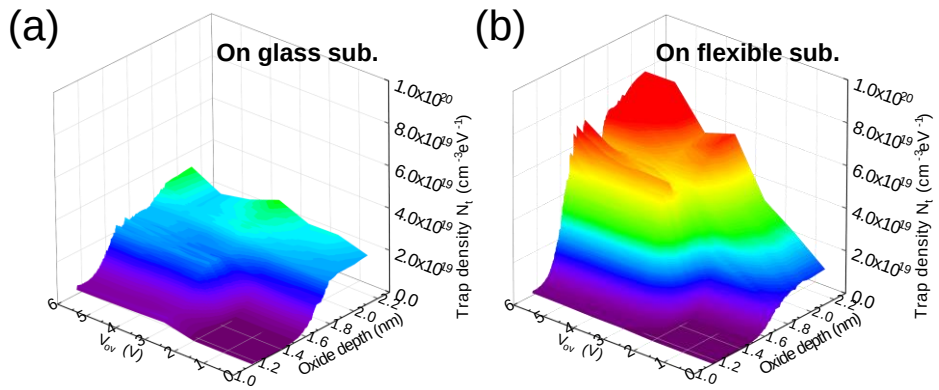

Figure 5.8. 3D Contour of trap density N_t distribution for oxide depth z and $|V_{OV}|$ for glass substrate and flexible substrate, respectively. It is observed that LTPS TFTs on both substrates have gate bias dependence. (a) For the LTPS TFT on the glass substrate, N_t is less depending on V_{OV} and z compared to the device on the flexible substrate. (b) In contrast, higher $|V_{OV}|$ increases N_t for the LTPS TFT on the flexible substrate. Especially at $|V_{OV}|$=6 V, peak of N_t is shown. At this point, flexible substrate shown approximately 4 times higher N_t than glass substrate.

proportional to $(g_m/I_{DS})^2$, which means that CNF+CMF model explains the noise behavior of LTPS TFTs on both substrates. In Figure 5.7(b), the normalized PSDs (symbols) at f=10 Hz about all $|V_{OV}|$ are well fitted by CNF+CMF model (lines) for both glass and flexible substrates. It should be noticed that LTPS TFT on the flexible substrate shows higher ${S_{I_{DS}}/I_{DS}}^2$ than one on the glass substrate at same $(g_m/I_{DS})^2$ and at same $|I_{DS}|$, in Figure 5.7(a) and (b), respectively. From ${S_{I_{DS}}/I_{DS}}^2$, the gate-to-source voltage normalized PSD ${S_{I_{DS}}/I_{DS}}^2$ can be extracted by Eq. 5.6 as follows:

$$\frac{S_{I_{DS}}}{{I_{DS}}^2} = \frac{S_{V_{GS}}}{{V_{GS}}^2} \qquad \text{(Eq. 5.6)}$$

The trap density N_t can be evaluated, also the dependence of trap density used to determine drain current PSD as follows [32, 35, 36]:

$$N_t = \frac{f W_G L_G {C_{ox}}^2 S_{V_{GS}}}{q^2 kT\lambda\left(1+\alpha\mu_{eff}C_{ox}\frac{I_{DS}}{g_m}\right)^2} \quad \text{(Eq. 5.7)}$$

where $S_{V_{GS}}$ is the PSD of the gate voltage noise, λ the tunneling attenuation length in gate insulator (~1 $\AA$ for Si/SiO_2). Oxide depth z is translated by the measured f as follows [37, 38]:

$$z = \lambda \cdot ln(\frac{1}{2\pi f \tau_0}) \quad \text{(Eq. 5.8)}$$

where τ_0 is the time constant that is usually taken as 10^{-10} s. From Eq. 5.5−5.7, N_t profiles as a function of z can be calculated for each $|V_{OV}|$. Figure 5.8(a) and (b) illustrate the N_t profiles for LTPS TFTs on glass and substrates as a function of $|V_{OV}|$. On the flexible substrate, trap profiles steeply increase from relatively shallow depth compared to LTPS TFT on the glass substrate. Mostly, the flexible substrate shows higher N_t profiles compared to the glass substrate for especially $|V_{OV}|$>2 V. Over certain bias point $|V_{OV}|$=6 V, the N_t of flexible substrate is approximately up to 4 times higher than glass substrate as shown in Figure 5.8(b). The result of LFN analysis is consistent with DC characteristics. The DC characteristics (poor *SS*, suppressed I_{on} and μ_{eff}) of LTPS TFT on the flexible substrate are influenced by higher E_B which makes effective N_t higher as shown in Figure 5.5(c). Therefore, from DC characteristics and LFN analysis, it seems that the difference of electrical properties between LTPS on glass and flexible substrate mainly comes from the effective N_t according to the interface traps at the gate insulator-to-active channel and grain-to-grain boundaries.

Table 5.2 The extracted parameters fitted by temperature dependent effective mobility model for polycrystalline Silicon.

	on Glass Substrate	on Flexible Substrate
Grain Size L_{grain} (μm)	0.65	0.67
Barrier Height E_B (meV)	0.4	7.0

5.4 Conclusion

In conclusion, DC and LFN characteristics for LTPS TFTs on glass and flexible substrates have been studied to understand factors which affect electrical properties such as I_{on}, V_{TH}, *SS*, and μ_{eff}. Through temperature dependent characterization, the different *SS* and μ_{eff} trend have been observed between devices on the glass and flexible substrates. Larger SS of LTPS TFT on the flexible substrate is caused by higher C_{it} and C_{dep} than on the glass substrate. We found that the μ_{eff} for both LTPS TFTs on glass and flexible substrate have different property because E_B for flexible substrate is approximately 18 times higher than that of glass substrate although the size of grains is similar for both devices. Such higher E_B of flexible substrate could make the μ_{eff} suppressed and *SS* increased. From the LFN analysis, one-order higher noise level is observed for the flexible substrate compared to the glass substrate. Up to 4 times N_t for LTPS TFTs on the flexible substrate are distributed across the oxide depth. It can be explained that LTPS TFT on flexible substrate has worse DC performance such as *SS* and μ_{eff} due to interface traps at the gate insulator-to-active channel and grain-to-grain boundaries, which are induced by E_B.

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Summary and Conclusion

The dissertation provides insights into the electrical characterization and modeling of various advanced electronic devices based on MOSFET structure. The characterization and modeling techniques can be valuable for the design and optimization of advanced MOS transistors in various technologies, enabling the development of more efficient and reliable electronic devices, including Nanosheet FETs on FDSOI, GaN HEMTs, and LTPS TFTs.

Because of extremely aggressive scaled down, it is more complicated to carry out device characterization. The methodologies to extract electrical parameters such as threshold voltage, subthreshold swing, mobility, and series resistance were introduced. Also, low frequency noise was discussed on the useful tool to evaluate electronic devices.

For instance, electrical characterization of 2-vertically stacked Nanosheet FETs on FDSOI was performed using statistical analysis. Various dimensions of NFET and PFET devices were investigated, and electrical parameters were extracted using methods such as Y-function and LW function. The correlation of different electrical parameters was investigated, and the standard deviation of each parameter (threshold voltage, gain, series resistance, and ideality factor) was utilized for the interpretation of Pelgrom's law. Also, the statistical analysis of the low frequency noise was presented. The average noise value acts 1/f like behavior and can be explained by the carrier number fluctuations model.

Following this, detailed electrical characterization and transistor parameter extraction were performed on GaN/Si HEMTs down to deep cryogenic temperatures. The crucial transistor parameters were extracted using the Y-function and Lambert-W function methods. The results showed that these GaN/Si HEMT devices demonstrated good functionality at very low temperatures, with improvements in mobility and subthreshold slope. The source-drain series resistance was found to be more limited by contact resistance than by the 2DEG access region resistance at lower temperatures.

In addition, the carrier transport of p-type low temperature polycrystalline silicon (LTPS)

thin-film transistors (TFTs) on flexible substrates was studied and compared to that on glass substrates. Temperature-dependent characterizations were carried out to investigate the origin of carrier transport on different substrates. It was found that the barrier height between grain boundaries had more influence on the degradation of LTPS TFTs on flexible substrates than the grain size. The total trap density for flexible substrates was higher than that of glass substrates, supporting the higher barrier height in devices fabricated on flexible substrates.

By applying different characteristics (variability, temperature dependency, and low frequency noise) in various electronic devices,

Publication

Versatile

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Chapter 5.

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Conference presentation

1. **IEEE Electron Devices Technology and Manufacturing Conference (EDTM)**, 2023, 1st author, Oral presentation, Drain Current Variability in 2-Levels Stacked Nanowire Gate All Around P-Type Field Effect Transistors
2. **Korean Conference on Semiconductor (KCS)**, 2023, 1st author, Oral presentation, Global Variability in 2-levels Stacked Nanowire Gate-All-Around Field Effect Transistor
3. **International Conference on Solid State Devices and Materials (SSDM)**, 2022, 1st author, Oral presentation, Drain Current Variability Assessment in 2-levels Stacked Nanowire Gate All Around Field Effect Transistors
4. **Korean Conference on Semiconductor (KCS)**, 2021, 1st author, Oral presentation, The Carrier Transport Characteristics in LTPS TFTs
5. **Korean Conference on Semiconductor (KCS)**, 2020, co-author, Poster presentation, Random Telegraph Noise (RTN) Analysis depending on Si/SiGe Channel in Gate-All-Around (GAA) FET
6. **Material Research Society (MRS) Fall**, 2019, 1st Author, Poster presentation, Substrate dependent active channel characteristics in low-temperature polycrystalline silicon thin film transistors
7. **Korean Conference on Semiconductor (KCS)**, 2019, Oral presentation, 1) High Temperature Characterization of High-k/Metal-Gate 2-stacked Gate-All-Around Nanowire FET versus FinFET, 2) Low Frequency Noise Variability Analysis Depending on Epi-Source/Drain in GAA(Gate-All-Around) FET
8. **IMID**, 2018, 2nd Author, Poster presentation, Analysis of SiO2 thin film properties for high performance TFT
9. **AWAD**, 2018, 1st Author, Poster presentation, The Impact of Series Resistance in Multi-Channel Omega-gate Nanowires PMOS FETs by Low Frequency Noise Analysis
10. **Korean Conference on Semiconductor (KCS),** 2018, 2nd Author, Oral presentation, High-Temperature Characteristic of Low-Temperature Polycrystalline Silicon Thin-Film Transistors (LTPS-TFTs) on Glass and Plastic Substrates