Étude CEM d'un driver de MOSFET SiC 1,7 kV

Hadiseh Geramirad

N°d'ordre NNT : 2020LYSEC031

THESE de DOCTORAT DE L'UNIVERSITE DE LYON
Opérée au sein de l'Ecole centrale de Lyon

Ecole Doctorale N° 160
(Ecole Doctorale d'Electronique, Electrotechnique, Automatique)

Spécialité de doctorat : **Génie Electrique**
Discipline : **Electronique**

Soutenue publiquement le 25/11/2020, par :
Hadiseh GERAMIRAD

EMC study of a 1.7 kV SiC MOSFET gate driver

Devant le jury composé de :

CLAVEL, Edith/ Maître de Conférences Université de Grenoble	Rapporteure
CANAVARO, Flavio/ Professeur Université Politecnico di Torino	Rapporteur
IDIR, Nadir/ Professeur Université de Lille	Examinateur
Costa, François/ Professeur Université de Paris Est Créteil	Examinateur
VOLLAIRE, Christian/ Professeur Université de Lyon	Directeur de thèse
BREARD, Arnaud/ Professeur Université de Lyon	Encadrant
MOREL, Florent/ Dr SuperGrid Institute	Encadrant
LEFEBVRE, Bruno/ Dr SuperGrid Institute	Invité

Abstract

The growing market for renewable energy technologies results in a fast growth in power electronic technologies. Most of the renewable energy technologies produce DC power therefore power electronic converters are needed to convert DC into AC power. Power electronic converters are widely used in voltage range up to +/-1MV and up to several GW power. Given the recent rapid growth in the performance of power semiconductors like Si, SiC and GaN power devices for high-efficiency power applications, there is a need for dedicated gate drivers to deal with SiC semiconductors in new converter generations. To meet the development of these applications, this research work has been carried out on the power electronic field presenting a gate driver for a half-bridge SiC MOSFET power module to be applied in a medium/high voltage power converter.

The principle of operation of converters operation is based on switching. SiC MOSFETs as the switching elements of converters offer many advantages including low conduction losses, high speed and high voltage switching which increase the efficiency and power density. However, it brings some challenges for converter designers like increasing electromagnetic interferences which disturb the converter operation. Gate drivers provide interfaces between the control signal and switching actions in converters. They are also a path for electromagnetic interferences due to their isolated power supply. Gate drivers can be one of the elements which can act on switching transitions and reduce the generated electromagnetic interferences in converters. This reduce also the electromagnetic interferences passing through gate drivers. Therefore to keep the converter in its safe operation, this study targets two main objectives. First protecting gate drivers by limiting the amount of interferences passing through them in order to achieve the operation of the converter at rated value. Secondly reducing the generated electromagnetic interferences by means of gate driver at the semiconductor level by modifying the voltage waveform applied for driving semiconductors. Reaching these objectives results in improving the electromagnetic compatibility of converters.

At first, a commercial 1.7 kV SiC MOSFET half-bridge device is used as a switching leg in a 100 kW Dual Active Bridge DC/DC converter. The device is controlled by a commercial gate driver. The investigation in the converter prototype shows the importance of the conducted electromagnetic interferences passing through the gate drivers. The uncontrolled magnitude of the conducted electromagnetic interferences disturbs the triggering of the semiconductors. This phenomenon is called "self-disturbance". It prevents the proper operation of the converter at rated voltage and power. Self-disturbance phenomenon highlights the effect of the gate drivers on the operation of the converter. This part of the study shows the need of new gate driver techniques to reduce the interferences from semiconductors.

The second contribution addresses the challenge of gate perturbation due to fast switching in SiC MOSFET based converters. A well-known gate voltage perturbation issue due to the fast switching of semiconductors results in self-disturbance phenomenon. This problem is solved by a new circuit implemented in a classical gate driver architecture. It is proposed to filter the parasitic current flowing into the gate by a bifilar common-mode choke in addition of the classical protection circuit. Thanks to this proposed method, the electromagnetic interferences passing through gate drivers are reduced. This part shows the sensitivity of the SiC MOSFET gate drivers design to parasitic elements and measurement probes. The performance of the classical differential probe is compared with optical isolated voltage probe by measuring the gate-source voltage of semiconductors. It clarifies how the parasitic elements of the measurement probes affect the measurements and it allows the optimization of the gate driver design.

The final contribution is the development of a new driving technique. A new inductive feedback gate driver is designed based on the direct drain/source current measurement of the SiC MOSFET power module. The dynamic adjustment of the gate current with this new gate driver technique reduces the generated interferences thanks to moderate switching voltage and current slops. The proposed gate driver achieves a better trade-off between losses and conducted emissions compared to the classical series-connected passive resistors for SiC MOSFET gate drivers.

Résumé

Le marché croissant des énergies renouvelables entraîne un développement rapide des technologies de l'électronique de puissance. Une large partie de la production d'énergie renouvelable se fait en courant continu ou à fréquence variable, c'est pourquoi des convertisseurs électroniques de puissance sont nécessaires pour obtenir du courant alternatif à fréquence fixe.

Les convertisseurs en électronique de puissance sont largement utilisés dans des applications de tension allant jusqu'à +/-1MV et de puissance allant jusqu'à plusieurs GW. Étant donné les améliorations rapides et récentes des semiconducteurs de puissance comme les modules Si, SiC et GaN pour les applications à haut rendement, il est nécessaire de disposer des nouvelles commandes de ces interrupteurs.

Le principe de fonctionnement des convertisseurs est basé sur la commutation des interrupteurs. Ceux-ci offrent de nombreux avantages, notamment de faibles pertes en conduction, une vitesse de commutation élevée, et une bonne tenue en tension qui augmentent l'efficacité et la densité de puissance. Cependant, ils posent certains défis, tels que l'augmentation des interférences électromagnétiques qui perturbent le fonctionnement du convertisseur. Les circuits de commande de grille (driver) fournissent des interfaces entre le signal de commande et les semiconducteurs, et constituent également une voie de passage pour les interférences électromagnétiques en raison des éléments parasites de leur alimentation isolée. Ceux-ci font partie des éléments qui peuvent agir sur les commutations et réduire les interférences électromagnétiques générées par les interrupteurs dans les convertisseurs. Premièrement, ils protègent les circuits de commande de grille en limitant la quantité d'interférences qui les traversent et qui permettent de maintenir leur fonctionnement des convertisseurs. Deuxièmement, ils réduisent les interférences électromagnétiques générées par les circuits de commande au niveau des semiconducteurs en modifiant la forme d'onde de la tension de grille.

Tout d'abord, un demi-pont MOSFET SiC 1,7 kV du commerce est utilisé dans un convertisseur continu/continu de type dual active bridge (DAB) de 100 kW, contrôlé par un driver du commerce. L'amplitude incontrôlée des interférences électromagnétiques perturbe la fermeture des semi-conducteurs. Ce phénomène est ici appelé "auto-perturbation" et empêche le fonctionnement du convertisseur à tension et puissance nominales. Cette partie de l'étude montre la nécessité de nouvelles techniques de commande de grille pour réduire les interférences liées aux commutations.

La deuxième contribution, traite du défi que représente la perturbation de la grille due à la commutation rapide dans les convertisseurs à base de MOSFET SiC. Un problème bien connu de perturbation de la tension de grille lors des commutations des semi-conducteurs entraîne un phénomène d'auto-perturbation. Ce problème est résolu par l'ajout d'un élément à un circuit de commande classique. Il est proposé de filtrer le courant parasite entrant dans la grille par une inductance bifilaire en mode commun. Grâce à cette méthode, les interférences électromagnétiques traversant les drivers sont également réduites. Cette partie montre la sensibilité de la conception des circuits de driver et des sondes de mesure. Les performances d'une sonde de tension optique isolée sont évaluées en mesurant la tension grille-source des semi-conducteurs. Cela clarifie la manière dont les éléments parasites des sondes de mesure affectent les mesures et permet d'optimiser la conception des circuits de commande de grille.

La dernière contribution est le développement d'une nouvelle technique de circuit driver. Un nouveau driver doté d'une boucle inductive est conçu sur la base de la mesure du courant de drain ou de source des MOSFETs. L'ajustement dynamique du courant de grille réduit les interférences générées grâce à une tension et un courant de commutation modérés. La commande de grille proposée permet un meilleur compromis entre les pertes et la CEM par rapport aux méthodes classique d'ajout de résistances en série.

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Introduction

1.1 General introduction

Electricity is the fastest-growing type of the end-use energy consumption [78]. In addition electricity generation is one of the leading cause of industrial pollution all over the world because it is mostly produced from coal, nuclear and non-renewable power plants [78]. Renewable energy sources can be used to produce electricity with fewer environmental impacts. To achieve more clean energy, Europe announced the 2030 climate and energy framework. Its objectives include [140]:

1. At least 40% cuts in greenhouse gas emissions (from 1990 levels).
2. At least 32 % share for renewable energy.
3. At least 32.5 % improvement in energy efficiency.

One of the solutions is that energy industry integrates more and more renewable energy resources. For Europe to meet ambitious de-carbonisation targets, renewable energy sources are expected to increase significantly in final energy consumption by 2030 [140].

To integrate renewable energies to the grid, the new grid requires the development of new technologies. That made power electronics systems increasingly popular [86]. Power electronics can change renewable energies from being minor energy source to act as important power sources [16]. Hence, the power electronics which

control the flow and conversion of electrical energy is an important research area for integrating renewable energies [121]. To achieve this objective High/Medium Voltage Direct Current (HVDC/MVDC) technology offers several advantages compared to Alternating Current (AC) transmission such as power transmission between unsynchronised AC distribution [115]. For this purpose, DC/DC converter is an expected technology for MVDC/HVDC transmission systems (see Fig. 1.1). The converter excellent features fit various HVDC projects [59, 127].

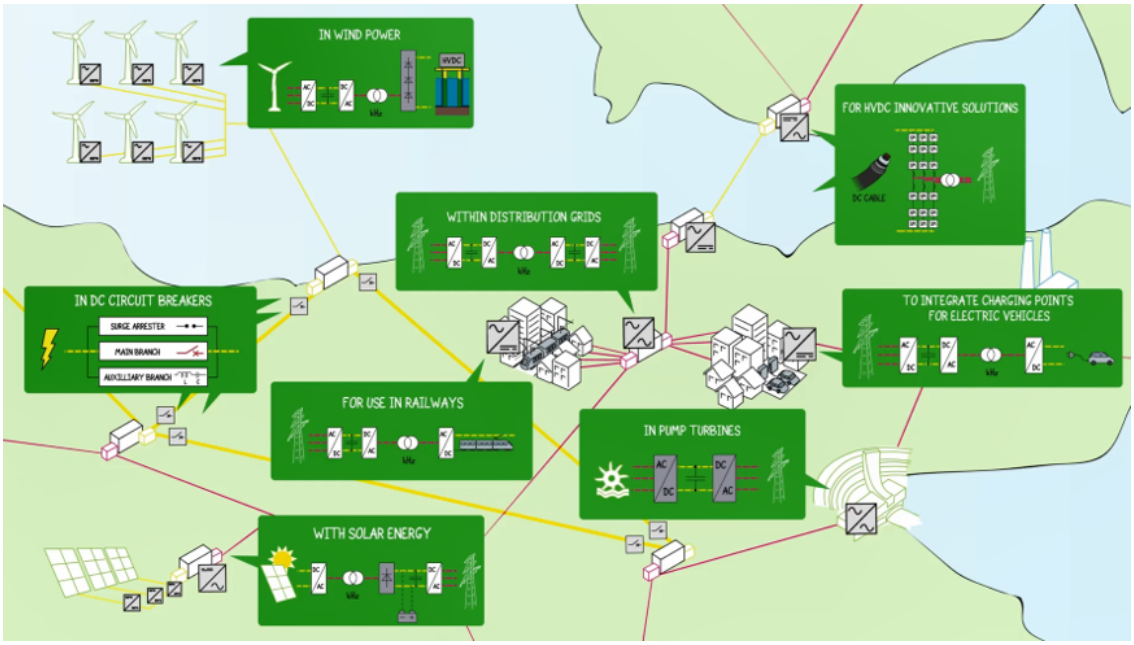


Figure 1.1 – Converter applications in integrating the renewable energies to transmission and distribution grids [145].

High frequency power electronic converters based on solid state transformer (SST) gain considerable attention due to their numerous functions including regulation, power quality, power control, efficient interface for distributed generation and storage management [93, 95, 129]. Figure 1.1 shows examples of converter applications in future electrical networks.

Converters are composed of semiconductor devices operating in switching modes. The power quality in a distribution system with high penetration of renewable energy resources highly relies on power converter switching transients [17]. Using high frequency switching components such as SiC MOSFET offers a solution to improve power density of converters but due to its fast switching nature it increases the level of interferences [82].

In converters, gate drivers serve as an interface between the control strategy (switching sequences) and the power switching action. So gate drivers are one of

the elements that can help converter designer to advance through fast switching and increase the converter efficiency.

In this chapter, the necessity of the present work in the field of power electronic to develop renewable energy integration to grid and energy transmission is explained. SiC MOSFET switching steps will be explained in details. Then the role of gate driver in switching transition is explained. Moreover, it lays the basic information for the material presented in chapters 2 to 5 which focus on the gate driver design, the electromagnetic interferences of the gate drivers and switching transitions.

1.2 Why SiC MOSFET based converter?

Previous section explained the important role of power electronic converters in electricity industry. This section explains how new technology of semiconductors can improve the efficiency and power density of converters. The switching elements of the converters enable to regulate the level of current and voltage. Wide-bandgap (WBG) power semiconductors as switching elements of converters allow power electronic converters to reach higher power density and efficiency and thus they recently appear in commercial products. Silicon-carbide metal-oxide-semiconductors field-effect transistors (SiC MOSFET), as one type of WBG devices is able to switch higher voltages faster and with higher switching frequency. Faster switching leads to less losses [94].

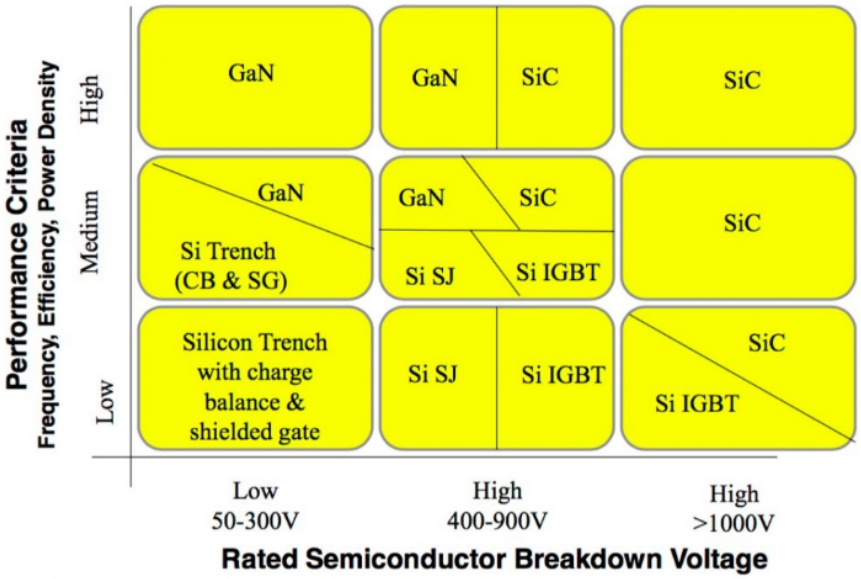


Figure 1.2 – WBG comparison for high/medium voltage application [11].

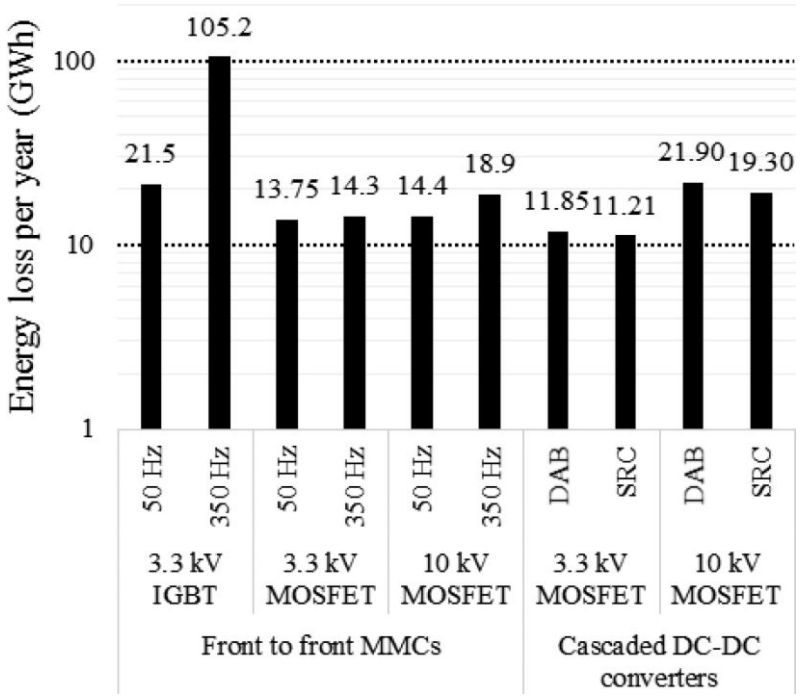


Figure 1.3 – Converter energy loss per year for different solutions [87].

The SiC material characteristics provide devices with a very high-blocking voltage (see Fig. 1.2). These characteristics make it very attractive for MVDC/HVDC application as an enabling factor to answer the constantly increasing demand for higher power density and higher efficiency in many power-electronic applications. Industrial fields such as rail traction, grid transmission and distribution system are currently working on R&D development on these devices.

SiC MOSFET power devices are expensive, so the benefit of using them rather than another cost-effective technologies has to be huge [11]. The comparative investigation reported in [87] presents an example of the energy losses per year for different converters comparing two different technologies of semiconductors for HVDC applications. The big amount of energy saving by using SiC MOSFET is not negligible as reported in figure 1.3. In this survey the cost of energy per year has been considered as 150 $\frac{\$}{MWh}$. It is shown by using 3.3 kV SiC MOSFET for front to front MMC, it can save more than 13 $M\$$ per year. This gain can be increased by Dual Active Bridge DC/DC converter. In this estimation the price of SiC MOSFET is not considered, however, by ongoing development on the SiC MOSFET semiconductors, the price is decreasing yearly [105].

One of the good examples that is commercially mature is the 1.7 kV SiC MOSFET power module from Wolfspeed manufacturer [168]. This device provides low on-resistance resulting in low power losses compared with Si devices in a same ranges [47, 128]. The device is well established and well cost-optimized in the range

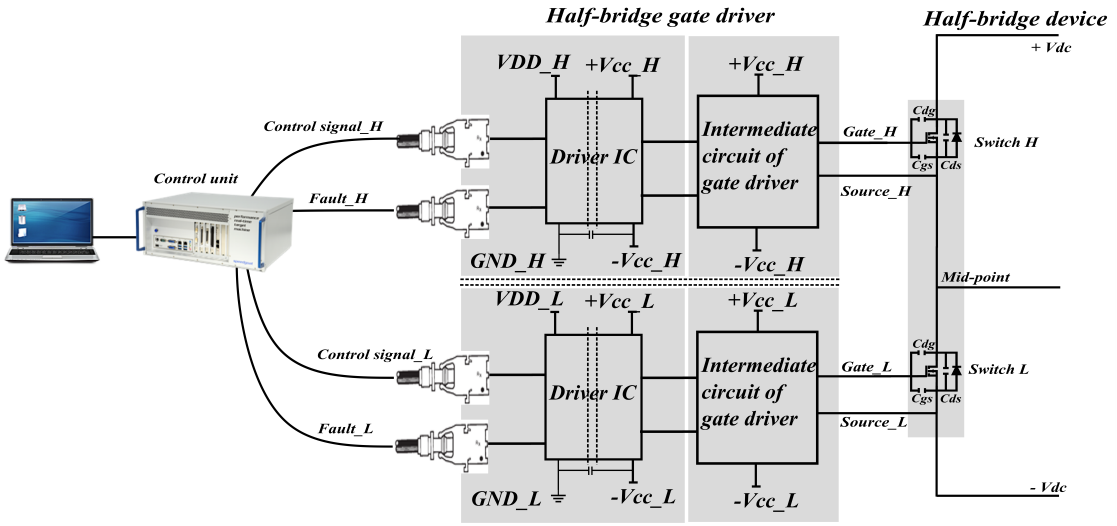


Figure 1.4 – Control unit and gate driver for medium/high voltage power semiconductor.

of 1200 V to 1700 V which makes it as a suitable choice to replace Si IGBT in medium voltage range converters.

1.3 Gate drivers for controlling power SiC MOSFETs switching

1.3.1 Classical gate driver for SiC MOSFET

In power electronics applications, the control signals are provided by a controller unit (DSP, FPGA, etc). Depending on the application, the signal can be transferred through fibre optics or by wires (see Fig. 1.4). The control signal is synthesized and transferred to the semiconductors by a gate driver unit. So with the help of gate drivers, power switches turn-on/off and that is how converters can regulate the voltage and current.

For small power/low voltage application, the control signal is provided by the ICs with voltages in the range of 3.3 V to 5 V. Very few power devices can be directly driven by the digital outputs [143]. For medium/high voltage applications, an intermediate circuit is needed to convert the low power signals to higher voltages/currents to drive the power switches. The intermediate circuit receives the turn-on/off signals from IC and convert it to the suitable level of voltage/current for turning on/off the power semiconductors (see Fig. 1.4).

The basic function of an IC driver in a gate driver unit mainly includes following tasks:

1. Provide sufficient current/voltage levels to an intermediate circuit of gate driver.

2. Provide protection units including Desaturation and Miller clamp for power switching devices under certain conditions (sending fault signals to controller in figure 1.4).

3. Provide isolation for control signals from the large signal swings of the power switching devices.

There are many IC drivers for power devices on the market. In case of normally off field-effect components like SiC MOSFETS, the drivers are called "FET IC drivers" [139]. As it has been explained for medium/high voltage semiconductors, the device is turned-on/off with bigger voltage bias. Then the needed current/voltage to turn-on/off the device is provided by the "push-pull" electronic circuit. There are many commercial IC drivers called push-pull (totem-pole) driver [14, 15]. The push-pull structure is adapted to the structure of the intermediate circuit of the gate driver (see Fig.1.5) which provides enough voltage bias for fast turn-on/off transition of the power switch.

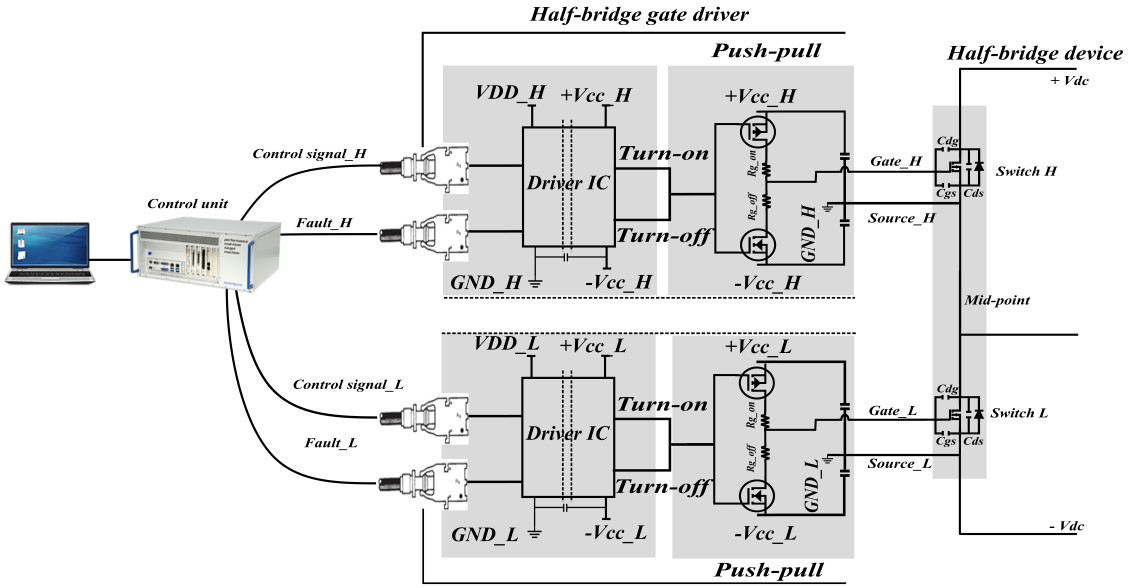


Figure 1.5 – Control unit and intermediate gate driver circuit with push-pull for medium/high voltage power semiconductor.

Switching transition of the SiC MOSFET involves charging and discharging the parasitic elements which are due to the physics of the semiconductor (see parasitic capacitors C_{dg}, C_{gs} and C_{ds} in Fig. 1.14). For medium/high power semiconductor, in order to have minimum switching transition time, it is necessary to provide enough current/voltage bias to charge and discharge these input and output capacitances of the power SiC MOSFET. This current/voltage is provided by the push-pull circuit

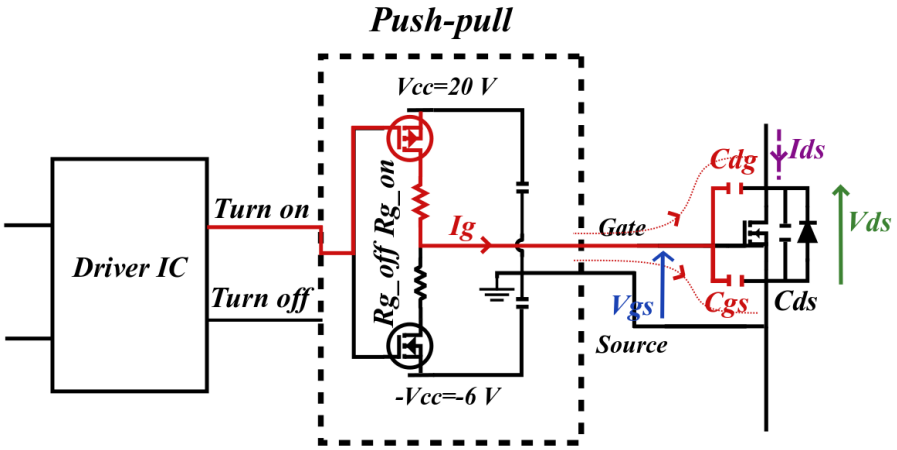


Figure 1.6 – Turn-on transition of SiC MOSFET with push-pull circuit.

in the intermediate gate driver circuit. Figure 1.5 shows the classical push-pull output stage of the gate driver. The combination of NMOS and PMOS transistors constitutes the push-pull circuit. In this structure, the gate of these transistors are controlled and tied to each other in order to receive the on/off orders from IC drivers. The drain nodes of the push-pull transistors are connected to each other to form the gate current and gate bias voltage of the power semiconductors. The SiC MOSFET switching transition with the help of intermediate circuit is detailed in following section.

1.3.2 SiC MOSFET switching-transition

In this part, turn-on/off transitions of the SiC MOSFET with the help of the push-pull gate driver are described. Understanding the role of each element of gate drivers in addition to the parasitic elements of semiconductor which act during switching transition is necessary. It gives a basis to control the switching transition and to achieve an optimised gate driver.

1.3.2.1 Turn-on transition of SiC MOSFET

Turning on the PMOS in the push-pull circuit will charge the output node and pull up the output potential to turn-on the power device (see Fig. 1.6). The turn-on event of the SiC MOSFET semiconductor can be divided into four intervals as depicted in figure 1.7.

In the first step the input capacitance of the device is charged from 0 V to V_{th}. The big amount of current provided at the beginning of this period is needed to transfer the channel status from open to saturation state. During this time slot, most of the gate current is charging the C_{gs} capacitance. A small current flows

through the C_{dg} also (see Fig. 1.6). As the voltage increases at the gate terminal, the voltage across C_{dg} is faintly reduced. This period is called turn-on delay. During this period both I_{ds} and V_{ds} remained without changes.

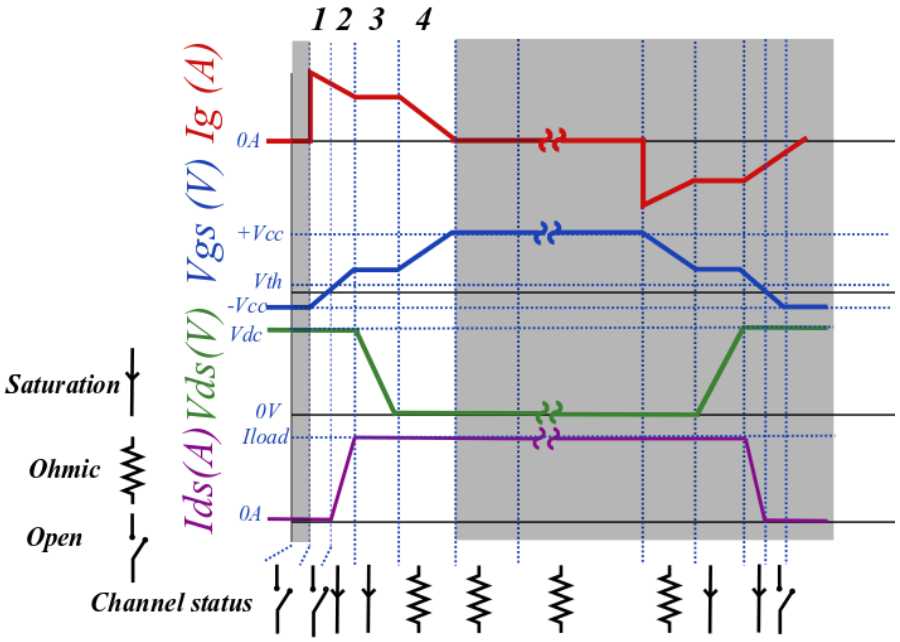


Figure 1.7 – Turn-on transition intervals of SiC MOSFET.

Once the gate is charged to the threshold voltage (V_{th}), the MOSFET is ready to carry the current. Therefore, in the second step, the gate bias is rising from V_{th} to the Miller level. On the gate side, the current is flowing into the C_{gs} and C_{gd} capacitors like during the first time slot and that is how the gate bias voltage is increasing (see Fig. 1.6). On the output side of the device, I_{ds} is increasing while V_{ds} is constant (off-level). Until I_{ds} is totally transferred into the MOSFET and the V_{ds} stays in its off level.

In the third period, the gate is already charged to the sufficient voltage (C_{gd} and C_{gs} are charged completely), therefore, the device is ready to carry the entire load current (I_{ds}). This allows V_{ds} to fall. During the V_{ds} falling period, V_{gs} stays constant. This is the Miller region in the gate voltage waveform and this is the time interval where the gate driver can affect the switching transition. It can be seen how the duration of this period in V_{gs} waveform can change the conduction of the drain current. All the gate current available from the driver is diverted to discharge the C_{gd}. This discharge facilitates the rapid voltage change of V_{ds}. Therefore, if the gate current varies at the beginning of this period, the I_{ds} rising would have changed also. The V_{ds} drop also depends on the I_{ds} current.

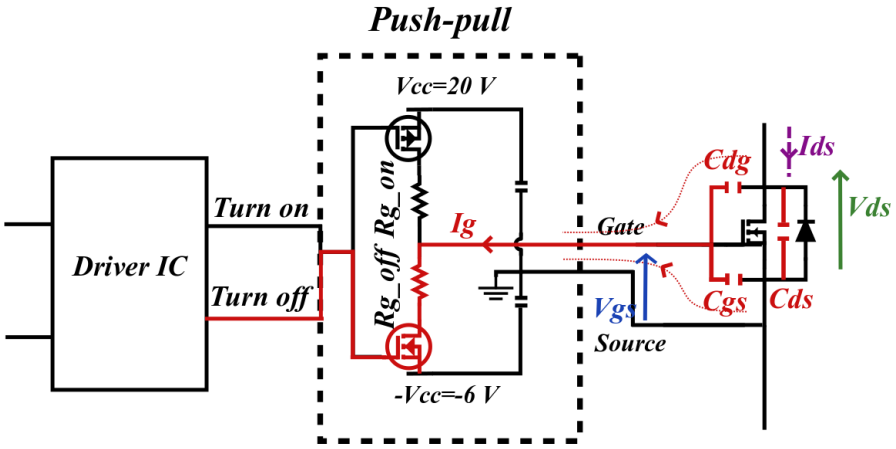


Figure 1.8 – Turn-off transition of SiC MOSFET with push-pull circuit.

The forth step is called "fully turn-on" period. To fully enhance the conducting channel of the MOSFET, it is needed to apply a higher gate voltage. Therefore, in this period, the gate reaches the final value of the gate bias.

V_{gs} increases from the Miller region to the final value (here for 1.7 kV SiC MOSFET, the value is equal to 20V). This step is accomplished by charging C_{gs} and C_{gd}, therefore, the I_g is split between these two capacitors. As long as these capacitors are charged, I_{ds} is still constant and V_{ds} is decreasing as the on resistance of the device (in the physics of the device) is being reduced. When the gate bias reaches Vcc, V_{ds} drops to almost zero. In this step I_{ds} is the full load current and V_{ds} is defined by the $I_{ds} * Rds_{on}$ (Rds_{on} is the drain-source on resistance in the physics of the device).

1.3.2.2 Turn-off transition of SiC MOSFET

By turning on the lower NMOS and turning-off the upper PMOS, the output node will be discharged below the threshold voltage (V_{th}) of the device and turn-off starts. In other words, the turn-off procedure of the SiC MOSFET can be presented as back tracking of the turn-on procedure.

First interval, like turn-on procedure is the turn-off delay. This is the time required to discharge the C_{gs} and C_{gd} capacitors from its initial values to the Miller level (see Fig. 1.8). During this time, the gate current lead to discharge the $C_{gs} + C_{gd}$. V_{ds}, starts to increase slightly as V_{gs} is decreasing from its maximum value. I_{ds} current is still constant.

In the second period, V_{ds} rises from the $I_{ds} * Rds_{on}$ value to the final Vds_{off} level (V_{dc}). During this period (Miller region in V_{gs}), the gate current is strictly provided by the discharging current of the C_{gd} and C_{ds}. The phenomena during this period

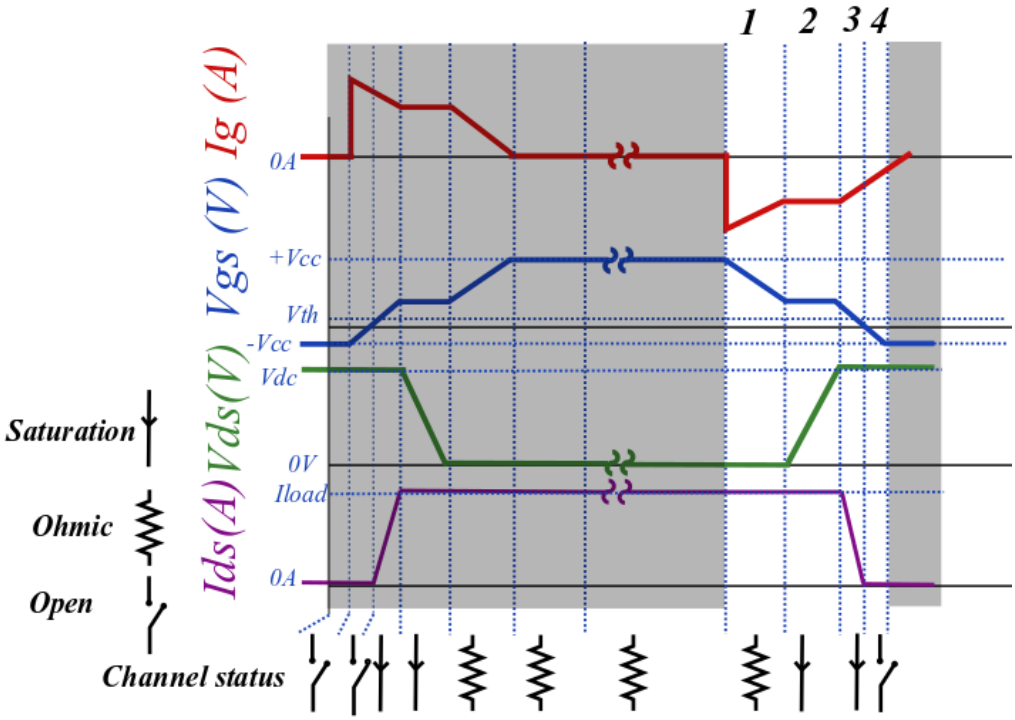


Figure 1.9 – Turn-off transition intervals of SiC MOSFET.

depends on the gate bias. Changing the gate bias in this period leads to change the gate current and consequently the V_{ds} rising time (switching time).

At the beginning of the third, V_{gs} resumes falling down to V_{th}. In this part, the majority of the gate current is provided by discharging the C_{gs}. The MOSFET is in its linear operation and I_{ds} reaches zero by the end of third time slot (see Fig.1.9). This is the second step where changing of the gate bias can modify the gate current and consequently the discharging process of the C_{gs}. In this period, by regulating the gate bias by means of the gate driver, it is possible to modify the switching transition.

The last step of the turn-off procedure is when both C_{gd} and C_{gs} are fully discharged and gate current reduced (see Fig. 1.9). V_{gs} is reduced down to reach negative bias. I_{ds} and V_{ds} remain constant.

It can be seen that all the four time steps in turn-on and turn-off procedure are functions of the parasitic capacitance values and also the required voltage variation across these capacitors. For the commercial power module, we are not able to change the capacitances unless by adding external capacitances in gate drivers. But, changing the voltage across them can change the gate current and consequently the switching transitions. That is how gate driver can act on switching transition. In other words, the switching speed can be modified by steps 2 and 3 in both turn-on

and turn-off. This emphasizes the importance of the optimised gate drive technique for high speed and high frequency switched mode power converters.

1.3.3 Conduction and switching losses

When a switch is turned on or off, energy is lost. This type of the energy loss is called switching loss of the power switch and it depends on the voltage across the switch and the current passing through the switch. In addition the switching duration is a main player of the switching losses (see Fig. 1.10).

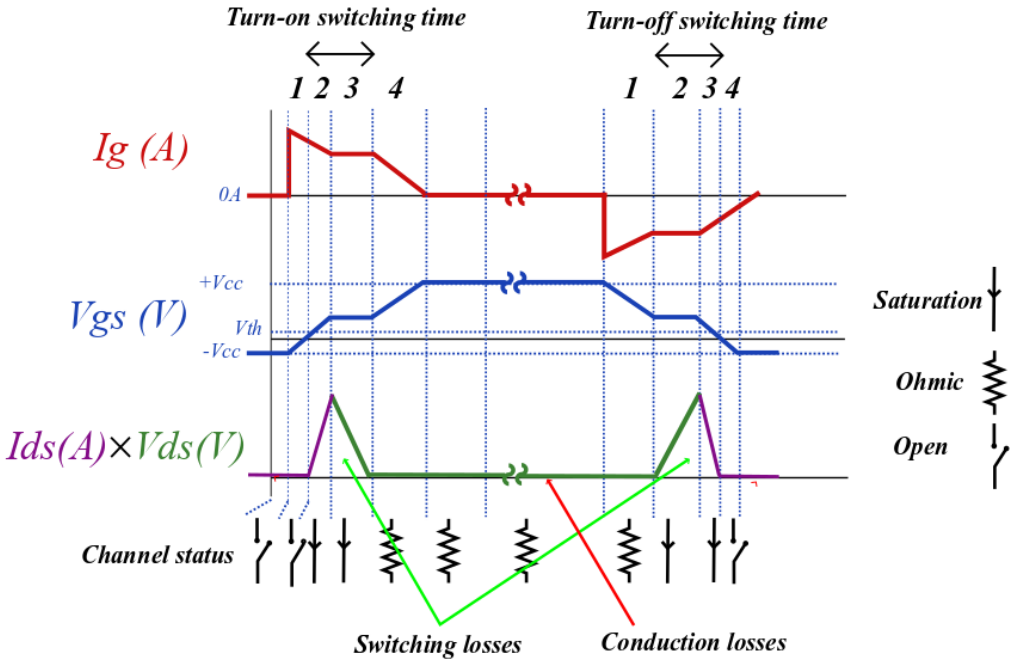


Figure 1.10 – Switching transition considering switching losses and conduction losses.

When a switch is off, usually the leakage current through the switch is negligible. But when the switch is on, the energy loss depends on the current through the switch and a forward voltage of the switch. This type of energy loss is called conduction loss of the switch (see Fig. 1.10).

The average power loss in a switch over one switching cycle is given by the following equation which consists of the conduction and switching losses:

$$\overline{P_s} = \frac{1}{T_{sw}} \int_0^{T_{sw}} I_{ds} V_{ds} dt = \overline{P_{sw}} + \overline{P_{cond}} \tag{1.1}$$

assuming that the on and off switching times are small compared to switching cycle, T_{sw} and the leakage current is negligible. Thus the conducted losses can be calculated based on equation 1.2.

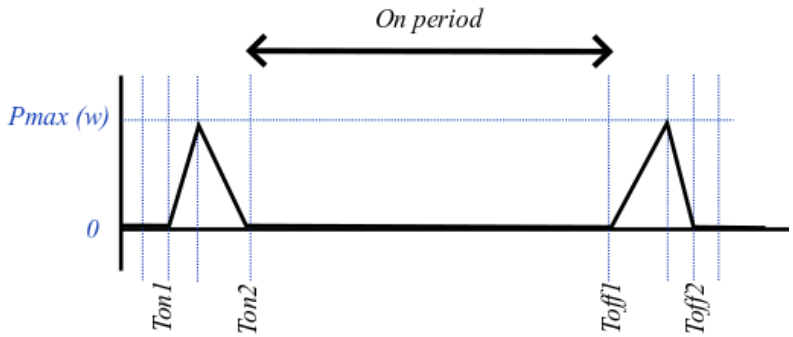


Figure 1.11 – Switching and conduction losses.

$$\overline{P_{cond}} = V_{on} I_{on} D \tag{1.2}$$

where D can be calculated based on the following equation:

$$D = \frac{T_{on}}{T_{sw}} \tag{1.3}$$

Assuming the time intervals for turn-on and turn-off process of the switch as they are marked as switching time (T_{on} and T_{off} in figure 1.11), the switching losses can be calculated as:

$$\overline{P_{sw}} = f_{sw} \left(\int_{Ton_1}^{Ton_2} I_{ds} V_{ds} dt + \int_{Toff_1}^{Toff_2} I_{ds} V_{ds} dt \right) \tag{1.4}$$

where Ton_1 and Ton_2 are the times when gate signals are applied to turn-on the device. Like turn-on, the $Toff_1$ and $Toff_2$ are the times when the gate signal applied to turn-off the device. This equation shows that the switching losses is proportional to the switching duration. In another words slower switching transition leads to longer switching period and this results in increased losses. This explains the trend towards the fast switching in power converters and the new researches to use SiC MOSFETs as switching elements in converters. As it can be seen, the main part of the losses in the power converter is due to the switching losses which depends on the switching times and switching frequency.

Although fast switching is the solution to increase the efficiency, it increases the $\frac{di_{ds}}{dt}$ and $\frac{dv_{ds}}{dt}$ across the switch which affects the electromagnetic interferences generation. In all power electronic systems, there are stray inductances (L) and capacitances (C) due to interconnections between the power components via wire, parasitic capacitances of the semiconductors and parasitic capacitances due to different level of voltage potential between conductors. In a power electronic circuit when a power switch is turned on/off, stray inductances associated with a current

loops are charged and discharged. The energy stored in the inductor depends on the current magnitude and inductance value. Each time that the switch is turned on/off, it creates significant over voltage during switching transition due to the rate of change of current.

$$V_{ov} = L\frac{di}{dt} \tag{1.5}$$

On the other hand, the capacitive couplings (C in equation 1.6) in the layout of the converter are charged and discharged during turning on/off of the switch. The energy stored in the capacitors depend on the voltage magnitude and capacitance value. It creates significant pulse current when the switch is turned on/off.

$$I_{ov} = C\frac{dv}{dt} \tag{1.6}$$

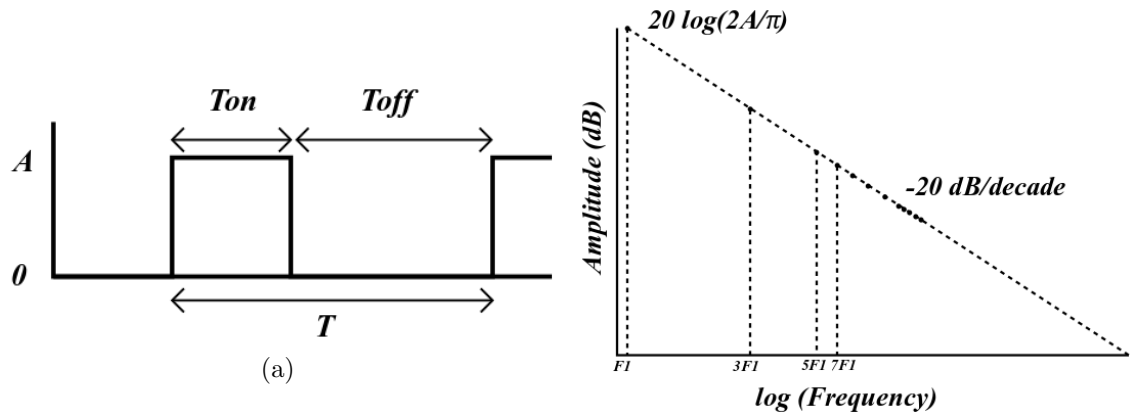
Therefore, two major sources of electromagnetic interferences in power electronic are $\frac{dv}{dt}$ and $\frac{di}{dt}$ during switching times. In fact, a DC voltage of few hundreds volts is switched by a power semiconductor in a short time (few tens nano seconds) which creates significant leakage current. Although these generated interferences can be reduced by decreasing switching speed, but decreasing the $\frac{di}{dt}$ and $\frac{dv}{dt}$ means increasing losses. Thus the converter designers should find a proper trade off between losses and EMI to determine the switching time and benefit the semiconductor potential. The other alternative is to reduce the stray inductances of power electronic system using a better layout, interconnection of components and converter configuration.

1.3.4 EMI reduction and trade-off with losses

It has been explained that the switching slew rate is the origin of the electromagnetic interferences in switching mode power converters. To understand the effect of the switching slew rate in generating EMI, the spectral analysis of different waveforms are depicted in figures 1.12 and 1.13.

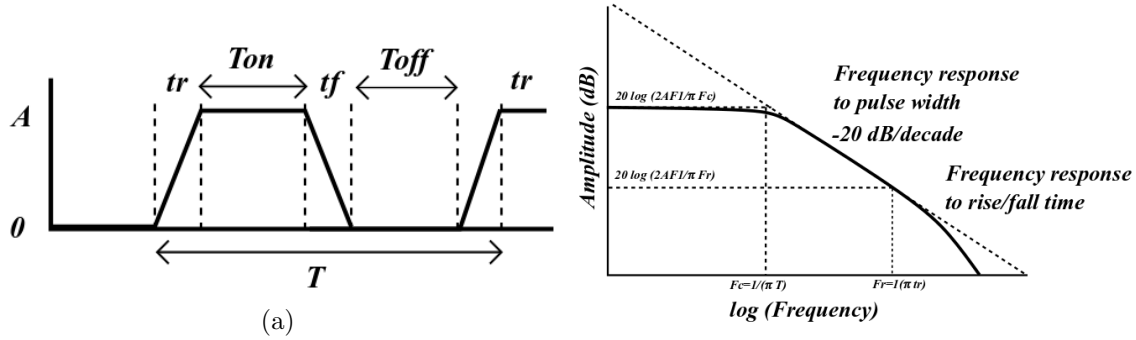
Figure 1.12 shows the a square waveform of the period T with amplitude A for an ideal switch. This waveform can be the idealised representative waveform of the drain-source voltage or drain/source current of the semiconductors. The waveform has several important timing parameters that determine the spectral envelop for EMI.

1. The overall period T which is the fundamental frequency that is $F1 = \frac{1}{T}$.
2. The on and off times, T_{on} and T_{off}.
3. The amplitude A



(a) (b)

Figure 1.12 – Square waveform (a) Time domain representation (b) Frequency domain spectral.



(a) (b)

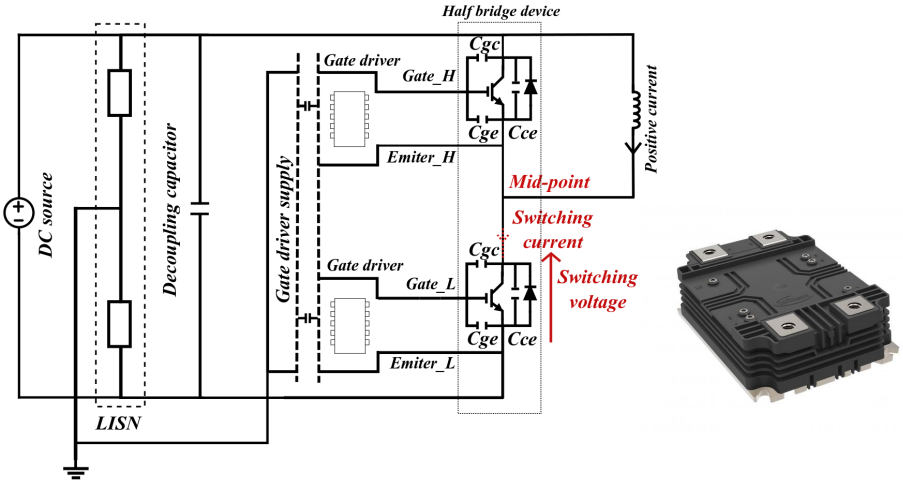
Figure 1.13 – Trapezoidal waveform (a) Time domain representation (b) Frequency domain spectral.

To determine the spectrum, or frequency components of this waveform Fourier analysis is a common method for representing any repetitive waveform. The fundamental frequency can be seen as a cut-off frequency (see Fig. 1.13), above which the amplitudes of frequency components falls off with inverse frequency. The $1/F$ fall-off causes an amplitude reduction of the harmonics of 20 dB/decade, as shown in figure 1.12.

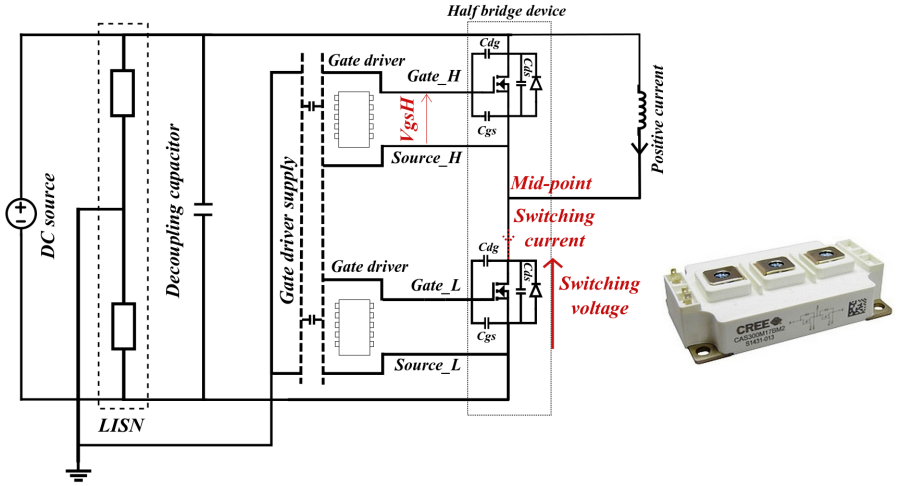
Voltage/current waveform of the semiconductors are not like an ideal waveform presented in figure 1.12.a. It has been shown in section 1.3.2 that the voltage/current waveforms can be approximated by a trapezoidal waveform with finite rise/fall times. Figure 1.13 shows a trapezoidal waveform with amplitude A in a period T. Considering rise time and fall time of t_r and t_f respectively, its frequency evolution shows the cut-off frequency variation based on the period T, t_r and t_f. Because the rise and fall times are finite, the energy of harmonics at high frequencies is less than that of an ideal square wave. A faster switching (small rise/fall time) shifts the cut-off frequency towards higher value. In this way, parasitics elements

might be subjected to this voltage/current variation. It can reduce losses but emissions can pass through parasitic elements and disturb the proper functions of the converter.

Here to show the effect of fast switching (high voltage/current slew rate) in voltage and current waveform oscillations, the switching characteristics obtained with 1.7 kV SiC MOSFET (CAS300M17BM2 package) and a 3.3 kV IGBT (FF450R33T3E3, XHP3 package) have been experimentally compared in a clamp inductive circuit for half-bridge device (see figures 1.14 and 1.15). This circuit represents the classical architecture to evaluate the half-bridge device as the fundamental switching cell of most of the converters (The platform is presented in chapter 3 in details).



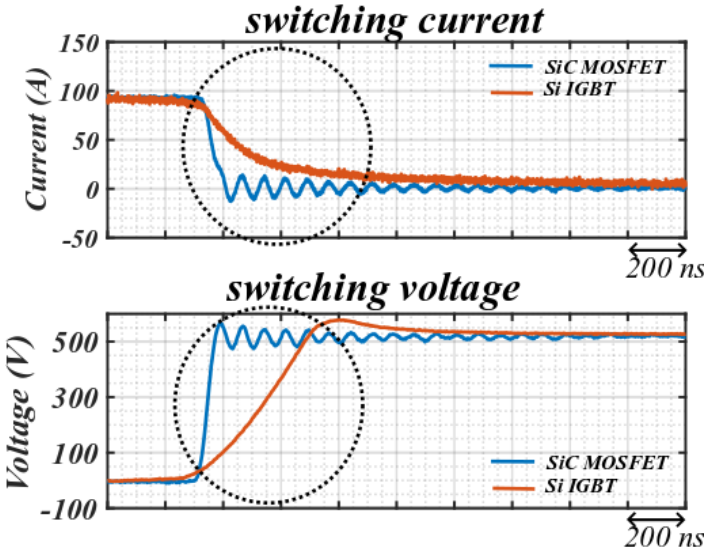
(a)



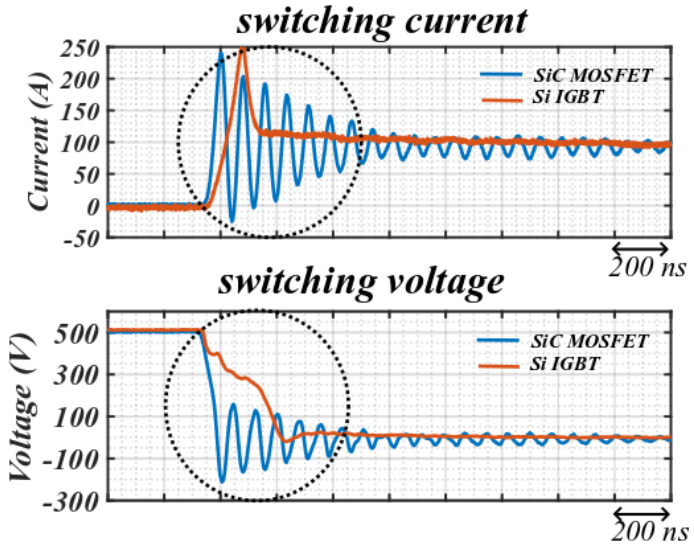
(b)

Figure 1.14 – Semiconductor characterising circuit (a) SiC MOSFET characterising (b) IGBT characterising

The switching waveforms comparison has been shown in figure 1.15. By pushing up the switching speed of the SiC MOSFET and the IGBT power module to obtain minimum switching losses (minimum external gate resistance), it can bee seen that the SiC MOSFET obtained almost 4 times faster switching transition compared to the IGBT (see Fig. 1.15). However, during turn-on and turn-off transition, the SiC MOSFET switching creates voltage and current oscillations (overshoot). The fast variation of voltage and current across the switch, creates these overshoots of voltage and current (V_{ov} and I_{ov}) (see equations 1.5 and 1.6).



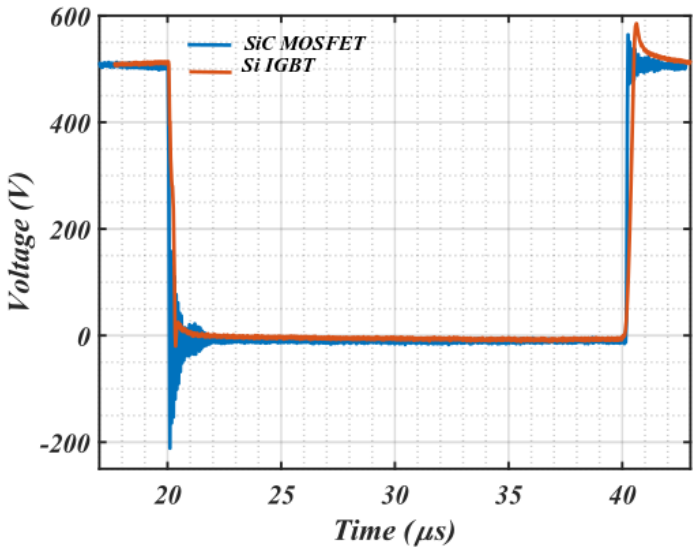
(a)



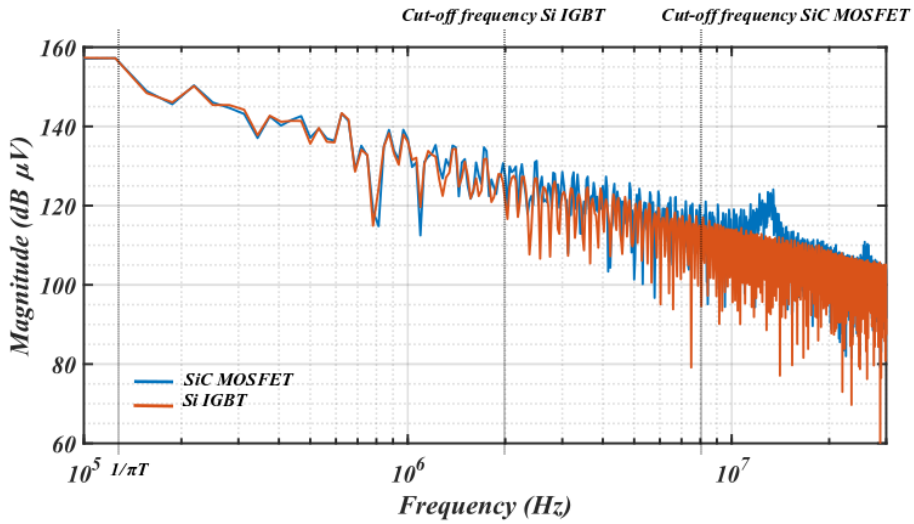
(b)

Figure 1.15 – Experimental comparison between switching characteristic of Si IGBT and SiC MOSFET in 500 V DC voltage, 100 A of load current (a) Turn-off transition (b) Turn-on transition.

These figures show realistic waveforms due to the existence of the parasitic elements in the converter layout. Oscillation appear as resonant peaks in high frequency and, as it has been explained, the parasitic elements became more and more important in higher frequency which can disrupt the operation of the converter. The effect of this fast switching in increasing the electromagnetic interferences is depicted in figure 1.16. The frequency spectra of one switching period of IGBT and SiC MOSFET are compared in this figure. It can be seen that the SiC MOSFET switching speed moved the cut-off frequency in higher value which increases the excitation of parasitic elements in the layout of the converter.



(a)



(b)

Figure 1.16 – Experimental comparison between switching characteristic of Si IGBT and SiC MOSFET in 500 V DC voltage, 100 A of load current (a) Voltage time domain representation (b) Voltage frequency domain representation.

This experimental comparison revealed the significant difference that should be considered in terms of driving and protecting SiC MOSFET compared to Si IGBT which should be encountered in gate driver design [56].

1.4 EMC definition

Electromagnetic compatibility (EMC) is the ability of electrical equipments and systems to function properly in their electromagnetic environment. The proper function happens by limiting the unintentional generation, propagation and reception of electromagnetic energy. Uncontrolled electromagnetic energy may cause unwanted effects such as electromagnetic interferences (EMI) or even physical damage in operational equipments [166]. The goal of EMC study is the correct operation of different equipments in a common electromagnetic environment.

EMC study covers usually three main topics (see Fig. 1.17):

1. Electromagnetic emissions or disturbances: indicate the disturbing electrical equipments that can disrupt the operation of other equipments.

2. Electromagnetic susceptibility which indicates the capacity of the device to withstand disturbances from other electronic devices in the vicinity or from the environment.

3. Coupling which describes the phenomenon of disturbances propagation that occur between the sources and the victims.

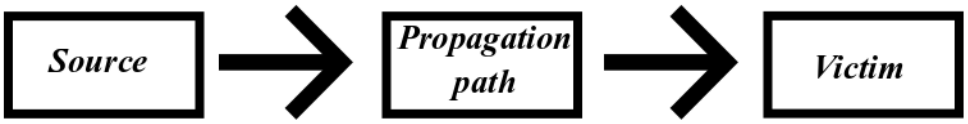


Figure 1.17 – Elements of EMC study.

Based on above definition, there is a source of perturbation which produces electromagnetic interferences (EMI). This electromagnetic interferences propagate through the coupling paths and depends on the type of these coupling paths (conducted or radiated) and can disrupt the other electrical devices (victim)(see Fig. 1.17).

1.4.1 Conducted and radiated emissions

If the source and the victim are distant and without galvanic connection (the source and victim are in separate circuits without electrical connection), the parasitic energy between the source and the victim is transmitted through a magnetic field

(H) and an electric field (E) or in the form of an electromagnetic wave (see Fig. 1.18). These disturbances are called **radiated** disturbances. This type of disturbances normally appears from 30MHz [8].

If the source and the victim of EMI are nearby (close coupling) with or without galvanic link, the coupling path at low frequencies can be due to the electrical connection (capacitive, resistive, inductive or the combination of all of them). This disturbances are called **conductive** disturbances (see Fig. 1.18). They propagate through power or transmission cables as well as in energy source or load. The conducted emissions disturb the electronic equipments in lower frequency compared to radiated from 150 kHz to 30 MHz [8].

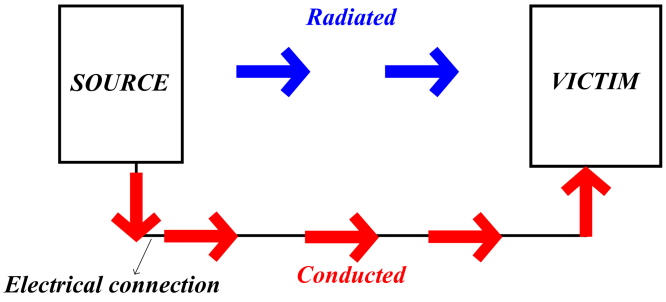


Figure 1.18 – Conducted and radiated emissions.

In this work, the EMC study focuses only on conducted emissions. The perturbation occurs in the range of kHz which can be seen in the spectrum of voltage and current in the following chapter 1.5. The conducted disturbances occur either in common-mode (CM), or in differential mode (DM)(see Fig. 1.19). Both modes of disturbances may exist simultaneously, however, the separation of these modes makes the study simpler. In complicated electrical system (like multi-level converters), the DM mode can be transferred into CM mode and vice versa.

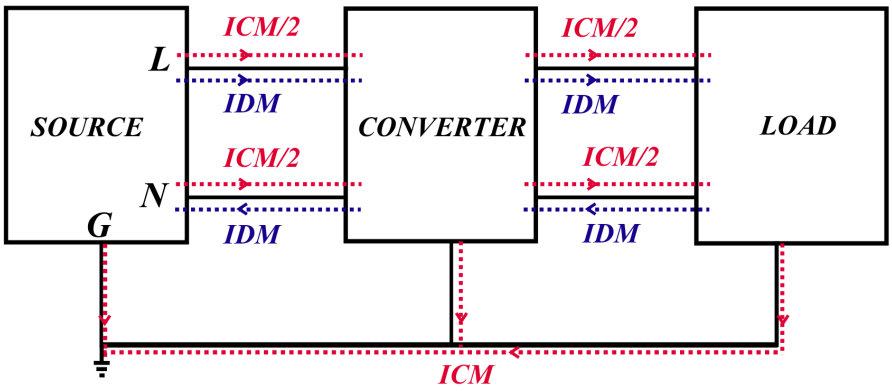


Figure 1.19 – Differential and Common-Mode in converter.

Common-Mode disturbances (CM): The CM current (noise) propagates in the same direction on all the conductors (phases) and is looped back by the ground

(most of the time through the parasitic capacitors). The voltage of this mode is calculated from the average of the voltages between each phase and ground. In converters mostly large and rapid variations of the voltage ($\frac{dv}{dt}$) generates the CM noise (see Eq. 1.6) [8].

Differential-Mode disturbances (DM): The DM current (noise) propagates symmetrically by one conductor passing from the source to the victim then to the load in a power electronic converter system. The DM voltage is applied between two conductors. The noise is returned to its source through another conductor in inverse direction. In switched mode converter, this current is generated mostly by high $\frac{di}{dt}$. (see Eq. 1.5) [8].

1.5 EMC in power electronic converters

As it has been explained, the EMC issue in power electronic converters rely on the switching cell as the source of perturbation [36].

In the following section, the appearance of oscillations due to parasitic elements will be discussed.

1.5.1 Conducted emissions in a switching cell

In the section 1.3.2, the fundamental switching cell of the switched-mode power converter has been shown. The generated electromagnetic interferences due to voltage/current variation propagates towards the load and the supply network or even to the source of EMI through the electrical connection. In practice, during switching transitions in a converter, the switching cell includes many parasitic elements which causes DM and CM noises. To explain the results of figure 1.16, the fundamental clamped inductive circuit shown in figure 1.14 is transformed into figure 1.20. This circuit shows the principal parasitic elements contributing in generation of conducted noises (voltage and current oscillations).

The existence of these parasitic elements is unavoidable in the converter layout. In general, there are two groups of parasitic elements which contribute to the voltage and current waveforms: the switching loop parasitic elements and the power loop parasitic elements. All the parasitic elements in the semiconductors in addition of the parasitic elements in the gate drivers shape the switching loop. On the other hand, the parasitic elements which are due to the layout of the converter and connection to the semiconductors create the power loop.

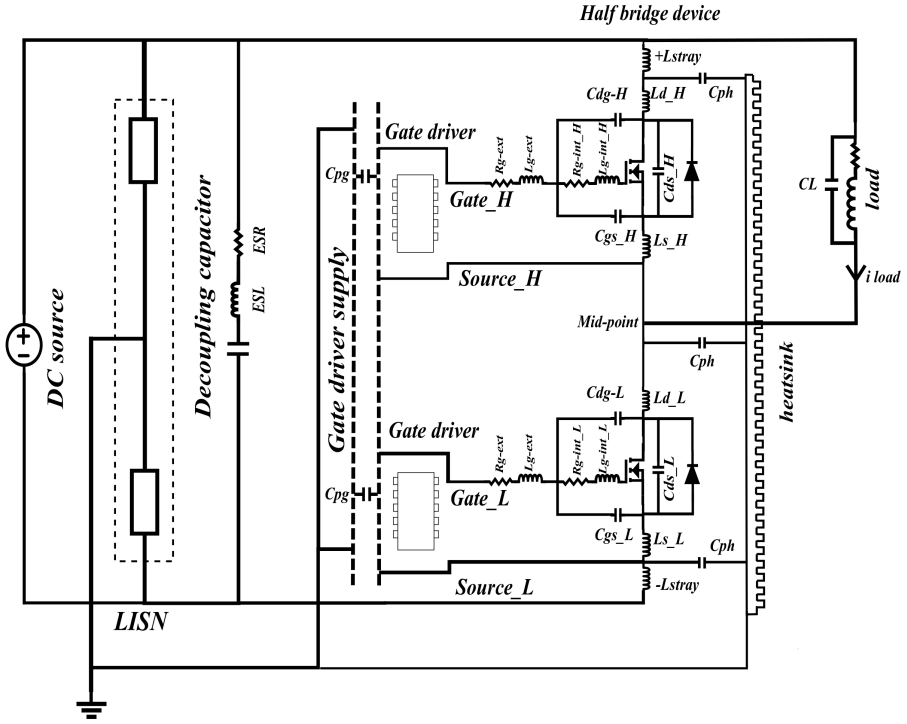


Figure 1.20 – Half bridge switching cell considering parasitic elements.

In the figure 1.20, besides the parasitic capacitances corresponding to the physics of the SiC MOSFET presented in section 1.3.2, CL is the equivalent parallel capacitance to load. $Lg-int$, $Ld\_L + Ls\_H$ and $Ls\_L + Ld\_H$ are respectively the gate inductance, switching inductance and common-source inductance introduced by the packaging of the semiconductors. L_strays are parasitic inductances caused by the drain and source terminals of the device connected to the DC bus (converter layout). Rg_{int} and $Rg-ext$ are respectively the inner and external gate resistance of the DUT. The $Lg-exts$ are the parasitic inductances created by the connection of the gate terminals of the device to the gate driver plus the gate driver parasitic inductance (PCB tracks).

Based on equations 1.6 and 1.5, the high $\frac{di}{dt}$ in the wiring (normally shown as L) is the source of the differential perturbation and the cause of voltage overshoot in the converter (see Fig. 1.21).

While, when the propagation coupling is capacitive, high $\frac{dv}{dt}$ excites these coupling paths and the noise is propagated through these capacitive couplings. This is the main cause of ground current overshoot in the converter. The propagated CM noise in switching cell is shown in figure 1.22.

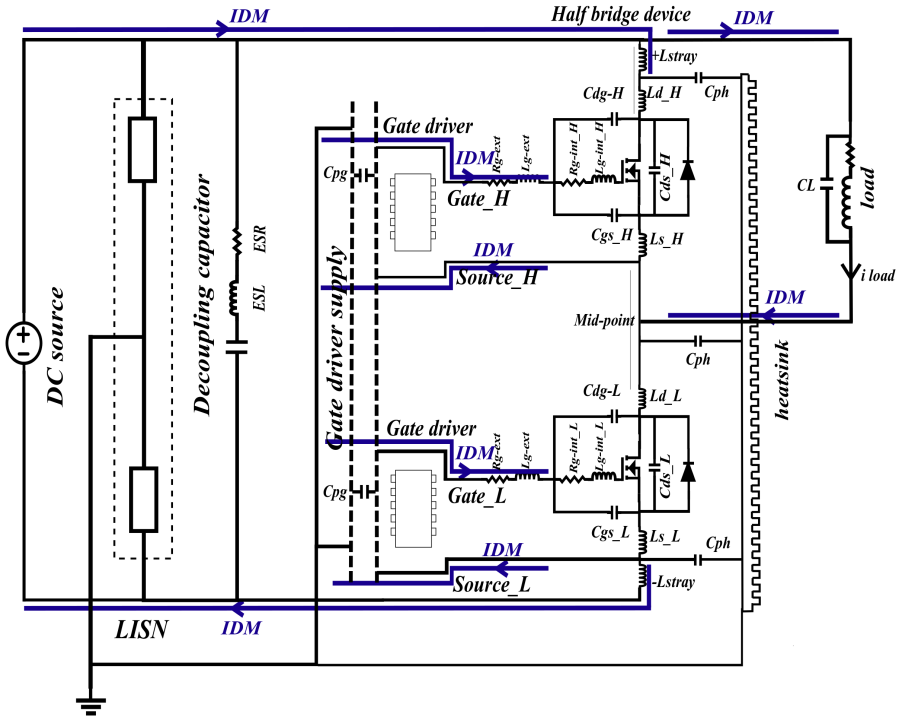


Figure 1.21 – Conducted emission, differential noise in switching cell.

1.5.2 Voltage/current overshoot in switching transition

Typical information on MOSFET switching waveforms are listed in the data-sheet of the device. However, these numbers correspond to the specific test conditions which make the comparison of products from different manufactures difficult. This is because the measurement set-up is different in most of the cases. This difference stems from the switching ringing and switching slope shown in figure 1.15. The cause of switching ringing phenomenon of SiC MOSFET is widely reported [120].

It is very difficult to separate the effect of the parasitic elements of each component of the test circuit in switching oscillation [116, 172, 173]. However here the main parasitic elements which contribute to switching oscillations are presented in figure 1.20 and the effect of gate driver to reduce the effect of these parasitic elements in switching ringing will be discussed.

In this configuration, the body diode of the high-side switch is the element which conducts the load current during the free-wheeling phase. The C_{ds} parasitic capacitance in the data-sheet of the SiC MOSFET includes the parasitic capacitance of the device plus the parasitic capacitance of the body diode. For analysing the switching oscillations, the low-side switch is the controlled component whereas the only function of the high-side switch is to conduct the load current during off state of the low-side switch. Therefore, the switching oscillation can be controlled only

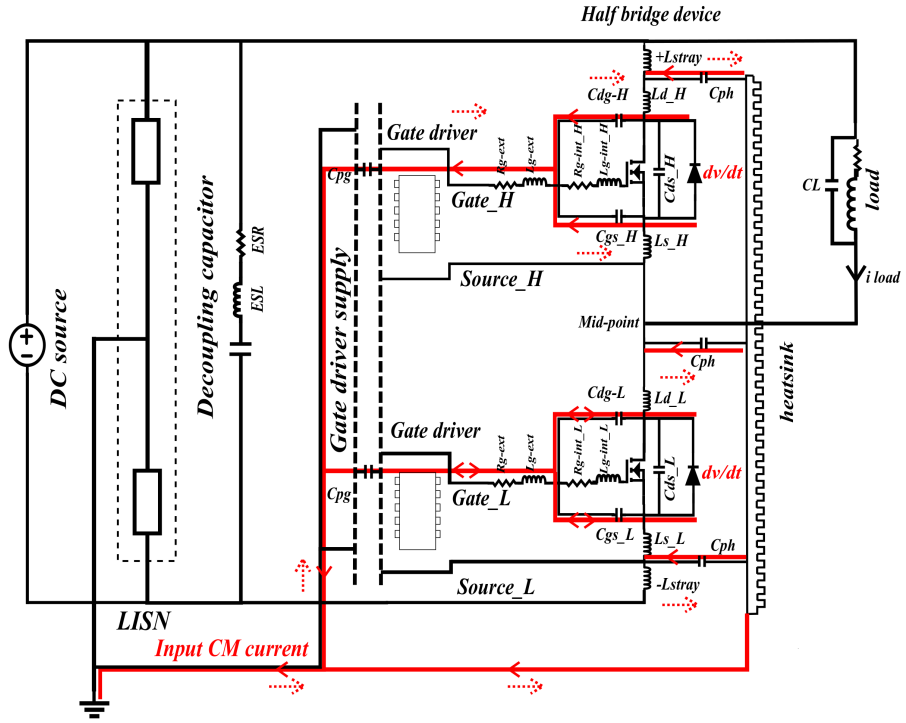


Figure 1.22 – Conducted emission, common-mode noise in switching cell.

by the low-side gate driver. It will be the same when high-side switch is controlled as well.

The switching waveform considering the parasitic elements are presented in figures 1.23 and 1.24. In this part, the cause of ringing in the half-bridge switching transition will be discussed. To explain the created voltage and current overshoot, it will be focused on the phases 2, 3 and 4 of the turn-on and turn-off transitions. When the current and voltage across the switches changes and the channel status as well. Then the effect of gate driver to change the switching slew rate in order to control the electromagnetic interferences is discussed.

1.5.2.1 Turn-on switching ringing

As it has been explained in section 1.3.2, based on current and voltage behaviour across the switch, the turn-on and turn-off transition of the SiC MOSFET are divided into 4 time intervals. Figures 1.23 and 1.24 show the transition intervals with additional effects of the parasitic elements.

During delay period, interval 1, when the gate voltage changes, the applied gate current is a function of the gate inductance which is depicted in figures 1.23. The applied gate voltage is constant during this time therefore, the gate impedance is changing, the rise/fall time of the gate current and consequently the charging/discharging of the gate capacitances (C_{gs} and C_{gd}). The gate impedance is

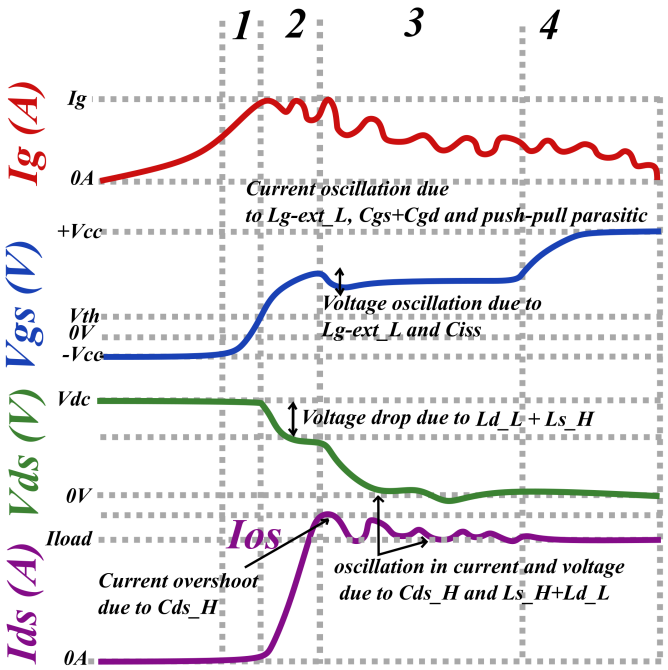


Figure 1.23 – Switching ringing during turn-on transition due to the parasitic elements.

the sum of $Rg-ext$, $Rg-int$, $Lg-ext$ and $Lg-int$, considering that the gate inductor is mainly due to the PCB tracks in electronic board and that the gate resistance is chosen during the design stage. Therefore, the lower impedance leads to higher current and shorter delay time interval. One of the practical techniques which influences the gate impedance and helps fast switching and consequently reduces the gate current ringing is to place the push-pull circuit as close as possible to the gate terminal of the device under test.

In phase 2, when the gate voltage reaches the threshold voltage of the SiC MOSFET and the device starts to conduct current (saturation region), the drain-source terminals keeps blocking the dc bus voltage while the current continues flowing through the high-side body diode. By increasing Ids, the current variation across the parasitic inductances (L_d $+L_s$) causes a voltage drop on Vds. In this stage, the peak gate current varies based on the Vcc value. Therefore, modifying the gate bias in this periods leads to change the blocking drain-source voltage and consequently the drain current. In many gate drivers, by adding series resistance into gate, the impedance of the gate changes and consequently the peak gate current changes also. This leads to longer Miller region and consequently slower switching transition. The problem with this classical technique is the added impedance due to series resistance in all the switching intervals. New techniques try to effectc during specific parts of Miller region in order to reduce the effect of long Miller period. These techniques are discussed in chapter 4.

Phase 3 is the interval where the drain current ringing happens. This is the time when drain current reaches its peak. Current ringing occurs under the resonance of the output capacitance of the device (C_{ds}) and the parasitic inductances includes L_d and L_s in the switching loop and also the L_+stray and L_-stray in the power loop. Therefore, controlling the current variation slope can reduce the ringing in this step. The gate impedance is constant, then the V_{gs} is changing the gate current and charging of the input capacitance. Also this period can be modified by gate driver as the element which can change the driving voltage bias. If V_{gs} reaches its maximum in a longer period, the Vds drops slowly which decrease $\frac{dv_{ds}}{dt}$.

1.5.2.2 Turn-off switching ringing

As it has been explained, the turn-off transition is the opposite tracking of the turn-on, therefore, the turn-off delay follows the same phenomenon as turn-on (see Fig. 1.24).

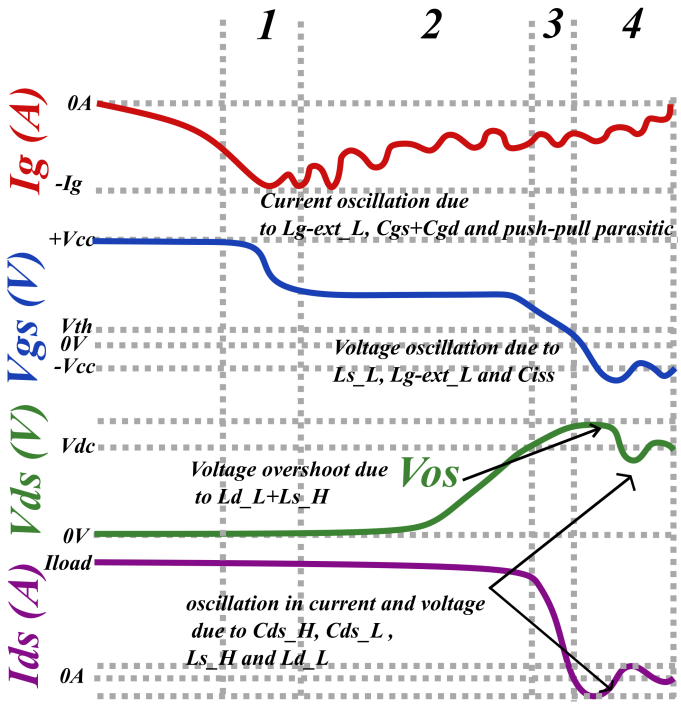


Figure 1.24 – Switching ringing during turn-off transition due to the parasitic elements.

In phase 2, during voltage rise time, I_{ds} keeps the same value until V_{gs} reaches the Miller level. Because V_{ds} is not high enough, I_{ds} is still i_{load}. This is the phase where the device passes from the saturation region to the ohmic region.

In time interval 3, the drain current decreases with V_{gs}. The drain current is transferred to the body diode of the high-side switch. Therefore, the voltage overshoot happens due to the $\frac{di}{dt}$ across the L_stray, L_d and L_s. This is one of the

region where the gate driver can act on during turn-off transition in order to control the current/voltage slope.

In phase 4 of the turn-off process, although the turn-off process is finished, the input capacitance of the device will continue to discharge. Meanwhile, as a result of resonance between the parasitic inductance of power loop (L_stray) and output capacitance of the device (C_{ds}), V_{ds} continues to oscillate even when the current I_{ds} reaches the zero level.

In the last interval, the current ringing is happening. The parasitic elements of the load in resonance with the parasitic element of the body diode of the high-side device (mostly C_{ds}) creates current ringing. In this region also gate driver can control the amount of ringing by controlling the rate of change of drain current. This can be done by changing the gate bias.

1.5.3 EMI phenomenon related to gate drivers

In section 1.3 role of gate driver has been explained. Then the main circuit of the gate driver and how this circuit turns-on/off the switches was explained. In this section, it will be shown how gate driver can be one of the victims of EMI in converter. It has been explained that the gate driver has to provide at least two functions in converters. The signal transmission and the power supply for switching [58]. The signal transmission includes signals for switching orders and protection of the device (see Fig. 1.25). The signal transmitter (for example opto-coupler) provides isolation between the controlled input signal and the gate of the power switching device. This isolation stage appears with $C_{gd,iso}$. The power supply provides a voltage source to produce enough voltage bias for power semiconductors. The design of the power supply is challenging since this part of the circuit should provide a high isolation with a low coupling capacitance (see DC/DC converter in gate driver in the Fig. 1.25). The presence of the parasitic coupling capacitances in the isolated supply (C_{pg} and $C_{gd,iso}$) in half-bridge gate driver is unavoidable.

As it has been explained, the CM current flows through capacitive coupling and return through cables to the earth (see Fig. 1.22). Moreover, it has been shown how parasitic elements provide the propagation path. Then in a switched mode converter, these parasitic capacitances in the power supply of the gate drivers represent a path of CM current [34] (see Input CM current in figure 1.22). So passing the large amount of CM current through gate drivers makes gate drivers as potential victims of the EMI. This issue is depicted in each following chapters of these dissertation.

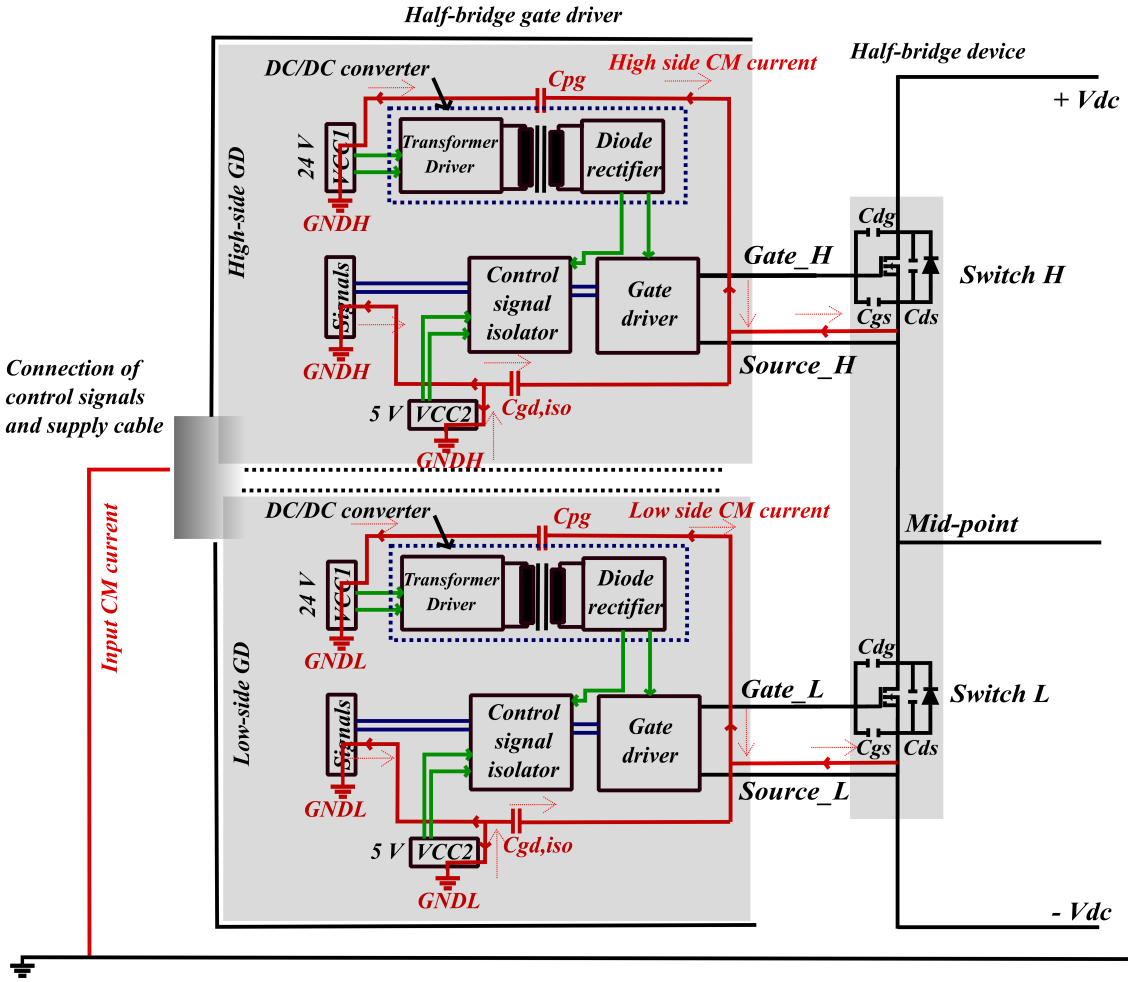


Figure 1.25 – CM current path in half-bridge gate driver.

The C_{pg} of the gate drivers is normally much higher than the $C_{gd,iso}$ which leads to lower impedance. Therefore, CM currents is higher through C_{pg} than the $C_{gd,iso}$. However, since they are sharing the same ground (GND in figure 1.25), the CM current can still disturb the control circuit. The risk of control disruption can be reduced by using optical fibres for transferring the control signal. Optic fibre technology leads to reduce significantly the value of $C_{gd,iso}$. However, as it can be seen in figure 1.25, due to ground layout, the risk of control disruption always exists.

It is very important that converters can work properly in a complicated electromagnetic environment. Thus, electromagnetic compatibility (EMC) is a significant characteristic of any electronic device including converters. Filtering the generated EMI maybe one of the common solution. However, EMI filter usually occupies significant volume of total converter. Hence, reducing the EMI noise of power converter can help to reduce the volume of EMI filter and to improve the total power density of the converter [92, 93].

A limited CM current passing through the gate driver is required in order to guarantee proper operation of the gate drivers and consequently converters. This concept addresses the EMC study of the gate driver in this PhD work.

1.6 Thesis objectives

To overcome ringing, several actions can be carried on. The parasitic parameters of devices and converters should be optimised by a novel device structure. The package layout can be optimized. Special care must be taken in the design of the converter [118, 170, 183]. It is possible to control the switching (current/voltage slops) as well by means of gate driver as one of the elements which can change the switching transition and generated ringing. The switching transition modification is the main objective of the present work. However, in general, reducing the switching slops can reduce the EMI but it increases losses. In this work, it is aimed to reduce the EMI while finding a better trade-off with losses compared to existed solutions is one of the main criteria.

The Wolfspeed 1.7 SiC MOSFET power module has been chosen to be studied in this project as one of the most mature commercial products with the highest voltage and current rating in recent years (3.3 kV, 6.5 kV and 10 kV SiC MOSFETs are still in the R & D prototyping stage). The fast switching, optimised package and well established characteristics of this power module greatly hindered the applications of this device in power electronics. In this work also, this device is used as a switching leg in the considered converter. This research work has been carried out in SuperGrid Institute as a industrial partner in collaboration with the Ampère laboratory (academic partner).

1.6.1 Academic objectives

Si IGBT is standard for switching elements in a converter in many applications. However, SiC MOSFET based converter are suffering by the big amount of electromagnetic interferences. Then it comes to the question that if there is a certain methodology to study the EMI behaviour of converters to face this challenge and benefit SiC MOSFET characteristics? The second question might be how to define or apply this methodology based on system requirements to solve the electromagnetic interferences issue due to SiC MOSFETs?

It is highly important to answer those two questions to considerably increase the power density, reduce the losses and deal with EMI in SiC MOSFET based

converters. In industry, the main actual solution is to decrease the switching speed to overcome EMI. Therefore, due to rapid growth of converter application, in order to increase the efficiency of the converter, there are several researches going on to find a proper solution which does not affect the losses. So as from the academic side, this work was included in the research activities that is ongoing in the field of high voltage engineering and wide band gap components for high voltage conversion in École centrale de Lyon and Ampère Laboratory.

1.6.2 Industrial objectives

The present work is financed by SuperGrid Institute company. The main mission of SuperGrid Institute is to offer value-added technologies and services to support the development of electric power systems that aim to increase energy efficiency and integrate renewable resources into the grid on a wide scale [145].

Among 5 research programs, this project is included in the activity of power electronic and converters technology group. Where the researchers focus on developing power electronic technologies that meet the requirements of the future DC grid. The research topics cover innovative technologies of converters to build highly efficient MVDC/HVDC transmission system, notably to use in DC transmission line.

It has been explained how new WBG devices such as SiC MOSFET can help to integrate more and more renewable energies into grids. However, it comes with some challenges that need to be studied profoundly. This work was accomplished in this context and it is based on the IGBT gate driver prototype designed and developed for controlling the IGBTs as the switching elements of converters (see Fig. 1.26) in SuperGrid institute.

The project is based on an intensive experimental program to achieve the following objectives:

1. Highlight the main differences between the IGBT and SiC MOSFET gate driver.

2. Test and verify the difference between the switching performance of the commercial IGBT and SiC MOSFET switches which affect the gate driver design.

3. Benefit of switching as fast as possible with SiC MOSFETs while dealing with generated EMI.

4. Investigate and highlight the effect of the gate driver on EMI behaviour of converters.

5. Propose a solution by means of gate driver for SiC MOSFET based converter to reduce the current/voltage oscillations in order to reduce EMI in converters.

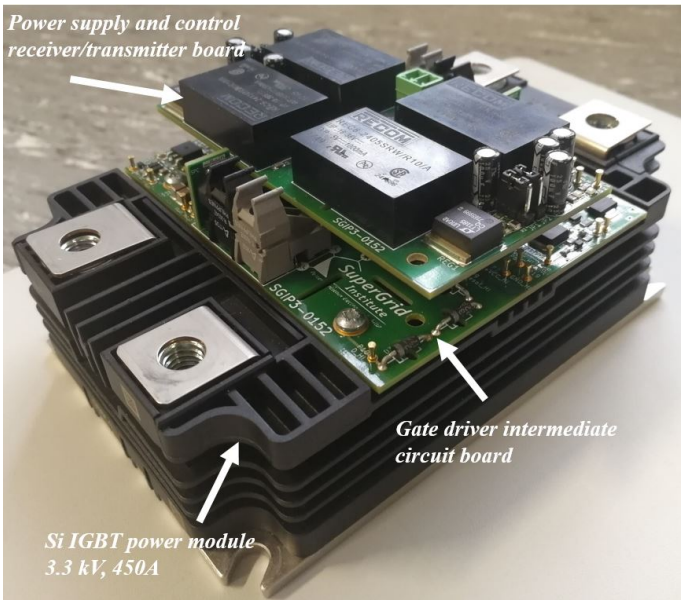


Figure 1.26 – IGBT gate driver prototype integrated with Si IGBT power module.

6. Draw the challenges and design specifications for development of the SiC MOSFET gate-driver power module for future work to be continued for higher voltage power modules in the company.

1.7 Thesis outline

The dissertation includes 6 chapters. **This chapter** explains the motivation and the need of using SiC MOSFETs in converters. Then, the difficulty of using SiC MOSFETs is detailed. The effect of gate driver as the element which can influence the switching behaviour of the SiC MOSFET is described in this chapter. Then how modifying switching characteristics can change EMI is reported. The objective and test platform needed to achieve those objectives are highlighted as well.

Chapter 2 presents a system-level EMI investigation in a new 3-phase 1.2 kV 100 kW insulated DC/DC converter. In this converter, achieving full operation is prevented by false triggering. This false triggering is called in this dissertation "self-disturbance". The study reveals the paths of common-mode currents in the converter where the gate driver circuit is one of the main path. Moreover, this chapter explains how being a CM current path can impact the operation of gate drivers and can disrupt the proper operation of the converter. A corrective solution is proposed. It allows to reach the nominal operation of the converter. This study gives a basis that we need to focus on gate driver to reduce the common-mode current passing through gate drivers. This common-mode current reduction can

improve the converter operation as well. The content of this chapter was published in the following conference articles.

I. "Conducted EMI reduction in a 100kW 1.2kV Dual Active Bridge converter" by Hadiseh GERAMIRAD, Florent MOREL, Piotr DWORAKOWSKI, Bruno LEFEBVRE, Thomas LAGIER, Philippe CAMAIL, Chrisitan VOLLAIRE, Arnaud BREARD. presented in PCIM Europe 2020 conference.

II. "Experimental EMI study of a 3-phase 100kW 1200V Dual Active Bridge Converter using SiC MOSFETs" by Hadiseh GERAMIRAD, Florent MOREL, Piotr DWORAKOWSKI, Philippe CAMAIL, Bruno LEFEBVRE, Thomas LAGIER, Chrisitan VOLLAIRE presented in European conference on power electronics and application EPE 2020.

After targeting to focus on the electromagnetic interferences reduction by means of gate driver, **the third chapter** describes the novel double pulse test platform for half-bridge power modules used as the experimental set-up for EMI study of gate driver design. The platform elements and the measurement equipments are explained in this chapter. The platform is used to examine the switching characteristics and gate driver design. Therefore, it is needed to model the test bench for future simulation studies as a first step. According to the literature review and based on the requirements of this work, a time domain modelling method has been chosen and explained to build an EMI model for the test bench. The EMI model has been simulated in LTspice and has been compared with experimental results in this chapter.

In chapter 4 one of the main differences between Si IGBT and SiC MOSFET gate driver are encountered. It discusses precisely the common-mode current generated by fast switching passing through gate-driver, which leads to driving-voltage perturbations and disturbs the correct triggering of switches. This false triggering is called in this dissertation "self-disturbance". The classical solution in gate driver design is simulated and examined experimentally for this issue in SiC MOSFET gate driver. Then a new solution is proposed and compared with the classical solution. In this chapter, the measurement technique which influences the design of the gate driver also is investigated precisely. The publications that have been compiled from this chapter are as follows.

I. "Experimental study of the self-disturbance phenomena in a half-bridge configuration of Si IGBT and SiC MOSFET switches" by Hadiseh GERAMIRAD, Florent MOREL, Bruno LEFEBVRE, Christian VOLLAIRE and Arnaud BREARD in PCIM Europe 2020 conference.

II. "Measuring small differential-mode voltages with high common-mode voltages and fast transients – Application to gate drivers for wide band-gap switches" by Hadiseh GERAMIRAD, Florent MOREL, Bruno LEFEBVRE, Chrisitan VOLLAIRE and Arnaud BREARD in international symposium on electromagnetic compatibility, EMC Europe 2020.

III. "Étude experimentale de la CEM des drivers d'un demi-pont avec MOSFET SIC et IGBT" by Hadiseh GERAMIRAD, Bruno LEFEBVRE, Florent MOREL, Arnaud BREARD and Christian VOLLAIRE in 20ème colloque international et exposition sur la compatibilité électromagnétique (CEM 2020) to be presented in October 2020.

The chapter 5, proposes an innovative solution by means of new design of gate driver in order to reduce the EMI generated by the semiconductors. This chapter focuses on reducing the EMI from the source of EMI by modifying the switching transitions. The solution is simulated and the results are analysed. Then, the final gate driver prototype considering the integrated solutions proposed in chapters 4 and 5 is experimentally validated. The new gate driver is compared experimentally with the classical increasing gate resistance solution. So as the performances are compared and the concept is validated in terms of losses while it reduces the EMI.

Chapter 6 presents a conclusion of this work, the advantages and disadvantages of the proposed solutions are explained. Moreover, the perspectives and potential applications and improvements for this work are listed in this chapter.

2

EMI study of the 1.7 kV SiC MOSFET gate driver in a 1200 V, 100 kW three-phase DC/DC converter

2.1 Introduction

It has been explained that the power converters are based on switching techniques [20]. Then in chapter 1, it has been shown that rising/falling of the voltages and currents across the switches due to switching excites the parasitic elements and creates EMI in converters. Moreover, using faster switching techniques is a trend to increase the efficiency which results in more electromagnetic interferences.

EMI study is a vast research topic. In previous chapter it has been stated that in this work it is focused on conducted electromagnetic interferences. The conducted EMI issues in converters are reported in [37, 126, 134]. Moreover, it has been detailed that how electromagnetic interferences is a common problem in all SiC MOSFET based converters. For this reason, implementing SiC MOSFETs

and dealing with the generated EMI adds a new dimension to the design of power converters.

To solve an aforementioned EMI problem in a converter, it should be considered that the parasitic elements change over their frequency band, the topology of the converter and the switching speed may vary from one design to another one. So as, there is not a well-defined design methodology for all converters. It is then difficult to have a general attitude to solve EMI problems [175]. Hence it is always a challenge to ensure that the CM current of a converter is well-controlled in order to not disturb its critical elements like gate drivers and controllers.

There are several active elements which contribute to EMI generation and propagation in a converter. The context of this work is related on the conducted emissions, precisely the CM current passing through the 1.7 kV SiC MOSFET gate driver in a converter (see section 1.5.3 in introduction chapter).

Knowing the effect of the converter elements on the CM current passing through gate driver helps designer to reach the optimised design. The design in which sensitive elements like gate drivers are less affected. Hence, identification of the CM current paths and investigation on the effect of theses paths in an isolated DC/DC converter prototype are the topics studied in this chapter. The problem stated in following sections of this chapter addresses the main goal of this PhD work.

This chapter is organised as follows. Section 2.2 describes the considered converter in this study. Section 2.3 gives a review of reported works focused on the CM current reduction in DC/DC converters. The problem observed in this converter will be detailed in section 2.4 and the CM current investigation will be shown in section 2.5. The proposed solution is shown and evaluated in section 2.6. At the end, the conclusion of this chapter and the perspectives are presented in sections 2.7 and 2.8 respectively.

2.2 Experimental set-up

The application under test is a 3-phase dual active bridge converter (DAB). The DAB topology is a well-known configuration as it features high power density, high efficiency, bidirectional power flow capability, inherent soft switching and low number of passive components [41, 131]. In general, an isolated DAB (see Fig. 2.1) consists of two voltage source converters (VSC) coupled to a Medium Frequency Transformer (MFT) for isolating the primary VSC from the secondary VSC. The DC sides of the VSCs are in parallel with capacitors C1 and C2 and the AC side of each VSCs connected to the transformer.

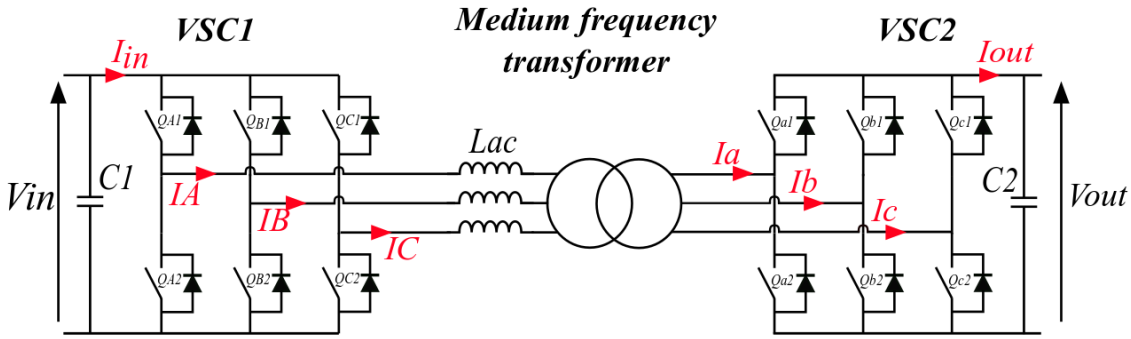
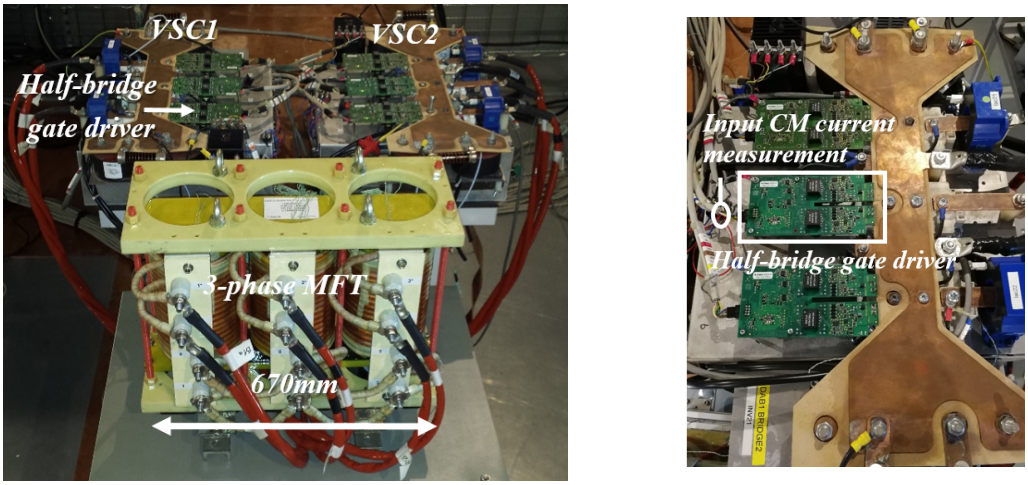


Figure 2.1 – DAB3 schematic.

The two VSCs generate phase shifted voltage with square waves. These voltages are applied to the primary and secondary sides of transformer. The corresponding phase shift changes the voltage across the transformer leakage inductor. The leakage inductance of the transformer is the main element to complete the energy transfer from primary VSC to the secondary VSC. Moreover, this leakage inductance with the help of the output capacitance of the semiconductors C_{ds} serves the soft switching mechanism in DAB topology. Most of DABs are single-phase (with two legs per VSC). The one used in this work is a three-phase converter.



(a) (b)

Figure 2.2 – DAB3 prototype (a) Converter structure (b) Input CM current measurement.

The considered 3-phase DAB (DAB3) in this work is a 100 kW converter able to switch up to 1.2 kV voltage (see Fig. 2.2). The objective of this prototype is to experiment and validate the design flow including the design tool, manufacturing and testing. The DAB3 converter prototype has been developed in SuperGrid institute and the design details are reported in [41, 89, 90]. VSCs are able to operate in single phase and 3-phase configurations. The AC link operates in the frequency range of 20 kHz allowing to optimize the efficiency according to the converter operating

point [88]. In the DAB3, all legs (1.7 kV SiC MOSFET power module [168]) inside both 3-phase VSCs are controlled to generate high-frequency square wave voltage (50% duty cycle) and are controlled with half-bridge gate drivers. The voltages created by VSCs are phase shifted with respect to each other to control the power flow through the MFT. Thus the power can be transmitted from VSC1 to VSC2 or vice versa. The transformer ratio is set to 1:1 and the connection of windings is fixed to Yy [41]. The 100 kW SiC MOSFET based converter (see Fig. 2.2) operates at 20 kHz switching frequency.

2.3 Review of EMI investigations in DC/DC converters

There are some studies focused on EMI modelling and experimental analysis of DC/DC converters [133, 137, 153] and some of them focused on DAB configuration [66, 85]. In these studies, the comparisons between experimental performance and simulation highlight the difficulty of the EMI analysis based on simulation. Moreover, these studies are focused on low voltage/power converters. On the other hand, converters topologies are different from one publication to the another one. Therefore, there is no general solution that can be applied for all converters. For instance, there are some experimental works for low/medium power flyback converters [12, 81, 109, 135] and some experimental works focused on the DAB topology [79]. However, to own best knowledge, there is no research focused on experimental EMI behaviour of a 3-phase DAB (DAB3) using SiC MOSFETs in medium/high voltage/power converter.

In general, as it has been explained in introduction, for a conducted EMI problem to be solved, there are two categories of solutions. The first consists in investigation of the switching transition (source of EMI) which acts on the current and voltage transition. The second is to minimize and optimise the coupling paths as a propagation path for interferences. A third one would be to investigate on victim side to increase immunity.

2.3.1 EMI reduction from the source

In the case of reducing the EMI from the source, reducing the switching slope is the most common way to reduce the EMI nowadays in industry. This technique comes with increasing losses. However, using SiC MOSFET and decreasing the switching

slope leads to increase the switching losses while the goal of converter designers is to decrease the switching losses.

Recently soft switching methods have been recommended to reduce switching losses which can reduce the EMI issues [29]. Soft switching techniques can be in the form of zero-voltage switching (ZVS) and zero-current switching (ZCS) methods [175]. According to the application and soft switching method, the soft switching technique restricts the $\frac{di}{dt}$ and $\frac{dv}{dt}$ of switching transition.

In recent years, several topologies of soft switching converters have been presented [1, 2, 29]. For DABs, the phase shifted control is one of the most interesting methods to achieve ZVS conditions in full bridge converter. Unlike the soft switching technique presented in [19] in which external capacitors are added in parallel with switches, phase-shift controlled soft-switching uses the parasitic elements in the circuit to implement soft switching conditions [89, 97]. Therefore, this technique does not need adding passive component to the circuit. The ZVS condition is achieved by using the resonance of the primary leakage inductance of the transformer and the output capacitors (C_{ds}) of the switches [97]. This technique was also implemented in the DAB3 in this work, the details are explained in [89].

Recently new technologies of gate drivers for controlling the $\frac{di}{dt}$ and $\frac{dv}{dt}$ of semiconductors also intend to reduce the generated EMI from semiconductors (source of EMI). This subject will be discussed precisely in chapters 4 and 5.

2.3.2 Optimised propagation paths

The second category of the solutions acts on the coupling paths [63, 114]. The CM current paths are provided by capacitive coupling. In an isolated DC/DC converter, there are plenty of coupling capacitances [33] which provide propagation paths [9, 113, 179]. Some options have been presented for mitigating EMC issues in DC/DC converters by means of optimised layout [66, 113, 162].

There are plenty of researches discussing EMI issues in systems with Wide Band Gap devices in which they try to optimise packaging of semiconductors and reduce the parasitic elements [180].

There are several studies where the effect of the parasitic capacitances in DAB elements have been measured experimentally [25, 52, 181] and also several new techniques to reduce these coupling paths [84, 137]. In most of the presented cases, a CM electromagnetic disturbance issue is due to the circulation of the CM current in the converter layout [51, 63, 109].

If we consider EMC test costs, anticipating and modelling of conducted EMI is needed at initial design stages to avoid additional test costs and re-design of the

converter elements [98]. However, after design stage, the installation of the converter is an important factor for proper operation of the converter. The coupling paths which correspond to the physical layout must be taken into account seriously when it comes to installation and prototyping of the converter. Moreover, the layout of the converter differs in each application which makes it difficult to bring out general solution for different converter structures. For instance, the effect of coupling paths in redirecting and reducing the CM current from sensitive part of the circuit has been studied through the use of shielding, filtering, interconnection modification or the combination of all of them [40, 150, 177].

Troubleshooting and removing an EMI problem in a completed prototype is a difficult task. In many cases when the electronic elements are disturbed by EMI, the first solution is the EMI filter. The size and cost of the electromagnetic filters are important for high power density converters [92–94].

There are not several studies focused on EMI issue of a completed converter. In [192] the work considered the physical layout configuration effect on the EMI of the gate driver and how the ground layout changes the EMI of the control. Reducing the CM noise of the power converter from sensitive part of the circuits can help to simplify the filter design and to reduce the total size. Moreover, in this way the problem can be solved with minimum changes on converter topology. This figured out the main idea of this chapter.

Considering all these constraints for EMI study of the converters, this chapter intends to give an insight through physical connections of the insulated DC/DC converters. The impact of this physical connections in CM current of the gate drivers will be discussed. The study is focused on the main loops of the CM current in 3-phase dual active bridge prototype (DAB3). The objective is to understand the effect of the parasitic elements which affect the gate driver operation.

2.4 Problem statement

The noise source in each leg of the VSC is the voltage variation across MOSFETs/diodes. The propagation paths are provided by the coupling capacitances in the layout of the converter which experience high $\frac{dv}{dt}$. The main coupling capacitors that are subject to fast variations of the voltage are shown in figure 2.3 in red.

The gate drivers provide an interface between the control circuit and the power semiconductors for switching. Parasitic capacitances of the semiconductors (C_{gd} and C_{gs}) provide propagation paths to gate drivers for parasitic currents created

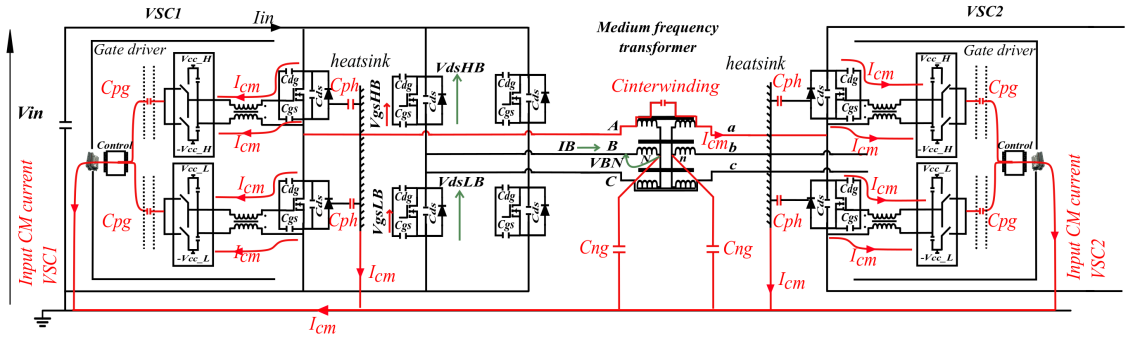


Figure 2.3 – Main CM current paths in a DAB3.

by $\frac{dv}{dt}$ across the switches (see Fig. 2.3). With SiC MOSFETs, the high-speed high-voltage variation across switches induces a CM current which can disturb the gate bias and consequently jeopardize the correct triggering of the switch. This phenomenon is called in this dissertation "self-disturbance". This shows that a significant amount of the CM current finds the gate drivers as a propagation path [9, 58]. The CM current can continue flowing to the control circuit through the capacitive coupling in isolation stage of the gate driver (C_{pg}). This may lead to disturbances of the control signals due to circulation of the CM current in the supply stage of gate driver (see Fig.1.25). Moreover, the parasitic capacitances in the isolated supply of the gate driver provide a path for the CM current to flow into the gate drivers also.

The voltage variations across the windings of the transformer turn the parasitic capacitances of the transformer as other paths in which the current can circulate [91] from one VSC to the another and also shunt the CM current into the ground (C_{ng} and $C_{interwinding}$ in Fig. 2.3) [12].

The parasitic capacitance between the device and the heat-sink provides another path for the CM current to the ground (C_{ph} in Fig. 2.3) [85]. The existence of these parasitic paths in the layout of the converter is unavoidable. Also changing the value of the related capacitances can not be done after the design phase.

Measuring all these parasitic elements in the converter layout is a difficult task. Moreover, in practice, due to physical limitations, it is very difficult to measure all the CM currents passing through these parasitic elements which makes the analysis more challenging. For example, in this prototype, the CM current passing through the heat-sink and the current passing through the parasitic capacitances of the MFT cannot be measured. In addition, when the converter is completed, changing these parasitic elements is costly and time consuming because some parts need to be reconstructed or some connections in the layout needs to be changed.

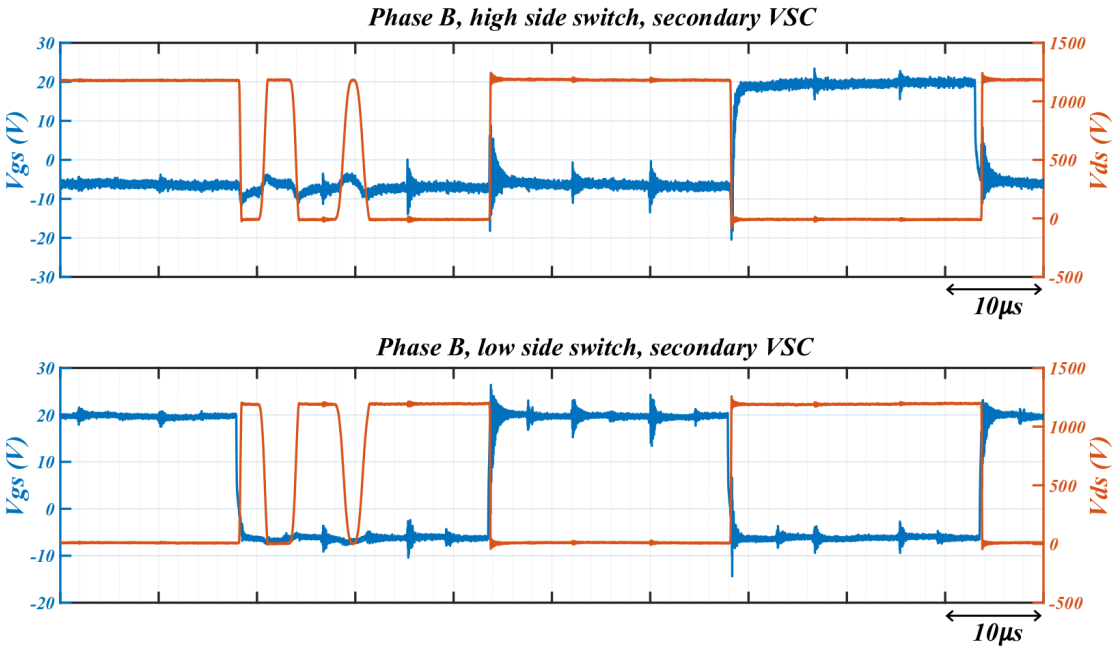


Figure 2.4 – Experiemental result of false triggering of SiC MOSFET in DAB3, 1200V, 100kW.

In the considered converter, the SiC MOSFET devices (switching-legs) are triggered between -6 V to 20 V. During normal operation of the converter, a false triggering phenomenon was observed from the DC voltage above 800 V in phase B of the secondary VSC in converter. The control signal has been sent from the controller but the switch did not receive it properly. This can be seen in figure 2.4. The measurement points has been shown in figure 2.3. The high-side switch of the half-bridge has not been triggered to on-state, while the low-side switch was turned-off. Therefore, the two switches in a same leg were in off state at the same time. The voltages across the switches in the switch-leg, phase B are shown. The sum of the two V_{ds} perturbations is equal to the DC voltage. The V_{ds} behaviour is due to the resonance of the C_{ds} capacitance of the switches and magnetizing inductance of the transformer. Then the converter could not reach its nominal operation due to this false triggering (see Fig. 2.4). It was encountered as an obstacle to achieve the nominal operation of the converter.

The CM current of the corresponding gate driver at two levels of transferred power was measured. The experimental results in figures 2.5 and 2.6 show the measured input CM current of the gate driver for different levels of power in phase B of the secondary VSC. The measurement points are shown in figure 2.3. It is noteworthy that the operation of the converter at 0kW means there is no power transfer from primary VSC to the secondary VSC. There is no active power in the inverter but there is a small magnetizing current in the transformer.

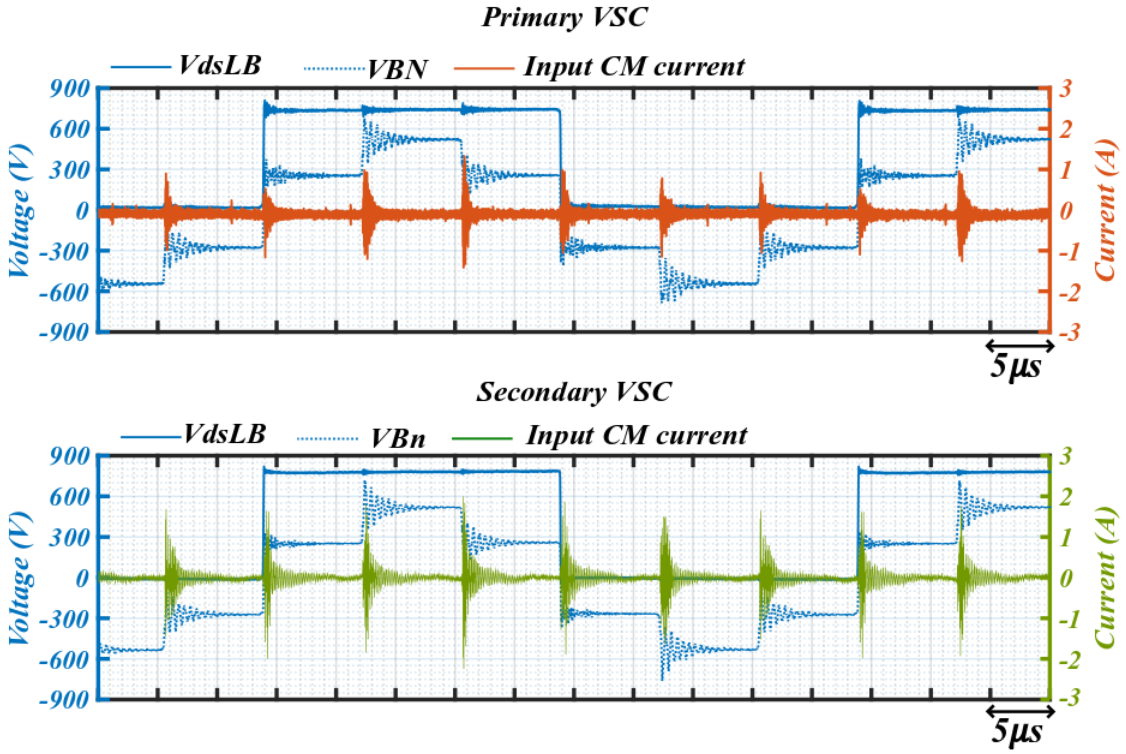


Figure 2.5 – Experimental results, input CM current, phase B of DAB3, 800V, 0kW.

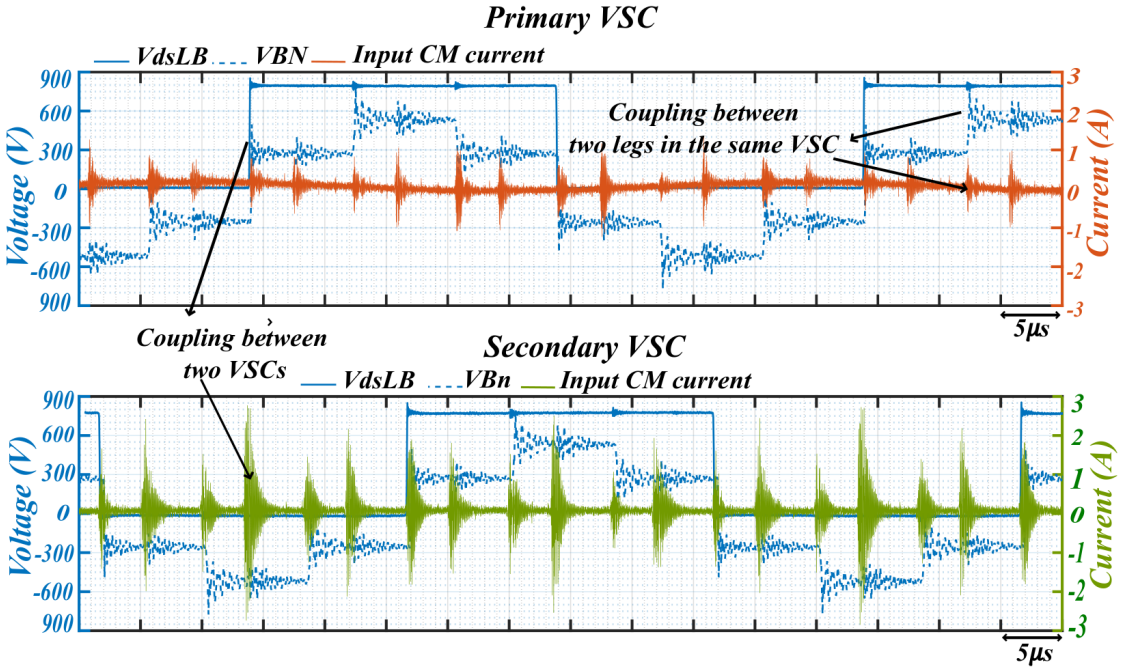


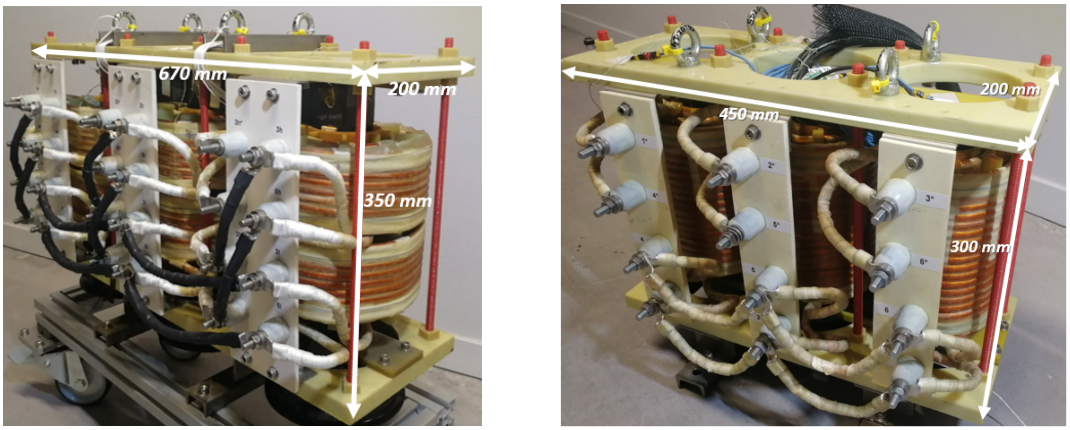
Figure 2.6 – Experimental results, input CM current, phase B of DAB3, 800V, 100kW.

These captured currents highlight two issues. The big magnitude of the CM current in secondary VSC compared to primary VSC might explain the origin of the false triggering in secondary VSC. Secondly each leg of VSCs switches at 20kHz means each switch creates a CM current every 25μs. Then the experimental results shown in figures 2.5 and 2.6 revealed that the CM current passing through a gate driver is not dominated only by the voltage variations across the corresponding switch but also by the voltage variation in other legs of the same VSC. The generated CM current pulse is repeated between the turn-on and turn-off transition of the corresponding switch. This shows the circulation of the CM current in the layout of the converter and CM leakage from one VSC to the other one (see Fig. 2.6). This shows the complexity of the CM current analysis in a completed converter.

2.5 CM current investigation in DAB

In a previous EMI study carried out in a DAB converter, a single phase DAB with SiC MOSFET 1.7 kV switches (see figure 1 in annex of chapter 2) was analysed. The converter was constructed based on two VSCs with very similar parasitic elements and ground connections. Therefore, one inverter was simulated in Ansys simplorer (see figure 2 in annex). The simulation investigation was carried out to find the parasitic elements in converter layout which has the larger impact on the CM current passing through gate driver. Based on this study, it was concluded that the parasitic capacitances of the transformer to the ground C_{ng}, can redirect the input CM current to the ground and consequently reduces the input CM current of gate drivers. Therefore, as a system level solution it was proposed to connect the screen of transformer to the ground (a copper foil inserted between primary and secondary winding and then directly to the ground). With the help of this connection, the impedance between the windings and ground at high frequencies has been reduced and CM currents flowed through this path rather than through the capacitances in the isolation stage of gate driver. Consequently it decreases the CM current of the gate driver (see figures 3 and 4).

In the application under test in this chapter, the effect of the parasitic elements of transformer prototype has been studied experimentally by means of two different transformers prototype (see Fig.2.7). The T1 is able to provide a coupling in Δ Δ and Yy configuration enabling to test the control for two types of vector groups while T2 is always in Yy configuration. This different types of winding changes the geometry of the transformer (see Fig.2.7).



(a) (b)

Figure 2.7 – Transformer prototypes, (a) T1 (b) T2.

The MFT model parameters are shown in figure 2.8. In the structure of the transformer, there are three types of parasitic capacitances: The parasitic capacitance between winding layers (C_p and C_s in Fig. 2.8), the inter-winding capacitance between primary winding and secondary winding ($C_{interwinding}$ in Fig. 2.8) and the parasitic capacitance between star point to the ground in Yy configuration (C_{ng} in Fig. 2.8).

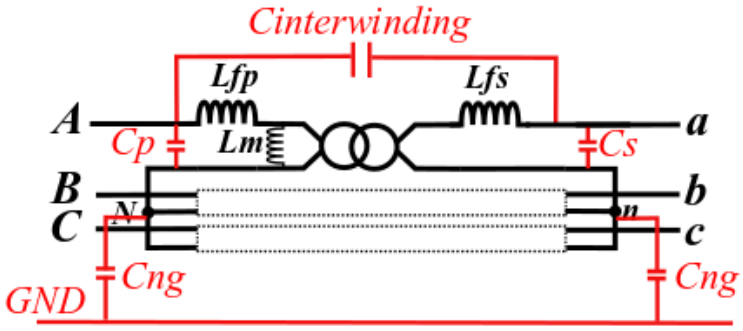


Figure 2.8 – Model parameters of transformers in Yy configuration.

In order to show the effect of these capacitances, the input CM current of gate drivers has been compared between T1 and T2. The different geometry of these two transformers leads to different values of parasitic capacitances. The experimental comparison is shown in figure 2.9.

The experimental results shown in figure 2.9 reveals a significant CM reduction with T2. The frequency domain comparison of the input CM current of gate drivers is shown in 2.10. The significant amount of the CM current reduction is observed around 10 MHz which correspond to the rise/fall time of the V_{ds} of each switch ($\frac{dV_{ds}}{dt} = \frac{11\ kV}{\mu s}$).

The stray capacitances were measured with an impedance meter in this frequency range. The measured values are shown in table 2.1. Looking at table 2.1, it

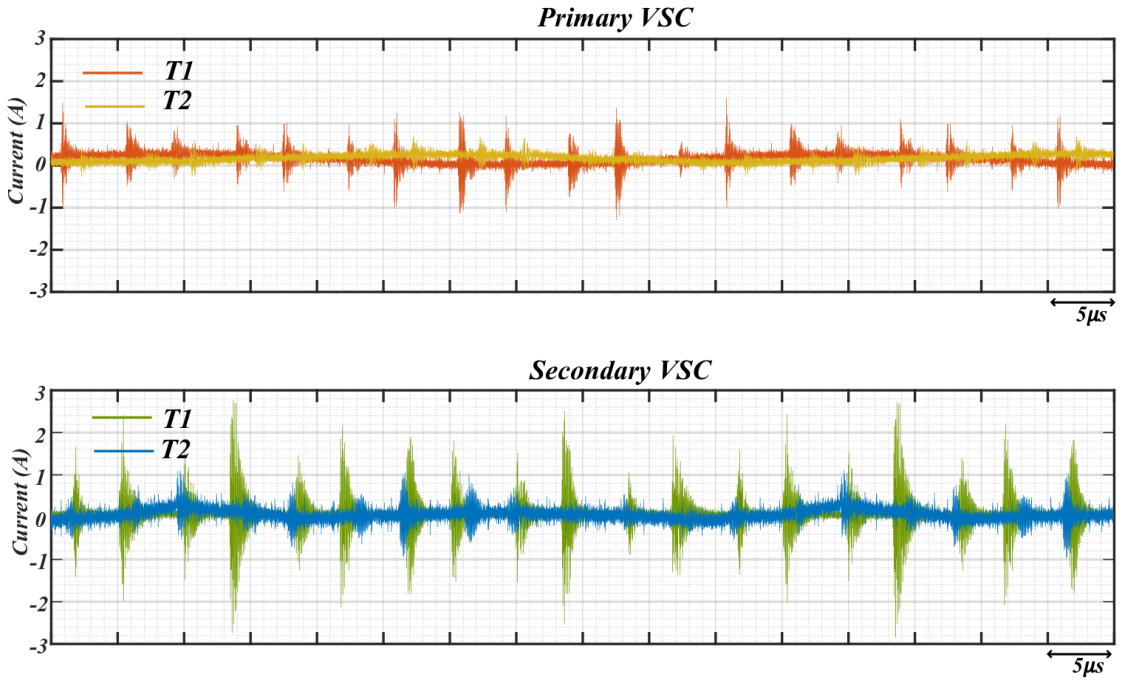


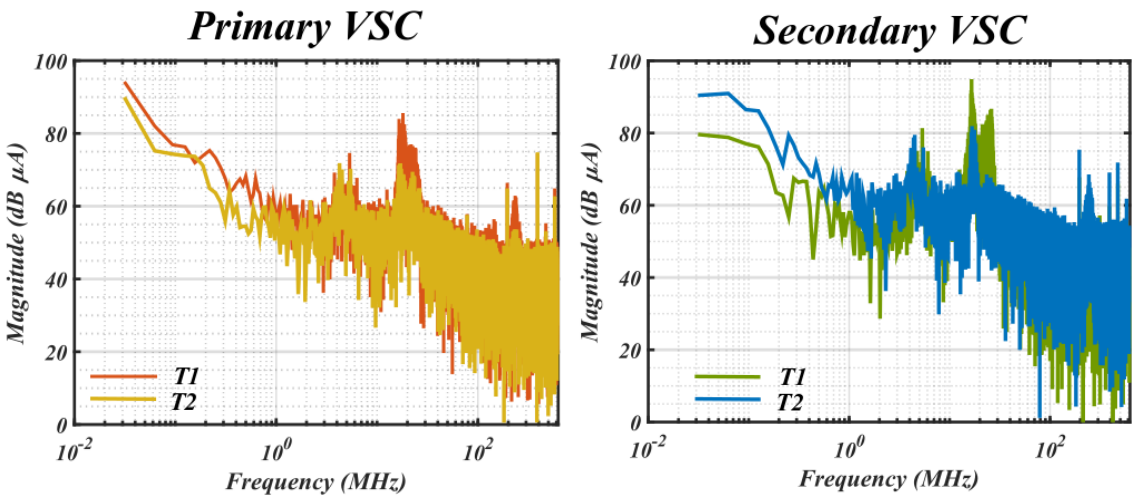
Figure 2.9 – Experimental results comparison, time domain, input CM current, phase B of DAB3 with two transformers, 800V, 100kW.

can be seen that the bigger parasitic capacitances between the winding and also between the star point to the ground provide a smaller impedance path which can shunt the CM current to the ground.

Table 2.1 – Parameters of the transformers based on impedance measurement in Yy configuration [41]

Parameter	**Unit**	**T1**	**T2**
L_{fp}	μH	17	8
L_{fs}	μH	17	8
L_m	mH	1	1
C_p	pF	30	65
C_S	pF	30	60
$C_{interwinding}$	pF	80	85
C_{ng}	pF	30	50

Transformer T2 provides a low impedance path for CM current and hence reduces the leakage of the CM current from primary VSC to the secondary. It is noteworthy that the CM current occurs in different time shifts when the transformers is changed. This comes from two different leakage inductances. This changes the phase shift as well (see Table. 4.1). Looking into the frequency domain demon-



(a) (b)

Figure 2.10 – Experimental results comparison, frequency domain, input CM current, phase B of DAB3 with two transformers, 800V, 100kW.

stration of the CM current presented in figure 2.10, it can be seen that T2 can significantly reduce the CM current passing through gate driver.

Based on the above problem statement and CM current investigation, "EMI performance" of the converter is assessed regarding the magnitude of the input CM current in the gate drivers. The objective is to reduce the EMI of the gate drivers while the isolation stage of the converter is provided by the transformer T1. In other words, in this work solving the self-disturbance problems is addressed by the reduction of the magnitude of the CM current through the gate drivers.

2.6 Proposed solution to reduce the EMI through the gate driver

As it has been explained, in the architecture of the dual active bridge converter, the parasitic capacitances of the transformer provide a CM current path between VSCs and between VSCs and ground. The effect of these elements in CM current of gate drivers has been tested thanks to two different designs of transformer. It has been shown how parasitic capacitances to the ground could shunt the CM current generated by voltage variations in each VSC.

In order to correct the false triggering and enable converter to continue its operation with T1, the CM current through gate drivers should be reduced. Therefore, the CM current from VSCs to ground and from primary VSC to the secondary should be reduced. This objective can be achieved if the CM current can find a path of lower impedance than that of the isolation stage of the gate driver.

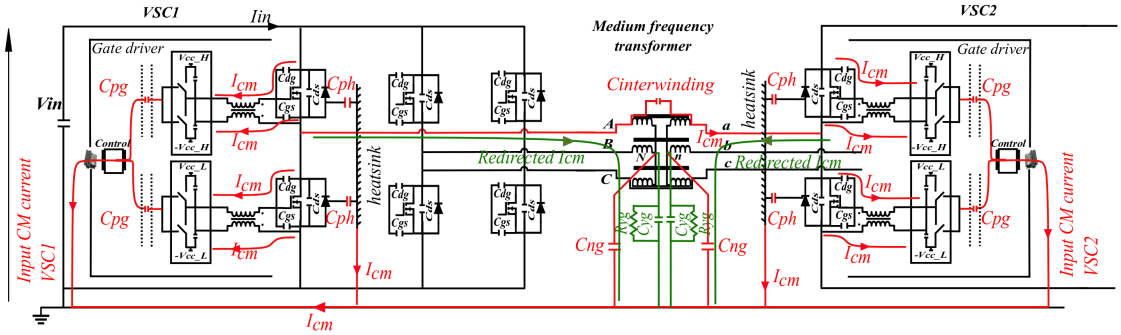


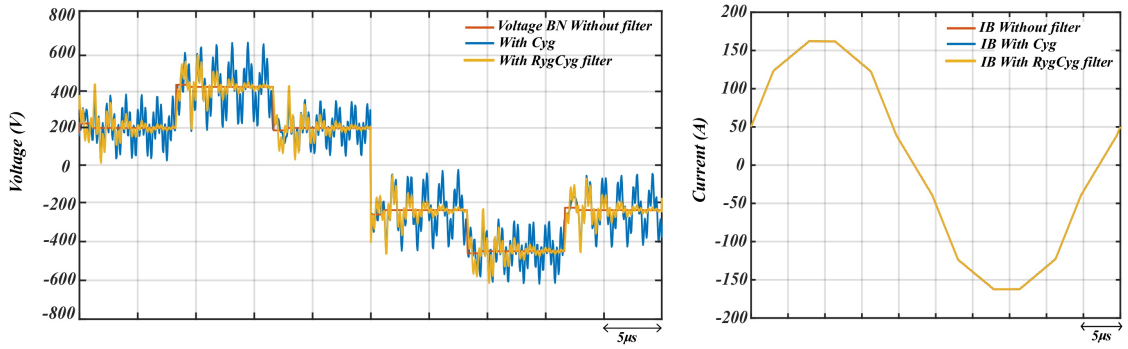
Figure 2.11 – Proposed ground layout modification for DAB3 (added components in green).

With the objective of minimizing the loops of the CM, it is proposed to modify the electrical ground connection of the converter. The proposed corrective solution, is to connect the star-points (N in VSC1 and n in VSC2 in figure 2.3) of the MFT to the ground through a capacitor C_{yg} (see figure 2.11). The main idea is to introduce another path for the CM current so that it does not pass through the gate drivers.

As it has been depicted in Table 2.1, the parasitic capacitance between the winding and ground C_{ng} is about 30 pF which is in the same order of magnitude as C_{pg} (20 pF) of the gate driver. The proposed additional star-point capacitor C_{yg} should have a capacitance value high enough compared to the one in the galvanic isolation of the gate drivers. So as, it can provide a path of lower impedance for the CM current. Lower impedance in the ground connection makes the path preferable for the CM current to the ground and redirects the noise that was flowing through the transformer. The star-point connection prevents propagation of the CM current to the secondary VSC (see Fig. 2.11, dashed line in green). The C_{yg} value of 100 pF was chosen. The DAB3 was simulated in Matlab Simulink considering the model of the transformer (see Table 2.1) and including C_{yg}. The simulations have been carried out to evaluate the proposed solution in terms of voltage and current across the transformer. The simulation results are presented in figure 2.12.

The B phase voltage and current correspond to three cases: without C_{yg}, with C_{yg} and with C_{yg} and R_{yg}. It can be observed a significant voltage oscillation when the C_{yg} is added. However, adding the resistor R_{yg} damped the oscillation. The phase current is not influenced by C_{yg} or R_{yg}.

The proposed solution was applied to the prototype in order to verify its effectiveness and to measure the performance of the converter in a continuous test mode. Figure 2.13 illustrates the effect of the proposed connection in CM current of the gate drivers in VSC2. As it can be seen, the added capacitance shunts the CM current to the ground. Moreover, the magnitude of the transferred CM current from primary VSC to the secondary has been reduced (The CM current due to



(a) (b)

Figure 2.12 – Simulation results, DAB3, 800 V, 100 kW with proposed ground layout modification (a) phase B, voltage across transformer (b) Phase B, current.

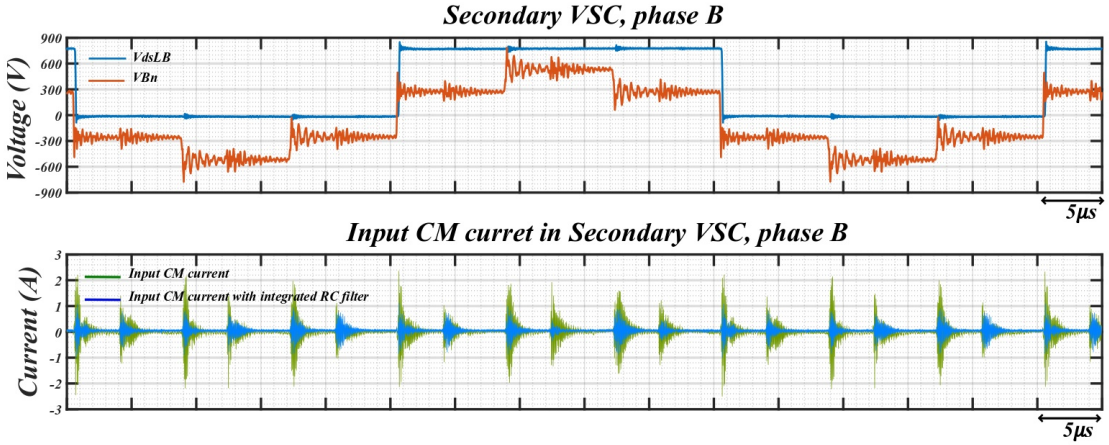


Figure 2.13 – Experimental results, time domain, DAB 3, 800 V, 100 kW, input CM current reduction in VSC2 and voltage in VSC1 and VSC2.

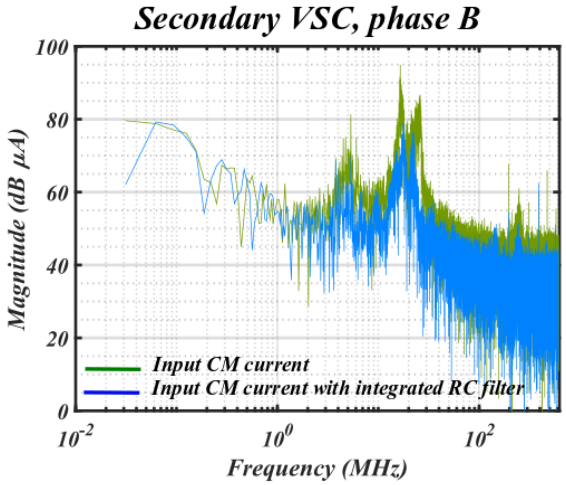
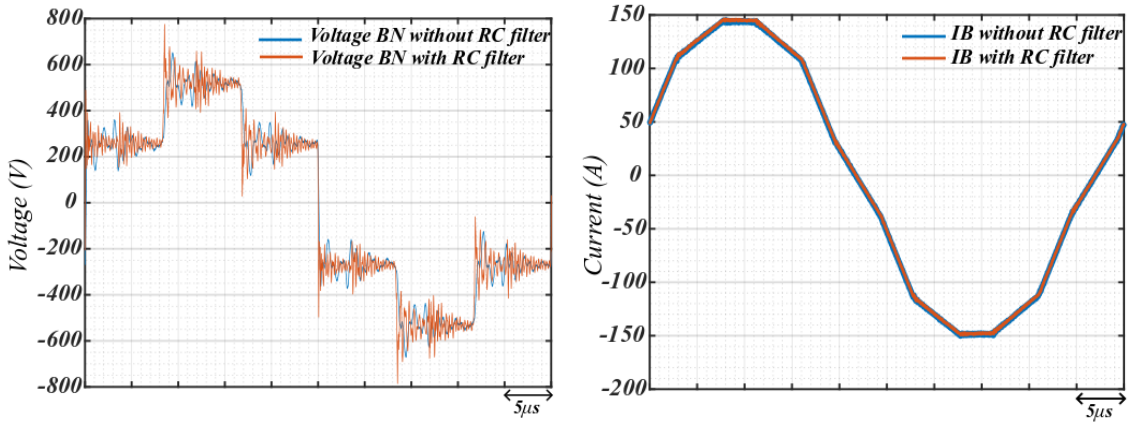


Figure 2.14 – Experimental results, frequency domain, DAB3, 800 V, 100 kW, input CM current reduction in VSC2 without RC filter and with RC filter.



(a) (b)

Figure 2.15 – Experimental results, DAB3, 800 V, 100 kW with proposed ground layout modification (a) phase B, voltage across transformer (b) Phase B, current.

coupling between two VSCs is shown in figure 2.6). The peak of the CM current in secondary VSC is significantly reduced (by up to 75%) which allows converter operation above 800V. This confirms that self-disturbance was due to the level of CM current through the gate drivers. The frequency domain analysis is shown in figure 2.14. It can be seen that the added filter reduced the CM current in the same frequency range where T2 in figure 2.10 reduced the CM current.

The current and voltage in phase B have been measured and have been compared with the corresponding waveforms without added filter in order to show that they have not been significantly changed due to the proposed solution. Figure 2.15 illustrates that the added capacitance has not changed the normal behavior of the converter. Moreover, thanks to the proposed solution it is possible to increase the voltage of the converter and reach the nominal operation (see Fig. 2.16).

2.7 Conclusion

This part of the work intends to look at the physical connection of the converter. Moreover, the effect of the physical connection in CM current of the gate driver has been discussed. The experimental study in this chapter addressed the electromagnetic compatibility issue of the 100 kW, 1200 V, SiC MOSFET based prototype. The big amount of the input CM current through gate drivers disturbed the control circuit of the converter. Indeed, the isolated supply of the gate drivers provides a propagation path for this current. Therefore, the amplitude of the CM current of the gate driver has been considered here as the main indicator of EMI behaviour of the converter. A corrective solution for a completed prototype has been proposed.

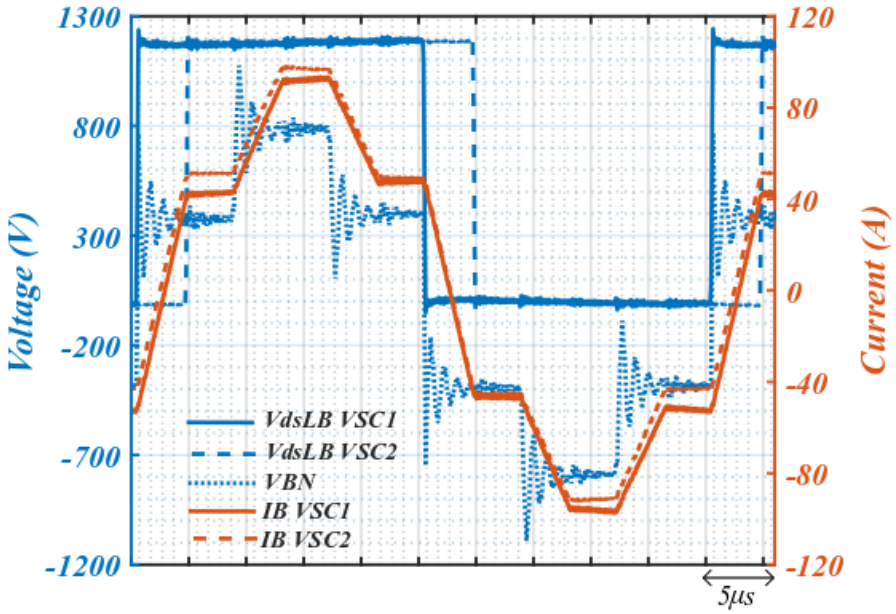


Figure 2.16 – Experimental results, nominal operation of DAB3 with ground layout modification, 1200V, 100kW and T1 in Yy configuration.

The solution is to connect the star-point of the transformer to the ground through a RC filter. This system-level strategy for ground connection of insulated converters allows to divert the CM current circulation from sensitive part of the system and reduce the magnitude of the CM current without decreasing switching speed. EMI behavior of the insulated DAB should be considered at early design stage of the converter. So as, this work can help converter designers for further prototyping and installation.

2.8 Perspectives

The potential limitation of this study is the added resistance to the passive filter. In this specific design, implementing only the capacitance without the damping resistor adds voltage oscillations across the transformer terminals. The damping resistor reduces the voltage oscillations but it adds some power losses. Therefore, for further MFT designs the CM impedances should be considered as a fully-fledged design specification. At present, MFT design procedures rarely include this criteria in the optimization process. Also when the sizing constraints allows to have a screen between primary and secondary windings, connecting the screen to the ground can minimize the CM current loop and provide a low impedance path for CM current.

As it has been explained, the converter benefits from soft-switching method. Soft switching involves zero voltage switching (ZVS) and zero current switching (ZCS)

depending on the direction of the current. This method can reduce the CM current passing through the gate drivers. Moreover, this study has showed the effect of the input CM current of the gate driver in the operation of the converter. For further works, there is a need to focus on the gate driver and consider it as a CM mode current path. If the generated CM current due to the switching transition is reduced, then the CM current passing through the gate driver and consequently in the converter layout would be reduced too. In the following chapter, the gate driver for a soft-switching converter based on SiC MOSFET will be studied.

3

Double pulse test-bench and EMI modelling

It has been explained in chapters 1 & 2 that the gate driver is not only a potential victim of the electromagnetic interferences but also an element which can change the magnitude of the EMI. Therefore, it is targeted to achieve an optimised driving technique. To evaluate different design techniques and switching transition modifications it is focused on a fundamental switching element of the converter which is the half-bridge device and corresponding half-bridge gate driver.

In order to optimise the design of the gate driver, in each step, the gate driver should be practically evaluated. The performance of the gate driver and the switching characteristics of the device provide the information to tune the design stage. However, prior to the experimental part, the behaviour of the converters, gate drivers and the devices under test can be optimised during the design stage. In this step, the simulation tools can help to estimate the behaviour of the electronic devices.

Here in this chapter, it is tried to model the circuit under the test including the gate driver, the device under test and the layout of the converter at the first step of the study. The goal of modelling in this work is to estimate the level of

the interferences and find a model which shows a behaviour similar to that of the converter. This model should enable us to test the different gate driver designs.

Based on above-mentioned objectives, this chapter is organised as follows. First, the double pulse test-bench is introduced. Then the switching transition steps are detailed and the switching characteristics time intervals of a half-bridge device are presented. The state of the art of the modelling techniques to determine the electromagnetic interferences are reviewed in the third part of this chapter. The elements of the converter have been measured and simulated in "LTspice" simulation tool, they are demonstrated in section four. The simulated converter is compared with experimental data in fifth section. The chapter ends with a conclusion.

3.1 Introduction of double pulse test-bench

The inductive clamp circuit, double pulse test, is used to achieve switching transition analysis (see Figure 3.1). In general, the double pulse test is used to characterise one switch and regarding the free-wheeling current, either the external diode is used to carry the current during turn-off transition of the switch or the body diode of the complementary switch.

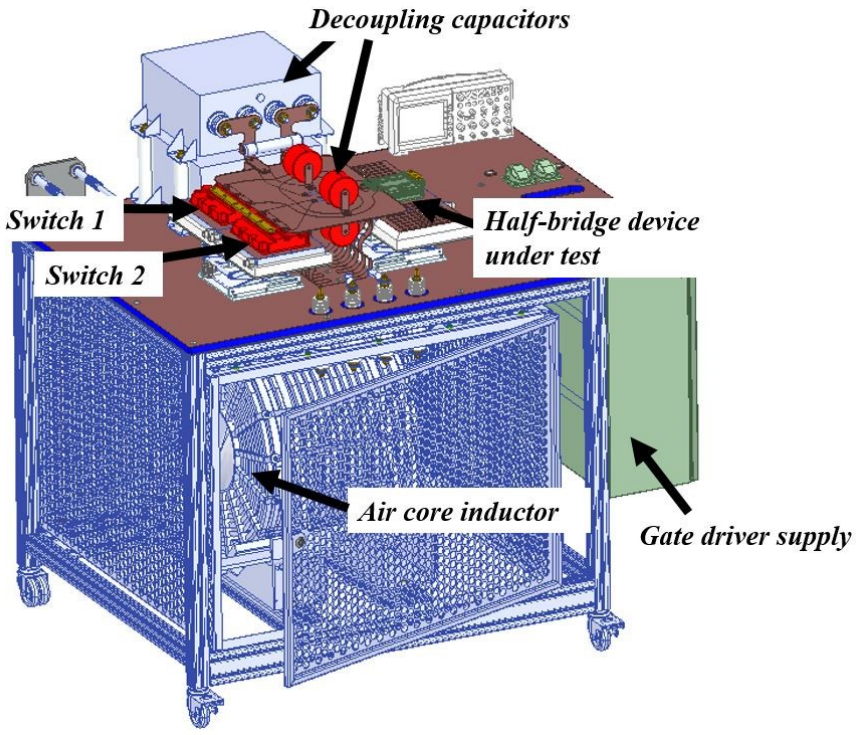


Figure 3.1 – Full-bridge double pulse test bench configuration

In this work, the target is to analyse the fundamental switching cell of the converter which is the half-bridge device. According to the converter topology and operating point, both soft-switching and hard switching transition can occur. The soft switching condition can be achieved with different methods. A half-bridge device is used as a switching cell. This means that, during a given time (dead-time), the diode in the power module is used as the free-wheeling (FWD) element. For this purpose, the circuit should be able to control the current in the load with both directions as it has been shown in figure 3.2 to characterise both high-side and low-side switches. Therefore, the typical clamp inductive circuit is changed to a full bridge converter where switches 1 and 2 are used to manage the current direction. By turning on the switch 1 (marked as red dashed-line), the high-side switch is free-wheeling the current which is called in this dissertation positive current. In the opposite direction (marked as green-dashed line), it is called negative current direction. During switching transition of the half-bridge device, there two switches (switches 1 & 2) are not involved in losses calculation and EMI consideration.

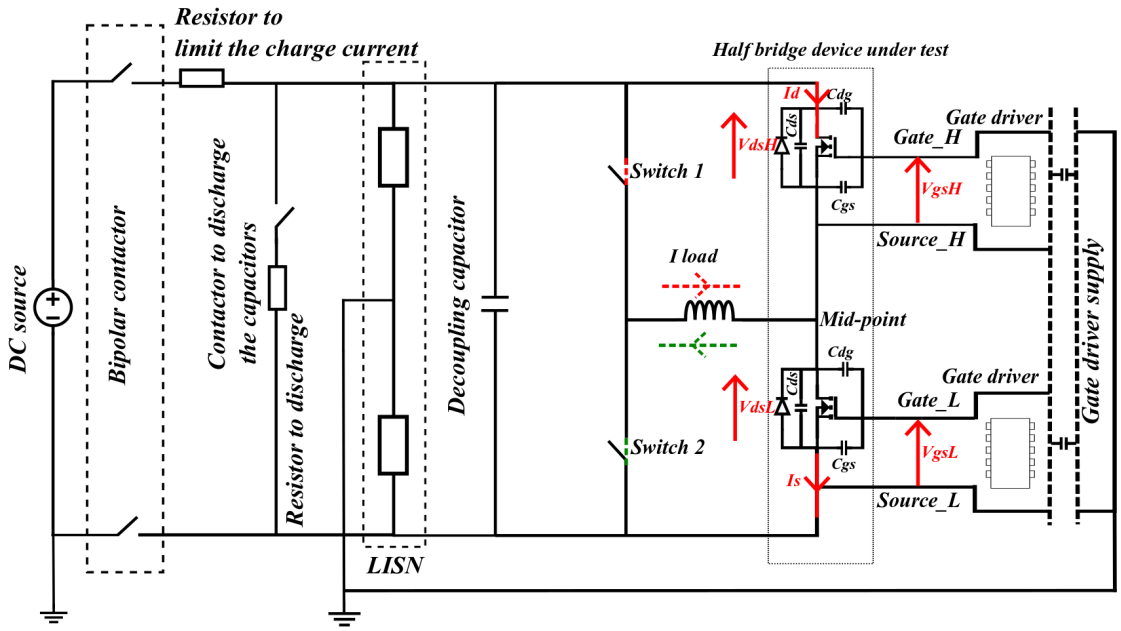


Figure 3.2 – Full-bridge double pulse test circuit

The platform is used to study the generated EMI of the half-bridge device passing through the power supply of the corresponding gate driver and the converter. In order to provide a precise impedance to the power input of the half-bridge device and also to provide repeatable measurements of the generated noise, there is a need of a Line Impedance Stabilization Network (LISN) device. In order to achieve this goal and to keep the measurement completely floating from the network ground, a bipolar contactor is used in the circuit (see Fig. 3.2). During the switching charac-

terisation of the half-bridge, the contactors are managed to be open therefore, the floating measurement can be achieved. The other elements that are used during high voltage test is shown in figure 3.2.

3.2 Half-bridge switching steps

Basically eight switching conditions occur in half-bridge switching characteristics (see figures 3.4). These steps have been shown in the case of positive current in figure 3.4. It will be the same for negative current direction also but with inverse switching characteristics between high-side and low-side.

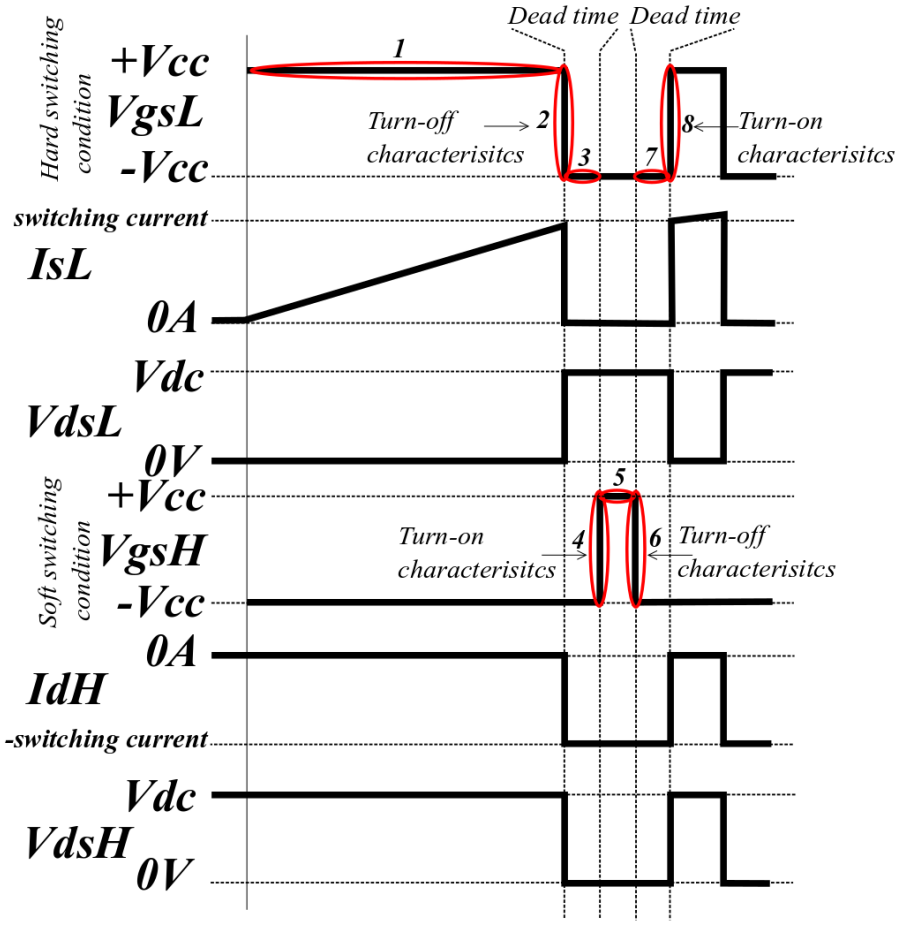


Figure 3.3 – Double pulse inductive voltage and current waveform.

When the load current is in positive current direction, the reverse recovery effect can be monitored at the high-side switch and for the negative current direction it is in low-side switch. For these two transitions, it is managed with a dead time. The dead time (**steps 3 & 7** in figure 3.3) in this application is chosen relatively high such that no cross current can occur in any case.

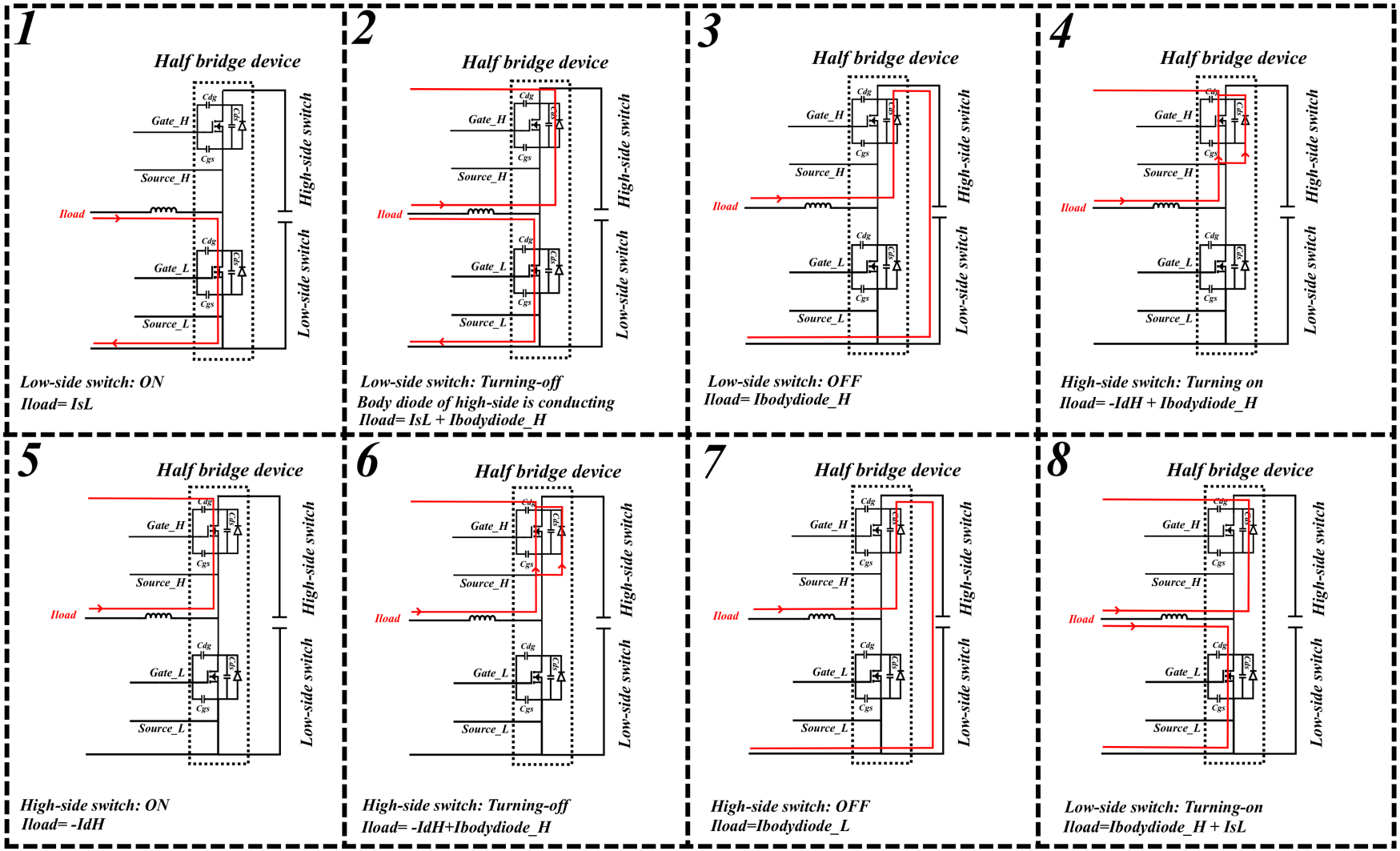


Figure 3.4 – Different steps in inductive double pulse test circuit.

Step 1 shows on-state of low-side switch to establish the desired current value (switching current) in the inductive load (inductance in the test bench).

Step 2, the turn-off of the first switch (low-side) creates current in the FWD, here is the Schottky diode of the upper-switch. Due to the high load inductance and short turn-off period, the load current is almost constant.

The second turn-on pulses in the low-side switch (**step 8)** results in reverse recovery of the FWD hence the current overshoot in the SiC MOSFET device switching. To avoid device degradation, normally the device under test is tested with a switching current lower than its nominal value. Vds overshoot at turn-off of the high-side switch should be kept below the SiC MOSFET rated values. Therefore, for example the rated voltage and current values of the device under test in this work are 1700 V and 350 A, the maximum switching characterisation test voltage is done up to 1.2 kV and switching current up to 200 A.

During switching transition, as it has been explained, the parasitic elements charged and discharges which creates the switching ringing which are the source of electromagnetic interferences. In order to test the efficiency of the gate driver design in reducing the generated EMI and evaluate the switching characteristics of the device with different gate driver designs, the EMI model of the circuit is needed. Therefore, the EMI modelling of the circuit is presented in the following sections.

3.3 State of the art of EMI modeling in power electronics

The objective of EMI modelling of any electronic system is to have a model which can simulate similar behaviour to that of the real application. In this way, most of the EMI phenomena can be anticipated in advance. In general, EMI modelling can be categorised in two groups, exhaustive modelling (direct modelling) [117] and behavioural modelling (indirect modelling) [99]. Often exhaustive modelling uses time domain simulation while indirect method is based on frequency domain simulation. The detail of both approaches will be explained then based on the requirement of the EMI study in the current work (see section 3.3.3), the selected modelling technique will be explained.

3.3.1 Exhaustive approach

The exhaustive modelling gives a physical representation of each element of the system under test. This is a classic way to model any type of circuit. This modelling approach, incorporates both discrete and integrated passive components, active components (such as switching devices) the interconnections and the control circuit as well.

In this approach, each device is modelled separately and then integrated into the final simulation. The time domain simulation can be followed by a frequency domain analysis. Then it can be compared with the frequency analysis of the real application.

The time domain simulation allows to take into account the non-linearities of circuit components. Regarding the active devices in this approach, a complete model should represent its behaviour during switching transition and its static characteristics [13, 68]. An exhaustive modelling example is presented in [13] in the case of a boost converter (see Fig. 3.5). It gave a precise model of the converter. However, the system under test is not complicated in terms of number of switches and converter layout. Therefore, for converters with a single switching cell, this type of modelling is suitable to predict the EMI. However, knowing the internal structure of the converter and proper model of the switching elements is necessary to have a proper model.

In terms of difficulties for this type of modelling, it can be said that, there are a lot of commercial components in which the detailed model is confidential. Another point is that in exhaustive modelling (detailed modelling), there are several variables changing during simulation time which makes the simulation time considerably long [70]. On the other hand, in order to have a model fitting to the real application, there is a need of small time step for simulation in order to get precise results. This leads to convergence problems in simulation [136]. These constraints in simulation are the difficulties in front of having an accurate model. Examples of software which provide this simulation methods are: LTSpice, SABER, Ansys simplorer.

3.3.2 Behavioural modelling

Behavioural modelling or system modelling means developing an overall EMC model of the converter. The simulation tools are often working in frequency domain [49]. The aim of this approach is to represent the behaviour of the system (or components) without knowing the internal structure. Behavioural EMI mod-

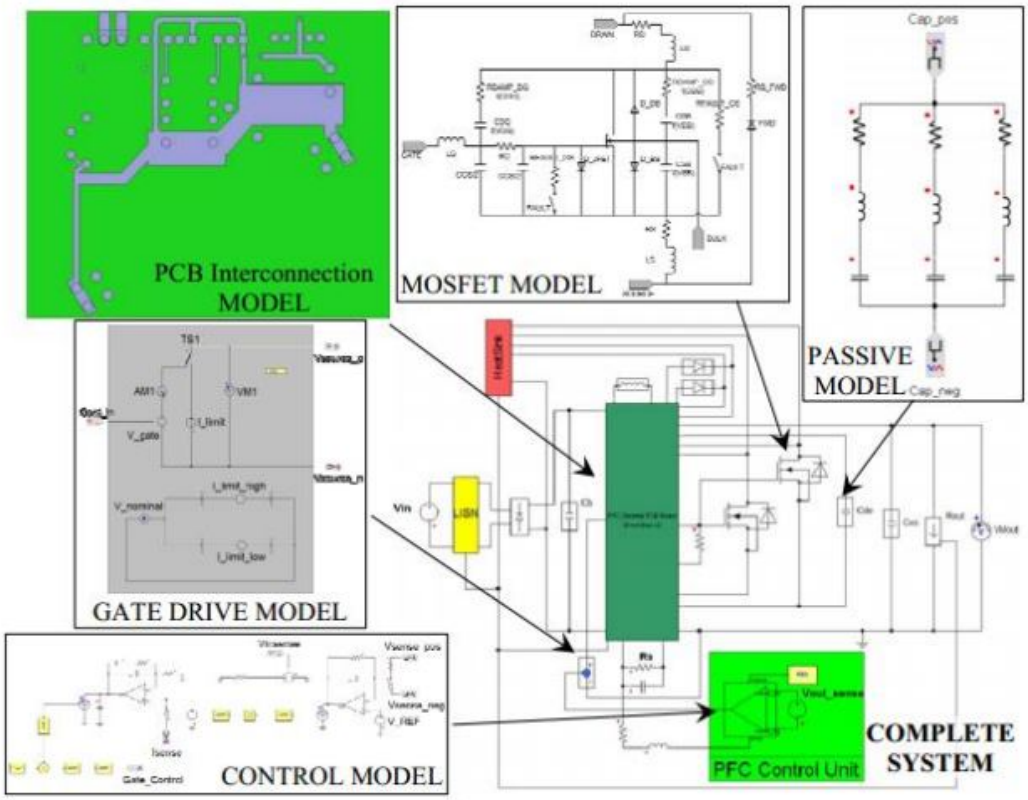


Figure 3.5 – Example of exhaustive EMI modelling [13].

elling often are created to be used in the frequency domain. Compared to previous exhaustive approach, it benefits from faster calculation.

The behavioural approach builds-up the system with simplified model in which all the characteristics of the converter elements are considered. For this approach, there is no need of internal knowledge of the converter and particularly parasitic elements. This type of modelling is often based upon measurements. Since its interest is the general behaviour of the system, the elements of the model are limited. Normally this approach is used to estimate the EMC signature of converter prototype. It can be used to size an EMI filter in shorter time compared to exhaustive modelling approach [26].

There are several frequency domain simulation models created for EMI modelling of inverter, which approximate non-linear source characteristics by linear modellings. On the other hand, there are physics-based equivalent circuit models [77]. These models are often used to simulate either CM [71] or DM noises [48]. They are valid if one of both can be identified as dominating emissions. Under these circumstances, the switches are replaced by a single CM or DM noise source.

On the other hand, there are modular-terminal-behavioural (MTB) models like [49]. These “black-box” models can produce very accurate simulation results with

little information about the internal structure of the modelled device. The MTB black box model allows the converter to be represented by an equivalent diagram generating the same parasitic signals as those measured. The semiconductors are replaced by equivalent sources and equivalent impedances [50].

Figure 3.6 – Behavioural EMI modelling with 5 parameters (black box).

An example of MTB black box modelling approach is represented in figure 3.6. The model is based on the quadrupole principle with two current sources and three impedances (see Fig. 3.6). The identification of the model parameters is made through input measurements of the device to be modelled. These measurement are carried out under different operating conditions. Voltages and currents (V1, V2, I1 and I2) are measured for the different operating points. Then a system of equations is proposed and the solved equations give the impedance values of Z1, Z2 and Z3 and equivalent sources as Is1 and Is2.

Although black box models are simpler to simulate compared to exhaustive models, they are less suitable to get a good understanding of the propagation paths ones. Moreover, for this measurement based modelling method, the quality of signal acquisition is of great importance [136]. The identification of parameters depends on these signals. In case of time domain measured signals, those must have enough points in one period of study so as not to loose information [136]. A FFT can be performed after the acquisition to obtain the parameters of the model in the frequency domain. Another disadvantage of this method is that errors can appear in the measurement because of the sensitivity of the measurement devices. So this type of modelling is not suited for the trial and error optimisation of the electronic device which is the case in this work.

3.3.3 Chosen EMI modelling for this work

The reported modelling methods works remain limited for applications with complex geometries circuits and some do not perform well over the entire range of frequencies. The complex circuits are also generally not very easy to express analytically.

The black box model shows good results but once one of the parameters of the circuit changes, the measurements and the identification of model parameters need to be re-examined. This modelling technique is not convenient for filter optimization or when we seek to reduce disturbances by optimizing cabling or electrical connection modification. Moreover, as it has been mentioned, it does not clarify the propagation paths for an EMI issue in converter.

The exhaustive analysis considers both sources of EMI and propagation paths. However, the exhaustive direct modelling requires precise models of the semiconductors as well as parasitic elements of the converter schematics. These elements can be estimated as long as the analysis is done for simple converters. When the system gets complicated in terms of number of active components and geometry, the accuracy of the model is reduced. Therefore, it can show trends of the system under test but not accurate information.

The choice of the method depends on the objective of the study. The objective in this work is to study the switching trajectory of semiconductors thanks to gate driver modification. Moreover, the effect of the propagation path (electrical connection) should be considered which makes the exhaustive temporal simulation a more appropriate method to be continued.

However, the platform under test in this work is complex and identifying all the parasitic elements is not an easy task. The main objective of the modelling in this work is to reproduce the same behaviour as that of the real application. It is expected that the modelled circuit shows a similar tendency to measurement results of the circuit. To examine the effect of the gate driver design and switching trajectory, LTspice simulation tool is chosen.

With this type of simulation, we can study the effect on EMI behaviour of each components of the gate driver circuit and SiC MOSFET switches, couplings, routing, etc of the converter can be studied.

3.4 Double pulse test elements and modelling

3.4.1 Passive components

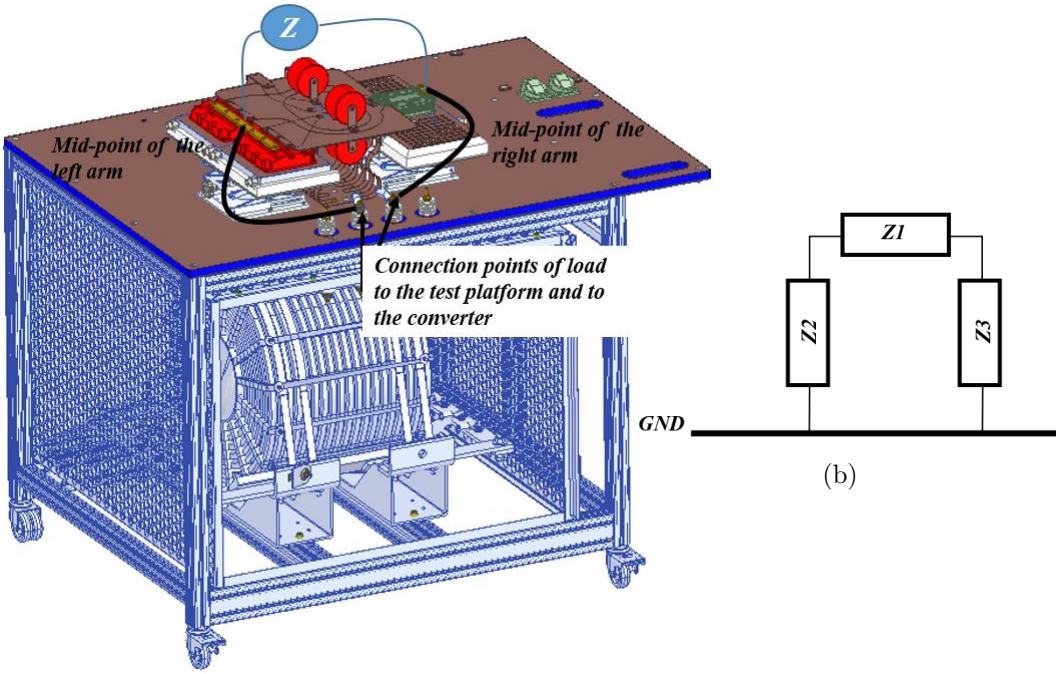
The passive elements of the double pulse test should be modelled as well as the active elements. To obtain the equivalent circuit of the passive components (decoupling capacitors, load) , these elements were measured by an impedance meter apparatus and the measurements have been reproduced in AC simulation with “LTspice” for

comparison purpose. For Busbar, the simulation has been done in "Q3D Ansys tool" and then compared with measurement.

3.4.1.1 Inductor modelling

The load consists of an air inductor. Basically the inductor (L) value should be large enough to maintain the switching current during a switching period. In a half-bridge test platform, some stray elements of the load (inductor) will influence the switching and the EMI performance which should be considered for modelling.

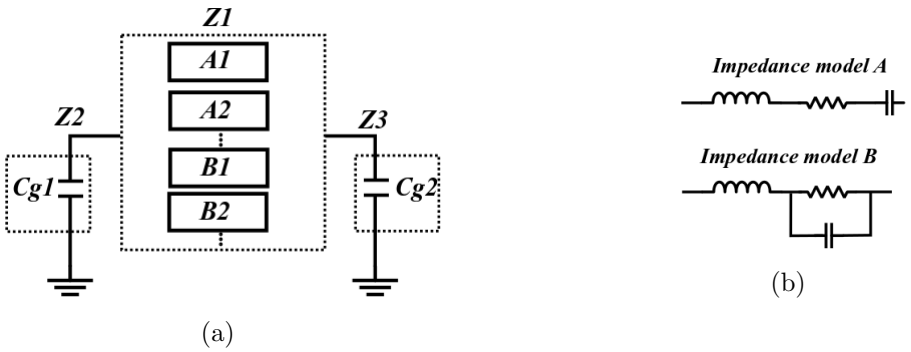
The measurement points to model the load inductor are shown in figure 3.7.a. The measured impedance of the load includes several resonances. The measured impedance between the terminals of the load consists of the RL load (Z1 in figure 3.7.b and the parasitic capacitances of the load to the ground (Z2 and Z3 in figure 3.7.b). It is necessary to consider the parasitic capacitances which leads to the CM EMI propagation paths. The inter-winding capacitance of the load, which is often modelled as in parallel with RL, will influence the switching characteristics (C_L in figure 1.20 in chapter 1) because this capacitance is in parallel with the output capacitance of the device under test. Therefore, the value of this capacitance should be considered in EMI modelling of the switching cell.



(a) (b)

Figure 3.7 – Load impedance measurement (a) Impedance measurement (b) Equivalent circuit of load impedance.

To model the air inductor and the parasitic capacitances to the ground, the method reported in [136] is applied in this work. The parasitic capacitance to the ground and the load impedance are calculated based on impedance measurement separately. To model the air inductor, the vector fitting (VF) procedure reported in [39, 64, 65] allow us to calculate the self-inductance and self-capacitance of the load. It provides two structures for RL and the parasitic capacitances. The equivalent model of the load is a combination of two impedance structures which are shown as A and B in figure 3.8.



(a) (b)

Figure 3.8 – Load model (a) load impedance structure (b) equivalent impedance model generated by curve-fitting.

The equivalent impedance model consists of several paralleled models of A and B where the numbers of impedances in parallel corresponds to the numbers of poles in the curve-fitting used to generate equivalent impedance of the inductor. The values of Z1, Z2 and Z3 are shown in the tables 3.1, 3.2 and 3.3. The negative value correspond to non-physical components which are generated by curve-fitting only to complete the models and fit the several resonances. The frequency analysis of the proposed model and the measured impedance are compared in figure 3.9. The equivalent model can fit the measurement up to a 30 MHz frequency range.

Table 3.1 – Parameter values of the modelled inductor.

Z_A	**Value**
Z_{A1}	$R_1 = 28m\Omega$, $L_1 = 1.5mH$
Z_{A2}	$R_2 = 2414\Omega$, $L_2 = 27\mu H$
Z_{A3}	$R_3 = 163\Omega$, $L_3 = 733\mu H$, $C_3 = 97pF$
Z_{A4}	$R_4 = 75\Omega$, $L_4 = 8.62\mu H$, $C_4 = 211pF$
Z_{A5}	$R_5 = 8.04\Omega$, $L_5 = 8.515\mu H$, $C_5 = 100pF$
Z_{A6}	$R_6 = 12\Omega$, $L_6 = 2.33\mu H$, $C_6 = 208pF$
Z_{A7}	$R_7 = -1.3992\Omega$, $L_7 = -1.52\mu H$, $C_7 = -242pF$

Table 3.2 – Values of the modelled inductor for configuration B.

Z_B	**Value**
Z_{B1}	$L_1 = 1.2\mu H$, $R_1 = 78943\Omega$, $C_1 = 56pF$
Z_{B2}	$L_2 = 45\mu H$, $R_2 = 2892\Omega$, $C_2 = 39pF$
Z_{B3}	$L_3 = -9.13\mu H$, $R_3 = -11284\Omega$, $C_3 = -93pF$
Z_{B4}	$L_4 = -2.8235\mu H$, $R_4 = -1110\Omega$, $C_4 = -172pF$
Z_{B5}	$L_5 = 1.49\mu H$, $R_5 = 4409.1816\Omega$, $C_5 = 247pF$

Table 3.3 – Values of the modelled parasitic capacitances to the ground.

C_g
$C_g1 = 170pF$
$C_g2 = 110pF$

3.4.1.2 Decoupling capacitance modelling

In fast switching, the decoupling capacitances decrease the equivalent impedance of the converter layout and this allows to reduce the circulation of the transient current in the converter layout due to switching of semiconductors (it reduces the differential mode disturbances). Moreover, decoupling capacitors stabilize the DC voltage at the input of the converter. In this double pulse test, two groups of capacitances have been installed (see Fig. 3.10).

Two units of 2.5 kV capacitors around 2.5 mF are used to stabilize the DC voltage of the double pulse test bench. These capacitors are used to supply the current to the inductor during the test. They are called C_{dc}. For impedance measurement they have been considered as one unit. To model these capacitances also the curve fitting method results in a impedance structure shown in figure 3.11.

The DC capacitances consist of two parallel units shown in figure 3.11 and thanks to an optimisation method, the extracted values for the proposed model are shown in table 3.4.

Table 3.4 – Values of the model of the DC decoupling capacitances.

Z_C	**Value**
Z_{C1}	$L1 = 66nH$, $R1 = 1.6m\Omega$, $C1 = 3.3mF$, $R2 = -15\Omega$
Z_{C2}	$L1 = 322nH$, $R1 = -11\Omega$, $C1 = 127pF$, $R2 = 171\Omega$

The frequency analysis of the measured impedance and the modelled impedance in LTspice simulation tool based on table 3.4 are compared in figure 3.12. The

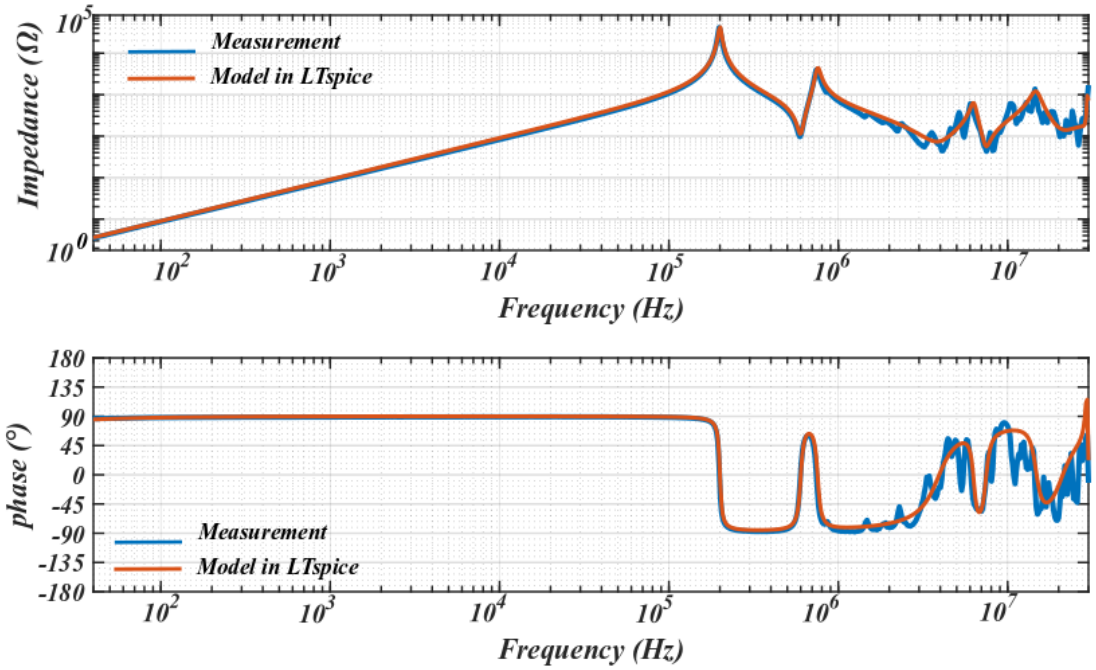


Figure 3.9 – Inductor modelling and comparison with impedance measurement between the terminals of the load.

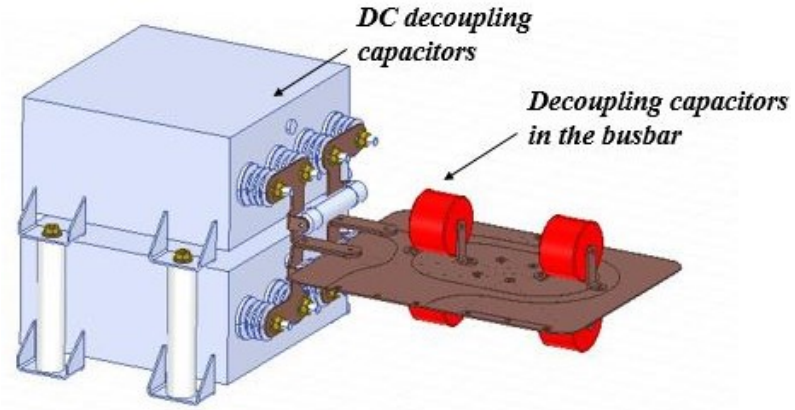
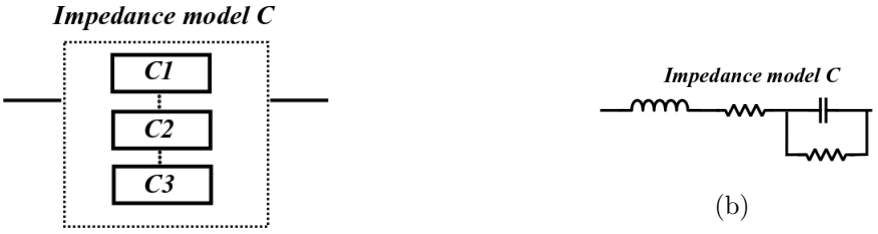


Figure 3.10 – Decoupling capacitors implemented into the busbar of the double pulse test.



(a) (b)

Figure 3.11 – Decoupling capacitors model (a) Capacitor impedance structure (b) equivalent series resistance and inductance model.

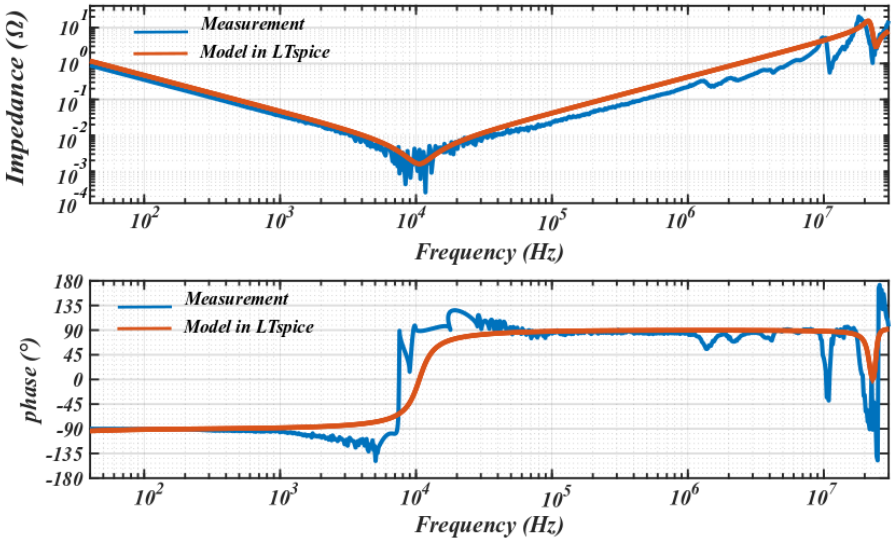


Figure 3.12 – Modelled decoupling capacitor, comparison of impedance measurement and LTspice AC simulation.

proposed model fits reasonably the measurement. However, since the equivalent series inductance (ESL) is too high, for the main power loop, secondary capacitors are used in addition. It consists of 4 units of film capacitors. The four capacitances of 2.5 kV capacitors of 2 μF embedded on the busbar of the converter. The extracted values for each test bench decoupling capacitors based on the proposed impedance model in figure 3.11 are listed in table 3.5.

Table 3.5 – Test bench decoupling capacitance value in double pulse set-up.

Z_C	**Value**
Z_{C1}	$L1 = 15nH$, $R1 = 34m\Omega$, $C1 = 2.06\mu F$, $R2 = 3.1345\Omega$
Z_{C2}	$L1 = 267nH$, $R1 = 1.72\Omega$, $C1 = 6.48nF$, $R2 = -26\Omega$
Z_{C3}	$L1 = 76nH$, $R1 = -7.23\Omega$, $C1 = 639pF$, $R2 = 13\Omega$
Z_{C4}	$L1 = 20nH$, $R1 = 9.37\Omega$, $C1 = 327pF$, $R2 = -11\Omega$

The measured capacitor with the impedance meter and the simulated equivalent circuit in LTspice are compared in figure 3.13. It can be seen that the proposed method fits almost all the resonances of the measured capacitance up to 30 MHz.

3.4.1.3 Busbar modelling

To connect the components of the converter (clamp inductive circuit), a laminated busbar is used to minimize the parasitic impedance of the switching loop and power loop. To model the laminated busbar, it has been tried to proceed impedance measurement for each part of the circuit. However, due to strong coupling between

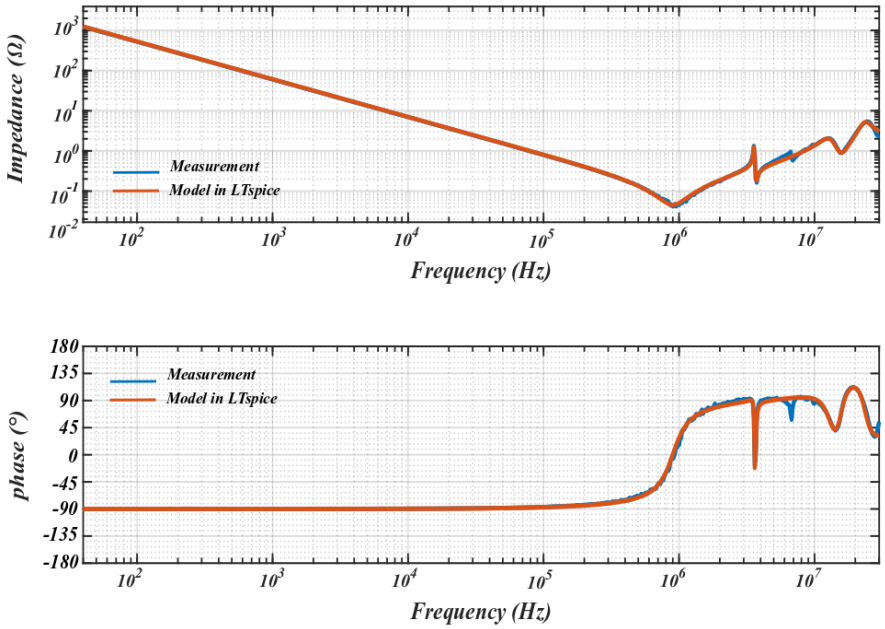


Figure 3.13 – Modelled decoupling capacitor in the busbar, comparison of impedance measurement and LTspice AC simulation of calculated equivalant model up to 30 MHz.

the positive and negative layer, the capacitive behaviour overcomes the impedance measurement and the measured impedance was not a real representative of busbar impedance (especially for inductive parts). Therefore, the measurement has been carried out between the terminals of the device under test while the other terminals are short-circuited. This allows to measure the overall impedance seen by the semiconductors like the stray impedances called as L_{stray} in figure 1.20.

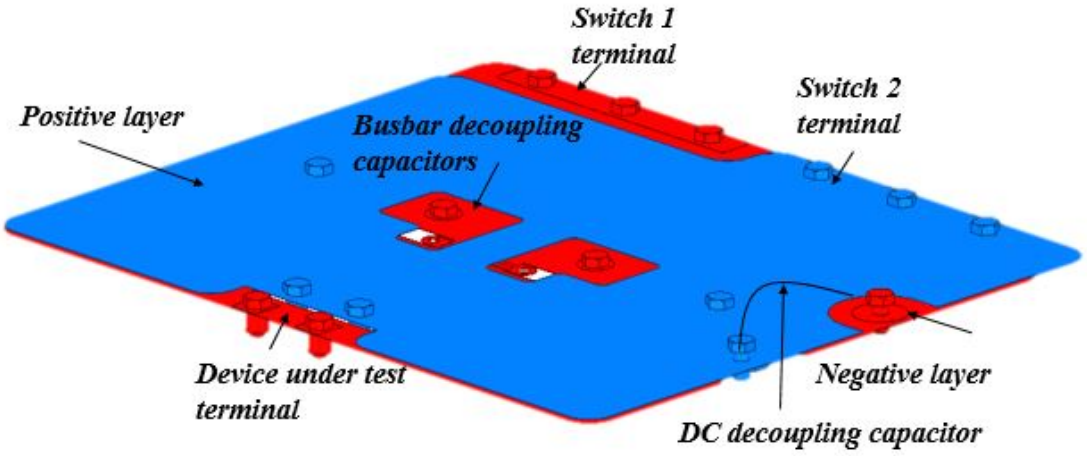


Figure 3.14 – Busbar Q3D modelling.

The Q3D simulation has been carried out for impedance calculation of the busbar to be compared with measurement. The reduced model of Q3D model has been exported to “team builder” to reproduce the impedance behaviour for AC simula-

tion. The comparison is shown in figure 3.15. An equivalent impedance based on figure 3.15 including 67 nH self inductor and 12 mΩ resistance is considered for the converter layout based on the measurement for power loop. The impedance matrix value has been imported to LTspice for converter layout.

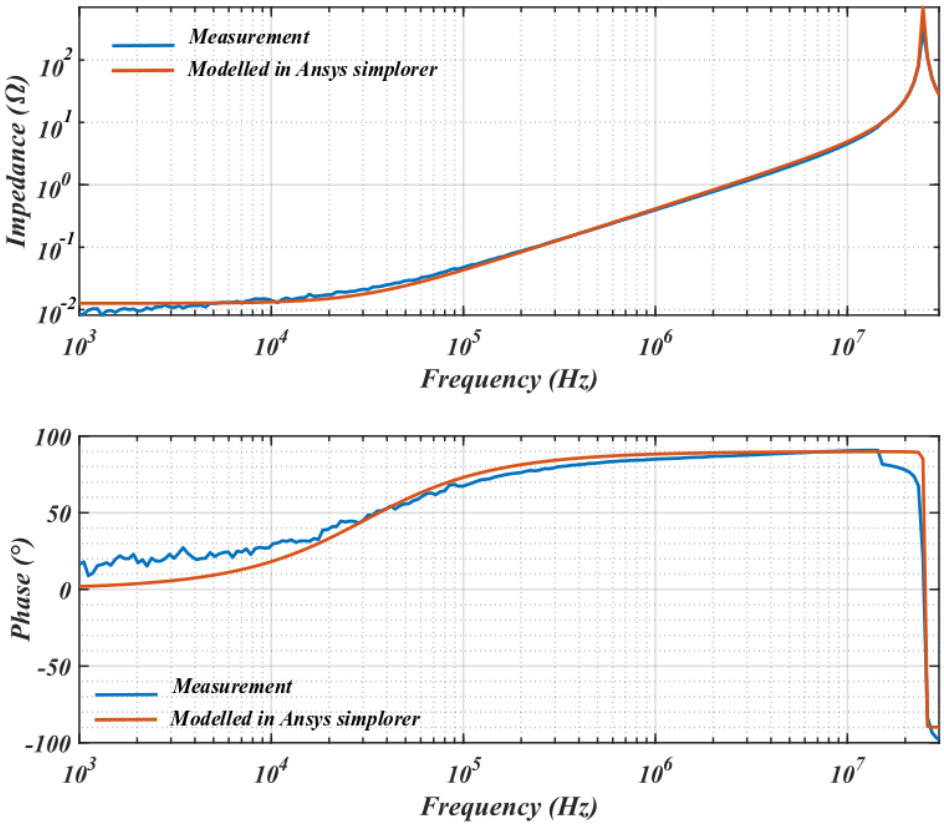
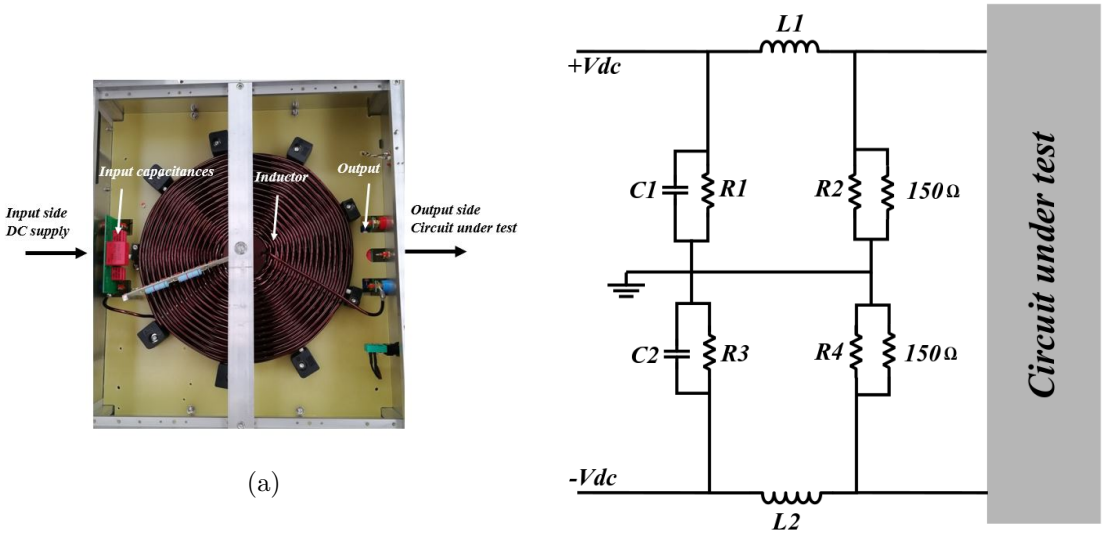


Figure 3.15 – Comparison of Modelled busbar and impedance measurement between the terminals of the device under test.

3.4.2 LISN modelling

Although this work is not following any EMI standard, however, in order to ensure the re-productivity of the measurements for comparative studies, a Line Impedance Stabilizing Network (LISN) is used in the double pulse test-bench. The place where the LISN is connected to the circuit under the test is shown in the figure 3.2. It acts as a low pass filter placed between the DC source network and the circuit under test. The LISN isolates the circuit under test from the power supply and measurement from high frequency disturbances. The LISN used in this work is a 150 Ω PVDC 8300 device, with a frequency range from 150 kHz to 30 MHz and able to handle the 100 A current and a line to ground voltage up to 1500 V. The ground of LISN is used to fix the ground reference of the measurement (see Fig. 3.1).

To complete the simulation model, the model of LISN (from Fig. 3.16.b) was used in the simulation tool. A model from the data sheet of the device has been used since the measurement of each components separately was not possible due to the internal structure of the device (see Fig. 3.16).



(a)

(b)

Figure 3.16 – Line Impedance Stabilization Network (a) Internal structure (b) Equivalent circuit.

In this model, L_1 and L_2 are equals to 135 μH. $R1$ and $R3$ provide 1.5 $Meg\Omega$ resistance in parallel with the input capacitances C_1 and C_2 which are equal to 44 nF. Finally R_2 and R_4 provide 1 kΩ in parallel with 150 Ω resistance of the LISN.

3.4.3 Active components modelling

The active components in the double pulse circuit consist of the device under test and some transistors that exist in the circuit of the gate driver.

For transistors in the gate drive, models provided by the manufactures and are imported to the simulation tool.

The device under test in this work is a 1.7 kV SiC MOSFET from CREE company [168]. This is a commercial device and the company has not provided the model of the power module yet. Based on reported information in [88], the power module consists of 5 dies (1.7 kV with 45 $m\Omega$ internal resistance in parallel with 5 Schottky diodes. The model of the device under test was also constructed in LT-spice tool and was tuned based on the provided information from the manufacturer in the 1.7 kV SiC MOSFET data-sheet. Moreover, the body diode of the device

is considered as well. Therefore, the model of the device was built on the basis of a sub-circuit in LTspice to be implemented in the double pulse test circuit. The basic model of the die and Schottky diode are provided in appendix of this chapter (Appendix of chapter .2).

3.5 Simulation in LTspice

As it is well-known that the voltage at the mid-point of the half-bridge is the point of origin of the CM EMI. This voltage is modified by the parasitic capacitance between this point and the ground. Then, the parasitic capacitance between the negative and positive terminals of the busbar to the table (which is considered as the ground in this platform) has been measured as well. The values of the capacitances are considered receptively 7 nF, 4 nF and 4 nF.

Finally, by implementing all of these parasitic elements and active components in LTspice simulation tool (see Fig. 3.17), it is possible to simulate the switching behaviour of the SiC MOSFET. In the following section, the simulation results will be compared with the experimental ones.

To reproduce the SiC MOSFET switching behaviour, the output stage of the gate driver has been modelled (see Fig. 3.17). The output stage includes PMOS and NMOS of the push-pull circuit and decoupling capacitors to generate the driving signal for the SiC MOSFET. In this work, the external gate resistance of the gate driver is always set to 0.2 Ω. The internal gate resistance and parasitic inductance of the SiC MOSFET has been considered based on the SiC MOSFETs data-sheet [168]. The set-up has been shown in figure 3.18. The gate-source voltages are shown in figures 3.19 and 3.20 and they are compared with experimental waveforms.

The first point in this comparison is the miller region. Based on the explanation related to switching characteristics in chapter 1, this region is controlled by the gate impedance and input capacitance charging of the SiC MOSFET (see time intervals 1 and 2 in figure 1.7 of chapter 1). The gate impedance in this simulation is considered to be equal to the value given in the data-sheet and even the external gate inductance due to the connection of the gate driver to the device has not been considered so as to not slow down the switch. The difference between the gate-source voltage is mainly due to the dynamic behaviour of the input capacitances of the device. This phenomenon can be seen in both high-side and low-side driving voltages.

In SiC MOSFET power module, the kelvin-source connection is often provided to measure the gate-source voltage in a right point and to allow a proper control of

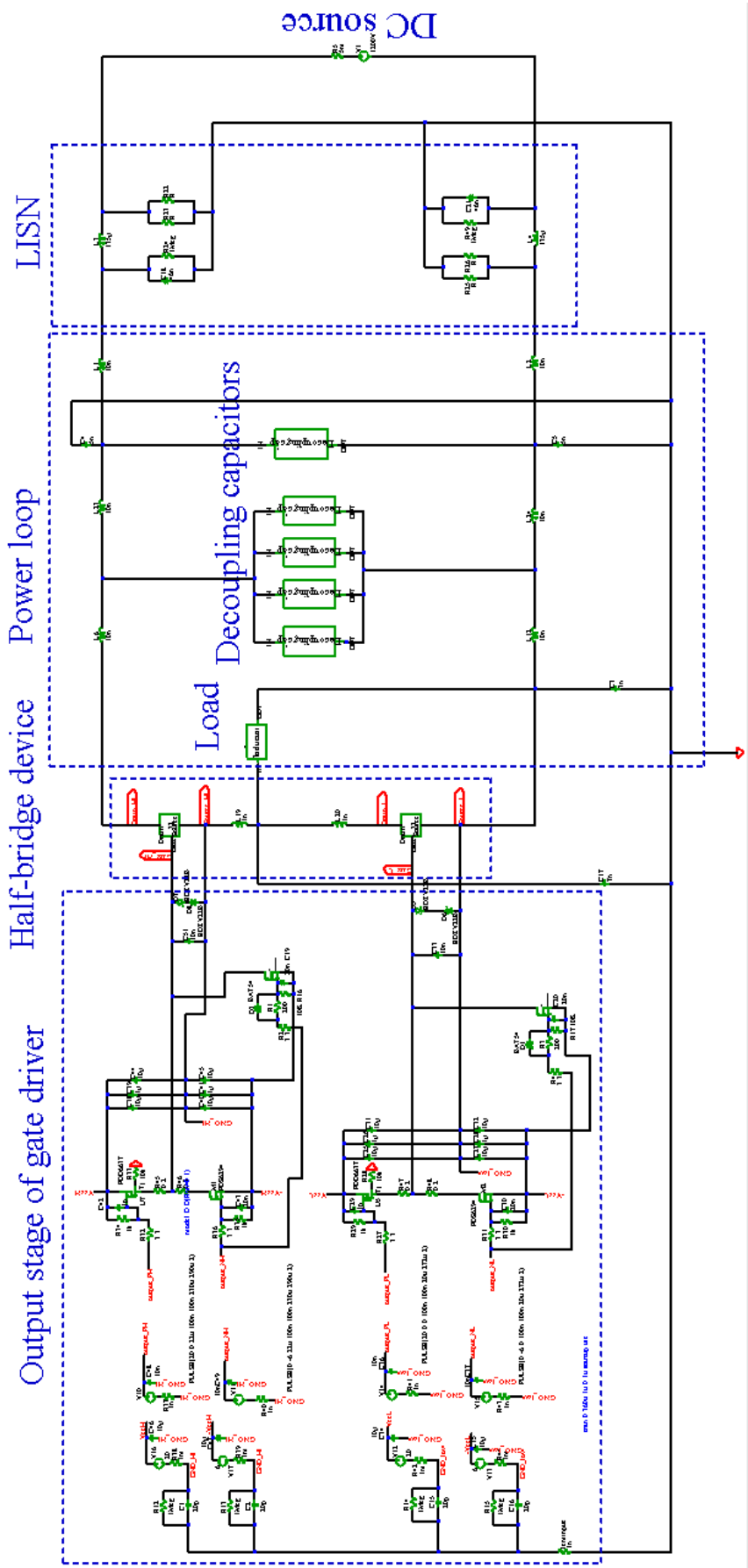


Figure 3.17 – Simulated double pulse test in LTspice.

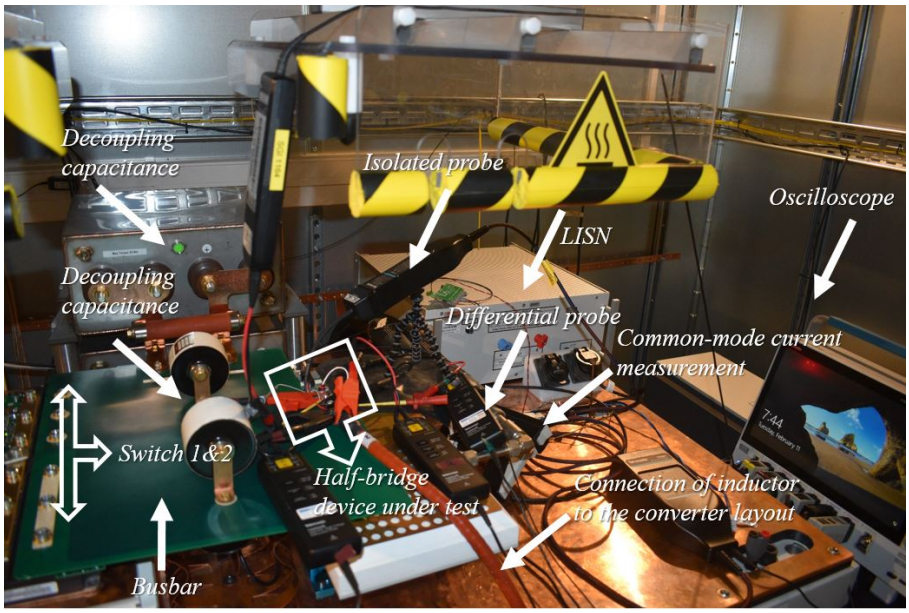
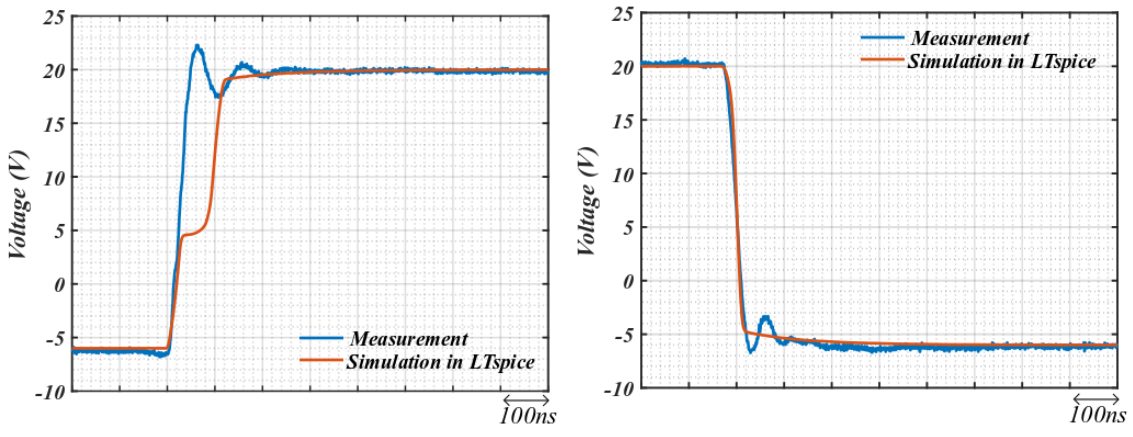
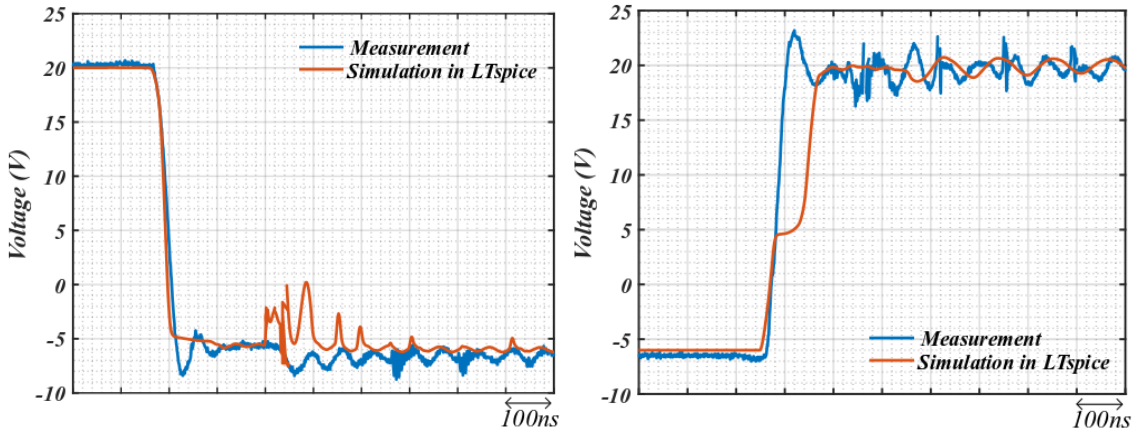


Figure 3.18 – Double pulse test bench, set-up



(a) (b)

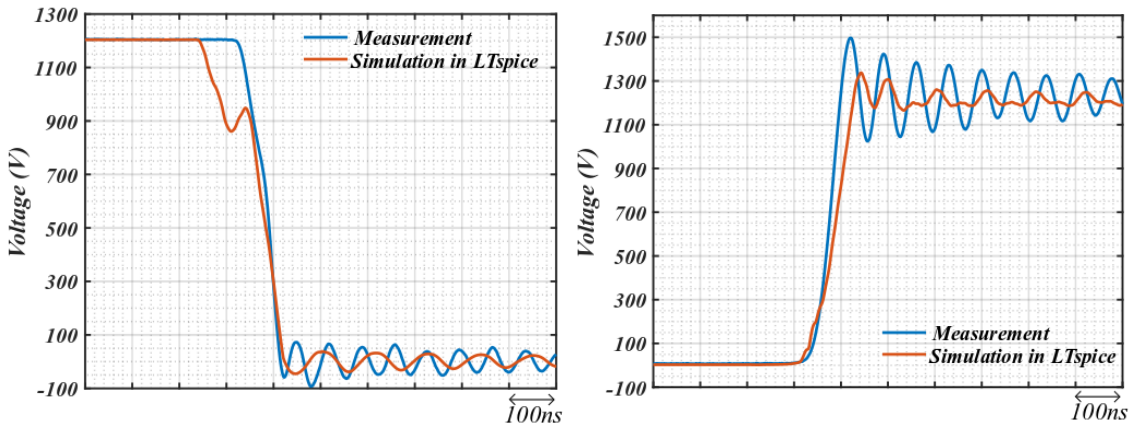
Figure 3.19 – Comparison between modelled double pulse test circuit and measurement, 1200 V, -200 A switching characteristics, uncontrolled switch (soft-switching condition) VgsL (a) Turn-on transition (b) Turn-off transition



(a) (b)

Figure 3.20 – Comparison between modelled double pulse test circuit and measurement, 1200 V, -200 A switching characteristics, controlled switch (hard-switching condition) VgsH (a) Turn-off transition (b) Turn-on transition

the switch. This connection also aims to reduce the gate loop inductance. Moreover, it helps to avoid gate drivers perturbation through the parasitic voltages generated by fast switching source current flowing inside the source inductance. Since the model of the complete package is not provided by the manufacturer, in our case this connection is missing which might change the driving waveforms.

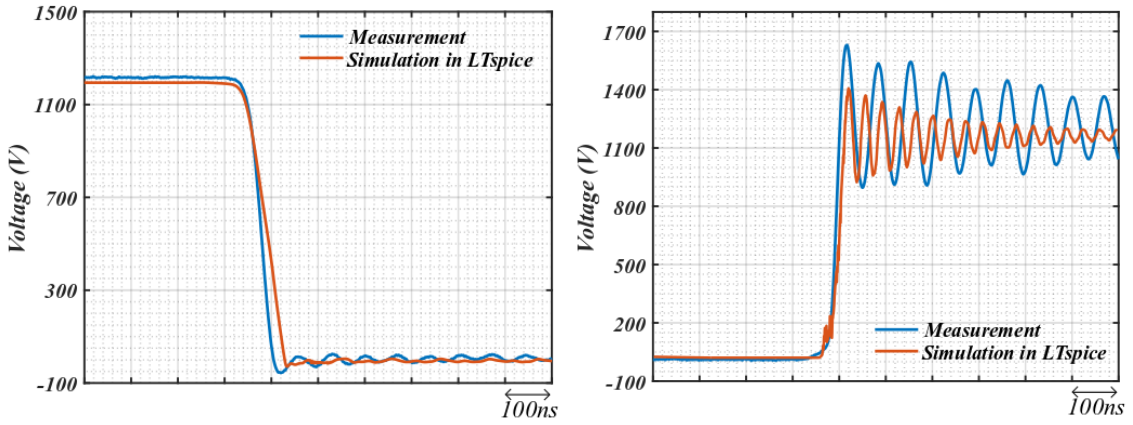


(a) (b)

Figure 3.21 – Comparison between modelled double pulse test circuit and measurement, 1200 V, -200 A switching characteristics, controlled switch (hard-switching condition), VdsH (a) Turn-on transition (b) Turn-off transition

The difference in the miller region in gate-source voltage waveforms results in a slight difference in the drain-source voltage slopes. In this double pulse test, the switching voltage and current waveforms across the uncontrolled switch (soft switching) are the projection of the current and voltage waveforms across the con-

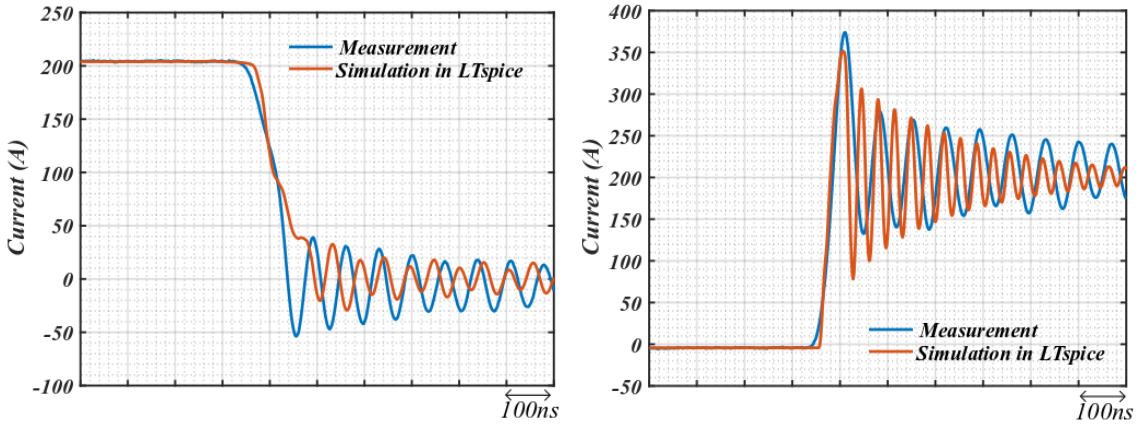
trolled switch (hard switching). Therefore, similar behaviours are shown in figures 3.21 and 3.22.



(a) (b)

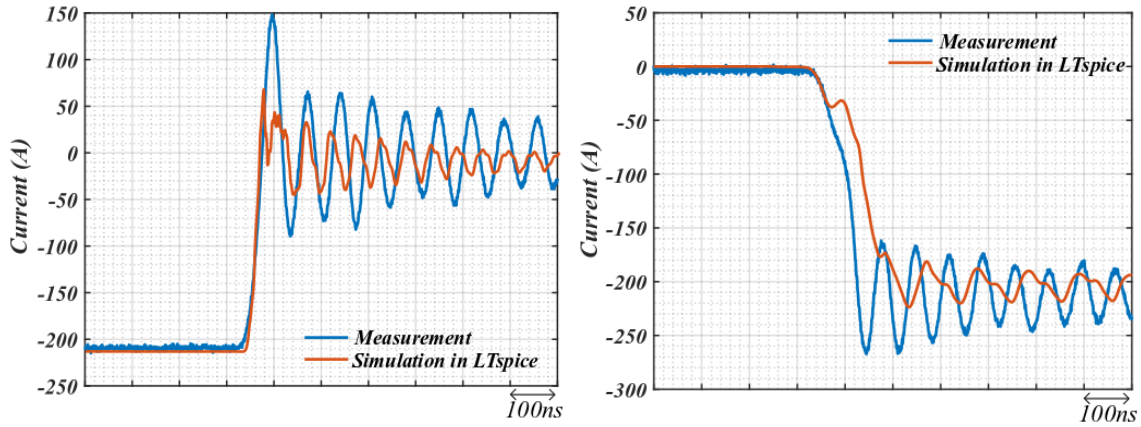
Figure 3.22 – Comparison between modelled double pulse test circuit and measurement, 1200 V, -200 A switching characteristics, uncontrolled switch (soft-switching condition) VdsL (a) Turn-on transition (b) Turn-off transition

Looking into figures 3.21 and 3.22, during turn-on transition of the high-side and turn-on transition of the low-side, a voltage drop appears. As it has been explained in chapter 1, this voltage drop is mainly due to the parasitic inductances named as Ld_L and Ls_H in figure 1.23. These parasitic inductances are due to the packaging of the device. In this work, these values were added manually based on the data-sheet of the device due to lack of information on the package model. Therefore, it can be concluded that a more accurate model of the switch and also of the converter layout can improve the simulated circuit behaviour.



(a) (b)

Figure 3.23 – Comparison between modelled double pulse test circuit and measurement, 1200 V, -200 A switching characteristics, controlled switch (hard-switching condition) IdsH (a) Turn-off transition (b) Turn-on transition



(a) (b)

Figure 3.24 – Comparison between modelled double pulse test circuit and measurement, 1200 V, -200 A switching characteristics, uncontrolled switch (soft-switching condition) IdsL (a) Turn-on transition (b) Turn-off transition

Switching current waveforms are depicted in figures 3.23 and 3.24. Besides the switching slopes difference that are already explained, the difference in the switching characteristics comes from the parasitic inductances in the package and in the layout of the converter. The problem of the power module package-model are shown in these waveforms. Since there is no kelvin-source connection, the source of the power module is connected directly to the converter layout (see Fig. 3.17).

Increasing the parasitic impedances in the simulation circuit to reproduce the switching oscillations leads to inaccurate gate-source voltage waveforms and consequently inaccurate switching characteristics. Moreover, the convergence problem occurs due to large number of active components influenced by these parasitic elements. However, as it has been explained, the main aim of the modelling in this work is to have a similar behaviour which gives trends similar to the real application. The model enabled to simulate different gate driving techniques which are evaluated in the following chapters 4 and 5.

3.6 Conclusion

The experimental test platform used in this work has been presented. To characterise the half-bridge module, a novel double pulse test-bench was used. The full-bridge converter enabled to measure the switching characteristic of the high-side and low-side switches at the same time. Moreover, it gave the soft-switching characteristics which normally are not defined in data-sheet of semiconductors. In this work, the exhaustive simulation method is chosen since the propagation paths and their effect on the switching behaviour are of interest. With the help of the

LTspice simulator it was possible to reproduce the switching behaviour of the SiC MOSFET power module. The model of the power module under test is the element which affects the compliance of the model with the experimental results. Our simulation method can give a good understanding of the propagation paths and the effect of the gate driver techniques in current and voltage waveforms across the semiconductors and finally explain the EMI behaviour of the converter.

4

Mitigation of the self-disturbance phenomena in a half-bridge power module

4.1 Introduction

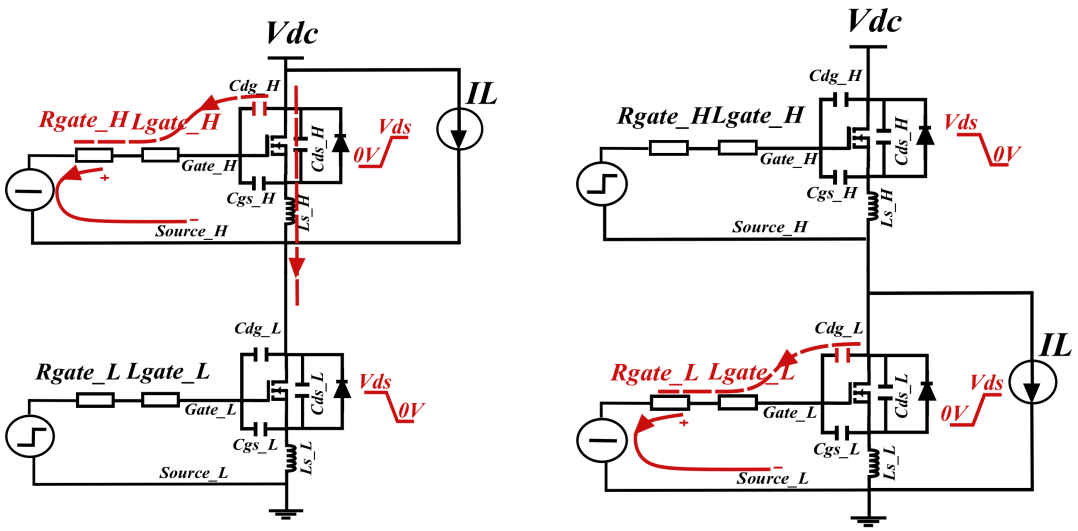
As it has been explained in the introduction, by increasing the switching speed to obtain minimum switching losses, converter parasitic elements are subject to large dv/dt and di/dt values which can generate disturbances. In a half-bridge configuration, during switching transient with high dv/dt, each switch affects the operation of the complementary switch in a phase-leg. The fast variation of the voltage across a switch in an half-bridge produces an unavoidable voltage perturbation on the complementary switch due to parasitic elements of the device. The generated CM current due to complementary switching passes through the gate driver isolation and can disturb the controller of the converter. Therefore, keeping in mind that the main objective of this work is to benefit from the maximum switching speed of the SiC MOSFET, this chapter explains how to deal with the parasitic gate voltage without increasing the losses.

This chapter is organized as follows. Section 4.2 explains the mechanism of the voltage perturbation in the gate which is called in this work "self-disturbance" phenomenon. Section 4.3 highlights the causes of the self-disturbance phenomena. The classical solution to reduce the voltage perturbation is presented in section 4.4. The importance of the measurement in this particular part of the dissertation will be discussed in section 4.5. Section 4.6 illustrates the proposed solution to reduce the perturbation and the chapter ends by section 5.4 as a conclusion. All the experimental results presented in this chapter have been carried out in the test platform presented in chapter 3.

4.2 Problem statement

4.2.1 Positive parasitic-voltage in gate

During turn-on transient of the lower switch (controlled switch, hard switching condition) the voltage across the switch is decreasing from dc bus (Vdc) to 0 Vdc, at the same time the voltage across the upper-switch (synchronous switch, soft switching condition) is increasing from 0 V to Vds (during dead time). The increasing voltage across the upper switch creates an increasing voltage across the Miller capacitance of the semiconductor (Cdg_H). This positive voltage induces a current going into the gate loop and generates a positive voltage perturbation (see Fig. 4.1.a). If this parasitic voltage exceeds the threshold voltage (V_{th}) of the switch, the induced current can charge the equivalent input capacitance (C_{iss}) of the device and the operation of the SiC MOSFET will not stay in cut-off region and will enter to the saturation region which can partially or fully turn-on the device. This partial turn-on results in a shoot-through current leading to additional losses in both switches and potential circuit oscillations since the shoot-through current passes the parasitic inductance Ls_H and Ls_L in semiconductor package. These parasitic elements pull down the source voltage of the switches in the half-bridge configuration and decrease the switching speed [112]. In case of fully turn-on of the switch, a short-circuit happens due to the simultaneous conduction of both switches of the half-bridge which can destroy the semiconductors [178]. The same phenomenon can be repeated in the lower switch (see Fig. 4.1.b). During dead time, as soon as the upper switch (controlled switch-hard switching condition) turns on, an increasing voltage across the lower switch (synchronous switch-soft switching condition) creates parasitic voltage across the low-switch gate (see Fig. 4.1.b).



(a) (b)

Figure 4.1 – Positive gate perturbation in half-bridge SiC MOSFET (a) High-side perturbation (low-side switch is controlled and high-side switch is in soft switching condition) (b) Low-side perturbation (high-side switch is controlled and low-side switch is in soft switching condition).

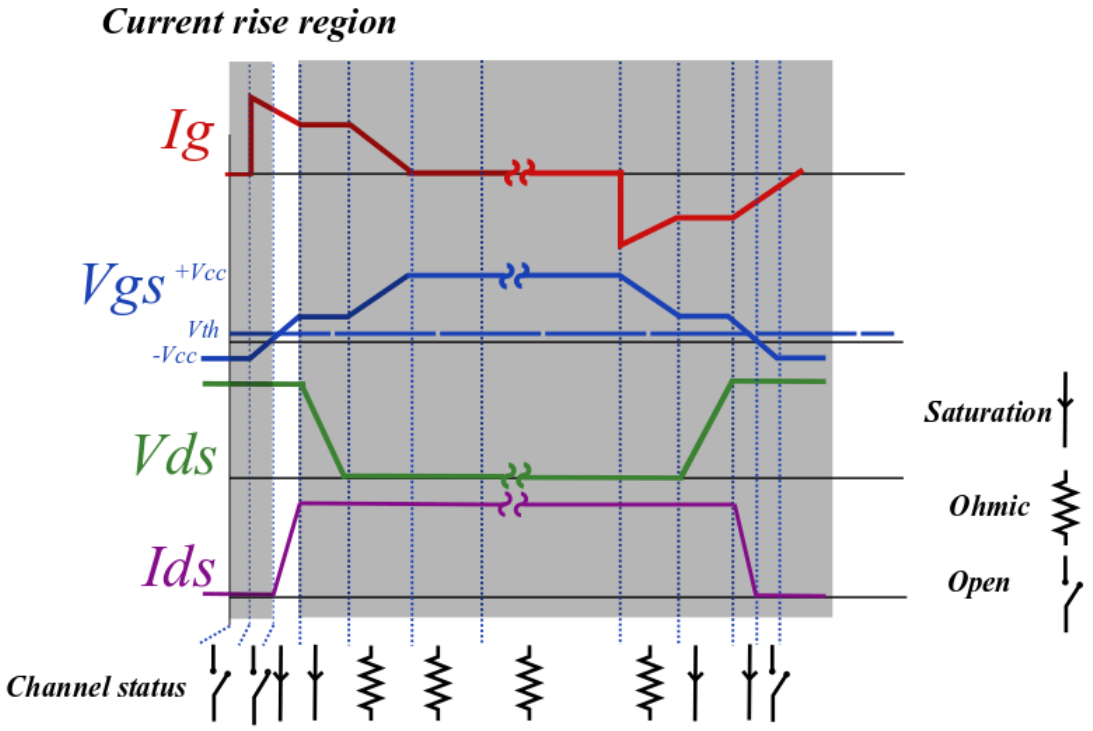
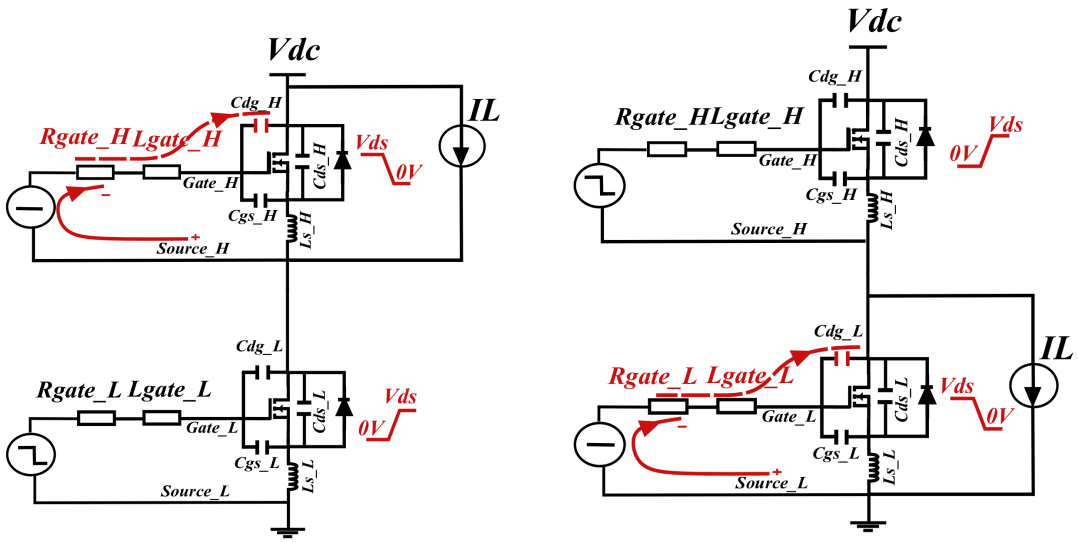


Figure 4.2 – Turn-on transition of SiC MOSFET

4.2.2 Negative parasitic-voltage in gate

Similar to turn-on transition, during turn-off transition of the lower switch (controlled switch, hard switching condition), the decreasing voltage across the synchronous upper switch (Vdc to 0 V) coupled to the Miller capacitance Cdg_L and due to the parasitic elements of the gate, creates a negative parasitic voltage across the gate of the switch. If this negative voltage exceeds the maximum allowable negative gate bias of the switch, it can over stress and may destroy the gate oxide layer of the power MOSFET [55, 60, 76]. As it has been explained before, the same phenomenon repeats during turn-off transition of the upper-switch (controlled switch, hard switching condition) which creates negative gate voltage perturbation during the dead-time in lower-switch (see Fig. 4.3).



(a) (b)

Figure 4.3 – Negative gate perturbation in half-bridge SiC MOSFET (a) High-side perturbation (low-side switch is controlled and high-side switch is in soft switching condition) (b) Low-side perturbation (high-side switch is controlled and low-side switch is in soft switching condition).

This phenomenon has been called in many dissertations “cross-talk”, “self-turn-on”, “false turn-on”, “false triggering”, etc. This positive and negative parasitic voltage perturbation due to complementary switching transient in half-bridge configuration is called in this work “self-disturbance” phenomenon since it can disturb the normal operation of the switches and the increased associated CM current due to this phenomenon consequently can disturb the operation of the converter and increase the losses.

4.3 Contributors in self-disturbance phenomena

The mechanism of this induced voltage on the gate has been studied in [18, 54, 74, 111, 157, 182, 185]. Analytical investigation of the circuit during turn-on and turn-off has shown that the maximum gate voltage perturbation is given by equation. 4.1 [112, 144] where (see figures 4.1 and 4.3) the dv/dt is the slew rate of the voltage across the switch, C_{iss} is the input capacitance of the DUT, C_{dg} is the Miller capacitance of the DUT and R_{gate_H} is the gate resistance, thus these elements contribute to the peak of the driving voltage perturbation. It is noteworthy that the same equation can be applied to $V_{gs_L}(max)$ also.

$$V_{gs_H}(max) = \frac{dv}{dt} R_{gate\_H} C_{dg\_H} \left(1 - e^{\frac{V_{DC}}{\frac{dv}{dt} C_{iss} R_{gate\_H}}} \right) \tag{4.1}$$

Based on figures 4.1, 4.3 and equation 4.1, it can be concluded that the voltage perturbations are mainly dominated by the voltage variation and the value of the junction capacitances. The impedance of the gate path ($R_{gate\_H} + L_{gate\_H}$) is an unavoidable factor in the design of the gate driver which has to be minimized at early design stage of the gate driver layout and packaging of the semiconductors. The parasitic inductance is the sum of the PCB tracks from the output stage of the driver to the added parasitic inductor due to the connection of the gate driver to the device and a parasitic inductance due to the packaging of the device [107].

To further highlight the effect of the parasitic capacitances and the switching characteristics that adds difficulty to the design of the SiC MOSFETs gate driver compared to IGBTs gate driver, the SiC MOSFET and Si IGBT has been measured experimentally in a double pulse test platform that has been presented in detail in chapter 3 (see Fig. 4.4).

The Wolfspeed SiC MOSFET half-bridge module CAS300M17BM2 package [168] and Infenion IGBT half-bridge FF450R33T3E3 package [3] have been selected to be compared experimentally. The electrical characteristics of the two modules are outlined in Table 4.1. In order to keep the effect of the gate impedance constant between two tests for a fair comparison, the same gate driver has been used for both analyses. The external gate resistance in the design of the gate driver is fixed to 0.2Ω for both IGBT and MOSFET tests. The added external gate resistance is small compared to the internal resistance, so as, the effect of the added resistance on switching speed is negligible and both switches operate at the maximum switching speed. Moreover, a fair comparison has been respected by implementing the same gate driver on the same layout of the double pulse test. The only difference is -as

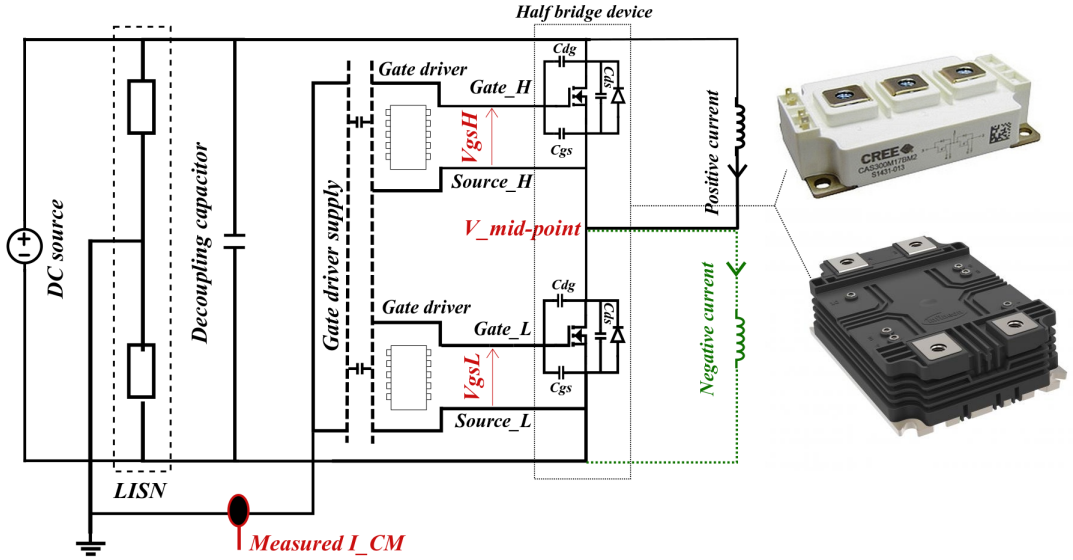


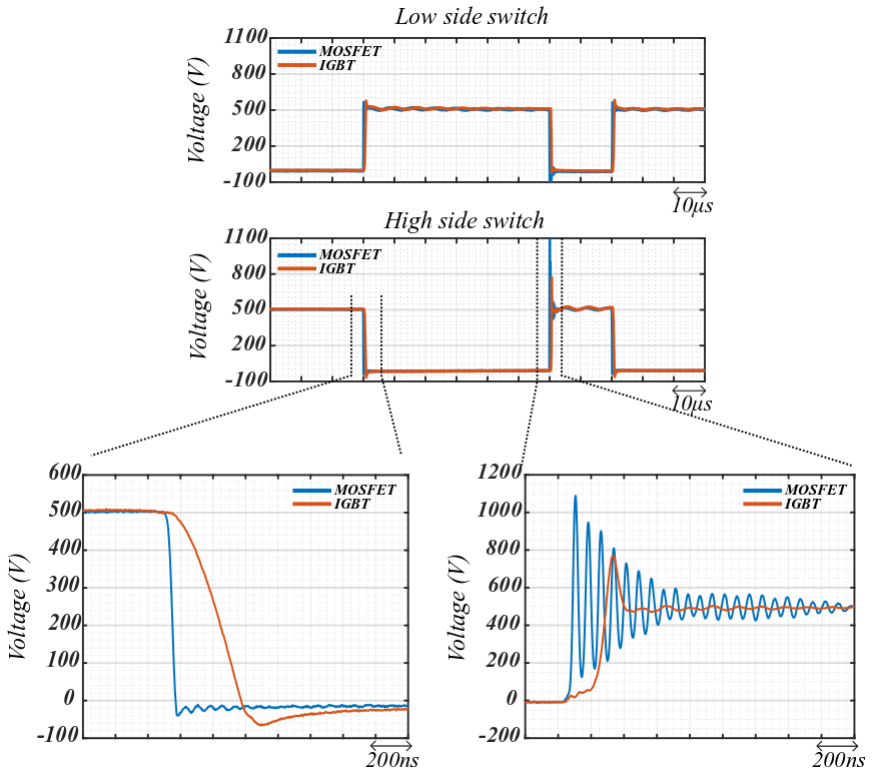
Figure 4.4 – Double pulse test set up for IGBT and MOSFET

it is advised in the data sheet of the two devices- the SiC MOSFET gate driver has been supplied between +20 V to −6 V and the IGBT supply has been regulated between +15 V to −15 V.

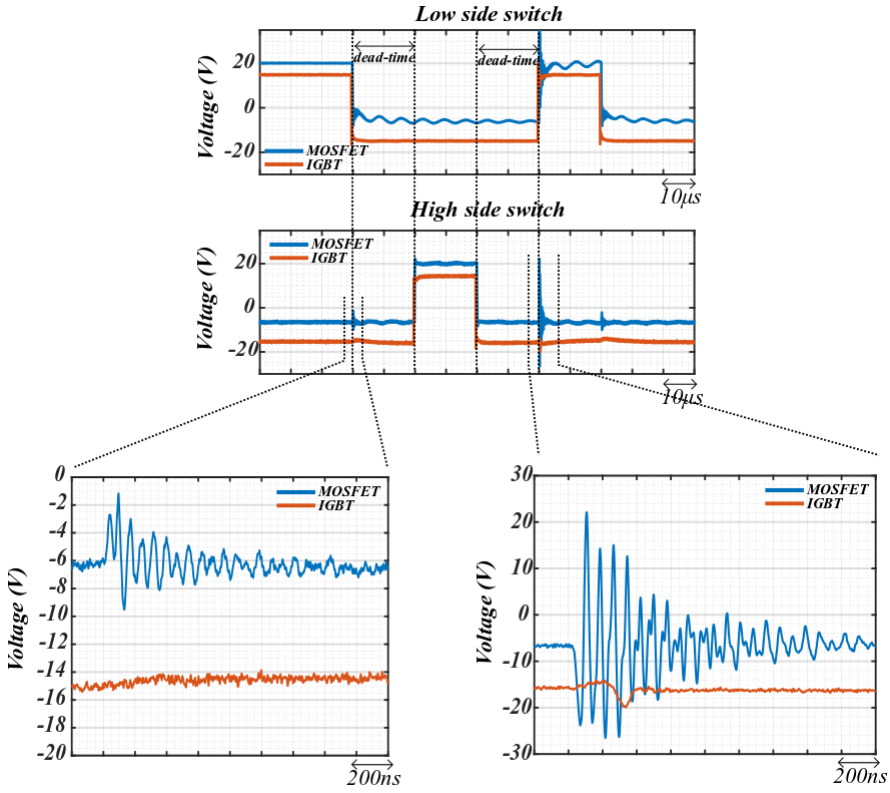
Table 4.1 – Electrical characteristic of the considered MOSFET and IGBT module [168] and [3].

Parameter	Unit	SI IGBT	SiC MOSFET
Vth	V	5.2	2.5
Ciss (Cgs+Cdg)	nF	84	20
Coss (Cds)	nF	3.5	2.5
Crss (Cdg)	nF	2	0.08
Qg	μC	12.5	0.273
Qrr	μC	230	324
Rint	Ω	1.3	3.7

The experimental results shown in figures 4.5 and 4.6, prove that, almost 4 times faster switching speed of the SiC MOSFET compared to IGBT module causes a higher gate voltage perturbation even if the value of the junction capacitance is lower in SiC MOSFET. The significant gate voltage perturbation prevents increasing the DC voltage and using all the abilities of the SiC MOSFET power module. Therefore, in a half-bridge configuration, in order to fully benefit from the potential advantage of fast switching rate of SiC MOSFET and guarantee the proper operation of the power devices, self-disturbance phenomena should be suppressed. Moreover, the bigger negative bias of the IGBTs compared to SiC MOSFETs, reduces the risk of short-through in half-bridge configuration of the IGBTs. Therefore, self-disturbance

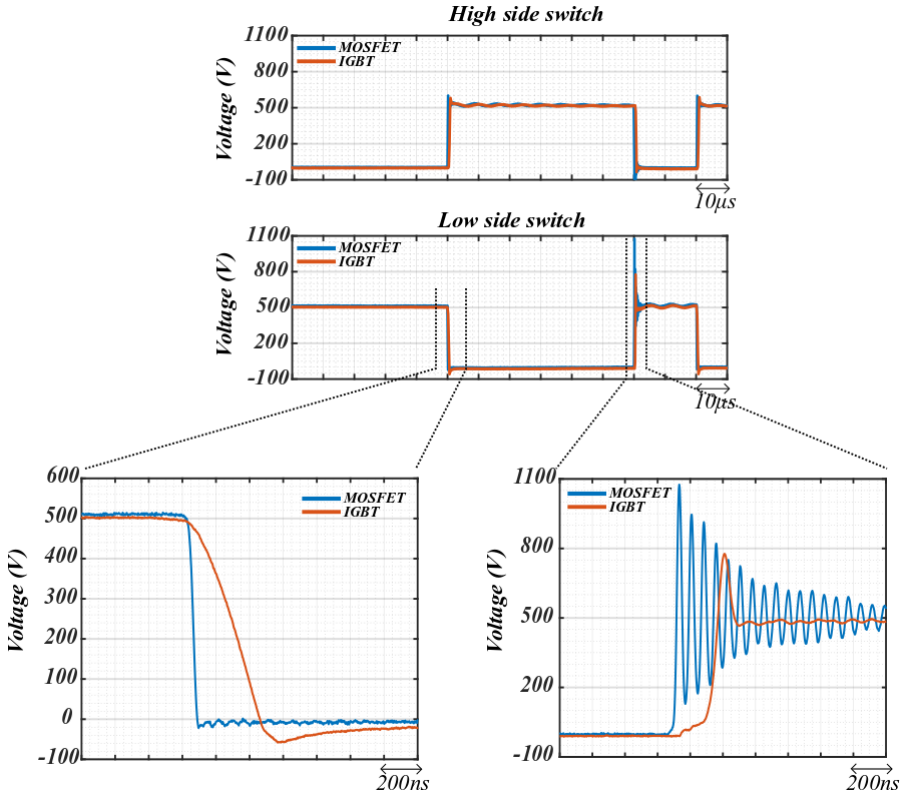


(a)

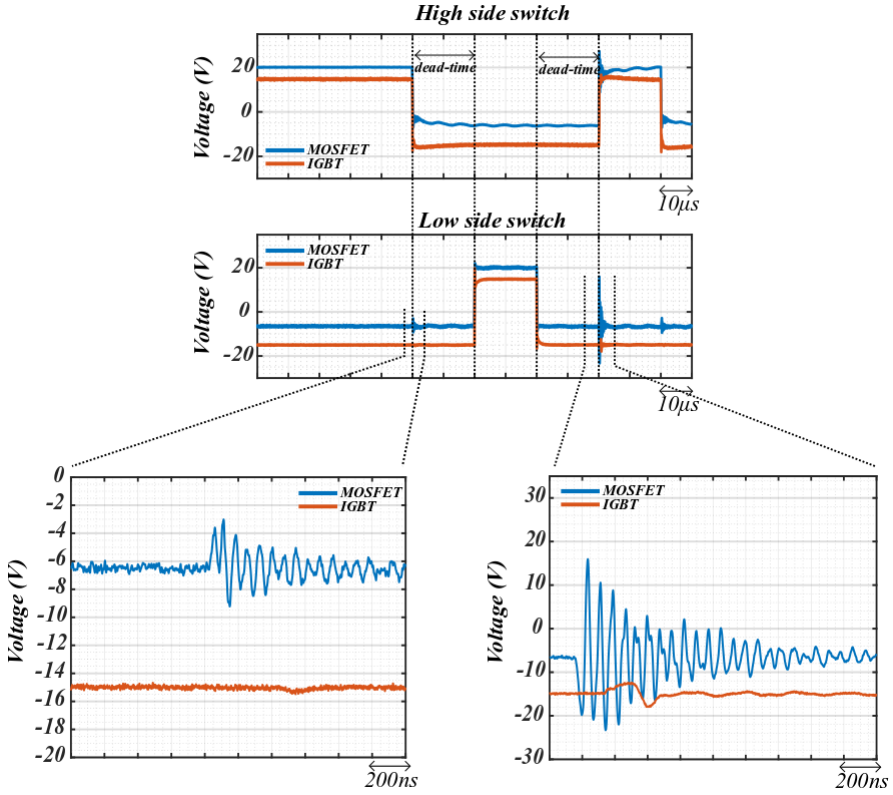


(b)

Figure 4.5 – Comparison between IGBT and MOSFET in double pulse test, 500 V, +150 A (low-side switch is controlled in hard switching condition, high-side switch is synchronous in soft-switching condition) (a) drain-source voltage comparison (b) gate-source voltage comparison.



(a)



(b)

Figure 4.6 – Comparison between IGBT and MOSFET in double pulse test, 500 V, -150 A (high-side switch is controlled in hard switching condition, low-side switch is synchronous in soft-switching condition)(a) drain-source voltage comparison (b) gate-source voltage comparison.

phenomenon is one of the first element that should be considered when introducing SiC MOSFETs in a converter instead of IGBTs.

The same experiments have been repeated for negative current direction in test platform where the low-side switching is affected by the upper-side switch. As it can be seen in figure 4.6, when the low side switch is in soft-switching conditions, the maximum voltage perturbation reached 15 V compared to 20 V when the high-side switch is in soft-switching (Fig. 4.5). The experimental results shown in figures 4.5 and 4.6, illustrate that in order to fully benefit from the potential advantage of fast switching rate of SiC MOSFET and guarantee the proper operation of the power devices, self-disturbance phenomena should be suppressed. Moreover, the bigger negative bias of the IGBTs compared to SiC MOSFETs reduces the risk of short-through in half-bridge configuration of the IGBTs. Therefore, at the very beginning of the design of gate driver this different characteristics has to be considered seriously.

4.4 State of the Art and active Miller-clamp protection circuit

As it has been shown in section 4.3, the effect of the complementary switching prevents increasing the DC voltage due to the significant gate voltage perturbation in SiC MOSFET. Therefore, in order to develop the SiC MOSFET gate driver, it is necessary to consider the difference between SiC MOSFET and IGBT where self-disturbance is one of the main challenges. As it is shown in section 4.3, switching speed is the key contributor to this phenomenon.

The classical method to reduce the self-disturbance is to slow down the switching speed. It reduces the voltage variation (dv/dt) across C_{dg} and consequently reduces the induced current to the gate. This method is obtained by prolonging the charging of the input capacitance of the device (C_{iss}) either by adding an external input capacitance [141, 178], either by increasing the gate resistance [6, 124, 138]. Increasing the gate resistance while the gate paths for turn-on and turn-off are not separated increases the impedance of the gate and increases the risk of self-disturbance. So as, it is extremely important to provide different paths for $Rgoff$ and $Rgon$ for gate driver.

Slowing down the switching speed results in increasing losses which is in contrary with the goal of using SiC MOSFETs. During the development of the gate driver for SiC MOSFETs, there have been several works illustrating the different methods to suppress the gate-source voltage perturbation with a minimum effect on

the switching speed [112, 156, 191]. The methods which suppress the gate voltage perturbation can be categorized into two fields, active and passive methods. Moreover, most of the proposed solutions mainly focus on reducing the positive gate voltage perturbation with less attention given to the negative spurious voltage in gate-source [156].

4.4.1 Passive methods

The main aim of the passive method is to take advantage of the negative gate bias of the SiC MOSFET. In these methods, it is tried to move the parasitic voltage below V_{th} by imposing a negative offset for the gate voltage. Since this negative voltage bias is achieved by passive elements, these methods are called passive methods [28, 178, 188, 189]. Most of these proposed method increase losses. Reference [156] presented a novel resistor-capacitor-diode level shifter to establish a negative voltage bias during turn-off of the device for half-bridge devices and to keep the voltage below the threshold voltage of the device under test.

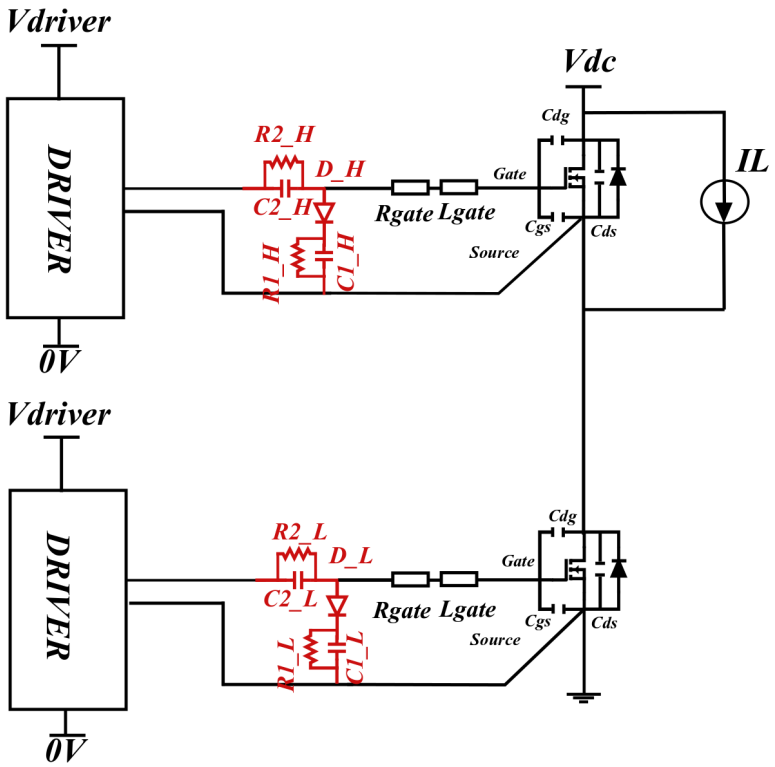


Figure 4.7 – Gate driver with RCD level shifter

The gate is supplied between $Vdriver$ V and 0 V (see Fig.4.7). During turn-on state of the low side switch, when gate voltage $Vdriver$ is applied to the level

shifter circuit, the D_L is forward biased and $C1\_L$ and $C2\_L$ get charged. The steady-state voltage across the input capacitance during turn-on is equal to:

$$Vgs\_on = \frac{R1_L}{R1_L + R2_L} \times Vdriver \tag{4.2}$$

and when the gate-source voltage of the device is turned to off-state which is $0V$, the Vgs is equal to:

$$Vgs\_off = -\frac{R1_L}{R1_L + R2_L} \times Vdriver \tag{4.3}$$

Since this method is composed of only passive components, it can be easily integrated in the design of the gate driver. However, imposing the Vgs is based on the charging and discharging of the $C1$ and $C2$ which are assumed to be enough bigger than the input capacitance of the device under test. These additional capacitances can affect the turn-on switching speed. Considering that, during turn-on transition, there is a need to charge this added capacitance, it will increase the charging time of the input capacitance of the device and consequently slow down the switching speed. Although the proposed gate driver has reached a better trade off compared to [188] and [189] in terms of losses authors did not provide a method to overcome negative parasitic voltage. Negative biasing of the SiC MOSFET is low compared to Si devices so the negative spurious voltage should be taken into account seriously since it can over-stress the devices. To do so, the references [55, 156, 190] presented similar passive solutions for negative gate parasitic voltages but there is no solution proposed for positive gate perturbation. Moreover, the mentioned solutions have not been experimentally validated for high power SiC MOSFET. Besides all the advantages and disadvantages of the passive methods, most of these methods have pursued to provide a negative bias with passive components while the proposed gate driver in this work is the voltage source push-pull (totem-pole) gate driver which facilitates to provide a negative bias for gate (see Fig. 4.8). The gate is driven between $V_{cc} = 20$ V and $-V_{cc} = -6$ V.

4.4.2 Active methods

Another category of solutions that has been presented to overcome self-disturbance is called "active methods". For these methods, an assistant circuit is added to the gate driver circuit. The assistant circuit is activated during off-state of the switch by an external control signal. The main idea of the active methods is to regulate the impedance of the gate during off-state by proposing a path of lower impedance to

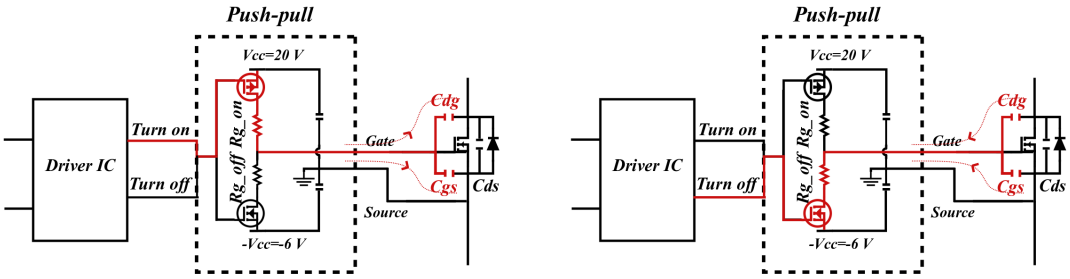


Figure 4.8 – Output stage of gate driver with push-pull (totem-poll) (a) Turn-on transition in push-pull (b) Turn-off transition in push-pull

the induced current towards the negative bias of the gate [165, 178, 184, 191]. Figure 4.9 shows a typical schematic of the active methods.

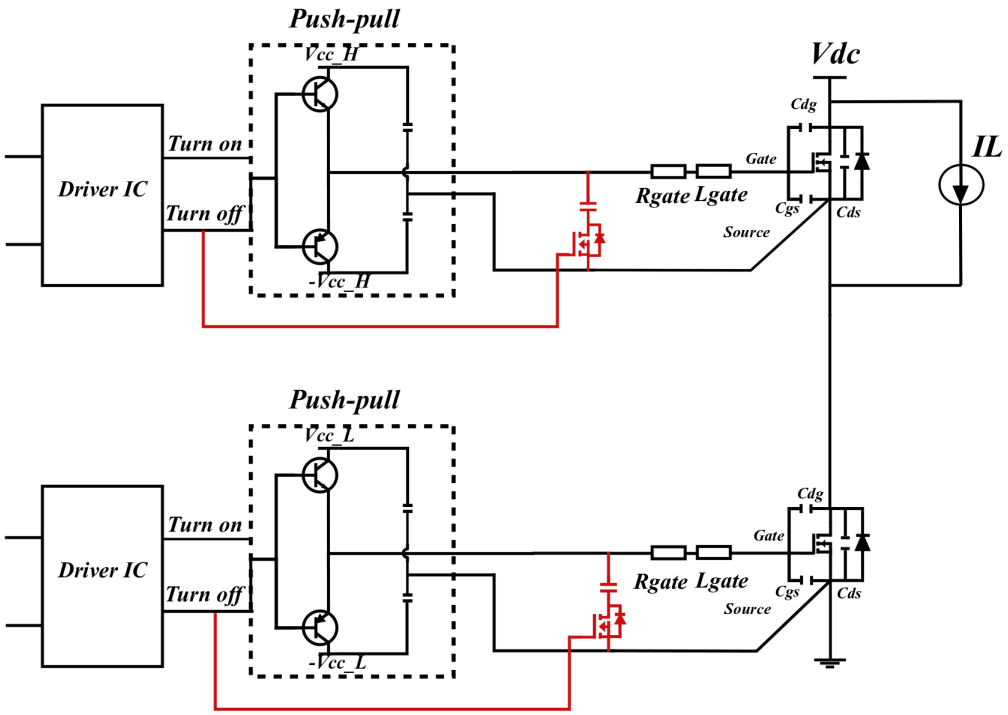


Figure 4.9 – Gate driver with integrated assistant circuit for self-disturbance [184].

Most of the proposed auxiliary circuits corresponds to an added transistor between gate and source which is activated during turn-off state of the switch in synchronous conditions (soft switching) and a capacitor in order to shorten the impedance of the proposed path to the induced current (see Fig. 4.9).

An appropriate control of the transistor of the auxiliary circuit can minimize the parasitic voltage in the gate. The complexity of this method relies on synchronizing the logic signal to turn-on the auxiliary transistor based on the main power device turn-off transition. In addition, to keep small the proposed path impedance to the induced current, it is advised to choose the capacitance big enough in order to

reduce the impedance (in red in Fig. 4.9). The big capacitance in the assistant circuit can affect the turn-on transition of DUT since it will be in parallel with the input capacitance of the device which is the case in [184] (see Fig.4.9). Another gate driver has been proposed in [184] (see Fig. 4.10).

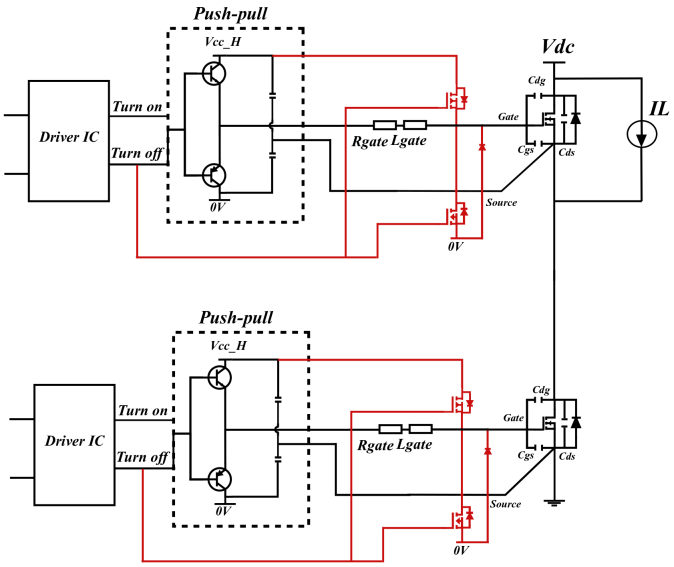


Figure 4.10 – Gate driver with integrated assistant circuit for self-disturbance [184].

The methodology in the design of this gate driver is based on the cancellation of the charge stored in the Miller capacitance C_{dg} by providing negative pre-charging of the input capacitance. In this proposed circuit, the device is supplied between 0 V and $VccH$. This assistant circuit provides a path for pre-charging the input capacitance by the auxiliary circuit added to the push-pull circuit of the driver. However experimental results shown in this work are limited to turn-off bias of the SiC MOSFET to 0 volt which consequently increase losses.

4.4.3 Proposed active Miller-clamp protection

Respecting the goal of keeping the switching speed, the Miller clamp protection circuit proposed in this work consists of an N channel MOSFET, one resistance and one capacitance (see Fig. 4.11).

The transistor is a power MOSFET (FDD13AN06A0) able to pass the 50 A peak current ($(C_{dg} + C_{gs})\frac{dv}{dt}$). The output capacitance of the auxiliary transistor is usually an order of magnitude smaller than the input capacitance of the DUT. This is how it guaranties that the assistant circuit has no impact on the turn-on switching behaviour. An example of this method is proposed in [32] but the experimental result is limited to $10V/ns$ while in this work is about $30V/ns$. When the SiC MOSFET (DUT) is turned off, the turn-off signal order of the IC driver is

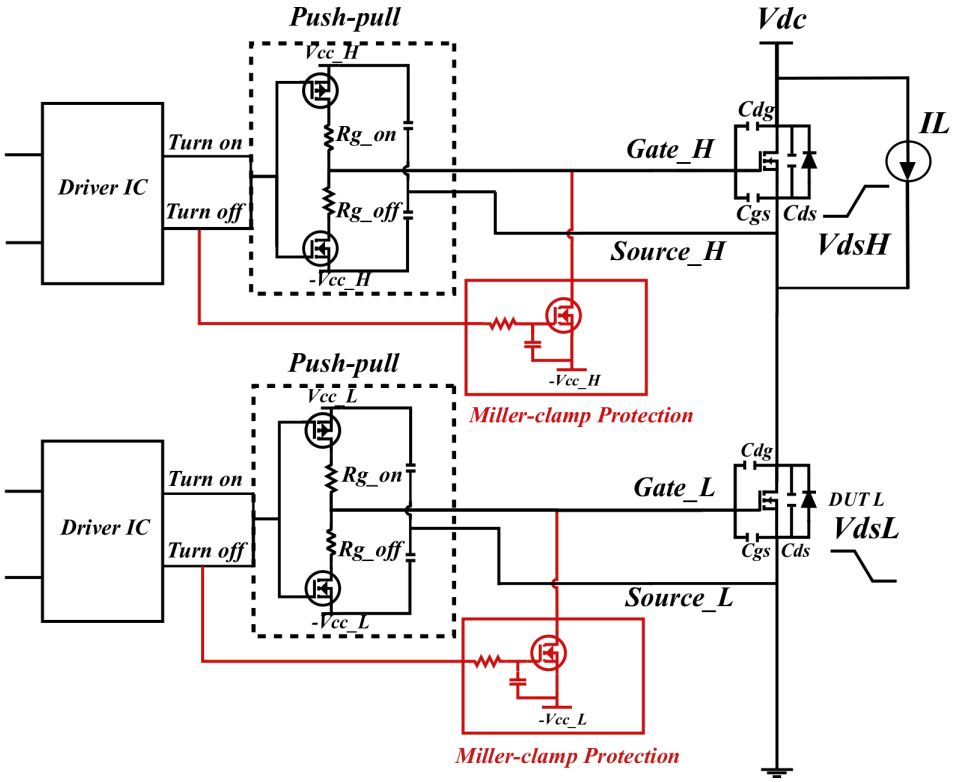
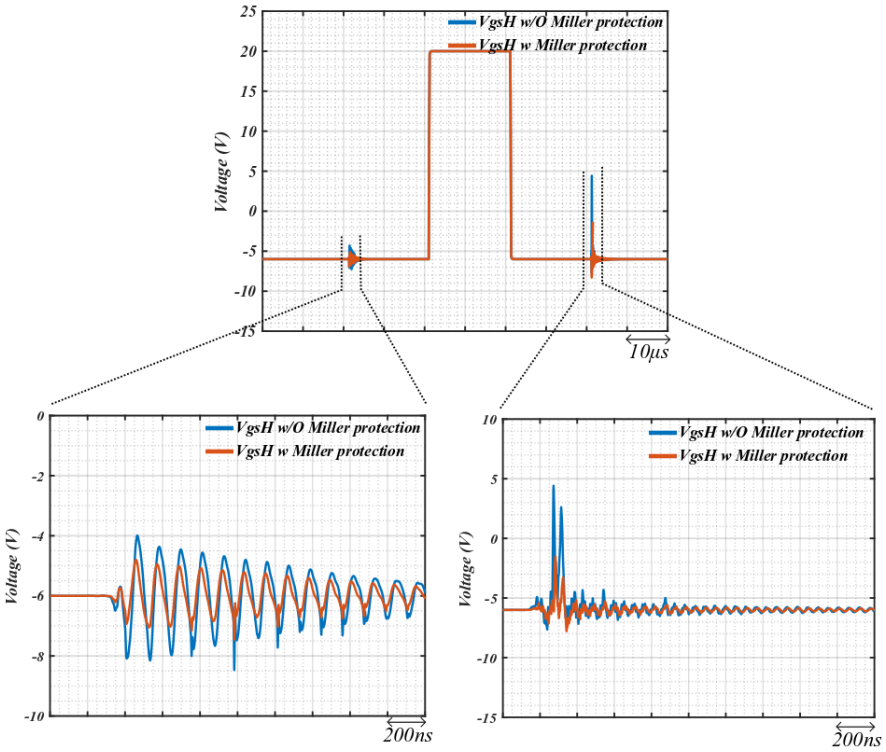


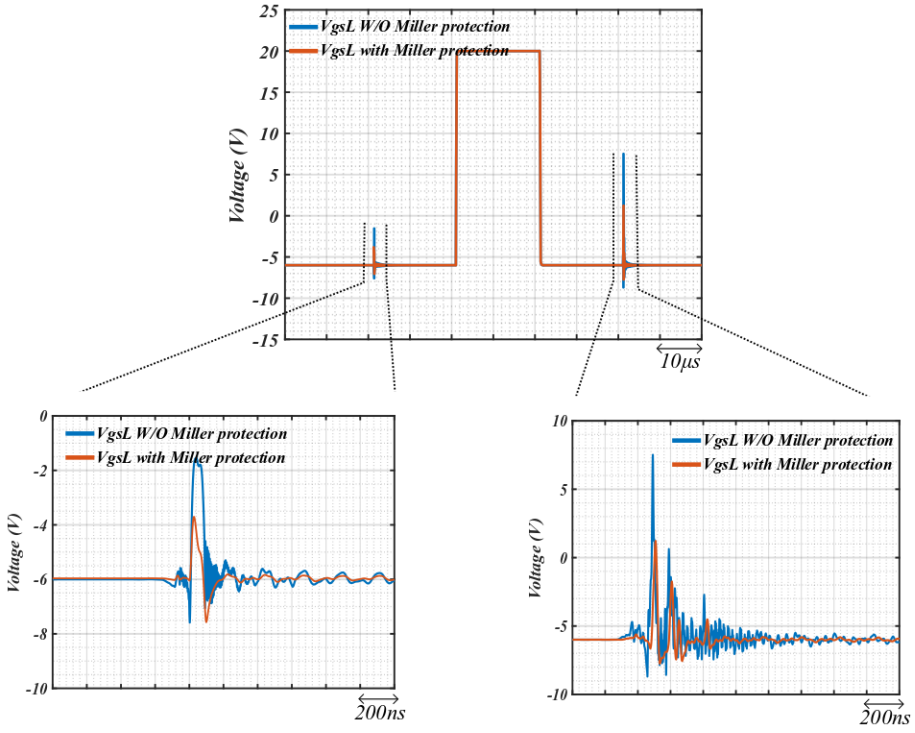
Figure 4.11 – Gate driver with proposed integrated Miller clamp protection assistant circuit.

sent to the transistor which forms a very low impedance path and shunts the induced Miller current. This introduced path instead of actual gate path, seen by the Miller capacitance induced current can reduce the gate perturbation. A concern is that in order to effectively clamp the gate voltage to the negative bias, the Miller-clamp MOSFET should turn-on when the device under test is fully turned-off. Therefore, to address the turn-on time interval of the switch in Miller-clamp protection, a first-order R-C circuit have been placed to provide a delay for turning-on the MOSFET and make sure that the actual gate voltage of the device under test is in its lower voltage. The turn-off order logic signals of auxiliary transistors are the same as that of their complementary main power devices except that the auxiliary transistors will remain ON until the end of the turn-off of the associated switch. To do so, the synthesized logic signals of the auxiliary transistors are the same as the turn-off logic signal of the DUT. The assistant circuit is called “Active Miller-clamp protection” and the circuit is shown in red in the figure 4.11.

The gate assistant circuit has been implemented in LTspice circuit, as it can be seen in figure 4.12, with 500 VDC supply voltage level. It can keep the parasitic perturbation less than the threshold voltage of the SiC MOSFET (see Fig. 4.12).



(a)



(b)

Figure 4.12 – Simulation results of comparison between the gate driver with (W) with Miller clamp integrated circuit and without (W/O) Miller clamp integrated circuit, double pulse test, 500 V (a) VgsH (synchronous switch, soft switching condition) in +150 A (b) VgsL (synchronous switch, soft switching condition) in -150 A.

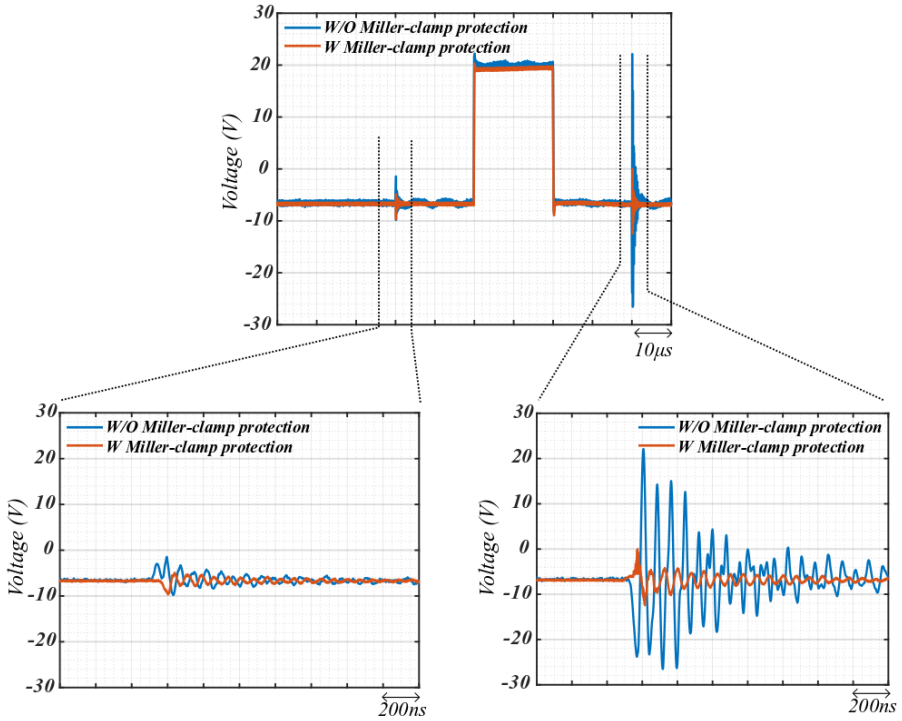
The same test has been done in the double-pulse test experimental-platform. The SiC MOSFET half-bridge module has been tested considering the active Miller-clamp protection integrated into the gate driver. The experimental results with integrated protection circuit for both sides of the half-bridge module have been compared with the gate driver without active Miller-protection circuit in both inductor current directions. The results are shown in figure 4.13. It can be seen that the protection circuit is able to decrease both negative and positive perturbations and keep the parasitic voltage lower than the threshold voltage for DC voltages up to 500 V. In this test, the voltage varied with a slope of about ($12.5kV/\mu s$).

The measurements have been repeated with increasing DC voltage levels to show the effectiveness of the Miller-clamp in simulation and during experimental considering the gate resistance always set to 0.2Ω. By increasing the DC voltage level up to 1200 V (corresponding to a voltage slope of about $30kV/\mu s$), it can be seen that the protection circuit can not completely keep the parasitic voltage lower than the device threshold-voltage (see Fig. 4.14 and Fig. 4.15). It can be seen that by increasing the voltage slope ($\frac{dv}{dt}$), the Miller clamp protection is no more able to overcome the voltage perturbation and consequently the parasitic voltage exceeds the threshold voltage of the device.

The simulation and experimental results have illustrated that Miller clamp protection is limited in this application to a voltage of 500 V level of voltage. Adding an external capacitance to the Miller protection circuit, can further shorten the impedance of the proposed gate path to the induced current to gate and reduce the voltage perturbation but at the same time it can affect the turn-on transition of the DUT. The active assistant circuit presented in [176] applied for the same DUT as in this work, showed the increase of losses and Vgs oscillation due to the added capacitance to the assistant circuit (see Eq. 4.4 [154]) leading to a following equation represents the value of the gate resistance:

$$R_g \leqslant 2\sqrt{\frac{L_g}{C_g}} \tag{4.4}$$

In simulation, the external capacitor has been added to the Miller clamp circuit (see Fig. 4.16). For example, in 700 V DC voltage level, in order to reduced the voltage perturbations less than the threshold voltage, a 40 nF capacitor has been added to the circuit to reduce the parasitic voltages. The simulation results are shown in figures 5, 6, 7, 8 in annex of this chapter. They illustrate how this added capacitance can change the switching speed and also generates oscillation to gate



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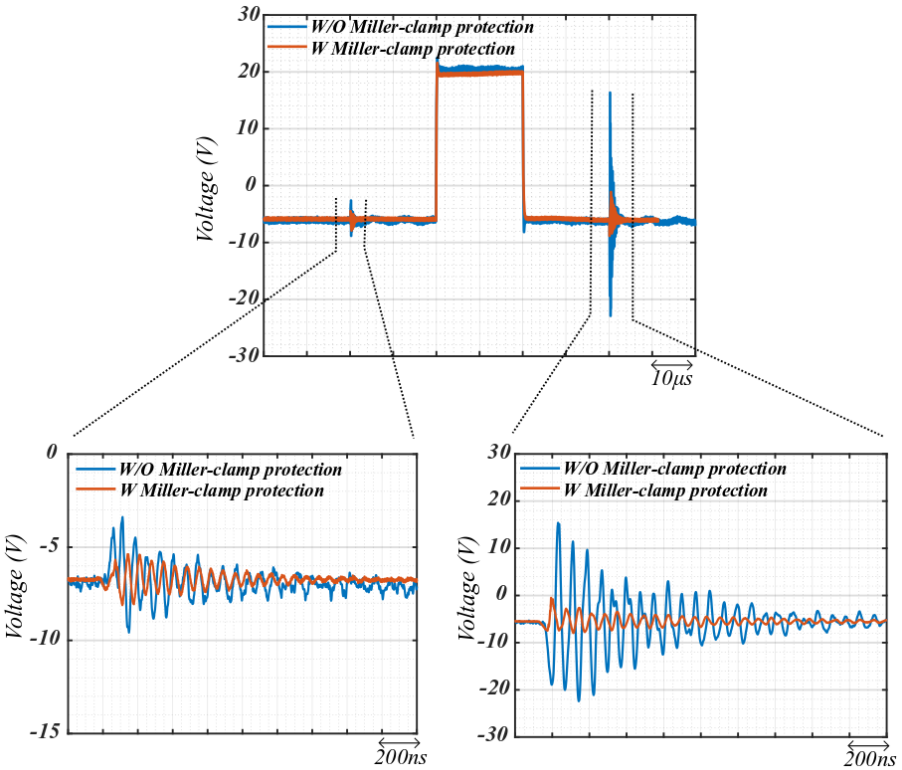
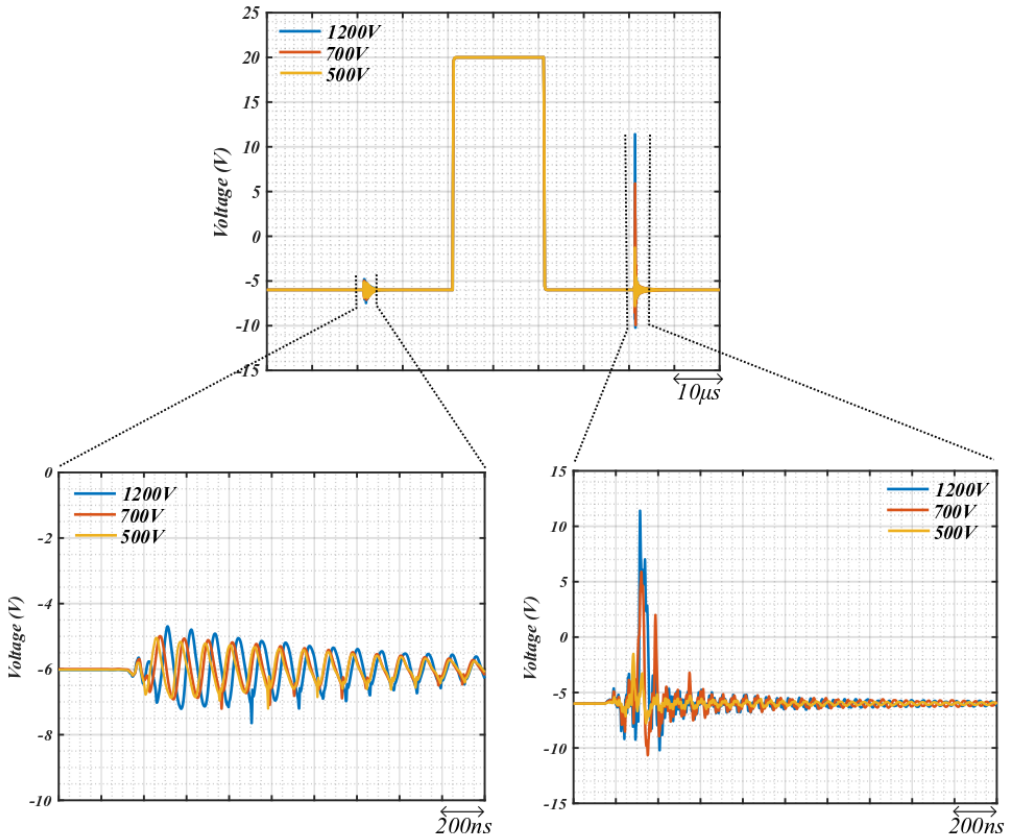


(b)

Figure 4.13 – Experimental results of comparison between the gate driver with (W) with Miller clamp integrated circuit and without (W/O) Miller clamp integrated circuit, double pulse test, 500 V (a) VgsH (synchronous switch, soft switching condition) in +150 A (b) VgsL (synchronous switch, soft switching condition) in -150 A.



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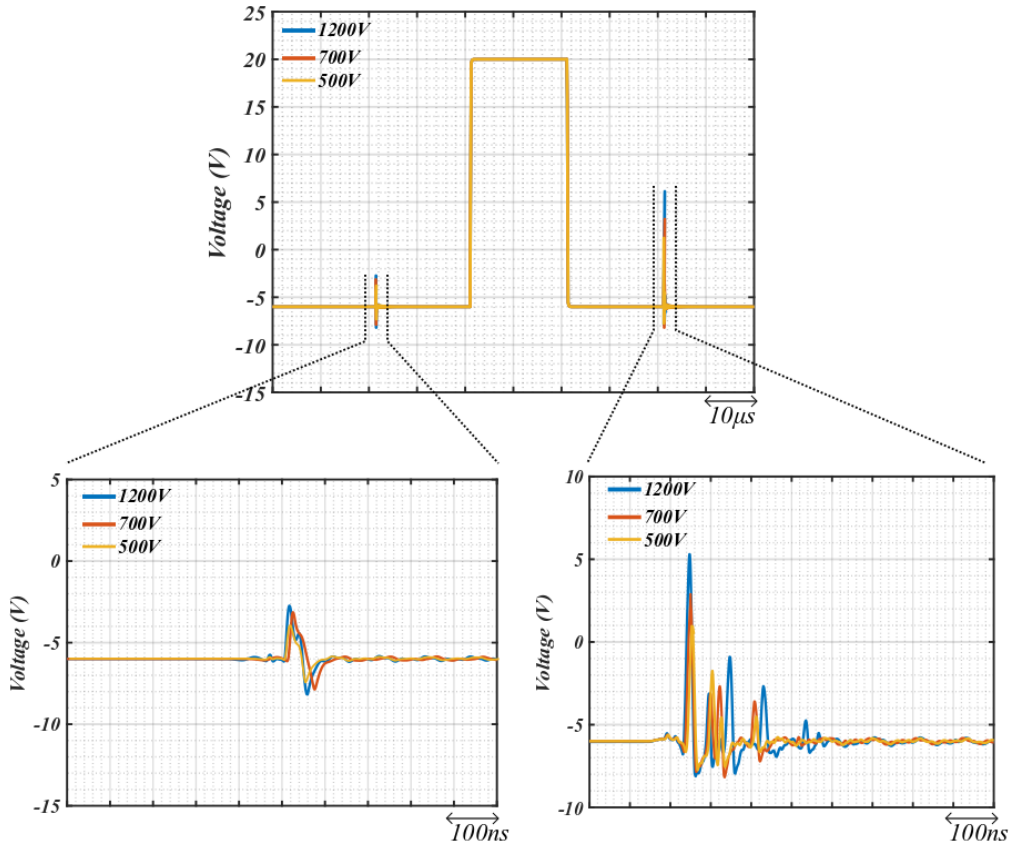
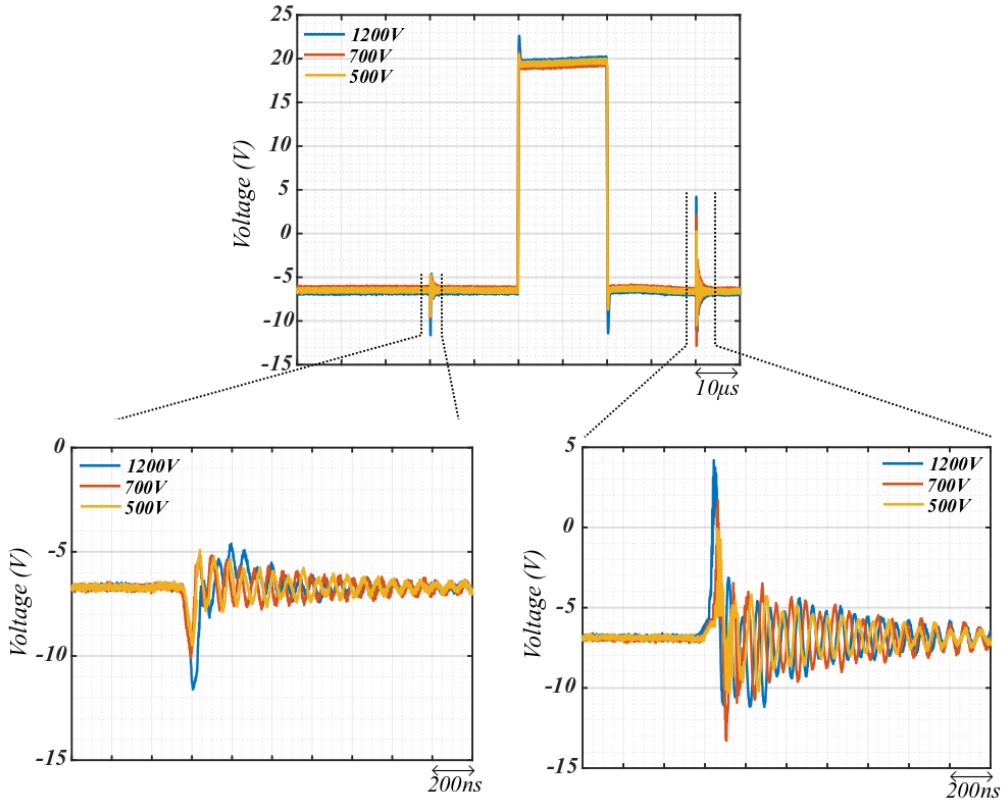
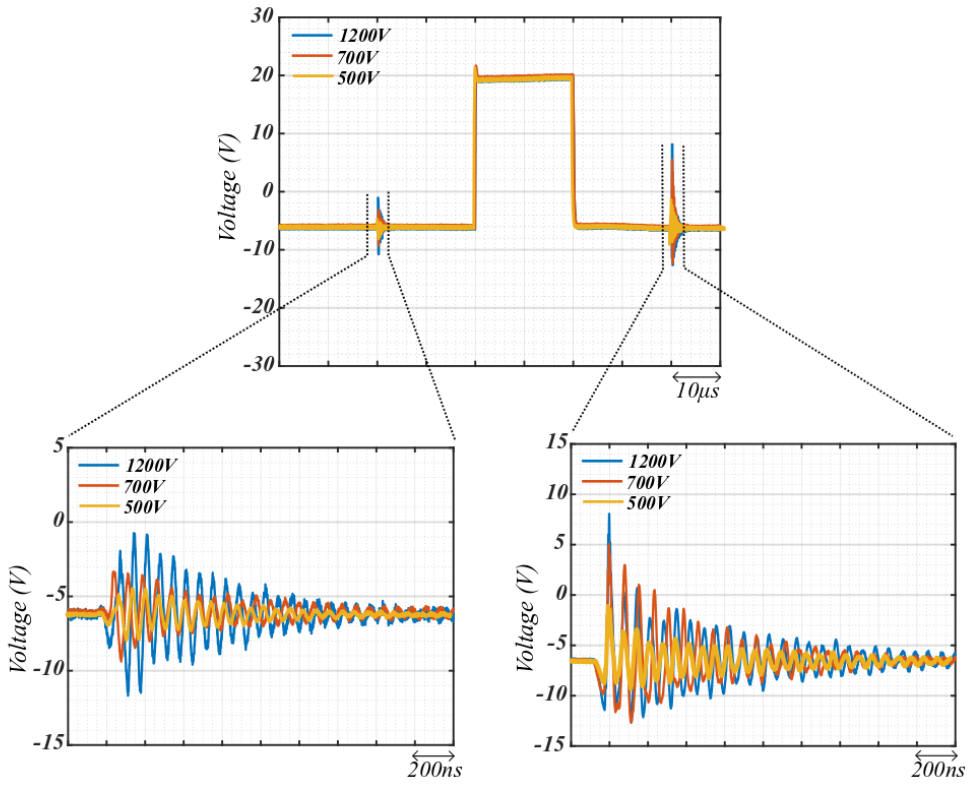


(b)

Figure 4.14 – Simulation results with Miller clamp integrated circuit, double pulse test, 500 V, 700 V, 1200 V (a) VgsH in +150 A (b) VgsL in -150 A.



(a)



(b)

Figure 4.15 – Experimental results with Miller clamp integrated circuit, double pulse test, 500 V, 700 V, 1200 V (a) VgsH in +150 A (b) VgsL in -150 A.

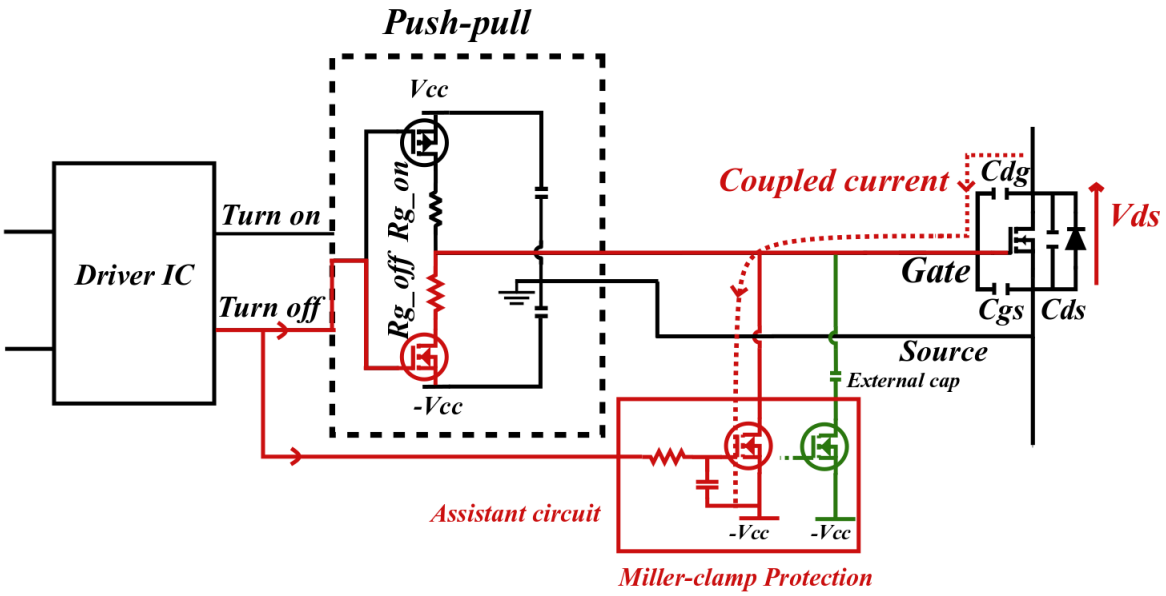
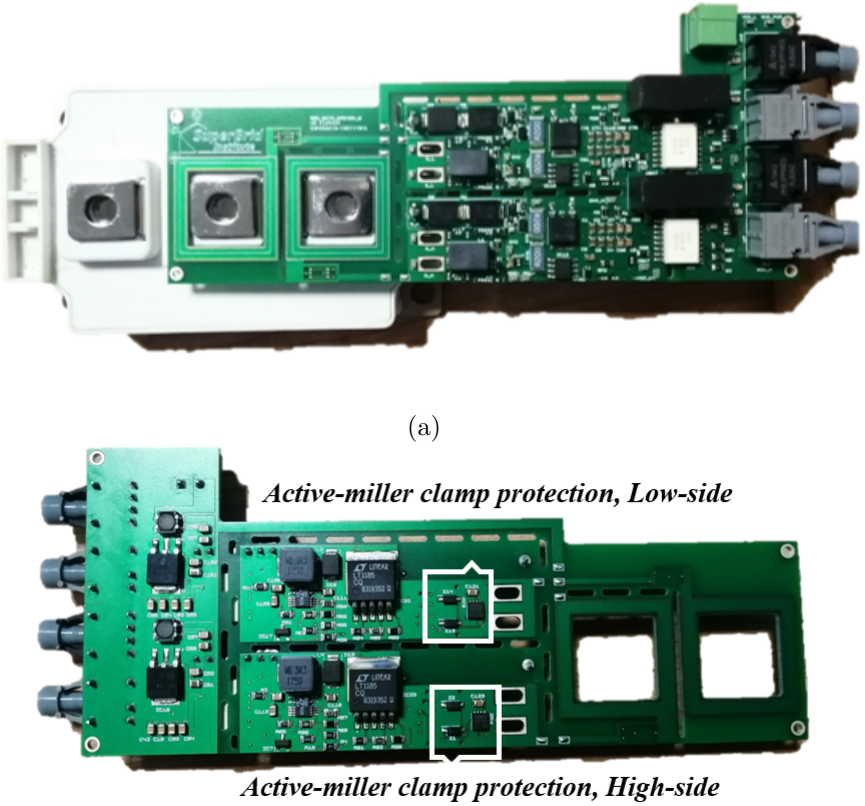


Figure 4.16 – Miller clamp protection circuit with added capacitance in green.



(a)

(b)

Figure 4.17 – Gate driver with proposed integrated Miller clamp protection assistant circuit (a) front view (b) back view.

voltage. The goal is to keep the switching speed as high as possible. To do so, in practice, this capacitance has not been added to the circuit (see Fig. 4.16).

Special attention should be also paid to the PCB layout of the gate driver circuit. Besides shortening the PCB tracks of the output stage from the gate driver to the device, it is vital to reduce the Miller-clamp protection loop. Therefore, the N Channel MOSFET should be placed as close as possible to the device under test (see Fig. 4.17). In the final prototype, thanks to double sided electronic board as it can be seen in Fig. 4.17, the small impedance loop has been respected.

4.5 Measuring a small differential voltage in a half-bridge

As it has been shown in section 4.4, gate-voltage measurement is used to optimize the design of the gate driver for fast switching SiC MOSFET. Comparing simulation and experimental results as shown in section 4.4 revealed the complexity of the system which is very hard to simulate accurately. Therefore a proper measurement technique is vital in this stage of the design of the gate driver to diagnose the problem which consequently affects the operation of the converter. The challenge is to measure a small signal inside a high switching voltage environment. The phenomenon is more clear for high-side switch in a half-bridge configuration with fast semiconductor devices where voltage probes are subject to high CM voltages (mid-point voltage variation in half-bridge device) with fast transients. Hence, this section compares experimentally the conventional differential probes with new optically isolated probes technology for measuring a small signal (26 V peak to peak, gate-source voltage of the SiC MOSFET) with a 1200 V CM voltage the (mid-point in figure 4.18) and high switching rates created by SiC MOSFET varying rapidly between 0 V to the DC source voltage (in this work $dv/dt \approx 30kV/\mu s$).

Most of the measurement equipment are affected by this big CM voltage and switching speed. So it is intended to show the great importance of the quality of the measurement in the design of the gate driver.

4.5.1 Challenges in front of the measurement in fast switching speed

The ability of the measurement equipment to deal with this CM voltage (mid-point in figure 4.18) without transferring it into a perturbation for the output signal is called CM rejection ratio (CMRR). The CMRR of a measurement equipment is

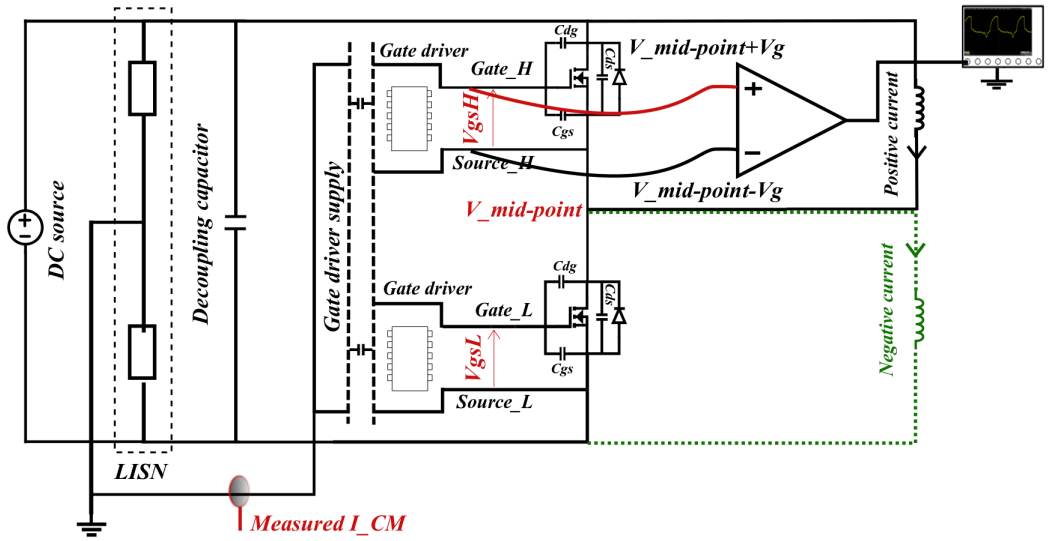


Figure 4.18 – Double pulse test schematic during VgsH measurement.

generally degraded at high frequency whereas the increase of switching speed is a trend in power electronic industry. Therefore, using maximum switching speed increases the risk of losing important information due to limitation of the measurement equipment. Moreover, the optimized design will be compromised because it will be based on incorrect measurement results. In this part of the manuscript, it is targeted to show the importance of the measurement in the design of the gate driver due to the specificity of the power converter. The experimental results of the section 4.4.3 will be re-discussed to show the aforementioned importance of the measurement in the gate driver design. Measurement challenges in gate-source voltage include: measuring small signals (26 V peak to peak) in the presence of fast variation of a high CM voltage (here $dv/dt = 30kV/\mu s$), measuring the correct gate perturbation due to the complementary switching effect (see section 4.2) and gate signal oscillations due to the parasitic inductance in the layout of the converter [171].

4.5.2 Theory of operation of voltage probes and problem statement

4.5.2.1 Conventional differential probe

The state of the art of differential measurement technologies for floating signal measurement like VgsH (both measurement points without ground reference) is conventional differential probe. In theory, it consists of two well-matched input voltage dividers linked to a differential amplifier to produce output signal as an

image of the measured signal. The ground referenced output signal of the differential amplifier as an indicator of the measured signal is the attenuated input signals [61] (see Fig.4.19).

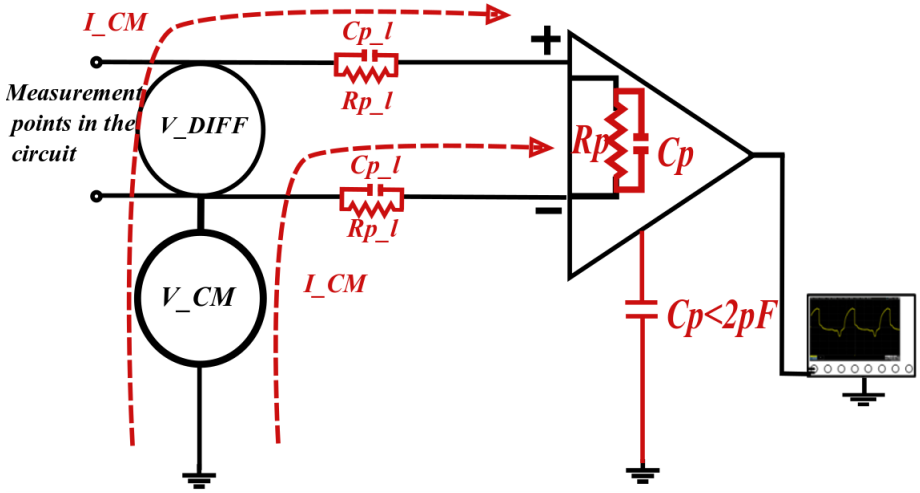


Figure 4.19 – Conventional differential probe

With the differential probe technique, both of the differential inputs of the probe are high impedance (high resistance and low capacitance). With the balanced impedance of both probe tips and low capacitance inputs, floating measurement can be done without risk of loading the circuit under test. If the inputs of this amplifier are connected to the same source signal, it is expected to have a zero output. An ideal differential amplifier would reject 100% of the CM signal that is how the output would be zero. However, in practice, it is very difficult to provide these balanced inputs impedances for differential probes and the probe fails to provide a good representation of the actual measured signal [21] in high voltage switching environment. The limitation of the probe is due to the imposed effect of the CM voltage (mid-point voltage in Fig.4.18). The CMRR of the measurement device is degraded at high frequency. This frequency is related to the maximum rise time of the signal not the switching frequency. So in high switching speed of high voltage semiconductor, the measurement is affected by this factor. Another factor that limits the ability of the differential probe is the effect of the long input leads of the probe. These limitations are more remarkable when testing power devices with fast switching under high voltage and consequently high CM voltage [147].

4.5.2.2 Isolated differential probe

The input stage of isolated probes is a voltage divider (similar to conventional differential probe) with much higher impedance (up to 10^3 times more) in comparison with conventional differential probe (Fig. 4.20)[148].

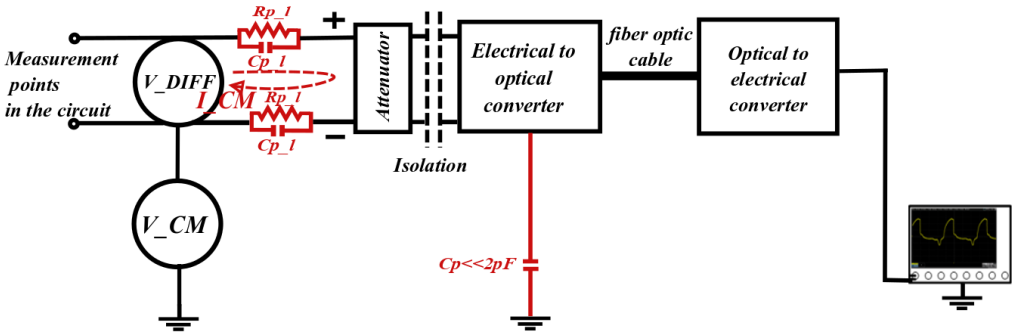


Figure 4.20 – Isolated differential probe

Moreover, in order to reach the minimum parasitic capacitance, all the connections of the probe terminals are locally shielded. The sensor head of the device provides an interface to change the measured data (electrical) to optical signal thanks to the electronic to optic converter. In addition, the electrical-to-optic and optic-to-electrical converters provide an optical isolation of the device under test from the oscilloscope. A fibre optic cable carries the information of the measured signal (instead of an electrical cable) which reduces the effect of the lead parasitic of the probe to almost zero. Conceptually, the electric-to-optic converter senses and sends the signal without involving the error of the unbalanced input of the differential amplifier. Moreover, the optical isolation of the supply of the isolated probe reduces the parasitic capacitances to a very small value. That is how it can remove the effect of the CM voltage rejection of the differential amplifier [148].

4.5.3 Experimental comparison between the two measurement technologies

The VgsH with t_{rise} equal to $70ns$ is measured where the mid-point voltage of the half-bridge is changing from 0 V to the supply voltage (1200 V) in maximum switching rate ($30kV/\mu s$) of the SiC MOSFET ($R_g = 0.2\ \Omega$). The measurements have been repeated in two different directions of the current. The differential probe [147], isolated probe [148] and an oscilloscope with a maximum 2 GHz bandwidth are used to be sure that the bandwidth of the measurement equipments (Eq. (4.5)) are 5 times bigger than the measured signal bandwidth (Eq. (4.6)) [73]. Lower bandwidth of the measurement would underestimate the value of the peak voltage

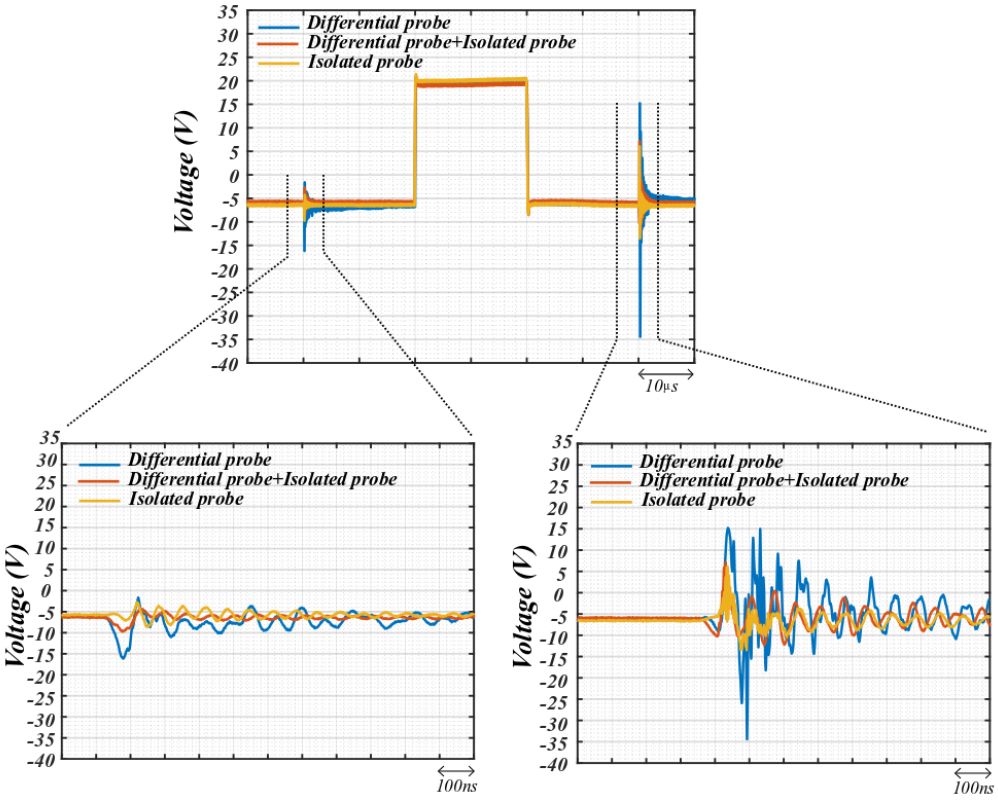


Figure 4.21 – VgsH experimental comparison of conventional differential probe and isolated probe, double pulse test, 1200 V, +150 A.

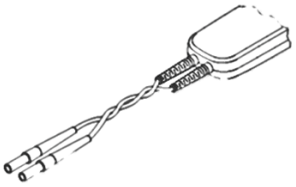
in the gate-source voltage of the device under test and consequently mislead in the design of the electronic device.

$$BW_{-3dB} = 1/\sqrt{1/BW^2_{-3dB,scope} + 1/BW^2_{-3dB,Probe}} \tag{4.5}$$

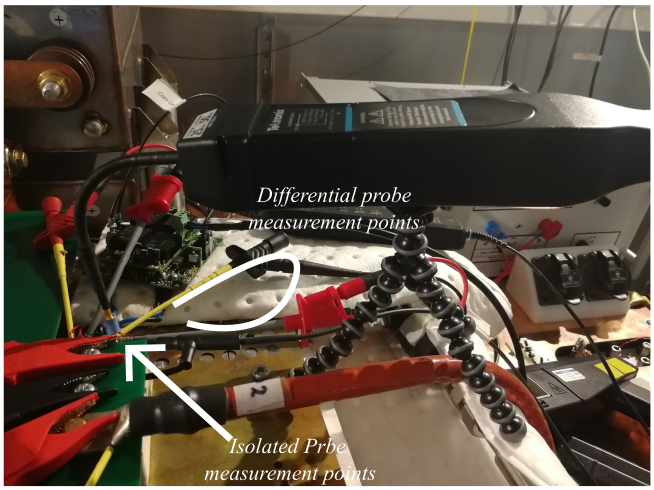
$$BW_{GHz} = 0.35/T_{rise}(nsec) \tag{4.6}$$

The comparison has been done by measuring VgsH where the CMRR ability of the probes should be able to reject 1200 V from 5 MHz (measured signal frequency bandwidth). The conventional differential probe data sheet provides the information of CMRR between 3.2 MHz to 100 MHz equal to 30 dB and 26 dB respectively [147]. Thanks to equation 4.7, it can be expected to have an error between 20 V to 37 V. Therefore, the error due to the conventional differential probe is not negligible. The same calculation can be done for the isolated probe with the ability of the CMRR from 160 dB at 1 MHz to 80 dB at 1 GHz which concludes to expect an error between 12 μV to 120 mV [148].

$$CMRR = 20 \times log10(V2/V1)(dB) \tag{4.7}$$



(a)



(b)

Figure 4.22 – Compare the inductance loop due to measurement techniques (a) twisted probe lead in conventional differential probe (b) inductance loop comparison between two technologies of the differential probe.

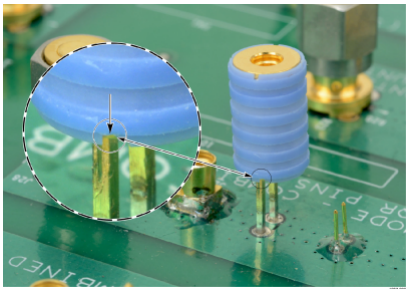


Figure 4.23 – Shielded solid metal connector system for isolated differential measurement [149].

The effect of the low CMRR of the conventional differential probe is shown in figure 4.21 where the difference between voltage perturbation changes based on different configurations.

A long lead is convenient for the user which is the case in classical differential probe. However, any piece of wire has distributed inductance, and the distributed inductance reacts to AC signals by increasingly impeding AC current flows results in a low frequency oscillation in measuring small signal (Vgs). In conventional differential probe by twisting two conductors (see Fig.4.22.a), it is tried to remove the harmful effect of the inductance loop of probe leads but in fast CM voltage variation is not efficient.

However in practice the probe leads cannot be completely coupled equally to the two opposite conductors (probe's lead), therefore it cannot eliminate all of the interferences due to the high CM voltage variation. In comparison by looking

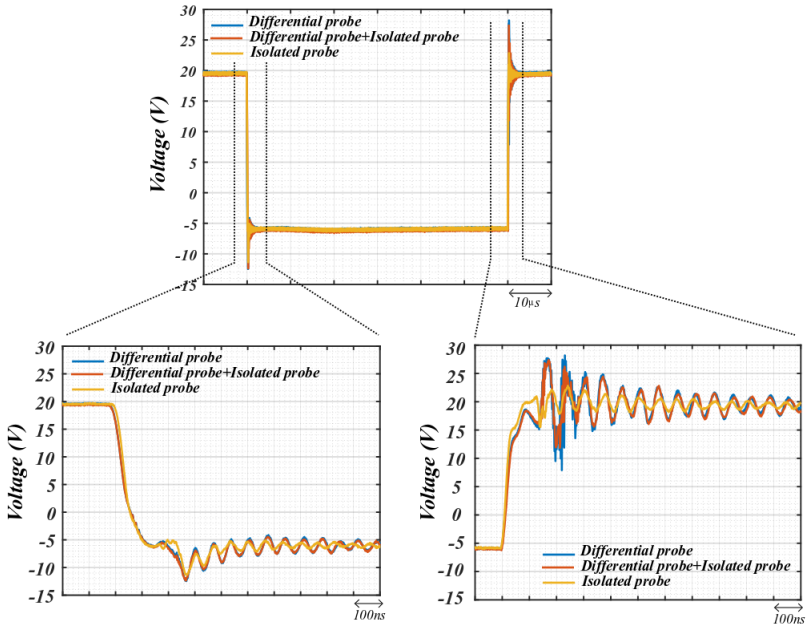


Figure 4.24 – VgsH experimental comparison between conventional differential probe and isolated probe, double pulse test, 1200 V, -150 A .

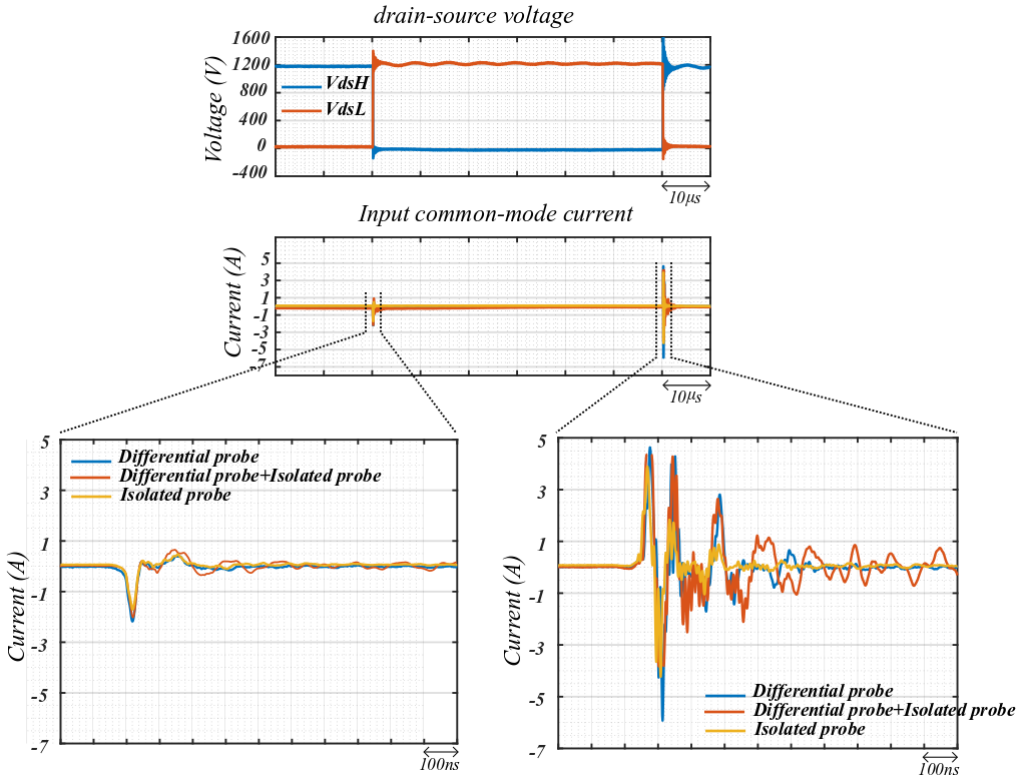


Figure 4.25 – Experimental comparison between conventional differential probe and isolated probe, Common-mode current of gate driver, in 1200 V, +150 A double pulse test.

into figure 4.22, it can be seen how new technology of the floating measurement reduced the inductance loop due to the measurement points connection. For Vgs measurement, it is important to minimize the effect of the input capacitance of probes and ground lead length. The small connectors of the isolated probe, could overcome the problem thanks to completely solid metal body of the connectors [149] (see Fig.4.23). The ground lead's inductance interacts with the probe input capacitance to cause ringing, it can be seen more precisely in figure 4.24 where the lead's parasitic impedance reacts to high CM voltage.

Following the investigation on the reaction of two different technologies of differential probes, the input CM current of the gate driver (measurement point is shown in Fig. 4.18) has been measured during the voltage variation across the switches. The goal is to show the impact of the different isolation of the two differential probes in producing wrong measurement data and how the parasitic elements of the voltage measurement as a path for the CM current change the measurement results. The new technology of the isolated differential probes increases the impedance of the input lead [148] while the value of the parasitic capacitance is very small compared to conventional one [21]. Moreover, optical isolated supply of the isolated probe prevents offering a path to for CM current into the circuit under test and measurement equipments.

The earth connected measurement [61] of the CM current (I_{CM}) of the gate driver power supply has been done for the two probes under 1200 VDC. The measured VgsH with isolated probe (yellow curve in figure 4.21) clarifies the CMRR ability effect of the probe when it is compared with captured VgsH by means of conventional differential probe (blue curve in figure 4.21). Moreover, repeating the same measurement while both conventional and isolated probes are connected shows how conventional probe provides a path for CM current and adds parasitic inductances due to the probe lead which changes the Vgs curve and consequently the gate driver behaviour (red curve in figure 4.21). The effect is more clear when only isolated probe is connected (yellow curve in figure 4.21). Experimental results (Fig. 4.25) showed how parasitic capacitance provides a path for the CM current, while optical isolation of the isolated probe outperforms the conventional differential probe up to 6 dB of the peak of the CM current. Therefore, in this work, due to the high switching rate of SiC MOSFET, gate-source measurements have been performed with optically isolated probe.

4.6 Proposed solution to reduce self-disturbance

The investigation shown in section 4.4.3 explained that thanks to Miller-clamp protection, the gate voltage perturbation is kept lower than the threshold-voltage for DC voltage up to 500V. The effectiveness of Miller-clamp protection in maximum switching rate has not been validated in higher voltage operation of the SiC MOSFET. Hence, for solving the perturbations due to fast switching, the CM current generated has been measured across each switch and in gate driver supply (24 V). The measurement points are shown in figure 4.26.

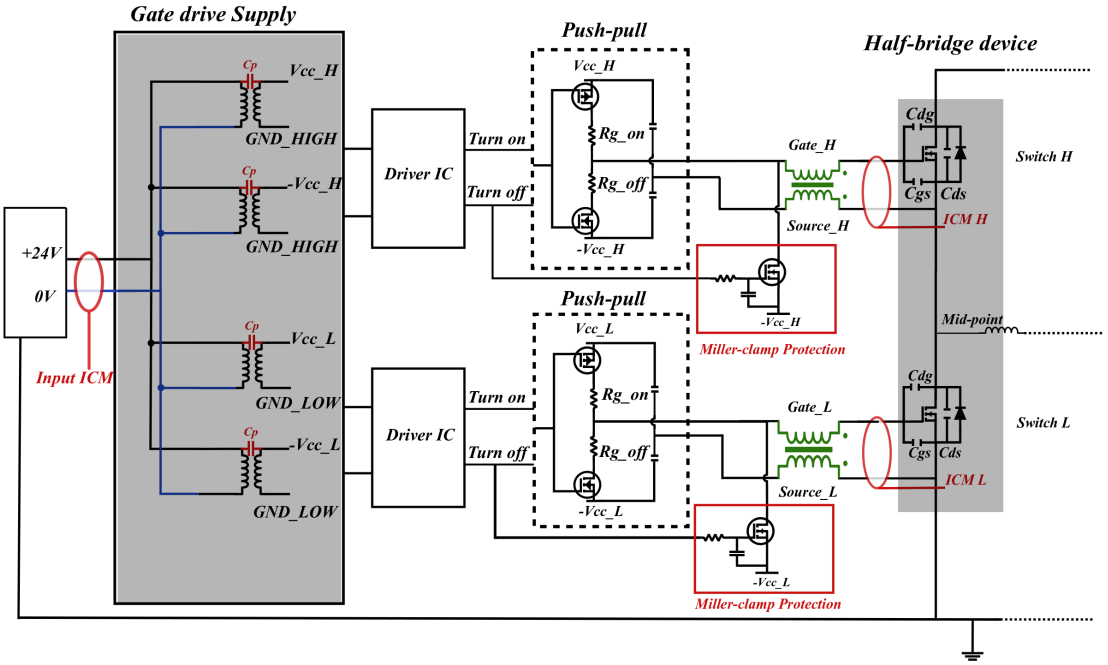


Figure 4.26 – Gate driver with proposed integrated Miller clamp protection assistant circuit for self-disturbance and proposed solution in green.

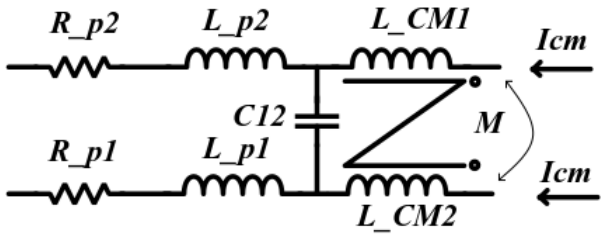
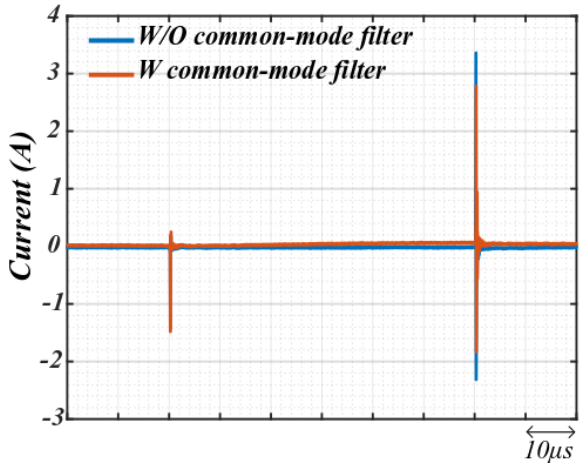


Figure 4.27 – Equivalent circuit model of a CM inductor.

The proposed solution is to filter the associated CM current of fast switching before it goes through the gate driver. Therefore, based on the measured CM current (Fig. 4.28 and Fig.4.29), a CM inductor is implemented in the gate driver



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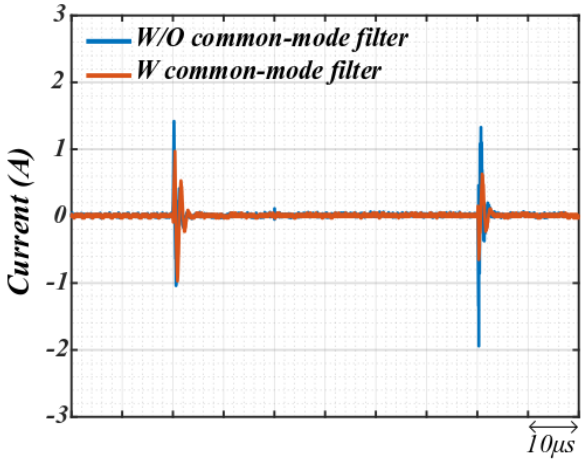

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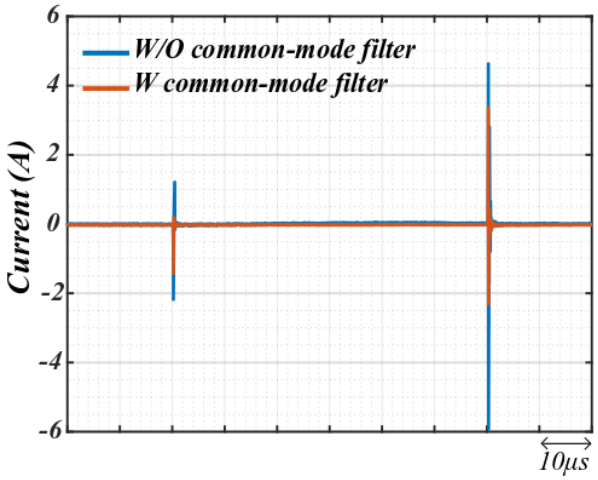
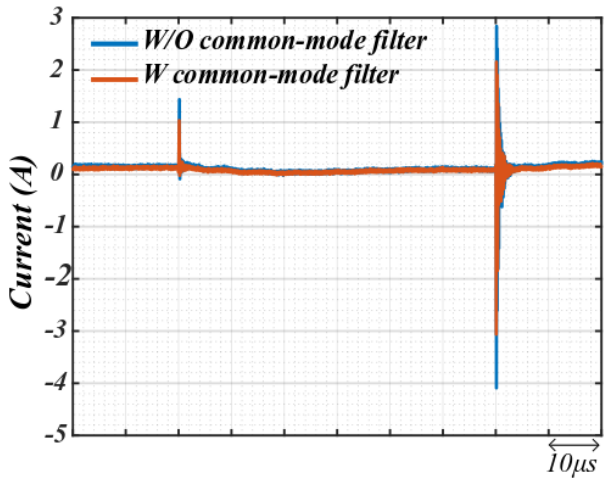


(c)

Figure 4.28 – Experimental comparison of ICM between the gate driver without (W/O) CM choke and the gate driver with (W) CM choke, Double pulse test, 1200 V, +150 A (a) ICMH (b) ICML (c) ICM-input.



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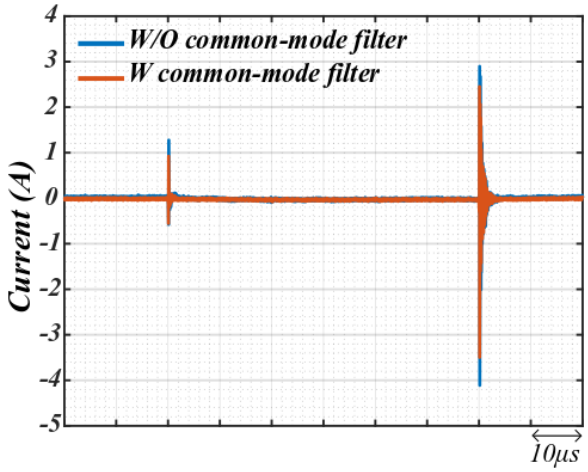

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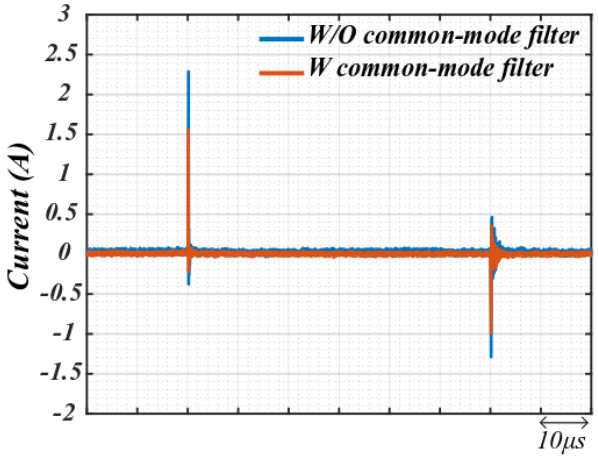


(c)

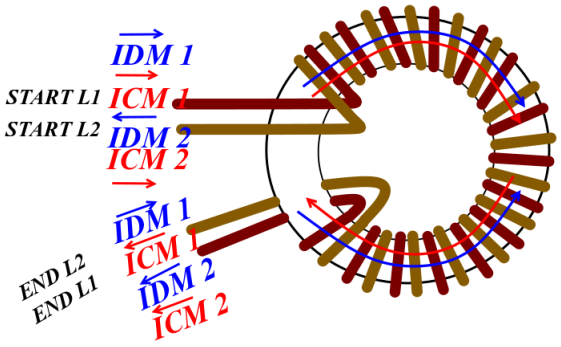
Figure 4.29 – Experimental comparison of ICM between the gate driver without (W/O) CM choke and the gate driver with (W) CM choke, Double pulse test, 1200 V, -150 A (a) ICMH (b) ICML (c) ICM-input.

circuit to attenuate the 500mA/ μs CM current generated by the voltage variation (30kV/μs) across the input capacitance of the device (see Eq.4.8).

$$\Delta V = L\frac{\Delta I}{\Delta t} \tag{4.8}$$

Looking into the equivalent model of the CM filter (see Fig.4.27 [146]), apart from the CM inductor, there are parasitic elements which can affect the gate-source signal.

Considering the equation 4.4, the chosen filter should have a low impedance for differential mode (DM) ($L_{\_P1}$ and $L_{\_P2}$ in figure 4.27) so as not to affect the behaviour of the gate drive signal during turn-on and turn-off but it should have a big impedance in CM to block the high frequency induced current to the gate and protect the gate driver against voltage perturbation [30].



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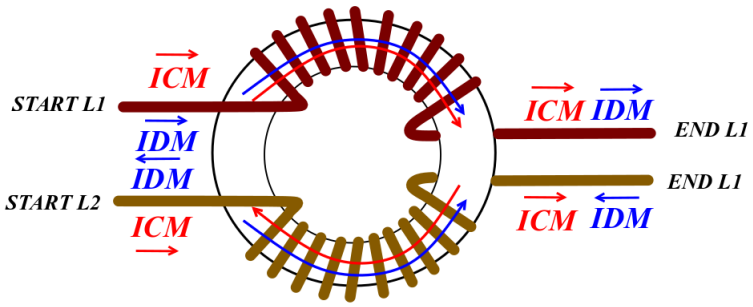


(b)

Figure 4.30 – CM inductor (a) Bifilar winding (b) Sectional winding.

There are two types of windings for CM chokes: sectional and bifilar (see Fig. 4.30). The sectional components has a higher leakage inductance (DM inductor at low frequency) since there is more insulation barrier (core) between the windings, while the CM function of the two coils is the same (see Fig. 4.32). Therefore, in order to have minimum impact on the switching speed and gate oscillation, a bifilar choke (one-way winding) is used.

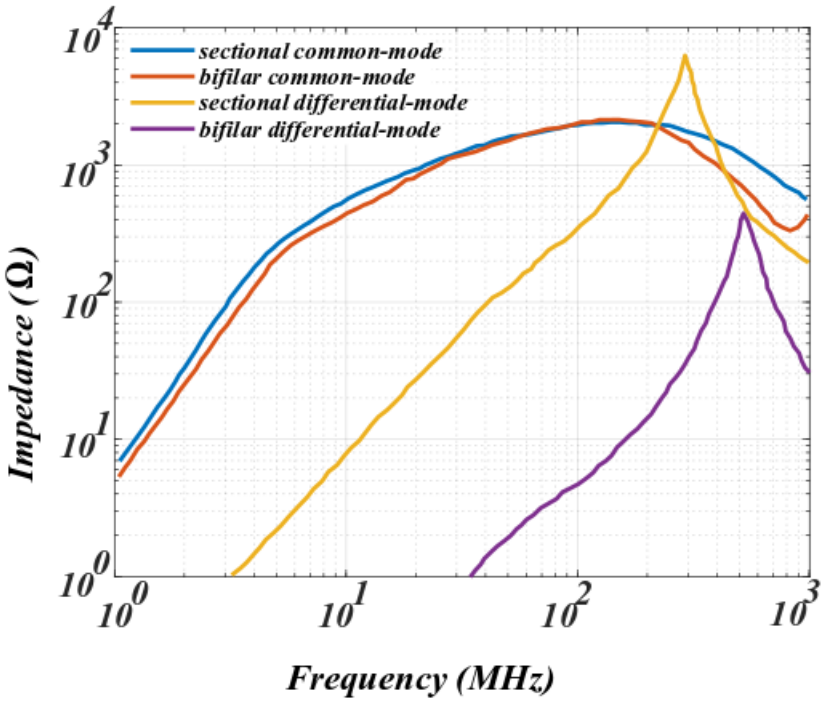


Figure 4.31 – Impedance comparison.

To attenuate ICML and ICMH, several CM chokes have been selected to have the least possible effect in gate-source waveform over-voltage and oscillation. The chosen bifilar 11 μH CM choke with ring core and the core materials of MnZn has been compared in terms of impedance in different modes (see Fig. 4.32).

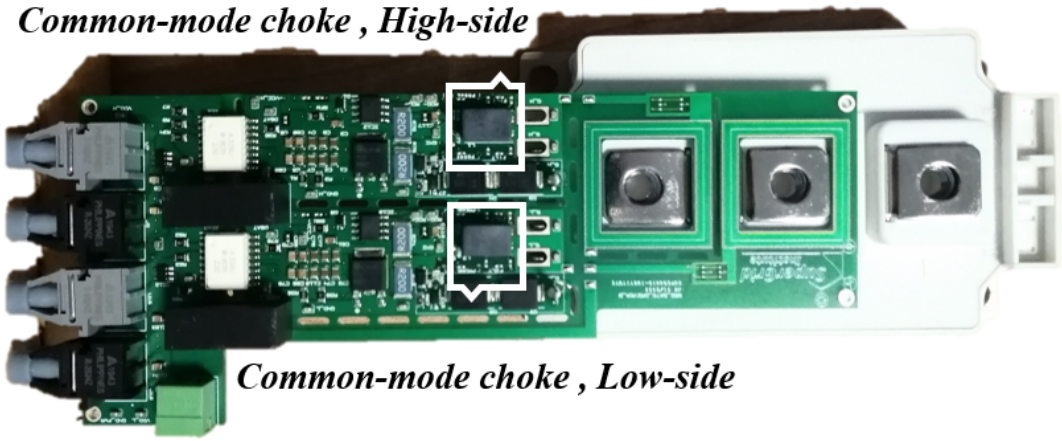
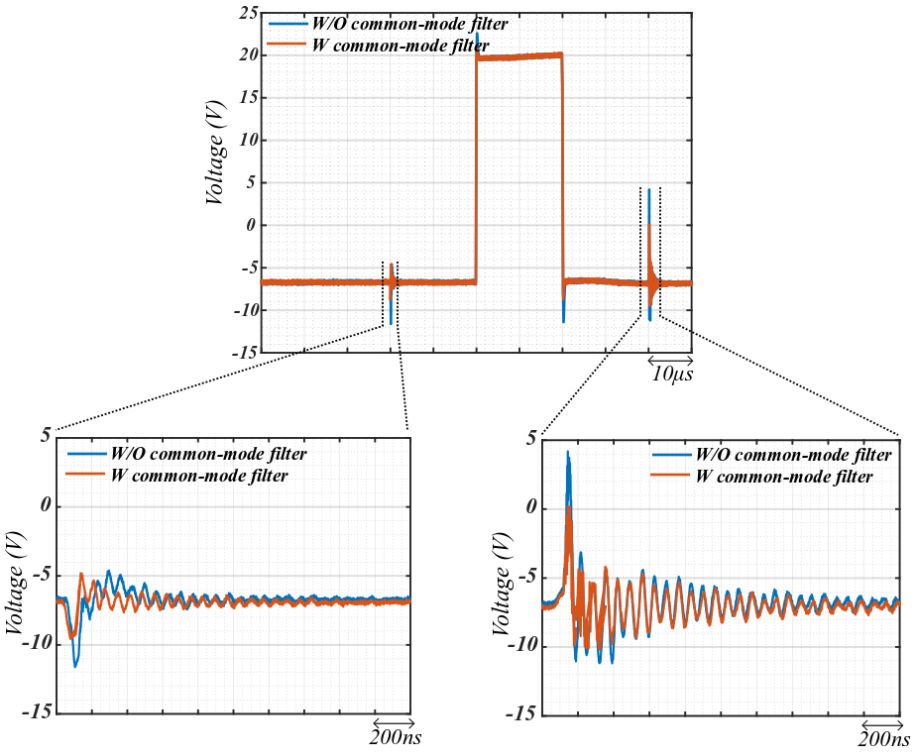


Figure 4.32 – Embedded CM choke in gate drive prototype.

Experimental results (see figure 4.33) confirm that, by choosing bifilar winding chokes it is possible to keep the parasitic voltage lower than the threshold voltage of the device under test.

The Vgs waveforms of the synchronous switches embedding the proposed method has been measured in double pulse test in both directions of the current



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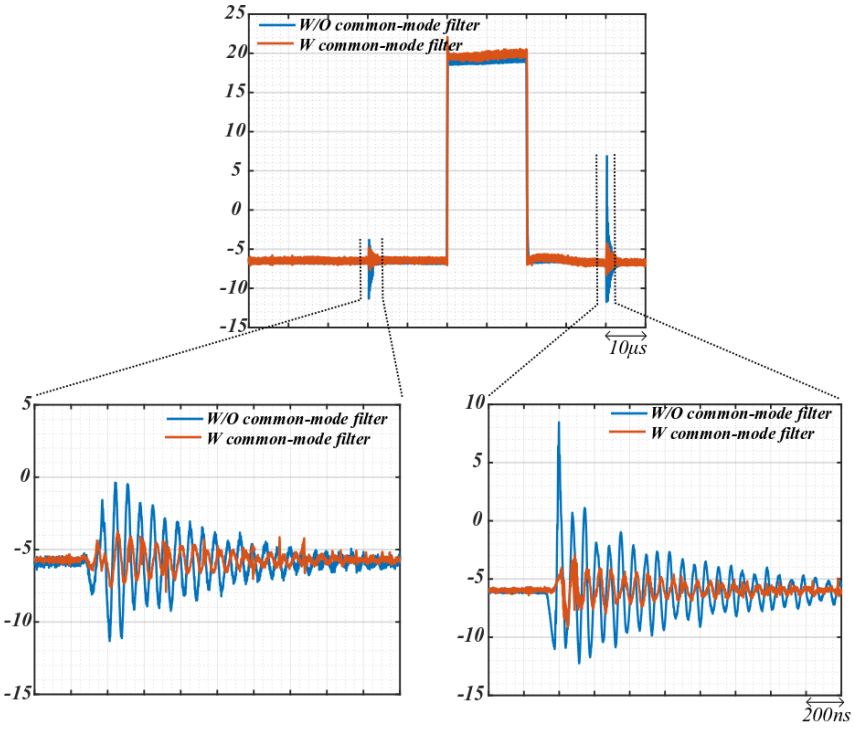
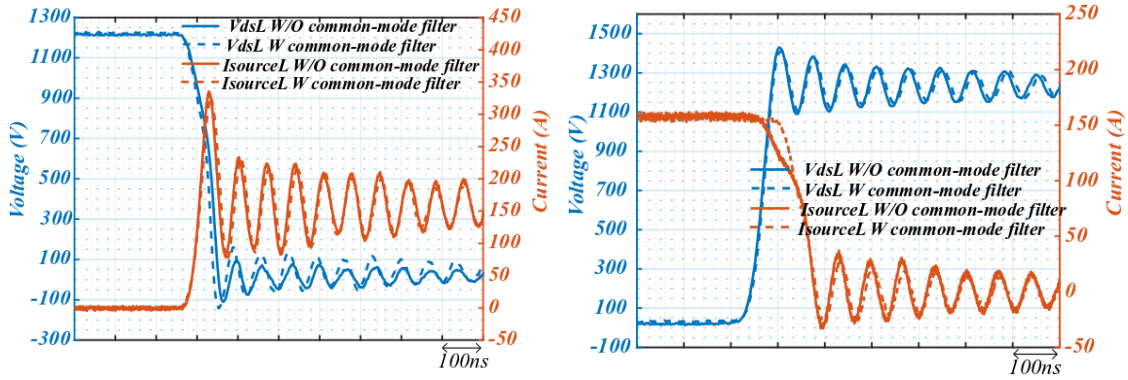


(b)

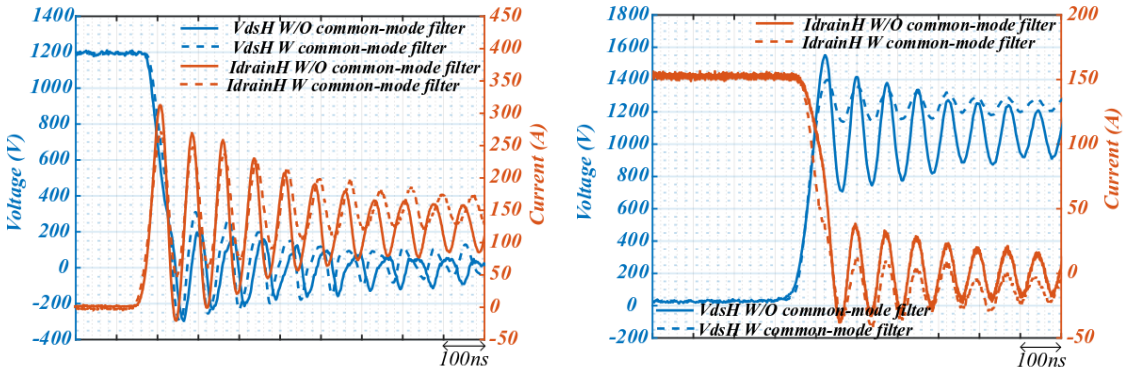
Figure 4.33 – Vgs comparison between the gate driver without (W/O) integrated CM choke and the gate driver with (W) integrated CM choke, Double pulse test in 1200 V(a) VgsH at +150 A (b) VgsL at -150 A



(a) (b)

Figure 4.34 – Vds and Is comparison between the gate driver without (W/O) integrated CM choke and the gate driver with (W) integrated CM choke, Double pulse test in 1200 V, +150 A (a) VdsL Vs. IdsL turn-on transition (b) VdsL Vs with Ids turn-off transition.

in the inductor. As it has been shown in figure 4.33, the proposed method can reduce the gate perturbation to a value lower than the threshold voltage of the SiC MOSFET (which equals to 2.5 V) even with a high DC voltage (1200 V).



(a) (b)

Figure 4.35 – Vds and Id comparison between the gate driver without (W/O) integrated CM choke and the gate driver with (W) integrated CM choke, -150 A (a) VdsH with IdH turn-on transition (b) VdsH Vs. IdsH turn-off transition.

The switching voltage and current have been measured before and after implementing the CM inductor. Comparison of the switching waveforms in figures 4.34 and 4.35 prove that the switching losses will not be affected by the added component since the voltage and current slopes have not been changed. Implementing the CM choke reduces the magnitude of the CM current high-side and low-side (see figures 4.28 and 4.29). By implementing the CM inductor, input CM current has been reduced by up to 20% without increasing the losses. The input CM current reduction coming from the blocked CM current generated across each switch in half-bridge.

4.7 Conclusion

In this chapter, the self-disturbance phenomena in phase-leg configuration with IGBTs and SiC MOSFETs have been compared on a double-pulse test bench. The experimental results showed the severity of the problem with SiC MOSFETs compared to IGBTs due to the higher switching speed ability of the SiC MOSFET and different characteristics of IGBT compared to MOSFET. Moreover, the more negative allowable bias of the IGBT reduces the risk of self-disturbance phenomenon. Therefore, one of the first requirements of the SiC MOSFET gate driver has been recognised. To overcome the complementary switching effect, the Miller-clamp protection circuit has been implemented considering that keeping the switching speed is a priority. The conventional active Miller-clamp protection has been tested with different DC voltage levels to show the effectiveness of the protection circuit. The experimental results revealed that, in order to use the potential ability of fast high power SiC MOSFET device, there is a need for another solution. A new method has been proposed to overcome the parasitic gate perturbation and take advantage of high speed high voltage SiC MOSFET. The CM current generated by fast switching has been measured and it has been proposed to block this CM current before it goes to the gate. By choosing a bifilar choke, it is possible to block the associated current and reduce the gate-voltage perturbation. The proposed solution has been validated under experimental condition of 1200V, 150A switching transition. The advantage of the new method is the significant reduction of the input CM current of the gate driver without reducing the switching speed.

In addition, the importance of the measurement accuracy has been discussed precisely due to significant effect of Vgs correct waveform on converter efficiency and stability based on the gate driver design. In circuits such as a half-bridge, where large CM voltages and fast edge rates occur, small amplitude signals such as the Vgs signals are very difficult to be measured accurately without superior CM rejection ratio. Due to the parasitic elements of the conventional differential probe, there is a risk of measurement errors and also unexpected loading of the circuit under test in fast switching power electronic converters. High input impedance and low parasitic capacitance of the isolated probes are important parameters for high voltage phase-leg configuration measurement specification. New technology of differential isolated probe provides this characteristic. Measuring the common-mode current of the gate driver validated the necessity of using the new optical differential measurement technology of the differential measurement equipment.

5

New approach for EMI reduction by means of gate driver

5.1 Introduction

As it has been shown in previous chapters, the switching transients of the semiconductors are the source of EMI in power converters. One of the solution that can be applied to control the EMI is an individual switching trajectory modification. Gate drivers are considered as an interface between control signal and switching. Therefore, in order to control the EMI, during switching, gate drivers can act to reduce the generated EMI by changing the current and voltage across the switches. Many researches have been done in this domain in order to control the current and voltage variation across the switch by gate-source signal modification. The switching trajectory modification to deal with EMI issue of the power converter can be classified into two main groups: conventional passive approach and new active control method. In this chapter, the main ideas and operational principles of the passive and active methods are discussed in section 5.2.1 and 5.2.2. After highlighting the advantage and drawbacks of these methods, the new approach of inductive boost gate driver will be discussed in section 5.2.3 which figured the main idea of the proposed gate driver in this work. The new gate driver with inductive feedback

will be presented in section 5.3. After underlining the principles and design process of the new proposed gate driver, the new gate driver prototype will be validated experimentally in this section. The section 5.4 is the conclusion of this chapter.

5.2 State of the art: EMI reduction by means of gate driver

5.2.1 Conventional passive approach to deal with EMI by means of gate driver

The passive methods are the non-modified methods during switching transition in which the output stage of the gate driver is predefined (in design stage) and can not change during the switching trajectory. The two well-known main approaches among passive methods to reduce the EMI are gate driver with high adjusted gate resistance and Resonant Gate Driver (RGD). Gate driver with big gate resistance damps the switching oscillations and slows down the switching speed. RGD affects the switching speed by changing the charging and discharging of the parasitic capacitance of the semiconductors.

5.2.1.1 Increasing the gate resistance

Increasing the gate resistance is the conventional approach to reduce voltage/current spikes by prolonging charging and discharging time of the capacitors C_{gs} and C_{dg} [132, 158]. It is widely known that the gate resistor values of the power semiconductors can control the switching losses behaviour and the oscillation. However, a trade-off between these two parameters is required since increasing the R_g causes a dramatic increase of switching losses. It seems to be the simplest solution and easiest to implement, but recent works which will be presented in section 5.2.2 have shown that acting on different switching steps to reduce the EMI leads to a better trade-off with losses than increasing gate resistance.

5.2.1.2 Resonance Gate Driver (RGD)

The main goal of the RGD is to reduce the power losses in the gate driver circuit. This technique acts on recovering the energy stored in the input capacitance (C_{iss}) of the power module [10, 38, 43, 53, 75, 104]. The charging and discharging times of the input capacitance thanks to an inductor can be modified which reduces the switching speed and consequently reduces the EMI of the gate

driver. In the literature, two types of "constant current gate driver" [43] and "resonant current gate driver" have been reported [38]. The structure of the current gate driver consists of four switches (normally off MOSFETs) in the gate driver. Controlling the gate current with four switches adds complexity to the control circuit [42]. Moreover, this structure does not allow to control the gate source voltage between positive and negative gate bias which is vital in high voltage fast SiC MOSFET gate drivers (self-disturbance phenomena explained in chapter 4). The main problem is the pre-charge of the passive components in gate driver circuit which could affect the whole performance of the SiC MOSFET [43].

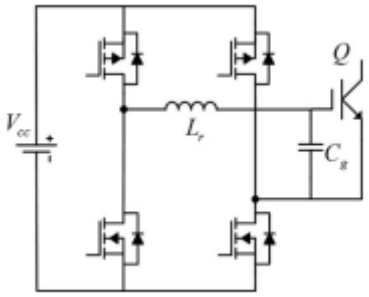


Figure 5.1 – Resonant current gate-driver circuit [42].

Above presented RGD circuits are designed only for specific applications and sometimes may not operate for others. As instance, a certain design approach must be taken into account for a synchronous buck converter circuit since the circuit has two devices that are switching (half-bridge device). Proposed gate drivers in [186] and [174] are dual channel isolated RGD solution suitable for the DC-DC converter which recovers the energy of gate with better efficiency compared to a conventional resonant gate drive. It can drive two MOSFETs as a dual channel driver and has ability for negative gate voltage which avoids self-disturbance. However, in those drivers like the others reported in [10, 53, 75, 104], the gate voltage rise time is considerably slowed down at the very beginning of the transition due to current source gate drive. It is not a relevant solution for present study because, the main aim of the present work is to benefit from the fast switching speed of SiC MOSFET.

These drivers are simple solutions and low cost but they have a fixed profile and the variable parameters are limited. These specifications do not meet the requirements of this research work. Providing the rush-current at the beginning of the switching transition by means of RGD is difficult to achieve. That is why, the push-pull gate driver which provides enough current for fast SiC MOSFET switching transition has been chosen.

5.2.2 Active Gate Driver (AGD) to deal with EMI by means of gate driver

Active Gate Drivers (AGD) have been introduced mostly to control the switching transition of the Si IGBTs [101, 103]. AGD may be adapted to control the switching transition of SiC MOSFETs. AGD techniques control the switching by driving the gate circuit of the MOSFET/IGBT and consequently does not require any modification in the original topology of power converter neither in using passive nor active devices. The AGD is applied on the control signals and consequently in gate driver. The principle is to change the slope profile of the gate source voltage. Reported researches on AGDs classified them in three groups: gate voltage control, gate current control, gate resistance control while there are some AGDs which implement both current and voltage controls [102].

5.2.2.1 Open-loop concepts

The open-loop gate drivers have been developed to control different phases of the switching transition. The main principle of this method is to act on current rising/falling and voltage rising/falling subdivisions of the switching transition without any dynamic feedback to the controller of the gate driver. To achieve this, it is needed to act on the gate voltage or gate current in those specific periods to modify the switching waveforms (Fig. 5.2).

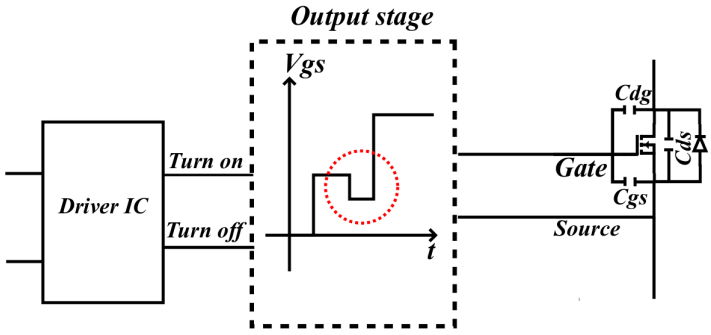


Figure 5.2 – Open-loop concept gate driver.

The method has been presented mostly for IGBT gate driver for example [69, 72, 96, 108, 142, 164] and also for a FPGA controled IGBT gate-driver [142]. However, the approach is not able to satisfactorily compensate the non-linearities of the IGBTs and the variation of the operating point towards temperature as it has been reported in [100]. Among the open-loop methods, only the switch-able gate

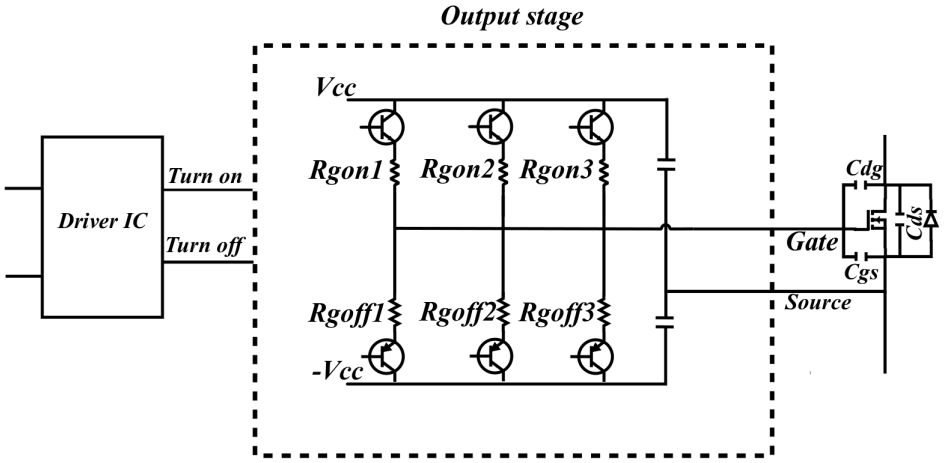


Figure 5.3 – Gate driver with open-loop control and discrete gate resistance.

resistance for controlling the gate current, has been implemented on chip level SiC MOSFET [167] (see Fig. 5.3).

The main idea of this approach is to decrease the energy of gate as it has been explained, during the Miller-plateau of the SiC MOSFET switching trajectory, where the overshoot of the current and voltages occurs (see Fig. 5.4). The considerable delay in turn-off transition of this method, is the main drawback of this open-loop gate driver [167].

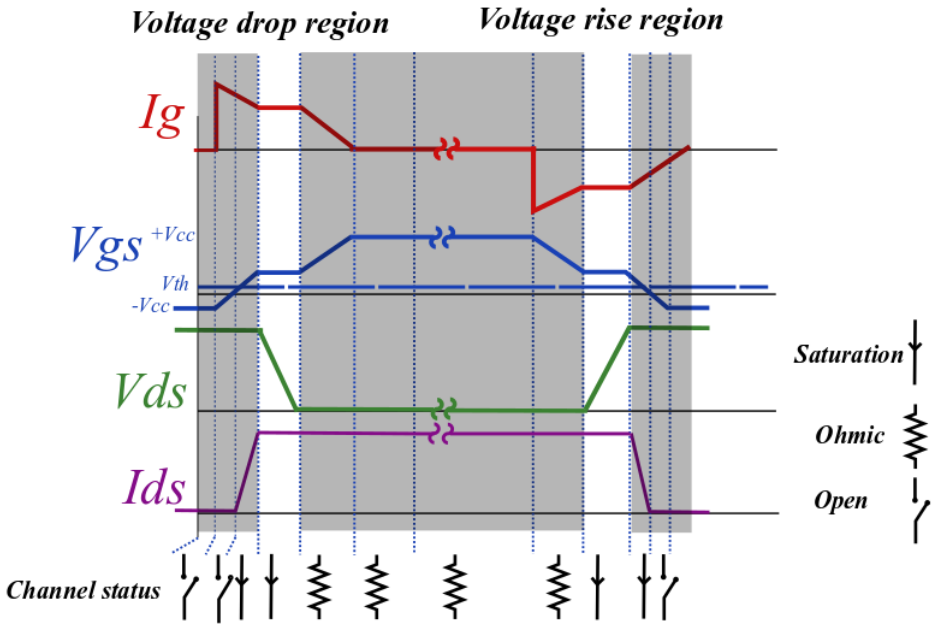


Figure 5.4 – Miller-plateau regions in MOSFET switching transition.

Different switching characteristics of IGBT compared to SiC MOSFET switching such as tail current, different voltage/current fall/rise time prevent from achieving a fair trade-off between EMI and losses with open-loop gate driver for SiC MOSFET.

Moreover, in all above mentioned open-loop gate drivers, the proposed method has not been practised yet using high voltage/high current SiC MOSFET power module. The proposed gate drivers used for IGBT power modules have been limited to specific $\frac{di}{dt}$ and $\frac{dv}{dt}$ range.

5.2.2.2 Closed-loop concepts based on voltage or current monitoring

Unlike open-loop gate driver, the closed loop gate driver is defined based on the monitoring of different phases of the switching transition and then act during the corresponding time interval. A dynamic feedback to the controller of the gate driver is an essential element in this type of driving.

It can be split into analogue feedback control [122, 163] and digital (e.g. FPGA based controller) close-loop controller [67, 83]. These methods needs to generate the current or voltage reference to be compared with the sensed voltage and current of the switch. This adds difficulty and complexity to the circuit of the gate driver. The generated delay, due to comparison of the reference voltage/current with the captured voltage/current of the switch is not negligible in fast switching (in order of tens of nanoseconds (ns)). However, all the proposed gate drivers for IGBTs struggled with this unwanted delay. So as the combination of the voltage and current control has been done only in digital gate driver due to complexity of the reference generation and comparison at the same time in analogue circuit ([101] see Fig. 5.5).

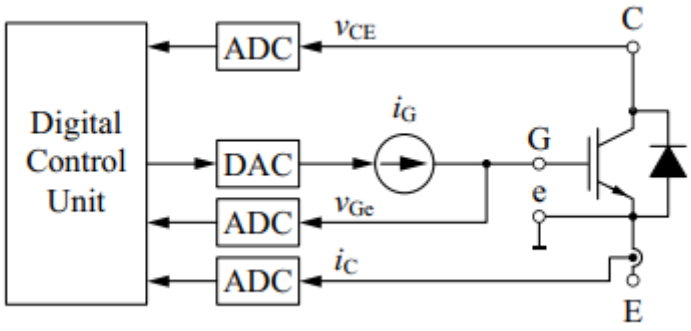


Figure 5.5 – Digital gate driver unit with Analogue to Digital converters (ADC) for measuring current and voltage of device and Digital to Analogue converters (DAC) for controlling the gate current [101].

A new closed loop feedback gate driver has been proposed for SiC MOSFET [22, 123, 125]. By means of two independent comparators, the gate-source voltage is compared to four reference voltages. Due to fast switching of the SiC MOSFET, a delay compensator has been implemented in the circuits (see Fig. 5.6)

The complexity of the system consists in current sensor, generating four references and the control of switching of different gate resistances (S1 and S2 in

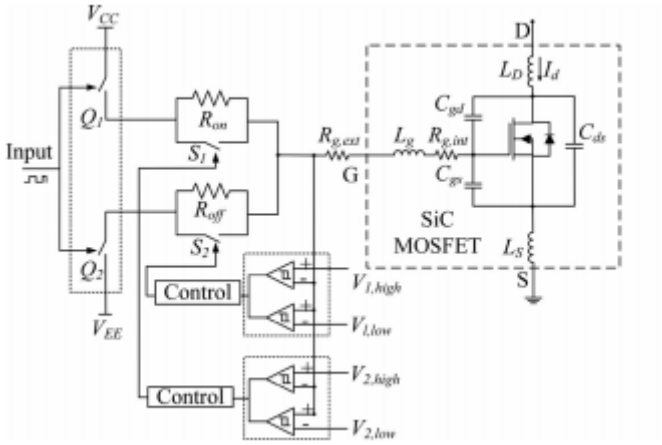


Figure 5.6 – Schematic of Closed-loop SiC MOSFET gate driver [123].

figure 5.6). Although the presented gate driver resulted in a good trade-off between losses and EMI but it has not been tested using high voltage/current power module. The experimental results are limited to chip level SiC MOSFET. Therefore, the current level required to turn-on of the device will be problematic concerning the proposed gate driver in this work.

Another closed-loop gate driver for SiC MOSFET has been presented in [130, 152]. The proposed gate driver (see Fig. 5.7) successfully regulates the turn-on voltage and current slope thanks to a voltage reference generator.

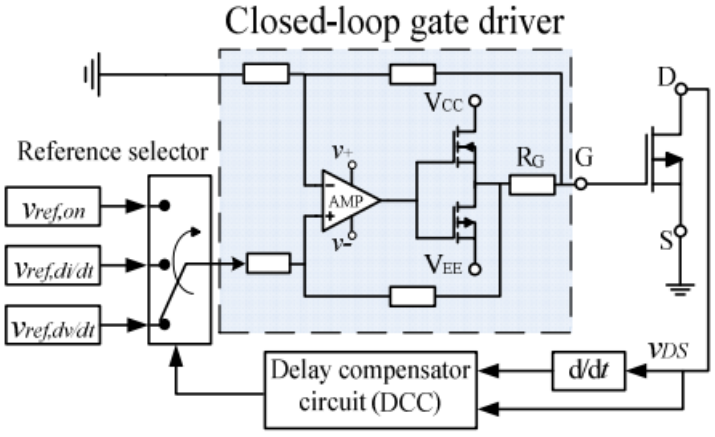


Figure 5.7 – Block diagram of the proposed control schematic [130].

Like [123] this closed loop also suffers from the added delay to switching trajectory which has been partially solved using a compensator circuit. Although the work has presented a voltage overshoot and a current overshoot control, it has been stated in [130] that the combination of two controls cannot be implemented for SiC MOSFET. It is because feed-back loop delay cannot be neglected in comparison with the total transition of the SiC MOSFET. However, the proposed analogue

closed-loop control has not been validated at high switching speed and the drain current is limited to 24A in a chip-level SiC MOSFET.

5.2.2.3 Digital sequential closed-loop concepts with negative gate current

An adaptive iterative closed-loop control has been reported in [23, 24] called Negative Gate Current (NGC) approach and it has been validated experimentally for 1200V, 200A IGBT module (Fig. 5.8).

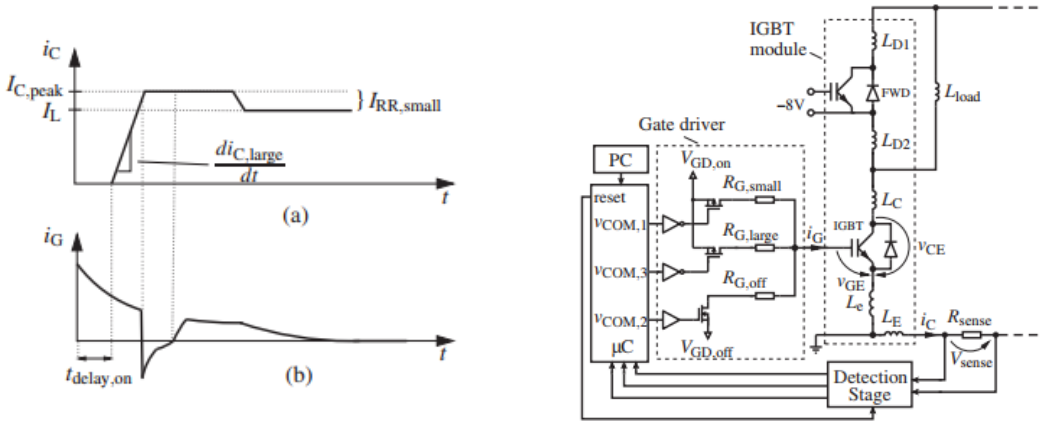


Figure 5.8 – Negative Gate Current closed-loop approach (a) main principal (b) control schematic [24].

A detection circuit has been implemented to measure the slope and peak current, in each turn-on process of the device. This information is fed to the micro-controller to provide signals called V_{com} to activate suitable gate resistance. The duration of the V_{com} signals, figures out the negative current duration (see Fig. 5.8.a). The detection block and control circuit presented in this work are complicated. Like previous presented works, the control has not been applied to SiC MOSFET. Due to imposed delay generated by closed loop, the controller is digital. Considering the Miller-plateau region, where the control acts, knowing that this region is shorter in SiC MOSFET characteristics, then the control can impose a considerable delay to the switching trajectory of the SiC MOSFET. Moreover, SiC MOSFET compared to IGBT needs more current to pass from saturation to ohmic region. It makes it even more difficult to provide a negative current during Miller-plateau.

5.2.3 Inductive gate driver

5.2.3.1 Coupling between switching loop and power loop

Inductive feedback gate driver, is a new gate drive method which has not been the subject of profound discussion for SiC MOSFET power module yet. The principal theory of this method is based on the effect of the mutual inductance between the switching loop (gate-loop) and power loop.

In general, the magnetic couplings between the different interconnections and different elements of the converter are represented by Mutual inductances in addition to usual parasitic elements (R,L,C) [5]. Normally power converter circuits consist of two major parts. The lower level voltage part (including gate drivers and control) and higher level power circuit part (see Fig. 5.9, Mutual inductance are shown in dashed lines).

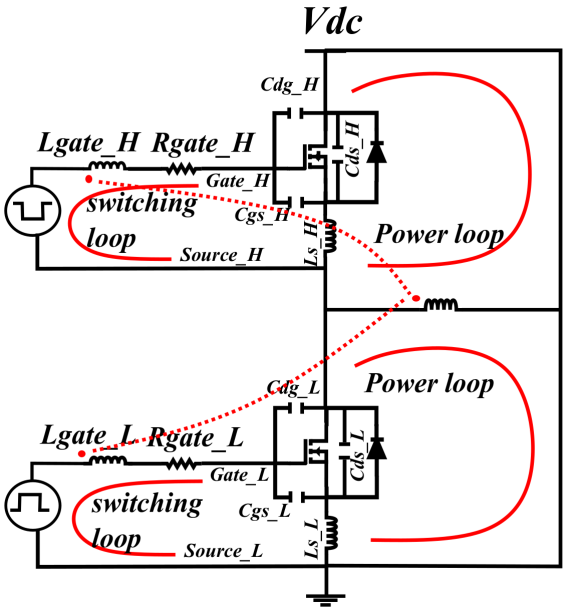


Figure 5.9 – Switching loop and power loop in a half-bridge device.

In the layout of the converter, the low voltage level is in the vicinity of the high power loop. Many works have discussed the inductance of the power loop [7, 27, 31, 155]. The vicinity of the switching loop and power loop like any other electronic circuit leads to a mutual inductance between the two loops (see Fig.5.9) which will affect the switching characteristics directly [106]. The information on the parasitic elements of the device under test and the power loop can help to understand the mutual inductance between switching loop and power loop. Reference [119] investigates the influence of the mutual inductance between the gate drive loop and power loop. In this work, besides converter layout, the effect of coupling between control

loop and power loop in voltage and current overshoot has been discussed precisely. The parametric study presented in this work has shown that a negative coupling leads to a reasonable trade-off between losses and EMI because it decreases the current and voltage overshoot.

The objective in this work is not to calculate the mutual inductance between the parasitic elements but to show how this coupling (here the mutual inductance is a tool to model the coupling) can be used to reduce the EMI of the converter.

5.2.3.2 Inductive boost gate driver

In [44–46, 169] the coupling between switching loop and power loop has been made and used in gate driver design to boost the gate current and modify the switching behaviour (see Fig. 5.10).

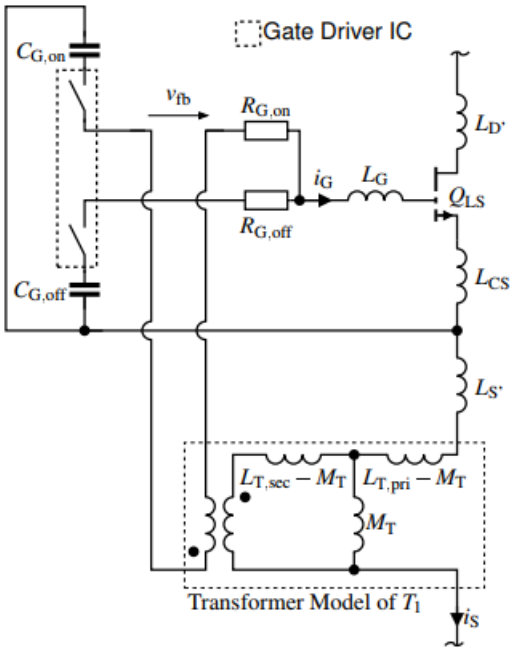


Figure 5.10 – Inductive boost gate driver approach schematic [44].

In the proposed gate driver in [44–46, 169], only a current transformer is added to the circuit of the buck converter to transfer energy between the power path to the gate path while all the classical design of the gate driver remains without modification. The proposed gate driver benefits from simpler design compared to the gate drivers described in section 5.2.2. The experimental results illustrated in [44–46] have shown that the transformer coupling could compensate the influence of the added parasitic elements to the gate which might change the switching behaviour. Experimental results obtained with several switches with different characteristics

showed that this method can be applied for different kinds of switches including chip level GaN and SiC MOSFET.

5.3 Proposed inductive feedback gate driver for EMI reduction

Conventional methods of increasing gate resistance or using resonant circuits work to limit overshoots but have not been reported as a good trade-off between losses and EMI.

In case of open-loop discrete resistance control, changing the gate resistance seems to be effective. However, this method has the lack of adjustment of $\frac{di}{dt}$ and $\frac{dv}{dt}$ in different operating conditions. It is because various discrete resistance values should be used with various switches which makes it difficult to change from one application to another.

Closed-loop control of $\frac{di}{dt}$ and $\frac{dv}{dt}$ of the switch at the same time -which can prevent losses to increase- has not been applied in SiC MOSFET power module due to the significant delay generated by the control loop. Moreover, sensing fast rise/fall time adds another challenge for this concept of gate driver. The needed bandwidths of the embedded sensors are difficult to achieve.

The presented methods in sections 5.2.1, 5.2.2 and 5.2.3.2, are mostly applied for a chip level semiconductor. Moreover, they have presented experiemental results based on clamp inductive circuit. This configuration, does not allow to characterise the half-bridge configuration. Consequently, there is no information provided for soft switching condition.

The inductive feedback gate driver does not create a delay during switching modification. Implementing this method for a power module is a challenge. The feedback will be inserted between the gate driver and power module where the practical implementation is unknown yet. Therefore it gives a great motivation to study the inductive feedback gate driver for a half-bridge module in this work. The main advantage is the simplicity of this natural feedback. There is no need of control modification. This method can be applied to many power modules despite the device characteristics.

5.3.1 Operation principles and circuit configuration

Taking into account the previous review, if the gate current is reduced during the time interval where the current/voltage overshoot of switch happens, it can reduce

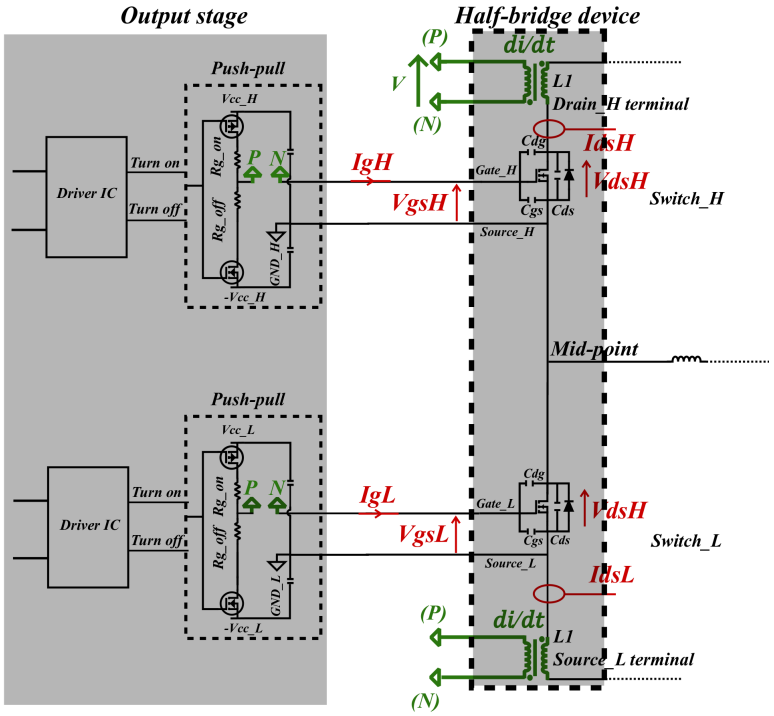


Figure 5.11 – Inductive feedback gate driver.

consequently the EMI issue. The gate driver presented in section 5.2.3.2 showed that, increasing the gate current during this period thanks to positive mutual inductance can boost the turn-on transition of the switch. On the other hand, the presented result in [35, 119] reported that indirect coupling (negative mutual inductance) between the switching loop and power loop during current/voltage rise/fall time, can moderate the switching slope and consequently the current/voltage overshoot of the switch. In this work, based on the mutual inductance theory, a simple and easy implementation natural feedback to the gate circuit thanks to a coupling between power loop and switching loop has been proposed to reduce the gate current. The positive mutual inductance relates to the fact, that increasing current slopes, creates positive voltage and vice versa.

In half-bridge configuration, there is only one switch which is controlled (hard switching). So the switching characteristic of the complementary switch (soft switching), is the projection of the switch in hard switching. The feedback can reshape the switching voltage and current signals in hard switching condition (gate-source voltage and current is changing in the same subdivision). This leads to reshape the voltage and current transition of the complementary switch (soft switching condition).

The goal is to keep the conventional circuit of the gate driver and to integrate only a simple feedback to the gate driver circuit (see Fig.5.11). This feedback should

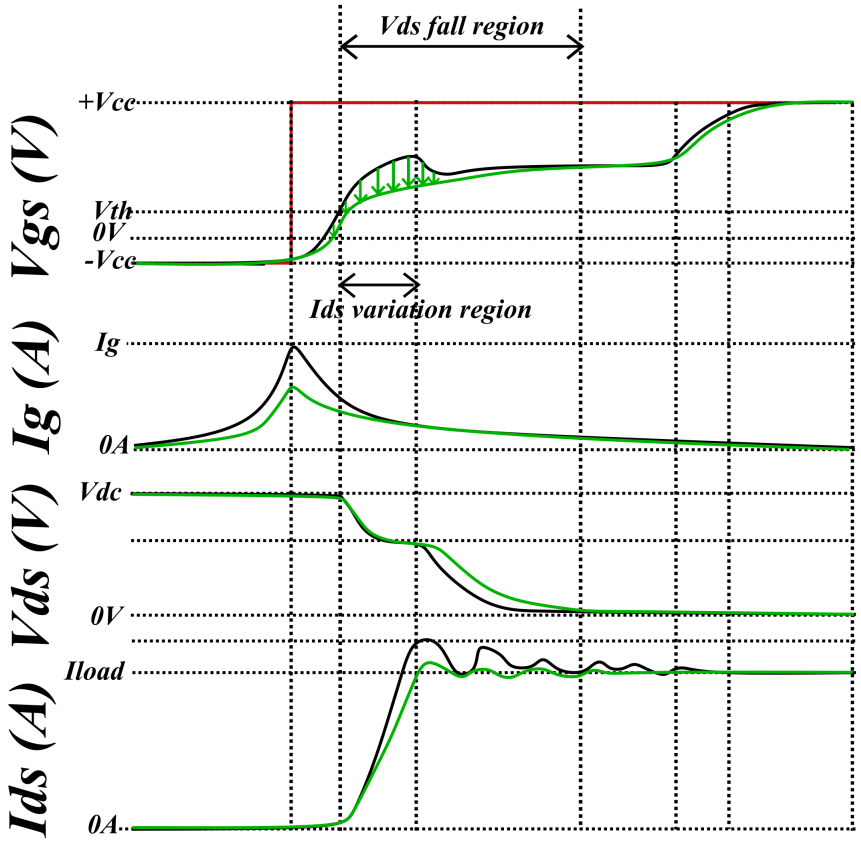


Figure 5.12 – Inductive feedback gate driver, turn-on transition (proposed method modification in green).

reduces the gate current based on switching characteristics. To apply this method, there should be a gate driver feature able to change the gate current. This concept could be realized by sensing the current variation across the switch and inject a voltage based on current variation to the gate. This voltage can reduce the gate energy and gate current similar to [44–46]. In addition, the design should consider the specification of a SiC MOSFET power module gate-driver also. Another constraint is that the feedback should not add any delay on the switching transition. So as, all these gate current modifications should be made during switching transition of $\frac{di}{dt}$.

It means that faster $\frac{di}{dt}$ (more voltage and current oscillation) needs more reduction of gate energy and vice versa. This feedback can be undertaken by means of a rogowski coil which senses the current and creates a voltage due to current variation of the switch in real time switching transition (see Fig.5.11). Then the created voltage can be embedded into the gate driver to alter the gate-source voltage of the device (Fig. 5.12 and Fig. 5.13).

The operation of the proposed gate driver is shown in figures 5.12 and 5.13. In turn-on transition, the current variation creates positive voltage which thanks to

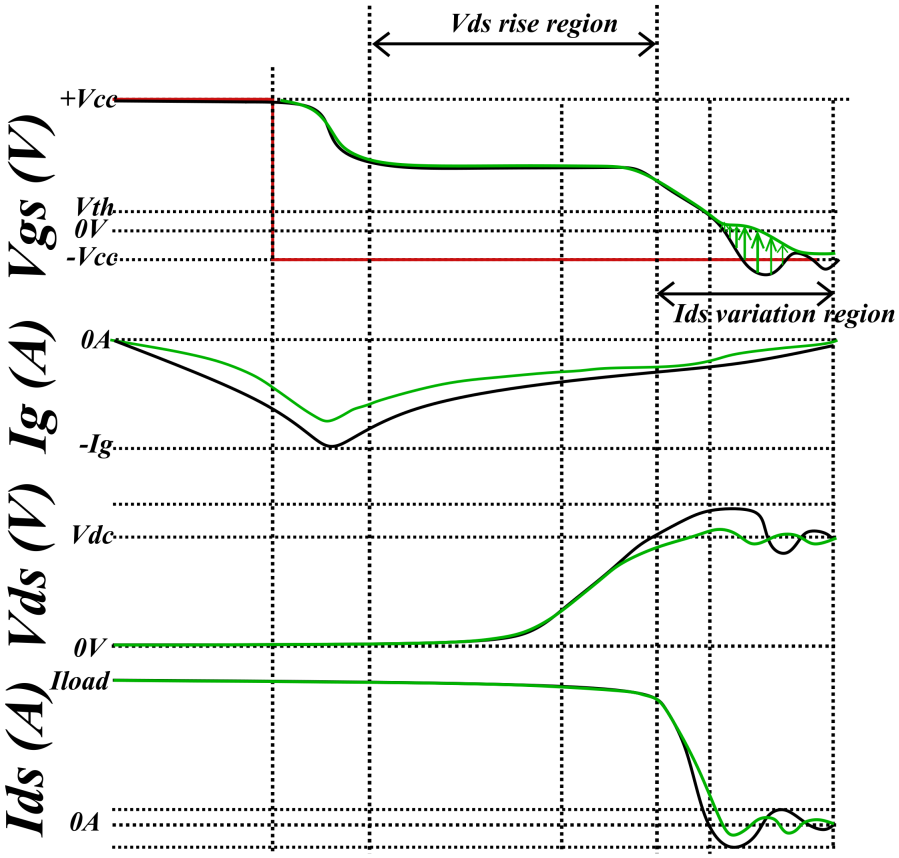


Figure 5.13 – Inductive feedback gate driver, turn-off transition (proposed method modification in green).

PCB design will be inverted before being implemented to the gate circuit. The added voltage will decrease the level of the gate current and consequently moderate the switching slopes and reduces the oscillation since $\frac{di}{dt}$ and $\frac{dv}{dt}$ decreased (see Fig. 5.12). On the opposite side, during turn-off, decreasing $\frac{di}{dt}$ creates a negative voltage which is injected as a positive voltage to the gate so as to reduce the level of the gate current and switching slope (see Fig. 5.13).

5.3.2 Rogowski coil design and specification

As it has been explained in section 5.3.1, the negative voltage to reduce the gate current can be provided by a rogowski coil which senses the current variation and creates a voltage. To implement the rogowski coil to the gate driver design, the challenge is the physical implementation and minimization of parasitic elements due to the installation of the coil into gate driver circuit.

This concept has been realized by a careful design of a core-less PCB rogowski coil [4, 187]. Similar core-less PCB coils have been used as a direct current measure-

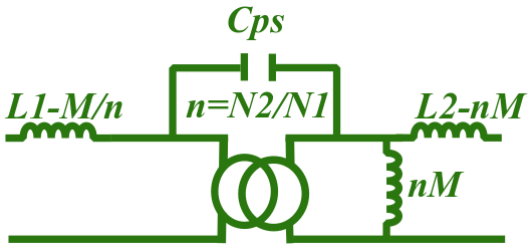


Figure 5.14 – Equivalent circuit of a rogowski coil.

ment technique as reported in [110, 151, 160, 161] for fast short-circuit protection of power semiconductors.

Figure 5.15 – Device under test terminals, 1.7 kV SiC MOSFET power module [168].

The classical equivalent circuit model of the rogowski coil (see Fig. 5.14), consists of two inductors L_1 and L_2. The primary side L_1 corresponds to the terminal of the device under test (see Fig.5.15). Since it is planned to integrate the coil on the top of the device, for the primary side L_1, only the value of the terminal inductance is considered. Moreover, like this, there is no added parasitic component to the power loop due to the integration of the rogowski coil to the power circuit. Compared to the power loop circuit parasitic inductance (physical connection of the device into layout of the converter), the impedance of the terminal of the device is very small (about 10nH).

The secondary side L_2 will be placed in the gate path. The critical point in integrating the rogowski coil to gate driver is the added parasitic inductance ($L_2 - nM$). It can be optimized by proper design of the rogowski coil providing enough

(a) (b)

Figure 5.16 – Different winding of PCB rogowski coil (a) With return-wire winding (b) Bifilar winding [62].

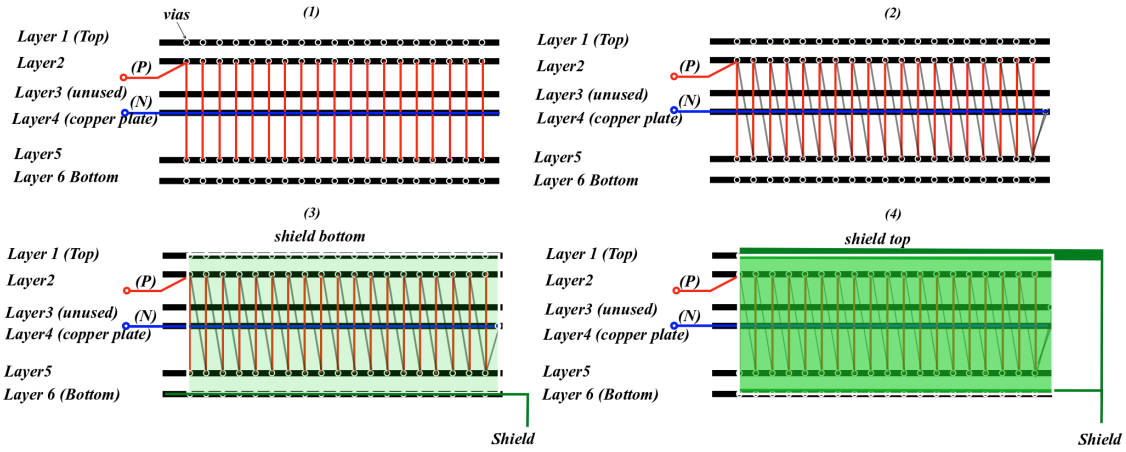
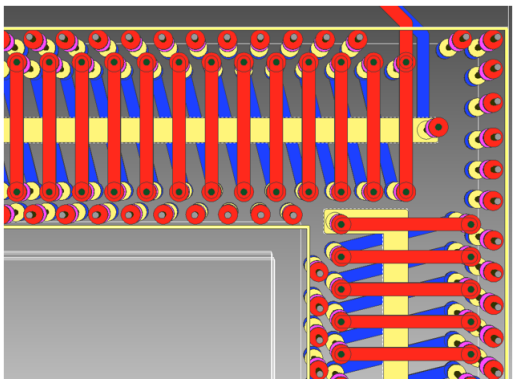


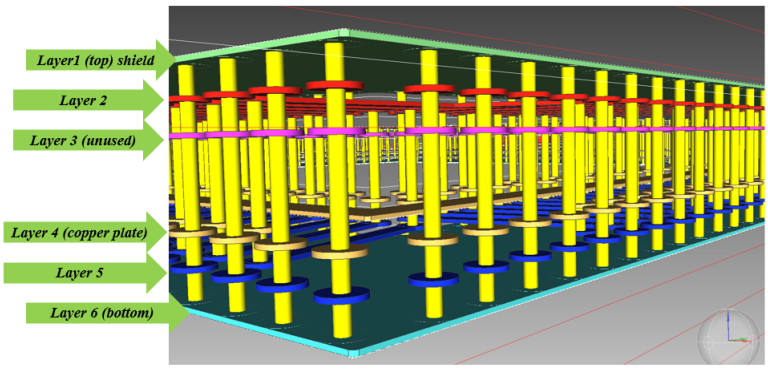
Figure 5.17 – PCB rogowski winding process.

coupling between primary and secondary coils (M) and a proper type of winding. To do so, based on previous researches on core-less rogowski coils [57, 62, 80] where the current is not completely perpendicular to the rogowski coil as the case here, a compensated coil has been chosen [62]. The primary of the coil is the terminal of the device. The shape of the terminal of the 1.7 kV SiC MOSFET is unknown(Fig. 5.15).

Among two winding techniques including winding with a return wire (see Fig. 5.16.a) and bifilar winding (see Fig. 5.16.b), a return wire compensated winding type has been chosen. This winding has been chosen due to its lower impedance and better immunity to noise [57]. In this type of winding, by continuing the turns (red lines in figure 5.17) at the end of the coil (surface of coil), a single return trace is made by passing all along the center of winding back to the starting point (see Fig. 5.17, blue line indicates the return-wire which here is a copper foil). The coil was manufactured by a 6 layer PCB (see Fig. 5.18) shown in figure 5.17. The first layer is the going wire and the second layer provides the return winding. Then two layers of the shielding are provided (PCB shield show as step 3 and 4 in figure 5.17).



(a)



(b)

Figure 5.18 – PCB rogowski coil (a) top view (b) cross-section view.

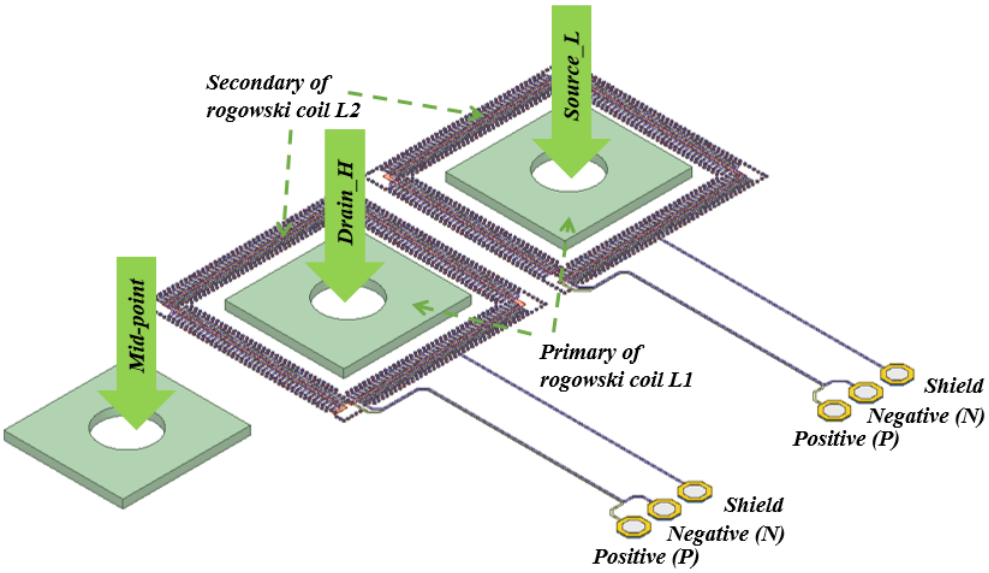


Figure 5.19 – Implementing Rogowski to the terminal of device.

To achieve the proper mutual inductance and reduce the effect of the added parasitic inductance (small leakage inductance), the number of turns in the secondary should be high enough compared to that of the primary. Therefore, a single turn to sense the current and maximum possible turns in secondary leads to increase the mutual inductance. To increase the number of turns in the secondary, the smallest via size and PCB track with the width of 0.2 mm dimension have been chosen. Moreover, due to size of the device terminal and considering both terminals are close to each other, the length of the PCB rogowski coil was limited to 1.2 mm. With the 6 layer PCB, a rogowski coil with 150 turns on the secondary has been manufactured to be implemented on the top of the device (see Fig. 5.19). The 150 turns, have been placed all around the terminal of the device where the current is passing as it can be seen in figure 5.19. Therefore, due to the device geometry, the maximum number of turns is achieved.

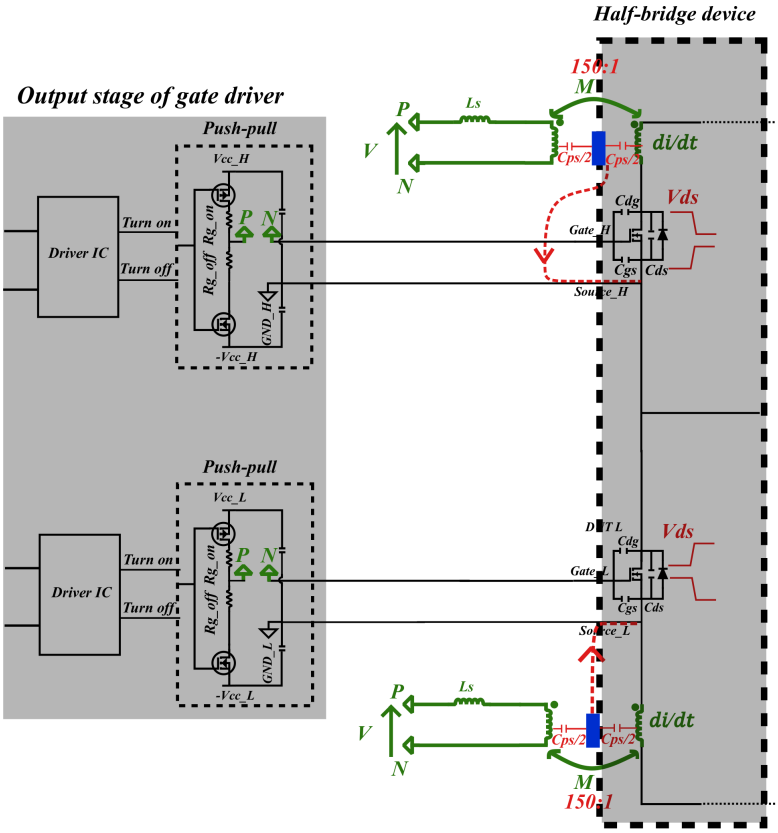


Figure 5.20 – Shielded rogowski coil.

The design integrates two rogowski coils into a half-bridge power module to sense the current of low-side and high-side switch. Then the coils are implemented in a half-bridge power module gate driver. As it can be seen in figure 5.19, the Rogowski coil is implemented on the top of the device terminal, where the voltage is changing at 30 kV/μs in this work. The parasitic capacitance between the primary inductor

and secondary winding (C_{ps} in figure 5.14) of the coil provides a coupling path for this voltage variation across the switch ($C_{ps}\frac{dv_{ds}}{dt}$). To overcome this problem, the PCB rogowski coil has been shielded by two PCB layers shield on top and bottom layer of the coils. The shield layers have been connected to the source of each switch in half-bridge device (see Fig. 5.20).

5.3.3 Experimental validation of rogowski coil

The impedance of the manufactured PCB was measured by impedance meter. The maximum rise time of the SiC MOSFET current is expected to be $40ns$ (corresponds to the frequency range up to 9 MHz). Therefore, the coil should be inductive in this range. The frequency response of the coil (see Fig. 5.21) illustrates that the current signal frequency is widely included up to $64MHz$ (first resonance) inside the frequency response of the manufactured coil. Moreover, the absolute inductance of the secondary is about $400nH$. To measure the mutual inductance and coupling factor of the rogowski coil, the coil has been tested in double pulse test at different current levels and $\frac{di}{dt}$ (see Fig. 5.23). The measurement points are shown in figure 5.22.

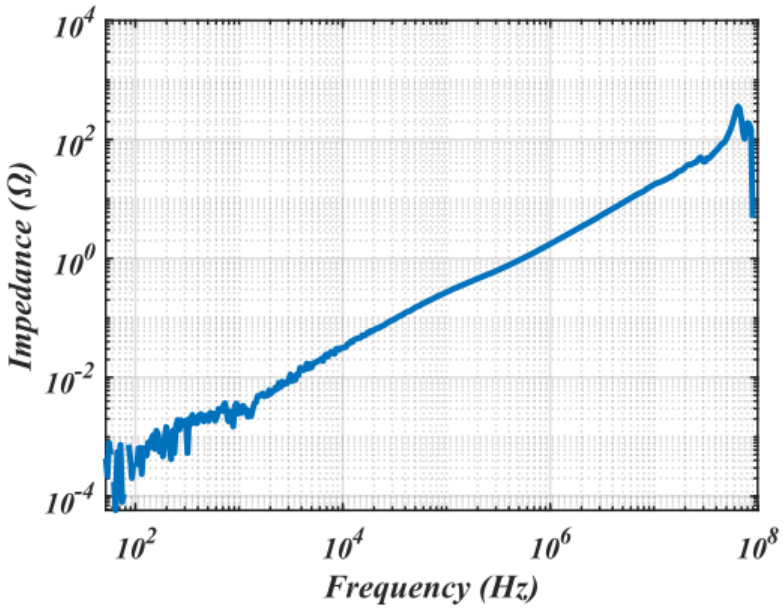


Figure 5.21 – Impedance measurement of PCB Rogowski.

The measured voltage (see Fig. 5.23) based on equations 5.1 and 5.2 [159] resulted in 30 nH and 0.47, Mutual inductance and coupling factor respectively (with open circuit in the secondary side and considering the interwinding capacitance is very small) It is noteworthy that the primary of the coil based on the data-sheet of

the power module [168] has been considered around $10nH$. The numerous number of turns in secondary of coil (150 turns) guarantees a reasonable mutual inductance that can compensate the induced inductance to the gate ($L2 - nM$ in Fig. 5.14).

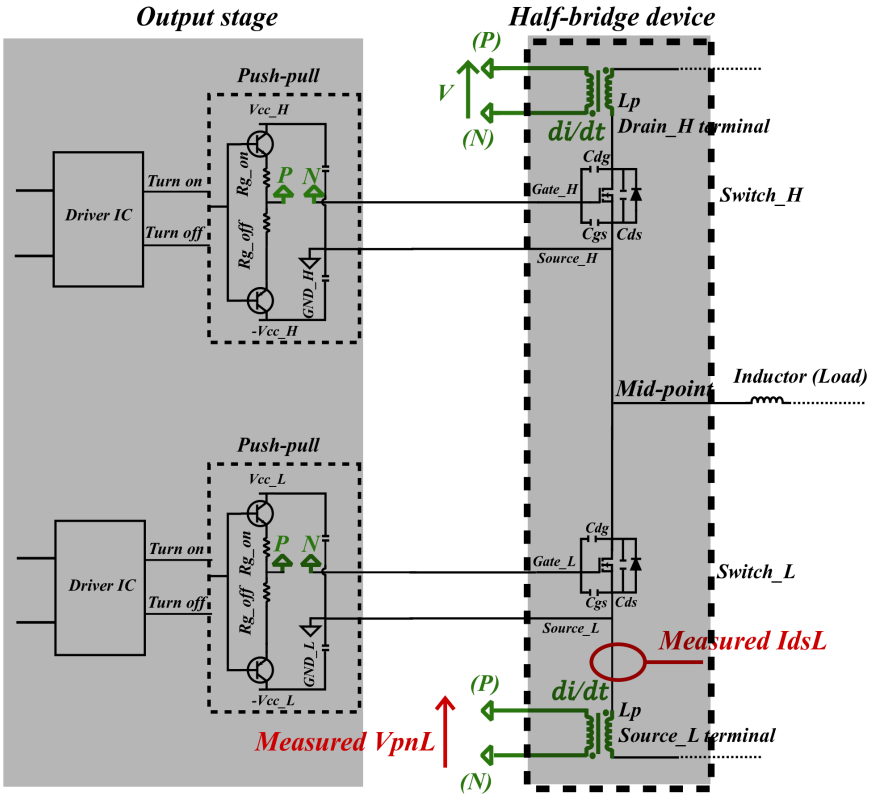


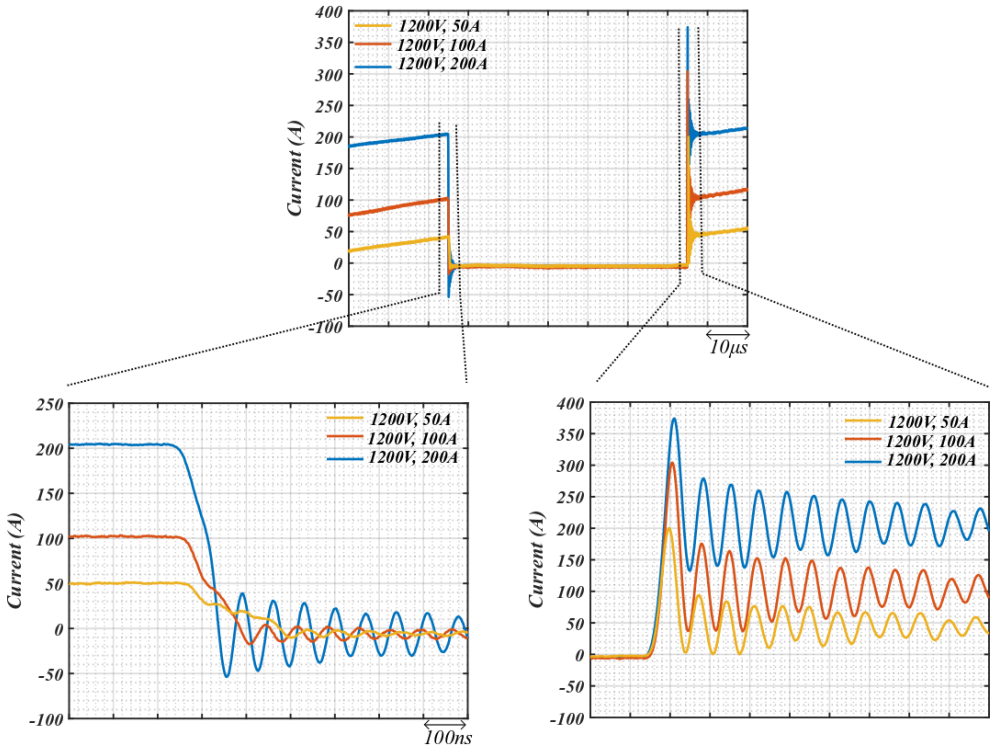
Figure 5.22 – Measuring created voltage by means of rogowski coil.

$$V = -M\frac{di_1}{dt} \tag{5.1}$$

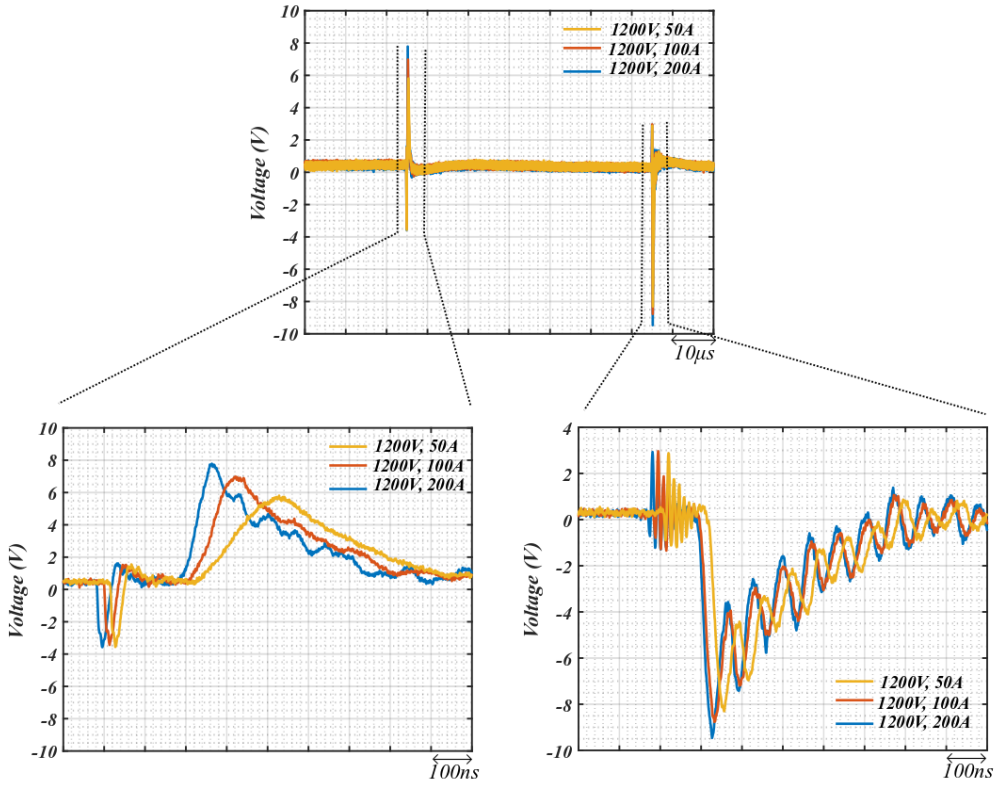
$$K = \frac{M}{\sqrt{L_1 L_2}} \tag{5.2}$$

Measuring the created voltage at the output stage of the rogowski coil comes with some difficulties. The fast rise time of the current and also created voltage in the presence of the fast voltage variation in mid-point of the half-bridge device reduces the accuracy of the measurement in terms of amplitude and frequency of the oscillation, therefore, as it has been noticed in chapter 4, the use of an isolated probe is necessary.

Experimental results shown in figure 5.23, validate the coil operation and created voltage based on current variation at the output stage of the rogowski coil. The maximum number of secondary turns leads to obtain enough created voltage (peak of 10V). As it can be seen, during turn-off transition, while the $\frac{di}{dt}$ is changing based



(a)



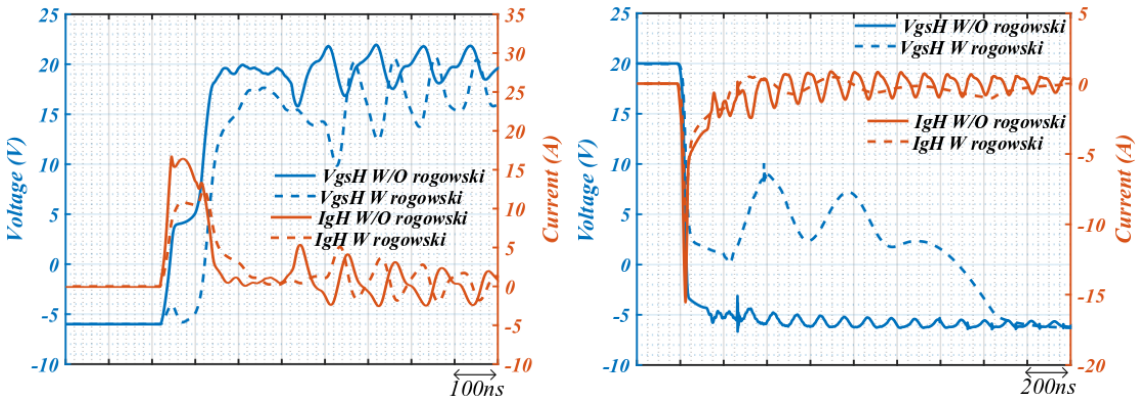
(b)

Figure 5.23 – Experimental results of generated voltage with rogowski coil, double pulse test, 1200 V, +50 A, +100 A, +200 A. (a) IdsL (b) VpnL.

on the inductor current, the voltage created by the rogowski coil is changing as well. Therefore, the rogowski coil can provide enough voltage to reduce the gate current and can be implemented to the gate driver.

5.3.4 Gate driver with integrated rogowski coil, simulation and experimental results

The rogowski coil with specified coupling factor and identical primary and secondary inductor measured in section 5.3.2, has been added to the circuit of the gate driver in LTspice simulation ($R_g = 0.2\ \Omega$). The simulation circuit is depicted in chapter 3. The circuit has been tested for both turn-on and turn-off transitions. Figure 5.24, shows the power MOSFET turn-on and turn-off transitions and the effect of the induced voltage to the gate with the integrated rogowski coil. The induced negative voltage reduces the voltage bias of the gate and consequently the gate current. Furthermore, voltage and current waveforms of the controlled switch (hard switching) are shown in figure 5.25.



(a) (b)

Figure 5.24 – VgsH with IgH, double pulse test, simulation, 1200 V, -200 A, comparing between without coupling (W/O) and with coupling (W) (a) Turn-on transition (b) Turn-off transition.

It can be seen that the gate current has been decreased during turn-on and turn-off which moderate the switching slope and oscillation. During turn-on transition, the impact of the rogowski coil is small on the V_{ds} voltage and it increases the oscillation of the current. During turn-off, the impact is what we expected for voltage and it slow-down slightly the current and voltage. Looking into the current shape in figure 5.25, it can be seen the current is disturbed which is not realistic due the connection of the power module to the layout explained in chapter 3.

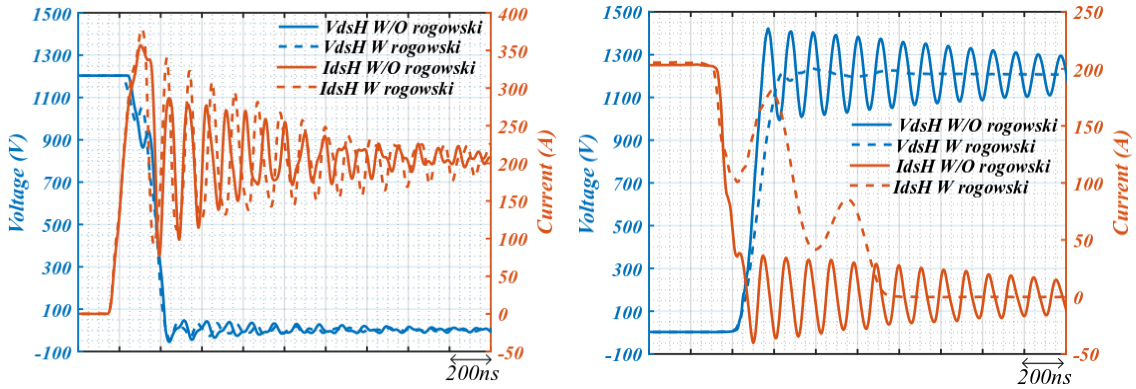


Figure 5.25 – VdsH with IdsH, double pulse test, simulation, 1200 V, -200 A, comparing between (W/O) without coupling and (W) coupling (a) Turn-on transition (b) Turn-off transition.

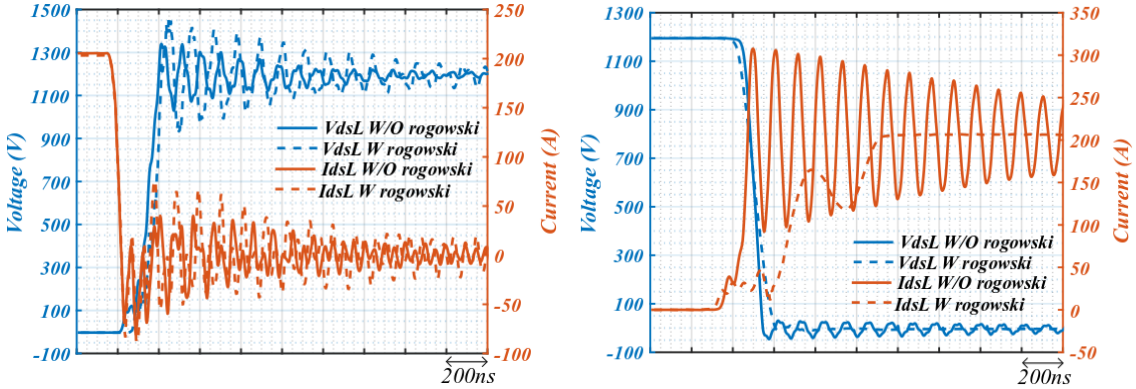


Figure 5.26 – VdsL with IdsL, double pulse test, simulation, 1200 V, -200 A, comparing between (W/O) without coupling and (W) coupling (a) Turn-off transition (b) Turn-on transition.

However, it can be seen in figure 5.25.a that the effect of the rogowski coil in gate source voltage does not dominate the effect of the added inductor to the gate during turn-on transition. This effect can be seen in voltage and current oscillation at turn-on of the high-side switch. Finally, the simulation results for the low-side switch (uncontrolled-soft switching condition) which is the projection of the high-side switch transition confirm the effect of the rogowski coil in turn-off transition more than in turn-on.

More current oscillations during turn-on leads to not decrease the CM current while, during turn-off transition, the induced voltage moderates the switching speed and consequently the generated EMI. Similar phenomenon has been reported in [45]. The current oscillations can be damped by increasing the gate resistance but as it has been explained, the goal is to use SiC MOSFET at its maximum switch-

ing speed. Therefore, since the approach has more positive impact on turn-off, in practice the method has been applied only for this turn-off transition.

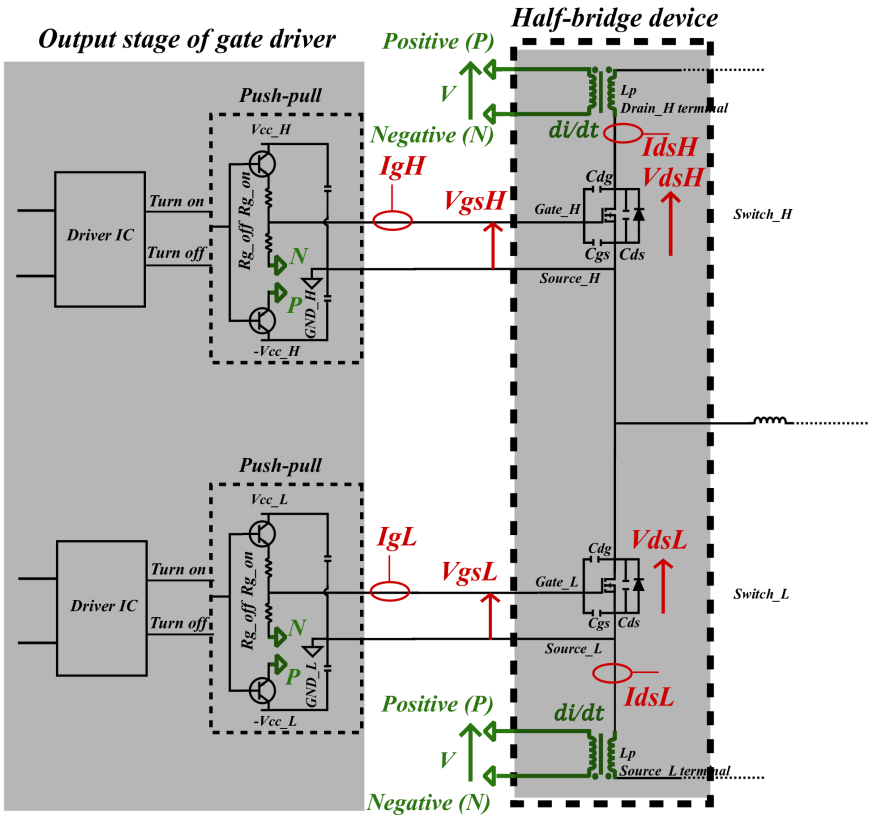
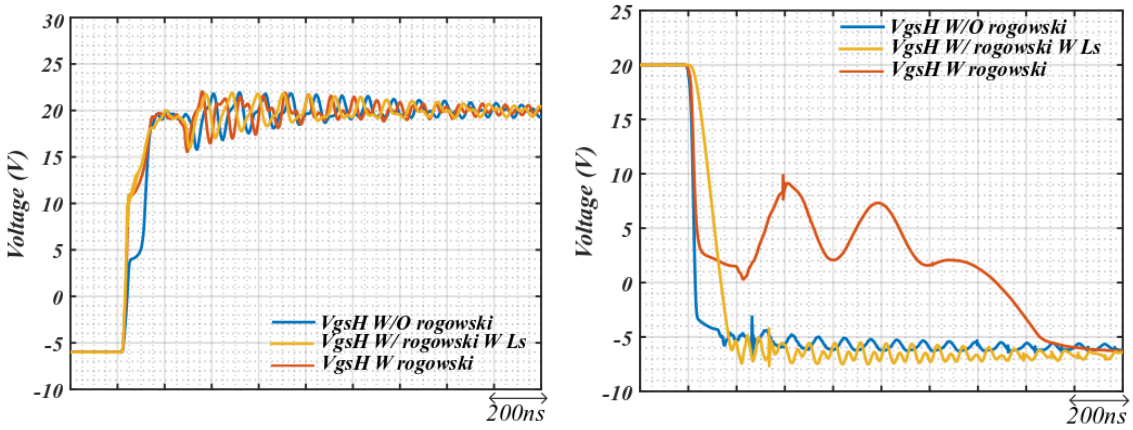


Figure 5.27 – Integrating the rogowski coil to turn-off path of push-pull in output stage of gate driver.

Moreover, to prove the effect of the coupling the output of the rogowski coil has been integrated in the turn-off path of the push-pull (see Fig. 5.11). To distinguish the effect of the coil, the self-inductance of the rogowski ($L_2 = 400nH$) has been added to the circuit and the simulation results compared the circuit without feedback (considering the $K = 0$, $L_1 = 0$ and $L_2 = 400nH$), with added inductance and with rogowski coil.

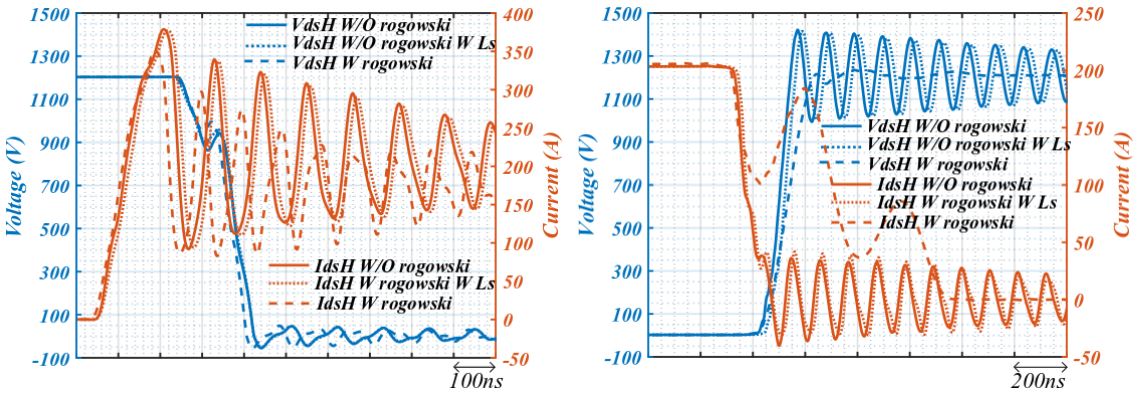
Comparing Vgs waveforms, shown in figure 5.28, illustrates that the induced voltage to the gate, does not affect the Miller-plateau region of Vgs. It has been explained in chapter 1 that changing this region leads to slow down the voltage and current variation across the switch. Increasing gate impedance to prolong this region changes the voltage/current rise and fall time. Here, the injected voltage thanks to rogowski coil, is not added during the Miller region. The voltage is added where the current is falling and that is moderate the switching current and voltage. Therefore, it is expected to have better trade-off comparing to the methods proposed in section 5.2.1 with losses. It is noteworthy that as it has been explained in chapter 3,



(a) (b)

Figure 5.28 – Vgs comparison (hard switching), double pulse test, simulation, 1200 V, -200 A, comparison between (W/O) without coupling, (W) with added inductor due to secondary of rogowski (Ls) and (W) coupling, (a) Turn-on transition (b) Turn-off transition.

the model of the semiconductor can not represent properly the behaviour of input capacitance which results in a behaviour of current in figure 5.29.



(a) (b)

Figure 5.29 – VdsH with IdH (hard switching), double pulse test, simulation, 1200 V, -200 A, comparison between (W/O) without coupling, (W) with added inductor due to secondary of rogowski (Ls) and (W) coupling, (a) Turn-on transition (b) Turn-off transition.

The switching waveforms presented in figures 5.29 and 5.30 highlight the effect of the added leakage inductance which is largely compensated by the coupling effect of the rogowski coil in turn-off transition. So as its effect on switching transition is negligible and induced voltage thanks to rogowski coil leads to gate current reduction in which reduces the current/voltage oscillations. The rogowski coil has been implemented in the gate driver of SiC MOSFET as it can be seen in figure 5.31.

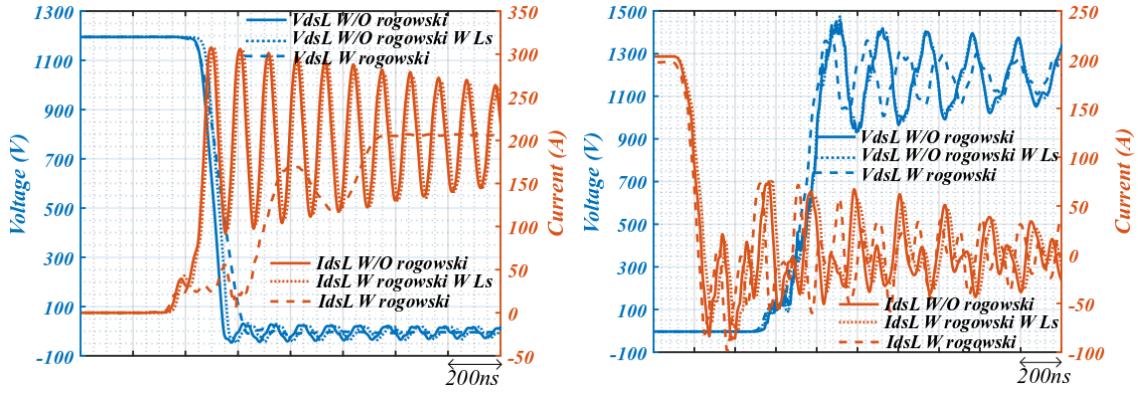


Figure 5.30 – VdsL with IdsL (soft switching), double pulse test, simulation, 1200 V, -200 A, comparison between (W/O) without coupling, (W) with added inductor due to secondary of rogowski (Ls) and (W) coupling, (a) Turn-on transition (b) Turn-off transition.

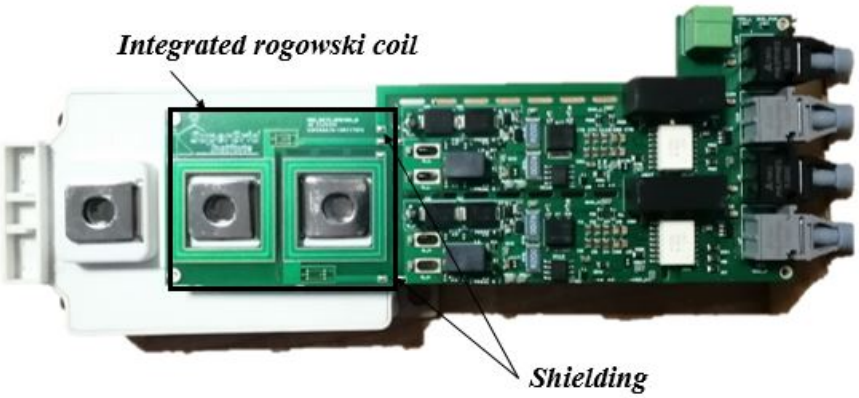
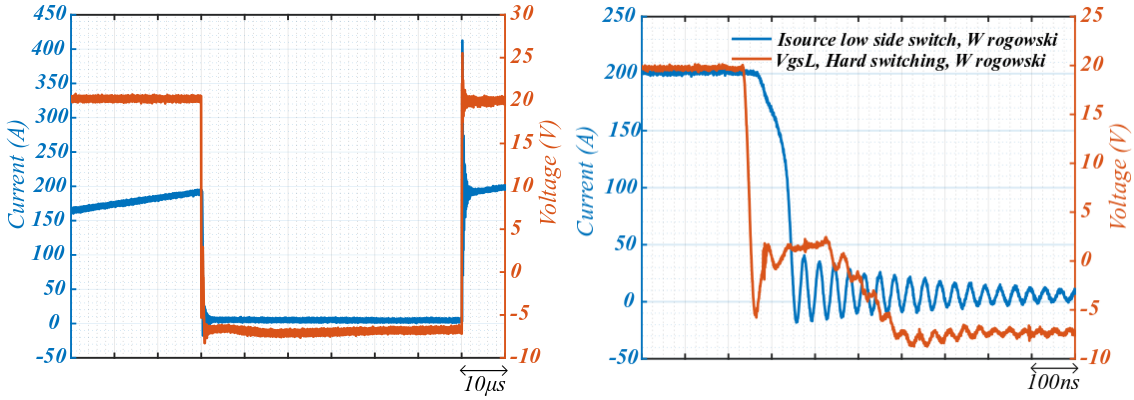


Figure 5.31 – Gate driver for SiC MOSFET with integrated rogowski coil.

The proposed gate driver has been evaluated experimentally in double pulse test platform in both positive and negative current directions in the inductor. As it is shown in figure 5.32, during switching transition of low-side switch in hard-switching condition, where the current in the switch is changing, a rogowski coil feedback is acting (turn-off transition).

As shown in figure 5.32.a, when the current is decreasing, the coil adds a voltage to the gate bias of the device. The modified Vgs and induced voltage has been compared with gate driver without rogowski coil in figure 5.33. The added coil does not change the turn-on transition.

Following the gate-source voltage modification in hard switching condition, the voltage and current waveforms of the switch (see Fig. 5.34), depict a moderate slope of the current and voltage. The reduction in the amplitude of the oscillations



(a) (b)

Figure 5.32 – VgsL with IsL (hard switching), experimental result, double pulse test, 1200 V, +200 A, rogowski coil integrated to gate driver (a) switching transition (b) Turn-off transition.

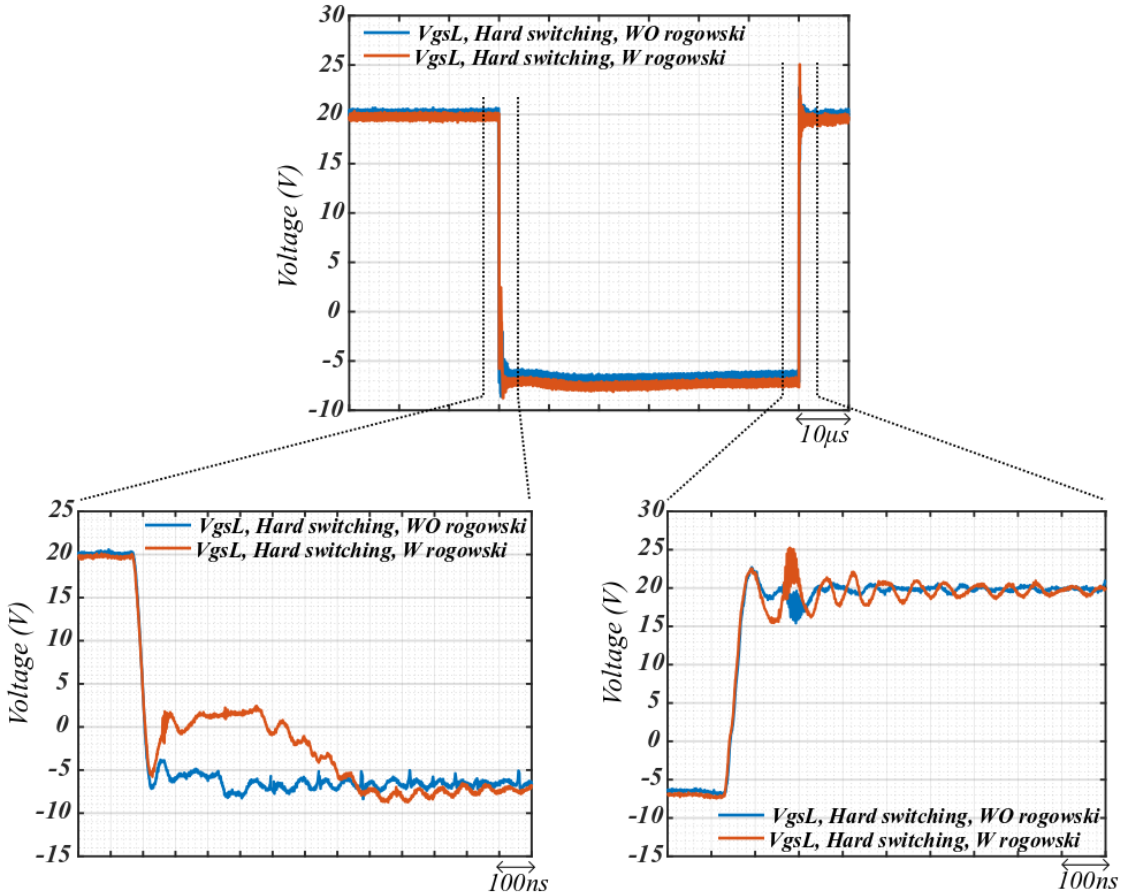
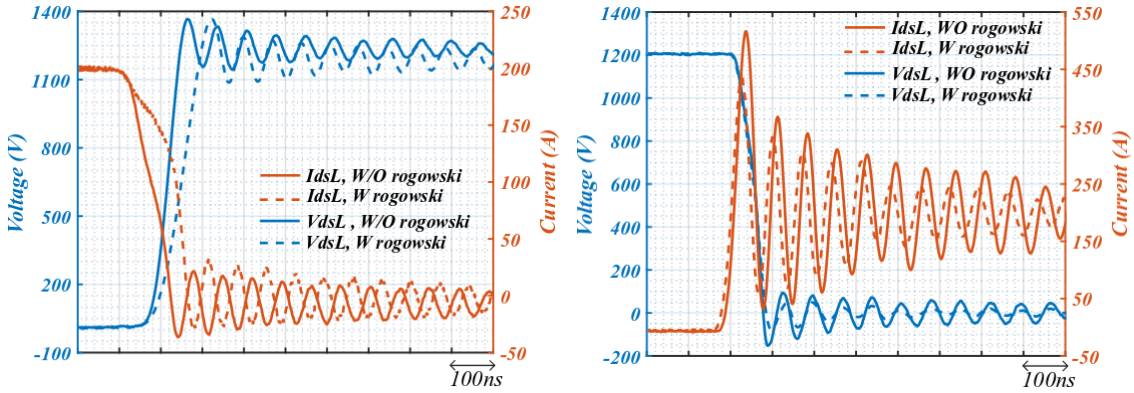
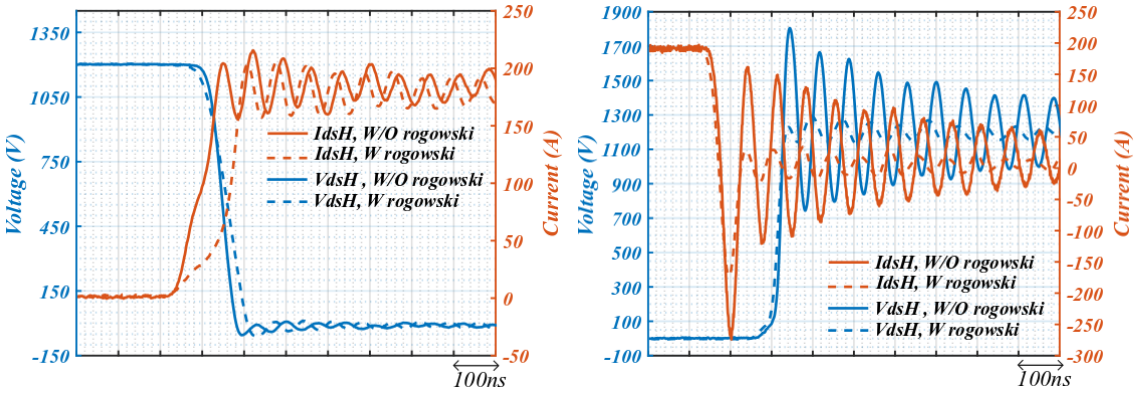


Figure 5.33 – VgsL comparison (hard switching), experimental result, double pulse test, 1200 V, +200 A, Comparison VgsL (W/O) rogowski coil and (W) with rogowski coil integrated to gate driver.



(a) (b)

Figure 5.34 – VdsL with IsL, double pulse test, experimental result, 1200 V, +200 A, comparing between (W/O) without rogowski coil and (W) rogowski coil integrated to gate driver, (a) Turn-off transition (b) Turn-on transition.



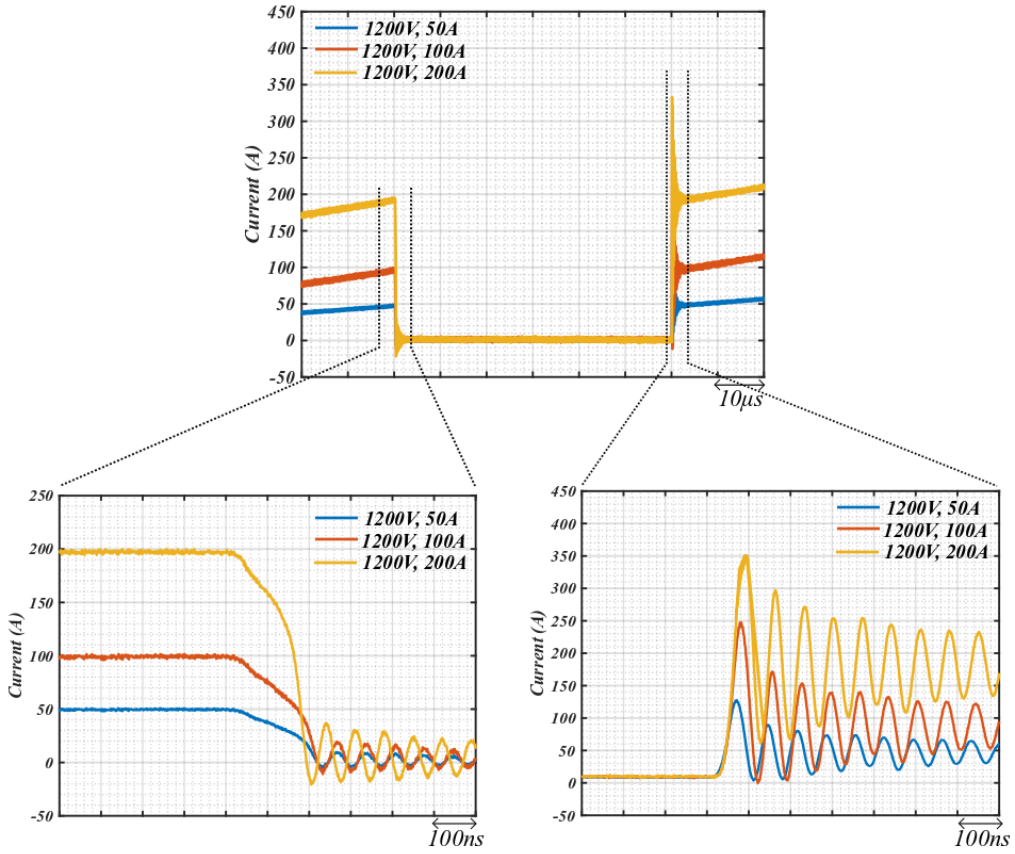
(a) (b)

Figure 5.35 – VdsH with IdH, double pulse test, experimental result, 1200 V, +200 A, comparing between (W/O) without rogowski coil and (W) rogowski coil integrated to gate driver, (a) Turn-on transition (b) Turn-off transition.

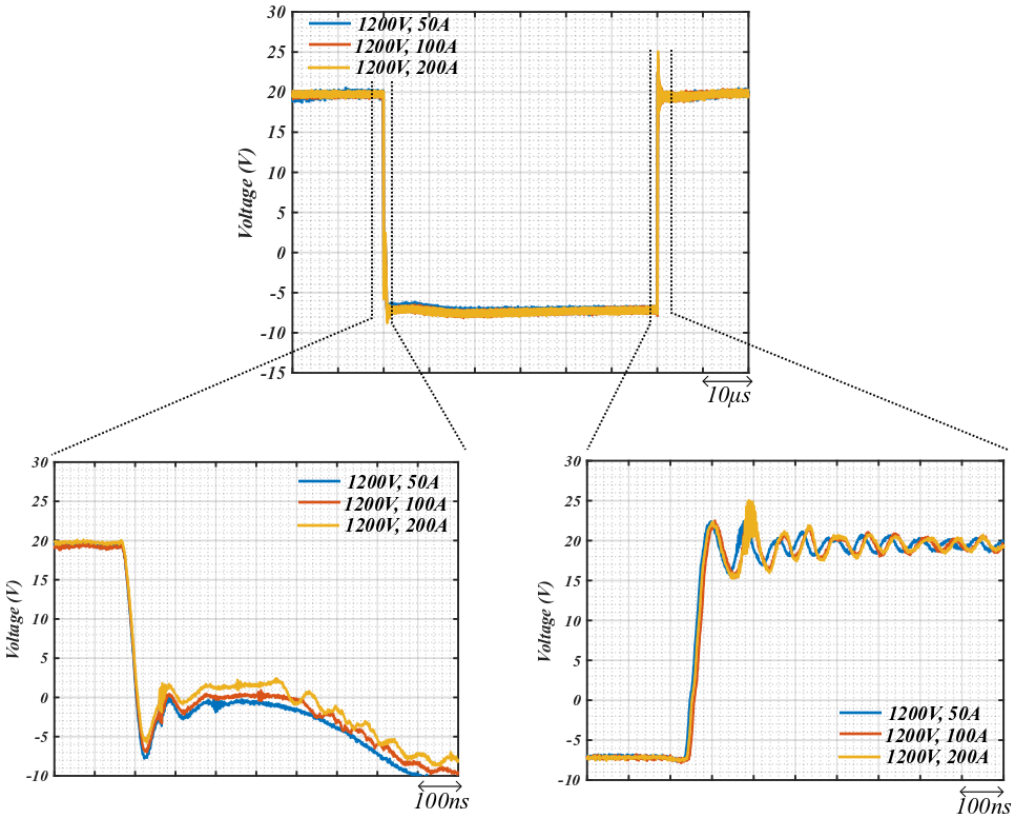
(Figure 5.34.b) is due to the added inductor in push-pull path which slightly changes the turn-on transition (shown in simulation result in figure 5.28).

The switching waveforms of the uncontrolled switch (high-side switch) is displayed in figure 5.35. As it has been explained, the current and voltage waveforms of this switch (soft switching condition) is shaped based on the other side (hard switching) therefore, similar current and voltage waveforms to the low-side switch can be seen in figure 5.35.

The double pulse test has been repeated for different current levels. By increasing the current, the level of variation of di/dt is changing during turn-off (see Fig. 5.36.a). Different $\frac{di}{dt}$ result in different induced voltage to the gate during turn-off (see Fig. 5.36.b) which leads to have different switching slopes. Experimental results shown in figure 5.37, illustrates the effectiveness of the proposed method at high current and high voltage SiC MOSFET.

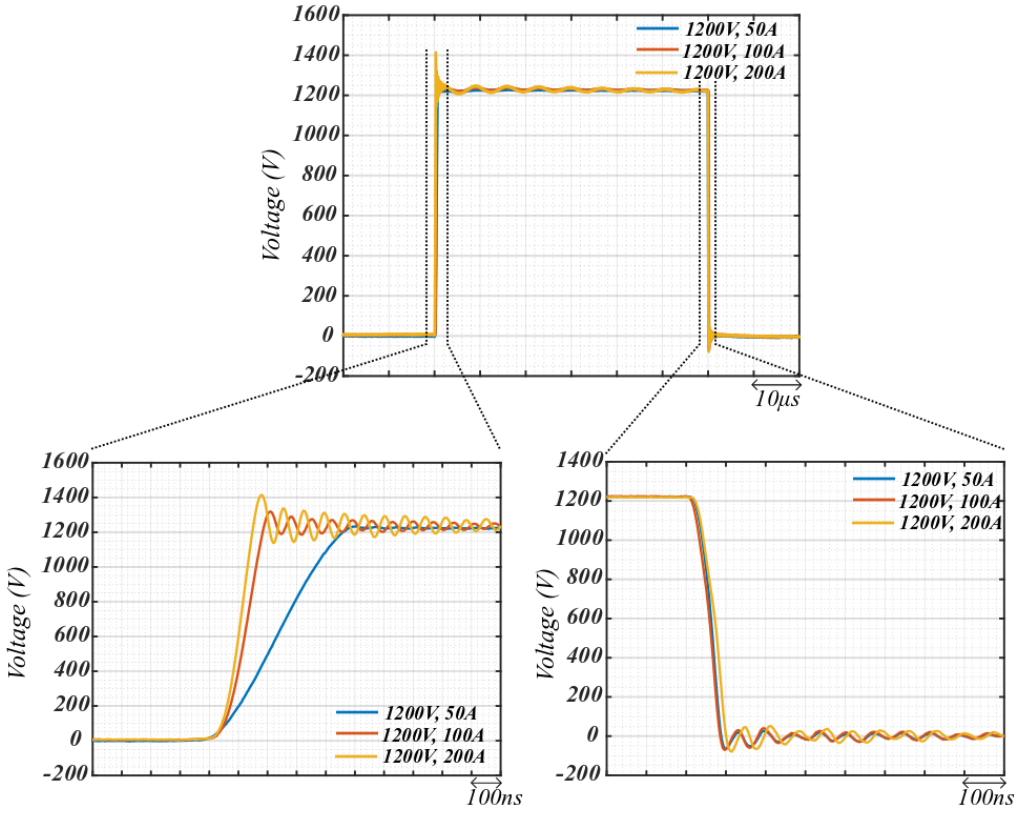


(a)

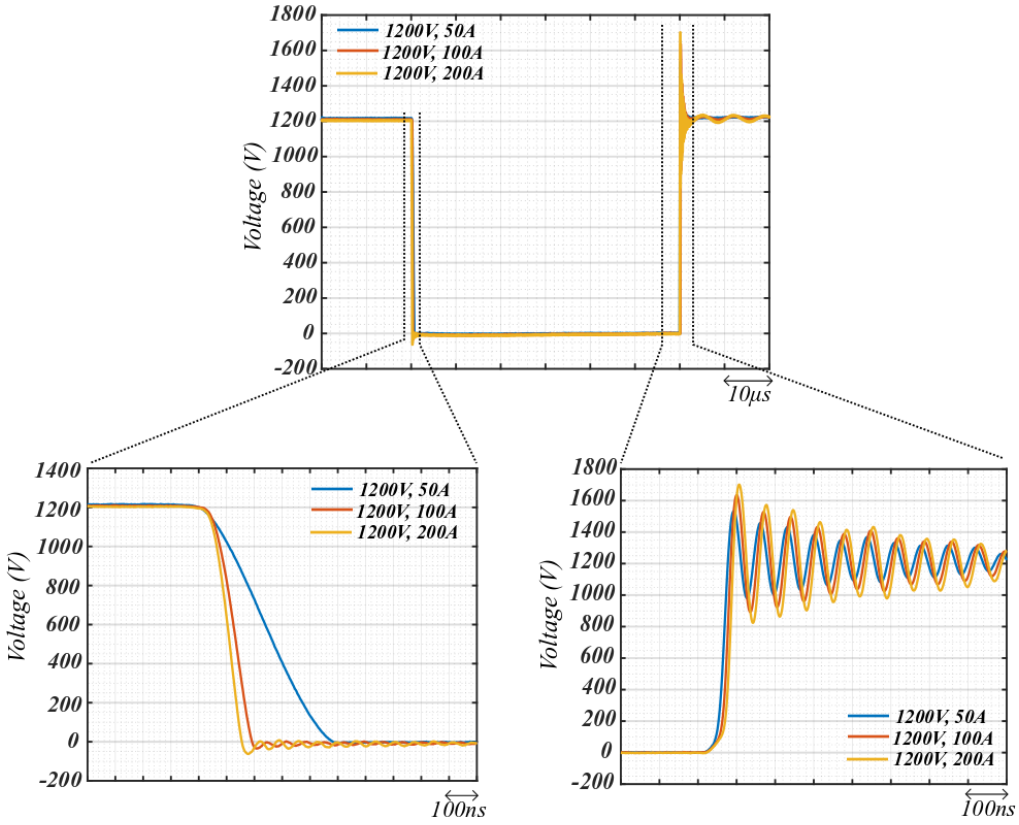


(b)

Figure 5.36 – IsL and VgsL (hard switching), experimental result, double pulse test, gate driver with integrated rogowski coil, 1200 V, +50 A, +100 A, +200 A (a) IdsL (b) VgsL.



(a)



(b)

Figure 5.37 – Vds measurement, experimental result, double pulse test, gate driver with integrated rogowski coil, 1200 V, +50 A, +100 A, +200 A (a) VdsH (soft switching) (b) VdsL (hard switching).

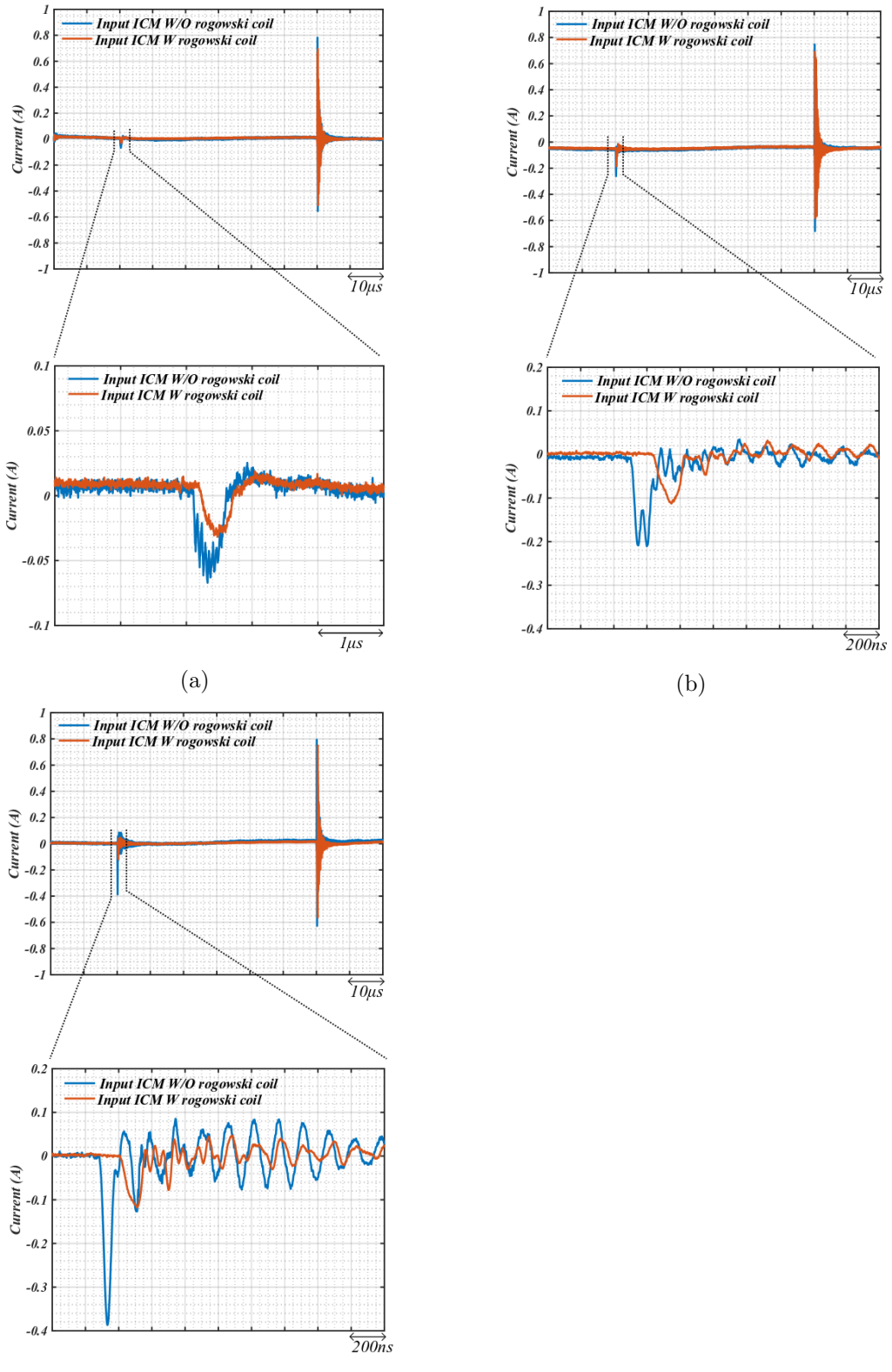


Figure 5.38 – Experimental Input ICM comparison between the gate driver without (W/O) integrated rogowski coil and with gate driver with (W) integrated rogowski coil, Double pulse test, 1200 V (a) +50 A (b) +100 A (c) +200 A.

The effectiveness of the induced voltage can be seen through the input CM current reduction shown in figure 5.38. It has been explained in chapter 2 that for the converter applications, turn-on soft switching helps to reduce the EMI while turn-off transition is still a question since it happens in hard-switching conditions. The experimental results presented in figure 5.38 shows the effect of the proposed gate driver in EMI reduction by affecting the turn-off transition. The switching characteristics has been repeated for double pulse test in negative current direction where the low side switch is in soft switching and the high side switch is in hard switching conditions. The experimental results are shown as figures 9, 10, 11 and 12 in Annex of this chapter.

5.3.5 Trade-off comparison between the proposed method and classical increasing gate resistance

In order to evaluate the proposed method in terms of losses compared to conventional increasing gate resistance method, it has been tried to have the same amount of the input CM current reduction as integrating rogowski coil by means of increasing the gate resistance. This was achieved by increasing the gate resistance from 0.2 Ω to 5 Ω (see Fig. 5.39). The experimental comparison is shown for the case where the high-side switch is controlled. The level of the CM current in turn-off and turn-on is almost the same.

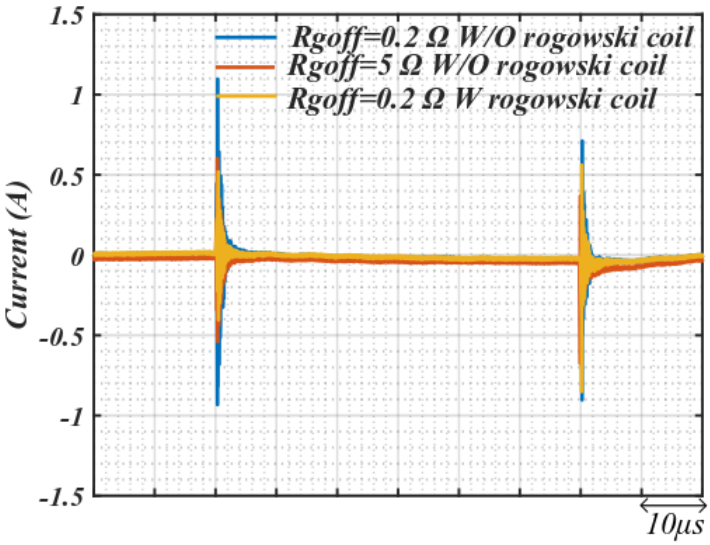
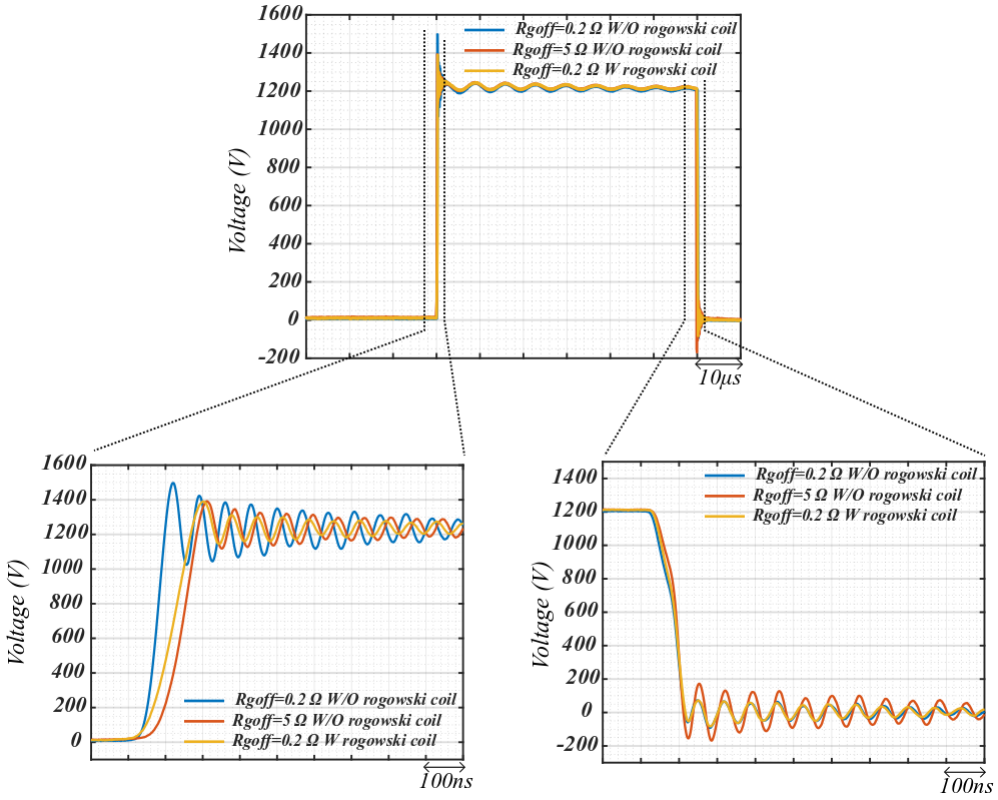
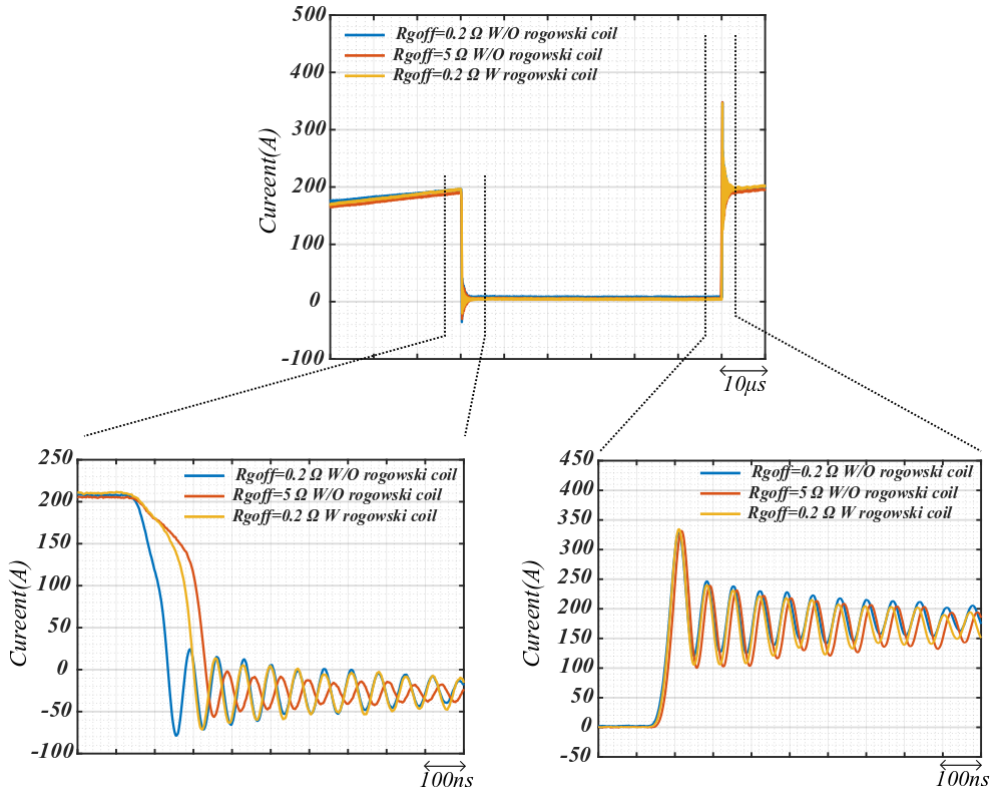


Figure 5.39 – Input CM current comparison, experimental result, double pulse test, 1200V, -200A

Experimental comparison between the current and voltage switching waveforms shown in figure 5.40, illustrates that by increasing the gate resistance to achieve



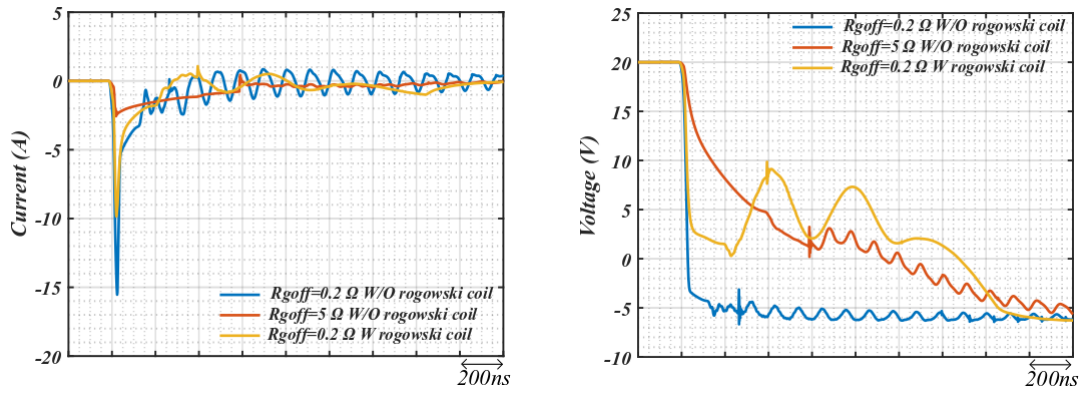
(a)



(b)

Figure 5.40 – VdsH with IdsH comparison (hard switching), experimental result, double pulse test, 1200 V, -200 A, comparison between gate driver (W/O) without rogowski and (W) with integrated rogowski coil (a) VdsH comparison (b) IdsH comparison.

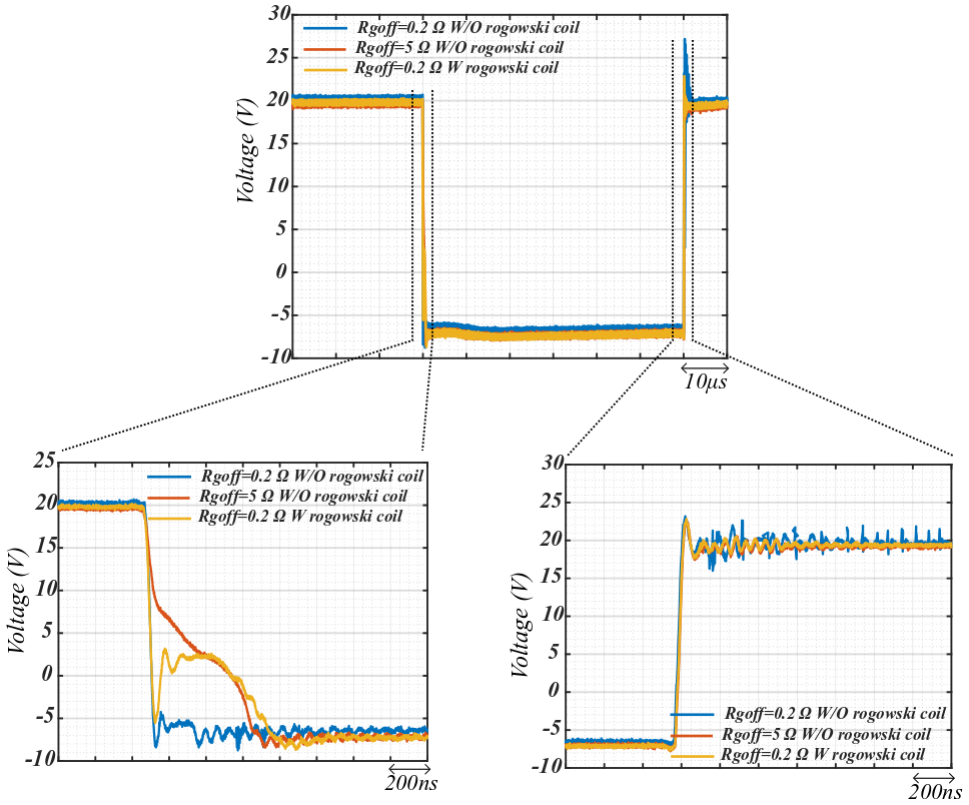
the same amount of CM current reduction, it slows down the switching slope which results in increasing switching losses compared to proposed method in this work (see Fig.5.43). To explain the difference between the methods, the Vgs waveforms of both methods have been compared in figure 5.42. The more decrease of switching slope by increasing the Rg_{off} stems from the prolonged Miller-plateau region during turn-off transition which slows down the discharging of the input capacitance of the device. Increasing the gate resistance can reduce the gate current and at the same time delay and reshape the Miller-plateau shown in figure 5.42.a. The phenomenon has been reproduced in simulation and figure 5.41 shows how increasing the gate resistance decreases the gate current level drastically compared to the inductive feedback gate driver. The more the gate current decreases, the more the switching slope decreases and the losses increases.



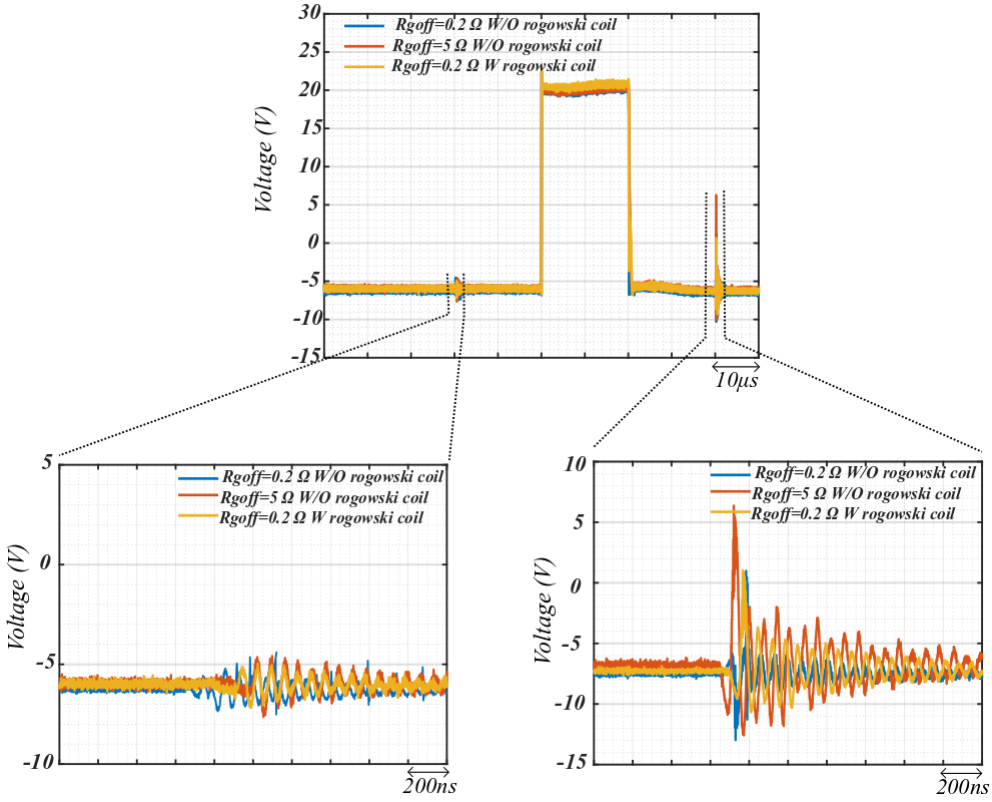
(a) (b)

Figure 5.41 – IgH and VgsH (hard switching) during turn-off transition, simulation result, double pulse test, 1200 V, -200 A, comparison between gate driver (W/O) without rogowski and Rgoff=0.2 Ω, (W/O) with increased Rgoff=5 Ω and gate driver (W) with integrated rogowski with Rgoff=0.2 Ω (a) IgH comparison (b) VgsH comparison.

The switching losses have been calculated based on explanation from chapter 1 figure 1.10. The proposed gate driver outer-performs the conventional approach by better trade-off with losses as it has been shown in figure 5.43 up to 12 %. Moreover, during these measurements, only Rg_{off} has been increased while keeping the Rg_{on} equal to 0.2 Ω, the turn-on switching speed has not been changed. Looking into experimental results shown in figure 5.42.b, it can be seen that by increasing Rg_{off}, the impedance of the gate has been increased and the voltage variation across the low-side switch has been coupled to gate path and due to the increased gate impedance exacerbated the self-disturbance phenomenon (The phenomenon explained in Chapter 4). On the other hand, the injected voltage due to rogowski coil in low-side switch (soft switching) occurs during dead time where the injected



(a)



(b)

Figure 5.42 – Vgs comparison, experimental result, double pulse test, 1200 V, -200 A, comparison between gate driver (W/O) without rogowski and (W) with integrated rogowski coil (a) VgsH (hard switching) (b) VgsL (soft switching).

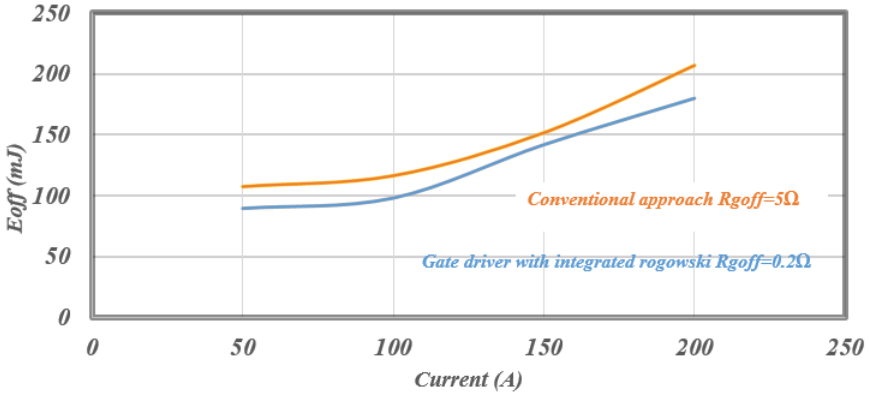


Figure 5.43 – Comparison of the turn-off losses between conventional approach and proposed gate driver.

voltage is in opposite polarity of the induced gate perturbation which shows another positive point of the proposed method.

5.4 Conclusion

A new method of controlling turn-off switching process of 1.7 kV SiC MOSFET gate driver is presented in this part of the work. The inductive feedback gate driver thanks to a simple feedback from drain current to the gate, induces a positive voltage during turn-off, thereby reduces the gate current during a short period. This gate current reduction moderates the switching slope and voltage/current switching oscillations. The method has been tested and validated for a 1.7 kV SiC MOSFET power module. The new method reduce the input common-mode current of the gate driver as it has been targeted and explain in chapter 1. Decreasing the input common-mode current decrease the risk of self-disturbance in the operation of the converter. Increasing gate resistance is one of the best solution for the moment to overcome EMI problem in SiC MOSFET based converter, however, thanks to new techniques such as inductive feedback, achieving better efficiency is feasible. The gate driver can be used in converter operating in ZVS where the hard-switching turn-off is happening. Therefore, the proposed gate driver can act on turn-off transition and improve the EMI behaviour of the converter. In comparison with reviewed approaches for active SiC MOSFET gate driver, the proposed feedback has not imposed any delay in switching transition of the SiC MOSFET. Therefore, there is no need of delay compensator circuit for this approach. Unchanged turn-on process has been shown experimentally which means that the applied method on turn-off will not change the turn-on switching speed of the converter. Moreover, the reduction in turn-on oscillation due to slight change in gate-source voltage brings

benefit. This makes the proposed gate driver a relevant choice for ZVS converter type.

Although the added inductance to the gate, increases the gate impedance during the dead-time, but opposite induced voltage during positive and negative gate perturbations in soft switching condition, compensates the self-disturbance phenomenon independently.

6

Conclusion and perspectives

Conclusion

This dissertation considered the difference between switching characteristics of the Si IGBT and SiC MOSFET semiconductors which affect the gate driver designs. Then the study focused on the conducted electromagnetic interferences generated by fast SiC MOSFET semiconductors in converters and the effect of the interferences on the gate drivers.

The study focused on commercial power semiconductors including Si IGBT and SiC MOSFET that are used nowadays in power converter applications. The experimental comparison indicated that SiC MOSFETs can be very competitive as a replacement of Si IGBTs. SiC MOSFET characteristics showed clearly the potential to deliver revolutionary impact in power converter efficiency. By comparing two devices, the side effect of this superior characteristics has been revealed as switching current/voltage overshoot. This fast variation of switching voltage/current and also voltage/current oscillation are the main origins of converter operation disruption. Therefore, this PhD work intended to show the challenges in front of converter designers by using new semiconductors like SiC MOSFETs. Electromagnetic compatibility study in converters is a multi dimension task. Here it is tried to focus on

false-triggering phenomenon due to electromagnetic interferences and to propose a methodology to overcome this issue.

The electromagnetic interferences generated by SiC MOSFETs were creating disorders which have been observed in a 100 kW three-phase 1.2 kV Dual Active Bridge converter prototype. It has been proved that the exacerbated interferences were disturbing the correct triggering of switches. The false-triggering of semiconductors due to uncontrolled magnitude of the interferences was called "self-disturbance" phenomenon in this project. This study showed that the uncontrolled electromagnetic interferences passing through gate drivers (input common-mode current) is one of the causes that can disturb the converters operations. Therefore, dealing with self-disturbance became the objective of this work to keep the proper operation of the converter. This goal has been achieved by applying two different types of solutions. A system level solution and a circuit level solutions. The system solution was intended to divert the parasitic current from the susceptible device (here the gate driver) and secondly to reduce the interferences from the source.

The system level solution is focused on the converter grounding layout and the effect of the parasitic capacitances to the ground which provide paths for common-mode currents to come back to its source. The proposed embedded filter in the transformer structure reduced the interferences significantly and enabled the converter to achieve its nominal operation. The investigation gives a technical information for future transformer design. It is experimentally proved that the transformer design can act on improving EMI behaviour of gate drivers and consequently power converters.

Regarding the circuit level solution it is targeted to reduce the EMI by means of gate driver. The study considered the specification of SiC MOSFETs which lead to self-disturbance phenomena to design and develop a new gate driver for 1.7 kV SiC MOSFET power modules. For this part of the study, a full-bridge converter has been considered which allows the comparative studies. The simulation tool and the modelling approach presented for this converter clarified the effect of the switch model for EMI study.

The SiC devices with low threshold voltage, low maximum allowable negative gate voltage were subject to gate voltage perturbations. To overcome this phenomenon, a gate assistant circuit is proposed for complementary switching effect suppression in a phase-leg configuration. The test results coming from 1.7 kV SiC MOSFETs showed that the gate assistant circuit improved the switching performance and allowed tests up to a certain DC bus voltage level with minimum gate resistance (fast switching). However, this solution is not adequate to achieve the

potential rated voltage/current of the device. Then a new method in the form of an integrated bifilar common-mode filter into the gate driver circuit has been validated experimentally to be able to reduce the self-disturbance up to 20%. Furthermore, the proposed filter implementation in addition with assistant circuit notably reduced the electromagnetic interferences passing through the gate driver. This input common-mode current reduction makes this method suitable for converter applications considering the reported phenomenon in a 100 kW converter prototype.

In a second part of the self-disturbance reduction by means of gate driver, a new inductive feedback gate driver for SiC MOSFET power module (1.7 kV as an example) was developed and validated experimentally up to 1200 V, 200 A. The gate driver was implemented into power module terminals. A gate-current open-loop control has been inserted in this driver to control the $\frac{di_{ds}}{dt}$ and $\frac{dv_{ds}}{dt}$ of the power module by modifying the $-6V$ gate bias. The aim of current/voltage switching slop control was to limit the conductive interferences passing through the gate driver of the power module without introducing delay into switching transition. Therefore, by modifying the negative bias of the driver (- 6 V) during switching transition, the turn-off controlled switching transition has been achieved. This moderate switching transition resulted in limited electromagnetic interferences. The experimental studies validated the proposed method at different voltage and current levels. To achieve the same performance in terms of EMI, the conventional method (increasing gate resistance) has been applied to the gate driver. The experimental results verified 17% energy losses saving thanks to the new proposed method.

The DC/DC converter prototype in this work benefits from soft-switching ZVS method. ZVS can reduce the generated electromagnetic interferences during turn-on transition. However, turn-off transition still is a question that needs to be answered. One of the main challenges in turn-off transition as it has been shown in this study as well, is the classical increasing gate resistance became a critical issue in fast switching. In the case of fast switching half-bridge semiconductors, it is not possible to decrease the turn-off switching speed by series gate resistance without decreasing the switching speed for turn-on of the complementary switch. This is because fast turning-on of one of the switches in half-bridge device creates parasitic current which couples to the turn-off gate impedance path of other switch in half-bridge and creates the self-disturbance explained in chapter 4. In this concept, considering all the constraints for fast switching and soft switching techniques applied in the 100 kW converter, the proposed gate driver introduces a suitable method for high efficiency soft-switching converters. The driver performances were validated at turn-off without affecting turn-on switching transitions. Another advantage is that the

proposed gate driver benefits the classical gate driver design with minimum changes in the layout.

Perspectives

Several improvements for this work can be considered. From the experimental work carried out in the 100kW converter, the common-mode impedance to the ground can be considered at early stage of the transformer design. The detailed model of the transformer which considers the parasitic capacitance to the ground can help designer to anticipate the common-mode current circulation during the modelling stage of the converter. Moreover, the precise high frequency knowledge of the converter behaviour can help to reduce the EMI of converters. Another point of improvement that can be considered for this work is conducting measurement with a Line Impedance Stabilization Network. While there is not a standard for EMI study on high frequency of 100 kW converter, considering the effect of the network interferences can improve the proposed methodology for EMC study of the converter.

Considering the reported conclusions and benefits of the proposed gate driver, the following steps to continue this work are proposed.

1. In modelling section, the detailed model of the gate driver can be studied. Reduced model of the electronic board can help to have more realistic gate source voltage waveforms.

2. In this work, the modelling of the semiconductor package is missing some points including kelvin-source connection and gate terminal parasitic impedance. These elements affect directly the gate voltage waveform and consequently the switching characteristics because they impact directly the parasitic elements of the gate loop and consequently the switching loop. Moreover, a more accurate dynamic model of the switch can improve the modelled converter. In this way, the chosen value for the common-mode filter proposed in chapter 4 can be optimised in simulation which is less time consuming than an experimental method. The difference between simulation and experimental results showed the importance of these elements as well. Therefore, a more accurate model of the semiconductor package leads to a more optimised design and reduces the experimental time and costs.

3. The method has been validated for turn-off transitions. The created voltage thanks to the rogowski coil can be added to the positive gate bias which can boost the gate charging and consequently boost the turn-on transition of the semicon-

ductor. It is off interest to evaluate the performance of the gate driver for faster switching applications.

4. Short-circuit protection is one of the most critical features of gate drivers which prevents semiconductor switches from breakdown or explosion. The shoot-through current passing through the half-bridge device during short-circuit phenomenon will damage and destroy the device. It became more critical with the emergence of HVDC/MVDC application because power electronic components are expensive for these applications and the energy release due to explosion is huge. The conventional solution for Si IGBT protection is the DeSaturation (DeSat) that uses the device output characteristics. The DeSat protection usually reacts within several microseconds. It is due to the fact that the DeSat circuit responds when the V_{ce} (Voltage across the switch) is close to zero. The difference between IGBT and SiC MOSFET is that the SiC MOSFET current (I_{ds}) keeps increasing even though the V_{ds} voltage is still at high value (See Fig.1.7 in chapter 1). This characteristics makes the current overshoot considerably bigger than the Si IGBTs. On the other hand, it makes the accumulated energy bigger than the Si IGBTs. So as SiC MOSFET needs faster response circuit compared to DeSat circuit because the device can not withstand long time with this huge amount of current overshoots. SiC MOSFET characteristics became an interesting research topic nowadays like in SuperGrid institute. Direct drain-source current measurement is one of the method that can process faster than conventional DeSat circuit. Therefore, one of the possible future projects of the present work is to benefit the integrated rogowski coil for short-circuit protection circuit.

5. One of the current techniques used in prognostics and state of the health monitoring for power electronic modules is to monitor thermo-sensitive electrical parameters of the semiconductor devices such as saturation current. The integrated rogowski coil in this work can be applied for smart gate drivers for device health monitoring, junction temperature estimation and failure diagnostic.

6. As a final perspective of this PhD work, an experimental validation will be conducted on a high-power converter prototype (100 kW, 1.2 kV Dual Active Bridge converter) to evaluate the performance of the proposed gate driver in a completed converter prototype.

.1 Appendix chapter 2

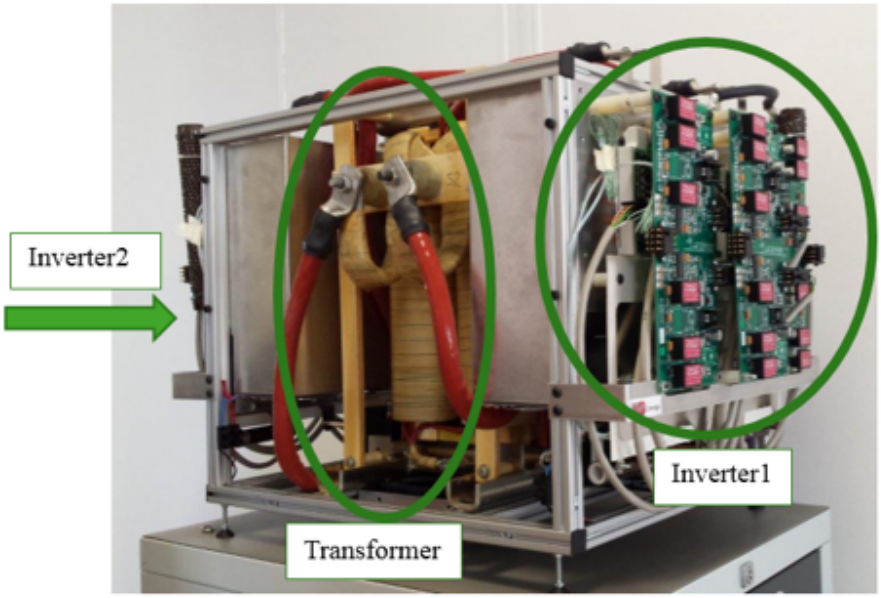


Figure 1 – Single phase DAB prototype, 1200V, 100kW, 1.7 kV SiC MOSFET as a switch.

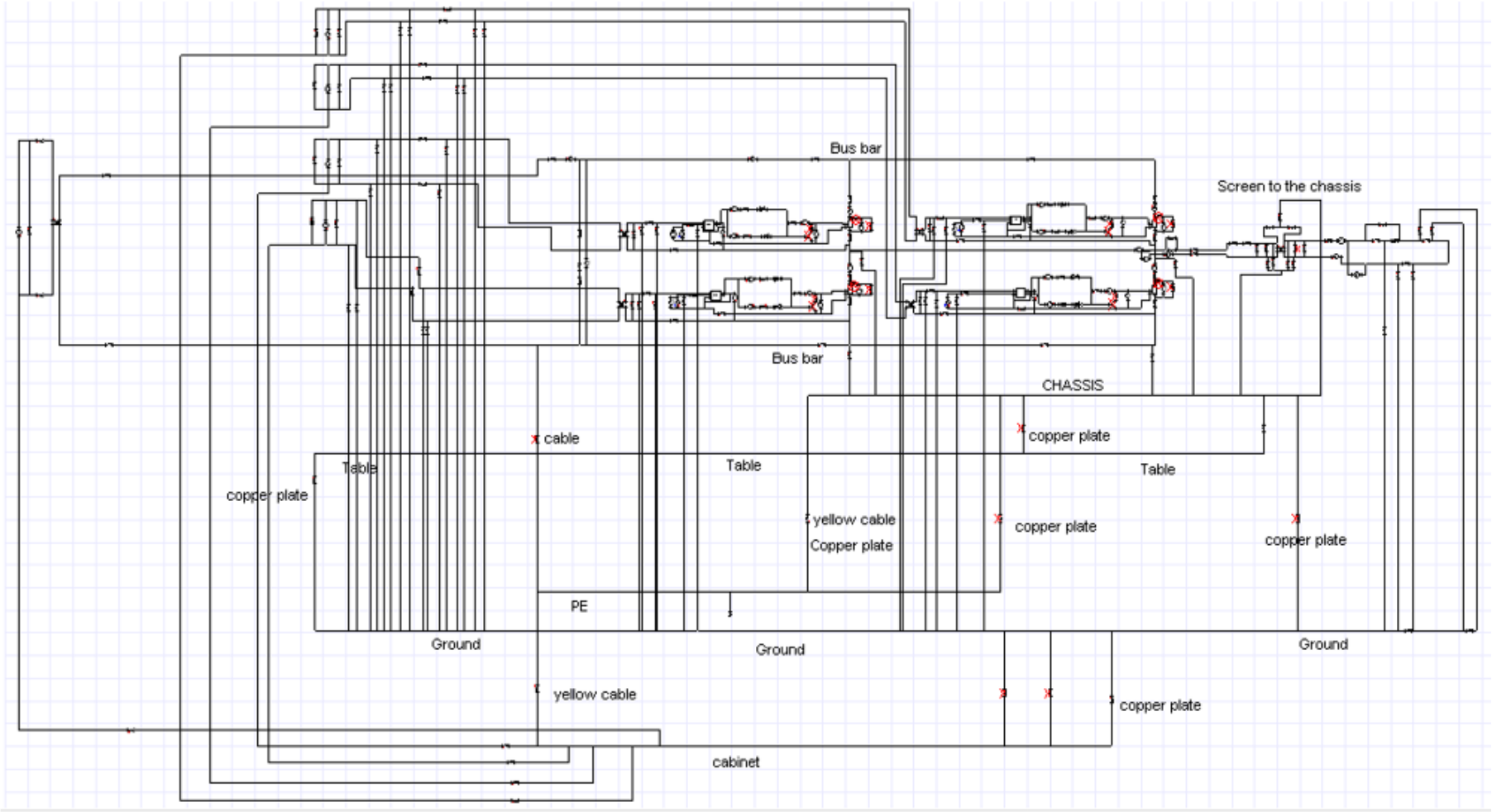


Figure 2 – Single phase VSC1 simulation schematic in simplorer

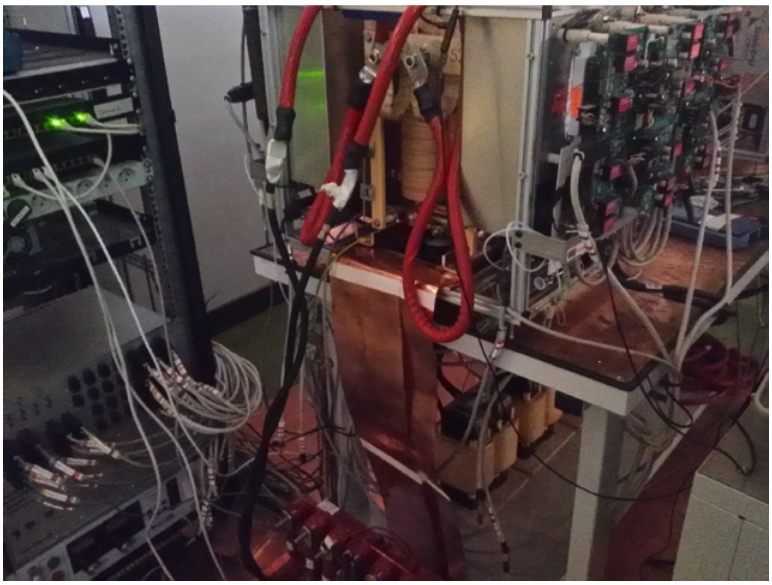


Figure 3 – Single phase DAB prototype ground modification, screen of transformer to ground

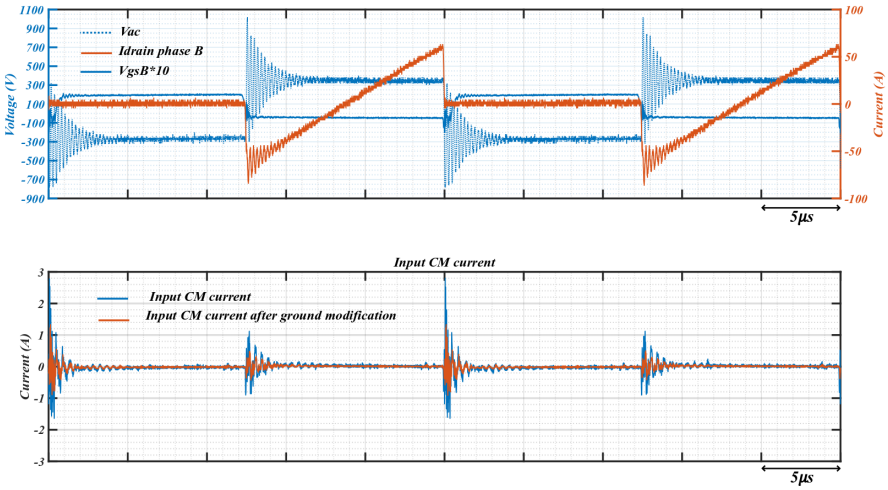


Figure 4 – Experimental results, input CM current of VSC1.

.2

Appendix chapter 3

The model of the 1.7 kV die and the Schottky diode used to create the power module.

```
**     DISCLAIMER
********************************************************************************
**     This model is provided as is, where is, and with no warranty of any kind
**     either expressed or implied, including but not limited to any implied
**     warranties of merchantability and fitness for a particular purpose.
********************************************************************************
************************************************************
****    Cree SiC MOSFET C2M0045170Ddie Spice Library Beta Version
****    Version 1.0 Date: 11-28-2016
************************************************************
****    Revision record
****    Version Beta    Initial Release
****    Version 1       Included model number at subcircuit to avoid library overlapping when two Modfet
models called
********************************************************************************
****NO Parasitics Included
****Tj = Junction Temperature
****Tc = Case Temperature
************************************************************

.subckt C2M0045170Ddie d g s Tj Tc
.param af1=1
xgmos   d1 g1 s1 Tj Tc gmos_C2M0045170D params: af=af1

Ls          s      s1     1f
R_Ls         s      s1     10
Rg          g1     g2     {1.3/af1}
Lg          g      g3     1f
R_Lg         g      g3     10
Ld          d      d3     1f
R_Ld         d      d3     10
B1          d2     d1     I=(V(d2,d1))/((0.0000012457*((V(Tj))**2)+0.0001582286*(V(Tj))+0.02808)+1n)
R_A          d2     d1     1E12
Vgate_s      g3     g2     0
Vdrain_s     d3     d2     0
Gheat        0      Tj     value = {abs((V(d,s)*I(Vdrain_s)))+abs((V(g1,g2)*I(Vgate_s)))}
XCGD         d1     g1     cgdmos_C2M0045170D params: af=af1
CGS          g1     s1     {5000.49p*af1}
CDS          d2     s1     {120p*af1}
D1           s1     d2     bodydiode_C2M0045170D
D2           s1     d2     bodydiode_C2M0045170D
D3           s1     d2     bodydiode_C2M0045170D
R0 N1 Tj 3.55m
R1 N2 N1 10.7m
R2 N3 N2 15.7m
R3 N4 N3 36.6m
R4 N5 N4 19.2m
R5 N6 N5 8.23m
R6 N7 N6 19.9m
R7 N8 N7 20.8m
```

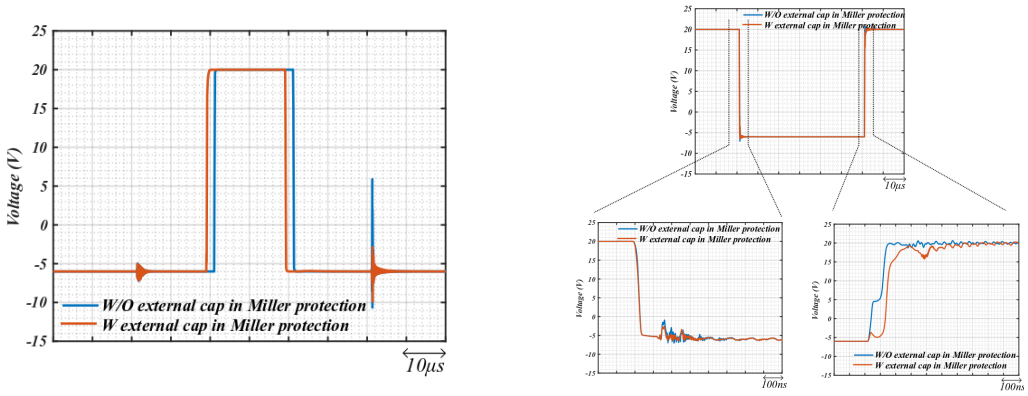
```
R8 N9 N8 32.3m
R9 N10 N9 33.8m
R10 N11 N10 22.1m
R11 N12 N11 10.1m
R12 N13 N12 4.11m
R13 Tc N13 2.79m
C0 Tj Tc 4.89m
C1 N1 Tc 18.3m
C2 N2 Tc 46.3m
C3 N3 Tc 19.1m
C4 N4 Tc 19.8m
C5 N5 Tc 94.3m
C6 N6 Tc 0.149
C7 N7 Tc 0.121
C8 N8 Tc 0.132
C9 N9 Tc 0.121
C10 N10 Tc 0.174
C11 N11 Tc 0.432
C12 N12 Tc 2.04
C13 N13 Tc 28.9

.ends C2M0045170Ddie
****************************************

.subckt gmos_C2M0045170D d1 g2 s1 Tj Tc

.param Adj = 0.56
B2          NET1   0     V=(-0.0070857143*(V(Tj))+13.8924285714)
R_B          NET1   0     1E12
B3          NET2   0     V=((0.0000229873*((V(Tj))**2)-0.0191998834*(V(Tj))+7.1423903627)*Adj)
R_C          NET2   0     1E12
.param p3  = 7.5
.param p4  = 0.0257
.param p5  = 2.1
.param p6  = 2.0
.param p7  = 0.5
.param p8  = 0.001
.param p9  = {2*p3*p4}
.param p10 = {p9*p4}
.param p11 = -10
.param p12 = 25

R100 g1 s1     1e9
E100 g1 s1     value = {limit(V(g2,s1),p11,p12)}
G1 d1 s1 value =       {
+     if(V(d1,s1)<0,
+          -p10*V(NET1,0)*((ln(1+exp((v(g1,s1)-V(NET2,0))/p9)))**p5)
+          *(1+p8*v(s1,d1))
+          ,
+          p10*V(NET1,0)*((ln(1+exp((v(g1,s1)-V(NET2,0))/p9)))**p5)
```

```
+		*(1+p8*v(d1,s1))
+		)
+			}
G2 d1 s1 value =	{
+	if(V(d1,s1)<0,
+		p10*V(NET1,0)*((ln(1+exp((v(g1,s1)-V(NET2,0)-p6*(v(s1,d1))**p7)/p9)))**p5)
+		*(1+p8*v(s1,d1))
+		,
+		-p10*V(NET1,0)*((ln(1+exp((v(g1,s1)-V(NET2,0)-p6*(v(d1,s1))**p7)/p9)))**p5)
+		*(1+p8*v(d1,s1))
+		)
+			}

.ends gmos_C2M0045170D
****************************************

.model bodydiode_C2M0045170D d(is=2.8e-10 cjo=875.8p bv=2500 m=0.676 EG=3.26 vj=3.82 n=4.85
+	rs=0.035  trs1=-0.0054642499  trs2=0.000017345606988 Tnom=25
+	tt=15n ibv=500u Xti=10 level=1)
****************************************

.subckt cgdmos_C2M0045170D d2 g
.param k1=1553.65p
.param k2=0.525
.param ka=80.096
.param kb=0.6678
.param kc=5.5277
G11 g d1 value =	{
+		af*k1*(
+		(1+(limit(v(d1,g),0,650))*(1+ka*(1+TANH(kb*V(d1,g)-kc))/2))**-k2
+		)*ddt(v(g,d1))
+			}
R_CGD d1 d2 1e-3
C_CGD g d1 {1p*af}
.ends cgdmos_C2M0045170D
****************************************
```

```
**
**      Release 2.1 notes
**      1.  New models for C3D16065A and C3D30065D
**
**      Release 2.2 notes
**      1.  New C3D12065A diode model
**
**      Release 2.3 notes
**      1.  Fixed reference error in C3D04060E and C3D04065E models
**
**      Release 2.4 notes
**      1.  New C3D 2A models for TO-220 and TO-252 packages
**      2.  New C3D TO-220F models
**********************************************************************************


**********************************************************************************
**      Die Models
**********************************************************************************



.model CPW31700S025B
+       d(
+       level   =       1
+       Is      =       9.45179E-15
+       N       =       1.053344223
+       Eg      =       1.228273985
+       xti     =       0.1
+       Rs      =       0.032
+       trs1    =       0.006966895
+       trs2    =       4.76848E-05
+       Cjo     =       2.10012E-09
+       VJ      =       1.088038868
+       M       =       0.459393913
+       bv      =       3162.765329
+       tbv1    =       -0.000540626
+       tbv2    =       -2.0191E-06
+       tt      =       0
+       )
```

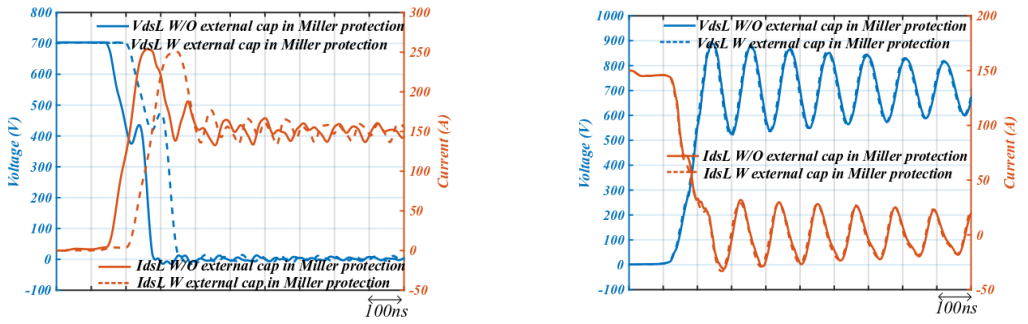
.3

Appendix chapter 4



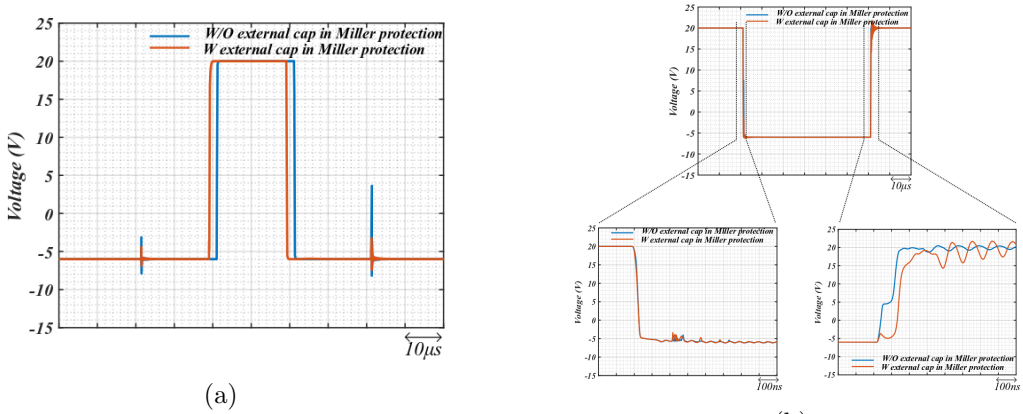
(a) (b)

Figure 5 – Simulation results of comparison between the gate driver with Miller clamp integrated circuit without (W/O) external capacitance and the gate driver with Miller clamp integrated circuit with (W) 40 nF external capacitance, double pulse test, 700 V, 150 A (a) VgsH (b) VgsL.



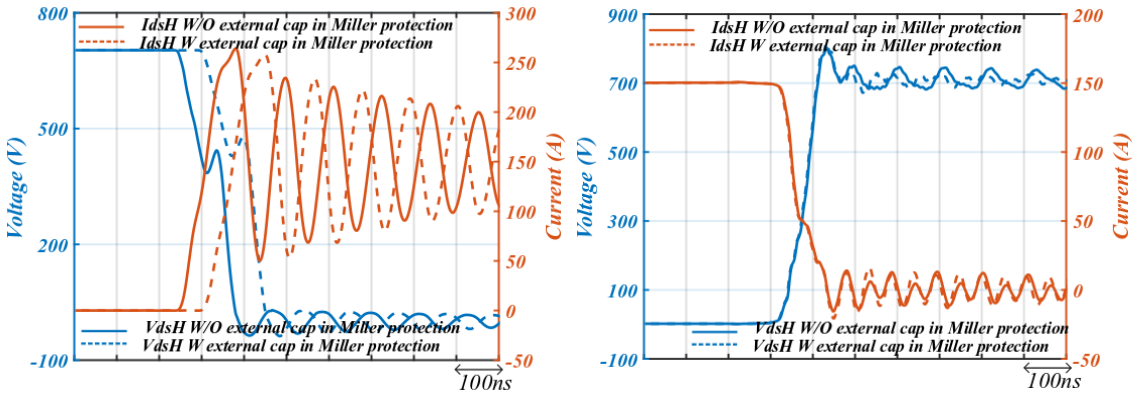
(a) (b)

Figure 6 – Simulation results of comparison between the gate driver with Miller clamp integrated circuit without (W/O) external capacitance and the gate driver with Miller clamp integrated circuit with (W) 40nF external capacitance (a) VdsL Vs. IdsL, on transition (b) VdsL Vs. IdsL, off transition.



(a) (b)

Figure 7 – Simulation results of comparison between the gate driver with Miller clamp integrated circuit without (W/O) external capacitance and the gate driver with Miller clamp integrated circuit with (W) 40nF external capacitance, double pulse test, 700V, 150A (a) VgsL (b) VgsH



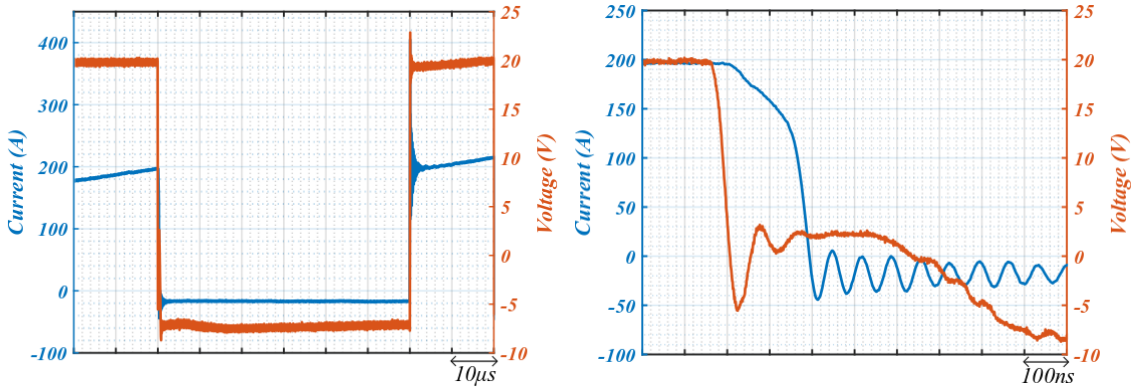
(a) (b)

Figure 8 – Simulation results of comparison between the gate driver with Miller clamp integrated circuit without (W/O) external capacitance and the gate driver with Miller clamp integrated circuit with (W) 40nF external capacitance (a) VdsH Vs. IdsH, on transition (b) VdsH Vs. IdsH, off transition.

.4

Appendix chapter 5

Experimental results illustrate the same switching waveform as it has been presented for the positive current in inductor. It means, during the switching transition, when the high-side switch is in hard switching condition, the rogowski coil has been provided similar voltage to induce to gate path even though the high side switch is not ground reference.



(a) (b)

Figure 9 – VgsH comparison (hard switching), experimental result, double pulse test, 1200V, -200A, Comparison VgsL (W/O) rogowski coil and (W) with rogowski coil integrated to gate driver (a) Switching transition (b) Turn-off transition

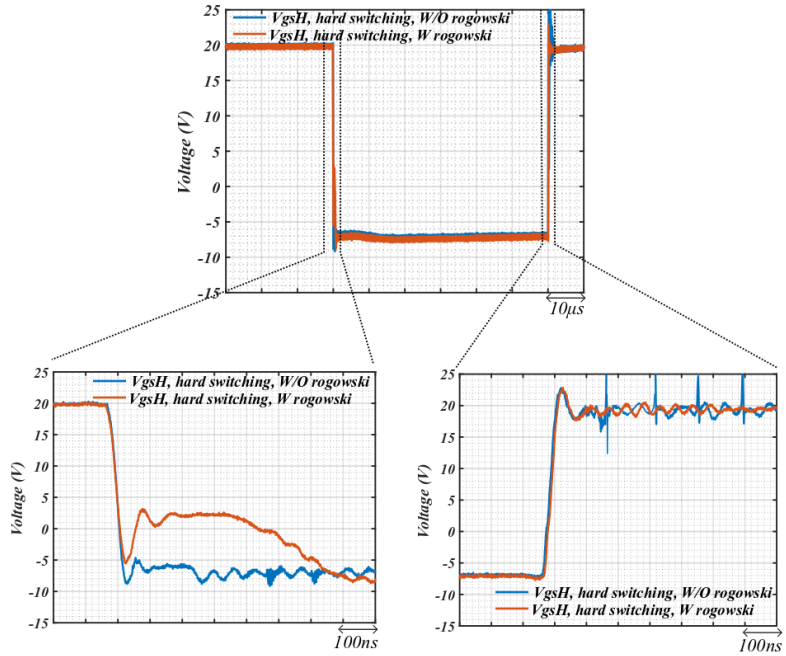
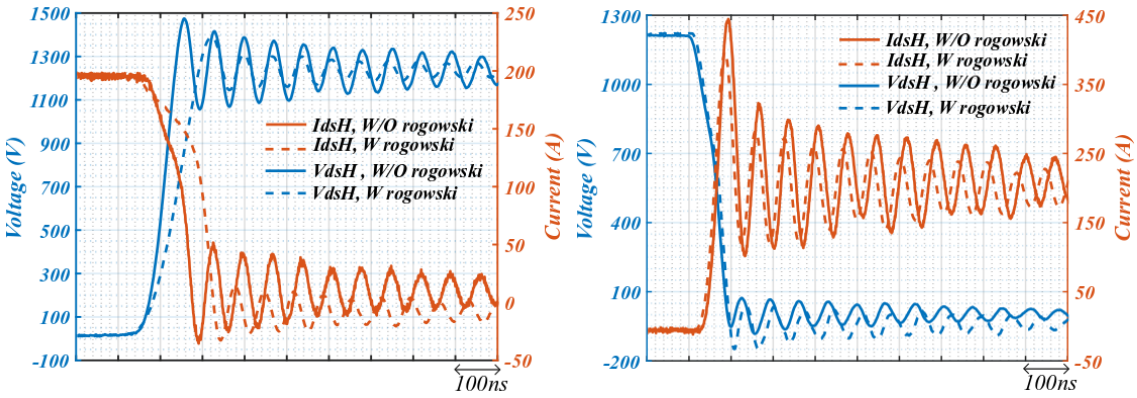
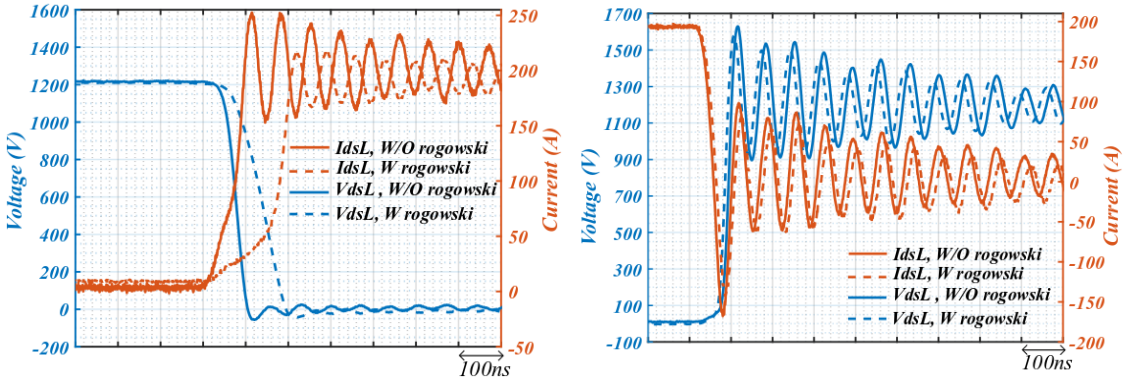


Figure 10 – VgsH comparison (hard switching), experimental result, double pulse test, 1200V, -200A, Comparison VgsL (W/O) rogowski coil and (W) with rogowski coil integrated to gate driver.



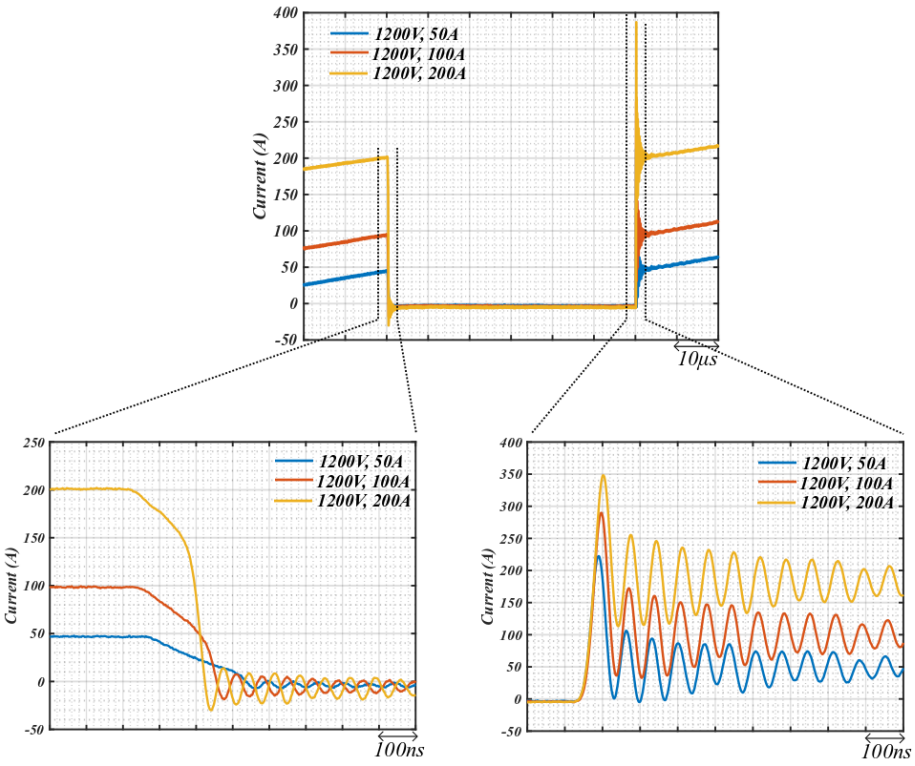
(a) (b)

Figure 11 – VdsH with IdsH (hard switching), double pulse test, experimental result, 1200V, -200A, comparing between (W/O) without rogowski coil and (W) rogowski coil integrated to gate driver (a) Turn-on transition (b) Turn-off transition.

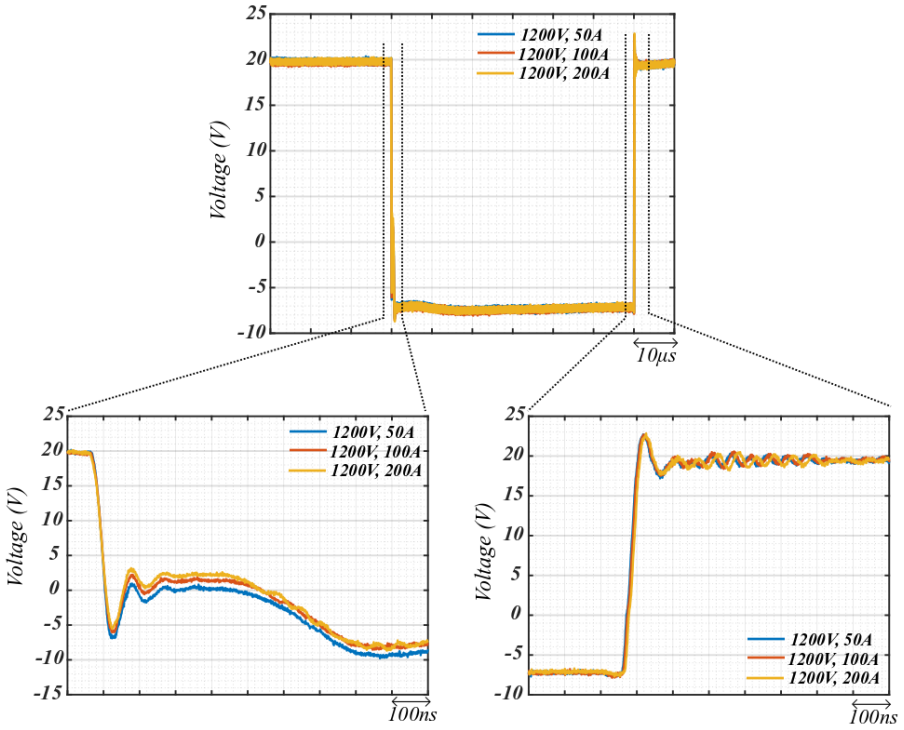


(a) (b)

Figure 12 – VdsL with IdsL (soft switching), double pulse test, experimental result, 1200V, -200A, comparing between (W/O) without rogowski coil and (W) rogowski coil integrated to gate driver (a) Turn-on transition (b) Turn-off transition.

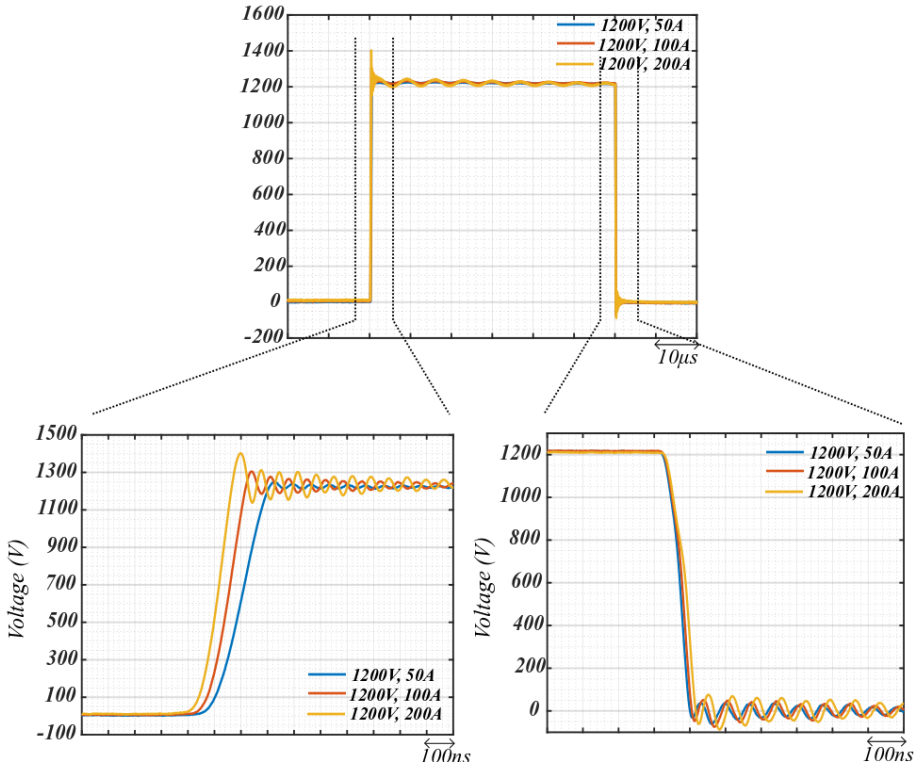


(a)

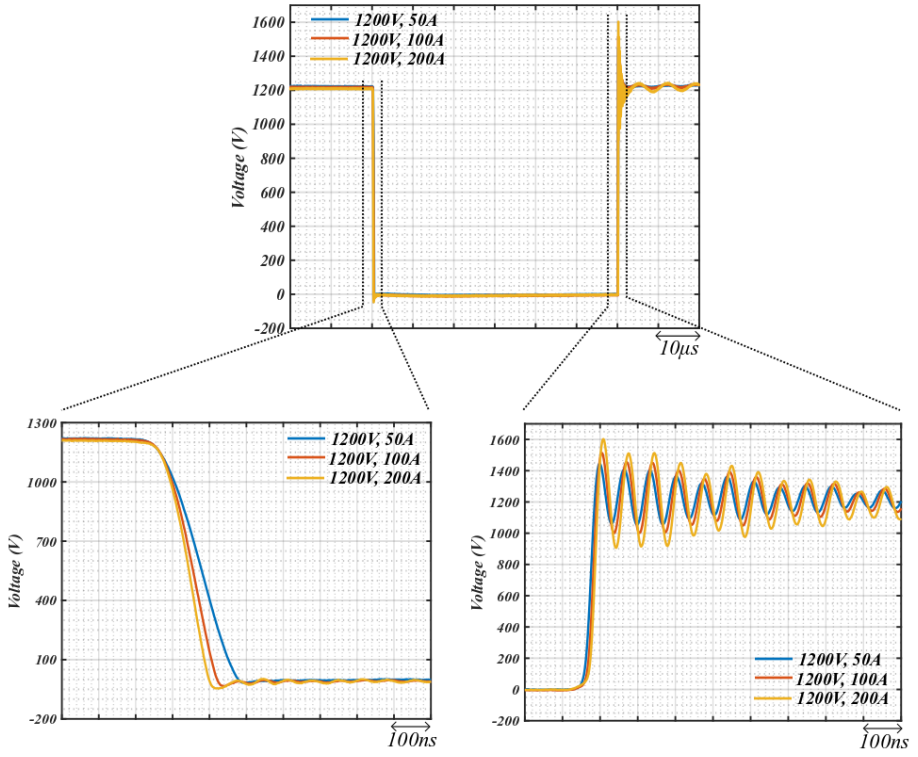


(b)

Figure 13 – IdsH and VgsH, experimental result of gate driver with integrated rogowski coil, double pulse test, 1200V, -50A, -100A, -200A (a) IdsH (b) VgsH.



(a)



(b)

Figure 14 – Vds, experimental result of gate driver with integrated rogowski coil, double pulse test, 1200V, -50A, -100A, -200A (a) VdsL (b) VdsH.

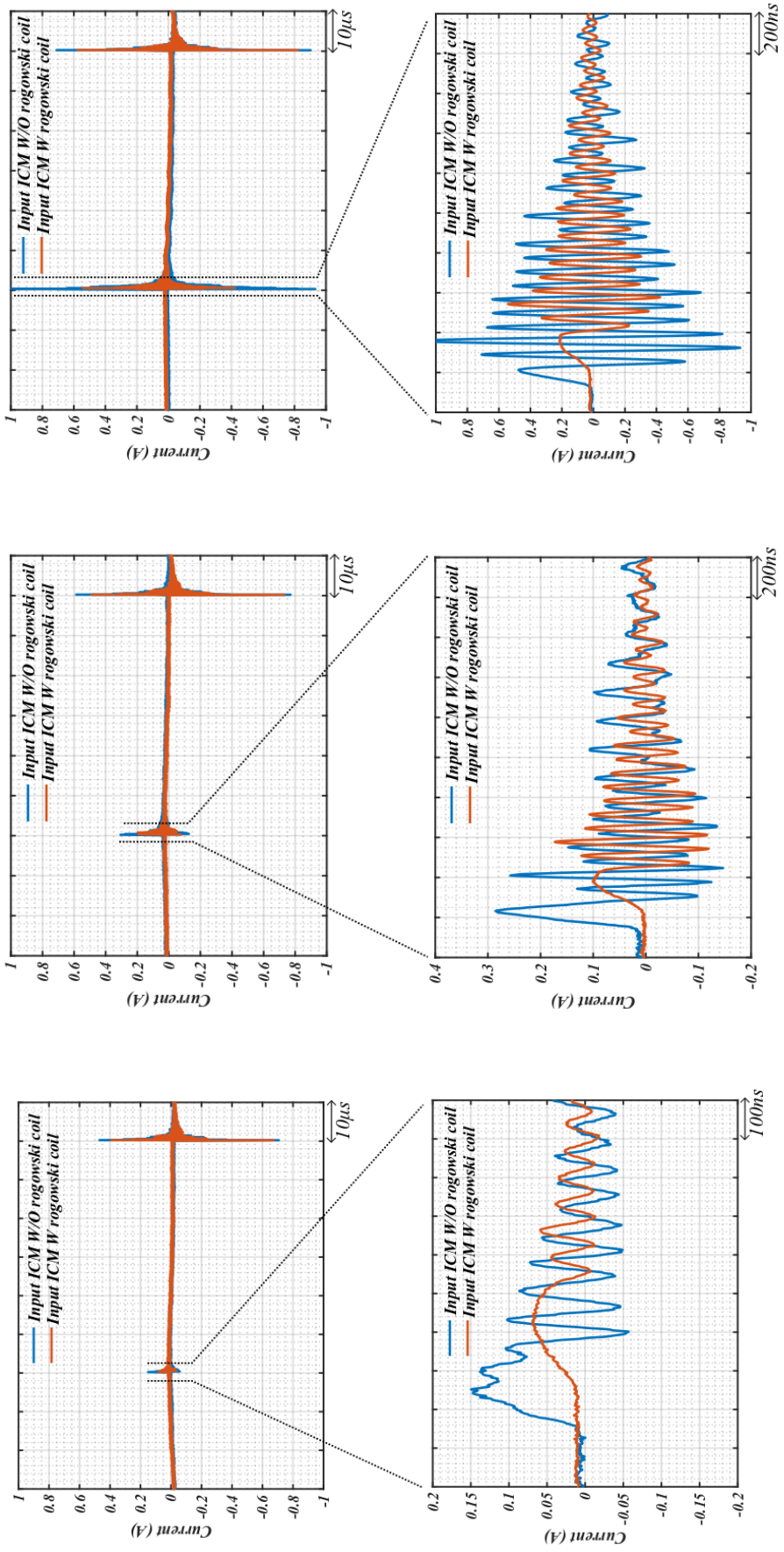


Figure 15 – Experimental Input ICM comparison between the gate driver without (W/O) integrated rogowski coil and with gate driver with (W) integrated rogowski coil, Double pulse test, 1200V (a) -50A (b) -100A (c) -200A.

Bibliography

[1] Ehsan Adib and Hosein Farzanehfard. "Analysis and design of a zero-current switching forward converter with simple auxiliary circuit". In: *IEEE transactions on power electronics* 27.1 (2010), pp. 144–150.

[2] Ehsan Adib and Hosein Farzanehfard. "Family of isolated zero current transition PWM converters". In: *journal of power Electronics* 9.2 (2009), pp. 156–163.

[3] Infineon Technology AG. *FF450R33T33E3 Field stopIGBT3 and Emitter Controlled 3 diode datasheet*. 2018.

[4] A Ahmed et al. "Design and test of a PCB Rogowski coil for very high dI/dt detection". In: *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*. IEEE. 2012, DS1a–2.

[5] M Akhbari, JL Schanen, and R Perret. "Switching cell design with EMC and commutation losses criteria". In: *Conference Record of the 1999 IEEE Industry Applications Conference. Thirty-Forth IAS Annual Meeting (Cat. No. 99CH36370)*. Vol. 2. IEEE. 1999, pp. 1432–1439.

[6] Abdulaziz Alghanem. "Smart Gate Driver Design for Silicon (Si) IGBTs and Silicon-Carbide (SiC) MOSFETs". In: (2016).

[7] Masato Ando and Keiji Wada. "Design of DC-side stray inductance for high speed switching inverter based on normalization procedure". In: *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE. 2015, pp. 2432–2437.

[8] Giulio Antonini, Saverio Cristina, and Antonio Orlandi. "EMC characterization of SMPS devices: circuit and radiated emissions model". In: *IEEE Transactions on Electromagnetic Compatibility* 38.3 (1996), pp. 300–309.

[9] Anup Anurag et al. “Design Considerations and Development of an Innovative Gate Driver for Medium-Voltage Power Devices With High dv/dt”. In: *IEEE Transactions on Power Electronics* 34.6 (2018), pp. 5256–5267.

[10] Brede Arntzen and Dragan Maksimovic. “Switched-capacitor DC/DC converters with resonant gate drive”. In: *IEEE Transactions on Power Electronics* 13.5 (1998), pp. 892–902.

[11] Alex AVRON. *Who really needs GaN or SiC Power Devices*. 2016. URL: `https://www.pntpower.com/question-really-needs-gan-sic-power-devices/`.

[12] Yongjiang Bai et al. “A novel balanced winding topology to mitigate EMI without the need for a Y-capacitor”. In: *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE. 2016, pp. 3623–3628.

[13] Andrew C Baisden, Dushan Boroyevich, and Jacobus Daniel Van Wyk. “High frequency modeling of a converter with an RF-EMI filter”. In: *Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*. Vol. 5. IEEE. 2006, pp. 2290–2295.

[14] Laszlo Balogh. “Design and application guide for high speed MOSFET gate drive circuits”. In: *Power Supply Design Seminar SEM-1400, Topic*. Vol. 2. 2001.

[15] Laszlo Balogh. “Fundamentals of MOSFET and IGBT gate driver circuits”. In: *Texas Instruments–Application report, SLUA618-March* (2017).

[16] F. Blaabjerg et al. “Power Electronics in Renewable Energy Systems”. In: *2006 12th International Power Electronics and Motion Control Conference*. 2006, pp. 1–17.

[17] Frede Blaabjerg et al. “Power electronics in renewable energy systems”. In: *2006 12th International Power Electronics and Motion Control Conference*. IEEE. 2006, pp. 1–17.

[18] Juergen Boehmer, Joerg Schumann, and Hans-Guenter Eckel. “Effect of the miller-capacitance during switching transients of IGBT and MOSFET”. In: *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*. IEEE. 2012, LS6d–3.

[19] Mangesh Borage, Sunil Tiwari, and Swarna Kotaiah. “A passive auxiliary circuit achieves zero-voltage-switching in full-bridge converter over entire conversion range”. In: *IEEE Power Electronics Letters* 3.4 (2005), pp. 141–143.

[20] Frederick Bordry. “Power converters: definitions, classification and converter topologies”. In: (2006).

[21] Alex Van den Bossche and Dimitar Bozalakov. “Two channel high voltage differential probe for power electronics applications”. In: *2013 15th European Conference on Power Electronics and Applications (EPE)*. IEEE. 2013, pp. 1–6.

[22] Alejandro Paredes Camacho et al. “A novel active gate driver for improving SiC MOSFET switching trajectory”. In: *IEEE Transactions on Industrial Electronics* 64.11 (2017), pp. 9032–9042.

[23] M. Cenusa, G. Cretu, and M. Pfost. “Adaptive, Iterative Closed-Loop Control for the Turn-on of IGBTs with Improved Efficiency”. In: *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*. 2016, pp. 1–6.

[24] Marius Cenusa, Gabriel Cretu, and Martin Pfost. “An improved method of controlling IGBT modules using an optimized gate current waveform”. In: *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*. VDE. 2014, pp. 1–6.

[25] Ritwik Chattopadhyay et al. “Modelling, design and analysis of three limb high frequency transformer including transformer parasitics, for SiC Mosfet based three port DAB”. In: *IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society*. IEEE. 2016, pp. 4181–4186.

[26] H. Cheaito et al. “Virtual Bulk Current Injection: Modeling EUT for Several Setups and Quantification of CM-to-DM Conversion”. In: *IEEE Transactions on Electromagnetic Compatibility* 59.3 (2017), pp. 835–844.

[27] Cai Chen et al. “Investigation, evaluation, and optimization of stray inductance in laminated busbar”. In: *IEEE Transactions on power electronics* 29.7 (2013), pp. 3679–3693.

[28] Jian Chen et al. “An RC Snubber Circuit to Suppress False Triggering Oscillation for GaN Based Half-Bridge Circuits”. In: *2019 IEEE 10th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*. IEEE. 2019, pp. 670–673.

[29] Wu Chen, Xinbo Ruan, and Rongrong Zhang. “A novel zero-voltage-switching PWM full bridge converter”. In: *IEEE Transactions on Power Electronics* 23.2 (2008), pp. 793–801.

[30] Zheng Chen, Dushan Boroyevich, and Rolando Burgos. “Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics”. In: *The 2010 International Power Electronics Conference-ECCE ASIA-*. IEEE. 2010, pp. 164–169.

[31] Zheng Chen, Dushan Boroyevich, and Rolando Burgos. “Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics”. In: *The 2010 International Power Electronics Conference-ECCE ASIA-*. IEEE. 2010, pp. 164–169.

[32] Zheng Chen et al. “Modularized design consideration of a general-purpose, high-speed phase-leg PEBB based on SiC MOSFETs”. In: *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*. IEEE. 2011, pp. 1–10.

[33] Yongbin Chu and Shuo Wang. “A generalized common-mode current cancelation approach for power converters”. In: *IEEE Transactions on Industrial Electronics* 62.7 (2015), pp. 4130–4140.

[34] F Costa et al. “An innovative gate drive to control electromagnetic perturbations emitted by a MOSFET chopper”. In: *EPE ‘99, Lausanne* (1999).

[35] F Costa et al. “An innovative gate drive to control electromagnetic perturbations emitted by a MOSFET chopper”. In: *EPE ‘99, Lausanne* (1999).

[36] François Costa and Didier Magnon. “Graphical analysis of the spectra of EMI sources in power electronics”. In: *IEEE Transactions on Power Electronics* 20.6 (2005), pp. 1491–1498.

[37] Francois Costa and Didier Magnon. “Graphical analysis of the spectra of EMI sources in power electronics”. In: *IEEE Transactions on Power Electronics* 20.6 (2005), pp. 1491–1498.

[38] Ian D De Vries. “A resonant power MOSFET/IGBT gate driver”. In: *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No. 02CH37335)*. Vol. 1. IEEE. 2002, pp. 179–185.

[39] D. Deschrijver et al. “Macromodeling of Multiport Systems Using a Fast Implementation of the Vector Fitting Method”. In: *IEEE Microwave and Wireless Components Letters* 18.6 (2008), pp. 383–385.

[40] Dianbo Fu et al. “Analysis and suppression of conducted EMI emissions for front-end LLC resonant DC/DC converters”. In: *2008 IEEE Power Electronics Specialists Conference*. 2008, pp. 1144–1150.

[41] Piotr Dworakowski et al. “3-phase medium frequency transformer for a 100kW 1.2 kV 20kHz Dual Active Bridge converter”. In: *IECON 2019-45th Annual Conference of the IEEE Industrial Electronics Society*. Vol. 1. IEEE. 2019, pp. 4071–4076.

[42] Wilson Eberle, Yan-Fei Liu, and Paresh C Sen. “A new resonant gate-drive circuit with efficient energy recovery and low conduction loss”. In: *IEEE Transactions on Industrial Electronics* 55.5 (2008), pp. 2213–2221.

[43] Wilson Eberle et al. “A current source gate driver achieving switching loss savings and gate energy recovery at 1-MHz”. In: *IEEE Transactions on Power Electronics* 23.2 (2008), pp. 678–691.

[44] M. Ebli, M. Wattenberg, and M. Pfost. “A gate driver approach enabling switching loss reduction for hard-switching applications”. In: *2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS)*. 2017, pp. 968–971.

[45] Michael Ebli and Martin Pfost. “A gate driver approach using inductive feedback to decrease the turn-on losses of power transistors”. In: *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. VDE. 2018, pp. 1–6.

[46] Michael Ebli and Martin Pfost. “A novel gate driver approach using inductive feedback to increase the switching speed of power semiconductor devices”. In: *2017 19th European Conference on Power Electronics and Applications (EPE’17 ECCE Europe)*. IEEE. 2017, P–1.

[47] J. Fabre and P. Ladoux. “Design of a high-power Multilevel Chopper with 1700 V / 300 a SiC MOSFET half-bridge modules”. In: *2016 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*. 2016, pp. 163–169.

[48] L Ferrer et al. “Modelling of differential mode conducted EMI generated by switched power inverters”. In: *IECON’03. 29th Annual Conference of the IEEE Industrial Electronics Society (IEEE Cat. No. 03CH37468)*. Vol. 3. IEEE. 2003, pp. 2312–2315.

[49] Mikaël Foissac, Jean-Luc Schanen, and Christian Vollaire. ““Black box” EMC model for power electronics converter”. In: *2009 IEEE Energy Conversion Congress and Exposition*. IEEE. 2009, pp. 3609–3615.

[50] Mikaël Foissac et al. “System simulation for EMC network analysis”. In: *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE. 2011, pp. 457–462.

[51] Dianbo Fu et al. “Analysis and suppression of conducted EMI emissions for front-end LLC resonant DC/DC converters”. In: *2008 IEEE Power Electronics Specialists Conference*. IEEE. 2008, pp. 1144–1150.

[52] Dianbo Fu et al. “Novel techniques to suppress the common-mode EMI noise caused by transformer parasitic capacitances in DC–DC converters”. In: *IEEE Transactions on industrial electronics* 60.11 (2012), pp. 4968–4977.

[53] Hideaki Fujita. “A resonant gate-drive circuit capable of high-frequency and high-efficiency operation”. In: *IEEE transactions on Power Electronics* 25.4 (2009), pp. 962–969.

[54] Tsuyoshi Funaki. “A study on self turn-on phenomenon in fast switching operation of high voltage power MOSFET”. In: *2013 3rd IEEE CPMT Symposium Japan*. IEEE. 2013, pp. 1–4.

[55] Feng Gao et al. “A gate driver of SiC MOSFET for suppressing the negative voltage spikes in a bridge circuit”. In: *IEEE Transactions on Power Electronics* 33.3 (2017), pp. 2339–2353.

[56] Hadiseh Geramirad et al. “Experiemental study of the self-disturbance phenomena in a half-bridge configuration of SiIGBT and SiC MOSFET switches, PCIM 2020 (in press)”. 2020.

[57] Dominic Gerber, Thomas Guillod, and Jürgen Biela. “IGBT gate-drive with PCB Rogowski coil for improved short circuit detection and current turn-off capability”. In: *2011 IEEE Pulsed Power Conference*. IEEE. 2011, pp. 1359–1364.

[58] L. Ghossein et al. “State of the Art of Gate-Drive Power Supplies for Medium and High Voltage Applications”. In: *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. 2016, pp. 1–8.

[59] Daniel Gómez et al. “Requirements for interconnection of HVDC links with DC-DC converters”. In: *IECON 2019-45th Annual Conference of the IEEE Industrial Electronics Society*. Vol. 1. IEEE. 2019, pp. 4854–4860.

[60] Jose Ortiz Gonzalez and Olayiwola Alatise. “Crosstalk in SiC Power MOSFETs for Evaluation of Threshold Voltage Shift Caused by Bias Temperature Instability”. In: *2019 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)*. IEEE. 2019, P–1.

[61] Michael Grubmüller, Bernhard Schweighofer, and Hannes Wegleiter. “Development of a differential voltage probe for measurements in automotive electric drives”. In: *IEEE transactions on industrial electronics* 64.3 (2016), pp. 2335–2343.

[62] Thomas Guillod et al. “Design of a PCB Rogowski Coil based on the PEEC Method”. In: *2012 7th International Conference on Integrated Power Electronics Systems (CIPS)*. IEEE. 2012, pp. 1–6.

[63] Srinivas Gulur, Vishnu Mahadeva Iyer, and Subhashish Bhattacharya. “Improved Common Mode Noise Models for Three Level T-Type Neutral Point Clamped Converters”. In: *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE. 2018, pp. 6398–6403.

[64] B. Gustavsen. “Improving the pole relocating properties of vector fitting”. In: *IEEE Transactions on Power Delivery* 21.3 (2006), pp. 1587–1592.

[65] B. Gustavsen and A. Semlyen. “Rational approximation of frequency domain responses by vector fitting”. In: *IEEE Transactions on Power Delivery* 14.3 (1999), pp. 1052–1061.

[66] Djilali Hamza and Praveen K Jain. “Conducted EMI noise mitigation in DC-DC converters using active filtering method”. In: *2008 Ieee Power Electronics Specialists Conference*. IEEE. 2008, pp. 188–194.

[67] Karsten Handt et al. “Fully digitally controlled gate drive unit for high power IGBTs”. In: *Proc. PCIM Europe, Nuremberg, Germany* (2012).

[68] Allen R Hefner. “An improved understanding for the transient operation of the power insulated gate bipolar transistor (IGBT)”. In: *20th Annual IEEE Power Electronics Specialists Conference*. IEEE. 1989, pp. 303–313.

[69] Robert Hemmer. “Intelligent IGBT drivers with exceptional driving and protection features”. In: *2009 13th European Conference on Power Electronics and Applications*. IEEE. 2009, pp. 1–4.

[70] P. Hillenbrand et al. “Frequency domain EMI-simulation and resonance analysis of a DCDC-converter”. In: *2016 International Symposium on Electromagnetic Compatibility - EMC EUROPE*. 2016, pp. 176–181.

[71] P Hillenbrand et al. “Understanding conducted emissions from an automotive inverter using a common-mode model”. In: *2015 IEEE International Symposium on Electromagnetic Compatibility (EMC)*. IEEE. 2015, pp. 685–690.

[72] Nadir Idir, Robert Bausiere, and Jean Jacques Franchaud. “Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors”. In: *IEEE Transactions on Power Electronics* 21.4 (2006), pp. 849–855.

[73] Tektronix Inc. *ABC of Probes: A Primer*. Tech. rep.

[74] Hiroki Ishibashi et al. “An analysis of false turn-on mechanism on high-frequency power devices”. In: *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE. 2015, pp. 2247–2253.

[75] Masanori Ishigaki and Hideaki Fujita. “A resonant gate-drive circuit capable of high-frequency and high-efficiency operation”. In: *IEEJ Transactions on Industry Applications* 127 (2007), pp. 1090–1096.

[76] Saeed Jahdi et al. “Temperature and switching rate dependence of crosstalk in Si-IGBT and SiC power modules”. In: *IEEE Transactions on Industrial Electronics* 63.2 (2015), pp. 849–863.

[77] Meng Jin, Ma Weiming, and Zhang Lei. “Determination of noise source and impedance for conducted EMI prediction of power converters by lumped circuit models”. In: *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No. 04CH37551)*. Vol. 4. IEEE. 2004, pp. 3028–3033.

[78] Ari Kahan. *EIA projects nearly 502050, led by growth in Asia*. 2019. URL: `https://www.eia.gov/todayinenergy/detail.php?id=41433`.

[79] MN Kheraluwala et al. “Performance characterization of a high-power dual active bridge DC-to-DC converter”. In: *IEEE Transactions on industry applications* 28.6 (1992), pp. 1294–1301.

[80] M. Koga et al. “Application-specific micro Rogowski coil for power modules - Design tool, novel coil pattern and demonstration”. In: *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*. 2016, pp. 1–5.

[81] Pengju Kong and Fred C Lee. “Transformer structure and its effects on common mode EMI noise in isolated power converters”. In: *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE. 2010, pp. 1424–1429.

[82] Florian Krismer. “Modeling and optimization of bidirectional dual active bridge DC-DC converter topologies”. PhD thesis. ETH Zurich, 2010.

[83] H. Kuhn, T. Koneke, and A. Mertens. “Considerations for a Digital Gate Unit in high power applications”. In: *2008 IEEE Power Electronics Specialists Conference*. 2008, pp. 2784–2790.

[84] N Vijaya Kumar and N Lakshminarasamma. “Comparison of Planar Transformer Architectures and Estimation of Parasitics for High Voltage Low Power DC-DC Converter”. In: *2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*. IEEE. 2018, pp. 1–6.

[85] Saurabh Kumar, Sai Kiran Voruganti, and Ghanshyamsinh Gohil. “Common-mode Current Analysis and Cancellation Technique for Dual Active Bridge Converter based DC System”. In: *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, pp. 6949–6956.

[86] Vinod Kumar et al. *Power Electronics, Drives, and Advanced Applications*. CRC Press, 2020.

[87] T. Lagier, P. Ladoux, and P. Dworakowski. “Potential of silicon carbide MOSFETs in the DC/DC converters for future HVDC offshore wind farms”. In: *High Voltage* 2.4 (2017), pp. 233–243.

[88] Thomas Lagier. “Etude des macromolécules de lixiviat: caractérisation et comportement vis-à-vis des métaux”. PhD thesis. Poitiers, 2000.

[89] Thomas Lagier and Philippe Ladoux. “Theoretical and experimental analysis of the soft switching process for SiC MOSFETs based Dual Active Bridge converters”. In: *2018 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*. IEEE. 2018, pp. 262–267.

[90] Thomas Lagier et al. “A 100 kW 1.2 kV 20 kHz DC-DC converter prototype based on the Dual Active Bridge topology”. In: *2018 IEEE International Conference on Industrial Technology (ICIT)*. IEEE. 2018, pp. 559–564.

[91] Guixing Lan, Siliang Zhang, and Xinke Wu. “Analysis and reduction of common mode current of the transformer in a full-bridge LLC battery charger”. In: *2017 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific)*. IEEE. 2017, pp. 1–5.

[92] J. Le Leslé et al. “Multi-objective optimisation of a bidirectional single-phase grid connected AC/DC converter (PFC) with two different modulation principles”. In: *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2017, pp. 5298–5305.

[93] J. Le Leslé et al. “Optimum design of a single-phase Power Pulsating Buffer (PPB) with PCB-integrated inductor technologies”. In: *2018 IEEE International Conference on Industrial Technology (ICIT)*. 2018, pp. 782–787.

[94] J. Le Lesle et al. “Optimisation of an Integrated Bidirectional Interleaved Single-Phase Power Factor Corrector”. In: *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. 2018, pp. 1–8.

[95] Liang Wang et al. “High-frequency solid-state transformer power conversion technologies for energy internet”. In: *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*. 2017, pp. 1397–1401.

[96] Carmelo Licitra et al. “A new driving circuit for IGBT devices”. In: *IEEE transactions on power electronics* 10.3 (1995), pp. 373–378.

[97] B-R Lin, Kevin Huang, and David Wang. “Analysis and implementation of full-bridge converter with current doubler rectifier”. In: *IEE Proceedings-Electric Power Applications* 152.5 (2005), pp. 1193–1202.

[98] Jianwei Liu et al. “Fast prediction for conducted EMI in flyback converters”. In: *2015 IEEE International Conference on Computational Electromagnetics*. IEEE. 2015, pp. 247–249.

[99] Qian Liu, Fei Wang, and Dushan Boroyevich. “Modular-terminal-behavioral (MTB) model for characterizing switching module conducted EMI generation in converter systems”. In: *IEEE Transactions on power electronics* 21.6 (2006), pp. 1804–1814.

[100] Y. Lobsiger and J. W. Kolar. “Stability and robustness analysis of d/dt-closed-loop IGBT gate drive”. In: *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2013, pp. 2682–2689.

[101] Y Lobsiger and JW Kolar. “Closed-Loop di/dt and dv/dt IGBT Gate Drive Concepts”. In: *ed. ETH Zurich, Switzerland: Power Electronic Systems Laboratory* (2013).

[102] Yanick Lobsiger. “Closed-Loop IGBT Gate Drive and Current Balancing Concepts”. PhD thesis. ETH Zurich, 2014.

[103] Yanick Lobsiger and Johann W Kolar. “Closed-loop IGBT gate drive featuring highly dynamic di/dt and dv/dt control”. In: *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE. 2012, pp. 4754–4761.

[104] D. Maksimovic and S. Dhar. “Switched-capacitor DC-DC converters for low-power on-chip applications”. In: *30th Annual IEEE Power Electronics Specialists Conference. Record. (Cat. No.99CH36321)*. Vol. 1. 1999, 54–59 vol.1.

[105] Alinaghi Marzoughi. “Investigating Impact of Emerging Medium-Voltage SiC MOSFETs on Medium-Voltage High-Power Applications”. PhD thesis. Virginia Tech, 2018.

[106] Takashi Masuzawa et al. “Modeling method of stray magnetic couplings in an EMC filter for a SiC solar inverter”. In: *2014 International Power Electronics Conference (IPEC-Hiroshima 2014-ECCE ASIA)*. IEEE. 2014, pp. 2366–2371.

[107] Zichen Miao et al. “Package influence on the simulated performance of 1.2 kV SiC modules”. In: *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. IEEE. 2015, pp. 306–311.

[108] Loïc Michel et al. “FPGA implementation of an optimal IGBT gate driver based on Posicast control”. In: *IEEE transactions on power electronics* 28.5 (2012), pp. 2569–2575.

[109] M. Miloudi et al. “Analysis and reduction of common-mode and differential-mode EMI noise in a Flyback switch-mode power supply (SMPS)”. In: *2012 20th Telecommunications Forum (TELFOR)*. 2012, pp. 1080–1083.

[110] Slavko Mocevic et al. “Phase current sensor and short-circuit detection based on rogowski coils integrated on gate driver for 1.2 kv sic mosfet half-bridge module”. In: *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE. 2018, pp. 393–400.

[111] Katsuaki Murata and Koosuke Harada. “A self turn-on mechanism of the synchronous rectifier in a DC-DC converter”. In: *INTELEC 2004. 26th Annual International Telecommunications Energy Conference*. IEEE. 2004, pp. 642–646.

[112] Katsuaki Murata, Koosuke Harada, and Tsuyoshi Harimoto. “Self turn-on loss of MOSFET as synchronous rectifier in DC/DC buck converter-in case of a low driving impedance”. In: *2008 IEEE Power Electronics Specialists Conference*. IEEE. 2008, pp. 3348–3353.

[113] RT Naayagi. “Electromagnetic compatibility issues of dual active bridge DC-DC converter”. In: *2013 International Conference on Energy Efficient Technologies for Sustainability*. IEEE. 2013, pp. 699–703.

[114] MH Nagrial and A Hellany. “Radiated and conducted EMI emissions in switch mode power supplies (SMPS): sources, causes and predictions”. In: *Proceedings. IEEE International Multi Topic Conference, 2001. IEEE INMIC 2001. Technology for the 21st Century.* IEEE. 2001, pp. 54–61.

[115] Alireza Nami and Hamed Nademi. “Modular multilevel converter (MMC) and its control”. In: *Control of Power Electronic Converters and Systems*. Elsevier, 2018, pp. 141–166.

[116] Parthasarathy Nayak et al. “Study of the effects of parasitic inductances and device capacitances on 1200 V, 35 A SiC MOSFET based voltage source inverter design”. In: *2014 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*. IEEE. 2014, pp. 1–6.

[117] Simon Niedzwiedz and Stephan Frei. “Transient emission analysis of EV-and HEV-powertrains using simulation”. In: *2013 International Symposium on Electromagnetic Compatibility*. IEEE. 2013, pp. 247–252.

[118] Jukkrit Noppakunkajorn, Di Han, and Bulent Sarlioglu. “Analysis of high-speed PCB with SiC devices by investigating turn-off overvoltage and interconnection inductance influence”. In: *IEEE Transactions on Transportation Electrification* 1.2 (2015), pp. 118–125.

[119] Ko Ogata and Keiji Wada. “Influence of induced voltage noise on switching characteristics for a power converter circuit”. In: *2016 URSI Asia-Pacific Radio Science Conference (URSI AP-RASC)*. IEEE. 2016, pp. 126–129.

[120] Niall Oswald et al. “An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched all-Si, Si-SiC, and all-SiC device combinations”. In: *IEEE Transactions on Power Electronics* 29.5 (2013), pp. 2393–2407.

[121] JD Páez et al. “DC-DC Converters for HVDC Grids: A Survey”. In: *Int. Conf. on Components and Systems for DC grids*. Vol. 9. 2017, pp. 1–14.

[122] P. R. Palmer and H. S. Rajamani. “Active Voltage control of IGBTs for high power applications”. In: *IEEE Transactions on Power Electronics* 19.4 (2004), pp. 894–901.

[123] Alejandro Paredes et al. “A new active gate driver for improving the switching performance of SiC MOSFET”. In: *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE. 2017, pp. 3557–3563.

[124] Alejandro Paredes et al. “A novel active gate driver for silicon carbide MOSFET”. In: *IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society*. IEEE. 2016, pp. 3172–3177.

[125] Alejandro Paredes et al. “Switching trajectory improvement of SiC MOSFET devices using a feedback gate driver”. In: *2018 IEEE International Conference on Industrial Technology (ICIT)*. IEEE. 2018, pp. 847–852.

[126] Drabek Pavel and Kus Vaclav. “EMC issues of power electronic converters”. In: *2009 IEEE International Symposium on Electromagnetic Compatibility*. IEEE. 2009, pp. 296–301.

[127] J. D. Páez et al. “Overview of DC–DC Converters Dedicated to HVdc Grids”. In: *IEEE Transactions on Power Delivery* 34.1 (2019), pp. 119–128.

[128] J. Rabkowski and T. Platek. “Comparison of the power losses in 1700V Si IGBT and SiC MOSFET modules including reverse conduction”. In: *2015 17th European Conference on Power Electronics and Applications (EPE’15 ECCE-Europe)*. 2015, pp. 1–10.

[129] M. M. Rana, R. Rahman, and M. M. Rahman. “Solid State Transformer based on cascade multilevel converter for distribution network”. In: *2016 9th International Conference on Electrical and Computer Engineering (ICECE)*. 2016, pp. 527–529.

[130] Hossein Riazmontazer et al. “Closed-loop control of switching transition of SiC MOSFETs”. In: *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE. 2015, pp. 782–788.

[131] A. R. Rodríguez Alonso et al. “An overall study of a Dual Active Bridge for bidirectional DC/DC conversion”. In: *2010 IEEE Energy Conversion Congress and Exposition*. 2010, pp. 1129–1135.

[132] Miguel Rodríguez et al. “An insight into the switching process of power MOSFETs: An improved analytical losses model”. In: *IEEE Transactions on Power Electronics* 25.6 (2010), pp. 1626–1640.

[133] E. Rondon et al. “Conducted EMC prediction for a power converter with SiC components”. In: *2012 Asia-Pacific Symposium on Electromagnetic Compatibility*. 2012, pp. 281–284.

[134] E. Rondon et al. “Impact of SiC components on the EMC behaviour of a power electronics converter”. In: *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2012, pp. 4411–4417.

[135] E. Rondon-Pinilla et al. “Modeling of a Buck Converter With a SiC JFET to Predict EMC Conducted Emissions”. In: vol. 29. 5. 2014, pp. 2246–2260.

[136] Eliana Rondon-Pinilla. “Conception de convertisseurs électroniques de puissance à faible impact électromagnétique intégrant de nouvelles technologies d’interrupteurs à semi-conducteurs”. PhD thesis. 2014.

[137] Mohammad Ali Saket, Navid Shafiei, and Martin Ordonez. “Planar transformer winding technique for reduced capacitance in LLC power converters”. In: *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE. 2016, pp. 1–6.

[138] Nazmus Sakib, Madhav Manjrekar, and Abasifreke Ebong. “An overview of advances in high reliability gate driving mechanisms for SiC MOSFETs”. In: *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. IEEE, pp. 291–294.

[139] Sanket Sapre. *Isolated Gate Drivers—What, Why, and How*. 2018. URL: `https://www.analog.com/en/analog-dialogue/articles/isolated-gate-drivers-what-why-and-how/`.

[140] Oliver Sartor et al. *EU’s 2030 Climate and Energy Framework and Energy Security*. Climate Strategies., 2014.

[141] Shinji Sato et al. “Forced-air-cooled 10 kW three-phase SiC inverter with output power density of more than 20 kW/L”. In: *Materials Science Forum*. Vol. 679. Trans Tech Publ. 2011, pp. 738–741.

[142] G Schmitt, R Kennel, and J Holtz. “Voltage gradient limitation of IGBTs by optimised gate-current profiles”. In: *2008 IEEE Power Electronics Specialists Conference*. IEEE. 2008, pp. 3592–3596.

[143] Shaowei Zhen et al. “A high efficiency synchronous buck converter with adaptive dead time control for dynamic voltage scaling applications”. In: *2011 IEEE/IFIP 19th International Conference on VLSI and System-on-Chip*. 2011, pp. 43–48.

[144] Yusuke Sugihara et al. “Analytical investigation on design instruction to avoid oscillatory false triggering of fast switching SiC-MOSFETs”. In: *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE. 2017, pp. 5113–5118.

[145] supergrid. *supergrid institute at a glance*. 2020. URL: https://www.supergrid-institute.com/en/about-us/supergrid-institute-at-a-glance/.

[146] Wenhua TAN. "Modeling and Design of Passive Planar Components for EMI Filters". PhD thesis. L'ECOLE CENTRAL DE LILLE, 2012.

[147] Tektronix. *High-voltage differential probes,* Online. Apr. 2019.

[148] Tektronix. *Isolated measurement system*. Online. Feb. 2018.

[149] Tektronix. *TIVM series IsoVu measurement system*. www.tek.com.

[150] Masahiro Terasaki et al. "Design and analysis for noise suppression of DC/DC converter". In: *2014 IEEE Electrical Design of Advanced Packaging & Systems Symposium (EDAPS)*. IEEE. 2014, pp. 109–112.

[151] Masanori Tsukuda et al. "Micro PCB Rogowski coil for current monitoring and protection of high voltage power modules". In: *Microelectronics Reliability* 64 (2016), pp. 479–483.

[152] Vamshi Krishna M and K. Hatua. "Current controlled active gate driver for 1200V SiC MOSFET". In: *2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*. 2016, pp. 1–6.

[153] Mahinda Vilathgamuwa, J Deng, and KJ Tseng. "EMI suppression with switching frequency modulated DC-DC converters". In: *IEEE Industry Applications Magazine* 5.6 (1999), pp. 27–33.

[154] EL Segundo Vrej Barkhordarian International rectifier. *Power MOSFET Basics*. Tech. rep. International Rectifier.

[155] Keiji Wada, Akihiro Hino, and Masato Ando. "High-speed analysis of bus bar inductance for a laminated structure". In: *IEEJ Journal of Industry Applications* 2.4 (2013), pp. 189–194.

[156] Jianjing Wang and Henry Shu-Hung Chung. "A novel RCD level shifter for elimination of spurious turn-on in the bridge-leg configuration". In: *IEEE Transactions on Power Electronics* 30.2 (2014), pp. 976–984.

[157] Jianjing Wang and Henry Shu-Hung Chung. "New insight into the mechanism of the spurious triggering pulse in the bridge-leg configuration". In: *2013 5th International Conference on Power Electronics Systems and Applications (PESA)*. IEEE. 2013, pp. 1–6.

[158] Jianjing Wang, Henry Shu-hung Chung, and River Tin-ho Li. "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance". In: *IEEE Transactions on Power Electronics* 28.1 (2012), pp. 573–590.

[159] Jingang Wang et al. "Design and experimental study of a current transformer with a stacked PCB based on B-dot". In: *Sensors* 17.4 (2017), p. 820.

[160] Jun Wang. "Switching-cycle control and sensing techniques for high-density SiC-based modular converters". PhD thesis. Virginia Tech, 2018.

[161] Jun Wang et al. "A High-Speed Gate Driver with PCB-Embedded Rogowski Switch-Current Sensor for a 10 kV, 240 A, SiC MOSFET Module". In: *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE. 2018, pp. 5489–5494.

[162] Quandi Wang et al. "Parameter extraction of conducted electromagnetic interference prediction model and optimisation design for a DC–DC converter system". In: *IET Power Electronics* 6.7 (2013), pp. 1449–1461.

[163] Y. Wang et al. "Real-time Optimization of IGBT/Diode Cell Switching under Active Voltage Control". In: *Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*. Vol. 5. 2006, pp. 2262–2268.

[164] Zhiqiang Wang et al. "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules". In: *IEEE Transactions on Power Electronics* 29.7 (2013), pp. 3720–3732.

[165] Zhiqiang Wang et al. "Design and performance evaluation of overcurrent protection schemes for silicon carbide (SiC) power MOSFETs". In: *IEEE Transactions on Industrial Electronics* 61.10 (2014), pp. 5570–5581.

[166] WIKIPEDIA. *Electromagnetic compatibility*. 2020. URL: `https://en.wikipedia.org/wiki/Electromagnetic_compatibility#cite_note-1`.

[167] Bjoern Wittig and Friedrich Wilhelm Fuchs. "Analysis and comparison of turn-off active gate control methods for low-voltage power MOSFETs with high current ratings". In: *IEEE Transactions on Power Electronics* 27.3 (2011), pp. 1632–1640.

[168] Cree Wolfspeed. *CAS300M17BM2 Rev. A,1.7kV All-Silicon Carbide Half-Bridge Module datasheet, Rev A*. 2014.

[169] Z. Wong, Y. Chen, and C. Hsu. "Over-current Suppression for Parallel Connected GaN HEMTs". In: *2019 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*. 2019, pp. 1–6.

[170] K Yamaguchi and K Katsura. "Research on optimization design of high efficient low noise SiC-MOSFETs inverters". In: *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*. IEEE. 2015, pp. 1442–1448.

[171] Tatsuya Yanagi, Hirotaka Otake, and Ken Nakahara. "The mechanism of parasitic oscillation in a half bridge circuit including wide band-gap semiconductor devices". In: *2014 IEEE International Meeting for Future of Electron Devices, Kansai (IMFEDK)*. IEEE. 2014, pp. 1–2.

[172] Xin Yang et al. "Robust stability analysis of active voltage control for high-power IGBT switching by Kharitonov's theorem". In: *IEEE transactions on power electronics* 31.3 (2015), pp. 2584–2595.

[173] Xin Yang et al. "Shaping high-power IGBT switching transitions by active voltage control for reduced EMI generation". In: *IEEE Transactions on Industry Applications* 51.2 (2014), pp. 1669–1677.

[174] Zhihua Yang, Sheng Ye, and Yan-Fei Liu. "A new dual-channel resonant gate drive circuit for low gate drive loss and low switching loss". In: *IEEE Transactions on Power Electronics* 23.3 (2008), pp. 1574–1583.

[175] Mohammad Rouhollah Yazdani, Hosein Farzanehfard, and Jawad Faiz. "Classification and comparison of EMI mitigation techniques in switching power converters-A review". In: *Journal of Power Electronics* 11.5 (2011), pp. 767–777.

[176] Shan Yin et al. "A novel gate assisted circuit to reduce switching loss and eliminate shoot-through in SiC half bridge configuration". In: *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE. 2016, pp. 3058–3064.

[177] Youn Hee Lee and A. Nasiri. "Analysis and modeling of conductive EMI noise of power electronics converters in electric and hybrid electric vehicles". In: *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*. 2008, pp. 1952–1957.

[178] Haider Zaman et al. "Suppression of switching crosstalk and voltage oscillations in a SiC MOSFET based half-bridge converter". In: *Energies* 11.11 (2018), p. 3111.

[179] Peroutka Zdenek and Drabek Pavel. “Electromagnetic compatibility issues of variable speed drives”. In: *2002 IEEE International Symposium on Electromagnetic Compatibility*. Vol. 1. IEEE. 2002, pp. 308–313.

[180] B. Zhang and S. Wang. “An Overview of Wide Bandgap Power Semiconductor Device Packaging Techniques for EMI Reduction”. In: *2018 IEEE Symposium on Electromagnetic Compatibility, Signal Integrity and Power Integrity (EMC, SI PI)*. 2018, pp. 297–301.

[181] Huan Zhang et al. “Two-capacitor transformer winding capacitance models for common-mode EMI noise analysis in isolated DC–DC converters”. In: *IEEE Transactions on Power Electronics* 32.11 (2017), pp. 8458–8469.

[182] Lei Zhang et al. “Performance evaluation of high-power SiC MOSFET modules in comparison to Si IGBT modules”. In: *IEEE Transactions on Power Electronics* 34.2 (2018), pp. 1181–1196.

[183] Liqi Zhang et al. “Integrated SiC MOSFET module with ultra low parasitic inductance for noise free ultra high speed switching”. In: *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. IEEE. 2015, pp. 224–229.

[184] Zheyu Zhang et al. “Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration”. In: *IEEE Transactions on Power Electronics* 29.4 (2013), pp. 1986–1997.

[185] Zheyu Zhang et al. “Analysis of the switching speed limitation of wide bandgap devices in a phase-leg configuration”. In: *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE. 2012, pp. 3950–3955.

[186] Zhiliang Zhang, Fei-Fei Li, and Yan-Fei Liu. “A high-frequency dual-channel isolated resonant gate driver with low gate drive loss for ZVS full-bridge converters”. In: *IEEE transactions on power electronics* 29.6 (2013), pp. 3077–3090.

[187] L Zhao, JD Van Wyk, and WG Odendaal. “Planar embedded pick-up coil sensor for power electronic modules”. In: *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC'04.* Vol. 2. IEEE. 2004, pp. 945–951.

[188] Qun Zhao and Goran Stojcic. “Characterization of Cdv/dt induced power loss in synchronous buck dc–dc converters”. In: *IEEE Transactions on Power electronics* 22.4 (2007), pp. 1508–1513.

[189] Qun Zhao and Goran Stojcic. “Characterization of Cdv/dt induced power loss in synchronous buck DC-DC converters”. In: *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC'04.* Vol. 1. IEEE. 2004, pp. 292–297.

[190] Qi Zhou, Feng Gao, and Tao Jiang. “A gate driver of SiC MOSFET with passive triggered auxiliary transistor in a phase-leg configuration”. In: *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE. 2015, pp. 7023–7030.

[191] Yusuke Zushi et al. “A novel gate assist circuit for quick and stable driving of SiC-JFETs in a 3-phase inverter”. In: *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE. 2012, pp. 1734–1739.

[192] I Zverev et al. “Influence of the gate drive techniques on the conducted EMI behavior of a power converter”. In: *PESC97. Record 28th Annual IEEE Power Electronics Specialists Conference. Formerly Power Conditioning Specialists Conference 1970-71. Power Processing and Electronic Specialists Conference 1972*. Vol. 2. IEEE. 1997, pp. 1522–1528.