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# Integration of mid-infrared lasers on silicon photonic integrated circuits

Andres Remis Janez

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**Unité de recherche : Institut d'Électronique et des Systèmes – UMR CNRS 5214**

**Integration of mid-IR lasers on silicon photonic  
integrated circuits**

**Présentée par Andres REMIS**

**Le 4 décembre 2023**

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et Jean-Baptiste RODRIGUEZ**

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# **Integration of mid-IR lasers on silicon photonic integrated circuits**



# Index

LIST OF FIGURES .....	III
LIST OF TABLES .....	VII
LIST OF EQUATIONS .....	VII
INTRODUCTION .....	1
<b>1 CHAPTER 1. STATE OF THE ART AND MOTIVATIONS .....</b>	<b>3</b>
1.1 SILICON PHOTONIC INTEGRATED CIRCUITS .....	3
1.1.1 <i>Photonic integrated circuit</i> .....	3
1.1.2 <i>Silicon photonics</i> .....	4
1.2 LIGHT SOURCES .....	5
1.2.1 <i>Group-IV semiconductor lasers</i> .....	5
1.2.2 <i>III-V semiconductor lasers</i> .....	5
1.3 INTEGRATION APPROACHES .....	6
1.3.1 <i>Heterogeneous integration</i> .....	6
1.3.2 <i>Monolithic integration</i> .....	8
1.4 COUPLING CONFIGURATIONS .....	10
1.5 APPLICATIONS OF SI PICs .....	12
1.5.1 <i>Optical sensing in the mid-infrared</i> .....	12
1.5.2 <i>Mid-IR lasers</i> .....	13
1.6 CONCLUSION .....	17
<b>2 CHAPTER 2. DISCRETE GASB-BASED DIODE LASERS GROWN ON GASB AND SI SUBSTRATES .....</b>	<b>19</b>
2.1 DIODE LASER HETEROSTRUCTURE .....	19
2.2 MBE GROWTH .....	21
2.3 LASER FABRICATION PROCESS .....	22
2.3.1 <i>Laser ridge</i> .....	23
2.3.2 <i>Bottom contact etching</i> .....	24
2.3.3 <i>Dielectric deposition and opening</i> .....	25
2.3.4 <i>Metallization</i> .....	25
2.4 LASER CHARACTERIZATIONS .....	27
2.4.1 <i>General aspects of laser characterization</i> .....	27
2.4.2 <i>Laser properties</i> .....	29
2.5 THEORETICAL GAIN MODEL .....	33
2.6 DISCUSSION .....	35
2.7 CONCLUSION .....	37
<b>3 CHAPTER 3. INTEGRATION OF GASB-BASED DIODE LASERS ON A SI PIC .....</b>	<b>38</b>
3.1 CONFIGURATION .....	38
3.2 CHALLENGES .....	39
3.3 ETCHED-FACET DLS .....	41
3.3.1 <i>Fabrication of a smooth and vertical facet</i> .....	42
3.3.2 <i>Process flow of etched-facet DLS</i> .....	50
3.3.3 <i>Characterizations of etched-facet DLS</i> .....	57
3.4 FABRICATION OF SIN-BASED WAVEGUIDES .....	59
3.5 OXIDE REMOVAL FOR LATER GROWTH .....	61
3.5.1 <i>Wet etching</i> .....	62
3.5.2 <i>Dry etching</i> .....	63
3.6 EPITAXIAL GROWTH .....	64



3.7	POLYCRYSTAL REMOVAL .....	67
3.8	LASER PROCESS ON THE SI PIC.....	70
3.8.1	<i>Facet definition</i> .....	71
3.8.2	<i>Ridge definition</i> .....	72
3.8.3	<i>Bottom contact definition</i> .....	73
3.8.4	<i>Insulation and opening</i> .....	73
3.8.5	<i>Metallization</i> .....	74
3.8.6	<i>Substrate thin-down and cleavage</i> .....	75
3.9	CHARACTERIZATIONS OF DLS ON THE RECESSED SI.....	76
3.10	LIGHT COUPLING MEASUREMENT .....	78
3.11	SIMULATIONS .....	81
3.12	CONCLUSION .....	83
<b>4</b>	<b>CHAPTER 4. INCREASING THE COUPLING EFFICIENCY OF THE INTEGRATED GASB DIODE LASERS ON THE SI PIC .....</b>	<b>86</b>
4.1	FILLING THE GAP .....	86
4.1.1	<i>Simulations</i> .....	86
4.1.2	<i>Filling the gap with PMMA</i> .....	90
4.2	LASER PROCESS OPTIMIZATION TO REDUCE THE GAP .....	91
4.2.1	<i>Polycrystal removal optimization</i> .....	91
4.2.2	<i>Laser facet definition</i> .....	92
4.2.3	<i>Thin III-V peak removal</i> .....	93
4.3	ALTERNATIVE APPROACHES .....	95
4.3.1	<i>Waveguide fabrication on etched-facet laser by e-beam evaporation</i> .....	95
4.3.1	<i>Waveguide fabrication on etched-facet laser by PECVD</i> .....	97
4.4	CONCLUSION .....	103
	<b>GENERAL CONCLUSION AND PERSPECTIVES.....</b>	<b>106</b>
<b>5</b>	<b>APPENDIX .....</b>	<b>110</b>
5.1	TYPE-I QUANTUM WELL DIODE LASERS .....	110
5.2	PROCESS TECHNIQUES.....	112
5.2.1	<i>UV photolithography</i> .....	112
5.2.2	<i>ICP etching</i> .....	114
5.2.3	<i>PECVD</i> .....	114
5.2.4	<i>Electron beam evaporation</i> .....	115
	<b>REFERENCES.....</b>	<b>116</b>
	<b>LIST OF PUBLICATIONS.....</b>	<b>124</b>

# List of figures

Figure 1. Representation of a Silicon photonic chip.[15].....	4
Figure 2. Transmission window of different waveguide materials. The white areas are the wavelength range over which waveguide propagation loss is less than 2 dB/cm. The orange areas are the wavelength range over which loss is high.[8] .....	5
Figure 3. Energy band structure of GaAs, an example of direct bandgap. ....	6
Figure 4. III-V-on-Si heterogeneous integration approaches. a) Wafer-bonding. b) Flip-chip integration. c) Micro-transfer printing.[39] .....	7
Figure 5. a) Silicon crystal structure. b) III-V crystal structure. c) Sketch of a V-polar domain and a III-polar domain separated by the antiphase boundary (III-III and V-V bonds).[59].....	9
Figure 6. Energy gap and wavelength vs. lattice constant for some elementary and binary semiconductor materials. ....	9
Figure 7. TEM pictures of GaSb layer grown on Si substrate where threading dislocations are visible (Courtesy of Karl Graser, PDI Berlin). ....	10
Figure 8. The two main light coupling configurations. a) Evanescent coupling of a III-V laser into a Si waveguide thanks to a taper section.[69] b) Butt-coupling configuration of a laser into a Si waveguide.[72].....	11
Figure 9. a) 2-5- $\mu\text{m}$ mid-IR spectrum.[79] b) Mid-IR sensors applications.[85] .....	13
Figure 10. Band structure alignments for a selection of unstrained III-V binaries at 300 K.[88] .....	14
Figure 11. Band alignments and recombination mechanisms of QW diode lasers, interband cascade lasers and quantum cascade lasers.....	14
Figure 12. L-I-V curves of different types of lasers grown on on-axis Si substrates. a) ICL. b) QCL. c) DL. [62]–[64].....	15
Figure 13. Threshold current densities vs. wavelength of different types of mid-IR lasers.[81] .....	16
Figure 14. Structure design of the diode lasers grown on a) GaSb substrates and on b) Si substrates containing different number of QWs in the active zones for each substrate (1-4 QWs). ....	20
Figure 15. Band structure details of the design for a DL grown on Si. a) A band structure detail for the entire structure. b) A band structure detail for the QWs[62].....	21
Figure 16. a) 20x20 $\mu\text{m}^2$ AFM image of the 2-QWs laser surface. b) Omega-2theta high-resolution X-ray diffraction scan of the same laser. ....	22
Figure 17. Sketch of the final device after processing. a) DL on native GaSb substrate. b) DL on Si substrate. ....	23
Figure 18. Tracking signal of the etching for the whole heterostructure: reflectance vs. etching time. ....	24
Figure 19. Sketch of the fabrication step of the laser ridge.....	24
Figure 20. Sketch of the fabrication process of DLs on Si. ....	26
Figure 21. Representation of a L-I-V curve from a laser characterization. ....	27
Figure 22. Broad-area laser characteristics in pulsed operation for the two series. Light output versus current density curves of 1.5 mm-long DLs with different numbers of QW. ....	30
Figure 23. Broad-area laser characteristics in pulsed operation for the two series. Threshold current density versus the number of QWs for different cavity lengths.....	31
Figure 24. L-I-V data in CW for 1-QW DLs with an 8 $\mu\text{m}$ -wide ridge and different cavity lengths. a) On Si substrate. b) On GaSb substrate. ....	31
Figure 25. Extracted internal losses versus the number of QWs for the two series. ....	32
Figure 26. L-I data for 2-QWs DLs on Si and GaSb with a 10- $\mu\text{m}$ wide ridge and 1-mm long cavity for different measurement temperatures.....	33
Figure 27. Fits of the threshold current density for the two series for the 1.5-mm long DLs.....	35

Figure 28. The gain model calculations for the two series. (a) Modal gain vs current density curves for different number of QWs. (b) The optimal number of QWs vs the total optical losses.....	36
Figure 29. a) Cross-section and b) 3D sketch of an integrated GaSb DL on a Si PIC with light coupled from the active zone of the DL to the core of the waveguide. ....	39
Figure 30. Cross-section sketch of challenging fabrication steps of the integration of the DL on the Si PIC in order to couple light from the active zone of the DL to the core of the SiN waveguide. ....	40
Figure 31. Light beam output of a DL taken with an IR camera.[119] .....	41
Figure 32. Cross-section sketch of the effect of the air gap on the light coupling. ....	41
Figure 33. Resist profile after a standard lithography using a) soft contact and b) vacuum contact....	43
Figure 34. SEM image of the chromium mask used during photolithography.[119] .....	44
Figure 35. Sketch of the influence of the hard bake on the resist and semiconductor flanks. a) no hard bake is performed. b) hard bake is performed. ....	47
Figure 36. Sketch of the fabrication of a hard mask. ....	47
Figure 37. SEM image of the semiconductor flank using SiN hard mask with no hard bake of the resist. ....	48
Figure 38. SEM image of the semiconductor flank using SiN mask and a hard bake at 110°C during 4 minutes.....	49
Figure 39. Mask design of the laser facet. ....	50
Figure 40. ICP etching tracking signal.....	51
Figure 41. SEM images of the laser facet. ....	51
Figure 42. Mask design of the laser ridge. ....	52
Figure 43. SEM images of the laser ridge definition step. a) after lithography and before ICP etching. b) after ICP etching.....	52
Figure 44. Mask design of the electrical insulation. ....	53
Figure 45. SEM images of the laser facet after the electrical insulation and opening. ....	53
Figure 46. Mask design of the metal deposition.....	54
Figure 47. SEM images of the final device after the metallization step. ....	55
Figure 48. Sketch of the etched-facet DL process flow.....	55
Figure 49. Sketch of the cleavage step. Etched- and cleaved-facet lasers are obtained on the same bar. ....	56
Figure 50. Images of a laser bar with several etched-facet lasers and cleaved lasers. a) optical image. b) SEM image[119]. ....	56
Figure 51. L-I-V curves in CW operation at RT of DLs grown on GaSb substrate with a) cleaved facets and b) etched-facets. ....	57
Figure 52. Threshold current density as a function of the cavity length in CW and RT for etched- and cleaved-facet DLs. ....	58
Figure 53. a) Front and b) cross section view sketch of the SiN WGs fabrication. ....	59
Figure 54. SEM image of the front of the WG.....	60
Figure 55. Schematic of the Si PICs: the pattern of the 100 mm wafers is organized with several 20x20 mm <sup>2</sup> dies, each one containing two recessed areas together with 20 SiN waveguides each one. ....	61
Figure 56. SEM image of the SiN waveguide with a remaining SiO <sub>2</sub> step on the Si substrate. ....	61
Figure 57. Cross-section view sketch of the PIC fabrication. ....	62
Figure 58. SEM images of the removal SiO <sub>2</sub> step attempts with HF solution. a) before etching. b) after 18 minutes etching with a damaged Si substrate. c) zoomed image on the WG stack before etching and d) after etching.....	63
Figure 59. Process sketch of the oxide removal by ICP dry etching. ....	64
Figure 60. SEM images of the SiO <sub>2</sub> step removal by ICP dry etching.....	64
Figure 61. 3D sketch of the epitaxial growth step. ....	65

Figure 62. a) Top view of the die before and after the epitaxial growth. b) high-resolution X-ray diagram measured in the laser growth. c) AFM image taken on top of the laser structure. ....	66
Figure 63. Cross-section SEM image of a similar Si PIC after the epitaxial growth.[119] .....	67
Figure 64. 3D sketch of the polycrystal removal step. ....	67
Figure 65. Different mask protections for the polycrystal removal step. The green rectangles correspond to the resist. ....	68
Figure 66. Pictures of a die before and after the polycrystal removal. ....	69
Figure 67. SEM images of the sample after the polycrystal removal for different masks. a) The protection goes 20 $\mu\text{m}$ into the WG stack, b) 15 $\mu\text{m}$ and c) 10 $\mu\text{m}$ .....	70
Figure 68. Facet definition photolithography using the same parameters as those of discrete etched-facet lasers. ....	71
Figure 69. SEM images of the laser facet definition. a) Top view of the sample after hard mask opening. b) Facet angle measurement after facet etching.....	72
Figure 70. SEM images of the ridge definition step. a) angled view. b) top view. ....	73
Figure 71. SEM image of the bottom contact next to the laser ridge. ....	73
Figure 72. a) SEM and b) optical image of the electrical insulation step.....	74
Figure 73. a) SEM and b) optical images of the device after the metallization step. ....	74
Figure 74. Sketch of the laser process flow on the Si PIC. The different process steps are facet etching, laser ridge, bottom contact, electrical insulation and metallization. ....	75
Figure 75. Images of the final die showing a) the two series of lasers and waveguides and b) the cleavages performed after polishing. ....	76
Figure 76. a) 3D sketch of the final device and DL characterizations. b) Top view image of the bar mounted on a Cu heat sink and measured on a probe station. ....	76
Figure 77. a) L-I-V curves of the DLs on the Si PIC taken in the CW regime at RT for a series of 8 DLs. b) L-I-V curves taken at different temperatures between 20 and 80 C (setup limited) for a typical DL. ..	77
Figure 78. Emission spectrum recorded from the DL at RT in the CW regime at $\sim 2 \times I_{\text{th}}$ drive current. 77	77
Figure 79. 3D sketch of the light coupling characterizations. ....	78
Figure 80. IR image of the laser bar on the probe station with a) zero drive current and b) 250-mA drive current.....	79
Figure 81. IR images at the output of the waveguide with the laser operating at 250 mA. a) front view. b) angled view. ....	79
Figure 82. IR images at the output of the waveguide with the laser operating at 250 mA. a) without the mechanic shield. b) with the mechanic shield.....	80
Figure 83. L-I curves of a DL-WG pair where both laser ridge and WG are 10 $\mu\text{m}$ wide, taken in the CW regime at RT. ....	81
Figure 84. 2D TE mode profiles supported in the DL ridge and in the SiN WG.[70] .....	81
Figure 85. Transmittance as a function of the air gap for different passive core materials.[70] .....	82
Figure 86. Transmittance as a function of the air gap for a SiN/SiO <sub>2</sub> waveguide and for different passive core thicknesses.[70] .....	83
Figure 87. Cross-section sketch of the DL butt-coupled with the WG with a filled gap with a material with a higher refractive index. ....	87
Figure 88. FDTD simulations of the transmittance as a function of the gap size for different gap materials.....	88
Figure 89. a) Threshold current density as a function of the cavity length for different materials filling the gap. b) Threshold current density as a function of the refractive index of the material filling the gap for a cavity length of 1.5 mm with and without HR coating and a cavity length of 3 mm without HR coating. ....	89

Figure 90. Absorption measurement of a PMMA drop as a function of the wavelength with and without a bake. ....	90
Figure 91. a) Optical image of the PMMA drop deposited on the sample. b) L-I curves after filling the gap with PMMA of a DL-WG pair. ....	91
Figure 92. Optimized polycrystal removal step for two different mask alignments resulting in different gaps. ....	92
Figure 93. SEM pictures after the lithography of the laser facet of two samples a) and b) where the gap was reduced. ....	92
Figure 94. SEM images of the samples. a) image after the facet etching, b) after the laser ridge. ....	93
Figure 95. SEM image of the lithography result using the same parameters as the bottom contact etching. ....	94
Figure 96. SEM image of the sample after the III-V peak removal step and before removing the resist. ....	94
Figure 97. Sketch of the process technique to deposit the WG layers by lift-off technique after the DL fabrication. ....	96
Figure 98. SEM images of a first test. a) Resist profile after the lithography. b) Device after the lift-off. ....	97
Figure 99. SEM images of PECVD depositions on a 6.5- $\mu\text{m}$ depth etched facet. a) Deposition of 3.9 $\mu\text{m}$ of $\text{SiO}_2$ . b) Deposition of 0.8 $\mu\text{m}$ of $\text{SiN}$ on top of the 3.9- $\mu\text{m}$ $\text{SiO}_2$ layer. ....	97
Figure 100. Sketch of the process steps to fabricate the WGs integrated with the etched-facet lasers with a $\text{SiO}_2$ gap. ....	98
Figure 101. FDTD simulations of the new configuration. a) with air as the top cladding. b) with 1 $\mu\text{m}$ of $\text{SiO}_2$ as the top cladding. ....	99
Figure 102. SEM images of laser morphology. a) after the etching of the facet. b) after the entire laser process. ....	100
Figure 103. SEM picture of PECVD depositions of $\text{SiO}_2$ and $\text{SiN}$ depositions on the facet. ....	101
Figure 104. a) Sketch of the WG definition lithography. b) SEM image of the device after the WG definitions step. ....	101
Figure 105. Mask design of the waveguide and laser ridge definition. The laser ridge mask has a T-shape close to the laser facet to push the corners away. ....	102
Figure 106. SEM image of the device after the ridge definition. ....	102
Figure 107. Images of the final device after the metallization step. a) SEM image. b) optical image. ....	103
Figure 108. Different transition process of a semiconductor material interacting with a photon: absorption, spontaneous emission and stimulated emission. ....	111
Figure 109. Sketch of the resist spread evenly over the surface of the sample after spin coating. ....	113
Figure 110. Sketch of the sample brought into contact with the mask and exposed to UV light. ....	113
Figure 111. Sketch of the sample after development. a) In the case of positive resist. b) In the case of negative resist. ....	113
Figure 112. Sketch of the sample after etching. a) In the case of positive resist. b) In the case of negative resist. ....	114
Figure 113. Sketch of a lift-off technique using electron beam evaporation technique for metal deposition with a) a positive resist profile, b) a negative resist profile, and c) an accentuated negative resist profile. ....	115

# List of tables

Table 1. Parameters of the photolithography of the laser ridge definition. ....	23
Table 2. ICP recipe previously optimized to etch GaSb-based compounds.....	23
Table 3. Lithography parameters of bottom contact etching.....	24
Table 4. Lithography parameters of the metal contact step. ....	25
Table 5. Recombination coefficient values. ....	35
Table 6. SEM pictures of resist flanks after hard bake for different temperatures and times.....	45
Table 7. SEM pictures of semiconductor flanks after hard bake for different temperatures and times and an etching time of 9 minutes. ....	46
Table 8. Hard mask parameters of the facet etching step.....	49
Table 9. Photolithography parameters for the laser ridge definition for the etched-facet process.....	52
Table 10. Photolithography parameters of the metallization step for the etched-facet process.....	54
Table 11. Photolithography parameters of the polycrystal removal step. ....	68
Table 12. Lithography parameters for the facet definition on a Si PIC.....	71
Table 13. Refractive index of different materials under study. ....	82
Table 14. Refractive indices of different materials. ....	87

# List of equations

Equation 1. External quantum efficiency.....	28
Equation 2. The inverse of the external quantum efficiency as a function of the cavity length.....	28
Equation 3. Characteristic temperature related to the threshold current.....	29
Equation 4. Characteristic temperature related to the external quantum efficiency.....	29
Equation 5. Threshold current density.....	33
Equation 6. Fabry-Perot cavity losses. ....	33
Equation 7. Optical gain of a single QW structure. ....	34
Equation 8. Lorentzian function.....	34
Equation 9. Modal gain. ....	34
Equation 10. Current density as a function of the recombination coefficients. ....	34
Equation 11. Modal gain as a function of the current density. ....	34
Equation 12. Threshold current density as a function of the recombination coefficients.....	36
Equation 13. Threshold current density as a function of the inverse of the cavity length. ....	58
Equation 14. Reflectivity at an interface between two media 1 and 2. ....	88
Equation 15. Fabry-Perot cavity losses when the reflectivity of the mirrors is not equal. ....	88
Equation 16. Beer-Lambert law. ....	90
Equation 17. The gain provided by the system is equal to the total optical losses: the laser threshold. .....	111



# Introduction

The miniaturization of electronic chips, guided by Moore's Law, has been a cornerstone of the exponential growth of computing and telecommunications, achieving high levels of performance, low power consumption and reduced manufacturing costs. However, the integration density of transistors is arriving to its limits as the power dissipation in chips and the cost per transistor reach an asymptote.[1], [2] Photonic integration, and in particular silicon photonics, has been considered as one of the most promising solutions to overcome these limitations. By harnessing the properties of light rather than electrons, silicon photonics enables optical components to be integrated alongside electronic circuits on the same chip, taking advantage of the very mature silicon industry and CMOS technology. This approach would enable higher bandwidth, low energy consumption and reduced heat generation, providing a cost-effective solution. Significant advances have been made by researchers and industry leaders. However, one of the major remaining challenges is the realization of highly efficient laser sources on these silicon platforms. Much work has been devoted to address this challenge. In particular, the high efficiencies of III-V semiconductors have led to the demonstration of discrete high-performance lasers grown on their native III-V substrates. The next step is to integrate such lasers onto silicon photonic circuits. The heterogeneous integration consists of growing the III-V material on its native substrate and transferring it to the silicon platform, whereas the monolithic integration is based on the direct epitaxial growth of III-Vs on silicon. Although the heterogeneous integration is the most advanced strategy, the monolithic integration is considered the most promising route to low-cost and high-volume production of silicon photonic chips. However, this approach is still in its infancy and further research is needed. Especially, achieving light coupling between the integrated lasers and passive Si-based waveguides would be a major breakthrough towards the realization of fully integrated silicon photonic chips.

Silicon photonics has expanded beyond datacom/telecom into many other application fields. Of interest, the mid-infrared wavelength range is very attractive as many biological and chemical species exhibit their fingerprint absorption lines at these wavelengths. Optical sensing in the mid-infrared is therefore in high demand for societal, environmental and medical



applications, among others. However, mid-infrared sensors are bulky and expensive because they still rely on discrete devices. Silicon photonics would offer the opportunity to integrate these mid-infrared devices on silicon platforms to achieve miniaturized, robust and low-cost sensors. To develop these mid-infrared sensors, lasers emitting at these wavelengths are required. Among III-V lasers, GaSb-based lasers are capable of covering the mid-infrared spectral range.

The nanoMIR group specializes in antimonide technology (III-Sbs) and has led major research projects on the integration of antimonides on silicon for mid-infrared sensors. It was within this group that I carried out my work. The aim of my PhD is the integration of GaSb-based lasers on silicon photonic integrated circuits. To achieve this goal, I have carried out different investigations, which are described in 4 different chapters.

In the first chapter, I present the context and motivation of my work in more detail, together with the state of the art. I describe the different approaches to integrating III-V lasers on silicon. I then present the different research efforts in the epitaxial growth of III-V materials on silicon that have overcome significant challenges, followed by the various approaches for coupling the lasers to passive waveguides within a silicon photonic circuit. Finally, I discuss the importance of mid-infrared optical sensing for several vital applications, as well as GaSb-based laser sources capable of covering the mid-infrared wavelength range.

In chapter 2, I investigate the degradation of laser performance caused by threading dislocations, an unavoidable crystalline defect arising from the epitaxial growth of III-Vs on Si. I describe the laser structure and fabrication process, followed by the laser characterizations which are analyzed using a theoretical gain model.

Chapter 3 presents the integration of these GaSb-based lasers on a silicon photonic integrated circuit with the aim of coupling light into passive Si-based waveguides. I begin by describing the associated challenges and then address the development of the laser process on a plain GaSb substrate. Then, I move on to the various fabrication steps, starting with the waveguide fabrication and continuing with the epitaxial growth and processing of the GaSb-based lasers. I then describe the properties of the integrated lasers. Finally, I discuss the light-coupling measurements with the help of simulations.

Chapter 4 is dedicated to the investigation of alternative approaches to increase the light coupling efficiency. I first discuss the possibility of increasing the coupling efficiency by filling the gap between the laser and waveguide. I then studied other approaches to significantly reduce the gap size and thus increase the coupling efficiency.

# 1 Chapter 1. State of the art and motivations

## 1.1 Silicon photonic integrated circuits

### 1.1.1 Photonic integrated circuit

A photonic integrated circuit (PIC) is a circuit that uses optical signals to perform various functions, similar to how electronic circuits use electrical signals. The idea of a photonic integrated circuit began to take shape in the early years of optical communications in the mid-20<sup>th</sup> century, when researchers and engineers explored the use of light for communication. They were developing optical components such as lasers, modulators or photodetectors, which were discrete and bulky components. As for microelectronics, the goal of a photonic integrated circuit is to integrate all photonic components on a single chip, which would reduce the size, cost and power consumption of the optical components and interconnections. Photonic integration took a significant step forward with the invention of the diode laser in 1962 by Robert N. Hall.[3], [4] Diode lasers provided a compact and highly efficient source of coherent light, which was fundamental to enable the generation of optical signals in integrated circuits. The term “photonics” began to be widely used to describe the use of light to replace applications previously achieved with electronics. In the 1970s, the invention of planar waveguides, structures that can confine and guide light within a thin substrate, was considered a major breakthrough for photonic integrated circuits. Since then, much work has been done to fully integrate photonic functionalities on a single platform, primarily on Indium Phosphide (InP) substrates. The first integration of a laser with another optical component was demonstrated by Suzuki *et al.* in 1987.[5] Since then, a large range of active and passive photonic components with great performance have been developed in the InP technology, and the fabrication of full photonic integrated circuits with more than 1000 on-chip components was demonstrated.[6]

### 1.1.2 Silicon photonics

While InP technology was being developed, other research focused on the so-called Silicon (Si) photonics. In fact, InP is a very expensive material and the fabrication of chips relies on 75-mm wafers.[7] The goal of silicon photonics is to integrate photonic and electronic components on a common silicon wafer (Figure 1). This would allow to merge the benefits of PICs with the ones of the very advanced and cheap silicon industry and CMOS technology.[8] It would enable photonics to be scaled up to high levels of integration with improved performance and low cost production based on standard 300-mm wafers used in Si microelectronics.[9], [10], [11], [12], [13], [14]

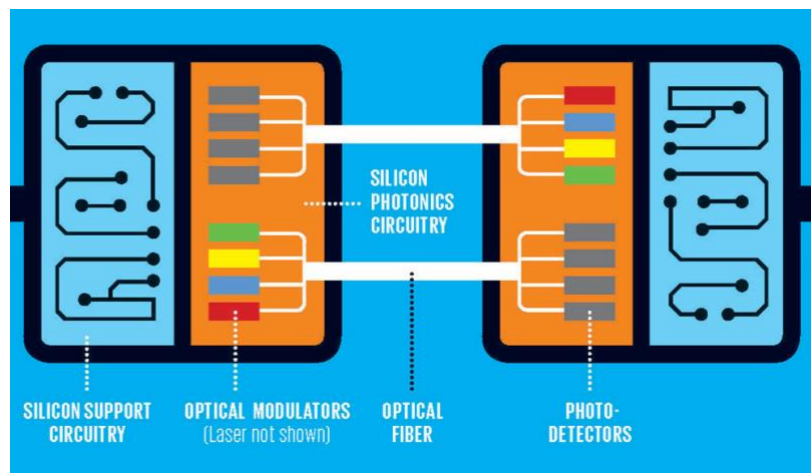


Figure 1. Representation of a Silicon photonic chip.[15]

Additionally, the optical properties of Si and its related materials allows a large range of applications.[16] Silicon has a wide wavelength transparency window, from 1 to 8  $\mu\text{m}$ , approximately (Figure 2). It can also be combined to a high-quality native oxide ( $\text{SiO}_2$ ) that serves not only as an insulator and protection but also as a confinement layer thanks to the low refractive index compared with the one of Si (1.4 vs 3.4).[17] Additionally, SiN-based waveguides have recently emerged as a favorable platform thanks to their wider transparency window in the short-wave infrared, lower optical losses and superior high-power handling capability as compared to Si.[18], [19], [20], [21], [22] In addition, SiN has also a higher refractive index than  $\text{SiO}_2$  (1.4 vs 2). This makes SiN/ $\text{SiO}_2$  waveguides ideal for light propagation. SiN waveguides have been used for example for spectroscopy applications based on surface enhanced Raman spectroscopy.[23] Electro-optic modulators have also been reported using SiN-based platforms.[24], [25] Interestingly, the wavelength transparency window can be increased by introducing Germanium (Ge) which is transparent up to 15  $\mu\text{m}$ , approximately (Figure 2). It has a high refractive index (4), which offers the possibility to effectively guide light as well, notably using SiGe material.[26] Other functionalities, like optical modulation, can also be implemented on this platform.[27], [28]

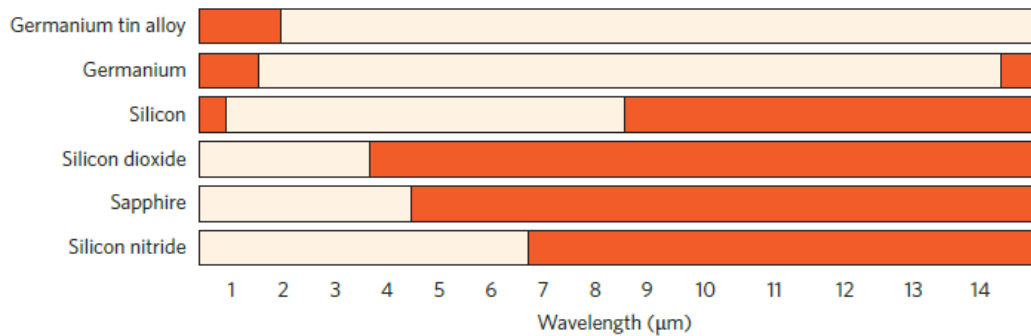


Figure 2. Transmission window of different waveguide materials. The white areas are the wavelength range over which waveguide propagation loss is less than 2 dB/cm. The orange areas are the wavelength range over which loss is high.[8]

Silicon photonics has been considered during the last decade as the most promising platform for the realization of ultra-dense photonic chips. However, one of the biggest challenges in silicon photonics is the realization of high-performance light sources, the component that generates light. It has been the focus of research and has been extensively studied as it is a fundamental step toward the realization of silicon photonic chips. There are several ongoing research efforts that address this problem using different approaches that we will summarize in the next section.[29]

## 1.2 Light sources

### 1.2.1 Group-IV semiconductor lasers

Since the platform of interest is Si-based, the most appealing way to realize the light source would be with Si-based lasers. There has been much research on Si-based lasers for this reason. Ge-based lasers have also been studied because of their compatibility with the Si foundries. However, Si and Ge are semiconductor materials with an indirect bandgap: the lowest energy of the conduction band and the highest energy of the valence band do not share the same wavevector. Due to the energy and momentum conservation laws, the emission of light by the radiative recombination of an electron-hole pair requires that a third particle (a phonon) be involved in the transition, which is highly improbable. This makes indirect bandgap materials not efficient for light emission. Despite this inconvenient, some progress has been made by exploiting sub-bandgap light-emission processes involving one- and two-phonon assisted transitions.[30] In addition, some recent impressive progress has been made using GeSn alloys which allows to obtain a direct bandgap structure.[31], [32], [33] However, the performances are still too low, making III-V semiconductor lasers the best candidates to date for the integration of lasers on Si platforms.[34], [35], [36]

### 1.2.2 III-V semiconductor lasers

III-V semiconductors refers to compounds composed of elements from group III and group V of the periodic table. These materials are known for their excellent electronic and optoelectronic properties. They are the most efficient materials for light emission because most of them, like GaSb, InAs or GaAs, among others, exhibit a direct bandgap. In this case, the lowest

energy level of the conduction band and the highest energy level of the valence band are at the same wavevector (Figure 3). This makes electron-hole pair radiative recombination highly efficient.

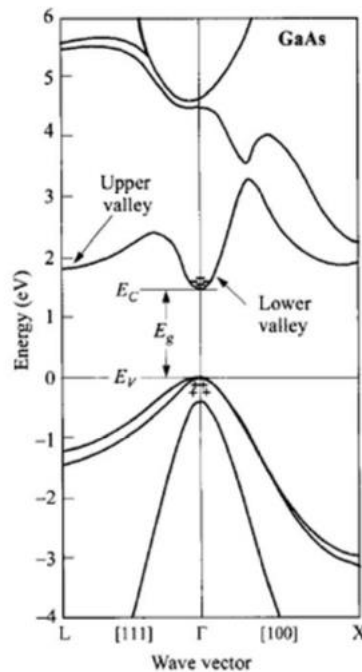


Figure 3. Energy band structure of GaAs, an example of direct bandgap.

III-V lasers also have the flexibility to address a large range of wavelengths, which makes them highly interesting for several applications. For these reasons, they have been extensively studied and they have emerged as the best candidates for the integration of lasers on PICs. Among all the III-V materials, III-Vs crystallizing in the zinc-blende crystal structure are the ones studied for a long time in our group.

In the next section we will describe the different approaches and challenges of integrating these III-V lasers on Si wafers.

## 1.3 Integration approaches

It exists two integration approaches: the heterogeneous and the monolithic integrations. In this section we are going to address these different integration strategies.

### 1.3.1 Heterogeneous integration

The heterogeneous integration consists in the transfer of III-V materials or components grown on their native substrate, onto the Si wafer. In this strategy, there are three main techniques: wafer-to-wafer or die-to-wafer bonding, flip-chip integration and micro-transfer printing. The wafer-to-wafer bonding technique involves growing the III-V materials on their native substrate after which the unprocessed III-V wafer is bonded onto the Si wafer, typically after the Si front-end processes are complete, *e.g.* waveguide fabrication. The III-V native

substrate is then removed followed by the device processing (Figure 4a).[37], [38] The advantage of this technique is that the devices are defined using lithography after bonding which enables a high alignment accuracy with the waveguides.[39] Flip-chip integration involves pre-fabricated III-V devices that are aligned and bonded to the Si photonic circuit after the Si front-end and back-end processes are complete (Figure 4b). This technique is quite slow as it involves single-laser transfer (typically 100 units per hour). Finally, micro-transfer printing starts with a finished Si photonic wafer with local back-end openings, where the devices need to be integrated. Multiple coupons of pre-processed devices are simultaneously transferred in a single operation onto the Si wafer by the use of stamps (Figure 4c), typically a soft elastomeric material such as polydimethylsiloxane (PDMS).[39], [40], [41] In one printing cycle, a large number of devices are transferred, resulting in a high throughput integration, similar to the wafer-to-wafer bonding technique. In addition, as with flip-chip integration, this technique allows pre-testing of the devices on their native substrate as they are fabricated prior to their integration on the target Si photonic wafer.

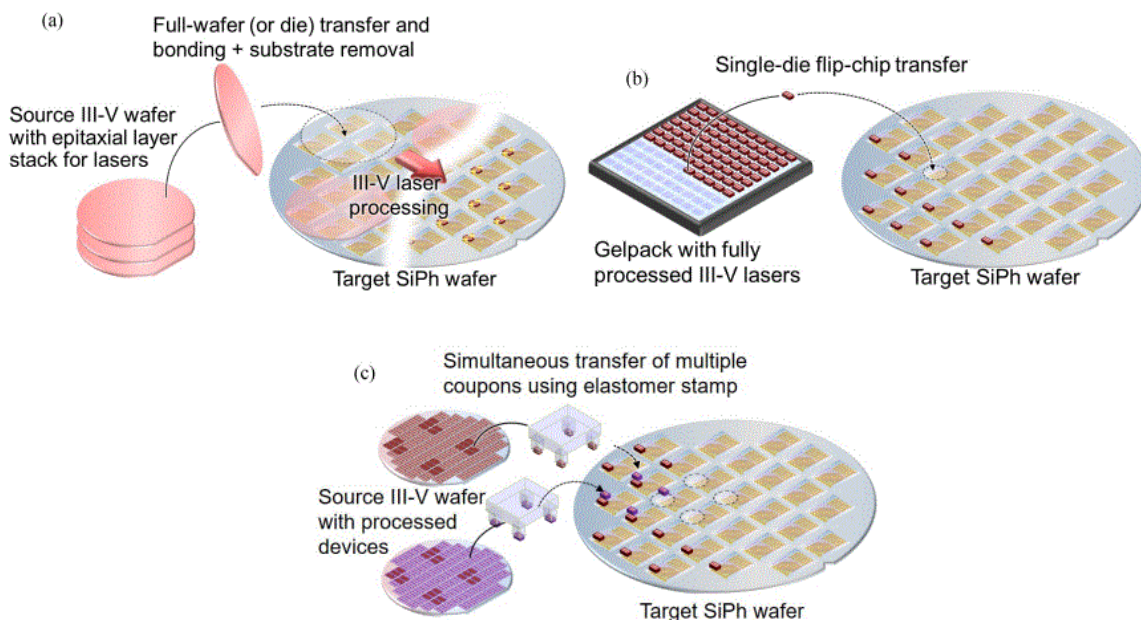


Figure 4. III-V-on-Si heterogeneous integration approaches. a) Wafer-bonding. b) Flip-chip integration. c) Micro-transfer printing.[39]

The heterogeneous integration approach is the most advanced one nowadays.[42], [43], [44], [45] Some commercial products have already entered the market.[46] Despite the maturity of this strategy, it is expected that the monolithic integration will surpass the heterogeneous one in terms of scalability and economic perspectives in the mid- to long-term.[47], [48] In addition, the heterogeneous integration requires etching away the native III-V substrate, a practice that would not be sustainable in the long term.

### 1.3.2 Monolithic integration

The monolithic integration is based on the direct epitaxy of the III-V material on the Si platform. Although, this is a promising strategy several challenges have to be addressed such as the poor crystal quality of the III-V-on-Si epitaxial material and the complex integration process.

The direct epitaxy of III-Vs on Si generally leads to a large density of crystal defects caused by the lattice, thermal and polarity mismatches between III-Vs and Si. These crystal defects will affect the device performance. When two materials with different thermal expansion coefficient, such as III-Vs and Si, are exposed to high temperatures, the lattice retraction will be different for both materials during cooling down. This, in turn, generates stress in the sample, which can result in the formation of macroscopic cracks for a too-high stress. This can be avoided by using slow temperature ramps during cool down. Another problem is that Si is a non-polar material (crystal made of only one type of atoms) arranged in the diamond crystal structure (Figure 5.a)) whereas III-Vs are polar materials (two types of atoms with different ionicity) arranged in the zinc-blende crystal structure (Figure 5.b)). As the zinc-blende crystal structure doesn't have an inversion symmetry, two different bonds between the III-V and the Si structure will exist. As a result, two different domains will grow from the III-V-Si interface: the so-called V-polar and III-polar domains. At the interface of these two domains, III-III and V-V bonds occurs which form so-called antiphase boundary (APB).[49] These APBs create short-circuits in devices and deteriorate their electrical characteristics. This issue is one of the most important challenges for the integration of III-Vs on Si. Much research has been devoted for a long time to study APBs and to find growth strategies that allow their suppression. Ways to avoid them have been established to demonstrate GaAs-based lasers grown on CMOS-compatible (on-axis) Si substrates.[50], [51], [52] The strategy used consisted in growing templates such as GaAs on Si or GaP on Si by metal-organic vapor phase epitaxy (MOVPE), which allows a Si surface preparation that rapidly avoids APBs. The samples are then transferred to a molecular beam epitaxy (MBE) machine to grow the laser heterostructure. InP-based lasers on Si have also been reported using MOVPE growth, but on patterned Si substrates, which are only marginally compatible with the industry.[53], [54] Later, a strategy based on growing an AlGaAs layer on top of the on-axis Si substrate by MBE allowed to demonstrate InAs-based lasers grown on a single MBE run.[55], [56] In our group, great efforts were done to burry APBs within a GaSb buffer layer. III-Sb lasers fully grown by MBE on Si were reported but they were grown on Si substrates having a large offcut ( $6^\circ$ ), not compatible with the industry standards.[57], [58] In the following years, a significant breakthrough was achieved by further optimizing the Si substrate preparation to burry APBs. This achievement allowed to demonstrate a variety of mid-infrared lasers epitaxially grown by MBE on on-axis, CMOS-compatible, Si substrates. [59], [60], [61], [62], [63], [64]

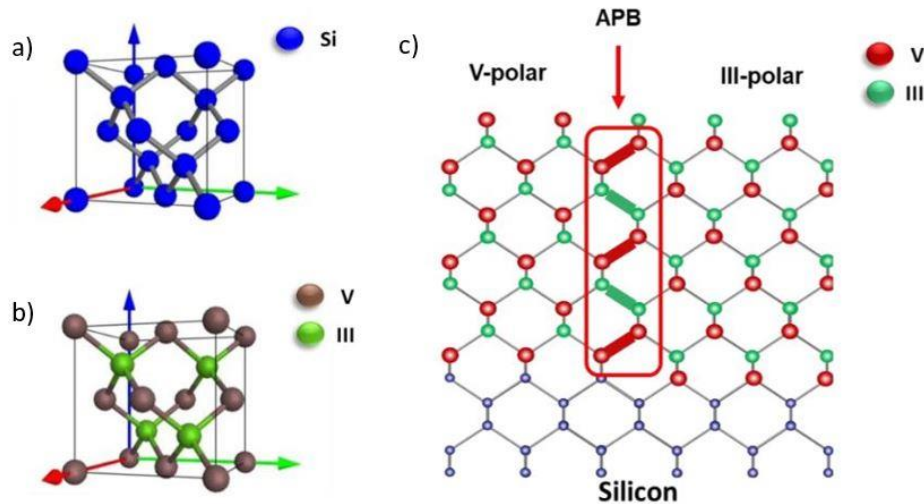


Figure 5. a) Silicon crystal structure. b) III-V crystal structure. c) Sketch of a V-polar domain and a III-polar domain separated by the antiphase boundary (III-III and V-V bonds).[59]

The APBs issue has been resolved in our group. However, another type of defects is created during the III-V-on-Si epitaxial growth: dislocations. Actually, the lattice parameter mismatch between most of the III-V compounds and Si is very high (Figure 6). This leads to stress accumulation during the growth. At a given thickness, the stress is released by generating dislocations.

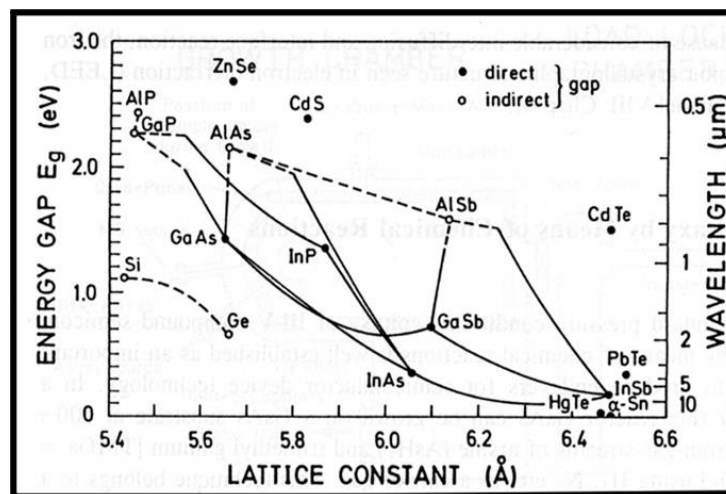


Figure 6. Energy gap and wavelength vs. lattice constant for some elementary and binary semiconductor materials.

The most common type of dislocation are threading dislocations (TDs) and they are inevitable.[65], [66] They propagate through the entire epitaxial structure, as can be seen in Figure 7, reaching the active zone where they will act as non-radiative recombination center and degrade laser performance. Even if they cannot be avoided, their density can be reduced, and this is one of the main challenges regarding the monolithic integration scenario. Much research has been devoted to reducing the threading dislocation density (TDD)[67] and some strategies have proven effective, such as growing filter layers in order to annihilate dislocations. The lowest TDD achieved in our team for a GaSb-on-Si growth is in the low- $10^7 \text{ cm}^{-2}$ , compared



to the  $10^9 \text{ cm}^{-2}$  when no growth strategy is applied and to  $10^3 \text{ cm}^{-2}$  for growths on native GaSb substrate.

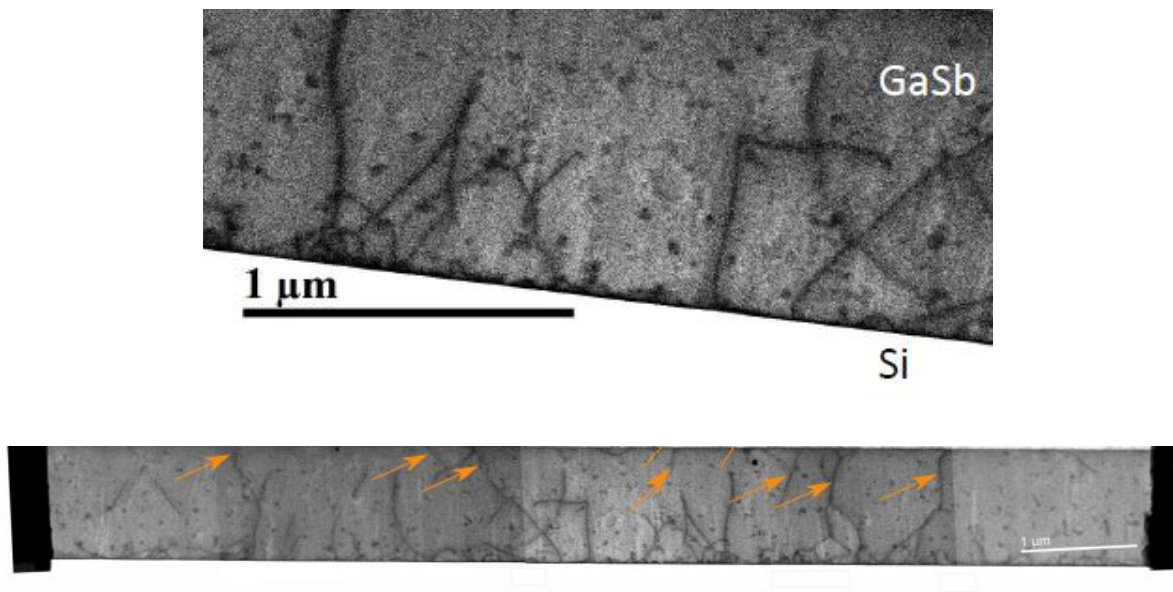


Figure 7. TEM pictures of GaSb layer grown on Si substrate where threading dislocations are visible (Courtesy of Karl Graser, PDI Berlin).

The monolithic integration approach is the most promising one in terms of scalability and cost reduction. High-performance lasers have been reported despite the high defect density arising from the III-V-on-Si growth. However, these lasers have only been demonstrated as discrete devices. The next step toward fully integrated Si photonic chips would be to integrate them on a Si PIC and demonstrate the light coupling from the integrated lasers to passive Si-based waveguides. To address this challenge, different coupling configurations have been studied, either for the heterogeneous or monolithic approach, and I will compare them in the next section.

## 1.4 Coupling configurations

The high defect density arising from the III-V laser growth on Si is not the only challenge of the monolithic integration scenario. The next challenge is the complex fabrication process of lasers on the Si PICs. While the laser cavity mirrors are not difficult to obtain by simple cleavage for discrete III-V-on-Si lasers, for lasers integrated on Si PICs this approach is no more an option since the lasers and the Si PIC are on the same chip. The optical cavity should therefore be processed by other means. The fabrication strategy should also enable the coupling of these active components with the rest of the circuit, *i.e.* the light output from the laser sources should be coupled into passive waveguides which will guide the light to the other optical functions. There are two main coupling configurations that are being studied: evanescent coupling and butt-coupling.

The evanescent coupling is the configuration traditionally used in the heterogeneous integration. It is achieved by bringing the laser and the waveguide into close proximity such

that the electromagnetic field of the laser penetrates into the waveguide via the evanescent field (Figure 8.a)).[68] A taper is used to progressively reduce the effective refractive index down to the one of the waveguide in order to enable the light coupling. This configuration requires very precise alignment to achieve high coupling efficiency. But, when properly implemented, it can provide very high coupling efficiency, with values reaching up to 90%.[69]

On the other hand, the butt-coupling configuration involves aligning the laser and waveguide face-to-face (Figure 8.b)). The optical field is transmitted by optical mode overlap. This configuration is generally easier to fabricate and align compared to evanescent coupling but the coupling efficiency is lower. The primary reason for this is the high sensitivity of the coupling efficiency to the gap between the laser and the waveguide[70] and also the mismatch between the laser mode and the waveguide mode. A coupling efficiency for this configuration of around 60% have been reported in the heterogeneous approach by Romero-Garcia *et al.*[71]

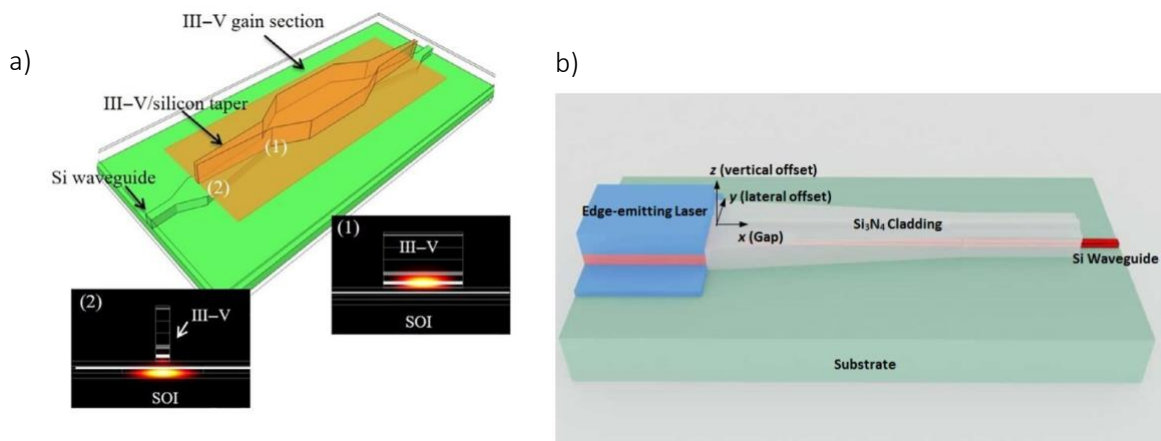


Figure 8. The two main light coupling configurations. a) Evanescent coupling of a III-V laser into a Si waveguide thanks to a taper section.[69] b) Butt-coupling configuration of a laser into a Si waveguide.[72]

Overall, for applications that demand high coupling efficiency, the evanescent coupling may be the preferred choice even if the fabrication process is less straightforward. Regarding the monolithic integration, the growth of III-V lasers on Si inevitably results in crystal defects detrimental to device performance. Strategies to reduce their density requires growing thick buffer layers (1-5  $\mu\text{m}$ ) underneath the laser structure. These layers prevent implementing evanescent light coupling from the laser into the waveguide because of the large vertical distance between the laser active zone and the waveguide core, resulting in a drastic increase of the coupling losses. The alternative solution is therefore to implement the butt-coupling configuration. This is the coupling configuration that I developed in my work.

At the beginning of my Ph.D., no III-V lasers had been demonstrated that were monolithically integrated on Si and optically coupled to passive Si-based waveguides. This is the main objective of my thesis as this is considered a key challenge to unlock the realization of Si photonic chips.

## 1.5 Applications of Si PICs

The soaring demand for silicon photonics chips was initiated in the datacom/telecom applications. Actually, in the microelectronics industry, the miniaturization and integration density of transistors, guided by the Moore's Law, is arriving to its limits.[2] It is, therefore, necessary to find an alternative solution to increase communication bandwidths and reduce power consumption, and Si photonics would enable the rapid transmission of data at high bandwidths, providing a cost-effective solution.[73] Silicon photonics has been extended to many other applications besides datacom/telecom, such as optical sensing, optical interconnects, LiDAR (Light Detection and Ranging) systems or quantum technologies, to name but a few.[74], [75], [76], [77], [78] Among these applications, the development of technologies based on optical sensing has been considered a vital need for several applications that we will discuss in the next section.

### 1.5.1 Optical sensing in the mid-infrared

The short-wave portion of the mid-infrared (SWIR) electromagnetic spectrum, ranging from 2 to 5  $\mu\text{m}$ , contains transparency windows of the atmosphere as well as absorption lines of many biological and chemical species (Figure 9a).[79] Developing sensors which work in this wavelength range has been, therefore, considered a vital need for societal, environmental or medical applications, among others (Figure 9b). Their demand has increased significantly in the last decade. In the 2-5- $\mu\text{m}$  spectrum (Figure 9a), gases of interest, such as CO, CO<sub>2</sub>, HF or CH<sub>4</sub>, absorb light. Accurate measurement of the concentration of these molecules is crucial. For instance, detecting CH<sub>4</sub>, a gas with low explosion limit in the air and known for contributing to global warming,[80] is vital for leak detection[81] and gas emission monitoring. Also, the detection of toxic gases like CO or CO<sub>2</sub>[82] is essential for industrial process and air quality controls, for disease diagnosis in the health care sector, to name a few. In addition, some portions of the spectrum are of interest as there are H<sub>2</sub>O windows, which avoids interference of atmospheric water. In this thesis, I mainly worked on lasers emitting near 2.3  $\mu\text{m}$ , a wavelength of interest for trace gas sensing because of the presence of absorption lines of CH<sub>4</sub>, NH<sub>3</sub> and CO, and a H<sub>2</sub>O transparency window (Figure 9a).[83] In addition, this wavelength has recently being used for LIDAR applications.[84]

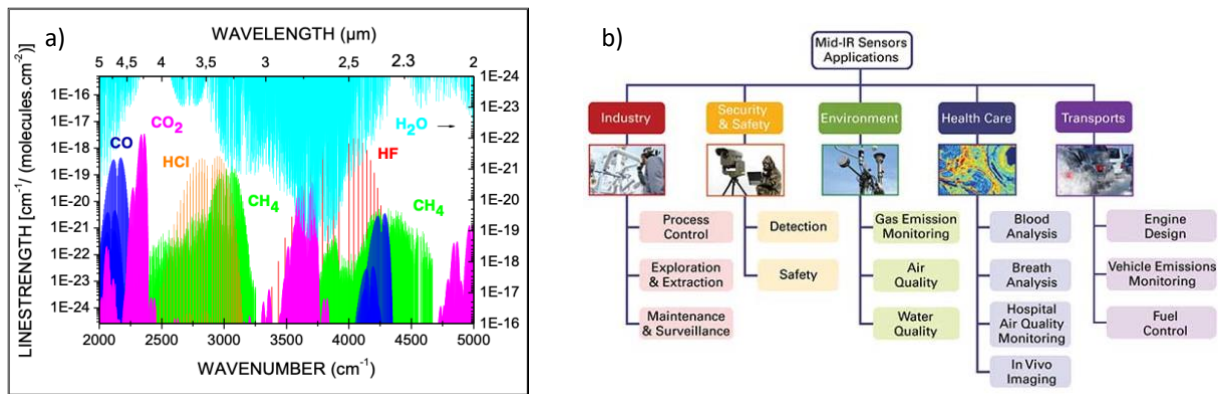


Figure 9. a) 2-5- $\mu\text{m}$  mid-IR spectrum.[79] b) Mid-IR sensors applications.[85]

The specific characteristics and requirements of these sensors depend on the application. In general terms, they need to be sensitive and selective to detect very low molecule concentrations and target the desired molecule or gas. Much research is focused on sensors based on laser spectroscopy. The TDLAS technique, that stands for Tunable Diode Laser Absorption Spectroscopy, is widely used for gas sensing. The light emitted by the laser source passes through a sample of the gas of interest. If the wavelength of the laser matches the absorption line of the molecule, part of the light is absorbed. The transmitted laser light, after passing through the gas sample, can be measured with photodetectors. The photodetector measures the intensity of the transmitted light at the absorption wavelength and the concentration of the gas can be deduced using Beer-Lambert relation. Other techniques can also be used for gas detection such as QEPAS (quartz-enhanced photoacoustic spectroscopy) or CEPAS (cantilever-enhanced photoacoustic spectroscopy) which are based on the detection of acoustic waves generated by the de-excitation of the target gas molecules.

These mid-IR sensors require laser sources emitting at the wavelengths of interest. In the next section, we will discuss about mid-IR lasers.

## 1.5.2 Mid-IR lasers

### 1.5.2.1 The antimonide technology

As discussed previously, III-V lasers are the best candidates for Si PICs thanks to their high efficiency. They also have the flexibility to address a wide range of wavelengths in the mid-IR through the choice of adapted materials and the engineering of the band structure (Figure 6). For example, to address wavelengths in the 2-5- $\mu\text{m}$  spectral range, antimonides are adapted and these are the ones that have been studied for a long time in our group. Antimonides refers to compounds that have a lattice constant close to 0.61 nm, such as GaSb, InAs and AlSb compounds and their ternary, quaternary and pentanary alloys.[86] They can cover the 2-5- $\mu\text{m}$  wavelength range while being closely lattice-matched to GaSb or InAs (Figure 6). Another feature of these compounds is the variety of band alignments.[87] Figure 10 shows the band alignments of III-V binaries in the antimonide material system. We can see different bandgap energies as well as different band alignments (type-I, II and III). The GaSb/AlSb system is type I.

The valence-band maximum of AlSb is lower than the conduction-band minimum of InAs, giving a type-II band alignment for the AlSb/InAs heterostructure. Finally, the conduction-band minimum of InAs being lower than the valence-band maximum of GaSb, the InAs/GaSb system is type-III. By choosing the right material system and properly designing the composition and layer structure, band engineering allows covering the entire mid-IR spectrum.

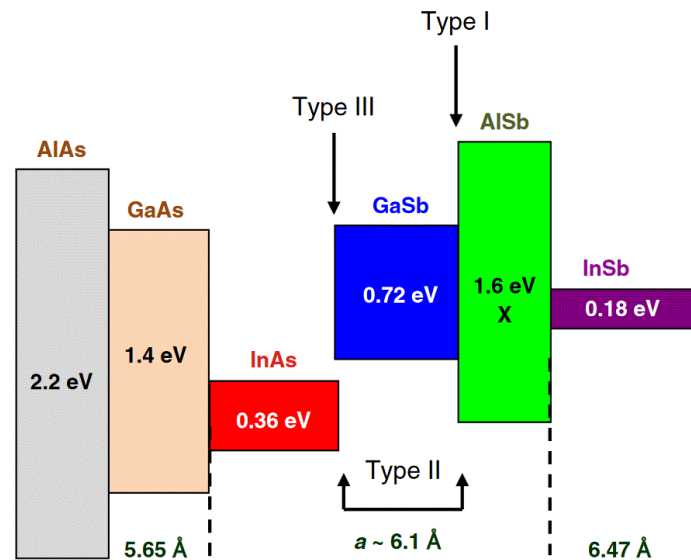


Figure 10. Band structure alignments for a selection of unstrained III-V binaries at 300 K.[88]

### 1.5.2.2 Mid-IR lasers and state of the art on Si substrates

There exist different types of lasers such as diode lasers (DLs), interband cascade lasers (ICLs), quantum cascade lasers (QCLs), among others. They are differentiated by their band structure engineering and carrier confinement schemes leading to distinct emission wavelengths and characteristics.

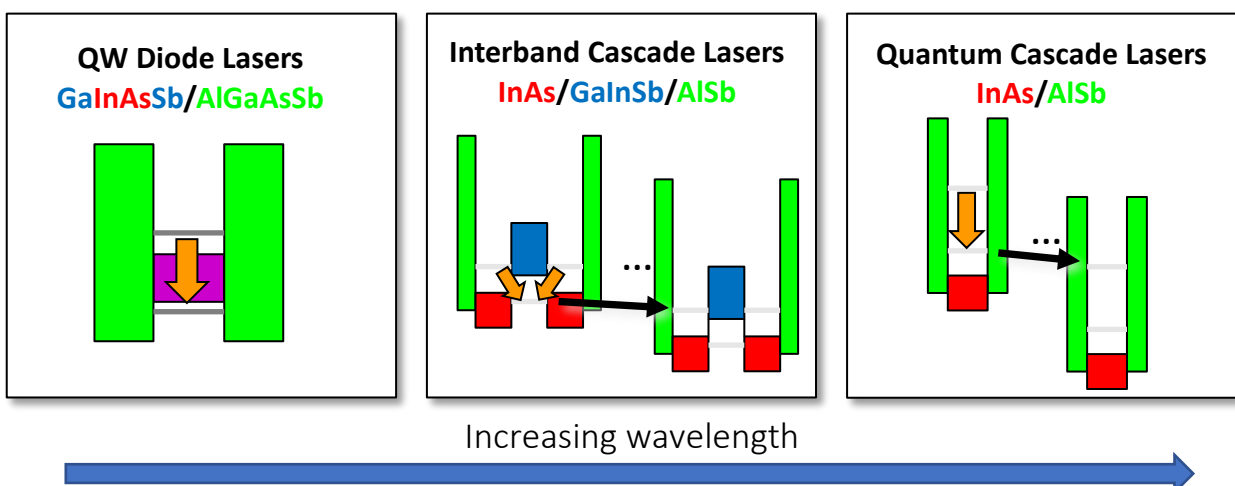


Figure 11. Band alignments and recombination mechanisms of QW diode lasers, interband cascade lasers and quantum cascade lasers.

ICLs involve interband transitions in a type-II QW where carriers are collected and transferred to the next neighbor type-II QW, leading to a cascade effect. Their design allows

addressing wavelengths from 3 to 7  $\mu\text{m}$ . The first ICL was reported in 1997 with an emission wavelength at 3.8  $\mu\text{m}$ . [89] The ICLs studied in our team are based on GaInSb/InAs type-II QWs. Their epitaxial growth on on-axis Si substrates has been demonstrated emitting at 3.4  $\mu\text{m}$  in the continuous-wave regime and with high performance (Figure 12.a). [64] A quantum cascade laser is based on intersubband transitions within the conduction band in a repeated stack of quantum well structures also creating a cascade effect. QCLs were first demonstrated in 1994 and emitted at 4.2  $\mu\text{m}$  in pulsed operation. [90] However, they allow going to longer wavelengths and they are now capable of covering a wide range of wavelengths in the mid-IR, going up to 25  $\mu\text{m}$  thanks to the low-energy intersubband transitions (Figure 13). [91] QCLs epitaxially grown on on-axis Si substrates and emitting at 8  $\mu\text{m}$  have also been reported in our group (Figure 12.b). They are based on InAs/AlSb structures (Figure 11). [63]

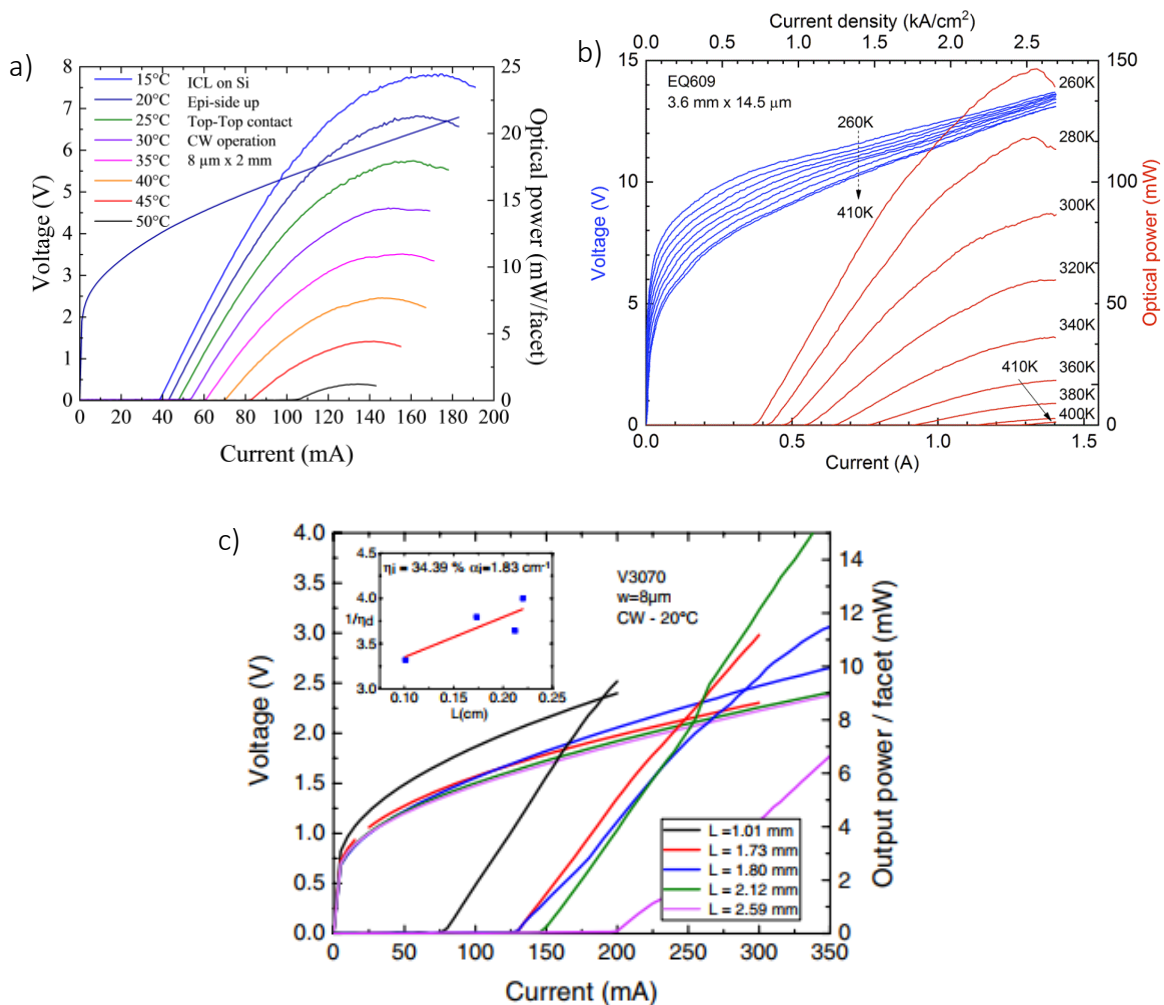


Figure 12. L-I-V curves of different types of lasers grown on on-axis Si substrates. a) ICL. b) QCL. c) DL. [62], [63], [64]

On the other hand, DLs are based on interband transitions in a type-I quantum well structure (Figure 11) and are able to address part of the SWIR wavelength range. The first Sb-based electrically pumped type-I QW diode laser was demonstrated in 1984 using AlGaSb/GaSb QWs emitting at 1.65  $\mu\text{m}$  in pulsed operation. [92] In our group, DLs are fabricated with GaInAsSb/AlGaAsSb (QW/barrier) quaternaries and emission wavelengths between 1.55 and



3.3  $\mu\text{m}$  have been demonstrated.[93] Diode lasers emitting at 2.3  $\mu\text{m}$  have been studied for a long time and they have been used for all the different investigations carried out during my thesis, because they can easily be benchmarked. Although DLs emitting at 2.3  $\mu\text{m}$  can be achieved with InP-based lasers, GaSb-based DLs exhibit lower threshold current densities in this spectral range.[69], [94] The state of the art GaSb DLs grown on an on-axis Si substrate before the start of my PhD exhibited a threshold current in continuous-wave operation of around 75 mA for a cavity length of 1 mm and a laser ridge of 8  $\mu\text{m}$  (Figure 12.c), high temperature operation and a few tens of mW output power.[62]

Each type of laser has unique characteristics that make them suitable for specific applications in different regions of the mid-IR electromagnetic spectrum. The threshold current density as a function of the operating wavelength for the different types of laser is summarized in Figure 13.

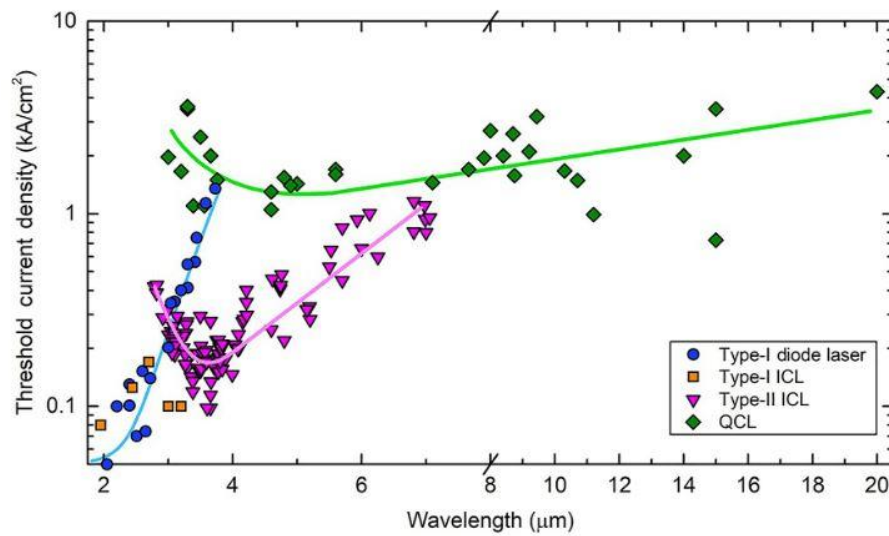


Figure 13. Threshold current densities vs. wavelength of different types of mid-IR lasers.[81]

As discussed in section 1.3.2, threading dislocations arise from the highly-mismatched III-V-on-Si growth and are unavoidable. They create energy levels within the bandgap with which carriers can interact through non-radiative recombination mechanisms (see section 5.1). ICLs are based on transitions between the conduction and valence bands of the neighboring layer, which makes the recombination of the carrier with the defect level in the bandgap unlikely.[64] QCLs are based on intersubband transitions in the conduction band, so carriers do not interact with the defect level in the bandgap. However, while ICLs and QCLs are highly tolerant to threading dislocations,[63], [64], [95] the performance of DLs is dramatically degraded by these defects as the transitions are from the conduction band to the valence band of the QW layer. Great efforts have been made in our team to reduce the TDD. Although significant progress has been made and an improvement in DL performance has been observed, it is not yet comparable to the performance of DLs grown on native GaSb substrate. I have thus

proposed to study the effect of threading dislocations on the GaSb-based DL performance to address this challenge.

## 1.6 Conclusion

Silicon photonics has emerged as the most promising technology for reducing the cost and increasing the scalability of photonic integrated circuits. The main remaining challenge is the realization of efficient light sources on Si. III-V semiconductor lasers have proven high efficiency and are considered the best candidates for this challenge. The heterogeneous integration of III-V lasers on Si is the most mature approach and devices have already been commercialized. In contrast, the monolithic integration is still in its infancy. However, there is evidence that the monolithic integration will increase the integration density and reduce cost and waste. It is therefore the most promising approach for realizing ultra-dense photonic chips, despite the poor crystal quality of the III-V-on-Si epitaxial growth. Impressive progress has been made in avoiding APBs. Threading dislocations are inevitable, although their density can be decreased to limit laser degradation. Still, all epitaxial III-V lasers on Si reported so far are discrete devices grown on plain Si substrates. The next step is to integrate these lasers on a Si PIC with light coupled into waveguides.

The realization of Si PICs is highly demanded for several applications. Among these applications, optical sensing in the mid-IR have been identified as a vital need for many societal or medical applications, among others. Antimonides have some excellent features that allow them to cover the entire mid-IR wavelength range while being lattice-matched to GaSb. They are therefore the best candidates so far for the integration of laser sources on a Si PIC for sensing applications.

The objective of my thesis is to take a step forward towards the monolithic integration of mid-IR lasers on Si photonic chips. In chapter 2, I will investigate the impact of threading dislocations on the performance of GaSb-based diode lasers. In this chapter, a meticulous study will be carried out to understand the origin of the degradation of the laser structures. In chapter 3, I will address the integration of lasers on a Si PIC with light coupled into passive Si-based waveguides. In this monolithic scenario, several challenges will be faced such as the limitation of using a butt-coupling configuration, which makes an air gap inevitable, the epitaxial growth of the lasers on a Si PIC and the complex laser processing to achieve light coupling. Finally, in chapter 4, I will propose alternative solutions in order to increase the coupling efficiency. The main test vehicle during my thesis was GaSb-based DLs emitting near 2.3  $\mu\text{m}$  because they have been studied for a long time in our team and they can be easily compared with DLs grown on their native GaSb substrate.





## 2 Chapter 2. Discrete GaSb-based diode lasers grown on GaSb and Si substrates

In the previous chapter, we have discussed the importance of GaSb-based materials to address the mid-IR part of the spectrum for sensing applications. In addition, we have also discussed the different integration approaches and we concluded that the monolithic integration of these lasers on Si is the most promising technique in terms of cost, footprint reduction and large-scale production. However, one of the biggest challenges is the poor crystal quality arising from the epitaxial growth. As opposed to APBs,[60]·[61]·[96] threading dislocations are unavoidable due to the highly mismatched growth. They dramatically affect the laser performance by inducing non-radiative recombinations, which increases the laser threshold at the expense of the device's lifetime. For now, some aspects of the mechanisms responsible for this deterioration remain unclear in the literature where it is often stated that dislocations introduce additional optical losses as well.[58], [97], [98], [99] In order to study the effect of threading dislocations, we will compare in this chapter two series of GaSb diode lasers emitting near 2.3  $\mu\text{m}$ . One series is grown on native GaSb substrates, whereas the other one is grown on Si substrates. First, I will present the growth and fabrication process of the two series of GaSb diode lasers. The experimental results will be analyzed and confronted to a theoretical gain model which will allow extracting the impact of dislocations on the laser performance.

### 2.1 Diode laser heterostructure

During my Ph.D., I mainly worked on diode lasers designed to emit near 2.3  $\mu\text{m}$  (transition energy near 0.542 eV).[87] In this section, I present the design of the laser heterostructure for diode lasers grown on GaSb and on Si substrates.

We used two series of four samples containing different numbers of QWs ( $1 \leq n_{\text{QW}} \leq 4$ ) grown by solid-source molecular beam epitaxy (MBE) on (001)-oriented GaSb and Si substrates. The active zones are based on 9-nm-thick  $\text{Ga}_{0.67}\text{In}_{0.33}\text{As}_{0.08}\text{Sb}_{0.88}$  QWs confined by  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}_{0.02}\text{Sb}_{0.98}$  barrier layers and are embedded within 800-nm  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}_{0.02}\text{Sb}_{0.98}$  waveguides.[81] The band structure details of the QWs are shown in Figure 15. Two n- and p-type  $\text{Al}_{0.9}\text{Ga}_{0.1}\text{As}_{0.08}\text{Sb}_{0.92}$  cladding layers ensure carrier and photon confinement in the active region. Indeed, the higher the Al content, the higher the bandgap, which allows confining the carriers in the active region. Also, the higher the Al content, the lower the refractive index which allows confining the optical mode in the active zone. A highly doped, p-type GaSb contact layer was grown atop all structures. In the case of DLs grown on Si substrates, a 1- $\mu\text{m}$  thick GaSb buffer layer was first grown to suppress APBs.[59] A highly conductive  $\text{InAs}_{0.92}\text{Sb}_{0.08}$  contact layer was then grown to enable a top-top contact configuration, which avoids driving the current through the highly defective Si/GaSb interface.[58] Finally, an additional 0.5- $\mu\text{m}$ -thick GaSb buffer layer was inserted between the InAsSb contact layer and the laser structure to avoid the optical mode to overlap with the low bandgap InAsSb layer which could absorb part of the light.

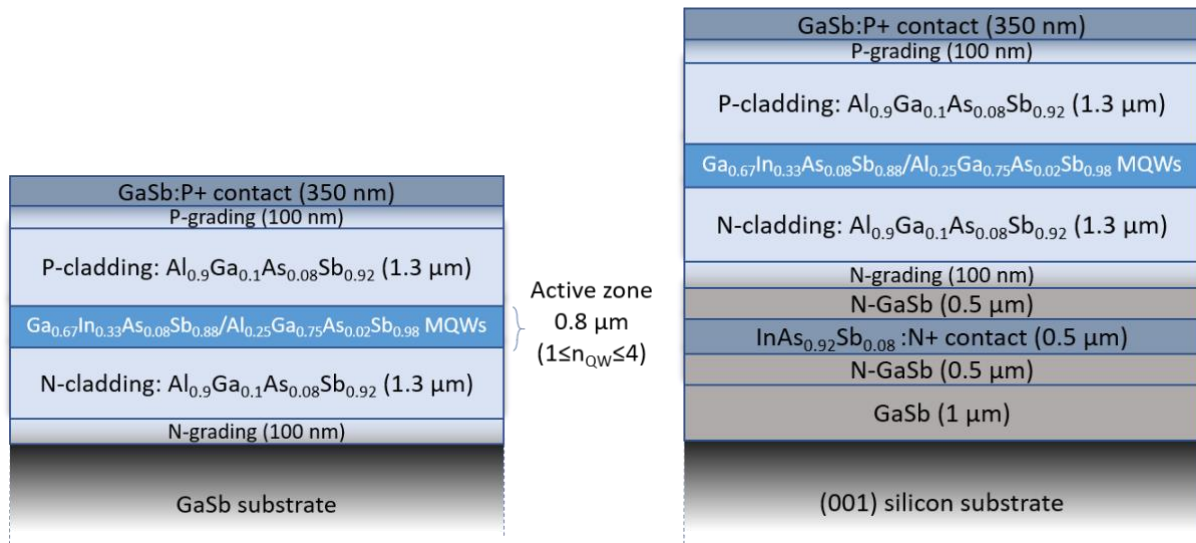


Figure 14. Structure design of the diode lasers grown on a) GaSb substrates and on b) Si substrates containing different number of QWs in the active zones for each substrate (1-4 QWs).

The QWs have a lattice mismatch of  $\sim 1.5\%$  with respect to GaSb, whereas the  $\text{Al}_x\text{Ga}_{1-x}\text{As}_y\text{Sb}_{1-y}$  layers are lattice matched to GaSb. The laser structures with different number of QWs and different substrates are shown in Figure 14 and the band structure details of the whole structure in the case of the 2-QWs laser grown on Si is shown in Figure 15.

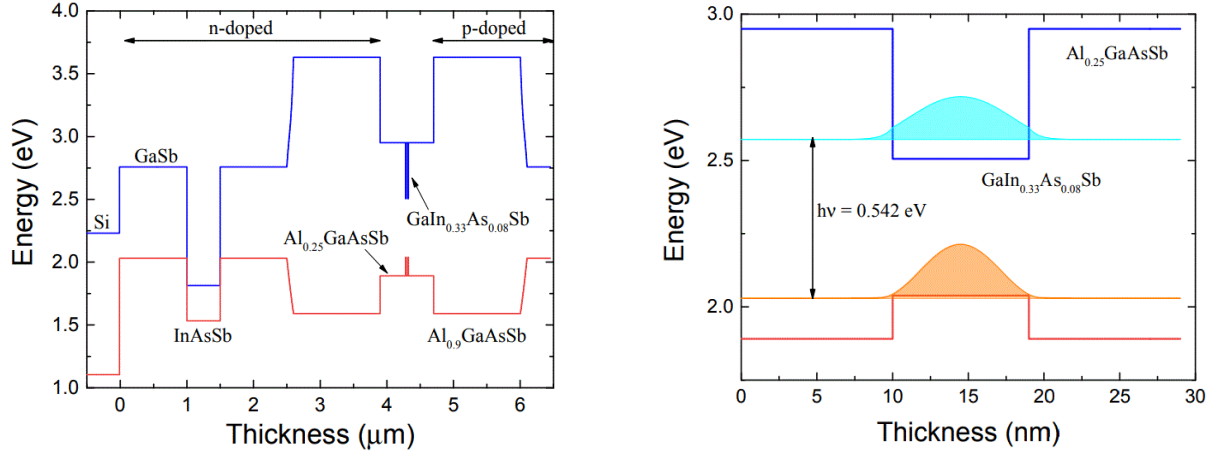


Figure 15. Band structure details of the design for a DL grown on Si. a) A band structure detail for the entire structure. b) A band structure detail for the QWs[62].

## 2.2 MBE growth

The laser heterostructures were grown by molecular beam epitaxy (MBE) which is a widely used technique to grow high-quality crystalline layers of semiconductor materials with precise control of the thickness at the atomic level. The growth process involves an ultra-high vacuum chamber to minimize impurities and contamination. High-purity elemental or molecular sources, called effusion cells, are heated to evaporate the atoms/molecules which will be deposited onto the heated substrate. The temperature of each cell can be precisely controlled to achieve the desired evaporation rate, thus the desired growth rate. An uncertainty of 3% on the growth rate can be achieved which results on an uncertainty on the growth thickness of less than 100 nm.

In the case of DLs on Si, the substrates were first annealed at 1000°C for 10 mins, followed by the growth of 50 nm of GaSb at ~400°C and the rest of the 1-μm buffer layer was grown at 500°C. These growth conditions allow the annihilation of the APBs.[62] The temperature was then set to 470°C to grow the InAsSb contact layer, the additional 1-μm thick GaSb layer (in the case of DLs on Si) and the laser heterostructure.

After growing these two series of four lasers, a structural characterization of the wafers was done. Figure 16.a) shows a 20x20 μm<sup>2</sup> atomic force microscopy (AFM) image of the surface of the 2-QWs laser heterostructure on Si and Figure 16.b) the omega-2theta high-resolution X-ray diffraction scan of the same laser. The AFM image confirms the absence of APBs emerging at the surface of the samples grown on Si. The AFM image shows also a spiral-like growth emerging on the surface of the sample which is caused by the presence of TDs. By counting the number of spirals, an upper bound of  $9 \times 10^7 \text{ cm}^{-2}$  is estimated for the TDD. The same result was obtained for all lasers grown on Si, regardless of the number of QWs. The X-ray diffraction scan exhibit sharp interference fringes which confirms that the active zone is well-defined. Also, the single peak of GaSb confirms the lattice matching of the  $\text{Al}_x\text{Ga}_{1-x}\text{As}_y\text{Sb}_{1-y}$  layers with GaSb. Similar X-ray diffraction characteristics were seen for the other lasers grown on Si. The X-ray

diffraction scan for lasers on GaSb exhibited narrower peaks than for lasers on Si due to the lower defect density.

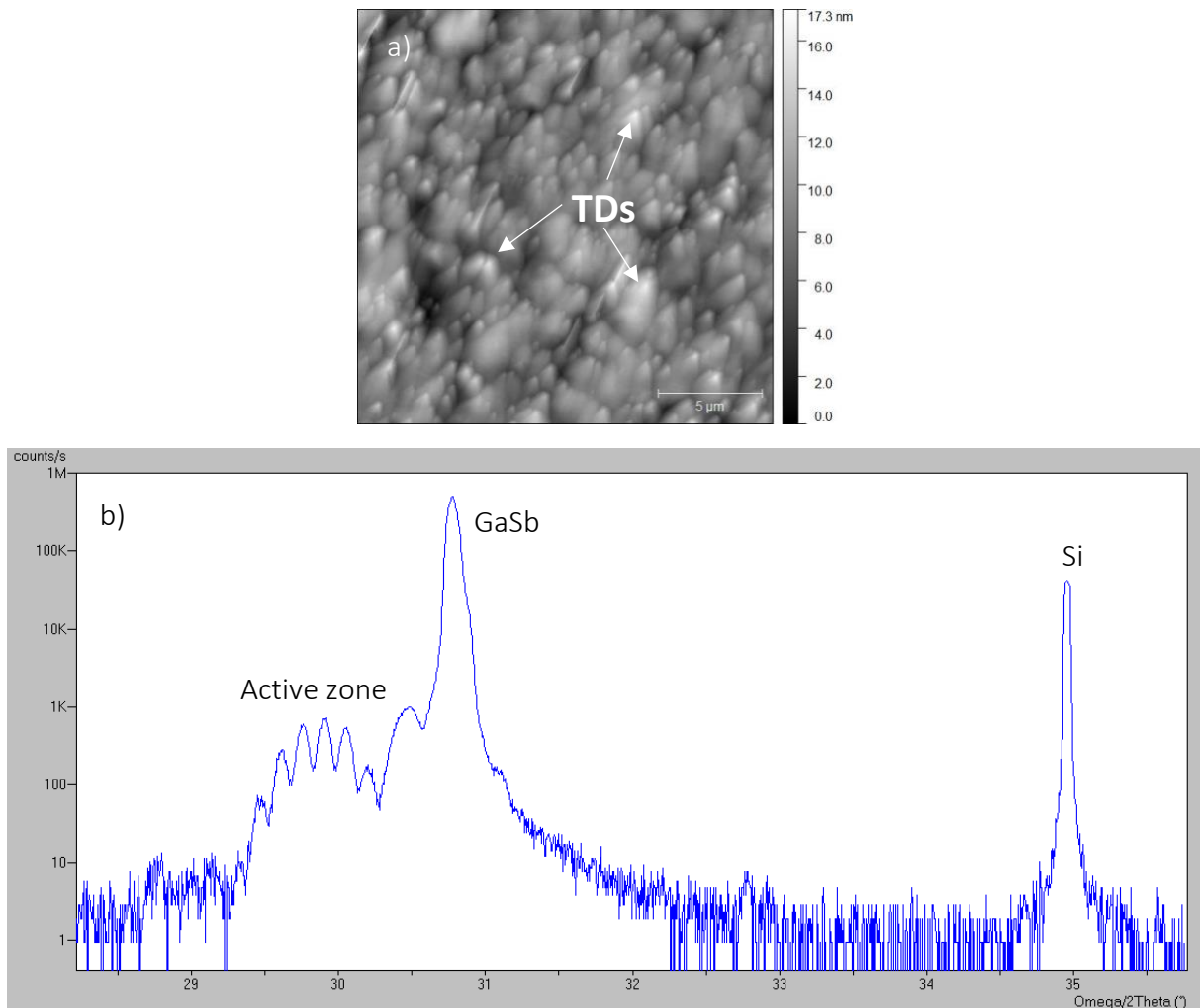


Figure 16. a) 20x20 μm<sup>2</sup> AFM image of the 2-QWs laser surface. b) Omega-2theta high-resolution X-ray diffraction scan of the same laser.

## 2.3 Laser fabrication process

In this section, I will describe the process flow to fabricate the lasers grown on Si substrates. Lasers grown on GaSb substrates have a similar process flow that I will comment later. In order to fabricate these lasers, four photomasks are needed for four different main steps: laser ridge definition, bottom contact etching, electric insulation and metallization. The Fabry-Perot cavity is formed at the end of the process by cleaving. Figure 17 shows 3D sketches of the final device in the case of DLs on GaSb (Figure 17.a) and on Si (Figure 17.b).

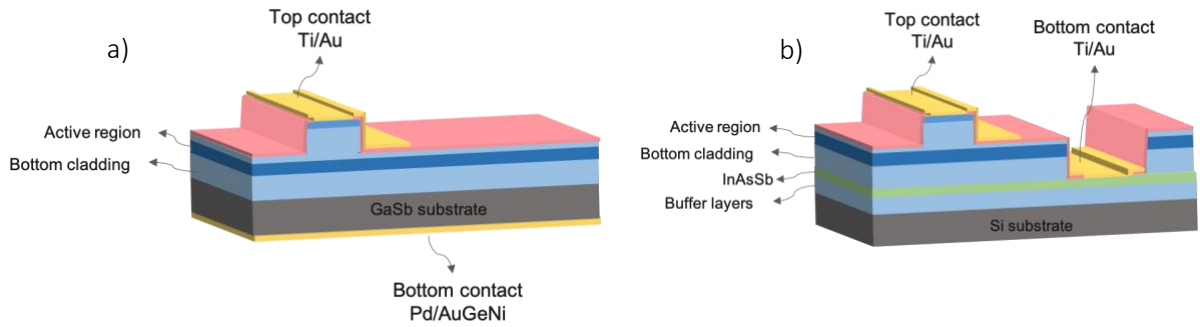


Figure 17. Sketch of the final device after processing. a) DL on native GaSb substrate. b) DL on Si substrate.

### 2.3.1 Laser ridge

The first step of the laser process is the laser ridge definition, which defines the area where the current is injected into the active zone. It also allows confining the optical mode within the ridge. Different ridges are present on the mask: wide ridges of 100  $\mu\text{m}$  and narrow ridges of 5, 8 and 10  $\mu\text{m}$ .

In order to fabricate the laser ridges, a UV photolithography (see section 5.2.1) is first performed using the positive resist AZ1518 and the standard lithography parameters displayed in Table 1. The alignment of the sample with the mask should be performed such that the (110) plane of the sample is perpendicular to the ridges in order to later facilitate the cleavage of the Fabry-Perot cavity. A precise alignment is needed to maximize the reflectivity of the future mirrors.

Spin-coating				Soft bake		Exposure		Development
Resist	v (rpm)	Ramp (s)	t (s)	T ( $^{\circ}\text{C}$ )	t (min)	Contact mode	t (s)	t (s)
AZ1518	4000	2	30	110	1	Soft contact	30	30

Table 1. Parameters of the photolithography of the laser ridge definition.

The ridges are then etched by ICP dry etching (see section 5.2.2). As shown in Figure 19, the resist will act as an etching mask and the unmasked regions will be etched away to define the ridges. The dry etching is performed using the Cl-based recipe presented in Table 2. This recipe was previously optimized in the laboratory for GaSb-based compounds.

$\text{BCl}_3$	$\text{Cl}_2$	Ar	Temperature	Pressure	RF power	ICP power
4 sccm	2 sccm	6.5 sccm	10 $^{\circ}\text{C}$	1.5 mTorr	60 W	300 W

Table 2. ICP recipe previously optimized to etch GaSb-based compounds.

A tracking tool is available to follow the etching. It is a laser source pointing the unexposed surface of the sample. While etching the material, a variation of the reflectivity is detected as well as a variation of the refractive index when another layer of the structure is reached. A typical tracking signal recorded during etching of the full heterostructure is shown in Figure 18. Each layer of the laser structure can be identified which makes it possible to accurately stop the etch at the desired depth. The etch rate of this recipe is very similar for each layer and is around  $\sim 350$  nm/min. For defining the laser ridge, the etching is stopped just before reaching

the active zone at a depth of  $\sim 1700$  nm, to minimize the current spreading as well as the optical losses on the sidewalls.[100], [101]

Finally, the resist is removed with acetone, alcohol and  $O_2$  plasma.

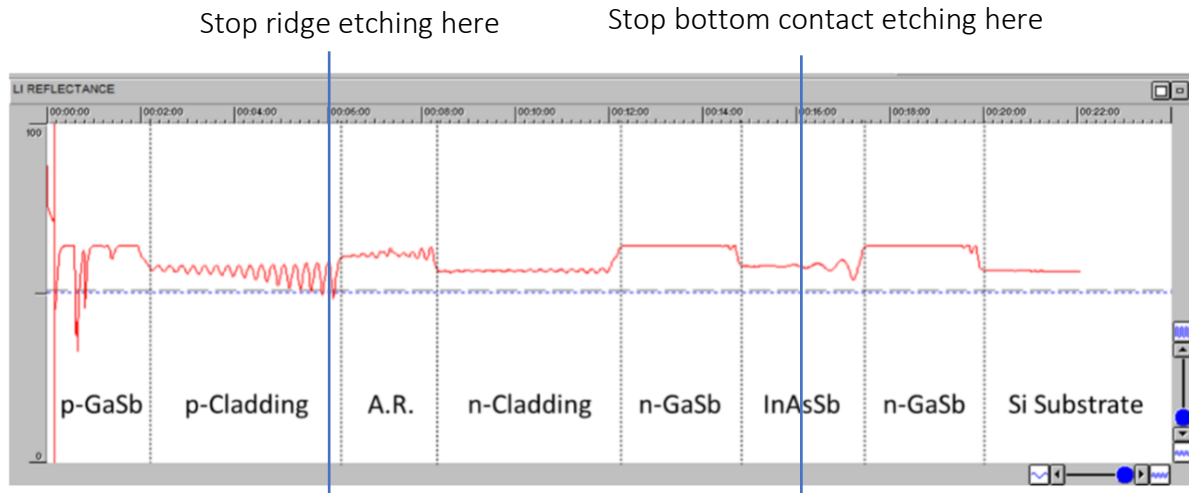


Figure 18. Tracking signal of the etching for the whole heterostructure: reflectance vs. etching time.

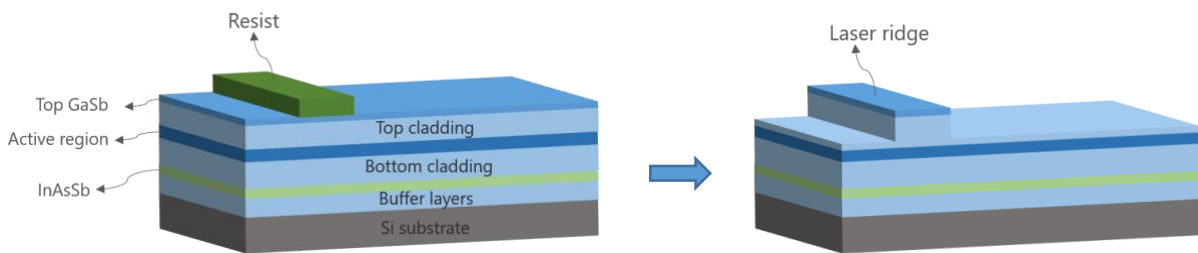


Figure 19. Sketch of the fabrication step of the laser ridge.

### 2.3.2 Bottom contact etching

The second main step is the bottom contact. A second etching is performed in order to reach the InAsSb layer which serves as the n-contact layer and avoids the current flowing through the highly defective Si/GaSb interface.

As this step involves a deep etching ( $\sim 3 \mu\text{m}$ ), a thick resist is required to ensure protection of the masked regions throughout the etch, especially the laser ridges. For this purpose, two identical spin-coatings are performed, with the parameters shown in Table 3. A longer exposure duration was used (1 minute) to ensure the full exposure of the thicker resist.

Spin-coating				Soft bake		Exposure		Development
Resist	$v$ (rpm)	Ramp (s)	$t$ (s)	$T$ ( $^{\circ}\text{C}$ )	$t$ (min)	Contact mode	$t$ (s)	$t$ (s)
AZ1518	3000	8	30	110	1	Soft contact	60	40
AZ1518	3000	8	30	110	1			

Table 3. Lithography parameters of bottom contact etching.

The dry etching is then done and stopped in the middle of the InAsSb layer (Figure 18).

### 2.3.3 Dielectric deposition and opening

The next step is the electrical insulation by deposition of a thin film (350 nm) of  $\text{Si}_3\text{N}_4$ . This dielectric layer will avoid the current injection through undesired areas. Two windows are then opened through this layer, on top of the ridge and on top of the bottom contact, where the metal will be deposited later. The opened surfaces define the contact surface between the metal and the contact layers.

The 350-nm thick  $\text{Si}_3\text{N}_4$  layer is deposited by PECVD at  $280^\circ\text{C}$  (see section 5.2.3), and the opening areas are then defined by photolithography. The same parameters as for the laser ridge definition are used (Table 1). The alignment should be very precise because any shift in the alignment will result in an unprotected ridge sidewall and an unsuccessful current injection.

The openings are then realized by ICP etching in another machine equipped with F-based gases, which are more efficient for dielectric materials. The etching was controlled by a laser tracking signal as for the etching of semiconductors. The recipe is very selective; which prevents damaging the semiconductor material.

### 2.3.4 Metallization

The final main fabrication step is the deposition of the metal contacts in order to inject the current into the device. A photolithographic step allows defining the regions of the metal contacts: on top of the GaSb p-type layer and the InAsSb n-type layer. Then, the metal deposition is done followed by a lift-off of the resist to remove the metal from the undesired zones (see section 5.2.4)

Here, a negative resist should be used for the lift-off. At this step, the surface of the sample shows height differences larger than  $3\ \mu\text{m}$ . In order to guarantee an effective lift-off, we use a double layer technique to obtain a thicker resist layer. It consists in using two resists with different solubilities in the developer which creates a shape that promotes the discontinuity of the metal layer. The lithography parameters are given in Table 4.

LOR5A					AZ2020				
Spin-coating			Soft bake		Spin-coating			Soft bake	
v (rpm)	Ramp (s)	t (s)	T ( $^\circ\text{C}$ )	time	v (rpm)	Ramp (s)	t (s)	T ( $^\circ\text{C}$ )	time
4000	2	30	180	2 mins	4000	2	30	110	1 min

Exposure		PEB bake		Development
Contact mode	time	T ( $^\circ\text{C}$ )	time	time
Soft contact	7 s	110	1 min	1 min 45 s

Table 4. Lithography parameters of the metal contact step.

After photolithography and before the metal deposition, the native oxide should be removed to ensure the ohmic contacts. The de-oxidation is done by dipping the sample in a hydrochloric acid solution  $\text{HCl}:\text{H}_2\text{O}$  (1:4).



The deposition of Ti/Au (20/400 nm) is performed by e-beam evaporation (see section 5.2.4). The 20-nm Ti layer is used to improve the adhesion of the contacts to the sample surface and the 400-nm gold layer is used to get ohmic contacts. Note that the use of Al-based contacts, which are CMOS-compatible contacts, is possible for our GaSb-based materials. [102] Afterwards, we performed the lift-off by using an acetone bath to dissolve the resist and lift the metal from the undesired areas.

A sketch of the entire process flow is shown in the figure bellow (Figure 20).

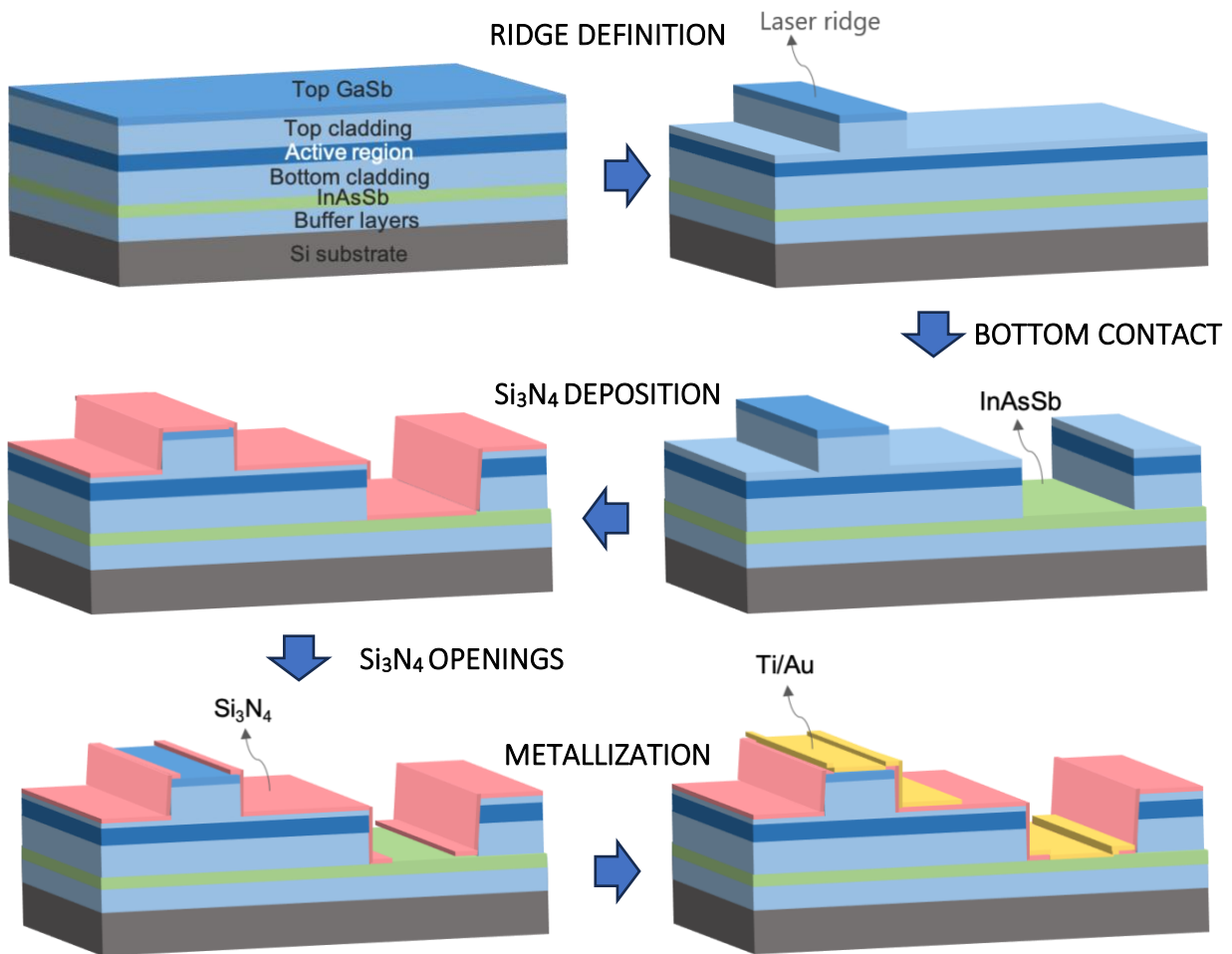


Figure 20. Sketch of the fabrication process of DLs on Si.

In the case of DLs on native GaSb substrates, the bottom contact step is skipped. Instead, Pd/AuGeNi (5/200 nm) is deposited directly on the backside of the GaSb substrate after thinning down the substrate. This second metal deposition acts as the n contact. After deposition, an annealing at 200°C is performed to form the ohmic contact on the n-side of the DL.

The next step is the cleavage which forms the mirrors of the Fabry-Perot cavity. For this purpose, the substrate is thinned down by mechanical polishing down to around 150  $\mu\text{m}$ . Thin samples allow for a high-quality cleavage resulting in a high-quality Fabry-Perot cavity, especially for DLs grown on Si, which is a hard material and tends to have a deformed cleavage

from the (110) to the (111) plane. We then cleaved the sample in different laser bars with different cavity lengths. No special treatment was applied to improve the reflectivity of the cleaved facets. The laser bars were then soldered onto Cu heat sinks and measured on a probe station.

## 2.4 Laser characterizations

In this section, I will first describe the setup used for laser characterization. Then, I will explain how important information can be extracted from these measurements. The laser characterizations will then be confronted to a theoretical gain model.

### 2.4.1 General aspects of laser characterization

All measurements have been done on a probe station by placing manually the probes on the laser contacts. They consist on injecting a current into the device and measure the electrical and optical characteristics of the diode laser. A L-I-V plot is obtained which shows the current-voltage curve (I-V) together with the current-light output curve (L-I). This measurement can be done in two different regimes: pulsed operation and continuous-wave (CW) operation. The pulsed mode, used for broad-area lasers ( $\sim 100 \mu\text{m}$  ridges), prevents the device from self-heating and allows accessing the intrinsic characteristics of the laser structures, in particular the laser threshold. In addition, the effects due to the sidewalls of the ridge can also be neglected with broad-area lasers. In this configuration, the light emitted by the laser is measured by a non-calibrated, liquid-nitrogen cooled, InSb photodetector. The CW measurements are performed with narrow-ridge ( $5\text{-}10 \mu\text{m}$ ) DLs to better mimic the actual operating conditions in practical situations. In this case, the devices heat up and thermal effects appear. Besides the I-V characteristics, the light output is measured with a calibrated powermeter. A typical L-I-V plot is represented in Figure 21.

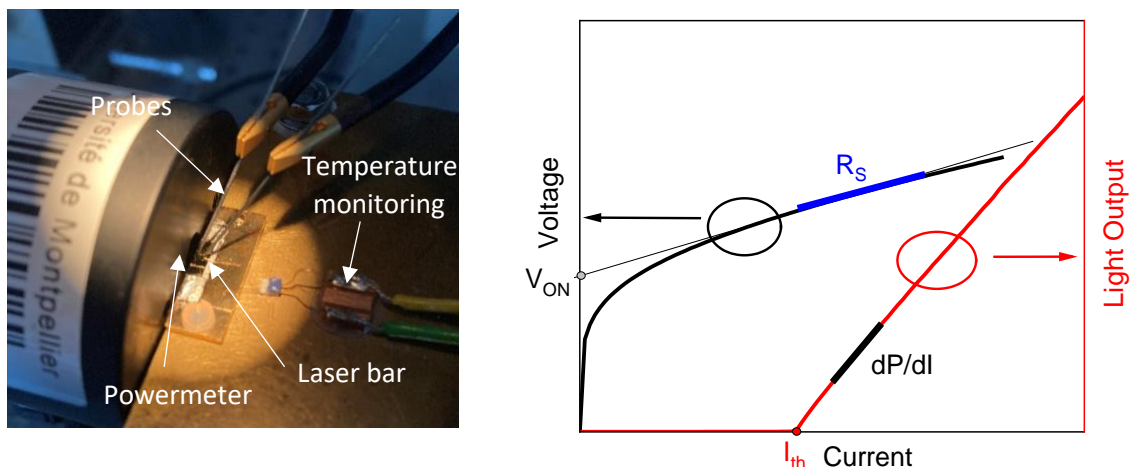


Figure 21. Representation of a L-I-V curve from a laser characterization.

From this L-I-V curve, several parameters can be extracted which give information on the device. From the I-V curve, one can extract the turn-on voltage ( $V_{ON}$ ) by taking the intercept of the tangent of the I-V curve with the voltage axis. The slope  $V/I$  of the I-V curve tangent gives the series resistance of the diode ( $R_s$ ) which is composed of the resistance of the material, the resistance of the metal contacts and the resistance of the welding. From the L-I curve, one can identify the threshold current  $I_{th}$  (Figure 21) that is the current required to achieve lasing (see section 5.1). The smaller the threshold current and the series resistance, the lower the power consumption of the device. The threshold current density,  $J_{th}$ , is the ratio of the threshold current to the surface of current injection (cavity length x ridge width). It is the preferred metric in pulsed operation of broad-area devices for evaluating the intrinsic qualities of the laser structure. In CW operation, one can extract the external quantum efficiency ( $\eta_d$ ), defined as the ratio of the number of emitted photons ( $\frac{\lambda dP}{hc}$ ) to the number of injected carriers ( $\frac{dI}{q}$ ) which gives the Equation 1.[103]  $\eta_d$  can thus be calculated by measuring the slope efficiency of the L-I curve  $\frac{dP}{dI}$  above the threshold:

$$\eta_d = \frac{q\lambda dP}{hc dI}$$

Equation 1. External quantum efficiency.

where  $q$  is the electron charge,  $\lambda$  is the emission wavelength,  $h$  is the Planck's constant and  $c$  is the speed of light.

The internal quantum efficiency ( $\eta_i$ ) refers to the ratio of the number of photons generated by an electron-hole pair recombination to the number of carriers injected into the active region. The photons generated within the waveguide can be absorbed or scattered, giving an intrinsic value of the optical losses: the internal losses ( $\alpha_i$ ). The external quantum efficiency  $\eta_d$  is related to these two parameters  $\eta_i$  and  $\alpha_i$ . The evolution of  $\frac{1}{\eta_d}$  with the cavity length of the laser allows extracting the internal losses  $\alpha_i$  and the internal quantum efficiency  $\eta_i$  using the following equation:[104]

$$\frac{1}{\eta_d} = \frac{1}{\eta_i} + \frac{\alpha_i}{\eta_i \ln(R^{-1})} L$$

Equation 2. The inverse of the external quantum efficiency as a function of the cavity length.

where  $L$  is the Fabry-Perot cavity length and  $R$  is the reflectivity of the mirrors, assuming that they have the same reflectivity.

To extract these parameters, it is therefore necessary to cleave laser bars of different cavity lengths.

An important requirement for various applications is also the temperature stability. Therefore, the laser properties are also measured as a function of the temperature in CW. As

discussed before, the temperature affects the laser threshold and the slope efficiency  $dP/dI$ . In fact, it increases non-radiative recombination rates, leading to an increase in the threshold current and a decrease in the quantum efficiency, and thus in the optical power. The temperature dependence of the threshold current and the external quantum efficiency is given by the empirical exponential equations[105]:

$$I_{th} = I_0 \exp\left(\frac{T}{T_0}\right)$$

$$\ln(I_{th}) = \ln(I_0) + \frac{T}{T_0}$$

*Equation 3. Characteristic temperature related to the threshold current.*

$$\eta_d = \eta_{d0} \exp\left(-\frac{T}{T_1}\right)$$

$$\ln(\eta_d) = \ln(\eta_{d0}) - \frac{T}{T_1}$$

*Equation 4. Characteristic temperature related to the external quantum efficiency.*

The so-called characteristic temperatures  $T_0$  and  $T_1$  represent the sensitivity to the temperature of the laser threshold current and the external quantum efficiency, respectively.

## 2.4.2 Laser properties

As explained above, broad-area lasers were first characterized in pulsed operation at room temperature (RT) to assess the threshold current density of the structure. As an example, the L-I curves of the 1.5-mm long DLs with varying QW numbers on both GaSb and Si substrates are plotted in Figure 22.

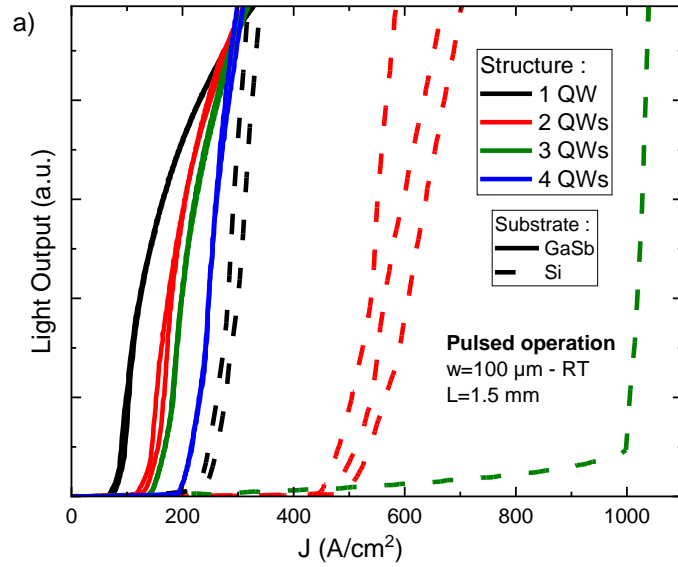


Figure 22. Broad-area laser characteristics in pulsed operation for the two series. Light output versus current density curves of 1.5 mm-long DLs with different numbers of QW.

To get an overview of the whole set of results, the evolution of the threshold current density as a function of the number of QWs ( $n_{QW}$ ) for different cavity lengths is shown in Figure 23. Due to the much higher threading dislocation density in DLs on Si compared to those on GaSb, threshold current densities are higher. For DLs on Si, they range from 193 to 1155 A/cm<sup>2</sup> for a number of QWs ranging from 1 to 3, respectively, whereas for DLs on GaSb, they range between 68 and 238 A/cm<sup>2</sup> for a number of QWs ranging from 1 to 4, respectively. For both series, the threshold current density increases with the number of QWs regardless of the cavity length; therefore, the best threshold is achieved with the structures having one QW, whatever the substrate. However, the slope of  $J_{th} = f(n_{QW})$  is significantly steeper for DLs grown on Si than for those grown on GaSb. As a consequence, we could not reach the threshold current with the DLs fabricated from the 4-QWs-structure grown on Si. Indeed, the extrapolated threshold would be as large as  $\sim 2.3$  kA/cm<sup>2</sup>, which is beyond the limit of our setup. In contrast, the threshold current density obtained with the 1-QW structure (200 A/cm<sup>2</sup>) is the best reported so far for GaSb-based DLs grown on Si.[62]

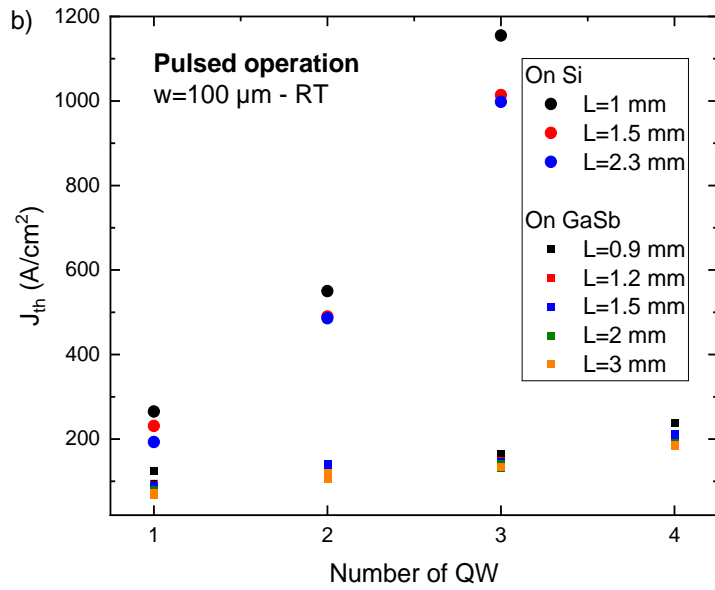


Figure 23. Broad-area laser characteristics in pulsed operation for the two series. Threshold current density versus the number of QWs for different cavity lengths.

Narrow-ridge were then characterized in CW operation at RT. The L-I-V data of DLs with an 8- $\mu\text{m}$  wide ridge and different cavity lengths are plotted in Figure 24.a) for DLs on Si and in Figure 24.b) for DLs on GaSb. The turn-on voltage for DLs on Si is in the 0.7-1 V range and the series resistance is around 4  $\Omega$ , comparable to that measured with DLs on GaSb substrates. DLs on GaSb exhibit threshold currents from 40 to 84 mA for cavity lengths between 1.5 and 3 mm. On the other hand, for DLs on Si the threshold currents vary between 75 and 120 mA for cavity lengths between 1 and 2.3 mm, which are again the best results ever reported with GaSb-based DLs grown on Si.[62]

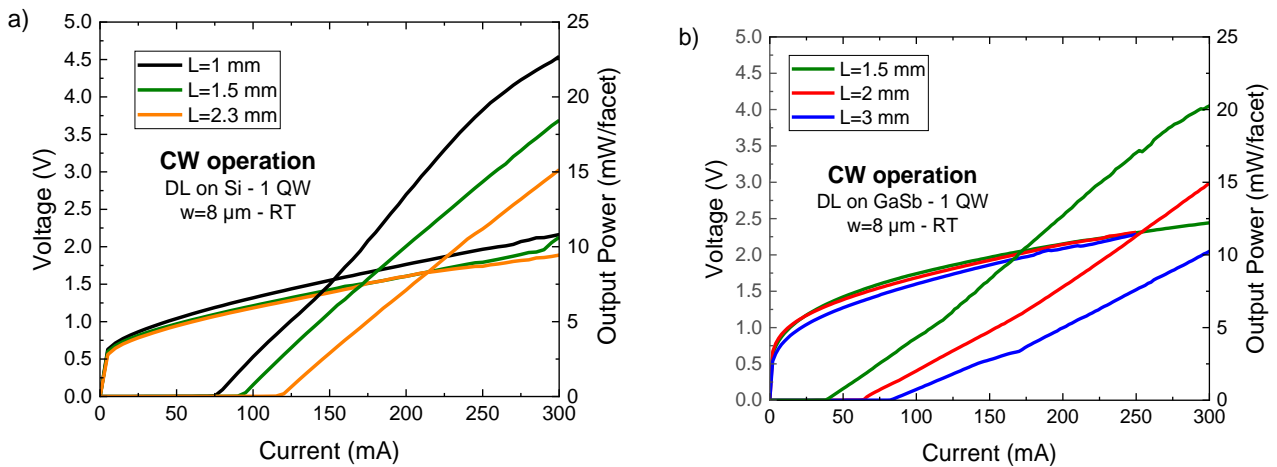


Figure 24. L-I-V data in CW for 1-QW DLs with an 8  $\mu\text{m}$ -wide ridge and different cavity lengths. a) On Si substrate. b) On GaSb substrate.

The internal quantum efficiency and the internal losses are calculated by using the Equation 2. The internal losses as a function of the number of QWs for DLs on Si and on GaSb are plotted in Figure 25. The results and trends are similar for both. The internal losses increase with the QW number, which we ascribe to increasing free carrier absorption and inhomogeneous carrier injection in the multi-QW structures.[106] In contrast the internal quantum efficiency  $\eta_i$  remains relatively constant between 40-50% for all structures.

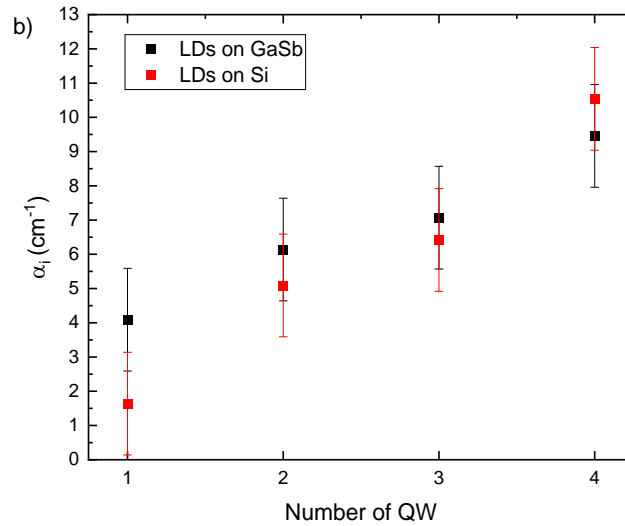


Figure 25. Extracted internal losses versus the number of QWs for the two series.

Narrow-ridge DLs were also measured for different temperatures in CW. As an example, the L-I data for 2-QWs DLs grown on GaSb and Si, with a 10- $\mu\text{m}$  wide ridge and a 1-mm long cavity is plotted in Figure 26 for measurement temperatures from 20 to 70°C (limited by the experimental setup). The threshold current varies between 42 and 82 mA for DLs on GaSb and between 120 and 200 mA for DLs on Si. The external quantum efficiency, which is proportional to the slope  $\frac{dP}{dI}$ , is lower for DLs grown on Si. Through Equation 3 and Equation 4, we deduced the characteristic temperatures  $T_0$  and  $T_1$ .  $T_0$  is similar on both substrates (91 and 97 K), whereas  $T_1$  is lower for DLs on Si (117 K vs 147 K). Similar trends have been observed for all QW numbers. The lower  $T_1$  for DLs on Si than on GaSb reflects the fact that the high TDD makes the external quantum efficiency sensitive to temperature.





Besides the internal losses,  $J_{tr}$  and  $G_0$  are needed to calculate the threshold current density from Equation 5. These parameters can be deduced from the optical gain of a single QW structure, which is calculated as a function of the energy of the emitted photon  $E$  and the carrier density  $N$ , thanks to the following equation:[103], [109], [110], [111]

$$g(E, N) = \frac{\pi e^2 \hbar M_t^2}{\varepsilon_0 n c m_0 E} \rho(E) (f_c(E, N) - f_v(E, N))$$

Equation 7. Optical gain of a single QW structure.

where  $\rho(E)$  is the density of states,  $f_c(E, N)$  and  $f_v(E, N)$  are the Fermi functions in the conduction band and in the valence band, respectively,  $M_t$  is the dipole matrix element, and  $n$  is the real part of the refractive index. The gain broadening caused by the intraband scattering is taken into account in the model by convoluting the calculated gain by a Lorentzian function (Equation 8), [103], [109]

$$L(E) = \frac{1}{\pi} \frac{\hbar/\tau_{in}}{\left(\frac{\hbar}{\tau_{in}}\right)^2 + E^2}$$

Equation 8. Lorentzian function.

where  $\tau_{in}$  is the instersubband relaxation time.

The modal gain is then obtained using the following expression:[103], [109]

$$G_{modal}(E, N) = N_W \Gamma_W G_{conv}(E, N)$$

Equation 9. Modal gain.

where  $G_{conv}$  is the gain convoluted with the Lorentzian function.

Afterward, we calculated the modal gain at the energy of the peak modal gain. Finally, we calculated the modal gain as a function of the current density  $G_{modal}(J)$  by substituting  $N$  by  $J$ , thanks to the following equation:

$$J = \frac{q N_w L_w}{\eta_i} (AN + BN^2 + CN^3)$$

Equation 10. Current density as a function of the recombination coefficients.

where  $L_w$  is the QW width,  $\eta_i$  is the internal quantum efficiency taken from the experimental results, and  $A$ ,  $B$ , and  $C$  are the SRH, radiative, and Auger recombination coefficients, respectively.[81]

The modal gain as a function of the current density  $G_{modal}(J)$  is now known, and the parameters  $J_{tr}$  and  $G_0$  can, finally, be extracted using the following equation (Equation 11), as well as the threshold current density seen above (Equation 5):

$$G_{modal}(J) = N_W \Gamma_W G_0 \ln\left(\frac{J}{J_{tr}}\right)$$

Equation 11. Modal gain as a function of the current density.

## 2.6 Discussion

We fitted these  $J_{th}$  values to the experimental values for both series of DLs on GaSb and DLs on Si, by adjusting the SRH coefficient  $A$  (Equation 10), while  $B$  and  $C$  were taken from the literature.[107], [109] We used the same  $B$  and  $C$  coefficient for both substrates since they are intrinsic to the materials and heterostructures.

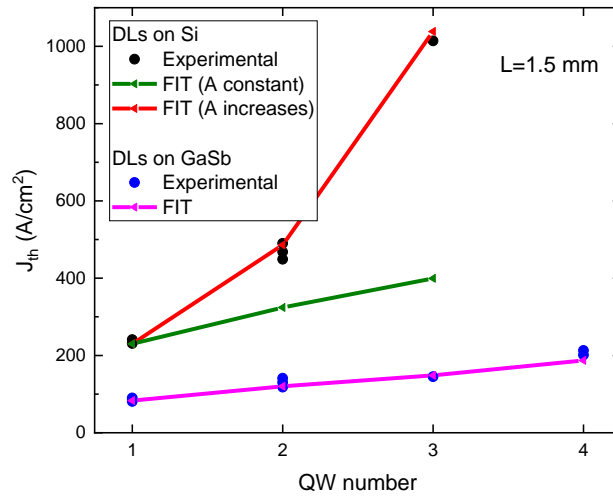


Figure 27. Fits of the threshold current density for the two series for the 1.5-mm long DLs.

Figure 27 shows the experimental and fitted  $J_{th}$  values for the two series. The agreement for the DLs on GaSb is excellent. In contrast, for DLs grown on Si, it was not possible to adjust all experimental curves assuming the same SRH coefficient  $A$  (Figure 27), which suggests that for these DLs, the  $A$  coefficient increases with the number of QWs. We tentatively ascribe this behavior to the introduction of two new QW/barrier interfaces for every additional QW in the structure. In turn, at such high dislocation densities, misfit dislocation arms propagate at each interface and create additional non-radiative recombinations,[112], [113], [114] which is also consistent with the steep variation in the threshold current density with the number of QWs observed for the DLs grown on Si (Figure 23).

Coefficient	DLs on GaSb	DLs on Si		
	1-4 QWs	1 QW	2 QWs	3 QWs
$A$ ( $s^{-1}$ )	$3.9 \times 10^7$	$1.1 \times 10^8$	$1.3 \times 10^8$	$2.4 \times 10^8$
$B$ ( $cm^3 s^{-1}$ )	$4.4 \times 10^{-10}$	$4.4 \times 10^{-10}$	$4.4 \times 10^{-10}$	$4.4 \times 10^{-10}$
$C$ ( $cm^6 s^{-1}$ )	$2 \times 10^{-28}$	$2 \times 10^{-28}$	$2 \times 10^{-28}$	$2 \times 10^{-28}$

Table 5. Recombination coefficient values.

The final values used to fit all data are in table. For the  $A$  coefficient, the final values calculated for the DLs grown on GaSb are close to those found in the literature, [107], [109] whereas much higher values have to be used for the DLs grown on Si to account for non-radiative SRH recombination introduced by the dislocations. [115] As we can see in the Equation 12, the increase of the SRH coefficient  $A$  results in an increase of the threshold current density.

$$J_{th} = \frac{qN_wL_w}{\eta_i} (AN_{th} + BN_{th}^2 + CN_{th}^3)$$

Equation 12. Threshold current density as a function of the recombination coefficients.

Finally, we show in Figure 28.a) the calculated modal gain vs current density curves for all DLs grown on both GaSb and Si substrates. First, we observe that the transparency current density  $J_{tr}$  ( $J$  for which the modal gain equals zero) increases with the number of QWs, as expected. Above transparency, the differential modal gain increases with the number of QWs. [116] For the DLs grown on Si, the larger SRH recombinations increase the transparency current and all curves are shifted toward larger current densities, whereas the modal gain decreases. This results in an increased laser threshold (Equation 5), as also observed experimentally in Figure 23.

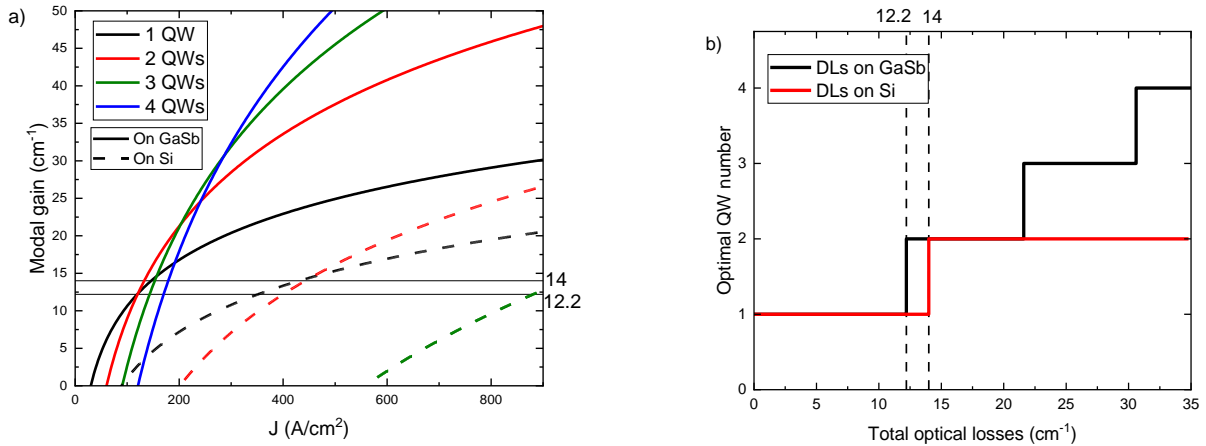


Figure 28. The gain model calculations for the two series. (a) Modal gain vs current density curves for different number of QWs. (b) The optimal number of QWs vs the total optical losses.

Figure 28.a) can be used to determine the optimal number of QWs if the total losses are known. The total losses of DLs grown on native GaSb substrates have typically been measured by different groups in the 10–20 cm<sup>-1</sup> range. [108], [109], [117] If we consider total losses of 10 cm<sup>-1</sup>, for example, the modal gain equals this value at the laser threshold. The lowest threshold current density is then obtained for a structure having one QW (Figure 28.a)). In contrast, for total losses of 15 cm<sup>-1</sup>, the lowest threshold current density is obtained for a structure with two QWs (Figure 28.a)). In fact, when the optical losses increase, the optimal number of QWs switches from one to two QWs at 12.2 cm<sup>-1</sup> in the case of DLs on GaSb and at 14 cm<sup>-1</sup> in the case of DLs on Si, as it is summarized in Figure 28.b). The fact that these values are very similar

(12.2 and 14 cm<sup>-1</sup>), and that the optimal number of QWs for both DLs on Si and on GaSb is the same (one QW), indicates that threading dislocations do not introduce significant optical losses to the structures, in contrast to what is often claimed. It also confirms the results shown in Figure 25 where the extracted internal losses for both DLs on Si and on GaSb are very similar.

## 2.7 Conclusion

In this chapter we have studied the effect of threading dislocations on the performance of GaSb DLs.

I first presented the structure design of the GaSb diode lasers under study. Two series of DLs containing different number of QWs in their active zone were grown on GaSb and Si substrates. I introduced the different fabrication techniques and showed in details the fabrication process of these DLs. Afterwards, we showed the laser properties in the CW regime for narrow ridges and in pulsed operation for broad-area lasers. As expected, DLs on Si have worse performance than that of DLs on GaSb in terms of threshold current.

The laser properties were then confronted to a theoretical model. This comparison showed that the gain properties in the structure are deteriorated when the TDD is high, due to an increase of the SRH recombination coefficient  $A$ . The transparency current density increases and the differential modal gain is drastically reduced, resulting in an increase of the threshold current density. In the case of DLs on Si, the coefficient  $A$  increases with the number of QWs whereas it remains constant for DLs on GaSb. We then observed, thanks to the theoretical model, that an increase of the total optical losses results in an increase of the optimal number of QWs. By studying the modal gain as function of the current density for different QWs and substrates, we demonstrated that since the optimal number of QWs is the same for both substrates, threading dislocations do not introduce additional optical losses.

This work allows a better understanding of performance degradation arising from threading dislocations, which is important for the decision making regarding the heterostructure design. This allowed us to demonstrate record threshold currents for GaSb DLs grown on Si thanks to a single QW heterostructure (200 vs. 400 A/cm<sup>2</sup> in pulsed operation).[62] Although the performance of DLs on Si has been improved in terms of threshold, the still-too-high TDD drastically affects the laser lifetime. Reducing the TDD is therefore the main objective to achieve similar performance to that of DLs on GaSb.

## 3 Chapter 3. Integration of GaSb-based diode lasers on a Si PIC

As seen in section 1.5.2.2, high performance discrete mid-IR lasers on Si have already been demonstrated. The next step towards fully integrated mid-IR Si photonic chips is the integration of these lasers on a Si PIC with light coupled into a waveguide (WG). In this chapter, I explore the optical coupling between GaSb DLs and waveguides based on a butt-coupled geometry (see section 1.4). The laser and waveguide being on the same chip, cleavage is not an option to form the optical cavity mirrors. Therefore, I first developed a cleavage-free DL process, which I will show in detail. This study demonstrated that this new process gives DLs with similar performance to that of cleaved DLs. This DL process was then transferred and adapted to DLs grown on a Si PIC, and I will present the properties of these DLs directly fabricated on the PIC and the light coupling results. Finally, I will discuss these results with simulations carried out by another PhD student M. Paparella, which allowed us to understand the critical aspects of this configuration and the coupling efficiency value obtained in this investigation.

This work started in the framework of the H2020 program of the European Union (REDFINCH, GA 780240 and OPTAPHI, GA 860808),[118] in collaboration with the Polytechnic University of Bari (Italy), the Munster Technological University and the Tyndall National Institute in Cork (Ireland). The collaboration started with the thesis of L. Monge-Bartolomé.[100]

### 3.1 Configuration

The Si photonic platform under study mimics what a real, albeit simple, PIC would be. As a first approach, we considered only WGs without any other optical function. We decided to use the GaSb diode lasers emitting near  $2.3 \mu\text{m}$  studied in chapter 2. The DL structure is the same as that shown for DLs on Si in section 2.1, with 2 QWs in the active zone. As discussed in section 1.1.2, SiN-based WGs are a very promising platform thanks to their low losses and wide transparency window in the SWIR. We therefore decided to use these materials for our WGs.

They consist of a 0.8  $\mu\text{m}$ -thick SiN layer for the core, clad by two SiO<sub>2</sub> layers: 3.9  $\mu\text{m}$  for the bottom cladding and 1  $\mu\text{m}$  for the top cladding (Figure 29). The thickness of the bottom cladding was chosen to vertically align the active zone of the DL with the passive core of the WG. The thickness of the top cladding should not exceed the p-cladding + top contact of the DL, to ensure a good and uniform contact between the lithography mask and the resist on top of the laser stack for future process steps. Figure 30 shows a cross-section sketch of the configuration. There is an unavoidable air gap between the laser and the waveguide, which I will explain in the next section.

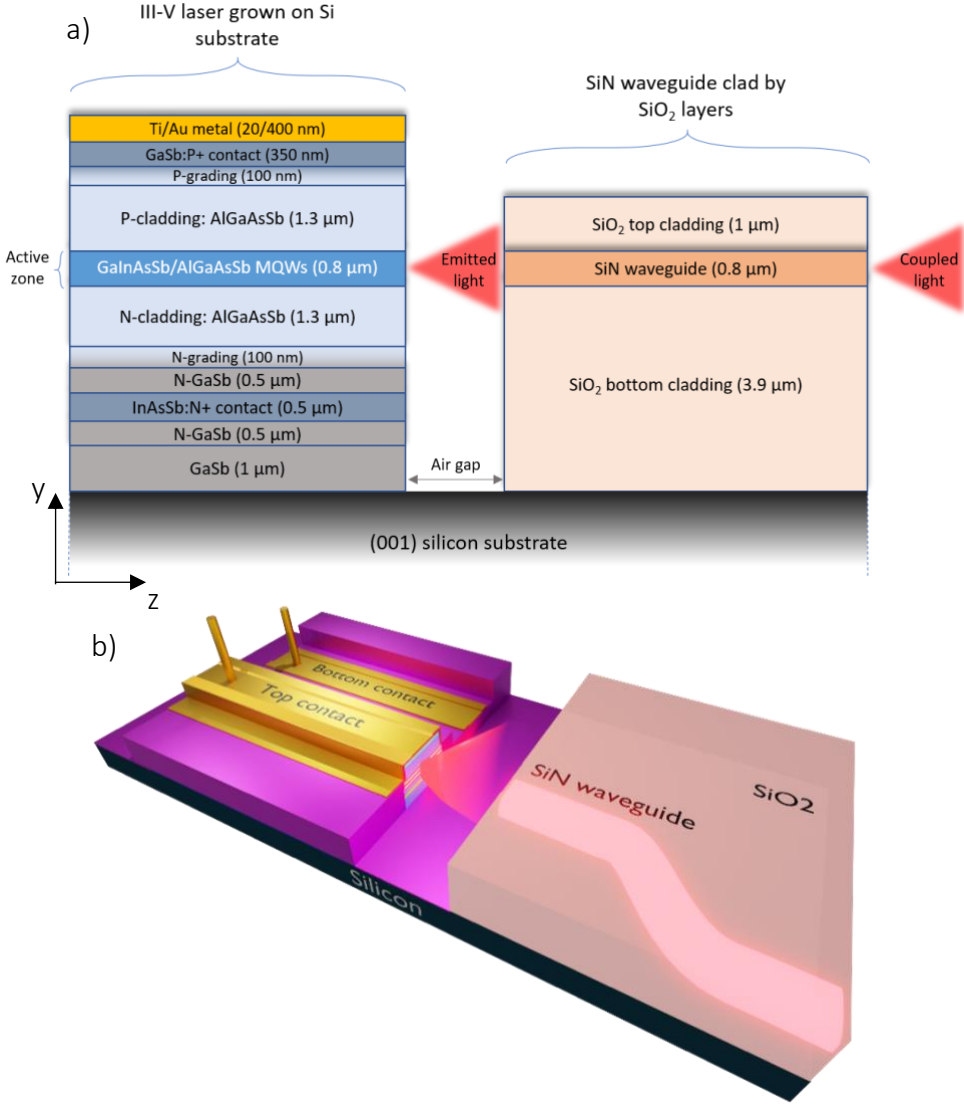


Figure 29. a) Cross-section and b) 3D sketch of an integrated GaSb DL on a Si PIC with light coupled from the active zone of the DL to the core of the waveguide.

### 3.2 Challenges

A number of challenges had to be faced in the experimental study. We chose to fabricate the lowest loss SiN waveguides, which require deposition and treatment at high temperatures

(above 400°C). Lasers cannot withstand these temperatures, so there was no option but to fabricate the WGs first, pattern the PIC wafers to define the epitaxy areas, and then epitaxially grow and process the DL structure. During the fabrication of the Si PIC, it was crucial not to damage the crystal quality of the Si substrate, as GaSb epitaxy is extremely sensitive to the Si surface organization.[61] The epitaxial growth of the DL heterostructure on the Si PIC was also challenging, as in our team DL heterostructures had only been grown on plain Si substrates. Also, since MBE is not selective, the GaSb laser structure was deposited as a polycrystal on top of the amorphous WG stack and at the DL/WG interface during epitaxy. A dedicated wet etching process had then to be developed to remove the undesired III-V polycrystal material. Note that this step creates an unavoidable air gap at the DL/WG interface (Figure 30). Since in the monolithic approach the DL and WGs are on the same chip, cleavage is not an option to form the DL cavity mirrors as we did in section 2.3. A new DL process involving dry etching of the facets had to be developed to obtain high quality mirrors. This process impacts the air gap size between the DL and the WG. Finally, the entire DL process was carried out without compromising the quality of the Si PIC.

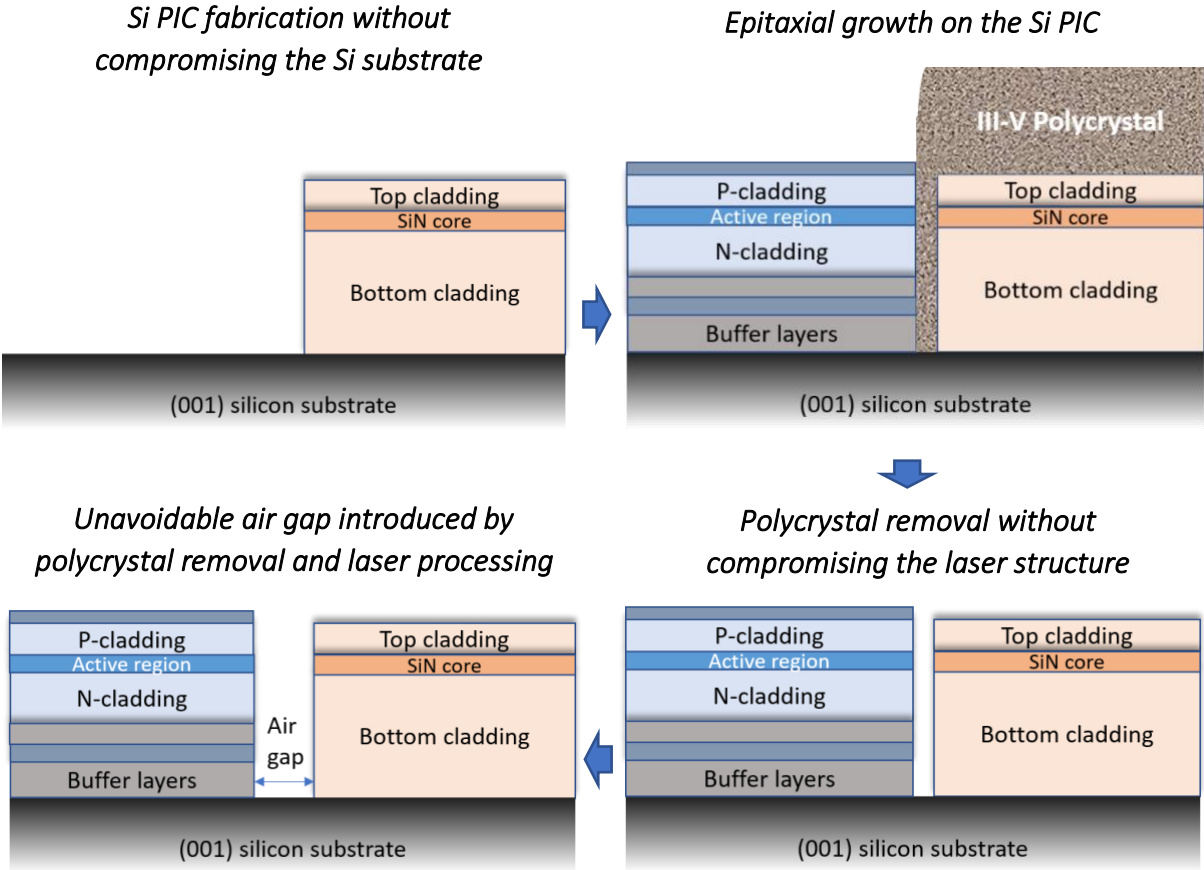


Figure 30. Cross-section sketch of challenging fabrication steps of the integration of the DL on the Si PIC in order to couple light from the active zone of the DL to the core of the SiN waveguide.

An IR camera image of the light beam at the output of a cleaved DL was previously taken, showing a high vertical divergence of the light beam (Figure 31). The beam divergence at the output was as high as 60°. [121] This high value is due to the high contrast in refractive index between the DL active zone and air (3.695 vs 1) and to the narrow output aperture of the DL (0.8 μm).

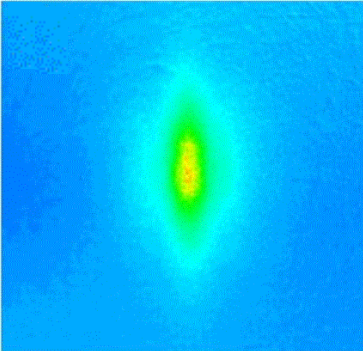


Figure 31. Light beam output of a DL taken with an IR camera. [120]

As illustrated in Figure 32, the size of the air gap is expected to have a drastic effect on the light coupling due to the high divergence of the laser beam. If the air gap is narrow (Figure 32.a), more light is coupled than if the air gap is large (Figure 32.b). A major challenge was therefore to achieve an air gap as narrow as possible to maximize the light coupling.

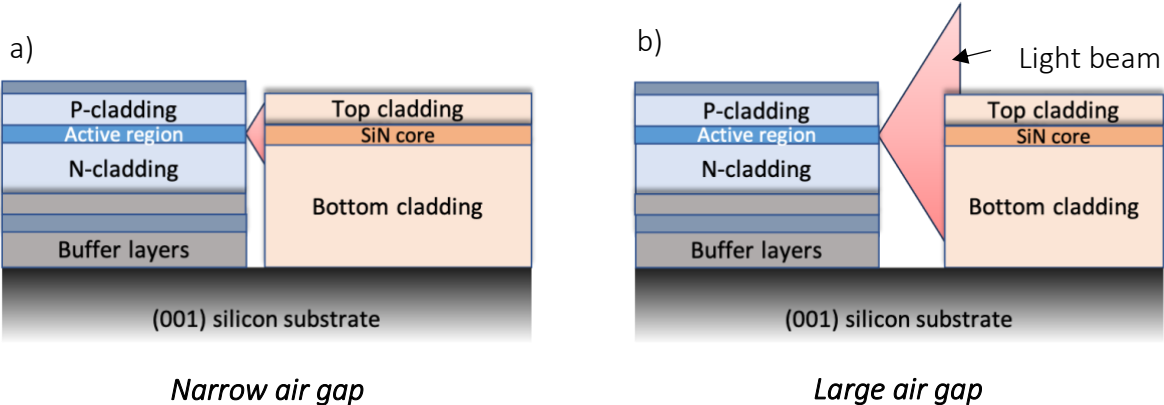


Figure 32. Cross-section sketch of the effect of the air gap on the light coupling.

I will start by addressing one of the key challenges: the development of a new cleavage-free DL process with high-quality facets.

### 3.3 Etched-facet DLs

The objective of this section is to form high quality facets. This requires the facet to be smooth to have good reflectivity and preserve laser performance, and vertical to promote light coupling. According to Fresnel’s equations, when a beam of light reaches an interface between two media with different refractive indices with an incident angle of 90°, the transmitted beam is not deflected from the direction of incidence. Conversely, if the facet angle is larger (resp. smaller) than 90°, the beam will be deflected downwards (resp. upwards). The aim is therefore



to achieve a facet that is as vertical as possible in order to avoid any deviation of the light beam and to ensure that the coupling is maximized.

Wet etching has been studied to form etched facets for GaAs-based lasers, but chemical techniques lead to under-etching of the material, resulting in low facet reflectivity.[122], [123] On the other hand, dry etching techniques can avoid under-etching and provide anisotropic profiles. Focused ion beam (FIB) is a very efficient and precise technique for facet-etching that has been used mainly for very small and high-resolution patterns.[124] However, this technique requires etching the laser facets one by one and is not available in our laboratory. On the other hand, ICP etching (see section 5.2.2), has also been demonstrated to be a good alternative for obtaining high quality facets,[125], [126], [127], [128], [129] and all laser facets on a PIC could be etched in a single process step. Especially, a previous work in our team by L. Monge-Bartolomé *et al.* has demonstrated high-quality etched facets using ICP, similar to those formed by cleavage.[119], [120] A smooth facet was achieved in this work but the facet angle was  $102^\circ$ , which is not optimal for light coupling. Here, I decided to use ICP etching as well and my aim was to achieve a facet angle of  $90^\circ$  while preserving the facet smoothness.

I will first present the development of smooth and vertical facets. Then, I will adapt this etched-facet process to fabricate etched-facet DLs. I will end with the DLs characterizations and conclusions.

### 3.3.1 Fabrication of a smooth and vertical facet

I have studied the fabrication of etched facets using photolithography and ICP etching. Several parameters play an important role in the etched-facet profile. First, the mask is a critical factor since the pattern is transferred from this mask to the semiconductor. The mask flanks should therefore be smooth and vertical. Various lithography parameters can be optimized to obtain the desired profile. The mask material should be resistant so that it does not etch away. Also, the etching recipe should be selective with respect to the mask. I used a resist mask as a starting point.

#### 3.3.1.1 Resist mask

I decided to start with a positive resist: AZ1518 (see section 2.3.1). Then, the ICP recipe had to be chosen. Etching of GaSb-based and Al-rich materials using  $\text{BCl}_3$ ,  $\text{Cl}_2$  and Ar gases, similar to what was used in chapter 2 (see Table 2), has been previously studied.[125], [126], [127] When a high  $\text{Cl}_2$  flow is used, chemical etching dominates, the etch rate is high and the facets are rough. In contrast,  $\text{BCl}_3$  favors physical etching: the etch rate is low and the facets are smooth. In addition,  $\text{BCl}_3$  seems to be a very efficient gas for high-Al content layers. Finally, Ar is necessary to avoid very low etch rates. The recipe used in chapter 2 thus seems to be a good compromise between the different gases and to favor physical etching with  $\text{BCl}_3$ . I therefore decided to use the same recipe.

To fabricate the etched-facet lasers, the structure must be etched at least through the active zone. I chose to stop in the middle of the bottom cladding because the longer the etching time, the less vertical the facet.[120] At an etch rate of  $\sim 350$  nm/min, the etching time is 9 minutes and the depth is  $\sim 3.2$   $\mu\text{m}$ . The AZ1518 resist with standard lithography parameters is thick enough ( $\sim 1.8$   $\mu\text{m}$ ) to withstand the 9-minute etching. Preliminary tests were first conducted on GaSb substrates.

### 3.3.1.1.1 Vacuum contact

As explained in section 5.2.1, there are different contact modes between the lithography mask and the sample. The vacuum contact mode is the mode in which the highest pressure is applied. A high pressure is intended for high resolution patterns as it allows for vertical resist flanks. So, I decided to do a lithography using vacuum contact as a starting point for this study. The lithography parameters are the same as in Table 1. The morphology of the resist flank is shown on the scanning electron microscopy (SEM) images in Figure 33.a and the semiconductor flank after 9 minutes of etching is shown in Figure 33.b. The facet angle is  $94^\circ$  and the roughness is high.

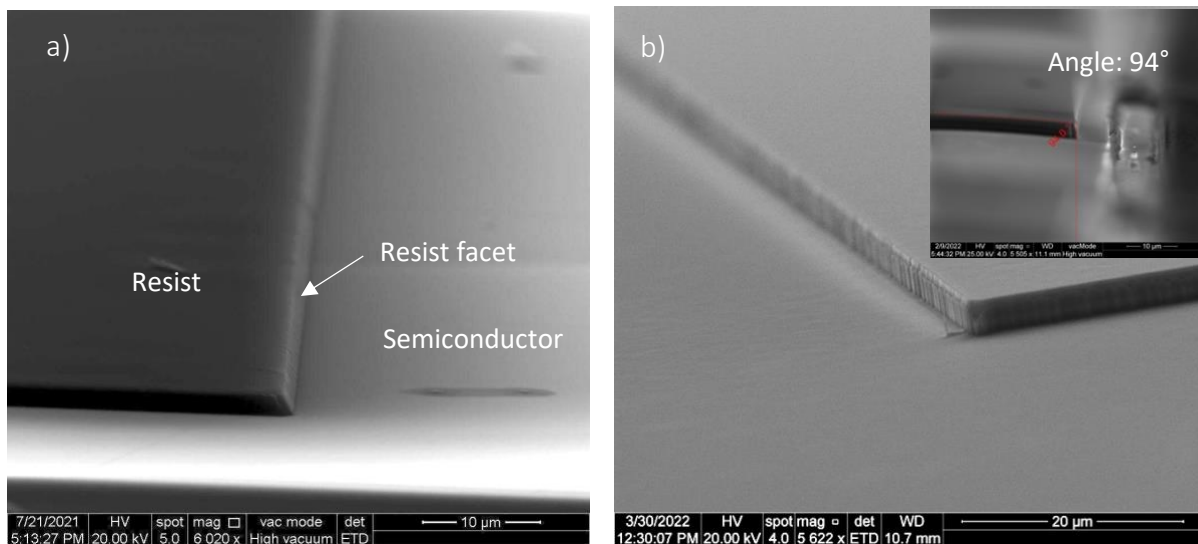


Figure 33. Resist profile after a standard lithography using a) soft contact and b) vacuum contact.

A SEM picture of the chromium mask used in photolithography was previously taken in our team showing that the edges of the pattern are not completely straight (Figure 34). This results in rough flanks of the resist. The resist should therefore be subjected to some treatments to reduce its roughness.

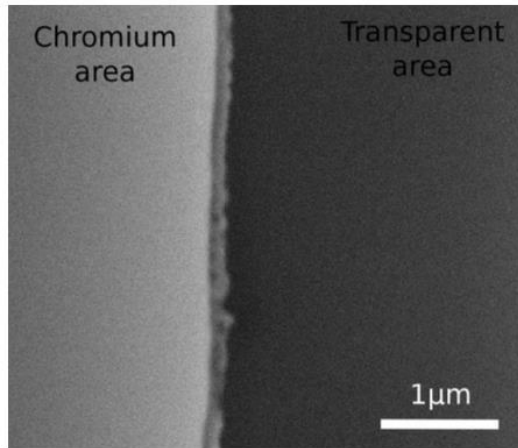


Figure 34. SEM image of the chromium mask used during photolithography.[120]

#### 3.3.1.1.2 Hard bake

As explained in section 5.2.1, a hard bake can be performed after development to change the resist profile,[130] so I decided to do some tests by introducing a hard bake for different temperatures and times to see if an improvement could be achieved. Table 6 shows the different resist flank profiles for two different temperatures (110°C and 115°C) and three different times (1,2 and 4 minutes).

The temperature and duration of the hard bake influence the resist making it flow and round at the edges. The verticality decreases but the smoothness of the flank increases. A 5°C increase in temperature results in a very round flank. However, at a fixed temperature, increasing the time from 1 to 4 minutes changes slightly the resist profile. Overall, hard bake temperature and time make the resist flank round and less vertical, but smoother.

	T=110°C	T=115°C
1 min	<p>7/21/2021 HV spot mag □ vac mode det 5:10:25 PM 20.00 kV 5.0 6 009 x High vacuum ETD</p>	
2 mins	<p>8/31/2021 HV spot mag □ vac mode det WD 3:11:08 PM 20.00 kV 5.0 9 876 x High vacuum ETD 11.8 mm</p>	<p>8/31/2021 HV spot mag □ vac mode det 4:19:48 PM 20.00 kV 5.0 9 051 x High vacuum ETD</p>
4 mins	<p>7/21/2021 HV spot mag □ vac mode det 10:41:58 AM 20.00 kV 5.0 4 000 x High vacuum ETD</p>	<p>7/20/2021 HV spot mag = WD vacMode 10:38:57 AM 20.00 kV 5.0 6 000 x 10.1 mm High vacuum</p>

Table 6. SEM pictures of resist flanks after hard bake for different temperatures and times.

Table 7 shows the SEM pictures of the corresponding semiconductor flanks after 9 minutes of etching.

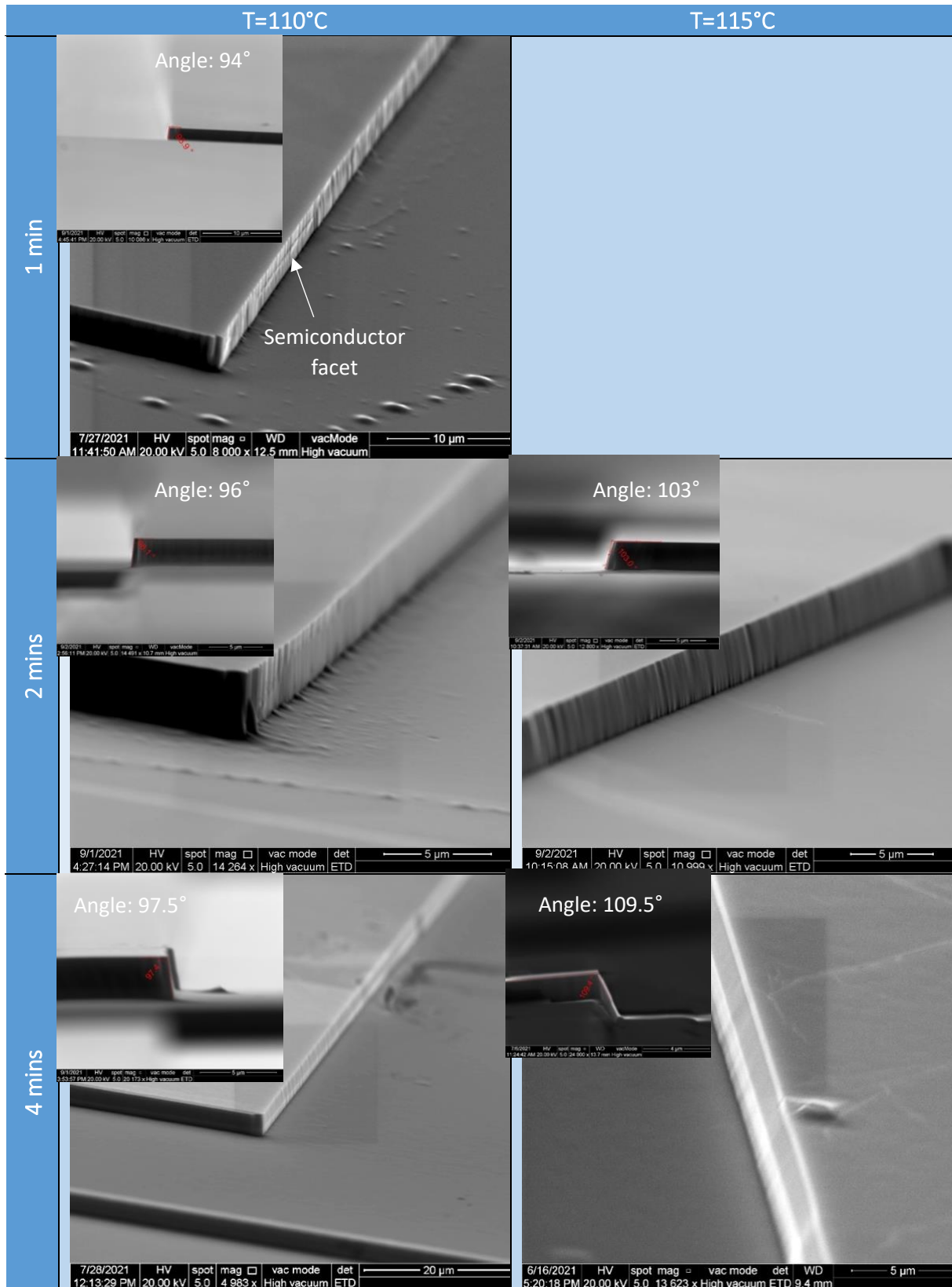


Table 7. SEM pictures of semiconductor flanks after hard bake for different temperatures and times and an etching time of 9 minutes.

As the pattern is transferred from the resist mask to the semiconductor, the semiconductor flanks become smoother and less vertical as the hard bake time and temperature increase.

Figure 35 shows a sketch summarizing what we observed in this series of tests.

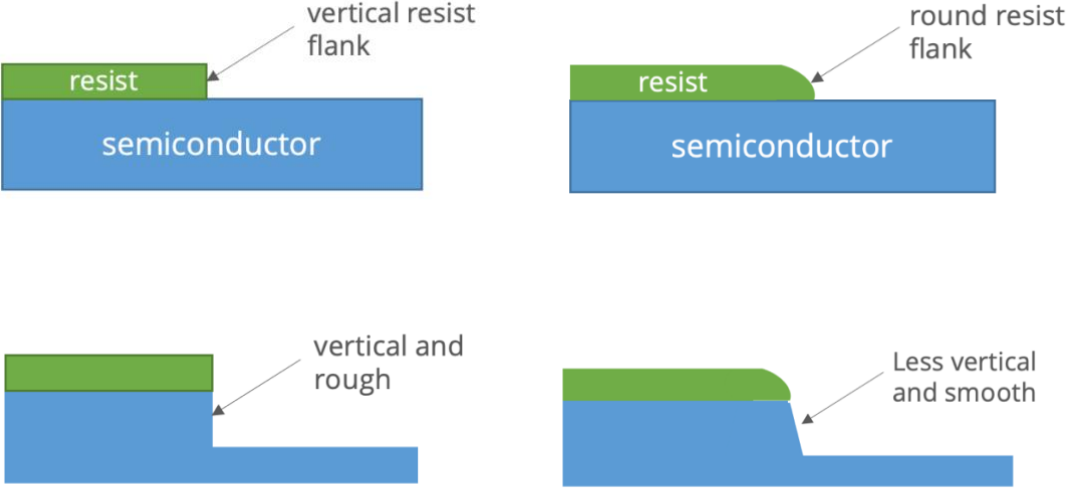


Figure 35. Sketch of the influence of the hard bake on the resist and semiconductor flanks. a) no hard bake is performed. b) hard bake is performed.

A hard bake at 115°C for 2 minutes or at 110°C for 4 minutes gives very smooth flanks and one can expect a reflectivity similar to that of cleaved facets,[119], [120] but the flanks are not vertical. I then decided to use a hard mask, which should give a more anisotropic etching and is widely used in the industry.

**3.3.1.2 Hard mask**

A hard mask can be obtained by transferring a pattern from a resist to an underlying material that is usually more resistant and will serve as a mask for etching the device structure. This more resistant material will provide mechanical and chemical stability during the etching. Figure 36 shows a sketch of the most common method of fabricating a hard mask.

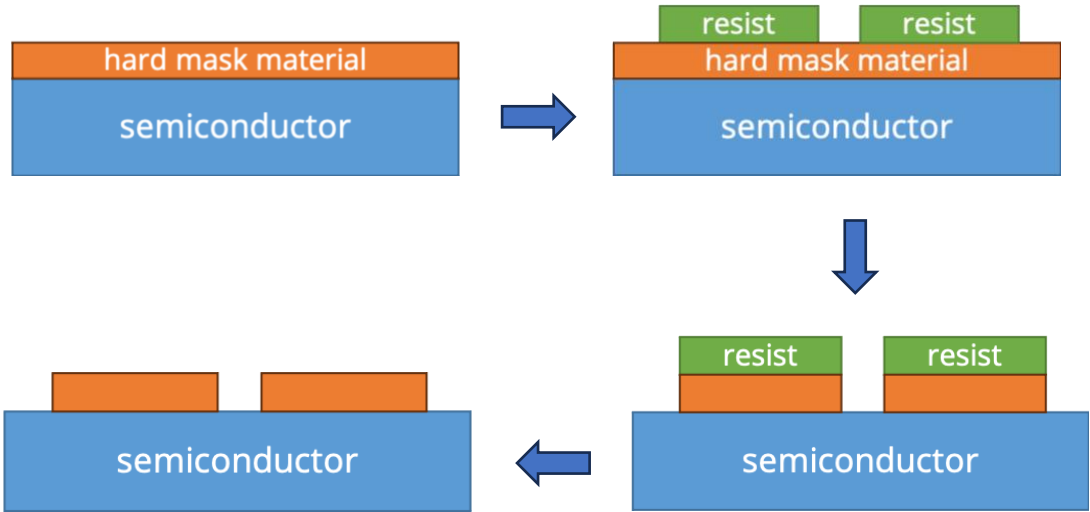


Figure 36. Sketch of the fabrication of a hard mask.

The most commonly used hard mask materials are dielectrics such as SiO<sub>2</sub> or SiN, and various metals. The fabrication of metal hard masks involves a lift-off technique (see section 5.2.4), which is a less straightforward technique than the standard UV lithography + etching technique (Figure 36). I therefore decided to use either SiO<sub>2</sub> or SiN, which are available in our facilities by PECVD deposition. SiN is known for its excellent mechanical and chemical stability. In particular, SiN is more resistant than SiO<sub>2</sub> to the Cl-based and Ar etchants used in our standard ICP recipe (Table 2), resulting in higher selectivity than SiO<sub>2</sub>. A SiN hard mask can therefore provide a higher level of anisotropy than a SiO<sub>2</sub> hard mask, making it a preferred material for achieving smooth and vertical sidewalls.[131], [132], [133]

#### 3.3.1.2.1 Development of the hard mask facet process

The first step is to calibrate the SiN thickness needed to withstand the 9-minutes etching of the facet. I did some ICP etching tests with the standard recipe to determine the etch rate of the SiN. I found that the minimum SiN thickness required is around 770 nm. I decided to use 800 nm, a thickness still thin enough to avoid cracks (see section 3.1).

First, the 800-nm thick SiN layer was deposited by PECVD. The photolithography was then performed in vacuum contact mode and without hard bake of the resist. The hard mask openings are then performed using the dedicated ICP recipe. Once the SiN mask is fully opened, the resist is removed to avoid any other masking effect that could affect the verticality of the semiconductor sidewalls. The sample is then transferred to the other ICP machine to etch the semiconductor facet for 9 minutes. Finally, the remaining SiN hard mask is removed by ICP. The semiconductor flank is rough and concave (Figure 37).

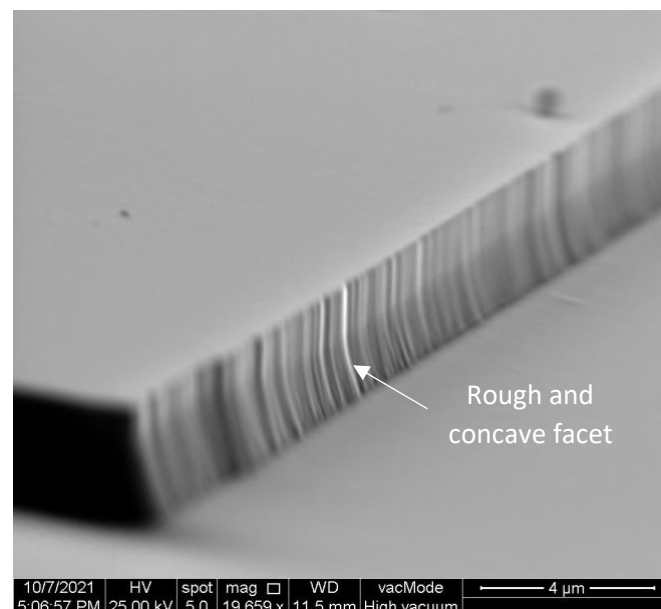


Figure 37. SEM image of the semiconductor flank using SiN hard mask with no hard bake of the resist.

To avoid this problem, I decided to hard bake the resist to smooth its flank and thus that of the SiN mask. The hard bake was performed at 110°C for 4 minutes (see section 3.3.1.1).

SEM images of the semiconductor flank after etching the facet during 9 minutes are shown in Figure 38.

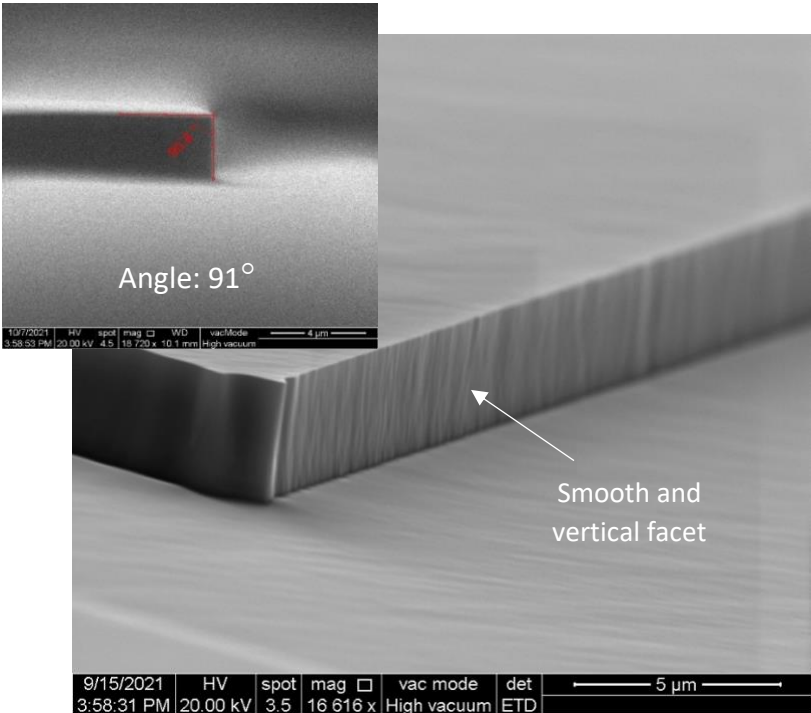


Figure 38. SEM image of the semiconductor flank using SiN mask and a hard bake at 110°C during 4 minutes.

We can observe that when the resist is smoothed with a hard bake, the results are completely different. The flank of the semiconductor is very smooth and has an angle of 91°. With such a facet angle, the angle of the laser beam deviation would be lower than 3°, which can be neglected given the high beam divergence. Note also that the facet roughness is very low, which should result in a reflectivity similar to that of cleaved facets, [119], [120] so I decided to validate this process, and to use it to fabricate an etched-facet DL. The final parameters of the facet process are shown in Table 8.

Hard Mask	Spin-coating				Soft bake		Exposure	
SiN thickness	Resist	v (rpm)	Ramp (s)	t (s)	T (°C)	t (min)	Contact mode	t (s)
800 nm	AZ1518	4000	2	30	110	1	Vacuum contact	30

Development		Hard bake	
t (s)	T (°C)	t (min)	
30	110	4	

Table 8. Hard mask parameters of the facet etching step.

In the next section, I will present a step-by-step description of the etched-facet DL process flow, followed by the DL characterizations. I will also compare the performance of etched-facet DLs with that of cleaved-facet DLs.



### 3.3.2 Process flow of etched-facet DLs

Previous work in our team has demonstrated that defining the facets at the beginning of the process flow results in a more vertical and smoother facet than if it is done in the middle or at the end of the process.[120] In fact, at the beginning of the process, the sample is still planar and the resist after spin-coating is flat and homogeneous. Therefore, the contact between the lithography mask and the sample is good, which improves the verticality. So, I started the process flow by defining the laser facets. The challenge is then to protect the laser facet during the remaining part of the process flow.

I applied the full etched-facet laser process to a typical DL structure grown on a GaSb substrate. Note that if the laser were grown on Si, the results would be the same, since the facet definition does not depend on the substrate. The heterostructure design is the same as that studied in section 2.1. The process flow is divided in different main steps: facet etching, ridge definition, dielectric deposition and opening and metallization.

#### 3.3.2.1 Facet definition

The first step is to define the facets to form the Fabry-Perot cavity. The lithography mask has etched-facet cavities of different lengths (1, 1.5, 2 and 2.5 mm) (Figure 39).

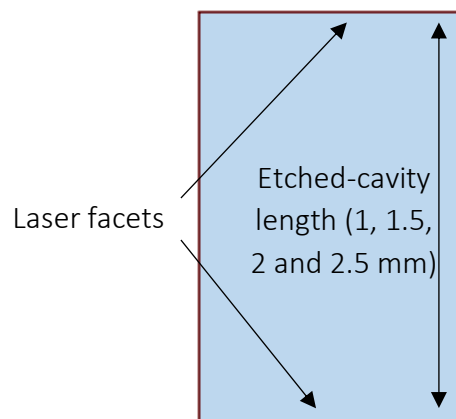


Figure 39. Mask design of the laser facet.

First, the hard mask was fabricated using the same parameters as in the previous section (Table 8). The facet etching was then performed and stopped after passing through the active zone in the middle of the bottom n-cladding (Figure 40).

Stop facet etching here

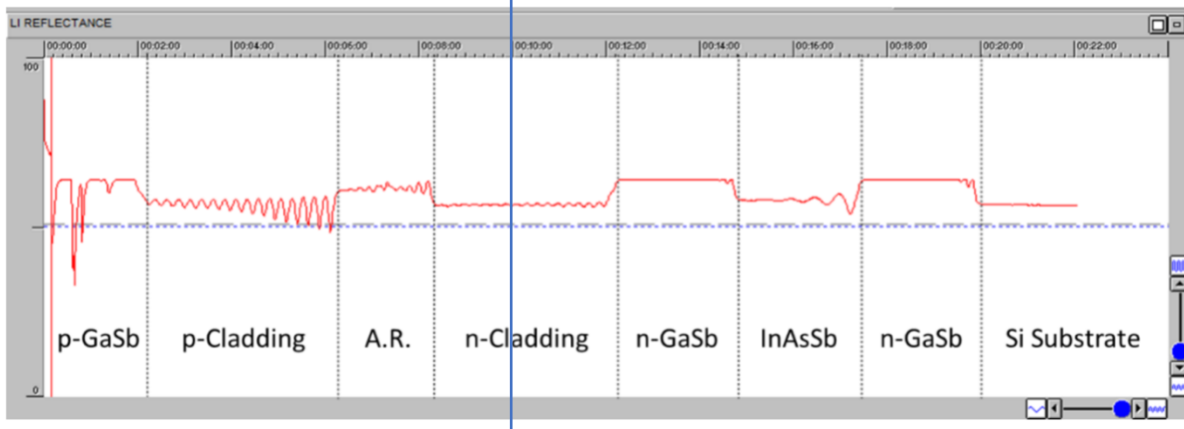


Figure 40. ICP etching tracking signal.

Finally, the laser facet was analyzed by SEM. Figure 40 shows SEM images of a smooth and vertical facet similar to that obtained with a GaSb substrate (previous section). The quality is thus the same whether the etching is performed on a GaSb substrate or on a laser heterostructure.

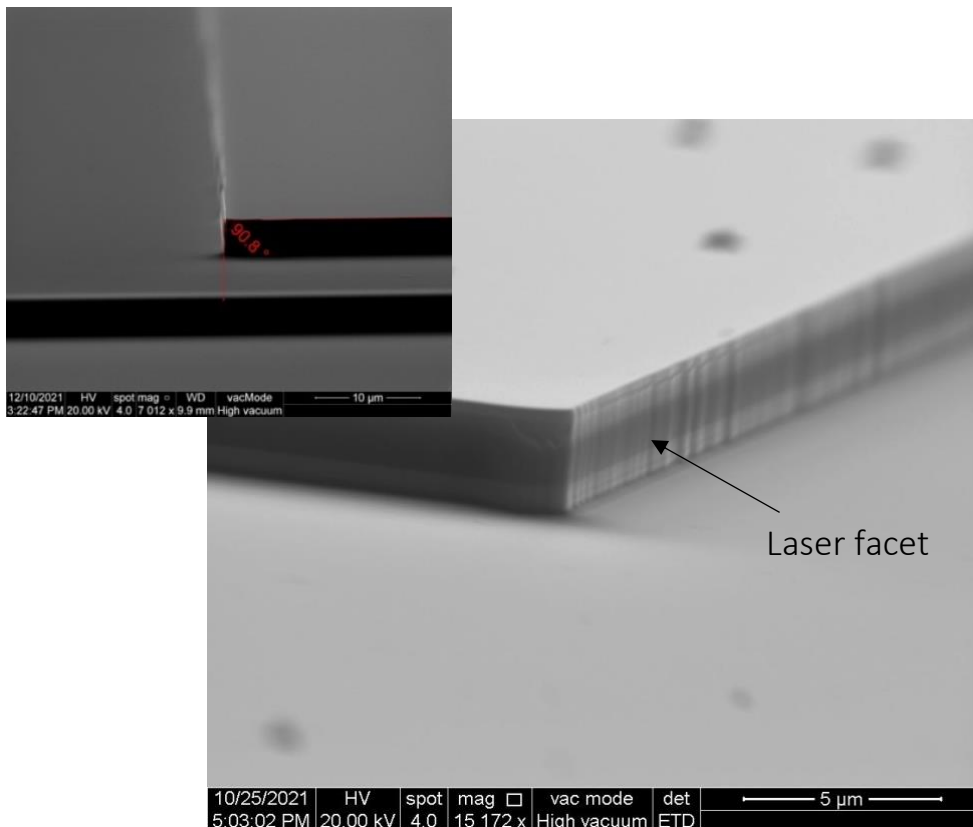


Figure 41. SEM images of the laser facet.

### 3.3.2.2 Ridge definition

The next step is to define the laser ridges. The mask was designed to have ridges 10  $\mu\text{m}$  longer than the etched cavity. At each end of the cavity, the ridges are therefore offset by 5  $\mu\text{m}$

from the laser facet (see Figure 42) to protect the laser facet during etching. The laser ridges are 10- $\mu\text{m}$  wide.

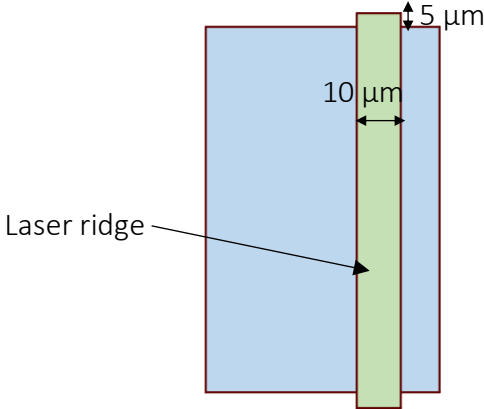


Figure 42. Mask design of the laser ridge.

The resist is thinner on top of the facet than on the planar regions (Figure 43.a). Therefore, to ensure that the resist is thick enough on top of the laser facet, the spin-coating speed was reduced and the exposure time was increased. The photolithography parameters are depicted in Table 9.

Spin-coating			Soft bake		Exposure		Development	
Resist	v (rpm)	Ramp (s)	t (s)	T ( $^{\circ}\text{C}$ )	t (min)	Contact mode	t (s)	t (s)
AZ1518	3000	8	30	110	1	Soft contact	45	50

Table 9. Photolithography parameters for the laser ridge definition for the etched-facet process.

The sample was then transferred to the ICP to perform the dry etching. As with the standard cleaved laser process, the etching was stopped just before reaching the active zone. Figure 43 shows SEM images of the device before (Figure 43.a) and after (Figure 43.b) ridge etching. It can be seen that the resist successfully protected the laser facet during etching.

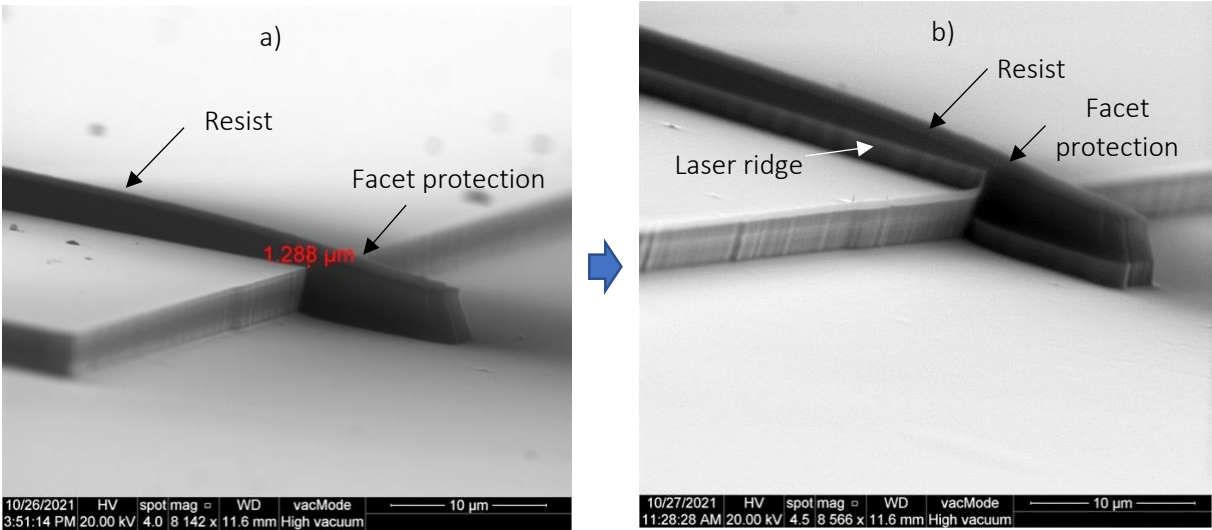


Figure 43. SEM images of the laser ridge definition step. a) after lithography and before ICP etching. b) after ICP etching.

### 3.3.2.3 Insulation and opening

The next step is the electrical insulation. The dielectric opening mask was designed to remove the dielectric from the top of the laser ridges, but also from the laser facets (Figure 44).

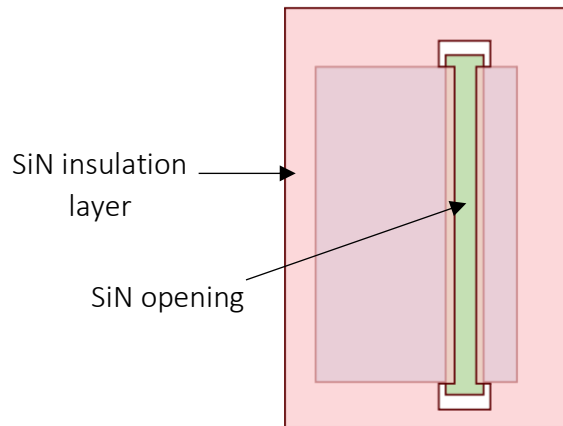


Figure 44. Mask design of the electrical insulation.

After SiN deposition and ICP opening, the sample was examined by SEM to check that the laser facets had not been damaged (Figure 45). We can observe that the dielectric material on the laser facet has been removed without affecting the quality of the facet. We can also observe that small portions of SiN material were not removed. This is due to the high verticality of the facets that acts as a mask during the highly anisotropic ICP etching. The distance between the top of the facet and the remaining dielectric material is around  $\sim 2.9 \mu\text{m}$ , which is well below the active zone and avoids any significant problem.

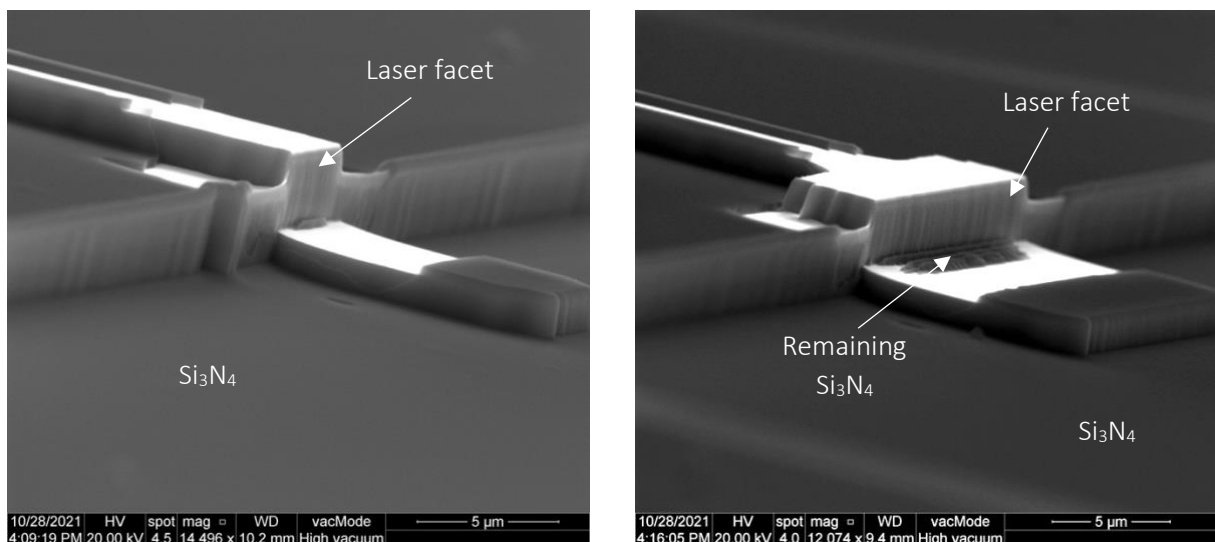


Figure 45. SEM images of the laser facet after the electrical insulation and opening.

### 3.3.2.4 Metallization

The final step is metallization. The metallization mask was designed to deposit the metal with a  $10\text{-}\mu\text{m}$  offset from the laser facets (see Figure 46) to avoid any contamination and to ensure an effective lift-off.

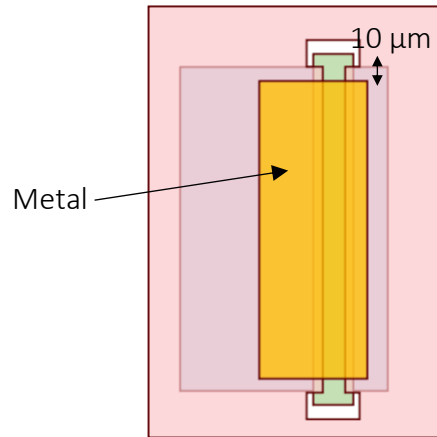


Figure 46. Mask design of the metal deposition.

In this process, we did not use the double layer negative resist as in section 2.3.4 because it would have required dipping the sample in the developer for 2 minutes 30 seconds to remove the LOR5A resist. Since the developer attacks GaSb-based materials, this step could damage the unprotected laser facets. Instead, we used only the negative resist AZ2070, which is thick enough to allow the subsequent lift-off.[134] The lithography parameters are listed in Table 10.

Spin-coating				Soft bake		Exposure	
Resist	v (rpm)	Ramp (s)	time	T (°C)	time	Contact mode	time
AZ2070	4000	2	30 s	110	1 min 10 s	Soft contact	10 s

PEB bake		Development
T (°C)	time	time
110	1 min 10 s	1 min 30 s

Table 10. Photolithography parameters of the metallization step for the etched-facet process.

Prior to metallization, the sample was de-oxidized by immersion in an HCl:H<sub>2</sub>O bath. The metal contacts Ti/Au (20/400 nm) were deposited and the lift-off was performed afterwards. SEM images of the final device are shown in Figure 47.

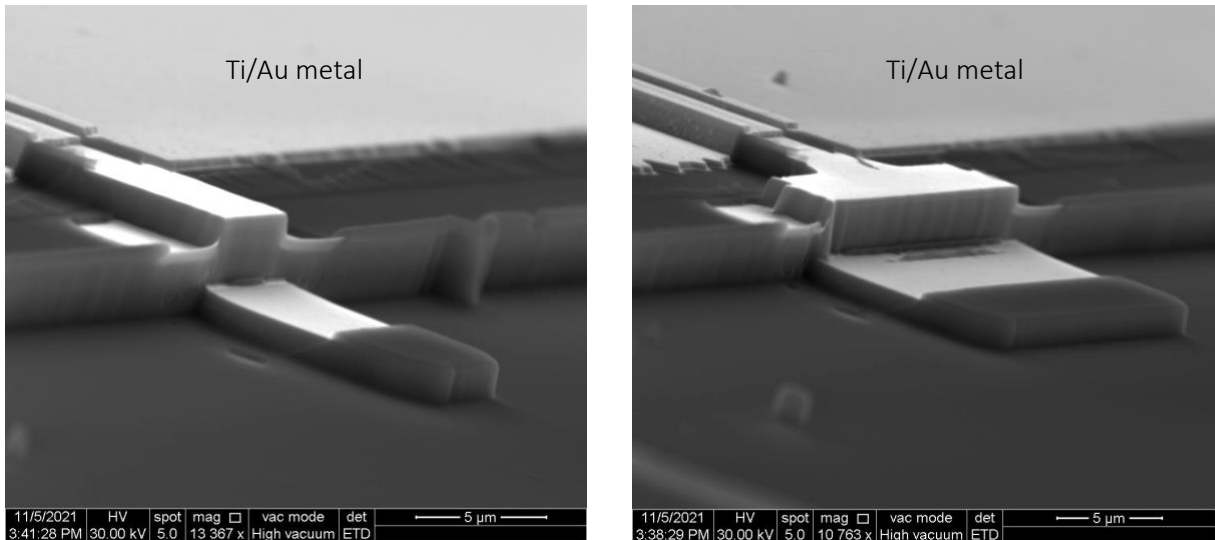


Figure 47. SEM images of the final device after the metallization step.

The substrate was then thinned down to  $\sim 150 \mu\text{m}$  and a Pd/AuGeNi (5/200 nm) metal layer for the n-contact was deposited on the backside of the GaSb substrate as for cleaved DLs on GaSb (section 2.3). A sketch of the entire process is shown in the figure below (Figure 48).

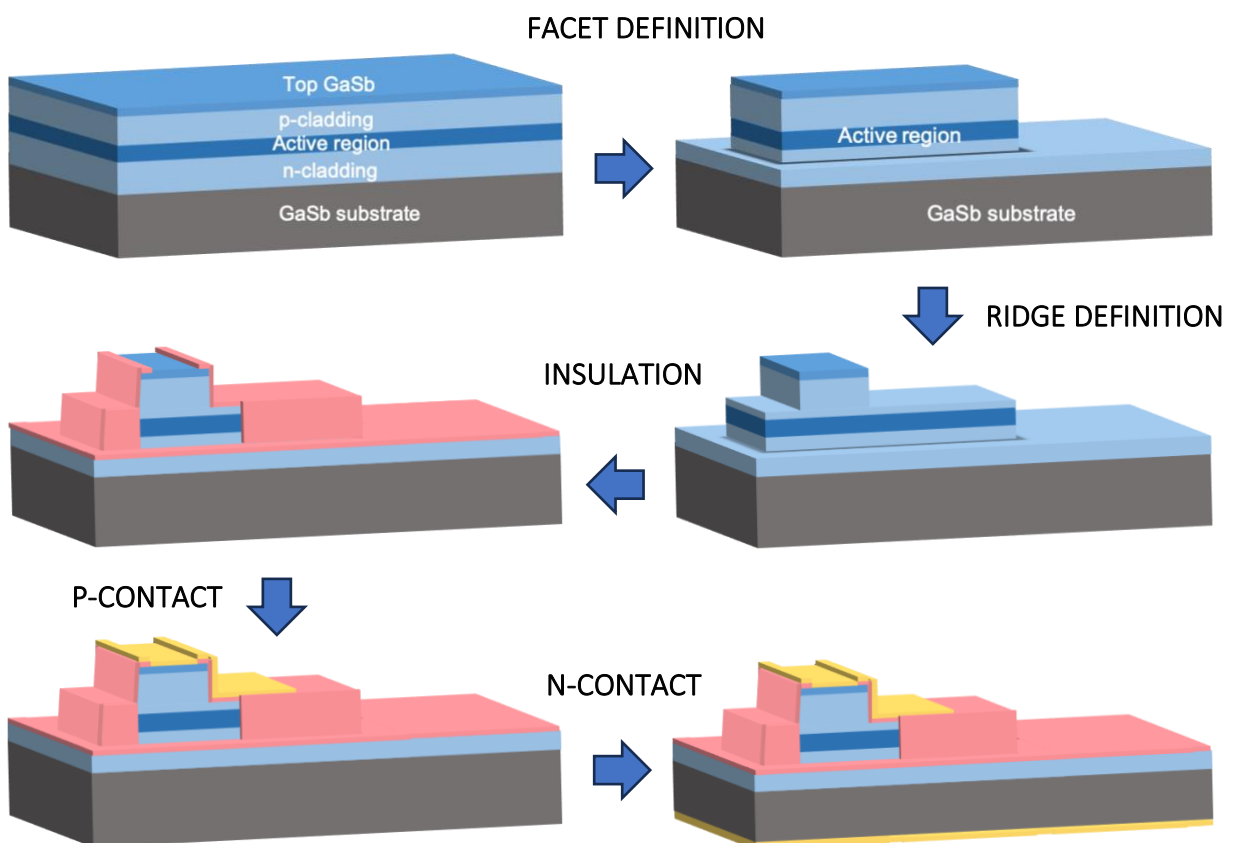


Figure 48. Sketch of the etched-facet DL process flow.

The masks were designed to also have cleaved lasers between the etched-facet lasers (see Figure 49). In addition, they were designed to have a 200- $\mu\text{m}$  distance between the etched-facet lasers of different cavity lengths (see Figure 49). The cleavage was performed in the middle

of this region, so that etched- and cleaved-facet lasers could be obtained side-by-side on the same bar for an easy comparison. The cavity length of the cleaved lasers is therefore  $\sim 200 \mu\text{m}$  longer than that of the etched-facet lasers (Figure 49).

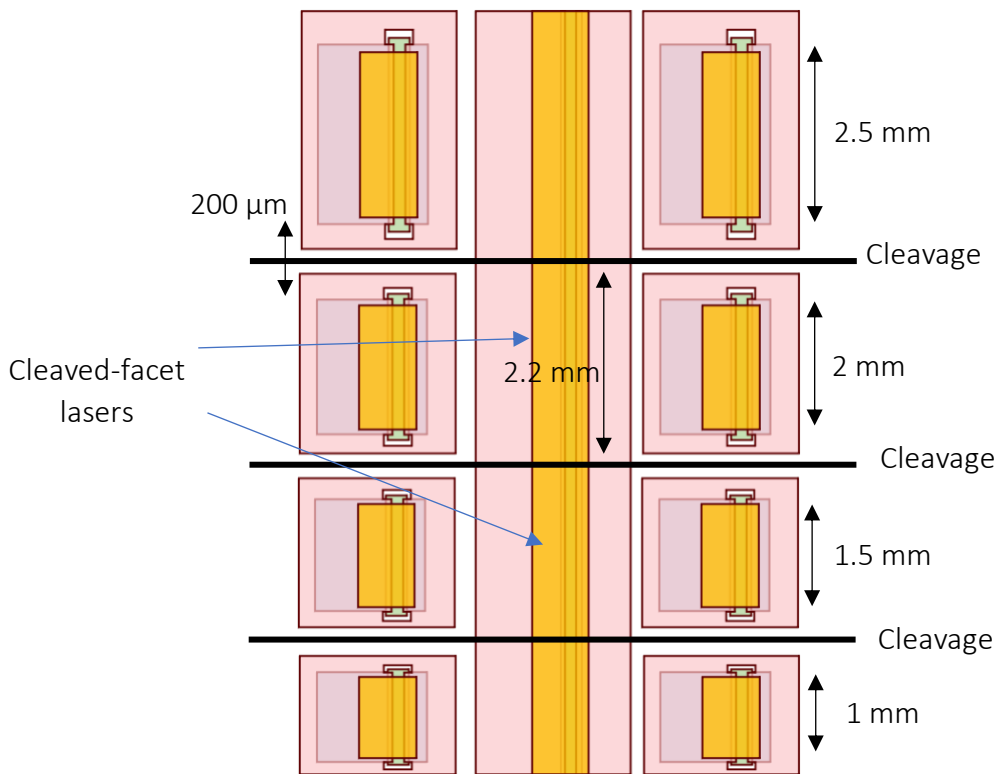


Figure 49. Sketch of the cleavage step. Etched- and cleaved-facet lasers are obtained on the same bar.

Figure 50 shows a bar containing etched- and cleaved-facet lasers. The laser bars are then soldered onto Cu heat sinks for characterization on a probe station.

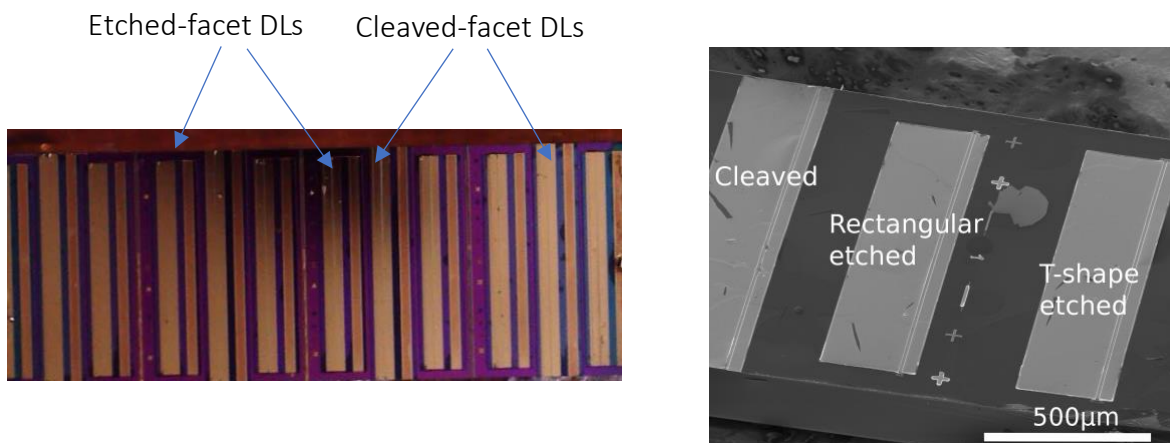


Figure 50. Images of a laser bar with several etched-facet lasers and cleaved lasers. a) optical image. b) SEM image[120].

### 3.3.3 Characterizations of etched-facet DLs

The final step is the characterization of the lasers. We will compare the performance of etched-facet DLs with that of cleaved DLs and conclude on the quality of the etched facets. The L-I-V measurements were performed in CW mode at RT and the light was detected by a calibrated powermeter. Figure 51 shows the L-I-V curves for cleaved- and etched- facet DLs.

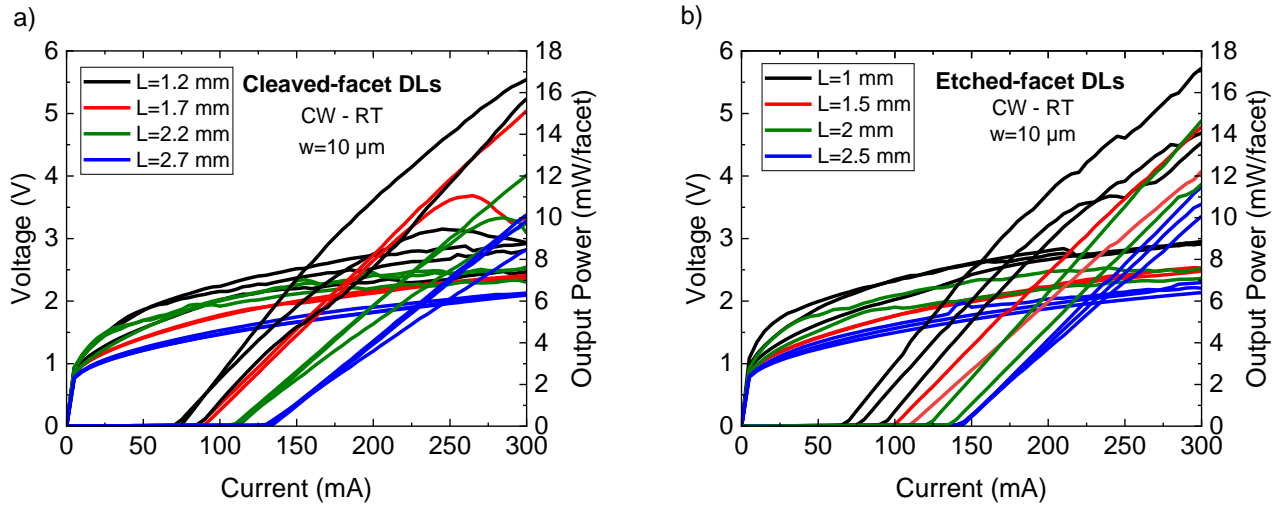


Figure 51. L-I-V curves in CW operation at RT of DLs grown on GaSb substrate with a) cleaved facets and b) etched-facets.

The curves exhibit very similar performance for both cleaved and etched DLs. The I-V curves show a turn-on voltage ranging from 0.8 to 1.4 V for both types of DLs. The series resistance for both varies from 3 to 5.6  $\Omega$  depending on the cavity length. Regarding the L-I curves, the threshold current for cleaved DLs ranges from 70 to 135 mA for cavity lengths from 1.2 to 2.7 mm, respectively. Etched-facets DLs exhibit similar threshold currents ranging from 65 mA for 1-mm long DLs, up to 145 mA for 2.5-mm long ones. In addition, the external quantum efficiency is as well very similar for both, decreasing from approximately 35% to 20% with increasing cavity length (see Equation 2), meaning that no significant optical power is lost with etched-facet cavities. The threshold current density as a function of the inverse of the cavity length in CW and RT for etched-facet and cleaved-facet DLs is shown in Figure 52.



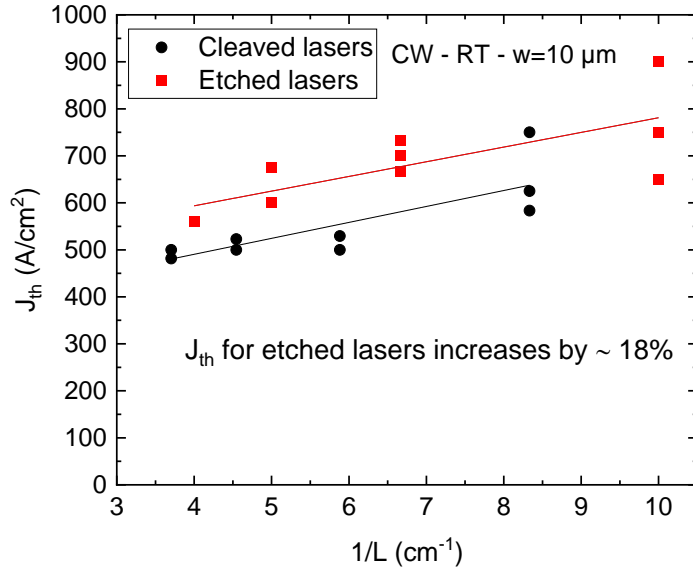


Figure 52. Threshold current density as a function of the cavity length in CW and RT for etched- and cleaved-facet DLs.

The reflectivity of the facets can be analyzed by extracting the slopes of the curves in Figure 52 and using the following equation,[135], [136]

$$J_{th}(L) = J_{th}(\infty) - \frac{C}{L} \ln(R)$$

Equation 13. Threshold current density as a function of the inverse of the cavity length.

where  $J_{th}(\infty)$  is the extrapolated threshold current density for an infinite cavity length,  $C$  is a constant that can be extracted from cleaved-facet DLs,  $L$  is the cavity length and  $R$  is the facet reflectivity.

The constant  $C$  is intrinsic to the laser structure. Therefore, the slope of the curves depends only on the reflectivity of the facet. Since the slope of the curves is the same for both, we can conclude that the reflectivity of the etched-facet DLs is very similar to that of cleaved-facet DLs. However, the threshold current densities for etched-facet DLs are ~18% higher regardless of the cavity length. We attribute this behavior to the fact that in etched-facet DLs, the metal is not in contact with the entire length of the laser ridge (see section 3.3.2.4), creating absorbing regions at both ends of the laser ridges. We thus believe that this is not an effect of the etched facets, but rather a degradation of the performance due to the mask design.

In conclusion, we have established a fabrication process for smooth and vertical facets using SiN hard mask and ICP dry etching. The results are very promising as we have achieved the desired verticality (close to 90°) without losing the smoothness previously obtained in our team. A complete etched-facet DL process was then performed by incorporating the facet etching step and carefully adapting it to ensure protection of the laser facet during the entire process. The performance of etched-facet DLs was compared with that of cleaved-facet DLs

fabricated on the same sample. The laser performance is very similar for both, leading us to conclude that the reflectivity of etched-facet cavities is close to that of cleaved-facet cavities. This process has therefore been validated and will be transferred and adapted to fabricate these etched-facet DLs on the Si PIC with the aim of coupling the laser light into the SiN waveguides.

### 3.4 Fabrication of SiN-based waveguides

The first step is the fabrication of the Si PIC composed of the SiN-based waveguides and the Si recessed areas. The WGs were processed in the 100 mm Si CMOS line of the Tyndall National Institute in Cork. First, the 3.9- $\mu\text{m}$  thick SiO<sub>2</sub> bottom cladding layer was realized through thermal oxidation of the (001) silicon wafers. This thickness was chosen to allow the growth of the thick buffer layer of the laser structure while maintaining the vertical alignment of the passive core of the WG with the active zone of the laser. The passive core was then fabricated by depositing 0.8  $\mu\text{m}$  of SiN by PECVD, followed by the patterning of the WGs with an s-bend shape using UV lithography and ICP etching. The widths of the WGs were chosen to be 10, 15 and 20  $\mu\text{m}$ . 1  $\mu\text{m}$  of SiO<sub>2</sub> was then deposited by PECVD for the top cladding. A sketch of the front view of this first part of the PIC process is presented in Figure 53.a.

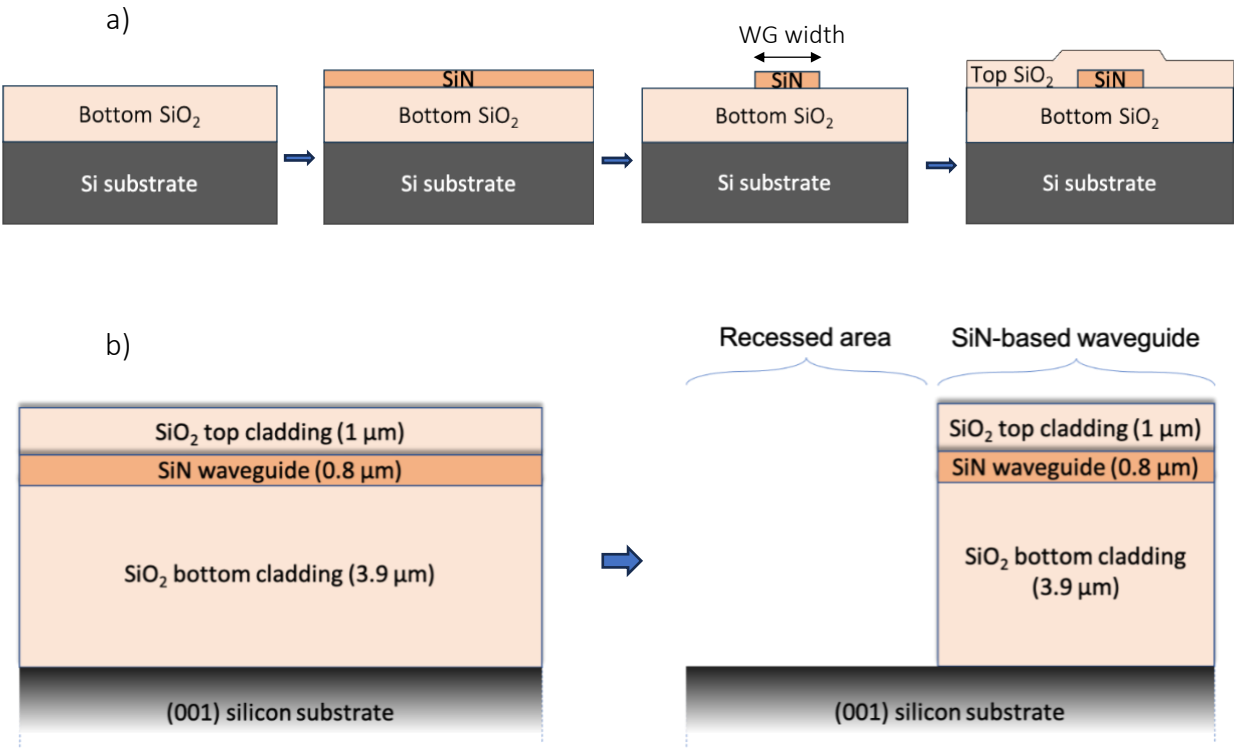


Figure 53. a) Front and b) cross section view sketch of the SiN WGs fabrication.

In order to create the areas where the laser structures will be grown, an etching was performed to reach the Si substrate (Figure 53.b). A single-step ICP dry etching, could damage the surface of the Si substrate as the F-based SiO<sub>2</sub>/SiN etching recipe is not selective. Wet etching with hydrofluoric acid (HF), on the other hand, is very selective. However, because it is

isotropic, it also etches the SiN/SiO<sub>2</sub> structure laterally. Thus, in order to avoid obtaining a concave facet and compromising the crystal quality of the Si substrate, a two-step etching process was performed. First, the pattern was etched ~95% of the way through the SiO<sub>2</sub>/SiN stack using ICP, leaving approximately 200-300 nm of SiO<sub>2</sub>. The remaining SiO<sub>2</sub> was then removed using buffered oxide etching (BOE) to preserve the Si crystal quality. This approach provided a close-to-vertical dielectric facet with an angle <10° and the preservation of the Si crystal quality. Figure 54 shows a SEM image of the WG stack.

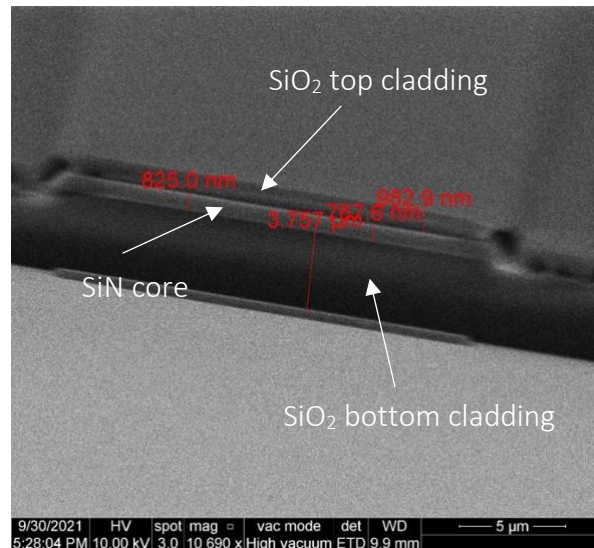


Figure 54. SEM image of the front of the WG.

The 100 mm wafers were organized into multiple dies of 20 x 20 mm<sup>2</sup>. Each die carries two series of recessed areas and s-bend waveguides (Figure 55). The dimensions of the recessed areas are 16 x 2.5 mm<sup>2</sup>. The s-bend waveguides are 5-mm long with a 300-μm offset. One of the series contains only 10 μm-wide WGs and the other contains 10, 15 and 20-μm wide WGs to investigate the influence of WG width on coupling efficiency. There are also 100-μm WGs in each series to study the coupling of broad-area lasers in pulsed operation. Laser growth and processing were done on these 20 x 20 mm<sup>2</sup> dies.

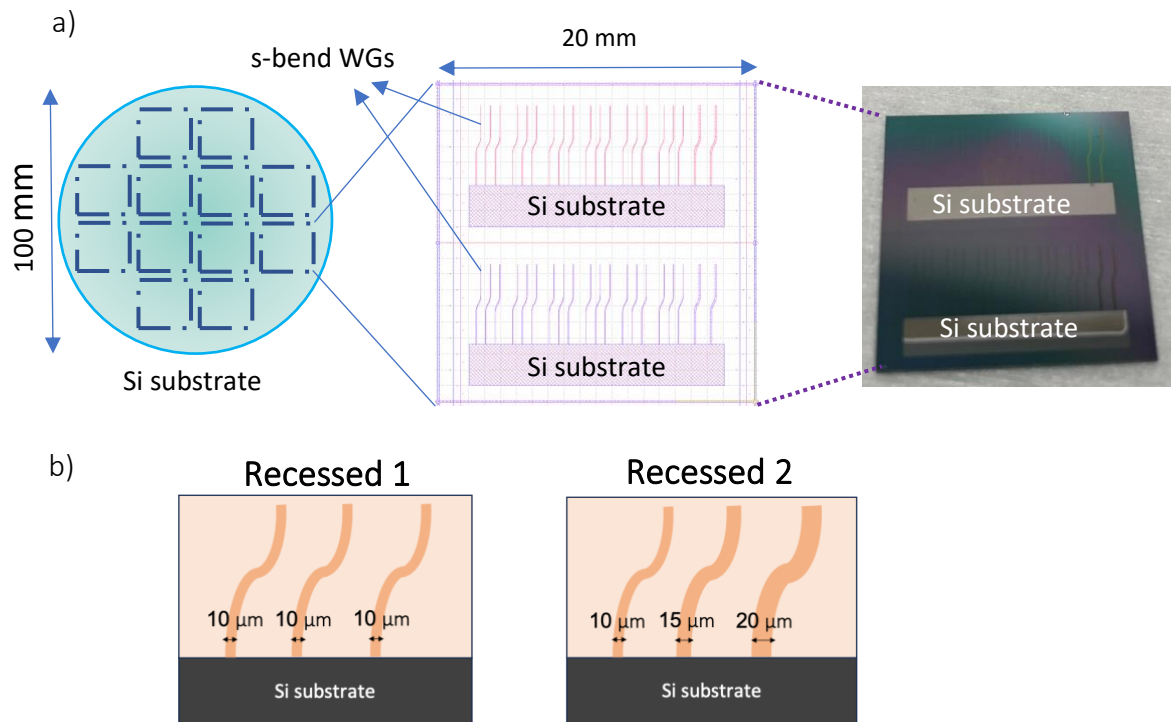


Figure 55. Schematic of the Si PICs: the pattern of the 100 mm wafers is organized with several 20x20 mm<sup>2</sup> dies, each one containing two recessed areas together with 20 SiN waveguides each one.

We received some of these 100 mm wafers from Tyndall. The next step in our lab was to prepare the sample prior to the subsequent epitaxial growth of the laser structure.

### 3.5 Oxide removal for later growth

The samples were analyzed before epitaxial growth. A SEM image of a 20-μm wide SiN waveguide and the Si substrate is shown in Figure 56. It can be seen that some material remains on the recessed area in front of the WG. This was the case for each WG in the dies. This material is a SiO<sub>2</sub> layer that was not removed by the BOE etching seen in the previous section.

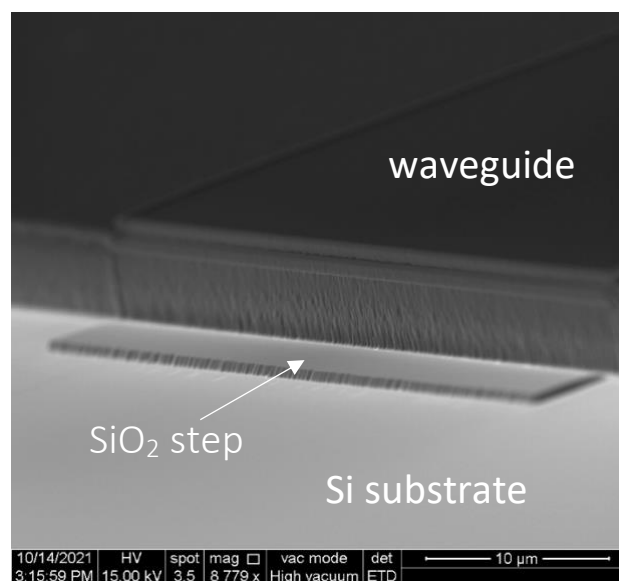


Figure 56. SEM image of the SiN waveguide with a remaining SiO<sub>2</sub> step on the Si substrate.

The reason for this is that the mask used to reach the Si substrate was designed to stop 5  $\mu\text{m}$  before the end of the waveguide (see Figure 57) in order to obtain a high-quality facet during the first step of  $\sim 95\%$  ICP etching. However, this resulted in a thicker remaining oxide of 5  $\mu\text{m}$  in length in front of the WG facet. The BOE etching intended to remove the remaining oxide was intentionally stopped when the thinner oxide layer was etched, not realizing that an oxide step was left in front of the facet (Figure 57).

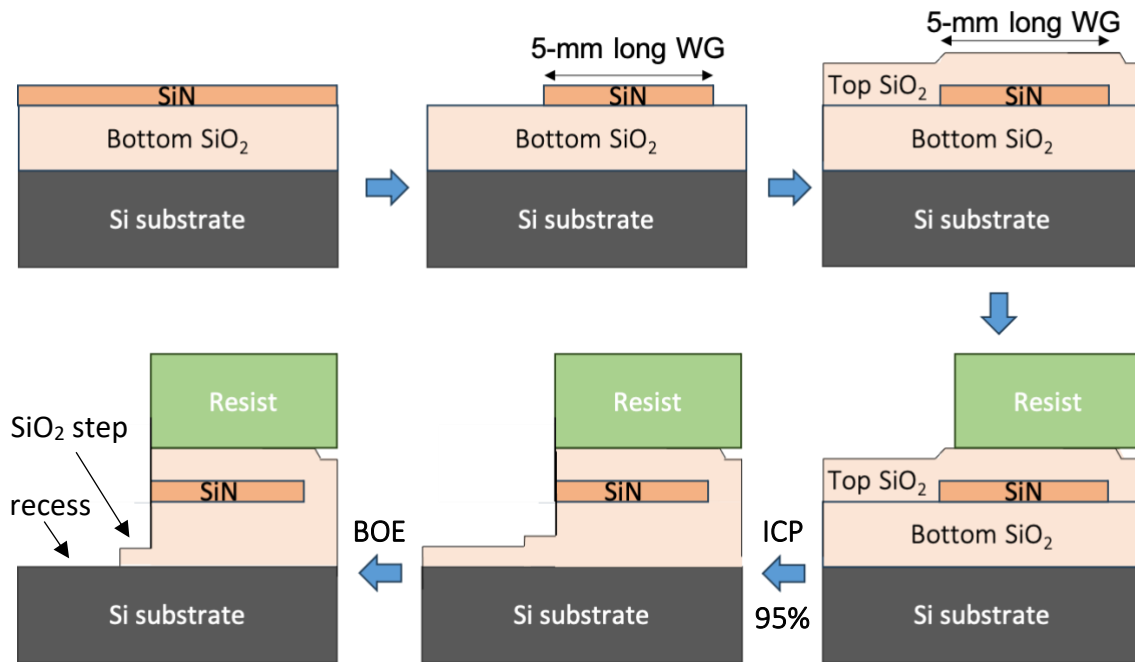


Figure 57. Cross-section view sketch of the PIC fabrication.

The  $\text{SiO}_2$  step remaining on the Si substrate will perturb the epitaxial growth close to the waveguide facet. As discussed in section 3.2, the objective is to obtain the narrowest possible gap between the DL and the WG in order to reduce coupling losses as much as possible. The III-V polycrystal deposition that will arise from this oxide step will force us to define the laser facet further away from the WG. It is therefore very important to try to remove the step without compromising the quality of the Si surface.

### 3.5.1 Wet etching

I first decided to attempt etching the  $\text{SiO}_2$  step with a HF solution that is highly selective for removing oxides. I tried HF diluted with water in this ratio: HF:H<sub>2</sub>O (1:10).

First, a standard photolithography was performed to protect the WGs. The Si substrate and the oxide step were exposed. The etch rate of the oxide with this solution was very low. Nevertheless, every 1 or 2 minutes, the sample was analyzed under the optical and SEM microscopes to verify the etching. After 18 minutes, the oxide step was completely removed. However, the Si substrate was damaged as we can observe in Figure 58.b. Figure 58.c and d show enlarged images of the WG stack where we can see that even though the WG was protected

during etching, the wet solution damaged the top cladding as well as the SiN core of the WGs. After several trials with different solution proportions, the problem persisted.

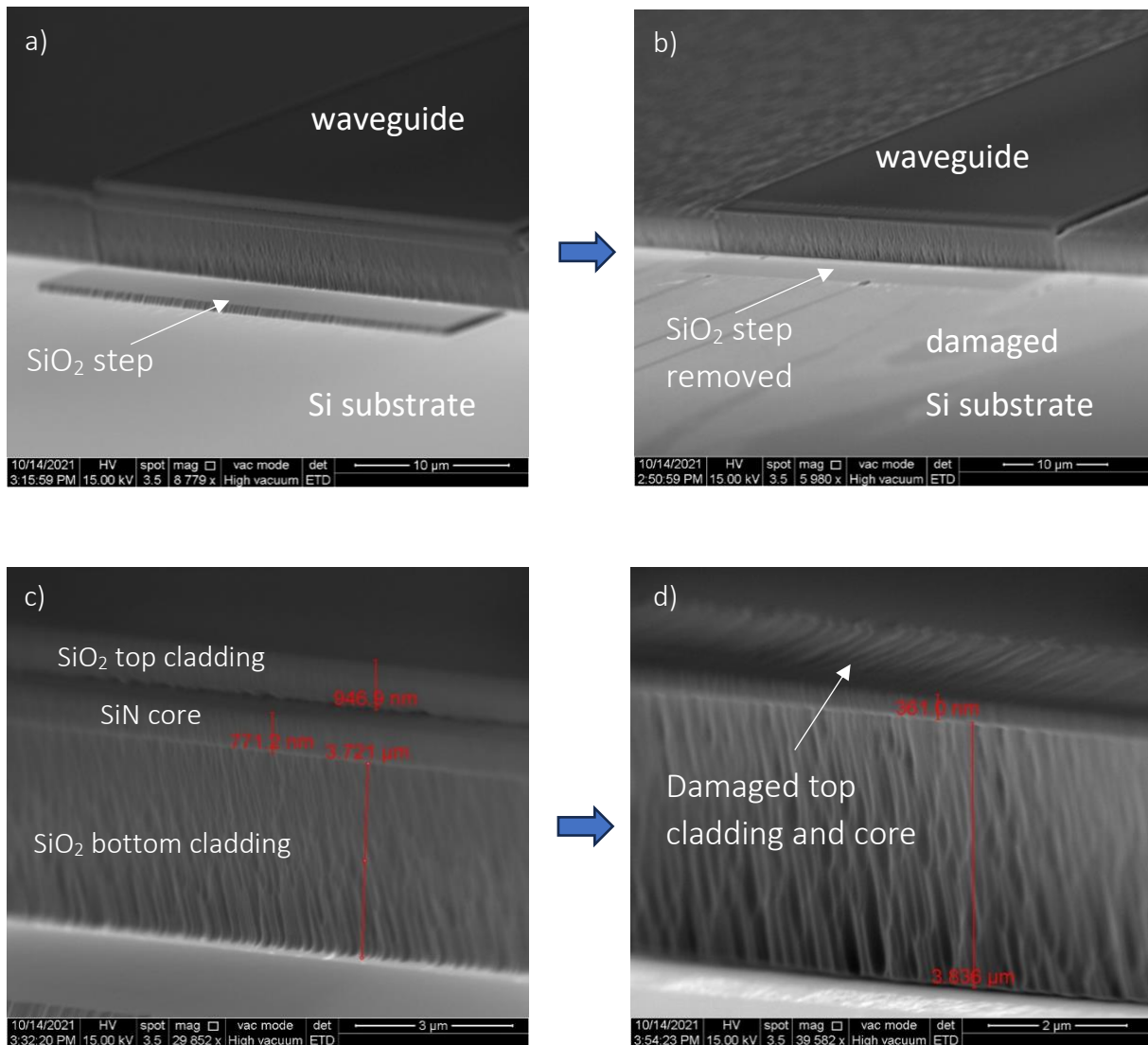


Figure 58. SEM images of the removal SiO<sub>2</sub> step attempts with HF solution. a) before etching. b) after 18 minutes etching with a damaged Si substrate. c) zoomed image on the WG stack before etching and d) after etching.

### 3.5.2 Dry etching

I then tried to remove the SiO<sub>2</sub> step with ICP dry etching. We did not have an adapted mask to expose only the SiO<sub>2</sub> step and protect the Si substrate and the WGs. I thus decided to protect the WGs and leave the oxide and Si substrate exposed using standard photolithography. Of course, the F-based recipe for oxide etching of the ICP will also etch the Si substrate as it is not selective. In fact, we assumed that a smooth and homogeneous etching would not affect the Si surface and would not affect the epitaxial growth.

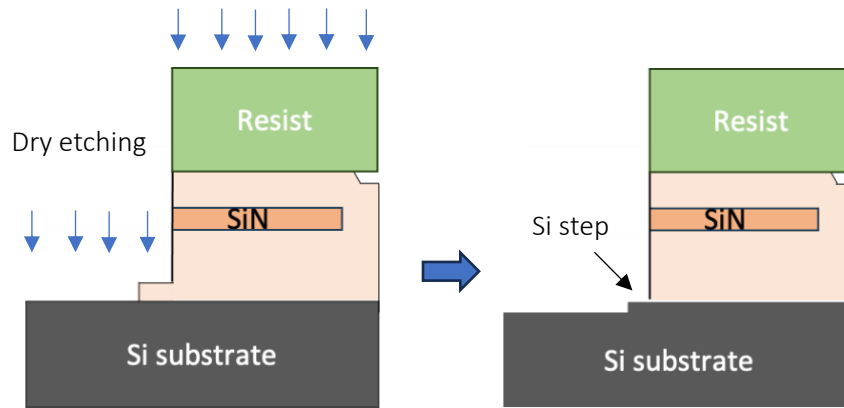


Figure 59. Process sketch of the oxide removal by ICP dry etching.

A sketch of this process trial is shown in Figure 59, where we can observe that after etching, a step of Si is formed. This step being in the Si crystal substrate, it is expected that crystalline growth will take place on top of it, unlike the previous configuration with a step of non-crystalline  $\text{SiO}_2$  material. The result is shown in Figure 60. We can observe that the oxide has been completely removed. The step in front of the waveguide is now a crystalline Si step.

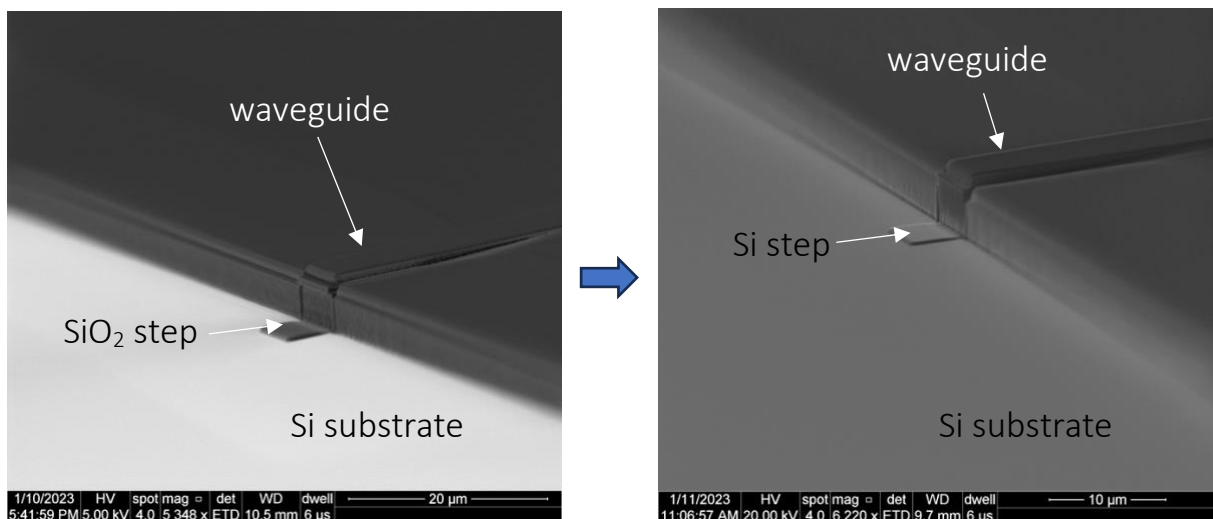


Figure 60. SEM images of the  $\text{SiO}_2$  step removal by ICP dry etching.

The next step is the epitaxial growth of the laser heterostructure. We performed the growth on samples with and without the  $\text{SiO}_2$  step.

### 3.6 Epitaxial growth

Before epitaxial growth, the sample must be free of contamination and oxidation. A cleaning process is therefore essential to achieve good quality growth. I have developed a process in which the sample is first cleaned with acetone, ethanol and isopropanol to remove any contamination. The sample is then dipped in a bath of  $\text{HF}:\text{H}_2\text{O}$  (1:10) for 45 seconds to remove any oxidation layer formed on the high-quality Si surface. The sample is then quickly transferred to the MBE chamber.



The buffer layer growth sequence and conditions were similar to those described in section 2.2 for the growth on plain Si substrates.[61] The WG stack and GaSb-on-Si templates were inspected at various stages to fine-tune the growth process and ensure an APB-free GaSb surface. The PIC integrity was maintained during this initial growth sequence. The Si PICs were then transferred to another MBE reactor to grow the entire DL heterostructure. The structure design is the same as that investigated in section 2.1.

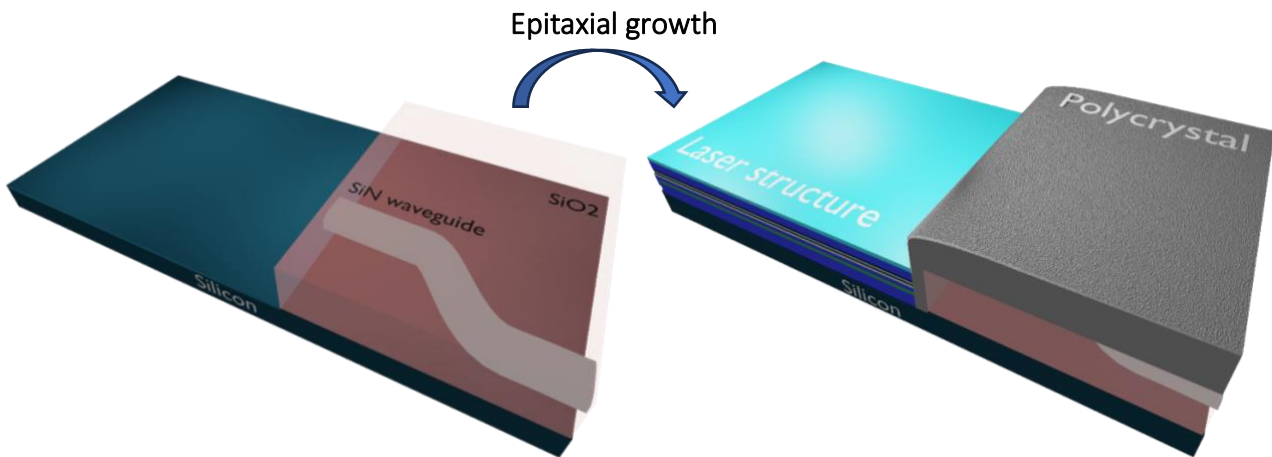


Figure 61. 3D sketch of the epitaxial growth step.

After epitaxy, the Si PIC exhibits two distinct areas (Figure 61 and Figure 62.a). On the recessed areas, the single-crystal laser structure is grown while on top of the amorphous WG stack, a  $\sim 6\text{-}\mu\text{m}$  thick III-V polycrystal material is deposited. In the case of the sample without the residual oxide step, the quality of the laser growth was poor. This is due to a disorganized Si surface after ICP etching of the oxide step. No device could be fabricated with such a sample and the idea of removing the oxide step to reduce the air gap between laser and WG was abandoned. In contrast, the sample with the oxide step exhibits a good crystal quality except in the oxide step region. The high-resolution x-ray diffraction diagram measured in the laser growth (Figure 62.b) shows well-defined diffraction features for the whole DL structure, reflecting the good growth quality. The AFM image taken on top of the laser structure confirms the absence of APBs reaching the sample surface (Figure 62.c). The roughness RMS is as low as 2.5 nm. The TDD is estimated to be in the mid- $10^7\text{ cm}^{-2}$ . All these results are very similar to those obtained on DLs grown on plain Si wafers demonstrating that the Si surface after WG fabrication is comparable to that of a planar Si substrate.



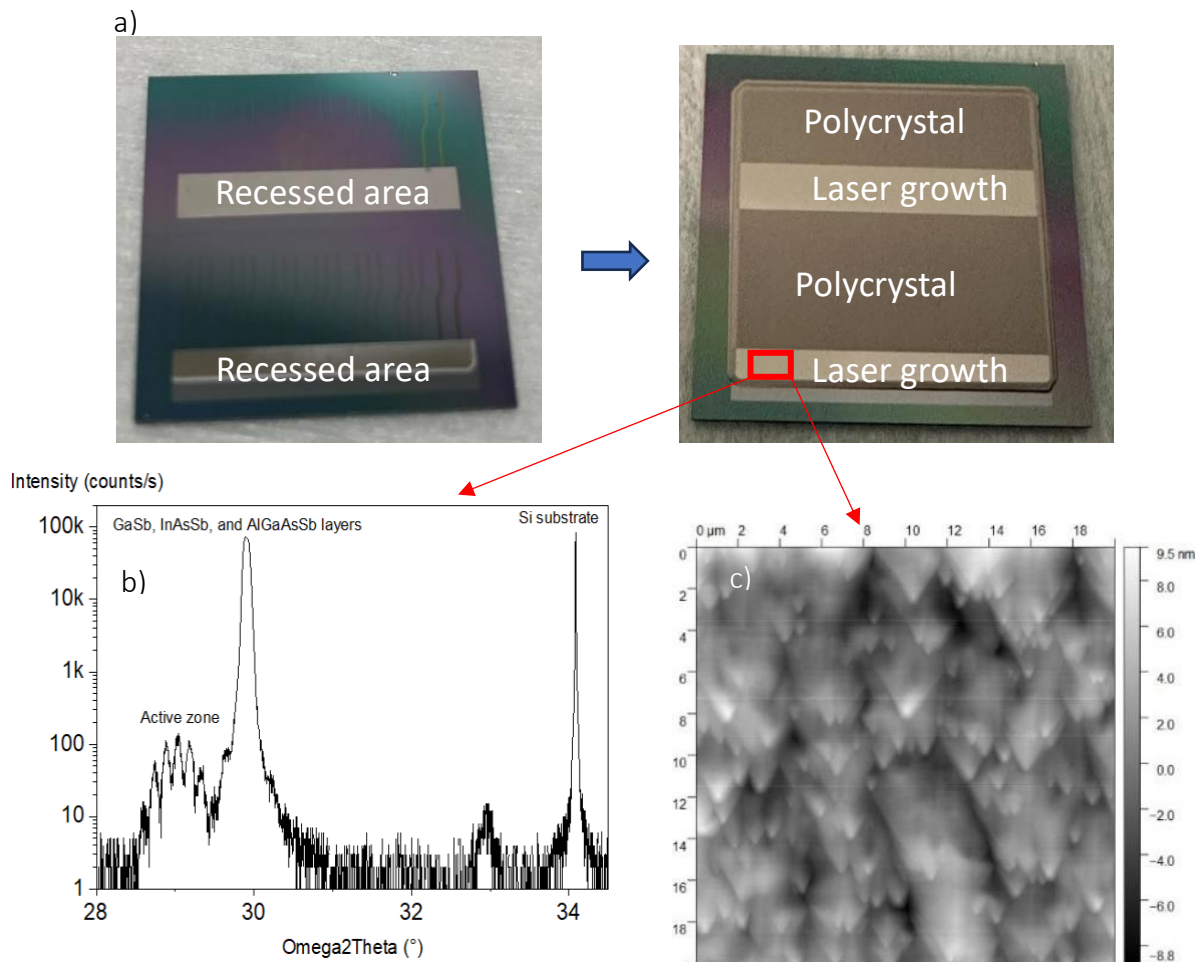


Figure 62. a) Top view of the die before and after the epitaxial growth. b) high-resolution X-ray diagram measured in the laser growth. c) AFM image taken on top of the laser structure.

Previously in our team, a cross-section image of a similar Si PIC after epitaxial growth was taken (see Figure 63). We can see that III-V polycrystal material is not only deposited on top of the WG stack but also between the WG facet and the laser crystal structure. The polycrystal laying in the III-V/dielectric interface will interfere with the light emitted by the laser that should be coupled into the WG. Removing this polycrystal will introduce an air gap between the DL and the WG. The polycrystal deposited onto the WG stack should also be removed to avoid the large height difference between the top of the polycrystal on the WG stack and the top of the laser structure. Indeed, leaving this polycrystal would compromise the good and homogeneous contact between the lithography mask and the sample for the subsequent process steps.

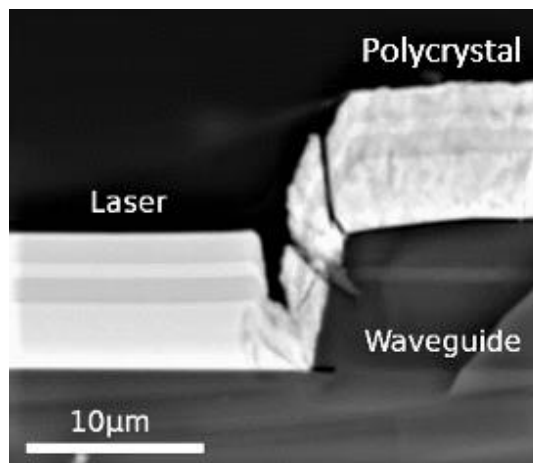


Figure 63. Cross-section SEM image of a similar Si PIC after the epitaxial growth.[120]

### 3.7 Polycrystal removal

This step involves etching away the polycrystal while preserving the WG stack and protecting the laser structure. The objective is to be able to remove the polycrystal on top of the WGs, but also the one at the laser structure/WG interface (Figure 64). This one should be removed in a very controlled and precise manner to avoid damaging the laser structure.

A wet etching solution based on citric acid ( $C_6H_8O_7$ ) and capable of removing the entire polycrystal material, had previously been developed.[100] The etching consists of first performing photolithography to protect the laser structure and then performing wet etching. The solution removes the polycrystal by lifting it off. It is very selective and does not damage the WG material. However, it can pass through the resist protection and reach the laser structure, which we call under-etch. The resist protection should therefore extend to the WG area to minimize the under-etch.

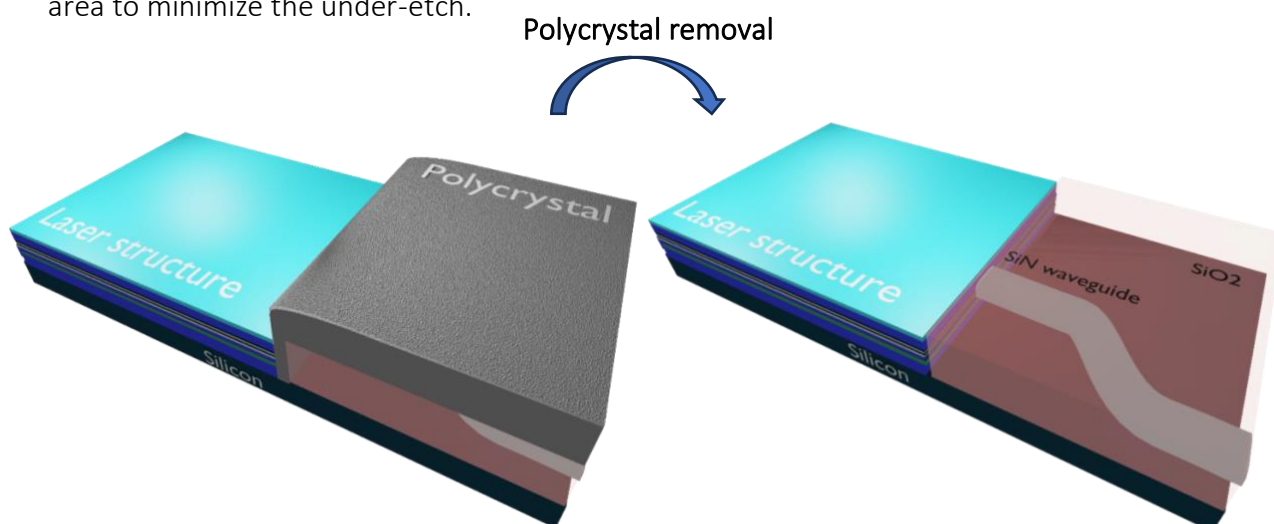


Figure 64. 3D sketch of the polycrystal removal step.

The photolithography parameters are given in Table 11. First, the resist AZ5214 is diluted with the solvent AZEBR in a ratio of 2:1. This diluted resist has a very low viscosity, which allows the gap between the laser structure and the waveguide to be filled with resist during the spin-

coating step, thus protecting the laser structure during etching. On the other hand, a low viscosity results in a lower thickness, and another layer of undiluted AZ5214 resist was spin-coated atop the diluted resist to increase the total resist thickness. The sample is then aligned with the lithography mask. Here, I will show three different alignments made to achieve the desired result. The alignments consisted of protecting the laser structure and going into the polycrystal material area for 10, 15 and 20  $\mu\text{m}$  respectively, as shown in Figure 65.

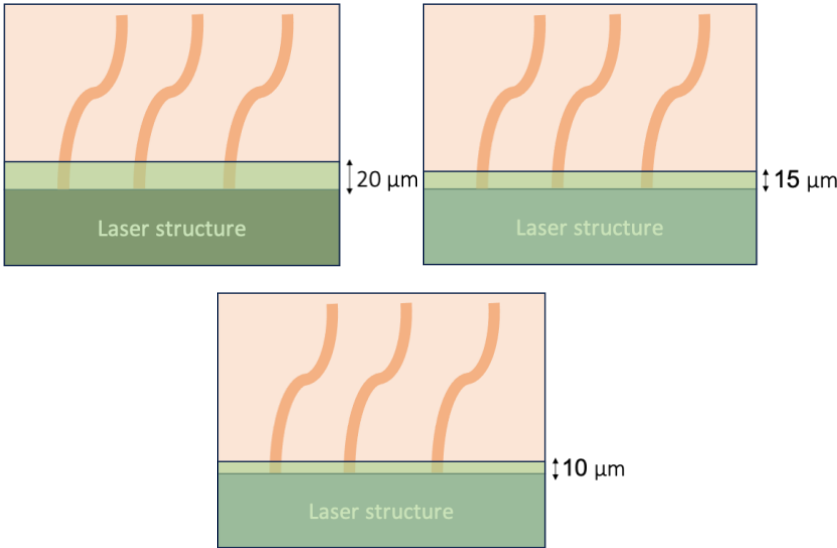


Figure 65. Different mask protections for the polycrystal removal step. The green rectangles correspond to the resist.

AZ5214:AZEBR (2:1)					AZ5214				
Spin coating			Soft bake		Spin coating			Soft bake	
v (rpm)	Ramp (s)	t (s)	T (°C)	t (min)	v (rpm)	Ramp (s)	t (s)	T (°C)	t (min)
4000	8	30	125	1	4000	2	30	125	1

Exposure		Development
Contact mode	Time (s)	Time (s)
Soft contact	40	60

Table 11. Photolithography parameters of the polycrystal removal step.

The samples were then immersed in the solution  $\text{C}_6\text{H}_8\text{O}_7 : \text{H}_2\text{O} : \text{H}_2\text{O}_2 : \text{HF}$  (1g : 1mL : 1mL : 0.001mL). After some trials, I found that 1 minute and 45 seconds was required for complete removal of the polycrystal. SEM and optical images confirm that the polycrystal was removed while the WG stack was undamaged.

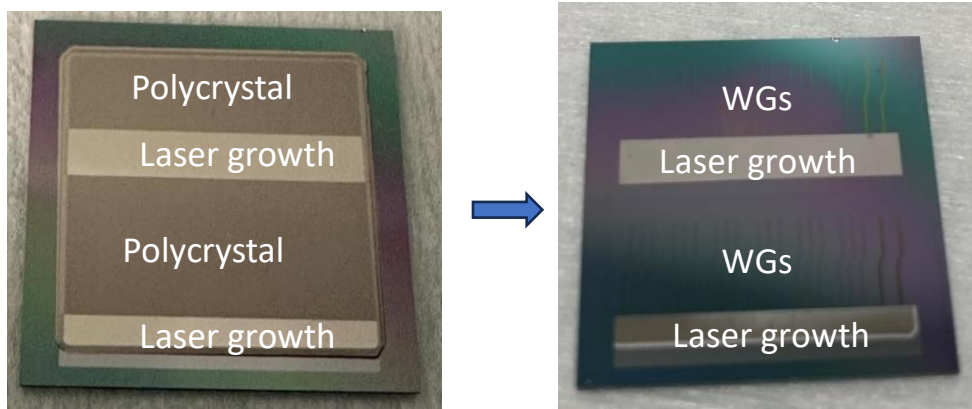


Figure 66. Pictures of a die before and after the polycrystal removal.

Figure 67 shows SEM images of three different results corresponding to the three different alignments (Figure 65). We can observe that the under-etch is different depending on the distance between the protection and the laser/polycrystal interface. In the case of a 20- $\mu\text{m}$  protection, the polycrystal was not completely removed from the WG stack (Figure 67.a). There is still 12  $\mu\text{m}$  of polycrystal left. In the case of 15- $\mu\text{m}$  protection, the polycrystal has been completely removed from the WG stack and from the WG/laser structure interface (Figure 67.b). However, we can observe a poor-quality laser growth in front of the passive waveguide, which is a consequence of the oxide step (see section 3.5). Therefore, to ensure a high-quality facet, the laser facet should be defined at least 10-11  $\mu\text{m}$  away from the waveguide facet. In the case of a 10- $\mu\text{m}$  protection, the under-etch is more pronounced and the laser structure was etched away leaving a gap as large as  $\sim 10 \mu\text{m}$  (Figure 67.c). In addition, the wet etching resulted in a very isotropic laser structure flank, leaving us no choice but to define the laser facet further away if we were to use this sample. I decided to continue with the laser process using the sample with 15- $\mu\text{m}$  protection in which, among the three results, the narrower gap could be achieved (Figure 67.b).

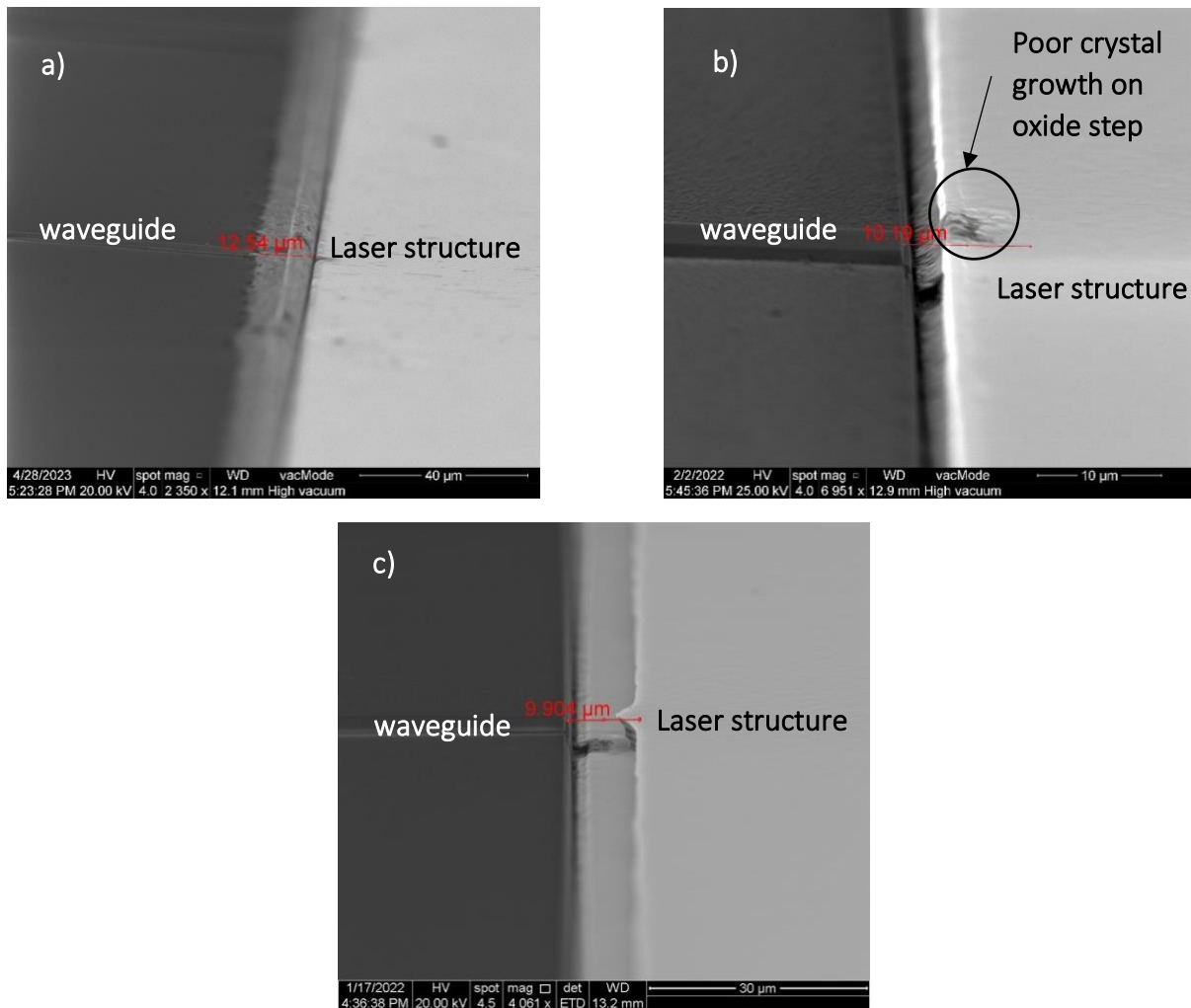


Figure 67. SEM images of the sample after the polycrystal removal for different masks. a) The protection goes 20 μm into the WG stack, b) 15 μm and c) 10 μm.

### 3.8 Laser process on the Si PIC

The next step is the laser process. Here, the process investigated in section 3.3.2 is implemented and adapted to take into account the PIC architecture. Throughout the process, the WG stack should be protected. The masks were thus designed with a WG stack protection for each step of the laser process. The protection mask extends 2 μm or more from the laser/waveguide interface, depending on the process step, to ensure a complete protection of the WG facet. In the laser growth area, similar designs to those used in section 3.3.2 were used for the laser process. This process requires precise and careful lithography alignments to ensure the success of each step while protecting the WG stack and achieving the smallest possible air gap. For the laser facet definition, different masks were designed with different gaps between the laser and the WG, giving us the flexibility to choose the best distance depending on the polycrystal removal result (see Figure 67). The cavity length is designed to be 1.5-mm long and the ridge is 10-μm wide for all lasers.

### 3.8.1 Facet definition

The first step in the laser process is the laser facet etching. The parameters for the deposition of the SiN hard mask are the same as those used in section 3.3.2.1. For the lithography step, a previous test was done on the sample from Figure 67.c using the same parameters as in section 3.3.2.1. The SEM image shows that the resist is much thinner at the edge of the WG than on the flat regions (Figure 68), which could compromise the protection of the WG facets during etching.

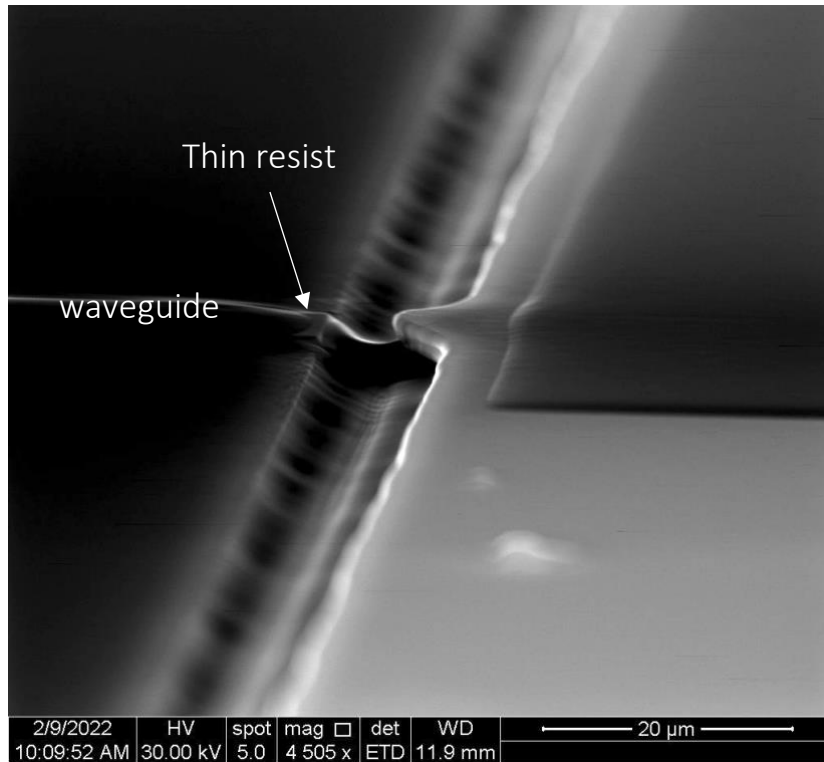


Figure 68. Facet definition photolithography using the same parameters as those of discrete etched-facet lasers.

I decided to increase the thickness of the resist by decreasing the spin-coating rotation speed. We then aligned the sample with the lithography mask. For this sample, the facet was defined at a distance of  $\sim 11 \mu\text{m}$  from the WG facet, avoiding defining the facet close to the poor crystal growth arising from the oxide step (previous section). The new lithography parameters are listed in Table 12.

Spin-coating				Soft bake		Exposure	
Resist	v (rpm)	Ramp (s)	t (s)	T (°C)	t (min)	Contact mode	t (s)
AZ1518	3000	8	30	110	1	Vacuum contact	45

Development		Hard bake
t (s)	T (°C)	t (min)
40	110	4

Table 12. Lithography parameters for the facet definition on a Si PIC.

The hard mask opening was then performed followed by the resist removal. SEM images and profilometer measurements confirm the protection of the WG facet. Figure 69.a shows a top view image of the hard mask opening. Note that the gap achieved here is  $\sim 11 \mu\text{m}$  for this sample. We expect that the gap could easily be reduced to close to  $\sim 3 \mu\text{m}$  if the oxide step problem is solved.

Finally, the facet etching was performed the same way as for discrete etched-facet lasers (section 3.3.2.1). The remaining SiN mask was removed by ICP. SEM images confirmed that the WG stack was not damaged during this step. The facet etching is similar to that of discrete etched-facet DLs. However, due to the more complex architecture of the Si PIC, the contact between the resist on the laser structure and the lithography mask is not as good as on a simple Si substrate. As a consequence, the facet angle is slightly higher ( $\sim 92.5^\circ$ ) as we can observe in Figure 69.b.

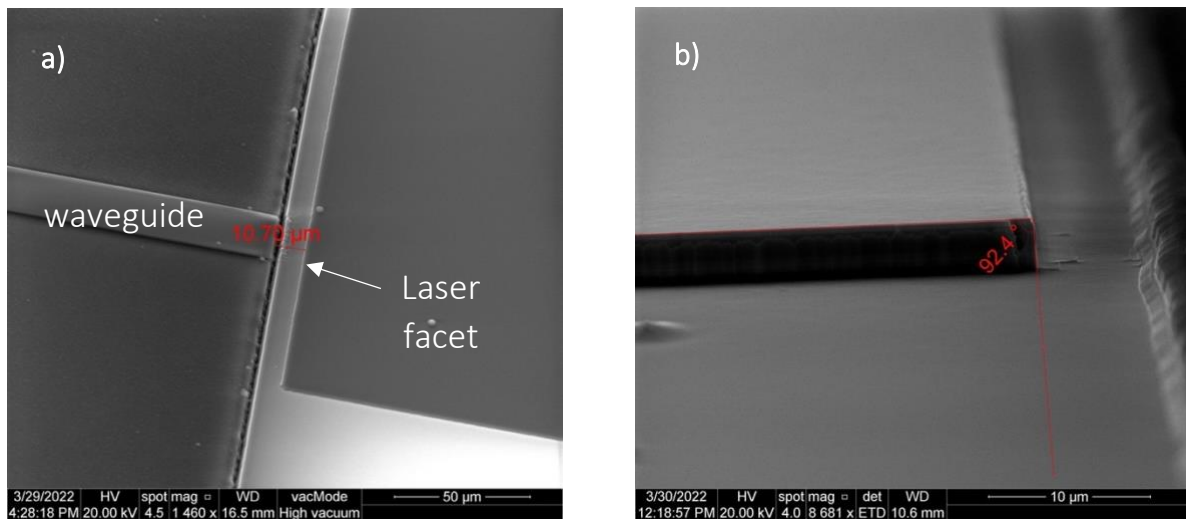


Figure 69. SEM images of the laser facet definition. a) Top view of the sample after hard mask opening. b) Facet angle measurement after facet etching.

### 3.8.2 Ridge definition

The next step is the laser ridge definition. We used the same lithography and ICP etching parameters as those presented in section 3.3.2.2. The SEM image in Figure 70.b shows an accurate alignment of the laser ridge with the waveguide.



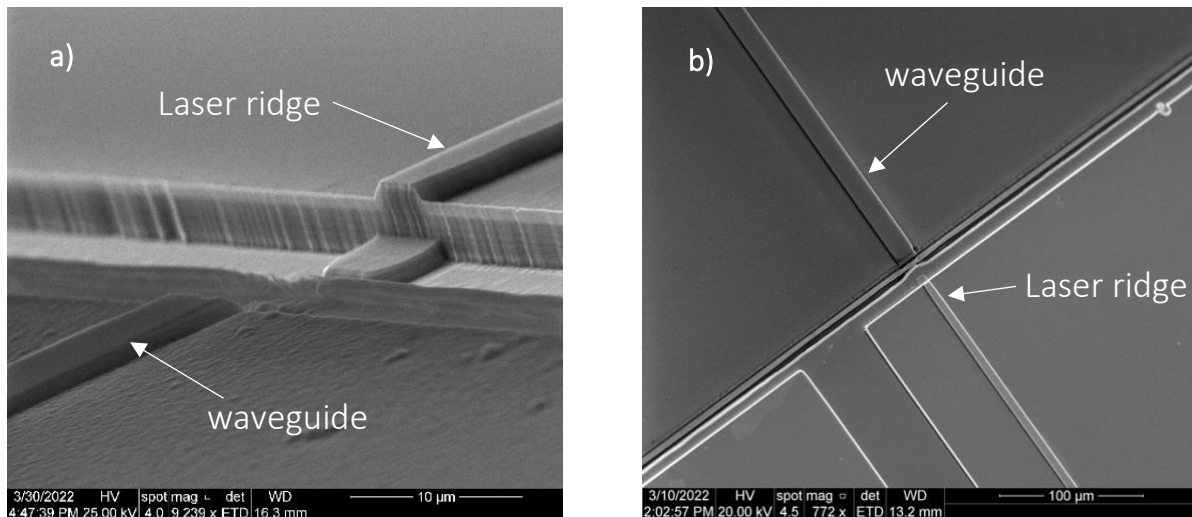


Figure 70. SEM images of the ridge definition step. a) angled view. b) top view.

### 3.8.3 Bottom contact definition

We then etched down to the InAsSb layer for the bottom contact. The mask was designed to protect everything except the bottom contact openings next to the laser ridges (Figure 71). We used the same lithography parameters as in section 2.3.2. These parameters result in a thick resist ( $\sim 2.6 \mu\text{m}$ ). The WG stack and laser were therefore well protected and there were no specific parameters to adjust. The openings of the bottom contact were large enough to be able to point the laser tracking to control the etching. The etching was stopped in the middle of the InAsSb layer.

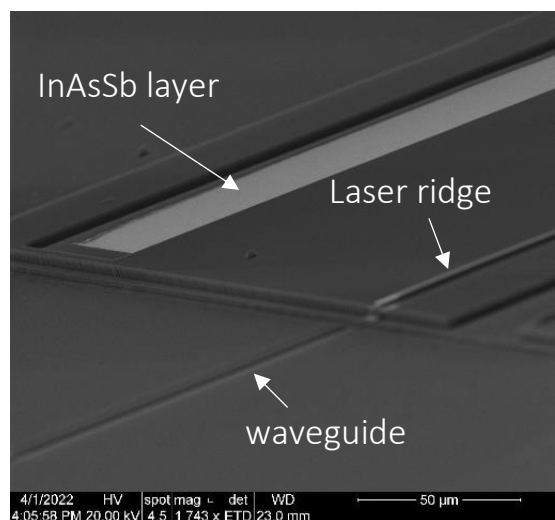


Figure 71. SEM image of the bottom contact next to the laser ridge.

### 3.8.4 Insulation and opening

Electrical insulation was then performed. SiN deposition, lithography and SiN opening were carried out using the same parameters as in section 3.3.2.3. Here, as the SiN is deposited over the entire sample, the SiN opening mask was designed to leave the WGs unprotected in order to remove the SiN insulation layer from the WG stack. In the laser area, everything is



protected except the SiN openings at the top of the laser ridge and bottom contact, and the laser facet. Figure 72 shows some images of the device after this step. The SiN material has been successfully removed from the laser ridge, bottom contact and facet. Other SEM images confirm that the WGs were not damaged after ICP etching.

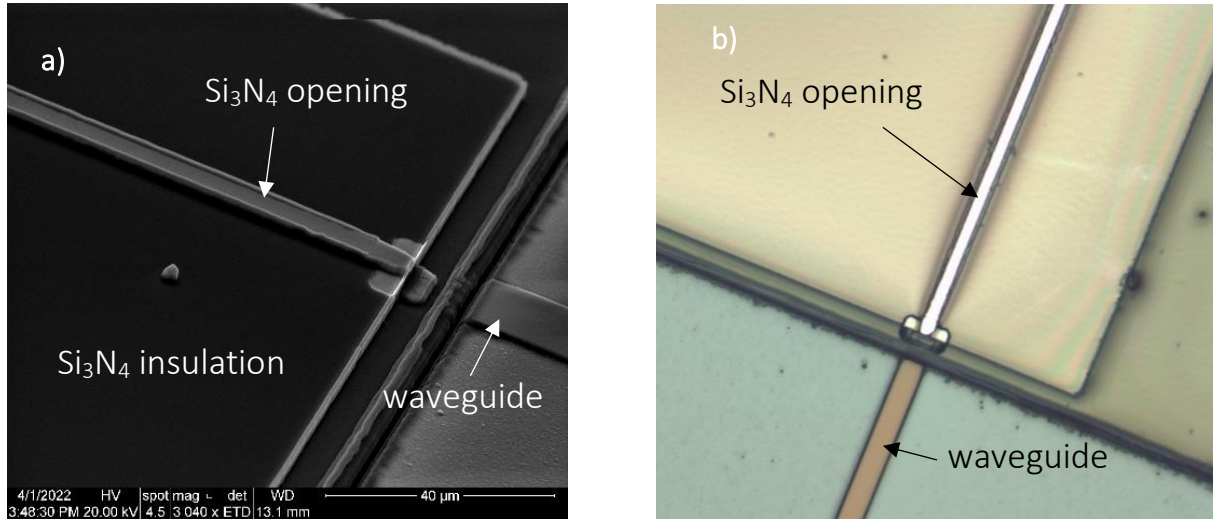


Figure 72. a) SEM and b) optical image of the electrical insulation step.

### 3.8.5 Metallization

The final technological step is the metal deposition. Photolithography and e-beam metal deposition were performed with the same parameters as those used in section 3.3.2.4. The mask was designed so that the metal is deposited on the top of the ridge and the bottom contact, while lifting the metal in the other regions, provided that lift-off is possible in the large region on top of the WG stack. As we can observe in Figure 73, the lift-off was successful. The metal was well deposited on the top of the ridge and on the bottom contact, while it is lifted from the other regions, including the WG stack.

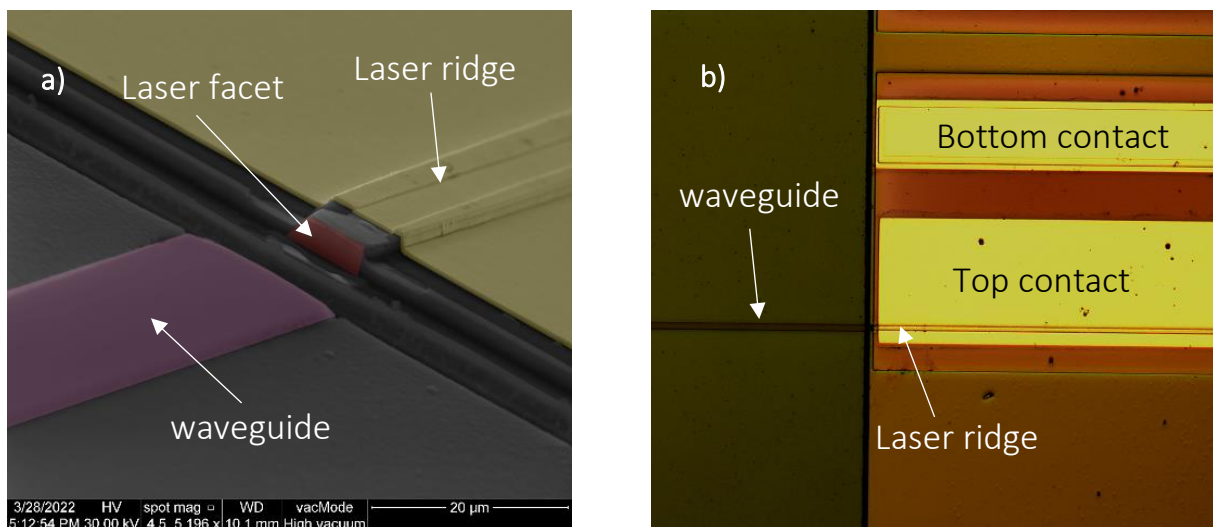


Figure 73. a) SEM and b) optical images of the device after the metallization step.

A sketch of the entire laser process flow is shown in Figure 74.

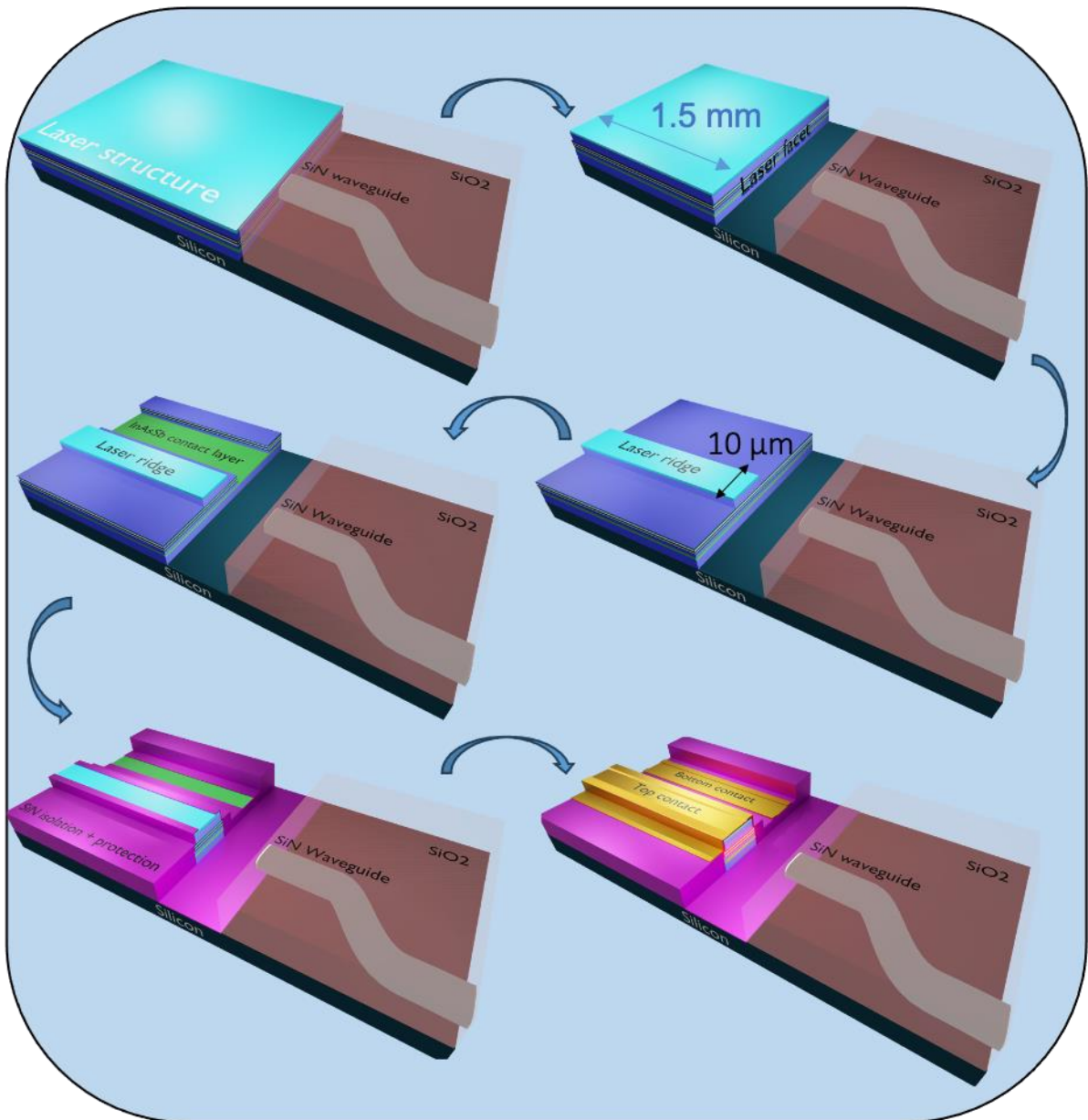


Figure 74. Sketch of the laser process flow on the Si PIC. The different process steps are facet etching, laser ridge, bottom contact, electrical insulation and metallization.

### 3.8.6 Substrate thin-down and cleavage

The final step before characterization is substrate polishing and cleavage. An image of the final die is shown in Figure 75.a. The sample was thinned down from  $\sim 700 \mu\text{m}$  to  $\sim 200 \mu\text{m}$ . If the sample is thicker than  $200 \mu\text{m}$ , cleaving is very difficult. Conversely, if the sample is too thin ( $< \sim 200 \mu\text{m}$ ), it bends due to the highly strained SiO<sub>2</sub>/SiN/SiO<sub>2</sub>-on-Si stack. After polishing, cleavage was performed in four different parts of the sample as shown in Figure 75.b. Two cleavages were performed as close as possible to the back etched-facet of the lasers. The other two were made in the waveguide region to obtain a cleaved output of the waveguide. The bars were then soldered onto a Cu heat sink and measured on a probe station.

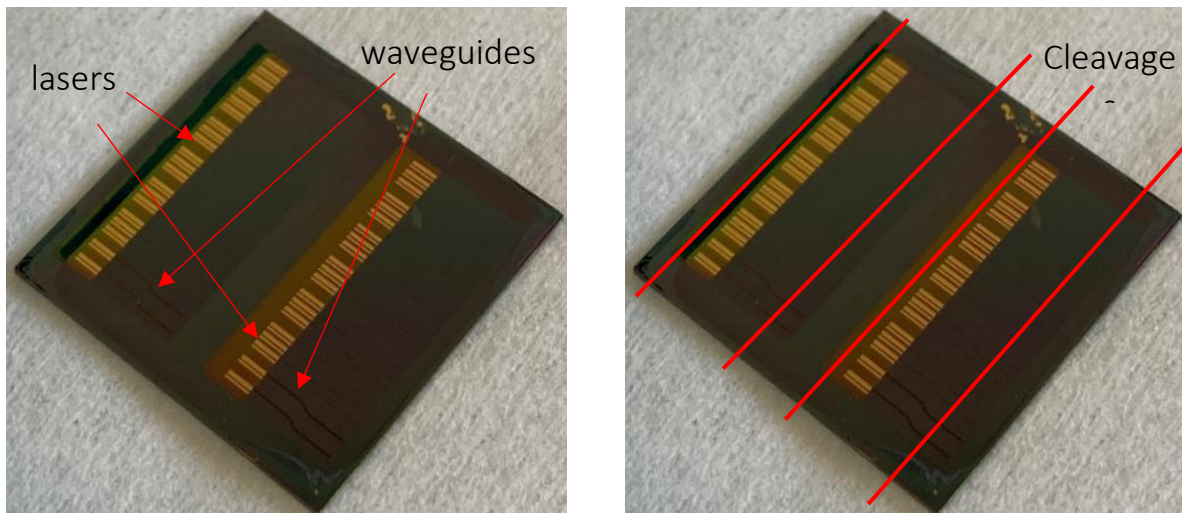


Figure 75. Images of the final die showing a) the two series of lasers and waveguides and b) the cleavages performed after polishing.

### 3.9 Characterizations of DLs on the recessed Si

First, the DLs integrated on the Si PIC are characterized and their performance is benchmarked against similar DLs grown on planar Si wafers. The L-I-V measurements are performed by measuring the output power emitted from the back etched-facet of the laser using a calibrated powermeter as shown in Figure 76. The measurements are done in CW operation at RT for all lasers, and for a representative DL, the measurements were also taken at different temperatures.

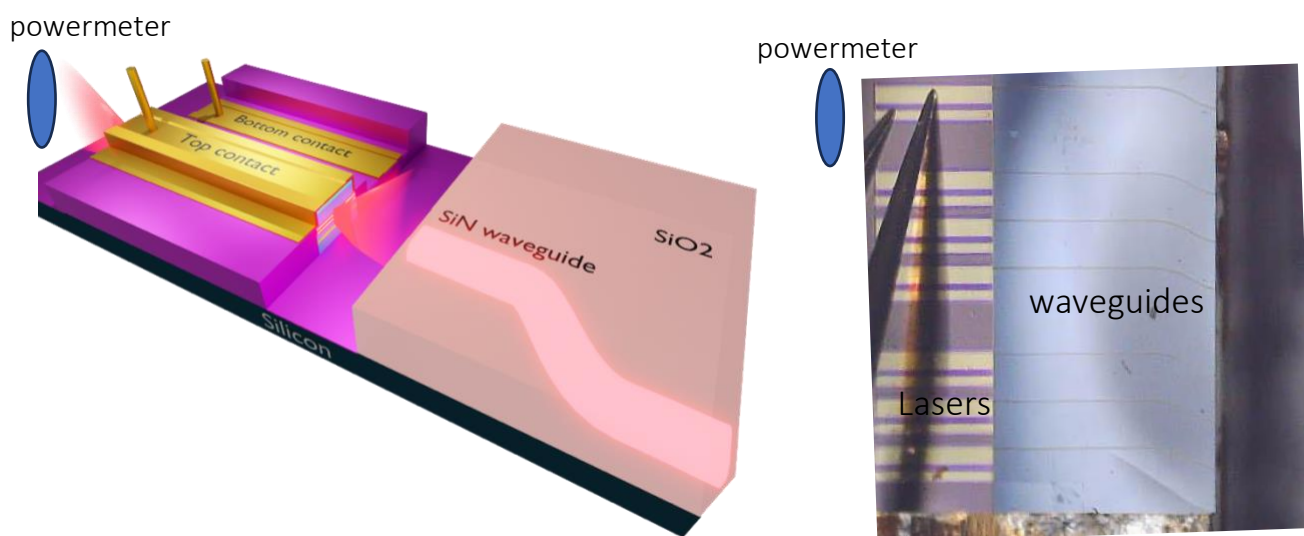


Figure 76. a) 3D sketch of the final device and DL characterizations. b) Top view image of the bar mounted on a Cu heat sink and measured on a probe station.

Figure 77.a shows the L-I-V curves taken in the CW regime at RT from 8 DLs of the laser bar. All DLs did lase. The turn-on voltage is slightly higher than 1 V and the series resistance is around 3  $\Omega$  for all DLs. These results are similar to those achieved with discrete DLs of similar design grown on GaSb[137], [138] and on Si substrates.[62], [88] The threshold current  $I_{th}$

varies from 135 to 150 mA and the output power at 400 mA current varies between 7 and 10 mW, depending on the DL. The values spread from one laser to the other is within the typical variation range of our laser process for discrete DLs on Si. The L-I-V curves taken at different temperatures for a representative DL are plotted in Figure 77.b. The threshold current varies between 163 and 283 mA for measurement temperatures ranging from 20°C to 80°C, limited by the experimental setup. From this series of measurements, we can extract the corresponding characteristic temperatures  $T_0$  and  $T_1$ , which represent the sensitivity to the temperature of the threshold current and of the external quantum efficiency, respectively (see section 2.4). The values are 110 K for  $T_0$  and 81 K for  $T_1$ , which again are typical values for discrete GaSb DLs.[139]

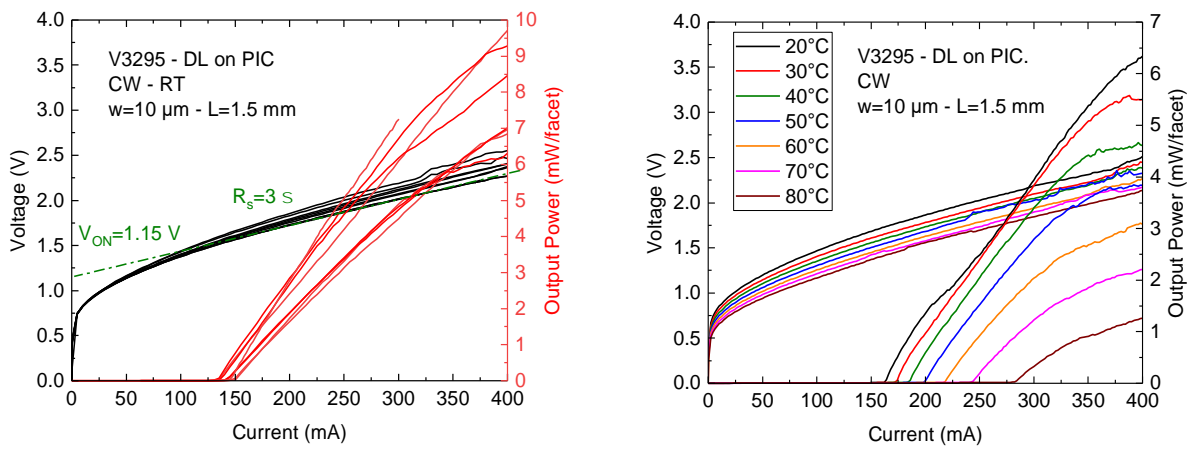


Figure 77. a) L-I-V curves of the DLs on the Si PIC taken in the CW regime at RT for a series of 8 DLs. b) L-I-V curves taken at different temperatures between 20 and 80 C (setup limited) for a typical DL.

The emission spectrum recorded from a DL in CW operation and RT is shown in Figure 78. The emission wavelength is near 2.3  $\mu$ m, as expected from the heterostructure design.

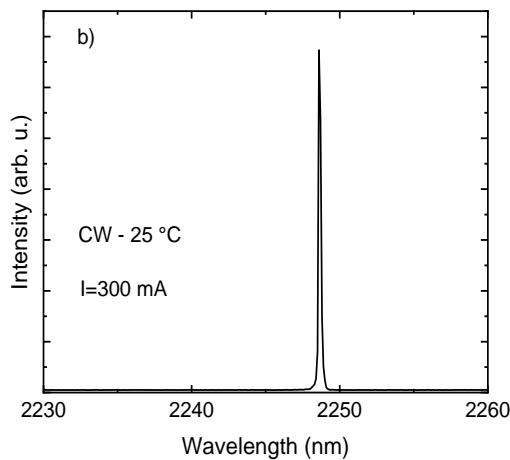


Figure 78. Emission spectrum recorded from the DL at RT in the CW regime at  $\sim 2 \times I_{th}$  drive current.



The performance of the DLs epitaxially integrated on the Si PIC is therefore similar to that of discrete DLs on planar Si substrates. We can then conclude that despite the complex PIC architecture and integration process, a number of steps can be validated. First, we were able to fabricate the Si PIC while maintaining the quality of the Si surface for subsequent epitaxial growth. The same procedures typically used for the epitaxial growth of discrete DLs on plain Si substrates were used to achieve a high-quality growth on the PIC trench. The polycrystal removal and laser process were successfully adapted to the particular sample architecture, in spite of its complex geometry. A recent comparison of epitaxial and heterogeneously integrated discrete GaSb-based lasers has revealed better performance of epitaxial lasers in terms of threshold current and temperature stability.[88] Since the performance of lasers fabricated here on a Si PIC is similar to that of discrete lasers on Si, we expect a superior performance also for lasers integrated on a Si PIC.

### 3.10 Light coupling measurement

The next and final step is to evaluate whether the light emitted by the laser is coupled into the SiN waveguides.

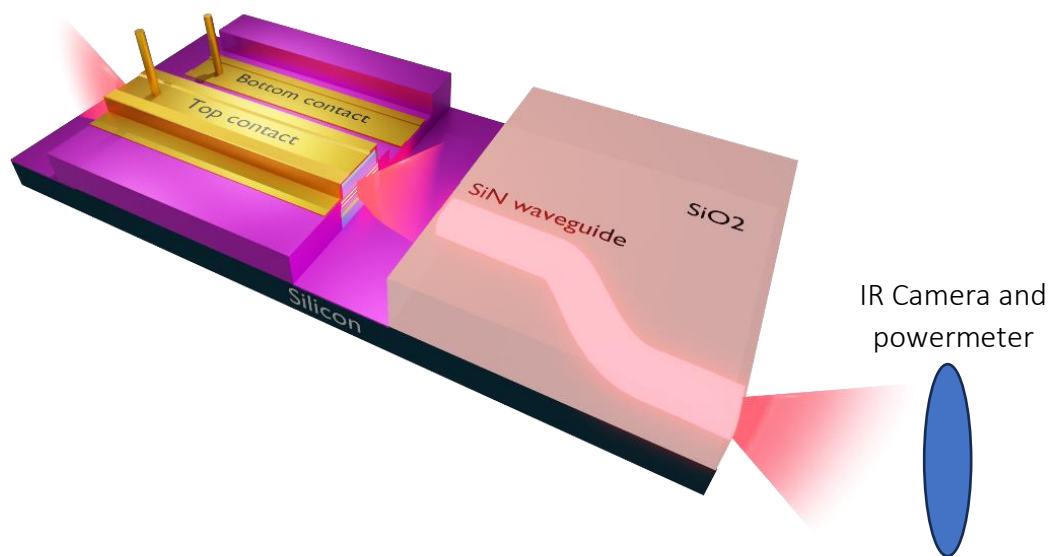


Figure 79. 3D sketch of the light coupling characterizations.

First, an IR camera was used to capture the light that could be coupled, guided and coming out from the waveguide output facet. The camera was first placed far away to capture the whole set up. Figure 80 shows two IR images of the whole setup at zero current and 250 mA (above threshold). Three white spots can be seen when the laser is operating at 250 mA (Figure 80.b). The top spot corresponds to the light output from the back etched-facet of the DL. The middle spot corresponds to the light output from the other end of the laser before it is coupled into the waveguide. Finally, the last spot is the light that is coupled into the WG and emerges from the WG facet.

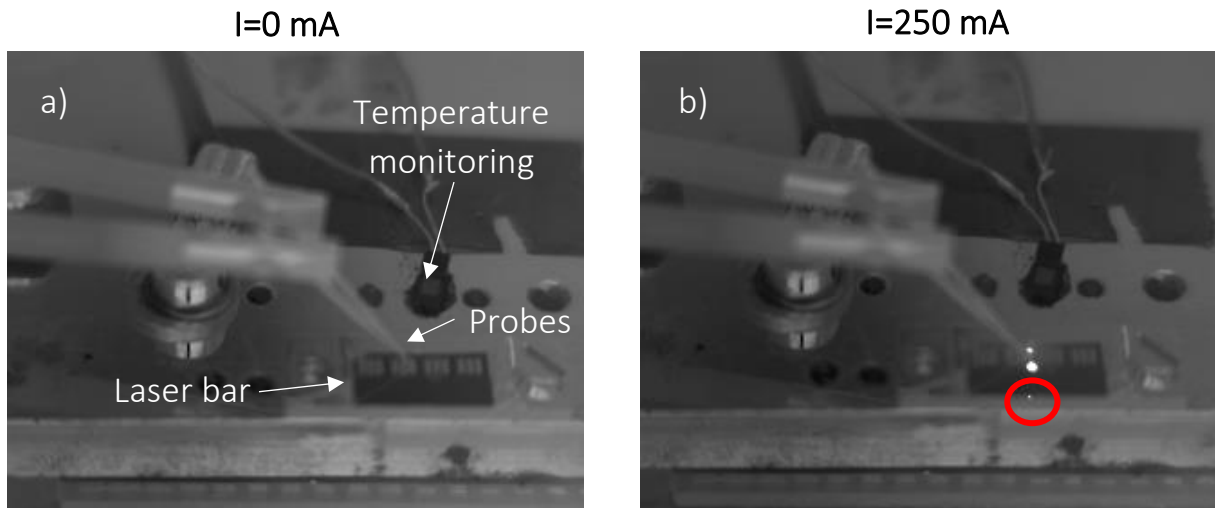


Figure 80. IR image of the laser bar on the probe station with a) zero drive current and b) 250-mA drive current.

The camera was then placed closer to the laser bar and at the output of the waveguide. Two different images taken from different angles are shown in Figure 81. Figure 81.a shows a front-view IR image where we can observe two light spots: the light arising from the cone of the laser facet and reaching the camera (large spot), and the coupled and guided light spot (narrow spot). Figure 81.b shows an IR image taken with an angle in order to avoid the light from the laser facet hitting the camera. This image shows a clearer coupled and guided spot at the output of the waveguide.

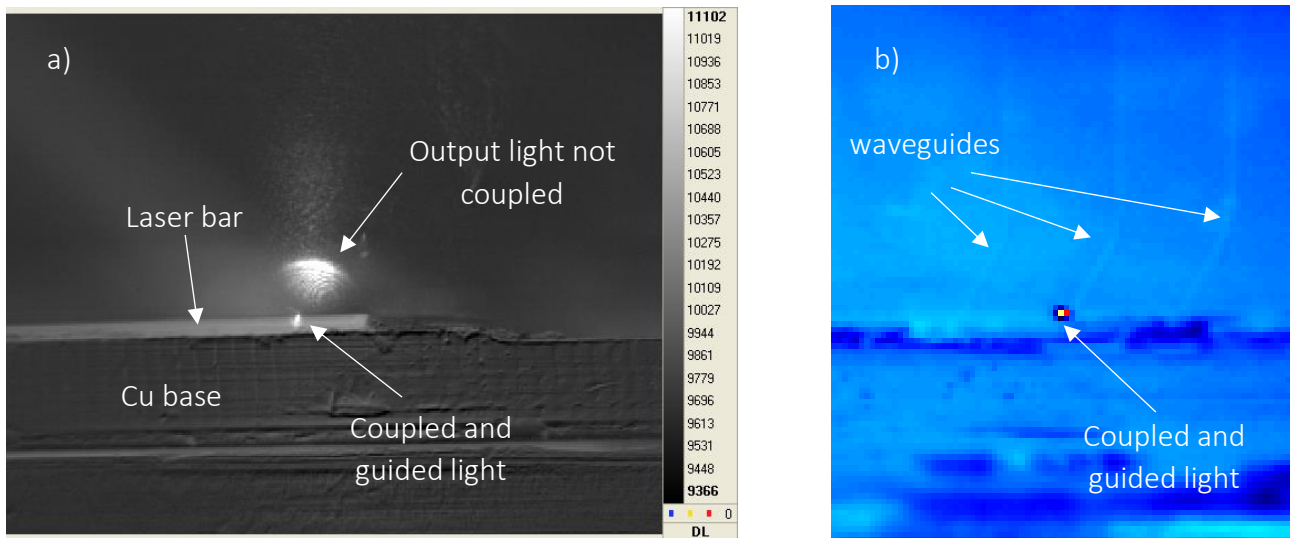


Figure 81. IR images at the output of the waveguide with the laser operating at 250 mA. a) front view. b) angled view.

Finally, in order to perform power measurements, the light arising from the laser facet that is not coupled into the waveguide should be blocked so that only the coupled light is collected. A Cu mechanical shield was used to block this light. As the powermeter would be placed at the output of the waveguide, we took further IR images with the camera placed in the same position to check if the direct light was correctly blocked. The IR image in Figure 82.b

shows that the light cone emitted by the laser facet is now blocked. We could then proceed with the power measurements.

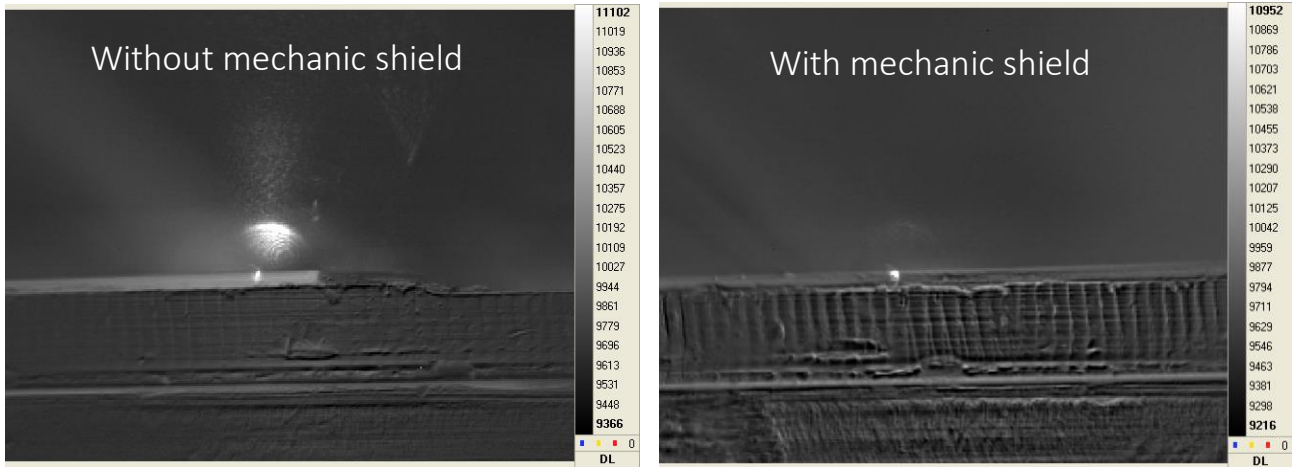


Figure 82. IR images at the output of the waveguide with the laser operating at 250 mA. a) without the mechanic shield. b) with the mechanic shield.

The final set of investigations consisted of measuring the WG output power as a function of the DL drive current. It was then compared to the optical power emitted from the back-facet of the DL (direct emitted light) to derive the light coupling efficiency. The setup measures the coupled light power at the output of the WG whereas the laser output power is measured at the back facet of the laser. The L-I curves of a representative DL-WG pair, where both the laser ridge and the waveguide are 10- $\mu\text{m}$  wide, were recorded in CW operation at RT (Figure 83). The black curve represents the output power emitted by the DL whereas the blue curve was measured at the output of the WG facing the same DL. Both curves exhibit a threshold current of 135 mA. The threshold does not seem to be affected by any reflection of light from the dielectric stack towards the DL facet. The optical power at 400 mA drive current from the back facet of the laser has a value of 12.7 mW, while that from the WG output is 1.2 mW, giving a minimum value of about 10% of coupling efficiency. This value was found for the majority of the DL/WG pairs. The propagation losses in the SiN waveguides are very low at this wavelength ( $\sim 0.1\text{-}2.5$  dB/cm), [140], [141] so we assume that the optical losses are mainly insertion losses. Since the coupling efficiency is 10%, the insertion losses are estimated to be 10 dB.

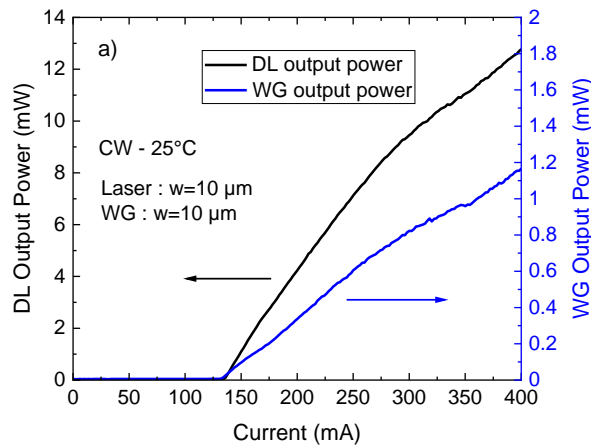


Figure 83. L-I curves of a DL-WG pair where both laser ridge and WG are 10  $\mu\text{m}$  wide, taken in the CW regime at RT.

### 3.11 Simulations

To understand the critical aspects of light coupling in this configuration, as well as the experimental coupling efficiency value, we have performed 3D finite-difference time-domain (FDTD) simulations. The calculations have been carried out by Michele Paparella.[70] FDTD solves Maxwell's equations in the spatial and time domains.[142] The monitor is settled in the passive core collecting the light coupled in the waveguide, as shown in the inset of Figure 85. The refractive index of the gain section of the DL is set to 3.695 for the active zone and 3.27 for the top and bottom claddings.[70] The optical modes are calculated for a wavelength of 2.3  $\mu\text{m}$ , and the WG and DL ridge widths are chosen to be 10  $\mu\text{m}$ . Preliminary simulations were carried out to study the overlap between the optical mode in the DL ridge and that in a SiN WG, which was found to be  $\sim 86\%$ . The 2D TE profiles of the supported mode in the ridge and in the SiN WG are shown in Figure 84.

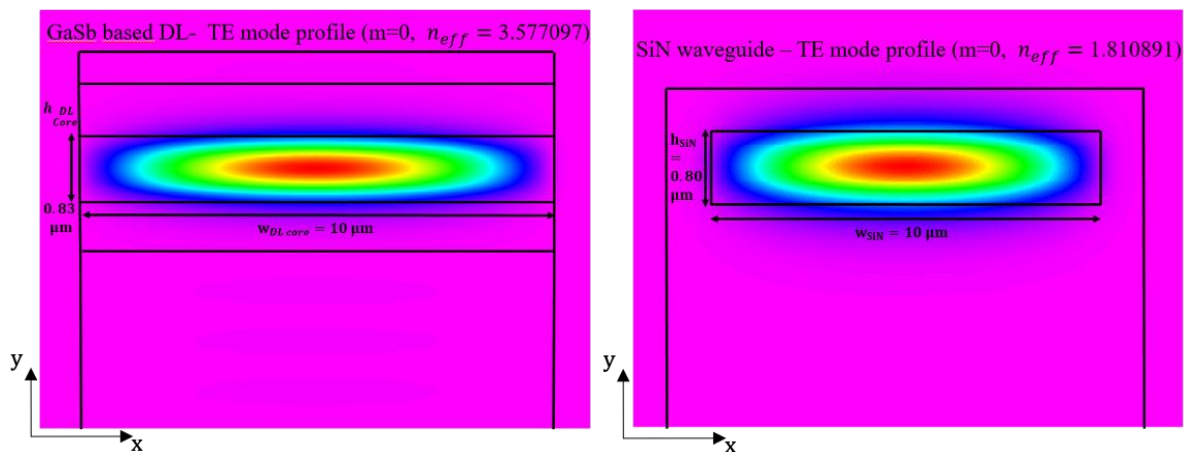


Figure 84. 2D TE mode profiles supported in the DL ridge and in the SiN WG.[70]

Figure 85 shows the simulated transmittance as a function of the air gap for different passive core materials whose refractive indices are listed in Table 13. The transmittance in our system is defined as the ratio of the power collected by the monitor located in the WG core to



the output power of the DL. In the absence of a gap, the transmittance is as high as ~90% due to the low refractive index contrast between the DL and the WG core. However, when an air gap is introduced, a high refractive index contrast appears (DL-air), resulting in a high divergence of the laser beam, and the coupling drastically decreases. Above approximately 2-2.5  $\mu\text{m}$ , the transmittance remains relatively constant at around 20% in the best case which is a SiN core ( $n_{\text{SiN}} = 2$ ) surrounded by  $\text{SiO}_2$  claddings ( $n_{\text{SiO}_2} = 1.44$ ). In the constant region, the transmittance oscillates for all materials. This is most likely due to a Fabry-Perot effect created by the cavity formed by the gap closed by the DL and WG facets.

Refractive indices								
DL active zone	DL claddings	Air	SiN	$\text{SiO}_2$	Si	BCB	ChG ( $\text{Al}_{20}\text{Se}_{80}$ )	Ge
3.695	3.27	1	2	1.44	3.44	1.53	2.59	4

Table 13. Refractive index of different materials under study.

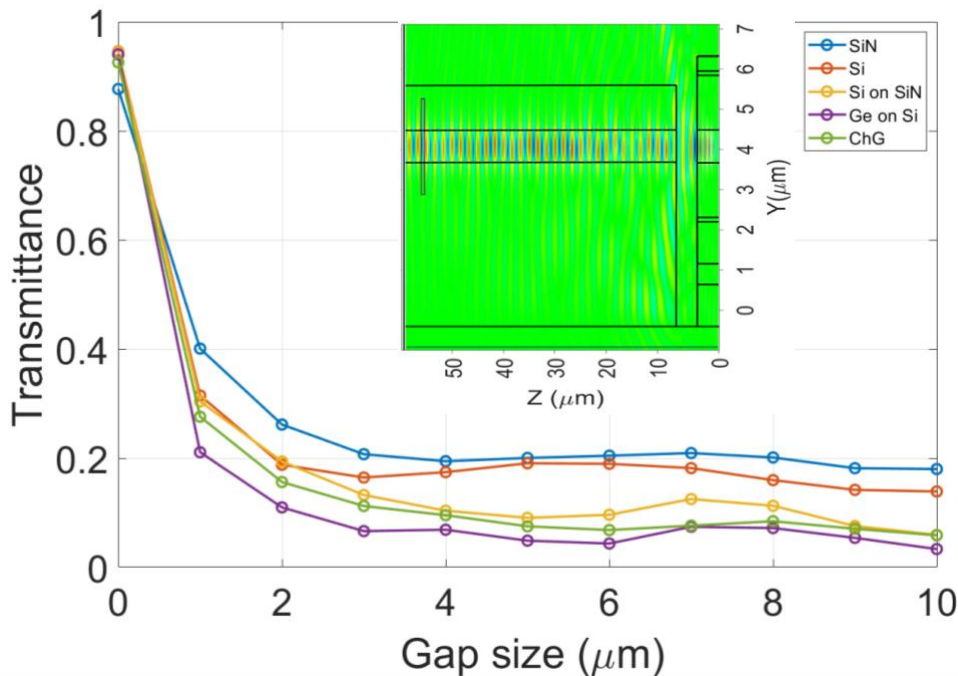


Figure 85. Transmittance as a function of the air gap for different passive core materials.[70]

The measured coupling efficiency is in line with the theoretical calculations. Experimentally, we obtained an air gap of about 11  $\mu\text{m}$ . According to simulations, an air gap of 10  $\mu\text{m}$  should give a coupling efficiency below 20%, which is relatively close to our experimental result.

We studied as well the influence of the thickness of the passive core on the transmittance. The divergence of the beam being high, a large portion of the light is not directed towards the input of the passive core. Increasing the thickness of the passive core should therefore increase the coupling efficiency. We simulated the transmittance into the SiN/ $\text{SiO}_2$  waveguide for SiN thicknesses in the 0.7 to 1.4  $\mu\text{m}$  range, as a function of the air gap size (Figure 86). For a fixed gap of 5  $\mu\text{m}$ , the transmittance increases from around 20% to 30%

as the SiN thickness increases from 0.7 to 1.4  $\mu\text{m}$ , respectively (inset of Figure 86). Although increasing the thickness of the passive core could provide an improvement in transmittance, growing thick layers of SiN, typically above 1  $\mu\text{m}$ , results in the formation of cracks which would affect light propagation.[143]

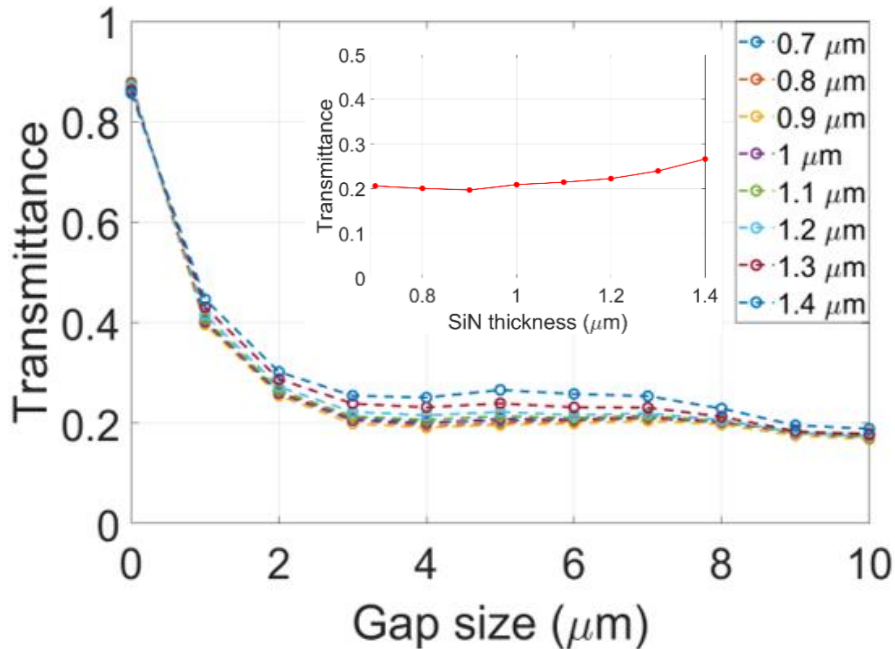


Figure 86. Transmittance as a function of the air gap for a SiN/SiO<sub>2</sub> waveguide and for different passive core thicknesses.[70]

### 3.12 Conclusion

In this chapter, we have investigated a monolithic integration approach to epitaxially grow a GaSb DL on a Si PIC with light coupling between the integrated laser and a SiN waveguide in a butt-coupling configuration. As a test vehicle, we used the same GaSb DL studied in chapter 2, which can be easily benchmarked. For the Si PIC, we decided to use SiN-based waveguides clad by SiO<sub>2</sub> layers, which have low losses in the near-to-mid-IR wavelength range.

In this monolithic approach, the laser cavity mirrors cannot be fabricated by cleaving because the DL and the PIC are on the same chip. An etched-facet process was therefore addressed separately. First, we developed a fabrication process aimed at obtaining smooth and vertical facets. The smoothness obtained was similar to that previously achieved in our team, with a reflectivity similar to that of cleaved facets. A verticality of 91° was achieved, a very promising value for light coupling in this butt-coupling configuration. An entire DL process was then established to fabricate etched-facet DLs with similar performance to that of cleaved lasers. We concluded that the etched-facet process could be validated and adapted to the Si PIC.

We then studied the integration of the DL on the Si PIC. The first challenge to overcome was the fabrication of the SiN waveguides without compromising the surface quality of the Si

substrate. The epitaxial growth of the laser heterostructure was then successfully performed using the same strategies and similar growth conditions used for discrete DLs on plain Si substrates. The III-V polycrystal material deposited on the WG stack and at the laser/WG interface could be removed, followed by laser facet definition. However, these two steps and the problem of the oxide step created a gap of about  $\sim 11 \mu\text{m}$  for this sample. The rest of the laser process was then successfully carried out to demonstrate an integrated DL with similar performance to that of DLs grown on plain Si substrates. We then demonstrated that 10% of the light emitted from the laser facet is coupled and propagated in the s-bend waveguide. Note that the air gap has two origins, one is the polycrystal material deposited at the III-V/WG interface during epitaxy, the other one is the definition of the cavity mirrors. The first origin is unavoidable and the second one could be reduced by solving the oxide step problem, which can be easily solved during the fabrication, and by refining the laser process steps, or by using FIB for the facet definition.[144]

We have then performed FDTD simulations to understand the light coupling behavior in this configuration. They show that the air gap between the DL and the WG has a strong influence on the coupling efficiency due to the high refractive index contrast between the DL active zone and the air, which induces a high divergence of the laser beam. In addition, we have compared the simulations with the experimental results. The experimental value is in agreement with the FDTD simulations.

Interestingly, only two other works have demonstrated optical coupling using a monolithic integration approach on Si platforms, and they were done in the same time period as ours.[145], [146] They used quantum dot lasers coupled to SOI[145] and to SiN[146] waveguides by FIB for facet etching.

This study was carried out using GaSb DLs, which are very sensitive to threading dislocations, which degrades the device lifetime. This approach can be extended to any semiconductor material system provided that the antiphase domain problem can be solved and the process steps are established. We demonstrated that the various process steps do not pose any fundamental issue. This approach can therefore be implemented with long-lifetime ICLs or QCLs, paving the way for long-lifetime integrated sensor chips.

The next challenge is to increase the coupling efficiency, as 10% is still too low for most applications. In the next chapter we will study different approaches to increase the coupling efficiency of this butt-coupling configuration by reducing the air gap, filling the gap or achieving zero gap.



# 4 Chapter 4. Increasing the coupling efficiency of the integrated GaSb diode lasers on the Si PIC

In the previous chapter we have demonstrated for the first time the optical coupling between the monolithically integrated GaSb DL and the SiN waveguide in a butt-coupling configuration. Still, we have also seen that the coupling efficiency was limited by an air gap inherent to the processing. In this chapter, we will evaluate possible solutions and alternatives to increase the coupling efficiency.

## 4.1 Filling the gap

### 4.1.1 Simulations

As discussed in section 3.11, the air gap has a drastic impact on the coupling efficiency, reducing it from 80% to around 20% for gaps above 2  $\mu\text{m}$ . This is due to the high refractive index contrast between the laser active zone and the air (3.695 vs. 1), which causes high beam divergence, resulting in high insertion losses. Therefore, reducing the refractive index contrast should reduce the beam divergence. We have investigated the coupling when the air gap is filled with a material of higher refractive index in order to reduce the refractive index contrast (Figure 87).

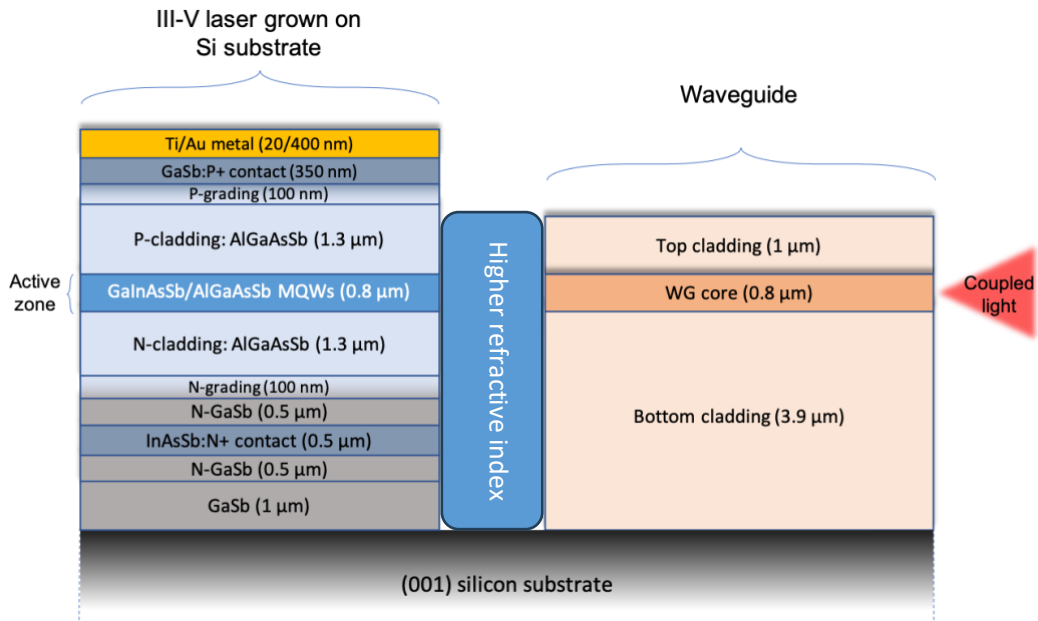


Figure 87. Cross-section sketch of the DL butt-coupled with the WG with a filled gap with a material with a higher refractive index.

We first performed FDTD simulations to study the improvement in coupling efficiency when filling the gap with various materials that are considered transparent for wavelengths near  $2.3 \mu\text{m}$  and whose refractive indices are given in Table 14. The transmittance as a function of the gap size for the different materials is shown in Figure 88. An improvement in the coupling can be observed with all materials. For example, for a gap fixed at  $5 \mu\text{m}$ , the transmittance increases from  $\sim 20\%$  when the gap is air, to  $\sim 40\%$  when the gap is amorphous silicon (inset of Figure 88) or  $\sim 30\%$  when the gap is SiN, for example. In addition, it can be observed that the reduction in coupling efficiency with the gap size is less drastic when filled with these higher index materials than with the air gap.

Refractive index								
DL active zone	DL claddings	Air	SiN	SiO <sub>2</sub>	PMMA	Si	BCB	ChG (Al <sub>20</sub> Se <sub>80</sub> )
3.695	3.27	1	2	1.44	1.47	3.44	1.53	2.59

Table 14. Refractive indices of different materials.

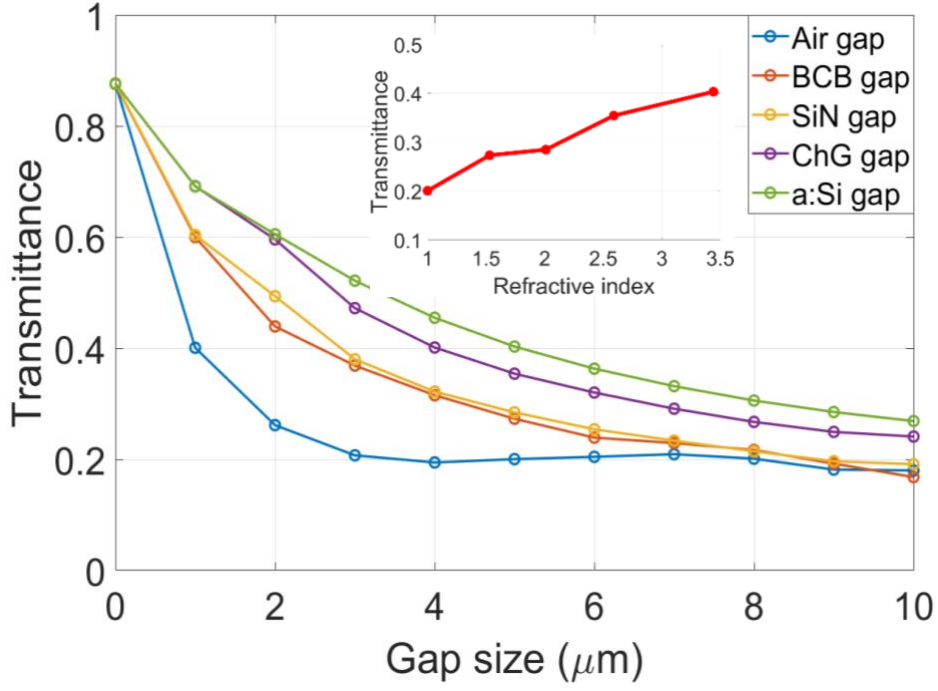


Figure 88. FDTD simulations of the transmittance as a function of the gap size for different gap materials.

On the other hand, reducing the laser/gap refractive index contrast will also reduce the reflectivity of the laser facet. I have therefore also investigated the effect of the reduced reflectivity on the laser performance, using the same theoretical gain model as in section 2.5 for a 2-QWs structure grown on Si. As mentioned in that section, the gain model does not take into account thermal effects, so the calculation results would correspond to broad-area lasers operating in the pulsed regime. The reflectivity at an interface of two media 1 and 2 can be calculated for the simplest case with normal incidence using the following equation:

$$R = \left| \frac{n_1 - n_2}{n_1 + n_2} \right|^2$$

Equation 14. Reflectivity at an interface between two media 1 and 2.

where  $n_1$  and  $n_2$  are the refractive indices of the media 1 and 2, respectively.

This equation explains the reduction in reflectivity when the refractive index contrast is lower. The laser cavity has two mirrors with different reflectivity values and the Fabry-Perot cavity losses are now given by:

$$\alpha_{FP} = \frac{1}{2L} \ln \left( \frac{1}{R_1 R_2} \right)$$

Equation 15. Fabry-Perot cavity losses when the reflectivity of the mirrors is not equal.

where  $R_1$  is the reflectivity of the back etched-facet with air as the second medium ( $R_1 \sim 0.3$ ) and  $R_2$  is that of the other etched-facet with the new gap filling material as the second medium.

I then calculated the threshold current density using Equation 5 for a 2-QWs structure on Si and for different gap filling materials corresponding to different refractive indices  $n_2$ , which

influence the reflectivity  $R_2$ . Figure 89.a shows the calculated threshold current density as a function of the cavity length for different gap filling materials. We can observe that the curves are shifted to higher threshold current density values as the refractive index increases. We can also observe that the threshold current density drastically increases as the cavity length decreases. Using longer cavities can therefore attenuate the increase in threshold. In addition, depositing a high-reflection (HR) coating on the back etched facet of the laser can be an option to increase the facet reflectivity, which can easily reach up to 90%,[147] and compensate for the reduction in reflectivity of the other facet. Figure 89.b shows the evolution of the threshold current density as a function of refractive index for a cavity length of 1.5 mm with and without HR coating ( $R_1=0.9$ ), and a cavity length of 3 mm without HR coating. In the case of no HR coating on the back etched facet and a cavity length of 1.5 mm, which is the length of our DLs, the threshold current density increases from 470 to 510, 590, 720 and 1310 A/cm<sup>2</sup> when the gap is filled with SiO<sub>2</sub>, SiN, chalcogenide and amorphous silicon, respectively. However, in the case of an HR coating and a cavity length of 3 mm, the threshold is maintained or even reduced for refractive indices up to that of chalcogenide. The reduction in reflectivity caused by filling the gap with higher index materials would therefore not be a problem given these options.

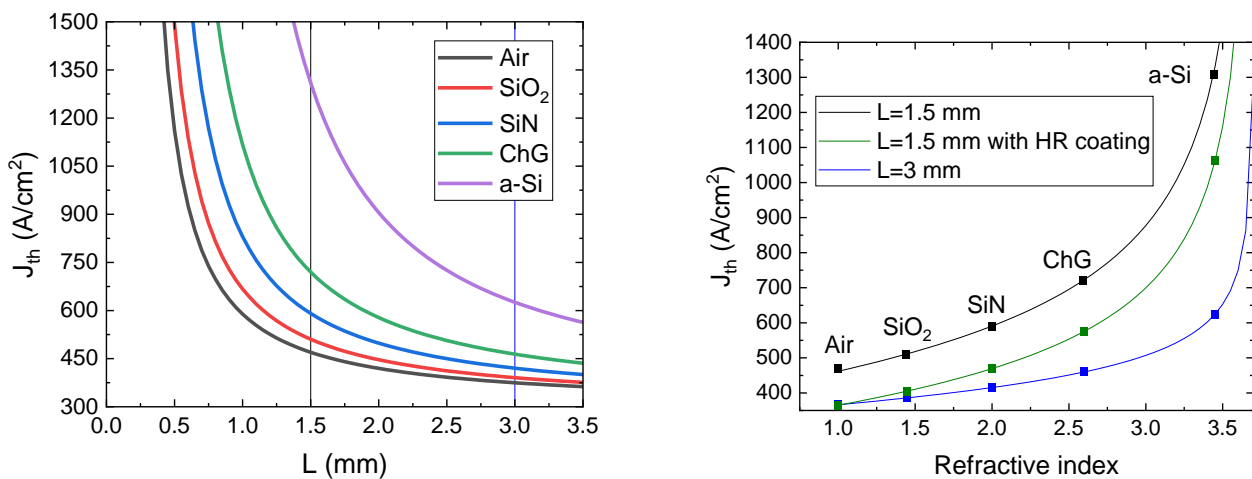


Figure 89. a) Threshold current density as a function of the cavity length for different materials filling the gap. b) Threshold current density as a function of the refractive index of the material filling the gap for a cavity length of 1.5 mm with and without HR coating and a cavity length of 3 mm without HR coating.

On the other hand, it is also necessary to consider whether filling the gap with these materials is feasible from a fabrication point of view. For materials such as amorphous silicon or chalcogenide, filling a narrow gap may prove cumbersome. However, polymers such as benzo cyclobutene (BCB) ( $n=1.53$ ) or polymethyl methacrylate (PMMA) ( $n=1.47$ ) could easily fill the gap thanks to their liquid state prior to polymerization. In addition, SiO<sub>2</sub> or SiN would also be good candidates due to their precise and homogeneous deposition by PECVD.



### 4.1.2 Filling the gap with PMMA

As a first approach, we decided to fill the gap in the sample fabricated in the previous chapter with PMMA, which has a similar refractive index to that of SiO<sub>2</sub>. We first evaluated the absorption of PMMA. A drop was first applied to a microscope slide with a pipette and a FTIR absorption measurement was carried out with and without baking the PMMA. The transmittance as a function of the wavelength is shown in Figure 90.

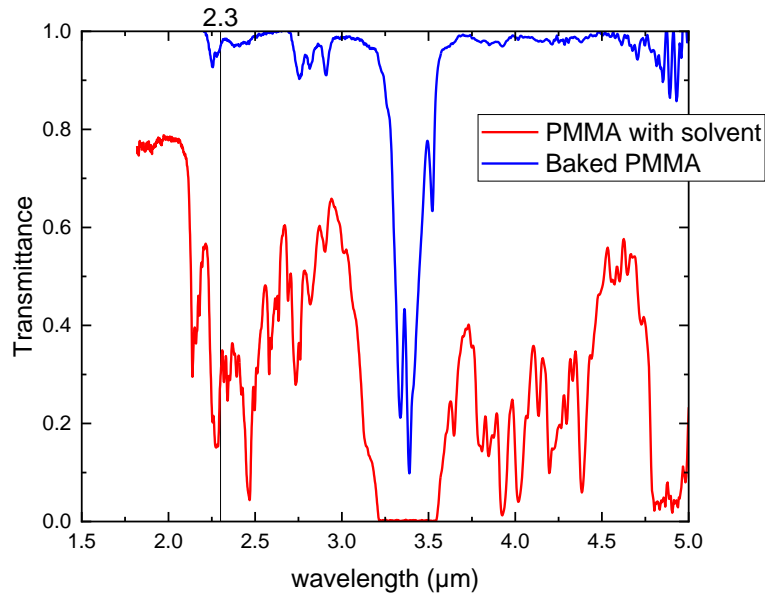


Figure 90. Absorption measurement of a PMMA drop as a function of the wavelength with and without a bake.

We can observe that when the PMMA is not baked, the absorption is high in the 2-5- $\mu\text{m}$  range, whereas when it is baked, the solvent is evaporated and the transmittance is close to 97% for wavelengths near 2.3  $\mu\text{m}$ , where our DL emit. The drop thickness was measured at different spots with the profilometer. The absorption was then calculated using the Beer-Lambert law (Equation 16),

$$\frac{I}{I_0} = \exp(-\alpha \cdot d)$$

Equation 16. Beer-Lambert law.

where  $I$  and  $I_0$  are the transmitted and initial intensity of the light, respectively,  $I/I_0$  thus represents the transmittance,  $\alpha$  is the absorption in the PMMA and  $d$  is the thickness of the PMMA drop.

We obtained a value as low as  $\sim 0.3 \text{ cm}^{-1}$  which shows that the PMMA absorption can be neglected near 2.3  $\mu\text{m}$ . The gap was then filled with PMMA by pouring and baking a drop in the gap area of a representative DL/WG pair (see Figure 91.a). L-I measurements were then taken on this DL/WG pair (Figure 91.b).

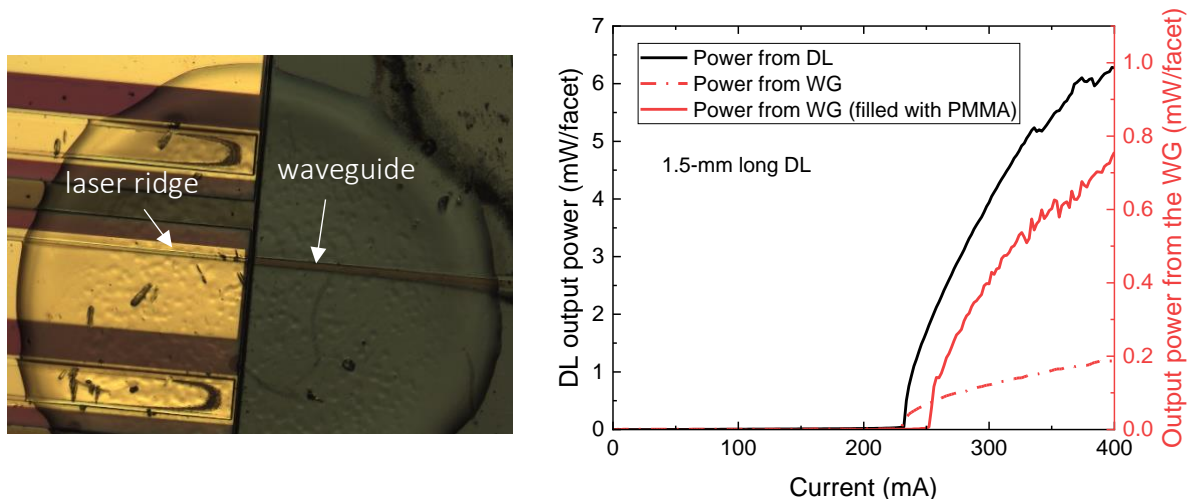


Figure 91. a) Optical image of the PMMA drop deposited on the sample. b) L-I curves after filling the gap with PMMA of a DL-WG pair.

In Figure 91.b, the black curve represents the L-I characteristic of the etched-facet DL. The dashed red curve and the solid red curve represent the L-I curve of the coupled light with an air gap and with a PMMA gap, respectively. For this particular device, the coupling efficiency has been improved by a factor of 4 (from 3% with an air gap to 11% with a PMMA gap). In addition, an increase of  $\sim 8\%$  in the threshold current is observed (from 233 to 252 mA), which is not a significant deterioration compared to the improvement in coupling. As mentioned before depositing a HR coating on the back etched-facet of the laser can be an option to compensate for the reduction in reflectivity of the other facet. This result confirms that the PMMA drop is filling the gap and is in good contact with the DL facet, resulting in a reduction of the DL reflectivity. This shows that gap filling is a promising strategy to improve the coupling efficiency. Note that we could not perform this measurement on a DL/WG pair with 10% of coupling efficiency because of the many previous measurements taken on these lasers, which caused their lasing degradation due to their short lifetime

In addition, the FDTD simulations (Figure 88) show that the narrower the gap, the stronger the improvement in coupling by filling the gap. Therefore, in the next section, I decided to further optimize the process of the laser on the Si PIC in order to achieve a narrower gap than that achieved in the previous chapter.

## 4.2 Laser process optimization to reduce the gap

### 4.2.1 Polycrystal removal optimization

The first optimization of the laser process consisted in precisely calibrate the polycrystal removal step (see section 3.7) in order to obtain a laser facet close to the WG. As discussed in section 3.7, different mask alignments result in different under-etching of the epitaxial structure. By refining this alignment, I was able to reduce this under-etching, allowing the gap to be reduced. Two different results are shown in Figure 92. At the end of this step, the gap of

the first sample is  $< 5 \mu\text{m}$  (Figure 92.a) whereas the one of the second sample is near  $7 \mu\text{m}$  (Figure 92.b). Note that in the first sample, the poor crystal quality arising from the growth on the oxide step (see section 3.7) is still present whereas it was removed on the second sample.

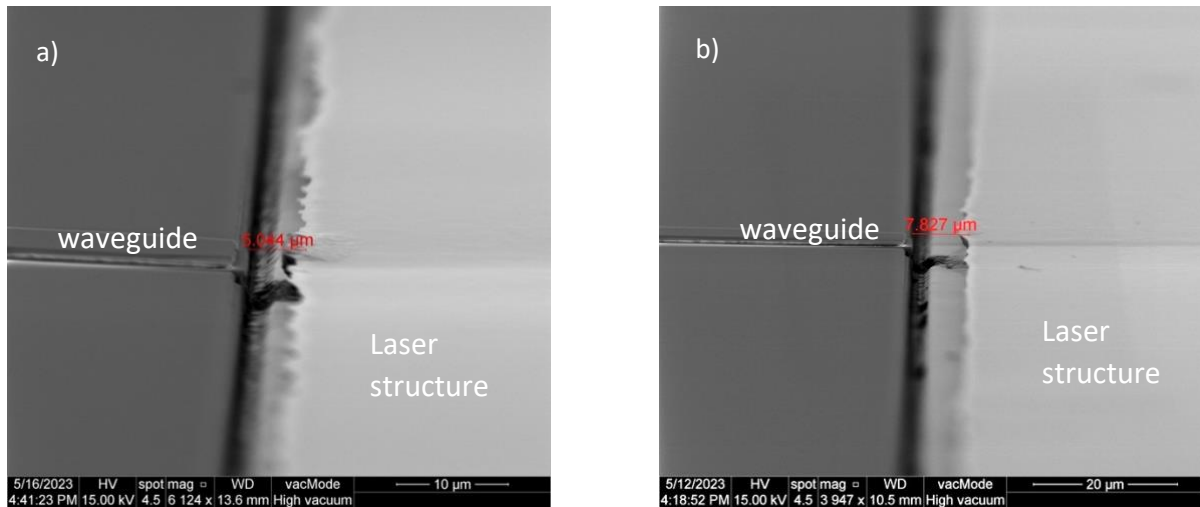


Figure 92. Optimized polycrystal removal step for two different mask alignments resulting in different gaps.

#### 4.2.2 Laser facet definition

The next step is to define the DL facet. Figure 93 shows SEM images of both samples after the lithography of the DL facet, carried out with the same parameters as in the previous chapter. We can observe that for both samples, a minimum air gap of slightly more than  $7 \mu\text{m}$  could be obtained, instead of the  $\sim 11 \mu\text{m}$  achieved in the previous chapter.

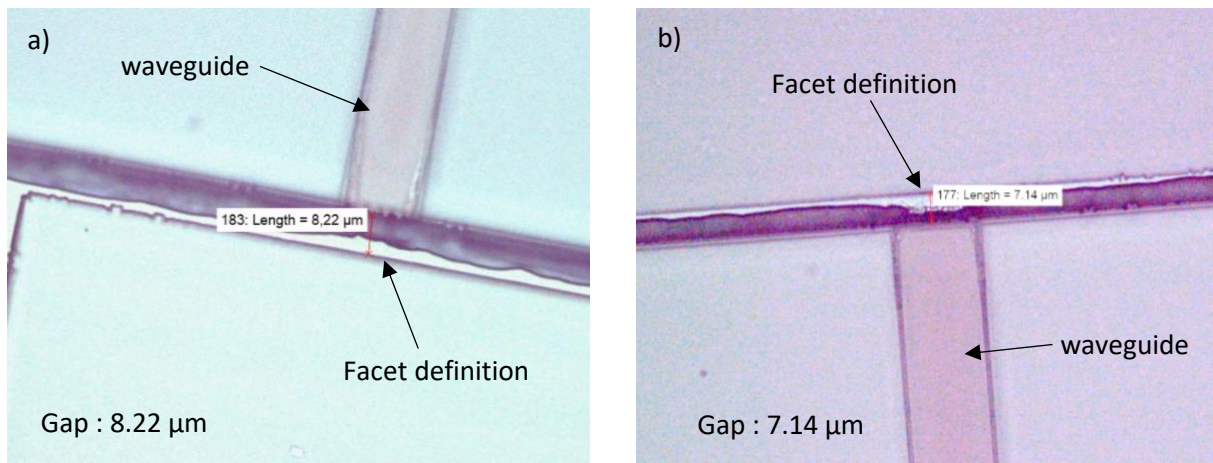


Figure 93. SEM pictures after the lithography of the laser facet of two samples a) and b) where the gap was reduced.

Further SEM images confirm similar laser facet smoothness and angle as those obtained in the previous chapter (Figure 94). However, it can be observed that at the edge of the epitaxial growth, the III-V structure has not been completely etched, leaving behind a thin III-V “hill” in the middle of the air gap which could cause reflections and disturb light coupling. This edge effect is due to the narrow aperture of the mask during the ICP etching of the laser facet. It has been observed in previous works and is unavoidable. We therefore decided to perform an

additional step to try to remove this peak in the gap without compromising the quality of the DL and WG facets.

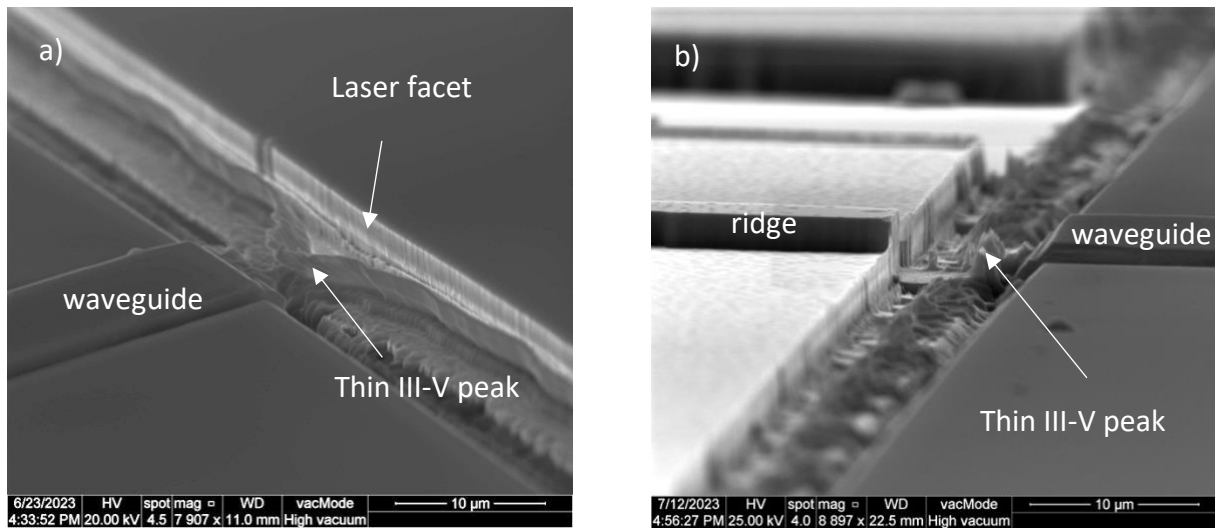


Figure 94. SEM images of the samples. a) image after the facet etching, b) after the laser ridge.

### 4.2.3 Thin III-V peak removal

In order to remove this III-V peak remaining in the middle of the gap, a new mask was designed to allow dry etching in the gap while protecting the WG and DL facets. The opening in the gap was designed to be 4- $\mu\text{m}$  wide. The lithography was performed on the first sample using a double layer of the positive resist AZ1518 to ensure complete protection of the WG and DL facets, especially the facet edges. The first attempt was done using the bottom contact lithography parameters from Table 3. A very precise alignment should be carried out to avoid exposing either of the two facets. The result of the lithography is shown in Figure 95.a. We can observe that the opening is not fully achieved. This is due to the narrow aperture of 4  $\mu\text{m}$  together with the thick double layer resist. After several attempts, we found that an exposure time of 4 minutes and a development time of 1 minute and 20 seconds was necessary to completely open the resist in the gap (Figure 95.b).

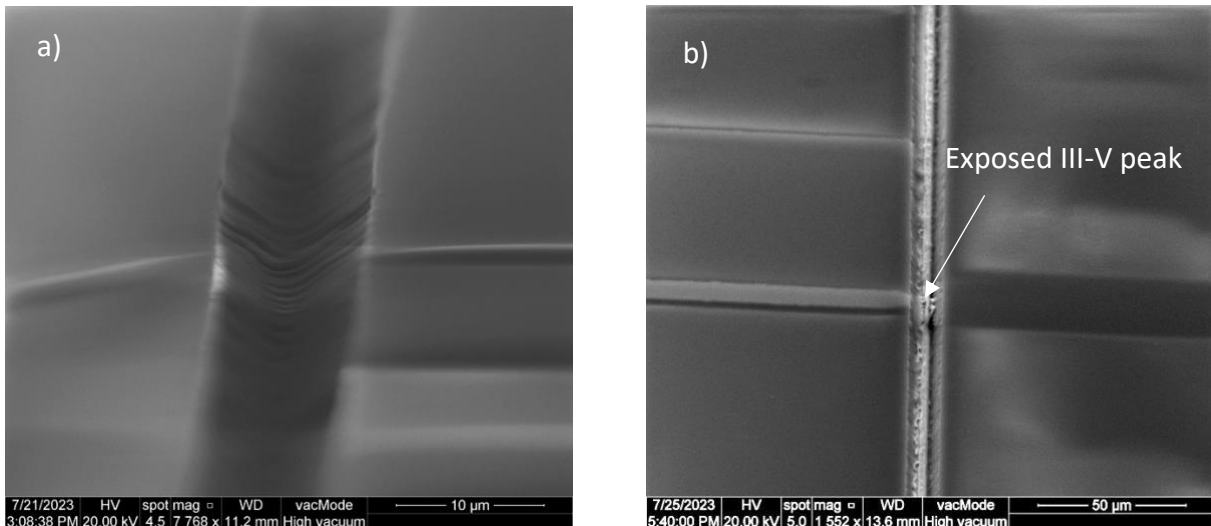


Figure 95. SEM image of the lithography result using the same parameters as the bottom contact etching.

We then performed the ICP etching to remove the III-V peak. After 12 minutes we could observe that the peak was completely etched, leaving behind a clear air gap while protecting the WG and DL facets, as we can see in Figure 96.

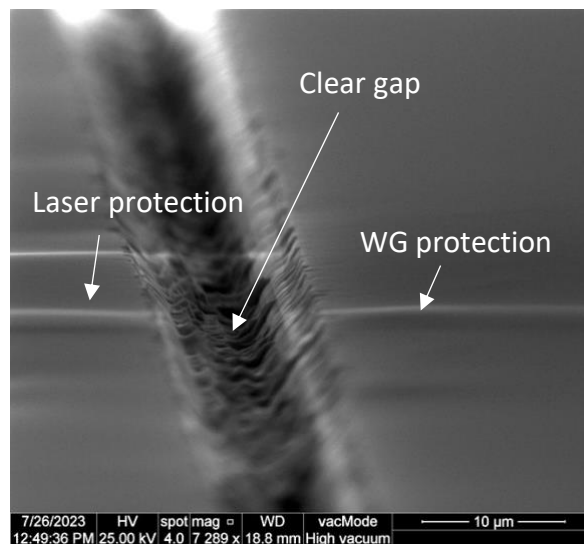


Figure 96. SEM image of the sample after the III-V peak removal step and before removing the resist.

The subsequent process steps (bottom contact, electrical insulation and metallization) were then carried out using the same parameters as those used in the previous chapter. The substrate was then thinned down and cleaved in the same way as in the previous chapter.

The bars were mounted on Cu heat sinks and characterized. Unfortunately, the lasers did not achieve lasing. After analysis, we found that the problem stemmed from the doping of the laser heterostructure. Although we were unable to demonstrate an improvement in coupling efficiency with these new samples, we were able to demonstrate a refined laser process that allowed the air gap to be reduced.

According to the FDTD simulations, a gap of 7  $\mu\text{m}$  is still not sufficient to achieve high coupling efficiencies. However, the gap could be reduced (limited by the width of the polycrystal material deposited at the III-V/WG interface) by solving the  $\text{SiO}_2$  step problem and by using other techniques such as e-beam lithography or FIB. In the next section, we decided to explore alternative approaches to reducing the gap size.

## 4.3 Alternative approaches

In chapter 3, we decided to investigate the light coupling using the lowest loss SiN waveguides fabricated at Tyndall. In that case, it was necessary to fabricate the Si PIC first, and then grow and process the DL structure to avoid damaging the laser during the high-temperature passive waveguide fabrication. However, another alternative is to fabricate SiN WGs using low temperature processes such as PECVD deposition at 280°C or e-beam evaporation deposition near room temperature, both of which are available in our clean room. The advantage of this would be to grow the III-V laser structure first, and then have the freedom to perform the laser and waveguide fabrication steps in the most appropriate order.

As a first approach we aimed to fabricate the laser facet and then deposit the WG layers in such a way that a butt-coupled geometry is achieved, with a vertical alignment of the WG core with the laser active zone. We have investigated two different approaches, which I will describe in the next sections.

### 4.3.1 Waveguide fabrication on etched-facet laser by e-beam evaporation

#### 4.3.1.1 Preliminary test

This first approach consists of patterning a resist to protect the laser facet, depositing a WG layer by e-beam evaporation, and performing a lift-off to remove the WG layer from the unwanted areas (Figure 97). For the lithography, a thick negative resist such as AZ2070 is required to cover the laser facet and the top of the laser structure. The negative resist profile, together with the anisotropic deposition of the e-beam evaporation technique, should allow a discontinuity in the deposited WG layer to allow for later lift-off (Figure 97). This process could be repeated for each WG layer to form the WG stack. Finally, ICP etching could be performed to define a high quality WG facet. Note that this fabrication technique can only be performed with e-beam evaporation. PECVD depositions in our clean room are done at 280°C, which would burn the resist and prevent lift-off.

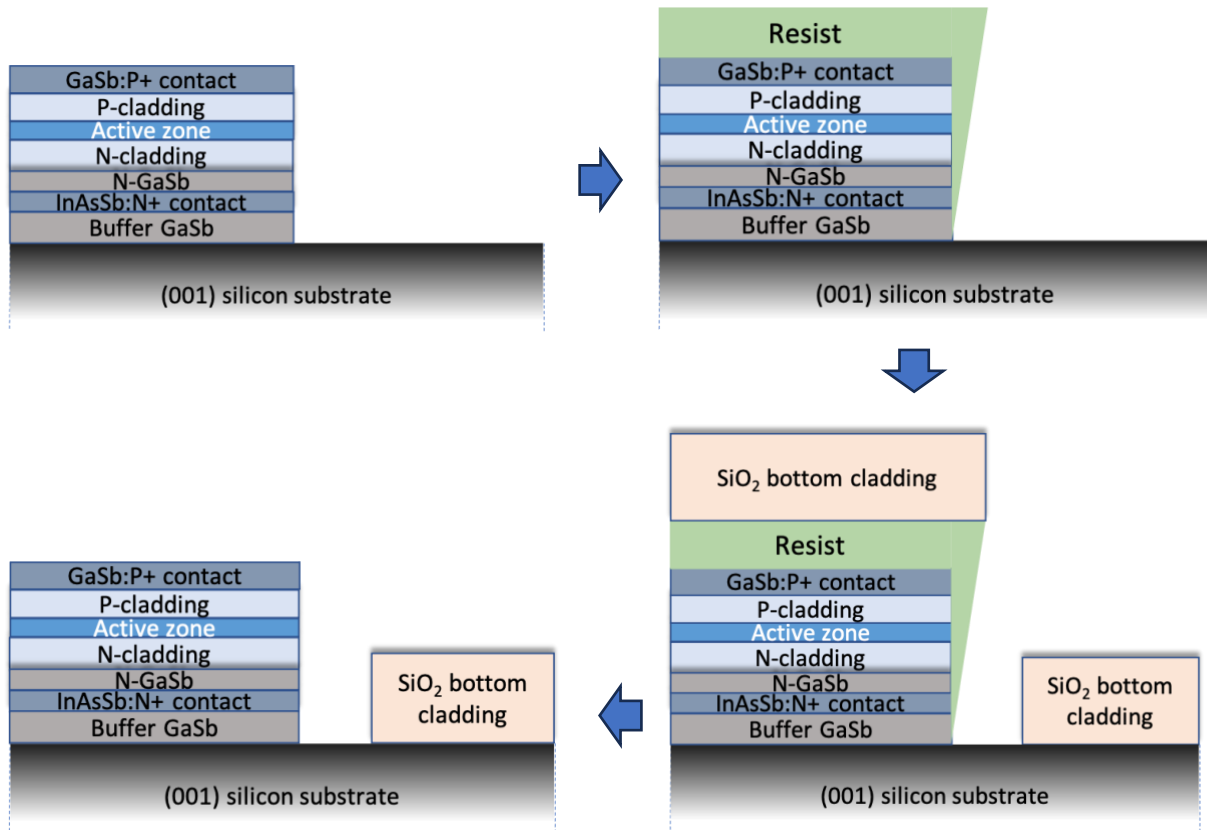


Figure 97. Sketch of the process technique to deposit the WG layers by lift-off technique after the DL fabrication.

A preliminary test was done on a GaSb substrate to investigate the feasibility of the process described above. A negative mask providing a 5- $\mu\text{m}$  protection of the laser facet was used. First, typical etched facets were performed. The lithography was then carried out using the negative resist AZ2070 and the parameters from Table 10. 400 nm of  $\text{SiO}_2$  were then deposited by e-beam evaporation and the undesired areas were successfully lifted (Figure 98). With this mask and lithography parameters, the gap between the facet and the  $\text{SiO}_2$  layer is around  $\sim 4.5 \mu\text{m}$ . However, the lithography mask and parameters could be modified to change the resist location and profile and reduce the gap size, which would be promising for achieving higher coupling efficiencies.



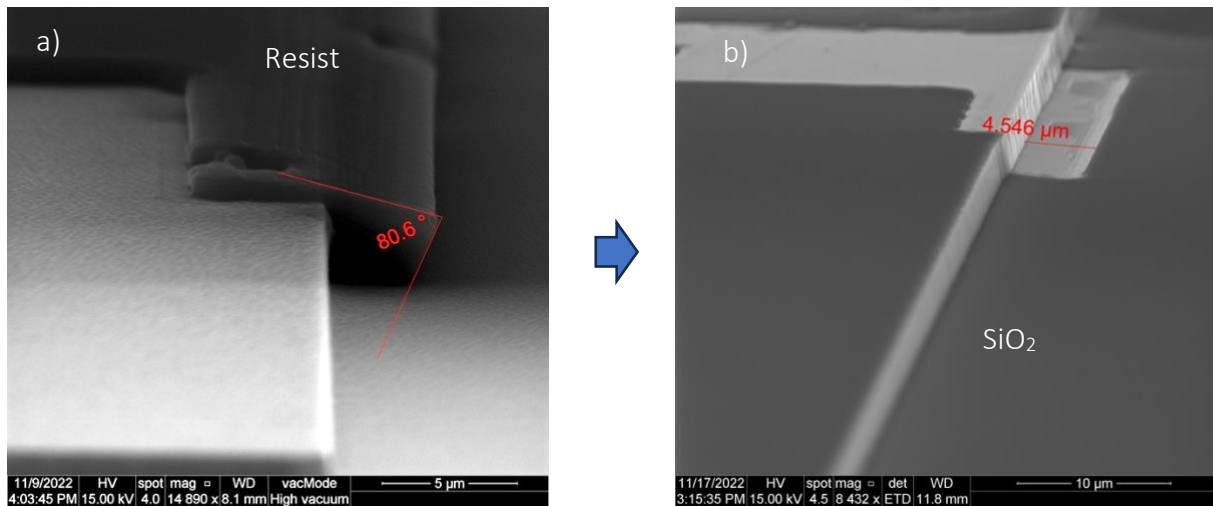


Figure 98. SEM images of a first test. a) Resist profile after the lithography. b) Device after the lift-off.

### 4.3.1 Waveguide fabrication on etched-facet laser by PECVD

In parallel, a second approach was also investigated. This one consists of depositing by PECVD the WG layers without prior photolithography.

#### 4.3.1.1 Preliminary tests

We realized preliminary tests on a GaSb substrate. Etched facets were first performed with the typical process technique, but this time the etching depth was  $\sim 6.5 \mu\text{m}$ . This depth was chosen in order to deposit a SiO<sub>2</sub> bottom cladding layer with the same thickness as in the previous chapter ( $3.9 \mu\text{m}$ ) and vertically align the active zone of the laser with the passive core of the waveguide. The SiO<sub>2</sub> bottom cladding layer was deposited by PECVD followed by  $0.8 \mu\text{m}$  of SiN core layer.

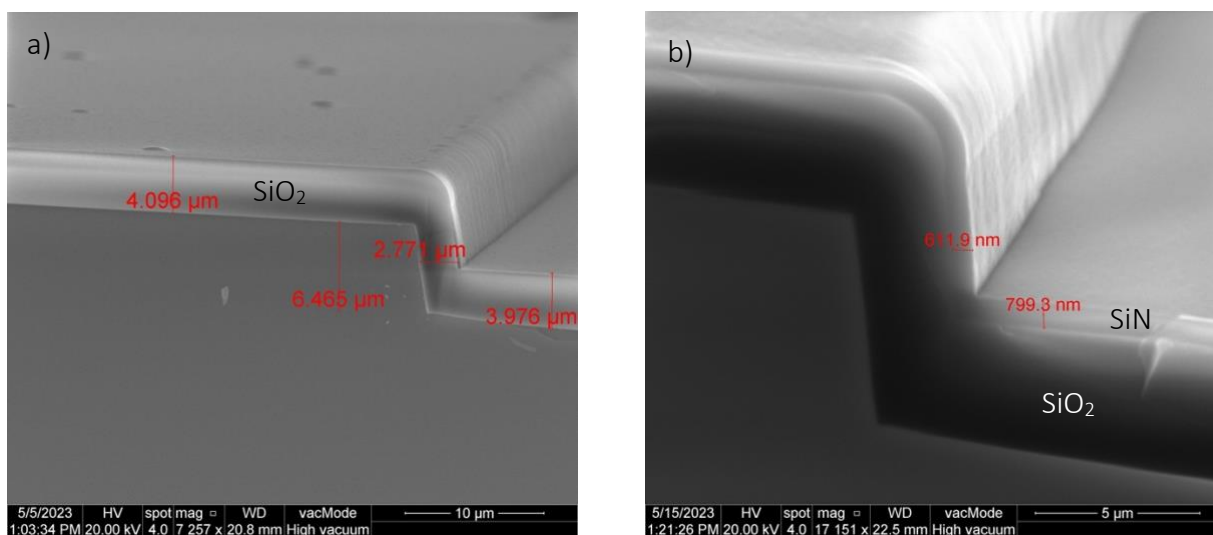


Figure 99. SEM images of PECVD depositions on a  $6.5\text{-}\mu\text{m}$  depth etched facet. a) Deposition of  $3.9 \mu\text{m}$  of SiO<sub>2</sub>. b) Deposition of  $0.8 \mu\text{m}$  of SiN on top of the  $3.9\text{-}\mu\text{m}$  SiO<sub>2</sub> layer.

Figure 99 shows SEM images of the depositions on the etched facet. We can observe that the SiO<sub>2</sub> and SiN depositions are conformal. We can therefore imagine using this configuration on a real DL where the SiO<sub>2</sub> layer deposited in front of the laser active zone would



act as a SiO<sub>2</sub> gap between the laser and the SiN WG core. However, we can observe that the etched facet is not as vertical (105°) as the one obtained in section 3.3.1.2 (91°). The deeper the etching, the higher the facet angle. On the other hand, the SiO<sub>2</sub> bottom cladding could be thinner than 3.9 μm without compromising the confinement of the optical mode in the SiN layer, which would allow reducing the etching depth of the facet while being vertically aligned with the WG core, thus reducing the facet angle. In addition, the thickness of SiO<sub>2</sub> deposited in front of the etched facet is proportional to the thickness on the planar regions. Reducing the thickness of the SiO<sub>2</sub> bottom cladding will therefore also reduce the size of the SiO<sub>2</sub> gap. Figure 99.a shows that a deposition of 3.9 μm of bottom cladding results in a gap of ~2.77 μm. With this observation, we can expect, for example, a gap size of around ~0.9 μm with a bottom cladding thickness of 1.3 μm, which is very promising for increasing the coupling efficiency. We decided to prioritize this approach as the results are more promising than in the first approach. A sketch of this configuration is shown in Figure 100.

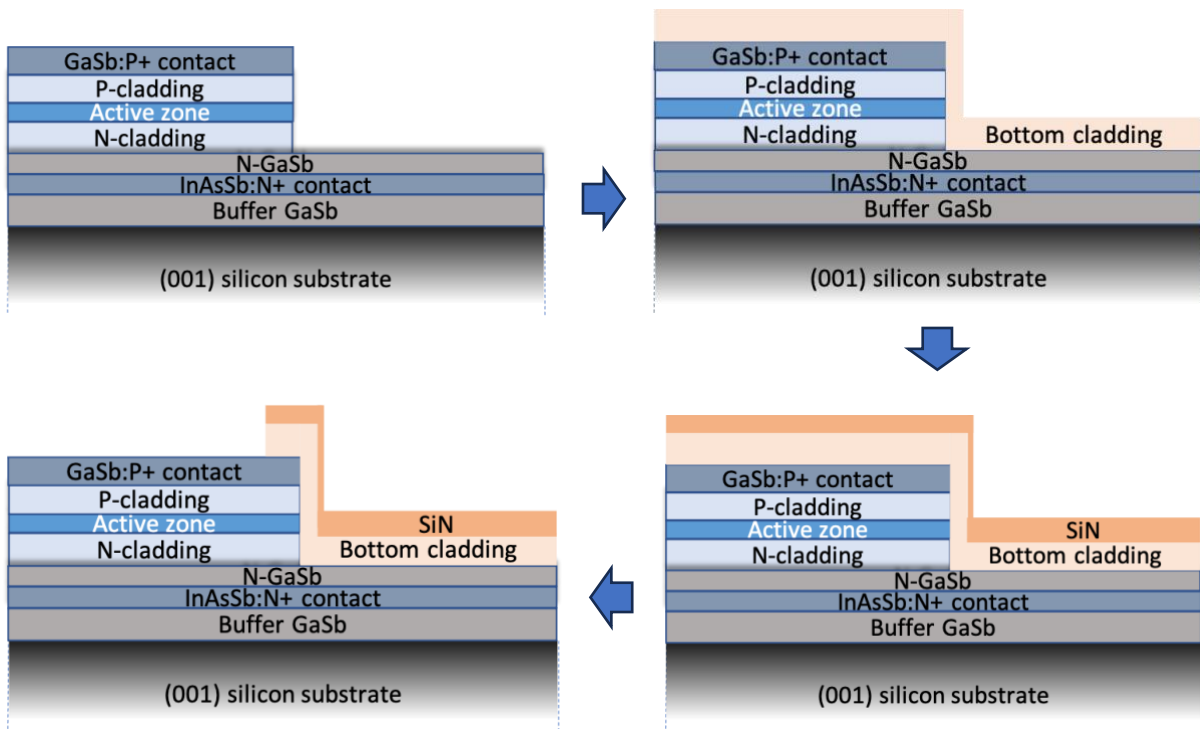


Figure 100. Sketch of the process steps to fabricate the WGs integrated with the etched-facet lasers with a SiO<sub>2</sub> gap.

#### 4.3.1.2 FDTD simulations

We have performed FDTD simulations to explore the optical coupling with this configuration and to investigate whether the mode can be well confined with a bottom cladding thickness of 1.3 μm. The SiO<sub>2</sub> gap size was set to 1 μm. The thickness of the SiN layer was set to 0.8 μm. Two simulations were performed, one with no WG top cladding (air) and the other with 1 μm of SiO<sub>2</sub> top cladding. The depth of the laser facet stops at the end of the laser structure bottom cladding, as shown also in Figure 100.

The simulations are shown in Figure 101. The results are very promising. We can observe that the mode is well confined in the SiN layer and that no evanescent field reaches the GaSb

layer below the SiO<sub>2</sub> cladding. The coupling efficiencies are as high as 45% and 50% for a configuration with no top cladding and with 1 μm of SiO<sub>2</sub> top cladding, respectively. These values are very high compared to those obtained in the configuration from chapter 3. We thus decided to develop a fabrication process in order to demonstrate the feasibility of this configuration and the optical light coupling with an improved efficiency.

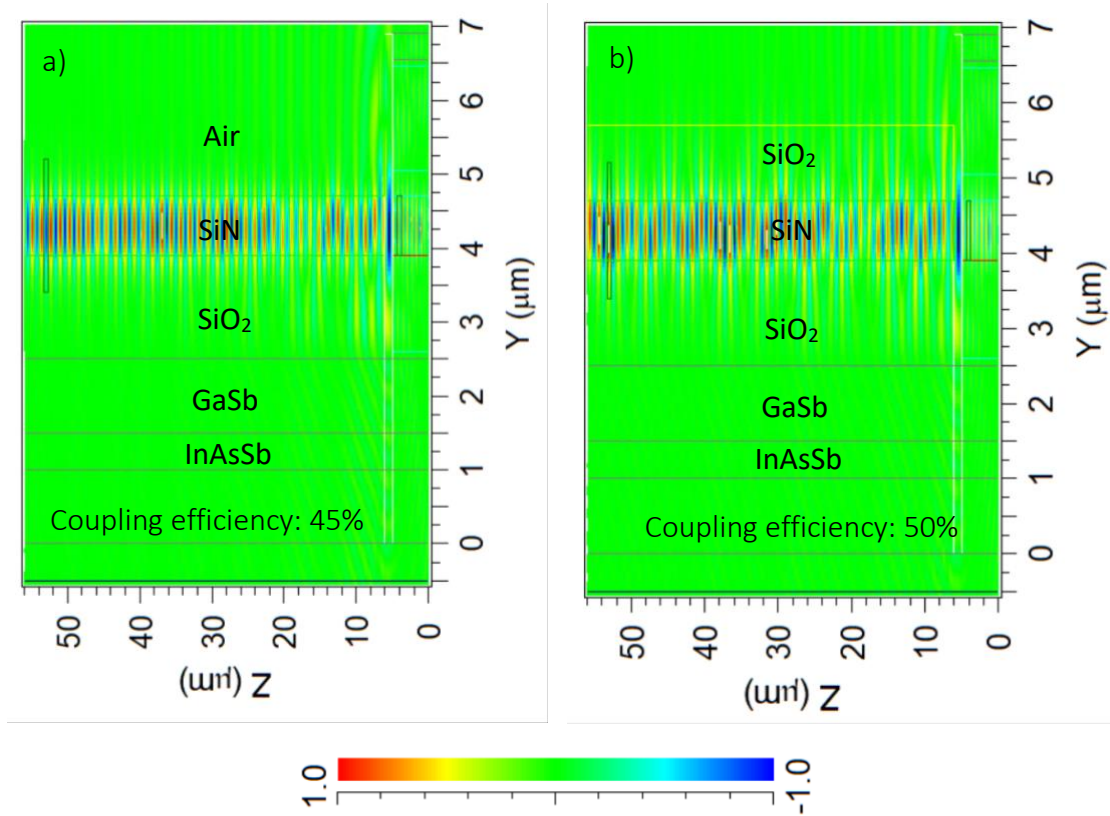


Figure 101. FDTD simulations of the new configuration. a) with air as the top cladding. b) with 1 μm of SiO<sub>2</sub> as the top cladding.

#### 4.3.1.3 Laser and waveguide fabrication process

While designing the lithography masks for this process, we have found that the most appropriate fabrication sequence is to process the WGs after etching the laser facet, so that the WGs are fabricated on a flat surface (Figure 102.a). Fabricating the WGs after the entire laser process would cause problems due to the complex morphology resulting from the other laser process steps (Figure 102.b).

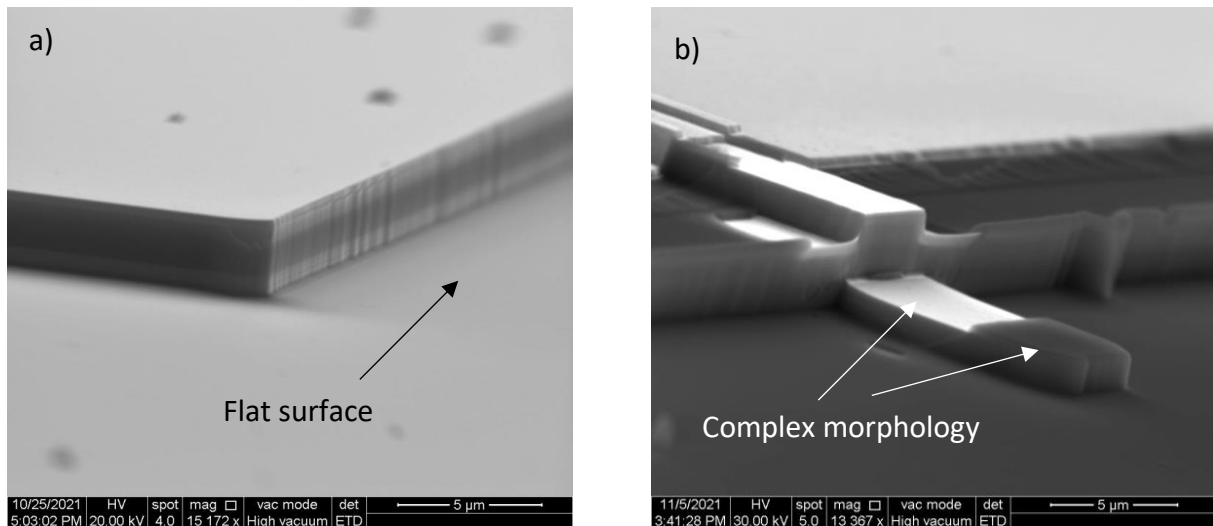


Figure 102. SEM images of laser morphology. a) after the etching of the facet. b) after the entire laser process.

As a first approach, I decided to do the fabrication first on a GaSb substrate to develop the new process. The next step would be the fabrication using GaSb DL grown on Si.

The WG consist in 1.3 μm of SiO<sub>2</sub> bottom cladding, 0.8 μm of SiN core layer and air or 1 μm of SiO<sub>2</sub> for the top cladding. The lithography masks for this fabrication were carefully designed to allow the laser and waveguide to be fabricated without compromising either.

The first step is the etching of the laser facet. The etched-facet laser cavities are 1.5-mm long. To be able to deposit 1.3 μm of SiO<sub>2</sub> bottom cladding for the WG while being vertically aligned with the laser structure, the facet etching was stopped at the end of the bottom cladding. For this purpose, the thickness of the SiN hard mask was adapted. Then, we deposited 1.3 μm of SiO<sub>2</sub> bottom cladding followed by 0.8 μm of SiN passive core by PECVD. Figure 103 shows a SEM picture of the bottom cladding deposition on the facet. We observe that less than 1.3 μm of SiO<sub>2</sub> are deposited on the flat areas whereas ~0.9 μm are deposited on the facet as expected from the test in Figure 99.

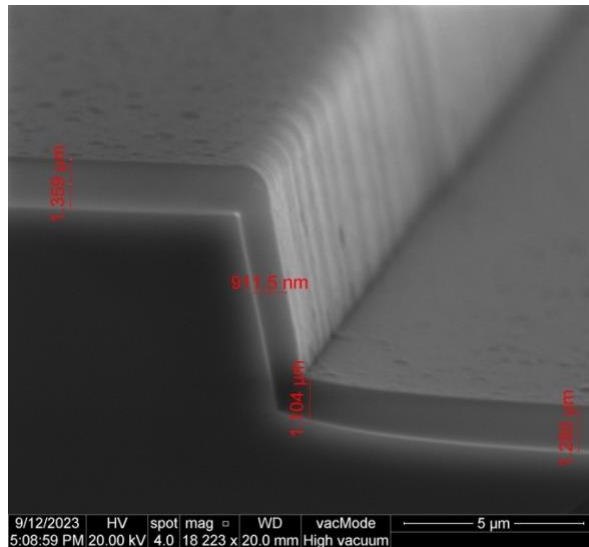


Figure 103. SEM picture of PECVD depositions of  $\text{SiO}_2$  and  $\text{SiN}$  depositions on the facet.

The next step is the WG definition. WGs were designed with an s-bend shape similar to that described in chapter 3 and are 10- $\mu\text{m}$  wide. The mask extends 5  $\mu\text{m}$  more on the etched-cavity to ensure the total protection of the WG stack located on the laser facet (Figure 104.a). The etching is performed by ICP and stopped at the end of the 0.8  $\mu\text{m}$  of  $\text{SiN}$ . Figure 104.b shows a SEM image of the device after the WG definition.

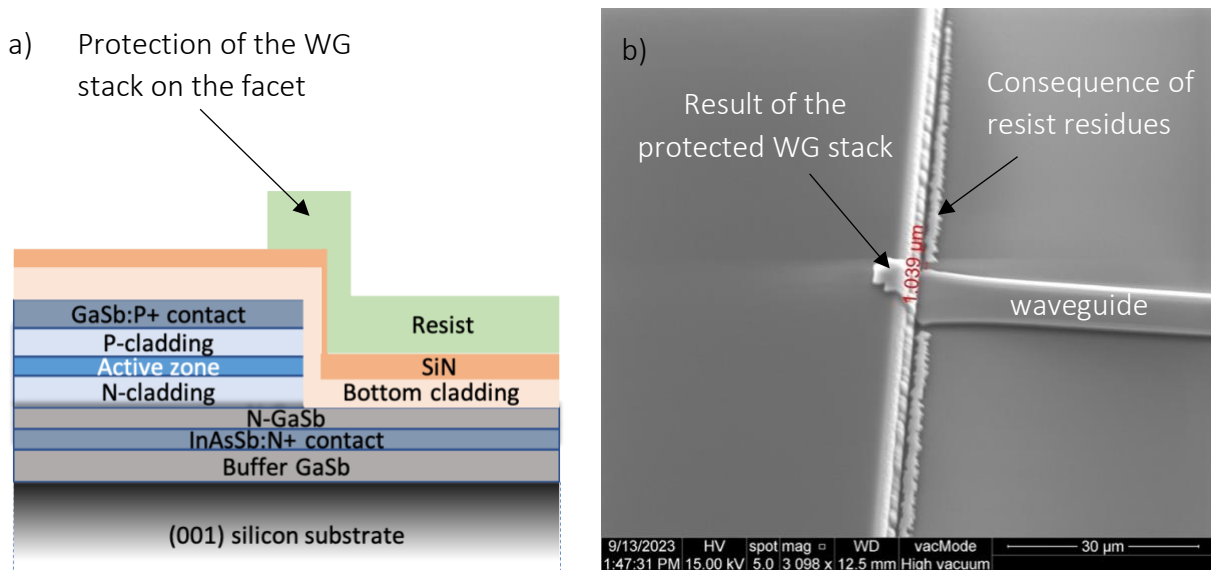


Figure 104. a) Sketch of the WG definition lithography. b) SEM image of the device after the WG definitions step.

We can observe that the WG stack on the facet was well protected thanks to the 5- $\mu\text{m}$  mask extension. However, the resist on the WG stack near the facet was very thin and close to being completely removed during the etching. To ensure that the resist is thick enough on this region, the rotation speed has to be reduced. In addition, we can observe in Figure 104.b some remaining  $\text{SiN}$  material on both sides of the WG near the facet, a consequence of resist residues after the lithography step. The remaining  $\text{SiN}$  does not reach the WG and this should not affect the light confinement in the WG. However, to ensure that there are no resist residues, the

exposure time will be increased. During this WG definition step, the SiN layer was removed from the top of the etched-facet cavity. An additional step was required to remove the remaining SiO<sub>2</sub> bottom cladding from the top of the cavity while protecting the WGs. The SiO<sub>2</sub> layer was successfully removed using ICP (Figure 106.a).

We then proceeded with the laser ridge definition. The ridge is 10-μm wide. The mask allows the ridge definition to be merged with the 5-μm extension coming from the WG definition. This allowed the laser ridge to be defined along the entire length of the etched-facet cavity (see Figure 105).

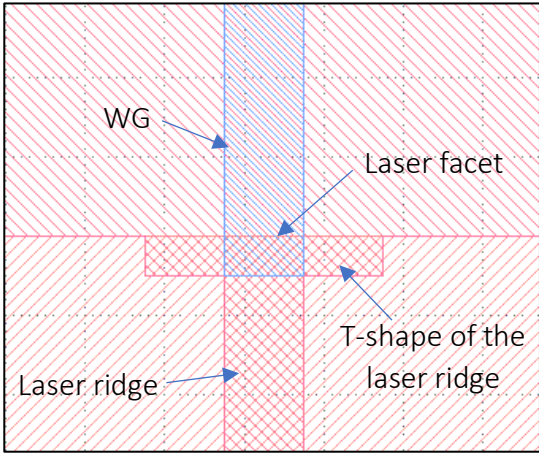


Figure 105. Mask design of the waveguide and laser ridge definition. The laser ridge mask has a T-shape close to the laser facet to push the corners away.

The mask also has a T-shape to push the corners away and avoid damaging the laser facet (Figure 105). The WGs were protected during etching. Figure 106.b shows a SEM image of the device after this step.

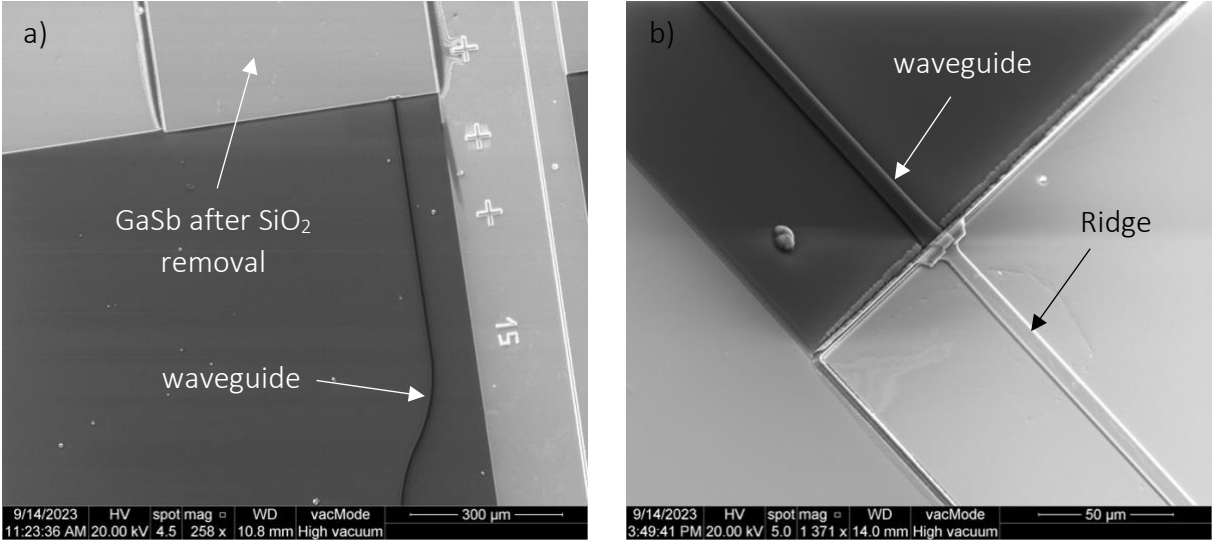
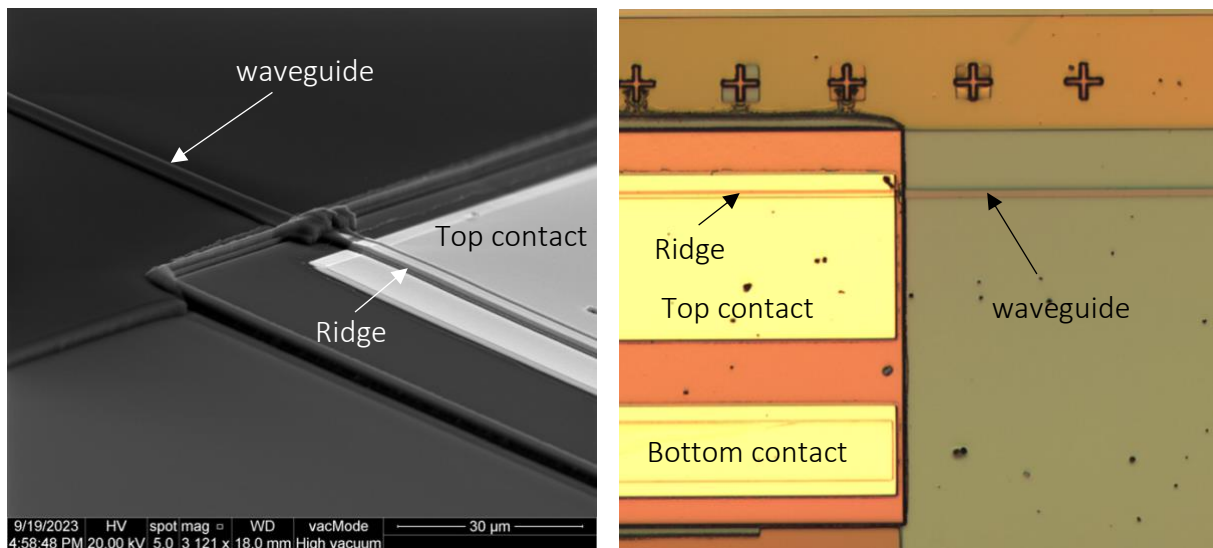


Figure 106. SEM image of the device after the ridge definition.

The bottom contact etching was then performed followed by the electrical insulation. The SiN insulation layer was removed from the top of the ridge and bottom contact as well as

the top of the WG stack. Finally, the Ti/Au metallization was performed. SEM and optical images of the final device are shown in **Figure 107**. The laser facet, SiO<sub>2</sub> gap and waveguide were successfully protected during these last process steps.



*Figure 107. Images of the final device after the metallization step. a) SEM image. b) optical image.*

The fabrication process for this new approach has now been developed. We have demonstrated that it is possible to fabricate lasers and WGs in a butt-coupling configuration with a  $\sim 0.9\text{-}\mu\text{m}$  SiO<sub>2</sub> gap in between the laser and the passive WG. Although the lithography parameters in the waveguide definition step had to be adjusted, no significant problems were encountered throughout the entire fabrication process. The next step is to demonstrate this fabrication process with a GaSb diode laser grown on a Si substrate and to couple light into the fabricated passive waveguide with improved efficiency. In addition, this approach can be improved by further reducing the SiO<sub>2</sub> bottom cladding layer thickness, as long as the light is well confined in the WG, which would result in an even narrower gap. It can therefore open the way to further promising investigations aimed at reducing the gap size and demonstrating that high coupling efficiencies can be achieved.

## 4.4 Conclusion

In this chapter, we have investigated several alternatives to increase the coupling efficiency. The first approach was to fill the air gap between the laser and the WG with a material of higher refractive index to reduce the divergence of the laser beam. FDTD simulations show an improvement in coupling efficiency. However, the theoretical gain model shows a deterioration in the laser threshold when the gap is filled with higher index materials, due to the reduction in reflectivity of the laser facet. Especially, as the refractive index approaches that of the laser active zone, the laser threshold is drastically affected. A first test was carried out by filling the gap with PMMA, a material with a similar refractive index to SiO<sub>2</sub> ( $n=1.47$ ). The coupling was improved by an order of 4 (from 3% to 11%), while the laser

threshold increased by 8%. The threshold degradation is low compared to the efficiency improvement, which is a very promising result for the gap-filling approach.

FDTD simulations show that the gap size is still critical for coupling efficiency, even when the gap is filled with a higher index material. I therefore decided to optimize the laser process in order to reduce the gap size. I was able to refine some steps and overcome new issues arising from this new process to demonstrate a minimum gap size of  $\sim 7 \mu\text{m}$  without reducing the laser facet quality. As discussed previously, the gap could be easily further reduced provided the  $\text{SiO}_2$  step problem is solved and by using other techniques such as e-beam lithography or FIB. Unfortunately, due to a doping problem in the laser heterostructure, the DLs did not lase and we could not perform further investigations such as filling the gap.

Alternative fabrication approaches and configurations were then investigated. These new approaches involve fabricating the waveguides after etching the laser facet. The most promising approach is to deposit the WG layers by PECVD without prior photolithography. Preliminary tests showed a conformal deposition of the layers, allowing us to imagine a possible coupling configuration with a very narrow gap made of  $\text{SiO}_2$ , while being vertically aligned with the laser active zone. According to FDTD simulations, the coupling efficiency should increase up to 45-50% with this configuration. We then developed a fabrication process on a GaSb substrate to demonstrate the feasibility of this configuration. We could demonstrate the fabrication of WGs in a butt-coupled geometry with a device mimicking a DL and with a  $\text{SiO}_2$  as small as  $\sim 0.9 \mu\text{m}$ . The next step would be to perform this process with a GaSb diode laser grown on a Si substrate and demonstrate high coupling efficiencies. In addition, this approach can be improved by further reducing the  $\text{SiO}_2$  bottom cladding layer thickness, resulting in an even narrower gap. It is therefore a very promising approach for achieving high coupling efficiencies. Finally, as with the approach discussed in chapter 3, the approaches investigated in this chapter can also be extended to other types of lasers and material systems.





# General conclusion and perspectives

Silicon photonics offers the potential to reduce the size, cost and power consumption of photonic integrated circuits. It has therefore been a major driver for much research in several application areas. This technology is highly demanded for mid-IR sensors, which are still based on discrete devices. The key step towards the realization of fully integrated, robust and low-cost mid-IR sensors is the demonstration of monolithically-integrated lasers on a Si PIC. To this end, my thesis focused on unlocking the process of the monolithic integration of lasers on a Si PIC with light coupling into passive Si-based waveguides.

In chapter 0, I presented the beginnings of the photonic integration and the benefits and potential solutions that silicon photonics can provide to PICs. The remaining challenges of this technology were then presented, such as the need to realize efficient laser sources on such a platform. I explained that III-Vs are the most efficient materials for light emission because most of them have a direct bandgap. For this reason, I reviewed the different approaches to integrating such lasers on Si platforms. The monolithic integration has proven to be the most promising approach for high-volume and cost-effective production of Si photonic chips. Afterwards, I presented the challenges of this approach, such as the poor crystal quality arising from the epitaxial growth of III-Vs on Si. I presented the impressive progress made by our team in terms of limiting the defect density in the laser structures, in particular the annihilation of antiphase domains, which led to the demonstration of high-performance lasers epitaxially grown on CMOS-compatible Si substrates. Still, threading dislocations are unavoidable and much research has been dedicated to reduce their density and understand their impact on these GaSb-based lasers. The next key step in the integration of lasers on Si is the optical coupling between the lasers and Si-based passive waveguides. To this aim, I introduced the main coupling configurations. I explained why the butt-coupling configuration is the most suitable strategy for the monolithic approach. I then focused the discussion on the importance of the mid-IR spectral range for various vital applications. I explained that GaSb-based lasers are capable of addressing this wavelength range and the importance of their monolithic

integration on Si for the realization of robust and low-cost mid-IR sensors. The objective of my thesis was then to integrate GaSb-based lasers on Si PICs.

In chapter 2, I investigated the effect of threading dislocations on the performance of GaSb-based diode lasers emitting at 2.3  $\mu\text{m}$ . To this end, two series of DLs with different numbers of QWs grown on their native GaSb and Si substrates were studied. I first described the laser heterostructures, followed by the MBE growth. Then, I presented each step of the laser process in detail, as well as the laser properties. As expected, DLs grown on native GaSb substrate exhibited better performance than DLs grown on Si. I then compared the laser properties to a theoretical model that I used to understand the origin of the laser performance degradation. I showed that the gain characteristics of the laser structures are affected by an increase in SRH recombinations within the QWs, resulting in an increase in the threshold current density. In addition, I showed that the optimal QW number depends on the total optical losses of the structure, and since the optimal QW number was the same for both DLs on GaSb and on Si, I concluded that threading dislocations affect the gain properties of the structures without introducing additional optical losses. These results allowed a better understanding of the effect of threading dislocations on the properties of the DLs structures. In addition, this investigation allowed to demonstrate record performance for GaSb DLs grown on Si.

In chapter 3, I demonstrated the integration of these GaSb-based DLs on a SI PIC with light coupled into passive SiN-based waveguides. First, I introduced the objective of this investigation, followed by the numerous challenges to be overcome. I then described the development of etched facets, required to monolithically integrate lasers on a PIC. I demonstrated etched-facet DLs with similar performance to cleaved-facet DLs. I then presented the fabrication details of the waveguides and the recessed areas dedicated to the growth of the DLs structures. I then showed the result of the MBE growth on the Si PIC, which was similar to that of plain Si substrates. However, polycrystal material is deposited on top of the WGs and between the DL/WG interface. I then demonstrated the polycrystal removal followed by the successful laser process on the Si PIC. I then presented the characterization of the DLs. They exhibited similar performance to discrete DLs grown on plain Si substrates. I showed that about  $\sim 10\%$  of the light was coupled into the SiN waveguides. Finally, FDTD simulations were presented to understand this coupling efficiency value. In particular, these simulations showed the drastic effect of the air gap between the DL and the WG on the coupling efficiency. All the challenges in this chapter have been overcome to achieve a major advance in the monolithic integration for low-cost and compact Si photonic chips.

In chapter 4, I explored alternative approaches to increasing the coupling efficiency. First, I presented FDTD simulations showing that the coupling efficiency can be increased by filling the gap between the laser and the waveguide with a higher index material, which reduces the refractive index contrast and thus the divergence of the laser beam. However, this would result in a reduction in the reflectivity of the laser facet and thus the laser performance. I then

showed the first test by filling the gap with PMMA, a polymer with a refractive index that seemed to offer a good compromise between coupling improvement and laser degradation. The coupling efficiency increased by an order of 4, while the laser threshold increased by only ~8%. I then presented the new optimizations in the laser process on the Si PIC which made it possible to reduce the air gap between the laser and the waveguide, which would increase the coupling efficiency. Finally, I showed further investigations using different fabrication approaches. One of these approaches is particularly promising, as it allows achieving a very narrow gap filled with SiO<sub>2</sub>. In addition, FDTD simulations predict a high coupling efficiency of 50% in this configuration. I then presented the development of the laser and waveguide fabrication process that allowed to demonstrate that a butt-coupling configuration with a gap as small as 0.9 μm of SiO<sub>2</sub> can be achieved. The next step will be the fabrication of real DLs to demonstrate high coupling efficiency. These results are very promising and open the way for further investigations to achieve high coupling efficiencies. In particular, if the WG bottom cladding is further reduced, the gap would also be reduced, allowing the coupling efficiency to be further increased.

The monolithic integration scenario of mid-IR sensors took a major step forward with the significant progress in III-V-on-Si epitaxial growth, in particular the elimination of APBs. Since then, two other challenges have been considered key to unlocking the monolithic integration approach: limiting the degradation of laser performance due to unavoidable threading dislocations and demonstrating the integration of mid-IR lasers on a Si PIC with light coupling into passive Si-based WGs. My PhD focused on these challenges and the results achieved were a major breakthrough towards fully monolithically integrated mid-IR sensors based on Si photonics. I carried out an important study to understand the effect of dislocations on DL performance. I also demonstrated a successful process and configuration for coupling light from monolithic lasers to passive waveguides. This achievement also provides a way to fabricate butt-coupled epitaxially integrated photodetectors, as the laser devices can be used as photodetectors under reverse bias. It also opens up the possibility of investigating the integration of other optical components to realize various optical functionalities on the same Si chip, such as an integrated sensing system based on SiN evanescent waveguides [148] or the integration of SiN electro-optic modulators. [25] I then proposed a new approach that showed great promise for achieving high levels of coupling efficiency, which would already fulfil one of the requirements of mid-IR spectroscopy. Note that the work presented in this thesis can readily be transferred to the integration of interband cascade lasers and quantum cascade lasers that appear to be relatively immune to dislocations, and thus offer a better lifetime than DLs grown on Si. Finally, yet important, the approaches proposed in this thesis can be extended to other material systems, making these results a major step forward towards silicon photonics integration for applications beyond optical sensing.



# 5 Appendix

## 5.1 Type-I quantum well diode lasers

A laser, which stands for Light Amplification by Stimulated Emission of Radiation, is a device that generates a coherent and intense beam of light through a process called Stimulated Emission. The working principle of a laser involves several key components and processes: the gain medium, the pumping system and the optical cavity. The gain medium is a material/region that is able to amplify the light through stimulated emission process. The gain material is excited to a higher energy state by an external energy source such as electrical current or optical absorption. And finally, an optical cavity allows a counter-reaction process. The interaction of these three elements is necessary to obtain a laser. We will see more in details the different processes.

In our case the gain medium is a semiconductor material. A semiconductor is a material that exhibits electrical conductivity between that of a conductor and an insulator. Its conductive properties depend on the conditions and they can be changed by introducing impurities in the crystal structure, by temperature or by the interaction with an external energy source. It has two main energy bands separated by the bandgap energy, the valence band (the highest energy band containing electrons at absolute zero temperature) and the conduction band (the lowest energy band that can accept electrons to carry electrical current) (Figure 108). And in fact, the interaction of the semiconductor material with photons gives rise to three main processes: absorption, spontaneous emission and stimulated emission. The absorption consists on an energy transfer from an incident photon to an electron in the valence band which will be recombined with a hole in the conduction band. The spontaneous emission corresponds to a transition between an electron in the conduction band and a hole in the valence by the emission of a photon that has random direction and phase. And the stimulated emission is based on an energy transfer between an incident photon and an electron in the conduction

band by the emission of a second photon that has a polarization and direction identical to the incident photon (coherent light).

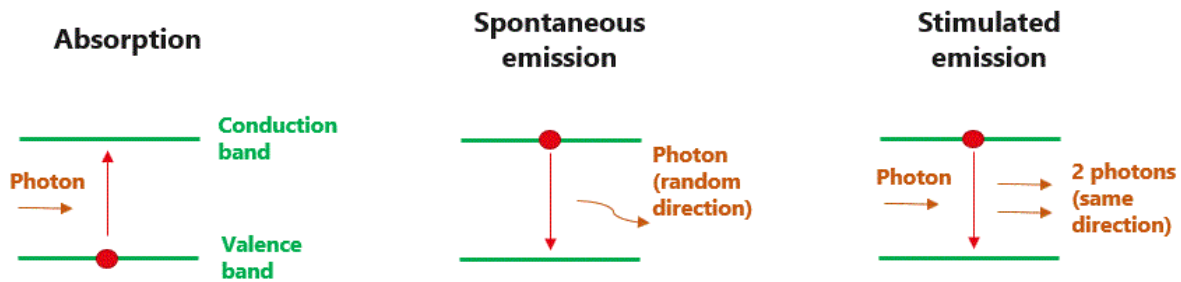


Figure 108. Different transition process of a semiconductor material interacting with a photon: absorption, spontaneous emission and stimulated emission.

This last process is the one responsible for the amplification. However, this process happens just under certain conditions. To have stimulated emission it is necessary to create a population inversion: the number of excited electrons in the conduction band is higher than the one of electrons in the valence band. The population inversion is achieved by electrical or optical pumping. In our case, we use electrical current to inject electrons in the conduction band. In addition, to lead to stimulated emission, an optical cavity, typically a Fabry-Perot cavity, is necessary to allow photons to travel back and forth across the gain material thanks to its mirrors (counter-reaction). In the gain media, the three processes occur: absorption, spontaneous emission and stimulated emission. At a certain injected current value, the stimulated emission dominates and the media will achieve the transparency. Above this value the system provides gain. The laser threshold is achieved when this gain overcomes the total optical losses: the intrinsic losses and the cavity losses.

$$Gain_{threshold} = total\ optical\ losses = intrinsic\ losses + cavity\ losses$$

Equation 17. The gain provided by the system is equal to the total optical losses: the laser threshold.

In my thesis, I mainly worked on quantum well diode lasers. The basic structure of a diode laser consists of a p-i-n junction. The p-i-n junction is formed by doping the semiconductor with impurities to create regions with excess positive charge (p-type) and excess negative charge (n-type). The active zone of the laser that is the intrinsic region (i) composed of quantum wells, is located in between the two doped regions. When a forward bias voltage is applied to the diode, electrons from the n-type region and holes from the p-type region will meet in the active zone and recombine. DLs operation is based on transitions within the quantum wells. A quantum well is obtained by sandwiching a thin layer of semiconductor material with a given energy bandgap between two wider barrier layers of a different semiconductor material with much higher bandgap energy. The difference of bandgap energy between the two types of semiconductors allows the confinement of carriers within the thin quantum well layer, where the transitions will occur. In a QW, the carriers are confined in one direction of the space because of the very thin layer (in the order of a few nm). This confinement of carriers in a well-

defined region leads to quantized energy levels forming a series of discrete energy states, as opposed to bulk materials. The wavelength of the emitted photons depends on the material and the quantum well width, leaving the possibility to engineer the structures to achieve the desired wavelength. There are different types of quantum well lasers. A type-I laser is based on transitions within the conduction and the valence band of the same material. On the other hand, in a type-II quantum well laser, the transitions occur from the conduction band of one material to the valence band of the neighbor material. This is important to understand because the sensitivity to some defects will not be the same for one structure as for the other. We are going to discuss the different types of recombinations in the next paragraph.

There exist three main types of recombination of an electron-hole pair: radiative recombination, Shockley-Read-Hall (SRH) recombination (non-radiative) and Auger recombination (non-radiative). Radiative recombination involves a direct recombination of an electron and a hole resulting in the emission of a photon. This is the type of recombination that is essential for lasers where the goal is to generate light. SRH recombination involves the interaction of carriers with impurities or defects in the crystal structure resulting in non-radiative recombination processes. This recombination is the one responsible of laser degradation when the TDD in the crystal is high, *e.g.*, after the III-V-on-Si growth. Finally, Auger recombination involves the recombination of an electron-hole pair resulting in the transfer of energy to another carrier instead of emitting a photon. The non-radiative processes of SRH involves defects located in the bandgap of the QWs. The carrier confined in the QW will lose energy by relaxing first in the defect energy level and then in the valence band. Type-I diode lasers are therefore very sensitive to these defects as the transitions occurs within the QW layers

## 5.2 Process techniques

In this section, I will describe briefly the different techniques used to fabricate the lasers.

The laser process has been done using ultraviolet (UV) photolithography for pattern transferring, inductively coupled plasma (ICP) technique for etching the materials, plasma-enhanced chemical vapor deposition (PECVD) for deposition of dielectric materials and electron beam (e-beam) evaporation for deposition of metallic layers. These techniques are standard techniques widely used in the microelectronics industry and research laboratories.

### 5.2.1 UV photolithography

The goal of the UV photolithography is to transfer a pre-defined pattern from a mask to the sample by using a photosensitive material. The photosensitive material is called resist and it is typically a polymer. The pattern defined on the mask has glass regions which are transparent to UV light and chromium regions which are not. This will allow to expose the resist to the UV light on some areas and protect it on other areas, creating a pattern on the resist. The different steps of the UV photolithography are:

- Spin coating: the resist is applied to the sample and it is spun at high speed, spreading the resist evenly over the surface of the sample. The thickness of the resist depends on its viscosity and the rotation speed. In fact, resists have a solvent which keeps them in a liquid state and becomes easy to spin them over the surface of the sample. The resist is then baked to evaporate part of this solvent.



Figure 109. Sketch of the resist spread evenly over the surface of the sample after spin coating.

- Exposure: the sample is brought into contact with the mask. The UV light passes through the transparent regions of the mask and exposes the underlying resist. This exposure causes a chemical reaction in the resist, altering its solubility properties. The power of the UV lamp and the exposure time are essential parameters to ensure the exposure of the total thickness of the resist.

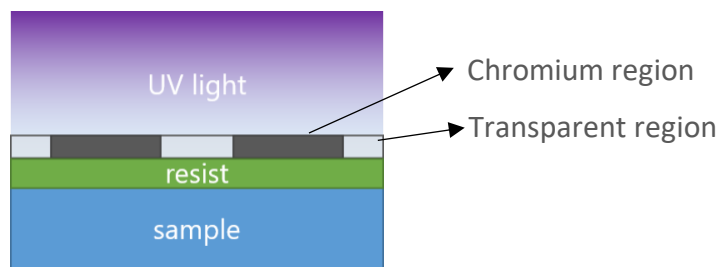


Figure 110. Sketch of the sample brought into contact with the mask and exposed to UV light.

- Development: the sample is dipped into a solution to develop the pattern. This solution will selectively remove either the exposed or unexposed regions of the resist, depending on the type of the resist. This step reveals the desired pattern on the sample surface. In the case of the positive resist, the UV light changes its chemical structure and the developer dissolve the exposed regions while the unexposed regions remain on the sample. In the case of the negative resist, it is initially soluble in the developer and when exposed to UV light, cross-linking reaction of the polymer molecules occurs. As a result, the exposed regions remain on the sample and unexposed regions are dissolved by the developer.

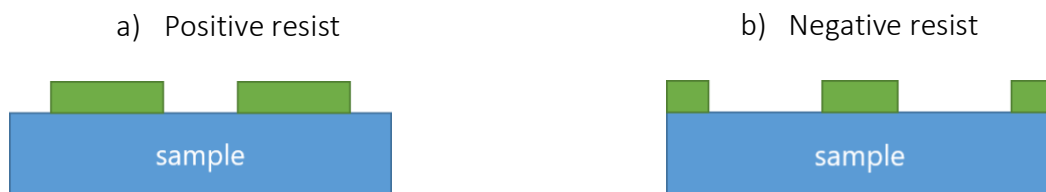


Figure 111. Sketch of the sample after development. a) In the case of positive resist. b) In the case of negative resist.



As it is shown in Figure 111, the pattern is now transferred from the mask to the resist (or inversely transferred if the negative resist is used) for later processing, *e.g.*, etching, material deposition, ion implantation. An example of the final sample if the later processing is an etching is shown in the figure below (Figure 112).



Figure 112. Sketch of the sample after etching. a) In the case of positive resist. b) In the case of negative resist.

There are additional steps and parameters during the photolithography process that are used depending on the resist requirements and process. There are different contact modes during exposure: soft contact, hard contact and vacuum contact. The difference between them is the applied pressure (from low to high, respectively) which changes the resolution of the patterning. Low pressure is used for low resolution and high pressure for high resolution. The exposure time is also an important parameter as it changes the resist profile, especially for negative resist. Post-exposure bake is typically performed after the exposure of a negative resist to complete the cross-linking reaction. Hard bake is used after the development in order to change the resist profile. All these parameters are very important to achieve the desired etching or deposition profiles and were carefully used during my thesis.

### 5.2.2 ICP etching

Generally, dry etching techniques are more repeatable and anisotropic than wet etching techniques which make them preferable for some process. During my thesis I mainly used ICP which is a dry etching technique for precise and controlled removal of material. It is based on the creation of a plasma formed by applying radiofrequency (RF) power to a coil on a low-pressure environment and where on one hand, the accelerated molecules impact the surface of the sample, resulting in physical etching. On the other hand, molecules also react with the sample, resulting in chemical etching. The dominance of one etching mechanism over the other depends on the gas composition. Some molecules tend to react with the materials while others tend to bombard the surface. It is, therefore, important to choose the right recipe depending on the desired etching mechanism.[125] This technique can provide anisotropic profiles when the physical etching dominates which was essential for the work carried out in my thesis. The other parameters that influence the etch rate and profile are the gas flows, ICP and RF powers, temperature and chamber pressure.

### 5.2.3 PECVD

PECVD is a thin film deposition technique used for dielectric deposition. It combines the principles of chemical vapor deposition (CVD) with the use of plasma to enhance the deposition process. It is based on a chemical reaction of reactive species from the plasma with the precursor gas near the surface of the sample. Chemical reactions occur, resulting in the

deposition of a thin film on the surface. The film grows layer by layer as the reactive species continuously react with the precursor gas. Various parameters such as gas flow rates, chamber pressure, RF power and temperature, are carefully controlled to achieve the desired deposition rate and uniformity.

### 5.2.4 Electron beam evaporation

The electron beam evaporation technique uses an electron beam to vaporize a metal target source, allowing controlled deposition of metal atoms onto a sample. The process also takes place in a high-vacuum environment to minimize contamination and ensure precise control of the film thickness and uniformity. The accelerated electrons with high energy strike the target causing rapid heating and vaporization of the metal atoms. The metal atoms are directed to the sample and deposited on the surface. The deposition rate depends on the electron beam power and the deposited film thickness can be measured in situ by a quartz crystal monitor.[149]

Usually, metal depositions are done using a lift-off technique. It involves the deposition of the metal layer on the sample and subsequently removing the unwanted portions on the material by lifting the resist that was protecting these regions, leaving behind the desired pattern. The lifting is typically done by an acetone bath. A negative resist is typically used because of the resist profile, which facilitates the later lift-off of the undesired portions of material. In Figure 113, the results of this technique depending on the resist profile are shown.

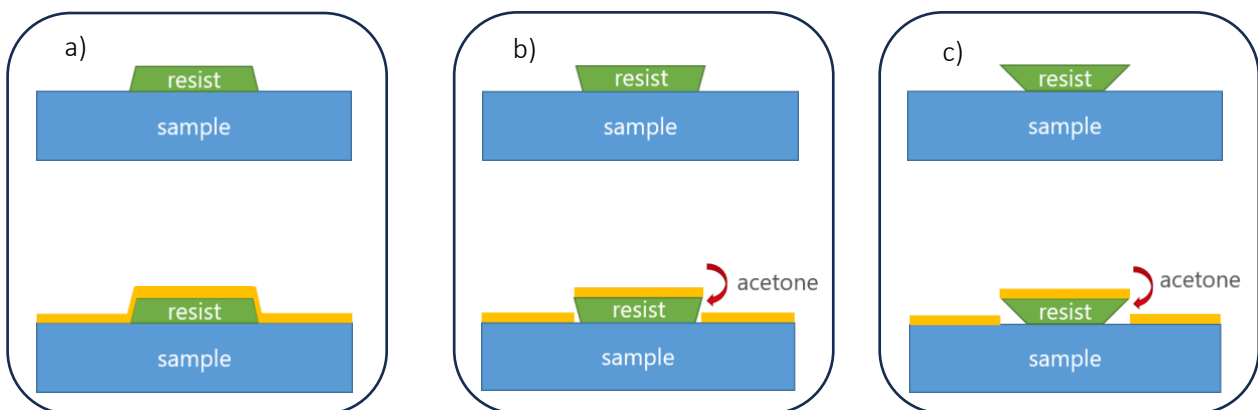


Figure 113. Sketch of a lift-off technique using electron beam evaporation technique for metal deposition with a) a positive resist profile, b) a negative resist profile, and c) an accentuated negative resist profile.

The positive resist (Figure 113.a) gives a profile with a positive slope which is not adapted for a lift-off. The metal is deposited as a continuous layer and is completely covering the sidewall of the resist which makes the lift-off impossible because the acetone can't reach the resist. On the other hand, the negative profile (Figure 113.b) will leave a discontinuity of the layer making it possible for the acetone to reach and lift the resist together with the undesired material. The negative resist profile can be accentuated (Figure 113.c) by decreasing the exposure time during the photolithography which facilitates the lift-off.

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# List of publications

## Journal articles

- Kinjalk, K., Gilbert, A., Remis, A., Loghmari, Z., Cerutti, L., Patriarche, G., Bahriz, M., Teissier, R., Baranov, A.N., Rodriguez, J.-B., & Tournié, E. (2022). Quantum cascade lasers monolithically integrated on germanium. *Optics Express*, 30(25), 45259-45266. <https://doi.org/10.1364/OE.472473>

- Remis, A., Monge Bartolomé, L., Boissier, G., Waguaf, M., Rodriguez, J.-B., Cerutti, L., & Tournié, E. (2023). Effect of dislocations on the performance of GaSb-based diode lasers grown on silicon. *Journal of Applied Physics*, 133, 093103. <https://doi.org/10.1063/5.0135606>
- Remis, A., Monge Bartolomé, L., Paparella, M., Gilbert, A., Boissier, G., Grande, M., Blake, A., O’Faolain, L., Cerutti, L., Rodriguez, J.-B., & Tournié, E. (2023). Unlocking the monolithic integration scenario: optical coupling between GaSb diode lasers epitaxially grown on patterned Si substrates and passive SiN waveguides. *Light: Science & Applications*, 12:150. <https://doi.org/10.1038/s41377-023-01185-4>.

## Conferences

- Andres Remis, Laura Monge Bartolomé, Guilhem Boissier, Jean-Baptiste Rodriguez, Laurent Cerutti, and Eric Tournié. “Effect of quantum-well number on the performance of GaSb-based type-I laser diodes grown on silicon” (Oral Presentation). SPIE Photonics West, “Novel In-plane Semiconductor Lasers XXI”, 2022, San Francisco, USA.
- Andres Remis, Daniel Andrés Diaz-Thomas, Laura Monge Bartolomé, Marta Rio Calvo, Audrey Gilbert, Guilhem Boissier, Alexei Baranov, Jean-Baptiste Rodriguez, Laurent Cerutti, and Eric Tournié. “Mid-Infrared Sb-based interband lasers grown on on-axis Si (001) substrates” (Oral Presentation). CSW conference, 2022, Ann Arbor, USA.
- Kumar Kinjalk, Audrey Gilbert, Andres Remis, Zeineb Loghmari, Laurent Cerutti, Michael Bahriz, Roland Teissier, Alexei Baranov, Jean-Baptiste Rodriguez, and Eric Tournié. “Monolithic integration of InAs-based quantum cascade lasers on germanium” (Oral Presentation). SPIE Photonics West, “Silicon Photonics XVIII”, 2023, San Francisco, USA.
- Andres Remis, Michele Paparella, Audrey Gilbert, Laura Monge Bartolomé, Guilhem Boissier, Marco Grande, Laurent Cerutti, Alan Blake, Liam O’Faolain, Jean-Baptiste Rodriguez, and Eric Tournié. “Butt-coupling of semiconductor lasers and passive waveguides by direct epitaxy on patterned Si photonic wafers” (Oral Presentation). CSW conference, 2023, Jeju Island, Korea.
- Michele Paparella, Andres Remis, Laura Monge Bartolomé, Jean-Baptiste Rodriguez, Laurent Cerutti, Marco Grande, Liam O’Faolain, and Eric Tournié. “A Numerical and Experimental Butt-coupling Analysis of GaSb Diode Laser Grown on Silicon Photonic Integrated Circuit” (Oral Presentation). CLEO Conference 2023, Munich, Germany.

## Invited conferences

- Andres Remis, Michele Paparella, Laura Monge Bartolomé, Audrey Gilbert, Marta Rio Calvo, Guilhem Boissier, Marco Grande, Laurent Cerutti, Liam O’Faolain, Jean-Baptiste Rodriguez, and Eric Tournié. “Butt-coupled mid-IR diode lasers grown on patterned Si photonic wafers”. SPIE Photonics West, “Silicon Photonics XVIII”, 2023, San Francisco, USA.
- Eric Tournié, Andres Remis, Michele Paparella, Audrey Gilbert, Laura Monge Bartolomé, Marta Rio Calvo, Daniel Andrés Diaz Thomas, Zeineb Loghmari, Laurent Cerutti, Alexei Baranov, Roland Teissier, and Jean-Baptiste Rodriguez. “Mid-IR lasers epitaxially integrated onto Si”. 45<sup>th</sup> Freiburg Infrared Colloquium, 2023, Freiburg, Germany.
- Andres Remis, Michele Paparella, Laura Monge Bartolomé, Audrey Gilbert, Guilhem Boissier, Marco Grande, Alan Blake, Liam O’Faolain, Laurent Cerutti, Jean-Baptiste Rodriguez, and Eric Tournié. “Monolithic Integration of GaSb Diode Lasers on a Silicon Photonic Circuit” (Invited Speaker). CLEO Conference 2023, Munich, Germany.
- Eric Tournié, Michele Paparella, Andres Remis, Audrey Gilbert, Marta Rio Calvo, Laura Monge Bartolomé, Guilhem Boissier, Marco Grande, Laurent Cerutti, Alan Blake, Liam O’Faolain, and Jean-Baptiste Rodriguez. “Mid-IR lasers epitaxially integrated on Si photonic circuits”. International Nano-Optoelectronics Workshop (iNOW 2023), 2023, Wurzburg, Germany.
- Eric Tournié, Jean-Baptiste Rodriguez, Laurent Cerutti, Audrey Gilbert, Milan Silvestre, Maeva Fagot, Marta Rio Calvo, Andres Remis, Michele Paparella, Guilhem Boissier, Kumar Kinjalk, Zeineb Loghmari, Roland Teissier, and Alexei Baranov. “Epitaxial integration of mid-infrared III-V devices on group-IV substrates”. E-MRS Fall Meeting, Symposium A: “Integration of advanced materials on Silicon: from classical to neuromorphic and quantum applications”, 2023, Warsaw, Poland.
- Eric Tournié, Andres Remis, Michele Paparella, Audrey Gilbert, Marta Rio Calvo, Laura Monge Bartolomé, Guilhem Boissier, Marco Grande, Laurent Cerutti, Alan Blake, Liam O’Faolain, and Jean-Baptiste Rodriguez. “Integration of Mid-IR lasers and Si photonic circuits”. 46<sup>th</sup> European Semiconductor Laser Workshop, 2023, Glasgow, U.K.



## Abstract

Silicon (Si) photonics has emerged as one of the most promising technologies for the realization of ultra-dense photonic chips thanks to the mature Si industry, the large wafer size and the optical properties of Si and related materials. One of the major remaining challenges is the integration of high-performance light sources on Si. In particular, III-V semiconductor lasers are very efficient and their monolithic integration on Si, *i.e.* direct integration via epitaxy, is considered the most promising route to low-cost and large-scale fabrication of Si photonic chips. Among the various applications of Si photonics, optical sensing in the mid-IR is in high demand for societal, environmental or medical applications, among others. GaSb-based lasers have emerged as a technology capable of covering the mid-IR wavelength range. Therefore, the objective of my thesis is to integrate GaSb-based diode lasers on Si photonic integrated circuits (PICs). To this aim, I first investigated the degradation of laser performance caused by threading dislocations arising from the III-V-on-Si epitaxial growth. I then demonstrated the fabrication of these lasers on a Si PIC with similar performance to that of discrete lasers on Si. In addition, light coupling between the lasers and SiN-based waveguides was demonstrated. Finally, I investigated alternative approaches to increase the coupling efficiency. I developed the fabrication process of a new promising approach which paves the way for further investigations aimed at achieving high coupling efficiencies. Altogether, these results represent a significant step towards the monolithic integration of lasers on Si PICs for cost-effective and compact mid-IR sensors.

## Résumé

La photonique silicium (Si) est apparue comme l'une des technologies les plus prometteuses pour réaliser des puces photoniques ultra-denses, grâce à la maturité de l'industrie du Si, à la grande taille des wafers et aux propriétés optiques du Si et des matériaux connexes. L'un des principaux défis qui restent à relever est l'intégration de sources lasers à haute performance sur Si. En particulier, les lasers à semi-conducteurs III-V sont très efficaces et leur intégration monolithique sur Si, c'est-à-dire l'intégration directe par épitaxie, est considérée comme la voie la plus prometteuse vers la fabrication de puces photoniques Si à faible coût et à grande échelle. Parmi les diverses applications de la photonique Si, la détection optique dans le moyen infrarouge est très demandée pour des applications sociétales, environnementales ou médicales, entre autres. Les lasers à base de GaSb sont apparus comme une technologie capable de couvrir la gamme du moyen infrarouge. L'objectif de ma thèse est l'intégration diode lasers à base de GaSb sur des circuits photoniques intégrés Si (PIC). A cette fin, j'ai d'abord étudié la dégradation de la performance du laser causée par des dislocations provenant de la croissance épitaxiale III-V-sur-Si. Ensuite, j'ai démontré la fabrication de ces lasers sur un PIC Si avec des performances similaires à celles des lasers discrets sur Si. En outre, le couplage de lumière entre les lasers et des guides d'ondes à base de SiN a été démontré. Enfin, j'ai étudié des nouvelles approches pour augmenter l'efficacité du couplage. J'ai développé le process de fabrication d'une nouvelle approche prometteuse qui ouvre la voie à d'autres recherches visant à atteindre des efficacités de couplage élevées. Dans l'ensemble, ces résultats représentent une étape importante vers l'intégration monolithique de lasers sur des PICs Si pour des capteurs dans le moyen infrarouge compacts et économiques.