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# A 5G mmW bidirectional integrated transmitter in a hybrid and digital beamforming system

Lucien Paquien

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Par Lucien PAQUIEN

**Transmetteur intégré bidirectionnel dédié à la 5G mmW dans un  
système de formation de faisceaux hybride et numérique**

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**Titre :** Transmetteur intégré bidirectionnel dédié à la 5G mmW dans un système de formation de faisceaux hybride et numérique

**Mots clefs :** 5G, 22nm CMOS FD-SOI, Emetteur-récepteur, Bidirectionnel, Formation de faisceaux

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**Résumé :** La demande croissante en débit pour les télécommunications mobiles a conduit à l'utilisation de systèmes à formation de faisceaux afin de limiter notamment l'impact des pertes de propagation dans l'espace libre (FSPL) sur le bilan de liaison, dues à l'élévation de la fréquence d'opération. Afin de pouvoir orienter un faisceau directif concentrant la majorité du gain d'un réseau d'antennes en direction d'un utilisateur donné, un nombre important de circuits radiofréquences intégrés (RFFE) est nécessaire.

De manière conventionnelle, les RFFE 5G sont généralement constitués d'un amplificateur à faible bruit (LNA), et d'un amplificateur de puissance (PA). Ces derniers sont physiquement dissociés, et alternativement adressés avec un élément commuté, afin de fonctionner en duplexage par répartition dans le temps (TDD). Dans ce cas, non seulement l'élément commuté implique des pertes et un besoin en surface silicium non négligeable, mais aussi les RFFE ne sont utilisés que la moitié du temps (dû au TDD). Aussi, cet important espace silicium requis est ensuite à multiplier par le nombre d'éléments que compose le système à formation de faisceau. De plus, l'espacement entre chaque antenne constituant le réseau d'antennes étant proportionnel à la longueur d'onde, ce dernier pourrait donc fonctionner à des fréquences de fonctionnement plus élevées si les RFFE sont miniaturisés. Dans ce travail, une solution permettant l'élimination du besoin d'un élément commuté, ainsi qu'à la fusion des LNA et PA est proposé, induisant une forte réduction de la surface silicium requise, utilisant la technologie GF 22nm CMOS FD-SOI. Bien que la conception de fonctions millimétriques (mmW) soit abordé, l'aspect conversion de fréquence ainsi que l'étude de fonctions de bande de base sera également discuté, avec notamment la conception d'un mixer passif RF, de deux filtres passe-bas RC actifs reconfigurables d'ordre 2 et 4, d'un amplificateur à gain variable (VGA), d'un bloc analogique tampon  $50\Omega$ , d'un commutateur bipolaire à deux directions (DPDT), ainsi qu'une chaîne de génération de signaux en quadrature, grâce à l'association d'un coupleur hybride (HCPLR), et d'un oscillateur local (LO) externe hors-puce. Le système complet sera caractérisé pour démontrer l'intérêt de ces structures en termes de performances et de surface silicium requise, et des pistes d'améliorations seront énumérées.

**Title:** A 5G mmW bidirectional integrated transmitter in a hybrid and digital beamforming system

**Key words:** 5G, 22nm CMOS FD-SOI, Transceiver, Bidirectional, Beamforming

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**Abstract:** The increasing demand for data rate for mobile telecommunications has led to the use of beamforming systems in order to notably limit the impact of free space propagation losses (FSPL) over the link budget, due to the elevation of the operating frequency. In order to be able to direct a directional beam concentrating the majority of the gain of an antenna array towards a given user, a large number of integrated radio frequency front-ends (RFFE) is necessary.

Conventionally, 5G RFFEs generally consist of a low noise amplifier (LNA), and a power amplifier (PA). The latter are physically dissociated, and are alternatively addressed using a commuted element, in order to operate in time division duplexing (TDD). In this case, not only does the switched element involve losses and a significant silicon surface requirement, but also the RFFEs are only used half the time (due to TDD). Also, this large silicon area required must then be multiplied by the number of elements that constitutes the beamforming system. In addition, the spacing between each antenna constituting the antenna array being proportional to the wavelength, the latter could therefore reach higher operating frequencies if the RFFEs are miniaturized. In this work, a solution allowing the elimination of the need for a commuted element, as well as the merging of the LNA and PA is proposed, inducing a strong reduction in the silicon surface area required for the same operation than conventional architectures, using the GF 22nm CMOS FD-SOI technology. Although the design of millimeter functions (mmW) will be discussed, the frequency conversion aspect as well as the study of baseband functions will also be covered, including the design of a RF passive mixer, two reconfigurable second- and fourth-order active-RC low-pass filters, a variable gain amplifier (VGA), a 50 $\Omega$  analog buffer, a double pole double throw (DPDT) switch, as well as a generation chain of quadrature signals, done from the combination of a hybrid coupler (HCPLR), and an external off-chip local oscillator (LO). The complete system will be simulated to demonstrate the relevancy of these structures regarding performances and required silicon surface, and axis for improvement will also be listed.

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# LIST OF ABBREVIATIONS

<b>1G</b>	First Generation Mobile Communication
<b>2G</b>	Second Generation Mobile Communication
<b>3G</b>	Third Generation Mobile Communication
<b>4G</b>	Fourth Generation Mobile Communication
<b>5G</b>	Fifth Generation Mobile Communication
<b>5G NR</b>	5G New Radio
<b>6G</b>	Sixth Generation Mobile Communication
<b>ACLR</b>	Adjacent Channel Leakage Ratio
<b>ADC</b>	Analog to Digital Converter
<b>AM/AM</b>	Amplitude Modulation to Amplitude Modulation
<b>AM/PM</b>	Amplitude Modulation to Phase Modulation
<b>APMOM</b>	Alternative Polarity Metal-Oxide-Metal
<b>BB</b>	Baseband
<b>BBBA</b>	Bidirectional Baseband Amplifier
<b>BEO</b>	Back-End Of Line
<b>BER</b>	Bit Error Rate
<b>BO</b>	Back-Off
<b>BS</b>	Base Station
<b>BW</b>	Bandwidth
<b>CDMA</b>	Code Division Multiple Access
<b>CG</b>	Conversion gain
<b>CM</b>	Common Mode
<b>CMFB</b>	Common Mode Feedback
<b>CMOS</b>	Complementary Metal Oxide Semiconductor
<b>CMRR</b>	Common Mode Rejection Ratio
<b>CMSL</b>	Common Mode Stabilization
<b>DAC</b>	Digital to Analog Converter
<b>DC</b>	Direct Current
<b>DCOC</b>	DC Cancellation loop
<b>DPDT</b>	Double Pole Double Throw
<b>DSP</b>	Digital Signal Processing
<b>EVM</b>	Error Vector Magnitude
<b>FDD</b>	Frequency Division Duplexing
<b>FD-SOI</b>	Fully Depleted Silicon-On-Insulator
<b>FE</b>	Front-End

<b>FET</b>	Field-Effect Transistor
<b>FSPL</b>	Free Space Loss
<b>GF</b>	GlobalFoundries
<b>GSG</b>	Ground-Signal-Ground
<b>GSGSG</b>	Ground-Signal-Ground-Signal-Ground
<b>GSM</b>	Global System for Mobile Communications
<b>HB</b>	Harmonic Balance
<b>HCPLR</b>	Hybrid Coupler
<b>I/O</b>	Input/Output
<b>ICP1</b>	Input 1 dB-Compression Point
<b>ID</b>	Inner Diameter
<b>IIP3</b>	Third-Order Input Intercept Point
<b>IMD3</b>	Two-tone Third-Order Intermodulation Distortion
<b>IoT</b>	Internet Of Things
<b>LAIR</b>	Laboratory of Integrated RF Architectures
<b>LNA</b>	Low Noise Amplifier
<b>LO</b>	Local Oscillator
<b>LOS</b>	Line Of Sight
<b>LPF</b>	Low-pass Filter
<b>LSB</b>	Lower Sideband
<b>LVT</b>	Low Voltage Threshold
<b>MIMO</b>	Multiple-Input Multiple-Output
<b>mmW</b>	Millimeter-Wave
<b>MOSFET</b>	Metal-Oxide-Semiconductor Field-Effect Transistor
<b>NF</b>	Noise Figure
<b>NMOS</b>	N-type MOS
<b>NR</b>	New Radio
<b>OBUE</b>	Operating Band Unwanted Emission
<b>OCP1</b>	Output 1 dB-Compression Point
<b>OFDMA</b>	Orthogonal Frequency Division Multiple Access
<b>OIP3</b>	Output Third Order Intercept Point
<b>OOB</b>	Out-Of-Band
<b>OTA</b>	Operational Transconductance Amplifier
<b>PA</b>	Power Amplifier
<b>PAE</b>	Power-Added Efficiency
<b>PDK</b>	Process Design Kit
<b>PD-SOI</b>	Partially Depleted Silicon-On-Insulator
<b>PMOS</b>	P-type MOS
<b>PMU</b>	Power Management Unit



<b>PPF</b>	Polyphase Filter
<b>PSD</b>	Power Spectral Density
<b>PSS</b>	Periodic Steady-State
<b>QAM</b>	Quadrature Amplitude Modulation
<b>QPSK</b>	Quadrature Phase-Shift Keying
<b>RF</b>	Radio Frequency
<b>RFFE</b>	RF Front-End
<b>RVT</b>	Regular Voltage Threshold
<b>RX</b>	Receiver
<b>SNR</b>	Signal-to-Noise Ratio
<b>SP</b>	S-Parameter
<b>SPDT</b>	Single Pole Double Throw
<b>SPEL</b>	Spurious Emission Limit
<b>SPI</b>	Serial Peripheral Interface
<b>SRF</b>	Self-Resonant Frequency
<b>SSB</b>	Single-Sideband
<b>SX</b>	Frequency Synthesis
<b>TCP/IP</b>	Transmission Control Protocol/Internet Protocol
<b>TDD</b>	Time Division Duplexing
<b>TDMA</b>	Time Division Multiple Access
<b>TIA</b>	Transimpedance Amplifier
<b>TL</b>	Transmission Line
<b>TRX</b>	Transceiver
<b>TX</b>	Emitter
<b>UHD</b>	Ultra-High Definition
<b>USB</b>	Upper Sideband
<b>VGA</b>	Variable Gain Amplifier
<b>VNA</b>	Vector Network Analyzer

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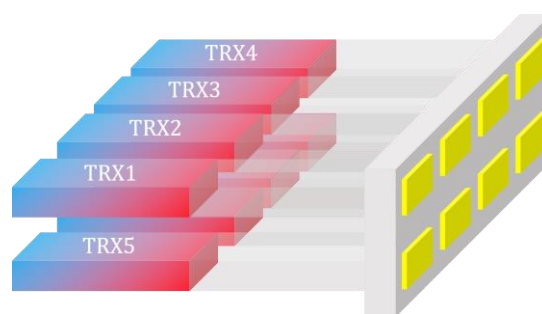
# GENERAL INTRODUCTION

## 1.1 THESIS POSITIONING

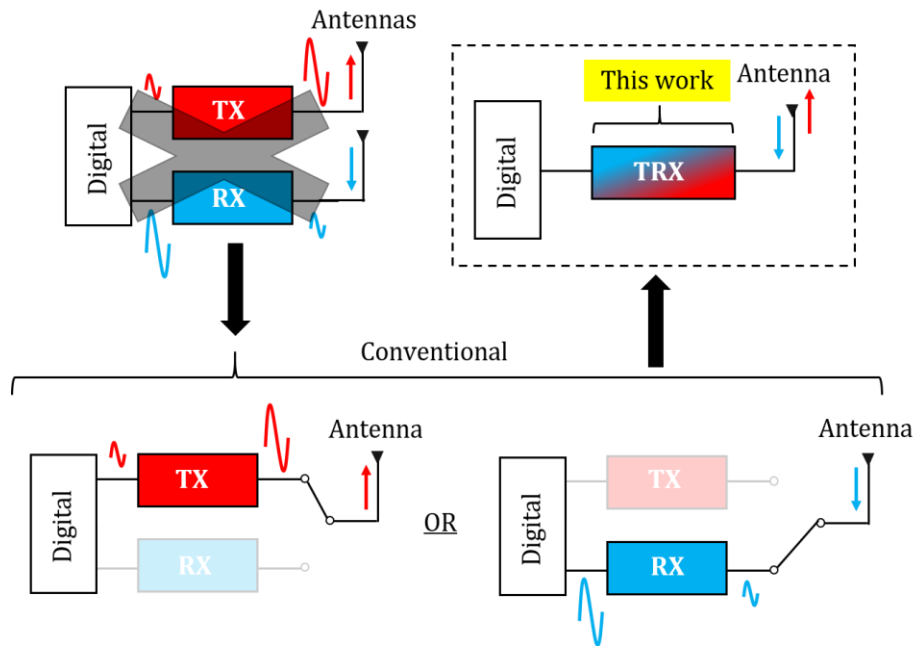
This thesis is based on the study and design of a 5G telecommunication system. In this 3-years PhD thesis, a complete bidirectional transceiver was designed for massive-MIMO 5G FR2 applications, whose organization plan is described in the next sections. An ongoing project was being carried out in parallel of the thesis work inside the foster laboratory (*Laboratory of integrated radio-frequency architectures - LAIR*) in Grenoble, France, with the aim of designing a transceiver intended to provide a 5G MIMO access point inside an aircraft, allowing on-flight 5G services by taking benefit from an expanding satellites constellation. Short-range applications are relevant in this case considering the small volume of the cabin: a good signal-to-noise ratio (SNR) can therefore be maintained, even for demanding complex modulations.

The project system requirements were evaluated from the thesis foster lab technical team, and was followed by the accomplishment of this present work. The originality of our design is the proposal of an innovative bidirectional system. A bidirectional system is described as such the input and the output can play alternatively mutual roles.

Ordinary, in order to limit the number of antennas composing a multi-elements system (illustrated in Figure 1), a commuted component (such as a switch) addresses the TX front-end to the antenna when operating in transmit mode (TX), and addresses the reception (RX) front-



**Figure 1: Simplistic illustration of the DBF structure where the TRX paths are associated with a 2x4 antenna array**



**Figure 2: Independent antenna used for the TX and RX (top left), TRX antenna reusing (bottom), and our work over a bidirectional TRX front-end**

end when operating in receive mode, in order to reuse it. This concept is illustrated Figure 2. This time-dependent operating mode is called TDD. In TDD, both RX and TX are periodically enabled in time, with the goal of lowering potential impact over one another as much as possible.

Conventionally in typical MIMO-based transceivers architectures, both TX and RX chains are physically separated into different chip locations, as in Figure 3, to facilitate the design of both chains by making the design almost independents from one another. Almost, because the switching device is not transparent in practice. Then, dedicated matching networks allows to set appropriate impedances to the RF front-ends. However, separated matching networks including large inductors (mostly) will lead to a significant required silicon area. Indeed, because of the TDD, the lumped components are only used half the time in this case.

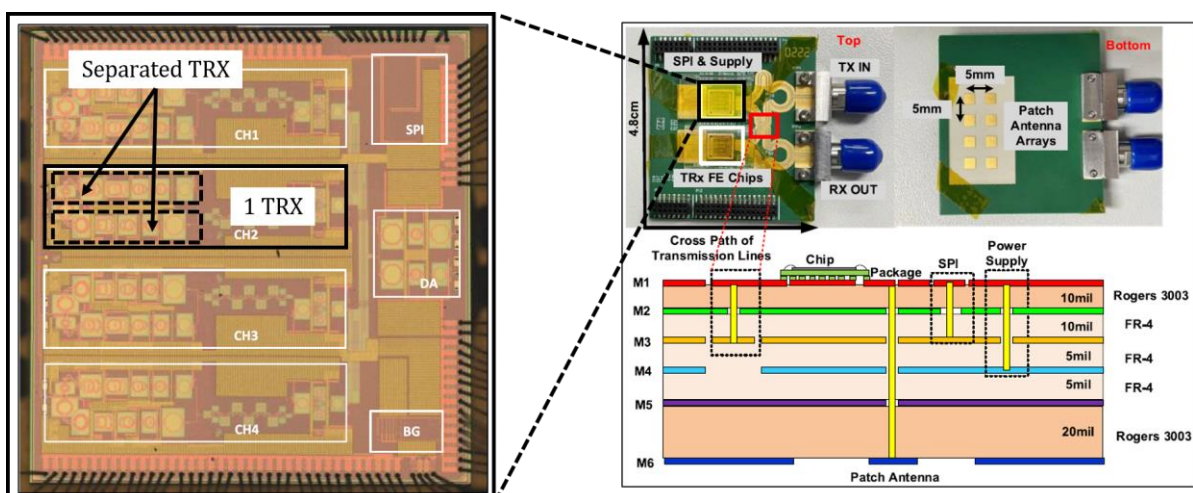
Moreover, RF switched components will lead to a systematic deterioration of both TX power efficiency and RX noise. It also implies the incorporations of extra matching networks, necessitating non-negligible extra silicon surfaces.

The bidirectional architectures will remove the need for lossy switching components as well as using efficiently the silicon since matching networks are fully reused in both RX and TX mode. In theory, the required silicon will be reduced by a close to a factor of two.

In order to operate, massive-MIMO systems need a large number of TRX paths, this duplication allows beamsteering. Hence, every saving made over one building block is to be multiplied by at least the number of paths, in the case of a digital beamforming architecture, which results in significant area surfaces as in Figure 3. For instance, in the case of a digital beamforming architecture (DBF) including  $N$  paths,  $N$  RF front-ends are required. Similarly, based on the I/Q technique,  $N$  paths will induce  $2N$  baseband building blocks.

On the one hand, reducing the size of transceiver will increase the capacity of the system and provide an effective solution for compact and low-cost applications. On the other hand, it will also potentially allow the use of smaller antenna array pattern whose individual spacing is being proportional to the wavelength. Smaller arrays could be potentially being employed at even higher frequencies than conventional topologies. In a technological situation where 6G is already being developed at the time this manuscript is written, this solution appears to be meaningful.

At the heart of all considerations, trade-offs will have to be made all across this work, because of the matching network reusing concept. Of course, a great deal of differences exists between the design of an emitter and a receiver. The most telling example of these design differences would be the co-matching between the power matching for the PA, done using a load pull analysis, and the noise matching for the LNA, done by small a signal analysis. Trade-offs will need to be found, and if possible, at the lower performance costs.



**Figure 3: Die photograph of a four-element transceiver in 65nm CMOS (left) and the six-layer PCB in the case of an eight-elements (2x4) phased array module (right) with annotations [1]**

Finally, the high operating frequency will provide a high data rate for short-range applications taking benefit of the performances of the GF 22nm CMOS FD-SOI (or 22FDX) technology at mmW frequencies.

## 1.2 THESIS OBJECTIVES

To sum up, the key backbones challenges of this work can be listed as bellow

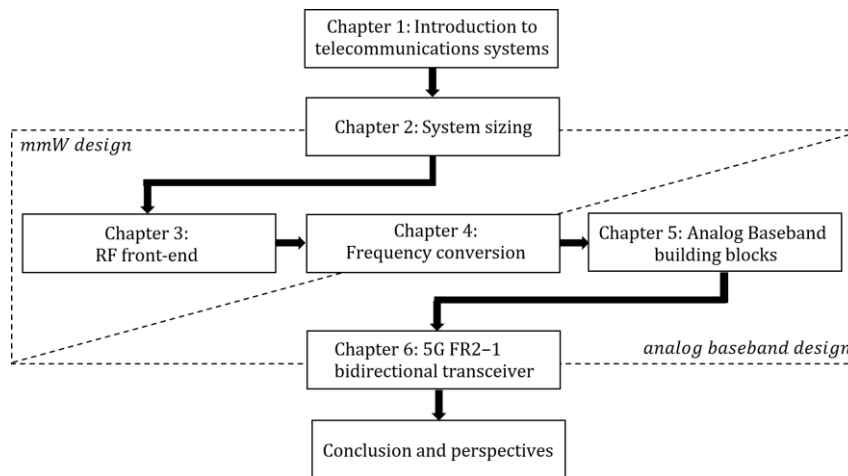
- Characterizing and using adequately the 22FDX technology
- Identifying the key building blocks at the system-level transceiver design in both analog baseband and mmW domains
- Finding trade-offs (and if possible new architectures) to ensure appropriate a bilateral operating mode
- Layout (general rules and electro-migration verifications) of all the building blocks
- Experimental measurement characterization of a full transceiver in a lab

## 1.3 THESIS ORGANIZATION

The chapter-by-chapter organization of this manuscript can be described as follows. Chapter one provides a historical timeline of mobile technological improvements. Features, employed modulations, and also some economic considerations of the 5G are exhibited. The distinction between the various types of 5G is then made, in order to focus in a specific mmW frequency range. Multiples multiplexing and duplexing techniques are presented in order to fully understand the surroundings of our system in a massive-MIMO environment. The beamsteering and beamforming concept using various architectures are presented and compared.

In chapter two, the project beyond this work is presented. The block diagram of the full system is presented, and a system overview was made to set expected performances of each chosen building blocks in order to respect specifications imposed by the project. Then, the PDK components (passive and active) used in the design are introduced.

In chapter three, the mmW part of the work will be described through the RF front-end usually composed of a PA for the TX mode and one LNA for the RX mode. The concept of bidirectionality will be used to design a bidirectional PA-LNA. Two tape-outs will be described.



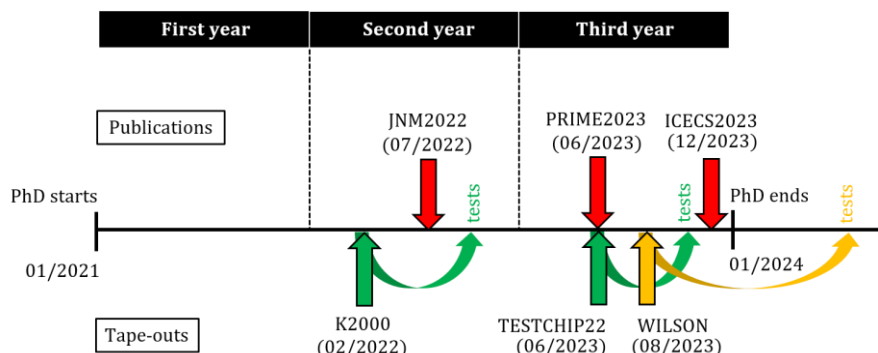
**Figure 4: Thesis chapter-by-chapter organization**

In chapter four, the frequency generation will be studied. It is composed of one part over the design of the mixer, allowing the down- (in RX mode) and up-conversion (in TX mode), and the generation of quadrature RF signals, mandatory to ensure the correct operation of the mixer.

In chapter five, the analog baseband building blocks will be designed. It will be composed of a set of elementary functions such as filters, variable gain amplifiers, switches and buffers.

In chapter six, once the entire design was carried out, a summary of the performances of the full transceiver was exhibited. A conclusion over the appropriateness of the system will be made.

Finally, perspectives for the future works and improvement axis will be expressed in the light of all the comments that were made in the different sections of this PhD work. The thesis organization is summarized within the following chart flow Figure 4. Publications and tape-outs conducted during the thesis are chronologically summarized in Figure 5.



**Figure 5: Thesis publications and tape-outs chronology**





# Chapter 1: INTRODUCTION TO TELECOMMUNICATION SYSTEMS

**E**ver since humankind gathered into societies, individuals tried to communicate using a common language. Afterwards, new methods of communications emerged to further maximize gains in time that could make a valuable difference. From a distance, where voice was not an option, sound signals, light or even smoke signals can substitute common languages to signify the presence of an event to be shared to others members of a community. By doing that, they can organize with a precious advance. Combinations of multiple techniques can even send a rather complex signal, even though the materials involved are primitive. It also leads to the question of unifying methods of communications not to get a wrong interpretation of the messages, by the mean of standardization.

The complexity of communications systems never stopped improving to reach the ones we know today, with the emergence of telecommunications, using personal cell phones. It has reached a point at which anyone can communicate with everyone almost instantly, using affordable tools, and nearly everywhere.

## 1.1 EVOLUTION OF MOBILE TELECOMMUNICATIONS

In order to understand what we should expect from new mobile generations and look forward, it is important to look back from what it originally started, to discern a trend, and anticipate future technological improvements. Wireless technologies are relatively recent concepts, when original telecommunication systems were fully wire-based.

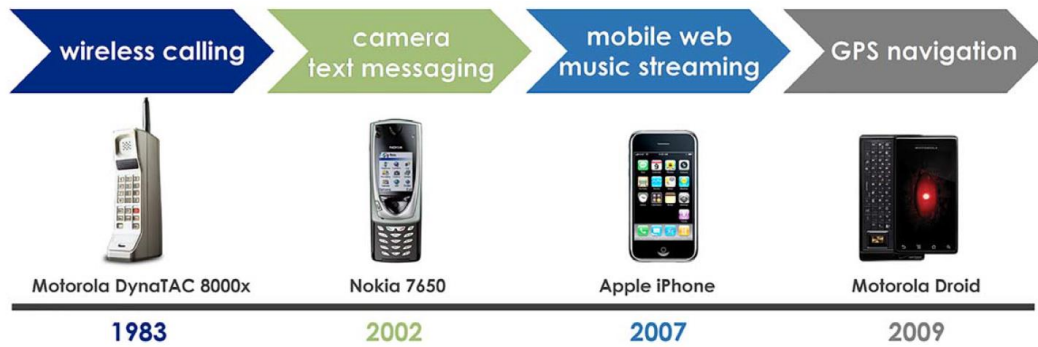
The denomination cell phone describes a much more convenient portative wireless device which uses a cellular network made of base stations used for the sake of telecommunications.

The very first mobile generation (1G) was born in the 70's. The frequency spectrum was subdivided into smaller bandwidth, allowing a user to exclusively access a specific smaller channel for the duration of his communication, by the mean of the frequency division multiple access (FDMA) technology. Based on analog modulation, the transmitted data type is voice, and the data rate is only 1.9kpbs. The main drawbacks are its single-user characteristic, the very poor efficiency of the frequency spectrum usage, and its sensitivity to potential interferers.

Every decade came with a new mobile generation, considering the rising interest and need from the public. Hence, in the 80's came the second mobile generation. This time the 2G (GSM) uses the time division multiple access (TDMA) technology and for the first time, it is based on digitalization. Using this technology, multiple users (instead of just one) can access a given channel alternately in time, and benefit from a much higher data rate.

Then, the third mobile generation (3G) was developed in the 90's. All the resources in bandwidth are now available (instead of subdivision) to every user. Each user uses a code to modulate their emission data which will be correctly demodulated at the baseband station, by using the exact same key: this allows to provide a high-speed internet access, as well as encryption.

Finally, the IP-based fourth mobile generation (4G) emerged using the orthogonal frequency-division multiple access (OFDMA) technique. The frequency spectrum is subdivided into subcarriers defined in an orthogonal fashion to maximize spectrum efficiency while reducing channels interferences. This generation reaches a data rate as high as 200Mbps [2] [3] [4].



**Figure 6: Cell phone functional evolution [5]**

This data rate continuous expansion from generation to generation enabled the number of data types to evolve from analog callings to online video streaming, in particular [5].

At first, mobile communications were reserved to a very restricted part of the population with sufficient financial income. After the never-ending decrease of prices, it has begun very popular and more efficient than ever. In thirty years, data rates have been multiplied by more than 100 000. Table 1 summarizes the characteristics of various mobile generation from the oldest to the latest. Now, the new generation of mobile communication (5G) is already been promoted by telecom providers, and will be discussed in the next section.

Technology	1G	2G	2.5G	3G	4G
Design began	1970	1980	1985	1990	2000
Service	Analogue voice	Digital voice	High-capacity packets, MMS	High-capacity broadband data	Higher capacity, completely IP, multimedia
Multiple access	FDMA	TDMA, CDMA	TDMA, CDMA	CDMA	OFDMA
Standards	AMPS, TACS, NMT	CDMA, GSM, PDC	GPRS, EDGE	WCDMA, CDMA2000	Single standard
Bandwidth	1.9 kbps	14.4 kbps	384 kbps	2 Mbps	200 Mbps
Core network	PSTN	PSTN	PSTN, packet network	Packet network	Internet

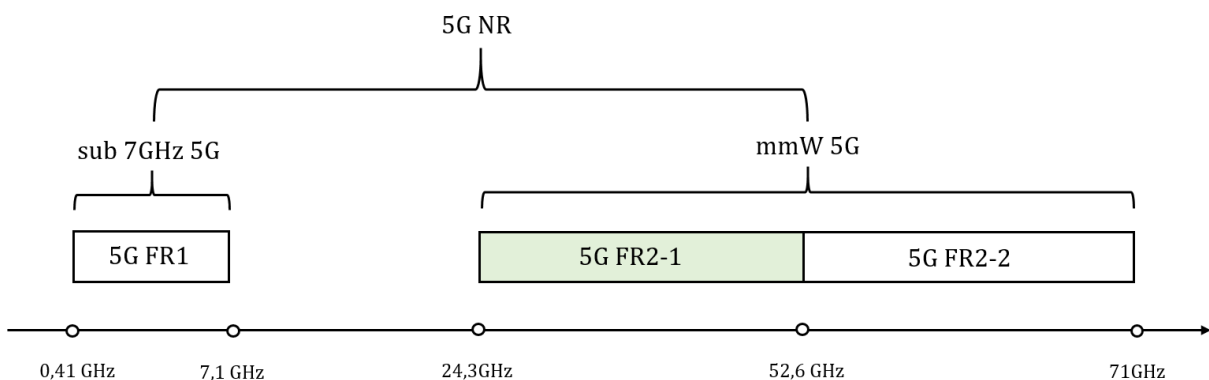
**Table 1: Mobile generation technological history from 1G to 4G [3]**



Another remarkable thing about 5G is its multi-standard capability: meaning that the 5G will reuse old standards, and use additional frequency bands.

Many are the industry fields that would be impacted by this mobile revolution. This impact is quantified in Figure 7. They are numerous because a large panel of applications that supports the 5G. It can be achieved through the use of smart robots, camera monitoring, sensors, tracking, remote reliable device connections, or even with autonomous vehicles [9]. In this way, it will raise an extraordinary economic interest worldwide. Indeed, a recent report made by IHSMarkit® in 2020 shows that trends predict a \$13.1 trillion in global sales activity in 2035 as in Figure 7. The unexpected post-COVID-19 situation also pushed forward the need for an even more digitalized and connected world [6]. Another crucial point is the high compatibility of 5G with IoT, serving industry sectors.

It is also important to clarify the different types of 5Gs. As shown in Figure 8, 5G NR bands are separated into two main families: the sub-7GHz 5G (5G FR1 frequency bands) – which are used for the majority of the current 5G mobile communications – and the mmW 5G (5G FR2-X frequency bands), mostly dedicated for short-range applications [10]. A new attractive band unofficially known as the 5/6G FR3 band is already being investigated, ranging from 7.1 to 24.3GHz.



**Figure 8: Description of the 5G NR frequency bands**

The mmW prefix denotes frequencies whose wavelength is in the order of centimetres which roughly correspond to frequencies ranging from 30 to 300GHz. As we see, the 5G FR2 bands are located at much higher frequencies and more importantly, where more bandwidth (BW) is available. They are hence helpful candidates for applications expecting high data rate. On

the one hand, a higher operating frequency will provide a higher data rate, but on the other, propagation losses in the air will therefore increase. The free-space path losses (*FSPL*) are defined in [11] by

$$FSPL = \left(\frac{4\pi d}{\lambda}\right)^2 = \left(\frac{4\pi f}{c}\right)^2 \quad (1)$$

Where  $d$  is the distance that separates both emitter and receiver,  $f$  the operating frequency,  $c$  is the speed of light, and  $\lambda$  is the wavelength. It shows that the propagation losses are proportional to the frequency squared. More that, this attenuation will also worsen due to bad weather conditions, as well as the presence of obstacles between the users and the base stations [2].

### 1.1.2 5G NR FR2-1

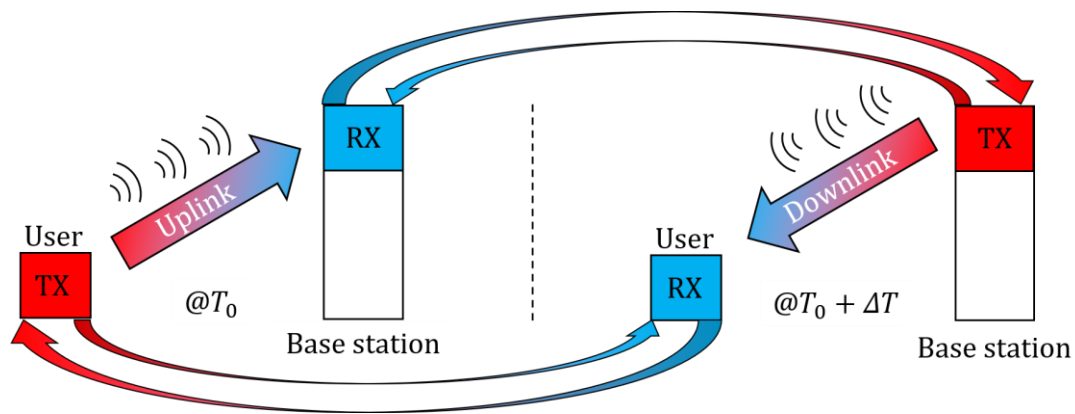
#### 1.1.2.1 Duplexing and multiplexing techniques

In this section, and for the rest of the thesis work, an exclusive focus will be made over the 5G FR2-1 frequency bands as listed in Table 2.

Band	Range of frequencies in FR2-1			
	Uplink [GHz]	Downlink [GHz]	Bandwidth [MHz]	Duplex Mode
n257	26.5 – 29.5	26.5 – 29.5	50/100/200/400	TDD
n258	24.25 – 27.5	24.25 – 27.5	50/100/200/400	TDD
n259	39.5 – 43.5	39.5 – 43.5	50/100/200/400	TDD
n260	37 – 40	37 – 40	50/100/200/400	TDD
n261	27.5 – 28.35	27.5 – 28.35	50/100/200/400	TDD

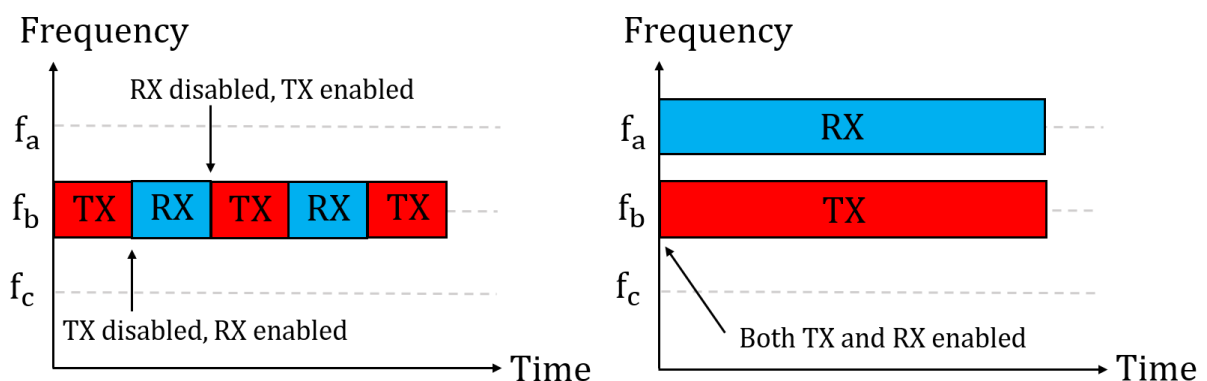
**Table 2: 5G-FR2-1 frequency bands [10]**

It is important to notice the 3GHz-bandwidth which is available for the five bands. In our case, the chosen band of interest was the n260 band ranging from 37GHz to 40GHz. As it can be observed the bandwidth of the channels can vary from 50MHz to 400MHz. The developed system must hence be reconfigurable. We also observe that the uplink and downlink connections frequencies are identical: this is typical for TDD systems. This principle is described Figure 9 and the TDD and FDD techniques are compared Figure 10.



**Figure 9: Uplink and downlink connections between a user and a base station in TDD**

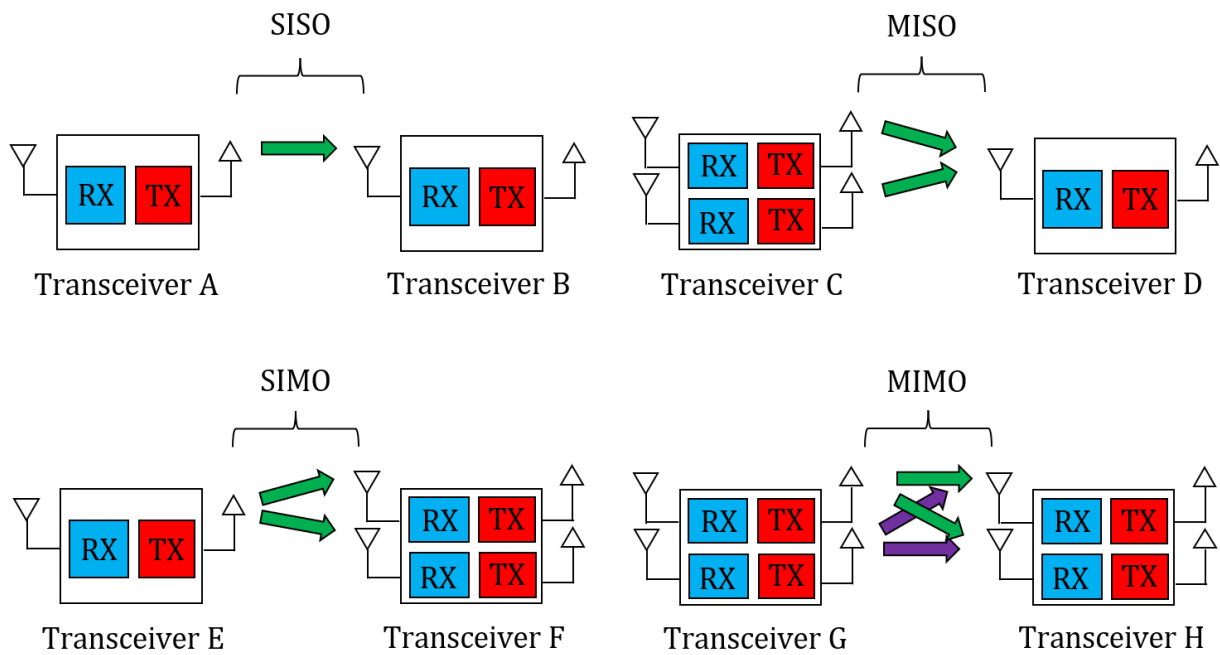
In TDD, when the emitter operates, the receiver is turned off. Inversely, when the transmitter operates, the receiver is turned off. In the case of the FDD, both receiver and transmitter operate at the same time, but using different operation frequencies. The main issue of such architectures is the possible interference from the TX over the RX. For instance, while the TX operates, it generates high-power signal that can be presented to the receiver. In TDD the receiver is off, while in FDD it expects a different frequency.



**Figure 10: Difference between two multiplexing modes: the TDD (left) and the FDD (right)**

There are also multiple telecommunication multiplexing techniques existing in order to insure multiple efficient and reliable communications at the same time using the same propagation channel. Those are listed in Figure 11. The acronyms SISO, MISO, SIMO, and MIMO respectively stand for single-input single-output, multiple-inputs single-output, single-input multiple-output and multiple-inputs multiple-outputs. The type of multiplexing hence depends on the number of input and output involved in the communication. In our work case, it is about multiple cell phones communicating to a base station also in communication with multiple cell phones as in between transceiver G and H: the multiplexing technique is hence



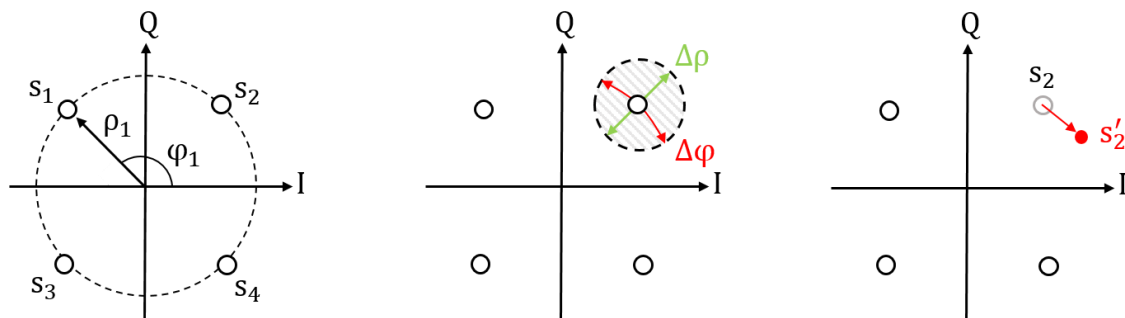


**Figure 11: Examples of various telecommunication multiplexing techniques**

MIMO. When hundreds of antennas are deployed over a BS, we no longer talk about MIMO, but about massive-MIMO instead [12].

#### 1.1.2.1 Modulation

Modulation is an attractive way to transmit data efficiently. If we consider the simplistic example of using light as a medium of communication, the presence of light would mean 1 and its absence as a 0. This way, the light has been modulated from a light signal to a digital data. The 5G uses (more or less) the same principle except the information is contained inside the amplitude  $\rho$  and the phase  $\varphi$  of an electromagnetic signal  $s(t)$  defined as  $s(t) = \rho \sin(\omega t + \varphi)$  where  $\omega = 2\pi f$ . In the case of a Q-PSK (or 4-QAM) modulation, each symbol  $S_1$ ,  $S_2$ ,  $S_3$  and  $S_4$  respectively carry the binary information  $(00)_2$ ,  $(01)_2$ ,  $(10)_2$



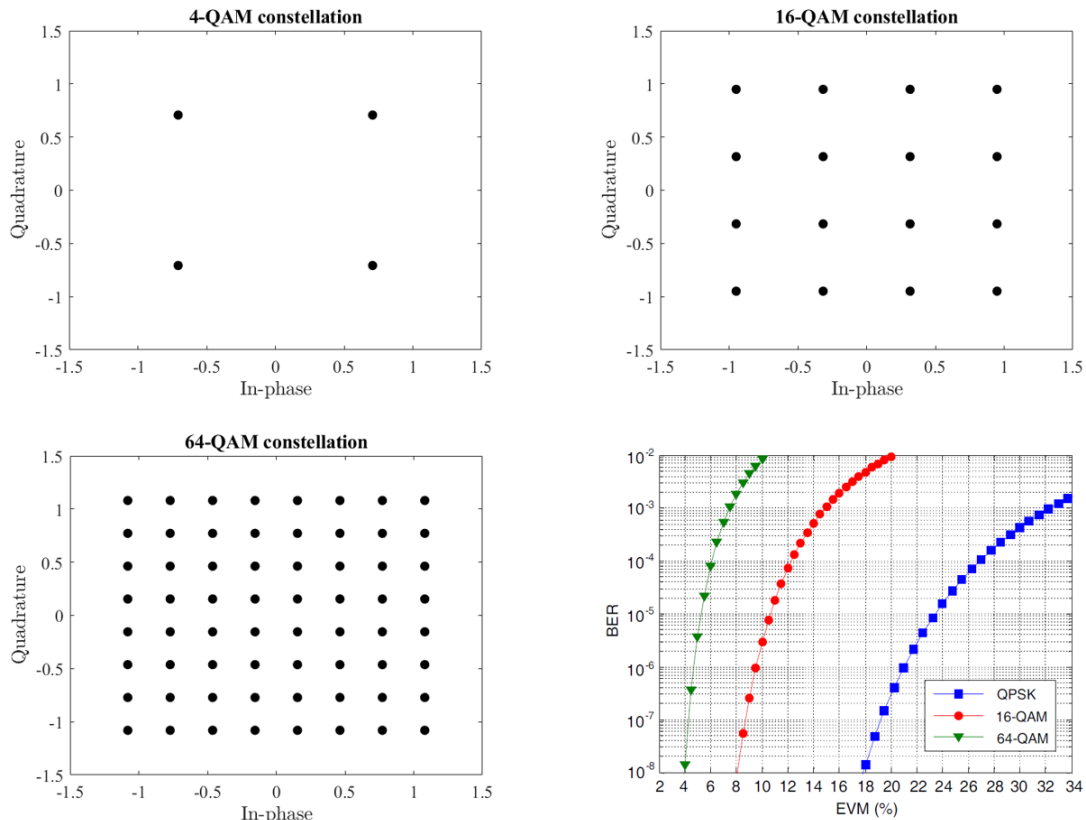
**Figure 12: Symbols and symbolic representation of EVM in the case of a 4-QAM modulation**

and  $(11)_2$  as shown in the constellation diagram Figure 12. The module here are constants  $\rho_1 = \rho_2 = \rho_3 = \rho_4$  but the phases  $\{\varphi_i\}_{i \in [1,4]}$  vary from  $90^\circ$  (S2) up to  $270^\circ$  (S4).

In real systems, it is nearly impossible to transmit or receive signals with a perfectly defined phase and/or amplitude. Hence, some phase and amplitude errors can be induced by electronic functions, or by the propagation channel, and the effective (transmitted or received) symbol will contain an error. The error vector from S2 to S2' in Figure 12 is quantified with the Error Vector Magnitude (EVM) metric. The EVM is defined in [13] as

$$EVM = \frac{\sum_{n=1}^M |S'_n - S_n|^2}{\sum_{n=1}^M |S_n|^2} \quad (2)$$

Where  $S'_n$  is the magnitude of the actual symbol while  $S_n$  is the magnitude of the expected symbol. In other words, if the EVM becomes larger than a given threshold value (specific to a given modulation) misinterpretation of the symbol will occur during the demodulation process. The Q-PSK can be adapted in modulation containing more symbols to enhance data rate. By doing so, the margin over the EVM maximal value will hence shrink.



**Figure 13: 4-QAM, 16-QAM, 64-QAM modulations constellation, and associated BER versus the EVM [14]**

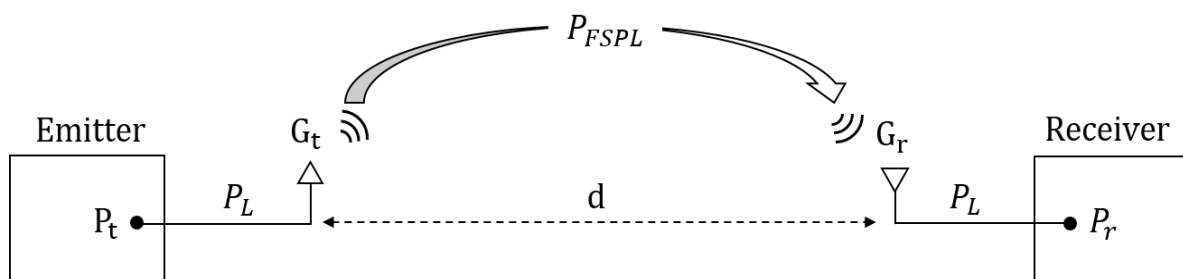
Constraints over building blocks used for demanding PSK modulations will increase and it will be more challenging to design. As we see on the right-hand bottom side of Figure 13, to obtain the same bit error rate (BER) with a 4-QAM modulation scheme, the EVM using a 64-QAM modulation has to be much smaller due to the closer proximity between neighbour symbols.

### 1.1.2.2 Link budget

In order to size electrical systems, it is important to understand what happens to the electromagnetic signal, when emitted and propagated into the telecommunication channel. In line of sight (or LOS), one of the key equation of telecommunications is the link budget that can be expressed as

$$P_r = P_t + G_t - P_L - P_{FSPL} + G_r \quad (3)$$

Where  $P_r$  is the received power,  $P_t$  the transmitted power,  $G_t$  is the transmitter antenna gain,  $P_L$  the miscellaneous power losses,  $P_{FSPL}$  the propagation losses defined in Equation (1) and  $G_r$  is the receiver antenna gain. Power are expressed in dBm and Gains in dBi. This equation is illustrated as in Figure 14.



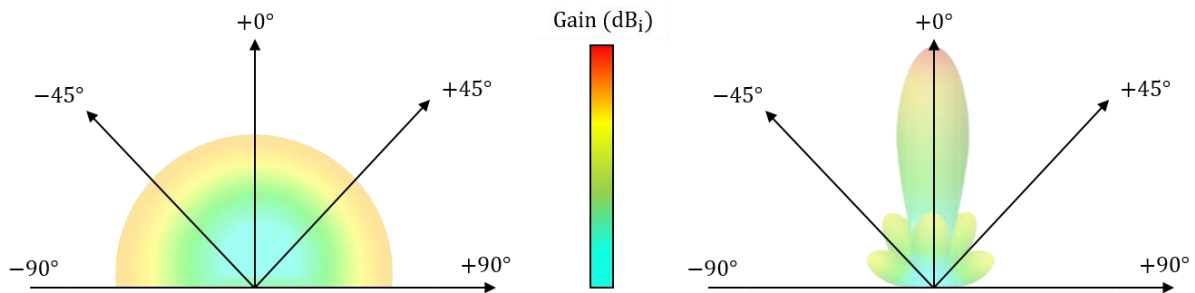
**Figure 14: Typical link budget illustration**

As we have seen, the received power is a function of both TX and RX antenna gain. One way of increasing one antenna gain is to increase its size. However, using large electrical elements will lead to mechanical problems.

Arrays seem therefore relevant candidates to provide extra gain (Figure 14 right). Arrays are also useful because not only they are highly versatile they are also very compact [15]. They therefore constitute a strong alternative in high frequencies integrated telecommunication systems.

## 1.2 THE BEAMFORMING CONCEPT

The beamforming technique describes an antenna radiation pattern exhibiting directivity (or is beam-shaped as in Figure 15 right). As a comparison, isotropic antenna spread their power in all possible directions (see Figure 15 left).



**Figure 15: Illustration of isotropic and directive radiation patterns**

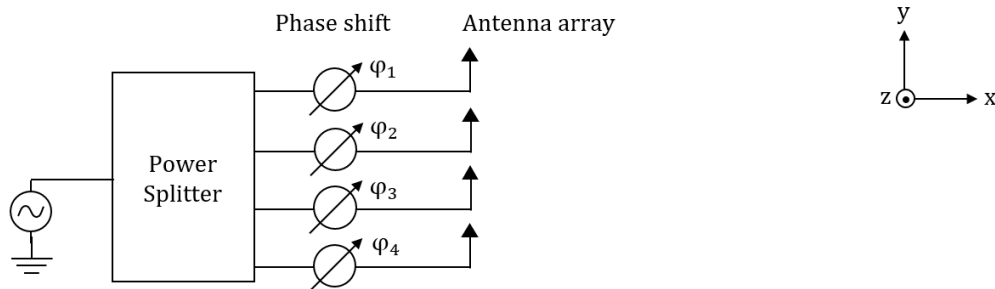
Isotropic antennas can cover much more space at all-time using only one lobe, but the power is not efficiently used since some power is sent in direction where there are no users, and no need for connections. In the other case, the power is mainly concentrated into a main lobe resulting in much more gain, but has to target the user using space scanning techniques because it is now directive. It leads to the reduction of interferences since the power is concentrated into space. This extra gain source will relax trade-offs between output power, SNR and power consumption over the FEOL of both emission and reception chains, if this array is used in a transceiver. It is possible to adapt the radiation angle, thanks to the beamsteering technique. MIMO and massive-MIMO systems are based on the beamforming technique, allowed by the use of antenna arrays.

### 1.2.1 BEAMSTEERING

Indeed, the radiation beam can be orientated in space to point a user in order to take maximum benefit of the directive gain as illustrated in the previous section. In this case, a 2D beamsteering is presented.

Figure 16, illustrates a simplistic sub-beamforming system composed of one power source, one power splitter that spreads the power equitably into the four branches, four phase

shifters and a 4x1 antenna array. The vertical orientation (across the  $(\widehat{O, x, y})$  angle, noted  $\theta$ ) is called *elevation* and the horizontal orientation (across the  $(\widehat{O, y, z})$  angle, noted  $\phi$ ) is called *azimuth*. In order to obtain a 3D beamsteering, extra columns need to be added to the 4x1 array.



**Figure 16: Beamsteering technique explained within an analog beamforming architecture (1/3)**

The beam orientation is done applying right phases for  $\varphi_1$ ,  $\varphi_2$ ,  $\varphi_3$  and  $\varphi_4$  found in Figure 16. The Relative phase conditions between adjacent paths for beamsteering are described in [16]:

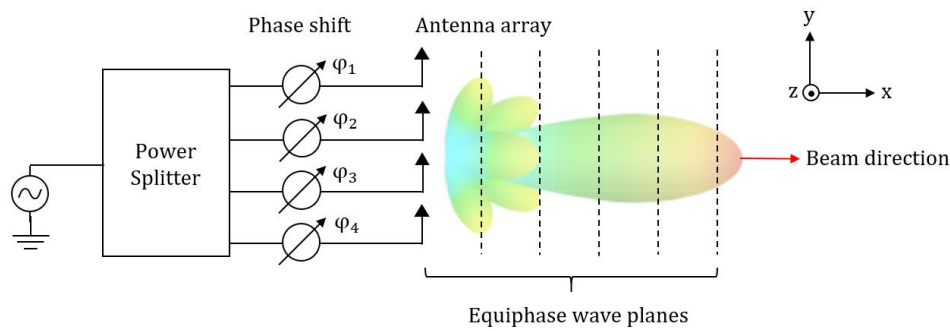
$$\Delta\varphi = 2\pi \left( \frac{d \sin \theta}{\lambda} \right) \quad (4)$$

Where  $\Delta\varphi$  is the relative phase between two paths ( $\varphi_1$  and  $\varphi_2$  or  $\varphi_3$  and  $\varphi_4$  for instance),  $d$  is the distance between two antennas,  $\theta$  is the steering angle and  $\lambda$  the wavelength.

This allows beamforming to produce almost any radiation patterns and maximizing gain in the main lobe, while having very little power in the secondary lobes. It also nullifies the power between lobes.

- *First case scenario*

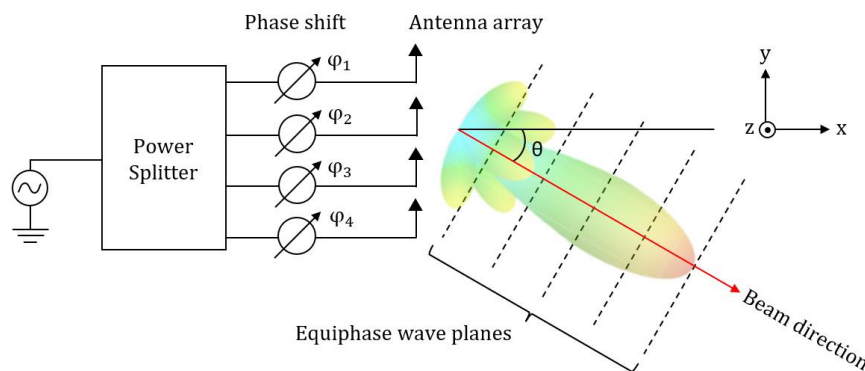
In this case,  $d = \lambda/2$  and the relative phase shifts  $\Delta\varphi$  equals to  $\pi$  between each four neighbour paths as in (4) then  $\theta$  equals to 0 and the beam is orientated toward the x axis. Equiphase wave planes are in parallel with the antenna array as in Figure 17. Constructive interferences create beams while destructive interferences create nulls (inter-lobes minima).



**Figure 17: Beamsteering technique explained within an analog beamforming architecture (2/3)**

- *Second case scenario*

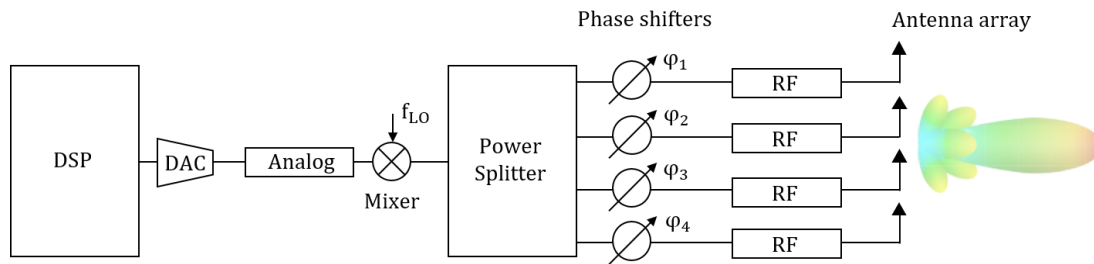
In this case,  $d = \lambda/2$  and the relative phase shifts  $\Delta\varphi$  equals to  $\pi\sqrt{2}$  between each four neighbour paths as in (4) then  $\theta$  equals to  $45^\circ$ . Equiphase planes shifted from the previous case and the beam should be orientated as in Figure 18.



**Figure 18: Beamsteering technique explained within an analog beamforming architecture (3/3)**

### 1.2.2 ANALOG BEAMFORMING

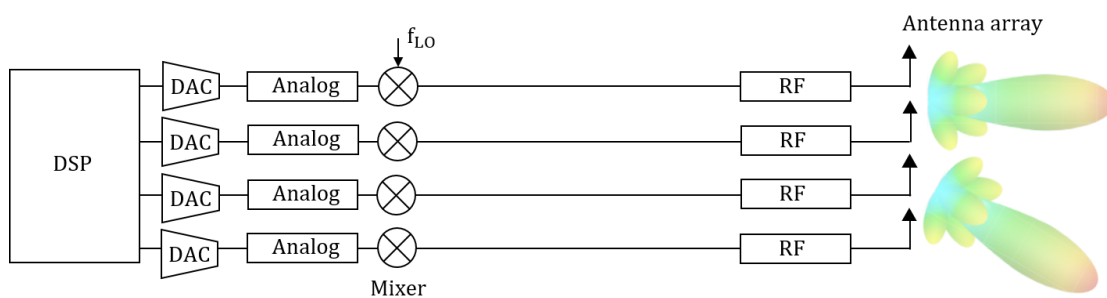
They are multiple ways to use the beamforming technique, based on architectural differences. The analog beamforming technique uses a structure where only one FEOL is involved. The RF signal power is spread equally within the four branches and then phase shift is applied. Consequently, only one beam is created and so only one user can benefit from it as in Figure 19. Therefore, it is not suitable for MIMO communications. However, due to the high simplicity of the architecture and the reduced number of blocs involved, it is area efficient as well as power efficient. The phase shifting can even be realized by phase shifters within the analog baseband chain, or by changing the phase of the RF mixer LO signal (also known as LO beamforming) [17].



**Figure 19: (RF) analog beamforming typical architecture**

### 1.2.1 DIGITAL BEAMFORMING

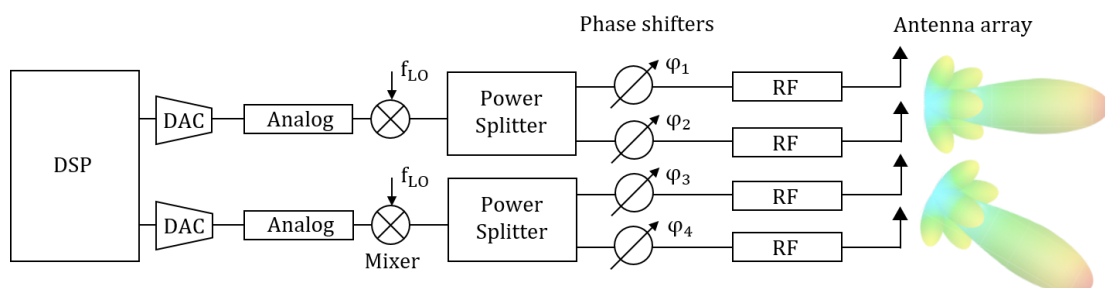
As to the digital beamforming it is very similar to the analog beamforming technique except each antenna as a dedicated FEOL. Since all paths are independent, several beams can hence be created and numerous users can benefit it at the same time. However, the duplication of FEOL will lead to a larger phased array system and a higher power consumption, even though the phase shift is done digitally. The architecture is described Figure 20.



**Figure 20: (RF) digital beamforming typical architecture**

### 1.2.2 HYBRID BEAMFORMING

The hybrid beamforming is a combination of the two previous techniques taking advantage of an optimized power consumption at a reduced chip size allowing multi-users communications.



**Figure 21: (RF) hybrid beamforming typical architecture**

### 1.2.3 BEAMFORMING TECHNIQUES SUMMARY

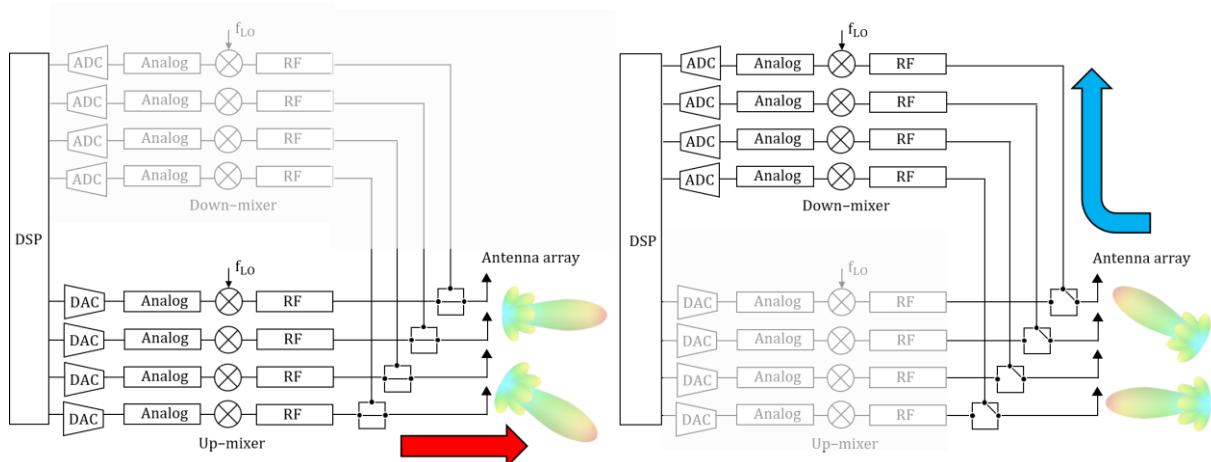
Pros and cons of the various beamforming techniques were summarized in the table below.

Beamforming technique	Advantages	Drawbacks
Analog	Simple architecture Good power efficiency	Single beam, single user Not versatile
Digital	Multi beam, multi users Reconfigurable	High power consumption, LO precision, ADC linearity
Hybrid	Multi beam, multi users Versatile	Lower power consumption than digital

**Table 3: Beamforming techniques summary and brief comparison**

### 1.3 INTRODUCTION TO BIDIRECTIONAL SYSTEMS

A bidirectional circuit allows its input and output to play alternatively mutual roles. Such systems are relevant in TDD systems where TX and RX are alternatively enabled and shares the same integrated antenna. From a system point of view, if we consider the previous digital beamforming architecture in Figure 20, and we adapt it into a conventional bidirectional operating mode, we obtain the architecture as in Figure 22. As we can see the antenna array respectively play the role of input (in RX mode) and output (in TX mode) while the digital signal processing (DSP) acts both as input (in TX mode) and output (in TX mode).



**Figure 22: Conventional bidirectional RF digital beamforming system in TX (left) and RX mode (right)**





# Chapter 2: SYSTEM SIZING

**J**ust like an architect designs plans for buildings, electronic engineers think of system sizing way before placing the first stone – the first stone being a transistor in our case.

Once the surroundings of the work were defined (as in Chapter 1), multiple studies need to be carried out in order to isolate potential critical limitations in the RF front-end (RFFE) design.

This work was conducted in parallel with a project that will be described in this chapter. An ongoing system design headed by the foster lab (LAIR) technical team is presented and compared with the thesis work goals, in order to understand clearly the main innovative differences between the two designs.

Once the thesis building blocks were presented, block-by-block specification tables are presented to define the design targets. A more accurate description of each building block specifications will be presented in the adequate section.

Finally, an overview of different elementary technological elements (passive and active) used in the thesis – taken from the process design kit (PDK) – will also be presented.

## 2.1 THESIS APPLICATIVE CONTEXT: THE BEYOND5 PROJECT

The BEYOND5 project is an Ecsel European project which started 1<sup>st</sup> June 2020, coordinated by SOITEC, with the ambition of pushing the level of connectivity further. The global aim is to gather within Europe the full radio-frequency electronics supply chain, serving sensing and telecommunications purposes, taking benefit from the SOI technology [18].

The internet as we know it today was born in 1983, when the TCP/IP technology allowed to connect simultaneously 500 computers with one another. Within a year this number doubled, and by then, this number kept on increasing [19]. Later on, the internet connectivity even reached the mobile telecommunication sector, as depicted in the previous chapter, allowing a massive use of the internet almost everywhere using cell phones. Since the early 2000's, the internet has even become available even inside aircrafts. Originally, based on connections with base-station located at the ground, it has expanded to connections with satellites, which are much more effective. This industry has become a multi-billion dollars flourishing market [20]. One of the technical goals of the BEYOND5 project is to incorporate a 5G mobile access point inside an aircraft to guarantee the use of on-flight high-speed mobile services, as illustrated in Figure 23. The in-cabin demonstrator will include the designed front-end modules terminated with a 4x4 antenna array, and was planned by the end of 2023. The idea was to implement one of the TRX designed through this thesis inside the multi-elements system to practically prove the interest of bidirectional circuits for 5G FR2 MIMO systems.



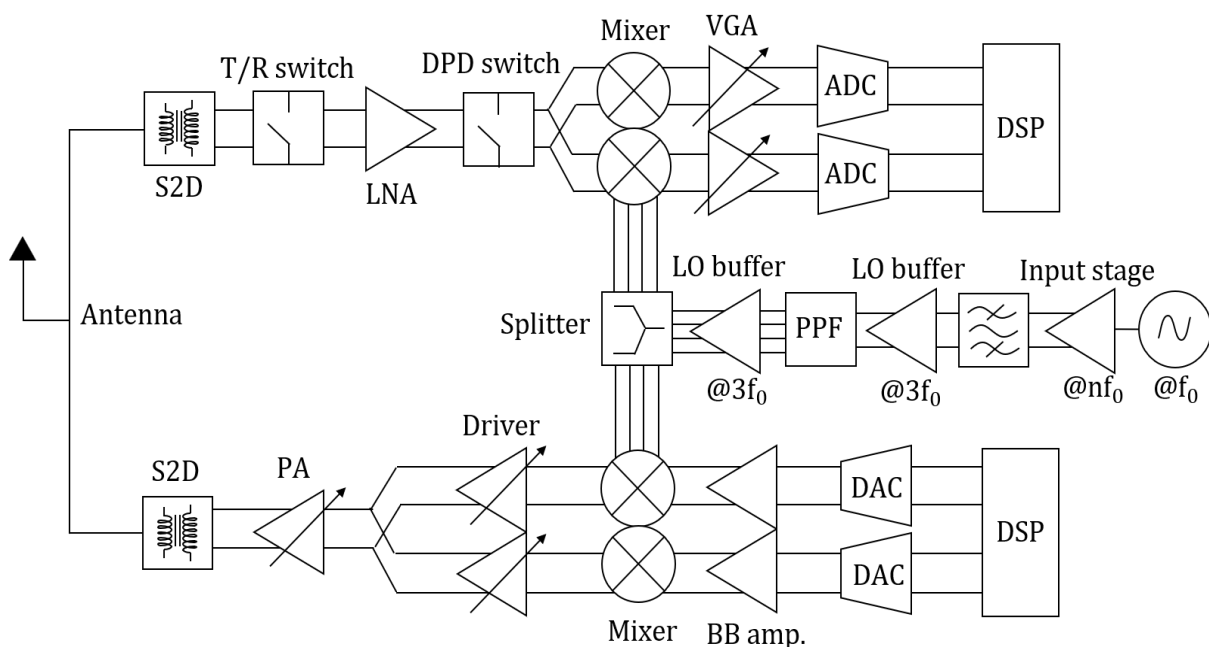
**Figure 23: Illustration of the integration of a 5G FR2-1 MIMO on-flight access point**

### 2.1.1.1 PROJECT DESCRIPTION

#### 2.1.1.1.1 Architecture

This section is about the presentation of the design conducted by the lab technical team.

In this transceiver design, both TX and RX chains are physically separated from one another and are alternatively addressed using a commuted element called a Single Pole Double Throw (SPDT or T/R, TRX switch) in order to limit the number of antennas, and to guarantee the TDD. However, by doing so, all the matching networks are dedicated to specific building blocks, and a large silicon area is hence required.



**Figure 24: BEYOND5 chip building blocks**

As we can observe, it does not only imply the separation of some electrical functions, but also the redundancy of others (such as mixers for instance, or baseband amplifiers). This front-end is duplicated four times to get the 2x2 subsystem described in Figure 25.

The building blocks allocation is described in Figure 25 (top), where all fundamental functions of the transceiver can be observed within the RX and TX paths, including frequency synthesis (SX), HS-IO (high-speed input-output), and digital functions such as serial peripheral interfaces (SPI), power management units (PMU), and digital and analog-to-analog and digital converters (ADCs and DACs).

The corresponding layout is depicted at the bottom of the same figure. The idea beyond this PhD work is to demonstrate that thanks to the concept of bidirectionality, it is possible to provide similar performances at a much lower silicon footprint.

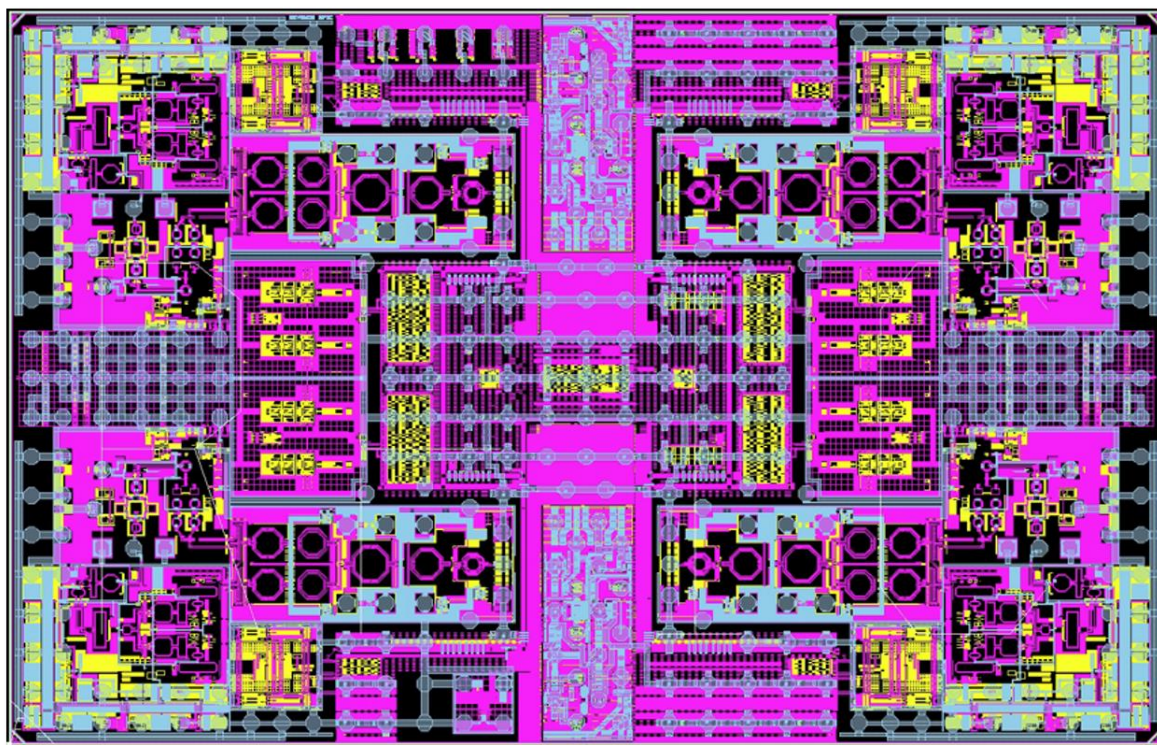
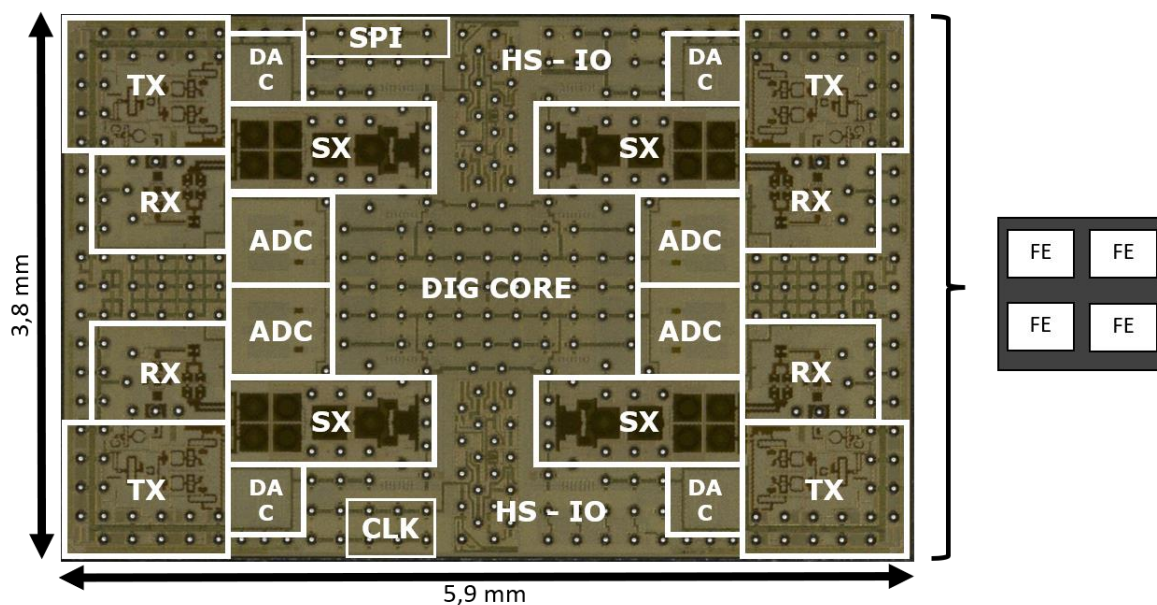


Figure 25: Die photography with building blocks allocations (top) and corresponding layout (bottom)

### 2.1.1.2 Performances

The performances of the previous system presented in Figure 25 operating within the 5G FR2-1 n260 frequency band were reported within a table as in Figure 26, exhibiting very encouraging results as to an up and downlink data rate respectively as high as 225 and 150Mbps, under typical conditions for a 10 meters distance, and using a 64-QAM modulation scheme.

Those performances acted as a target for our thesis project, the goal being consuming less silicon surface. Moreover, interesting comparisons can be made between this and our design, to quantify the potential impact of trade-offs over the efficiency of bidirectional systems.

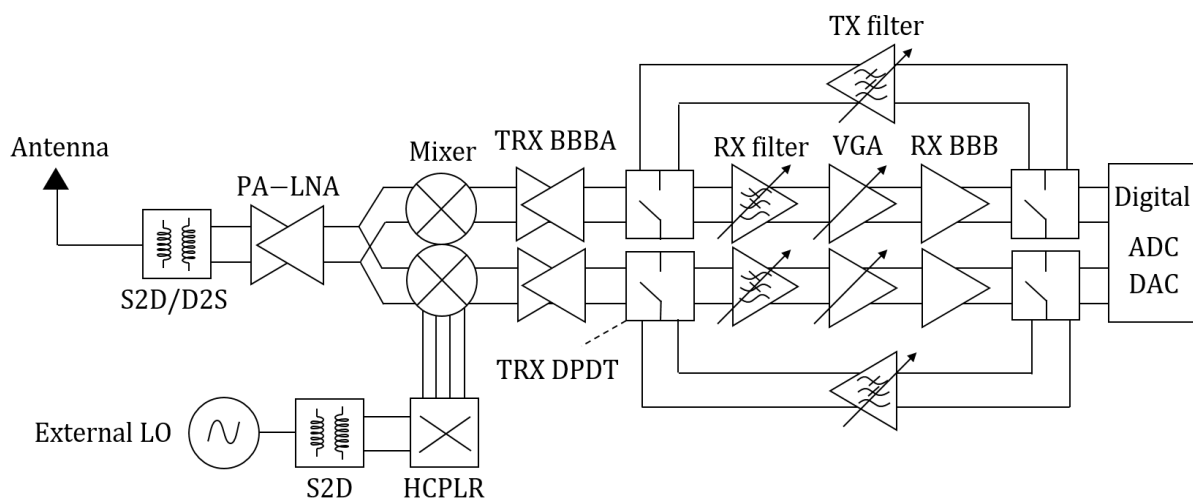
Parameter		Min	Typ.	Max	Unit
Radio Channel	n260	37	38,5	40	GHz
Number of Front-Ends (antennas) per IC			4		/
Operating temperature range	T <sub>JUNCTION</sub>	0		100	°C
Size			22,4		mm <sup>2</sup>
Total Chip Power consumption	RX mode		461		mW
	TX mode		843		mW
Channel Bandwidth (Max = Analog BW)			50	75	MHz
Output Power	P <sub>out</sub>		0		dBm
Effective Isotropic Radiated Power	EIRP			24	dBm
Receiver dynamic range		-86		-28	dBm
Base band sampling frequency	RX		240	250	MHz
	TX		600	700	MHz
IO data rate	Downlink		150		Mbps
	Uplink		225		Mbps
Adjacent Channel Leakage Ratio (ACLR)	Absolut Limit			-20	dBm/Hz
Total TX EVM (64 QAM – 10m)			4,50	5,94	%

**Figure 26: Post-layout simulations summary of the BEYOND5 chip**

## 2.1.1 THESIS CHOSEN ARCHITECTURE

### 2.1.1.1 Block diagram

The adopted block diagram for this work is depicted Figure 27. As it is noticeable from Figure 24, this new block diagram has the ambition of a much higher compacity. Some functions are fully reused such as the PA-LNA, the RF mixer, and the entire quadrature LO generation chain.



**Figure 27: Thesis transceiver building blocks description**

An ideal bidirectional system would reuse all lumped components, and so electrical nodes. However, the TX and RX specifications over functions that need to share electrical nodes can highly differ. For instance, in both cases, high frequency amplification needs to be performed in the RF domain. It is hence very interesting to implement bidirectional structures. However, regarding the analog baseband chain, specifications of the two chains differ so much, that a switching component appears to be the only effective and simplistic option. Additionally, since no magnetic components are required, the baseband electrical functions require less silicon surface than the RF ones so the separation of TX and RX analog baseband chains is then less critical. This system is composed of several fundamental building blocks enumerated as follows

- A PA-LNA constituting the RF front-end, and responsible for the high frequency amplification in both TX and RX mode
- A RF Mixer allowing the direct frequency conversion from one frequency domain to another

- A baseband TRX double pole double throw (DPDT) switch alternatively addressing both TX and RX analog baseband chains
- A hybrid coupler (HCPLR) for the quadrature generation of LO RF signals mandatory for the usage of the selected mixer
- Reconfigurable TX and RX filters for the 5G FR2-1 BW channel selection
- A RX VGA for a digitally controlled gain amplification

The antenna and oscillator design are not covered in this thesis. The antenna is assumed to be an ideal  $50\Omega$  load, while the LO RF signal is generated using an off-chip single-ended external source.

#### 2.1.1.1 Power budget

In order to know the conditions under which the transceiver will operate and to establish the power budget, DACs and ADCs involved are characterized as in the following Table 4 and Table 5 regarding their power-handling capability. Hence, the block-by-block power budgets were established for the TX and RX chains as in Table 6 and Table 7.

ADC DYNAMICS	
Max input voltage (single-ended)	250mV <sub>peak</sub>
Mean input voltage (single-ended)	71.4mV <sub>rms</sub>
Mean power (50 $\Omega$ )	-10dBm
Max power (50 $\Omega$ )	-2dBm
Impedance (single-ended)	50 $\Omega$

*Table 4: RX ADC characteristics summary*

DAC DYNAMICS	
Max output voltage (single-ended)	125mV <sub>peak</sub>
Mean output voltage (single-ended)	41.7mV <sub>rms</sub>
Mean power (50 $\Omega$ )	-14.5dBm
Max power (50 $\Omega$ )	-5dBm
Impedance (single-ended)	50 $\Omega$

*Table 5: TX DAC characteristics summary*



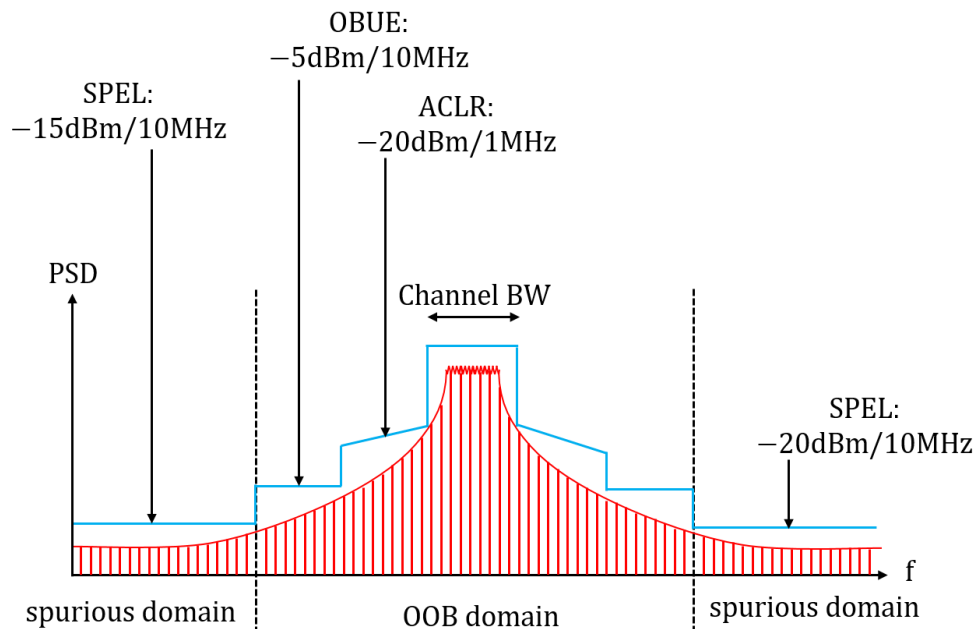
Initial TX power budget				
	Typical gain (dB)		Output power (dBm)	
	Mean Pdac	Max Pdac	Mean Pdac	Max Pdac
TRX DPDT	-2	-2	-13.5	-4
TX Filter	0	0	-13.5	-4
TX VGA	9.5	0	-4	-4
TRX DPDT	-2	-2	-6	-6
BBBA+Mixer	-3	-3	-9	-9
Combiner	3	3	-6	-6
PA-LNA	11	11	5	5
Total	7	7		

**Table 6: TX block-by-block power budget for various DAC power configurations**

Initial RX power budget						
	Min	Typical	Max			
Input power (dBm)	-73	-50	-38			
	Gain (dB)			Output power (dBm)		
	Min	Typical	Max	Min	Typical	Max
PA-LNA	22	23	24	-51	-27	-14
Mixer+BBBA	0	1	2	-51	-26	-12
TRX DPDT	-2	-2	-2	-53	-28	-14
Splitter IQ	-3	-3	-3	-56	-31	-17
RX Filter	-1	0	1	-57	-31	-16
RX VGA	50	23	7	-7	-8	-9
50Ω Buffer	-1	0	1	-8	-8	-8
TRX DPDT	-2	-2	-2	-10	-10	-10
Total	65	42	30			

**Table 7: RX block-by-block power budget for various power configurations**

Even though the TX VGA is mentioned in the power budget, it was not designed, the emitter was hence designed to handle the maximal DAC input power, and this amplifier could be added in future works. The gain variation could also have been implemented in the TX filter/BBBA design.



**Figure 28: Emission spectrum (red) and emission mask (blue)**

Finally, once in-band specifications were set, the emission mask over the power spectral density (PSD) was illustrated as in Figure 28, setting limits over the output spectrum.

As depicted in Figure 28, in order to reduce interferences from one communication band to another, the emitter spectrum (in red) needs to be within the emission mask (in blue). The transmit spectrum mask defines the maximal affordable power within a given channel and its surroundings. Multiple acronyms can be listed and defined as the

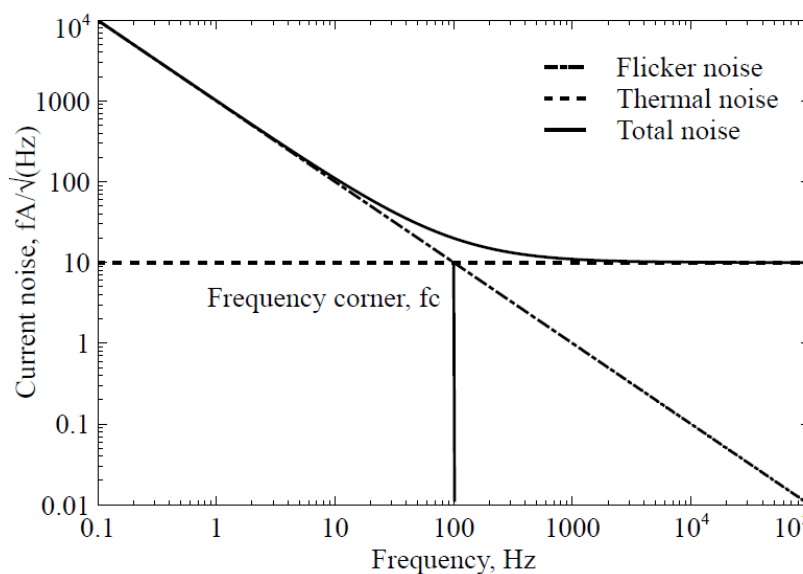
- ACLR: Adjacent Channel Leakage Ratio, which quantifies the power that will land in a neighbour channel
- OBUE: Operating Band Unwanted Emission, which are emissions located closely to the channel
- OOB domain: Out-Of-Band domain
- SPEL: Spurious Emission Limit

This graph will set constraints over the selectivity of the TX filter, and the limits of non-linearities caused by the PA and the LO leakage, in particular.

### 2.1.1.2 Noise budget

Noise is everywhere in any real electronic systems and depicts an unpredictable fluctuation of the electrical signals amplitude. As a result, the detection threshold of the minimal signal amplitude (or sensitivity) of receivers is deteriorated [21]. Noise sources are numerous and depend on the semiconductor technology involved. In field-effect transistors (FET), the noise contributions can be limited as two major contributors [22] as

- The flicker noise (or  $1/f$  noise) occurring at low frequencies
- The thermal noise, resulting from the continuous random motion of charge carriers



**Figure 29: Representation of Flicker and thermal noise, in a particular case [23]**

These two noises are illustrated in [23] through Figure 29, in a specific case scenario. The total current noise (y-axis in  $\text{fA}/\sqrt{\text{Hz}}$ ) is composed of various noise currents mostly coming from the access resistance terminals noise, as well as both thermal and flicker noise in the conduction channel [24].

The noise figure ( $NF$ ) is a key metric to quantify noise, and evaluate the degradation of the SNR. A large  $NF$  will lead to a larger EVM. In other words, if the noise amplitude gets too close to the same order of magnitude of a data-carrying signal, it will be impossible to differentiate from one another, and carried data will be lost. It is hence important to conduct a specific noise study, to anticipate and minimize its impact.

A fundamental way of studying the noise impact coming from various contributors (in a multiple-stage system design) is to calculate the affordable noise contribution for each building block. With this intention, the Friis formula was used, defined as:

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots + \frac{F_N - 1}{G_1 G_2 \dots G_{N-1}} \quad (5)$$

Where the noise factors  $\{F_i\}_{i \in \llbracket 1, N \rrbracket}$  of the various stages are part of the total noise factor  $F_{tot}$ . The noise figure  $NF$  is defined as a function of  $F$  as

$$NF_i = 10 \log F_i \quad (6)$$

Formula (5) clearly highlights that the noise contribution of the RF front-end  $F_1$  is critical, while other stage contributions are divided by the linear gain of previous stages, and are expected to play a less prominent role. A meticulous care of the optimisation of the RF front-end  $NF$  is then mandatory. The application of formula (5) allowed to fill a table where each goal noise contribution is reported in Table 8. The I/Q split induces at least a 3dB loss per path since the signal power is spread within two differential quadrature branches, within the mixer. The noise contribution is hence included in the mixer performances.

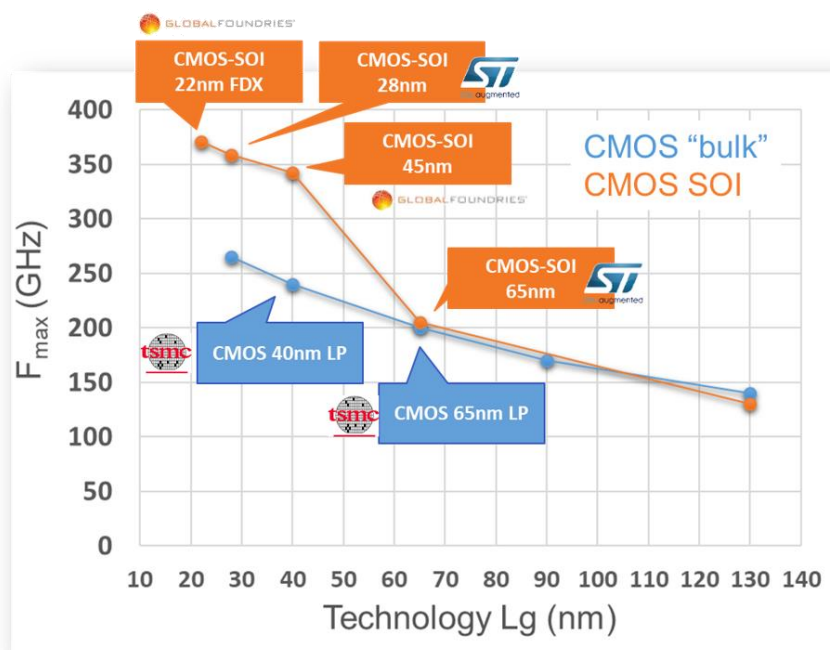
RX noise budget			
	Gain (dB)	NF (dB)	NF total (dB)
PA-LNA	23	6	6
Mixer	-7	12	6.1
Splitter IQ	-3	X	
BBBA	11	10	6.3
TRX DPDT	-2	2	6.3
RX Filter	0	15	6.4
VGA	25	20	6.7
50Ω Buffer	0	15	6.7
TRX DPDT	-2	2	6.7

**Table 8: RX block-by-block and global noise budget under typical conditions**

An alternative representation of the RX block-by-block noise and power budget was also graphically represented in Appendix A, page 180.

## 2.2 CMOS TECHNOLOGIES COMPARISON

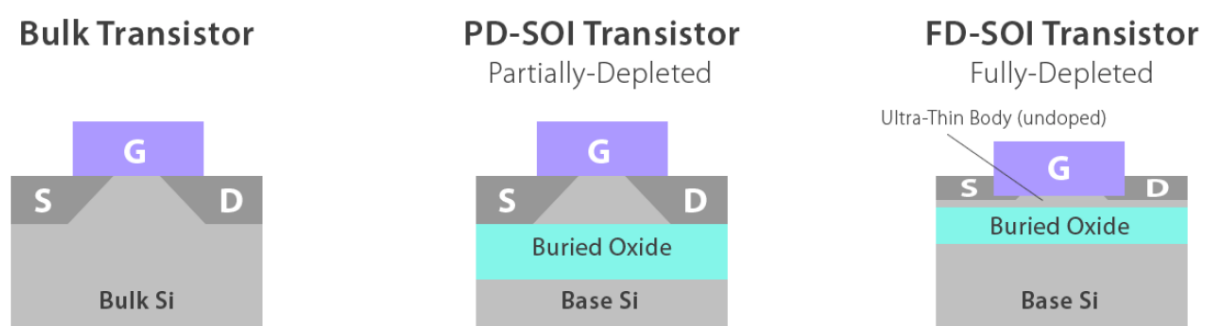
The very first model of field-effect transistors was patented by the physicist Julius Edgar Lilienfeld in 1925, but due to the lack of maturity of the semiconductor processes, very little enthusiasm resulted from it. We had to wait until that Walter H. Shockley, John Bardeen and Walter Brattain, invented the bipolar transistor in 1948 (more than twenty years later) and until 1958 to finally get to the first integrated MOSFET circuit based on only two transistors. Since then, CMOS processes has conquered the semiconductor industry thanks to its high-integration capability at reduced costs [25]. This continuous CMOS devices size reduction (transistor's gates length  $L_g$ ) allowed an ever-increasing improvement of the operating frequency as in Figure 30.



**Figure 30: Quick overview of the evolution of  $f_{max}$  with respect to the channel gate length using different CMOS processes [26]**

The reason beyond this progress is mainly due to the improvement of manufacturing techniques, since the RF performances of integrated systems are highly correlated with the quality of the metal layers and substrates [27]. However, in the MOSFET case, the technology shrinking came with issues such as the increase of parasitic capacitances, leakage currents and variability: performances will be highly affected for small geometries. Since linearity is a major

aspect of telecommunications systems, manufacturing innovations had to be made. To overcome these issues and to keep track of Moore's Law, the silicon-on insulator (SOI) technology came as a perfect candidate [28]. The SOI technology was firstly introduced in the 80's [29]. The geometry remains quite similar from a bulk technology, but the main difference is the addition of an oxide layer "buried" inside the body. The depth and width of this buried oxide can vary, as well as the channel doping, and differentiate the PD from the FD-SOI process. The cross-section view of respectively bulk CMOS, PD-SOI and FD-SOI transistors are compared Figure 31.



**Figure 31: Comparison of sectional views between bulk CMOS, PD-SOI and FD-SOI silicon processes [30]**

Applying an appropriate set of biasings over the three transistor terminals (gate G, drain D and source S) of a bulk transistor will enable current flowing from the drain to the source within a doped conduction channel. However, variations and impurity can occur in the doping process, and, the current can also flow into unwanted directions. In the PD-SOI and FD-SOI case, the charge carriers are fully contained in a thinner horizontal channel. This oxide provide isolation between the substrate and the channel.

The large knowledge and experience that the semiconductor industry has on the PD-SOI technology, as well as its relatively simplistic process, made it a reference in today's RF designs, even though shrinking is limited [27] [31]. The fully depletion is the next technological step. Its ultra-thin property allows to get rid of channel doping, and hence impurity and variability.

The FD-SOI technology benefits from very low leakage currents, low variability, low body-effect, a short-channel effect reduction, a lower threshold voltage, a higher  $g_m$ , its resistance to latch-up due to isolation between wells, and mostly, lower intrinsic capacitances allowing

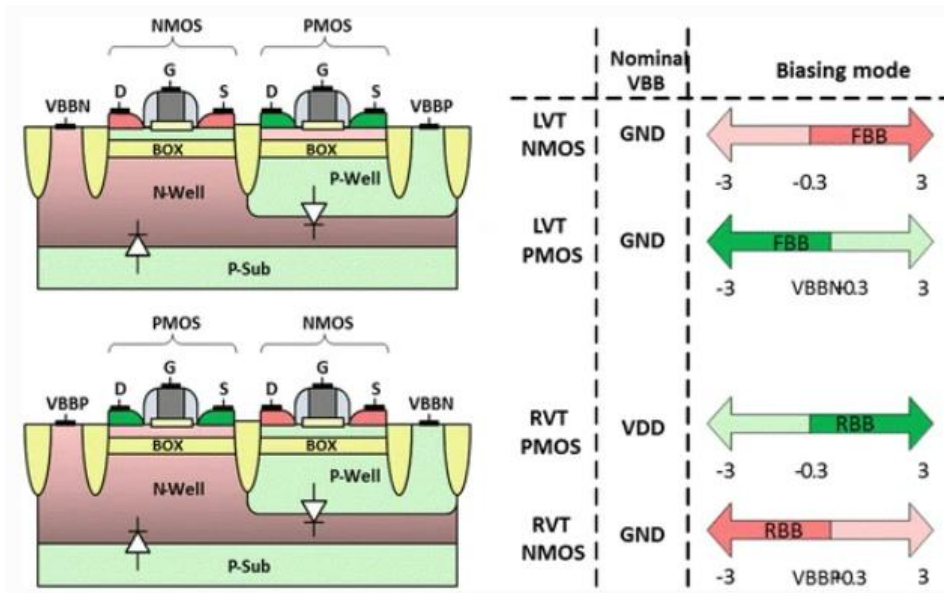


Figure 32: Cross section of 28nm UTBB FDSOI CMOS transistors Top – Low VT (LVT) transistors; Bottom – Regular VT (RVT) transistors [32]

an operation at higher frequencies [24] [28]. The performances domination of SOI over the bulk technology has been stated numerous times in the literature as in [29] and [32].

Among CMOS FD-SOI transistors, another process distinction can be made. Regularly, a NMOS is implemented on a P-well (RVT). However, if a NMOS is implemented on a N-well, it is a flipped-well (LVT). As the well changes in the four configurations, the induced diodes change, and consequently the body biasing conditions, as in Figure 32 and Figure 33 in the case of a 28nm UTBB FDSOI transistor [32]. Hence, the threshold voltage can be modulated in multiple

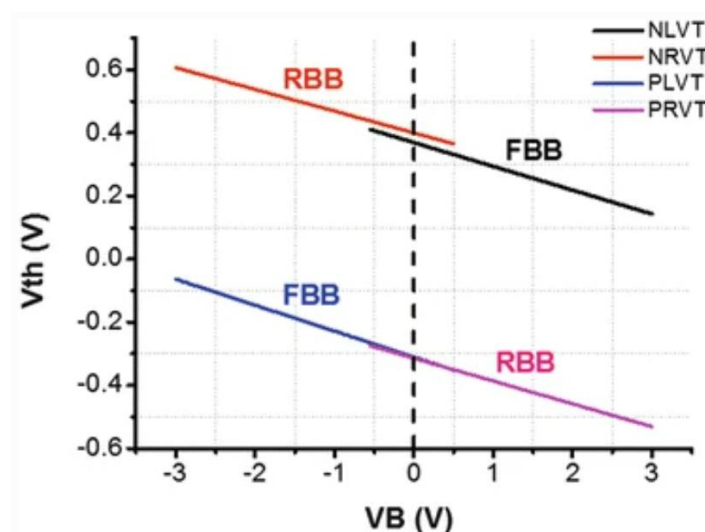
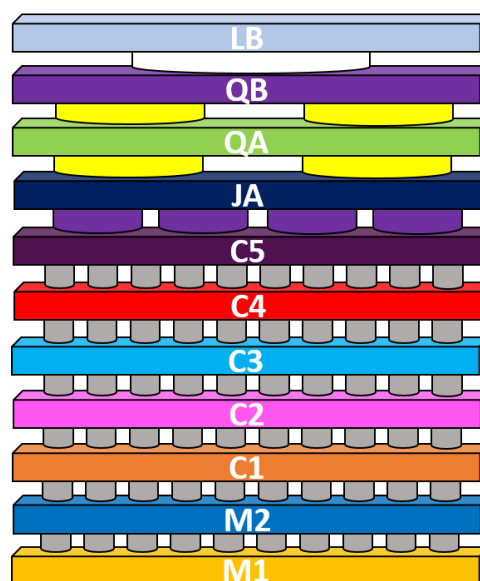


Figure 33: Threshold voltage (VT) variation with respect to body biasing voltage for RVT and LVT devices in 28nm FDSOI technology [32]

ways, using the forward body biasing (FBB) technique biasing at VB the VBBN and VBBP terminals.

The technology 22nm FDX was identified by the BEYOND5 project team to be the best candidate for the design to be conducted, hence the same technology is used in our work. The GF 22nm FDX (OPTION19) technology was hence used in our transceiver design. This technology will provide a high  $f_t$  at an enhanced  $g_m$ . The selected technology has a back end of line (BEOL) illustrated as Figure 34. It is composed of the superposition of 11 interconnected metal layers (11ML) from the thinner (M1) to the thicker (LB). Each of these layers has specific dielectric properties, and so dedicated roles in the layout routing.

In this work, the layers QA, QB and LB are dedicated to RF and supply paths, JA to analog bias supply paths, C5 and C4 to digital routing, C3 to ground patterns, C1 and C2 to analog routing carrying current, and finally M1 and M2 are dedicated to PDK PCELLs, guardring and back-gate connections. More that, an electromigration calculator (furnished by GF) is used throughout the thesis to guarantee the steady behaviour of each interconnection and routing path and ensure a long enough lifetime, even within hostile environments. If an interconnection is sized too small to conduct a given current, it will behave as a fuse that bursts, disabling the connection leading to the dysfunction of the IC in worst cases.



**Figure 34: Illustration of the metal stack of the 22nm FD-SOI technology**



## 2.3 22FDX PDK COMPONENTS DESCRIPTION

### 2.3.1 ACTIVE COMPONENTS

Transistors are fundamental components part of almost all electronic systems. They can operate within two states: they can be either ON or OFF. The first-order approximation is a resistor  $R_{on}$  and a capacitor  $C_{off}$  when they are respectively in the ON or OFF-state. Both  $R_{on}$  and  $C_{off}$  are directly correlated with the geometrical size of the transistor (width  $W$  and length  $L$ ). A NMOS transistor gets into its ON state when a sufficient potential difference is applied between the gate and the source, and in other words when

$$V_{gs} > V_{th} > 0 \quad (7)$$

Where  $V_{th}$  is the threshold voltage of the transistor. In addition, the transistor in an ON-state can operate within multiple regions, due to the voltage applied across the drain and source terminals. For  $V_{ds} < V_{gs} - V_{th}$  the transistor will operate in the *triode* region, where  $V_{th}$  is the threshold voltage. In this case, the DC drain current is expressed as

$$I_d = \frac{\mu_n C_{ox}}{2} \left( \frac{W}{L} \right) \left[ (V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad (8)$$

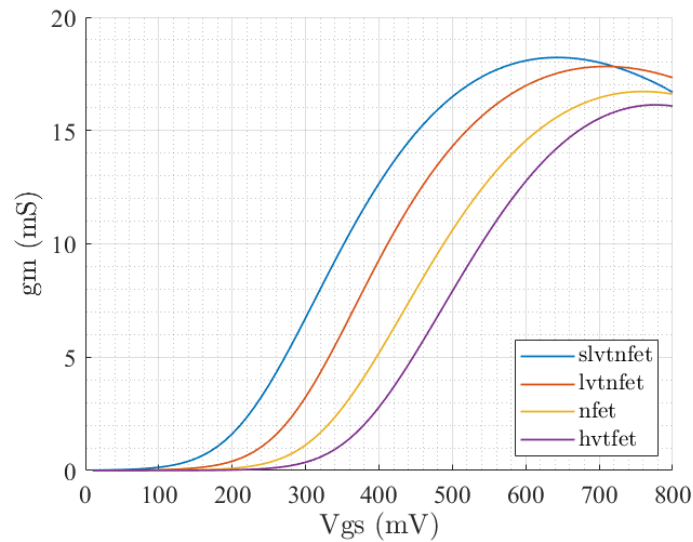
Where  $\mu_n$  is the mobility of charge carriers,  $C_{ox}$  is the surface oxide capacitor, and  $W/L$  is defined as the *aspect ratio*. Then, for sufficiently high drain-source voltages,  $v_{ds} > v_{gs} - v_{th}$  it operates within the *saturated* region and the DC drain current is then expressed as

$$I_d = \frac{\mu_n C_{ox}}{2} \left( \frac{W}{L} \right) (V_{gs} - V_{th})^2 \quad (9)$$

The transconductance  $g_m$  of a transistor is also a key metric, defined as follows

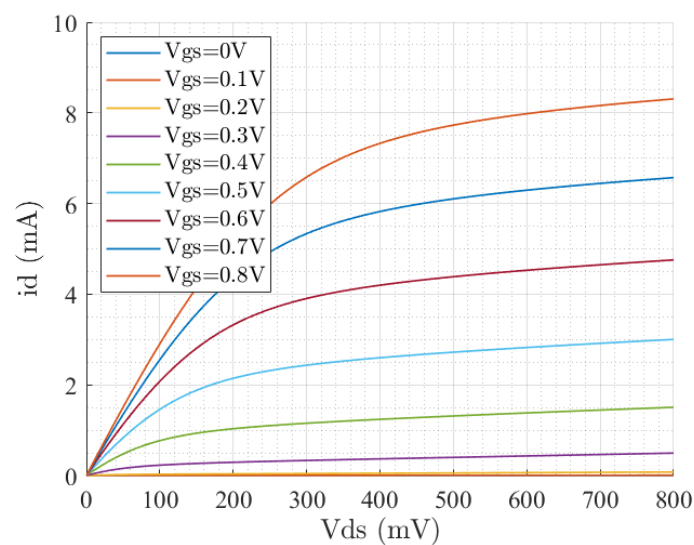
$$g_m \triangleq \frac{\partial I_d}{\partial V_{gs}} \quad (10)$$

A DC simulation was performed to plot the  $g_m$  with respect to the gate-source potential using different types of NFET transistors such as the super-low-VT (*slvtnfet*), low-VT (*lvtnfet*), regular-VT (*nfet*) and high-VT (*hvtnfet*) transistors as in Figure 35. It is clear that the super-low VT exhibits the higher  $g_m$  and the lower  $V_{th}$ .

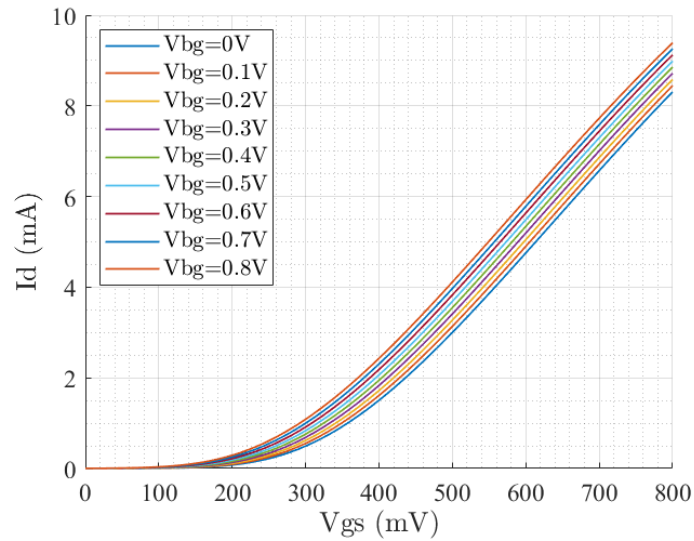


**Figure 35: DC transconductance with respect to the gate-source voltage @ $W=10\mu\text{m}$  and  $Wf=1\mu\text{m}$  for various PDK NFET transistors**

The  $i_d(v_{ds})$  curves were then plotted under multiple gate-source voltage conditions as in Figure 36 using a *slvtnfet* transistors. The two regions (triode and saturation) can be observed: where in the left the drain current responds linearly to the application of drain-source voltage, while for a high enough of drain-source voltage, the drain current starts to saturate. It also shows that the non-modulation of the channel length assumption (flat current response in the saturation region), is not realistic for accurate transistor modeling. However, it provides a close model, useful for simplistic first-order calculations.

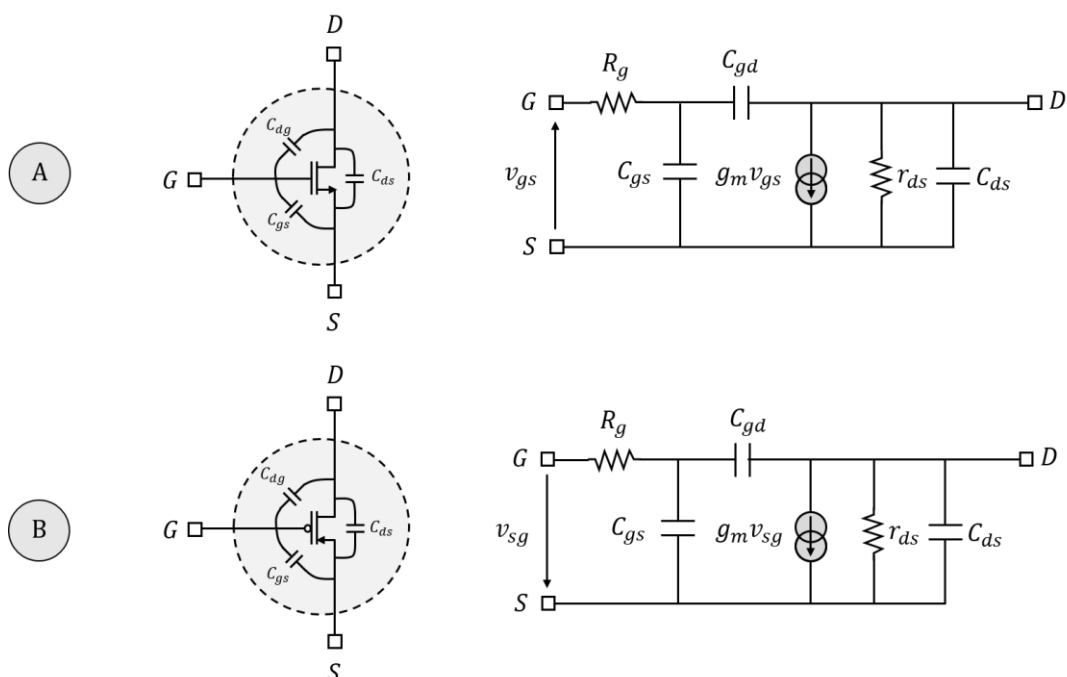


**Figure 36: DC drain current of a *slvtnfet* with respect to the drain-source voltage @ $W=10\mu\text{m}$  and  $Wf=1\mu\text{m}$  for multiple gate-source biasing conditions**



**Figure 38: DC current  $I_d$  of a slvtnfet with respect to the gate-source voltage @ $W=10\mu\text{m}$  and  $W_f=1\mu\text{m}$  for multiple back-gate biasing conditions**

Finally, as anticipated from Figure 33, various voltages were applied to the back-gate terminal of a slvtnfet, and a reduction of roughly 18% ( $\approx 60\text{mV}$ ) of the threshold voltage can be observed from the lowest to the highest back-gate biasing configuration. The quasi-static model of both NMOS and PMOS, neglecting any channel length modulation is given Figure 37 where  $C_{gs}$ ,  $C_{ds}$  and  $C_{gd}$  are respectively the gate-source, drain-source and gate-drain intrinsic capacitors of the transistor.



**Figure 37: Intrinsic small-signal high frequency model of saturated NMOS (A) and PMOS (B)**

These capacitances are proportional to the transistor geometrical size. Two metrics are crucial to characterize the high frequency operation capability of a given semiconductor technology.

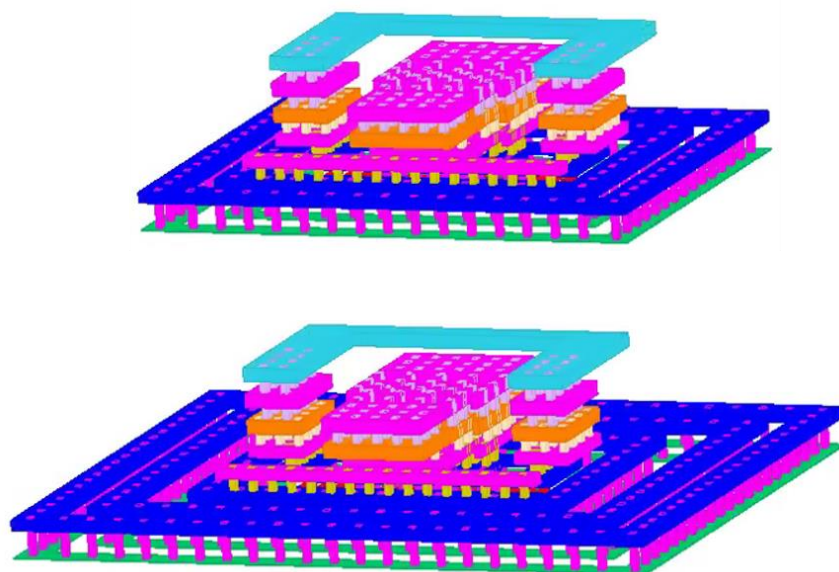
The transition frequency  $f_T$  is, is the frequency at which the current gain equals to zero while the maximal frequency  $f_{max}$  corresponds to the maximum oscillation frequency, that was previously plotted Figure 30. Both of these metrics are correlated with the intrinsic capacitors  $C_{gd}$ ,  $C_{gs}$  and  $C_{ds}$ , in particular [33]. The analytical expression of  $f_T$  and  $f_{max}$  is described in [26] through the equations below

$$f_T \approx \frac{g_m}{2\pi (C_{gs} + C_{gd})} \quad (11)$$

$$f_{max} \approx \frac{f_T}{2\sqrt{R_g(r_{ds} + 2\pi f_T C_{gd})}} \quad (12)$$

Where  $R_g$  is the gate access resistance assumed prominent over the over the other terminal accesses resistances, and needs to be minimized by choosing the adequate geometry of the transistor to reduce its impact at the operating frequency.

Finally, as an illustration, two *s/vt* NMOS and PMOS transistors with identical gate width and length were visualized using metal layers above C3.

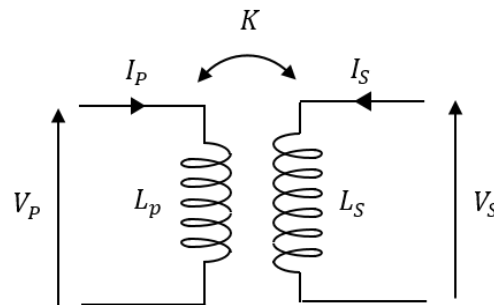


**Figure 39: 3D layout view of a slvt PMOS transistor (bottom) and NMOS transistor (top)**

## 2.3.2 PASSIVES

### 2.3.2.1 Transformers

Transformers are key passive components in RF designs. They are based on the magnetic coupling between two metal layers, constituted by the primary and secondary coils. Transformers can be typically schematized as in Figure 40.

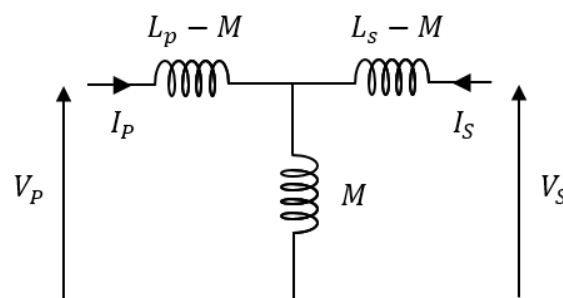


**Figure 40: Basic representation parameters of a transformer [34]**

The resulting coupling coefficient  $K$  is a function of the mutual inductance  $M$  of one transformer.  $I_p$  and  $I_s$  respectively represents the current flowing through the primary and secondary coil. The impedance of one inductance being defined as

$$Z_L = jL\omega \quad (13)$$

The mutual inductance  $M$  of a transformer is defined in Figure 41.



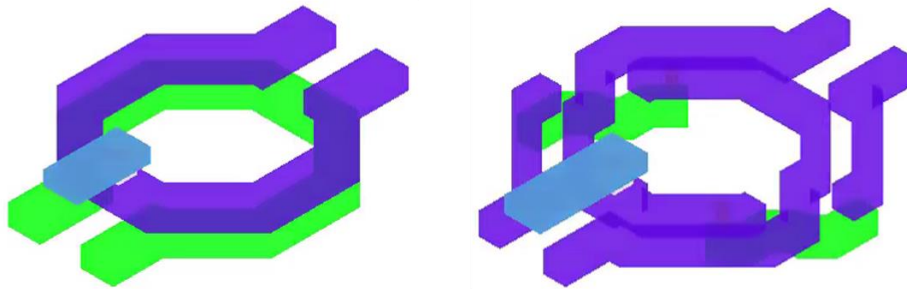
**Figure 41: First-pass lossless transformer model (T version) [35]**

Where the coupling coefficient is derived in [35] as a function of the primary and secondary inductances as well as the mutual inductance defined in Figure 41 as

$$K = \frac{M}{\sqrt{L_1 L_2}} \quad (14)$$

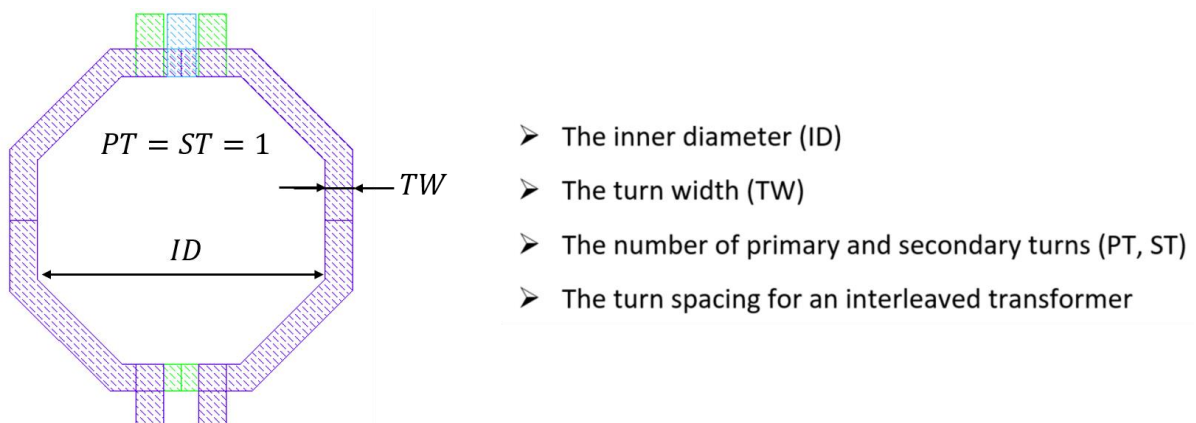
There are two main types of integrated transformers: planar (interleaved) and vertical (stacked) transformers as in Figure 42, but they also can have other shapes than as it is here.

In order to increase the value of inductances, instead of widening the primary and/or secondary that would lead to significant area consumption, multiple turns can be realised.



**Figure 42: 3D layout view of a planar coupling transformer (left) and a vertical coupling transformer (right)**

However, in mmW design a transformer does not use more than two turns because of the significance impact of losses, and the lowered resonance frequency [34]. The electromagnetic coupling occurs horizontally or vertically between the thick top two layers QA and QB (green and purple). Their primary and secondary inductances are geometrically defined following the geometrical parameters:

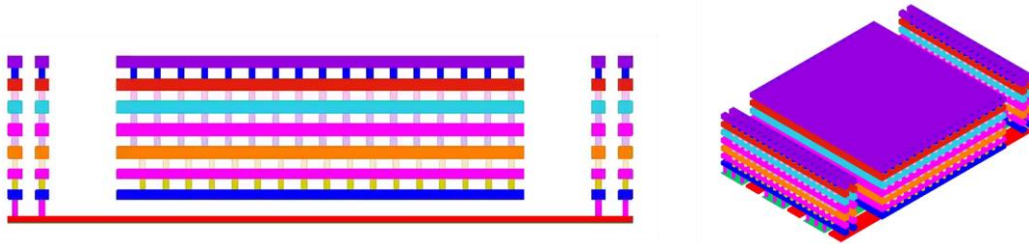


**Figure 43: Geometrical parameters of a stacked transformer and associated layout top view**

The behavior of a transformer is characterized from the quality factor of the primary  $Q_P$  and secondary  $Q_S$  inductors, and the coupling coefficient  $K$  between QA and QB. Perfect lossless coupling leads to  $K = 1$  but in real cases, it is below one.

### 2.3.2.1 Capacitors

Capacitors are elementary passive lumped components used in integrated circuits, as they store electrical charges from a voltage potential. A capacitor is composed of multiple conductive layers separated by a dielectric layer. The 3D-cross section and layout view layout of the PDK alternative polarity metal-oxide-metal capacitors (APMOM) is presented Figure 44.



**Figure 44: Cross section (left) and 3D layout view (right) of a 22nm CMOS FD-SOI APMOM capacitor**

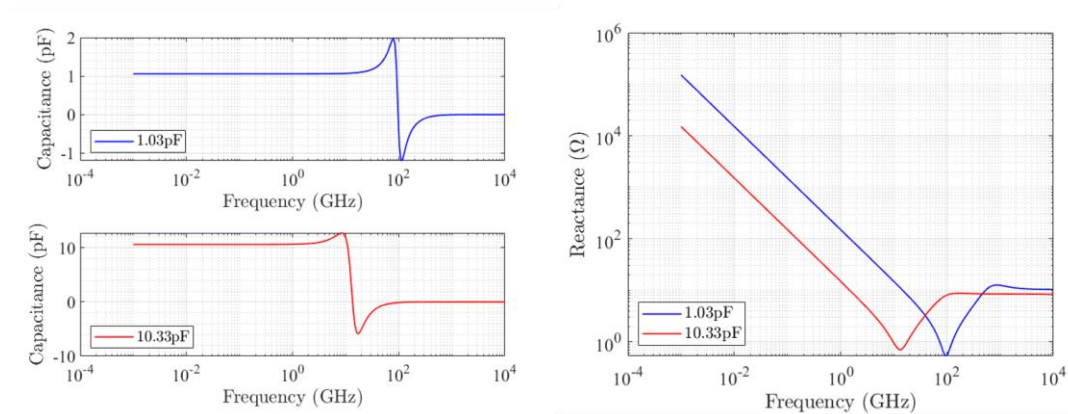
Their capacitance is proportional with their geometrical parameters (length  $L$  and width  $W$ ), as well as the number of metal layers involved. The more layers involved, the greater its capacitance will be for a fixed size. The PDK offers two families of capacitors: MOM (metal-oxide-metal) and APMOM. A brief capacitance density comparison is made between various available capacitors named with a letter from A to G using layers from M2 and C5.

	APMOM A	APMOM B	APMOM C	APMOM D	APMOM E	APMOM F	APMOM G
Cap. density (fF/ $\mu\text{m}^2$ )	7.6	7.1	3.6	3.1	2.5	1.1	0.7
Voltage (V)	1.8	2.5	3.3	4	5	7	10

**Table 9: Capacitance density comparison between various PDK MOM and APMOM capacitors**

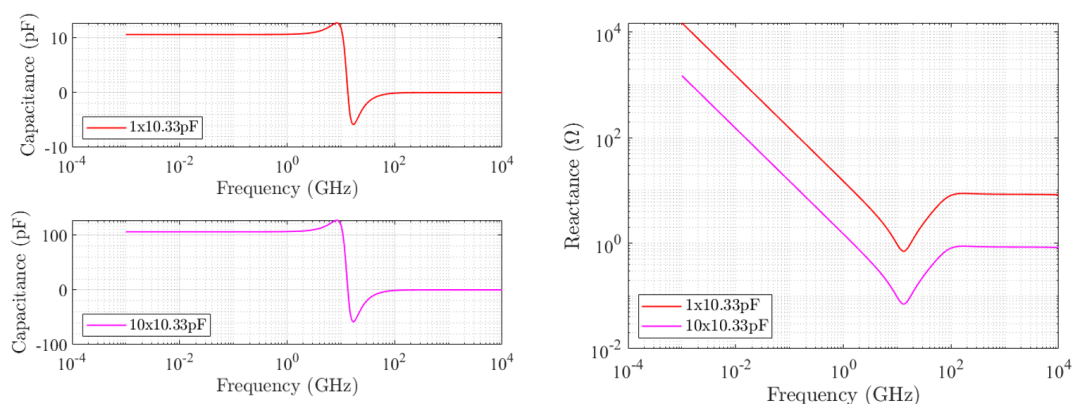
It is clear that a trade-off between the capacitance density and voltage-handling of a capacitor needs to be made. In our case, the supply voltage is only 0.8V, and so any listed capacitor can be used. For compact applications, low-voltage APMOM capacitors seems to be good candidates. Another key characterization metric of lumped components is the self-resonance frequency (SRF). The PDK describes non-idealistic component models than can exhibits different behaviours in very high frequencies. The impedance of the capacitor  $Z_C$  is defined as

$$Z_C = \frac{1}{jC\omega} \quad (15)$$



**Figure 45: SRF visualisation of two capacitors of different values, observable over the capacitance and the reactance profile (1/2)**

Where  $j$  is the complex number defined as  $j^2 = -1$ ,  $C$  is the capacitance and  $\omega$  is the pulsation. This SRF needs to be located at least at a high enough multiple of the operating frequency (or  $SRF \gg f_{RF}$ ), in order to guarantee a steady capacitor behavior. Large capacitors are useful when used as DC-block in multi-stages architectures to make the biasing conditions independent from one stage to another. A large value is required to lower its impedance and so its losses. However, a large capacitance value will lower the SRF, so a trade-off is to find. Similarly, decoupling capacitors are used to filter high frequencies in biasing paths, to avoid the RF modulation of DC signals, which can cause voltage stress on transistors. In Figure 45, the SRF is shifted from 96.4GHz to 13.1GH from when respectively using a  $\approx 1\text{pF}$  and  $\approx 10\text{pF}$  1.8V APMOM capacitor. In practice, instead of having very large capacitors, many are placed in parallel. If a bank of unit capacitors is used, it is shown in Figure 46 that the SRF observable over the capacitance and reactance of the capacitor remains unaffected.



**Figure 46: SRF visualisation of two capacitors of different values, observable over the capacitance and the reactance profile (2/2)**





## Chapter 3: RF FRONT-END

The most critical part of transceivers is the RF front-end. Operating at high frequencies, its performances will have a significant impact over the transceiver overall behaviour. Since it is located right after the antenna, the power-handling (for the power amplifier (PA)) and its noise contribution (for the low noise amplifier (LNA)) have to be studied with a great care to ensure the adequate operation of the chip.

Both LNA and PA will hence be studied one at a time in this chapter. A state-of-the art analysis was conducted for each amplifier in order to anticipate standalone performances we could expect, at the desired design frequency.

After that, the unidirectional elementary amplifying cell will be analysed to understand the capacitive neutralization concept, which will be at the heart of our PA-LNA design. The transistors involved will also be characterized.

The bidirectional core cell will then be presented, as well as the realized matching networks, interconnecting the two amplifying stages.

Finally, measurements will be presented with the realization of the two following tape-outs

- RUN1: "K2000" (PA-LNA)
- RUN2: "TESTCHIP22" (PA-LNA discussed in this chapter, and the RX analog baseband chain, the latter being discussed in Chapter 4)

As a conclusion, the performances of our bidirectional RF front-end will be compared with the proposed specifications, and with bidirectional amplifiers found in the literature.

### 3.1 BASICS

#### 3.1.1 MILLIMETER-WAVE TRANSCEIVERS FRONT-END MODULE OVERVIEW

A front-end module is usually composed of a RF PA (within the TX path) and a RF LNA (within the RX path). Usually, conventional bidirectional RF front-ends physically separate the TX from the RX path and address them alternatively in time, using most of the time a commuted element, as in Figure 47. This addressing operation can either be implemented with or without a single pole double throw (SPDT) switch as in Figure 48 [36] [37].

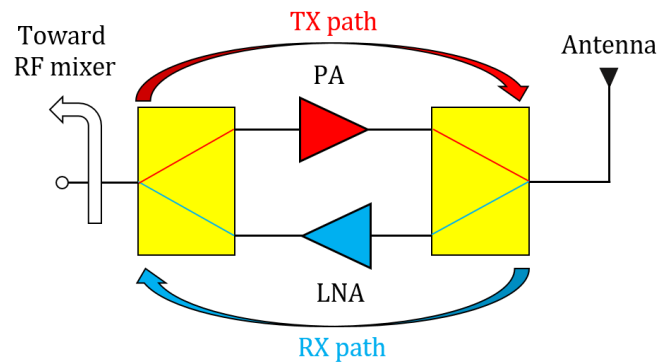


Figure 47: Illustration of a conventional way of building the RFFE in multi-elements systems

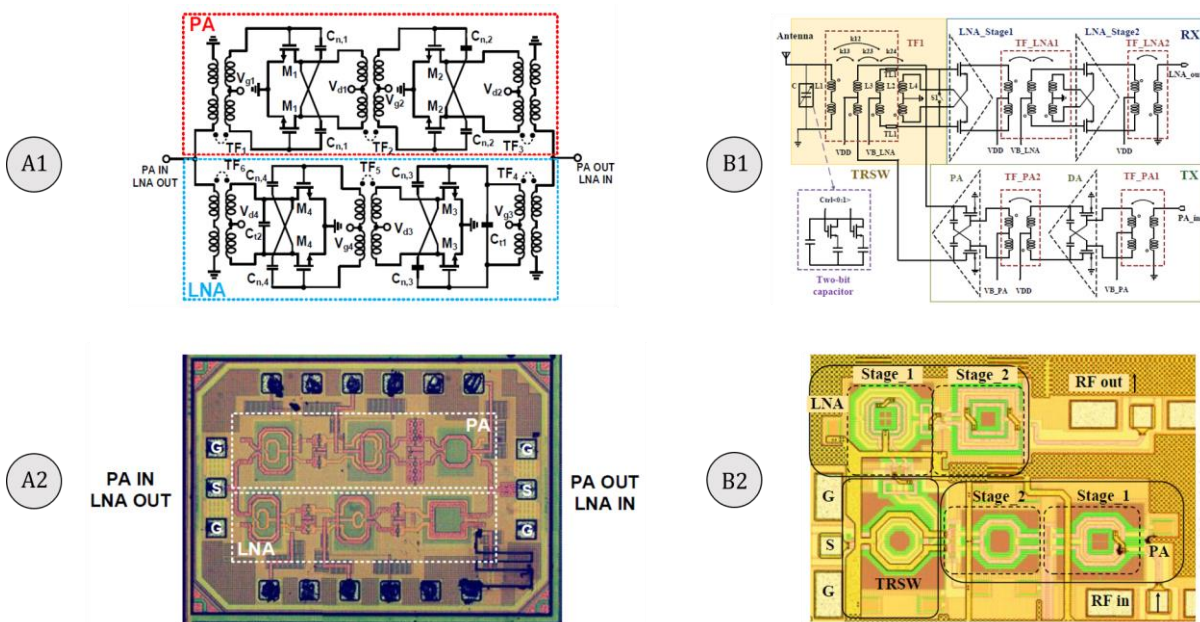


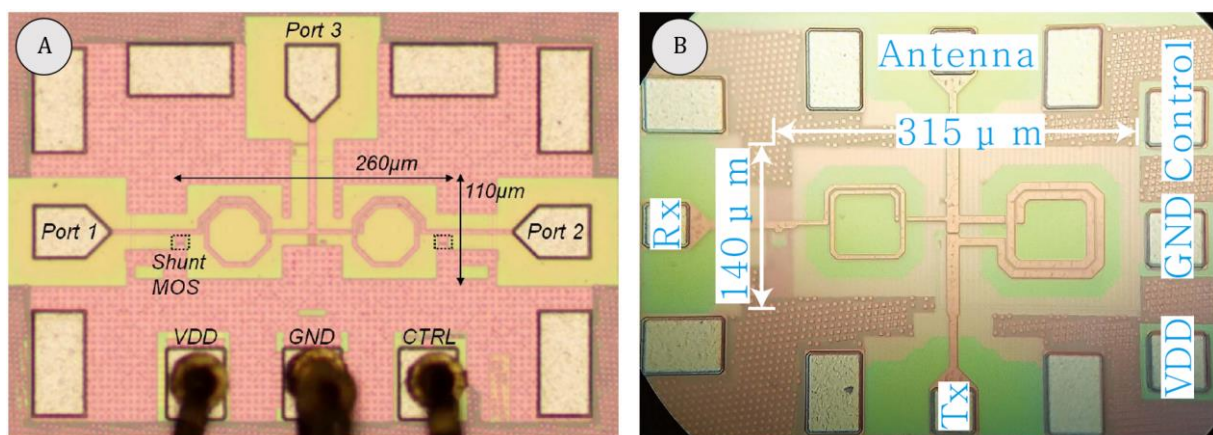
Figure 48: Complete schematic of a switchless bidirectional PA-LNA (A1) and associated microphotograph (A2) [37], schematic of a PA and a LNA including a TRSW (B1) and associated microphotograph (B2) [36]

Again, in order to limit the number of antennas, SPDT switches hence became crucial building blocks in phased array systems. A brief overview of RF SPDT performances was conducted in Table 10 with examples taken from the literature.

	EuMC (2018) [38]	EuMC (2021) [39]	LMWC (2019) [40]	IWS (2021) [41]	LMWC (2020) [42]	RFIC (2018) [43]	SiRF (2021) [44]
Technology	65nm CMOS	130nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm SOI
Insertion loss (dB)	1.8	1.5	0.7 – 1.1	<1.9	2.8	<1.9	0.8
Frequency (GHz)	28	30 – 46	25 – 30	35 – 45	21 – 36	1 – 28	24 – 31
Core area (mm <sup>2</sup> )	0.029	0.050	0.043	0.009	0.035	0.010	0.002

**Table 10: RF CMOS SPDT literature overview**

Many works were conducted in order to improve the figure-of-merits of SPDT switches through the improvement of their port-to-port isolation, power-handling, insertion losses, as well as their compactness. Indeed, SPDT subsequent induced losses at mmW frequencies will affect both TX and RX chains and would also require a dedicated matching network [41] [44] including large inductors noticeable in Figure 49 (A and B). The order of magnitude of insertion losses is roughly around 1.5dB at mmW frequencies.



**Figure 49: Microphotograph of two 65nm CMOS SPDT switches (A) from [38] and (B) from [40]**

### 3.1.2 POWER AMPLIFIERS

#### 3.1.2.1 Figure-of-merit

The behavior of power amplifiers (PA) can be characterized by the mean of five main metrics

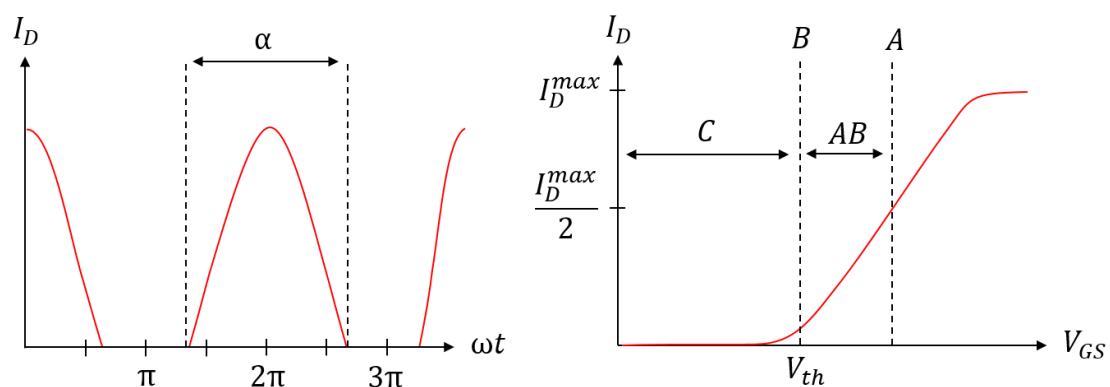
- The power-added efficiency (*PAE*)
- The power gain (*G<sub>P</sub>*)
- The output power 1dB compression point (*OCP<sub>1dB</sub>*)
- The maximum (or saturated) output power (*P<sub>sat</sub>*)
- The linearity (*OIP3, AM/PM, AM/AM* distortions)

In this section, these metrics will be defined.

First of all, both power-added efficiency (PAE) and efficiency ( $\eta$ ) are defined as follows

$$PAE(\%) = \left( \frac{P_{out} - P_{in}}{P_{DC}} \right) \times 100 \quad \eta(\%) = \left( \frac{P_{out}}{P_{DC}} \right) \times 100 \quad (16)$$

Where  $P_{out}$  is the output power,  $P_{in}$  the input power and  $P_{DC}$  is the DC power. In other words, the two efficiency indicators are optimized when the output power is maximized at a reduced DC power. The maximum reachable theoretical efficiency  $\eta_{max}$  depends on the biasing conditions of the power amplifier regardless the size nor technology of the transistors involved, as in Figure 50. As the gate-source potential  $V_{GS}$  increases, the conduction angle  $\alpha$  is widened to reach  $2\pi$  (Figure 50 left) in a case of a class-A amplifier (Figure 50 right).



**Figure 50: Illustration of the impact of the conduction angle using a sine waveform (left) and amplifiers design classes identification over a  $I_D = f(V_{GS})$  plot**

In a multi-stage amplifier design, a combination of design classes can be used in order to optimize the overall efficiency, but at a cost of higher magnitude and phase distortions leading to an EVM deterioration [45]. Those four linear classes, illustrated in Figure 50, can be listed as in Table 11 comparing the theoretical maximal efficiency  $\eta_{max}$  of various linear amplifier classes [46].

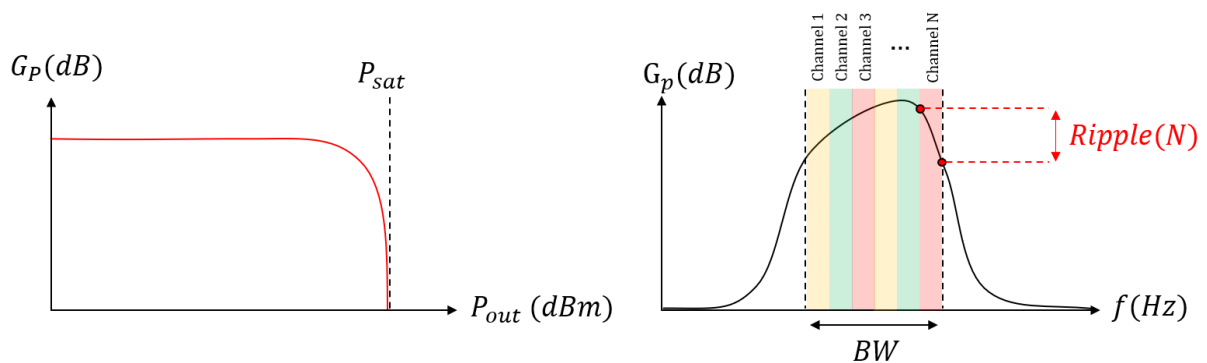
Linear design classes	Conduction angle $\alpha$	$\eta_{max}$
A	$2\pi$	50%
AB	$\pi < \alpha < 2\pi$	$50\% < \eta < 78.5\%$
B	$\pi$	78.5%
C	$\alpha < \pi$	$78.5\% < \eta < 100\%$

**Table 11: Linear PA operating classes in function of the conduction angle and corresponding efficiency**

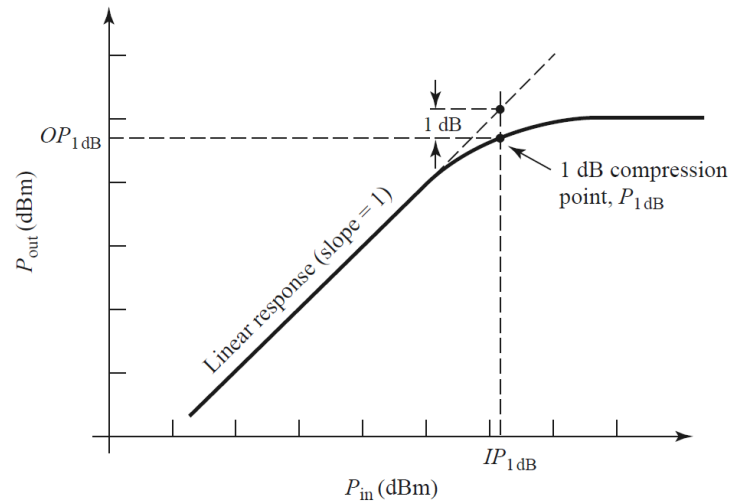
Power-handling is also a critical aspect of power amplifiers design as they are located at the end of the TX RFFE, where the power level presented at its input is at its highest level. The power gain  $G_P$  is defined as the ratio between the input and output power as

$$G_P = \frac{P_{out}}{P_{in}} \quad (17)$$

When active devices saturate, they are no longer able to provide more power at the output, reaching their saturated output power value ( $P_{sat}$ ) while the input power keeps on increasing, resulting in the power gain  $G_P$  drop as in Figure 51. This power gain can also vary across a given bandwidth. Across each channel, the gain can vary resulting in gain ripple. In our case, the gain ripple was evaluated in the wider channel BW configuration of 400MHz.



**Figure 51: Illustration of the power gain with respect to the output power (left) and illustration of gain ripple with respect to frequency (right)**

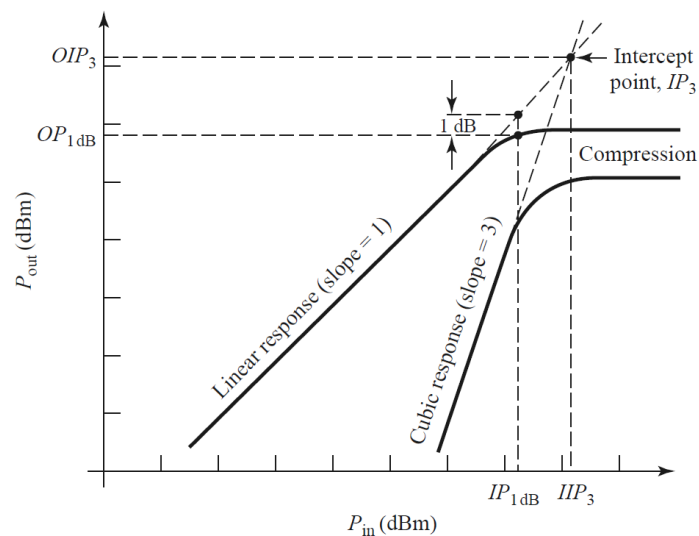


**Figure 52: Definition of the 1dB compression point for a non-linear amplifier [21]**

The input- and output-referred compression points  $IP_{1dB}$  (or  $ICP_{1dB}$ ) and  $OP_{1dB}$  (or  $OC P_{1dB}$ ) are graphically defined Figure 52. From this plot, a relationship between  $IP_{1dB}$  and  $OP_{1dB}$  can be expressed as

$$OP_{1dB} = IP_{1dB} + (G_p - 1) \quad (18)$$

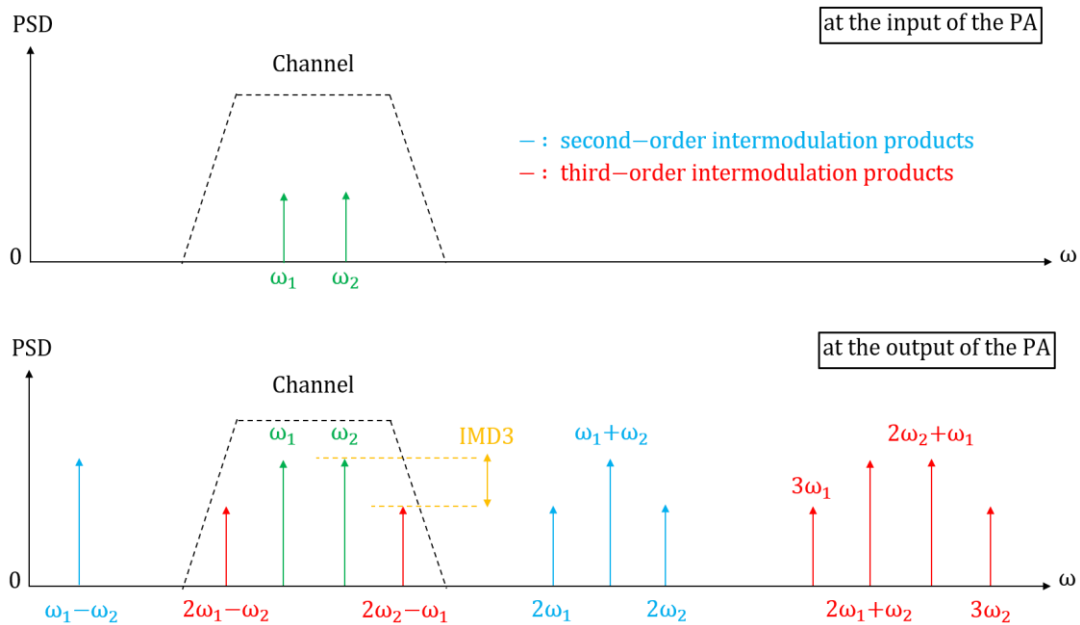
As the input power gets too close to  $IP_{1dB}$ , the amplifier will no longer respond linearly. In telecommunication systems, a certain margin – or back-off (BO) – is taken to guarantee a good linearity, and whose value depends on the modulation scheme involved. When two tones are presented at the input of a power amplifier, intermodulation products will be generated at



**Figure 53: Third-order intercept diagram for a non-linear component [21]**

the output and will deteriorate the performances of the TX chain. Finally, the linearity can be quantified using multiple indicators such as AM/AM and AM/PM (respectively amplitude and phase single-tone distortion).

The cubic response as a slope of three, meaning that for a 1dBm power increase in the amplified fundamental tones, the third-order intermodulation products power will increase by 3dBm. At some point, the amplitude of intermodulation products will get close to the amplitude of the fundamentals, and it will be impossible to discern them from one another. In the frequency domain, the spectral power density can be illustrated as in Figure 54 where the spectrum is represented at the input (top) and at the output (bottom) of a power amplifier.



**Figure 54: Non-linear PA input (top) and output (bottom) spectrum of second- and third-order two-tone intermodulation products with  $\omega_1 < \omega_2$**

The output spectrum is composed of harmonics  $h$  defined as such

$$h(m, n) = m\omega_1 + n\omega_2 \quad (n, m) \in \mathbb{Z}^2 \quad (19)$$

While the order of a product  $o(m, n)$  of a specific harmonic is defined by

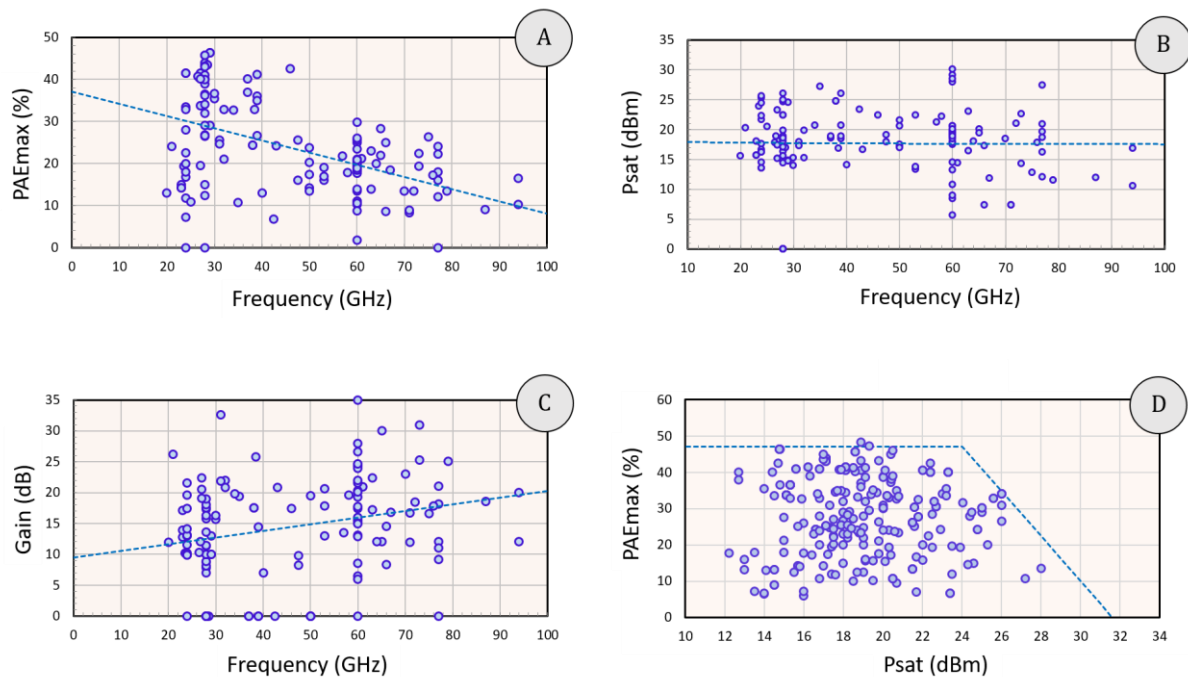
$$o(m, n) = |m| + |n| \quad (n, m) \in \mathbb{Z}^2 \quad (20)$$

The two-tone third-order intermodulation distortion (IMD3) is also defined in yellow in Figure 54 as the power ratio in  $dB_c$  between a fundamental and a third-order intermodulation product.



### 3.1.2.2 State-of-the art

The power amplifier to be designed in this thesis will operate within the 5G FR2-1 n260 band, whose center frequency is set to 38.5GHz. A state-of-the art comparison was conducted in order to be aware of the performances we can expect from trends, in the case of unidirectional mmW CMOS integrated standalone PAs, as in Figure 55.



**Figure 55: CMOS PA PAEmax (A), Psat (B) and Gain (C) trends, and device limitation (D) [47]**

A very complete bibliographical study of PA trends is available in [47] where performances of a large number of PAs from various technologies taken from the literature are compared. Considering the scope of our thesis work, the focus was made on the performance trends of CMOS-only PAs at mmW frequencies. These graphs allowed to identify performance trends over the main CMOS PA metrics at 40GHz as

- $PAEmax_{trend} \approx 25\%$  from Figure 55 (A)
- $Psat_{trend} \approx 17.5dBm$  from Figure 55 (B)
- $Gain_{trend} \approx 14dB$  from Figure 55 (C)

Moreover, the last graph Figure 55 (D) allows to identify the technological PAE limit of state-of-the art mmW CMOS PAs, operating between 20 and 50GHz, of roughly 47%.

### 3.1.3 LOW NOISE AMPLIFIERS

#### 3.1.3.1 Figure-of-merit

Low noise amplification is another crucial concept in telecommunication systems. Its role is to perform a first amplification over very weak signals coming from transmitters after being greatly attenuated during the free-space propagation.

As we saw in Chapter 2 the noise contribution of the first RF block is prominent and will highly affect the overall transceiver performances. The main LNA performances indicators can be listed as

- The noise figure ( $NF$ )
- The linearity ( $ICP1$  and  $IIP3$ )
- The gain ( $S_{21}$ )
- The bandwidth ( $FBW$ )

They are two ways to optimize  $NF_{min}$  (and hence  $NF$ ). On the one hand, the geometrical size of a transistor has an optimum to reduce the transistor noise contribution at a given frequency. On the other hand, the biasing condition can also exhibit a noise optimum.

The bandwidth can be characterized through an absolute metric with the -3dB BW, or a relative metric with the fractional bandwidth ( $FBW$ ) defined as

$$FBW = \frac{f_{max} - f_{min}}{f_0} \quad (21)$$

It gives an indication of the frequency range within which the amplifier can operate, as a multiple of the operating frequency. Wideband (or reconfigurable bands) LNAs can offer the flexibility of being compatible with multiple 5G FR2-1 bands.

The small-signal voltage gain  $S_{21}$  is defined within the scattering parameters matrix for a 2-ports network configuration, where the S-matrix  $S$  is defined as follows

$$S = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \quad (22)$$

$S_{11}$  and  $S_{22}$  are respectively the input and output voltage reflection coefficient,  $S_{21}$  is the forward voltage gain, and  $S_{12}$  is the reverse voltage gain.

They can be defined as follows

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \Rightarrow \begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 \\ b_2 = S_{21}a_1 + S_{22}a_2 \end{cases} \quad (23)$$

Where  $a_1$ ,  $a_2$  and  $b_1$ ,  $b_2$  are respectively the incident and reflected waves illustrated in Figure 56 defined in [21] and [48].

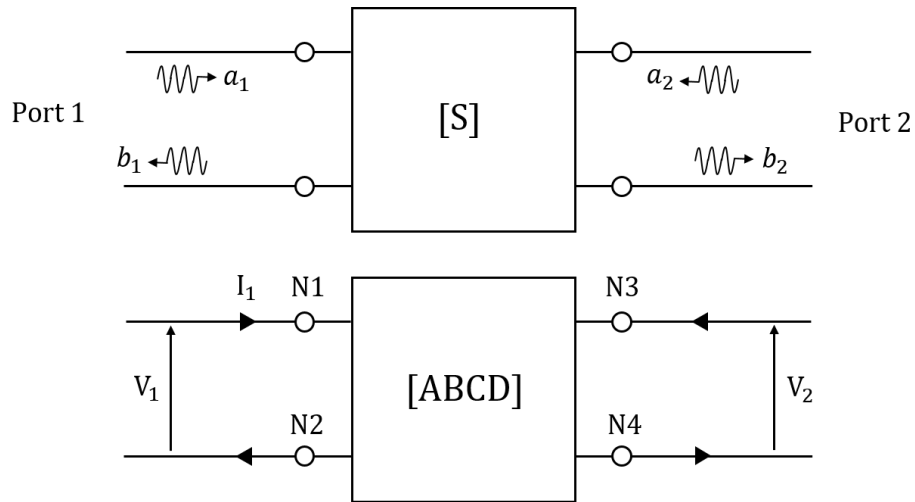


Figure 56: Quadripole definition using the S-matrix (top) and the ABCD matrix (bottom) [21]

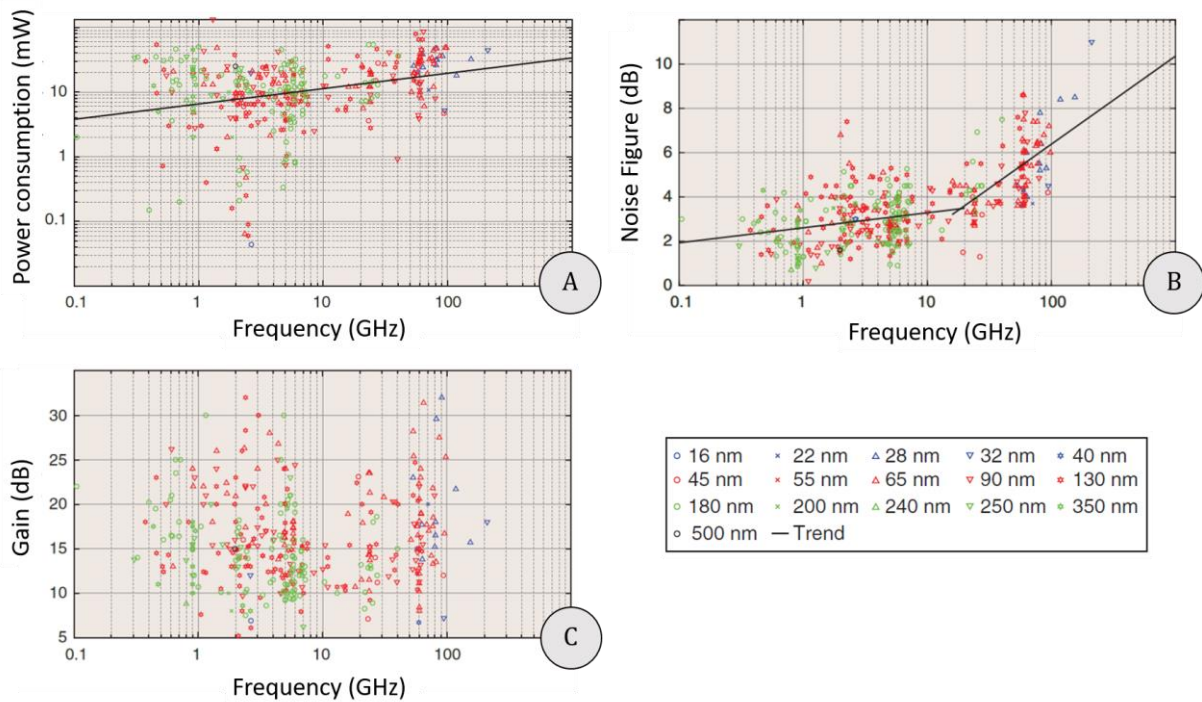
From (23), it is possible to define the scattering parameters as functions of the incident and reflected waves  $\{a_i\}_{i \in \llbracket 1,2 \rrbracket}$  and  $\{b_i\}_{i \in \llbracket 1,2 \rrbracket}$  as

$$\begin{aligned} S_{11} &= \left. \frac{b_1}{a_1} \right|_{a_2=0} \\ S_{12} &= \left. \frac{b_1}{a_2} \right|_{a_1=0} \\ S_{21} &= \left. \frac{b_2}{a_1} \right|_{a_2=0} \\ S_{22} &= \left. \frac{b_2}{a_2} \right|_{a_1=0} \end{aligned} \quad (24)$$

S-parameters are widely used in the small-signal electrical characterization of integrated RF circuits. The remaining figure-of-merits were defined in the previous sections.

## 3.1.3.2 State-of-the art

The same study was conducted over unidirectional standalone mmW CMOS integrated standalone LNAs taken from the literature, in order to identify a trend of achievable performances as in Figure 57, crucial to establish realistic system specifications.



**Figure 57: CMOS LNA power consumption (A) noise figure (B) and gain (C) versus the center frequency including trends - when defined - using various technology nodes from 16nm to 500nm [49]**

These plots allowed to isolate performances trends of CMOS LNAs at 40GHz as

- $P_{dc\_trend} \approx 16\text{mW}$  from Figure 57 (A)
- $NF_{trend} \approx 5\text{dB}$  from Figure 57 (B)
- $Gain_{trend} \text{ NONE}$  from Figure 57 (C)

Another remarkable thing about these plots is the linear degradation of power consumption due to the complexity of making efficient high frequency amplifiers (Figure 57 (A)). It also indicates that actually two NF trends can be identified – below and above 20GHz – where the high frequency gain is obtained using numerous stages. The noise being mainly caused by transistors at these frequencies, it would results in a higher NF [49].

## 3.2 UNIDIRECTIONAL NEUTRALIZED DIFFERENTIAL PAIR

### 3.2.1 CMOS COMMON-SOURCE TRANSISTORS BIASING

Before considering the neutralized differential pair, a study was conducted in order to determine the biasing conditions of transistors used in the PA and the LNA designs, discussed in the next section. With this intent, we considered the two schematics in Figure 58.

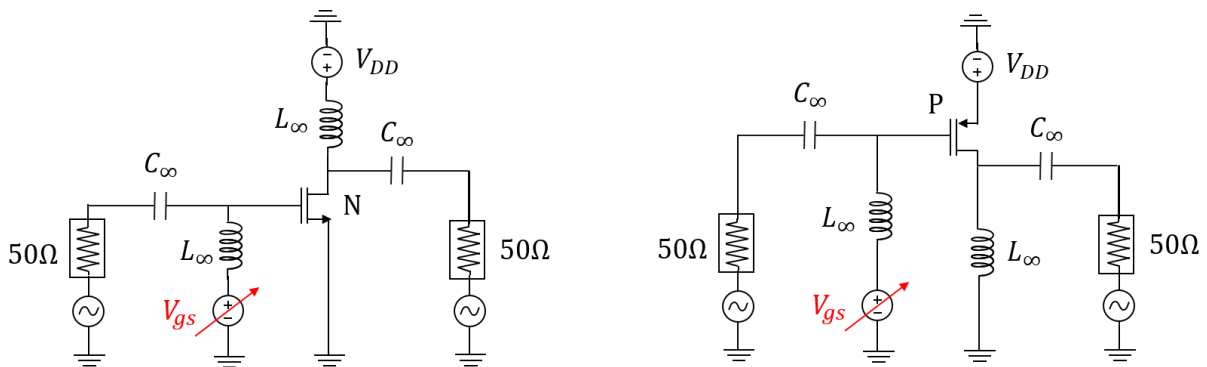


Figure 58: NMOS (left) and PMOS (right) characterisation test-bench used to plot Figure 59

Variations were applied to the gate-source potential (in red) and three indicators were plotted: respectively the linear (drain or source) current density  $J$ , the minimum noise figure  $NF_{min}$ , and the maximum available gain  $G_{max}$  at 38.5GHz. The current density  $J$  is defined as the ratio between a current and a unit of length (here, the width  $W$  of a transistor),

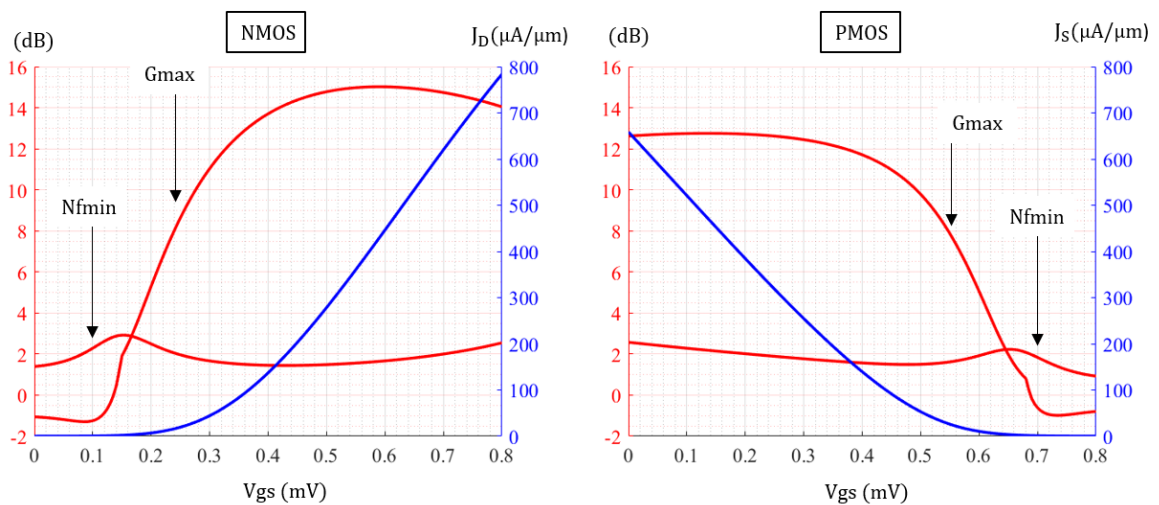


Figure 59: PMOS (right) and NMOS (left) linear current density  $J$ ,  $G_{max}$  and  $NF_{min}$ , with respect to the variation of the gate-source potential  $V_{gs}$

$NF_{min}$  and  $G_{max}$  respectively depict the minimal achievable noise figure  $NF$  and the maximum power gain  $G_p$  under optimal input/output impedance matching conditions. As we can see from Figure 59, the optimum  $NF_{min}$  for PMOS transistors used within LNA designs is reached for lower value of  $J$  (typically  $\approx 150\mu A/\mu m$ ) than for the gain optimum of NMOS transistors used within PA designs (typically  $\approx 300\mu A/\mu m$ ).

### 3.2.2 NMOS DIFFERENTIAL PAIR AND CAPACITIVE NEUTRALIZATION

We now consider a schematic of a NMOS neutralized differential pair as in Figure 60, which will be the base concept to understand our bidirectional amplifier core cell. Different colours (purple and yellow) mean an out-of-phase condition. The neutralization capacitor  $C_{neutr}$  can either be an integrated capacitor, or cold NMOS/PMOS transistors, using their off-state capacitors. The performances comparison between available options can highlight the best suitable neutralization component to use in the design.

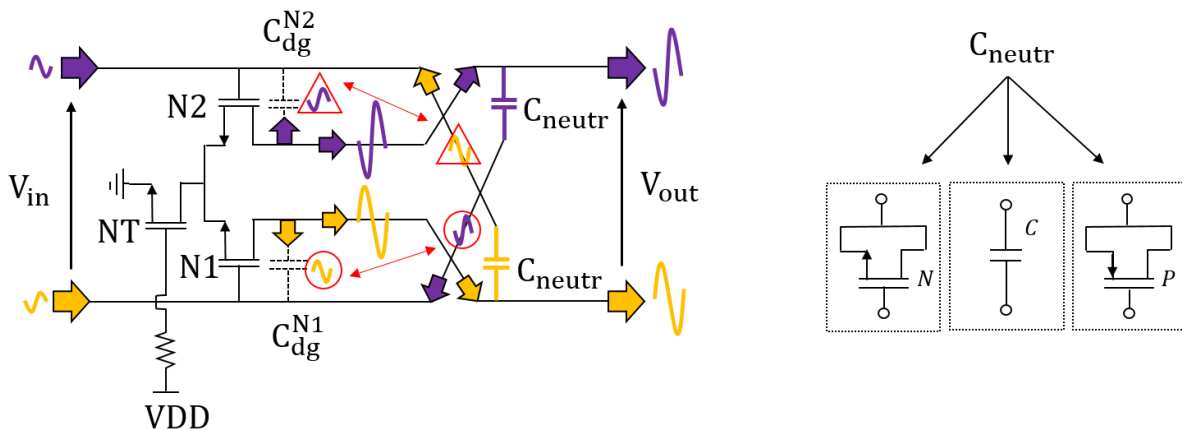


Figure 60: Illustration of the neutralization principle of a NMOS differential pair

The neutralization of the Miller effect analysis is conducted in [50] demonstrating that neutralization capacitor  $C_{neutr}$  must verify the relationship

$$C_{neutr} = C_{dg}^{N1} = C_{dg}^{N2} \quad (25)$$

The addition of  $C_{neutr}$  will constitute a positive feedback loop that need to exactly counterbalance the intrinsic negative feedback caused by the drain-gate intrinsic capacitors  $C_{dg}^{N1}$  and  $C_{dg}^{N2}$  substituting part of the amplified signal and bringing it back to the input. A wrong value for this capacitor will lead to either performances deterioration, or instability.

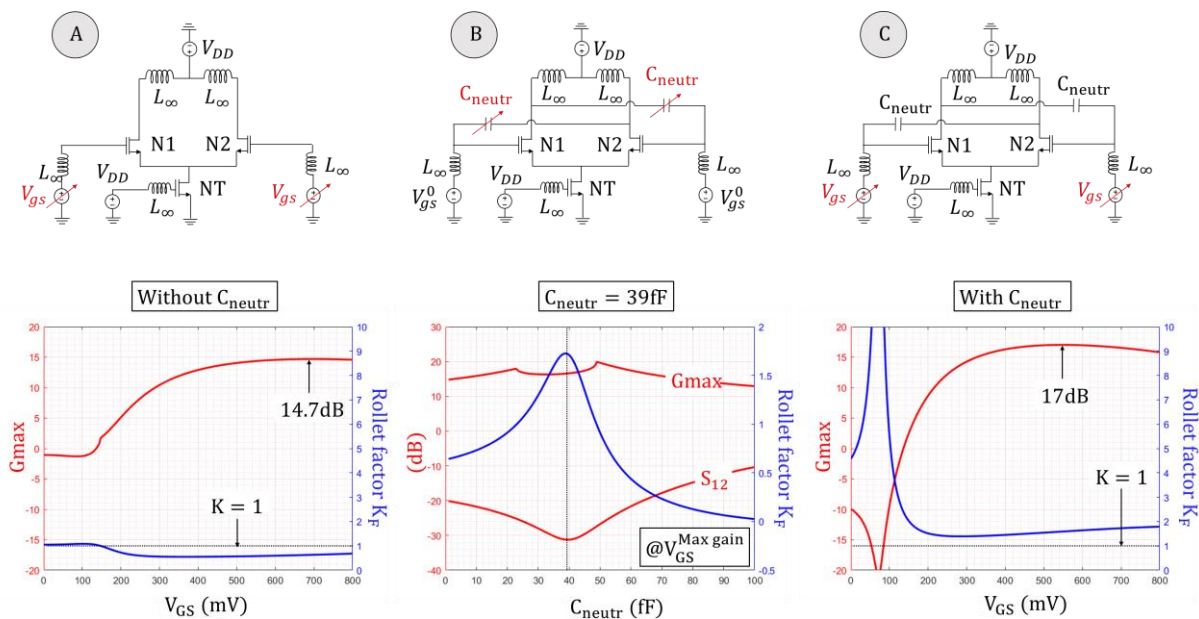
The maximum available gain  $G_{max}$  is defined in [24] in a case of a two-ports network as

$$G_{max} = MAG = \left| \frac{S_{21}}{S_{12}} \right| (K_F - \sqrt{K_F^2 - 1}) \quad (26)$$

The stability factor  $K_F$  (or Rollet's factor) is also a crucial small-signal indicator that characterises the stability of a system, and is defined in [24] as

$$K_F = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}||S_{21}|} = \frac{2\Re(Z_{11})\Re(Z_{22}) - \Re(Z_{12}Z_{22})}{|Z_{12}Z_{21}|} \quad (27)$$

The *Rollet criterion* states that a stability factor  $K_F$  strictly greater than one implies unconditional stability. In other words, stability no matter what impedances that could possibly be presented at the input and output of the device. In Figure 61 (A) we can observe that as soon the NMOS transistor gate-source potential gets close to the threshold voltage, the transistor gets into an instability state. In (B) we added a capacitive element, using an ideal capacitor and swept its value. As we can see,  $K_F$ ,  $G_{max}$  and  $S_{12}$  are maximized for a specific value of  $C_{neutr}$  with the value 39fF for transistors whose width is 180 $\mu$ m. Finally, it is checked in (C) that unconditional stability is verified for any gate-source potentials. Neutralized differential pairs are widely used in the design of 5G mmW amplifiers [51] (PA) [52] (LNA), and will be the base principle of our bidirectional amplifier design.



**Figure 61: Differential pair  $G_{max}$  (A), neutralized differential pairs  $G_{max}$  and Rollet factor (B) (C) with respectively respect to  $V_{gs}$ ,  $C_{neutr}$  and  $V_{gs}$  respectively, at 38.5GHz**

### 3.3 DESIGN OF A MMW BIDIRECTIONAL AMPLIFIER

#### 3.3.1 SPECIFICATIONS

First of all, specifications of each amplifier were established in Table 12. These specifications will be compared with the actual performances of the bidirectional amplifier which themselves will be compared with the state-of-the art, at the end of this chapter.

PA	
Power gain (dB)	14
Gain ripple (dB)	$\pm 1$
OIP3 (dBm)	17.3
OCP1 (dBm)	4.9
IMD3 (dBc)	35
AM/PM distortion ( $^{\circ}$ )	2
BW (GHz)	3.6
Input matching (dB)	-15
Reverse isolation (dB)	-15
LNA	
Power gain (dB)	23
BW (GHz)	3.6
Gain ripple (dB)	$\pm 1$
NF (dB)	6
IIP3 (dBm)	-18
Input matching (dB)	-15
Output matching (dB)	-15
Reverse isolation (dB)	-15

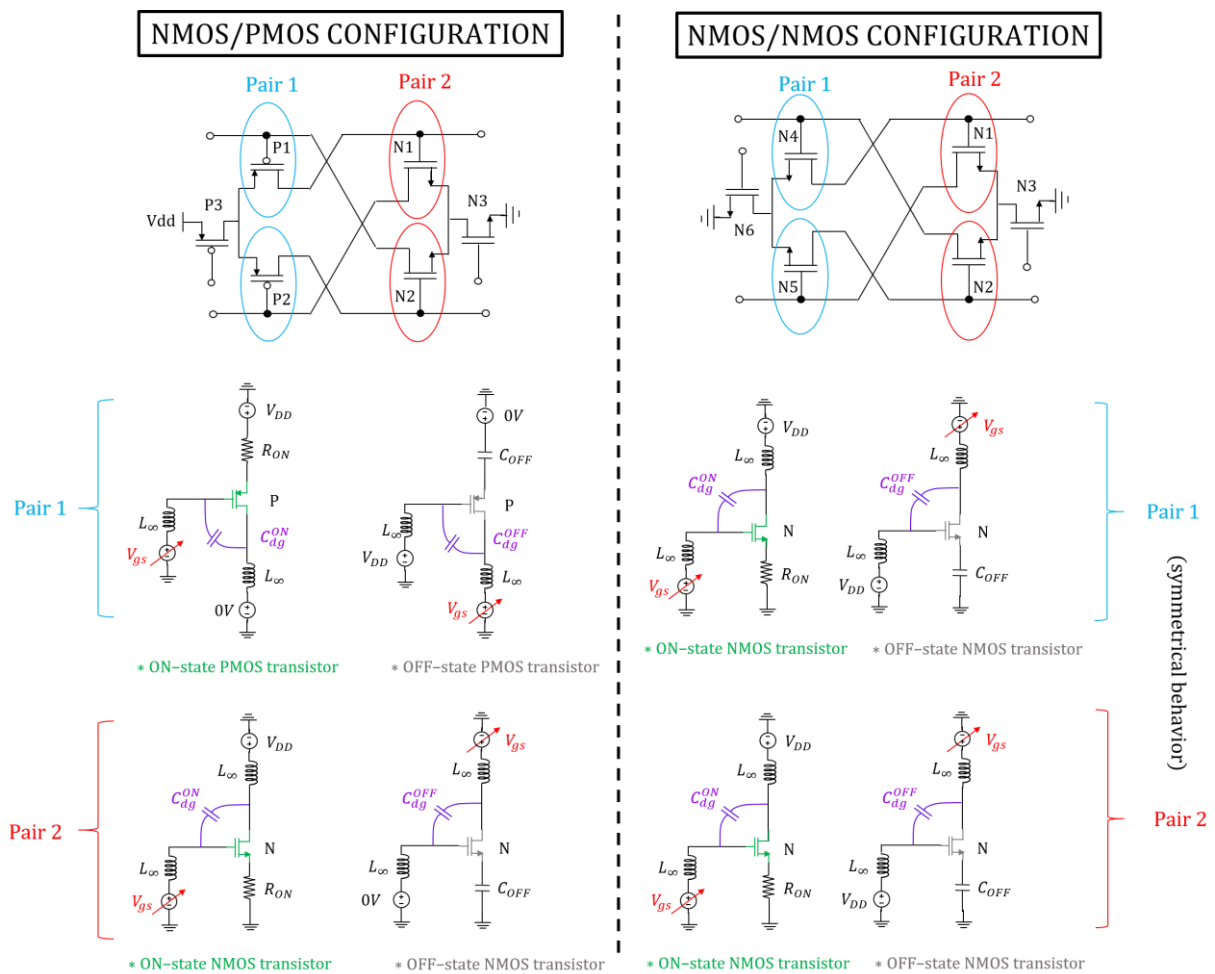
**Table 12: Specification table of the PA and LNA**

Within the next section, the core circuitry of our bidirectional amplifier, based on the previous analysis, will be described and characterized.



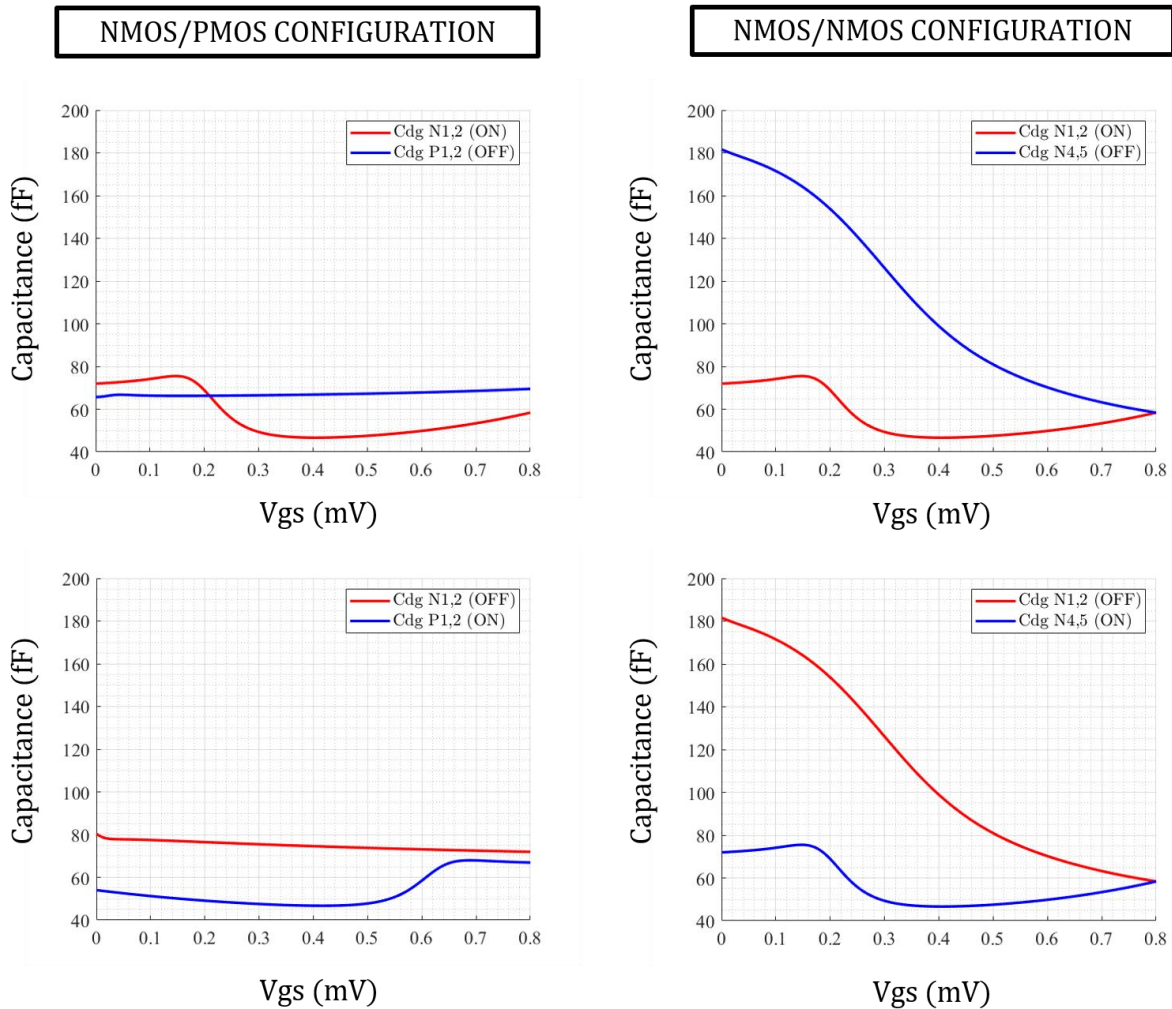


It appears that the best trade-off in terms of number of fingers for the PMOS transistors is roughly 60. In the literature, the most compact bidirectional mmW amplifier with the best performances are mostly based on interconnected differential pairs [53] [54]. The idea of using CMOS transistors was taken into account when studying the variation of the non-linear variation of intrinsic capacitances  $C_{dg}$  induced by biasing. Indeed, it is mandatory to understand those variations, because as we saw, the value of the neutralization capacitor  $C_{neutr}$  needs to have a very specific value otherwise it would lead to problems brought up in the previous section. The electrical nodes sharing implies the variation of biasing conditions over the two modes. A simplistic test-bench was implemented in order to observe this impact over the value of the on-state and the off-state transistors  $C_{dg}$  within the NMOS/NMOS and NMOS/PMOS configuration as in Figure 64.



**Figure 64: Description of the test-bench used to plot the variation of NMOS and PMOS  $C_{dg}$  with respect to the application of various voltage potentials over their three terminals, within the NMOS/PMOS (left) and the NMOS/NMOS configuration (right)**

As a result, the on- and off- $C_{dg}$  were plotted with respect to the application of various source, gate and drain potentials that will be applied due to the specific connections implied by this topology, and will differ depending on the selected operating mode.



**Figure 65: Non-linear variations of the intrinsic capacitance  $C_{dg}$  with respect to the biasing implied by the interconnections of the schematic in the NMOS/PMOS (left) and the NMOS/NMOS (right) configuration**

In the NMOS/NMOS configuration, the differential pairs are sized the same way, but if needed, one pair can be constituted of smaller transistors, and an extra capacitor has to be added between the drain a gate terminal to boost the smaller intrinsic capacitance  $C_{dg}$ . The analysis still remains the same. The linearity requirements can be more demanding over the PA transistors than the LNA ones, and larger transistors could be expected within the PA design. As we see, less capacitance fluctuation is observable in the case of the CMOS differential pair, resulting in a better neutralization considering the neutralization condition exhibited in (25).

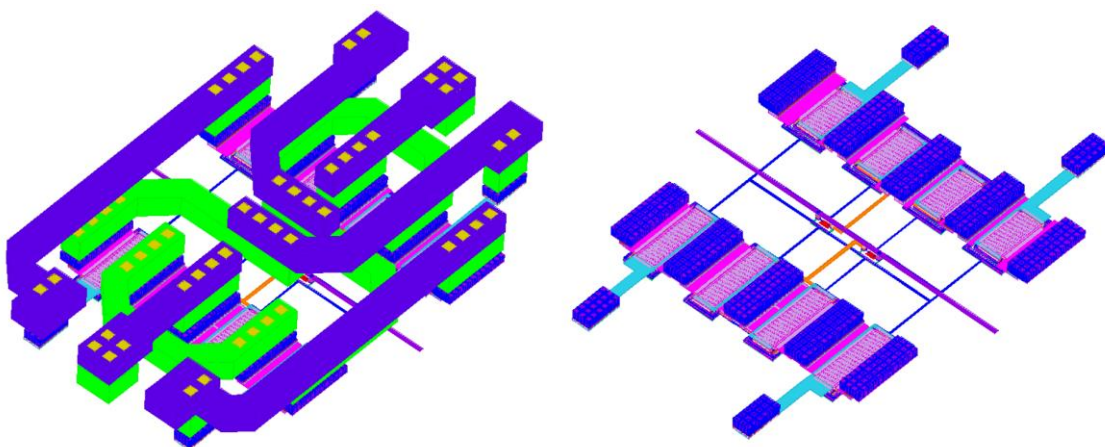
The difference between the on- and off- $C_{dg}$  are more than three times bigger in the NMOS/NMOS configuration than in the NMOS/PMOS configuration, in the worst case. The relevancy of the usage of NMOS/PMOS transistors was also demonstrated through the complete work published in 2022 at ISSCC – during the design of our amplifier – based on the same topology, exhibiting very promising results, at reduced silicon surface. It also states a higher efficiency with a 2dB increase of saturated power and 25% PAE increase, compared with the NMOS/NMOS architecture [54].

The number of fingers of LNA transistors fixed to 60. The driver stage uses transistors twice as small in order to reduce the overall DC power. The size of the transistors of the two amplification stages were reported in Table 13.

	Transistors width W ( $\mu\text{m}$ )					
	N1	N2	N3	P1	P2	P3
Main stage	180	180	360	135	135	270
Driver stage	90	90	180	67	67	134

**Table 13: Transistors sizing summary of the two amplifiers (main and driver stages)**

The finger width ( $W_f$ ) of PMOS transistors was set to 750nm, while the width of NMOS transistors was set to 1 $\mu\text{m}$  to respectively optimize the noise figure, power gain. The layout of the core main amplifier was then conducted as in Figure 66. Figure 66 (left) describes the full



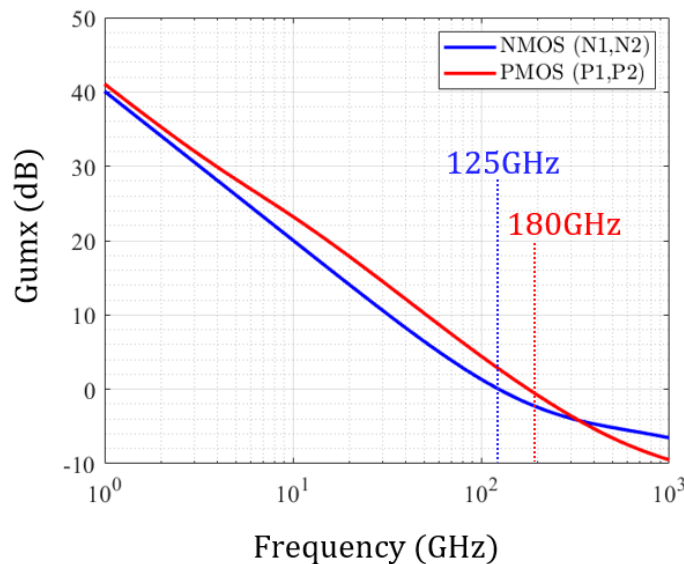
**Figure 66: 3D view of the main stage amplifier core cell (left) without QA and QB layers (right)**

3D-view of the main stage core cell, while Figure 66 (right) describes the same cell without the top thick layers, in order to have a better view of the transistors using bottom metal layers. The *gain* transistors are located on the external sides while the tail transistors are in the middle, and sized two times bigger than *gain* transistors in order to reduce their on-state resistance, and hence enhance the output voltage swing. Thick metal layers were used (QA and QB) to reduce the resistivity of the RF path.

The maximal frequency  $f_{max}$  of the NMOS and PMOS transistors was plotted in Figure 67 when NMOS are biased to optimize the gain and the PMOS to optimize the noise figure. For NMOS transistors  $f_{max}$  is equal to 125GHz while for PMOS, it is equal to 180GHz.  $G_{umx}$  is defined as the unilateral power gain used in the definition of  $f_{max}$  defined in [24] as

$$G_{umx} = U = \frac{\left| \frac{S_{21}}{S_{12}} - 1 \right|^2}{2 \left( k \frac{S_{21}}{S_{12}} - \Re \left( \frac{S_{21}}{S_{12}} \right) \right)} \quad (28)$$

And defines  $f_{max}$  as the frequency at which  $G_{umx}$  is equal to 0dB as in Figure 67.



**Figure 67: NMOS and PMOS  $f_{max}$  identification using the maximal unilateral gain ( $G_{umx}$ ), of the transistors used in the design of the main amplification stage**

Now that the core amplifier cell was characterized, two amplifying stages were used in the design, interconnected using matching networks described within the next section.

### 3.3.3 IMPEDANCE MATCHING

Both small-signal noise and large signal analysis were performed in order to know the maximal achievable performances for multiple transistor sizes, and anticipate the potential trade-off due to matching network reusing. The small-signal analysis was performed using an S-parameters (SP) simulation, while the large signal analysis was performed using a periodic steady state (PSS) simulation. As we see, the respective optimums of the four plotted metrics Figure 68 are located in different – but close – impedance grids. The goal of this design is to get nearby each optimum reusing the matching networks, while minimizing the impact of the potential induced trade-offs.

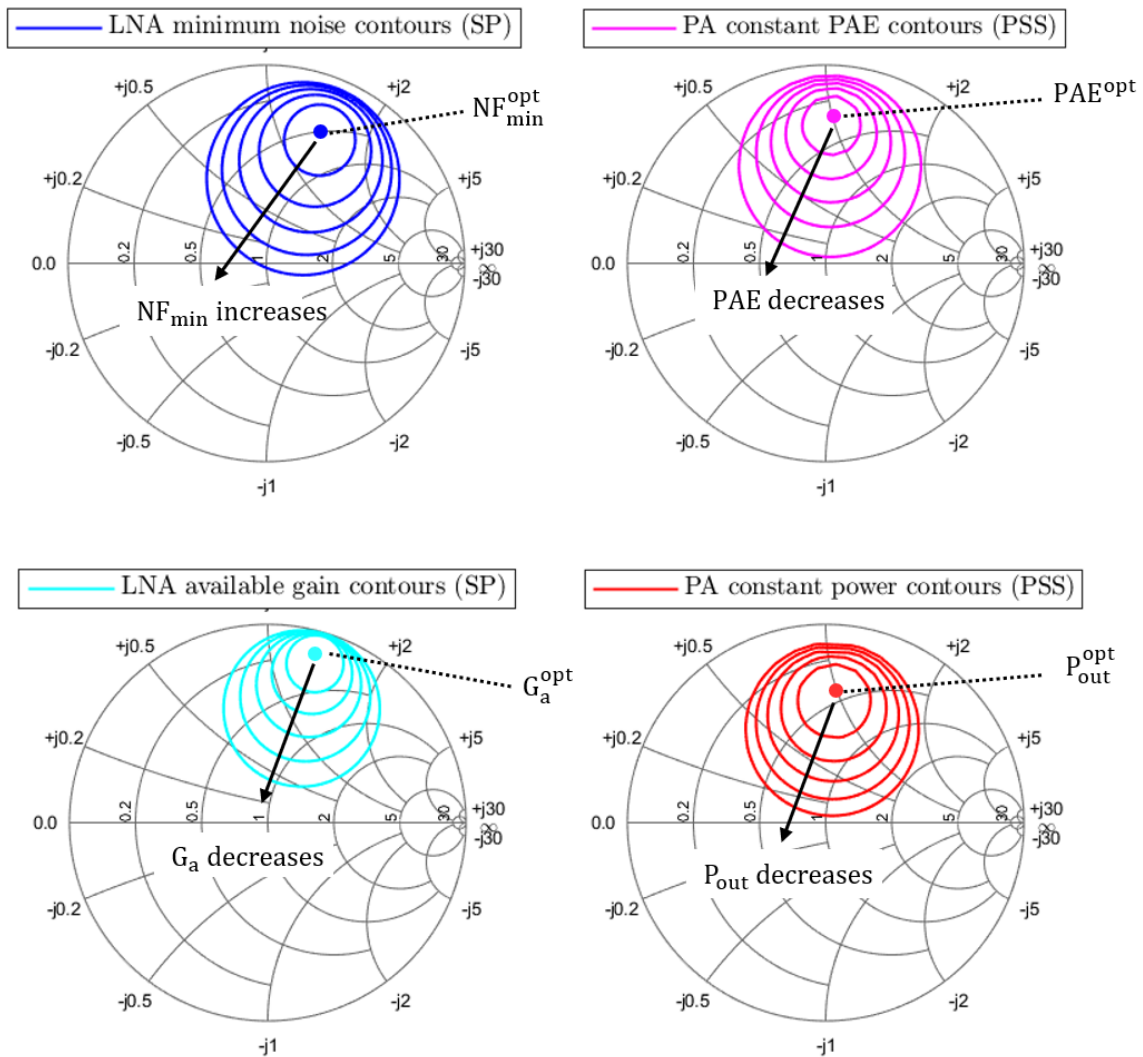


Figure 68: Noise, available gain (LNA) constant PAE and constant power contours (PA) of the main stage

The entire amplifier is built and operates as in Figure 69. It is composed of two amplification stages, interconnected with integrated transformers and custom inductors. Tuning capacitors  $C_{t1}$  and  $C_{t2}$  are located at the input and output to ensure a  $50\Omega/100\Omega$  input/output impedance matching. Most of the biasings are applied using the center-tap of transformers.

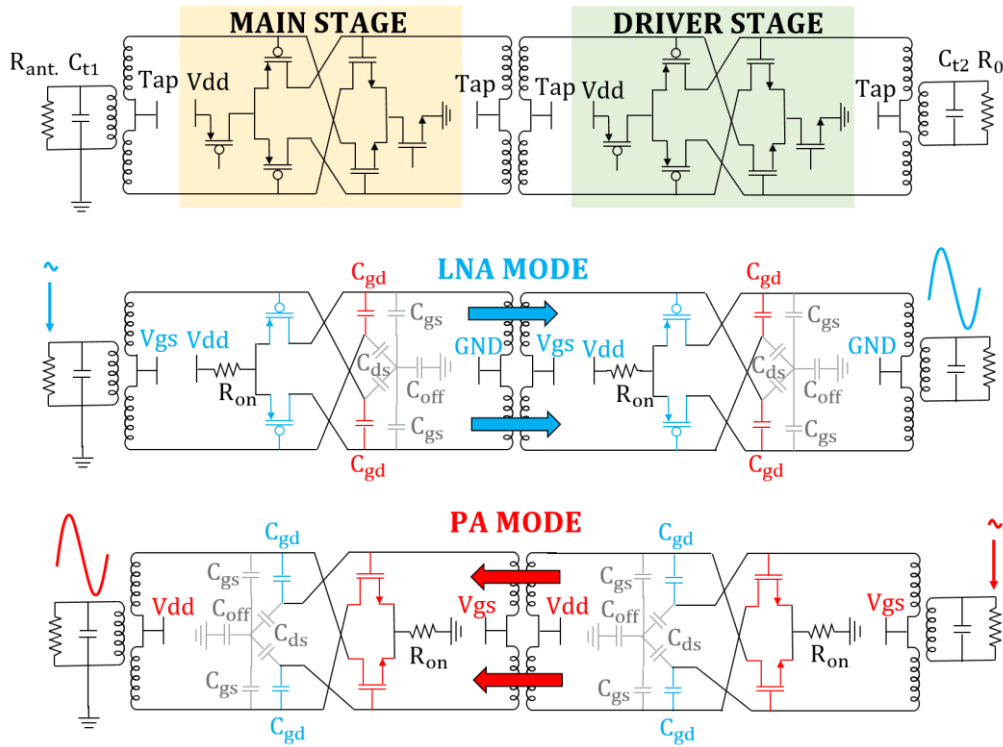


Figure 69: Bidirectional amplifier schematic and associated PA and LNA operating modes

The two available PDK transformers (stacked and planar) were compared with respect to their  $G_{max}$  (at 38.5GHz) and their  $SRF$  as in Figure 70.

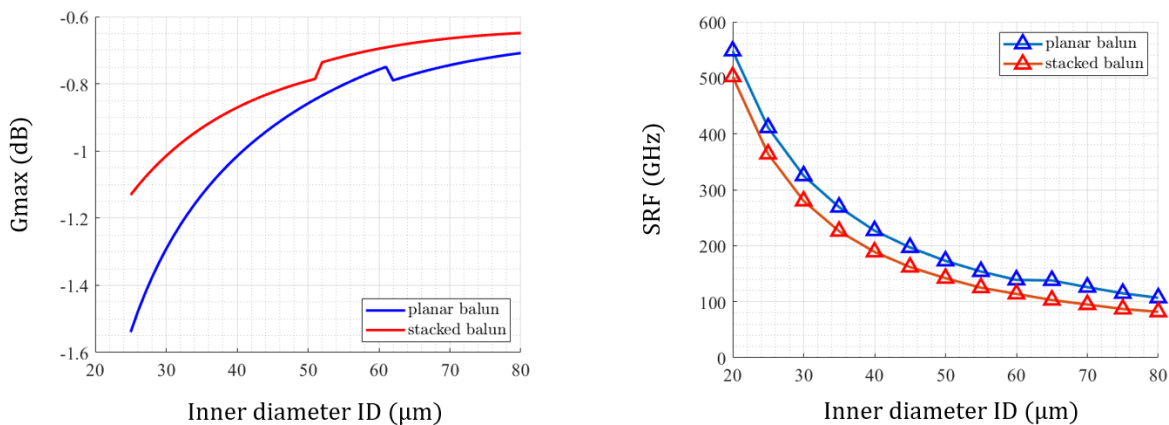
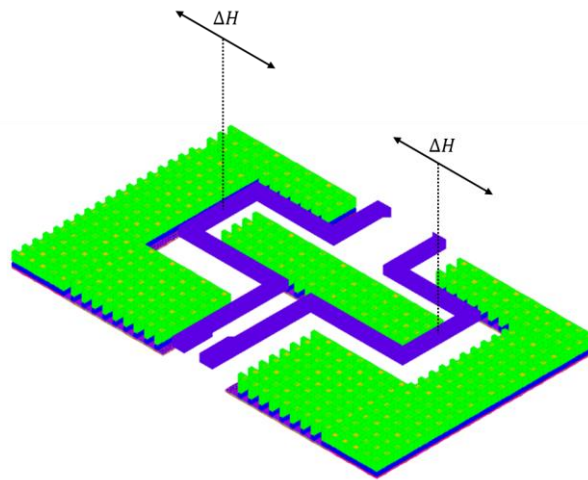


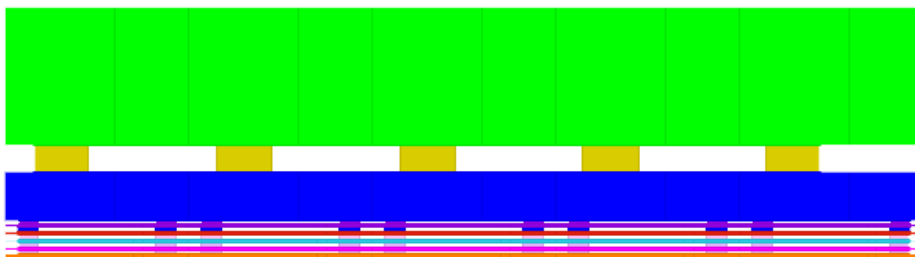
Figure 70: Performances comparison between stacked and planar PDK transformers

On the one hand, the stacked transformer exhibits a higher  $G_{max}$  than the planar one, but on the other has a lower  $SRF$ . The three stacked transformers were connected with the two amplifier stages (arbitrarily named “main” and “driver” stages) using custom paperclip-shaped inductors to enhance compacity. This inductor was designed using a thick metal layer (QA or QB) and surrounded with a global ground plane as in Figure 71. The tuning parameter  $\Delta H$  allowed to perform fine tuning during the post-layout electromagnetic simulations process, without changing the length of the matching network.



**Figure 71: 3D layout view of a designed custom paperclip shaped inductor surrounded by a ground plane**

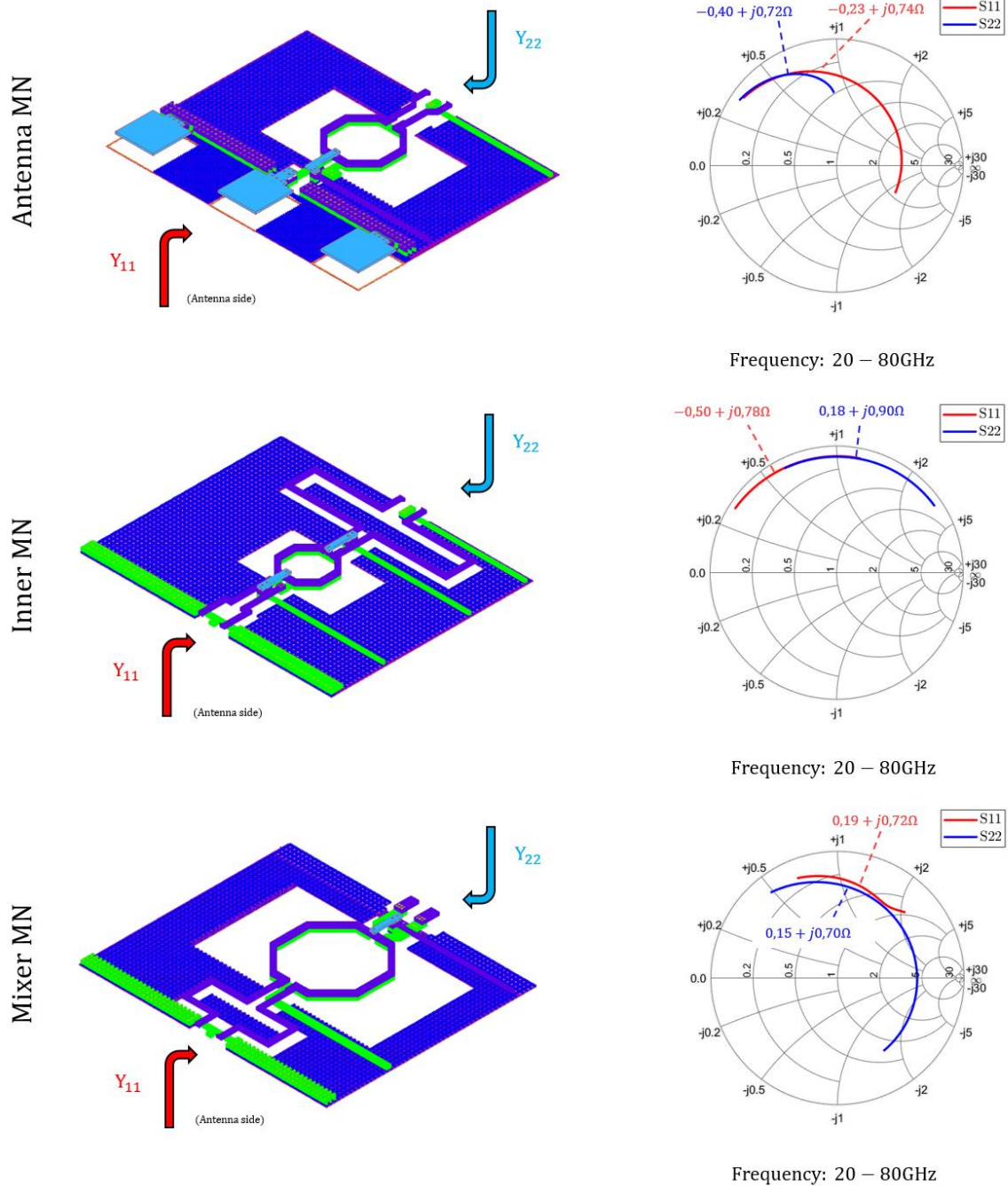
The ground plane is built using the superposition of stacked metal layers in order to reduce its overall resistivity. High resistivity ground plane would result in voltage drops that will limit the voltage swing of active devices, and hence deteriorate performances. This ground plane unit cell is defined in mosaic matrix (1x5) whose unit cell is depicted in Figure 72 using metal layers from QA to C1 interconnected with vias.



**Figure 72: Sectional view of the ground plane 5x1 matrix mosaic used in Figure 71**



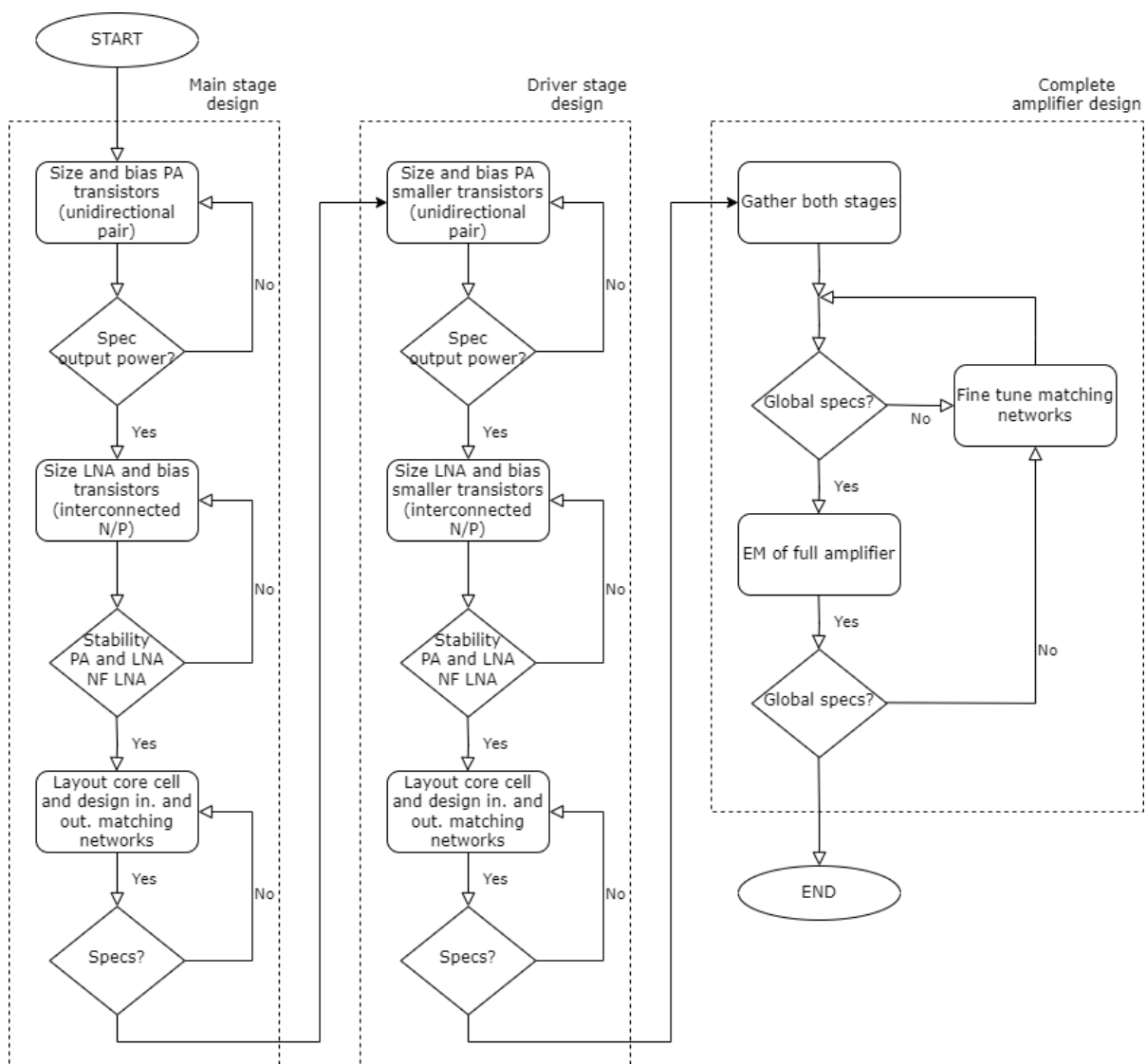
The three realized matching networks Figure 69 were illustrated with 3D-views, and were characterized through smith charts plots representing each input and output admittances with markers at the center frequency 38.5GHz as in Figure 73.



**Figure 73: Admittance summary of the three matching networks used to interconnect the two amplification stages (main and driver stages)**

At the heart of all consideration, trade-offs between the design of the PA and the LNA have to permanently be found. The main stage was studied first. Then the driver stage was designed and interconnected with the main stage with designed matching network characterized using electromagnetic simulations. Once the amplifications stages were gathered, fine tuning was performed in order to optimize performances, mainly playing on the values of custom inductors, and hence their heights.

Finally, a simulation of the entire PA-LNA was conducted to get the best accuracy over the description of its behavior. This design flow is described in Figure 74.

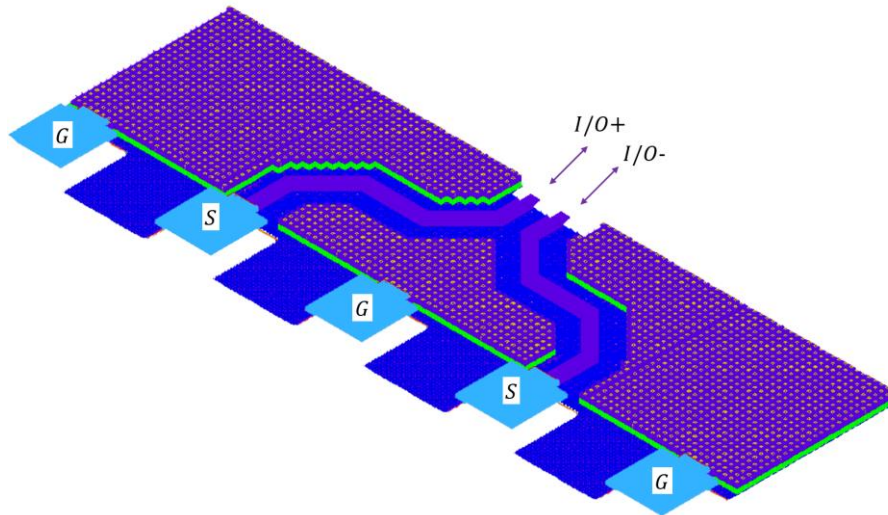


**Figure 74: Design flow of the designed two-stage bidirectional amplifier**

### 3.3.4 LAYOUT AND RESULTS

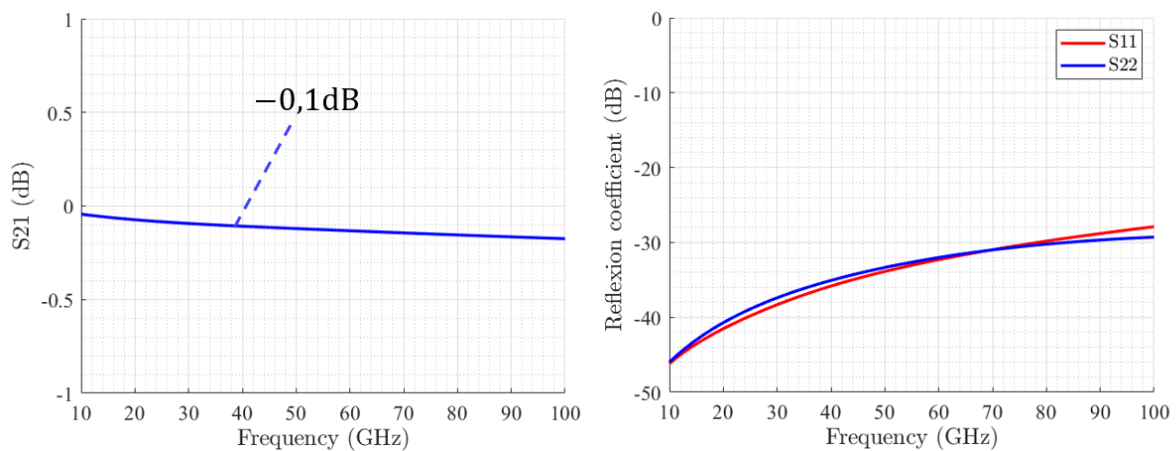
#### 3.3.4.1 Post-layout simulations

For the RUN1 the PA-LNA is terminated with two 50 $\Omega$  GSG pads, while in RUN2 the PALNA is terminated with GSG and GSGSG pads, both terminated with a 50 and 100 $\Omega$  load resistors. In

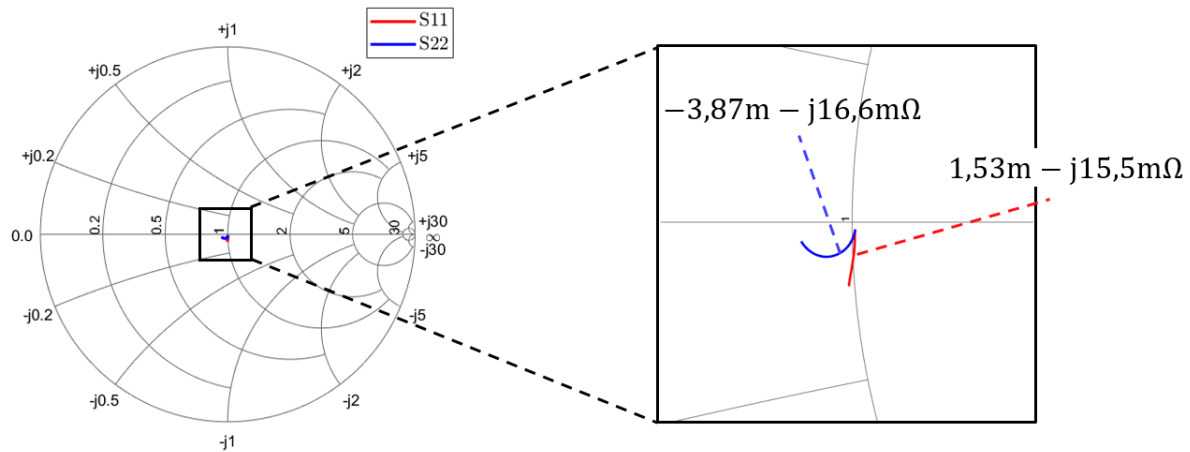


**Figure 75: 3D layout view of the 100 $\Omega$ -differential transmission line**

order to connect the amplifier to the GSGSG pads, a 100 $\Omega$ -transmission line was designed as in Figure 75. This single-to-differential (and vice-versa) PA-LNA was the amplifier incorporated to the final thesis transceiver chip (RUN3, discussed in Chapter 6).

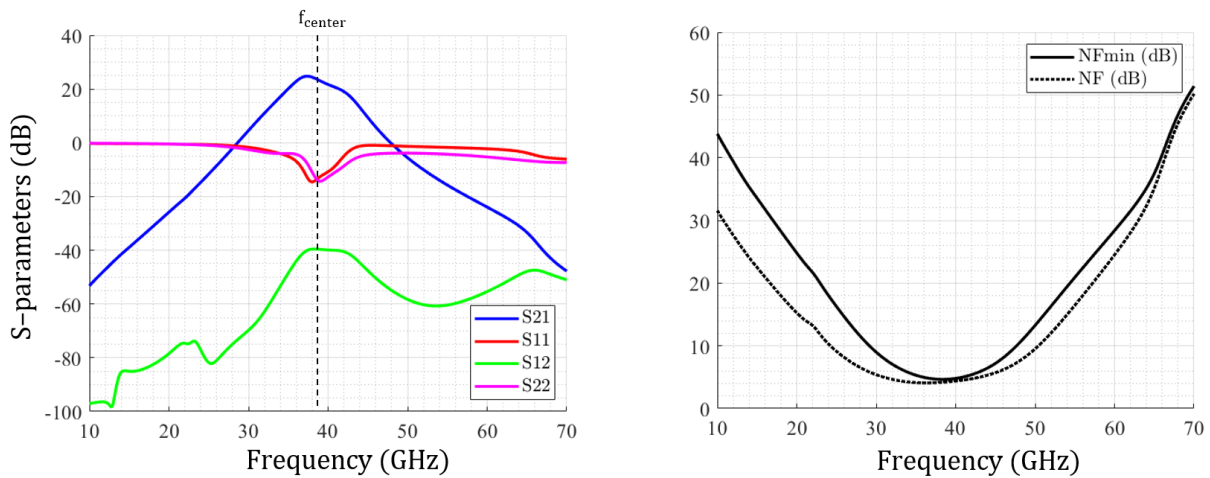


**Figure 76: Post-layout simulations of the designed 100 $\Omega$ -differential transmission line including NF and S21 (left) and input/output reflexion coefficients (right)**



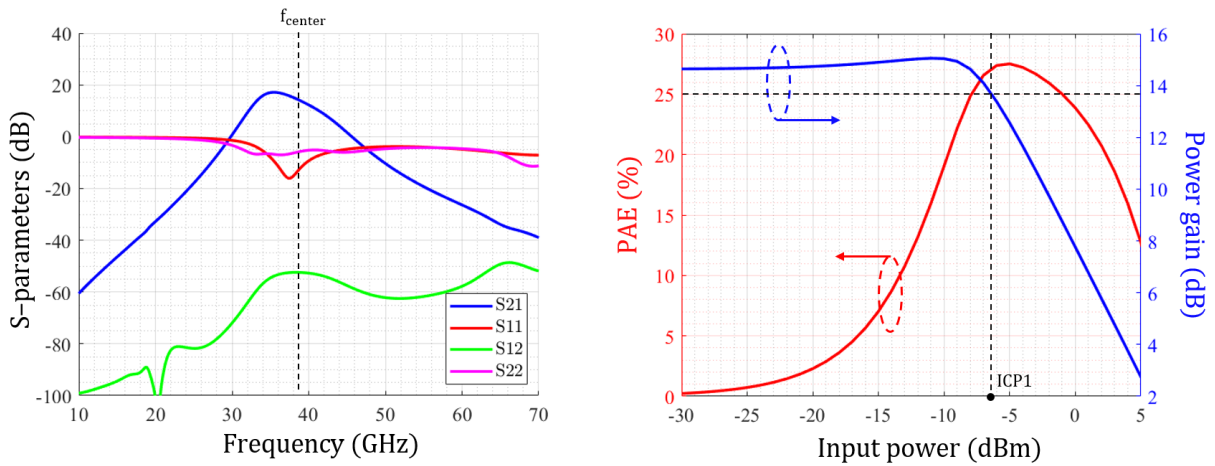
**Figure 77: Smith chart plot of the  $S_{11}$  and  $S_{22}$  of the  $100\Omega$ -differential transmission line**

This transmission line was characterized as in Figure 76, exhibiting a  $S_{21}$  of 0.1dB and  $S_{11}$  and  $S_{22}$  of -36.1dB and -35.4dB respectively (port 1 and port 2 being located respectively in the S pads side and the differential I/O side) at 38.5GHz. The smith chart in Figure 77 shows an input and output impedance very close to  $50\Omega$ .



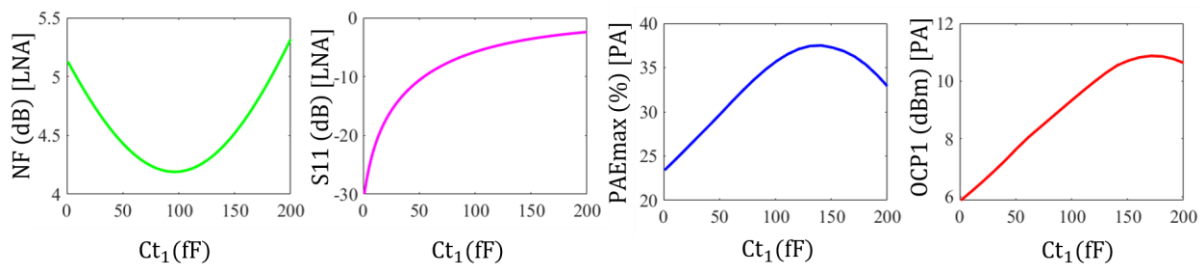
**Figure 78: Simulated LNA S-parameters (left) and  $NF_{min}$ ,  $NF$  (right)**

The LNA exhibits a small-signal gain of 23.8dB, a  $NF$  of 4.6dB and good adaptation at the input and output with a  $S_{11}$  and  $S_{22}$  respectively equal to -13.4dB and -13.8dB. The isolation  $S_{12}$  of the PA-LNA is -39.6dB, and the DC power consumption is 21mW at a supply voltage  $V_{DD}$  of 0.8V. The performances of the PA are depicted in Figure 80. It exhibits a power gain of 14.4dB with an adequate input matching with a  $S_{11}$  equals to -13.5dB. The large signal analysis shows a peak PAE of 27.4%, a saturated power of 7.5dBm while the OCP1 is equal to 7.1dBm. The PA consumes 17.8mW at the 1dB compression point.



**Figure 80: Simulated PA S-parameters (left) and power gain and PAE (right)**

The required silicon area for this PA-LNA is only  $0.11\text{mm}^2$ , when considering only the core area (without pads and the  $100\Omega$ -differential transmission line).

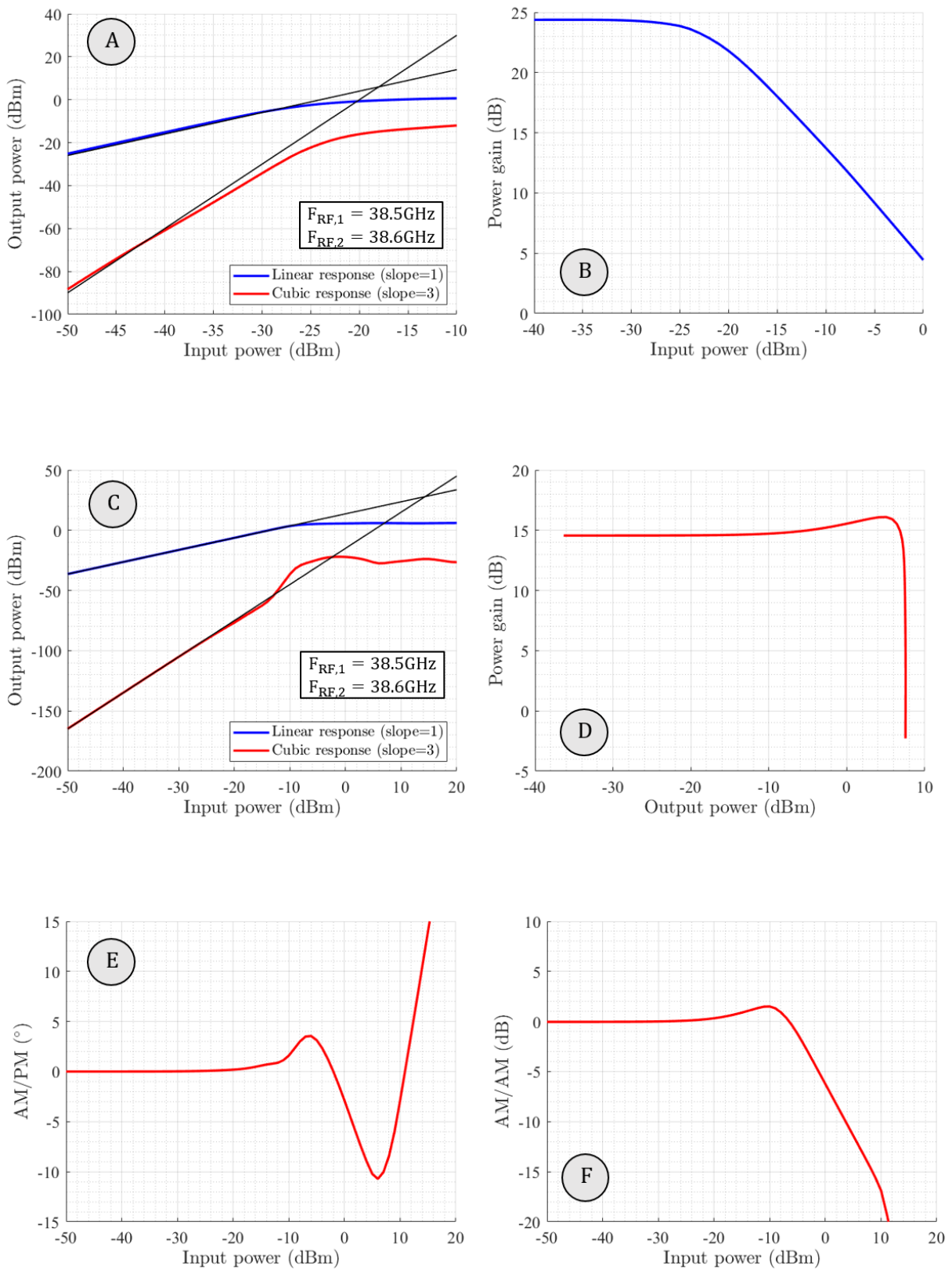


**Figure 79: Design trade-off illustrated with the impact of the variation of the antenna capacitor**

The trade-offs are illustrated with the variation the PA-LNA  $NF$ ,  $S_{11}$ ,  $PAEmax$  and  $OCP1$  when sweeping the value of antenna-side capacitor. As it can be seen, and as expected, the optimums of the four curves are reached for different value of the antenna capacitor  $Ct_1$  illustrating well the trade-off concept of PA-LNA design.

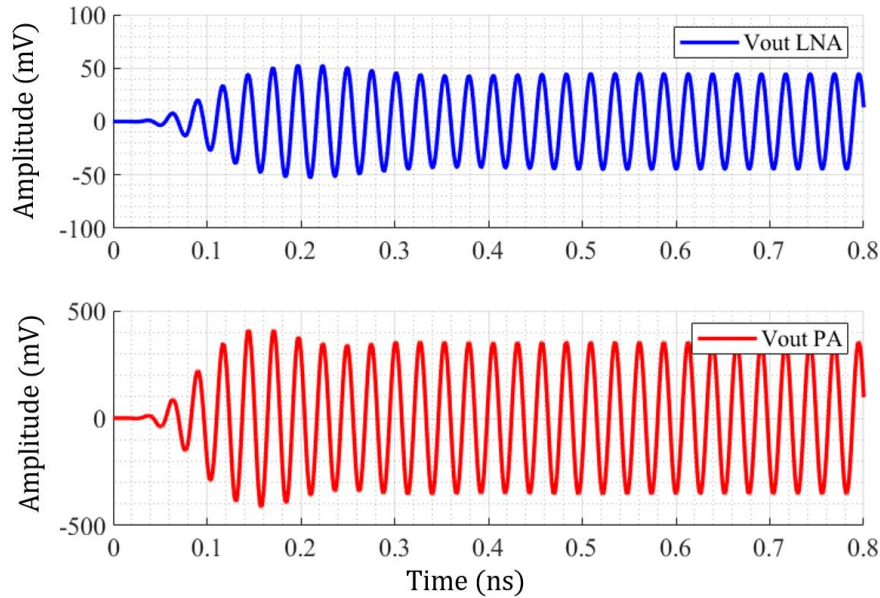
A two-tone (at 38.5GHz and 38.6GHz) large signal analysis was conducted exhibiting a LNA  $IIP3$  and  $ICP1$  of -18dBm and -23dBm and finally a PA  $OIP3$  of 27.6dBm from Figure 81 (A) and (C).

Finally, with a single-tone (at 38.5GHz) large signal analysis AM/AM and AM/PM distortion were characterized for the PA showing an AM/PM distortion of  $3.6^\circ$  at  $OCP1$  and a maximal AM/AM distortion of 1.49dB Figure 81 (E) and (F).



**Figure 81: LNA IIP3 interpolation (A) and power gain (B) and PA OIP3 interpolation (C) power gain (D) AM/PM (E) and AM/AM (F) distortions**

A transient analysis was conducted to get the time-response of the amplifiers. Figure 82 allows to get the set-up time in LNA mode (0.277ns) and PA mode (0.198ns).



**Figure 82: Simulated transient response at maximum input power at 38.5GHz**

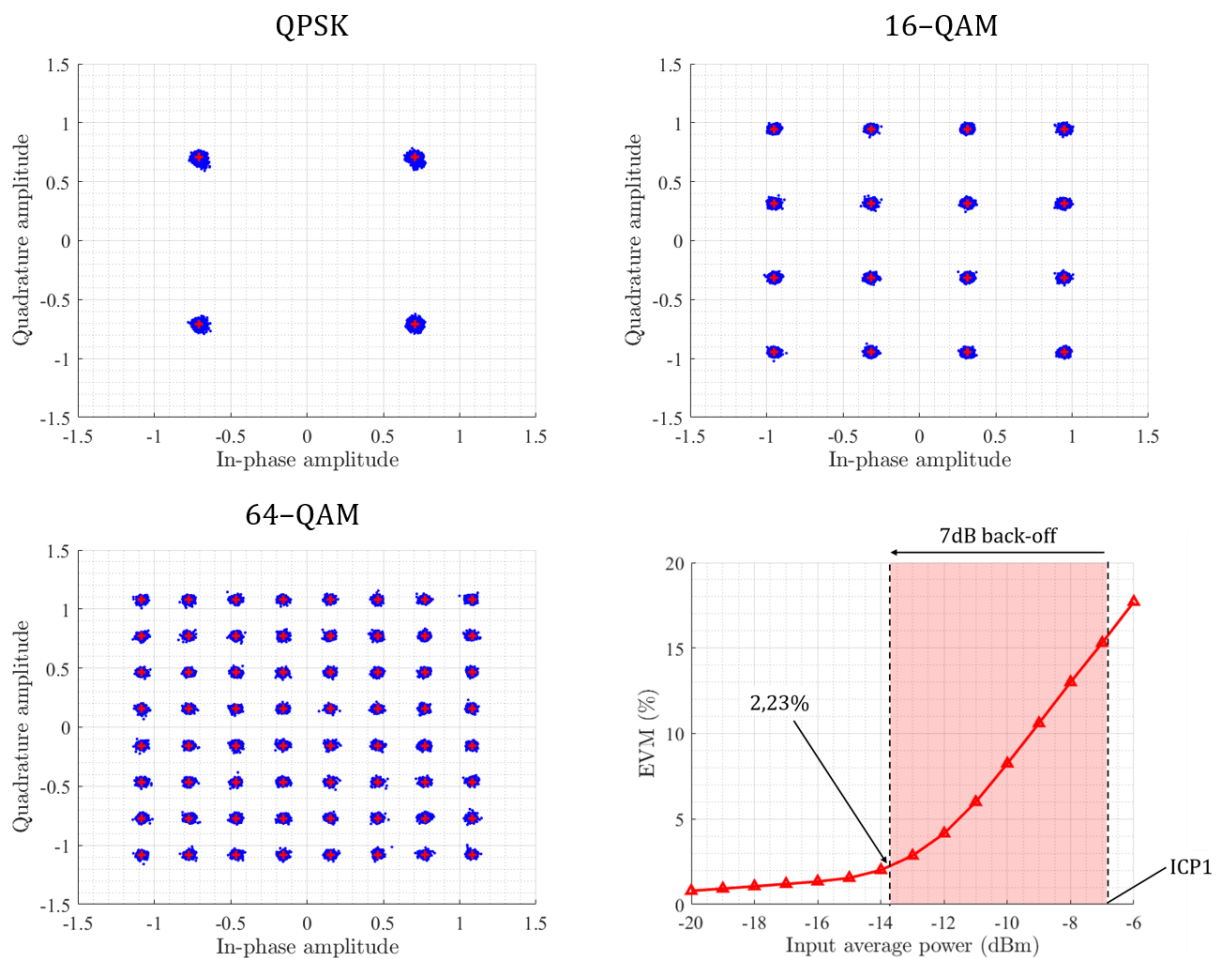
Input signals are generated at 38.5GHz and at the maximal input powers mentioned in the power budget Chapter 2. Finally, statistical Monte Carlo simulations were conducted to evaluate the sensitivity of the circuit to process variation and mismatch Table 14.

Monte Carlo Analysis (200 points)	Process		Mismatch	
	Mean	Std Dev.	Mean	Std Dev.
LNA Mode				
S21 (dB)	23.56	1.16	23.78	0.03
NF (dB)	4.68	0.12	4.65	0.002
PA Mode				
OCP1 (dBm)	6.46	0.93	7.06	0.012
PAEmax (%)	25.65	2.16	27.51	0.014

**Table 14: PA-LNA post-layout statistical simulations over LNA S21 and NF and over PA OCP1 and PAEmax**

The previous table demonstrates a very low dependency of mismatch variation when considering only the contribution of transistors. As to process variations, variation over the main metrics remains within an acceptable range of variation considering the obtained standard deviations  $\sigma$ .

Modulated signals were used in order to plot the constellation diagrams Figure 83 using various modulations schemes such as QPSK, 16- 64- and 256-QAM. For this simulation, the PA average input power was set at  $ICP1$  with a 7dB BO, the channel bandwidth to 400MHz, the subcarriers are spaced by 120 kHz and 264 indexed RB's (resource blocks) were used. The 5G NR channel number is 2254167. The EVM is then plotted with respect to the input power and exhibits a 2.23% EVM, at 7dB BO using a CP-OFDM 64-QAM modulation scheme, in the maximum transmission bandwidth configuration of 400MHz.



**Figure 83: Constellation diagram of 4- 16- 64-QAM modulations and evolution of the EVM with respect to the average PA input power, in the case of a 64-QAM OFDM modulation**



### 3.3.4.2 Measurements RUN1: K2000 (PA-LNA)

The PA-LNA was the first building block realized within this thesis at the beginning of the year 2022. The first tape-out included a single-ended 50 $\Omega$  standalone PA-LNA in GF 22nm FDX terminated with two ground-signal-ground (GSG) RF pads. This first version of the PA-LNA was fabricated and as it is presented Figure 84, using the GF 22nm FD-SOI technology. The 6x6 DC pads are located at the south, and the GSG RF pads are respectively located at the east and west of the chip.

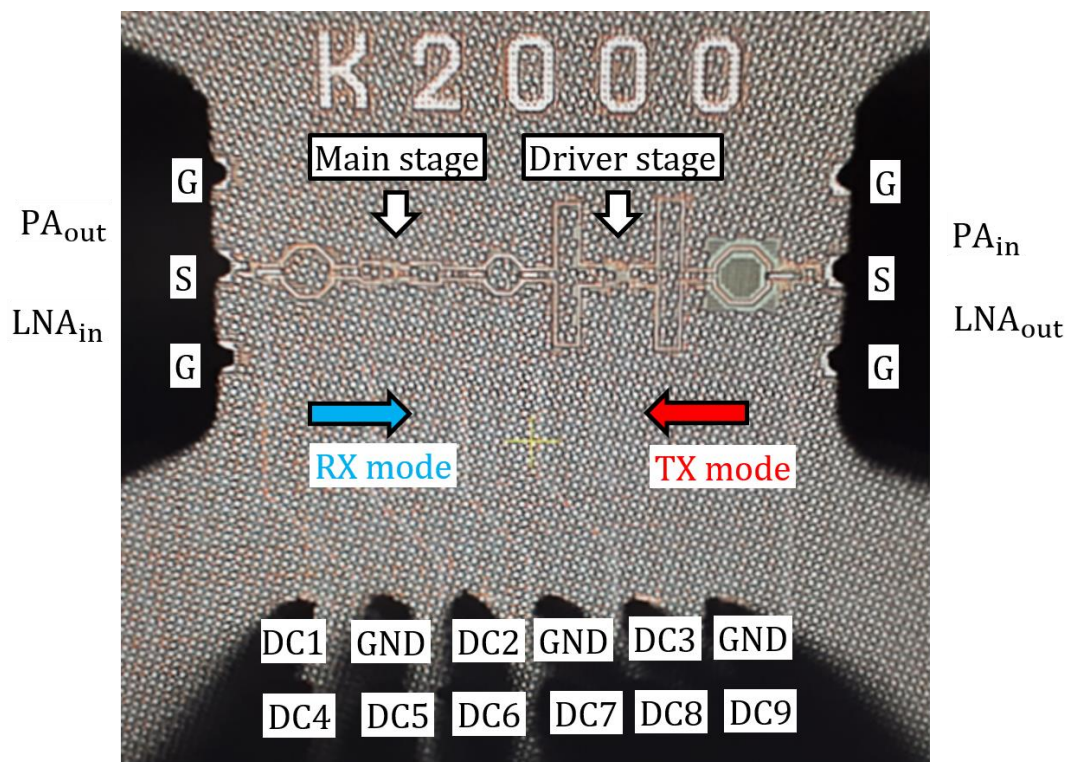
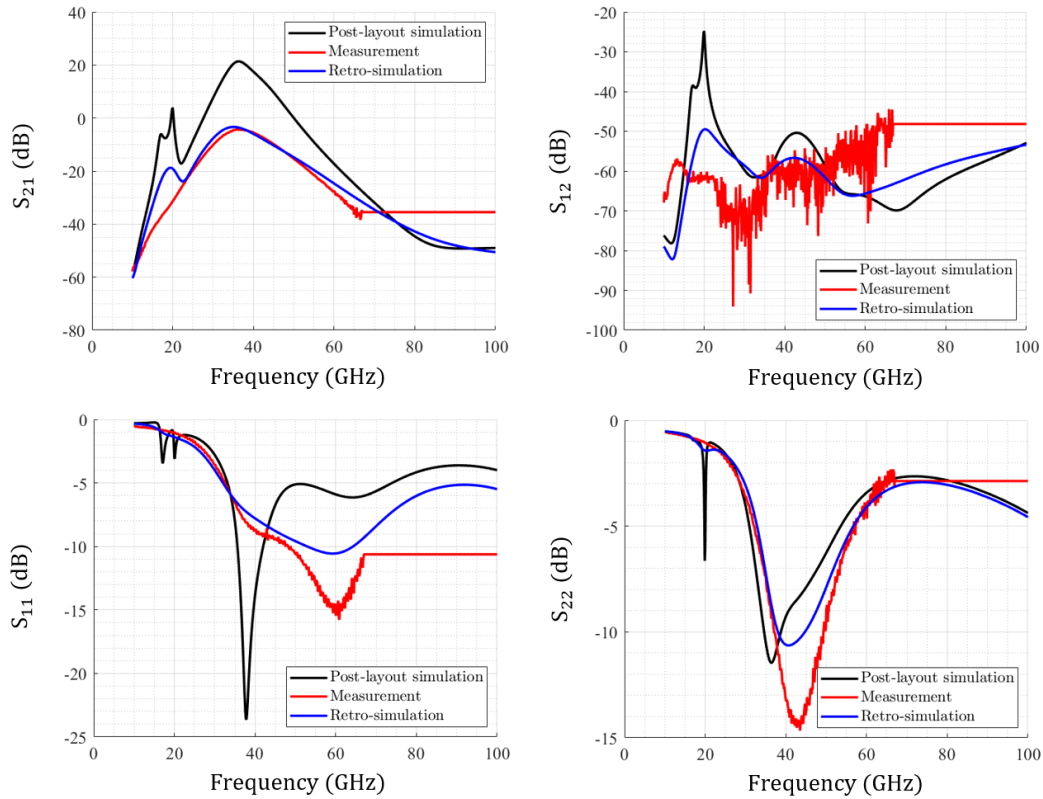


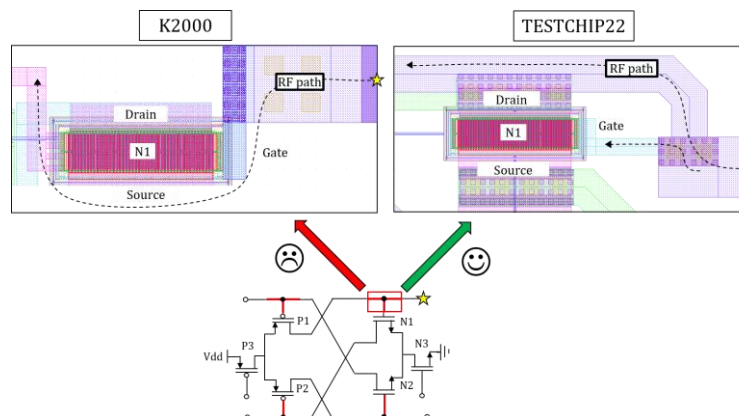
Figure 84: Layout of K2000 (A) and corresponding die photograph (B)

Several sensing resistors were used to verify both biasing and supply voltages in both modes. Unfortunately, the circuit was found to be dysfunctional in both PA and LNA mode. Measured supply currents and biasings were found very similar than in post-layout simulations. The measured LNA S-parameters are plotted in Figure 85. The first noticeable things are the drop of the forward voltage gain  $S_{21}$  from 19.6dB to -4.8dB, the input matching shifting from 40GHz to 60GHz, and the close behavior between measurements and simulations with respect to the output matching and the isolation. The layout resistivity of various RF paths was hence investigated in order to seek the cause of such a significant voltage gain drop. The main layout issue was found to be a high resistivity path in the amplifier core cells as in Figure 86.



**Figure 85: K2000 LNA comparison of measured, simulated and retro-simulated  $S_{11}$ ,  $S_{22}$ ,  $S_{12}$  and  $S_{21}$**

Hence, a particular attention was paid to the design of these paths, and the previous layout was compared to the proposed alternative solution. The retro-simulations were obtained by adding a series resistor at different nodes of the transistors, and a really good fit can be observed when comparing with the retro-simulations and measurement results. The proposed layout solution is presented Figure 86 and was incorporated within the next PA-LNA integrated to the TESTCHIP22 chip. One metal layer was also added to the global ground plane to further reduce its resistivity.



**Figure 86: Illustration of the high resistivity path issue identified over the layout of the core cells and proposed layout alternative**

### 3.3.4.1 Measurements RUN2: TESTCHIP22 (PA-LNA)

A second version of this amplifier was realized, and integrated within the TESTCHIP22 chip at the middle of the year 2023, in the light of the previous design. An opportunity of silicon area allowed to re-send the updated dysfunctional PA-LNA that was sent the previous year.

This time, the PA-LNA is matched to  $50\Omega$  and  $100\Omega$  as it will be in the final transceiver design. In the previous design, the impact of decoupling capacitors remained acceptable (gain spikes located around 20GHz Figure 85) since the stability of the amplifier was still verified. In this new design, the impact of decoupling capacitor (included in K2000) was so important over the stability of both PA and LNA that the decoupling capacitors inside the PA-LNA cell were removed, and the decoupling was realized within the I/O ring only instead (north 6x1 and south 4x1 DC pads Figure 87). The stability was hence verified.

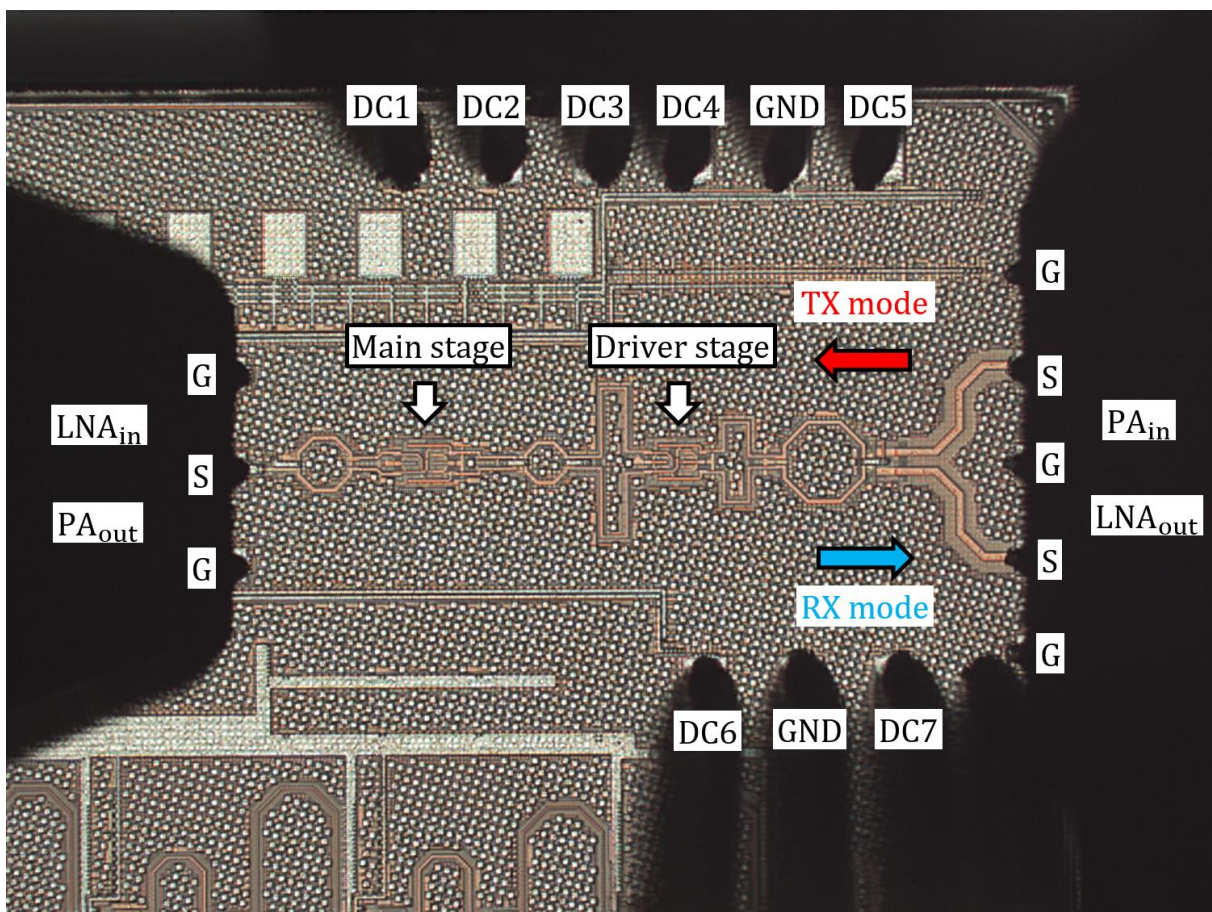
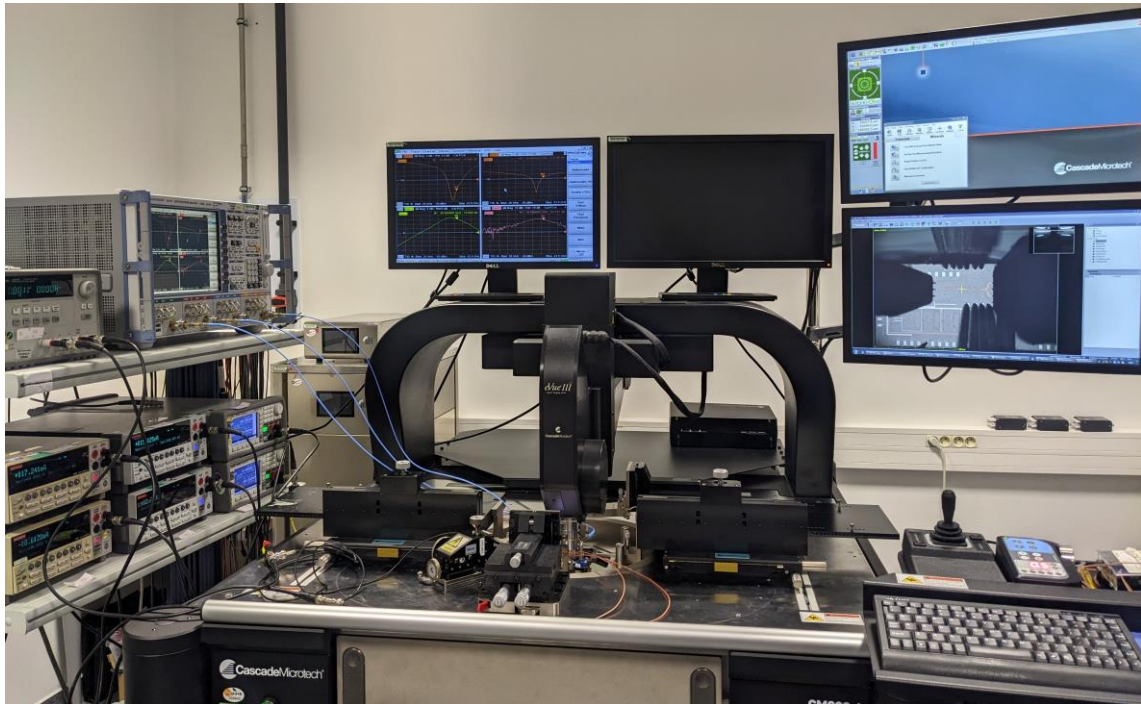
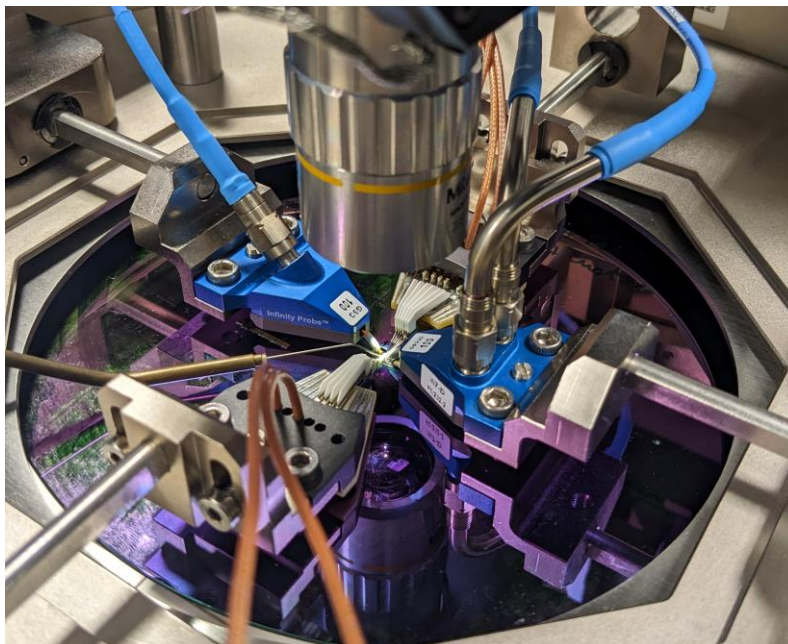


Figure 87: TESTCHIP22 chip layout (top) including the proposed second version of the PA-LNA



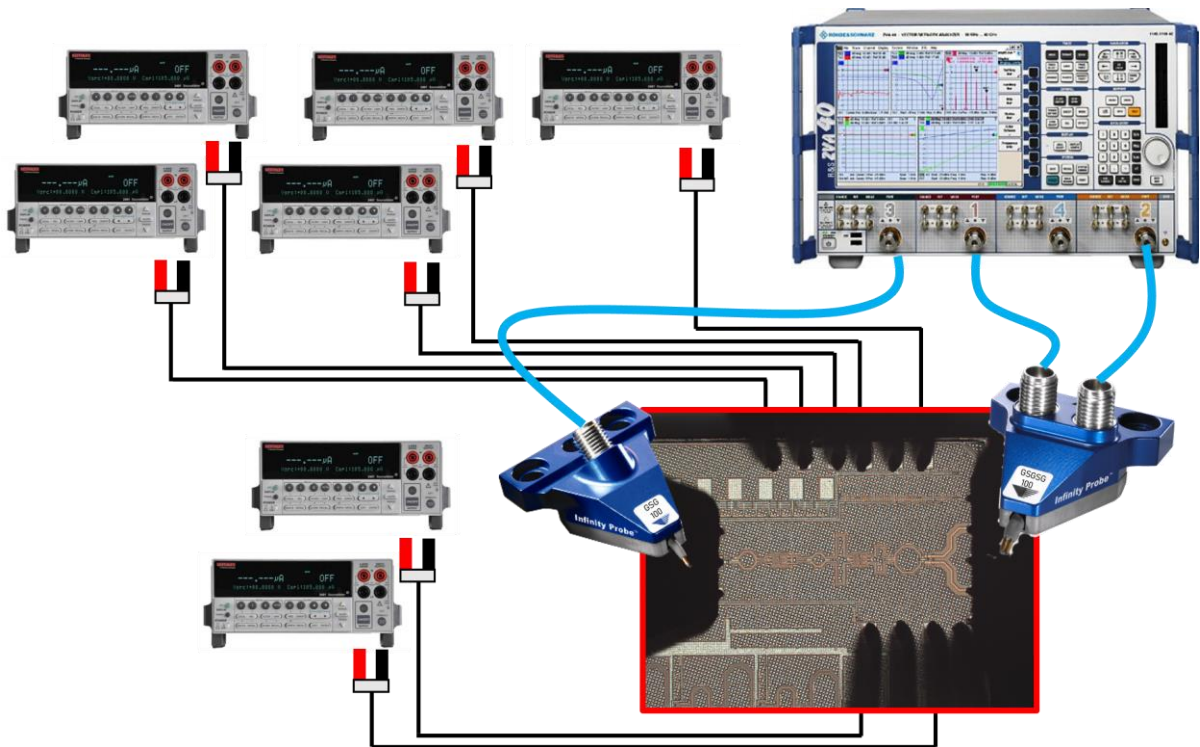
**Figure 88: TESTCHIP22 PA-LNA test setup**

The measurement setup is very similar than the K2000 one, and so described just once. It is depicted Figure 88 where voltage supplies and the ROHDE&SHWARZ ZVA 40 4-port VNA are on the left while the semi-automatic probe station located in the middle, controlled with a computer, using a micro camera to discern the chip and the probes. A close-up picture Figure 89 allow to observe the RF 100 $\mu$ m pitch GSG and GSGSG cascade probes (in blue).



**Figure 89: TESTCHIP22 PA-LNA test setup with a close-up view over the RF and DC probes**

Finally, the summary of the experiment setup was proposed in Figure 90.



**Figure 90: Simplified view of the TESTCHIP22 (PA-LNA) experimental test setup**

The biasings applied to the various DC pads in the TESTCHIP22 (PA-LNA) chip were reported in Table 15 within the two operating modes.

	DC1	DC2	DC3	DC4	DC5	DC6	DC7
TX MODE							
Voltage (V)	0.3	0.8	0.8	0.8	0	0.23	0
RX MODE							
Voltage (V)	0	0	0.45	0.45	0.8	0	0.8

**Table 15: TESTCHIP22 PA-LNA DC typical values applied to the DC probes**

The gate-source potential of PMOS transistors is identical for both stages, and set to optimize NF while the NMOS transistors used in the main and driver stages are respectively in AB and B class to optimize both the output power and efficiency.

The single- (true) differential S-parameters are plotted Figure 92 in PA (left) and LNA mode (right). In LNA mode it exhibits a  $S_{21}$  of 15.8dB (maximum 17.5dB at 37GHz) – when DC currents are matched with the simulations – and a  $S_{11}$  of -15.4dB and a  $S_{22}$  of -8.9dB. It also provides a reverse isolation of more than 40dB at 38.5GHz. In PA mode, measurements indicate a  $S_{21}$  of 5.47dB (maximum 10.5dB at 34GHz) and a  $S_{11}$  of -6.7dB.

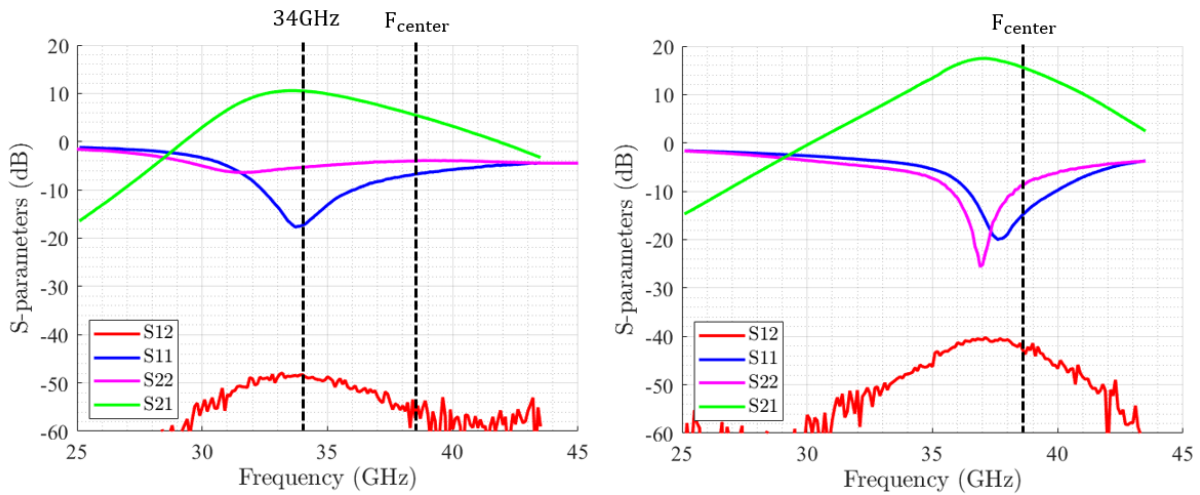


Figure 92: Measured PA (left) and LNA (right) S-parameters

After that, a large signal analysis was conducted in PA mode Figure 91. It exhibits a peak  $PAE$  of 9.1% and 4.34% when the input is excited with a 34GHz and 38.5GHz input tone, respectively. As to the LNA, it exhibits in Figure 93 a single to (true) differential power gain of 15.7dB and highlight the 1dB-compression point located at -18dBm while the PA exhibits a OCP1 of 1.6dBm, a  $P_{sat}$  of 5.4dBm and a OCP1 of 0dBm, a  $P_{sat}$  of 5.1dBm in the 34GHz and

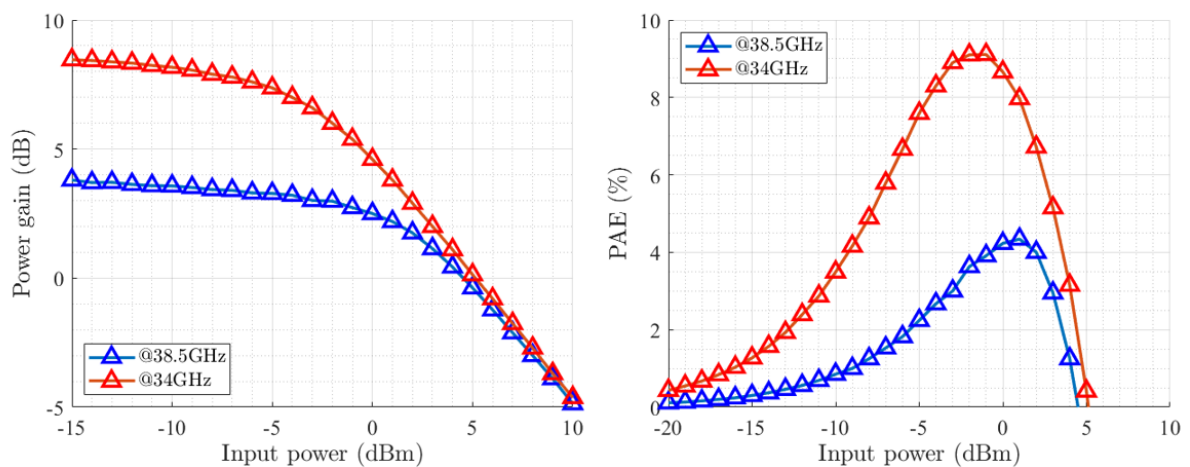
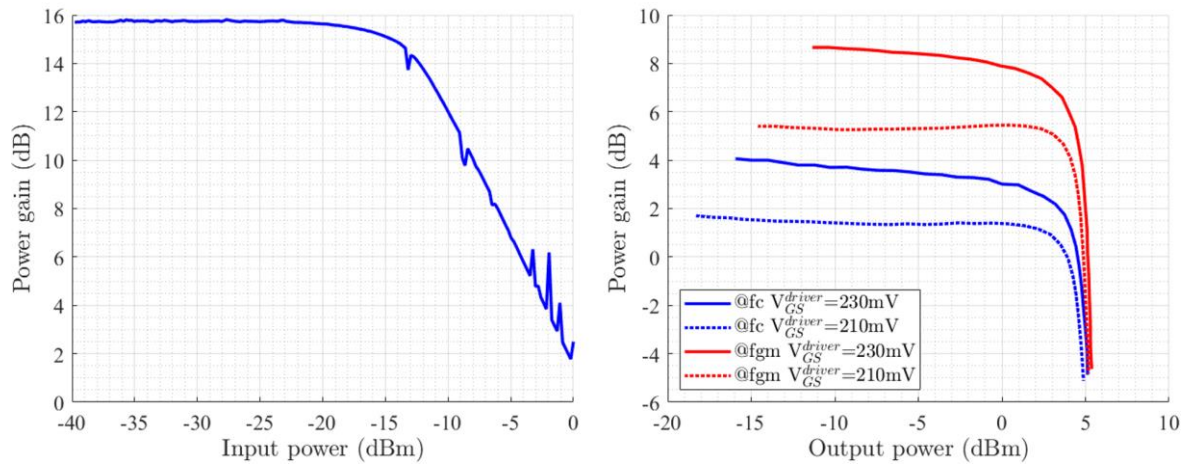
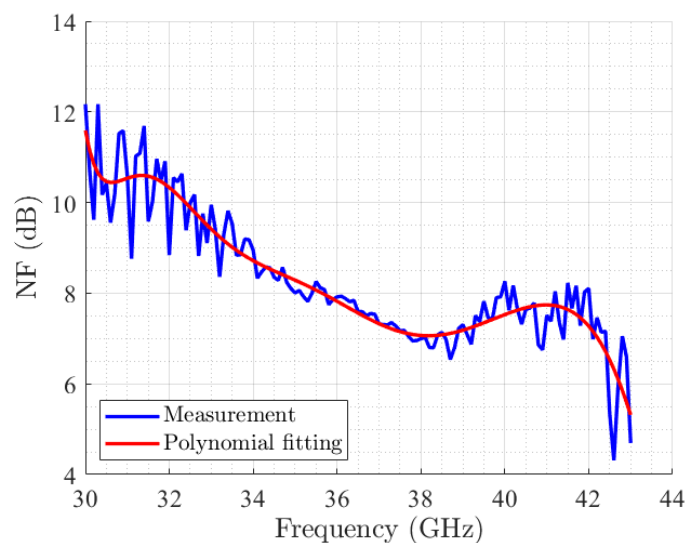


Figure 91: Measured PA power gain (left) and PAE (right) at 34GHz (red) and 38.5GHz (blue)



**Figure 93: Measured LNA (left) and PA (right) power gain compression under various driver stage biasing configuration and at different input-tone frequencies**

38.5GHz input tone configurations respectively, under typical biasings. The driver stage transistors biasing was lowered in order to see how can the  $OCP1$  can be extended. Finally, the  $NF$  of the LNA was plotted as in Figure 94, where the measured  $NF$  is fitted using a high order polynomial function. The measured  $NF$  is approximated to 7.1dB, using a 10th order polynomial fitting function. This value is higher than expected mainly because LNA gain is lower than expected. It still reaches a minimal value at 38.5GHz. The Monte Carlo simulations estimated a variation of 2%  $PAE$  and a 1-dB gain variation. The gain drop is also explained with the port 2 adaptation mismatch. Unfortunately, since the chip arrived late in the thesis, complementary simulations would be required to clearly identify the layout/modeling issue.



**Figure 94: Measured and polynomial approximation of the LNA 3-ports  $NF$**

### 3.4 SUMMARY

The initial specification tables for both PA and LNA were filled with the post-layout simulation results as in Table 16 and Table 17, the measurement results being unsatisfactory.

LNA		
	Specification	Post-layout simulation
Power gain (dB)	23	23.8
3dB BW (GHz)	3.6	4.3 @peak gain
Gain ripple (dB)	$\pm 1$	1.1 @400MHz ch. BW
NF (dB)	6	4.6
IIP3 (dBm)	-18	-18
Input matching (dB)	-15	-13.4
Output matching (dB)	-15	-13.8
Reverse isolation (dB)	-15	-39.6

*Table 16: LNA post-layout performances compared with specifications*

PA		
	Specification	Post-layout simulation
Power gain (dB)	14	14.4
Gain ripple (dB)	$\pm 1$	1.1 @400MHz ch. BW
OIP3 (dBm)	17.3	27.6
OCP1 (dBm)	4.9	7.1
IMD3 @Pin=-20dBm (dBc)	35	27.8
AM/PM distortion @OCP1 (°)	2	3.6
-3dB BW (GHz)	3.6	5.4 @peak gain
Input matching (dB)	-15	-13.3
Reverse isolation (dB)	-15	-52.4

*Table 17: PA post-layout performances compared with specifications*



### 3.5 COMPARISON WITH THE STATE-OF-THE ART

	ASPDAC (2020) [53]	IMS (2021) [37]	RFIC (2020) [55]	MWCL (2021) [56]	ISSCC (2022) [54]	<b>This work (2023) [57]</b>
Process	65nm CMOS	90nm CMOS	28nm CMOS	65nm CMOS	45nm SOI	22nm FD-SOI
Frequency (GHz)	26.5-29.5	30-39.2 34-38.1	56-72	52-67	25.3-42 27-38	37-40
Architecture	Merged TRX	Separated TRX	Separated TRX	Merged TRX	Merged TRX	Merged TRX
Nb. of stages	2	5	4	2	2	2
Core size (mm <sup>2</sup> )	0.11	0.215	0.23	0.07	0.11	0.11
TX gain (dB)	14	18.3	21	16.1	18.9	14.4
TX Psat (dBm)	15.1	15.1	13	9.6	19.2-17.2	7.5
TX OCP1 (dBm)	11.3	13.3	9.5	5.1	18.4-16.3	7.1
TX PAE (%)	8.6	29	10.9	11.5	33.6-29.9	27.4
TX power (mW)	149@1V	81@1.2V	87@0.9V	70@1.2V	171@2V	18@0.8V
RX gain (dB)	N/A	17.6	15.3	16.1	17.6	23.8
RX NF (dB)	4.2	4.7	3.8	7.1	5.2-7.8	4.6
RX power (mW)	31@1V	25@1.2V	12@0.9V	70@1.2V	66@1.1V	21@0.8V

**Table 18: PA-LNA post-layout simulations compared with the state-of-the art**

### 3.6 CONCLUSION

Finally, the performances of our bidirectional amplifier were compared with prior works found in the literature as in Table 18. It appears clearly that bidirectional integrated front-ends represent a very attractive solution for compact and/or low-cost applications.

As to the comparison between specifications and simulated performances, extra efforts can be done over the gain flatness over the channel for both modes. For example, (switched) shunt resistors can be added, but would also lead to the decrease of the gain. As to the AM/PM distortion, a different set of biasings would need to be thought of, especially for the class B driver stage that contribute significantly to the increase of this distortion. In any ways, it would lead to re-thinking the matching networks to find another satisfying trade-off to entirely meet design specifications.

An automated approach for the optimization, and the computation of co-simulations using programming resources have a high interest in these architectures, and would save a precious time in the next design processes. In our case, the design was “hand-made” and was highly time-consuming. An interesting idea would be the iteration of the testing of transistors sizes in order to get even closer optimum impedance grids for the two amplifiers.

From the comparison with the state-of-the art Table 18, a reduction ratio of the required silicon of roughly two can be achieved, by taking benefit of bidirectional topologies. It is also noticeable that similar attractive performances can be achieved when comparing the bidirectional amplifiers that reuse the matching networks, with architectures that separate them.

It is however at a higher design complexity cost, since trade-offs need to be found, instead of having the flexibility of dealing with the design of the two amplifiers almost independently.

The measurement results would also suggest extra investigations over both the electromagnetic modeling and layout of the chip, including the I/O ring.



# Chapter 4: FREQUENCY CONVERSION

**F**requency conversion is a concept at the heart of telecommunication systems. In order to increase data rates, signals are modulated using high frequency carriers. As it is challenging to elevate the operating frequency within digital circuitries, a signal is either up-converted (in TX mode) from a low to a high frequency, or down-converted (in RX mode) from a high to a low frequency. Furthermore, as the RF signal treatment can be challenging, silicon consuming and power-hungry, some processing operations can be done at a lower frequency instead (in the analog baseband domain, or at an intermediate frequency). The mixer is the entity that allows this frequency conversion from a domain to another.

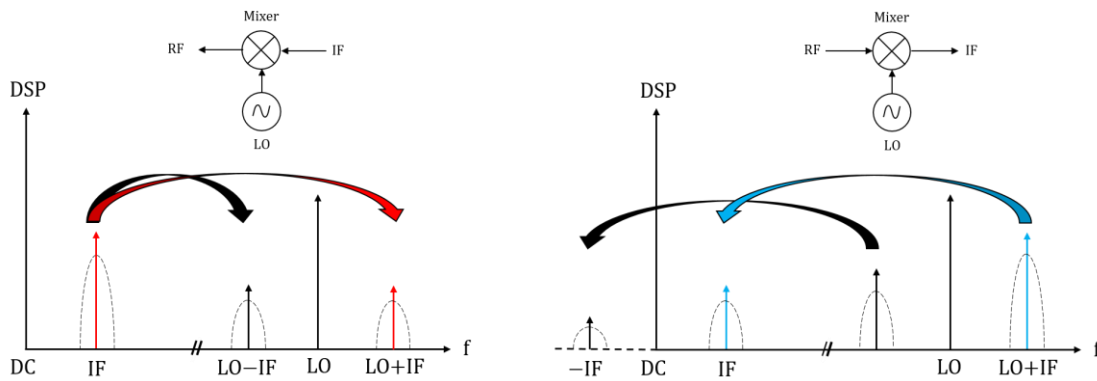
In this chapter, mixers and systems in which they operate will be compared. The focus will then be made over the design of a double-balanced passive mixer cell as well as the network required to generate and propagate quadrature signals, generated using an integrated hybrid coupler (HCPLR) associated with an external (off-chip) single-ended LO source. A baseband buffer will also briefly be described, but will be fully justified and defined in Chapter 5.

Finally, the whole frequency conversion chain behaviour will be described with post-layout simulations and compared with system specifications.

## 4.1 MIXERS

### 4.1.1 BASICS

A mixer is a 3-port device that translates the frequency of an input signal to another using signal multiplication. It is an elementary building block in telecommunication systems. They can be used in two configurations as in Figure 95, either in the up-conversion (in red) or in the down-conversion (in blue) configuration.



**Figure 95: Frequency shift in emission mode (left) and receive mode (right)**

In the TX mode, the LO+IF tone is defined as the upper sideband (USB) while the LO-IF tone as the lower sideband (LSB). In the RX mode, the -IF tone is the image frequency. One input signal  $s_{in}(t) = A\cos(\omega_{in}t)$  is multiplied with the LO signal  $s_{LO}(t) = B\cos(\omega_{LO}t)$ , resulting in  $s_{out}$  expressed as

$$s_{out} = AB \cos(\omega_{in}t) \cos(\omega_{LO}t) = \frac{AB}{2} [\cos\{(\omega_{in} + \omega_{LO})t\} + \cos\{(\omega_{in} - \omega_{LO})t\}] \quad (29)$$

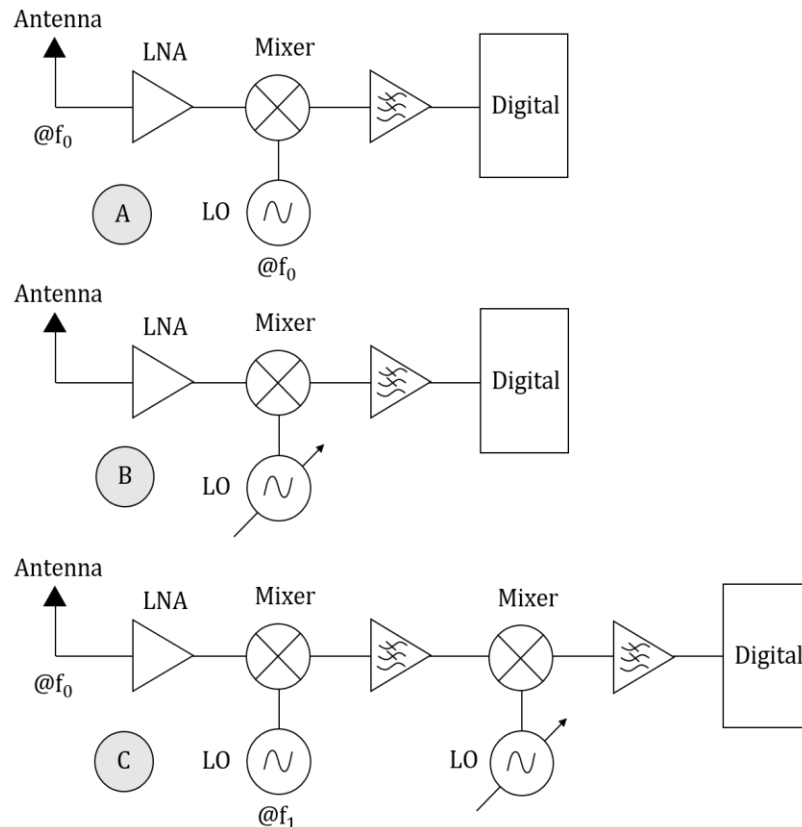
Mixers can be differentiated into two main families: actives and passive mixers. They have both advantages and disadvantages, summarized in Table 19 from [58], [59] and [60].

Active		Passive	
Pros	Cons	Pros	Cons
High gain Lower LO drive	DC power More complex to get a bidirectional operating mode AC coupling capacitors	High linearity Intrinsically bidirectional No DC power Broader BW Simple design	High losses High LO drive

**Table 19: Performances comparison between active and passive mixers**

#### 4.1.2 RECEIVER TOPOLOGIES

We previously saw that there are several types of mixers. Within receivers, there are also multiple ways to use them as in Figure 96, which depicts the most classical architectures.



**Figure 96: Receiver topologies: homodyne (A), heterodyne (B) and super-heterodyne (C)**

Figure 96 (A) defines a homodyne type receiver (or zero-IF) basic architecture. The LO frequency is identical with the one of the RF input signal. Figure 96 (B) is very similar to (A) but the frequency of the LO does not match the RF, introducing an intermediate frequency, whose choice is based on a trade-off between selectivity and image frequency rejection. Finally, Figure 96 (C) depicts a super-heterodyne architecture, where two LO are required, but relaxes the trade-off found in heterodyne architectures [61].

The homodyne architecture was chosen over the others since there is no image frequency, it is also simple to design, and because it is highly favorable for integration. On the other hand, this topology will induce a DC offset, which will need to be taken into account. The topology (A) was selected in our transceiver design.

In our case Figure 96 (A) was adapted to get Figure 97 (A'). A double-balanced mixer cell is to be implemented to generate the differential quadratic signals through the I and Q path.

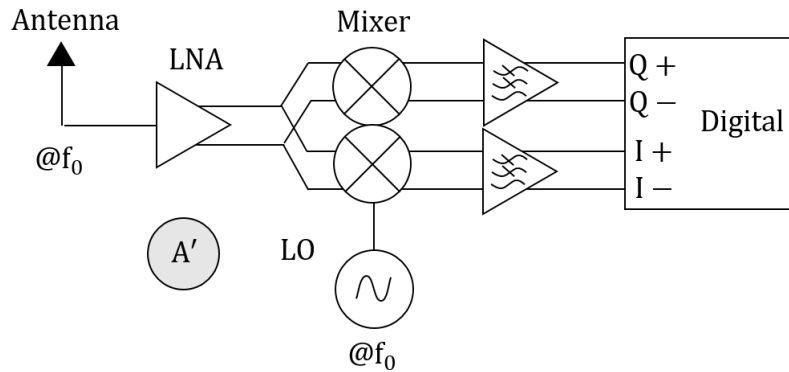


Figure 97: Quadratic receiver architecture basic illustration

This topology is based on a double-balanced mixer. In TX mode, the total BW is multiplied by 2. In RX mode, the image frequency is rejected, but will have a high sensitivity to phase and amplitude imbalance, induced by mismatch and process variation.

#### 4.1.3 DESIGN OF A DOUBLE-BALANCED PASSIVE MIXER

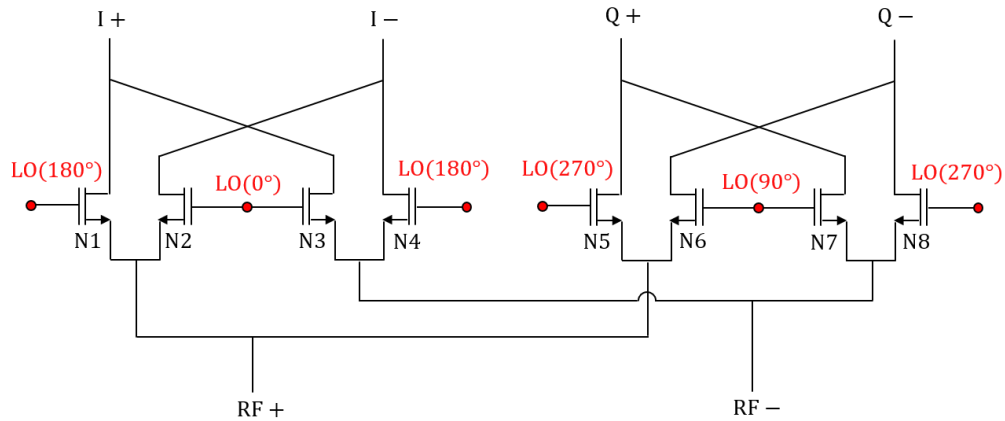
The figure-of-merit of RF mixers can be listed as below

- Noise figure (NF)
- Conversion gain (CG)
- Power consumption ( $P_{DC}$ )
- Linearity (IIP3)
- Port-to-port isolation ( $S_{12}$ ,  $S_{13}$ )

The port-to-port isolation is critical in direct conversion receiver as the LO swing is relatively high compared to the amplitude of RF signals. The conversion gain  $CG$  can either be positive (active mixers) or negative (passive mixer). In the latter case, the conversion gain is sometimes called insertion losses. The  $CG$  for double-balanced passive and active mixers are defined in [62] as

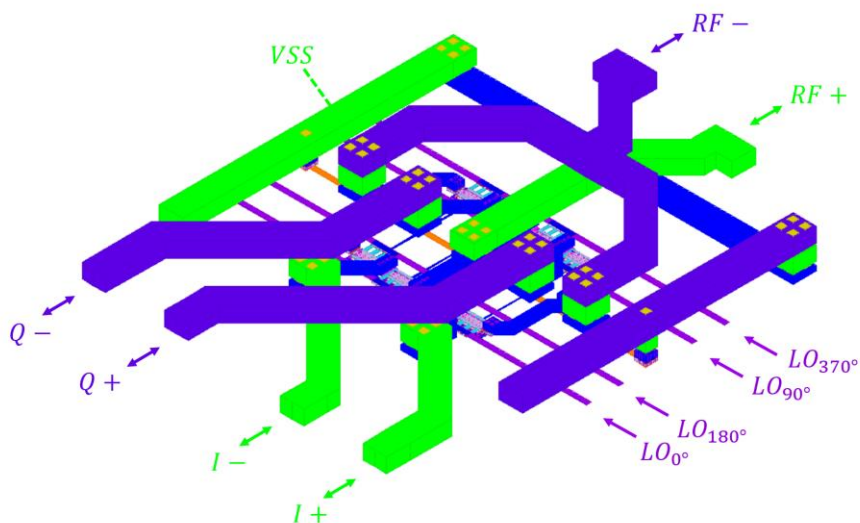
$$CG_{passive}^{opt.} = \frac{2}{\pi} \quad \text{and} \quad CG_{active}^{opt.} = \frac{2}{\pi} g_m R_D \quad (30)$$

It is clear from (30) that  $CG_{passive}^{opt.}$  is negative (in dB) while  $CG_{active}^{opt.}$  can be positive (in dB) for adequate couples of transistor transconductance and loading resistor ( $g_m$ ,  $R_D$ ).



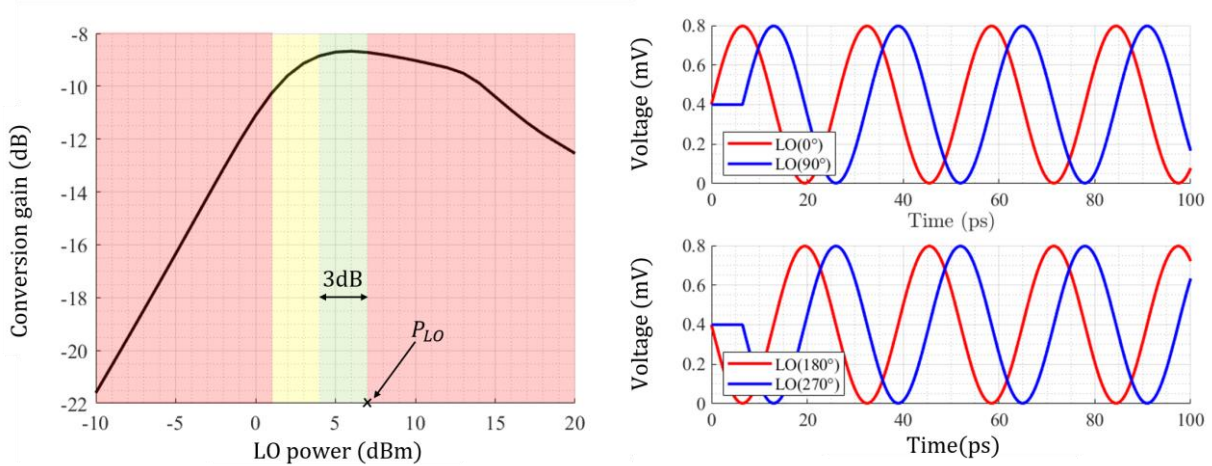
**Figure 98: Schematic of the proposed double-balanced passive mixer**

Active mixers are not conventionally bidirectional since active devices are not able to provide positive reverse gain, but isolation instead. However, there are examples of active mixers in the literature designed to enable a bidirectional operating mode as in [60] and [63]. Nevertheless, it is much simpler to use passive mixers as they are intrinsically bidirectional since they are based on series switches. The designed mixer is described in Figure 98. Gilbert mixers are widely used in RF integrated circuit designs as they provide both RF and LO feedthrough [64], reject even order distortion and provide a high linearity [58] and include the signal splitting/combining operation. This is why in this work; this topology has been chosen. The layout of the mixer was conducted as in Figure 99. The transistors were sized identically whose width is equal to  $40\mu\text{m}$ , with finger widths of  $1\mu\text{m}$ , and gate lengths of  $20\text{nm}$ , to mitigate the impact of both switches' intrinsic capacitances and on-state resistors.



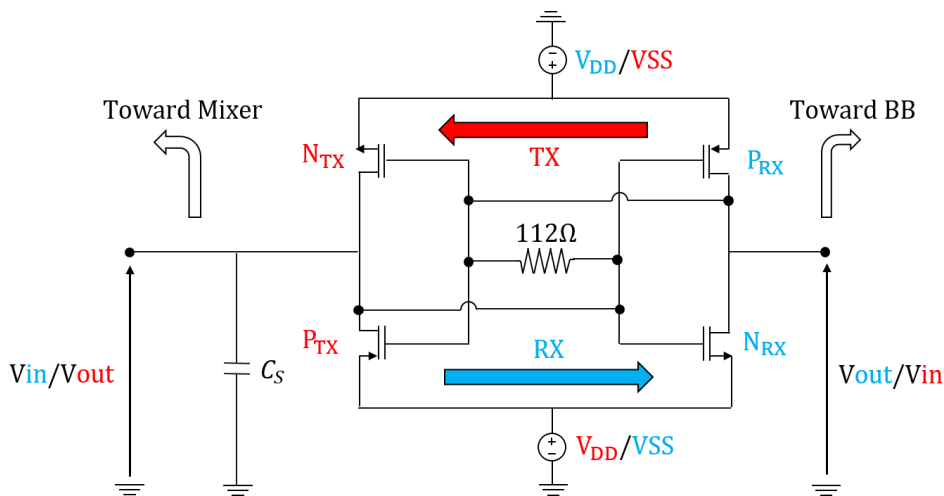
**Figure 99: 3D layout view of the proposed double-balanced passive mixer**





**Figure 100: TX I-path USB mixer CG with respect to the LO amplitude (left) and corresponding LO quadratic signals used as inputs for the designed mixer (right)**

The TX mode USB conversion gain of the designed mixer was plotted with respect to the LO amplitude  $P_{LO}$  Figure 100, and shows that – as predicted – a high voltage swing is required over the gate of transistors (N1-N8) to reduce the insertion losses.  $f_{LO}$  and  $f_{RF}$  are respectively 38.5GHz and 38.6GHz. The amplitude was chosen as such even if the effective  $P_{LO}$  is smaller than expected, the insertion losses remain almost constant (within the green area). The choice of the amplitude could however be restrained by the capability of the external source to deliver enough power. In this section,  $P_{LO}$  is set to 7dBm. A pseudo-differential self-biased bidirectional baseband amplifier (BBBA) was implemented in order to present a low impedance – conventionally done using a transimpedance amplifier (TIA) – at the output of the RF mixer in RX mode, as well as providing a highly linear amplification stage for the TX mode.



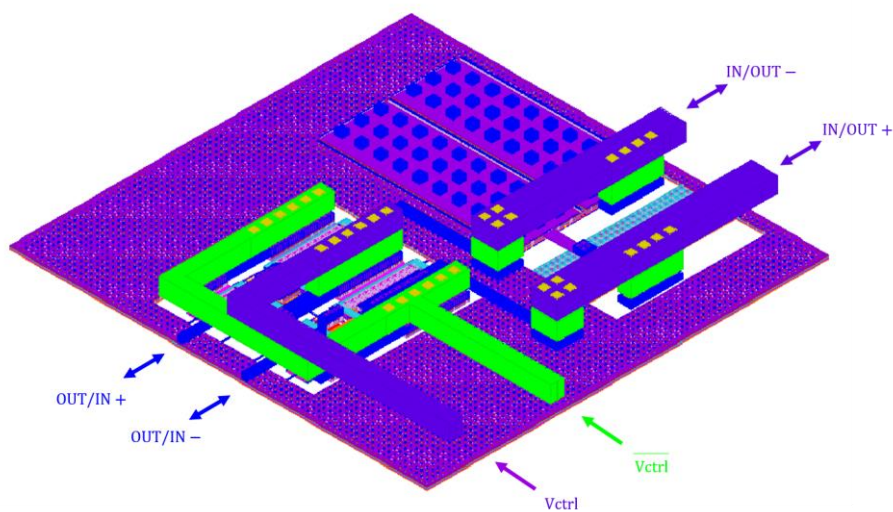
**Figure 101: Schematic of the TRX BBBA**

	$N_{TX}$	$P_{TX}$	$N_{RX}$	$P_{RX}$
$W$ ( $\mu\text{m}$ )	99	90	49.5	45

**Table 20: Transistors sizing summary of the TRX BBBA cell**

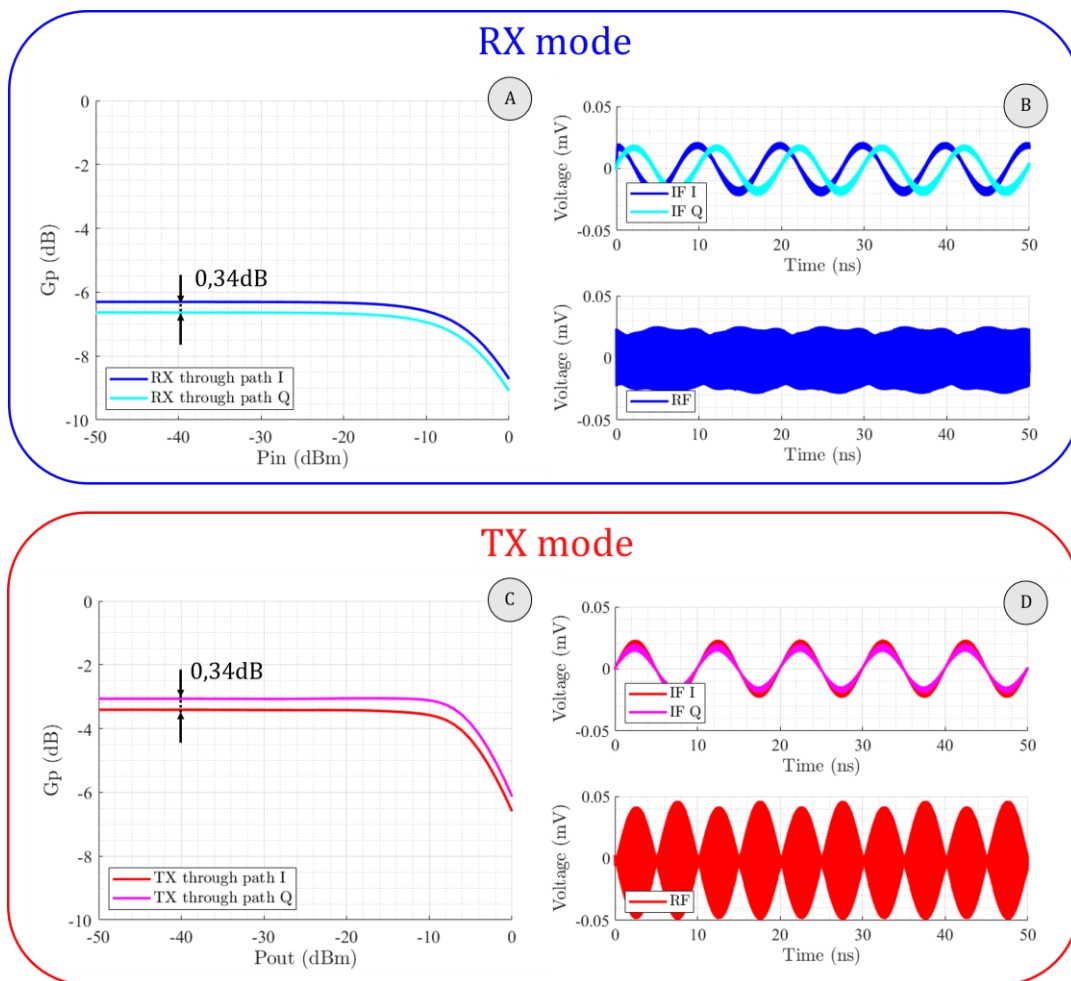
Initially, the whole TRX baseband chain was supposed to be implemented in a bidirectional fashion, reusing all electrical nodes. That is why no switched components were implemented in series with the feedback resistor in Figure 101.

The supply voltages located at the top and the bottom of this figure are alternatively  $V_{DD}$  and  $V_{SS}$ , resulting in switching ON or OFF the adequate inverter cells and providing a bidirectional operation mode and sharing the electrical nodes. Its performances will be included in the summary of the whole frequency conversion chain. The transistors length  $L$  was set to 40nm to optimize gain and widths are mentioned in Table 20. The inverter amplifier will also be fully characterized within the next chapter about the analog baseband building blocks designs. Shunt capacitors  $C_S$  were also implemented between the bidirectional baseband amplifier and the RF mixer to filter the RF component leaked within the IF path. Its value was fixed to 3pF. This architecture hence allows to reuse these large capacitors in both RX and TX mode. The layout was hence conducted as in Figure 102. Finally, transient simulations were performed in order to visualize the effect of frequency multiplication of this bidirectional passive mixer, in both modes as in Figure 103. In TX mode, the two I/Q branches are exited in phase (D top) and the resulting RF signal is plotted (D bottom), and the



**Figure 102: 3D layout view of the TRX BBBA**

corresponding insertion losses are exhibited (C). In RX mode, the RF terminal of the mixers is exited (B bottom), and both signal resulting in the I and Q branch are plotted (B top). Similarly, differential insertion losses are plotted (A) and the gain imbalance can be determined. In both cases, the signal multiplication is observed as expected, when in TX mode, the IF signal is up-converted into a high frequency signal while in RX mode, the RF signal is down-converted into a low frequency signal. The main difficulty in this design is also the propagation of the baseband common mode of  $V_{DD}/2$  since series decoupling capacitors cannot be used in this design without having an enormous value – and hence silicon footprint – since the lower corner frequency of the canal is fixed to 30kHz (and the upper frequency varies from 50MHz to 400MHz). The passive mixer has a DC power of 0mW while the bidirectional baseband amplifier (BBBA) consumes 4.2mW and 8.5mW in RX and TX mode respectively. At that time of the analysis, the I/Q LO signals are generated using an ideal voltage source.

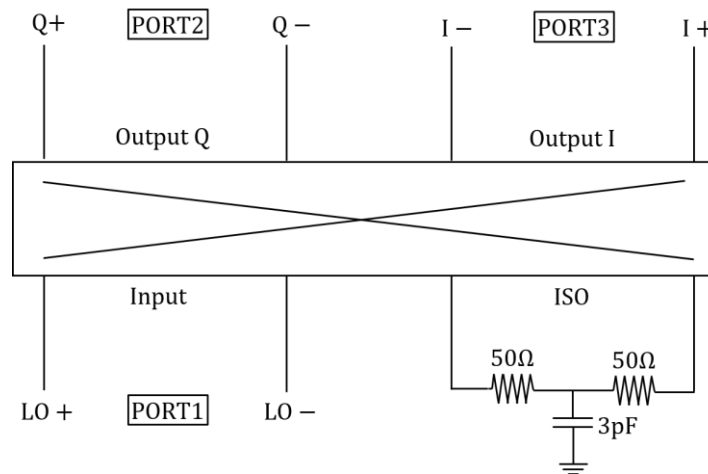


**Figure 103: USB conversion gain (a) and (c) and transient response (b) and (d) of the mixer and the BBBA using an ideal LO source in TX mode (red) and RX mode (blue)**

## 4.2 QUADRATURE LO GENERATION

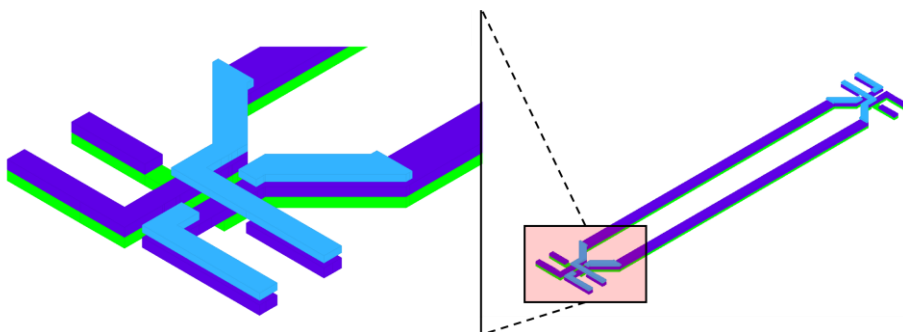
### 4.2.1 DESIGN OF A QUADRATURE HYBRID COUPLER

In this thesis, the oscillator design generating the LO signal was not covered. An off-chip external source was used instead. In order to get two differential signals in quadrature from a single-ended LO, multiples techniques are available such as using a hybrid coupler (HCPLR) based on magnetic coupling [65], or a polyphaser filter (PPF) [66], for instance. In our case we reused an existing HCLPR design, whose symbol is illustrated in Figure 104.

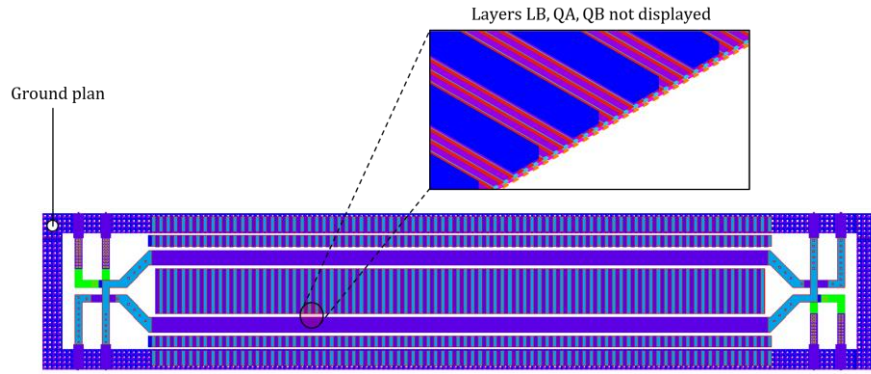


**Figure 104: Schematic of the proposed quadrature hybrid coupler**

A HCLPR is a 4-port device whose ports are respectively named I, Q, LO and ISO. In this case, the ISO port is terminated with a pseudo-differential 100Ω load, even though in our case, a 100Ω load would be adequate since the HCPLR is meant to be used with differential signals. The resulting differential signals in port 2 and port 3 are in quadrature. The layout is presented Figure 105 using the three top layers, including an enlarged view over two of the input

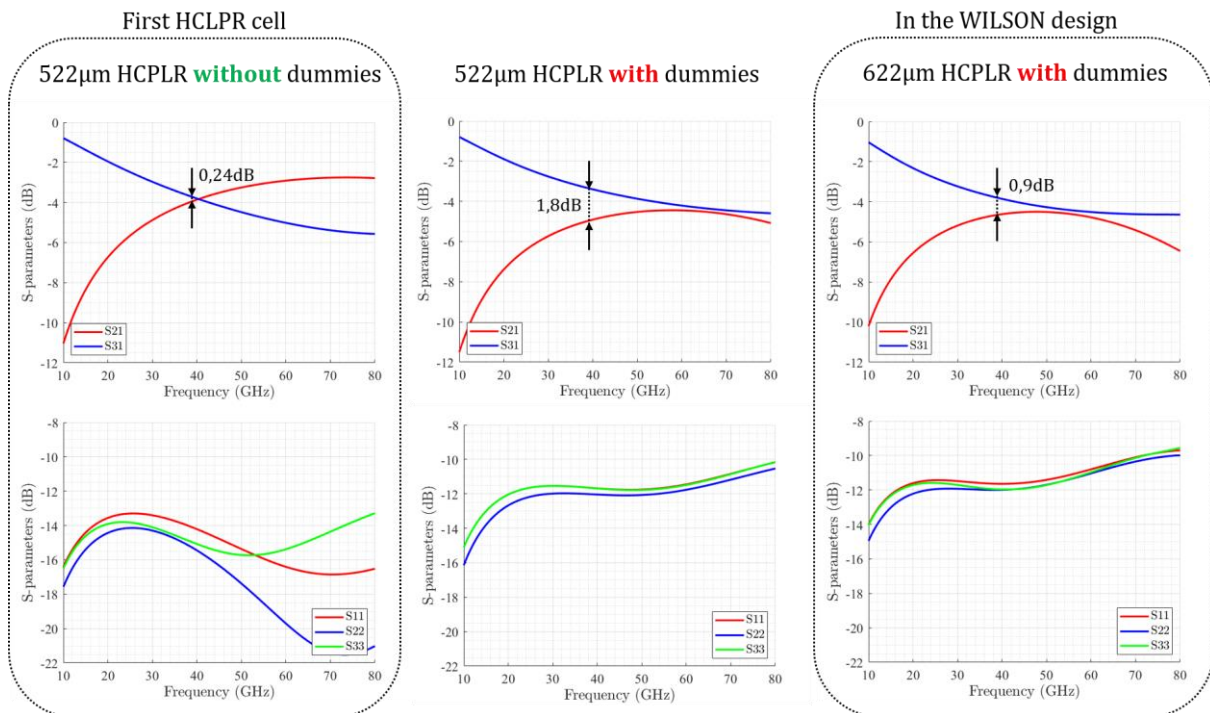


**Figure 105: 3D layout view of the proposed quadrature hybrid coupler**



**Figure 106: 3D layout view of the proposed hybrid coupler including the proposed dummies pattern**

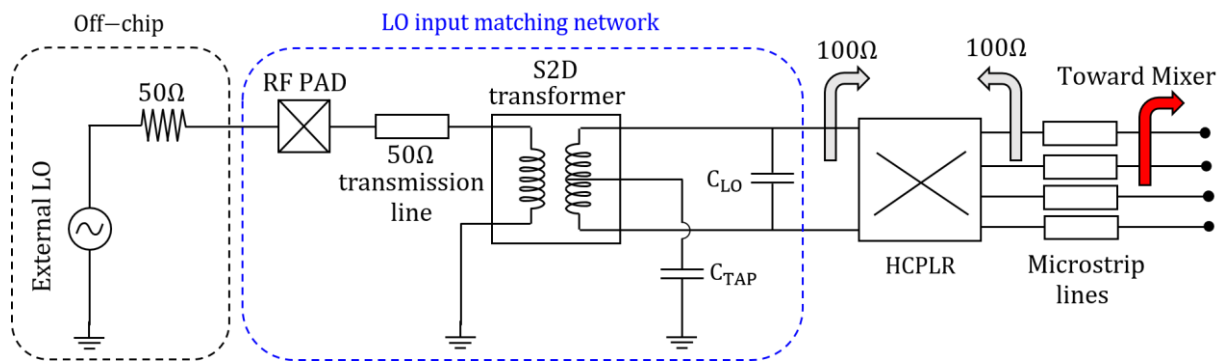
terminals. The main drawback of the HCPLR is its substantial size, that is not optimal for compact applications, and a PPF would have been preferred. Nevertheless, higher insertions losses are expected compared to the latter, and so LO buffers would have been required, resulting in a higher DC power, as well as a higher developing time. As it is very large, exclude layers could not be added to the whole surface of the HCPLR, and a dummies pattern is presented in Figure 106. In Figure 107 the post-layout S-parameters are plotted in various configurations: on the left, when the HCPLR is composed only of the coupling layers, in the middle when the dummies pattern is added, and in the right when the size is adjusted, exhibiting a final gain imbalance of 0.9dB.



**Figure 107: Designed HCLPR at a first length without (left) and with the dummies pattern (center) and with an adjusted length (right)**

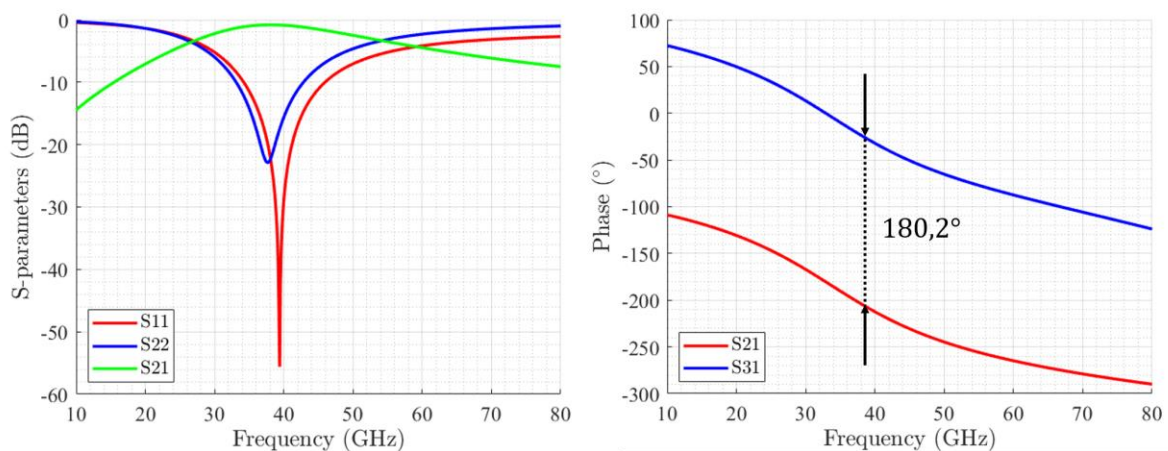
### 4.2.2 IMPEDANCE MATCHING

The signal generated using a 50Ω external LO source must be converted into a differential signal using a balun. This 50Ω source must also be matched with the 100Ω hybrid coupler using a matching network depicted as in Figure 108. This coupler will be responsible for the quadrature generation mandatory for the proper use of the double-balanced passive mixer.



**Figure 108: Impedance adaptation between the single-ended LO external source and the proposed hybrid coupler**

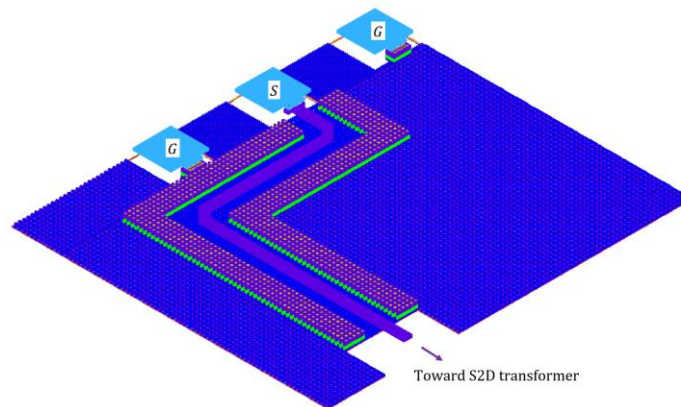
The S-parameters and the output phases of this matching network were plotted Figure 109 (left) where  $S_{21}$ ,  $S_{11}$  and  $S_{22}$  are respectively -0.8dB, -25.8dB and -20.9dB and the output is (almost) perfectly differential at 38.5GHz. In this design, the single-to-differential (S2D) transformer's  $ID$  is 77μm, and the tuning capacitors  $C_{LO}$  and  $C_{TAP}$  are respectively equal to



**Figure 109: 2-ports and 3-ports S-parameters of the LO input matching network without the 50Ω TL**

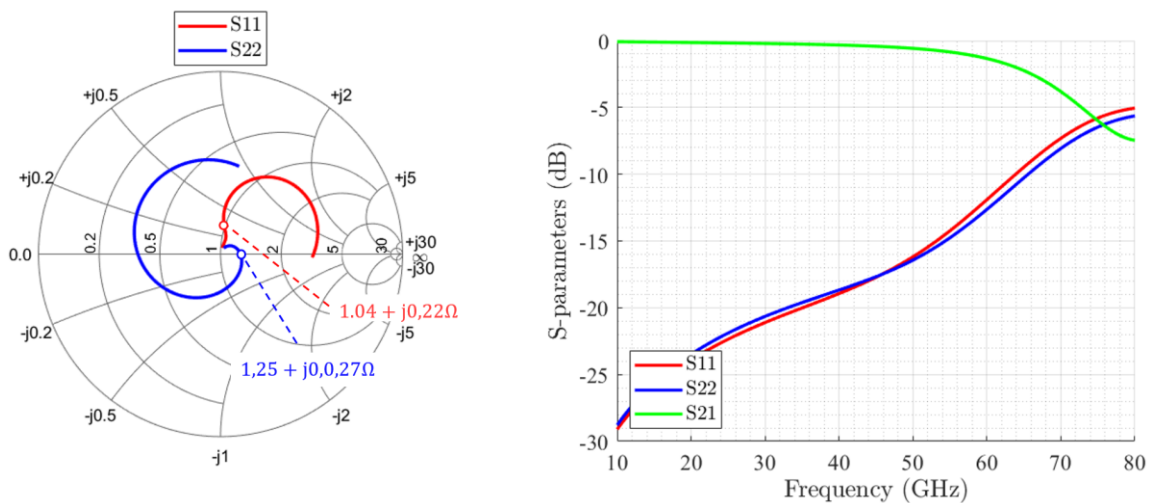
113fF and 1.56pF (right). In this analysis the 50Ω TL is no yet taken into account, and assumed ideal at this point.

Finally, in order to connect the balun to the RF LO GSG pad, a 50Ω transmission line was implemented and characterized. In this work, this single-ended 50Ω transmission line was chosen to be as long as possible to eliminate the need for a differential transmission line placed after the S2D transformer that could have led to a potential differential mode deterioration.



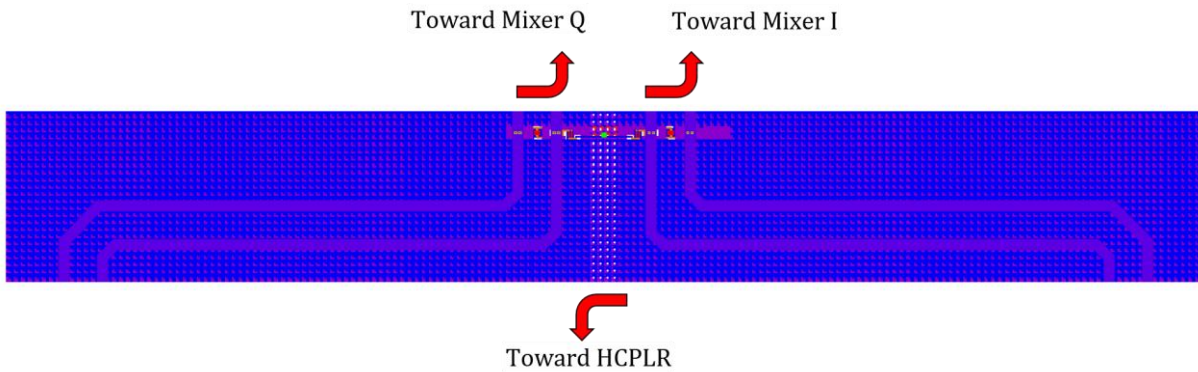
**Figure 110: 50Ω transmission line used in the distribution of the external LO to the S2D transformer**

The transmission line is depicted in Figure 110 as it will be implemented in the final integrated transceiver WILSON chip (Chapter 6). The transformer is hence placed as close as possible to the input of the HCPLR. This transmission line is characterized in Figure 111 exhibiting  $S_{21}$  of -0.3dB and input and output reflexion coefficient below -15dB at 38.5GHz.



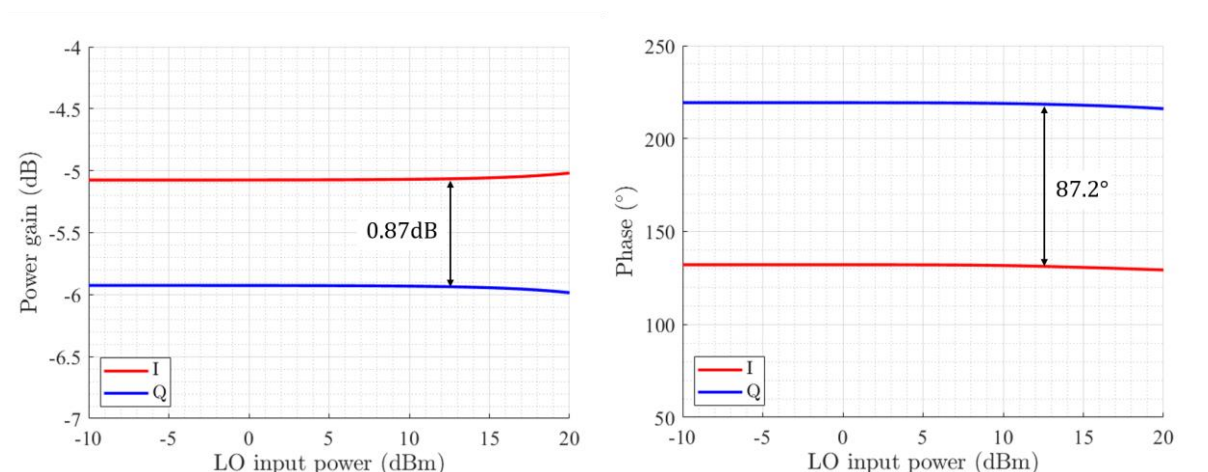
**Figure 111: S-parameters of the 50Ω transmission line in a smith chart (left) and in decibels (right)**

The output of the hybrid coupler is interconnected with the mixer through a microstrip line as in Figure 108, whose layout is presented in Figure 112. Two  $100\Omega$  shunt resistors were added between respectively the Q+ and Q- as well as I+ and I- nodes, to refer the output power level to a fixed impedance value, and a  $V_{DD}/2$  common-mode was applied.



**Figure 112: Double-balanced micro strip line used in the distribution of the quadratic LO to the RF Mixer**

Finally, a performances summary of the I/Q LO generation chain was plotted in Figure 113 with respect to the LO input power, in order to verify the power-handling of the HCPLR as to the gain and phases imbalances. As expected, being based on passive elements, the I/Q LO generation chain can handle a high LO drive without significant distortions. From Figure 113 the output quadratic phase condition and gain imbalance remain unaffected by the increase of the LO drive level, while the differential gain imbalance between the I and Q terminals is  $0.87\text{dB}$ , and the differential phase imbalance is  $2.8^\circ$  at the selected LO power ( $12.5\text{dBm}$ ).



**Figure 113: Quadrature LO generation gain and phase imbalance**



### 4.3 PERFORMANCES SUMMARY OF THE INTEGRATED FREQUENCY CONVERSION CHAIN

The specifications over both TX and RX frequency conversion chains were established and reported in Table 21 and Table 22.

TX mixer + HCPLR + BBBA	
	Specification
Gain imbalance (dB)	$\pm 0.5$
Phase imbalance ( $^{\circ}$ )	$\pm 2$
Insertion losses (dB)	0
LO leakage (dBc)	-30
Image rejection (dBc)	-30

*Table 22: TX mixer performances specifications*

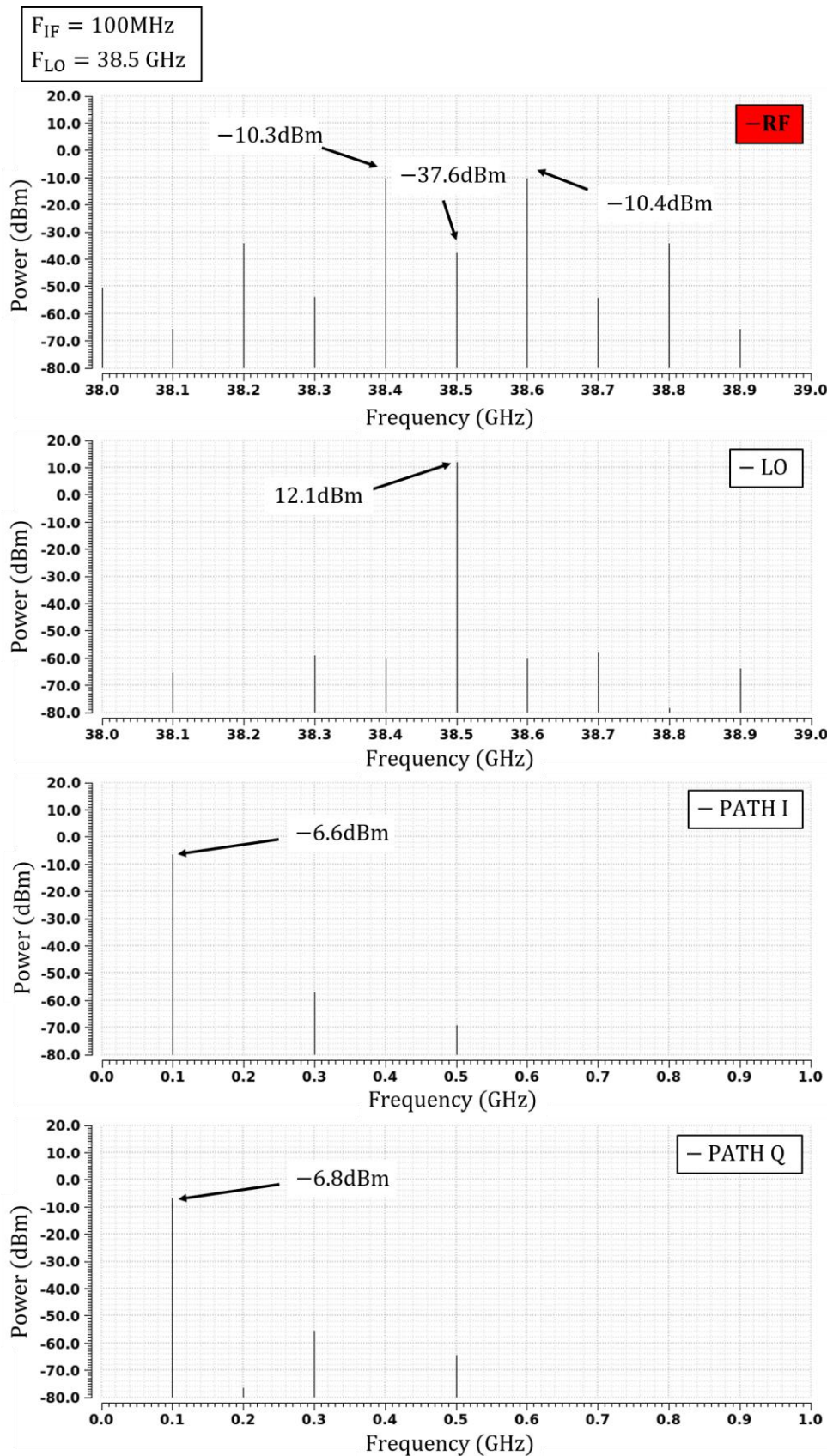
RX mixer + HCPLR + BBBA	
	Specification
Gain imbalance (dB)	$\pm 1$
Phase imbalance ( $^{\circ}$ )	$\pm 3$
Insertion losses (dB)	0
LO leakage (dBc)	-30
NF (dB)	12

*Table 21: RX mixer performances specifications*

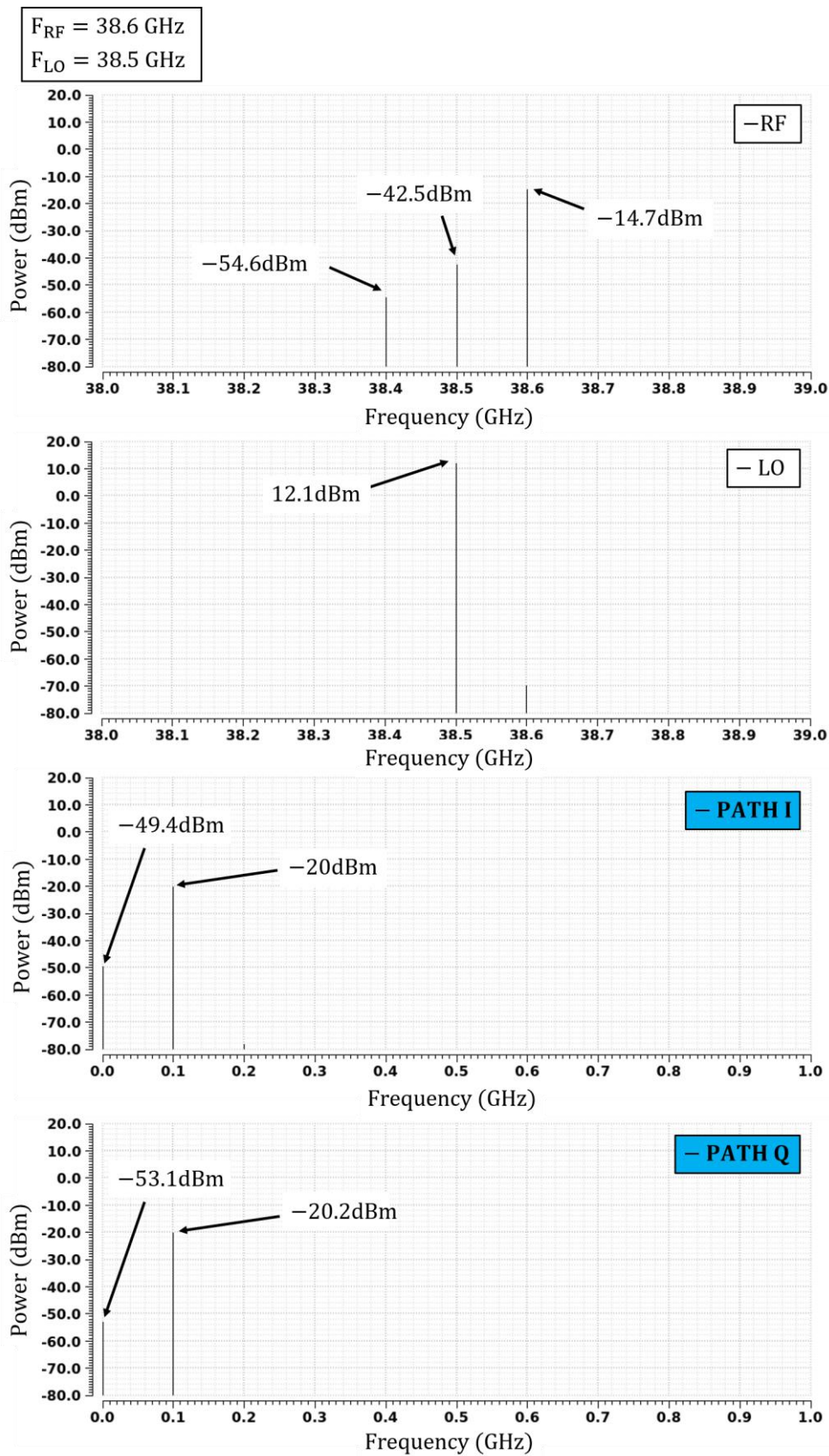
This section includes the post-layout simulations of the electromagnetic models of

- The bidirectional double-balanced passive mixer
- The bidirectional baseband amplifier (BBBA)
- The HCPLR including the dummies pattern, his matching network
- The GSG RF pads

The output spectrums of this frequency conversion chain are plotted Figure 114 in TX mode and Figure 115 in RX mode and the up- and down- conversion can be respectively observed.



**Figure 114: Spectral characterisation of the frequency conversion chain in the TX up-conversion mode at maximal input power (TX power budget)**



**Figure 115: Spectral characterisation of the frequency conversion chain in the RX down-conversion mode at maximal input power (RX power budget)**

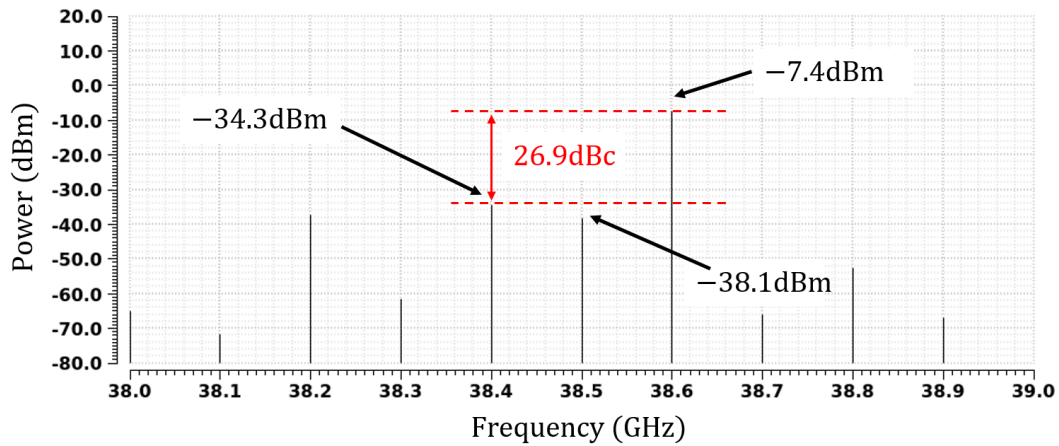


Figure 116: TX up-conversion mode image rejection plot when using the I/Q path in quadrature

In the TX and RX mode the LO leakage is respectively -50.2dBm and -54.6dBm. In the TX mode, as expected, using in-phase baseband inputs, the power is spread equally within the USB and LSB. In the TX mode, using quadratic baseband inputs, the image frequency is rejected by 26.9dBc as in Figure 116. As to the RX noise analysis, the single-sideband (SSB) NF through path I and path Q is 18.6dB and 18.8dB respectively, as in Figure 117. The I-path and Q-path DC offset is respectively -49.4dBm and -53.1dBm. These levels are not equal due to the presence of mismatch.

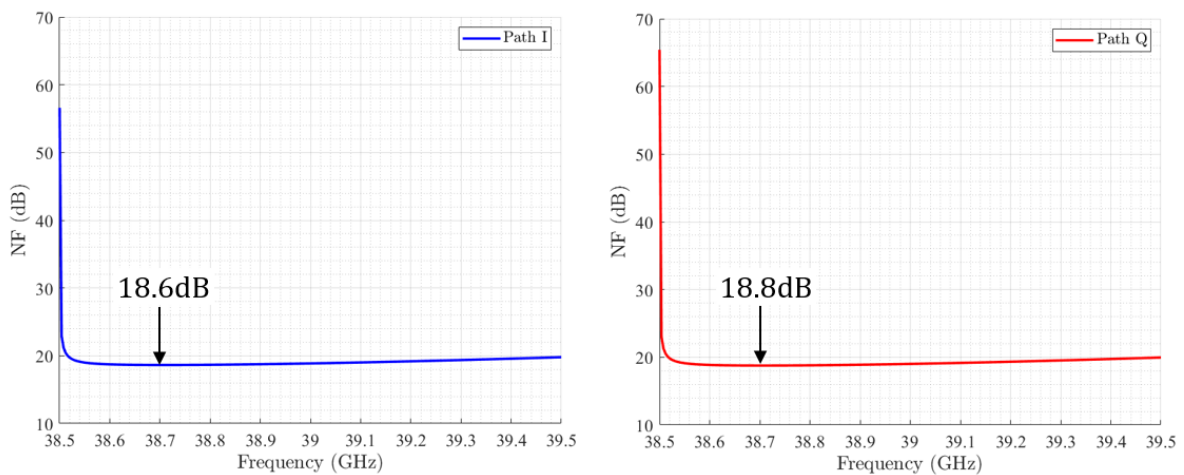


Figure 117: SSB NF of the frequency conversion chain in RX mode through the I and Q path

Finally phase and gain imbalances of the entire frequency chain were studied in Figure 118. In TX mode, the phase imbalance varies is  $2.6^\circ$  at most while the gain imbalance remains below 1dB. In RX mode, the I/Q relative phases vary more exhibiting a phase variation of  $7^\circ$ , and a gain imbalance also below 1dB. The phase imbalance is due to the improper phase condition of signals generated by the HCPLR, and more precisely affected by the selected

dummies pattern. Indeed, a complementary study would be required to propose a better choice of pattern/length in the HCLPR design to mitigate its impact.

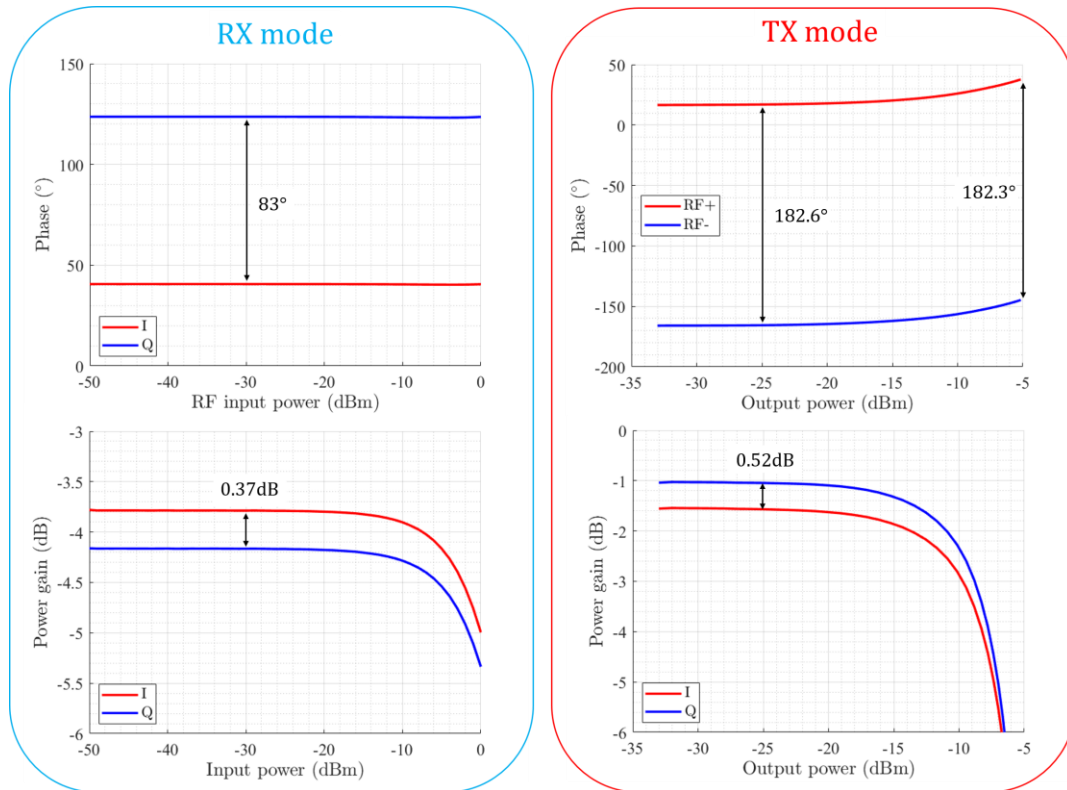


Figure 118: Phase and USB gain imbalance in TX mode and in RX mode of the frequency conversion chain

#### 4.4 CONCLUSION

As a conclusion, initial specifications were compared with post-layout simulation results in the TX and the RX modes in Table 23 and Table 24.

TX mixer + HCPLR + BBBA		
	Specification	Post-layout simulations
Gain imbalance (dB)	$\pm 0.5$	0.54
Phase imbalance ( $^{\circ}$ )	$\pm 2$	$< 2.6$
Insertion losses (dB)	0	$> 1.6$
LO leakage (dBc)	-30	-50.2
Image rejection (dBc)	-30	-25

Table 23: TX mixer post-layout performances compared with specifications

RX mixer + HCPLR + BBBA		
	Specification	Post-layout simulations
Gain imbalance (dB)	$\pm 1$	$< 1$
Phase imbalance ( $^{\circ}$ )	$\pm 3$	7
Insertion losses (dB)	0	$< 4.1$
LO leakage (dBc)	-30	-54.6
NF (dB)	12	18.6 (SSB)

**Table 24: RX mixer post-layout performances compared with specifications**

From these tables, three axes of improvement can be identified. The image rejection ratio can be improved by reducing the mismatch induced by the layout. As to the noise figure, it can either be improved using a different topology of BBBA, or either changing the initial noise budget and adding more constraints over other blocks. As to the subsequent phase imbalance that will lead to an EVM deterioration, another dummies pattern is to be investigated to mitigate its impact.



# Chapter 5: ANALOG BASEBAND BUILDING BLOCKS

**M**ost of signal processing operations are usually done in the analog baseband domain as it is less silicon- and power-hungry and less challenging than in the RF domain. The analog baseband processing is about the shaping of electrical signals to be emitted or to be received. As the real-world electronics is composed of multi-harmonics signals, the first aspect is about filtering, or rejecting the non-valuable harmonics, without altering the quality of the data. It is also about amplifying signals since DACs cannot increase their output current indefinitely to drive the 50Ω input load (in TX mode) and also because, because received data can have extremely low amplitude (in RX mode). Within this section, the baseband front-end of the system will be presented through various designs, each one being preceded with important basics reminders. The key functions that were designed in this chapter are listed as below

- A Variable Gain Amplifier (VGA)
- Two low-pass filters (LPF)
- A Double Pole Double Throw (DPDT) switch
- A 50Ω buffer
- A bidirectional baseband amplifier (BBBA) – mentioned in the previous chapter

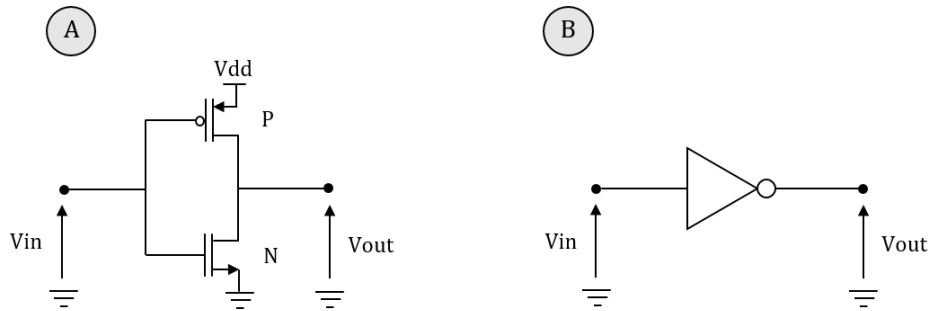
In each case, initial performances were compared with actual results in order to conclude over the relevancy of the chosen architecture.



## 5.1 VARIABLE GAIN AMPLIFIER

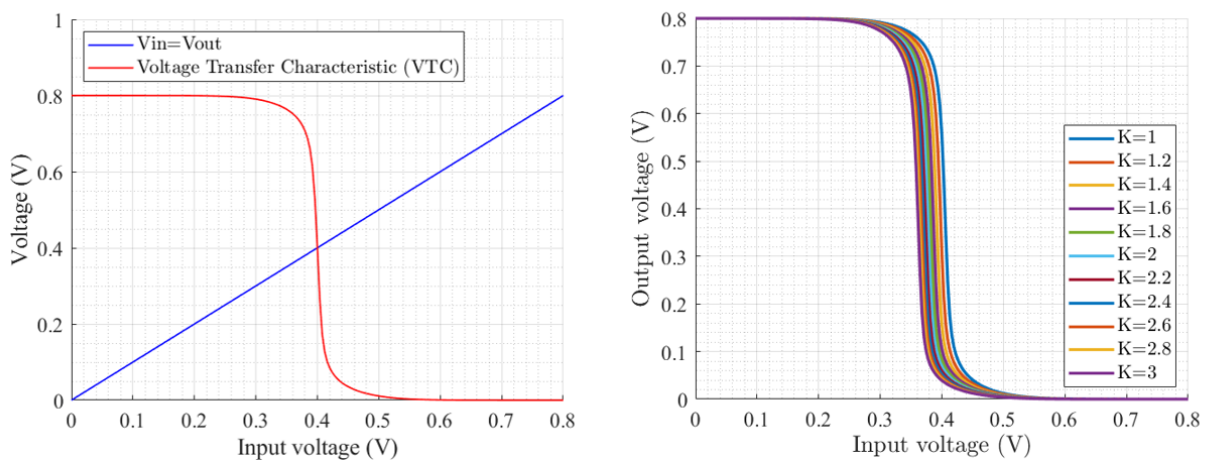
### 5.1.1 AMPLIFIER UNITY CELL: THE INVERTER CELL

In this work, baseband transconductance cells were realized using inverters, whose schematic and symbol are defined in Figure 119.



**Figure 119: Schematic of an inverter cell (A) and its associated symbol (B)**

Inverter cells are elementary functions used in digital and analog functions as they benefit for a high integration capability (no capacitors nor inductors required), a rail-to-rail output swing (from  $V_{SS}$  to  $V_{DD}$ ) [67], an enhanced gain at high frequency and at low power, where the gain is being proportional to the sum of NMOS and PMOS transconductance (respectively  $g_m^N$  and  $g_m^P$ ) and without any internal nodes [68]. The relative sizing of PMOS with respect to NMOS is done to set the maximum gain reached for an input common mode (CM) located at half- $V_{DD}$  as in Figure 120, using the ratio  $K_T = W_N/W_P = 1.15$ , with *s/vt* transistors with a gate length of 40nm.

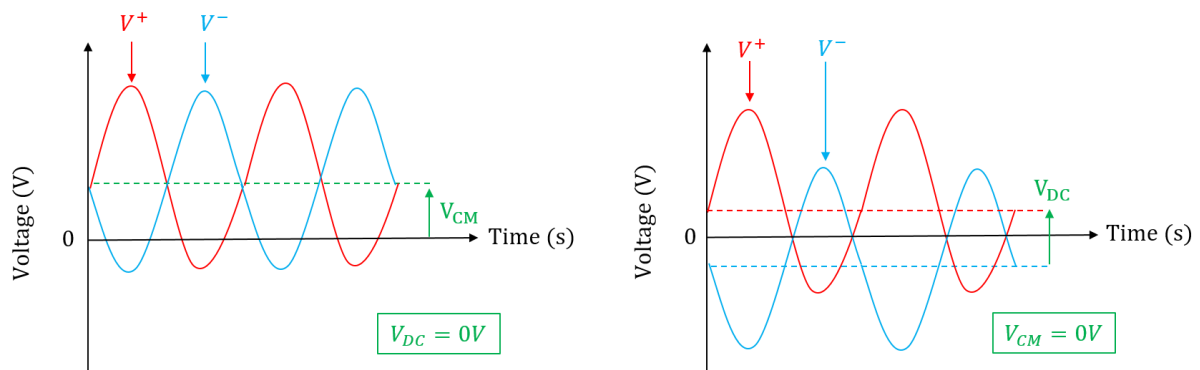


**Figure 120: VTC of the designed inverter cell (left) and impact of variation of  $K_T$  over the VTC (right)**

### 5.1.1 DC OFFSET AND COMMON MODE

The DC offset and the common mode (CM) are two key concepts in the design of baseband functions as they can drastically change the behaviour of an electrical function if not properly being taken care of. The common mode is defined as the mean value between two single-ended signals over a time period, while the DC offset represents the difference between the positive and negative signals of a differential signal. They are both expressed in **(31)** and illustrated as in Figure 121.

$$\begin{aligned} V_{DC} &= V^+ - V^- \\ V_{CM} &= \frac{V^+ + V^-}{2} \end{aligned} \quad (31)$$



**Figure 121: Common mode (left) and DC offset (right) illustration**

In direct conversion receivers (DCRs) the DC offset is mainly caused by the self-mixing of the LO through the mixer, and by the mismatch of the circuitry [69]. It can either be attenuated using a high-pass filter (HPF) or a cancellation feedback-loop (DCOC). As to the common mode it has to be stabilized using common mode stabilization loops (CMSL) or common mode feedback (or forward) loops (CMFB) respectively using an internal stabilization loop, generating and forcing the wanted CM on a given node, using multiple architectures [70], or using an external CM regulation loop, commonly based on the detection of the average output error, being amplified, and brought back to the input [71].

Amplifiers need to be free of these two variations as much as possible, because the DC offset and CM variations would most likely lead to the saturation of the next stages, and greatly deteriorate performances [72].

### 5.1.2 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The chosen operational transconductance amplifier (OTA) topology was taken from [73]. This architecture includes a CMSL composed of N3-N8 where the common mode is generated by N3,4 [74] and is amplified and isolated from the output by N6,8 while N5,7 provide input isolation. Transistors N1,2 provide the gain of the amplifier.

All transistors were sized identically where  $W_N$  and  $W_P$  are respectively  $11.5\mu\text{m}$  and  $10\mu\text{m}$ . The gate length is set to  $40\text{nm}$ .

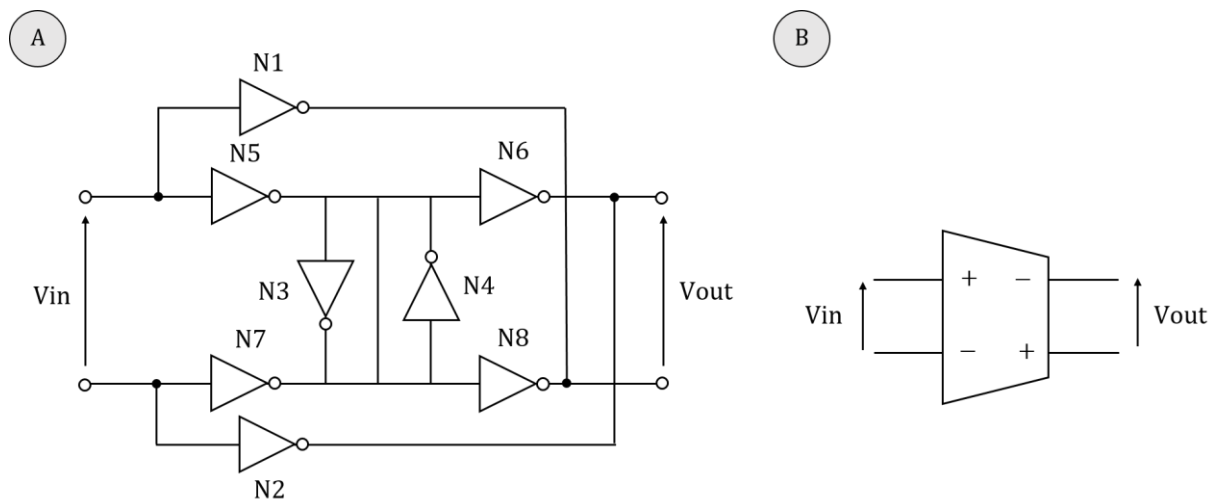


Figure 122: Schematic of the designed OTA (A) and its associated symbol (B)

In order to characterize an open-loop amplifier, two margins are usually employed to indicate the feedback phase and gain margins – respectively  $M_\varphi$  and  $M_G$  – defined as follows

$$M_\varphi = \arg(H_{OL}(j\omega_{0dB})) + 180^\circ \quad (32)$$

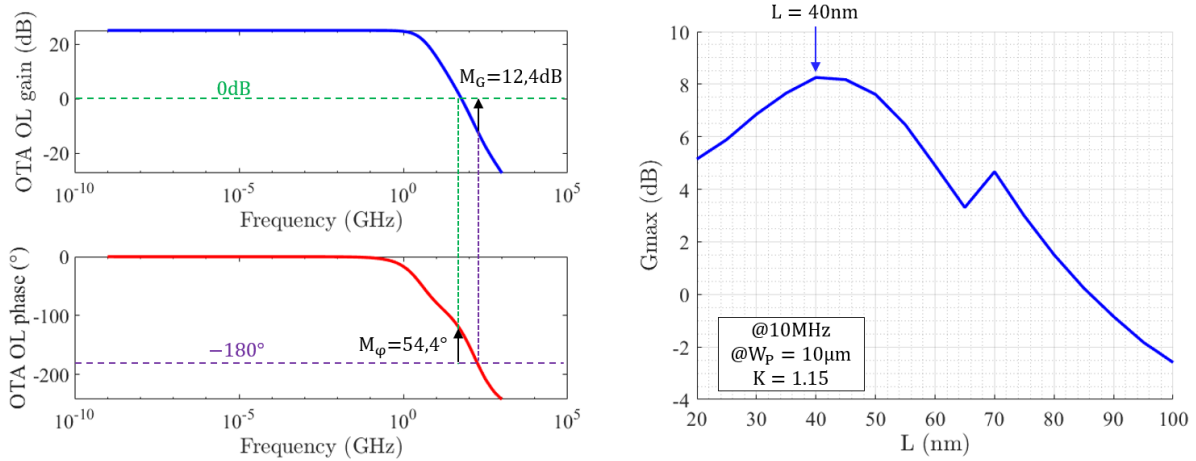
$$M_G = -20\log(|H_{OL}(j\omega_{-180^\circ})|)$$

The stability of the OTA is guaranteed when  $M_\varphi$  and  $M_G$  are typically within the following ranges

$$30^\circ \leq M_\varphi \leq 60^\circ \quad (33)$$

$$M_G \geq 6\text{dB}$$

These margins were highlighted from the bode plot of the designed OTA (open-loop) Figure 123. The OTA exhibits a  $M_\varphi$  of  $54.5^\circ$  and a  $M_G$  of  $12.4\text{dB}$  as well as a DC gain of  $25\text{dB}$ .



**Figure 123: Open-loop Bode plot of the designed OTA (left) and selection of the VGA transistor gate length (right)**

Now that the OTA was characterized, the variable gain amplifier (VGA) design will be presented in the next section.

### 5.1.3 DESIGN OF A VARIABLE GAIN AMPLIFIER

#### 5.1.3.1 Specifications

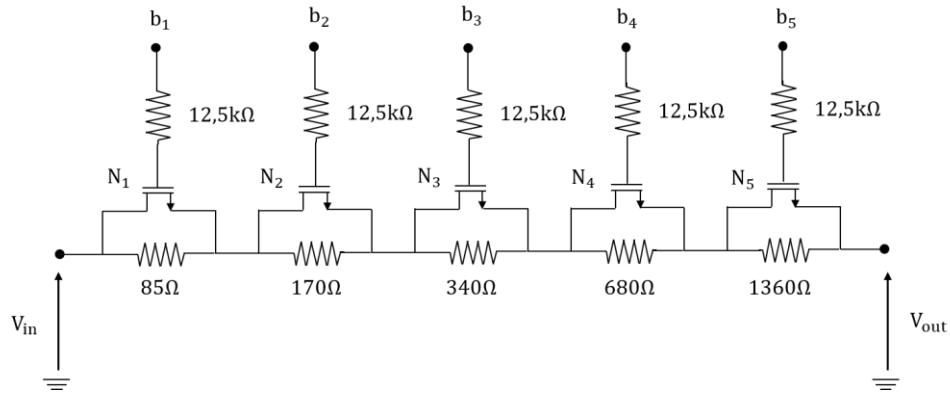
The specifications of the RX VGA were summarized in Table 25.

RX VGA	
	Specification
Gain range (dB)	7 – 50
Step size (dB)	0.5
CMRR (dB)	30
DCOC (dBc)	-40
-3dB BW (GHz)	> 1
NF (dB)	20

**Table 25: Specification table of the RX VGA**

Among the specification listed above, as it was mentioned in the previous section, this VGA will have to contain a DC cancellation loop (DCOC) as well of a strong rejection of the common mode.





**Figure 125: Schematic of the proposed variable resistor chosen for  $R_A$**

The value of the unity resistor  $R_0 = 85\Omega$  is sized to obtain a step size of 0.5dB. In [75] the lower cut-off frequency  $\omega_{HPF}$  as well as the DC attenuation  $A_{DC}$  can be derived as

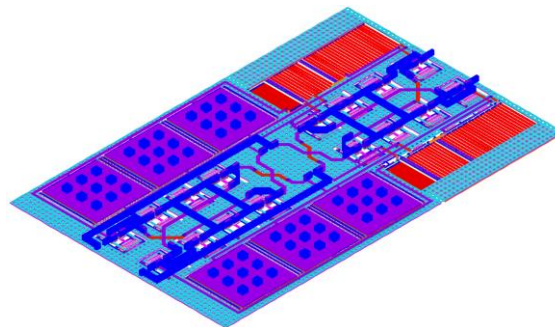
$$\omega_{HPF} = \left(1 + A_2 \frac{R_B}{R_C}\right) \left(\frac{1}{C_0 R_C A_2}\right) \quad (36)$$

$$A_{DC} = 1 + A_2 \left(\frac{R_B}{R_D}\right) \quad (37)$$

The values of the lumped components used in this design are listed within Table 26 and the layout is presented Figure 126. In this design PDK *npcres* (N+ Polysilicon Silicided) resistors and *apmom* (2.5V APMOM) capacitors were used. As to the resistors used for the application of the digital command, PDK *reopnarnpcres* (Narrow High-R N+ Polysilicon OP) resistors were used instead.

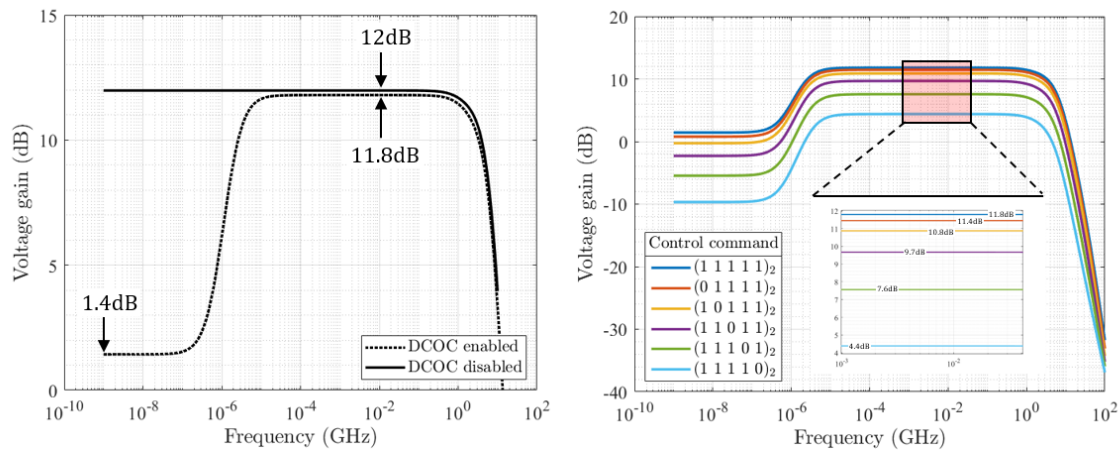
$R_B$	$R_C$	$R_D$	$C_0$
4625 $\Omega$	5M $\Omega$	11561 $\Omega$	1pF

**Table 26: Value of lumped resistors used in the design of one stage of the VGA**



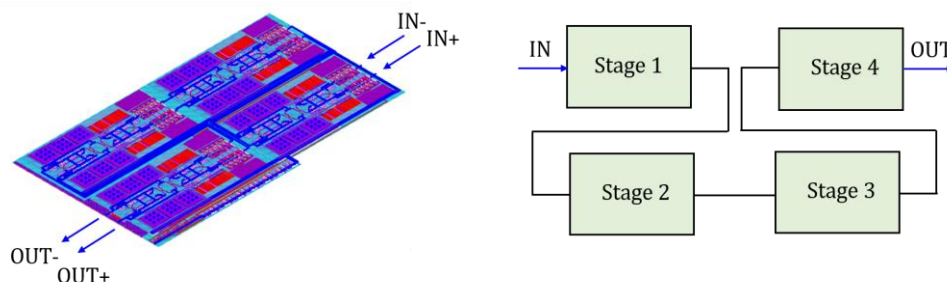
**Figure 126: 3D layout view of one stage of the proposed VGA**

As the gain of the VGA is only controlled by the input resistors  $R_A$ , (36) and (37) would suggest that both  $\omega_{HPF}$  and  $A_{DC}$  will remain constant for a fixed ratio  $R_B/R_C$ . However, using  $R_B$  as a parameter for multiple gain modes, will also require a change in the value of  $R_C$  to guarantee a constant  $\omega_{HPF}$ . It will also change the required values for  $R_A$  as the closed-loop gain of an ideal OPAMP is defined as the ratio  $R_B/R_A$ .



**Figure 127: Voltage gain of only one stage of the VGA with and without the DCOC loop (left) and gain variation caused by the 5 bits digitally-controlled switched resistor (right)**

Figure 127 depicts the voltage gain of one stage of the VGA with and without the DCOC loop. As it is shown in the left, the DC is rejected by 10.6dB as it should, when enabling the feedback loop. It also exhibits a variation of the lower and upper cut-off frequencies of roughly from 1.8kHz to 2.9kHz and from 4.8GHz to 3.5GHz respectively (in the right). Hence, each bit is alternatively activated in order to illustrate the gain decrease due to the increase of the series input resistor. Each switched resistor has a different weight over the gain decrease (respectively 0.4, 1, 1.9, 3.8 and 7.4dB Figure 127). The final VGA integrated in the final chip is composed of four stages wired in a square shape to enhance compacity as in Figure 128.



**Figure 128: Layout and arrangement of the square-shaped four-staged VGA including the binary command multiplexing**

### 5.1.3.3 Four stages RX VGA

The strategy employed was to provide the gain over four stages of variable gain amplification as in Figure 129. In order to lower the noise contribution of the RX VGA, the gain of stages is lowered from the last to the first stage (Friis formula). Among the seven bits involved, two bits are used to select the adequate stage and the five remaining bits are used as in the previous schematic to control the value of the input resistors  $R_A$ .

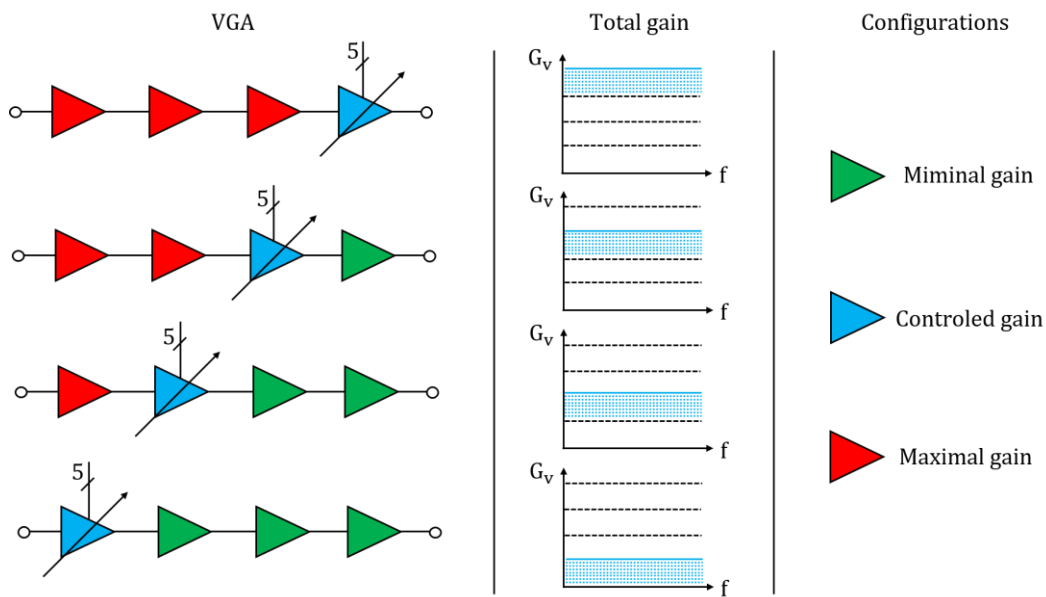


Figure 129: Gain control strategy of the four stages RX VGA

The maximal gain range of the VGA is described Figure 130 where the minimal and maximal reachable gains are respectively 8dB and 48.5dB. The VGA consumes 39mW at maximal gain.

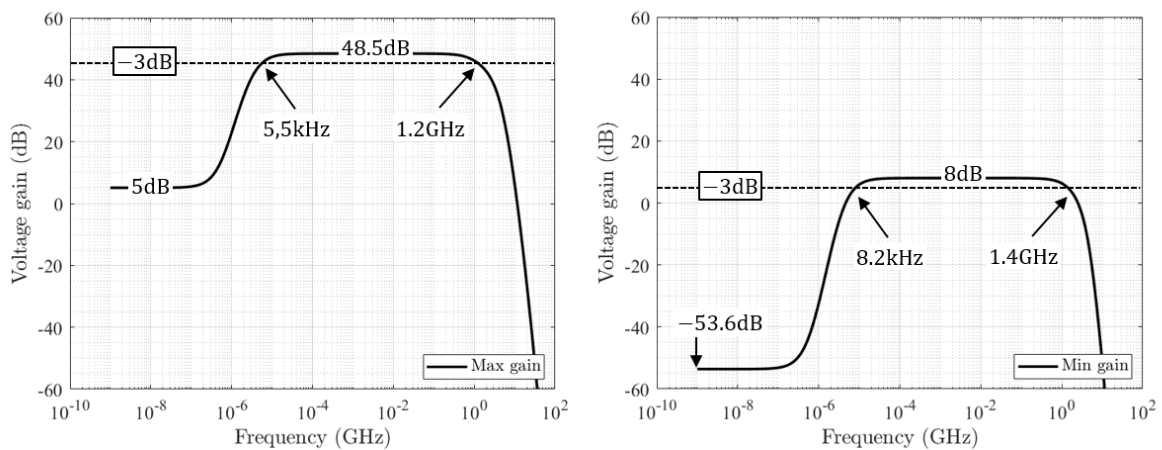
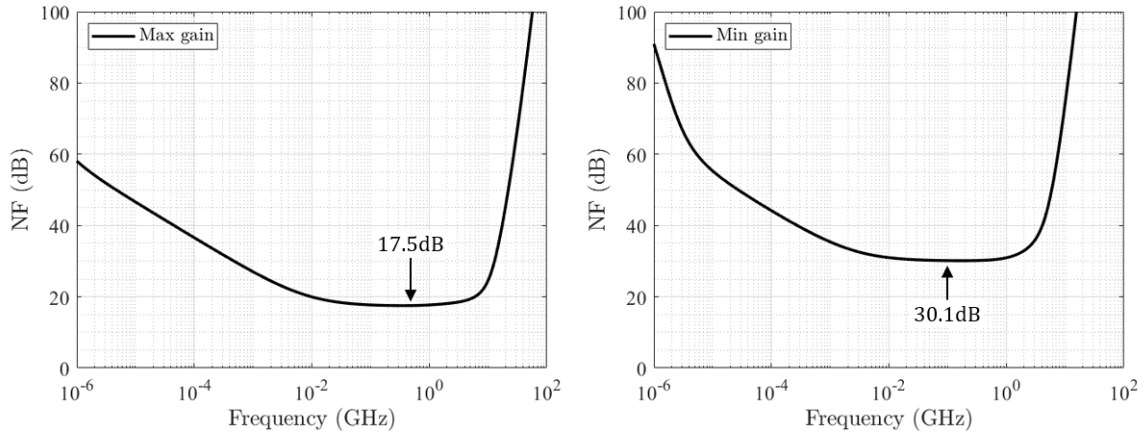


Figure 130: Four-staged RX VGA in the highest (left) and lowest (right) gain configuration

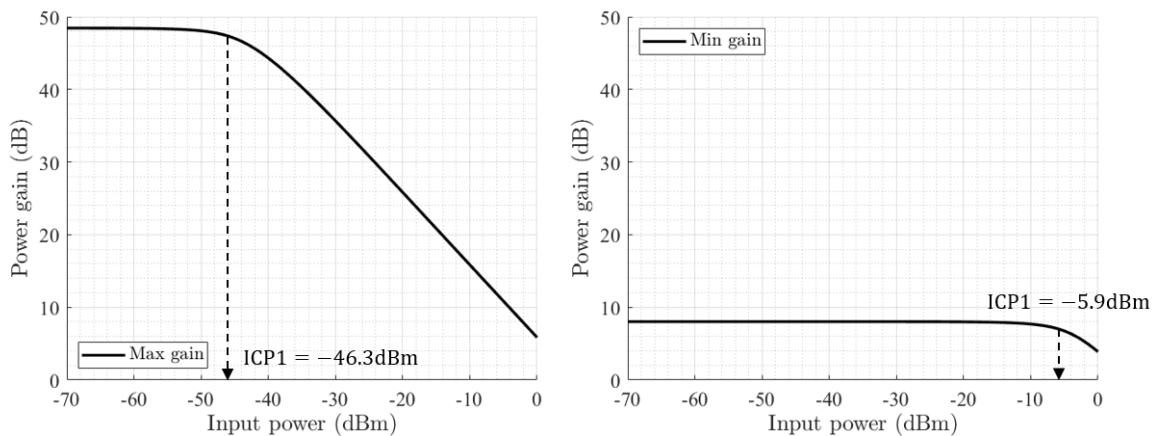


The noise was hence investigated Figure 131 within the two most critical configurations, where a NF of 17.5dB is achieved in the maximal gain configuration, and 30.1dB when the VGA performs the lowest gain.



**Figure 131: Four-staged RX VGA NF in the highest (left) and lowest (right) gain configuration**

Finally, the power-handling capability of the VGA was considered within the maximal and minimal gain configurations in Figure 132, exhibiting a variation of the ICP1 from -46.3dBm to -5.9dBm.

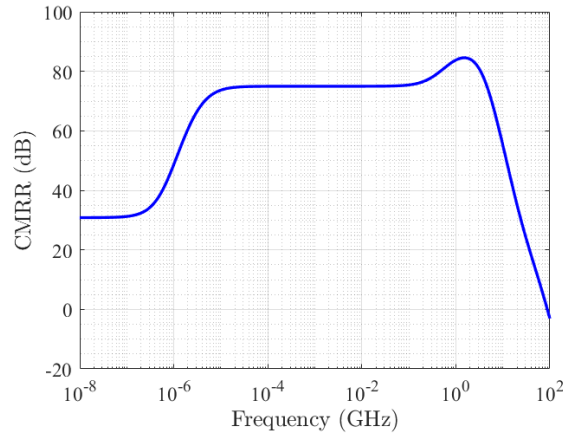


**Figure 132: Power gain with respect to the input power of the designed four-staged RX VGA in the highest (left) and the lowest (right) voltage gain configuration**

The common mode rejection ratio is defined as a function of the differential voltage gain  $A_v^d$  and the common mode voltage gain  $A_v^{cm}$  as

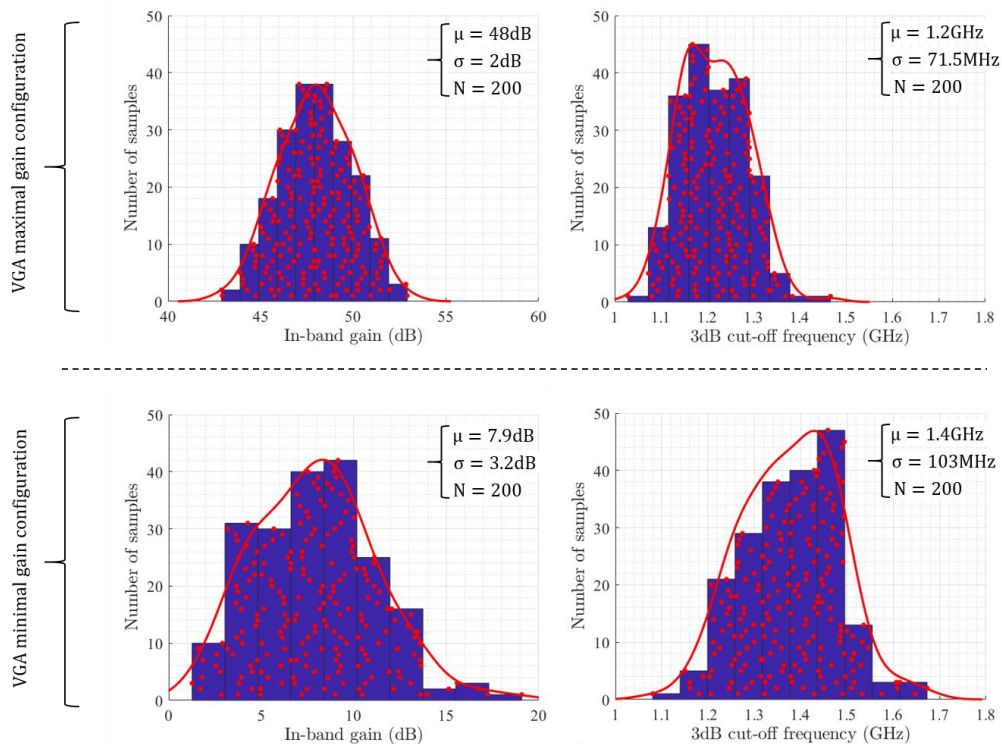
$$CMRR_{dB} = 20 \log \left( \frac{A_v^d}{A_v^{cm}} \right) \quad (38)$$

Consequently, in order to increase the rejection capability of the amplifier, the common mode amplification needs to be as low as possible while the differential gain needs to be high. The CMRR of the VGA was plotted Figure 133 and is greater than 31dB from DC to 21GHz.



**Figure 133: CMRR of the proposed four-staged RX VGA**

Finally, 200-points Monte Carlo process and mismatch simulations were performed, exhibiting a low impact of these variations over the performances of the VGA, considering the standards deviations, where the gain varies by 4% and the 3dB upper cut-off frequency by 5.9% only.



**Figure 134: 200-points Monte Carlo statistical simulations over the in-band-gain (left) and the 3dB cut-off frequency (right) of the proposed VGA, within the maximal and minimal gain configuration**

### 5.1.3.4 Conclusion

Finally, the post-layout performances of the designed RX VGA (Figure 128) were compared with the initial specifications in Table 27. This amplifier responds to all specifications and it appears to be an adequate choice for the design of the transceiver. Note that the last stage of the VGA is followed by a shunt resistor in order to lower the input impedance of the 50 $\Omega$  buffer, to ensure that each stage will provide the same gain.

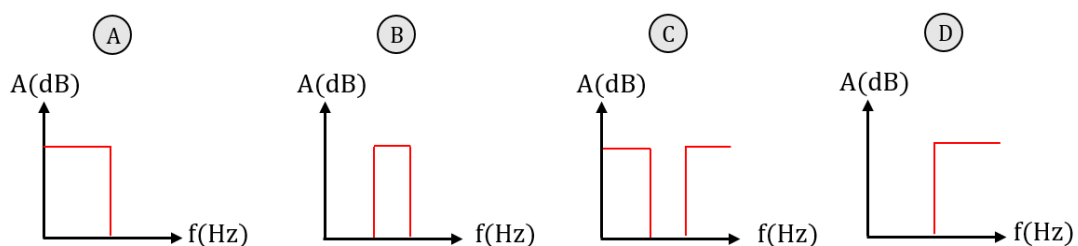
RX VGA		
	Specification	Post-layout simulations
Gain range (dB)	7 – 50	8 – 48.5
Step size (dB)	0.5	$\approx 0.5$
DCOC (dBc)	40	$> 43.4$
CMRR (dB)	30	$> 31$
-3dB BW (GHz)	$> 1$	1.2
NF (dB)	20	17.5

*Table 27: RX VGA post-layout performances compared with specifications*

## 5.2 FILTERING

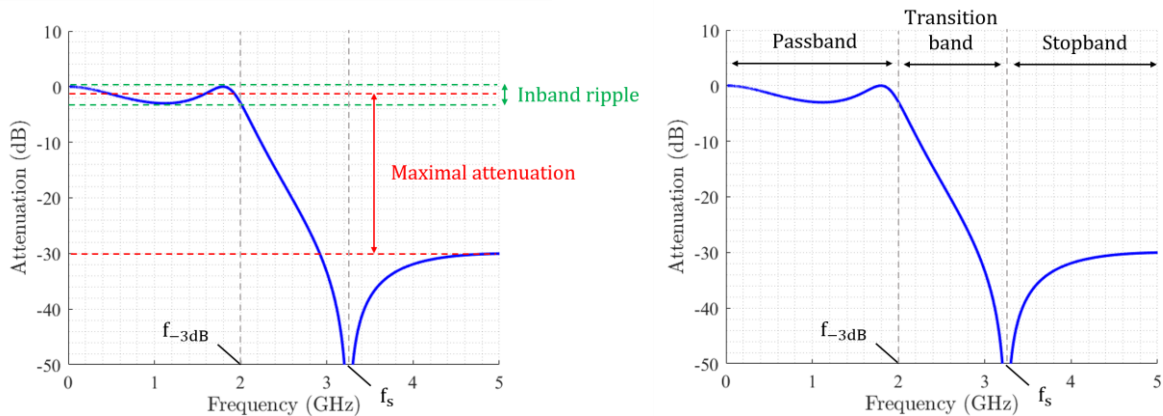
### 5.2.1 BASICS

Filters are crucial building blocks as they shape signals in order to remove unwanted harmonics. They are numerous kinds of filters, listed in Figure 135. High-pass filters can be used to remove the DC component that can be induced in direct-conversion receivers. Band-pass filters are useful to select a given frequency band removing harmonics below and above.



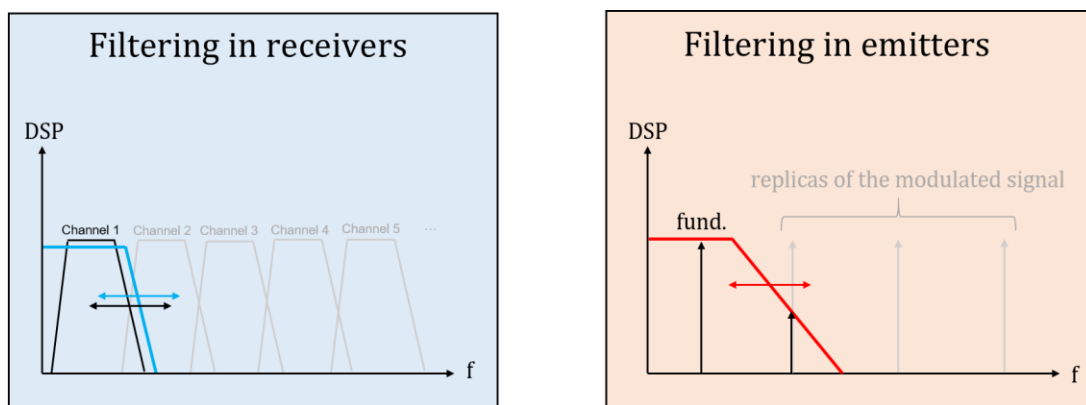
*Figure 135: Ideal frequency response of various filter types: low-pass (A), band-pass (B), band-reject (C) and high-pass (D)*

Band-reject filters do the opposite operation. Finally, low-pass filters are useful to keep the low frequencies and remove any possible RF leakage into a baseband signal. In this thesis a low-pass filter is to be designed. In Figure 136 (right) various regions of operation of the filter are depicted, and the main variables and parameters can be defined (left).



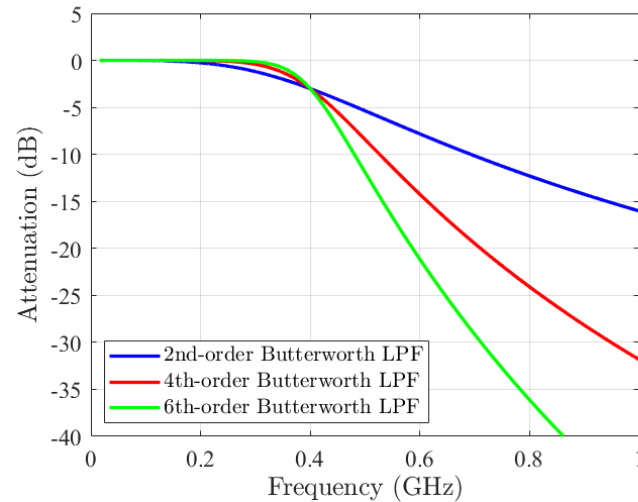
**Figure 136: Illustration of the low-pass filter main parameters over the example of the frequency response of a third-order elliptic low-pass filter**

In transceivers, the need for filtering is not similar when considering the emission path, and the reception path because the spectrums to be processed are different [77]. As illustrated in Figure 137, in receivers, filtering is about the selection of a given channel whose bandwidth can vary. High selectivity filters are required in order to reject neighbor channels, and/or limit the filtering of in-band data. In transmitter, it is about rejecting the replicas of modulated signal generated in the digital domain (DACs). A fourth order filter will hence be designed in the receiver design when a second order will be required in the transmitter design. These two filters attenuation profiles are mentioned in Figure 138 in the case of second to sixth order low-pass Butterworth ideal filters, whose 3dB cut-off frequency is set at 400MHz.



**Figure 137: Illustration of the different filtering needs within a transceiver**

Butterworth prototypes filters were preferred over Bessel and Tchebychev ones in our case to optimize passband gain flatness, at a reasonable roll-off in the transition band [78].



**Figure 138: Ideal frequency response second- fourth- and sixth- order Butterworth low-pass filters**

### 5.2.2 SECOND ORDER AND FOURTH ORDER ACTIVE-RC LOW-PASS FILTER DESIGN

There are two families of filters, they can either be active or passive. Passive filters are intrinsically bidirectional because passive lumped components have symmetrical properties. However, as they induce losses, active filters were preferred. Considering the high linearity requirements typical of 5G systems, and the relatively low cut-off frequencies to achieve, active-RC topologies were chosen over Gm-C filters [79]. However, both gm-C and active-RC filters will be sensitive to process variations [80], and even though a calibration circuitry would be mandatory for a proper use of the filter, it was not covered in the thesis. Finally, the specifications over the two filters are dressed in Table 28 and Table 29.

TX Filter	
	Specification
Order	2
Gain ripple (dB)	$\pm 1$
Insertion losses (dB)	$< 2$
Reconfigurability	4 BW

**Table 28: Specification table of the TX filter**

RX Filter	
	Specification
Order	4
Gain ripple (dB)	$\pm 1$
Insertion losses (dB)	$< 4$
Reconfigurability	4 BW
NF (dB)	15

Table 29: Specification table of the RX filter

The schematic of the proposed active-RC low-pass (or Rauch) filter is illustrated Figure 139.

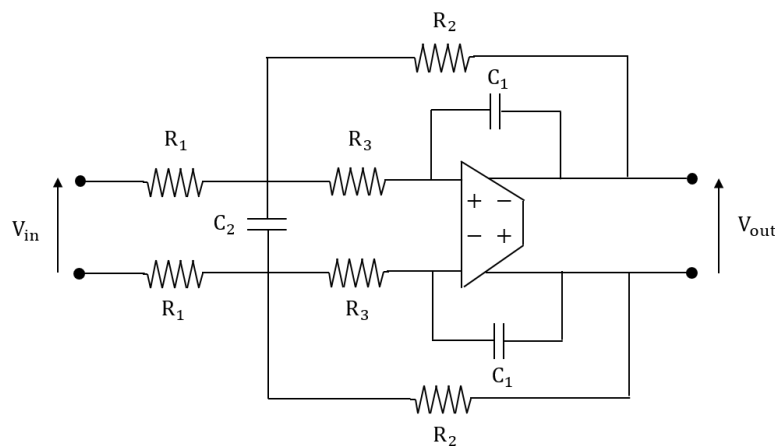


Figure 139: Schematic of the second order active-RC low-pass filter used in the TX and RX paths

In order to calculate the value of each lumped components (respectively R1, R2, R3, C1 and C2), a well-known design table was used as in Table 30, from our work published in [81].

Filter order	Stage 1		Stage 2		Stage 3	
	FSF	Q	FSF	Q	FSF	Q
2	1	0.707				
3	1	1	1			
4	1	0.541	1	1.307		
5	1	0.618	1	1.162	1	
6	1	0.518	1	0.707	1	1.932

Table 30: Design table of multi-stages Butterworth low-pass filters

Once the filter order is selected, it indicates the quality factor of each stage. The ideal transfer function one stage of a single-ended multiple-feedback (MFB) low-pass filter, is expressed as

$$H(s) = \frac{-R_2/R_1}{1 + C_1 \left( R_3 + R_2 + \frac{R_2 R_3}{R_1} \right) s + (C_1 C_2 R_2 R_3) s^2} \quad (39)$$

Where multiple variables can be identified such as the linear gain as

$$K = -R_2/R_1 \quad (40)$$

The frequency scaling factor, or *FSF* as

$$FSF = \frac{1}{2\pi f_c \sqrt{R_2 R_3 C_1 C_2}} \quad (41)$$

As well as the quality factor as

$$Q = \frac{\sqrt{R_2 R_3 C_1 C_2}}{R_3 C_1 + R_2 C_1 + R_3 C_1 (-K)} \quad (42)$$

In this work, several simplifications were made as follows

$$K = -1 \quad R_2 = R_3 \quad C_0 = C_1 = \frac{C_2}{n} = 100fF \quad (43)$$

Where  $n \in \mathbb{Z}$  and is determined using (42) and Table 30. Finally, these equations led to the expression of the required value for the resistors for  $R_1, R_2$  and  $R_3$  to select a given  $f_i$  as

$$\{R_{1,2,3}^{(i)}\}_{i \in \llbracket 1,4 \rrbracket} = \left\{ \frac{1}{6\pi f_i C_0 Q_F} \right\}_{i \in \llbracket 1,4 \rrbracket} \quad (44)$$

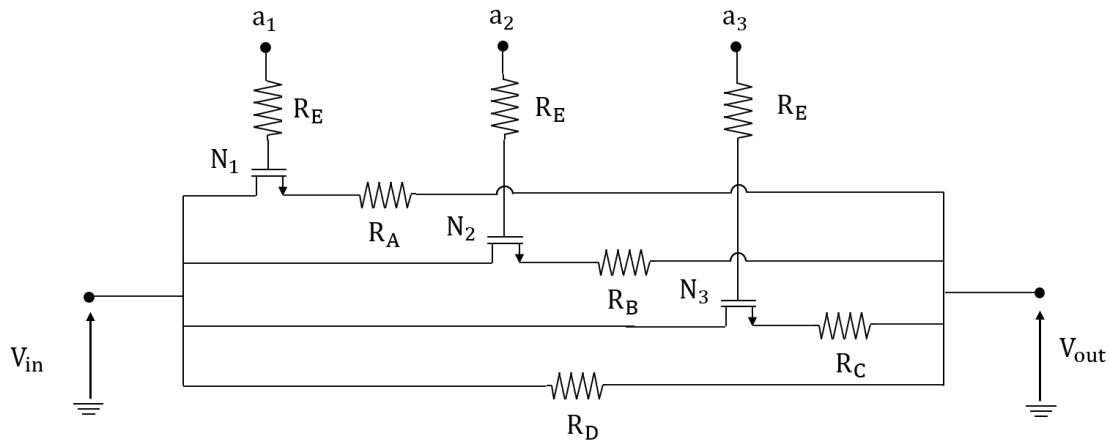


Figure 140: Schematic of the variable resistor used in the reconfigurable low-pass filters

Then the adequate value of the resistors is calculated to get an appropriate BW from 50MHz to 400MHz. In practice this variable resistor was implemented as in Figure 140 using a 3-bits digital command  $(a_1, a_2, a_3)$  using transistors (N1-3) whose width was set to  $2.4\mu\text{m}$  and length to 20nm. The resistor  $R_E$  has a value of  $12.5\text{k}\Omega$ . The effect of the binary command over the BW selection is described in Table 31.

$(a_1 a_2 a_3)_2$	$(111)_2$	$(110)_2$	$(100)_2$	$(000)_2$
BW	400MHz	200MHz	100MHz	50MHz

**Table 31: Effect of the binary command over the expected filters BW selection**

In the case of the TX filter, the digital command mentioned above should set the value of the resistors to the value listed in Table 32. In the case of the RX filter, those values are mentioned into Table 33, for the two stages.

TX filter					
$R_A$	$R_B$	$R_C$	$R_D$	$C_1$	$C_2$
600 $\Omega$	1200 $\Omega$	2400 $\Omega$	4800 $\Omega$	100fF	460fF

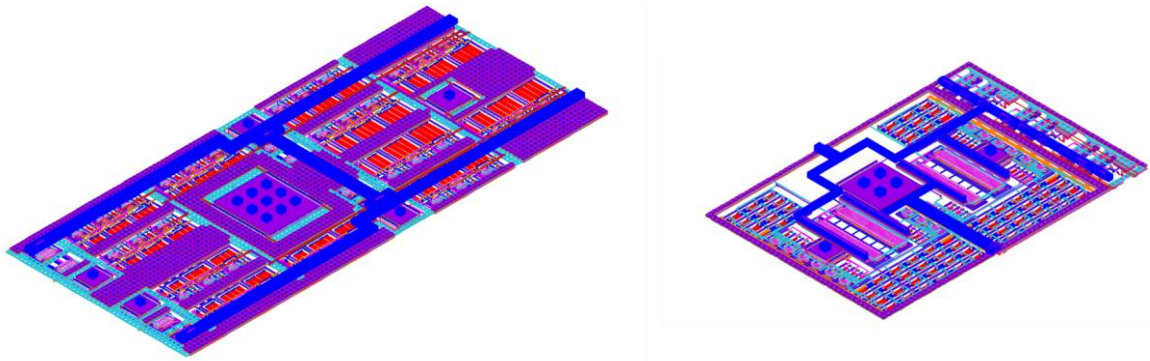
**Table 33: TX filter lumped components value summary**

RX filter					
$R_A$	$R_B$	$R_C$	$R_D$	$C_1$	$C_2$
First stage					
2500 $\Omega$	5550 $\Omega$	11650 $\Omega$	12200 $\Omega$	100fF	172fF
Second stage					
700 $\Omega$	1950 $\Omega$	4510 $\Omega$	5060 $\Omega$	100fF	995fF

**Table 32: RX filter lumped components value summary**

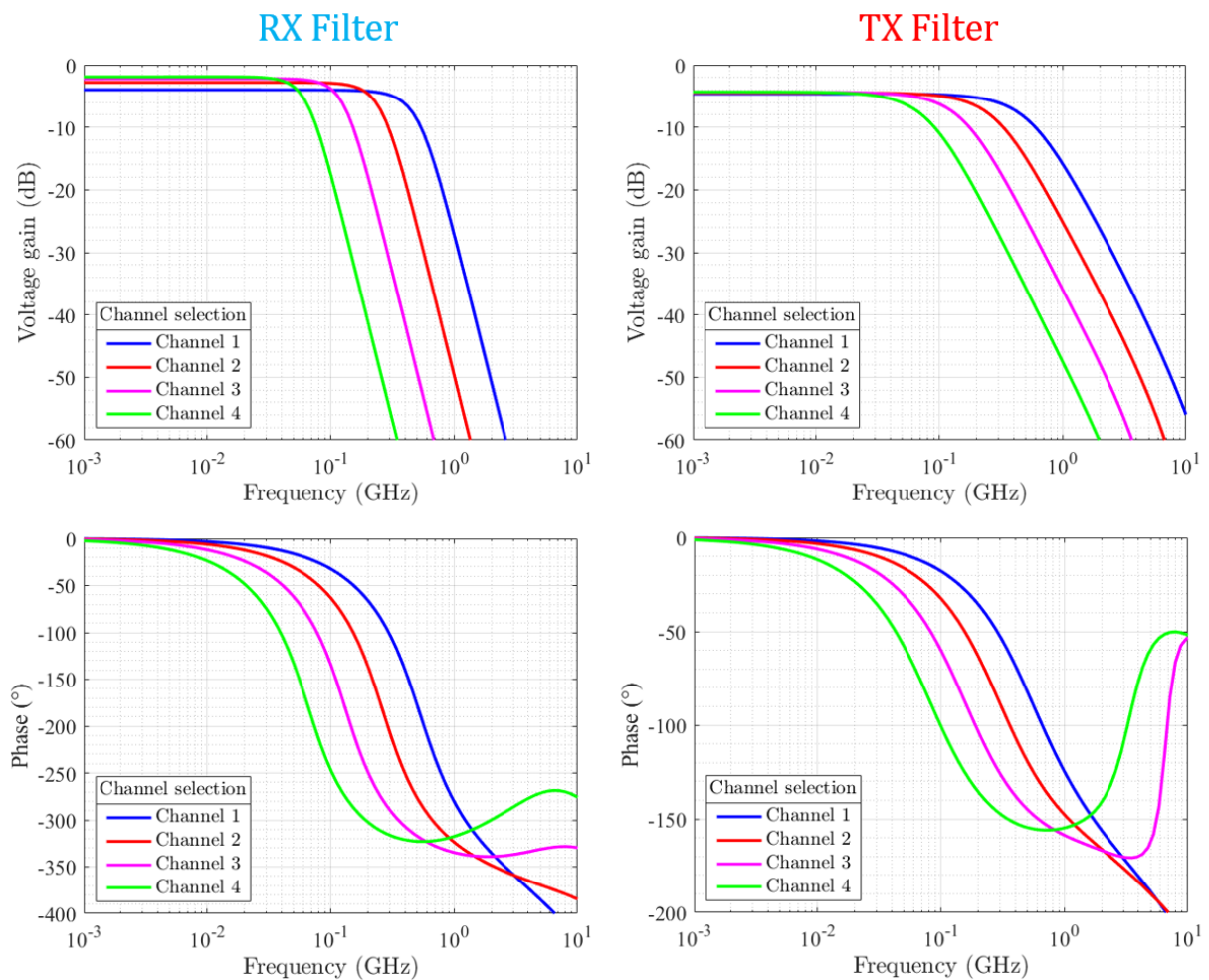
Finally, the layout of the two filters was realized as in Figure 141. In the TX filter design, the gate widths of NMOS and PMOS are respectively  $114\mu\text{m}$  and  $100\mu\text{m}$  and in the RX filter design they are respectively  $21.5\mu\text{m}$  and  $20\mu\text{m}$ , with equal gate lengths set to 40nm. The resistors  $R_A, R_B, R_C$  and  $R_D$  were implemented using PDK *reopnpr* (High-R N+ Polysilicon OP) and the capacitors using 2.5V *apmom* PDK capacitors. As to the resistors  $R_E$  used for the application of the digital command, *reopnarnpres* (Narrow High-R N+ Polysilicon OP) PDK resistors were used.



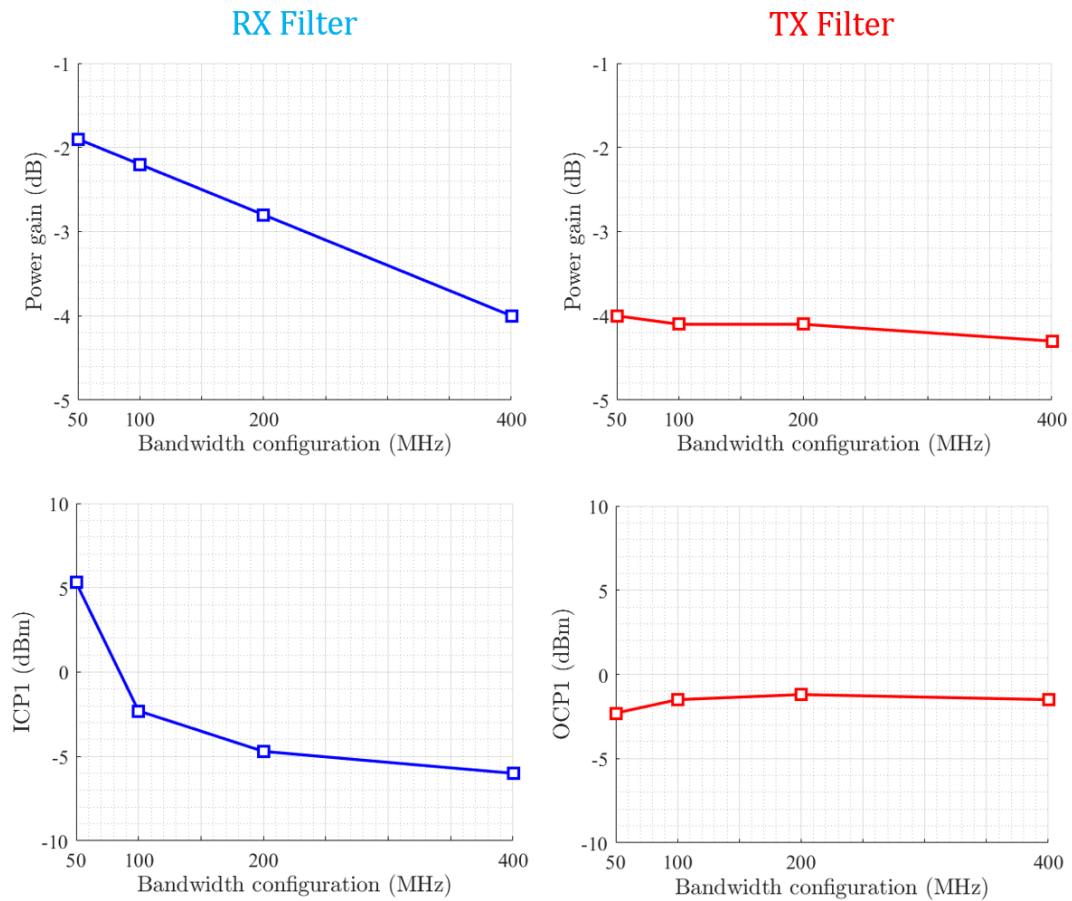


**Figure 141: 3D layout view of the proposed reconfigurable band unidirectional RX fourth order (left) and TX second order (left) active-RC low-pass filters**

The bode plots of the two designed filters were plotted in Figure 142. The RX filter in-band voltage gain varies from -4dB to -1.9dB from the broader to the narrowest BW configuration. Similarly, the TX exhibits an in-band gain ranging from -4.3dB to -4dB. The TX and RX filters respectively consume 11.9mW and 4.5mW.

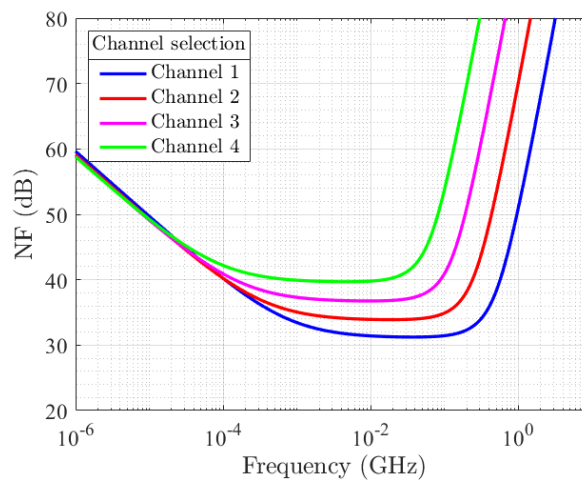


**Figure 142: Bode plots of the proposed RX and TX low-pass filters**



**Figure 143: Impact of resistors variation over the ICP1 and power gain of the RX (blue) and TX (red) filters**

As the feedback resistor value of the active-RC filters changes, both output power and noise are impacted, and these two impacts are respectively quantified in Figure 143 (using a single in-band input tone at 1MHz) and Figure 144 within the four BW configurations. The RX filter NF varies from 31.3dB to 39.8dB.



**Figure 144: Impact of the BW channel selection over NF of the RX filter**

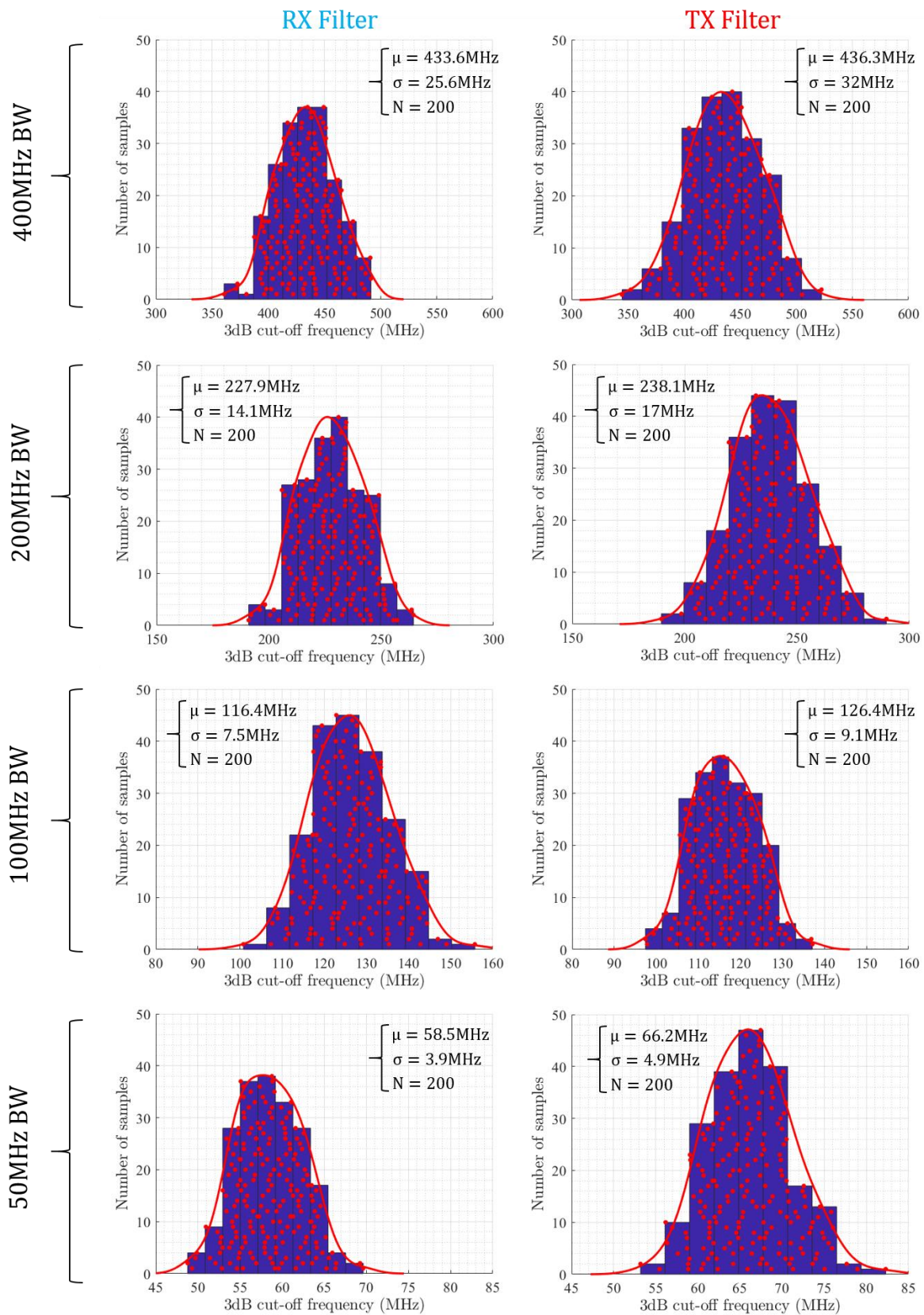


Figure 145: Process and mismatch Monte Carlo simulations over the RX (left) and TX (right) filter under their four BW configurations (from 400MHz (top) to 50MHz (bottom))

### 5.2.3 CONCLUSION

Finally, the performances of the two designed filters are compared with initial specifications in Table 34 and Table 35.

TX filter		
	Specification	Post-layout simulations
Order	2	2
Gain ripple (dB)	$\pm 1$	$\approx 0$
Insertion losses (dB)	$< 2$	$-4 < IL < -4.3$
Reconfigurability	4 BW	$f_{-3dB}$ : 65/126/238/437MHz

*Table 35: TX filter post-layout performances compared with specifications*

RX filter		
	Specification	Post-layout simulations
Order	4	4
Gain ripple (dB)	$\pm 1$	$\approx 0$
Insertion losses (dB)	$< 4$	$-4 < IL < -1.9$
Reconfigurability	4 BW	$f_{-3dB}$ : 59/118/231/440MHz
NF (dB)	15	$31.3 < NF < 39.8$

*Table 34: RX filter post-layout performances compared with specifications*

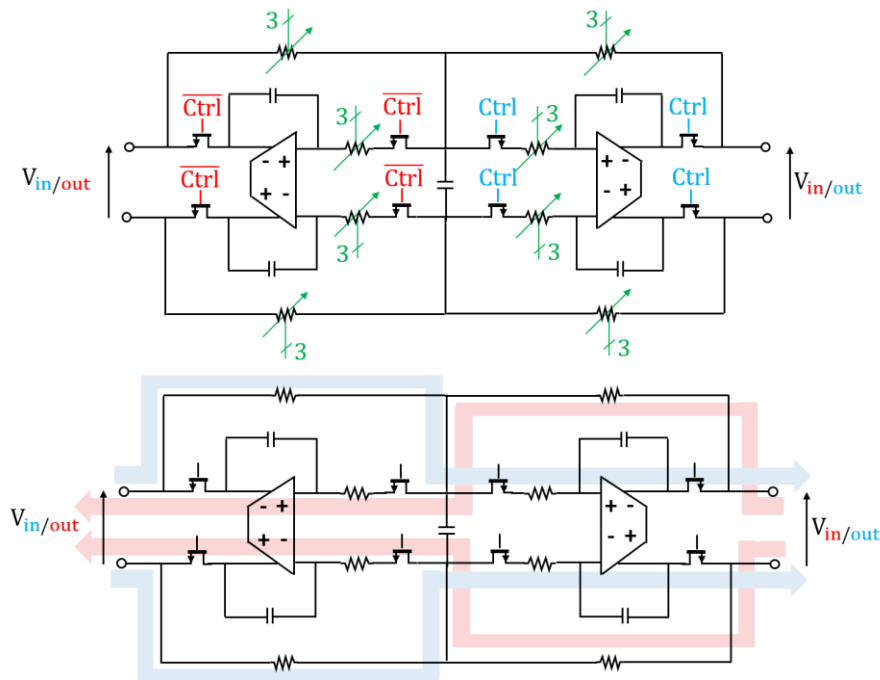
From these tables, the major issue is the subsequent noise figure due to the choice of small value for the Miller capacitor. In order to improve noise, larger capacitors should be considered for  $C_1$  and  $C_2$ , maintaining their ratio identical. However, it will lead to a larger silicon footprint. It also remarkable that due to resistor switching, the noise figure varies by 8.5dB between the selections of the larger to the smaller BW.

This noise figure will be critical in the global noise figure calculation that will be highlighted in the final section analyzing the behavior of the WILSON<sup>1</sup> transceiver chip.

<sup>1</sup> WILSON is the name given to the transceiver designed in this Ph.D. work

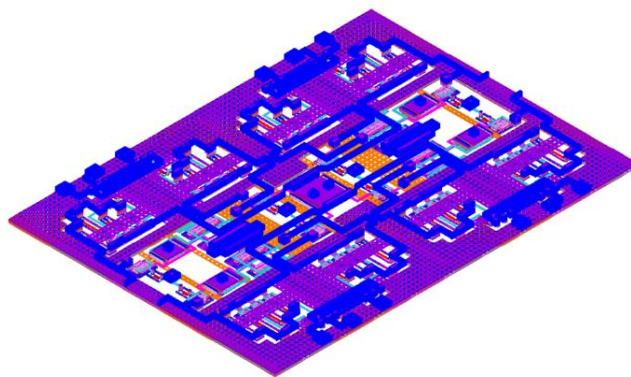
### 5.2.4 TOWARD A BIDIRECTIONAL FILTERING OPERATING MODE?

A novel architecture of bidirectional filter was proposed in our work published in [81]. This filter was not included in the final transceiver design. The principle of the operation of this filter is explained in Figure 146 exhibiting the two operating modes.



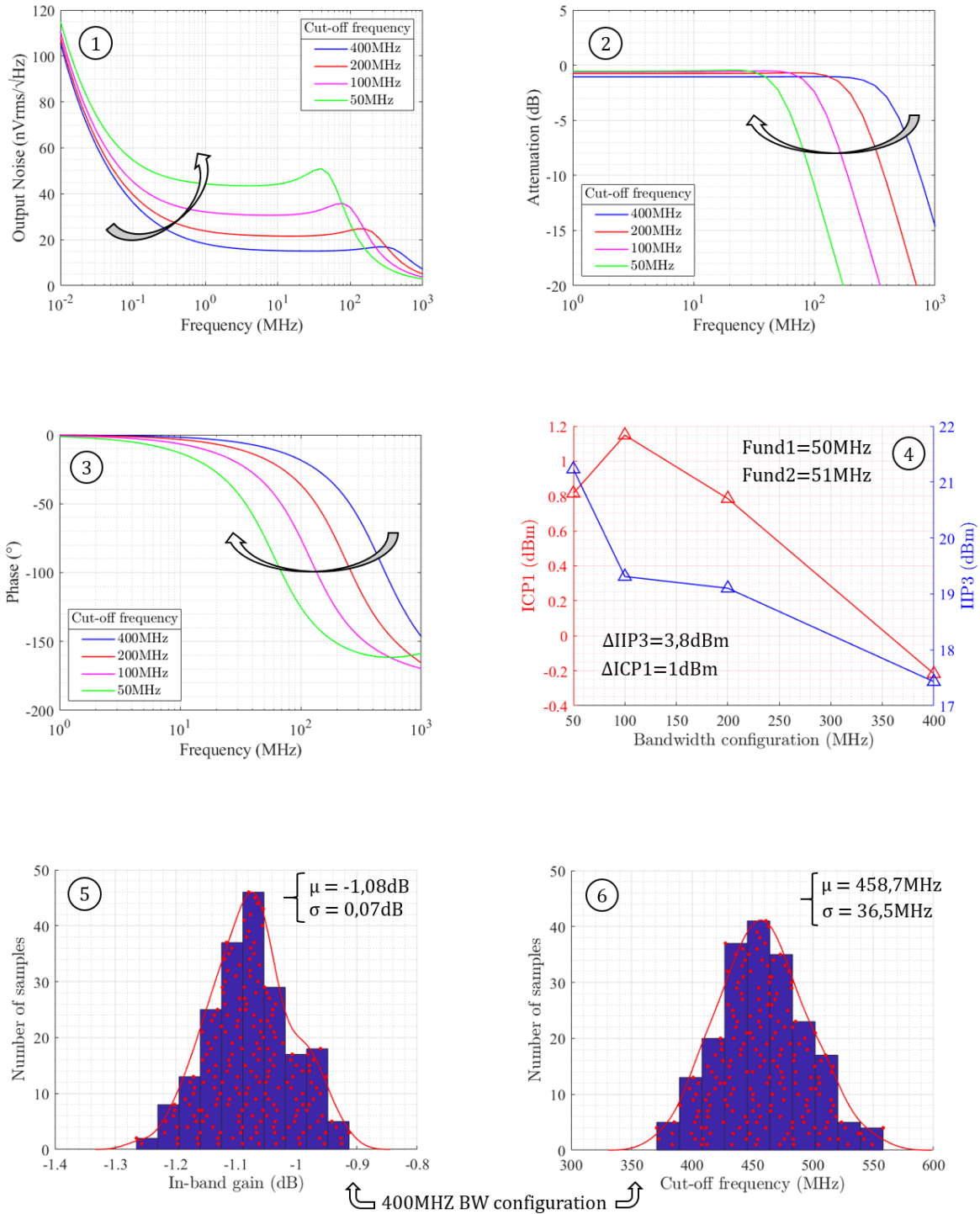
**Figure 146: Schematic of the proposed reconfigurable band bidirectional low-pass filter**

Both OTA are alternatively enabled using isolation transistors. The switched resistors are identical in the two modes. This architecture reuses most of the lumped components and roughly 71% of the layout presented in Figure 147 is used bilaterally. This filter uses the same PDK libraries of lumped components than the TX and RX filters previously presented.



**Figure 147: 3D layout view of the proposed reconfigurable band bidirectional low-pass filter**

Bode plots, large signal analysis as well as Monte Carlo post-layout simulations were performed in Figure 148 to summarize the performances of this bidirectional low-pass filter.



**Figure 148: Output-referred noise (1) in-band gain (2) phase (3) ICP1 and IIP3 (4) under the four BW configurations and Monte Carlo analysis over the in-band gain (5) and cut-off frequency (6) of the proposed bidirectional filter at 400MHz BW**

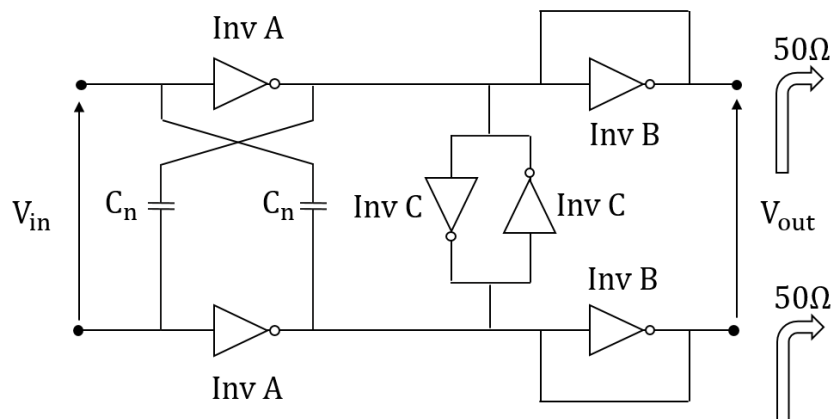
### 5.3 50Ω RX BUFFER

In order to load the VGA with a high impedance and drive a 50Ω input impedance of one single-ended ADC, a specific building block was designed whose specifications are listed in Table 36. This buffer is mandatory to avoid a gain drop for the last stage of the VGA which expect a high impedance at its output.

RX 50Ω buffer	
	Specification
Power gain (dB)	$0 \geq$
$S_{22}$ (dB)	-15
-3dB BW (GHz)	$> 1$
NF (dB)	15

**Table 36: Specification table of the 50Ω RX buffer**

Its schematic is described in Figure 149. It is composed of two neutralized inverters (INVA), followed by two inverters whose transistors are diode-connected (INVB). These transistors were sized to present 50Ω at the output while INVA transistors to provide enough voltage gain to meet the specifications. Finally, two inverters INVC were implemented to force the differential mode of the pseudo-differential circuit. The respective sizes of the transistors used for INVA, INVB and INVC were hence reported in the Table 37. The value of the neutralization capacitors  $C_n$  was fixed to 57 fF to enhance both stability and gain. In this design, *lvtnfet* and *pfet* transistors were used, the length L of the PMOS is fixed to 32nm while the length of NMOS

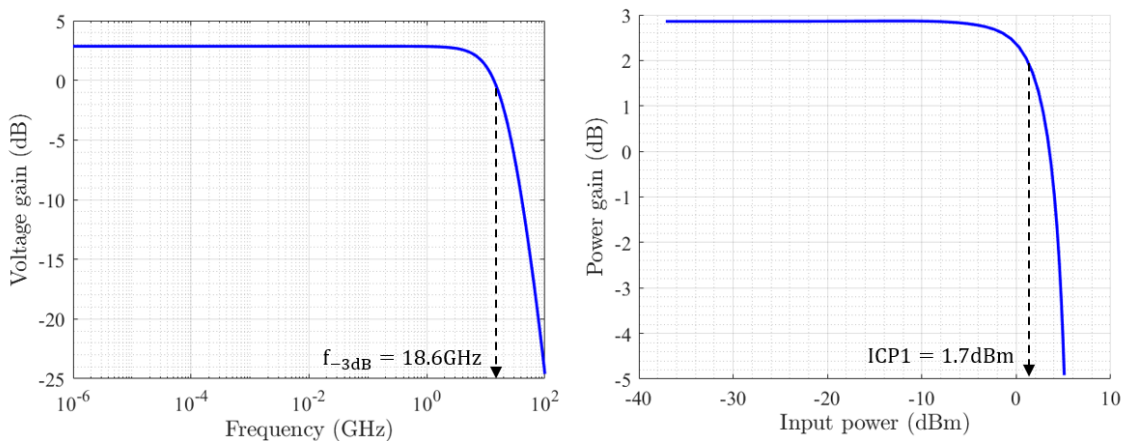


**Figure 149: Schematic of the proposed 50Ω RX buffer**

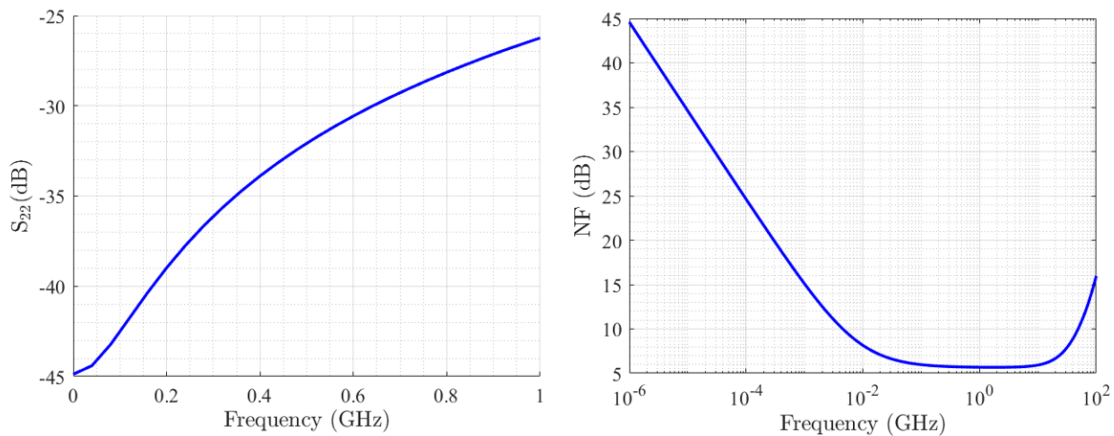
Transistor widths W (in $\mu\text{m}$ )					
INV A		INV B		INV C	
N	P	N	P	N	P
66	136	19.2	45	1	4.5

**Table 37: Transistors sizing summary of the proposed 50Ω RX buffer**

is set to 20nm. Figure 150 shows a good output matching when presenting a 50Ω load resistor at the output. The  $NF$  of the 50Ω RX buffer reaches a minimal in-band value of 5.7dB. A post-layout AC and PSS analysis were performed to characterize its power-handling as well as its cut-off frequency. The 3-dB cut-off frequency is 18.6GHz, the ICP1 is 1.7dBm and it exhibits a power gain of 2.86dB when excited with a 10MHz input single-tone. This RX 50Ω buffer consumes a DC power of 4.1mW.



**Figure 151: AC voltage gain (left) and PSS power gain compression (right) of the 50Ω RX buffer**



**Figure 150: 50Ω RX buffer  $S_{22}$  (left) and NF (right)**



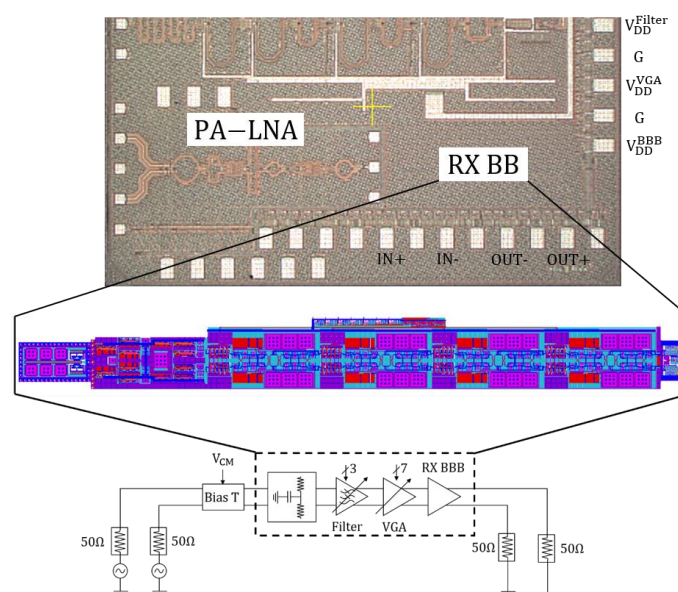
RX 50Ω buffer		
	Specification	Post-layout simulations
Power gain (dB)	$0 \geq$	2.86
$S_{22}$ (dB)	-15	$< -15$
-3dB BW (GHz)	$> 1$	18.6
NF (dB)	15	5.7

**Table 38: 50Ω RX buffer post-layout performances compared with specifications**

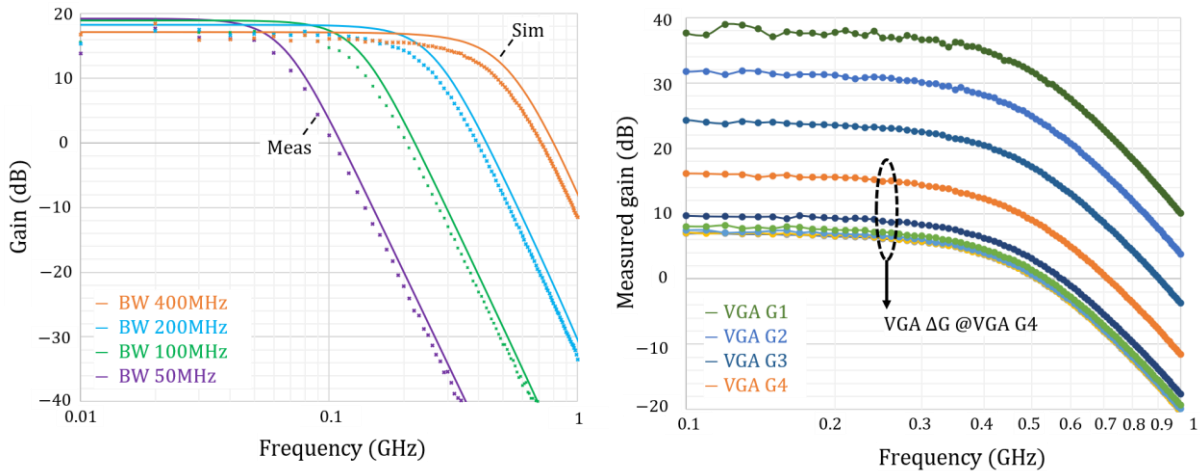
Post-layout simulations were hence compared with the specifications in Table 38, and this building block appears to be adapted to meet the requirements.

#### 5.4 MEASUREMENTS RUN2: TESTCHIP22 (RX ANALOG BASEBAND BLOCKS)

The TESTCHIP22 chip included a second version of the PA-LNA, as well as the RX analog baseband chain of the transceiver. The block diagram and the corresponding subsystem is described in Figure 152. It includes a reconfigurable fourth-order low-pass filter, a 7-bits controlled VGA, a 50Ω baseband buffer and a pseudo-differential 100Ω input shunt resistor reference, associated with a 3pF capacitor. The communication between the SPI and this IC is fully described in Chapter 6, and the binary commands are identical to the one used to control the transceiver. These 28-bits commands are listed and described in Appendix B. Figure 153 highlights the reconfigurability of the IC in given filter BW and VGA gain configurations.

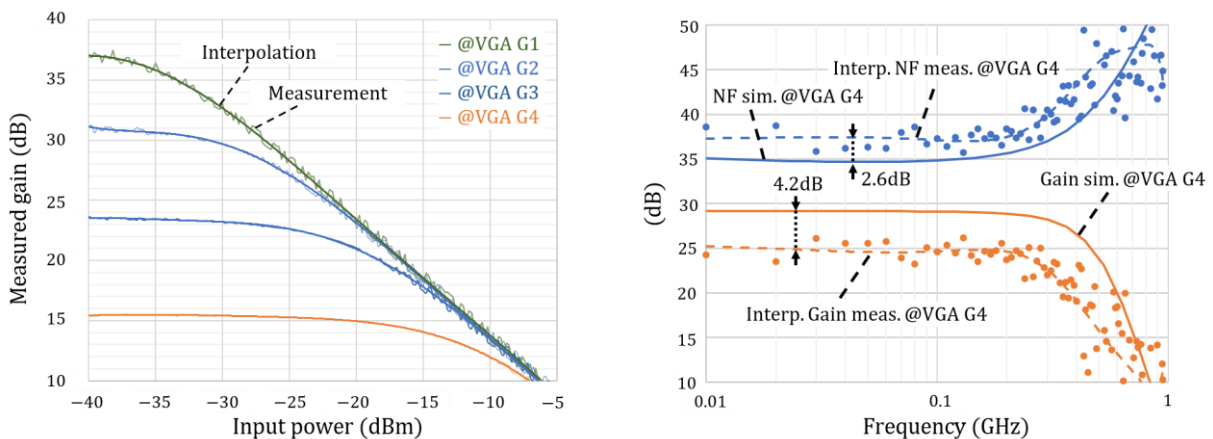


**Figure 152: Schematic, layout and chip view of the RX building blocks within the TESTCHIP22 chip**

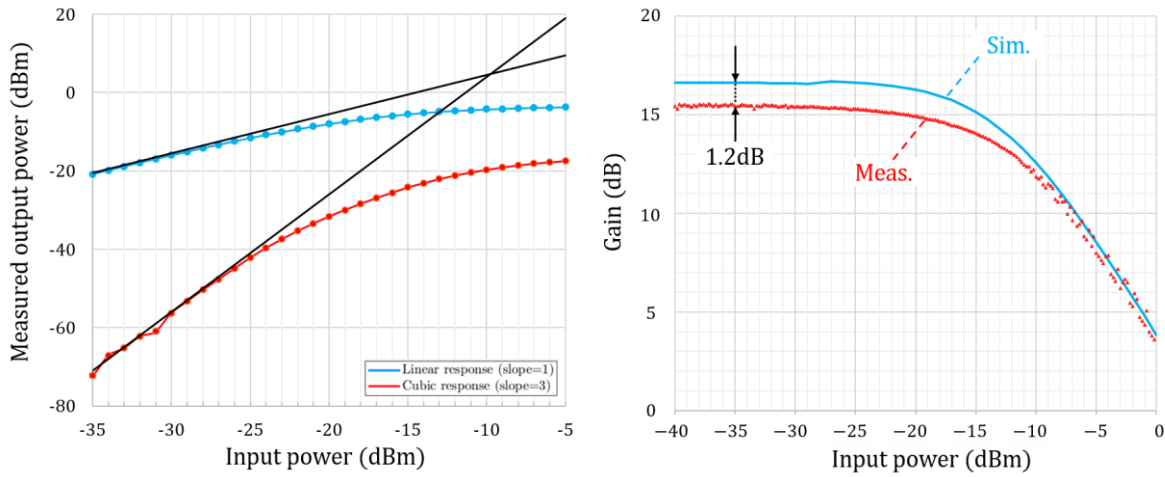


**Figure 153: TESTCHIP22 (BB RX) measured and simulated gain (dashed and solid) in the four BW configurations in the VGA G4 configuration (left) and measured gain variation of the main states of the VGA at maximal BW (right)**

The highest measured and simulated cut-off frequencies are compared and are 370MHz and 430MHz respectively. As expected, this cut-off frequency varied due to process variation, by 14%. The other cut-offs frequencies deviations can be extrapolated with this observation. The VGA main gain configurations measurements are illustrated, successively reducing the gain from the maximum to the minimum of the three last stages. Then, the gain of the first stage is reduced by 6.4dB, 1.6dB, 0.6dB, 0.3dB and 0.1dB from its maximum at 100MHz, activating only one bit from the LSB to the MSB. The input power is swept in Figure 154, in the main four configurations previously mentioned. The measured ICP1 are only observable for the two bottom curves and are equal to -24.8dBm and -17.2dBm (in the VGA G3 and VGA G4 gain configurations respectively). The single-ended  $NF$  is measured and compared with simulations in the VGA G2 configuration.



**Figure 154: TESTCHIP22 (BB RX) input power sweep in four gain states of the VGA (left) and measured single-ended gain and NF compared with simulation, in the VGA G2 gain configuration (right)**



**Figure 155: TESTCHIP22 (BB RX) measured IIP3 (left) and measured gain compared with simulation, in the VGA G4 configuration (right)**

A gain drop of 4.2dB is noticed using the interpolated measured gain, resulting in the increase of the interpolated measured  $NF$ . The measurement extrapolations are done using a sixth-order polynomial function. In this setup, the noise source noise is a Noisecom NC346D source, and the VNA is a ROHDE&SHWARZ FSW67 analyzer. When the DC currents of the various blocks are matched with the simulations, Figure 155 is plotted exhibiting a gain variation of 1.2dB, due to typical fabrication imperfections, and/or due to the resistivity of probes contacts. The simulated and measured ICP1 are respectively -15.8dBm and -17.2dBm in the VGA G4 gain configuration. The IIP3 is evaluated using two input tones at 50MHz and 51MHz (1MHz offset) in the VGA G4 gain configuration, and is equal to -9dBm. In this design, the DPDT switch was not yet incorporated, and is discussed in the next section.

### 5.5 TX/RX BB SWITCHING

In this work, DPDT switches were implemented in order to alternatively address the TX and RX BB paths. The specifications of this block were presented in Table 39.

TRX DPDT	
	Specification
Insertion losses (dB)	2
OCP1 (dBm)	0
NF (dB)	2

**Table 39: Specification table of the TRX DPDT switch**

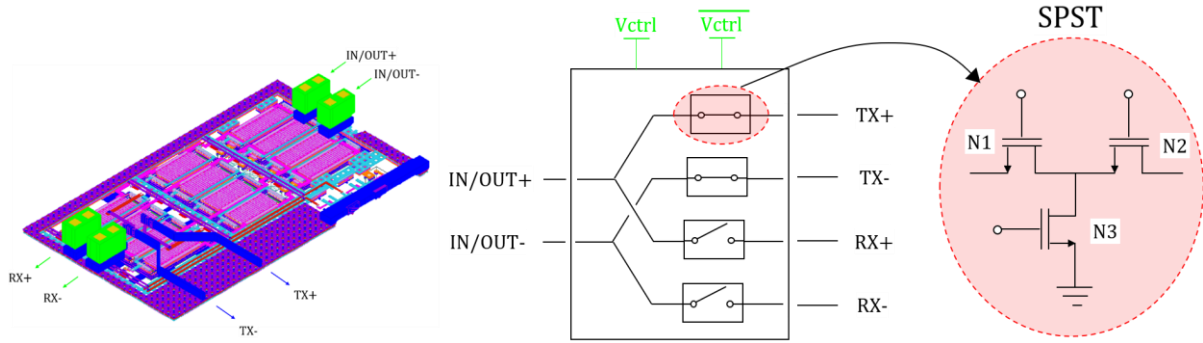


Figure 157: Schematic and 3D layout view of the TRX DPDT switch

A SPST switch is basically a switched transistor where the drain plays the role of the input and the source of the output (and vice-versa in our case). The goal is to limit the ON-state resistor of this transistor described in [82] as

$$R_{ON} = \frac{1}{\mu C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_T)} \quad (45)$$

As we can see the insertion losses are inversely proportional to the width of the transistor and is reduced for minimum gate lengths. However, as the value of intrinsic capacitances increases with the width, the resulting impedance decreases, resulting in the lowering of the  $C_{OFF}$ . A trade-off is hence to find between the  $R_{ON}$  and  $C_{OFF}$  through the choice of the transistor width. In this work, two switched transistors (N1 and N2) were implemented as in Figure 157 to enhance port-to-port isolation. The transistor N3 is used to fix the intermediate voltage potential to a known reference ( $V_{SS}$ ). Post-layout simulations were conducted in Figure 156 exhibiting insertion losses of 1.9dB and an in-band noise figure of also 1.9dB. It exhibits an adequate power-handling with an OCP1 of -0.2dBm.  $R_{ON}$  and  $C_{OFF}$  are respectively 26.1Ω and

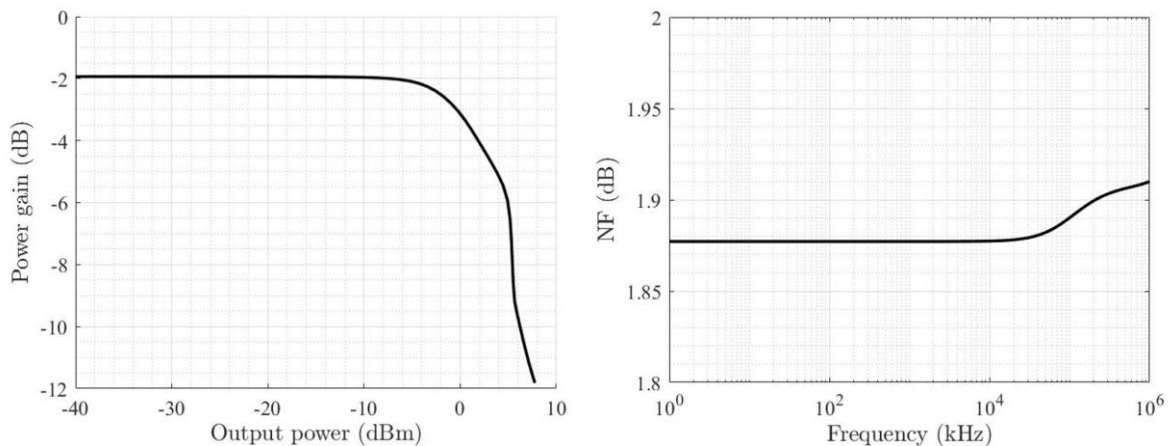
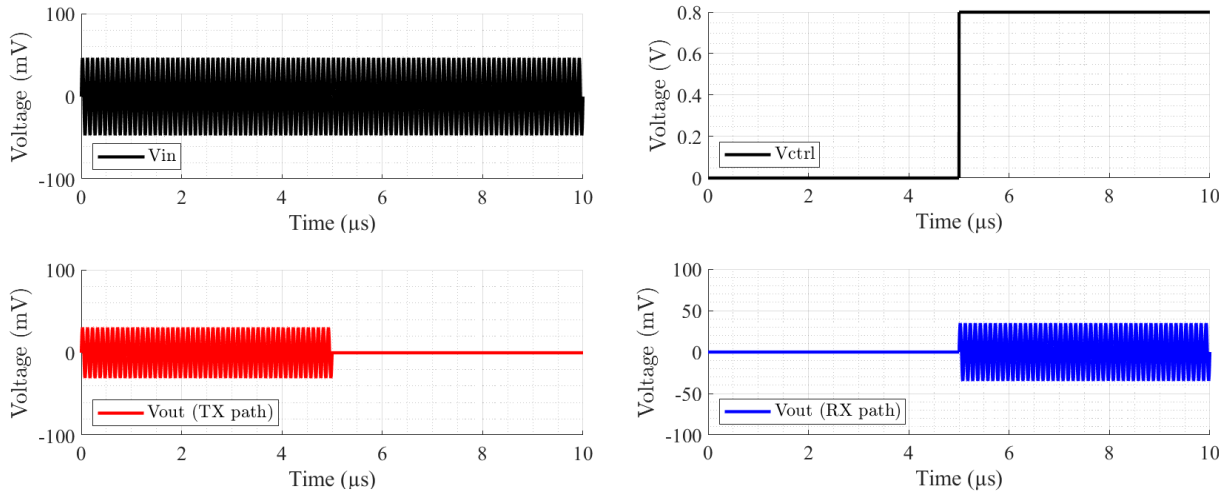


Figure 156: Power gain with respect to the output power (left) and noise figure (right) of the TRX DPDT switch



**Figure 158: Transient response of the TRX DPDT switch over the TX and RX path when varying the command voltage  $V_{CTRL}$**

86.5fF. Finally, a transient analysis was conducted Figure 158 where the input voltage is plotted in black and the TX and RX output signals are represented in red and blue respectively. The control command  $V_{CTRL}$  is commuted from 0 to  $V_{DD}$  at  $5\mu\text{s}$ . The post-layout simulations and initial specifications were hence compared Table 40, and as we see the selected DPDT meets the requirements.

TRX DPDT		
	Specification	Post-layout simulations
Insertion losses (dB)	2	1.9
OCP1 (dBm)	0	0.2
NF (dB)	2	1.9

**Table 40: TRX DPDT switch post-layout performances compared with specifications**

## 5.6 CONCLUSION

Finally, an operational baseband TRX chain was designed. In future works, the  $NF$  of certain building blocks could to be optimized, respectively for the RX filter and for the RX VGA in order to mitigate their impact over the overall  $NF$  leading to a subsequent EVM deterioration. The design of a TX VGA will also be required to furnish sufficient gain over the chain, and/or provide more flexibility as well as a better control over the RMS power presented at the input of the PA, without using the DACs at their maximal output power.



# Chapter 6: 5G FR2-1 INTEGRATED BIDIRECTIONAL TRANSCEIVER

**N**ow that all the building blocks were designed, they were assembled to build our bidirectional transceiver, which was sent to fabrication.

This section will highlight the transceiver performances through post-layout simulations – only – of both emitter and receiver including the I/O ring as well as digital functions. Measurements are not mentioned in this manuscript, since they could not have been done in the remaining time. The serial peripheral interface (SPI) was used in order to control the state of the reconfigurable building blocks (such as the filters and the VGA), and so described. A non-exhaustive list of commands was used in simulations in order to verify the main states of the chip.

Finally, some remarks were made about the strengths and weaknesses of this chip design, basically summarizing what was stated in the previous sections. Hence, this transceiver was compared with 5G transceivers found in the literature regarding both performances and silicon footprint.

## 6.1 LAYOUT AND RESULTS

### 6.1.1 RUN3: WILSON

The WILSON chip was fabricated in 22nm CMOS FD-SOI whose die microphotograph is presented in Figure 159. The chip area is 1.6mm<sup>2</sup> including DC and RF pads.

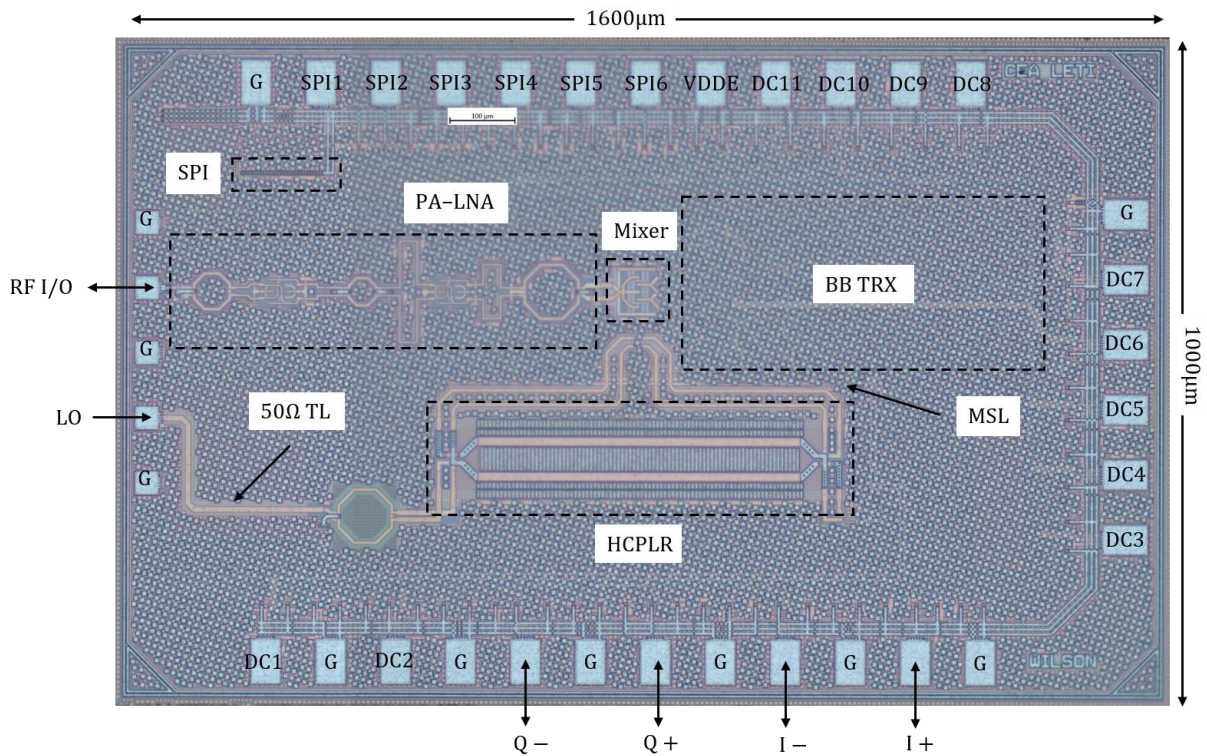


Figure 159: WILSON die microphotograph

The DC voltages required to be applied on the various DC pads of the chip in order to obtain a TX or a RX operation mode are reported in Table 41. The RF I/O pads are used as input in RX mode and as an output in TX mode. The baseband I/Q I/O are located at the south of the chip.

	DC1	DC2	DC3	DC4	DC5	DC6	DC7	DC8	DC9	DC10	DC11	VDDE
TX	$V_{G,1}^{PA}$	$V_{G,2}^{PA}$	$V_{DD}^{DPDT}$	$V_{CM}^{LO}$	$V_{DD}^{BBRX}$	$V_{DD}^{BBTX}$	$V_{CM}^{BB}$	$V_{DD,1}^{LNA}$	$V_{DD,2}^{LNA}$	$V_{D,1}^{PA}$	$V_{D,2}^{PA}$	1.8
	0.23	0.3	0.8	0.4	0	0.8	0.4	0	0	0.8	0.8	1.8
RX	$V_{D,1}^{LNA}$	$V_{D,2}^{LNA}$	$V_{DD}^{DPDT}$	$V_{CM}^{LO}$	$V_{DD}^{BBRX}$	$V_{DD}^{BBTX}$	$V_{CM}^{BB}$	$V_{DD,1}^{LNA}$	$V_{DD,2}^{LNA}$	$V_{G,1}^{LNA}$	$V_{G,2}^{LNA}$	1.8
	0	0	0.8	0.4	0.8	0	0.4	0.8	0.8	0.45	0.45	1.8

Table 41: Required DC voltages purpose and value to obtain the RX and TX modes



The area occupied by each building block is reported in Table 42.

	PA-LNA	Mixer	HCPLR	TRX BBBA	RX filter	TX filter	RX VGA	RX buffer	TRX DPDT
S(mm <sup>2</sup> )	0.114	0.005	0.078	0.006	0.005	0.002	0.030	0.001	0.001

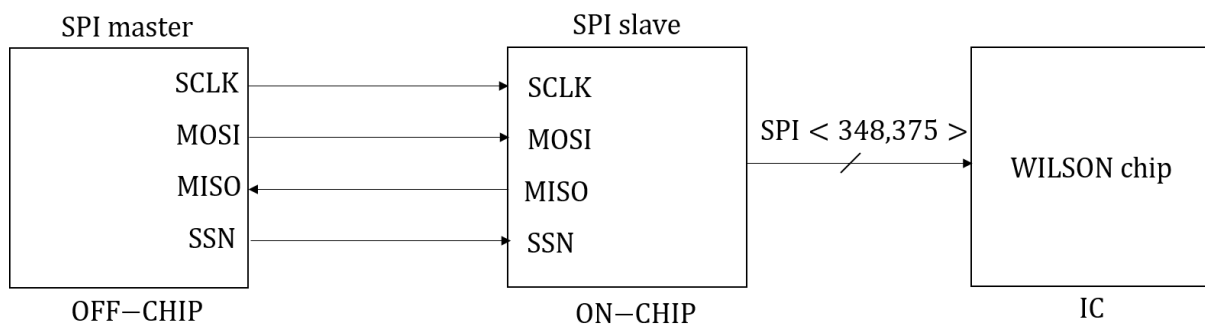
**Table 42: WILSON block-by-block silicon footprint**

A SPI was integrated within the chip in order to command various building blocks. The name of each pin is reported in Table 43 with a correspondence with the chip layout. The slave SPI pins are respectively Master Input Slave Output (MISO), Master Output Slave Input (MOSI), Serial Clock (SCLK), Slave Select (SSN) and Slave Reset (SSN). The communication between the master SPI (off-chip), and the slave SPI is described as in Figure 160.

SPI1	SPI2	SPI3	SPI4	SPI5	SPI6
VDD SPI	SPI MISO	SPI MOSI	SPI SSN	SPI SCLK	SPI RSTN

**Table 43: Correspondence between the WILSON DC pins names and the slave SPI pin names**

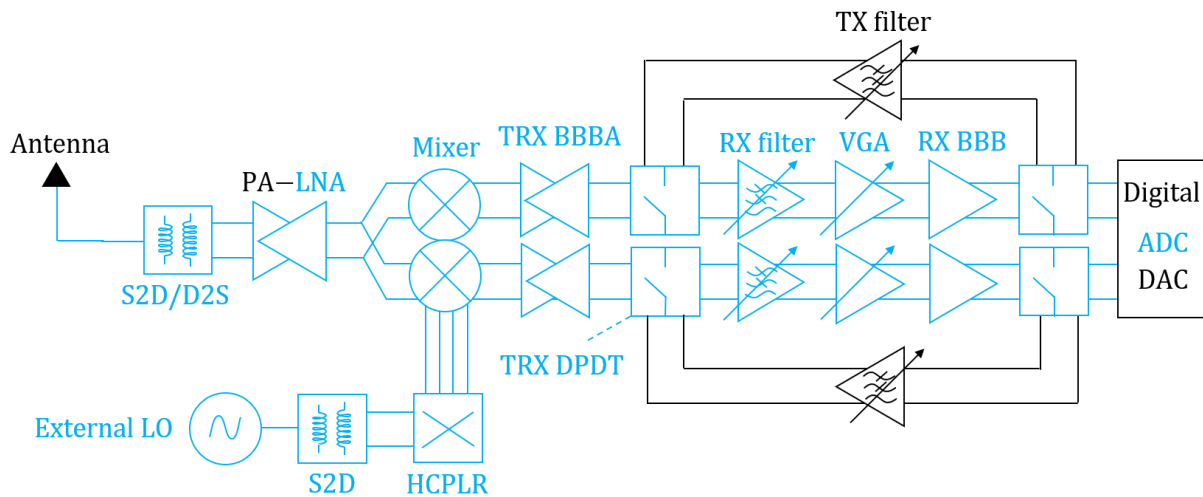
As the chip was delivered at the end of the thesis, it was not yet characterized. A non-exhaustive list of post-layout simulations were conducted instead in this chapter. The chip register map can be found in Appendix B at page 181. It describes the various combinations of the 24-bits binary command, associated with the main states of the chip. This table will set the binary words to be sent by the SPI for varying the gain of the RX VGA, for varying the BW of the RX and TX filters in their four BW configurations, setting the right BB paths using the DPDT, and enabling the PA or the LNA. The default setting is also mentioned.



**Figure 160: Communication between both the master and slave SPI and between the slave SPI and the fabricated IC**

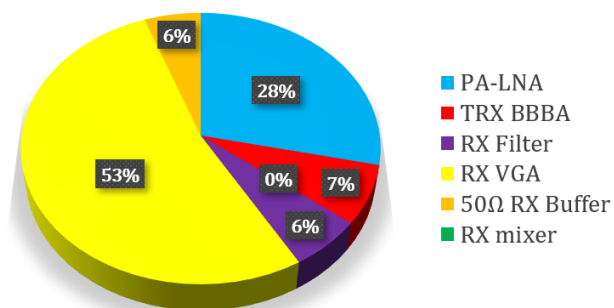
### 6.1.2 SIMULATION RESULTS IN RX MODE

In this section, post-layout simulations of the chip in receive mode were made, including the I/O ring and the SPI. The simulated core building blocks are highlighted in blue in Figure 161.



**Figure 161: Simulated WILSON RX chain**

The DC power budget of each building blocks is mentioned in Figure 162 with a global static consumption of 73.8mW. The main contributor is the RX VGA due to its subsequent maximal gain over more than 1GHz BW. In this work, no calibration circuitries are implemented but they would be required especially for the RX and TX filters BW setting, for a better accuracy.



**Figure 162: WILSON RX chain DC power budget**

The RF input, IF output and LO input spectrums are presented in Figure 163 and Figure 164, within the maximal and minimal RX VGA gain configurations. The DC levels are -45.1dBm and -54.1dBm through the path I and Q. These values differ due to the presence of mismatch.

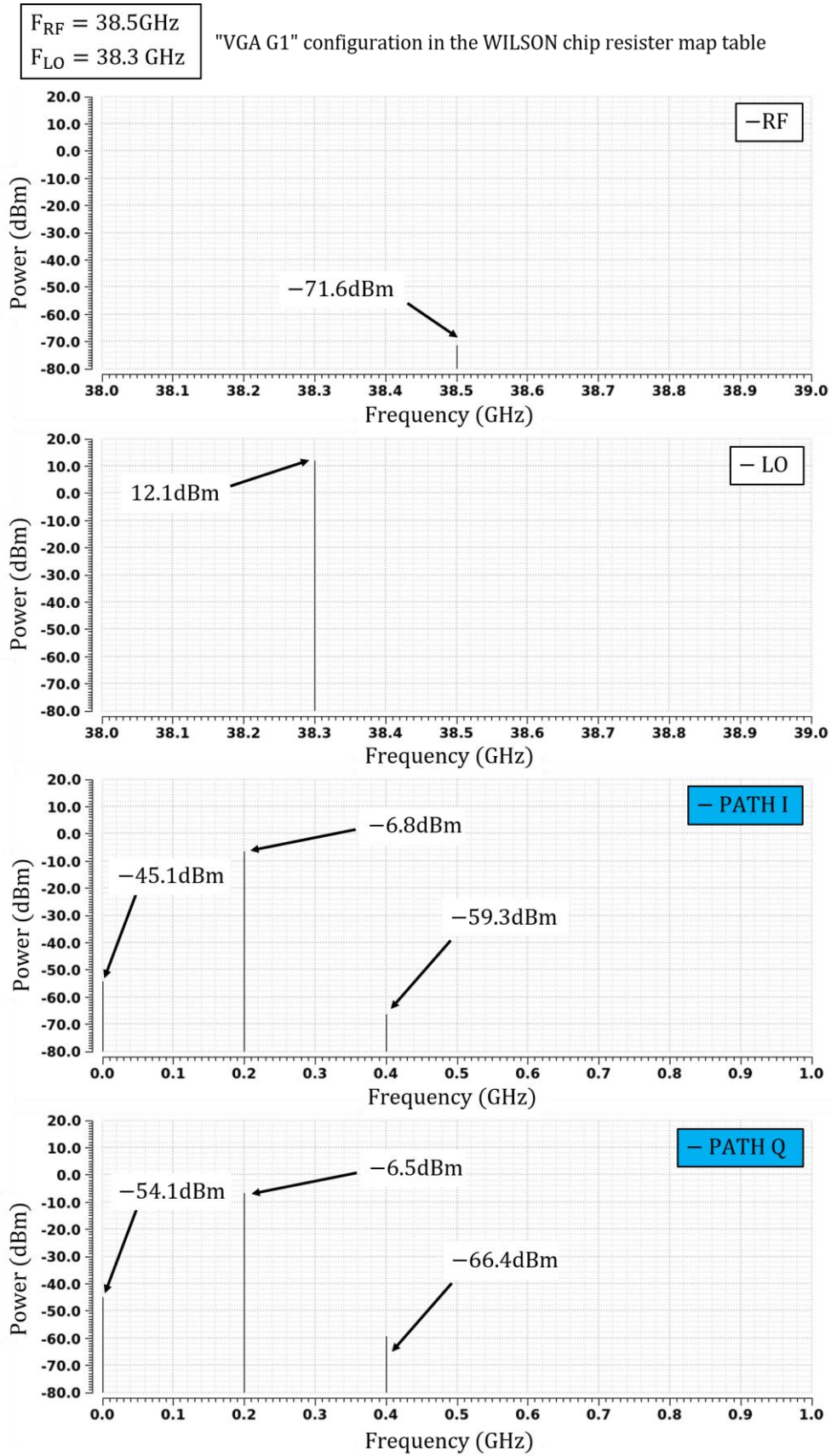


Figure 163: WILSON RX mode spectral characterisation at minimal input power

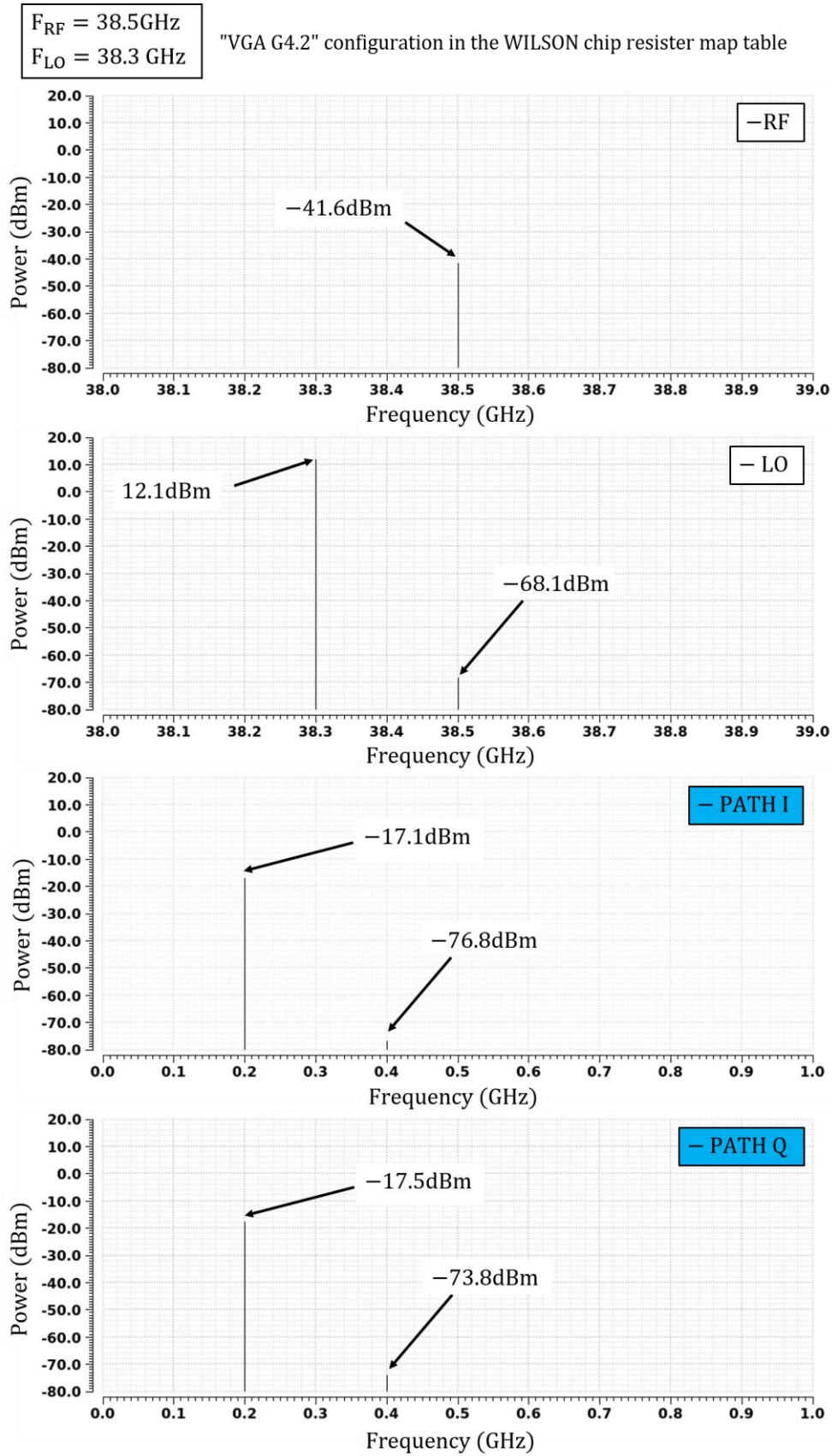
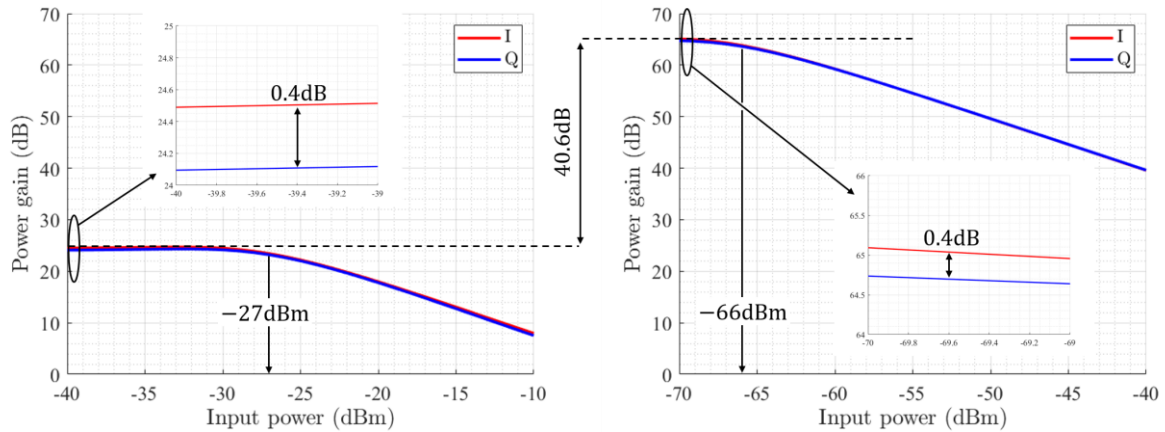


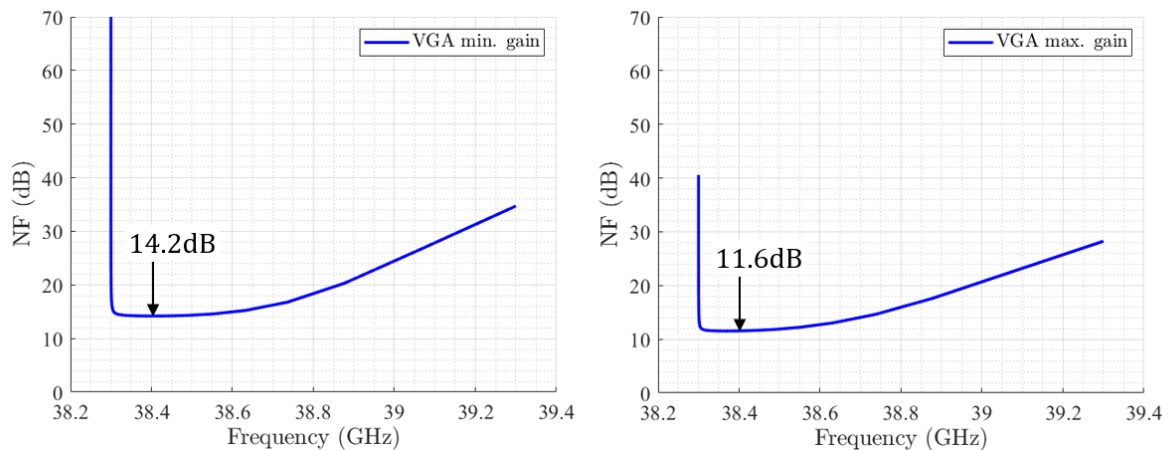
Figure 164: WILSON RX mode spectral characterisation at maximal input power

Finally, the power-handling of the chip was evaluated in the highest and lowest VGA gain configuration as in Figure 165. It highlights an ICP1 ranging from -66dBm with a power gain of roughly 65dB when the input power level is close to the receiver's sensitivity, and -27dBm with a power gain of roughly 24.3dB when this input power level reaches its maximum. The LO and RF tones are respectively set to 38.3GHz and 38.5GHz.



**Figure 165: WILSON RX chain power gain with respect to the input power in the VGA lowest (left) and highest (right) gain configuration**

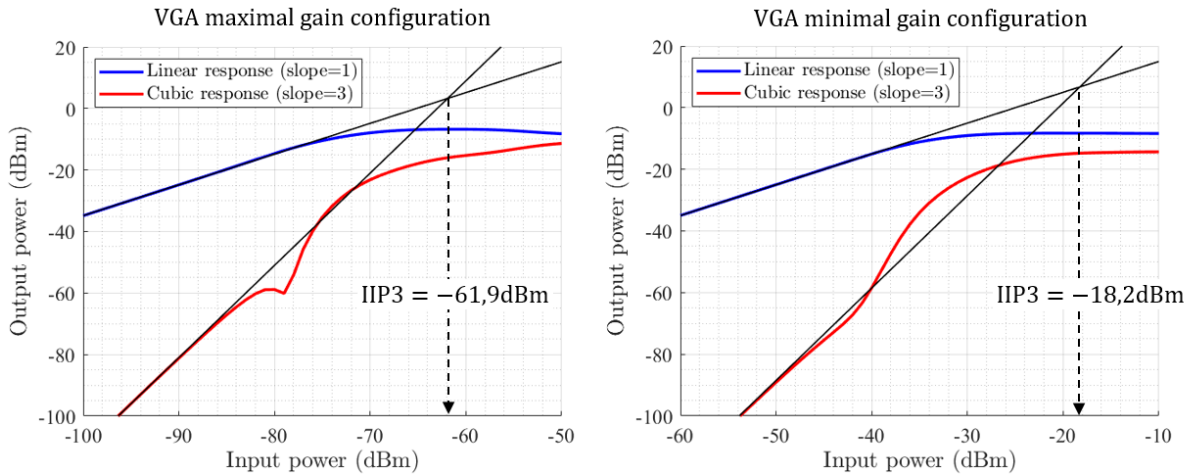
Finally, a noise analysis of the chip was conducted in the maximum and minimum VGA gain configuration as in Figure 169, whose SSB  $NF$  varies from 11.6dB to 14.2dB through the I-path.



**Figure 166: WILSON RX SSB I-path NF in the VGA lowest (left) and highest (right) gain configuration**

In order to meet specifications, either the LNA (4.6dB  $NF$ ) has to provide more gain to mitigate the impact of the following blocks, or the RX filter subsequent  $NF$  needs to be lowered (and/or the filter gain increased), to obtain an overall  $NF$  below 8dB.

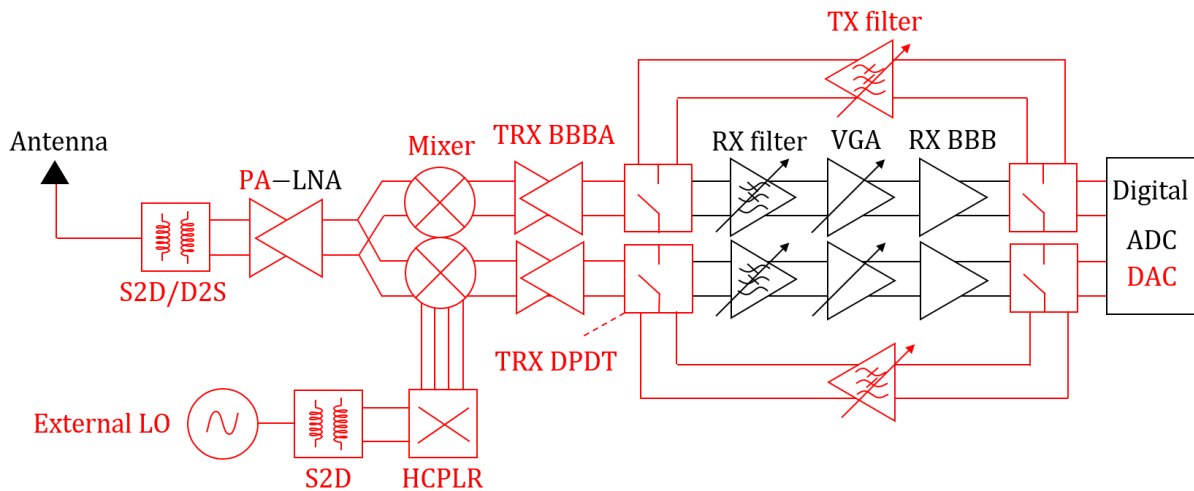
Finally, the two-tone third-order intermodulation products of the receiver were evaluated using a harmonic balance simulation using two input tones  $f_1$  and  $f_2$  at 38.51GHz and 38.52GHz, and by using a LO whose amplitude and frequency are 12.5dBm and 38.5GHz respectively. Figure 167 exhibits an IIP3 ranging from -61.9dBm to -18.2dBm from the highest gain to the lowest gain configuration.



**Figure 167: IIP3 interpolation of the receiver in the maximal and minimal VGA gain configuration at the maximal RX filter BW configuration**

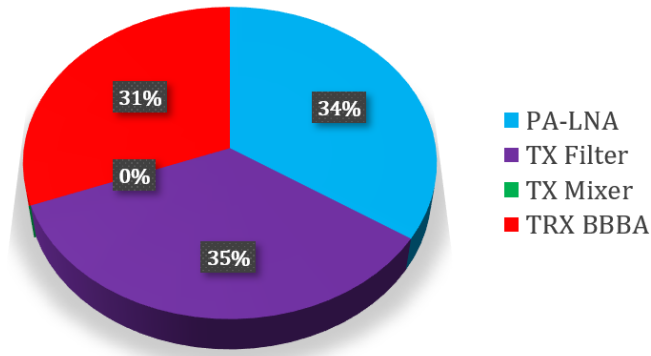
### 6.1.1 SIMULATION RESULTS IN TX MODE

In this section, post-layout simulations of the chip in transmission mode were made, including the I/O ring and the SPI. The simulated core building blocks are highlighted in red Figure 168.



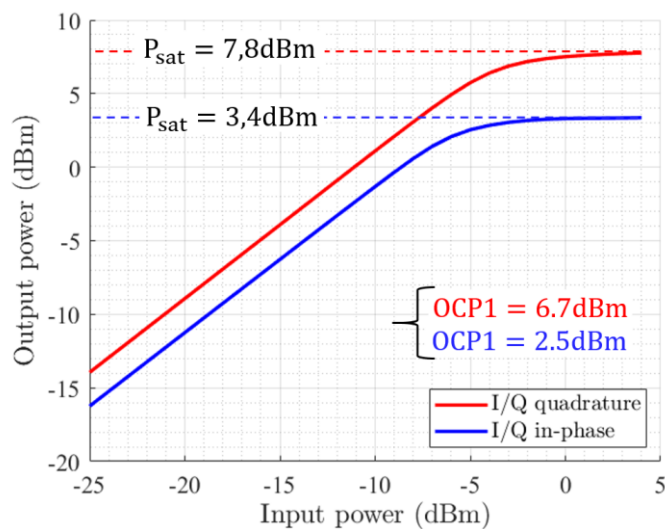
**Figure 168: Simulated WILSON TX chain**

The entire TX chain consumes only 34.1mW of static DC power and the repartition of the consumption of each building block is reported in Figure 169.



**Figure 169: WILSON TX chain DC power budget**

One remarkable thing is the consumption of the TX filter due to the subsequent size of the transistors involved that have to drive the low impedance presented by the input of the passive mixer. The Figure 171 and Figure 172 were obtained using the codes mentioned in the register map, at maximum DAC output power using respectively in-phase and in-quadrature baseband input signals, exhibiting the USB, LSB gains as well as the LO leakage and the image rejection ratio. Finally, the saturated output power of the chip in TX mode was evaluated in Figure 170 when I/Q baseband sources are respectively in quadrature or in phase resulting in a  $P_{sat}$  ranging from 7.8dBm to 3.4dBm.



**Figure 170: WILSON TX USB output power with respect to the input power (DACs output)**

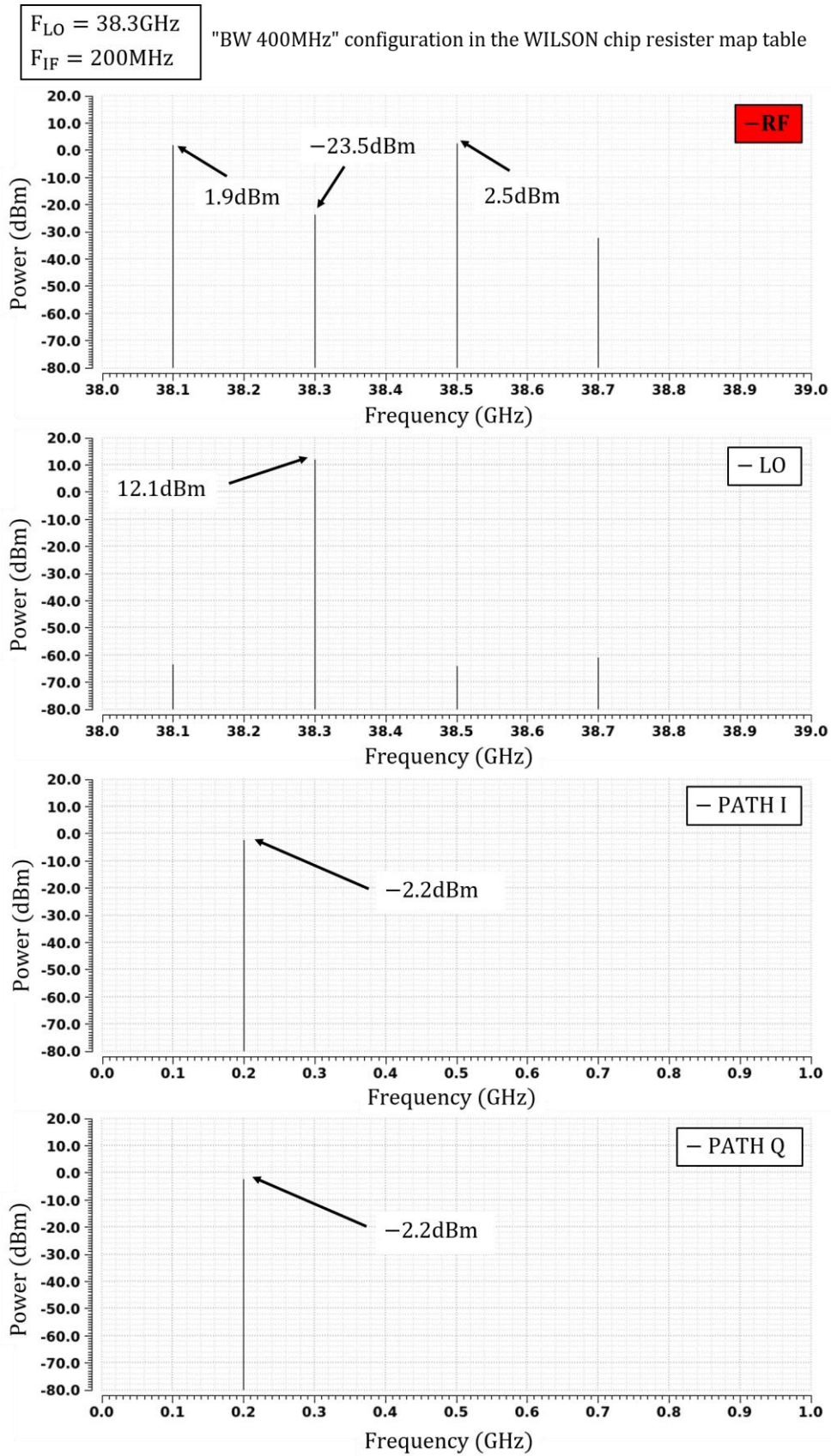


Figure 171: WILSON TX RF output power spectrum using in-phase I and Q under the 400MHz BW configuration at maximum DAC output power



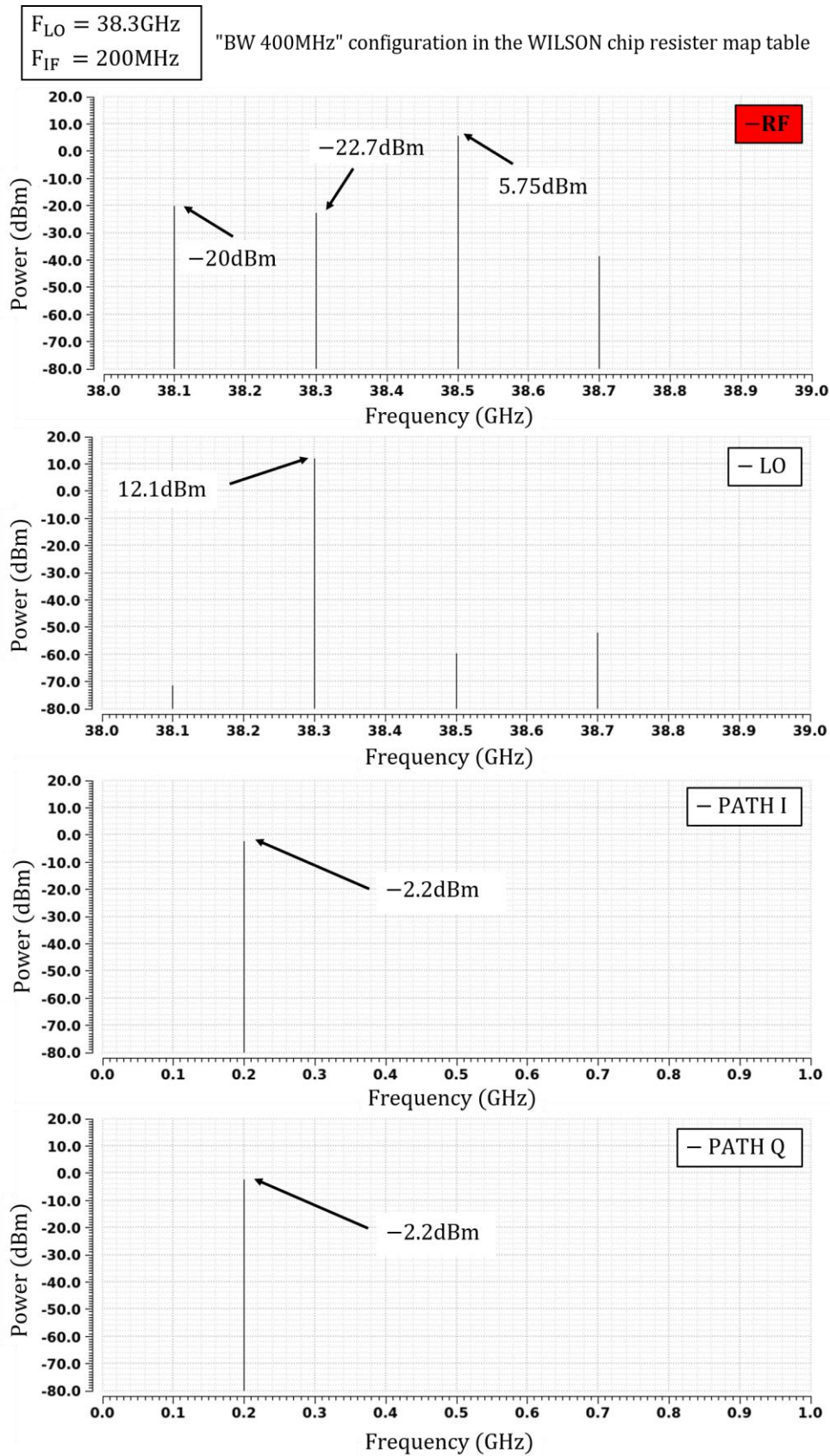
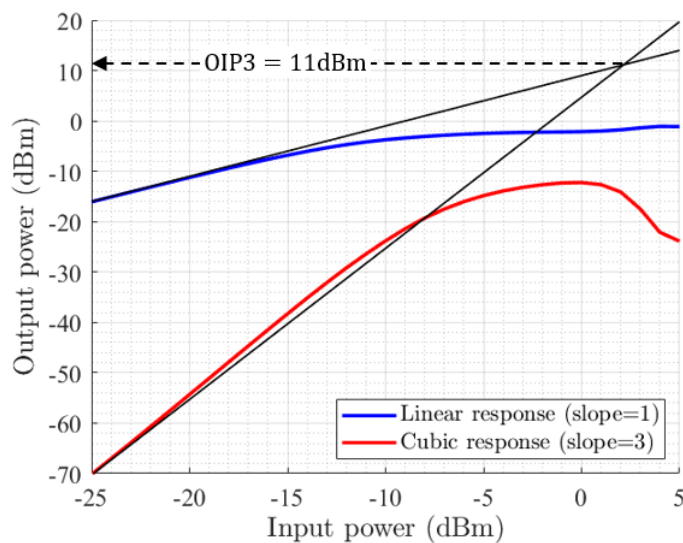


Figure 172: WILSON TX RF output power spectrum using quadrature I and Q under the 400MHz BW configuration at maximum DAC output power

From Figure 171 and Figure 172 the LO leakage is respectively ranging from -35.6dBm to -34.8dBm exhibiting a USB power gain of 4.7dB and 8dB.

The third-order intermodulation products of the transmitter were evaluated using a HB simulation using two input tones  $f_1$  and  $f_2$  at 10MHz and 20MHz, using a LO whose amplitude and frequency are 12.5dBm and 38.5GHz respectively. The OIP3 was interpolated at 11dBm as in Figure 173.



**Figure 173: OIP3 interpolation of the transmitter at maximal DAC output power and at the maximal TX filter BW configuration**

## 6.2 CONCLUSION

In this chapter, an integrated 5G FR2-1 transceiver, designed during the three years of this PhD thesis, was described through post-layout simulations. It exhibits promising characteristics as to its performances and chip size.

A summary of state-of-the art 5G transceivers operating at various frequencies is depicted in Figure 174, comparing the main performances and chip sizes of transceivers using matching network reusing in the design of the RFFE (D and E - in green), and others that don't (A to C - in yellow). It is clear that the bidirectional technique led to a strong reduction of the required silicon of each element.

Even though the system was not characterized in practice with measurements, a testing campaign will be carried out by the lab technical team.

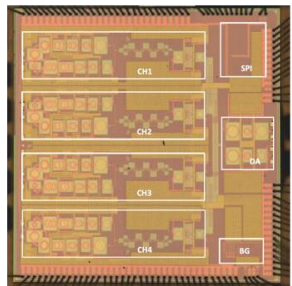
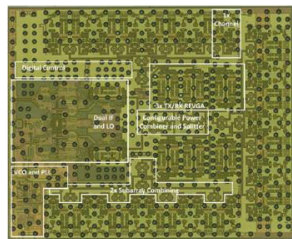
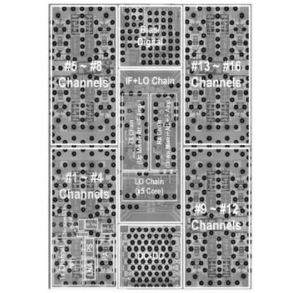
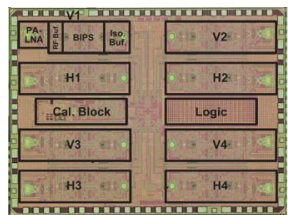
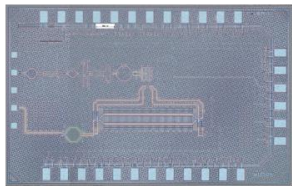
		5G transceivers	
A		65nm CMOS (24-30GHz)	
		<b><u>TX mode</u></b> EVM (%) <sup>4</sup> = 8.7 Pdc ele. (mW) = 115 Psat (dBm) > 16.5	<b><u>RX mode</u></b> NF (dB) = 5.1 <sup>5</sup> Pdc ele. (mW) = 80 Gain ele. (dB) = 25.8
		Size per TRX element : 4 mm <sup>2</sup>	
B		28nm CMOS (24GHz)	
		<b><u>TX mode</u></b> EVM (%) <sup>4</sup> = 5.2 Pdc ele. (mW) = 90 Psat (dBm) > 14	<b><u>RX mode</u></b> NF (dB) = 4.4 - 4.7 Pdc ele. (mW) = 42 Gain ele. (dB) = 32-34
		Size per TRX element : 1.16 mm <sup>2</sup>	
C		28nm CMOS (39GHz)	
		<b><u>TX mode</u></b> EVM (%) <sup>4</sup> = 4.5 <sup>13</sup> Pdc ele. (mW) = 115 Psat (dBm) > 16.5	<b><u>RX mode</u></b> NF (dB) = 4.2 - 4.6 Pdc ele. (mW) = 39 Gain ele. (dB) = 16-59
		Size per TRX element : 1.88 mm <sup>2</sup>	
D		65nm CMOS (28GHz)	
		<b><u>TX mode</u></b> EVM (%) <sup>4</sup> = 4.9% <sup>1</sup> Pdc ele. (mW) = 252 Psat (dBm) = 15.1	<b><u>RX mode</u></b> NF (dB) = 4.2-5 Pdc ele. (mW) = 112 Gain ele. (dB) ≈ 17
		Size per TRX element : 0.75 mm <sup>2</sup>	
E		22nm CMOS FD-SOI (39GHz)	
		<b><u>TX mode</u></b> EVM (%) <sup>4</sup> > 2.2 <sup>2</sup> Pdc ele. (mW) = 34.1 Psat (dBm) = 7.8	<b><u>RX mode</u></b> NF (dB) > 11.6 Pdc ele. (mW) = 73.8 Gain ele. (dB) = 24.5-65
		Size per TRX element : 0.79 (0.40 without LO GEN)	
		/wo merged mmW FE	<sup>1</sup> 800MHz BW <sup>2</sup> @7dB back-off <sup>3</sup> @Pout max
		/w merged mmW FE	<sup>4</sup> 400MHz BW 64-QAM OFDM <sup>5</sup> minimum

Figure 174: 5G transceivers overview from (A) to (D) are respectively [1], [83], [84] and [85]

# GENERAL CONCLUSION

In this three years PhD thesis, a 5G FR2-1 transceiver was to be designed almost from scratch. In order to do so, the 5G has been introduced, and compared with previous generations. The selected frequency range, the duplexing technique as well as the employed modulation was presented in Chapter 1. In Chapter 2, the system was hence sized in order to get block-by-block specifications, to set design targets. The design started in Chapter 3 with the conception of a mmW bidirectional amplifier. This amplifier exhibits very promising simulated characteristics as a  $NF$  of 4.6dB and a gain of 23.8dB in LNA mode and a  $P_{sat}$  of 7.5dBm with a  $PAE$  of 27.4% in PA mode, at the center of the frequency band located at 38.5GHz. The size of this amplifier was found very remarkable compared with the state-of-the-art, and requires a silicon area of only 0.11mm<sup>2</sup>. This amplifier was published and sent two times in fabrication using the 22nm CMOS FD-SOI technology, in a standalone fashion (K2000, TESTCHIP22), and one time within the final integrated transceiver (WILSON). Even though the first version of this amplifier was dysfunctional, the second one exhibited attractive performances, but were degraded compared with post-layout simulations. In chapter 4, the frequency conversion aspect was addressed, through the design of a double-balanced passive mixer, whose operation was highly favourable to a simple integration into bidirectional systems. As the SX was not covered in this work, an off-chip LO source was associated with a designed integrated hybrid coupler in order to obtain quadrature signals mandatory for a proper use of the mixer. Also, 50Ω transmission lines as well as microstrip lines were also designed and integrated in the WILSON chip to propagate various RF signals. In chapter 5, the baseband I/Q branches were designed. In this thesis, a 7-bits controlled VGA, two reconfigurable filters, a TRX DPDT switch and a 50Ω buffer were designed. The design of a bidirectional filter was also presented, and published. These blocks were integrated in the TESTCHIP22 and WILSON chips and controlled using an integrated SPI. The TESTCHIP22 chip provided the measured performances of the analog baseband blocks only. Finally, in Chapter 6, the entire transceiver was simulated and sent to fabrication. One single element provides a  $P_{sat}$  of 7.8dBm consuming 34.1mW in transmit mode, as well as a  $NF$  of 11.6dB (at maximum gain) with a gain ranging from 24.5dB to 65dB in receive mode. Axis of improvements are presented in the next section.

# DISCUSSION AND PERSPECTIVES

This manuscript presented the design of a 5G FR2-1 transceiver which was fabricated in 22nm CMOS FD-SOI operating at 38.5GHz, meant to be included in a digital beamforming architecture. Most of the building blocks were designed especially for this work. It was stated previously, this transceiver will be characterized in order to verify with measurements its adequate behaviour, and more generally to demonstrate the relevancy of bidirectional systems in multi-elements architectures, even though the literature already suggests their interest, at the glance of the works published in recent years. This work allowed to isolate several points that seem to be essential for future works. First of all, the choice of the HCPLR of LO was not relevant for compact applications given the substantial size of the stacked coupled lines, but was a good choice in terms of developing time, considering that a prior design could be adapted within this work. Secondly, the dummies pattern could be shaped differently, in this work it was chosen as such the metal density was as high as possible, but drawbacks over performances could hence be noticeable. A better trade-off is hence to be found. A TX VGA will also be mandatory to set the RMS power value at the input of the PA as such a sufficient BO is obtained to guarantee its EVM contribution to remain low. This actually could have been implemented with a variable gain BBBA (or filter) using a digitally-controlled feedback resistor. A bidirectional TRX baseband VGA could also be investigated for saving silicon surface. In general, it is always interesting to think ahead of architectures providing a bilateral operation, as they are meant to be included in multi-elements systems – such as digital beamforming systems – and hence will be duplicated many times. However, it will come to a higher complexity cost for RF/analog designers. Then, extra work could also be done to incorporate calibration circuits, that are mandatory to guarantee the proper behaviour of circuits sensitive to process variations, such as active-RC active filters. Finally, the noise figure of the RX VGA and filter can be optimized by using a different set of lumped components (capacitors in particular) to meet the requirements imposed by the use of 64-QAM CP-OFDM modulation schemes. To put it in a nutshell, this manuscript represents a complete overview of both system and design analysis which can be used for future works over 5G bidirectional transceiver designs, meant to be integrated in digital or hybrid beamforming architectures.

# LIST OF PUBLICATIONS

## INTERNATIONAL CONFERENCES

- L. Paquien, B. Martineau, D. Belot, and N. Deltimple, “Design of a 37-40GHz bidirectional amplifier for 5G FR2 radio beamforming systems in 22nm CMOS FD-SOI,” in *2023 30th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Dec. 2023, pp. 1–4. doi: 10.1109/ICECS58634.2023.10382936.
- L. Paquien, B. Martineau, D. Belot, and N. Deltimple, “A compact bidirectional reconfigurable 2nd-order low-pass filter for 5G FR2 applications,” in *2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, Jun. 2023, pp. 77–80. doi: 10.1109/PRIME58259.2023.10161920.

## NATIONAL CONFERENCES

- L. Paquien, B. Martineau, D. Belot, and N. Deltimple, “Conception d’un amplificateur bidirectionnel pour système radio à formation de faisceau 5G FR2 37-41GHz en technologie CMOS 22nm FD-SOI,” *22èmes Journées Nationales Micro-Ondes (JNM), 2022, Limoges, France.*

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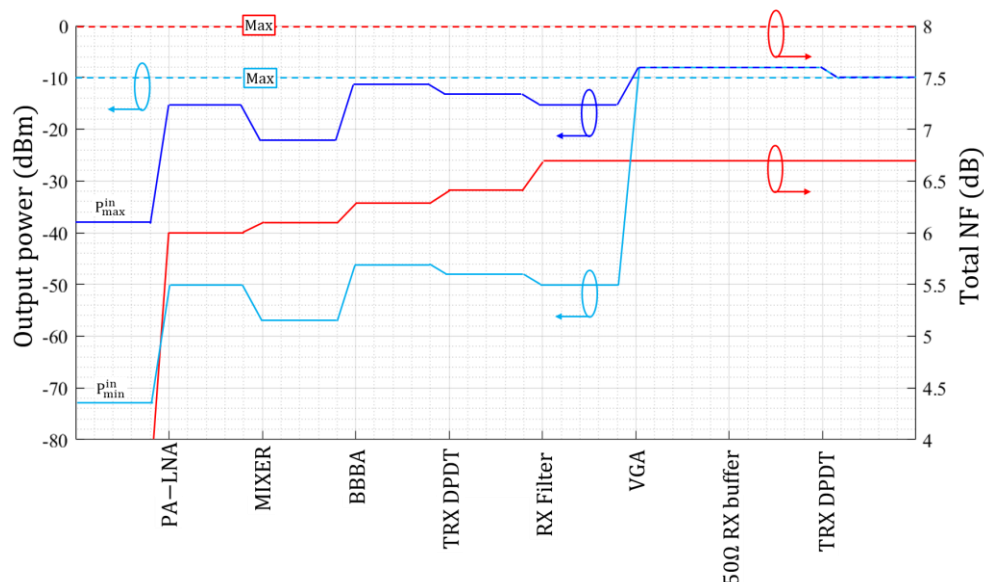
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# APPENDIX A: GRAPHIC REPRESENTATION OF THE RX POWER AND NOISE BUDGET

As an illustration, the power and noise budget tables in page 34 were represented in a graph in order to visualize the increase of the  $NF$  stage after stage, as well as the power levels throughout the system when the received input power is at its maximum (dark blue), and when the input power reaches the sensitivity of the receiver (light blue).



**Figure 175: Alternative representation of the power (blues) and noise (red) budget in RX mode**

It can be seen that the reconfigurability of the gain of the receiver is only made varying the gain of the baseband VGA to provide a constant power at the input of the ADCs. The VGA  $NF$  was taken under the worst-case scenario, when its gain is minimal, for illustration simplicity.

# APPENDIX B: WILSON CHIP REGISTER MAP TABLE

Register map		Default	Rx enable	Tx enable	VGA G1	VGA G2	VGA G3	VGA G4.1	VGA G4.2	VGA AG	BW 400MHz	BW 200MHz	BW 100MHz	BW 50MHz	BW 400MHz	BW 200MHz	BW 100MHz	BW 50MHz				
SPI_REGM<348>	BB_RX_DIG_STAGE_CTRL_I	0	0	0	1	0	1	0	0	G1.2.3.4	0	0	0	0	0	0	0	0				
SPI_REGM<349>	BB_RX_DIG_LOW_GAIN_MODE_I	1	1	1	0	0	1	1	1	G1.2.3.4	1	1	1	1	1	1	1	1				
SPI_REGM<350>	BB_RX_DIG_STAGE_CTRL_Q	0	0	0	1	0	1	0	0	G1.2.3.4	0	0	0	0	0	0	0	0				
SPI_REGM<351>	BB_RX_DIG_LOW_GAIN_MODE_Q	1	1	1	0	0	1	0	1	G1.2.3.4	1	1	1	1	1	1	1	1				
SPI_REGM<352>	BB_RX_DIG_VGA_I<0>	0	0	0	1	1	1	1	0	X	0	0	0	0	0	0	0	0				
SPI_REGM<353>	BB_RX_DIG_VGA_I<1>	0	0	0	1	1	1	1	0	X	0	0	0	0	0	0	0	0				
SPI_REGM<354>	BB_RX_DIG_VGA_I<2>	0	0	0	1	1	1	1	0	X	0	0	0	0	0	0	0	0				
SPI_REGM<355>	BB_RX_DIG_VGA_I<3>	0	0	0	1	1	1	1	0	X	0	0	0	0	0	0	0	0				
SPI_REGM<356>	BB_RX_DIG_VGA_I<4>	0	0	0	1	1	1	1	0	X	0	0	0	0	0	0	0	0				
SPI_REGM<357>	BB_RX_DIG_FILTER_I<0>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
SPI_REGM<358>	BB_RX_DIG_FILTER_I<1>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
SPI_REGM<359>	BB_RX_DIG_FILTER_I<2>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
SPI_REGM<360>	BB_RX_DIG_VGA_Q<0>	0	0	0	1	1	1	1	0	X	0	0	0	0	0	0	0	0				
SPI_REGM<361>	BB_RX_DIG_VGA_Q<1>	0	0	0	1	1	1	1	0	X	0	0	0	0	0	0	0	0				
SPI_REGM<362>	BB_RX_DIG_VGA_Q<2>	0	0	0	1	1	1	1	0	X	0	0	0	0	0	0	0	0				
SPI_REGM<363>	BB_RX_DIG_VGA_Q<3>	0	0	0	1	1	1	1	0	X	0	0	0	0	0	0	0	0				
SPI_REGM<364>	BB_RX_DIG_VGA_Q<4>	0	0	0	1	1	1	1	0	X	0	0	0	0	0	0	0	0				
SPI_REGM<365>	BB_RX_DIG_FILTER_Q<0>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
SPI_REGM<366>	BB_RX_DIG_FILTER_Q<1>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
SPI_REGM<367>	BB_RX_DIG_FILTER_Q<2>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
SPI_REGM<368>	SPDT_TX_DIG	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1				
SPI_REGM<369>	PA_MODE_DIG	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1				
SPI_REGM<370>	BB_TX_DIG_FILTER_I<0>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
SPI_REGM<371>	BB_TX_DIG_FILTER_I<1>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
SPI_REGM<372>	BB_TX_DIG_FILTER_I<2>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
SPI_REGM<373>	BB_TX_DIG_FILTER_Q<0>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
SPI_REGM<374>	BB_TX_DIG_FILTER_Q<1>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
SPI_REGM<375>	BB_TX_DIG_FILTER_Q<2>	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1				
Tx mode					max gain														min gain			
Rx mode					max gain														X<4> min gain [per gain config]			

Figure 176: Register map of the WILSON chip

