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Functionalization of field effect transistors based on transition metal dichalcogenides : towards high-performance devices

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THÈSE

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Discipline/ Spécialité Chimie

Fonctionnalisation de Transistors à Effet de Champ à Base de Dichalcogénures de Métaux de Transition: Vers des Dispositifs Performants

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Résumé de Thèse

Au cours des dernières décennies, les dispositifs semi-conducteurs traditionnels à base de silicium ont suivi la « loi de Moore », évoluant vers une taille plus petite et des fonctions plus puissantes.^[1; 2] Cependant, à mesure que la taille du canal continue de diminuer, les transistors sont confrontés à de nombreuses limitations physiques, telles que la génération de chaleur, les fuites et les effets de canal court, qui conduisent également à la quasi-stagnation de la « loi de Moore ».^[3; 4] Par conséquent, il est impératif de développer des matériaux semi-conducteurs hautes performances de nouvelle génération.

Parmi les semi-conducteurs bidimensionnels (2D), les dichalcogénures de métaux de transition (TMD) affichent une bande interdite réglable, une surface libre de liaisons pendantes, d'excellentes propriétés optiques et optoélectroniques et une transparence flexible, etc.^[5-7] De plus, en tant que matériaux 2D à l'échelle nanométrique, ils ont une épaisseur à l'échelle atomique, une surface spécifique élevée et une grande surface plane au niveau atomique. Leurs propriétés physiques et chimiques sont facilement affectées par des changements dans les environnements de surface et d'interface.^[8-10] De ce fait, leur interfaçage avec des molécules fonctionnalisées modifie radicalement leurs propriétés, ouvrant des perspectives intrigantes pour des applications dans les futurs dispositifs électroniques et optoélectroniques. Pour ces raisons, ils ont attiré une large attention et deviennent les alternatives les plus prometteuses aux semi-conducteurs traditionnels à base de silicium.^[11; 12]

Le TMD prototypique est le bisulfure de molybdène (MoS_2). Il combine d'excellentes propriétés électriques, optiques et mécaniques, et surtout, il peut supprimer efficacement l'effet de canal court qui apparaît lors de la réduction de la taille du canal dans les semi-conducteurs traditionnels à base de silicium, ce qui le rend très pertinent pour son intégration en tant que composant actif dans les transistors à effet de champ (FET).^[13; 14]

Le diséléniure de tungstène (WSe_2), avec ses propriétés naturelles uniques de canaux de transport doubles d'électrons et de trous et son excellente accordabilité de polarité de

transport, est devenu un matériau vedette pour le développement de circuits logiques à haut rendement.^[15; 16] Par conséquent, il présente un grand potentiel dans les futures applications de puces et de circuits logiques intégrés (LC).^[17; 18]

Cependant, malgré leur énorme potentiel, l'utilisation des TMD dans les appareils électroniques est encore au stade exploratoire. Les FET basés sur des TMD souffrent toujours de barrières d'injection de porteurs élevées, d'une grande résistance de contact et d'un épinglage au niveau de Fermi (FLP) important entre les électrodes métalliques et les semi-conducteurs.^[19; 20] De plus, les FET de type N purs et les FET de type P purs, en tant que composants de base essentiels pour les circuits intégrés, manquent toujours de méthodes stables et fiables pour contrôler efficacement la polarité de transport de porteur dans les FET à base de TMD.^[21; 22] À cet égard, ces défis sont abordés dans cette thèse en exploitant la fonctionnalisation des interfaces de l'appareil, notamment :

- i. Fonctionnalisation des semi-conducteurs TMD via une stratégie d'ingénierie des défauts avec des molécules auto-assemblées.
- ii. La fonctionnalisation des électrodes à contact supérieures via la technologie d'auto-assemblage avec des monocouches auto-assemblées (SAM).
- iii. La fonctionnalisation des électrodes de contact supérieures par pré-ajout de couche auxiliaire d'injection d'électrons/trous.

Ce travail de thèse comprend 3 projets :

Le 1^{er} projet est axé sur l'application de la fonctionnalisation des semi-conducteurs TMD pour la reconnaissance des isomères. Tout d'abord, la surface de cristaux de MoS₂ monocouche exfoliés mécaniquement a été étudiée. Grâce à la caractérisation de son épaisseur, de sa morphologie, de ses propriétés spectroscopiques (spectroscopie Raman, spectroscopie de photoluminescence (PL)) et compositionnelles (spectroscopie photoélectronique à rayons X, XPS), ses excellentes caractéristiques de surface ont été

démonstrées. Ensuite, la stratégie d'ingénierie des défauts a été utilisée pour éliminer une partie des atomes de S de la monocouche MoS₂ par recuit à haute température de 300 °C, générant une certaine quantité de défauts de lacunes de soufre, qui sont des sites hautement réactifs pour la liaison chimique avec des molécules (Figure I).

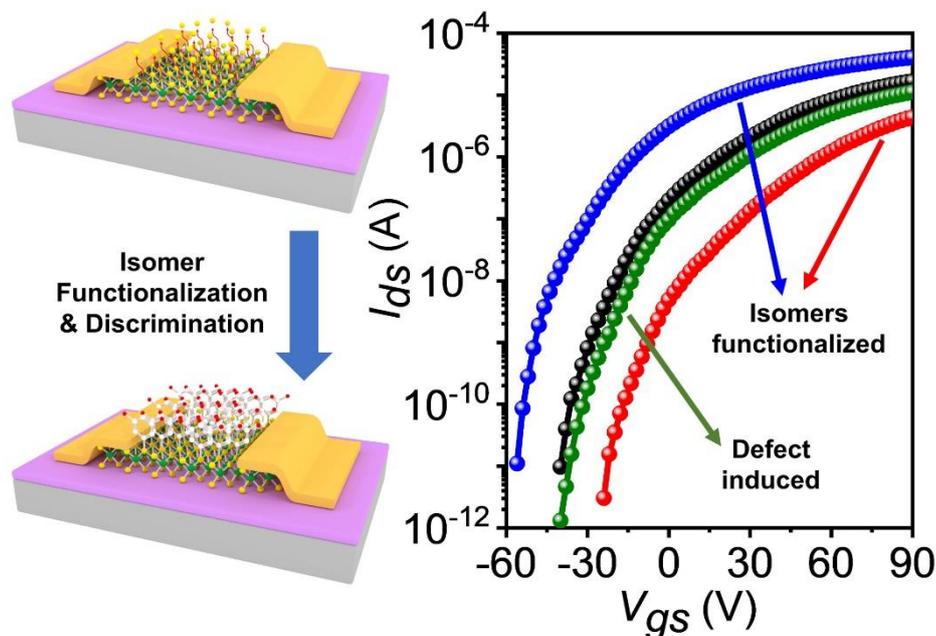


Figure I Illustration schématique des étapes de fonctionnalisation des isomères pour les dispositifs FET. Panneau de gauche : Fonctionnalisation de défauts induits par des semi-conducteurs MoS₂ monocouche avec des isomères via l'auto-assemblage. Panneau de droite : Courbes de transfert du dispositif FET MoS₂ monocouche vierge, comparées aux dispositifs induits par défaut et fonctionnalisés par les isomères.

Les propriétés morphologiques et spectroscopiques ainsi que leur composition de la monocouche MoS₂ ont été à nouveau caractérisées par microscopie, analyse élémentaire XPS, Raman et PL, prouvant la génération réussie de défauts. Ensuite, deux isomères de même formule chimique mais de structure différente ont été choisis, à savoir le 2,6-difluorobenzèthiol (26DFBT) et le 3,5-difluorobenzèthiol (35DFBT). En raison des positions différentes des deux groupes de substituants fluor, bien qu'ils aient la même formule chimique et des structures chimiques similaires, ils présentent une orientation de moment dipolaire opposée et des propriétés de dopage induites par dipôle différentes. La

chimisorption d'isomères moléculaires fonctionnalisés au thiol a été utilisée pour les ancrer sur des défauts de manque de soufre, les attachant de manière covalente à la monocouche MoS₂, donnant une fonctionnalisation robuste de la monocouche MoS₂ (Figure I). Les décalages de pic de Mo 3d et S 2p dans les spectres XPS, le décalage du pic A1g dans les spectres Raman et les changements d'intensité et de position du spectre PL indiquent que 26DFBT peut introduire un dopage électronique dans MoS₂, tandis que 35DFBT peut introduire un dopage de trous dans MoS₂. De plus, les résultats des FET montrent également que la tension de seuil (V_{th}) du dispositif MoS₂ fonctionnalisé 26DFBT se décale négativement, tandis que le V_{th} du dispositif MoS₂ fonctionnalisé 35DFBT se décale positivement (Figure I). La modulation de la densité de porteurs de charge est aussi élevée que 10^{12} cm^{-2} , étant comparable aux dopants moléculaires conventionnels, permet ainsi une reconnaissance précise des isomères. Nos résultats soulignent le potentiel des matériaux 2D à des fins de discrimination moléculaire, en particulier pour l'identification d'isomères complexes.

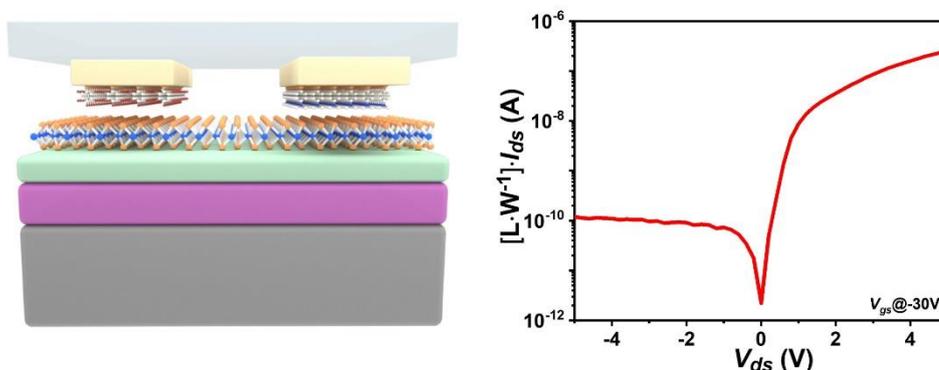


Figure II Illustration schématique du dispositif FETs MoS₂ asymétrique et tracé semi-logarithmique de la courbe de sortie dans des conditions de polarisation de grille de -30 V. L'électrode de drain est une électrode fonctionnalisée PFBT et l'électrode fonctionnalisée DABT est mise à la terre.

Le 2^e projet se concentre sur l'étude de l'influence de l'utilisation d'électrodes supérieures fonctionnalisées auto-assemblées sur l'injection de porteurs dans les dispositifs FET à base de TMD. Une approche d'ingénierie de contact a été démontrée pour fonctionnaliser les électrodes pour la configuration des FET à contact supérieur en transférant des électrodes

pré-modifiées chimiquement. Les électrodes à motifs ont d'abord été préparées par évaporation thermique à travers un masque, puis les électrodes à motifs ont été modifiées avec une fonctionnalisation d'auto-assemblage. Des molécules avec différentes directions dipolaires nous ont permis d'ajuster la fonction de travail (WF) de l'électrode Au de 5,00 eV pour l'électrode nue à 4,30 eV pour les électrodes fonctionnalisées (diméthylamino)benzénethiol (DABT) ou 5,67 eV pour les électrodes fonctionnalisées au 2,3,4,5,6-pentafluorobenzénethiol (PFBT). En utilisant la technologie de transfert à sec, les électrodes fonctionnalisées ont été transférées sur une surface de film de polydiméthylsiloxane (PDMS), puis retournées et stratifiées physiquement sur la surface des TMD pour fabriquer des FET avec des électrodes de contact supérieur fonctionnalisées (voir la structure des FET à la figure II). Notre étude montre que les électrodes pré-fonctionnalisées avec des molécules donneuses d'électrons peuvent améliorer considérablement les performances du dispositif, avec une mobilité moyenne aussi élevée que $30 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ et une barrière d'injection de porteur aussi faible que 0,19 eV. Cependant, les FET avec des électrodes pré-fonctionnalisées avec des molécules contenant des groupes attracteurs d'électrons peuvent réduire considérablement les performances du dispositif, avec une mobilité moyenne aussi faible que $8,1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ et une barrière d'injection aussi élevée que 0,53 eV. En raison de l'avantage du contact van der Waals (vdW) entre l'électrode et le semi-conducteur, le FLP est atténué, avec un facteur d'épinglage de 0,33, ce qui est bien supérieur au 0,1 pour les électrodes à évaporation thermique. De plus, des FET avec des électrodes fonctionnalisées asymétriques ont été fabriqués, c'est-à-dire des diodes Schottky, en transférant des électrodes pré-fonctionnalisées avec différentes molécules (Figure II). Le dispositif montre un excellent rapport de rectification (RR) supérieur à 10^3 , qui est attribué aux différentes barrières d'injection des électrodes source-drain en raison de la fonctionnalisation chimique asymétrique des électrodes des deux côtés (Figure II).

Le 3^{ème} projet est dédié à l'étude de l'impact de la fonctionnalisation de la couche de transport auxiliaire électron/trou pré-ajoutée d'électrode sur le type de porteur dans les FET à base de TMD. La différence entre les interfaces d'électrodes obtenues par la méthode de transfert à sec sans solvant et la méthode classique d'évaporation thermique a été

caractérisée dans un premier temps. Les électrodes de transfert sèches sans solvant peuvent directement stratifier physiquement l'interface atomiquement plate sur le semi-conducteur pour obtenir un contact vdW sans endommager le cristal TMD. La technologie des électrodes de transfert à sec a été utilisée pour fabriquer des FET basés sur un cristal WSe₂ déposé chimiquement en phase vapeur (CVD) avec des électrodes Au ou Ag, respectivement. En raison de l'interface non destructive du contact vdW, le dispositif FET avec des électrodes Au présente une ambipolarité dominante de type P, tandis que le dispositif FET avec des électrodes Ag présente une ambipolarité presque équilibrée des électrons et des trous. Ensuite, les électrodes ont été fonctionnalisées en ajoutant au préalable une couche de transport auxiliaire d'électrons/trous lors de la préparation des électrodes, puis en préparant des électrodes métalliques à motifs par le biais d'une approche de masque et d'évaporation thermique. Pendant le transfert d'électrode, la couche auxiliaire est laminée avec l'électrode métallique sur la surface cristalline WSe₂, réalisant un contact vdW entre la couche auxiliaire et les TMD. L'électrode en or pré-fonctionnalisée avec une couche d'injection de trous (HIL, trioxyde de molybdène (MoO₃)) démontre un transport unipolaire de type P, et les porteurs d'électrons sont considérablement supprimés pour disparaître en raison du WF plus élevé de MoO₃ que 6 eV, ce qui rend son niveau de Fermi plus adapté avec la bande de valence (VB) de WSe₂. De plus, l'électrode Ag avec une couche d'injection d'électrons (EIL, 8-Quinolinolato lithium (Liq)) en tant que couche auxiliaire présente un transport unipolaire de type N, et les porteurs de trous dans le canal sont supprimés pour disparaître en raison du WF de Liq est plus proche de la bande de conduction (CB) de WSe₂, ce qui rend l'injection d'électrons plus favorable. Les résultats ont été vérifiés avec du WSe₂ à quelques couches exfolié mécaniquement, et les mêmes résultats ont été obtenus (Figure III). En outre, une diode métal-semi-conducteur-métal (MSM) a été fabriquée en transférant une électrode avec une couche auxiliaire différente sur la même surface cristalline WSe₂ développée par CVD et a démontré un RR de 10³. Enfin, un onduleur logique basé sur des FET NMOS et PMOS WSe₂ avec un gain maximum de 1,73 à une tension d'entrée de 5 V a été démontré.

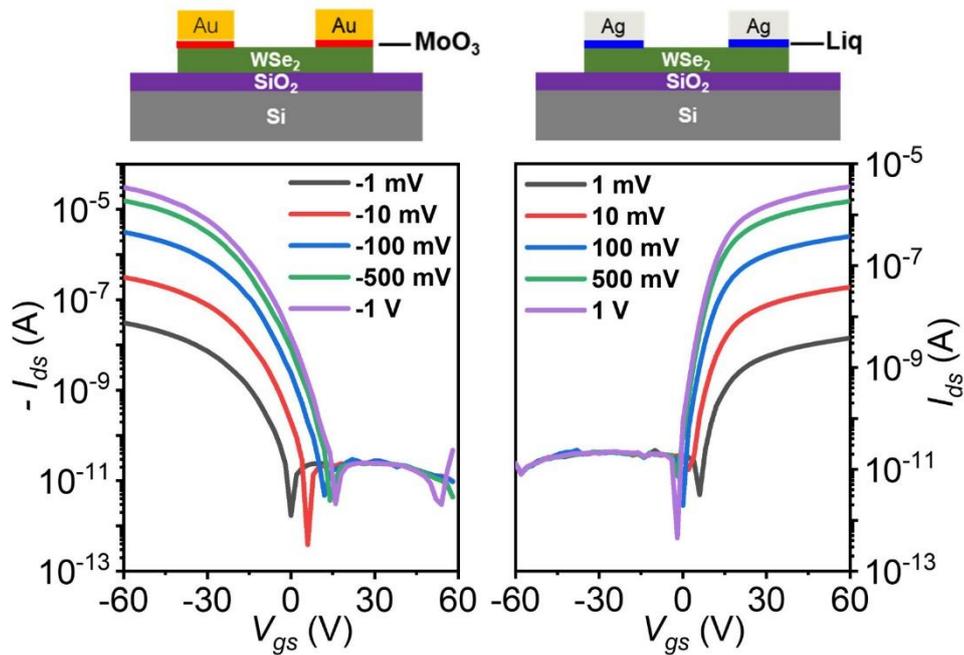


Figure III Schéma de principe des FET WSe₂ avec contact vdW d'électrodes fonctionnalisées par couche auxiliaire et leurs courbes de transfert.

Dans cette thèse, la fonctionnalisation des FET à base de TMD est systématiquement étudiée, y compris la fonctionnalisation du semi-conducteur TMD et la fonctionnalisation de l'électrode métallique. Nos travaux montrent que la fonctionnalisation des dispositifs est une approche puissante qui peut être utilisée pour fabriquer des dispositifs hautes performances, notamment des FET, des diodes et des onduleurs logiques, etc. En particulier, la fonctionnalisation des semi-conducteurs a montré un potentiel unique pour distinguer les isomères, tandis que la fonctionnalisation des électrodes offre d'énormes opportunités pour les diodes et les circuits logiques. La fonctionnalisation de l'appareil offre une stratégie sans précédent et puissante pour ajuster les propriétés des FET à base de TMD et adapter les performances de l'appareil à la demande. Ces résultats ouvrent la voie à la fabrication de circuits intégrés à base de matériaux 2D.

Abstract

In the past few decades, traditional silicon-based semiconductor devices have followed “Moore's Law”, developing towards smaller size and more powerful functions.^[1; 2] However, as the channel size continues to shrink, transistors face many physical limitations, such as heat generation, leakage and short-channel effects, which also lead to the near-stagnation of “Moore's Law”.^[3; 4] Therefore, it is imperative to develop next-generation high-performance semiconductor materials.

Among two-dimensional (2D) semiconductors, transition metal dichalcogenides (TMDs) display adjustable bandgap, dangling bonds free surface, excellent optical and optoelectronic properties and flexible transparency, etc.^[5-7] Moreover, as nanoscale 2D materials, they have atomic-scale thickness, high specific surface area and large atomic-level flat surface area. Their physical and chemical properties are easily affected by changes in the surface and interface environments.^[8-10] Because of this reason, their interfacing with functionalized molecules drastically modify their properties, opening intriguing perspectives for applications in future electronic and optoelectronic devices. As a result of these reasons, they have attracted widespread attention and are becoming the most promising alternatives to traditional silicon-based semiconductors.^[11; 12]

The prototypical TMDs is molybdenum disulfide (MoS_2). It combines excellent electrical, optical and mechanical properties, and most importantly it can effectively suppress the short-channel effect that appear upon shrinking the channel size in traditional silicon-based semiconductors, making it highly relevant for its integration as active component in field of field-effect transistors (FETs).^[13; 14] Tungsten diselenide (WSe_2), with its unique natural properties of electron and hole dual transport channels and excellent transport polarity tunability, has become a star material for the development of high-efficiency logic circuits.^[15; 16] Therefore, it holds great potential in future chip and integrated logic circuits (LCs) applications.^[17; 18]

However, despite their enormous potential, the use of TMDs in electronic devices is still in the exploratory stage. TMDs-based FETs still suffer from high carrier injection barriers, large contact resistance and serious Fermi-level pinning (FLP) between metal electrodes and semiconductors.^[19; 20] Moreover, pure N-type FETs and pure P-type FETs, as essential basic building blocks for integrated circuits, still lack stable and reliable methods to effectively control the carrier transport polarity in TMDs-based FETs.^[21; 22] In this regard, such challenges are tackled within this thesis by exploiting the functionalization of the device interfaces, including:

- i. TMDs semiconductor functionalization via defect engineering strategy with self-assembled molecules.
- ii. The top-contact electrodes functionalization via self-assembly technology with self-assembled monolayers (SAMs).
- iii. The top-contact electrodes functionalization by pre-addition of electron/hole injection auxiliary layer.

This thesis work comprises 3 projects:

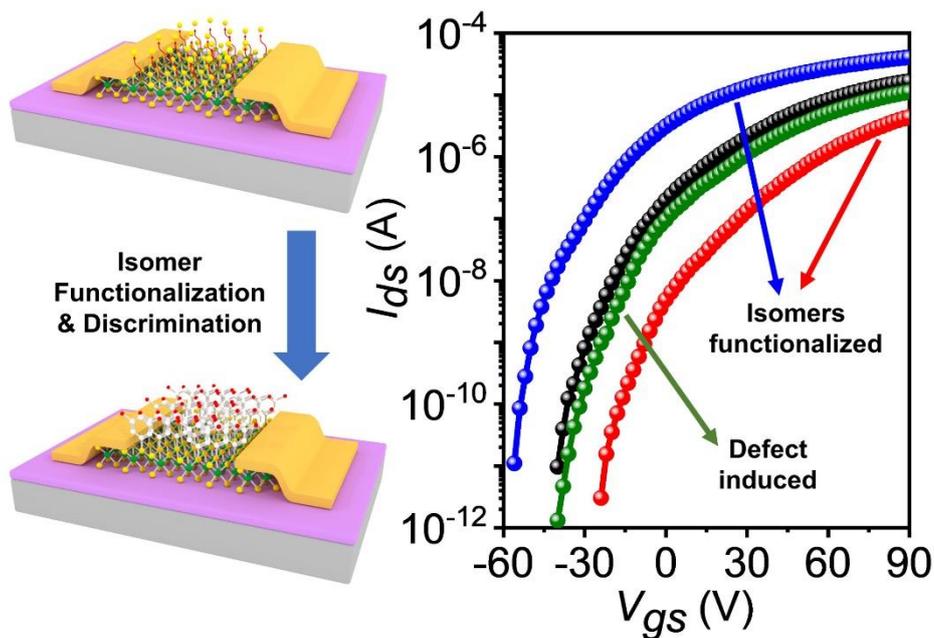


Figure I Schematic illustration of isomers functionalization steps for FET devices. Left panel: Functionalization of defects induced monolayer MoS₂ semiconductor with isomers via self-assembly. Right panel: Transfer curves of pristine monolayer MoS₂ FETs device, compared with defect induced and isomers functionalized devices.

The 1st project is focused on the application of TMDs semiconductor functionalization for isomer recognition. First, the surface of mechanically exfoliated monolayer MoS₂ crystals was investigated. Through characterization of its thickness, morphology, spectroscopical (Raman spectroscopy, photoluminescence (PL) spectroscopy) and compositional (X-ray photoelectron spectroscopy, XPS) properties, its excellent surface characteristics were demonstrated. Then, the defect engineering strategy was used to remove part of the S atoms from monolayer MoS₂ by high-temperature of 300 °C annealing, generating a certain amount of sulfur vacancy defects, which are highly reactive sites for chemical bonding with molecules (Figure I). The morphological and spectroscopical properties as well as their composition of the monolayer MoS₂ was again characterized by microscopy, XPS elemental analysis, Raman and PL, proving the successful defects generation. Next, two isomers with the same chemical formula but different structures were chosen, i.e., 2,6-difluorobenzenethiol (26DFBT) and 3,5-difluorobenzenethiol (35DFBT). Due to the different positions of the two fluorine substituent groups, although they have the same chemical formula and similar chemical structures, they exhibit opposite dipole moment orientation and different dipole induced doping properties. Chemisorption of thiol-functionalized molecular isomers was used to anchor them on sulfur vacancy defects, covalently tethering them to the monolayer MoS₂, yielding a robust functionalization of the monolayer MoS₂ (Figure I). The peak shifts of Mo 3d and S 2p in XPS spectra, the shift of A_{1g} peak in Raman spectra and the intensity and position changes of the PL spectrum indicate that 26DFBT can introduce electron doping to MoS₂, while 35DFBT can introduce hole doping to MoS₂. Moreover, the FET results also show that the threshold voltage (V_{th}) of the 26DFBT functionalized MoS₂ device shifts negatively, while the V_{th} of the 35DFBT functionalized MoS₂ device shifts positively (Figure I). The modulation of the charge carrier density is as high as 10^{12} cm^{-2} , being comparable to conventional molecular dopants, thus allowing precise recognition of isomers. Our findings underscore the potential of 2D

materials for molecular discrimination purposes, in particular for the identification of complex isomers.

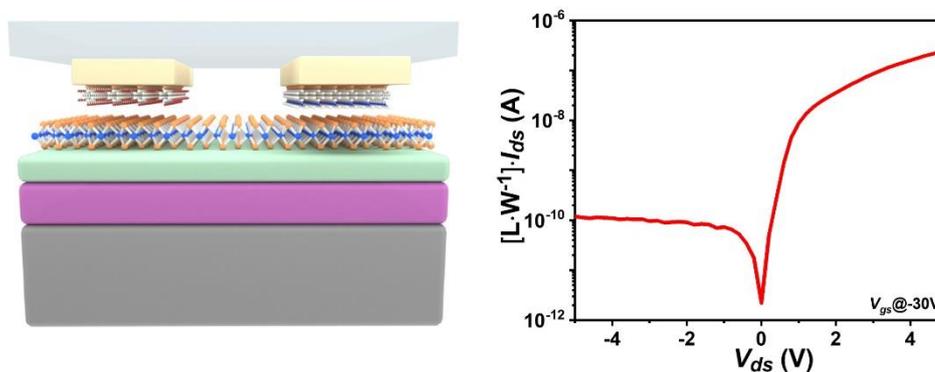


Figure II Schematic illustration of asymmetric MoS₂ FET device and semilogarithmic plot of the output curve at -30 V gate bias conditions. The drain electrode is PFBT functionalized electrode and the DABT functionalized electrode is grounded.

The 2nd project is focused on studying the influence of using self-assembled functionalized top-electrodes on the carrier injection in TMDs-based FET devices. A contact engineering approach was demonstrated to functionalize the electrodes for top-contact FETs configuration by transferring chemically pre-modified electrodes. Patterned electrodes were first prepared by thermal evaporation through a mask, and then the patterned electrodes were modified with self-assembly functionalization. Molecules with different dipole directions allowed us to adjust the work function (WF) of the Au electrode from 5.00 eV for bare electrode to 4.30 eV for (dimethylamino)benzenethiol (DABT) functionalized electrodes or 5.67 eV for 2,3,4,5,6-pentafluorobenzenethiol (PFBT) electrodes. By making use of dry-transfer technology, the functionalized electrodes were transferred onto a polydimethylsiloxane (PDMS) film surface, and then flipped and physically laminated on the TMDs surface to fabricate FETs with functionalized top-contact electrodes (see the FETs structure in Figure II). Our study shows that the electrodes pre-functionalized with electron-donating molecules can significantly improve device performance, with an average mobility as high as 30 cm² V⁻¹ s⁻¹ and a carrier injection barrier as low as 0.19 eV. However, the FETs with electrodes pre-functionalized with molecules containing electron-withdrawing groups can dramatically reduce device performance, with an average mobility

as low as $8.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and an injection barrier as high as 0.53 eV . Due to the advantage of van der Waals (vdW) contact between the electrode and the semiconductor, FLP is alleviated, with a pinning factor of 0.33 , which is much higher than the 0.1 for thermally evaporated electrodes. Furthermore, FETs with asymmetric functionalized electrodes was fabricated, i.e., Schottky diodes, by transferring electrodes pre-functionalized with different molecules (Figure II). The device shows an excellent rectification ratio (RR) more than 10^3 , which is attributed to the different injection barriers of the source-drain electrodes due to asymmetrical chemical functionalization of the electrodes on both sides (Figure II).

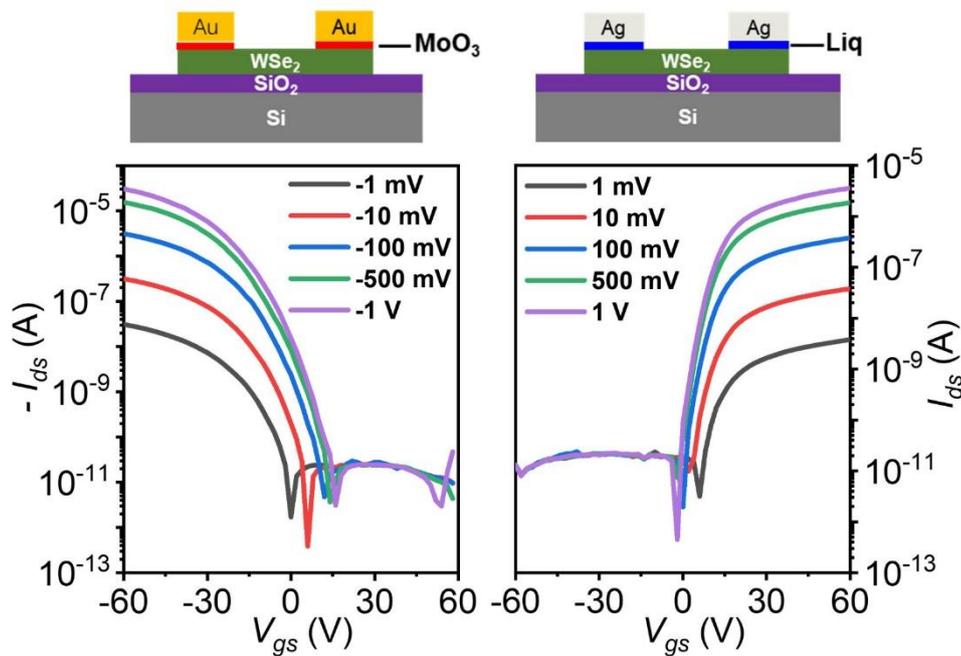


Figure III Schematic diagram of WSe₂ FETs with auxiliary layer functionalized electrodes vdW contact and their transfer curves.

The 3rd project is dedicated to the investigation of the impact of the functionalization of the electrode pre-added electron/hole injection auxiliary layer on the carrier type in TMDs-based FETs. The difference between the electrode interfaces obtained by the solvent-free dry transfer method and the conventional thermal evaporation method was characterized firstly. The solvent-free dry transfer electrodes can directly physically laminate the atomically flat interface onto the semiconductor to achieve vdW contact without any damage to the TMDs crystal. The dry transfer electrode technology was used to fabricate

FETs based on chemically vapor deposited (CVD) WSe₂ crystal with Au or Ag electrodes, respectively. Owing to the non-destructive interface of vdW contact, the FET device with Au-electrodes exhibit P-type dominant ambipolarity, while the FET device with Ag electrodes exhibit nearly balanced ambipolarity of electrons and holes. Then, the electrodes were functionalized by pre-adding electron/hole injection auxiliary layer during electrode preparation and then prepared patterned metal electrodes through mask and thermal evaporation approach. During electrode transfer, the auxiliary layer is laminated with the metal electrode onto the WSe₂ crystal surface, realizing vdW contact between the auxiliary layer and TMDs. The pre-functionalized gold electrode with a hole injection layer (HIL, molybdenum trioxide (MoO₃)) demonstrates exhibited unipolar P-type transport, and the electron carriers are significantly suppressed to disappear due to the higher WF of MoO₃ than 6 eV, which makes its Fermi level more matched with the valence band (VB) of WSe₂. In addition, the Ag electrode with an electron injection layer (EIL, 8-Quinolinolato lithium (Liq)) as the auxiliary layer exhibits unipolar N-type transport, and the hole carriers in the channel are suppressed to disappear due to the WF of Liq is closer to the conduction band (CB) of WSe₂, making electron injection more favorable. The results were verified using mechanically exfoliated few-layer WSe₂, and the same results were obtained (Figure III). Furthermore, metal-semiconductor-metal (MSM) diode was fabricated by transferring electrode with different auxiliary layer onto the same CVD-grown WSe₂ crystal surface, and demonstrated a RR of 10³. Finally, a logic inverter based on NMOS and PMOS WSe₂ FETs with a maximum gain of 1.73 at an input voltage of 5 V was demonstrated.

In this thesis, the functionalization of TMDs-based FETs is systematically studied, including the functionalization of the TMDs semiconductor and the functionalization of metal electrodes. Our work shows that functionalization of devices is a powerful approach that can be used to fabricate high-performance devices, including FETs, diodes, and logic inverters, etc. In particular, the functionalization of semiconductors shown unique potential for distinguishing isomers, while the functionalization of electrodes offers enormous opportunities for diodes and logic circuits. The device functionalization offers an unprecedented and powerful strategy to tune the properties of TMDs-based FETs and tailor

the device performance on demand. These results pave the way for the manufacture of integrated circuits based on 2D materials.

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Symbols and Abbreviations

● Symbols

Symbols	English
$^{\circ}\text{C}$	Degree celcius
Δn	Charge carrier density change
Φ_{CNL}	Charge neutrality level
Φ_{SB}	Schottky barrier
\AA	Ångström
C_i/C_{ox}	Capacitance of dielectric layer per unit area
e	Elementary charge
ϵ_{ox}	Dielectric constant of the dielectric layer
E_0	Vacuum energy level
E_F	Fermi energy
eV	Electronvolt
I_{ds}	Drain-source current
I_{off}	Off-state current of field-effect transistor
I_{on}	On-state current of field-effect transistor
J	Current density
k	Boltzmann constant
K	Degree Kelvin
L	Channel length
R_c	Contact resistance
S	Pinning factor
T	Temperature
t_{ox}	Thickness of dielectric layer

μ	Field-effect mobility
V	Volt
V_{ds}/V_{DS}	Drain-source voltage
V_{FB}	Flat-band voltage
V_{gs}/V_{GS}	Gate voltage
V_{th}	Threshold voltage
W	Channel width
W_f	Work function of (functionalized-) electrode
W_m	Work function of metal
W_s	Work function of semiconductor
χ	Electron affinity
X	Neutral exciton
X^-	Negative trion

● Abbreviations

1/2/3D	One/two/three-dimensional
26DFBT	2,6-Difluorobenzenethiol
35DFBT	3,5-Difluorobenzenethiol
AFM	Atomic force microscopy
AHAPS	N[3-(trimethoxysilyl)propyl]ethylenediamine
ALD	Atomic layer deposition
B.E.	Binding energy
BGBT	Bottom-gate bottom-contact
BGTC	Bottom-gate top-contact
BP	Black phosphorus
CA	Contact angle

CB	Conduction band
CMOS	Complementary metal oxide semiconductor
CVD	Chemical vapor deposition
CVT	Chemical vapor transport
DABT	(Dimethylamino)benzenethiol
DCB	Dichlorobenzene
DFT	Density functional theory
d-MoS ₂	Defective-contained molybdenum disulfide
EBL	Ebeam lithography
E _c	Conduction band energy
EGaIn	Eutectic gallium-indium
EIL	Electron injection layer
E _v	Valence band energy
F4TCNQ	2,3,5,6-Tetrafluoro-7,7,8,8- tetracyanoquinodimethane
FETs	Field-effect transistors
FLP	Fermi-level pinning
GAAFET	Gate-all-around field-effect transistors
Gr	Graphene
h-BN	Hexagonal boron nitride
HER	Hydrogen evolution reaction
HIL	Hole injection layer
HOMO	highest occupied molecular orbital
IPA	Isopropanol
ITO	Indium-tin-oxide
JFET	Junction field-effect transistor
K.E.	Kinetic energy
KPFM	Kelvin probe force microscopy

LB	Langmuir-Blodgett
LCs	Logic circuits
Liq	8-Quinolinolato lithium
MBCFET	Multi-bridge-channel field-effect transistors
MIGS	Metal-induced gap states
MoO ₃	Molybdenum trioxide
MoS ₂	Molybdenum disulfide
MOSFET	Metal-oxide-semiconductor field-effect transistors
MSM	metal-semiconductor-metal
NMOS	N-type metal oxide semiconductor
OFET	Organic field-effect transistor
OTMS	Octadecyltrimethoxysilane
OTS	Octadecyltrichlorosilane
PDMS	Polydimethylsiloxane
PESA	Photoelectron spectroscopy in ambient conditions
PFBT	2,3,4,5,6-Pentafluorobenzenethiol
PFS	Trichloro(1H,1H,2H,2H-perfluorooctyl)silane
PMOS	P-type metal oxide semiconductor
PL	Photoluminescence
PMMA	Poly(methyl methacrylate)
PS	Polystyrene
RR	Rectification ratio
R _{RMS}	Root-mean-square roughness
S/D	Source/drain
SAMs	Self-assembled monolayers
SB	Schottky barrier
SBH	Schottky barrier height

Symbols and Abbreviations

SEM	Scanning electron microscope
SS	Subthreshold slope/swing
STM	Scanning tunneling microscopy
TGBC	top-gate bottom-contact
TI	Topological insulator
TLM	Transfer length method
TMDs/TMDCs	Transition metal dichalcogenides
UPS	Ultraviolet photoelectron spectroscopy
UV	Ultraviolet
VB	Valence band
vdW	Van der Waals
VFET	Vertical field-effect transistors
V_s	Sulfur vacancy concentration
WF	Work function
WSe ₂	Tungsten diselenide
XPS	X-ray photoelectron spectroscopy

Chapter 1 Introduction

Semiconductors serve as the cornerstone of the electronics industry and underpin the advancements in information technology. Logic circuits, which utilize semiconductors as building blocks, are extensively employed across diverse fields, including information communication, computing, artificial intelligence, consumer electronics, and aerospace etc. The genesis of modern electronics can be traced back to a pivotal breakthrough achieved at Bell Labs in 1947, i.e. the invention of field-effect transistors (FETs)^[1]. In 1965, Intel's founder, Gordon Moore, posited the renowned Moore's Law, asserting that "the number of transistors in an integrated circuit approximately doubles every 18-24 months", which markedly propelled the growth of the semiconductor industry^[2]. Moore's Law dictates that the rapid strides in opto-electronics science and technology are primarily attributed to the extraordinary miniaturization of semiconductor devices, resulting in the continuous reduction in transistor size^[3; 4].

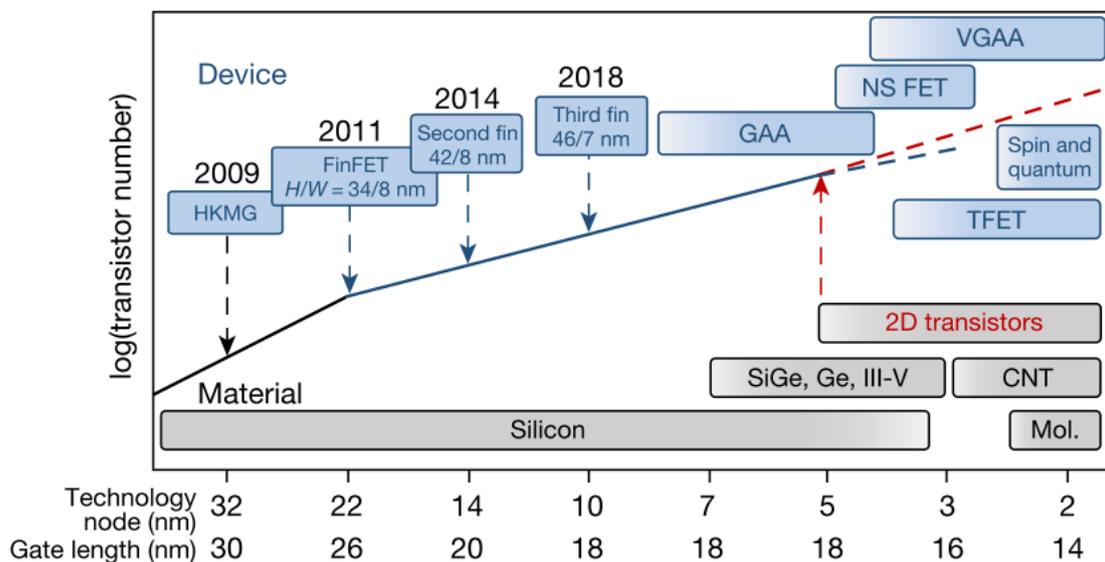


Figure 1.1 Trend of transistor scaling versus technology node and physical gate length.^[4]

At present, TSMC has declared the successful mass production of cutting-edge 5 nm transistors, and is progressing towards 3 nm dimensions. In fact, when the transistor size enters the 22 nm technology node (physical gate length), the original technology node

nomenclature loses its physical significance, becoming more of a "marketing slogan", with the actual physical gate length of transistors denoted by the same technology node differing among manufacturers. For instance, Intel's 10 nm node technology exhibits a physical gate length of approximately 18 nm and a fin width of around 7-8 nm, rendering it comparable to the 7 nm or even 5 nm nodes proclaimed by TSMC and Samsung.^[5]

The continuous shrinkage in the gate length necessitates a corresponding decrease in the thickness of the silicon-based semiconductor (or the fin width in FinFETs), and the performance of integrated chips is increasingly influenced by diminishing device dimensions. Such miniaturization poses numerous physical challenges, such as the limited scope for reducing semiconductor thickness, the significant impact of ultra-thin semiconductor surface roughness, the inevitable surface dangling bonds, particularly the short channel effect and quantum tunneling effect, etc.^[6-8] These factors contribute to severe leakage, heat generation, and carrier scattering in silicon-based FETs, which substantially degrade device performance, hinder the continuous scaling of transistors, and gravely jeopardize the operation of integrated chips^[9; 10]. Although the industry has now developed new configurations, such as FinFET^[3; 11], GAAFET (Gate-all-around FETs)^[12; 13], and MBCFET (multi-bridge-channel FETs)^[14; 15], to extend Moore's law, overcoming the aforementioned physical limitations remains challenging. Thus, exploring new semiconductor materials compatible with silicon-based processes and employing them as active components for fabricating high-performance optoelectronic devices is of paramount importance.

Two-dimensional (2D) materials have garnered considerable global interest in the quest for novel semiconductor materials. 2D materials comprise a class of ultrathin sheet-like crystals or films, wherein electrons can only move ballistically in two dimensions, while the remaining dimension is confined to materials at the atomic scale^[16]. Such 2D materials exhibit unique physical, chemical, and mechanical properties, which are absent in conventional bulk materials, making them interesting components for applications in

wearable smart electronics^[17], field-effect transistors (FETs)^[18], flexible memory devices^[19] and chemical sensors^[20], among others. Furthermore, the atomic thickness of 2D material represents the ultimate material thickness, rendering such class of materials the prototypical components for future integrated circuits scaled below 5 nm. Since Geim and Novoselov successfully fabricated single-layer graphene using mechanical exfoliation technology in 2004^[21], the 2D material family has expanded considerably, encompassing key systems such as transition metal dichalcogenides (TMDs)^[22], topological insulator (TI)^[23], hexagonal boron nitride (h-BN)^[24] and black phosphorus (BP)^[25], etc. Among these, TMDs have been extensively investigated as the most promising building block for next-generation semiconductor and optoelectronic semiconductor materials.

Despite significant progress has been achieved in TMDs particularly when integrated as active components, semiconducting layer, in FETs, a major challenge in 2D electronic devices consists in attaining high-performance with 2D materials which possess a high-stability, i.e., they do not deteriorate upon exposure to air because of high sensitivity to O₂, H₂O and CO₂^[26]. Some other challenges and opportunities for researchers to address in the future include i) exploring the multifunctional applications of semiconductor devices based on TMDs through molecular functionalization, taking advantage of the high sensitivity of ultrathin materials to environmental changes to enable highly sensitive and selective interaction with molecules. ii) reducing the carrier injection barrier and effectively enhancing device performance. The contact resistance between the electrode and TMDs semiconductors, as well as the mismatch between the conduction band (CB) or valence band (VB) of TMDs semiconductors and the work function of source-drain electrodes leads to suboptimal device performance, which greatly limits the application of TMDs-based FETs. iii) tuning the properties of TMDs-based FET devices, particularly the carrier type (polarity). Although this is an essential step for TMDs to advance towards large-scale integrated circuits in the future, such key issues are still open with no effective methods reported to date. To address these challenges, this thesis demonstrates how chemical functionalization, through defect engineering as well as interface optimizations, enables to

discriminate isomers and realize high performance and polarity regulated TMDs-based FET devices, thereby solved some key dilemmas in the field. This thesis is organized into the following 8 chapters:

Chapter 1 introduces the research background, scope and structure of the thesis.

Chapter 2 is focused on TMDs-based FET devices and introduces the readers to TMDs, TMDs-based FET devices, the factors affecting their performance and their applications.

Chapter 3 is dedicated to the TMDs-based functionalization method with self-assembled monolayers (SAMs). This section includes the introduction of the classification of SAMs, the kinetics of the self-assembly and factors affecting the self-assembly process, the main parameters to be considered in SAMs and their application in TMDs-based FET devices.

Chapter 4 presents the technical methodology and experimental characterization and testing techniques used in this thesis.

Chapter 5 demonstrates the new functions of TMDs in isomer discrimination through the TMDs chemical functionalization.

Chapter 6 establishes a general method for top-contact electrodes functionalization to achieve performance tuning of TMDs-based FETs.

Chapter 7 demonstrates the polarity tuning of TMDs-based FETs and its application in logic circuits by transferring the auxiliary layer functionalized electrodes through vdW integration strategy.

Chapter 8 summarizes the research content of the thesis and discusses the future perspectives of this field of science and technology.

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Chapter 2 Transition Metal Dichalcogenides (TMDs)-Based Field-Effect Transistors (FETs)

2.1 Introduction

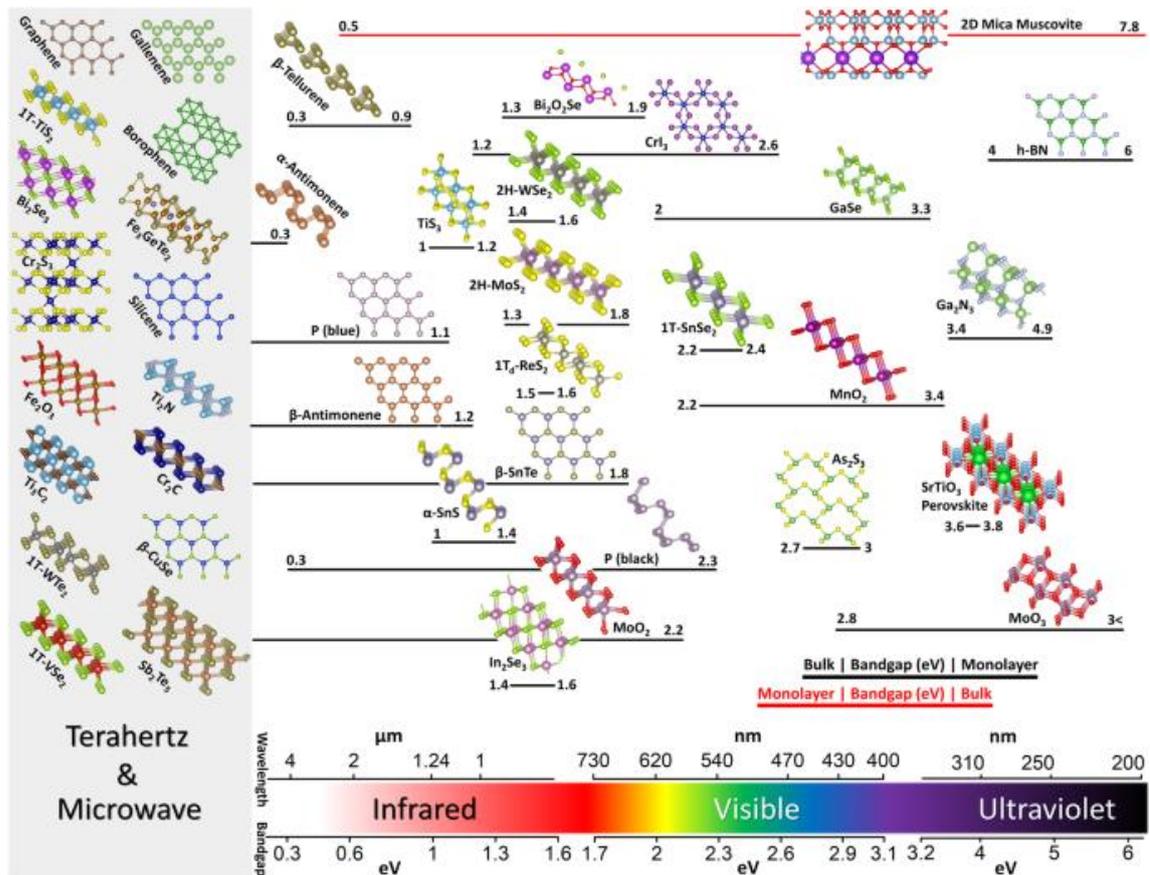


Figure 2.1 2D materials and their bandgaps and corresponding wavelengths.^[1]

Over the past two decades, the scientific community has witnessed the discovery and emergence of two-dimensional semiconductor (2D) materials that are establishing themselves as novel semiconductor materials holding unique physical and chemical properties, such as a sizeable band gap, high I_{on}/I_{off} ratio, relatively high mobilities, strong light interaction, excellent scalability, and immunity to short-channel effects. These materials are anticipated to replace or complement traditional silicon materials as key components in future integrated circuits below the 5 nm node.^[2-4] So far, as more ultra-thin materials have been developed, the 2D material family has been fully expanded.^[1; 5-8]

Figure 2.1 illustrates the 2D material family and their bandgaps with corresponding wavelengths. This thesis primarily focuses on transition metal dichalcogenides (TMDs), and this chapter will introduce the properties of TMDs and TMDs-based FETs.

2.2 Transition metal dichalcogenides (TMDs)

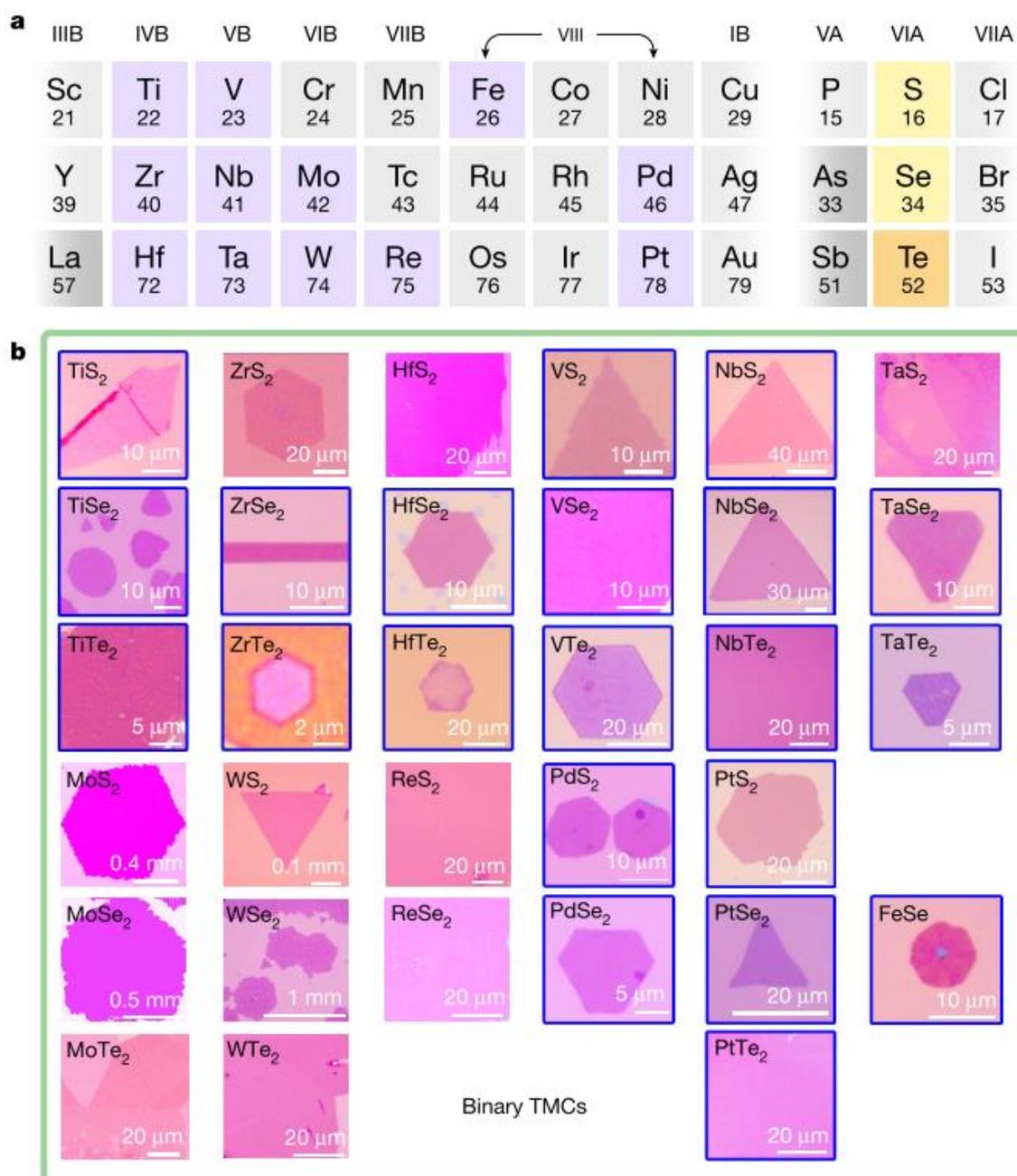


Figure 2.2 TMDs library. a) Transition metals and chalcogen elements in the periodic table. b) 32 TMDs and their optical images.^[9]

TMDs are the most extensively studied 2D materials, with layer-number-dependent

bandgaps that transition from bulk indirect to monolayer direct bandgaps. Generally, the chemical composition of TMDs is MX_2 , where M represents transition metals (highlighted in purple in Figure 2.2a) and X represents chalcogens (highlighted in yellow in Figure 2.2a). Optical images of the 32 TMDs composed of M and X permutations are displayed in Figure 2.2b.^[9] As some of these TMDs are unstable and challenging to prepare (particularly Nb, Pt, and Ti-based TMDs), the most commonly used TMDs are MoS_2 , due to its greater stability, WSe_2 , with its ambipolar system, and WS_2 , known for its outstanding photoluminescence properties. The TMDs employed in this thesis are MoS_2 and WSe_2 .

2.2.1 TMDs electronic structure

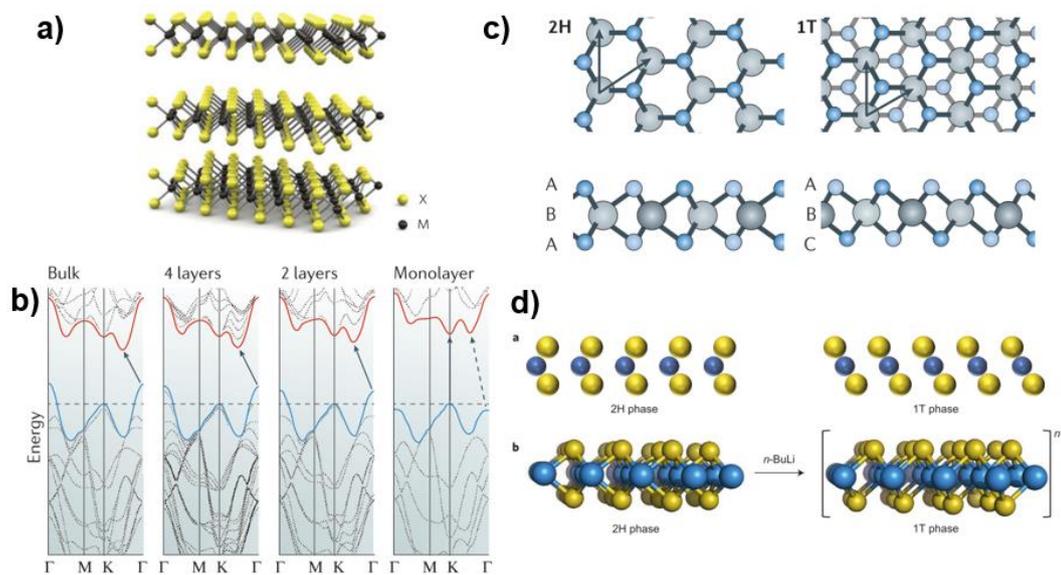


Figure 2.3 Electronic structure of TMDs. a) Layered structure of TMDs.^[5] b) Layer dependent bandgap. c) 2H and 1T phase of TMDs.^[10] d) Phase transition from 2H to 1T.^[11]

Since TMDs have a layered structure and their bandgaps are layer-dependent, such as, there is a bandgap transition from indirect for bulk of 1.3 eV to direct for monolayer of 1.8 eV for MoS_2 (Figure 2.3a and b).^[5] Due to the varying coordination of the transition metal atoms, TMDs exist in different structural phases. For instance, MoS_2 commonly occurs in trigonal prismatic (2H) and distorted octahedral (1T) phases, as illustrated in Figure 2.3c.^[11; 12] The 2H phase of MoS_2 is the most thermodynamically stable and serves as a suitable semiconductor material for semiconductor devices, while the 1T phase is a metallic phase utilized for the hydrogen evolution reaction (HER).^[10] It has been reported that MoS_2 can be transformed from 2H phase to 1T phase through n-BuLi solution treatment,^[11] as

depicted in Figure 2.3d, whereas reversibility to the 2H phase can be attained upon high temperature treatment^[13]. Because of our interest in exploiting their semiconducting nature, all TMDs used in this thesis are 2H phase crystals.

2.2.2 TMDs optical and optoelectronic properties

TMDs possess exceptional optical and optoelectronic properties, making them popular choices for photodetectors and light-emitting devices. Figure 2.4a displays the three Raman vibration modes of bulk MoS₂, with E¹_{2g} and A_{1g} modes observed near 400 cm⁻¹.^[5] The in-plane E¹_{2g} mode results from the opposite vibration of two S atoms relative to the Mo atom, while the A_{1g} mode is associated with the out-of-plane vibrations of the S atoms in opposite directions.^[14] Furthermore, the Raman spectra of TMDs exhibit a clear thickness dependence, as shown in Figure 2.4b and c. As the thickness of MoS₂ increases, so does the frequency difference between these two modes.^[15] Consequently, the Raman spectrum can be employed to identify the thickness of the TMDs crystal.^[14]

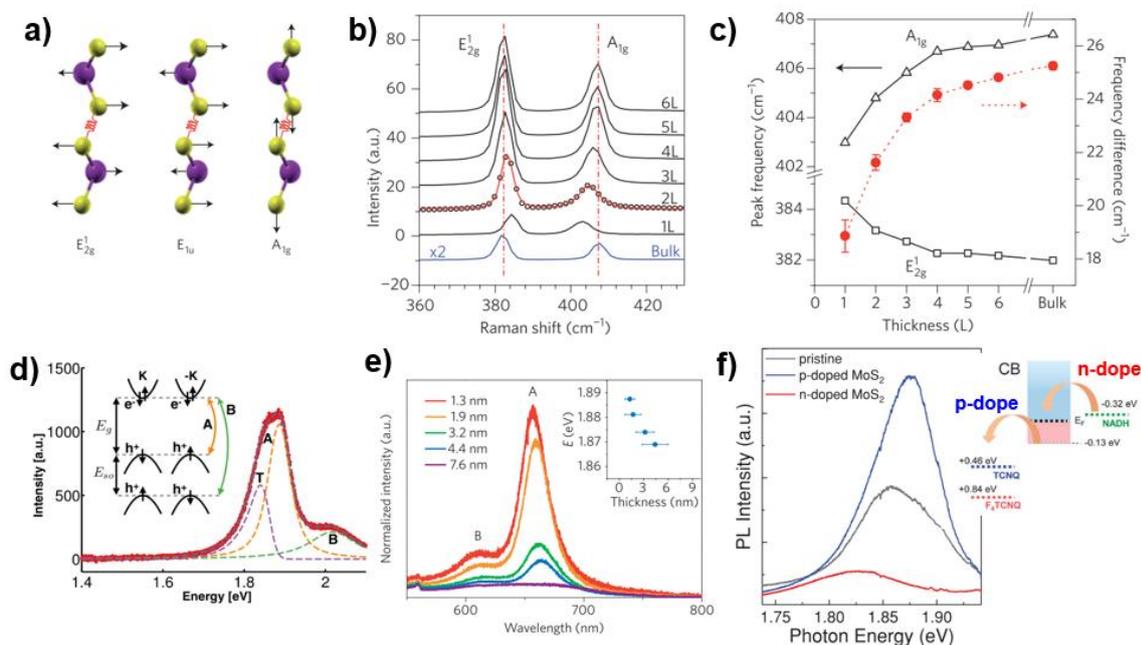


Figure 2.4 Spectrum of TMDs. a) Raman active mode of MoS₂.^[5] b) Layered dependent Raman spectra of MoS₂. c) The frequency of E¹_{2g} and A_{1g} modes and their difference as a function of layer thickness. d) PL spectrum of MoS₂ at RT. A and B denote excitons, and T denotes the trion.^[16] e) Layered dependent PL spectra of MoS₂.^[13] f) Effect and mechanism of doping on MoS₂ PL.^[17; 18]

The 2D ultrathin feature of TMDs reduces the dielectric screening, leading to the generation

of strong interactions and many-body states, such as trions and excitons.^[5] Excitons are Coulomb interacted electron-hole pairs, while trions are formed through the combination of electrons or holes with excitons. Figure 2.4d presents the photoluminescence (PL) spectra of MoS₂ corresponding to the two main peaks of the exciton band, i.e. A and B, which relate to the direct-gap transitions of the Brillouin zone between the maximum of the split VB and the minimum of the CB at the K-point.^[16] The B peak is an exciton peak, and the A peak comprises an exciton and a negatively charged trion peak. Compared to MoSe₂ and WSe₂ (whose PL peak contains excitons and positively and negatively charged trions), the positively charged trion is not observed in PL peak of MoS₂, which is due to the higher electron density of its body. It has been discovered that as the thickness of MoS₂ decreases to a monolayer, the PL intensifies, which can be explained by the direct gap of monolayer MoS₂.^[13] Moreover, the transition from indirect^[13] to direct bandgap leads to an enhancement of PL quantum yield by $\sim 10^4$ (Figure 2.4e). These optoelectronic features render TMDs extremely promising for light-matter interaction devices, such as photovoltaics, light-emitting devices, and photodetectors. Additionally, the high surface-to-volume ratio of TMDs makes them particularly sensitive to surrounding environment changes. When adsorbates are present on the TMDs surface or the environment alters, TMDs experience changes like charge transfer and doping (Figure 2.4f), which can be detected by shifts in Raman or PL spectra or by combining TMDs into FETs to measure changes in electrical signals. This opens the door for TMDs in molecular functionalization and sensors.^[5; 17; 18]

2.2.3 Defects in TMDs

Theoretical analyses reveal that the experimentally measured optical and electrical behaviors of TMDs are not fully consistent with those of perfect crystals, such as discrepancies between PL spectra and calculated results of perfect crystal structures, and the difference between the n-type and p-type behaviors of TMD devices etc.^[19; 20] These findings suggest that the prepared TMDs are not perfect crystals, but rather contain some structural defects.^[21] The most common defects in TMDs are vacancy defects and dislocation defects. Figure 2.5 showcases six types of defects in TMDs, including single

sulfur vacancy (V_S), disulfide vacancy (V_{S_2}), vacancy of Mo atom and bonded three S atom (V_{MoS_3}), vacancy of Mo atom and bonded all S atoms (V_{MoS_6}), one Mo occupying two S sites (Mo_{S_2}), two S atoms occupying one Mo site (S_{2Mo}).^[22] Among these, V_S defects are the most common due to their lowest formation energy.^[23] Understanding and addressing these defects in TMDs is crucial for optimizing their performance in various optoelectronic applications.

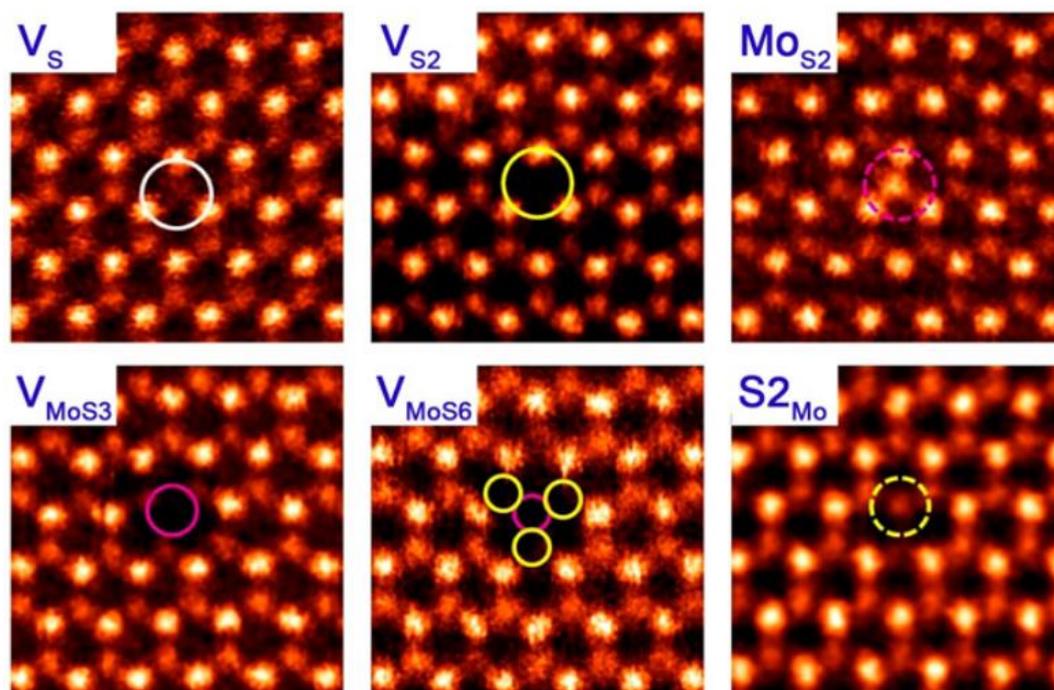


Figure 2.5 High-resolution images of different defect types in TMDs. (Atomic resolution annular dark field (ADF) image of MoS_2 defects)^[22]

Defect engineering of TMDs, such as sulfur vacancies (V_S), has emerged as a viable strategy to modulate their optical and electrical properties, including regulating PL intensity^[20; 24], enhancing catalytic HER^[25; 26], and controlling carrier mobility^[27], etc. Several methods have been developed to artificially create defects in TMDs, including high-temperature thermal annealing^[28; 29], ion irradiation/bombardment^[28; 30; 31], electron irradiation^[32], and plasma treatments^[33; 34], etc. Furthermore, the literature demonstrates that defects in TMDs can be covalently bonded to thiol-containing molecules, which can repair defects and enable multifunctionalization of TMDs (see Figure 2.6), such as doping, as described in section 3.5.3.^[35; 36] In this thesis, we also employ this method to artificially

create defects and covalently link thiol-containing isomers for isomer identification.

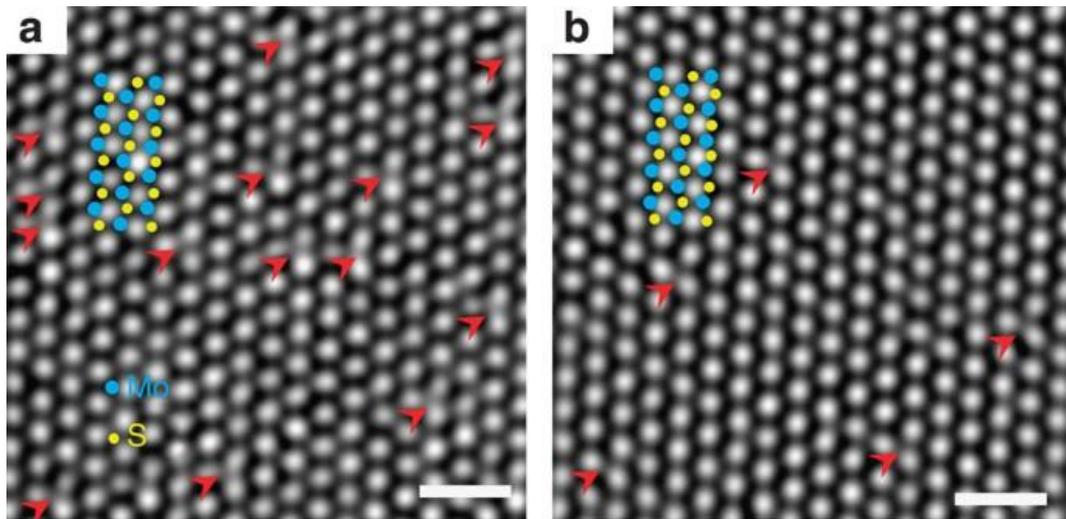


Figure 2.6 STM images of monolayer MoS₂ before and after thiol repair.^[35]

2.3 TMDs-based FETs

Field-effect transistors (FETs or FET) were first proposed by Julius in 1930^[37] and are based on the principle of regulating carrier concentration in a semiconductor via an applied external electric field, which in turn controls the magnitude of the current flowing through the semiconductor. In 1947, Shockley et al.^[38] of Bell Labs first fabricated a junction field-effect transistor (JFET), and in 1960, Kahng et al.^[39] of Bell Labs invented a metal-oxide-semiconductor field-effect transistor (MOSFET) to replace JFET. MOSFETs have since become the basic unit of integrated circuits, ushering in the semiconductor chip era. However, according to Moore's Law, silicon-based transistors now face a bottleneck, as it is challenging to continue advancements at the 3-5 nm scale.^[40-42]

As previously introduced, 2D materials, and in particular TMDs, are promising candidates for next-generation semiconductor materials due to their exceptional optical and electrical properties, as well as the dangling bonds-free surface. These properties offer significant advantages and potential especially in FETs and devices composed of FETs, such as logic circuits, flexible circuits, and memories, etc. In 2011, Kis et al.^[43] first reported a top-gate transistor based on monolayer MoS₂ with a switching ratio exceeding 10⁸ and a mobility beyond 200 cm²V⁻¹s⁻¹ when using a 30 nm high-k dielectric material, HfO₂, as the top

dielectric layer. Additionally, its excellent optical properties enable TMDs to play a crucial role in optoelectronic device research, and their atomically thin, ultrasensitive surface allows for substantial potential in molecular functionalization^[5]. For example, in 2012, Zhang et al.^[44] reported the potential of MoS₂ for photodetectors, and Makarova et al.^[45] discussed the potential of MoS₂ for molecular functionalization. Consequently, TMDs-based FETs attracted considerable attention in the context of beyond Moore's law and the advancement of integrated circuits.

In this thesis, we focus on FETs, the core building block of integrated circuits, and study their performance enhancement and regulation through functionalization. Subsequently, we will introduce the structure and working principle, main parameters, factors affecting performance and applications of TMDs-based FETs based on the research progress in this field.

2.3.1 Structure of TMDs-based FETs

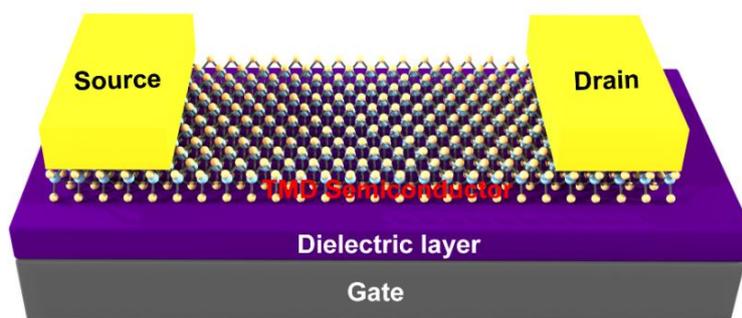


Figure 2.7 Typical TMDs-based FET device 3D structure.

FETs primarily consist of electrodes (source electrode (S), drain electrode (D), and gate electrode (G)), a dielectric layer, and TMDs semiconductor. Figure 2.7 illustrates a three-dimensional (3D) structure of typical TMDs-based FETs. Conventionally, planar FETs can be classified into four configurations, as displayed in figure 2.8a-d, which are distinguished by their geometry. These configurations include bottom-gate top-contact (BGTC), top-gate top-contact (TGTC), bottom-gate bottom-contact (BGBT), and top-gate bottom-contact (TGBC). In addition to planar configuration, a vertical configuration (VFET, figure 2.8e) exists. These architectures resemble those employed in organic field-effect transistor

(OFET). Furthermore, due to the unique structure of TMDs, a distinct configuration arises, that is, edge-contact of TMDs semiconductor (Figure 2.8f). Different configurations greatly influence device performance. The majority of research focuses on the BGTC configuration because of its ease of preparation and effective carrier injection. However, as the bottom electrode configuration involves the mechanical transfer of TMDs and exhibits less effective carrier injection than the top electrode configuration, yielding large contact resistances^[46-51], its overall performance is not optimal and is typically used only for functional modification of the electrode.

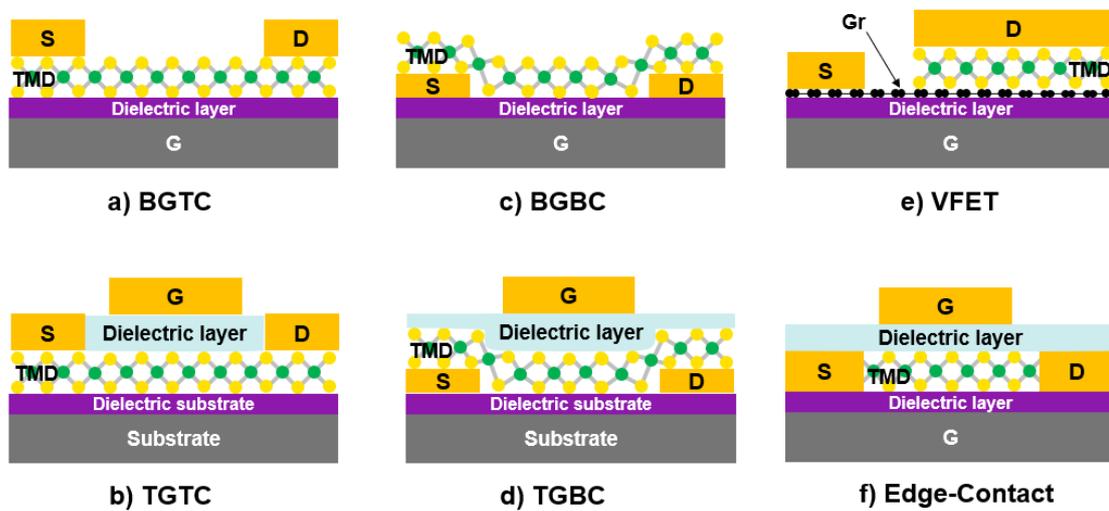


Figure 2.8 Schematic diagram of TMDs-based FET devices structure. a) bottom-gate top-contact (BGTC). b) top-gate top-contact (TGTC). c) bottom-gate bottom-contact (BGBC). d) top-gate bottom-contact (TGBC). e) vertical FETs (VFET). f) edge-contact FET.

In the top-gate configuration, the gate is positioned above the semiconductor and dielectric layer, often resulting in exceptional carrier mobilities, particularly when high-k dielectric materials are utilized. Nonetheless, the absence of dangling bonds on the TMDs surface can cause inhomogeneous dielectric layer growth during atomic layer deposition (ALD), limiting FETs contact performance.^[52] In 2022, Duan et al. reported a method to fabricate top-gate FET devices by transferring the electrodes of integrated dielectric layer, further expanding this configuration.^[53] Owing to the atomic-level thickness of TMDs, the tunneling leakage current between source and drain electrode is larger in the VFET configuration, making it less frequently reported.^[54] In 2021, Liu et al. described monolayer

TMDs-based VFETs with conducting channels under 1 nm, prepared by transfer electrodes.^[55] Compared to top-contact and bottom-contact TMDs, one-dimensional (1D) edge contacts can generate orbital overlap at the TMDs/metal electrode interface due to the presence of dangling bonds at the TMDs edge, facilitating carrier injection by lowering the injection barrier.^[56-63]

It is important to note that, due to the small size of mechanically exfoliated TMDs crystals (approximately 10 μm), the electrode size in the widely used BGTC configuration generally exceeds that of TMDs, resulting in a mixed contact of top and edge contact in this configuration. All devices in this thesis are based on the BGTC configuration.

2.3.2 Working principle of TMDs-based FETs

To comprehend FET operation, it is crucial to first understand what happens when semiconductor and metal electrodes come into contact. Assume a metal electrode (e.g., Au) contacts an n-type semiconductor (e.g., MoS₂), with $W_m > W_s$. Before contact, they share the same vacuum energy level (E_0), as shown in Figure 2.9a. Now envision connecting them with a wire while still distant. Since $(E_F)_s$ is higher than $(E_F)_m$, electrons in the semiconductor flow to the metal electrode. As a result, the metal electrode surface becomes negatively charged, and the semiconductor surface is positively charged with the same charge amount. This leads to a decrease in the electrode potential and an increase in semiconductor potential until their Fermi levels align and the system reaches equilibrium, as illustrated in Figure 2.9b.

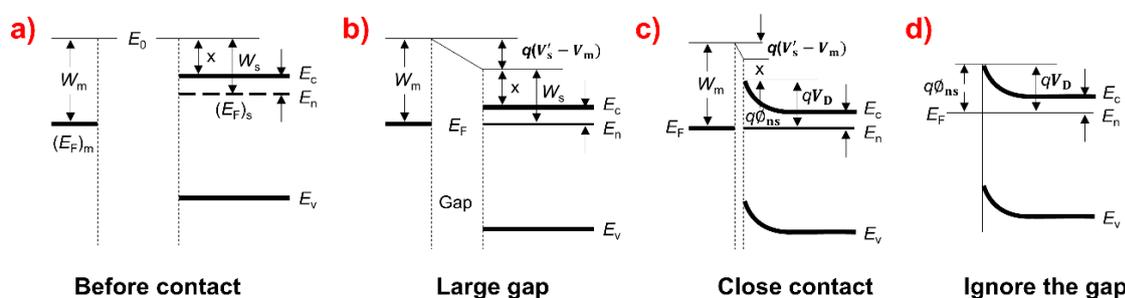


Figure 2.9 The energy band diagram of a metal electrode in contact with an n-type semiconductor, and $W_m > W_s$.

Now, let us consider the scenario where the distance between the electrode and the semiconductor decreases. As the distance decreases, the positive charge density on the semiconductor surface near the metal electrode side increases and is distributed within the surface layer of the semiconductor. This creates a positive space charge region with the electric field direction pointing from the semiconductor's interior to its surface, raising the surface electron energy of the semiconductor compared to the interior, and consequently bending the semiconductor's energy band, as shown in Figure 2.9c. However, for simplifying theoretical analysis, the ideal simplified model is typically considered, in which the gap between the electrode and the semiconductor is disregarded, and the potential decay and contact potential difference between them are not considered, as shown in Figure 2.9d. The difference between the conduction band edge (CB) of the semiconductor and the Fermi level of the electrode constitutes the Schottky barrier (SB, Φ_{SB}).

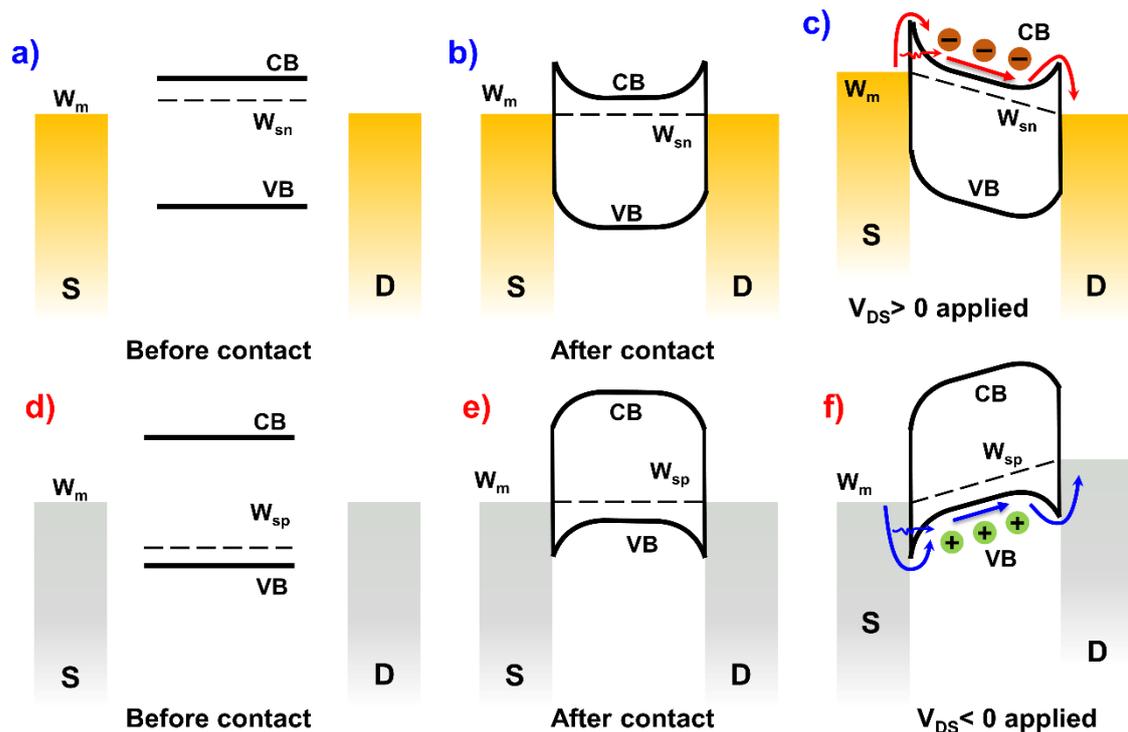


Figure 2.10 Band diagram of the working principle of unipolar FETs. a–c) FETs consist of metal electrodes and an n-type semiconductor, and $W_m > W_{sn}$. d–f) FETs consist of metal electrodes and a p-type semiconductor, $W_m < W_{sp}$. S/D on behalf of source and drain electrode, respectively. The arrows represent the different injection mechanisms. Solid line with arrow: thermionic emission. Waved line with arrow: field emission (tunneling).

Now let's consider the case of FETs, figures 2.10a-c display the case of metal electrodes contacting an n-type semiconductor, with $W_m > W_s$, similar to figure 2.9. Before contact, their energy levels are depicted in Figure 2.10a. Following contact, energy band bending occurs at the source (S) and drain (D) electrode contact locations within the semiconductor (Figure 2.10b). When a small positive bias voltage (V_{DS}) is applied, a potential difference arises on both sides of the S/D electrode, driving electrons to be injected directionally from the S electrode into the semiconductor and collected by the D electrode, as demonstrated in Figure 2.10c. If the semiconductor exhibits poor conductivity (larger gap or Fermi level far from the energy band edge), fewer internal carriers available, and the device remains in the off state without charge flow. Upon applying a negative gate voltage (V_{GS}), electrons are repelled from the interface between the semiconductor and the dielectric layer, establishing a depletion layer that drives the semiconductor energy band rise, further increasing the SB and reducing the carrier concentration. Further increasing negative V_{GS} may create an inversion channel, facilitating the high mobilities. Conversely, when a positive V_{GS} is applied, negative charges are attracted to the interface between the semiconductor and the dielectric layer, generating an accumulation of electrons in the conduction band, driving the semiconductor energy band drop, further reducing the SB and increasing the carrier concentration. When the applied gate voltage flattens the semiconductor's energy band, i.e., the energy band is no longer bent, the V_{GS} at this point is termed the flat-band voltage (V_{FB}).

For TMDs such as MoS_2 , the threshold voltage (V_{th}) is not at 0 V because the Fermi energy level is close to the CB edge, carriers exist within the semiconductor, and conductivity is high, so when $V_{GS} = 0$ V, the device may still have carriers to flow. This also related to the dielectric layer material, gate electrode materials, and other factors, necessitating a comprehensive consideration. For 2D materials with atomic-level thickness, the gate voltage modulation on the semiconductor at the interface (space charge region) can be transformed into the modulation of the entire 2D material, rendering the gate modulation more robust compared to conventional semiconductor materials.

For P-type semiconductors, the situation is analogous. The energy band diagram of $W_m <$

W_{sp} is shown in Figure 2.10d-f. Negative V_{GS} leads to the formation of hole multi-carrier accumulation, while positive V_{GS} results in minority carrier accumulation.

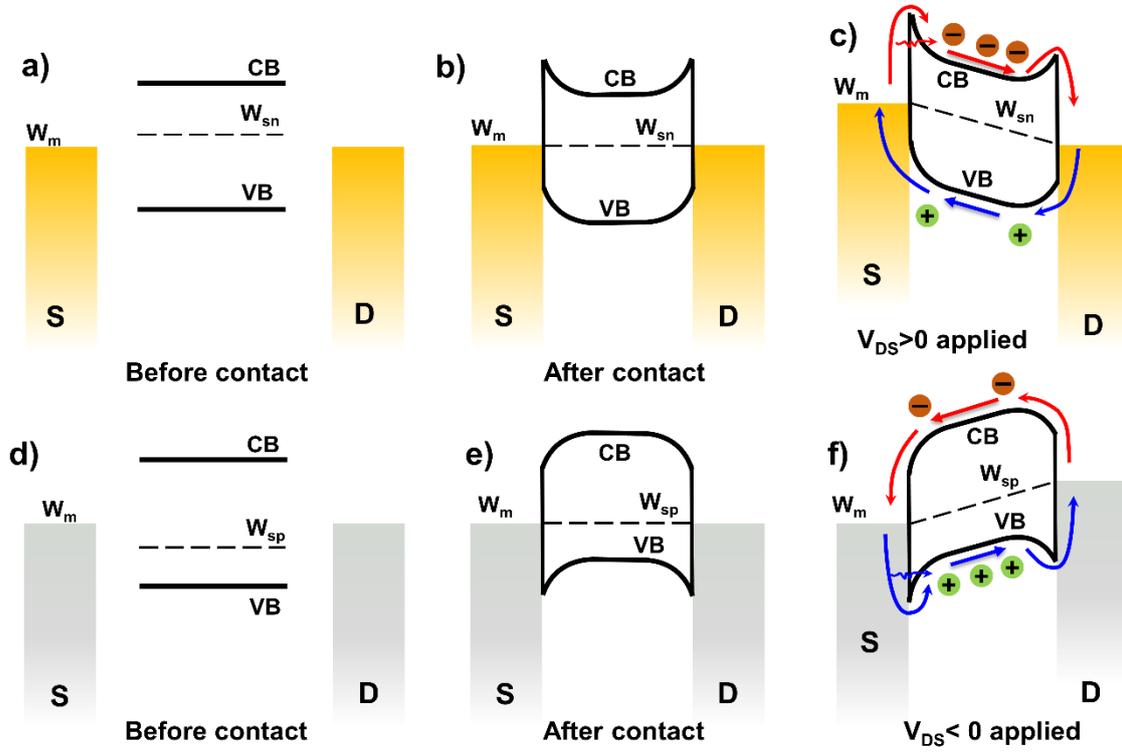


Figure 2.11 Band diagram of the working principle of ambipolar FETs. a–c) FETs consist of metal electrodes and an n-type dominant ambipolar semiconductor, and $W_m > W_{sn}$. a–c) FETs consist of metal electrodes and a p-type dominant ambipolar semiconductor, $W_m < W_{sp}$. S/D on behalf of source and drain electrode, respectively.

For ambipolar semiconductor materials (e.g., WSe_2), since the Fermi level is close to the middle of CB and VB, the semiconductor combines both electron transport and hole transport. The energy band change is similar to that of unipolar semiconductors. We present two scenarios illustrating the working principles of FETs composed of metal electrodes in contact with n-type dominant ambipolar semiconductors (figure 2.11a-c, $W_m > W_{sn}$) and p-type dominant ambipolar semiconductors (figure 2.11d-f, $W_m < W_{sp}$), respectively.

For n-type dominant ambipolar semiconductors (Figure 2.11a-c), the Fermi level is closer to the conduction band edge. Before contact, the energy levels are shown in Figure 2.11a. After contact, energy band bending occurs at the source and drain electrode contact locations within the semiconductor (Figure 2.11b). A small V_{DS} ($V_{DS} > 0$) causes a

simultaneous flow of electrons and holes. When a positive gate voltage is applied ($V_{DS} > 0$), the electron SBH decreases, and the device operates in an n-type mode (Figure 2.11c). In this mode, electrons are the majority carriers, and their concentration increases with increasing positive gate voltage. When a large negative gate voltage is applied ($V_{DS} > 0$), the electron SBH increases and the hole SBH decreases, the device operates in a p-type mode.

Similarly, for p-type dominant ambipolar semiconductors (Figure 2.11d-f), the Fermi level is closer to the valence band edge. Before contact, the energy levels are depicted in Figure 2.11d. Following contact, energy band bending occurs at the source and drain electrode contact locations within the semiconductor (Figure 2.11e). When a negative gate voltage is applied ($V_{DS} < 0$), the hole SBH decreases and the electron SBH increases, and the device operates in a p-type mode (Figure 2.11f). In this mode, holes are the majority carriers, and their concentration increases with increasing negative gate voltage. When a large positive gate voltage is applied ($V_{DS} > 0$), the device operates in an n-type mode.

In summary, the operation of FETs based on ambipolar semiconductor materials, such as WSe₂, depends on the applied gate voltage, which modulates the energy band structure and carrier concentrations. By controlling the gate voltage, it is possible to tune the transport properties and switch between n-type and p-type operation modes, enabling a wide range of applications in electronic devices.

2.3.3 The main parameters of TMDs-based FETs

2.3.3.1 Transfer curve, output curve and threshold voltage

The properties of the FETs were characterized by electrical measurements. Figure 2.12 displays the transfer and output curves of TMDs-based FETs. When $V_{GS} < V_{th}$, the device is off, and the device turns on when $V_{GS} > V_{th}$ (V_{th} represents threshold voltage). When the device is turned on and V_{GS} is fixed, if $V_{DS} < |V_{GS} - V_{th}|$, the FETs operate in the linear region, wherein the semiconductor channel is analogous to a resistor, and the I_{DS} is proportional to the V_{DS} . The current in the channel can be described by:

$$I_{DS} = \frac{W}{L} \mu C_i (V_{GS} - V_{th}) V_{DS} \quad (2 - 1)$$

Where, W is the channel width, μ is the linear mobility, C_i is the capacitance of dielectric layer per unit area. When $V_{DS} > |V_{GS} - V_{th}|$, the FETs operate in the saturation region. As V_{DS} increases, I_{DS} reaches saturation and does not increase further. The current in the channel can be described by:

$$I_{DS} = \frac{W}{2L} \mu C_i (V_{GS} - V_{th})^2 \quad (2 - 2)$$

Where, μ is the saturation mobility.

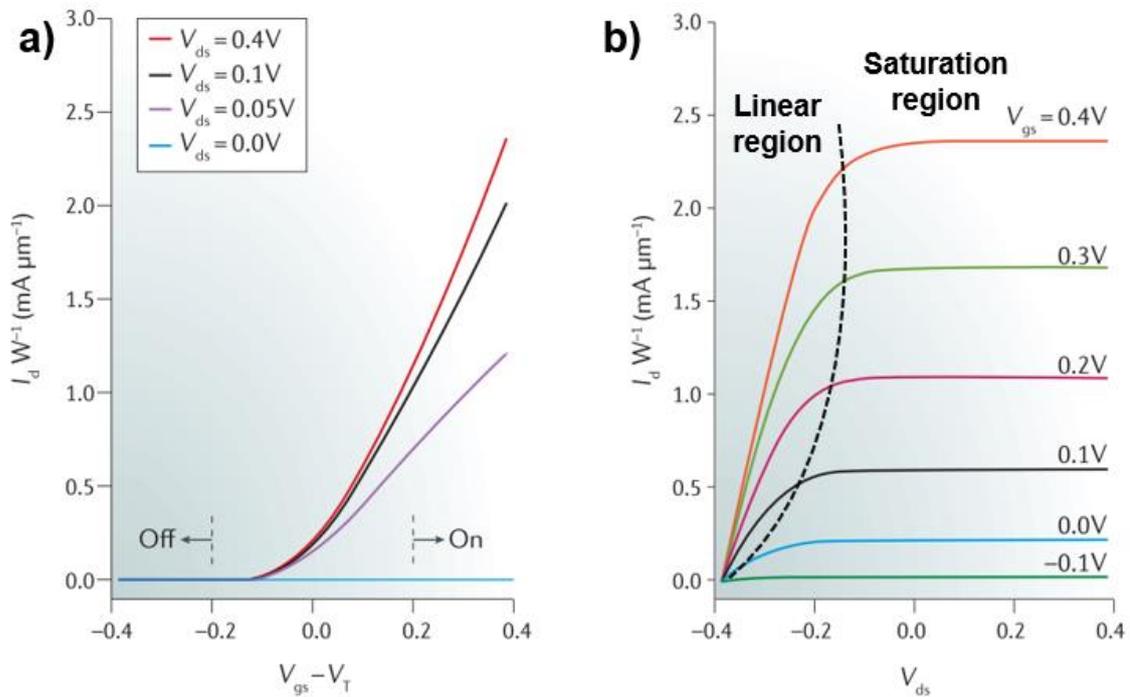


Figure 2.12 Transfer curves and output curves of TMDs-based FETs.^[3]

TMDs-based FETs with BGBC configuration generally operate in the linear region. In this thesis, all devices operate in the linear region.

2.3.3.2 Mobility

Mobility (μ) represents the rate of carrier drift per unit electric field; it is one of the most important key performance indicators in FETs, with unit is $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. Mobility is typically calculated from the transfer curve, but the calculation formula differs when the device operates in various regions.

When the device operates in the linear region, the mobility can be obtained from the linear

fitting of transfer curve according to formula 2-1:

$$\mu = \frac{L}{WC_i V_{DS}} \cdot \frac{\partial I_{DS}}{\partial V_{GS}} \quad (2-3)$$

When the device is operating in the saturation region, according to formula 2-2,

$$\sqrt{I_{DS}} = \sqrt{\frac{WC_i}{2L}} \mu (V_{GS} - V_{th}) \quad (2-4)$$

Therefore, the saturation mobility can be obtained from the linear fitting of $\sqrt{I_{DS}} - V_{GS}$ curve:

$$\mu = \frac{2L}{WC_i} \left(\frac{\partial \sqrt{I_{DS}}}{\partial V_{GS}} \right)^2 \quad (2-5)$$

The mobility in this thesis is calculated by formula 2-3 in the linear region.

2.3.3.3 On/off ratio

The on/off (I_{on}/I_{off}) ratio is defined as the ratio of the I_{DS} of FETs in the on-state to that in the off-state. The gate control generates on-state and off-state in FETs, which correspond to “0” and “1” in binary. Consequently, the I_{on}/I_{off} ratio directly determines whether FETs can be used in logic circuits (generally higher than 10^6). A favorable I_{on}/I_{off} ratio indicates that the FET possesses high stability and immunity to interference, which is crucial for logic circuits. It has been reported that the I_{on}/I_{off} ratio of FETs based on monolayer MoS_2 can reach up to 10^{10} .^[64]

2.3.3.4 Subthreshold slope

Subthreshold slope (SS) represents the switching speed of FETs from the off state to the on state, and its unit is mV/dec. It is defined as

$$SS = \frac{dV_{GS}}{d(\lg I_{DS})} \quad (2-6)$$

Generally, the smaller the SS value, the faster the switching speed of the device from the off state to the on state. The theoretical limit of SS is 60 mV/dec.

2.3.3.5 Contact resistance

The contact resistance (R_c) refers to the resistance value at the contact interface between the metal electrode and the semiconductor in FETs. The contact between metal electrodes and TMDs is mainly categorized as ohmic contact and Schottky contact, with different contact types significantly impacting the device performance. R_c is primarily measured using the transfer length method (TLM), four-probe method, Kelvin probe force microscopy method (KPFM), and Y-function method.

2.3.4 Charge transport mechanism in TMDs-based FETs

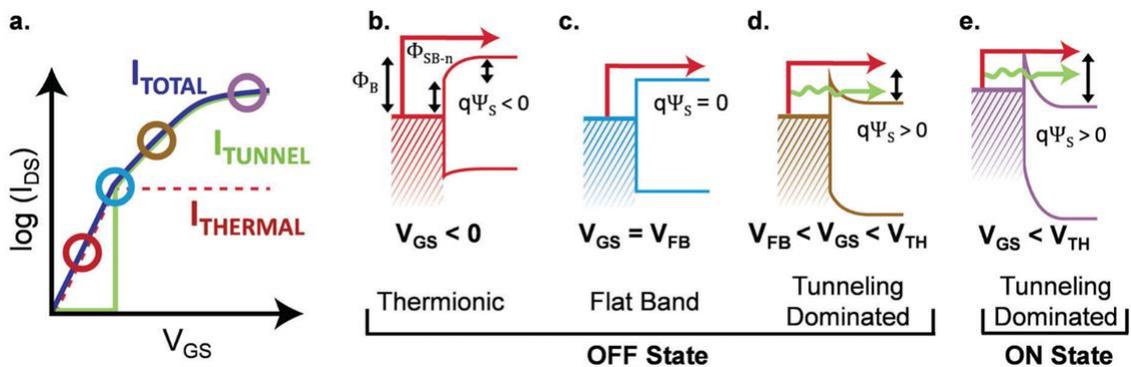


Figure 2.13 Charge transport mechanism in TMDs-based FETs. a) transfer curve with various transport mechanism region. b) thermionic region. c) flat band condition. d-e) tunneling dominated region.^[65]

The typical charge transport mechanism of TMDs-based FETs is depicted in Figure 2-13, which usually involves thermionic emission and thermally assisted tunneling. For example, for FETs comprising metal and n-type semiconductor ($W_m > W_{sn}$) as shown in figure 2.10 in Section 2.3.2. When $V_{GS} < V_{FP}$, the charge transport mechanism is thermionic emission. When $V_{FP} < V_{GS} < V_{th}$, the device remains in the off state, and the charge transport mechanism is dominated by thermally assisted tunneling. When $V_{GS} > V_{th}$, the device is in the on state, and the charge transport mechanism is dominated by tunneling.^[65]

2.4 Factors affecting TMDs-based FETs performance

2.4.1 Electrode engineering

The energy difference between the Fermi level of the metal and the energy band (CB or VB) of the semiconductor determines the Schottky barrier height (SBH). Therefore, selecting a metal material with an appropriate WF can reduce the injection barrier. Figure 2.14 presents the energy band alignment of various TMDs materials and metal electrodes. For example, Duan et al.^[66] utilized a Ni/Au alloy as the electrode to prepare high-performance MoS₂ FET devices. Das et al.^[67] fabricated MoS₂ FETs with mobility exceeding 700 cm² V⁻¹ s⁻¹ using scandium (Sc) as the electrodes. Furthermore, low WF metal like In^[68], Bi^[69] and Sb^[70] have been reported to prepare high-performance MoS₂ FETs.

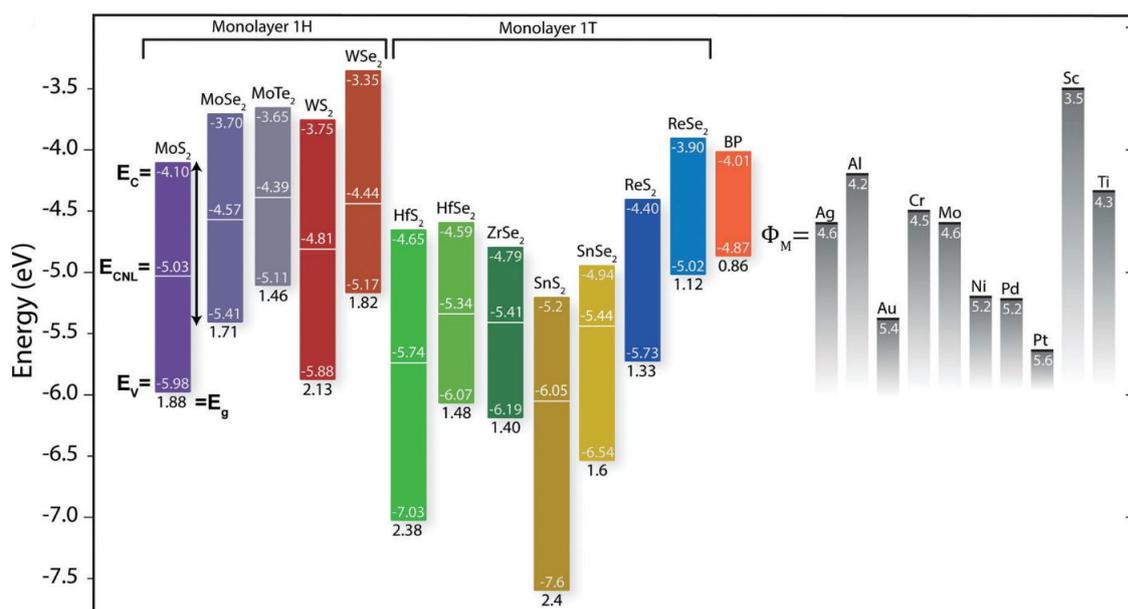


Figure 2.14 Band alignment of various TMDs materials and metal electrode contact metals.^[65]

2.4.2 Fermi level pinning (FLP)

Although metals with optimized WF can be chosen to minimize the SBH of FETs, severe Fermi level pinning (FLP) of TMDs to metal electrodes has been reported, resulting in limited effectiveness of this approach.^[71] It has been reported that, regardless of the contact metal used, MoS₂ FETs exhibit n-type behavior, and the Fermi levels of Sc, Ti, Ni, and Pt

are all pinned near the CB of MoS₂, corresponding to a pinning factor of $S \sim 0.1$, as shown in figure 2.15^[72]. In the case of WSe₂, the Fermi level is closer to the middle of the bandgap. Despite using high WF electrodes of Ni and Pd (5.2 eV), which theoretically align with VB of WSe₂, neither forms a p-type contact, and both exhibit ambipolarity^[73].

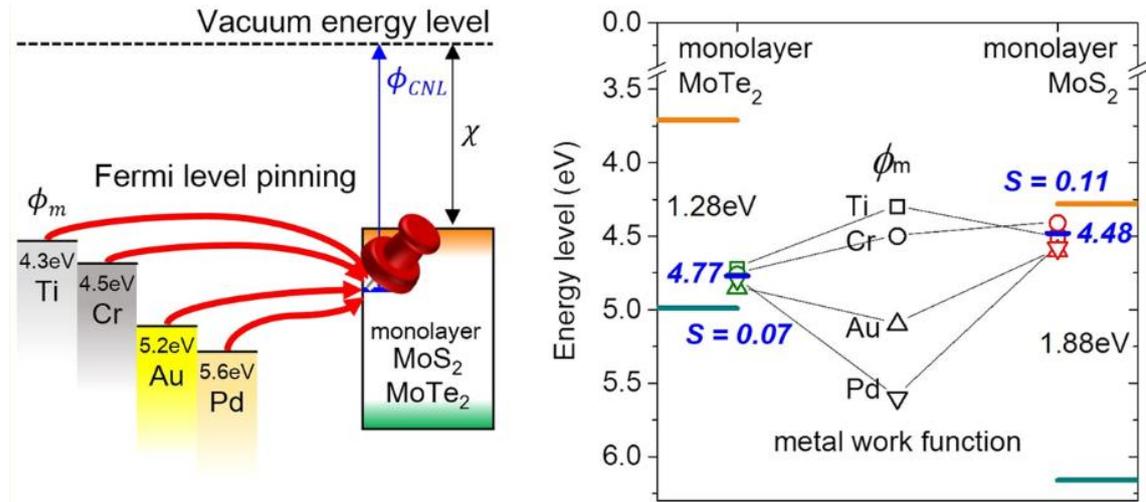


Figure 2.15 Fermi level pinning of TMDs with evaporated metal electrodes.^[71]

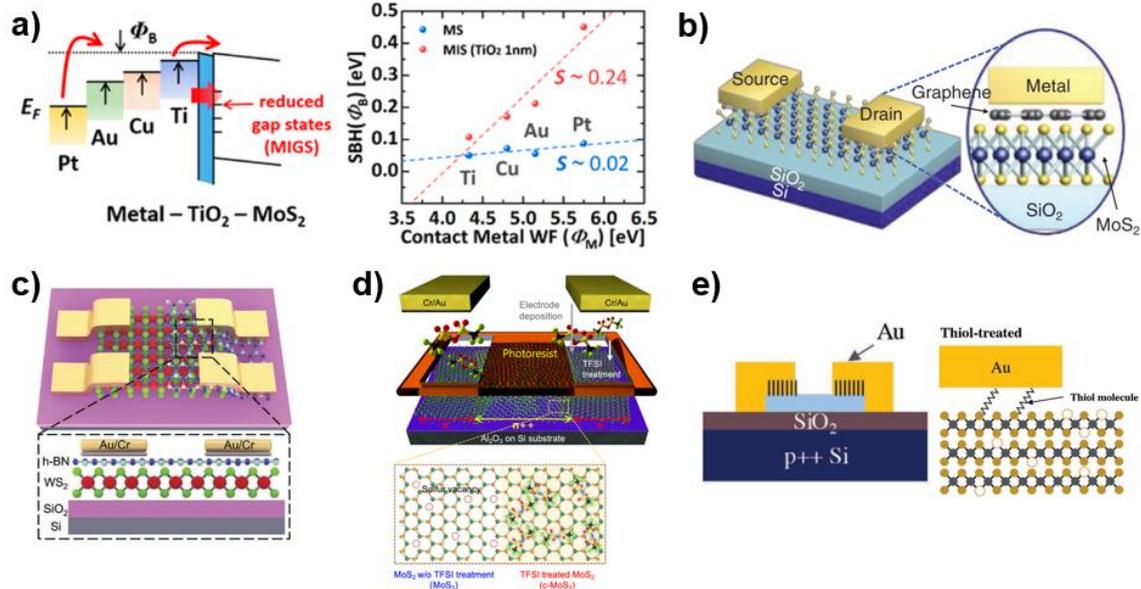


Figure 2.16 Several approaches of Fermi level depinning. a) insertion of metal oxide layer and corresponding pinning factor^[74]. b) introduction of graphene^[75]. c) insertion of h-BN tunneling layer^[76]. d) contact doping^[77]. e) functionalizing electrodes with SAMs^[78].

Various methods have been developed to improve the contact between electrodes and semiconductors and achieve Fermi level depinning (Figure 2.16), such as using van der

Waals (vdW) contacts^[79; 80], inserting h-BN tunneling layer or metal oxide layer^[74; 81; 82], introduction of graphene^[75], contact doping^[77; 83], and functionalizing electrodes with self-assembled monolayers (SAMs)^[78; 84; 85].

2.4.3 Contact engineering

The contact engineering of FETs mainly involves different interface contacts, including the interface contact engineering between electrodes and semiconductor and that between semiconductor and dielectric layer. In this thesis, we focus on the interface between electrodes and semiconductor, and primarily introduce the interface engineering of this interface.

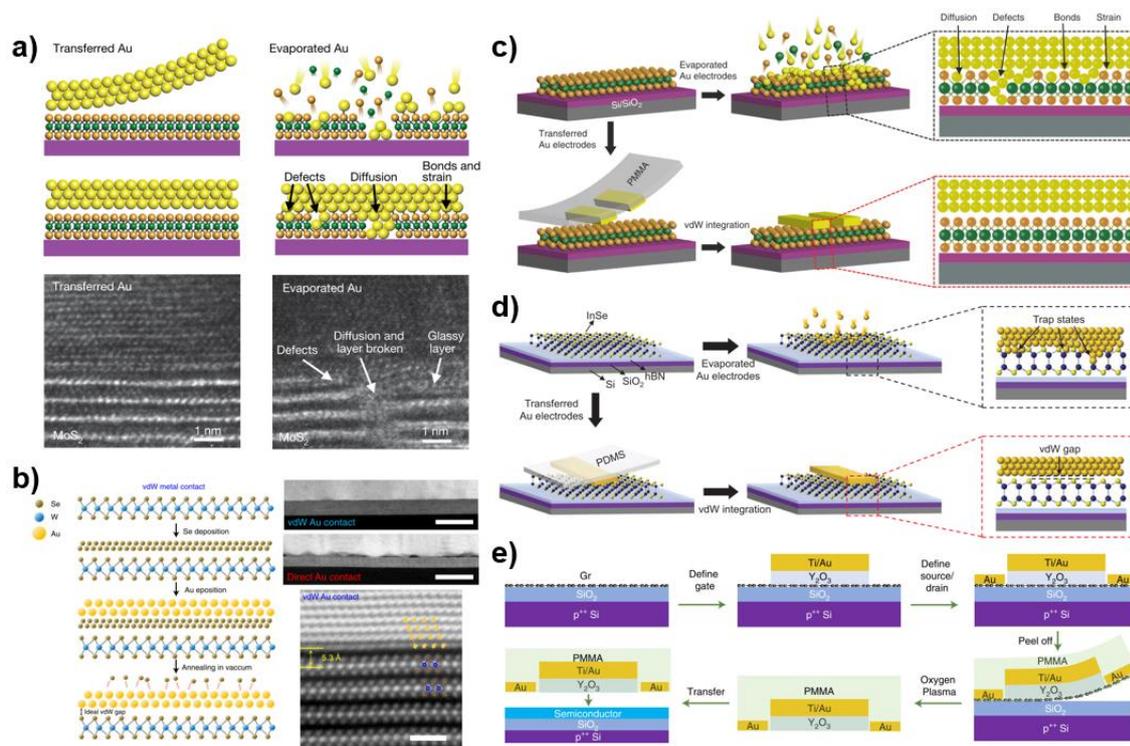


Figure 2.17 TMDs-based FETs fabricated by vdW contacts and direct metal deposition.^[53; 79; 80; 86; 87]

The SBH of metals in contact with TMDs can be predicted according to the Schottky-Mott rule, but the experimental values often deviate from the predicted values. This is due to “hot” energy damaging the TMDs semiconductor surface when evaporating metal electrodes, resulting in surface defects, which is also considered one of the reasons for FLP.

Figure 2.17 compares direct metal deposition and transfer electrode vdW contacts. As demonstrated, the vdW contact can provide a clean surface and prevent TMDs damage, thus revealing the intrinsic performance of the TMDs.^[88] Duan et al.^[79] fabricated MoS₂ FETs with vdW contact by transferring electrodes, and discovered that the SBH fully conformed to the Schottky-Mott rule. They subsequently reported WSe₂ FETs prepared by transfer electrodes and top-gated MoS₂ FETs^[53; 87; 89]. Additionally, Chhowalla et al.^[68] reported that the low melting point metal In can be directly deposited on the MoS₂ surface, forming a vdW contact. They directly deposited metal on the TMDs surface by controlling the evaporation parameters, realizing vdW contact between high WF electrodes (Pt, Pd) and TMDs^[90].

In this thesis, we also employ the transfer electrode method to achieve the vdW contact between functionalized metal electrodes and TMDs.

2.5 TMDs-based FETs applications

2.5.1 Metal–semiconductor–metal (MSM) diodes

The ultrathin 2D structure of TMDs and their sensitive contacts with metal electrodes create favorable conditions for applying FETs to metal-semiconductor-metal (MSM) diodes. Asymmetric charge injection diodes (Schottky diodes) or asymmetric electron-hole injection diodes (p–n diodes) fabricated using asymmetric S/D electrodes have been reported. Lee et al.^[78] introduced thiol molecules between one of the metal electrodes and MoS₂, providing an additional tunneling path for electrons injection, thus preparing asymmetric carriers injection Schottky diodes, as displayed in figure 2.18a-b, with the highest rectification ratio (RR) exceeding 10. Duan et al.^[79] prepared MSMs (p-n photodiodes) with vdW contacts by transferring asymmetric electrodes (Ag and Pt), as illustrated in figure 2.18c-d, due to the asymmetric electron and hole injection of the diode, the RR is as high as 10⁸ with an ideality factor η of 1.09. Similarly, Chhowalla et al.^[90] prepared In/Au-MoS₂-Pt MSMs (p-n photodiodes) with vdW contacts on the same MoS₂ crystal by evaporation (figure 2.18 e-f), and the RR of the device was as high as 10⁷. In this

thesis, we fabricated functionalized electrode Schottky diodes with vdW contacts using transfer electrodes, which will be introduced later.

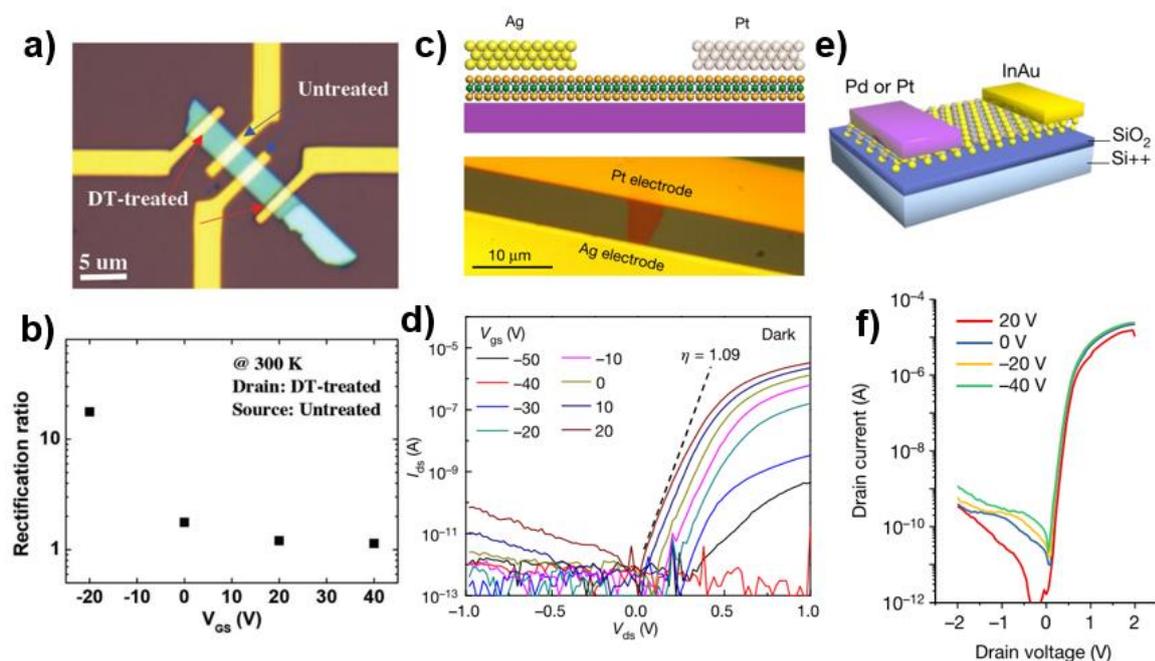


Figure 2.18 TMDs-based metal–semiconductor–metal (MSM) diodes.^[78; 79; 90]

2.5.2 Logic circuits (LCs)

TMDs-based FETs possess a high $I_{\text{on}}/I_{\text{off}}$ ratio, making them ideal components for fabricating logic circuits (LCs). A logic inverter based on complementary metal oxide semiconductor (CMOS) is one of the fundamental units of integrated circuits, capable of outputting a logic signal opposite to the input signal. In addition to high-performance n-type FETs (NMOS), high-performance p-type FETs (PMOS) are also crucial for the implementation of LCs. Due to the strong n-type doping from interfacial impurities and the existence of FLP, the majority of TMDs-based FETs are NMOS. TMDs-based PMOS is challenging to prepare, so researchers generally employ double-gate FETs, doping, or high work function metal contacts with ambipolar WSe_2 to achieve p-type transport.^[91] Das et al.^[92] reported that ambipolar FETs based on WSe_2 with high WF electrode Pd contact or low WF electrode Ni contact were controlled by dual-gate electrostatic doping to realize p-type or n-type transport, and subsequently prepared a complementary logic inverter (figure 2.19a-c), which exhibits a maximum gain of 25 at $V_{\text{DD}}=5\text{V}$. Javey et al.^[93] first doped WSe_2

by surface charge transfer doping and then used different WF electrodes (Au and Pt) to construct NMOS and PMOS, preparing a complementary logic inverter with a maximum gain of 13 at $V_{DD}=3V$, as shown in figure 2.19d-f.

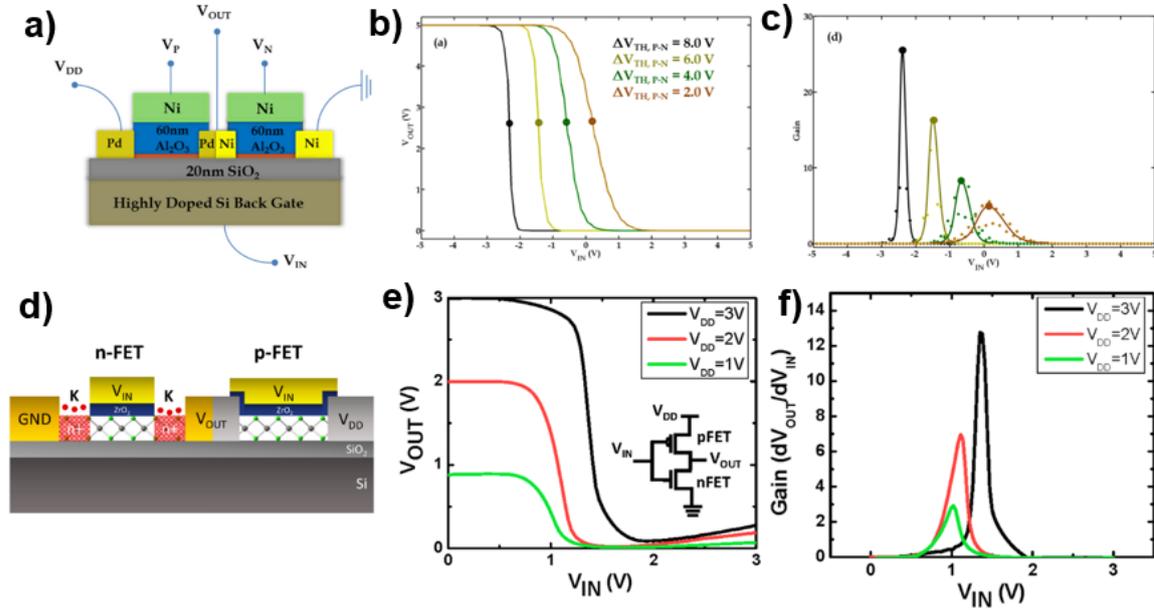


Figure 2.19 Complementary logic inverters based on WSe_2 .^[92; 93]

In addition to the aforementioned methods, the polarity of TMDs can also be regulated by controlling the contact between TMDs and metal electrodes. Liu et al.^[87] reported that the polarity of WSe_2 FETs was regulated using the same contact metal but different integration methods, i.e., thermal evaporation and low-energy vdW integration (electrode transfer) methods. As shown in Figure 2.20, the FETs with gold electrodes prepared by conventional thermal evaporation exhibit pure n-type electron transport behavior (NMOS) due to the existence of FLP between the electrodes and the semiconductor, while the FETs with gold electrodes prepared by transfer method exhibit pure p-type hole transport behavior (PMOS) due to the absence of FLP. A doping-free logic inverter was thus fabricated with a gain of 340 at $V_{DD} = 5.5 V$. They also demonstrated more complex logic NAND and NOR circuits. Similarly, in this thesis, we achieved polarity modulation of WSe_2 FETs by controlling the type of functionalized auxiliary layer between the vdW contact electrodes and WSe_2 semiconductor, and then demonstrated the logic inverter.

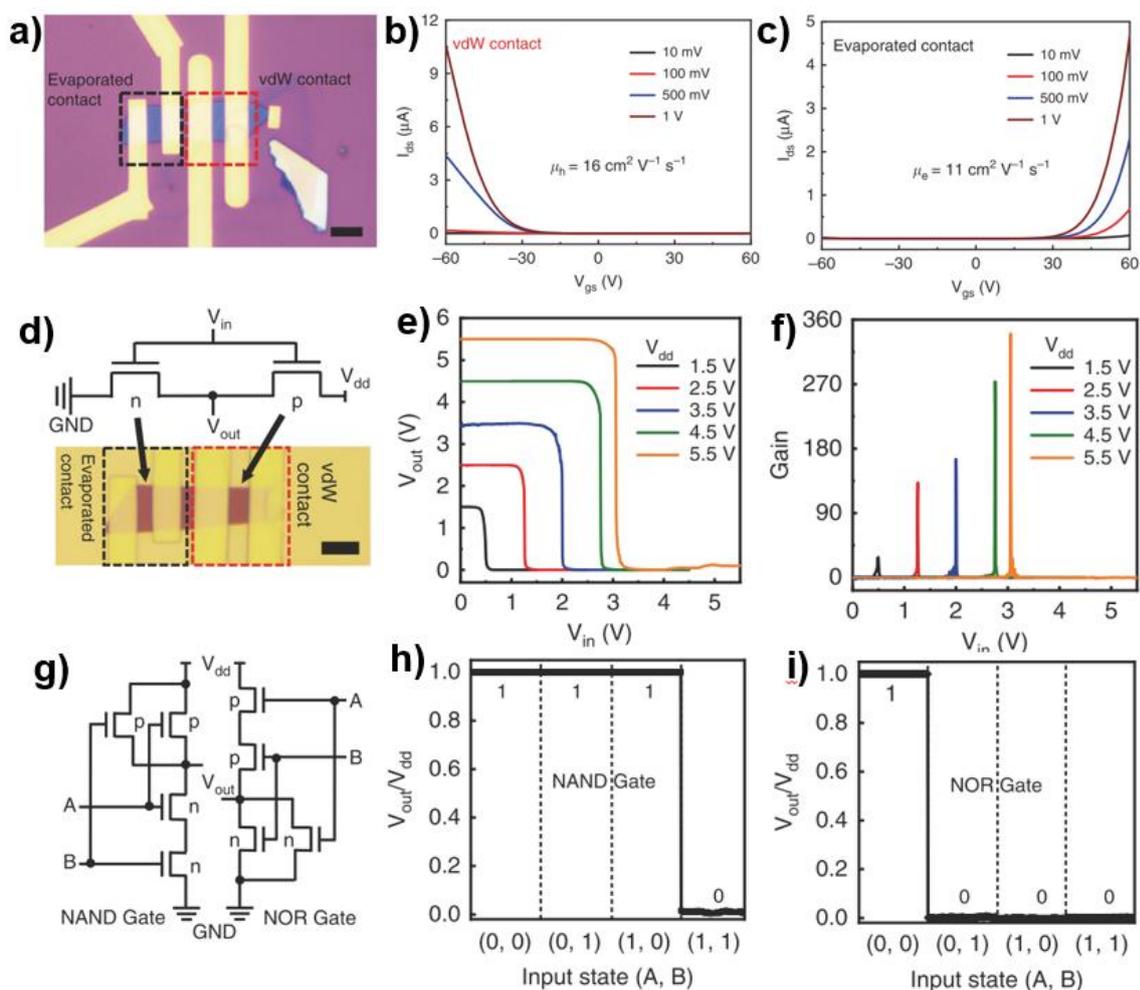


Figure 2.20 CMOS logic circuit based on WSe₂ FETs with different contact methods.^[87]

2.6 Summary

This chapter introduces the readers to TMDs-based FET devices, by explaining why TMDs can be excellent candidates for next-generation semiconductors, and analyzing FETs prepared from them, presenting their applications in logic circuits. The conclusions are as follows:

1. The types of TMDs materials, their unique electronic structural features, optical and optoelectronic properties, as well as the defects they contain are introduced, demonstrating their potential for the preparation of high-performance FETs and molecular functionalization.
2. TMDs-based FETs devices and their performance influencing factors are introduced,

their structural composition and characterization parameters are presented. We focused on the charge transport mechanism of the devices and explained how to improve the performance of FETs through electrode engineering and contact engineering, etc.

3. Combined with the device application in this thesis, the application of TMDs-based FETs in logic circuits is introduced, including diodes and inverters, etc.

2.7 References

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Chapter 3 Self-Assembled Monolayers (SAMs)

Functionalization of FETs

3.1 Introduction

Self-assembled monolayers (SAMs) are ordered thin films composed of a single layer of molecules, formed upon a thermodynamically driven process of molecular adsorption onto a substrate surface. During the self-assembly process, molecules spontaneously arrange into ordered monolayers on the basal plane of the substrate via covalent or non-covalent interactions (Figure 1).^[1] The simplicity and wide applicability of the process make SAMs an attractive platforms for constructing superlattices and for engineering surfaces. Consequently, SAMs are frequently employed in surface science, nanotechnology, and materials science to modify the surface properties of materials at the molecular level. SAMs represent an important class of materials due to their unique surface properties, such as their high stability, chemical resistance, and the capability to control surface functionality and reactivity. SAMs are also known to play an important role in FET devices^[2; 3] as they can be utilized for the controlled functionalization of source and drain electrodes^[4-6], of the dielectric substrate^[7-9], of the semiconductor^[10-12], and of the gate electrode^[13].

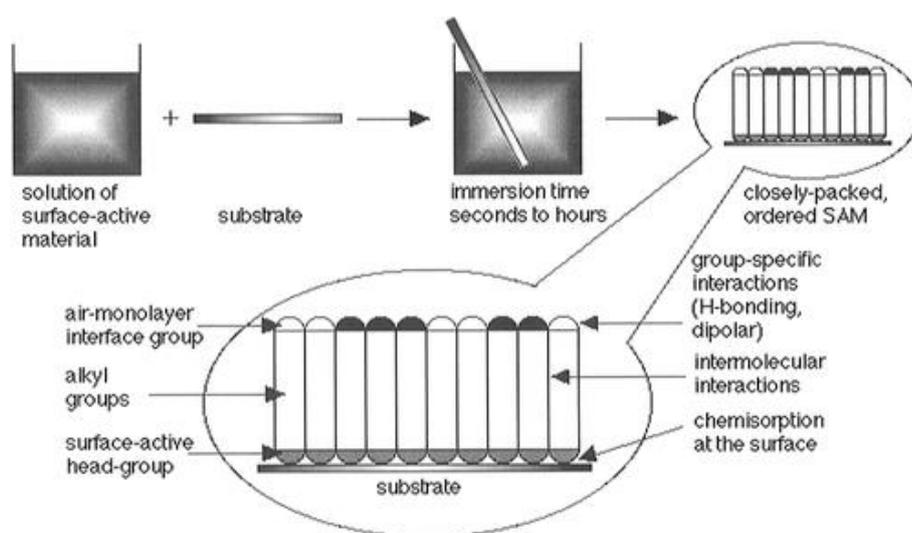


Figure 3.1 The formation process of self-assembled monolayers can be attained by simply immersing the substrate into a solution containing the target molecule.^[1]

Langmuir-Blodgett (LB) is another type of self-assembly process, accomplished by the mechanical force of the dwelling instrument. Although it can be employed to prepare single molecular layers (SAMs), bilayers, and multilayers,^[14] its usage is limited due to the poor stability and mechanical properties of LB membrane films (molecule-substrate interactions are van der Waals forces) and the high number of surface defects. Consequently, it falls beyond the scope of this thesis.

3.2 Classification of SAMs

According to the types of self-assembled molecules and substrates, SAMs can be mainly classified into the following categories:

3.2.1 Organic sulfide and selenium compounds SAMs

Sulfides and selenium compounds possess strong affinity for transition metal surfaces, attributable to the potential multiple bond formation of S and Se with surface metal clusters.^[1] These molecules encompass alkyl sulfides, alkyl disulfides, thiophenols, thiophenes, thioureas, and alkyl selenols. Among them, the most extensively employed are SAMs formed by organosulfides on transition metals, such as Au^[15-17] and Ag^[18-21]. Moreover, it has been reported that organosulfides can also form SAMs on copper^[22], platinum^[23; 24], mercury^[25; 26], iron^[27; 28], gallium arsenide^[29], and InP^[30] surfaces. In recent years, some studies have demonstrated that the S of organosulfides can repair chalcogenide vacancies on the surface of TMDs by covalent bonding to form SAMs^[31; 32], further expanding their applications scope.

3.2.2 Organosilicon derivatives SAMs

Organochlorosilanes, organoalkoxysilanes, and organoalkylaminosilanes can form SAMs on substrate surfaces containing hydroxyl groups, achieved by utilizing Si-O-Si bonds linked to silanol groups (-SiOH) on the substrate surface. Suitable substrates for these molecules include SiO₂^[9; 33; 34], GeO₂, Al₂O₃^[35], glass^[36], quartz^[37], mica^[38], ZnSe^[36], and Au^[39]. This approach is widely employed in the modification of various substrates, particularly organic/inorganic electrical devices (Figure 3.2). In Chapter 6, the molecule

we used to functionalize the sacrificial substrate is of this kind, specifically, octadecyltrichlorosilane (OTS) functionalized on SiO_2 .

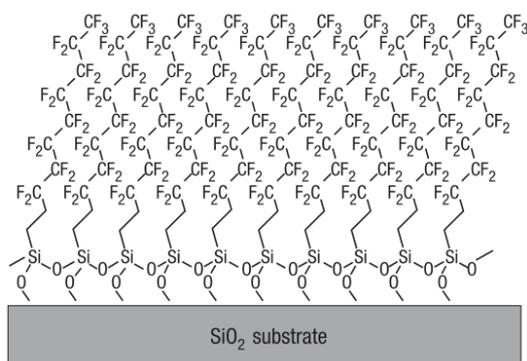


Figure 3.2 The organoalkoxysilanes SAMs on SiO_2 substrate.^[40]

3.2.3 Organic fatty acid SAMs

Organic fatty acid molecules, such as long-chain n-alkanoic acid, can be adsorbed onto the surface of metal oxide solid substrates (e.g., Al_2O_3 , AgO , CuO , and ITO (indium tin oxide)) to form SAMs through acid-base reaction (Figure 3.3). The underlying mechanism involves the formation of surface salts between carboxylate anions of fatty acid molecules and surface metal cations.^[7; 41-44]

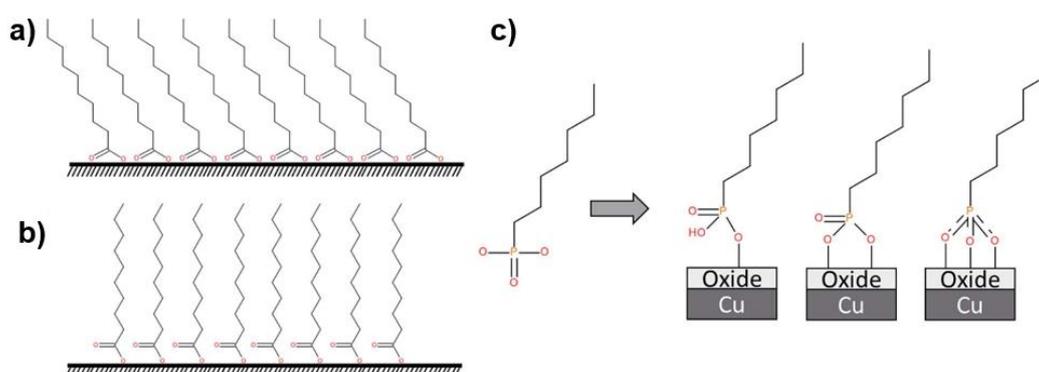


Figure 3.3 The formation of carboxylic acid SAMs (a and b) and alkylphosphonic acid SAMs on copper oxide (c).^[44]

3.2.4 Alkyl SAMs on silicon

It has been reported that alkyl chains can be covalently bonded to Si substrates via C–Si bonds, forming SAMs through a multi-step free radical reaction.^[45] However, due to the

complexity of the reaction and the low quality of the resulting SAMs, these types of molecules have not been widely employed.

3.3 Kinetic process

The most common SAMs are obtained via the self-assembly of organic sulfides on Au or by covalent grafting on 2D semiconductors. This thesis focuses on this type of SAMs, hence we introduce here their formation mechanisms.

3.3.1 Kinetic process of SAMs on Au

Taking common organic thiols as an example, organic thiols are oxidatively added to the Au surface through the S-H bond. Subsequently, hydrogen is reduced and eliminated to generate H₂ molecules, as illustrated in the reaction equation below^[46; 47]

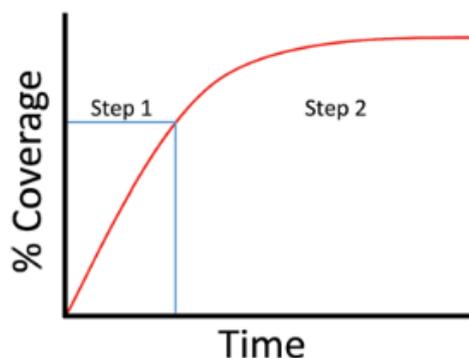
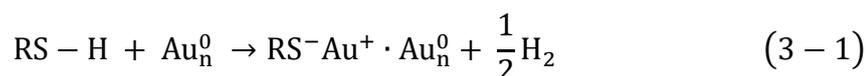


Figure 3.4 Two-step formation process of SAMs on Au.^[44]

The reaction is considered to occur in two steps: the first step is a rapid Langmuir adsorption step, lasting only a few minutes, during which the film thickness reaches 80%-90% and the contact angle reaches almost its maximum value (when low concentration solutions are used, i.e., below 1 μM , the reaction is slower, and this step takes > 100 minutes). The second step is a very slow surface crystallization step, which occurs during the timeframe of several hours. The film thickness and contact angle will reach their maximum value, and the film changes from disorder to order structure (Figure 3.4).^[44; 48]

3.3.2 Kinetic process of SAMs on TMDs

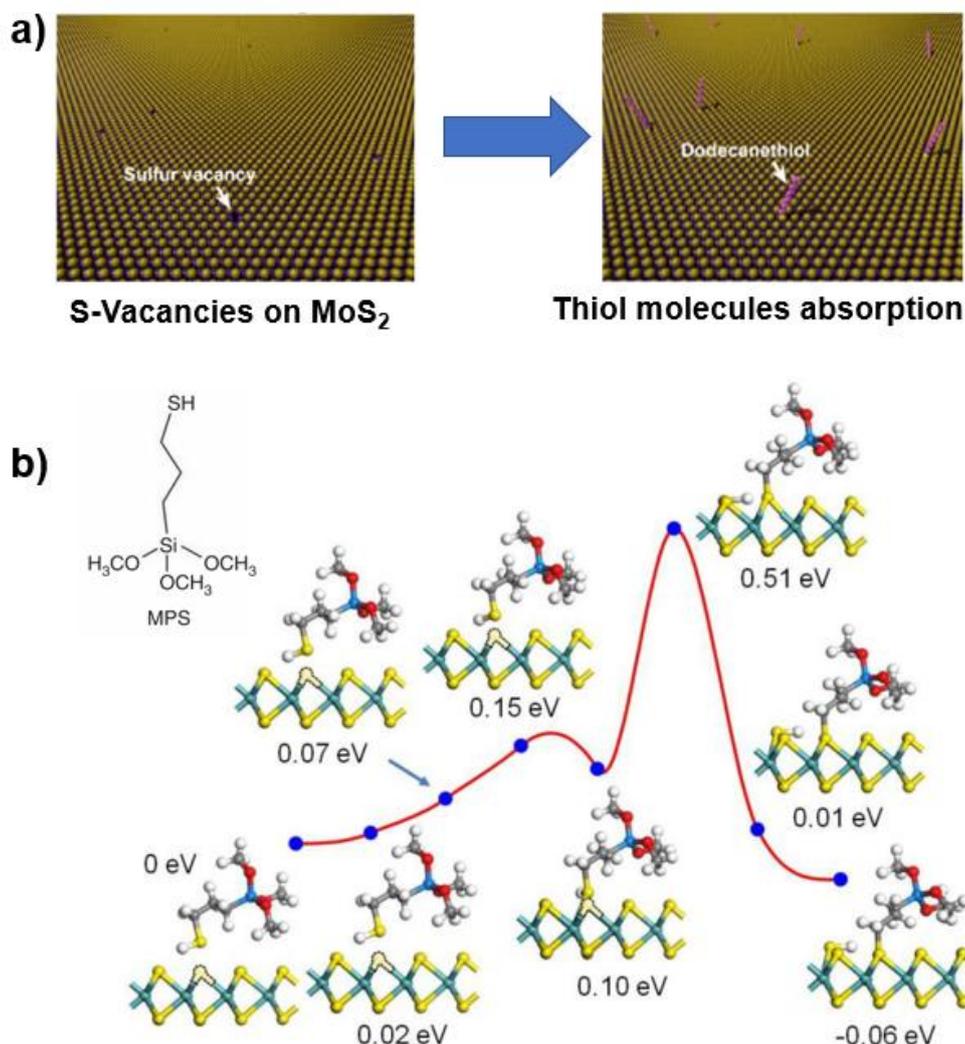


Figure 3.5 The kinetic process of the reaction between S-defects containing TMDs and thiolated molecules.^[49; 50]

The formation of organosulfide SAMs on 2D semiconductor surfaces occurs through the covalent bonding of S atoms in sulfides to S-vacancies in TMDs semiconductors. Taking MoS₂ as an example, the sulfur group in sulfides tends to form covalent bonds with unsaturated vacancy defects in the sulfur layer and Mo edges. The sulfide molecule chemisorbs onto the S-vacancy through the sulfur atom, cleaving the S–H bond and forming a thiolate surface intermediate. The dissociated H atoms bond to adjacent S atoms.^[50] In this process, the sulfur vacancies on MoS₂ surface serve as catalytic reaction sites (Figure 3.5).^[10; 49-53] Molecules covalently grafted on the surface of MoS₂ can also

break the S-C bond in a suitable environment, completing the defect repair of MoS₂^[50].

3.4 The main parameters of SAMs

Once the substrate has been functionalized with SAMs, it is essential to characterize the resulting SAMs to assess their quality. The following main parameters of SAMs are those which are assessed:

3.4.1 Thickness

The thickness of SAMs is commonly measured using ellipsometers, profilometry, or AFM. The thickness of SAMs can provide information on molecular orientation when compared to theoretical values.

3.4.2 Morphology

The morphology of SAMs is typically characterized by high-resolution AFM or STM, enabling the observation of individual molecular structures, atomic arrangements on surfaces in three dimensions, and the physical and chemical properties associated electronic behavior. For instance, well-packed alkanethiol molecules on gold surfaces exhibit a flat and uniform morphology, reflecting the substrates underneath. (Figure 3.6) However, when the affinity between SAMs molecules and the substrate surface is low or deposition conditions are suboptimal, SAMs molecules may form clusters or islands on the substrate, leaving gaps between them.^[54]

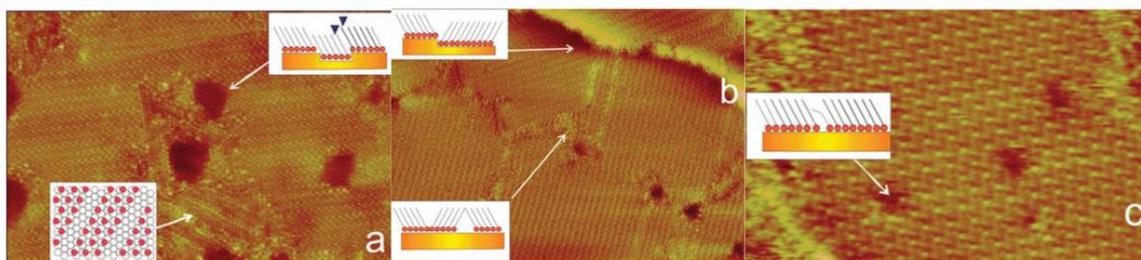


Figure 3.6 STM images of alkanethiolate SAMs on Au (111).^[54]

3.4.3 Hydrophilicity and surface energy

The hydrophilicity (or hydrophobicity) and surface energy of SAMs can be measured with

a contact angle (CA) by using water or organic solvents as liquid media. The surface energy of a SAMs reflects the amount of energy required to increase the SAMs' surface area or break intermolecular forces between SAM molecules. The surface energy can also reveal several characteristics of the SAMs, such as its wettability, adhesion, and reactivity towards other molecules or surfaces. CA analysis reflects the structural compactness of SAMs. In general, hydrophobic molecules exhibit a contact angle (water) greater than 90° , and the denser the structure, the larger the CA. Hydrophilic molecules exhibit a contact angle less than 90° , and the better the hydrophilicity, the smaller the CA. (see Figure 3.7)

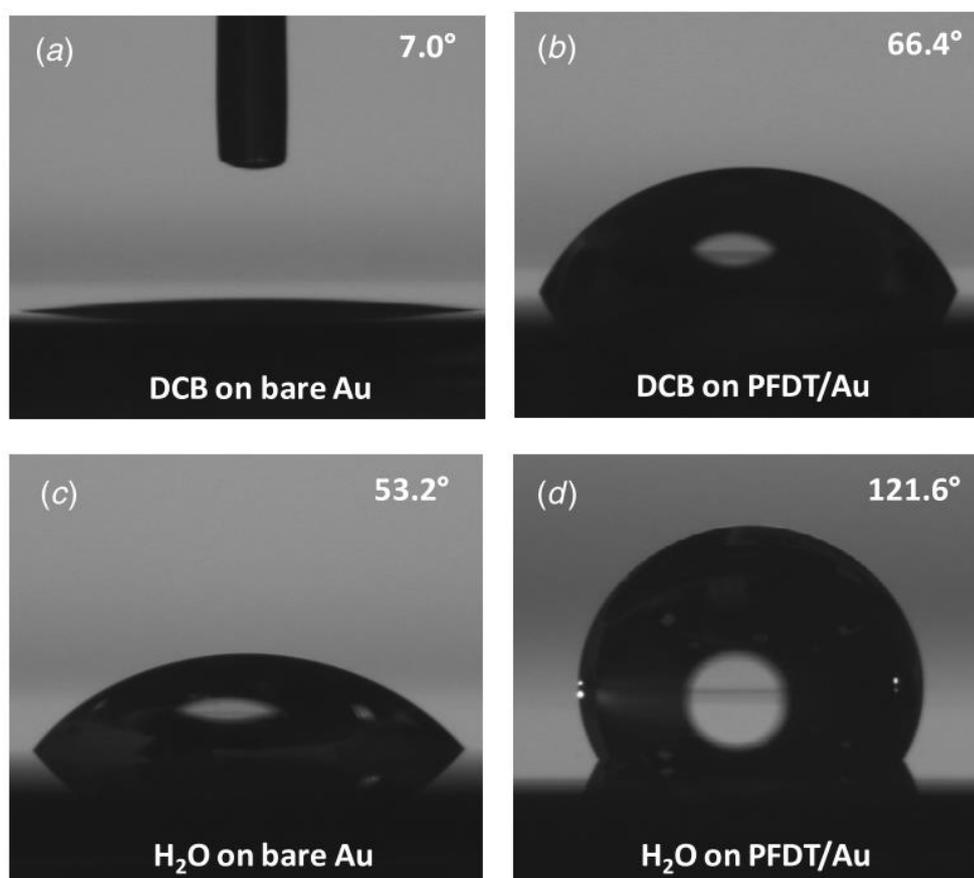


Figure 3.7 Contact angles of dichlorobenzene (DCB) and water on bare Au surface (a & c) and PFDT SAMs functionalized Au surface (b & d).^[55]

3.4.4 Elements or chemical composition

The elemental analysis of SAMs is carried out by X-ray photoelectron spectroscopy (XPS). By offering an atomic composition mapping of a surface, it can provide the most intuitive

evidence of molecular presence and assist in qualitative and quantitative elemental analysis, and chemical state assessment. Therefore, it is widely employed in SAMs characterization.

3.4.5 Energy level

The energy levels of SAMs can be determined by ultraviolet photoelectron spectroscopy (UPS). The vacuum UPS not only offers an estimation of the work function (WF) of SAMs from the secondary electron cut-off edge (see Figure 3.8), but it also provides key information to quantify the injection barrier from the Fermi edge (inset of Figure 3.8), and determine the energy of the highest occupied molecular orbital (HOMO) value of SAMs.^{[15;}

56; 57]

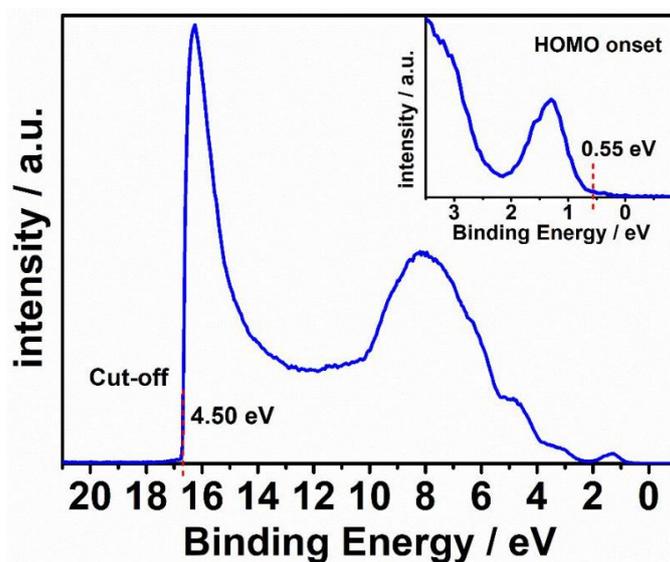


Figure 3.8 UPS of 6-(Ferrocenyl)hexanethiol (FHT) SAMs, the red dash line is the cutoff edge of secondary electrons and the illustration is the enlarged Fermi edge (the injection barrier edge).^[15]

3.4.6 Conductance

One of the crucial parameters that must be taken into account when functionalizing devices, and especially when functionalizing electrodes are functionalized, is the electrical properties of the SAMs, including its conductance (C). It is crucial to choose the appropriate molecules for such functionalization because if the electrical resistance of SAMs is too high, injection from electrode to semiconductor becomes challenging. The electrical signal of SAMs is measured by integrating SAMs in-between two electrodes

thereby forming a molecular junction, and measuring the current value (I) when a specific voltage (U) is applied. (See Figure 3.9) According to the measurement results, the conductance information of SAMs can be calculated from $C = I/U$.^[58-61]

Generally, the conductance of SAMs is strongly related to the nature of molecular structure. Electron tunneling is more efficient when taking place through an unsaturated chain rather than through a saturated one. Moreover, the current decreases exponentially with the length of the chain. Hence to maximize conductance and minimize the tunneling resistance, short conjugated molecules comprising just one benzene ring in its main chain were selected to functionalize the electrodes in this thesis.

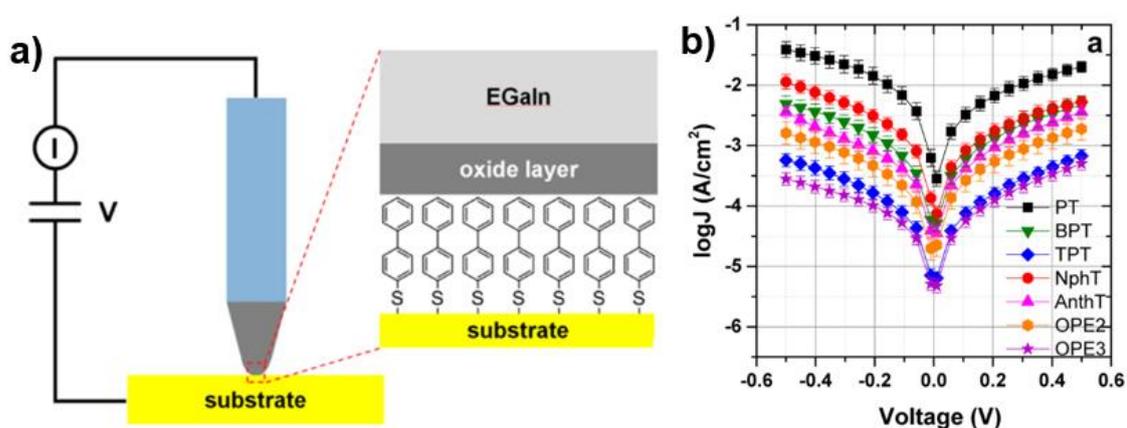


Figure 3.9 Schematic of electrical measurement of SAMs and electrical properties of various SAMs.^[61]

3.5 Application of SAMs functionalization in FETs

As one of the most important means of functionalization, SAMs have been widely used in FETs. This thesis primarily focuses on the application of SAMs in FETs, covering three aspects: one is used to functionalize the source and drain metallic electrodes and adjust the WF of electrodes, the second is used to functionalize the dielectric layer, and the third is used to functionalize the semiconductor layer.

3.5.1 Functionalization of metal electrodes

For FET devices, the energy level difference between the electrode and frontier orbitals of

the semiconductor determines the injection barrier of the device, thus affecting the overall performance of the FET devices. However, due to the limited variety of electrode materials, it is difficult to find a metal material that matches well the energy level of the semiconductor. Therefore, it is necessary to modify the electrode to reduce the injection barrier of the device and improve performance.^[62-65] The electrode's functionalization with SAMs is a viable approach to adjust its WF. The direction of the change can be controlled by the SAMs molecular dipole moment orientation, and the magnitude of the change can be controlled by the size of dipole moment, which endows unlimited possibilities for the electrode to match the semiconductor energy level.^[66; 67] Consequently, SAMs have been widely used to adjust the WF of electrodes in FETs.^[2; 5; 6; 68; 69]

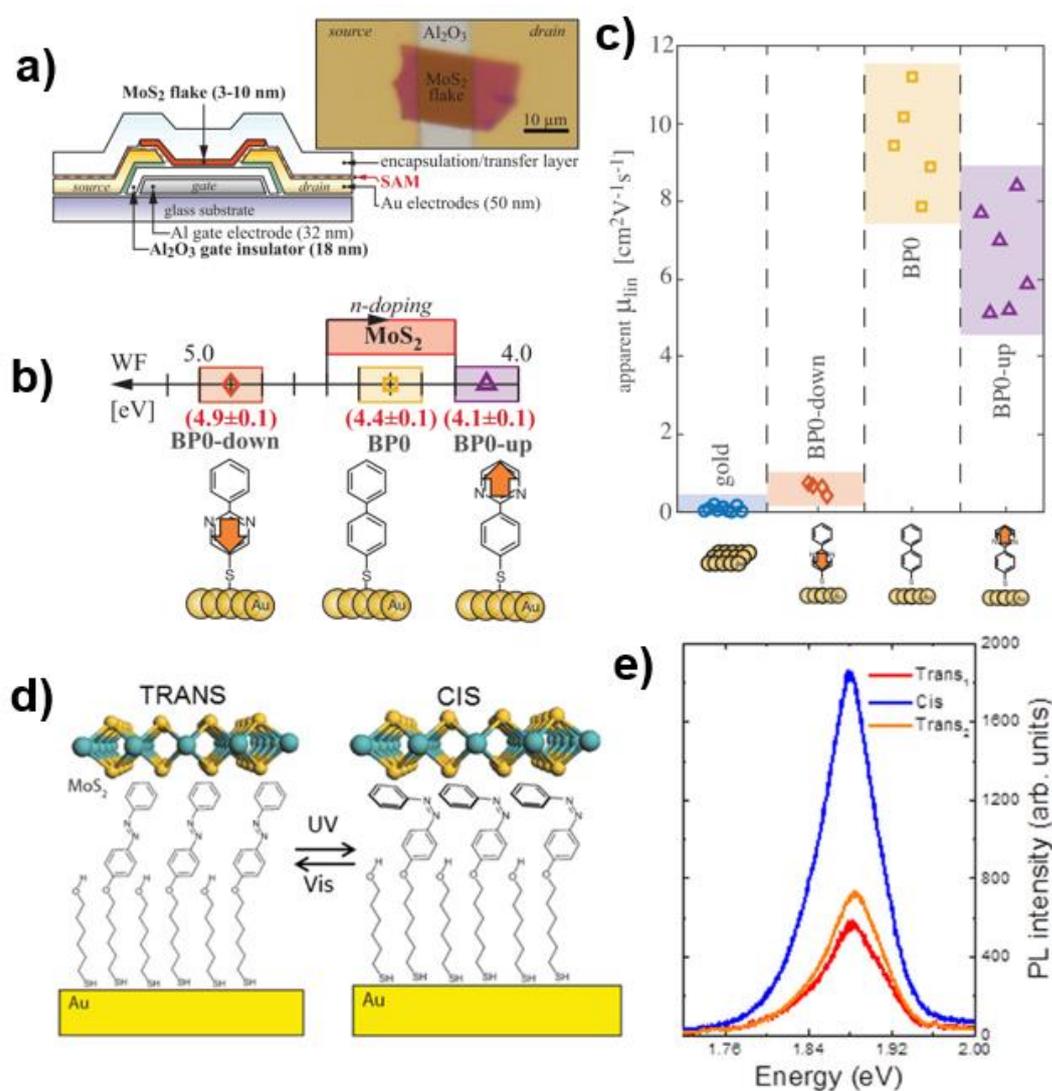


Figure 3.10 Application of SAMs functionalized electrodes. a) Schematic and optical image of

MoS₂ FETs. b) Chemical structure of molecules. c) Linear mobility of FETs with (without) SAMs functionalization.^[70] d) MoS₂ on molecularly functionalized electrode with azobenzene in *trans* and in *cis* configuration. e) The change of MoS₂ PL spectrum caused by the conformational transition of azobenzene molecule.^[71]

Patrikar et al. modified Cu electrodes with SAMs of pentafluorobenzenethiol (PFBT) or perfluorodecanethiol (PFDT), to enhance the performance of FETs based on pentaphenylene. They proposed that the improved performance is due to the optimized charger injection and charge carrier doping effect of the SAMs on the electrode surface, which increased the concentration of charge carriers at the interface between the electrode and the semiconductor.^[69] Matković et al. investigated the use of pyrimidine-containing SAMs for interfacial band engineering at the interface between MoS₂ and Au in order to achieve contact-resistance-free bottom-contacts FETs (Figure 3.10). The authors proposed that the pyrimidine-containing SAMs can modify the electronic structure of the interface, resulting in a reduction of the SBH and thus reducing the contact resistance.^[70] Li et al.^[71] reported the characteristics of mono and bi-layer MoS₂ on electrodes functionalized with photo-switchable azobenzene molecules. As shown in Figure 3.10d and e, when MoS₂ is in contact with electropositive azobenzene molecules in the *trans* configuration, the PL spectrum shows n-doped features, whereas when the photoisomerization is *cis*, the doping effect decreases, PL magnitude increased by a factor of 3.^[12] This reveals the potential of photoisomerization of molecules functionalized electrodes for applications in FETs.

However, most of the works of functionalized electrodes reported so far rely on FETs in bottom-contact configuration. Conversely, top-contact configuration offers a more efficient charge injection^[72-77]. However, top electrodes are generally deposited by thermal evaporation, making their chemical modification difficult.^[72; 78; 79] Therefore, the fabrication of top-contact FETs with in which the electrodes are chemically functionalized remains a major challenge. Fortunately, the work in Chapter 6 of this thesis overcomes this challenge and proposes a general strategy for preparing the top-contact FETs configuration with SAMs functionalized electrodes, which fills the gap in the field.

3.5.2 Functionalization of dielectric layer

For FET devices, the SAMs can modify the surface properties of the dielectric layer, such as the surface energy and charge density, which can affect the performance of the device by influencing the interface between the dielectric layer and the channel material.^[9; 80] SAMs functionalization can also eliminate surface impurities of the dielectric layer, providing a stable and uniform surface, thereby enhancing the performance of the device. In addition, SAMs with functional end groups can dope semiconductors, thereby increasing or decreasing the carrier concentration.^[3; 81-83]

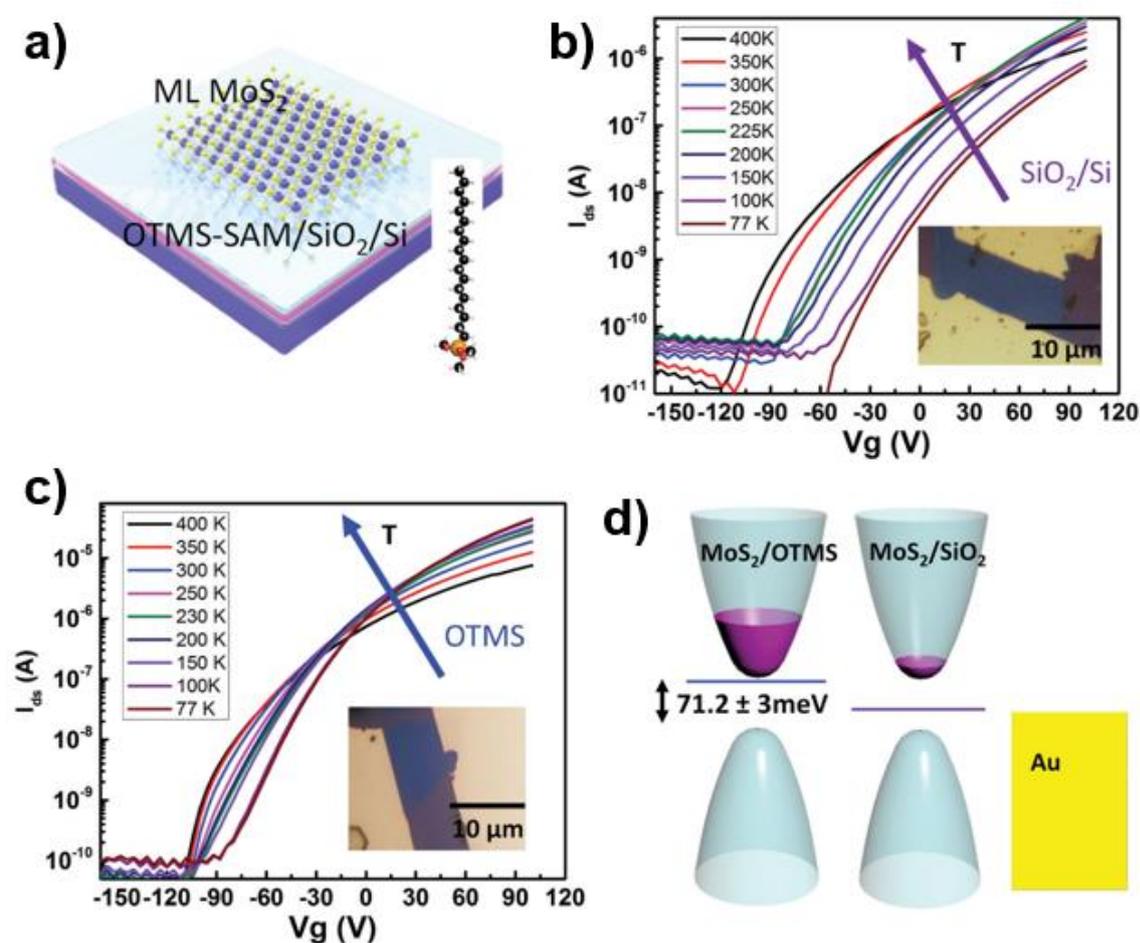


Figure 3.11 Effect of dielectric layer functionalization on semiconductor. a) Monolayer MoS₂ on OTMS functionalized SiO₂. b-c) Comparison of temperature dependent electrical properties of MoS₂ FETs on OTMS/SiO₂/Si and bare SiO₂/Si. d) Schematic diagram of energy level.^[33]

Figure 3.11 shows the transfer characteristics of MoS₂ FETs on octadecyltrimethoxysilane (OTMS) functionalized SiO₂/Si (3.11c) and untreated SiO₂/Si (3.11b) at different

temperatures. MoS₂ FETs on OTMS-functionalized substrate exhibits a mobility of 42 cm² V⁻¹ s⁻¹, which is an order of magnitude higher than that on untreated substrate. This is due to the fact that the charged impurity density of MoS₂ on OTMS-functionalized substrate is much lower than that of MoS₂ on untreated substrate.^[33] Najmaei et al. demonstrated the effects of substrates functionalized with SAMs containing different end functional groups on the electrical properties of MoS₂ FETs (see Figure 3.12). Their results show that the molecularly functionalized substrates with SH, NH₂, and CF₃ end groups can increase the mobility of MoS₂ FETs, while the mobility of MoS₂ FETs on hydroxylated SiO₂ decreases.^[8]

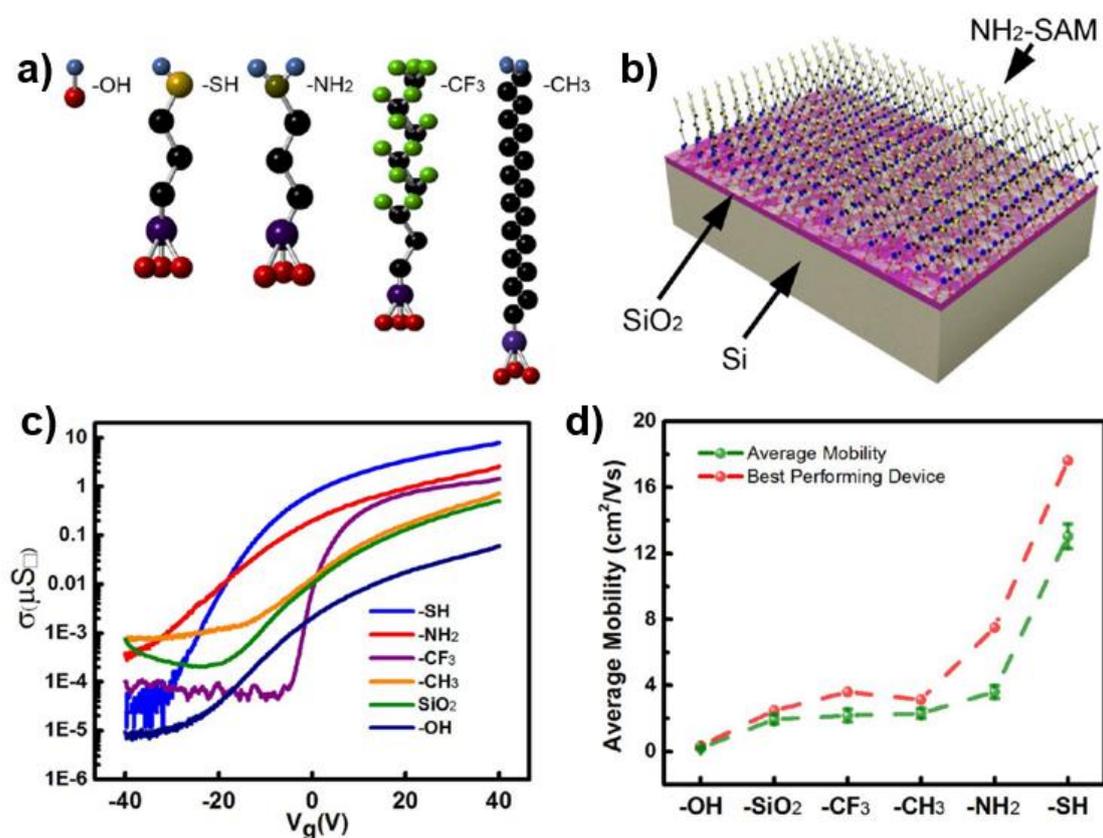


Figure 3.12 Effects of dielectric layers functionalization with different end molecules on MoS₂ FETs. a) Chemical structures of various SAMs with different end functional groups. b) Illustration of SAMs with NH₂ group functionalized substrate. b) Electrical properties of MoS₂ FETs with (without) various SAMs functionalized substrates. c) Mobility of MoS₂ FETs on various SAMs functionalized substrates.^[8]

3.5.3 Functionalization of semiconductor

In FETs, SAMs functionalization of semiconductors can modify the electrical properties of semiconductors, such as charge density, and photoluminescence, on the one hand, and can passivate TMDs semiconductor defects on the other hand.^[32; 51; 84; 85]

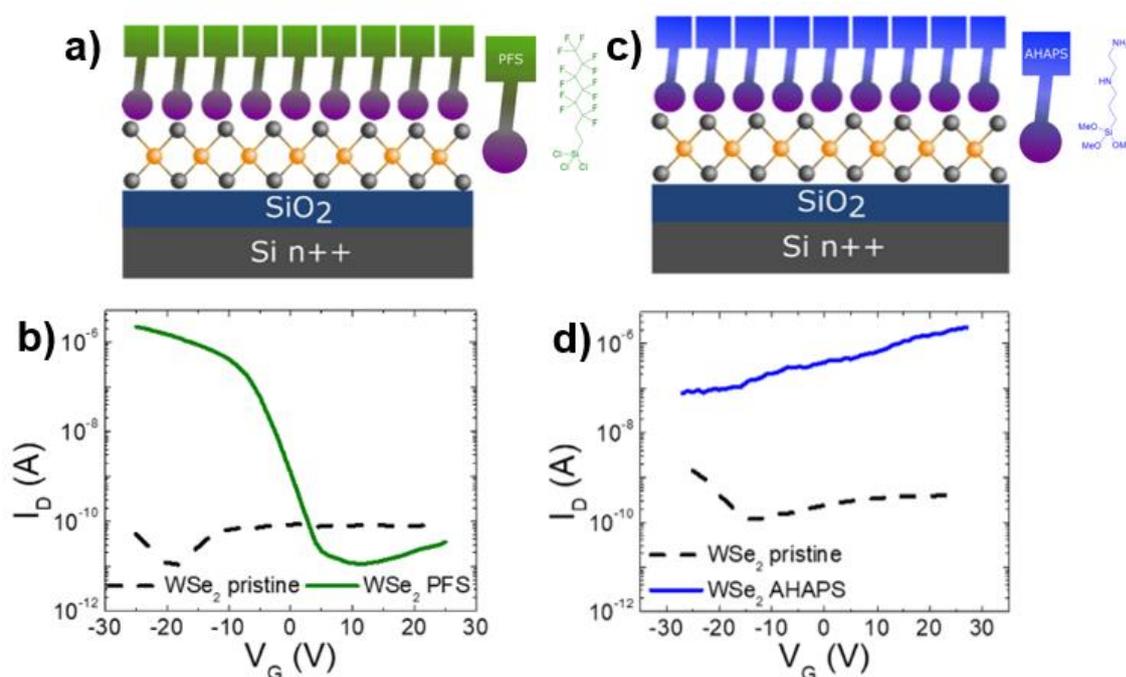


Figure 3.13 Effects of TMDs based semiconductor functionalization on FETs. a-d) Device architecture and corresponding transfer curve of WSe₂ functionalized with PFS (a-b) and AHAPS (c-d).^[86]

SAMs can be used to dope semiconductor by introducing functional groups or dopants. The functional group within SAMs can endow the semiconductor with various functionalities, such as photoresponse,^[87-94] electrochemical regulation,^[95; 96] sensing,^[97; 98] and enhancement of the hydrogen evolution reaction^[99] etc. Molecules featuring electron-donating or electron withdrawing groups can result in semiconductor doping through charge transfer or dipole induction, leading to increased carrier concentration and mobility.^[100; 101] This approach has been employed to enhance the performance of FETs, such as reducing the threshold voltage and increasing the on-current. Stoeckel et al. reported that functionalizing monolayer WSe₂ surfaces with silane-containing trichloro(1H,1H,2H,2H-perfluorooctyl)silane (PFS) and N[3-

(trimethoxysilyl)propyl]ethylenediamine (AHAPS) molecules can improve the electrical properties of monolayer WSe₂ FETs (Figure 3.13 a-d).^[86]

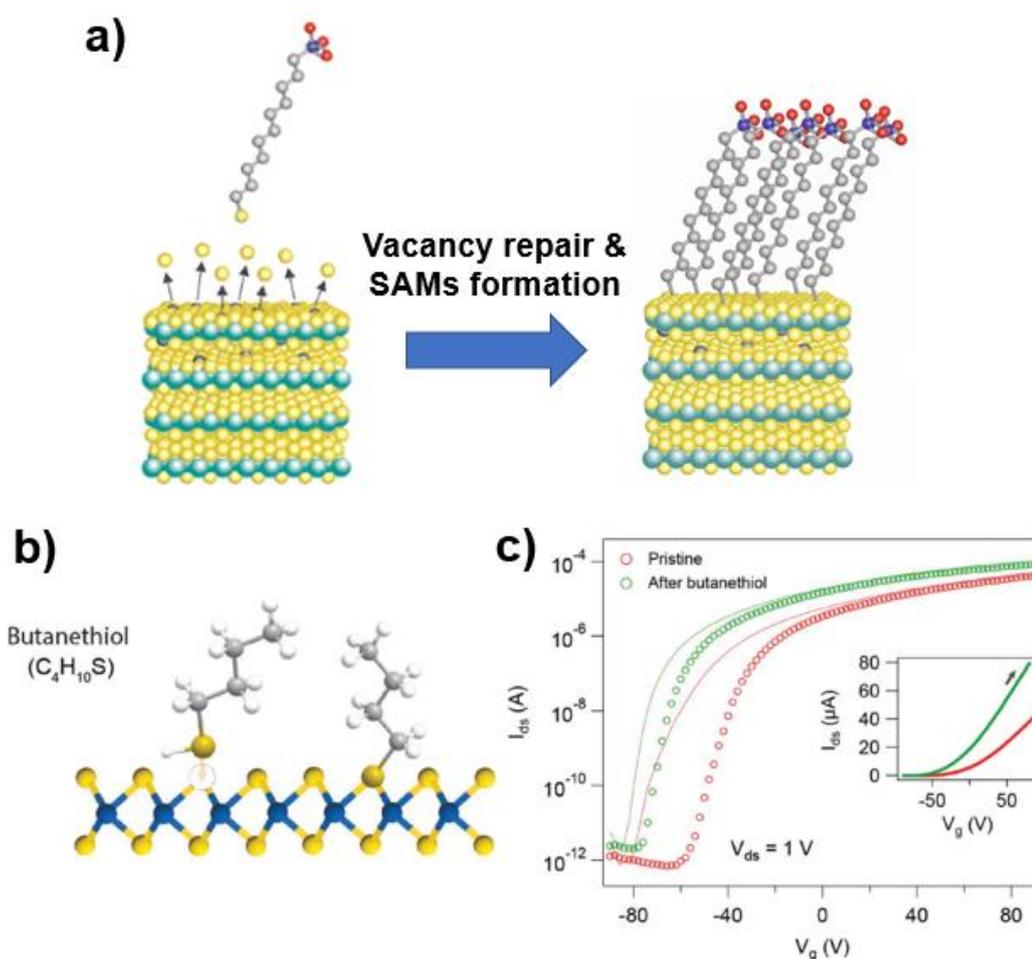


Figure 3.14 a) Schematic of SAMs functionalization on vacancy-containing TMDs. b-c) Schematic of butanethiol molecules repair the sulfur vacancies of MoS₂ via covalent interaction and the transfer curves before and after functionalization.^[31; 53]

SAMs can also be used to passivate defects in TMD semiconductors, improving device performance by reducing recombination losses and enhancing the charge carrier transport.^[102] Moreover, unlike organic semiconductors, when TMDs are functionalized (defect passivation) with SAMs, the S atoms of organosulfide molecules covalently graft onto the crystal surface, filling and repairing defects (Figure 3.14).^[31] Utilizing SAMs with unique groups or features to functionalize TMDs introduces the diverse characteristics of molecules into semiconductors, endowing them with strong application potential. Chapter 5 in this thesis demonstrates this approach by functionalizing the surface of defect

engineered MoS₂, achieving isomer discrimination by leveraging the sensitive surface of monolayer MoS₂.

Overall, SAMs functionalization of semiconductors in FETs represents a promising and versatile approach for developing high-performance electronic and optoelectronic devices with improved efficiency, stability, and multifunctionality.

3.6 Summary

This chapter explores the impact of SAMs functionalization on FETs, covering the introduction of SAMs classification, the kinetic process of SAMs assembly, the factors affecting the self-assembly process, and the key parameters of SAMs. Furthermore, we highlight the utilization of SAMs functionalization in FETs, comprising three main aspects:

First, the functionalization of electrodes can tune metal electrode work function, thereby reducing contact resistance and enhancing carrier injection. Second, the functionalization of dielectric layer, on the one hand, can eliminate surface impurities and provide a stable and uniform surface, leading to improved device performance. On the other hand, it can dope the semiconductor to increase the carrier concentration, thereby enhancing the performance of the device. Third, the functionalization of semiconductors, on the one hand, can dope semiconductors similarly to dielectric layer functionalization, on the other hand, the functional groups of molecules can also be introduced into semiconductors which endows semiconductors with multiple functions, such as photoresponse, electrochemical charge transfer, sensing, and others. Additionally, the semiconductor functionalization can repair the chalcogen vacancy defects of TMDs crystals and prepare multifunctional devices through molecular functional groups.

Overall, this chapter highlights how SAMs functionalization plays a pivotal role in FETs and enabling multifunctional devices. Given the myriad of molecular structures available, a broadest portfolio of functions can be imparted to FETs.

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Chapter 4 Experimental Techniques

4.1 Introduction

This chapter outlines the preparation methods for TMDs and TMDs-based FETs. It also introduces parameters and conditions employed for optical microscopy, AFM, Raman, PL, XPS, PESA, molecular junction preparation and testing, contact angle, SEM, device electrical characterization, and DFT theoretical calculations to offer a comprehensive perspective on the experimental techniques employed throughout the thesis.

4.2 Preparation of TMDs

4.2.1 Substrate preparation

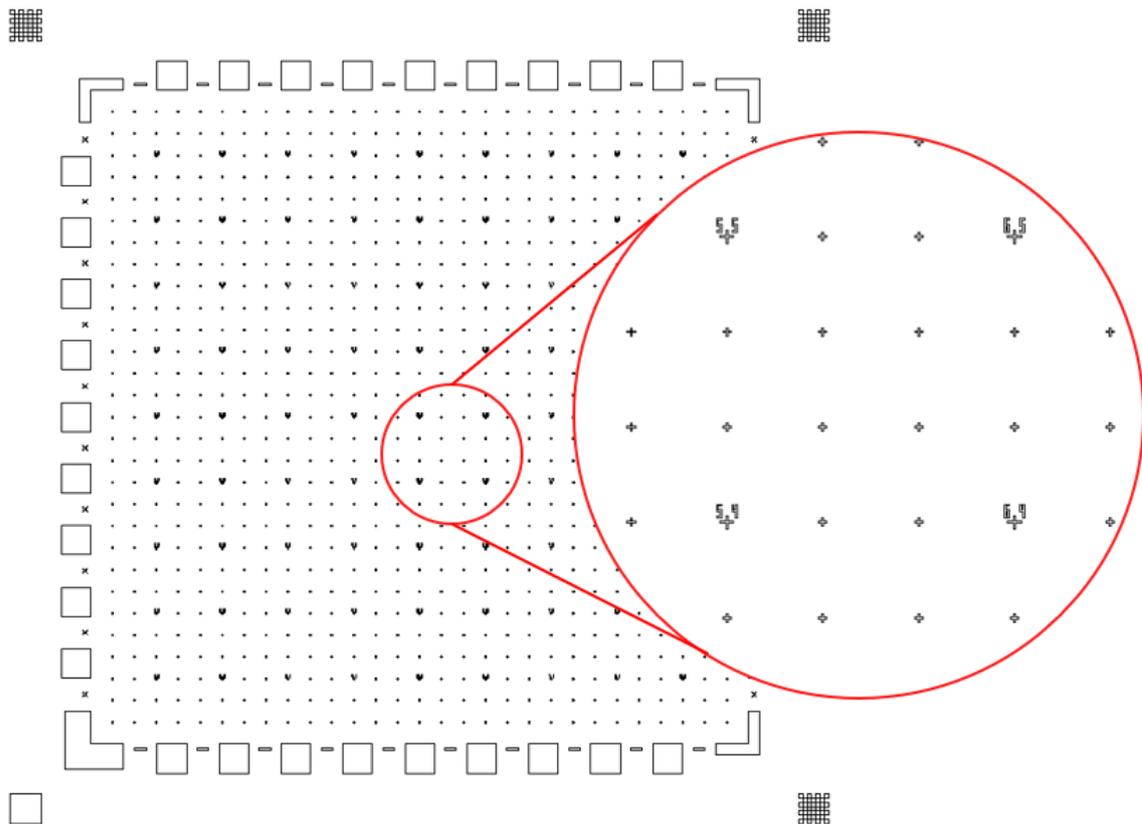


Figure 4.1 The pattern of substrate for FET device fabrication.

Heavily n-doped silicon wafer (surface doping: $n \sim 3 \times 10^{17} \text{ cm}^{-3}$) with a 270-nm-thick thermally grown silicon dioxide (SiO_2) layer serves as the bottom-gate substrate in this

thesis (wafer size: 12 mm × 12 mm). Custom-patterned wafers, designed by former colleague Dr. Simone Bertolazzi, were purchased from Fraunhofer IPMS (Germany), as depicted in Figure 4.1. The pattern comprises periodic cross markers and serial numbers used to locate randomly distributed TMDs crystals prepared by mechanical exfoliation. The periodic cross marks were prepared by depositing a 30 nm Au layer with a 10 nm indium-tin-oxide (ITO) adhesion layer.

The substrate underwent a standard cleaning protocol prior to its use: First, the surface was subjected to 10-minute sonication baths to remove photoresist and other organic materials on the surface. The substrate was then sonicated with isopropanol (IPA) and ethanol for 10 minutes each to eliminate surface adsorbates. After cleaning, the substrate was blow-dried using a nitrogen gun and treated with plasma for 10 minutes to thoroughly remove residual organic contaminants on the surface. The cleaned substrate was used immediately to prevent re-adsorption of contaminants during storage.

4.2.2 TMDs preparation

The TMDs preparation process comprises four parts: The first is the preparation of TMDs by traditional mechanical exfoliation method. The second is the preparation of CVD TMDs crystals and transfer from the purchased sapphire substrate to the target wafer substrate. The third is to artificially create chalcogen vacancy defects on the TMDs crystal surface through defect engineering. The fourth is the molecular functionalization of defect-containing monolayer MoS₂.

4.2.2.1 Mechanical exfoliation

The mechanical exfoliation technique used to create graphene from graphite, as reported by Geim and Novoselov in 2004, has become a widely adopted approach for preparing other 2D materials, including TMDs.^[1; 2] This quick and convenient method can produce monolayer, few-layer, and multilayer thick TMDs crystals. Mechanical exfoliation relies on the principle that interlayer van der Waals forces within TMDs are weak and easily broken. Although common Scotch tape can exfoliate TMDs flakes, it is not ideal due to

substantial adhesive residue. Nitto blue tape, which has weak adhesion and minimal residue, is often preferred. Nitto tape can break the interlayer van der Waals forces of TMDs through multiple folding and unfolding actions, ensuring large, high-quality crystals due to its weak adhesive force and low residue.

To minimize adhesive residue during experiments, polydimethylsiloxane (PDMS) is typically used to transfer the exfoliated TMDs from the tape to the substrate. The adhesion force between TMDs crystals and various materials differs, with the following hierarchy: TMDs/SiO₂ > TMDs/PDMS > TMDs/Tape > TMDs/TMDs. Consequently, PDMS can easily transfer TMDs from tape to PDMS and then from PDMS to the SiO₂ surface of the target substrate. This principle is applied to the preparation of homojunctions and heterojunctions and is widely used in 2D material transfers.^[3] Figure 4.2 displays a comparison of optical images of monolayer MoS₂ exfoliated directly using Scotch tape (3M) and those exfoliated with PDMS assistance. It is evident that PDMS-assisted exfoliation results in fewer glue residues and produces larger, higher-quality crystals, making them ideal for fabricating electrical devices like FETs.

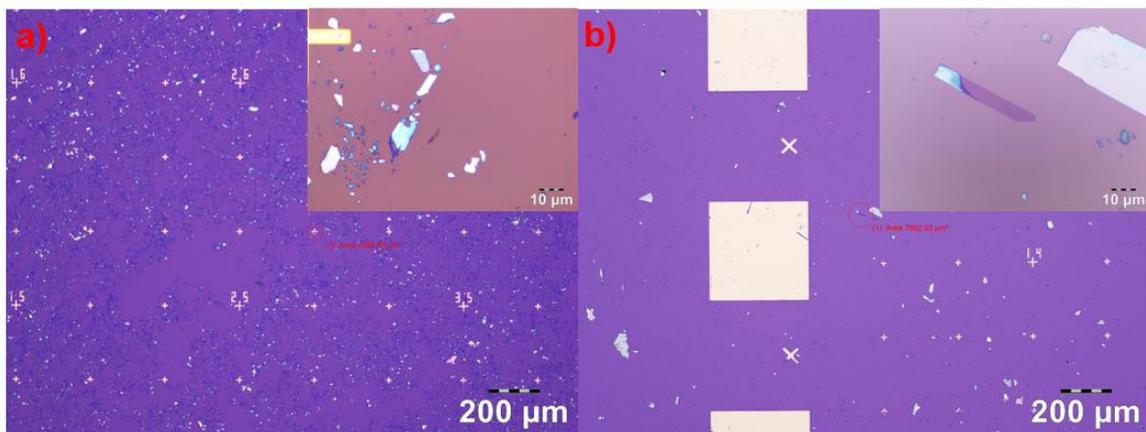


Figure 4.2 Comparison of optical images of monolayer MoS₂ exfoliated directly using Scotch tape (a) and exfoliated with PDMS assistance (b). Insets are a high-magnification picture of MoS₂ monolayer crystal obtained by this method.

In this thesis, bulk MoS₂ and WSe₂ crystals, grown using the chemical vapor transport (CVT) method, were purchased from SPI (United States) and HQ Graphene (Netherlands), respectively. We first peeled bulk crystals into thin layers with Nitto tape, and then obtained

monolayer or few-layer crystals by folding and unfolding the tape multiple times. Finally, the TMDs crystals were transferred to the silicon substrate using PDMS. The exfoliated crystals were identified under the bright field of an optical microscope. As TMD crystals with varying thicknesses (number of layers) display distinct contrasts under the bright field of an optical microscope, single-layer, few-layer, and multi-layer crystals can be easily distinguished.^[4; 5] Additionally, single-layer TMDs crystals generally exhibit photoluminescence (PL), enabling further validation of single-layer crystals using a microscope with PL functionality. Figure 4.3 shows the optical images of mechanically exfoliated MoS₂ with different layers, and the single-layer MoS₂ can be readily identified using optical microscopy.

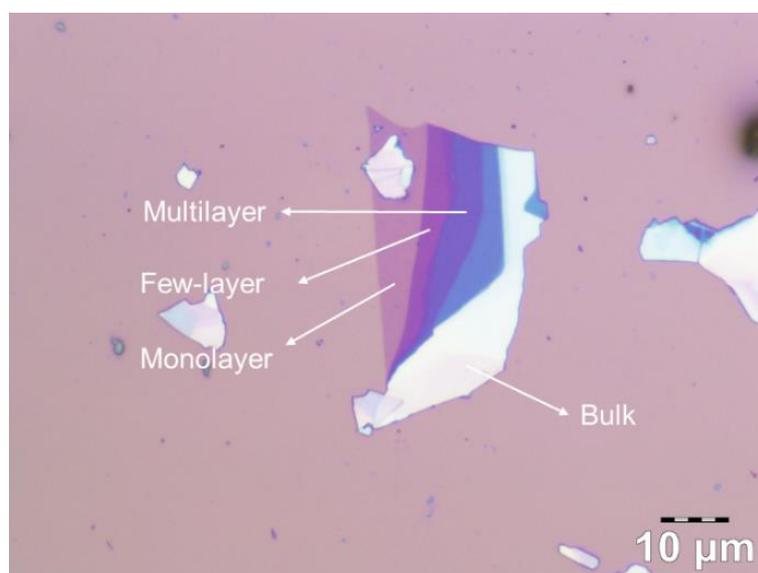


Figure 4.3 Optical image of mechanical exfoliated MoS₂ with different layers on Si/SiO₂ substrate.

4.2.2.2 Chemical vapor deposition (CVD) grown flakes transfer

Triangular monolayer TMDs crystals grown by chemical vapor deposition (CVD) on sapphire substrates were purchased from Six Carbon Technology (China). As SiO₂ is not an ideal substrate for CVD growth of TMDs crystals, they are typically grown on sapphire substrates, necessitating their transfer to silicon wafer surfaces for device fabrication. Figure 4.4 illustrates the standard transfer procedure for CVD-grown TMDs crystals from sapphire to Si/SiO₂ substrates. Initially, a polystyrene (PS) film (60 mg/mL, dissolved in toluene) was spin-coated onto the sapphire substrate containing CVD flakes, followed by

leaving it on the water surface for 20 min. After the solvent evaporation, the PS film was peeled off from the sapphire with the aid of a tweezer, and the PS film with CVD flakes floated on the water surface due to water's surface tension. The pre-cleaned wafer was then submerged in water to fish the PS film. Once the sample was transferred, a majority of the water was removed from its surface before heating to eliminate residual water and stabilize the sample (60 °C soft bake for 20 min, followed by a 90 °C bake for 30 min). The stabilized sample was subsequently immersed in a 60 °C toluene solution overnight to dissolve the surface PS film. Finally, the sample was extracted, and the solvent blown dry, yielding CVD-grown TMDs flakes on the Si/SiO₂ surface. Figure 4.5 displays optical images of CVD-grown TMDs flakes transferred onto SiO₂ surfaces.

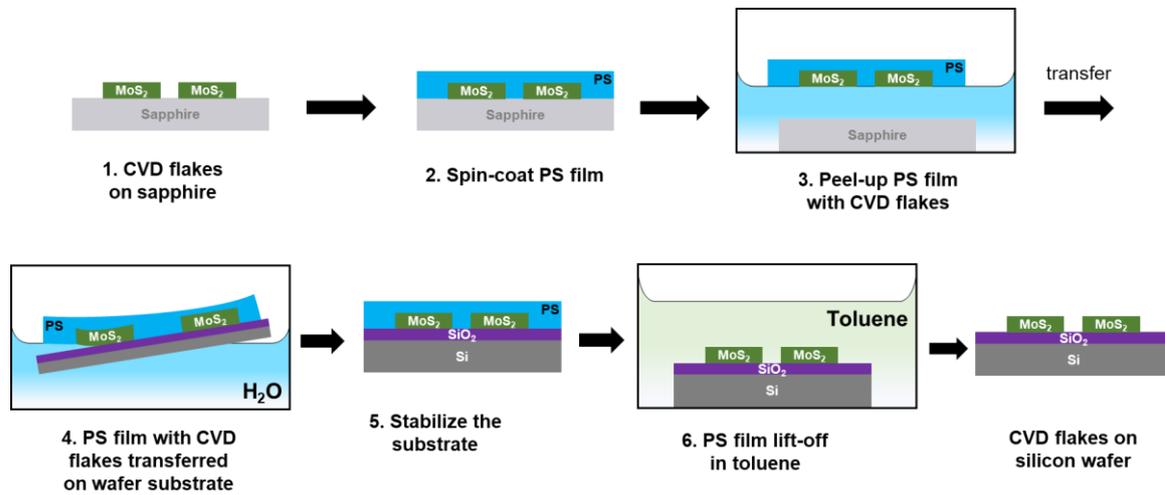


Figure 4.4 Process flow of CVD grown flakes transfer from sapphire to Si/SiO₂ substrate.

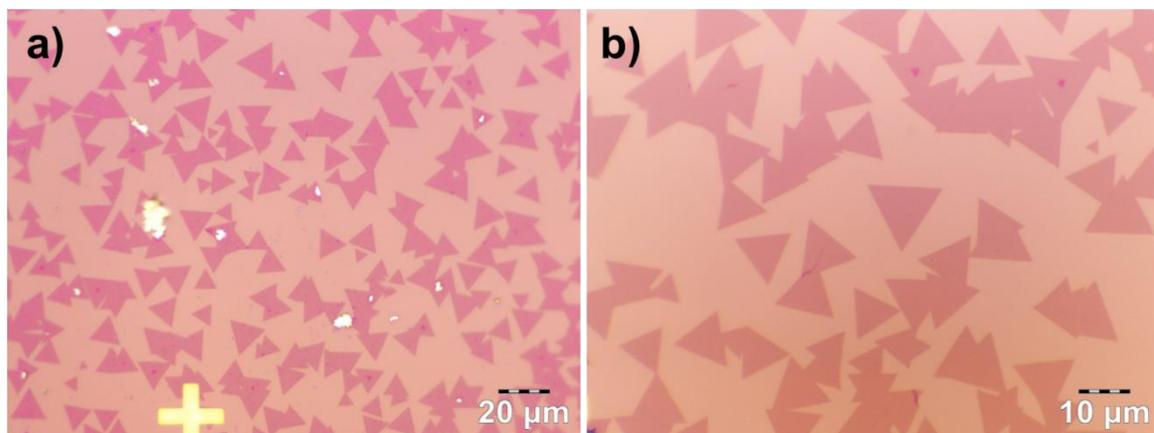


Figure 4.5 Optical image of CVD-grown triangular flakes on Si/SiO₂ substrate.

4.2.2.3 Sulfur-vacancy defects creation

Mechanically exfoliated TMDs crystals are unsuitable for covalent functionalization of molecules due to their insufficient surface defects. Consequently, defect engineering has been devised as a strategy for generating defects on TMDs crystals surface.^[6-9] Theoretical studies indicate that the Mo-S bond exhibits the lowest stability within the structure, and when ambient energy increases, the Mo-S bond breaks, enabling sulfur atoms to escape the surface.^[10; 11] Various methods for modulating the defect density of chalcogen vacancies have been reported, including high-temperature thermal annealing^[12; 13], ion irradiation/bombardment^[12; 14; 15], electron irradiation^[16], and plasma treatments^[17; 18], etc.

In this thesis, we employ the simplest high-temperature annealing method to create defects on monolayer MoS₂ surface. During defect creation process, the monolayer MoS₂ was treated on a hot plate at 300°C for an hour inside the glovebox to create sulfur-vacancy defects.

4.3.2.4 Functionalization of defects contained MoS₂

In this thesis, the TMDs functionalization relies on solution-processed molecular self-assembly, a widely used approach for molecular functionalization of TMDs. Molecules can attach to TMDs surface through physisorption or chemisorption. We utilized organic thiol-containing molecules covalently attached to the defective MoS₂ surface. During the functionalization process, the defective MoS₂ sample was immersed in a beaker containing a solution of thiol-containing molecules. Molecules interacted with MoS₂ to form a covalently self-assembled molecular layer. Although an excess of molecules would lead to physisorbed multilayer molecules, excess physisorbed molecules were removed through multiple washes with ample solvent, as confirmed by XPS characterization.

4.3 Device fabrication

In this thesis, we employ two techniques, i.e., photolithography and dry transfer, to fabricate TMDs-based FETs, diodes, and logic inverter devices, as detailed in the subsequent paragraphs.

4.3.1 Photolithography

Photolithography, a widely used microfabrication technique, is extensively employed in the fabrication of chips. Figure 4.6 demonstrates the standard photolithography fabrication process, conducted in an ultra-clean room. First, a photoresist layer is spin-coated onto the sample surface with TMDs (3000r/s for 45 s, Figure 4.6b). In this thesis, a positive photoresist (AZ1505) was utilized. Second, the sample is heated on a hot plate at 120 °C for 1 min, and the pre-designed patterned area is exposed using a lithography machine with the desired exposure dose of UV light (Figure 4.6c). Third, after exposure, the sample is immersed in the developer for 15 s, followed by immediate immersion in deionized water, and finally blown dry with a nitrogen gun (Figure 4.6d). Fourth, the post-lithography sample is placed in an inorganic evaporator, and the target metal electrode is thermally deposited in a high vacuum environment (maintaining vacuum below 10^{-7} mbar) (Figure 4.6e). Fifth, the sample with deposited electrode must be developed to remove the extra photoresist. Warm acetone (60 °C) is employed as the solvent for development. After development, the sample retains only the metal electrodes in the patterned area, producing a device (Figure 4.6f). Figure 4.7 presents an optical image of a FET device fabricated using photolithography.

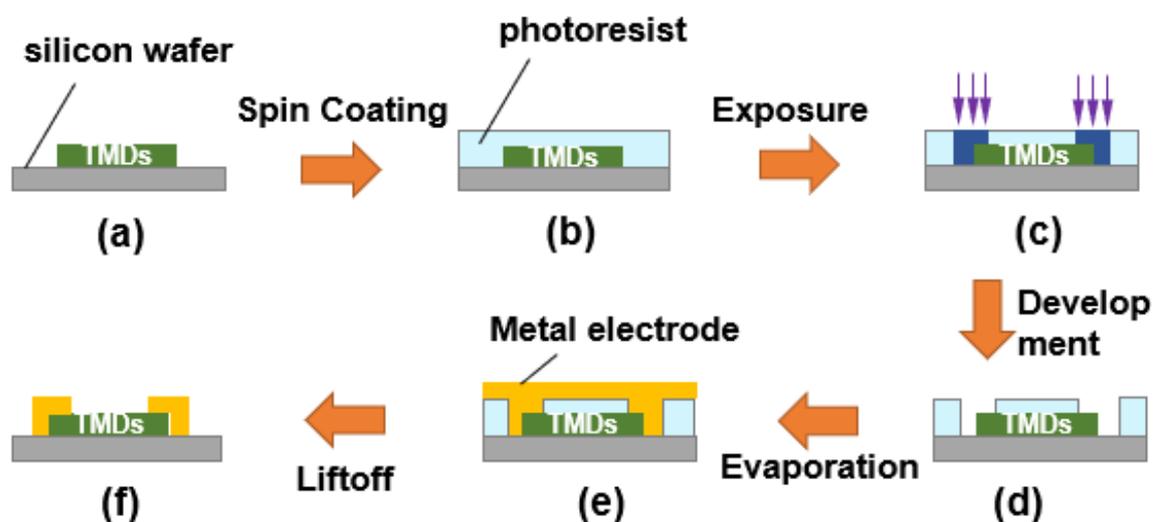


Figure 4.6 Flow diagram for the fabrication process of FETs by photolithography.

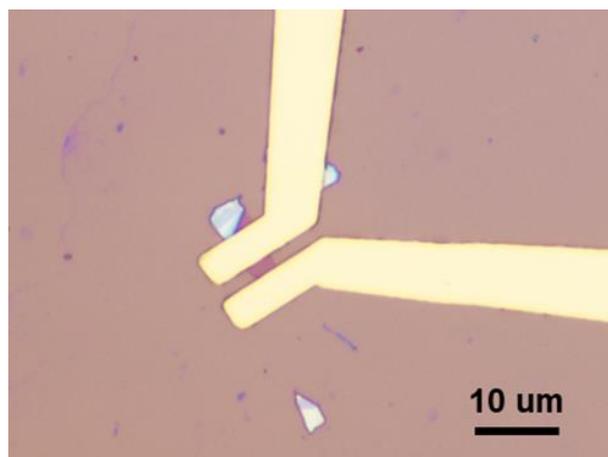


Figure 4.7 Optical image of FET device fabricated using photolithography.

4.3.2 Dry transfer

Photolithography (or electron beam photolithography), as a mature method for manufacturing micro-nano devices, is extensively applied in the production of various processor chips, sensors, logic circuits, and other fields.^[19-21] Currently, this technique is used to create chips for commercial devices (e.g., cell phones, computers, etc.). However, when applied to TMDs, additional problems arise. When metal electrodes are thermally deposited on TMDs surfaces, the thermal energy damages the crystal lattice at or near the interface due to TMDs' atomically thin crystals and dangling-bond-free atomically flat surfaces, resulting in the formation of metal-induced gap states between the electrodes and the semiconductor.^[22-25] This is also considered one of the primary causes for the emergence of Fermi level pinning. Therefore, to overcome these issues, the dry transfer technique was developed, enabling the creation of devices with van der Waals (vdW) contact between the electrodes and the semiconductor.^[23; 26-33] In this thesis, we also employed a dry transfer technique to fabricate vdW contact FET devices. This technique encompasses two methods: a PDMS-assisted dry transfer technique and a direct dry transfer technique.

4.3.2.1 PDMS-assisted dry transfer

Polydimethylsiloxane (PDMS)-assisted dry transfer technique is employed to fabricate FETs with functionalized top electrodes. Figure 4.8 and Figure 4.9 display the schematic and optical flow diagrams of the FET devices fabrication process, respectively. Initially,

the functionalized silicon wafer with OTS as sacrificial substrate to render the substrate hydrophobic and weaken the adhesion of subsequent thermally deposited metals, facilitating mechanical desorption and transfer. Patterned electrodes are then deposited onto the sacrificial silicon substrate surface by thermal evaporation through a patterned mask. The choice to functionalize the electrodes depends on the requirements. The (functionalized) Au electrode is stripped from the sacrificial substrate using a mechanical probe with a gallium-indium alloy coated tip (Figure 4.9 b and c show the electrode during stripping). The stripped electrode is transferred to the PDMS surface as one of the source/drain (S/D) electrodes of the FETs, and another electrode is transferred alongside the first electrode using the same method, serving as the other S/D electrode of the FETs (Figures 4.9 d and e show the electrodes during transferring, while Figures 4.8 d and 4.9 f–g depict the schematic and optical diagrams of the S/D electrodes on PDMS, respectively).

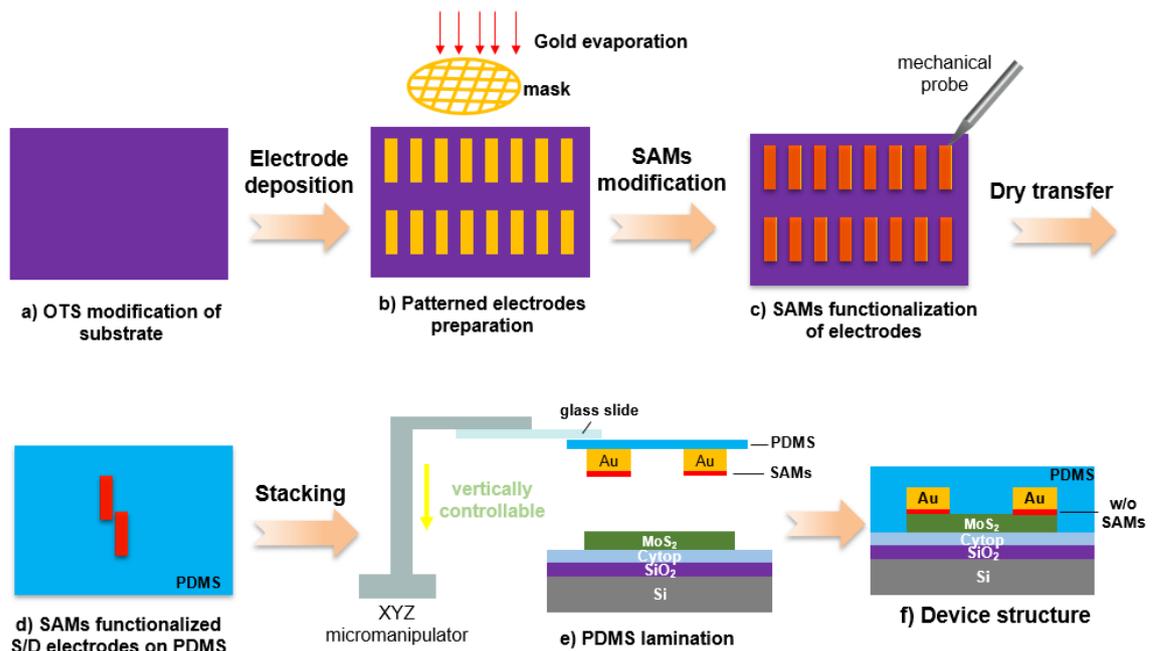


Figure 4.8 Flow diagram for the fabrication process of FETs by PDMS-assisted dry transfer.

Afterward, the PDMS film with electrodes is flipped and adhered to the slide, which is fixed on the transfer platform (Figure 4.8e). The transfer platform allows for control of the PDMS film in the three dimensions of XYZ. The prefabricated PDMS film with S/D electrodes is laminated onto the TMDs crystal surface under the microscope to fabricate

the FETs with bottom-gate top-contact (functionalized electrode) configuration. The PDMS film can be employed as an encapsulation layer to encapsulate and protect the device. The fabricated devices are annealed under vacuum to remove adsorbates prior to testing. Figures 4.8 f and 4.9 h display the schematic diagram and optical image of the FET devices fabricated using this technique, respectively. Notably, this technique can be employed to prepare FET devices with arbitrary channel length. As illustrated in Figure 4.10, the channel length is adjusted by controlling the distance from the first electrode during the transfer of the second electrode.

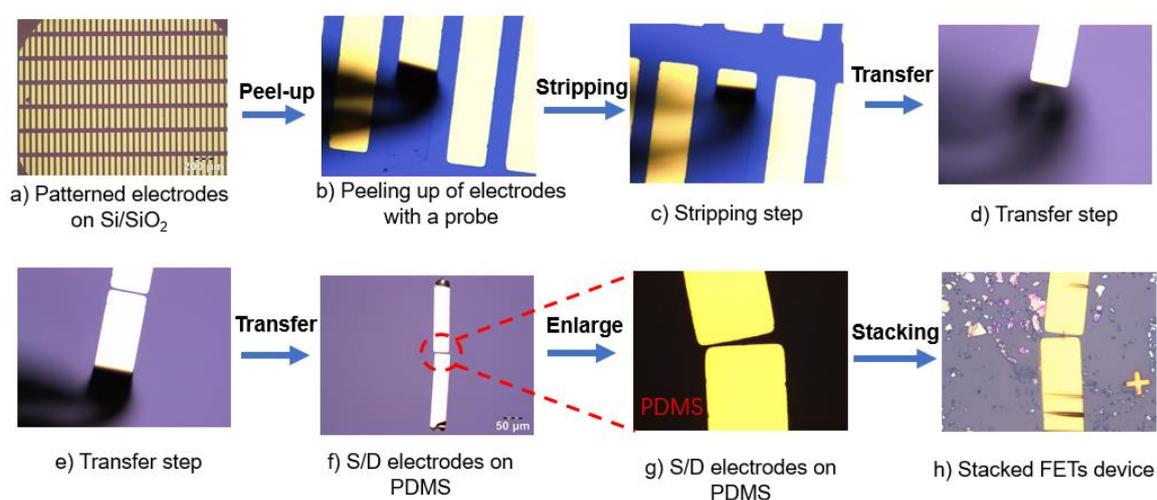


Figure 4.9 Optical flow diagram for fabricating FETs by PDMS-assisted dry transfer.

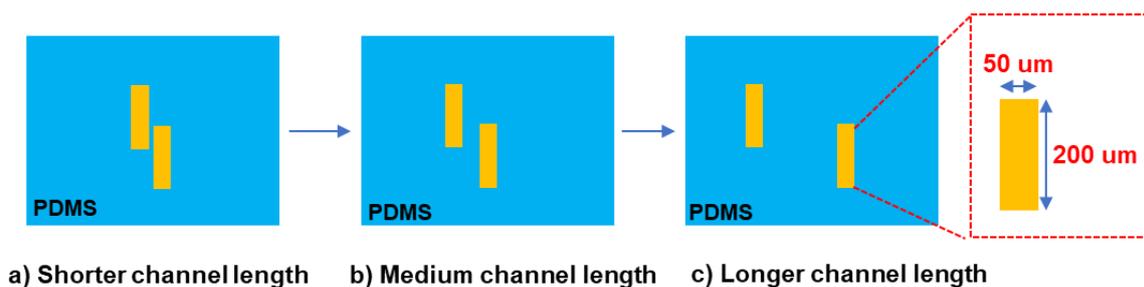


Figure 4.10 Schematic diagram of channel length dimensions of FETs fabricated by PDMS-assisted dry transfer.

Moreover, this strategy offers unique advantages in the preparation of asymmetric electrode devices. The fabrication of asymmetric electrodes, as reported in previous literature, necessitated multi-step photolithography, and for SAMs-modified asymmetric electrode devices, the process was even more intricate. In this thesis, we demonstrate that SAMs-

modified asymmetric electrode devices can be fabricated by merely transferring two electrodes functionalized by two different SAMs onto PDMS film. This will be introduced in detail in Chapter 6.

4.3.2.2 Direct dry transfer

The electrodes of FETs fabricated by PDMS-assisted dry transfer technique described above exhibit several advantages, the most distinctive being the ability to be functionalized with SAMs or other materials to create functionalized FET devices with a top contact configuration. However, a notable drawback is the relatively large surface roughness of the electrode (approximately 2 nm) and the inevitable contact resistance when interfacing with the TMDs crystal. Therefore, for devices not requiring SAMs functionalized electrodes, we employed the direct dry transfer technique to fabricate vdW contacted FET devices, since the atomically flat bottom surface of the electrode provides superior contact with the semiconductor crystal compared to the rough top surface.

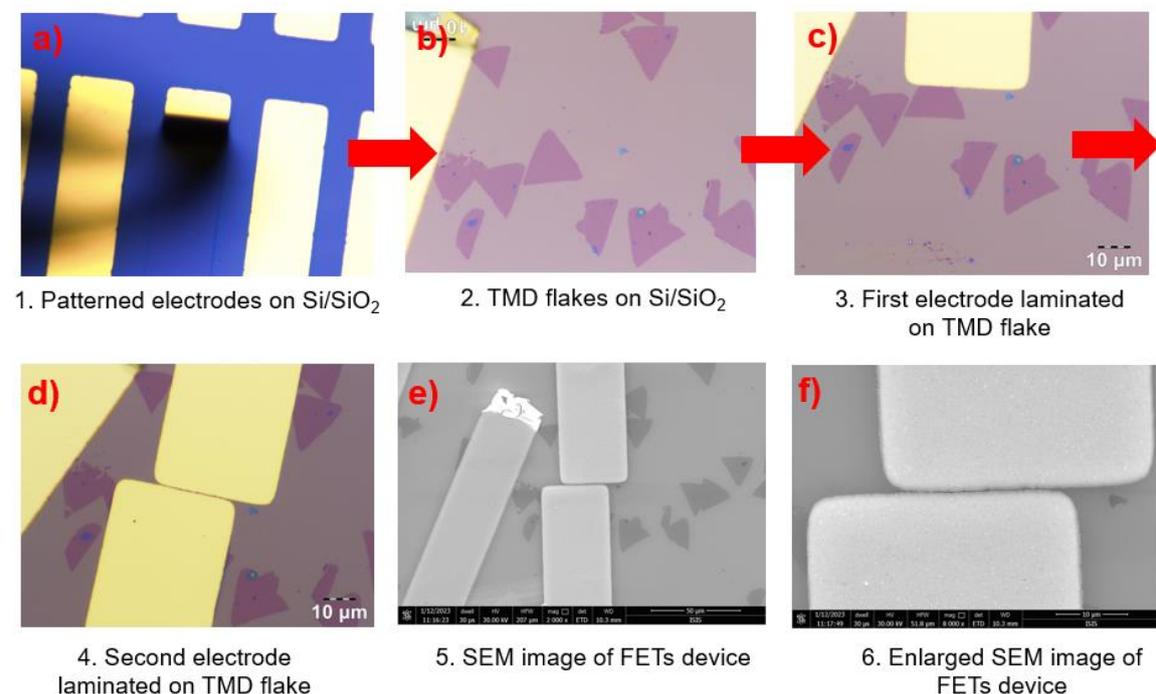


Figure 4.11 Optical flow diagram for fabricating FETs by direct dry transfer.

Figure 4.11 displays the optical flow diagram of the direct dry transfer technique. This method is akin to the PDMS-assisted dry transfer technique introduced in section 4.3.2.1.

Initially, a patterned metal electrode is prepared on a sacrificial substrate, and then the electrodes are picked up by a mechanical probe under an optical microscope and directly transferred to the surface of TMDs crystal. The channel size (length) is controlled by adjusting the distance between the two electrodes. Figures 4.11 d, e and f present the optical and SEM images of the fabricated FET devices, respectively. We utilized this technique to fabricate FETs with the narrowest channel length amounting to ca. 7 nm.

For the top-contact device functionalized with an auxiliary layer, we achieved this by depositing an auxiliary material before preparing patterned electrodes on a sacrificial substrate. The details will be introduced in chapter 7.

Compared with the reported techniques for preparing vdW contact devices with transfer electrodes, our method offers numerous advantages. First, it does not rely on photolithography, significantly reducing the manufacturing cost of the device. Second, the absence of solvents during the entire process eliminates the possibility of contamination and simplifies the preparation of diodes with asymmetric electrodes and logic circuits.

4.3.3 Device annealing process

Since the devices fabrication needs to be carried out in an atmospheric environment, pollutants will be adsorbed during the process, which can impact the physical and chemical properties of TMDs. Moreover, polymer or other solvent residues during the lithography process can lead to TMDs doping, adversely affecting subsequent device performance studies. Therefore, the annealing process is crucial for the device. In this thesis, the annealing process is conducted in a high vacuum (10^{-7} mbar) apparatus, with the target temperature set as required. Typically, devices containing organic molecules in the system undergo the annealing process under mild conditions. After annealing, pollutants, adsorbed water, oxygen, and other adsorbents are eliminated, and the contact between the electrode and semiconductor is enhanced, which is advantageous for obtaining the true performance of the TMDs device.

4.4 Characterization techniques

4.4.1 Optical microscope

All optical images in this thesis were recorded with an Olympus BX51 optical microscope equipped with PL function and polarizing function.

4.4.2 Atomic force microscopy (AFM)

Atomic Force Microscopy (AFM) images in tapping mode were obtained using a Bruker Dimension Icon set-up operating in air, in tapping mode. The tip model is TESPA-V2, and the tip stiffness K is 42 N m^{-1} .

4.4.3 Raman and photoluminescence (PL) spectroscopy

Raman and Photoluminescence (PL) spectra were carried out in atmosphere by Renishaw inVia spectrometer equipped with 532 nm laser. For PL, a grating of 300 l/mm is employed while for Raman spectroscopy, a grating of 2400 l/mm is employed. The wavenumber (energy) resolution is about 1.25 cm^{-1} ($\approx 1 \text{ meV}$).

4.4.4 X-ray photoelectron spectroscopy (XPS)

X-ray Photoelectron Spectroscopy (XPS) measurements were carried out with a Thermo Scientific K-Alpha X-ray photoelectron spectrometer with a basic chamber pressure of $\approx 10^{-8}$ mbar and an Al anode as the X-ray source (x-ray radiation photon energy of 1486.6 eV). Spot sizes of 400 μm and pass energies of 200.00 eV for wide energy scans and 10.00–20.00 eV for scans were used. All XPS spectra were calibrated using the C 1s peak at 284.8 eV as a reference.

4.4.5 Photoelectron spectroscopy in ambient conditions (PESA)

The Work Function (WF) was measured by Photoelectron Yield Spectroscopy in Air (PYSA), using an AC-2 Photoelectron Spectrometer (Riken-Keiki Co.). The ambient photoelectron yield measurements were performed by sampling in each measurement an area of about 4 mm^2 (beam size) with an ultraviolet (UV) incident light power of 300 nW

with a counting time of 10 seconds per point.

4.4.6 EGaIn molecular junction test



Figure 4.12 Sequential photographs showing the formation of the EGaIn tip.^[34]

Molecular junctions based on liquid metal eutectic gallium-indium (EGaIn) have been widely used in characterizing the electrical conductivity of SAMs.^[35-41] The preparation process is illustrated in Figure 4.12.^[34] First, the needle of the syringe containing EGaIn is placed near the sacrificial layer (gold substrate without the modified molecular layer). The EGaIn droplet is extruded to contact with the sacrificial substrate surface, and the syringe is raised until the droplet separates from the sacrificial substrate, forming a conical tip. The formed tip is moved to the SAMs surface until contact is made, creating a SAM molecular junction device. As the surface of EGaIn is easily oxidized to form a layer of Ga_2O_3 , it can effectively prevent SAMs short circuit and establish a stable molecular junction.

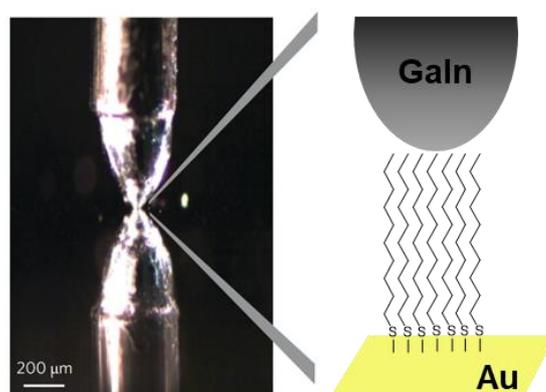


Figure 4.13 Optical picture of the EGaIn molecular junction during the test and the enlarged schematic diagram of the contact area.^[41]

During testing, the two cables of the source meter are connected to the metal needle of the syringe and the gold substrate, respectively (as shown in Figure 4.13). After constructing the setup, we initially tested it with a simple alkyl SAMs, and the electrical results are presented in Figure 4.14. As observed, as the SAMs molecule grows from C10 to C18, the molecular junction current significantly decreases and exhibits good repeatability.

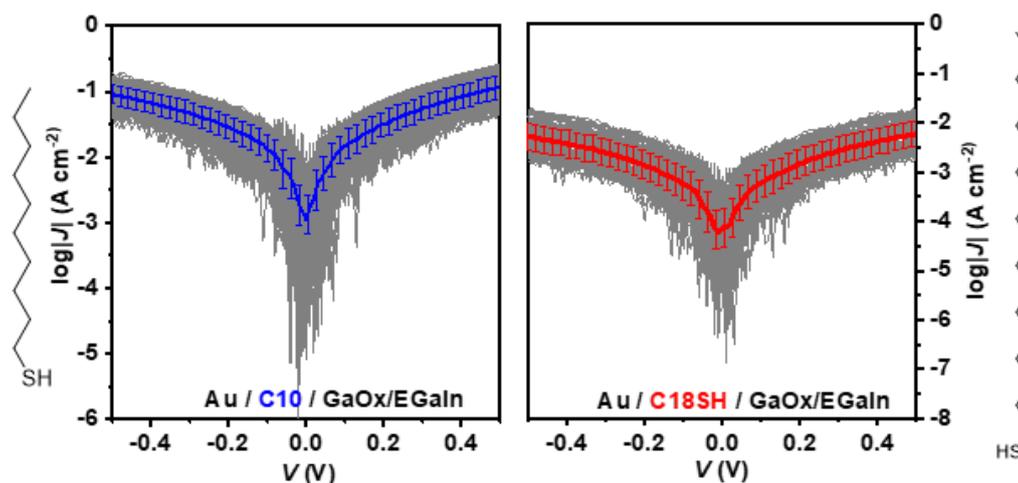


Figure 4.14 Molecular structure of C10 and C18 and electrical tunneling current of the C10 and C18 SAMs junctions on Au using an EGaIn droplet. The gray curves show the trace and retrace of more than 300 J(V). The blue and red line with logstandard deviations represent the average value.

4.4.7 Contact angle (CA)

Contact Angle (CA) measurements were performed on the Kruss DSA100S droplet shape analyzer. 2 μ L deionized water was dropped on the sample surface with a micro-syringe, the CA values were acquired in Young Laplace fitting method.

4.4.8 Scanning electron microscope (SEM)

The morphology and channel size of the narrow-channel FET devices in Chapter 7 were characterized with field-emission scanning electron microscope (SEM) FEI Quanta FEG 250 instrument S3 (FEI corporate, Hillsboro, Oregon, USA).

4.4.9 Electrical characterization

In this thesis, electrical tests of FETs are performed on a probe station situated in a nitrogen-

filled glove box under dark conditions, as displayed in Figure 4.15. The sample is placed directly on the metal support as back-gate and connected to the gate channel of the source meter. The position of the probe is controlled by a micromanipulator. The FET devices are electrically characterized by a Keithley dual-channel 2636A source meter.



Figure 4.15 A probe station photo in the glovebox.

Temperature dependent measurements are performed in a cryogenic probe station (Janis-CCR5-2) using a semiconductor parameter analyzer (Keithley 4200) with a vacuum degree of approximately 5×10^{-5} mbar.

4.4.10 DFT calculations

Charge density calculations were performed by using the Vienna ab-initio Simulation Package (VASP)^[42; 43]. The Perdew-Burke-Ernzerhof (PBE)^[44] functional was used to describe electron exchange and correlation. DFT-D2 method of Grimme^[45] was used in order to describe van der Waals forces. The Bader technique^[46] was adopted in order to determine the charge transfer in the structure. The kinetic energy cut-off for plane-wave expansion was set to 400 eV and the energy was minimized until its variation in the following steps became 10^{-4} eV. The Gaussian smearing method was employed for the total energy calculations and the width of the smearing was chosen as 0.05 eV. Total Hellmann-Feynman forces in the until was reduced to 10^{-3} eV/Å. (1,1,1) Γ -centered k-point samplings were used for the unit cells. 3000 grid points were used for electronic density of states

calculations.

4.5 References

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Chapter 5 Defect Engineering in Monolayer MoS₂: Towards Isomer Discrimination via Molecular Functionalization

The all-surface nature of two-dimensional (2D) materials renders them highly sensitive to environmental changes, enabling on-demand tailoring of their physical properties.^[1-3] Transition metal dichalcogenides (TMDCs), such as 2H molybdenum disulfide (MoS₂), can be used as sensory material capable to discriminate molecules possessing a similar structure with a high sensitivity.^[4-6] Among them, the identification of isomers represents an unexplored and highly challenging case. Here, we demonstrate that chemical functionalization of defect engineered monolayer MoS₂ enables isomers discrimination via a field-effect transistor read out. A multiscale characterization comprising X-ray photoelectron spectroscopy, Raman spectroscopy, photoluminescence (PL) spectroscopy, electrical measurement and theoretical calculations revealed that monolayer MoS₂ exhibits remarkable sensitivity to the differences in the dipolar nature of molecules arising from their chemical structure such as the one in difluorobenzenethiol isomers allowing their precise recognition. Our findings underscore the potential of 2D materials for molecular discrimination purposes, in particular for the identification of complex isomers.

5.1 Introduction

Over the last decade, two-dimensional (2D) transition metal dichalcogenides (TMDCs) have captured significant attention because of their unique electronic, optical, and mechanical properties.^[7-10] Among them, molybdenum disulfide (MoS₂) has emerged as a highly promising material for next-generation (opto-)electronic devices due to its exceptional characteristics, including high electron mobility, high $I_{\text{on}}/I_{\text{off}}$ ratio, tunable bandgap (from indirect bandgap of bulk material to direct bandgap of monolayer), and strong light-matter interactions.^[11-13] Furthermore, the weak interlayer interactions, dangling-bond-free atomically flat surfaces, and van der Waals bonding between adjacent

layers of MoS₂ makes it an ideal platform for developing atomically thin devices, such as photodetectors, photodiodes, and heterojunction devices.^[14; 15]

The combination with organic molecules has been proven to be an effective method to adjust the properties of MoS₂ via doping as a route to impart responsiveness to optical stimuli and chemical sensing capabilities as well as for realizing complementary metal–oxide–semiconductor circuits.^[1; 16-19] Defects in MoS₂ crystals are extremely reactive sites for the chemisorption of molecules enabling the generation of strong chemical bonds between MoS₂ and organic compounds.^[20] This method has several advantages, such as the protocol's simplicity, controllable number of bonded molecules and higher stability compared with van der Waals interaction of physical adsorption. These advantages have rendered chemisorption an attractive approach for exploring the effect of molecular functionalization of MoS₂ by developing novel functions for various applications.

Unfortunately, mechanically exfoliated MoS₂ crystals exhibit very few defects (defect concentration < 2%), making them inappropriate for chemical bonding with molecules.^[21; 22] Conversely, chemically vapor-deposited (CVD, defect concentration defect concentration $\leq 3\%$)^[23; 24] or chemically (liquid) exfoliated MoS₂ (defect concentration > 3%)^[25; 26] are more suitable for chemisorption strategies, but their excessively abundant defects and traps, disordered structure and inevitable ion residues lead to lower carrier mobility, lower $I_{\text{on}}/I_{\text{off}}$ ratios and overall poorer device performance, ultimately limiting their application in opto-electronic devices.^[27-29] To overcome this problem, defect engineering has been proposed as a strategy to create defects on the surface of TMDCs to tailor their properties and enable device chemical functionalization.^[4; 30-33] According to theoretical studies, the Mo-S bond has the lowest stability within the structure. When subjected to an external etching source, the Mo-S bond will break, allowing sulfur atoms to escape from the surface.^[34; 35] Several approaches have been reported for modulating the defect density of chalcogen vacancies, including high-temperature thermal annealing^[36; 37], ion irradiation/bombardment^[21; 36; 38], electron irradiation^[39], and plasma treatments^[40; 41], etc. These defects can act as active sites for the hydrogen evolution reaction (HER), improving the catalytic activity of MoS₂ in HER.^[42] Importantly, the controlled generation

of defects in the MoS₂ nanosheets does not irreversibly damage their crystal structure: defects healing via molecular functionalization makes it possible to recover the material's electronic and optical properties.^[16; 43; 44] In fact, these chalcogenide vacancies serve as anchoring sites for surface functionalization, which can enable covalent grafting of thiolated molecules yielding a modulation of the chemical, vibrational, electronic, optical, and magnetic properties of the 2D crystals.^[30; 45] The remarkable sensitivity of defect-containing TMDCs to their environment implies that even subtle modifications on their surface can significantly influence their intrinsic properties, rendering them highly sensitive for the identification of complex yet similar molecules, including isomers. The very similar properties of isomers make their discrimination unattainable with conventional discrimination methods.^[46] However, despite this potential, the dearth of reports on isomer recognition by TMDCs in the literature underscores a promising area for future research and development.

Here, we explored the application of defect engineering in monolayer MoS₂ for isomer discrimination. We exposed field-effect transistors (FETs) based on mechanically exfoliated monolayer MoS₂ to high-temperature treatment to create S-vacancy defects in the channel region. The devices were then chemically functionalized with thiolated difluorobenzenethiol isomers to enable their identification. To gain an exhaustive insight and control over this functionalization process, a comprehensive multiscale study of the optical, optoelectronic, electrical properties and theoretical calculations of MoS₂ before and after functionalization with isomers was performed.

5.2 Experimental methods

5.2.1 Materials and instruments

Materials: The MoS₂ bulk crystal semiconductor was purchased from SPI. The 3,5-difluorobenzenethiol (35DFBT) and 2,6-difluorobenzenethiol (26DFBT) were purchased from Sigma-Aldrich.

AFM Measurement: Tapping Mode Atomic Force Microscopy (AFM) imaging was

executed by means of a Bruker Dimension Icon set-up operating in air. The tip model is TESPA-V2, and the tip stiffness K is 42 N m^{-1} . R_{RMS} from AFM topographical images was estimated on flake regions of $0.5 \times 0.5 \text{ }\mu\text{m}^2$.

XPS Measurement: X-ray Photoelectron Spectroscopy (XPS) measurements were carried out with a Thermo Scientific K-Alpha X-ray photoelectron spectrometer with a basic chamber pressure of $\approx 10^{-9}$ mbar and an Al anode as the X-ray source (x-ray radiation of 1486 eV). Spot sizes of $400 \text{ }\mu\text{m}$ and pass energies of 200.00 eV for wide energy scans and 10.00–20.00 eV for scans were used. All XPS spectra were calibrated using the C 1s peak at 284.8 eV as a reference.

Raman and PL Spectroscopy: Raman and Photoluminescence (PL) spectra were carried out in atmosphere by Renishaw inVia spectrometer equipped with 532 nm laser. The excitation power was kept no more than 1 mW to avoid local heating damage effects. The wavenumber (energy) resolution is about 1.25 cm^{-1} ($\approx 1 \text{ meV}$).

Work Function Measurement: The Work Function (WF) was measured by Photoelectron Yield Spectroscopy in Air (PYSA), using an AC-2 Photoelectron Spectrometer (Riken-Keiki Co.). The ambient photoelectron yield measurements were performed by sampling in each measurement an area of about 4 mm^2 (beam size) with an ultraviolet (UV) incident light power of 300 nW with a counting time of 10 seconds per point.

Electrical Measurement: The devices were electrically characterized by a Keithley dual channel 2636A sourcemeter in a three-terminal configuration with the back gate contacted through an underlying metal plate in a glovebox filled with nitrogen in dark conditions.

5.2.2 Device fabrication, defects creation and functionalization

MoS₂ monolayer flakes were mechanically exfoliated from a bulk crystal using Nitto scotch-tape, and then a PDMS film (purchased from gel-pack) was used to transfer the crystals from the tape on thermally oxidized silicon substrates covered with a 270 nm-thick SiO₂ layer as dielectrics (Fraunhofer Institute IPMS, $\rho_{\text{Si}} \approx 0.001 \text{ }\Omega\cdot\text{cm}$) to minimize glue residue. Their thickness was monitored by optical microscope combined with Raman

spectroscopy and AFM. Back-gated FETs were fabricated by conventional photolithography method, and the metal electrodes (0.2 nm Cr and 60 nm Au) were thermally evaporated onto the patterned substrate. Then a mild lift-off process was carried out in acetone (60 °C), and the as prepared samples were annealed at 120 °C for 6 h in a high-vacuum chamber to improve the contacts and remove absorbents, such as water etc. During defects creation process, as-prepared devices were treated on a hot plate at 300°C for an hour inside the glovebox to create S-defects in the channel. During the isomeric functionalization process, defects contained MoS₂ monolayer samples were immersed into 1 mM DFBT in ethanol solution for 12 h, followed by rinsing with a large amount of ethanol and thermally annealed in vacuum at 100 °C to remove surface physisorbed molecules, evaporate solvent and stabilize system.

5.2.3 Calculation of sulfur vacancy concentration

The calculation of S-vacancy concentration (V_S) has been widely reported, here we adopt the method reported in the literature:^[21; 37; 47]

S-vacancy concentration in XPS S 2p core level spectra:

$$V_{S1} = \frac{A_{ds}}{7A_{ds} + 6A_s} \quad (5 - 1)$$

where, A_{ds} is the area of the defect component in S 2p core level spectra. A_s is the area of the sulfur component in S 2p core level spectra without defect.

S defect concentration obtained in XPS Mo 3d core level spectra:

$$V_{S2} = \left(1 + \frac{r}{2}\right) \left(\frac{A_{dMo}}{6(A_{dMo} + A_{Mo})}\right) \quad (5 - 2)$$

where, r is the S/Mo stoichiometric ratio. A_{dMo} is the area of the defect component in Mo 3d core level spectra. A_{Mo} is the area of the Mo component in Mo 3d core level spectra without defect peaks areas and higher binding energy molybdenum oxide peak area.

Then, the sulfur vacancy concentration (V_S) was calculated using the following formula:

$$V_S = \frac{V_{S1} + V_{S2}}{2} \quad (5 - 3)$$

5.2.4 Computational details

DFT calculations were performed with the projector-augmented wave (PAW) basis set, as implemented in the VASP code^[48; 49]. Exchange and correlation effects were treated at the Perdew–Burke–Ernzerhof (PBE) level of theory and the dispersion forces by the Grimme correction (PBE+D2)^[50; 51]. Dipole moment correction was employed along the ‘c’ axis (Z direction & perpendicular to the MoS₂ surface) with a kinetic energy cut-off of 600 eV and using a Monkhorst-Pack sampling of 3×3×1 for the Brillouin zone (BZ) integration on a 4×4×1 supercell of MoS₂ monolayer with the vacuum space set to be 30 Å to avoid the interaction with periodic images. Geometries of pristine and defective (–3% V_S) MoS₂ surfaces, as well as the thiophenol adsorbed MoS₂-3%V_S were fully optimized prior to calculation of work functions. The same computational criteria were used for calculations at the hybrid level of theory (HSE06). Work function (ϕ) of (DF)BT functionalized MoS₂ surface containing -3% sulfur vacancies (MoS₂-3% V_S) is calculated as difference of Fermi energy (E_f) and the electrostatic potential at vacuum level (E_p). Fermi level (E_f) is set to the energy of valence band maximum at the GGA/PBE level of theory and to the center of electronic band gap at the HSE06 level of theory.

5.3 Results and discussions

The sample preparation process is illustrated in Figure 5.2. Monolayer MoS₂ flakes were mechanically exfoliated on a heavily doped silicon substrate capped by a 270 nm-thick thermally grown SiO₂ dielectric layer. The monolayer flakes were identified by optical microscopy with PL and confirmed by Raman spectroscopy and atomic force microscopy (AFM), the latter exhibiting a thickness of about 0.80 nm, consistent with previous reports (see optical micrograph and corresponding AFM height image in Figure 5.1).^[52]

Back-gate MoS₂ FETs were then fabricated using conventional photolithography and lift-off processes, and the electrodes were deposited with 0.2 nm Cr as an adhesion layer and 60 nm Au. To generate sulfur-vacancy (S-vacancy) defects, the device samples were

exposed to 300 °C for one hour. Then, the defective MoS₂ (d-MoS₂) sample was functionalized with thiolated molecules. Details of the experimental protocol can be found in the section of experimental methods. In particular, as prototypical systems, we have selected two isomers of difluorobenzenethiol, i.e., 2,6-difluorobenzenethiol (26DFBT) and 3,5-difluorobenzenethiol (35DFBT), possessing the identical chemical formula but different dipole moment orientation. Figure 5.2f depicts the chemical structures of these two isomers.

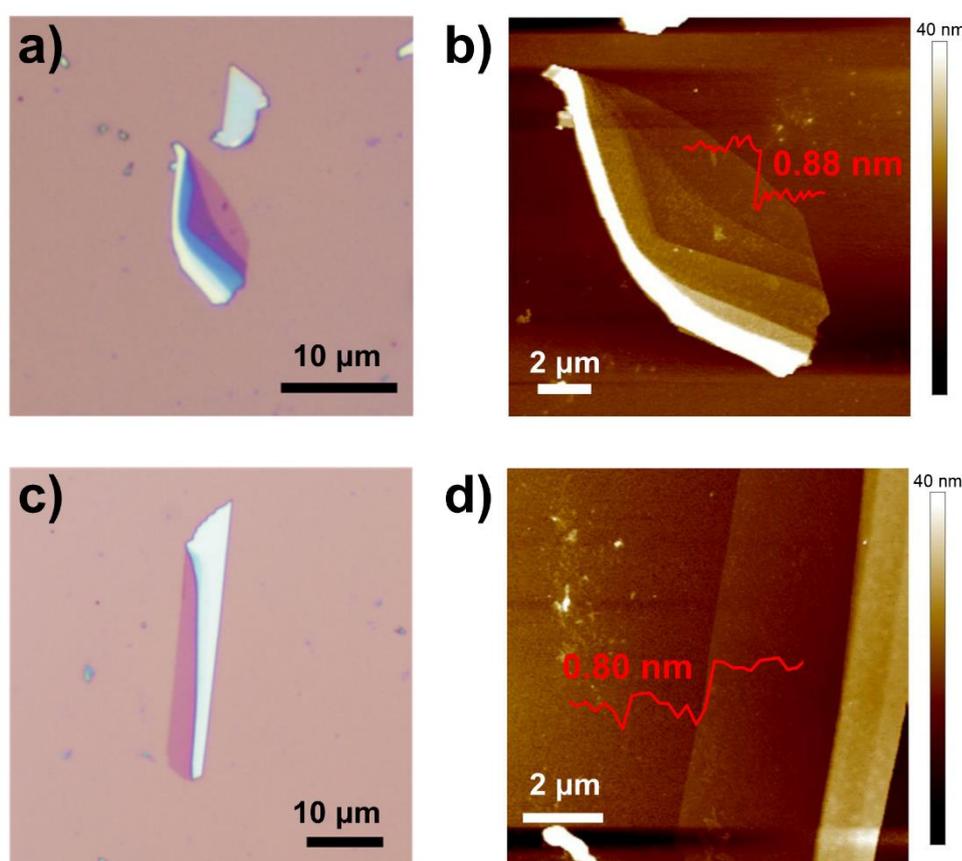


Figure 5.1 Optical image and corresponding AFM morphology image monolayer MoS₂ pristine flakes. These flakes correspond to figure 5.4 in main text. The R_{RMS} of these two monolayer MoS₂ surfaces are 0.48 nm for b) and 0.51 nm for d), respectively. The R_{RMS} was estimated on flake regions of $1.5 \times 1.5 \mu\text{m}^2$.

Upon MoS₂ functionalization, the different arrangement of F atoms in these molecules determines a dissimilar dipole moment orientation, resulting in distinct dipole-induced electrostatic gating manipulating the carrier density of the underlying 2D semiconductor.^[53]

^{54]} This provides a tool for isomer discrimination, which can be confirmed by the difference in secondary-electron cutoff as shown in Figure 5.3. Due to the different positions of the F substitutions, the molecule exhibits completely opposite properties.^[55] Because the two F atoms in 26DFBT are located adjacent to the thiol group, the strong upward dipole allows to shift the WF of Au from 4.88 eV to 4.45 eV, while the strong downward dipole 35DFBT molecule increased it to 5.27 eV. This demonstrates that despite their identical chemical formulas, there are differences in electronic properties that can be used for identification.

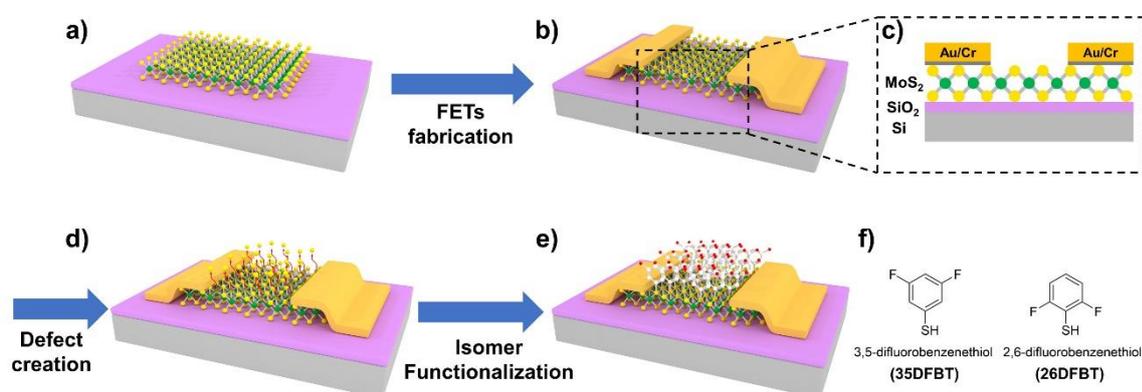


Figure 5.2 Schematic illustration of the preparation steps for the isomer functionalized FETs. a) Exfoliated monolayer MoS₂ flake on SiO₂/Si substrate. b) FET device fabricated by photolithography. c) Cross-sectional view of FETs. d) Defects induced on the surface of monolayer MoS₂ through defect engineering. e) Functionalization of monolayer MoS₂ semiconductors with isomers via self-assembled grafting. f) Chemical structure of the isomers (35DFBT and 26DFBT) used in this study.

Our methodology combines a variety of significant advantages. Firstly, we employ a monolayer MoS₂ crystal, which provides a notably more sensitive surface than few-layer or multilayer crystals. Secondly, high-temperature treatment was conducted in a glove box filled with inert gas in order to prevent extensive deterioration of monolayer MoS₂ crystals in the presence of air. Thirdly, in lieu of using traditional molecular modification techniques such as physical adsorption, vapor deposition and molecular coordination, we choose a chemically more controlled and robust solution based on the direct formation of covalent bonds between molecules and MoS₂ crystals. Fourthly, compared with previous work on molecular doping, we utilize structurally similar isomers whose dipole differences enable

discrimination. The devised approach based on the TMDCs controlled functionalization for the identification of isomers is universal. Lastly, the combined optical, optoelectronic and electrical characterizations provide an exhaustive and clear evidence of the dipole-induced doping effects brought about by the covalent modification of isomers, representing a notable advancement in TMDCs functionalization for molecular identification purposes.

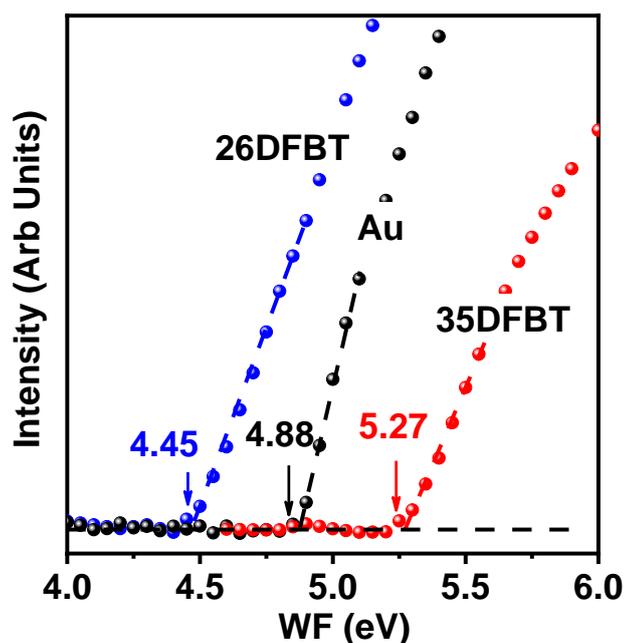


Figure 5.3 Secondary-electron cutoff of 26DFBT functionalized (blue dots) and 35DFBT functionalized (red dots) Au compared to the corresponding unfunctionalized Au (measures by PYSA).

5.3.1 Morphological characterization

The morphology and electronic structure of the MoS₂ monolayer crystal at each step of the process were *in situ* assessed to detect changes and confirm the covalent grafting of the molecular isomers onto the basal plane of MoS₂ via self-assembly. Figure 5.4a and d show the optical microscopy images of monolayer MoS₂, while Figure 5.1 displays the AFM topographical image. The pristine monolayer MoS₂ crystal exhibits an atomically flat surface with a root-mean-square roughness (R_{RMS}) of approximately 0.5 nm, due to its easy-to-peel van der Waals layered structure and the absence of dangling bonds on the surface.^{[56;}

^{57]} Figures 5.4b and e confirm the absence of changes in the thickness and roughness of

MoS₂ upon introduction of defects.

However, after molecular functionalization, a considerable increase in the average thickness of the MoS₂ monolayer has been observed. Figures 5.4c and f show that the thickness of monolayer MoS₂ augmented from 0.59 nm to 1.45 nm after the functionalization of 26DFBT molecules and from 0.66 nm to 1.46 nm after the modification of 35DFBT molecules. This increase in thickness can be ascribed to the covalent tethering of the difluorobenzenethiol molecules, as confirmed by the variation in vertical distance before and after functionalization perfectly matching the van der Waals contour of the grafted molecule. The thickness of the 35DFBT is slightly higher than that of the 26DFBT because the F atoms facing upward. In addition, after molecular grafting small grains appeared on the MoS₂ surface, and the R_{RMS} increased from 0.55 nm to 0.62 nm for the 26DFBT functionalized sample and from 0.60 nm to 0.88 nm for the 35DFBT functionalized sample, respectively, which is consistent with previous reports in the literature.^[47; 58] The above findings provide clear evidence that the difluorobenzenethiol isomers were successfully grafted to the MoS₂ surface.

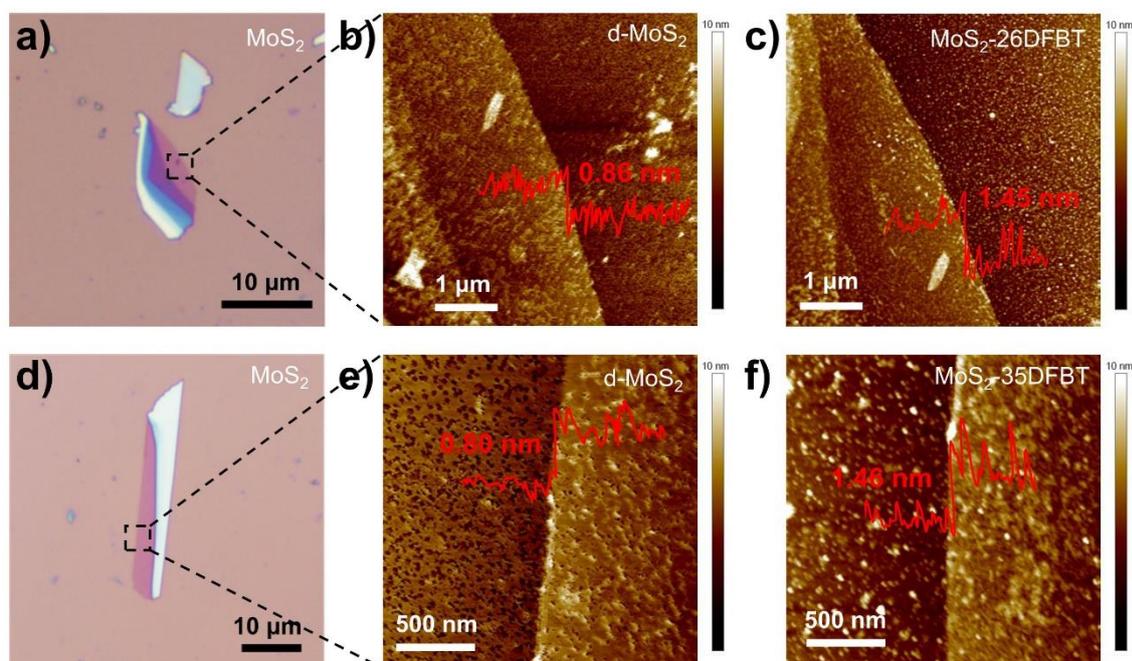


Figure 5.4 Optical microscopy images and *in situ* AFM morphology of pristine (a and d), defect-induced (b and e), and isomer-functionalized (c and f) monolayer MoS₂ flakes. The estimated R_{RMS}

in b and e amount to 0.55 nm and 0.60 nm, respectively. c) 26DFBT functionalized monolayer MoS₂ flake morphology. R_{RMS} is 0.62 nm. f) 35DFBT functionalized monolayer MoS₂ flake morphology. R_{RMS} is 0.88 nm.

5.3.2 Elemental characterization

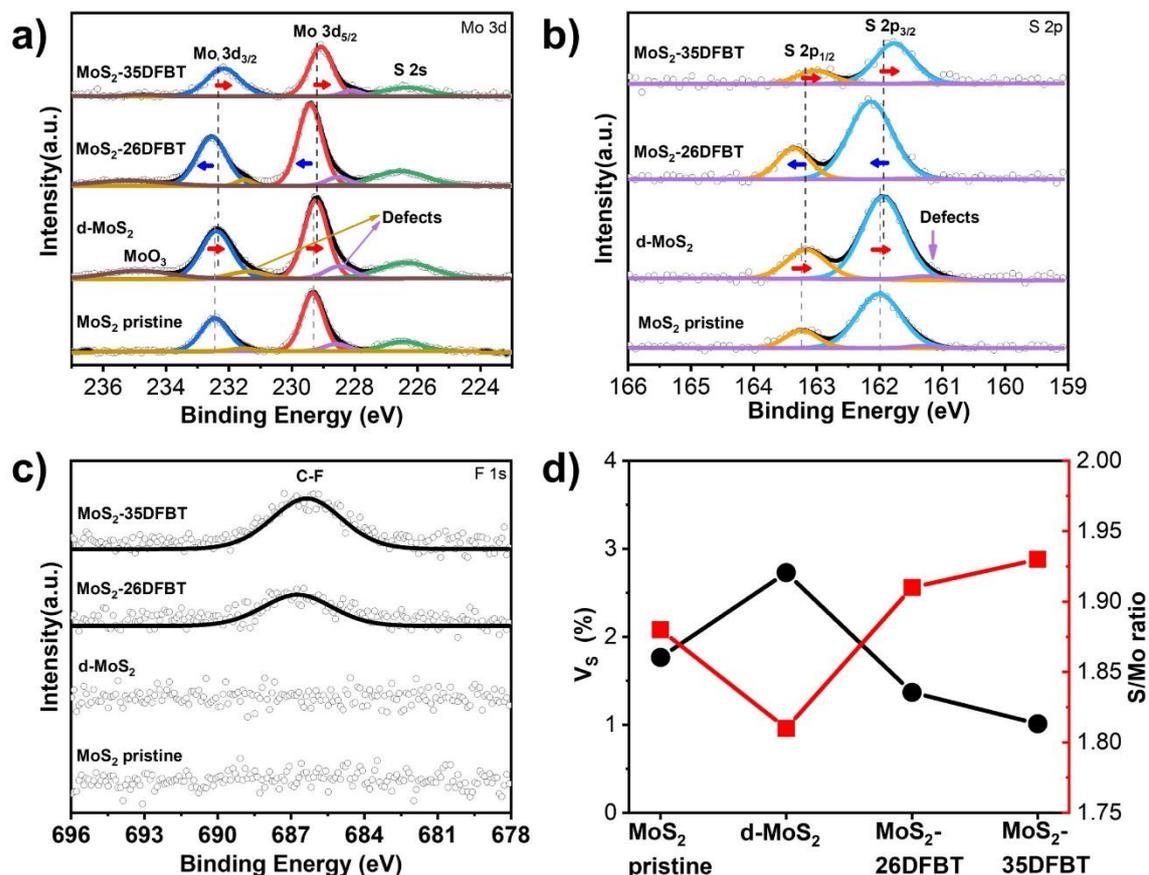


Figure 5.5 (a-c) High-resolution XPS Mo 3d, S 2p, and F 1s core-level spectra of isomers functionalized MoS₂ compared to the corresponding pristine and defect-induced surface. (d) Sulfur vacancy concentration (V_s) and S/Mo stoichiometric ratio of different samples.

High-resolution X-ray photoelectron spectroscopy (XPS) analyses provide important insights for assessing changes in the electronic structure of monolayer MoS₂ before and after isomers functionalization. Figure 5.5 portrays the Mo 3d, S 2p, and F 1s core-level spectra of MoS₂ monolayer for each step of the treatment. In the Mo 3d core energy level spectrum, the MoS₂ pristine monolayer shows spin-orbit splitting doublets from lattice Mo-S at 229.30 eV (Mo 3d 5/2, red curve) and 232.44 eV (Mo 3d 3/2, blue curve). Correspondingly, the S 2p core energy level spectrum exhibits spin-orbit splitting doublets

at 162.01 eV (S 2p 3/2, cyan curve) and 163.23 eV (S 2p 1/2, beige curve), consistent with literatures.^[59; 60] Interestingly, two additional shoulder doublets appeared at slightly lower binding energies of the Mo 3d peak (purple curve at 228.50 eV and khaki curve at 231.5 eV), which can be attributed to vacancy neighboring atoms. This feature is due to the chemical reduction of Mo caused by sulfur deficiency (valence of Mo < 4). Moreover, an additional component at the lower binding energy of 161.5 eV for S 2p was also attributed to S-vacancy defects.^[23; 59]

Table 5.1 Shifts of Mo 3d and S 2p peaks of MoS₂ pristine and defects induced MoS₂.

	MoS ₂ (eV)	d-MoS ₂ (eV)	Δ (eV)
Mo 3d 3/2	232.44	232.35	-0.09
Mo 3d 5/2	229.30	229.21	-0.09
S 2p 1/2	163.23	163.17	-0.06
S 2p 3/2	162.01	161.93	-0.08

The S-vacancy defects concentration (V_s , see section 5.2.3 for calculation details) and S/Mo stoichiometric ratio of MoS₂ were calculated from the integrated area of the S and Mo components. As shown in Figure 5.5d, the calculated V_s of mechanically exfoliated MoS₂ amounts to 1.77%, and the S/Mo stoichiometric ratio was 1:1.88, in line with previous reports.^[47] After high-temperature treatment, both Mo and S doublets shift toward lower binding energies, and the intensity of the defect component peaks increases notably, indicating that the Fermi level shifts toward the valence band (VB) edge.^[60] Table 5.1 summarizes the shift amount of Mo 3d and S 2p peaks positions before and after treatment. The V_s increased up to 2.73%, and the S/Mo ratio decreased to 1:1.81, indicating the increased defectiveness of the crystal, providing abundant sites for subsequent functionalization. Interestingly, a weak deconvoluted peak appeared at higher binding energies (235 eV), which represents the signal of oxidized molybdenum, suggesting partial oxidation of the Mo atoms.^[37; 40; 47; 61]

The F 1s core energy spectra of the isomer functionalized samples are shown in Figure 5.5c. Both spectra exhibit a distinct single peak that originates from the C-F bond in the molecule. The 35DFBT functionalized MoS₂ shows a higher intensity peak signal compared to the 26DFBT modified sample due to the exposed double F atoms in its molecular structure, which confirms again the isomer functionalization on the MoS₂ surface. However, the Mo 3d and S 2s spectra of the functionalized MoS₂ indicate a clear shift in opposite directions. Table 5.2 provides a summary of the amount of shift of the Mo 3d and S 2p peaks position before and after functionalization. The Mo and S peaks of MoS₂ shift toward higher binding energies by about 0.2 eV after functionalization with 26DFBT, indicating the Fermi level was closer to the conduction band (CB) edge and corresponding to n-type electron doping. In contrast, upon functionalization with 35DFBT, both Mo and S peaks of MoS₂ shift toward low binding energy by about 0.16 eV, suggesting the Fermi level was closer to the VB edge and corresponding to p-type hole doping.^[62-66] No additional peak was detected near 164 eV in the S 2p spectrum, indicating the absence of free or unbound thiol, i.e., no physisorbed molecules on the MoS₂ surface.^[67; 68] After isomer modification, the V_S of MoS₂ significantly reduced to 1.37% and 1.01%, as well as the S/Mo ratio increased to 1:1.91 and 1:1.93, corresponding to the functionalization of 26DFBT and 35DFBT, respectively. These results suggest that thiol-containing isomers can graft onto the MoS₂ surface through covalent bonding and are capable of repairing the S-vacancy defects as previously reported.^[20; 21; 45; 69-71]

Table 5.2 Shifts of Mo 3d and S 2p peaks before and after isomer functionalization.

	d-MoS₂ (eV)	MoS₂-26DFBT (eV)	Δ(eV)	MoS₂-35DFBT (eV)	Δ(eV)
Mo 3d 3/2	232.35	232.57	0.22	232.18	-0.17
Mo 3d 5/2	229.21	229.42	0.21	229.07	-0.14
S 2p 1/2	163.17	163.34	0.17	163.02	-0.15
S 2p 3/2	161.93	162.14	0.21	161.76	-0.17

5.3.3 Raman and PL characterization

To gain further insight into the impact of defects and isomeric functionalization on the electronic and optical properties of MoS₂ monolayers, Raman and PL spectra were recorded. The Raman spectra of a typical MoS₂ monolayer, featuring in-plane E¹_{2g} vibrational mode of Mo and S atoms at ~386 cm⁻¹ and out-of-plane A_{1g} vibrational mode of S atom at ~404.5 cm⁻¹, as shown in Figures 5.7a and b. The frequency difference between the two vibrational modes is layers dependent and is less than 20 cm⁻¹ for monolayer (see Figure 5.6 for Raman spectra of monolayer MoS₂).^[52; 72]

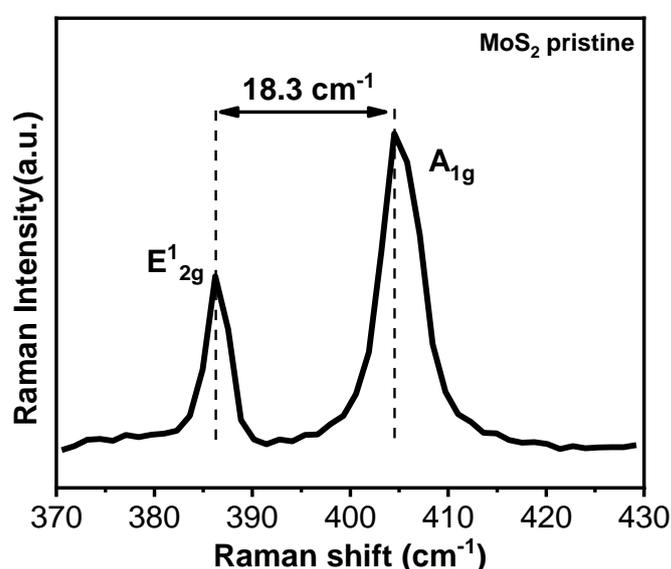


Figure 5.6 Raman spectra of monolayer MoS₂ flake, measured at room temperature in ambient. The frequency difference of 18.3 cm⁻¹ between E¹_{2g} mode and A_{1g} mode confirm the monolayer nature.

The defect-generating treatment resulted in a small blueshift in the A_{1g} peak by 0.12 cm⁻¹ (from the gray vertical dashed line to the black vertical dashed line in Figure 5.7a), and this offset correlated with the change in V_s (which increased by 0.96%), in agreement with previously reported defects induced by thermal annealing and ion irradiation.^[21; 73] However, after molecular functionalization, the A_{1g} peak shifts in two opposite directions compared to d-MoS₂ containing S-vacancy defects. It has been reported that the A_{1g} mode

is more sensitive to charge changes within MoS₂ than E¹_{2g}, and that a redshift of A_{1g} corresponds to higher electron concentration (n-doping), which increases electro-phonon scattering and weakens the vibration, whereas a blueshift corresponds to a lower electron concentration (p-doping), which weakens electro-phonon scattering and enhances the vibration.^[58; 62; 66] Specifically, 26DFBT functionalization resulted in a blue shift of A_{1g} peak of approximately 1.42 cm⁻¹, reflecting n-doping, whereas 35DFBT functionalization red-shifted by 1.17 cm⁻¹, suggesting p-doping. It is worth noting that the spectral resolution is about 1.25 cm⁻¹ (≈1 meV). The inset of Figure 5.7b depicts the dipole-induced doping effect and the dipole moment orientation of isomers grafted onto the MoS₂ monolayer, and the upward (downward) dipole orientation induces n-doping (p-doping), in agreement with the XPS results.

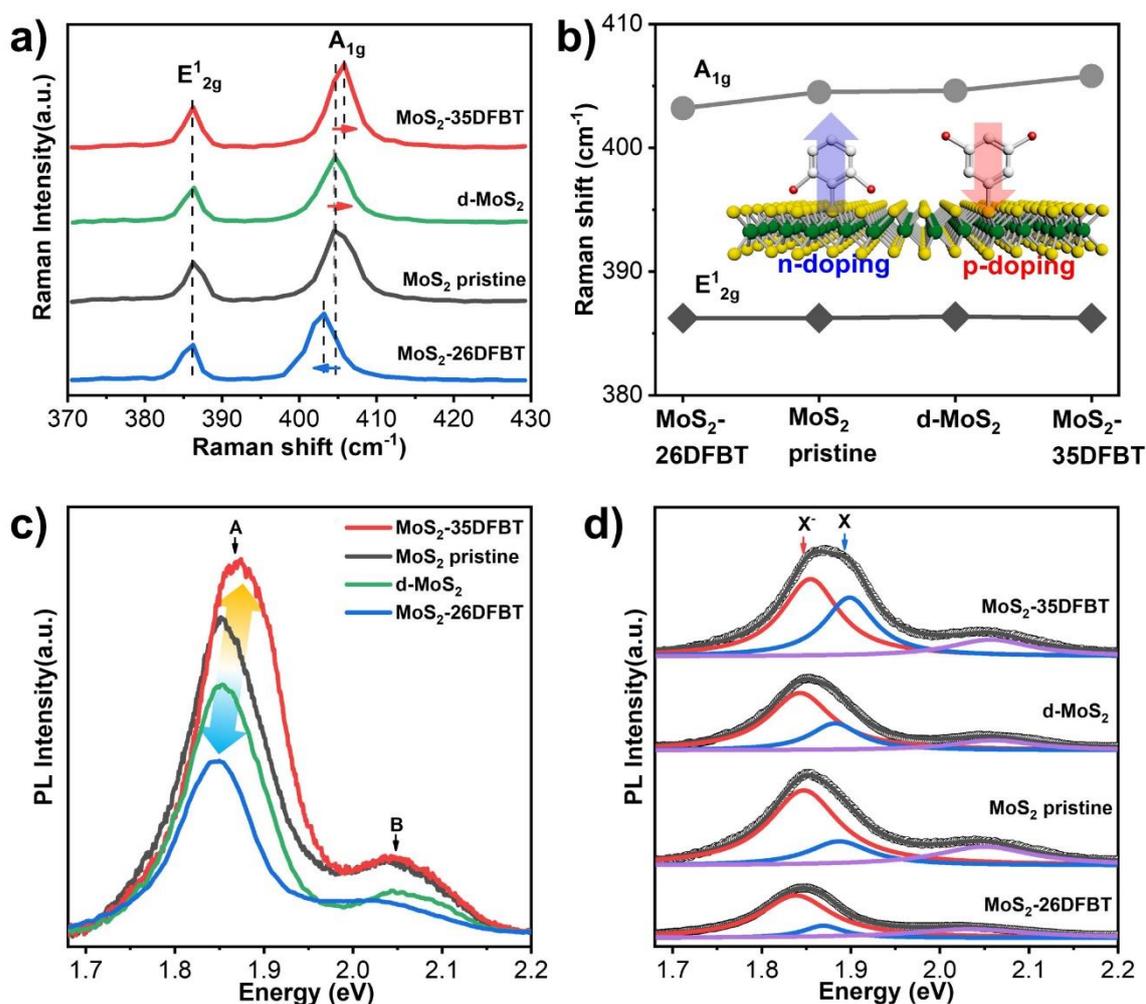


Figure 5.7 Raman spectra of pristine MoS₂, d-MoS₂ and functionalized with isomers. b) Plot of the Raman shift in E¹_{2g} mode and A_{1g} mode in Figure a. The inset demonstrates the dipole-induced doping effect and the dipole moment orientation of isomers functionalized on MoS₂ monolayer. c) PL spectra of pristine MoS₂, d-MoS₂ and functionalized with isomer. d) Analysis of the PL spectra with the peak deconvolution.

Figure 5.7c and d show the PL spectra and peak deconvolution analysis of monolayer MoS₂ before and after treatment. The PL spectra of monolayer MoS₂ exhibit two main peaks: the dominant A exciton peak at 1.85 eV and the relatively weak B exciton peak at 2.05 eV, which can be ascribed to the direct bandgap transition and spin-orbit splitting.^[62] The reduced PL intensity of the d-MoS₂ was caused by the introduction of defects, in line with the previous reports.^[21; 36] After 26DFBT functionalization, the peak intensity continues to decrease and redshift, while the intensity of MoS₂ functionalized with 35DFBT peak increased and blueshifted. This trend is in line with the dipole-induced change in the carrier density after functionalization of MoS₂ with the molecular isomers, which appears as a quenching and enhancement of the PL intensity resulting from n- and p-doping effects, respectively. Additionally, the A exciton peak can be deconvoluted into two components by Lorentz fitting, including a negative trion (X⁻, red curve) peak at approximately 1.85 eV and a neutral exciton (X, blue curve) peak at around 1.89 eV, respectively. Both monolayer MoS₂ and d-MoS₂ containing defects exhibit a trion (X⁻) peak that more weighted than the neutral exciton (X) peak, though the X peak of d-MoS₂ slightly enhanced. Following 26DFBT functionalization, the exciton peak X intensity decreased sharply, while the weight of the trion (X⁻) peak increased, and the PL peak was dominated by the trion (X⁻) peak, indicating a clear n-doping. In contrast, following 35DFBT functionalization, the weight of the neutral exciton (X) peak clearly increased, suggesting an obvious p-doping. This result is similar to the electron/hole dopant-induced PL changes reported in the literature.^[62; 65; 72]

5.3.4 Electrical characterization

To demonstrate the sensitivity of FETs based on monolayer MoS₂ for isomer identification, we performed electrical characterization of the devices before and after isomer functionalization (see the device schematic in Figure 5.2). Figure 5.8 shows the

representative transfer ($I_{ds} - V_{gs}$) and output ($I_{ds} - V_{ds}$) characteristics of the FETs based on pristine monolayer MoS₂, after the introduction of defects and subsequent isomer functionalization. To monitor the modifications in the electrical characteristics of the devices upon isomer functionalization, as well as to avoid potential bias that may arise from the comparison of different devices, we compared changes based on the same device. It can be seen that the monolayer MoS₂ FETs exhibits typical n-type transport behavior (black curve), while the linear threshold voltage (V_{th} , obtained in the linear transfer curve as the intersection of the transfer curve starting potential line and the off-state baseline. Figure 5.9 present the value extraction method and all linear transfer curves and their V_{th} values used in this study) slightly shifted to a negative gate voltage and the on-state current (I_{on}) slightly reduced following the introduction of defects (green curve). Such observations can be explained on the one hand in view of the introduction of S-defects acting as deep electron acceptors, and on the other hand by the occurrence of p-doping originating from the oxidation of partial Mo atoms in the crystal.^[47; 60]

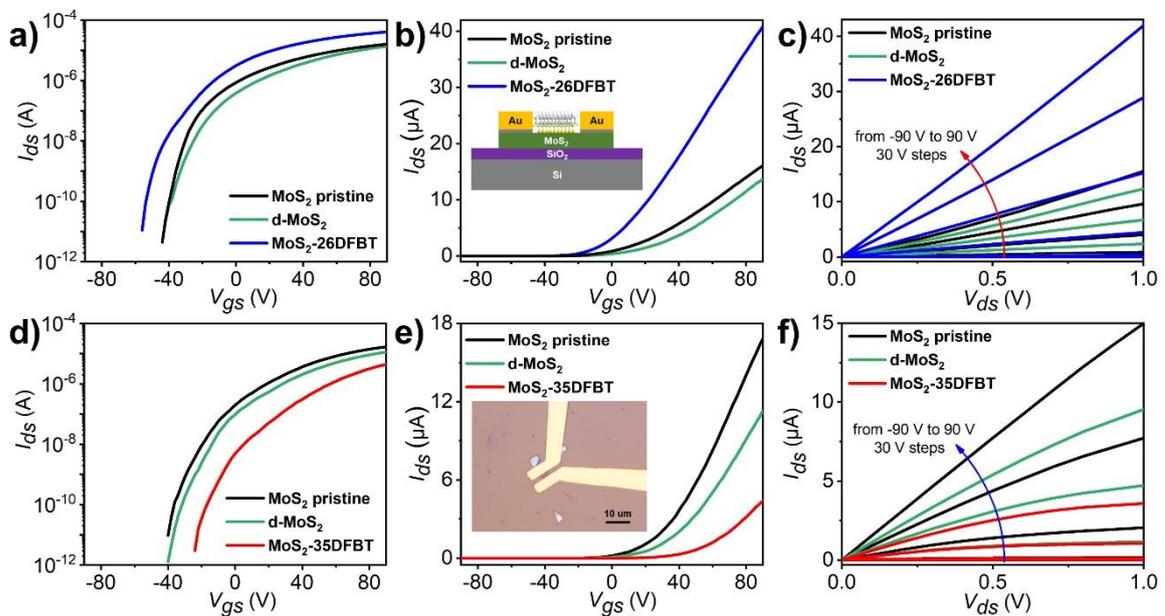


Figure 5.8 (a-b) Logarithmic and linear transfer curves ($I_{ds} - V_{gs}$) of pristine monolayer MoS₂ FETs, after induced defect and after functionalized with 26DFBT molecules. The applied bias is 1 V. The illustration in b is the scheme diagram of MoS₂ FETs functionalized with 26DFBT molecules. The channel length/width is 1.21 μm /4.65 μm . (c) Output curves ($I_{ds} - V_{ds}$) of above devices. (d-e) Logarithmic and linear transfer curves ($I_{ds} - V_{gs}$) of pristine monolayer MoS₂ FETs, after

induced defect and after functionalized with 35DFBT molecules. The applied bias is 1 V. The inset in e shows the optical microscopy image of the device based on the pristine MoS₂ monolayer. The channel length/width is 1.73 μm /2.59 μm . (f) Output curves ($I_{\text{ds}} - V_{\text{ds}}$) of above devices.

However, the devices undergo opposite changes following isomeric functionalization due to the doping effect induced by different dipole orientations of two molecules. 26DFBT functionalized devices display a negative shift of the transfer curves (blue curve) and an increase of the I_{on} , indicating n-doping effect. Conversely, 35DFBT functionalized devices exhibit a positive shift of the transfer curves (red curve) and a decrease of the I_{on} , suggesting a p-doping effect. These findings are in agreement with previous XPS, Raman and PL results. Furthermore, all devices exhibited $I_{\text{on}}/I_{\text{off}}$ ratios exceeding 10^6 before and after functionalization, and the linear output curves demonstrate that all devices possess ohmic contact between the electrodes and the semiconductor, as evidenced in Figure 5.8c and 5.8f, which means that MoS₂ always maintains excellent semiconducting properties.

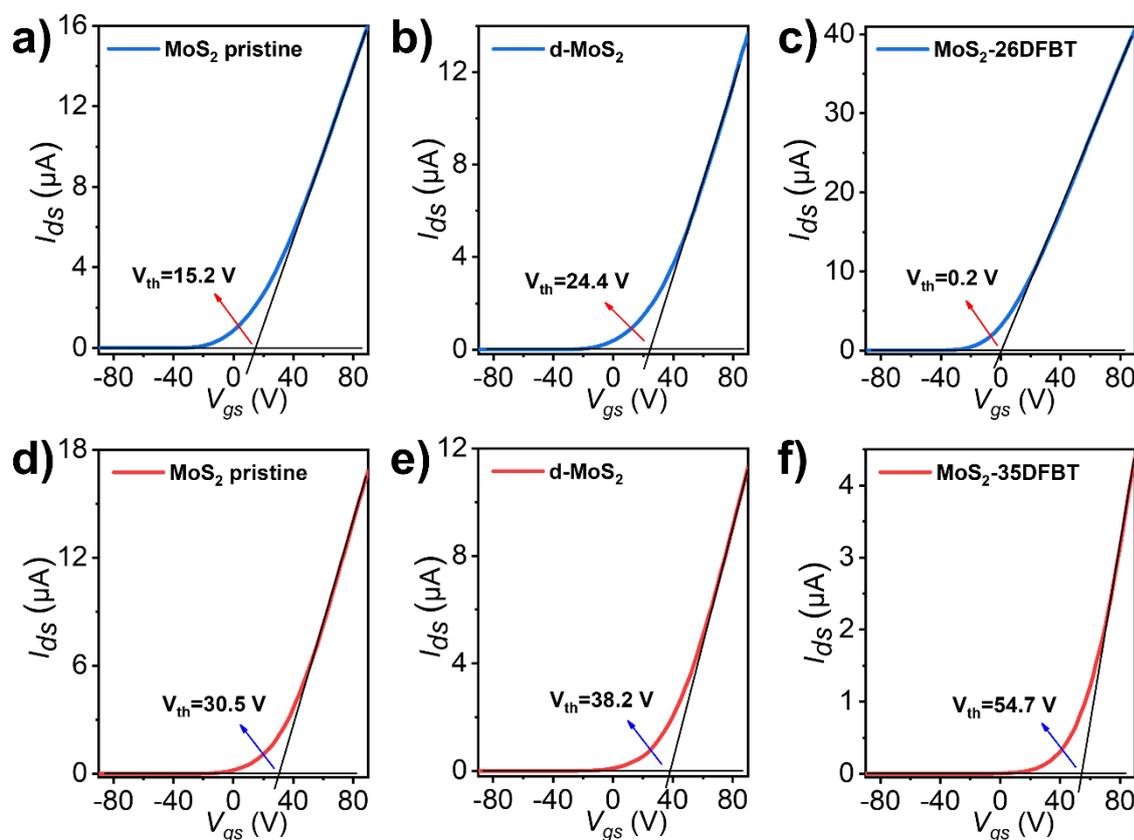


Figure 5.9 (a-b) Logarithmic and linear transfer curves of pristine monolayer MoS₂ FET device and functionalized with 35DFBT molecules. The illustration in b is the molecule structure of

35DFBT. (c) the optical picture of the device. (d-e) Output curves of the device before and after doping. (f) Schematic diagram of MoS₂ FET device functionalized with 35DFBT molecules.

Table 5.3 The changes in threshold voltage (V_{th}) and mobility (μ) for isomer functionalized devices.

	MoS ₂ pristine	d-MoS ₂	MoS ₂ - 26DFBT	MoS ₂ pristine	d-MoS ₂	MoS ₂ - 35DFBT
V_{th} (V)	15.2	24.4	0.2	30.5	38.2	54.7
μ (cm ² V ⁻¹ s ⁻¹)	4.5	4.1	9.7	15.1	11.5	6.2

Table 5.3 summarizes the changes in V_{th} and linear field-effect mobility (μ) of the devices before and after isomers functionalization. The linear carrier mobility μ was determined by the following equation

$$\mu = \frac{dI_{ds}}{dV_{gs}} \times \frac{L}{WC_{ox}V_{ds}} \quad (5 - 4)$$

where L and W are the channel length and width, and C_{ox} is the capacitance of dielectric layer per unit area. The charge in the carrier density change (Δn) within the channel can be quantified by the change of V_{th} with the equation below:^[57; 74]

$$\Delta n = \frac{C_{ox}\Delta V_{th}}{e} = \frac{\epsilon_{ox}\Delta V_{th}}{t_{ox}e} = 7.99 \times 10^{10} \text{ cm}^{-2} \quad (5 - 5)$$

where C_{ox} is the capacitance per unit area of dielectric layer, ΔV_{th} is the change of V_{th} , e is the elementary charge, ϵ_{ox} is the dielectric constant of dielectric layer, t_{ox} is the thickness of dielectric layer. The value of Δn is indicative of the molecule's dipole-induced doping capability. Following the calculations, it was found that 26DFBT functionalization enables to increase the carrier density by $1.93 \times 10^{12} \text{ cm}^{-2}$, which in turn led to an increase in mobility from 4.1 to 9.7 cm² V⁻¹ s⁻¹, while 35DFBT functionalization decreases the charge carrier density by $1.32 \times 10^{12} \text{ cm}^{-2}$, which resulted in a mobility decrease from 11.5 to 6.2 cm² V⁻¹ s⁻¹. The amount of Δn in this study is comparable to the previously reported molecular dopants, indicating that device functionalization is an efficient and

facile strategy for isomer identification.^[58; 62; 65]

5.3.5 DFT theoretical calculation

Theoretical calculations were performed to demonstrate the changes on MoS₂ before and after isomer functionalization. In particular, we calculated the dipole moment of the isolated molecules and the isomer-functionalized d-MoS₂ systems, as well as their work function (ϕ , WF) at the DFT/HSE06 level of theory, see Figure 5.10 and table 5.4. For comparison, we extended the calculations to benzenethiol (BT), lacking any substituent on the aromatic ring, so as to best shed light on the changes induced by the fluorine substituents. Due to the different positions of the F atoms, 26DFBT features an upward dipole with a dipole moment (D_f) of -1.44 D, while 35DFBT shows a downward dipole with a D_f of +0.99 D. When chemically adsorbed on d-MoS₂ (3% V_S), the dipole moment direction of the isomer-MoS₂ systems is consistent with that of the isolated molecules, as shown in figure 5.10d-f, and the WF changes accordingly: the WF calculated for MoS₂-26DFBT is lower than MoS₂-BT (5.14 eV) due to the upward dipole moment, while it is higher in MoS₂-35DFBT because of the downward dipole moment.

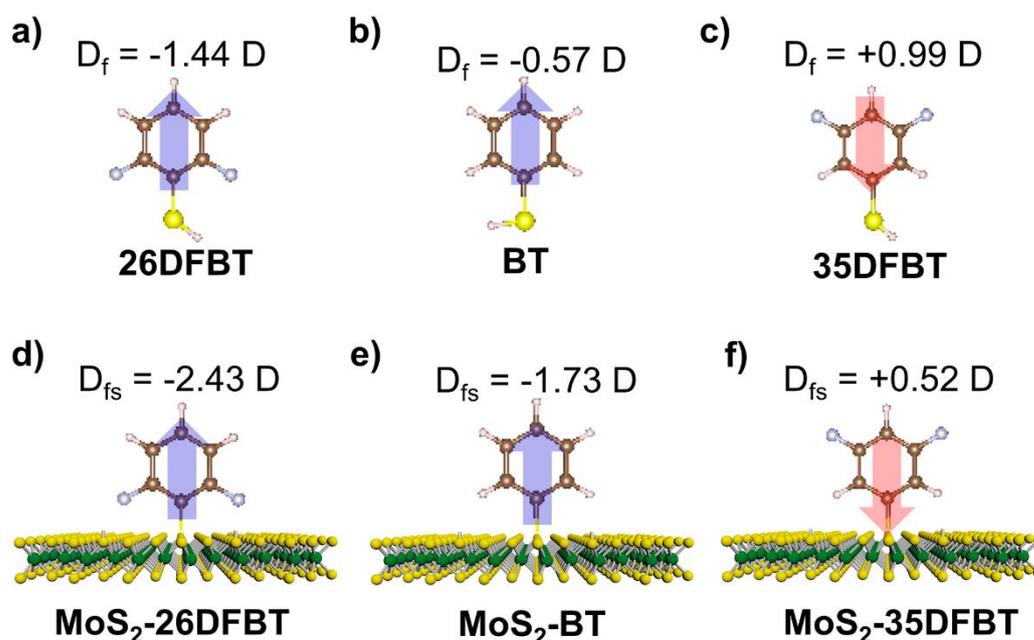


Figure 5.10 Calculated dipole moment of isolated isomer molecules and functionalized monolayer MoS₂ systems. For comparison, we additionally calculated benzenethiol (BT or thiophenol), which has no substituents on the benzene ring, and can clearly reflect the dipole moment change induced

by the F substituents in isomers. (a) 26DFBT, (b) BT, (c)35DFBT. (d) MoS₂-26DFBT system, (e) MoS₂-BT system, and (d) MoS₂-35DFBT system. D_f represents the dipole moment of isolated molecules, and D_{fs} presents the dipole moment of (DF)BT-MoS₂ system, the unit is Debye (D).

Figure 5.11 show the electronic band structure of monolayer MoS₂ chemisorbed with isomers on S vacancies (3% V_S) on a 4×4×1 supercell. The calculated ϕ of MoS₂-26DFBT and MoS₂-35DFBT are 5.09 eV and 5.42 eV, respectively. Compared to the d-MoS₂ (3% V_S) surface, with a ϕ of 5.23 eV, 26DFBT thus induces a relative n-doping with 0.14 eV increase in WF, whereas 35DFBT induces a relative p-doping with 0.19 eV decrease in WF. These relative shifts are consistent and in good quantitative agreement with the corresponding energy shifts measured by XPS. Also, the relative shift in the n-/p- doping due to functionalization is proportional to the axial dipole component of the molecule, similar to what observed for WS₂ (3% V_S) and WSe₂ (3% V_{Se}) surfaces in our previous theoretical investigations^[75]. Figure 5.11c and d show the calculated charge density difference maps of isomers functionalized d-MoS₂ (3% V_S), which related the difference between the total charge density of isomers covalently chemisorbed on d-MoS₂ (3% V_S) and the combined charge density of isolated isomer molecule and d-MoS₂ (3%V_S), demonstrates a strong interaction between isomers and MoS₂ (3% V_S).

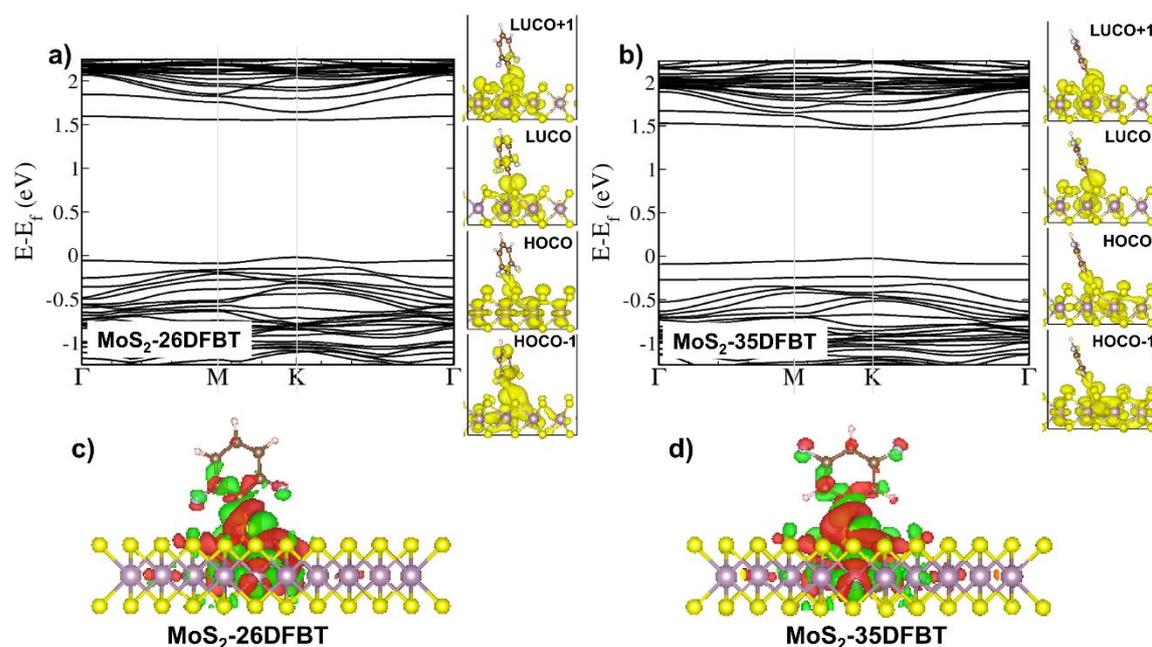


Figure 5.11 Electronic band structure of monolayer MoS₂ with the chemisorbed 26DFBT molecules

(a) and 35DFBT molecules (b) on 3% S vacancy sites. The right panel shows the charge distribution of the highest occupied crystal orbital (HOCO and HOCO-1) and the lowest unoccupied crystal orbital (LUCO and LUCO-1). c-d) show the charge density difference maps of 26DFBT and 35DFBT functionalized monolayer MoS₂ on S vacancy sites, respectively demonstrating a strong interaction between the isomers and MoS₂ (3% V_S).

In addition, we also calculated the WF at the DFT/GGA/PBE level of theory, WF of BT and 26-DFBT functionalized d-MoS₂ (3% V_S) surfaces are 5.32 eV and 5.21 eV respectively, whereas that of 35-DFBT functionalized d-MoS₂ (3% V_S) surface is 6.01 eV. Compared to the d-MoS₂ (3% V_S) surface, with a ϕ of 5.80 eV, 26-DFBT induces relative n-doping whereas 35-DFBT induces relative p-doping with corresponding shifts in the WF of -0.59 eV and +0.21 eV, respectively. These changes are comparable with the experimental results and the calculation at the DFT/HSE06 level of theory.

Table 5.4 DFT calculated work functions (ϕ) and dipole moment of molecules and MoS₂-DFBT systems.

System	ϕ^a (eV)	$\Delta^b\phi$ (eV)	Dipole moment (D)	
			Molecule	System
d-MoS ₂ (3% V _S)	5.23	-	-	-
MoS ₂ -BT	5.14	-0.09	-0.57	-1.73
MoS ₂ -26DFBT	5.09	-0.14	+0.99	+0.52
MoS ₂ -35DFBT	5.42	0.19	-1.44	-2.43

^a ϕ represents the work functions. ^b Δ represents the difference with d-MoS₂.

5.3.6 Mechanism analysis

Figure 5.12 displays the scheme of the suggested mechanism of isomeric functionalization on MoS₂ electronic structure. Initially, mechanically exfoliated pristine monolayer MoS₂ crystals exhibit n-type semiconductor properties (Figure 5.12a). However, the introduction of S-defects serves as deep acceptors, which shift VB towards the Fermi energy level, resulting in a reduction of device performance (Figure 5.12b). Subsequently, upon isomer covalent functionalization, 26DFBT induces n-doping, which shifts the CB toward the Fermi energy level and enhances the device performance (Figure 5.12c), while 35DFBT

induces p-doping, which shifts the VB toward the Fermi energy level and degrades the device performance (Figure 5.12d). Consequently, differences in device performance can be used to differentiate between isomers.

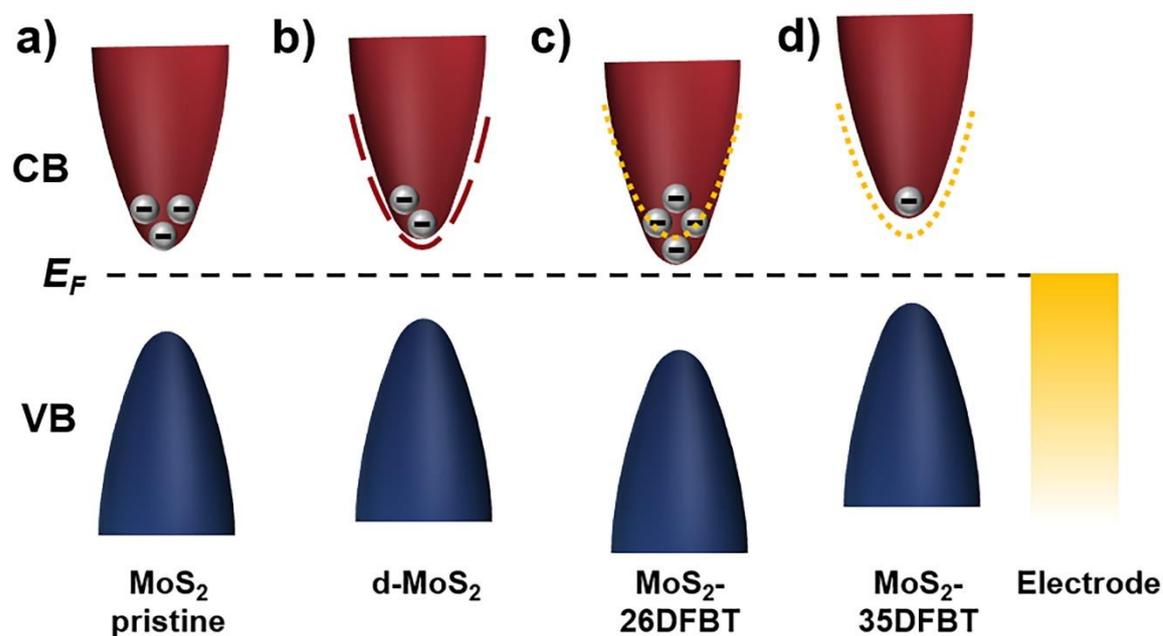


Figure 5.12 Mechanism of defect creation and isomers functionalization on the electronic structure of monolayer MoS₂. Fermi levels are aligned. The red and blue semi-ellipses denote the conduction band (CB) and valance band (VB), respectively. The red dashed line in b) indicates the CB of pristine MoS₂. The yellow dotted lines in c) and d) indicate the CB of d-MoS₂.

5.4 Conclusions

In conclusion, this study demonstrates a universal method to identify isomers by introducing S-vacancy defects through defect engineering on mechanically exfoliated MoS₂ monolayers, followed by isomer functionalization via covalent grafting. The identification of isomers was accomplished by analyzing XPS data, Raman spectra, PL spectra, and FETs characteristics. The distinct functionalization outcomes of MoS₂ monolayers resulted from the different magnitude and orientation of the dipoles in the molecular isomers, which led to discrepancies in the doping effects. These findings highlight the great potential of 2D materials for isomer identification, and suggest that this approach could be a simple, efficient and straightforward method for rapidly and selectively

identifying isomers and other hardly distinguishable compounds.

5.5 References

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Chapter 6 Asymmetric Functionalization of Top-Contact Electrodes: Tuning the Charge Injection in MoS₂ Field-Effect Transistors and Schottky Diodes

The fabrication of high-performance (opto-)electronic devices based on ultrathin two-dimensional channel materials requires the optimization of the charge injection at the electrode - semiconductor interface. While the chemical functionalization with chemisorbed self-assembled monolayers has been extensively exploited to adjust the work function of metallic electrodes in bottom-contact devices, such a strategy was never demonstrated when the top-contact configuration is chosen, despite the latter is known to offer enhanced charge injection characteristics. Here, we have developed a novel contact engineering method to functionalize gold electrodes in top-contact field-effect transistors (FETs), via the transfer of chemically pre-modified electrodes. The source and drain electrodes of the molybdenum disulfide (MoS₂) FETs were functionalized with prototypical thiolated molecules possessing by design different dipole moments. While the modification of the Au electrode with electron-donating molecules yielded a marked improvement of the device performance, the asymmetric functionalization of the source and drain electrodes with two different chemisorbed molecules with opposed dipole moment enabled the fabrication of a high-performance Schottky diodes with a rectification ratio of $\sim 10^3$. Our unprecedented strategy to tune the charge injection and extraction in top-contact MoS₂ FETs is of general applicability for the fabrication of high-performance opto-electronic devices based on 2D semiconductors in which the energetic asymmetry is required to boost the device functionality (e.g., for light-emitting transistors, solar cells, etc), enabling to tailor the device characteristics on-demand.

6.1 Introduction

Two-dimensional transition metal dichalcogenides (TMDCs) display a broad variety of outstanding electrical and optical properties making them ideal components for the next generation high-performance (opto)electronic devices.^[1-4] Among them, MoS₂ represents a prototypical 2D semiconductor as it combines several advantages such as a sizeable band gap, high I_{on}/I_{off} ratio, great scalability and immunity to short-channel effects.^[1; 5; 6] Although MoS₂ based field-effect transistors (FETs) showed good key performance indicators, the currently developed devices are far from exploiting the full potential of this semiconducting material. Major bottlenecks are associated to fundamental physical processes due to the presence of large Schottky barrier heights (SBH, Φ_{SB}), severe Fermi level pinning (FLP) and interfacial defects. In order to boost the device performance charge injection and extraction at the metal - MoS₂ interface need to be optimized.^[7-11] Numerous attempts have been made by using van der Waals (vdW) contacts^[12], low work function (WF) contacts^[13], insertion of h-BN tunneling layer or metal oxide layer^[14-17], introduction of graphene^[18], contact doping^[19], and via the functionalization of the electrodes with self-assembled monolayers (SAMs)^[8; 20] in devices based on bottom-contact geometries. Among them, SAMs functionalization has been proved to be a powerful and versatile method to adjust the WF of noble metals (Au, Ag, etc.) by reducing the SBH and contact resistance hence improving the carrier injection.

Among various configurations, FETs with bottom-contact geometries are the most commonly used. While they allow easy functionalization of the metallic electrodes with chemisorbed SAMs, they are far from being ideal for high-performance devices. Conversely, both theory^[21-26] and experiments^[22; 27] have unambiguously demonstrated that the top-contact configuration of staggered architecture offers better contacts and more efficient charge injection. This can be understood in view of some geometrical reasons: the injection of the coplanar architecture occurs from the contact edge into semiconductor, and all contact area facing the gate of staggered architecture can participate to the injection process.^[23; 28-32] However, the top electrode is generally prepared by thermal deposition,

hence it can hardly be chemically modified. On the other hand, deposition of metallic electrodes via the direct vacuum sublimation of “hot” metal atoms onto a molecular surface can be extremely invasive by destroying the molecular layer, leading to short circuits.^[33; 34] Moreover, the electrodes functionalization in bottom-contact devices still has some problems which are hard to be addressed. In the first place, due to the metal electrode strong electrostatic screening effect^[35; 36], the carrier injects from the contact edge of the electrodes which is limited by the thickness of the electrodes.^[28] Although in principle this can be improved by increasing the electrode thickness, another study demonstrates that the injection efficiency is not proportional to the thickness of the electrode. When the electrode becomes thicker, the injection efficiency deteriorates.^[37] Furthermore, since the semiconductor layer needs to be prepared after the functionalization of the electrode, the morphology and stacking structure of functionalized molecules have a significant influence on the formation of the semiconductor layer.^[38] Therefore, generally applicable methods for fabricating top-contact FETs with functionalized electrodes are nowadays highly sought after. Herein, we have devised an unprecedented dry-transfer approach enabling the efficient covalent functionalization of top-contacts in MoS₂ based FET devices. The electrodes are pre-functionalized with SAMs and physically laminated on the 2D semiconductor through vdW contact. The device performance can be tuned via the controlled electrodes functionalization with different chemisorbed SAMs to decrease (increase) the charge injection barrier. This strategy also enables the asymmetric functionalization of the source and drain top-contacts with molecules possessing opposite dipoles, to fabricate Schottky diodes with a rectification ratio exceeding 10³.

6.2 Experimental methods

6.2.1 Materials and instruments

Materials: Bulk MoS₂ crystals were purchased from SPI Supplies. The 2,3,4,5,6-pentafluorobenzenethiol (PFBT) was purchased from Sigma-Aldrich. The 4-(dimethylamino)benzenethiol (DABT) was purchased from TCI. The Cytop polymer was

purchased from Asahi Glass and diluted with dedicated CT-Solv.180 solution, the volume ratio is 1:2.

AFM Measurement: Tapping mode Atomic Force Microscopy (AFM) imaging was performed by using a Bruker Dimension Icon set-up operating in air. The tip model is TESPA-V2, and the tip stiffness K is 42 N m^{-1} .

Work Function Measurement: The Work Function (WF) was measured by Photoelectron Yield Spectroscopy in Air (PYSA), using a AC-2 Photoelectron Spectrometer (Riken-Keiki Co.). The ambient photoelectron yield measurements were performed by sampling in each measurement an area of about 4 mm^2 (beam size) with an ultraviolet (UV) incident light power of 300 nW with a counting time of 10 seconds per point.

XPS Measurement: X-ray Photoelectron Spectroscopy (XPS) measurements were performed in a high vacuum environment on a Thermo Scientific K-Alpha instrument. All XPS spectra were calibrated using the C 1s peak at 284.8 eV as a reference.

Contact Angle (CA) Measurement: Contact Angle (CA) measurements were performed on the Kruss DSA100S droplet shape analyzer. $2 \mu\text{L}$ deionized water was dropped on the sample surface with a micro-syringe, the CA values were acquired in Young Laplace fitting method.

Electrical Measurement: The FET devices were electrically characterized by a Keithley dual channel 2636A sourcemeter in a three-terminal configuration with the back gate contacted through an underlying metal plate in a glovebox filled with nitrogen in dark conditions. Schottky diodes are tested with the same instrumentation as FETs. Temperature dependent measurements were carried out in a cryogenic probe station (Janis-CCR5-2) using a semiconductor parameter analyzer (Keithley 4200) with a vacuum degree of about $5 \times 10^{-5} \text{ mbar}$.

6.2.2 Devices fabrication

6.2.2.1 Preparation of dielectric layer and semiconductor

The Cytop polymer dielectric layer was spin-coated onto the thermally oxidized silicon substrate (Fraunhofer Institute IPMS, $\rho_{\text{Si}} \approx 0.001 \text{ } \Omega \cdot \text{cm}$, $t_{\text{ox}} = 270 \text{ nm}$) with 3000 rpm for 60 s. Soft baked at 60 °C for 10 min, then cross-linked at 290 °C for 20 min in a nitrogen-filled glovebox. The thickness of the Cytop dielectric layer (85 nm) was determined by an Alpha-Step IQ surface profiler from KLA Tencor. The permittivity of Cytop is ~ 2.10 , and the capacitance of the Cytop/SiO₂ bilayer dielectric is 8.07 nF/cm². MoS₂ flakes were mechanically exfoliated from a bulk crystal by the Scotch-tape method and transferred to the commercial polydimethylsiloxane film (PDMS, purchased from gel-pak), then transferred on the Cytop/SiO₂ bilayer dielectric substrate. Their thickness was monitored by optical microscope combined with Raman spectroscopy and AFM. In this experiment, limited by the microscope resolution of probe station, two gold pads were deposited on both sides of the flake through a mask to increase the transferred source/drain electrode contact area and facilitate the connection between probe tip and electrodes.

6.2.2.2 Electrode fabrication and functionalization

Patterned gold electrodes (200 $\mu\text{m} \times 40 \mu\text{m}$, thickness 120 nm) were thermally evaporated on the surface of a silicon substrate (sacrificial substrate) through a copper mask (G100/400-C3, Glider Grids) by thermal evaporation. The sacrificial silicon substrate was pre-modified with octadecyltrichlorosilane (OTS). The OTS modified substrates were cleaned by sonification in chloroform and isopropanol, successively. With the pre-functionalization by OTS, the gold electrode has weak adhesion on the sacrificial substrate and can be mechanically desorbed and transferred. Before transfer, patterned electrodes after the UV/ozone cleaning treatment were immersed in a 5 mM ethanolic solution of DABT or PFBT molecules overnight for functionalization. An ethanol solution without any thiol molecules was used as a control experiment. After taking them out, they were gently rinsed several times with ethanol and dried with nitrogen.

6.2.2.3 Bottom-gate top-contact functionalized electrodes devices fabrication

The bottom gate top-contact functionalized electrodes devices were fabricated using PDMS-assisted dry transfer technique. In the transfer step, one piece of the (functionalized) Au electrode, approximately $40\ \mu\text{m} \times 200\ \mu\text{m}$ in size, was peeled from the substrate using mechanical probe. The tip of the probe was coated with Gallium-Indium alloy (purchased from Sigma-Aldrich). Next, this Au electrode piece was transferred onto a pre-cut PDMS film (gel-pak) surface. This electrode transfer technique has been used and reported many times as a mature technique.^[39-42] Same method was used to transfer another (functionalized) electrode to the side of first electrode. The channel size (length and width) between two (functionalized) electrodes can be customized according to crystal size (theoretically, the channel size can be adjusted arbitrary). Then, the PDMS film with (functionalized) electrodes was reversed and stucked on a glass slide, the glass slide was fixed at the arm of micromanipulator stage. The arm can be controlled in three dimensions of XYZ, then the electrodes were physically laminated on the MoS₂ flake surface immediately to fabricate the bottom-gate top-contact (functionalized electrodes) FETs under the alignment of the microscope telephoto lens. The PDMS film acts as an encapsulation layer to encapsulate and protect the device. The whole transfer processes can be completed within short exposure time to minimize any possible surface contamination. Finally, the device was annealed at 120 °C for 6 h in a high-vacuum chamber to remove possible absorbents.

6.2.2.4 Schottky diode fabrication

The preparation processes of the Schottky diode devices with asymmetric electrodes are the same as above, and two electrodes functionalized with different molecules were selected when forming the electrode channel on PDMS film (the step of figure 6.1b to 6.1c).

6.2.3 Calculation of contact resistance

Due to the limitation of device configuration, conventional transfer length method (TLM) and Kelvin probe force microscopy (KPFM) method cannot be applied in our case.

Therefore, the Y-function method was used here to extract contact resistance. The Y-function method has been widely reported and used to evaluate the contact resistance in the region of $V_{gs} - V_{th} \gg V_{ds}$ for both organic materials and TMDs semiconductor FETs.^[43-48]

If the additional voltage drops due to contact resistance R_C is considered, I_{ds} in a linear regime can be expressed as

$$I_{ds} = \frac{\mu}{1 + \theta_{ch}(V_{gs} - V_{th})} C_i \frac{W}{L} (V_{gs} - V_{th})(V_{ds} - I_{ds}R_C) \quad (6 - 1)$$

$$I_{ds} = \frac{\mu}{1 + \theta(V_{gs} - V_{th})} C_i \frac{W}{L} (V_{gs} - V_{th})V_{ds} \quad (6 - 2)$$

where μ , θ_{ch} , C_i , W , L , R_C , V_{th} , and θ denote the intrinsic mobility in linear regime, the mobility attenuation factor from channel, capacitance between the channel and the gate per unit area, the channel width, the channel length, the contact resistance, the threshold voltage and the mobility attenuation factor from both of channel and contact, respectively. From the definition of transconductance $g_m = \partial I_{ds} / \partial V_{gs}$, the Y-function is given by

$$Y = \frac{I_{ds}}{\sqrt{g_m}} = \frac{I_{ds}}{\sqrt{I_{ds} / [1 + \theta(V_{gs} - V_{th})] (V_{gs} - V_{th})}} = \sqrt{\mu C_i V_{ds} \frac{W}{L} (V_{gs} - V_{th})} \quad (6 - 3)$$

From the slope of the Y-function versus V_{gs} , the value s_1 of $\sqrt{\mu C_i V_{ds} W / L}$ can be extracted, and the value s_1 is a constant.

Define another function X as

$$X = \frac{1}{\sqrt{g_m}} = \frac{1 + \theta(V_{gs} - V_{th})}{\sqrt{\mu C_i V_{ds} W / L}} \quad (6 - 4)$$

θ could be extracted by plotting X-function versus V_{gs} . At strong accumulation, a linear behaviour is obtained with slope of s_2 , which attributes to the attenuation from contact

resistance.

$$\theta_c = \frac{\partial X}{\partial V_{gs}} \times \sqrt{\mu C_i V_{ds} W/L} = s_1 s_2 \quad (6-5)$$

Combine the equation (6-1) and (6-2). The attenuation factor θ can be described as following equation.

$$\theta = \theta_{ch} + \theta_c = \theta_{ch} + \mu C_i R_C \frac{W}{L} \quad (6-6)$$

where θ_c is the mobility attenuation factor from the contact.

$$R_C = \frac{\theta_c}{\mu C_i \frac{W}{L}} = \frac{s_2}{s_1} V_{ds} \quad (6-7)$$

6.3 Results and discussions

The back-gate top-contact MoS₂ FETs were developed with transferred top functionalized Au electrodes by making use of a novel dry transfer technique. The fabrication process is portrayed in Figure 6.1 (see the section of 6.2.2 for fabrication details). A patterned electrode array was first evaporated onto an octadecyltrichlorosilane (OTS) functionalized sacrificial silicon substrate through a copper shadow mask. These patterned electrodes are then functionalized with thiolated molecules after the UV/ozone cleaning treatment. Subsequently, these functionalized electrodes can be mechanically desorbed from the silicon, then dry transferred and laminated on a polydimethylsiloxane (PDMS) surface to form an interelectronic gap using a mechanical probe.^[39; 40] The MoS₂ flakes were mechanically exfoliated and transferred to the top of highly doped silicon (n++) covered with a SiO₂ (270 nm) layer and an insulating spin-coated polymer layer (Cyttop, 85 nm) as dielectrics. Compared with conventional Si/SiO₂ interface, the Cyttop film represents an ideal substrate for 2D semiconductor, because of its low surface energy, nearly free trap states, absence of dangling bonds and low permittivity ($\epsilon = 2.1$).^[49; 50] Finally, the previously prepared PDMS film exposing functionalized electrodes are aligned under a microscope and physically laminated on the top of the MoS₂ flake, resulting in a top-contact

FET device with functionalized electrodes. The PDMS film is then kept on the top of the device for suitable encapsulation and protection of the device.^[51]

The thickness of MoS₂ flakes was monitored by atomic force microscope (AFM) and Raman spectroscopy. We have used MoS₂ flakes with the thickness of 8~12 nm (12~19 layers) since such multilayered flakes are robust and they exhibit negligible flake-to-flake variation in the electron affinity and carrier mobility, as well as a low sensitivity to environment. The latter is key since our use of SAMs coated electrodes is aimed at modifying the WF of the electrode rather than at chemically modulating the local electronics of the MoS₂ layers via dipole induced doping or charge transfer.^[12; 52]

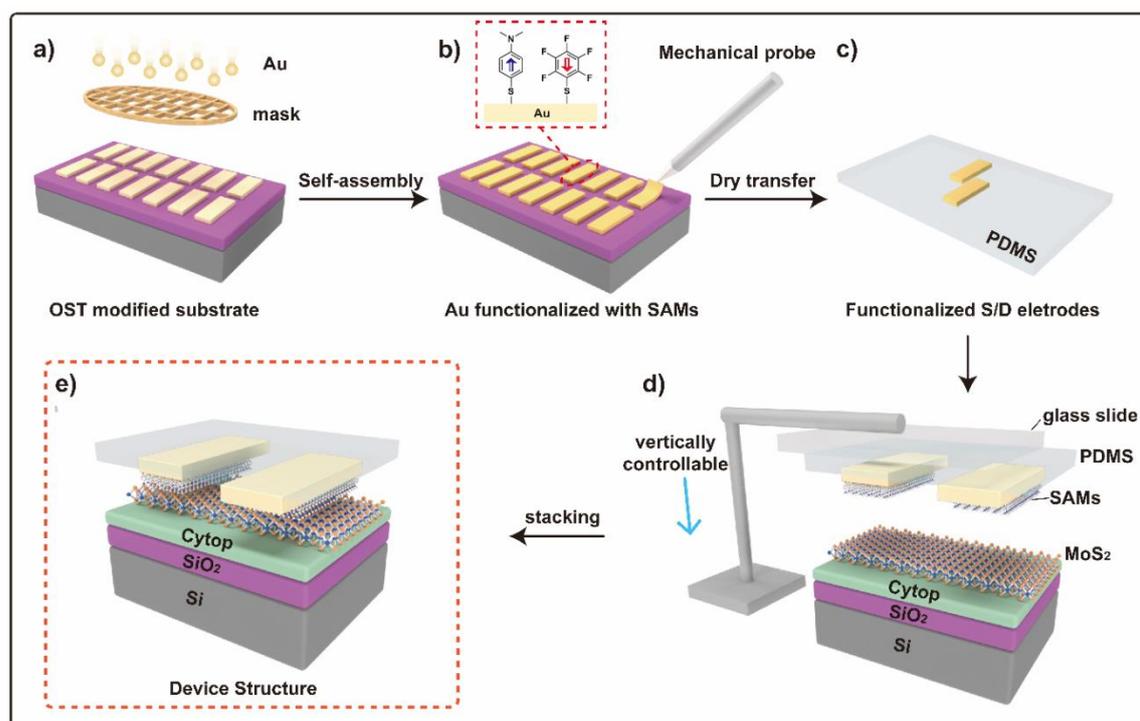


Figure 6.1 Schematic illustration of the procedure steps for the preparation of top-contact FETs devices with functionalized electrodes. a) Gold evaporation, b) functionalization via SAMs chemisorption, and c) transfer of functionalized electrodes onto PDMS mold. d) Dry transfer and lamination of functionalized electrodes from the mold onto the MoS₂ flake. e) Scheme of FETs structure with SAMs functionalized electrodes. Inset in b) Structures of the thiolated molecules (DABT and PFBT) used in this study. The dipole moment orientation within the molecules is indicated with colored arrows.

Figure 6.1e shows the architecture of the functionalized FETs device. These top (functionalized-) electrodes and 2D semiconductor are in contact and interacting uniquely via vdW forces. The latter has several advantages such as a lower FLP effect, reduction of the defect-induced gap states and suppression of the metal-induced gap states.^[53; 54] The dry transfer technique also possesses unparalleled advantages including the possibility to transfer (functionalized-) electrodes creating a damage-free interface when compared with the more invasive conventional thermal deposition. On the other hand, compared with traditional functionalized bottom-contact configuration, the SAMs in this top-contact configuration is only used to modify the top metal electrode, and have negligible influence on the semiconductor's structure and electronics. Therefore, the devices characteristics resulting from the exposure to various SAMs functionalized electrodes can be directly correlated to the dipole induced changes in the electron injection barriers, which is also known as SBH (Φ_{SB}).

According to the Schottky-Mott rule, the barrier height is defined as the potential difference between WF of the (functionalized-) electrode (W_f) and the electron affinity (χ , defined as the difference between the semiconductor conduction band edge and the vacuum level) of multilayer MoS₂ semiconductor, that is,

$$\Phi_{SB} = W_f - \chi \quad (6 - 8)$$

Unfortunately, due to severe FLP, the Schottky-Mott model is not applicable experimentally.^[55; 56] In this case, the electron SBH can be characterized by introducing pinning factor (S) and charge neutrality level (CNL, Φ_{CNL}).

$$\Phi_{SB} = S(W_f - \Phi_{CNL}) + (\Phi_{CNL} - \chi) = S \cdot W_f + b \quad (6 - 9)$$

The S was defined as the slope,

$$S = d\Phi_{SB}/dW_f \quad (6 - 10)$$

The S was varied from 0 for perfect FLP to 1 for no FLP. For MoS₂, a severe FLP effect of $S = 0.02 \sim 0.11$ has been reported by evaporating various metal electrodes.^[14; 55] In view of this, MoS₂ exhibits electron transport behaviour.

6.3.1 Characterization of electrodes

The characterization of the chemically functionalized electrodes was carried out prior to their transfer for preparation of FETs.

6.3.1.1 Morphological characterization

To assess the monolayer morphology, we performed atomic force microscopy (AFM) imaging and contact angle (CA) measurements (see Figure 6.2 and 6.3). The root-mean-square (R_{RMS}) roughness of evaporated Au as determined on an area of $2 \times 2 \mu\text{m}^2$ amounts to 2.05 nm.

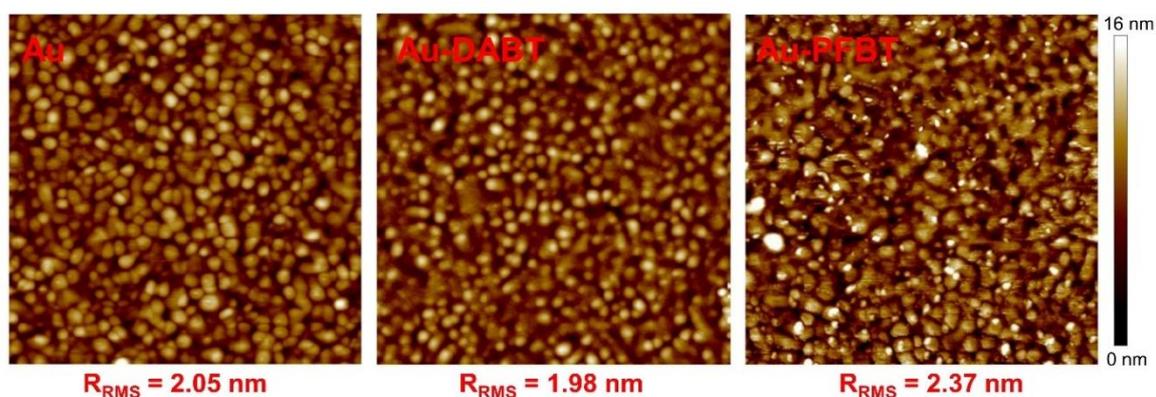


Figure 6.2 AFM morphology images of bare gold, DABT functionalized gold electrode and PFBT functionalized gold electrode. The values below indicate the root-mean-square roughness (R_{RMS}). Image size = $2 \times 2 \mu\text{m}^2$.

After functionalization with 4-(dimethylamine)benzenethiol (DABT) and 2,3,4,5,6-pentafluorobenzenethiol (PFBT) chemisorbed SAMs, it slightly changed to 1.98 nm and 2.37 nm, respectively. Such functionalization is also accompanied by a change in the CA from the 77.6° of bare electrode to the 86.7° and 58.0° of the PFBT and DABT coated films, respectively. The DABT and PFBT molecules, whose structure is displayed in Figure 6.1b and 6.4a, were chosen as prototypical thiolated molecules because they are rigid and shape persistent and are either strong electron-donor or acceptor. The short contour length along the molecular backbone simply comprising a benzene ring not only ensures good electrical conductivity and sufficient thermal stability, but also minimizes additional

tunnelling barriers between MoS₂ and metal electrode.^[57-59]

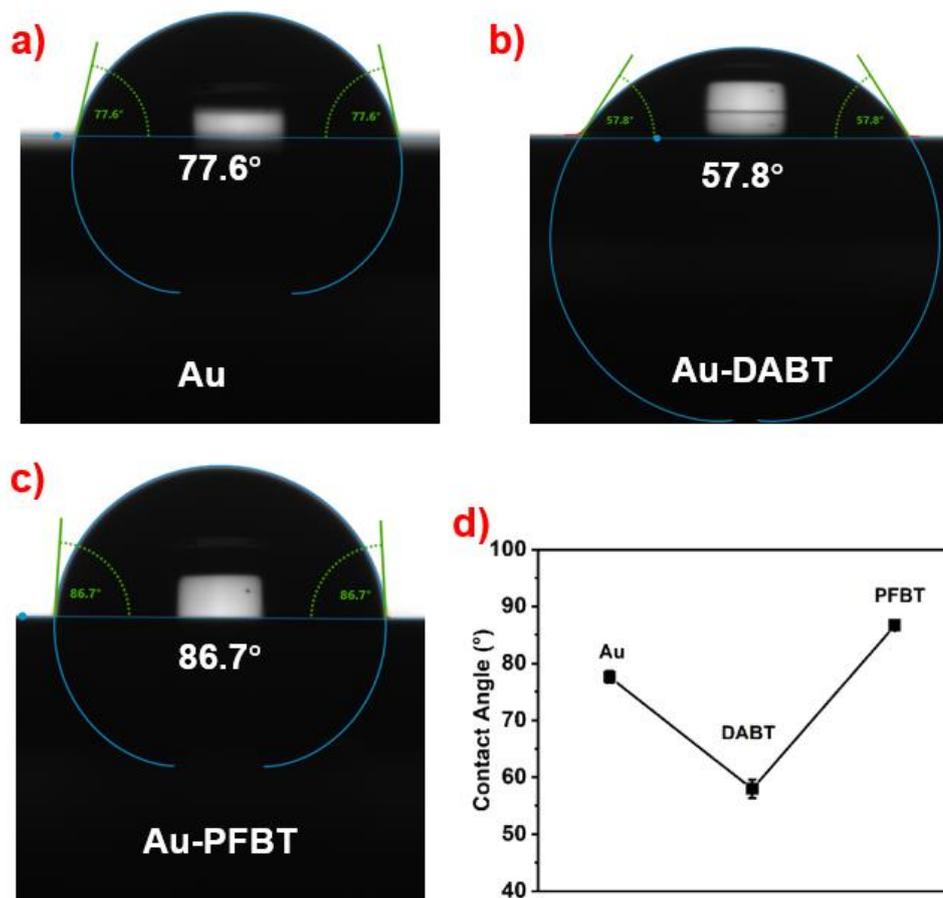


Figure 6.3 Contact angles of Au surfaces modified with benzenethiol derivatives (DABT and PFBT) and that of a bare Au surface. The water contact angle picture and the contact angle values at 0 min is 77.6°, 57.8°, and 86.7°, respectively.

6.3.1.2 Work function characterization

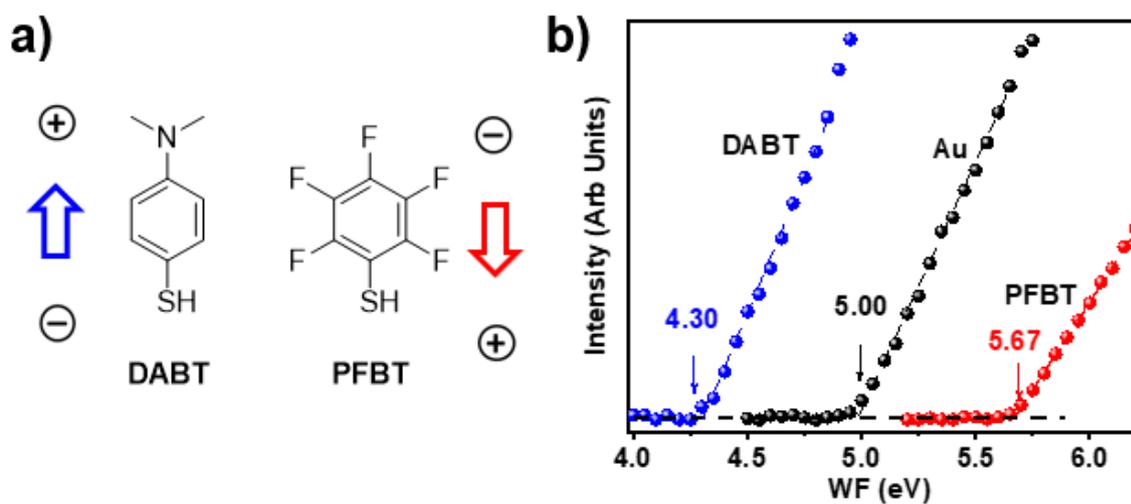


Figure 6.4 a) Molecular structures of DABT and PFBT, marked with dipole moment orientation. b) Secondary electron cut-off of DABT functionalized (blue dots) and PFBT functionalized (red dots) Au electrodes compared to the corresponding unfunctionalized Au electrodes (measures by PYSA).

The strong dipoles of molecules allow to modify the Au electrodes WF of a magnitude as high as 0.7 eV. In particular, the DABT molecule with its lone electron pair shifts the WF of Au electrode from 5.00 eV to 4.30 eV, while the fluorine-rich PFBT molecule increased it to 5.67 eV (see table 6.1 as well as Figure 6.4), as determined by Photoelectron Yield Spectroscopy in Air (PYSA). The unfunctionalized electrodes were utilized as a reference in the control experiment.

6.3.1.3 Elemental analysis

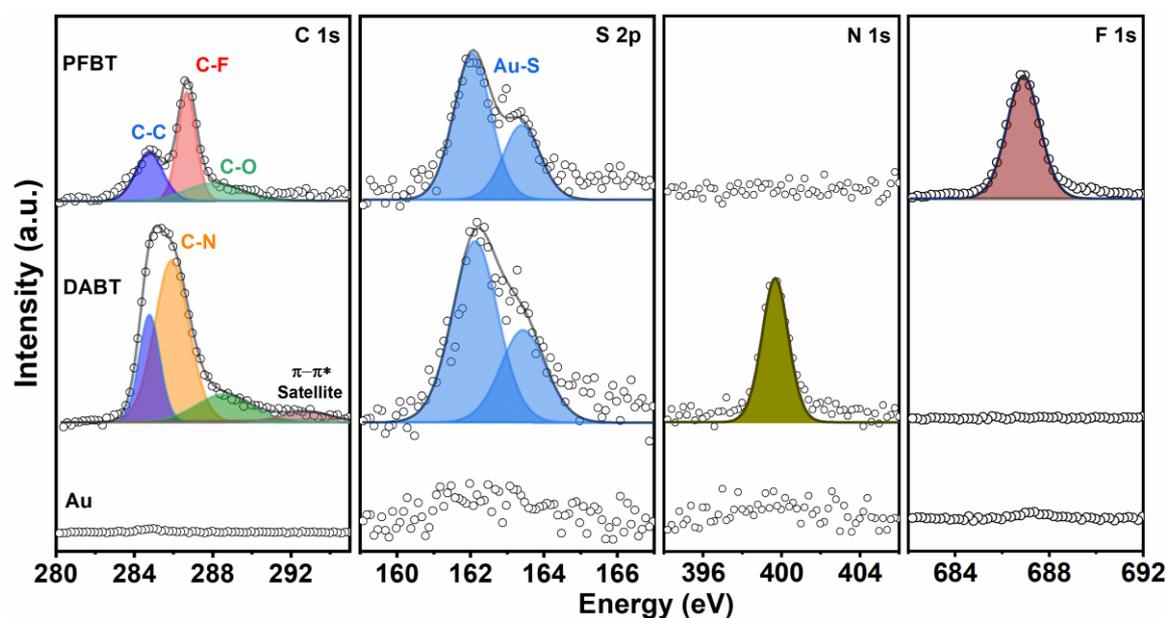


Figure 6.5 High-resolution XPS spectrum with C 1s, S 2p, N 1s and F 1s of DABT and PFBT functionalized Au electrodes compared to the corresponding bare Au surface.

The chemical composition of the electrodes assembled with the DABT and PFBT molecules can be directly analyzed by X-ray Photoelectron Spectroscopy (XPS). Figure 6.5 shows the C 1s, S 2p, N 1s and F 1s spectra of modified electrodes and compared to the bare electrode. The C 1s peaks of DABT monolayer exhibit the typical C-C bond and C-N bond at 284.8 eV and 285.3 eV, respectively. Similarly, PFBT monolayer displays the C-

C bond and C-F bond at 284.8 eV and 286.7 eV, respectively. A clear single symmetric peak of N 1s (at 399.7 eV) and F 1s (at 686.9 eV) provide unambiguous evidence for the formation of the monolayer, by indicating the presence of DABT and PFBT molecules, respectively.^[60; 61] In addition, S 2p core level spectrum of SAMs showed only one doublet peak at 162.1 eV corresponding to S chemisorbed onto the gold surface through a thiolate bond.^[62]

6.3.2 Characterization of MoS₂ crystal

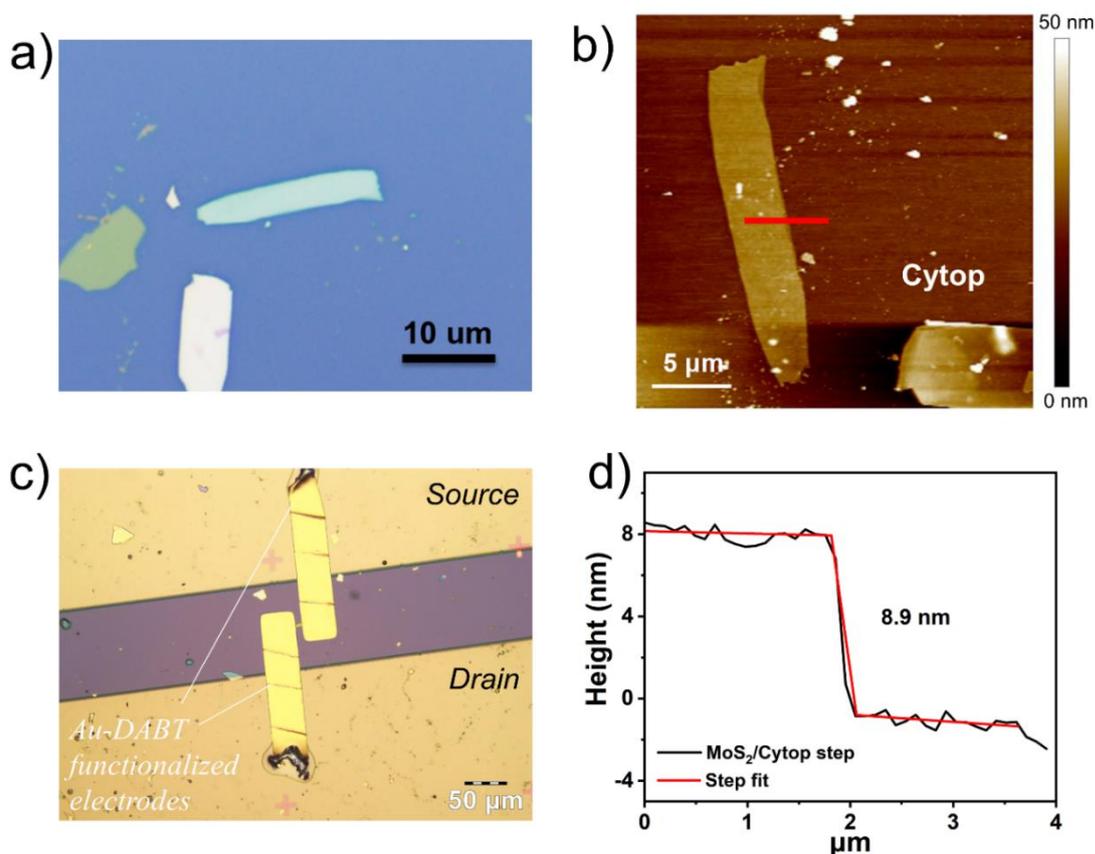


Figure 6.6 a-c) Top-view optical and topographical AFM images of PDMS assisted exfoliated MoS₂ flake sample as well as corresponding device optical image. d) Height profiles of flake along the red short line in AFM image.

The number of layers of MoS₂ flakes were confirmed by a Raman scattering analysis and an AFM analysis, as shown in Figure 6.6 and Figure 6.7. The sample thickness of 8~12 nm (thickness of monolayer MoS₂ = ~0.65 nm, the thickness of flake in figure 6.6 is 8.9 nm) from the AFM measurement and the frequency difference of 24.8 cm⁻¹ between the

E_{2g} and A_{1g} modes in the Raman spectra supported the successful acquisition of 12~19 layers MoS₂ via mechanical exfoliation. Photoluminescence (PL) spectrum showed the trion X⁻ characteristic peaks of multilayer MoS₂ flake.

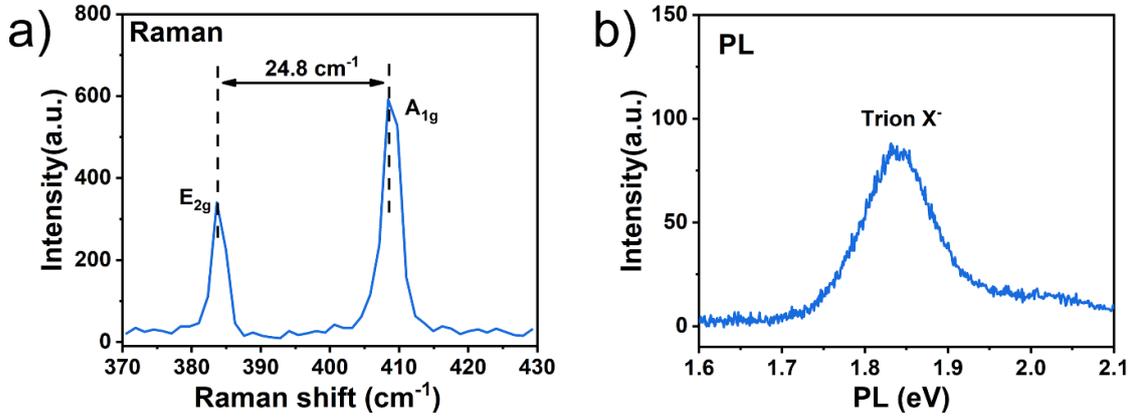


Figure 6.7 Raman (a) and PL (b) spectra of multilayer MoS₂ flakes, measured at room temperature in ambient.

6.3.3 Electrical characterization of FETs

To investigate the electrical properties of the SAMs modified top-contact electrodes on the carrier injection, we measured the transfer and output characteristics for the unfunctionalized, PFBT functionalized, and DABT functionalized MoS₂ FETs under nitrogen environment (Figure 6.8). For the sake of comparison, channel length and width normalized current ($I = I_{ds} \frac{L}{W}$) of MoS₂ FETs as a function of back-gated voltage (V_{gs}) are displayed in Figure 6.8b and 6.8c, where I_{ds} is the source drain current, and L/W is the length/width ratio of the channel. Figure 6.8d-f shows the typical output curves of devices. Table 6.1 summarizes the extracted electrical parameters of these devices. The non-ohmic “S” shape of the output characteristics at lower bias indicates an obvious Schottky barrier in the carrier injection region, especially for PFBT functionalized electrodes.^[20; 63] With the increasing bias voltage, the contact between the electrode and MoS₂ displays ohmic-like behaviour. The device comprising unfunctionalized Au electrode exhibit transfer curves typical for electron transport in MoS₂ FETs with a threshold voltage (V_{th}) of 7.1 V, which is in contrast to the p-type behavior of previous studies.^[12] This is mainly attributed to

substrate induced doping and the appreciable roughness of the electrode surface.^[49; 50; 53]

The linear carrier mobility μ can be extracted by the following equation

$$\mu = \frac{dI_{ds}}{dV_{gs}} \times \frac{L}{WC_i V_{ds}} \quad (6-11)$$

where L and W are the channel length and width, and C_i is the capacitance of bilayer dielectric per unit area.

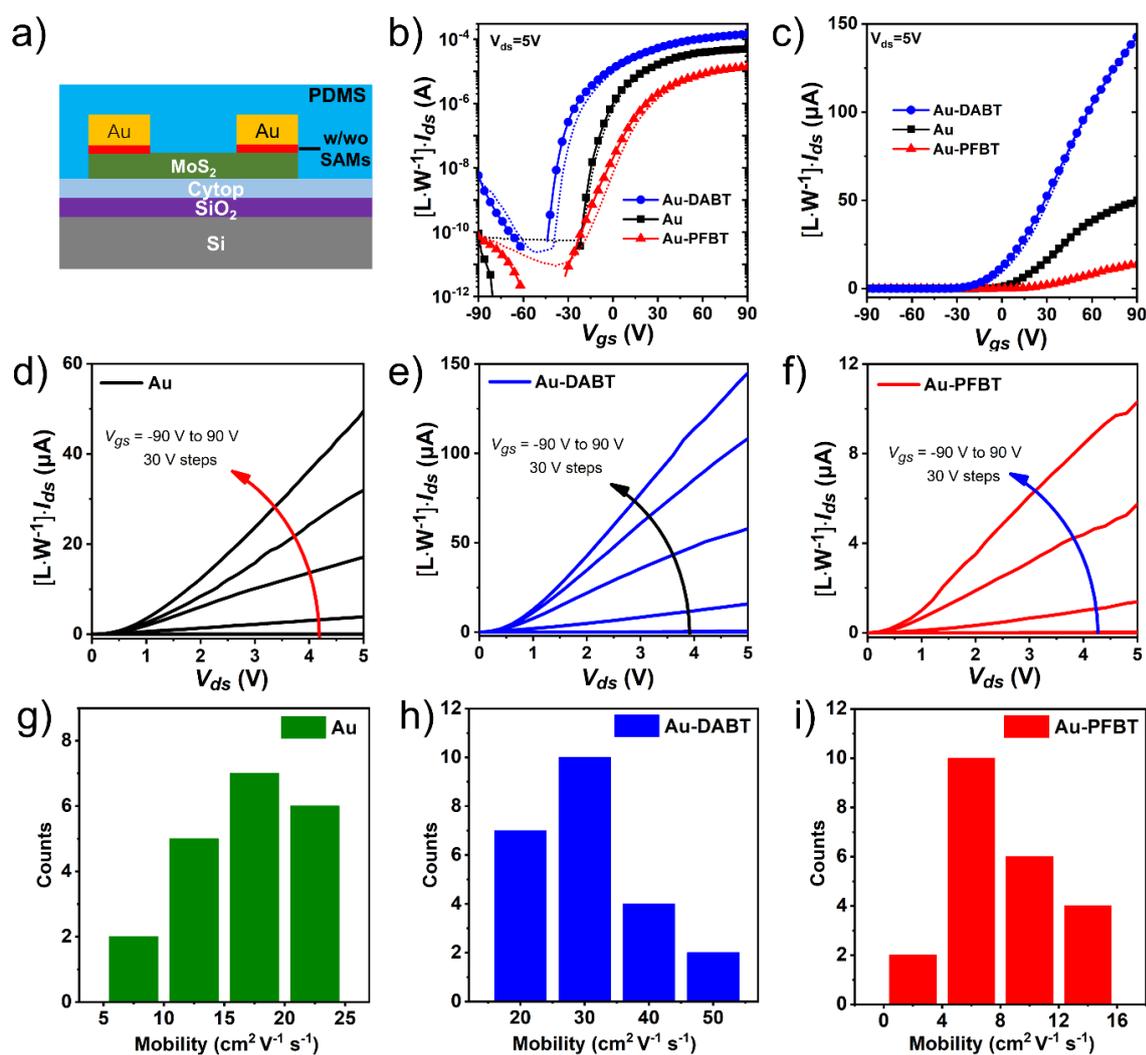


Figure 6.8 a) Scheme of top-contact FETs with functionalized electrodes structure. (b-i) Comparison of MoS₂ top-contact FETs with bare Au electrode and SAMs functionalized electrodes. b,c) Semilogarithmic and linear plot of I_{ds} vs V_{gs} transfer curves at a fixed bias voltage (V_{ds}) of 5 V. d-f) I_{ds} vs V_{ds} output curves at a step V_{gs} from -90 V to 90 V with a 30 V intervals. g-i) Statistical distribution of the linear mobility of top-contact FETs devices with functionalized and

unfunctionalized electrodes.

The statistical distribution and average values of the apparent linear mobility (μ) are depicted in Figure 6.8g-i and table 6.1. The best performance was obtained for the device with DABT treated electrode with the average μ values of $30.6 \pm 8.8 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. While the devices with bare Au electrode exhibit moderate performance with the average μ values of $16.9 \pm 5.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and the FET containing the PFBT treated electrode exhibit degraded performance with the average μ values of $8.1 \pm 3.6 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. As a result, compared with bare gold electrodes, DABT treated electrodes facilitate the charge injection and improve the device performance, while PFBT-treated electrodes suppress it. Moreover, these results also exhibit better performance than the bottom-contact configuration.^[20]

Table 6.1 Parameters of reported top-contact (functionalized) electrode FETs devices.

Type	CA [°]	WF [eV]	SBH[eV]	μ [$\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{S}^{-1}$]	V_{th} [V]	ΔV_{th} [V]	Δn [cm^{-2}]	R_c [$\text{k}\Omega$]
Au	77.6 ± 1.0	5.00	0.19	16.9 ± 5.2	7.1 ± 5.9	-	-	50.6 ± 8.5
Au- DABT	58.0 ± 1.7	4.30	0.07	30.6 ± 8.8	-14.3 ± 11.5	-21.4	1.08×10^{12}	17.6 ± 4.8
Au- PFBT	86.7 ± 0.4	5.67	0.53	8.1 ± 3.6	18.1 ± 9.4	11.0	-5.54×10^{11}	83.5 ± 12.3

WF represents work function. CA represents contact angle. The SBH Φ_{SB} values were measured experimentally. Δn represents charge carrier density change. The contact resistance (R_c) was simulated by Y function method.

Besides the relevance of the field-effect mobility, the threshold voltage engineering is also important towards the device performance optimization.^[64-67] As shown in Figure 6.8c and 6.13h, DABT functionalized electrodes resulted in a significant negative shift of V_{th} (-21.4 V) and an apparent increase of I_{ds} without augmenting the hysteresis, evidencing the n-doping of MoS₂. From the V_{th} shift, the change of charge carrier densities (Δn) can be estimated from following formula,^[68]

$$\Delta n = \frac{C_i \Delta V_{th}}{e} = 5.04 \times 10^{10} \Delta V_{th} \text{ cm}^{-2} \quad (6 - 12)$$

where Δn is the change in electron density, e is the elementary charge. The quantified Δn amounts to $1.08 \times 10^{12} \text{ cm}^{-2}$, being a value comparable to those observed when using traditional n-dopants.^[68-70] On the other hand, a clear positive shift of V_{th} (11.0 V) and a substantial decrease of the overall current were obtained upon PFBT functionalized electrodes also without increasing the hysteresis, evidencing a p-doping effect. The estimated Δn amounts to $-5.54 \times 10^{11} \text{ cm}^{-2}$, in line with reported molecular p-dopants.^[70-73]

However, a previous report by Lee et al.^[48] demonstrated that the contact region modification with thiolated molecules of any type can be instrumental to improve device performance by reducing the injection tunneling barrier and by creating additional tunneling percolation pathways. This is because thiol molecules were directly deposited on the flake surface and chemically adsorbed at the sulfur vacancies of MoS₂ by generating a covalent bond with Mo atoms. The healed and repaired sulfur vacancy defects bring about the elimination of interface states and the improvement of overall performance.^[74-76] It is reported that defects on the surface of MoS₂ can be utilized to control the device electrical behaviour.^[77-79] Moreover, the thermally evaporated Au with MoS₂ interface is degenerately doped, which is different from the transferred Au.^[54] Our results above based on the top-contact configuration clearly revealed that in absence of chemical functionalization of the MoS₂, the increase of WF of the Au electrode yields a significant degradation of the device performance. This also suggests that SAMs functionalization of top-electrode is an efficient way to control carrier transport in MoS₂ transistors. Significantly, the possibility of transferring metal electrodes functionalized with appropriate SAMs makes it possible to tune the device performance with a high precision.

6.3.4 Temperature dependent electrical characterization

To further evaluate the impacts of SAMs functionalized electrode on the charge injection, we extracted the SBH by using the following thermionic emission equation:^[55; 80]

$$I_{ds} = AA^*T^2 \exp\left(-\frac{\Phi_{SB}}{k_B T}\right) \exp\left(\frac{qV_{ds}}{k_B T}\right) \quad (6-13)$$

$$\Phi_{SB} = -k_B \left[\frac{d \ln(I_{ds}/T^2)}{d(1/T)} \right] \quad (6-14)$$

where A is the junction area, A^* is the equivalent Richardson constant, k_B is the Boltzmann constant and T is temperature. The Φ_{SB} is the slope of a linear fit to $\ln(I_{ds}/T^2)$ as a function of $1/T$, equation 6-14. In this way, the Φ_{SB} under various gate voltages and the effective Φ_{SB} (under the flat-band condition) can be obtained. Figure 6.9a-c show the temperature dependent transfer characteristics of MoS₂ transistors with bare Au electrode and SAMs functionalized electrodes. The extracted Φ_{SB} at various gate voltages for all devices are shown in figure 6.9a-c. As can be seen, the effective Φ_{SB} amounts to 0.19, 0.07 and 0.53 eV for bare Au electrode, DABT and PFBT functionalized electrode, respectively.

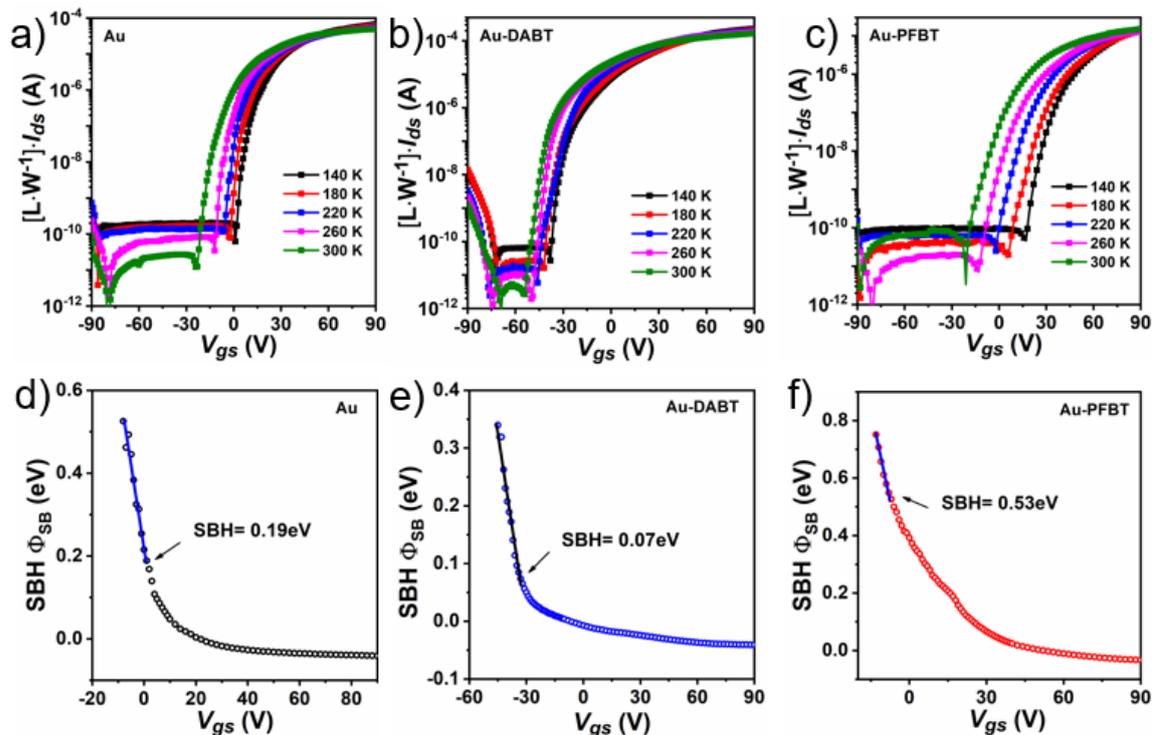


Figure 6.9 a-c) The transfer curves of MoS₂ transistors with functionalized and unfunctionalized electrodes under various temperature. d-e) Extracted SBH values at various gate voltages for MoS₂ FETs with functionalized and unfunctionalized electrodes.

The extracted effective Φ_{SB} for various electrodes as a function of the corresponding work functions are displayed in Figure 6.10. The dash line is the linear fitting with a slope indicating a pinning factor (S) of 0.33. The value is much larger than the previously reported values of 0.02~0.11 for deposited metals, and better than metal oxide interlayer of 0.24.^[14; 55] This confirms that metal electrodes functionalized with various SAMs can be used to alleviate FLP and tune the SBH of multilayered MoS₂ FETs.

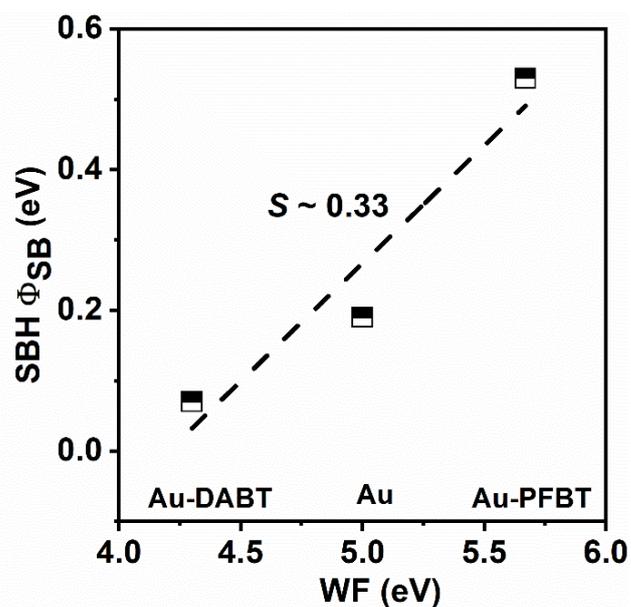


Figure 6.10 i) Experimentally determined effective electron SBH as a function of work function for the bare Au, DABT and PFBT functionalized electrode cases.

6.3.5 Charge transport mechanism

Figure 6.11 illustrate the mechanism of SAMs functionalized electrode on the charge injection. Interfacial charge transfer process takes place upon deposition of the electrodes onto the semiconducting MoS₂ flake. For device based on bare Au electrodes (figure 6.11a), a Φ_{SB} of 0.19 eV was reported. As shown in figure 6.11b, the functionalization with DABT molecules determines a decrease in the WF (4.30 eV) significantly reducing the Φ_{SB} hence promoting carrier injection from electrode to semiconductor, thereby overall improving the device performance. On the contrary, the PFBT functionalized electrode (5.67 eV) displays a major enhancement in the Φ_{SB} , worsening the electron injection at the

electrode-semiconductor interface, hence yielding an overall degradation of the device electrical characteristics (figure 6.11c).

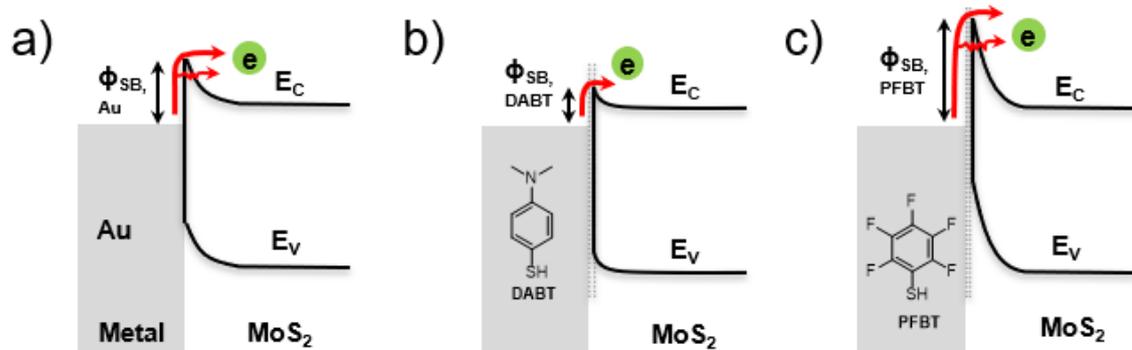


Figure 6.11 a-c) Energy band diagrams for multilayer MoS₂ crystal contacted with bare gold electrode (b), DABT (a) and PFBT (c) functionalized gold electrode. The red arrows represent the different injection mechanisms. From top to bottom: thermionic emission, field emission (tunneling).^[81] The gray dotted line represents the molecular spacing.

6.3.6 Contact resistance

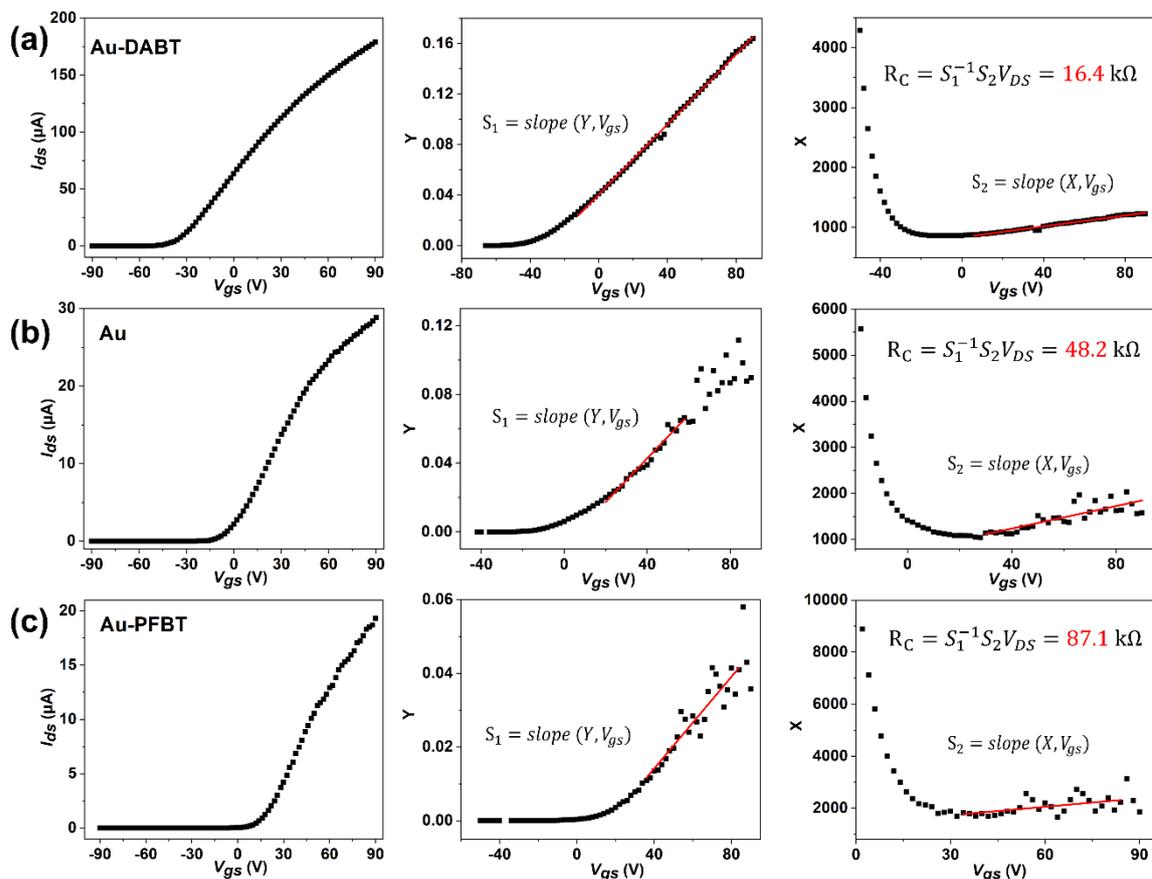


Figure 6.12 I_{ds} vs V_{gs} transfer curves, Y-function and $1/\sqrt{g_m}$ of FETs with bare Au (b) and DABT (a) and PFBT (c) functionalized electrodes.

Due to the limitation of device configuration, conventional transfer length method (TLM) and Kelvin probe force microscopy (KPFM) method cannot be applied in our case. Therefore, the Y-function method was used here to extract contact resistance. Figure 6.13 shows the contact resistance (R_C) of the various devices which was evaluated by using Y-function method (see Figure 6.12), being an established protocol for evaluating R_C in organic materials and TMDs semiconductor based FETs.^[43; 45; 46] Detailed information regarding the Y-function method can be found in section 6.2.3. The extracted R_C value amounts to 17.6 ± 4.8 , 50.6 ± 8.5 , and 83.5 ± 12.3 $k\Omega$ for DABT functionalized, unfunctionalized, and PFBT functionalized electrodes in top-contact MoS_2 FETs, respectively. The estimated width-normalized R_C resulted 66.2 ± 33.8 , 144.8 ± 33.1 , and 337.8 ± 166.2 $k\Omega \cdot \mu\text{m}$, respectively. These findings are consistent with the trends of μ and V_{th} , and are in line with previous reports.^[48; 81]

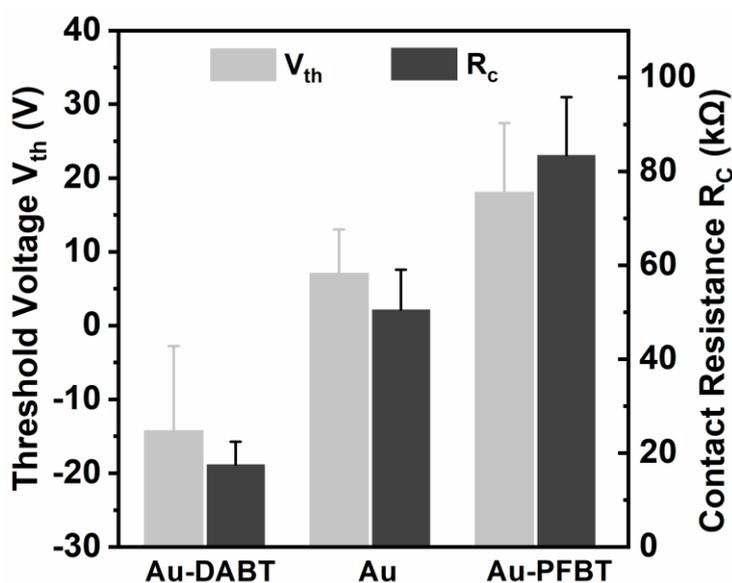


Figure 6.13 Threshold voltage V_{th} and contact resistance R_C of FETs devices for the bare Au, DABT, and PFBT functionalized electrodes cases.

6.3.7 Impact of SAMs on carrier transport

The very interface between the molecules and the MoS_2 is notorious to have a minimal

impact of the charge transport through the electrode-molecular monolayer-MoS₂ semiconductor junction as comprehensively explained by Liu et al.^[12] Here we show that the molecules we have chosen has a minimal effect on the carrier transport through the device. The molecular monolayer operates as an ultrathin tunneling barrier for charge injection at the electrode-semiconductor interface. In order to minimize the influence of such tunneling barrier, DABT and PFBT were selected because they combine the following characteristics: First, the length of these molecules is below 1 nm (about 6 Å), and the short contour length of the conjugated molecule ensures minimal tunneling barrier.^[59]

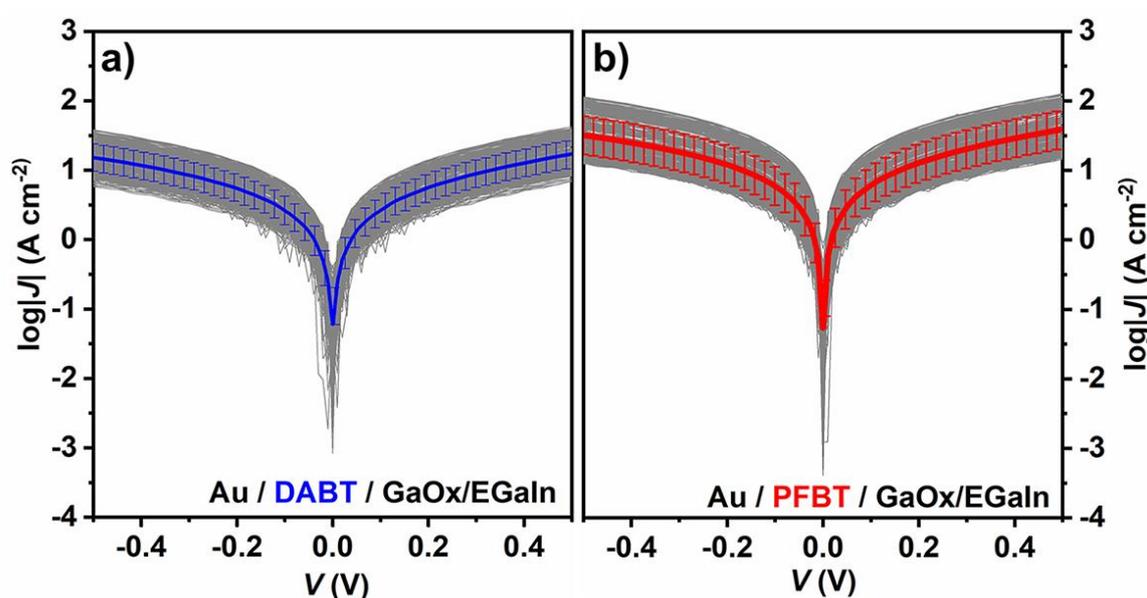


Figure 6.14 Electrical tunneling current of the DABT and PFBT SAMs junctions on Au using an EGaIn droplet. The gray curves show the trace and retrace of more than 300 J(V). The blue and red line with log-standard deviations represent the average value.

Good conductivity of the DABT and PFBT SAMs on Au also can be seen from EGaIn droplet junction measurement (Figure 6.14). Second, the charge transport type through the shortest conjugated aromatic molecule (single benzene ring) is super fast temperature independent tunneling transport.^[52; 82-85] Conversely, for long molecules the barrier becomes thicker determining a transition from tunneling to hopping mechanism which brings into play also smaller current temperature dependence.^[86-92] In this case the devices operation and transport will be injection limited. Third, due to the transition voltage, the

tunneling resistance of the molecular junction decreases significantly as the voltage increases, especially when the bias exceeds 1 V.^[91-93] Given that in our FETs devices electrical characterizations the applied source-drain bias is 5 V, the tunneling resistance for the charge injection is minimal. Despite the small magnitude of the tunnelling barrier due to the molecular monolayer, the accurate theoretical description of the electrical characteristics of the charge injection in the device should comprise the interplay of the energy levels matching and the tunneling barrier.

6.3.8 Schottky diodes with asymmetric electrodes

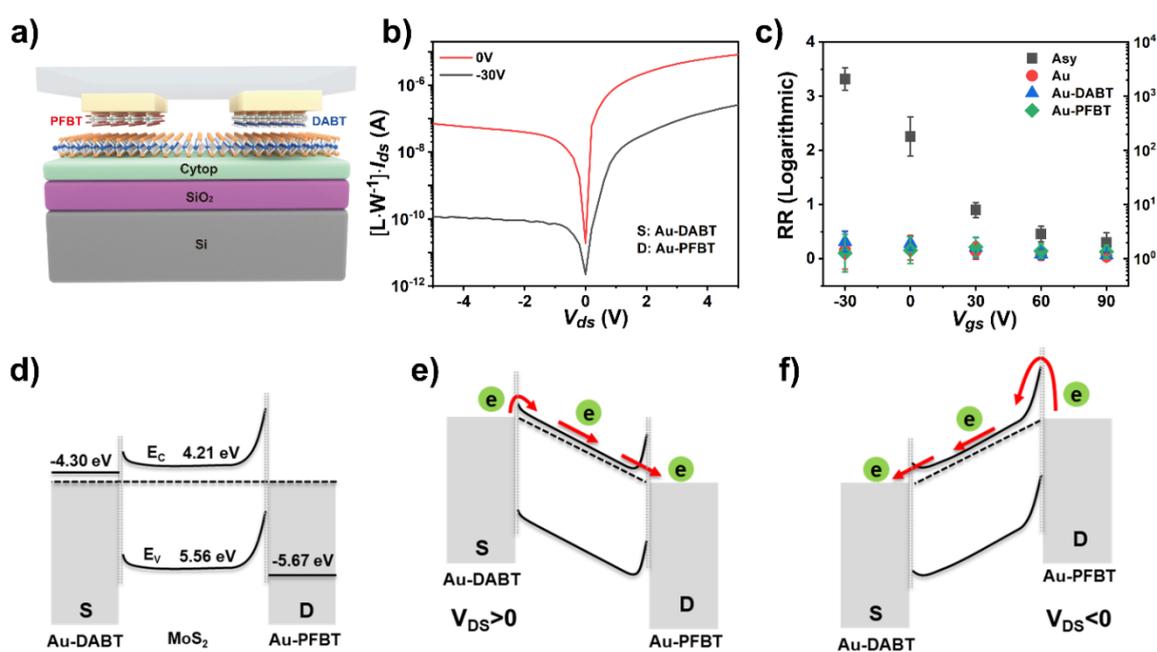


Figure 6.15 (a) Schematic illustration of asymmetric MoS₂ FETs device. (b) Semilogarithmic plot of the $I_{ds} - V_{ds}$ output curve at 0 V and -30 V gate bias conditions. The drain electrode is PFBT functionalized electrode and the DABT functionalized electrode is grounded. (c) Rectification ratio at V_{ds} in different gate bias conditions. d-f) Energy band diagram of asymmetric MoS₂ FETs devices. (d) Energy band diagram at thermodynamic equilibrium. The black lines show the original WF energy of DABT and PFBT functionalized electrode. (e) Energy band diagram at positively biased source-drain condition. (f) Energy band diagram at negatively biased source-drain condition.

By taking the method a step further, it is also possible to transfer pairs of diversely SAMs functionalized electrodes to introduce electronic asymmetry in the device thereby enabling the fabrication of Schottky diodes. Figure 6.15a shows the schematic cartoon of the metal–semiconductor–metal (MSM) Schottky diode produced by transferring DABT and PFBT

functionalized electrodes as vdW contacts. The $I_{ds} - V_{ds}$ output characteristics of Schottky diode as a function of V_{gs} are reported in figure 6.15b and figure 6.16. The use of DABT and PFBT functionalized asymmetric electrodes yielded a decrease of the V_{gs} from 90 V to -30V, with a significant increase in the rectification ratio (RR) reaching a maximum value of 10^3 at the V_{gs} of -30 V, as shown in figure 6.15c, which is comparable to the diodes produced using asymmetric metal or oxidized metal contacts.^[94-96] This can be understood that negative V_{gs} shifts the energy bands upward, which results in the increase in the injection barrier. With the increasing of V_{gs} , the energy bands were shifted downward, which makes the channel more conductive, and an increased current is observed. At strong accumulation region, the barriers on both sides are negligible and the RR becomes uniform.^[94]

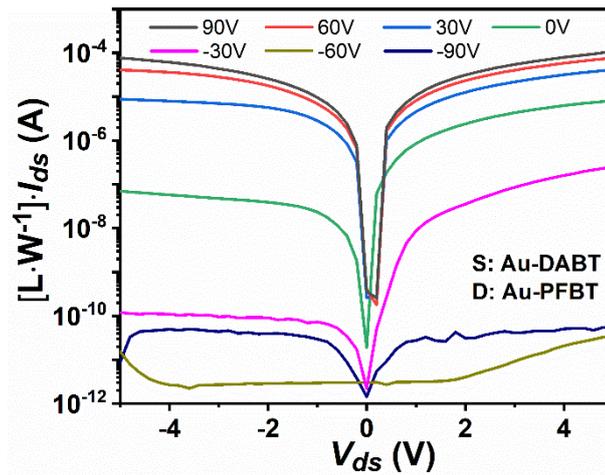


Figure 6.16 Semilogarithmic plot of the $I_{ds} - V_{ds}$ output curve at different gate bias conditions. The drain electrode is PFBT functionalized electrode and the DABT functionalized electrode is grounded.

Figure 6.15d reports a scheme of the energy band diagrams for functionalized asymmetric electrodes MoS₂ FETs. As aforementioned, the WF of the DABT and PFBT functionalized Au electrodes are different. Once the electrodes are in contact with the semiconductor, the charge will flow from the semiconductor to the Fermi level of the electrodes, thereby forming different space charge regions on both two contact areas of the semiconductor surface, which also results in different injection barrier heights for the DABT and PFBT

functionalized electrodes (Figure 6.15d). When the DABT functionalized electrode is grounded, the carriers can be injected through a lower barrier from DABT functionalized electrode into semiconductor (Figure 6.15e) when a positive V_{ds} is applied. Conversely, when a negative V_{ds} is applied, the carriers must overcome a higher barrier to be injected from PFBT functionalized electrode into the semiconductor (Figure 6.15f), yielding a poor electron injection and lower currents, leading to a rectification.

6.4 Conclusions

In summary, we have reported for the first time on the integration of chemically functionalized source and drain electrodes in top-contact MoS₂ FETs by using the dry transfer technique. We have demonstrated that the SAMs functionalized electrodes in top-contact configuration can significantly modulate the performance of FETs by choosing commercially available thiol molecules with different dipoles moment. In perfect agreement with the theoretical prediction, the electrodes functionalization determines a reduction of the injection barrier which yields in an efficient improvement of the device performance. Furthermore, we have upgraded this approach to enable the asymmetric functionalization of source and drain electrodes that resulted in the fabrication of high-performance Schottky diodes. This technique not only eliminates the influence of bottom electrode modification on the semiconductor by enhancing the area of injection, but also offers a viable approach for the functionalization of top electrodes for tuning the device characteristics. The work we presented here thus demonstrated a generally applicable functionalized metal integration strategy for the construction of high-performance staggered 2D semiconductor-based FETs, which can be extended to other delicate functional materials, such as organic single crystal or thin-film semiconductors, and to other applications in which asymmetry is required like planar inverters, light-emitting devices and solar cells.

6.5 References

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Chapter 7 Solvent-Free Van der Waals Integration of Functionalized Electrodes for Two-Dimensional Semiconductor Device Polarity Modulation

Two-dimensional (2D) semiconductors have attracted considerable interest for applications in digital logic circuits. Since direct metal deposition can lead to interfacial disorder and Fermi level pinning, the transfer of metal electrodes to form van der Waals (vdW) contacts with 2D materials has been exploited yet, controlling the polarity of 2D transistors is still a major challenge. Here, we report a solvent-free electrode transfer strategy that allows vdW integration of 3D metal electrodes with auxiliary layer and 2D semiconductors. By changing the auxiliary layer, the polarity regulation of monolayer and few-layer WSe₂ FETs is realized. A robust and optimized pure n-type transistor is developed by adding the electron injection layer as an auxiliary layer for the Ag electrode. Pure p-type transistor with optimized performance is achieved by the hole injection layer as an auxiliary layer. Benefiting from the vdW integration strategy of functionalized electrodes, a metal-semiconductor-metal diode with a rectification ratio of 10³ and a logic inverter with a voltage gain of 1.73 at a bias voltage of 5 V are realized, demonstrating the potential for applications in logic circuits.

7.1 Introduction

Two-dimensional transition-metal dichalcogenides (TMDs) have emerged as next-generation semiconducting materials for future electronics, due to their ultrathin bodies, dangling-bond-free surface and in-plane ultrafast electronic transport characteristics for transistors.^[1-5] While high quality TMDs large-area wafer-level synthesis has been produced by chemical vapor deposition (CVD)^[6; 7] to date, TMDs based transistors still face many challenges when exploited to realize complementary metal oxide semiconductor

(CMOS) logic circuits (LCs) applications^[8; 9]. The most critical challenge is to control the device polarity (both p- and n-type) in the same semiconductor and achieve high-quality contacts with electrodes, as is done with silicon-based semiconductors through doping, which is essential for low power consumption and high-performance complementary LCs^[10]. However, TMDs such as molybdenum disulfide (MoS_2), tungsten diselenide (WSe_2) and others, are intrinsically incompatible with conventionally substitutional doping in silicon-based CMOS field-effect transistors (FETs), making it impossible to regulate device polarity through ion implantation processes^[11]. In addition, unlike the robustness of silicon-based semiconductors, conventional lithography and deposition of electrodes (both metal and other materials) also cause interfacial defects and metal-induced gap states (MIGS) in TMD crystals^[12; 13], resulting in Fermi-level pinning (FLP) near the conduction band^[14], which in turn limits the intrinsic properties of TMDs, and once again hinders the development of TMDs toward integrated circuits.

Current implementations of TMD-based LCs mainly rely on two different TMD semiconductors^[15-17], which involve semiconductor variability, different processing and preparation conditions and stability, etc., and are not compatible with CMOS technology. This is because, in general, most TMD-based FETs prepared by the lithography process are NMOS due to FLP^[14], regardless of the kind of metal electrode, so TMD-based NMOS are very mature. However, there are few pure p-type 2D semiconductors, and only black phosphorus (BP)^[18; 19], 2D tellurium^[20; 21], $\alpha\text{-MnS}$ ^[22], etc. have been reported so far, but harsh preparation or use conditions limit their applications^[23]. Therefore, PMOS is usually realized by doping semiconductors or using high work function (WF) metals as electrodes to facilitate hole injection^[24-27]. It has been reported that even MoS_2 with deep valence band energy level can achieve p-type transport by choosing suitable dopants^[28; 29]. However, due to structural limitations, the doping of TMDs is non-noumenon doping and usually has poor stability^[23]. Although PMOS can be achieved on ambipolar TMDs (e.g., WSe_2 and MoTe_2) by depositing high WF metals (e.g., Pt in 5.6 eV, Pd in 5.2 eV, etc.) the MIGS induced during deposition and the resulting FLP are still difficult to avoid, which also limit the device lifetime and increase the energy consumption^[24; 30].

Recent work has shown that van der Waals (vdW) contact between electrodes and TMDs can provide a near-perfect interface that can fundamentally eliminate MIGS and FLP from interface, and thus allowing TMDs to exhibit a more intrinsic performance.^[12; 13; 31-34] For example, high performance NMOS with ultra-low contact resistance and Schottky barrier can be prepared by vdW contact of low WF electrodes with TMD.^[12; 35; 36] In addition, ambipolar and pure P-type devices can also be realized by contacting high WF electrodes with the vdW of the TMD.^[12; 13; 33] PMOS with Pt and Pd 3D-metal-based vdW contact has also been reported using standard electron beam evaporation process.^[33] Nonetheless, in the direct lithography process, the contamination and damage of TMD may still be unavoidable.^[37] Recently, a doping-free strategy to modulate the polarity of WSe₂ transistors using the same contact metal but a different integration method has attracted attention.^[10] WSe₂ FETs with evaporated gold contacts exhibit n-type characteristics due to FLP. In contrast, the device with low-energy vdW integrated transfer gold electrodes exhibit p-type transport behavior. This provides opportunities for the implementation of high performance doping free LCs. But it depends on the thickness of WSe₂, where NMOS performance is limited at thinner WSe₂. Therefore, the implementation of LCs based on the same semiconductor still remains challenge.

Our previous work described in Chapter 6 demonstrated that pre-functionalization of vdW contact electrodes in TMD-based FETs can achieve modulation of device performance.^[38] However, typical transfer and integration of vdW electrodes reported so far involves the use of polymer stamps and thermal release tapes to peel and laminate metal electrodes. During this process, wrinkles or bubbles may form, which not only damages the reliability of the process but also poses serious challenges to the alignment between the TMD and the electrodes.^[34] In addition, the direct contact of the polymer with the TMD channel can also cause potential contamination, resulting in unintentional doping, defects, strains and degradation of TMD surface quality.^[31] Moreover, the use of a lithography process to fabricate electrodes on a sacrificial substrate or directly on a TMD crystal requires multiple exposures to chemical solvents and resists. This is not only prone to contaminant residues,

but also prevents pre-functionalization of electrodes, especially using organic molecules with vdW contact, because the acetone necessary in the process will dissolve the organic molecules, resulting in functional failure.

Here, we report a solvent-free integration strategy for functionalized 3D-metal electrodes and 2D-TMD semiconductors with vdW contacts, where the directly deposited functionalized electrodes with auxiliary layers are picked up and laminated directly onto TMD surface. The whole process does not require lithography, does not use polymer stamps, does not involve any solvents, and it avoids all possible sources of pollution. Short-channel FET with a channel length of 110 nm is prepared, and the channel length at the narrowest part of the device is only 7 nm, being the narrowest channel FETs prepared without lithography. The polarity of WSe₂ FETs can be regulated by modifying the auxiliary layer. Pure electron (NMOS) or pure hole (PMOS) injection of WSe₂ semiconductors is achieved using an electron injection layer (EIL) or a hole injection layer (HIL) as an auxiliary layer, respectively. Benefiting from the excellent electrode integration strategy, metal-semiconductor-metal (MSM) diode with a rectification ratio of 10³ is fabricated by transferring electrodes functionalized with different auxiliary layers onto the same WSe₂. A logic inverter is demonstrated based on WSe₂ NMOS and PMOS with polarity control capability with different auxiliary layers.

7.2 Experimental methods

7.2.1 Materials and instrumentation

Materials: Bulk MoS₂ crystals were purchased from SPI Supplies. Triangular monolayer CVD WSe₂ crystals on sapphire substrate were purchased from Six Carbon Technology (China). MoO₃ and 8-Hydroxyquinolinolato-lithium (Liq) were purchased from Ossila.

AFM Measurement: Tapping mode Atomic Force Microscopy (AFM) imaging was performed by using a Bruker Dimension Icon set-up operating in air. The tip model is TESPA-V2, and the tip stiffness K is 42 N m⁻¹.

Electrical Measurement: The FETs devices were electrically characterized by a Keithley

dual channel 2636A sourcemeter in a three-terminal configuration with the back gate contacted through an underlying metal plate in a glovebox filled with nitrogen in dark conditions. Schottky diodes are tested with the same instrument as FETs. Logic inverter is tested in a cryogenic probe station (Janis-CCR5-2) using a semiconductor parameter analyzer (Keithley 4200) with a vacuum degree of about 5×10^{-5} mbar.

7.2.2 Devices fabrication

7.2.2.1 Preparation of semiconductor

Chemical vapor deposition (CVD)-grown WSe₂ flakes transfer: Triangular monolayer WSe₂ crystals grown by chemical vapor deposition (CVD) on sapphire substrate were purchased from Six Carbon Technology (China). Initially, a polystyrene (PS) film (60 mg/mL, dissolved in toluene) was spin-coated onto the sapphire substrate containing CVD flakes. The PS film was then peeled off from the sapphire with the aid of a tweezer on the water surface, with the CVD flakes adhering to it. Due to water's surface tension, the PS film with CVD flakes floated on the water surface. A pre-cleaned wafer was employed to fish the PS film from the wafer surface. Following transfer, the sample was vacuum dried, then baked at 60 °C for 20 min and 90 °C for 30 min. Subsequently, the sample was immersed in a 60 °C toluene solution overnight to remove the surface PS film. Finally, the sample was taken out and blown dry with a nitrogen gun.

7.2.2.2 Preparation of (auxiliary layer functionalized) electrodes

Electrode fabrication, functionalization, dry transferring and lamination process.

First, the SiO₂ surface was functionalized with octadecyltrichlorosilane (OTS) as a sacrificial substrate, making it hydrophobic and weakening the adhesion of subsequently thermally deposited materials to facilitate mechanical desorption and transfer. An auxiliary layer (5 nm Liq or MoO₃) was thermally deposited on the sacrificial substrate, followed by patterned metal electrodes deposited through a copper mask (G100/400-C3, Glider Grids) via thermal evaporation. For the Liq auxiliary layer, 90 nm Ag and 30 nm Au were

deposited, with Au serving as a protective layer to prevent Ag oxidation. For the MoO_3 auxiliary layer, 90 nm Au was deposited.

7.2.3.3 FETs devices with van der Waals (vdW) contact electrode fabrication

FETs devices with van der Waals (vdW) contact electrode were fabricated using a solvent-free direct dry transfer technique. During the transfer process, a mechanical probe with a gallium-indium alloy coated tip was used to pick up the metal electrode (functionalized with an auxiliary layer) from the sacrificial substrate. The stripped electrode was immediately transferred and physically laminated on the WSe_2 flake surface under the alignment of microscope lens. The same method was employed to transfer another electrode onto the WSe_2 flake surface, fabricating top-contact FETs. Lastly, the device was annealed at 120 °C overnight in a high-vacuum chamber.

For WSe_2 FET devices without auxiliary layer, the auxiliary layer deposition step was omitted during the fabrication process.

7.2.3.4 Metal–semiconductor–metal (MSM) diode fabrication

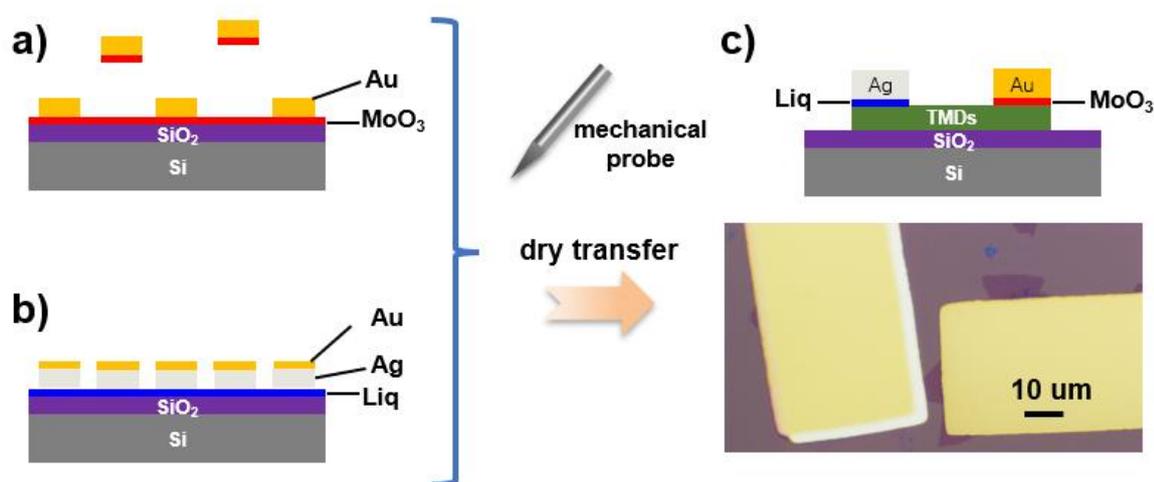


Figure 7.1 Fabrication process of WSe_2 MSM diode with different auxiliary layer functionalized electrodes using vdW integration processes.

The preparation processes for the metal–semiconductor–metal (MSM) diode devices with asymmetric electrodes were identical to the aforementioned steps. The schematic diagram of the process is shown in Figure 7.1. Two electrodes functionalized with different auxiliary

layers were selected and physically laminated onto a single WSe₂ flake surface under the alignment of microscope lens.

7.2.3.5 Logic inverter fabrication

The preparation processes for the logic inverter with PMOS and NMOS are identical to aforementioned steps, and the schematic diagram of the device and optical image are presented in Figure 7.2. When transferring the electrodes, control their direction and connect one electrode from the PMOS to one electrode of the NMOS.

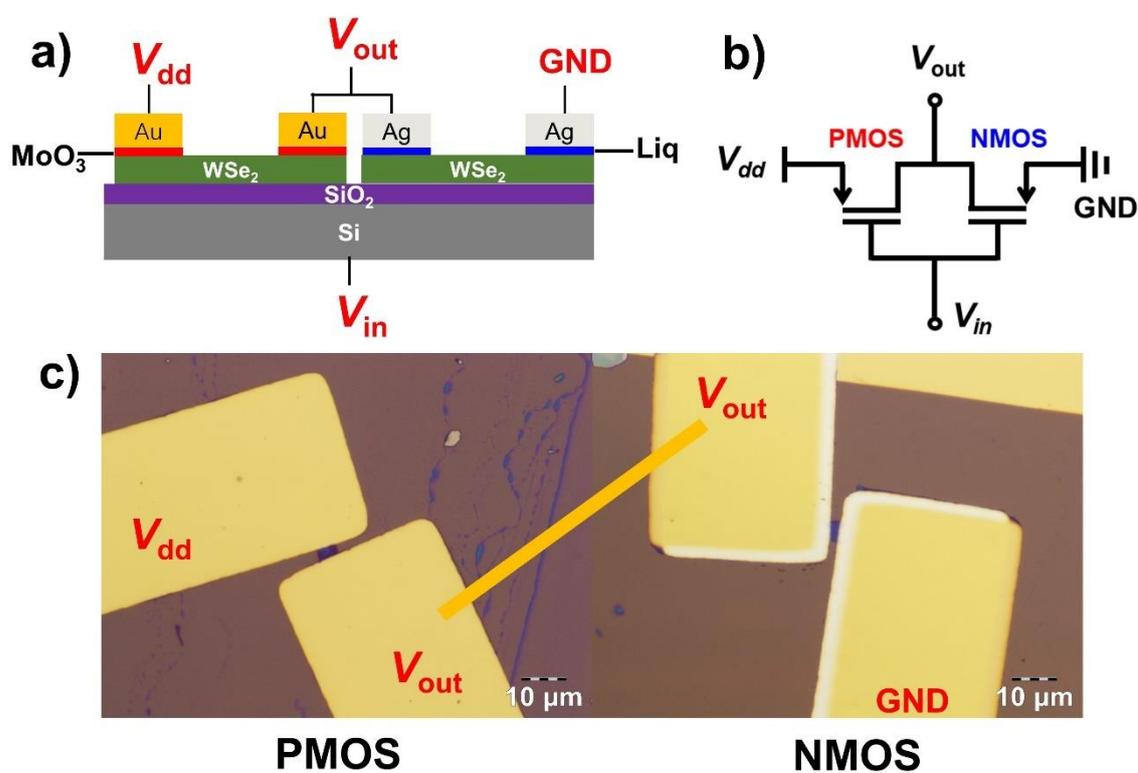


Figure 7.2 Schematic diagram and optical image of WSe₂-based logic inverter.

7.3 Results and discussions

The back-gate top-contact FETs were developed with transferred auxiliary layer functionalized electrodes employing vdW contact with WSe₂. Figure 7.3a–e schematically illustrates the device fabrication process. Briefly, a 5 nm auxiliary layer is first deposited on the sacrificial substrate, with the electron injection material 8-Hydroxyquinolinolato-

lithium (Liq) or hole injection material MoO_3 chosen as the auxiliary layer. Then, patterned metal electrodes (90 nm Au or 90 nm Ag with a 30 nm Au protective layer) are deposited onto the auxiliary layer surface through a mask. Subsequently, the functionalized electrodes are picked up by a mechanical probe under a microscope and physically laminated onto the WSe_2 surface via vdW interaction.^[38] The chemical vapor deposited (CVD) WSe_2 flakes are pre-transferred onto a highly doped silicon substrate covered with a 270 nm-thick SiO_2 layer as dielectrics. The results were also verified with exfoliated WSe_2 flakes. The device structure is displayed in Figure 7.3e. For WSe_2 FET devices without electrode functionalization, the auxiliary layer deposition step in Figure 7.3b was omitted during the fabrication process. Direct metal deposition or auxiliary layer deposition on the WSe_2 surface, which was reported to damage the TMD surface and generate defects, was avoided. Our work establishes an atomically clear and clean metal-auxiliary layer/ WSe_2 interface.

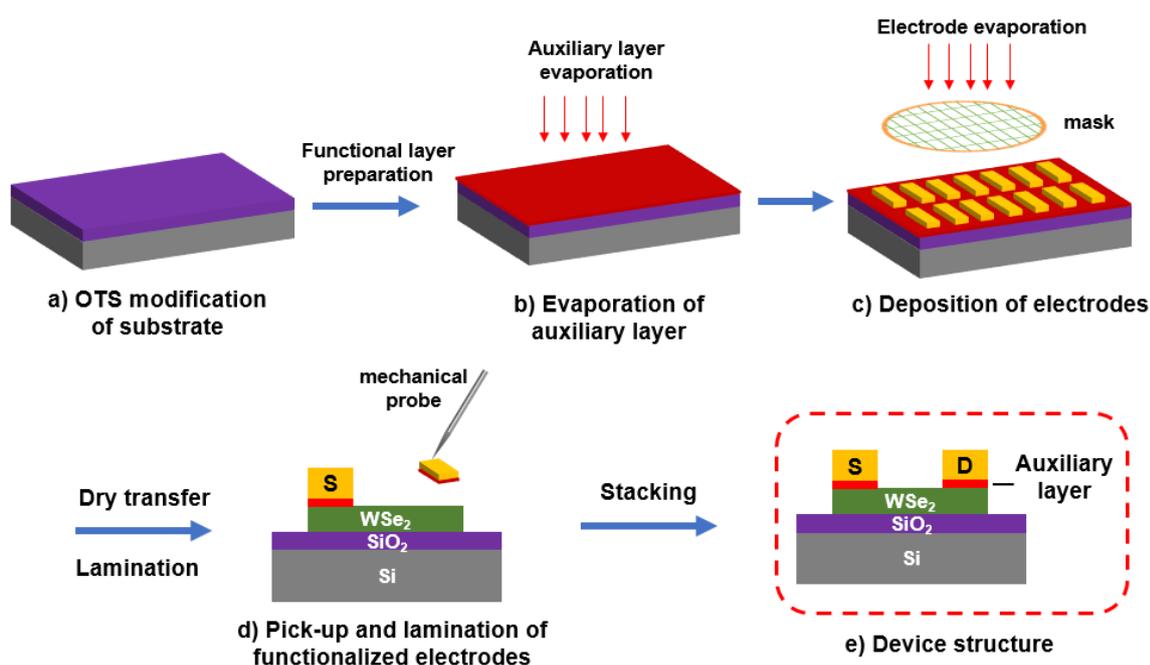


Fig 7.3 Fabrication process of WSe_2 FETs with auxiliary layer functionalized electrodes using vdW integration processes: Sacrificial Si/SiO_2 substrate modified with OTS (a). The auxiliary layer evaporated on the sacrificial substrate (b). Patterned metal electrodes evaporated on the auxiliary layer surface through a mask (c). The above prepared functionalized metal electrodes with auxiliary layer picked up with a mechanical probe physically laminated on WSe_2 surface with vdW

interaction (d). e Schematic of a FET device that auxiliary layer-functionalized electrodes vdW contact with WSe₂.

7.3.1 VdW contact FETs based on CVD-grown WSe₂ flakes

7.3.1.1 Characterization of CVD-grown WSe₂ flakes

Figure 7.4 a-b depict the topography of a CVD-grown WSe₂ crystal after being transferred onto a Si/SiO₂ substrate. A triangular-shaped crystal with a thickness of approximately 0.77 nm can be observed, indicating monolayer characteristics.^[39] The crystal surface roughness (R_{RMS}) on regions of $5 \times 5 \mu\text{m}^2$ is 0.64 nm. Raman and PL spectra exhibit typical properties of monolayer WSe₂ (Figure 7.4 c-d).

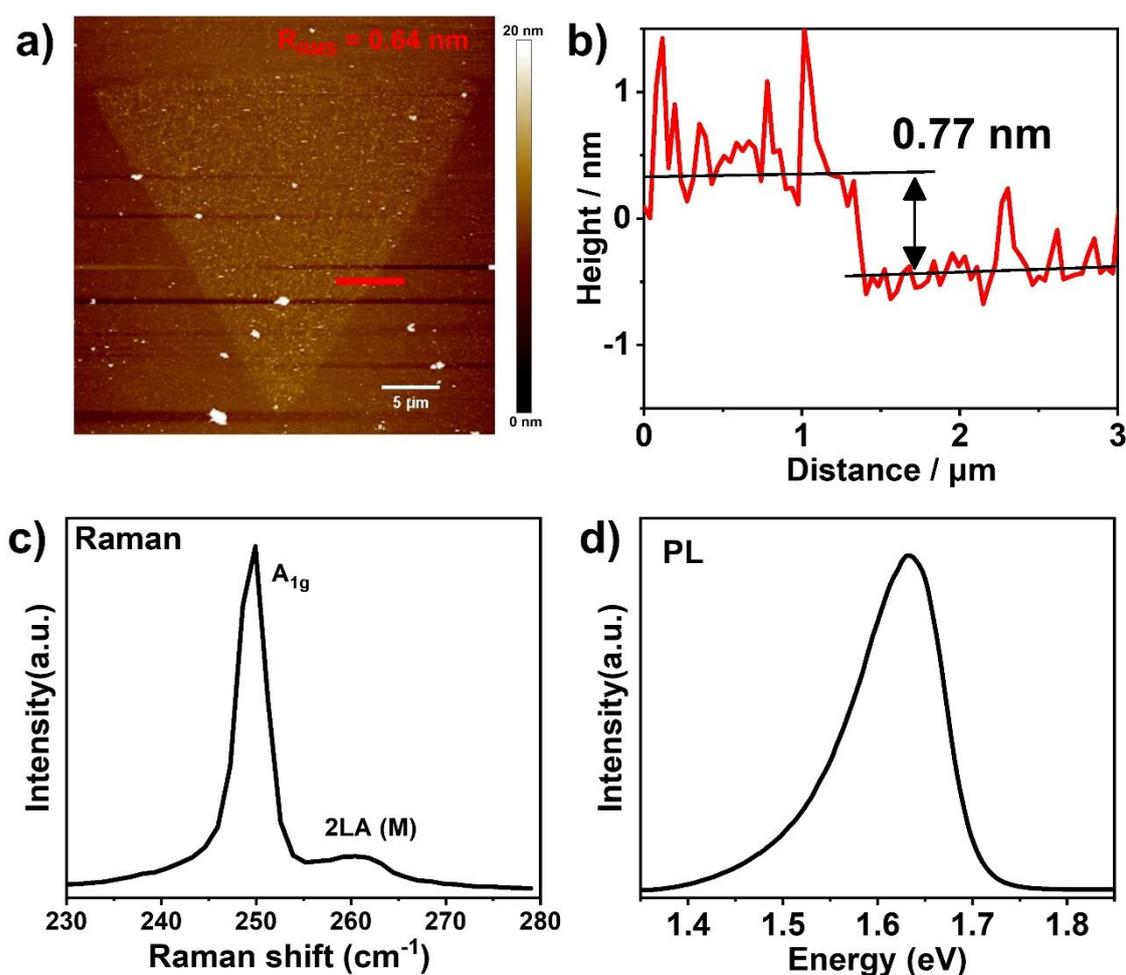


Figure 7.4 Morphology the thickness of CVD-grown WSe₂ flake. $R_{\text{RMS}} = 0.64 \text{ nm}$. The red height curve in (b) shows thickness along the red short line in (a). Raman (c) and PL (d) spectra of CVD-

grown WSe₂ flake on AlO₃ substrate, measured at room temperature in ambient.

7.3.1.2 *VdW contact FETs with Au electrode*

In comparison to methods such as PDMS-stamp with prefabricated electrodes on its surface, our work utilizes a solvent-free dry transfer method to laminate the bottom surface of the electrode onto the semiconductor surface. This method benefits from the atomically flat surface of the silicon wafer, and the bottom surface of the electrode also exhibits comparable flatness. Figure 7.5 presents the AFM topography images of the top and bottom surfaces of a thermally deposited gold electrode. The comparison reveals that the roughness of the electrode's bottom surface is 0.32 nm, while that of the top surface is 8.96 nm. This indicates that the bottom surface will provide better contact with WSe₂, generating minimized interface defects.

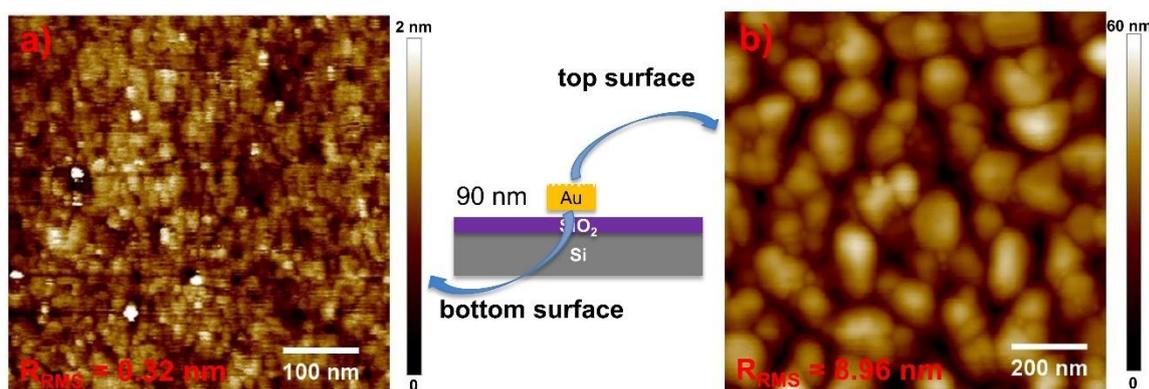


Figure 7.5 Morphology comparison of bottom and top surfaces of evaporated Au electrode. The bottom surface roughness is 0.32 nm. The top surface roughness is 8.96 nm.

Figure 7.6a-c presents the architecture of the FETs device vdW contact to the Au electrode, the energy band diagram, and the device image. Figure 7.6d-f displays the typical transfer and output curves of devices. Since the WF of gold is close to the valence band (VB) of WSe₂ and without FLP, the hole injection barrier (SBH_h) in the device is substantially lower than the electron injection barrier (SBH_e), resulting in hole-dominated transport characteristics. The hole mobility at 1 V bias is 5.8 cm² V⁻¹ s⁻¹ and the I_{on}/I_{off} ratio is approximately 10⁷. The output curves demonstrate the ohmic contact behavior between WSe₂ and the Au electrode.

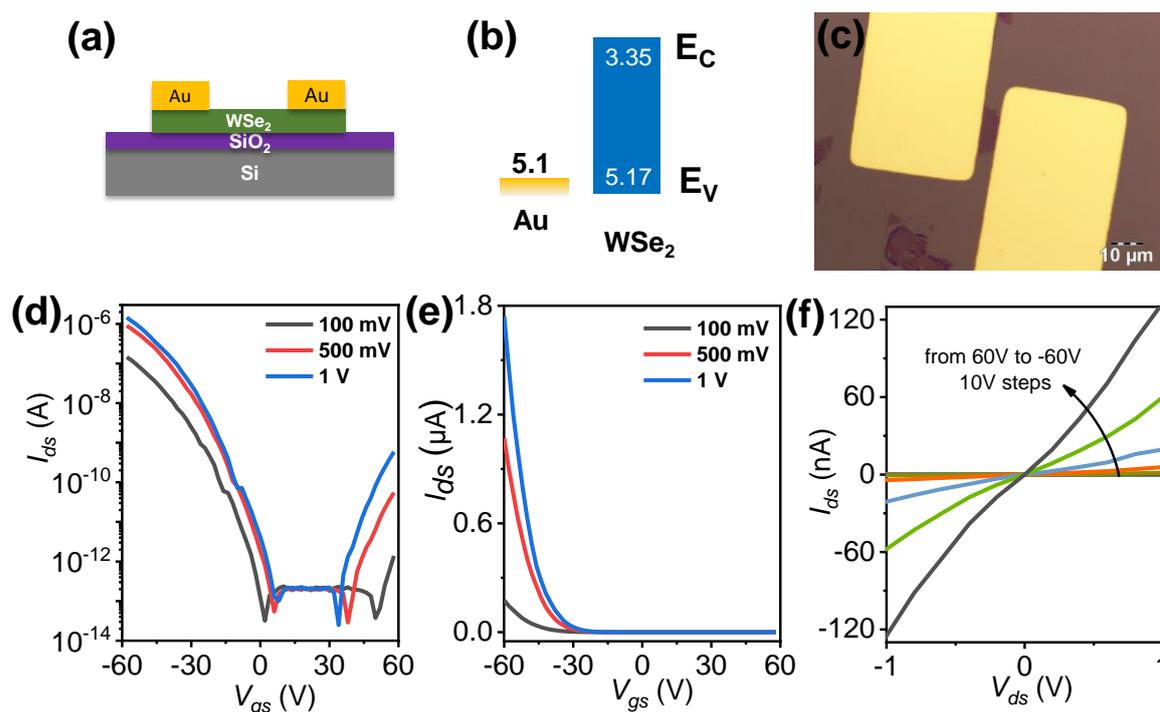


Figure 7.6 (a) Device schematic diagram of the device with Au vdW contact. (b) Energy band diagram of the device. (c) Optical picture of the device. (d-f) Logarithmic and linear transfer curves and output properties of the device.

7.3.1.3 VdW contact short-channel FETs with Au electrode

It is worth noting that this technique can be employed to prepare FETs devices with arbitrary channel length. To explore the minimum resolution of this strategy, short-channel FETs with nanoscale channel lengths were fabricated. Limited by the wavelength range of visible light, the optical microscope cannot discern channel length shorter than 200 nm (half the shortest wavelength of visible light).

Figure 7.7 displays the scanning electron microscope (SEM) images and electrical curves of WSe₂ FETs prepared using this method, with average channel lengths of 110 nm and 250 nm, respectively. It is evident that when the device length is scaled down to hundreds of nanometers, WSe₂ still exhibits FET properties, but the electron transport gradually increases. This may be attributed to the short distance between the source and drain electrodes, which amplifies the electron transport signal, especially when the channel length reaches 110 nm. It is important to note that due to the edge roughness of the

electrodes, the shortest channel position of the FETs in Figure 7.7a is 7 nm, and further shortening of the channel length would result in a short circuit within the device. This represents the narrowest channel length of FETs fabricated without lithography ever reported so far, and this value could be further improved by optimizing the edge roughness of the electrodes.

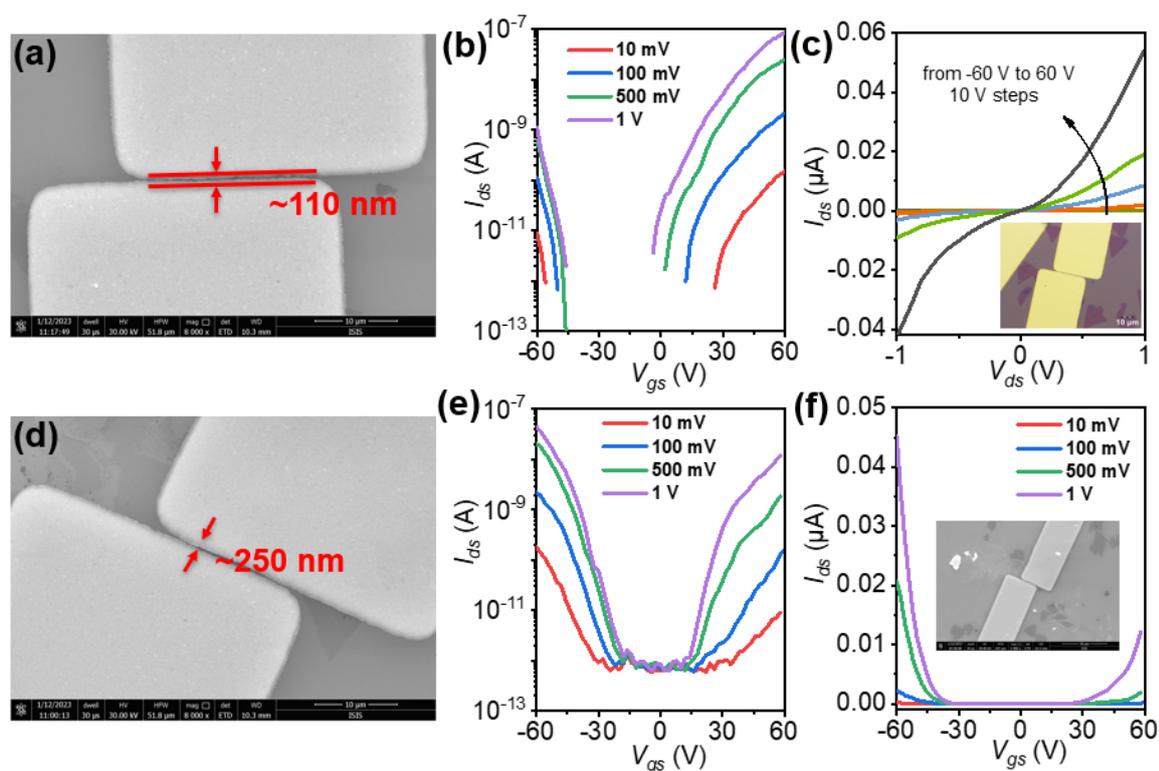


Figure 7.7 WSe₂ short-channel FETs devices in vdW contact with Au electrodes. (a-c) SEM image and transfer and output curves of WSe₂ FETs with a channel length of 110 nm. The inset in c is the optical image of the device. (d-f) SEM image, logarithmic and linear transfer curves of WSe₂ FETs with a channel length of 250 nm. The inset in c is the global SEM picture of the device. The channel length of the device is the average value of 50 positions in the channel in the SEM picture.

7.3.1.4 VdW contact FETs with MoO₃ functionalized Au electrode

MoO₃ possesses a very high WF (>6 eV) and has been extensively utilized as a hole injection layer (HIL) in organic electronics.^[25; 40; 41] It has also been reported as a p-type dopant for doping the TMD interface.^[27; 42; 43] Here, a 5 nm MoO₃ interlayer was introduced underneath the Au electrode to tune the electrical properties of WSe₂. The vdW contact between MoO₃ and WSe₂ avoids direct thermal deposition, which would damage the

crystal^[43]. Figure 7.8 exhibits the AFM topography images of MoO₃ deposited below and above Au electrode. The comparison shows that the bottom surface roughness of MoO₃ deposited below Au electrode is 0.19 nm, while the top surface roughness of MoO₃ deposited above Au electrode is 4.96 nm. This again demonstrates the advantage of utilizing the bottom electrode interface.

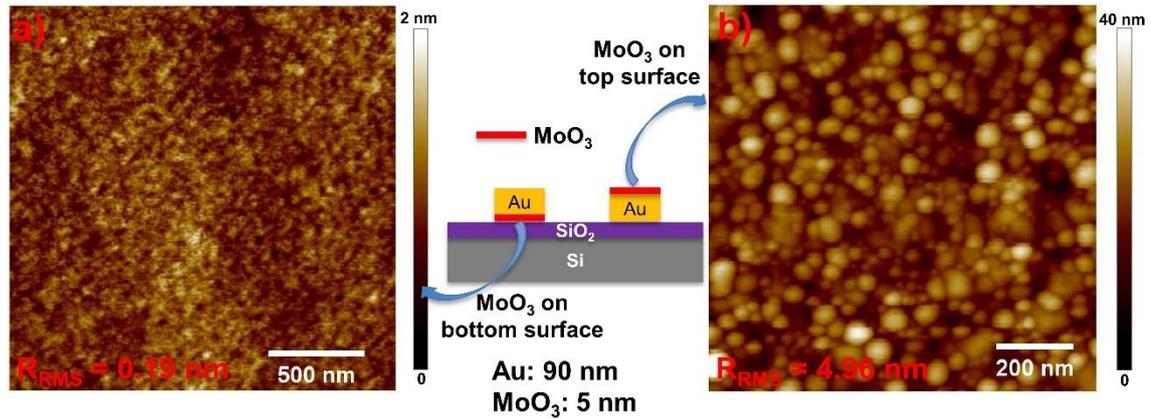


Figure 7.8 Morphology comparison of MoO₃ deposited below and above Au electrode. The bottom surface roughness of MoO₃ deposited below Au electrode is 0.19 nm. The top surface roughness of MoO₃ deposited above Au electrode is 4.96 nm.

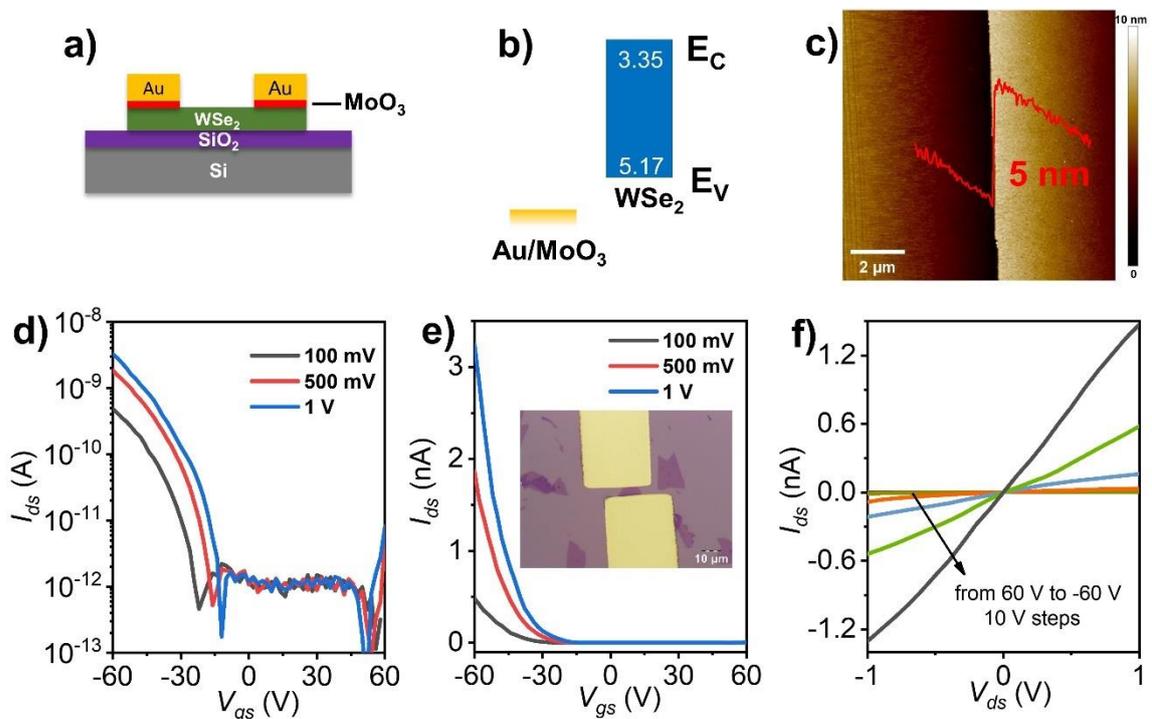


Figure 7.9 (a) Schematic diagram of WSe₂ device with Au/MoO₃ electrodes vdW contact. (b)

Energy band diagram of this device. (c) The height of the MoO₃ layer. (d, e) Logarithmic and linear transfer properties of the device. The illustration in e is the optical picture of the device. (f) Output curves of the device.

Figure 7.9 presents the schematic diagram, energy band diagram, and electrical characteristics of the electrodes functionalized with MoO₃ as the HIL in vdW contact with WSe₂. As evidenced by the electrical curves in Figure 7.9d-f, after introducing the MoO₃ HIL as an auxiliary layer between Au and WSe₂, the transfer properties exhibit a good hole-unipolar transport (PMOS), and the electron transport nearly completely vanishes. This can be explained by the high WF value (> 6 eV) of MoO₃, which lowers the SBH_h, facilitates hole injection from the electrode to WSe₂, and increases the SBH_e, enabling electron injection more difficult. The linear output curve indicates that there is a good ohmic contact behavior between the HIL-functionalized Au electrode and the WSe₂ semiconductor.

7.3.1.5 VdW contact FETs with Ag electrode

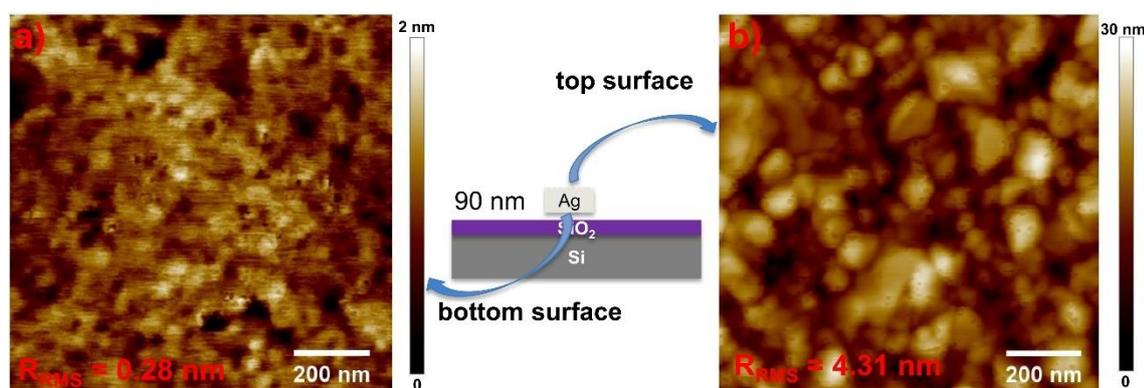


Figure 7.10 Morphology comparison of bottom and top surfaces of evaporated Ag electrode. The bottom surface roughness is 0.28 nm. The top surface roughness is 4.31 nm.

To achieve FLP-free N-type transport in FETs based on the WSe₂ semiconductor, a silver electrode was selected due to its well-known lower WF than gold, which facilitates the injection of electrons. Similarly, we also investigated the difference in roughness between the top and bottom surfaces of thermally deposited Ag electrodes (without a protective layer) on silicon wafer. Figure 7.10 displays the AFM morphologies of the top and bottom surfaces of the thermally deposited Ag electrode. The bottom surface of the electrode

exhibits atomic level flatness with a roughness of 0.28 nm, while the top surface roughness reaches 4.31 nm. This suggests that the bottom surface of Ag electrode can provide a super-flat vdW contact with the WSe₂ compared to the top surface, thereby eliminating the MIGS and FLP defects at the interface between the metal electrode and the semiconductor.

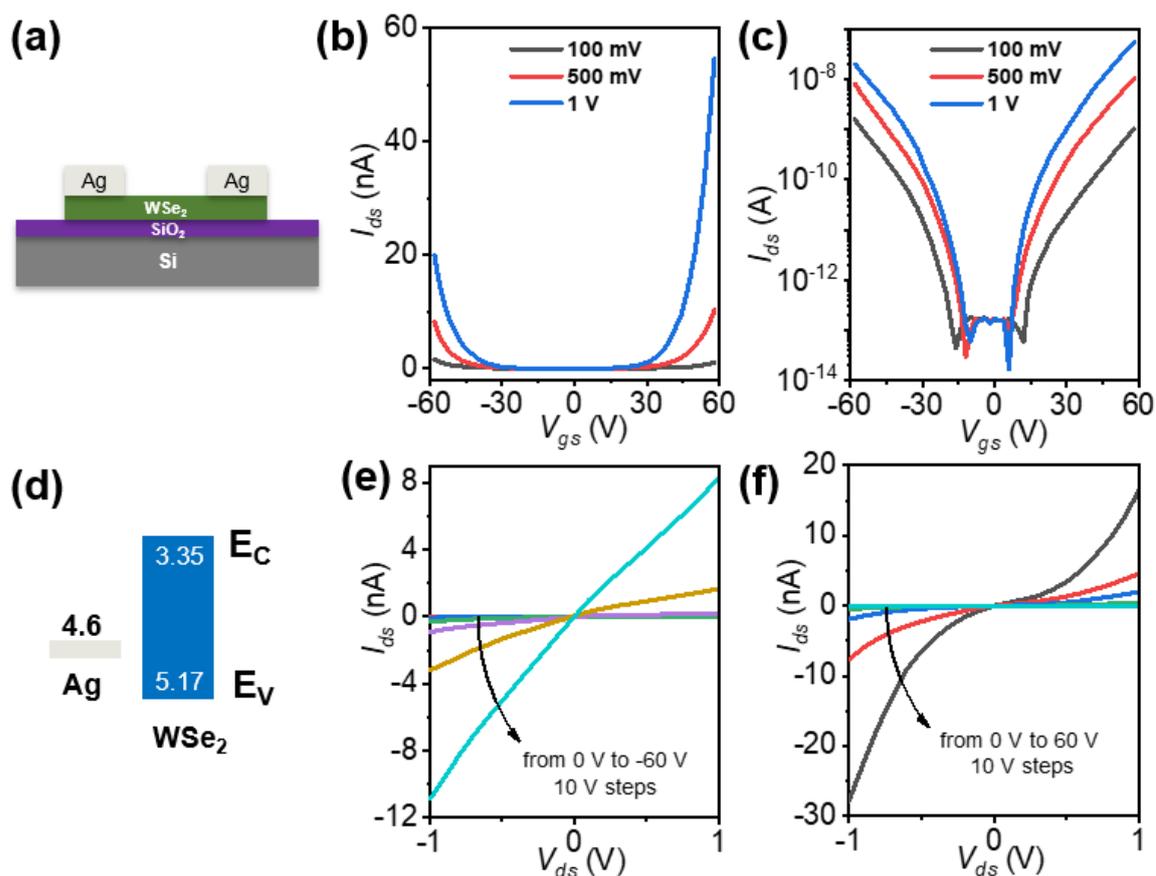


Figure 7.11 (a) Schematic diagram of WSe₂ FETs device vdW contact with single Ag. (b-c) Ambipolar logarithmic and linear transfer curves of the device. (d) Energy band diagram of Ag and monolayer WSe₂. (e-f) The output properties of the device at hole transport side and electron transport side.

Figure 7.11a presents the FET device with CVD-grown WSe₂ integrated with Ag electrodes via vdW forces. The transfer and output curves of the device are depicted in Figure 7.11b, c and e, f, respectively. A balanced hole and electron ambipolar transport behavior was observed, with the electron mobility of the device at 1 V being 0.17 cm² V⁻¹ s⁻¹ and hole mobility being 0.10 cm² V⁻¹ s⁻¹. The I_{on}/I_{off} ratios of both electron and hole sides exceeding 10⁵. This phenomenon can be attributed to the WF of Ag being positioned in the middle of

the CB and VB of monolayer WSe₂, figure 7.11d shows the energy band diagram of the device, revealing significant injection barriers for both electrons and holes, with the Schottky barrier height for electrons (SBH_e) being slightly larger than that for holes (SBH_h). Ambipolar transport in the WSe₂ FET demonstrates potential for polar modulation. The output properties of the device at hole transport side and electron transport side are illustrated in Figure 7.11e-f. It is evident that the device exhibits ohmic contact for hole transport, while the non-linear output curve indicates Schottky contact for electron transport, consistent with the energy band diagram.

7.3.1.6 VdW contact FETs with Liq functionalized Ag electrode

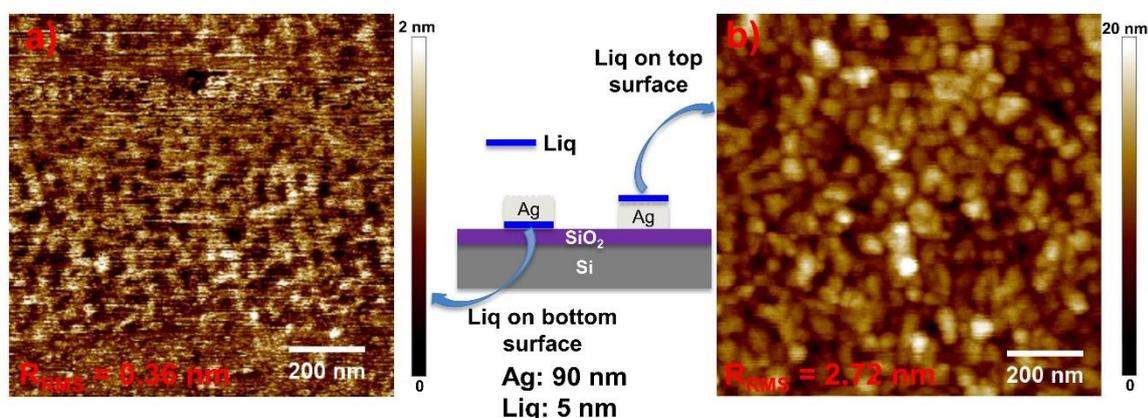


Figure 7.12 Morphology comparison of Liq deposited below and above Ag electrode. The bottom surface roughness of Liq deposited below Ag electrode is 0.36 nm. The top surface roughness of Liq deposited above Ag electrode is 2.72 nm.

8-Hydroxyquinolinolato-lithium (Liq), in conjunction with Ag or Al, is typically employed as an electron injection layer (EIL) material in organic electronic devices, particularly OLED^[44; 45]. In this study, to obtain a pure n-type FLP-free WSe₂ FET, a 5 nm Liq interlayer was introduced underneath the Ag electrode to tune the electrical properties of WSe₂. Figure 7.12 exhibits the AFM topography images of Liq deposited below and above Ag electrode. The comparison shows that the bottom surface roughness of Liq deposited below Ag electrode is 0.36 nm, comparable to the bottom surface roughness of pure Au, Ag metal electrodes, as well as MoO₃ functionalized Au electrodes, while the top surface roughness of Liq deposited above Ag electrode is 2.72 nm. This again shows that the bottom electrode

interface can provide a better contact effect with the WSe₂ interface.

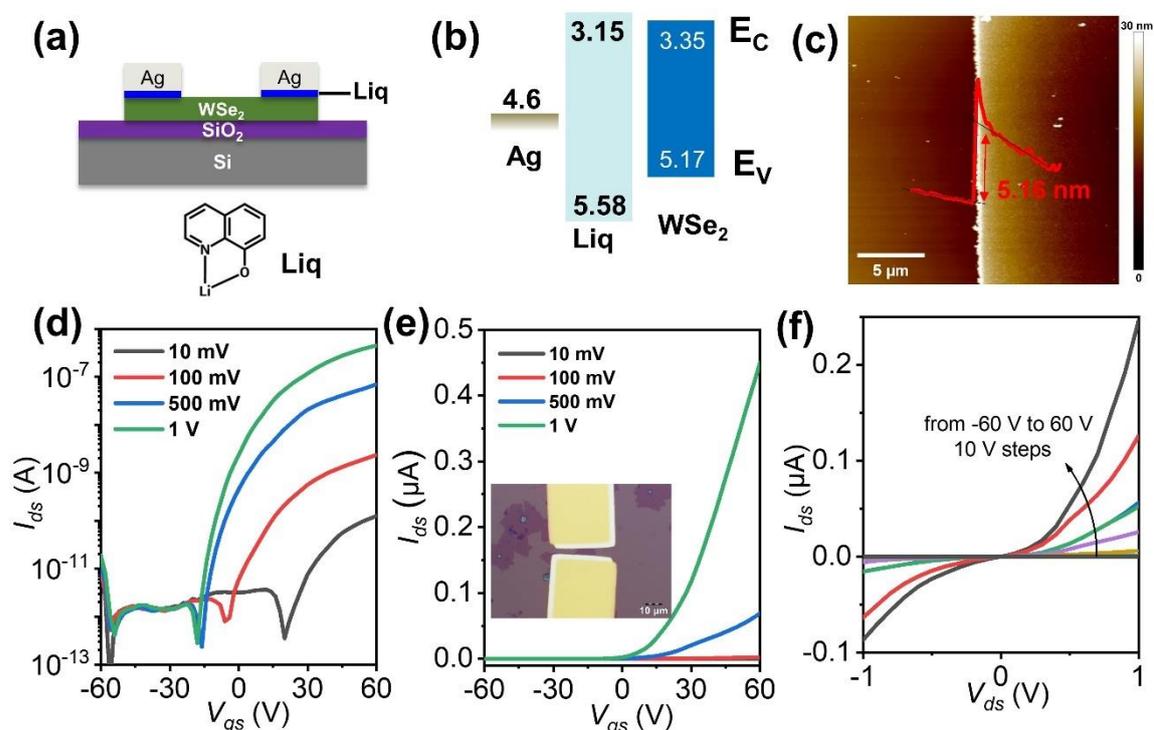


Figure 7.13 (a) Device schematic diagram of the device with Ag-Liq vdW contact and molecule structure of Liq. (b) Energy band diagram of this device. (c) The AFM measured height of the Liq layer. (d-f) Logarithmic and linear transfer and output properties of the device. The illustration in e is the optical picture of device.

The Liq layer coupled with an Ag electrode was physically laminated on the monolayer WSe₂ surface, as depicted in figure 7.13a and 7.13c. To protect Ag from oxidation, 30 nm Au was evaporated on top of Ag (see inset optical image in figure 7.13e). Figure 7.13d-f exhibit the typical transfer and output curves of FETs. The transfer curves (figure 7.13d-e) demonstrated an effective electron-unipolar transport (NMOS) with a mobility of 1.49 cm² V⁻¹ s⁻¹ and an I_{on}/I_{off} ratio exceeding 10⁵, while hole transport is nearly absent. The output curves indicate Schottky contact between the electrode and semiconductor. These results indicate that Liq, when employed as a charge injection layer between Ag and semiconductor, can effectively promote electron injection and suppress hole transport.

7.3.2 VdW contact FETs based on exfoliated few-layer WSe₂ flakes

In addition to CVD-grown monolayer WSe₂, we have also fabricated vdW contact devices on mechanically exfoliated few-layer WSe₂ to validate the findings.

7.3.2.1 VdW contact FETs with MoO₃ functionalized Au electrode

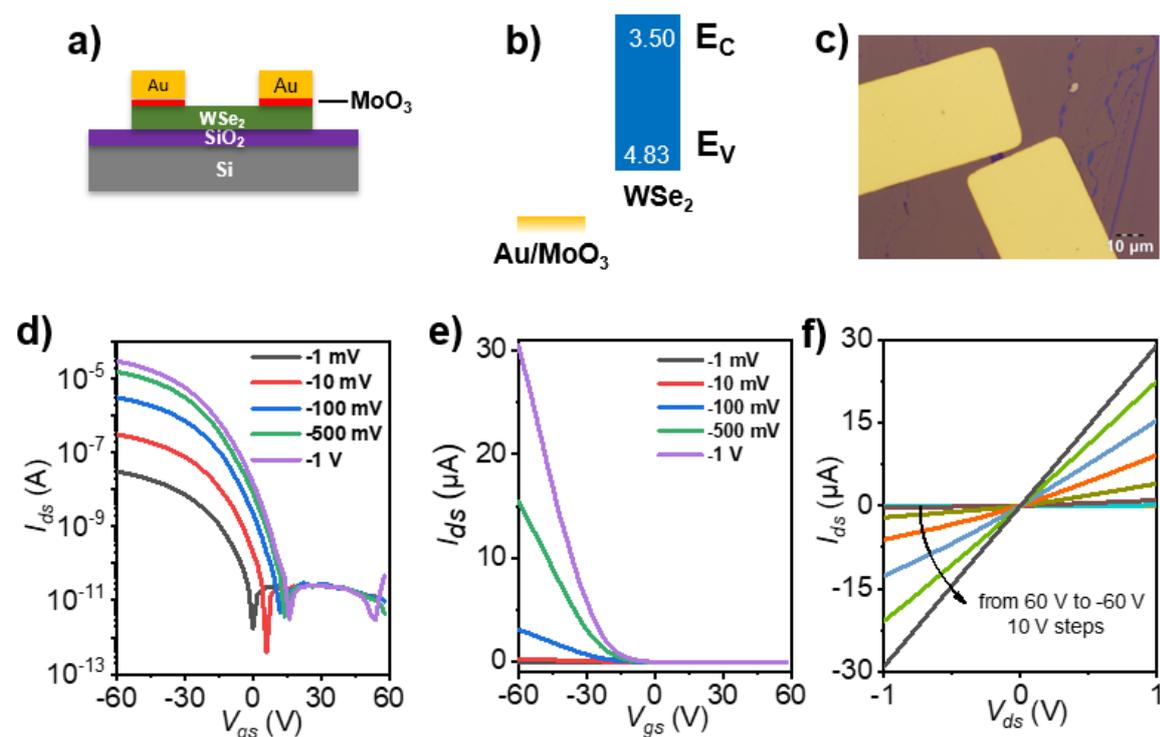


Figure 7.14 (a) Device schematic diagram of the device based on few-layered WSe₂ vdW contacts with Au-MoO₃ electrode. (b) Energy band diagram of this device. (c) The optical picture of the device. (d-f) Logarithmic and linear transfer and output properties of this device.

Figure 7.14 presents FETs with Au-MoO₃ vdW contacts on exfoliated few-layer WSe₂ flakes. The device exhibits high performance P-type characteristics (PMOS), with no electron transport branch present. A hole mobility of 45 cm² V⁻¹ s⁻¹ and an I_{on}/I_{off} ratio as high as 10⁷ were observed. Furthermore, the on-state current is nearly four orders of magnitude higher than that of monolayer WSe₂ FETs. This indicates that WSe₂ conductivity significantly increases with a higher number of layers. Figure 7.14f demonstrates the ohmic contact behavior between the MoO₃ functionalized Au electrode and the WSe₂ semiconductor, consistent with CVD-grown monolayer WSe₂ FET devices.

7.3.2.2 VdW contact FETs with Liq functionalized Ag electrode

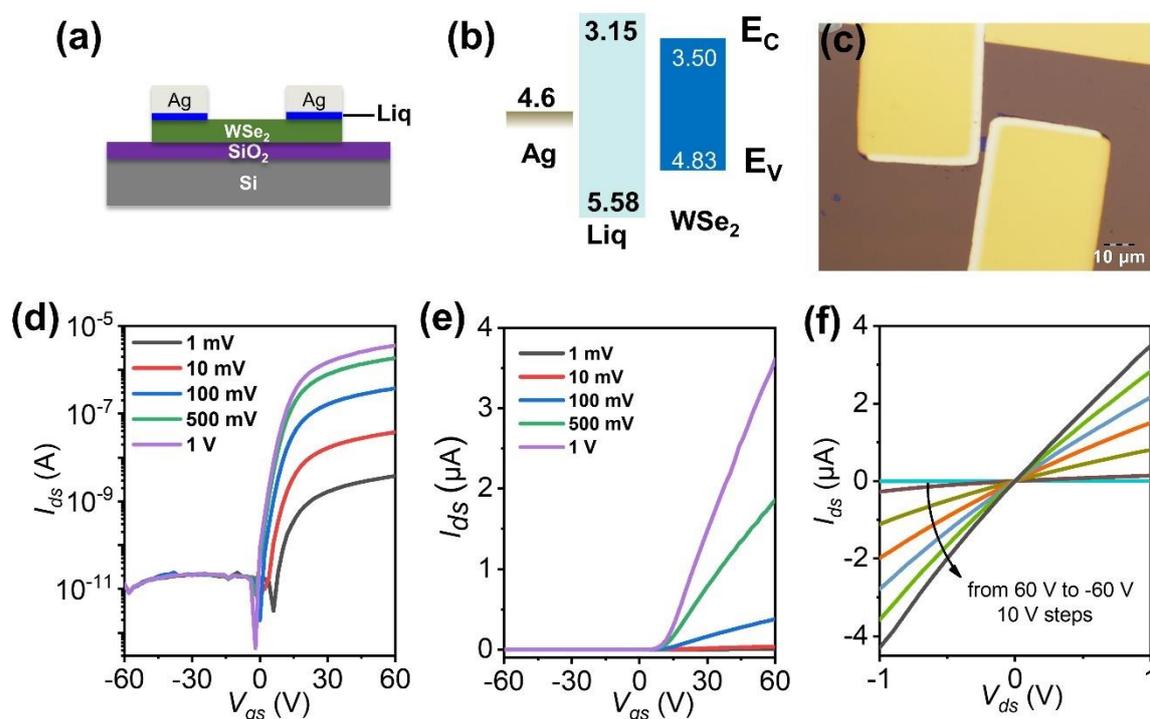


Figure 7.15 (a) Device schematic diagram of the device based on few-layered WSe₂ vdW contacts with Ag-Liq electrodes. (b) Energy band diagram of this device. (c) The height of the Liq layer. (d-f) Logarithmic and linear transfer and output properties of this device.

Similarly, as shown in Figure 7.15, after introducing a 5 nm EIL Liq between the Ag electrode and the exfoliated few-layer WSe₂ semiconductor, the electrical transport curve of the FET device exhibits unipolar N-type electron transport behavior (NMOS) without the presence of hole transport (Figure 7.15d and e). An electron mobility of $3.37 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and an $I_{\text{on}}/I_{\text{off}}$ ratio as high as 10^6 can be observed. The device performance is significantly better than that of monolayer WSe₂ FETs. The output curves indicate a good ohmic contact between the electrodes and the semiconductor, which is also consistent with CVD-grown monolayer WSe₂ FETs.

7.3.3 Metal–semiconductor–metal (MSM) diodes

By further advancing this strategy, the metal–semiconductor–metal (MSM) diodes can be fabricated by transferring various auxiliary layer functionalized electrodes onto a single CVD-grown WSe₂ flake with vdW contact. This is difficult to achieve using conventional

lithographic processes, and the transfer of organic layer-functionalized electrodes is also incompatible with all previously reported vdW transfer strategies for electrodes. This highlights the unique advantage of our solvent-free dry transfer method.

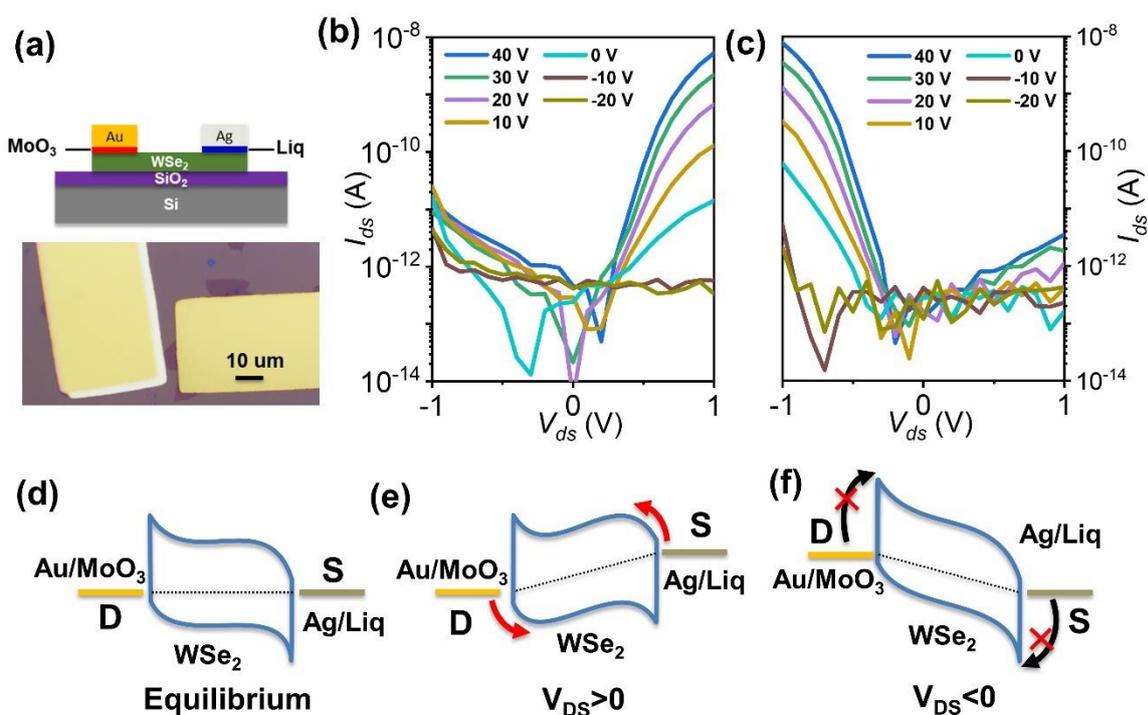


Figure 7.16 (a) Schematic and optical image of metal-semiconductor-metal (MSM) diode. (b) Semilogarithmic plot of the I_{ds} - V_{ds} output curves from -20 to 40 V gate bias conditions. The Au-MoO₃ electrode is biased and the Ag-Liq electrode is grounded. (c) Semilogarithmic plot of the I_{ds} - V_{ds} output curves of device with reversed source and drain electrode. (d-e) The energy band diagrams of MSM diodes at equilibrium (d), positive biased (e) and negative biased (f) conditions.

Figure 7.16a depicts the schematic and optical image of the MSM diode, where WSe₂ has vdW contacts with Liq-functionalized Ag electrode and MoO₃-functionalized Au electrode. For the asymmetric Au-MoO₃ and Ag-Liq contacts, the device exhibits a distinct rectification behavior (Figure 7.16b-c) with a rectification ratio (RR) of approximately 10³. This is comparable to diodes fabricated using asymmetric metal or oxidized metal and SAMs functionalized metal contacts.^[46-48] The rectification behavior of the diode stems from the difference in Schottky barrier between the two electrodes and WSe₂ at equilibrium (Figure 7.16d). Specifically, when the Au-MoO₃ electrode is biased and the Ag-Liq electrode is grounded, a positive bias is applied allows smooth carrier injection from the

electrode into WSe₂ semiconductor due to the small SBH (Figure 7.16e), resulting in a relatively large current. Conversely, a negative bias prevents carrier injection due to a larger SBH, maintaining the device in the off-state (Figure 7.16f). In contrast, when the Ag-Liq electrode is biased and Au-MoO₃ is grounded, carriers can only be injected into WSe₂ under negative bias due to the large SBH under a positive bias, resulting in a reversed rectification behavior (Figure 7.16c).

7.3.4 Logic inverter circuits

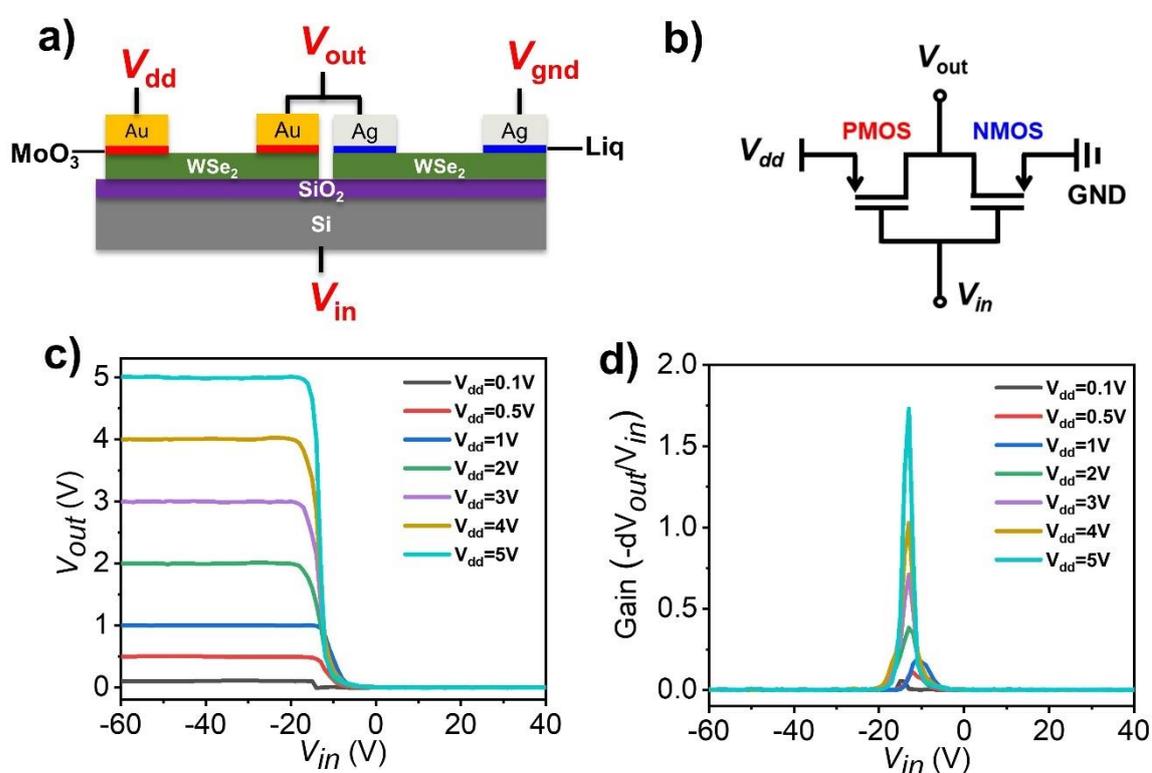


Figure 7.17 (a) The inverter diagram is composed of NMOS and PMOS WSe₂ FET devices. (b) Circuit diagram of the inverter. (c) The voltage transfer characteristics of the inverter as a function of the input voltage with different V_{dd} from 0.1 V to 5 V. (d) The corresponding voltage gains of the resulting inverter.

The transfer of the auxiliary layer functionalized electrodes enables the preparation of high-performance NMOS and PMOS devices, facilitating the polarity regulation of WSe₂ FETs, their easy integration into logic circuits. Employing this strategy, for example, one can prepare complementary logic inverters by connecting NMOS and PMOS in series. In this

study, we fabricated logic inverters based on WSe₂ NMOS and PMOS by employing the dry transfer of auxiliary layer functionalized electrodes, as shown in Figure 7.17a. Since the device polarity is regulated by the HIL and EIL, the logic inverter exhibits robust inverter behavior. Figure 7.17c displays the voltage transfer characteristics of the logic inverter as a function of input voltage, V_{dd} ranging from 0.1 to 5 V. The corresponding voltage gain of the logic inverter is illustrated in Figure 7.17d, with a maximum gain of 1.73 achieved at an input voltage of 5 V. The gain value is limited by the excessively thick dielectric layer of the FETs. Both the inverter input voltage and voltage gain can be improved by reducing the oxide thickness. This research provides valuable insights into the fabrication of high-performance complementary logic inverters based on WSe₂ and demonstrates the potential for further optimization and integration in advanced electronic applications.

7.4 Conclusions

In summary, we have reported a solvent-free dry transfer strategy and demonstrated that the polarity regulation of WSe₂ FETs can be achieved by transferring an auxiliary layer-functionalized electrode. When the electron injection layer Liq was employed as the auxiliary layer of the Ag electrode, high-performance, pure N-type FETs were achieved. Similarly, when the hole injection layer MoO₃ was utilized as the auxiliary layer of the Au electrode, high-performance, pure P-type FETs were realized. This polarity regulation is applicable to both CVD-grown monolayer WSe₂ and mechanically exfoliated few-layer WSe₂. Furthermore, we harnessed this approach to enable the asymmetric functionalization of source and drain electrodes, resulting in the fabrication of high-performance MSM diodes. By making use of these strategies, we could fabricate complicated integrated circuits. Specifically, by exploiting WSe₂ NMOS and PMOS devices, a logic inverter was prepared. The highest gain of the inverter was 1.73 at an input voltage of 5 V. Our work not only presents a viable approach for tailoring the performance of 2D materials on demand but also paves the way for utilizing 2D material semiconductors in the manufacture of integrated circuits. This strategy can be extended to other solvent-sensitive semiconductor

materials, such as unstable TMDs and organic semiconductors, further expanding its potential applications.

7.5 References

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Chapter 8 Conclusion and Outlooks

Owing to their tunable bandgap, high mobility, high $I_{\text{on}}/I_{\text{off}}$ ratio, and larger surface-to-volume ratio, TMDs have emerged as ideal components for next-generation high-performance electronic devices, garnering massive attention in the development of high-performance field-effect transistors. In this thesis, we combine the molecular approach with TMDs, by using principles of molecular functionalization, to control fundamental physical processes in 2D field-effect transistor (FET) devices and improve their performance. Device functionalization encompasses the functionalization of TMDs semiconductor and the functionalization of electrodes: Through semiconductor functionalization, a new capability of TMDs-based FETs toward isomers discrimination is developed. Electrode functionalization enables tuning and polarity regulation of TMDs-based FETs, showcasing their potential applicability in integrated circuits.

1. Functionalization of TMDs for isomers discrimination.

Leveraging defect engineering strategies, S defects are initially introduced into mechanically exfoliated monolayers MoS_2 through high temperature treatment. Subsequently, isomer molecules are covalently grafted onto the basal plane of the monolayer MoS_2 surface via a molecular functionalization approach. Benefiting from the high sensitivity of monolayer TMDs to diverse environments, the functionalized MoS_2 exhibits discernible changes. We characterized the morphology, elemental composition, Raman spectra, photoluminescence and FET electrical signals of monolayer MoS_2 prior to and following defect creation, as well as before and after isomer functionalization. The discrimination ability of MoS_2 stems from differences in isomer dipoles. Upon varying the dipole orientations, electron or hole doping in MoS_2 is induced, resulting in carrier concentration changes within the channel up to 10^{12} , thus enabling efficient isomer discrimination.

2. Self-assembly functionalization of the top-contact electrodes for asymmetric carrier injection in FETs

We devised a novel contact engineering approach to functionalize gold electrodes in top-contact field-effect transistors (FETs) by transferring SAMs pre-modified electrodes. The source and drain electrodes of MoS₂ FETs are functionalized by employing thiolated molecules with distinct dipole moments. Modifying Au electrodes with electron-donating molecules (DABT) led to a significant enhancement in device performance, while functionalization of electron-withdrawing molecules (PFBT) resulted in a notable decline in device performance. Moreover, high-performance Schottky diodes with a rectification ratio of approximately 10³ were fabricated using asymmetrically functionalized electrodes and dipolar opposing molecules on both electrodes. Our innovative strategy for tuning charge injection and extraction in top-contact MoS₂ FETs is broadly applicable to the fabrication of high-performance optoelectronic devices based on 2D semiconductors, thereby enabling on-demand tailoring of device characteristics.

3. vdW integration of auxiliary layer functionalized electrodes with TMDs for polarity tuning of TMD-based FETs

We developed a vdW integration strategy utilizing auxiliary layer functionalized electrodes with TMDs to achieve the polarity regulation in WSe₂ FETs. By employing an electron injection layer as an auxiliary layer to functionalize the electrodes, the transition from ambipolar to purely N-type WSe₂ FETs is achieved. Similarly, the transition from ambipolar to purely P-type WSe₂ FETs is realized by using a hole injection layer as an auxiliary layer to functionalize the electrodes. Furthermore, short-channel FETs with an average channel length of 110 nm and the narrowest of 7 nm is fabricated, marking the minimum channel length reported thus far for FETs manufactured without lithography. Metal-semiconductor-metal diodes, with a rectification ratio exceeding 10³, are prepared by transferring electrodes functionalized with distinct auxiliary layers onto the same crystal. The rectification ability is comparable to that of diodes with asymmetric metal electrodes and SAMs asymmetric functionalized electrodes. As proof of concept, NMOS and PMOS are fabricated using electrodes functionalized with different auxiliary layers, and the application of logic inverter is demonstrated with a voltage gain of 1.73 at V_{DD} = 5 V. The potential of TMDs-based FETs for integrated circuits is showcased.

This thesis explores the new functions of TMDs through functionalization strategy, addressing the critical challenges of injection barrier optimization and charge transport, thus enhancing performance. It also solves the polarity regulation problem of TMDs-based FETs, laying the foundation for the advancement of high-performance devices and integrated circuits. Furthermore, our work provides a guideline for the development of new functionalities at semiconductor interfaces. Our approach of exploring new functions via molecular modifications of semiconductor interfaces can be further expanded by taking advantage of the diversity of molecules. For example, by employing sensory molecular functionalization one can use TMDs-based FET devices to detect humidity, pressure, gas, ions and even viruses with a high sensitivity and selectivity, opening the floor for applications in biosensing and biomedical diagnostics. The functionalization of semiconductors with photoresponsive molecules enables to enhance the responsiveness to different light wavelengths, which can be relevant for the development of novel photodetectors and memory devices.

Additionally, our work opens new pathways for the functionalization of interfaces between the metal electrodes and TMDs with vdW contact in FETs. We realized functionalization of this interface through pre-chemical functionalization (SAMs) and pre-physical functionalization (direct thermal evaporation) of electrodes. The solvent-free vdW integration strategy considerably expands the range of materials available for functionalization, indicating that the functionalization of this interface is no longer restricted to solvent-stabilized materials but virtually any solid material. In the future, the material of the functionalized layer can be further altered to enable performance regulation for all TMDs. For instance, 1) the addition of a ferromagnetic material layer may result in the realization of spin response in TMDs-based FETs. 2) incorporating a rectifying molecule layer could lead to unidirectional injection in FET devices, yielding a diode with high RR. 3) introducing a strong dopant layer may enable contact doping for FET devices, among other possibilities.

Nonetheless, certain limitations exist in this thesis. For example, besides the semiconductor-air and semiconductor-electrode interfaces reported in this thesis for

functionalization in TMD-based FETs, there are also semiconductor-dielectric layer interface and the interface between the edge of the TMDs and the metal electrode (edge contact configuration), all of which hold substantial potential for the functionalization of FETs.

Moreover, the functionalization of FET devices is not only restricted to a single interface, but also two or more interfaces can be simultaneously and independently selected for device functionalization to develop multifunctional responsiveness. For example, 1) dual-interfaces functionalization in TMDs-based FETs: within the same device, a photoresponsive molecular layer is used to functionalize the semiconductor interface and an injection layer is employed to functionalize the electrode-semiconductor interface. This allows phototuning while modulating the polarity of TMDs-based FETs, significantly broadening the device's modulation capabilities. 2) triple-interfaces functionalization in TMDs-based FETs: in the same device, a photoresponsive molecular layer is used to functionalize the dielectric layer, SAMs are employed to functionalize the electrode for controlling carrier injection effect, and sensing molecules are applied to functionalize the semiconductor interface. This enables the adjustment of device detection capabilities for humidity, pressure, gas, ions or viruses by altering the wavelength of the light source, all while accommodating different carrier injection effects, ultimately achieving multi-level response and modulation.

Furthermore, the fabrication of integrated circuits necessitates high-performance FETs as building blocks for logic circuits. The application of functionalized FETs in logic inverter has been reported, and these devices also demonstrate potential for the construction of more complex logic circuits, such as NAND or NOR. Additionally, the solvent-free vdW integration method we introduced for functionalized electrodes and TMDs is anticipated to extend from individual devices to large-scale integrated devices, potentially replacing conventional lithography. This approach is expected to enable the performance and polarity tuning of large-scale devices, ultimately facilitating the development of large-scale integrated circuits based on TMDs.

Statement of Work

All experiments and data analysis reported in this thesis were carried out by the author (Bin HAN), except for the following:

Chapter 5: The DFT calculation was carried out by Sai Manoj Gali under the supervision of Prof. David Beljonne (Université de Mons, Mons, Belgium).

Chapter 6: The FETs electrical measurement was performed in collaboration with Yuda Zhao. The contact resistance was calculated by Chun Ma. The patterned electrode was prepared by Xinzi Tian under the supervision of Prof. Wenping Hu (Tianjin University, Tianjin, China). The AFM study was performed by Can Wang. The XPS spectrum was performed by Ye Wang.

Chapter 7: The transfer of CVD-grown WSe₂ crystal was performed by Hanlin Wang. The SEM study was performed by Verónica Montes García.

All the images displayed in this thesis were designed by the author (Bin HAN), and all the original projects reported in this thesis were designed and developed by Bin HAN and Prof. Paolo Samorì.

List of Publications

1. **Bin Han**, Sai Manoj Gali, Shuting Dai, David Beljonne, Paolo Samorì*. Isomers Discrimination via Defect Engineering in Monolayer MoS₂. *Submitted*.
2. **Bin Han**, Hanlin Wang, Verónica Montes García, Paolo Samorì*. Solvent-Free van der Waals Integration of Functionalized Electrodes for Two-Dimensional Semiconductor Device Polarity Modulation. *In preparation*.
3. **Bin Han**, Yuda Zhao, Chun Ma, Can Wang, Xinzi Tian, Ye Wang, Wenping Hu, Paolo Samorì* Asymmetric chemical functionalization of top-contact electrodes: tuning the charge injection for high-performance MoS₂ field-effect transistors and Schottky diodes. *Adv. Mater.*, **2022**, *34*, 2109445. DOI: 10.1002/adma.202109445
4. Xinzi Tian, Jiarong Yao, Lijuan Zhang, **Bin Han**, Jianwei Shi, Jianwei Su, Jie Liu, Chunlei Li, Xinfeng Liu*, Tianyou Zhai, Lang Jiang, Fangxu Yang, Xiaotao Zhang, Ye Zou, Rongjin Li*, Wenping Hu. Few-layered organic single-crystalline heterojunctions for high-performance phototransistors. *Nano Research*, **2022**, *15*, 2667-2673. DOI: 10.1007/s12274-021-3730-3
5. Yifan Yao, Yusheng Chen, Kuidong Wang, Nicholas Turetta, Stefania Vitale, **Bin Han**, Hanlin Wang, Lei Zhang, Paolo Samorì* A robust vertical nanoscaffold for recyclable, paintable, and flexible light-emitting devices. *Sci. Adv.*, **2022**, *8*, eabn2225. DOI:10.1126/sciadv.abn2225
6. Can Wang, Rafael Furlan de Oliveira, Kaiyue Jiang, Yuda Zhao, Nicholas Turetta, Chun Ma, **Bin Han**, Haiming Zhang, Diana Tranca, Xiaodong Zhuang, Lifeng Chi, Artur Ciesielski*, Paolo Samorì* Boosting the electronic and catalytic properties of 2D semiconductors with supramolecular 2D hydrogen-bonded superlattices. *Nat. Commun.*, **2022**, *13*, 510. DOI: 10.1038/s41467-022-28116-y
7. Baili Li, Ziyang Wang, **Bin Han**, Xi Yu. Characterization methods and analytical techniques for nanogap junction. *Chapter 4 of the Book: Nanogap Electrodes*, T. Li (Ed.), **2021**, DOI: 10.1002/9783527659562.ch4
8. **Bin Han**, Yao Li, Xuan Ji, Xianneng Song, Shuaishuai Ding, Baili Li, Hira Khalid, Yaogang Zhang, Xiaona Xu, Lixian Tian, Huanli Dong, Xi Yu*, Wenping Hu* Systematic modulation of charge transport in molecular devices through facile control of molecule–electrode coupling using a double self-assembled monolayer nanowire junction. *J. Am. Chem. Soc.*, **2020**, *142*, 9708-9717. DOI: 10.1021/jacs.0c02215

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9. Xianneng Song, **Bin Han**, X. Yu*, W. Hu. The analysis of charge transport mechanism in molecular junctions based on current-voltage characteristics. *Chem. Phys.*, **2020**, 528, 110514. DOI: 10.1016/j.chemphys.2019.110514

List of Presentations

1. **Bin Han**, Yuda Zhao, Chun Ma, Can Wang, Xinzi Tian, Ye Wang, Wenping Hu, Paolo Samorì. *Chem2Dmat 2023*, Bologna, Italy, 15-18 May 2023. Oral presentation
2. **Bin Han**, Yuda Zhao, Chun Ma, Can Wang, Xinzi Tian, Ye Wang, Wenping Hu, Paolo Samorì. *2D Transition Metal Dichalcogenides 2023 (TMD2023)*, Cambridge, UK, 26-29 June, Poster

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Bin HAN

韩 宾

At ISIS, Strasbourg

Fonctionnalisation de Transistors à Effet de Champ à Base de Dichalcogénures de Métaux de Transition: Vers des Dispositifs Performants

Résumé

Cette thèse se penche sur l'optimisation des performances et la régulation des transistors à effet de champ (FET) à base de dichalcogénures de métaux de transition (TMD) bidimensionnels (2D) par stratégie de fonctionnalisation. Grâce à cette approche avancée, de nouvelles fonctionnalités sont développées et le contrôle des performances et de la polarité des transistors est réalisé. La fonctionnalisation des semi-conducteurs permet aux TMD 2D d'être prometteurs dans la discrimination des isomères. Grâce à une stratégie d'intégration de van der Waals (vdW), des électrodes de contact supérieur fonctionnalisées par couche moléculaire ou auxiliaire établissent un contact vdW sans épingleage au niveau de Fermi avec des TMD 2D. En modifiant le type moléculaire et la couche auxiliaire, les performances et la polarité du transistor sont modulées. Ces dispositifs ont démontré leur applicabilité en tant que blocs de construction pour les circuits intégrés, y compris les diodes et les onduleurs logiques. Notre stratégie de fonctionnalisation ouvre de nouvelles opportunités pour les applications TMD au-delà de la loi de Moore et des circuits intelligents intégrés.

Mots clés : dichalcogénures de métaux de transition, transistors à effet de champ, monocouches auto-assemblées, fonctionnalisation moléculaire, ingénierie des contacts vdW

Résumé en anglais

This thesis delves into the performance optimization and regulation of two-dimensional (2D) transition metal dichalcogenides (TMDs)-based field-effect transistors (FETs) by functionalization strategy. Through this advanced approach, novel functionalities are developed and control of transistor performance and polarity is achieved. The functionalization of semiconductors enables 2D TMDs to exhibit promise in isomer discrimination. Through a van der Waals (vdW) integration strategy, molecular or auxiliary layer-functionalized top-contact electrodes establish Fermi level pinning-free vdW contact with 2D TMDs. By altering the molecular type and auxiliary layer, the performance and polarity of the transistor are modulated. These devices demonstrated applicability as building blocks for integrated circuits, including diodes and logic inverters. Our functionalization strategy opens up new opportunities for TMDs applications beyond Moore's Law and integrated smart circuits.

Keywords: Transition metal dichalcogenides, field-effect transistors, self-assembled monolayers, molecular functionalization, vdW contact engineering