Diamond electro-optically controlled JFET

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To cite this version:

Martin Kah. Diamond electro-optically controlled JFET. Micro and nanotechnologies/Microelectronics. Université Grenoble Alpes [2020-..], 2024. English. NNT : 2024GRALT009 . tel-04584226

HAL Id: tel-04584226

https://theses.hal.science/tel-04584226

Submitted on 23 May 2024

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ GRENOBLE ALPES

École doctorale : EEATS - Electronique, Electrotechnique, Automatique, Traitement du Signal (EEATS)
Spécialité : Nano électronique et Nano technologies
Unité de recherche : Institut Néel

Transistor de type JFET en diamant controlé électro-optiquement

Diamond electro-optically controlled JFET

Présentée par :

Martin KAH

Direction de thèse :

Julien PERNOT PROFESSEUR DES UNIVERSITES, UNIVERSITE GRENOBLE ALPES	Directeur de thèse
Nicolas ROUGER Chercheur, Institut National Polytechnique de Toulouse	Co-directeur de thèse

Rapporteurs :

Jocelyn ACHARD
PROFESSEUR DES UNIVERSITES, UNIVERSITE SORBONNE PARIS NORD
Ken HAENEN
FULL PROFESSOR, Universiteit Hasselt

Thèse soutenue publiquement le **12 janvier 2024**, devant le jury composé de :

Etienne GHEERAERT, PROFESSEUR DES UNIVERSITES, Université Grenoble Alpes	Président
Julien PERNOT, PROFESSEUR DES UNIVERSITES, Université Grenoble Alpes	Directeur de thèse
Nicolas ROUGER, DIRECTEUR DE RECHERCHE, CNRS DELEGATION OCCITANIE OUEST	Co-directeur de thèse
Jocelyn ACHARD, PROFESSEUR DES UNIVERSITES, UNIVERSITE SORBONNE PARIS NORD	Rapporteur
Ken HAENEN, FULL PROFESSOR, Universiteit Hasselt	Rapporteur
Mariko SUZUKI, DOCTEURE EN SCIENCES, Universidad de Cádiz	Examinatrice
Florin UDREA, FULL PROFESSOR, University of Cambridge	Examinateur

Acknowledgement

In the context of this PhD journey, I am profoundly grateful to all the individuals and contributors within the diamond community who have tirelessly driven the advancement of this remarkable material. To those whom I've had the privilege of meeting and engaging with, I extend my heartfelt thanks for your warm welcome and the invaluable experiences shared. For those yet to be encountered, I trust that time will eventually lead our paths to cross. In both cases, for all readers, if any questions are raised by this manuscript, I would be delighted to try to answer them or discuss them, so please do not hesitate to contact me.

I wish to express my sincere gratitude to all the members of the jury Ken Haenen, Jocelyn Achard, Etienne Gheeraert, Mariko Suzuki and Florin Udrea (and a particular thought for Richard Jackman) for their unwavering interest and expertise, which have not only enriched me personally but have also greatly enhanced the quality of this manuscript. If I may, the following section is dedicated as a public expression of gratitude to those who have contributed to the completion of this endeavor, and is presented in their native language.

Il me tient à cœur de commencer ces remerciements par mes deux professeurs sans qui cette aventure n'aurait jamais pu voir le jour. Du fond du cœur, merci Julien Pernot et Nicolas Rouger. Merci pour votre confiance, patience, enthousiasme, les connaissances et l'expertise que vous m'avez transmises et plus généralement votre éducation, autant sur le plan personnel que professionnel. Merci Julien de m'avoir pris sous ton aile il y a cinq ans, d'avoir toujours maintenu un parfait équilibre entre encadrement et autonomie, et de m'avoir guidé à travers cette thèse plus comme un ami que comme un patron. Merci Nicolas pour ta disponibilité et ton optimisme sans faille, tu es l'une des personnes les plus efficaces que je connaisse, ta rigueur et ton organisation me serviront toujours d'exemple. En tant que "pères spirituels", vous avez su me transmettre votre passion pour le diamant et toutes ses particularités physiques, sujet sur lequel j'ai réellement pu m'épanouir durant ces cinq dernières années, et que je ne suis pas près de quitter de sitôt. Votre encadrement va me manquer, j'ai toujours du mal à être succinct, mais *Allez l'OM* !

Cette thèse, ainsi que tous les savoirs que j'ai pu acquérir au cours de celle-ci, aurait été beaucoup moins riche sans la présence de l'ensemble des permanents de l'équipe SC2G de l'Institut Néel, qui ont tous contribué à ce travail à un moment ou à un autre (et à mon épanouissement au sein de celui-ci). Merci David Eon pour ton soutien et tes enseignements, moi aussi j'aime la bière à la cerise. Etienne Gheeraert, merci d'avoir toujours pris un moment pour répondre à mes questions et merci de m'avoir prêté de la prestance quand le besoin s'en faisait sentir (tu m'enverras le modèle de ta veste de costume). Merci Etienne Bustarret., Pierre Muret et Gwénolé Jacopin pour m'avoir donné goût à la spectroscopie de manière générale et à toutes les discussions intéressantes qui vont de pair. J'aimerais aussi saluer tous les membres de l'équipe CS du Laplace, et particulièrement Marc Cousineau, Damien Risaletto, Anne Castelan et Marine Couret, qui ont porté une attention particulière à mes travaux ou avec qui j'ai eu la chance de collaborer sur d'autres projets.

Je souhaite exprimer ma reconnaissance envers toutes les personnes qui ont contribué, tant techniquement que moralement, en offrant leur expertise, leur compréhension et leur encouragement, transformant ainsi cette expérience de thèse en une aventure collective enrichissante. Mes premières pensées se tournent vers tous les membres de Diamfab, dont l'expertise a été cruciale dans la fabrication de mes échantillons. Cependant, je tiens surtout à vous remercier pour les précieux moments de convivialité et de camaraderie partagés ensemble. Ces moments ont créé des liens forts qui vont au-delà du cadre professionnel. Un remerciement spécial va à Juliette

Letellier pour m'avoir initié aux subtilités de la fabrication du diamant et pour avoir partagé avec bienveillance ses précieuses techniques secrètes.

Restant dans le contexte de la fabrication, je souhaite également exprimer ma gratitude envers tout le personnel du pôle NANOFAB, notamment Gwenaelle Julie, Jean-Francois Motte, Bruno Fernandez, Latifa Abbassi et Thierry Crozes. Avec 15 répétitions du dernier niveau de lithographie par échantillons, c'est principalement grâce à vous et à votre bonne humeur contagieuse que je garde un bon souvenir (presque nostalgique) de la salle blanche. Je suis également très reconnaissant de l'aide apportée par les ingénieurs de recherche des différents pôles techniques de l'Institut Néel, notamment Arnaud Claudel, David Barral, David Jeguso, Richard Haettel, Laurent Cagnon et spécifiquement Fabrice Donatini. Merci, Fabrice, pour tout ce que tu m'as enseigné, tout ce que tu as mis en place, mais surtout pour ton dévouement et ta sympathie.

Je n'oublie pas non plus ceux qui ont assuré un suivi régulier de mes travaux et de mon engagement, Alain Sylvestre, ma marraine Valérie Guisset et Clément Hébert, qui m'a également permis d'élargir mes horizons vers d'autres applications du diamant. Un merci particulier aux stagiaires Salma El-Messaoudi, Jacopo Ruggeri et Inès Alimi, qui sont venus m'épauler sur les mesures de ces composants innovants, et pour l'expérience qu'ils m'ont apportée. Je leur souhaite le meilleur pour la suite.

Je souhaite exprimer ma gratitude envers mes amis, qu'ils soient de longue date ou plus récents, et pour beaucoup rencontrés au cours de cette magnifique aventure. Merci à ceux qui sont éloignés, qui me connaissent depuis mes premiers signes de calvitie, mais avec qui rien n'a changé, comme Arnaud et Quentin. Merci au trio montagnard, Léo, Théodore et Théo, qui m'ont connu avec moins de cheveux mais qui m'ont toujours entouré et soutenu depuis. Un grand merci à la famille multiculturelle du bureau D423, Julien, Duy, Hussein, Coralie et Marine, qui a su illuminer toutes mes journées de travail, ainsi qu'une bonne partie de mes week-ends. Je suis reconnaissant envers ma fraternité espagnole adoptive, Jésus et Béa, ainsi que tous les autres doctorants que j'ai eu l'honneur de côtoyer au cours de ces cinq dernières années : Madalina, Rémy, Sylvain et Cédric. En tant que successeur de tes travaux, Cédric Masante, je te remercie beaucoup pour l'exemple que tu as été et pour le professeur que tu as incarné alors que j'étais encore ton stagiaire. Parler d'exemples, il me semble important de mentionner les anciens étudiants de l'équipe Gauthier Chicot, Khaled Driche, Jessica Bousquet et Juliette Letellier, qui sont restés dans le domaine (à peu près à un étage) et qui à leur tour, contribuent à former les générations futures. À mes compagnons encore sur la route, Damien, Dov, Hugo et Pietro, merci, et je vous souhaite autant de plaisir que j'en ai eu au cours de cette aventure.

Pour finir (et avec les meilleurs), je voudrais exprimer un immense merci à ma famille, à ceux que je considère comme mes parents, Laurent et Myriam, ainsi qu'à mes frères et sœurs de cœur, Romane, Mila et Léon. Merci, tonton, pour m'avoir appris à vivre avec passion, pour mes passions, et merci, Myriam, pour ta force et ta sagesse.

Nadège, un grand merci pour tout. Merci pour tout ton soutien, car sans ton aide, je n'aurais jamais pu m'épanouir de la même manière. Pour cela et pour tout le reste, tout le mérite de ce travail te revient.

Contents

List of Figures

List of Tables

Introduction

Energy stands as an indispensable cornerstone in the contemporary landscape of our societies, underpinning economic growth and modernization. Its value resonates across various economic sectors, playing a pivotal role in industrial processes, services, transportation and telecommunications, but also across vital aspects of life, clean water supply, heating or refrigeration unit and healthcare. Primary energy sources like natural gas, oil, coal, and uranium, found naturally as deposits on Earth, are routinely harnessed and primarily processed (mainly combusted) to generate electricity, which serves as a more convenient and versatile energy carrier that forms the backbone of our modern society. Coupled with a context of a burgeoning urban population, all around the world, and the emergence of new economies, the global demand for electricity is on an incessant rise. Over the next decades, experts from the International Energy Agency anticipate an astonishing growth in global electricity demand, from 16,400 terawatt-hours (TWh) per year in 2007 to a staggering 28,900 TWh per year by 2030. Moreover, the increasing population density in compact urban regions, combined with the preferred decentralized electricity generation, underscores the necessity of enhancing our electrical transport and conversion infrastructures, particularly in light of the challenges posed by its storage.

Even if the world electricity demand remained resilient in 2022 amid the global energy crisis triggered by Russia's invasion of Ukraine, the soaring demand for electricity still rose by more than 2% per year, hence brings forth pressing concerns. The consistent and sustainable supply of electricity is know from the beginning of industrial era to be under threat due to the finite nature of primary energy sources. Additionally, regarding the climate concern our society tends to initiate, the production of electricity is responsible for a significant portion of greenhouse gas emissions, particularly carbon dioxide (CO_2). These emissions contribute to the overall increase in global warming and, consequently, the ongoing challenge of climate change. The projection indicates a worrisome trajectory, with CO_2 emissions from electricity production expected to surge by approximately 40% by 2030.

Reducing the environmental impact of electricity production and effectively managing fossil energy sources are critical imperatives for perennial modern societies. The global focus on sustainable development and combating climate change is evident in initiatives taken by the biggest consumer countries, especially European ones or the USA. Interestingly, "Smart Grid" projects, which aimed at dynamic energy management through continuous communication between, various asynchronous production site, utilities and consumers, have been well-received and tends to be adopted worldwide. Incorporating adaptive power conversion systems, control units, and automated flux regulation into the electricity distribution network inherently enhances loss management. This approach ultimately facilitates, implantation of renewable energy sources on electricity distribution network and a more balanced production-to-consumption ratio, aligning ecological and economic priorities for both producers and consumers. Alongside smart grids, the electrification of the transport and heating sectors continued to accelerate globally, with record numbers of electric vehicles and heat pumps sold in 2022, contributing to this green energy paradigm shift.

At the core of these embedded or intelligent energy systems, power semiconductor devices play a pivotal role in sustaining high voltage, current, and temperature demands, particularly in applications like power conversion. Historically, silicon has been the dominant material for power devices due to its well-established technology and cost-effectiveness, benefiting of more than 60 years of extensive research and development. However, silicon devices are encountering limitations associated with their physical properties. As device designs become more complex and intricate, enhancing silicon's performance becomes increasingly challenging and costly. In contrast, a transformative shift has been unfolding in recent years with the adoption of wide-bandgap semiconductors like SiC and GaN, which offers better performances than silicon in terms of power handling, switching-frequency and lower losses for smaller devices active area. Both material mentioned herein-above have been widely developed since twenty years and are already commercially available. However, based on the same performances trade-offs, "Ultra-Wide Bandgap" (UWBG) materials, including AlN, Ga_20_3 and Diamond, are recently explored as they feature superior properties that could pave the way for the next generation of power electronics devices. Unipolar UWBG semiconductor devices, capable of matching or surpassing the current-carrying capacity of bipolar silicon devices, offer significant advantages in terms of operational frequency and reducing energy losses, which place them as highly beneficial materials for potential integration into power converters.

Even if diamond-based technologies are at their early stage of development and way less mature than their competitors on power market, they tend to gain substantial attention for applications beyond conventional semiconductor technologies. The limitations of incremental approach for diamond-based devices, e.g. applications of concept originally developed for silicon where much smaller band gap energies are at stake, are well-established and tend to be overcome through the increasing number of innovative diamond-based devices proposal. Thanks to its exceptional physical properties diamond offers novel opportunities for a wide range of multi-disciplinary application, like: localized electric and magnetic signal probing, reliable data processing, and secure communication in both harsh and in-vivo biological environments. The development of diamond devices capable of non-volatile charge storage and individual device addressing is essential for creating monolithic diamond-based systems. These devices can serve various purposes, from on-chip energy storage for power supply to information storage with read and write access (non-volatile memory), or be individually addressed on-chip for applications in neuronal multiplexers and hold potential for aerospace and harsh environment applications.

This thesis revolves around the convergence of power electronics and novel hybrid technologies that integrate optical and electrical principles to leverage the vast energy potential inherent in diamond. Recent advancements have showcased diamond power devices with intrinsic, p-type, and n-type doping control, opening up exciting opportunities for innovative control mechanisms. Nevertheless, several technological challenges must be overcome before these devices can fully unlock the potential of diamond and its large-scale production. In the context of developing diamond JFETs involving n-type diamond doping, several critical issues need to be addressed:

- (i) How can we develop and implement reliable device models that account for the unique characteristics of diamond? Is the high ionization energy of dopants redhibitory or, oppositely, a new playground for innovative concept?

- (ii) Is diamond mature enough for conceptualization of large-scale devices meeting power market specifications? Is it possible to harness existing processes and established design methodologies employed in others power-oriented materials to showcase the feasibility of large-scale device production using diamond, transcending the prevalent focus on miniature configurations?

- (iii) Is the recently demonstrated electro-optical control of diamond pn junctions reproducible and exploitable as a building block for the production of diamond-based memories? Is phosphorus-doped diamond, with lower activation energy than nitrogen-doped diamond, beneficial in an optimized structure regarding the switching capabilities and the optical control?

- (iv) How can we experimentally verify the substantial potential of diamond-based non-volatile photo-switches, demonstrating their adaptability for specific applications and seamless integration into devices initially not tailored for such functionalities?

To provide answers to these issues, this manuscript is organized as follows:

- **Chapter 1:** The first chapter introduces diamond as the ultimate Ultra-Wide Band-Gap Semiconductor (UWBGs) regarding its overwhelming properties. State-of-the-art concerning diamond diodes and most advanced transistors, particularly well-suited for power electronics, are presented. Specific attention is also paid to optically-active defects in diamond, which have gained increasing interest in recent years. As a bridge between optically-controlled memory and power electronic transistors, the innovative concept of the diamond-based Non-Volatile Photo-Switch (NVPS) is introduced. Within the context of this thesis, an optimized NVPS structure designed for high-power management in memory applications, is proposed.

- **Chapter 2:** Comprehensive exploration of the design considerations for large-scale NVPS devices by delving into the intricacies of the sustainable fabrication processes, the optimization of device parameters, and the expected performance characteristics is provided along the second chapter. Given the early-stage success of realizing a diamond-based non-volatile memory within this thesis, this chapter concentrates on the fundamental building blocks that have been incorporated to enhance the device's functionality. Additionally, it extends into the development of large-scale devices through an interdigited architecture to align with the requirements of the power electronics market. Numerous parameters, spanning the domains of diamond growth and device geometry, necessitate careful adjustment to align with the expected performance criteria for the final component. These adjustments often involve trade-offs among various parameters. Therefore, a comprehensive understanding of the underlying physics of diamond, particularly in the context of JFETs, even within a simplified 1D model, is indispensable. This understanding serves the dual purpose of evaluating the potential of diamond-based devices and providing a foundational framework for comparison with experimental results.

- **Chapter 3:** Once ideal structural and geometrical parameters has been computed through specific trade-offs to propose an optimized JFET architecture, the third chapter present the fabrication process aside with layers and contacts characterizations. Failure analysis is also conducted and discussion are opened around impact of the diverse parameters divergence regarding functionalization of the devices.

- **Chapter 4:** The last chapter delves into the remarkable capabilities of diamond-based non-volatile photo-switches (NVPS) and their potential memory-related applications. Examination of the underlying principles, operation, and advantages of diamond-based NVPS are presented, while their robustness and capacity for high-speed operation have been enhanced, underlying promising prospect concerning their memory applications. Benefits of gate contact closering in comparison to the reference sample, previously fabricated by C. Masante during his thesis, and its potential for switching without leakage currents or compromising device robustness, is demonstrated.

Chapter I

Diamond, quintessential material for next generation electronic devices

This first chapter serves as an introduction to diamond, one of the most renowned allotropic forms of carbon, recently proposed as promising Ultra-Wide Band-Gap Semiconductor (UWBGs) with immense potential in advanced technologies. Overwhelming properties of diamond, its promising modern applications and the current synthesis methods employed to meet the growing demand for cutting-edge diamond-based devices, are introduced. Historically known primarily for its role as an insulating gemstone, laboratory-grown diamonds have now been harnessed to efficiently modulate and control electrical conductance, even achieving metallic conduction. This capability holds significant promise for emerging diamond-based diodes and transistors, particularly well-suited for power electronics. Specific attention is also paid to optically-active defects in diamond, which have gained increasing interest in recent years. Notably, the Nitrogen-Vacancy (NV) center charge state has exhibited remarkable results in the realm of quantum communication, serving as a key component of quantum memory systems. As a bridge between optically-controlled memory and power electronic transistors, the innovative concept of the diamond-based Non-Volatile Photo-Switch (NVPS) is introduced. Within the context of this thesis, an optimized NVPS structure designed for both high-power management alongside the additional prospects of memory applications, is proposed.

I.1 Diamond exceptional properties for advanced technologies applications prospects

In a society where the term *Carbon* tends to carry a negative connotation, one of its most renowned allotropic forms, diamond, paradoxically remains a symbol of opulence and prestige. This paradox is intricately connected to the environmental and economic challenges that our modern society confronts, particularly in the realm of energy management. As semiconductors play a pivotal role in addressing these challenges, this introductory section aims to unveil the exceptional attributes of diamond and explore its diverse range of multidisciplinary applications.

I.1.1 The vision of diamonds through the ages

Human understanding of diamonds has naturally evolved over the ages, yet the almost sacred reverence associated with these precious gems, as observed in the earliest recorded accounts of their discovery, remains deeply ingrained in the collective consciousness. The earliest mentions of diamonds in human history trace back to 3000 BC in India [1, 2], where Buddhist texts referred to them as the *fruit of the stars* [3]. Notably, during this period, glass had not yet been discovered, and the gem's transparency, symbolizing purity, was the foremost physical characteristic observed by humanity. This inherent transparency has continued to captivate our fascination through the ages. Another well-known property of diamonds, their exceptional hardness, was first harnessed by our civilization around 400 BC in China and Yemen. During this time, diamonds were utilized to shape and drill a variety of iron tools [4], as well as to manufacture on other precious gemstones like sapphire and jade pearls [5]. This practice was also widespread in ancient Egypt, where diamonds were regarded as unbreakable and chemically indestructible [6, 7].

During the same era, around 300 BC in ancient Greece, the mechanical properties of this remarkable gem were so captivating that its name underwent a transformation, evolving into ἀδάμας (adamas), which translates literally to *unshakeable, unbreakable, inflexible* [8]. Nevertheless, diamonds retained a strong connection to the divine realm, often being referred to as the hardest material used to craft the weapons and instruments of the gods, such as Cronos' sickle or Cupid's arrow [9]. It was believed that only the gods possessed the secret to their creation. This belief, however, is a testament to the enduring challenge, still relevant today, of polishing, cutting, and crafting diamonds. This period left an indelible mark on the history of diamonds, primarily through the legacy of their name, ”adamas,” as emphasized by the philosopher Θεόφραστος (Theophrastus) in his work Περὶ Λίθων (Treatise on Gemstones) [10]. The philosophy of Theophrastus advocated that ”humans should be encouraged to seek knowledge through science rather than rely solely on wealth.” This perspective may seem somewhat paradoxical in the context of diamonds today. Their natural forms, hardness, transparency achieved through partial polishing, and rarity render them inherently alluring. Consequently, diamonds have been highly coveted and symbolized richness since Antiquity.

This image of wealth and nobility persisted throughout the Middle Ages and the Renaissance [11]. During this time, diamonds were primarily used for ornamental and medicinal purposes. European kings eagerly sought them for their crowns due to their rarity and beauty [12], to the extent that Louis IX enacted sumptuary laws reserving diamonds exclusively for the sole sovereign [13]. Nobility assigned arbitrary medicinal properties to diamonds, particularly a presumed ability to counteract poisons. However, this belief was cast into doubt when Pope Clement VII died from ingesting diamond powder [14, 15]. It is also worth noting that the association of wealth with diamonds was limited to male sovereigns until 1477 when Maximilian I broke with tradition by presenting his wife with a diamond engagement ring [16]. This custom persisted into the modern era, where it evolved into a thriving market where natural and synthetic diamonds competed [17].

Our understanding of diamonds has undergone a significant transformation over the past two centuries, particularly in the modern and contemporary eras. This transformation was initiated by the collaborative efforts of A. Lavoisier [18, 19] and S. Tennant [20], who demonstrated that diamonds, much like coal, were composed of pure carbon. This revelation, supported by the fact that the combustion of diamonds produced the same volume of carbon dioxide as an equivalent mass of coal, sparked a race to synthesize diamonds. This race not only spurred in-depth investigations into diamond properties but also delved into the processes responsible for their formation. However, these early attempts were often met with failure, with notable efforts led by J.B. Hannay [21] and H. Moissan [22]. Interestingly, Moissan, in the course of an unsuccessful attempt, managed to synthesize silicon carbide (SiC) in 1894, which is nowadays a (more advanced) rival to diamonds in power electronic market. The race to create diamonds reached its culmination in 1955 when F. Bundy and H.T. Hall [23] published their groundbreaking work, providing the first definitive proof of successful diamond synthesis. Simultaneously, advancements in quantum physics and solid-state physics were revolutionizing our understanding of diamonds, asides with its newly industrial accessibility, a wide range of applications has been opened up. All these recently understood properties and applications, positioning diamond as one of the ultimate materials for our future needs, will be delve in greater detail along the different parts of the following sections.

I.1.2 Crystalline structure

When we refer to carbon, we are usually referring to its best-known stable isotope, Carbon-12 $\left({}^{12}_{6}C\right)$, which is composed of six protons, neutrons and electrons. Its ideal symmetry of mass between the baryons that make up the atomic nucleus (protons and neutrons) and, above all, of charge between the electrons and protons, gives an atomic orbitals (AO) configuration (or commonly called electronic configuration) of the $1s^2\ 2s^2\ 2p^2$ type. Inherited from the precepts of quantum mechanics, an AO represents iso-surfaces, which delimit the region within which the probability of the presence of an electron is maximal. The AO representation, which takes into account the undulatory behaviour of the electron, is a direct extension of Bohr's atomic model, in which carbon has four electrons in its outer L-shell. From this configuration, carbon is bivalent and only these four electrons, two in the s-orbitals and two in the p-orbitals, contribute to the formation of covalent bonds. These orbitals can't form molecular bonds directly, but as a linear combination of the orbitals, called hybridization, molecular bonds are possible. In the case of carbon, three different configurations of the AO are possible, among sp-, sp^2- or sp^3-hybridization.

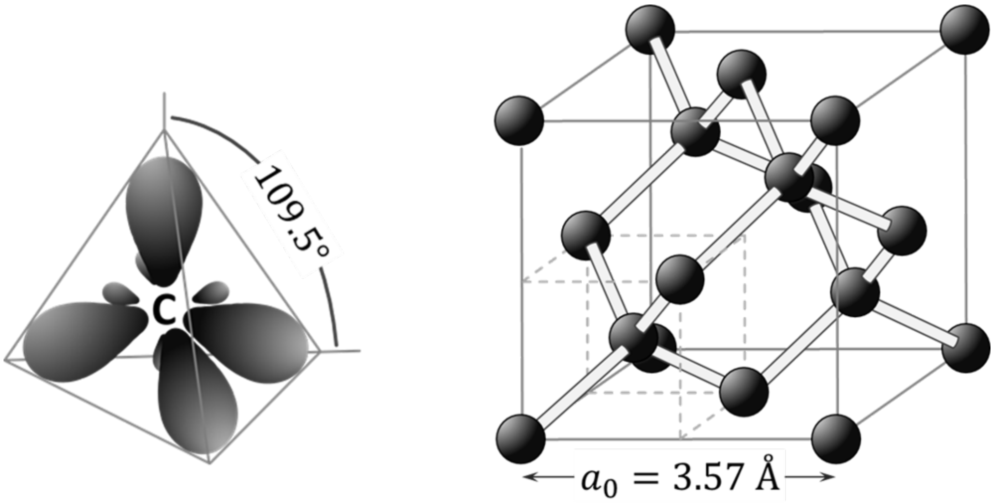

Figure I.1: Left, schematic representation of the four sp^3-hybridization of carbon atomic orbitals, inscribed inside a tetrahedron where the four carbon closest neighbours are angled by 109.5°. Right, diamond unit cell composed by face centered cubic lattice structure with a motif of two basis carbon atoms at each lattice point, sitting at $(0,0,0)$ and $\left(\frac{1}{4},\frac{1}{4},\frac{1}{4}\right)$. The tetrahedral sp^3-hybridization of carbon atoms are constrained inside the dashed cube, representing one fourth of the unit cell volume.

In the most simplest sp-configuration, one (and only one) p-orbital is hybridized with one s-orbital, forming two sp-orbitals that are opposed to each other with an angle of 180°. The demonised carbon dioxide (CO_2), is the perfect example of this hybridization, were a single carbon atom is twicely double bounded to two oxygen atoms in the same plan. For sp^2-configuration, two of the three p-orbital are hybridized with the s-orbital, leading to three equal sp-orbitals that are flatly oriented with an angle between each other of 120°. Bonds along this hybridized configuration, typically give rise to the most stable form of carbon but also an excellent conductor for heat and temperature, the so-called graphite. Last but not least, the sp^3-hybridization describing diamond is formed when all the three p-orbitals are hybridized with the remaining s-orbital, leading to four equal sp^3-orbitals. These AO can be inscribed into tetrahedrons, separated by an angle of 109.5°, as schematically depicted in Fig. I.1. This configuration mainly describes methane (CH_4) stable in its gaseous form under normal temperature and pressure conditions, but also diamond as the high pressure allotropic form of carbon, meta-stable at low temperature and pressure. In the later diamond sp^3-hybridization, each carbon atoms are bound to four others in order to form a face-centered cubic (FCC) Bravais lattice with a motif of two carbon atoms.

Diamond primitive unit cell, depicted in Fig. I.1, can be seen as equivalent to two interpenetrating FCC lattices, offset from one another along a body diagonal by one-quarter of its length. The structure motif is thus composed of two carbon atoms located at each lattice point, one at $(0, 0, 0)$ and the other at $\left(\frac{1}{4}, \frac{1}{4}, \frac{1}{4}\right)$, where the coordinates are fractions along the cube side, of length $a_0 = 3.567$ Å. Subsequently, the closest carbon atoms covalent bond length is equal to 1.54 Å which, coupled to the eight equivalent carbon atoms in the unit cell, give rise to the highest naturally occurring atomic density of 1.76×10^{23} cm^{-3}. Multiplying this huge atomic density by the average atomic mass of a carbon atom results in a theoretical mass density for diamond of 3.52 g/cm^3. Compared to other semiconductors having the same *zincblende* lattice structure, like silicon (Si), gallium arsenide (GaAs) or indium antimonide (InSb), a unique feature of carbon atoms in the diamond lattice is the strength of their bonds. The cohesive energy in diamond being 7.58 eV/atom [24, 25], it explains the relatively high energy (between 30 and 45 eV [26] depending from crystalline orientation) necessary to displace an atom from its Bravais lattice site. All these properties - compactness, strong intrinsic bonds and high displacement energy - form the basis of the exceptional mechanical properties attributed to diamond.

I.1.3 Mechanical applications of the hardest naturally occurring material

Diamond has been previously mentioned as a meta-stable allotropic form of carbon under our atmospheric pressure and temperature conditions, but paradoxically, it is also one of the hardest and most durable materials known to humanity. As mechanical properties of diamond could be the subject of a whole thesis, only the most impacting properties are roughly summarized in table I.1 and discussed along this section, in order to further introduce the importance of diamond crystals sizes and orientations.

Table I.1: Comparison of mechanical properties for silicon (Si), silicon carbide (4H-SiC) and diamond.

	Si	4H-SiC	Diamond
Cohesive energy (eV/atom)	4.63 [24]	6.34 [27, 28]	7.58 [24, 25]
Hardness (kg/mm^2)	1000-1500 [29]	3450-3750 [30]	4000-12200 [31]
Young's modulus (GPa)	130-190 [32]	347-440 [33, 34]	500-1200 [31]
Shear modulus (GPa)	50-80 [32]	130-197 [33, 34]	500-570 [35, 36]
Poisson's ratio	0.065-0.36 [32]	0.13-0.23 [33, 34]	0.075-0.2 [37, 38]
Fracture toughness ($\text{MPa.m}^{1/2}$)	0.62-1.29 [32]	1.4-3.47 [30, 39]	5-18 [31]
Tensile strength (GPa)	0.9-16 [40, 41]	0.8-13.5 [42]	90-225 [43]
Compressive strength (GPa)	3.5-13 [41, 44]	30-34 [45]	223-470 [43]

From quantum mechanics, it has been showed that strongest atoms bonding is obtained, in solids, between AO of the same energy level. Applied to carbon in its diamond crystalline structure, carbon atoms are strongly bounded to each others, rendering diamond extremely hard. It ranks as the hardest natural material on the Mohs scale of mineral hardness, with a perfect score of 10. This means that it can only be scratched by another diamond, making it highly resistant to wear, abrasion, and scratching. Coupled to its impressive tensile strength, which means that diamond can withstand a tremendous amount of force without breaking or deforming, it is exceptionally durable in various applications, from cutting tools (angle grinder blades) to industrial materials (diamond cutter and anvil).

Compared to silicon (Si) and 4H-silicon carbide (4H-SiC), diamond is extremely stiff and exhibits one of the lowest friction coefficient. These properties can be directly observed through its high Young's modulus or Shear modulus which are the highest observed for naturally occurring materials. Diamond is able to maintain its shape and resist deformation even when subjected to heavy loads or pressure and is particularly valuable in mechanical systems where minimizing friction is essential.

While diamond is exceptionally hard, it is not particularly tough in the sense of resisting fracture or shattering. It can be brittle and may cleave or fracture along specific planes when subjected to a strong impact or stress concentration. This inhomogeneity along its primary crystallographic planes is responsible for the huge discrepancy of each value reported in table I.1, for all the materials compared. In a diamond gem of finite volume, the unit cell introduced earlier (Fig. I.1) is isotropically and homogeneously repeated numerous times. The periodicity of the pattern is expressed through a network of nodes (lattice apexes) which, when joined in pairs, define a directional vector of the Bravais lattice, more commonly known as the reticular direction. These directions are affiliated with perpendicular planes, reticular plans, along which diamond gems facets demonstrate different physical properties. Two of the mainly used diamond crystalline orientation, (001) and (111), are depicted in Fig. I.2, illustrating the transition from the unit cell to an extended lattice.

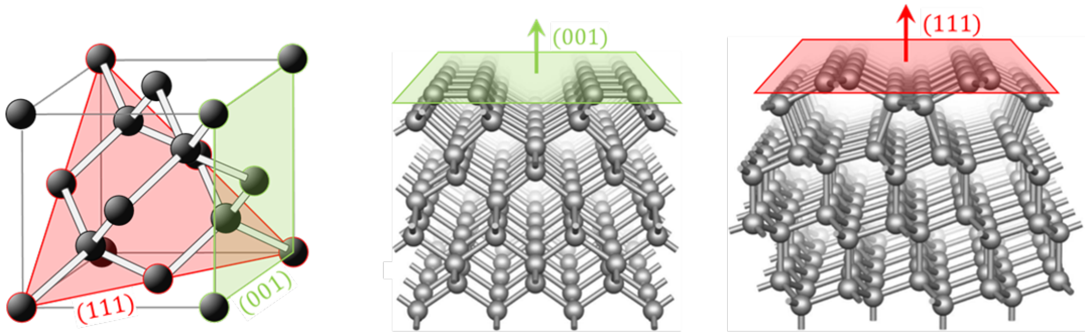

Figure I.2: Left, diamond unit cell with enlightened, in green the (001) reticular plan on a side of the cubic face centered lattice, and in red the (111) reticular plan along the cube diagonal. Center, perspective view of the (001)-(2×1) surface, where the uppermost C atoms form isolated dimers. Right, the (111)-(2×1) Pandey-chain surface, in which the top two rows of C atoms form zigzag chains extending into the plane of the diagram. The perspective views of the atomic geometries are the most stable for the clean (001) and (111) surfaces. Representation taken from [46].

First-principles calculations, based on density functional theory (DFT), have revealed an intriguing phenomenon in diamond's mechanical properties. When subjected to compressive or tensile forces along the (001) direction, the material displays nearly identical strengths, both around 225 GPa. However, in the (111) direction, a substantial discrepancy is evident, with tensile strength measuring approximately 90 GPa and compressive strength soaring to about 470 GPa [43]. This significant difference has also been experimentally confirmed with diamond nano-needles [47], underlining that the quality of the diamond itself plays a vital role, most of the time even more critical than its crystalline orientation. It is essential to note that in all the properties discussed herein-above, calculations are based on the assumption of a pure diamond crystal (or Si and 4H-SiC, respectively), and the experimental values are derived from high-purity mono-crystals. Any disruption of the crystalline periodicity, such as dislocations, point defects, or impurities, can significantly diminish the mechanical properties of diamond. This ultimately renders diamond a fragile material, as demonstrated in a sample fabricated within this thesis (detailed in section III.2.2). From a different perspective, the intentional introduction of non-carbon species into the diamond lattice is significantly influenced by its crystalline orientation. This adds complexity to diamond doping but underscores its importance in the development of future components based on this extraordinary material.

I.1.4 Band structure

To deepen the comprehension of diamond's extraordinary properties, it is imperative to introduce the concept of the electronic band structure. This forms the foundation of our understanding of the diverse mechanisms governing thermal and electrical conduction, as well as optical absorption and emission in diamond. The electronic band structure delineates the spectrum of possible and forbidden energy states that electrons (or their absence, namely holes) within the solid can occupy. Similar to the prior sections, the mathematical formalization of the band structure became attainable through the quantum perspective on matter, particularly emphasizing the wave-particle duality of electrons. For a single-electron scenario, independent of time, the energy acquired by the electron, denoted as E_k, is correlated with its wave-function, represented as $\psi_k(\vec{r})$, where $\vec{r}$ stands for the position vector, through Schrödinger's equation:

$$\left[-\frac{\hbar^2}{2m^*}\Delta^2 + V(\vec{r})\right]\psi_k(\vec{r}) = E_k\psi_k(\vec{r}) \tag{I.1}$$

Where, $\hbar$ represents the reduced Planck's constant, m^* denotes the electron mass, Δ stands for the Laplacian operator and lastly, $V(\vec{r})$ accounts for the polynomial potential that influences the electron within the diamond lattice. Concerning this potential, the forces acting on an electron at any point in space within the crystal, denoted as $\vec{r}$, is directly derived from this potential $V(\vec{r})$. Consequently, its expression must encompass potential interactions between the electron and all subsequent electrons and carbon atoms comprising the nearly infinite diamond lattice, compared to the unique electron's size and mass. This situation gives rise to an N-body problem, for which analytical or numerical solutions are nonexistent. Nevertheless, this challenge was addressed through a formulation initiated by F. Bloch during his thesis [48], astutely pointing out that "in the case of a perfect infinite crystal, electrons are subject to a periodic potential with the translational symmetry of the atoms constituting the crystal". Utilizing the Bloch theorem, which hinges on the crystal's symmetry and, consequently, the periodic nature of the potential energy $V(\vec{r})$, the solutions of the Schrödinger's equation yield a wave-function basis, each associated with an energy eigenstate:

$$\psi_k(\vec{r}) = e^{i\vec{k}\vec{r}}U_n(\vec{k},\vec{r}) \tag{I.2}$$

with $\vec{k}$ representing the wave vector, n as a numerical index associated with the band number, and $U_n(\vec{k},\vec{r})$ as a periodic function replicating the lattice periodicity along $\vec{r}$. While the work of Bloch introduced a profound understanding of crystal symmetry and periodicity, a better representation has been brought by L. Brillouin [49] through the integration of a zone in reciprocal space (phase space) bearing his name. The first Brillouin zone can be described either as the volume enclosed by surfaces equidistant from the central atom and its nearest neighbors or as the set of points in k-space reachable from the origin without crossing a reticular plane. As illustrated in Fig. I.3 (top right) for diamond, the first Brillouin zone is the minimal volume that allows tiling the reciprocal diamond space without gaps. Within this zone, electron behaviors can be projected throughout the entire crystal. The intersection of Brillouin's and Bloch's work can be summarized as most pertinent information for understanding a crystal's electronic properties resides within the first Brillouin zone, particularly within its energy bands.

Energy dispersion curves for diamond as a function of the wave vector calculated either by using the *ab initio* discrete variational method with linear combination of AO (LCAO) Bloch basis set [50], or the empirical pseudo-potential method (EPM) [51], are shown in Fig. I.3. The dispersion curves are represented for wave vectors along paths in the first Brillouin zone, colored for representation purpose, and major symmetry points (Γ, Δ, etc.) have been enlightened.

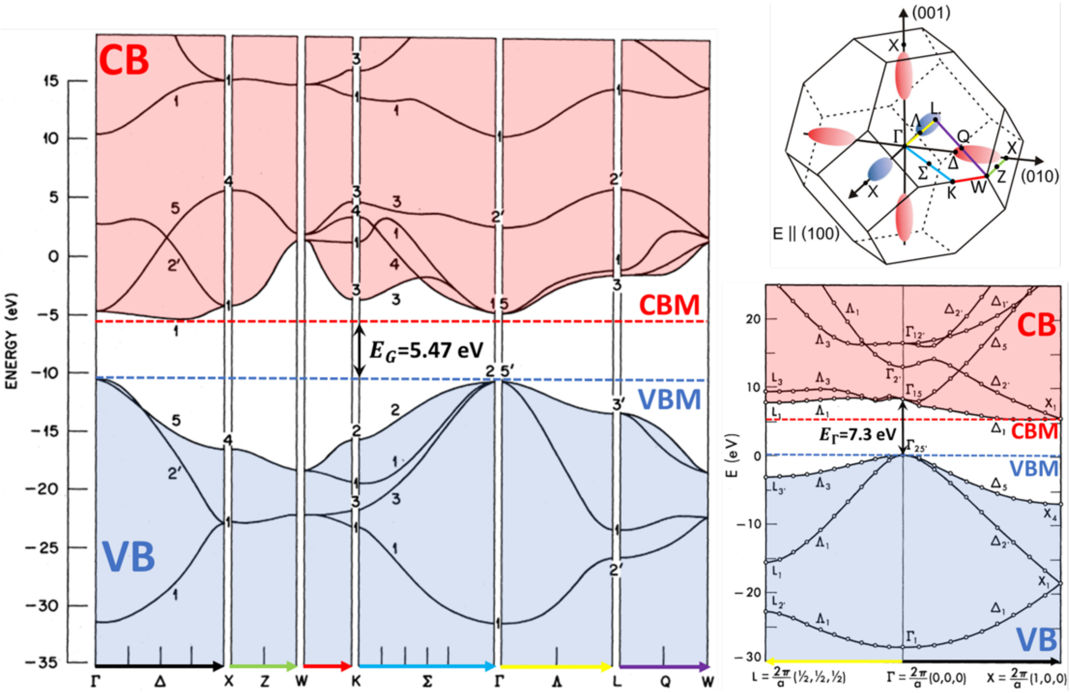

Figure I.3: Diamond electric band structure at 300 K computed by: on the left, ab initio calculation using LCAO and taken from [50]; bottom right, EPM, taken from [51]. The valence band with its VBM has been re-colored in blue, and the conduction band with its CBM in red, in order to enlighten the diamond indirect bandgap of 5.47 eV, compared to the direct bandgap of 7.3 eV at the Γ point. Top right, diamond first Brillouin zone taken and modified from [52], with the six equivalent conduction band valleys highlighted such as the wave vector emphasized.

Energy dispersion curves can be classified into two primary bands, creating a continuum of allowed energy states separated by a gap of forbidden energy eigenstates. The valence band (VB), depicted in blue in Fig. I.3, with its valence band maximum (VBM) situated at Γ, encompasses electrons that contribute to the local cohesion of the solid. Electrons within the valence band are localized and, therefore, cannot participate in electrical conduction phenomena, even if absence of electrons, namely holes, which are in turns delocalized in the VB can efficiently participate to electrical conduction. In contrast, the conduction band (CB), in red, with its conduction band minimum (CBM) located at (0.76, 0, 0) from Γ, along the Γ-X direction, comprises electrons in delocalized states that partake in electrical conduction. Furthermore, due to crystal symmetry of the Fd$\bar{3}$m class, six equivalent CBM (valleys), located along (001) reticular planes, are available for diamond similarly to silicon that belong to the same group of symmetry. Electronic properties of solids are fundamentally contingent on the distribution of electrons in the VB or CB, as well as the energy gap that separates them. At the center of the Brillouin zone, at the Γ symmetry point, diamond exhibits a direct band gap of 7.3 eV. This value is so substantial that, in isolation, this localized transition renders diamond purely insulating. From a different perspective, the extensive overlap of atomic orbitals (AO) of adjacent carbon atoms involved in a C-C covalent bond generates a consequent energy difference between the occupied bonding AO and the unoccupied anti-bonding AO, resulting in a wide forbidden energy gap. However, the minimum bandgap of diamond, arising from the difference between the CBM and the VBM, is indirect and computed to be 5.47 eV at 300 K. This value remains very high, however, which justifies the fact that diamond was for a very long time considered to be an insulator, before being used as a semiconductor, and even now as a ultra-wide bandgap semiconductor (UWBGs). The term “indirect” signifies that for an electron to transition from the VB to the CB, it must receive not only the energy of the indirect bandgap but also an additional momentum provided by another source. Temperature, manifesting as vibrations of the carbon atoms around their

Bravais lattice positions or through quasi-particles called phonons, enhances this transition probability. As phonons interactions present a major concern in diamond electrical, optical and thermal properties the next section is dedicated to their influence.

I.1.5 Role of phonon in diamond properties

Phonons are quanta of vibrational energy associated with the lattice vibrations in a crystalline material, and are often described as collective vibrational modes involving the motion of atoms around their Bravais lattice position in a crystal. Similarly to photons, phonons exhibit both particle-like and wave-like characteristics, and thus are mainly characterized by a wave-vector. The latter represents their momentum in the reciprocal space of the crystal lattice, imaging their propagation direction, and is correlated to the phonons frequencies which determine their energy. This correlation is done through phonon dispersion relations, specifically reported for diamond in Fig. I.4, which are at the origins of many diamond macroscopic transport properties.

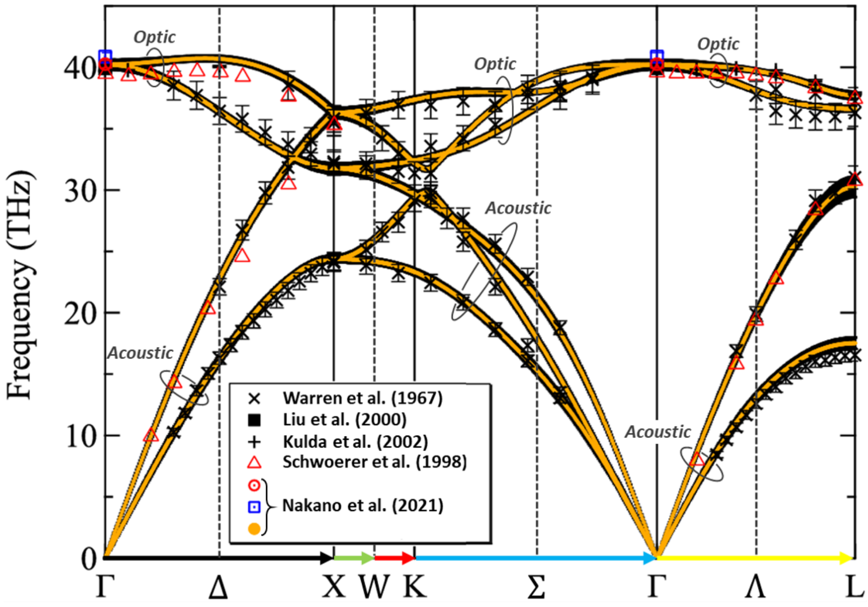

Figure I.4: Phonon dispersion relation of diamond, taken and modified from Nakano et al. [53]. Experimental data acquired by neutron or X-rays scattering are gathered from the work of Warren et al. [54], Liu et al. [55], Kulda et al. [56] and Schwoerer et al. [57]. Theoretical points, computed by ab initio variational quantum Monte Carlo (VMC) simulations, and sourced from [53] are displayed through yellow circles. Calculated Raman frequencies are additionally shown through dotted red circles and dotted blue squares.

Phonons are splitted in two main types corresponding to dedicated generation mechanism and properties. The former, acoustic phonons, corresponds to coherent movements of lattice atoms out of their equilibrium positions and are mostly induced by thermal excitation or stress relaxation. These acoustics modes are commonly associated with relatively low energies and long wavelength. They are differentiated by their propagation direction or polarisation vector, commonly expressed through comparison between wave vectors to the high symmetries directions: longitudinal acoustic phonons (LA) or transverse acoustic (TA). The second, optical phonons, corresponds to out-of-phase movements of lattice atoms where their oscillations results in a change in the crystal's dielectric constant (its ability to respond to an electric field). These modes are induced by electromagnetic radiation in the optical frequency range and can only be induced in crystal structure with more than one atom per unit cell, like diamond, silicon or 4H-SiC. Oppositely to acoustic phonons, optical phonons have an higher energy range, linked to more complex atomic motion, but similarly to the former, they are differentiated by their propagation direction: longitudinal optic phonons (LO) or transverse optic (TO).

Regarding diamond, since there are two carbon atoms in the unit cell, Born Von Kármán periodic conditions lead to the discretization of six different phonon branches: three acoustic and three optic branches. While materials with phonon band gaps are typically insulators, those without band gaps, like diamond, are more often considered as conductors or semiconductors. Due to the close proximity of carbon atoms in the diamond crystal lattice, phonon vibration modes with very high energies are allowed, affiliated with oscillation frequencies exceeding tens of terahertz. These high-energy phonons play a significant role in defining the mechanical properties of diamond reported in Table I.1. The elevated phonon frequencies in diamond result in high group velocities of acoustic waves. In essence, the speed of sound in diamond, ranging from 12 to 18 km/s, stands as one of the highest observed to date. This extreme speed of sound is directly linked to the elasticity constants of diamond and underpins the exceptional value of the Young's modulus for this material. While this sound velocity exhibits anisotropic characteristics and strongly depends on the direction of wave propagation, the high frequencies associated with transverse phonons are responsible for the notably high shear modulus.

The phonon dispersion relation may seem somewhat abstract, but the study of the carbon atoms that make up diamond on an atomic scale makes it possible to justify its exceptional mechanical properties, as well as its thermal, optical and electrical properties. As these latter properties are at the heart of this manuscript, the next sections will be dedicated to them.

I.1.6 Electrical properties

Since diamond belongs to UWBGs, intrinsic diamond conduction band is almost devoid of free electrons at room temperature (RT). Since 5.47 eV are required to push a valence electron inside the conduction band and the thermal energy at 300 K being 0.025 eV, intrinsic carrier can be considered nonexistent in diamond at RT. Subsequently intrinsic diamond resistivity is huge compared to others industrially used semiconductors (Si, 4H-SiC) and diamond is generally recognized as an insulating material. Due to the consequent cost of diamond substrate and their limited availability on semiconductors market, diamond will never compete with silicon in the domain of micro-electronic, where decades of research and development brought the later to its hegemony. However, in a society where power consumption exponentially increases, efficient energy conversion and management, as main concern of power electronics, push silicon to face its electrical and physical limits. In this context, diamond, as the crown jewel of UWBG semiconductor, is expected to overcome every other materials for this specific power electronic applications, due to its unique electronic properties summarized in Table I.2.

In intrinsic diamond (and semiconductors in general), phonon scattering governs the free carriers velocity under high electric field, commonly named saturation drift velocity [62, 63]. Therefore due to accessibility of highly energetic optical phonons (160 meV), diamond is one of the material of the highest saturation drift velocity, as with 2.7×10^7 cm/s reported for electrons [64]. Diamond carriers (both for holes and electrons) saturation velocity is higher than in Si or 4H-SiC, and unlike its competitors, this velocity maintains its high rate even under high-intensity electric fields [65, 66]. Although, an anisotropy of the charge carriers' drift velocity is observed in diamond with respect to the main crystallographic directions, as a direct consequence of the multi-valley band structure.

Diamond relative dielectric constant is defined by the magnitude of the dielectric polarization (dipole moment per unit volume) induced by a unit electric field, relative to vacuum. Through its direct link with the capacitance of a device, low relative dielectric constant semiconductor is preferable to minimize the dielectric losses (energy that goes into heating the dielectric material in a varying electric field). In this purpose, diamond, with almost half the relative dielectric constant of Si, offers a valuable device active area diminution when compared with silicon diodes of equivalent breakdown voltage withstand. Measurements over high frequency range (1 kHz - 20 GHz) further demonstrated that dielectric losses in diamond are almost negligible ($< 10^{-6}$

Table I.2: Key room temperature electronic properties of silicon (Si), silicon carbide (4H-SiC) and diamond [58–61]. Only a rough overall comparison is encouraged between the materials presented as most properties mentioned rely on doping levels, crystals quality and measurement or calculation technique.

	Si	4H-SiC	Diamond
Bandgap E_G (eV)	1.12	3.26	5.47
Critical electric field E_c (MV/cm) [a]	0.3	2.8	10
Electron mobility μ_e (cm^2/V.s) [a]	1500	1000	1060
Hole mobility μ_h (cm^2/V.s) [a]	480	120	2100
Electron saturation drift velocity v_e^{sat} (10^7 cm/s)	1.1	1.9	2.7
Hole saturation drift velocity v_h^{sat} (10^7 cm/s)	0.8	1.2	1.4
Relative dielectric constant ε_r	11.9	9.8	5.7
Intrinsic resistivity (Ω/cm) ρ_{int}	10^3	10^9	10^{16}
Relative JFOM	1	260	6600
Relative KFOM	1	6.8	32

[a] Doping and temperature dependent.

to 10^{-2}) [67–69]. A valuable property for noise level reduction in readout electronics, where diamonds detectors are promised to a successful future.

The critical electric field and mobility of diamonds, which can be intentionally adjusted through impurity incorporation, deserve a particular focus within the scope of this thesis, thoroughly explored in upcoming sections II.3.1.b. All electrical properties, presented in table I.2, can be amalgamated within the framework of "figure of merits" (FOM). Noticeably, Johnson [70] proposed a relation (JFOM) between operating power and frequency in transistors to predict their performance limitation under quickly repeated high power load:

$$JFOM = \left[\frac{E_c v^{sat}}{2\pi}\right]^2 \tag{I.3}$$

Couple years later, Keyes [71] developed a figure of merit (KFOM) that takes into account the thermal limitation of the material on the high frequency performances of the devices. In completion to the JFOM, it assesses the potential of material for use in integrated circuits, and is expressed as:

$$KFOM = \lambda_{th}\sqrt{\frac{cv^{sat}}{2\pi\varepsilon_r}} \tag{I.4}$$

where λ_{th} is the diamond thermal conductivity (developed in the next section) and c the speed of light. Despite the high values obtained with both JFOM and KFOM, indicating that, theoretically, diamond could be 32 times less thermally limited than silicon under high frequency power loads, diamond has not yet satisfied the potential which these results appear to suggest. These FOM should be treated with caution and serve mainly to demonstrate the as yet undeveloped potential of diamond in high-frequency, high-power-density applications.

Diamond disposes of a unique physical and electronic properties combination: high critical electric field, low relative dielectric permittivity, such as comparable electron and hole mobility, unlike other semiconductor materials where conduction is dominated by electrons. The key word here is "combination". If each individual physical property is selected for comparison, there are other materials which have superior values of such a property. For example, the room temperature electron mobility of 1060 $cm^2/V.s$ is lower than that of Si (1500 $cm^2/V.s$) and far less than InSb ($\approx$ 80000 $cm^2/V.s$). However, it is not in the same niche of specific applications that diamond is destined to be used, and taking into account the technological limitations of current manufacturing processes and anticipated performance, hole conduction holds more relevance for diamond. Nevertheless, no other material is comparable to diamond when compared in terms of the combination of mechanical, thermal, electrical, optical, and chemical properties. These combined properties make diamond an exceptional candidate semiconductor for high temperature, high power, high frequency, and harsh environment applications.

I.1.7 Thermal conductivity

As integrated circuit clock speeds and power densities increase, while package footprints and chip-set surfaces decrease, the heat generated in most electronic devices increase. Over the past decades the computing power has increased, more or less following the Moore's law, and therefore thermal management has become a major consideration. A heat spreader attached to integrated circuits, efficiently lower the operating temperature of the chip, ensuring optimal operating environment for the devices and, at the same time, more effective control of the life-cycle of these same components. Diamond placed itself as the most attractive candidate for this application thanks to its extremely high thermal conductivity (23 $W.cm^{-1}.K^{-1}$) - at almost up to six times greater than that of copper (4 $W.cm^{-1}.K^{-1}$), diamond possesses the highest known thermal conductivity value at room temperature.

Debye modelisation [72] implies that diamond is devoid of free electrons up to high temperature, in the range of the Debye temperature. As a consequence, almost all the heat or thermal energy imposed to diamond gems, is transferred by phonons within the crystal lattice. Coupled to the fact that carbon atoms are small, light-weighted, tightly and isotropically bonded to each other, the allowed phononic vibrational modes are highly energetic, or occur at high frequencies (up to 40 THz). Ultimately, high-energy phonon are able to carry more heat and, at RT, few atomic vibrations are present to impede the passage of thermal waves hence, thermal conductivity is unusually very high. Further consideration of the Boltzmann-Peierls modelisation, allow description of the evolution of the phonons distribution function in diamond, giving rise to its low thermal expansion coefficient or its low heat capacity.

The huge decrease in cost of lab-grown diamond over the past decade, has helped its conceptualisation as heat spreader over other possible materials. Progresses have been made concerning growth conditions, allowing diamond to be used as coating [74, 75] and placed as close as possible to the devices active area. While diamond coatings can effectively cover both planar and three-dimensional objects, challenges exist in terms of bonding adaptation. Excessive thermal conductivity at interfaces, due to poor interface quality, remains a primary concern. For this purpose, bulk mono-crystalline diamond, often combined with buffer layers, is preferred and has demonstrated superior heat management capabilities. This is enlightened in the work of Ohki et al. [73], as depicted in Fig. I.5. The utilization of monolithic diamond heat spreaders has the potential to address the thermal management issues associated with other ultra-wide bandgap semiconductors (UWBGs), more commonly used in power transistors (Si $\approx$ 0.15 $W.cm^{-1}.K^{-1}$; GaN $\approx$ 0.25 $W.cm^{-1}.K^{-1}$; 4H-SiC $\approx$ 0.37 $W.cm^{-1}.K^{-1}$), where high power operation can be limited by devices overheating. In applications demanding high power handling and management, power components fabricated entirely from diamond are a compelling choice. Already able to operate at high temperature ($>$ 423 K) [76], diamond based transistors are one of the most promising candidates for future power electronic applications. Diamonds used for heat spreaders have also proved beneficial for use with high-power thin light-emitting diodes [77] or even as heat-spreading coating for laser cavity mirrors [78]. Both of these applications additionally benefit from the exceptional optical properties of diamond, which will be discussed in the following section.

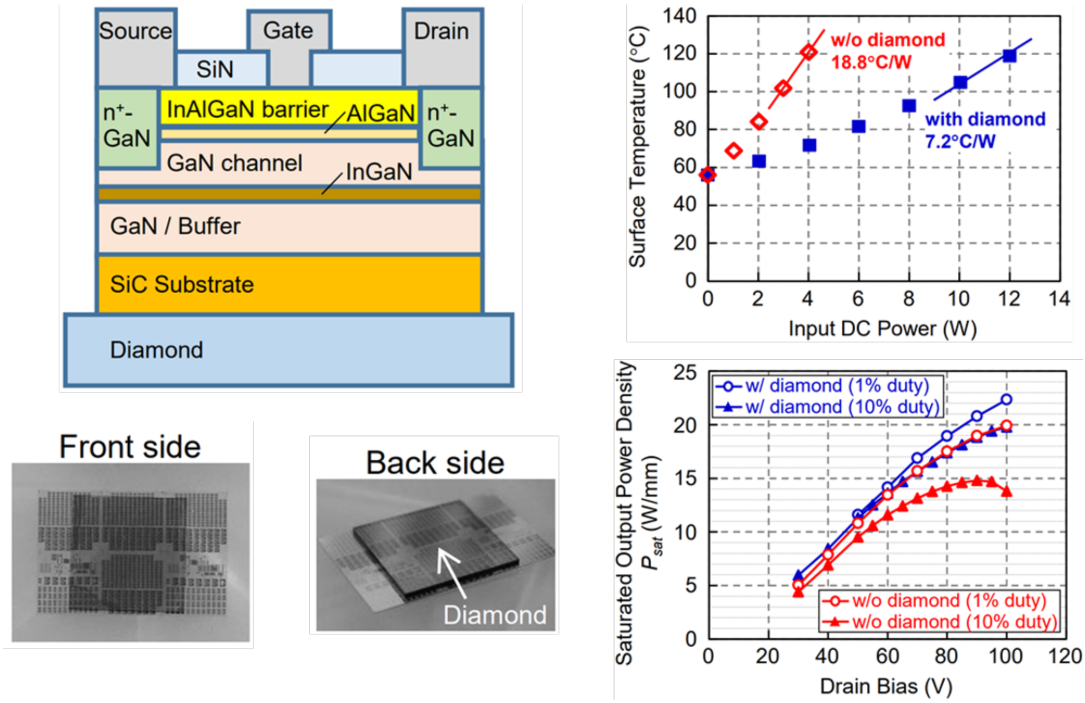

Figure I.5: Left, schematic cross-sectional view and photographs of InAlGaN/GaN HEMT on a SiC substrate bonded to a diamond heat spreader by the surface activated bonding method. Right, correlation between (top) surface temperature and input power measured by an infrared camera and (bottom) saturated output power and drain bias evaluated by load-pull measurement. Graphs taken from [73].

I.1.8 Optical properties

In the preceding sections, properties of intrinsic diamond have been explored, but crystalline defects such as impurities or dislocations, have not been introduced so far. It's essential to note that naturally occurring intrinsic diamonds are non-existent, as impurities incorporated during their formation alter the lattice symmetry and ultimately affect their optical transparency. Nevertheless, lab-grown diamonds, benefiting from better control over impurity integration during growth, have more recently demonstrated the ability to approach the qualities of intrinsic diamonds. The presence of diverse non-carbon species in the lattice can significantly impact the electromagnetic absorption spectrum of diamond. Historically, monocrystalline diamonds have been categorized by their principal defect's optical absorption signature, making this section the ideal context for such an exploration.

I.1.8.a Intrinsic diamond

In an intrinsic diamond lattice, as no allowed states exist within the indirect bandgap, no electron can interact with electromagnetic radiation with energies lower than the bandgap value of 5.47 eV. However, phononic modes sub-exist below the bandgap energy, and electromagnetic radiation can be absorbed by the crystal in a form of so-called vibrational absorption (or vibronic absorption). Thanks to the huge energy scale of diamond, the energy difference between the edge absorption (indirect bandgap) and vibrational absorption, is sufficiently large to make it transparent from the ultraviolet (UV) to the infrared (IR), covering the full visible region (400-800 nm). The absorption spectrum of high quality single crystal diamond is shown in Fig. I.6.

There is no one-phonon absorption in pure, defect-free diamond (which would appear around 0.16 eV - 7.5 μm) [80], as also for other mono-atomic crystals with inversion symmetry such

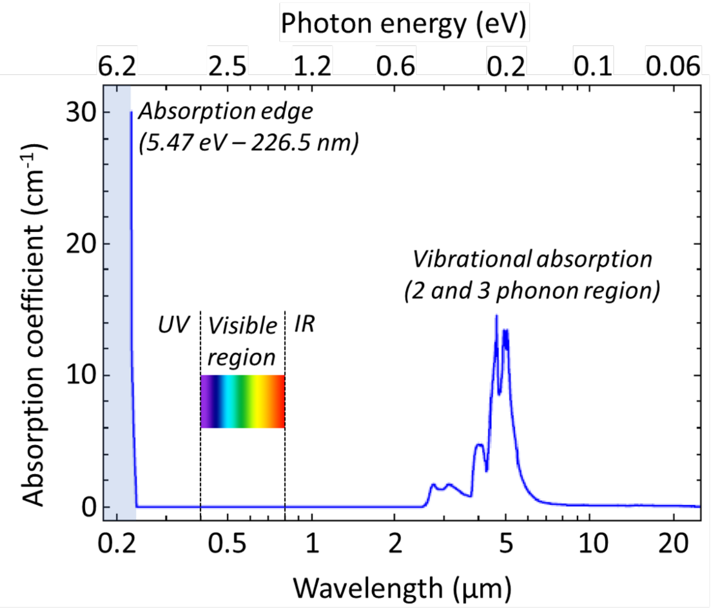

Figure I.6: Absorption spectrum of intrinsic diamond, taken and modified from [79]

as Si. The movement of nuclei in vibrational modes of the lattice are countered by equal and opposite movement of neighbors (π out of phase), so that no dipole moment for coupling with radiation can be induced, ultimately rendering the one-phonon absorption impossible in intrinsic diamond. However, dipole moments may also be induced in the crystal via interaction of the incident photon with more than one phonon, although with reduced oscillator strength; originating of lattice vibrational absorption in pure diamond between 0.47 eV (2.6 μm) and 0.19 eV (6.2 μm). From a classical viewpoint, the absorption mechanism can be qualitatively understood as one phonon inducing a net charge on atoms, and a second phonon (or more) vibrating the induced charge to create a dipole moment [81, 82].

Thanks to its ultra-wide bandgap and lacks of first-order infrared absorption, diamond is one of the most broadly transmitting solids. Coupled to its inner hardness, diamonds are highly desirable material for a variety of optical lenses including the operation under high thermal load or harsh environmental conditions [83–85]. Due to its transparency in the visible range, particle detectors made of high purity diamond are solar-blind, hence no light-tight packaging or screening is needed to ensure visible light insulation from UV detection [86, 87]. For these applications, high diamond purity is required as any polluting absorption occurring at energy lower than the bandgap, witnesses of the presence of a defect within the lattice. It introduces additional states into the band gap where one-phonon absorption may proceed by spoiling the local symmetry.

I.1.8.b Main optical impurity in diamond, through color classification

Less than a century ago, in 1934, Robertson et al. mentioned for the first time that there appeared to be "Two types of diamond" [88]. Based upon deep ultraviolet absorption spectra, statistics made on a gemstone batch of 200 to 300 elements, revealed that majority of diamond were opaque at wavelengths shorter than about 300 nm, while a few of them were transparent down to a wavelength of 225 nm. This differentiation ultimately gave rise to the type I and type II classification system where, subsequent research unveiled that the variance in absorption properties could be attributed to the substantial presence of nitrogen in type I diamonds.

Over time, this classification system has evolved further (see Fig. I.7) as our understanding of the various nitrogen positions within the diamond crystal lattice and the diverse interactions

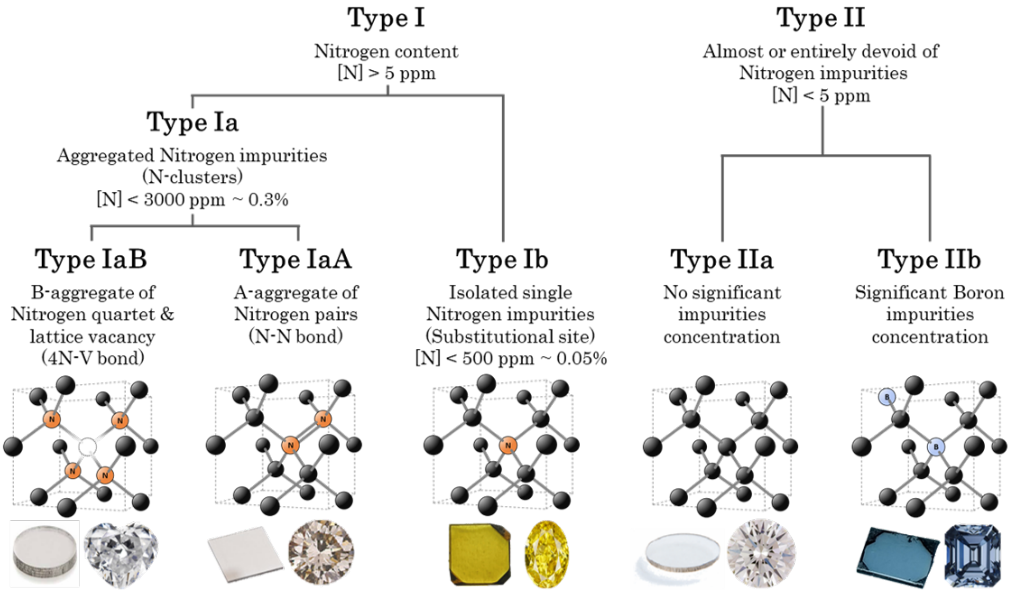

Figure I.7: Different monocrystalline diamond types classification

associated with it has deepened. Type la diamond, containing either or both of the A and B centres, vary from colourless to a yellow/brown colour. While A-center (or -aggregate) refers to di-nitrogen or nitrogen dimer, substituting two neighbouring carbon atoms, the B-center refers to four adjacent substitutional nitrogen atoms surrounding a vacancy (4N+V). Concerning type Ib diamonds, their high single-substitutional nitrogen contents gives them a yellow/orange (rusty) colour. Lastly, the purest type of diamond, type IIa, previously presented as intrinsic are colourless, whereas type IIb, which exhibit significant boron concentration, range from colourless to deep blue.

I.1.8.c Optical signature of impurities

Typical visible-ultraviolet and infra-red absorption spectra of intrinsic, type I and type II diamonds are reproduced in Fig. I.8. It is important to note that many of the spectra presented depend on impurity concentrations or crystal quality, thus only a rough overall comparison is encouraged between the different diamond types.

While intrinsic diamond (type IIa) has an absorption edge at the bandgap energy of 5.47 eV (226.5 nm), type IaA diamonds, containing A-centres, reduced the ultraviolet absorption threshold to an energy of about 4 eV (300 nm). This "secondary absorption edge" has been shown to be strongly correlated to the IR bands in the one-phonon absorption region (7.5 - 10 μm) [90], especially the most prominent IR peak at 159 meV (1282 cm-1) linked with LO phonons at the L symmetry point [91]. As no photo-conductivity could have been efficiently linked with these defects, "the secondary absorption edge" has been correlated to internal transitions at the A centre, rather than to transitions into the conduction band [92]. Similarly, the B-aggregate, has a slightly increased (or broader) absorption in the ultraviolet, but also a shifted absorption edge when compared to intrinsic diamond. It also exhibits broader and stronger infra-red features, than those which occurred due to the A aggregate. The distinctive features of the one-phonon absorption due to the B aggregates are a spike of intensity at the Raman energy 165 meV (1332 cm^{-1}) and a maximum at 145 meV (1175 cm^{-1}). However, as this centre is difficult to obtain in isolation (often coupled with the A band or a mix between the two configuration reported in Fig. I.7), there is a lack of data concerning its attribution to any phononic mode [92, 93]. Photo-conductivity thanks to the B-aggregates has also never been proven, hence shift of the absorption edge has been attributed to internal transitions at the B centre.

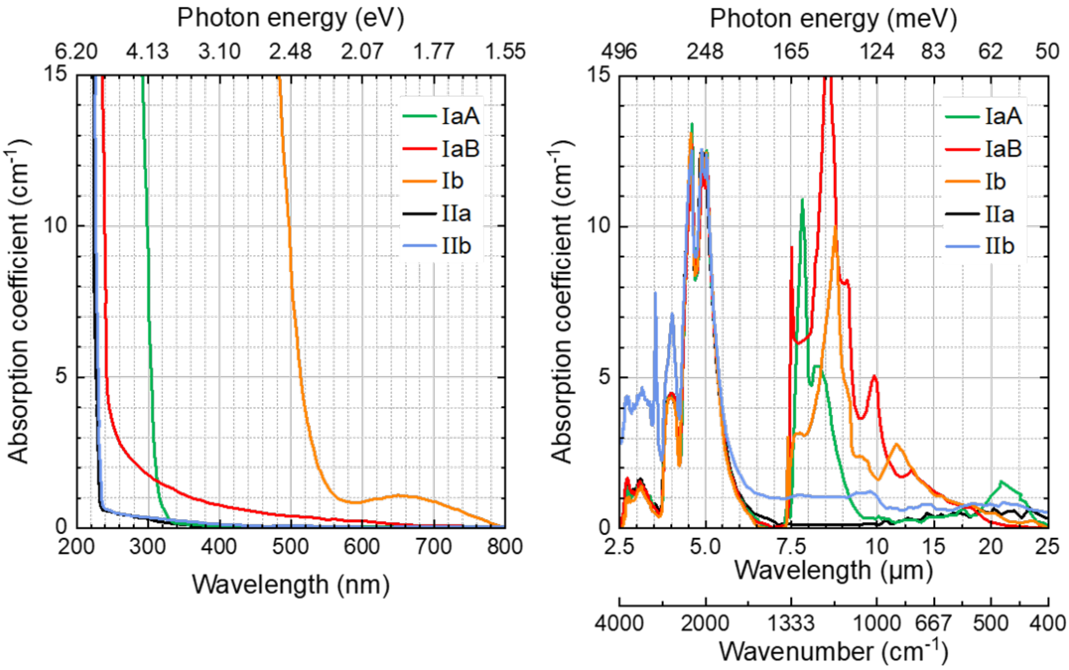

Figure I.8: Typical visible-UV and IR absorption spectra of intrinsic diamond (type IIa) and diamond containing A centres (type IaA), B centres (type IaB), single-substitutional nitrogen (type Ib) and boron (type IIA). Data taken from [89] for an arbitrary impurity concentration and crystal quality.

Type Ib diamonds also show additional infrared features but the most noticeable difference is the strong absorption in the visible and near-ultraviolet. Nitrogen, being a group V element, acts as a donor in diamond lattice when placed in substitution of a carbon atom. Thermo-electrical measurement revealed that the donor level formed is deep inside the gap, with a thermal activation energy of 1.7 eV [94], whereas the optical threshold has been found at 2.2 eV [95]. The energy shift between the two measurements is a consequence of the Jahn-Teller effect in diamond [96, 97], where substitutional nitrogen with its affiliated degenerate electronic energy levels distort the lattice in order to lift the degeneracy and lower its energy. Oppositely to its aggregated forms, single substitutional nitrogen UV absorption is due to transitions into the conduction band from its localized energy states within the bandgap [98]. Transitions that do not involve phonon are commonly mentioned as zero phonon lines (ZPL) and feature sharp absorption peaks, whereas broadened UV-absorption bands, coupled to IR sharp peaks, are common feature of vibronic absorption.

Oppositely to Ib diamonds, type IIb diamonds only exhibit broadened and low IR absorption coefficient in the one-phonon region, but introduced additional features in the multi-phonon region (2.6 - 6.2 μm), without introducing absorption changes in the UV-visible spectrum compared to intrinsic diamond. Substitutional boron atoms in diamond lattice have been proven to act as acceptor, with a ground state about 370 meV above the valence band [99]. As boron is much less steric than nitrogen, compared with carbon, the Jahn-Teller effect is not observed in the energy configuration of boron and so the optical and thermal activation energies are identical. While the three peaks at 307, 346 and 363 meV have been recognized as bound-state transitions, the continuum starting at 370 meV and extending toward visible range has been correlated to ionisation of the centre leading to photo-conductivity [99].

I.2 Supplying diamonds suited for every leading-edge technology

Diamond, renowned for its exceptional properties, stands as a promising candidate for a wide range of emerging technologies, from high-power electronics to advanced optical devices. However, harnessing diamond's full potential in these applications requires a careful consideration of its production and purity. This section delves into the intricacies of supplying diamonds that are tailored to meet the specific requirements of leading-edge technologies. From the controlled growth of lab-grown diamonds to the management of impurities, we explore the crucial factors that make diamond not just a gem of nature but a gem of technology.

I.2.1 Synthesis of mono-crystalline diamond

I.2.1.a High-pressure high-temperature (HPHT) synthesis

The initial synthesis of diamond can be traced back to 1955 when the High Pressure High Temperature (HPHT) method was first introduced [23]. Remarkably, this method is mimicking natural formation conditions of diamonds remains the primary approach for producing diamond substrates. It operates through the utilization of belt press systems that exert pressures exceeding 5 GPa, accompanied by temperatures of at least 1800 K. These conditions are applied to a sp^2 carbon source in order to reach the phase change to sp^3 diamond, significantly catalyzed by the presence of a diamond seed. What ensues is the growth of diamond, simultaneously expanding along multiple crystallographic directions, as schematized in Fig I.9 asides with carbon phase diagram enlightening preferential growth conditions. The most stable orientations of HPHT diamond crystals, known as facets, include (100), (110), (111), and (113), whereas large mono-sector are more easily obtained with (100) orientation.

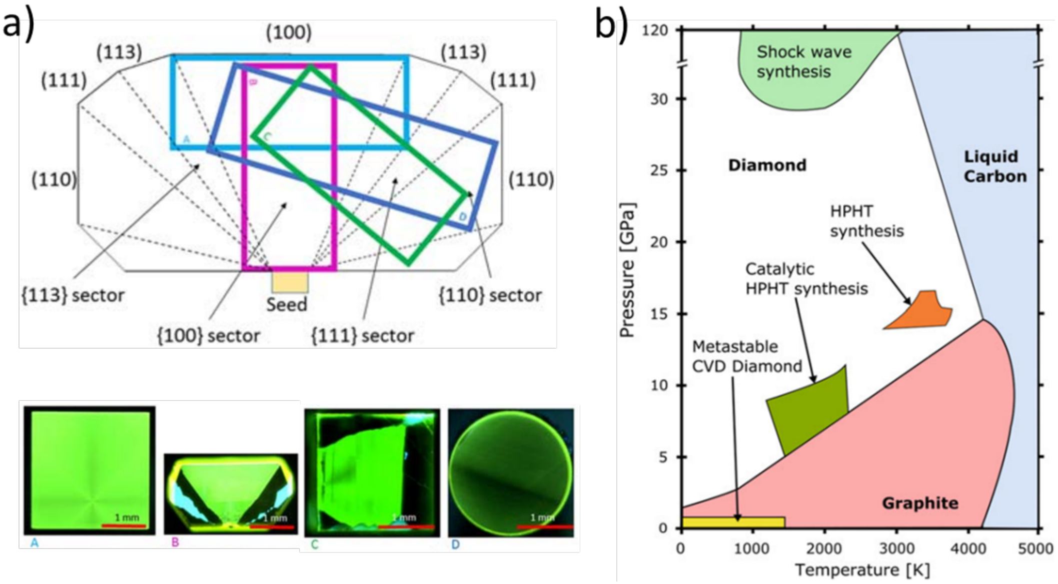

Figure I.9: a) Scheme of a typical cuboctahedral HPHT substrate obtained from a diamond seed. Crystallographic directions are reported as well as the position where (100)-, (110)-, (111)-, and (113)-oriented plates have been sliced (light blue, pink, green, and dark blue rectangles, respectively), prior to their photo-luminescence observation. Graph taken from [100]. b) Phase diagram of carbon, enlightening the different diamond synthesis techniques. Graph taken from [101], modified from [102].

Type IIb, HPHT-grown diamonds, has been used as active layers for the fabrication of vertical devices, but their higher resistivity compared to metallic CVD-grown heavily doped diamond (p-type), limits their uses to application where the current is not a key factor [103]. In the concern of type IIa diamonds grown by HPHT, they are not purely intrinsic and commonly display a p-type character with boron concentration $[B] \leq 10^{15}$ cm^{-3}. They are less available commercially but of great interest for achieving vertical transistors and/or Schottky diodes regarding their superior crystallographic quality. However, HPHT growth excels in the synthesis of high crystallographic quality type Ib diamonds, by providing lower dislocation density substrates compared to CVD-growth. The most common source of nitrogen in HPHT process is the air that present in pores of high pressure cell during its assembly [104]. However, the N-content present in the growth medium, and therefore in the resulting HPHT diamonds, can be controlled over a wide range by judicious addition of a suitable catalyst. While titanium or aluminium powders act as nitrogen getter in the growth chamber, allowing minimal nitrogen concentration of ≤ 1 ppm [105], nitride-based catalyst (NaN_3 or P_3N_5) gives access to higher N-content, up to 1000 ppm [77]. There is strong demand for these Ib substrates, because of their insulating properties provided by deep nitrogen donors, which is a factor of interest for lateral transistors and pseudo-vertical Schottky diodes [106] coupled to their superior quality.

I.2.1.b Diamond chemical vapor deposition (CVD)

The idea of creating diamonds by adding carbon atoms one by one, leading to a tetrahedrally bonded carbon structure, brought about an obvious advantage in terms of equipment and energy costs than traditional HPHT methods. Early experiments in the late 1950s and 1960s attempted to grow diamonds on natural diamond surfaces through the thermal decomposition of carbon-containing gases at 1100 K under reduced pressure [107, 108]. However, the growth rate was slow, and impure mixed phases, including graphite, were often deposited alongside the diamonds. A breakthrough occurred in the late 1960s when researchers discovered that introducing atomic hydrogen during the deposition process could selectively, and preferentially, etch graphite, leaving behind pure diamond [109, 110]. This chemical vapor deposition (CVD) technique was further developed, allowing diamond growth on non-diamond substrates [111], leading to the so-called hetero-epitaxy, a really promising discovery for diamond substrate cost reduction. In 1982, Matsumoto et al. established a “hot filament reactor” for growing high-quality diamond films on non-diamond substrates at significant rates [112, 113]. The following year, they introduced another method using a microwave plasma (MP) reactor, nowadays qualified with their institute name “National Institute for Research in Inorganic Materials” (NIRIM), more detailled in [114, 115]. Alongside the NIRIM reactor architecture, the commercially available “ASTEX-type” CVD reactors, depicted in Fig. I.10, are the most common reactors architecture used for CVD monocrystalline diamond homo-epitaxial growth. CVD diamond current control in layers thickness, doping level, and wider doping range than HPHT, make this technique the core of electronic-grade diamond doped active layers fabrication, driving ongoing research and development in both academic and industrial diamond-based devices.

While each growth method differs concerning the activation of gas phase containing carbon precursor molecules (e.g. hot filament, MP, DC arc jet or plasma torch), they all share a few features in common: the precursor gas (usually methane, CH_4) is diluted in excess of hydrogen, in a typical mixing ratio of 1-15 % volume CH_4, and the substrate temperature being usually greater than 900 K to ensure the formation of diamond rather than amorphous carbon. The scheme provided in Fig. I.11 shows a simplified version of the diamond homo-epitaxial CVD chemistry, whereas in depth complementary information can be found elsewhere [118, 119].

In the precise case of (MP)CVD, especially inside the plasma, the process begins by dissociating di-hydrogen (H_2) molecules into hydrogen (H) atoms, which interact with the diamond surface to create active sites or hydrogenate it, as illustrated in Fig. I.11 (i) and (ii). After surface activation reaches a kinetic equilibrium, methane is introduced into the gas mixture. In the plasma, methane reacts with hydrogen atoms to form CH_3 groups and H_2 molecules, allowing the former CH_3 groups to be further bonded to active sites on the diamond surface, as depicted

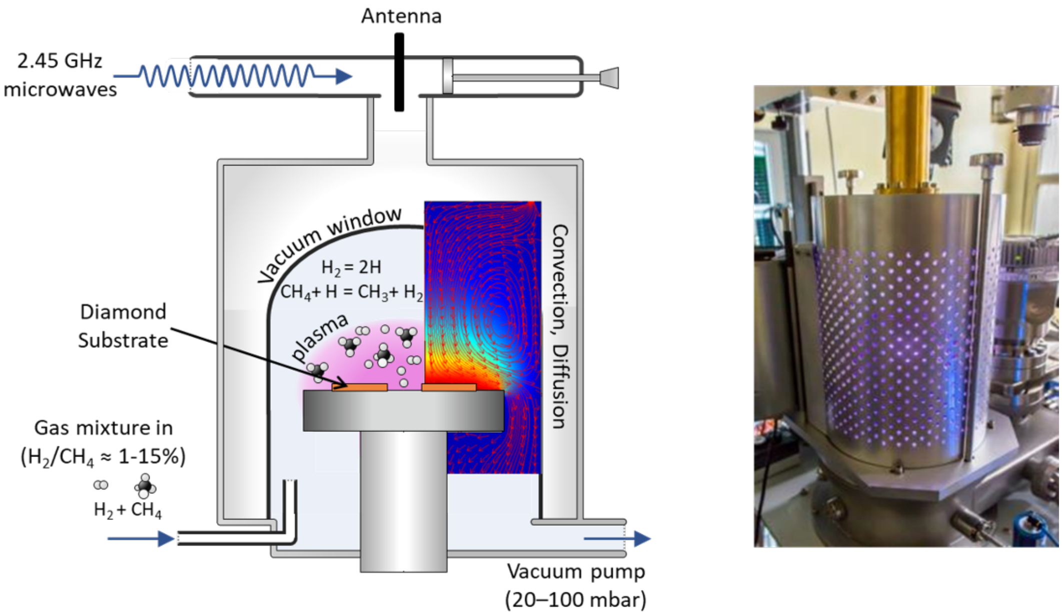

Figure I.10: Schematic diagram of ASTEX-type (MP)CVD reactor with picture of a commercially available Plassys reactor. Courtesy to D. Eon [116] and J. Letellier [117]

in Fig. I.11 (iii) and (iv). Once bonded, H atoms can react with bonded CH_3 groups, leaving CH_2 groups attached to the diamond surface and releasing molecular hydrogen as a byproduct (refer to Fig. I.11 (v) and (vi)). The same chemical reaction subsequently happens where, another hydrogen atom can react with the CH_2 group, liberating di-hydrogen and ultimately incorporating the carbon into a new diamond layer (see Fig. I.11 (vii) and (viii)). New active sites can be again created by the hydrogen atoms allowing the process to go on in a cycle as long as required [119].

Along the whole process, hydrogen play multiple role: sp^3 surface termination preventing sp^2 graphitic lattice reconstruction of the surface, or sp^2 graphitic phase etcher. As atomic hydrogen etch graphitic sp^2 carbon many times faster than diamond like sp^3 carbon, diamond growth could thus be considered as five steps forward, but four steps back, with the net result being a slow build-up of diamond. The growth rate varies from 1 to 150 μm/h, depending on the pressure and the gases mixture used. Noticeably, inclusion of oxygen in the gas mixture has been reported to reduce defect formation by enhancing hydrogen etching of amorphous carbon. Oxygen may also act as an etchant itself and improve the reaction of CH_3 with the surface, particularly during initial growth stages, ultimately increasing the growth rate [120]. The last advantages offered by (MP)CVD is its reproducibility concerning diamond doping control. Main diamond dopants can be introduced during (MP)CVD by the addition in the gas mixture of a molecular precursor, but this precise feature will be more detailled in a further section.

I.2.1.c Wafer availability: diamond road-map to large-scale devices and substrates

Previously presented diamond growth techniques (CVD and HPHT) were roughly compared, but for their uses in power devices fabrication, HPHT substrate are preferred for their high crystalline quality, whereas CVD growth offers many more advantages and reproducibility in terms of active layer production (thickness and doping). Both techniques are used, or ignored, depending on the advantages and disadvantages they offer, but they share a common interest that is crucial to the future development of diamond power components, which is currently greatly lacking in terms of industrialisation: the growth of large scale wafers.

Commercially available mono-crystalline substrates, produced through either CVD or HPHT

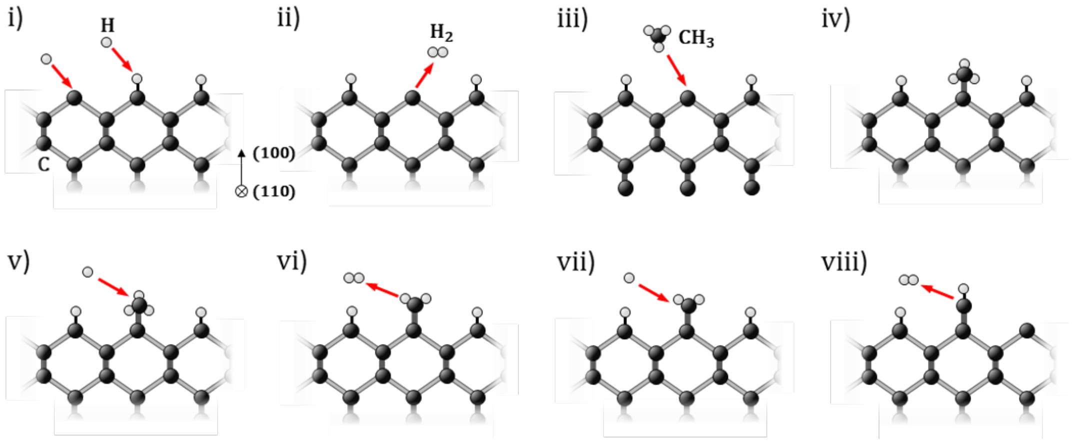

Figure I.11: Schematic process for diamond MPCVD epitaxy based on the representation of [59, 118]

methods, offer sizes of up to 4 mm and 10 mm radii, with dislocation densities ranging from 10^6 to 10^2 cm^{-2}. Of these, HPHT electronic-grade wafers are primarily employed in device development, by mean of their larger size and better qualities. While HPHT technology is prepared for 2" wafer production, the absence of a current market for such substrates has led to a counterproductive feedback loop. This results from limitations in substrate quality, reproducibility, and size that restrict device capabilities and prospects, consequently discouraging investments in expanding wafer sizes and enhancing quality. To break this detrimental cycle, there is a pressing need to manufacture devices that surpass the limitations of silicon and SiC devices, thereby stimulating interest and investments. With improved performance and eventual widespread adoption, the diamond market, currently influenced by the gem industry (and gemstone pricing decoupled from market dynamics), will diverge into two distinct markets.

It is important to point that, up to now, most of the best diamond power devices ever realised, based on current density handling and breakdown field sustainability, have been fabricated upon small active area [61]. When normalised over effective volume of operation, current flow or breakdown field of diamond based power device have already demonstrated tremendous values. However, absolute current rating and breakdown voltage are still insufficient regarding the technical specifications of power component market. The reason being strongly correlated with substrate (and layers) non-homogeneity, either between different batches or within a standalone substrate, where compact devices design are less affected by probabilistic diamond defect occurrence [121]. Nevertheless, to cross-reference with the counterproductive feedback loop introduced in the previous paragraph, attempt at realisation of large-scale devices which exceeds the singular bar of sustaining 1 kV (OFF-state) and 1 A (ON-state) is an issue of major importance for diamond. Within this context, an inter-digited transistor architecture is proposed within this manuscript and detailed in the second chapter, with an adequate design in order to meet the aforementioned criteria.

From a growth perspective, various solutions are under development to reduce costs and increase the size of diamond wafers. These include mosaic wafers created through ion implantation, cleavage, and subsequent fusion via CVD growth, as demonstrated in reference [123], or the "smart-cut" process developed by CEA and CNRS [124–126]. Another approach involves hetero-epitaxy [127, 128], where CVD layers are grown on silicon, iridium, or sapphire substrates. Fig. I.12 provides an overview of the current state of diamond wafers, including their size, quality, cost, and future projections. These solutions hold significant promise and, if successful, could broaden the range of applications for diamond by reducing its production costs. However, substantial advancements are still required to enhance crystalline quality and reproducibility.

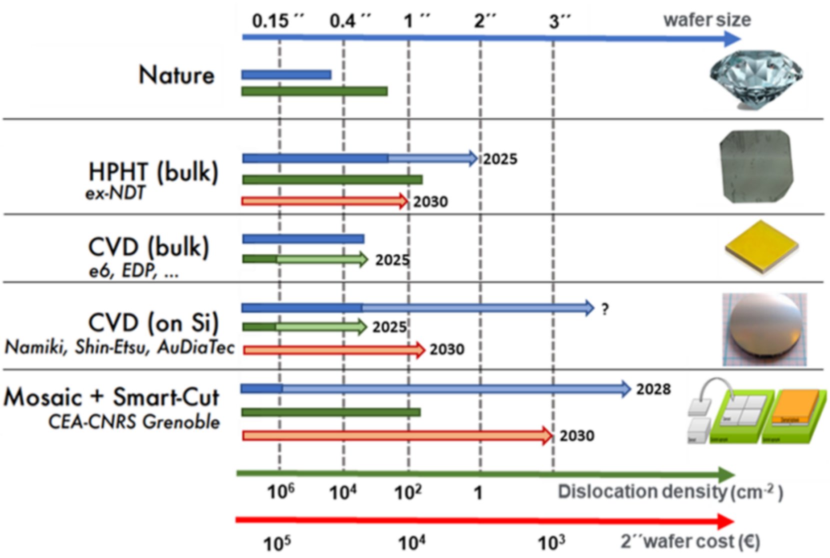

Figure I.12: Diamond wafer classified through their growth technique along with their actual and expected future projection: size, dislocation density and cost. Graph presented in [122], available elsewhere [59].

I.2.2 Diamond doping, from gemstone to conductive material

I.2.2.a Main diamond dopants

Boron, nitrogen, and phosphorus stand out as the only prevalent dopants in diamond, each playing a distinct role in its electrical properties. Doped diamonds are distinguishable to other materials employed for power electronic applications, like Si and 4H-SiC, due to its deeper ionization energies, as schematized in Fig. I.13.

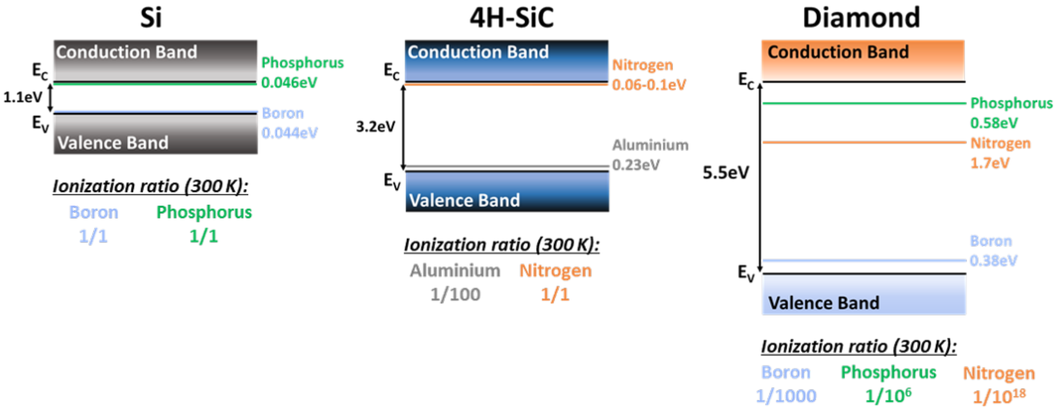

Figure I.13: Schematic band diagram enlightening the ionization energies of the dopants for Si, 4H-SiC and diamond for both donors (n-type) and acceptors (p-type). Ionization ratio, at RT, are also presented but, only a rough overall comparison is encouraged between the materials presented as it relies on doping levels.

Among these, boron, primarily employed for p-type doping, has been extensively studied and holds a unique position. It possesses the lowest ionization energy of effective diamond dopants, measured at 0.37 eV [129]. This characteristic poses a challenge, as boron-doped diamond, even being the shallower known dopants for diamond, experiences partial ionization at room temperature. As comparison, at RT and for low doping level ($N_A \leq 10^{17}$ cm^{-3}), almost 100 % of boron dopants are ionized in silicon, whereas for diamond only 0.1 % are thermally ionized. However, there are benefits for diamond to operate at high temperature and high power loads, where thermal losses successfully participate in mitigating the partial ionization. In most semiconductors, a temperature increase over RT degrades the resistivity ρ, due to the decreasing mobility μ as phonon interaction becomes stronger:

$$\rho(T, N_A, N_D) = \frac{1}{q \cdot [\mu_p(T, N_A, N_D) \cdot p(T, N_A, N_D) + \mu_n(T, N_A, N_D) \cdot n(T, N_A, N_D)]} \tag{I.5}$$

The 1D electrical resistivity mentioned above is influenced by the inverse proportionality to the concentrations of free electrons (n) and holes (p). These concentrations, along with their mobility, are subject to variations based on factors such as dopant(s) (N_A for p-type and N_D for n-type), compensation (respectively N_D for p-type and N_A for n-type), temperature, and the injection mechanisms, whether being bipolar or unipolar. Besides geometrical considerations (shape, thickness l, area S, etc...) generally chosen to minimize the power devices series resistance ($R_S = \rho \times l/S$) and so favor high forward currents, the most important parameter to enhance the latter is to lower the semiconductor resistivity. Concerning boron-doped diamond, the optimal operating temperature hovers between 500 and 700 K (depending on doping level), where a balance between carrier mobility and concentration is reached [130]. At this threshold, p-diamond transcends every others competing materials for power electronics applications, or even at lower temperature like 350 K where boron-doped diamond ON-state resistivity is theoretically lower than nitrogen-doped SiC, for the same breakdown voltage withstand (hence doping level) [131].

Concerning n-type doping, it has been one of the most important research themes for diamond, since feasibility of the CVD growth. Among the group V elements, nitrogen can be the most favorable atom to be incorporated into diamond lattice because its atomic radius is close to carbon's. The fifth electron of this donor occupies an anti-bonding C-N orbital, thereby lengthening the corresponding bond. Therefore, isolated substitutional neutral nitrogen in diamond, goes slightly off-centre into the (111) directions [97], compared to its ideal tetrahedral coordination in the lattice. This small displacement imposes to substitutional nitrogen to form a deep donor state at 1.7 eV below the conduction band minimum, rendering RT conductivity without the mean of an external energy source (temperature or light) non-existent.

Also part of the group V elements, phosphorus, when placed in substitution of a carbon atom in diamond lattice, form a deep donor. Even if, the ionization energy of phosphorus has undergone debate, with values ranging from 0.43 to 0.63 eV [132, 133], two values seem to be more frequently reported in recent publications between 0.57 and 0.6 eV [134–136]. On the same basis than nitrogen, phosphorus is expected to be shifted from its ideal tetrahedral coordination in the diamond lattice, along the (111) direction, although no evidence of this behavior has been reported so far. Subsequently, no optical/thermal ionization energy splitting is considered for phosphorus doped diamond. While conductivity has been evidenced in phosphorous-doped diamond [137], the resistivity remains very high ($\approx 10^6$ Ω.cm), except for heavily doped layer where, the carrier transport mechanism shifts from band conduction to hopping conduction. When the phosphorus concentration exceeds 10^{20} cm^{-3}, the specific resistance at room temperature becomes lower than 10^2 Ω.cm through nearest-neighbor hopping conduction. From the viewpoint of the device active layer, higher carrier mobility achieved through light doping is preferable, whereas heavy doping is preferable for lower resistance including ohmic contact. However, it is important to consider the numerous issues faced in the concern of achieving controlled and reproducible phosphorous doping in diamond.

I.2.2.b Impurity incorporation efficiency during step-flow MPCVD

Available controlled doping for CVD diamond growth

Boron is the most controlled and reproducible diamond dopant up to date, especially through its incorporation by means of diborane (B_2H_6) or trymethylboron ($B(CH_3)_3$) during CVD process. A wide doping level range is accessible, from layers characterization technique lowest detection limit, $N_A \approx 10^{14}$-10^{15} cm^{-3}, to heavy boron concentration $N_A > 10^{21}$ cm^{-3}. For heavily doped layers, studies revealed a transition to a metallic state at approximately $3 - 4.5 \times 10^{20}$ cm^{-3} [138, 139] and a superconducting state at $5 - 7 \times 10^{20}$ cm^{-3}, particularly at low temperatures [139, 140]. While the ability to control doping levels and thickness has been well-established, it's worth noting that defects tend to impose limits on the maximum achievable high-quality thickness.

Phosphorus, today's best diamond n-type dopant, can be incorporated within the lattice thanks to the adding of phosphine (PH_3) during the CVD growth process. However, compared to boron, its doping efficiency, control such as its reproducibility is still one of the main issue, hence an active research field, regarding bipolar devices fabrication. It was theoretically predicted that phosphorous doping would not be an easy task due to the low phosphorous solubility in the diamond lattice [141]. Ion implantation has been proposed in a first place, as an effective solution through the non-equilibrium feature of the method but there was no convincing report on dopants activation, except in the recent work of E. Abubakr et al. [142]. They demonstrated an innovative laser-induced doping method, allowing phosphorous incorporation into an insulating monocrystalline diamond at ambient temperature and pressure conditions. In 1997, Koizumi et al. [133] succeeded in forming n-type, phosphorous-doped diamond thin films during the growth of (111)-oriented epitaxial layer, under well optimized CVD experimental conditions, allowing the achievement of high crystalline perfection. The incorporation is favoured in the (111) direction but has been also achieved in the (100) direction, couple years later [143]. The results were convincing successful n-type doping of diamond on (100) orientation applying unique growth conditions during CVD that was different from (111) case. Nevertheless, for (100)-oriented diamonds, the doping control is limited within 10^{18} to 10^{19} cm^{-3}, still far behind (111)-oriented results ranging from 10^{16} to 10^{21} cm^{-3}. Although, for (100)-oriented phosphorous-doped diamond, the Hall mobility is reported rather high [144] and it is hopeful to have better quality n-type diamond than (111)-oriented in the future. However, heavily doped layers are predominantly available in the (111) direction so far.

Step-flow growth mechanism and doping efficiency

As mentioned herein-above, growth conditions must be adapted, both for boron and phosphorous doping, depending on the substrate crystalline orientation. Specifically, gas mixture, gas flow rate and pressure such as micro-wave input power in the case of (MP)CVD, as the main grower-dependent parameters. Nevertheless, dopants incorporation efficiency, shared a common strong dependency to the substrate misorientation angle. Realisation of a perfectly (100)- or (111)-oriented substrate is highly challenging, whether the growth method used (CVD or HPHT), due to the atomic precision that would be required between the repeated cutting, polishing and atomic-scale characterization. Even if atomically-flat diamond have already been reported [145], they only concern small layer area, while most diamond substrates exhibit a mis-angle θ_{mis} regarding their vicinal growth orientation. Mis-angle up to a maximum of 5° are commonly achieved and give rise to a terrace-like diamond surface, depicted in Fig. I.14. Subsequently, two different growth mechanisms may be favoured or disadvantaged, through the grower-dependent parameters tuning: island growth, where nucleation happens at random sites and clusters grow in size (but also in number), or step-flow growth, in which nucleation happen into atomic step edges and growth happens perpendicular to the respective vicinal planes.

During step-flow growth, schematized in Fig. I.14, it exists a competition between dopants

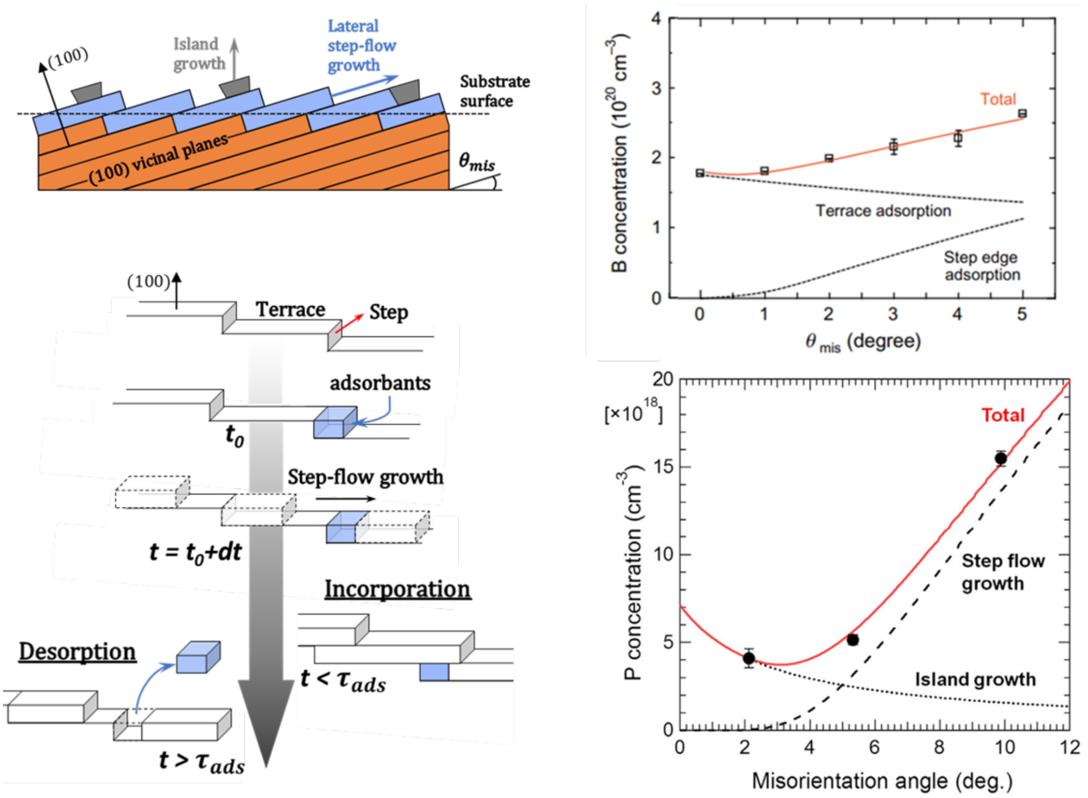

Figure I.14: Top left, schematic of step-flow accompanied with island growth, of diamond films on misoriented (100) surface. Bottom left, incorporation/desorption mechanisms of boron during step-flow growth. Right, incorporated boron (top) or phosphorous (bottom) concentration as function of the substrate misangle θ_{mis}, enlightening the competition of dopants adsorption between terrace (island growth) and step-edge sites (step-flow). Noticeably, data are reported for hot-filament (HF)CVD growth concerning boron, and plasma-enhanced (PE)CVD growth concerning phosphorous. This choice of representation purpose also comes from the lack of experimental data in this concern, although similar behavior has been reported concerning (MP)CVD [146, 147]. Graphs have been taken and modified from [148] for boron and schemes and from [149] for phosphorus.

incorporation and desorption along the growth duration. Step edge adsorption leads to incorporation when, the lifetime of a surface-bonded admolecules is greater than the time required to overgrow the former introduced dopant. Otherwise, desorption occurs and incorporation efficiency at the step edges is strongly reduced. This mechanism has been reported to be greatly promoted in the growth of boron doped diamond thanks to higher substrates misangles [148, 150], even in doped-layers where strong doping gradients have been used (delta-doped) [151].

Concerning phosphorous-doping, as being achieved with high quality by a few teams around the world, there is a lack of statistics concerning the reported impacts of substrate misangles. Furthermore, the (111)-oriented crystals, favoring phosphorus incorporation, have been extensively developed and, hence characterized in this sense compared to (100)-oriented crystals. The few reports made on (111)-oriented crystals, demonstrated that, the phosphorus incorporation concentration in the diamond lattice, increased with misangles decrease [152, 153]. However, in contrast to the tendency of phosphorus incorporation, the growth rate decreases with misangles decrease. This is considered to be related to step density lowering as the off angle decrease, resulting in a reduction of carbon adsorbing site on the surface. Alternatively this also could arise from the surface migration length of phosphorus admolecules being longer than that of hydrocarbon species, maximizing the phosphorus donor concentration of diamond with as large a terrace width of a (111)-substrate as possible [153]. On the contrary, the only study (to the author's knowledge) that gathered multiple mis-oriented and phosphorus-doped, (100)-diamond, evidenced that the phosphorus incorporation enhances with an increase in the substrate misorientation angle in spite of the same gas flow and plasma conditions [149]. Justified oppositely to (111)-oriented growth by, the decrease in terrace width with increasing misorientation angle. Both, the desorption time of adsorbed phosphorus atoms on the (100)-misoriented surface of the growing diamond film, and the time until the impurity is covered by a next coming over layer, have been demonstrated to be both one order of magnitude lower than for boron. However, like it was reported in the case of boron [148], a growth rate decrease is observed for increased mis-orientation, up to a limit around 10° (when reported).

To partially summarize about doped diamond (MP)CVD growth, thin active layers quality is strongly dependent on intrinsic properties of the substrate (like misangle and surface roughness). To get rid of this low, (but not without consequences), intrinsic variability, growing conditions can be adapted but it would require extensive and non-cost efficient sample preparation, for a non-guaranteed payout. However, the lateral devices fabricated within this thesis utilize a highly phosphorous-doped (100)-oriented layer, stacked beneath boron-doped layers, which is highly challenging to achieve. Subsequently, a particular attention is required on the intrinsic layer properties settled during CVD growth. As it rules the devices conduction and sustainability properties, by means of models presented throughout this chapter and the following one, characterisation of the grown layer is at the core of this manuscript.

I.2.2.c Incomplete ionization and carrier concentration

Ionization energy versus doping level

Before delving into the resistivity temperature dependence, it is valuable to examine the variation of acceptor ionization energy versus boron-doping density, as this characteristic significantly impacts hole concentration. Fig. I.15 represents the activation energy for boron and phosphorus as function of the impurity concentration as well as the experimental values reported in literature for CVD doping level range (10^{15} cm^{-3} $\leq N_{imp} \leq 10^{22}$ cm^{-3}).

For light boron doping levels, below 10^{19} cm^{-3}, the experimental ionization energy remains relatively constant, around 380 meV, corresponding to the difference between the fundamental boron acceptor level and the valence band maximum. However, as the doping level increases above this value, the ionization energy, E_A, decreases due to the overlapping of the acceptor wave functions, induced by the distance closering between dopants in the lattice. It allows hopping conduction, where holes localized on an acceptor localized state inside the bandgap, can tunnel towards nearby ionized acceptor states. Viewable as holes hopping from one site to another, this mechanism is strongly influenced by temperature, doping or compensation, favouring hopping between nearest neighbour states (NNH) or more distant states (variable range hopping - VRH). Coupled to band conduction, it further efficiently decreases the resistivity and needs to be accounted in heavily doped layer, up to the metal-insulator transition at $N_A = 3 \times 10^{20}$ cm^{-3} [138]. For doping levels exceeding this value, E_A is zero as the boron impurity band conduction merges with the valence band. In this metallic conduction regime, the resistivity significantly drops compared to the levels observed before the transition. Additionally, this resistivity exhibits almost no temperature dependence and metallic diamond layer are noticeably well-suited for creating low-resistivity ohmic contacts at the drain and source regions of diamond FET devices (detailled in section II.5). This dependence of the boron activation energy on the doping level, is well-represented by the empiric law proposed by Pearson and Bardeen [168]. With tailored parameters for boron-doped diamond it yields:

$$E_A = E_{A,0} - \alpha \times N_A^{1/3} \tag{I.6}$$

Where $E_{A,0} = 0.38$ eV refers to the boron ionization energy at low doping level and the prefactor $\alpha = 5.5 \times 10^{-8}$ (eV.cm) is a fitting parameter adjusted to obtain the metal-insulator

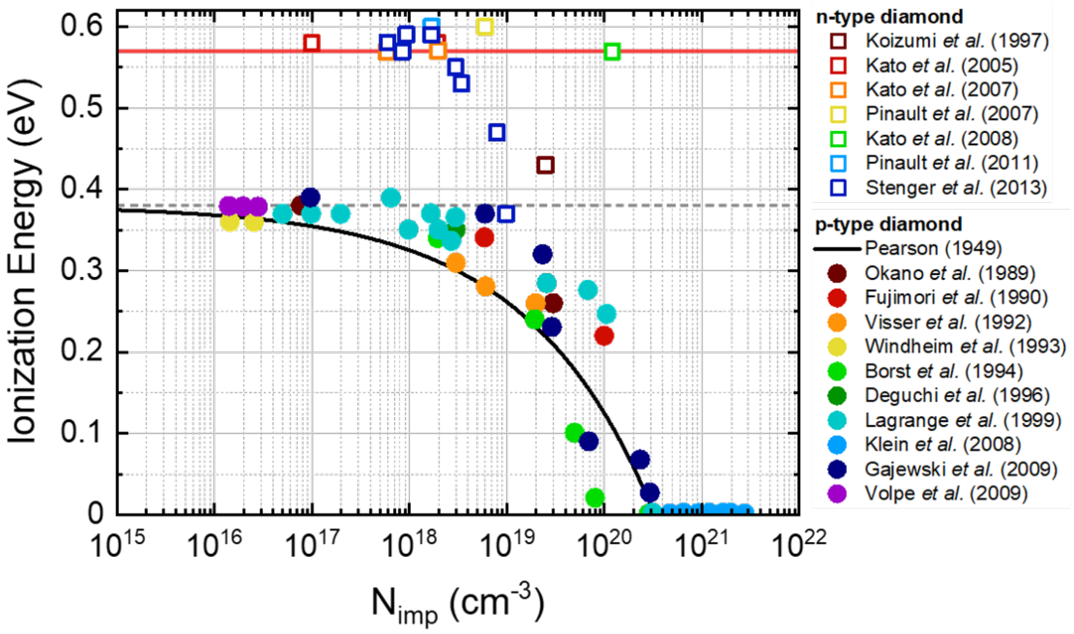

Figure I.15: Activation energy as a function of the acceptor density for p-type and donor density for n-type diamond. Figure inspired from [154], updated with metal-insulator transition from [138], where experimental value are reported for boron [139, 155–163] and for phosphorus [133, 134, 143, 164–167]. Solid black line for p-type is a fitting curve following Pearson and Bardeen model [168] whereas for n-type activation energy, a constant value (0.57 eV) was assumed.

transition at 3×10^{20} cm^{-3}. While literature often refers to a metal-insulator transition at 4.5×10^{20} cm^{-3}, a more recent study has revisited the phase diagram of boron doped layer [138], where mesa patterns minimizing the parasitic currents induced by doping inhomogeneities, have been used to unveil the presence of a metallic transition at 3×10^{20} cm^{-3}. Hence, the prefactor $\alpha = 5.5 \times 10^{-8}$, adjusted to the later mentioned insulator-metal transition should be preferred.

Concerning phosphorus donors, a constant ionization energy of $E_D = 0.57$ eV has been commonly assumed over the doping range available (10^{16} $cm^{-3} \leq N_A \leq 10^{20}$ cm^{-3}). The fact that this value has been reported only a few times in literature, linked to the successful achievement of phosphorus-doped diamond for few teams around the world, provide a lack of statistics about the potential lowering of E_D with doping level increase. The lowest value, $E_D = 0.43$ eV, obtained by the precursor work of Koizumi et al. [133] was underestimated because the temperature dependence of carrier concentration, including the influences of hopping conductivity due to heavy doping level ($N_D \geq 10^{19}$ cm^{-3}) and also crystalline defects, were omitted. Further films characterization demonstrated the strong impact of hopping conduction mechanism in phosphorus-doped diamond, to such an extent that it becomes predominant over band conduction at room temperature [169–171]. The activation energy has been revised by further Hall measurements of higher quality phosphorus-doped films and have been confirmed to be closer to 0.57 eV [152]. Lastly, and more recently, lower ionization energies $E_D = 0.47$ and 0.53 eV, have been reported by Stenger et al. [134] asides with a modelisation of E_D lowering versus N_D increasing. However, they have only been reported by a unique research team and probably needs more statistical confirmation. Additionally, models introduction of the conduction band-edge shifting [172], and band edge tailing [173, 174], are promising but the non-hydrogenoid model of phosphorous in diamond, seems to impede their validity range, in the sense that additional calculations are required to validate these hypothesis.

Free carrier concentration vs. doping level, compensation and temperature

Besides the heavily doped layers used to enhance formation of ohmic contacts (see section II.5.2.a), the typical range of doping levels used in the active regions of lateral power FETs is below 10^{18} cm^{-3} since high doping levels lead to diminution of the mobility as described in the next section, and lower breakdown voltages as detailed in the second chapter. Therefore, hopping conduction mechanisms are not accounted in the further calculations but they are briefly discussed at the end of this section, as JFET transistors designed in this thesis should benefit from heavily phosphorus-doped layer. The case of non-degenerated diamonds could be considered, with the constant, low impurity concentration ionization energy, but Pearson and Bardeen's law has been preferred for boron doped diamond (eq. I.6). Subsequently, from the charge balance equations and neutrality equation between the number of positive and negative charges, accounting both free and fixed charges, the free electron and hole densities (n and p respectively) are determined by the use of Fermi-Dirac distribution. Hence for a p-type material, the free hole concentration can be expressed as function of temperature T, doping level N_A and compensation N_D by [134, 156, 175]:

$$p(T, N_A, N_D) = \frac{1}{2}(\phi_a + N_D)\left(\sqrt{1 + \frac{4\phi_a \cdot (N_A - N_D)}{(\phi_a + N_D)^2}} - 1\right) \tag{I.7}$$

Similarly, for an n-type semiconductor, the free electron density is given by:

$$n(T, N_D, N_A) = \frac{1}{2}(\phi_d + N_A)\left(\sqrt{1 + \frac{4\phi_d \cdot (N_D - N_A)}{(\phi_d + N_A)^2}} - 1\right) \tag{I.8}$$

$$\text{where} \quad \phi_{a(d)}(T, N_{A(D)}) = g_{h(e)} \cdot N_{V(C)} \cdot \exp\left(-\frac{E_{A(D)}}{k_B T}\right) \tag{I.9}$$

with k_B the Boltzmann's constant, $g_h = 1/4$ and $g_e = 2$ the degeneracy factor for both holes and electrons respectively, along with $N_V(T)$ and $N_C(T)$ the effective density of state of the valence and conduction band, respectively. In the framework of parabolic approximation [176], they are expressed through their temperature dependence:

$$N_{V(C)}(T) = (M_{V(C)}) \cdot \frac{2(2\pi \cdot m^*_{h(e)} \cdot k_B T)^{3/2}}{h^3} \tag{I.10}$$

with h the Planck's constant, $M_C = 6$ used to compute $N_C(T)$, the number of equivalent conduction band minima located along $\Gamma - X$ (see section I.1.4) and $M_V = 1$ for $N_V(T)$, similarly associated to the single valence band maximum. The electron and holes density-of-state mass, m^*_e and m^*_h respectively, are computed from the experimental value extracted from cyclotron resonance of optically excited carriers in ultra pure diamond [177]: $m^*_e = 0.496\ m_0$ and $m^*_h = 0.848\ m_0$, expressed as function of the electron mass $m_0 = 9.11 \times 10^{-31}$ kg.

Based on equations I.7 and I.8, the Fig. I.16 illustrate for both boron-doped and phosphorus-doped diamond, the dramatic effect of compensation and oppositely the huge benefits of high temperature, on the free hole and electron concentrations. Free carriers concentrations with compensation ratios among 0%, 1% and 10% are calculated, which align with commonly reported values for various boron-doping levels but still remains optimistic value (amongst the lowest reported) for different phosphorous-doping levels[178].

In p-diamond, a limited number of acceptors are ionized around room temperature, part of the carriers are trapped by donor atoms and the free hole density is drastically decreased. To image this, uncompensated p-diamond typically exhibits a low ionization rate (p/N_A) at RT, with around 1%, or even less than 0.1% if the compensation ratio exceeds 10%. In other terms, if the boron-doping level targeted is 10^{17} cm^{-3}, at RT the computed free hole concentration in an uncompensated layer is expected to be 8×10^{14} cm^{-3} whereas it drops to 5×10^{13} cm^{-3}

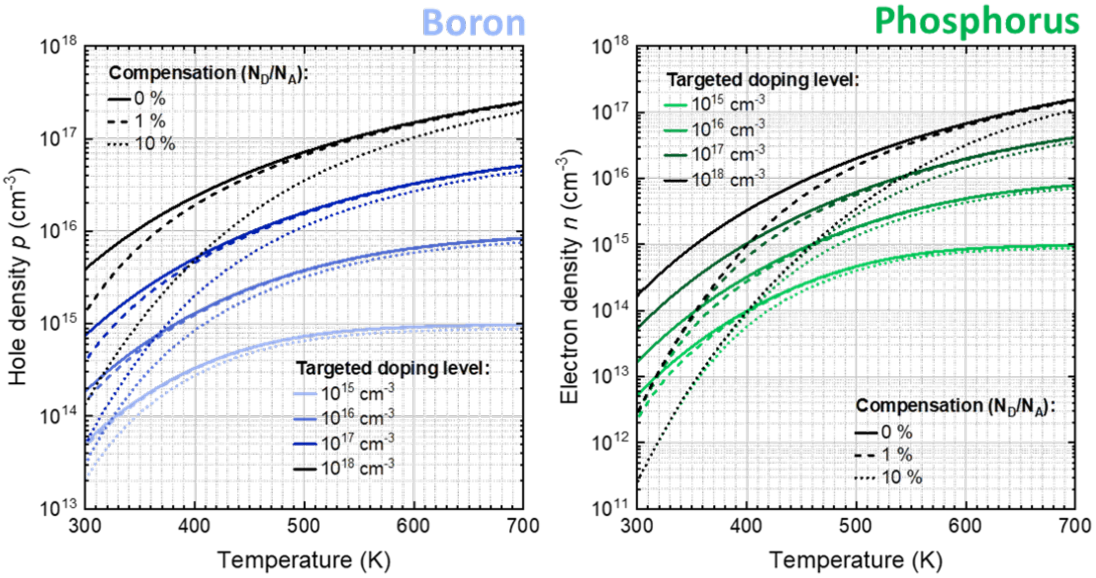

Figure I.16: Calculated free hole (left) and electron (right) concentration of both boron-doped diamond, and phosphorus-doped diamond respectively, as function of temperature for various doping level and compensation couples.

with a compensation of 10%. This low ionization rate, is of crucial importance for the devices ON-state as the resistivity (see equation I.5) is mainly hindered at room temperature by the low free carrier density. As temperature increases, the free hole concentration becomes larger with respect to the donor density, mainly due to the thermal ionization of the dopant, in turns diminishing the compensation impact. For instance, still for a targeted boron-doping level of 10^{17} cm^{-3}, at 500 K, calculations suggest that without compensation, the hole concentration is around 1.5×10^{16} cm^{-3} which corresponds to an ionization ratio of 15%, while with 10% compensation the hole concentration is expected to be 10^{16} cm^{-3}, with a 10% ionization ratio.

Free electrons in phosphorus-doped diamond also follow a similar behavior than free holes in boron-doped diamond, although compensation and temperature effects are way more impactful. Calculations reveal that for uncompensated n-diamond, the ionization rate (n/N_D) at RT is less than 10^{-3}, and further drop to 10^{-6} when compensation ratio surpasses 10%. At 500 K, for a targeted donor concentrations of 10^{17} cm^{-3}, an uncompensated layer exhibit a free electron density of 6×10^{15} cm^{-3} or an ionization ratio of 6%, whereas with 10% compensation the ionization ratio drops to 3%, corresponding to a free electron density of 3×10^{15} cm^{-3}. In comparison, p-type doping results in twice more acceptor ionization in the same doping and compensation ranges. The same comparison is even more pronounced at lower temperatures and for higher doping level, especially for an increase in compensating species in phosphorous-doped diamond.

The benefits of high temperature or, negative temperature coefficient, in diamond is demonstrated to be strongly contingent upon the compensation ratio even when dealing with relatively low compensator concentration levels. However, this dependency significantly attenuates as the temperature elevates, even if the mobility is affected in an opposited direction.

I.2.2.d Free carriers mobility models

Free carrier mobility, like free carrier concentration, is a key parameter subject to variations based on temperature and doping levels. While H-terminated FETs have gained interest over the last two decades due to their uses of diamond surface conduction through 2D hole gas (2DHG), they reached a point where the weak 2DHG mobility becomes the limiting factor compare to the

2DHG sheet carrier concentration [179]. Even if, recent progresses have been achieved to improve this trade-off [180], the mobility reported are below bulk p-conduction achievable values. This later statement needs to be tempered with latest results obtained on H-terminated FET where mobility of 600 cm^2/V.s have been reported [180] thanks to the use of hexagonal boron nitride (h-BN) as gate dielectric. However, in a bulk conduction device with minimal surface effects, the principal mechanisms considered for scattering are phonons and impurities, as elaborated in detail in the work of Pernot et al. [181, 182]. In this work, an empirical mobility model is developed and provides the dependence of μ as function of doping level, N_A for p-type or N_D for n-type, compensation and temperature by the following:

$$\begin{aligned} \mu(T, N_{imp}) &= \mu_{300K}(N_{imp}) \times \left(\frac{T}{300}\right)^{-\beta(N_{imp})} \\ \text{where} \quad \beta(N_{imp}) &= \beta_{min} + \frac{\beta_{max} - \beta_{min}}{1 + \left(\frac{N_{imp}}{N_\beta}\right)^{\gamma_\beta}} \\ \text{and} \quad \mu_{300K}(N_{imp}) &= \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N_{imp}}{N_\mu}\right)^{\gamma_\mu}} \end{aligned} \tag{I.11}$$

Compensation is accounted in the herein-above model, through $N_{imp} = N_A + N_D$ as being the sum of both main dopant impurities and compensating ones. All the parameters used in this model are listed in table I.3.

Table I.3: Empirical mobility model parameters after [156, 181]

Symbol	β_{min}	β_{max}	γ_β	γ_μ	N_β	N_μ	μ_{min}	μ_{max}
Unit	*no*				cm^{-3}		cm^2/V.s	
Hole	0	3.11	0.617	0.73	4.1×10^{18}	3.25×10^{17}	0	2016
Electron	0	2.17	0.585	0.564	3.75×10^{17}	9.9×10^{16}	0	1030

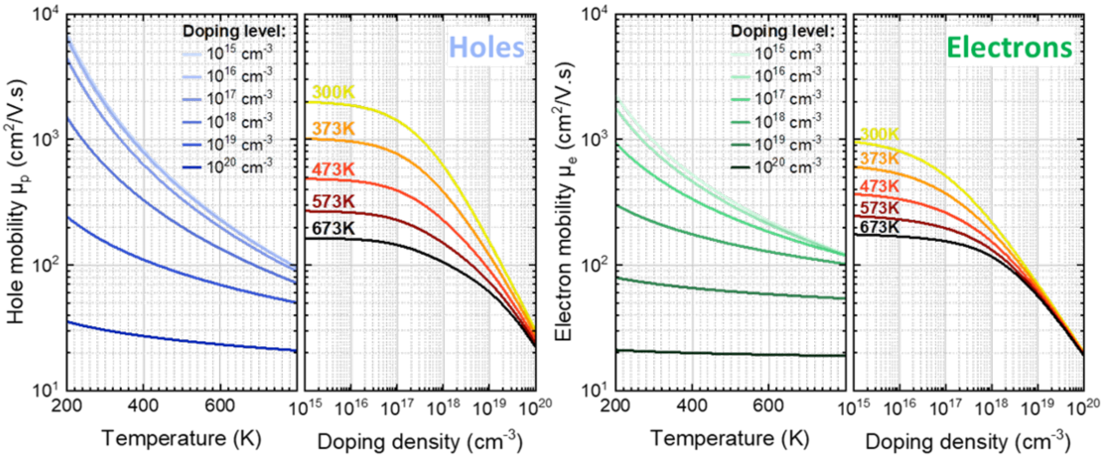

Figure I.17: Calculated, hole (left) and electron (right) mobility values, as function of either: (left sub-graphs) temperature for various doping densities between 10^{15} and 10^{20} cm^{-3}; and (right sub-graphs) doping densities for different temperatures, ranging from RT (300 K) to 673 K (400° C). Noticeably, compensations have been neglected as well as hopping mechanisms, even if models provided by equation I.11 and development made in section I.2.2.e can take it into account.

As depicted in Figure 1.13, the mobility exhibits modest variations versus doping level when, N_A for holes and N_D for electrons, are below 10^{17} cm^{-3}, due to the predominance of phonon scatterings. At RT, the mobility for a boron-doped diamond at 10^{15} cm^{-3} stands at 1987 cm^2/V.s, contrasting with 1417 cm^2/V.s at 10^{17} cm^{-3}. Similar behavior is observed for phosphorus-doped diamond, where, at 10^{15} cm^{-3} the computed mobility is 945 cm^2/V.s, whereas it drops to 518 cm^2/V.s at 10^{17} cm^{-3}. Beyond this threshold, a more pronounced reduction in mobility ensues, driven by the dominance of impurity scattering mechanisms, causing it to decline to 153 cm^2/V.s at 10^{19} cm^{-3} for p-diamond, 71 cm^2/V.s at 10^{19} cm^{-3} for n-diamond. Regarding the impact of compensation, a 10% compensation ratio induces a mobility twice lower than the maximum value expected for uncompensated p-type, but also n-type, material [178]. In both p- and n-diamond, as the temperature increases, all scattering mechanisms, encompassing phonons and impurities, exhibit a negative temperature coefficient. This reversed temperature dependence compared to free carriers densities, leads to the mobility of a layer doped at 10^{17} cm^{-3} decreasing from, 1417 cm^2/V.s at RT to 392 cm^2/V.s at 400 K for p-diamond, and 518 cm^2/V.s at RT to 261 cm^2/V.s at 400 K for n-diamond. However, mobility generally drops for a few order of magnitude versus temperature, whereas free carrier concentration increase way more over the same range.

I.2.2.e Resistivity: toward negative temperature coefficient

Bulk conduction resistivity

By the use of the mobility and free carrier density models introduced in the last sections, the resistivity with its doping level, compensation and temperature dependence, can be further compiled, using eq. I.5, as reported in Fig. I.18. The color scale representation conceptualized by Traoré et al. [178] has been preferred for its completeness and ease of reading offered. Experimental data reported in literature are also provided where resistivity value of each symbol is indicated by its face color according to the color bar located on the right side.

In the vicinity of RT and below, the temperature-dependent resistivity in diamond is primarily ruled by dopant ionization which completely overcome the mobility decrease. It results in the observed negative temperature coefficient, offering diamond conductive properties to be enhanced in harsh thermal environment. However, as the temperature rises above 500 K, the higher ionization rate, close to exhaustion regime (full dopant ionization) for lower doping levels, confronts a reduction in mobility attributed to optical phonon scattering. Consequently, this interplay leads to an upswing in resistivity with increasing temperature, even more marked for lower doping levels, giving rise to an optimal operating temperature. While being close to 500 K for low doped p-diamond, this optimal temperature is significantly higher for n-diamond as the exhaustion regime is still not reached at 500 K, even for low doping levels. Additionally, this critical temperature value escalates significantly in response to higher doping levels, rendering it impractical for device operation where compound packaging are not optimized for such thermal stress. Therefore, except for exceedingly low doping levels or higher than the metallic transition for boron-doped diamond, the negative temperature coefficient is anticipated to persist across the entire operational temperature range for diamond devices relying on bulk conduction, including the ones fabricated and characterized within this thesis. Furthermore, the experimental datas reported in literature seems to be in good agreement with the model proposed and only punctual discrepancy are observed, comforting the relevance of the latter for future device design.

As a direct consequence of level depth, the high thermal load that would be required in n-diamond unipolar devices, to be competitive with p-diamond in terms of conductivity, has discouraged their development over the last decades. Additionally, an experimental correlation can be drawn between the phosphorous doping level and compensation, as further discussed in [182]. This experimental correlation is different to p-diamond, where no relation was evidenced between doping level and compensation densities. In the few experimental data discussed here, the donor density increase is counterbalanced by a higher compensation level in such a way that the carrier concentration is always ranging around the same value. Further analysis would be

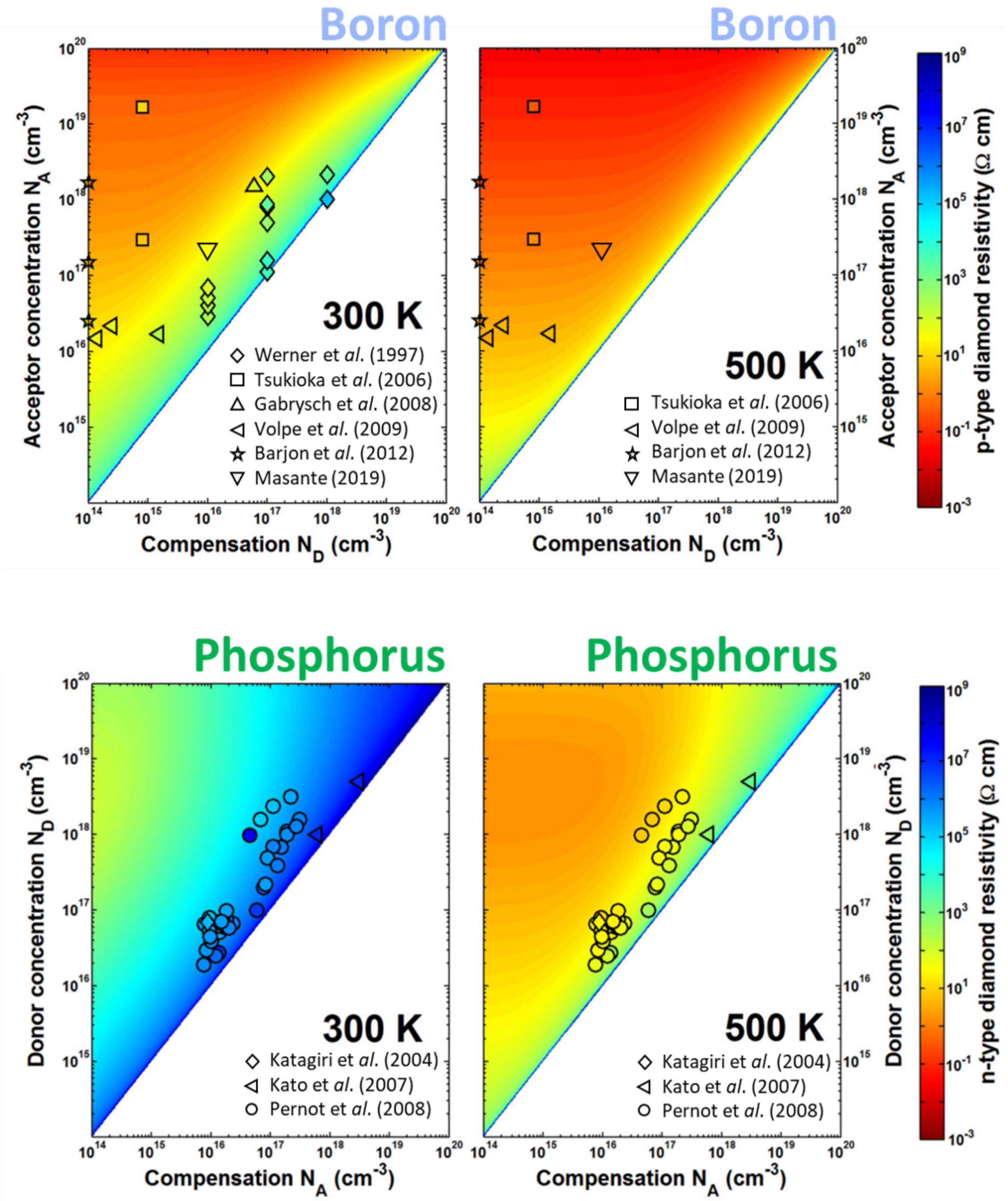

Figure I.18: Boron-doped p-type diamond (top) and phosphorus-doped n-type diamond (bottom) resistivity as a function of acceptor concentration and donor concentration respectively, asides with compensation at 300 K (left-hand graphs) and 500 K (right-hand graphs). Graphs taken and modified from [178] where color scales have been privileged for ease of reading. Experimental data, from [58, 156, 183–186] for boron-doped diamond and from [144, 182, 187] for phosphorus-doped diamond, are colored in respect to their reported resistivity (regarding the color scale).

strongly appreciated to confirm this dependency, especially related to growth conditions, for the future of n-diamond device prospect. Nevertheless, for bipolar devices such as pn diodes, n-diamond are commonly heavily doped in order to enhance the hopping conduction, thus ultimately giving rise to resistivity reduction.

Toward heavy doping and hopping mechanisms

As mentioned all along the previous sections but not accounted, heavily-doped ($10^{18} - 10^{19}$ cm^{-3}), n- and p-diamond conductivity, is enhanced by carriers hopping from neutral to ionized impurities. In boron-doped diamond, the resistivity below the metallic transition, has been proven to be governed by a combination of band conduction and variable range hopping (VRH) mechanism [139, 188]. However, the doping level range where VRH becomes predominant lies outside the scope of this thesis, and thus, this mechanism will not be elaborated upon in this manuscript, while for more detailed information on this topic one can refer to [189–192]. In this section, the discussion delves into nearest neighbor hopping (NNH) as being the main conduction mechanism in heavily phosphorus-doped diamond at reasonable temperature [171], and regarding its uses proposal made in this manuscript. Already reported to significantly decrease the layer resistivity [169], NNH impact can be taken into account from previous calculation by the reformulation of the resistivity model, following [170]:

$$\begin{aligned} \rho_n &= \frac{1}{q \cdot n \cdot \mu_{eq}} \\ \text{where} \quad \mu_{eq} &= \mu_n + \frac{n_{hop}}{n} \cdot \mu_{hop} \\ \text{and} \quad \mu_{hop} &= \frac{1}{6} \cdot \frac{q \cdot R_{hop}^2}{k_B T} \cdot \nu_{ph} \cdot \exp\left(-2\alpha \cdot R_{hop} - \frac{q \cdot W_{hop}}{k_B T}\right) \end{aligned} \tag{I.12}$$

With n the free electron density calculated from eq. I.8, μ_n the conduction band mobility modelized by eq.I.11, μ_{hop} commonly used to represent the hopping mobility [190] and n_{hop} the hopping carrier concentration. The latter is commonly simplified as the non-ionized carrier concentration given by $n_{hop} = N_D - n$, assuming that all the non-ionized impurities participate to hopping mechanism. R_{hop} is the hop length or the mean distance between impurities, simplified as $R_{hop} \approx N_D^{-1/3}$ [193], $\nu_{ph} = 2 \times 10^{11}$ s^{-1} is the phonon scattering probability, $\alpha^{-1} = 1.8$ nm is the localization length of the wave-functions overlapping [189, 194] and W_{hop} is the thermal activation for the hopping process, which has been taken equal to 51 meV, but could vary regarding to the doping level according to [169].

Fig. I.19 shows the calculated resistivity, using eq. I.12 of phosphorus-doped diamond as function of doping level or temperature. The resistivity decrease due to participation of hopping conductivity appears clearly at 200 K for doping levels around 2×10^{18} cm^{-3}, with a slight increase at 300 K where it becomes predominant for doping levels higher than 10^{19} cm^{-3}. As the tunneling probability is sensitive to the tunneling distance R_{hop}, doping concentrations strongly affect the hopping mobility, and ultimately its contribution to the total resistivity. A steep decrease in μ_{hop} can be observed with lower doping concentration, where hopping conductivity is absent. This behavior is reliable with experimental datas reported in literature [169, 171]. At RT, an almost identical resistivity was reported for doping levels of 3×10^{18} cm^{-3} and 10^{18} cm^{-3}, while a drop of more than an order of magnitude, not predicted by the unique band-conduction model, has been reported for a doping level of 3.9×10^{19} cm^{-3}. As NNH is based on activation type carrier conduction, μ_{hop} is further reduced at low temperature but, with a lower impact than the conduction band mobility. At higher temperature, the effect of hopping mechanism tends to vanish due to consequent increase of the ionization rate. Taking into account that $n \ll N_D$, even at 600 K and for $N_D > 10^{18}$ cm^{-3}, the neutral impurity number $n_{hop} = N_D - n$ does not significantly change. However, by considering the mobility, the hopping mechanism becomes less conducting compared to band conduction at 600 K when mobility is considered. Consequently, the contribution of NNH conduction to the resistivity is diminished, as observed at 500 and 600 K for a fixed doping level.

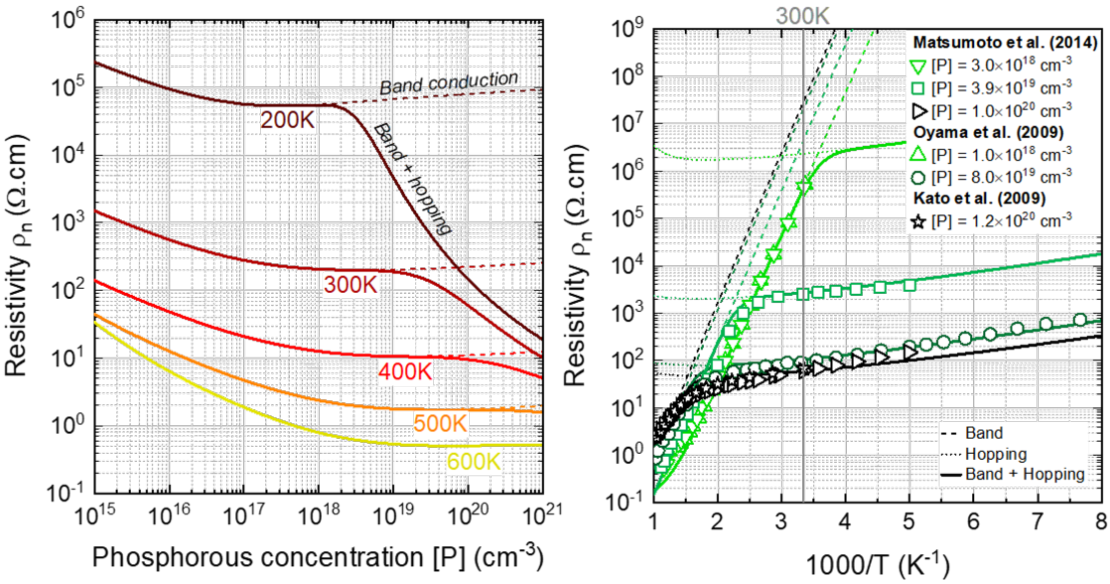

Figure I.19: Left, calculated phosphorus-doped diamond resistivity as function of doping level for different temperatures, taking into account the combined effect of band and hopping conduction mechanism (solid lines), compared to band-only conduction (dashed lines). Right, calculated phosphorus-doped diamond resistivity as function of 1000/T for various doping level corresponding to the data reported in [169, 171, 195].

I.3 State of art for innovative diamond based devices

In this section, the concept of power electronics will be introduced, as well as the state of art of diamond-based devices, mainly focused on achieved diodes and transistors. A specific attention is paid to JFET devices, delving into the higher challenges they faced compared to MOSFET and MESFET devices, which tends to be a way more developed. A concept of diamond-based memory using a non-volatile photo-switch, at the heart of this manuscript, is presented. A presentation of its wide range of application, from integrated and/or embedded power electronic devices to chronic biomedical implants, passing by quantum communication future prospects will be done.

I.3.1 Diamond for power electronics

Power electronics, which involves the use of solid-state electronic devices to manage and convert electrical power for specific needs, is integral to modern energy systems. The tremendous demand for electric energy, particularly in European countries with limited storage options, along with the ongoing climate change challenges, calls for sustainable energy production and efficient transmission systems. Current model relies on centralized electrical power generation followed by high-voltage transmission to minimize conduction losses. This high voltage requires multiple conversion stages regarding its wide range of final applications, necessitating power devices capable of converting electricity into various voltage and current levels. These devices, including rectifiers (AC-DC), inverters (DC-AC) conversions, and amplification/attenuation converters, play a crucial role in this process.The surge in energy demand has elevated the significance of power electronics, driving its global market to a remarkable 29 billion euros in 2020. While silicon-based devices proved their hegemony on this market, which will continue its expanse in the future due to the worldwide growing demand for sustainable electricity production, the later also originate for most energy losses in the entire energy distribution chain. This paradox turns the current status of power electronics into a bottleneck for sustainable energy usage, regarding the economic and politic context, but it also opens a niche for future development.

These losses primarily result from material limitations within the devices, which can be primarily seen as electrical switches, conducting current during the ON-state and blocking it during the OFF-state. During the ON-state, the device's resistance, related to material resistivity, dissipates heat due to the Joule effect, especially for high current levels faced in power electronics. During the OFF-state, the device must withstand the maximum voltage, ranging from hundreds of volts to tens of kV, depending upon technical specifications, which are mostly associated with the material's critical electric field (omitting geometrical parameters). These two material properties are intricately linked, leading to a fundamental trade-off in power electronics: ON-state vs. OFF-state performance. Apart from conduction losses, switching losses, arising from the time required for devices to transition between ON and OFF-states, constitute a substantial part of total power device losses. In every switch, whether using gate capacitance for transistors or junction capacitance for diodes, there's a need to charge or discharge, with the associated current flow under high voltages (during transient), resulting in losses. While current silicon technology reaches its theoretical limits, a door is opened for UWBGs materials, with diamond on top of the list regarding its exceptional properties demonstrated along the previous sections, to access better performances and noticeably, better ON vs OFF-state trade-off.

I.3.1.a Schottky and pn-diodes

Diamond Schottky diodes are the most developed component nowadays and have primarily been developed using boron-doped layers due to the challenges associated with low phosphorous incorporation and the high activation energies required for n-type dopants. Bipolar devices, on the other hand, have limited advantages because of the high built-in voltage of the p–n junctions. Subsequently, bipolar diodes are suitable mainly for ultra-high-voltage applications, exceeding 10 kV, and low to medium-frequency applications, if bipolar carrier lifetime is high enough to significantly reduce the ON state voltage drop under high injection regime (to compensate the high built in potential) [61].

Both unipolar and bipolar diamond diodes have been successfully manufactured and summarized in Fig. I.20, including Schottky, metal-intrinsic-P (MIP), Schottky p–n diodes (SPND) for unipolar action, and pn junctions and PIN diodes for bipolar action. Concerning p-type diamond Schottky diodes, the literature reports high blocking voltages (up to 10 kV) [196] and critical electric field (7.7 MV/cm) [197], although material quality disparities have led to discrepancies in experiments. Some diodes have achieved remarkable currents, exceeding 10 A [198], and have demonstrated high-temperature (above 525K) operations without degrading the Schottky properties [121, 197, 199].

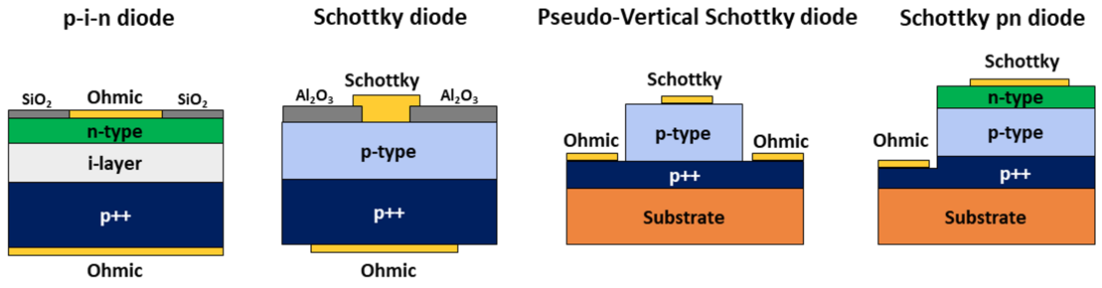

Figure I.20: Scheme of the different fabricated diamond diodes.

Regarding architectures, the limited technology stage in terms of etching [200] and growth, asides with the challenges to obtain large-size, self-standing, low-resistive single crystals, have led to push the use of pseudo-vertical architectures the preferred solution. The best trade-off to date has been achieved with Zr for pseudo-vertical diamond diodes [197], while a 5 A and more than 1 kV, vertical diode has been demonstrated with Pt Schottky metal [201].

Diamond vertical p-i-n diodes have been successfully developed, but issues related to carrier lifetime control, reproducibility, and uniformity persist [202, 203]. Furthermore, the high built-in voltage of the pn junction [204] remains a limiting factor in this device structure development. To address these challenges, Schottky pn-type diodes have been proposed, allowing the Schottky metal on top of the n-type layer to deplete the n-type doped layer in both the ON and OFF states, supporting hole injection from the p+ layer during the ON state and sustaining the reverse voltage simultaneously. Schottky pn-diodes demonstrated the highest current density among diamond diodes and benefits from the high switching speed ($\approx$ 10 ns) [205] of the Schottky diodes but, in relation to their conduction mechanisms both through the contact (thermionic emission) and the layer (hopping) is significantly lowered at higher temperature [206]. Noticeably, on the pseudo vertical architecture, the p++ layer lateral resistance can be a limiting factor in the devices current capacity [207]. In fact, the p++ layer are designed thin despite there low resistivity, and so the layer lateral resistance can be significant compared with the vertical resistance of the weakly boron-doped p-layer.

While most of the summarized diamond-based diodes presented here show promising standalone performance for power electronic applications, their greatest value lies in serving as a solid foundation for transistor fabrication. When employed as gate contacts, they enable the modulation of channel resistivity, leading to the development of various transistors morphologies and architecture.

I.3.1.b Transistors

Recent advancements in the control of diamond doping and layer quality have given rise to a diverse array of transistor concepts capitalizing on this material's exceptional properties. Notably, metal-semiconductor FET (MESFET), H-terminated FET (HFET), junction-FET (JFET), inversion metal-oxide semiconductor FET (MOSFET), outlined schematically in Fig. I.21 and diamond deep-depletion MOSFET (D3MOSFET) have been fabricated and demonstrated successful operation. This work will focus primarily on an in-depth analysis of the junction field effect transistor (JFET) working principle, while briefly reviewing other noteworthy innovative structures, their achievements, and the challenges they have addressed or are yet to overcome. Comprehensive insights into the workings and modeling of each structure can be found in [208], while detailed reviews of diamond transistors are available in [61, 209]. In the early stages of diamond technology development, transistor architectures were predominantly lateral, but the transition towards vertical configurations is anticipated to enhance performance in the years ahead, supported by the development of more optimized etching and growth processes.

Inversion and H-terminated MOSFET

The most attractive or trendy research on diamond transistors currently focuses on lateral MOSFET devices utilizing 2D hole gas (2DHG) on H-terminated diamond. In these FETs, surface conduction through hole accumulation at the diamond/oxide interface is strongly enhanced by the transfer doping process, which occurs through energy levels within the oxide layer [210]. Proximity between transferred charges and the 2D hole gas has been identified as a key factor limiting mobility, hence ON-conductivity performances. Increasing the separation between them has led to mobility improvements of up to 680 $\mathrm{cm^2/Vs}$ at carrier concentrations of 10^{12} to 10^{13} $\mathrm{cm^{-2}}$ [180, 211]. These transistors exhibit excellent on-state performance, particularly at room temperature, with record current densities exceeding 1.6 A/mm [180], bypassing the limitations posed by the high ionization energy of boron. Although the maximum estimated breakdown field for these FETs is 3 MV/cm, considerably lower than the theoretical bulk critical field of 10 MV/cm, they have achieved a record OFF-state voltage of 2 kV [212]. Nevertheless, the upward scalability of this breakdown voltage is expected to stay pretty low compared to bulk transistors. However, H-FETs feature great interest for radio-frequencies (RF) power electron-

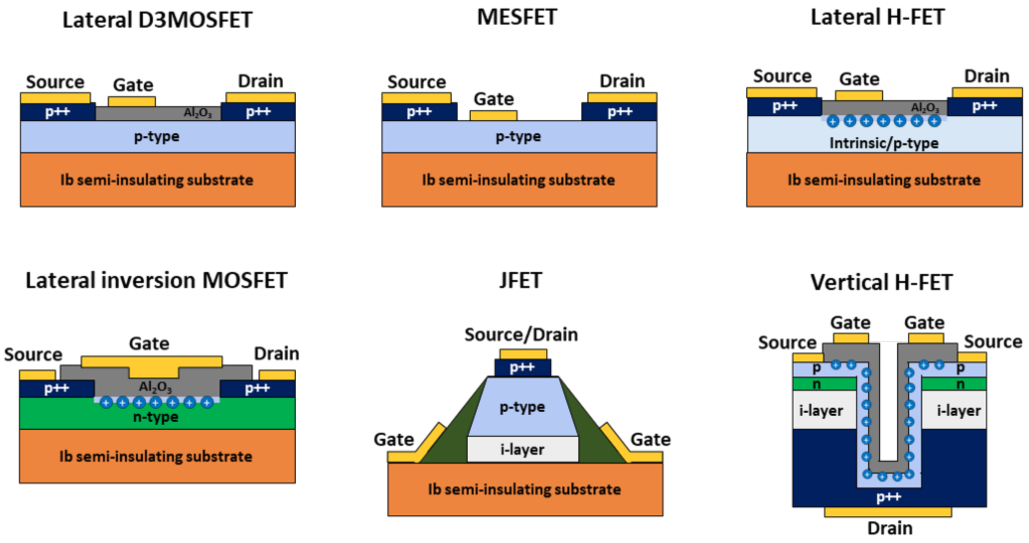

Figure I.21: Cross section scheme of the different most advanced diamond-based transistors.

ics where current and power gain at a maximum operation frequency of up to 100 GHz have been demonstrated [213, 214]. While, normally-off H-FETs have been developed using various techniques, such as partial gate interface oxidation [212] or nitrogen implantation [215], their persistent main challenges lie in time and temperature stability, even if significant progresses have been made in recent years, enabling operation at temperatures above 600K [216].

Additionally, it seems important to consider that the feasibility barrier of vertical components in diamond (which offer a better resistance/breakdown voltage compromise) has been partly overstepped by the successful fabrication of the vertical H-FET, which gather all the most advanced and challenging fabrication process of diamond [217, 218]. However, even if this challenge has been surpassed, and the feasibility of such transistors proven, the recorded current and breakdown voltages are still way below expectations, rendering these device not competitive with other architecture at their actual stage of development. On the same basis, a lateral inversion MOSFET employing phosphorus-doped diamond layer covered by alumina as gate oxide, has been firstly introduced by Matsumoto et al. [219]. This prototype, mostly designed for proof of concept, achieved a significant maximum drain current density of 1.6 mA/mm and a channel field effect mobility of 8 cm^2/Vs. Others subsequent proof-of-concept inversion transistors were developed either, in freestanding hetero-epitaxially grown diamond [220] or through the use of a nitrogen-doped diamond body [221]. It's important to note that these devices (vertical H-FET and inversion MOSFET) were not competitive with other architectures, especially in terms of blocking voltages, but they also were not designed with that mind and more to prove the feasibility of these concepts.

Depletion-based FET

Depletion-based FETs, encompassing JFETs, MESFETs, and D3MOSFETs, strongly benefit from high-temperature operation regarding boron-doped channel activation rate (see section I.2.2.e), while the OFF-state is achieved by full-width channel depletion beneath the gate. In the case of D3MOSFET, the off-state operation relies on the deep depletion, driven by the exceptionally long minority carrier generation time in diamond. Compared to MESFETs, it gives access to higher doping, hence better current performance, but interfaces with oxides always host a high density of interface states, which, associated with different charge/discharge mechanisms, limits switching capabilities and significantly affect leakage current. MESFETs performances are also hindered by interfaces issues, particularly underneath the gate Schottky gate contact, where lightly doped channel region are preferred to mitigate gate leakage, particularly at high temperatures. Various diamond MESFETs, employing different Schottky metals (e.g., Mo, Pt, Al), have been demonstrated, recording maximum current densities of 2 mA/mm at high temperatures (600 K) [222] and breakdown voltages (BV) above 2 kV [223]. Highest breakdown voltages for diamond-based transistors have been reached by MESFETs based on reverse blocking (RB) configurations, showcasing a maximum BV of 3 kV, but coupled with limited maximum on-state current of 1 µA [224]. MESFETs showed elevated breakdown voltages, which additionally scale pretty well with the drift layer enlarging, but the critical electric field reached inside the channel (≈ 2.1 MV/cm) is still far from the ideal diamond critical field of 10 MV/cm. Based on these criteria, D3MOSFETs have demonstrated impressive characteristics, including a drain current density of 10 mA/mm under an operating temperature of 523 K and also a BV of 175 V corresponding to a maximum electric field of 5.4 MV/cm (estimated field peak under the gate, at breakdown voltage) [76]. However, the scalability of this OFF-state capability is strongly limited by the oxide and diamond-oxide interface quality, mostly leading to oxide-caused prematured breakdown [58]. It is important to notice that, this limit can still be addressed with appropriate device design, especially the addition of a source-field plate in the lateral D3MOSFET as recently developed within Diamfab, in collaboration with, Laplace and Institut Néel [225, 226].

The best ON-current/OFF-breakdown voltage ratio was obtained by the use of a JFET architecture, based on p-n+ junctions with high BV of up to 1 kV [227]. JFETs with both normally-on and normally-off variants have been proposed, offering access to whether unipolar and bipolar conduction. Unipolar normally-on JFETs exhibit impressive current densities of 10 A/cm^2 at room temperature and close to 600 A/cm^2 at 500 K, but still with low absolute current value (≈ 2μA) due to reduced device active area [228, 229]. They can block over 600 V with a breakdown field exceeding 6 MV/cm [230]. Normally-off JFETs are created by reducing the doping concentration or channel width to deplete the entire channel under the gate at 0V. These JFETs have lower current density due to the reduced thickness and increased resistivity of the channel [231]. Noticeably, bipolar mode operations pushed forward the ON-conductivity of JFETs, up to 3500 A/cm^2 at 500K, but also with diminished breakdown voltage at higher temperature [228, 229]. The realization of non-volatile diamond memory based on JFET transistors, the focus of this thesis, is also a very good excuse to benefit from the scalability of JFETs performances with the transistors active areas. Consequently, a splitted part of this thesis has been devoted to the realisation and characterisation of large scales diamond-based JFETs, one of the most promising architecture, but also challenging in respect to the n-type diamond growth and its associated high electrical resistivity.

I.3.2 Focus on junction field effect transistors

I.3.2.a JFET references and validated milestones

Effective doping control, being one of the most important pre-requisite for electronic devices, is historically a serious hurdle concerning n-type diamond. Nitrogen or phosphorous, the two n-type dopants of diamond, are still not effective enough to produce high electron densities at room temperature, justifying the late development of diamond based JFET compared to unipolar devices like MOSFET or MESFET. Although a controversial diamond BJT have been demonstrated earlier in 1982 [232], no clear demonstration of successful n-type doping was reported in this previous work, hence bipolar operation was questionable. Control of the n-type doping have been disruptive until the early 2000s, with the demonstration of a δ-doped JFET [233, 234] but especially with the work of Koizumi et al. [133] that reports the first successful realization of n-type mono-crystalline diamond. However, JFET reported by the use of stacked δ-doped p-type conduction channel and nitrogen doped layer as gate, has still not demonstrated clear off-current state at room temperature. Nevertheless, architecture building blocks such as recess gate or gate field plate have been successfully implemented and are promising for on-state resistance and breakdown voltage optimization, even if low nitrogen ionization was still the main technological issue.

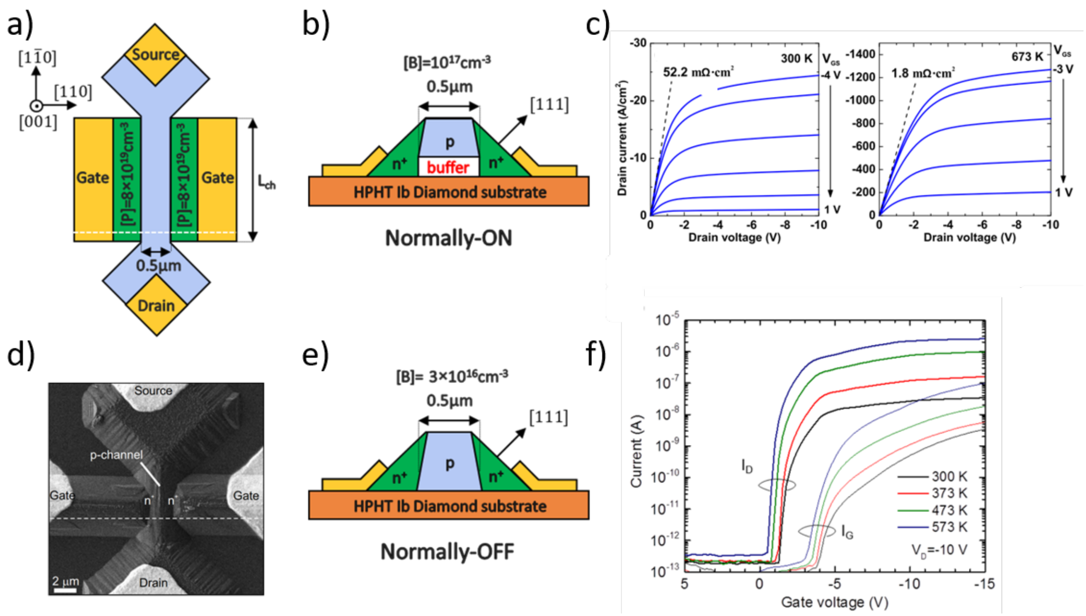

Figure I.22: (a) Top view, (b) cross sectional view of schematic diamond JFET and (c) drain current density as function of drain voltage for different gate bias, for Normally-ON diamond based JFET. (d) SEM image of normally-ON sample, (e) cross sectional view and (f) drain current density and gate current density as function of gate voltage for Normally-ON diamond based JFET. Graphs from [228, 230, 235, 236]

A decade ago, the first diamond-based JFET that can be switched OFF by gate voltage, at room temperature, have been demonstrated in [228, 230, 235, 236], and today remains the reference for this transistor architecture. The devices, reported in fig. I.22 (b) and (e), uses lateral pn-junctions to control the conductance of a bar-shaped p-channel and thus exhibiting transistor characteristics shown in fig. I.22(c) and (f) respectively. Room temperature functionalization of this diamond JFET has been brought by the resolution of the main technological breakthrough, the partial activation of n-type dopants used for the gate layer.

The realization of these devices has been made possible thanks to the work initiated by Koizumi et al. [137] about (111) phosphorus doped diamond, and followed by Kato et al. [237] concerning the selective growth control of (100) highly phosphorus doped layer. This skillful technique benefits of patterned surface morphologies along (001)-oriented diamond, to control growth rate and doping along the (111) direction, known to be most effective for phosphorus incorporation. More than bringing control of the device at room temperature, this breakthrough gave rise to a p-channel resistivity of 52.2 mΩ.cm^2 and a breakdown voltage of 600 V corresponding to a critical electric field of 6.2 MV/cm (considering that electric field peak is located at the boundary between the n-side gate and the p-channel on the drain side). This elevated critical electric field is among the highest reported in diamond, where other architectures like MOSFET or MESFET suffer from diamond/oxide or diamond/metal respectively, interface quality, giving rise to a maximum critical field of 3-5 MV/cm.

Other building blocks have been reached in the concern of the realization of a normally-OFF device [228] which is preferred for power applications. Adaptation of the p-channel doping, regarding to n-type gate layer doping, demonstrated the full depletion of the channel without gate voltage application as shown in fig. I.22 (f). This milestone has also been enhanced by removing the buffer layer, sandwiched between the p-channel and the Ib diamond substrate which most diamond lateral devices reported in literature make use of, due to their high crystalline

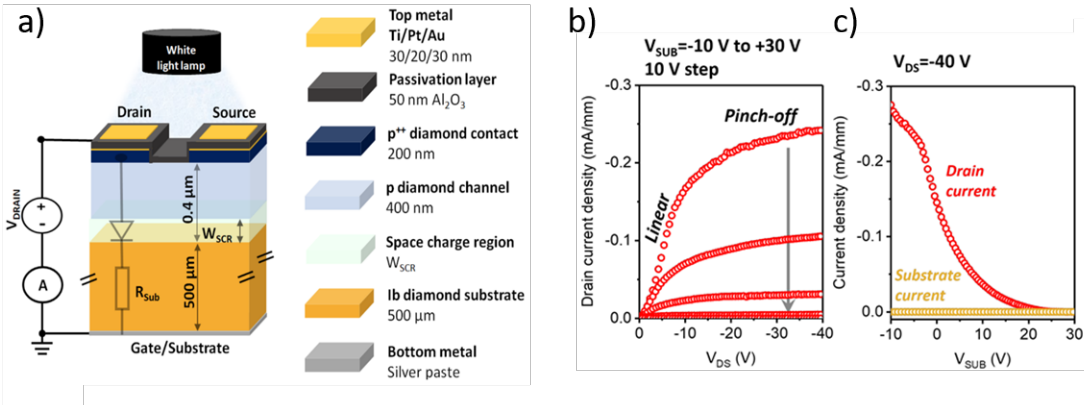

Figure I.23: (a) Cross section of JFET using Ib diamond substrate as gate layer. (b) Drain current density as function of drain voltage for different gate/substrate bias, at RT and under white light irradiance of $11mW.cm^2$*. (c) Transfer characteristic. Courtesy of Masante et al. [241]*

quality and low defect density. However, due to growth condition, these substrates contain a high level of nitrogen impurities ($\approx 10^{19}\ cm^{-3}$), acting as deep donor state, as demonstrated through the Fermi level position of nitrogen doped layer used in Schottky-pn diodes [238]. Even if, due to an ionization energy of $> 1.7eV$ [94, 239], nitrogen doped diamond is devoid of free electron at room temperature and thus insulating, a pn-junction is formed between the n-type diamond substrate and the p-channel inducing a SCR in the latter.

I.3.2.b JFET using nitrogen doped substrate as gate

This parasitic partial depletion of lateral bulk transistors conduction channel, induced by the substrate, has been suggested in the PhD of T.T. Pham [240]. Even if it has been observed before (fig. I.22 (b) and (e)), it has never been discussed in the literature earlier. Initially treated as parasitic effect for MOSFET or MESFET lateral device, C. Masante demonstrated in his thesis [58] that the pn diode, formed by the Ib substrate (500 μm thick) and the boron doped epitaxial layer, can be modulated intentionally, thanks to high temperature or illumination as the few ionized donors are enough to allow for charge transfer from SCR. Sample fabricated, named GD-030, and affiliated transistor characteristics of this previous work are reported in fig. I.23. The main JFET breakthrough, incomplete n-type layer ionization, has been solved through the application of an external energy (e.g. optical or thermal energy) on the device, which can be decorrelated from electrostatical control of the transistor.

With this innovative milestone, the gate control can be tuned active/inactive, with application of external power, or inactive under the dark at room temperature, allowing the conception of a non-volatile photo-switch [241]. Nonetheless, the JFET presented in fig. I.23 (a) has not been designed for this purpose, thus the structure as presented was not optimized for non-volatile memory application. Thick Ib diamond substrate, even under illumination or high temperature, is still highly resistive as well as backside gate contact. It induces a large internal gate resistance that lowers the transistor dynamic and thus hampers its competitiveness for other applications. Although the first NVPS demonstration has been made possible thanks to substitutional nitrogen contained in the Ib substrate, its first design is also its main limitation factor. As major part of this manuscript, better trades-off have thus been taken concerning its architecture to optimize its light collection efficiency such as its power throughput. Mainly, a highly phosphorus-doped thin layer has been added to the transistor stack, between the p-channel and the Ib substrate, such as the gate contact have been brought closer to the active area of the transistor.

I.3.2.c Diamond based non-volatile photo-switch presentation

Conventional FETs operate by controlling the conduction channel's depletion or population through a gate bias voltage for analog or digital operations. In contrast, the proposed non-volatile photo-switch (NVPS) is an hybrid structure where, the external illumination activates or freezes the state of the device. In typical semiconductors with shallow donor or acceptor energy levels, doping level and carrier concentrations are nearly equal at room temperature, resulting in conductive materials. However, in nitrogen-doped diamond, deep nitrogen donor levels preserve the insulating properties of diamond, even at high doping levels (above 10^{19} cm^{-3}), preventing the layer from every electrical driving. This state is referred to as the freeze state of the device, where absence of electrons in the nitrogen-doped layer limit all the kinetics of the transistor. External illumination, by contrast, promotes some of the nitrogen-bounded electrons to the conduction band, increasing the free carrier concentration and transitioning the device into a conducting state, referred to as the active control state. The device can be electrically driven through application of a gate voltage, especially turned from ON to OFF or vice-versa, solely in this active control state. However, the transition from active to freeze control states still requires application of an external energy such as light excitation. It's important to distinguish this concept from photo-conductive semiconductor switch devices [242] that also benefits from the optically accessible, substitutional nitrogen donor level in diamonds [243]. Optically generated carriers most participate in conduction which means these devices require a high power pulsed laser source to be efficient. Oppositely, here photo-generated electrons are used to activate or passivate a pn junction, in order to control JFETs channel conductivity, as enlightened by Fig.I.24.

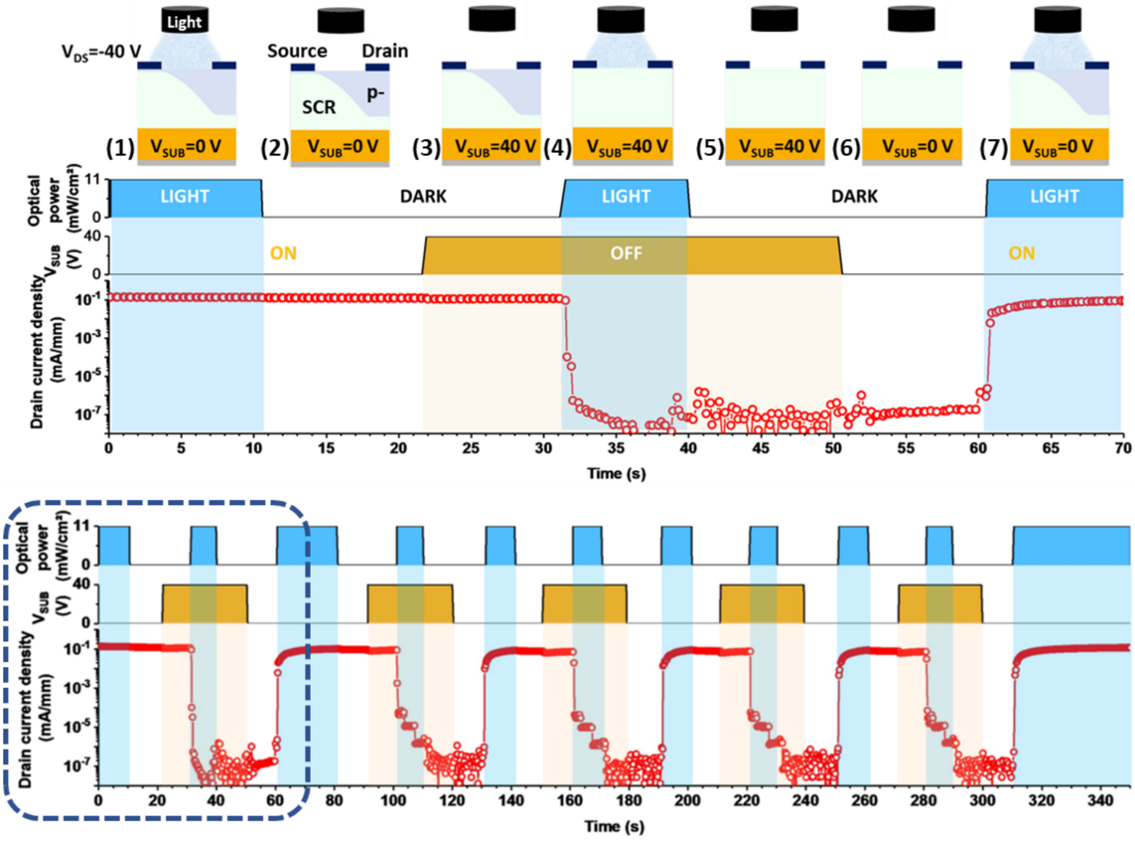

Figure I.24: (top), measured switched drain current density over one commutation cycle of the fabricated JFET under $V_{DS} = -40$ V, as function of the light (ON/OFF) and substrate (used as gate) bias. The device is only able to commute under an optical signal, and periodic repetition of the signals could have been reported (bottom). Courtesy to [241].

In this work, current flows through the bulk of the boron-doped layer, called in the later p-channel, between the drain and source contacts, maintained under constant bias. The Ib nitrogen-doped substrate function as the gate, where under optical illumination, the gate contact on the back side of the substrate controls the SCR extension in the channel. The typical pinched-off, ON-state, is schematized in Fig. I.24, where the extension of the SCR underneath the drain contact saturates the current flow in the p-channel, when the drain to gate bias approaches or is greater than the threshold bias ($V_{th} \approx 30$ V from Fig. I.23 c)). Ultimately, by biasing the substrate's backside under illumination gives rise to an extension of the SCR, resulting in a depletion of the channel, hence the OFF-state.

Fig. I.24 illustrates a measured commutation cycle under a fixed drain-to-source bias (V_{DS} = -40V, pinch-off) where optical control can freeze the device's electrostatics. The commutation cycle, splitted in seven steps are described below [241]:

(1) With the light on, the substrate-to-source is grounded ($V_{SUB} = 0$ V), establishing a bulk conduction channel between the drain and source, considering the normally-ON character of the fabricated JFET.

(2) When the light is turned off, the free electron concentration in the nitrogen-doped substrate becomes extremely low (freeze state). In an ideal scenario without compensation from acceptor ions at RT, the free electron concentration falls below 10^4 cm^{-3}. The hole current in the p-channel is negligibly affected and thus considered constant.

(3) Gate substrate is biased ($V_{SUB} = 40$ V) to fully deplete the channel (OFF-state). However, because the nitrogen-doped gate lacks free carriers in the dark, no electrostatic modulation is allowed from charge conservation at the edge of the SCR. Subsequently, the channel remains conductive, even if the gate voltage corresponds to an expected OFF-state. This first part consisting in half of the proof of non-volatility where a stored state (ON-state) cannot be changed by the control bias in the freeze state of the transistor.

(4) The light is turned back on, providing the optical trigger signal to activate the device (active control state), it responds to the electrical gate command previously imposed and maintained, and switches to the OFF-state. The channel becomes fully depleted, and the drain current drops below the detection limit.

(5) Turning off the light returns the device to the freeze state, where no addressing remain possible through electrostatical control.

(6) Applying a gate electric command to switch the device to the ON-state ($V_{SUB} = 0$ V) doesn't change the channel's insulating state due to the absence of optical excitation. This particular point is the second part of the non-volatility proof, particularly this step affiliated to the robustness of the memory which rely on the capability of the memory to conserve its current state after the removing of every control power supply.

(7) When the light is turned back on (active state), the device switches to the ON-state, perfectly recovering its initial state.

This sequence was repeated several times, as shown in Fig. I.24, to ensure measurement reliability. Although the first cycle may appear different, all subsequent cycles exhibited the same characteristic. However some challenges need to be addressed concerning this innovative device in order to pave the way for numerous practical applications where the superior properties of diamond semiconductors can be advantageously exploited. The threshold voltage should be reduced while optimizing the threshold voltage vs. ON-state resistance trade-off, as presented for example for lateral diamond MOS-gated FET in [244]. Nonetheless, this large threshold voltage in the device demonstrated here does not have any impact on the electro-optical control presented herein-above, it still greatly impact its range of application prospect were low control power is essential. Furthermore, the large RC time constant and, more precisely, the huge internal gate resistance caused by the high substrate's thickness and resistivity meant that the turn-on and -off time were long ($\geq 1-2$ s) compared to other FET architectures. To overcome these challenges, addition of a thin phosphorus-doped diamond layer was considered and presented in this manuscript. The lower activation energy of phosphorous compared to nitrogen, coupled to an optimized device design, is reported to efficiently lower the internal gate resistance. Subsequently, a gain has been reported on the commutation time without any increase in gate leakage current or impact on the robustness of the memory.

I.4 Summary & conclusion

The unique properties of diamonds, explored along this first chapter, have maintained our fascination of this material through the ages. Beyond its popular association with ornamental jewelry, wealth, and unbreakability, a deeper insight into its microscopic physical properties gave the foundations that underlie the macroscopic characteristics of diamonds. These properties make diamond one of the most versatile and potentially high-performing materials across a wide range of applications, like embedded power electronics, bio-electronic or quantum communication, that are in constant demand for next-generation innovative devices. While diamonds are commonly seen as insulating materials, successful doping transforms them into ultra-wide bandgap semiconductors. The incredible combination of physical and electronic attributes, such as high breakdown voltage, exceptional thermal conductivity, low dielectric constant, and radiation resistance, sets diamond apart. It's essential to emphasize the term "combination" because no other material comes close to matching diamond's blend of mechanical, thermal, electrical, optical, and chemical properties.

Diamond-based Junction Field Effect Transistors (JFETs) leverage these outstanding properties, boasting maximum electric fields (5.2-6.5 MV/cm) that approach the theoretical limit (10 MV/cm). They also handle high current ratings (600 A/cm^2) at elevated operating temperatures (500 K), where many other power-oriented semiconductors face challenges. However, prior designs restricted the active area, limiting the maximum ON-current to just 2 µA above 500 K and the room-temperature (RT) breakdown voltage to over 600 V. Although these results still fall short of the technical requirements for power devices, progress has been made over the past decade in diamond growth, doping, and overall fabrication. This progress has paved the way for larger-scale active areas in JFETs. This specific aspect is a focal point in this thesis, where interdigited JFETs, expanding the drain-to-source active area, have been manufactured to demonstrate that diamond devices have reached a level of maturity that allows for up-scaling. This positions diamond devices to compete with other more established and commercially available Wide Bandgap Semiconductors (WBGs) like SiC and GaN.

Another significant aspect of this thesis focuses on the design, production, and evaluation of the recently introduced Non-Volatile Photo-Switch (NVPS). Although this novel added switchable state was initially perceived as a disruptive factor in lateral MOSFET power devices, it has been further explored in this thesis for its potential memory applications. Devices dedicated to substantial uses of this effect were conceptualized, fabricated and characterized and results are transmitted inside this manuscript. The high internal gate resistance, responsible of extended commutation-time, initially reported for this device, were systematically decreased by closering of the gate electrode contact and are expected to be further enhanced by introduction of a thin highly phosphorus-doped layer. Importantly, these optimizations are also highly beneficial for large-scale interdigited transistors and their power electronic applications prospects. Even if some trade-offs concerning crucial parameters for each application remain, each design position taken are justified in the second chapter, and these choices impacts are reviewed in the last chapter of this manuscript.

Chapter II

Building blocks for diamond JFET: from theoretical model to device conception

This second chapter provides a comprehensive exploration of the design considerations for large-scale NVPS devices. It delves into the intricacies of the sustainable fabrication processes, the optimization of device parameters, and the expected performance characteristics. Given the early-stage success of realizing a diamond-based non-volatile memory within this thesis, this chapter concentrates on the fundamental building blocks that have been incorporated to enhance the device's functionality. Additionally, it extends into the development of large-scale devices through an interdigited architecture to align with the requirements of the power electronics market. Numerous parameters, spanning the domains of diamond growth and device geometry, necessitate careful adjustment to align with the expected performance criteria for the final component. These adjustments often involve trade-offs among various parameters. Therefore, a comprehensive understanding of the underlying physics of diamond, particularly in the context of JFETs, even within a simplified 1D model, is indispensable. This understanding serves the dual purpose of evaluating the potential of diamond-based devices and providing a foundational framework for comparison with experimental results.

II.1 Structure and fabrication process overview

Four samples have been fabricated using process reported in fig. II.1. Two of them, named PS1 and PS2, benefits of the thin highly phosphorus-doped layer, as presented on the right hand side. The two others, NS3 and NS4, presented on the left hand side, reproduce the reference sample GD-030 [58], but the back-gate metallic contact is taken on the frontside of the sample, with an inter-digited architecture that will be presented in the next section. The p-channel properties have been chosen identical to the reference GD-030, demonstrated in Fig. I.23. As first advantages, it benefits of the already optimized trade-off between its doping level and thickness, targeted to be $N_A = 1 \times 10^{17}\ cm^{-3}$ for a 400 nm thick layer. Assuming an acceptable doping level deviation, reported at $N_A = 2 \times 10^{17}\ cm^{-3}$ by C-V measurements, the same recipe has been used in this work, where growth parameters are expected to provide a doping level ranging between $N_A = 1 - 2 \times 10^{17}\ cm^{-3}$. Subsequently, it opens comparative study that enlighten the impact of both, back-gate with a frontside contact and/or the dopant used for this layer.

Process flow main steps are described in fig. II.1, and are composed as follow:

(i) Active channel growth: Epitaxy, performed by Microwave Plasma-enhanced Chemical Vapor Deposition (MPCVD), of a 400nm thick boron-doped layer (targeted doping level $N_A = 2{\times}10^{17}\ cm^{-3}$). Used as conduction channel for JFET, the four growths have been performed with

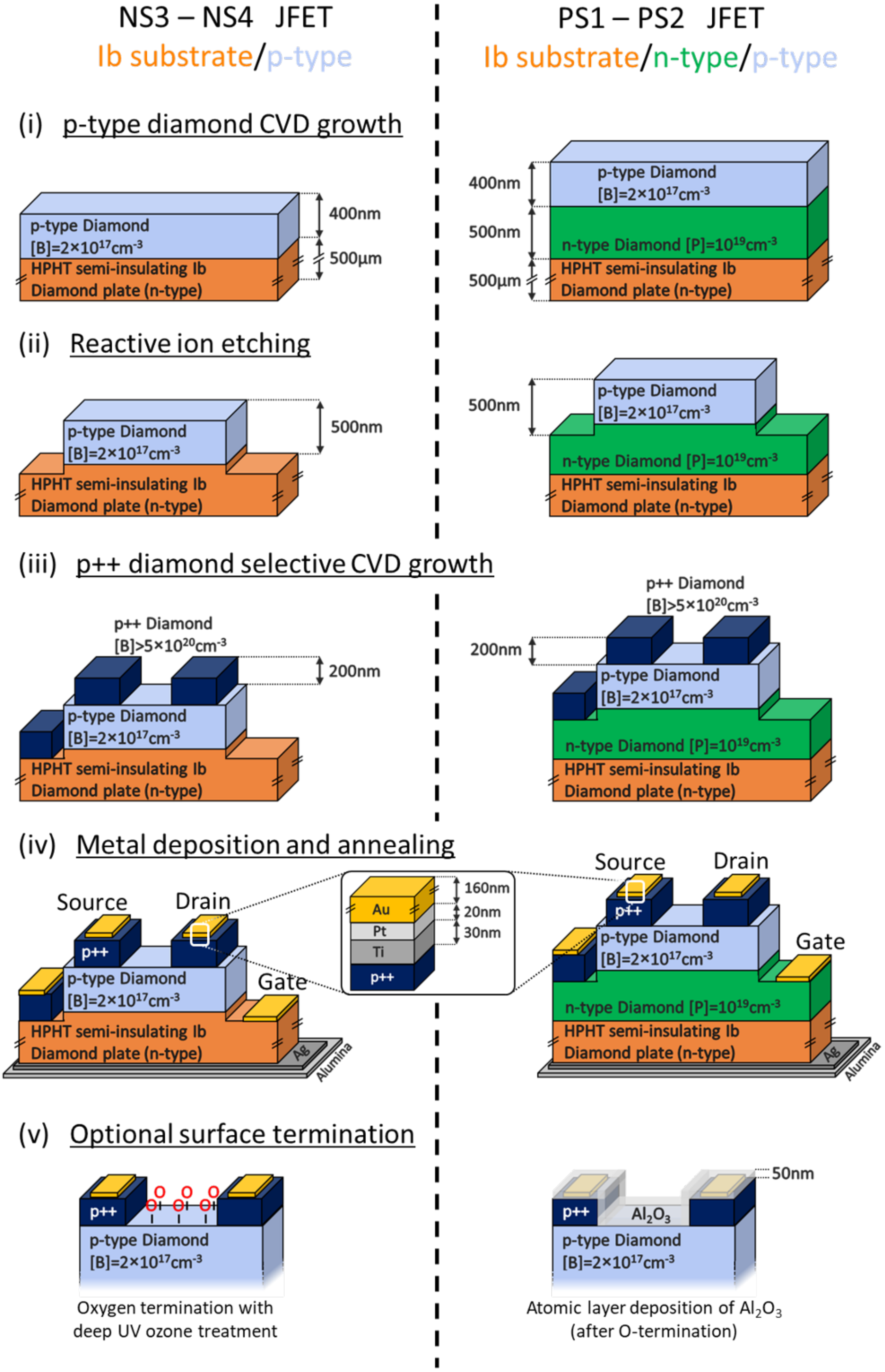

Figure II.1: Schematic cross sections at the main fabrication steps of diamond JFET using Ib substrate, on the left, or (100) highly phosphorus doped layer, on the right, as gate.

the same recipes as reference sample GD-030 [58]. Typical resistivity for layers corresponding to the same recipe are in the range of $2-70$ Ω.cm [244, 245], depending on compensation measured.

(ii) Mesa-etching of the channel: Inductively Coupled Plasma - Reactive Ion Etching (ICP-RIE) using CF_4 and O_2 gases in order to etch 550 nm from the top face of the sample and isolate p-channel mesa structures. Etching went down to the substrate, or phosphorus-doped layer for sample PS1 and PS2, in order to isolate multiple JFET that can be further paralleled and to allow gate contacting from the top face. Thick nickel mask has been used to protect the non-etched area, and samples were cleaned with hot acid mixture to remove graphitic phases and surface contamination, before and after this process.

(iii) p-type ohmic contact: Selective growth of 200 nm thick heavily boron-doped diamond using MPCVD. The boron concentration targeted $[B] > 5 \times 10^{20}\ cm^{-3}$, is higher than metallic transition level [138, 139, 246] and thus, an ohmic contact resistivity of the order $10^{-5} - 10^{-7}$ Ω.cm^2 [247, 248] is expected.

(iV) Metallic contact deposition: Source, drain and front gate contacts were defined by laser lithography and then deposited by metal evaporation, followed by an annealing at 500 °C at high vacuum ($< 10^{-7}$ mBar) during 30 min to allow carbide formation. The metallic stack is composed of: titanium for diamond adherence (30 nm), then platinum (20 nm) to avoid titanium/gold inter-diffusion and finally gold (160 nm) to facilitate wire-bounding and protect the contact from being oxidized. As metal/semiconductor contacts play a crucial role in the overall structure, section II.5 provides a detailed exploration of their significance and properties.

(v) Surface termination: An oxygen termination, by deep UV ozone technique, have been realized on the four samples in order to passivate diamond surfaces. Highly resistive behavior of the p-channel can be due to uncontrolled partial depletion of the p-channel caused by Fermi-level pining from the top face of the stack. For this purpose, an optional Atomic Layer Deposition (ALD) of alumina could have been performed in the case of an absence of conduction between source and drain contact.

Table II.1: Summary of the four samples fabricated during this PhD and reference sample GD-030, with the fabrication parameters targeted.

	PS1	PS2	NS3	NS4	GD-030
Substrate	(100) Ib HPHT $4 \times 4mm^2$				
Gate layer	Phosphorus $[P] = 10^{19}cm^{-3}$ $t = 500$ nm		Substrate, Nitrogen $[N] = 10^{19}cm^{-3}$ $t = 500\ \mu m$		
p-channel	400nm thick boron doped $[B] = 2 \times 10^{17}cm^{-3}$				
Surface termination	Oxygen				
Surface passivation	Al_2O_3 50 nm	No	No	No	Al_2O_3 50 nm

Table II.1 summarizes the key parameters targeted for the four samples fabricated in this thesis and the previously achieved sample GD-030. Compared to previously reported JFET [228, 230, 233–236], the use of Ib substrate instead of epitaxial growth of nitrogen doped layer used as gate, facilitates the fabrication process of the whole transistor stack. Diamond fabrication process is not an easy task due to the non-standard size of its substrates ($4 \times 4 \times 0.5$ mm^3), compared to other material like SiC where 6-inch substrate with low dislocations density are commercially available [249]. Clean room facilities have been adapted to this unusual shape but, lowering the number of fabrication steps, reduces the total number of critical failures that can still happen during clean room processes and thus facilitating the reproducibility of the samples. Simplification of the fabrication process also enabled complexification of lithography mask that have been used in order to realize large-scale devices presented in the next section.

II.2 Mask design

Several JFET transistors and characterization devices (e.g. TLM structures discussed in section II.4.1) with varying sizing parameters were created within the half of each 4×4 mm^2 substrate, as shown in fig. II.2.

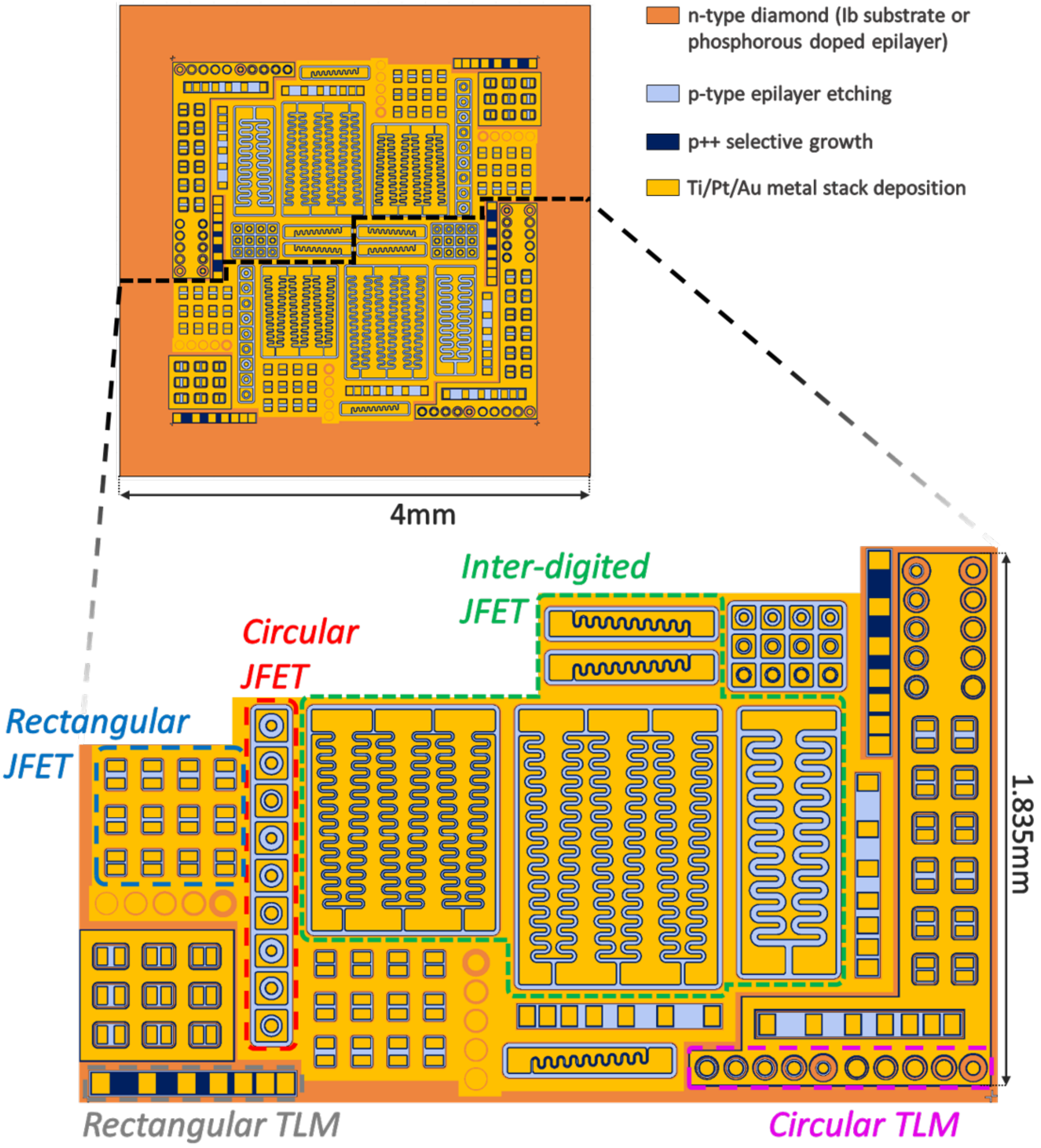

Figure II.2: Overview of the designed mask, on top, and zoom on one of the two identical patterns on the bottom. Non-highlighted patterns are variations of the different JFET or characterization devices reported on the mask.

These devices were duplicated two times, with a sufficient margin of 400 μm from the substrate's edges. This precaution was taken due to challenges in achieving a uniform layer of photo-resist in this specific area during the spin-coating process. Typically, a safe margin of 500 μm is maintained; however, by introducing a cleaning step into the spin-coating process (consisting of 30 seconds of spinning with a droplet of acetone followed by 30 seconds of spinning with a droplet of Iso-Propyl Alcohol at 6000 RPM), a more uniform deposition of resist could be achieved up to 300 μm from the sample edges. Consequently, by reducing the safe resist margin by 200 μm, the usable area of the substrate increases by 1.24 mm^2, equivalent to 8% of the total substrate surface. A compromise was made to maintain a margin of 400 μm in order to ensure a uniform resist deposition and achieve better reproducibility, even at the cost of reducing the available surface area (3.2×3.2 mm^2) for device fabrication.

Non-uniformities in the characteristics of actives layers, impurities, point or volumic defects, or also imperfections induced during fabrications process, could significantly impact large-scale devices. Even if these statements are valid for every semiconductor materials, diamond is still even more impacted due to the small size of available substrate. It has been well emphasized by Umezawa et al. [121] where larger Schottky diodes face lower breakdown electric field, due to leakage current density increase, such as specific ON-state resistances and ideality factors non-uniformities across the sample. This study has shown that designing multiple individual devices on the same substrate, rather than larger devices, offers a safer approach to achieve high current density or reduce electric field crowding in the off state. However, this approach comes with the limitation of being unable to reach high absolute current values or high breakdown voltages, due to the constraints imposed by the small scale of the devices.

However, in order to answer power electronic market requirements summarized through the key value of reaching 1 A in the on-state and sustain 1 kV in the off-state, large-scale diamond devices will, at some point, be necessary. For this reason, large area inter-digited diamond JFET has been designed and will be detailed in subsection II.3.4. This innovative design for diamond has been placed in the center of the mask to lower the impact of lithography misalignment but also to benefit of a better homogeneity in the p-type layer characteristics. The later being strongly dependent on the growth reactor used (CVD plasma shape), but also substrate roughness and off-angle [250]. A compromise was made, taking into account the previous work conducted by Umezawa et al. [121], and a considerable number of single individual JFETs were designed across the outer region of the 3.2×3.2 mm^2 available fabrication surface. These single JFETs will be discussed in the next subsection, II.3, as they enable comparative studies (with inter-digited transistors) and statistical characterization due to the abundance of similar devices available.

II.3 JFET geometry and SCR morphology

Two designs have been chosen for the single JFET architecture, presented in fig. II.3, and distributed across the mask, with various drain to source length L_{SD} among: 5, 10, 15 and 20 μm. While lateral circular-shaped JFET architectures have been extensively developed for materials such as Si [251, 252] or SiC [253], this is the first implementation of such architecture for diamond.

Circular JFETs based on silicon have been developed due to their radiation hardness in power conversion modules, or for their low-noise detection capabilities. These JFETs take advantage of a vertical architecture, where an array of cylindrical transistors, connected in parallel, are controlled by the lateral extension of pn-junctions. Compare to silicon, vertical diamond transistor has still not been reached but diamond, composed of the lightest carbon group elements is already considered as the best semi-conductor for harsh environment operations [254, 255]. Before achieving a breakthrough with diamond vertical JFETs, a study on the impact of SCR morphology on the key parameters of the transistor has been conducted in this manuscript. Additionally, for memory applications, the circular shape has shown a reduction in the loss of robustness in the frozen-off state, as discussed further in section IV.4.

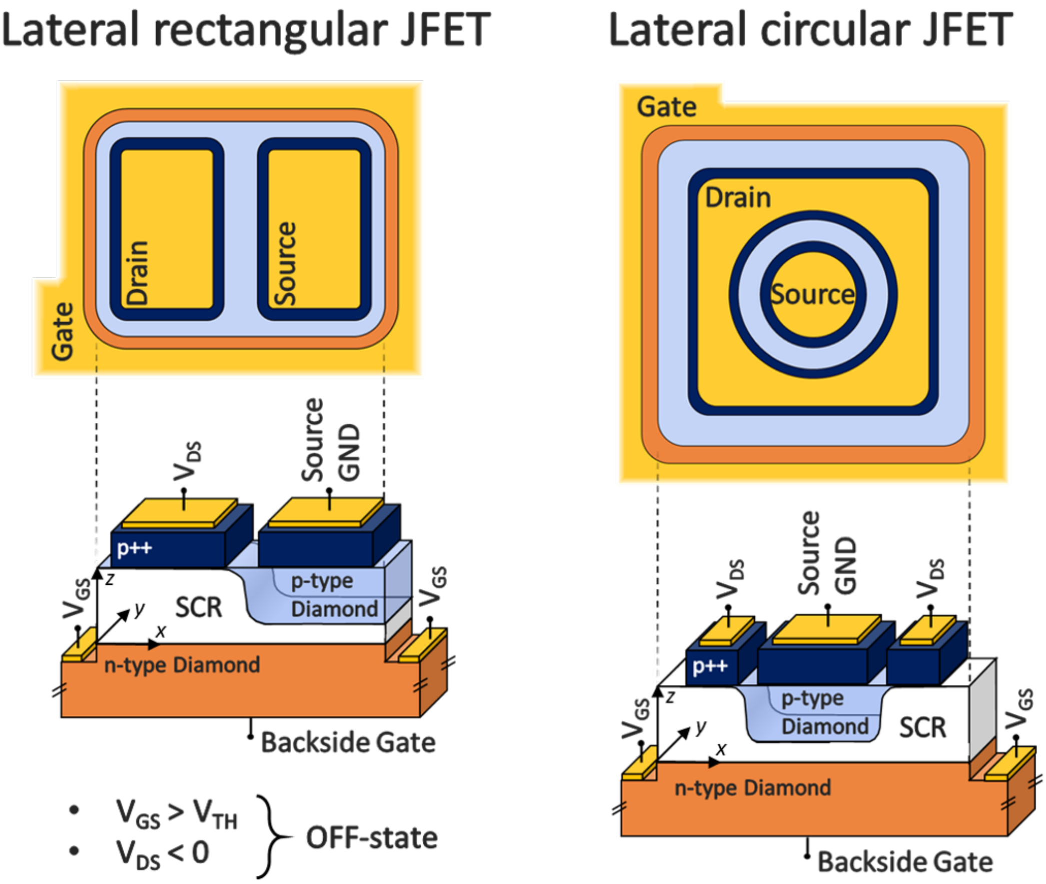

Figure II.3: Top views of a lateral rectangular-shaped or circular-shaped JFET with their cross-sectional schematic views on the bottom. Scale reported in the figure has been maintained constant but source to drain spacing varies.

II.3.1 Space Charge Region dimensionning

Electrostatic control of the designed JFET is achieved through the polarization of an abrupt vertical pn-junction. This diode, composed of two oppositely charged semiconductors, must be ruled by charge conservation at thermal equilibrium. Meaning that, in order to have conservation of charge neutrality, the fixed negative charge developed in the p-side must be equal to the fixed positive charge in the n-side or:

$$\iiint_{V_{SCR,p}} |\rho_p(x,y,z)|\,dx\,dy\,dz = \iiint_{V_{SCR,n}} |\rho_n(x,y,z)|\,dx\,dy\,dz \tag{II.1}$$

Where ρ_p and $V_{SCR,p}$ are respectively the charge density and the depleted volume associated in the p-side (depicted in fig. II.3), and ρ_n and $V_{SCR,n}$ the same variable for the n-side of the abrupt junction.

Equation II.1 being valid in three dimensions, whatever the doping level or ionization fraction, some hypothesis can be done to reduce its dimensionality dependencies. First, by definition of the depleted region, no free carrier are available in this volume due to intense electric field. This statement is not totally true if we consider the existence of the Debye length, where, due to electrical field continuity at the edge of the SCR, hole can penetrate in the SCR near its p-type edge, and the same is true for electrons near the n-type edge of the SCR. But as this phenomenon does not disturb the potential equilibrium, it will not be taken into account for a first approach. Secondly, the doping profile of both region is assumed homogeneous along the plan parallel to the abrupt junction (x,y). This assumption takes into account the size of the designed transistor compared to layer doping inhomogeneities reported for diamond [250]. Thus, the charge equilibrium of equation II.1 can be reduced as:

$$\int_0^{W_{SCR,p}} N_A(z)dz = \int_0^{W_{SCR,n}} N_D(z)dz \tag{II.2}$$

The total width of the depletion region, denoted as W_{SCR}, is determined by the extensions of the SCR in the p-side $W_{SCR,p}$ and n-side $W_{SCR,n}$ of the abrupt junction (in non punch-through configuration). This can be expressed as $W_{SCR} = W_{SCR,p} + W_{SCR,n}$, as shown in the inset of fig. II.4. Based on equation II.2, the extension of the depletion region is primarily determined by the distribution of doping densities, $N_A(z)$, in the p-type region and $N_D(z)$ in the n-type region. It should be noted that the equation as reported, does not account for fixed charges that act as traps in the diode, which may be present as impurities but not as dopant. Among this uncontrolled impurities, specific attention should be paid to compensation, which gather the main oppositely charged impurity incorporated in both side, hence acceptor-like defects in n-side and donor-like defects in p-side. Neglected in charge equilibrium used in equation II.2, if the compensation density due to fixed traps is significant compared to the doping level, it should be included within the integral over the distance from the abrupt junction (z).

II.3.1.a Nitrogen doped samples, homogeneous dopant concentration

In general case the doping density is considered homogeneous, which mean a concentration of donor and acceptor constant in their respective regions ($N_A(z) = N_A$ and $N_D(z) = N_D$). In this case [208, 256], equation II.2 can be simplified as follow:

$$N_A W_{SCR,p} = N_D W_{SCR,n} \iff \frac{N_A}{N_D} = \frac{W_{SCR,n}}{W_{SCR,p}} \tag{II.3}$$

Form chosen on the right hand of equation II.3 enlightens the doping level trade-off that rules SCR extension in both part of the junction. If $N_D >> N_A$ implies that $W_{SCR,p} >> W_{SCR,n}$ and vice-versa. For samples NS3, NS4 and GD-030, where $N_A = 2 \times 10^{17} cm^{-3}$ and $N_D \simeq 10^{19} cm^{-3}$, the dopants concentration ratio $N_A/N_D \simeq 0.02$ indicates that 98% of the full depletion width is in the p-type layer, justifying the further approximation $W_{SCR} \simeq W_{SCR,p}$. This equality, relevant as a first approximation for an ideal junction, must nonetheless be considered in the context of significant compensation, especially when there is a substantial mismatch in compensation between the two layers. Indeed, the decrease in effective charge resulting from a significant density of compensating impurities can noticeably impact $W_{SCR,p/n}$ by varying from a few to several tenths of a percent. Therefore, this aspect should not be disregarded in the concern of diamond and in general, as demonstrated in section I.2.2.e but it also does not have high influence on low compensated layers.

Thanks to the use of equation II.3 and the solution of Gauss-Poisson equation, the depletion width of the SCR in non punch-through configuration can be expressed:

$$W_{SCR} \simeq W_{SCR,p} = \sqrt{\frac{2\varepsilon_{SC}}{eN_A(1 + N_A/N_D)} V_{bi}} \tag{II.4}$$

Where ε_{SC} is semiconductor specific dielectric constant that can be expressed as $\varepsilon_{SC} = \varepsilon_r \cdot \varepsilon_0$, product between semiconductor relative permittivity ($\varepsilon_r = 5.7$ for diamond) and vacuum permittivity (ε_0). Additionally, V_{bi} is the built-in potential, corresponding to Fermi levels difference between the p-type and n-type regions, under equilibrium with no external bias. Also named diffusion potential, it represents the balance between the electric field due to the fixed charges in the depletion region and the diffusion forces due to the concentration gradient of majority carriers. Acting as a potential barrier that controls the flow of majority carriers across the junction, it is expressed for non-degenerate semiconductor:

$$V_{bi} = \frac{k_B T}{q} \ln\left(\frac{n_{n0} p_{p0}}{n_i^2}\right) \tag{II.5}$$

Where $k_B T$ is the thermal energy, defined as product of Boltzmann constant k_B and the temperature T, and n_i is the intrinsic carrier concentration which is considerably low for diamond ($\approx 10^{-27}$ cm^{-3}) compared to silicon ($\approx 3 \times 10^{10}$ cm^{-3} at RT) due to the large band-gap. Densities n_{n0} and p_{p0} are the n-side bulk electron and p-side hole concentrations, respectively, in the neutral region at thermal equilibrium and without external excitation. One can remark that through the use of these densities incomplete ionization of doped diamond is accounted. For samples NS3, NS4 and GD-030 using concentration mentioned above, at room temperature $V_{bi} = 4.1$ V yielding a built-in SCR extension $W_{SCR}(0V) = 112$ nm which correspond to 28% of the width of the p-type layer t_p. It means that 72% of the p-channel should be conducting and 28% insulating at RT.

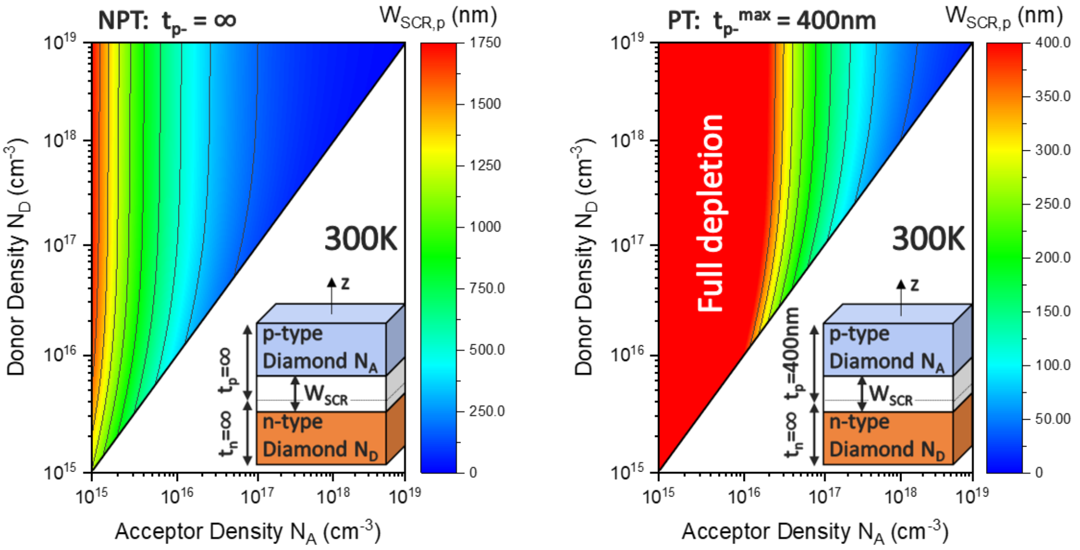

Figure II.4: Extension of the depleted region in the p-side $W_{SCR,p}$ as function of the dopant concentration in both part of the non-biased pn-junction represented in the inset. Left hand figure is in non-punch through configuration and right hand figure is in punch through by fixed p-type width of 400 nm.

This calculation demonstrates that a normally-OFF transistor can be easily designed by maintaining the same doping level and only adjusting the p-channel thickness t_p. This assertion must be supplemented by insisting on the neglect of compensation. In cases where compensation is no longer a minor consideration, the balance of depleted charges and, consequently W_{SCR}, is significantly affected. Insufficient control over compensation, on either side, carries a high risk of having, in the best scenario, a normally-ON transistor that was intended to be normally-OFF, and in the worst case (with very strong compensations), a completely blocked transistor (no modulation of p-channel conductivity within reasonable voltage ranges). However, while normally-OFF transistors and low threshold voltages are almost mandatory for power electronics, this design choice is hindered by a trade-off that affects JFET performances. It particularly impacts the ON-resistance and blocking voltage capabilities of the devices due to the limitations of the SCR extension in the p-channel, usually known as the punch-through design (PT). The lateral architecture developed within the context of this thesis, refer to conduction between drain and source contacts placed on the same plan as the substrate main orientation (plan (x, y) in Fig. II.3), whereas conductance modulation is brought by vertical depletion of the p-channel (z axis). In this case, the PT design refer to the limited vertical extension of the SCR, within the p-channel, due to the finite thickness of t_p, mandatory to obtain an OFF-state regarding the p-channel doping level. Head-on demarcation needs to be done between PT design without applied bias, hence normally-OFF transistors, and PT that can be reached during avalanche breakdown at high external voltages.

Figure II.4 shows simulation results for the depletion extension in the p-type region with two configurations, non-punch trough (NPT) and PT design depending on both sides dopant concentration without bias application. PT design gives a rise to a lower ON-state resistance for the same doping level compared to NPT design. At the opposite, in the latter design, only a part of the p-type layer is depleted and withstand the total voltage in case of an avalanche breakdown. To efficiently compare the two configuration, PT and NPT, analysis must be carried out at the same voltage withstand. This latter comparison has been done by Chicot et al. [257] where, for the same fixed voltage withstand, fabricated devices thicknesses and therefore doping are inevitably different. It enlightens the presence of an optimum truncation coefficient which, for a given voltage withstand, minimises the total on-state resistance. Nonetheless, this optimum truncation coefficient is different between a unipolar component (without conductivity modulation) and a bipolar component, considering injection of minority carriers which modulate the voltage withstand zone.

II.3.1.b Electric field distribution in Ib substrate based pn-junction

Blocking voltage capability, which is crucial parameter for power devices and has been discussed several times in this manuscript, is governed by the electric field distribution across the vertical pn junction formed between the substrate and the p-channel for the NS3 and NS4 samples. Notably, when the Ib substrate is kept in the dark at room temperature, a significant potential difference can be sustained between the drain and the substrate due to the insulating nature of the latter. Even when applying 1 kV to the drain electrode of reference sample GD-030, no measurable current could be detected. In this scenario, the potential drop occurs across the full thickness of the substrate ($t_{sub} = 500\ \mu$m), and the estimated electric field of 20 kV/cm remains low compared to the critical electric field of 10 MV/cm for diamond.

Change undergoes when the substrate is activated by illumination or thermal energy, through generation of free carriers inside the latter, which in turns strongly modifies voltage drops along the stack. In this case, the potential drop is assumed to be held by the thin p-channel layer which, sooner or later, leads to breakdown of the device. The critical electric field reached at breakdown of the p-channel as function of the depth is presented in fig. II.5 for different layer depths t_p and different doping levels. Calculations have been performed by N. Rouger using the optimized routine adapted for diamond [258], considering impact ionization coefficients from [130].

As expected for a pn-junction, the maximum electric field E_M is located at the p-type and n-type semiconductor junction boundary. Furthermore, for the PT design used in fig. II.5, the critical electric field E_C reached at breakdown of the junction is increasing with t_p shortening, as being related to the avalanche breakdown mechanism. Supporting that PT design strongly confines the electric field over the reduced layer depth, hence providing lower protection from avalanche breakdown for a define biasing condition.

Importantly, this 1D modelization considered that the upper limit for E_M is fixed by impact ionization effect, leading to avalanche breakdown. In a reverse biased pn-junction, especially under high field condition, minority carriers that diffuse in the SCR will drift and gain enough kinetic energy to ionize the lattice atoms. Consequently, one or more electron-hole pairs are generated through elastic collisions which, will in turns also be accelerated to generate more and more electron-hole pairs. This cascading phenomenon multiplies any small current I_0 by a multiplication factor M, given by [130]:

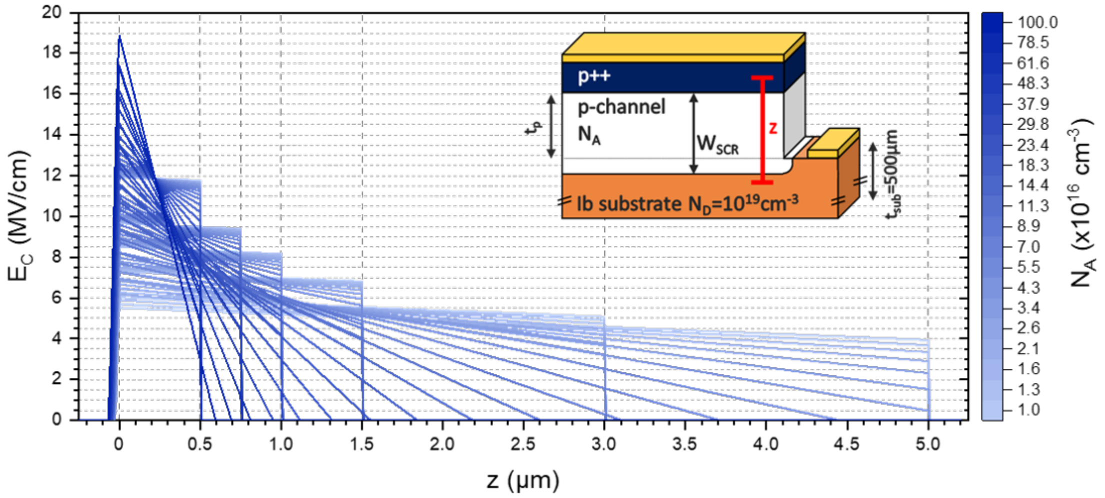

Figure II.5: Electric field distribution at avalanche breakdown, as function of the depth z in the Ib substrate based pn-junction for different punch-through configuration. Schematic cross section of the structure enlightens the cutline where computation have been performed using optimized routine proposed in [258]. The thickness t_p is varied over 0.5, 0.75, 1, 1.5, 3 and 5 µm such as the doping level with 20 log-spaced points between 10^{16} cm^{-3} and 10^{18} cm^{-3}

$$M = \frac{1 + k\exp\left[-\int_{W_{SCR,n}}^{W_{SCR,p}} (\alpha_p - \alpha_n)dz'\right]}{(1+k)\left(1 - \int_{W_{SCR,n}}^{W_{SCR,p}} \alpha_p \exp\left[-\int_{W_{SCR,n}}^{z} (\alpha_p - \alpha_n)dz'\right] dz\right)} \tag{II.6}$$

Where k is the ratio of an electron injection current I_{e0} to a hole injection current I_{h0}, α_p, and α_n are the ionization coefficients of holes and electrons, respectively. They represent the electron-hole pairs generated by a carrier per unit distance and are further bias dependent [259]. Junction breakdown occurs when mathematically M factor tends to infinity or when the ionization integral for holes I_p, tends to 1, such as:

$$I_p \equiv \int_{W_{SCR,n}}^{W_{SCR,p}} \alpha_p \exp\left[-\int_{W_{SCR,n}}^{z} (\alpha_p - \alpha_n)dz'\right] dz \to 1 \tag{II.7}$$

In literature, regarding diamond, this equation is displayed as hole-initiated avalanche breakdown and could be improved taking into account k ratio, displayed in equation II.6. Up to now, there is no accurate extraction of diamond α_n and α_p, such as temperature dependence establishment, in literature due to the difficulty to reliably measure the critical field of diamond, as it requires to minimize edge effects and leakage current in the fabricated test structures. Moreover, it would requires several samples, with different doping levels and drift region thicknesses, that ensure the obtainment of avalanche breakdown from the 1D vertical junction only to extract reliable ionization coefficients. At this development stage, this is particularly difficult with small-sized diamond devices, both for thick and lightly doped that gives rise to a low electric field but throughout a thick region, or thin and heavily doped diamond layers, exhibiting extremely high electric field in a tiny volume. However expression of this coefficient can be simplified in Chynoweth's form, according to the work proposed by Hiraiwa et al. [130, 260] which considers a geometric average of both electron and holes ionization rates, given by:

$$I_p = \int_{W_{SCR,n}}^{W_{SCR,p}} \alpha dz \to 1 \qquad \text{with } \alpha \equiv \sqrt{\alpha_p \alpha_n} = \sqrt{9.44 \cdot 10^4 \exp\left(\frac{-1.9 \cdot 10^7}{|E(z)|}\right)} \tag{II.8}$$

The absolute value of the electric field as a function of depth, denoted as $|E(z)|$, can be expressed using the Gauss-Poisson resolution of the 1D pn-junction model. It is worth noting that I_p is highly dependent on W_{SCR}, resulting in the critical electric field reached at avalanche breakdown being strongly dependent on the doping level, as illustrated in Fig. II.6. The critical field grows with the doping level from 3.8 MV/cm at $N_A = 10^{15}$ cm^{-3} to 9.5 MV/cm at $N_A = 10^{17}$ cm^{-3} for diamond. For comparison, 4H-SiC critical field varies from 1.8 MV/cm to 3.5 MV/cm for the same respective doping levels mentioned above. Even if diamond is better placed than 4H-SiC for high field handling, both totally out-perform silicon for off-state capabilities where the latter saturates at a critical electric field of 0.5 MV/cm at $N_A = 10^{17}$ cm^{-3}.

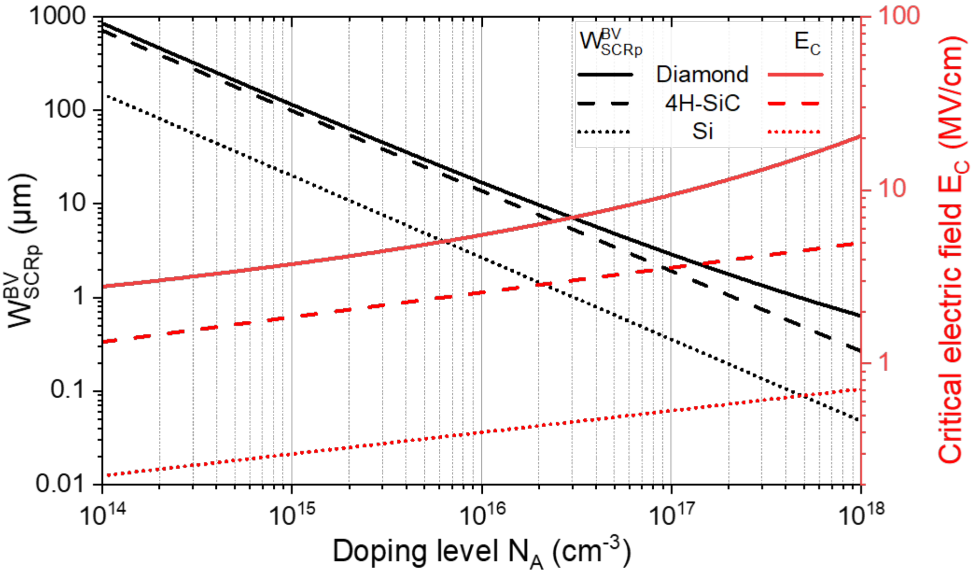

Figure II.6: Calculated room temperature critical electric field and associated pn-junction space charge region extension, reached at avalanche breakdown versus doping level, in non punch-through configuration using ref. [260] or for 4H-SiC and Si ref. [261].

The simple 1D non punch-through modelization is highly convenient for first approach device design but still induces strong hypothesis that could turn calculations inefficient when higher dimensions are considered. In equation II.6, only the minority carrier injection in the space-charge region are considered to give rise to avalanche breakdown. Furthermore in the same equation, contributions of holes and electrons are not accurately separated, as they could be by differentiating the multiplication factors dedicated to each. Additionally, the equation completely omits carrier generation inside or outside the SCR, whether due to thermal or optical energy. To account for photo-generated carriers, a dedicated multiplication factor, as proposed for Avalanche Photo-Diodes (APD) models [262], should be used. However, it is worth noting that such a modelization has still not been reported for diamond in the literature. Thermally-generated carriers inside the SCR have been taken into account in fig. II.5 by the implementation of a dedicated multiplication factor over the computation routine proposed in [257, 258]. Finally, when ranking semiconductors for their critical electric field at the same doping level, it may be less meaningful than comparing their maximal breakdown voltages for different doping levels, as discussed in the next section.

II.3.1.c Breakdown voltage: debut of WBG semiconductor ranking

Initially, when designing a power component, the associated technical specifications refer to target values for breakdown voltage and on-state resistance. In addition, volume and weight constraints may be added to these technical specifications, depending on the field of application (aeronautics, embedded electronics, etc.). In order to compare semiconductor materials effectively, it makes more sense to compare them on the basis of breakdown voltage equi-potentials and thus to classify them according to the constraints involved on the associated active layers (thickness, doping). Fig. II.7 (left) enlightens conductive layer requirement for a targeted breakdown voltage between 0.6 and 1 kV, using the trade-off between conductive channel doping level and the computed breakdown voltage for Si, 4H-SiC and diamond.

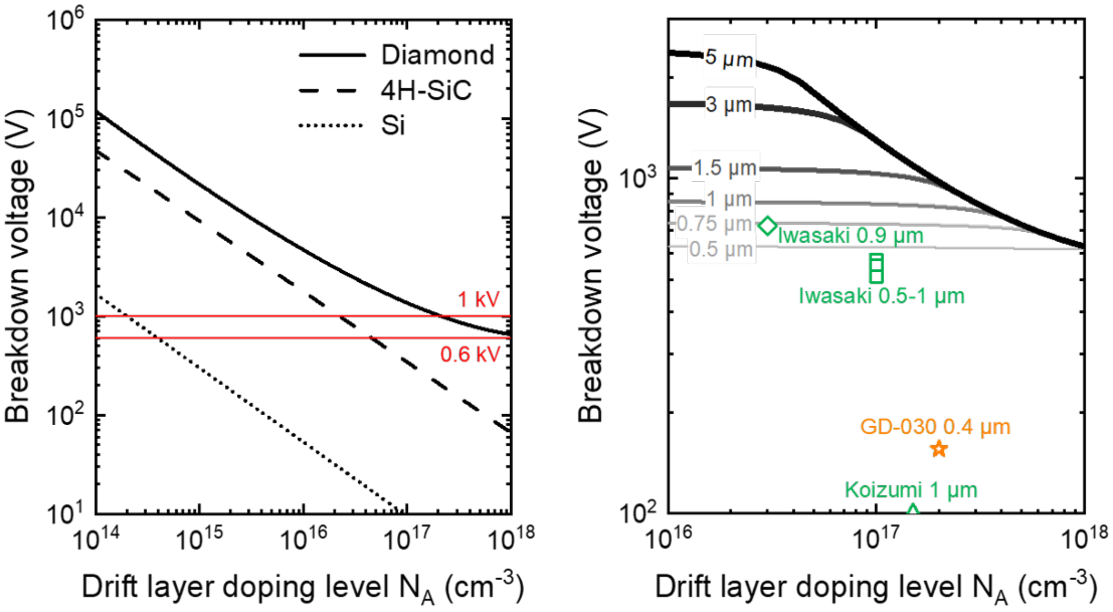

Figure II.7: Calculated room temperature avalanche breakdown voltage versus doping level. At left, in non punch-through configuration using ref. [260] for diamond and for ref. [261] 4H-SiC and Si. At right, in punch-through configuration for various p-type diamond epi-layer width, using calculation routine presented in ref. [258]. Experimental results reported in literature for various diamond-based pn-junction are reported in green for phosphorous doped n-type layer and orange for nitrogen, such as the p-layer width affiliated [230, 241, 263, 264].

The breakdown voltage, as being expressed $V_{BV} \propto E_C \times W^{BV}_{SCR,p}$ (both depicted in fig. II.6), decreases with the doping level N_A as the SCR thickness $W^{BV}_{SCR,p}$ is reduced for the same voltage. Based on the pn-junction modelization presented here, to target a breakdown voltage of at least 0.6 kV, doping level of the diamond conductive layer needs to be lower than $N_A = 10^{18}$ cm^{-3}, corresponding to a NPT layer width of at least 1.76 μm. As comparison, for the same targeted breakdown voltage it would require for 4H-SiC a maximum doping level of $N_A = 4.8 \cdot 10^{16}$ cm^{-3} corresponding to a NPT layer width of 3.55 μm, and for Si a maximum doping level of $N_A = 4 \cdot 10^{14}$ cm^{-3} for a NPT layer width of 44.2 μm. Consequently, to achieve the same target breakdown voltage, diamond requires only half the volume occupied by a SiC-based component. Moreover, with a remarkably close density for both materials (3.21 g/cm^{-3} for SiC compared to 3.53 g/cm^{-3} for diamond), diamond-based power devices could significantly weight twice less than their SiC-based counterparts while maintaining similar characteristics. This weight advantage holds particular value for applications in aeronautics and aerospace where diamond is promised to excel. Notably, the difference between SiC and diamond is even more pronounced when compared to silicon. Diamond devices utilize 25 times less volume and weight 16.5 times less than silicon-based components, for the same performances. Although in the above calculations only the active area of the components is taken into account, the reality may be slightly different if the thickness of the substrate required for mechanical reasons is accounted.

In addition to the advantages of weight and space savings, another crucial aspect to consider is the accessible doping range for diamond compared to its competitors when targeting a specific breakdown voltage. Since the resistivity of a layer is strongly dependent on the density of the free carriers it contains, which in turn is intrinsically linked to the doping level, diamond offers the potential for lower layer on-resistances compared to other materials for a targeted breakdown voltage. Moreover, the on-resistance of the diamond layer can be further reduced by adopting the punch-through (PT) design, which involves thinner layers. However, this comes at the cost of decreasing the breakdown voltage, as illustrated in Fig. II.7 (right). In a pure design context, disregarding any punctual or extended defects near the junction, there exists an optimum PT truncation coefficient η that minimizes the total on-state resistance at a given voltage withstand. For example, the NS3 and NS4 samples employ $\eta = 0.25$ (corresponding to a PT layer thickness of 0.4 μm compared to an NPT $W_{SCR,p}^{BV} \approx 1.5$ μm). According to the work done by Chicot et al. [257], the optimal η value for a breakdown voltage ranging between 1 kV and 10 kV is around 0.7 (± 0.2). While this deviation from the optimum value reported in previous work may seem significant, the choice of reduced layer thickness is mainly influenced by another trade-off, specifically between the threshold voltage and on-state resistance, which will be discussed in a later section. Importantly, the optimum truncation coefficient varies between unipolar components, without conductivity modulation, and bipolar components, where the injection of minority carriers modulates the voltage withstand zone.

The substantial benefits of diamond, surpassing other semiconductors like SiC or Si, highlight its outstanding potential as a promising material for next-generation, small, and lightweight embedded power devices. However, it is important to acknowledge that, to date, no diamond pn junction (identical in design to the approach proposed in this manuscript) has been reported to reach its theoretically designed breakdown voltage values. The most popular ones, including reference sample GD-030, are listed in Fig. II.7 (right) along with the associated PT p-layers thicknesses. While some measurements obtained by Iwasaki et al. [263] come close to the theoretical calculations, others are far from the expected breakdown voltage. This discrepancy can largely be attributed to the non-negligible presence of defects at the interface, which are not accounted for in the models presented above and lead to significant dispersion in the measured characteristics. The 1D modelization, while highly convenient for first approach device design, has its limitations. Well-known edge effects, such as extended defects in the vicinity of the junction boundary, can create localized peak electric fields, resulting in premature breakdown of the device. Furthermore, analytical solutions for predicting or preventing the formation of these defects are not available. To effectively account for these parasitic effects, extensive use of finite element simulation tools would be necessary. However, at present, such tools are not yet fully optimized for diamond semiconductor devices. Despite these challenges, the potential of diamond as an exceptional semiconductor material for advanced power devices remains promising. However, to unlock the full potential of diamond-based pn junctions, particular attention must be paid on the doping level and layer thickness control. The sensitivity assessment of these parameters directly highlights the strong impact that a potential standard deviation can have on the performance of fabricated JFET.

II.3.1.d Phosphorous doped samples, non-homogeneous donor density

The homogeneous doping level assumption simplifies the calculations and is relevant for a first approach, but in practical devices, the doping profiles are not abrupt, especially near the metallurgical junction. The non-homogeneous doping profile of a layer may result from a parasitic effect due to the doping conditions themselves, such as the Gaussian distribution characteristic of ion implantation doping, or may be required by the designer to minimise the lattice mismatch between two semiconducting layers. In diamond, phosphorus is much more voluminous than carbon, so producing a layer heavily doped with phosphorus involves a non-negligible change in the diamond's lattice parameter. To minimise the stresses imposed on the layer and the mesh mismatch with the epitaxial recovery of the p-type layer, a linear decrease in phosphorus concentration was chosen over the last 100 nm of the layer. The linearly graded junction should ensure a better junction quality, especially in terms of extended and punctual defect formation reduction in the vicinity of the junction.

In this particular case, equation II.3 coming from electric field continuity at the junction boundary, is not valid anymore and doping level gradient in the phosphorous doped layer needs to be accounted. The linearly graded doping profile is defined by $N_D = a \cdot z$ with $a = (N_D^{fixed} - N_D^{interface}/z_{grad}) = 10^{24}$ cm^{-4} where $N_D^{interface}$ is the doping level at the junction boundary and N_D^{fixed} is the constant doping level reached at a distance $z_{grad} = 100$ nm from the junction boundary. The resulting doping level distribution in the vicinity of the junction boundary is represented in fig. II.8 for PS1 and PS2 samples using the linearly graded n-type dopants concentration and NS3, NS4 as well as reference sample GD-030 using constant doping levels. In the same figure, the ionised dopant concentrations on either side of the pn junction, obtained by finite element simulation using Nextnano software, were added as a visual guide to the extension of the SCR for both cases. Solving the Gauss-Poisson equation in the case of a linearly graded n-type doping [208], juxtaposed with a constant p-type doping, with the strong hypothesis of full ionization, gives rise to an absolute electric field in both part expressed as:

$$|E_p(z)| = \int_0^z \frac{eN_A(z)}{\varepsilon_{SC}} dz = \frac{eN_A}{\varepsilon_{SC}}(z - W_{SCR,p}) \qquad \forall\ 0 \leq z \leq W_{SCR,p} \tag{II.9a}$$

$$|E_n(z)| = \int_0^z \frac{eN_D(z)}{\varepsilon_{SC}} dz = \frac{e \cdot a}{2\varepsilon_{SC}}(z^2 - W_{SCR,n}^2) \qquad \forall\ 0 \leq z \leq -W_{SCR,n} \tag{II.9b}$$

The computed field for both unbiased structure is depicted in fig. II.8 (dashed line of the bottom graph) for $-W_{SCR,n} \leq z \leq W_{SCR,p}$. Space charge region extension can be obtained through electric field continuity at the junction boundary (z = 0) as:

$$N_A W_{SCR,p} = \frac{a}{2} W_{SCR,n}^2 \qquad \Longleftrightarrow \qquad \frac{2N_A}{a} = \frac{W_{SCR,n}^2}{W_{SCR,p}} \tag{II.10}$$

In both cases, the maximum electric field E_C is reached at the junction boundary ($z = 0$ nm) and a linear field decrease for constant doping level value, or a quadratic decrease for linearly graded doping are evidenced. Additionally, impact of the linearly graded junction is, as expected, almost negligible inside the p-type layer. A small 5 nm difference between the extension of the both cases SCR, also reflected on E_C, which almost introduces no change in the PT limited breakdown voltage study conducted in the previous section. The main difference between the two cases is observed in the n-side of the junction where the SCR extension, without biasing, differs from 20 nm ($W_{SCR,n} \approx 2$ nm for constant doping level and $W_{SCR,n} \approx 22$ nm for linearly graded doping level). This difference, which is potentially negligible given its small value with respect to the thickness of the layer, nevertheless leads to a slight decrease in the capacitance of the layer. Using a straightforward approach, with large underlying assumptions, the capacitance of the SCR can be expressed as $C_{SCR} = \varepsilon_{SC}/(W_{SCR,n} + W_{SCR,p})$, giving $C_{SCR} = 37$ nF.cm^{-2} and $C_{SCR} = 44$ nF.cm^{-2} for linearly graded and constantly doped junction respectively. This 16% lowering of the capacitance coupled to the lowering of the internal gate resistance thanks to the use of phosphorous is expected to have a non-negligible beneficial impact on the commutation time of the fabricated transistors as it will be developed in the last chapter of this manuscript.

To counterbalance the relevance of diamond finite element simulation tools, Nextnano software was employed to model the two diodes described above, making use of its 1D Poisson's equation solver. The electric field resulting from these simulations is shown in fig. II.8 and demonstrates very good agreement with the analytical models presented in this section. The maximum electric fields are slightly lower than those obtained by analytic 1D modelling due to a spreading of the field close to the SCR boundaries, itself generated by the optimisation of the charge gradient. The use of the finite element method allows the incomplete ionisation of the

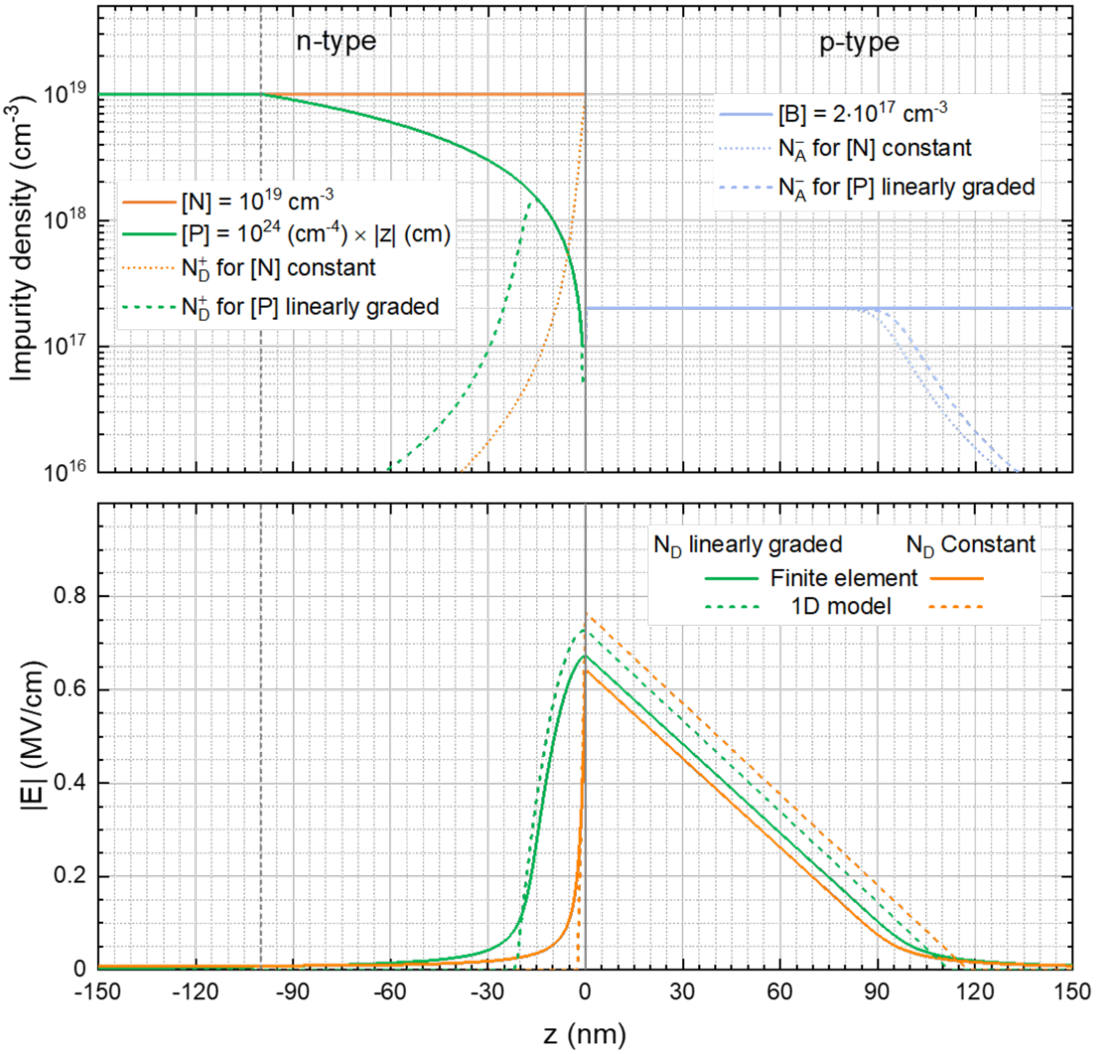

Figure II.8: On top, doping level distribution in the vicinity of the pn junction boundary, with constant n-type dopant distribution for sample NS3, NS4 and GD-030 in orange such as linearly graded distribution for PS1 and PS2 samples in green. Ionized dopant defining the SCR boundary, simulated by finite element method are displayed in dashed line. On the bottom, distribution of the electric field in the two types of diodes described above, using finite element simulation (full line) or analytical resolution of 1D model (dashed line).

diamond dopants to be taken into account. Thus, for static models, which do not consider either carrier generation or recombination, the results obtained are consistent for a first approach dimensionning. More complex simulation methods gives better resolution, especially near the edges of the SCR, opening for more in depth analysis with regard to the specific characteristics of diamond, but at a cost of more complexity and potentially over-weighted contribution.

It is important to note that the difference in electric field distribution in the two structures is non-negligible at 0 V, although this difference diminishes with the application of an increasing reverse bias. Despite the fact that a wider total SCR induces a higher probability of carrier generation in the latter, favouring avalanche breakdown, the total width of the SCR at voltages close to breakdown is practically identical for the two dopant distributions considered here. Generally speaking, if the doping gradient is high, or the depth over which this effective gradient is low, its impact on the diode breakdown voltage will be negligible. Just as important as the breakdown voltage, the electrostatic control of JFETs based on these two pn junctions, governed mainly by the threshold voltage of the transistors, will be detailed in the next section.

II.3.1.e Electrostatic control of pn-junction, toward JFET threshold voltage

By applying a potential difference across these pn junctions, the depletion depth of the space-charge region W_{SCR} can be effectively controlled, thereby modulating the conductance of the junction. This rectifier characteristic, exhibits two distinct limit states: an ON state for forward bias when the SCR is reduced to its minimum (application of a negative voltage on the n-type semiconductor), leading to maximum conductance governed by the as grown properties of the most resistive layer; and an OFF state, for reverse bias, when the SCR is extended to its maximum, encompassing the entirety of the lowest-doped layer in the case of a PT design (application of a positive voltage on the n-type semiconductor), resulting in minimum conductance approaching zero. The latter can be used on its own, as a diode, or, in the context of this work, as a JFET gate allowing electrostatic control of the conductance of the p-channel, which is modulated by applying a voltage variation to the gate electrode (schematically shown on fig. II.9). Reconsidering equation II.4 by addition of its applied voltage dependence while keeping the same hypothesis made concerning a extension mainly done in the p-channel, $W_{SCR,p}$ is given by:

$$W_{SCR,p}(V) = \sqrt{\frac{2\varepsilon_{SC}}{eN_A(1+N_A/N_D)}(V_{bi}-V)} \tag{II.11}$$

Where the built-in voltage V_{bi}, calculated for both n-dopant distributions through equation II.5, is 4.1 V in case of nitrogen doped gate and 4.8 V for phosphorous doped one. In the particular case of linearly graded junction, equation II.11 is not valid anymore and cubic dependence [208] have to be considered as depicted in fig. II.9. By modulating W_{SCR} within the pn junction, through variations in the gate voltage V_{GS}, the conductive cross-section of the channel gradually changes ultimately reaching full depletion, at the threshold voltage expressed as:

$$V_{TH} = V_{bi} - \frac{qN_At_p^2}{2\varepsilon_{SC}} \tag{II.12}$$

Although it would seem interesting to reduce the conduction channels thickness t_p, for a fixed doping level, to ultimately decrease the ON-resistance, this comes at the expense of an elevated threshold voltage required to reach the off state, as equation II.12 displays the square dependence of V_{TH} regarding to t_p. Even though doping level and compensation are important factors affecting the breakdown voltage and ON-resistance, the threshold voltage of the JFET is also influenced by these parameters, with an even higher sensitivity to channel thickness control (fig. II.9). Special care has to be taken during fabrication steps where, an acceptable variation of 5% during mesa-etching of the p-layers to structure the conduction channel of the transistor could leads to a ±7 V variation on the targeted $V_{TH} = 47$ V for a 400 nm p-channel and a dopants concentration $N_A = 2 \times 10^{17}$ cm^{-3}. The designer can adjust the threshold voltages by varying the epilayer thickness, transitioning from a normally-off, resistive device to a more conducting one with higher V_{TH} values, but in turns, this change comes at the expense of requiring more charge to be switched off.

II.3.2 Breakdown voltage vs. ON-resistance

The last sections were dedicated to the understanding and modelization of pn junctions in order to provide the necessary tools for design optimisation and analysis of diamond based JFET. However, one crucial trade-off in power electronics still needs to be considered: the balance between ON-state and OFF-state performance. While ideal JFET ON-state performance is mainly limited by the p-channel specific ON-resistance $R_{ON}S$, the OFF state is restricted by avalanche breakdown characterized by a breakdown voltage V_{BD}. These ideal conditions are rarely met and must be tempered alongside factors such as increased $R_{ON}S$ due to contact resistance and OFF-state leakage current, which can lead to premature avalanche phenomena.

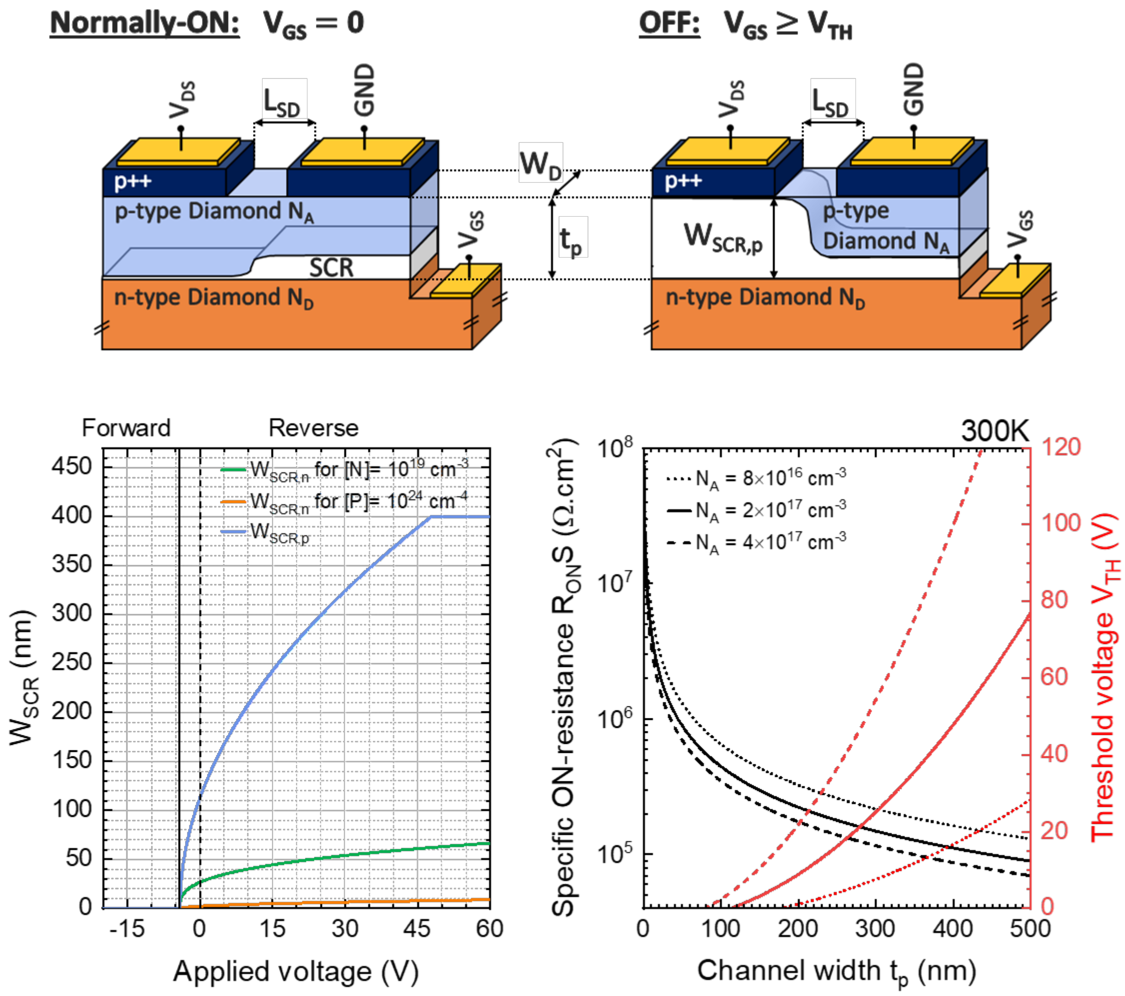

Figure II.9: Schematic cross section of diamond based JFET using nitrogen doped Ib substrate as gate layer (e.g. NS3, NS4 and GD-030 samples), in normally-ON configuration without bias application on the n-side, and OFF state with $V_{GS} \geq V_{TH}$ (constant negative bias is ensured on V_{DS}). Bottom left, space charge region extension in the multiples studied layers as function of the applied bias for a 400 nm thick p-layer and a doping level $N_A = 2 \times 10^{17}$ cm^{-3} and, bottom right, threshold voltage such as $R_{ON}S$ for various channel thickness t_p and diverse doping levels (for representation purpose V_{bi} has been assumed equal for the two different pn junction configurations presented in this thesis.)

Although these factors have been omitted in the following calculations, they can significantly impact the device's performance and should be taken into account whenever possible. Based on these considerations, the minimum specific on-state resistivity versus the breakdown voltage is displayed in fig. II.10 (left) for Si, SiC and diamond, each in NPT conditions for typical FET-channel doping level ($\simeq 10^{14} - 10^{17}$ cm^{-3}). The V_{BD} is calculated using models presented in section II.3.1.c and $R_{ON}S$ in NPT design, is calculated using resistivity extracted from section (X.X) multiplied by the depletion layer thickness reached at V_{BD}, hence $R_{ON}S = \rho W_{BV}$. In the particular case of PT design, the depletion layer thickness t_p is fixed and thus $R_{ON}S = \rho t_p$.

Strong trade-off appears when minimization of $R_{ON}S$ requires to maximize the doping level to decrease the resistivity and W_{BV}, as opposed to the maximization of V_{BD} which require low doping level to reach highest values. This could be enlightened for NPT diamond diodes where at a doping level of $N_A = 3 \times 10^{15}$ cm^{-3} a JFET p-channel exhibits an $R_{ON}S$ of 0.15 Ω.cm^2 (RT) while sustaining 10 kV, compared to a p-channel doped at $N_A = 2 \times 10^{17}$ cm^{-3} with $R_{ON}S$ of 0.78 $m\Omega$.cm^2 (RT) and sustain capabilities of more than 1 kV. Note that, to account threshold

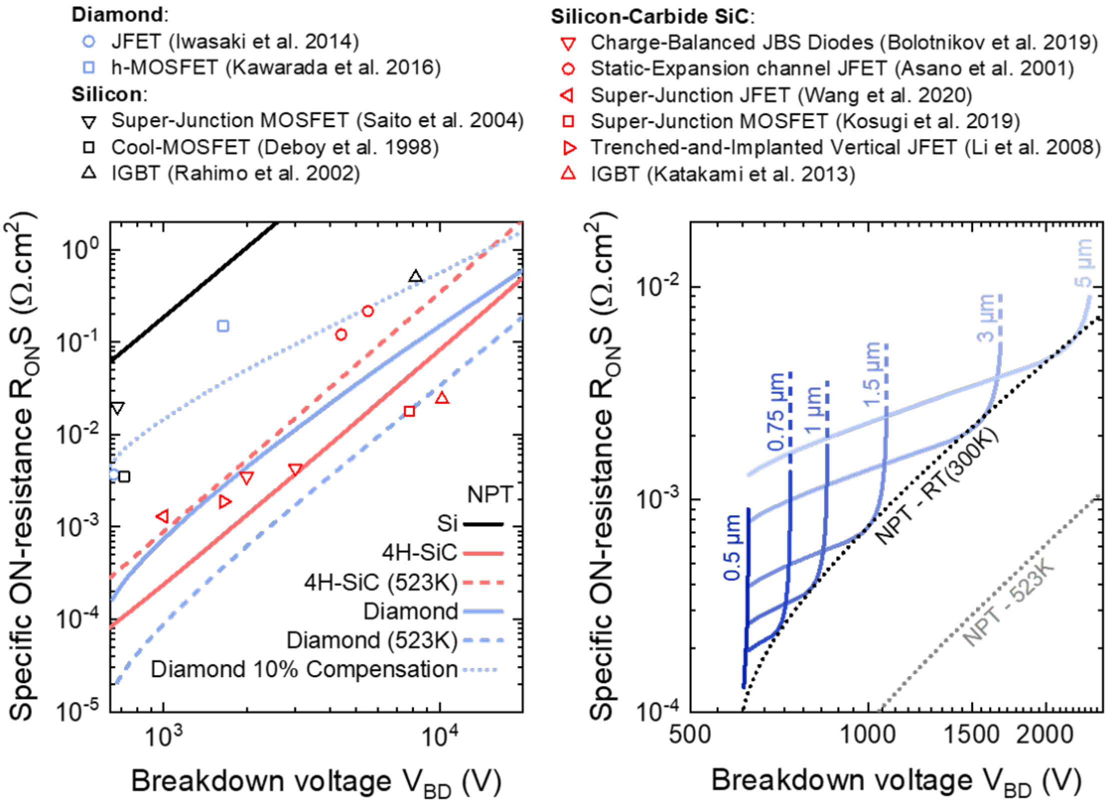

Figure II.10: Specific ON-state resistance vs breakdown voltage for a non-punch through (Left) and punch through (right) diamond pn junction diode at RT and 523K. The trade-off is also represented on the left hand graph for Si at RT, with calculations based on [265–267], and calculated for SiC at RT and 500K using [261, 268, 269]. Some of the best experimental results from diamond transistors [230, 270], such as Si based transistors [271–273] and SiC based FET [274–279] reported in literature are represented, aside with the devices architecture, for comparison. Right hand graph make a focus on the different PT configurations, thanks to the use of breakdown voltage previously computed on fig. II.7, using calculation routine proposed in [258] and based on the ionization coefficients from [260].

voltage trade-off presented in the previous section, achieving a JFET that sustain 1 kV with a room temperature specific ON-resistance as low as 0.78 $m\Omega$.cm^2 implies $t_p = 1.7$ μm, hence an absurd value of $V_{TH} \approx V_{BV} = 10$ kV. According to fig. II.10 (right), reaching the same specific ON-resistance in PT design with $t_p = 500$ nm, requires a doping level of at least $N_A = 1.3 \times 10^{16}$ cm^{-3} but in this case V_{BD} is limited to 625 V, with acceptable V_{TH} potentially reaching values lower than 15 V, depending on the doping level chosen.

Compared to other materials, where devices performances decrease with temperature rise, the trade-off is ameliorated for diamond at higher temperature due to increased carrier density. Although it should be noted that in the breakdown voltage models presented in this manuscript, temperature dependence is not taken into account. Based on rough comparison at room temperature, 4H-SiC devices illustrated by [261, 268, 269], exhibit better overall performances than diamond. However, at their respective optimal working temperature, diamond (523K) outperforms SiC at room temperature. While SiC experiences mobility reduction with temperature increase [268], in a environment where power electronic devices typically operate at temperatures significantly higher than RT (between 423 and 523 K) more diamond deep acceptors become ionized, thereby widening the performance gap between diamond and SiC. Note that silicon (computed using [265–267]) has been added to the figure as reference for the sake of comparison but its 1D theoretical limits are well under those of diamond and SiC.

Although it is important to precise that relatively recent silicon technologies, such as CoolMOS [272], super-junction MOSFET [271] or IGBT [273] have already overcome the theoretical limitations. To achieve such performances, silicon-based power electronic devices required decades of development and mostly relied on large-scale parallelized devices (super-junction). In contrast, small-sized diamond-based transistors [230, 270], despite having lower technology maturity, already compete with equivalent or even superior power handling capabilities. As silicon, some SiC devices reported in literature also have already overcome the theoretical 1D limitation through the uses of super-junction [277] or IGBT [279]. However, most of the SiC devices, especially commercially available ones, are already in their optimized operating range meaning that further technological improvement will requires the mobilisation of substantial resources. At the opposite diamond theoretical limits, compared to actually reported devices, indicates that significant improvement can be obtained ultimately planing on using junction termination extension to overcome 1D limitation as for Si and SiC.

For the position of this thesis, electro-optical control of the fabricated JFET is expected to provide both, an high breakdown voltage without illumination of the device (n-type devoid of free carrier) and a specific ON-state resistance enhanced by bi-polar mode operation [228] under light exposure. Gate drivers in power electronics are well optimized for insulated gate transistors like MOSFETs and IGBTs, hence, diamond based JFETs and depletion mode HEMTs have not been well received since there is significantly more power dissipated during the ON-state by the non-insulating gates [280]. Using insulating n-type layer (Ib substrate) that can be turned inactive as function of the illumination brought to the device, can efficiently solve this on-state power dissipation problematic. However to achieve this goal particular attention needs to be paid to the different device active layers characteristics, where small deviation in the targeted values can induce strong performances reduction, as demonstrated along this section such as in fig. II.10 where a 10% compensated p-type layer has been reported. The effect of the latter on the overall device performance can be dramatic, adding a decade in the theoretical specific on-resistance.

II.3.3 JFET gate design summary

Based on the physics of the vertical pn junction, the expected performances in terms of conductivity and blocking voltage capabilities of the lateral JFET architecture have been deduced. Innovative (100)-oriented highly phosphorous-doped layer, designed as linearly graded junction (linear decrease of the doping level in the vicinity of the junction boundary) to lower trap density potentially formed by epilayers lattice mismatch, have been reported to have a meaningless influence on the JFET key parameters ideal limitation (built-in potential, critical electric field). However, this demonstration must be tempered by the ideal consideration of models, such as the complete ionization of dopants, presented in this section. A point on which the use of phosphorus would make it possible to overcome the technological limitations and increase the overall performances recorded on nitrogen-doped gate JFET [241].

For a 400 nm thick and at a doping level of $N_A = 2 \times 10^{17}$ cm^{-3} for the p-channel, the ideally targeted $R_{ON}S$ is 0.18 $m\Omega$.cm^2 while blocking voltage calculations ensure the sustain of 600 V with a relatively high threshold voltage of 46 V. Compared to semiconductors like silicon and 4H silicon-carbide, diamond exhibits resistivity diminution with temperature rising such as higher critical electric field, enabling it to achieve higher breakdown voltages while maintaining lower on-state resistances. This advantageous position on the $R_{ON}S$ vs V_{BV} trade-off chart demonstrates the potential for diamond-based devices to outperform existing technologies under harsh or extreme operating conditions.

However, it is essential to consider the challenges associated with diamond-based device fabrication and technology maturity. As supported by devices reported in literature for the three materials compared in this study, diamond devices are still in the early stages of development compared to well-established Si and SiC technologies. Given the inherent difficulty of processing small sized diamond samples, lateral architecture is preferred over a vertical design which has not been achieved yet for diamond, limiting the number of technological steps but also the potential output performances. Therefore, further research, optimization, and advancements in diamond device fabrication, growth control and processing techniques are needed to fully reach the potential benefits of diamond in the $R_{ON}S$ vs V_{BV} trade-off. Ultimately, based on SiC and Si actual 1D limitations, diamond-based devices have the potential to revolutionize power electronics and find applications in a wide range of high-power and high-temperature scenarios.

II.3.4 Inter-digited JFET conception

II.3.4.a Targeted performances

Diamond-based JFETs have demonstrated the highest current density handling capabilities among diamond FETs in power electronic applications. The current density record, as reported by Iwasaki et al. [228] and presented in fig. I.22, achieved 450 A/cm^2 (normalized by p-channel cross section) at 673K for V_{DS} = -5 V and zero gate bias. With V_{GS} = -3 V and zero gate bias, the current density can be enhanced to 1200 A/cm^2 under the same drain voltage and temperature conditions. However, it is important to consider two factors when evaluating these extreme values. Firstly, the absolute current measured is in the range of a few μA, and the high current density has been achieved through the utilization of small-sized p-channel devices with adapted doping levels (as discussed in section II.3.2). Secondly, the breakdown voltage reached for these JFETs is 600 V [230]. In comparison, diamond MESFETs [281] have demonstrated a breakdown voltage of 1.5 kV, and H-terminated MOSFETs [212] have shown more than 2 kV, although both devices have a limited current density in the range of few mA/mm. Currently in the literature, there are no reported diamond-based FETs that simultaneously meet the power market requirements of sustaining 1 kV in the off-state and conducting 1 A in the on-state.

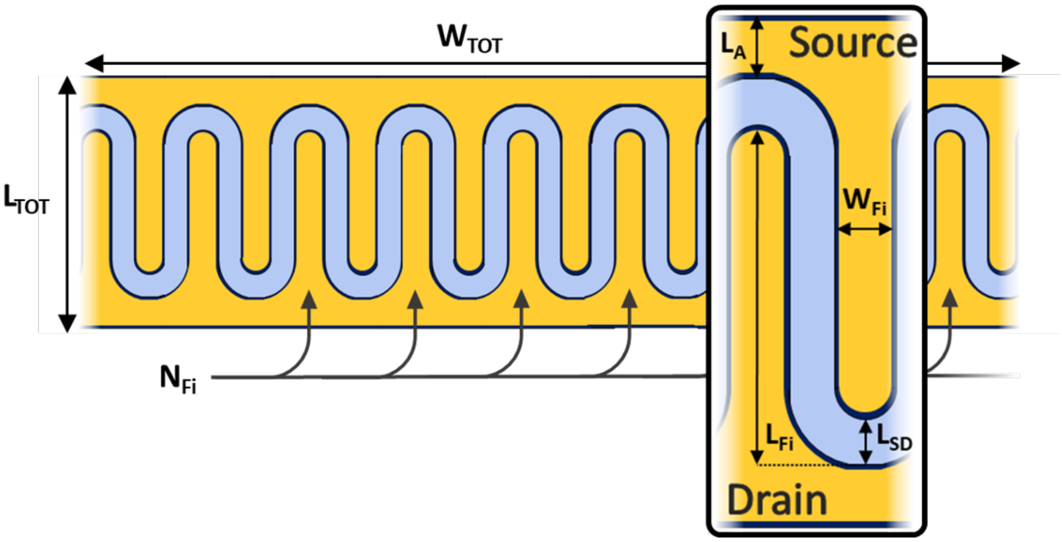

Figure II.11: Top view of the designed inter-digited JFET. Main length and width used for the design are reported in the focus of a unitary single-fingered cell.

In order to meet the aforementioned criteria, an inter-digited (IDT) architecture, as depicted in fig.II.11, has been developed. While IDT designs have already been proposed for diamond-based devices, they have not been previously explored as performance enhancers for power applications. However, IDT designs have demonstrated promising results in other areas, such as detectors, where they enhance device collection efficiency [89]. Additionally, IDTs are essential for the fabrication of surface acoustic wave (SAW) resonators [282], enabling the creation of resonance cavities. In both applications, the primary objective is to increase the active area of the devices by widening the electrodes. This concept can be extended to lateral power transistors, where an increased active region area of the drain electrode leads to reduced on-resistance for a fixed layer depth, resulting in improved current rating capabilities.

The design, as presented in this manuscript, is divided in two steps. Firstly, a unitary single fingered cell, depicted in the zoomed-in of fig. II.11 has been defined and optimized for 0.6 kV breakdown voltage. Optimization process, developed in previous section, involved adjustment of the doping level and thickness of the p-channel through pn-junction model, which is vertically used as gate. More than fixing the avalanche breakdown voltage theoretically reachable by the structure, it also defines the resistivity of the p-channel ρ_p. Secondly, the exchanging surface between drain and source electrodes has been optimized through multiplication of the single-fingered cell. The latter increases active channel width within a smaller device area, with the goal of enabling a current handling capacity of 1A.

II.3.4.b Through enlarged active area

Taking into account risks related to large-scale devices emphasized by Umezawa et al. [121], area allowed for IDT fabricated on each samples have arbitrary been chosen to not exceed 40% of the available fabrication surface. This choice, at the user's expense, ensure a safe functionality margin regarding to the amount of IDT mis-fabrication possibilities, which will be developed in the next subsection. Additionally, only symmetrical drain and source electrodes are considered in order to avoid any uncontrolled current or electric field crowding that can appear, as for circular transistor for example [283, 284]. It is worth noting that, for the same reason of crowding avoidance, the ends of the designed fingers were given a round shape, similar to the shape of the facing access electrodes. In general, it is advisable to minimize the presence of steep and abrupt angles during mask design. In the present case, the round shape is crucial to ensure a consistent drain-to-source length throughout the IDTs, even if the lithographic steps are challenging through mis-alignment that can appear across the different fabrication steps.

Optimization of on-state current is modelized through minimization of the p-channel on-resistance expressed as:

$$R_{ON} = \frac{\rho_p L_{SD}}{W_{ID}(t_p - W_{SCR,p})} + 2R_C\Sigma_D \tag{II.13}$$

In the given equation, ρ_p represents the resistivity of the conducting p-channel, which was determined in section I.2.2.e, and t_p the targeted width of the p-channel epi-layer. The variables L_{SD} and W_{ID} correspond to the drain-to-source length and the total width of the drain electrode, respectively. The second part of the equation takes into account the contact resistance per unit area, denoted as R_C, multiplied by the surface area of the drain contact, Σ_D. It should be noted that since the drain and source electrodes are symmetrical and identical, the access resistance is considered twice in the calculation.

To optimize the on-resistance, the decision was made in equation II.13 to prioritize the absence of bias on the pn-junction used as the gate. Consequently, the conductive width of the p-channel is expressed as $(t_p - W_{SCR,p})$ and is approximately 280 nm for the fabricated samples, without gate bias. However, by applying a negative voltage bias to the gate, effectively putting the pn-junction in a direct state, the $W_{SCR,p}$ value can be reduced to nearly zero. This adjustment allows the useful conductive width of the p-channel to become equal to t_p. This choice of representation was driven by the objective of nullifying energy consumption in the absence of a gate voltage.

In diamond lateral FET architectures, reducing the drain-to-source length L_{SD} to minimize the on-resistance faces limitations imposed by the architecture itself or the fabrication process. It is assumed here that, for a targeted breakdown voltage, there is a drain-source distance that allows the ON-resistance to be minimised, taking into account a safety margin for ease of fabrication. Lateral MOSFETs or MESFETs, for instance, encounter challenges with gate placement between the drain and source contacts on the top face of the p-channel. Additionally, they are constrained by a trade-off where a sufficient gate-to-drain distance is necessary to achieve high blocking voltage, at the expense of increased on-state resistance. For the JFET presented in this manuscript, the electrostatic control is achieved through the backside of the p-channel, allowing for the relocation of the gate contact. Distancing the gate contact incurs an increased gate internal resistance but also offers greater flexibility in lowering L_{SD} until the fabrication process limit is reached. To explore various possibilities, four different drain-to-source lengths were selected for IDT fabrication. Starting from the riskiest option at 2 μm, which is near the resolution limit of our laser lithography, the lengths progress to 5 μm, 10 μm, and finally 20 μm. IDTs with a source-to-drain length of 2 μm were positioned at the center of the mask, where resist deposition is most uniform, aiming to minimize possible short-circuit occurrences.

For a fixed rectangular surface on a sample, denoted as $\Sigma_{TOT} = L_{TOT} \times W_{TOT}$, where W_{TOT} represents the total width and L_{TOT} represents the total length, the single-fingered cell presented in the zoomed-in section of fig. II.11 was adapted to be replicated as many times as possible to fulfill Σ_{TOT}. Initially, the access length L_A was determined and set to be equal to W_{Fi}, ensuring that the maximum length for a single finger $L_{Fi} = L_{TOT} - L_{SD} - 2L_A$ was achieved. This approach guarantees that the fingers are as long as possible within the designated area. Subsequently, W_{Fi} was calculated for an increasing number of fingers N_{Fi}, and the corresponding values were used to determine the access, channel, and total resistances of the IDTs. This design protocol is depicted in fig. II.12, considering a drain-to-source length of 2 μm for diamond based IDTs, with a doping level of $N_A = 2 \times 10^{17}$ cm^{-3} allowing to sustain 0.6 kV in NPT regime (even more but $L_{SD} = 2$ μm have been set as minimal value to account for lithography limits). As comparison, silicon and silicon carbide based IDTs, with the same targeted breakdown voltages of 0.6 kV, hence adapted layer parameters, are also depicted. While SiC equivalent layer (400 nm thick) would require at least $L_{SD} = 3.8$ μm and a maximum of $N_D = 4.5 \times 10^{16}$ cm^{-3} to be able to sustain 0.6 kV, the trade-off is even worst with silicon which would at least display $L_{SD} = 49.4$ μm and a maximum of $N_D = 4 \times 10^{14}$ cm^{-3}. Noticeably, the channel resistance is compared to the sum of the access resistance R_{Acc} and the contact resistance R_C. Through this approximation, we have a resistance majorant, as the current is distributed inside the finger between the downstream finger piece and the active semiconductor zone. However in denser simulations, a more complex resistance network between the metallized fingers and the transistor's active zone should be taken into account.

Regarding diamond at 300K, the p-channel resistivity was assumed to be 4.2 $\Omega.cm$ based on measurements conducted on the reference sample GD-030 and parameters provided in Table II.1. Contact resistance per unit area and the resistivity of the metallic diamond composing the stack were also determined from measurements on this sample, yielding values of 7×10^{-5} $\Omega.cm^2$ and 3×10^{-3} $\Omega.cm$, respectively [58]. As shown in fig II.12, increasing the number of fingers N_{Fi} imply reducing the finger width W_{Fi}, which leads to a decrease in total resistance. This implies that in diamond devices, it is advantageous to use as many fingers as possible with the smallest width. However, two fabrication limitations must be considered. Firstly, the laser lithography used in this work (Heidelberg DWL66FS) has a resolution limit of 2 μm. Secondly, based on 2D cylindrical calculations by Chicot et al. [257], the round shaping of the finger ends should not be below 20 μm to prevent a decrease in breakdown voltage due to 2D effects. Consequently, for the four fabricated samples with $L_{SD} = 2$ μm, the optimal ratio was determined to be $N_{Fi} = 9$ and $W_{Fi} = 20$ μm. This design targets an on-resistance of 172 Ω at 300 K, which can be reduced to 32 Ω at 500 K. In comparison, considering electronic lithography with a resolution in the range of a few tenths of a nanometer and neglecting 2D parasitic effects, the resistance could potentially reach 5.4 Ω at 500 K with 80 parallelized fingers that are 500 nm thick.

The significant difference between the channel resistivity and the contact resistance for diamond, implies that the conduction in the p-channel at room temperature will still be limited

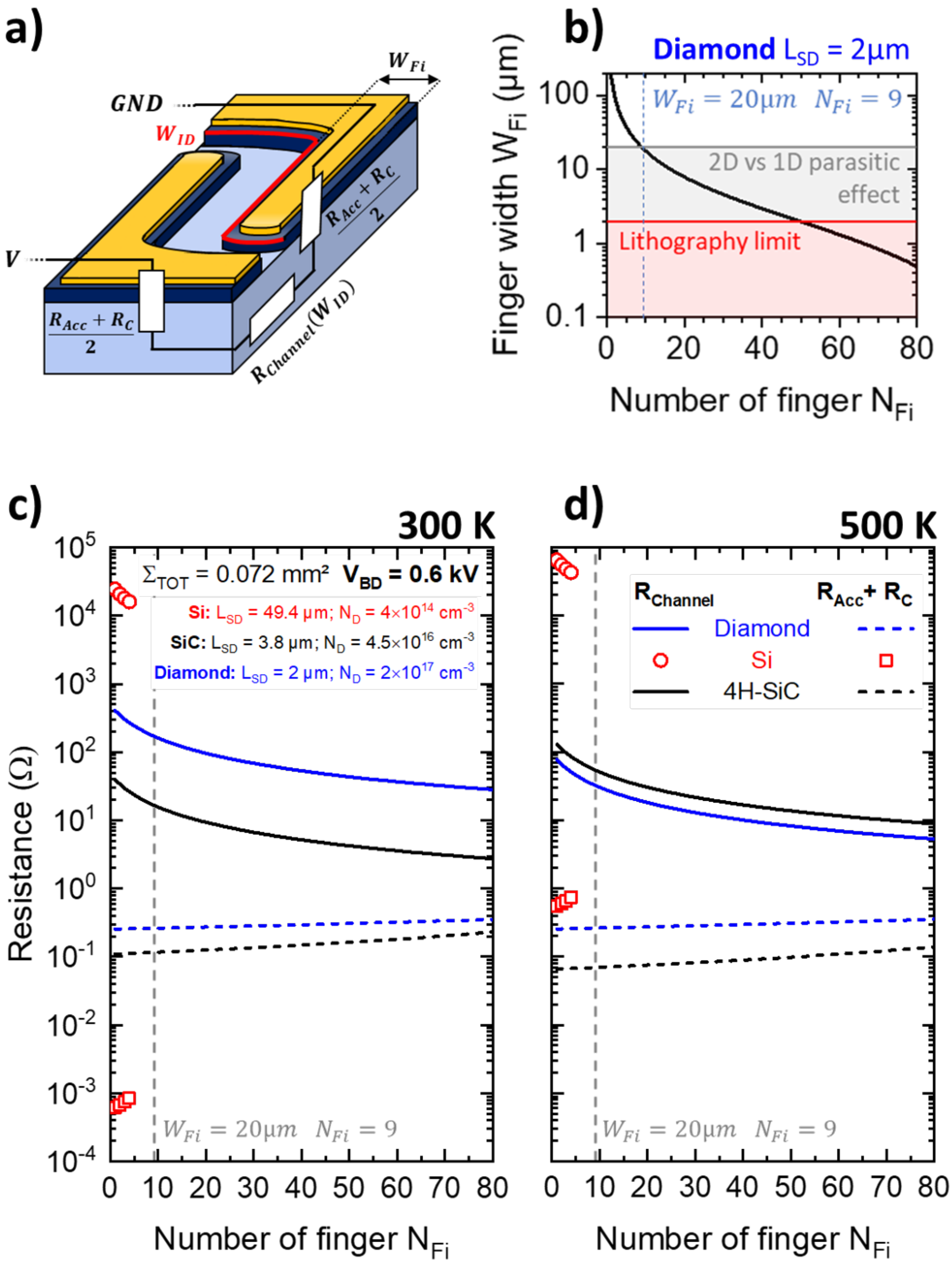

Figure II.12: a) 3D representation of a single fingered unitary cell and associate electrical equivalent circuit. b) W_{Fi} as function of N_{Fi} for diamond design, with the lithography limit of $L_{SD} = 2\mu m$. c) Access plus contact resistance, and channel resistance of the designed inter-digited JFET as function of N_{Fi} at 300K, and d) 500K for a fixed total area (0.072 mm^2) but variable drain to source spacing L_{SD} corresponding to the minimal NPT length required for each material to sustain 0.6 kV in OFF-state. Blue lines are used for diamond resistance, black lines for silicon carbide (4H-SiC) where resistivity and contact resistance are extracted from [285–288], and open circles and squares stands for silicon (Si) where resistivity and contact resistance are extracted from [208, 289, 290]. Optimized doping level and L_{SD} used for computation are displayed and have been extracted from section II.3.1.c, whereas for silicon only 4 points are displayed regarding the significant L_{SD} required for a fixed total surface.

by incomplete ionization, regardless of the electrode shape design. As a comparison, the same structure was simulated using phosphorous-doped silicon instead of diamond. The resistivity of the n-channel layer and the contact resistance per unit area of the silicon were obtained from [289, 290] and found to increase with temperature. This indicates that, for N_{Fi} values higher than 10, the measured on-resistance becomes influenced by the access resistance, making it dependent on the device geometry. In the worst-case scenario, with a high finger density (e.g., higher than 70), the on-resistance of the IDTs is primarily determined by the access resistance, highlighting losses induced by the design itself.

Table II.2: Summary of the fabricated IDT and their targeted performances

L_{SD} (μm)	2	5	10	20
Total surface allocated (mm^2)	0.43	1.05	1.43	0.7
Divided into	6	12	12	4
Single IDT				
Σ_{TOT} (mm^2)	0.036	0.072	0.103	0.13
W_{TOT} (μm)	400	605	790	740
L_{TOT} (μm)	90	120	130	175
L_{Fi} (μm)	48	75	80	115
N_{Fi}	9	12	13	9
$R_{ON}(300K)$ (Ω)	172	225	387	839
$R_{ON}(500K)$ (Ω)	33	42	73	158
Wire-bounded IDTs				
$I_{300K}(V_{DS} = 5V)$ (mA)	175	266	155	72
$I_{500K}(V_{DS} = 5V)$ (mA)	910	1430	822	380

The selection of wide access lengths facilitates the merging of different IDTs, resulting in a distinctive "radiator-shaped" structure, as depicted in fig. II.13. Notably, an incremental access length, L_A, has been incorporated in each designed IDT to ensure a safe margin regarding minimization of current crowding at high electric fields. Furthermore, large and thick contact pads have been added to allow easy probing of the IDTs and also for wire bonding should the target of 1A that need to be reached. Both implementation that have been added on each designed IDTs, summarized in table II.2, with a common $W_{Fi} = 20\ \mu m$, is expected to optimize the overall performances of the device through almost 3.5 A handling at 500K with $V_{DS} = 5\ V$ on one diamond substrate.

II.3.5 Summary and process discussion

The IDT design process as proposed coupled to the electrical characterization revealed that for further diamond power applications, the density of fingers must be increased till reaching the fabrication process limits. Although this work considered an adequate finger width to mitigate 2D perturbations, the cost of optimizing this parameter outweighs the potential benefits of increasing the finger density.

As mentioned many times along the design protocol, the lithography patterning process is an essential milestone for IDT fabrication. Even if this process tends to be standardized among the team, it is still a bit of a "black magic" due to the rough nature of the diamond surface coupled to small sample size, which causes a variation in photo-resist thickness. The proposed JFET design in this manuscript requires only three lithography steps, but the IDT design introduces strict constraints on the alignment between each lithography step. The misalignment tolerance for each sample is set at 5 μm for translation in the surface plane and 3.4 mrad (or 0.2 degrees)

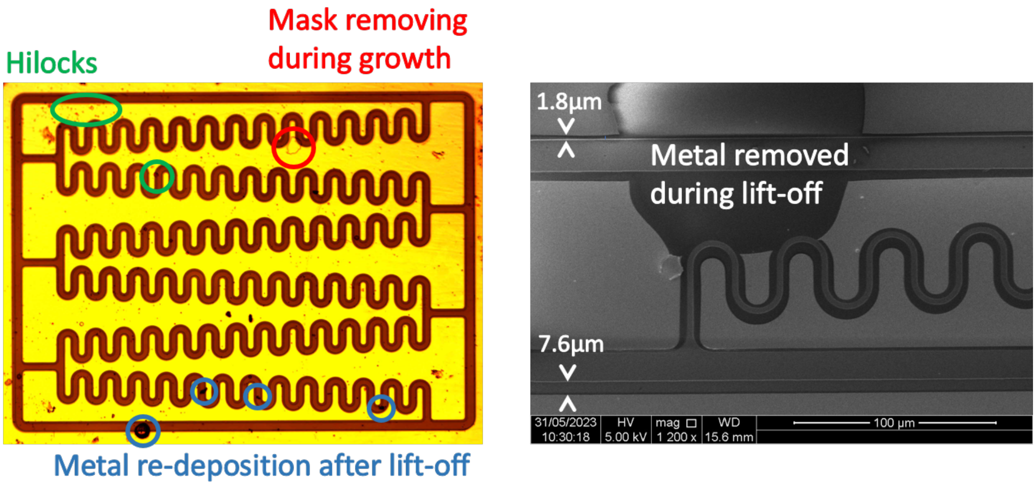

Figure II.13: Optical image of IDT with $L_{SD} = 10$ µm on the left and SEM image of IDT with $L_{SD} = 2$ µm on the right. Both images have been emphasized with defects introduced during different fabrication steps.

for rotation from the center of the samples. These tolerances, particularly the alignment between gate metal deposition and p-type mesa structures, are close to the limits of what can be achieved. However, more relaxed tolerances are considered for the alignment between metallic diamond selective growth and mesa structuring through p-type etching, providing a more comfortable margin for alignment precision. Initially the yield of mis-aligned metallizations was very high and rather disappointing, but after much practice the yield improved considerably, with between 2 and 3.8 μm in translation in the surface plane and between 2.2 and 3.1 mrad being obtained.

Coupled to mis-alignment, photo-resist remaining or being withdrawn on the desired surface can create a short circuit between device fingers. A lot of attention was taken to avoid the formation of any short circuits between the two electrodes; examples of such defects can be seen in fig. II.13. Any defect which makes contact to two electrodes of different polarity (e.g. drain and source or gate in drain for off-state) would render the device unusable as a path of low resistance would be made in parallel to the highly resistive path through the diamond different layer. These defects primarily arise from photoresist over- or under-development, as well as over-growth or etching issues. Such issues can have a significant impact on the fabrication process, leading to the formation of very narrow or broken fingers during each step.

As detailed in this section, fabrication of diamond devices is challenging due to the absence of standardized processes. The limited sample size and the lack of precise control over critical steps, such as defect-free growth and lift-off procedures, have further hindered production of large-sized devices in the last few years. Additionally, the availability of substrates is constrained, and the time required to complete fabrication can extend to several months depending on equipment availability. For this specific IDT design, the initial yield of working devices was very low due to short gate metal to p-type mesa-structure length used, but after mask adaptation and much practise the yield improved considerably, with over 75 % being obtained. These factors collectively contribute to the difficulty in scaling up performances of diamond based large scale devices. However, it is worth noting that the finger-to-finger spacing, which was defined during the metallic diamond selective growth process, was successfully maintained constant. Additionally, the fabrication of IDTs with a 2 μm drain-to-source spacing was achieved successfully, showing great promise for high on-current handling capabilities.

II.4 Layer and contact characterization devices and techniques

As failure can happen in any step, many layers and contact characterization devices such as transfer length method (TLM) contacts or surface-controlled pn-junction, of various shapes and sizes have been fabricated on the samples surface, allowing for a complete electrical and optical characterization.

Diodes and transistors electrical characteristics that are presented along this and next chapter were performed at Néel Institute, in a home-made vacuum and temperature controlled, probe station. Most electrical measurements were performed using a double channel Keithley 2612b and/or a single channel Keithley 2410 as well as a ModuLab XM-MTS Solartron analytical system. SMU 2612b, in DC source and measurement mode was used for its low current detection limit of 1 pA within a bias range of 200 V. For this purpose, dedicated LabVIEW programs have been coded and developed by the author, especially for transient measurement which can be completed by quick time resolved drain current measurement acquired by a Tektronix TDS2022b oscilloscope, after passing through a current-to-voltage converter. The Keithley 2410 was, for its part, used to investigate the blocking off-state of devices thanks to its 1.1 kV maximum applied bias voltage with drawbacks cost of a lower detection limit mentioned at 1 nA by the manufacturer. Lastly, Solartron was also used for DC measurement and source, with properties close to Keithley 2612b, for convenience regarding to multi-contact measurement. It should be noticed that, the latter can be used for capacitance voltage/frequency measurement as it provides AC signal with frequency ranging from 1 mHz to 1 MHz and rms of 200 mV. It is important to notice that as often as possible, instrument wiring with device under test (DUT) is achieved through tri-axial cable. This improvement have been brought to ensure highest precision capabilities during low-current measurements, where additional leakage current between the core and shield could arise from traditional co-axial insulator.

Regarding device contacting, precise control over the 3D displacement of removable tungsten tips is achieved using piezoelectric micro-manipulators. To maintain optimal electrical continuity, the tungsten tips are regularly cleaned through RIE to prevent oxidation that can result from air exposure. The approach of the tips towards the metallic contacts is observed and controlled using a binocular microscope, focused through a quartz porthole. This setup ensures that there is no absorption of UV or visible light when the microscope column is replaced with optical setup presented in section IV.1.2.b.

Temperature control ranging from 77 K to 650 K is achieved thanks to a Linkam cooling system. While the regulated temperature is applied to the sample holder, it is important to note that some samples presented in this thesis require electrical backside contacts. To ensure this backside contacting samples are sticked on alumina plate by the use of silver paint (shown in fig. II.1). This allows the polarity of the sample to be controlled but also induced a temperature gradient inside the alumina plate, between the sample-holder and diamond samples. To monitor and control this temperature gradient, a Pt100 thermometer is always positioned on the alumina plate next to the DUT and so, all temperature referenced throughout this manuscript will be based on measurements taken by the Pt100 thermometer, ensuring consistent and reliable temperature information.

II.4.1 Structure dedicated to electrical characterisation

II.4.1.a p-channel characterisation device

The diamond resistivity and the contact resistances, as key parameters that define the on state resistance of the device, needs to be precisely characterized on each fabricated samples. To achieve this, specific Transfer Line Method (TLM) structures, depicted in fig. II.14, have been designed and distributed on the outer part of the mask.

TLM structures enable resistance measurements between constant surface contact patterns

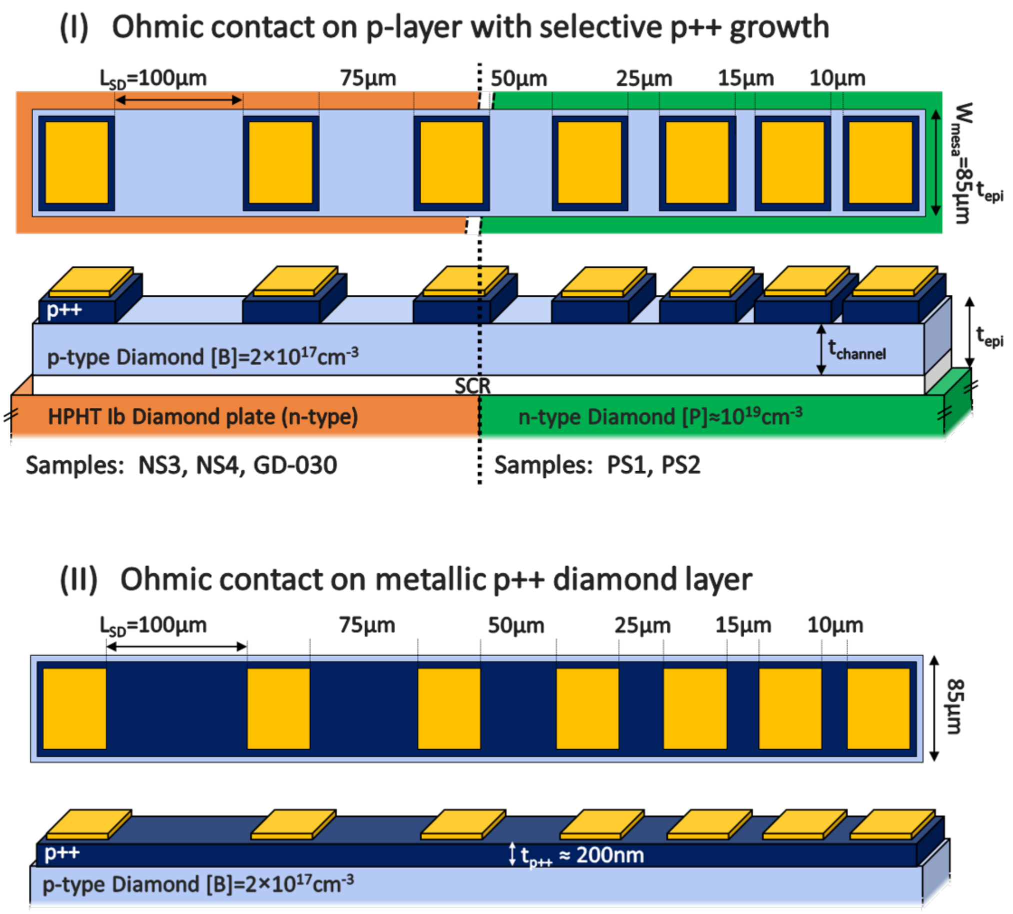

Figure II.14: Top view and side view of the mask used to fabricate the rectangular-shaped TLM structures which have been used to analyse the p-channel (top) and metallic (bottom) diamond resistivity and contact resistance.

at varying distances. Thus, by the use of equation II.5 and in an ideal case, linear relationship will arise between measured resistance and L_{SD} variations. Then by an assumption on the mobility (as it is dependent on doping level), for a given temperature, doping level can be extracted from the resistivity measurement using the slope of the $R = f(L_{SD})$ curves, such as contact resistance extrapolation using $R = f(L_{SD} = 0)$. For this purpose two linear designs are proposed to respectively extract: p-channel resistivity and affiliate metal/selective growth contact resistance, such as p++ layer resistivity. It is assumed that the resistance contributed by the metal stack is negligible in these designs.

This method can serve as a more compact alternative to Hall-effect measurement (with strong assumptions), providing free carrier characterization, assuming mobility (or vice-versa). It requires only the mesa-structuring with $L_{SD} \gg t_{epi}$ to ensure current flows between linearly spaced patterned contacts and allows for 1D modelization. Throughout the p-channel TLM results presented in this manuscript, the removal of the SCR extension has been ensured prior to each measurement. The back-face pn-junction has been strongly biased in forward to ensure $t_{channel} = t_{epi}$, without injecting any noticeable minority carrier from the n-type substrate to the p-type region (e.g. n-type vertical leakage current is much smaller than TLM lateral current). Moreover, since p-type diamond is expected to exhibit higher conductivity compared to nitrogen or phosphorus-doped diamond, any extension of the current line path inside the substrate or phosphorus epi-layer is negligible.

II.4.1.b n-type diamond and gate contact characterization device

To minimize the number of fabrications steps on the four fabricated samples, it has been chosen to not isolate n-type mesa-structures through an etching process. Consequently, linear rectangular shaped TLM, as demonstrated in the previous section, are not feasible because of the non-control of current line spreading between two neighbour contacts that could have been introduced. To overcome this, circular shaped TLM devices (c-TLM), depicted in fig. II.15 have been used, allowing n-type layers full characterization and further devices fabrication.

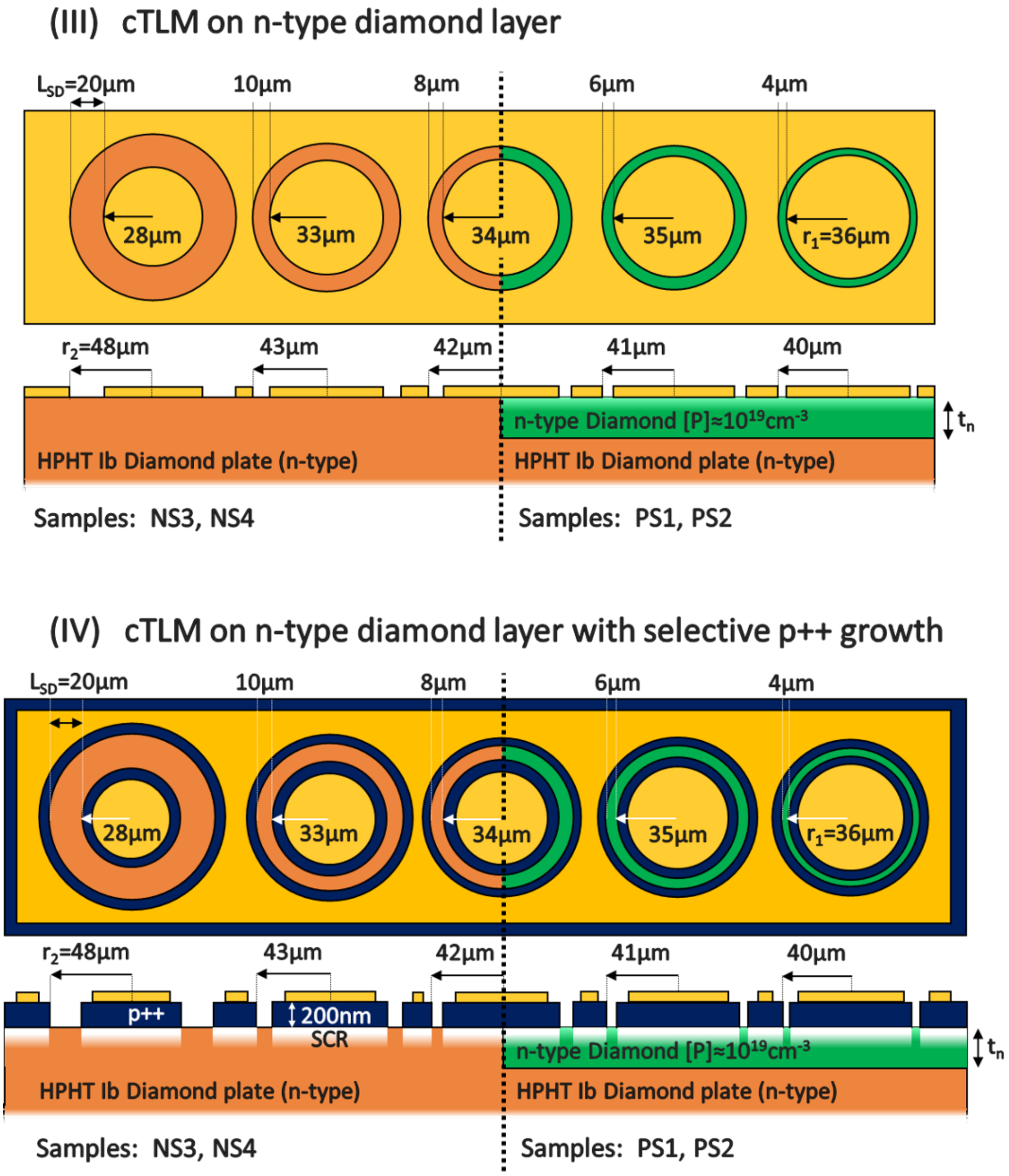

Figure II.15: Top view and side view of the mask used to fabricate the circular-shaped TLM structures. On top, n-type layer resistivity and gate metal contact properties characterization c-TLM and on the bottom, tunneling-pn junction for samples PS1 and PS2 or p++n capacitor for samples NS3 and NS4.

In c-TLM, current flow between two circular electrodes, one with an inner radius r_1 and another with outer radius r_2. When the aspect ratio $r_1 + r_2$ is maintained constant, even through variations of both radius, the on-resistance between the two electrodes linearly depends on the contact spacing $L_{SD} = r_2 - r_1$. Adding the geometric aspect ratio, the on-resistance R_{ON} is expressed [166, 291]:

$$R_{ON} = \frac{R_S}{2\pi}\left[L_T\left(\frac{1}{r_1}+\frac{1}{r_2}\right)+\ln\frac{r_2}{r_1}\right] \tag{II.14}$$

With R_S being the layer sheet resistance ant L_T the transfer length which can be thought of as the distance over which most of the current transfers from the semiconductor into the metal or vice versa. It can be expressed as:

$$L_T = \sqrt{\frac{R_C}{R_S}} \quad \Longleftrightarrow \quad R_C = R_S L_T^2 \tag{II.15}$$

Similarly to regular (linear) TLM, fitting of $R_{ON} = f(L_{SD})$ for various r_1, r_2 couples, (while maintaining $r_1 + r_2 = cste$) with equation II.14 yields the free parameters R_S and L_T and then extrapolation of R_C through equation II.15. It is important to note that if non-ohmic contact behavior, such as Schottky contact, occurs, additional characterizations are required to validate this approach. In the case where both contacts exhibit Schottky behavior, resulting in two back-to-back diodes, no current can be observed, rendering these structures ineffective.

Regarding samples PS1 and PS2, the enhancement of n-type contact ohmicity was investigated through the creation of a tunneling pn-junction. Achieving ohmic contacts on n-type diamond remains a significant challenge, but the introduction of a highly boron-doped diamond layer prior to metal deposition was anticipated to facilitate hole tunneling from the p++ diamond valence band to the phosphorus impurity level. This tunneling enhancement, combined with the hopping mechanism in the n-type layer, yielded promising results, which will be discussed in detail in Section III.6.2. Similarly, samples NS3 and NS4 utilized nitrogen-doped diamond as the n-type layer and also employed c-TLM with p++ selective growth. In this case, since the nitrogen layer lacks free carriers at room temperature and is completely insulating, the emphasis is on capacitive applications, which will be of significant importance for future integration of small-sized passive components. However, due to inherent challenges in n-type diamond growth and dopant activation that leads to n-type conductivity, a particular attention is paid to the dopant incorporation in the these layer, especially through spectroscopy technique presented in the next section.

II.4.2 Spectroscopy and imaging techniques

Thanks to the use of an Scanning Electron Microscope (SEM), an energetic electron beam (e-beam) is focused on the DUT, leading to the generation of electron-hole pairs through valence band electron excitation which are promoted to the conduction band. This high density of electron-hole pairs enables the investigation of carrier drift-diffusion and various recombination mechanisms. These mechanisms, depicted in fig. II.16, offer valuable insights into the properties, quality and purity of the semiconductor material.

II.4.2.a Cathodoluminescence

Cathodoluminescence spectroscopy (CL) is an optical, contactless and non-destructive technique, generally used to investigate defects and among which dopants in a semiconducting material [293]. This technique is based on luminescence spectroscopy, which involves the emission of photons resulting from radiative recombination when a solid is exposed to an electron beam.

Among the excess electron-hole pairs generated, a proportion remains spatially linked due to Coulomb interaction. These coupled particles form quasi-particles known as excitons, characterized by an electron-hole coupling energy E_X, estimated around 80-93 meV for diamond [294–296]. In semiconductors in general, excitons are able to travel like a particle through the crystal without any apparent charge transfer, and thus be referred to as free excitons FE. However, this unimpeded diffusion is further limited in doped semi-conductor where free-exciton can be bounded or trapped by neutral impurities via van der Walls interactions and in this case

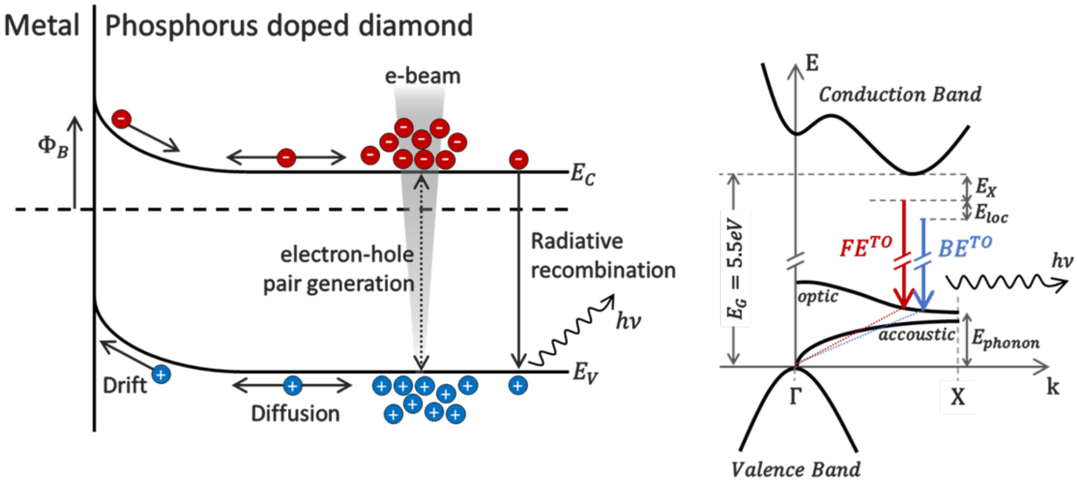

Figure II.16: At left, band diagram example of a Schottky contact on n-type diamond where electron hole pairs are generated by an e-beam. Enlightening the drift-diffusion of the excess holes generated that leads to electron beam induced current (EBIC) and the radiative recombination of both oppositely charged carrier which is used in cathodoluminescence (CL) spectroscopy. Courtesy to [59] modified from [224]. On the right, diamond band diagram with main intrinsic and extrinsic transitions, that are scanned during CL spectroscopy. Courtesy to [115], based on the work of [292].

called bound exciton BE. Stronger localization of the excitons in the real-space, near neutral impurity, is permitted through a binding energy-shift E_{loc} as schematised in fig. II.16. Values of 75±2 meV and 51 meV for E_{loc} have been reported for phosphorus[297] and boron [292] respectively. In terms of proportion, the bound excitons number increases with the neutral impurity concentration.

As electrostatic couplings of two charged particles of the same charge, both BE and FE have a short lifetime enlightened by different recombination processes [293, 297]. Only considering the radiative recombination, energy of the photon emitted is directly linked, by energy conservation, to excitonic transition that occurred. For diamond, as part of indirect band-gap semiconductor, the conduction band minimum is located in Δ_1 symmetry point (0.76% of Γ-X). In this specific case, photon emission needs to be assisted by absorption or emission of phonons, to ensure momentum conservation as depicted in fig. II.16. Phonon energy involved are denoted $\hbar\omega_{phonon}$, where ω_{phonon} is the phonon frequency associated to various vibration modes (longitudinal or transversal, such as acoustic or optic). Subsequently, in the one-phonon process, the energy of the emitted photon is $h\nu = E_G - E_X - E_{loc} - \hbar\omega_{phonon}$ for BE recombination and $h\nu = E_G - E_X - \hbar\omega_{phonon}$ for FE respectively.

Main diamond FE and BE excitonic transition linked to boron or phosphorus are summarized in Table II.3, emphasizing the generated photon energy as function of the phonon involved in the transition. By the use of CL, the light is collected and separated into its component wavelengths by a monochromator, allowing a precise discrimination of the photon received as function of their energy. Concerning boron doping, Omnès et al. [299] demonstrated that boron concentration can efficiently be measured, with a high precision (even if SIMS analysis report the boron incorporation, CL doping level extraction exhibit one decade better resolution than SIMS), through the intensity ratio of BE^{TO} and FE^{TO} peaks, respectively noted $I_{BE^{TO}}$ and $I_{FE^{TO}}$. The linear relationship, valid for doping level ranging from 10^{16} cm^{-3} to 10^{18} cm^{-3} at cryogenic temperature (4 K) is:

$$[B]_{CL}(cm^{-3}) = 3.5 \times 10^{16} \times \frac{I_{BE^{TO}}}{I_{FE^{TO}}} \tag{II.16}$$

Following the same intensity ratio comparison, Barjon et al. [298] demonstrated that this

Table II.3: Main excitonic transition in boron and phosphorous doped diamond [103, 293, 298, 299]

Symbol	Phonon involved	Photon energy (eV)	λ (nm)
Intrinsic			
FE^{TO}	Transversal Optic	5.27	235.1
FE^{TA}	Transversal Acoustic	5.32	232.9
FE^{LO}	Longitudinal Optic	5.25	236.0
Boron			
BE^{TO}	Transversal Optic	5.21	237.8
BE^{LO}	Longitudinal Optic	5.19	238.7
BE^{NP}	No-Phonon	5.36	231.2
Phosphorus			
BE^{TO}	Transversal Optic	5.19	238.7
BE^{TA}	Transversal Acoustic	5.24	236.4
BE^{NP}	No-Phonon	5.33	232.4

approach is also valid for phosphorus concentration estimation within the range starting from 2×10^{15} cm^{-3} to 2×10^{18} cm^{-3} at 102 K, expressed as:

$$[P]_{CL}(cm^{-3}) = 1.0 \times 10^{17} \times \frac{I_{BE^{TO}}}{I_{FE^{TO}}} \tag{II.17}$$

Furthermore than doping level extraction, CL spectroscopy have proven great interest for point defect investigation such as extended defects, like dislocations, observations and in some cases, quantification. Mainly for diamond, well known band-A emission is often associated to broad bands in CL spectrum at 2.3 and 2.5 eV for the green band, and 2.9 eV for the blue band [103]. These broad bands have been linked with radiative extended defects and specifically its CL intensity is directly linked to dislocation density through the scanned layer. As the latter could affect transistor performances and mainly on-resistance and breakdown voltage, its observation is of major interest. Furthermore, CL measurements have been performed at 5 K for boron doped layers in order to enhance *BE* exciton radiative transition, and between 5 K and 120 K for phosphorous doped layers to have better comparison with the literature [298]. Unveiling doping level and defects through CL spectroscopy lays the foundation for a complementary analysis, electron beam-induced current (EBIC), which provide better overview of the defect localisation through their detrimental impact on conductivity (field and current crowding).

II.4.2.b Electron beam induced current

As demonstrated along this section, electron-holes pairs created in semiconductors inside SEM chamber, contain many structural or compositional information on the latter. To complete high resolution composition informations provided by CL, electron beam induced current technique (EBIC) is a complementary analysis that allows junction, electrically active defect (hot-spots) or internal field imaging. Similarly to CL, EBIC is strongly correlated to electron-hole pairs creation, at a difference that it uses carrier drift current as imaging signal and thus, it will benefit of generated carriers low recombination rate (as carrier recombination lower the number of free carrier that drift in presence of an electric field).

In semiconductor materials, the displacement of carriers is typically governed by the well-known drift-diffusion equation. When a sample is subjected to an electric field, drift mechanism becomes dominant, where free carriers align their motion along the direction of the field, depending on their polarity. Such a field can be external, when semiconductor is biased and thus giving rise to majority carrier current, or internal, naturally occurring in pn-junctions or under a Schottky contact. Subsequently, if excess electron-hole pairs are generated inside or near (at a maximum distance equal to diffusion length) an electric field, they will be separated and will drift at opposite direction. In a case of a Schottky contact on phosphorous doped diamond at equilibrium, as depicted in fig. II.16, minority holes current can be collected on the Schottky contact. Majority electrons being blocked by the upward band bending caused by Fermi level alignment.

By linearly moving the e-beam focal point across the sample surface, close to a depletion region, an EBIC line-scan can be recorded. This technique enables electric field scanning within the device and further allows the detection of localized defects or hot-spots that cause abrupt changes in the EBIC current. Moreover, leveraging the scanning rate adaptation of the SEM, the collected current can be pre-amplified before being sent to a video card, enabling EBIC mapping or imaging [224]. The pre-amplifier discretizes the current into gray levels, with bright EBIC contrast indicating the presence of high electric fields. Additionally, the quality of metallic contacts can be examined by identifying hot-spots, which correspond to preferential paths of leakage current. An increase in leakage current is observed through an increase in EBIC signal or contrast.

In this manuscript, EBIC imaging has primarily been used to characterize the metallic contact made on phosphorous doped epi-layer, such as the gate pn-junction SCR extension. In the first case, to reach ohmic contact, a large area gate metal deposition have been performed. However, in the case of the c-TLM presented in section II.4.1.b the inner contact is more likely to exhibit Schottky behavior, which can be observed thanks to unbiased EBIC imaging. Applying bias to this structure allows for the observation of electric field crowding defects. In the second case, the imaging of pn-junction SCR modulation enables the correlation between its lateral extension dependence and electrical measurements.

II.4.2.c SEM setup

To generate electron-hole pairs, a FEI Quanta 200 SEM has been used to provide focused e-beam on the sample within an acceleration voltage range from 0.2 to 30 kV.

For CL spectroscopy, samples are placed on a GATAN cooling stage allowing efficient temperature control from liquid helium temperature (4 K) to room temperature (300 K). The light resulting from radiative electron-hole pairs recombination is collected thanks to a hole pierced parabolic mirror which can remotely be placed between the samples and the e-gun column. Light emitted is thus reflected in a collimated beam towards a planar-convex lens before being focalized on the entrance slit of a Horiba iHR550 Jobin Yvon monochromator. The latter is provided with near UV 600 gr/mm or 1800 gr/mm mirror gratings and ±0.025 nm resolution coupled with wavelength accuracy of ±0.2 nm. A CCD (256×1024 matrix pixels), preceded by a photo-multiplier, is finally used to analyse the light emitted and generate CL spectrum.

Concerning EBIC, an home-made removable probing holder station is used to ensure remote contacting of the sample in the SEM chamber. Line-scan measure are performed thanks to a tri-axially wired Keithley 6485 pico-ammeter. For mappings, a Stanford Research System SR570 pre-amplifier is used, discretizing for 16 bits, more than 65,000 gray levels in the range of ±1 V of the associated video card.

Electron-hole pairs creation or generation has been numerously mentioned in previous sections, but an induced hypothesis have been assumed in the latter, being the accelerating voltage

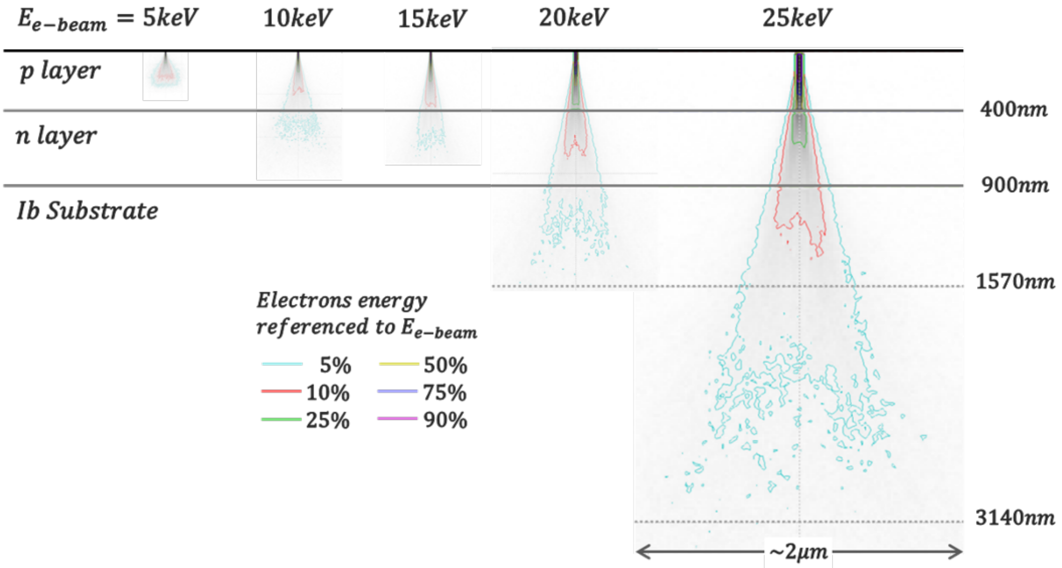

Figure II.17: e-h generation volume in samples PS1 and PS2 calculated by Monte Carlo simulation for different e-beam energies among 5, 10, 15, 20 and 25 keV, and constant number of electrons (e-beam current). Equi-deposited energy lines emphasize main electron interaction depths and have been calculated for 5×10^5 *electrons and a grid mesh of 1nm.*

adaptation as function of the scanned layer. Mechanism involved for electron-hole pairs generation will not be described in details in this thesis as it has already been well described and detailed in literature [224, 293]. Nonetheless, Monte-Carlo simulations, presented in fig. II.17, have been done on samples PS1 and PS2 in order to enlighten the importance of acceleration voltage adaptation regarding to the epi-layer sounding. For the considered structure, to probe only the p-type layer, an e-beam accelerating voltage of 7 keV should not be exceeded. As p-layer have been etched in both samples mentioned herein-above, the phosphorous doped epi-layer is accessible from the front face similarly to the p-mesa structure. For this reason, CL analysis have been performed with an acceleration voltage of 5 keV and at liquid helium temperature.

II.5 Epilayer electrical contacts

Ohmic contacts are crucial for JFETs as they enable efficient current flow in the conduction channel between source and drain electrodes, such as a better gate electrostatic control. These contacts establish low-resistance pathways, facilitating the unrestricted injection and extraction of charge carriers. Such contacts are already well-mastered on p-type diamond, thanks to the use of metallic diamond, reached by high boron incorporation underneath contact metal deposition [248, 300]. Oppositely, realizing ohmic contacts on phosphorous-doped diamond is still very challenging [137, 166, 301], hence particular attention must be paid to this point when fabricating components using these layers like PS1 and PS2 samples. High phosphorus ionization energy [302] makes it difficult to achieve high carrier concentrations and efficient carrier injection at the metal-diamond interface, leading to non-ohmic, so called rectifying, behavior.

II.5.1 Theory for ohmic contact on diamond

Theoretically, achieving ohmic behavior at the boundary of a metal-semiconductor junction requires unimpeded charge injection without any barrier. In an ideal scenario, drift and diffusion of both majority and minority free carrier is ruled by Dirichlet boundary conditions, where the metal and the semiconductor quasi-Fermi level are equal, hence charge-neutrality is ensured on the boundary. However, in practical applications, these ideal conditions are seldom met, and the deposition of a metallic electrode on a semiconductor typically results in a rectifying behavior known as a Schottky contact. This introduces a Schottky barrier φ_b, which restricts carrier injection [208]. Nevertheless, if the barrier height is sufficiently small, careful design can mitigate the additional contact resistance associated with this barrier, making it negligible compared to the resistivity of the semiconductor itself and thus considered as ohmic contact [303]. The latter already obtained for other wide band-gap semiconductors like p-GaN [304] or n-type 6H-SiC [305], has been reached on metallic p-type diamond [248], but is still under investigation for n-type diamond.

II.5.1.a Ohmic contacts vs. Schottky contacts

The Schottky behavior of semiconductor contacts can be effectively explained by the Schottky-Mott theory, which suggests that the band alignment in a metal-semiconductor (MS) junction involves the transfer of charges from one side to the other, resulting in the convergence of quasi-Fermi levels at the interface. As a consequence, a metal-semiconductor junction can exhibit either ohmic or Schottky behavior depending on the differences in work functions between the two materials. In the case of a p-type, boron-doped diamond, an ohmic contact is formed when the metal work function φ_m is higher than that of the semiconductor φ_{sc} (fig. II.18). Conversely, for $\varphi_m < \varphi_{sc}$, the contact becomes rectifying, displaying the characteristic features of a Schottky diode. On the other hand, in the case of phosphorous doping, an ohmic contact is obtained when $\varphi_m < \varphi_{sc}$, while a rectifying behavior is observed for $\varphi_m > \varphi_{sc}$.

One can observe that in the thermal equilibrium of an ohmic contact, as shown in fig. II.18 for boron-doped epilayer, there is an upward bending of the semiconductor bands at the interface, leading to hole accumulation. Forward polarisation of such a junction allows the holes in the diamond to be injected unhindered into the metal, as the holes do not encounter a significant barrier. Conversely, in reverse bias, the upward band bending behaves like an anode or a hole reservoir, which efficiently supply plenty of holes. These statements have been extensively observed and characterized in the case of p-type diamond ([59, 115]). However, they remain hypothetical for (100)-oriented phosphorous-doped diamond as no successful fabrication of an ohmic contact has been reported. In the ideal scenario of an ohmic contact for phosphorous-doped diamond, forward biasing should enable unimpeded electron flow from the diamond toward the metal electrode, considering also an ideal non-negligible proportion of donor being ionized. Conversely, in reverse biasing, the ideal downward band bending should act as an electron reservoir (cathode), efficiently providing an abundant supply of electrons. Alternatively, ohmicity can also be reached thanks to a significant tunneling carrier injection through the contact, reducing the contact resistance to considerably lower value than n-layer sheet resistance. Consequently, for both dopants ideal case described above, the conduction performance would be primarily determined by the layer resistance, following Ohm's law.

Schottky contact is characterized for p-type diamond with a downward band bending, with $\varphi_m < \varphi_{sc}$ near the junction boundary and, at the opposite, an upward band bending $\varphi_m > \varphi_{sc}$ for n-type diamond. This bending can be observed through the diffusion potential V_{d0} in a analogous way to the pre-established built-in potential model for the pn junction. Mott-Schotkky theory describes lower metal work function compared to semiconductor through introduction of a barrier φ_{bn} for electrons, and φ_{bp} for holes, that arises from charge transfer from the semiconductor to the metal. Caused by Fermi-level alignment, charges transfer results in creation of a depletion region W_{sch} where uncompensated ionized donor or acceptor atoms form a space charge region underneath the metallic contact. Bases of transport mechanism already involved asymmetry in the Schottky contact model where electron and hole barriers (for n-type and p-type diamond, respectively) at the semiconductor-to-metal interface are not equivalent depending on carrier injection direction. The diffusion potential, denoted as V_{d0}, represents the barrier experienced by electrons/holes entering the metal from the semiconductor, while the Schottky barrier height φ_b accounts for electron/holes injection toward the semiconductor (applicable

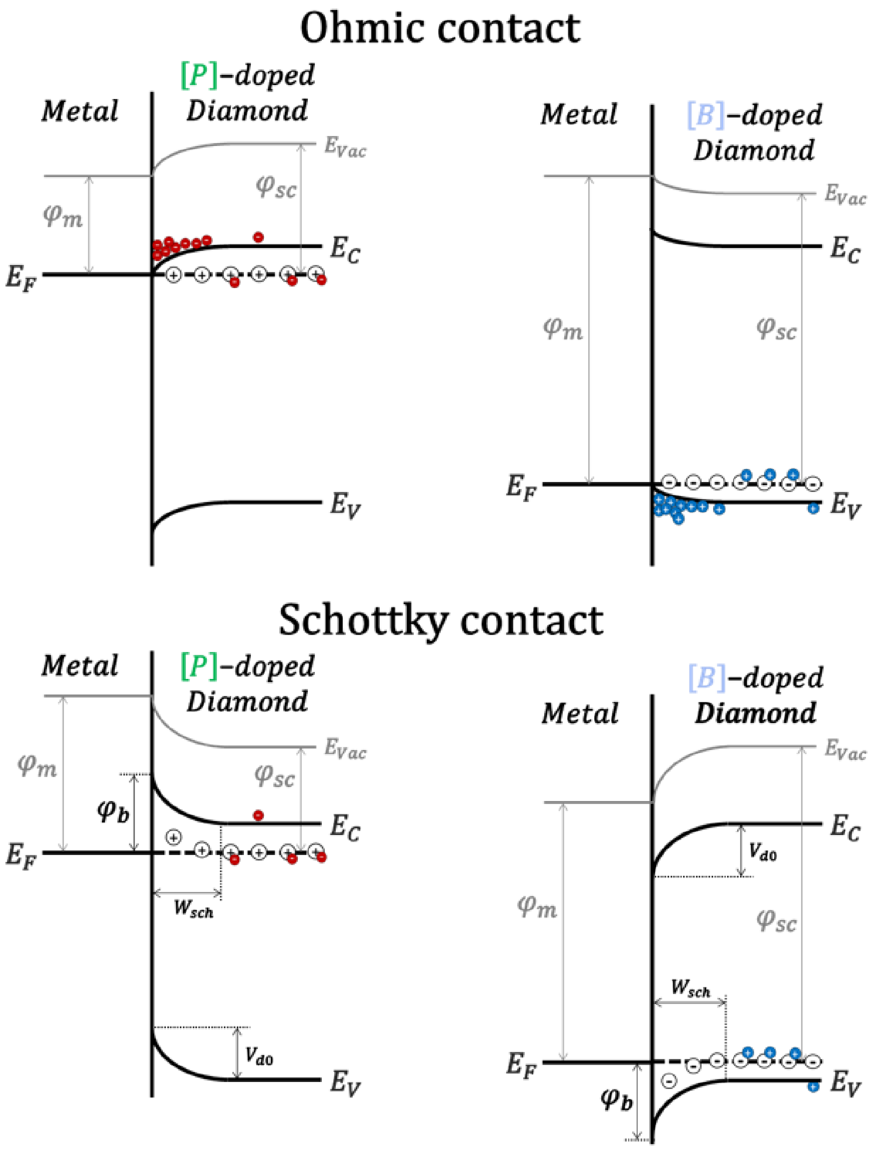

Figure II.18: On the left, band structure of metal/phosphorous-doped diamond Ohmic (Top) and Schottky (bottom) contact, and respectively on the right band structure of metal/boron doped diamond Ohmic (Top) and Schottky (bottom) contact at thermal equilibrium without bias.

to both p-type and n-type). Applying a forward bias voltage higher than the diffusion barrier ($V_{app} > V_{d0}$) enables electrons or holes (depending on the semiconductor type) to be governed by the electric field imposed on the structure. Consequently, they can cross the junction boundary without hindrance as the effective diffusion barrier V_{d0} becomes negligible compared to the electric field. In contrast, in reverse bias (or when $V_{app} < V_{d0}$), the barrier widens, preventing significant free carrier crossing due to the presence of a wide depletion region.

II.5.1.b Contact resistance modelization from charge carrier injection at metal-diamond interfaces

Given the rectifying and asymmetrical behavior of Schottky contacts, the simple application of Ohm's law is inadequate for describing non-linear current transport mechanism. This section aims to provide a better understanding of the leverage parameters influencing the formation of ohmic contacts by exploring the transport mechanisms of carriers across Schottky contacts. It is important to note that this section will only provide a summary of well-established models, as more detailed analyses can be found elsewhere [59, 115, 208]. In the goal of exploring contact resistance provided by Schottky models, only unbiased Schottky diodes are considered. Consequently, factors such as image forces and imperfections in the boundary area are not considered here, although they can significantly impact the Schottky barrier height and, consequently, the contact resistivity. Additionally, tunneling mechanism like Trap-Assisted Tunneling (TAT) and Phonon-Assisted Tunneling Emission (PATE) depicted on Fig. II.19, are not taken into account in this first approach calculation regarding to their strong bias dependence. Even if it should be noticed that, both TAT and PATE mechanisms can contribute to the overall tunneling current with TAT exhibiting its maximum value at low bias and PATE pre-dominance favorized at low temperature operation. Significant presence of traps and their associated energy levels can introduce non-ideal behavior and deviations from the ideal Schottky diode model presented here.

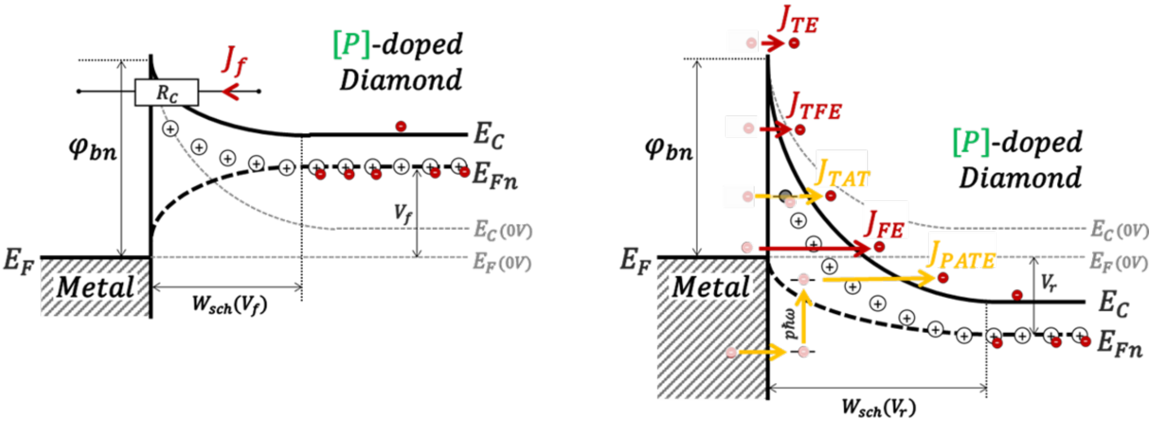

Figure II.19: Forward (left) and reverse (right) polarisation of n-type diamond Schottky contact enlightening diverse current transport mechanisms (valid in both polarisation but only represented in reverse for the sake of clarity).

The evaluation of the specific contact resistance R_C at zero bias serves as a valuable figure-of-merit for comparing the quality of contacts between semiconductors and metals. R_C is independent of the contact surface and is defined as the reciprocal of the derivative of the current density with respect to the voltage across the diode boundary [208]:

$$R_C = \left(\frac{dJ}{dV}\right)^{-1}_{V=0} \tag{II.18}$$

The current density J crossing the metal-semiconductor junction, denoted as J_f for forward biasing and J_r for reverse polarization, can be classified into three main types: Thermionic Emission (TE), Thermionic Field Emission (TFE), and Field Emission (FE). The relative contributions of each component to the total current depend on the temperature and doping level of the semiconductor. To distinguish their contribution, a rough criterion known as the characteristic energy E_{00} is used and compared to thermal energy (k_BT) to identify the ranges where each component dominates (fig. II.20). This criterion, E_{00}, is related to the transparency of the barrier encountered by free particles during the tunneling process [306] and is commonly interpreted as:

$$E_{00} = \frac{q\hbar}{2}\sqrt{\frac{N_{sc}}{m_t^*\varepsilon_{sc}}} \tag{II.19}$$

Where N_{sc} is the semiconductor doping level where it can respectively be N_A for p-type or N_D for n-type, $\varepsilon_{sc} = \varepsilon_r\varepsilon_0$ is the semiconductor dielectric constant and m_t^* the effective mass of the tunneling particle. Raw approximation is done in this manuscript where carrier masses will be used as m_t^*, a choice that can further be completed if needed, but is acceptable for an unbiased approach. Consequently, for holes in diamond, only light and heavy holes are considered, (spin-orbit band is assumed unoccupied as suggested by Richardson constant of 90 A.cm^{-2}K^{-2} [115]) with effective masses $m_{lh}^* = 0.265\ m_0$ and $m_{hh}^* = 0.642\ m_0$ [177, 181]. Similarly, for the free electrons, which are considered the primary tunneling particles in n-type diamond, the effective mass is $m_e^* = 0.496\ m_0$ [177, 307]. As E_{00} is only dependent from doping level, each current transport mechanism contribution is identified below and classified thanks to thermal energy scaling:

Thermionic Emission (TE), $k_BT \gg E_{00}$

When thermal energy is significantly higher than characteristic energy or for low to moderate doping levels, TE dominates and common Schottky barrier behavior prevails without majority free carrier tunneling. TE is a fundamental (electrons in n-type or holes in p-type semiconductor) emission mechanism that occurs when carriers overcome the energy barrier at the metal-semiconductor interface by thermal energy and escape into (reverse polarisation) or from (forward biasing) the semiconductor material. Current transport associated to TE, J_{TE}, is governed by the Richardson-Dushman equation, which derivated through II.18 gives rise to a contact resistance:

$$R_C^{TE} = \frac{k_B}{A^*Tq} \exp\left(\frac{q\varphi_b}{k_BT}\right) \tag{II.20}$$

Concerning free electrons in n-type semiconductor, A^* Richardson constant commonly used is 120 A.cm^{-2}K^{-2}. As the temperature increases, more carriers in the respective region (depending on the polarisation) gain sufficient energy to overcome the Schottky barrier, resulting in an increased J_{TE}. TE is a significant contributor to the total current flow in Schottky diodes, especially at higher temperatures, and plays a crucial role in the device's overall behavior. Equation II.20 also demonstrates that low barrier height is preferred in order to obtain small contact resistance, hence exhibiting a good ohmic contact behavior.

Field Emission (FE), $k_BT \ll E_{00}$

Oppositely to thermionic emission, when the thermal energy is much lower than characteristic energy, hence for low temperature or high doping level, FE is dominant. The latter being referred to a tunneling process where carriers (electrons or holes) overcome the Schottky barrier at the metal-semiconductor interface by virtue of a strong electric field. By the use of Gauss-Poisson equation applied to the Schottky diode, the maximum value of the electric field is reached at the interface and is mainly dependent on the doping level in the semiconductor (similarly to pn-junction interface). Consequently, even without biasing of the diode, a charge carrier present in the vicinity of the metal-semiconductor interface is enable to tunnel through the Schottky barrier giving rise to a contact resistance given by:

$$R_C^{FE} = \frac{k_B \sin(\pi c_1 k_B T)}{A^*\pi q T} \exp\left(\frac{q\varphi_b}{E_{00}}\right) \qquad \text{with} \qquad c_1 = \frac{1}{2E_{00}} \ln\left(\frac{4\varphi_b}{-\varphi_{n,p}}\right) \tag{II.21}$$

Where c_1 is a parameter introduced in the methodology proposed by Padovani and Stratton [308] that compares the barrier height φ_b and $\varphi_{n,p}$, where φ_n represents the energy difference between E_C and E_F for n-type semiconductor and φ_p the energy difference between E_F and E_V for p-type semiconductor. Since the barrier height cannot be minimised beyond a certain point, especially for wide band-gap semiconductors, a good ohmic contact should preferentially operate in this FE tunneling regime.

Thermionic Field Emission (TFE), $k_BT \approx E_{00}$

At characteristic energy E_{00} close to thermal energy, between TE and FE, TFE mechanism dominates as being combination of both models previously mentioned. While FE is a pure tunneling process, TFE involves tunneling of thermally excited carriers experiencing a thinner barrier than in FE. Contact resistance due to TFE is given by:

$$R_C^{TFE} = \frac{k_B\sqrt{E_{00}}\cosh\left(\frac{E_{00}}{k_BT}\right)\coth\left(\frac{E_{00}}{k_BT}\right)}{A^*Tq\sqrt{\pi q(\varphi_b-\varphi_{n,p})}}\exp\left(\frac{q(\varphi_b-\varphi_{n,p})}{E_{00}\coth\left(\frac{E_{00}}{k_BT}\right)}+\frac{q\varphi_{n,p}}{k_BT}\right) \tag{II.22}$$

It has to be noticed that, thermal energy to characteristic energy comparison criterion $E_{00}/k_BT \approx 1$ can be ambiguously defined. The specific range where TFE mechanism dominates current flowing through the metal-semiconductor boundary can strongly differ from a device to another as the range $k_BT \ll E_{00}$ for TE and $k_BT \gg E_{00}$ for FE are non accurate. The latter enlightened in fig. II.20, where arbitrary fixed deviation of 90% have been taken from $E_{00}/k_BT = 1$, is mainly a guideline for the eyes and cannot be used to roughly discriminate and isolate the different mechanism contributions. Consequently, depending on the doping level and contact quality, TFE can be the main contact conduction mechanism or considered negligible compared to the two other mechanisms.

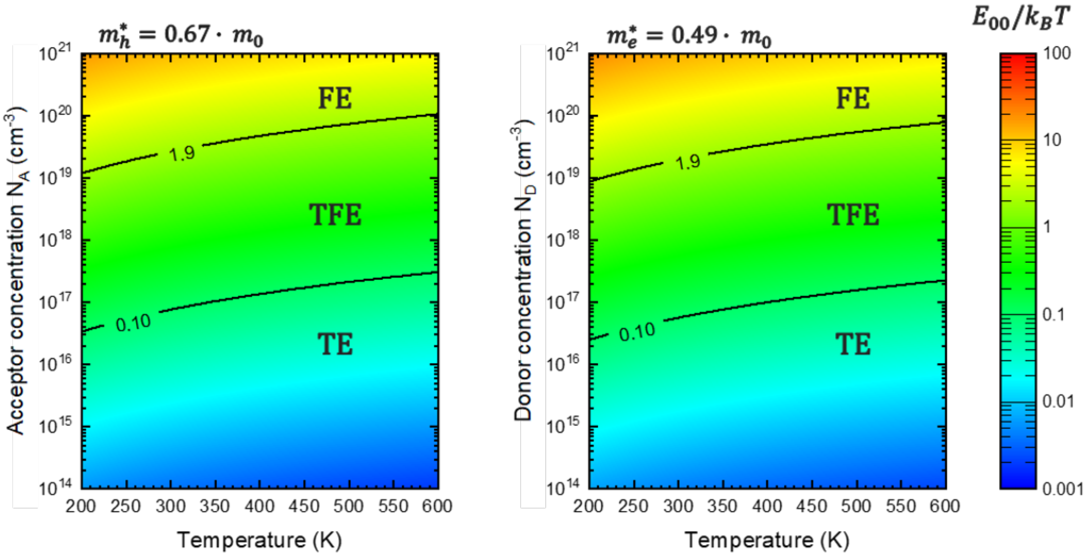

Figure II.20: Ratio between tunneling energy (E_{00}) and thermal energy (k_BT) mapped in color scale versus, temperature T in horizontal axis and acceptor N_A or donor N_D concentration in vertical axis. Left hand graph corresponds to holes for Schottky contact on boron-doped diamond and right hand graph stands for electrons in case of a Schottky contact on phosphorus-doped diamond. Separation of the different regimes is supposed through the solid guideline at $E_{00}/k_BT =$ 0.1 and 1.9.

II.5.1.c Contact resistance vs epilayer doping level

Using the model described in the previous section, the ideal minimal contact resistance can be modelized for both p-type (boron-doped) and n-type (phosphorous-doped) diamond, as reported in Fig. II.21. It is important to note that in order to calculate the lowest contact resistance obtainable, as a function of doping level, the contribution of the three models mentioned above, FE, TFE and TE, is discriminated by the lowest contact resistance value computed. Thus,

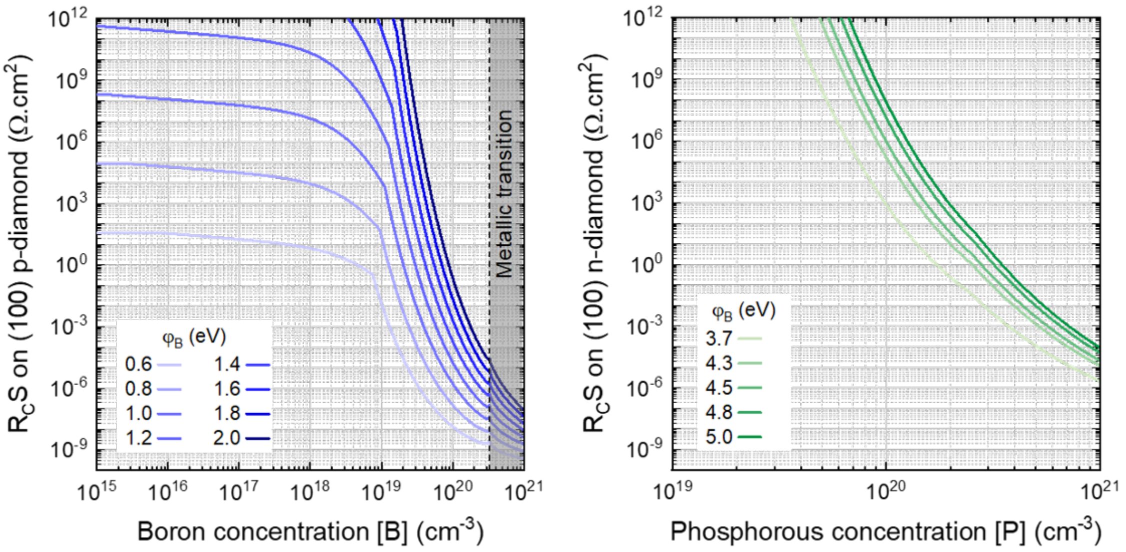

Figure II.21: Specific contact resistance R_C of (100)-oriented, boron (left) or phosphorous (right) doped diamond as function of the doping level. Simulations have been performed at 300K for different commonly reported barrier height for both dopants, according to [309–311].

isolation of each mechanism predominance is considered by the minimisation of the specific contact resistivity.

The specific contact resistances R_C were determined at room temperature, and in the models considered, their variation is primarily influenced by the doping level and the barrier height. In the case of TE dominance, with low doping levels and low barrier heights at room temperature, the specific contact resistances (R_C) are independent to the respective doping concentration and rely solely on the barrier height φ_b. Conversely, in the case of FE dominance, at high doping levels, R_C decreases significantly and abruptly with doping concentration, following a specific dependence proportional to $\exp\left(N^{-1/2}\right)$. However, it should be noted that in cases where FE or TFE predominates, the position of the Fermi level relative to the conduction or valence band (e.g., φ_n for phosphorus and φ_p for boron) becomes crucial. Therefore, these simulations take into account the depth of the donor or acceptor levels, the proportion of ionized dopants, and the compensation effect by considering the position of the Fermi level in the two different epilayers. Furthermore, concerning boron-doped diamond, as the metal-insulator transition is observed [138] for doping level higher than $\approx 3 \times 10^{20}$ cm^{-3}, the model presented here tends to not be valid anymore and more metal/metal consideration [312] should be taken into account. Based on these observations, it is obvious that to achieve low values of R_C, hence approaching contact ohmicity, high doping concentrations, low barrier heights, or a combination of both should be employed.

The development of contact ohmicity on wide and ultra-wide band-gap semiconductors is inherently more complicated than for silicon due to the energy scales involved. Not limited to diamond, the establishment of ohmic contacts is a significant research focus for materials like GaN and AlGaN [313, 314], which remains a constraining element for the performance of high electron mobility transistors (HEMTs). Formation of an ohmic contact was previously introduced as a result of the metal work function being higher than the semiconductor´s (fig. II.18). However, metals does not generally exist with a low enough work function to yield a low barrier on ultra-wide band-gap materials. Especially diamond among them, further taking into account its strongly pinned interfaces. Oxygen termination is widely used in the case of diamond for its positive electron affinity, allowing the passivation of the surface by a pinning of the Fermi level about ≈ 1 eV from the top of the valence band for O-terminated/(100)-oriented boron-doped diamond [311], and 4.4-4.5 eV from the conduction band for O-terminated/(100)-oriented phosphorous-doped diamond [309, 310]. This huge discrepancy, forces low resistive phosphorous diamond contacting to be obtained in high doping level range ($\geq 5 \times 10^{19}$ cm^{-3}) where FE tunneling is predominant. Oppositely, H-terminated diamond with negative electron affinity, gives rise to a potential surface conduction due to accumulated holes [315] but also to a, smaller than O-terminated [316], surface Fermi-level pinning. This potential surface reconstruction during diverse fabrication steps brought the Schottky barrier height to be strongly dependent on the metal work function such as surface termination coverage homogeneity [316].

To summarize, obtaining a perfect pinning-free surface, highly desirable to reach low resistive ohmic contact on diamond is challenging to realize without first achieving an atomically flat surface. To overcome this technical milestone and enhance contact ohmicity, establishment of more heavily doped surface layer [58] or even graphite hetero-junction formation thanks to ion implanted diamond [317] solutions have been developed.

II.5.2 State-of-art for diamond ohmic contact fabrication

II.5.2.a (100)-oriented boron doped diamond ohmic contact formation

Ohmic contact can be easily achieved on boron-doped diamond by narrowing the depletion layer width of a contact by introducing a heavily doped layers between the metal and the diamond active layer. The Schottky barrier thickness decreases, as being dependent on the inverse square root of the doping level, further consequently enhancing the FE tunneling current through the barrier, as represented in Fig. II.22. As an example, the barrier width reported for a doping level of 1.2×10^{21} cm^{-3} is 0.57 nm, which represents less than two atomic mono-layers of diamond with a lattice parameter of 0.37 nm (neglecting the lattice parameter modification reported at high boron content layers [318]). For this doping level and associated barrier width, the lowest specific contact resistance of 2.8×10^{-7} Ω.cm^2 has been reported for (100)-oriented highly boron doped diamond, involving also an annealing at 693 K [248].

For heavily boron doped diamond, the mostly used metal to obtain ohmic contact is titanium (Ti) which presents a good adherence on diamond surface such as a good thermal stability. It is demonstrated that the post-thermal annealing process further enhances the properties of the ohmic contact, being considered that a chemical reaction between Ti and (100)-oriented p-type diamond, such as carbide formation. The well-established titanium carbide (TiC) formation provide an even better adherence of titanium based contact on diamond surface such as a barrier height reduction, increasing the FE tunneling current, hence in turn lowering the specific contact resistance.

From literature, this method has shown efficient reproducibility from its early uses [320] till transistors drain and source specific contact resistances lowering [58, 247]. As reported in Fig. II.22 (bottom right), post-thermal annealing with temperature ranging between 673 K and 873 K efficiently decreases the specific contact resistance of more than one decade [300] but temperature higher than ≈1000 K tends, at the opposite to increase R_C about a decade also [300, 320]. This discrepancy at high temperature could be strongly linked to the different annealing atmosphere qualities used in the different work (not systematically reported) but an affirmation about this difference is complicated to assert. Nevertheless, post-thermal annealing in reasonable temperature range and under inert atmosphere is mandatory to obtain lower R_C, even if heavy boron doping still tends to be more effective in this purpose.

For the positioning of the samples manufactured in this thesis, with a contact layer doping of $[B] \geq 5 \times 10^{20}$ cm^{-3}, a specific contact resistance of less than 10^{-6} Ω.cm^2 is expected. It represents two decades less than reference sample GD-030, that has been processed using the same selective growth recipes, conditions, surface termination and post-thermal annealing as described in section II.1.

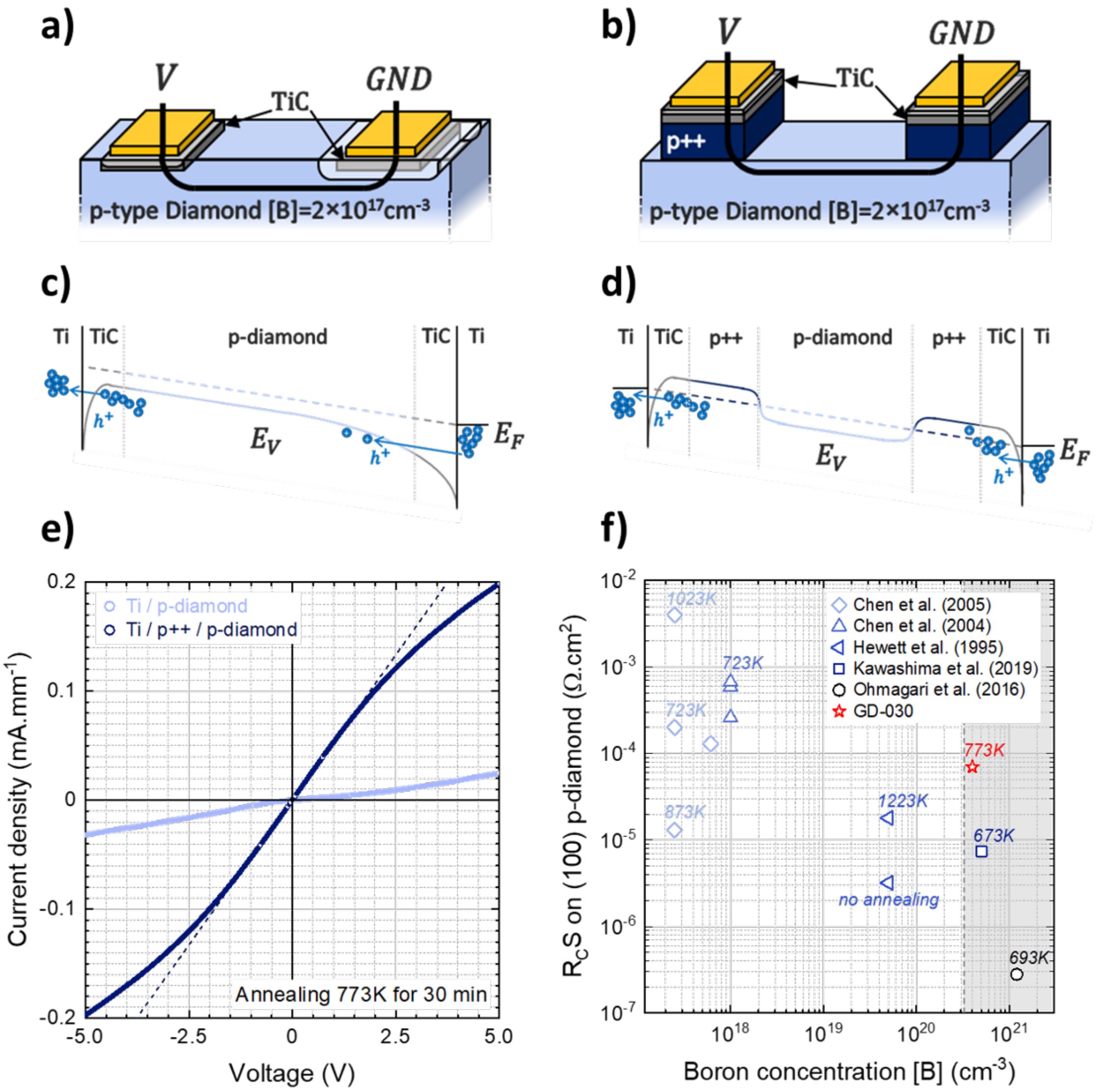

Figure II.22: a) Schematic cross section of metal/p-diamond and b) metal/p++/p-diamond under bias with c) and d) their affiliated band diagram along the conduction lines represented in the schematic cross section. e) both structure respective IV characteristics, measured at room temperature (300 K) between two 15 µm spaced contacts (datas taken from [58]). f) literature reported contact resistance on (100)-oriented boron doped diamond as function of the doping level, for various annealing temperatures, according to [58, 247, 248, 300, 319, 320].

II.5.2.b Phosphorous-doped diamond contacting

Oppositely to boron doped diamond presented before, realization of an ohmic contact on n-type diamond is currently a major challenge for diamond bipolar devices such as pn junctions, considering that no low-resistive ohmic contact on n-type diamond has been achieved yet. Concerning the (100)-oriented phosphorous doped layer, only a few reports attest of the successful operation of fabricated Schottky diodes [135, 309, 310] compared to (111)-oriented layers, better documented since the control of phosphorous incorporation along this orientation is more efficient [143]. However, while actual data concerning (111)-oriented n-type diamond outnumber reports performed on the similar (111)-oriented layers, the latter are thought to be preferred for future device applications. Due to, better electronic quality of (100)-oriented diamond layers compared to their equivalent grown on (111)-oriented substrates [135, 321], at least equivalent contacting performances could be ultimately expected from both orientation.

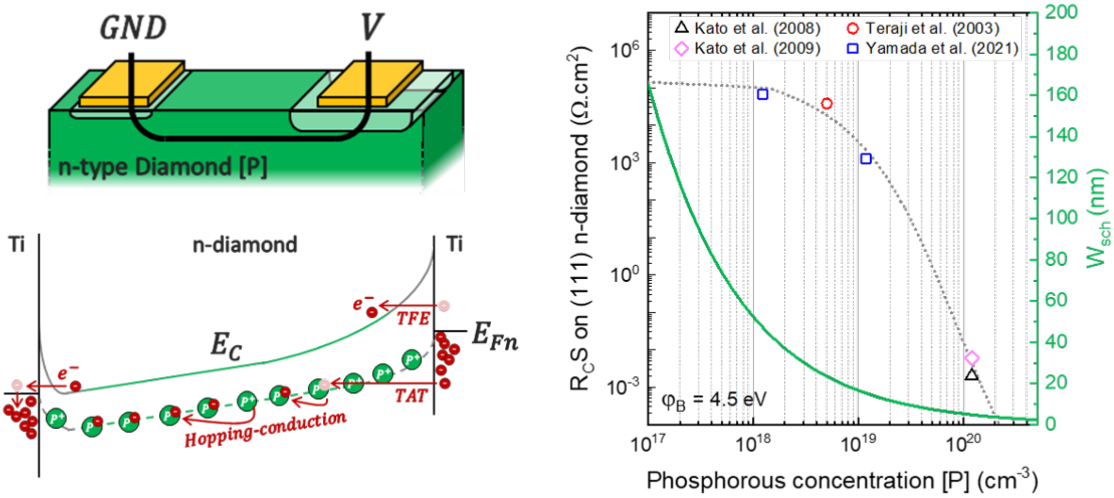

Figure II.23: Left, schematic cross section of Ti/phosphorus-doped diamond under bias and its affiliated band diagram along the conduction line represented in the schematic cross section. Right, specific contact resistance of (111)-oriented phosphorous doped diamond, as reported in the literature [123, 166, 195, 301], depending on dopant concentration, aside with the changes of the barrier width W_{sch} (in green referenced to right axis scale). As a visual guide, a fitting (gray dashed line) has been performed using TFE, TE and FE models to enlighten TFE main contribution among the whole doping level range.

However, regardless, of crystalline orientation, no metal has yet demonstrated a low Schottky barrier height on n-type diamond. A deep Fermi-level pinning, around 4.2-4.65 eV [135, 310] from the conduction band, is observed at the (100)-oriented such as (111)-oriented phosphorus-doped diamond/titanium interface, tentatively attributed to oxygen termination. Furthermore, there is no observation about a similar carbide formation as for the boron doped diamond coupled with no reported benefits from post-thermal annealing. Consequently, the counterpart realistic solution is to improve the carrier injection efficiency by narrowing the barrier width through heavy doping.

Fig. II.23 shows the specific contact resistance of (111)-oriented phosphorous doped diamond, as reported in the literature, depending on dopants concentration, aside with the changes of the barrier width W_{sch}. The specific contact resistance could be lowered to $\approx 10^{-3}$ Ω.cm^{-3} for one of the highest phosphorous doping level reported of 1.2×10^{20} cm^{-3} and using titanium as metal contact [195]. Assuming the same doping level and a commonly reported Schottky barrier height of 4.3 eV, W_{sch} is calculated to be around 5 nm, assuming simple Schottky-junction theory [115]. This depleted region extension, would be still significantly wide to ensure pure FE tunneling process, renown to be an essential transport mechanism to provide low contact resistivity. From the same modelization, to obtain a contact resistivity negligible compared to phosphorus-doped layer bulk resistivity, accounting hopping conduction, a heavy doping level of over 4×10^{21} cm^{-3} would be required [316]. A high value, challenging regarding to the strain involved inside the grown layer such as the poor crystalline quality expected from this heavy phosphorous doping. Additionally, reported contact resistance could be even lowered, down to $\approx 10^{-4}$ Ω.cm^{-3}, thanks to the use of high temperature ($\approx$ 700 K for [P]$= 1.2 \times 10^{20}$ cm^{-3} according to [195]). Thermal instability which unfortunately, even by using high dopant concentration, witnesses of TFE as being the dominant transport mechanism at the present Ti/heavily phosphorus-doped diamond interface, even if other mechanisms, like trap assisted tunneling emission is certainly involved but hard to differentiate.

For JFET fabrication, the challenging realization of ohmic contact on n-diamond gate can significantly hindered the desired bipolar ON-state operation, where minority carrier injection can increase the ON-current. Although, in unipolar regime (no charge injection from the gate epi-layer), a high internal gate resistance, as being the sum of the specific layer and contact resistance, is a considerable curb on gate current leakage. Despite the high contact resistivity of phosphorus-doped layer, this problem was overcome in this work by using surrounding large-area gate contacts. Even if the contact resistivity itself is high, enlarged contact area efficiently lower the contact resistance (as $R_C = \rho_C/S_C$ with S_C the contact area). This guarantees a lower contact resistance than bulk ON-resistance of the n-gate layer, as well as a homogeneous distribution of the gate potential around the active area of the transistors.

II.5.3 NVPS contacts conception

II.5.3.a Phosphorus-doped diamond contact resistivity reduction: tunneling junction proposition

Based on the previously described Schottky diode model, two important building blocks for ohmic contact realisation on phosphorus-doped diamond has been developed: selection of metals with low work function [322] and heavily doped n-type layer [195]. However, even if both of these solutions are mandatory, they were not sufficient to reach low-resistivity ohmic contact. Unimpeded carrier injection through the n-diamond/metal interface is strongly dependent on surface termination which must be released from the consequent Fermi-level pinning to potentially exhibit ohmic behavior. The latter, hard to achieve, is still being under investigation, where innovative diamond surface terminations are tested [323, 324]. Alternatively, a complete change in the crystalline morphology under the contact electrode thanks to graphitization by ion implantation [317] or even Laser-induced defect that enhanced phosphorous incorporation in the lattice [325], have proven promising results. It still have to be noticed that in these two last cases, the contact is not properly made on diamond but on a lattice-altered area, which induce high thermal instability but also eventually diminishes the blocking voltage capabilities of the contact.

Almost a century ago, in 1932, J. Frenkel in collaboration with A. Joffe [312], or L. Nordheim [326], predicted and proposed the possibility of making a semiconductor/rectifying metal contact with the particularity of having a lower contact resistance in reverse than in forward. It was only 25 years later, as a culmination of his thesis work, that L. Esaki [327] reported the fabrication of a pn junction, using metallic germanium (above the insulating metal transition for each), attesting to the feasibility of this type of contact which today bears his name, or mostly referred as tunneling junction. This work exploits the direct band-to-band (BTB) tunneling that appears when both p- and n-side are degenerated and the SCR sufficiently narrow. An electron in the conduction band of the n-side is allowed to tunnel through the SCR, to reach an unoccupied state in the valence band of the p-side. The resulting current increases monotonically in the reverse polarisation, due to the latter tunneling, and exhibits a negative-differential-resistance over the early part of forward polarisation ultimately reaching the exponential increases common of pn junction [208, 327].

To mimic the unimpeded carrier injection of an ohmic contact on phosphorus-doped diamond, it is proposed inside this thesis to explore the potentiality of fabricating a diamond-based tunneling junction as depicted in fig. II.24.

The junctions developed in the course of this thesis are not strictly classified as tunnel junctions with characteristics similar to those of Esaki diodes. This distinction arises because the metal-insulator transition for phosphorus-doped diamond has not been achieved yet, hypothetically assuming its feasibility. Consequently, the emergence of a band-to-band tunneling (BTB) mechanism for diamond may appear to be idealistic and, at its best, of negligible influence. This perception is reinforced when considering the lateral extensions of the space charge region (SCR), which contradicts the notion of increased tunneling effect. Nonetheless, it has been thought here that an elevation in reverse current could be conceived through tunneling from the p-side holes, available in the valence band, to the fixed phosphorous donor state in the n-type

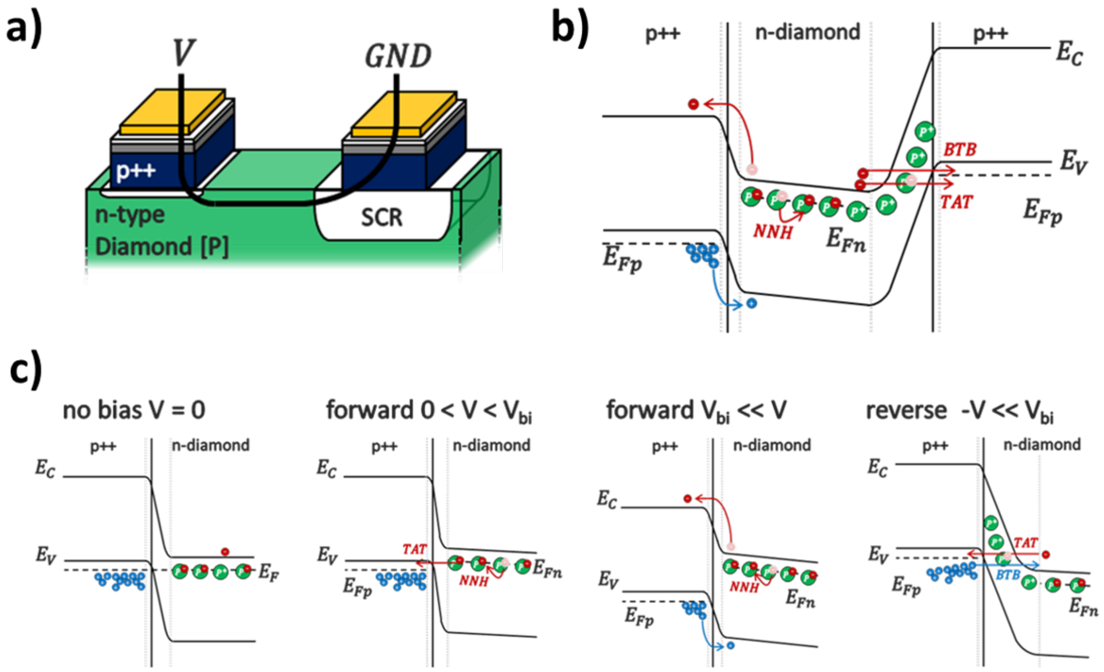

Figure II.24: a) schematic cross section of Ti/p++/phosphorus-doped diamond tunneling junction under bias and b) its affiliated band diagram. c) simplified energy-band diagram of a p++/Phosphorus-doped diamond contact, from left to right: thermal equilibrium without bias; forward bias with low voltage compared to junction built-in voltage, exhibiting TAT emission current at interface and NNH in n-side; forward bias at high voltage reaching diffusion current without tunneling; reverse bias with increased TAT emission and band-to-band tunneling.

region. At room temperature, the deep level of phosphorous donors confines the Fermi level near the donor ionization energy $E_C - 0.58$ eV (with the primary dependence lying in compensation effects). Consequently, a density of states is available for electrons within the p++ diamond valence band, thus augmenting tunneling likelihood and consequently predicting a reduction in junction resistivity.

Currently, a comprehensive grasp of the charge transport mechanisms within a diamond pn junction remains elusive. The intricacy is compounded by the unsuitability of many numerical simulation tools, whether finite element or difference, for diamond materials. This compounds the challenge in conducting relevant simulations and forming consistent anticipations of outcomes. However, the groundwork laid by Garino et al. [328] has significantly advanced our comprehension of conduction mechanisms in diamond pn junctions. Their work has particularly underscored the dominance of tunneling phenomena within such devices. The present study aims to build upon this foundation by extending the analysis into the reverse behavior of diodes. In a first hand this will serve to augment the insights already gathered and offer a more comprehensive perspective. In an other hand, this tunneling-contact appears to offer an elegant solution, distinct from previous achievements, presenting an avenue for unobstructed carrier injection from the gate, consequently enabling substantial amplification of the drain current in bipolar operation mode.

II.5.3.b Ib substrate contacting

The realization of ohmic contacts on n-type diamond has been proved challenging, partly owing to the deep donor level formed by phosphorus ($E_A = 0.58$ eV). The situation is even more daunting for nitrogen-doped diamond, where the donor level is notably deeper at 1.7 eV from the bottom of the conduction band. This presents a significant obstacle to the fabrication of ohmic contacts on nitrogen-doped diamond, which can even be deemed close to impossible. However, this challenge can potentially be bypassed by employing large contact areas. It enables achieving an absolute contact resistance lower than the consequently high substrate resistance, reported in the range of a few tenths of GΩ even under non-equilibrium conditions induced by white light illumination at 11 mW/cm^2 [241].

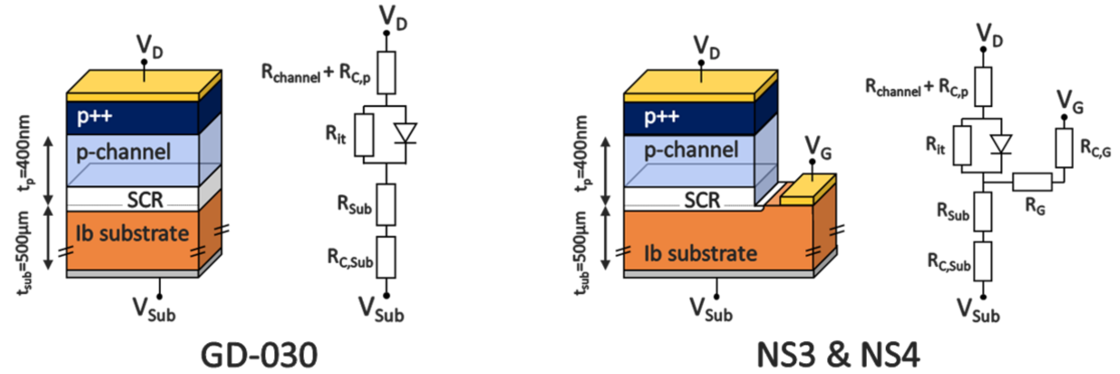

Figure II.25: Comparative schematic cross-section and equivalent gate-to-drain electric sub-circuit representation of GD-030 reference sample, NS3, and NS4 samples. In the former, p-channel electrostatic control is achieved through a bottom-face substrate contact (silver paint), while in the latter, the gate contact (Ti/Pt/Au) is strategically positioned on the top-face, in proximity to the p-mesa.

The reference sample GD-030, illustrated in Fig. II.25, features back-face contact of the Ib substrate achieved through the uniform application of silver paint across the entire substrate surface. Given the dimensions of 4×4 mm^2, the contact resistance $R_{C,Sub}$ is presumed to be lower than the resistance of the thick substrate, denoted as R_{Sub}. This presumption is substantiated by the effective modulation of substrate resistivity, as depicted in Figure III.1. However, the differentiation between these two resistance contributions has been challenging in the as-fabricated stack due to the lack of control over current line spreading (conduction line cross section) within the substrate. Nevertheless, observations made during various bonding-detachment processes revealed that annealing at temperatures exceeding 550K significantly enhances the conductivity of this back-face contact.

For the samples manufactured within the scope of this thesis, an alternative contacting approach has been proposed. This solution is particularly relevant for NS3 and NS4 samples, which also employ the Ib substrate as the JFET gate layer. In this approach, the gate contact is positioned closer to the active area of the transistor, specifically on the top face of the stack. According to previously documented findings [58], it was anticipated that the gate resistance R_G will be significantly lower than R_{Sub}. This reduction in internal gate resistance is projected to enhance carrier injection during bipolar mode operation and elevate the dynamic performance of the fabricated JFET. However, this improvement may come at the cost of elevated gate leakage current and a potential reduction in reverse blocking voltage capabilities. Predicting an increased value for the gate contact resistance $R_{C,G}$ is more challenging to ascertain. The reduced gate contacting surface inherently leads to higher contact resistance. Nevertheless, the deposition of metallic contacts using Ti/Pt/Au, along with subsequent post-thermal annealing, offers better control and cleaner results. This improved process control holds the promise of achieving more reproducible outcomes despite the smaller contact area.

It's important to note that when splitting $R_{C,G}$ and R_G as counterparts to $R_{C,Sub}$ and R_{Sub}, respectively depicted in fig. II.25, a voltage-divider equivalent circuit is created. Consequently, significant values of both resistances can substantially impact the effective bias applied at the SCR edge, leading to a disruptive forward shift of the threshold voltage in the fabricated transistors. However, while achieving ohmic contacts is mandatory for optimized, high-performance devices, the electrical control of p-channel conductivity is still ensured, mainly relying on the voltage applied at the SCR edges. Moreover, PS1 and PS2 samples, benefiting from phosphorus-doped gate layers, are also designed with top-face gate contacts. The higher ionization ratio of these layers will enhance conductivity, thus providing better electrostatic control of the devices with the expected trade-off of higher gate leakage current.

II.6 Conclusion

This chapter drew upon the physics of the pn junction and existing literature to project the expected performance metrics for the simplest lateral JFET design. This encompassed aspects such as conductivity and blocking voltage capabilities, while also predicting JFET characteristics based on established models and parameters. In recognition of the inherent challenges associated with working on small-sized diamond samples and the complexities surrounding high-quality n-type diamond growth, an emphasis was placed on streamlining the technological steps. Especially reducing their numbers is a crucial point to lower process-induced defect density, required to envisage large-scale devices. Consequently, the lateral large-scale inter-digited JFET architecture was optimized to align with these considerations. While more intricate designs theoretically hold the potential for superior performance, they would necessitate further advancements in fabrication processes and diamond growth control.

The interdigited JFET architecture, while strongly compatible with NVPS fabrication, could necessitates further optimizations that are often counterproductive for NVPS performance, and vice versa. One remarkable aspect of this trade-off relates to the metallic covering of the p++ layer source and drain contacts, which plays a critical role in enhancing on-state conductivity but can hinder the light collection efficiency of the NVPS. Striking a balance between these two aspects required trade-offs in design, but perfect design for both applications can be reached even if they would require more complex models and fabrications process. The discussions in this chapter operated on the assumption of ideal pn-junctions or layer contacts, where no parasitic charges or defects were present. The use of 1D equations was prevalent in these discussions. However, it's crucial to acknowledge that unintentional impurities, structural defects, and inhomogeneities can significantly impact layer resistivity. In some cases, they can render the device nearly insulating, effectively eliminating JFET operation and characteristics. Additionally, the 2D geometry effects, particularly the influence of edges, were not considered in the model employed here. These considerations pose challenges in terms of prediction and are intricately tied to the fabrication process. A more comprehensive evaluation of their impact will be addressed in the subsequent chapter.

Chapter III

Samples fabrication and layer characterisation

This chapter delves into the fabrication and layer characterization of the optimized JFET architecture proposed in the previous chapters. While ideal structural and geometrical parameters have been computed through specific trade-offs, fabrication processes have an inherent margin of error that can strongly impact desired technical specifications of the JFETs. As part of the fabricated transistors have been reported electrically insulating, a failure analysis is conducted and discussion are opened around impact of the diverse parameters divergence regarding functionalization of the devices.

III.1 Ib HPHT diamond substrate

As qualitative and renown base for lateral FET, diamond Ib substrate grown by High-Pressure/High-Temperature (HPHT) have been used for the four fabricated samples as foundation block. This 4×4 mm^2 substrate are provided by SUMITOMO Electric Industries and their electrical and optical properties, as being the starting point of this work, are presented along this section.

III.1.1 Electrical grade

Typically, in the applied temperature gradient method used for HPHT-growth process [329], high nitrogen contents have been observed in as grown diamond. Such impurity incorporations have been proven to be caused by the presence of residual nitrogen in the growth environment, which is provided in the metal solvent/catalysts and/or by the adsorbed nitrogen on the diamond powder that is used as carbon source. Subsequently, SUMITOMO substrates are generally provided with a nitrogen content, affiliated with the growth conditions, in a range of 10 to 200 ppm.

Moreover, substitutional nitrogen has been proven to act as deep donor [94, 239], with an ionization energy $E_{D,N} = 1.7$ eV, which is too high to reach low resistivity layer at room temperature. Resistivity of 10^{16} $\Omega.cm$ have been reported [330] for the same substrate, also provided by SUMITOMO for a nitrogen content ranging between 140 and 200 ppm. This content measurement supported by secondary ion mass spectroscopy (SIMS) also enlightens other incorporated species like, 20 ppm of aluminium, 1 ppm of iron and 1 ppm of nickel, coming from solvent alloy composition. This various species incorporation, is considered negligible for devices fabrication as nitrogen doped substrate are mainly used for their insulating properties, but in this work it will further be discussed in the next chapter that they can form traps and impact robustness of the non-volatile off-state provided by the NVPS.

Nitrogen, as being one of the most dominant impurities in both natural and HPHT synthetic diamonds, is therefore the main substrate impurity to characterize. Especially neutral single nitrogen placed in substitutionnal site of the diamond lattice, called N_S^0. Indeed, even if high nitrogen content (140-200ppm) has previously been reported through SIMS analysis, it does not reflect the number placed in substitution of a carbon atom, hence the activated nitrogen content. During harsh HPHT growth condition, nitrogen atoms are frequently segregated along the growing (111) planes in preference to others. Consequently, sectoral nitrogen incorporation occurs which can differ nitrogen concentration by a factor up to 100 [331]. Moreover, this incorporation preferential site is more likely to produce nitrogen dimer known as A-centers (two nearest neighbour susbtitutionnal nitrogen) or trimer, such as aggregates who exhibit totally different impurity behavior than N_S^0.

Taking into account various discrepancies in nitrogen lattice positioning, the effective density of substitutional nitrogen commonly reported for this substrate falls within the range of approximately 10^{19} cm^{-3}. It is essential to highlight that throughout this manuscript, the term "semi-insulating" is used to refer to the commonly used Ib substrate, as its resistance R_{Sub} can be efficiently modulated by the application of illumination (as shown in fig. III.1, previously reported for GD-030 sample) or by temperature increase, as reported in previous work [58]. The electrical properties of the substrate strongly depend on the operating conditions, which can be deliberately adapted for electro-optical device control [332], or inadvertently leading to detrimental effects. Therefore, the designation "semi-insulating" tends to be more appropriate. Considering the strong dependence of the substrate's electrical properties on the operating environment, it is crucial to conduct optical and compositional studies of these Ib substrates. These investigations will provide valuable insights and enable better understanding and control of the substrate's behavior in various applications.

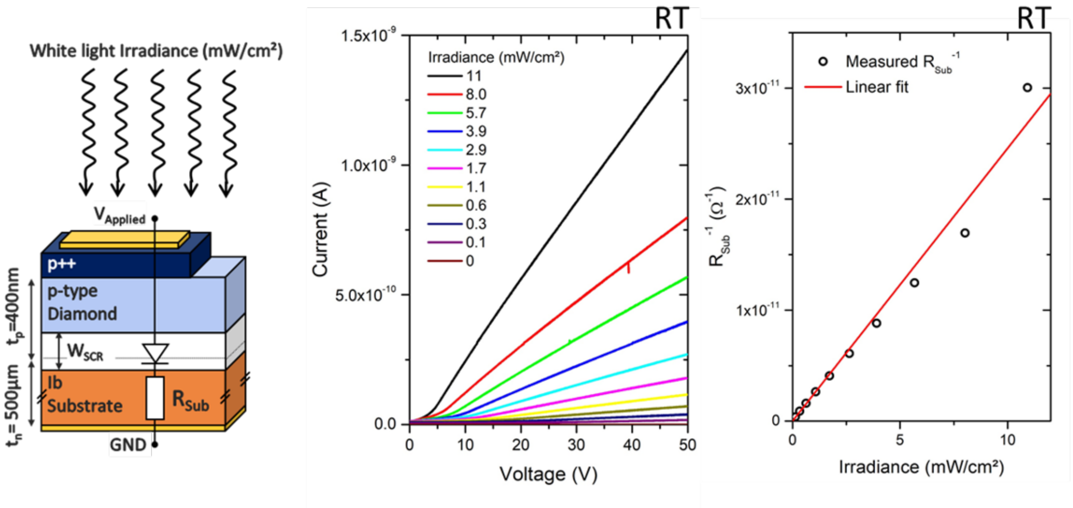

Figure III.1: Left, schematic cross section of pn diode using thick Ib substrate as n-type layer, under illumination. Equivalent electrical circuit is superimposed while substrate's backside is contact with silver paint. Center, forward IV characteristics of the diode, measured for different irradiance and ensuring a dark current below detection limit of 1 pA. Right, extracted R_{Sub}^{-1} as function of the irradiance, exhibiting a linear dependence proportional to free electron density photo-generated. Graphs from [58].

III.1.2 Optical properties

Defects or impurities present in the diamond lattice may induce a dipole momentum that modifies photon absorption of the semiconductor which can then be separated in two categories: electronic or vibronic absorption. Considering pure intrinsic diamond, electronic absorption, ruled by energy conservation, can only occur when the energy of the incident electromagnetic wave (e.g. illumination) is sufficient to promote a charge carrier from the valence band to the conduction band. Consequently, intrinsic, impurity free and free of lattice extended defects diamonds are transparent above UV region (regarding to the wavelength). This purely hypothetical and ideal case reach a limit where strong fundamental absorption due to electron-hole photo-excitation across the indirect band gap starts at 225 nm.

Point defects, like nitrogen, efficiently modify the electronic configuration of the band-gap and thus, leads to a change of the periodic boundary structure of the lattice. Subsequently, electronic transitions may occur between the defects energy states within the band-gap. These transitions are allowed through energy quantum absorption, like single photon, equal to the energy that separates the states, giving rise to sharp absorption features commonly reported as zero phonon lines (ZPL) [103].

Previously mentioned in the last section for exciton, as diamond is part of indirect band-gap semiconductors, optically induced transition frequently involves phonon. In this case, illumination electromagnetic wave may be coupled to a defect related bond vibration, ensuring energy and momentum conservation resulting in a vibronic absorption. Due to temperature, diamond atomic nucleus vibrates around an equilibrium position, giving rise to a charge deformation with the surrounding electrons, thus generating a small oscillating electric dipole. Normally in defect free intrinsic diamond, this induced dipole momentum caused by a single phonon is nonexistent as diamond inversion symmetry efficiently prevents this formation [333]. Indeed, neighbouring carbon atoms would have equal displacements and induced dipole momentum, but opposite and π out of phase, translated in this case by a null wave-vector (k = 0). In the case of nitrogen incorporation in diamond lattice, the absorption coefficient of the sample is directly proportional to the effective dipole momentum squared. Meaning that, illumination absorption intensity by nitrogen vibronic absorption is proportional to the number of optically active centers available.

The latter properties have been used in this work to control the N_S^0 concentration through Fourier transform infrared spectroscopy (FTIR). Furthermore, as optically-controlled JFET switching states and dynamics are dependent on the light collection efficiency of the structure, transmittance measurements have been performed on the Ib substrate. Photo-ionization of the N_S^0 with direct electron transition to the conduction band produces strongly rising photon absorption from the green to the blue spectral region. Absorption that has been observed starting from $E_{D,N} = 1.7\ eV$ and rising continuously to the band edge.

III.1.2.a Transmittance measurement

Transmittance measurements that have been performed on a Ib substrate provided by SUMITOMO Electric by the use of a PerkinElmer Lambda 900 UV/VIS/NIR Spectrometer is shown on fig. III.2.

Absorption toward the near infrared (NIR), ranging between 900 nm and 1600 nm illumination wavelength, is almost constant in this region with 25% of the light being absorbed or indistinguishably reflected (reflectance has not been normalized). As no observable nitrogen related state transition in the detection range of the spectrometer were expected in this range, punctal defect impurities is hard to de-correlate from sample reflectance which arise from the front or backside of the substrate. Considering that all the light is reflected in this range, and thus no impurity-related absorbance, give rise to an optical index of $n = 2.371$, consistent with the result obtained in literature [103] in this range and for Ib diamond.

Abrupt transmittance change at 840 nm is due to the spectra being recorded in two stages. Internal monochromator, such as filtering optics, used within this apparatus needs to be adapted as function of the spectral part observed. In the case presented in fig. III.2, spectrum in the UV/VIS range (200-840 nm) is juxtaposed with a spectrum recorded in the NIR range (840-1600 nm). As no representative scaling factor have been introduced, an abrupt change arise on the reconstituted spectrum with no physical phenomenon meaning other than instrumentation being adapted. Absorption coefficient α has been extrapolated from transmittance measurement using common Beer-Lambert law as:

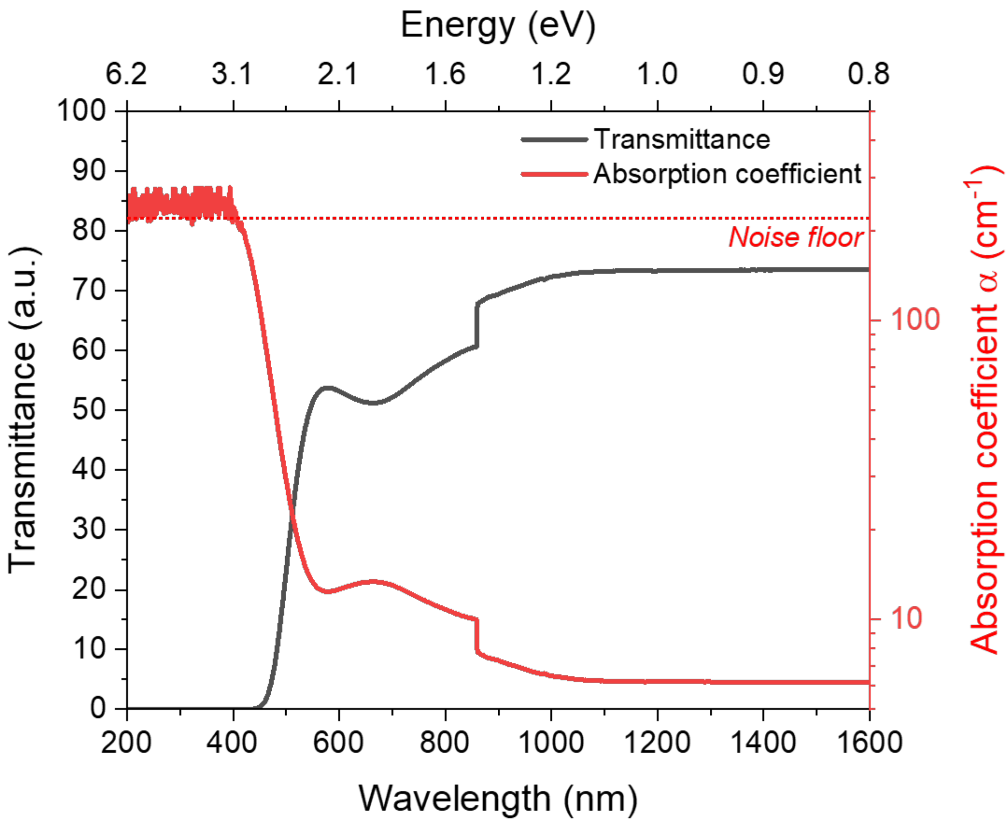

Figure III.2: Ib HPHT diamond substrate transmittance on the left axis (black curve) and calculated optical absorption coefficient on the right axis (red curve), as function of illumination wavelength or energy.

$$\alpha\ (\mathrm{cm}^{-1}) = \frac{\ln(\mathrm{T}_\lambda)}{t_{sub}\ (\mathrm{cm})} \tag{III.1}$$

Where T_λ is the transmittance measured for a defined wavelength and t_{sub} the substrate thickness (0.5 mm), here expressed in cm as α is commonly expressed in cm^{-1}. Using the Beer-Lambert law implies a strong assumption about the level of doping, which is then considered to be homogeneous and uniform in the layer being measured. As mentioned before in section II.3.1.d, this assumption can be further discussed but, taking into account the well-mastered HPHT growth conditions, substitutionnal nitrogen density has been considered homogeneous in this part.

Interesting spectral part to attest of substitutional nitrogen presence is below 800 nm, in the visible range. The transmittance declines with illumination wavelength increase, hence absorption coefficient rises, starts at 580 nm corresponding to an illumination energy of 2.14 eV. This absorption augmentation is referenced as witnesses of high susbtitutionnal nitrogen content of the substrate. The latter photo-ionization process starts to occur when the illumination energy is higher than 1.7 eV (720 nm). However, this represents the minimal energy for an electron to reach the conduction band minimum, which means a strongly localized process. Increasing the photon energy allows excitation of the same electron higher in the conduction band, corresponding to delocalized states. This implies that the optical capture cross-section for substitutionnal nitrogen increases with the illumination energy [334], hence the absorption increases. It is important to notice that for illumination lower than 400 nm ($\geq$3.5 eV), the 500 μm thick Ib substrate used are opaque, hence most of the light applied on the sample is absorbed close to the surface.

Although high concentration of nitrogen is revealed thanks to transmittance measurement, no clear quantification could be performed. Unfortunately, no absorption peaks have been observed at 720 nm, demonstrated by Khan et al. [335] to be strongly correlated with N_S^0 concentration. For this purpose, more accurate technique FTIR spectroscopy, has been employed to quantify nitrogen incorporation in the Ib substrate used.

III.1.2.b FTIR spectroscopy

Fourier Transformed Infrared (FTIR) spectrometer uses a Michelson interferometer to provide, through Fourier transformation, absorbance and/or transmittance of the tested sample. Compared to a conventional dispersive spectrometer, FTIR spectroscopy allows for faster acquisition of spectra with an enhanced signal-to-noise ratio. It benefits from multiplexing (or Felgett) acquisition, where all wavelengths are measured simultaneously, and it avoids the need for a series of slits to restrict light input, which is a characteristic feature of dispersive spectrometers (known as the Jacquinot or throughput advantage). For this purpose a Nicolet FTIR spectrometer from Thermo-Fischer has been used to characterize Ib HPHT diamond substrate provided by SUMITOMO Electrics. Data presented in Fig. III.3, have been recorded by J.Bousquet (from Diamfab), on a raw substrate from the same batches than the one used to fabricate the devices presented in this manuscript.

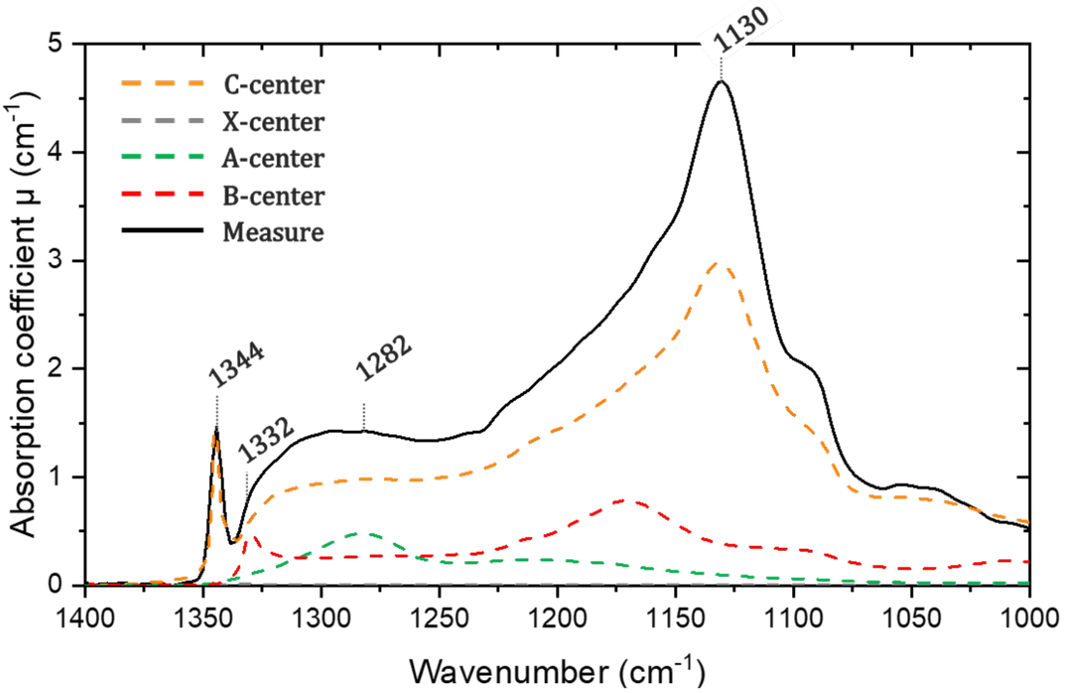

Figure III.3: Measured spectra of nitrogen-related defects centers in the diamond one phonon region at room temperature (full line). Dashed lines represent the absorption spectra of 1 ppm of single defects commonly reported in literature [336–338] which have been scaled thanks to multiplying factor in order to enlighten convoluted fit performed on the experimental data.

Feature offered by FTIR spectra is the sample thickness determination as it relies on the characteristic oscillation patterns generated by interference effects. The Michelson interferometer compares the light-wave path lengths of a fixed reference and a variable one, which are then recombined prior to sample traverse. Without delving into intricate details, the signal amplitude of the Fourier transform acquired after passing through the sample can exhibit typical resonance oscillations. Through dual electromagnetic wave interference model and assuming knowledge of the optical index of the observed material, this resonance phenomenon enables precise determination of the samples thicknesses. For its lack of interest, detailed calculations are not developed, but a substrate thickness t_{sub} of 518.5 (± 16) μm have been computed concerning the Ib substrates used in this work. In line with the range announced by the provider, this value will be used in turns throughout next chapters of this manuscript, even if previous calculations that considered a thickness of 500 μm remain in good agreement with the measured value.

Absorbance spectra were therefore recorded on the basis of the proportionality between the intensity of absorption by optically active centers and the density of these centers available in the substrate. Subsequently for thick layers, extrapolation of the absorption coefficient can be also made through Beer-Lambert law, but adapted for absorbance [339]:

$$\mu\ (\mathrm{cm}^{-1}) = \frac{2.303}{t_{sub}\ (\mathrm{cm})} \log_{10}\left(\frac{1}{(1-\mathrm{A}_\lambda)}\right) \tag{III.2}$$

Where A_λ is the measured absorbance at a defined wavelength which can be expressed $\mathrm{A}_\lambda = 1 - \mathrm{T}_\lambda$. Alternatively, and mandatory for small thicknesses diamond layers, the intrinsic multi-phonon absorption at 2000 cm^{-1} can be used to normalise and baseline the absorption coefficient, equal to 12.3 cm^{-1} according to [340]. In this work, equation III.2 has been used to compute the absorption coefficient, giving a rise to a value of 12.38 cm^{-1} at 2000 cm^{-1} wavenumber, hence already in good agreement with literature. Once the spectra depicted in fig. III.3 have been baselined, convoluted Lorentzian line-shapes are used to fit and replicate the spectrum recorded.

Common nitrogen related defects give rise to well characterised infrared absorption spectra in the one-phonon region (1000-1400 cm^{-1}), relying on different nitrogen bounding or position in diamond lattice. In this range, calibration factors have been empirically calculated [336–338], relating absorption coefficient at a specific energy to single defect concentration, reported below:

$$\text{C-center } (N_S^0):\quad \mu_{1130} = 25\ (\pm 5)\ \text{atomic ppm per cm}^{-1} \tag{III.3}$$

$$\mu_{1344} = 37.5\ \ \text{atomic ppm per cm}^{-1} \tag{III.4}$$

$$\text{X-center } (N_S^+):\quad \mu_{1332} = 7\ (\pm 0.5)\ \text{atomic ppm per cm}^{-1} \tag{III.5}$$

$$\text{A-center } (N_2):\quad \mu_{1282} = 16.5\ (\pm 1)\ \text{atomic ppm per cm}^{-1} \tag{III.6}$$

$$\text{B-center } (N_4V):\quad \mu_{1282} = 79.4\ (\pm 8)\ \text{atomic ppm per cm}^{-1} \tag{III.7}$$

Spectra affiliated to each single centers from equation III.3 to III.7 are depicted in fig. III.3 (dashed lines), where a multiplying factor has been used to obtain a realistic convolution fit of the experimental data. Starting with substitutionnal neutral nitrogen N_S^0, deconvoluted absorption coefficient $\mu_{1130} = 2.96\ cm^{-1}$ and $\mu_{1344} = 1.47\ cm^{-1}$ have been measured, corresponding to $N_S^0 = 74\ (\pm 14.8)\ ppm$ and $N_S^0 = 55.1\ ppm$ respectively. Averaging both value and associated standard deviation give a value of $N_S^0 = 64.5\ (\pm 7.4)\ ppm$ translated as $[N_S^0] = 1.13 \times 10^{19}\ cm^{-3}$. Furthermore, ionized substitutionnal nitrogen N_S^+ representing the X-center, seems to not participate to substrate absorbance, as absorption coefficient peak at 1332 cm^{-1} could mainly be described thanks other broad band participation. Subsequently, the substitutionnal nitrogen concentration measured $N_S = N_S^0 + N_S^+$ can be reduced to $N_S \approx N_S^0 \approx 10^{19}\ cm^{-3}$, in good agreement with the range announced by the provider, SUMITOMO Electric and with previous assumptions [58].

Additionally, di-nitrogen and nitrogen aggregates impurity band raised from measurement deconvolution. Both impurity is referenced [336, 338, 341] to enhanced absorption coefficient at the same wavenumber 1282 cm^{-1} and thus needs to be deconvoluted by the use of the full spectral range. In measure reported in fig. III.3, A-center is pro-eminent compared to B-center. Calculation using equation III.6 and III.7, respectively denote a di-nitrogen concentration of $[N_2] = 7.7\ (\pm 0.5)\ ppm = 1.3 \times 10^{18}\ cm^{-3}$ and nitrogen aggregates (coupled with a vacancy) concentration of $[N_4V] = 20.6\ (\pm 2)\ ppm = 3.5 \times 10^{18}\ cm^{-3}$. Meaning that nitrogen aggregates, non-negligibly representing 22% of the total nitrogen incorporated (only considering the impurities aforementioned), have been favorized over di-nitrogen, with 8% of substrate nitrogen related impurity composition, during the HPHT growth process. Furthermore, this analysis considers only the main one-phonon region centers. Other centers such as N_n or N_nV_m centers can be observed using alternative methods, such as photo-luminescence, specifically for NV centers.

III.1.3 Ib Substrate contents summary

The Ib HPHT substrate provided by SUMITOMO Electrics was thoroughly investigated for its nitrogen content, serving as foundation tile for the fabricated transistors. These substrates are preferred due to their insulating properties resulting from electron deficiency at room temperature. The latter being provided by substitutionnal nitrogen preferential incorporation during the HPHT growth process. FTIR spectroscopy analysis revealed a substitutional nitrogen concentration of approximately $N_S \approx 10^{19}\ cm^{-3}$, in line with the values provided by the supplier. Additionally, the substrate thickness was found to be reliable, measuring approximately $t_{sub} \approx 500\ \mu m$. Transmittance measurements further confirmed and highlighted the presence of the substitutional nitrogen, manifesting as sub-band-gap absorption starting from 600 nm illumination and progressing towards near-total absorbance for wavelengths below 400 nm. Multiples nitrogen complexes, coupled or not with vacancies, have also been observed among theses substrates. Their concentration not exceeding 30% of the total nitrogen incorporation will be considered as negligible for the next sections, except for their potential donor trap states that can influence memory freezing off-state robustness, which will be developed in section IV.4. Although, through the technique used within this work, no compensating impurity concentration could be evidenced, the presence of impurities other than nitrogen cannot be ruled out. Nevertheless, these Ib substrates still exhibit the lowest dislocation density among synthetic diamond. A highly valuable property for innovative (100) phosphorous-doped epi-layer growth, presented in the next section, where dislocations propagation can be seen as killer defect for the fabricated devices. Remarkably, no building block has been added from substrate characterization, but its content precise knowledge will offer better understanding of NVPS working principles and subsequently, more relevant levers for action concerning its future embedded electronic implantation.

III.2 (100) Highly phosphorus-doped diamond

To partially solve absence of free electron in nitrogen doped diamond, which hindered JFET control and performances, a highly phosphorous doped diamond epi-layer has been grown on top of previously studied Ib substrates. This 500 nm thick layer has been grown by R.J. Nemanich and F. Koeck from Arizona State University (ASU). A constant doping level of $[P] = 10^{19}\ cm^{-3}$ for the first 400 nm, starting from interface with Ib substrate, has been targeted for the growth, while the last 100 nm doping level is linearly decreasing for technical issues, until a value of $[P] = 10^{17}\ cm^{-3}$, as detailed in section II.3.1.d.

Frequently mentioned in this manuscript, technical realisation of mono-crystalline phosphorous doped diamond homo-epitaxial layer was historically very challenging compared to boron doping. Theoretical calculations predicted that substitutionnal phosphorus P_S, should form a shallow donor states in diamond lattice [342], even if its incorporation was also predicted to be difficult due to low phosphorous solubility in diamond [141]. The latter being caused by atomic phosphorus size compared to carbon, which can induce strong lattice distortion or reconstruction. Additionally, phosphorus incorporation has been demonstrated to be more efficient along the (111) growth direction rather than (100), justifying the earlier development of high crystalline quality layer on (111) orientation [133, 343] compared to (100) direction. The first successful demonstration of (100)-oriented highly phosphorous-doped diamond layers was conducted by Kato et al. in 2004 [143]. Unique CVD growth conditions were employed for the epitaxial growth of phosphorous-doped diamond layers along this crystalline orientation, which differed from those used for (111)-oriented growth. It should be noticed that even if the doping control was limited ($\approx 10^{18} - 10^{19}\ cm^{-3}$) in this proof of feasibility, the reported Hall mobility was relatively high. These findings provided hope for the future development of higher-quality n-type diamond layers in the (100) orientation, awaited to allow better performances, compared to (111)-oriented diamond.

Nowadays, different teams around the world reported successful phosphorous-doped diamond growth along the (100) crystalline orientation [344, 345], but no usage evidence of these layers inside lateral JFET has, up to now, ever been reported. Considering the fabrication difficulty of this layer, this section will be dedicated to impurity content and quality control of the highly (100) phosphorous-doped diamond epi-layer. For this purpose spectroscopy method presented in previous sections will be used and discussions will be held in the concern of lattice strain induced by high phosphorous incorporation.

III.2.1 Cathodoluminescence doping level extraction

Control of the incorporated phosphorous density in the crystal lattice has been performed in two steps. First Secondary Ion Mass Spectroscopy (SIMS) has been done by the epi-layer provider (R.J. Nemanich and F. Koeck), not directly on the provided samples, but on samples coming from the same batch, where total amount of incorporated phosphorous atoms can be extracted. A phosphorous incorporation of 10^{19} cm^{-3} has been observed in the samples analyzed by SIMS, hence assumed in the subsequent sections. Secondly, cathodoluminescence performed at Néel Institute has been used in order to characterize the position of phosphorous impurities in the lattice, especially the density positioned in substitutionnal site P_S which exhibits an ionization energy of 0.58eV.

III.2.1.a Low temperature luminescence spectra

Fig. III.4 shows the sub-band-gap CL spectrum that has been recorded for PS2 sample at cryogenic temperature (4K) and normalized with respect to the free exciton peak intensity (5.27 eV). It has been chosen to only represent spectrum recorded on PS2 sample because the measurements taken on the PS1 sample are very similar, if not almost identical, and therefore do not provide any additional information. The CL recorded spectra can be decomposed in three main parts: multiple impurity region (1.5−2.5 eV), blue A-Band region (2.5−4.5 eV) and excitonic region (5−5.5 eV).

1.5−2.5 eV region

Multiple peaks between 1.5 and 2.5 eV, associated with various potential origins, are commonly reported for diamond. As details of each observable peaks in this region can be tedious and make no contribution to the sample analysis, only the one of interest are reported in this manuscript, but reference can be made to [103] for details of the peaks measured.

Starting from the lowest energy, a noticeable broad band spreading from 1.5 eV to 2.1 eV centered at 1.98 eV is reported. This band has already been observed in phosphorous-doped CVD diamond films [346] and has tentatively been attributed to phosphorous-vacancy complexes. The origin of this CL broad band can potentially be explained by the spin-polarized ab-initio calculations conducted by Jones et al. [347] These calculations suggest that phosphorus-vacancy (PV) complexes in diamond function as deep acceptors, with an energy level located approximately 2.8 eV above the valence band. Consequently, donor-acceptor recombination can take place at pairs of substitutional phosphorous and PV complexes, resulting in emission similar to that observed in blue A-Band.

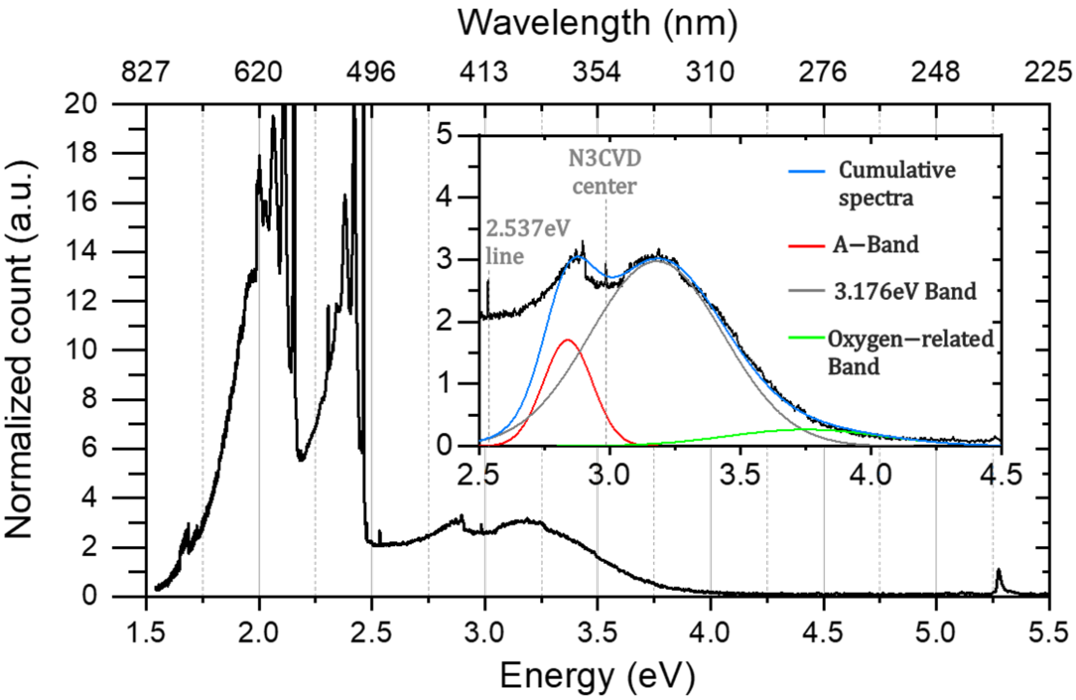

Figure III.4: Cathodoluminescence spectrum recorded at 4K on the (100) highly phosphorous-doped diamond epi-layer of sample PS2. A focus on the A-Band related defect ($\approx 2.5 - 4.5$ eV) is made on the inset where deconvolution of the spectrum has been enlightened by the use of commonly referenced peaks [103].

The red band, affiliated with an intrinsic vacancy-related defect is strongly marked by the presence of the sharp peak at 2.146 eV. However the part of the spectra where this peak is located (1.7−2.2 eV), surprisingly exhibits line-shape pretty close of pink luminescence spectra observed for diamond grown by combustion flame method [348]. This could be correlated with a high intrinsic defect proportion in the highly phosphorous-doped layer as commonly observed with the latter growth-technique.

Concerning the broad band between 2.2 and 2.5 eV, paired with multiple well defined peaks in this range, two main contributions, the green band and the H3 center could be confidently evidenced. The green band, enlightened by its A and B-component peaking at 2.34 eV and 2.39 eV respectively, is often produced in CVD diamond films by H-plasma treatment. Although, oxidation in acids and subsequent annealing could make this peak disappear. As both have been performed on the sample prior to CL measurement, non-diamond carbon phases [349] is the most likely to be responsible for the Green Band observation. Secondly, H3 center is defined through the three-splitted peaks at 2.42, 2.46 and 2.53 eV. The H3 center is preferentially formed in the (100) growth sectors and can be induced by strong mechanical deformations, next to dislocation lines as example.

Importantly, the spectra presented in this section were acquired at the edge of the sample as well as at the end of the manufacturing process (after step oxygen termination in fig. II.1). Furthermore, a silver paint deposit was applied to overcome the disruptive SEM-induced charging effects observed at the centre of the sample. This could imply a potential inter-contamination of the different layers measured as well as potential inclusion of defects induced by the different manufacturing stages. In addition, the main emission peaks reported could be described without including the presence of nitrogen defects, although it is important to note that the line-shape of recorded spectra is surprisingly close to the one reported par Gippius et al. [350] characterizing nitrogen ion implantation.

2.5−4.5 eV region

CL spectrum recorded in this region is presented in the inset of fig. III.4 as well as the convoluted spectra used to fit the experimental data. First, the blue band-A, well known as a feature of extended defects such as dislocations, is observed through broad band centered at 2.88 eV and a fitted FWHM of 0.24 eV. Band-A emission has been correlated to sp^2 defects in diamond structures at incoherent grain boundaries, in the case of poly-crystalline diamond, and/or dislocations. As data have been normalized by FE^{TO} peak intensity, A-band emissions are almost twice higher meaning that amount of dislocations present in the layer are far from being negligible.

The second broad band observed is centered at 3.176 eV with a FWHM of 0.6 eV. Unfortunately, no satisfactory correspondence has been found in the literature for the emission from this band. ND1 centers can potentially be the main responsible for this peak but as it is linked with charged single vacancy, multiple annealing performed on the sample should have removed their CL signature.

Finally, a very broad band of FWHM 0.7 eV and centered at 3.75 eV is observed. As commonly reported for CVD diamond, this band is believed to appear due to oxygen diffusion. This oxygen diffusion could be enhanced by oxygen-cleaning RIE process, during three-acid cleaning that has been performed along the fabrication process, during oxygen termination, or directly during growth where oxygen is added to the gaseous mixture while epi-layer growth. Since extended defects are observable through others CL peaks, one can assume that oxygen could preferentially be included among these defects.

5−5.5 eV excitonic region

Excitonic spectra shown in Fig. III.5 were recorded between 4 K and 102 K in order to extract substitutionnal phosphorus concentration through equation II.17. The recorded spectra have been normalized in respect to FE^{TO} peak emission, that has been clearly observed along the whole temperature range.

Unfortunately, no clear evidence of substitutionnal phosphorus incorporation could be evidenced through excitonic spectra analysis as no $BE-$phonon interaction have been observed. Both BE^{TO} and BE^{TA} are non-existent in the experimental data, meaning that no reliable comparison between excitonic emission could be done to extract doping level from this spectral range. Surprisingly, BE^{NP} peaks is observed and its intensity is growing as function of the temperature increase such as FE peak is broadening. Subsequently, the first hypotheses that could be drawn implies phosphorous which have been incorporated in the layer but its placing in substitutionnal site is below the CL detection limit of 2×10^{15} cm^{-3} according to [298]. Furthermore, as witnessed by BE^{NP} presence, the phosphorous observed in this case should be strongly localized as this emission does not involve momentum-bringer phonon.

The second hypothesis, more probable, could stems from the shortened life time of phonons in the measured samples. Diamond is well renown for its exceptional thermal conductivity due to the high speed at which phonons can travel through its lattice. The latter being attributed to the strong covalent bonds between carbon atoms in the diamond face centered cubic structure. These bonds lead to a relatively long phonon lifetime in diamond, in the range of 10 ps according to the density functional theory calculation initiated by Debernardi et al. [351], assumed to be limited by the spontaneous decay of an optical phonon into two acoustic phonons. However, a study conducted 15 later by Lee et al. [352] on different natural and synthetic (CVD and HPHT) diamonds, testified of the strong correlation between anharmonic decay of phonon lifetimes related to impurities, punctual or extended defects, crystal boundaries, and stress gradients [353]. Especially, characterizations done on thick Ib substrate proved that high nitrogen content can have a detrimental effect on the phonon lifetime but still a lower impact than dislocation density. In the case of PS2, it could be assumed that phosphorus behave the same way as

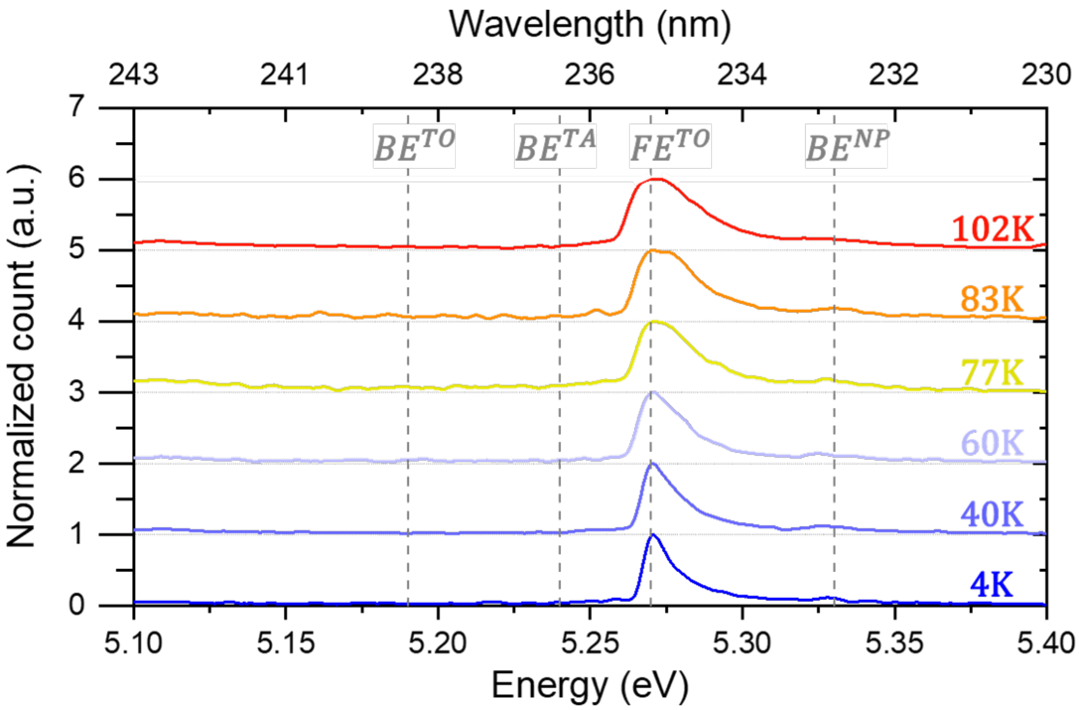

Figure III.5: CL spectrum centered in excitonic region at different temperature, recorded on the (100) highly phosphorous-doped diamond epi-layer of sample PS2. Each spectrum have been normalized in respect to FE^{TO} peak emission and have been shifted for representation purpose.

nitrogen contents, coupled to the highly strained layer, resulting in a too small optical phonon lifetime. Ultimately, the coupling between bound-exciton and phonon could be too short to be observed, which in turns disrupt any conclusion about phosphorous content of the layer.

III.2.1.b Summary

Sub-band-gap CL spectrum have been performed at different cryogenic temperature on the (100) highly phosphorous-doped layer as grown on PS1 and PS2 samples. Unfortunately, no clear evidence of substitutionnal phosphorus incorporation could be given through excitonic spectra analysis or, at least stating on a density below $2 \times 10^{15}\ cm^{-3}$. Alternatively multiple band involving acceptor-donor recombination are observed where phosphorous in different complexes, like PV, potentially exhibit compensating acceptor behavior. Punctual species like oxygen and hydrogen incorporation, common regarding to CVD diamond epi-layer growth, have also been extrapolated. The latter, probably enhanced by a high density of extended defects that have also been characterized through the multiple coloured band. Values of the emission peaks characterizing theses defects also reveal that the phosphorous-doped layer is highly strained. It is important to notice that the spectra were recorded at the edge of the sample as well as at the end of the manufacturing process, implying potential inter-contamination of the different layers measured as well as potential inclusion of defects induced by the different manufacturing processes.

III.2.2 Strain discussion

The size of phosphorus atomic nucleus, being 1.5 times larger than carbon, results in the occupation of a larger volume on the diamond's Bravais lattice, approximately 3.375 times more. This steric effect is further evidenced by the longer covalent bond length of phosphorus, around 1.1 Å, compared to the 0.74 Å for carbon atoms in diamond. Consequently, strong orientational incorporation dependence such as high strain is a common feature of high phosphorous content epi-layer. Even trace amounts of phosphorus atoms introduced during the CVD growth process, mainly governed by highly sensitive surface reactions involving atomic hydrogen and carbonaceous species, can profoundly influence the morphology and crystalline quality of the resulting diamond films. This effect is particularly pronounced in (100)-oriented growth, where phosphorus incorporation is exceptionally challenging compared to (111) doping, with an incorporation efficiency two orders of magnitude lower [123]. The difficulty in phosphorus incorporation on (001)-oriented surfaces is theoretically explained by first-principles calculations, which indicate that the formation energy of phosphorus atoms on the diamond surface is significantly lower than in the bulk [354]. This suggests a tendency for phosphorus to segregate on the diamond surface during growth. Subsequently, to mitigate excessive sub-surface phosphorus doping, the incorporation of phosphorus was reduced in the final few hundred nano-meters of the growth, leading to a linearly decreasing doping profile.

Many studies have been historically conducted to characterize and thus lower as much as possible strain in these epi-layers. Previously discussed CL spectra, demonstrated that the phosphorus-doped layer used for PS1 and PS2 are not spared from high extended defect density, additionally observed through delamination of the fabricated sample PS2 as shown on fig. III.6.

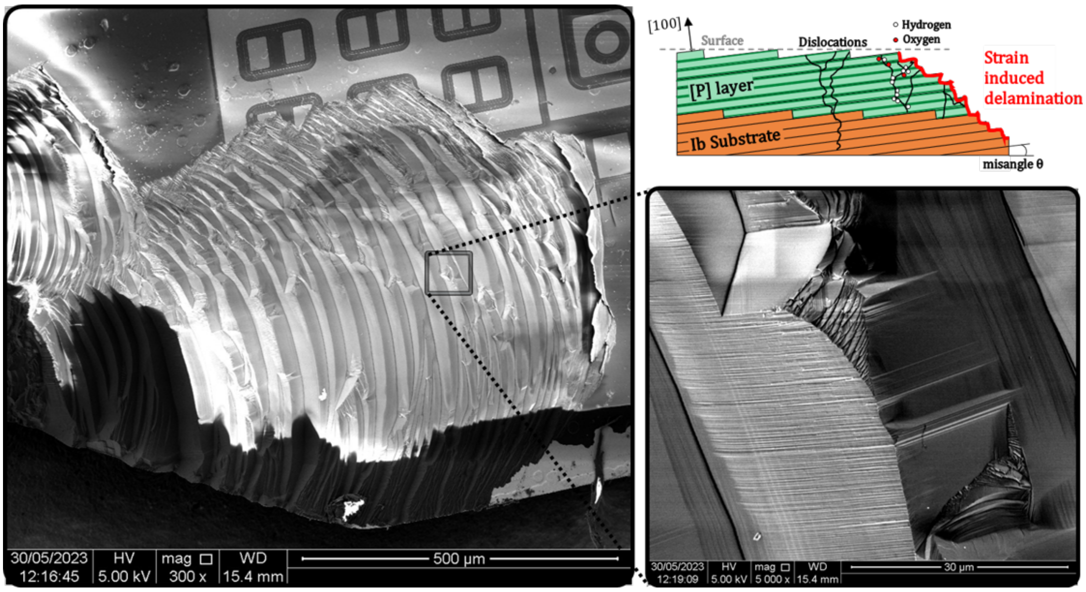

Figure III.6: SEM images of PS2 sample's corner-cut which exhibit wide area of delamination. A schematic cross-sectional view of the stack is also juxtaposed, enlightening dislocations and impurity aggregations that are enhanced around theses dislocations.

In general, for the convenience of electrical characterization, samples are affixed to an alumina plate using conductive silver paint. This provides both a reliable ohmic contact on the backside of the sample and effective electrical insulation for the entire stack in the characterization environment. To remove the samples from the alumina plate, a small rotational force is applied to the substrate, breaking the silver paint dried adhesive. This method has been commonly employed for inter-process sample characterization and is considered gentle on the hardness of diamond. However, during the first application of this method to sample PS2, delamination along the edges unexpectedly occurred. Following fruitful discussions with Professors E. Gheeraert (Institut Néel, Grenoble) and S. Koizumi (NIMS, Tsukuba), pioneers in control of phosphorus incorporation in diamond, it was revealed that such detrimental damages were frequently observed in the early stages of high phosphorus content epi-layers. In some cases, delamination has even been observed without any external forces being applied to the sample. The origin of this disruptive effect has been attributed to the high hydrogen content, which diffuses with temperature and forms aggregated complexes around extended dislocations. These complexes, illustrated in Figure III.6, can be likened to hydrogen bubbles formed during the Smart-cut process. It is worth noting that oxygen has been included in the illustration, as its presence has been detected through CL spectroscopy.

The observed delamination also displays a distinct ”staircase” pattern, where the steps appear to be uniformly oriented. The presence of sharp and well-defined step terraces can be tentatively explained by the CVD growth model proposed by Ohmagari et al. [148], with the assumption that their findings are applicable to phosphorus layers. It is proposed that a misaligned substrate angle during CVD growth promotes lateral nucleation of diamond, resulting in the formation of terrace-like morphologies in the as-grown layer. Additionally, phosphorus and potentially other impurity defects are more prone to preferential incorporation at the junctions of these terraces, leading to the formation of phosphorus complexes that differ from substitutional donor states. This phenomenon could explain the absence of their signatures in the CL spectra, as well as strong emission of defects related band. In summary, delamination is attributed to the presence of extended and localized extrinsic defects (aggregated or otherwise), which introduce strain into the sample and potentially reveal anisotropic terracing growth at the edges of the sample.

III.3 Lightly boron doped diamond epi-layer

The doping level of boron in the p-channel is a crucial parameter that significantly affects the on-resistance, blocking voltage, and threshold voltage of the fabricated transistors. To gain a deeper understanding of the boron concentration, spectroscopic information were obtained through CL measurements performed on each fabricated sample. These measurements will provide valuable insights into the defect signatures, complementing the electrical characteristics discussed later. Building upon the characterization of defects in the phosphorus-content layer presented in the previous section, a study was conducted to correlate and compare the defect signatures in both layers. This analysis allowed for further validation of previous hypotheses and investigation of defect propagation mechanisms.

III.3.1 Growth and mesa-etching

The p-layer of the four samples presented along this manuscript were grown by Diamfab company. After the growth process, there was no significant surface roughness change, with a range of approximately 10 nm observed for all four fabricated samples. Fig. III.7, using sample NS3 as an example, shows optical profilometer images that confirm this observation. It is worth noting that the averaged surface roughness R_a is relatively high compared to the atomically-flat surfaces achievable in diamond [145, 355]. The high surface roughness observed along all three stages is primarily induced during the substrate polishing phase. Diamond is well-known for its extreme hardness, which leads to residual parallel scratches on the surface caused by mechanical polishing, as this critical process is arduous. These scratches are clearly observable and propagate through each layers grown where they are main contributor to the high surface roughness. Consequently, the line-scanned surface roughness is higher in directions perpendicular to the main orientation of the scratches compared to the parallel orientations. This anisotropic nature is reflected in the higher R_a value reported for large surface scans.

Concerning punctual surface defect and volumic defect that extended all the way to the surface, identified as hillocks and crystallites, their number seemed to not have been increased through the p-channel growth and its etching. At least, no satisfactory correlation could be made at this stage to extract a correct yield from each sample. Their distribution being not homogeneous and varying a lot from one sample to another, no relevant statistics have been made. However, measurements presented in fig. III.7 have been recorded at the center of the sample NS3, but defect density increases sharply as the distance from edges of the sample

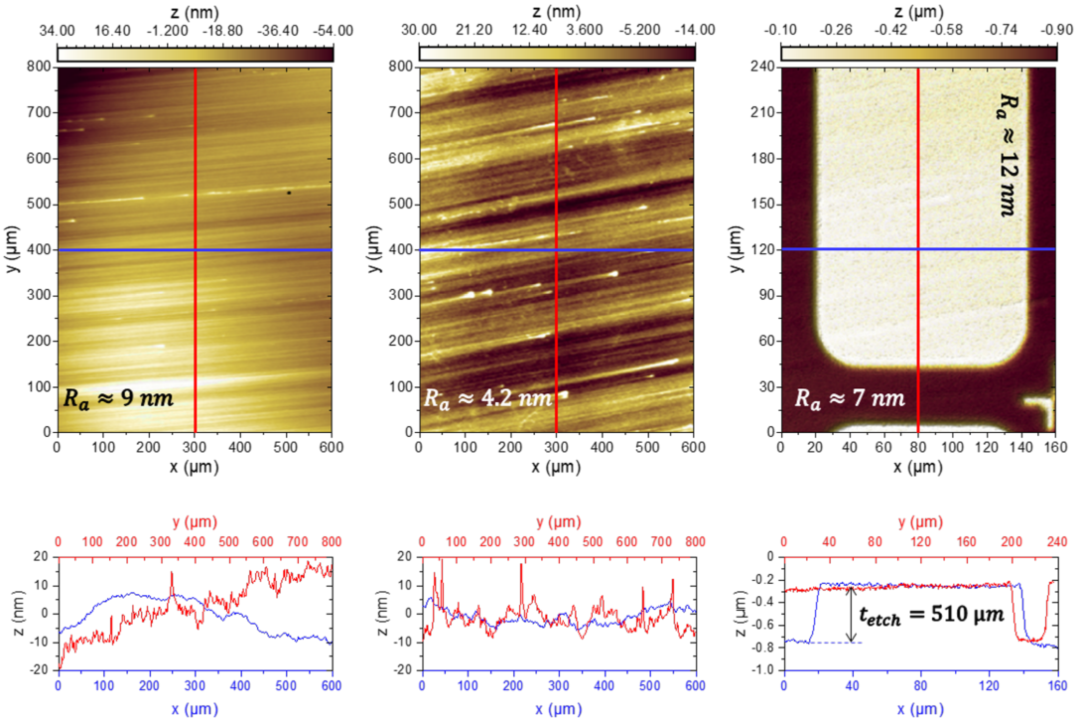

Figure III.7: Optical profilometer images of sample NS3 surface from left to right, before p-layer growth, after this growth and after its RIE etching. Scan line referenced in blue (along x axis) and red (y axis) are plotted at the bottom to enlighten polishing impact and etched depth.

decreased, especially for PS1 and PS2.

One can remark that non negligible averaged surface roughness and high volumic and surfacic defect density can lead to increase scattering of charge carriers, resulting in higher resistive losses and thus reduced JFET on-state performance. Furthermore, it can introduce additional defect states at the pn junction interface, leading to increased leakage current, also the hindered uniformity of the junction can result in uneven distribution of electric field and potential barriers, affecting each JFET electrostatical control, performances and reliability. While dislocation and impurity are potential killer-defects and have the power to seriously impede JFET electrical performances, surface roughness can further influence significantly the Fermi level position of the p-channel on the front-side interface. Particularly, a pinning effect [356] is more likely to arise in rough surface, thus creating an uncontrolled depletion layer, hindering the ON-state conductivity of the fabricated JFET. However, due to the limited number of processed samples and the variability of the results, no definitive conclusions could be drawn regarding the specific impact of surface roughness on JFET electrical characteristics. Although oxide encapsulation has been tested on PS1 and NS3 samples in order to fix the Fermi level pining from the front-side, no improvement of the conductivity of these sample could have been observed.

III.3.2 Cathodoluminescence measurement

In order to isolate and estimate punctual and volumic defects or p-layer doping level, 4 K sub-band-gap CL spectra have been recorded on each fabricated samples at various positions (fig. III.8). Similarly to the study previously conducted on the phosphorous-doped epi-layer, only the main interesting band-emissions features are discussed here. Additionally, the spectra presented in this section were also acquired at the end of the manufacturing process adding the same potential layer inter-contamination as well as inclusion of defects induced by the different manufacturing stages.

Firstly, the measured spectra reveal that the green band and H3 center are more pronounced

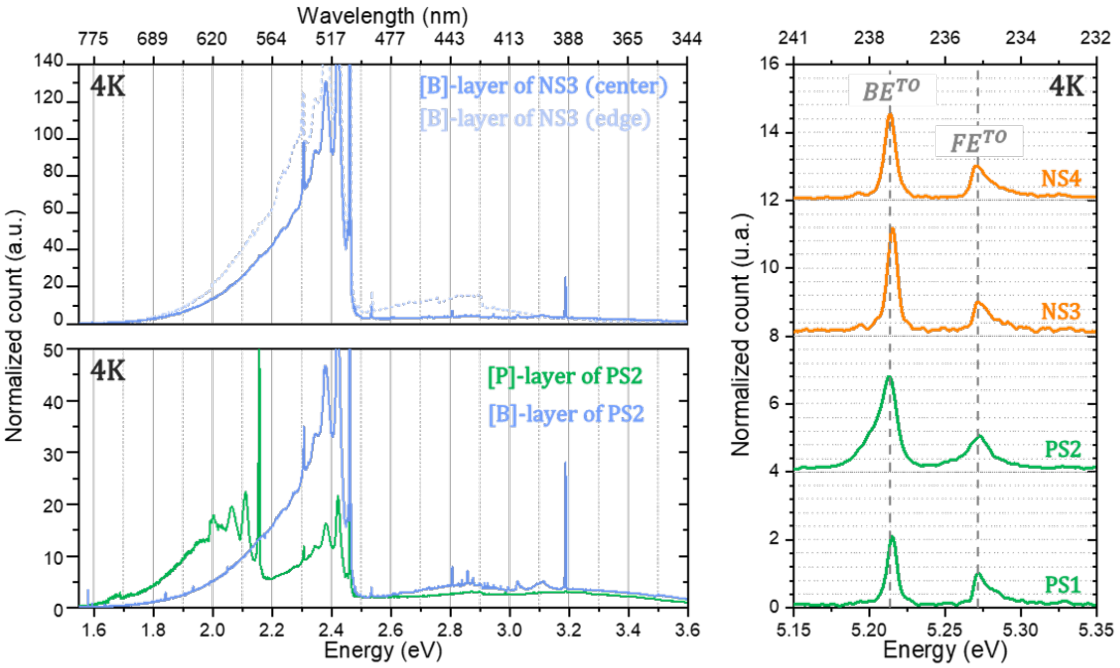

Figure III.8: 4K cathodoluminescence spectrum recorded on the boron-doped layer of each sample. Spectra recorded on top left figure compare defects band-emissions between the center and the edge of sample NS3. At bottom left a comparison is made between spectra obtained on the phosphorous-doped layer and the boron doped layer of the same sample, PS2. Excitonic-emission region recorded at the center of each samples is presented on the right figure.

in boron-doped diamond samples compared to phosphorus-doped layers. The intensity of the green band, indicating hydrogen presence, is higher in NS3 and NS4 samples than in PS1 and PS2. Although quantitative density cannot be determined from these results, it is hypothesized that both epi-layers have a high hydrogen content, with a tendency to form impurity-related complexes in the phosphorus-doped layer. The absence of the 1.98 eV band in the boron-doped layer, which was prominent in the phosphorus layer of sample PS2, further supports this hypothesis. In summary, while high hydrogen incorporation is observed in both layers, it manifests differently with the formation of singular defects in the boron-doped layer and phosphorus-vacancy complexes in the phosphorus-doped layer. Additionally, as the measurement has been performed at 5 kV e-beam accelerating voltage, hence a maximum scanned depth of 300 nm, near-surface defect composition is potentially highly accounted in the recorded spectra. Tentatively, the difference of hydrogen positioning in the two layer studied could be a witness of the Fermi level positioning near the front-side interface. Different Fermi level pining is expected to allow for different defect CL signature, even if these defect have the same position in the band-gap.

In the case of the H3 center, characterized by the three-splitted peaks at 2.42, 2.46 and 2.53 eV, more than way higher peaks intensity, the associated broad band is also widened, especially for samples NS3 and NS4 using nitrogen as gate layer. The presence of this peak in phosphorous-doped layer of PS2 sample was attributed to strong mechanical deformations next to dislocation lines, but this hypothesis was made by neglecting nitrogen presence. In the case of the p-layer H3 center is almost always juxtaposed with N3 center [103], the latter being related to A- and B-aggregates of nitrogen. Another justification for the presence of a stronger H3 center presence in p-layers could thus arise from nitrogen content that are aggregated with or without vacancy, and thus possibly form compensating defects. This hypothesis is further supported by the presence of multiple peaks related to nitrogen content in general (peaks between 3 and

3.4 eV for example). A proper quantification of these defect density is hard to realize on the basis of CL spectra alone, but could be of importance regarding to their potential major impact on devices performances. Further photo-luminescence (PL) or Raman spectroscopy would be required to status on the ammount of nitrogen A- and B-aggregates.

Secondly, the intensity of the blue band-A emission was found to be stronger in each p-layer growth performed on the four samples, compared to phosphorus-doped layer. While it was already pronounced in the latter, its recorded intensity was twice as prominent in the boron-doped layer of sample PS2. This suggests that most of the dislocations originating from the phosphorus-doped layer propagated through the p-layer, combined with additional dislocations introduced during the p-growth process. Furthermore, the band-A emission significantly increases with distance from the center of the sample, consistent with optical profilometry measurements that suggested lower crystalline quality at the sample edges. This observation also supports the relationship between the H3 center and the green band defect, as their respective spectral resolutions and band emissions exhibit the same behavior as mentioned above.

In contrast to the PS2 phosphorus-doped layer, a clear emission from BE^{TO} peak could be recorded, hence substitutionnal boron concentrations have been extracted using equation II.16. Dispersion has thus been measured by CL recorded at different locations of the samples. However, this study has been limited by SEM-induced charging effect that hindered measurement upon a wide area of the device. It should be noticed that surprisingly this disturbing charging effect which cause loosing of CL signals, was only observed on PS1 and PS2 samples, but no more explanation other than layer quality could be proved. However, considering that charging effect arise mainly in insulating material, where charges are accumulated in a confined region and can not be evacuated, it can be thought that the scanned area where charging effect occur are insulating. The latter strongly involves either an undoped or a fully compensated area. Nonetheless, at least 3 points in the worst case and 5 points normally, taken at each samples corners and centers, could have been characterized and measurements have been compiled in fig. III.9. Doping levels ranging between $4.16 \times 10^{16}\ cm^{-3}$ and $1.01 \times 10^{17}\ cm^{-3}$ have been obtained with an average value for all the samples of $6.75 \times 10^{16}\ cm^{-3}$. Not far from the targeted $2 \times 10^{17}\ cm^{-3}$ growth value, CL measured substitutionnal boron concentration is only 33% of the target, representing a doping error of almost -200%. As reference, GD-030 averaged doping levels of $2.4 \times 10^{17}\ cm^{-3}$ have been extrapolated from (C-V) Mott-Schottky measurements [58], corresponding to a doping error of +140% from the $1 \times 10^{17}\ cm^{-3}$ targeted during growth. Noticeably, the growth parameters of the four fabricated samples as presented in this work, were the same that the one used for GD-030 p-layer growth.

III.3.3 Summary

Phase-shift optical interferometry and sub-band-gap CL spectroscopy have been performed on boron-doped epi-layers of the four fabricated samples. Averaged substitutionnal boron acceptor incorporations on samples batch of $6.75 \times 10^{16}\ cm^{-3}$ have been reported with a consequent deviation from targeted $2 \times 10^{17}\ cm^{-3}$ value. Oppositely to doping levels reported in the reference sample GD-030, previously fabricated using the same growth conditions, doping levels measured in this work are almost 3 times lower than the target. Stronger density of compensating defect, donor like nitrogen complexes, can be reasonably considered for this divergence as their acceptor-donor recombination signature emissions could be correlated to CL spectra. The latter also comforts the electrical measurements reported in section III.5.3 where an high compensation can be involved.

Comparison between spectra measured on phosphorous-doped layers and boron-doped layers validates the main hypothesis previously done concerning defects presence, and so on propagation, in both layers. The latter has also been supported by optical phase-shift interferometry, exhibiting non negligible averaged surface roughness of ≈ 10 nm and displaying punctual surface defects identified as hillocks or crystallites which could arise from volumic extended defect that

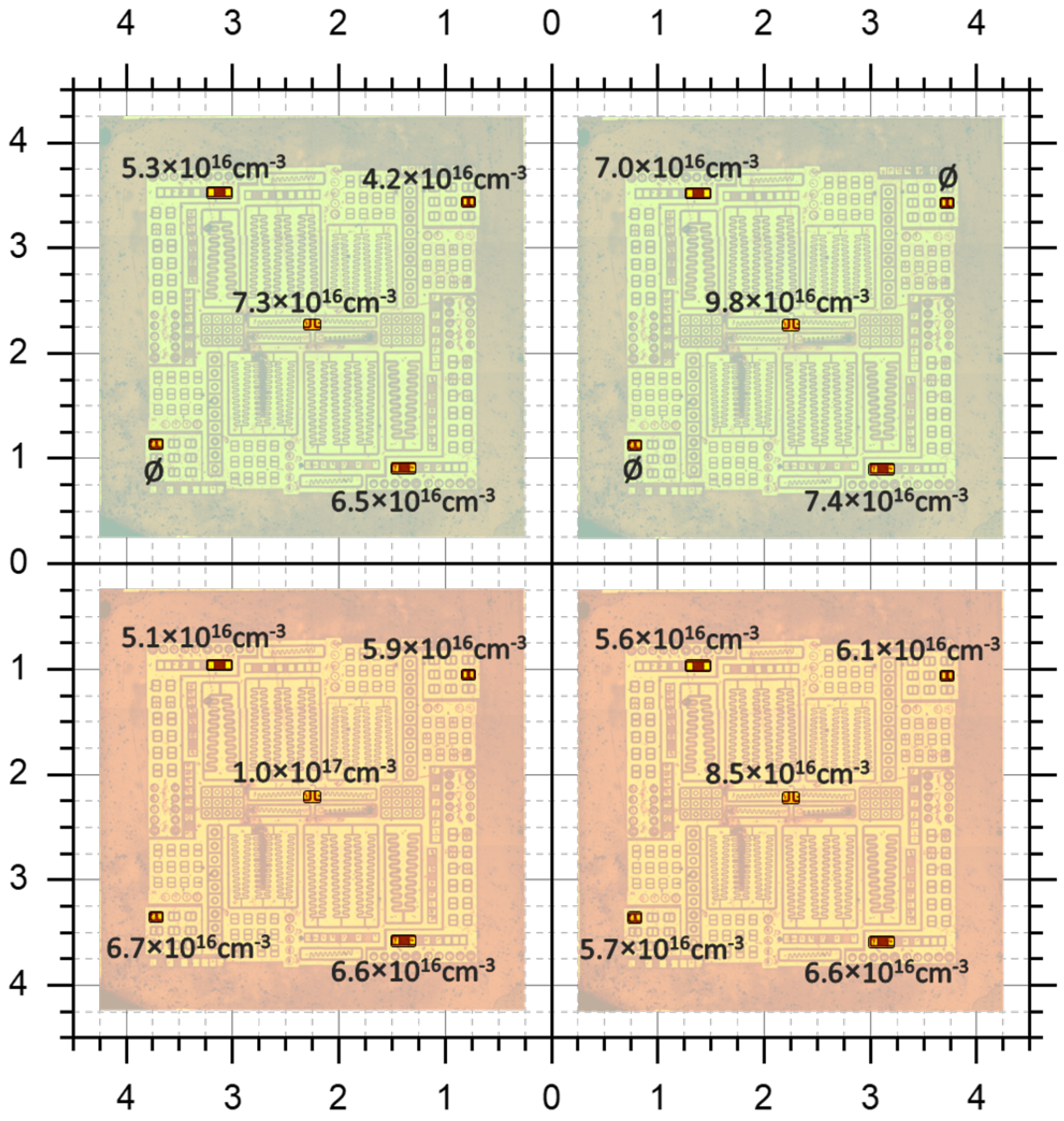

Figure III.9: Extracted substitutionnal boron concentration from the BE^{TO}/FE^{TO} peak ratio intensity according to equation II.16, at different enlightened location, on each of the four fabricated samples (top left PS1 and right PS2; bottom left NS3 and right NS4). ∅ symbol has been used to specify absence of measurement due to SEM-induced charging effect that caused loss of CL signals.

propagate to the surface. It should be noticed that both doping levels and defects density extrapolated are non-homogeneous and vary a lot as function of distances with the samples center. Higher defect density coupled with lower substitutionnal boron concentration are reported near the samples edges. Considering the spherical shape of the plasma used during CVD growth, a higher average substitutional boron concentration of 8.94×10^{16} cm^{-3} was observed at the center of the sample, compared to an average of 6.07×10^{16} cm^{-3} within a circle with a radius between 1.5 and 2 mm centered at the sample's center. This trend was also observed in the reference sample GD-030 [58], potentially indicating a preferential formation of boron complexes near the edges of the sample or simply a lower incorporation efficiency at sample's edges. It needs to be precised that in these cases, compensation ratio can be recorded higher at the edges of the samples because boron incorporation is lower in this area. Consequently, on the hypothesis of a constant compensating donor incorporation, the ratio $k = N_D/N_A$ can be increased on the outer part of the sample.

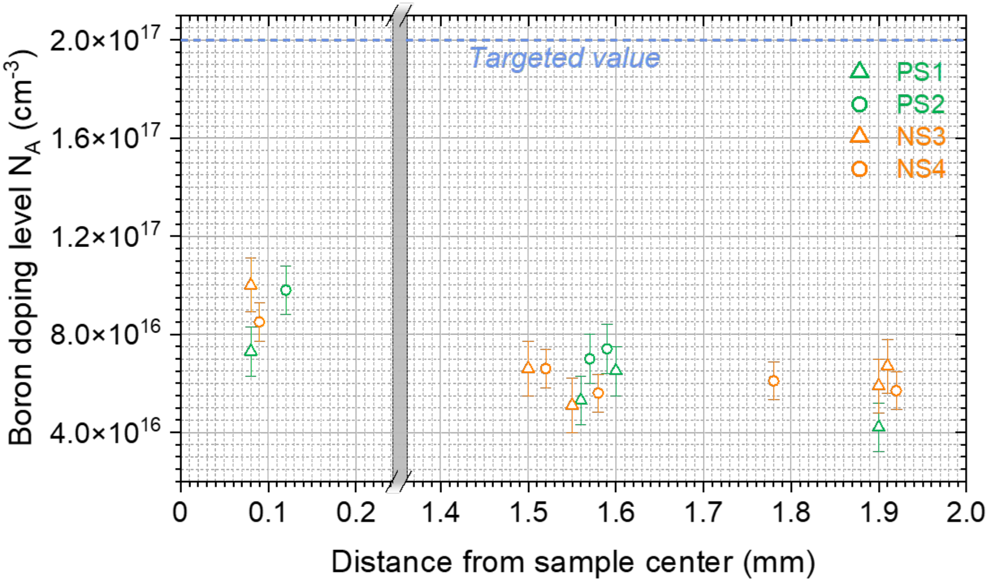

Figure III.10: Boron doping density extracted from the BE^{TO}/FE^{TO} peak ratio intensity of 4 K cathodoluminescence, as function of distance to the center for the four fabricated sample.

III.4 Process finalization: Drain, Source and gate contact fabrication

III.4.1 Selective heavily boron-doped layer growth

Introducing a 200 nm thick heavily boron-doped ($N_A \approx 10^{21}$ cm^{-3} targeted) layer was accomplished through selective MPCVD growth, thanks to the use of a 300 nm thick titanium mask. The lithographic mask was applied using Heidelberg DWL66FS laser lithography, followed by the electron beam evaporation of titanium. An optimal metal choice due to its strong adherence to diamond and its robustness under demanding growth conditions. After the growth process, the titanium mask was eliminated using an aqua regia solution (HNO_3 + HCl; 1:3), followed by a boiling tri-acid (HNO_3 + H_2SO_4 + $HClO_4$; 1:3:4) bath. This ensured the removal of TiC formed on the diamond surface due to the elevated temperature exposure during growth, such as removing non-metallic surface contamination like graphite. It has to be noticed that this cleaning procedure has been used between each fabrication steps in order to maintain the cleanest possible surface all along the different processes.

Upon optical inspection following mask removal (refer to fig. III.11), it appeared that a reasonably consistent p++ layer thickness of approximately 230 nm has been achieved, displaying minimal variance across different samples. The slight 15% deviation from the target value is deemed inconsequential, as it has negligible impact on JFET characteristics compared to the p-channel which is significantly more weighing on the specific ON-resistance and threshold voltage. Considering the planar resolution, the use of a thick Ti mask limits the achievable resolution in this manufacturing process to around a micrometer, despite optimized resist/laser exposure coordination. Consequently, all components with a Drain-Source width $L_{SD} \geq 5$ μm were successfully manufactured, whereas the yield was less consistent for inter-digited JFETs with $L_{SD} = 2$ μm. Given that this spacing approaches the lithographic resolution limit, the JFETs were strategically designed at the center of the sample, where resist deposition is anticipated to be more uniform. To validate this, two inter-digited transistors (with $L_{SD} = 2$ μm) were intentionally placed at the edges of the lithography mask, approximately 450 μm from the sample's edge. Out of the 24 transistors of this type fabricated, only 14, or nearly 60%, where fabricated as intended. Notably, among the edge-placed transistors with $L_{SD} = 2$ μm, only NS4

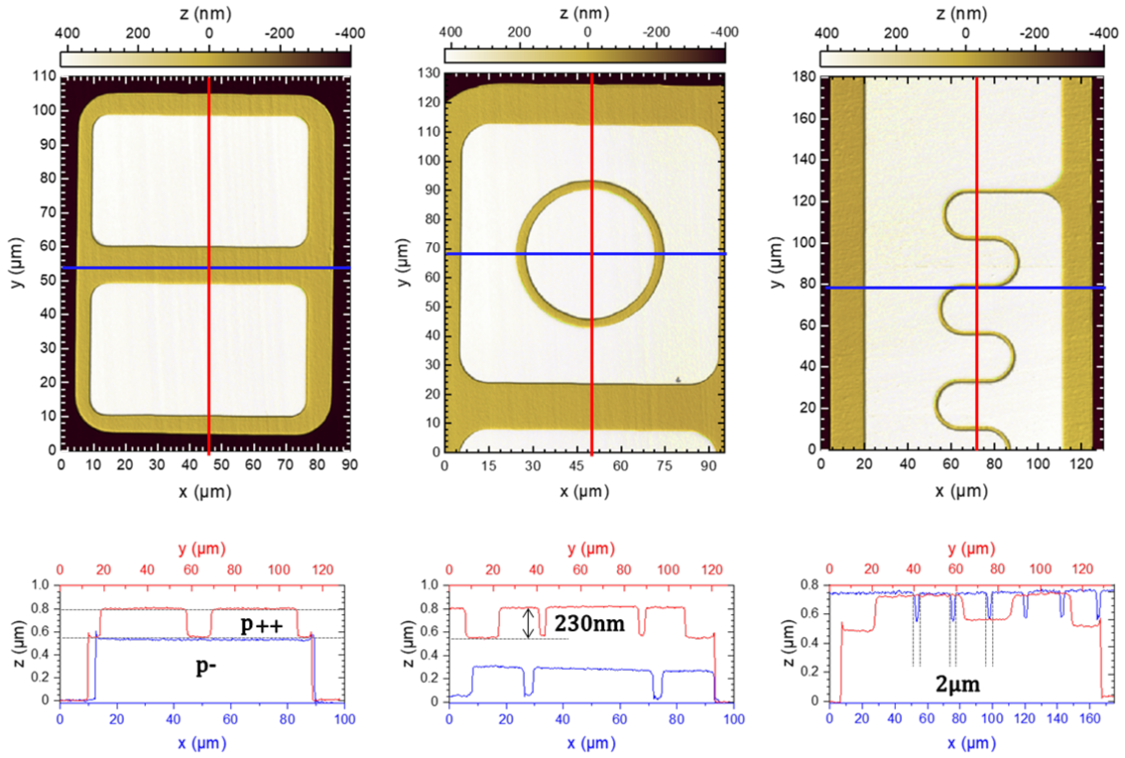

Figure III.11: Optical profilometry images taken after selective growth metallic mask removal of, from left to right: rectangular-shaped JFET with 10 µm drain to source spacing, circular-shaped JFET with 5 µm drain to source spacing and inter-digited JFET with the lowest spacing achieved on the samples batch of 2 µm between source and drain electrodes. Scan line referenced in blue (along x axis) and red (y axis) are plotted at the bottom to enlighten the stacked layers thicknesses.

achieved the desired resolution, while in the case of sample PS2, this spacing could not even been reached on 2 transistors center-placed (fig. III.12). The later attributed to growth under the mask or its outright removing, during MPCVD selective growth preceded by H_2 plasma.

Although the selective growth process approached its limits in terms of homogeneity, devices that allowed for greater scaling tolerance were successfully manufactured with a yield exceeding 90%. Notably, it was observed that unresolved or ill-defined devices were concentrated in regions exhibiting higher surface defect densities, as illustrated in fig. III.12. Among the surface defects commonly reported in literature [114, 357], un-epitaxial crystallites, flat-topped hillocks, and pyramidal hillocks were identified on the fabricated samples. While the distribution of these defects is not uniform and varies significantly among different samples, they are consistently present in varying quantities and have a tendency to cluster around the sample edges. Hillock-type defects were found to stem from extended crystallographic imperfections like clusters of dislocations formed at the interface or propagating across it. Conversely, un-epitaxial crystallites were discovered to be embedded within the CVD layers without any direct association with extended defects or underlying imperfections [357]. Although conventional methods cannot eliminate hillock defects, un-epitaxial crystallites can be effectively removed through hydrogen or oxygen plasma treatments (RIE).

The decision was made to abstain from subjecting the fabricated samples to oxygen-cleaning via reactive ion etching (RIE) after the selective growth process. This choice was based on the potential impact such cleaning could have had on the surface smoothing of the p++ layer, potentially counteracting efforts to reduce un-epitaxial crystallite density. However, this cleaning procedure was indeed employed after each resist development step to prevent excessive resist deposition in non-exposed areas, ensuring the smoothness and cleanliness of the uncovered layers. Additionally, for the preparation of metal/n-diamond contacts, as stated in section (II.5.2.b),

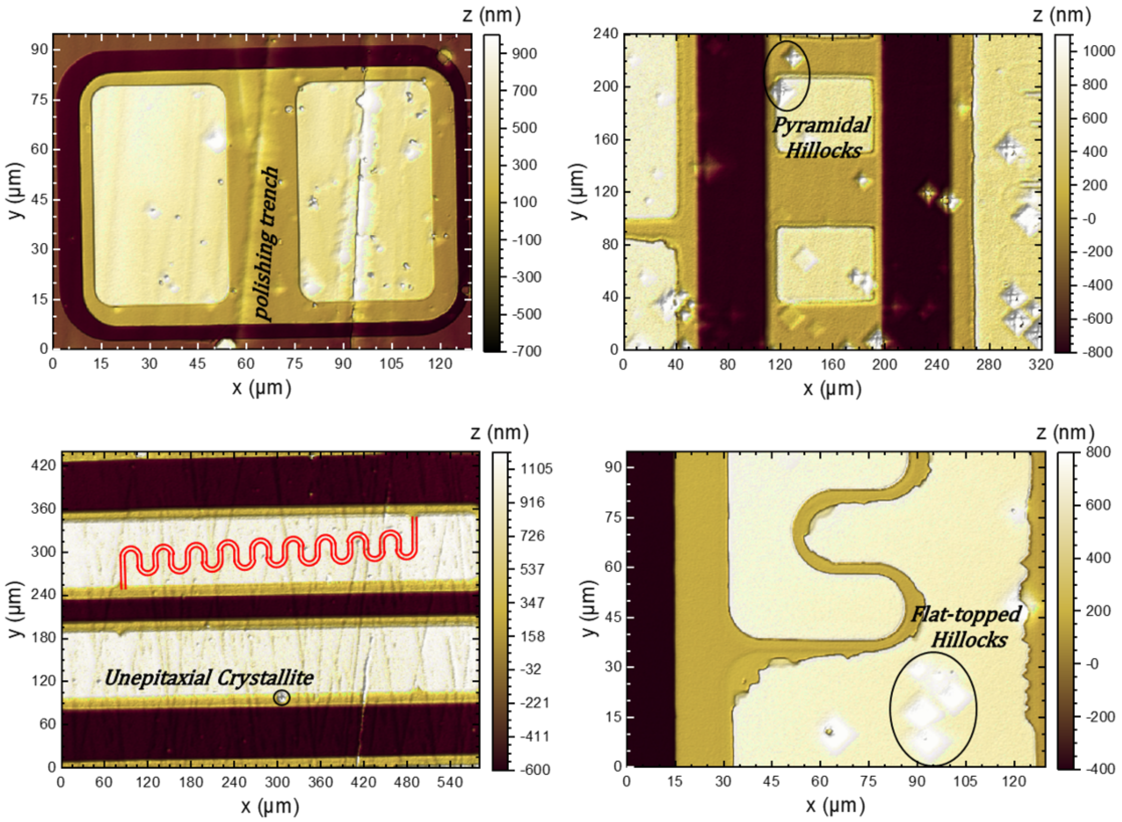

Figure III.12: Optical profilometry image of: (Top left) PS2 sample rectangular shaped JFET exhibiting large and deep polishing trench; (Top right) PS1 sample linear TLM bar with dense amount of pyramidal and flat-topped hillocks; (Bottom left) PS2 sample enlightening un-resolved 2 µm spaced inter-digited JFET; (Bottom right) PS1 sample 2 µm spaced inter-digited JFET with poor edge resolution and flat-topped hillocks.

surface termination is a key parameter. In this sense, exposure to an oxygen plasma just before evaporation of the future metal contacts (all in a clean room controlled atmosphere), ensures better surface coverage with oxygen and thus better control of Fermi level pinning at the interface.

It is anticipated that defects observed here would adversely affect JFET performance, a conclusion previously illuminated in the context of Schottky diodes [358]. Nevertheless, due to the limited number of functional samples and the substantial variability in results, no definitive conclusions could be drawn regarding the potential negative impact of such defects on the electrical characteristics of the JFETs. In spite of these concerns, it is worth noting that the overall defect density observed on the four fabricated samples remained relatively low. Moreover, the growth process exhibited a higher level of reproducibility compared to previously manufactured batches of samples, especially that comprising the reference sample GD-030 [58].

III.4.2 Contact metal deposition

Last stage of fabrication rely on contacts fabrication that has been deposited by laser lithography followed by metal evaporation. The metallic stack is made up of titanium (30 nm), platinum (20 nm) and gold (160 nm), and the deposition is identical for all the electrodes, source, drain and gate carried out at the same time.

It is important to emphasize that, even though electrodes deposition occurs simultaneously for drain, source and gate, compared to MOSFET or MESFET with separated metal deposition [58, 59], this step needs to be repeated at least five times (depending on the specific sample) to achieve satisfactory lift-off and alignment results. The design intentionally incorporates a low misalignment tolerance at its foundation, aiming to optimize component density on the same sample. To maximize the contact area of the gate electrodes on the front face, these were designed as monolithic blocks extending across the entire active fabrication surface, with a deviation of 5 μm from the p-mesa. Similarly, for the source and drain electrodes, a tolerance of 4 μm was chosen with respect to the edges of the p++ layers for the same purpose. Additionally, the wire-bonding of various components necessitated a thicker layer of gold, which in turn required the use of a thicker and more robust resists, hence less easily removable, ultimately increasing the complexity degree of the fabrication process.

While each of these constraints surpasses the previous technological limits achieved within the team, their combination significantly narrows their individual tolerances. Notably, the fabricated samples encountered challenges with the lift-off process, necessitating repeated cleaning, resist re-deposition, and metal evaporation. Despite the absence of reported contamination or surface deterioration resulting from the successive lithography cycles, there exists a potential for negative repercussions. Nonetheless, a notable improvement in lift-off quality was achieved by employing N-Methyl-2-pyrrolidone (NMP) heated to 350K instead of acetone. This seemingly minor optimization featured substantial results, increasing the yield of spatially resolved components after lift-off to over 90%, as witnessed by PS2 sample image in fig. III.13.

Following the metal deposition, the samples underwent annealing at 773K in an ultra-high vacuum environment ($< 10^{-7}$ mBar) for a duration of 30 minutes. This annealing process aimed to promote the formation of TiC at the titanium-diamond interface, enhancing metal adherence and subsequently reducing contact resistances. Notably, it should be observed that the recorded thickness of the metallic stack (≈ 180 nm) was slightly lower than the targeted value (210 nm). This deviation is tentatively attributed to the uneven deposition of gold caused by variations in the pellets within the evaporator crucible.

Regarding the vertical extent of the metallic stack, while its thickness is advantageous for facilitating wire bonding, it presents a counterproductive effect on light collection efficiency. Although transparent contacts [325] or semi-transparent contacts [359] have previously been developed for diamond, they require the utilization of very thin metal layers (< 10 nm). As a potential avenue for future exploration in this regard, the incorporation of a heavily boron-doped layer could allow for the removal of the drain and source contacts. Although this would elevate the series resistance, it holds the potential benefits of achieving enhanced electro-optical control of the devices.

III.4.3 Fabrication conclusion

As expounded upon in these sections, a total of four samples incorporating JFET structures have been successfully fabricated. These JFETs utilize either a thick Ib substrate or a (100)-oriented phosphorus-doped layer as the gate contact. These fabricated samples exhibit the advantage of a streamlined fabrication process encompassing merely three lithography steps: p-channel mesa etching, p++ selective growth, and metallic contact deposition.

The final phase of sample production involves surface oxidation achieved through deep UV ozone plasma treatment. This treatment is crucial in averting any uncontrolled surface terminations that could lead to issues such as surface conduction or the diminishment of p-channel width due to the strong pinning of the Fermi level at the channel's top surface. Employing a Xenon EXCIMER UV lamp emitting at a wavelength of 172 nm, the samples are exposed to oxygen plasma for a duration of 2 hours within a controlled vacuum environment of 500 mbar.

The intricate nature of diamond device fabrication is exacerbated by the absence of standardized processes. Challenges arise from the limited sample size and the imperfect control of certain critical steps, such as defect-free growth and the lift-off procedure. Factors that have strongly impeded the production of larger-sized devices. Nonetheless, through adept design strategies and process stream-lining, our focus has been directed towards producing sizable components within compact areas. This concerted approach has led to an impressive yield of over 90% for suc-

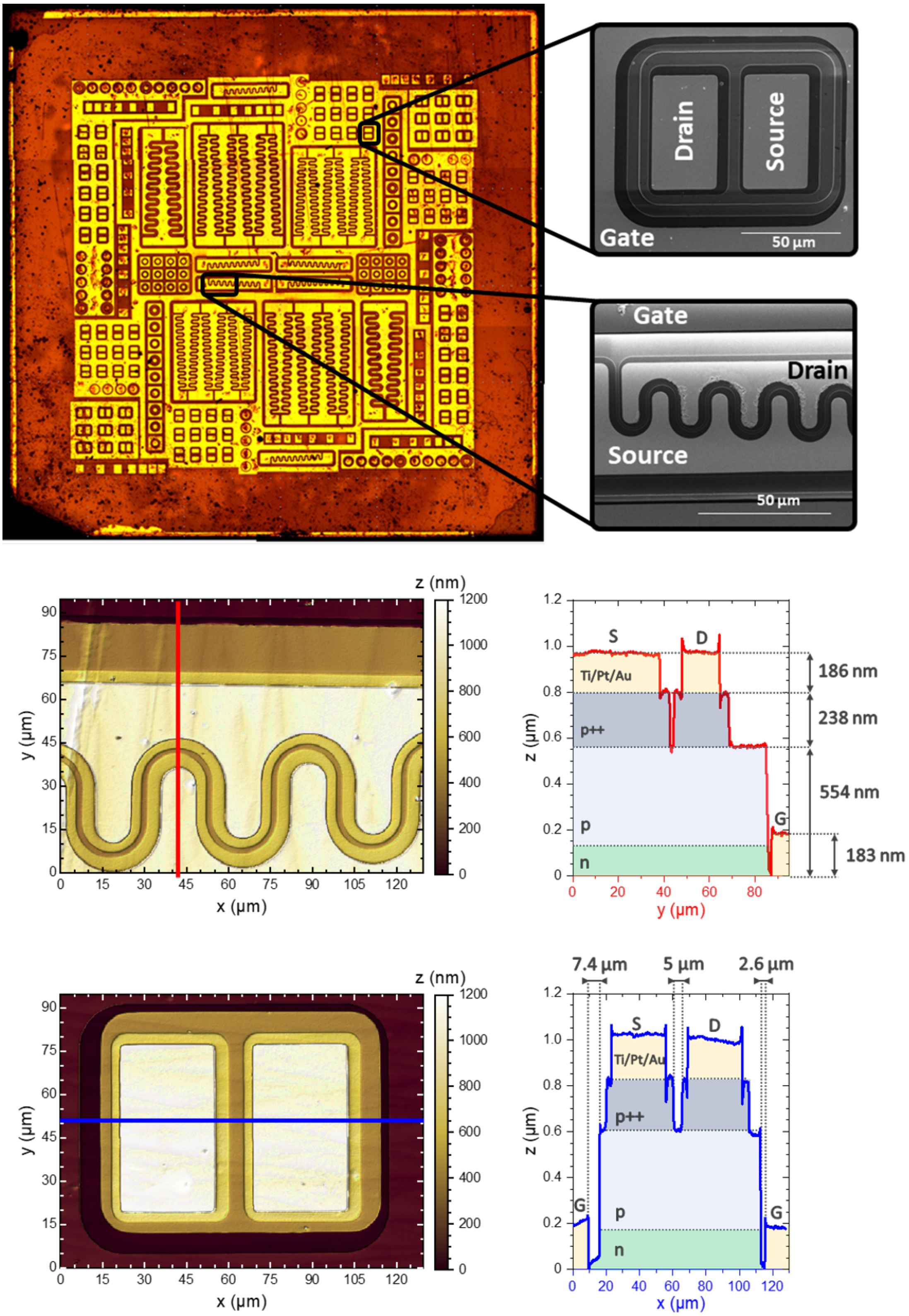

Figure III.13: Optical, SEM and profilometry images of PS2 sample after fabrication steps completions. SEM images focused on 5 µm spaced drain to source rectangular shaped JFET and a 2 µm inter-digited JFET. Optical profilometry images made on the same devices enlighten the measured depth of the layers composing the stack such as lithographic mis-alignment of ±2.4 µm (linear translation). Depth profile have been recolored considering the ideal layer stack targeted.

cessfully resolved devices at the culmination of the fabrication process. Differing from previous endeavors within the team, the fabricated samples feature large-scale inter-digited transistors coexisting with multiple small devices dispersed across the substrate's surface and separated by mesa etching. In a parallel characterization stage, C. Masante [58] reported encountering two defective samples out of the six he processed. These defects stemmed from poor lift-off or selective growth failure, rendering these samples unusable. In stark contrast, the four fabricated samples presented in this manuscript demonstrate a distinct absence of any disruptive fabrication failures at the same developmental stage. Subsequent electrical characterization of these samples has yielded conclusions closely aligned with those drawn in this previous work. Given the potential for challenges to arise at any stage, it's notable that only the PS2 samples have exhibited current transport and p-channel conductance modulation, allowed by the pn junction employed as a gate. Despite this advancement, as expounded upon in section (III.5.3), a lack of insight into the mechanisms leading to the non-functionalization of the other samples persists.

Consequently, from an electrical standpoint, only one fully operational sample (PS2) has emerged out of the four that were processed. This modest success ratio aligns with previous reports utilizing the same facilities, where the fabrication of small-sized diamonds exhibited similar challenges (for instance, one fully functional sample, GD-030, out of 6 fabricated [58]). This underlines the intricate nature of small-scale diamond fabrication. Given the limited availability of substrates and the substantial time investment required (owing to shared equipment availability), a majority of the successful device operations showcased in this manuscript have been conducted on the PS2 sample.

III.5 Boron-doped layers electrical transport characterizations

Considering that the p-channel resistivity, such as the drain and source contact resistances, are JFETs key parameters that define the ON state performances of the fabricated devices, this section is dedicated to the electrical characterization of these of importance parameters. They have been determined using specifically designed TLM structures, presented in Fig. II.14, by measuring the resistance between contacts patterns for varying distances. Placed in the outer corners of the mask designed, the linear geometry used for the p- and p++ type TLM enables statistical characterisation of the resistivity variability (expected in view of the CL results). Additionally, it allows for reproducibility study between the various samples fabricated during this thesis, as well as previous fabricated transistors within the team [59, 224, 244, 245].

Unfortunately, statistical analysis has been really limited over the fabricated samples considering the high malfunctions yield obtained at the early stage of electrical characterizations. Fig. III.14 images this low functional devices yield through current-voltage characteristics comparison between the four fabricated samples. Measurements displayed here, have been done on a TLM bar with selective p++ growth underneath the 25 µm spaced contacts. Only PS2 sample exhibits measurable current (higher than detection limit of 1 pA) at room temperature, without any illumination. Moreover, further measurements on various places of PS1, NS3 and NS4 samples show the same results (not displayed here for their lack of interest), stating on the absence of p-channel conduction under conditions mentioned herein-above.

Given the considerable disparities observed in the electrical measurements conducted on the four fabricated samples, their examination will be broadly divided into two sections. Firstly, the characterization of the fully operational PS2 sample will be presented and secondly, a failure analysis of the PS1, NS3, and NS4 samples will be conducted, along with proposed solutions to reclaim their functionality. It's important to note that the unexpected insulating behavior, which could stem from various sources during fabrication or growth processes, is challenging to definitively attribute to a single step. Despite all of the effort that has been put to heal these samples, they still remain insulating and will not be characterized elsewhere than this section. Furthermore, many of the explanations put forth in the following sections are currently in the

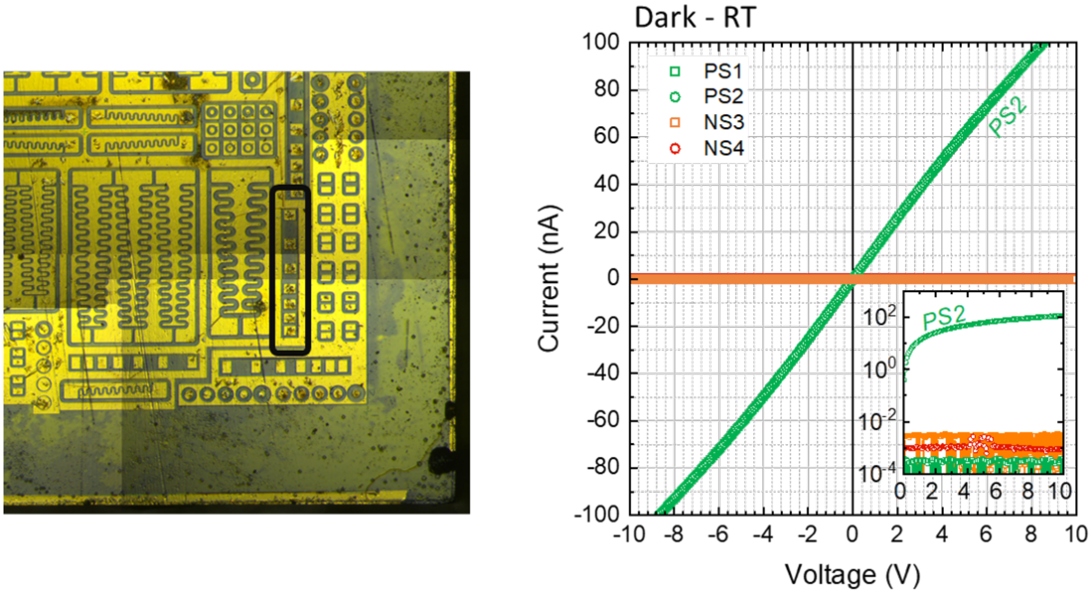

Figure III.14: Optical microscopic image of a rectangular-shaped TLM bar developed on p-diamond mesa structure featuring the p++ selectively grown layer beneath each metallic contact pattern. The I(V) characteristics were measured on 25 µm spaced pads for all four fabricated samples. The inset displays the positive biasing in logarithmic scale, highlighting the lack of current in samples PS1, NS3, and NS4. The measurements were conducted in a dark environment at room temperature.

realm of hypotheses and may necessitate more thorough investigation to establish their validity.

III.5.1 Heavily-doped contacting layer

Prior to channel intrinsic properties characterizations, the resistivity of the metallic diamond layer such as the contact resistance formed by the Ti/Pt/Au stack deposited on top of it, has been characterized. Resistance versus distance plot, extracted from current-voltage characteristics for incremental distances (reported for PS2 sample on Fig. III.15), reveals a resistivity of 2.4 mΩ·cm for the 200 nm heavily boron doped layer. This value is much lower than the ideal (theoretical) p-channel resistivity, where in the later 4 Ω·.cm at RT is in the highest obtainable expectation considering no compensation. Furthermore, the contact resistance R_C is extracted to be 3.3 Ω at RT attesting from a low metal/diamond interface barrier obtained thanks to carbide formation at the interface as expected by the annealing of thin titanium layer in contact with the heavily boron doped diamond.

For such a low resistive contact, the computation of the specific contact resistivity must consider that the current line does not spread inside the diamond below the whole metallic contact. For lateral geometries, the current mostly flows through the edges of the contact, up to the transfer length L_T. The later found to be equal to 2.1 μm has been determined by the resistance versus distance plot of Fig. III.15. Subsequently, the specific contact resistivity, considering that the majority of the voltage drop underneath the metallic pads takes place within in the transfer length, can be expressed as:

$$\rho_C = R_C \times L_T \times W_m \tag{III.8}$$

where W_m is the width of the metallic pads. For the given values $L_T = 2.1$ μm, $R_C = 3.3$ Ω, and $W_m = 70$ μm, the calculated ρ_C is 4.8×10^{-6} Ω.cm^2. When compared to existing literature and supported by Fig. III.16, this value is higher than the record obtained by Ohmagari et al. [248] using 693 K annealing, but slightly better than Kawashima et al. [247] who used

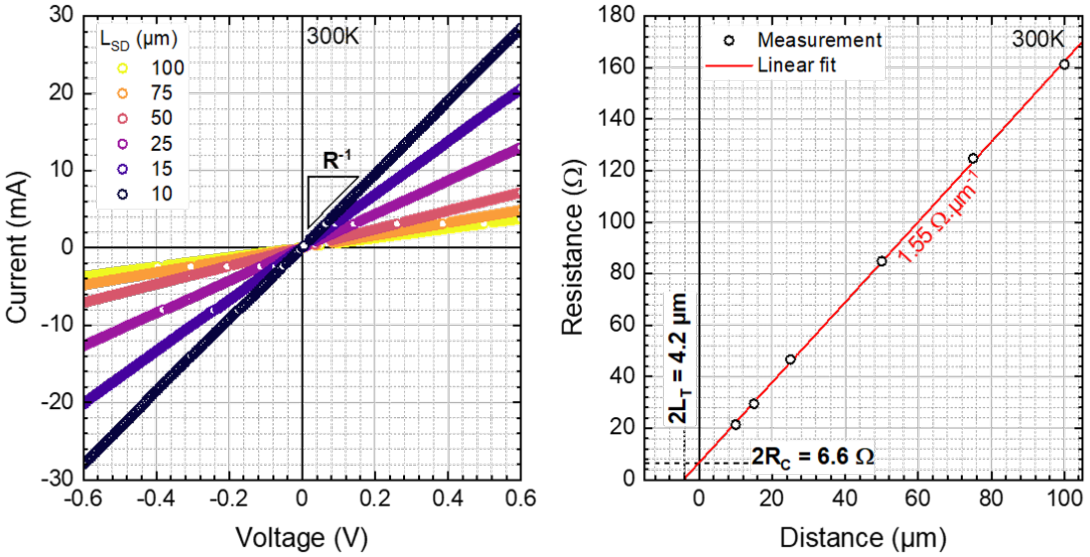

Figure III.15: Left, I(V) characteristics measured on the rectangular-shaped TLM structures fabricated on the selectively grown p++ layer (schematized in Fig. II.14), for different distances L_{SD} between Ti/Pt/Au contacting pads at room temperature. Right, plot of the extracted resistance as function of L_{SD} at room temperature.

673 K annealing. The values reported in this study are thus in good agreement with metallic conduction attributed to the heavily boron-doped layer, with an expected doping density ranging between 5×10^{20} cm^{-3} and 1.5×10^{21} cm^{-3}.

Considering the changes in specific contact resistivity, an optimal post-thermal annealing temperature could be determined depending on the doping level. For doping levels below 10^{18} cm^{-3}, the best results have been obtained with 873 K annealing [300, 319]. In contrast, for doping levels above the metallic transition, the reference value was achieved with 693 K annealing (notably, annealing temperatures above or below this value resulted in lower specific contact resistivity). A more comprehensive analysis, encompassing a wider range of fabricated samples, would be necessary to validate this behavior. While currently not a limiting factor for diamond devices, this aspect should gain significance in the near future as commercial availability of diamond transistors will require optimized fabrication processes.

As comparison with the previously reported GD-030 reference sample [58], the specific contact resistivity obtained using the same growth recipe has been reported with a decade difference. It further confirms that oxide encapsulation performed on GD-030, without etching of the oxide layer above the metallic contact pads, has a slight impact on the contact resistance as well as the transfer length.

The p++ layer's resistivity exhibits a weak dependence on temperature, as depicted in Fig. III.16, which is also an indication that the heavily boron-doped diamond layer is degenerate, implying a metallic nature. The slight positive temperature coefficient further supports the observed transport characteristics akin to metals. Activation energies were estimated, following a similar approach as in [248], and were found to align well with enhanced field emission tunneling (as discussed in section II.5.1.b) at the metal/metallic diamond interface, as elucidated in previous research. Additionally, a connection with interface dislocations is postulated, which could potentially explain the variations in specific contact resistivity between this published work and the results evidenced in this study.

It's worth noting that while the p-channel characteristics have exhibited substantial variations among the four fabricated samples, the heavily boron-doped layer consistently demonstrates highly reproducible and uniform behavior across all samples. Given the similarity of outcomes and to avoid redundancy, results are not provided for every sample; only those of the

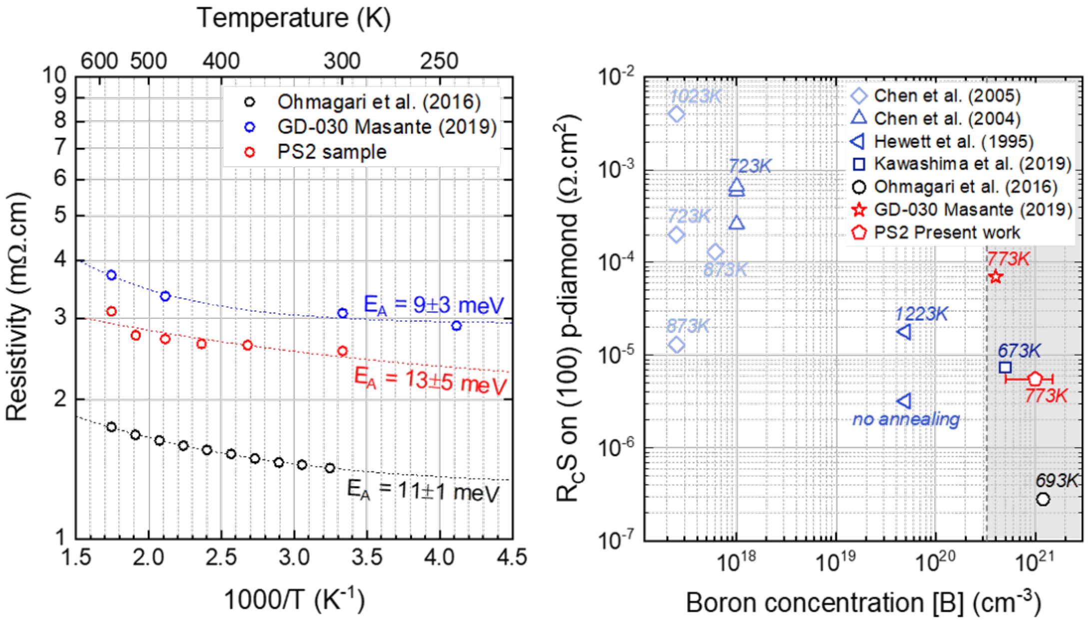

Figure III.16: *Left, temperature dependence of p++ diamond layer resistivity. Heavily boron-doped layer has been prepared by selective CVD growth, with a targeted doping level higher than the metallic transition (between 5×10^{20} cm^{-3} and 1.5×10^{21} cm^{-3}). Dash lines show fitting curve corresponding to activation energy (E_A) reported asides. Right, literature reported specific contact resistivity on (100)-oriented boron doped diamond as function of the doping level, for various annealing temperature, according to [58, 247, 248, 300, 319, 320].*

PS2 sample are shown here. Consequently, both the p++ layer and the metal contacts formed on it exhibit resistances significantly below the ideal p-channel resistance, thus having minimal disruptive impact on the functionality of the fabricated JFETs. Furthermore, the strong consistency observed in the results related to these selectively grown layers suggests that they are unlikely contributors to the non-functionality observed in the PS1, NS3, and NS4 samples.

III.5.2 PS2 p-channel electrical characterization

Current-voltage (I(V)) measurements conducted on the linear TLM-bar of the PS2 sample, considering diverse metallic contact pad spacing and a range of environmental conditions, especially variations in temperature and illumination, are shown in Fig. III.17. As the partial ionization of the dopants in diamonds constitutes a central focus of this thesis, investigating the effects of external stimuli that can be decoupled from the electrostatic control of the components is essential. As discussed in section I.2.2.a, at room temperature and with a target doping level of 2×10^{17} cm^{-3}, the fraction of ionized boron stands at around one in a thousand. By elevating the ambient temperature of the device under test up to 523 K, the population of free carriers engaged in electrical transport rises, leading to a remarkable 30-fold increase in the recorded current. This ionization ratio can be further enhanced by a factor of three through the application of white light with a moderate optical power density of 11 mW/cm^2.

It is worth noting that in both scenarios, the device is driven out of equilibrium due to carrier generation by external stimuli. However, thermal and optical sources provide continuous carrier generation, maintaining, on average, a density of generated carriers that ensures a pseudo-equilibrium state along the reported I(V) characteristics. Notably, illumination of the samples consistently amplifies the measured p-channel current by a factor of 3, regardless of the ambient temperature. While increasing temperature is more efficient to reduce the resistance than using illumination alone, the thermal-optical coupling results in an even more significant enhancement at elevated temperatures. Comparing measurements conducted in the dark at 373 K to those

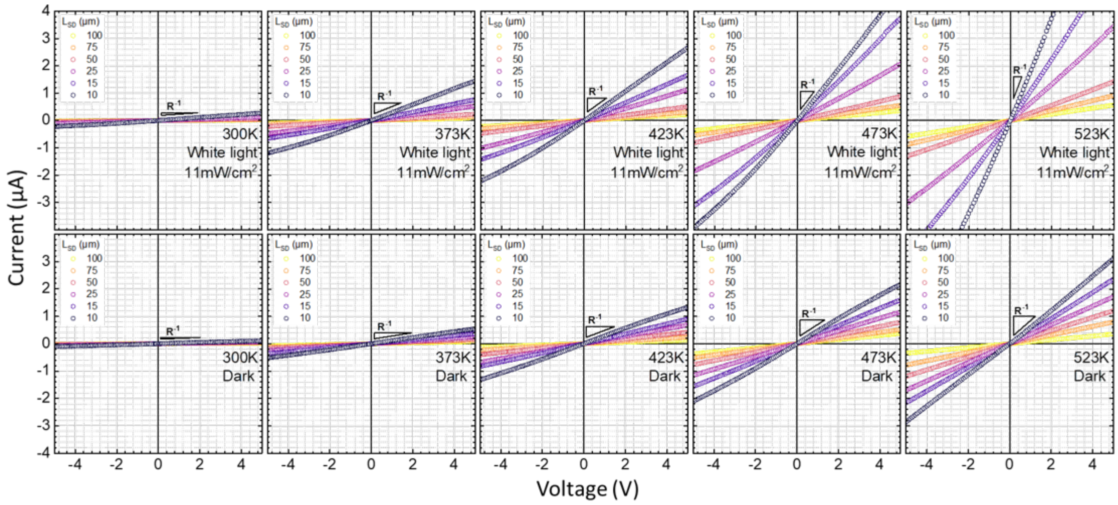

Figure III.17: I(V) characteristics measured on the rectangular-shaped TLM structures fabricated on the p-channel (using selectively grown p++ layer underneath metallic contact pads schematized in Fig. II.14), for different distances L_{SD} between Ti/Pt/Au contacting pads. From left to right the temperature is increased by 50 K starting from 300 K to 523 K. Figures on top reported the devices under white light irradiance of 11 mW/cm^2, where bottom ones are obtained in the dark. Noticeably, the n-layers underneath the p-channels have been grouded during measurments.

obtained at room temperature under white light irradiation, it appears that the current reported at 523 K tends to be closer to the value measured at 423 K with white light irradiation. This trend is tentatively attributed to the increase in the boron optical capture cross-section with rising temperature [360]. However, it is important to consider that this assumption must be weighed against the impact of illumination on the potential barrier present between the metallic diamond and the p-channel. Impact of SCR extension, causing an uncontrolled depletion of the p-channel (detailled in section III.5.3.b) should be avoided here thanks to the grounding imposed to the n-layer on each measurments.

III.5.2.a Contact resistance and metallic diamond/p-channel interface

Similarly to the previous study done on the p++ layer, the resistance extracted from I(V) characteristics (Fig. III.17) is plotted versus the distance between two metallic contacts for the different temperature and illumination conditions used. Results are reported in Fig. III.18, while a better insight of the structure can be found in Fig III.19 (or alternatively II.14).

Even if light and temperature have a similar impact on the ionization of boron inside the p-channel, a significant difference between their respective contribution is observed at the p-channel/metallic diamond interface. While under the dark, a transfer length such as a contact resistance varying with imposed temperature could be extracted, no similar observation could be extrapolated from same measurements under illumination (also coupled with the same temperature range). The former gives rise to an average transfer length of 5.76 μm, slightly higher than previously reported metal/p++ diamond contacts, and no coherent variation with temperature is observed. However, concerning the contact resistance R_C, an exponential decrease is observed with temperature rising, as enlightened in Fig. III.19.

Due to the presence of a barrier φ, resulting from Fermi level alignment at the interface between the degenerate p++ layer and the p-channel, the injection of free holes from the p-channel (or inside, depending on polarization conditions) is slightly impeded. This constrained injection is observed as the primary contributor to the contact resistance observed in the absence of illumination, as illustrated in the equivalent series resistor circuit depicted in Fig. III.19. For comparison, at room temperature and when neglecting the metal resistance (which is signifi-

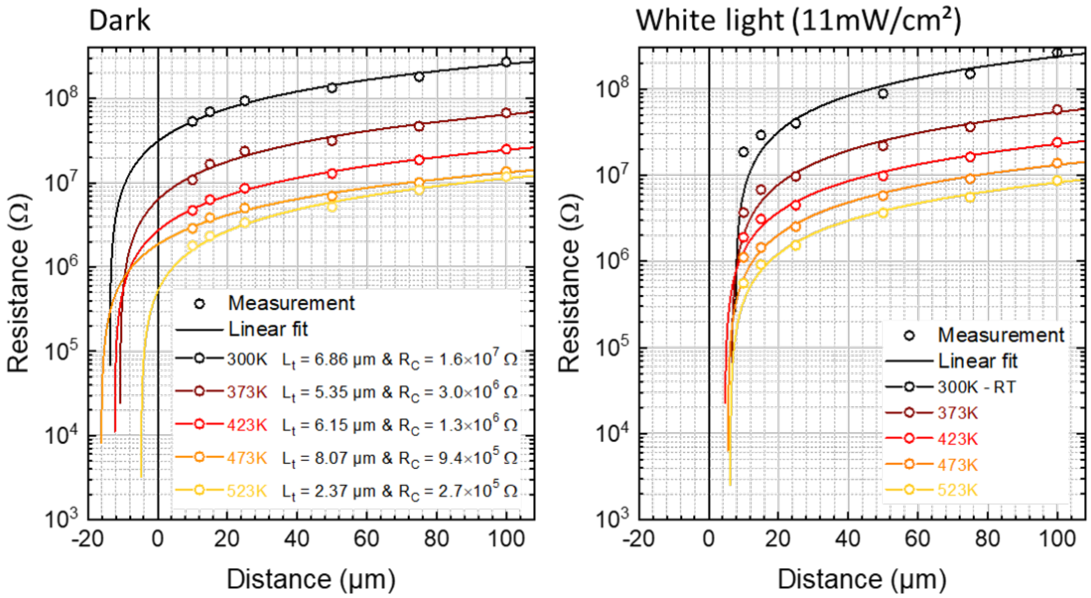

Figure III.18: Resistance versus distance between metallic contacts pads for linear rectangular-shaped TLM structure presented in II.14, measured in the dark (left) or under white light illumination (right), both at room temperature. Measured datas (open circle) has been fitted (straight line) using linear decrease but logarithmic scale representation has been preferred for reading ease. For negative distances part, the fitted curves have been plotted till reaching negative resistance extrapolation, allowing transfer length L_T and contact resistance R_C extraction.)

cantly lower than the others), the metal contact resistance on the heavily boron-doped layer, as well as the sheet resistance of the layer itself, has previously been shown to be 3.3 Ω and 1.2 Ω, respectively. These values are notably lower than the 16 MΩ extracted from the metal/p++/p-channel stacked layers, highlighting the significant impact of the non-avoidable p++/p-channel barrier formation. To further support this behavior, the reduction in contact resistance with increasing temperature aligns with the thermionic field emission (TFE) carrier injection regime, as described in section II.5.1.b. In this regime, the density of free holes crossing the barrier is enhanced by higher thermal energy, contributing to the observed trend.

Illumination of the TLM test structures with white light at an irradiance power density of 11 mW/cm^2 not only alters the resistivity of the p-layer but also affects the measured carrier injection through the p++/p-channel interface. However, when characterizing these structures under combined illumination and temperature conditions, it becomes impossible to directly extract contact resistance or transfer length parameters. This challenge arises because the fitted resistance values become zero for contact distances ranging from 4 to 8 µm. This outcome invalidates the parameter extraction process, as a projected negative resistance for positive distances would be contradictory regarding fundamental transport laws. Interestingly, the non-validity of TLM parameter extraction under illumination can be attributed to a more significant modification in measured resistance for shorter distances (10, 15, and 25 μm) compared to longer distances ($\geq$ 50 μm). Given that the data was collected from the same p-layer mesa-structured TLM bar, it can be assumed that the boron concentration remains homogeneous along various distances, as does the photo-generated carrier density. Potentially, the non homogeneous, extended, or punctual defects distribution could still impede, or enhance, the current flow between metallic pads and give rise to a non-linear resistance variation over pads distances. This hypothesis was quickly ruled out (or at least related to contact resistance) because little variability was observed between the different TLM bars (strategically positioned at the four corners of the sample), which all showed a similar trend. This statistical observation, not shown in this manuscript due to its low relevance, nevertheless reveals that this change in resistance at short

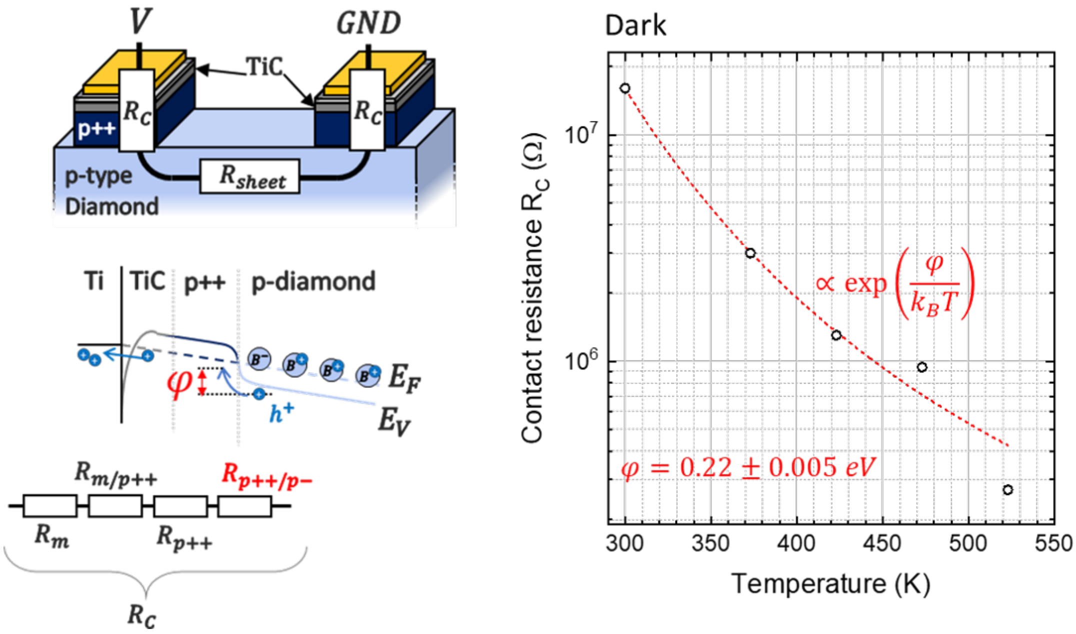

Figure III.19: Left, schematic cross section of metal/p++/p-diamond TLM contacts, under bias, with equivalent series resistors equivalent circuit superimposed. Band diagram of a single contact is displayed underneath, enlightening the barrier height φ formed at the p++/p-channel interface. A decomposition of the contact resistance R_C formed is proposed in respect of the stacked layer displayed in the band diagram. Right, contact resistance extracted as function of temperature (open circle). The red dashed line stands for the fit performed on the measured datas, using exponential decrease through the barrier height, in turns extracted to $\varphi = 0.22 \pm 0.005\ eV$.

distances does not stem from a probabilistic mechanism or depend on a random parameter. Tentatively, contact resistance, which was previously shown to be primarily dependent on the barrier height φ at the p++/p-channel interface, is hypothesized to exhibit non-linear variations under illumination, hence being responsible of the TLM model non-validity. It's worth noting that quantifying changes in the interface barrier solely based on this observation (Fig.III.18) is not sufficient. More comprehensive analysis using advanced characterization tools is needed to provide deeper insights about impact of the light on the p++/p-channel interface.

III.5.2.b p-channel resistivity

Ultimately, low field resistivity of the conducting p-channel has been extracted from the linear slope of R(distance) measurement, under various ambient conditions (e.g. light and temperature), and is plotted in Fig. III.20 as function of the temperature, with and without light.

A decrease of the resistivity as function of temperature rising is observed, as it was expected by the increasing of free holes, largely dominating the mobility lowering. The resistivity as function of temperature is fitted thanks to the empirical model described along section I.2.2.e, (especially using equations I.5) where the doping level N_A and the compensation N_D are fitting parameters. Two fits were carried out in both cases (dark and white light illumination) in order to highlight the discrepancy observed between theoretical models and experimental datas.

Under dark conditions, the best-fit parameters yielded $N_A = 1.6 \times 10^{15}$ cm^{-3} with a compensation ratio of 94.5%. This fitting process involved the measured data across a decade for the temperature range, from 300 K to 523 K, with both N_A and N_D treated as free parameters. Surprisingly, the extracted doping level in this case resembles that of an unintentionally doped layer with an extraordinarily high compensation ratio. This result starkly contrasts with the previously reported $N_A = 7.2 \times 10^{16}$ cm^{-3} obtained from averaged CL measurements (refer to Fig. III.9) and is, therefore, considered inappropriate. To complete this observation, a second

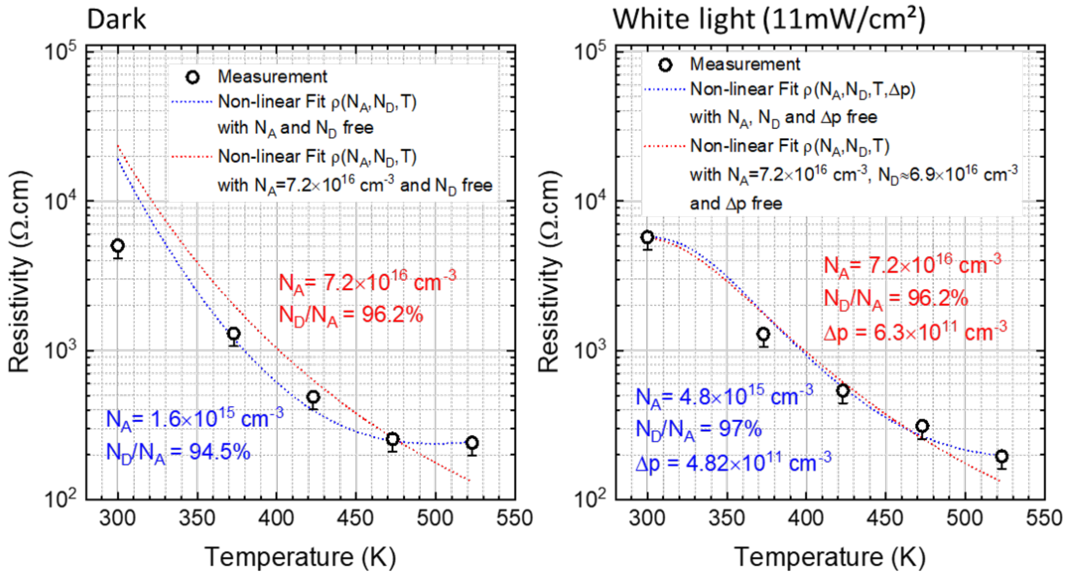

Figure III.20: Resistivity of the p-channel, extracted (open circles) from resistance versus distance plot (Fig. III.18), under the dark (left) and under white light irradiance of 11 mW/cm^2 (right). Dashed line stands for fits performed using equation I.5 (involving variations of p and mu$_p$ with temperature, doping level and compensation), where both doping level N_A and compensation N_D, are used as fitting parameters. Dashed blue line reports fit performed considering unrestricted values for both N_A and N_D, and dashed red line reports fit performed with fixed $N_A = 7.2 \times 10^{16}$ cm^{-3}, extracted from averaged PS2 CL measurements (see Fig. III.9). Under illumination (right), photo-generated free carrier Δp has been added to the fitting model and extracted in both cases.

fit was conducted by fixing $N_A = 7.2 \times 10^{16}$ cm^{-3}. However, this fit resulted in an overall trend that deviated further from the experimental data but still indicated an exceptionally high compensation ratio exceeding 96%. It's worth noting that in both cases, the resistivity at room temperature was not accurately described by the fitting models and appeared inconsistent. This inconsistency might be attributed to variations in the channel width across the entire temperature range, potentially caused by uncontrolled extensions of the backside SCR. Even though the n-layer (or substrate) remained grounded throughout the measurement stages, the diverse SCR extensions, depending on temperature, could have reduced the effective channel thickness.

To account for the influence of white light on the structure, the fitting function was adapted by incorporating the photo-generated free hole density, denoted Δp, as a fitting parameter. Changes in mobility due to illumination were neglected, as they were considered insignificant compared to the increase in carrier concentration. Similar to dark conditions, the best fit was achieved by allowing N_A, N_D, and Δp to vary freely, however, this approach resulted in inappropriate doping levels and compensation, as reported in Fig. III.20. Nevertheless, when the doping level was fixed at $N_A = 7.2 \times 10^{16}$ cm^{-3} and the compensation extracted without illumination (96.2%) was applied, the fitted curve exhibited good agreement with the experimental data, especially a better fitting is observed for room temperature resistivity. In this case, the density of photo-generated free holes, $\Delta p = 6.3 \times 10^{11}$ cm^{-3}, fell within an appropriate range, consistent with similar study done on the Ib substrate under illumination (refer to Fig. III.1). Comparing both fits, the doping level has a lesser impact than compensation on the fitted output curves, while the photo-generated free hole density computed remains at a similar order of magnitude for both doping levels. This observation aligns with the detrimental effect that such a high compensation ratio can have on the resistivity, where the reported resistivity at room temperature ($\rho = 5$ kΩ·cm) is more than three decades higher than the targeted value ($\rho = 5$ Ω·cm).

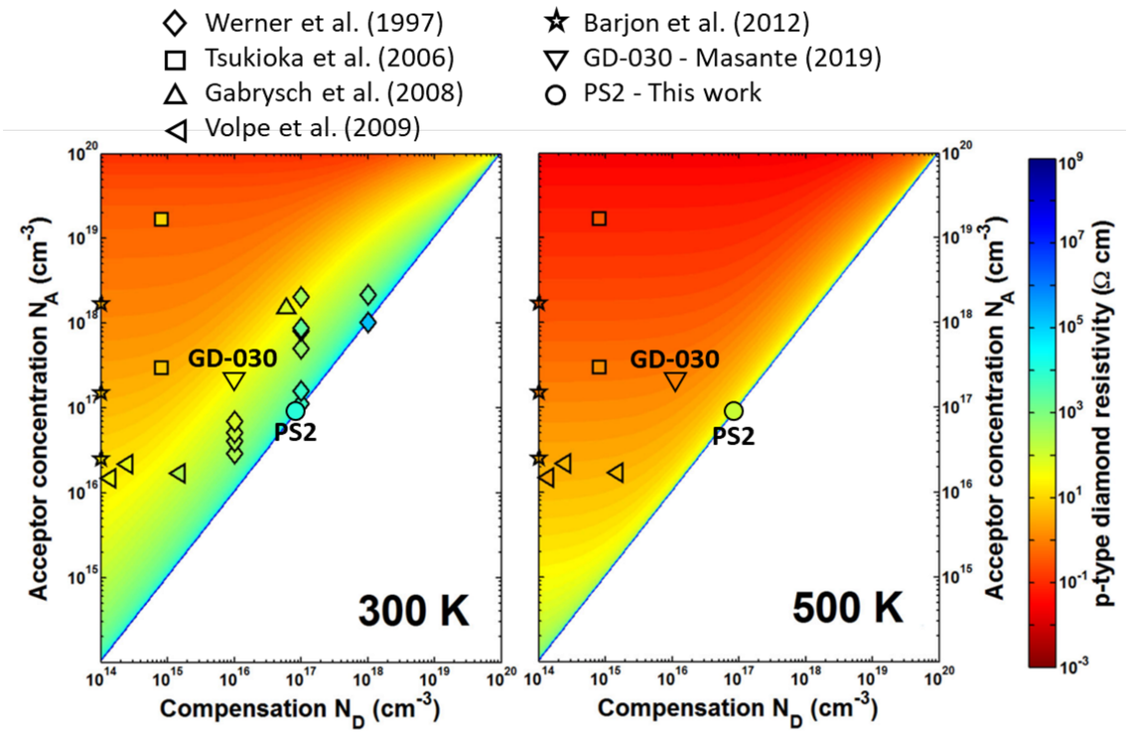

Figure III.21: p-channel resistivity as function of acceptor concentration N_A and compensating donor concentration N_D, in various p-type diamond layers reported in literature, from [58], updated from [178]. Experimental datas are taken from Barjon et al. [186], Volpe et al. [156], Gabrysch et al. [185], Werner et al. [183], Tsukioka et al. [184], reference GD-030 from Masante [58] and this work

A comparison of the extracted compensation ratio to literature is shown in Fig. III.21, compiled by Traore et al. [178] and updated by C.Masante [58]. The compensation ratio values reported in literature have a very wide range, but even if obtaining 95% could have been reported 25 years ago [183], this value is uncommon nowadays. Based on values reported since 2009, at 500 K, the resistivity of ≈ 200Ω.cm measured in this thesis is the worst. Regarding to the deleterious effect of high compensation on layer resistivity, reducing it is mandatory to scale up ON-state performances of the fabricated devices.

III.5.2.c High resistance and compensation impact on transport characteristics

The high compensation previously reported, has been mentioned to have a detrimental impact on the p-channel resistivity but it is also demonstrated along this section to also impact the contact resistance. Concerning the former, Fig. III.22 enlighten the 96.2% compensation ratio extracted for PS2 sample, compared with the 5.5% extracted from reference sample GD-030 which gives rise to more than two decades difference in the concern of the layer resistivity.

The substantial difference in layer resistivity can primarily be attributed to the significant contrast in ionized free carrier density computed for both devices, as illustrated in Fig. III.20. The free hole density, along with their mobility, was extracted from the temperature-dependent resistivity data using models detailed in section I.2.2.e. The mobility is quite similar for both samples, reflecting comparable total impurity numbers (the sum of dopants and compensation density) of $N_{\text{imp}} = 1.4 \times 10^{17}$ cm^{-3} for PS2 and $N_{\text{imp}} = 2.1 \times 10^{17}$ cm^{-3} for GD-030, which has a relatively minor impact on the p-layer resistivity. However, the carrier density is strongly influenced by the difference in doping levels, and even more so by the compensation effect, as demonstrated by the three-decade difference observed at room temperature between the two samples. This difference remains nearly constant within the studied temperature range, and

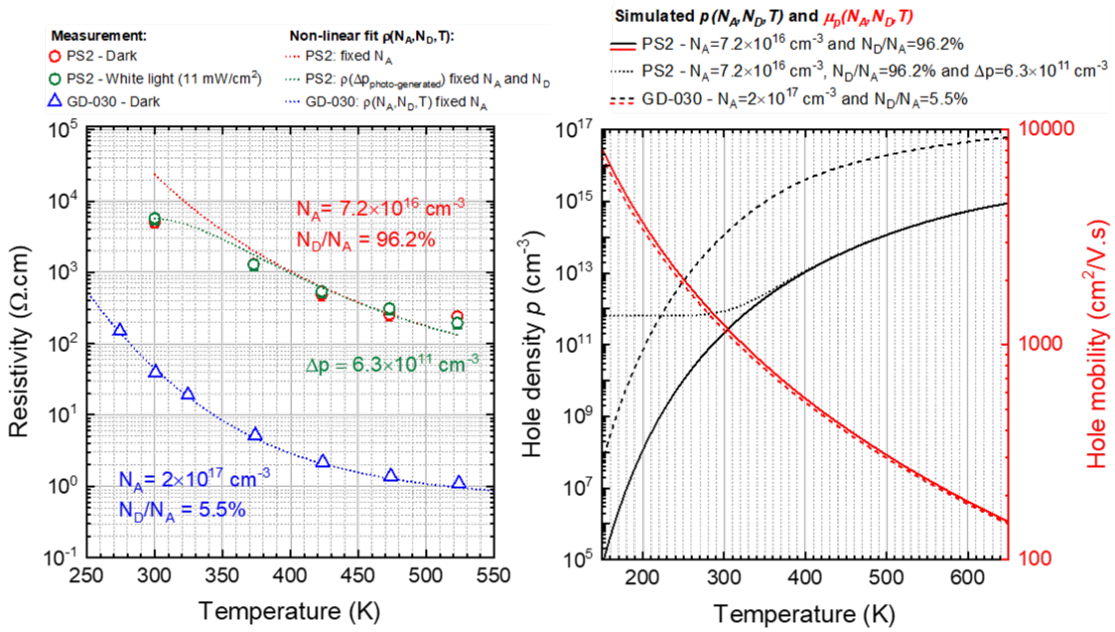

Figure III.22: Left graph: p-channel resistivity, under the dark (red) and under white light irradiance of 11 mW/cm^2 (green) for PS2 sample (open circles) and reference sample GD-030 (open blue triangle). Dashed line stands for fits performed using equations (X.X), where doping level N_A have been fixed using averaged CL measurements for PS2 (see Fig. III.9) or capacitance voltage measurement for GD-030 [58], in order to extract compensation ratio N_D/N_A. Green dashed line stands for the extracted photo-generated free holes, considering fixed N_A and N_D extracted without illumination. Right graph: Simulated free holes density and their associated mobility as function of temperature, using models presented in section (X.X) with N_A and N_D extracted from left hand graph.

illumination does not significantly affect operating temperatures above 350 K. Nevertheless, when illuminated, PS2 samples exhibits a consistent free hole density of 6.3×10^{17} cm^{-3}, which can compensate for the high compensation effect at lower operating temperatures (below 200 K).

Interestingly, concerning the barrier height of 0.22 eV, arising from the p++/p-channel interface and previously reported in Fig. III.19, the computation of the Fermi level position in the p-channel can give a better insight of the barrier origin such as its link with compensation. By definition, in non-degenerate semiconductors, the doping concentrations are generally smaller than the valence band density of state N_V, and the Fermi level E_F is more than several $k_B T$ above the valence band E_V. In this case, the Fermi-Dirac integral over the density of state (DOS), where Boltzmann statistics apply, simplifies Fermi-level expression [208] as:

$$E_F - E_V = k_B \cdot T \cdot \ln\left(\frac{N_V}{p}\right) \tag{III.9}$$

where the free hole density (p) is calculated using equation I.7, which establishes a relationship between the Fermi level position, doping level, compensation, and temperature. Fig. III.23 illustrates the variations in Fermi level positions as a function of the compensation ratio ($k = N_D/N_A$). In the p-channel, with a doping level of $N_A = 7.2 \times 10^{16}$ cm^{-3} and a compensation ratio of 96.2%, the Fermi level is positioned 0.21 eV above the valence band. Given the proximity of this value to the barrier height at the p++/p-channel interface (see Fig. III.19), it is supposed that a free hole from the p-channel needs to overcome a barrier ($\varphi \approx E_F$) to be injected into the p++ layer. This hypothesis is further supported by the idea that a free hole in the p-channel can tunnel into an available free state in the p++ layer (or vice versa), which, due to Fermi level alignment, is likely located at an energy level E_F. Consequently, the high contact resistance at the p++/p-channel interface is primarily determined by the Fermi level position within the p-channel, which is in turn dependent on the layer's compensation ratio, as illustrated in the band diagram in Fig. III.23. It's important to note that Fermi level position variations are relatively small for compensations below 80%. However, for compensations exceeding this value, the Fermi level position increases exponentially with the compensation ratio. As a result, while variations in the compensation ratio between 10% and 20% have an insignificant impact, the same variation between 85% and 95% has a dramatic effect on the Fermi level position and, consequently, carrier injection at the interface.

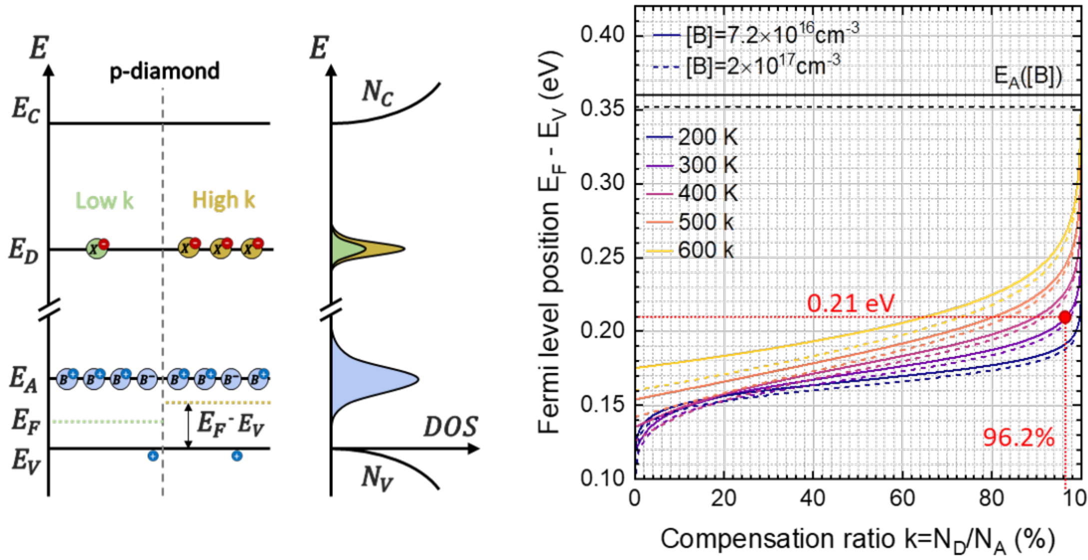

Figure III.23: Left, schematic band diagram and density of state (DOS) for the p-diamond layer at thermal equilibrium. Two cases are represented to enlighten the Fermi level position variation, with low compensation ratio (k) at left and high compensation ratio on right. Right, Fermi level position (referenced through valence band position $E_F - E_V$) as function of compensation ratio for various temperatures and doping levels.

As an initial partial conclusion for the PS2 sample, electrical conduction was observed, albeit significantly deviating from the initial expectations and well beyond the predicted potential margin of error. Abnormally high contact resistance and layer resistivity, on the order of tens of MΩ and a few kΩ.cm, respectively, have been reported. Both of these issues have been attributed to a very high compensation ratio, exceeding 95%, which has been shown to have a detrimental impact on the overall performance of the fabricated devices. Since this sample is the only one that exhibited operational characteristics, it provides insights into the non-functionality of the others, where fully compensated layers could effectively prevent conduction, as observed in the case of the PS1, NS3, and NS4 samples.

III.5.3 PS1, NS3 and NS4 samples failure analysis

Oppositely to PS2 sample, no efficient conduction has been reported for the three other fabricated samples. More precisely, the characterized devices where too resistive at low bias and at room temperature in a way that no current (below detection limit of nA/mm) could be recorded below 80 V in these conditions. Regarding the very large compensation extracted from PS2 sample (above 95%), the most likely hypothesis regarding the non-functioning of the other three fabricated device, is the presence such high compensation. To status on this assumption, a failure analysis is conducted in the following sections.

III.5.3.a External energy application toward higher ionization ratio

In the case where 1/1000 substitutionnal boron atoms are ionized at room temperature, and more than 95% of them could be compensated, it is reasonable to consider that boron-doped diamond partial ionization can cause the p-layer to be recorded as insulating. However, in this case, the conductivity should still be tunable thanks to external power application such as temperature increase or illumination. Both, coupled or not, have been tried and reported on Fig. III.24.

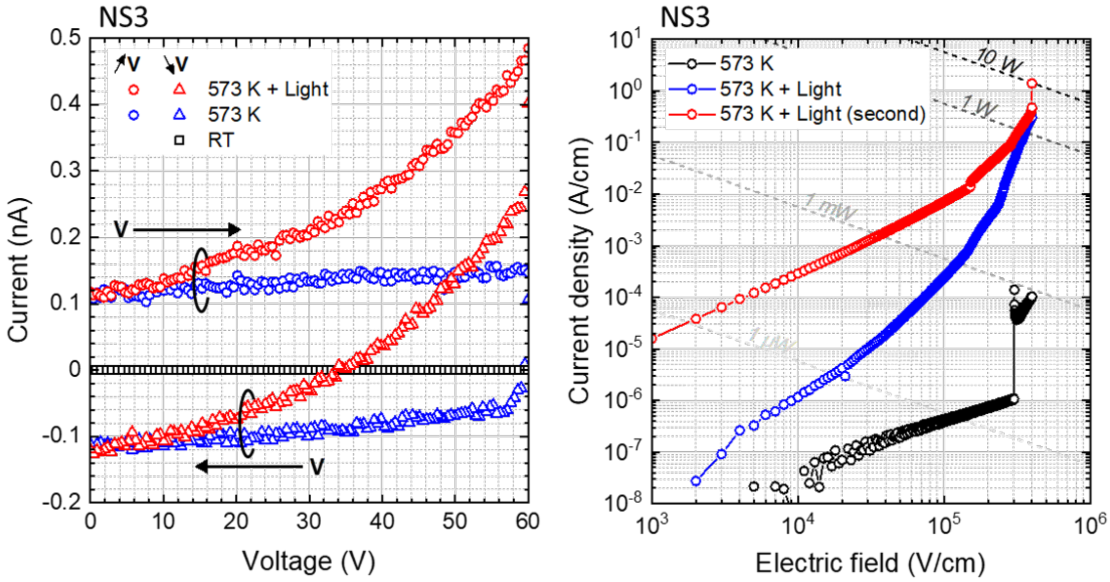

Figure III.24: Left, I(V) characteristics of 25µm spaced TLM contacts, on sample NS3, for different temperature and illumination (white light of 11mW/cm^2) conditions. Hysteresis is enlightened by increasing or decreasing biasing conditions. Right, current density vs. electric field at 573 K, before and after illumination. Illuminated measure has been repeated twice to enlighten disparity caused by successive measurements.

Although the measured current shows significant enhancement at elevated temperatures (250°C) and even more so when exposed to white light irradiance of 11 mW/cm^2, the recorded values at 50 V remain below the nanoampere (nA) range, whereas an ideal value of 7.5 mA was anticipated for contacts spaced at 25 µm. Moreover, while illumination does lead to a slight improvement in the activation of conductive impurities, with a better efficiency than high temperature, it remains way below the targeted value. A noticeable hysteresis effect is observed between the voltage increasing and decreasing steps, indicating the presence of active impurities or traps within the layer or at the interface with the p++ layer. This has been verified with analogous measurements on PS2 sample, which exhibited higher conductivity where, hysteresis under illumination was observed at high sampling rates but tended to diminish at slower rates more suited for non-equilibrium conditions. A more detailed analysis of these defects, potentially through techniques like deep-level transient spectroscopy (DLTS), might offer further insights. However, given the subpar results achieved, substantial effort would be needed to obtain meaningful feedback. High voltage measurements indicated a breakdown voltage of 997 V, corresponding to a critical electric field of 400 kV/cm, significantly below the theoretical value of 10 MV/cm expected for diamond. Additionally, high-voltage I(V) characteristics were obtained in multiple trials under illumination, with increased conductivity consistently reported after the first measurement. This subsequent rise in current density is tentatively attributed to self-heating of the sample, resulting from its need to handle significant power during high-voltage operation. While temperature changes were monitored on an alumina plate, holding both the sample and the thermometer, during the experiments, the confirmation of this behavior using a thermal camera during power load tests will be necessary to validate the self-heating hypothesis.

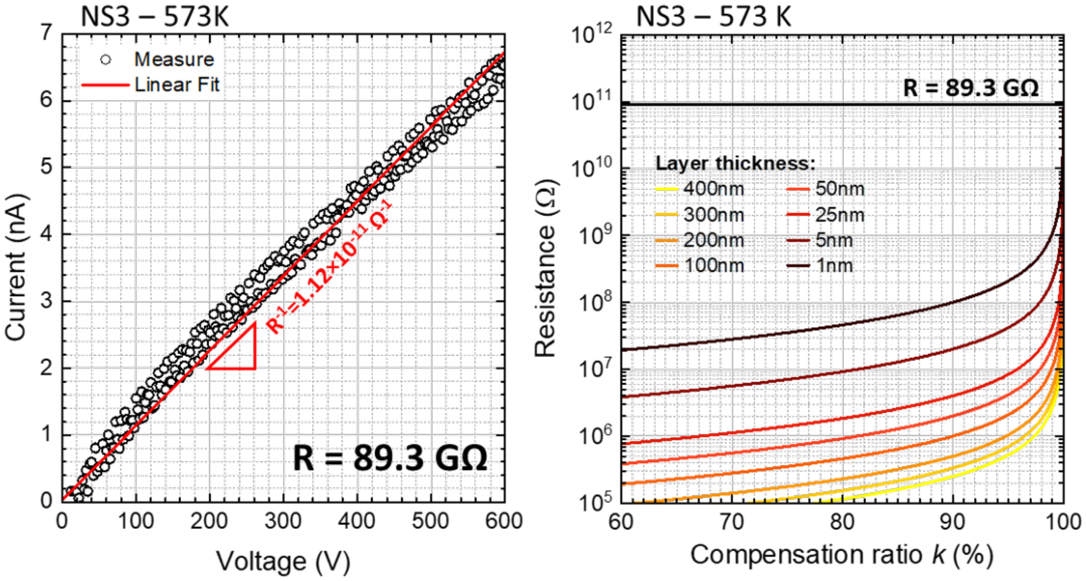

Figure III.25: Left, I(V) characteristics of 25µm spaced TLM contacts, on sample NS3, at 573 K and under the dark. Linear fit have been performed to obtain the layer resistance. Right, simulation of the resistance versus compensation ratio $k = N_D/N_A$ *for different layer thickness* t_p*. Models presented in section I.2.2 have been used to simulate this dependency, whereas layer thickness which tends toward low value are used to enlighten the insufficiency of boron activation or compensation models solely to describe non-functionalization of the devices. Boron doping level of* 6.6×10^{16} *cm*$^{-3}$ *used in this simulation have been extracted from cathodoluminescence measurements at the same place of the electrical characterisation (see Fig. III.9).*

Fig. III.25 illustrates how insufficient boron doping levels or an extremely high compensation ratio fail to explain the non-functionalization of the devices. High-temperature (573 K) dark I(V) characteristics reveal an exceptionally high resistance of 89.3 GΩ. For comparison, a defect-free, uncompensated layer with uniform thickness would exhibit a resistance less than 85 kΩ, which is six orders of magnitude lower than the measured value. The models outlined in Section I.2.2 were used to better illustrate the detrimental impact resulting from growth-related issues. It's worth noting that the impact on layer resistance is less severe for compensation ratios between 60% and 90%, resulting in a tenfold increase. In contrast, extremely rare compensation ratios between 98% and 100% lead to over two decades of resistance increase. To achieve the measured 89.3 GΩ resistance with a boron doping level of 6.6×10^{16} cm^{-3}, estimated via CL, calculations suggest that the p-layer must be approximately 1 nm thick, with a compensation ratio as high as 99.8%. In comparison to previously reported work using the same growth methods and equipment [58, 245], this discrepancy in compensation ratio and layer thickness appears inconsiderable. It does, however, indicate that a thinner layer than the initially targeted 400 nm was likely fabricated, and potential alternative mechanisms may be influencing its effective thickness for current conduction.

III.5.3.b p-channel backside depletion due to uncontrolled n-type gate biasing conditions

This section is a preliminary exploration of how controlled gate biasing profoundly influences the optimization of the p-channel conduction cross-section within the fabricated JFET. Here, we focus primarily on parasitic phenomena, especially those related to the potential non-functionalization that might arise from uncontrolled n-type gate biasing. Detailed JFET piloting will be thoroughly addressed in the subsequent chapter. As established in previous discussions, the need for an effective p-channel conduction cross-section has been identified as a critical factor in explaining the non-functionalization observed in samples PS1, NS3, and NS4. Coupled with the threshold voltage shift, as discussed in section II.3.1.e, which results from variations in doping levels, compensation, and layer thickness, exploring the possibility of normally-off transistors was mandatory. However, our findings in this regard have been inconclusive. The three different configuration used are summarized in Fig. III.26, whereas optimised activation conditions have been ensured through white light illumination of 11 mW/cm^2 and high temperature, 573 K.

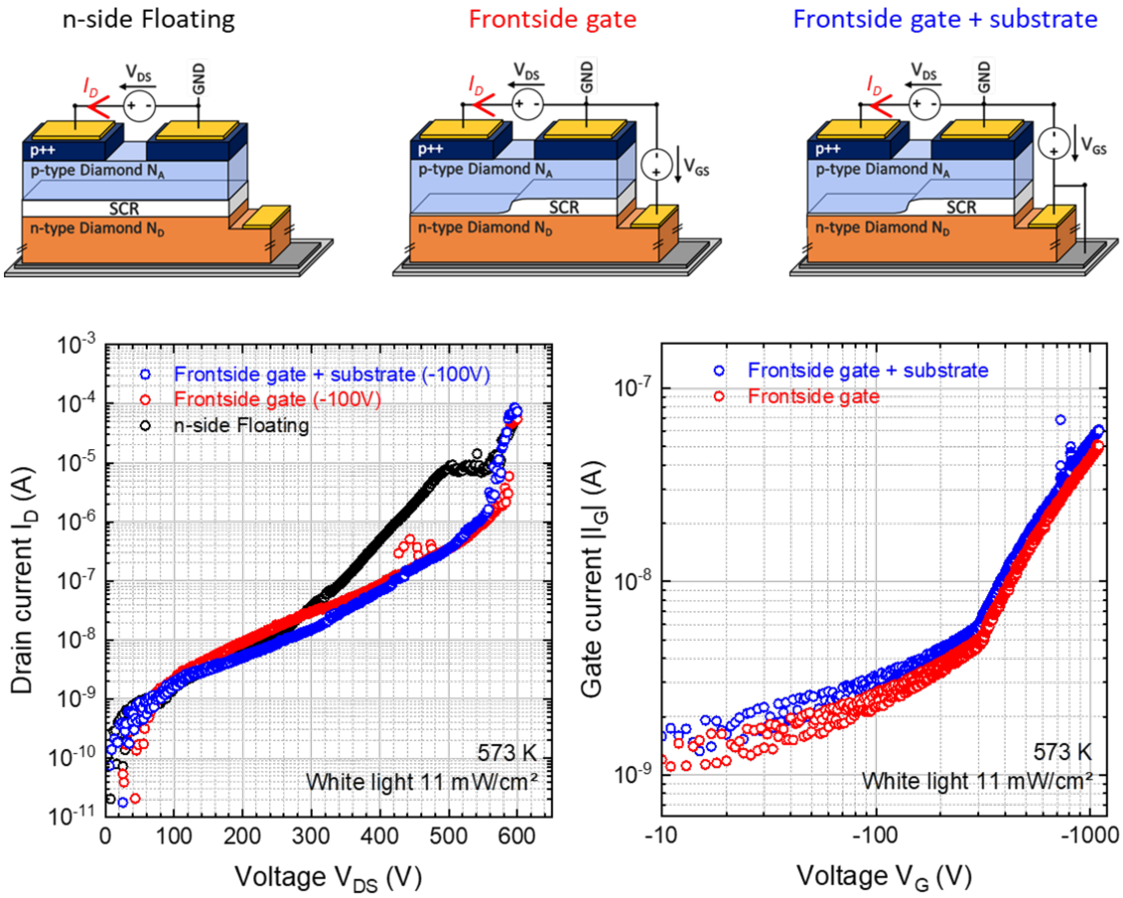

Figure III.26: Top, schematic cross section of the three n-side biasing configurations used on NS3 sample. Bottom, output $I_D(V_{DS})$ characteristics (left) and gate leakage current vs. gate bias $I_G(V_{GS})$ (right) for the three configurations depicted herein-above, at 573 K and under white light irradiance of 11 mW/cm^2.

In the initial configuration, experiments were conducted without applying bias to the n-diamond. It was observed that more than 400 V were required to achieve an absolute current value exceeding a μA. Surprisingly, when negative voltage was applied to the n-side, effectively biasing the pn junction formed with the p-channel in the forward direction and minimizing the space charge region (SCR), the results were even less favorable. This was observed when biasing either the frontside gate or both the frontside gate and the backside of the substrate to prevent and bypass any potential front-gate malfunction. Strikingly, these gate biasing configurations resulted in a lower drain current density compared to scenarios without any n-side biasing. To put this into perspective, current levels above μA were only achieved at voltages exceeding 550 V for both gate biasing configurations. Moreover, in the latter case, a negligible gate current was recorded, which was orders of magnitude lower than the drain current. This observation underscores that gate polarization does not significantly contribute to the reduction in drain current. In conclusion, it was found that biasing the n-side has no discernible impact on the p-channel's conductivity. It also indicates that the non-functional transistors are not inherently normally-off or depleted by the extension of the pn junction's space charge region into the p-layer.

III.5.3.c p-channel frontside depletion, Fermi level pinning and oxide encapsulation

While p-channel depletion from the backside has been ruled out, depletion from the topside of the sample, arising from Fermi level pinning has also been unveiled. By definition, diamond surfaces does not have the same periodicity as the bulk, thus fixed electron states in the forbidden band may sub-exists [361] near the surface due to symmetry rupture. Subsequently, lower energy states may be filled, whereas higher energy states may be left empty. Highly related with the diamond surface termination, O-, H- or even OH-terminated [46], Fermi level positioning at diamond surface or interfaces gives rise to potential accumulation layer for holes (H-FET) or oppositely a depletion layer thanks to O-termination [356]. Subsequently, uncontrolled (or poor) diamond surface termination can lead in the formation of a SCR, arising from the topside in the lateral JFET geometry presented in this manuscript, ultimately causing the reduction of the p-channel effective conduction cross-section. However, even if this effect cannot be properly removed, except by modifying the diamond surface, it can be fixed thanks to oxide encapsulation. In the specific case of oxide addition, Fermi level pinning arising from charge transfer at the interface between the diamond and oxide. Alumina deposition has thus been realized on PS1 samples after oxygen termination thanks to deep UV ozone technique, in order to passivate the surface and fix the depletion layer caused by Fermi-level pinning. Deposition has been realized by Atomic Layer Deposition (ALD) at 380°C, with the same characteristics than GD-030 reference samples, e.g. 50 nm followed by a 500°C annealing for 30 min in high vacuum [58]. Scheme of this encapsulation and electrical characterisation after oxide deposition are reported in Fig. III.27.

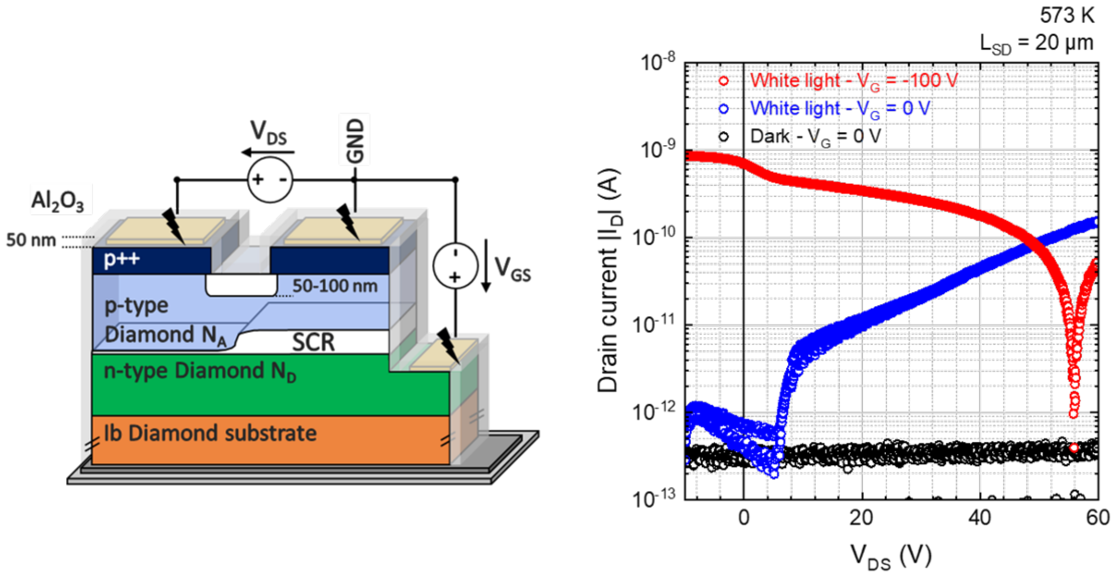

Figure III.27: Left, schematic cross section of PS1 sample after ALD oxide deposition. The oxide can be punctually opened through the application of high voltage on its surface, right on top of a metallic contacting pad. Right, output $I_D(V_{DS})$ characteristics for various external and polarisation conditions: white light (11 mW/cm^2) ON or OFF, and V_G using frontside gate plus substrate biasing as shown in Fig. III.26 maintained at 0 bias or strongly polarized in forward with -100 V where the SCR from the backside should be totally removed.

As depicted, the surface covered by the oxide layer in the sample is shown to have a substantial surface potential, leading to the depletion of a portion of the p-layer. Previous studies [76, 245] have determined that this depleted layer's thickness typically ranges between 50 nm and 100 nm, based on CV measurements. It's worth noting that slight variations in these reported values can be observed depending on factors such as temperature and biasing conditions. One additional plausible hypothesis is that surface pinning may be mitigated by optical excitation, although this assumption requires further analysis and has not been thoroughly investigated in this work. Regrettably, despite the addition of oxide, no significant improvement in conductivity was observed, and thus, the effective conduction cross-section of the p-channel remains unresolved. This remains the case even under optimized activation conditions, including high temperature (573 K) and white light illumination (11 mW/cm^2), as well as forward biasing the n-side. At 50 V, the current level remains markedly blocked at less than 0.1 nA, significantly below the expected output in the range of a few mA. Nevertheless, it's important to highlight that the electrostatic control of channel conductivity through the n-side gate has been substantially altered. This is evidenced by the measurable nA current for zero bias conditions and the absence of current at 56 V. This intriguing regime is tentatively attributed to the photogeneration of carriers originating from both the p-channel and the n-gate layer, but a more detailed exploration of this phenomenon has not yet been conducted.

While oxide encapsulation did not resolve the p-channel's poor conductivity, it did demonstrate, through a significant modification in electrostatics, the sensitivity of the channel to the modulation of effective conduction thickness. Higher drain voltages, could potentially have led to an opening of the p-channel, retrieving conductivity expected for a boron doping level of 6.6×10^{16} cm^{-3}, but this would have been too far from the targeted voltage operating range of the transistor.

III.5.4 Summary

Efforts to restore the p-channel's conductivity to the intended levels have proven to be unsuccessful. Multiple strategies were explored to enhance both the expected free hole density, potentially hindered by high compensation ratios, and the effective conduction cross-section of the lateral p-channel, which could be affected by parasitic depletion layers from the frontside and/or backside. High operating temperature combined with white light illumination was employed to enhance the boron ionization ratio, as detailed in section I.2.2.e, but the observed impact fell short of expectations. This attempt revealed that high compensation ratios alone do not account for the extraordinarily high resistance recorded in the p-channel. The geometry of the channel must also be influenced by fabrication issues, thus contributing to the observed almost-insulating properties. Efforts were made to modulate the effective channel thickness, which is a challenging parameter to verify non-destructively and a significant factor affecting current flow. Unfortunately, these attempts did not yield conclusive results. Furthermore, the prospects of JFET operation were explored, including strong forward biasing of the gate or the pn junction formed between the p-channel and the n-side layer, with the aim of eliminating the backside SCR, potentially responsible for non-functional transistors. Surprisingly, the results obtained under these conditions were even less favorable in terms of current density compared to keeping the n-gate floating (unbiased and unconnected). Depletion from the topside of the p-channel was fixed through O-termination and subsequent oxide encapsulation, yet the results remained unconvincing and fell short of achieving the desired p-channel conductivity. Of course, various combinations of these solutions were attempted, but none provided a more promising outlook. In summary, non-functional samples likely result from a combination of factors, including lower boron doping levels, very high compensation ratios, and thinner layer thickness compared to the targeted values. In this unfortunate scenario, it appears that the PS2 sample may have been less affected by these unfavorable trade-offs than the other samples, making it relatively more conductive, though still below the initially planned specifications. These observations offer valuable insights into the potential impact of fabrication or growth-related issues that need to be considered for future optimization and fine-tuning of the p-channel's conduction characteristics.

III.6 Gate contacts and layers electrical properties

Given that n-diamond layers are integral for controlling channel width and managing leakage current in fabricated JFETs, a comprehensive understanding of their properties is mandatory. A particular emphasis is placed on examining the critical role played by the added phosphorous layer in terms of contact ohmicity. Regarding functionalization results obtained by prior characterizations focused on the p-channel, this section concentrates primarily on PS2 sample, but a comparison is still held with PS1 sample which also benefits from the phosphorus-doped layer. However, it's worth noting that the dedicated TLM structure and models, as presented in section II.4.1.b, used to assess both layer resistivity and contact properties, were found to be inadequate in explaining the non-ohmic behavior observed. Nonetheless, despite these limitations, the analysis has provided valuable insights, and the ensuing discussions revolve around the constraints of these models.

III.6.1 Non-Ohmic behavior: Phosphorous non-ionization and/or non-activation

First typical current-voltage I(V) characteristics measurement attempts, on PS1 and PS2 samples, were conducted under the dark, at RT, and were sold by an absence of conductivity, with a reported current below the detection limit of 0.1 pA. This first observation directly questioned the doping level and quality of the phosphorous-doped layer, as for similar layer properties and measurements conditions, current higher than the μA was expected [166, 169, 195]. However, similarly to boron, illumination and higher temperature were used to enhance dopants ionization and record I(V) characteristics presented in Fig. III.28.

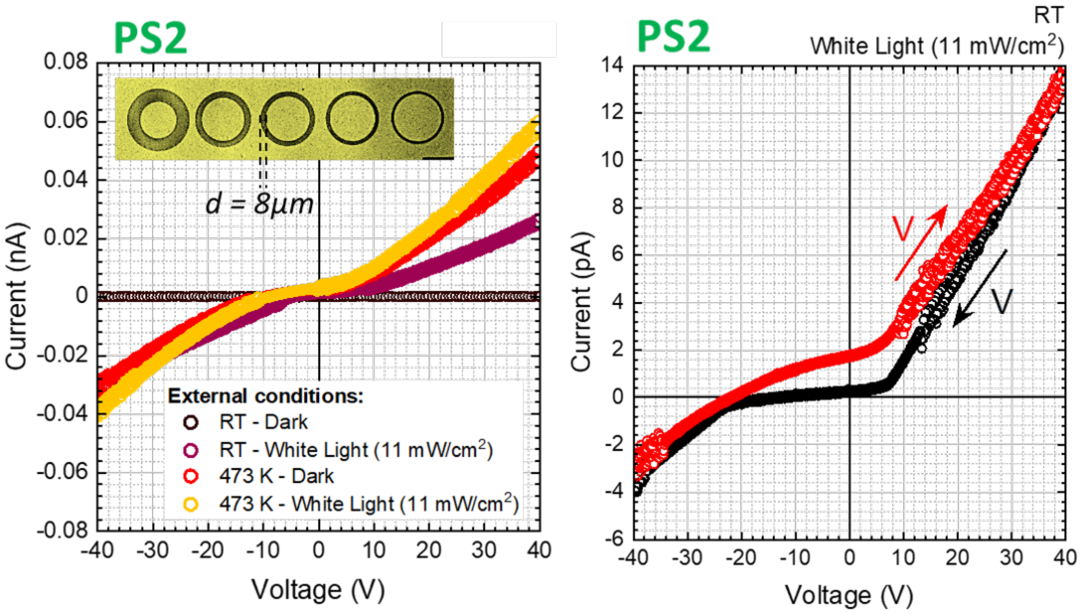

Figure III.28: Left, typical current-voltage I(V) characteristics between two 8 µm spaced neighboring contact pads of PS2 sample, under various illumination and operating temperature couples. Right, focus on I(V) hysteresis between downward or upward voltage changes, measured at RT under a white light illumination of 11 mW/cm^2.

While the ionization ratio can be effectively modulated with the assistance of illumination, temperature, or both, the recorded current levels remain significantly low. This observation, whether examined in isolation or, more crucially, in conjunction with CL measurements reported in section III.2.1, initiates discussions and failure analysis akin to those concerning the p-channel. The attainment of high phosphorous activation, such as its placement in substitutional sites within the lattice rather than interstitial sites or grouped in complexes, has been a feat achieved by only a select few research teams worldwide [143, 152, 165, 344, 345]. In most of these reports demonstrating room temperature conductivity, no illumination was required to achieve notable current values. Furthermore, enlightenment required in this work to bring conductivity in the layer, also come along non-equilibrium conditions where layer resistivity extraction can be over-estimated without specific models implementations. Obviously, an ideal ohmic property was clearly not obtained, the contact behavior is closer to a non-ideal Schottky diode, as a non-negligible barrier remains at low voltages. This behavior is further supported by the EBIC image shown in Fig. III.29, where the inner circular TLM contact remain Schottky over different polarity, as witnessed by the brightening SCR underneath the contact electrode.

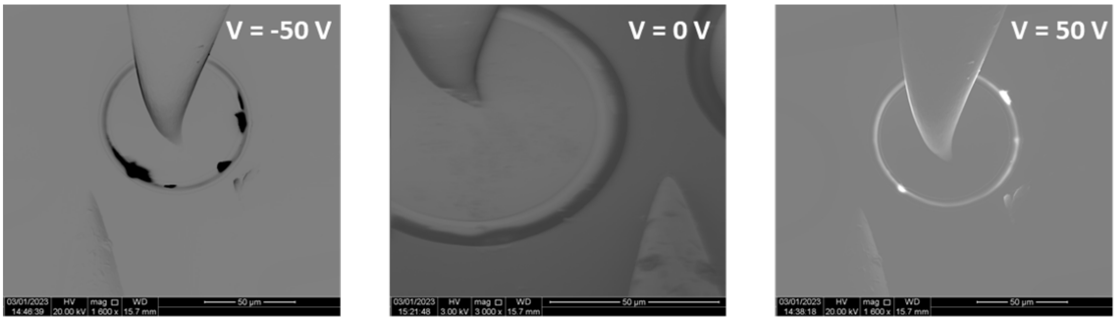

Figure III.29: EBIC images of 10 µm spaced circular TLM contact pads of PS2 sample, under various biasing condition, imposed on the inner electrode.

The barrier does not exhibit a significant changes with light or temperature, as it could be previously reported for Schottky diodes with thin semi-transparent gold deposition [362]. Fabrication of such semi-transparent metal deposition on phosphorous doped diamond must be further developed as it could be highly beneficial for NVPS fabrication due to the significant increase of the light collection efficiency provided. Nevertheless, a slight barrier changes have been reported, depending on both voltage sweep rate but mainly on the difference between voltage rising or falling. Noticeably, for upward voltage sweep, from negative values toward positive ones, a non negligible current is recorded at zero bias, while being not observed for falling voltages. The latter attests of a charge carrier detrapping, where fixed states are full-filled at high voltages and emptied during the sweep. Hysteresis loop results from large trap capture and/or emission time constants which, respectively, characterize the time required for majority carriers to reach a steady-state value during charging and discharging processes [363]. Through the contribution of external energy, e.g. light or temperature, the n-diamond is pushed out of equilibrium, hence time related charge trapping or detrapping could strongly contribute to this hysteresis [364].

Poor ohmic behavior was also observed on PS1 sample as depicted in Fig. III.30, which, even if previously being reported as non-functional for JFET applications due to the absence of p-channel conductivity, should exhibit n-type conductivity.

For PS1, almost no dependence of the I(V) characteristics regarding the contact spacing has been recorded at low voltages. Under higher biasing conditions (≥30 V) slight modulations are induced but still in the range of few pA, way below the µA for same doping levels targeted [169] or the mA for one order of magnitude higher doping level [166]. This trend holds true for PS2 as well, although we do observe a more pronounced disparity between positive and negative current values. It's worth noting that in the aforementioned references, where a non-ohmic behavior was also reported, the I(V) characteristics were clearly dependent on the contact spacing, underscoring the potential low activation obtained in the devices fabricated within this

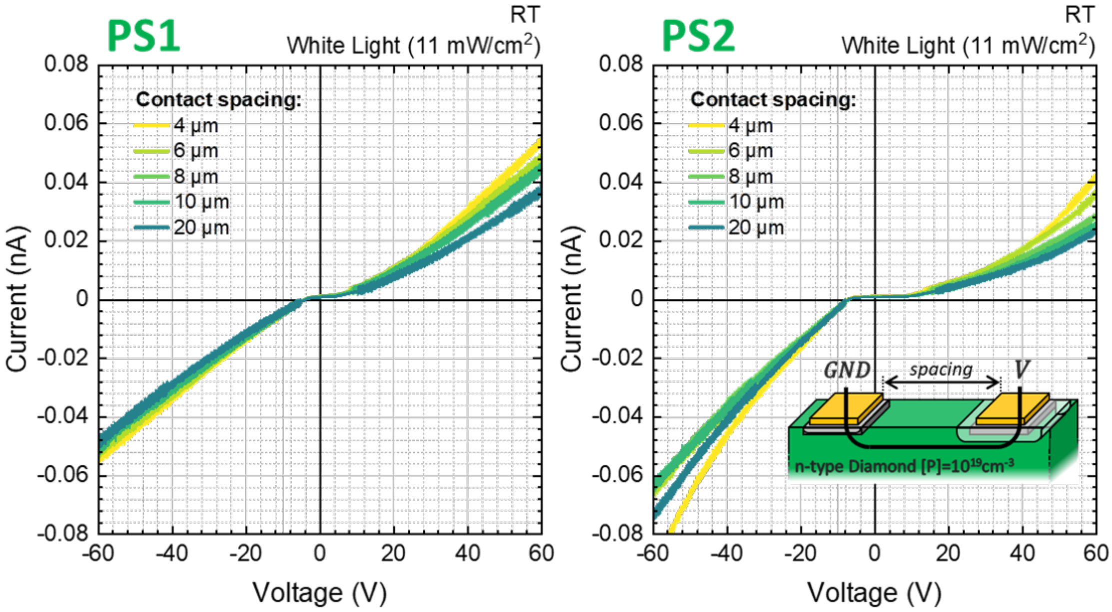

Figure III.30: Typical current-voltage I(V) characteristics between two neighboring contact pads corresponding to different contact spacings of sample PS1 (left) and PS2 (right), Ti/n-diamond contacts, measured at RT and under a white light illumination of 11 mW/cm^2.

thesis. Extraction of each inter-electrodes resistance have been performed and are discussed in the next section where a comparative study with tunneling junction seems more appropriate for the discussion.

III.6.2 Comparison with tunneling junction on Phosphorus layer

The tunneling junction presented in section III.6.2 have been fabricated on both PS1 and PS2 samples, through circular TLM architecture as depicted in Fig. II.15. While the phosphorous concentration in the n-gate layer has been called into question in the previous section, the heavily boron doped layer p++ has been demonstrated to exhibit metallic behavior, as designed, with low layer resistivity and remarkably low Ti/p++ diamond contact resistivity. Subsequently, although the phosphorous doping level is potentially not at the expected level, a comparison with and without selective p++ growth underneath the metallic contact, can still be conducted and significant enhancement could has been reached concerning the contacting properties. A comparison of the typical current-voltage I(V) characteristics measured on PS2 sample, for circular TLM using or not the tunneling junction are shown in Fig. III.31.

III.6.2.a Toward space-charge limited current regime

To avoid as much as possible the time related charging and discharging processes that can impact the non-equilibrium (enlightened) current measurements, I(V) characteristics were acquired with a low sweep rate of 10 mV/s to allow majority carriers to reach a pseudo steady-state. The log-log representation has been chosen for the I(V) characteristics as it better emphasizes that, at higher bias, the linear ohmic regime evolves toward a space-charge limited current (SCLC), whatever the presence of the p++ layer or not. The current conduction in both architecture is carried out by free carriers injected from or to the heavily boron-doped layer into the phosphorous-doped n-layer and over the junction barrier via various potential tunneling mechanism (see section II.5.1). As the injected charge increases with the voltage increase, the charge neutrality is disturbed as the injected charge carriers do not relax into the material quickly enough and, thereby, start accumulating in the n-region. This causes the current–voltage relation to transition from linear

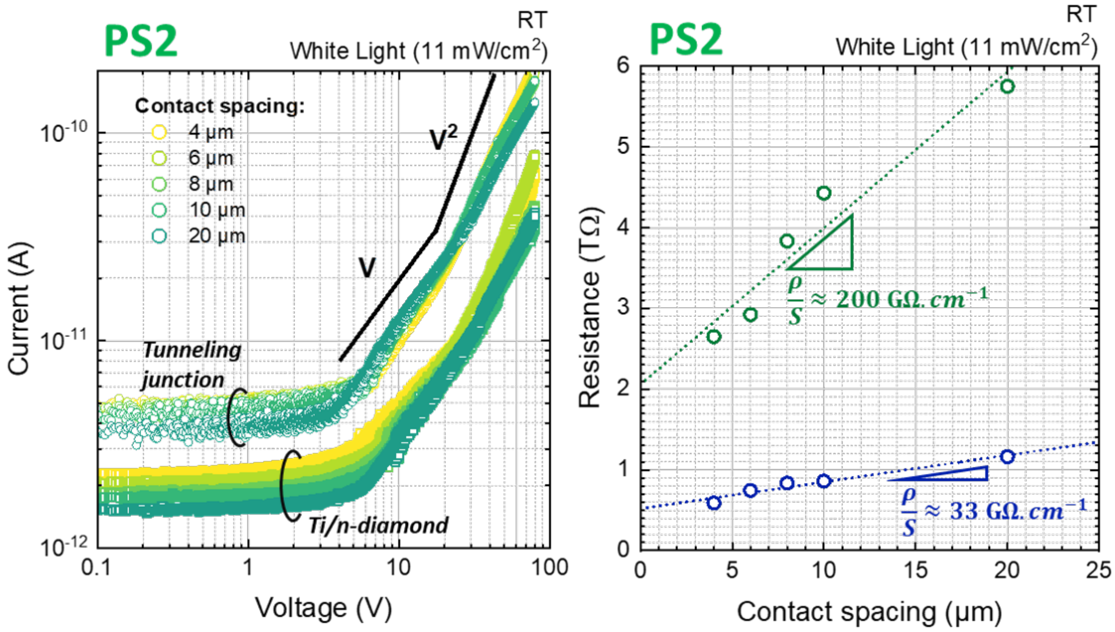

Figure III.31: Left, typical current-voltage I(V) characteristics between two neighboring contact pads corresponding to different contact spacings of sample PS2. Tunneling junction refers to Ti/p++/n-diamond contacts (open circles) whereas others refer to Ti/n-diamond contacts (open square), measured at RT and under a white light illumination of 11 mW/cm^2. Straight black lines are guide for the eyes for ohmic regime (V) and Child's law regime (V^2).Right, extracted inter-electrodes resistance as function of electrodes spacing in circular TLM configuration with (blue) and without (green) the tunneling junction configuration. Short dotted lines are least mean square fitting of the data.

ohmic conduction to SCLC regime [365].

Subsequently, the specifics of SCLC become prominent when certain traps within the material, depending on their nature and their energy level relative to the Fermi level, hinder the direct injection of carriers from the contacts [366, 367]. For charged traps among them, involving carrier repulsion at the interface and, mostly for traps located deeper within the material, a critical voltage threshold V_{th}^{SCLC} must be surpassed to overcome this repulsion and reach unimpeded carrier injection. V_{th}^{SCLC} is intrinsically dependent on the separation distance between the contacts and the traps concentration. Once the SCLC threshold voltage is exceeded, at higher voltage, the current arises from the injection of carriers at the contact, resulting in a sharp increase in current, sometimes incorrectly attributed to impact ionization [368]. Beyond V_{th}^{SCLC} and at higher voltages, the current obeys Mott-Gurney law and becomes solely dependent on free carrier mobility (μ) rather than the density of electrons (n) present in the n-layer:

$$I(V) = \frac{8q\varepsilon_{SC}\mu S}{9L^3}V^2 \tag{III.10}$$

where q is the elementary charge, S and L are the contact surface and electrode distance respectively. Noticeably, under the presence of a high trap density, the square dependence with voltage can evolve toward exponential terms, hence higher power law than the second order can be reached [366, 369].

In the present I(V) characteristics, an abrupt transition is observed in both tunneling or simple junction at threshold voltage of 25-30 V. The current tends to square dependence over the voltage but it is more or less pronounced, with a strong correlation for lower spaced contacting electrodes. Fitting performed on the I(V) curves for various distance and both architecture, using equation III.10 revealed a really poor mobility (below 0.001 cm$^2/V.s$) compared to values reported in literature for Hall mobility of highly phosphorous doped layer [169, 370]. For these calculations, as an example, it has been assumed $S = 1.33 \times 10^{-4}$ cm^2, for an electrode spacing $L = 8\mu$m. A first hypothesis, assuming band conduction, could arise from the overestimation of the conduction area under consideration, where a part of the n-layer can be depleted from the top-side of the sample due to Fermi-level pinning. Or in the same idea than the p-channel, the thickness of the phosphorus-doped layer suffered from growth issue and is distant from the ideal 400 nm targeted. While SCLC regime is linked to an electrostatic modification imposed by charges injection, it is most probable that electrons transport mechanism is ruled by hopping on localized states rather than in the conduction band. SCLC has been already observed couples of times on p-diamond Schottky diodes [365, 371], its modelization on n-diamond highly suffers from a lack of statistics.

III.6.2.b Tunneling junction favored carrier injection

Each inter-electrode resistance, estimated from the linear region in the I(V) characteristics, was plotted as a function of the contact electrode spacing L in Fig. III.31. The data show a linear relationship between d and the high resistance recorded, even if only small current variations were recorded. Assuming a contact area limited by the inner contacting electrode of the circular TLM structure ranging between 1.64-1.88$\times10^{-6}$ cm^2 the extracted resistivity of the n-layer without selective p++ growth is more than 3.5$\times10^5$ Ω.cm, at least four orders of magnitude more than state-of-the-art report [169, 195]. In this case the contact resistance of Ti/n is deduced to be around 1 TΩ, corresponding to a specific contact resistivity of 1.3$\times10^6$ Ω·cm^2, a really poor value compared to commonly admitted and expected ones. The barrier width could be insufficiently narrow for tunneling through the barrier to take place, which adds another point to the hypothesis of a lowered doping level.

However, the same analysis done on the fabricated tunneling junction with the same geometrical ratio, reports a layer resistivity of 5.4$\times10^4$ Ω.cm for similar specific contact resistivity of 10^6 Ω.cm^2. A small enhancement is however reported which tends to imply a lower contact resistivity extracted for the tunneling junction. This expected results still required to be tempered by the tremendous resistance value obtained in both architectures. Regarding the layer resistivity measured, which is close to the one measured over the whole nitrogen-containing substrate volume for reference sample GD-030 [58], the prospect of gate internal resistance lowering through the uses of phosphorous layer is seriously compromised at the current state of this development.

III.6.3 Summary

The initial current-voltage (I-V) measurements on PS1 and PS2 samples at room temperature in the dark showed almost no conductivity, raising doubts about the phosphorus-doped layer's doping level. Attempts to improve the situation with illumination and higher temperatures yielded only slight increases in current. These low current levels, coupled with cathodoluminescence (CL) results (discussed in section III.2.1), initiated discussions mirroring those related to the p-channel. Attaining effective phosphorus activation, placing it in substitutional sites within the lattice rather than interstitial sites or complexes, is a rare achievement. Most reports of room temperature conductivity under similar conditions did not require illumination, yet this work achieved conductivity under non-equilibrium conditions. The observed behavior was closer to that of a non-ideal Schottky diode, with an observable barrier at low voltages. Notably, there was almost no dependence of the I-V characteristics on contact spacing at low voltages. Under higher bias conditions, slight modulations occurred but were still in the range of a few pA, far below the microampere (µA) range reported in similar studies.

Inter-electrode resistance extraction and a comparative study with tunneling junctions (as discussed in section III.6.2) were conducted. Although, the tunneling junctions tends to exhibit a lower contact resistivity more statistical analysis would be further required to confirm this behavior. Nevertheless, even if the results are slightly better, they still require to be tempered by the tremendous resistance value obtained in both architecture. Regarding the actual layer resistivity measured, which is close to the one measured over the whole nitrogen-containing substrate volume for reference sample GD-030 [58], the prospect of gate internal resistance lowering through the uses of phosphorous layer is seriously compromised at the moment. A transition from linear ohmic conduction to space-charge limited current (SCLC) occurred as the voltage increased, with a threshold voltage of 25-30 V. The current's square dependence on voltage was more pronounced in cases with smaller electrode spacing. This behavior deviated from reports where I-V characteristics were dependent on contact spacing. However, in both scenarios, extremely high resistance values were observed. The measurements raised concerns about the ideal doping level and the possibility of reducing gate internal resistance through the phosphorus layer.

III.7 Secondary ion mass spectroscopy analysis

Electrical characterization asides with CL spectra have completely cast into doubt the doping level, compensation and layer thickness of both, the n-gate and p-channel. Subsequently, a complementary perspective was belatedly deemed necessary to status on insulating layers origins. In this regard, secondary ion mass spectrometry (SIMS) stands out as a valuable characterization tool as it gives access to the incorporated elements concentration relative to their depth in the crystal volume. While it doesn't directly reveal the doping levels due to the varied positions impurities can occupy in the lattice, when combined with other probing techniques such as CL and electrical measurements, it facilitates a detailed examination of the inner parameters of the layers.

SIMS is a powerful analytical technique mainly used in semiconductor field to determine the elemental and isotopic composition of materials. In this technique, a focused ion beam is directed onto the surface of a sample, causing the ejection of secondary ions and subsequently, punctual degradation of the observed sample. These secondary ions are then extracted and analyzed in a mass spectrometer. By measuring the mass-to-charge ratio of these ions, information about the elemental and isotopic composition of the sample can be extrapolated. SIMS offers high sensitivity, allowing for the detection of trace elements at the parts-per-billion level, such as depth profiling capabilities, allowing for the analysis of elemental distribution as a function of depth in a material. Details concerning this technique will not be provided here, for its lack of relevance regarding to the subject of this work, but detailed possibilities and characteristics offered by this technique can be found elsewhere [372]. Measurements performed by Probion are reported in Fig. III.32. Boron concentrations have been analysed thanks to oxygen ions (O^+), accelerated on the samples surfaces with impact energies of 5.5 keV. All other species, hydrogen, nitrogen, oxygen and phosphorous, have been analysed thanks to cesium ions (Cs^+) with 14.5 keV impact energies. Analysed surfaces are about 30 µm diameter and have been concentrated near the samples center, mostly around interdigited transistors. Noticeably, sounding depths were calibrated using stylus profilometry and confirmed by optical profilometry.

From the first observation, none of the four samples produced lived up to expectations and almost none of the design specifications presented in the second chapter were met, except for the heavily boron-doped layers. Following the analysis direction, from the topside of the sample, the heavily boron doped layer has been successfully realized with a doping level above the metallic transition. Their thickness lie about 200 nm as targeted which is in good agreement with contact and layer resistivity extracted. Oppositely, the boron doped p-channels exhibit higher discrepancy, especially in the concern of layer thickness. While boron concentrations are coherent with values extracted from CL, every layer grown has been reported thinner than the 400 nm targeted. For the particular case of sample PS1, over the first 150 nm from the edge of the p++ layer, the nitrogen compensation is almost an order of magnitude, at peak, higher than

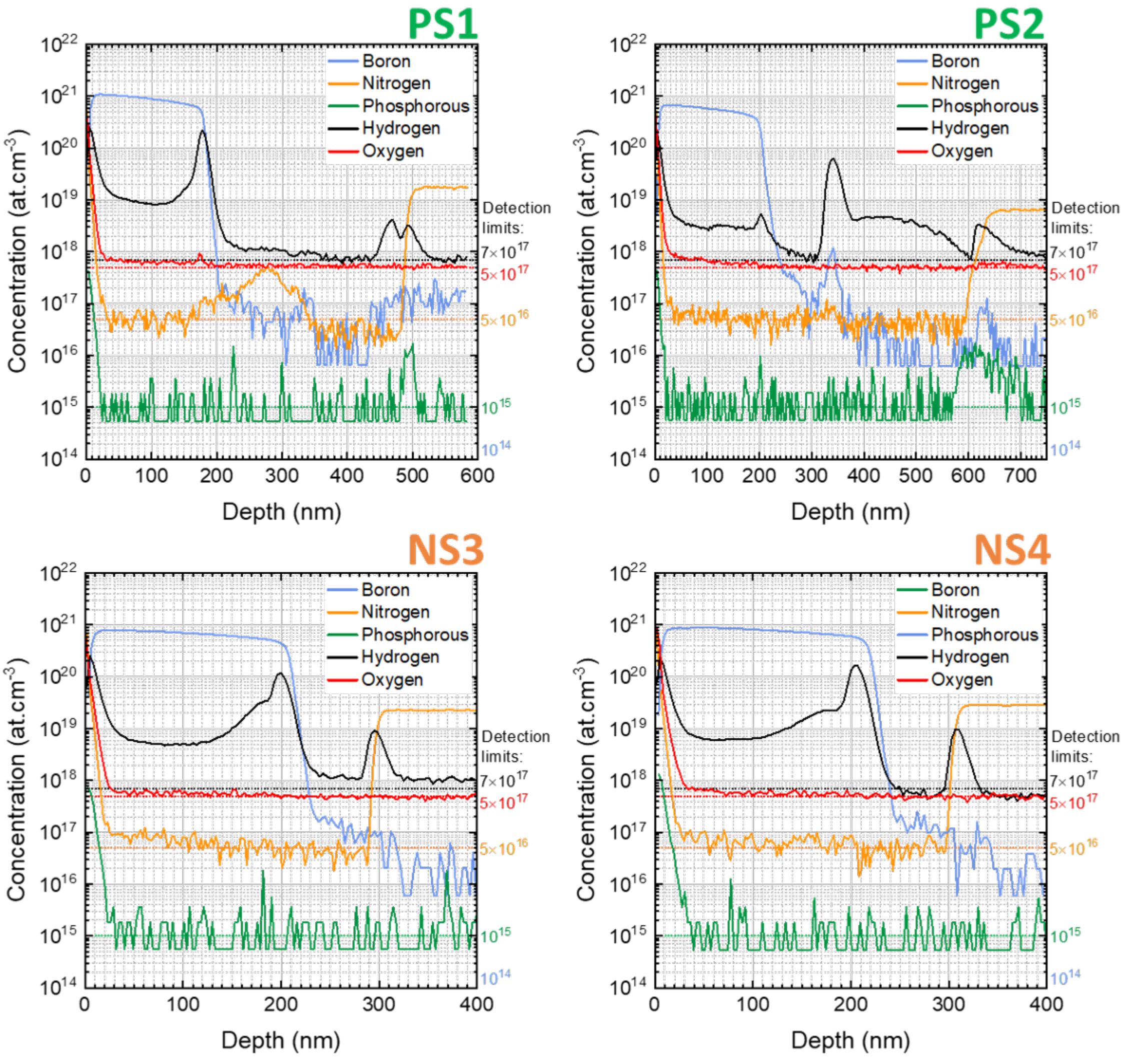

Figure III.32: SIMS depth profile of the four samples fabricated within this thesis. Detection limits are enlightened by dashed lines, with corresponding value reported aside.

the boron concentration. If we assume that nitrogen is incorporated in substitutionnal site, this part of the channel exhibits a n-type behavior (from nitrogen deep donor) with a compensation ratio due to boron of 10%. In the other case, if part of the nitrogen atoms does not form any donor-like state and boron remain the main active impurity, the tremendous remaining compensation is highly suspected to be responsible of the non-functionalization of the sample.

The same electrical non-activity reported on NS3 and NS4 sample could be easily justified by the thickness of the as-grown p-channel reported around 100 nm, hence 1/4 of the targeted value. This thinner effective conduction cross section, coupled to potential back-side (pn junction) and top-side (Fermi-level pinning) depletion layer render these samples completely OFF and unusable for transistors application. Surprisingly, PS2 sample, which featured conductivity, exhibits a doping level peak, close to the p++ contact with a nitrogen concentration below detection limit for the full device depth, except for the Ib substrate of course. Even if the boron concentration falls below 5×10^{16} cm^{-3} after the peak increase, the overall compensation is lower than for PS1 sample, justifying the functionalization difference.

The most surprising and unfortunate results are the absence of phosphorous concentration on top of the Ib substrate for both samples that should make good use of, namely PS1 and PS2. While in the former a small concentration of 10^{16} cm^{-3} is observed over 20 nm, PS2 attests of the presence of phosphorous in the samples with a small concentration going above 5×10^{15} cm^{-3}

over 100 nm. Furthermore these concentrations are in both samples observed near the junction with the substrate, but localized inside this one. These results are in good agreement with low temperature CL results, where phosphorus concentration could not be extracted because of the absence of bound exciton signature peak. Additionally, layer separations are often associated with a sudden increase in the hydrogen concentration due to the H-plasma used prior to the growth. However, in the case of PS1 and PS2, a rough separation was hard to realize considering the unresolved p-channel/phosphorous-doped gate separation. To conclude, it is important to note that the n-type contacting properties characterized in the previous section were inefficient because of the absence of a sufficient n-type phosphorous dopants in the layer.

III.8 Conclusion

Along this chapter, fabrication steps are reported aside with structural and electrical characteristics of the as-grown layer. Imaging and non-destructive electrical measurements have been carried out in a first hand, but appeared to be insufficient to status on the origins of the insulating properties of the p-channel reported on PS1, NS3 and NS4 samples. It was shown that, in relation to the different resistivity of the layers measured, the optimal layer intrinsic parameters inherent to the optimized JFET architecture, i.e. doping, compensation and film thickness, had to be questioned. SIMS analyses were carried out late in the process, after the manufacturing process had been completed, and confirmed a strong divergence in the internal layer parameters in the four samples manufactured during this thesis. Noticeably, SIMS analyses are usually and most commonly preferred earlier in the manufacturing process, after layer growth for example, as they are, by definition, destructive to the material being scanned. Coupled to the analysis technique cost, expertise it required (regarding diamond), low equipment availability, but especially its counter-productive impact regarding the etched area on the small sized substrate and the large-scale interdigited device design, SIMS analysis was not considered sooner in the fabrication process.

Comparison of CL, electrical and SIMS results demonstrate that none of the four samples met the design specifications, as depicted in Fig. III.33, except for the heavily boron-doped layers. The boron-doped p-channels have decent channel doping levels with a deviation mean around 50% of their targeted value but are way thinner than expected. These results, in good agreement with CL spectra, also justify the insulating property reported for PS1, NS3 and NS4 p-channel. Failure analyses have also been conducted for these samples but unfortunately, neither oxide encapsulation or n-side polarisation, permit to retrieve even a slight conductance or modulation of conductance. Most importantly, an unexpected absence of phosphorous concentration have been observed whereas heavily doping was targeted for PS1 and PS2. Only small rise in this concentration tends to appear near the topside of the substrate, attesting of the attempts to incorporate phosphorous. However the concentration is still below boron's one and way below nitrogen's, but can still justify the defect signature observed in CL measurements in the low energy range. However, the unsuccessful attempt to produce a phosphorus-doped layer is in no way responsible for the problems of thickness on p-channels, as confirmed by the results for NS3 and NS4 samples. Mis-alignment of the substrate as a potential responsible for these width divergence, have been investigated by X-ray diffraction (XRD) at European Synchrotron Radiation Facility (ESRF). Results are still under analysis but as first observations, the samples displayed a small mis-orientation angle (0 - 1°) which could justify a significant variation in growth rate [148].

These results emphasize the critical role of layer thickness and dopant concentrations in the functionality of the samples. As mentioned couples of times during the introduction of this manuscript, diamond is still a non-mature material compared to Si or SiC for example, and diamond-based device development is strongly coupled to our capacity to supply reliable and high quality layers. Whereas large-scale inter-digited JFET and NVPS applications will not

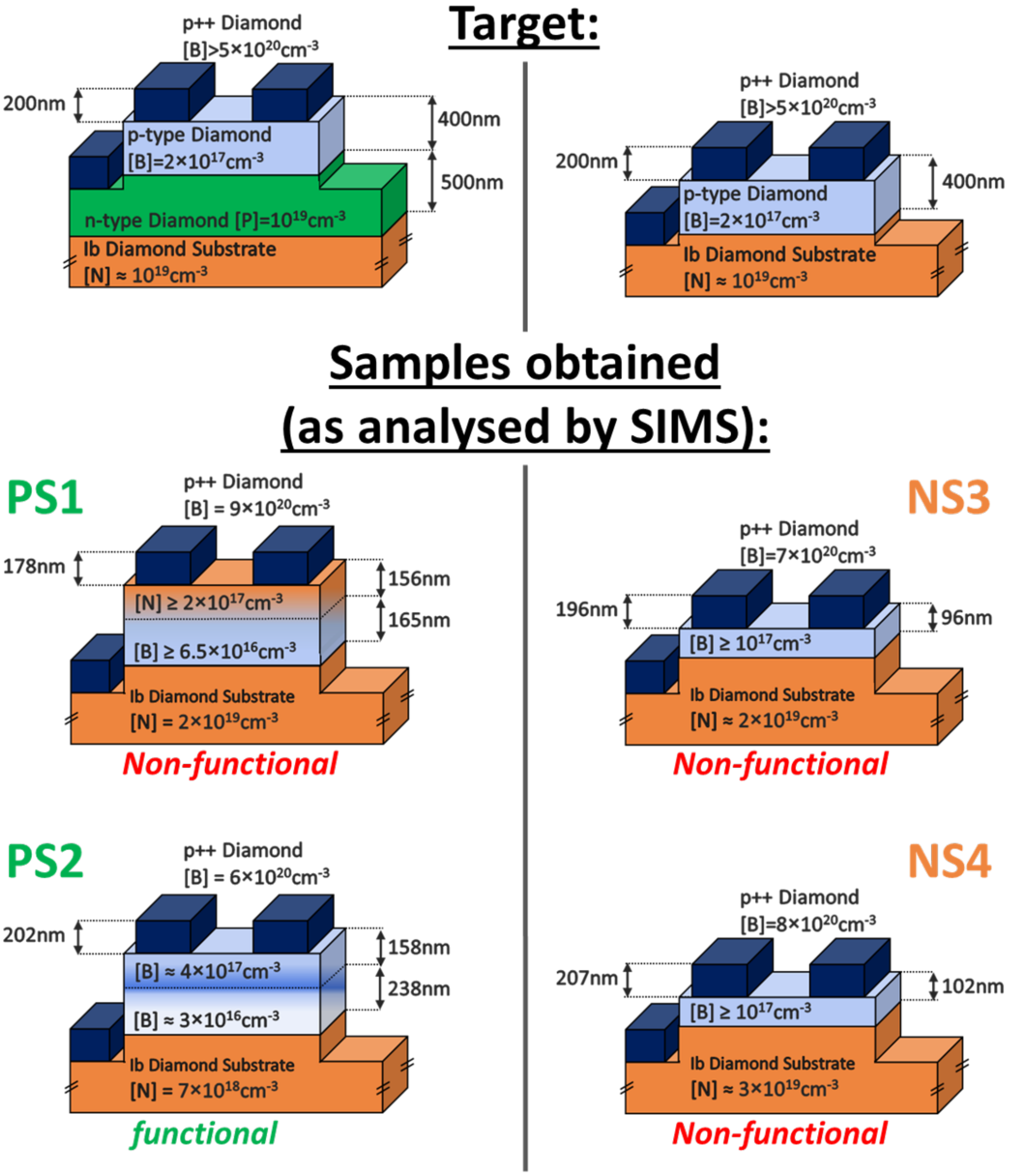

Figure III.33: Schematic cross section of the JFET fabrication design targeted (top), and the samples fabricated, according to SIMS results (bottom).

be competitive, as being far below expectations at the moment, some critical points of interest concerning PS2 sample transistors operation, have been reported and are developed in the next chapter.

Chapter IV

Diamond-based non-volatile photo-switch: memory applications

This chapter delves into the remarkable capabilities of diamond-based non-volatile photo-switches (NVPS) and their potential memory-related applications. Examination of the underlying principles, operation, and advantages of diamond-based NVPS are presented, while their robustness and capacity for high-speed operation have been enhanced, underlying promising prospects concerning their memory applications. Despite the challenges faced in fabricating functional samples within this thesis, we highlight a notable success with one of the four processed samples, PS2, which demonstrated electro-optical controllability. We also explore the benefits of gate contact closering in comparison to the reference sample, GD-030, and its potential for high-frequency switching without leakage currents or compromising device robustness.

IV.1 Gate pn junction optical control

At the basis of the innovative diamond-based NVPS, an intriguing avenue of exploration lies in harnessing the potential of gate pn junction optical control. This section unveils the mechanisms through which the application of light can allow the electrical modulation of the gate pn junctions behavior in these devices. By understanding the intricate interplay of photo-conductivity and photo-activation, deeper insight is brought on how this optical control is harnessed to achieve high-speed and robust non-volatile memory functionalities in the fabricated JFET. Thus, the next section will delve deeper into the core operational principles of the electro-optically controlled pn junction. A particular attention is paid to the difference between backside (GD-030) and/or frontside (PS2) gate configuration as depicted in Fig. IV.1.

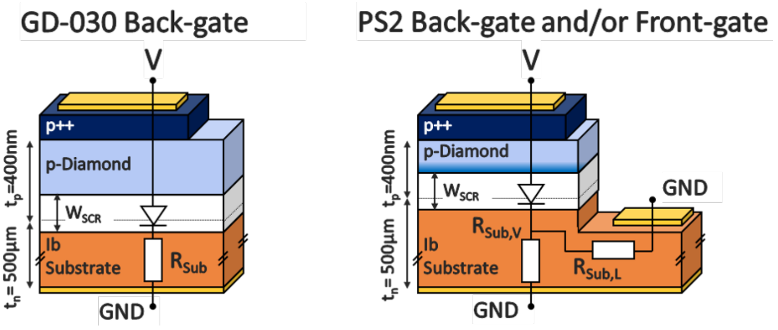

Figure IV.1: Schematic representation of GD-030 (left) and PS2 (right) gate pn diode. Back side of the substrate is contacted with silver paste

IV.1.1 Working principle

IV.1.1.a Kinetically limited dynamics

A schematic representation of the band diagram of the abrupt pn junction and fixed charge concentration are shown in Fig. IV.2, at equilibrium and under reverse bias V_{Bias}. Nitrogen is taken as n-type dopant to illustrate the operation principle, regarding the low phosphorous concentration reported in the previous chapter. However, the discussion below is expected to work for phosphorous also, with higher light collection efficiency, hence better dynamics.

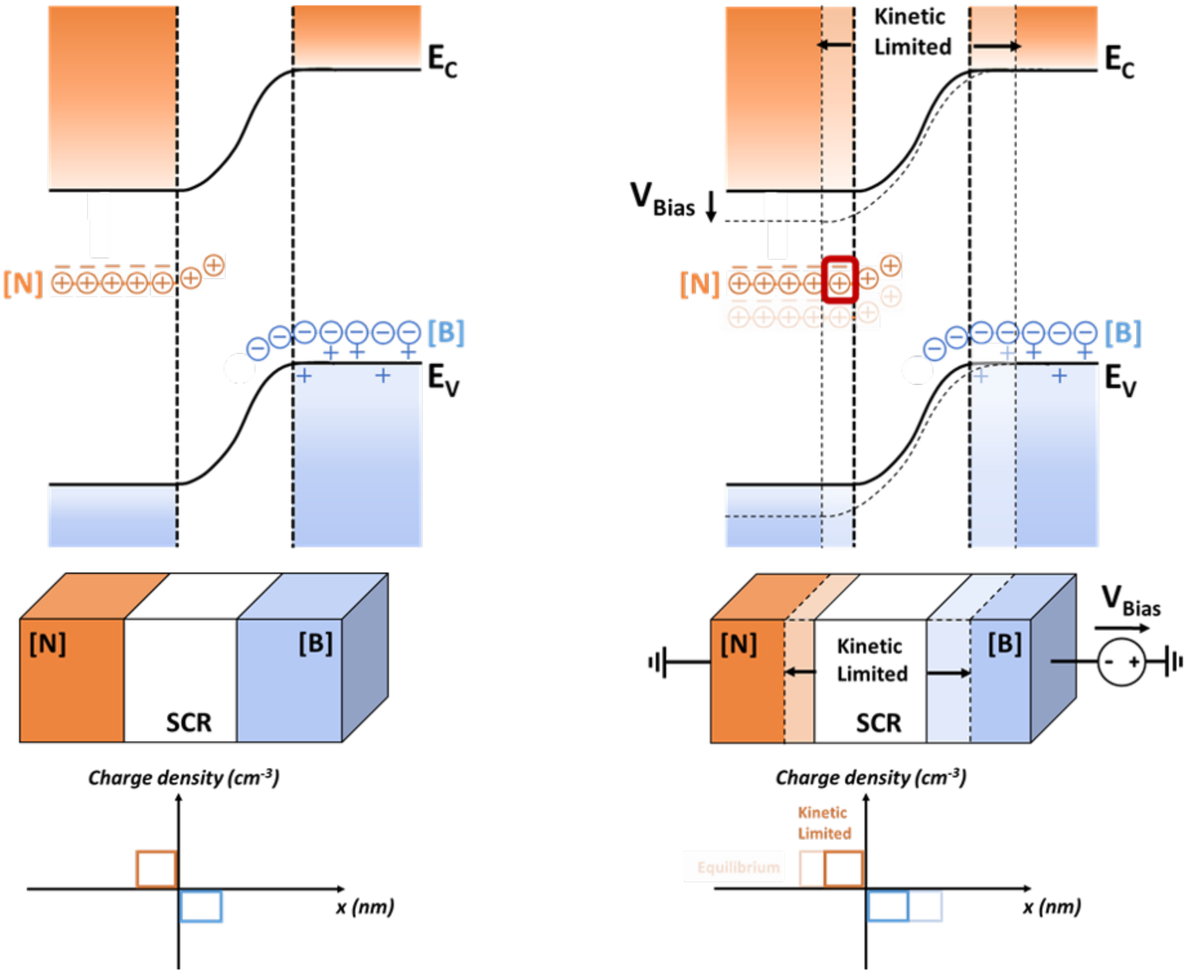

Figure IV.2: Schematic representation of band diagram, structure and fixed charge density of an abrupt boron-doped/nitrogen-doped diamond pn junction under: (left) equilibrium and (right) reverse bias, at room temperature and in the dark.

At thermal equilibrium, juxtaposition of p-type and n-type semiconductor results in the formation of a homojunction and a space-charge region SCR, by definition empty of either free electrons or holes. Within this SCR, only fixed charges remain which are in this case, positively charge fixed nitrogen atoms in the n-side and negatively charged boron atoms in the p-side. Without light, in the dark, when this junction is biased in reverse, e.g. negative bias applied on the p-side, no space charge modulation is observed. In common pn junction under the same conditions, like silicon-based one in full ionization regime thanks to shallower donor and acceptor, the SCR is extended. Whereas, in a diamond-based pn junction due to the depth of the dopant, no SCR depth modulation is possible due to charge conservation inside the SCR. To respond to the reverse polarisation, bulk nitrogen dopants located near the edge of the SCR needs to become ionized. While boron dopants are partially ionized at room temperature, extension of the SCR in the p-side is possible but the variation in positive fixed charge number needs to be in agreement with the oppositely charged ones. Subsequently, by charge conservation, the extension of the SCR is totally limited by the non ionization of nitrogen dopant near the edge of the SCR. In terms of timing, achievement of an equilibrium state corresponding to the polarisation applied is kinetically limited as, randomly distributed event like cosmic rays, can induce nitrogen ionization, hence restore SCR modulation.

This non-controllability of the diamond-based pn junction under packaged device condition (low temperature in the dark) can however be seen in the framework of this thesis as half of the proof of non-volatility. This electrical non-operability of the device without external energy application forms the basis of an inactive state, where whatever the polarisation applied the SCR extension is not changed.

IV.1.1.b Illumination switch

A second state, when the device is active or when the SCR extension can be modulated normally by varying the biasing condition, is obtained when an external energy is imposed to the system such as appropriate light or temperature. At room temperature due to the Boltzmann's statistical distribution of thermal energy, some electrons can still acquire the nitrogen thermal ionization energy of [94], even if it's higher than the average thermal energy at room temperature. So, even though nitrogen is a deep donor, there's still a non-zero probability of finding electrons in the conduction band at room temperature, and this probability becomes greater as the temperature rises. Considering this huge thermal energy scale, optical activation between 1.7 and 2.2 eV [95, 97] is easier to reach, especially thanks to the use of visible light. Such light activation of the pn junction controllability is schematized in Fig. IV.3.

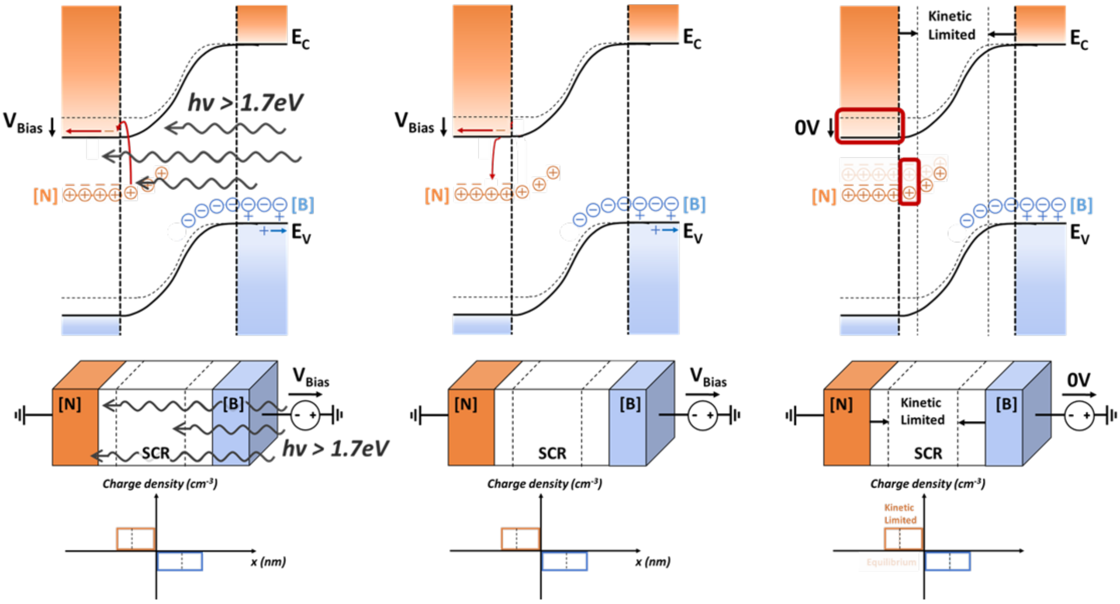

Figure IV.3: Schematic representation of band diagram, structure and fixed charge density of an abrupt boron-doped/nitrogen-doped diamond pn junction at RT, under: (left) reverse bias and illumination, (center) reverse bias in the dark, imaging the transitional state induced by light switch-off, and (right) zero bias in the dark.

While under its freeze state, the junction does not respond to the reverse biasing condition under the dark (Fig. IV.2), illuminations efficiently ionizes the neutral nitrogen dopant fixed near the edge of the SCR, hence extension of the later is possible (Fig. IV.3 left). Electrons absorb the energy of photons and so raise from the localised deep nitrogen donor state to the conduction band and further drift in the n-layer over a distance related to their lifetime [373], toward the cathode. The retrieving of freeze state, from active state, is achieved by first, removing of illumination and secondly changes of polarisation. When enlightenment is removed, electrons in the conduction band of nitrogen doped diamond either recombine with a fixed nitrogen donor in the bulk or drift along the electric field. Subsequently, n-side diamond recover its insulating property and return devoid of free electrons, hence the junction goes back in its freeze state. Every further voltage changes, or even removing, in this state, does not imply any SCR thickness modulation. Lack of conduction band electron prevents the ionized nitrogen in the SCR, near the edge, to be compensated and so the charge conservation to be changed. Again, a kinetic limitation is imposed by the negligible nitrogen ionization rate at RT.

In the model proposed here, the external illumination activates or freezes the junction. In this sense, the latter can be driven by a combination of electrical and optical signals, providing a higher degree of freedom. It forms the basis of NVPS working principle, as contacts can be deposited on the p-side of the junction in order to fabricate JFET that are electro-optically controlled. Memory application is brought by the addressable freeze and active state.

IV.1.2 Light activation and photo-conductivity

Light-activated pn junction concept has to be distinguished from photo-conductivity, even if both are linked through the SCR thickness management. Photo-conductivity is enlightened for both samples PS2 and GD-030 in Fig. IV.4 where irradiance modulation of a white light beam has been compared to the resistance modulation implied in the nitrogen doped layer.

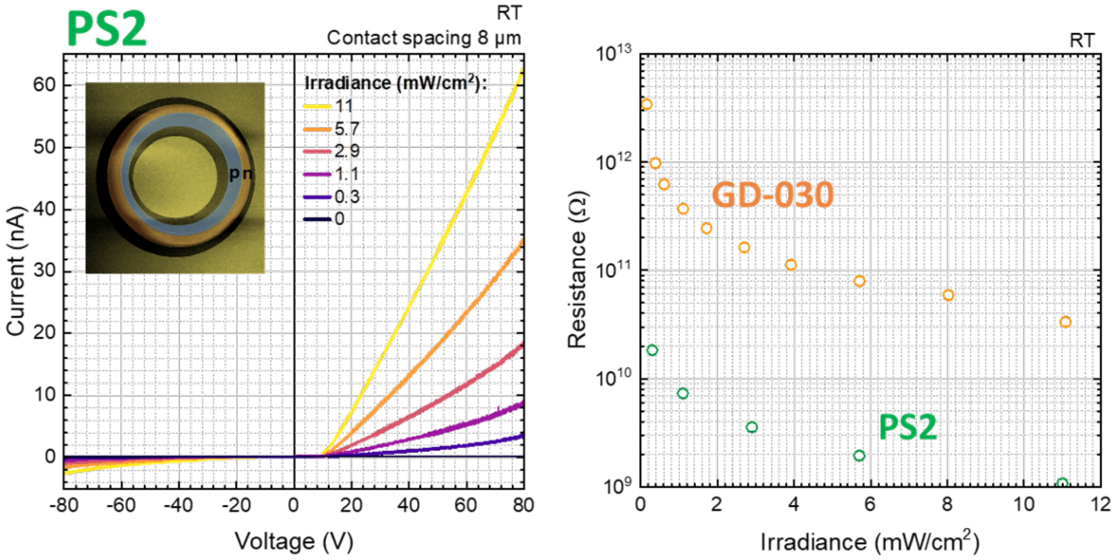

Figure IV.4: Left, current-voltage characteristic, I(V), measured under different irradiances for PS2 samples. Image of the lateral pn junction is reported in the inset (recolored) and the dark current is reported below the detection limit (<0.1 pA). Right, comparison of RT extracted layer resistance as function of the irradiance, for both PS2 with front-gate and GD-030 with back-gate (see Fig. IV.1).

Extrinsic photo-conductivity is necessary implied in the process imaged in Fig. IV.3 where it ensures evacuation of the free electrons photo-generated. While photo-conductivity could enhance on-state performances in the particular bipolar mode operation of the designed large-scale devices [228], its impact has been reported relatively low on boron dopants used in the p-channel. This is only considering extrinsic photo-conductivity, i.e. for boron $E_A < E_{ph} < E_G$ (with E_{ph} the photon energy), but it seems important to note that in the case of intrinsic photo-conductivity (creation of electron-hole pairs at $E_{ph} > E_G$) absorption is very high, and so is free carrier photo-generation. While band-to-band absorption (intrinsic photo-conductivity) is privileged in diamond based photo-detector, that have already proven their efficiency for deep UV detection [374, 375], this regime is avoided in this work as irradiances with energies lower than the diamond bandgap are used. Subsequently photo-conductivity does not significantly participate to the p-channel conductivity during the diverse NVPS operations, and regarding its ionization ratio (1/1000), photo-ionization of boron atom is considered negligible.

The added switchable state in the pn-junction has to be distinguished from photo-conductive semiconductor switch devices [242] which have also been demonstrated to use nitrogen-doped diamonds [243]. Most optically generated carriers participate in conduction which means these devices strongly benefits from the use of a high power pulsed laser source. For example, the device reported in [243] makes use of a pulsed laser with pulse power of about 6.7 kW (the average power is 25 mW). A power range far away from one used in Fig. IV.4, where measurements have been performed using the adjustable white light (LEICA CLS 150 LED) of the microscope. Additionally, it is important to notice that the irradiance values were determined thanks to a photo-diode, but this method only gives a mean value of the light spot power density, which is not homogeneous. Nevertheless, high power range is demonstrated to not actually being the main limiting factor for NVPS application.

IV.1.2.a Light power density impact

Extrinsic photo-conductivity mechanism, is strongly enhanced by light power density rising as for a fixed photon energy, hence a fixed optical capture cross section, their flux and density is increased, implying a higher interaction probability with non-ionized nitrogen donors. This mechanism is however less efficient than intrinsic photo-conductivity as only a fraction of the incident power is generating carriers, due to the dispersion of nitrogen atoms in the lattice, i.e. $[N]/[C] \approx 10^{-4}$. For the highest irradiance reached of 11 mW/cm^2, the photo-generated carrier density was estimated to be in the order of 10^8 cm^{-3} for reference sample GD-030 [58]. This small concentration was deduced using mobility and incomplete ionization models (see section I.2.2.e), being compared to with the same resistivity value obtained in the dark by heating up the sample. The validity of this modelization can be questioned, but no similar study concerning nitrogen doped diamond has been reported. However, reference sample GD-030 exhibits resistance ranging between 0.03 to 3 TΩ, corresponding to the crossing of the substrate vertically, whereas PS2 sample displayed resistance varying from 1 GΩ to 20 GΩ, thanks to the use of the front-gate contact.

Furthermore, regarding the thickness of the metal deposition, hence non-transparent electrodes, illumination do not reach the semiconductor underneath all contacts available in the structure. Then, irradiation tuning is considered to not influence the Ti/n metal interface properties, especially the barrier height in the diode behavior reported in section III.6.1. It further comforts that the internal gate resistance is limited by the poor layer activation and not dominated by any contact resistance modulation. Moreover, the opaque metallic contacts strongly limit the light exposure of the active region of the diodes. Therefore, generated carrier densities of at least four orders of magnitude higher than the one deduced here could be obtained with a higher irradiance and semi-transparent contacts.

IV.1.2.b Light energy dependence

Owing to diamond's significant indirect band gap, the intrinsic photo-conductivity would typically necessitate photons with wavelengths shorter than 225 nm. However, in measurments performed previously (Fig. IV.4), the white light source used emits photons outside the UV range. Consequently, the observed photoelectric effect can solely be attributed to extrinsic photo-conductivity, mainly related with nitrogen donors. In contrast to intrinsic photo-conductivity where both electron-hole pairs are generated, extrinsic photo-conductivity produces only one type of carrier, namely electrons. Although boron impurities present in the stacked layers are also ionized during illumination, their concentration is negligible compared to the nitrogen density available in the substrate region. As demonstrated in Section IV.1.1.b, boron ionization is not the limiting factor for conductivity inside the pn junction. To evidence the role of nitrogen in extrinsic photo-conductivity, current has been acquired as function of the photon wavelength trough a dedicated setup presented in the same Fig. IV.5.

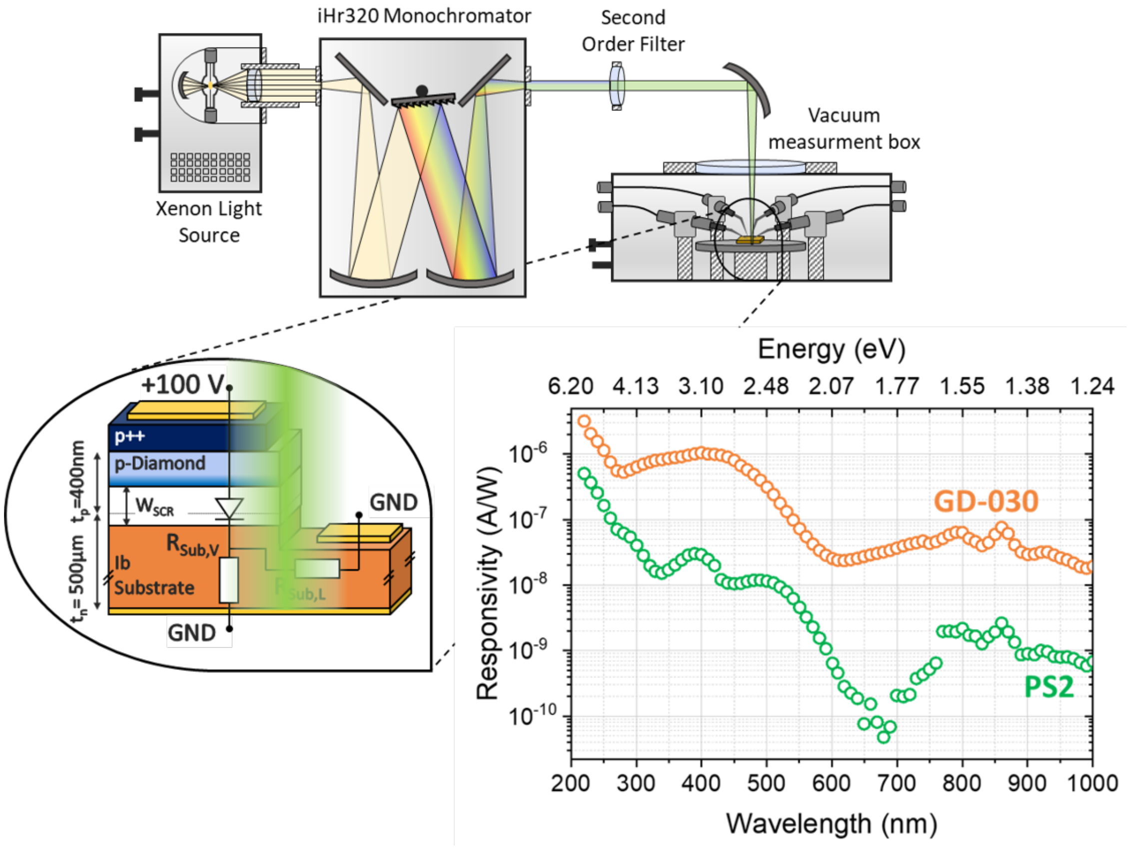

Figure IV.5: Schematic representation of the illumination setup where poly-chromatic light is filtered in a monochromator, prior its injection inside a vacuum and temperature controlled probe station. Graph, responsivity (current measured normalised by the source power density) as function of the irradiation wavelength on both PS2 and GD-030 sample, biased in forward (+100 V).

While illumination source is provided by a Newport 1000W, UV enhanced, Xenon Lamp, monochromatic light is obtained thanks to an Horiba iHR 320 monochromator allowing a light band-with through the whole setup between 200 nm (6.2 eV) and 2000 nm (0.62 eV). Light is then focused inside a probe station thanks to wavelength adapted optical fibers, and monochromatic signals are always filtered before injection to avoid second diffraction order transmission. Both samples have been maintained under vacuum, strongly polarized in forward (+ 100 V) and light energy sweep is operated, starting from lowest energy toward the highest. It is important to notice that spectra have been acquired in separated windows and reconstructed afterward to optimize filters cascade and optical fiber transmittance range.

The vertical (GD-030) or pseudo-vertical (PS2) pn junction responsivity increases in respect to the illumination wavelength decrease. Starting around 600 nm, it aligns with the ionization energy of nitrogen donors, which is estimated to fall within the range of 1.7 eV [94, 239] to 2.2 eV [95, 334]. The previous value reported for reference sample GD-030 was 1.45 eV [58], which was lower than commonly reported values, hence was questioned in respect to its extraction method. Nevertheless nitrogen optical activation is observed in both samples, and variations in photo-current is increased at higher illumination energy as supported by the increasing of the optical capture cross section of substitutional nitrogen in respect to irradiation energy increase [334, 376].

Added to the photo-conductivity, pn junction activation is also suggested in the current vs. irradiation energy reported in Fig. IV.5. As forward biasing condition have been constantly maintained and illumination energy raised from 1.24 eV to 6.2 eV, forward current raising is obtained by a combination of photo-conductivity and SCR modulation. This particular point of interest is better underlined in section IV.1.2.b where the same protocol is used on JFET commutation cycles.

IV.2 Quasi-static transistor characteristics toward larger active area

IV.2.1 Quasi-static regime, impact of the drain to source voltage sweep rate

Before going forward inside the transistor characteristics, it is important to specify the non-equilibrium conditions implied by the need of photo-activation on the transistor. The pn junctions formed on both samples PS2 and GD-030, between the p-channel and the substrate exhibits very high resistance. Attempts in modulating the SCR with a n-side biasing without illumination, have been shown to be kinetically limited, hence would take a considerable amount of time to reach equilibrium. However, light significantly reduces this time constant, hence allow effective modulation of the SCR or also modulation of the capacitance of the SCR. Further observations, presented in the next sections, correlated this time-related variation to the RC time constant that emerges from the SCR capacitance C_{SCR} and the n-layer resistivity R_n (as being the highest). To illustrate, considering a SCR with a 100 nm width and a typical substrate resistivity of 0.3 GΩ·cm, either under light exposure or at 250°C, the calculated time constant falls around 0.7 seconds. Results with different geometry and external conditions, generally displayed time constants spanning seconds to minutes, rendering almost impossible the achievement of a true quasi-static condition. However, an approach to these conditions involves experimenting with different sweep rates for the drain to source voltage (V_{DS}), as supported by Fig. IV.6.

In the conditions of our measurements at RT, the n-side gate (or substrate) such as the source, are shorted and grounded, hence the backside pn junction is solely activated by light. The depletion layer from the topside of the sample, due to Fermi level pinning near the surface, has ever been observed to be influenced by any kind of illumination. Further investigation in this concern could be achieved by capacitance-voltage measurements, photo-induced current transient spectroscopy (PICTS), or optical deep level transient spectroscopy (O-DLTS), but will still be hard to achieve regarding the large volume required to enhance capacitance signal and the potential contamination of the results from surface state and layer defects. In this regard the SCR width due to surface pinning is further considered constant, reported around 50 nm for reference sample GD-030 [58] and considered with a safety margin of 50-100 nm for PS2 sample. Since the modulation of the backside SCR is time-dependent, through its correlation to RC equivalent model, a slower sweep rate of V_{DS} results in a broader SCR, reducing the drain current. This aligns with the observations reported in Fig. IV.6, where the fastest sweep rate of 20 V/s leads to a significantly higher maximum drain current at $V_{DS} = -40$ V, whereas slower sweep rates tend to converge toward an I(V) characteristic that approximates the quasi-static regime. Notably, the 0.2 V/s and 2 V/s characteristics are nearly identical and similar behavior is observed for both samples. Consequently, to avoid current density overestimation, reported here up to 30 - 50%, all subsequent measurements have been conducted using a sweep rate of 0.2 V/s. The latter ensures better reproducibility but significantly impact the characterization time, where output characteristics $I_D(V_{DS})$ from 0 to 40 V, with different gate voltages, can last more than 30 min.

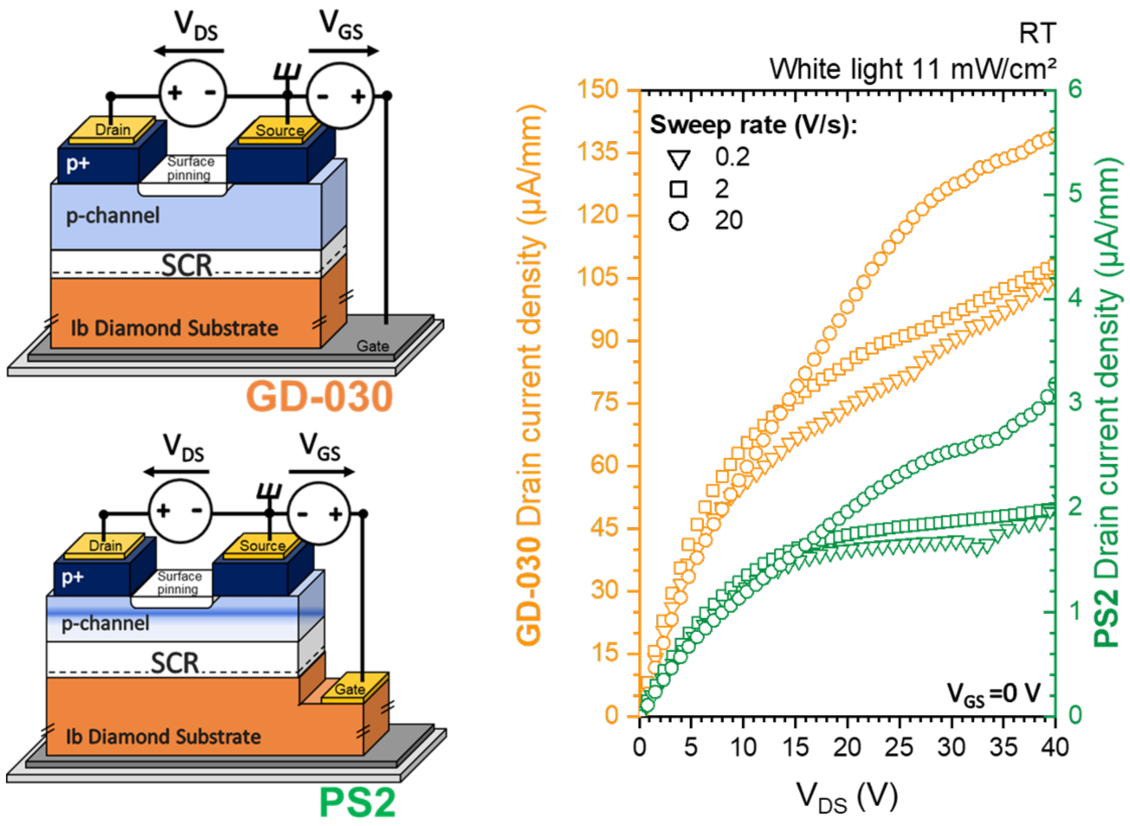

Figure IV.6: PS2 and GD-030 samples drain current density as function of drain to source voltage (V_{DS}) for different sweep rates. The measurement was performed at 250 °C under a 11 mW/cm^2 white light irradiance, ensuring 0 V biasing between gate and source.

IV.2.2 Activated JFET electrical characteristics

IV.2.2.a Transistor output and transfer characteristics

The two fabricated samples exhibit clear transistor effect as demonstrated in Fig.IV.7(d) and (g), where the channel conductance can be modulated in order to switch ON or OFF the device.

Firstly, during the JFET ON-state, in the linear region, the drain-to-source voltage V_{DS} regulates and controls the drain current flow I_D following regular Ohm's law. With absence of gate-to-source V_{GS} biasing or for $V_{GS} < V_{th}$, further augmentation of V_{DS} causes the JFET to transition into the pinch-off regime. Subsequent rise in V_{DS}, creates an increase to the gate-to-drain biasing V_{GD}, compared to the unchanged source-to-drain biasing V_{GS}. This non-fair modulation, implies stronger reverse polarisation for V_{GD} when compared to V_{GS}, thus the p-channel/n-gate junction SCR underneath the drain contact undergoes significant extension, while no change is implied underneath the source contact. The SCR morphology, depicted in Fig. IV.7 (b), forces the effective conduction cross section of the p-channel to narrow underneath the drain, ultimately resulting in crowding of the carrier flow. In this regime, the trade-off between current elevation due to V_{DS} augmentation and resistance decrease in the pinched region due to geometrical aspect ratio lowering, reach a perfect balance. Subsequently, I_D enters inside a saturation regime, where the JFET operates near its maximum current capacity, and any additional amplification of V_{DS} have no beneficial effect on the current density.

Secondly, by adjusting the gate-to-source voltage V_{GS}, the channel effective conduction cross section is modulated by the SCR extension, hence the current density in saturation regime can be controlled. Ultimately, for high gate voltage such as $V_{GS} \geq V_{th}$ the off state is reached (Fig. IV.7 (c)), when the p-channel is completely pinched by the SCR extension, in such a way that

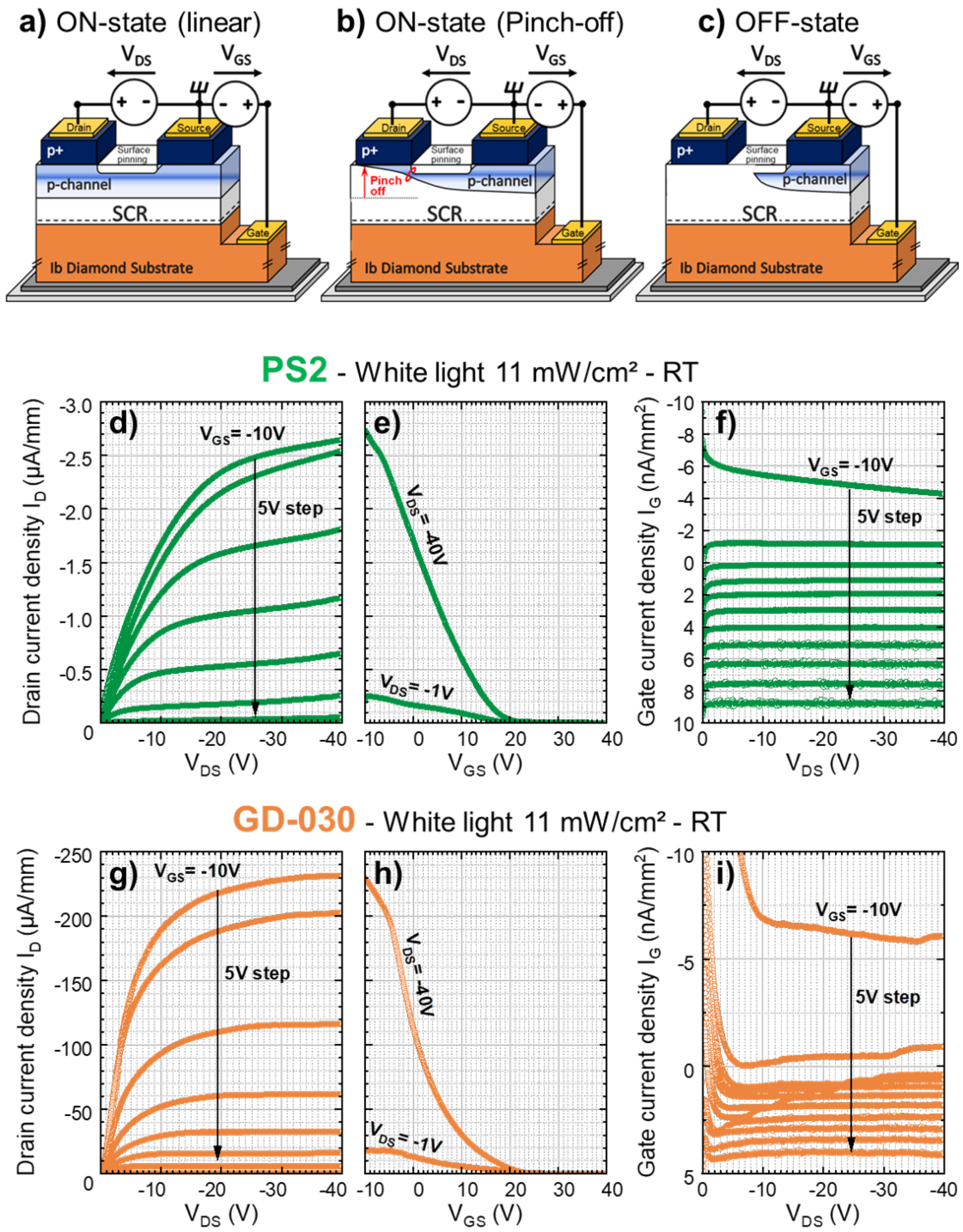

Figure IV.7: Schematic cross section of PS2 sample in: ***a)*** *ON-state at low V_{DS} (linear regime),* ***b)*** *at high V_{DS} (pinch-off regime) and* ***e)*** *in OFF-state. same regime are observed for GD-030 sample and schematized operation can be found elsewhere [241].* ***d)*** *PS2 and* ***g)*** *GD-030, quasi-static RT transistor characteristic, drain current versus drain-to-source voltage, measured for gate voltages varying from -10 V to +40 V with 5 V steps and continuous 11 mW/cm^2 optical power density.* ***f)*** *PS2 and* ***i)*** *GD-030, gate current density I_G measured at the same time are presented as function of V_{DS} for the same V_{GS} variations.* ***e)*** *PS2 and* ***h)*** *GD-030, transfer characteristics ($I_D(V_{GS})$) for $V_{DS} = -40V$ in saturation regime and $V_{DS} = -1V$ in the linear regime.*

no conductive path exists within the p-channel. Additionally, in an ideal situation, the SCR extension is sufficiently wide to block any leakage tunneling current mechanism that could cause carrier to cross the SCR, giving birth to power loss in the OFF-state.

It is important to notice here that these characteristics were obtained under white light illumination, with optical power density of 11 mW.cm^{-2}, to keep the NVPS in it's active state and thus, enabling the modulation of the channel conductivity. The threshold voltage observed for both samples is around 20 V as it can be observed on the transfer characteristics represented in Fig.IV.7(c) and (f). For higher gate voltages, the transistors remain in their OFF state and a leakage current in the order of few $nA.mm^{-2}$ is observed for both samples as witnessed by Fig. IV.7 (f) and (i). One can remark that, even if the gate contact is made on the top face of sample PS2, in fact closer to the active area of the JFET, the measured leakage current is not higher than the one measured for reference sample GD-030, although the current line ranges through the width of the whole substrate. In fact different results could have been expected by the addition of highly phosphorous-doped layer, but regarding the present incorporation and/or activation ratio, gate contact of sample PS2 can be considered to have been fabricated on the substrate topside surface (refer to section III.7 for more details). Concerning the drain current density reached at the saturation, the difference of two orders of magnitude between the two samples is also explained by the higher compensation, boron doping level vs. channel depth in-homogeneity, and lower layer thickness in PS2 sample as summarized in the previous chapters.

IV.2.2.b Gate biasing and SCR modulations

To have a better quantitative insight in the p-channel conductivity modulation offered by the n-gate polarisation, the JFET transfer characteristics, $I_D(V_{GS})$, plotted in Fig. IV.7 have been used to compute the SCR extension as function of the gate polarisation as reported in Fig.IV.8.

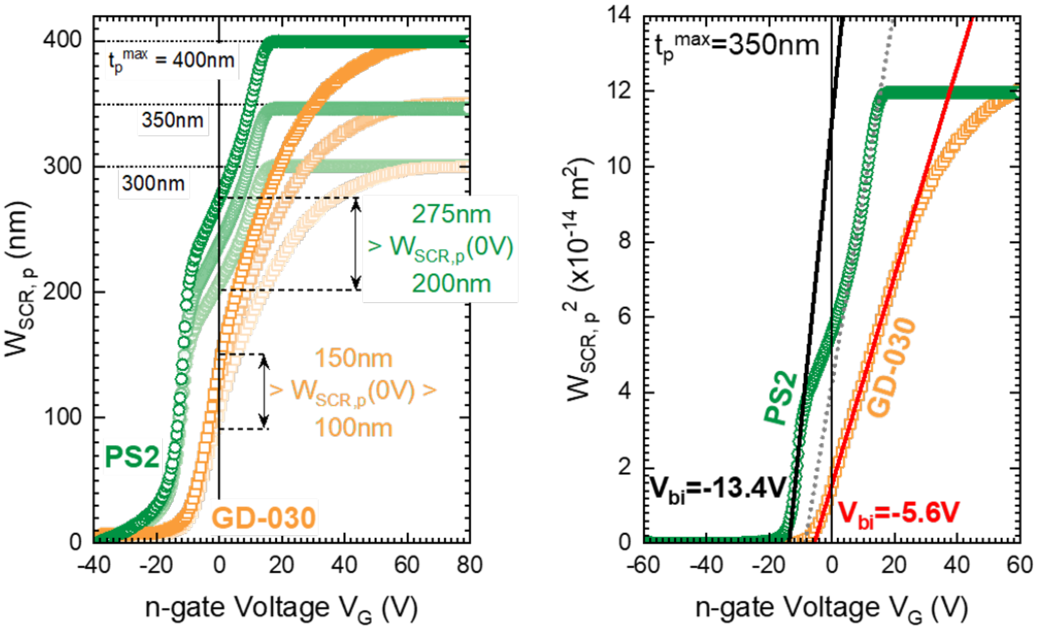

Figure IV.8: PS2 and GD-030 extracted p-channel SCR depletion width $W_{SCR,p}$ (left) and $W_{SCR,p}^2$ (right) as function of the n-gate voltage V_G, considering various p-channel thickness t_p among 400 nm as targeted, 350 and 300 nm as channel thickness limited by pinned surface induced depletion layer. $W_{SCR,p}^2$ has only been represented considering a median value of $t_p =$ 350 nm, close to the depletion reported from the pinned surface on GD-030 sample.

Low constant drain-to-source bias of -1 V has been used to ensure $V_{DS} \ll V_{GS}$, in order to be able to consider the SCR extension in the p-channel $W_{SCR,p}$ to be uniform within the whole channel depth t_p. Measurements have been performed at RT with a white light irradiance of 11 mW/cm^2 to ensure active state and V_{GS} has been swept from -60V to +80V with a sweep rate of 0.2 V/s (measurement time of 11min 40s). The drain-to-source current I_{DS} modulation is directly linked to the p-channel effective thickness variation, as $t_{ch} = t_p - W_{SCR,p}$. Considering the fixed $V_{DS} = -1$ V, the drain-to-source current can be approximated through the Ohm's law as:

$$I_{DS}(-1V) = -\frac{W_D \cdot (t_p - W_{SCR,p})}{\rho_p \cdot L_{SD}} \text{ in } (A/cm^2) \tag{IV.1}$$

Where, W_D and L_{SD} are the drain width and the drain to source electrodes spacing respectively. Making the assumption that the drain current saturation arise for negative gate bias, when $W_{SCR,p} = 0$ nm, linked to a maximum value I_D^{max}, then the SCR extension is given by:

$$W_{SCR,p} = t_p \cdot (1 - \frac{I_D}{I_D^{max}}) \tag{IV.2}$$

The variation of $W_{SCR,p}$ modelized through eq. IV.2 are represented in Fig. IV.8 for both reference sample GD-030 and PS2, considering various p-channel thickness. As previously reported on GD-030 and further considered for PS2 samples, the channel thickness is limited by a depleted layer arising from surface Fermi-level pinning. As a precise value of this depletion could not be extracted from PS2 sample due to the impossibility to perform impedance measurements (too high n-layer serial resistance), a maximum p-channel/n-gate junction SCR extension of 350 or 300 nm have been preferentially considered. However, for ease of comparison, the originally targeted thickness of the ideal p-channel, set at 400 nm, has also been included.

The variation of W_{SCR} for GD-030 sample is in good agreement with a square root dependence regarding V_G as planned by eq. II.11 or:

$$W_{SCR,p}^2 = \frac{2\varepsilon_0\varepsilon_{Diam}}{qN_A}(V_G - V_{bi}) \tag{IV.3}$$

A SCR extension, under equilibrium ($V_G = 0$ V), ranging between 100 nm and 150 nm is reported for GD-030 with a median value taken a 125 nm for a channel width of 350 nm. These results are in good agreement with the pn-junction modelisation proposed in section II.3.1.a for a doping level juxtaposition of $N_A = 2 \times 10^{17}$ cm^{-3} and $N_D = 10^{19}$ cm^{-3}, ultimately giving rise to a zero bias channel depletion of almost 35%.

Oppositely, in the case of PS2 sample, this ratio is pushed forward, up to 68% of the channel is depleted without bias application on the gate electrode. This high difference is however in pretty good agreement with the doping level variation inside the p-channel reported by SIMS analysis. Supported by the steep change around -10 V, in the expected single square root dependence of $W_{SCR,p}(V_G)$, the extraction of a doping level gradient in the p-channel enlightened. The doping level of $N_A = 1 - 2 \times 10^{16}$ cm^{-3} extracted from SIMS in the first 250 nm of the p-channel are in good agreement with a full depletion of this specific part at 0 bias. Additionally, increase in V_G in positive polarisation, results in a slower $W_{SCR,p}$ extensions than in the reverse polarisation direction, due to the higher doping level of the p-channel in the last 150 nm of the layer.

Those observations are furthermore supported by the combination of the linear fits performed in Fig. IV.8 and eq. IV.3. While below -6 V, a built-in potential V_{bi} of -13.4 V and a doping level of $N_A = 4.2 \times 10^{16}$ cm^{-3} is extracted, for gate voltages between 0 and 20 V, $V_{bi} = -8$ V and $N_A \approx 10^{17}$ cm^{-3} are reported. A p-channel doping level in the order of few 10^{16} cm^{-3} is in good agreement with a built-in voltage higher than 10 V (see eq. II.5), whereas the increase in doping level, around 10^{16} cm^{-3}, near the topside edge of the p-channel, is in good adequation with a built in voltage around 5-6 V, as reported for GD-030 sample with $N_A = 2.2 \times 10^{17}$ cm^{-3} and $V_{bi} = -5.6$ V.

As a direct consequence of the doping level gradient in the p-channel, the gate electrostatics control of the transistor is remarkably affected, but this appears to be a slight disturbance compared to resistivity dramatical decrease.

IV.2.3 Interdigited JFET

As a crucial part of this thesis work, the implementation of large-scale device, specifically interdigited transistor architecture, is enlighten in Fig. IV.9. A comparison is held between a single fingered JFET, with rectangular shape involving a drain width W_D of 80 μm and an interdigited JFET with a total drain width of 2 mm.

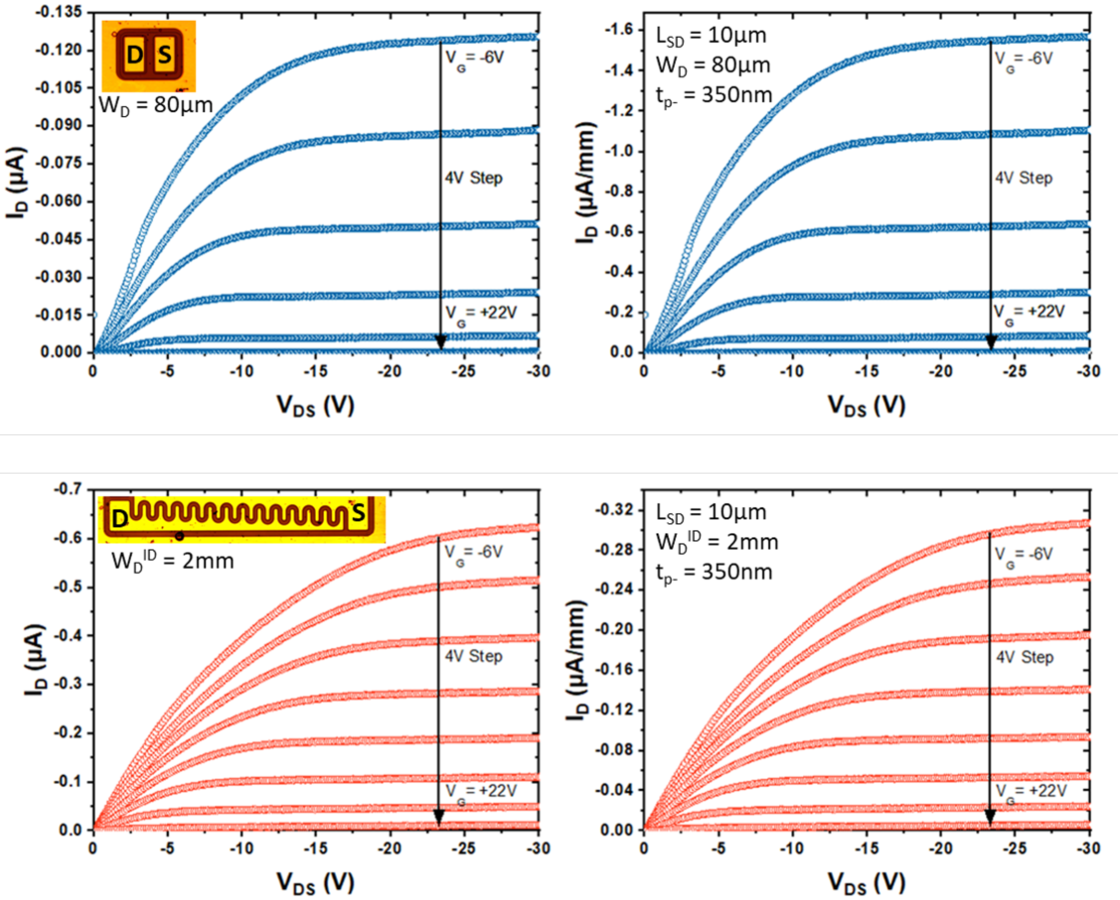

Figure IV.9: RT comparison of the drain current (left) and drain current density (right) as function of drain-to-source bias V_{DS} for a single, rectangular-shaped, JFET with $W_D = 80$ μm (top) and an interdigited JFET with $W_D = 2$ mm. Drain-to-source spacing L_{SD} of 10 μm and a layer thickness of 350 nm is used for both structure to ensure a comparison based on drain width only.

An identical drain-to-source spacing L_{SD} of 10 μm is used to ensure a comparison solely based on drain total width, subsequently assuming a constant layer thickness over the whole active area of 350 nm. Unfortunately, compared to the single fingered architecture, the current recorded in the interdigited one is only multiplied by 5 whereas the total drain width has been increased by a factor 25. The expected linear, correlation between drain current and the geometrical aspect ratio of the source-to-drain exchanging surface, is not observed for the only functional sample fabricated in during this thesis. This consequent difference compared to the initial target can be further explained by high volumic and surfacic non-homogeneities underneath the interdigited-shaped drain and source electrodes. The latter is further supported by the slighter increase of the resistivity in linear ON-state regime of the interdigited structure compared to the single-fingered one. Although the doping levels have been demonstrated to be inhomogeneous across the entire sample surface (see Fig. III.9), no CL spectra have been recorded at different points of the same interdigited device. Further measurements are needed to assess this possibility, especially mapping along the conduction channel should be under consideration. Furthermore, it is worth noting that the results obtained concerning the p-channel internal parameters being far from targeted ones, could have a significant impact in the poor yield obtained here. Premature breakdown of the transistors has also been observed during characterization of the devices, with a maximum voltage around 80 V for a drain-to-source spacing of 10 μm. Results are not shown here as they occur randomly during other non-dedicated characterization and dedicated study have been chosen to not be held regarding the destructive character of breakdown and the further analysis that still need to be done on the sample. The low breakdown field however reported from these observations, way below 1 MV/cm, is significantly far from the initial expectations of at least 600 V. It has been assumed that this limited voltage sustaining capabilities were strongly affected by the presence of impurities at the edge of the drain and source contacts, causing electric field crowding in these regions. This result, rising the same conclusion as low conductivity extracted, needs to be completed with EBIC characterization in order to visualize the potential current or electric field crowding zone at the edges of the interdigited contacts.

However, these results align with and complement the work initiated by Umezawa et al. [121]. They add the current yield of an augmentation of the current density regarding the number of active cell juxtaposition or the lengthening of the drain contact for lateral transistor devices. Even if the structure presented here proposes a poor linearity regarding the geometrical aspect ratio increase, it paves the way to initiate diamond-based device upscalling. As the yield of device functionnalization depends mainly on the growth and fabrication process quality, whatever the device design, large-scale device architecture must be attempted more in the future. At least dedicated area must be kept during the mask conception to make new attempts concerning interdigited transistors. While ON-state resistance of the power electronics oriented transistors are a major concern, its optimization should not be done to the detriment of other parameters like the commutation frequency, as more detailed in the next sections.

IV.3 Transistor dynamics

Interdigited transistors were demonstrated to be a good alternative to small-sized devices for a conduction losses reduction purpose, even if the design proposed reached a efficiency yield between 20 and 30% regarding the targeted active area up-scaling. However, while the focus in this modeling has primarily been on conduction losses, the trade-off between conduction and switching losses concerning the device's active area has been overlooked. To illustrate this critical trade-off, where diamond is expected to outperform other semiconductors in power management and equivalent losses, consider that diamond can operate up to five times faster than SiC, with a passive device volume reduced by a factor of three to five [61]. Subsequently, optimizing only the R_{ON} vs. BV trade-off for diamond based device is of paramount importance, but it must not be done at the expense of optimizing component switching frequency.

With this objective in mind, the NVPS concept introduced in GD-030 sample showed a need for improvement in switching speed to fully exploit the potential of this innovative device. While the phosphorous layer was not successfully achieved, moving the gate contact closer to the active area, as done on PS2 sample, demonstrated a notable reduction in switching time, showing promise for the device's future prospects. This timing reduction is presented along this section with a particular attention to the illumination dependence of the device. A larger active area usually leads to higher switching losses caused by an higher capacitance to charge and/or discharge during switching, also meaning a longer switching time and more energy required for state transitions. Accounting this trade-off, smaller active area device (rectangular shaped JFET) has been preferred in the following characterizations.

IV.3.1 Light dependency of JFET commutation cycles

The study conducted previously in the concern of the pn junction light activation (see section IV.1.2) have been further expanded to the working operation of JFET ON-OFF switching cycles. The commutations cycles are reported in Fig. IV.10, which provides an initial insight on the dependence of the JFET commutation time, especially the time to turn-OFF or respectively turn-ON the device, regarding the illumination power density and energy. Only results obtained from GD-030 reference samples are depicted here for representation purpose, as same overlapping results have been observed for PS2 sample.

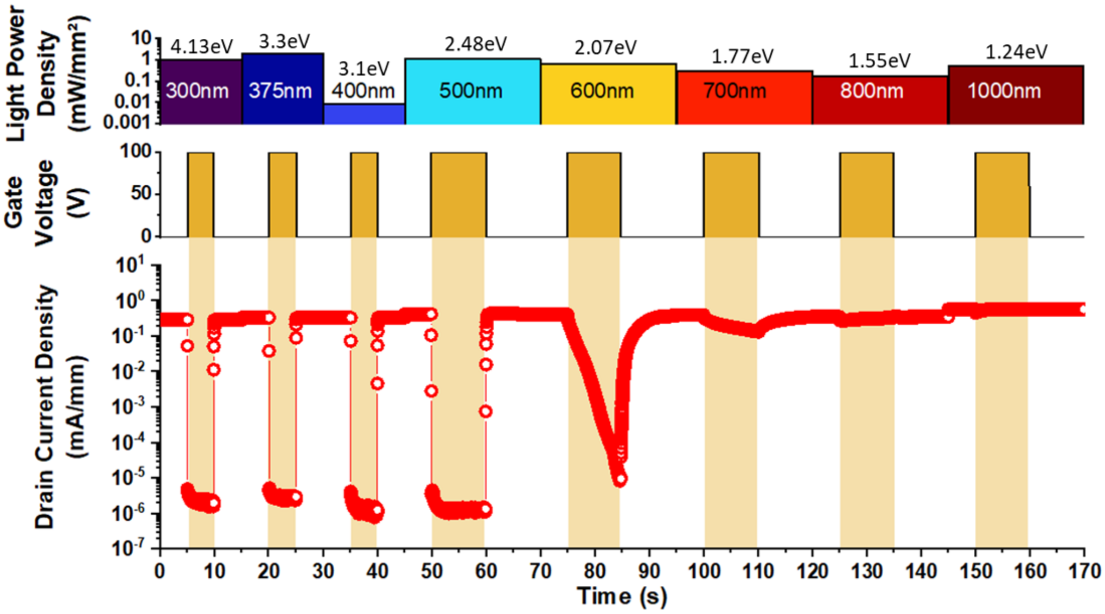

Figure IV.10: Sample GD-030, RT drain current density as function of time where drain-to-source bias of -40 V has been maintained and gate voltage pulses of +100 V on the n-gate were used to effectively control the p-channel conductance under various illumination conditions. Gate pulse of 5 s have been used for low wavelength as the commutation was faster than the drain current sampling rate of 50 ms, while pulse of 10 s were necessary at lower illumination energy. Cycles have been recorded separately and juxtaposed and color bar have been chosen to enlighten the maximum accessible power density range at each energy of the experimental setup.

The sample have been maintained under constant illumination along the whole measurement duration, to ensure the active state of the transistor, but the wavelength and the light power density received by the active area of the JFET from the top face (schematized in Fig. IV.11), is tuned. It is important to notice that, the light power density calibration has been measured on the top face of the sample. Due to thick metallic covering, a part of the light applied can be reflected or absorbed by the drain, source and gate metal contacts and thus lower the effective power density absorbed by the n-type diamond near the SCR.

Measurements have been performed at RT, where ON-state current of 0.25 mA/mm is obtained for $V_{DS} = -40$ V and OFF-state current are assumed to be in the order of 10^{-6} mA/mm. In good agreement with previous observations concerning the pn junction, commutation of the transistor state from ON to OFF or vice versa, is provided by a n-gate polarisation of +100 V under illumination energy higher than nitrogen ionization energy (1.7 eV). As both fabricated transistors are normally-ON thus, by application of $V_{GS} = +100$ V and thanks to photo-ionization of deep donor dopants, the conduction channel closes, namely the drain current fall down. Below 1.7 eV illumination energy the conductance of the p-channel is no more affected by the n-gate biasing, and no turning-OFF of the device is reported. However for illumination energy higher than 1.7 eV, closing and re-opening of the channel are observed with characteristic time constant varying with the illumination energy. The turning-OFF and turning-ON time during a single commutation cycle tends to be in the same order of the 50 ms sampling rate used for the drain current at illumination energy higher than the nitrogen optical ionization energy (2.2 eV). However, between 2.2 eV and 1.7 eV, both thermal and optical nitrogen ionization energy, the p-channel closering and re-opening is not recorded as steep as it this for UV illumination. While for UV illumination energy a single exponential decrease fit could have been performed, showing a single time constant dependency tentatively attributed to nitrogen ionization, at 600 nm illumination wavelength a double exponential decrease was at least necessary to describe the closing time of the p-channel. Origin of this double time constant is most probably inherent to various optical transition, assisted with phonons, that occur with different efficiency depending on the optical pumping energy.

Even if supplementary analysis could be done around this illumination energy to provide a better understanding of the fundamental process involved, it is not mandatory for switching performance enhancement of the device, as UV illumination are obviously more efficient. To provide a deeper quantitative analysis of this capability, the closing and opening time of the p-channel, defined in the next section, are more accurately measured in the following.

IV.3.2 Optically activated JFET commutation time

IV.3.2.a Falling and rising time compared to turn-OFF and turn-ON time

Generally dynamic performances of a commercially available transistor refers to two characteristic time constant of the device, namely the turn-off/on time and fall/rise time. Even if they are fundamentally related, they however describes slightly different aspects of a transistor's switching behavior. Turn-off time specifically refers to the time it takes for the transistor to switch from the conducting ON-state to the blocking OFF-state. It measures how fast a transistor can stop conducting current and effectively "turn off", thus encompass all time-related physical process from the application of a gate bias until the p-channel absence of conductivity. Fall time, on the other hand, is a broader term that, applied for transistors, describes the time it takes for drain current to transition from a high level (usually 90% of its ON-state value) to a lower level (usually below 10% of the ON-state current).

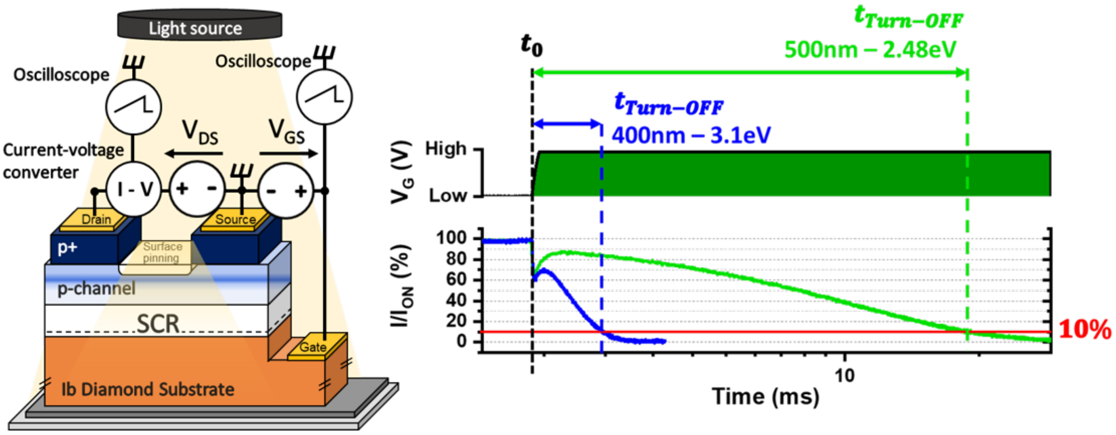

Figure IV.11: PS2, drain current normalized by its ON-state value and gate to source voltage as function of time, for different irradiance energies, and power densities. Definition of turn-OFF time stamps are enlightened for 400 and 500 nm wavelength.

To summarize this difference, the turn-ON/OFF delay is how long it takes from changing the gate voltage input until the current output starts to be modulated, whereas the rise/fall time is how long it takes to observe efficient current modulation, once it started to be modulated. In the NVPS proof of concept presented in this work both time constants are optimized for more mature devices and needs to be redefined for a first analysis approach. In this purpose, Fig. IV.11 illustrates the experimental setup used, aside with drain current transient reported on PS2 sample, where definition of turn-OFF time is imaged.

The time needed to shut OFF the device is in the following referenced as $t_{turn-OFF}$, but is redefined by the absolute difference between two timestamp: when the gate voltage is applied and V_G becomes different from 0, and when the drain current goes below 10% of its ON-state value, as imaged in Fig. IV.11. The experimental setup also enlighten the oscilloscope transient analysis that is triggered by gate voltage bias application and drain current transient analysis after being converted in a current-voltage converter. This setup further allow drain current transient record for different illumination conditions e.g. light power density and/or energy. Similarly the time required to turn-ON the device is defined by the absolute time difference when the gate voltage is removed (any change from the OFF-state voltage applied) and when the drain current goes above 90% of its ON-state value. The gate voltage settling time, as function of the voltage range used, is guaranteed by the manufacturer (Tektronix - Keithley) to be lower than 700μs, even if experimental results showed rising time from 0 to +60 V around 100 μs. This imply that the $t_{turn-OFF}$ and $t_{turn-ON}$ time reported above this value can be decorrelated from the gate voltage slew rate. These $t_{turn-OFF}$ and $t_{turn-ON}$ parameters have been chosen in order to take into account the different mechanism, like wavelength dependant charge trapping or detrapping [377], that occur during the transistor switch and can cause misestimation of both commutation time.

IV.3.2.b JFET turn-OFF/ON time vs. wavelength and optical power density

The turn-OFF and turn-ON time recorded for both, reference sample GD-030 and PS2 are plotted in Fig. IV.12 as function of the light power density and for illumination energy higher than nitrogen ionization energy in respect to previous observations (see section IV.3.1).

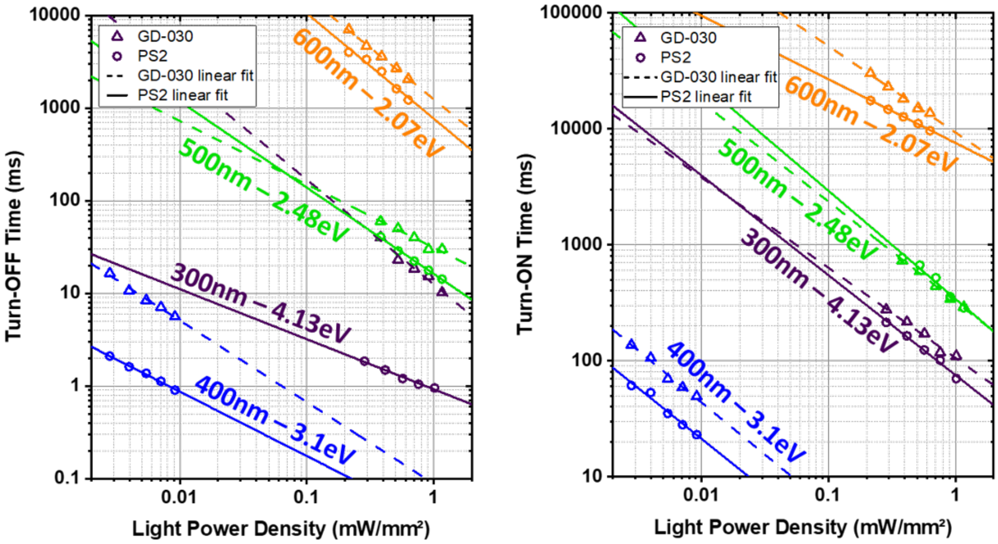

Figure IV.12: Turn-OFF (left) and Turn-ON (right) time for both GD-030 and PS2 samples as function of the illumination power density for different wavelengths. Open round markers and open triangle markers stand for PS2 and GD-030 respectively, measured data point, whereas solid (PS2) and dashed (GD-030) lines are linear fits for each wavelength value.

A photon wavelength ranging from 300 nm (4.13 eV) to 600 nm (2.07 eV) has been chosen to ensure the photo-generation of free majority carriers in the n-type region for both samples. The excess photo-generated electrons are thus responsible of the turn-ON or turn-OFF time lowering, as the illumination energy rise and/or the light power density rise, an highest quantity of free electrons is generated from their fixed donor states due to the increase of the optical capture cross section [376]. Especially, according to the work of W. Enckevort et al. [334], the optical absorption cross section of the nitrogen impurity in Ib diamond rises from, 0.1 a.u. (arbitrary unit due to normalisation with IR absorption coefficient) at 2 eV photon energy, to 5 a.u. at 4.15 eV photon energy. As both turn-ON and -OFF time dependence over the light power density, for each wavelength reported tends to follow a linear dependency, an equivalent resistor-capacitor (RC) circuit with a typical time constant τ [378] is tentatively proposed to justify the observed behavior:

$$\begin{aligned}\tau \approx R_{SUB} \cdot C_{SCR} &= \frac{\rho_n \cdot t_n}{S} \times \left| \frac{dQ_{SCR}}{dV_{GS}} \right| \\ &= \frac{t_n \cdot \epsilon_0 \epsilon_{Diam}}{e \cdot \mu_n \cdot (n_0 + \Delta n_{photo-generated}) \cdot W_{SCR}}\end{aligned} \quad \text{(IV.4)}$$

With R_{SUB} the substrate resistance which can be reduced as a product between the resistivity of the substrate ρ_n and a geometrical ratio t_n/S where t_n is the thickness of the n-type layer and S the surface of the p-type mesa structure formed on top of the n-type layer. C_{SCR} is the SCR capacitance formed at the interface of the pn junction, which is deduced by the derivative of the total charge localised in the SCR, Q_{SCR}, as function of the gate voltage applied V_{GS}. Finally, e is the elementary charge, μ_n is the electron mobility in Ib diamond substrate, ϵ_0, and ϵ_{Diam} the vacuum permittivity and the diamond permittivity respectively, W_{SCR} the SCR width and $(n_0 + \Delta n_{photo-generated})$ the free electron present at equilibrium n_0 plus the density of electron ionized by illumination $\Delta n_{photo-generated}$.

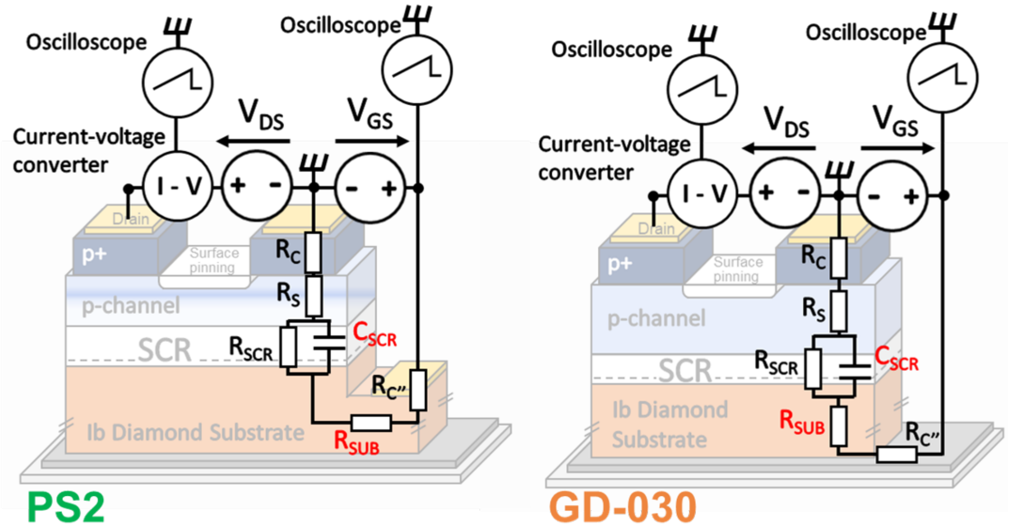

Figure IV.13: Schematic cross-sectional view of PS2 (left) and GD-030 (right) samples, with equivalent resistor-capacitor (RC) circuit modelisation proposed for the gate-to-source pn junction.

A schematized electronic circuit modeling the system is presented in Fig. IV.13 where resistance and capacitance participating in this pn junction model are enlighten. An increase of free carrier in the n-type diamond is assumed to not affect, or negligibly the electron mobility. The decrease due to ionised impurity scattering [370] is not observed, because the number of free electron that can be generated thanks to illumination $\Delta n_{photo-generated} \approx 10^{11}$ cm^{-3} for white light irradiance of 11 mW.cm^{-2}, should be negligible. Added to the fact that at room temperature and in the dark, the density of free electron being close to zero, one assume that $(n_0 + \Delta n_{photo-generated}) \approx \Delta n_{photo-generated}$. Furthermore, considering the constant illumination imposed to the structure and an electron generation only due to nitrogen photo-ionization, the carrier density $\Delta n_{photo-generated}$ is given by the product of electrons lifetime τ_e and their generation rate g, such as $\Delta n_{photo-generated} = \tau_e \cdot g$ [379]. Additionally, the proportionality between the generation rate and the optical capture cross section of single nitrogen impurity ($g(h\nu) \propto \sigma_e^{opt}(h\nu)$) [380], rules the dependence of the highest density of photo-generated carrier in respect to the illumination energy rises.

The gate contact closering in sample PS2 exhibits, in mean value (e.g. for every wavelength studied), four times lower turn-OFF time, for the same irradiance, than GD-030 sample where substrate backside contacting has been used. This benefit directly induced by the lower gate layer resistance is unfortunately less impactive for the turning-ON time of the transistor. It subsists a trade-off, when the capacitance C_{SCR} is decreasing, the n-type layer resistance R_{SUB} is increasing, added to the active area ratio of both transistor being almost equivalent, assumption is made that this leads to closer turning-ON time. Even if it is important to note that the gate contact closering provide a lower turning-ON time.

IV.3.3 Impact of the absorption depth of the light, toward optimized geometry

The turning-ON and -OFF time is reported higher for 300 nm (4.13 eV) irradiation than for 400 nm (3.1 eV), whereas higher ionization efficiency was expected in respect to illumination energy increase. In fact, more generally, the time lowering with energy rising is not respected for wavelength lower than 400 nm (3.1eV). For reference sample GD-030, this observation could be linked to transmittance sudden fall through the whole substrate at this energy. As depicted in Fig. IV.14, the transmittance fall lies in good agreement with the RC equivalent circuit modelisation proposed in the previous section.

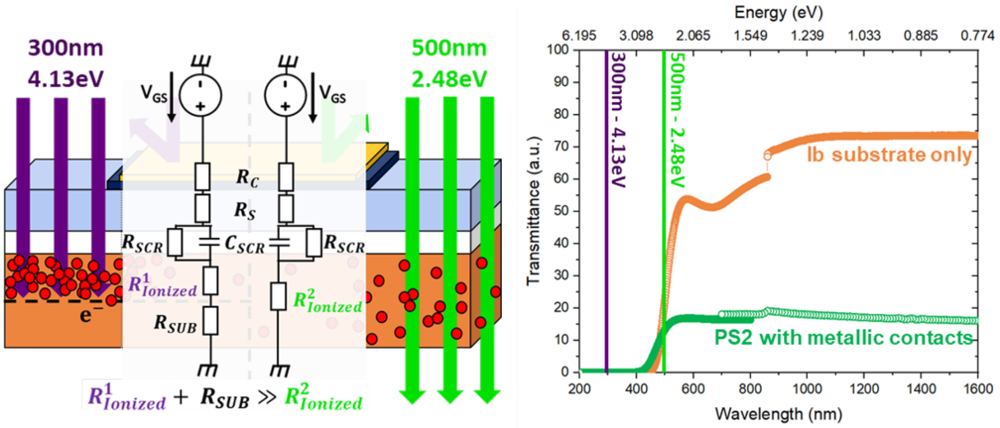

Figure IV.14: Left, schematic cross sectional view of GD-030, where gate-to-source electrical equivalent RC circuit have been superimposed for two different illumination energy. Right, UV-Visible transmittance spectra of PS2 sample at the end of the fabrication process compared to an "as-received" Ib HPHT diamond substrate. The strong absorption of PS2 sample causing the saturation at 20% transmittance is caused by the high sample frontside metallic coverage.

Using equation IV.4, the substrate resistance R_{SUB} of GD-030 sample is proposed to be decomposed in two distinct terms. In one hand the upper part of the substrate with a lower resistivity due to photo-ionisation and in an second hand the lower part of the substrate which is not illuminate anymore and therefore highly resistive (in the range GΩ). It ultimately leads to a rise in the turn-OFF and turn-ON time measured even if the light energy is more efficient for optical ionisation.

However in the case of PS2 sample, where the gate contact is made on the topside of the sample, hence considered less sensitive to volumic photo-ionization in the substrate, the same behavior has been reported. The hypothesis made in the concern of GD-030 does not seems to be sufficient to explain the same behavior observed in the case of PS2, or other mechanisms need to be involved. Most probably, considering that the model discussed herein-above is valid, a coupling still exists between the substrate's bulk and the upper part of the latter, near the top-side surface. Reason for this coupling need more investigations, especially pulsed light transient like photo-induced transient spectroscopy (PICTS) could bring complementary information regarding this behavior. Measurements where the Ib substrate on the backside of PS2 sample was biased with the same value as the gate-to-source voltage were performed, with the idea to avoid depolarisation effect that can lower the gate voltage application at the edge of the pn-junction. Unfortunately only a significant difference was recorded, hence no more conclusion could be drawn in this regard.

To give a partial conclusion on the dynamic of the optically activated JFET, the gate contact closering to the active area successfully lowered the turn-OFF and -ON, almost by a mean factor 4. For future device designs, prioritizing the optimization of light collection efficiency is crucial, even if it leads to an increase in conduction losses. This might occur due to a non-optimized design for the p-channel (including contacts), with n-gate light collection efficiency taking precedence over the p-channel's conduction losses. Removal of the drain and source metal deposition is really promising in this sense, regarding the metallic behavior and the transparency of heavily boron-doped diamond (p++ contacts layer), but more globally n-side layer thickness needs to be adapted regarding the illumination spectra.

IV.4 Robustness of the non-volatile OFF-state

IV.4.1 Room temperature robustness

As control of dopants efficiency, the second parameter studied is the robustness of the NVPS. It is defined by the time during which the JFET is able to maintain the freeze-OFF state, when every control power (optical and electrical) is removed from the structure, except for the drain voltage which implies a drain current density in the conduction channel I_D, witness of the transistor state.

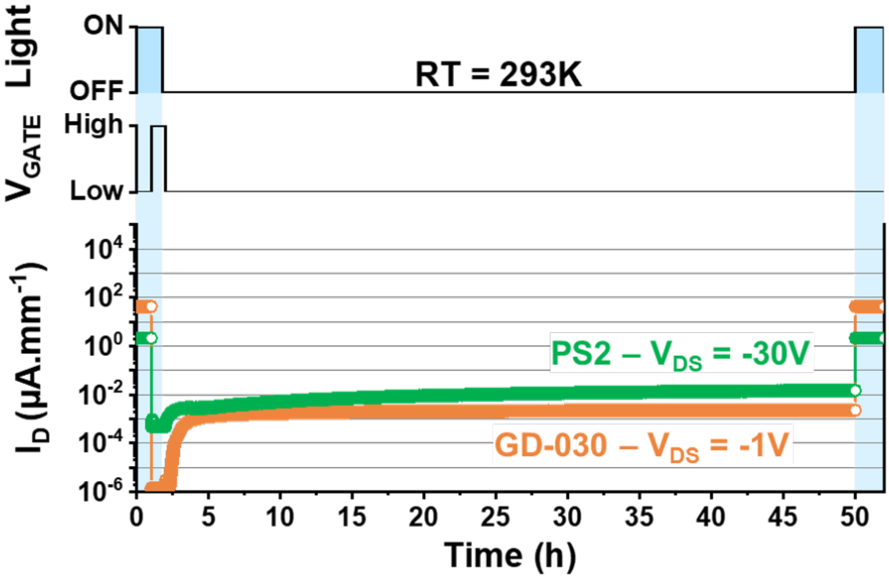

Figure IV.15: RT drain current density as function of time for GD-030 reference sample and PS2, after a closing cycle of the transistor and removing of optical and electrostatical control. Time range is adapted to demonstrate the robustness of the freeze and non-volatile OFF state that have previously been set by applying a gate voltage under illumination (active state).

The protocol used is shown in Fig.IV.15. First, the normally-ON transistors are turned OFF during the active state, by mean of a white light illumination of 11 mW.cm^{-2} and by applying a positive gate voltage. At RT, GD-030 sample has been measured with V_{DS} = -1 V and a gate voltage, mentioned as High, of V_G = 100 V, PS2 sample has been measured with V_{DS} = -30 V and V_G = 60 V. The drain to source voltage have been chosen for representative purpose and the gate to source voltage sufficiently high to ensure the full depletion of the conduction channel. Secondly, the light is removed, setting the NVPS in their frozen state and the gate voltage is, shortly after, turned OFF with a value of 0 V (Low). Thanks to the non-volatile properties, the transistors retrieving of their initial normally-ON state is kinetically limited. Thirdly, in the case of the transistor doesn't loose its frozen OFF state, the light is turned ON again to re-open the conduction channel to demonstrate the device functionality.

The re-opening of the conduction channel, or the lost of the non-volatile OFF state, is dependent of the probability for an electron fixed on its donor state to be generated prior to its recombination inside the SCR, inducing, by charge conservation, the retraction of this one. The generation probability of an electron in the n-type layer, whatever the mechanism involved, is dependent of the activation energy of the deep donor used and thus the temperature to which the transistors are subjected during operation. Robustness, or also the re-opening kinetic limitation of the transistors, temperature dependence is shown in Fig.IV.15 enlightening samples comparison.

At room temperature, non volatile OFF-state drain current (frozen state with V_{GS} Low) measured for sample GD-030 is four orders of magnitude lower than the ON-state current after two days of measurement. PS2 sample, with topside gate contact, still exhibit two orders of magnitude after the same duration, even if the ON/OFF ratio reported for both samples is different a similar re-opening behavior is reported. By conserving the criteria of considering the device closed when the drain current density is lower than 10% of its ON-state value, both sample are still closed after two days even if every control power has been removed from them. However, it should be mentioned that those results where highly reproducible in the concern of reference sample GD-030, whereas more discrepancy was observed in the concern of PS2. It has been found out that the rectangular or circular shape of the JFET characterized (see section II.3) significantly influences the stability of the non-volatile OFF state. While circular-shaped JFET proved good stability, hence reproducibility over the two days robustness, the rectangular design was more sensitive to random re-opening of the p-channel and robustness up to 16 hours, or less, could have been punctually observed. This difference illustrate the impact of the SCR morphology along the whole p-channel, where cylindrical extension offer better robustness. This circular architecture should be privileged in future NVPS realisation, when robustness is a crucial factor.

IV.4.2 High temperature degradation of the non-volatile OFF-state

Because the non-volatility is brought by the photo-ionization of substitutionnal nitrogen in the Ib substrate, any other source of ionization ratio increase in this layer is expected to be detrimental in regard to the non-volatile OFF state. In other terms, an increase of the temperature has been reported to be a degradation mechanism of the NVPS, ultimately causing for high temperature value ($>$ 250°C; 523 K) non-volatility effect loss (the JFET is always in its active control state). This detrimental impact is illustrated in Fig. IV.16 where the same protocol as described above has been used but at higher temperature, thus the same drain voltage of -30V and gate voltage noted High of 60V have been used for both samples.

At 100°C both samples have been maintained closed, by the mean of three orders of magnitude from the ON-state drain current density, during 2h30. This duration has been arbitrarily chosen but both samples can be maintained non-volatily closed for, at least, 2h30 at 100°C, with zero bias on the gate electrode and under the dark. The leakage current for sample GD-030 was measured higher than previously at room temperature but, at the opposite, sample PS2 shows lower leakage current for the same temperature. The mechanisms involved are still under

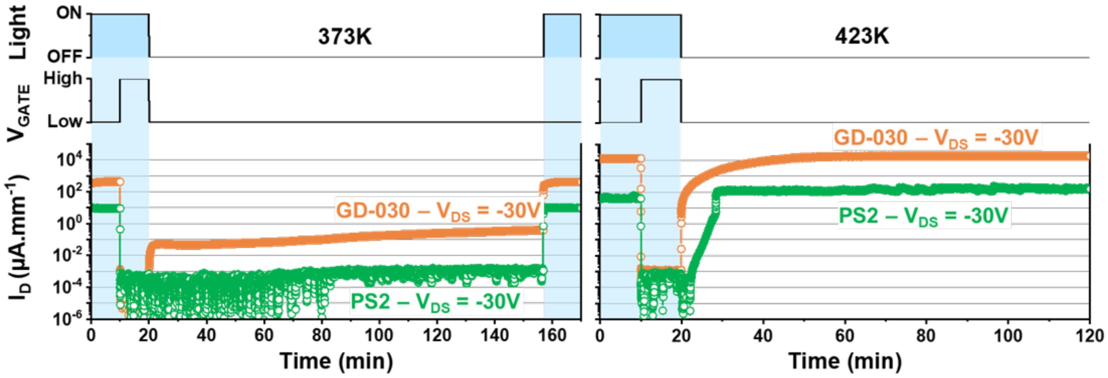

Figure IV.16: Left, 373 K (100 °) and right, 423 K (150 °) drain current density as function of time for GD-030 reference sample and PS2, after a closing cycle of the transistor and removing of optical and electrostatical control.

investigation but deep traps releasing electrons in the n-type layer is a good candidate.

When the temperature is increased up to 150°C, the robustness started to be degraded, as shown on Fig.IV.16. After the removal of gate voltage, shortly after the turning off of the light, the drain current density increases for both samples, causing a loosing of the non-volatile OFF state. Even if the re-opening mechanism seems to be different, the drain current density exceed 10% of the ON state value almost 7 min after the gate and light power supply removing, for both samples.

The robustness degradation was expected with the temperature increase due to its strong correlation with the ionisation probability of a dopant in the n-type region. Noticeably, regarding the SIMS results (see section III.7), no conclusion can be drawn regarding phosphorous impact on the non-volatile OFF state robustness. However it is strongly expected to provide lower stability, due to its higher optical capture cross-section than nitrogen [334, 376], but as counterpart it will provide lower commutation time for the device.

IV.5 Conclusion

To conclude this last chapter, a focus has been done on NVPS characterization for different external optical energy irradiation and biasing configurations. Successful transistor operation, however with poor on-state compared to the target caused by the deviation of compensation and layer thickness, were reported. The characterized interdigited transistors also suffered significantly from this deviation to such an extent that the initial target of 1 A and more than 1 kV could (and would, for the sample fabricated within this thesis) never been reached. Furthermore, the expected linear, or closer as possible, correlation between drain current and the geometrical aspect ratio of the source-to-drain exchanging surface (drain widening), is not observed for the only functional sample fabricated during this thesis (PS2). Only 20% efficiency have been recorded thanks to a drain widening up to 2 mm. However, as the yield of device functionnalization depends mainly on the growth and fabrication process quality, whatever the device design, large-scale device architecture must be attempted more in the future. Especially considering the possibility of device paralleling where 1 A handling does not seems inconsiderable for diamonds.

Under constant monochromatic illumination, sample fabricated within this thesis using gate contact closer to the transistor active area, demonstrates turning-OFF time for the fabricated JFET used as NVPS, divided by four (0.7 ms under 400nm illumination) compared to the reference sample, with substrate back-side gate contact (5 ms under 400nm illumination). Turning-ON of both transistors is closer from each other due to the trade-off that subsists between the n-type diamond resistance and the capacitance of the SCR, formed between the n-type diamond gate and the p-type diamond conduction channel. Dynamic capacitance of the pn junction model has to be developed in order to take into account the changes in free charge carrier over time, whereas capacitance could not be measured on the samples as being below detection limit. In terms of commutation performance for this kind of structure, a closering of the gate contact to the active area shows better results and thus, will be preferable for NVPS fast switching operation. Unfortunately the absence of significant phosphorous concentration does not allow any further conclusion on its impact but it is still expected to have a beneficial impact on the transistor dynamics. The robustness, or the time during which the transistor stay in the frozen OFF state, is demonstrated to not be affected by the use of the two configurations mentioned herein-above. The temperature is more critical for both transistors, lowering the robustness of more than two days at room temperature, to few minutes at 423 K which is still largely sufficient for power electronic or biological application. Further optimization can be done on the device design in order to improve the light collection efficiency, especially near the active area of the transistor.

General conclusion & Perspectives

The unique mechanical, thermal, optical and most importantly electrical, properties of diamond, were presented along the first chapter as an introduction to the leading-edge power electronic (and not solely) devices based on this superior material. The ongoing for large-scale diamond components is crucial for their future prospects in power electronics, as a true demonstration of diamond potential still lacks. This manuscript revolves around the convergence of power electronics and novel hybrid technologies that integrate optical and electrical principles to leverage the vast energy potential inherent in diamond. In this context, the heart of this thesis is dedicated to the development of large-scale diamond-based Junction Field Effect Transistors (JFET) that can be electro-optically controlled and used as non-volatile memory devices.

The principles of 1D pn junctions and existing literature were used to project the expected performance of a basic lateral JFET design. This analysis included factors like conductivity and blocking voltage capabilities, relying on established models and parameters. Recognizing the challenges associated with small diamond samples and high-quality n-type diamond growth, emphasis have been put on streamlining the technological steps, aiming to minimize process-induced defect density for large-scale devices. Optimized large-scale interdigited JFET architecture has been proposed to align with these considerations. Although more complex designs theoretically offer superior performance, they would require advancements in fabrication processes and diamond growth control. To illustrate this, it has been demonstrated that, theoretically, the ON-resistance of the device is still dominated by the channel resistance, meaning that an increase in the number of finger (multiplication by 2v or 3) will still be beneficial for the ON-state current without affecting the OFF-state blocking voltage. The interdigited JFET architecture, while compatible with NVPS fabrication, requires trade-offs that can affect NVPS performance, and vice versa. For instance, optimizing the metallic covering of the source and drain contacts enhances on-state conductivity, as it lower the contact resistance by more than 3 orders of magnitude, but may hinder the light collection efficiency of the NVPS. In this work, a metallic coverage of 60% of the PS2 sample surface, leads to a similar percentage loss in term of transmittance, revealing the negative impact of high metallic coverage on the light collection near active area of the transistors. Balancing these aspects may necessitate more complex models, simulations tools that are not optimized for diamond and fabrication processes. Throughout this chapter, discussions assumed ideal pn-junctions and layer contacts, without considering parasitic charges or defects. However, unintentional impurities and structural defects can significantly impact layer resistivity, potentially rendering the device insulating.

Successful operation of four fabricated JFET aside with the structural and electrical characteristics of the as-grown p-channel and n-gate layer and contacts are presented in this manuscript. Imaging and non-destructive electrical measurements were conducted initially, but proved inadequate for understanding the insulating properties of p-channels in three over the fourth samples fabricated. As a result, a reevaluation of parameters like layer resistivity, doping, compensation, and film thickness, which are critical for the optimized JFET architecture, was necessary. Subsequently, SIMS analyses were performed, revealing in juxtaposition with CL spectra and electrical measurments significant variations in the internal layer parameters among the four samples. Notably, none of the as-grown layer met the design specifications, except for the heavily boron-doped ones. The boron-doped p-channels had adequate doping-level but were way thinner than expected with compensation ratio than can goes over 100% in some cases, explaining the insulating properties in most of the fabricated samples. Despite efforts, such as oxide encapsulation and n-side polarization, no conductance was observed. Moreover, an unexpected absence of phosphorous concentration was noted. This result underscores the importance of layer thickness and dopant concentrations in sample functionality. It's worth noting that diamond technology is still evolving, and the development of diamond-based devices depends on providing reliable, high-quality layers. Nevertheless, despite the difficulties inherent in this exceptional material, a functional sample, in the sense that a transistor effect (JFET) was observed, was obtained from this production batch.

In particular, this successful fabrication allowed a focus on NVPS characterization for different external optical energy irradiation and biasing configurations. Successful transistor operation, however with poor on-state compared to the target caused by the deviation of compensation and layer thickness, were reported. A small insight has been given in the concern of interdigited transistors paralleling but for the same reason just mentioned the initial target of 1 A and more than 1 kV would never been reached. However, the possibility of device paralleling demonstrated promising results where 1 A handling does not seems inconsiderable for diamonds. Under constant monochromatic illumination, sample fabricated within this thesis using gate contact closer to the transistor active area, demonstrates turning-OFF time for the fabricated JFET used as NVPS, divided by four (700 μs under 400 nm illumination) compared to the reference sample, with substrate back-side gate contact (5 ms under 400 nm illumination). Turning-ON of both transistors is closer from each other due to the trade-off that subsists between the n-type diamond resistance and the capacitance of the SCR, formed between the n-type diamond gate and the p-type diamond conduction channel. Dynamic capacitance of the pn junction model has to be developed in order to take into account the changes in free charge carrier over time, whereas capacitance could not be measured on the samples as being below detection limit. In terms of commutation performance for this kind of structure, a closering of the gate contact to the active area shows better results and thus, will be preferable for NVPS fast switching operation. Unfortunately the absence of significant phosphorous concentration does not allow any further conclusion on its impact but it is still expected to have a beneficial impact on the transistor dynamics. The robustness, or the time during which the transistor stay in the frozen OFF state, is demonstrated to not be affected by the use of the two configurations mentioned herein-above. The temperature is more critical for both transistor, lowering the robustness of more than two days at room temperature, to few minutes at 423 K which is still largely sufficient for power electronic or biological applications. Further optimization can be done on the device design in order to improve the light collection efficiency, especially near the active area of the transistor.

Perspectives

Even if building blocks for JFET have been added and detailled within the context of this thesis, on the longer term, the development of both diamond-based large-scale power devices and innovative electro-optical control of diamond-based transistors still have several challenges to overcome.

To achieve devices with active areas on the order of a few mm^2, improvements in fabrication process reproducibility are necessary. While substrate production is geared towards preparing for 2" wafer production, the low demand for such substrates hinders their further development. This stems from limitations in substrate quality, reproducibility, and size, which, in turn, constrain device capabilities and potential, ultimately discouraging investments in expanding wafer sizes and enhancing quality. However, the interdigited architecture proposed in this work aims to break this paradoxical cycle by offering an easily implementable lateral device concept. In the development of diamond power devices, the focus has often been on diamond wafer size as a limiting factor. It's becoming increasingly clear that quality and reproducibility play a more significant role in creating competitive devices than simply achieving large-scale production. This is exemplified by the latest thesis defended within the group for the last decade, where similar functionalization yield were obtained independently of the devices developed. Until a technological breakthrough in the production of vertical transistors is achieved, the extensive development of larger area lateral devices should be prioritized in the coming years, particularly for bulk conduction-based devices such as deep depletion diamond-based transistors.

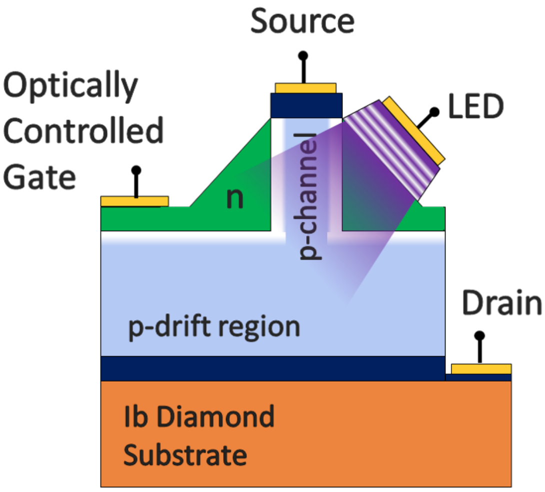

Figure IV.17: Schematic cross section representation of the targeted ideal and optimized futur NVPS, with a GaN LED bounded to n-type diamond on a vertical transistor architecture.

Moreover, diamond as semiconductor is not limited to high power applications. Bio-sensors and particle detectors, both in the potential scope of application for NVPS are also innovative active fields of research, playing a significant role in the basic understanding of diamond physics. Although this novel added switchable state was initially perceived as a disruptive factor in lateral MOSFET power devices, it has been further reported in this thesis to be sufficiently efficient to design devices based on the enhancement of this effect. The high internal gate resistance, responsible of extended commutation-time, initially reported for this device, were systematically decreased by closering of the gate electrode contact and are expected to be further enhanced by introduction of a thin highly phosphorus-doped layer, due to increase of light carrier efficiency. To provide perspectives about the building blocks that needs to be added on this device, Fig. IV.17 represent the ideal architecture that could be reached thanks to improvements listed below:

- metallic source and drain contact should be avoided around actives areas. Thanks to highly boron doped metallic diamond a low access resistivity, that almost never limit the conduction inside the p-channel, is obtained. The layer being thin is therefore almost transparent and its solely uses for contacts enhance the light power density absorbance inside the n-type diamond.

- Addition of phosphorous doped diamond still need to be demonstrated as performance enhancer. If it is expected to have a positive impact on the internal gate resistance, it is also highly challenging to grow and fabricate.

- High light power density can be reached by the bounding of a GaN light emitting diode directly on the diamond surface to maximize the light power absorbed. This solution, seems unrealistic at this stage of development regarding the technological breakthrough that needs to be overcome prior envisaging it.

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English abstract

Increasing population density within compact urban regions, when juxtaposed with the preferred decentralized electricity generation and its increasing demand, underscores the necessity of enhancing our electrical transport and conversion infrastructures, particularly in light of the challenges posed by its storage. Silicon-based power devices, which currently form the backbone of various conversion stages, have nearly reached their theoretical limits and the only road to improve their performance is to use new materials with better properties. Among potential candidates, diamond with outstanding physical properties is the ultimate semiconductor for power electronics that couple high power handling, high switching frequency, low losses and high thermal management capabilities. Besides being the hardest material, diamond possesses the best properties among ultra-wide band gap semiconductors including its high electron-hole mobility (1060-2100 $\text{cm}^2/\text{V.s}$ respectively), high critical electric field ($\geq$ 10 MV/cm) and high thermal conductivity (22 W/cm.K). Thanks to its exceptional physical properties diamond offers novel opportunities for a wide range of multi-disciplinary application, extending beyond to, but potentially compatible with, power electronics, like: localized electric, optic and magnetic signal probing, reliable data processing, and secure communication in both harsh and in-vivo biological environments. The development of diamond devices capable of non-volatile charge storage and individual embedded devices addressing is essential for creating monolithic diamond-based systems, highly beneficial for future intelligent power conversion system implantable in smart grids or aerospace harsh environment. Despite several technological limitations and bottlenecks that need to be addressed in order to extract diamond's full potential, like the challenging device fabrication due to small standard substrate size, lab-grown diamond layer quality and dedicated device architecture have made considerable progresses over the last decades.

This thesis is dedicated to the development of large-scale diamond-based Junction Field Effect Transistors (JFET) that can be electro-optically controlled and used as non-volatile memory devices. The optimization of these components, which serve dual purposes, is crucial for the future road-map of diamond technology. Firstly, in the realm of power electronics, there is a need for a true demonstration of large scale diamond devices potential. State-of-the-art devices, often optimized for small active areas, typically excel in either high current density handling or high breakdown field but seldom in combination of both. As a result, devices capable of both conducting 1 A in ON-state and withstanding 1 kV in the OFF state have yet to be demonstrated. On this purpose, the optimization of lateral JFET design especially diamond layer inner properties and inter-digited geometry modelisation has been proposed. Results below initial expectations have been reported but still holding the promise of achievability for the technical specification mentioned herein-above. Secondly, fabrication, characterization and optimization of a diamond-based JFET non volatile photo-switch has been achieved. Since the first demonstration of the structure at the early stage of this thesis, architecture featuring gate contact closer to the active area of the fabricated transistors exhibits better dynamics for equivalent leakage current. Increasing the light collection efficiency of the device by removing non-transparent metallic contact is expected to lower the commutation time of the device by at least one order of magnitude. Additionaly, robustness of the non-volatile OFF state have been reported over more than two days. By combining both functionalities, diamond technology is poised to capture the attention of researchers and companies, thereby driving further development and eventual commercialization.

French abstract

L'augmentation de la densité de population urbaine et la demande croissante d'électricité pour une production décentralisée des points de consommation, souligne la nécessité d'améliorer nos infrastructures de transport et de conversion électrique, notamment face aux défis posés par son stockage. L'hégémonie des composants à base de silicium pour l'électronique de puissance arrive à son terme aux grands bénéfice des semiconducteurs à ultra-large bande interdite, tel que le diamant, reconnu pour exceller dans ce domaine grâce à: la grande mobilité des électrons et des trous (1060-2100 $cm^2/V.s$ respectivement), un champ électrique critique élevé ($\geq$ 10 MV/cm) et une conductivité thermique élevée (22 W/cm.K). Grâce à ses propriétés physiques exceptionnelles, le diamant offre de nouvelles applications multidisciplinaires, allant au-delà de l'électronique de puissance, tout en restant compatible avec celle-ci, telles que: la détection de signaux électriques, optiques et magnétiques localisés et la communication sécurisée dans des environnements difficiles. Le développement de dispositifs en diamant capables de stocker non-volatilement des charges et d'adresser des dispositifs intégrés individuels est essentiel pour créer des systèmes monolithiques à base de diamant, bénéfiques pour les futurs systèmes de conversion de puissance intelligents implantables sur le réseaux électrique, ou les environnements difficiles. Malgré plusieurs limitations technologiques, notamment les difficultés de fabrication relatives à la petite taille des substrats standard; la qualité des couches de diamant synthétiques et le dévelloppement d'architecture de composant dédiés à ce dernier ont permit des progrès considérables au cours des dernières décennies.

Cette thèse est dédiée au développement de transistors à effet de champ à jonction (JFET) en diamant et de grande taille, pouvant être contrôlés électro-optiquement et utilisés comme mémoires non-volatiles. L'optimisation de la double fonctionnalitée de ces composants présente un interêt majeur dans le dévelloppement des futurs technologie à base de diamant. Premièrement, dans le domaine de l'électronique de puissance, il est nécessaire de démontrer le véritable potentiel des composant à base de diamant au travers de composant de grande taille. Les dispositifs de pointe, souvent optimisés pour de petites zones actives, excellent généralement soit dans la gestion d'une densité de courant élevé, soit dans les forts champs électriques, mais rarement dans la combinaison des deux. En conséquence, aucun dispositifs capables de conduire 1 A à l'état passant et de supporter 1 kV à l'état bloqué, n'a encore émergé. Pour répondre à ce point, une conception optimisée des JFETs latéraux a été proposée, fabriquée et charactérisée, en se basant sur une géométrie interdigitée. Des résultats en deçà des attentes initiales ont été rapportés, mais ils restent positifs et permettent néanmoins de valider le potentiel de ce type d'architecture. Deuxièmement, la fabrication, la caractérisation et l'optimisation d'un commutateur photo-électrique non volatile à base de diamant ont été réalisées. Depuis la première publication de cette structure innovante au début de cette thèse, l'architecture optimisée, avec un contact de grille plus proche de la zone active des transistors, présente de meilleure fréquence de commutation pour un courant de fuite inchangé. L'augmentation de l'efficacité de collection lumineuse du dispositif, spécifiquement en supprimant les contacts métallique non transparent, devrait permettre de réduire les temps de commutation du dispositif d'au moins un ordre de grandeur supplémentaire. De plus, la robustesse de l'état bloqué non volatile a été maintenus pendant plus de deux jours. L'optimisation de ces composants est une brique technologique supplémentaire démontrant la large gamme d'application du diamant qui au vus de sa maturitée croissante, sucite un interêt commercial grandissant.