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# Etude expérimentale et modélisation des phénomènes de cellules fragilisées dans les DRAM en environnement radiative.

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# THÈSE POUR OBTENIR LE GRADE DE DOCTEUR DE L'UNIVERSITÉ DE MONTPELLIER

En Electronique

École doctorale I2S – Information Structures et Systèmes

IES – Institut d'Electronique et des Systèmes

Étude expérimentale et modélisation des phénomènes de  
cellules fragilisées dans les DRAM en environnement radiatif.

Experimental study and modeling of weakened cell phenomena  
on DRAMs in radiative environment.

Présentée par NGUYEN Tran-Hoang

Le 15 Juin 2021

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# Abstract

In the harsh environment of space, high energetic particles are the source of many radiation effects which can not only degrade but also alter electrical components onboard spacecraft. As a result of inflight observations of the CARMEN experiment and the PICARD satellites star tracker's memory, a new type of error with unique characteristics, called weakened cells (or Intermittent Stuck Bit - ISB), has been observed. On the DRAM memory, this error occurred repeatedly at the same addresses, being persistent during power cycles of the device and randomly stuck/unstuck over time. While many studies suggest that displacement damages is the root cause, the main mechanisms in place are still under debate. This thesis, supported by CNES and TRAD company, has been carried out to study the phenomenon on DRAM devices, through both experiment and simulation. The inflight reference as well as new ones from different manufacturers were tested on the ground level under proton and heavy ions irradiation. Experimental results at the component level showed that the coupled effect of a damaged cell with a faulty DRAM refresh operation can lead to unexpected error behaviors. Meanwhile, TCAD simulations with ECORCE software provided more details on the underlying physical mechanisms at the single DRAM's cell level. The 2D model of the transistor accessed under single and combined radiation effects showed a dramatic increase in leakage current in the damaged cell, which is the main cause of the retention time degradation. Finally, the coherence between the two was joined to give a projection of future trends.

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En environnement spatial, des particules à haute énergie provoquent de nombreux effets sur les composants électroniques des satellites. Ce rayonnement dégrade le fonctionnement des composants et peut provoquer la défaillance du satellite. À la suite des observations en vol de l'expérience CARNMEN et de la mémoire du suiveur d'étoiles des satellites PICARD, un nouveau type d'erreur aux caractéristiques uniques, appelé cellules fragilisées (ou Intermittent Stuck Bit - ISB), a été observé. Sur la mémoire de la DRAM, cette erreur s'est produite de manière répétée aux mêmes adresses, et reste persistante lors des cycles de mise sous tension/arrêt de l'appareil et se bloque/débloque aléatoirement dans le temps. Cette thèse, soutenue par le CNES et la société TRAD, a été réalisée pour étudier le phénomène sur des dispositifs DRAM par l'expérimentation et la simulation. La mémoire DRAM utilisée par les satellites ainsi que plusieurs autres circuits ont été testés au sol sous irradiation de protons et d'ions lourds. Les résultats expérimentaux ont montré que l'effet couplé d'une cellule endommagée avec un fonctionnement de rafraîchissement de la DRAM défectueuse peut entraîner des erreurs inattendues. Parallèlement, les simulations TCAD avec le logiciel ECORCE ont fourni plus de détails sur les mécanismes physiques sous-jacents au niveau d'une cellule de la mémoire DRAM. Les modélisations TCAD du transistor ont montrés que l'effet combiné de plusieurs mécanismes générés par le rayonnement provoque une augmentation significative du courant de fuite du transistor. Ce courant est la principale cause de la diminution du temps de rétention. Enfin, la cohérence entre l'expérimentation et la simulation a été jointe pour donner une projection des tendances futures.



# Acknowledgement

In 2012, during Curiosity rover landing on Mars, I made up my mind to pursue my dream in space. This time, another rover named Perseverance is about to go through “7 minutes of terrors” to set wheels on Mars. Since I was a child, I have always been curious to study about Space and I have determined to follow that path. This PhD is another chance for me to get closer to my dream. My PhD is a long journey which includes many unforeseeable challenges. Fortunately, along that journey, I have received tremendous amount of support and assistance.

First and foremost, I would like to thank Françoise Bezerra from CNES and Nathalie Chatry from TRAD. I am grateful for their supports and suggestions during this work. This thesis was realized under generous support from CNES and TRAD.

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# General Introduction

In the harsh environment of space, there are not only apparent threats such as vacuum of space, meteoroids or space debris but also other invisible threats of space radiation. Before the Space Race began, cosmic rays were discovered in August 1912 by Austrian physicist Victor Hess [1] by high altitude balloon experiment. Following by the competition to launch the first spacecraft to orbit, Explorer 1 satellite of United States discovered the existence of radiation belts around the Earth - the Van Allen belts [2] in 1958. Soviet Union in that time was also able to detect solar wind particles in space with Luna 1 spacecraft in 1959 [3]. These discoveries and observations, among others, made it possible to early establish that space is a very hostile environment for electronics. It was one of the major motivations for many studies of the effects of radiation on electronics. The studies and controls of the impact of radiation on equipment has become indispensable for every space mission, more commonly known as Radiation Hardness Assurance (RHA).

Nowadays, with the blooming of the New Space race, more and more COTS (Components of The Shell) are used in space. Furthermore, more advance and powerful computer systems are brought to space in the faster pace. From radiation assurance point of view, it is necessary to continue the studies on physical mechanisms of degradation and malfunction of these systems. The threats caused by the radiative environment need to be understood and quantified to ensure the reliability of systems subjected by radiative environment. Among one of the main memories of every computer system, that will not be replace any time soon, is DRAM (Dynamic Random-Access Memory). It provides faster speed at cheaper price compare to SRAM or Flash memory. Due to its simple design, DRAM is susceptible with radiation effects which includes single event upset or stuck bits. However, a new type of error called weakened cells or some studies can refer as intermittent stuck bits arise recently. It was first observed inflight onboard CARMEN2 experiment by CNES (Centre National d'Etudes Spatiales) launched on 22th of June 2008 aboard JASON2 satellite and observed again on star tracker memory of PICARD satellite launched on June 15, 2010. This relatively new type of errors can be troublesome for Error detection and Correction Code (ECC) of the memories due to its randomness stuck/unstuck behavior.

This Ph.D. in partnership with CNES and the TRAD company - an expert in the radiation field, aims to study the weakened cells phenomenon in details. Firstly, the behaviors of weakened cells and its characteristics on DRAM under different energetic particles such as protons and heavy ions will be investigated through irradiation campaigns. Then, simulations with TCAD (Technology Computer Aided Design) tool ECORCE will be performed in order to study the physical mechanism underlying. The simulations will allow us to study the DRAM cell from not only single radiation effect but also combined ones. Finally, these studies will be correlated and give a projection for the future trends.

In order to present the works of this subject, the manuscript is structured in five chapters:

The first chapter presents an overview of different elements of space radiative environments as well as the models that are used. Then, the effects of radiation induced on the electronic components, which include both single event and cumulative effects, are introduced and

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explained. Moreover, the main object of study - weakened cell phenomenon is introduced along with literature studies done on the subject.

The second chapter is devoted to give a detail look into DRAM devices which are the main components endured the phenomenon. This chapter initiates with DRAM architecture and layout, following by DRAM working mechanism and its physical structure. Furthermore, different radiation effects on the device are also discussed.

Before going to the simulation works, the third chapter presents the experimental side of the thesis. The experiment campaigns were carried out in collaboration with TRAD under the support of CNES. These experiments help to understand the weakened cell phenomenon and identify new potential causes of the events. This chapter begins by describing the test configuration, test plan and concludes with experimental results.

The fourth chapter presents works from using TCAD simulation tool - ECORCE to study different radiation effect on the DRAM cell. In this chapter, ECORCE will be introduced with its physical principles. Then, a 1D model of the DRAM transistor access node with the effect of defect cluster is studied.

Finally, the 2D model of whole access transistor are constructed. In order to see the physical responses, not only individual type of radiation effect (defects cluster, volume traps and interface traps) but also combined of two or more effects are applied at the same time to the pristine device. The results obtained from this chapter will be used to correlate with experimental results in order to give an explanation for the phenomenon and predict trends for the future.

The manuscript ends with a general conclusion by the assessment of all the works carried out during this thesis. It shows the advances in the understanding of the weakened cell phenomenon, as well as perspectives, citing the avenues of interest for further studies on this subject.

# **Chapter 1: State of the art of the weakened cell phenomenon**

## **1.1. Introduction**

In order to start this study, it is necessary to show the effects of the radiation environment on the electronic components. This thesis will focus mainly on the space radiation environment, which is of particular interest for this study, where the weakened cells have been detected onboard satellites at the first place.

This chapter will start by discussing about various sources of space radiation, then following by their effects on electronic components. Explanations are given based on possible interactions between the particle and matter.

Finally, the weakened cell phenomenon will be discussed. The behaviors will be described from observation data, then the literature study will give us more details about the phenomenon. The main properties and possible origins are also mentioned.

## **1.2. Space Environment**

For every space mission, the space environment is one of the most important aspects to be considered in order to ensure the reliability of the system during operation period. There are various environmental factors that can affect the spacecraft on orbit including: Meteoroid and space debris; Atmospheric residual and energetic particles radiation.

As we know the Earth atmosphere does not end abruptly but extends to space with decreasing density as well as pressure. The excess at the upper part of atmosphere takes part in the drag that gradually decreases the orbit altitude and in the erosion on the surface of material. In the vacuum of outer space, we have other effects such as out gassing of material, cold welding between mechanical join and also the limitation of heat transfer method on the satellite's body. Meteoroid and space debris can cause physical impact at high velocity, the aftermath is usually catastrophic and it's getting worse when more debris are created. Last but not least, one of the most reason for malfunctions or even loss of functionality of electronic devices on board satellite is caused by energetic particles. There are three types of space radiation: Galactic Cosmic Rays (GCRs), solar energetic particles and trapped particles. Next sections will discuss in detail their properties as well as models in used.

### **1.2.1. Galactic cosmic rays (GCRs)**

Galactic Cosmic Rays (GCRs) are charged particles traveling near the speed of light originated from outside of the Solar System whose origin is not yet well defined. GCRs are composed of charged particles which contain atomic nuclei in the majority and only about 1% electrons. The nuclei consist of about 90% protons, 9% alpha particles and the rest are heavier ions [4]. The spectra peaks at around 1GeV and the energy can go up to  $10^{11}$ GeV [4], an overview of energy spectra is given in Figure 1 which shows the flux reaching the Earth in the form of the energy carried by particles per unit interval [5]. Their elements are stretched across Periodic Table, the relative abundance is shown in Figure 2 on the right.

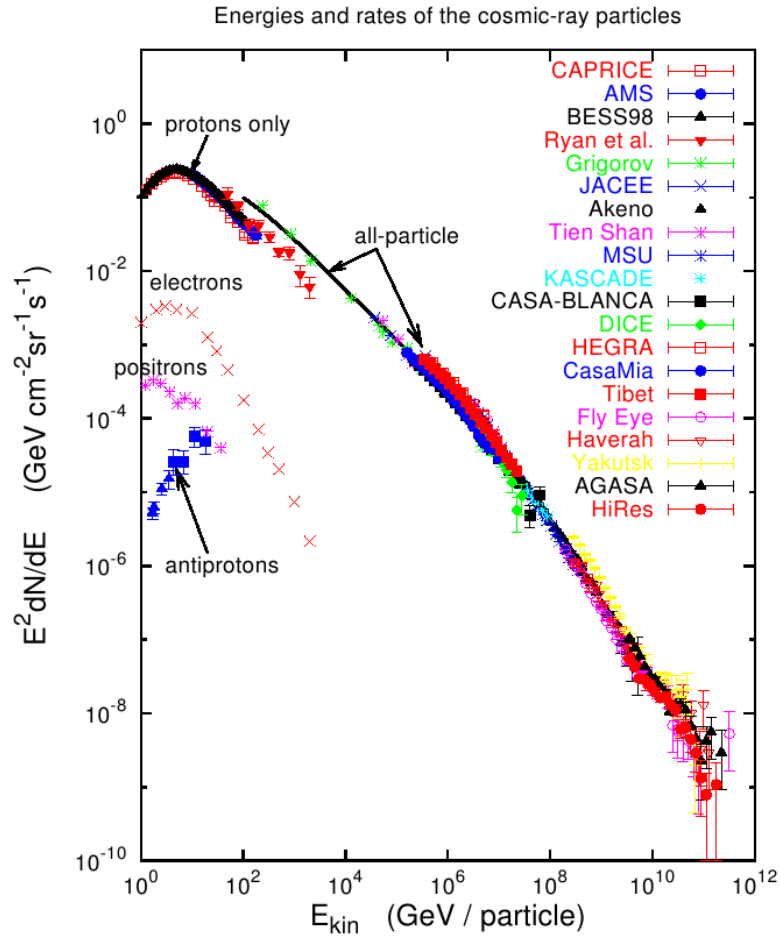


Figure 1: Overview cosmic ray flux over a wide energy range .The flux are presented in the form of the energy carried by particles per unit interval [5].

GCRs are in the form a continuous flux averaging at a few particle/cm<sup>2</sup>/s and vary according to solar activity. Ions with lower energy than 10GeV are modulated by the heliosphere and solar wind. At maximum solar activity, there is a lower flux with particles below 10 GeV that create the spectra as shown in Figure 2 (left). The relative abundances at 2 GeV of various particle species in GRCs and solar particles are also shown in Figure 2 (right).

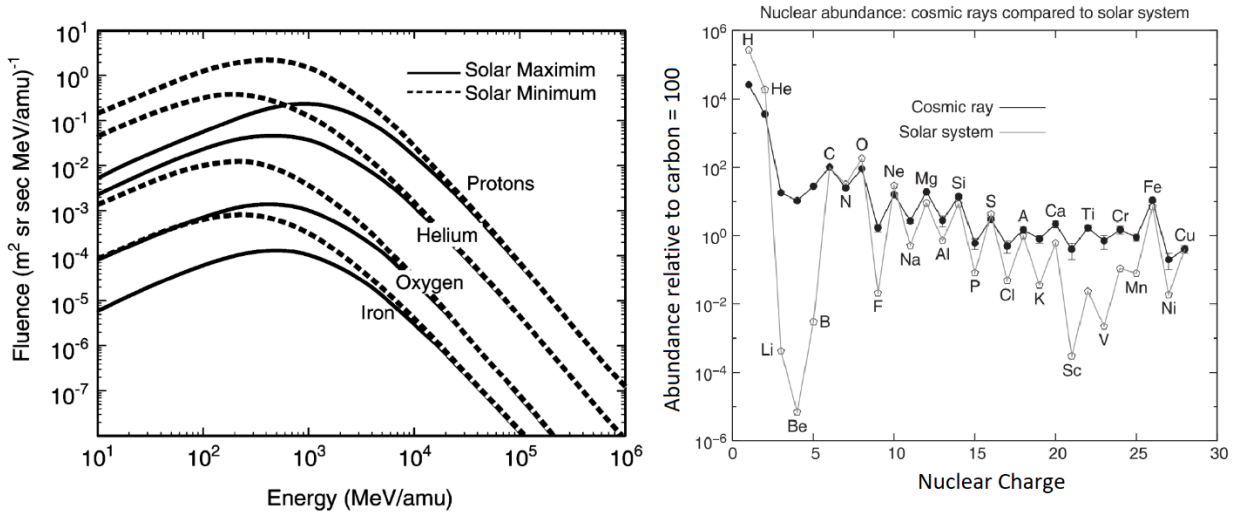


Figure 2: GCR energy spectra for protons, helium, oxygen and iron during solar maximum and solar minimum conditions (left) [6]. The relative abundances of GCR in cosmic ray and in the solar particles (right) [4].

Each space mission undergoes different cosmic ray spectra depending on its orbit relative to the geo-magnetic field. The Earth's magnetic field provides some good protection for the lower earth orbit as the charge particles are guided by the magnetic line. However, in the polar region, the magnetic line points towards the earth which will have a significant chance of interaction with the satellite on polar orbit. Despite their low density, GCRs can contribute significantly to microelectronic anomalies onboard satellites because of their high atomic number and energy.

The Cosmic Ray Effects in MicroElectronics (CREME96) model is widely used as a standard model of space environment as well as for microelectronics devices. CREME96 is the upgraded CREME86 model created by Dr. Jim Adams et.al. at U.S. Naval Research Laboratory. This model includes a comprehensive set of cosmic ray, flare ion LET, energy spectra and also geomagnetic shielding and material shielding [7].

In European's ECSS-E-ST-10-04C – Space environment standard, CREME96 has been replaced by the ISO15930 standard developed at Moscow State University (MSU). This model uses 12 months averages of Wolf (sun spot) number to account for the solar-cycle variation, and the Sun polar magnetic field for scale heliospheric changes [8].

Independently of the MSU's model, the Badhwar and O'Neill (BON) model developed at NASA is based on a similar approach to solving numerical equation for diffusion, convection, and adiabatic deceleration under the assumptions of a quasi-steady state and spherically symmetric interplanetary medium [9]. However, BON model is correlated with ground-based neutron monitoring to give long-term prediction, meanwhile MSU model is multi-parametric to fit solar cycle variation with observed sun sport numbers in the GCR intensity.

In the models mentioned above, the basic description of solar cycle variation is used to account for GCR intensity change, however this has been addressed to simplify into the single dependence on a well observed parameter. The model derived from ISO model by Daniel Matthia et.al. [10] uses a single parameter obtained from the measurements of the Advanced



Composition Explorer (ACE) spacecraft and the Oulu neutron monitor count rates. Figure 3 is the comparison of flux between models for GCR iron at different levels of solar activities.

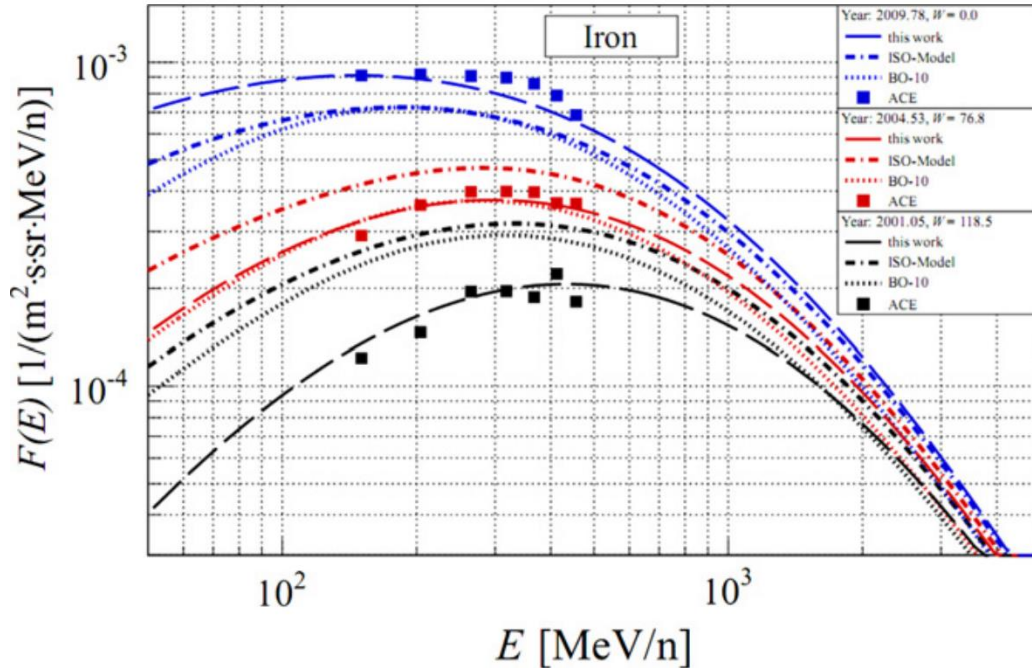


Figure 3: Comparison of the model presented by Daniel Matthia et.al. with the ISO model, the BO-10 model and ACE data for GCR iron. The selected dates between 2001 and 2010 represent low modulation ( $W_{ACE} = 0$ , solar minimum), moderate modulation ( $W_{ACE} = 76.8$ ), and strong modulation ( $W_{ACE} = 118.5$ , solar maximum)[10].

### 1.2.2. Trapped particles

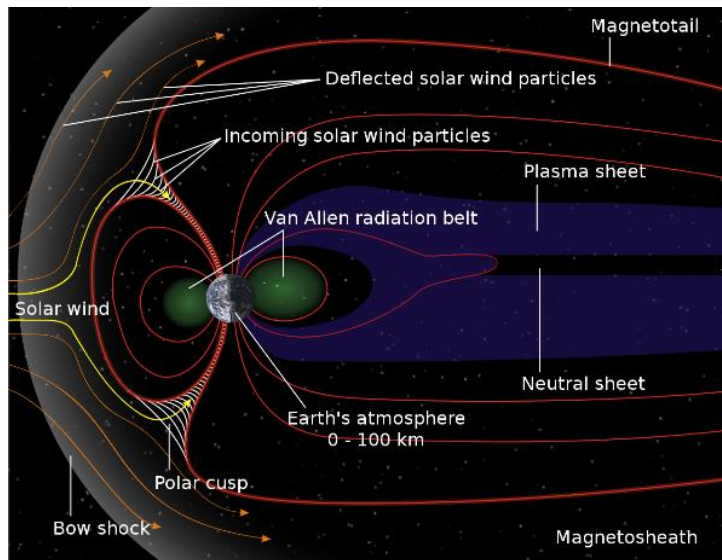


Figure 4: Illustration of Earth's magnetic field.

The Earth's natural protection against extreme solar winds and separates us from interplanetary medium is its magnetic field. Under pressure from solar wind, it forms a teardrop shape which the facing-Sun side is suppressed and the opposite side is extended away from the Sun. In the Earth electromagnetic field, charged particles are subjected to the Lorentz force:

$\vec{F} = q(\vec{v} \times \vec{B} + \vec{E})$  where  $q$  is the particles' charge,  $\vec{B}$  the magnetic field,  $\vec{E}$  is the electric field and  $\vec{v}$  is the velocity of the particles. The movements of trapped particles inside magnetic field are composed of three quasi-periodic motions (Figure 5): gyro motion around the magnetic field line, bounce motion between the conjugate of mirror points and drift motion around the Earth [11]. At the center of the belts, the trapped particles can reach a peak at around 500 MeV, while in geostationary orbit (GEO), the protons at a few MeV and the protons with energy above 10 MeV are limited at below 20000 km of altitude.

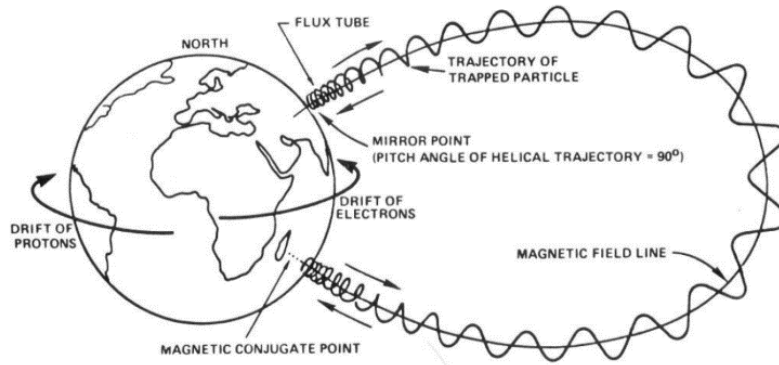


Figure 5: A descriptive drawing of the three types of motion of particles trapped in the Earth's magnetic field [11].

The magnetic field of the Earth is dipolar, its axis is tilted 11 degrees from the Earth rotation axis and offset 500km towards the north Pacific. The consequence is an anomaly region called the South America Anomaly (SAA), which is a manifestation of the inner proton belt over the South Atlantic region (Figure 6).

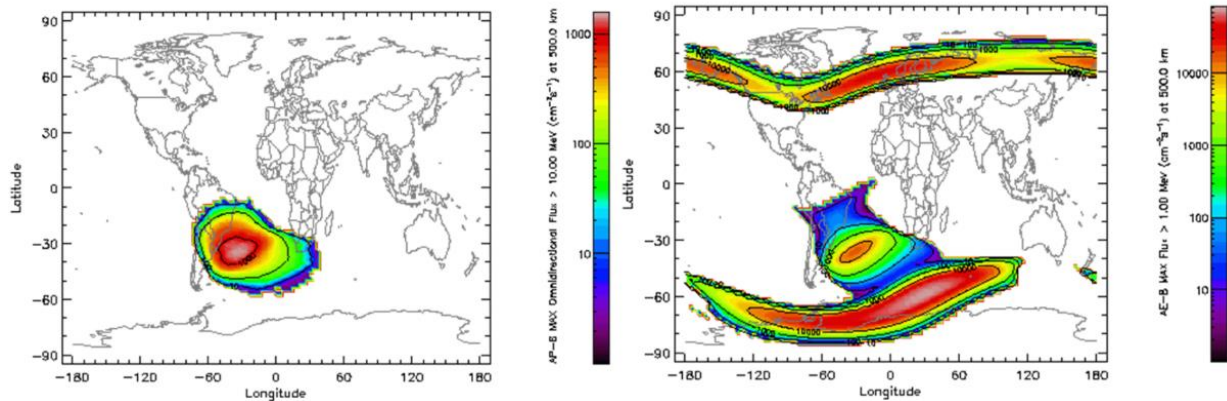


Figure 6: World map of the modelled trapped particle populations: (Left) AP-8 MAX integral proton flux >10 MeV at 500 km altitude; (Right) AE-8 MAX integral electron flux >1 MeV at 500 km altitude [8].

Charged particles from the sun and cosmic rays can be trapped inside the Earth's magnetic field and form Van Allen radiation belts. Proton and electron are the main components of the inner region, where the outer region is dominated by electron. Table 1 describes the particles, the energy and the range in which they mostly concentrated.

Table 1: Characteristics of the earth's radiation belts [12].

Particle	Energy	Extension (Earth's radius ~ 6400 km)
e-	1 keV – 10 MeV	1-10
p+	1 keV – 300 MeV	1-7

For the inner belt, the effects on electronics devices can include: total dose degradation, single event effects and nuclear activation [13]. In the meantime, the outer belt is dominated by electrons with energy less than 10 MeV. In low earth orbit (LEO), satellites are exposed to trapped protons and electrons from SAA and electrons for altitude below 1000km, and to the proton and electron for higher altitudes of the polar horn. Satellites in GEO and Medium Earth orbit (MEO) are mainly exposed to trapped electrons. Their effects are mainly: total dose, surface electro-static discharges (ESD) and internal charges.

The most commonly used models for trapped particles are AP8 (Aerospace Corporation Proton version 8) for protons and AE8 (Aerospace Corporation Electron version 8) for electrons. They were developed at Aerospace Corporation for the NSSDC at NASA/GSFC from experimental data collected between 1958 and 1978. The AP8 covers proton energy from 0.1 MeV to 400 MeV with a validated range of 1.15 to 6.6 Earth's radius, AE9 covers electron energy from 0.04 MeV to 7 MeV and a validated range of 1.2 to 11 Earth's radius [14]. Both models give us a static view of the radiation belt (Figure 7). Although they give predictions for solar minimum and maximum, they only provide long term average.

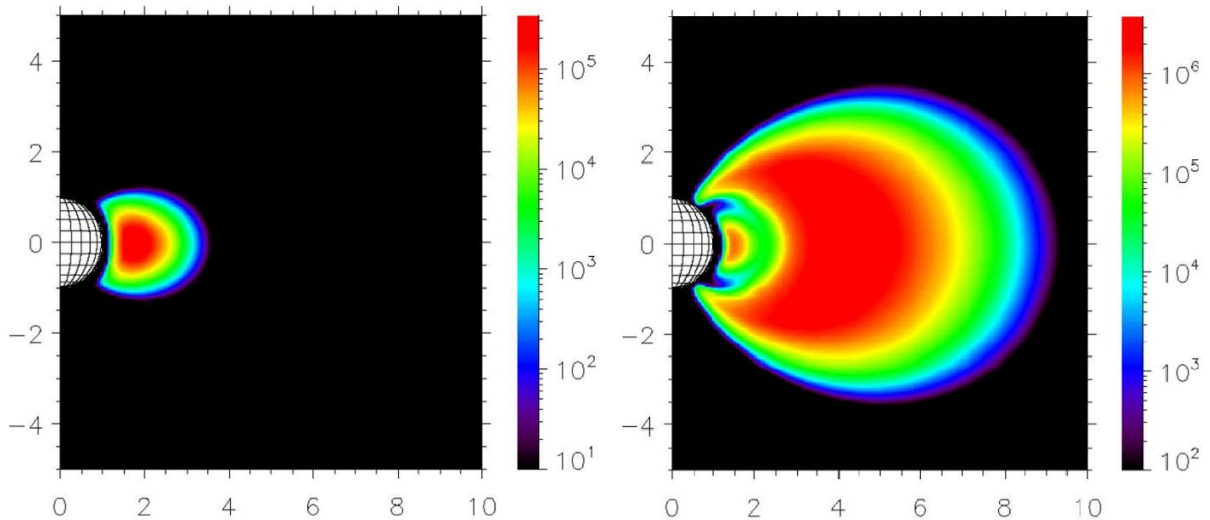


Figure 7: Omnidirectional integrated proton fluxes trapped in the radiation belt from NASA AP8 min model (Energy >10 MeV) (left). Omnidirectional integrated electron fluxes trapped in the radiation belt from NASA AP8 min model (Energy >10 MeV) (right). The mapping is done in magnetic coordinates given here in earth radii. [12]

The models present integral omni-directional electron and proton fluxes as a function of the geomagnetic coordinates  $B/B_0$  and  $L$  (where  $B_0 = 0.311653/L^3$  and  $L$  is the radius where a field-line crosses the equator). At present, AP8/AE8 are still the most widely used model for space engineering, however, it still has some drawbacks in need to upgrade to a better version.

Firstly, the Earth's magnetic field moving causes the SAA to drift primarily toward west-northwest and to a lesser extent north-northeast [15]. Moreover, it's shown that the model curves give significantly lower proton fluxes than the observation data for the inner radiation zone ( $L < 3$ ) [14]. Next, the data collected by the instruments onboard the Combined Release and Radiation Effects Satellite (CRRES) mission showed the variability of trapped environment very different from the static description of the AP8/AE8 models, in particular for the trapped electron. For the low altitude in the region of inner belt, CRRES has detected the maximum electron energy at 30 MeV in comparison with 7 MeV from the model. However, the electron fluxes are overestimated in the outer belt [16].

- New AP/AE model.

In order to upgrade AP8/AE8 model, the new one - AP9/AE9/SPM has been developed by NASA. Currently, through collaboration with international partner, the model will be renamed International Radiation Environment Near Earth (IRENE). The model is also implemented in latest versions of OMERE (CNES/TRAD software). In SPENVIS, this model is also used for evaluation purpose only. Table 2 summarizes the respective model coverages in energy and spatial location.

*Table 2: Species and spatial/energy ranges covered by the AE9/AP9/SPM models (where  $L^*$  is Roederer L-shell and  $L_m$  is traditional McIlwain L-shell) [17].*

<b>Model</b>	<b>AE9</b>	<b>AP9</b>	<b>SPM</b>
<b>Species</b>	e-	p+	e-, H+, He+, O+
<b>Energy</b>	40 keV—10 MeV	100 keV—400 MeV (V1.0-V1.05); 100 keV—2 GeV (V1.20)	1—40 keV (e-); 1.15— 164 keV (H+, He+, O+)
<b>Range in L</b>	$0.98 < L^* < 12.4$	$0.98 < L^* < 12.4$	$2 < L_m < 10$

It consists of a model for trapped protons (AP9), electrons (AE9) and space plasma (SPM). In comparison with previous model, AP9/AE9/SPM models cover a wider spatial and energy range. Moreover, it also implements data-based statistics quantifying uncertainties from both measurement and space weather variability. Furthermore, in order to estimate the worst-case hazards, it also includes dynamic scenarios modelled with Monte Carlo techniques to simulate space weather dynamics including spatial and temporal correlation. Figure 8 shows the comparison between AP8/AE8 and the new model AP9/AE9 for 30MeV proton (left) and 2MeV electron (right).

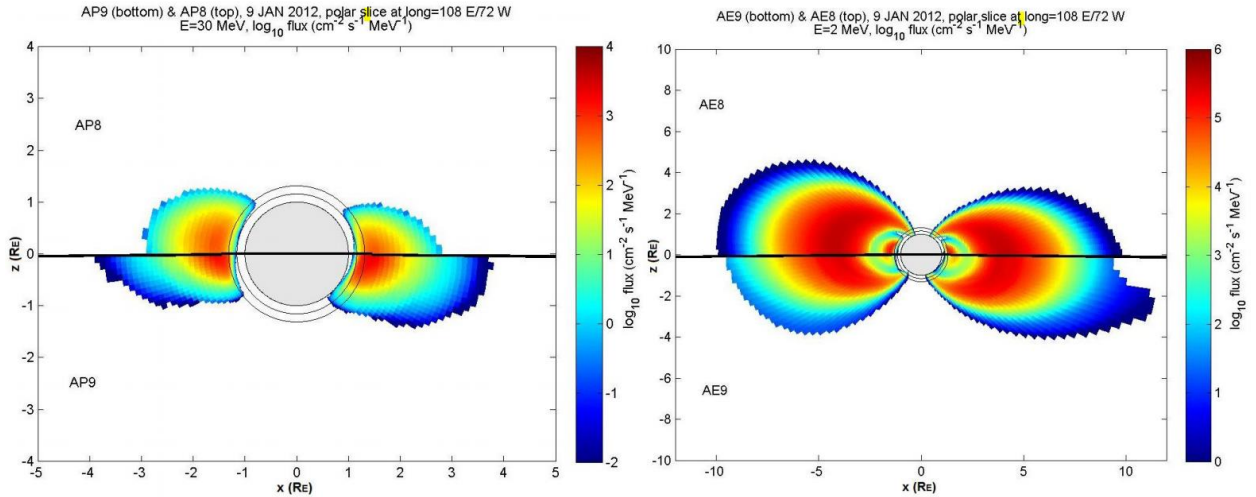


Figure 8: Comparison of AP8 (top) and AP9 V1.05 median (bottom) on a meridional cut through the radiation belts, 30 MeV proton fluxes (left). Same format, but for AE8 (top) and AE9 V1.05 median (bottom), 2 MeV electron fluxes. Axis labels are in units of Earth radii (right)[17].

#### - Local Model

In addition, new local models are introduced for specific region where the AP8/AE8 is not accurate enough. These models are widely diffused thanks to OMERE software. Several models are listed below:

- The “ONERA Protons Altitude Low” (OPAL) model for high energy protons (between  $E > 82$  MeV and  $E > 650$  MeV) at low altitude ( $< 800$  km) [18].
- The ONERA-CNES Slot Electron Model is for electron fluxes in the slot region between  $L = 2$  and  $L = 4$ . It calculates the integrated omnidirectional flux for energies between 0.1 MeV and 3 MeV [19].
- The OZONE model for the outer belt electron with energy from 300 keV to 10 MeV, valid for  $L^* > 4$ , depending on the year of the solar cycle [20].
- The ONERA MEO-V2 model is based on the measurement of radiation monitors onboard GPS platforms and valid for electron fluxes in energy from 0.28 MeV - 1.1 MeV [21].
- The IGE-2006 model is developed exclusively for geostationary orbit at a fixed altitude but is represented by a large  $L^*$  from 5.7 to 7.1 and valid for electron energy from 1 keV to 5.2 MeV [22].
- GREEN (Global Radiation Earth Environment) is a combination of the global models and local models mentioned above. It provides fluxes at any location between  $L^* = 1-8$ , all along the magnetic field lines, for all local times and for electron energy between 1 keV and 10 MeV and proton energy between 1 keV and 800 MeV [23].

### 1.2.3. Solar energetic particles

Apart from the cosmic energetic particles from outer solar system, the Sun actively ejects matter into the vicinity space. They are called Solar energetic particles (SEPs). The main contribution of SEPs are protons, heavier ions, electrons, neutrons, gamma rays and X-rays.

There are two types of solar energetic events that generate these particles: Solar flares and Coronal Mass Ejections (CMEs). Solar flares are the result of the excessed localized energy storage in the coronal magnetic field, then a burst of energy is released when it becomes too large. Meanwhile, Coronal Mass Ejection is a large eruption of plasma and magnetic field from the Sun's corona. Unlike gamma rays and X-ray which travel at the speed of light, hence reach the Earth in about 8 minutes, neutrons and charged particles can take from hours to days after ejection. SEPs is correlated with the solar activity cycle at a period of approximately 11 years. Figure 9 illustrates the periodic nature of solar particle events from the daily solar proton fluences measured by the Interplanetary Monitoring Platform-8 (IMP-8) and Geostationary Operational Environment Satellites (GOES) over a period of about 28 years.

Table 3: Characteristics of CMEs [24].

Hadron Composition	Energy	Integral Fluence (>10MeV/nucleon)	Peak Flux (>10MeV/nucleon)	Radiation Effects
96.4% protons 3.5% alphas ~0.1% heavier ions	Up to ~GeV/nucleon	$> 10^9 \text{ cm}^{-2}$	$> 10^5 \text{ cm}^{-2} \text{ s}^{-1}$	TID DD SEEs

Consisting of various natural elements, SEPs proton and alpha particles can cause permanent damage such as Total Ionizing Dose (TID) and Displacement Damage (DD). Furthermore, a small percentage of heavy ions associated with protons and alpha particles can cause transient and permanent Single Event Effects (SEEs). Solar Particle Events (SPEs) are difficult to predict, however multiple Space Weather initiatives are dedicated to address the problem.

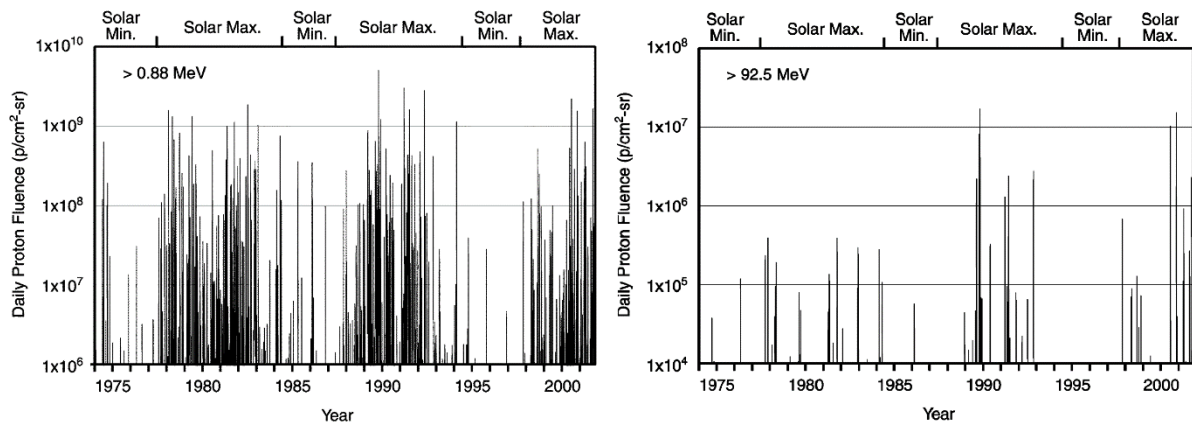


Figure 9: Daily fluences of >0.88 MeV protons (left) and >92.5 MeV proton (right) due to solar particle events between approximately 1974 and 2002 [25].

In order to assess the effect of solar particle events on satellite special for GEO, polar orbit and interplanetary missions, various approaches are used to evaluate the fluence as well as peak fluxes. They include a cumulative fluence of the mission, fluence of worst-case event, frequency distribution of event fluences and the frequency distribution of large peak fluxes.

The model currently used for the SEP is the Emission of Solar Protons (ESP) model for the estimation of long term cumulative proton fluence [26] which is provided in ECSS E-ST-10-04C [27]. The ESP replaces two commonly used: SOLPRO model [28] based on King's analysis of spacecraft measurements from solar cycle 20 data and a model from JPL [29] which was initially based on ground data from solar cycle 19 and spacecraft measurements from solar cycles 20 and 21. The ESP model provides worst-case peak flux and event-integrated fluence spectral models at user-specified confidence levels based on data from solar cycles 20 to 22 [30], [31]. The study in [32] showed the cumulative fluence of heavy ions from solar activity exceeds galactic cosmic rays during the solar maximum. The Prediction of Solar particle Yields for Characterizing Integrated Circuits (PSYCHIC) model is for heavy ion fluxes from solar events that includes the cumulative solar heavy ion fluences for almost all natural elements during the solar maximum activity [32]. The comparison between models of cumulative solar proton event fluences is shown in Figure 10.

Recently, the Solar Accumulated and Peak Proton and Heavy Ion Radiation Environment (SAPPHIRE) model developed through ESA's (Solar Energetic Particle Environment Modelling (SEPEM) application server is proposed to become part of ESA's standard in the future. It covers all SEP environment timescales across all relevant species in a consistent probabilistic manner. The model provides set of outputs including: mission cumulative fluence; largest Solar Particle Event (SPE) fluence; SEP peak flux [8].

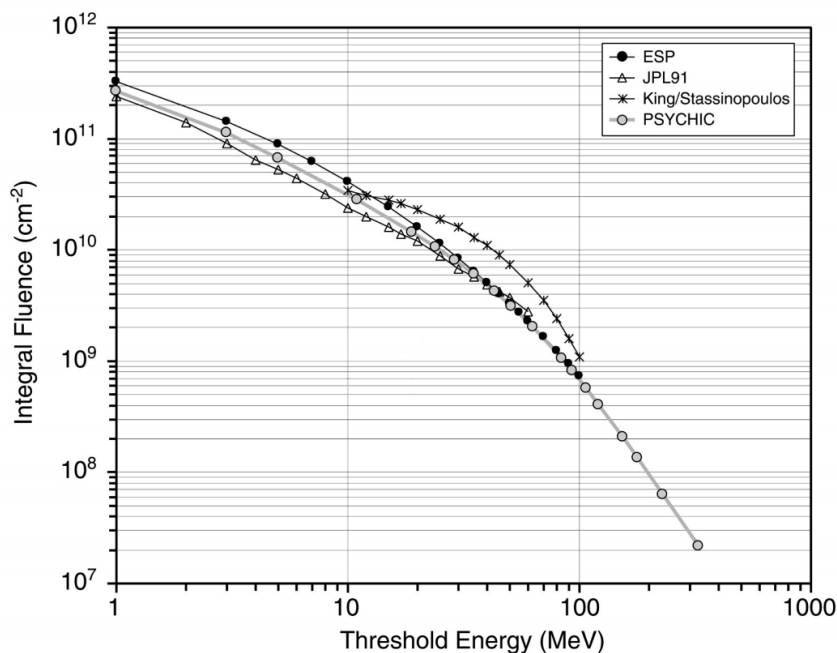


Figure 10: Comparison of different models of cumulative solar proton event fluence during solar maximum for a 2-year period and the 90% confidence level [33].

### 1.3. Radiation effects on electronics devices

The complexity and dynamics of space environment pose a threat to both satellites and spacecraft working on orbit. Its effects are not only on the material surface but also in the onboard electronics devices. This part will give an overview of the radiation effects on electronics devices under harsh environment such as space. In order to generalize the radiation

environment, following particles are considered: photons, charged particles (electrons, positrons and heavy ions) and nucleus (protons and neutrons).

Photon's interactions include:

- Photoelectric is when the photon's energy is absorbed by inner shell electron, then the electron gets excited and emitted from the atom.
- Compton scattering is an incoherent scattering as the photon transfers a portion of its energy to the electron and gets it emitted from the atom
- Rayleigh scattering is a coherent scattering as the photon retained its energy after the interaction.
- Pair production occurs when photon interacts with the electric field of the atomic nucleus. The photon annihilates while an electron and a positron are produced. The incoming photon must have an energy of at least 1022 keV to have pair production.

Photon interactions are mainly in Xray and gamma ray. It's used in laboratory source to simulate a total-dose space environment. The main effect of photon interactions is the creation of a secondary electron.

A particle loses its energy by interacting with either an electron or the nucleus of an atom. The stopping power is used to express the energy loss of particle per unit of length  $dE/dx$ . Equation (1.1) shows the stopping power of charged particles from three contributed interaction: ionizing, non-ionizing and radiative process. The ionizing interaction creates free charges in the material, while the non-ionizing interaction displaces atom's position from lattice.

$$-\left(\frac{dE}{dx}\right)_{total} = \left(-\frac{dE}{dx}\right)_{electron} + \left(-\frac{dE}{dx}\right)_{displacement} + \left(-\frac{dE}{dx}\right)_{radiative} \quad (1.1)$$

The electron and its antiparticle interaction include:

- Elastic interaction is a coulomb interaction with an atomic nucleus screened by the atomic electrons. The characteristics are the kinetic energy conserved and recoil energy is weak.
- Inelastic interaction is the interaction that produces the electronic excitation and ionization. In contrast with elastic interaction, the kinetic energy is not conserved.
- Bremsstrahlung emission is the deceleration of an electron (or a positron) in the electric field that leads to the emission of a photon.
- Cerenkov emission happens when a charged particle passes through an insulator at a speed greater than the speed of light in the medium.
- Positron annihilation occurs when a positron penetrates a medium and annihilates with electrons by the emission of two photons.

There are two main effects when ions and nucleons interact with matters: elastic and inelastic collision. Table 4 summarizes the different types of interactions.



Table 4: Interaction between energetic particles and matter summary.

Particle	Photons	Electrons, positrons	Ions	Nucleons
Processes	Rayleigh Photoelectric Compton Pair production	Elastic Inelastic Bremsstrahlung Cerenkov Annihilation	Elastic Inelastic	Elastic Nonelastic
Secondary particles	e-, e+, photons	e-, e+, photons	Ions, e	Ions, photons, nucleons (pion etc..)

Among the various complex interactions of radiation in materials, there are two main consequences in term of effects on electronics devices: Cumulative effects including Total Ionizing Dose (TID) and Displacement Damage (DD); Single Event Effects (SEEs).

### 1.3.1. Cumulative effects

Both TID and Single Event Effects (SEE) are originated from ionizing radiation. However, TID is a cumulative effect that takes a long time to accumulate impacts on devices, whereas, SEE is an instantaneous mechanism that can induce immediate failure of the devices. This part will discuss about cumulative effects in semiconductor devices.

#### 1.3.1.1. Total Ionizing Dose (TID)

Ionization of matter occurs when high energy particles interact with the atom of the target material. Photon-induced ionizing damage started with the emission of secondary electron from the photon-matter interaction along the track to generate electron-hole pairs, other charged particles can also directly create electron-hole pairs that lead to ionization damage. The energy required to create electron-hole pair in specific materials are listed in Table 5. The density of electron-hole pair generated by TID can be calculated as follows:

$$N = \frac{TID \times \rho}{E_p} \quad (1.2)$$

where TID is the total dose,  $\rho$  is density of the material and  $E_p$  is electron-hole pair generation minimum energy.

The ionizing effect is generalized as Total Ionizing Dose which implies the energy deposited per unit mass. The official unit of TID is Gray (Gy), however, between the radiation effects community rad is used more frequently, which can be converted to: 1 Gy = 1 J/kg = 100 rad.

Table 5: Minimum energy required to create electron-hole pairs and densities of pairs created per unit dose in different materials (GaAs, Si, SiO<sub>2</sub>) [34].

Material	$E_p$ (eV)	Density (g/cm <sup>3</sup> )	Pair density generated per rad, $g_0$ (pairs/cm <sup>3</sup> )
GaAs	~4.8	5.32	$\sim 7 \times 10^{13}$
Silicon	3.6	2.328	$4 \times 10^{13}$
Silicon Dioxide	17	2.2	$8.1 \times 10^{12}$

When an energetic particle passes through material, it loses energy along its travel distance. Previously, we mentioned about the stopping power, however, in order to have a stopping power which does not depend on the state of material, we can device the stopping power by material's volume mass to obtain mass-stopping power or so call Linear Energy Transfer (LET).

$$LET = -\frac{1}{\rho} \left( \frac{dE}{dx} \right)_{total} \quad (1.3)$$

The stopping power is often expressed in  $MeV \cdot cm^2/mg$ . The electronic stopping power and nuclear stopping power can be calculated for different incident particles and materials using SRIM/TRIM code [35].

- Mechanisms:

One of the main effects of ionization damage in semiconductor devices is the accumulation of trapped-charges inside the insulation layer that will interfere with their standard operation regimes. Major studies have been focused on the metal-oxide semiconductor (MOS) technologies because of the thin oxide silicon layer of gate oxide on the active semiconductor channel. However, as technology nodes keep decreasing, the concern is also applied to bipolar technologies in connection with trapped-charges-induced leakage paths near the field and passivation oxides [36].

The physical mechanisms of ionization defects in Silicon-Oxide can be described as Figure 11. First, the incident radiations generate electron-hole pairs, following by initial recombination of generated electron-hole pairs and then high mobile electrons will be transported to the gate and collected. Holes with low mobility will be slowly transported by hopping to the Silicon-Oxide/Silicon interface, where a fraction will be trapped in the oxide bulk due to O vacancies and lattice mismatch between SiO<sub>2</sub> and Si. The trapped holes form positive trapped charges close or at the SiO<sub>2</sub>/Si interface region [37]. The oxide-trapped charges can be neutralized over time by two mechanisms: electrons tunneling from the silicon into the oxide traps and/or thermal emission of electrons from the oxide valence band into oxide traps [38]. The activation energy of these mechanisms is quite low therefore a significant annealing of oxide-trapped can occur during a long radiation exposure period.

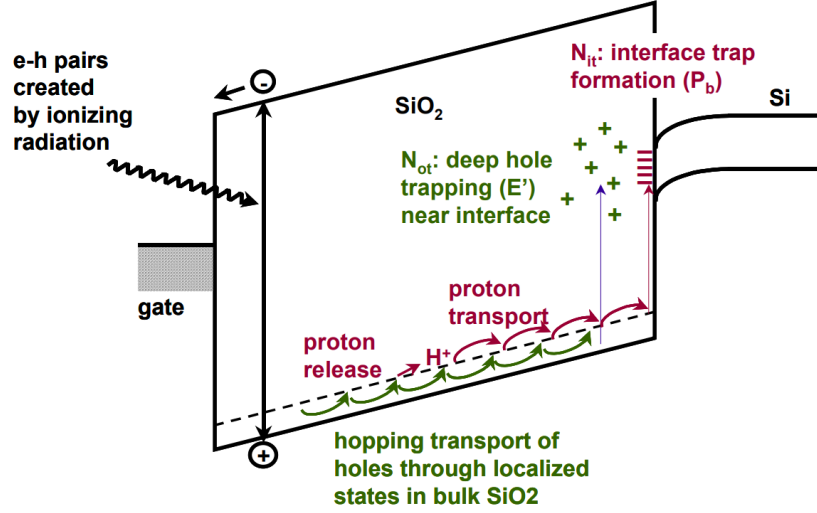


Figure 11: Illustration of the main processes for radiation-induced charge generation in the band diagram of an MOS structure in the presence of a positive gate bias [39].

During the transportation of holes by hopping, reactions between the holes and hydrogen-containing defects or doping complexes can release hydrogen ion (proton or hydrogen-related). The hydrogen ions can accumulate at the SiO<sub>2</sub>/Si interface and form an ionization defect called the interface trap [37]. The traps at interface can be modified by applying an external bias. The interface traps in the upper half of the band gap are dominant by acceptor type hence the traps are positive charged, whereas, the traps in the lower part of the band gap are donors and the traps are negatively charged [40]. The trapped carriers and interface traps are the main cause of the total dose effects where the properties of device are affected by radiations.

#### - Total Ionizing Dose Effects on MOSFET

In order to evaluate the electrical response of the MOS transistor to TID, the drain current versus the gate voltage ( $I_d = V_{gs}$  curves) is studied. Figure 12 shows the  $I_d = V_{gs}$  curves before and after radiation for both n-type and p-type MOS devices. The effects of trapped charges inside the gate oxide and/or at the gate-oxide/silicon interface is a shift of the CMOS transistors threshold voltage. The shifting threshold  $\Delta V_T$  can be determined by equation (1.4):

$$\Delta V_{ot,it} = \frac{-1}{C_{ox}t_{ox}} \int_0^{t_{ox}} x\rho(x)dx \quad (1.4)$$

where:  $C_{ox}$  is the gate capacitance,  $t_{ox}$  is oxide thickness and  $\rho$  is the charge density.

As mentioned earlier, the oxide traps are positively charged, so the threshold voltage shift by the oxide traps  $\Delta V_{ot}$  for both NMOS and PMOS are always negative which mean a shift of the curve to the left. However, for interface traps, threshold voltage induced by interface traps  $\Delta V_{it}$  is positive for NMOS transistors, and negative for PMOS transistors. Hence, the net threshold voltage shift  $\Delta V_T$  will be the sum of  $\Delta V_{ot}$  and  $\Delta V_{it}$  which is illustrated in Figure 12.

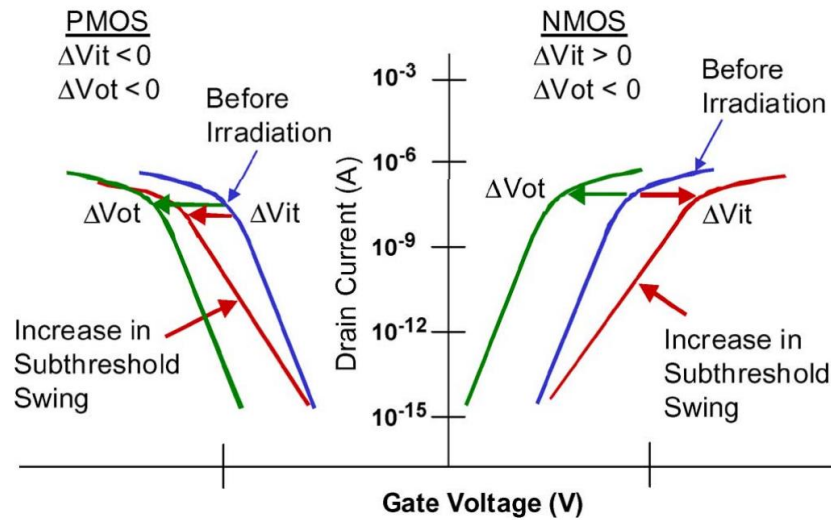


Figure 12: Threshold voltage shifts and subthreshold swing changes for NMOS and PMOS transistor relative to before irradiation curve [41].

### 1.3.1.2. Displacement Damage (DD)

In addition to the ionization effect, high-energy particles can cause non-ionization effect or so-called displacement damage in semiconductor materials by interacting with the nucleus of the atom.

- Mechanisms:

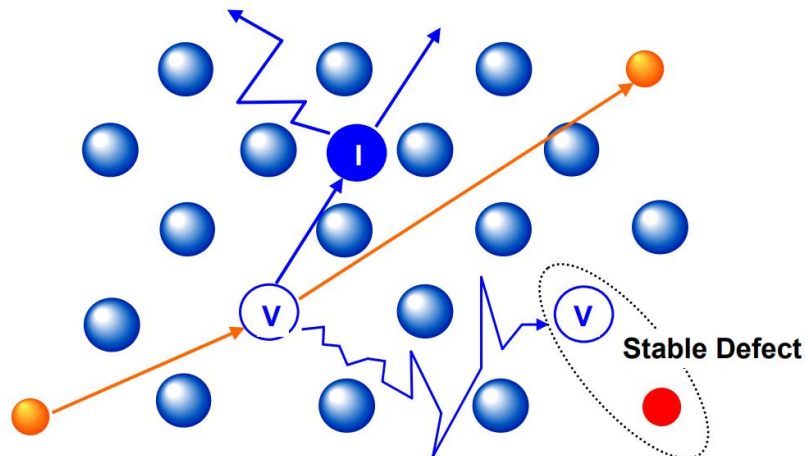


Figure 13: Illustration of displacement damage [42].

During irradiation interaction, the atoms can be knocked out of its position in the lattice and create permanent defects. The mass-stopping power is called Non-ionizing energy loss (NIEL) and is defined as the amount of energy loss per unit of length.

$$NIEL = -\frac{1}{\rho} \left( \frac{dE}{dx} \right)_{nuclear} \quad (1.5)$$

where:  $\rho$  is the density of the material and  $\left(\frac{dE}{dx}\right)_{nuclear}$  is the rate of energy loss in the material from non-ionizing processes. NIEL is expressed in units of  $\text{keV}\cdot\text{cm}^2/\text{g}$ .

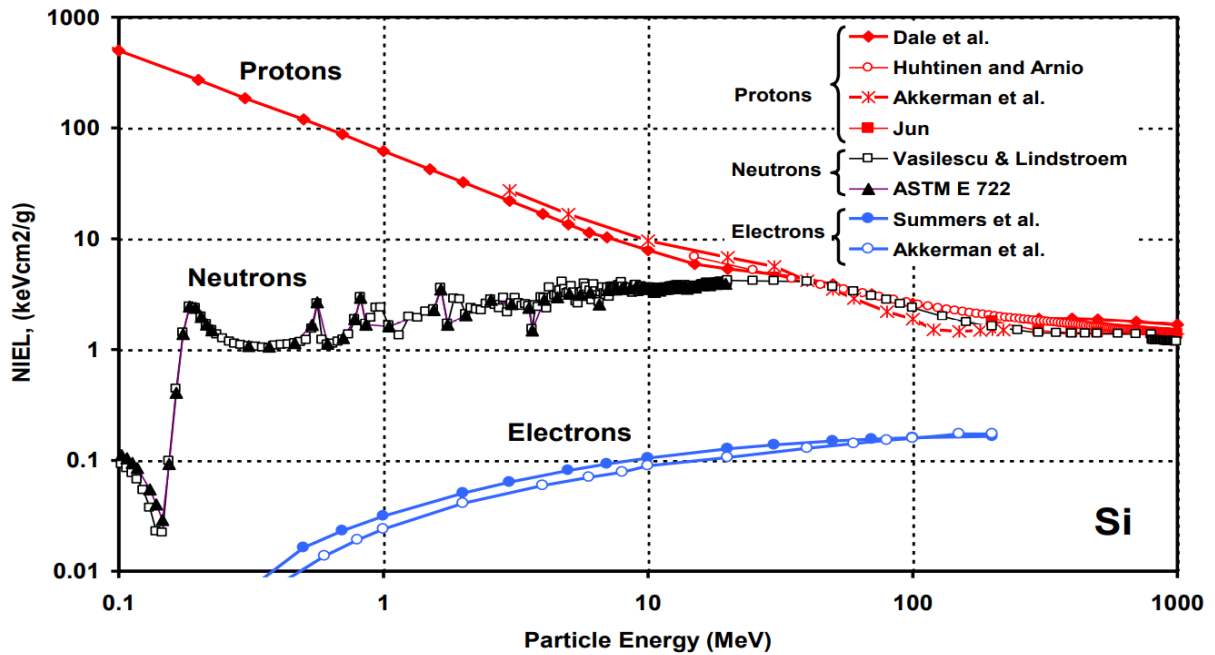


Figure 14: Non-ionizing energy loss in silicon [42].

The Displacement Damage Dose (DDD) or (TNID - Total Non-Ionizing Dose in space standard) term is used to describe the exposure of the material to the particle fluence and can be calculated by multiplying the NIEL of the particle with total fluence. It also can be expressed as the Displacement Damage Equivalent Fluence DDEF for mono-energetic beam i.e.,  $10\text{MeV}$  proton/ $\text{cm}^2$  or  $1\text{MeV}$  neutron/ $\text{cm}^2$ . Figure 14 shows NIEL in silicon for different particles and energies. To displace an atom permanently, incident particle must have sufficient kinetic energy to break the chemical bond and move it far away from its original position so that it does not retract immediately. The minimum energy required is called displacement threshold energy, in silicon the value  $E_d = 21\text{eV}$  is generally well admitted for protons, neutrons and heavy ions [43].

When the incident particle imparts enough energy, the target atom - Primary Knock-on Atom (PKA) is pushed to an unoccupied position. The empty place left behind is called vacancy and displaced atom is called interstitial, together they also called Frenkel pair. If the PKA has enough energy it can displace the second atom (SKA) and possibly more until the energy it can transfer is below the threshold. If the energy is large enough, the recoil energy in turn repeats the process and creates a cascade of defects inside matter. As it passes through the target material, PKA loses its energy and changes trajectory. At the end of the deflected atom path, a large cluster of defects may form (terminal cluster).

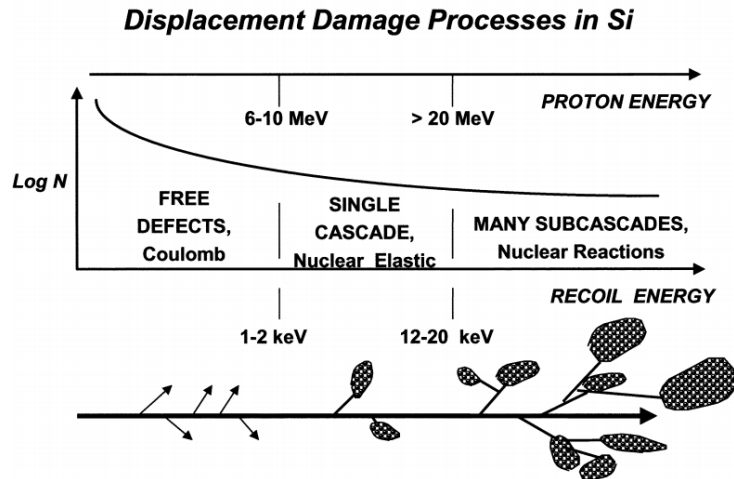


Figure 15: The relationship between defect cascade structure in Si and the primary knock-on atom (PKA) energy, predicted by Monte Carlo calculations [44].

A study by Wood et.al. [44] shows (Figure 15) the relationship between defect cascade structure in Si and primary knock-on atom (PKA) energy, predicted by Monte Carlo calculations. For recoil energies below 2 KeV, only point defects are produced. For higher recoil energies, sub-cascade clusters of defects are formed. Additionally, vacancies and interstitial can form adjacent to impurity to create defect-impurity complexes, for example the vacancy-phosphorus pair. Figure 16 illustrates defect cascade structure for a 50 keV Si recoil showing the overall dimension of the damage.

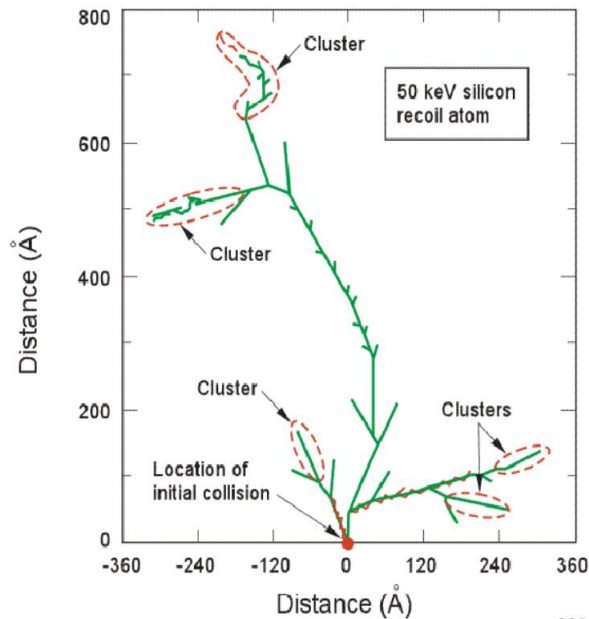


Figure 16: Defect cascade structure for a 50 keV Si recoil showing the overall dimension of the damage [42].

- Displacement damage effects on devices

Displacement damage induces a disturbance of lattice periodicity and may provide new energy levels in the bandgap. These defects states have major impact on the electrical properties

of semiconductor material and devices. Different effects of the defects created by radiation are discussed below.

The first is thermal generation of electron-hole pairs through an energy level near mid-gap. Electrons from valence band can get thermally excited to jump to the defect centers and subsequently to the conduction band to create a free electron-hole pair. However, only generation center with energy levels near mid-gap contributes significantly to the carrier generation rate. Moreover, the emission processes dominate capture processes when the free carrier concentration is much lower than the thermal equilibrium values, therefore the generation center of the defects is very impactful when it is situated in the depletion region of the device. Such centers increase the thermal generation rate, which in turn increases the leakage current of the devices.

Secondly, it is the recombination of electron-hole pairs. Free carriers can be captured by the defect center, then the carrier on the opposite side can be captured and recombined with the previous one. In general, the recombination process removes the electron-hole pair and hence reduces the minority carrier life time. This mechanism is responsible for the gain degradation of the bipolar transistor.

The next effect is the temporary trapping of the carriers at a typically shallow energy level. The introduction of an energy level close to the band can capture a free carrier and then re-emit to its band. The main effect is the reduction of the transfer efficiency in charge-coupled devices. The compensation of donors or acceptors by radiation-induced defect centers. The consequence is the reduction of the equilibrium majority-carrier concentration. Defect centers can also increase the tunneling of carrier rate through the band gap, which increases the leakage current.

To summarize, the radiation induced defects create new energy level in the band gap. As a result, they alter the behavior of devices by multiple mechanisms including generation, recombination, trapping, compensation, tunneling (Figure 17). The level of effectiveness depends on variables such as carrier concentration, temperature, and position in the device.

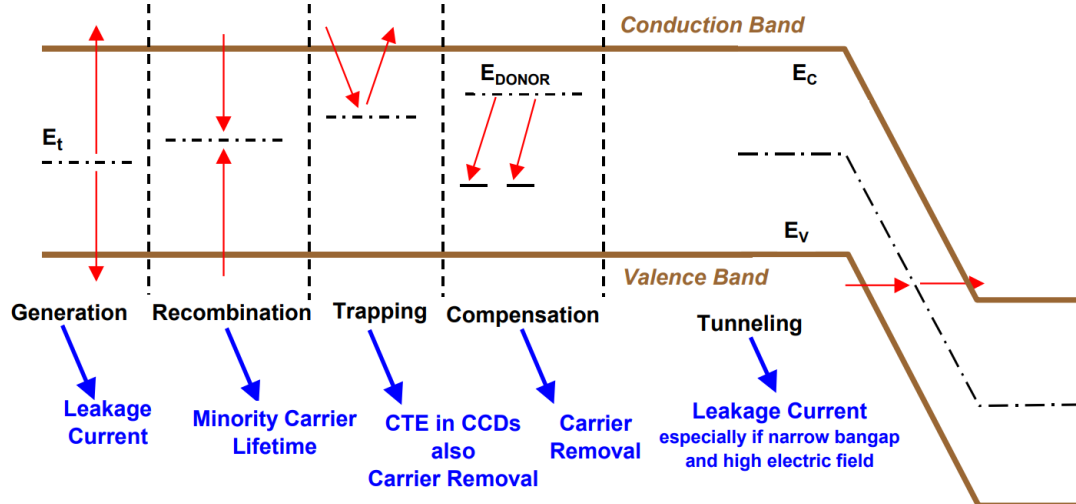


Figure 17: Effects of displacement damage in semiconductor devices [42].

Among those physical effects, the affected electrical devices can be divided into two groups:

- Bipolar transistors, optoelectronics and solar cells
- Visible imaging arrays

Bipolar junction transistor are minority carrier devices; hence displacement damage will degrade the gain and increase the leakage current. Optoelectronics devices include light-emitting diodes, photodiodes and phototransistors will degrade their performance when generation and recombination centers are introduced into the bandgap of the semiconductor. The dominant effect of displacement damage in solar cell material is the reduction of minority-carrier lifetime, which reduces the power output and efficiency.

Imaging sensors such as Charge-Coupled Devices (CCD), Active Pixel Sensors (APS) or CMOS Image Sensors (CIS) are susceptible not only with TID, SEE but also DD. The main effect of displacement damage in those devices is an increasing of the dark current both in terms of mean value and distribution. Many studies used APS and CIS to study the displacement damage effects on silicon thanks to the individual readout mechanism of these devices. The results suggest that the increasing in the dark currents can be mentioned as: increasing in the minority carrier [45], generation rate induced from points defect [46] and recent studies are focusing on the cluster of defects which will be discussed below.

#### - Models of Single Particle Displacement Damage in Silicon

In order to study the effects on minority carrier life time for post irradiation devices, various properties of the defect are required. That information includes the energy levels introduced in the band gap, the defect concentration, the capture and emission rate of electrons and holes for each level, the temperature dependence of these probabilities and various charge states for each defect [43]. Therefore, building the model for the defect is helpful to establish a correlation with the experimental data. One of the first models for defects is Gossick model [47]. Gossick et.al. proposed a model to account for differences between point defects and cluster of defects. This model proposed the properties for nano size defects cluster as following. The damaged region is considered as a spherical shape with its own density, energy level; the cluster dimension is around 20nm~100nm and the concentration of traps is around  $10^{18}$ - $10^{20}$  cm<sup>-3</sup>. However, the original Gossick model for a rather large cluster of defects (200nm) is not supported by more recent works.

The most recent work has gone into the detail of the creation of the defect cascade using the approach of combining different simulations.

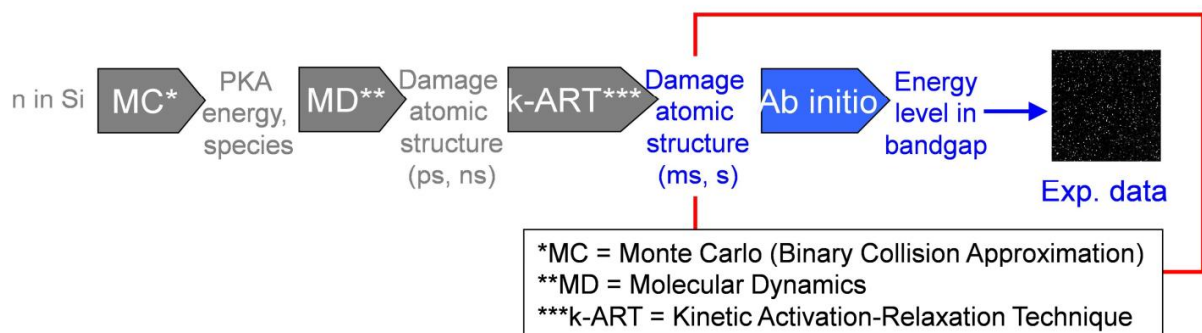


Figure 18: Schematic of the global simulation project [48].

The novel simulations (described in Figure 18) of Antoine Jay et.al. start with Monte Carlo simulations of the interactions of incident particles in Silicon to acquire realistic PKA (Primary Knock-on Atom) energies. Then the large statistics of PKA are used as input for Molecular



Dynamic (MD) simulation. MD is used to identify PKA's trajectory and the formation of the defect cascade [48]. The next step is to study the evolution of the defects on a larger scale using the kinetic Activation-Relaxation Technique (k-ART). This method is used to overcome the timescale limit of the classical MD simulation, hence providing an overview of more stable defects and defect clusters [49]. Finally, first principle calculations (also called as ab initio calculation) are used to characterize the damaged structures obtained at the end of the k-ART step [50].

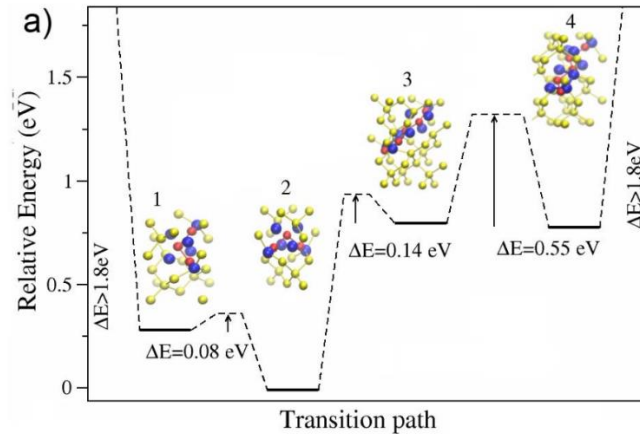


Figure 19: An example of simple flickering configuration: the tri-interstitial. The four configurations, their relative energy and the energy barrier [49].

The initial results gave us [50]:

- The clusters are mainly formed of small defect centers such as di-, tri- and quadri-vacancies and tri- and quadri-interstitials (2 to 4-V and 3 to 4-I respectively).
- One defect center can shift between configurations due to thermal excitation and low barrier between them. This flicker effect is believed to be the source of Random Telegraph Signal Dark Current (RTS DC) in image sensors.
- The cluster size distribution presents an exponential shape similar to the shape of the DC distributions experimentally measured in image sensors.

### 1.3.2. Single Event Effects

Beside cumulative effects, single event effects are growing concern for modern digital electronics. This part will discuss how a single particle can trigger a malfunction in semiconductor devices.

- Mechanism

When a single energetic particle interacts with microelectronics devices it can ionize the material in two ways: direct ionizing by the particle itself and indirect ionizing by secondary particles created from the nuclear reaction between the incident particle and the target material (Figure 20).

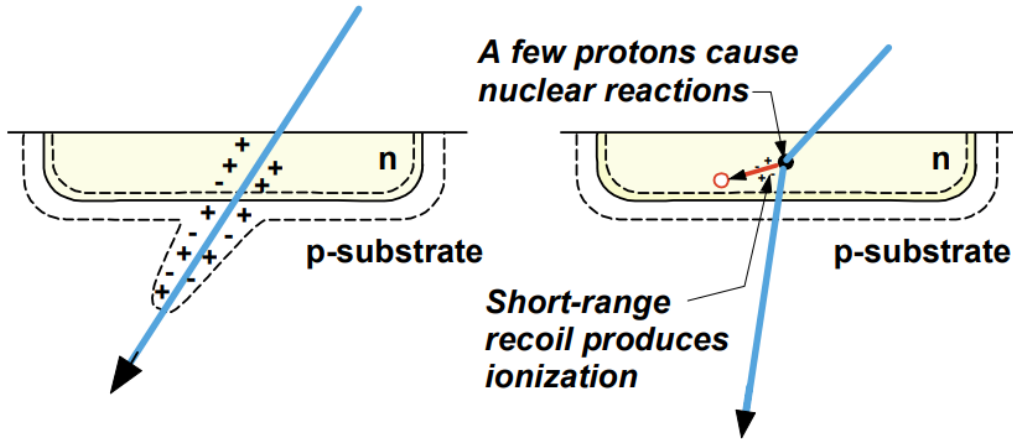


Figure 20: Two mechanism of SEE direct (left) and indirect (right) [51].

For direct ionizing, the high energy particle creates a free carrier along the trajectory before stopping in the material. The LET is used to describe the rate of energy loss per unit length and the total travel distance of particle inside material is called a range. Before coming, the LET of the particle reaches a peak towards the end of its track, referred as Bragg peak. Figure 21 shows LET of different ions in silicon, we saw that the higher the LET, the shorter the range of the particle.

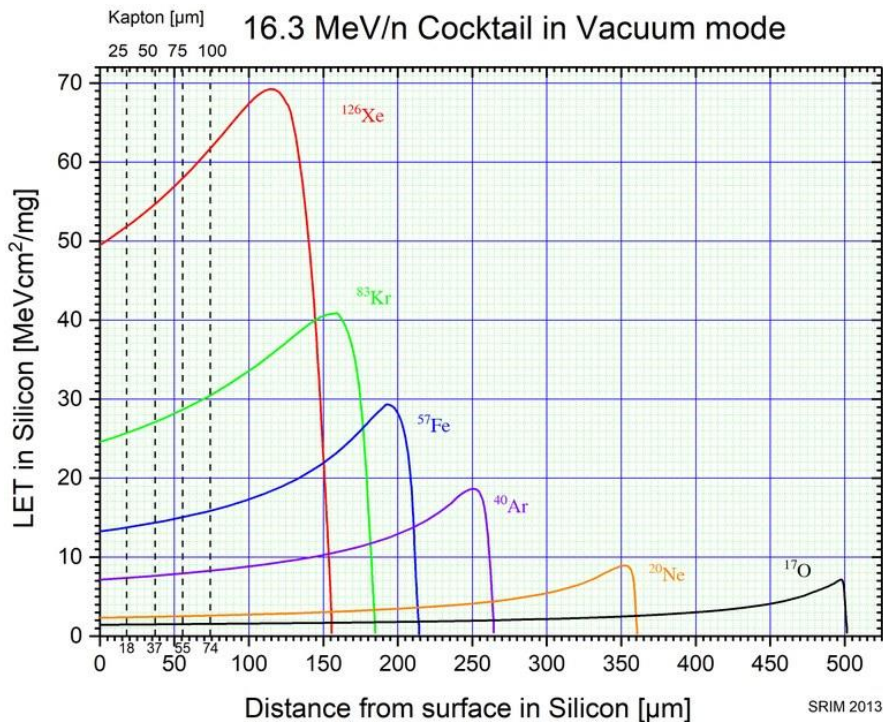


Figure 21: LET curves of 16.3 MeV/u cocktail ions in silicon vacuum mode. Vertical dash lines show the effective DUT surface positions when 25, 50, 75 and 100  $\mu\text{m}$  of Kapton is added front of the DUT [52].

Charge deposited per unit length can be calculated as equation (1.6):

$$Q_{dep} = 1.6 \times 10^{-2} \times \frac{\rho \cdot LET}{E_p} \quad (1.6)$$

where:  $\rho$  is the density of the material,  $E_p$  is the threshold energy for the creation of electron-hole pairs.

For indirect ionizing, when the incident particle not have enough energy to trigger direct ionizing, it can still trigger a nuclear reaction. That process produces recoiled fragments of target nucleus and alpha or gamma particles emission. These byproducts can in turn directly ionize the material along their path.

Charges that have been deposited along the path from particle strikes can be collected and disrupt the normal operation of the devices. Charge collection depends on the type of ion, its trajectory, and its energy along the track. Therefore, the term sensitive volume is defined as the region responsible for charge collection for a SEE. One of the most sensitive regions in a circuit is the reverse-biased junction, such as the drain area in a bulk MOS transistor. Along the track of the incident particle, a cylindrical of high-density electron-hole pairs is formed within a submicron radius. The free carrier close to the depletion area is collected due to the electric field, creating a transient current on the node. A simultaneous distortion of the potential forms a funnel shape that greatly enhances the efficiency of the drift current by extending the high field depletion region deeper into the substrate. The prompt charge collection phase happens within nanosecond scale then continues with the collection of charge by diffusion. Electrons slowly diffuse into the depletion region and all excess carriers have been collected, recombined, or diffused. Figure 22 shows the processes and the corresponding current diagram.

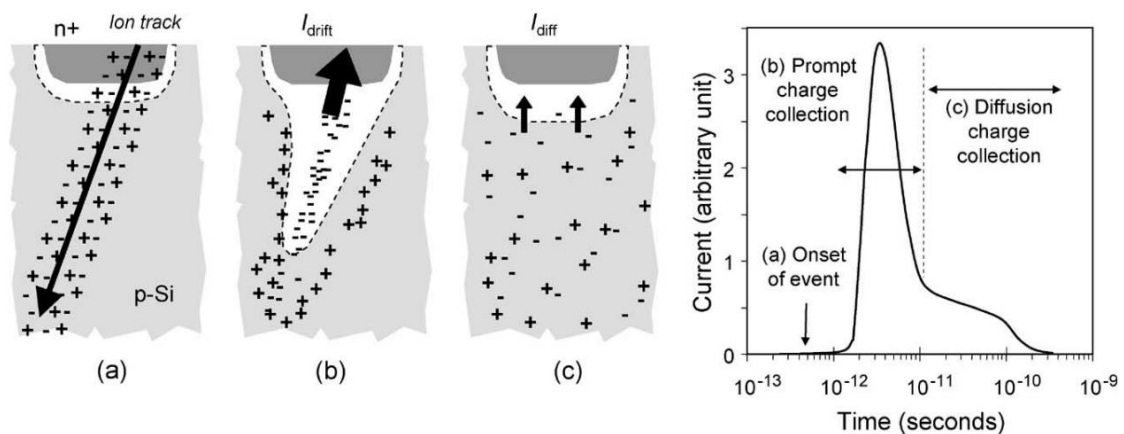


Figure 22: Charge generation and collection phases in a reverse-biased junction and the resultant current pulse caused by the passage of a high-energy ion [53]

- Single Event Effects on devices.

Single Event Effects in electronics devices are classified in two categories destructive or hard error and in-destructive or soft error.

The most common destructive events can be mentioned: single-event latch-up (SEL), single-event burnout (SEB) and single-event gate rupture (SEGR). Almost all CMOS silicon devices contain both n and p types have the appearance of parasitic p/n/p/n structures. When these structures are activated by the injection of ion-induced charges into the n-well, an abnormal high-current state will occur within the device: this is the Single Event Latch-up (SEL) illustrated in Figure 23. If the current is not removed quickly enough, the devices will be damaged by thermal runaway or failure of metallization [54].

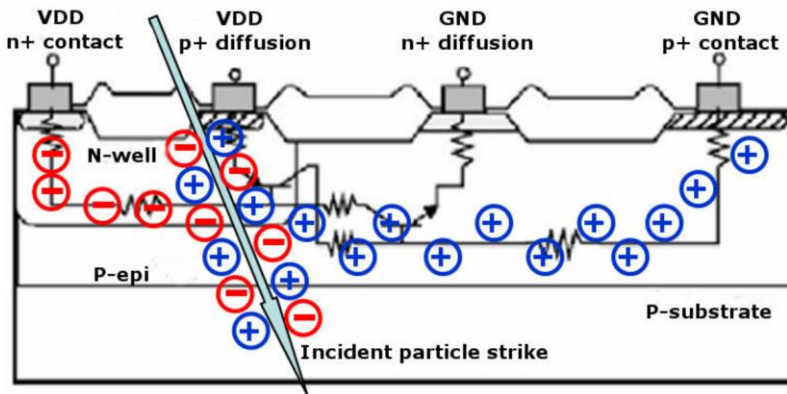


Figure 23: Initial electron-hole pairs and current tracks created by incident particle strike SEL [54].

Single-Event Gate Rupture (SEGR) and Single-Event Burnout (SEB) occur mostly in power devices. A SEGR permanently damages the gate insulator layer (dielectric breakdown) hence disrupts its ability to control current. Condition for SEGR is when the ion strikes vertically with respect to the devices (Figure 24 left). Along the ion track, electron is quickly swept toward drain contact, meanwhile holes accumulate close to Si/SiO<sub>2</sub> interface hence a temporary increase of electric field can breakdown gate oxide.

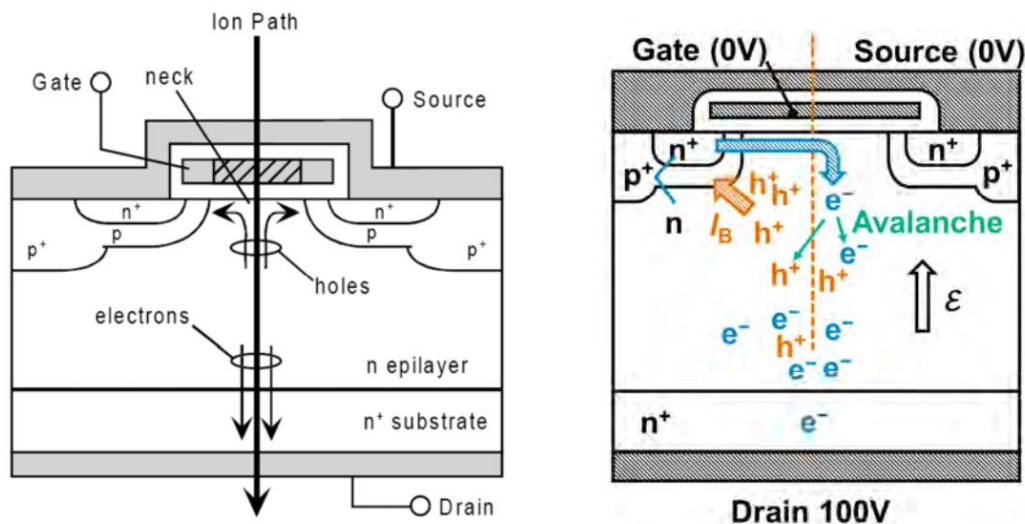


Figure 24: Structure of a vertical power MOSFET and current flow paths following a heavy ion strike, illustrating the onset of a SEGR event (left) and a SEB event (right) [55].

On the other hand, SEB does not damage the insulator but increases abruptly the source-to-drain current. SEB is triggered at a parasitic bipolar transistor form by n-source (emitter), p-body (base), and n-epitaxial (collector) regions of the device (Figure 24 right). When charge is released by an ion strike within the neck region of device, the parasitic transistor is active forward, and at high drain voltage an avalanche of collector current can occur that will lead to thermal issue and burnout of the devices.

There are many in-destructive errors or soft errors that can be mentioned: Single Event Transient (SET), Single Event Upset (SEU), Single Event Functional Interrupt (SEFI). As mentioned above, when a ion interacts with a microelectronics device, it deposits charges

within the material and can be collected and induce a transient current. This transient current may propagate along the system logic gates. It can change a memory element or give an additional false input to the memory element if it arrives before a clock edge.

Single Event Upset is the consequence of charge built up from the interaction that changes the logic state within memory elements, it's also called bit-flip. Moreover, single particle can impact multiple bits create Multiple bits upset (MBU). The phenomena can affect data integrity of all kind of memories including: DRAM, SRAM, Flash, flip-flop etc.... The details will be discussed in more detail in the next session.

Keeping up with device scaling trend, integrated circuit becomes more complex hence a single strike at particular area of control circuit can alter the normal operation of the devices. This is called Single Event Function Interrupt (SEFI).

## **1.4. Weakened cells phenomenon**

Among various effects on microelectronics devices induced by radiation, weakened cells have recently caught the eyes of researcher because of their abnormal behaviors. In previous works done by Axel Rodriguez, the phenomenon had been studied on both SRAM and DRAM devices. While, Axel proved that weakened cells observed on SRAM is mainly due to microdose and will not affect future generation, weakened cells on DRAM still have so many open questions [56]. This section will discuss how the phenomenon is observed and related studies.

### **1.4.1. Weakened cell behavior observation**

Observed on CARMEN2 experiment and PICARD satellite, the DRAM devices exposed to radiation environment showed the appearance of Single Event Upset. However, increased occurrence of SEU was observed in some specific addresses. These memory cells are more sensitive than the rest of the device with the same bits have been corrupted over time. Additionally, the corrupted bit can be rewritten therefore it's not considered as hard error - stuck bit. This effect has been called weakened cell [57], [58]. In Figure 25, multiple addresses started to show error and then stopped and sometimes it started to show error again, for example, in the case of address 57DFB8BC (green).

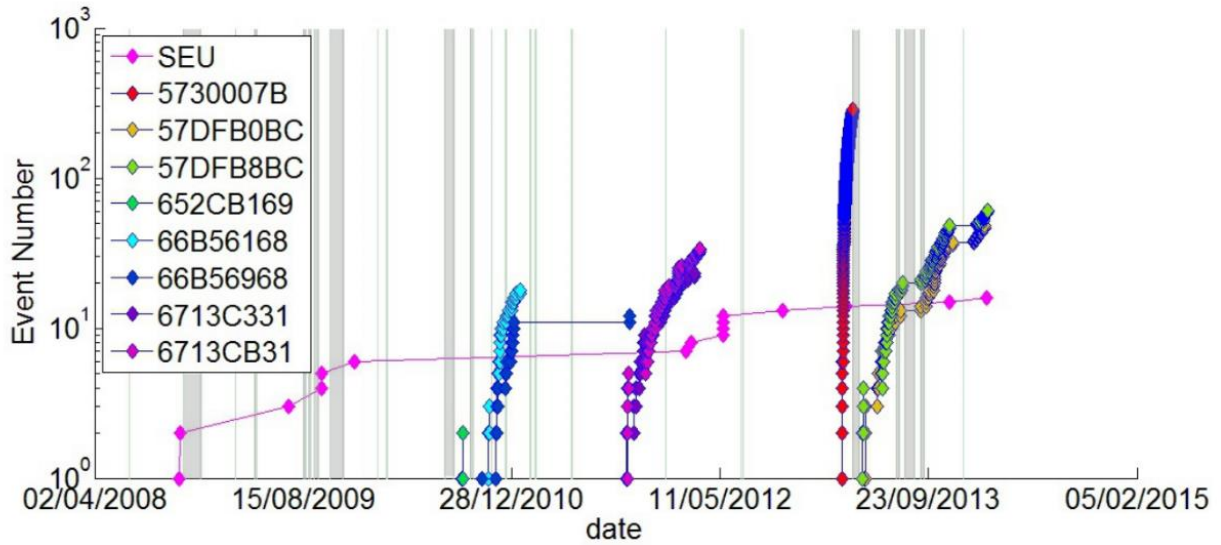


Figure 25: MMSD08512408S-Y Z35 on CARMEN experiment, Number of soft errors in function of the time and in function of the address for weakened cells [57].

The same behavior is also observed on PICARD satellite in LEO (Sun-synchronous near-circular orbit, altitude of 735 km), Figure 26 shows the cumulative number of upsets and the cumulative error number of each weakened cell addresses as the time evolution. The grey parts indicate that the error detection code onboard does not work to collect the data. Taking the address B7E418 for example, it started to be upset in 07/04/2011 then experienced multiple times of non-upset that lasted for hours to days then it showed the error again.

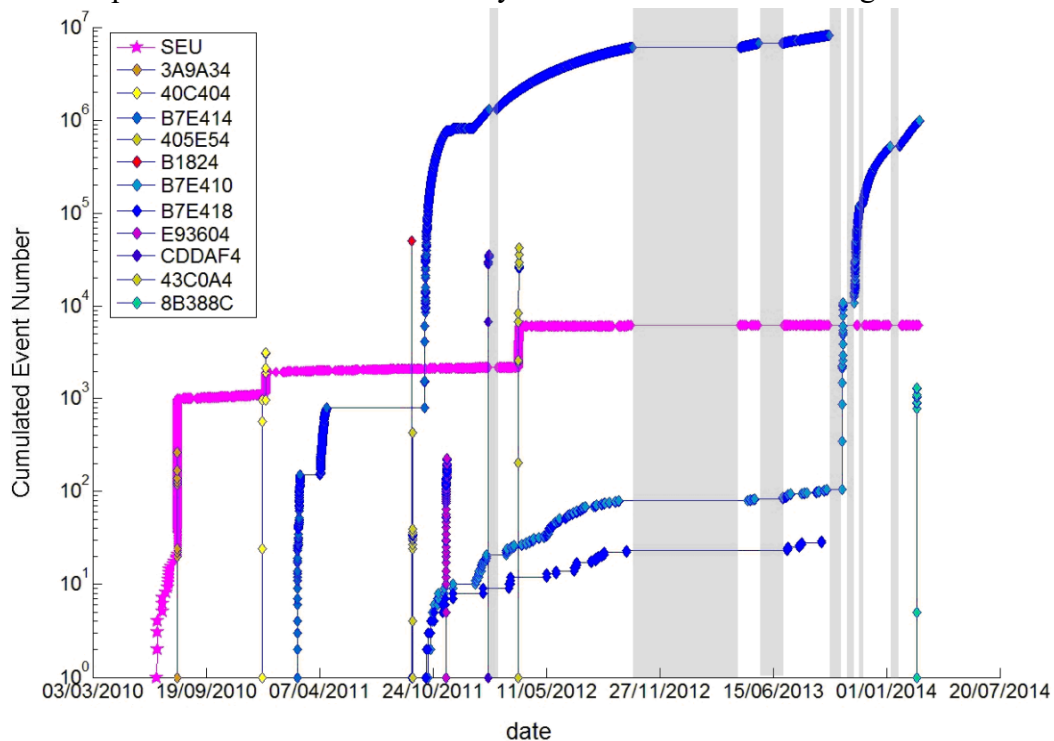


Figure 26: HY57V651620BLTC DRAM on PICARD Star tracker Cumulated, number of soft errors in function of the time and in function of the address for weakened cells [57].

Moreover, the majority of the errors begin in the South Atlantic Anomaly or in the high attitude region where the satellite experiences higher particle fluxes. Figure 27 and Figure 28 spotted the first occurrence of the weakened cells. The first weakened cell on CARMEN appears on 27/02/2010, at nearly 20krad (Si), while on PICARD the first weakened cell appears on 30/07/2010, at nearly 100rad (Si) very early into the mission.

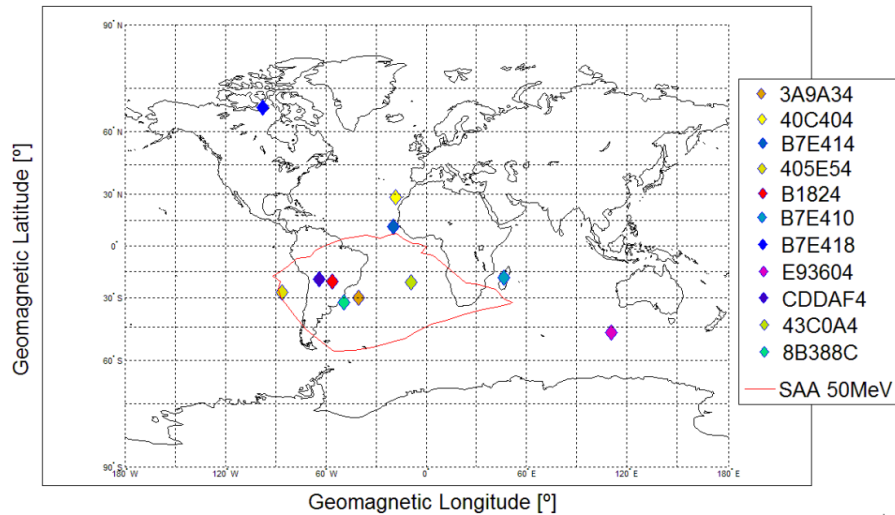


Figure 27: HY57V651620BLTC first weakened cell appearance cartography [57].

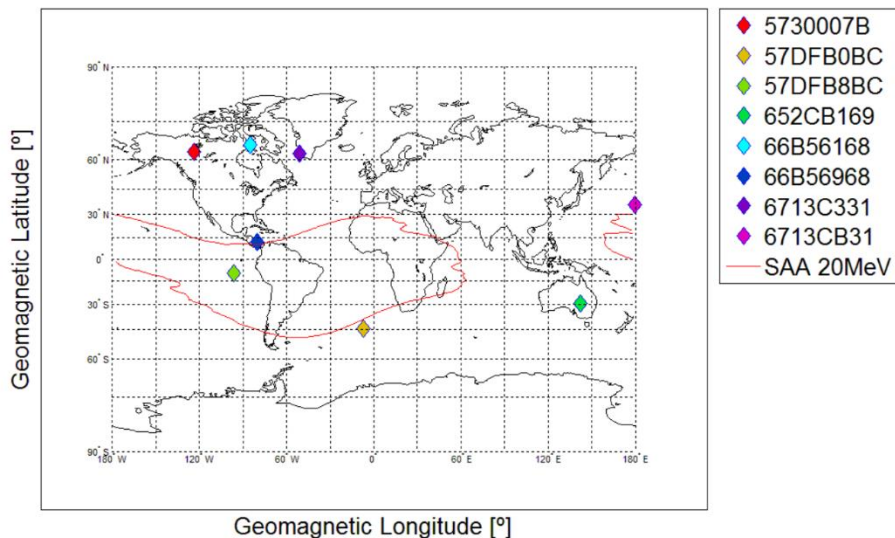


Figure 28: MMSD08512408S-Y Z36 first weakened cell appearance cartography [57].

From the inflight data, these weakened cells' behavior can be summarized as follows:

- Localized: means that the faulty behavior of specific memory cell is always at the same bit of the same word.
- Intermittent: means that the bit upset does not show up all the time but the cell can be working normally for a period of time before showing upset again.
- Persistent: means that power cycle by restarting the component does not fix the defective cells.

In the literature, these behaviors can also be referred to as “Intermittent Stuck Bits” (ISB).

### 1.4.2. Literature studies on the phenomenon

Stuck bits are another effect that has been observed by various studies about space radiation on DRAM devices. Resulting from a study of the Jet Propulsion Laboratory in 1994, stuck bits have been observed under heavy ion irradiation [59]. Moreover, the phenomenon is also detected under lighter particles such as proton [60]. On the other hand, DRAM may also exhibit to stuck-at-fault type of error where one signal node is tied to power rail or to ground [61]. One of the main differences between stuck bit and stuck-at-fault mechanism is that stuck bit can be an intermittent behavior [62].

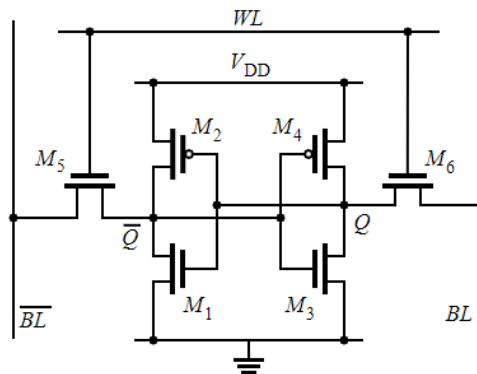


Figure 29: Standard 6T SRAM schematic.

SRAM typically consists of six MOSFETs (Figure 29), where the bit information is stored in two cross-coupled inverters formed by four transistors. SRAM maintains two stable states representing for 0- and 1-bit values. In addition, two more transistors are used as access transistors for read and write operations. When one of transistors is damaged and the bit information is lost, this leads to stuck bit.

One of the proposed methods to explain stuck bits is micro-dose [63] which is successfully used to explain Single hard error (SHE) on SRAM [64]. Micro-dose is the dose deposited by single charge particle into material. Oldham et.al. [65] investigated the impact of this charge creation in the gate oxide of a conventional MOS transistor. The study showed that a single ion can cause a significant shift in the threshold voltage of a transistor (Figure 30). Depending on the micro-dose strength, it may form a leakage between the source and the drain, which leads to a bit flip in a memory cell. If the leakage current is sufficient, it can keep the channel active even without the gate bias, hence the effect is permanent.



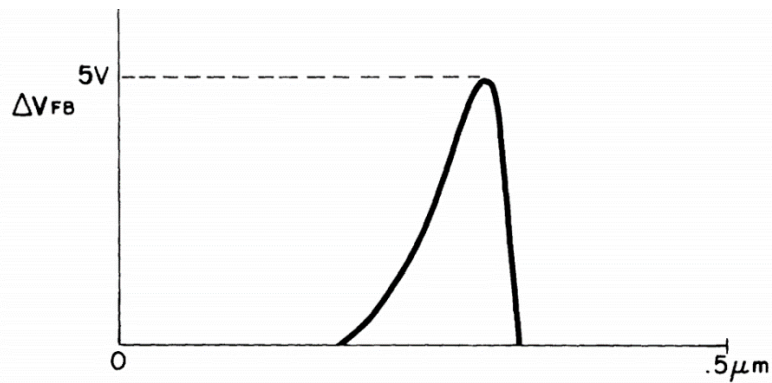


Figure 30: Flat band voltage shift as a function of position for the charge distribution in a 0.5μm channel [65].

Much different from SRAM, the structure of DRAM (presented in Figure 31) is relatively simple, with one transistor and one capacitor where it stores bit information. Because the charges stored in capacitor can leak away in various ways, DRAM need periodically “refresh” to maintain the data integrity. In case of external effects causing a higher leakage current, the charges inside capacitor can reduce below threshold thus returning a wrong value. The detailed studies of DRAM devices will be presented in chapter 2.

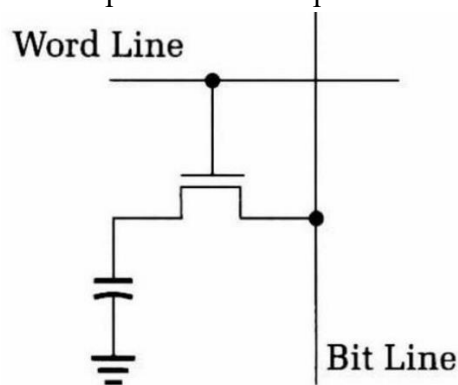


Figure 31: 1T1C Dram cell diagram.

Single event hard errors in DRAMs induced by a single energetic particle are proposed as the main mechanism for stuck bit. Shindou et al. studied the phenomenon in commercial DRAM [60] and showed that the capacitance of storage capacitor and the depletion region are the key parameters to evaluate the failure caused by bulk damage.

In contrast to SRAM, stuck bit on DRAM is proved not a micro-dose effect but a micro-displace damaged by single particle [66]. Evidences from the experiments show that the number of stuck bits is proportional to the fluence, however, the cross section per-bit is smaller than that of the area’s physical structures (Figure 32). Moreover, a higher cross section in lower energy proton also suggests further the role of micro-displacement damage over micro dose in DRAM devices.

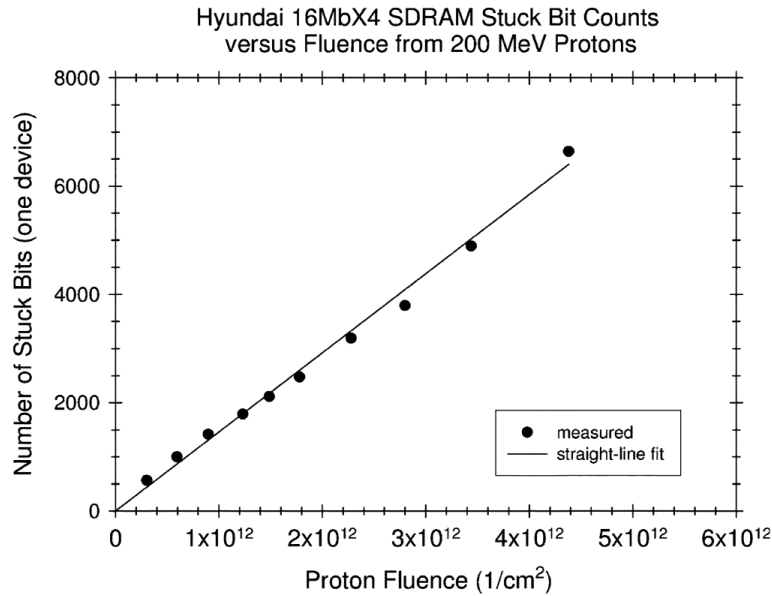


Figure 32: Stuck-bit counts versus fluence from 200 MeV protons taken from [66].

The experiments by David et.al. [67] irradiated DRAM under protons, neutrons and heavy ions and  $^{60}\text{Co}$  source. The experiment results showed that the memory cell degradation comes from single particle rather than local dose absorption. In addition, both degradation and annealing were not affected by the applied bias. Furthermore, the degradation is stable at room temperature and needs a high temperature to anneal. The experimental data also show a credible result of the relationship between NIEL and degradation in coherent with displacement damage in bulk (Figure 33).

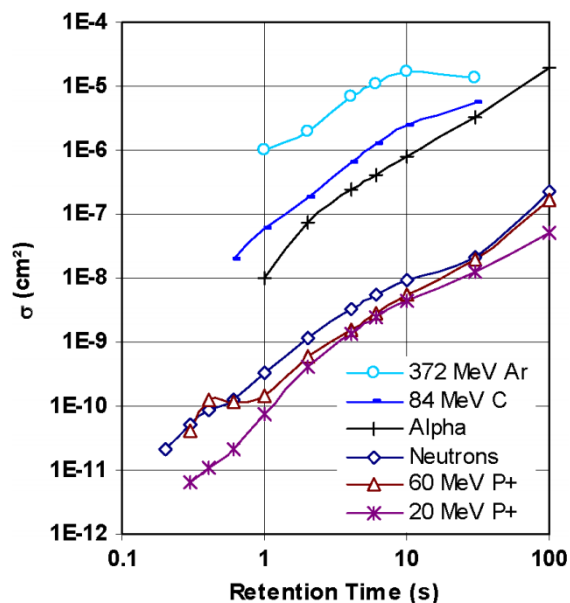


Figure 33: Degradation device cross section for different particle types with highest NIEL of Ar [67]

In the study by Chugg et.al. [68], they investigated the Random Telegraph Signal contribution to intermittent stuck bits (ISB) in proton and neutron irradiated by DRAM devices.

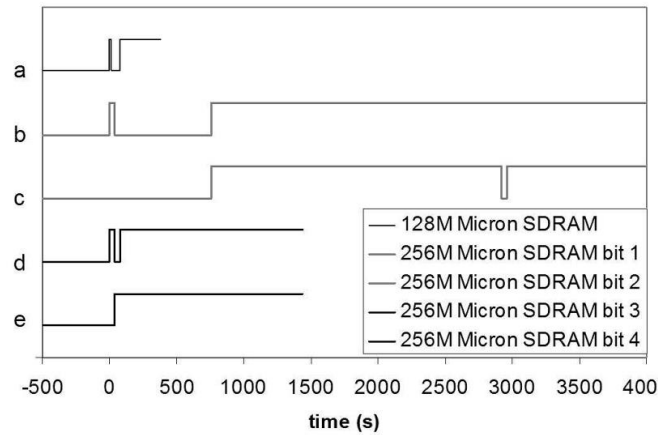


Figure 34: Intermittently stuck bits in proton irradiated 128 Mbit and neutron irradiated 256 Mbit DRAMs [68].

Interesting experimental results show that a proportion of the stuck bits became unstuck at a later time during the irradiation, and further observations point out that some of these subsequently spontaneously re-stuck as showed in Figure 34. Other important results concern the thermal effect on the behavior of the stuck bits. Figure 35 shows the error of each address with respect to the evolution of the read cycle. It shows that the ISB appeared early in the thermal cycle, and repeatedly stuck and unstuck when the temperature gradually increased. This proves that the ISB is not the artifact of noise in the leakage current when the difference in leakage current between low and high temperature is large enough. Furthermore, Chugg's experiment also showed that the number of observed stuck bits increases steeply with temperature which means that many damaged cells will show the sticking behavior when temperature increases the charge carrier availability. Comparison between unbiased and biased DRAM, where the same behaviors are also seen, provides additional evidence for ISB as a result of Single Particle Displacement Damage Event (SPDDE) phenomenon.

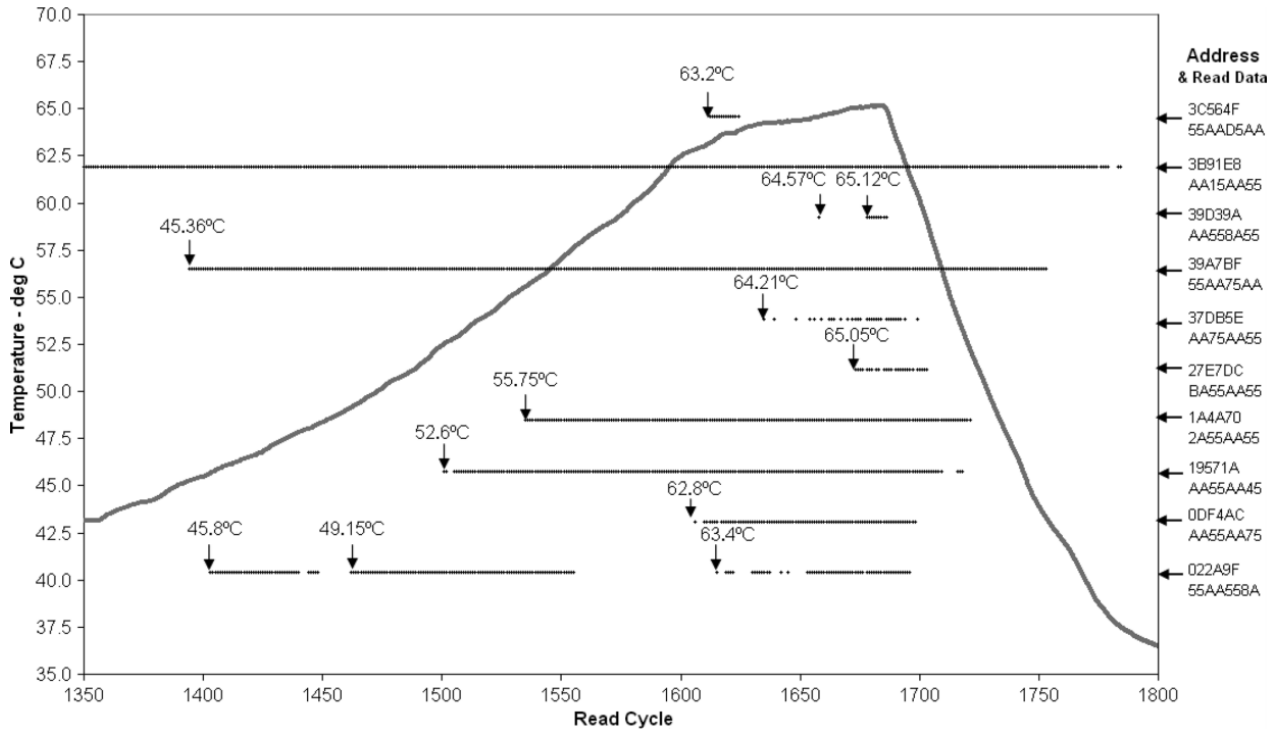


Figure 35: Manifestations of stuck and intermittently stuck bits post-irradiation correlated with a wide peak of temperature at the device [68].

With this experiment, Chugg et al. proposed a mechanism responsible for Random Telegraph Signal in leakage current. The model suggests that a single particle creating damage in bulk is able to create multiple close space defect amorphous clusters [69]. In the case illustrated in Figure 36, during the first five cycles of temperature, the bit consistently went stuck when the temperature exceeded 29°C and unstuck when the temperature fell below that. In contrast, during the next five-time cycles, the stuck/unstuck behavior transition was consistently at 43°C. This shows that the cell goes through different levels of leakage current within its displacement damage. Each of these states corresponds to a defect cluster that manifests low or high state of leakage current.

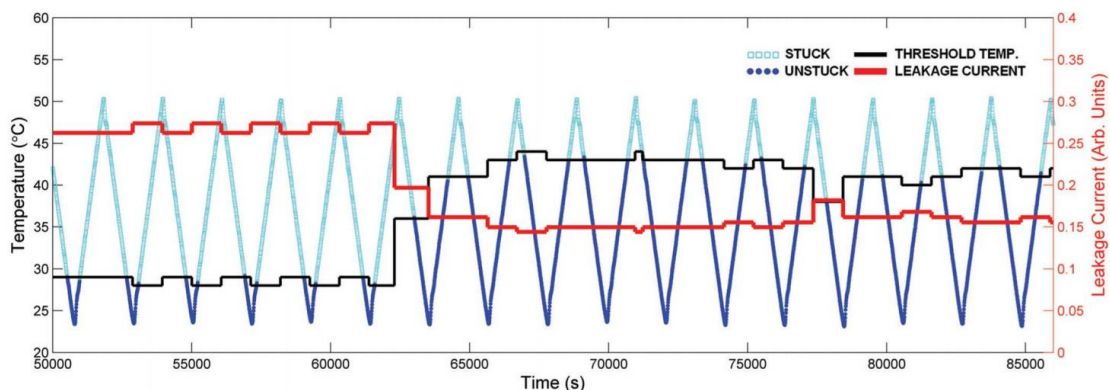


Figure 36: Sticking history for Micron 128 Mbit DRAM Sample 8 Address 3161DC Bit 14 sticking low and derived leakage current profile. [69]

An electrical model with the assumption that each defect cluster represents an effective resistance in its part of the leakage current path, which is independent of the other clusters.

Total resistance is  $R_{total}$  and the resultant leakage current is  $I_{leak}$  which is given in the Figure 37, each individual resistance  $R_a, R_b, R_c$  has two possible values representing two states of the clusters.

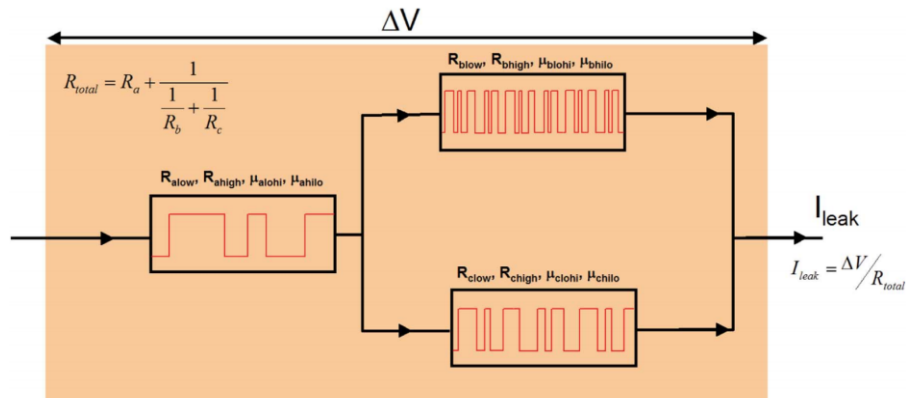


Figure 37: Example case of a resistive model of leakage currents through a 3-cluster leakage current complex. [69]

The similar RTS behavior is also detected in CCDs sensor [70], with the irradiation of light particles (electrons, photons) as well as heavier particles (protons, neutrons, heavy ions). As mentioned above, NIEL is used to correlate with the displacement damage from energetic particles. According to [71], at low NIEL values ( $<5 \times 10^{-5}$  MeV.cm<sup>2</sup>/g), isolated defects dominate, while at relatively high NIEL values ( $>2 \times 10^{-4}$  MeV.cm<sup>2</sup>/g), complex clusters dominate the displacement damage defects.

Recent research by Vincent Goiffon et.al. [72] has demonstrated that both ionizing radiation and non-ionizing radiation can enhance the variable retention time (VRT) in DRAMs cells. Among a large number of VRT cells, many of them can be a critical source of intermittent stuck bits. Figure 38 shows the maximum and minimum retention time of one million cells unirradiated, <sup>60</sup>Co irradiation and neutron irradiation. Experimental results show that neutron-induced displacement damage leads to the creation of VRT cells and that those cells can exhibit much lower retention times than TID induced ones.

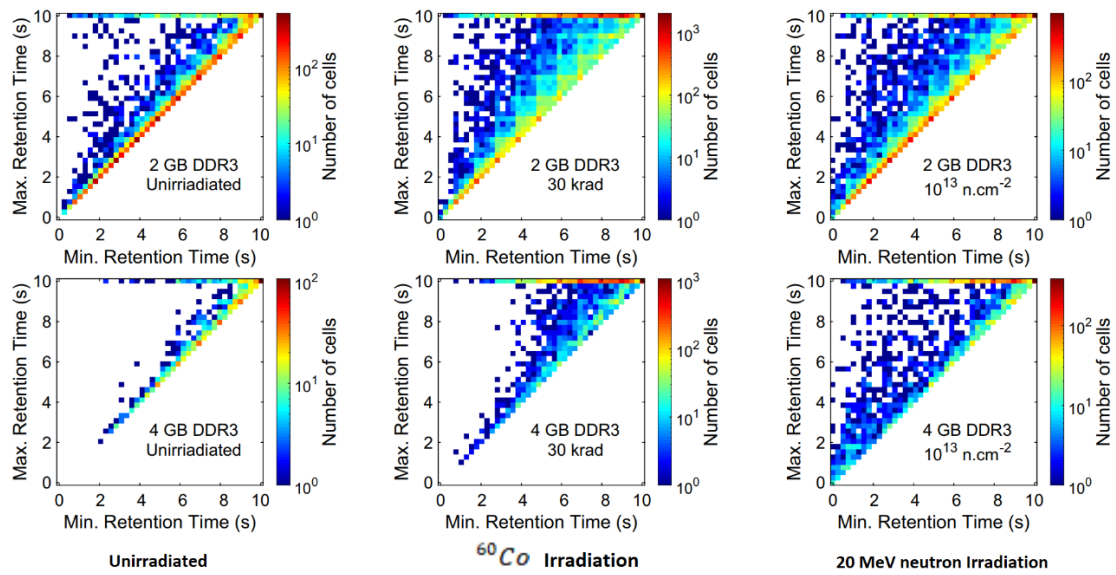


Figure 38: Minimum and maximum retention time distributions of the unirradiated DRAMs (left), DRAM exposed to  $^{60}\text{Co}$  gamma-ray (middle) and neutron irradiation (right) [72].

The paper suggested that the Dark current – Random Telegraph Signals in imaging sensors are also the origin of Variable Retention Time in DRAMs. Two origins of variable leakage current are highlighted in Figure 39. The first center is interface VRT centers exist in pristine device and are increased by Ionizing radiation dose; the second one is the bulk defects are mostly induced by displacement damage.

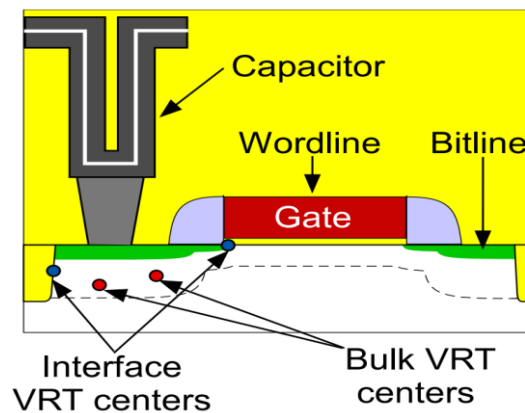


Figure 39: Cross sectional illustration of a DRAM cell (not to scale) showing the identified sources of radiation induced VRT [72].

## 1.5. Conclusion

In this chapter, the space radiation components including: Cosmic rays, Solar particles and trapped particle around the Earth have been summarized. Their effects on the electronics devices onboard satellite are also mentioned as well as the prediction model corresponding to each type of radiation. Two main effects are: single event effect from a single particle which happens instantaneously when the particle hits the sensitive volume; and cumulative effects which accumulate over time from Total ionizing dose and Displacement damage dose.

The harsh conditions of space have induced various malfunctions onboard satellite's electronics especially memories. SRAM and DRAM are two main volatile memory types which are commonly used in computer system as the main memory. From previous works, the weakened cells on SRAM will not pose a threat in future. However, the origin as well as the characteristics of weakened cells on DRAM still need to be studied.

In the scope of this thesis, weakened cells phenomenon on DRAM devices is focused. This special event has caught attention of many studies because of its complexity and unpredictability. From multiple works, the weakened cells are believed to come from displacement damage which a single particle can create bulk defect cluster. This damage can increase the leakage current of the DRAM thus creating stuck bit. Furthermore, different states of defect transition can create intermittent behavior.

Moreover, recent work has linked the variable retention time of DRAM cell to a potential source of weakened cell and intermittent stuck bits which originate from interface traps at storage node of the accessed transistor.

# **Chapter 2: DRAM devices and characteristics**



## 2.1. Introduction

The memory subsystem is indispensable in any computer system. Their functionality and performance are also affected by the characteristics of the memories. Semiconductor memories are the main contribution of the memory subsystem. The mainstream semiconductors can be mentioned: static random-access memory (SRAM), dynamic random-access memory (DRAM), and flash. Few other new emerging memory technologies have been developed to replace existing devices in the future: Phase Change Memories (PCRAM), Magnetic memories (MRAM), Resistive memories (RRAM). The different types of memory are listed in Table 6 where F is the minimum feature size during the fabrication process.

Mainstream memories can be classified into volatile and non-volatile types. Volatile memories will lose data when the power is off. There are two types of volatile memory: SRAM and DRAM. In contrast, the non-volatile ones such as flash are able to retain the information without power input. These differences make them suitable for different purposes from main memory to data storage.

Table 6: Semiconductor memories [73].

	Mainstream memories				Emerging memories		
	Volatile		Non-Volatile				
	SRAM	DRAM	NOR Flash	NAND Flash	STT-MRAM	PCRAM	RRAM
Main purpose	Cache	Main memory	Code Storage	Data storage			
Cell area	$100F^2$	$6F^2$	$10F^2$	$4F^2$	$6-50F^2$	$4-30F^2$	$4-12F^2$
Bit per cell	1	1	2	3	1	2	2
Voltage	<1V	<1V	>10V	>10V	<1.5V	<3V	<3V
Read time	1ns	10ns	50ns	10 $\mu$ s	<10ns	<10ns	<10ns
Write time	1ns	10ns	10 $\mu$ s – 1ms	100 $\mu$ s – 1ms	<10ns	~50ns	<10ns
Retention time	Unlimited	Limited (standard >64ms)	>10 years	>10 years	>10 years	>10 years	>10 years
Endurance in number of read cycle	$10^{16}$	$10^{16}$	$10^5$	$10^4$	$10^{15}$	$10^9$	$10^6 - 10^{12}$
Write energy per bit	fJ	10fJ	100fJ	10fJ	0.1pJ	10pJ	0.1pJ

DRAM stands for Dynamic Random-Access Memory; it consists of a single transistor and a capacitor where it stores information. The charges stored in capacitor are depleted through different leakage paths. Therefore, DRAMs need periodic refreshing to maintain the

information. Each bit of DRAM can be accessed (read/write) independently; thus, it's called random-access memory.

Despite the potential of new emerging memory devices, mainstream memories with mature technology are still dominant in the market. Among those, DRAM is popular choice for main memory of computer system due to its advantage of price and density over SRAM. As mentioned in Chapter 1, weakened cell phenomenon aren't a concern on SRAM in the future. Therefore, in the scope of this thesis, DRAM is our target of studying therefore this chapter will detail the principle of operation, structure and layout and its responses to radiation.

## 2.2. DRAM's chip architecture and layout

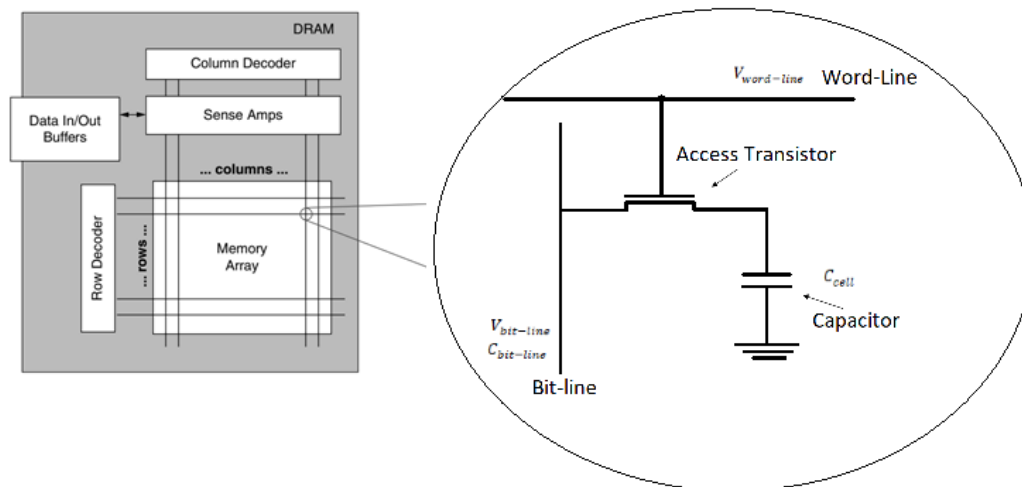


Figure 40: Basic organization of DRAM internals. The DRAM memory array is a grid of storage cells, where one bit of data is stored at each intersection of a row and a column.

**Error! Reference source not found.** 40 shows the basic architecture of a DRAM chip. A DRAM chip is decomposed into different levels of which the highest is a bank containing multiple small memory arrays. Each bank operates independently of each other and has its own peripheral circuit. One bank is composed from many smaller arrays of individual cells called mats. Finally, the smallest component is a single DRAM cell where the data is stored. In modern DRAM, a single cell consists of an access transistor and a capacitor. At the access transistor, the word-line connects directly to the gate, the bit-line connects to the source and the drain connects to the storage capacitor. However, the consideration of source and drain can be swapped depending on the operations of the DRAM cell.

In addition to the main memory array, every DRAM chip also includes many peripheral circuits such as row decoder, column decoder, sense amplifier and data buffer.

### 2.2.1. DRAM array layout

For each memory cell, the bit-line connects to the source of the access transistor, while the word-line is attached to the gate to control the flow of charges to the capacitor. The capacitance of capacitor is much lower than the long bit-line that connects hundreds or thousands of memory cells. Therefore, in order to read the digital value from the cell, a sense amplifier is

used to “sense” the data from the cell. In order to minimize the generated noise, a pair of bit-lines is connected to a single sense amplifier. Those bit-lines must have a similar voltage and capacitance, which means they must have an equivalent length and number of connected cells.

Two different bit-lines network structures are used: an open bit-line structure and a folded bit-line structure. In the open bit-line structure, the bit-line pairs connected to one sense amplifier come from a separated array segment, whereas in the folded bit-line structure, the bit-line pairs come from the same array (illustrated in Figure 41).

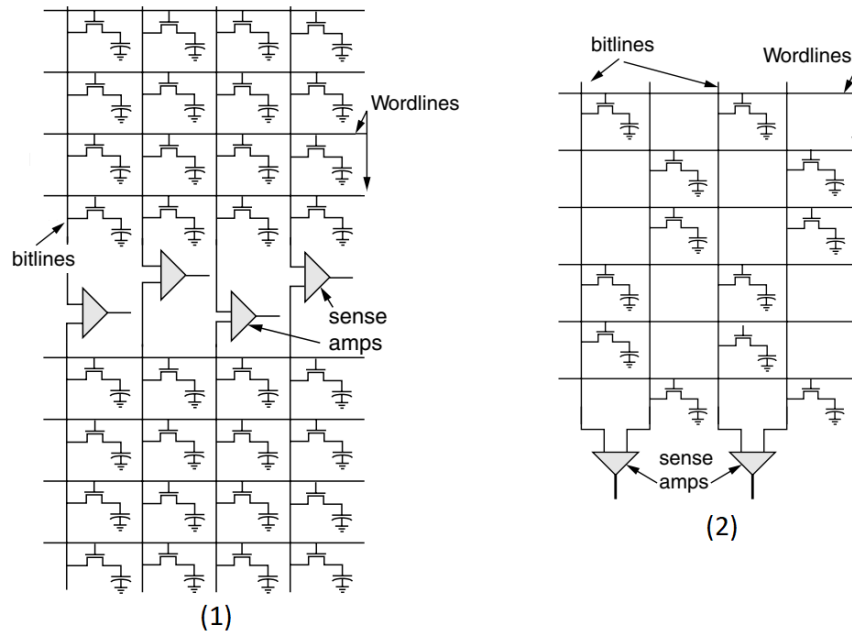


Figure 41: DRAM layout with Open bit-line (1) and Folded bit-line (2) [74].

The open bit-line structure has the advantage of having cells as small as  $6F^2$  compared to  $8F^2$  in the folded bit-line structure. However, some drawbacks of this structure such as higher noise and dummy array requirement at the edge of the memory array [74] lead to the dominance of the folded bit-line in the industry over the last 20 years. When the scaling of the semiconductor memory requires a more compact chip layout and lower cost of fabrication, the open bit-line structure has become the main structure of dense DRAM chips.

The proximity of the bit-line pairs in the folded bit-line structure means that the differential sense amplifier circuit, when paired with this array structure, exhibits superior common mode noise rejection characteristics. In other word, in the case of a charge spike induced by a single event upset (SEU) neutron or alpha particle striking the DRAM device, the voltage spike would have a good chance of appearing as common-mode noise at the input of the differential sense amplifier. In the case of the open bit-line array structure, the charge spike induced by the SEU would likely appear as noise on only one bit-line of a pair that connects to a sense amplifier.

### 2.2.2. DRAM generations

The modern DRAM operations are synchronized with an external clock; hence they know the clock cycle when the data is requested. Most DRAMs now are synchronous DRAM (SDRAM) and double data rate RAM (DDR SDRAM) with multiple generations and variations.

The first generation is SDRAM (or SDR SDARM) which stands for Single Data Rate SDRAM. It has the same internal clock and bus clock and can only read or write once per clock

cycle. SDRAM has a disadvantage when it needs to wait for the completion of a previous command to execute the next one.

The next generation of DRAM is DDR or Double Data Rate SDRAM. The first DDR SDRAM generation doubles speed of SDRAM by transferring the data on both rising and falling edge of the clock cycle. By improving the speed of the external data bus by two times and the DDR SDRAM, DDR2 SDRAM can reach a speed of 533 to 800 MT/s (where MT/s is mega-transfers per second referred to the number of operations transferring data per second). In the next generation of DDR3 SDRAM, manufacturers were able to reduce power consumption compared to DDR2 from 1.8V to 1.5V. Moreover, the prefetch is also gradually increased from 1bit to 8bit to catch up with the speed of CPU. The latest generation of DDR4 on the market provides a higher transfer rate at a lower operating voltage. Table 7 shows the differences between DRAM generations.

Table 7: Comparison of different DRAM generations.

SDRAM standard	SDR	DDR	DDR2	DDR3	DDR4
Internal rate (MHz)	100-166	133-200	133-200	133-200	133-200
Bus clock (MHz)	100-166	133-200	266-400	533-800	1066-1600
Prefetch	1bit	2bit	4bit	8bit	8bit
Data rate (MT/s)	100-166	266-400	533-800	1066-1600	2133-3200
Transfer rate (GB/s)	0.8-1.3	2.1-3.2	4.2-6.4	8.5-14.9	14-21.3
Voltage (V)	3.3	2.5/2.6	1.8	1.35/1.5	1.2
Refresh	64ms				

In the market, SDRAM is dominant. Therefore, in this study when we mention DRAM it is synchronous DRAM device.

### 2.3. DRAM's operation

One important component to read digital value of DRAM is the Differential Sense Amplifier (SA), the schematic of which is described in Figure 42. While the access transistor is used to control the charge flow in and out of the capacitor, SA is used to resolve the electrical charge of the cell's data.

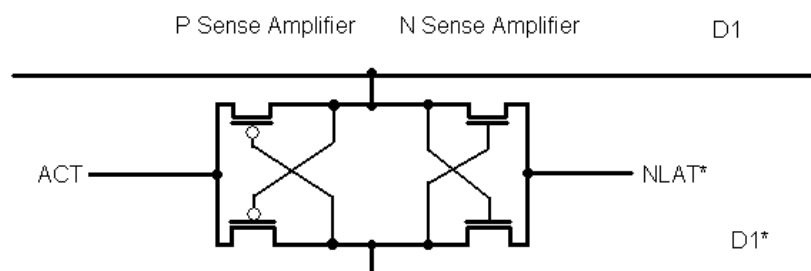


Figure 42: Sense amplifier schematic [75].

The first function of SA is to detect the differences of voltage swing on the bit-line when it receives shared charges from the capacitor. Secondly, the SA also restores the information of the cell after charges have been equalized with the bit-line. Finally, the SA also serves as a data buffer for different operations without the need to re-access the cell.

DRAM operations consist of different phases in which “Precharge” is the first before any follow up actions (Figure 43).

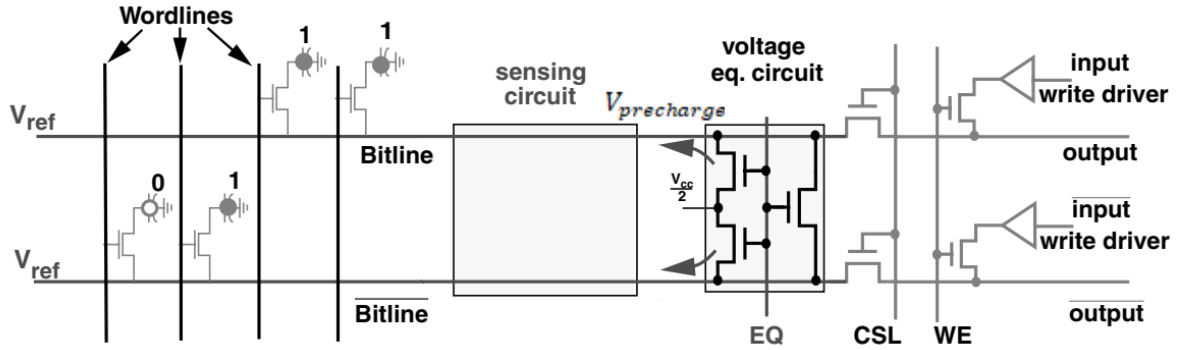


Figure 43: Precharge operation of DRAM [74].

When the DRAM Precharge, the bit-line will be applied a voltage  $V_{precharge} = V_{DD}/2$ .

The “Access” phase is when the access transistor is turned on, which is equivalent to the rise of the word-line. The “Sense” phase follows when the sense amplifier detects the voltage difference. Finally, the “Restore” phase is used to rewrite data in the capacitor.

Then the cell is ready to be read or written. For instance, in read operation of the cell storing charge at the value “1”, the word-line will rise to allow the charge to flow from the capacitor to the bit-line. Therefore, a voltage swing  $\Delta V$  will occur on the bit-line and be detected by differential sense amplifier and the value are describe in equation (2.1).

$$\Delta V = \frac{V_{DD}}{2} \frac{C_{cell}}{C_{cell} + C_{bit-line}} \quad (2.1)$$

Similarly, in case the cell does not store a charge at the value “0”, the voltage will drop by one  $\Delta V$ . Note that depending on the manufacture, they may encode the value “1” and “0” differently.

In write operation, the bit-line is raised high or low and the charges are equalized with the capacitor through the access transistor. Figure 44 illustrates the voltage waveform of the sense amplifier in read operation.

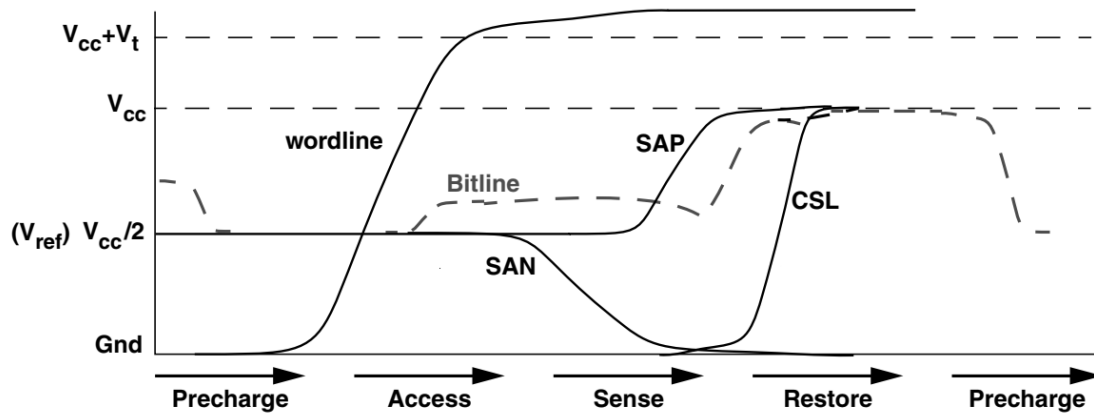


Figure 44: Sense amplifier voltage waveform in Read operation. simplified from [74].

As mentioned above, DRAMs must be periodically refreshed due to the charge leakage from the capacitor. The refresh operation is actually a dummy read and then a rewrite of the data in the cell. According to the JEDEC standards (standards for the microelectronics industry), DRAMs must be refreshed every 64ms.

## 2.4. DRAM's physical structure

As shown previously, the component of a single DRAM cell is simple to compare to other semiconductor memories such as SRAM. A one-transistor and one-capacitor structure allows DRAM to achieve a much higher density and low manufacture cost per bit. The initial design of two-dimensional devices called planar capacitor cell was a main trend in the 1 to 4 Mb DRAM chip. However, with the aggressive scaling of the industry, the cell has moved to a three-dimensional structure. Two main approaches of the capacitor placements are the trench capacitor cell, in which the capacitor is embedded deep inside the substrate, and the stack capacitor, in which the capacitor is attached on top of the access transistor.

Based on the patent of Dennard [76], the one-transistor memory cell was introduced with a planar structure (Figure 45). The initial device is composed of a MOSFET and a charge storage capacitor where the total stored charge consists of a junction capacitance and a bias-independent MOS capacitor [77].

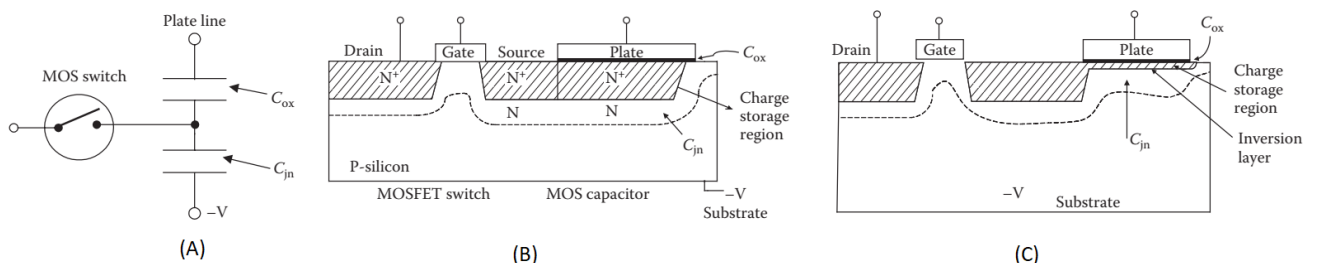


Figure 45: Planar transistor memory cell. (a) Equivalent circuit, basic structure (b) with diffusion storage, and (c) with inversion storage. (Redrawn from [77])

In order to increase the memory size with a planar structure, the industry needs to consider the MOSFET technologies as well as the complexity of the lithographic process, chip

performance and cost. Since 1979, the polysilicon-to-polysilicon (poly-to-poly or double-poly) storage capacitor has seen its structure adapted to the planar cell configuration [78].

However, the planar structure is the trend only for chip with a density up to 4Mb when the downscaling is difficult. Three-dimensional cell becomes the next choice for high density DRAMs in the form of trench and stack capacitor.

#### 2.4.1. Trench capacitor cell

The industry is always finding ways to minimize the cost of DRAM devices. This trend leads to the reduction of cell size in order to increase the density on the same silicon die. Beside scaling down the access transistor, the capacitor dispositions above the silicon surface or deep growth in the surface have become new solutions.

In the trench capacitor structure, the charge will be stored in a trench that is embedded below the surface level and in the silicon substrate. The first version of the trench capacitor was invented in 1982 with the first 1-Mbit DRAM generation. However, the problem with the first trench cell was the high soft-error rate caused by alpha particles. Additionally, the punch-through current between two adjacent capacitors will limit the downscaling of the DRAM cell in the future [79]. A newer generation of deep trench capacitors doped on the side and bottom of the trench to form N-type regions to prevent the decrease in memory cell capacitance [80], [81].

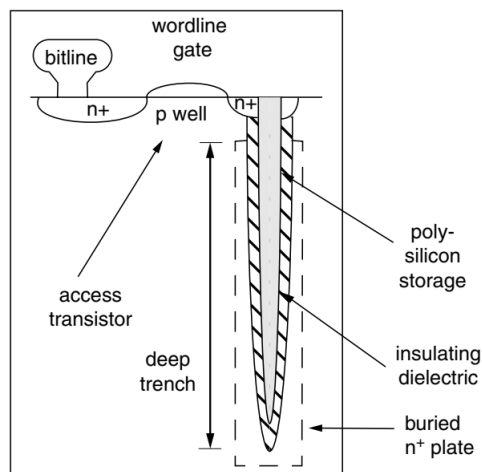


Figure 46: Cross-section view of a 1T1C DRAM with a trench capacitor [82]

However, in the newer generation of DRAM, a higher density of deep trench capacitor was required to achieve beyond the 4 Mbit chip. The new inverted-type trench cell was introduced with a deep polysilicon electrode surrounded by a thin insulator which is illustrated in Figure 46.

The deep trench capacitor allows a DRAM cell to reduce the silicon surface area without decreasing the storage cell capacitance. In a modern DRAM cell, the aspect ratio between the width and the depth of the trench capacitor can go up to 90:1.

### 2.4.2. Stack capacitor cell

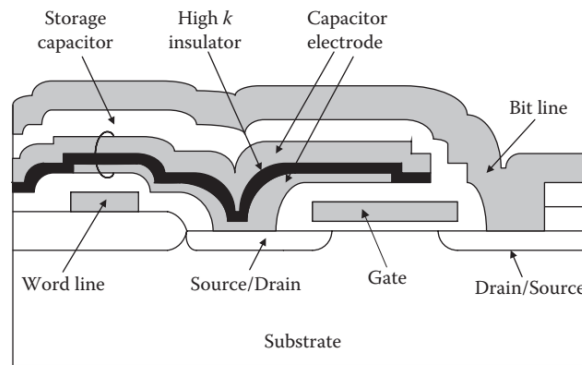


Figure 47: Basic structure of stacked capacitor cell [83].

In 1976, when Koyanagi was trying to eliminate the inversion and depletion capacitance of the MOS capacitor, he invented a three-dimensional (3D) cell [84], [85] called a stacked capacitor cell.

The basic structure of a stacked capacitor is described in Figure 47. The main difference with the trench capacitor structure is that the storage capacitor is stacked on the accessed transistor. The passive capacitor is formed with a sandwich layer of electrode-insulator-electrode of which the bottom electrode is connected to the source/drain of the transistor by a self-aligned contact. The self-aligned technique was also used to connect the bit-line to the source/drain and form the capacitor electrode.

By using the stacking, we can reduce the area occupied by the capacitor as well as utilize a high dielectric material as capacitor insulator to increase the capacitance. The first version  $\text{Si}_3\text{N}_4$  was used instead of  $\text{SiO}_2$  as capacitor insulator and polycrystalline silicon for both electrodes then a  $\text{Ta}_2\text{O}_5$  film with a five-time higher dielectric constant [83].

Since the bit-line is constructed above the storage node, it becomes more difficult to increase the capacitance of the capacitor by increasing the surface area. The Capacitor Over Bit-lines (COB) is the new implementation of the stacked capacitor structure to increase the DRAM density. Figure 48 shows the differences between the initial stack capacitor and the capacitor over bit-line structure.

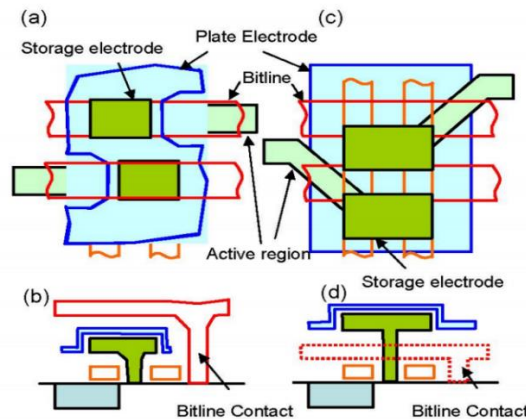


Figure 48: Comparison of cell layout and cross section of convention stack capacitor (a, b) and capacitor over bit-line structure (c, d) [86].



Both the trench and stacked capacitor structure have their own advantages and disadvantages. The trench capacitor is first grown deep into the silicon so that the higher level of metallic interconnection layers can be made easily on top. This maintains the logical compatibility between DRAM generations and accelerates the periphery. However, the stacked capacitor structure reduces the leakage current of the cell. Moreover, the passive stack capacitor can be built with a high-k insulator that will increase the capacitance. Last but not least, it also removes the limit of the trench capacitor by innovating the capacitor shape. Multi fin or cylinder are the next generations of stack capacitors. Figure 49 shows the development trend of DRAM cells.

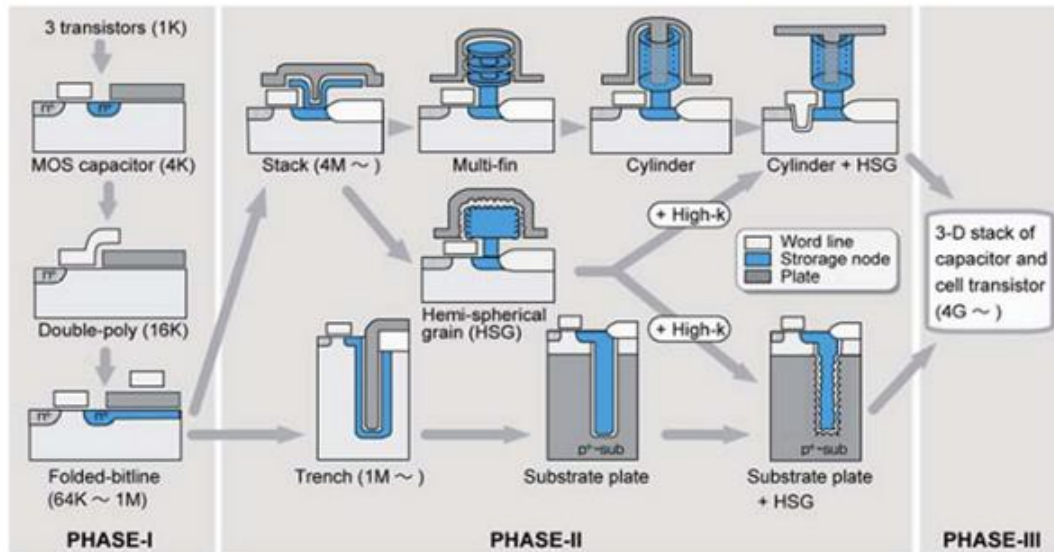


Figure 49: DRAM cell trend. Phases I, II, and III correspond to planar area shrinkage, 3-D capacitor, and 3-D stack of cell transistor and storage capacitor, respectively [87].

### 2.4.3. DRAM Access transistor technologies

As already mentioned, the two main components of a DRAM cell are the access transistor and the capacitor. In this section, we will discuss the transistor technologies used in the memory cell.

Unlike the logic transistor, the DRAM array transistor requires different properties. The DRAM access transistor focuses on an extremely low leakage current in order to achieve a longer retention time. Because of the one-transistor structure, DRAM cell is usually constructed from an NMOS transistor and the Gate has an overdrive voltage due to read/write activities of the cell.

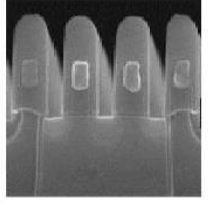
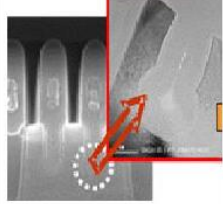
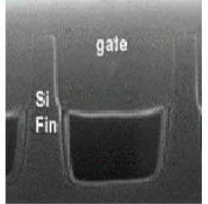
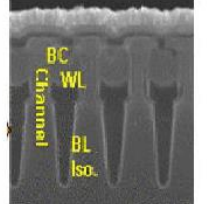
	Planar Tr.	RCAT	FinFET	Vertical Tr.
Technology	> 100nm	90nm ~50nm	50~30nm	< 30nm
Structure				

Figure 50: Evolution of DRAM cell transistor [88].

The DRAM access transistor is mainly a planar cell for technological nodes larger than 100nm. As the DRAM feature size shrinks, the transistor is struggle to maintaining the overall leakage current limit due to a higher electric field on the shrinking channel. One solution was to increase the channel doping concentration to increase the threshold voltage, so as to reduce the sub-threshold leakage current. However, the drawback is a high junction leakage current at the storage node and also reduces the current drive capability of the transistor [82]. To solve these problems, various new cell transistor structures and processes have been proposed.

Figure 50 shows the evolution of DRAM cell transistor design for different ranges of technological nodes. The first design was the Recess Channel Array Transistor (RCAT). Main advantage of RCAT is the increase in channel length within the same projected chip area. The recessed channel is formed in the silicon surface with a thin oxide layer and then a thick poly layer deposited on the substrate as a masking layer. Sphere-shaped RCAT (S-RCAT) is an improved form of RCAT that features a spherical ball part on the bottom of the recessed channel (Figure 51).

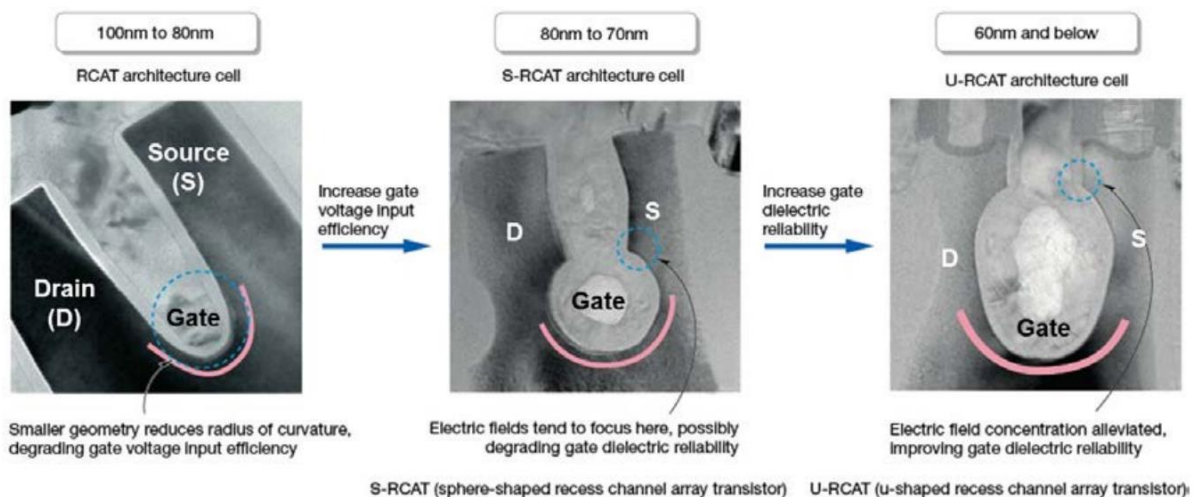


Figure 51: Recessed-Channel-Access-Transistor (RCAT) structures in DRAM technology [89].

In order to keep up with the downscaling of the traditional transistor, FinFET is the next design used for the access transistor. While RCAT has the advantages of low leakage and good refresh characteristics, FinFET has a high on-current due to the larger channel width. The Saddle FinFET was born to combine the best of RCAT and FinFET. Experiment shows that the on-current of the S-Fin was the largest, with an increase of 25% compared to RCAT [90].

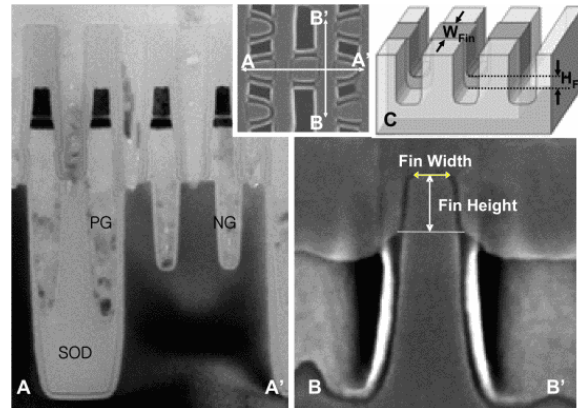


Figure 52: TEM cross-sections of saddle-fin cell-transistor on BL/WL direction [91].

In summary, in the modern technologies, DRAM cell access transistors have been successfully developed with different structural designs from the planar cell to Recess Gate and FinFET etc. Besides, the vertical gate transistor is under research and may become the next cell transistor technology. The DRAM cell layout is evolving from  $8F^2$  to  $6F$  and to the smallest theoretically  $4F^2$  (Figure 53) to increase the density and reduce the price per bit.

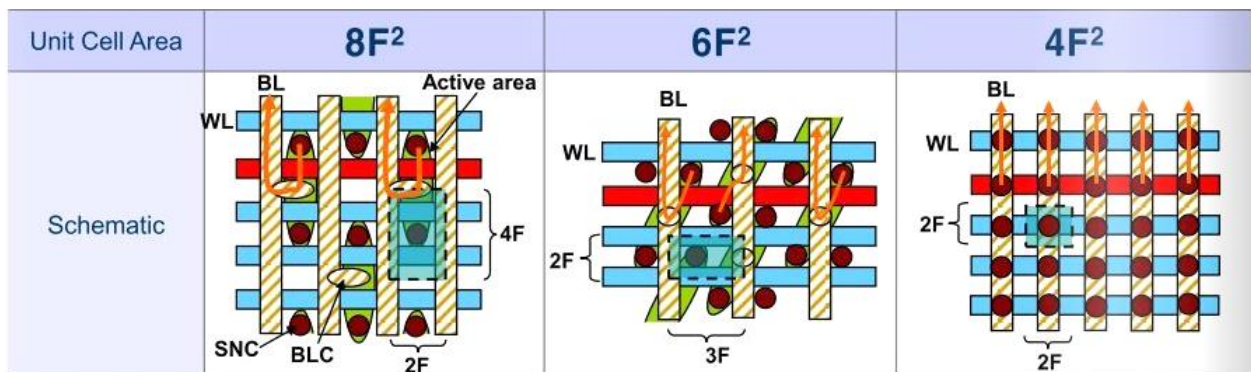


Figure 53: DRAM cell layout evolution [92].

#### 2.4.4. DRAM capacitor technologies

The capacitor is where DRAM cell stores its information in the form of an electrical charges. In addition, it is also the most critical issue when manufacturers try to shrink the cell size continuously. The original planar capacitor was formed with  $\text{SiO}_2$  as the dielectric and reducing the thickness was the main option to maintain capacitance when increasing the DRAM chip density. However, the increased leakage current prevented further thickness slimming down. Capacitance of the capacitor can be described as follows:

$$C = \frac{k\epsilon_0 A}{t} \quad (2.2)$$

where  $k$  is the relative dielectric constant of the material,  $\epsilon_0$  is the permittivity of the free space,  $A$  is area and  $t$  is the thickness of the capacitor's dielectric layer.

The above equation shows that to achieve the same capacitance, we need to (1) replace with an alternative higher dielectric constant material, (2) make structural innovations to increase the surface area of the capacitor or (3) decrease the thickness of the dielectric layer. The majority of the industry used  $\text{SiO}_2$  dielectric ( $k = 3.9$ ), but faces a reliability problem because of defects caused by local reduction of oxidation and breakdown fields. Since then,  $\text{Si}_3\text{N}_4$ -based capacitors, such as  $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{SiO}_2$  (ONO - oxide-nitride-oxide) or  $\text{SiO}_2/\text{Si}_3\text{N}_4$  (ON - oxide-nitride) multilayered dielectric structures have replaced the traditional  $\text{SiO}_2$  single-layer capacitors.

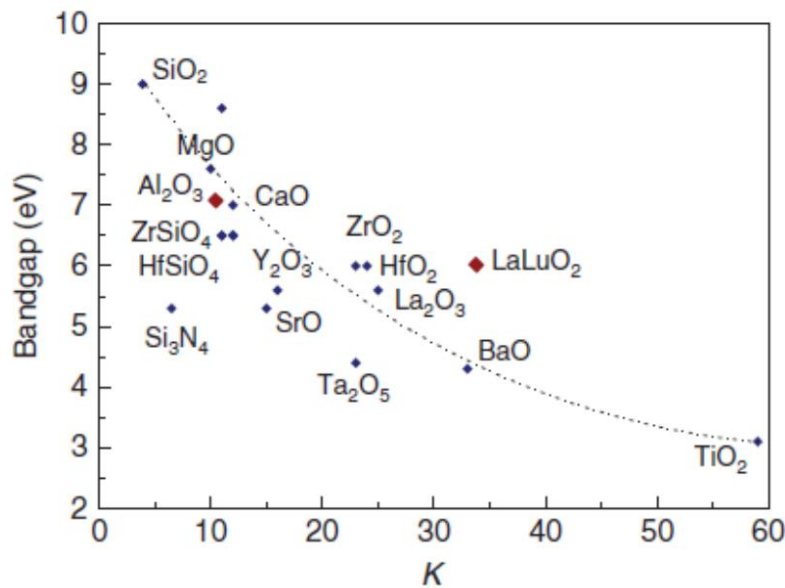


Figure 54: Static dielectric constant vs. bandgap for various High-K dielectrics as well [93].

High dielectric constant materials often referred to as high-k materials are a good solution for increasing capacitance. When shrinkage of the ON dielectric reaches its limits, alternative dielectric materials with higher dielectric constants are the next candidates.  $\text{Ta}_2\text{O}_5$  is the most promising dielectric for the next generation because  $\text{Ta}_2\text{O}_5$  capacitors can simply replace  $\text{Si}_3\text{N}_4$  capacitors without major process integration problems [94]. Few materials have been used to replace  $\text{SiO}_2$  such as  $\text{Al}_2\text{O}_3$ ,  $\text{HfO}_2$  etc. (see Figure 54). However, high-k materials tend to have a lower bandgap energy so the thickness of the thinner dielectric layer will increase the leakage current.

When the industry changes to a different dielectric, the capacitor structure also changes from SIS (silicon-insulator-silicon) to MIS (metal-insulator-silicon) and then to MIM (metal-insulator-metal). The selection of the electrode metal requires that it is compatible with the other materials on the chip, especially at different working temperatures. Different electrode materials such as TiN, platinum (Pt), ruthenium (Ru) are selected based on the type of high-k dielectric mentioned above [82].

With an aggressive downscaling of the capacitor footprint size, another solution to keep up the capacitance is to increase the effective capacitor area. One of the first methods is to texture the bottom polysilicon electrode before depositing an ultrathin dielectric, hence creating

asperities on the polysilicon surface that increase the effective area. The Hemispherical Grain Storage (HSG) Node has been developed at a DRAM density level of 64 Mbit for a Capacitor-Over-Bit-line (COB) cell structure (Figure 55).

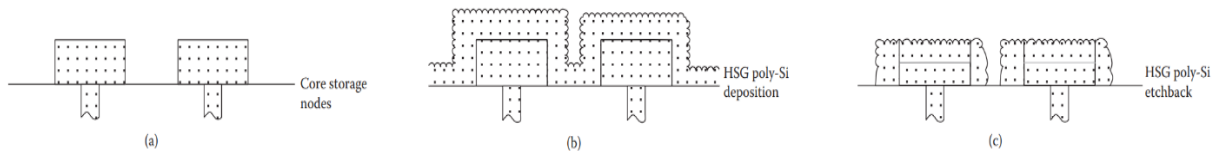


Figure 55: Fabrication steps for HSG poly-Si storage nodes for enlargement of storage node area by the HSG [95].

As briefly discussed in section 2.4.3., the shape of the stack capacitor can be modified to increase the surface area. The Crown-Shaped stack capacitor (Figure 56) was introduced in 1991 in a 64Mb chip by T. Kaga et.al, which provided a large capacitance charge of  $33 fC$  [96].

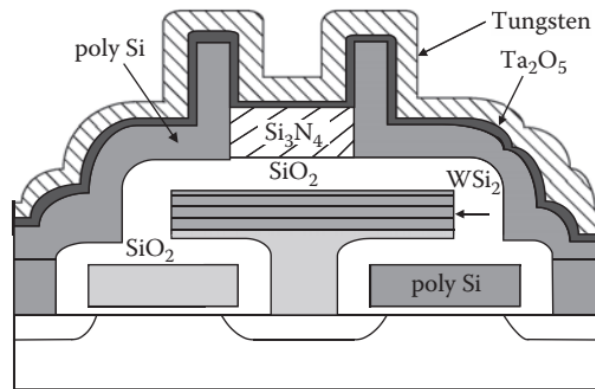


Figure 56: Schematic view of a CROWN cell [96].

S.G. Kim and others have reported that a fully integrated 512 Mbit DRAM with HSG-merged-AHO cylinder capacitor was successfully developed [97]. It is the combination of the cylinder structure and the HSG to achieve a high surface area. The process flow of the HSG one-cylinder storage node (RHOCS) is explained in detail compared to that of the conventional double HSG one-cylinder storage node (DHOCS) in Figure 57.

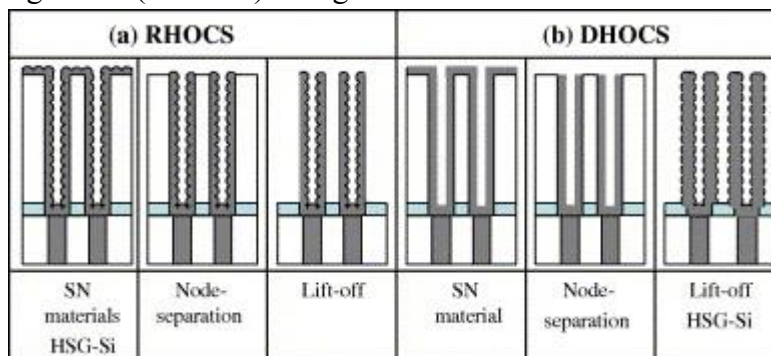


Figure 57: Schematic representation of (a) reverse HSG one cylinder storage node (RHOCS) and (b) DHOCS double HSG one cylinder storage node (DHOCS) [97].

The vertical structure can be used to further increase the 3D surface area of the capacitors. However, while we shrink down the horizontal area, we face mechanical limits in terms of

height. The cylinder structures have 2 bottom storage plate thicknesses, 4 dielectric thicknesses and 2 top storage plate thicknesses in each cell. A pillar structure has one top storage plate thickness, 2 dielectric film thicknesses and a bottom storage plate thickness in a cell width. This facilitates cell shrinkage, but by having 2 dielectric thicknesses instead of four, we need to increase the height of the pillar to keep up the capacitance [98]. Figure 58 shows the difference between the cylinder and pillar structure.

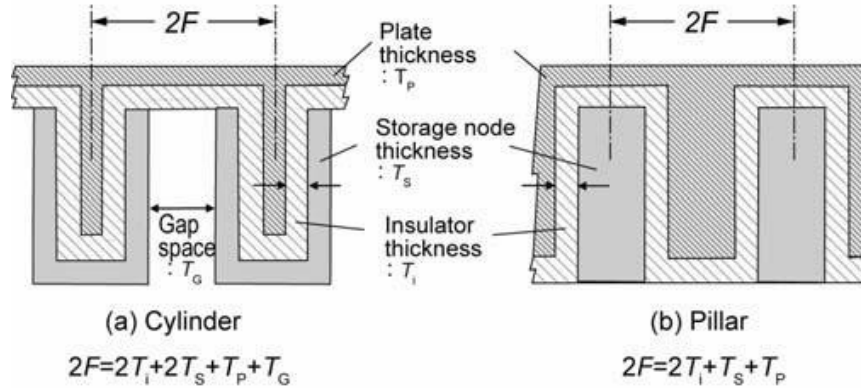


Figure 58: Relations among several film elements constructing the storage capacitor [87].

## 2.5. Characteristics of single DRAM cell

DRAM chips consume power through the peripheral circuit as well as through the memory cell array. DRAM contains its information as electrical charges on a cell composed of one transistor and one capacitor. However, the charges can gradually run out of the capacitor in many ways. Therefore, the DRAM cell must be refreshed periodically in order to maintain data integrity. According to JEDEC standards, each DRAM cell must be refreshed every 64ms. The time that one DRAM cell can store the data before the data is lost is called the retention time ( $t_{REF}$ ).

The retention time can be estimated using the equation below [99]:

$$t_{REF} \sim \frac{C_S \times \left( \frac{1}{2} V_{CC} - \Delta V_{BL} \right) - C_{BL} \times \Delta V_{BL}}{I_{leak}} \quad (2.3)$$

where:  $C_S$  and  $C_{BL}$  are capacitance of the cell and capacitance of parasitic capacitor in the bit-line respectively;  $I_{leakage}$  is total leakage current of the cell;  $\Delta V_{BL}$  is bit-line sensing voltage.

As we can see, the suppression of leakage currents is important to increase the retention time of the cell.

### 2.5.1. Variable retention time

Variable retention time (VRT) was first observed in 1987 [100] and then confirmed in most DRAM devices [101]. This phenomenon causes the retention time of many memory cells to change to different states randomly over time. There are two states level and multiple states level of VRT showed in Figure 59.

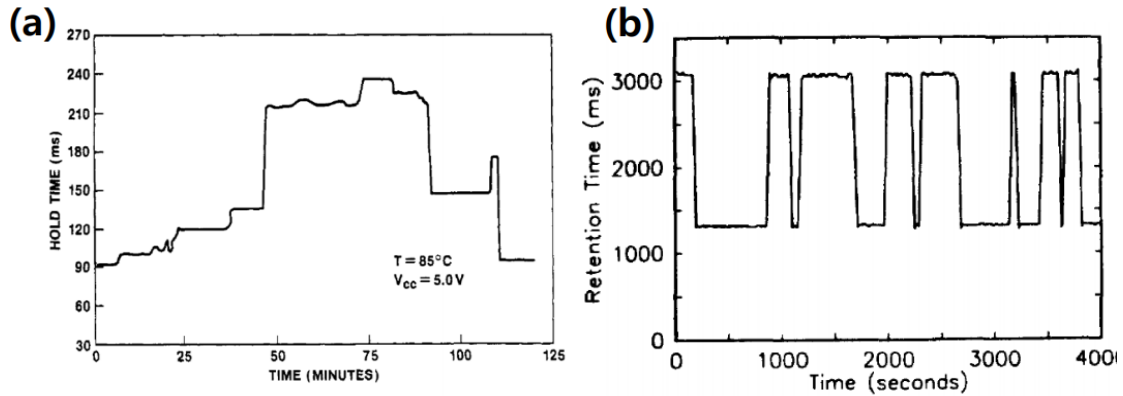


Figure 59: Multi states (a) and two states (b) variable retention time [100].

Initial studies have shown that the vacancy-oxygen  $V_2O_x$  defect is the cause of variation of the Junction leakage current as an attribute of gate induced leakage current at the storage node of the DRAM cell resulting from the VRT. The defect location is in the high-electric-field region near the gate edge. The good and bad state of leakage current is decided based on the traps energy level which are separated by  $\Delta E = E_{good} - E_{bad} \approx 0.1\text{eV}$  [102]. They also show that the good and bad states correspond to two orientations as shown in Figure 60. The structure fluctuation is believed to be responsible for the fluctuation of traps energy [103].

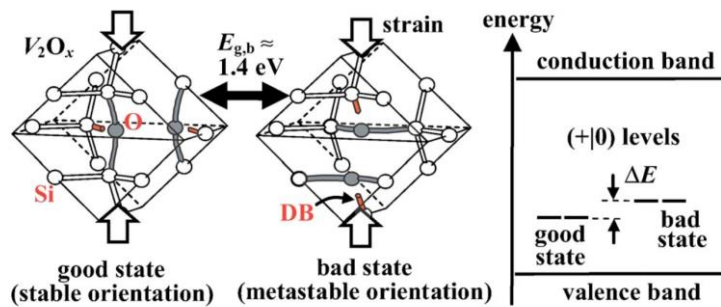


Figure 60: Model for bistable  $V_2O_x$  defect under strain: (left) Atomic view and (right) Energy-level view [102].

Other studies also have shown that the variation of  $I_{GIDL}$  (Gate-Induced Drain Leakage current) at the overlapping region of gate and drain is enhanced by a trapped electron. The model proposed that RTN (Random Telegraph Noise) in the junction leakage current (GIDL current) is induced by the trap-detrap site inside the dielectric layer or at the interface [104]. Figure 61 shows the variable in  $I_{GIDL}$  with  $\tau_c$  and  $\tau_e$  are the capture and the emission times of the electron from the trap.

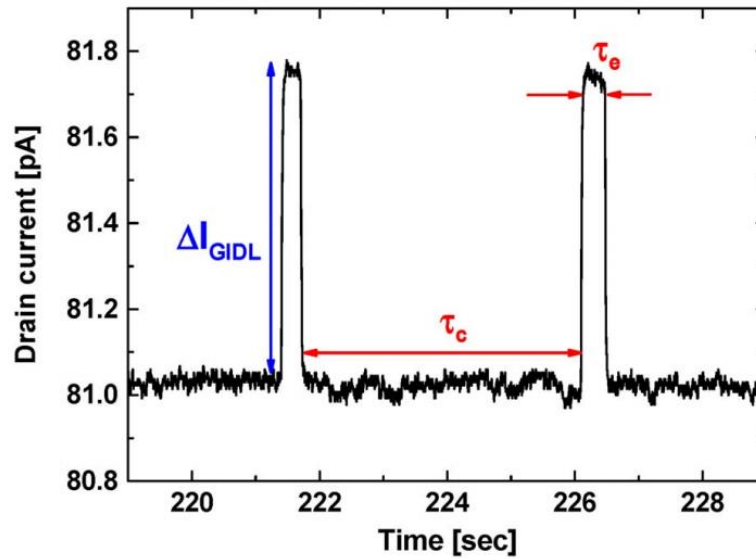


Figure 61:  $I_{GIDL}$  RTN in the time domain. The definition of the capture time  $\tau_c$ , for which a current is in the low state; the emission time  $\tau_e$ , for which current is in the high state; and the amplitude of RTN  $\Delta I_{GIDL}$  are shown in this figure [102].

This study also shows that with a lower voltage supplied in the latest DRAM generations (1.2-1.1V),  $I_{GIDL}$  is strongly dependent on temperature and suggests that  $I_{GIDL}$  mainly flows through Trap-assisted tunneling (TAT) [105].

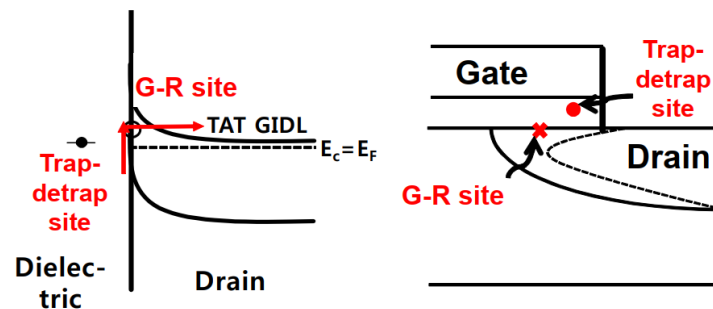


Figure 62: Demonstrations on RTN in TAT GIDL current caused by two trap sites in (left) energy band diagram and (right) cross-section view of planar MOSFET [105].

Figure 62 shows the diagram of two trap sites (generation-recombination site (G-R site) and trap-detrap site) causing an RTN in TAT GIDL current and their position in the planar MOSFET. TAT current will be discussed more detail in the next section.

### 2.5.2. Leakage currents in DRAM's access transistor

For a single DRAM cell, there are leakages from the transistor and from the capacitor itself. In this section we will discuss the different sources of leakage current in the access transistor.



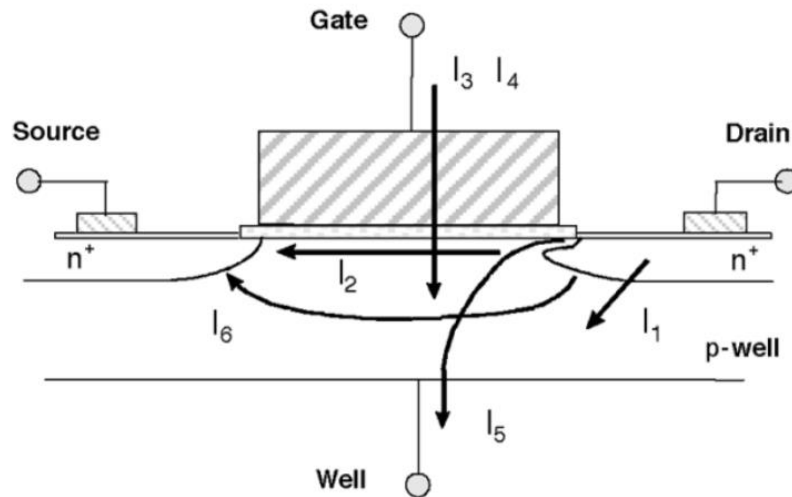


Figure 63: Leakage current paths in transistor [106].

The leakage current paths in a MOS transistor consist of:  $I_1$  - reverse-bias pn junction leakage;  $I_2$  - the subthreshold leakage;  $I_3$  - the oxide tunneling current;  $I_4$  - the gate current due to hot-carrier injection;  $I_5$  - the GIDL; and  $I_6$  - the channel punch through current.

### 2.5.2.1. *pn Junction Reverse-Bias Current*

In case of storing charges for value “1” at the capacitor, the pn junction at the storage node of the access transistor is typically reverse biased, hence there is occurrence of the pn junction leakage current. Two main components of junction leakage are the minority carrier diffusion/drift near the edge of the depletion region and the electron-hole pair generation in the depletion region of the reverse-biased junction. In the presence of a high electric field (approach  $10^6$  V/cm), the main channel of leakage is band-to-band tunneling of electrons from the valence band of the p-region to the conduction band of the n-region (illustrated in Figure 64), and the current density is described in equation (2.4).

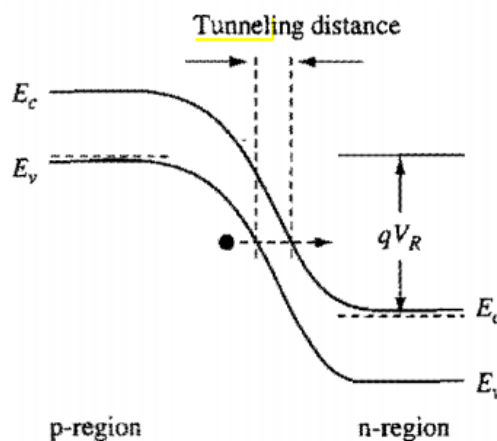


Figure 64: Schematic illustrating band-to-band tunneling in a p-n junction [107].

$$J_{BTBT} = \frac{\sqrt{2m^*}q^3EV_R}{4\pi^3\hbar^2E_g^{1/2}} \exp\left(-\frac{4\sqrt{2m^*}E_g^{3/2}}{3qE\hbar}\right) \quad (2.4)$$

where:  $E$  is the electric field;  $E_g$  is the energy bandgap;  $V_R$  is the reverse bias voltage across junction;  $q$  is electronic charge;  $\hbar$  is reduced times Planck's constant and  $m^*$  is the electron effective mass in Silicon.

### 2.5.2.2. Subthreshold Leakage

When the gate voltage is below the threshold voltage, subthreshold current occurs between source and drain of the MOS transistors. In the subthreshold region, the drain current is dominated by the diffusion current instead of the drift current [106].

In a strong inversion regime, a layer of minority carriers is formed on the channel surface and the presence of an electric field causes the drift current. In contrast, in a weak inversion regime, the diffusion of minority carriers due to a lateral concentration gradient creates the current flow within the channel. The weak inversion current density can be described as follows:

$$J_{subth} = \mu_0 C_{ox} \frac{W}{L} (m-1)(v_T)^2 \times e^{(V_G - V_{th})/mv_T} \times (1 - e^{-v_{DS}/v_T}) \quad (2.5)$$

where:  $m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{3t_{ox}}{W_{dm}}$

and  $V_{th}$  is the threshold voltage;  $v_T = KT/q$  is the thermal voltage;  $C_{ox}$  is the gate oxide capacitance;  $\mu_0$  is the zero-bias mobility;  $m$  is the subthreshold swing coefficient (also called body effect coefficient);  $W_{dm}$  is the maximum depletion layer width;  $t_{ox}$  is the gate oxide thickness and  $C_{dm}$  is the capacitance of the depletion layer.

Device scaling reduces the length of the transistor; however, it also introduces short channel effects which in turn affect the subthreshold current. When the channel is short enough, the high drain voltage can lower the potential barrier between source and drain, hence increase the subthreshold current due to the lower threshold voltage.

### 2.5.2.3. Tunneling into and Through Gate Oxide

As a result of the reduction in channel's length, the gate oxide thickness is also reduced in order to increase chip's performance. However, a thinner oxide coupled with a high electric field at the gate will increase the chance of tunneling of electron from the substrate to the gate through the oxide and vice versa.

Tunneling phenomenon happens at the Si/SiO<sub>2</sub> interface when the high electric field bends the energy pattern resulting a smaller potential barrier. The electrons that accumulate near the interface can tunnel into or through the SiO<sub>2</sub> gate layer and increase the gate current. The probability of electron tunneling depends on the thickness of the barrier, its height and its

structure. There are two different tunneling mechanisms involved: the direct tunneling and the Fowler–Nordheim tunneling.

- Direct Tunneling

In a very thin oxide (3 - 4nm [107]), electrons from the inverted silicon surface can tunnel directly through the forbidden energy barrier of the gate's dielectric layer to the gate's material. The electrons tunnel through a trapezoidal potential barrier when oxide voltage  $V_{ox}$  in Si/SiO<sub>2</sub> interface is lower than interface barrier height  $\Phi_{ox}$  (Figure 65).

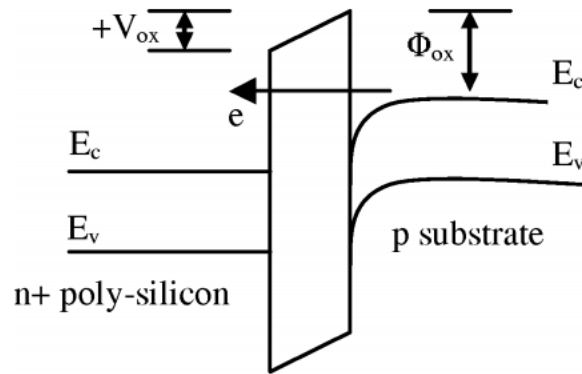


Figure 65: Band diagram of direct tunneling [106]

The direct tunneling current density can be expressed by the equation below [108]:

$$J_{DirectTunnel} = AE_{ox}^2 \exp \left\{ - \frac{B \left[ 1 - \left( 1 - \frac{V_{ox}}{\Phi_{ox}} \right)^{3/2} \right]}{E_{ox}} \right\} \quad (2.6)$$

where:  $A = \frac{q^3}{16\pi^2 \hbar \Phi_{ox}}$  ;  $B = \frac{4\sqrt{2m^* \Phi_{ox}^3}}{3\hbar q}$  and  $m^*$  is effective mass of electron in silicon conduction band.

Direct tunneling current is the composition of three major mechanisms: Electron tunneling from conduction band (ECB), electron tunneling from valence band (EVB) and hole tunneling from valence band (HVB) illustrated in Figure 66.

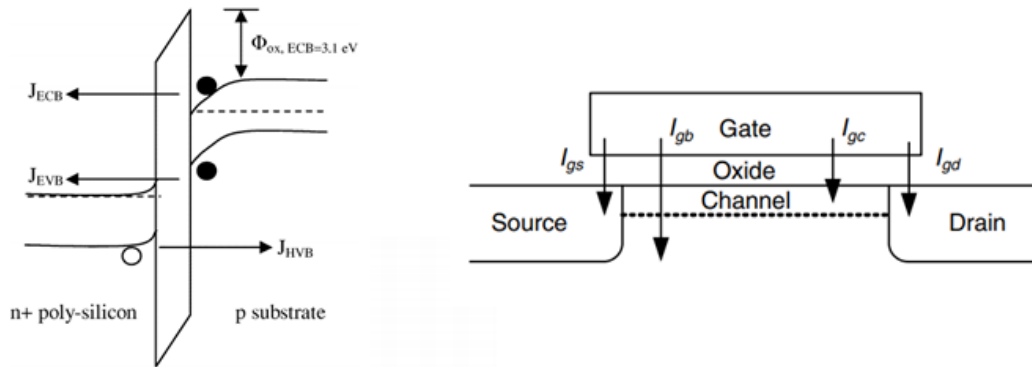


Figure 66: Direct tunneling mechanisms (left) and current composition (right) [109].

In NMOS, the ECB determines the gate to channel tunneling current in inversion, while the EVB controls the gate-to-body tunneling in depletion and inversion, and the ECB controls in accumulation. In PMOSs, HVB controls the gate to channel leakage in inversion, while EVB dominance the gate-to-body leakage in depletion, inversion and ECB in accumulation [106].

In MOS transistors, direct tunneling includes several different currents as shown in Figure 66 on the right. When the device is in the inversion region, there is a tunneling current between the gate and the channel ( $I_{gc}$ ); the current between gate and the bulk ( $I_{gb}$ ) flows both in accumulation and in inversion, and in all the operating regions there is a tunneling in the overlaps region of the gate with the source and drain ( $I_{gs}$  and  $I_{gd}$ ) [103]. The tunneling current in overlaps region has become significant with the short channel devices also called Gate Induced Drain leakage current.

The reduction of the barrier height at the Si/SiO<sub>2</sub> interface called image-force-induced barrier-lowering effect is due to the fact that the electron emission from Si to SiO<sub>2</sub> causes an accumulation of the image charge on the oxide side.

$$\Delta\Phi = \sqrt{\frac{q^3 E_{ox}}{4\pi\epsilon_{ox}}} \quad (2.7)$$

where  $\epsilon_{ox}$  is the permittivity of SiO<sub>2</sub>.

The image force effect is often neglected in the calculation of the tunneling current, however, for very thin oxides, the barrier lowering may have an impact on the calculation of the tunneling current [109].

#### - Fowler–Nordheim Tunneling

When a large positive voltage is applied to the gate metal relative to the substrate, the left side of the band diagram will be lowered in respect to the applied voltage (Figure 67).

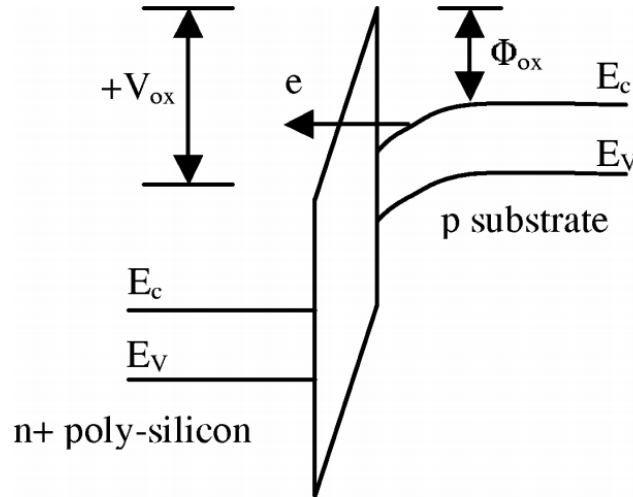


Figure 67: Band diagram of Fowler-Nordheim tunneling [106].

Contrary to the direct tunneling, when the dielectric is thick enough, the electron tunnels from the conduction band of the semiconductor to the conduction band of the oxide. Instead of tunneling through the trapezoidal potential barrier, the electrons pass through the triangular potential barrier. This tunneling current density is called Fowler-Nordheim Tunneling and can be expressed as a function of the applied voltage [110]:

$$J_{FN} = \frac{q^3}{16\pi^2 \hbar \phi_b} E_{ox}^2 \exp \left[ -\frac{4 \sqrt{2m^* \phi_b^3}}{3\hbar q E_{ox}} \right] \quad (2.8)$$

#### 2.5.2.4. Injection of Hot Carriers from Substrate to Gate Oxide

In modern MOS devices, the speed of channel's shrinkage is higher than the reduction of the applied voltage, which creates a high electric field in the channel. If the electrons and holes traveling through the channel can gain sufficient energy, they can cross the interface potential barrier and enter the oxide layer. This effect is mentioned as hot-carrier injection. In general, the injection from Si to SiO<sub>2</sub> is more likely for electrons than for holes, because electrons have a lower effective mass than holes, and the barrier height for holes (4.5 eV) is higher than that of electrons (3.1 eV) [111].

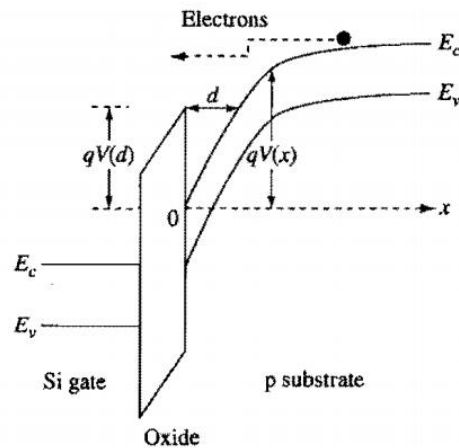


Figure 68: Hot electron injection diagram [111].

### 2.5.2.5. Gate-Induced Drain Leakage.

Gate-Induced Drain Leakage (GIDL) is one of the major leakages in MOS transistors with the presence of a high electric field at the drain junction. Especially in DRAM access transistors, when the capacitor stores the charges while the gate is usually negatively biased to suppress the subthreshold current [112]. Experimental data have shown that the GIDL is the main contribution of the tail retention time distribution for DRAM cells [113] which affects the retention characteristic of the whole chip.

When the gate receives a voltage of 0V or a negative voltage while the drain maintains a high applied voltage, the n+ drain region under the gate forms a depletion region and causes the band bending. If the electric field is high enough to cause the band bending at the oxide interface greater than or equal to the energy band gap  $E_g$  of the drain material, band-to-band tunneling will occur. The electron tunneling from the inverted drain surface to the quasi-neutral drain, and then move towards the drain. The holes left in the valence band after the electron tunneling process will move towards the substrate under the lateral electric field as illustrated in Figure 69.

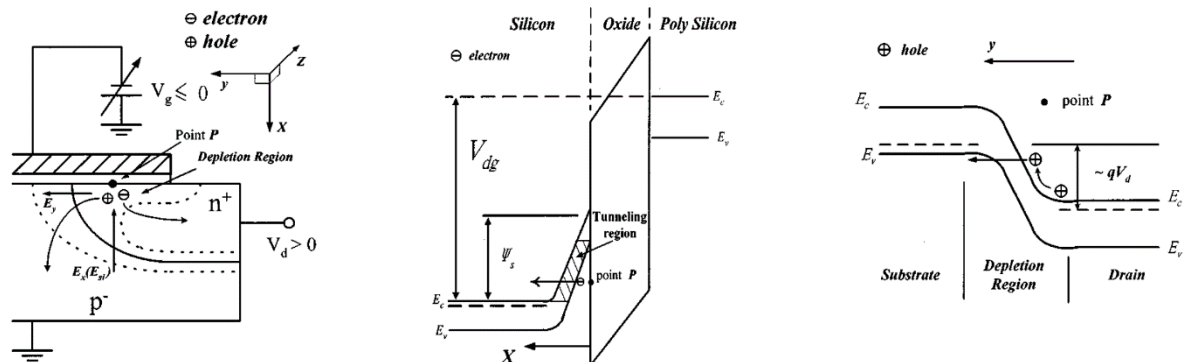


Figure 69: Cross-sectional view of a planar diode (left). Energy band diagram at point P in the x direction. Energy band diagram at point P in the y direction [114].

The tunneling current density is calculated from the Kane's tunneling [115] according to the following equation:

$$J_{GIDL} = AE^2 \exp\left(-\frac{B}{E}\right) \quad (2.9)$$

where  $A = \frac{m_r^{1/2}}{18\pi\hbar^2 E_G^{1/2}}$ ,  $B = \frac{\pi m_r^{1/2} E_G^{3/2}}{2\hbar}$  and  $E$  is the electric field.

### 2.5.2.6. Punch through

Punch through in a MOSFET occurs when the depletion layers around the drain and source regions merge into a single depletion region due to the short channel length. This creates a parasitic current deep under the substrate and cannot be controlled by the gate contact.

### 2.5.3. Leakage in storage capacitor

As mentioned in section 2.4.4, there are two methods to maintain the capacitance of the capacitor when shrinking down the device: increasing the surface area and increasing the dielectric constant. While the 3D structure allows to increase dramatically the surface area, a new high-k dielectric material is used for the new state of the art Metal-Insulator-Metal (MIM) such as: Ta<sub>2</sub>O<sub>5</sub>, ZrO<sub>2</sub>, HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub>.

For the MIM structure capacitor, there are several charge paths (Figure 70) to be transported through the dielectric: (i) thermionic emission, (ii) Fowler–Nordheim tunneling, (iii) Poole–Frenkel emission (PFE), (iv) trap-assisted tunneling (TAT), (v) trap-to-trap tunneling, and (vi) direct tunneling [116].

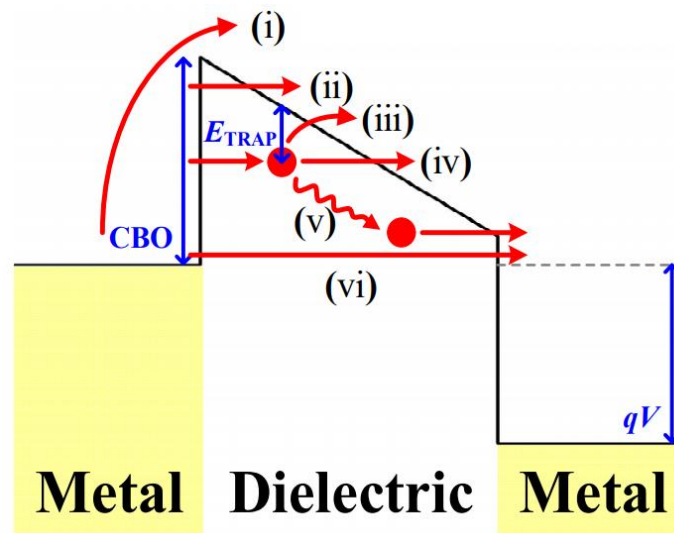


Figure 70: Leakage paths in MIM capacitor [116]. CBO is conduction band offset between the metal and dielectric layer,  $E_{Trap}$  is energy level of trap state.

When considering the dielectric is thick enough, above the limit of quantum mechanical tunneling, the dominance leakage current is the Schottky emission, i.e., the thermionic emission of charge carriers from the electrode in the conduction band of the dielectric.

The most widely used mechanism to describe leakage current for a high-k dielectric is Pool-Frenkel (PF) emission. It is due to the emission of electrons trapped inside the insulating material in the conduction band. The current density PF is given by [117]:

$$J_{PF} = CE \exp \left( \frac{-q \left( \phi_t - \sqrt{\frac{qE}{\pi \epsilon_r}} \right)}{kt} \right) \quad (2.10)$$

where  $E$  is the electric field,  $C$  is a trap-density-related constant,  $q$  is the electronic charge,  $\phi_t$  is the trap barrier height,  $\epsilon_r$  is the dynamic dielectric constant,  $k$  is the Boltzmann constant and  $T$  is the absolute temperature.

In addition to the PF emission, the trap-assisted tunneling current is also one of the main contributors to the leakage current of MIM capacitor [116]. It's composed of two steps: electrons from one electrode will tunnel to the traps then subsequently from the traps to another electrode. The expression of trap assisted tunneling current is given as follows:

$$J_{TAT} = A \exp \left( \frac{-8\pi \sqrt{2qm^*}}{3hE} \phi_t^{3/2} \right) \quad (2.11)$$

where  $A$  is a constant and  $\phi_t$  is the energy of the electron traps with respect to the conduction band edge of the dielectric.  $E$  is the electric field.

When the dielectric layer is thinner, the same approach with FN tunneling and direct tunneling is applied to calculate the leakage current.

#### 2.5.4. Radiation effects on DRAM

Despite the high sensitivity to radiation effects, DRAM is increasingly in demand for aerospace applications thanks to the high density and the help of error detection and correction code. The radiation effect on the DRAM chip can be classified as follows: Soft errors such as single bit upset (SBU) and Multiple Bit Upset (MBU); Hard errors such as Stuck Bit and our interest Weakened cells/Intermittent Stuck Bit (ISB); Single Event Functional Interrupt can be hard or soft and effect of TID.

##### 2.5.4.1. Single Bit Upset and Multiple Bit Upset

When a single ion strikes at the sensitive volume of the cell, data stored in the capacitor may be lost through access transistor or other part of the circuit due to the conductive path caused by ionizing radiation.

DRAM contain data in the form of charges in the capacitor, when the SBU occurs, the charges from the capacitor run out before the refresh period and the error is detected. Therefore, in most cases, one DRAM cell can be upset in one direction: from one to zero or from zero to one depending on the encoded value of manufacturer.



As in modern DRAM architecture, the bit-lines are configured in pairs (Figure 71), and a half will be programmed as one state while another half will be in the zero state. Since DRAM can only be upset in one direction, when the whole chip is written one (or zero), a half of the chip is vulnerable to the upset. This has been proven by previous studies [118], [119]. Moreover, when an ion striking gives a set of bit upsets in the same word, this is referred to as multiple bits upset (MBU).

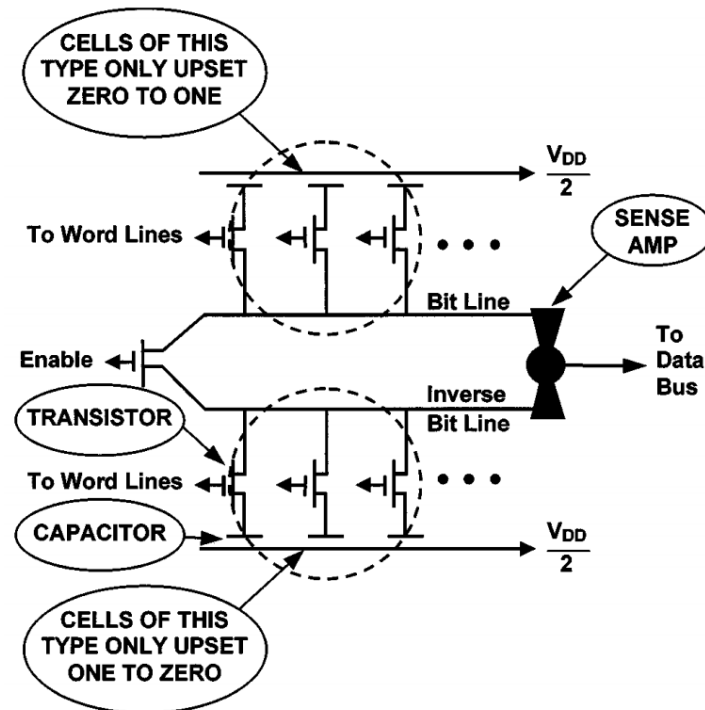


Figure 71: DRAM bit-line pair configuration [118].

The SBU and MBU in DRAM are soft errors which means the data can be re-written to the upset bit without a power cycle. Additionally, events occur on DRAM memory cells instead of peripheral circuits as in the case of SEFI. Figure 72 shows cross section per bit of few old DRAM references under proton and heavy ion irradiation.

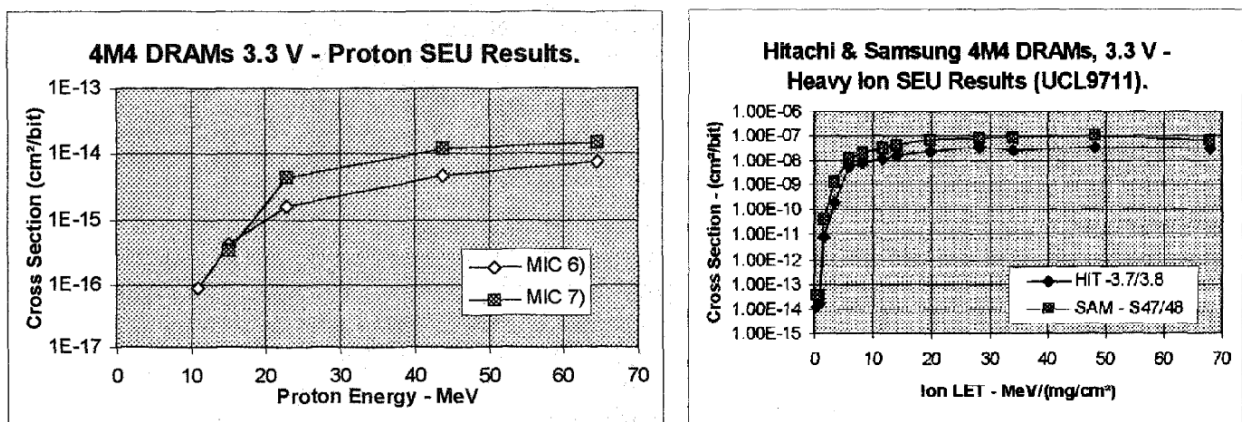


Figure 72: SBU cross section for SDRAM references under proton (left) and heavy ion (right) irradiation [120].

In new DRAM generation such as DDR3 SDRAM, the SBU cross section is significantly lower as showed in Figure 73. However, notice that chip density is much higher as well.

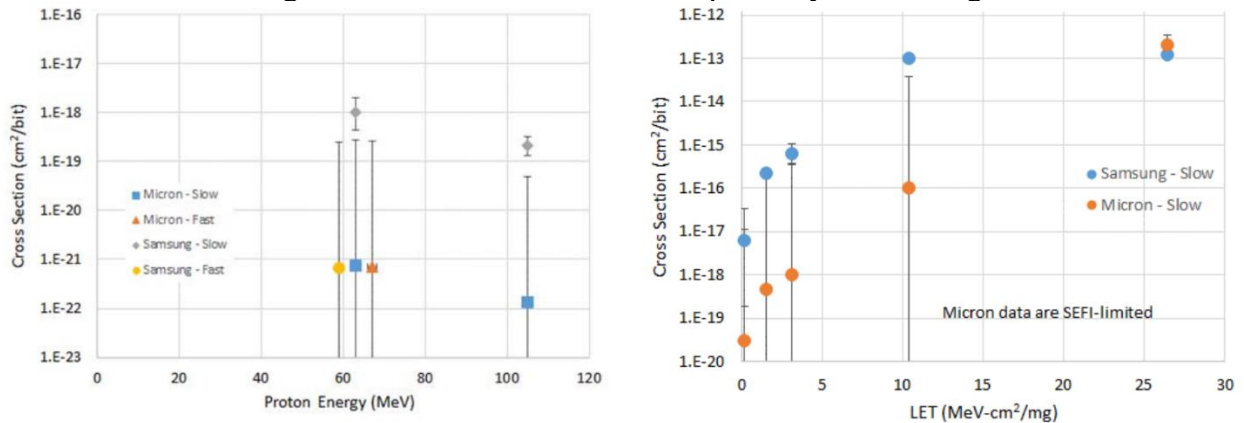


Figure 73: Cross section of DDR3 SDRAM references under proton (left) and heavy ion (right) irradiation [121].

#### 2.5.4.2. Stuck bits and Intermittent Stuck bits/Weakened cells

Stuck bits are caused by permanent damage which increases dramatically the leakage current of the memory cells. As a result, the cell will be unable to maintain data during the refresh period. The increase in leakage current is permanent, therefore re-writing the data or power cycling the device will not help recover damaged cells.

Stuck bits have been the subject of various studies in which the cause is proposed to be the displacement damage in bulk of the access transistor [60], [66].

By experiment, the comparison between the Ionization dose effect by Co-60 and the Proton experiment shows that: the number of errors increases linearly with increasing proton fluence, while Co-60  $\gamma$ -ray does not show any failure words even with a higher dose absorbed [60]. These data are also coherent with data from A. Samaras and the observation that the stuck bit can be observed at the beginning of the flight [57] and during the proton irradiation [58].

One of the previous causes of stuck bit is micro-dose. However, Edmond [66] showed that micro-dose by direct were rejected because of the small per bit cross section. Indirect ionization was also not the suitable cause because the experimental data show that the cross section increases as the irradiation energy decreases.

The cluster of defects induced by a single particle is the main cause of the stuck bit according to various evidences from experimental observation. First of all, the number of stuck bits increases proportionally to the fluence. Second, the small per-bit cross section compares to other physical mechanism. Finally, the low-energy incident particle induces a larger cross section due to a higher received NEIL as well as the increasing in the number of stuck bits when the irradiated device is unbiased [60].

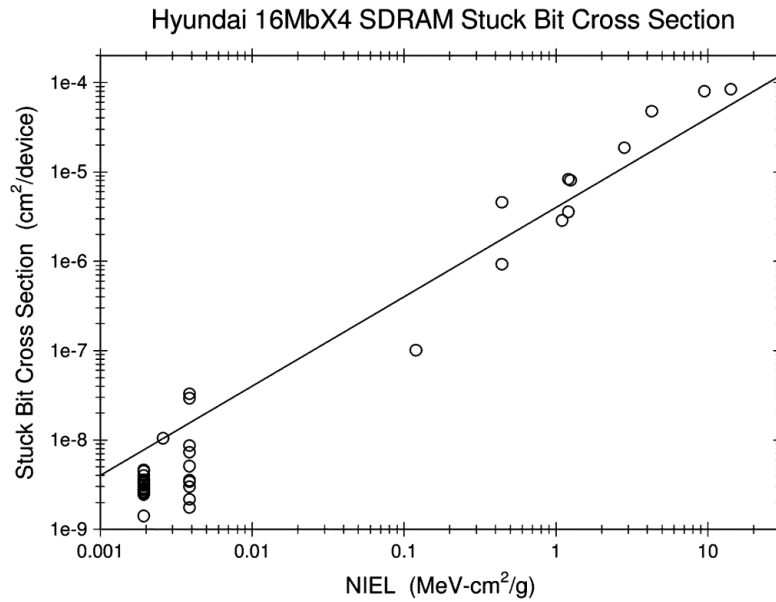


Figure 74: Stuck-bit counts versus fluence from 200 MeV protons plotted vs NEIL [66].

One particular case of Stuck bits is the Intermittent Stuck Bits which also called weakened cells, in which the damage cells can randomly get stuck and un-stuck during a period of time. The behavior was introduced in Chapter 1 is named weakened cell which is main objective of this study.

#### 2.5.4.3. Single Event Functional Interrupt

As DRAM become denser and more compact, it requires sophisticated peripheral circuit to operate consistently. SEFI is defined as a temporary functional interruption of normal operation induced by an energy particle in the sensitive volume of the peripheral circuit.

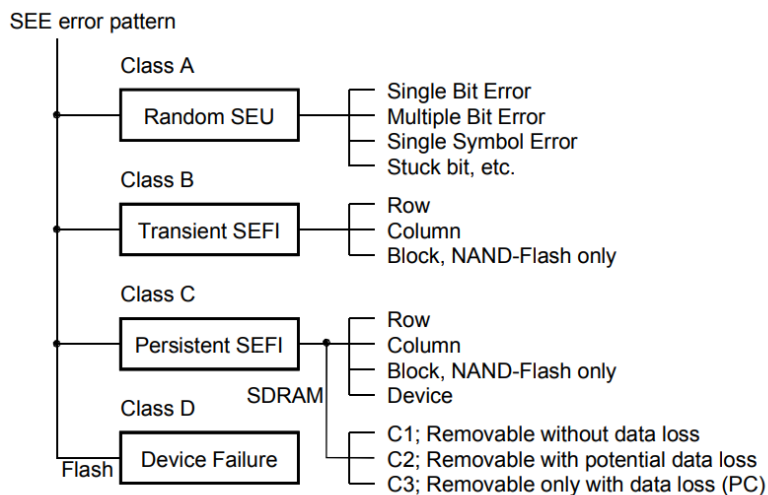


Figure 75: Error classification from [122].

SEFI, which causes a temporary non-functionality or interruption of normal operation induced by an energy particle in the affected device, can easily be dominant events for the sub-micron DRAM memories [122]. Different types of SEFIs have been classified as Figure 75. Transient SEFI appear as row errors, column errors, SEFIs originate from the internal device

control and interface circuitry and disappear on the next access. For persistent SEFIs, the error pattern can only be removed by an intervention of the memory controller or by power cycling. However, the price of this intervention is the loss of data.

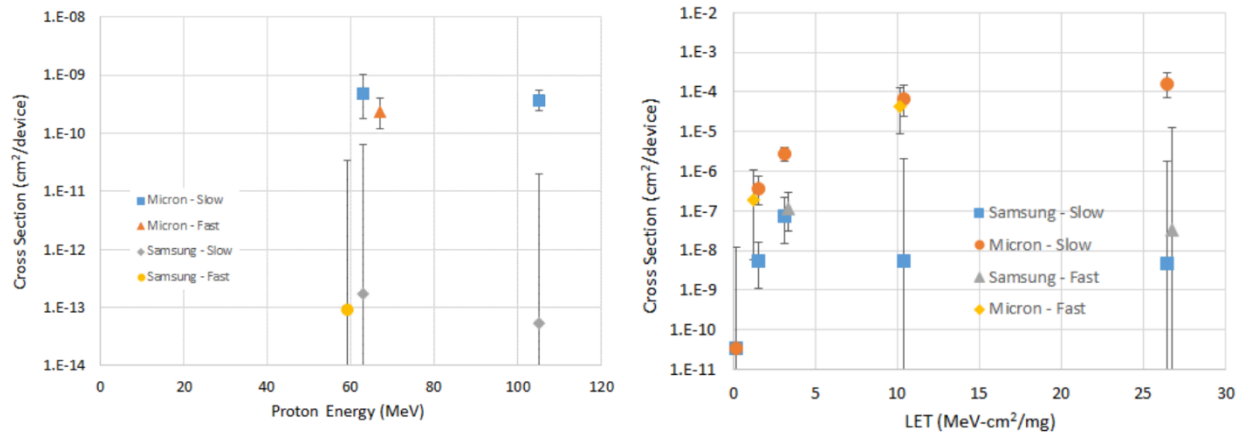


Figure 76: SEFI cross section for Micron and Samsung DDR3 SDRAM references under proton (left) and heavy ion (right) irradiation [121].

With sophisticated control circuits, new SDRAM generations are getting more vulnerable with SEFI. Figure 76 is an example of SEFI cross section under proton and heavy ion irradiation on DDR3 SDRAM.

#### 2.5.4.4. TID response

In addition to the single event effects, DRAM is also under the effects of the total ionizing dose (TID). While DATA retention time is an important characteristic of DRAM reliability, TID response of DRAM is a major concern in evaluating the retention time degradation of the memory cells.

For a specific DRAM device, the retention time is widely distributed due to the different leakage currents corresponding for each memory cell. We can also refer directly leakage current to the retention time of the cell from which experimental data can be obtained.

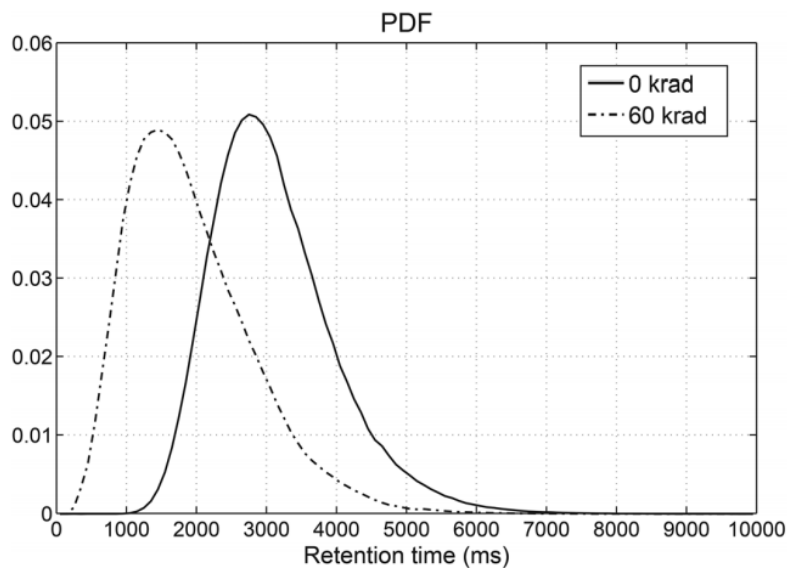


Figure 77: Probability density function of retention time before and after radiation [123].

Figure 77 shows the shift in the retention time distribution of DRAM devices after being exposed to 60krad radiation of Co-60 radiation  $\gamma$ -ray. Results show that the expected value of the distribution is reduced, but the standard deviation is slightly increased [123]. Figure 78 presents the cumulative failed bit at certain retention time up to 300ms. It is showed that retention times is gradual reduced with increasing adsorbed doses.

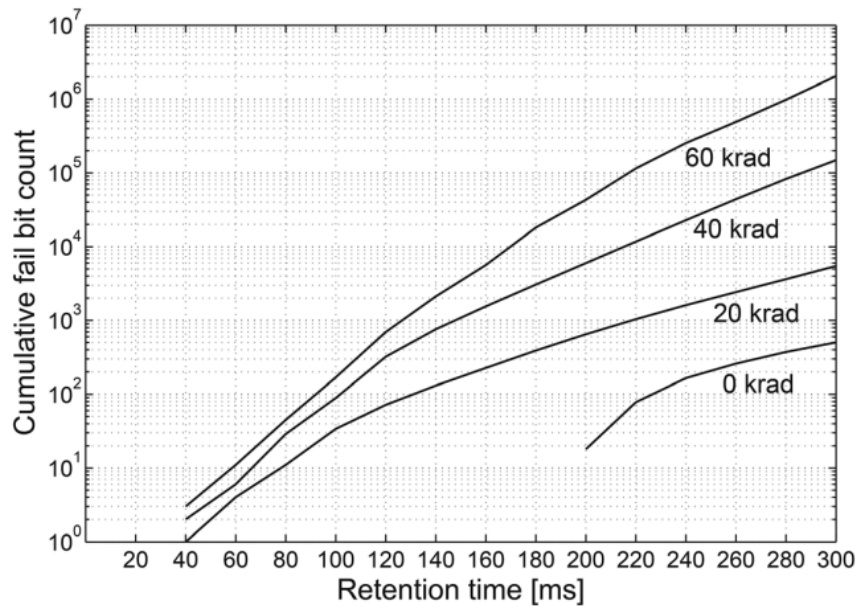


Figure 78: Cumulative fail bit count before and after radiation exposures [123].

Many studies have shown that the Gate Induced Drain Leakage (GIDL) current is the main contribution to the tail distribution of DRAM [112], [113]. As mentioned in chapter 1, two dominant mechanisms associated with TID effects in MOS oxide are positive trapped charge and interface states build-up. Moritz Fieback et al. succeed in modelling the GIDL after irradiation in [124]. Figure 79 shows the leakage currents  $I_{Rad\ GIDL}$  due to radiation and the normal GIDL current IGIDL without radiation for a single NMOS transistor. It's clear that  $I_{Rad\ GIDL}$  depends strongly on the total amount of trapped charges and increases fast with increasing drain voltage.

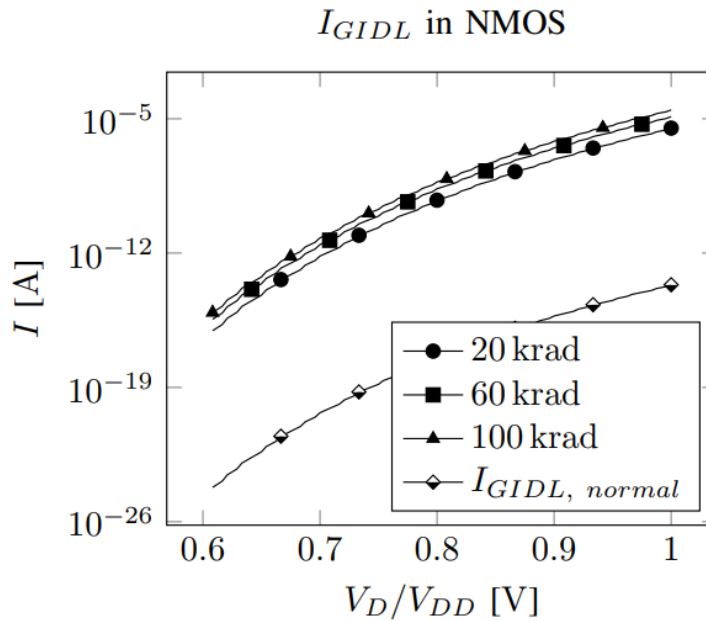


Figure 79: GIDL current due to charge trapping in a NMOS transistor [124].

## 2.6. Conclusion

As a result of market demands, DRAM manufacturers are scaling down DRAM chip aggressively in order to achieve higher density. The shrinkage of DRAM cells has introduced a new structural revolution in access transistors such as Recess Gate, FinFET and Buried Gate etc. The capacitor also evolves from a planar to a 3D structure such as deep trench and cylinder stack. All these innovations are aimed at decreasing the cell footprint and increasing the chip density. However, the limitation of leakage current is the main obstacle to extending the DRAM roadmap.

DRAM cell retention time are also on the verge of decreasing due to reduced cell capacitance. For instance, the capacitance of cell was reduced from 40fF to 25fF between the late 1980s and early 2010s.

Nevertheless, DRAMs are one of the major processor memories which will not be replaced anytime soon. In particular, with the development of Commercial off-the-shelf (COTS) devices in the space environment, it is also necessary to ensure the reliability of DRAM. Therefore, understanding the physical working mechanism of the devices themselves as well as the radiation response of the device will help maintain the future presence of DRAM in space system.

The next chapter will discuss the details of the testing facility, testing method and result of DRAM irradiation for various beam sources as well as focusing on explaining the root cause of weakened cells phenomenon.

# **Chapter 3: Experimental observation of weakened cells behavior under irradiation**

### 3.1. Introduction

Single Event Effects (SEEs) are known effects caused by space radiation on the electronic components onboard spacecrafts. In particular, Single Event Upset (SEU) is defined as an unexpected change of logic state inside digital components such as memories, FPGAs (Field-Programmable Gate Array) or microcontrollers. An SEU is not only capable of inducing data corruption in memories but also triggering a failure in complex components. SEUs are the main issue in space applications, which is why SEUs tests carried out on the ground allow evaluating the sensitivity of the event in orbit.

The inflight SEU detection on SDRAM components shows that SEU sensitivity is variable and is not consistent with ground characterization tests. These events appear to be preferential on specific addresses called weakened cells that have a greater number of errors compared to the other cells of the device. A weakened cell or so called intermittent stuck bit is identified as a memory address that frequently returns an error with always the same corruption bit. This type of error can be characterized by the following characteristics. Firstly, it is localized which means it only occurs at the preferential address; secondly, it's intermittent as the errors may randomly disappear after a period of time and re-appear; finally, it is persistent, which prevents the software from fixing the errors by restarting the devices. Hence, it is different from the hard error or stuck bit, which can permanently damage the devices.

#### 3.1.1. Previous test campaigns

Previous test campaigns performed by TRAD with the support of CNES have been conducted in order to study this type of phenomenon. Within the framework of R&T 2013 [125] (Figure 80), the initiated tests were conducted with SRAM and DRAM to highlight the phenomenon. The result shows the appearance of weakened cells under irradiation by neutrons and protons.

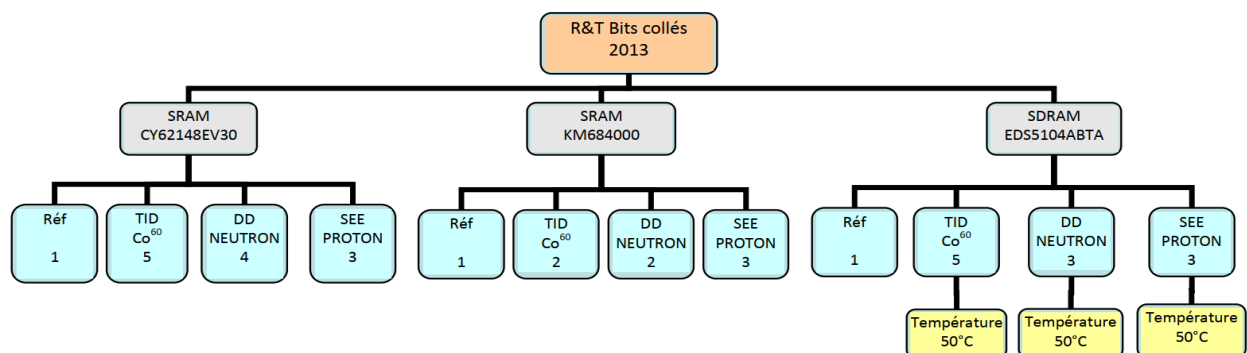


Figure 80: R&T 2013 experiment campaign [125]

In the R&T 2014 [126] (Figure 81) study, the SDRAM test bench was modified to characterize two new SDRAM references: HY57V651620BLTC (Hyundai) and EDS5104ABTA. These memories, which remained onboard the PICARD star tracker and CARMEN experiment, showed a strong sensitivity to the phenomenon. Cobalt-60, neutron and proton irradiation tests have been performed on these new references.



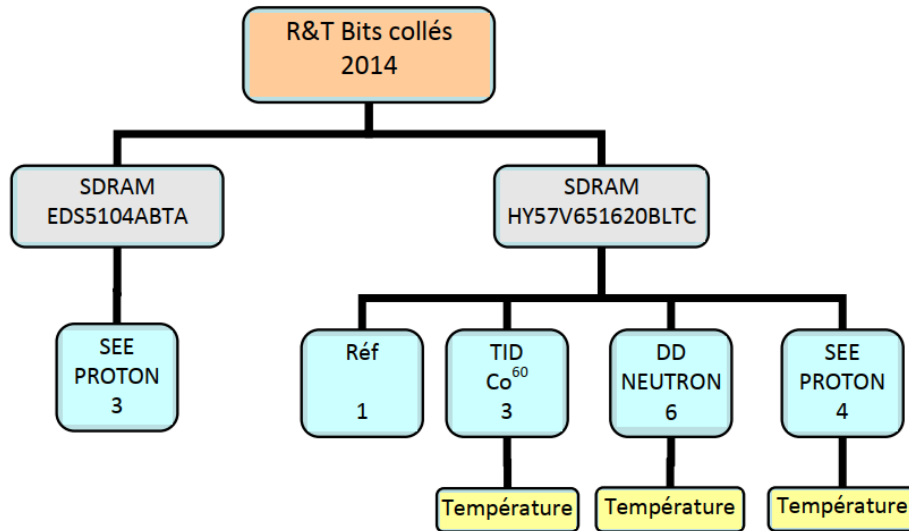


Figure 81: R&T 2014 experiment campaign [126]

The R&T 2015 [127] (Figure 82) study continued to investigate the weakened cell phenomenon on SDRAM memory components. The Cobalt 60 irradiation campaigns performed up to 300krad on unbiased devices and 50krad to device under functional test. During these campaigns no error has been detected. This is the proof that the ionizing dose alone is not the cause of weakened cells. Moreover, temperature tests on previously irradiated HY57V651620BLTC and EDS5104ABTA components were also conducted.

After excluding the effect of the ionizing dose on the phenomenon of weakened cells, the 2015 R & T focused on the impact of temperature on non-irradiated, neutron and proton irradiated SDRAM memories in order to determine a method that can reduce or annihilate the phenomenon of weakened cells.

The additional works performed in the frame of CNES study in 2015 (R&T2015 rev2) [128] showed that temperature has a significant impact on the number of erroneous addresses and on the retention time of memory cells. It was observed that for a given temperature, the number of erroneous addresses oscillates around the same value. The same observation was made for the cell retention time. In addition, this experimental campaign also showed that after applying a thermal annealing process on components irradiated by neutrons and protons, the component did not return to its original state. The retention time of all addresses has increased; however, some addresses still cannot be refreshed by the "auto-refresh" function. A plausible cause of failure would come from the logic of control that occurs during the refresh phases. This raises another hypothesis about cause of the weakened cells that need to be investigated, namely the refresh mechanism of the memory cell.

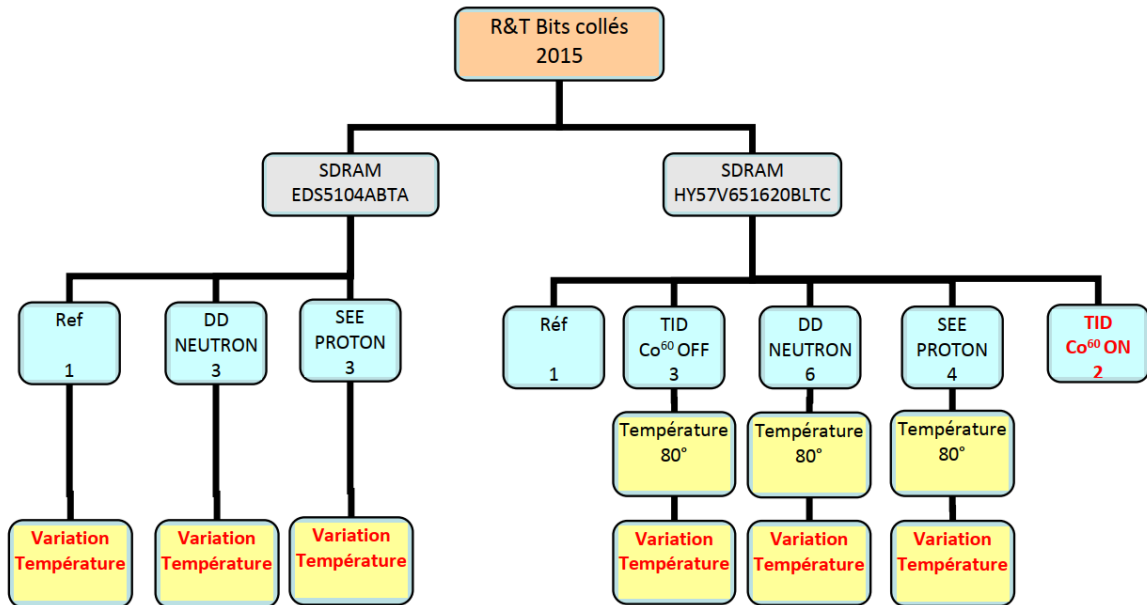


Figure 82: R&T2015 Experiment campaign [127]

In previous experiments, multiple campaigns have been performed to reproduce the weakened cells or intermittent stuck bit at ground level in DRAM. The behaviors of weakened cells must meet the criteria mentioned above: Localized, Intermittent and Persistent.

The previous experiments have also shown that the experiment with Co-60 did not induce stuck bit with an absorbed dose up to 300krad (Si) on unbiased part and up to 50krad (Si) on biased components. This can be concluded that the TID effect alone is not the main cause of weakened cells.

Table 8: SDRAM devices used in previous experiments.

Device	EDS5104ABTA-75	HY57V651620BLTC-10
Manufacture	Elpida	Hynix
Characteristic	128M × 4-bit SDRAM	4M x 16-bit SDRAM
Technology	NA	NA
Package	54-TSOP	TSTOP II-54
Vcc	3.0V - 3.6V	3.0V - 3.6V
Working temperature	0-70°C	0-70°C
Refresh	Auto refresh and self-refresh - 4096 refresh cycles / 64ms	Auto refresh and self-refresh - 4096 refresh cycles / 64ms

Proton and neutron irradiations also show that the evidences of weakened cells appear on the same components (listed on Table 8) as those used during flight. These results lead to displacement damage as the probable cause of the weakened cell effect. Moreover, the retention time degradation and refresh failure are proposed as combined effects to cause the weakened cells.

### 3.1.2. Experiment objectives

Based on those experiments, new irradiation campaigns are aimed to study the phenomenon more closely.

From the state of the art in chapter 1, the displacement damage clusters are favored by numerous researches, the new test campaigns aim at identifying any other different physical mechanisms involved. From that, we can consider which types of radiation effects is the main attributed factors. Moreover, with the increase in the density and the complexity of control circuit, SEFIs or any other refresh faulty mechanism must also be carefully examined. Other DRAM references with new technological advances are also tested for response to radiation and weakened cell phenomenon.

In addition, in the framework of this thesis, different irradiation facilities have been used, which provide a wide range of proton energies. At the beginning, Hyundai's memories are at the center of studies because they are the SDRAM reference used during the flight. However, new opportunities arise that allow to use new references from different SDRAM vendors as complementary information.

Finally, further testing is also required to study the affected cell quantitatively and coherently with the simulation results which are done at the cell level rather than at the device level.

## 3.2. Irradiation configuration

In order to have a good experimentation campaign, an appropriate test configuration must be developed. This section will discuss the details of the irradiation facilities used, the devices under test characteristics as well as the test bench.

### 3.2.1. Irradiation facilities

In the framework of this study, proton irradiation and heavy ion irradiation facilities are used to study the effects on SDRAM devices.

#### 3.2.1.1. *Proton irradiation*

- Cyclotron Resource Centre of the Catholic University of Louvain (UCL) facility

The Cyclotron Resource Centre of the Catholic University of Louvain (UCL) offers different types of radiation including protons - Light Ion Facility (LIF). The UCL Cyclone 110 accelerates protons up to 65MeV and then provides a maximum energy to devices at 62MeV. In order to achieve lower energies, a set of five remotely controlled plastic degraders enables to reach different energies from 10 to 62MeV, Table 9 shows a glimpse of the available beam's energies. For each energy, the homogeneity is greater than 10% over 80 mm diameter and the flux can be set from  $5.5 \times 10^3 - 2 \times 10^8$  proton/s/cm<sup>2</sup> [129].

Table 9: Shorten list of available Energy at UCL's LIF [129].

Energy [MeV]	LET [MeV.cm <sup>2</sup> /mg]	Range in silicon [mm]
<b>10</b>	$3.47 \times 10^{-2}$	0.71
<b>20.5</b>	$1.99 \times 10^{-2}$	2.5
<b>30.1</b>	$1.47 \times 10^{-2}$	4.94
<b>40.8</b>	$1.16 \times 10^{-2}$	8.49
<b>52.3</b>	$9.56 \times 10^{-3}$	13.21
<b>62</b>	$8.39 \times 10^{-3}$	17.87

- Paul Scherrer Institute (PSI) facility

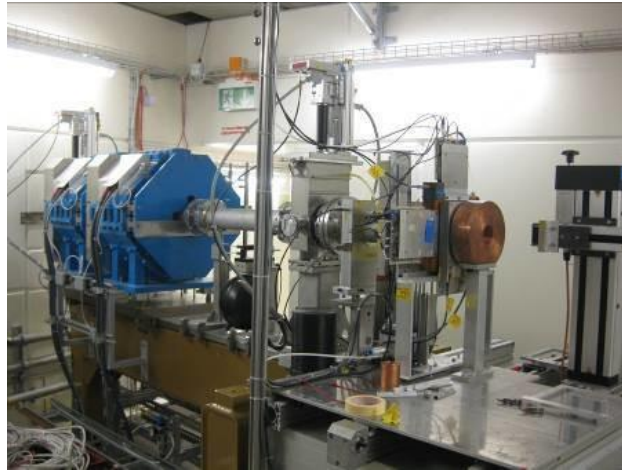


Figure 83: PIF area downstream at Paul Scherrer Institute [130].

Located in Switzerland, the PSI proton irradiation facilities (PIF) with PROSCAN accelerator provide initial energies from 74 MeV up to 230 MeV using the primary energy degrader. The beam is subsequently guided to the Experimental Area where PIF facility is located. The PIF experimental set-up consists of the local PIF energy degrader, beam collimating and monitoring devices. The maximum beam intensity in the PIF area can reach 2 nA for energies above 200 MeV, 5 nA for energies from 100 MeV to 200 MeV and 10 nA for energies below 100 MeV. The beam flux values are monitored by a set of counters and a PC-based data acquisition system. The system monitors proton flux and dose rate, calculates the total deposited dose and controls the position of the sample as well as beam focus parameters. The facility also allows the adjustment of the beam energy by means of the PIF local energy degrader [130].

Table 10: PSI PIF main features [130].

<b>Initial proton energies</b>	230, 200, 150, 100 and 74 MeV (Can be modified if requested)
<b>Energies available using the PIF degrader</b>	Quasi continuously from 6 MeV up to 230 MeV
<b>Maximum beam intensity at 230 MeV</b>	2 nA
<b>Maximum flux at 230 MeV for the focused beam</b>	$\sim 2 \times 10^9$ protons/s/cm <sup>2</sup>
<b>Beam profiles are of Gaussian-form with standard (typical)</b>	FWHM=10 cm
<b>Maximum diameter of the irradiated area</b>	9 cm
<b>Accuracy of the flux/dose determination</b>	5%
<b>Neutron background</b>	Less than $10^{-4}$ neutrons/(proton/cm <sup>2</sup> )
<b>Data acquisition</b>	Data acquisition system allows automatic runs with user pre-defined irradiation criteria
<b>Irradiation take place in air</b>	

### 3.2.1.2. Heavy Ion irradiation

In addition to the proton, heavy ions are also used to study the Single Event Effects on the electronics devices. Unlike proton irradiation, Heavy ions induce SEE primarily by depositing charges from direct ionization along the penetration track of the incident particles.

The GANIL facility is used to test electronic devices under heavy ions radiation, in a wide range of energy. SEE testing is possible with ions as Kr, Xe, Pb ... in a wide range of LET (16 to 96 MeV.cm<sup>2</sup>/mg), the main ion beams used are listed in Table 11 [131]. In practice, degraders are used to achieve the desired range and LET.

Table 11: Heavy Ions and their specifications at GANIL facility [131].

<b>Ion</b>	<b>Energy (MeV/u)</b>	<b>LET MIN (MeV.cm<sup>2</sup>/mg)</b>	<b>Range (μm)</b>	<b>LET MAX (MeV.cm<sup>2</sup>/mg)</b>	<b>Range (μm)</b>
<sup>36</sup> Ar	27	5.4	445	9.9	113
<sup>86</sup> Kr	60	11.0	1223	42.1	27
<sup>129</sup> Xe	50	26.5	685	64.3	35
<sup>208</sup> Pb	29	72.7	258	97.6	64

### 3.2.2. Device characteristics

As both the in-flight behaviors and on-ground experiments are observed on the Hyundai HY57V651620B devices, it is selected for the irradiation campaigns of this study.

The Hyundai HY57V651620B is a 67,108,864-bit CMOS Synchronous DRAM. It is organized in 4 banks of  $1,048,576 \times 16$  bits. More of its specifications have been mentioned in Table 12 and a datasheet is provided in [132]. The physical image and its pin configuration are presented in Figure 84.

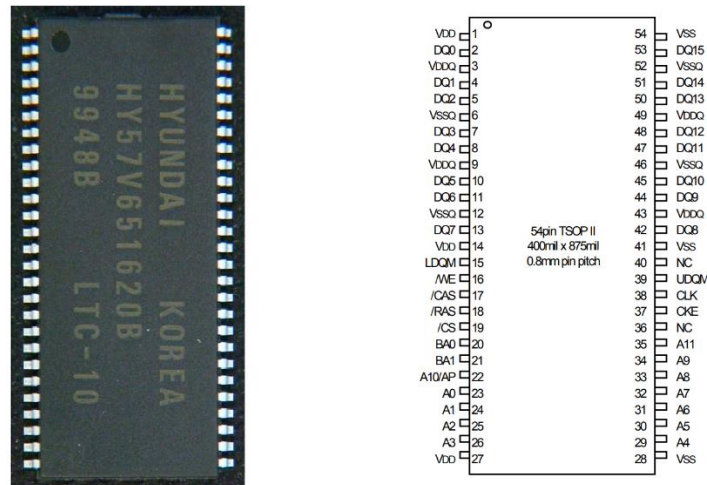


Figure 84: Hyundai HY57V651620B SDRAM and its pin configuration [132].

Because the Hyundai SDRAM devices are not available for purchase anymore on the market, new variances of SDRAM devices were selected to do more testing under irradiation. New SDAM references from Micron, Alliance and ISSI are selected according to a few criteria to be compatible with existing test benches such as: Vcc, package and organization of the chip.

Table 12: Technological specification of new SDRAM references.

Device	IS42S16400J-7TL	AS4C4M16SA-7TCN	MT48LC4M16A2P-6A
Manufacturer	Integrated Silicon Solution, Inc. (ISSI)	Alliance Memory	Micron
Technology node	72 nm	38 nm	NA
Memory size	64-Mb	64-Mb	64-Mb
Organization	1M words x 16Bits x 4Banks	1M words x 16Bits x 4Banks	1M words x 16Bits x 4Banks
Speed	143 Mhz	143 Mhz	167 Mhz
Vcc	3.3V	3.3V	3.3V
Working temp	from 0 to 70C	from 0 to 70C	from 0 to 70C
Package	54-pin TSOP II	54-pin TSOP II	54-pin TSOP II

<b>Refresh</b>	Auto refresh and self-refresh - 4096 refresh cycles / 64ms	Auto refresh and self-refresh - 4096 refresh cycles / 64ms	Auto refresh and self-refresh - 4096 refresh cycles / 64ms
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### 3.2.3. Test bench hardware configurations

The test bench was developed by TRAD and had been used in various experimental campaigns before. The test bench for this experimental campaign is composed of hardware and software components. The physical composition of the test bench includes a computer, an FPGA-based motherboard, two daughter cards with socket for SDRAM connected to two power supply boards (PSU 1 and 2), a power supply of programmable laboratory, a Guard System (SEL protection), a controller GPIB-USB, and all the necessary connectivity for the implementation of the bench.

While the main programmable power supply unit provides the general current, two power supply boards convert the received voltage into a sufficient value for two SDRAM daughter cards. These two power supply boards also act as access points for the current monitoring and latch-up detection units.

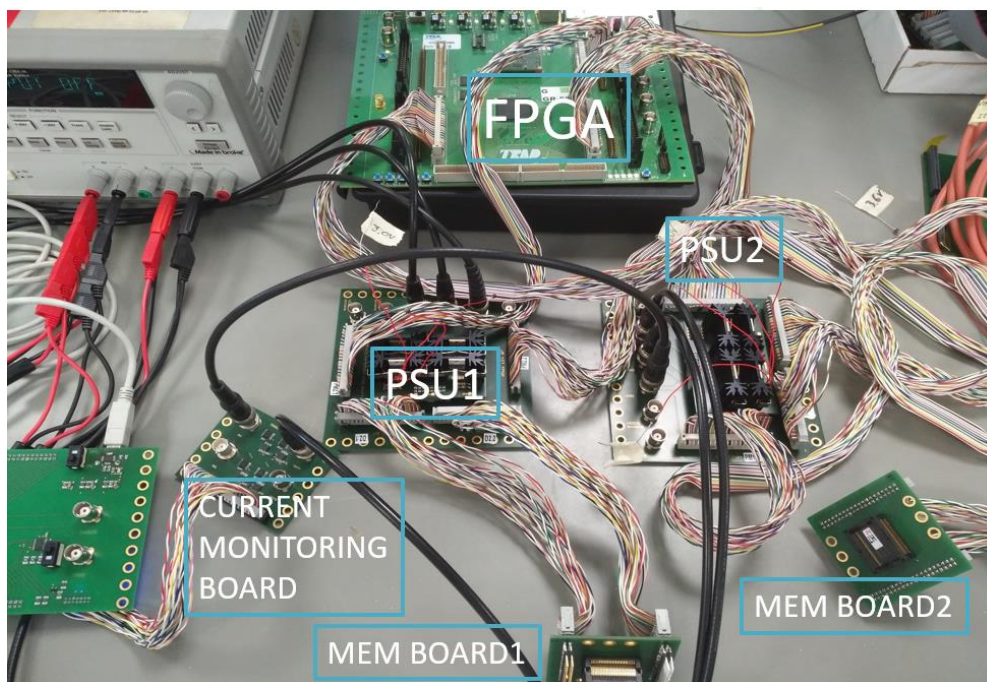


Figure 85: Testing bench assembled

The hardware was built based on the FPGA test board as the interface for the memory board and the computer. The FPGA receives the instructions sent by the computer and generates the corresponding signals to either test cards. Those commands are stored on board the memories of FGPA board to execute sequentially. This is due to the reading and writing process for the memory cell can be very fast and the transmission time of commands and instructions from the PC can affect the test result. Each interface cards transmits the signals from the FPGA to the SDRAM and manages the power supplies. The power board is fed by a programmable power supply unit that can be controlled by the computer via a GPIB-USB connection. The memory boards have interchangeable sockets in order to switch to a different memory chip.

In addition, VHDL is used to program FPGA, which is described in Figure 86.

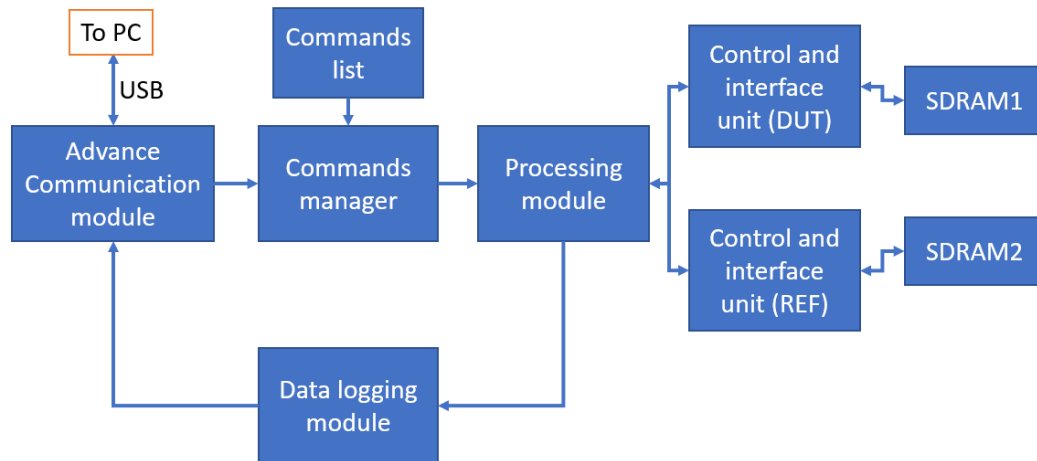


Figure 86: Test bench VHDL diagram

- Advanced Communication module

This module consists of an UART with a baud rate of 921600, a Selector and a Multi-Purpose Output Generator. It's accessible from other modules of the VHDL code within the FPGA. The module includes a decoder which allows receiving data from the PC as a set of 16-bit words as well as 8 interrupt vectors. It is also equipped with a 4Kb buffer for the larger data.

- Commands manager

This module receives a set of execution codes for the processing module and stores them in an internal memory. Triggered by interrupt vectors, it can store execution codes, delete them, or send them one by one to the processing module.

- Processing module

The function of this module is to execute different operations according to the execution codes that it has received from the instruction manager.

The operations include turning ON or OFF the power of each memory, initializing, comparing their data, checking the data of each of them, sending the counters Burst and SEL, the transmission of a synchronization frame or interruption in case of SEL. This module also includes a comparison algorithm to detect different types of errors on the memory which is described in the next part of the report.

- Data logging module

The recording of the test data is done automatically in two stages. During a run, all data sent by the FPGA is first stored as binary raw data files. These recordings are made by buffer files with a size of at least 32kB. This allows the application to run without requiring extra memory on the machine.

In a second step, when the run is finished, a results file is automatically generated with the list of errors encountered during the test run in the spreadsheet format. It contains all the events, organized in the same way as in the user interface table.

- Control and interface units



They are used to ensure the desired behaviors on the SDRAMs corresponding to the signals sent by the operations. The actions depend on the requests issued by the processing module to be performed.

- SEL detector

The detection of latch ups is not done by the FPGA card, but by the GUARAD System. However, it sends a signal to the FPGA whenever a latch up is detected. The detection module SEL continuously scans this signal in order to interrupt further operations at the level of the processing module.

### **3.2.4. Test bench software configuration**

Software is one important part of the test bench. It was built on LabVIEW and connected to the FPGA by a USB connection. The main functions of the software manage all the data streams for real-time error visualization and store on the PC storage disk, as well as exchanges of data and commands with the FPGA on the motherboard. Those include: setting parameters for the computer to interface with the FPGA (connection port, baud rate, data storage), setting parameters for memory chip according to the test (pattern, time delay, device under test), reading data from the chip and comparing with the expected data, sorting types of error based on their characteristics and last but not least giving user interface to easily control and monitor the testing process. There are two main configurations that have been used for testing: Retention time measurement and SEE (Functional) test. More details on each individually test configuration can be found in their specific sections below.

#### **3.2.4.1. Retention time test**

For every SDRAM memory cell, the retention time is the duration a cell is able to retain its information, so that when reading the cell, the information is interpreted correctly. The retention time is an important parameter to evaluate the degradation of the memory cells.

The method of this test consists of inserting longer and longer delays between writing and reading process until the data on the cell becomes erroneous. When the error occurs, the test resumes at the previous step, where no error has been detected, then, the retention time is refined from the delays that have been added. This method does not provide us the exact retention time of a cell but an approximate value. However, the accuracy of the measurement decreases from 10s to 1ms until the final measurement of the retention time.

- Test bench configuration

The testing configuration for retention time measurement is described as the diagram in the Figure 87.

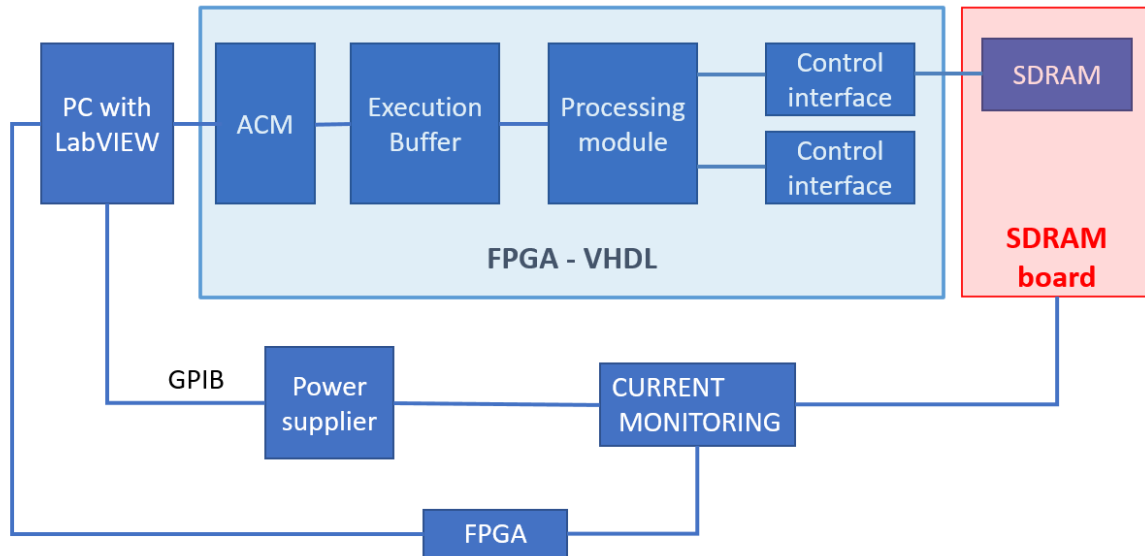


Figure 87: Testing bench configuration for retention time measurement

For the Retention time measurement, the test bench only needs to work with one targeting device that we want to measure. From the control software on the computer, we can define different patterns to write on memory cells and set the delay between the reading process, moreover we can write and read data from a specific address.

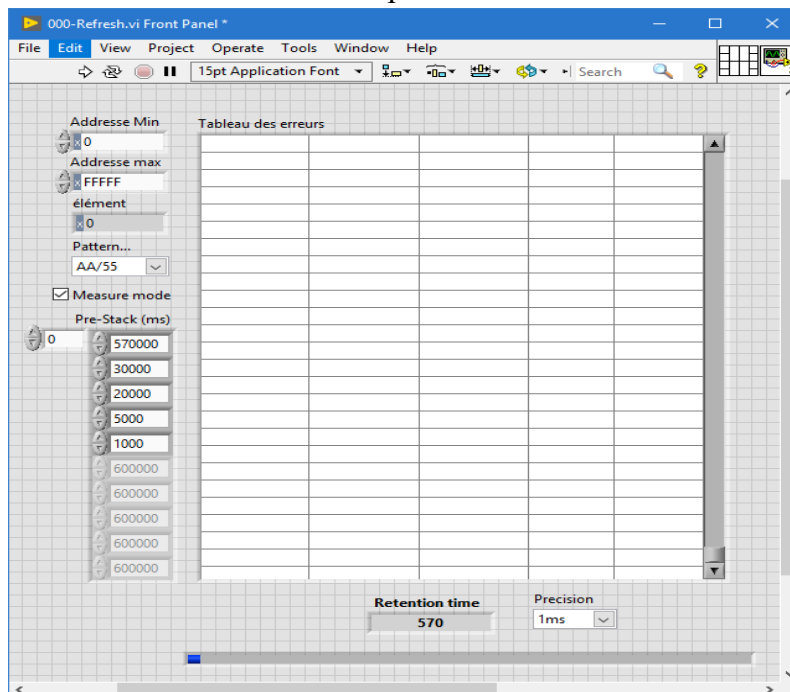


Figure 88: GUI for retention time measurement.

The software was built from LabVIEW with a graphical user interface to allow us to define the parameters of the test and monitor the result after each run. From the interface of the software in Figure 88, on the left, we can set the starting – ending address of the test, which allows us to go down to at least 1 address at a time. Next, in order to control which pattern to write in each memory cells, the Measure Mode check box allows us to measure the exact value of the retention time for specific addresses. The most important parameter for this test is the

value of different delay stacks to be added between write-read cycle. This parameter can be filled in the dialog box with decreasing numbers. Finally, we are also able to adjust the accuracy of the measurement by selecting different values at the bottom of the interface. Obviously, increasing the accuracy will increase the time consumption of the measurement.

- Testing algorithms

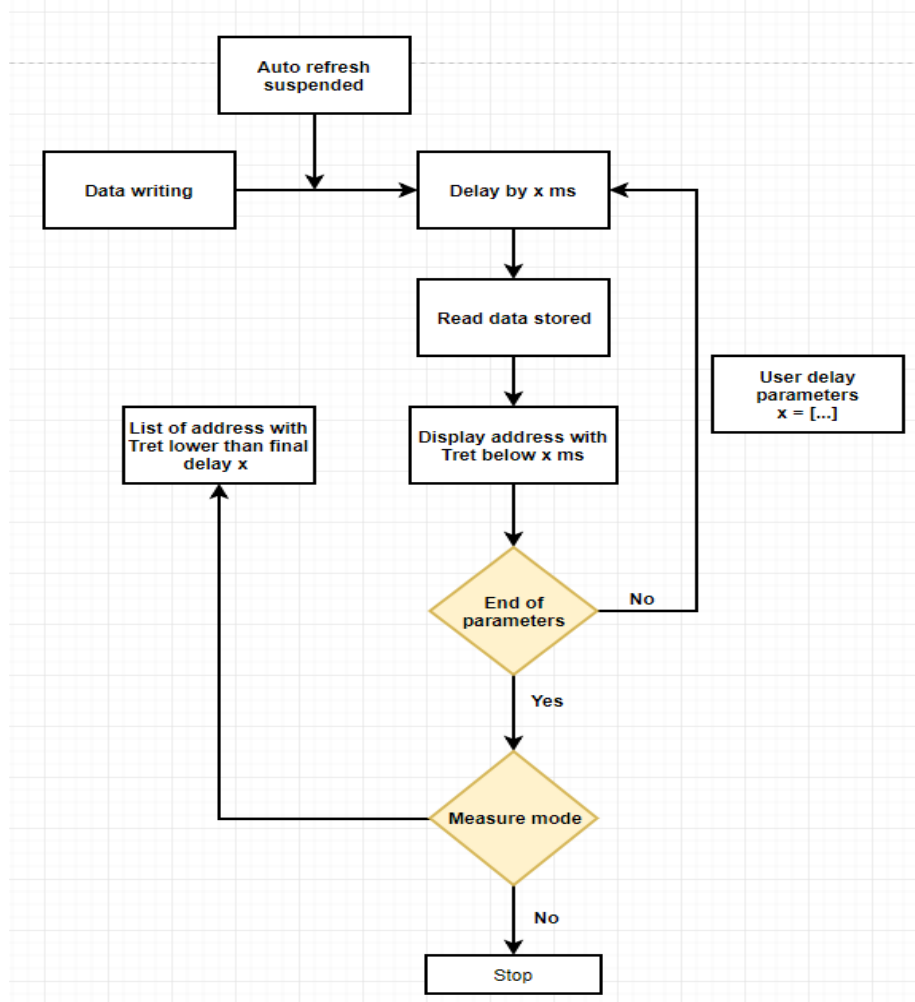


Figure 89: Retention time measurement algorithm.

The data of each memory cell will be destroyed after each operation (read, write, refresh) of the device. Therefore, after the patterns have been written to the memories, the auto-refresh mode will be suspended in order to keep the data intact from next operation mode of the memories within a defined period of time. Depending on the test, we can define different time delays to test different levels of retention time.

As mentioned before, the FPGA motherboard has two ports to connect to two SDRAM boards simultaneously. However, the Retention time measurement only needs to function with one device, therefore, first of all we must select the device under test in the LabVIEW code in order to choose the right device.

The simplified algorithm for the retention time measurement program is presented in Figure 89. At the beginning of the testing procedure, the data pattern will be written to the memory, the size depends on our pre-selection: full address or just a fraction of the whole memory. Based

on user-defined parameters, the delay time will be added before the start of the read cycle, while the auto refresh is suspended to prevent the memory from refreshing itself after a 64ms delay. The program continues to run sequentially with all of the given delay, then the result with expected data, actual data, the address of the error and the time delay for each address is displayed in the spreadsheet. However, this measurement method has few disadvantages. First, it does not show the exact value for the retention time but the population of the cells that has a lower retention time than the preset delay values. Second, the memory has more than one billion cell and the writing and reading process for the whole memory takes time. With a longer delay time, this extra time does not affect much the result because it is relatively small. However, we are dealing with some memory cells of which the retention time decreases a lot, therefore the little extra time added by the write-read cycle can counterfeit our final result.

Fortunately, the Measure Mode is added to overcome these problems. The principle of Measure Mode is basically the same as the normal working mode of the measurement. However, when the program finishes checking all the user-defined values, the Measure Mode will start to investigate every single address that has a lower retention time than the final and the lowest user-defined value. It will start with a large delay value at 10 seconds, and start to decrease automatically. Starting to decrease by 1 second, the Measure Mode will decrease to 100ms, 10ms then 1ms to get the most accurate value for the retention time. This mode will increase significantly the testing time; therefore, the user preset value should be in a descending order to help the program to run the Measure Mode as little as possible. Figure 89 represents the draft algorithm for the Retention time measurement.

#### **3.2.4.2. Functional test**

The SEE test bench was developed to detect the single event errors during irradiation to test the operation of the devices under the beam (called functional test). The different types of single events that can be detected are as follows:

- SEL (Single Event Latch-up): an SEL is detected if the consumption current of the memory becomes excessive without returning to its nominal value (current greater than 100 mA for more than 1ms since the peak current consumption of the device is around 50mA).
- SET (Single Event Transient): an SET is counted when a data recorded since the first time was wrong, then after a short waiting time (1 $\mu$ s) it recovers the correct value.
- SEU (Single Event Upset): an SEU is counted each time the system detects a corruption of the data.
- MBU (Multiple Bits Upset): an MBU is counted each time a data contains several corrupted bits in one word.
- Burst: is counted when the sequence of erroneous data appears simultaneously over a series of consecutive or non-consecutive addresses.

The principle of this test is to initiate 2 SDRAMs with an identical data pattern outside the beam and before irradiation, then to compare them continuously during irradiation. The data differences indicate the error in the memory of the device under test.

There are two functional test modes: dynamic test and static test. While dynamic test consists of continuously writing, reading and comparing the memory device under test and the

reference or pattern being written; static testing adds the desired delay time between two read cycles.

- Data pattern

There are various patterns that are used to test the memory devices such as all 1, all 0 or checker board AA/55 and reverse checker board 55/AA pattern. In this thesis, all of these pattern types are implemented on logical but not physical addresses of the test object.

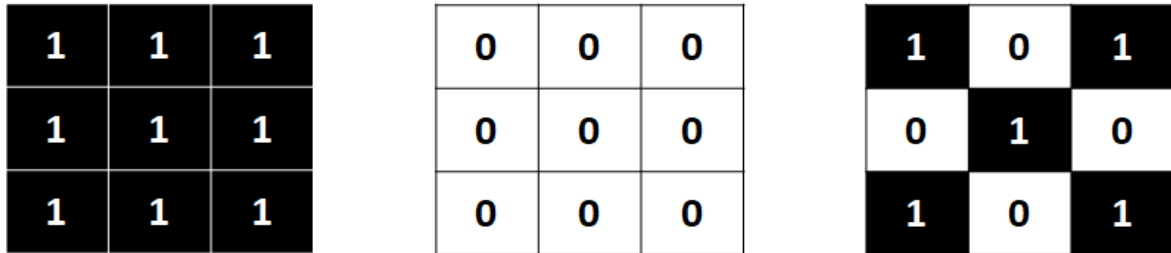


Figure 90: Different pattern using in data testing: All 1 (left), all 0 (middle), checker board or AA/55 (right).

The written pattern may have special effects on the retention time of the cell depending how manufacturer has encoded them. In fact, by using the retention time measurement for specific cells, we saw the behavior of a specific cell corresponding to the data it retains. For instance, one cell that has a certain retention time when one 1 is stored will have unlimited retention time when a 0 is written. This is due to the way manufacturers encode the value 1 or 0 for each memory cell. From our experiment data, the cell population is divided equally between 1 and 0 encoding.

- Test bench configuration

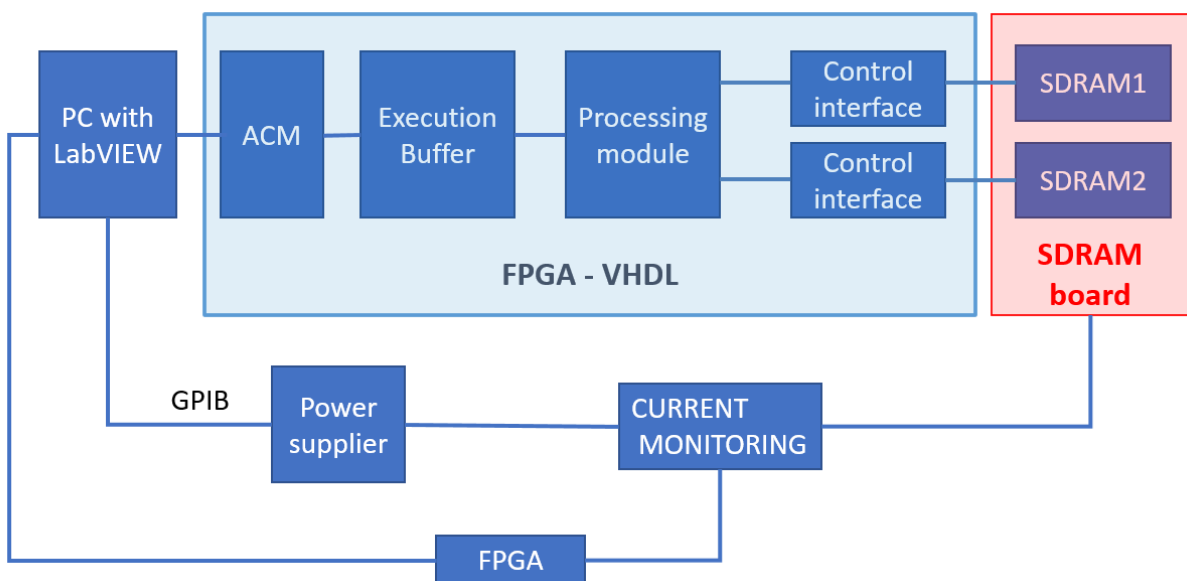


Figure 91: Functional test bench configuration

The main components are similar to the test bench for the retention time: PC equipped with LabVIEW connected by USB to the FPGA and two SDRAM boards. The SEE test configuration requires another reference SDRAM to perform the comparison at each run. The additional current monitoring board is capable of monitoring one specific device. Figure 91 shows the diagram of the functional test configuration.

The software built from LabVIEW is able to define the range of the memory address, the pattern to be written to the memory and especially the delay time for the retention time measurement.

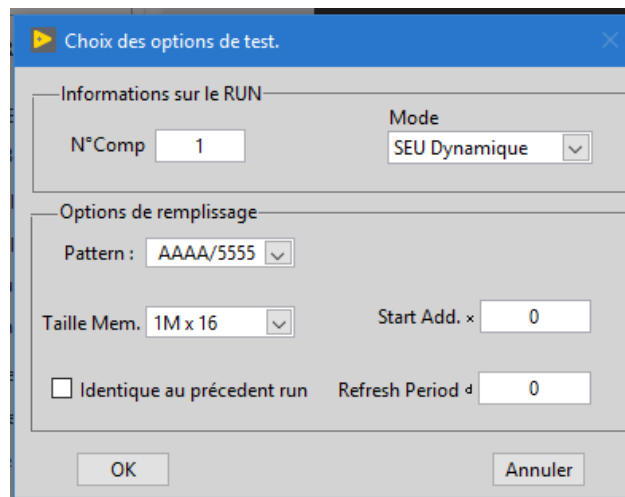


Figure 92: Set up GUI for functional test.

From each test run, the block appears to allow us to define the set of parameters to perform the test. N° Comp defines the device under test, we can choose between 0 and 1 depending on the device under irradiation, hence the remaining one is for reference. The block of parameters also allows us to set up different working mode of the test, the data patterns to be written to the memory, the size of the memory that we want to test, the starting address and finally the refresh period in ms.

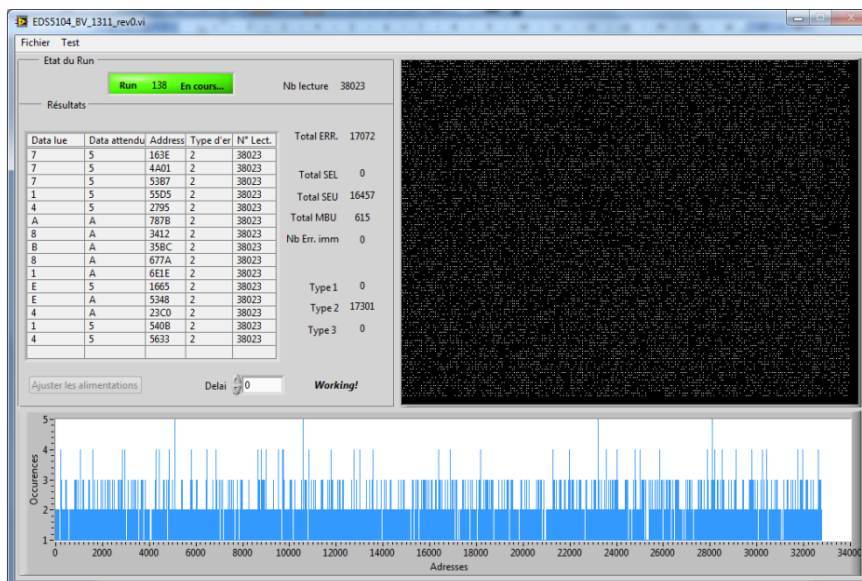


Figure 93: GUI for functional test

Figure 92 and Figure 93 show the set up and working GUI of the software. The user interface allows us to monitor the real time information. The spreadsheet on the left displays the last event occurred. Right next to it, we can see the real time value of: total read cycle, total errors, number of specific types of errors.

On the right, a graph representing the memory mapping displays white dots corresponding to the decoding of the addresses where an error was detected. This does not represent exactly the physical property of the devices but it gives us a good overview of the distribution of errors. In the lower part of the interface, the histogram shows the occurrence of the number of errors per address. This visualization is particularly suitable for the problem of weakened cells because if an address has recurring defects, we will see a peak on the histogram.

Once all the parameters have been entered, they are sent to the FPGA via a USB connection, and the test sequence is launched. During the initialization phase, a check is carried out on 2 SDRAM memories to ensure that the tested parts are functional. For test campaigns carried out after irradiation, the program will indicate in most cases that the devices are not in good condition, but this does not affect the test result.

- Test algorithm for detecting error types



Figure 94: Functional test error types detection algorithm.

The stored data will be read and compared with the write pattern to detect the error for each memory address. From there, the errors will be classified into different categories. The algorithm for classifying the types of error is described in Figure 94. If the error is detected by the mismatch of the read data, the reading will be performed again to make sure it's not the error type 1: false error of the reading process. If the error persists, the data will be re-written then re-read at each error address. After this write-read cycle, the address without the error will be classified as Error type 2: SEU/MBU. In case the errors are still present and not correctable on specific addresses, these are Error type 3: Hard error/Stuck bit.

### **3.2.5. Refresh mode**

For each DRAM device, there are two main refresh modes that can be selected by the user: self-refresh and auto refresh.

Self-refresh is low-power mode in which the DRAM maintains the refresh action internally. By deactivating the clock, DRAM executes the refresh operation by using internal refresh counter. Meanwhile, auto refresh is active command that is sent to the device to execute the refresh. This command is nonpersistent, so it must be issued each time a refresh is required. The interval between two refresh commands is standardized by JEDEC at 64ms. For instance, the 64Mb SDRAM with 4096 rows configuration will require 4096 auto refresh cycles every 64ms.

There are two ways to run the refresh command: distributed refresh and bulk refresh. For distributed refresh, it needs to provide an auto refresh command every  $15.625\mu\text{s}$ . On the other hand, a bulk of 4096 refresh command can be issued once every 64ms.

In this thesis, both distributed refresh and bulk refresh have been used depending on specific devices.

## **3.3. Test plan**

For each test run, a test scenario is provided in order to standardize the data recording scheme. Each device is functionally tested before irradiation to ensure the integrity of the test under beam. Moreover, each device is also characterized in terms of retention time in order to perform the comparison after irradiation.

### **3.3.1. Proton irradiation**

The proton irradiation had been carried out at UCL and PSI. The device under test was Hyundai HY57V651620.

For proton beam available at UCL, the test plan is mentioned in Table 13 with the Hyundai devices. Two main levels of energy are selected at 62MeV and 40MeV. Different fluence levels have been pre-selected to highlight the dependence of the upset rate and up to  $10^{11}\text{p/cm}^2$  which is recommended limit [133].

Most of the tests include multiple devices and are divided into two groups: Active functional test and un-biased devices. The general functional tests were run with AA/55 pattern. Moreover, all 1 (FFFF) and all 0 (0000) pattern were also used in order to identify the effect of the stored pattern on the sensitive of the devices.



Table 13: Test plan for proton irradiation at UCL on 26/02/2019.

Order	Beam energy	Fluence	Test parameters
1	62 MeV	$3.6 \times 10^{10} - 1.08 \times 10^{11}$ p/cm <sup>2</sup>	Dynamic functional test. Pattern AA/55, memory size 1Mx16 bit, refresh period 64ms. Unbiased.
2	62 MeV	$3.6 \times 10^{10}$ p/cm <sup>2</sup>	Dynamic functional test. Pattern FFFF, memory size 1Mx16 bit, refresh period 64ms. Unbiased.
			Dynamic functional test. Pattern 0000, memory size 1Mx16 bit, refresh period 64ms. Unbiased.
3	40 MeV	$3.6 \times 10^{10} - 9 \times 10^{10}$ p/cm <sup>2</sup>	Dynamic functional test. Pattern AA/55, memory size 1Mx16 bit, refresh period 64ms. Unbiased.

In addition to the proton experiment at UCL, another irradiation campaign was also carried out at the PSI facility with a higher energy and new devices. Three new SDRAM references from Alliance, ISSI and Micron manufacturer were selected (Table 14). These new devices were selected according to their suitable specifications to ensure a minimal modification of existing test bench available at TRAD. The irradiation campaign at PSI is under the support from European Space Agency (ESA).

Table 14: New SDRAM references for testing at PSI facility from 07/03/2020 to 08/03/2020.

Manufacturer	Name	Process technology	Size	Organization	Refresh rate	Package
Alliance	AS4C4M16SA	38nm	64Mb	1 Meg Bits x 16 Bits x 4 Banks	4096/64ms	54-pin TSOP II
ISSI	IS42S16400J	72nm	64Mb	1 Meg Bits x 16 Bits x 4 Banks	4096/64ms	54-pin TSOP II
Micron	MT48LC4M16A2	N/A	64Mb	1 Meg Bits x 16 Bits x 4 Banks	4096/64ms	54-pin TSOP II

The main difference between the new references and the previous Hyundai device is the refresh mode. While the Hyundai device uses bulk refresh, all three new references use distributed refresh.

Table 15 summarizes the test run of the new references.

*Table 15: Test run summary for new references at PSI facility from 07/03/2020 to 08/03/2020.*

Order	Beam energy	Total Fluence	SDRAM reference	Test parameters
1	200 MeV	$10^{11}$ p/cm <sup>2</sup>	ISSI	Dynamic functional test. Pattern AA/55, memory size 1Mx16 bit, refresh period 64ms.
		$10^{11}$ p/cm <sup>2</sup>	Alliance	
			Micron	
2	121.45 MeV	$2.01 \times 10^{11}$ p/cm <sup>2</sup>	Micron	
3	60.8 MeV	$2.0 \times 10^{11}$ p/cm <sup>2</sup>	Micron	
Post irradiation				
4			Micron	Dynamic functional test. Pattern AA/55, memory size 1Mx16 bit and 4Mx16bit, refresh period 64ms. Retention time measurement.
6			ISSI	Dynamic functional test. Pattern AA/55, memory size 1Mx16 bit and 4Mx16bit, refresh period 64ms. Retention time measurement.

### 3.3.2. Heavy Ions irradiation

The heavy ion Irradiation campaign took place in the GANIL facility with two samples named H1 and H23. The aim of this experiment is the appearance of weakened cells under heavy ion irradiation.

One extra step of the heavy ion irradiation is that we have to open the chip packet to expose the silicon die directly under beam. Figure 95 shows the device that has been delidded.



Figure 95: DRAM delidded backside (left) and front side (right).

The objective of the Heavy Ions campaign is to confirm the existence of weakened cells and supplementary effects; therefore, the main goal is to detect the largest number of weakened cells. Multiple runs are used to find the sensitive volume of the devices. Table 16 is a summary of each run of the H1 and H23 devices under  $^{129}\text{Xe}$  ion. The beam energy had been adjusted to give highest LET at estimated sensitive region from 245 to 255 $\mu\text{m}$ .

Table 16: Heavy Ion irradiation runs information perform by TRAD in April 2019

Run	Device	Energy (TRIM) (MeV/nuc)	Degrader Aluminum ( $\mu\text{m}$ )	Air (mm)	LET at surface (MeV.cm <sup>2</sup> /mg)	Range ( $\mu\text{m}$ )	Mean LET at 245-255 $\mu\text{m}$ from OMERE (MeV.cm <sup>2</sup> /mg)
1	1	45.92	0	82	26.97	686.45	34.1
2	1	45.92	0	82	26.97	686.45	34.1
3	1	34.21	200	100	32.03	452.25	48.62
4	Run Functional						
5	1	24.21	350	100	38.49	284.94	32.97
6	1	26.84	300	125	36.52	326.01	68.88
7	23	26.84	300	125	36.52	326.01	68.88
8	23	26.84	300	125	36.52	326.01	68.88

For details test run are provided in Appendix A.

### 3.4. Test results

The test results of the irradiation campaigns will be divided into two parts: retention time degradation and functional test.

First, the degradation of retention time under radiation is examined. By using retention time degradation cross section, it is possible to compare between different irradiation conditions and manufacturers. Then, the functional test will record the effects of a single event of the device under beam to investigate, while the weakened cells are focused in order to see their behaviors and to give proposals for modeling and simulation works.

### 3.4.1. Retention time degradation

As discussed in chapter 2, the amount of time that DRAM can maintain the data in the cell is called the retention time. Under irradiation, DRAM cell retention time is reduced, hence, the retention time is used to evaluate the degradation level of DRAM. Moreover, the retention time measurement of specific cell can provide more information about the phenomenon of weakened cells.

#### 3.4.1.1. Proton Retention time degradation

The cross section for the retention time degradation is evaluated according to the method of Shindou [60] and Rodriguez [58] by dividing the increase in the number of error bits at each refresh rate by the total fluence.

$$\sigma_{(t_{ret} < t_{delay})} = \frac{N - N_0}{\Phi}$$

where  $N$  and  $N_0$  is the number of addresses that fail to maintain the data for a specific delay time after irradiation and before the corresponding irradiation,  $\Phi$  is the total fluence in p/cm<sup>2</sup>.

- Retention time degradation from UCL campaign

The series of the delay time as input for the test is a decreasing series ranging from 100s to 100ms. During the test, none of the addresses fall below the 64ms refresh period of the JEDEC standard.

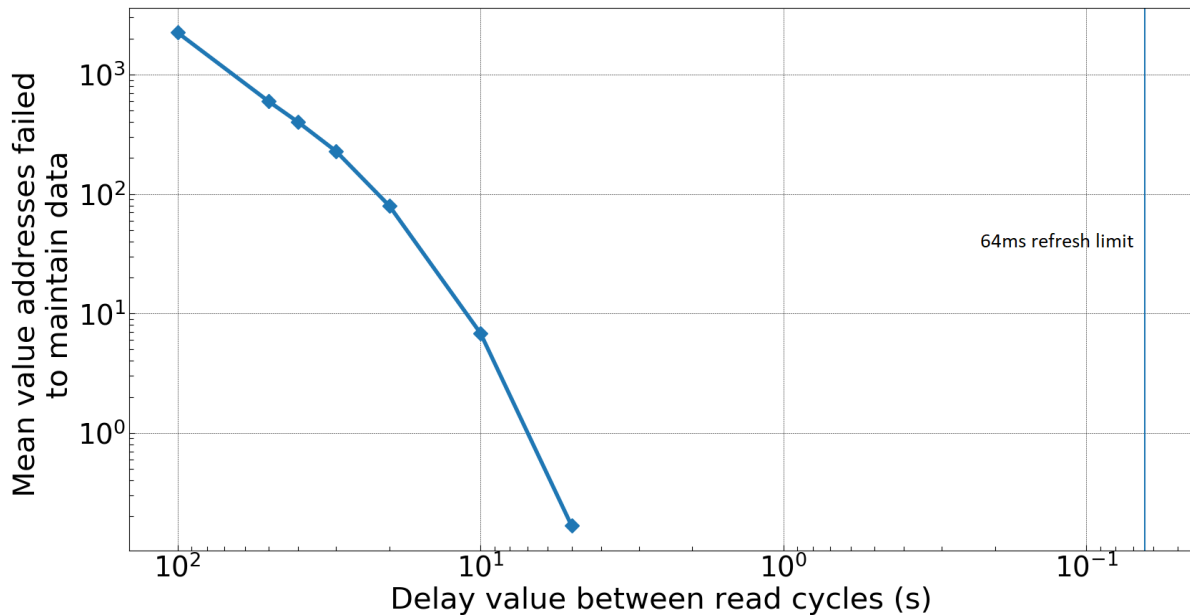


Figure 96: Mean value of number of addresses failed at specific time delay for 24 Hyundai pristine devices (before irradiation).

Figure 96 shows the average number of failed addresses of Hyundai devices at different delay time between read cycles before irradiation. The lowest retention time measured of a pristine device is well over than 5 seconds, taking into account the 64ms refresh limit, which means that the memories function as expected.

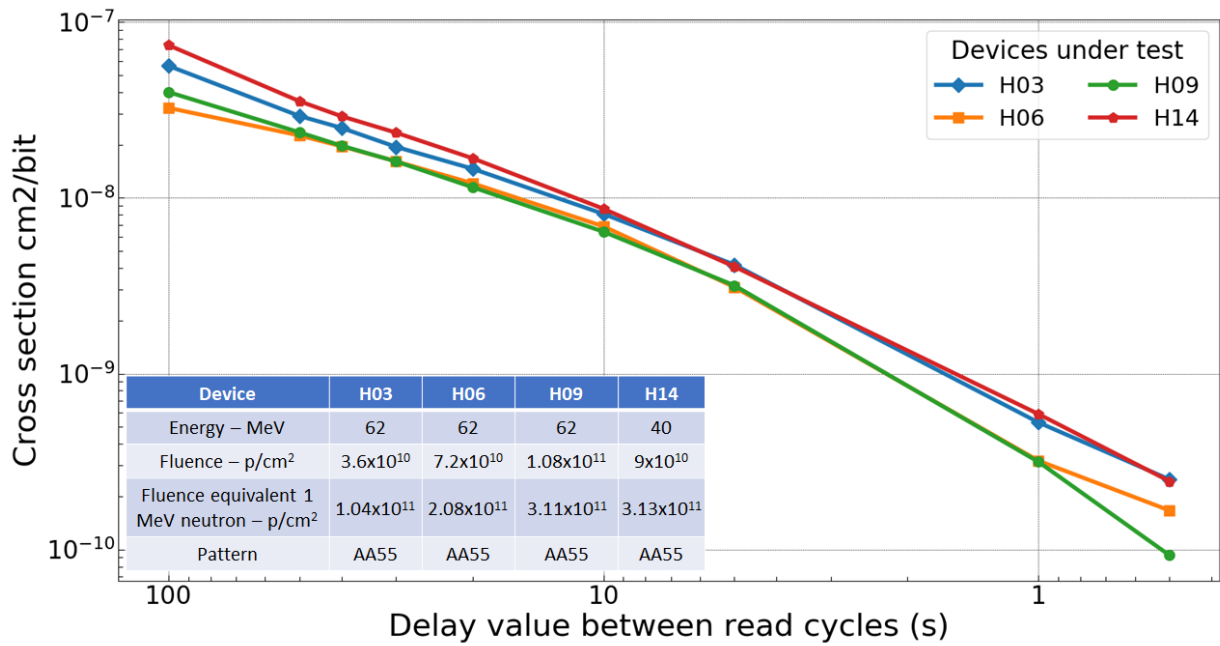


Figure 97: Retention time degradation of four Hyundai references H03, H06, H09, H14 after proton irradiation with pattern AA55.

After irradiation, cell degradation is visible for all delay values where the number of failed addressed has increased. Figure 97 describes the retention time degradation in cross section of the references: H03 ( $3.6 \times 10^{10}$  p/cm<sup>2</sup>), H06 ( $7.2 \times 10^{10}$  p/cm<sup>2</sup>) and H09 ( $1.08 \times 10^{11}$  p/cm<sup>2</sup>) were irradiated at 62 MeV and H14 ( $9 \times 10^{10}$  p/cm<sup>2</sup>) at 40 MeV. The cross-section curves are similar with a different fluence. This result indicates that the damage induced by the irradiation is proportional to the total fluence.

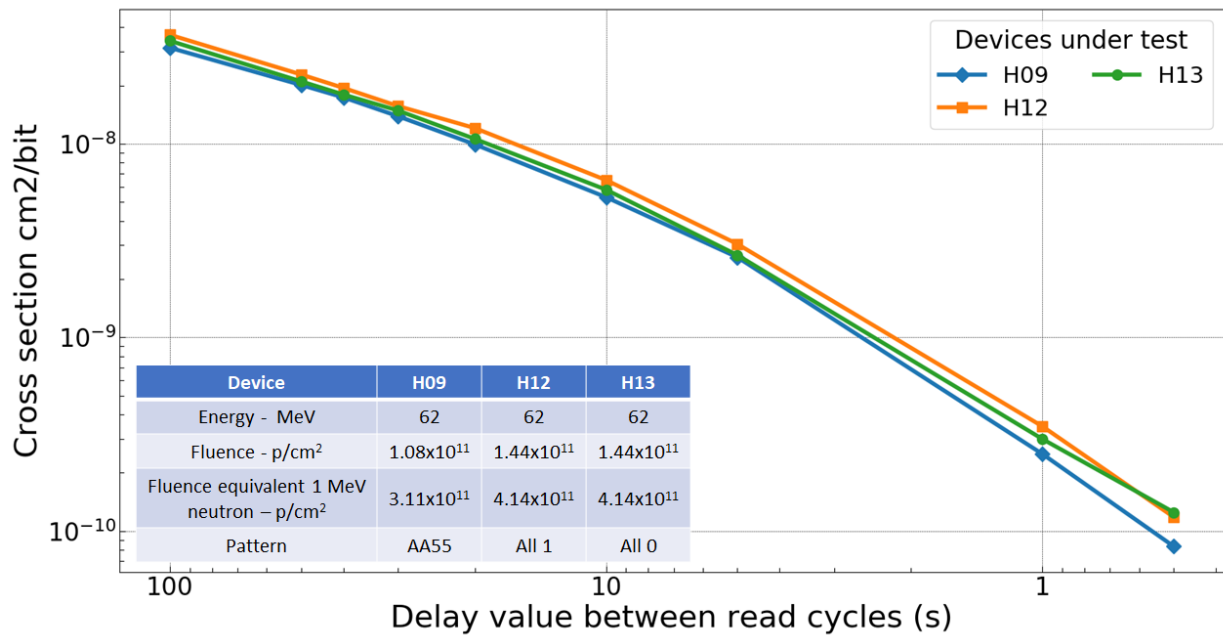


Figure 98: Retention time measurement between device with different data patterns.

Normally the devices are tested with a checkerboard (AA/55) pattern, however, in order to identify the effect of pattern, the special run with all 1 and all 0 are also performed. The cross-sectional curve of the retention time measurement of all 1 and all 0 patterns on 2 devices H12 and H13 is plotted in Figure 98. It clearly shows that the retention time degradation is not affected by the pattern written on the device during irradiation. This result is also coherent with the upset rate from the heavy ion experiment where the cross sections between checkerboard pattern (AA55) and reverse checkerboard pattern (55AA) are not distinctive.

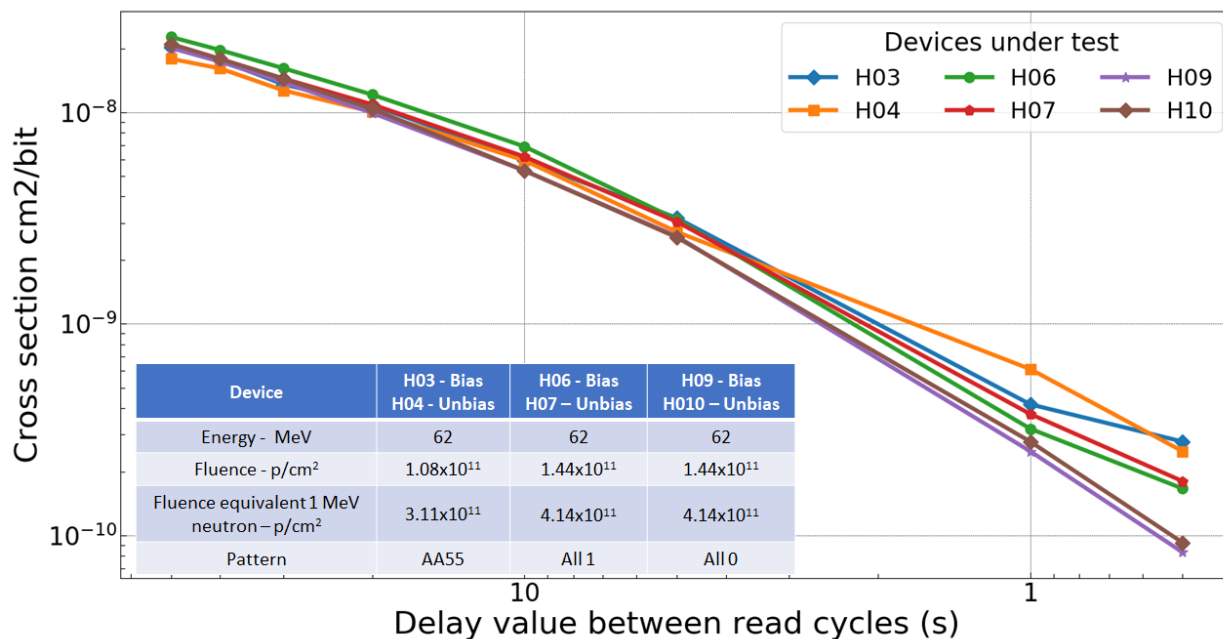


Figure 99: Retention time between biased and unbiased (floating) devices

In addition, Figure 99 presents the cross-section of the devices with different bias condition. For each irradiation condition, one device is actively biased and functionally tested, while another device is unbiased. The cross-sectional curves do not change with three level of irradiated fluence, and there is no significant difference between biased and unbiased devices.

- Retention time degradation from PSI irradiation campaign

For the second proton irradiation at the PSI, the dependent fluence of the retention time degradation was observed in the same way as during the UCL campaign.

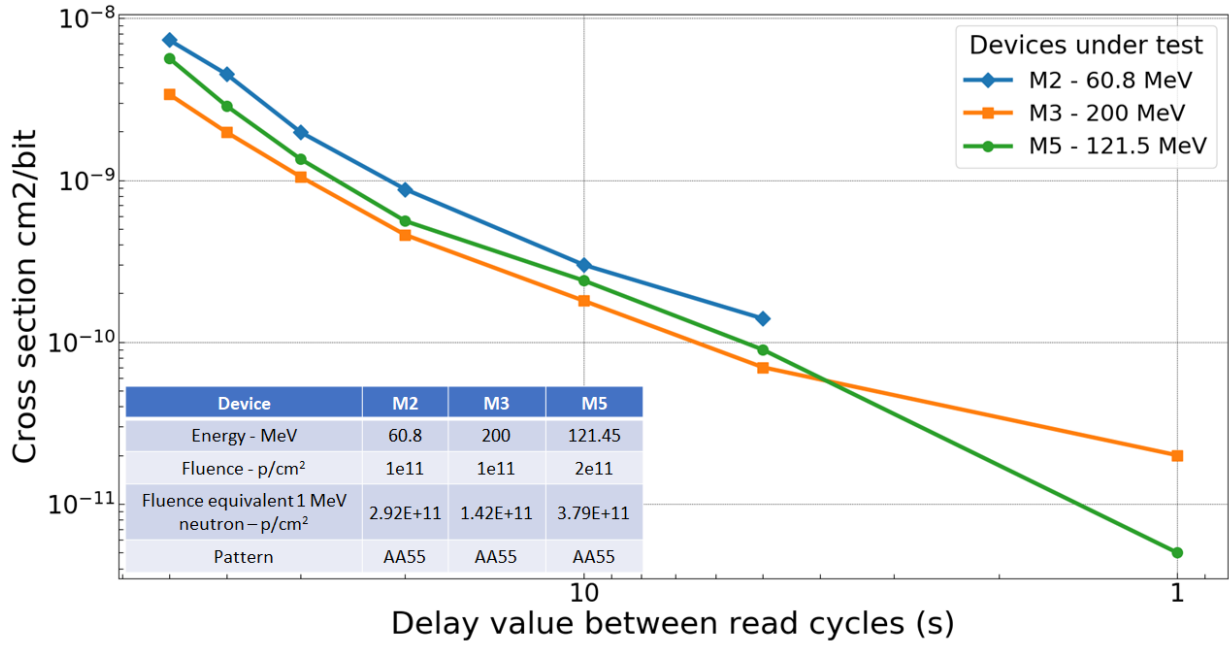


Figure 100: Retention time degradation for Micron devices with different fluence.

Figure 100 shows the retention time degradation cross section for M2 ( $10^{11}$  p/cm<sup>2</sup> – 60.8MeV), M3 ( $10^{11}$  p/cm<sup>2</sup> – 200MeV) and M5 ( $2 \times 10^{11}$  – 121.45MeV). It indicates that the cross section is higher with lower proton energy, since the lower proton energy can deposit higher energy to the silicon [43].

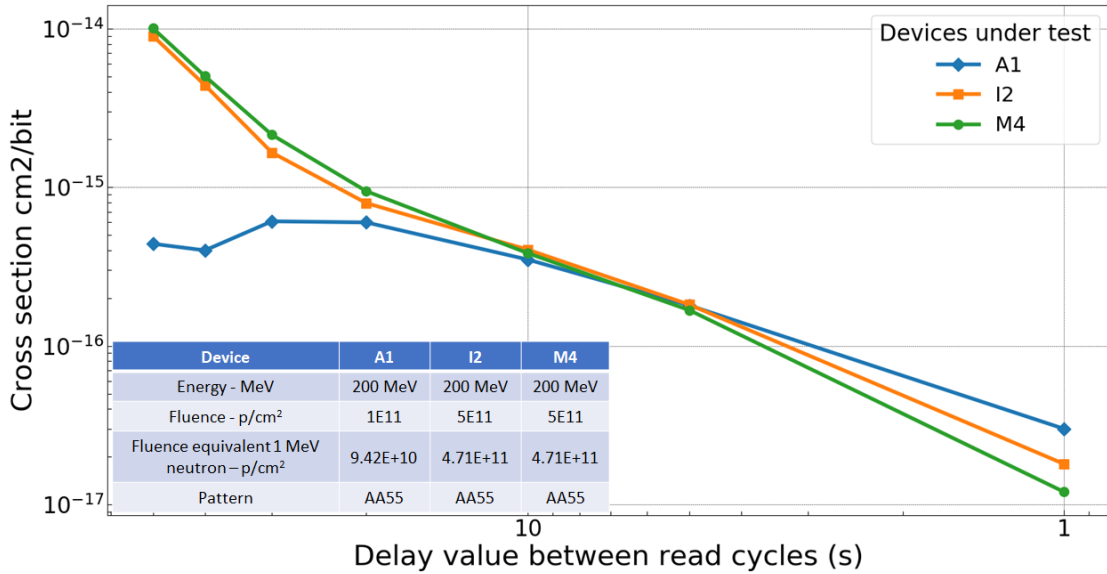
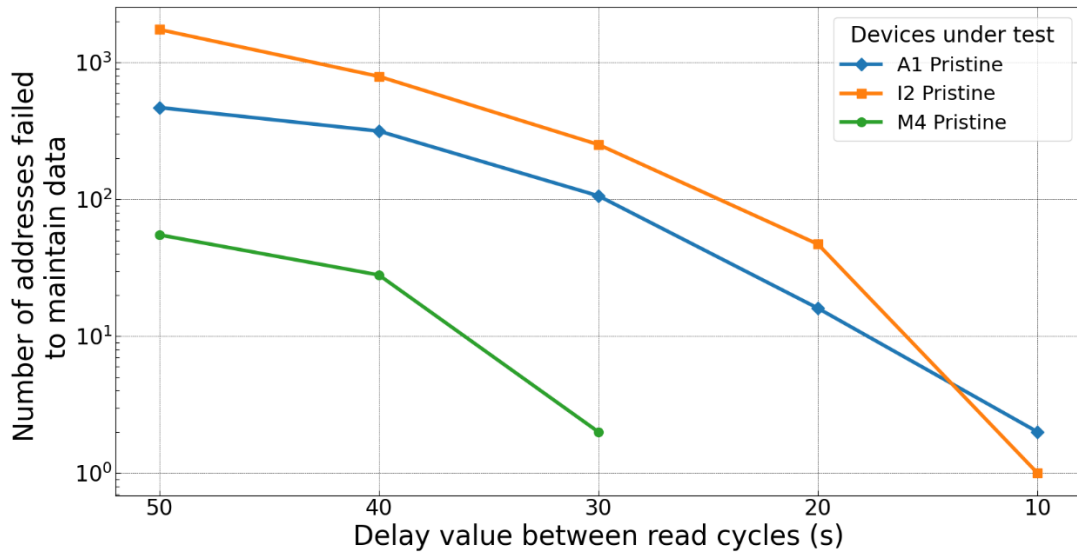


Figure 101: Retention time measurement between three new references under 200 MeV proton irradiation.

Figure 101 shows the different sensitivity for each new reference. While ISSI and Micron device remained under the same fluence ( $5 \times 10^{11}$  p/cm<sup>2</sup>) and energy (200 MeV), they show a different response to the degradation.



*Figure 102: Retention time comparison between Alliance (A1), ISSI (I2) and Micron (M4) pristine device. It shows clearly that Micron device has better retention time characteristic compare to others two.*

Before irradiation, the Micron device showed a much better retention time distribution on its cells as seen in Figure 102. However, after being irradiated at the same amount of degradation, both Micron and ISSI showed the same level of retention degradation which is surprising. This can be only explained by the fact that the saturation level of Micron and ISSI devices is reached at a fluence of  $5 \times 10^{11}$  p/cm<sup>2</sup>. For the Alliance device at a lower fluence, the degradation is much lower at a high retention time, however at a lower retention time, it also has the same cross section as Micron and ISSI.

No addresses with a retention time lower than the 64ms refresh limit (room temperature) are detected, which means no upset bit or stuck bits are supposed to be observed.

#### **3.4.1.2. Annealing at room and high temperature.**

After Irradiation, all devices are seen to recover under the room temperature. Figure 103 shows the number of failed addresses per delay level of the Hyundai H3 device after periods of time under the room condition. We notice that few addresses are recorded at a retention time less than 100ms in Figure 103. However, upon close examination, these results are due to the length of a read cycle, indeed there are no addresses that have a retention time lower than 100ms.



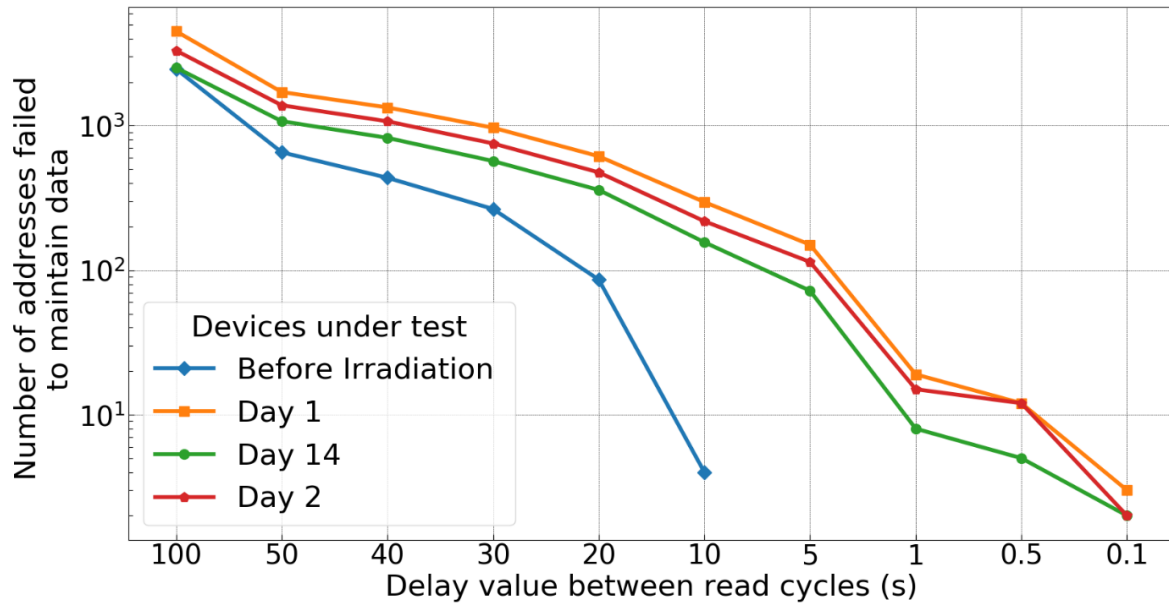


Figure 103: Annealing of retention time at room condition of device H3.

However, the recovery seems to slow down or be completely saturated, since, 2 weeks later it does not show much improvement.

Figure 104 is the annealing result of the Hyundai H07 device at high temperature (180°C for less than 30 minutes). By using high temperature annealing, the devices were able to recover to the closer state to the unirradiated device. The same behaviors were also observed on H14 with the same annealing method.

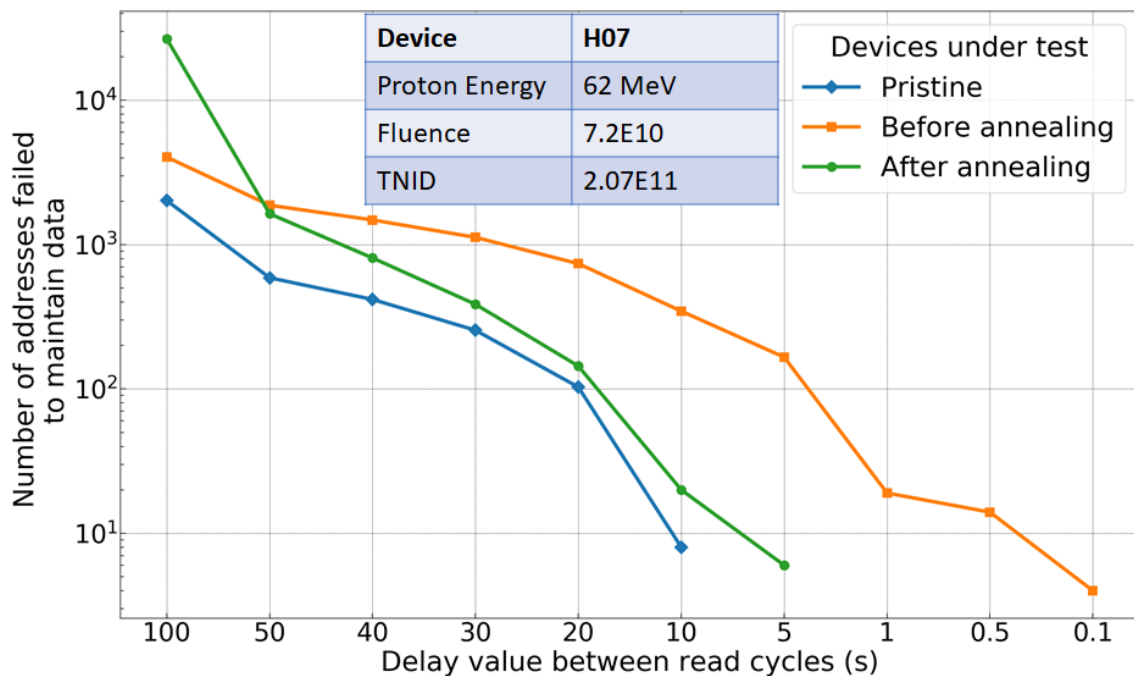


Figure 104: Comparison of retention time distribution of device H07 with different annealing conditions.

### 3.4.1.3. Heavy Ion degradation.

Like proton irradiation, heavy ions also induce a degradation of the retention time. Figure 105 shows the comparison before (blue curve) and after (orange curve) irradiation among different delays between read cycles for 1M addresses of memory a few weeks after irradiation campaign. The number of failed addresses increased for each level of delay. Data missing at a 40s delay of blue curve is due to the different delay times set up between two tests.

In particular, while the new device has the lowest retention of more than 5 seconds, the irradiated device has a various number of addresses with a retention time of less than 1 second. Measurements taken after irradiation show that no address has a retention time of lower than 64ms.

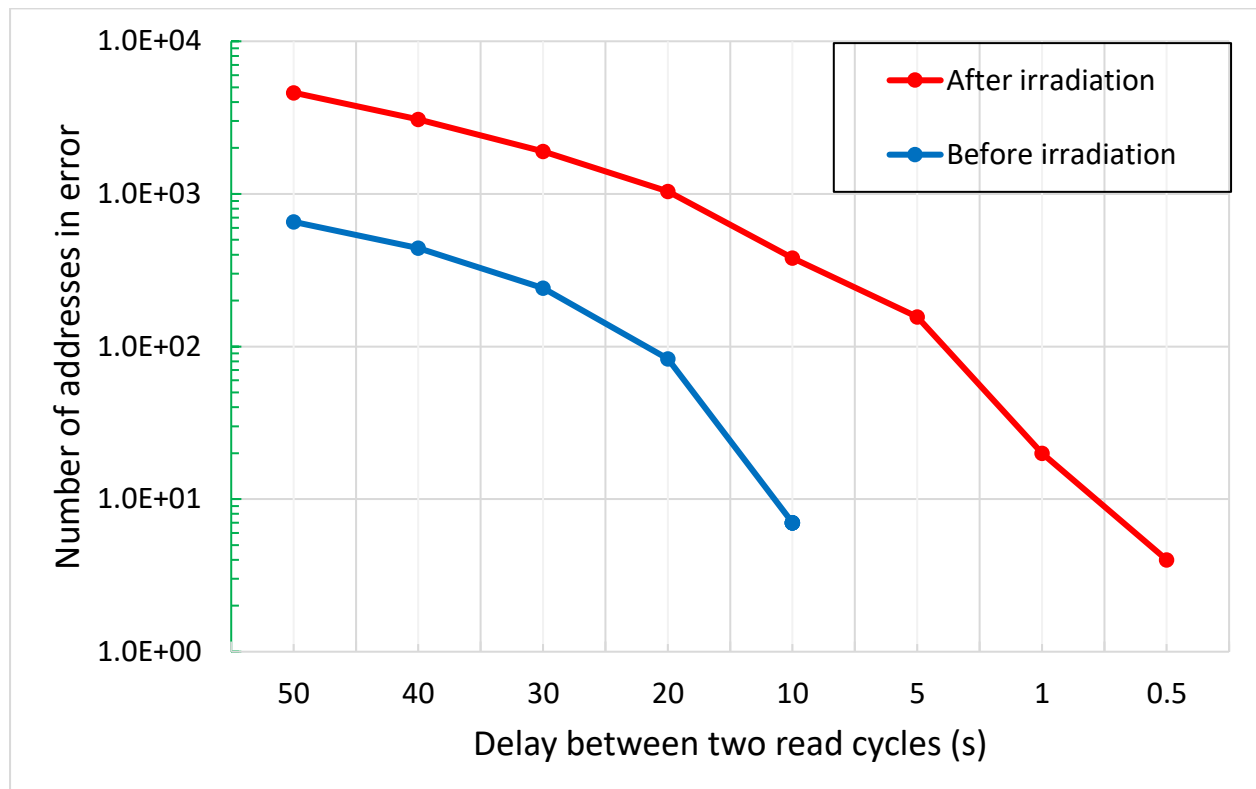


Figure 105: Comparison of number of address failed to maintain the data for each delay time of 2 read cycles before (blue) and after (red) irradiation for device H01.

### 3.4.2. Functional test of DRAM device

In addition to the retention time measurement, normal functional tests are used to assess the sensitivity of device under test with single even effects. In this section, single event effects under proton and heavy ions irradiation will be discussed. Moreover, data from current monitoring unit are also studied in detail.

#### 3.4.2.1. Proton Irradiation

- SEFI, Stuck bit and SEU in general

During irradiation, the Alliance devices are error-free, including SEU, Stuck bits and SEFI. On another hand, there are different types of bursts that can be observed in Micron DUTs. These can be classified as follows:

- The burst with a similar read pattern among addresses.
- The burst with a totally random read pattern among addresses.
- The burst that repeats a second time. Same behavior is seen in ISSI; however, they are not in two consecutive read cycle.
- The burst with a total number of errors in a single burst is the multiplier of 256 – row error
- The burst with a total number of errors in a single burst is not the multiplier of 256

It's difficult to find the exact location for each type of burst error, so for ease of consideration, these are recognized as SEFI.

Microns are the only sensitive reference to stuck bit in this test campaign. In the following, a few DUTs have been selected to further investigate the phenomenon.

The first DUT is M4 with 2 times irradiation. The first run with a fluence of  $10^{11}$  p/cm<sup>2</sup> at 200 MeV, M4 showed 2 bursts error and 19 hard error/stuck bits (showed in Figure 106).

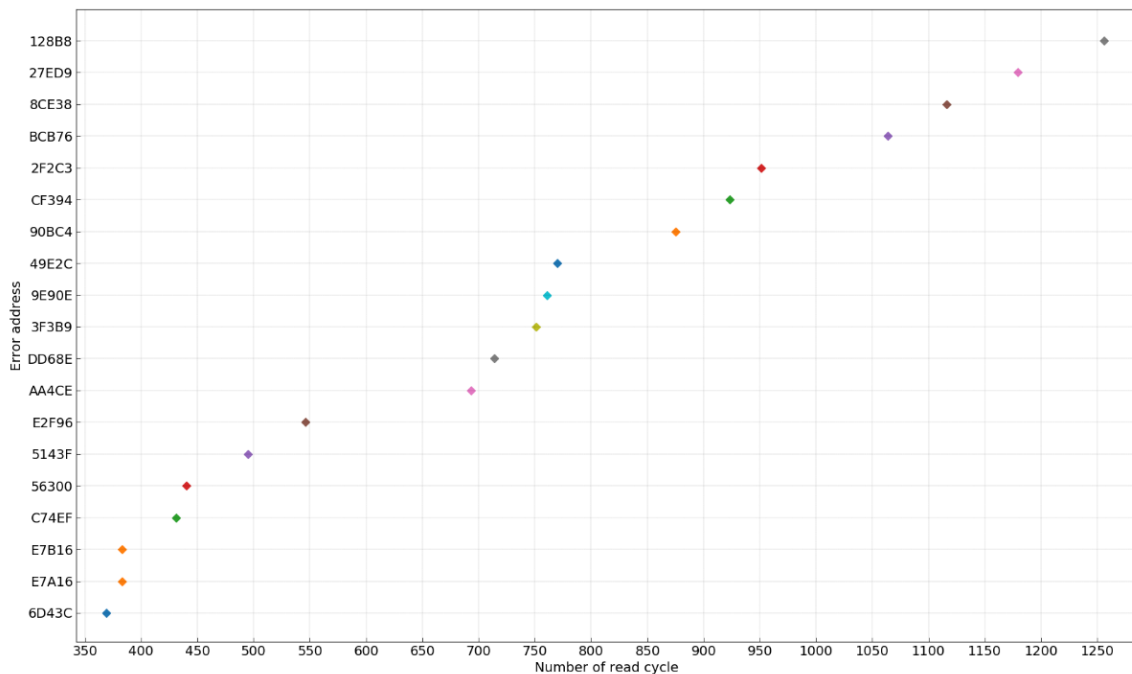


Figure 106: Stuck bit of M4 DUT as the evolution of read cycle for run 5<sup>th</sup>.

Taking a closer look at the read cycle 383<sup>th</sup>, we observed 2 errors at the same time. They are in the same column and on 2 consecutive rows.

Table 17: Error at read cycle 383<sup>th</sup> or M4 DUT

Data read	Data expected	Address	Error type	Read cycle
AA8A	AAAA	E7A16	3	383
2AAA	AAAA	E7B16	3	383

All the recorded errors are classified as type 3 (as mentioned in 2.4.2.3), which means hard errors/stuck bits. On the other hand, data cannot be re-written to the faulty addresses.

Let's now move on to the run number 9, on the same M4 with a cumulative fluence of  $4.10^{11}$  at 200 MeV. As expected, the number of burst and stuck bits has increased significantly with 10 burst errors and 39 new addresses (Figure 107). Of the 19 stuck bits in run 5, only 11 ones were detected in the first cycle and filtered out. It is interesting to note that between the couple addresses mentioned in Table 17, only E7A16 remains stuck in the second run.

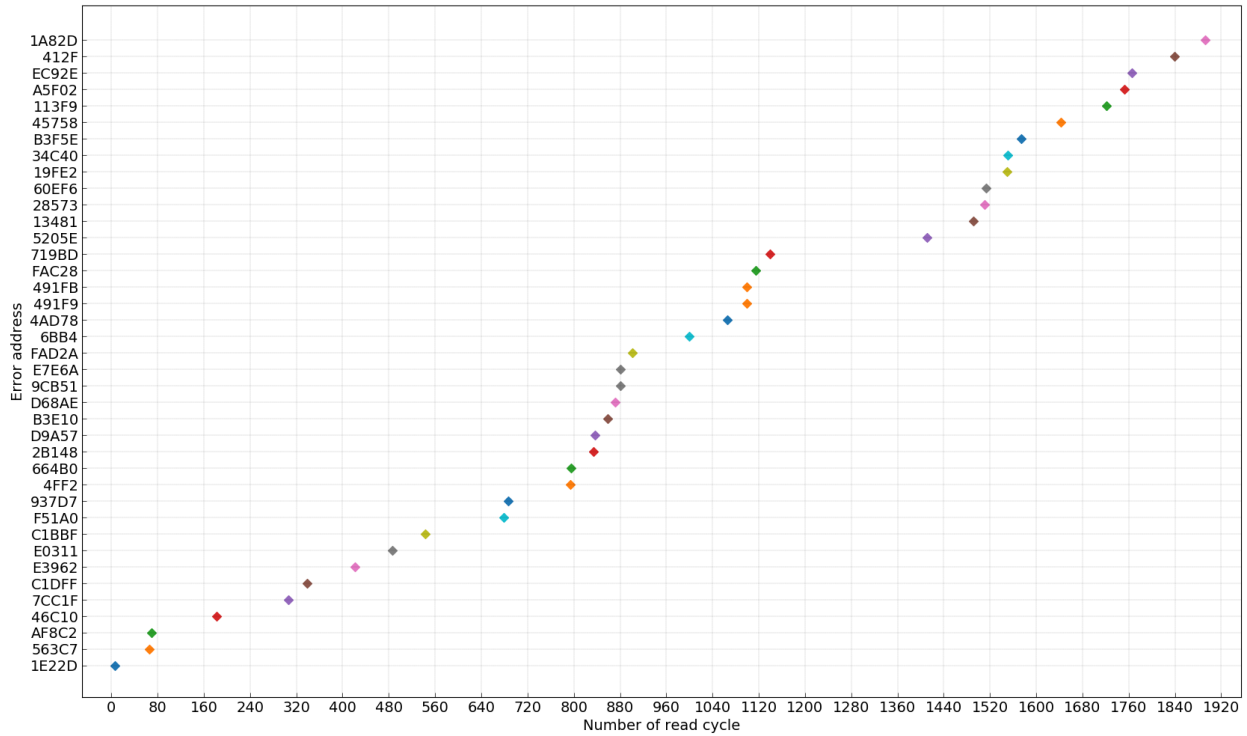


Figure 107: Stuck bit of M4 DUT as the evolution of read cycle for run 9<sup>th</sup>.

The same characteristic among the distribution of the stuck bits is the homogeneous spreading over time.

The M5 and M6 devices are tested at different levels of energy. Table 18 summarizes the errors at each level. At first glance, a lower energy seems to have a greater impact on the number of stuck bits. However, due to low number of errors recorded it's difficult to be certain.

Table 18: Different between DUT and corresponding error

DUT	Energy (MeV)	Fluence (p/cm2)	Burst	Stuck bit	Stuck bit Cross section (cm <sup>2</sup> /device)
<b>M5</b>	121.45	$2.10^{11}$	5	17	$8.5 \times 10^{-11}$
<b>M6</b>	60.8	$2.10^{11}$	3	26	$1.3 \times 10^{-11}$
<b>M4 (run 1)</b>	200	$1.10^{11}$	2	19	$1.9 \times 10^{-10}$

After irradiation with the M6 device, the retention time measurement was quickly performed to identify the lowest retention time in the device.

Figure 108 shows the stuck bit evolution as the read cycle of DUT M6 with the retention time of few addresses after irradiation are listed in Table 19. In order to save beam time, the retention time was measured in the first M addresses of memory at delay values of 5s, 2s, and 1s.

Among those stuck addresses, the retention time measurement shows clearly the degradation level. The lowest retention time is of address 89E2 at 401ms. And the addresses without a red mark mean that their retention time is higher than 5 seconds. There are no addresses with a retention time of less than 64ms refresh interval.

There is a trend, with a few exceptions: the addresses stuck at the beginning of the test show a longer retention time than the addresses stuck at the end of the test run. This can be explained by the fact that the cells have more time to recover after irradiation.

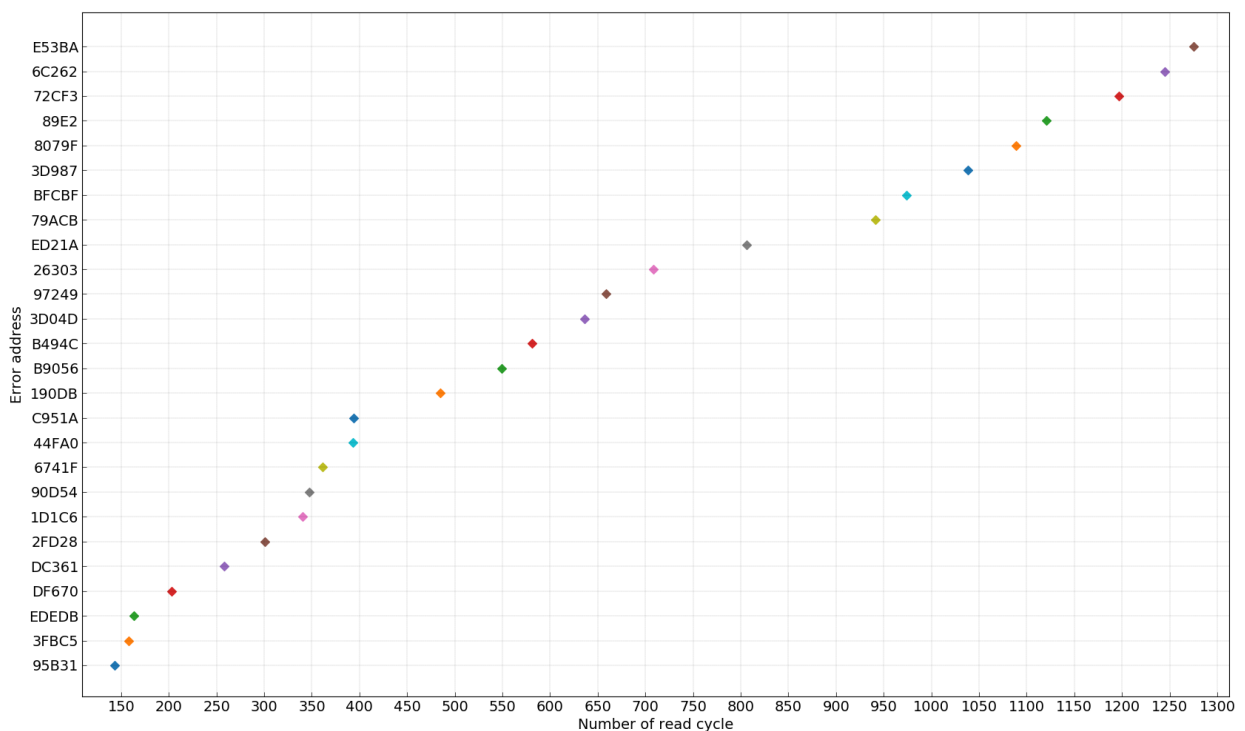


Figure 108: M6 with stuck bit evolution as read cycle and the retention time of addresses (run 17<sup>th</sup>).

It's worth mentioning that all stuck bit addresses in the test run have a retention time of more than 50s in non-irradiated devices.

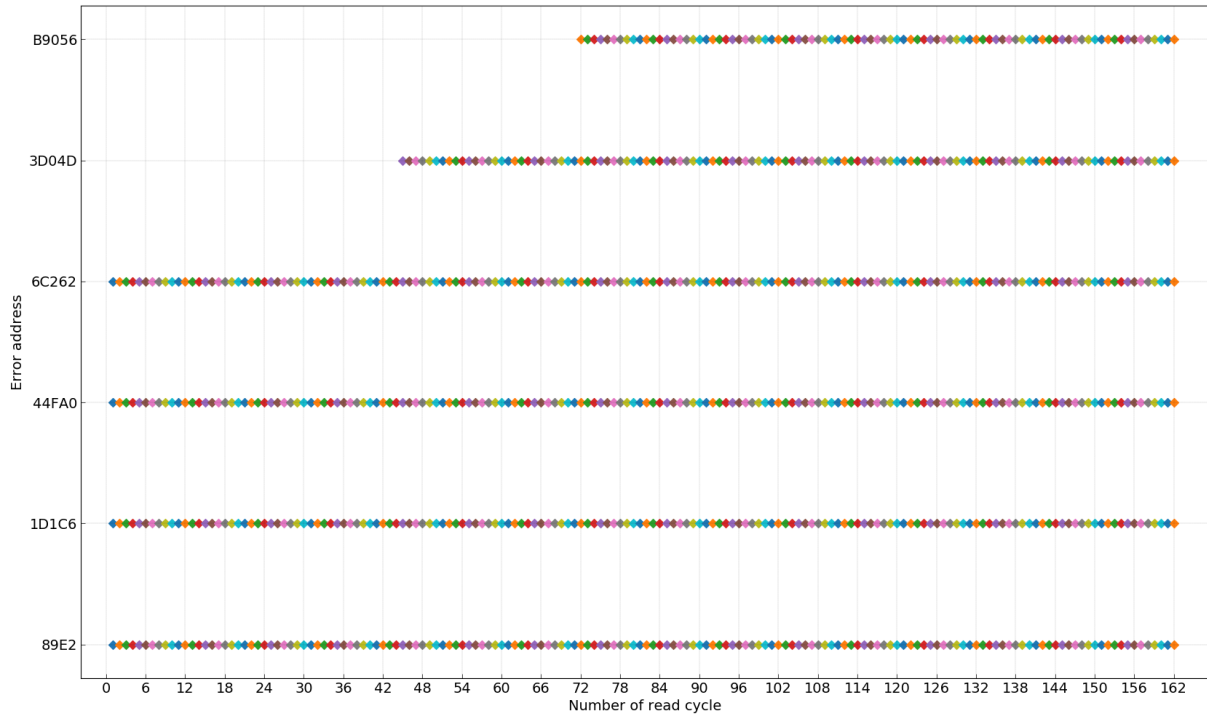


Figure 109: Error evolution corresponding to read cycle of DUT M6 post irradiation (run 18<sup>th</sup>).

Figure 109 shows the functional run right after irradiation. Unsurprisingly, 3 cells with the lowest retention time (83FCD, 44FA0, 89E2) are stuck in this test run, 2 addresses showing up after a while of running can be considered as weakened cells, and their retention time are greater than the refresh interval.

Table 19: Retention time range of addresses measures after irradiation of device M6.

Address	Retention time range	Address	Retention time range	Address	Retention time range
<b>95B31</b>	2000 – 5000	<b>44FA0</b>	<1000	<b>79ACB</b>	1000 – 2000
<b>3FBC5</b>	2000 – 5000	<b>190DB</b>	2000 – 5000	<b>BFCBF</b>	1000 – 2000
<b>DC361</b>	2000 – 5000	<b>B9056</b>	2000 – 5000	<b>89E2</b>	401
<b>2FD28</b>	2000 – 5000	<b>B494C</b>	1000 – 2000	<b>6C262</b>	500 – 1000
<b>1D1C6</b>	2000 – 5000	<b>3D04D</b>	1000 – 2000	<b>E53BA</b>	2000 – 5000

### 3.4.2.2. Heavy Ions Irradiation

- SEFI, Stuck bit and SEU in general

Several SEFIs are detected for the Hyundai device under heavy ion irradiation, however, the number of SEU constitutes the majority of observed errors (Table 20). Figure 110 shows the cross section of SEUs for heavy ion irradiation at GANIL.

Table 20: Summary of error on Heavy ion irradiation campaign.

Run	Devices	Mean LET 245-255um OMERE (MeV.cm <sup>2</sup> /m g)	Fluence	Total SEU without weakened cells events	SEU cross section per bit	SEFI number	Weaken ed cells address
1	H1	34.1	8.69×10 <sup>4</sup>	1736	1.99×10 <sup>-8</sup>	1 Hard SEFI	0
2	H1	34.1	5.16×10 <sup>5</sup>	16942	3.28×10 <sup>-8</sup>	1	2
3	H1	48.62	1.00×10 <sup>6</sup>	78171	7.82×10 <sup>-8</sup>	1	9
4	<b>Test run</b>						
5	H1	32.97	6.56×10 <sup>5</sup>	64973	9.90×10 <sup>-8</sup>	1	0
6	H1	68.88	5.14×10 <sup>5</sup>	71819	1.40×10 <sup>-7</sup>	1	43
7	H23	68.88	5.04×10 <sup>5</sup>	68857	1.37×10 <sup>-7</sup>	0	2
8	H23	68.88	5.04×10 <sup>5</sup>	66286	1.31×10 <sup>-7</sup>	1	25

The result shows no difference in the cross section of the AA/55 (run 7<sup>th</sup>) pattern compared to that of the 55/AA (run 8<sup>th</sup>) in the SEUs number.

As the main goal of this experiment campaign was to confirm the behavior of the weakened cells, it can be seen that the LET is relatively high and that the devices experience the saturation level in all the runs.

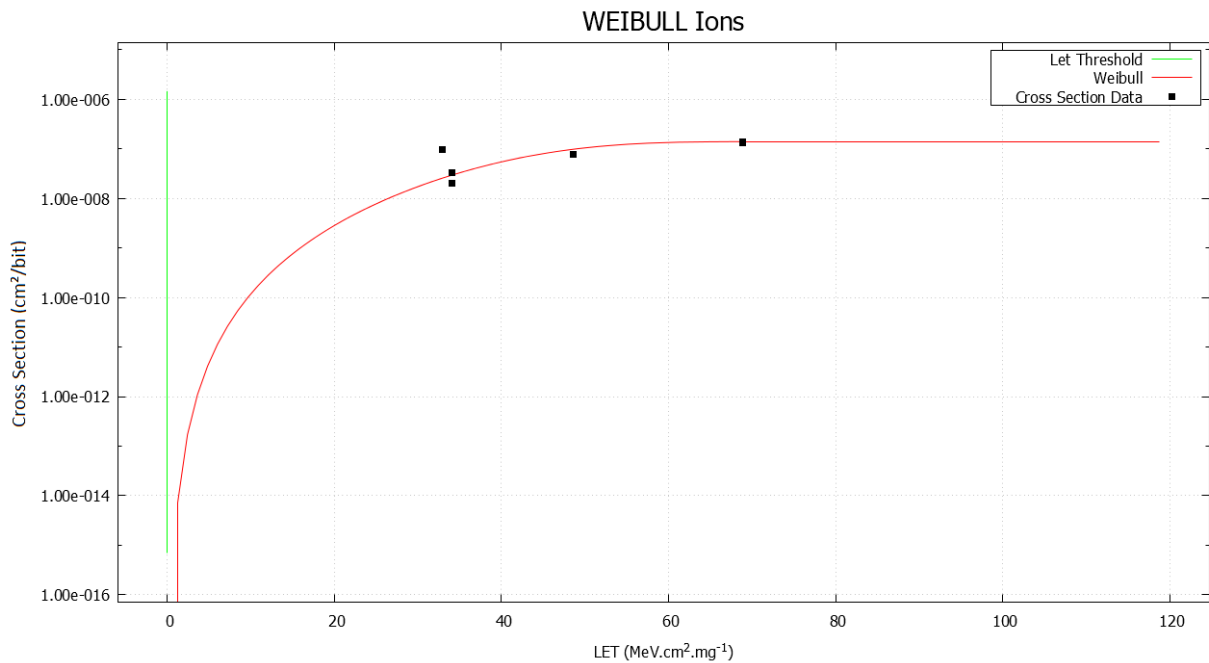


Figure 110: SEU cross section per bit of device H1 and H23 for heavy ion experiment without taking account the error from weakened cells (from OMERE).

The Weibull function is widely used to adjust cross-section data of the direct ionization SEE. It provides the flexibility to fit the LET threshold as well as the LET saturation values. The form of Weibull function is written in equation (3.1).

$$F(x) = A \left( 1 - e^{-\left(\frac{x-x_0}{w}\right)^s} \right) \quad (3.1)$$

where:

$x$  is the effective LET in MeV.cm<sup>2</sup>/mg;

$F(x)$  is the SEE cross-section in cm<sup>2</sup>/bit;

$A$  is the limiting or plateau cross-section cm<sup>2</sup>/bit;

$x_0$  is the onset parameter, such that  $F(x) = 0$  for  $x < x_0$  in MeV.cm<sup>2</sup>/mg;

$w$  is the width parameter in cm<sup>2</sup>;

$s$  is a dimensionless exponent.

The fitting parameters ( $A, x_0, w, s$ ) used in context of this thesis are extracted from OMERE software which is developed at TRAD and freely distributed [134]. Examination of specific data for each run will give us more details on the error's behavior.

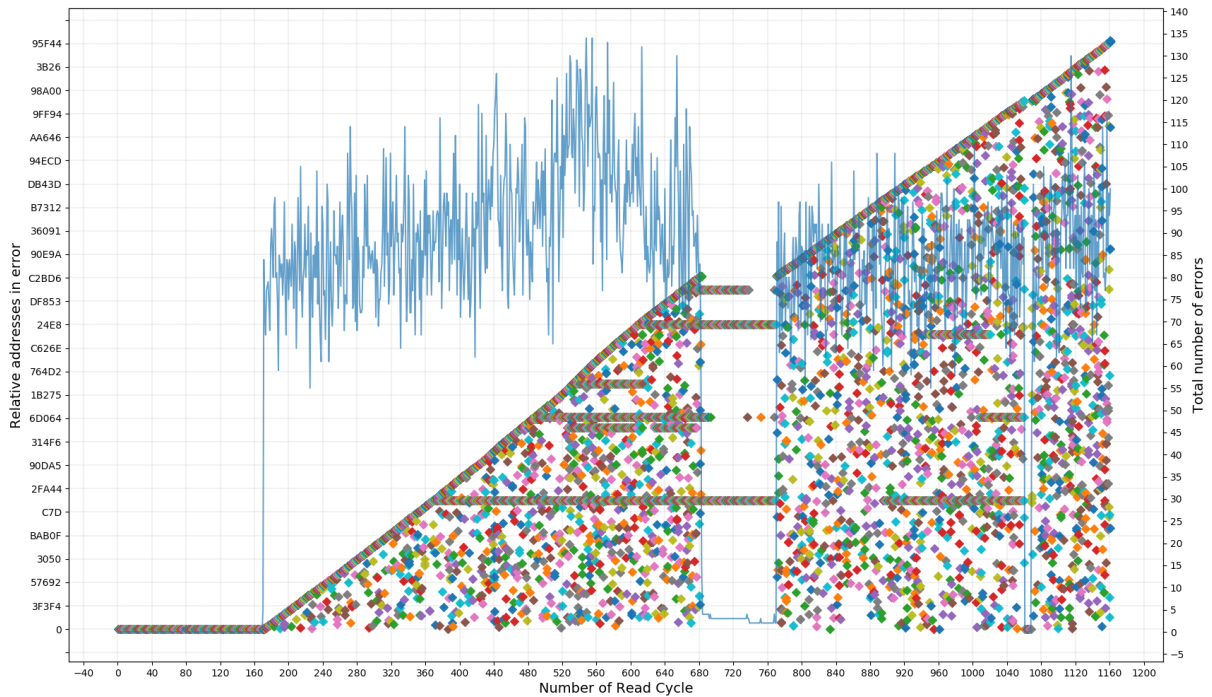


Figure 111: Number of errors per read cycle for device H1 - run 3<sup>rd</sup>, each point represents one single error detected. Due to large number of addresses, vertical axis only represents the relative address.

Figure 111 shows the erroneous addresses corresponding to the evolution of the read cycle during the test of the H1 device in the run number 3. The left vertical axis is a contracted list of addresses in errors sorted in chronological order, the horizontal is the read cycle evolution and the blue line indicates the total number of errors that occurred during a corresponding read cycle, with the scale on the right vertical axis. The single point indicates one error occurring during a specific read cycle. The figures show us that the beam starts at the 170<sup>th</sup> read cycle,



and a beam-off period between the 683<sup>th</sup> and 771<sup>th</sup> read cycles. Moreover, the SEFI at the 1061<sup>th</sup> read cycle is filtered out and indicated as 0 event marks.

The error increment line is proof that new errors happened in the new address during the irradiation period. The majority of the error are SEU's which are distributed randomly over 1M addresses of memory size. Few addresses showed repeated errors; however, the errors occur on the different bits of the word and do not appear instantaneously. Therefore, they are still considered as a single event upset. The total number of errors for each read cycle varies over time, however, the number of errors per read cycle follows the normal distribution and generally does not exceed the two times standard deviation  $2\sigma$ .

### 3.4.2.3. Studying of defective refresh mechanism

In order to identify weakened cells, the addresses in error were examined and only the addresses with the repeated errors are selected as candidates for weakened cells. Figure 112 shows the list of weakened cells detected from the 3<sup>rd</sup> run of device H1. On the vertical axis are the addresses and the horizontal axis shows the read cycle evolution, the yellow bar indicates the beam-off time. The result clearly shows that the number of weakened cells is much lower than the upset numbers.

The list of weakened cells detected are defined as high recurrence of error at a specific bit of one address. The filter allows us to see the specific address that is the candidate of weakened cells for our study. Figure 112 shows the list of weakened cells detected from run number 3 of device H1 (total error at Figure 111).

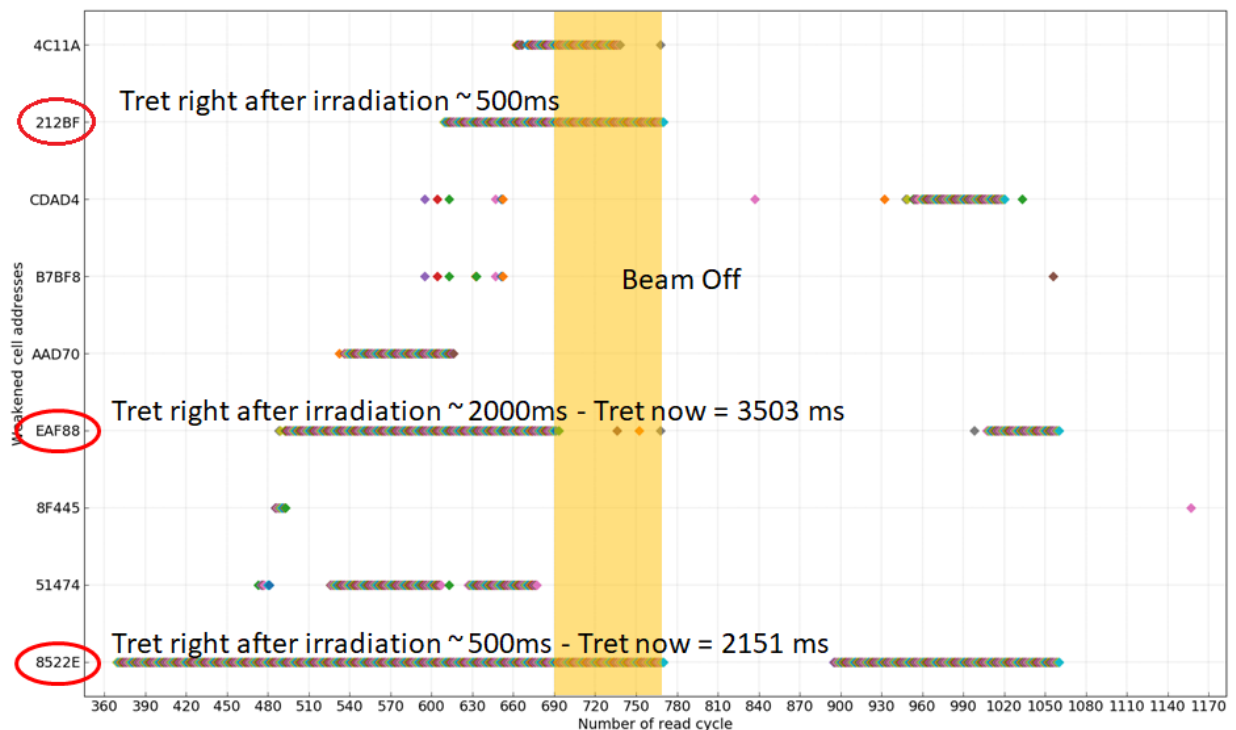
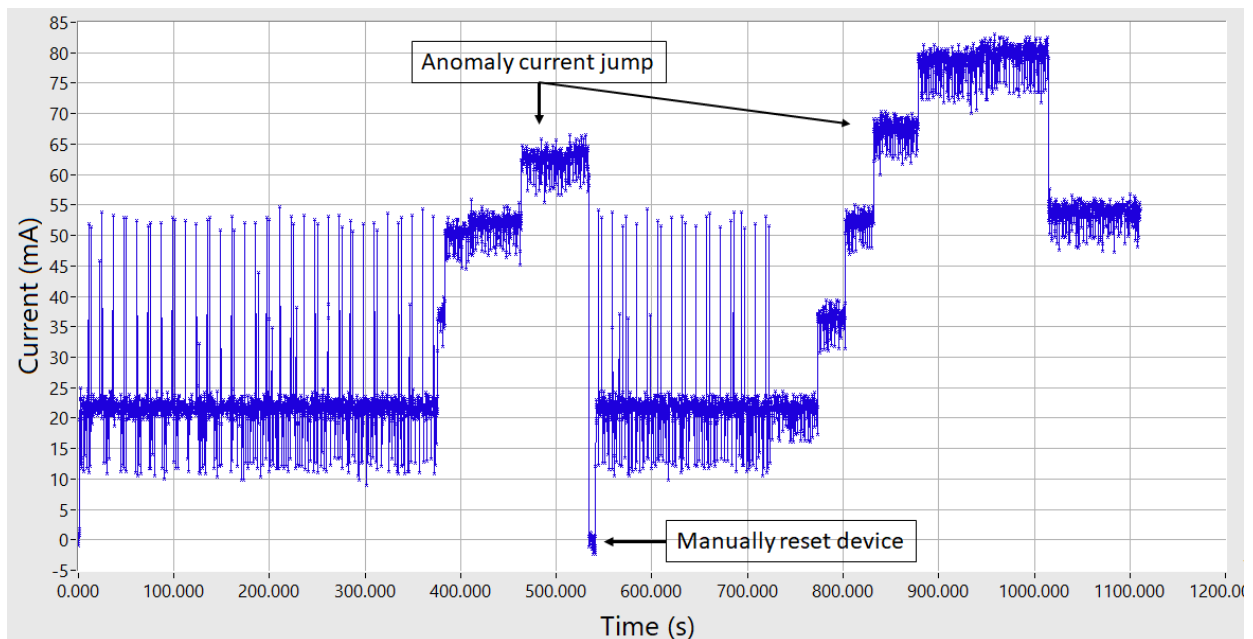


Figure 112: Weakened cell candidates on device H1 - run 3<sup>th</sup>. Yellow part indicate beam off time.

Right after each functional run, the retention time measurements were performed to measure the retention time of certain addresses that have a low retention time. The limitation of on-site retention time measurement is that it usually takes a long time and makes the test bench unavailable for the precious beam time. Therefore, the retention time thresholds were set at a low level to detect a small number of addresses that fail to hold the data in a short period of time. In fact, not all the weakened cells detected during a functional test have a retention time low enough to be measured. In case of run number 3 of device H1, two highlighted cases show the retention times around 500ms (8522E) and 2000ms (EAF88) just after irradiation; 2151ms (8522E) and 3503ms (EAF88) a few weeks after irradiation.

These results lead to two possibilities. First, the damaged cells were annealed rapidly at room temperature, which proves that the retention time right after irradiation exceeds the 64ms refresh threshold. Indeed, the increase in retention time after few weeks proves that the defective memory cells recovered at room temperature at higher retention time. Secondly, the refresh commands issued every 64ms by the control circuit are not performed on the devices. In order to investigate this hypothesis further, a current monitoring unit was installed to log the current consumption of the devices. Figure 113 shows the current consumption of the tested device - H1. The horizontal axis is the time evolution in seconds and the vertical axis represents the current in mA unit. The few increases in the current consumption from 373 to 534 seconds of the run time and corresponding to read cycle 388<sup>th</sup> can be clearly seen.



*Figure 113: Current monitoring from run number 3 of device H1 over time with jump in current consumption as indicated.*

Zooming in on the graph, it can be seen that the spike of about 55mA every 64ms is the refresh command issued by SDRAM controller. The square wave of current of around 23mA and lasts about 0.87s is the time needed for memory to read 1Mb of data. There is a short break between two continuous read cycles which last roughly 0.083s. Figure 114 shows the zoom of the current consumption at the 387<sup>th</sup> read cycle when the refresh spike disappears, or in other words, the refresh command was not performed on the device. On the next read cycle, the

current consumption has jumped to 50mA and then to 60mA while the device is still running. The brief off-current at 537 seconds is when the device must be restarted manually due to SEFI.

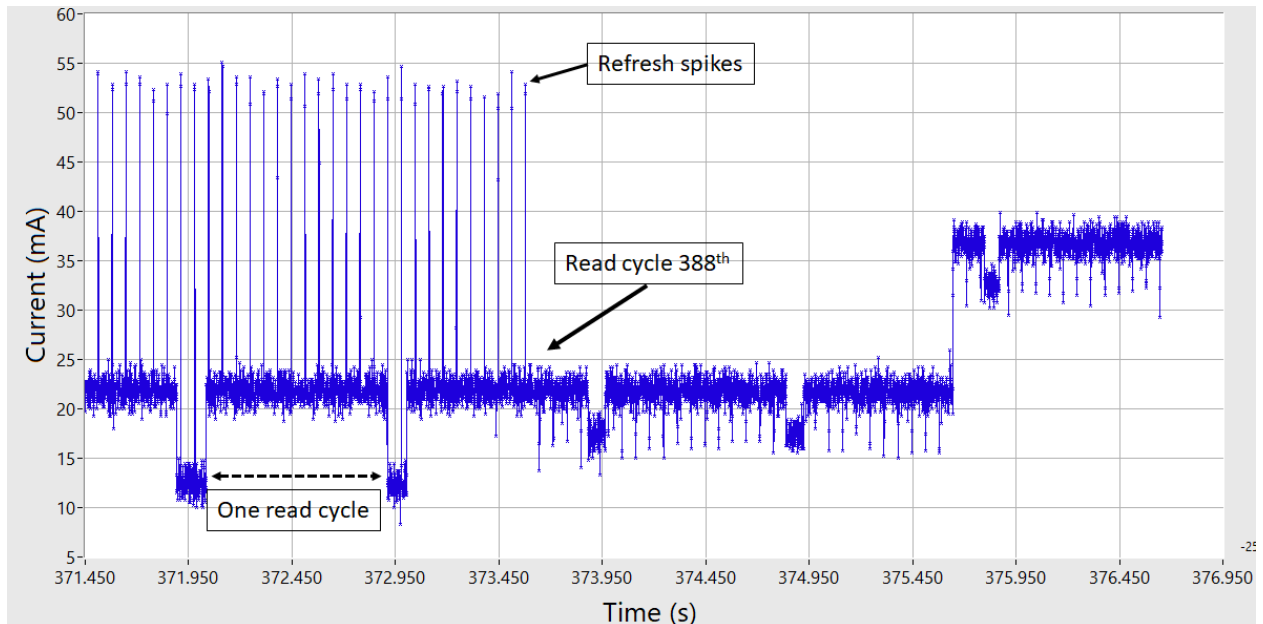


Figure 114: Zoom in of current consumption at read cycle 387<sup>th</sup>. At read cycle 388<sup>th</sup> the refresh spike disappears which coincides with the jump in the number of weakened cells.

Therefore, when the refresh does not work, the device does not have sufficient mechanism to maintain the data integrity for the 64ms requirement. However, in modern DRAMs, most cells are capable of maintaining data longer than this period and even up to a few seconds later. Thanks to this property, the Read and Write operation can be the main mechanism to “refresh” the data for the device. The only problem is that in this test case, the DRAM needs about 1 second to repeat the read-write action on 1Mb of data. Therefore, if the refresh does not work, the cells that can retain data for more than 1 second will probably not show the error, while the cell with a shorter retention time will be spotted. This finding is an important process to help us explain the result of retention time mentioned above.

However, it should be noted that, the first weakened cell showed up at read cycle 369<sup>th</sup> and the number of errors did not increase dramatically at read cycle 387<sup>th</sup>. This can be explained by assuming that the cell population is not heavily damaged as to be less than 1 second retention time. To clarify this point, we are continuing to investigate further on the next run of the device H1. Figure 115 shows the list of weakened cells from run number 6 of device H1.

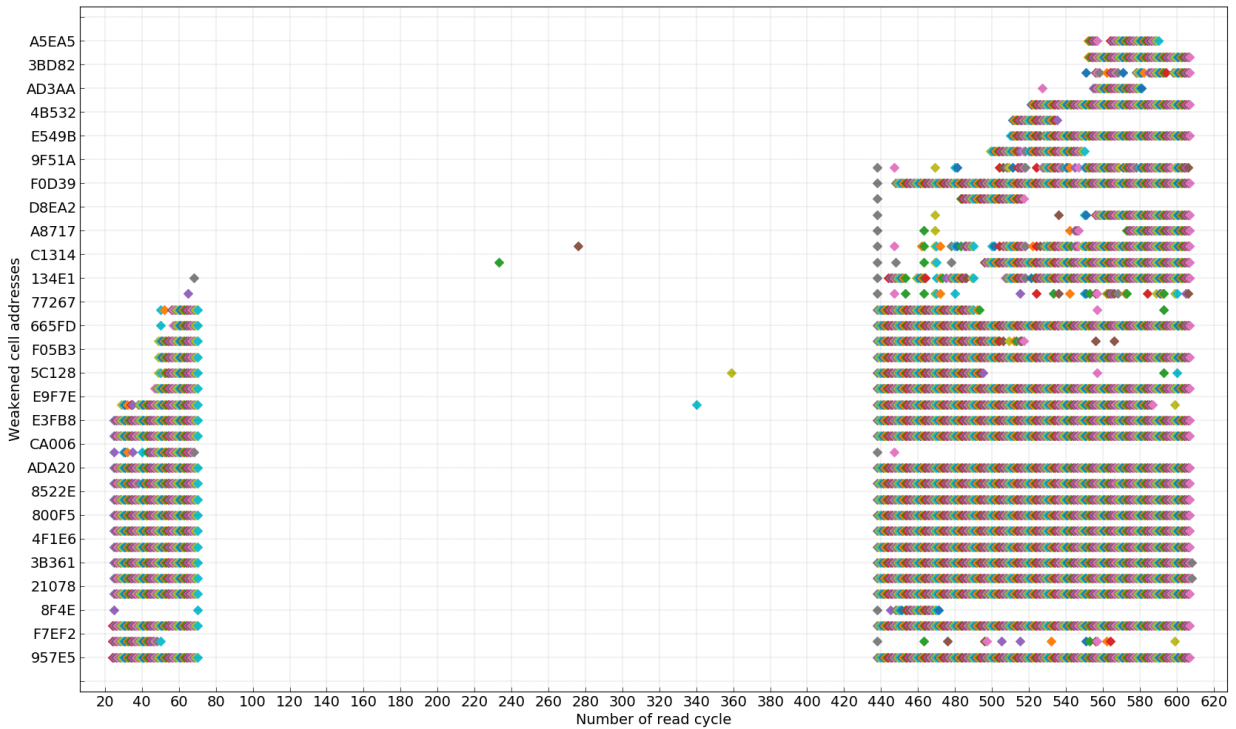
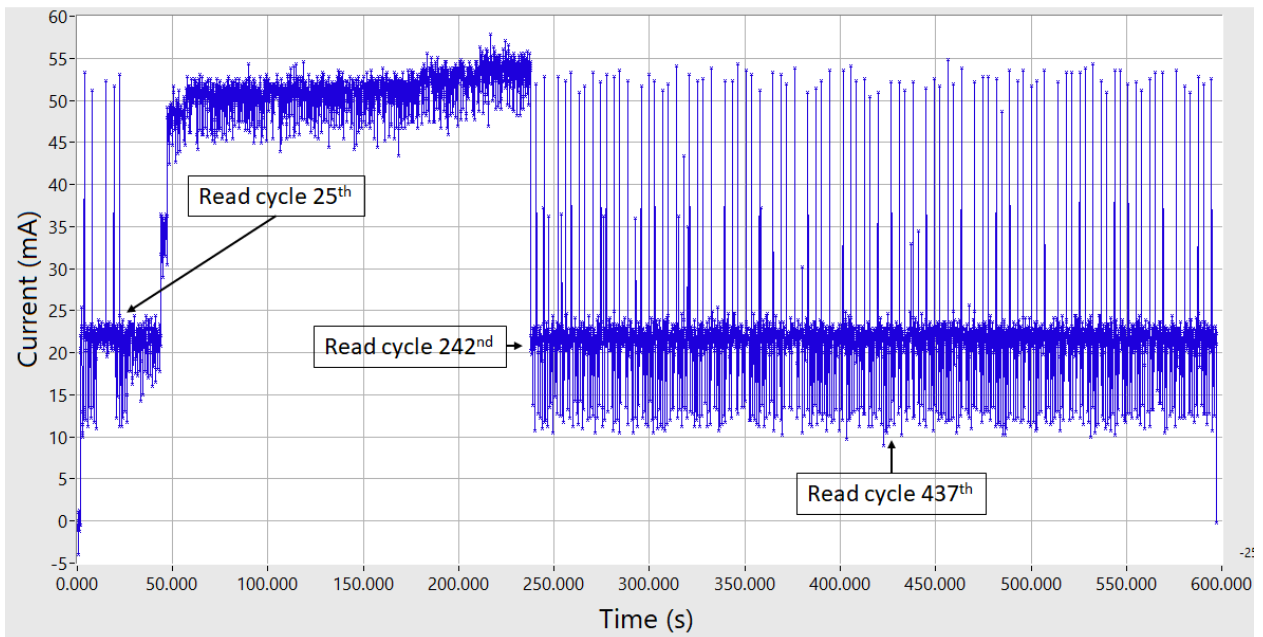


Figure 115: Weakened cell detected on run 6<sup>th</sup> of device H1 with two batches of error occur simultaneously: first batch from 25-71 read cycle ended with a SEFI, second batch from read cycle 438<sup>th</sup> right after the SEFI at read cycle 437. These are considered as weakened cells because it fits out criteria.

For run number 6, we saw an increase in the weakened cell simultaneously at read cycle 24<sup>th</sup>. Coincidentally, the current monitoring result (Figure 116) shows that the refresh commands stopped at read cycle 25<sup>th</sup>. Then, the high current anomaly jump event appears between 43 and 237 seconds.



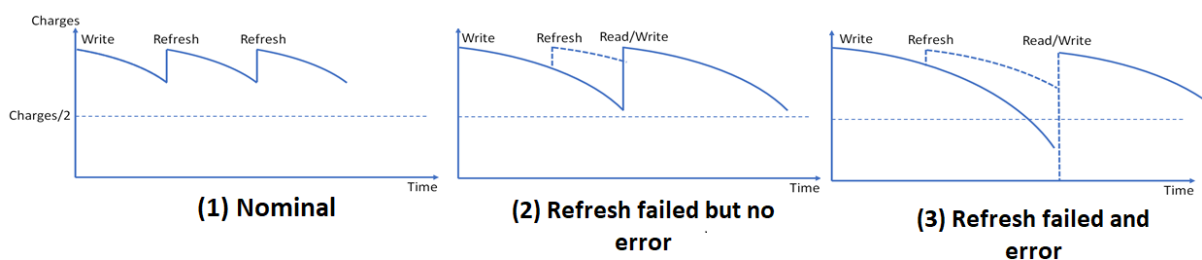
*Figure 116: Current consumption monitoring in device H1 run number 6. The refresh spike again disappeared from read cycle 25<sup>th</sup> and the jump in current consumption followed after that.*

The first batch of weakened cells from read cycle 25<sup>th</sup>-71<sup>st</sup> ended with a SEFI, and the device experienced a long period of high current. The second batch of weakened cell errors appeared from read cycle 438<sup>th</sup> right after the SEFI at read cycle 437<sup>th</sup>. This SEFI may be due to a power cycle on starting the beam. Current monitoring did not show any significant change in the current at a specific read cycle but a few small increases in current between the read cycles at a much lower current level (approximately 35mA).

Note that the faulty refresh behavior we observed through current monitoring is not exclusive to the H1 device but also occurred on the device H23. However, not all the devices show the increase in weakened cells or upset rate when the refreshes are not issued. This evidence, which has been gathered from previous discussions, suggests that the refresh malfunction only is not sufficient to induce weakened cells but that the cell retention time must also be less than the read duration of the device.

In order to explain what happened, let's take a look at 3 working cases in Figure 117:

- In the first case – nominal, the charges inside capacitor gradually depleted, however, due to refresh commands, it's restored above faulty readout limit (half of capacitance) therefore no error will occur.
- In second case – refresh mechanism failed; however, no error is observed. This is due to a fact that the device under test goes through frequently read/write command for data checking and these actions restore the charges stored inside DRAM cell the same as refresh. The period between read/write cycle depends on the memory size of the device. For our device with 1Mb of addresses, it takes roughly 1 second to read, hence if the cell's retention time is longer than this, no error will be occurred.
- Following the second case, we saw the error on the devices in the third case due to the fact that the cells that have retention time shorter than our read cycle period (about 1 second).



*Figure 117: Charges stored inside DRAM cells in three different cases.*

### 3.5. Temperature effects on retention time distribution

Therefore, the temperature dependence of the SEU rate on DRAM has been observed in the literature, few additional tests with the HYUNDAI HY57V651620 SDRAM were performed to verify the same behavior.

The tests with the thermal chamber were classified into two types: at fixed temperature and at ramping temperature within a range of temperature. The same retention time measurement and functional tests were carried out with two different temperature modes.

For the fixed temperature, the series of which 11°C steps have been carried out which is: -6°C; 5°C; 16°C; 27°C; 38°C; 49°C; 60°C; 71°C; 82°C. For each step, the thermal chamber was kept soaking for at least 60 seconds before any testing.

For the ramp temperature, the thermal chamber was set for the starting point at -6°C to 82°C then lowered to 27°C with an increase of 5 degrees per minute. The total duration of the temperature cycle is 17.6 minutes.

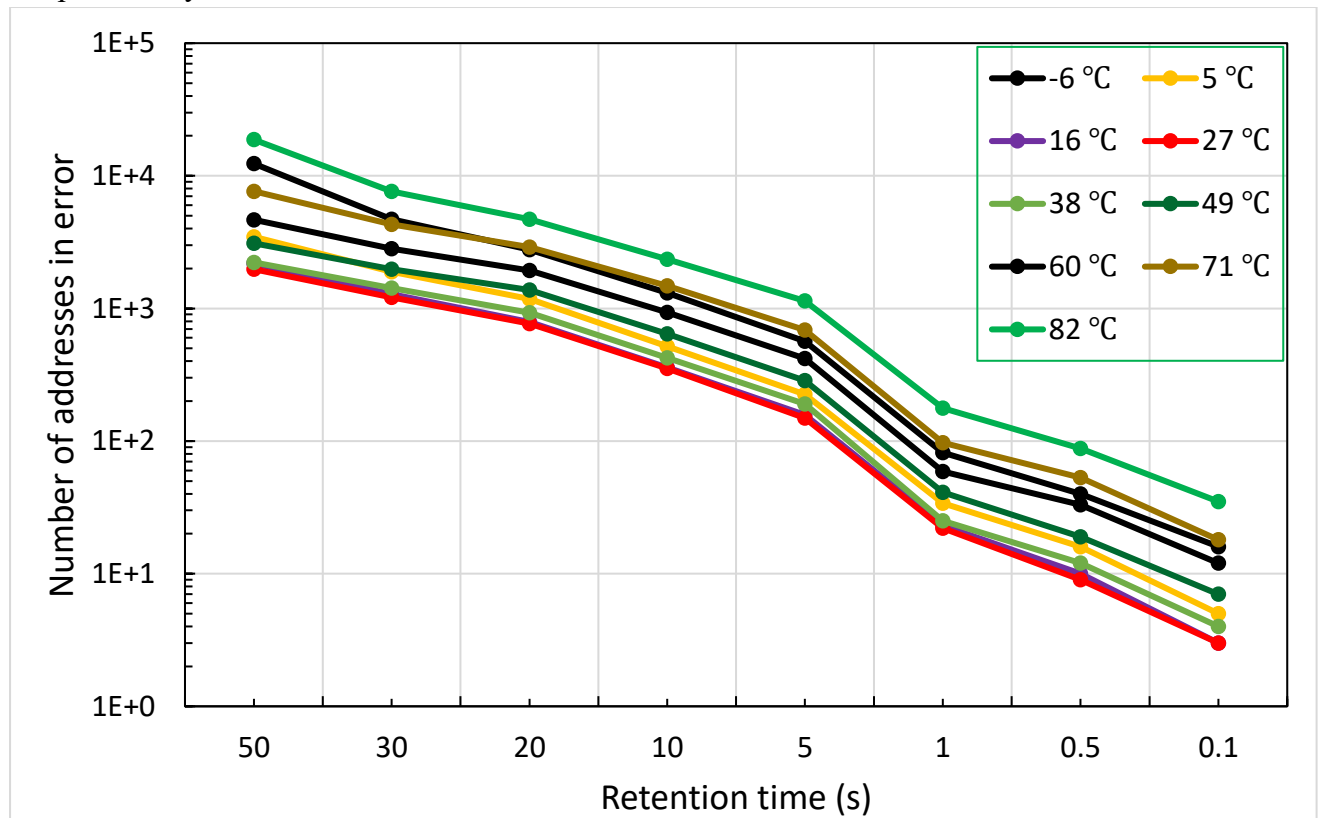


Figure 118: H3 devices cumulative errors with different delay time at different temperatures.

The distribution of the number of addresses in error for different delay time at different temperature is presented in Figure 118. In general, for each 11°C, the number of cumulative errors increases by approximately 1.5 times. In previous research, Adell showed by experiments that the leakage current will double every 11 degrees [135], while our experimental data shows the increase in the cumulative error as the result of an increase in leakage current at a certain delay time. However, it is not possible to directly conclude the quantitative relation between the two.

Figure 119 is another representation of the cumulative errors at different temperatures. Each curve shows the errors of a certain delay value at different temperatures. However, what is

interesting in this graph is that the smallest number of errors does not stay at the lowest temperature but around 27°C. This is due to the thermal chamber. During the temperature tests, the thermal sensor was attached directly on the surface of the devices, which does not correctly represent the real internal temperature of the devices. Therefore, there was a shift in the measurement, which leads to a shift in data for the temperature, but it still shows the behavior of the device at changing temperatures. After a comparison with different test results, the number of cumulative errors value at the 38°C is equivalent to the tests at room temperature, which is around 25°C.

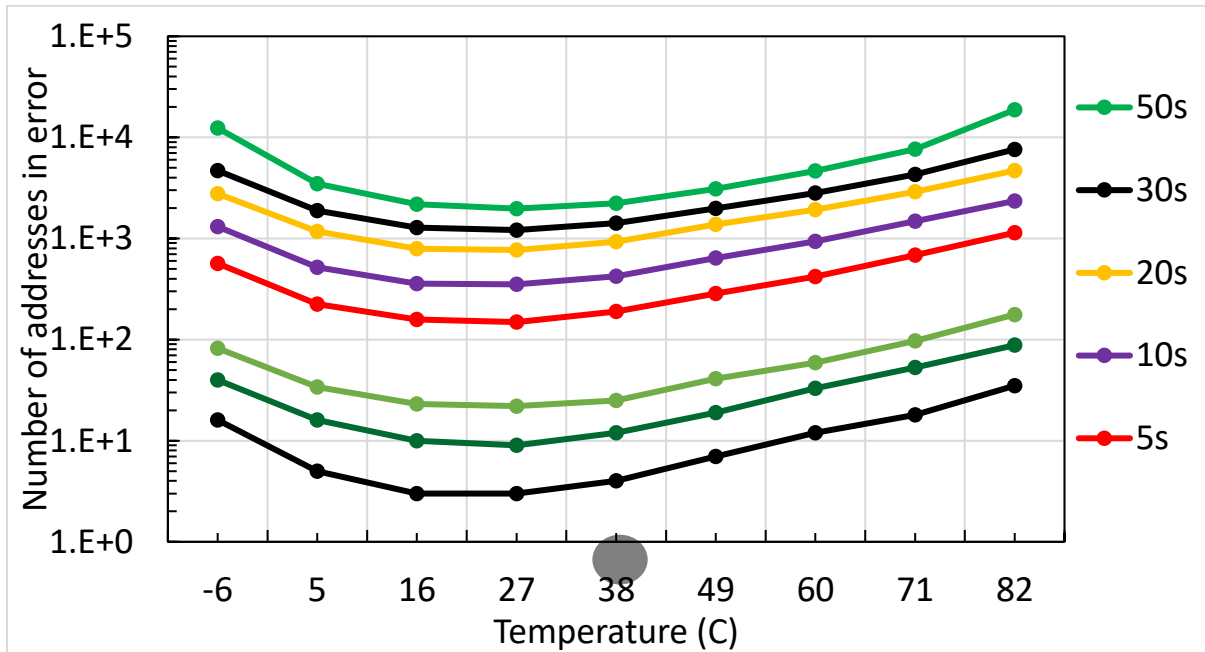


Figure 119: Another representation of H3 devices cumulative errors with different retention time at different temperatures.

### 3.6. Conclusion

From retention time measurement, we have seen that the cross-section for retention time degradation, especially for short period of time, are relatively small.

The retention time degradation is increasing with the increased proton fluence. Furthermore, different biased condition and patterns do not affect the degradation. This is explained by the evenly divided encoding scheme of DRAM device. By irradiating devices with different proton energies, we saw that lower proton energy induced higher retention time degradation due to higher LET deposited to the material.

The retention time measurement also allows us to measure the retention time of the defective cell to the nearest millisecond in terms of accuracy. The results are surprising because the observation shows no cell with a retention time below the 64ms refresh limit. This has raised the question of the combined effects that are taking place.

The important discovery made during the heavy ion irradiation campaign shows that the refresh mechanisms have been deactivated and followed by some high current jump events.

The deactivation of the refresh coupled with shorter retention time than the read time may indicate the appearance of errors during repeating read sequence.

Additional tests on the new references with smaller technological node show the low sensitivity of the SDRAM under proton to the phenomenon.

Through the experiments, it is almost certain that the weakened cells observed are the combined effect of defective cell and deactivation of the refresh command. Further suggestions regarding the variable retention time need to be studied on a large scale and over a long time in order to detect the phenomenon. The test bench has to be adapted to these new requirements.

In order to fully understand the physical mechanism underlying the defective cell, TCAD modeling is used and this is also the objective of the following chapter.



# **Chapter 4: 1D TCAD modeling of a defects cluster in PN junction of DRAM's storage node**

## 4.1. Introduction

The discussion from experimental data showed the combined mechanism might be the root cause of weakened cell behavior. These are refreshing faulty mechanism of the memory device and reduced retention time in defected cells under radiation. While refresh disabling in DRAM device are related to control logic and can be considered as one of SEFI side effect, defected cells under radiation need to be studied in details. Various studies about this subject mainly focus on the experimental aspect of the phenomenon but not the TCAD (Technology Computer-Assisted Design) modeling. Previous study done by Axel Rodriguez have shown that the cluster damage induced by single particle can increase leakage current and shorten the retention time of the memory cell [58].

In this chapter, we will use TCAD simulation to understand the underlying physical mechanisms of the defected cell under radiation. Moreover, it's necessary to identify any other mechanisms that can contribute to the phenomenon.

The first modeling is 1D model of PN junction of storage node of DRAM device. Then, the defect cluster is introduced to the model and then its effects are evaluated.

## 4.2. ECORCE software and physical models

ECORCE (in French: Etude du COmportement sous Radiation des Composants Electroniques, stands for Study of electronic devices behavior under irradiation) aims at modeling the behavior of the semiconductor-based electronic components and their response to radiation [136]. The software models single event transients and the total ionizing dose in semiconductor-based technology such as: Mosfet, capacitor, bipolar.

ECORCE is currently developed in the RADIAC [137] (RADIATION and Components) team at the IES (in French: Institut d'Electronique et des systèmes, stands for Institute of Electronics and Systems) of the University of Montpellier in France. Each section of the code was implemented separately in order to facilitate the creation of the modification of the physical laws. ECORCE is written in C++ and uses automatic derivation of nonlinear equations, SparseLib++ to solve linear equation systems, Qt5 for the graphical interface and Coin3D to define the geometry of the device graphically and plot the model results.

ECORCE is based on the finite element method which is used to discretize and solve the Drift-Diffusion Model (DDM) with Poisson's equation (allow to compute the electrostatic potential distribution) and the continuity equations (calculating the electrons and holes concentration).

This TCAD software integrates a dynamic meshing that automatically adapts to describe optimally the gradient of the different variables (potential, carrier density, etc.) for each calculation step in stationary or transient analysis mode. The dynamic meshing adds and removes nodes all along the modeling process to minimize the discretization errors and improve the calculation time. Therefore, the user does not have to take care of the meshing quality and refinement to perform the simulation. By only specifying the precision the user wishes to obtain, the mesh size is automatically modified according to the requirements (biases, irradiations, etc.).

As seen in the previous chapters, the radiation effects are divided into two categories such as the cumulative effects and the Single Event Effects (SEE). Cumulative effects are related to the ionizing rays (TID) and non-ionizing rays (Displacement Damage). The TID induces a charge trapping into the oxides, which leads to a degradation of the electronic properties of the electronic components such as a threshold voltage shift for the MOSFET transistors or the decrease in current gain for the Bipolar Junction Transistors. Single events are caused by a single highly energetic particle that deposits its energy all along of its trajectory into the silicon. The understanding of these mechanisms and the radiation-induced degradation remain nowadays a serious technological challenge. Therefore, the development of simulation software able to model the induced physical mechanisms is helpful to harden or develop mitigation methods.

In this section, fundamental equations of the semiconductor physics used in simulation software will be introduced as following:

- Drift-Diffusion equations, which calculate the transport of the charge carriers into the semiconductors using Poisson and holes and electrons transport equations.
- Trapping-Detrapping equations, which determine the charge trapping and charge detrapping into the oxides and at the surface of interfaces during irradiation using the MTD (Multiple Trapping-Detrapping) model.
- Heating equations, which define the temperature at any point of the mesh to understand the thermal behavior of semiconductor-based electronic component using the standards equation of thermal exchange.

These are differential equations. To solve them, the space domain is separated in small parts called elements. Then by applying linear approximation on each element, the equations are solved at each node of the mesh on the discretized domain. A mesh is composed of nodes, edge, and

faces as illustrated in Figure 120. Each mesh (of faces) can be rectangular or triangular. ECORCE use dynamic meshing generator [138].

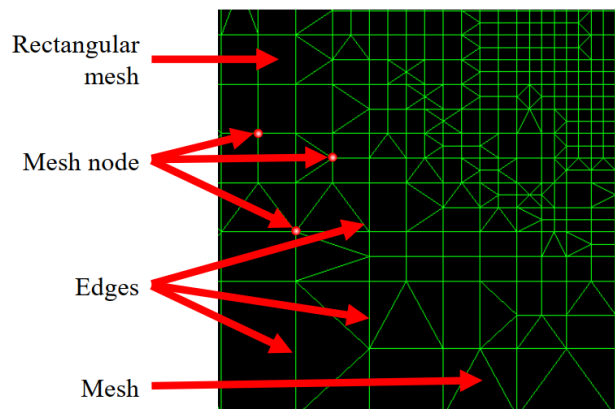


Figure 120: Presentation of the meshing used in ECORCE [139].

### 4.2.1. Drift-Diffusion equations (Poisson, holes and electrons transport)

The drift-diffusion model [140] calculate the charges carriers diffusion into the semiconductors by resolving Poisson's equations and electrons/holes transport with boundary condition specified.

#### 4.2.1.1. Calculation of the electrostatic potential $\psi$ : Poisson's equations

Poisson's equations calculate the electrostatic potential distribution in each point of the mesh and describe the electric behavior of electronic component semiconductor-based. After Maxwell's equations, we know that:

$$\vec{\nabla} \cdot \vec{D} = Q \text{ and } \vec{D} = \epsilon \cdot \vec{E} \quad (4.1)$$

where  $\vec{D}$  is the displacement vector,  $Q$  the total charge concentration [ $C/m^3$ ],  $\epsilon$  the permittivity ( $\epsilon = \epsilon_r \cdot \epsilon_0$ ) and  $E$  the electric field. From (4.1), we obtain:

$$\vec{\nabla} \cdot \epsilon \cdot \vec{E} = Q \text{ or } \vec{E} = -\vec{\nabla} \psi \quad (4.2)$$

where  $\psi$  is the electrical potential. Hence:

$$\nabla^2 \psi = -\frac{Q}{\epsilon} \quad (4.3)$$

The total electrical charge density  $Q$  is expressed as following:

$$Q = q \times (p - n + N_A^- - N_D^+) \quad (4.4)$$

where  $q$  is the elementary charge [ $C$ ],  $n$  and  $p$  respectively the electron and hole concentrations [ $m^{-3}$ ],  $N_A^-$  the charge impurity of acceptors [ $m^{-3}$ ] and  $N_D^+$  the charge impurity of donors [ $m^{-3}$ ]. Therefore, Poisson's equation is written as following:

$$\nabla^2 \psi = -\frac{Q}{\epsilon} = -\frac{q}{\epsilon} \times (p - n + N_A^- - N_D^+) \quad (4.5)$$

For this equation, fixed boundary conditions are applied at the contacts. The potential value is the sum of the biases applied and difference between the Fermi level and the void level. Thus, the internal electric field generated by the band structure is taken into account.

#### 4.2.1.2. Calculation of the electrons and holes concentration: Transport equation

The transport equations (or continuity equations) of holes and electrons calculate their concentration at each point of the mesh. There are calculated as following:

$$q \frac{\partial n}{\partial t} = \text{div } \vec{J}_n + q(G - R) \quad (4.6)$$

$$q \frac{\partial p}{\partial t} = -\text{div } \vec{J}_p + q(G - R) \quad (4.7)$$

with:

$$\vec{J}_n = qn\mu_n \vec{E} + qD_n \vec{\nabla} n \quad (4.8)$$

$$\vec{J}_p = qp\mu_p\vec{E} - qD_p\vec{\nabla}p \quad (4.9)$$

where, for the electrons  $n$ ,  $J_n$ ,  $\mu_n$  and  $D_n$  (respectively  $p$ ,  $J_p$ , and  $D_p$  for the holes) correspond to the electron density, electron current density, and electron mobility and distribution coefficient of the electrons (respectively of the holes).

When an electric field  $\vec{E}$  is applied, it creates a displacement of the charge carriers. Whereas the conduction velocity depends on the electric field and the temperature. Moreover, those equations also depend on the electron and holes mobility, the diffusion coefficient bounded by the mobility of Einstein's relationship:  $D_n/\mu_n = kT/q$  for the electrons and  $D_p/\mu_p = kT/q$  for the holes. In addition, the electrons-holes generation rate  $G$  caused by ionization [117], [141] and the recombination rate  $R$  of the electrons-holes pairs related to the Shockley-Read [142] and Auger [143] equations have an important role.

Under irradiation, the generation rate of electron-hole pairs resisting to the initial recombination depends on the electric field. This phenomenon is taken into consideration with the Yield function [144], [145].

#### 4.2.1.3. *Trapping-Detrapping equations for volume traps*

The energy diagram presented in Figure 121 describes the charges trapping-detrapping phenomenon implemented in ECORCE [146], [147]. The energy traps distribution into the oxide gaps can be represented by a set of level  $K$  for the electrons and level  $L$  for the holes. Both sets can be characterized by their activation thermal energy labeled as  $E_n$  for the electrons and  $E_p$  for the holes. Each trap level adds another equation to the drift-diffusion model. The interactions presented in Figure 121 represent:

- 1- The carrier drift in their respective bands,
- 2- The trapping of free carriers,
- 3- The recombination of trapped carriers by their free opposite carriers,
- 4- The thermal re-emission of trapped carriers in their respective bands,
- 5- The thermal emission of carriers of the opposite type from free traps.

The exchange of carriers between the level of the trap can be permitted only through their respective energetic bands. This model is known as the Multiple Trapping-Detrapping Model (MTD) [148]. An electron trap level is called acceptor-like (negatively charged when occupied by an electron) and a hole trap level is called donor-like (positively charged when occupied by a hole).

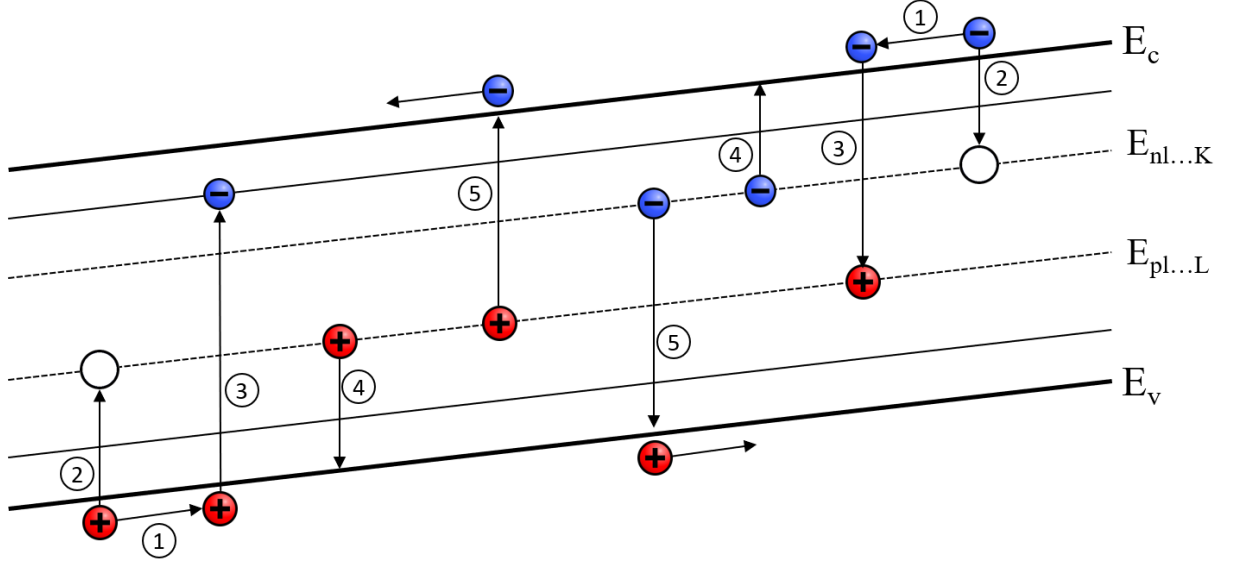


Figure 121: Interactions describing the charge trapping-detrapping model in the oxides [149].

For each electron trap level, ECORCE solves the following equations:

$$q \frac{\partial n_{ot}^{(i)}}{\partial t} = C_{not}^{(i)} - Rec_{not}^{(i)} - Ree_{not}^{(i)} + Reopt_{pot}^{(j)} \quad (4.10)$$

with:

$$C_{not}^{(i)} = \sigma_{not}^{(i)} (N_{not}^{(i)} - n_{ot}^{(i)}) (|\vec{J}_n| + J_{thnot}) \quad (4.11)$$

$$Rec_{not}^{(i)} = \sigma_{pr}^{(i)} n_{ot}^{(i)} (|\vec{J}_p| + J_{thpot}) \quad (4.12)$$

$$Ree_{not}^{(i)} = q R_{not}^{(i)} n_{ot}^{(i)} \quad (4.13)$$

$$J_{thnot} = q n v_{thnot} \quad (4.14)$$

$$J_{thpot} = q p v_{thpot} \quad (4.15)$$

$$R_{not}^{(i)} = \sigma_{not}^{(i)} v_{thnot} N_c e^{-q(E_c - E_{not}^{(i)})/kt} \quad (4.16)$$

$$Reopt_{pot}^{(j)} = q N_v \sigma_{nr}^{(j)} v_{thnot} (N_{pot} - p_{ot}) e^{-q(E_{pot}^{(j)} - E_v)/kt} \quad (4.17)$$

For each hole trap level, ECORCE solves the following equations:

$$q \frac{\partial p_{ot}^{(j)}}{\partial t} = C_{pot}^{(j)} - Rec_{pot}^{(j)} - Ree_{pot}^{(j)} + Reopt_{not}^{(i)} \quad (4.18)$$

with:

$$C_{pot}^{(j)} = \sigma_{pot}^{(j)} (N_{pot}^{(j)} - p_{ot}^{(j)}) (|\vec{J}_p| + J_{thpot}) \quad (4.19)$$

$$Rec_p^{(j)} = \sigma_{n_r}^{(j)} p_{ot}^{(j)} (|\vec{J}_n| + J_{thnot}) \quad (4.20)$$

$$Ree_p^{(j)} = q R_p^{(j)} p_{ot}^{(j)} \quad (4.21)$$

$$J_{thpot} = q n v_{thpot} \quad (4.22)$$

$$J_{thnot} = q p v_{thnot} \quad (4.23)$$

$$R_{pot}^{(j)} = \sigma_{pot}^{(j)} v_{thpot} N_v e^{-q(E_v - E_{pot}^{(j)})/kt} \quad (4.24)$$

$$Reopt_{not}^{(i)} = q N_v \sigma_{Pr}^{(i)} v_{thpot} (N_{not} - n_{ot}) e^{-q(E_{not}^{(i)} - E_v)/kt} \quad (4.25)$$

For the electrons,  $n_{ot}^{(i)}$ ,  $\sigma_{not}^{(i)}$  and  $N_{not}^{(i)}$  (same as  $p_{ot}^{(j)}$ ,  $\sigma_{pot}^{(j)}$  and  $N_{pot}^{(j)}$ , for the holes) respectively define the trapped charge carriers density, the trapping cross-section and the electrons density. As for the trapped carriers recombination cross-section and the energy level of electrons on the level  $i$  (and  $j$  for the holes) are defined by  $\sigma_{pr}^{(i)}$  and  $E_n^{(i)}$  for the electrons and  $\sigma_{nr}^{(j)}$  and  $E_p^{(j)}$  for the holes. Moreover, for the electrons,  $v_{thn}$ ,  $N_c$  and  $E_c$  (same as  $v_{thp}$ ,  $N_v$ , and  $E_v$  for the holes) respectively define the thermal velocity, the state density in the allowed band and the energy level in the allowed band for the electrons. This trap appears in the volume of the oxide, then the units used for volume traps are: [ $\text{cm}^{-3}$ ] for densities and [ $\text{C.cm}^{-3}.\text{s}^{-1}$ ] for capture, recombination and thermal emission rates. It will be different for interface traps.

To take into account those traps level, the density of electrostatic charge  $Q$  and the continuity equations become:

$$Q = \left( Q_{fix} + N_d - n - N_a + p - \sum_{i=1}^K n_{ot}^{(i)} + \sum_{j=1}^L p_{ot}^{(j)} \right) \quad (4.26)$$

$$q \frac{\partial n}{\partial t} = \text{div} \vec{J}_n + qG - \sum_{i=1}^K C_{not}^{(i)} - \sum_{j=1}^L Rec_{pot}^{(j)} + \sum_{i=1}^K Ree_{not}^{(i)} + \sum_{j=1}^L Reopt_{pot}^{(j)} \quad (4.27)$$

$$q \frac{\partial p}{\partial t} = -\text{div} \vec{J}_p + qG - \sum_{j=1}^L C_{pot}^{(j)} - \sum_{i=1}^K Rec_{not}^{(i)} + \sum_{j=1}^L Ree_{pot}^{(j)} + \sum_{i=1}^K Reopt_{not}^{(i)} \quad (4.28)$$

This model takes into consideration the trapping cross-section and the recombination cross-section depending on the electric field and the reduction of the activation energy depending on the electric field, known as the Poole-Frenkel effect.

In addition, the drift-diffusion model considers as well the thermal conductivity variation depending on the temperature and the variation of the carrier mobility depending on the dopant concentration, electric field, and free carrier density.

#### 4.2.1.4. Multi-trapping de-trapping equation for interface traps

Interface traps are formed from lattice mismatch between Oxide and Silicon atoms. In pristine devices, the interface traps density is low. Irradiation can generate much higher density.

In this study, we consider that interface traps density is distributed homogenously along gate's length.

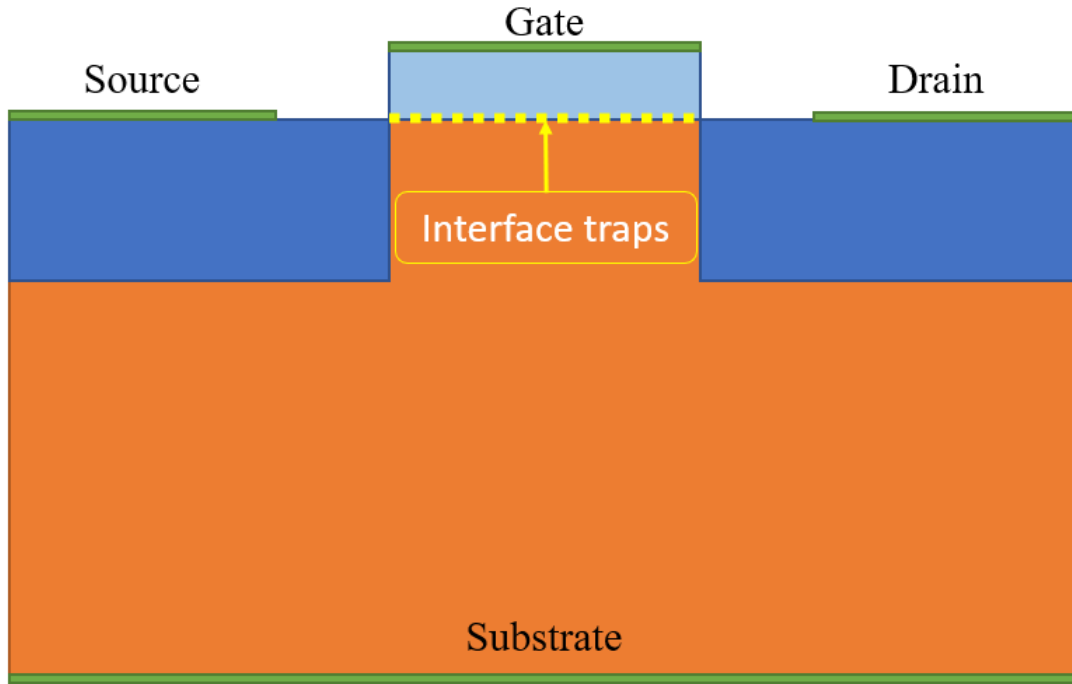


Figure 122: Interface layer between gate oxide and silicon.

Interface traps model in ECORCE uses the same MTD model than volume traps. The main difference are the units used: [ $\text{cm}^{-2}$ ] for densities and [ $\text{C.cm}^{-2}.\text{s}^{-1}$ ] for capture, recombination and thermal emission rates.

The energy traps distribution at the interface of Si/SiO<sub>2</sub> can be represented by a set of level M for the electrons and level N for the holes.

For each electron interface trap level, ECORCE solves the following equations:

$$q \frac{\partial n_{it}^{(k)}}{\partial t} = C_{nit}^{(k)} - Rec_{nit}^{(k)} - Ree_{nit}^{(k)} + Reopt_{pit}^{(l)} \quad (4.29)$$

with:

$$C_{nit}^{(k)} = \sigma_{nit}^{(k)} (N_{nit}^{(k)} - n_{it}^{(k)}) (|\overline{J_{nit}}| + J_{thnit}) \quad (4.30)$$



$$Rec_{nit}^{(k)} = \sigma_{p_r}^{(k)} n_{it}^{(k)} (|\overrightarrow{J_{pit}}| + J_{thpit}) \quad (4.31)$$

$$Ree_{nit}^{(k)} = q R_{nit}^{(k)} n_{it}^{(k)} \quad (4.32)$$

$$J_{thnit} = q n v_{thnit} \quad (4.33)$$

$$J_{thpit} = q p v_{thpit} \quad (4.34)$$

$$R_{nit}^{(k)} = \sigma_{nit}^{(k)} v_{thnit} N_c e^{-q(E_c - E_{nit}^{(k)})/kt} \quad (4.35)$$

$$Reopt_{pit}^{(l)} = q N_v \sigma_{n_r}^{(l)} v_{thnit} (N_{pit} - p_{it}) e^{-q(E_{pit}^{(l)} - E_v)/kt} \quad (4.36)$$

For each hole interface trap level, ECORCE solves the following equations:

$$q \frac{\partial p_{it}^{(l)}}{\partial t} = C_{pit}^{(l)} - Rec_{pit}^{(l)} - Ree_{pit}^{(l)} + Reopt_{nit}^{(k)} \quad (4.37)$$

with:

$$C_{pit}^{(l)} = \sigma_{pit}^{(l)} (N_{pit}^{(l)} - p_{it}^{(l)}) (|\overrightarrow{J_{pit}}| + J_{thpit}) \quad (4.38)$$

$$Rec_{pit}^{(l)} = \sigma_{n_r}^{(l)} p_{it}^{(l)} (|\overrightarrow{J_{nit}}| + J_{thnit}) \quad (4.39)$$

$$Ree_{pit}^{(l)} = q R_{pit}^{(l)} p_{it}^{(l)} \quad (4.40)$$

$$R_{pit}^{(l)} = \sigma_{pit}^{(l)} v_{thpit} N_v e^{-q(E_v - E_{pit}^{(l)})/kt} \quad (4.41)$$

$$Reopt_{nit}^{(k)} = q N_v \sigma_{p_r}^{(k)} v_{thpit} (N_{nit} - n_{it}) e^{-q(E_{nit}^{(k)} - E_v)/kt} \quad (4.42)$$

For the electrons,  $n_{it}^{(k)}$ ,  $\sigma_{nit}^{(k)}$  and  $N_{nit}^{(k)}$  (same as  $p_{it}^{(l)}$ ,  $\sigma_{pit}^{(l)}$  and  $N_{pit}^{(l)}$ , for the holes) respectively define the interface trapped charge carriers density, the interface trapping cross-section and the electrons density. As for the trapped carriers recombination cross-section and the energy level of electrons on the level  $k$  ( $l$  for the holes) are defined by  $\sigma_{p_r}^{(k)}$  and  $E_{nit}^{(k)}$  for the electrons ( $\sigma_{n_r}^{(l)}$  and  $E_{pit}^{(l)}$  for the holes). Moreover, for the electrons,  $v_{thnit}$ ,  $N_c$  and  $E_c$  (same as  $v_{thpit}$ ,  $N_v$ , and  $E_v$  for the holes) respectively define the thermal velocity, the state density in the allowed band and the energy level in the allowed band for the electrons.

In order to take into account those interface traps level, because of unit change between free carriers ( $\text{cm}^{-3}$ ) and carriers trapped at the interface ( $\text{cm}^{-2}$ ), all terms are taken into account by integrating over volume and surface the corresponding values. Therefore, the total electrostatic charge density  $Q$  and the continuity equations become:

$$\int_{volume} Q dv = \int_{volume} \left( Q_{fix} + N_d - n - N_a + p - \sum_{i=1}^K n_{ot}^{(i)} + \sum_{j=1}^L p_{ot}^{(j)} \right) dv \quad (4.43)$$

$$+ \int_{surface} \left( - \sum_{k=1}^M n_{it}^{(k)} + \sum_{l=1}^N p_{it}^{(l)} \right) ds$$

$$\int_{volume} q \frac{\partial n}{\partial t} dv =$$

$$\int_{volume} \text{div} \vec{J}_n + qG - \sum_{i=1}^K C_{not}^{(i)} - \sum_{j=1}^L Rec_{pot}^{(j)} + \sum_{i=1}^K Ree_{not}^{(i)} + \sum_{j=1}^L Reopt_{pot}^{(j)} dv \quad (4.44)$$

$$+ \int_{surface} - \sum_{k=1}^M C_{nit}^{(k)} - \sum_{l=1}^N Rec_{pit}^{(l)} + \sum_{k=1}^M Ree_{nit}^{(k)}$$

$$+ \sum_{l=1}^N Reopt_{pit}^{(l)} ds$$

$$\int_{volume} q \frac{\partial p}{\partial t} dv =$$

$$\int_{volume} -\text{div} \vec{J}_p + qG - \sum_{j=1}^L C_{pot}^{(j)} - \sum_{i=1}^K Rec_{not}^{(i)} + \sum_{j=1}^L Ree_{pot}^{(j)} + \sum_{i=1}^K Reopt_{not}^{(i)} dv \quad (4.45)$$

$$+ \int_{surface} - \sum_{l=1}^N C_{pit}^{(l)} - \sum_{k=1}^M Rec_{nit}^{(k)} + \sum_{l=1}^N Ree_{pit}^{(l)}$$

$$+ \sum_{k=1}^M Reopt_{nit}^{(k)} ds$$

#### 4.2.2. Heating equations (temperature calculation)

The heat equation [150] calculates the temperature at each point of the mesh and allows to describe the thermal behavior of semi-conductor based components. The equation is written as follow:

$$\nabla^2 T = \frac{1}{D} \frac{\partial T}{\partial t} - \frac{P}{\lambda} \quad \text{with } D = \frac{\lambda}{\rho c_p} \quad (4.46)$$

where T is the temperature in Kelvin, D the thermal diffusivity, P the thermal power generated per volume unit [ $\text{W.m}^{-3}$ ],  $\lambda$  the thermal conductivity [ $\text{W.m}^{-1}.\text{K}^{-1}$ ],  $\rho$  the density [ $\text{kg.m}^{-3}$ ], and  $c_p$  the thermal capacity of the material [ $\text{J.kg}^{-1}.\text{K}^{-1}$ ].

The generated thermal power per volume unit P depends on the equation selected by the user. If all of the equations of the drift-diffusion model are selected, the generated thermal power by volume unit P can be written as follow:

$$P = P_{\text{fix}} + \vec{E} \cdot \vec{J}_n + \vec{E} \cdot \vec{J}_p \quad (4.47)$$

where  $P_{\text{fix}}$  corresponds to a fixed thermal power defined by the user.

### 4.3. 1D simulation of PN junction at storage node

The decreasing of retention time is the key parameter to evaluate the DRAM cell degradation. Leakage current in DRAM cells is an ongoing research topic as it affects directly the refresh rate and leads to an increased power consumption, reducing the lifetime of DRAM cells. When the leakage current become substantial it can cause stuck bits. The cause of this phenomenon is strongly suggested by displacement damage cluster induced by single particle that can be found in space. In this work, we use TCAD simulation to investigate the basic mechanisms that lead to leakage current in degraded DRAM cells.

#### 4.3.1. DRAM cell and damage cluster model

##### 4.3.1.1. *Simulation model and discharge mechanism*

A DRAM cell consists of a MOSFET transistor connected to a capacitor that stores the cell information. After a write or refresh operation has been performed, charges start to leak off the capacitor, thus it requires a regular refresh to preserve information.

Capacitor's charge overtime is expressed as equation:

$$Q(t) = Q_0 e^{-\frac{t}{RC}} \quad (4.48)$$

At the first order, we consider discharge behavior of DRAM cell as the resistance – capacitor (RC) circuit. The time constant of the capacitor is given as:

$$\tau = RC \quad (4.49)$$

Where the resistance can be calculated from simulation result of total leakage current by applying Ohm law for RC circuit:  $R = \frac{V_{\text{Initial}}}{I_{\text{leakage}}}$ . For a submicron DRAM, capacitance value varies between 20fF and 40fF.

In theory, charges in capacitor are considered fully depleted at  $5\tau$ , when at  $0.7\tau$  charges are at half of its original capacitance. Consider initial leakage current  $I_{\text{leakage}}$ , the time required to discharge the capacitor to a certain voltage  $V$  is defined as:

$$t = -\frac{V_{\text{initial}}}{I_{\text{leakage}}} C \times \ln \left( \frac{V}{V_{\text{initial}}} \right) \quad (4.50)$$

During this study, we considered the cell's information was invalid when capacitor depleted 63% of its original capacitance which means at  $1\tau$ .

In order to represent the sensitive zone of charge as well as simplify our simulation and improve calculation convergence, 1D simulation of the P-N+ junction at the storage node has been chosen.

Its geometry and doping profile are represented in Figure 123. The size of junction is  $0.7\mu\text{m}$

divided equally for P size and N+ size, doping values are  $10^{17} \text{cm}^{-3}$  and  $10^{18} \text{cm}^{-3}$  respectively, and were selected to be compatible with the  $0.7 \mu\text{m}$  technology node. The device was chosen to represent the zone of interest with the idea parameters in order to understand the main mechanism. Its feature size is bigger than those from technology nodes featured in our previous study, but as we are mainly interested in reproducing the radiation induced leakage current enhancement, the obtained results will thus be considered relevant in proving of the mechanisms.

Reverse bias is applied to the junction to maximize the depletion area.

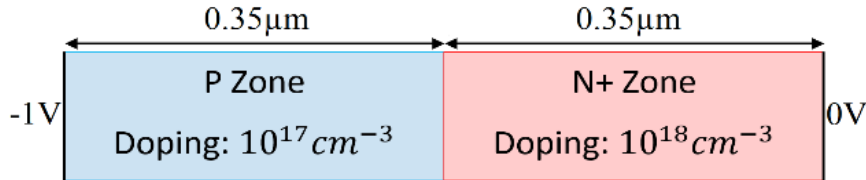


Figure 123: 1D P-N+ junction model

#### 4.3.1.2. Cluster model

This work presupposes that the decrease of retention time in DRAM cells is due to a decrease of resistance at storage node junction and it is caused by displacement damage cluster induced by proton, neutron or heavy ion.

Gossick proposed a model of cluster of defects [47] and it has been successfully implemented in previous study [151], [152]. The proposed model in use for acceptor-like type displacement damage cluster has a uniform spherical shape, with the size ranging from  $20\text{nm}$  to  $100\text{nm}$  and the concentration between  $10^{18}$  and  $10^{20} \text{cm}^{-3}$ . The defect energy level is  $0.56 \text{eV}$  in the middle of band gap energy.

However, the Gossick model has its limitation [153], which is the lack of cluster metastability, defect migration or annealing effect. As, our goal is to correlate the leakage current with cluster of defects, these properties can be disregarded in this study. In the following simulation, we consider the cluster as a slab of silicon, characterized by the width, the position in the junction and the concentration of acceptor-like traps.

### 4.3.2. Simulation and result

#### 4.3.2.1. Simulation results for pristine device

The simulation has been conducted first on non-damaged device. We then obtained a maximum leakage current of  $1.21 \times 10^{-17} \text{A}$  account for a  $700 \text{nm}^2$  junction.

In this study, we focused on the leakage current alongside the storage node PN junction where two leakage sources are dominant: Junction leakage and gate-induced drain leakage. For the technological nodes considered, gate-induced drain leakage (GIDL) and reverse-biased junction leakage are the dominant leakage mechanisms in the undamaged SDRAM cell [154]. GIDL, caused by band-to-band tunneling [155], is expected to rise when clusters are induced, but not by several orders of magnitude and is thus considered as negligible for a damaged SDRAM cell.

By using the equation (4.49) we acquired a  $1657\text{s}$  retention time (considering a typical  $20\text{fF}$  capacitance). It should be noted that the PN junction in this simulation is ideal and has no defects or migration through manufacturing process.

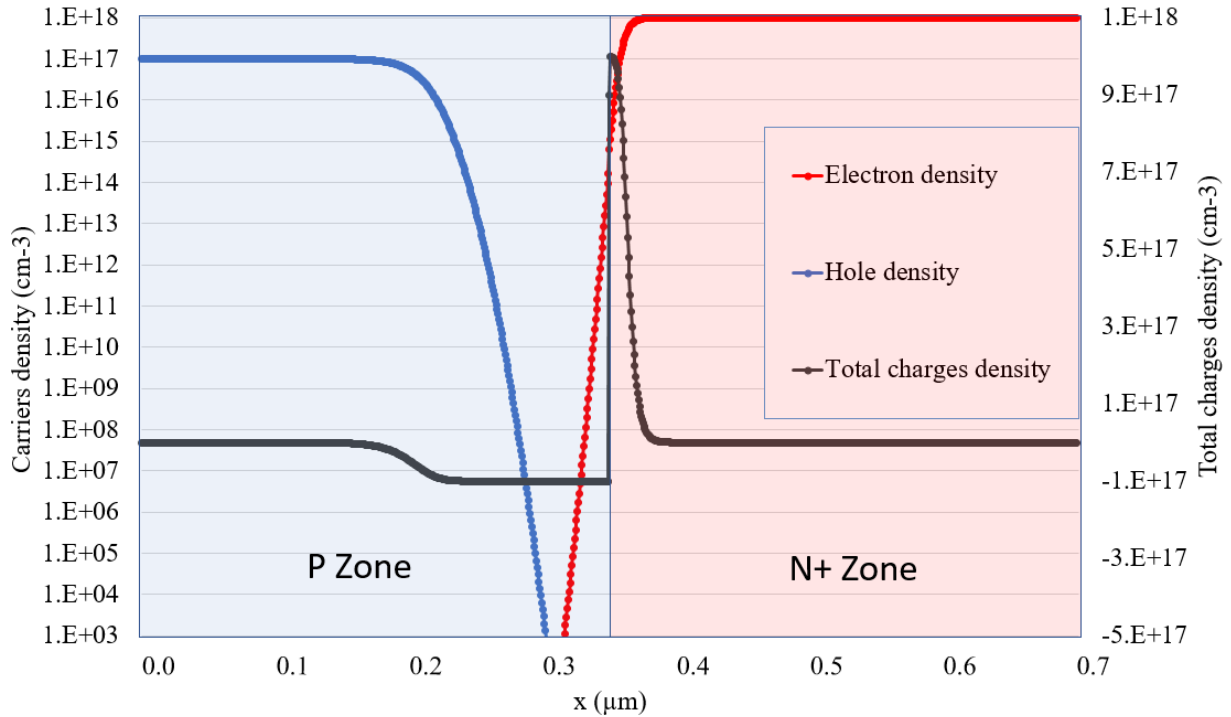


Figure 124: Carrier concentration and charge density of pristine junction.

Figure 124 represents the spatial distribution of carrier's density and total electric charge in P-N+ junction. The left axis represents electron and hole density in logarithm scale, while the right axis shows us the total charge. Due to the higher doping value in n+ side the depletion area is shifted toward the p zone.

#### 4.3.2.2. Main mechanism inside the damage junction.

In order to understand the main mechanisms of this phenomenon, we considered a 20nm width cluster placed inside the depletion area ( $x = 0.34\mu\text{m}$ ). The presence of defect cluster modified locally the carrier and electric charge as evidenced by Figure 125, which presents carrier density and total electric charge across a damaged junction.

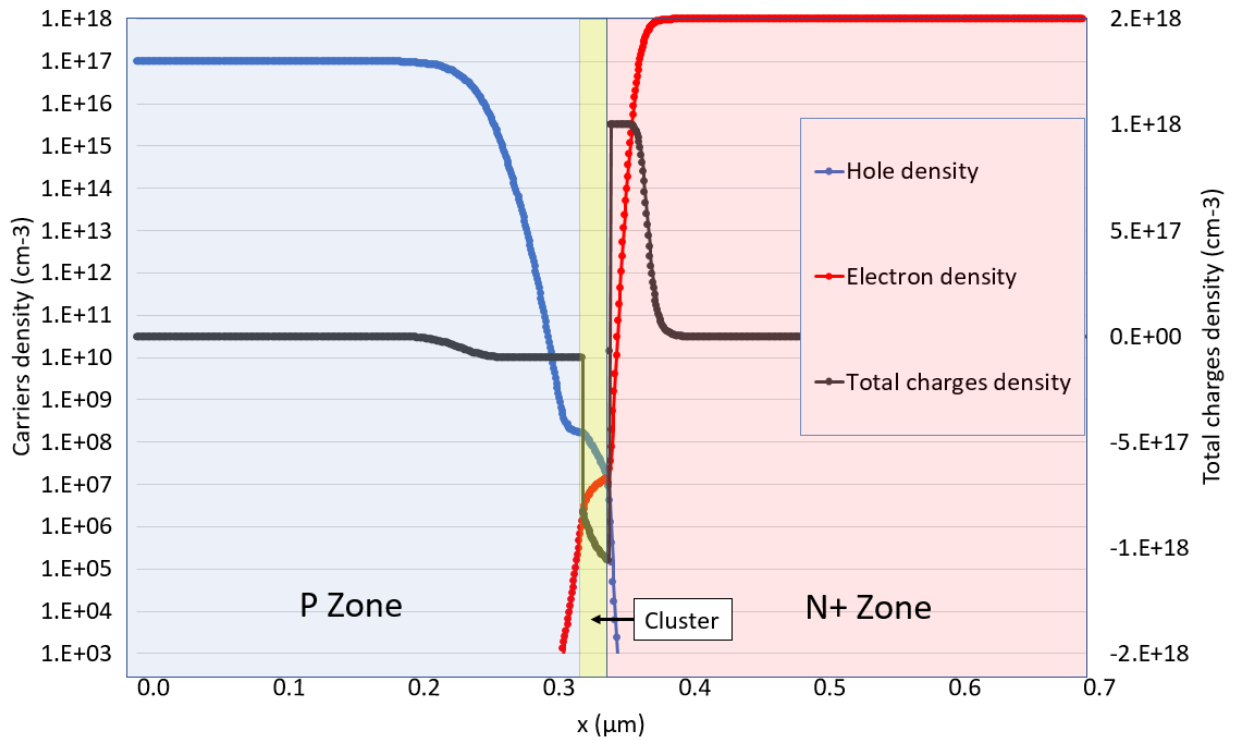


Figure 125: Carrier concentration and charge density of damage junction.

The contribution of the previously described generation/recombination processes are given in Figure 126, including recombination and generation rates and electric field in the P-N+ junction.

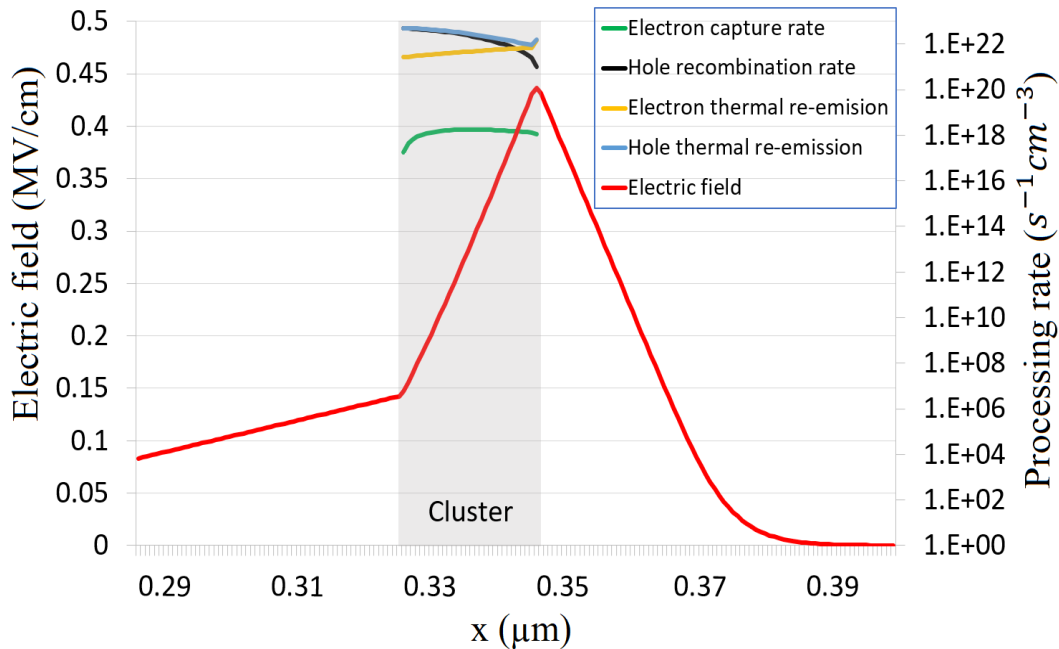


Figure 126: Generation, recombination, trapping process rate and electric field across damage junction.

Electron capture rate is orders of magnitude below the other processes' rates and thus can be considered as negligible. Thermal re-emission of holes reaches its maximum at the beginning of cluster position ( $x = 0.33\mu\text{m}$ ) however, most of them are recombined.

Closer to the end of cluster ( $x=0.35 \mu\text{m}$ ), thermal emission rate for trapped electron increases, resulting in the increase of the net electron generation rate. In the meantime, hole recombination decreases more sharply than thermal hole emission, leading to the increase of the net holes generation rate.

The carrier generation process can be summarized as: thermal emission of holes and creation of trapped electrons, then a part of generated holes recombines with trapped electrons. The remaining carriers mostly come from thermal emission of electron.

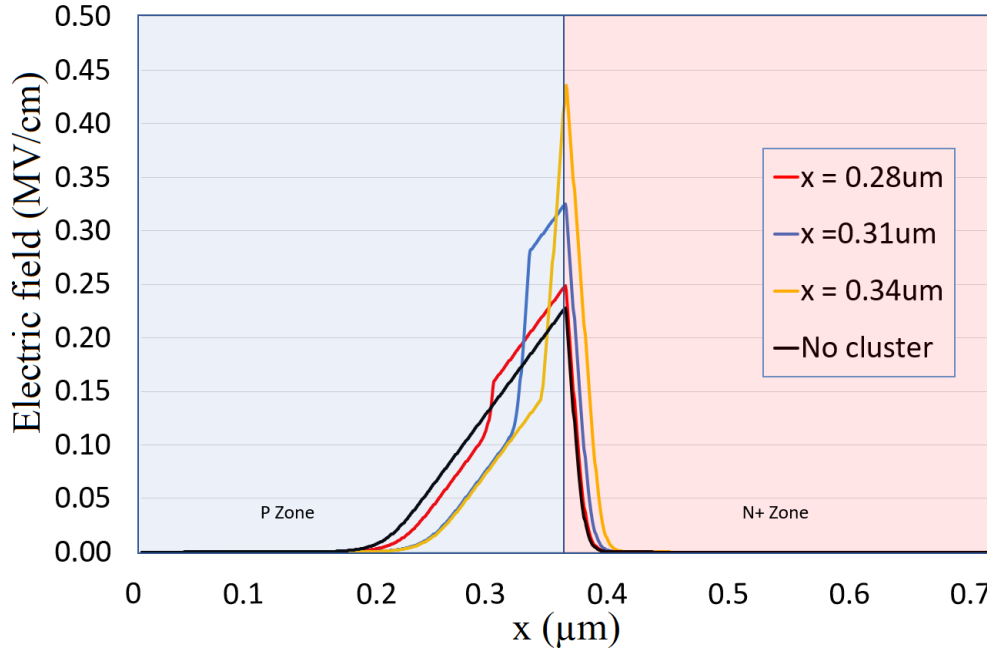


Figure 127: Electric field in the junction for different cluster position and comparison with pristine one.

The trapped electron also changes the shape and values of electric field inside the junction. Multiple linear regions have formed in the electric field curve instead of two linear regions in pristine P-N+ junction. Figure 127 plots the local electric field enhancement by different cluster's locations. In general, the electrical field is in the shape of three quasi-linear regions. From the beginning of depletion region to the beginning of cluster, the electric field increases linearly with the position, however with a lower value compare to the pristine junction. At the cluster, the electric field rise up fast as the result of high concentration of trapped electrons. Outside of cluster effect, the electric field slowly fall down until the end of P zone, then decreases rapidly toward the N+ zone.

#### 4.3.2.3. Influence of displacement damage cluster position.

The damage cluster has been placed at different positions alongside of the P-N+ junction to study the effect of its position on the device. In other words, we investigated the most sensitive regions where the creation of the cluster by a particle (such as cosmic ray) is an issue. Throughout the simulation we see that leakage current increases dramatically when the displacement cluster is within the depletion area. The leakage current increases to the maximum value of  $1.09 \times 10^{-11} \text{A}$  which corresponds to 1.84ms retention time of a 20fF capacitor fully

discharged, This value well below the JEDEC standard for refresh rate of DRAM memory (64ms).

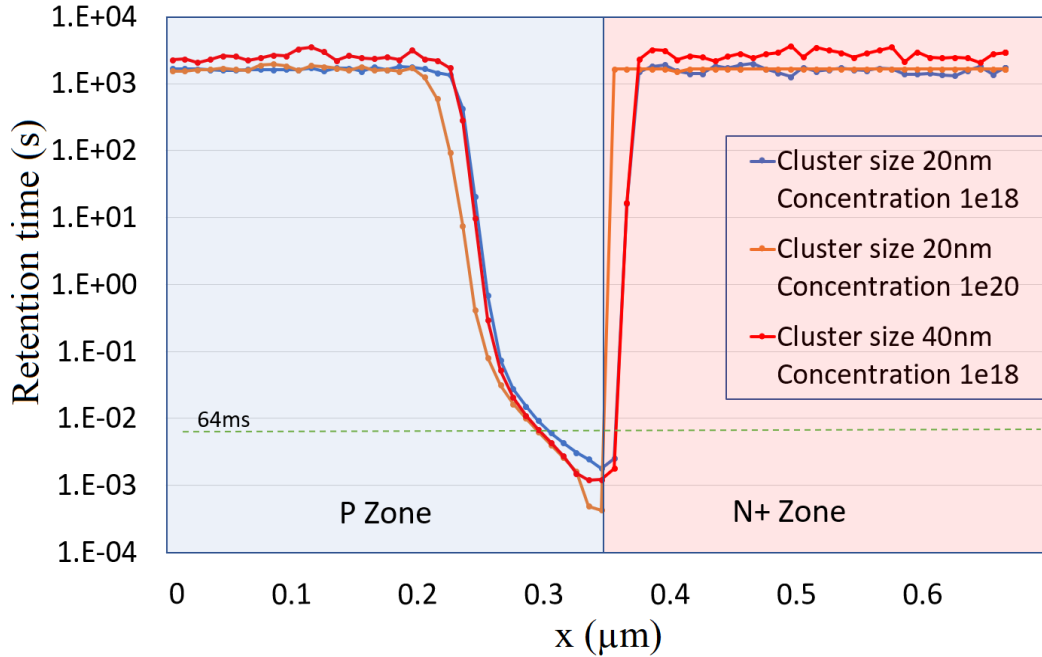


Figure 128: Retention time as function of cluster position.

Figure 128 shows the retention time at different positions of the displacement damage cluster. We can clearly see that a damage cluster has no effect on leakage current when it stays outside of the depletion area. However, when it falls into the depletion area, the retention time reduces rapidly and get the minimum as close to N+ zone. These results are in agreement with previous work that suggests that the cluster position has a crucial role when it is placed in the depletion area [68].

#### 4.3.2.4. Influence of temperature and applied voltage on damaged junction.

By using the same damaged junction with cluster of defects of 20nm, inside the depletion area  $x = 0.34\mu\text{m}$  and the concentration of  $10^{18} \text{ cm}^{-3}$ , we can study the effect of temperature as well as different voltage applied.



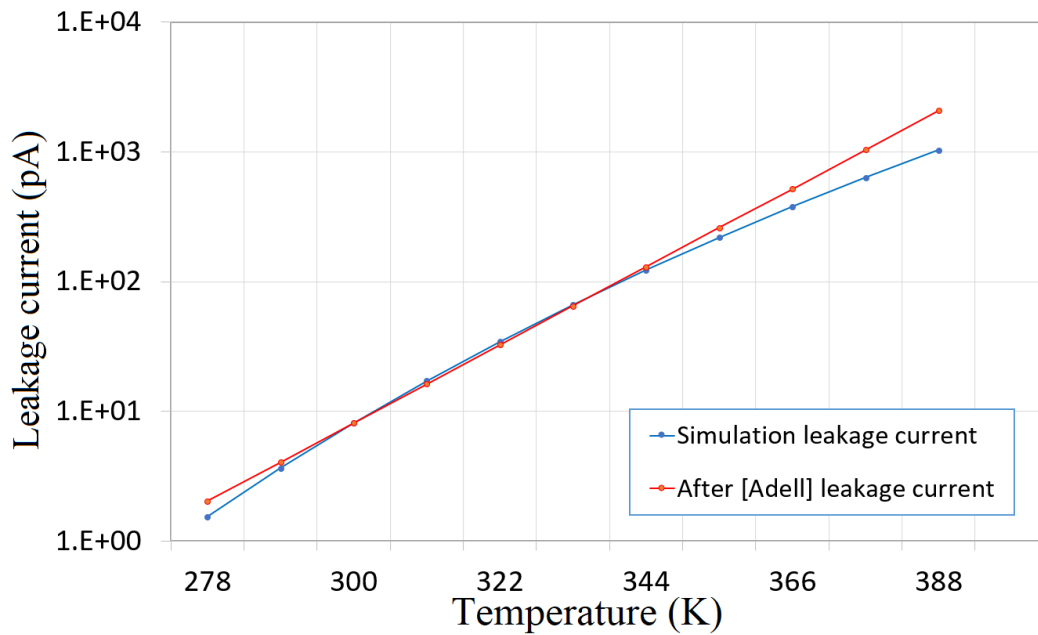


Figure 129: Leakage current as the function of temperature.

Previous studies show the strong dependency of temperature to the leakage current. Adell [156] experimentally showed that the leakage current is approximately doubled every 11K because of dependency of the intrinsic carrier density on temperature. By using ECORCE, we were able to simulate the phenomenon at different temperatures. Figure 129 represents the effect of temperature on leakage current of ECORCE's simulation in comparison with the calculation value based on value at 300K. We can see the consistency between two set of result from 300-385K working range of SDRAM.

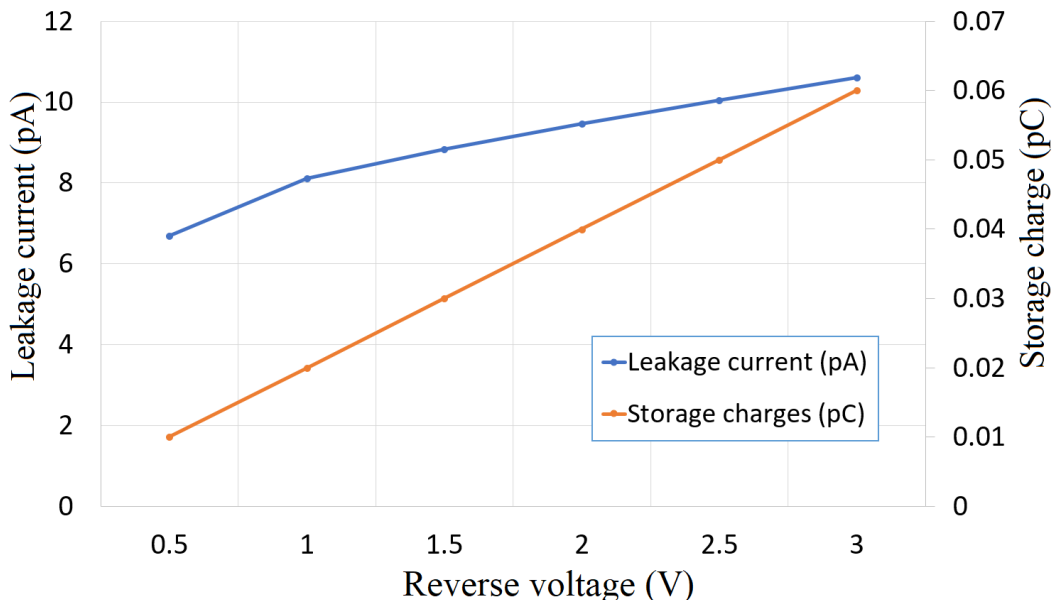


Figure 130: Leakage current and stored charge as the function of reverse voltages applied.

The influence of voltage applied to the storage node was investigated with the value modified from 0.5 V to 3V.

As seen from Figure 130, both leakage current and storage charge increase linearly with the reverse voltage, at least above 1V. The storage charges increase faster as the reverse voltages applied increase (by factor of 6), while, the leakage current increase in a slower rate (by factor of 1.5). Thus, the same cluster will have different impact on retention time, depending on the storage node voltage applied. Decreasing storage node can reduce the depletion zone width as sensitive volume, however, it can also reduce the retention time because the leakage current is still high compare to the charge stored in capacitor. On the other hand, increasing storage node voltages will increase the retention time by increasing the total charges in capacitor.

#### 4.4. Technological considerations

From the result presented above, it is clear that if the cluster stays outside of the depletion region it does not affect the leakage current of the junction. Therefore, the width of depletion region is the key parameter to evaluate the sensitive of a DRAM cell to the phenomenon.

The depletion zone width  $W$  for a P-N+ silicon junction is given by [18]:

$$W = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_{bi} - V)} \quad (4.51)$$

Where  $\varepsilon_0$  is the vacuum permittivity,  $\varepsilon_r$  is the relative permittivity of silicon,  $q$  is the elementary charge,  $N_A$  and  $N_D$  are the doping concentration of acceptor and donors respectively,  $V_{bi}$  is the junction's built-in potential and  $V$  is the applied voltage.

Under reverse bias, and if  $N_A \ll N_D$  the depletion region stays mostly on the P-zone then (7) can be simplified as:

$$W = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{q}\left(\frac{1}{N_A}\right)(V_{bi} + V_{storage})} \quad (4.52)$$

Two technological parameters that drive the sensitive volume of a single DRAM cell are the doping profile (the lower doping for P-zone, the bigger sensitive volume) and applied voltage.

Across SDRAM generations, the storage node voltage decreases. Another consequence of size downscaling across technology nodes is the increase of doping concentrations. This will decrease the depletion zone width but increase the cluster-induced junction leakage current.

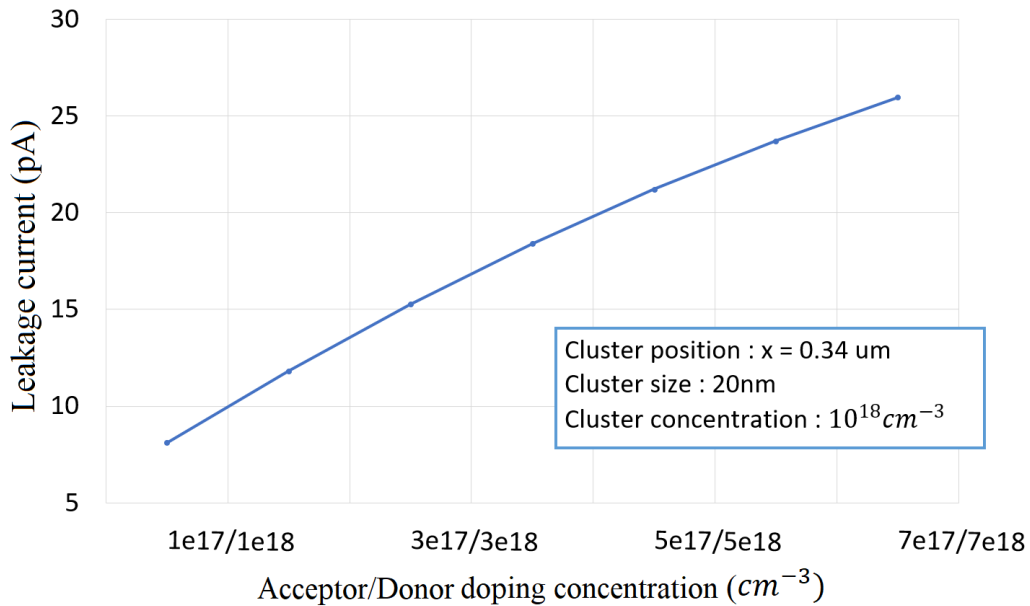


Figure 131: Leakage current as the function of acceptor/donor doping concentration.

Increasing of the acceptor doping concentration will reduce the size of depletion area, therefore keeping the same bias voltage will increase the potential inside the depletion region hence it will collect more charges and result is the leakage current rising.

The Figure 131 shows the simulation result of leakage current with the increasing of both acceptor and donor doping concentration and keeping the same other parameters of the junction as well as the cluster size of 20nm, concentration of  $10^{18}cm^{-3}$  and at position  $x = 0.34\mu m$ . The leakage current increase as the increasing of acceptor/donor doping.

#### 4.5. Conclusion

TCAD simulation of P-N+ junction storage node has been performed by considering the discharge of the equivalent RC circuit. Our TCAD simulation show that excess carriers generated through acceptor states then collected at the contact increase the leakage current.

Our modeling confirms a number of findings, hypothesized in earlier works: Damage clusters in the depletion region can increase greatly (by more than three orders of magnitude) the p-n+ junction's leakage current. As expected, when the cluster is created outside the depletion region (i.e, does not overlap with depletion region), it has no effect as carrier recombination compensates carrier generation.

Depending on working state of SDRAM cell, it is more vulnerable to data loss: different working voltages lead to different width of depletion region. Hence, the key parameter to evaluate the cell's sensitivity to degradation is the depletion region width, which depends on doping values and storage node voltage applied. Our study also shows the agreement with previous experimental results on cluster-induced leakage current that exponentially increases with temperature.

Our results and analysis have shown two technological parameters, namely the doping concentration of the P-doped area and the storage node voltage, can shape a cell's response to

single-event degradation, as they influence on both sensitive volume and leakage current of a cell.

In the next chapter, simulation will continue on 2D model and more defect models will be included into device.

# **Chapter 5: 2D TCAD modeling of defect cluster, interface traps and volume traps in a MOS transistor: singular and combined effects**

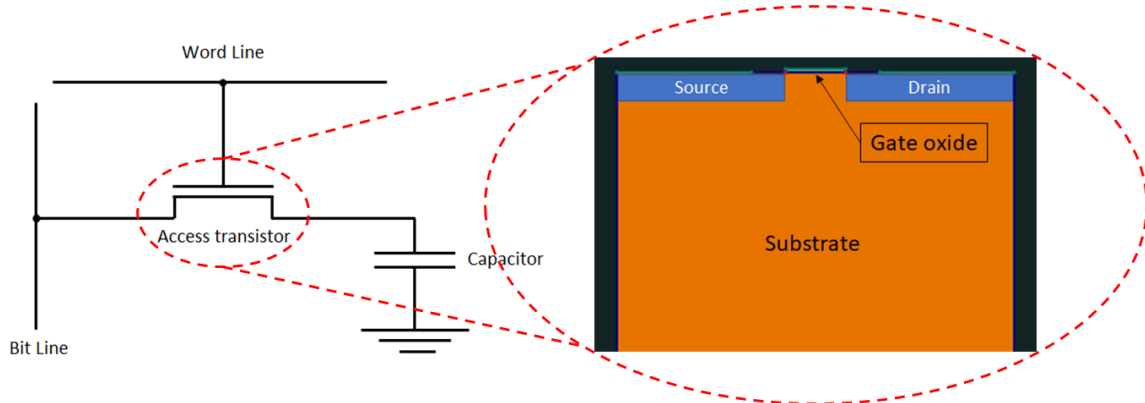
## 5.1. Introduction

In previous chapter, 1D simulation of the storage node was simulated and the effects of defect cluster have been showed. In this chapter 5, the 2D model of the access transistor will be studied with different defect's configurations. Beside defect cluster, interface traps and volume traps under influence of incident energetic particle will be studied.

This chapter starts with the defects model that ECORCE used in 2D modeling of the MOS transistor. Then, models for different types of radiation effects are introduced. Finally, singular and combined effects on the leakage current of the devices are presented.

## 5.2. 2D simulation of the DRAM access transistor

As mentioned in chapter 2, the main source of leakage current from DRAM cell is through transistor, therefore, a 2D model of access transistor is used in this thesis. First, the device is constructed and then different radiation effects will be implemented to observe device's leakage current response. We showed in chapter 2 that leakage current can come from the capacitor or the transistor of the cell. For the modeling we focus on the transistor.



*Figure 132: Access transistor of individual DRAM cell.*

### 5.2.1. 2D model of the device

Figure 133 shows the schematic of the NMOS access transistor that is created and analyzed using ECORCE software. In the framework of this thesis, with the aim of study the effect in qualitative aspect, an academic transistor model is used.

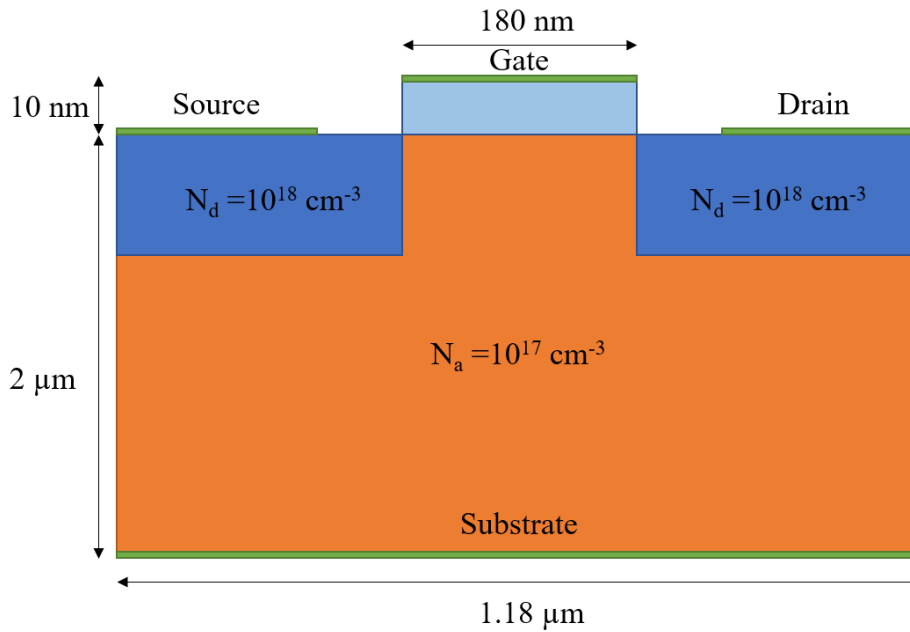


Figure 133: Schematic view of the 2D NMOS access transistor of DRAM cell used in this study.

Here, different regions (and the material used) of the device dimensions as well as doping profile can be identified.

The information of the transistor used for this study are presented as following:

- Gate length 180 nm
- Oxide material was  $\text{SiO}_2$ .
- Oxide thickness was 10nm.
- Source and Drain doping values were  $10^{18} \text{ cm}^{-3}$  with an n-type (Arsenic) impurity, with Gaussian profile
- Substrate doping value was  $10^{17} \text{ cm}^{-3}$  with a p-type (Boron) dopant with Gaussian profile

### 5.2.2. Simulation Methodology

The main objective of the simulation is monitoring the leakage current of the access transistor in off state.

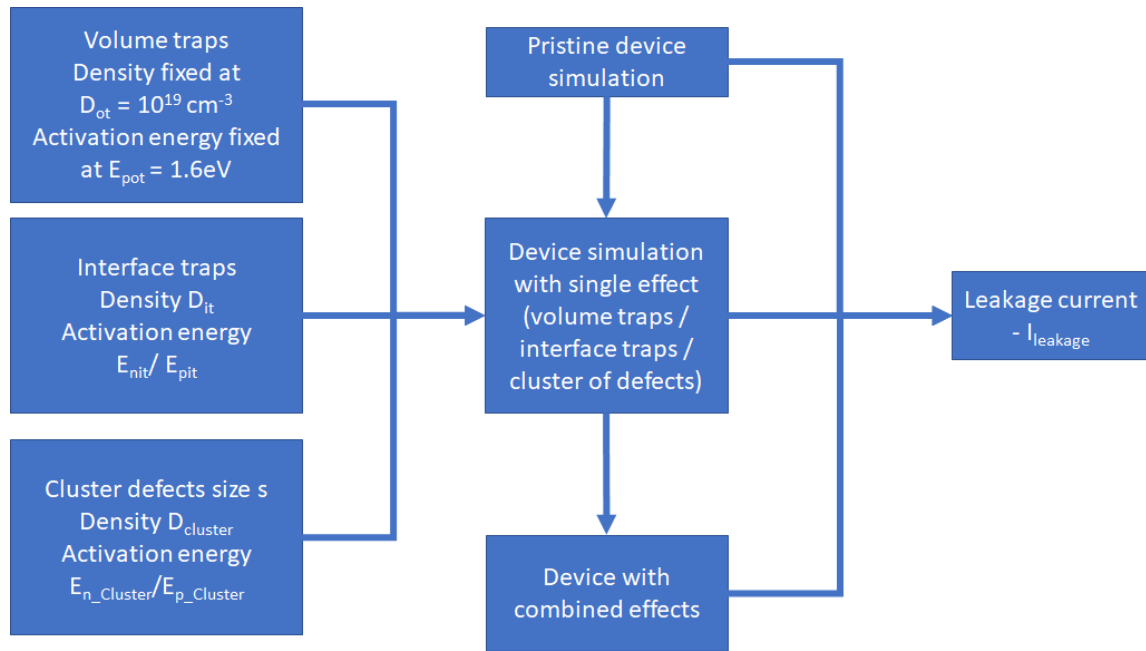


Figure 134: Simulation scheme of 2D modeling

We first simulate the device structure with no defects (pristine case) and then extract the leakage current ( $I_{leakage}$ ) when the gate bias is at 0V and the drain bias is at 3.3V. This is represented by the first block in Figure 134. Then, from the pristine device, three radiation effects are modeled separately:

- One trap level in volume of the oxide with density “ $N_{pot}$ ” ( $cm^{-3}$ ) constant and activation energy “ $E_{pot}$ ” (eV),
- One trap level created over entire interface between oxide and silicon with density “ $N_{pit}$ ” ( $cm^{-2}$ ) and activation energy “ $E_{pit}$ ” (eV),
- Cluster of defects created in the silicon with the size “ $s$ ” (nm), density “ $N_{cluster}$ ” ( $cm^{-3}$ ) and activation energy “ $E_{n\_cluster}$ ” or “ $E_{p\_cluster}$ ” (eV) at specific location (x,y) depending on clusters type.

From now on, the term activation energy -  $E_a$  will be used to clarify the activation energy respecting to the activation every of each trap or cluster type.

To reduce the field of investigation, we fixed the less sensitive parameters:

- $N_{pot} = 10^{19} cm^{-3}$ , constant in the oxide
- $E_{pot} = 1.6 eV$ , high enough to ensure trapped charges cannot be thermally reemitted
- $N_{cluster} = 10^{19} cm^{-3}$

With these single radiation effect modeling, we were able to extract the worst-case values of unfixed parameters, that is to say the values that give the highest leakage current.

Then, using these worst values and since the three effects interact each other, we simulate the effect of coupled phenomena:

- Traps in the volume of the oxide and cluster,
- Traps in the volume of the oxide and interface traps,
- Cluster and interface traps,



- Traps in the volume of the oxide, interface traps and cluster.

To be as close as possible to experiments, we modeled irradiation applying proton and Xenon ions with the same energy than the experiments. These particles are both able to create the three studied effects: trapping of charges in the volume of the oxide, creation of defects at the interface oxide-silicon and creation of cluster of defects in the silicon

While volume trapping and interface states are systematically generated by a particle, the cluster has only a probability to be created in silicon substrate. Furthermore, when it is created, the cluster position can be at any position along the track of the particle.

### 5.2.3. Cluster model for 2D simulation

Cluster model used in 2D simulation are similar to 1D model. However, while in 1D we only modeled p-type cluster, in 2D we also investigated the effect of n-type clusters. For 2D modeling we checked the influence of the cluster position for x and y axis as illustrated in Figure 136. the additionally n type cluster is included. The different is 2D representation and spatial position in the device. Specification of cluster is included in Table 21 and its spatial position is illustrated in Figure 136. The n-type cluster was also modeled for 2D simulation.

Table 21: Cluster specification used for 2D simulations.

<b>Cluster type</b>	N type or P type
<b>Cluster size</b>	20nm x 20nm
<b>Shape</b>	Rectangular
<b>Cluster density</b>	$10^{19} \text{ cm}^{-3}$
<b>Activation energy</b>	0.5eV

### 5.3. Simulation results

Figure 135 shows the modeled I-V characteristic of accessed transistor. The leakage current density for the pristine device is given for gate bias 0V is  $6.48 \times 10^{-14} \text{ A}/\mu\text{m}$ . This will be the reference current used to compare with enhanced leakage current induced by irradiation. Since we apply 2D modeling, the current depends on the thickness of the device. This is the reason why all current will be expressed as  $\text{A}/\mu\text{m}$ .

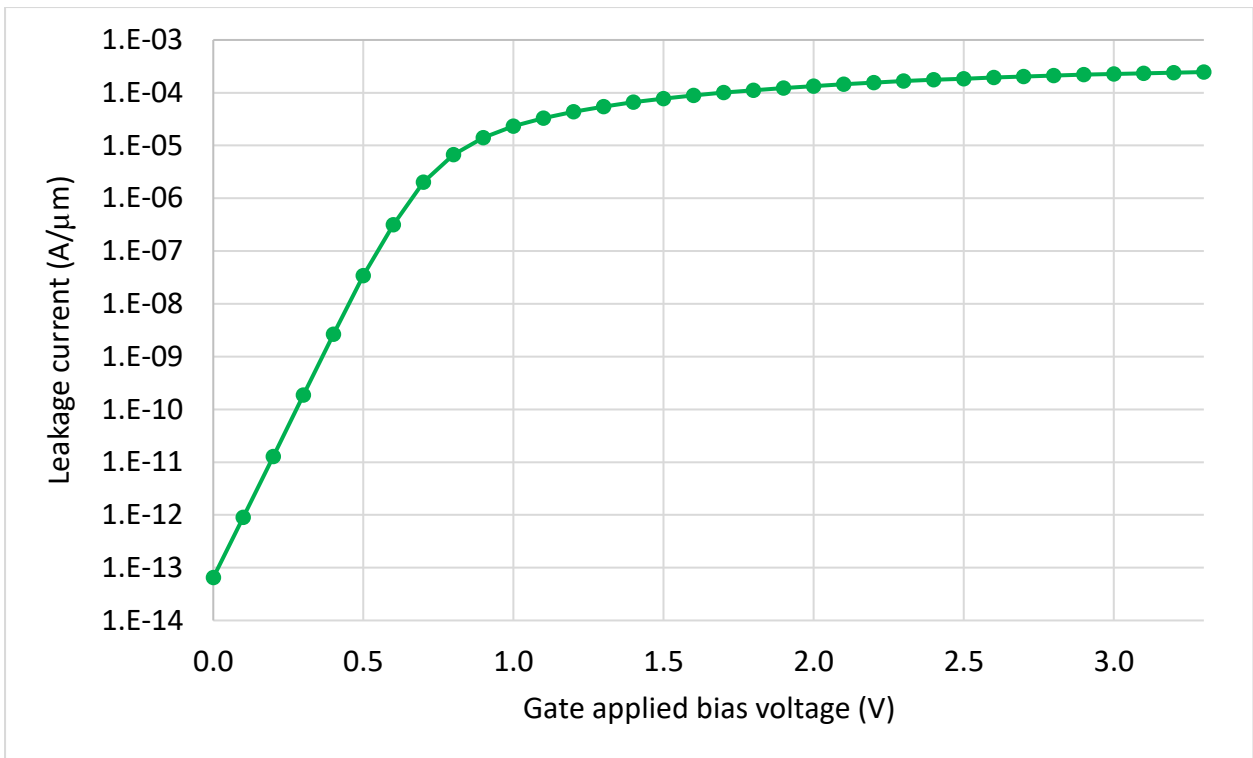


Figure 135: I-V characteristic of pristine device

For the next results, each simulated leakage current (each point on curves) required between 15 minutes and 2 hours of CPU time.

### 5.3.1. Simulation result of only single defects cluster

1D modeling of storage node PN junction showed that the effect of the cluster strongly depends on its position. In this part we will show the effect of the cluster on a 2D MOS transistor as a function of its position along x and y axis. Table 2 are cluster position range used in 2D simulation.

Table 22: Cluster position used to 2D simulation

<b>Cluster x position - Distance respect to the left edge of device</b>	0 – 1.1 μm
<b>Cluster y position - Distance from the center of cluster to Si/SiO<sub>2</sub> interface</b>	0.01 – 0.3 μm

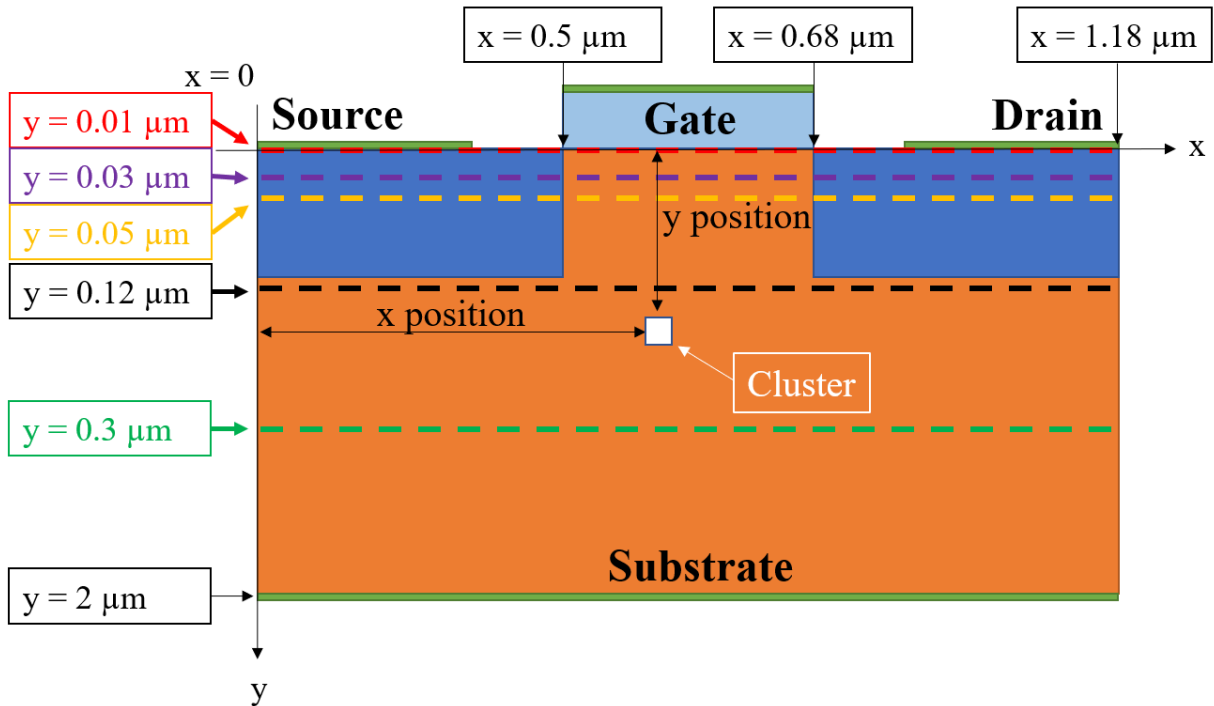


Figure 136: Cluster position illustrate on the 2D model of access transistor in x and y axis.

The illustration of cluster relative position inside device is presented in Figure 136. X position is distance from left side of device to the center of cluster, while y position is the distance from gate/channel interface to the center of cluster. In this study, x position will range from  $x=0\mu\text{m}$  to  $x = 1.18\mu\text{m}$ . There are several places for cluster that is chose because of its special location such as: inside substrate position:  $y = 0.3\mu\text{m}$ ; at the edge of depletion region:  $y = 0.12\mu\text{m}$ ; two position within depletion region  $y = 0.03\mu\text{m}$  and  $y = 0.05\mu\text{m}$ ; finally, right below the gate/channel interface  $y = 0.01\mu\text{m}$ .

Figure 137 and Figure 138 show the leakage current corresponding to the horizontal location of the cluster (x axis) for n type and p type. Each curve of the graph displays the leakage current for a vertical distance from the interface to the cluster (y axis).

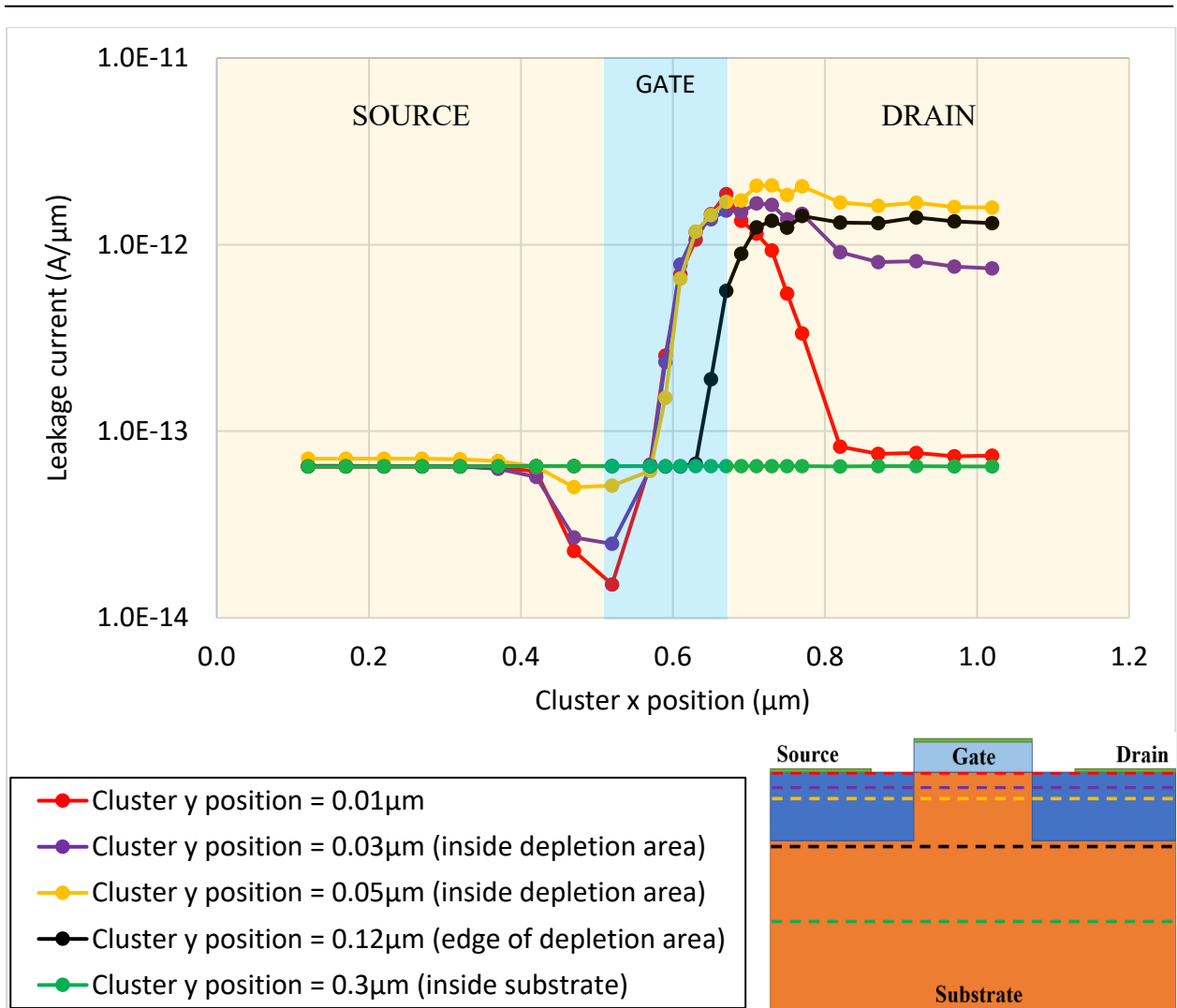


Figure 137: Leakage current as the position of defect cluster - n type cluster. Each line color corresponding to the y position on device model as showed in the bottom right corner.

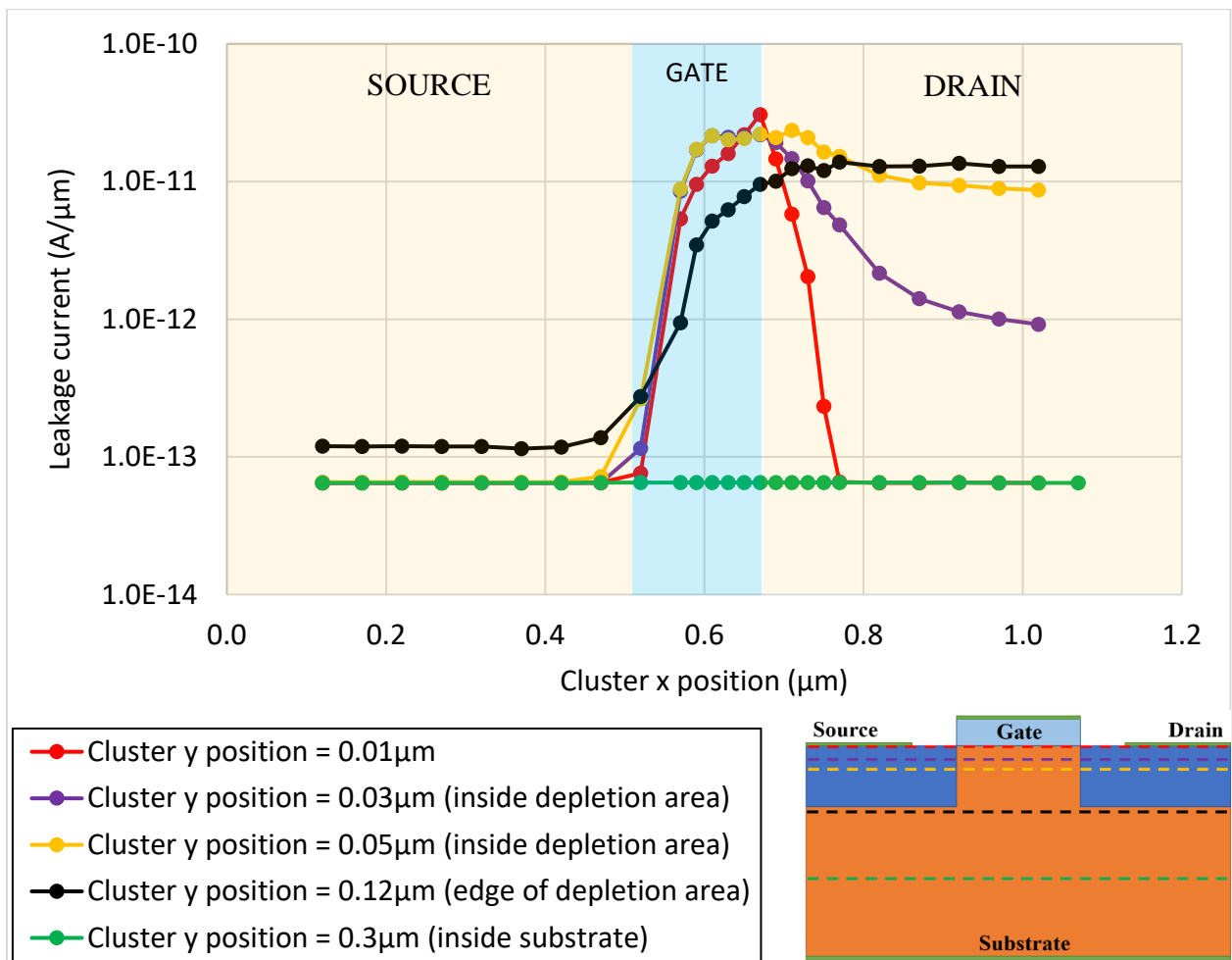


Figure 138: Leakage current as the position of defect cluster - p type cluster. Each line color corresponding to the y position on device model as showed in the bottom right corner.

The carrier generation is more efficient for p-type than for n-type cluster. This maximum leakage current is 16 times higher for p-type cluster than for n-type cluster. This will be explained when analyzing the effect of activation energy of cluster on the leakage current.

For both n-type and p-type cluster, we saw similar results: when cluster was positioned deep inside substrate, there was no effect on leakage current, similarly when cluster was at source region; when cluster was positioned close the channel, leakage current started to increase and reached maximum right under gate, next to drain region.

From results in Figure 137 and Figure 138 a sensitive region of defects cluster can be estimated as seen in Figure 139.

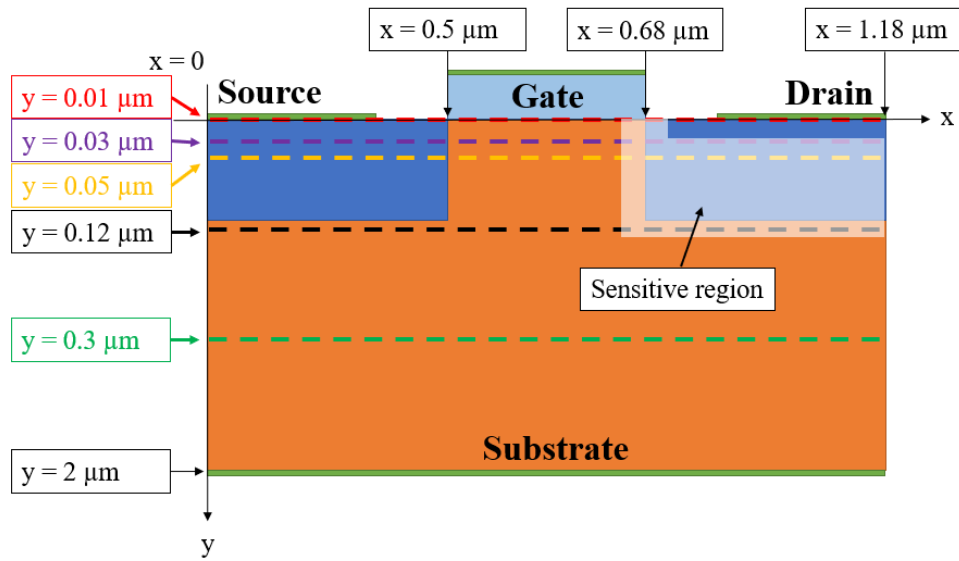


Figure 139: Estimated sensitive region for defects cluster within the device in order to increase leakage current.

Figure 140 gives the electric field as a function of x position for y position of clusters. It appears that the leakage current generated by the cluster is strongly related to the magnitude of the electric field.

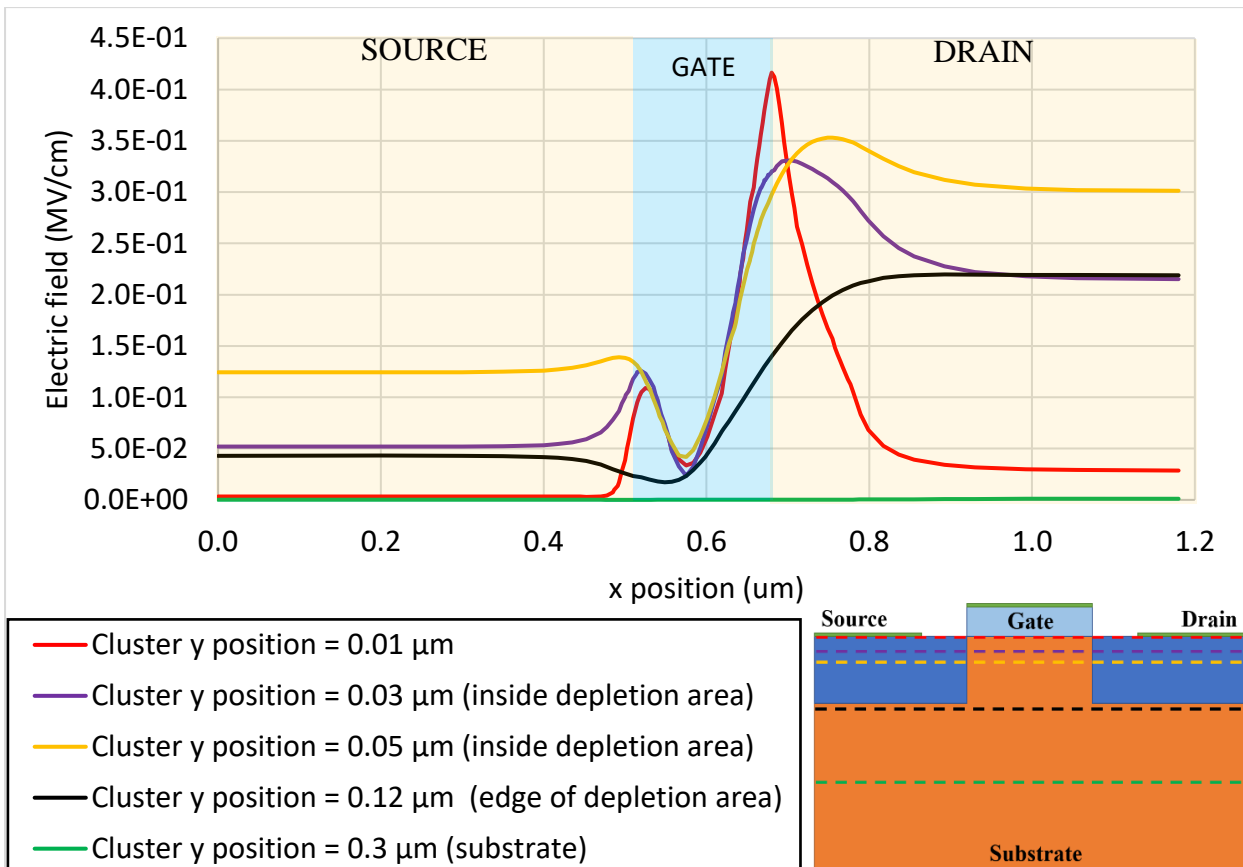


Figure 140: Electric field along x axis of the device.

To highlight this, Figure 137, 138 and 139 shows on the same chart the leakage current and the electric field for y position 0.01, 0.03 and 0.05  $\mu\text{m}$ .

The highest leakage current appears at position  $x = 0.68 \mu\text{m}$ ,  $y = 0.01 \mu\text{m}$  for which the electric field is the highest. This point is at the right edge of the oxide-silicon interface.

On these curves (figures 137-139), we can observe a shift between the electric field and the leakage current induced by the cluster. The electric field displayed was calculated for pristine device and does not take into account the electrostatic charge trapped in the cluster. This explains the shift to the left observed on these figures.

With these charts, the relationship between leakage current and electric field is obvious.

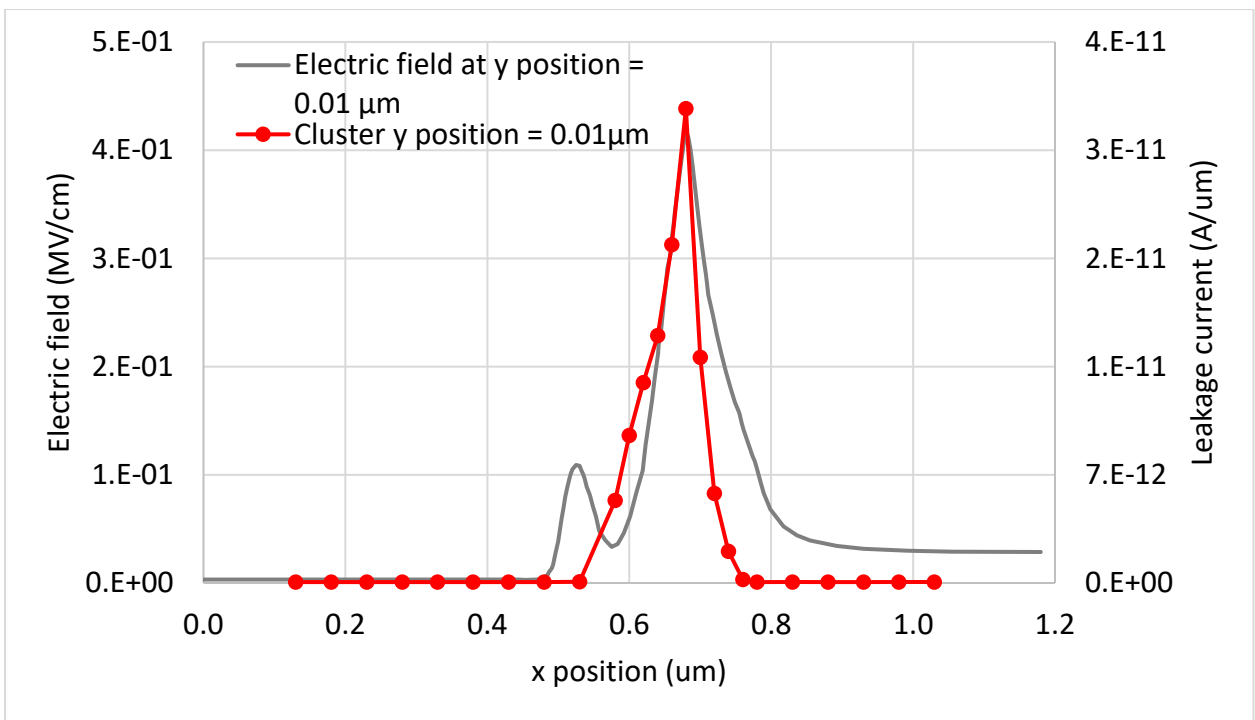


Figure 141: Electric field on pristine device and leakage current with p-cluster along x axis at  $y = 0.01\mu\text{m}$ .

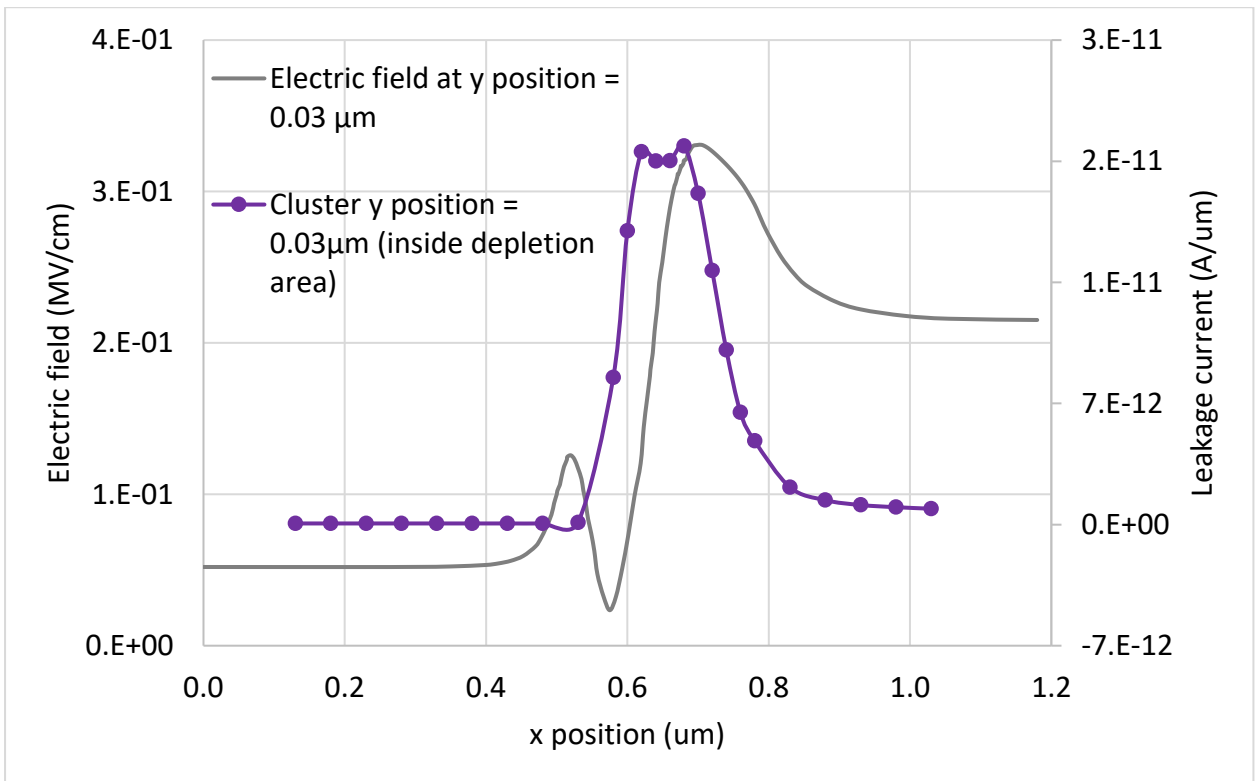


Figure 142: Electric field on pristine device and leakage current with p-cluster along x axis at  $y = 0.03\mu\text{m}$



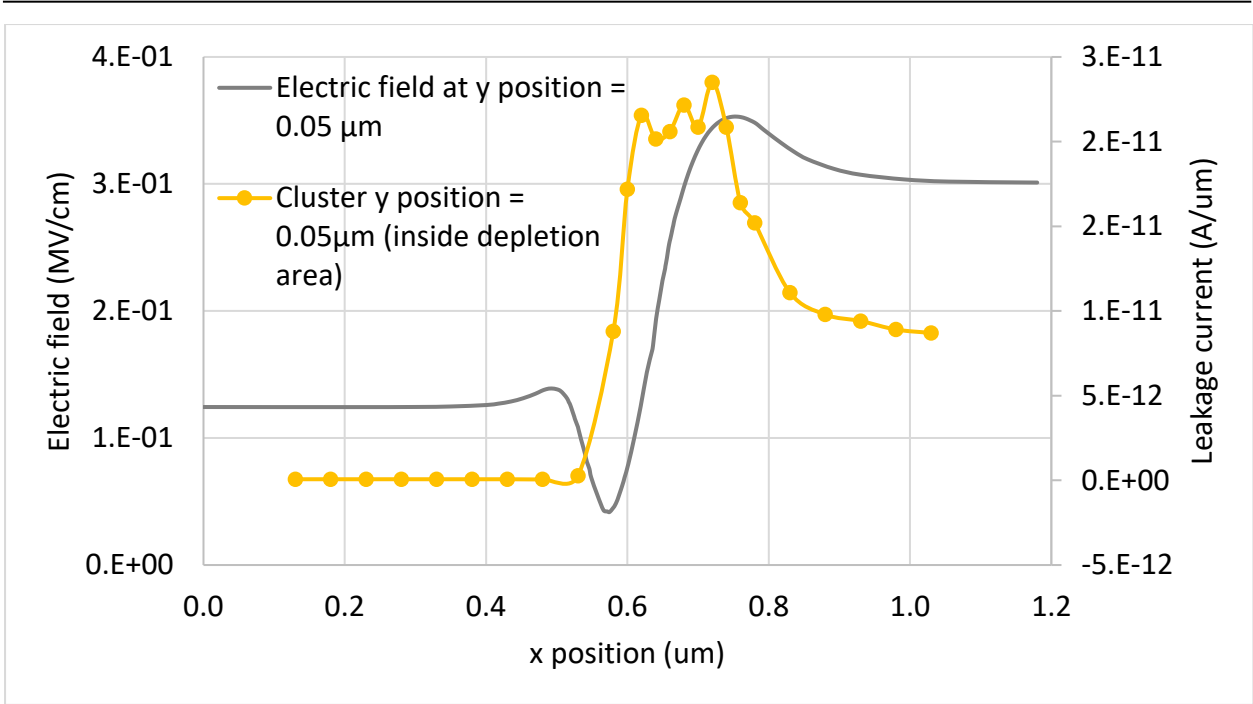


Figure 143: Electric field on pristine device and leakage current with p-cluster along x axis at  $y = 0.05\mu\text{m}$ .

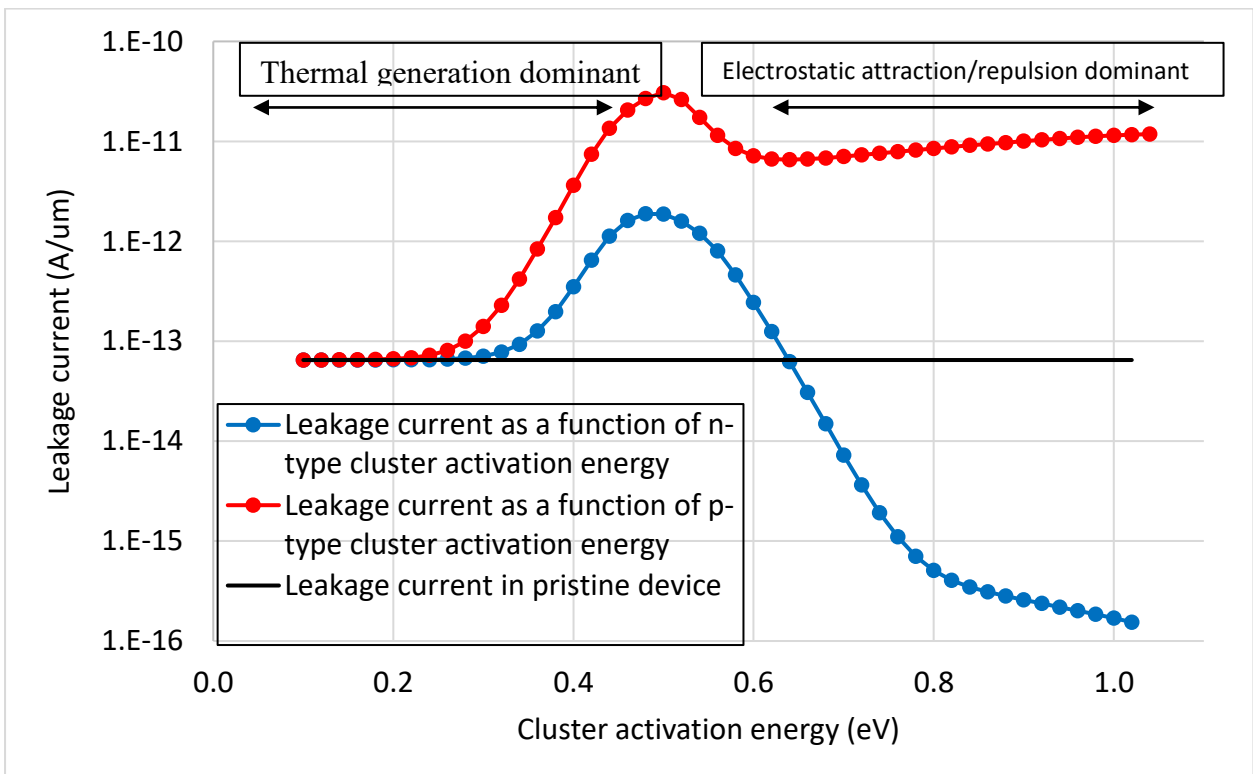


Figure 144: Leakage current as the function of cluster activation energy: n-type (blue), p-type (red) and black line indicates leakage current in pristine device.

In Figure 144, the leakage currents as a function of cluster activation energies are presented and the black line displays the leakage current of a pristine device. It shows clearly that when

activation energy of cluster is at 0.5eV, the leakage current is highest for both n-type and p-type cluster.

Analyze of modeling shows that the leakage current induced by p-cluster (respectively n-cluster) is the sum of 2 components:

- The thermal generation of electron-hole pairs
- The increase (respectively decrease) of free electron around the cluster by electrostatic attraction of the positive (respectively repulsion of negative) charges trapped inside the cluster.

The thermal generation can be explained by the four phenomena that occur in cluster we saw previously: capture or free carriers, thermal generation of trapped carriers, thermal generation of carriers of opposite type and recombination of trapped carriers. In order to generate leakage currents two phenomena must be activated: the thermal emission of carriers of opposite types and the thermal re-emission of trapped carriers. Considering a p-type trap, Figure 145 shows that  $E_a$  (activation energy) drives the thermal re-emission of trapped carriers and while the difference  $E_g$  (gap energy) –  $E_a$  drives the thermal emission of carriers of opposite type.

The mechanisms for electron-hole pairs generation include:

- a. From an empty trap an electron is thermally emitted into the conduction band. The rate of electron generation depends on the difference  $E_g - E_a$ . After electron emission, the trap is left with a hole.
- b. The trapped hole is thermally emitted in the valence band. The rate of holes generation depends on activation energy  $E_a$ . After hole emission the trap is empty.
- c. The free electrons and holes move according to the electric field. The process then can restart.

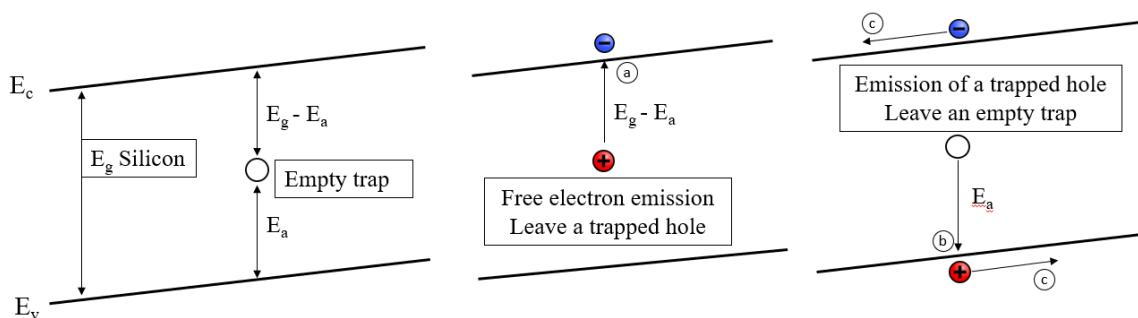


Figure 145: Mechanisms responsible for electron hole pairs generation with presence of traps.

The leakage current is maximum when these two effects are maximum. This occurs when the activation energy is around the middle of the band gap.

Comparison of p-cluster and n-cluster modeling shows that for p-cluster in Figure 145 the trapped charge is positive and attract free electron at the interface while for n-cluster, the

trapped charge is negative and push back electron from the interface. This explain why the highest leakage current induced by p-cluster is 16 times higher than the one induced by n-cluster.

For activation energy higher than 0.7eV, the leakage current of the p-cluster is higher than the one of the pristine device (black line) while for n-cluster it is lower than the one of the pristine device. For these energies, the thermal reemission of trapped carriers is negligible and trap are filled. Thus, the thermal generation disappears and the change of the leakage current is only driven by the electrostatic effect.

Figure 146 shows a crosscut of the free electron density for p-cluster and n-cluster along the interface for a 1eV activation energy. The free electron density is decreased around the cluster by the negative trapped charge for a n-cluster while it is increased for a p-cluster. This explains the decrease of the leakage current for the n-cluster compared to the pristine device and the increase for the p-cluster compared to the pristine device.

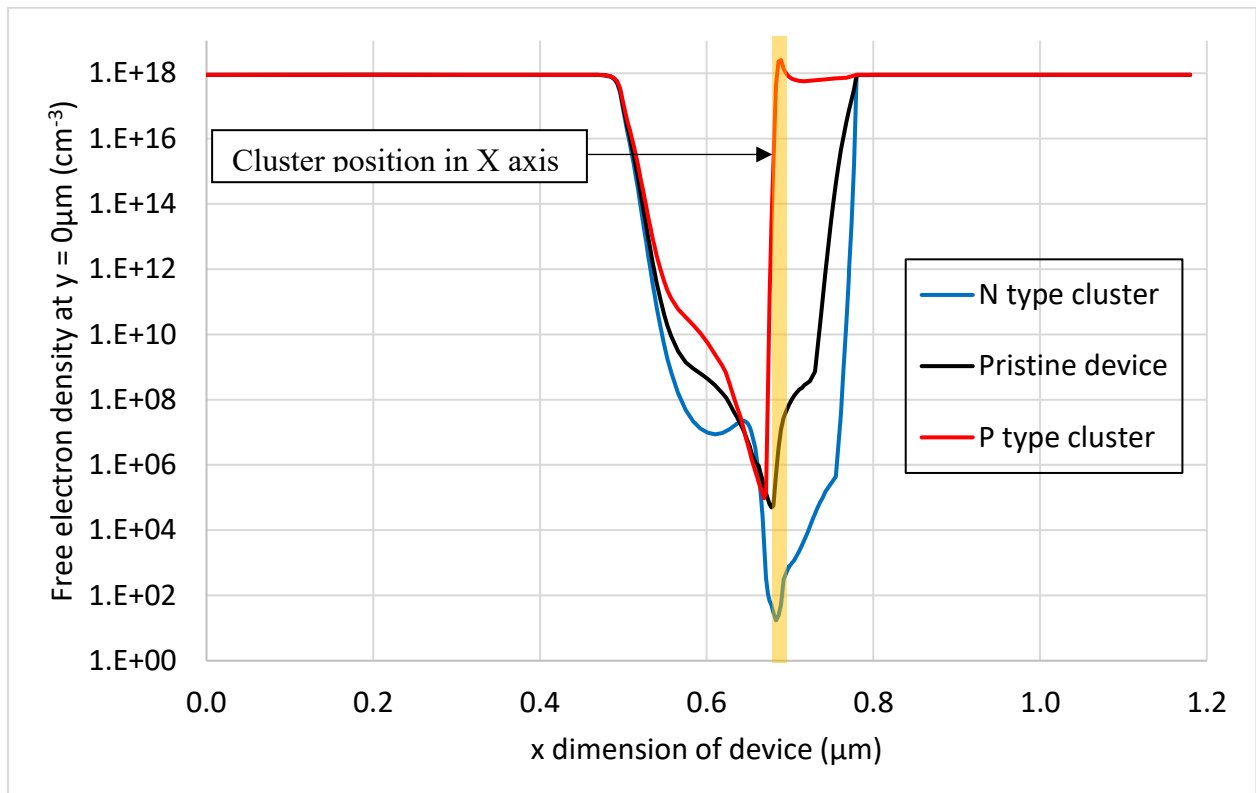


Figure 146: Cross section of free electron density at  $y = 0\mu\text{m}$  of: pristine device (black), device with n-cluster (blue) and device with p-cluster (red) at highest leakage current position. At 1eV activation energy.

### 5.3.2. Simulation results of only interface traps

One of the main contributions of TID effect on MOSFET devices is interface traps building up. In this section, interface traps are introduced to the pristine model of the device to analyze the impact of on the leakage current. The interface traps are represented as a homogeneously distributed layer between gate oxide and silicon.

In order to simulate the effect of interface traps accurately, reasonable values of traps parameters need to be defined beforehand. Those are density, activation energy and capture cross section.

- In pristine devices, the interface traps density  $D_{it}$  can stay at around  $10^{10} \text{ cm}^{-2}$  depend on the technology processing [157]. Under irradiation,  $D_{it}$  can range from  $10^{10}$  to  $10^{12} \text{ cm}^{-2}$  and is absorbed dose dependent. In this works, different values of interface traps density in the same range are used for simulations.
- Nature of interface traps (n-type or p-type) depend on is position in the bandgap. Traps in the lower portion can donate an electron (donor type) to silicon to become positive charged if the Fermi level at the interface is below the trap energy level. On the contrary, traps in the upper portion of the band gap can accept (acceptor type) an electron from the silicon and become negative charged if the Fermi level at the interface is above the trap energy level. In this study, target of simulation is acceptor type traps (p type) while no effect of donor type (n type) traps on the leakage current has been seen.
- Traps activation energy stays within the conduction band of silicon. Their energy levels are measure from the valence band, for example energy at  $E_{traps} = 0.1 \text{ eV}$  means the trap locate closer to valence band. In order to investigate the influence of interface traps activation energy, multiple simulations are performed with energy ranging from  $0.1 \text{ eV}$  to  $1.05 \text{ eV}$ .

Figure 147 shows the leakage current as the function of interface traps activation energy with traps density of  $2 \times 10^{11} \text{ cm}^{-2}$ .

As for cluster, the analyze of modeling shows that the leakage current induced by interface traps has 2 main origins:

- The thermal generation of electron-hole pairs
- The increase of free electron at the interface by electrostatic attraction of the positive charge trapped at the interface.

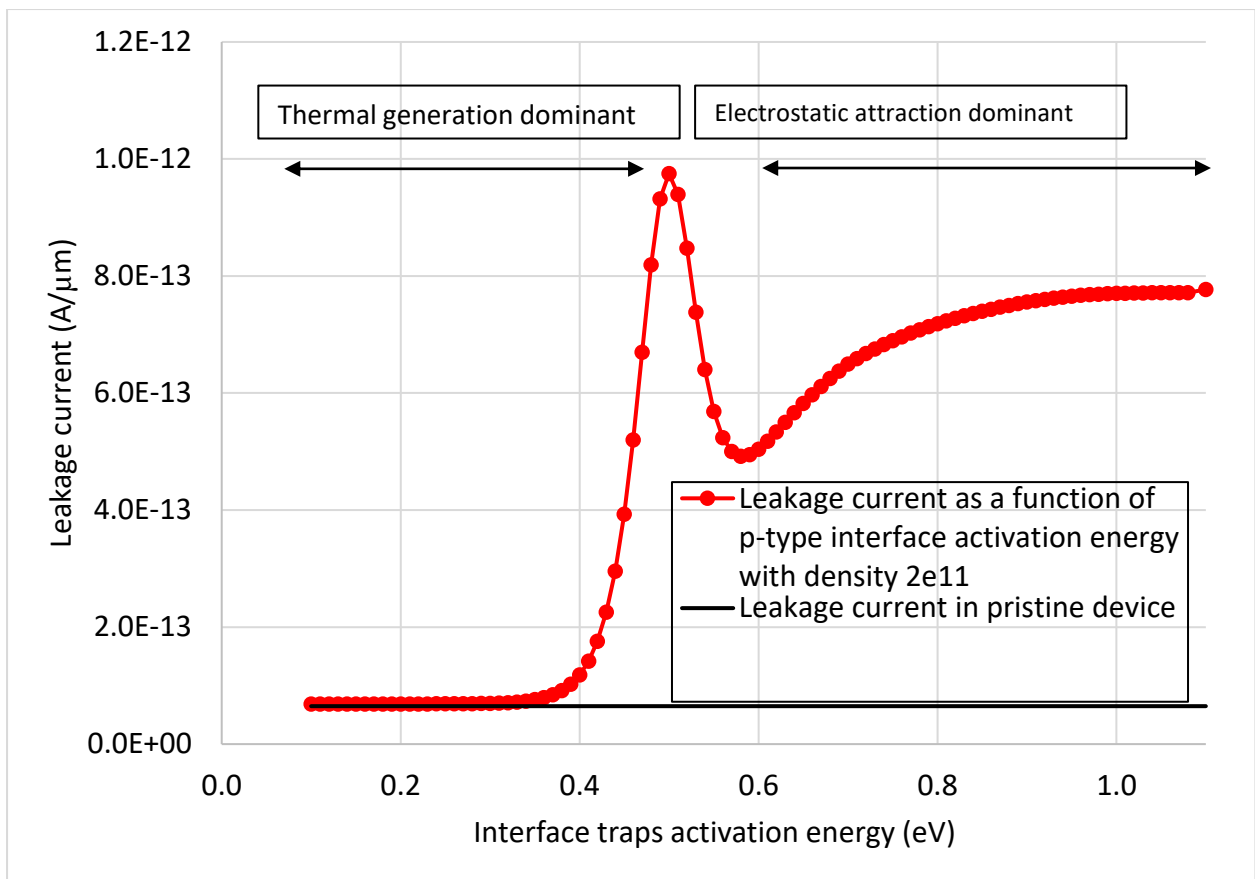


Figure 147: Leakage current as the function of p type interface traps activation energy with density of  $2 \times 10^{11} \text{ cm}^{-2}$ . Black line indicates leakage current on pristine device.

At low activation energy (from 0.1 to 0.4eV), holes captured by traps are quickly thermally reemitted in the valence band. Furthermore, the emission of electron from free traps is not possible because the energy between the trap and the conduction band is too high. Thus, there is no significant thermal generation of pairs and no electrostatic attraction of free electron since traps are nearly empty.

For middle activation energies (from 0.4 to 0.6eV) the thermal reemission of pairs is reduced but still efficient and the emission of free electron from empty traps becomes significant since the energy between the trap and the conduction band is reduced. Then, the thermal generation of electron-hole pairs is maximized. For high activation energy (from 0.6eV to 1.1eV) the activation energy becomes too high and the thermal reemission of trapped holes is negligible. The traps are filled with holes and the emission of electron from free traps no more exists. The increase of the leakage current is induced by the positive trapped charge that attract free electrons at the interface.

Figure 148 shows the leakage current for density of interface states ranging from  $10^{10}$  to  $2 \times 10^{12} \text{ cm}^{-2}$  for 2 activation energies: 0.5eV and 1eV. It is usually admitted that p-type activation range ceil around 0.6eV energy. However, in this study, this activation energy is used to study the electrostatic effect on the device.

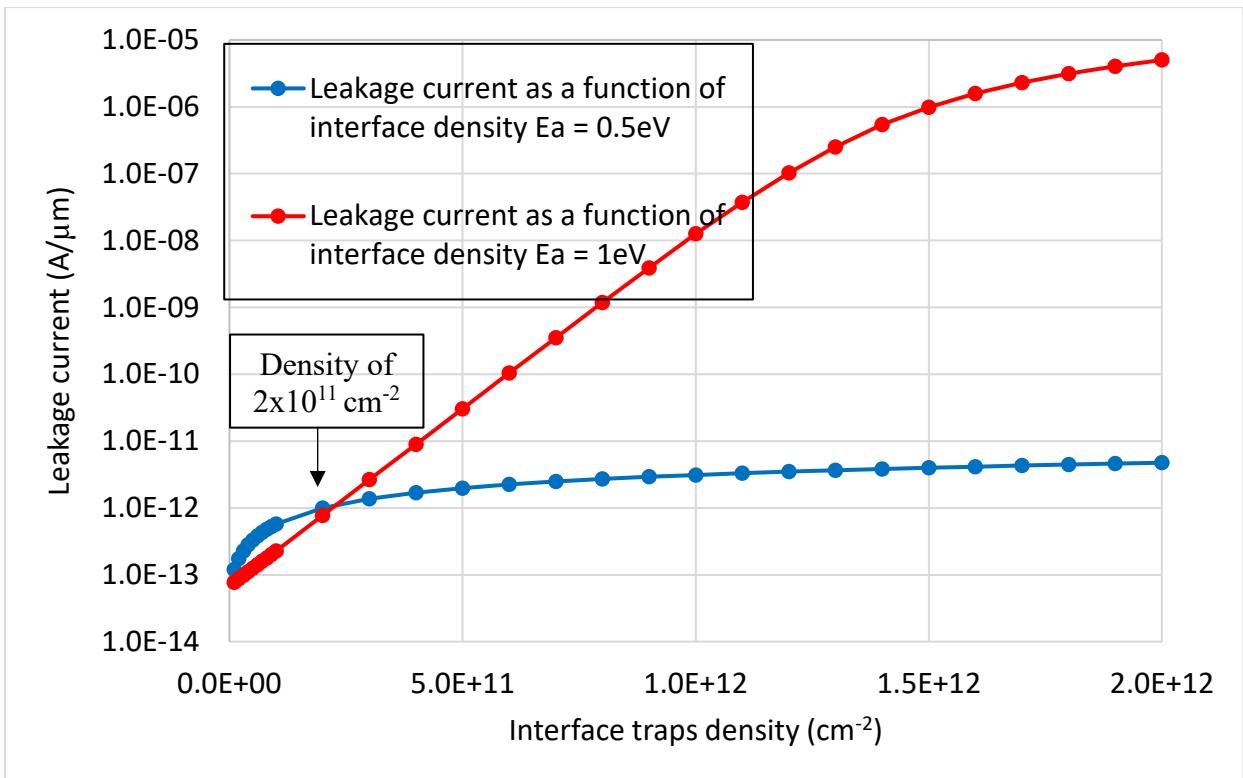


Figure 148: Leakage current as function of interface traps density with activation energy at 0.5eV (blue) and 1eV (red).

It appears that below an interface traps density of  $2 \times 10^{11} \text{ cm}^{-2}$ , the thermal generation is dominant since the current is higher for 0.5 eV than for 1eV.

Above  $2 \times 10^{11} \text{ cm}^{-2}$ , the electrostatic attraction of free electron is dominant since the current is higher for 1 eV than for 0.5eV.

For the following modelings, we will keep two set of values for interface traps:

- density of  $2 \times 10^{11} \text{ cm}^{-2}$  and activation energy of 0.5 eV
- density of  $2 \times 10^{11} \text{ cm}^{-2}$  and activation energy of 1 eV

Table 23: Leakage current summary table for interface traps activation energy ( $E_a$ ) and interface traps density ( $D_{it}$ ).

	Interface density ( $2 \times 10^{11} \text{ cm}^{-2}$ )	Interface density ( $2 \times 10^{12} \text{ cm}^{-2}$ )
<b><math>E_a = 0.5\text{eV}</math></b>	$9.9 \times 10^{-12} \text{ A}/\mu\text{m}$	$4.7 \times 10^{-12} \text{ A}/\mu\text{m}$
<b><math>E_a = 1\text{eV}</math></b>	$7.7 \times 10^{-13} \text{ A}/\mu\text{m}$	$5.0 \times 10^{-6} \text{ A}/\mu\text{m}$
<b>Pristine device</b>	$6.5 \times 10^{-14} \text{ A}/\mu\text{m}$	

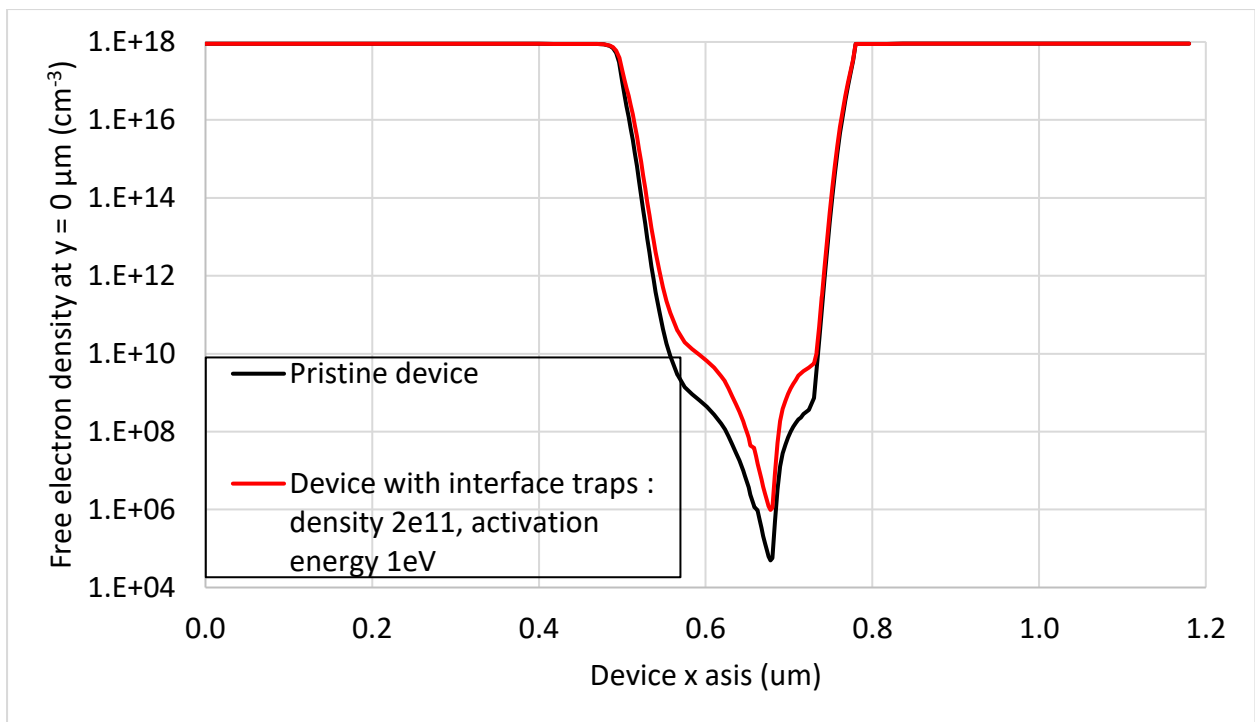


Figure 149: Free electron density across x axis of the device at  $y = 0 \mu\text{m}$ . Black line indicates pristine device. Red line is device with interface traps density of  $2e11$  and activation energy of  $1eV$ .

Figure 149 shows the free electron density along x axis at the position  $y = 0\mu\text{m}$  for pristine device and for device with interface traps density of  $2 \times 10^{11} \text{ cm}^{-3}$  and activation energy of  $1\text{eV}$ . This free electron density is responsible for the leakage current.

Under the gate, the free minimum electron density is around  $5 \times 10^4 \text{ cm}^{-3}$  for the pristine device and  $9.8 \times 10^5 \text{ cm}^{-3}$  for the device with interface traps  $E_a = 1\text{eV}$ . The ratio between these 2 values is around 20 and the ratio between leakage current of 2 models ( $6.48 \times 10^{-14}$  and  $7.7 \times 10^{-13} \text{ A}/\mu\text{m}$ ) is around 12. These two ratios show the link between the leakage current increase and the electrostatic attraction of the trapped charge at the interface for  $E_a = 1\text{eV}$ . They are not exactly the same because the ratio of leakage current depends on all free electron density along the interface and not only the minimum value.

### 5.3.3. Simulation results of only volume traps under influence from single energetic particle (Proton and Xe)

From cluster simulation, we saw that the highest leakage induced by the cluster appears for position  $x = 0.68\mu\text{m}$ ,  $y = 0.01\mu\text{m}$ . This position is selected for impact point of energetic particles.

In this part, we consider that a particle only generates electron-hole pairs in the gate oxide (illustrated in Figure 150). Because of low activation energy of n-type traps (typically  $0.8 \text{ eV}$ ), electrons are quickly removed from the oxide. At the opposite, p-type traps have a high activation energy (typically  $1.4 \text{ eV}$ ) and holes can stay trapped for years in the oxide. Thus, after an ion crossing the oxide will contain a positive charge. This positive charge, by

electrostatic attraction, increases the free electron density at the interface and thus increases the leakage current. This is usually called a microdose because it is equivalent to a Total Ionizing Dose but deposited at a very localized place.

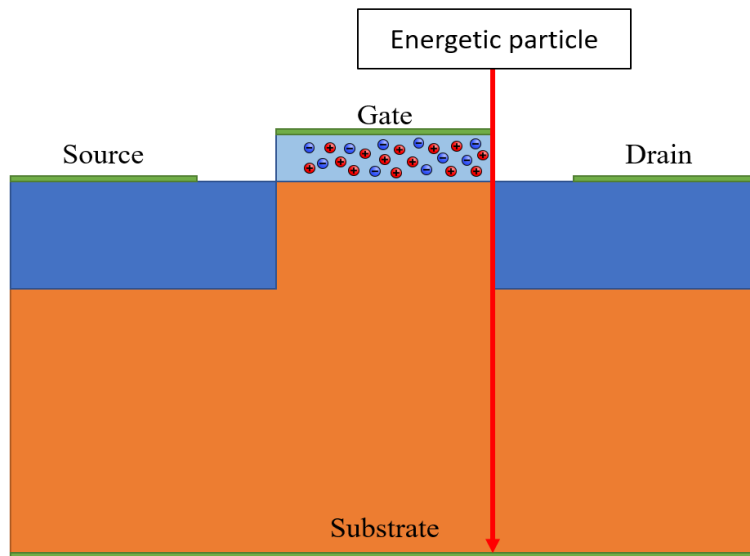


Figure 150: Trajectory of energetic particle used in modeling.

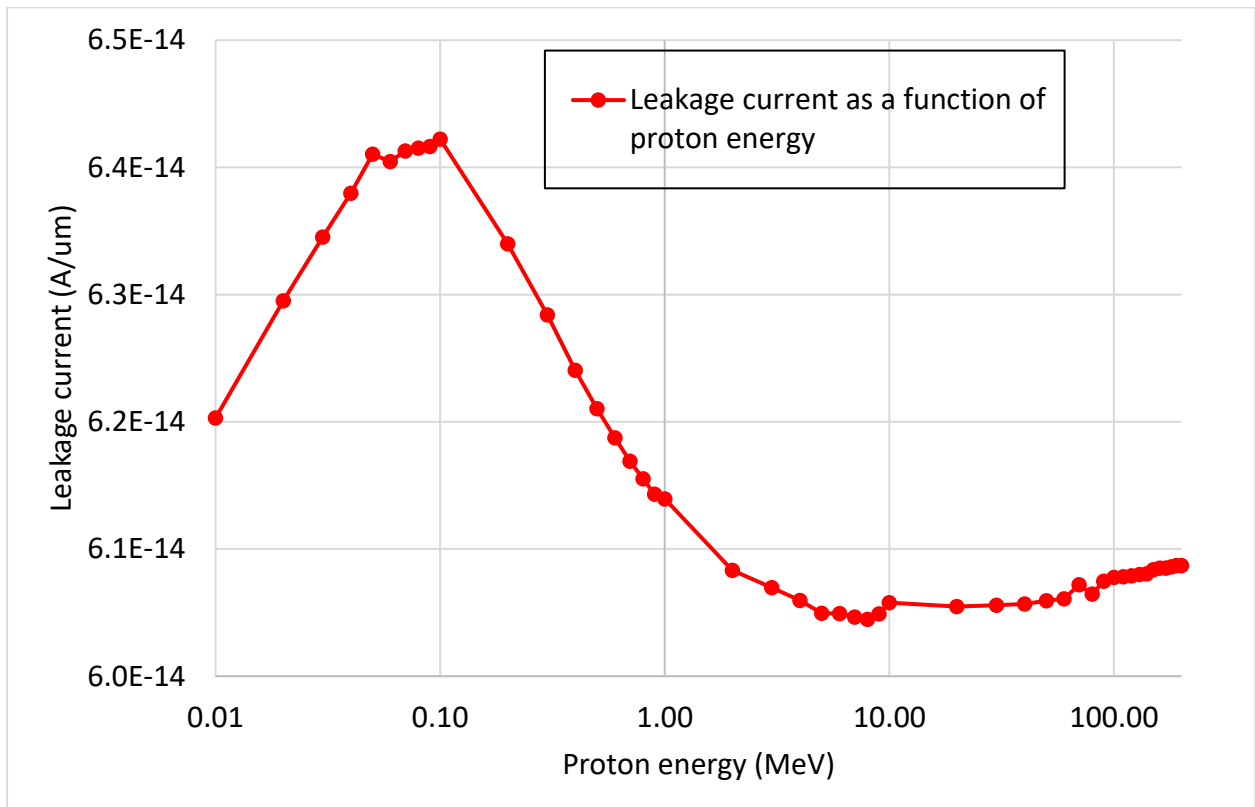


Figure 151: Leakage current as a function of proton energy.

Figure 151 shows the leakage current after a microdose deposited by a proton as a function of the proton energy. The leakage current is the same than for the pristine device. The initial



Linear Energy Transfer (LET) of the proton (highest modeled value: 150 keV/ $\mu\text{m}$ ) is too low, whatever its energy is, and the positive charge deposited in the oxide do not change the free electron density in the channel.

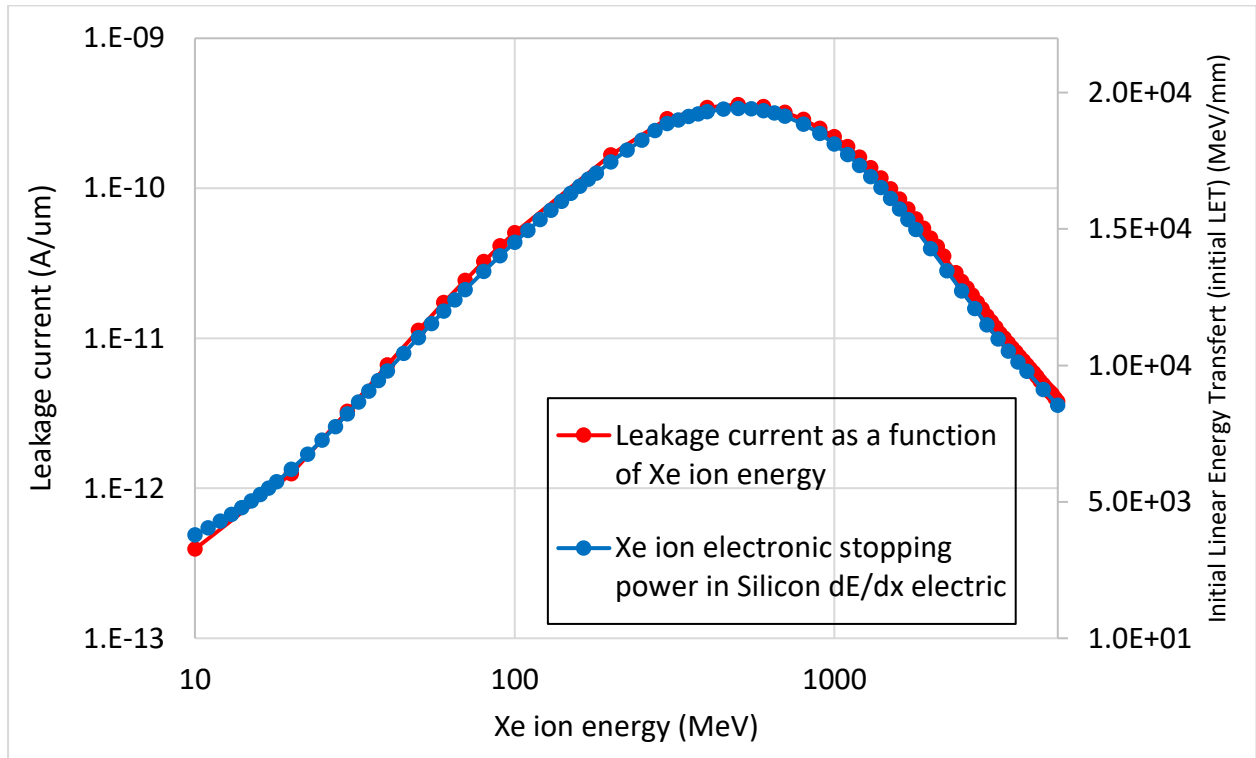


Figure 152: Leakage current as a function of Xe ion energy and corresponding initial LET from SRIM2013.

Figure 152 shows the leakage current after a microdose deposited by a Xe132 ion (blue curve) and the initial LET of the ion (red curve) as a function of the ion energy. We observe a high increase of the leakage current compared to the pristine device. The initial Linear Energy Transfer (LET) of the Xe132 ion (highest modeled value: 20 MeV/ $\mu\text{m}$ ) is much higher than the proton one. Then the positive charge deposited in the oxide increases significantly the free electron density in the channel.

The highest leakage current is  $3.62 \times 10^{-10}$  A/ $\mu\text{m}$  for a 500 MeV initial energy. The leakage current for the energy used in facilities (3.8 GeV) is  $7.53 \times 10^{-12}$  A/ $\mu\text{m}$  that is to say more than 40 times lower than the one for 500 MeV.

Furthermore, comparison between LET using a linear scale and leakage current using a logarithmic scale clearly shows that leakage current varies exponentially depending on the LET.

### 5.3.4. Combined effects simulations

Each ion impact generates a microdose and creates interface traps. The defects cluster has only a probability of creation since the ion must hit an atom to generate displacement damages.

In this part we will analyze the combination of the three phenomena created by an ion: cluster defects, interface traps, volume traps. As a first step, we could think that the leakage current induced by combined phenomena will be the sum of the leakage current induced by phenomena modeled separately. We will see that, because of electrostatic interactions between charges, an enhancement or a reduction of the sum of leakage current can be observed depending on the modeled effects.

#### 5.3.4.1. Combined effects between interface traps and defects cluster

In this section, the combined effect between interface traps and cluster is examined. In Figure 153, leakage current density as the function of interface traps density coupled with cluster stationary at highest leakage current position is presented. The red curve is modeled with interface traps activation energy of 0.5eV, while the blue one is with 1eV.

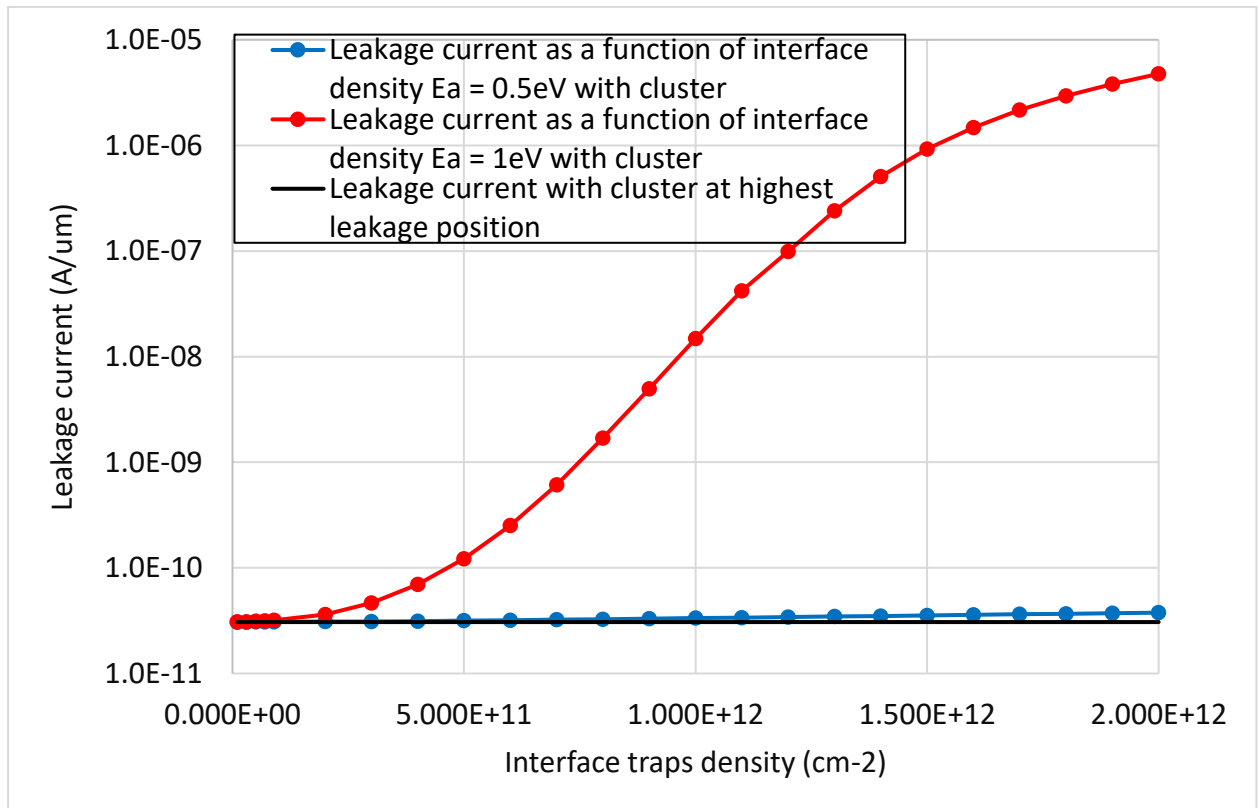


Figure 153: Leakage current density as function of interface traps density with activation energy  $E_a = 0.5\text{eV}$  (red) and  $E_a = 1\text{eV}$  (red) with cluster integrated. Black line indicates the leakage current of cluster at highest leakage position.

As mentioned previously, the cluster is p-type, at position  $x=0.68\ \mu\text{m}$ ,  $y=0.01\ \mu\text{m}$  with density  $10^{19}\ \text{cm}^{-3}$  and activation energy of 0.5 eV.

The Table 24 shows the leakage current density for cluster and interface traps alone, the sum of these values and the leakage current for combined effect. This is calculated for the value of the interface trap density of  $2 \times 10^{11}\ \text{cm}^{-2}$ .

Table 24: Leakage current ( $A/\mu m$ ) for singular and combined phenomena: cluster defects, interface traps ( $E_a$ : activation energy of interface traps and  $D_{it}$  density  $2 \times 10^{11} \text{ cm}^{-2}$ ).

	Defects cluster only	Interface traps only	Sum of effects alone ( $I_{sum}$ )	Combined effects ( $I_{combined}$ )	Ratio $I_{combined}/I_{sum}$
$E_a = 0.5 \text{ eV}$	$3.07 \times 10^{-11}$	$1 \times 10^{-12}$	$3.17 \times 10^{-11}$	$3.097 \times 10^{-11}$	0.98
$E_a = 1 \text{ eV}$	$3.07 \times 10^{-11}$	$7.7 \times 10^{-13}$	$3.147 \times 10^{-11}$	$3.631 \times 10^{-11}$	1.15

For activation energy of 0.5 eV and 1eV, an amplification of the leakage current appears (0.98 and 1.15). It is so small that it can be neglected. These small changes can be induced by differences in the mesh.

#### 5.3.4.2. Combined effects between volume traps (under influence of Proton and Xe ion) and defects cluster

In this section, the combined effect between Volume traps under fluence of Proton/Xe and cluster at the highest leakage position ( $x=0.68 \mu m$  and  $y=0.01 \mu m$ ) is examined.

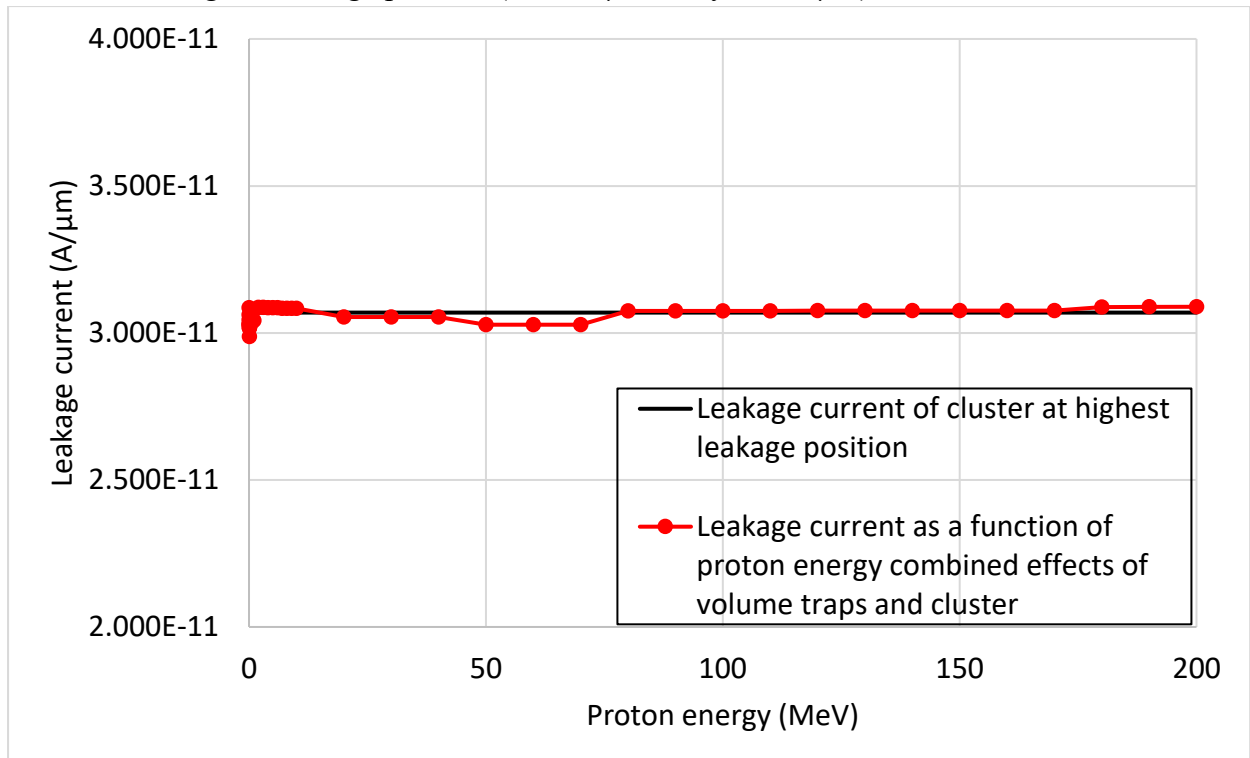


Figure 154: Leakage current as the function of proton energy with cluster integrated at highest leakage position (Combined effects of volume traps induced by proton beam and cluster).

Figure 154 shows this combined effect as a function of proton energy up to 300 MeV. Compared to the effect of cluster only, volume traps under fluence of proton has almost no effect on the leakage current. The small changes that are observed are probably induced by fluctuations of the distribution of the mesh. In contrast, the Xe ion significantly increases the leakage current as shown in Figure 155. Highest leakage current is recorded at 500 MeV which is coherent with stopping power provided previously.

Table 25: Leakage current ( $A/\mu m$ ) for singular and combined phenomena: cluster defects and 500 MeV Xe ion.

Defects cluster only	Volume traps only with Xe at 500 MeV	Sum of effects alone ( $I_{sum}$ )	Combined effects ( $I_{combined}$ )	Ratio $I_{combined}/I_{sum}$
$3.07 \times 10^{-11}$	$3.62 \times 10^{-10}$	$3.93 \times 10^{-10}$	$4.79 \times 10^{-10}$	1.23

As shown in Table 25, there is a moderate amplification factor for this combined effect: 1.23

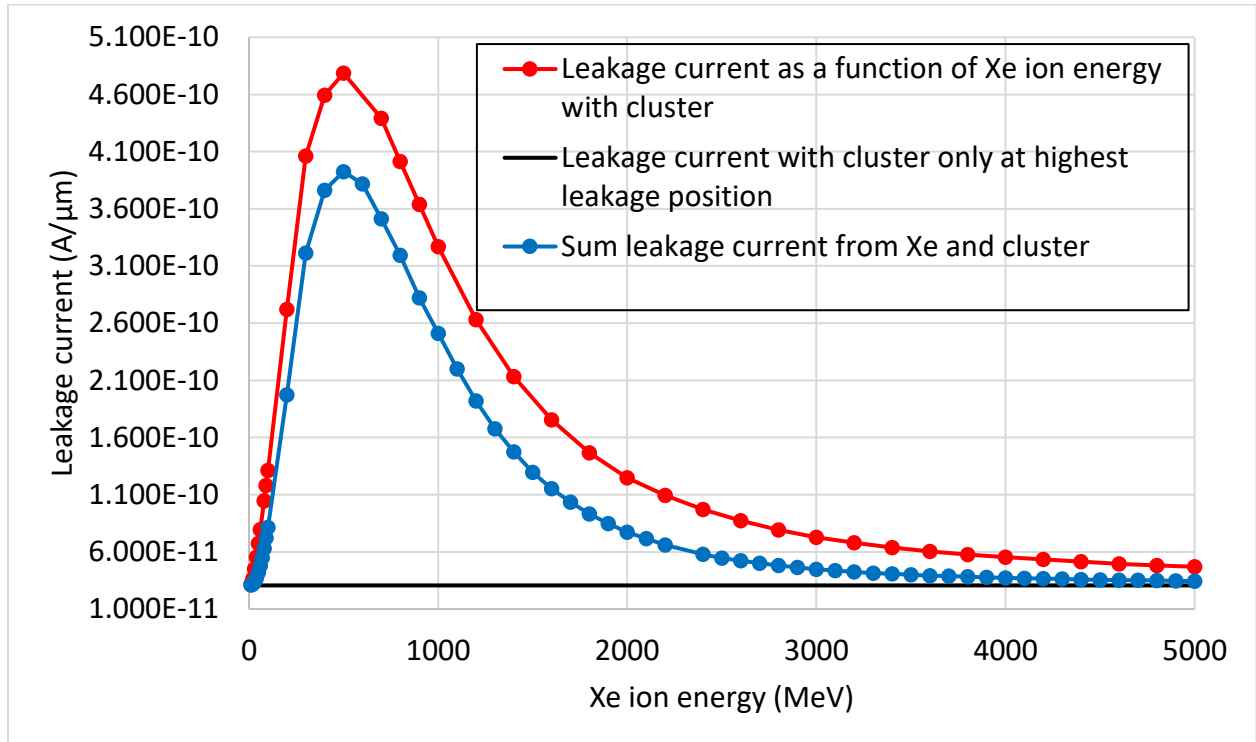


Figure 155: Leakage current as the function of Xe ion energy with cluster integrated at highest leakage position – red curve (Combined effects of volume traps induced by Xe ion beam and cluster). Blue line is the mathematical leakage current sum from Xe ion and Cluster separately. Black line indicates leakage current with cluster only.

#### 5.3.4.3. Combined effects between volume traps (under influence of Proton and Xe ion) and interface traps

In this section, the combined effect between Volume traps under fluence of Proton/Xe and interface traps for density  $2 \times 10^{11} \text{ cm}^{-2}$  and activation energy of 0.5eV and 1eV is examined.

Figure 156 shows this combined effect as a function of proton energy up to 200 MeV. Compared to the effect of interface trap only for 0.5eV and 1eV, volume traps under fluence of proton has no effect on the leakage current.

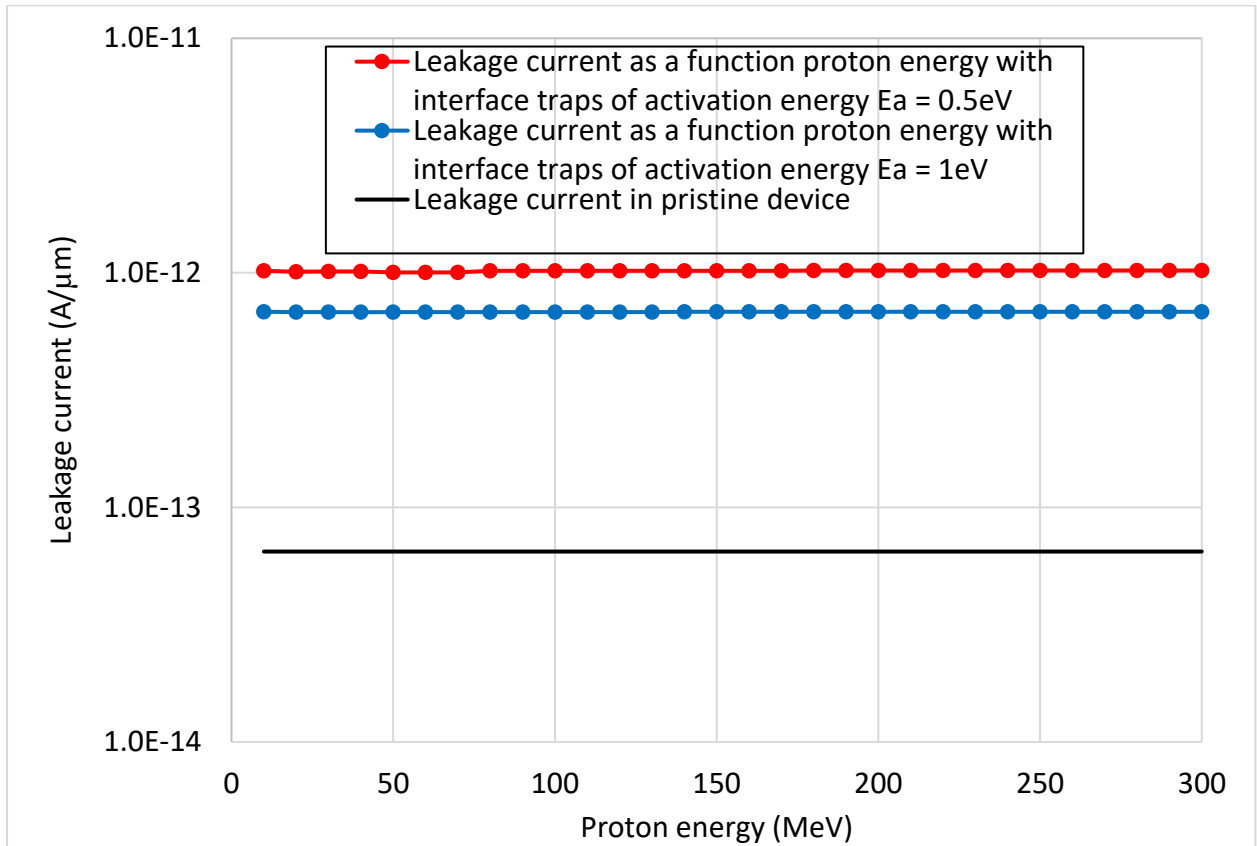


Figure 156: Comparison between leakage current from combined effects of volume traps with influence of Proton plus interface traps (0.5eV (red) and 1eV (blue)). Black line indicates leakage current in pristine device.

Figure 157 shows the leakage current induced by the combined effect of volume traps and interface traps as a function of Xe energy up to 5 GeV. Xe ion significantly increases the leakage current. Highest leakage current is recorded at 500 MeV which is coherent with stopping power provided previously.

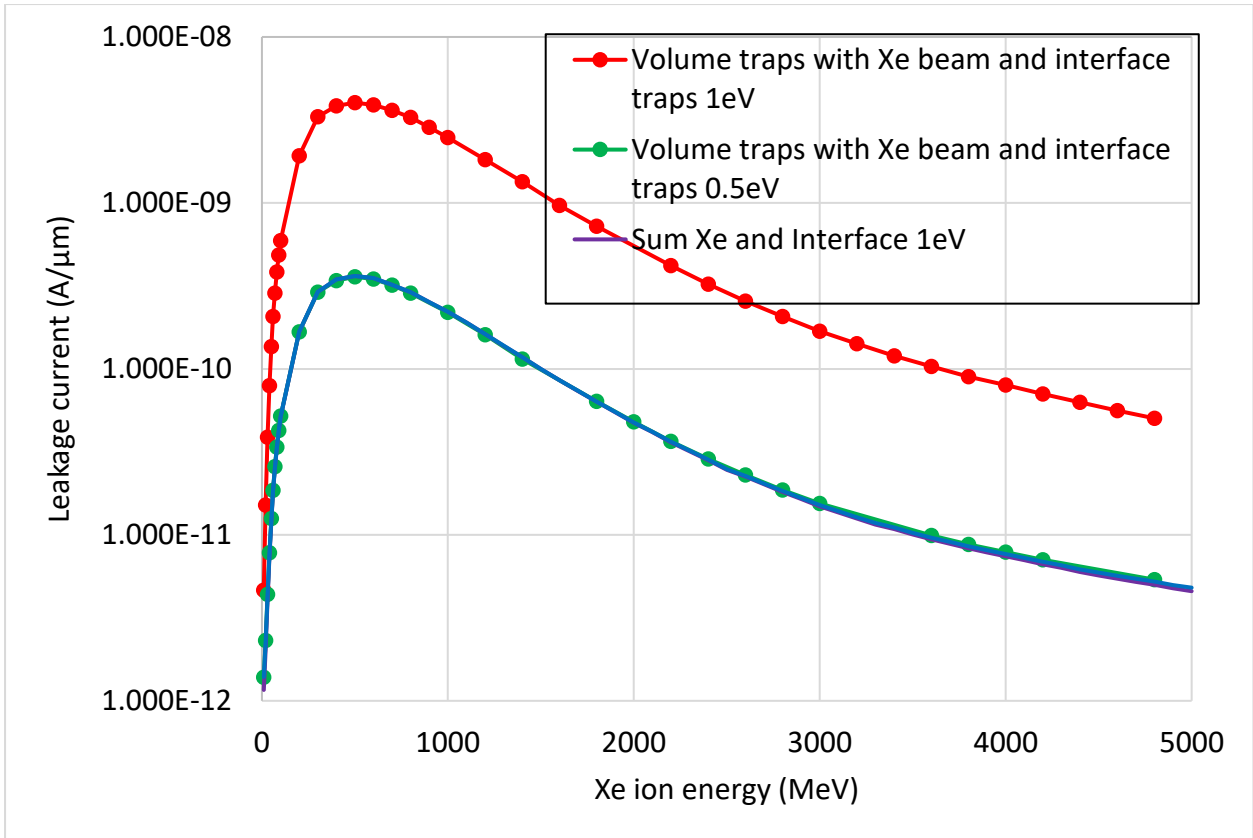


Figure 157: Comparison between leakage current from combined effects of volume traps with influence of Xe ion plus interface traps.

On Figure 157, three leakage currents are almost identical for all ion energies:

- the leakage current induced by the volume traps combined with interface traps at 0.5eV
- the sum of leakage current induced by volume traps and by interface traps at 0.5eV
- the sum of leakage current induced by volume traps and by interface traps at 1eV

Thus, interface traps at 0.5eV do not enhance the leakage current induced by volume traps under Xe ion. On the other hand, the combined effect of volume traps and interface traps at 1eV shows a multiplication factor of the leakage current higher than 10. The Table 26 summarize the values for a 500 MeV Xe ion.

Table 26: Leakage current ( $A/\mu m$ ) for singular and combined phenomena: interface traps and 500 MeV Xe ion ( $E_a$ : activation energy of interface traps).

	Xe 500 MeV Volume traps only	Interface traps only	Sum of effects alone ( $I_{sum}$ )	Combined effects ( $I_{combined}$ )	Ratio $I_{combined}/I_{sum}$
$E_a= 0.5 \text{ eV}$	$3.62 \times 10^{-10}$	$1 \times 10^{-12}$	$3.63 \times 10^{-10}$	$3.59 \times 10^{-10}$	0.99
$E_a= 1 \text{ eV}$	$3.62 \times 10^{-10}$	$7.7 \times 10^{-13}$	$3.628 \times 10^{-10}$	$4.01 \times 10^{-9}$	11.1

According to these results, the electrostatic attraction of free electrons by positive trapped charges is the dominant effect. The generation of electron-hole pairs by interface traps can be neglected.

**5.3.4.4. Combined effects of all three individual effects: volume traps (under influence of Proton and Xe ion), interface traps and defects cluster**

Finally, the combined effect between Volume traps under fluence of Proton/Xe and cluster at the highest leakage position ( $x=0.68 \mu\text{m}$  and  $y= 0.01 \mu\text{m}$ ) is examined.

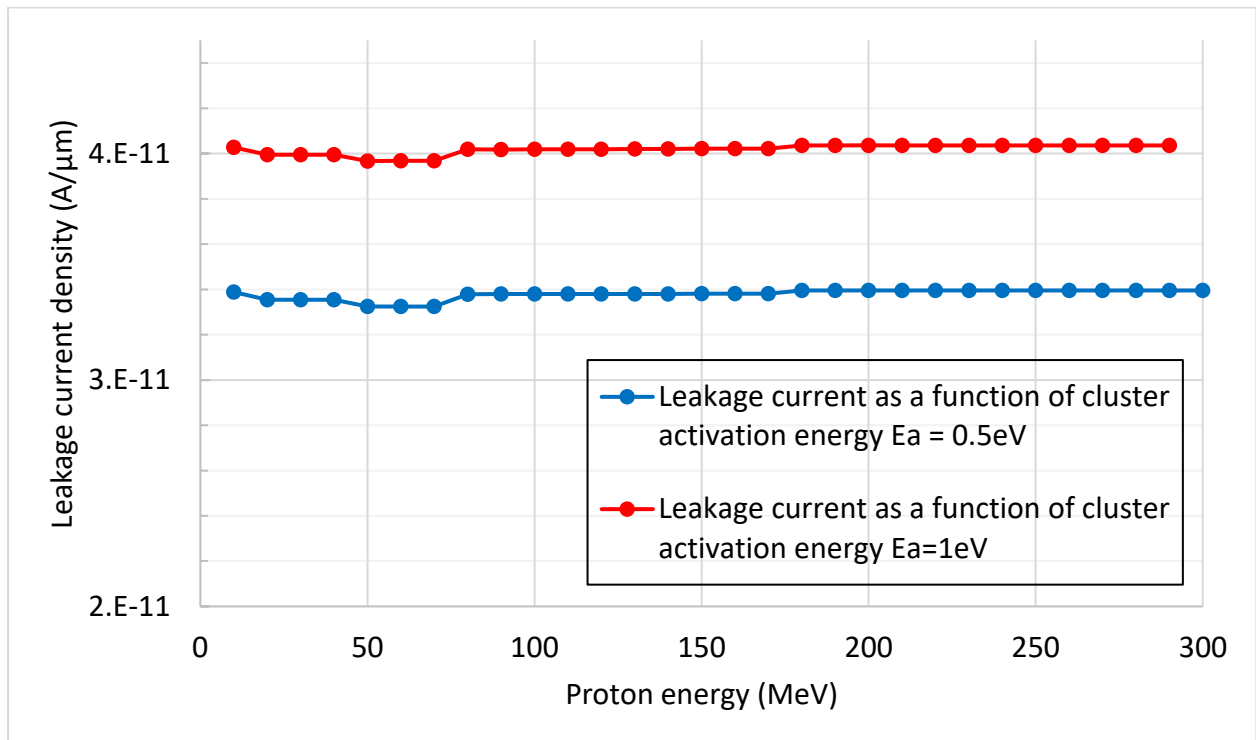


Figure 158: Leakage current density as the function of proton energy for combined effects of: volume traps under effect of proton incident particle, cluster at highest leakage position and interface traps with activation energy  $E_a = 0.5\text{eV}$  (blue) and  $E_a = 1\text{eV}$  (red). Black line indicates leakage current in pristine device.

As observed previously, the microdose deposited by the proton, whatever its energy, has nearly no effect on the leakage current. A small amplification factor is observed with 1eV activation energy of interface traps: 1.15 (see Table 27).

Table 27: Leakage current ( $A/\mu m$ ) for singular and combined phenomena: cluster defects, interface traps and 200 MeV Proton ion ( $E_a$ : activation energy of interface traps).

	Volume traps only	Interface traps only	Cluster only	Sum of effects alone ( $I_{sum}$ )	Combined effects ( $I_{combined}$ )	Ratio $I_{combined}/I_{sum}$
$E_a=0.5$ eV	$6.078 \times 10^{-14}$	$1 \times 10^{-12}$	$3.07 \times 10^{-11}$	$3.18 \times 10^{-11}$	$3.12 \times 10^{-11}$	0.98
$E_a=1$ eV	$6.078 \times 10^{-14}$	$7.7 \times 10^{-13}$	$3.07 \times 10^{-11}$	$3.15 \times 10^{-11}$	$3.63 \times 10^{-11}$	1.15

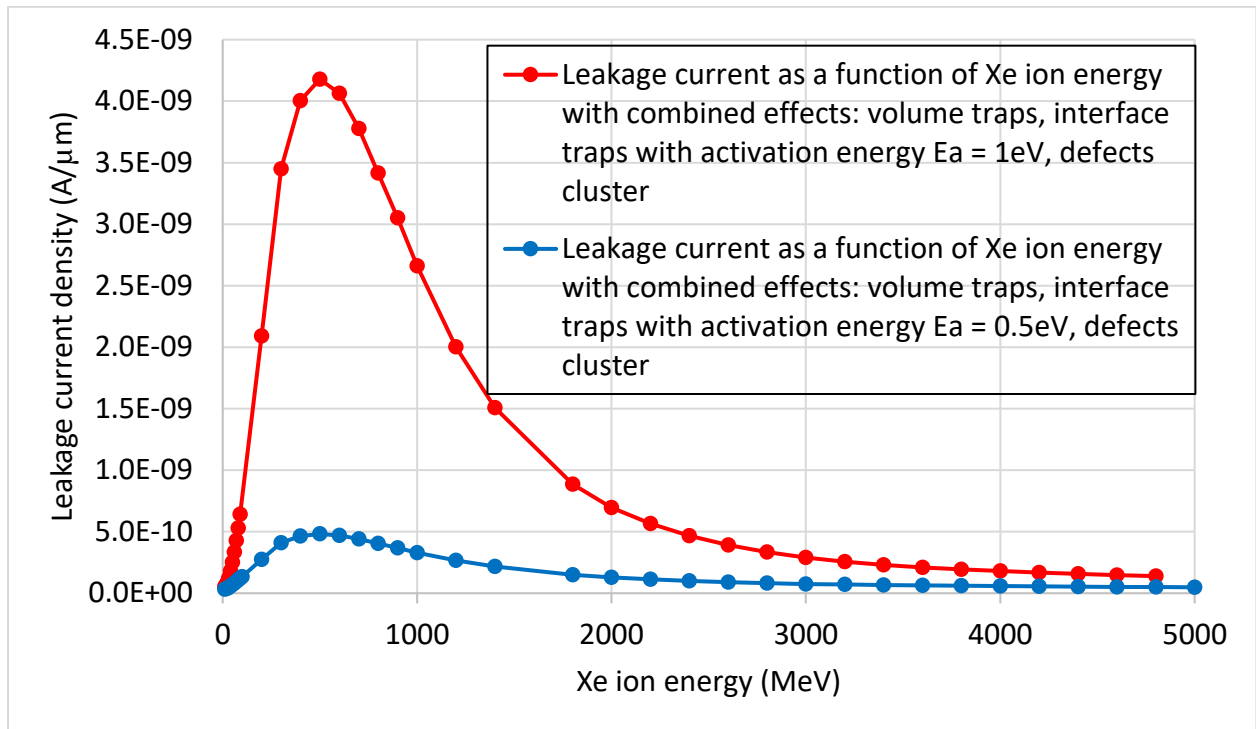


Figure 159: Leakage current as a function of Xe ion energy with combined effects: volume traps, interface traps with activation energy  $E_a = 1eV$  (red) and  $E_a = 0.5eV$  (blue) and defects cluster.

Table 28: Leakage current ( $A/\mu m$ ) for singular and combined phenomena: cluster defects, interface traps and 500 MeV Xe ion ( $E_a$ : activation energy of interface traps).

	Xe 500 MeV Volume traps only	Interface traps only	Cluster only	Sum of effects alone ( $I_{sum}$ )	Combined effects ( $I_{combined}$ )	Ratio $I_{combined}/I_{sum}$
$E_a = 0.5$ eV	$3.62 \times 10^{-10}$	$9.75 \times 10^{-13}$	$3.07 \times 10^{-11}$	$3.937 \times 10^{-10}$	$4.816 \times 10^{-9}$	12.2
$E_a = 1$ eV	$3.62 \times 10^{-10}$	$7.7 \times 10^{-13}$	$3.07 \times 10^{-11}$	$3.934 \times 10^{-10}$	$4.178 \times 10^{-9}$	10.6



Figure 159 shows the combined phenomena as a function of Xe energy up to 5 GeV. A strong amplification factor induced by the interface traps at  $E_a=1\text{eV}$  is observed for all the Xe ion energies.

Table 28 summarizes values for singular and combined phenomena for 500 MeV Xe ion.

For 0.5eV interface traps activation energy the amplification factor is low: 1.22 but significantly higher than without the cluster phenomena: 0.99. Thus, the cluster plays also a role in the amplification factor of the leakage current. At the opposite for 1eV interface traps activation energy, the amplification factor is high as for the modeling without the cluster: 10.6

In the conclusion we propose an explanation of the enhanced leakage current when combining the phenomena. This explanation was deduced from the analyze of modeling results.

## 5.4. Conclusion

From experiment data, we saw that the retention time of DRAM's cells decrease after irradiation. Since a memory cell is made of a capacitor and an accessed transistor, the leakage through the insulator of the capacitor or the leakage current of the transistor may be responsible of this reduction. In this chapter, TCAD modeling with ECORCE software has been used to understand the mechanisms at play in the accessed transistor after radiation effects.

When an energetic particle interacts with MOS transistor, there are three phenomena that can have an effect on the leakage current, depending on its energy and its impact location:

- creation of cluster of defects in the silicon
- trapping of positive charges in the gate oxide-silicon (microdose)
- interface traps build up between oxide and silicon.

By modeling we showed that two effects can be induced from these 3 phenomena:

- electron-hole pairs thermal generation by defects in the volume of the silicon and at the interface between the silicon and the gate oxide. The generation rate depends on the density of defects and the activation energy. It is maximized when the activation energy is in the middle of the silicon gap

- electrostatic attraction of free electron in the channel by positive trapped charges in the volume of the oxide, in the interface traps and in the cluster of defects.

We modeled separately and together the three phenomena. While we were expecting that the combined phenomena will give a leakage current equals to the sum of leakage currents for separated modelings, an amplification factor of more than 10 was seen.

This factor is only observed for the electrostatic attraction of free electron by positive trapped charges. For thermal generation, the combined leakage current is equal to the sum of leakage currents modeled separately.

Indeed, analysis of modelings shows that for 0V gate bias the leakage current changes exponentially as a function of positive trapped charge. Thus, adding the charges trapped in volume trap, interface traps and cluster defects gives a much higher leakage current than trapped charges modeled separately.

Our modelings are consistent with experiments. The low Linear Energy Transfer of proton ion explain why we did not get any stuck bits under proton beam. The trapped charge in the volume of the oxide is too low to have an effect.

On the other hand, Xe ions have a much higher Linear Energy Transfer and modeling show that the charges deposited in the volume of the oxide are significant. We modeled an increase of 4 orders of magnitude of the leakage current for the combined effects.

Furthermore, the facilities propose Xe beams energy of 3.8 GeV. To maximize the effect of the ion experiments the energy of the ions should be adjusted to reach the gate oxide at 500 MeV. Indeed, the electronics LET is 2 times higher and the nuclear LET is 6 times higher than for 3.8 GeV. Thus, the positive charge deposited in the oxide will be 2 times higher and the probability to create displacement damages will be 6 times higher.

# General Conclusion

In this thesis, the weakened cell phenomenon on DRAM in harsh space environment was studied from experiment as well as TCAD modeling and simulation perspectives. The randomness of stuck/unstuck behavior of weakened cell distinguished itself from normal soft error such as SEU or hard error such as permanent stuck bit.

The first chapter gave an overview of different space radiative environments as well as physical mechanisms that cause the degradation of electronic components. Subsequently, literature studies of weakened cells suggested that displacement damage is one of the main causes of increased leakage current in damage cells and intermittent behavior. Recent studies also suggested the possibility of both non-ionizing and ionizing radiation to induce variable retention time of DRAM cells. Depending on the level of damages, it can become a critical source of weakened cells (or also called intermittent stuck bits).

Second chapter described the physical structure, working mechanism and radiation response of DRAM devices. The physical structure of DRAM is simple and consists of one accessed transistor and one storage capacitor. The charges stored inside the capacitor indicate its digital value; however, various leakage sources require periodic refreshing of DRAM to maintain data integrity. DRAM cell characteristics were investigated with leakage paths through transistor and capacitor. Variable retention time due to gate-induced drain leakage current exists in every DRAM device before the irradiation was studied. In addition, the radiation response such as reduction of retention time after irradiation was also discussed. The industry insists on reducing cost and increasing density of DRAM. To achieve this, new 3D structures stack capacitor and trench capacitor have been introduced. Furthermore, in order to maintain sufficient retention time, new structures for capacitor and transistor as well as high-k materials have also been mentioned.

Prior to any modeling work, irradiation campaigns with proton and heavy ion were carried out to recreate the phenomenon by ground testing. The third chapter conveyed experimental aspect of this thesis on DRAM devices under proton and heavy ion irradiation.

Within the framework of a joint program with TRAD Company and the support of CNES, two proton irradiation and one heavy ion irradiation campaigns were carried out. The test bench developed by TRAD allowed not only the testing of single event effects such as SEU, stuck bits, SEFI but also the measurement of retention time for specific memory addresses. Furthermore, with the assistant of GeV devices, the test bench was able to monitor the current consumption of the devices during operation.

Since retention time represents the ability to hold data of DRAM memory cells, we used it as a metric to measure the degradation of DRAM after irradiation. Due to encoding scheme of manufacturers, half population of memory cells were able to keep the data for almost indefinite time, while another half had a limited time. For unirradiated devices, all of DRAM devices tested have the minimum retention time above 5 seconds. This is far greater than 64ms between refresh operations. However, after irradiation the retention time across devices under test (DUT) were decreased depending on the fluence and also proton energies with lower energies induced greater degradation. This result is coherent with other studies in the field.

Following the experimental data, many weakened cells were observed with heavy ion irradiation, but the phenomenon was less sensitive under proton irradiation. Although the retention time of certain damaged cells showed great reduction of retention time after irradiation, they were still able to maintain the data longer than 64ms refresh period. Under normal working condition, these cells should not show any error as long as of DRAM device function properly, however, stuck/unstuck behaviors were still observed. This raised a question about other faulty mechanisms that may occur between refresh operations. In fact, from the consumption current of devices under test, refresh operations were not working properly, which coincided with the increase in the number of weakened cells. During the functional test period, the DUTs were repeatedly read and written to observe the upset or stuck addresses, beside refresh, this operation also restores the data in the cell in addition of refresh command. Every read/write cycle took roughly 1 second to finish on 1Mb of memory, hence if the refresh did not work, cells with a retention time of more than 1 second could still preserve their data. A quick examination of retention time right after irradiation showed that a number of addresses with stuck/unstuck behavior had retention time lower or around 1 second. This is a possible evidence that the refresh was not working when these addresses showed an error. Not all errors during functional test had the retention time lower than read/write period which could be due to a fast annealing at room condition. This behavior had been observed after a high current event and could be reset by an SEFI.

The faulty refresh mechanism partly explained the intermittent behavior observed with a set of weakened cells. However, the physical mechanisms underlying defected cells, which cause the reduction of retention time, should still be examined. In order to achieve that, TCAD modeling with ECORCE was used. It aims to model the behavior of the semiconductor-based electronic components and their response to radiation with multi trapping-detrapping models.

First, a 1D model of PN junction in storage node was simulated with the presence of the Gossick model of defect cluster. The result showed that leakage current depends on position of cluster. The leakage current increased dramatically when it is inside the depletion region.

However, an energetic particle can create three phenomena in the transistor that can have an effect on the leakage current, including: the creation of cluster of defects in the silicon, the trapping of positive charges in the gate oxide-silicon (microdose) and the interface traps built up between oxide and silicon. From that, two mechanisms can be induced: electron-hole pairs thermal generation by defects in the volume of the silicon and at the interface between the silicon and the gate oxide; electrostatic attraction of free electron in the channel by positive trapped charges in the volume of the oxide, in the interface traps and in the cluster of defects.

In order to fully study all the possible radiation effects, 2D model of accessed transistor was constructed.

From cluster damage modeling alone, both n type and p type defects cluster were simulated. The similar results were seen in 2D model which leakage current increased when cluster was positioned in depletion region of accessed transistor. Moreover, the highest leakage current induced by p type cluster was 16 times higher than n type cluster. By analyzing the result, we saw a coherence of electric field with increased leakage current. In short, the highest leakage current of cluster position is at the highest electric field.

Furthermore, volume traps in gate oxide under the influence of the energetic particle were also studied. The modeling results showed that proton with low Linear Energy Transfer induced

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almost no effect. Meanwhile, Xe ions had a much higher Linear Energy Transfer and showed much higher increasing of leakage current due to the significant charges deposited in the volume of the oxide. These results are consistent with our experiments.

The third effect – interface traps were also studied through TCAD modeling. With interface traps density of  $2 \times 10^{11} \text{ cm}^{-2}$  and distributed evenly along gate oxide and silicon interface, we saw an increasing of leakage current.

In addition to the singular effect, combined phenomena were investigated. The results showed an enhance effect with factor up to 10. This factor was only observed for the electrostatic attraction of free electron by positive trapped charges, while it was not seen for thermal generation.

In conclusion, based on simulation results, we found an increase of the leakage current of the individual radiation effect, however, the enhance effect from combined two or more ones can induced even greater leakage current through accessed transistor.

The simulation results, in conjunction with experimental data, showed that the weakened cell behavior is a complex phenomenon that involved multiple defects at played. Those can be combined radiation effects at cell level and defection at system level of the chip that can obstruct the DRAM's normal working scheme, then in turn create stuck/unstuck behaviors.

During this thesis, the amount of both experimental and simulation works carried out has been significant, however, there is still room for future works. For instance, the existing test bench does not support the measurement of variable retention time that can exist in all generation of DRAM. This phenomenon couples with defected cells at certain level can induce similar stuck/unstuck behavior. For modeling aspect, there are so many parameters that can play an important role that has not been covered in this work due to time constrain. Those are cluster size, cluster density, multiple clusters, striking position of incident particle, discrete position of interface traps and especially tunneling currents when the devices' size are shrunk down.

# Publications and communication by the author

## **Publication accepted in a journal as first author**

H. T. Nguyen et al., “TCAD simulation of radiation-induced leakage current in 1T1C SDRAM,” *Microelectronics Reliability*, vol. 88–90, pp. 974–978, Sep. 2018, doi: 10.1016/j.microrel.2018.07.094.

## **Participation to an international conference**

Hoang Nguyen et al., “TCAD simulation of radiation-induced leakage current in SDRAM,” Poster session presented at 29th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, Aalborg, Denmark – October 1-5, 2018

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## References

- [1] “Cosmic rays: particles from outer space.” <https://home.cern/science/physics/cosmic-rays-particles-outer-space> (accessed Dec. 30, 2020).
  - [2] “Luna 1.” <https://nssdc.gsfc.nasa.gov/nmc/spacecraft/display.action?id=1959-012A> (accessed Dec. 30, 2020).
  - [3] “Explorer and Early Satellites.” [https://www.nasa.gov/mission\\_pages/explorer/explorer-overview.html](https://www.nasa.gov/mission_pages/explorer/explorer-overview.html) (accessed Dec. 30, 2020).
  - [4] T. K. Gaisser, R. Engel, and E. Resconi, *Cosmic Rays and Particle Physics*, 2nd ed. Cambridge: Cambridge University Press, 2016. doi: 10.1017/CBO9781139192194.
  - [5] A. M. Hillas, “Cosmic Rays: Recent Progress and some Current Questions,” *arXiv:astro-ph/0607109*, Sep. 2006, Accessed: Jan. 19, 2021. [Online]. Available: <http://arxiv.org/abs/astro-ph/0607109>
  - [6] G. D. Badhwar and P. M. O’Neill, “GALACTIC COSMIC RADIATION MODEL AND ITS APPLICATIONS,” p. 11.
  - [7] G. Santin, P. Truscott, R. Gaillard, and R. G. Alía, “Radiation environments: space, avionics, ground and below,” p. 142.
  - [8] “SPENVIS.” <https://www.spenvis.oma.be/help/background/gcr/gcr.html> (accessed Oct. 05, 2020).
  - [9] P. M. O’Neill, S. Golge, and T. C. Slaba, “Badhwar - O’Neill 2014 Galactic Cosmic Ray Flux Model Description,” p. 32, 2014.
  - [10] D. Matthiä, T. Berger, A. I. Mrigakshi, and G. Reitz, “A ready-to-use galactic cosmic ray model,” *Advances in Space Research*, vol. 51, no. 3, pp. 329–338, Feb. 2013, doi: 10.1016/j.asr.2012.09.022.
  - [11] A. S. Jursa, “HANDBOOK OF GEOPHYSICS AND THE SPACE ENVIRONMENT,” p. 25.
  - [12] Sé. Bourdarie and M. Xapsos, “The Near-Earth Space Radiation Environment,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 1810–1832, Aug. 2008, doi: 10.1109/TNS.2008.2001409.
  - [13] “Techniques for SEE Modeling and Mitigation,” p. 265.
  - [14] S. F. Fung, “Recent Development in the NASA Trapped Radiation Models,” in *Geophysical Monograph Series*, J. F. Lemaire, D. Heynderickx, and D. N. Baker, Eds. Washington, D. C.: American Geophysical Union, 2013, pp. 79–91. doi: 10.1029/GM097p0079.
  - [15] E. G. Stassinopoulos, M. A. Xapsos, and C. A. Stauffer, “Forty-Year ‘Drift’ and Change of the SAA,” p. 78.
  - [16] M. S. Gussenhoven, E. G. Mullen, and D. H. Brautigam, “Improved understanding of the Earth’s radiation belts from the CRRES satellite,” *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 353–368, Apr. 1996, doi: 10.1109/23.490755.
  - [17] W. R. Johnston, T. P. O’Brien, G. P. Ginet, S. L. Huston, T. B. Guild, and J. A. Fennelly, “AE9/AP9/SPM: new models for radiation belt and space plasma specification,” Baltimore, Maryland, USA, Jun. 2014, p. 908508. doi: 10.1117/12.2049836.
  - [18] D. Boscher, A. Sicard-Piet, D. Lazaro, T. Cayton, and G. Rolland, “A New Proton Model for Low Altitude High Energy Specification,” *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3401–3407, Dec. 2014, doi: 10.1109/TNS.2014.2365214.
  - [19] A. Sicard-Piet, D. Boscher, D. Lazaro, S. Bourdarie, and G. Rolland, “A new ONERA-CNES Slot Electron Model,” p. 7.
-

- 
- [20] S. Bourdarie *et al.*, “Outer Electron Belt Specification Model,” *IEEE Trans. Nucl. Sci.*, vol. 56, no. 4, pp. 2251–2257, Aug. 2009, doi: 10.1109/TNS.2009.2014844.
- [21] A. Sicard-Piet, S. Bourdarie, D. Boscher, R. Friedel, and T. Cayton, “Solar Cycle Electron Radiation Environment at GNSS Like Altitude,” presented at the 57th International Astronautical Congress, Valencia, Spain, Oct. 2006. doi: 10.2514/6.IAC-06-D5.2.04.
- [22] A. Sicard-Piet *et al.*, “A new international geostationary electron model: IGE-2006, from 1 keV to 5.2 MeV: GEOSTATIONARY ELECTRON MODEL,” *Space Weather*, vol. 6, no. 7, p. n/a-n/a, Jul. 2008, doi: 10.1029/2007SW000368.
- [23] A. Sicard, D. Boscher, S. Bourdarie, D. Lazaro, D. Standarovski, and R. Ecoffet, “GREEN: the new Global Radiation Earth ENvironment model (beta version),” *Ann. Geophys.*, vol. 36, no. 4, pp. 953–967, Jul. 2018, doi: 10.5194/angeo-36-953-2018.
- [24] D. V. Reames, “Particle acceleration at the Sun and in the heliosphere,” p. 79.
- [25] J. D. Cressler, “Extreme Environment Electronics,” p. 1022.
- [26] M. A. Xapsos, J. L. Barth, and E. G. Stassinopoulos, “Effects: Model for Emission of Solar Protons (ESP)--Cumulative and Worst-Case Event Fluences,” p. 32.
- [27] “ECSS E-10-04 Space Environment Standard.” ESA Requirements and Standards Division ESTEC, P.O. Box 299, 2200 AG Noordwijk The Netherlands.
- [28] E. G. Stassinopoulos, “SOLPRO: a computer code to calculate probabilistic energetic solar proton fluences,” p. 29.
- [29] J. Feynman, T. P. Armstrong, L. Dao-Gibner, and S. Silverman, “New interplanetary proton fluence model,” p. 8, 1990.
- [30] M. A. Xapsos, G. P. Summers, J. L. Barth, E. G. Stassinopoulos, and E. A. Burke, “Probability model for worst case solar proton event fluences,” *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, pp. 1481–1485, Dec. 1999, doi: 10.1109/23.819111.
- [31] J. L. Barth and E. G. Stassinopoulos, “Probability Model for Cumulative Solar Proton Event Fluences,” p. 5.
- [32] M. A. Xapsos, C. Stauffer, G. B. Gee, J. L. Barth, E. G. Stassinopoulos, and R. E. McGuire, “Model for solar proton risk assessment,” *IEEE Trans. Nucl. Sci.*, vol. 51, no. 6, pp. 3394–3398, Dec. 2004, doi: 10.1109/TNS.2004.839159.
- [33] M. Xapsos, “Modeling the Space Radiation Environment,” p. 63.
- [34] J. R. Schwank, “Basic Mechanisms of Radiation Effects in the Natural Space Radiation Environment.” Sandia National Laboratories Albuquerque, NM 87185-1083.
- [35] F. Z. James, *SRIM*. [Online]. Available: <http://www.srim.org/>
- [36] O. Timothy R, *IONIZING RADIATION EFFECTS IN MOS OXIDES*. World Scientific, 2000.
- [37] J. R. Schwank *et al.*, “Radiation-Induced Interface-State Generation in MOS Devices,” *IEEE Trans. Nucl. Sci.*, vol. 33, no. 6, pp. 1177–1184, 1986, doi: 10.1109/TNS.1986.4334575.
- [38] M. Schmidt and H. Köster, “Hole trap analysis in SiO<sub>2</sub>/Si structures by electron tunneling,” *phys. stat. sol. (b)*, vol. 174, no. 1, pp. 53–66, Nov. 1992, doi: 10.1002/pssb.2221740106.
- [39] J. R. Schwank *et al.*, “Radiation Effects in MOS Oxides,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 1833–1853, Aug. 2008, doi: 10.1109/TNS.2008.2001040.
- [40] P. J. McWhorter and P. S. Winokur, “Simple technique for separating the effects of interface traps and trapped-oxide charge in metal-oxide-semiconductor transistors,” *Appl. Phys. Lett.*, vol. 48, no. 2, pp. 133–135, Jan. 1986, doi: 10.1063/1.96974.
- [41] R. C. Lacoë, “Improving Integrated Circuit Performance Through the Application of Hardness-by-Design Methodology,” *IEEE Trans. Nucl. Sci.*, vol. 55, no. 4, pp. 1903–1925, Aug. 2008, doi: 10.1109/TNS.2008.2000480.
-



- 
- [42] C. Poivey, “TNID Total Non Ionizing Dose or DD Displacement Damage,” p. 40.
- [43] Insoo Jun *et al.*, “Proton nonionizing energy loss (niel) for device applications,” *IEEE Trans. Nucl. Sci.*, vol. 50, no. 6, pp. 1924–1928, Dec. 2003, doi: 10.1109/TNS.2003.820760.
- [44] S. Wood *et al.*, “Simulation of Radiation Damage in Solids,” *IEEE Trans. Nucl. Sci.*, vol. 28, no. 6, pp. 4107–4112, 1981, doi: 10.1109/TNS.1981.4335684.
- [45] C. Virmontois *et al.*, “Similarities Between Proton and Neutron Induced Dark Current Distribution in CMOS Image Sensors,” *IEEE Transactions on Nuclear Science*, vol. 59, no. 4, pp. 927–936, Aug. 2012, doi: 10.1109/TNS.2012.2203317.
- [46] J.-M. Belloir *et al.*, “Dark Current Spectroscopy in Neutron, Proton and Ion Irradiated CMOS Image Sensors: From Point Defects to Clusters,” *IEEE Trans. Nucl. Sci.*, vol. 64, no. 1, pp. 27–37, Jan. 2017, doi: 10.1109/TNS.2016.2641479.
- [47] B. R. Gossick, “Disordered Regions in Semiconductors Bombarded by Fast Neutrons,” *Journal of Applied Physics*, vol. 30, no. 8, pp. 1214–1218, Aug. 1959, doi: 10.1063/1.1735295.
- [48] M. Raine *et al.*, “Simulation of Single Particle Displacement Damage in Silicon – Part I: Global Approach and Primary Interaction Simulation,” *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 133–140, Jan. 2017, doi: 10.1109/TNS.2016.2615133.
- [49] A. Jay *et al.*, “Simulation of Single Particle Displacement Damage in Silicon—Part II: Generation and Long-Time Relaxation of Damage Structure,” *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 141–148, Jan. 2017, doi: 10.1109/TNS.2016.2628089.
- [50] A. Jay *et al.*, “Simulation of Single-Particle Displacement Damage in Silicon—Part III: First Principle Characterization of Defect Properties,” *IEEE Trans. Nucl. Sci.*, vol. 65, no. 2, pp. 724–731, Feb. 2018, doi: 10.1109/TNS.2018.2790843.
- [51] K. Sammy, “Space Radiation Effects on Microelectronics.” Radiation Effects Group, JPL, NASA.
- [52] “Heavy ion cocktails available at RADEF,” Jan. 04, 2021.  
<https://www.jyu.fi/science/en/physics/research/infrastructures/accelerator-laboratory/radiation-effects-facility/heavy-ion-cocktails>
- [53] R. C. Baumann, “Radiation-induced soft errors in advanced semiconductor technologies,” *IEEE Trans. Device Mater. Reliab.*, vol. 5, no. 3, pp. 305–316, Sep. 2005, doi: 10.1109/TDMR.2005.853449.
- [54] A. H. Johnston, “The influence of VLSI technology evolution on radiation-induced latchup in space systems,” *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 505–521, Apr. 1996, doi: 10.1109/23.490897.
- [55] P. Philippe, “SHORT COURSE NOTES - Overview of the main concepts of radiation effects and their evolution over the 30 years of RADECS conferences,” Sep. 2019.
- [56] A. Rodriguez, “Étude des Mécanismes de Déclenchement de Bits Collés dans les SRAM et DRAM en Environnement Radiatif Spatial,” PhD dissertation School of Informations, Structures, Systèmes, Université de Montpellier, 2017.
- [57] A. Samaras *et al.*, “Experimental Characterization and In-Flight Observation of Weakened Cell in SDRAM,” in *2015 15th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Moscow, Russia, Sep. 2015, pp. 1–8. doi: 10.1109/RADECS.2015.7365611.
- [58] A. Rodriguez *et al.*, “Proton-Induced Single-Event Degradation in SDRAMs,” *IEEE Trans. Nucl. Sci.*, vol. 63, no. 4, pp. 2115–2121, Aug. 2016, doi: 10.1109/TNS.2016.2551733.
- [59] M. Swift and A. H. Johnston, “A New Class of Single Event Hard Errors,” p. 6.
-

- 
- [60] H. Shindou, S. Kuboyama, N. Ikeda, T. Hirao, and S. Matsuda, "Bulk damage caused by single protons in SDRAMs," *IEEE Transactions on Nuclear Science*, vol. 50, no. 6, pp. 1839–1845, Dec. 2003, doi: 10.1109/TNS.2003.820727.
- [61] J. Segura and C. F. Hawkins, *CMOS electronics: how it works, how it fails*. New York: IEEE Press ; Wiley-Interscience, 2004.
- [62] A. M. Chugg, A. J. Burnell, P. H. Duncan, S. Parker, and J. Ward, "The Random Telegraph Signal Behavior of Intermittently Stuck Bits in SDRAMs," *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3057–3064, Dec. 2009, doi: 10.1109/TNS.2009.2032184.
- [63] A. Haran, J. Barak, D. David, E. Keren, N. Refaeli, and S. Rapaport, "Single Event Hard Errors in SRAM Under Heavy Ion Irradiation," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 5, pp. 2702–2710, Oct. 2014, doi: 10.1109/TNS.2014.2345697.
- [64] A. B. Boruzdina, A. V. Yanenko, A. V. Ulanova, A. I. Chumakov, D. V. Bobrovskiy, and V. M. Uzhegov, "Microdose effects in SRAM cells under heavy ion irradiation," in *2017 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Geneva, Switzerland, Oct. 2017, pp. 1–3. doi: 10.1109/RADECS.2017.8696109.
- [65] T. R. Oldham and J. M. McGarrity, "Ionization of SiO<sub>2</sub> by Heavy Charged Particles," *IEEE Transactions on Nuclear Science*, vol. 28, no. 6, pp. 3975–3980, 1981, doi: 10.1109/TNS.1981.4335658.
- [66] L. D. Edmonds and L. Z. Scheick, "Physical Mechanisms of Ion-Induced Stuck Bits in the Hyundai 16M $\times$  SDRAM," *IEEE Transactions on Nuclear Science*, vol. 55, no. 6, pp. 3265–3271, Dec. 2008, doi: 10.1109/TNS.2008.2006902.
- [67] J.-P. David, F. Bezerra, E. Lorfvre, T. Nuns, and C. Inguibert, "Light Particle-Induced Single Event Degradation in SDRAMs," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3544–3549, Dec. 2006, doi: 10.1109/TNS.2006.886210.
- [68] A. M. Chugg, A. J. Burnell, P. H. Duncan, S. Parker, and J. Ward, "The Random Telegraph Signal Behavior of Intermittently Stuck Bits in SDRAMs," *IEEE Transactions on Nuclear Science*, vol. 56, no. 6, pp. 3057–3064, Dec. 2009, doi: 10.1109/TNS.2009.2032184.
- [69] A. M. Chugg, J. McIntosh, A. J. Burnell, P. H. Duncan, and J. Ward, "Probing the Nature of Intermittently Stuck Bits in Dynamic RAM Cells," *IEEE Transactions on Nuclear Science*, Dec. 2010, doi: 10.1109/TNS.2010.2084103.
- [70] S. Kuboyama, H. Shindou, T. Hirao, and S. Matsuda, "Consistency of bulk damage factor and NIEL for electrons, protons, and heavy ions in Si CCDs," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 2684–2689, Dec. 2002, doi: 10.1109/TNS.2002.805360.
- [71] J. R. Srour and J. W. Palko, "A Framework for Understanding Displacement Damage Mechanisms in Irradiated Silicon Devices," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3610–3620, Dec. 2006, doi: 10.1109/TNS.2006.885796.
- [72] V. Goiffon *et al.*, "Radiation-Induced Variable Retention Time in Dynamic Random Access Memories," *IEEE Trans. Nucl. Sci.*, vol. 67, no. 1, pp. 234–244, Jan. 2020, doi: 10.1109/TNS.2019.2956293.
- [73] S. Yu and P.-Y. Chen, "Emerging Memory Technologies: Recent Trends and Prospects," *IEEE Solid-State Circuits Mag.*, vol. 8, no. 2, pp. 43–56, 2016, doi: 10.1109/MSSC.2016.2546199.
- [74] J. Bruce, W. N. Spencer, T. W. David, and A. Thomasian, "Memory Systems Cache, DRAM, Disk," in *Memory Systems Cache, DRAM, Disk*, Elsevier, 2008, pp. i–ii. doi: 10.1016/B978-0-12-379751-3.50036-9.
- [75] S. Thomas, "Introduction to Information Storage Technology." <https://www.cse.scu.edu/~tschwarz/coen180/LN/DRAM.html>
- [76] D. R.H., "US3387286.pdf," U.S. Patent US3387286A
-

- 
- [77] V. L. Rideout, "One-Device Cells for Dynamic Random-Access Memories: A Tutorial." *IEEE Trans. Electron Devices*, Vol. ED-26, no. 6, pp. 839–852, Jun. 1979.
- [78] V. L. Rideout, J. J. Walker, and A. Cramer, "A One-Device Memory Cell Using a Single Layer of Polysilicon and a Self-Registering Metal-to-Polysilicon Contact," vol. 24, no. 3, p. 9, 1980.
- [79] H. Sunami, T. Kure, K. Yagi, K. Yamaguchi, and S. Shimizu, "Scaling consideration and dielectric breakdown improvement of corrugated capacitor cell (CCC) for future DRAM," p. 4.
- [80] T. Sumi *et al.*, "A 60ns 4Mb DRAM in a 300mil DIP," *ISSCC Dig. Tech. Papers*, pp. 228–283, 1987.
- [81] P. Chatterjee, "Trench and compact structures for dRAMs," in *1986 International Electron Devices Meeting*, 1986, pp. 128–131. doi: 10.1109/IEDM.1986.191130.
- [82] M. A. Siddiqi, *Dynamic RAM technology advancements*. CRC Press Taylor & Francis Group, LLC, 2013.
- [83] M. Koyanagi, "The Stacked Capacitor DRAM Cell and Three-Dimensional Memory," *IEEE Solid-State Circuits Newsl.*, vol. 13, no. 1, pp. 37–41, 2008, doi: 10.1109/N-SSC.2008.4785690.
- [84] M. Koyanagi and K. Sato, "Japanese patent application," Tokugansho 51-78967, 1976
- [85] M. Koyanagi and K. Sato, "USP-4151607," USP-4151607, Jan. 05, 1977
- [86] S. Kimura, "Capacitor over Bitline (COB) DRAM Cell and its Contributions to High Density DRAMs," in *2008 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, Hsinchu, Taiwan, Apr. 2008, pp. 79–80. doi: 10.1109/VTSA.2008.4530807.
- [87] H. Sunami, "Dimension Increase in Metal-Oxide-Semiconductor Memories and Transistors," in *Advances in Solid State Circuit Technologies*, P. K, Ed. InTech, 2010. doi: 10.5772/8638.
- [88] K. Kim, "Future memory technology: challenges and opportunities," p. 5.
- [89] W. Kwon, "Novel Technologies for Next Generation Memory," University of California, Berkeley, 2013.
- [90] S.-W. Chung *et al.*, "Highly Scalable Saddle-Fin (S-Fin) Transistor for Sub-50nm DRAM Technology," in *2006 Symposium on VLSI Technology, 2006. Digest of Technical Papers.*, Honolulu, HI, USA, 2006, pp. 32–33. doi: 10.1109/VLSIT.2006.1705202.
- [91] Hyunjin Lee *et al.*, "Fully integrated and functioned 44nm DRAM technology for 1GB DRAM," in *2008 Symposium on VLSI Technology*, Honolulu, HI, USA, Jun. 2008, pp. 86–87. doi: 10.1109/VLSIT.2008.4588572.
- [92] Y. Chun, "Tutorial overview: DRAM Technology," SK Hynix lecture for POSTECH, 2012.
- [93] R. D. Clark, "Emerging Applications for High K Materials in VLSI Technology," p. 32, 2014.
- [94] K. S. Tang, W. S. Lau, and G. S. Samudra, "Trend in DRAM dielectrics." *Circuits and Devices*, May 1997.
- [95] M. Sakao *et al.*, "A capacitor-over-bit-line (COB) cell with a hemispherical-grain storage node for 64 Mb DRAMs," in *International Technical Digest on Electron Devices*, San Francisco, CA, USA, 1990, pp. 655–658. doi: 10.1109/IEDM.1990.237114.
- [96] T. Kaga *et al.*, "Crown-shaped stacked-capacitor cell for 1.5-V operation 64-Mb DRAMs," *IEEE Trans. Electron Devices*, vol. 38, no. 2, pp. 255–261, Feb. 1991, doi: 10.1109/16.69903.
-

- 
- [97] S.-G. Kim *et al.*, “Fully integrated 512 Mb DRAMs with HSG-merged-AHO cylinder capacitor,” p. 5, 2006.
- [98] S. Jones, “LithoVision 2019 – Semiconductor Technology Trends and their impact on Lithography,” Jan. 03, 2019. <https://semiwiki.com/semiconductor-services/ic-knowledge/8022-lithovision-2019-semiconductor-technology-trends-and-their-impact-on-lithography/>
- [99] Jooyoung Lee, Daewon Ha, and Kinam Kim, “Novel cell transistor using retracted Si/sub 3/N/sub 4/-liner STI for the improvement of data retention time in gigabit density DRAM and beyond,” *IEEE Trans. Electron Devices*, vol. 48, no. 6, pp. 1152–1158, Jun. 2001, doi: 10.1109/16.925241.
- [100] D. S. Yaney, C. Y. Lu, R. A. Kohler, M. J. Kelly, and J. T. Nelson, “A meta-stable leakage phenomenon in DRAM charge storage &#8212;Variable hold time,” in *1987 International Electron Devices Meeting*, 1987, pp. 336–339. doi: 10.1109/IEDM.1987.191425.
- [101] Restle, Park, and Lloyd, “DRAM variable retention time,” in *International Technical Digest on Electron Devices Meeting*, San Francisco, CA, USA, 1992, pp. 807–810. doi: 10.1109/IEDM.1992.307481.
- [102] T. Umeda *et al.*, “Single silicon vacancy-oxygen complex defect and variable retention time phenomenon in dynamic random access memories,” *Appl. Phys. Lett.*, vol. 88, no. 25, p. 253504, Jun. 2006, doi: 10.1063/1.2213966.
- [103] Y. Mori, K. Takeda, and R. Yamada, “Random telegraph noise of junction leakage current in submicron devices,” *Journal of Applied Physics*, vol. 107, no. 1, p. 014509, Jan. 2010, doi: 10.1063/1.3268479.
- [104] Byoungchan Oh *et al.*, “Characterization of an Oxide Trap Leading to Random Telegraph Noise in Gate-Induced Drain Leakage Current of DRAM Cell Transistors,” *IEEE Trans. Electron Devices*, vol. 58, no. 6, pp. 1741–1747, Jun. 2011, doi: 10.1109/TED.2011.2126046.
- [105] S.-W. Yoo, “Analysis on Characteristics and Trapping Mechanism of Trap Sites inside Dielectric or Drain Causing Random Telegraph Noise in TrapAssisted Tunneling GIDL,” DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING COLLEGE OF ENGINEERING SEOUL NATIONAL UNIVERSITY, 2016.
- [106] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, “Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits,” *PROCEEDINGS OF THE IEEE*, vol. 91, no. 2, p. 23, 2003.
- [107] E. Nadimi, C. Radehaus, E. P. Nakhmedov, and K. Wiczorek, “Calculation of the direct tunneling current in a metal-oxide-semiconductor structure with one-side open boundary,” *Journal of Applied Physics*, vol. 99, no. 10, p. 104501, May 2006, doi: 10.1063/1.2202196.
- [108] K. F. Schuegraf and C. Hu, “Hole Injection SiO<sub>2</sub> Breakdown Model for Very Low Voltage Lifetime Extrapolation,” *IEEE TRANSACTIONS ON ELECTRON DEVICES*, vol. 41, May 1994.
- [109] J. C. Ranuarez, M. J. Deen, and C.-H. Chen, “A review of gate tunneling current in MOS devices,” *Microelectronics Reliability*, p. 18, 2006.
- [110] M. Lenzlinger and E. H. Snow, “Fowler-Nordheim Tunneling into Thermally Grown SiO<sub>2</sub>,” *Journal of Applied Physics*, vol. 40, no. 1, pp. 278–283, Jan. 1969, doi: 10.1063/1.1657043.
- [111] Y. Taur and T. H. Ning, *Fundamentals of modern VLSI devices*, 2nd ed. Cambridge, UK ; New York: Cambridge University Press, 2009.
-

- 
- [112] Minchen Chang *et al.*, “Impact of gate-induced drain leakage on retention time distribution of 256 Mbit DRAM with negative wordline bias,” *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 1036–1041, Apr. 2003, doi: 10.1109/TED.2003.812498.
- [113] K. Saino *et al.*, “Impact of gate-induced drain leakage current on the tail distribution of DRAM data retention time,” in *International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138)*, San Francisco, CA, USA, 2000, pp. 837–840. doi: 10.1109/IEDM.2000.904447.
- [114] J.-H. Chen, S.-C. Wong, and Y.-H. Wang, “An Analytic Three-Terminal Band-to-Band Tunneling Model on GIDL in MOSFET,” *IEEE TRANSACTIONS ON ELECTRON DEVICES*, vol. 48, no. 7, p. 6, 2001.
- [115] E. O. Kane, “Zener tunneling in semiconductors,” *Journal of Physics and Chemistry of Solids*, vol. 12, no. 2, pp. 181–188, Jan. 1960, doi: 10.1016/0022-3697(60)90035-4.
- [116] W. Y. Choi, G. Yoon, W. Y. Chung, Y. Cho, S. Shin, and K. H. Ahn, “A Technology-Computer-Aided-Design-Based Reliability Prediction Model for DRAM Storage Capacitors,” *Micromachines*, vol. 10, no. 4, p. 256, Apr. 2019, doi: 10.3390/mi10040256.
- [117] S. Simon and K. N. Kwok, *Physics of Semiconductor Devices*. Willey, 2006.
- [118] L. Z. Scheick, S. M. Guertin, and G. M. Swift, “Analysis of radiation effects on individual DRAM cells,” *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, pp. 2534–2538, Dec. 2000, doi: 10.1109/23.903804.
- [119] B. Doucin *et al.*, “Study of radiation effects on low voltage memories,” in *RADECS 97. Fourth European Conference on Radiation and its Effects on Components and Systems (Cat. No.97TH8294)*, Cannes, France, 1998, pp. 561–569. doi: 10.1109/RADECS.1997.699001.
- [120] R. Harboe-Ssrensen, M. Briiggemann, R. Miille, and F. J. Rombeck, “Radiation Evaluation of 3.3 Volt 16 M-bit DRA Solid State Mass Memory Space Applications.,” p. 6.
- [121] S. M. Guertin and M. Amrbar, “Single Event Testing of SDRAM, DDR2 and DDR3 Memories,” in *2016 IEEE Radiation Effects Data Workshop (REDW)*, Portland, OR, USA, 2016, pp. 1–7. doi: 10.1109/NSREC.2016.7891742.
- [122] K. Grurmann *et al.*, “Heavy Ion sensitivity of 16/32-Gbit NAND-Flash and 4-Gbit DDR3 SDRAM,” p. 6.
- [123] A. Bacchini, G. Furano, M. Rovatti, and M. Ottavi, “Total Ionizing Dose Effects on DRAM Data Retention Time,” *IEEE Trans. Nucl. Sci.*, vol. 61, no. 6, pp. 3690–3693, Dec. 2014, doi: 10.1109/TNS.2014.2365532.
- [124] M. Fieback, M. Taouil, S. Hamdioui, and M. Rovatti, “Ionizing radiation modeling in DRAM transistors,” in *2018 IEEE 19th Latin-American Test Symposium (LATS)*, Sao Paulo, Mar. 2018, pp. 1–6. doi: 10.1109/LATW.2018.8349678.
- [125] “TRAD/CNE/R&T/BCOLLES/AS3/280814 Labege, rev 0,” Labege, Aug. 2014.
- [126] A. Rodriguez and A. Samaras, “R&T BITS COLLES - Rapport Final : Effet sur les composants SDRAM EDS5104ABTA et HY57V651620,” TRAD/CNE/R&T/BCOLLES-2/AS3/121214, Dec. 2014.
- [127] a Samaras, “R&T BITS COLLES - Rapport Intermédiaire : Irradiation en dose des composants Hyundai HY57V651620BLTC,” TRAD/CNE/R&T/BCOLLES-3/AS3/250915, Sep. 2015.
- [128] “TRAD/CNE/R&T/BCOLLES-3/AP/171215 , Revision 2,” Labège, Jul. 2016.
- [129] L. Standaert, N. Postiau, and M. Loiselet, “UCL irradiation facilities status,” in *2017 17th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Geneva, Switzerland, Oct. 2017, pp. 1–3. doi: 10.1109/RADECS.2017.8696227.
-

- 
- [130] “High Energy Site,” Paul Scherrer Institut (PSI).” <https://www.psi.ch/en/pif/description> (accessed Oct. 10, 2020).
- [131] M.-H. Moscatello, A. Dubois, and X. Ledoux, “Industrial applications with GANIL SPIRAL2 facility,” in *2016 16th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Bremen, Germany, Sep. 2016, pp. 1–3. doi: 10.1109/RADECS.2016.8093164.
- [132] *HY57V651620B 4 Banks x 1M x 16Bit Synchronous DRAM*. Hynix Semiconductor.
- [133] B. Stephen, M. Paul, L. Ken, and K. Scott, “Proton Test Guideline Development – Lessons Learned,” NASA/Goddard Space Flight Center, NASA Electronic Parts and Packaging (NEPP) Program Electronics Radiation Characterization (ERC) Project, Defense Threat Reduction Agency, Aug. 2002.
- [134] A. Varotsou *et al.*, “The OMERE radiation environment and effects engineering tool,” p. 18, 2017.
- [135] P. C. Adell, L. Edmonds, R. McPeak, L. Scheick, and S. S. McClure, “An Approach to Single Event Testing of SDRAMs,” p. 5.
- [136] A. Michez, S. Dhombres, and J. Boch, “ECORCE: A TCAD Tool for Total Ionizing Dose and Single Event Effect Modeling,” *IEEE Transactions on Nuclear Science*, vol. 62, no. 4, pp. 1516–1527, Aug. 2015, doi: 10.1109/TNS.2015.2449281.
- [137] “Radiac webpage.” <https://www.ies.univ-montp2.fr/edr/radiac/> (accessed Nov. 23, 2020).
- [138] A. Michez, J. Boch, A. Touboul, and F. Saigné, “Dynamic mesh for TCAD modeling with ECORCE,” *J. Phys.: Conf. Ser.*, vol. 738, p. 012128, Aug. 2016, doi: 10.1088/1742-6596/738/1/012128.
- [139] B. Thomas, “Étude des effets de synergie dans les circuits intégrés soumis à l’environnement spatial de rayonnements ionisants et neutres,” University of Montpellier, 2018.
- [140] “Apache Subversion.” <https://subversion.apache.org/> (accessed Nov. 22, 2020).
- [141] “Doxygen: Source code documentation generator tool.” <http://www.doxygen.org/> (accessed Nov. 22, 2020).
- [142] D. M. Caughey and R. E. Thomas, “Carrier Mobilities in Silicon Empirically Related to Doping and Field,” vol. 55, no. 12, pp. 2192–219, 1967.
- [143] G. Masetti, “Modeling of Carrier Mobility Against Carrier Concentration in Arsenic-, Phosphorus-, and Boron-doped Silicon,” p. 6.
- [144] W. Shockley and W. T. Read, “Statistics of the Recombinations of Holes and Electrons,” *Phys. Rev.*, vol. 87, no. 5, pp. 835–842, Sep. 1952, doi: 10.1103/PhysRev.87.835.
- [145] L. Huldt, N. G. Nilsson, and K. G. Svantesson, “The temperature dependence of band-to-band Auger recombination in silicon,” *Appl. Phys. Lett.*, vol. 35, no. 10, pp. 776–777, Nov. 1979, doi: 10.1063/1.90974.
- [146] C. M. Dozier, D. M. Fleetwood, D. B. Brown, and P. S. Winokur, “An Evaluation of Low-Energy X-Ray and Cobalt-60 Irradiations of MOS Transistors,” *IEEE Trans. Nucl. Sci.*, vol. 34, no. 6, pp. 1535–1539, 1987, doi: 10.1109/TNS.1987.4337511.
- [147] J. L. Leray, “Contribution à l’étude des phénomènes induits par les rayonnements ionisants dans les structures à effet de champ au silicium ou à l’arséniure de gallium utilisées en micro-électronique,” University of Paris-sud Orsay, 1989.
- [148] R. Escoffier, “Simulation numérique de l’effet des charges induites par irradiation dans les oxydes de structures MOS.,” p. 136.
- [149] C. R. Cirba, “Simulation numérique du piégeage et du dépiégeage dans les oxydes de composants MOS,” University of Montpellier, 1996.
-

- 
- [150] O. L. Curtis and J. R. Srour, "The multiple-trapping model and hole transport in SiO<sub>2</sub>," *Journal of Applied Physics*, vol. 48, no. 9, pp. 3819–3828, Sep. 1977, doi: 10.1063/1.324248.
- [151] O. L. Curtis and J. R. Srour, "Recombination within Disordered Regions: Influence of Barrier Height on Recombination Rate and Injection Level Effects," *IEEE Trans. Nucl. Sci.*, vol. 20, no. 6, pp. 196–203, 1973, doi: 10.1109/TNS.1973.4327393.
- [152] E. Žasinas, J. Vaitkus, and E. Gaubas, "Modeling Vacancy - Interstitial Clusters and Their Effect on Carrier Transport in Silicon," presented at the presented at the 24th RD50 Workshop, Bucharest.
- [153] J. R. Srour, C. J. Marshall, and P. W. Marshall, "Review of displacement damage effects in silicon devices," *IEEE Transactions on Nuclear Science*, vol. 50, no. 3, pp. 653–670, Jun. 2003, doi: 10.1109/TNS.2003.813197.
- [154] J. Yu and K. Aflatooni, "Leakage Current in DRAM Memory Cell," Jun. 2006, pp. 191–194. doi: 10.1109/UGIM.2006.4286380.
- [155] T. Y. Chan, J. Chen, P. K. Ko, and C. Hu, "The impact of gate-induced drain leakage current on MOSFET scaling," p. 4.
- [156] P. C. Adell, L. Edmonds, R. McPeak, L. Scheick, and S. S. McClure, "An Approach to Single Event Testing of SDRAMs," p. 5.
- [157] T. P. Ma and P. V. Dressendorfer, Eds., *Ionizing radiation effects in MOS devices and circuits*. New York: Wiley, 1989.

# Appendix A

## 1. Test run at UCL

Run	DUT	Beam Energy	Fluence	TNID	Test type	Test pattern	Refresh	Memory size
1	H3	62 Mev	3.6E10 p/cm <sup>2</sup>	1.04E+11	Dynamic functional test	AA/55	64 ms	1Mx16 bit,
	H4, H5				Unbiased			
2	H6	62 MeV	7.2E10 p/cm <sup>2</sup>	2.07158E+11	Dynamic functional test	AA/55	64 ms	1Mx16 bit,
	H7, H8				Unbiased			
3	H9	62 Mev	1.08E11 p/cm <sup>2</sup>	3.10737E+11	Dynamic functional test	AA/55	64 ms	1Mx16 bit,
	H10, H11				Unbiased			
4	H12	62 MeV	3.6E10 p/cm <sup>2</sup>	1.04E+11	Dynamic functional test	FFFF	64 ms	1Mx16 bit,
5	H13	62 Mev	3.6E10 p/cm <sup>2</sup>	1.04E+11	Dynamic functional test	0000	64 ms	1Mx16 bit,
6	H14	40 MeV	2 run total: 9E10 p/cm <sup>2</sup>	3.13E+11	Dynamic functional test	AA/55	64 ms	1Mx16 bit,
	H15, H16				Unbiased			
7	H17	40 MeV	3E10 p/cm <sup>2</sup>	1.04E+11	Dynamic functional test	AA/55	64 ms	1Mx16 bit,
	H18, H19				Unbiased			
8	H20	62 Mev	3.6E10 p/cm <sup>2</sup>	1.04E+11	Dynamic functional test + Heated at 70 c	AA/55	64 ms	1Mx16 bit,
	H21				Unbiased + heated at 70 C			
9	H12	62 MeV	1.08E11 p/cm <sup>2</sup>	3.11E+11	Dynamic functional test	FFFF	64 ms	1Mx16 bit,
10	H13	62 Mev	1.08E11 p/cm <sup>2</sup>	3.11E+11	Dynamic functional test	0000	64 ms	1Mx16 bit,



11	H22	10 MeV	1.08E11 p/cm <sup>2</sup>	6.26E+11	Dynamic functional test	AA/55	64 ms	1Mx16 bit,
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## 2. Test run at GANIL

Run	D U T	Energie (TRIM) (MeV/n uc)	Dege rader ( $\mu$ m)	Air (mm)	LET en surface (MeV.cm <sup>2</sup> /m g)	Range ( $\mu$ m)	LET zone sensible (MeV.cm <sup>2</sup> / mg)	Pattern	Flux (p/cm/s)	Temps (s)	Fluence (p/cm <sup>2</sup> )
1	1	45.92	0	82	26.97	686.45		AA/55	1.14E+03	76.00	8.69E+04
2	1	45.92	0	82	26.97	686.45		AA/55	1.16E+03	444.00	5.16E+05
3	1	34.21	200	100	32.03	452.25		AA/55	1.17E+03	852.00	1.00E+06
4	Functional run										
5	1	24.21	350	100	38.49	284.94		AA/55	1.08E+03	605.00	6.56E+05
6	1	26.84	300	125	36.52	326.01		AA/55	1.01E+03	511.00	5.14E+05
7	2 3	26.84	300	125	36.52	326.01		55/AA	1.12E+03	451.00	5.04E+05
8	2 3	26.84	300	125	36.52	326.01		AA/55	1.02E+03	493.00	5.05E+05

## 3. Test run at PSI

### Run during irradiation

Run	DUT A: Alliance I: ISSI M: Micron	Energy [MeV]	Fluence [p/cm <sup>2</sup> ]	Time [s]	Time [min]	Flux [p/cm <sup>2</sup> /s]	Mode	Pattern	Bias [V]	Refresh delay [ms]	Memory size tested
Day 1											
1	I-6	200	1.00E+11	924	15.4	1.08E+08	Dynamic	AA/55	3,3 V	64	1 Mb
2	I-6	200	4.58E+10	491	8.2	9.33E+07	Dynamic	AA/55	3,3 V	64	1 Mb
1	A-1	200	1.00E+11	926	15.4	1.08E+08	Dynamic	AA/55	3,3 V	64	1 Mb
2	A-1						functional				1 Mb
1	M-1	200	1.89E+10	175	2.9	1.08E+08	Dynamic	AA/55	3,3 V	64	1 Mb
2	M-1	200	1.89E+10	175	2.9	1.08E+08	Dynamic	AA/55	3,3 V	64	1 Mb
3	M-1						functional				4 Mb
4	M-1						functional				1 Mb
5	M-2						functional				1 Mb
6	M-2	60.81	1.00E+11	2564	42.7	3.90E+07	Dynamic	AA/55	3,3 V	64	1 Mb
7	M-2						functional				1 Mb
8	M-2						functional				4 Mb
9	M-2						Invalid run				
10	M-3	200	1.00E+11	879	14.7	1.14E+08	Dynamic	FFFF	3,3 V	64	1 Mb
Day 2											
1	I-1	200	1.00E+11	960	16.0	1.04E+08	Dynamic	AA/55	3,3 V	64	1 Mb
2	I-1						functional				
3	A-3	200	1.00E+11	960	16.0	1.04E+08	Dynamic	AA/55	3,3 V	64	1 Mb

4	A-3						functional				
5	M-4	200	1.00E+11	958	16.0	1.04E+08	Dynamic	AA/55	3,3 V	64	1 Mb
6	M-4						functional				
7	M-4	200	-	531	8.9	-	Dynamic	AA/55	3,3 V	64	1 Mb
8	M-4	200	4.00E+11	2991	49.9	1.34E+08	Dynamic	AA/55	3,3 V	64	1 Mb
9											
10	M-4						functional				
11	M-4						functional				
12	M-4						functional				
13	M-5	121.45	4.86E+10	281	4.7	1.73E+08	Dynamic	AA/55	3,3 V	64	1 Mb
14	M-5	121.45	1.52E+11	837	14.0	1.82E+08	Dynamic	AA/55	3,3 V	64	1 Mb
15	M-5						functional				
16	M-6	60.8	3.02E+10	192	3.2	1.57E+08	Dynamic	AA/55	3,3 V	64	1 Mb
17	M-6	60.8	1.70E+11	1080	18.0	1.58E+08	Dynamic	AA/55	3,3 V	64	1 Mb
18	M-6						functional				
19	M-6						ret				
20	M-6						functional	AA/55			
21	M-6						functional	55/AA			
22	M-6						functional	0000			
23	M-6						functional	FFFF			
24	M-7	200	2.00E+11	1492	24.9	1.34E+08	OFF				
25	M7						functional	AA/55			
26	M7						functional	55/AA			
27	M7						functional	AAAA			
28	M7						functional	5555			
29	M8	200	2.00E+11	1483	24.7	1.35E+08	Dynamic	0000	3,3 V	64	1 Mb
30	M8						functional	0000			1 Mb
31	M8						functional	0000			1 Mb
32	M8						functional	0000			4Mb
33	M8						functional	0000			4Mb
34	M9	200	2.00E+11	1484	24.7	1.35E+08	Dynamic	FFFF	3,3 V	64	1 Mb
35	M9						functional	FFFF			
36	M9						functional	0000			
37	M9						functional	FFFF			4 Mb
38	M9						functional	FFFF			4 Mb
39	M9						functional	0000			4 Mb
40	I-2	200	2.00E+11	1483	24.7	1.35E+08	OFF				
41	I-2	200	3.00E+11	2224	37.1	1.35E+08	OFF				

**Post Irradiation Run**

Run	DUT A: Alliance I: ISSI M: Micron	Worst ret time	Mode	Pattern	Memory size tested
1	M-1		Dynamic	AA55	1Mbit

2	M-1		Dynamic	AA55	4Mbit
3	M-1		Static	AA55	4Mbit
-	M-1	1,8s	Retention time	AA55	1Mbit
4	M-2			AA55	1Mbit
5	M-2			AA55	4Mbit
-	M-2	> 1s	Retention time	AA55	1Mbit
6	M-3			AA55	1Mbit
7	M-3			AA55	4Mbit
-	M-3	700 ms	Retention time	AA55	1Mbit
8	M-3		Dynamic	AA55	1Mbit
9	M-3		Dynamic	AA55	1Mbit
10	M-4		Dynamic	AA55	1Mbit
11	M-4		Dynamic	AA55	4Mbit
-	M-4	-	Retention time	AA55	1Mbit
12	M-5		Dynamic	AA55	1Mbit
13	M-5		Dynamic	AA55	4Mbit
-	M-5	?	Retention time	AA55	1Mbit
14	M-6		Dynamic	AA55	1Mbit
15	M-6		Dynamic	AA55	4Mbit
-			Retention time	AA55	1Mbit
16	M-7		Dynamic	AA55	1Mbit
17	M-7		Dynamic	AA55	4Mbit
-			Retention time	AA55	1Mbit
18	M-8		Dynamic	AA55	1Mbit
19	M-8		Dynamic	AA55	4Mbit
-		-	Retention time	AA55	1Mbit
20	M-9		Dynamic	AA55	1Mbit
21	M-9		Dynamic	AA55	4Mbit
22	M-9		Dynamic	AA55	4Mbit
-			Retention time	AA55	1Mbit
23	I-2		Dynamic	AA55	1Mbit
24	I-2		Dynamic	AA55	4Mbit
25	I-2		Dynamic	AA55	4Mbit
26	I-2		Retention time	AA55	1Mbit