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ON-CHIP GENERATION OF HIGH-FREQUENCY SINUSOIDAL SIGNALS USING HARMONIC CANCELLATION TECHNIQUE

Ankush Mamgain

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THÈSE

Pour obtenir le grade de

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Génération sur puce de signaux sinusoïdaux à hautes fréquences en utilisant des techniques d'annulation d'harmoniques

ON-CHIP GENERATION OF HIGH-FREQUENCY SINUSOIDAL SIGNALS USING HARMONIC CANCELLATION TECHNIQUE

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**ON-CHIP GENERATION OF HIGH-FREQUENCY
SINUSOIDAL SIGNALS USING HARMONIC
CANCELLATION TECHNIQUE**

Ankush MAMGAIN

*A thesis submitted for partial fulfilment of the
degree of Doctor of Philosophy*

Dedicated to my parents and all my teachers.

"Sometimes you have to fall before you fly. ~Anonymous"

—

Abstract

Built-in self-test (BIST) techniques play an important role in Analog, Mixed-signal, and RF (AMS-RF) circuits so that the time, cost, and complexity of testing these circuits in advanced nanometric processes can be improved. These circuits replace highly sophisticated and expensive AMS-RF testers. The stimuli generator is one of the important blocks in AMS-RF BIST circuits. In particular, many analog-RF tests require a high-quality sinusoidal signal as test stimuli. The focus of this thesis is to understand the challenges of generating a sinusoidal signal in the GHz range and mitigating these challenges using the harmonic cancellation principle. In the harmonic cancellation principle, a set of time-shifted periodic signals are scaled and added. In this process, harmonics of the periodic signal are cancelled and the fundamental frequency is retained at the output. The signal generator designed in this thesis focuses on canceling harmonics below the 11th harmonic. Despite its efficiency, this technique is highly susceptible to performance degradation due to mismatch and process variations. These variations affect time-shift and the duty cycle (also called timing inaccuracies) of the signal, particularly in high-frequency applications where precise control becomes increasingly challenging. To address this, a novel calibration architecture employs a coarse-fine delay cell, which effectively mitigates the impact of timing inaccuracies. One of the proposed solutions was fabricated using ST 28-nm FDSOI technology and validated. The measurement results show an SFDR greater than 60dBc for frequencies greater than 1 GHz after optimization, illustrating the potential of our architecture in enhancing the reliability and effectiveness of on-chip sinusoidal signal generation for AMS-RF integrated circuits.

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Introduction

Semiconductors are vital in modern daily life due to their wide range of applications such as consumer electronics, healthcare, IoT, telecommunication, aerospace, defense, etc. The global semiconductor industry market is projected to be a trillion-dollar industry by 2030, according to McKinsey & Company [1]. The sales grew by more than 20% to about \$600 billion in 2021. The projected industry's aggregate annual growth could average from 6 to 8% a year up to 2030, as shown in Fig. 1.1. The semiconductor market has several components such as microprocessors, microcontrollers, DSP, ASIC Design, analog mixed-signal (AMS) design, etc. The estimated market of AMS IC design in particular projected a revenue of \$90.32 billion in 2023. This figure is expected to grow by a compounded annual growth rate (CAGR) of 7.61% to \$121.10 billion by 2027 [4].

This boom in the semiconductor industry can be attributed to significant progress in the manufacturing process. These enhancements have facilitated the inclusion of an increasing number of transistors on a single chip, thereby improving the performance and increasing the functionality of the chip. The AMS circuit includes several blocks such as operational amplifiers, PLLs, ADCs, DACs, analog mixers, filters, etc.

1.1 AMS testing and challenges

Advanced CMOS processes are playing a significant role in shrinking circuit sizes while also enhancing performance and functionality. This miniaturization trend is a key factor

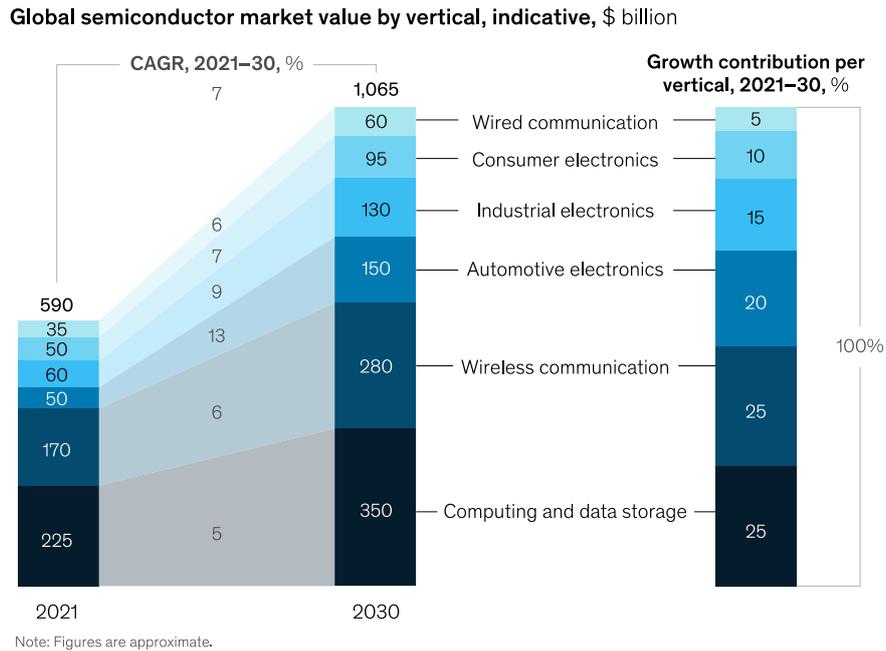


Figure 1.1: Projection of global semiconductor market. (Source: McKinsey & Company) [1]

in achieving more functionality for new-generation chips. However, these processes are accompanied by challenges, including defects, process variations, and mismatch variations which makes testing a crucial step for ensuring the functionality of the fabricated circuits. It saves the production and shipping costs of the company by identifying and, eventually, rectifying the defects at the early stage of production thereby reducing waste and improving the overall quality of the final product. The idea is to ensure that only fully functional products are sent to the customers which not only enhances the reliability of the product but also maintains the reputation of the brand. In summary, testing is essential for minimizing the production cost and maintaining a high-standard product.

However, testing these chips is becoming increasingly complex due to the limited number of IO pins, access to the internal nodes of circuits, test time, and cost of testers. International Technology Roadmap for Semiconductors (ITRS) in 2009 published a trend that shows that the manufacturing cost has been dropping, regardless, the cost of testing the digital circuits and AMS circuits is either increasing or almost constant as shown in Fig.1.2 [2]. This trend represents a significant shift from the past, where test costs were a smaller portion of total manufacturing expenses, to a scenario where testing now constitutes a larger portion, reflecting the evolving demands of high-tech industries. In terms of the test time, while the increased duration can be necessary to

1.1 AMS testing and challenges

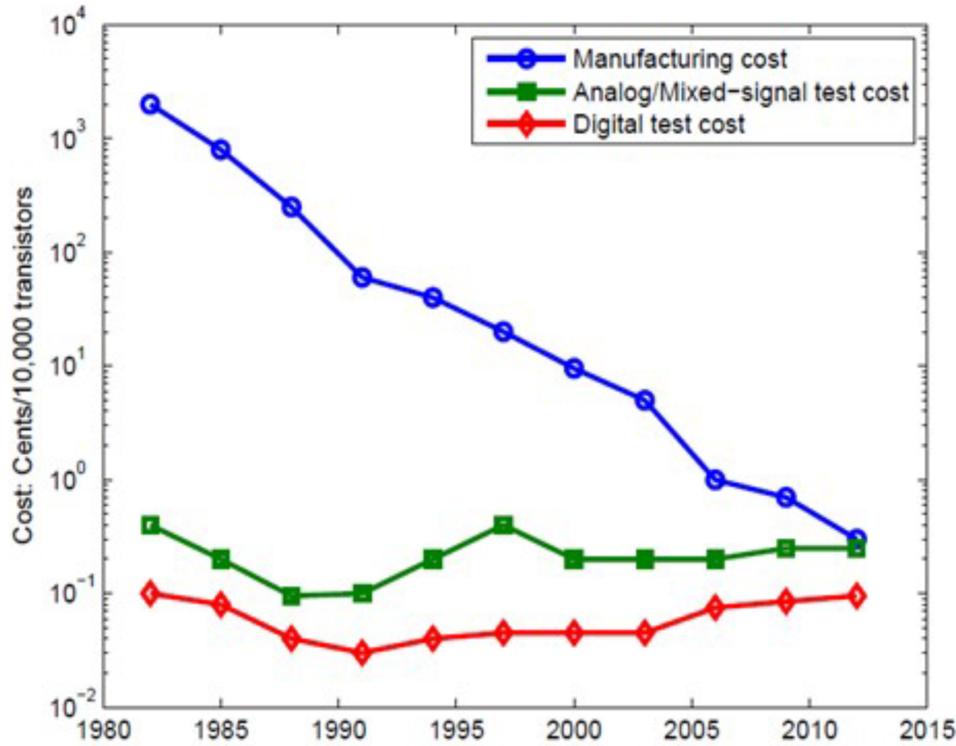
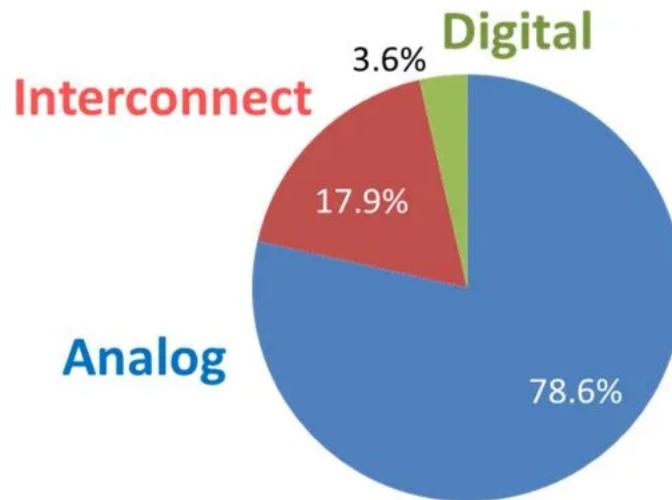


Figure 1.2: Manufacturing cost and test cost per transistor [2]

achieve optimal coverage and ensure reliability in critical applications, this requirement must be balanced with the product-to-market cycle to maintain a competitive edge in the industry.

Digital tests are generally more mature and reliable when compared to analog tests. Fig.1.3 illustrates the sources of the breakdown in an automotive IC, showing that the analog components are the major contributor to these failures. Automated test equipment (ATE) is used to test the ICs. ATE checks if the circuit meets its functional specifications. The ATE measures the circuit's performance under various conditions and compares it with the datasheet. To facilitate these functional tests, the testing setup includes a stimulus generator that stimulates the design under test (DUT), an acquisition instrument that receives and processes the data from DUT, power supplies, etc. There can be some conversion stages such as ADCs, and DACs for handling the signal or digital data. Additionally, there are special circuitry and interface devices used to connect and communicate with the circuit being tested which increases the complexity and cost. The block diagram of a test setup using ATE is shown in Fig.1.4



Source: ON Semiconductor

Figure 1.3: Source of electronic breakdowns in mixed-signal automotive ICs. (Reproduced from: [3])

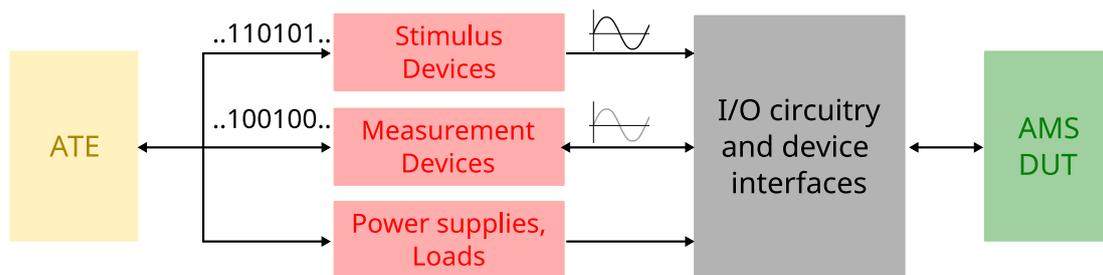


Figure 1.4: Block diagram of a test setup with automated test equipment

Testing analog circuits with Automated Test Equipment (ATE) involves complex challenges. Analog circuits require high-precision signal generation and measurement for diverse signal types which in turn requires expensive and sophisticated equipment. When compared to digital circuits, analog circuits exhibit significant variability due to factors like manufacturing processes and environmental changes, necessitating frequent calibration. Therefore achieving a high test coverage is difficult in analog circuits compared to digital circuits. Another major challenge is to make a balance between the speed of testing and the accuracy of results. Moreover, evolving fields in analog technologies like RF and mmWave require continuous efforts in updating the testing methodologies and equipment. To summarise, ATE for analog circuits demands high precision, versatility, and ongoing technological adaptation, all while managing cost

1.2 Built-In-Self-Test

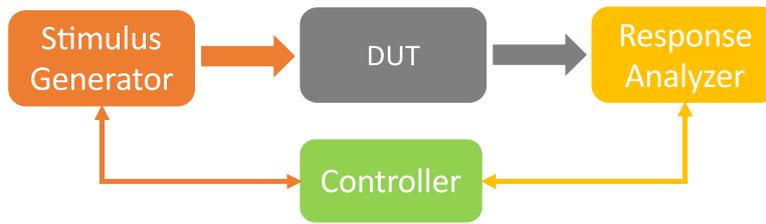


Figure 1.5: Block diagram of BIST

considerations.

1.2 Built-In-Self-Test

Built-in-Self-Test (BIST) circuits can be an effective solution to solve the challenges of AMS testing. The concept of BIST circuits dates back to the early 1960s, specifically in the context of self-testing digital evaluation equipment (STDEE) [5]. Initially, the main goals for developing an STDEE were to reduce the skill level required for maintenance, cut down repair times, and ensure maximal fault detection and isolation with minimal additional hardware. It also aims to allow self-test monitoring during the testing of the unit under test (UUT), preventing errors and failures that could harm personnel or equipment, and providing a manual self-test option for instances where the automatic self-test fails. Later, as the term BIST became popular, it was primarily developed for testing digital circuits and was aimed at shifting some of the ATE functionalities to DUTs. This shift was intended to minimize the complexity and cost of ATE equipment and improve the yield of the process.

Inspired by the success and wide adoption of digital BIST, significant research efforts have been dedicated to enable BIST solutions in the analog, mixed-signal, and RF domains. Thus, dedicated solutions have been presented in the literature for different circuit families and test applications [6–33]. In this regard, Fig.1.5 illustrates a generic BIST circuit that consists of blocks such as a stimulus generator, design under test (DUT), response analyzer, and controller. A stimulus generator generates a signal of particular characteristics that is given to DUT for testing its properties. Different types of stimuli are given to test the DUTs, such as a sine wave, square wave, triangular wave, or an arbitrary waveform that depends on the type of test to be performed. The response analyzer captures and processes the output of the DUT either in digital form or in analog. The controller is a low-cost digital ATE that controls the test operation.

1.3 Motivation

Testing of AMS circuits, such as ADCs, amplifiers, filters, SDRs, etc. depends on a clean analog signal. This analog test signal depends on the type of measurement that needs to be evaluated. For example, in the case of an ADC, a slow ramp signal is used as a stimulus to test the static parameters such as integral non-linearity (INL) and differential non-linearity (DNL). However, to test the dynamic properties of ADCs, such as Total Harmonic Distortion (THD) and Spurious-Free Dynamic Range (SFDR), a spectrally pure sinusoidal signal is used.

The focus of this thesis is to design an on-chip high-quality sinusoidal signal generator for a wide range of frequencies (MHz to GHz). It is important to comply with specific constraints when designing an analog stimulus generator for AMS-BIST applications, which are:

- **High Precision:** The generator must be capable of producing test signals with a level of linearity that surpasses that of the DUT. The high precision and good linearity do relate to a good value of THD and SFDR.
- **Programmability:** The generator should offer programmability, allowing adjustments in amplitude and frequency to align the test stimulus with the specific testing needs.
- **Minimal Footprint:** The area occupied by the generator should be kept to a minimum to preserve valuable chip real estate.
- **Complexity:** The design process should be streamlined to minimize the overall design effort and to facilitate technology migration.

1.4 Thesis Outline

Chapter 2 presents different types of sinusoidal signal generators relevant to this thesis. We discuss the advantages and disadvantages of each architecture. We also discuss why harmonic-cancellation-based architecture is well suited for a wide frequency range. In Chapter 3, the principle of harmonic cancellation is discussed in detail. In this chapter, we discuss the challenges of the harmonic principle-based generator when generating a signal for higher frequencies. We also analyze these challenges through behavioral simulations and mathematical analysis. Chapter 4 introduces three solutions that address and mitigate the challenges discussed in Chapter 3. This chapter also presents

1.4 Thesis Outline

the schematic-level simulation to validate the designs. In Chapter 5, the measurement results of one of the solutions are presented along with the discussion on results and comparison with the state-of-the-art. Finally, Chapter 6 concludes this thesis.

State of the Art

Implementing a successful Analog and Mixed-Signal (AMS) Built-In Self-Test (BIST) system hinges on developing a top-notch embedded analog signal generator. This type of generator plays an important role in stimulating the Device Under Test (DUT) effectively. In the realm of testing AMS circuits, there is a predominant need for applying analog stimuli like sine waves, triangular waves, and ramps that depend on the testing requirements. Among these signals, sinusoidal test stimuli hold importance, given their widespread application in characterizing a broad spectrum of AMS circuits. For instance, various standard techniques for testing Analog-to-Digital Converters (ADCs) rely on the precise application of sinusoidal test signals [34].

In this chapter, we embark on a comprehensive exploration of different signal-generation techniques that have emerged in recent years. Our primary focus will be on techniques that are well-suited for on-chip integration, tailored for BIST applications. The current state-of-the-art highlights numerous endeavors directed at implementing highly linear sine-wave generators [6, 29, 31–33, 35–47]. These generators can be categorized based on their architecture into two primary families: closed-loop generators and open-loop generators. Regardless of the chosen architecture, some techniques use harmonic manipulation, such as harmonic cancellation and distortion shaping, to enhance stimulus linearity while simultaneously simplifying circuit implementation.

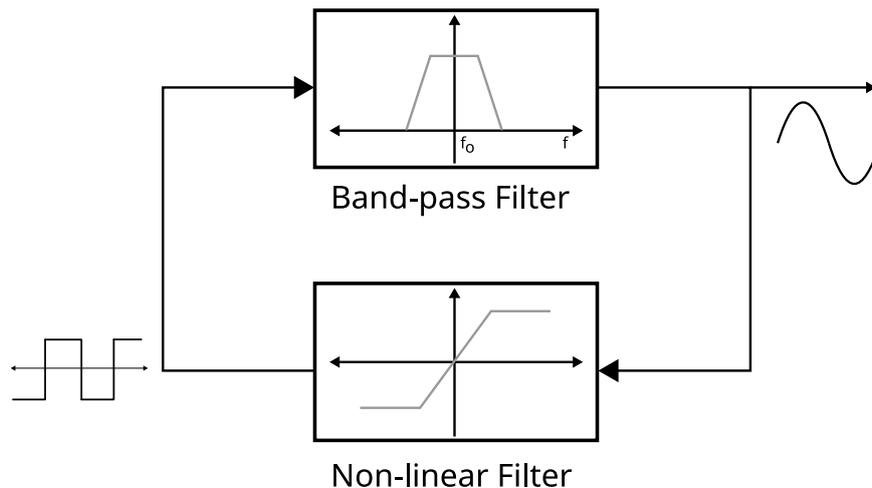


Figure 2.1: Basic block diagram of closed-loop oscillators.

2.1 Closed-Loop-Based Sinusoidal Signal Generator

One of the classical ways to generate a sinusoidal signal is by using an LC tank circuit. However, integrating such generators into BIST applications often proves challenging due to practical issues such as the complexity of design, large silicon area, power requirements, and wideband frequency generation. Figure 2.1 shows the basic block diagram of the closed-loop oscillators. The closed-loop architecture consists of a hard limiter, which is in the nonlinear feedback loop, along with a bandpass filter (BPF). The feedback converts the sinusoidal signal from the output to a square wave at the input of the BPF. A hard limiter is basically a comparator with either two or more than two output levels. The quality factor of the BPF must be high enough to reject all frequencies except the fundamental frequency. [29, 34] show that to attenuate the 3rd harmonic to -60 dB, the BPF must have a quality factor, Q-factor, of 100, which increases the design complexity and the area.

2.2 Switched-Capacitor Band-Pass Filter Oscillator

Switched-capacitor design techniques offer significant advantages when creating a high-quality band-pass filter with a substantial Q-factor. These benefits stem from the design's simplicity and its reduced susceptibility to issues like component mismatch and temperature variations. In a classical implementation described in [37], a filter-based oscillator employs a two-level limiter in combination with a switched-capacitor band-

2.3 Open-Loop Sinusoidal Signal Generator

pass filter. The measurement results in [37] show a Total Harmonic Distortion (THD) of -57 dB at the highest frequency equal to 1 MHz. The Q-factor of the BPF for this generator was 85. [30] used a four-level comparator that rejects the 3rd and the 5th harmonics, which reduces the design complexity of the BPF. The Q-factor required for this design is 10. The THD of -54.8 dB was reported in this work at an output frequency of 10 MHz.

It is important to note that this type of oscillator is most suitable for applications that operate at relatively low frequencies (in tens of MHz). This limitation arises from the design of switched-capacitor circuits that use operational amplifiers (OPAMPs) with limited frequency responses. Moreover, a major factor to consider is the substantial silicon area required for the capacitors, which can contribute to increased production costs.

2.3 Open-Loop Sinusoidal Signal Generator

Open-loop sinusoidal signal generators typically make use of digital signal processing techniques to create analog signals. The signal generation process, as conceptually illustrated in Fig. 2.2, generally involves three main components:

1. A digital pattern generator, which encodes a high-resolution digitized sinusoidal signal. These digital patterns can take the form of phase-shifted periodic signals or bitstreams.
2. A digital-to-analog (DAC) converter, responsible for translating the digital signal into the analog domain.
3. An analog filter at the output, designed to eliminate any unwanted harmonic components, such as a low-pass filter (LPF).

Unlike closed-loop oscillators, the frequency and amplitude of the generated signal can be easily controlled through digital means by configuring both the digital pattern generator and the DAC. This is in contrast to feedback-based oscillators, where signal characteristics depend on the gain of the band-pass filter. As a result, the filter requirements are significantly reduced, often requiring only a basic passive filter for the design.

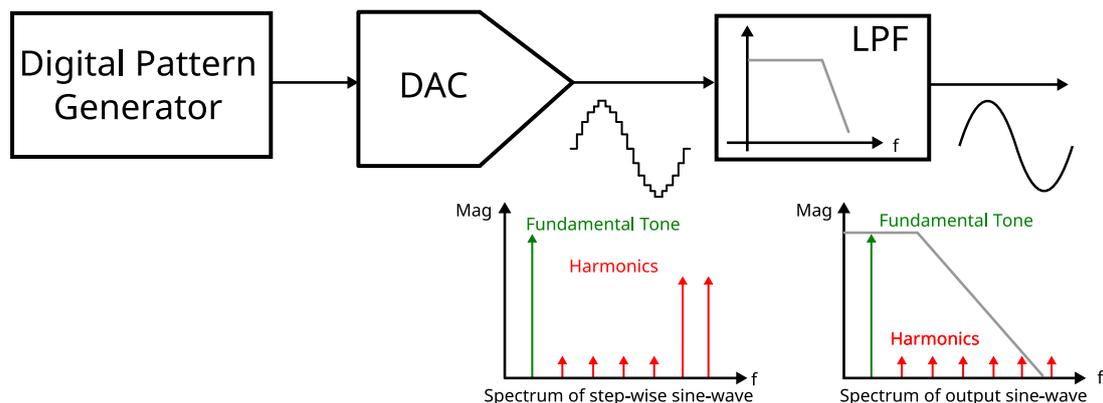


Figure 2.2: Conceptual illustration of the open-loop sinusoidal signal generator.

2.3.1 DDFS-Based Signal Generator

One of the classical architectures for sinusoidal signal generation is based on Direct Digital Frequency Synthesizer (DDFS) techniques, which were introduced in the 1970s [48]. The basic block diagram of a DDFS-based generator is shown in Fig. 2.3. It comprises a phase accumulator, followed by a Read-Only Memory (ROM), a Digital-to-Analog converter, and an output filter. The phase accumulator generates digital phases with the help of a clock signal (f_{clk}). The phase accumulator takes an m -bit Frequency Control Word (FCW) as input and generates a saw-tooth waveform representing a linearly changing phase of the sinusoidal signal. The ROM table, addressed by the phase accumulator's output, stores digital amplitude coefficients corresponding to the phase values of a single cycle of a sampled sine wave. These digital samples from the ROM are then converted into the analog domain using a DAC, resulting in an analog step-wise sinusoidal waveform. Finally, a LPF at the output attenuates unwanted harmonics, producing a linear sine wave. The frequency of the output signal depends on the FCW, the phase accumulator bit resolution (n), and the clock frequency (F_{clk}), as indicated by the formula.

The frequency of the output signal is given by the formula:

$$f_{\text{out}} = \frac{FCW \cdot f_{\text{clk}}}{2^n} \quad (2.1)$$

The spectral purity of the conventional DDFS-based generator is determined by the ROM's resolution. Unfortunately, a higher resolution leads to a larger ROM size, resulting in an increased area that results in slower access times. To address this issue, several optimization techniques have been developed. Some of these techniques take

2.3 Open-Loop Sinusoidal Signal Generator

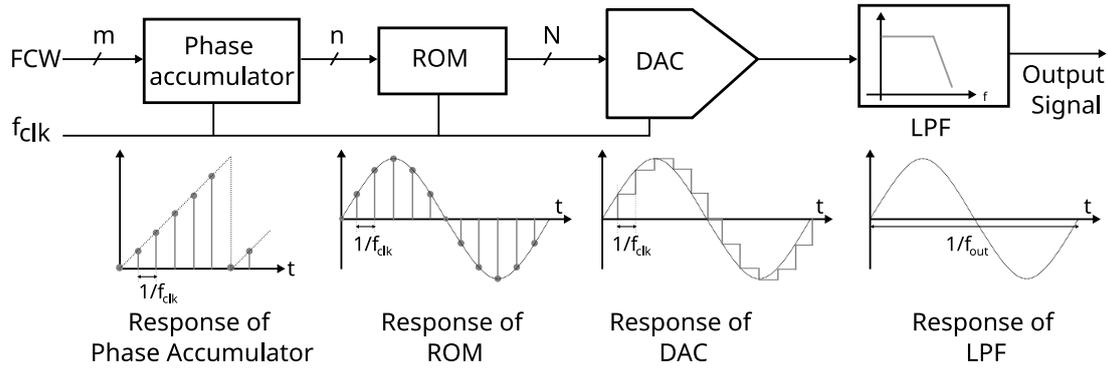


Figure 2.3: Basic block diagram of a DDFS-based signal generator.

advantage of the sinusoidal signal's symmetric characteristics and store only a quarter of a single period (from 0 to $\pi/2$) to reconstruct the entire signal (0 to 2π), reducing the number of samples and ROM size by a factor of four compared to the conventional approach [49].

Another optimization method aims to reduce the number of phase points used in the phase accumulator without degrading the output signal's linearity. This is achieved through techniques like the Sunderland sine-wave approximation method [50]. Various works [50, 51] have shown that this approach can compress the ROM size by a significant factor compared to the conventional generation technique. The results in [51] show a compression ratio of 165, and in [50], it is 51 when compared to a conventional technique.

Additionally, there are ROM compression techniques based on the Taylor approximation method discussed in [52, 53], which relies on linear interpolation between sine samples. These methods have also demonstrated significant ROM size reductions. [52] reports a compression ratio of 157, and [53] reports 64. [54–56] have used an algorithm based on the CORDIC (Coordinate Rotation Digital Computer [57]) algorithm, which led to further reducing the ROM size.

Despite these efforts to minimize ROM size, DDFS-based generators remain costly in terms of area, particularly for Built-In Self-Test (BIST) applications. Moreover, the linearity of the generated sinusoidal signal can be influenced by factors such as the linearity of DACs and output filter characteristics, which may degrade due to mismatch and technological variations. To address these challenges, various solutions have been proposed.

Work in [58, 59] discusses pre-distorting the original input sequence to match the noise shape with the DAC's characteristics, based on an estimation procedure. Another

approach discussed in [60] suggests using on-chip measurement instruments to measure the magnitudes and phases of unwanted harmonics, and with the help of feedback, the calibrations can be done. However, this method requires measurement equipment with higher accuracy and linearity than the DAC to be compensated. Otherwise, the estimation procedure may incorrectly attribute certain components to the DAC, potentially worsening its performance by introducing unnecessary terms. The work in [61–63] presents a ROM-less DDFS architecture. [61] presents a low-power DDFS architecture with a maximum operating frequency of 1.3 GHz. The unique hybrid design enhances traditional nonlinear digital-to-analog converters by combining a linear slope component with the approximated sine wave generated from a nonlinear DAC through an additional linear DAC. [62] presents a novel approach for a ROM-less DDFS utilizing a linear DAC and an analog triangle-to-sine converter (TSC), offering significant power savings compared to conventional ROM-based and nonlinear DAC-based DDFSs. The DDFS covers a wide bandwidth from DC to 2.5 GHz, achieving an SFDR of over 48 dBc at low frequencies and 45.7 dBc at 2.5 GHz. [63] This paper presents a based on a nonlinear DAC. The results show an SFDR of 55.1 dBc at 660 MHz. [61, 63] are implemented in CMOS process, and [62] is implemented in 0.350 μm Bi-CMOS technology.

2.4 $\Sigma\Delta$ -Based Signal Generator

The architecture of the $\Sigma\Delta$ -based generator, as illustrated in Figure 2.4, primarily focuses on reducing the demands of highly accurate and linear Digital-to-Analog Converters (DACs) by utilizing a single-bit optimized bitstream. The generation strategy relies on the noise-shaping characteristics of the $\Sigma\Delta$ encoding technique. Initially, a 1-bit $\Sigma\Delta$ -encoded version of an N-bit digital signal is created, which is subsequently transformed into the analog domain using a 1-bit DAC. At the output, an analog low-pass filter (LPF) is employed to reconstruct the sinusoidal signal. To effectively minimize shaped quantization noise and retain only the fundamental tone at the output, the order of the output LPF should be large enough to suppress the noise at higher frequencies due to the $\Sigma\Delta$ bitstream. The quality of the output signal is heavily influenced by the spectral content of the optimized $\Sigma\Delta$ bitstream [8, 9].

In literature, the $\Sigma\Delta$ bitstream generator can be realized using two distinct approaches. The first approach relies on a memory of the system where a segment of the $\Sigma\Delta$ -encoded signal is stored and periodically reproduced. The memory-based $\Sigma\Delta$ generator generally utilizes a Linear Feedback Shift Register (LFSR) with its output

2.5 Switched Capacitor-Based Signal Generator

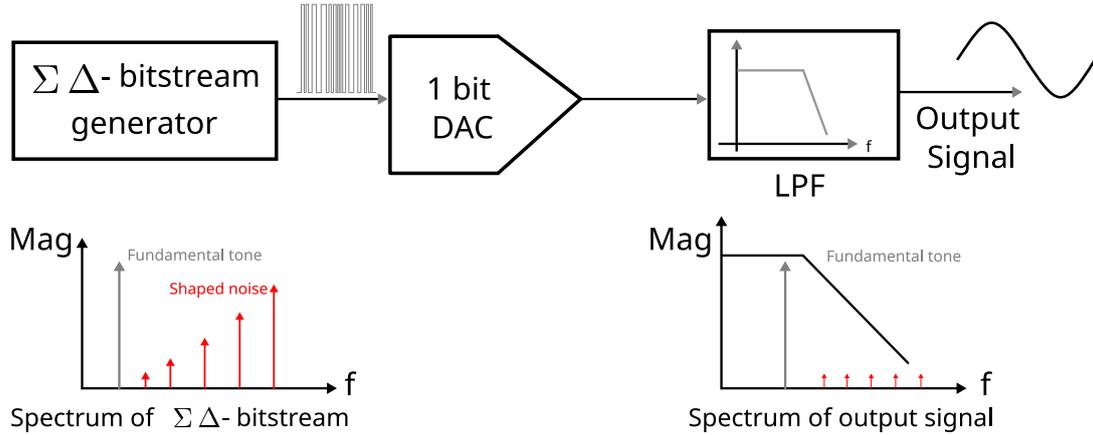


Figure 2.4: Basic block diagram of a $\Sigma\Delta$ -based signal generator.

looped back to the input, alongside a 1-bit DAC, which can be as simple as a digital buffer [6, 64]. This approach offers several advantages, including modulator speed and reduced circuit area. Work in [6, 36] has shown improvement in generating a more precise output signal by increasing the resolution of the $\Sigma\Delta$ bitstream, either by employing an LFSR with an extended length or by substituting the LFSR with a RAM.

On the other hand, the second approach takes the form of a closed-loop oscillator approach. It involves implementing a $\Sigma\Delta$ modulator within a gain loop configuration, alongside a digital resonator that generates an N-bit sinusoidal signal. The amplitude and phase of this signal are determined by the initial value stored in multi-bit registers [35]. This implementation offers high precision and superior frequency resolution. However, both implementations are constrained by the linearity of the filter and necessitate the design of a filter with high selectivity. For instance, in [35], a 6th-order filter was required to implement a $\Sigma\Delta$ -oscillator-based generator, effectively attenuating the shaped quantization noise.

2.5 Switched Capacitor-Based Signal Generator

Switched capacitor-based (SC-based) generators employ a programmable gain element with a DC input, functioning as a straightforward Digital-to-Analog Converter, to create a step-wise sinusoidal waveform, as shown in Figure 2.5. The linearity of the resulting sinusoidal output primarily depends on the quantity and precision of the step levels employed to build the signal. Nevertheless, enhancing the number of step levels entails an escalation in signal paths, consequently increasing the overall design complexity of

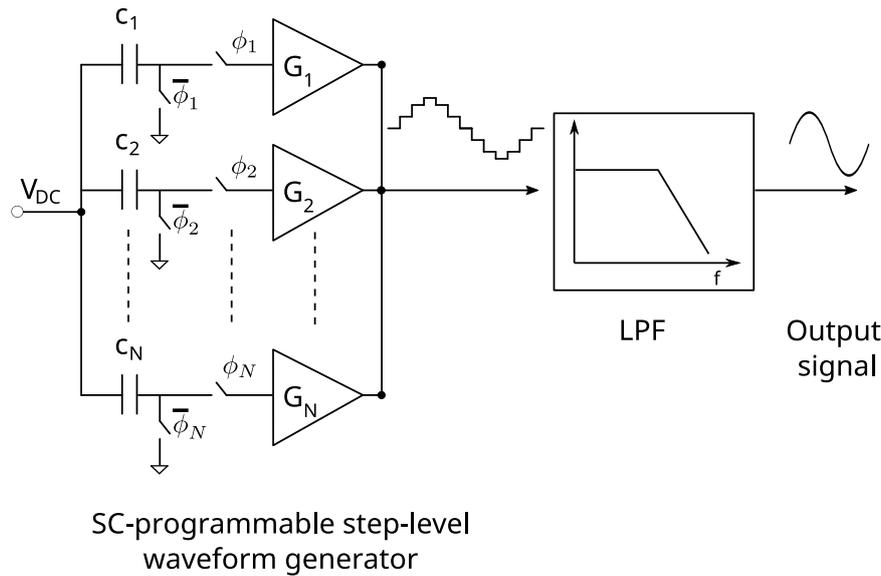


Figure 2.5: Basic block diagram of a switched capacitor-based signal generator.

the circuit.

Authors in [65, 66] have used a programmable SC-VGA (Switched Capacitor Variable Gain Amplifier) to create step-wise sinusoidal signals. Each gain step corresponds to an ideally sampled sine-wave value. This implementation offers advantages in terms of simplicity, compactness, and easy control of signal frequency and amplitude. However, concerning the linearity of the output signal, its performance is constrained by the accuracy and number of step levels, as well as the selectivity of the output filter. Enhancing the spectral purity of the output would require implementing more signal paths and using a highly selective filter with smooth characteristics, which in turn increases design complexity and area overhead.

Another approach that has been explored in [39, 67] is SC-filter-based generators. The basic principle in this approach is the integration of the generation and filtering stages to minimize the area overhead. In [39] and [67], a second-order low-pass filter is introduced, with input capacitors that have been modified to incorporate programmable capacitors. The linearity of the resulting sinusoidal output is heavily reliant on the linearity of the filter, as well as the quantity and precision of the generated step levels.

The results in [66] show a signal at 1 KHz having all harmonics below -60 dB and a signal-to-noise ratio of 60 dB. In [67], the reported Spurious-Free Dynamic Range (SFDR) of the output sinusoidal signal is 70 dB at 62.5 KHz frequency. Authors in [39] have reported a sinusoidal signal with 70 dB of SFDR at 40.7 MHz frequency.

2.6 The Distortion-Shaping Technique

The distortion-shaping technique, initially developed to enhance the linearity of low-cost external Arbitrary Waveform Generators (AWGs) [68, 69], compensates for non-linearity in analog and mixed-signal components within the generator’s signal path. It achieves this by strategically interleaving time-shifted variations of the desired sinusoidal signal. This process causes intermodulation products produced by subsequent non-linear components to shift low-order harmonics to higher frequencies, effectively relocating them from the primary signal tone. This approach simplifies the design of the generator’s output filter.

In this technique, instead of supplying the filter with a pure sinusoid, a signal is generated by alternating samples from two time-interleaved sinusoids. This signal composition cancels out third-order harmonic distortion originating from the non-linear filter. The distortion is shifted to higher frequencies, simplifying its removal through filtering. It is worth noting that the frequencies of these components depend on the sampling frequency used. This method can be extended to cancel out other harmonic components by using appropriately time-shifted versions of the original sinusoid.

The experimental results demonstrate a significant suppression (85 dBc) of third-order harmonic components at 1 MHz using AWGs [68, 69]. However, adapting this technique for higher frequencies can be challenging. These challenges can arise due to the necessity of a DAC operating at a higher sampling frequency, implementing it on an integrated chip, and ensuring a perfect time shift between two (or more) sinusoidal signals at the input.

2.7 Harmonic Cancellation-Based Signal Generator

The harmonic cancellation (HC) technique is based on combining a set of time-shifted and scaled versions of a given periodic signal. In this process, the most significant harmonics are canceled while retaining the fundamental frequency component at the output. The block-level representation of a harmonic cancellation-based generator is shown in Figure 2.6. $X_1(t)$, $X_2(t)$, etc., are the time-shifted periodic signals. These signals are first scaled by weights α_1 , α_2 , etc., and then added. In this process, lower-order harmonics of the periodic signal are canceled. The signal is then passed through a low-pass filter to attenuate the higher-order harmonics that couldn’t be canceled in the previous stage. The number of harmonics that can be canceled depends on the number of time-shifted signals, time-shift values, and the scalar weights. These scalar weights can be rational or irrational numbers, depending on the time-shift values and

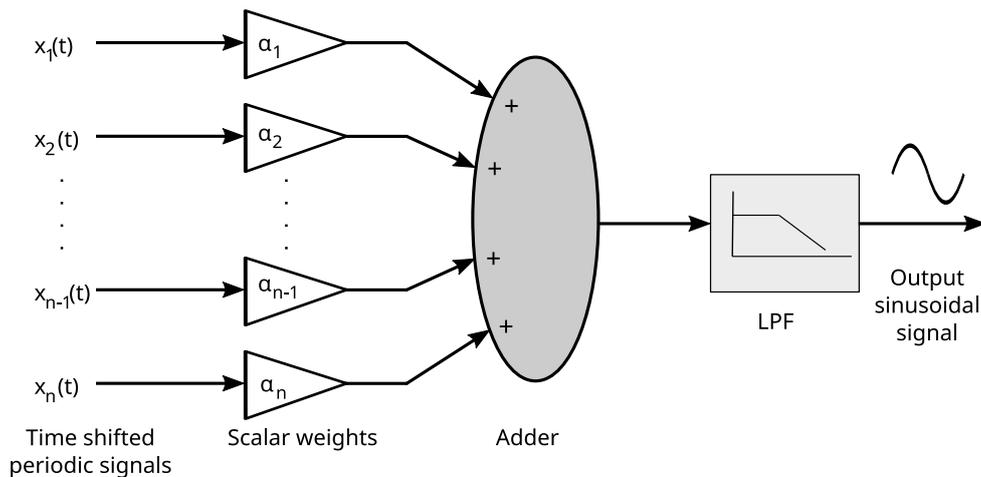


Figure 2.6: Block diagram of a harmonic cancellation-based signal generator.

the number of time-shifted signals [44]. A detailed discussion of harmonic cancellation-based generators and a mathematical explanation are provided in Chapter 3.

There are two approaches for generating these time-shifted signals. The first approach involves a digital counter, which requires an external clock or a locally generated clock signal. In this case, the frequency of the output sinusoidal signal is always less than that of the input clock signal and depends on the number of counter stages. This approach is digital-friendly and easily adaptable across different technologies. However, the limitation of this approach is that to generate an output sinusoidal signal at frequencies in the GHz range, the digital counter must operate at higher frequencies (which is equal to the number of stages of the digital counter times the required output frequency). This need for speed becomes a constraint due to the inherent limitations of digital circuits. The second approach involves using an N-stage ring oscillator. This oscillator can be designed to operate within the required output frequency range, addressing the limitation associated with the previous method. However, this technique is not as digital-friendly and necessitates careful layout design.

Regarding the scaling and adding of these time-shifted signals, two approaches exist in the literature. The first approach for scaling is with the help of a resistor-based network, and the second approach is based on a weighted DAC. In both cases, the signals are added with the help of a capacitor.

Authors in [31] have used digital circuits to generate time-shifted signals using a clock signal generated from a ring oscillator. A resistor-based network is used for scaling and summing these time-shifted signals, followed by a low-pass filter to attenuate the higher-order frequencies. In this work, a signal with -72 dB Total Harmonic Distor-

2.7 Harmonic Cancellation-Based Signal Generator

tion (THD) is reported at an output frequency of 10 MHz. As we know, analog circuits can be heavily impacted by mismatches and process variations, and these variations can affect the sinusoidal signal generator when exposed to the mismatch in time-shift values and scalar weights. To overcome this, some works have used calibration circuits along with the signal generator. Authors in [32] have proposed an interesting work on a sinusoidal signal generator in which they have used a calibration circuit. The calibration circuit is used to correct the mismatch in the time-shift value and the duty cycle of the signals. These time-shifted signals are generated with the help of a ring oscillator, and these signals are scaled with the help of a resistor-based network. The measurement results show a THD of -54.9 dB at 150 MHz and -62.6 dB at 850 MHz after optimization. A digitally controlled calibration-based resistor network for scaling and summing the time-shifted signals is proposed in [70]. The statistical simulation results show an improvement in the THD if the mismatch is dominated by scalar weights. In [45], the authors have used a partial dynamic element matching technique which helped in reducing the impact of the process and mismatch variations in the DAC stage where the time-shifted signals are amplified and added. The results show a Spurious-Free Dynamic Range (SFDR) of 69 dB at 2 MHz. In [47], the authors have reported another scheme in which they have used current steering DACs which can be calibrated externally for scaling and adding the time-shifted signals. The time-shifted signals are generated using a shift register. The measurement results show an average SFDR of 50 dB for frequencies ranging from 1 MHz to 333 MHz. The work in [43] proposed a new approach to implement the irrational scalar weights precisely, which is coupled directly with the output's linearity. In this work, the authors unveil an irrational coefficient generator using skew-circulant matrices (SCMs). The results show that at 0.8 MHz, the SFDR is 66.4 dB, and it is 38.4 dB at 100 MHz.

The generators based on the harmonic cancellation technique can offer several advantages compared to other techniques discussed above. They provide flexibility in attenuating the set of harmonics present in the frequency spectrum of the output signal without the need for additional hardware, as seen in the case of DDFS-based generators. However, some works in DDFS have proposed a ROM-less architecture, which can simplify the design and reduce the need for extensive memory resources. It is important to note that while ROM-less DDFS architectures have their merits, they typically have a limitation: the output frequency that can be generated often remains half of the input clock frequency. This constraint can impact their suitability for applications requiring high-frequency sinusoidal signals. Additionally, it is worth mentioning that DDFS-based generators, including ROM-less designs also consume more power compared to other generator techniques. The power consumption can be influenced by

factors such as the complexity of the architecture, the frequency of operation, and the requirement of high-speed DACs at the output. Despite these considerations, harmonic cancellation-based generators offer an efficient and flexible alternative for achieving clean and precise sinusoidal waveforms without the limitations associated with some other generator types.

Harmonic cancellation principle and its challenges

3.1 Harmonic cancellation

The Harmonic cancellation technique is based on combining a set of delayed and scaled versions of a given periodic signal in order to cancel out the most significant undesired harmonic components while retaining the fundamental frequency component at the output [58]. One can generate the signal with fundamental frequency by using any type of periodic signal. A periodic signal such as a sawtooth, triangular, and square wave consists of harmonics in its frequency spectrum as shown in Fig. 3.1. Properties of signals such as odd signal, even signal, duty cycle, and neither odd nor even signal define the power of harmonics in the frequency spectrum. For example, in case of a sawtooth-type signal, all harmonics are present, in case of a triangular-type signal only odd harmonics are present, similarly in case of a square-type signal which has a 50% duty cycle, only odd harmonics are present. Generating time-shifted signals of sawtooth and triangular waves for harmonic cancellation is not straightforward. Moreover, generating time-shifted square wave signals is relatively easier using a ring oscillator, especially for higher frequencies (up to a few GHz).

A periodic signal can be represented using Fourier expansion. Let us consider $x(t)$ a periodic signal whose Fourier expansion is:

Harmonic cancellation principle and its challenges

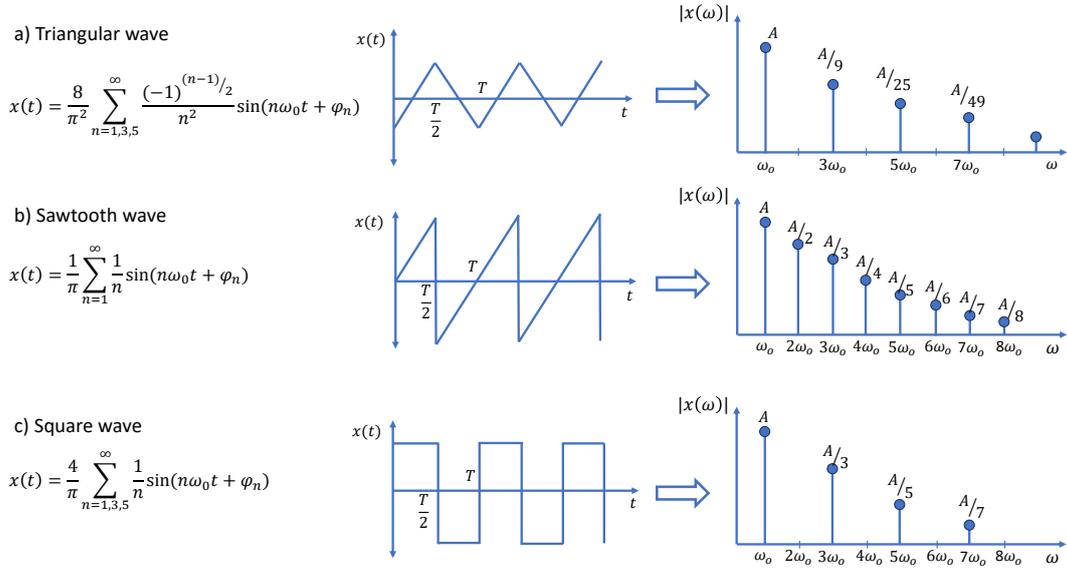


Figure 3.1: Different types of periodic signals with their frequency spectrum.

$$x(t) = \sum_{n=1}^{\infty} A_n \cos(n\omega_0 t + \theta_n) \quad (3.1)$$

where, A_n , θ_n , and ω_0 are the amplitude, the phase of n^{th} harmonic, and the fundamental radian frequency of signal $x(t)$ respectively. To understand the harmonic cancellation principle mathematically, let us define another signal $y(t)$ which is the linear combination of time-shifted and scaled version of signal $x(t)$:

$$y(t) = \alpha_0 x(t) + \sum_{i=1}^p \alpha_i [x(t + \Delta t_i) + x(t - \Delta t_i)] \quad (3.2)$$

where $x(t)$ is scaled by α_0 and p pairs of time-shifted signals with opposite time shift values Δt_i and $-\Delta t_i$ (can also be represented by phase shift values when converted in radians) with respect to the reference signal $x(t)$. These time-shifted signals are then scaled by α_i . After solving equation 3.1 and 3.2,

$$y(t) = \sum_{n=1}^{\infty} A_n \left[\alpha_0 + 2 \sum_{i=1}^p \alpha_i \cos(n\phi_i) \right] \cos(n\omega_0 t + \theta_n) \quad (3.3)$$

where, $\phi_i = \omega_0 \Delta t_i$.

3.1 Harmonic cancellation

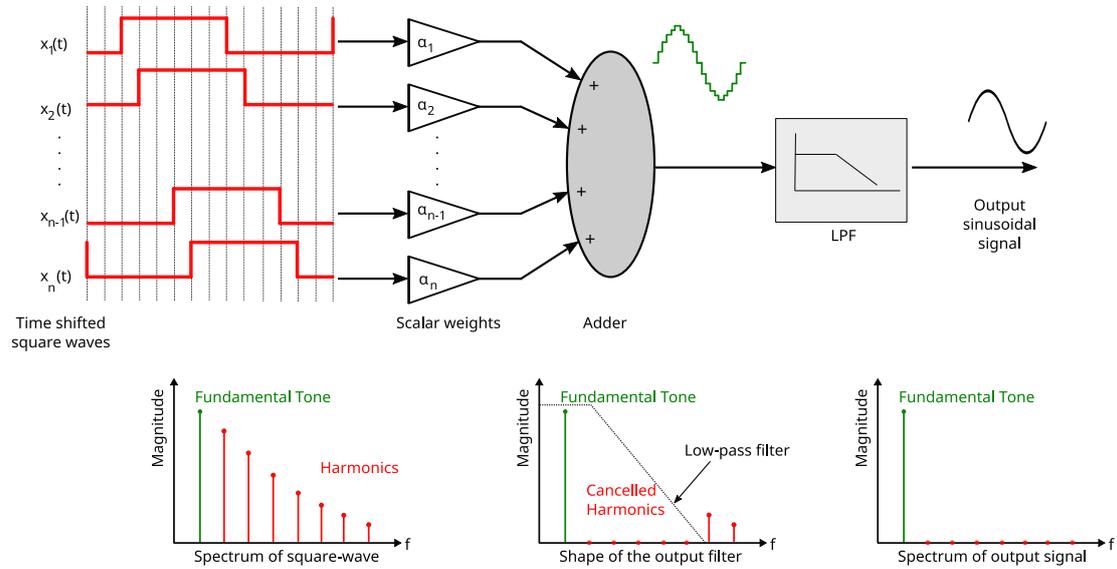


Figure 3.2: Harmonic cancellation based sinusoidal signal generator

In equation 3.3, signal $y(t)$ which is the combination of the scaled version of time-shifted signal $x(t)$ shows a similar frequency spectrum as signal $x(t)$. However, the amplitude of the harmonics of signal $y(t)$ is also scaled with a coefficient $\alpha_0 + 2 \sum_{i=1}^p \alpha_i \cos(n \phi_i)$, which is a function of the scalar weights and the phase shift values. If these scalar weights and the phase difference values are chosen correctly, a set of harmonics can be attenuated or completely canceled. The harmonic cancellation technique can be understood from Fig. 3.2 which is the block-level representation of the mathematical equation 3.2. The time-shifted square wave signals with 50% duty cycle (no even harmonics present in the frequency spectrum) are scaled with scalar weights, and then added. In this process, some of the harmonics of the signal are canceled. The number of harmonics that can be canceled depends on the number of time-shifted signals and the value of the scalar weights, and this defines the complexity of the design. After adding these signals, the generated output signal is then passed through a low pass filter (LPF), that attenuates the harmonics which are non-cancellable.

3.1.1 Generation of time-shifted signals

There are multiple ways by which the time shift values and the scalar weights are generated. In case of the time-shifted signals, some work has proposed to use an N-bit shift register that operates at a particular frequency and generates the number of time-shifted signals [44, 45, 47, 70], also shown in Fig. 3.3. In addition to this, an additional

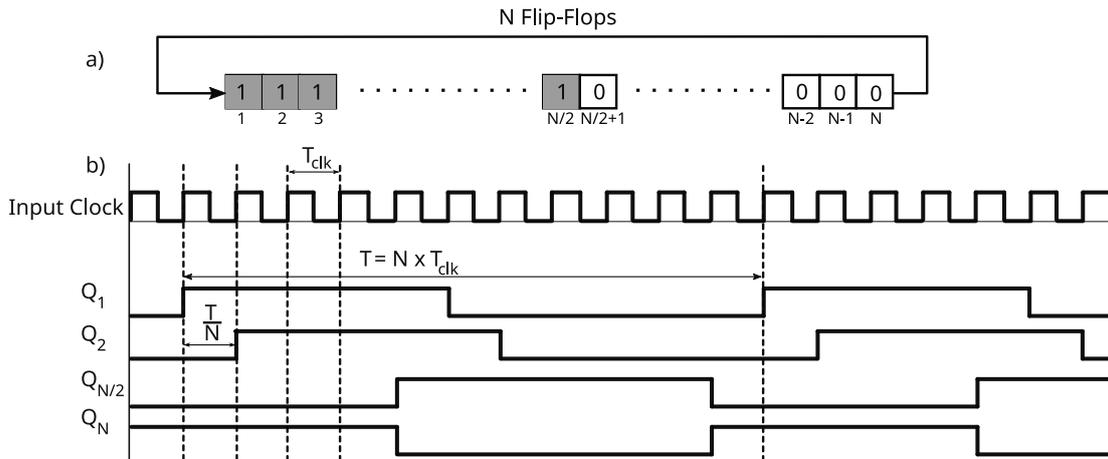


Figure 3.3: a) Block level representation of N flip-flops; b) Generation of time-shifted signals

clock is required for this type of generation, and the output signal frequency gets divided by the number of stages of the shift register which is F_{clk}/N . This approach is digital friendly, simple D-flipflops with preset/set functionality are required along with an external clock. However, when targeting a high-frequency output signal in the order of a few GHz, this approach poses difficulties, firstly, the requirement of an input clock signal of a very high frequency. Secondly, the flip-flops should be able to function at a higher frequency.

Another approach by which these time-shifted signals can be generated is by using a ring oscillator, where the phase difference depends on the number of stages of the ring oscillator [32, 71–73], also illustrated in Fig. 3.4. In this case, when used for sinusoidal signal generation, the frequency of the output signal remains the same as the fundamental frequency of the signal and a high-frequency sinusoidal can be generated. However, the challenges of this type of generation are the need for a careful design and layout of the oscillator which needs to be done manually ensuring as less as possible systematic mismatch in time shift and duty cycle.

3.1.2 Scaling and summing stage

There are two types of scaling and summing architectures that have been proposed in the literature. The first architecture is based on weighted current steering DACs [43, 46], and the second architecture is based on the weighted summing networks [31, 32, 71–73]. A weighted current steering DAC based adder is as shown in Fig. 3.5, and a

3.1 Harmonic cancellation

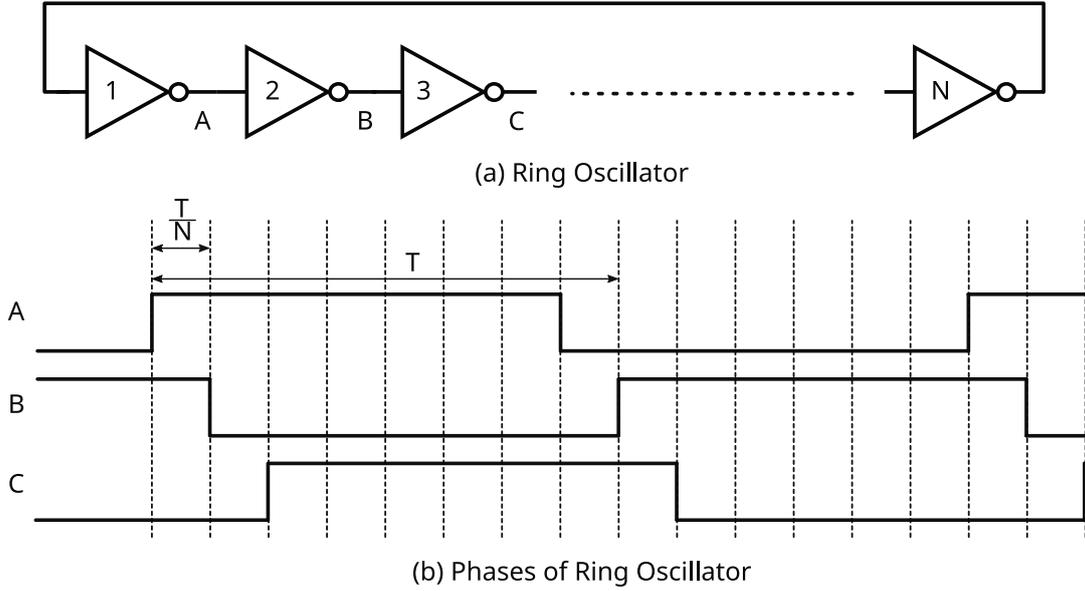


Figure 3.4: Generation of time-shifted signals with N stage ring Oscillator

weighted resistor based adder is shown in Fig. 3.6. A summing network based on a weighted resistor generates a proportionate current with the help of a digital buffer for a particular phase. Then all currents generated from these phases are added to a capacitor. The output of the summing network is connected to LPF so that the higher harmonics are canceled. Similarly, in the case of the DAC-based summing network, all phases control the weighted currents. All currents from each path are then added to a capacitor followed by LPF. However, designing a high-speed DAC-based adder circuit can be complex when operating at frequencies in the GHz range [74], while a weighted resistor-based adder can be a simpler choice for high-frequency sinusoidal signal generation. The weighted resistor-based adder can be impacted by the process and mismatch variations, but different matching techniques are used in such a way that these variations can be minimized. This is also discussed in chapter 5.

As discussed above in equation 3.3, the number of phase-shifted signals and the value of weights can decide the number of harmonics that can be canceled by making the coefficient $\alpha_0 + 2 \sum_{i=1}^p \alpha_i \cos(n\phi_i)$ to zero. Several combinations of phase difference and scalar weights have been explored in literature [32, 44]. One of the combinations to solve equation 3.3 for harmonics cancellation is when α_0 is set to 1 while other scalar

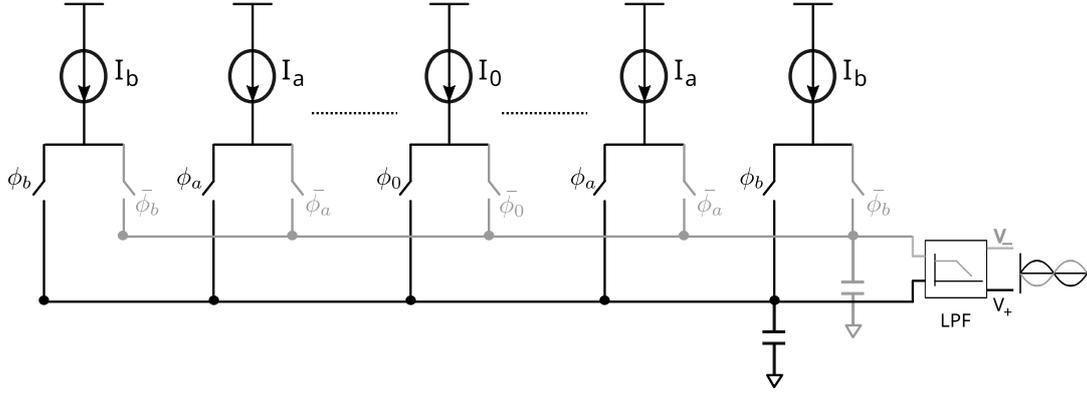


Figure 3.5: Weighted current steering DAC-based adder

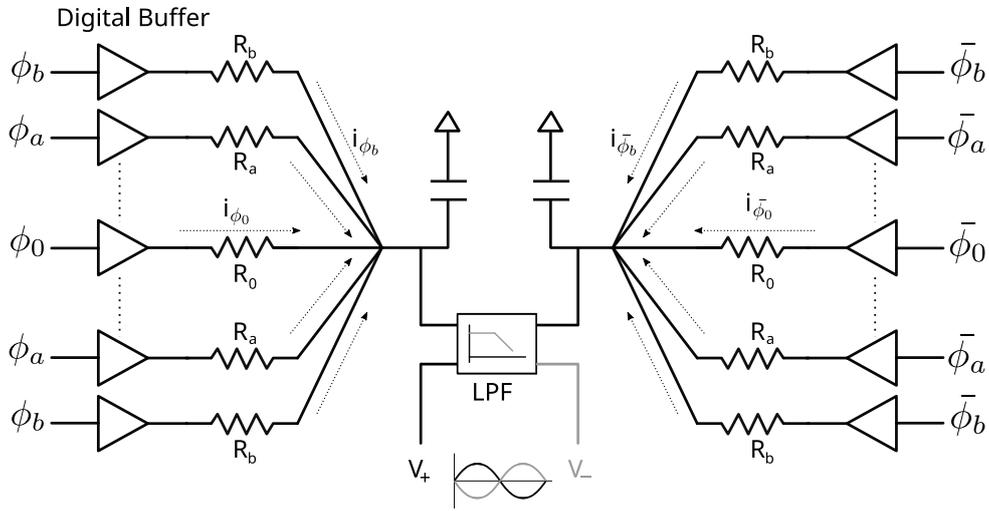


Figure 3.6: Weighted resistor based adder

weights and phases can be calculated by the following relation:

$$\begin{cases} \phi_i = i \frac{2\pi}{4(p+1)}, & 1 \leq i \leq p \\ \alpha_i = \cos\left(i \frac{2\pi}{4(p+1)}\right), & 1 \leq i \leq p \end{cases} \quad (3.4)$$

This relation allows the cancellation of a given set of lower order odd harmonics of the square wave signal $x(t)$, which are lower than the $2(2p+1)^{th}$ order, while the non-cancellable higher harmonics are attenuated with the help of LPF. Table 3.7 summarizes the phase shift and the scalar weights required for a p pair of square wave signals so that

3.2 Effect of timing inaccuracies in HC

p	N	Phase-shifts (ϕ_i)				Scalar weights (α_i)					1 st NC*
		ϕ_1	ϕ_2	ϕ_3	ϕ_4	α_0	α_1	α_2	α_3	α_4	
1	3	$\frac{\pi}{4}$	-	-	-	1	$\frac{1}{\sqrt{2}}$	-	-	-	7
2	5	$\frac{\pi}{6}$	$\frac{\pi}{3}$	-	-	1	$\frac{\sqrt{3}}{2}$	$\frac{1}{2}$	-	-	11
3	7	$\frac{\pi}{8}$	$\frac{\pi}{4}$	$\frac{3\pi}{8}$	-	1	$\sqrt{\frac{2+\sqrt{2}}{4}}$	$\frac{1}{\sqrt{2}}$	$\sqrt{\frac{2-\sqrt{2}}{4}}$	-	15
4	9	$\frac{\pi}{10}$	$\frac{\pi}{5}$	$\frac{3\pi}{10}$	$\frac{2\pi}{5}$	1	$\sqrt{\frac{5+\sqrt{5}}{8}}$	$\frac{\sqrt{5}+1}{4}$	$\sqrt{\frac{5-\sqrt{5}}{8}}$	$\frac{\sqrt{5}-1}{4}$	19

NC* - Non-cancellable harmonic

Figure 3.7: Generation of time-shifted signals with N stage ring Oscillator

a certain number of harmonics can be canceled. N defines the total number of signals required for a particular case.

It can be observed in the table that to cancel higher harmonics the number of phase-shifted signals is higher which shows a trade-off between the number of harmonics that can be canceled and the complexity of the generation of phase-shifted signals. A good trade-off that has also been explored in previous works [32, 46, 75] consists in using 2 pairs of signals (total 5 square wave signals) which can cancel all odd harmonics below the 11th harmonic. As illustrated in Fig.3.8, if A, B, C, D, and E are five signals, assuming signal C as the reference signal, then ϕ_{CX} is the phase difference between signal C and signal X. In this case, $\phi_{CA} = -\frac{\pi}{3}$, $\phi_{CB} = -\frac{\pi}{6}$, $\phi_{CD} = \frac{\pi}{6}$, and $\phi_{CE} = \frac{\pi}{3}$ or we can also say that all five consecutive signals are time shifted by $\frac{T}{12}$. Signal C is scaled by weight $\alpha_0 = 1$, signals A, E are scaled by weight $\alpha_2 = \frac{1}{2}$, and signals B, D are scaled by weight $\alpha_1 = \sqrt{\frac{3}{2}}$. A block diagram representation of a HC-based sinusoidal signal generator based on five phase signals is shown in Fig. 3.9.

3.2 Effect of timing inaccuracies in HC

The fabrication of integrated circuits in current technologies has its own challenges in the form of mismatch and process variations that can limit the performance of many

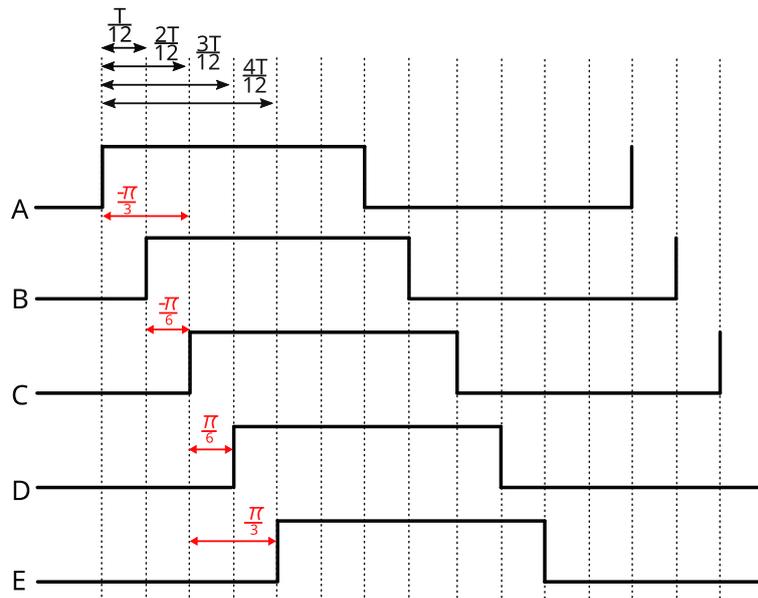


Figure 3.8: 5 time-shifted signals that cancel all odd harmonics below the 11th harmonic

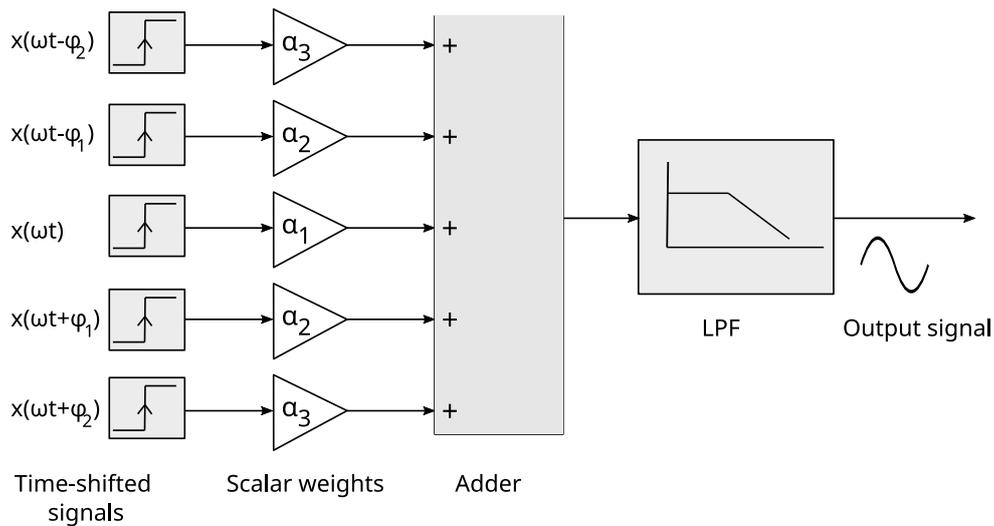


Figure 3.9: Block diagram of signal generator with 5 signals, time-shifted by $\frac{T}{12}$

circuits and systems. These variations can affect the performance of the harmonic cancellation by deviating the critical parameters such as the scalar weights, duty-cycle, and phase difference from the ideal values defined by equation 3.4. In this section, the effect of the main non-idealities that can degrade the performance of the harmonic cancellation will be discussed. The work in [45, 46, 76, 77] discussed these non-idealities in the

3.2 Effect of timing inaccuracies in HC

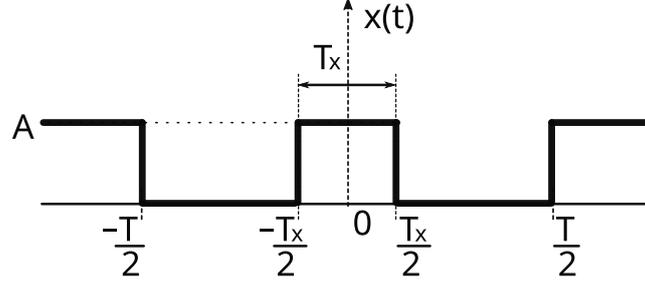


Figure 3.10: Square wave signal with time period equal to T and on-time equal to T_x

case of low-frequency scenarios, resulting in a predominance of the weight mismatch as the main cause of linearity degradation. This section focuses on understanding the challenges involved when HC-based signal generators are used for generating high-frequency signals.

Let us consider a signal $x(t)$ as shown in Fig. 3.10, with a time period equal to T . The signal is high for a time T_x that defines the duty cycle of the signal equal to $T_x * \frac{100}{T}$. Using Fourier expansion, $x(t)$ can be represented as equation 3.5, where a_0 is the dc component of the signal, n is the number of harmonics, ω_0 is the angular frequency of the signal which is equal to $\frac{2\pi}{T}$, a_n and b_n are coefficients of n^{th} harmonics.

$$x(t) = a_0 + \sum_{n=1}^{\infty} [a_n \cos(n\omega_0 t) + b_n \sin(n\omega_0 t)] \quad (3.5)$$

where $a_0 = \frac{AT_x}{T}$, $b_n = 0$ (because $x(t)$ is an even function), and $a_n = \frac{2A}{n\pi} \sin\left(\frac{n\pi T_x}{T}\right)$.

$x(t)$ can be written as:

$$x(t) = \frac{AT_x}{T} + \sum_{n=1}^{\infty} \frac{2A}{n\pi} \sin\left(\frac{n\pi T_x}{T}\right) \cos(n\omega_0 t) \quad (3.6)$$

Let us assume for simplicity that the DC component is zero ($a_0 = 0$), and the amplitude of the signal is unity ($A = 1$), $x(t)$ can be written as:

$$x(t) = \sum_{n=1}^{\infty} \frac{2}{n\pi} \sin\left(\frac{n\pi T_x}{T}\right) \cos(n\omega_0 t) \quad (3.7)$$

Solving equation 3.2 and 3.7:

$$y(t) = \sum_{n=1}^{\infty} \frac{2}{n\pi} \sin\left(\frac{n\pi T_x}{T}\right) \left[1 + \sum_{i=1}^p 2\alpha_i \cos\left(\frac{2n\pi \Delta t_i}{T}\right) \right] \cos(n\omega_0 t) \quad (3.8)$$

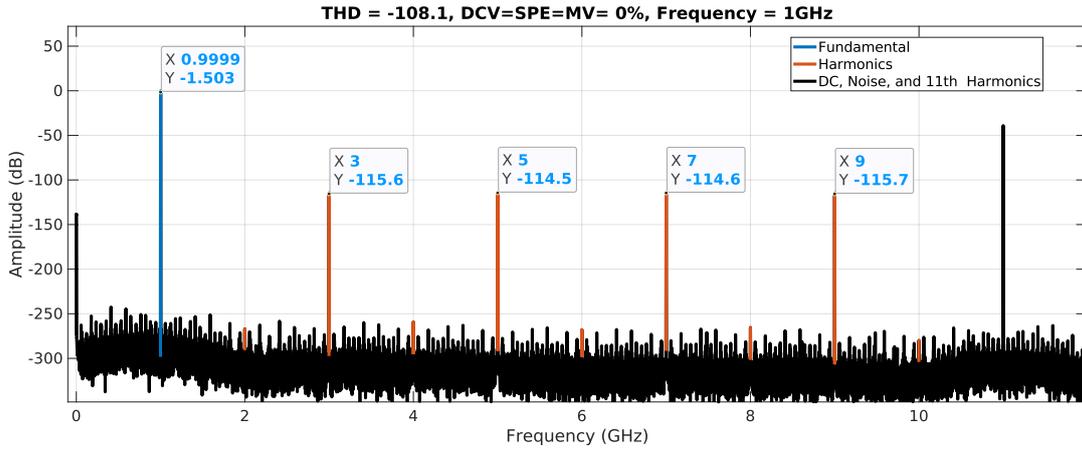


Figure 3.11: Spectrum of the ideal sinusoidal signal generated from the 5 phases based HC based sinusoidal signal generator

The first observation from equation 3.8 can be made that if the duty cycle is 50%, $\sin \frac{n\pi T_x}{T}$ is always 0 for all even harmonics. This means that ensuring a 50% duty cycle cancels all even harmonics. The second observation is that if there is a mismatch in the duty cycle which means T_x is not equal to $\frac{T}{2}$, all even harmonics will be present in the generated output sinusoidal signal. This will degrade the quality of the output signal. Similarly, if there are mismatches in the scalar weights (α_i) and time shifts (Δt_i), then odd harmonics will not cancel completely which will also degrade the quality of the output signal as well. With respect to these mismatches, three terminologies are defined in this section: duty cycle variation (*DCV*), static phase error (*SPE*), and mismatch variation (*MV*). The *DCV* and *SPE* are called timing inaccuracies because they depend on the time period of the signal which will be explained in the next section.

To understand the impact of these variations on the sinusoidal signal generator based on harmonic cancellation, a behavioral model of the signal generator similar to Fig. 3.9 with a first-order LPF is simulated on MATLAB. The mismatch and process variations are random, so the worst-case condition for a signal generator is considered in the shown results. As discussed earlier, we will consider 5 square wave signals, and the mismatch can either increase or decrease the parameters of the signal generator, which are phase difference, duty cycle, and scalar weights. For each parameter, there are 2^5 combinations, out of these 32 combinations, the worst combination was selected using MATLAB simulation. In the ideal case when no mismatch is present in the signal generator, the *THD* of the output signal is -108 dB, as all harmonics are well below -115 dB, as shown in Fig. 3.11. The *THD* of the output signal with no mismatch in the

3.2 Effect of timing inaccuracies in HC

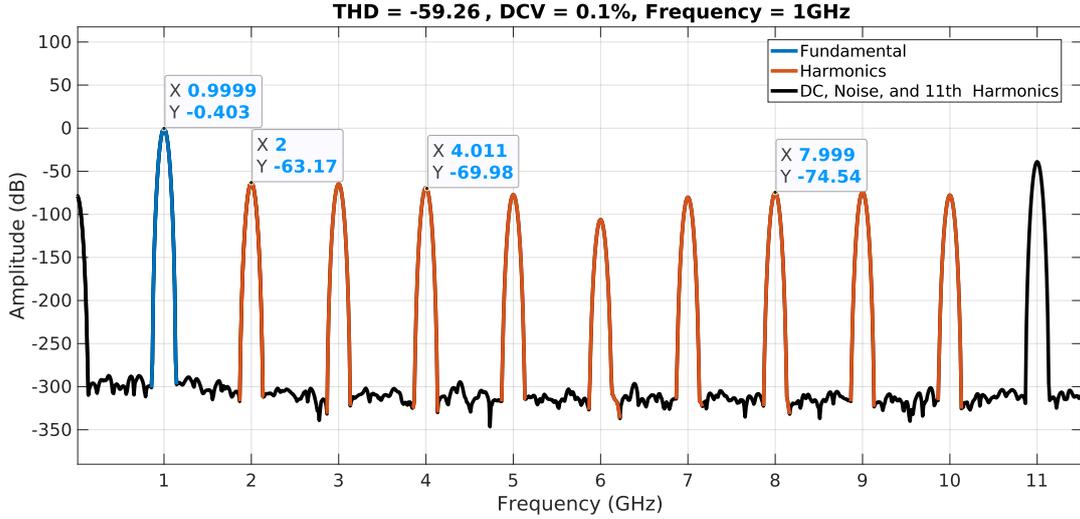


Figure 3.12: Spectrum of the sinusoidal signal when $DCV = 0.1\%$ @ Frequency = 1 GHz

signal generator will be very low, ideally, it would go to $-\infty$ which means no distortion.

3.2.1 Duty Cycle Variation (DCV)

It is defined as the percentage deviation of the duty cycle from its nominal value, which is 50% of the time period. It can be observed from equation 3.8 that if there is no mismatch in the weights and the phases, then harmonic cancellation does not have any effect on DCV . The spectral purity of the sinusoidal signal will be degraded because of the even harmonics, while all odd harmonics will be canceled. If there is an error of DCV in the duty cycle, then the total duty cycle is:

$$DC = 50\% \pm \frac{DCV \cdot 50}{100} \quad (3.9)$$

Fig. 3.12 shows the spectrum of the output signal at 1 GHz frequency when DCV is equal to 0.1% while SPE and MV are 0. The THD of the output for 0.1% is equal to -59.26 dB; however, the THD of the output signal degraded to -18.7 dB when DCV is increased to 10%. The spectrum of the output signal for 10% DCV is shown in Fig.3.13. Interestingly, both even and odd are affecting the THD of the signal which should not be the case as discussed earlier. The reason that both even and odd harmonics are degrading is that the duty cycle is not equal for all signals. This can be understood from Fig. 3.14 which shows the spectrum of the output signal for the same mismatch;

Harmonic cancellation principle and its challenges

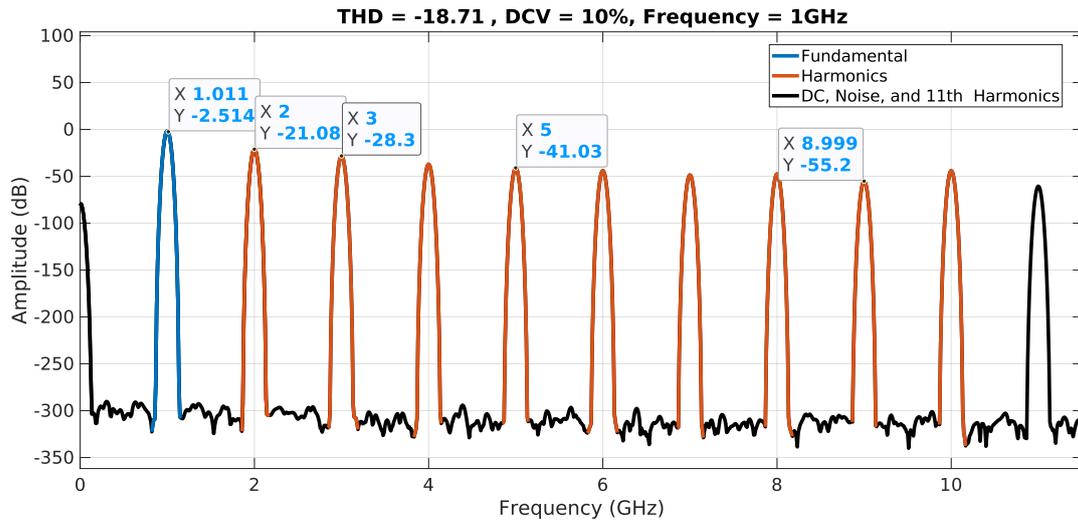


Figure 3.13: Spectrum of the sinusoidal signal when $DCV = 10\%$ @ Frequency = 1 GHz

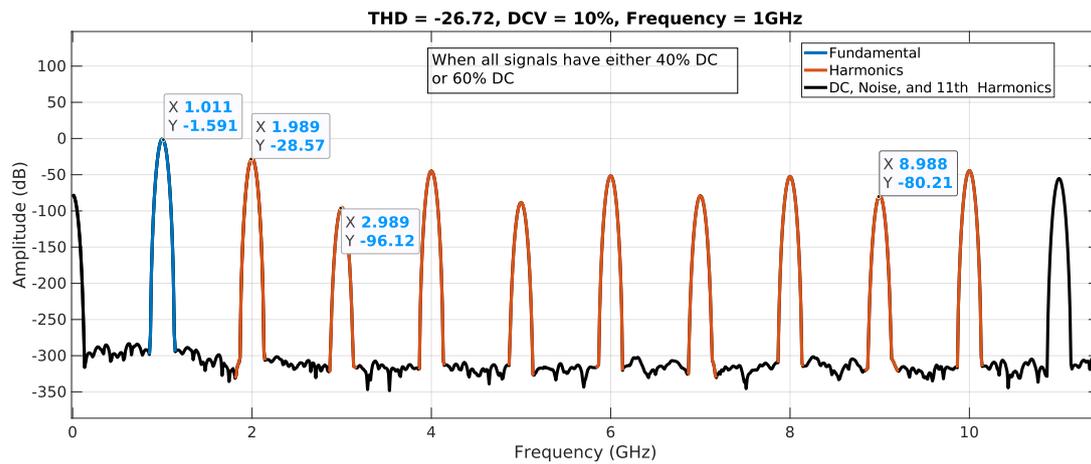


Figure 3.14: Spectrum of the sinusoidal signal when the duty cycle of all signals is either 40% or 60% @ Frequency = 1 GHz

however, the duty cycle of all signals is either 40% or 60%. In both cases, the THD of the output signal is -26.7 dB, which is dominated by even harmonics while odd harmonics are below -80 dB.

3.2 Effect of timing inaccuracies in HC

3.2.2 Static Phase Error (SPE)

It is defined as the variation in the relative phase between the square waves with respect to the time period of the signal. Ideally, the time shift between each signal should be $\frac{T}{12}$ discussed previously and also shown in Fig. 3.8. If there is an error of SPE in phase, then the total phase shift between two consecutive signals is:

$$\text{Phase Shift} = \frac{T}{12} \pm \frac{SPE \cdot T}{100} \quad (3.10)$$

Fig. 3.15 shows the spectrum of the output sinusoidal signal at 1 GHz, for SPE equal to 0.1%, which is equal to 1 ps, and the THD of the output signal is equal to -51.3 dB. The DCV and MV are 0 in this case. Because DCV is zero, all even harmonics are canceled. The THD is degraded because of the imperfect harmonic cancellation. Similarly, when SPE is 10%, the THD of the output signal degrades to -14.2 dB, as shown in Fig. 3.16. Interestingly, the 5th harmonic is also canceled here because the worst-case combination might be able to cancel the 5th harmonic but not others.

3.2.3 Mismatch Variation (MV)

It is defined as the variation in the weights responsible for harmonic cancellation in signal generators. If α_i is the scalar weight of a signal path, and MV is the mismatch in scalar weight, then the total scalar weight of a signal path is:

$$\alpha_i = \alpha_i \pm \frac{MV \cdot \alpha_i}{100} \quad (3.11)$$

Fig. 3.17 shows the spectrum of the output sinusoidal signal at 1 GHz, for MV equal to 0.1%, while keeping SPE and DCV equal to 0. The THD of the output signal is equal to -77.4 dB, which is excellent, as all even harmonics are not present. However, when MV is increased to 10%, the THD of the output signal degrades to -37.3 dB, as shown in Fig. 3.18.

The behavior model is simulated for a worst-case combination of these mismatches individually for a wide range of mismatch values. Fig. 3.19 consolidates the obtained worst-case THD for the generated output sine-wave as a function of the maximum percentage of variation for each effect, SPE , DCV , and MV . In absolute terms, it is clear that the timing errors (i.e., phase and duty cycle variations) drastically degrade the linearity of the output sinusoidal signal, while the effect of scale-weight mismatch remains more limited. However, it will be interesting to know how these variations are sensitive to the frequency of the output sinusoidal signal. To understand this, in the

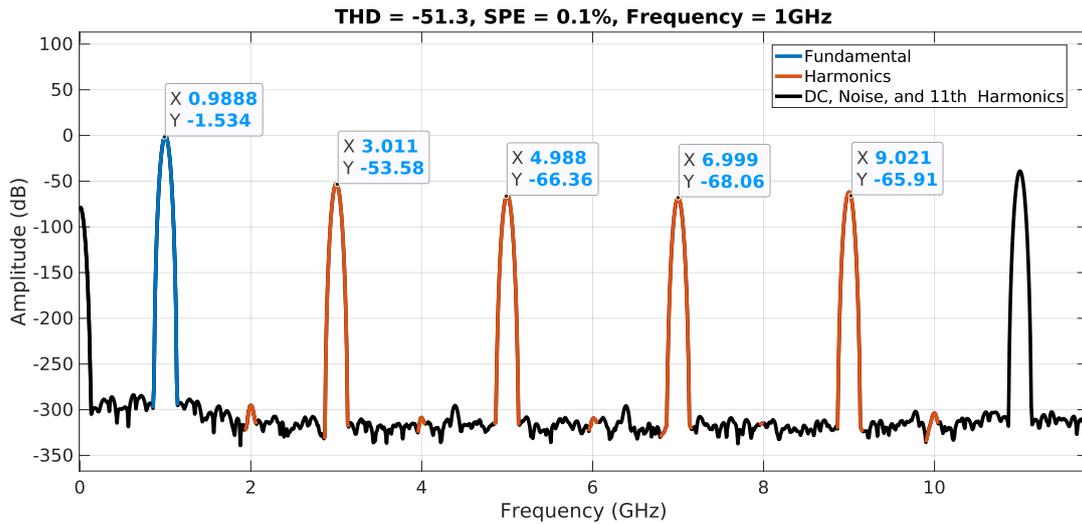


Figure 3.15: Spectrum of the sinusoidal signal when SPE is 0.1% @ Frequency = 1 GHz

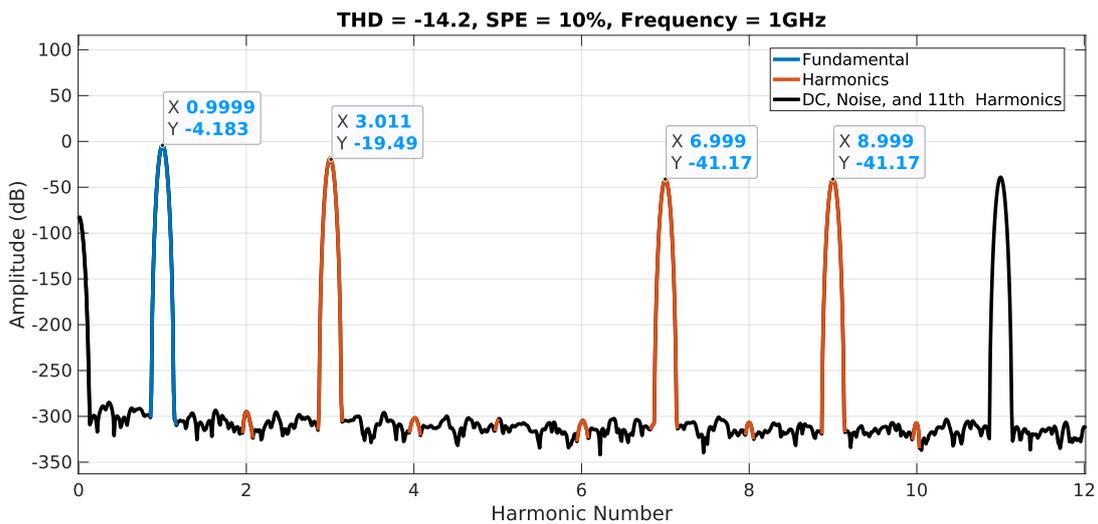


Figure 3.16: Spectrum of the sinusoidal signal when SPE is 10% @ Frequency = 1 GHz

following section, some important conclusions are made by exploring the equation of the harmonic cancellation, Equation 3.8, followed by some behavioral simulations that support these conclusions.

3.3 Sensitivity of frequency on mismatches

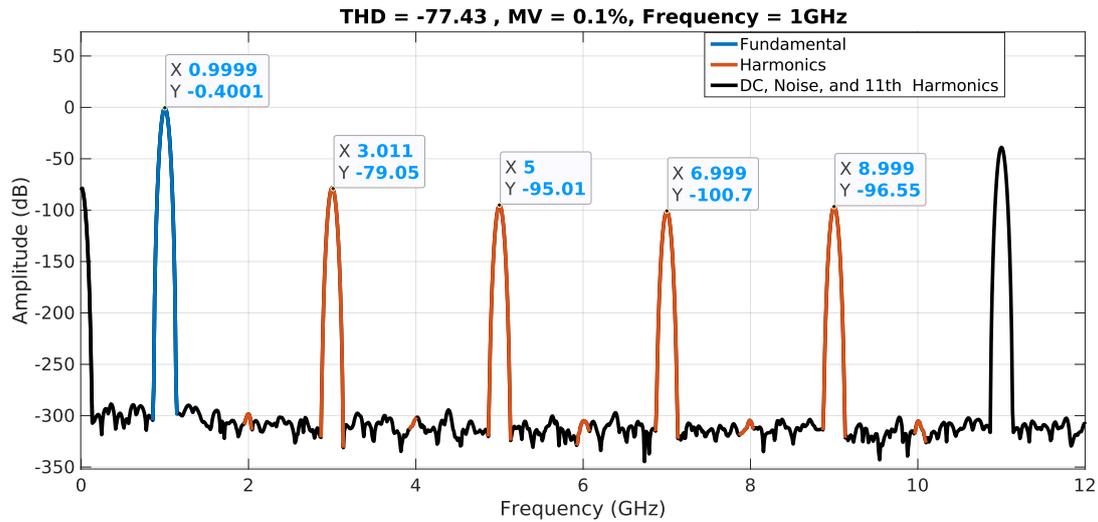


Figure 3.17: Spectrum of the sinusoidal signal when MV is 0.1% @ Frequency = 1 GHz

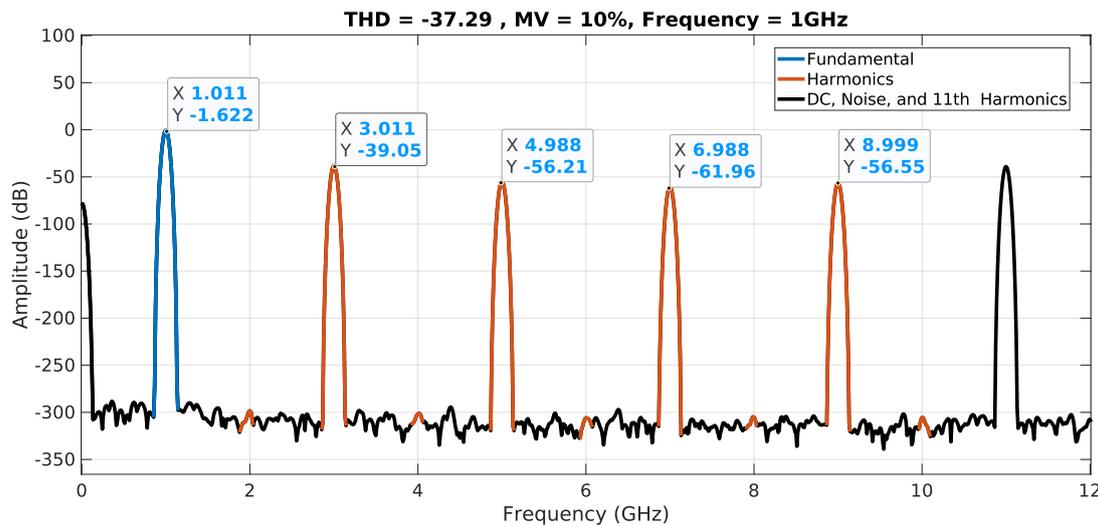


Figure 3.18: Spectrum of the sinusoidal signal when MV is 10% @ Frequency = 1 GHz

3.3 Sensitivity of frequency on mismatches

Sensitivity analysis is used to understand how a function responds to different sources of change in its inputs. In other words, it quantifies how changes in the input parameters of a function influence the output. Sensitivity analysis is essential when it is important to understand the identification of critical parameters that can influence output.

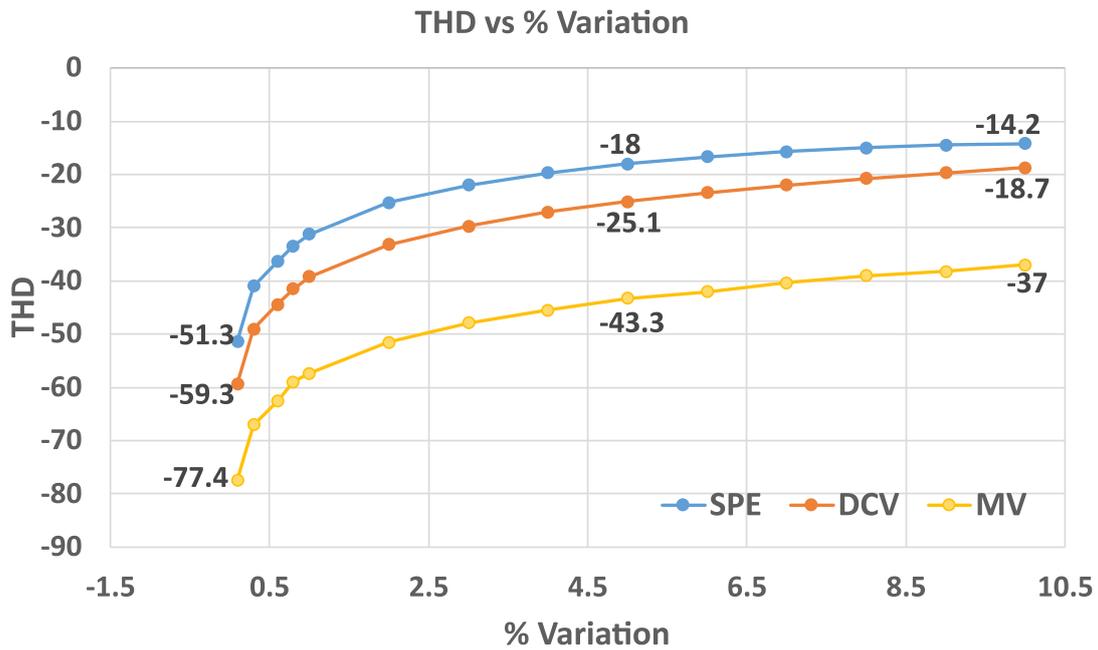


Figure 3.19: *THD* vs % Variation @ Frequency = 1 GHz

Consider a function,

$$y = f(a, b, c)$$

where y is the output that depends on input parameters a, b, c . The sensitivity of y to any of these parameters say a , can be evaluated through partial differentiation.

Let us define the following symbols:

- S_a : Sensitivity of y with respect to a
- $\frac{\partial y}{\partial a}$: Partial derivative of y with respect to a
- Δa : small change in parameter a
- Δy : Corresponding change in output y

The sensitivity S_a can be calculated as,

$$S_a = \frac{\Delta y/y}{\Delta a/a} = \frac{a}{y} \frac{\partial y}{\partial a}$$

3.3 Sensitivity of frequency on mismatches

which gives the percentage change in y for a given percentage change in a , assuming other variables are constant.

This sensitivity coefficient S_a can then be used to understand the impact of the parameter a on the output y . A higher value of S_a indicates that y is highly sensitive to changes in a , and thus, any change in a would significantly influence the change in y .

As discussed earlier, for a signal $x(t)$ which is even and periodic, $y(t)$ is expressed as:

$$y(t) = \sum_{n=1}^{\infty} \frac{2}{n\pi} \sin\left(\frac{n\pi T_x}{T}\right) \left[1 + \sum_{i=1}^p 2\alpha_i \cos\left(\frac{2n\pi\Delta t_i}{T}\right)\right] \cos(n\omega_0 t) \quad (3.12)$$

Since $y(t)$ is a function of T_x , Δt_i , and α_i , differentiating $y(t)$ with respect to T_x :

$$\frac{\partial y}{\partial T_x} = \sum_{n=1}^{\infty} \frac{2}{T} \cos\left(\frac{n\pi T_x}{T}\right) \left[1 + \sum_{i=1}^p 2\alpha_i \cos\left(\frac{2n\pi\Delta t_i}{T}\right)\right] \cos(n\omega_0 t) \quad (3.13)$$

Sensitivity with respect to T_x is,

$$S_{T_x} = \frac{T_x}{y(t)} \frac{\partial y(t)}{\partial T_x} \quad (3.14)$$

$$S_{T_x} = \frac{T_x \sum_{n=1}^{\infty} \cos\left(\frac{n\pi T_x}{T}\right) \left[1 + \sum_{i=1}^p 2\alpha_i \cos\left(\frac{2n\pi\Delta t_i}{T}\right)\right] \cos(n\omega_0 t)}{T \sum_{n=1}^{\infty} \frac{1}{n\pi} \sin\left(\frac{n\pi T_x}{T}\right) \left[1 + \sum_{i=1}^p 2\alpha_i \cos\left(\frac{2n\pi\Delta t_i}{T}\right)\right] \cos(n\omega_0 t)} \quad (3.15)$$

Equation 3.15 reveals an inverse relationship between the sensitivity of S_{T_x} and the time period of the signal; it can also be understood as it is directly proportional to the frequency of the output signal. When $T \rightarrow 0$, frequency $\rightarrow \infty$, the sine and cosine terms will be bounded between -1 to 1 , making the whole S_{T_x} term to ∞ . In other words, an increase in the frequency of the output signal while keeping the absolute value of the mismatch constant (in this case duty cycle T_x), increases S_{T_x} that leads to a degradation in harmonic cancellation. To affirm this conclusion, we will also present detailed behavioral-level simulations in the following section.

Differentiating $y(t)$ again with respect to Δt_i :

$$\frac{\partial y(t)}{\partial \Delta t_i} = \sum_{n=1}^{\infty} -\frac{8}{T} \sin\left(\frac{n\pi T_x}{T}\right) \sum_{i=1}^p \left(\alpha_i \sin\left(\frac{2n\pi\Delta t_i}{T}\right)\right) \cos(n\omega_0 t) \quad (3.16)$$

Sensitivity with Δt_i is defined by:

$$S_{\Delta t_i} = -\frac{4\Delta t_i \sum_{n=1}^{\infty} \sin\left(\frac{n\pi T_x}{T}\right) \sum_{i=1}^p \left(\alpha_i \sin\left(\frac{2n\pi\Delta t_i}{T}\right)\right) \cos(n\omega_o t)}{T \sum_{n=1}^{\infty} \frac{1}{n\pi} \sin\left(\frac{n\pi T_x}{T}\right) \left[1 + \sum_{i=1}^p 2\alpha_i \cos\left(\frac{2n\pi\Delta t_i}{T}\right)\right] \cos(n\omega_o t)} \quad (3.17)$$

Equation 3.17 also shows a direct relationship between the sensitivity of the phase with the frequency of the signal. This means that when the frequency of the signal is increased while keeping the absolute value of the mismatch to a constant value, increases $S_{\Delta t_i}$ which leads to a degradation in harmonic cancellation.

Similarly, differentiating $y(t)$ with respect to α_i :

$$\frac{\partial y(t)}{\partial \alpha_i} = \sum_{n=1}^{\infty} \frac{2}{n\pi} \sin\left(\frac{n\pi T_x}{T}\right) \left(\sum_{i=1}^p 2 \cos\left(\frac{2n\pi\Delta t_i}{T}\right)\right) \cos(n\omega_o t) \quad (3.18)$$

Sensitivity with α_i is defined by:

$$S_{\alpha_i} = \frac{\alpha_i \sum_{n=1}^{\infty} \frac{2}{n\pi} \sin\left(\frac{n\pi T_x}{T}\right) \left[\sum_{i=1}^p 2 \cos\left(\frac{2n\pi\Delta t_i}{T}\right)\right] \cos(n\omega_o t)}{\sum_{n=1}^{\infty} \frac{2}{n\pi} \sin\left(\frac{n\pi T_x}{T}\right) \left[1 + \sum_{i=1}^p 2\alpha_i \cos\left(\frac{2n\pi\Delta t_i}{T}\right)\right] \cos(n\omega_o t)} \quad (3.19)$$

Interestingly, equation 3.19 shows no relation between the sensitivity of scalar weight and the frequency of the output signal. This means that when there is a mismatch in the scalar weights, the *THD* should not be affected when the output frequency changes.

To affirm these conclusions, behavioral simulations are carried out to understand these equations in more detail. The absolute values of mismatch (*SPE*, *DCV*, and *MV*) are kept constant while the frequency of the output sinusoidal signal is varied. Fig. 3.20 shows the *THD* versus the frequency of the output signal while the mismatch parameters are kept to a constant value. The plot in blue color shows the trend of the degradation of the *THD* when *SPE* is fixed to 1 ps, which is the 1% *SPE* at 1 GHz, while *DCV* and *MV* are 0. The *THD* of the signal is -51.33 dB at 1 GHz when *SPE* is 1 ps, while it degraded to -41.7 dB when the frequency is increased to 3 GHz.

Similarly, the plot in orange color shows the degradation of *THD* when *DCV* is a fixed value, which is 0.1% at 1 GHz (0.5 ps, T_{on} is either 499.5 ps or 500.5 ps at 1 GHz), while *SPE* and *MV* are 0. The *THD* is -59.26 dB. When the frequency is increased to 3 GHz, the *THD* of the signal decreases to a value of -49.72 dB.

However, in the case of a 1% *MV* keeping *SPE* and *DCV* 0, the *THD* of the output signal remained constant at a value equal to -59.26 dB. This shows that *SPE* and *DCV* depend on the frequency of the output signal, and *MV* does not depend on the

3.4 Summary

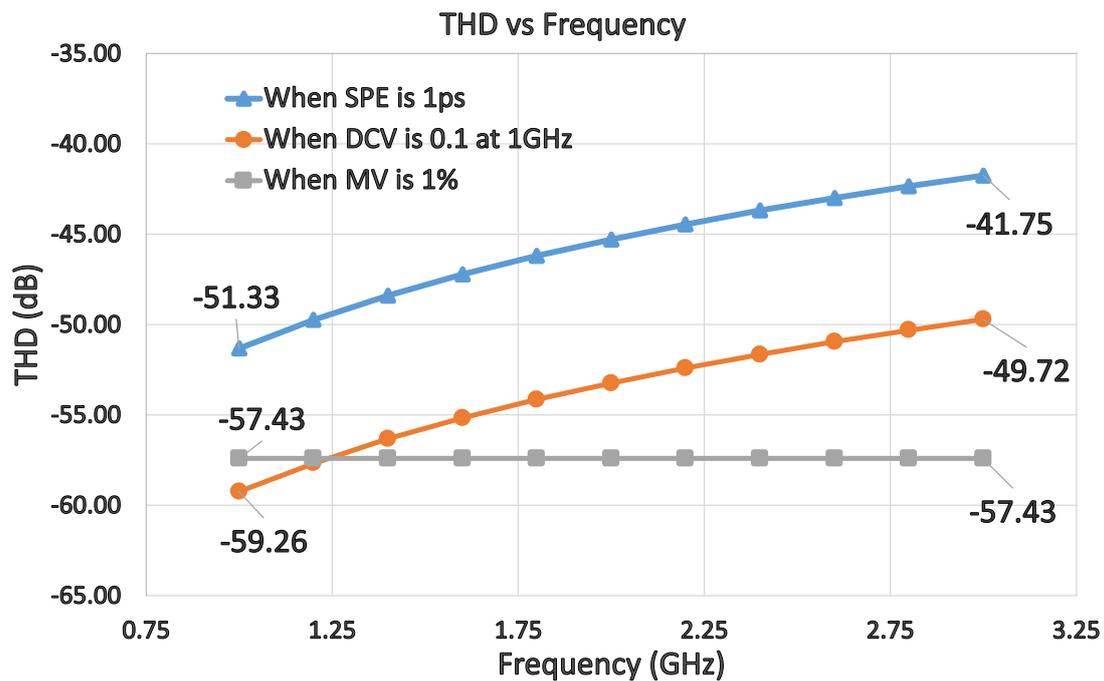


Figure 3.20: *THD* of the output signal when *SPE*, *DCV*, and *MV* are constant while the frequency of output signal is varied

frequency. Therefore, *SPE* and *DCV* are known as timing inaccuracies, which are extremely important when generating a sinusoidal signal for higher frequencies.

3.4 Summary

In this chapter, we started the discussion with the concept of harmonic cancellation. A pure sinusoidal signal can be generated by adding a scaled version of the time-shifted periodic signals which is a square wave signal in this case. Depending on the number of time-shifted signals, a particular number of harmonics of the periodic signal can be canceled. A good trade-off is to use a 5-phase system that cancels all odd harmonics below the 11th harmonic and by ensuring a 50% duty cycle the even harmonics will not be present at the output signal. We also discussed the types of mismatches that can degrade the performance of the sinusoidal signal generator based on harmonic cancellation which are *SPE*, *DCV*, and *MV*. A quantitative analysis using mathematical derivation and a qualitative analysis using behavioral simulations were also done for these mismatches to understand their implications on the signal generator. These analysis helped us understand the significance of timing inaccuracies (*SPE* and *DCV*) when

the frequency of a generated signal is increased especially in GHz. We concluded, when the frequency of the output signal is increased, the quality of the output signal (*THD* or the linearity of the output signal) degrades when the absolute values of *SPE* and *DCV* at a particular frequency are constant.

Practical implementations including mitigation strategies

The previous chapter gave us an understanding of the harmonic cancellation principle and its limitations when generating a sinusoidal signal at higher frequencies. It is shown that when the frequency of generation increases, for an absolute value of timing inaccuracies such as *SPE* and *DCV* at a particular frequency, the quality of the output sinusoidal signal degrades. Given the quantitative and qualitative analysis done in the previous chapter, it is clear that a practical implementation of a harmonic canceling generator targeting high-frequency signal generation has to carefully consider any timing issues that would otherwise limit the linearity of the generated signal. This explains the limited performance of previously reported generators at higher frequencies such as in [44, 45] that rely only on a calibration of the scaling weights, while the performance is limited by timing inaccuracies. Better results are obtained in [32] due to the introduction of timing calibration. The authors have introduced a calibration circuit based on a capacitor bank that corrects the timing inaccuracies present in time-shifted signals. The minimum and maximum values of the capacitor bank will also limit the maximum and minimum frequency of the generated signal.

In this chapter, we explore various methods for the effective implementation of a sinusoidal signal generator based on the HC principle at higher frequencies. A significant concern associated with this is the timing inaccuracies (*SPE* and *DCV*). We have meticulously developed and proposed three distinct strategies aimed at mitigating these

timing errors, ensuring a precise and reliable performance of the signal generator. Each solution is analyzed in detail, demonstrating their respective effectiveness.

As discussed in the previous chapter, the number of harmonics that need to be canceled depends on the number of time-shifted signals and weights. These solutions that will be discussed in the next section use a 5-phase type harmonic cancellation generator that can cancel harmonics below the 11th harmonic. These signals are time-shifted by $\frac{T}{12}$ which also means that these signals are phase-shifted by $\frac{\pi}{6}$ as illustrated in Fig.3.8. The first two solutions are based on external optimization, on the other hand, the third solution uses negative feedback in such a way that timing inaccuracies can be corrected using some reference voltages. The optimization algorithm to optimize the first two solutions is discussed in the next chapter.

4.1 Signal generator with a continuous duty cycle correction and a discrete phase correction circuit

The block diagram of the first solution for the practical implementation of a harmonic canceling sinusoidal signal generator at high frequencies is shown in Fig.4.1. A 6-stage differential ring oscillator is employed for generating the required 5 phases ($\phi_0 = 0$, $\phi_1 = \pm\frac{\pi}{6}$, and $\phi_2 = \pm\frac{\pi}{3}$ also shown in Fig.3.8). These signals are first passed through a buffer stage and subsequently a dedicated duty-cycle and phase error mitigation circuits are employed to calibrate timing inaccuracies in these generated square-wave signals. Finally, the calibrated phases are scaled, combined, and filtered by a low-pass output filter to generate an analog sinusoidal signal at the output. The pole of the output filter (LPF) is placed below the fundamental frequency. The 6-stage differential oscillator and the mitigation circuitry are implemented at the transistor level in ST 28 nm FD-SOI technology. The implementation of the rest of the generation circuitry which is a weighted sum of the generated phases, and filtering is modeled at behavioral level using VerilogA. The ring oscillator has been designed and biased for an oscillation frequency of around 1.4 GHz. As mentioned before, targeting such a high operating frequency requires the use of mitigation strategies for timing inaccuracies. To overcome these issues, a circuit-level mitigation solution for compensating static phase errors and duty cycle variations is used.

4.1 Signal generator with a continuous duty cycle correction and a discrete phase correction circuit

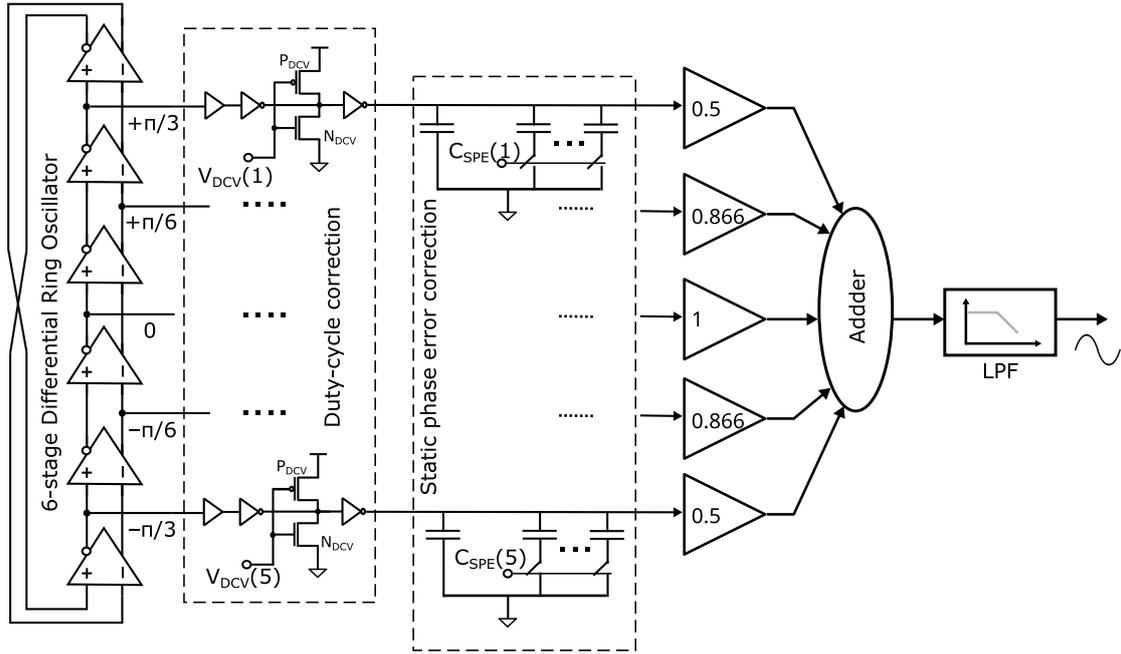


Figure 4.1: Block diagram of sinusoidal Signal generator with a continuous duty cycle correction and a discrete phase correction circuit

4.1.1 Mitigation of duty-cycle variation

The proposed duty-cycle correction circuit is based on a pulse-width modification circuit adapted from the work in [78]. The circuit representation of the pulse-width modification circuit is shown in Fig.4.2.(a), which can modify the duty cycle of an input signal with the help of control voltage (Correct_DC). Firstly, each of the phases generated by the ring oscillator is buffered and fed to the duty cycle correction circuit. The buffers are required since the correction in the duty cycle and the phase should not affect the internal nodes of the oscillator. When Correct_DC changes, it also changes the gate to source capacitance of the transistor and can change the frequency and the phase of signals generated from the oscillator. Otherwise, the phase and frequency of the oscillator can be affected. It consists of three stages of inverters; the drive strength of the first inverter is adjusted with the help of the second stage which has variable current sources connected at the output node of the first inverter. The current of the sources of the second stage is controlled with the help of the control voltage Correct_DC, which either changes the rise or fall times of the signal at the output node of the first inverter. The third stage is a comparator stage whose trip point is close to half of the supply voltage that rectifies the slew-deformed signal. When the control voltage Correct_DC decreases

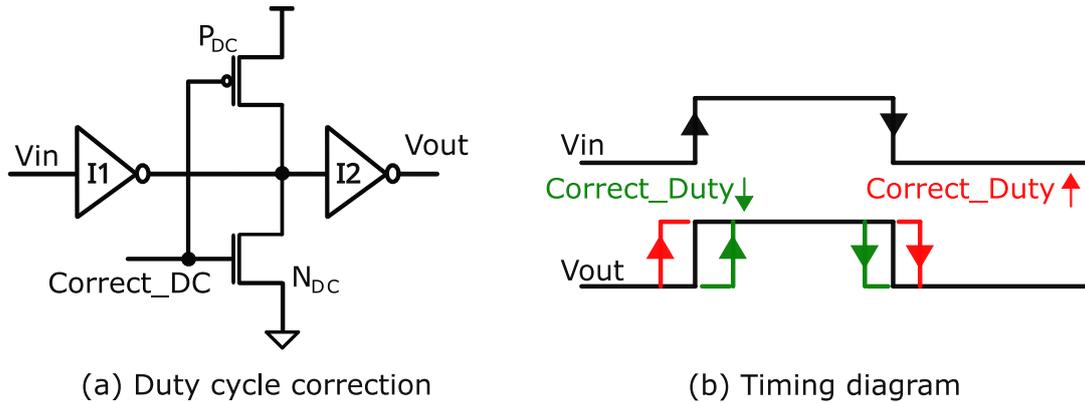


Figure 4.2: Duty cycle correction circuit

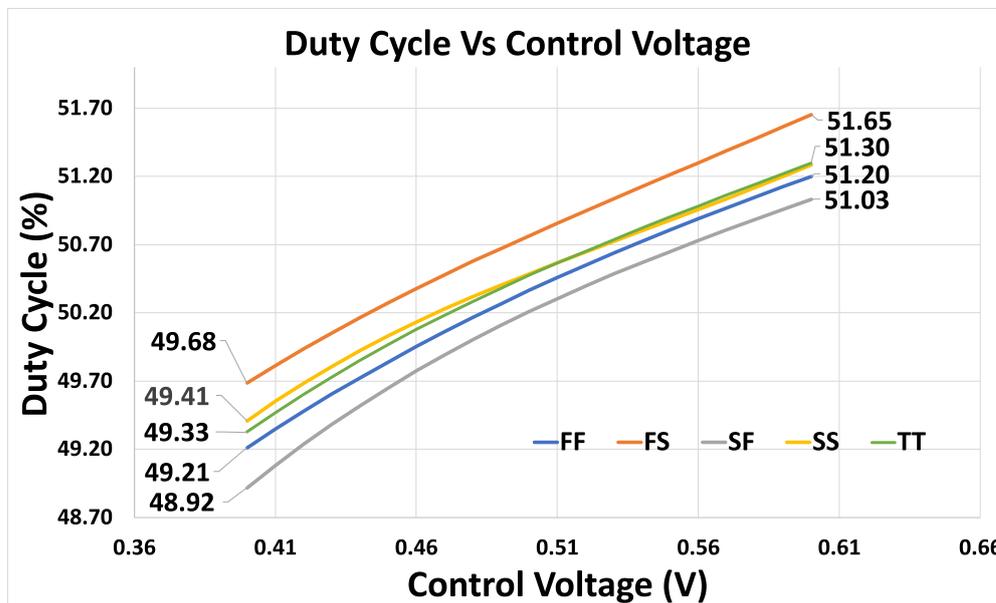


Figure 4.3: Simulation results of duty cycle correction circuit

the duty cycle of the output signal decreases while the duty cycle increases when the Correct_DC voltage increases as shown in Fig.4.2.(b). The duty cycle correction circuit is explained in more detail in section 4.3. The simulation results of the duty cycle correction circuit are shown in Fig.4.3 for Correct_DC voltage ranging from 0.38 V to 0.6 V. The circuit has been sized to achieve a tuning range of around $\pm 5\%$ duty cycle variation across the technology corners. Of course, this range can be increased either by changing the size of P_{DC} and N_{DC} or by cascading the multiple-duty correction circuit.

4.1 Signal generator with a continuous duty cycle correction and a discrete phase correction circuit

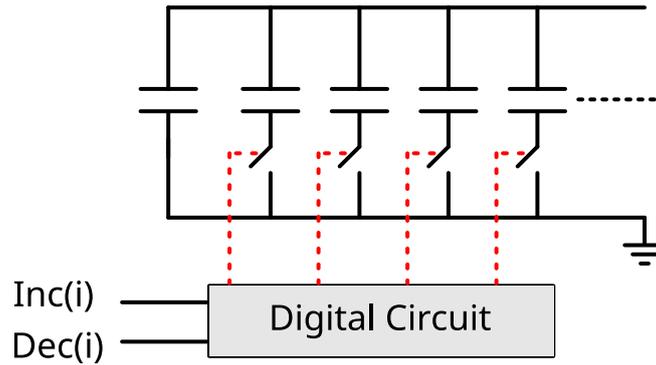


Figure 4.4: Static phase error calibration circuit

4.1.2 Mitigation of static phase error

The mitigation of the static phase error is achieved by loading the output of the duty-cycle correction circuit by a variable capacitor array as depicted in Fig.4.4. Let us consider two signals A and B for reference shown in Fig.3.8. Assuming that only the load capacitor of signal A is varied. When the load capacitor increases the delay of signal A increases and the phase of the signal, with respect to signal B decreases. Similarly when the load capacitor decreases the delay of the signal A decreases which increases the phase difference with respect to signal B. A digital circuit that generates the $C_{SPE}()$ control word either increases or decreases the load capacitor based on the signals Inc(i) or Dec(i) signal where i is the phase number (1 to 5). The capacitor array has been sized to correct phase errors up to $\pm 5\%$. It is important to notice that the output buffers in the duty-cycle calibration circuit decouple the two calibration knobs so there is no degradation of the duty cycle due to phase error corrections.

4.1.3 Simulation Results

To check the feasibility of the mitigation circuit discussed, 200 Monte Carlo simulations of this signal generator were performed using the models in the PDK of the selected ST 28 nm FDSOI technology. For this solution, only the mismatch contributions from the differential oscillator and the duty cycle correction circuit are considered. The standard deviation of the frequency from the oscillator is around 5.2 MHz and the mean is around 1.44 GHz, as shown in Fig.4.5. The X-axis shows the output frequency of VCO and the Y-axis shows the number of samples corresponding to the output frequency.

The obtained linearity is expressed in terms of the *THD* of the generated sinusoidal signal. The *THD* has been computed up to the 10th harmonic component since

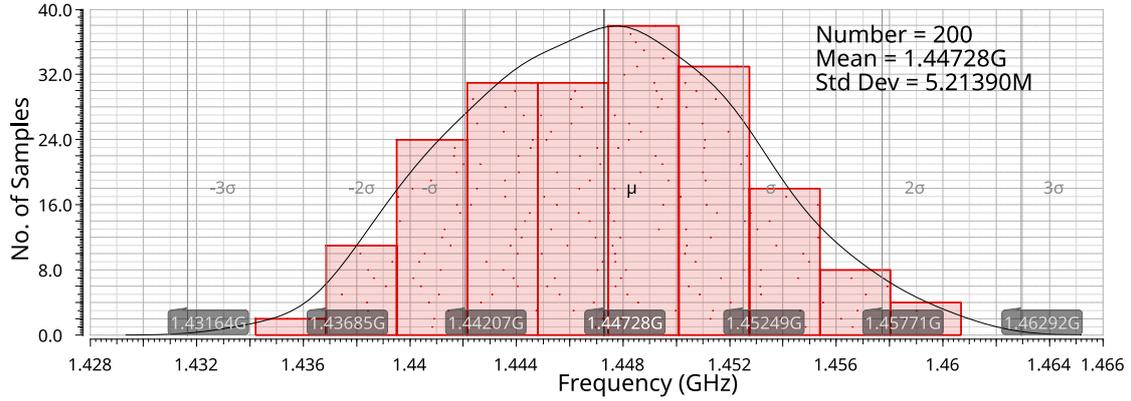


Figure 4.5: Monte Carlo results of oscillator's output frequency

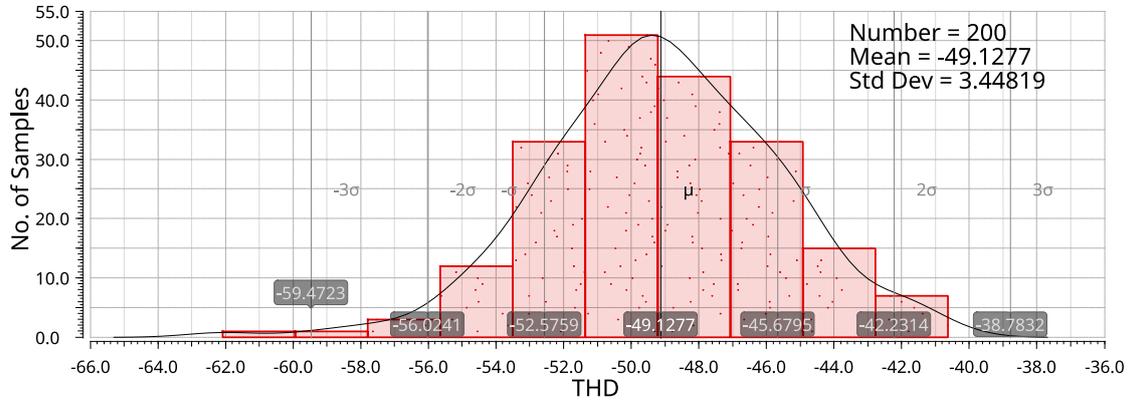


Figure 4.6: Monte Carlo results of *THD* of output sinusoidal signal

the proposed harmonic cancellation technique is targeted at the cancellation of the odd harmonics up to the 9th component. Fig.4.6 shows the Monte Carlo results of variations in the *THD* of the generated output sinusoidal signal. The nominal *THD* value of the sinusoidal signal at 1.45 GHz is -61 dB. The *THD* for the best case is around -62 dB while it is -40.6 dB for the worst case. The output spectrum of the uncalibrated worst-case generated signal is shown in Fig.4.7.(a) up to the 11th harmonic component. Initially, the duty cycle calibration was done, and that improved the *THD* to -51 dB which improved the *THD* by 11 dB. The spectrum of the sinusoidal signal after duty cycle correction is shown in Fig.4.7.(b). It is clear to see the improvement of the second and fourth harmonic components which are reduced by -20 dB and -10 dB, respectively. After correcting both duty cycle and phase of the signals, the *THD* of the output signal improved to -57 dB, which represents an improvement of 17 dB with respect to the uncalibrated generator as shown in Fig.4.7.(c). It is interesting to notice that even

4.1 Signal generator with a continuous duty cycle correction and a discrete phase correction circuit

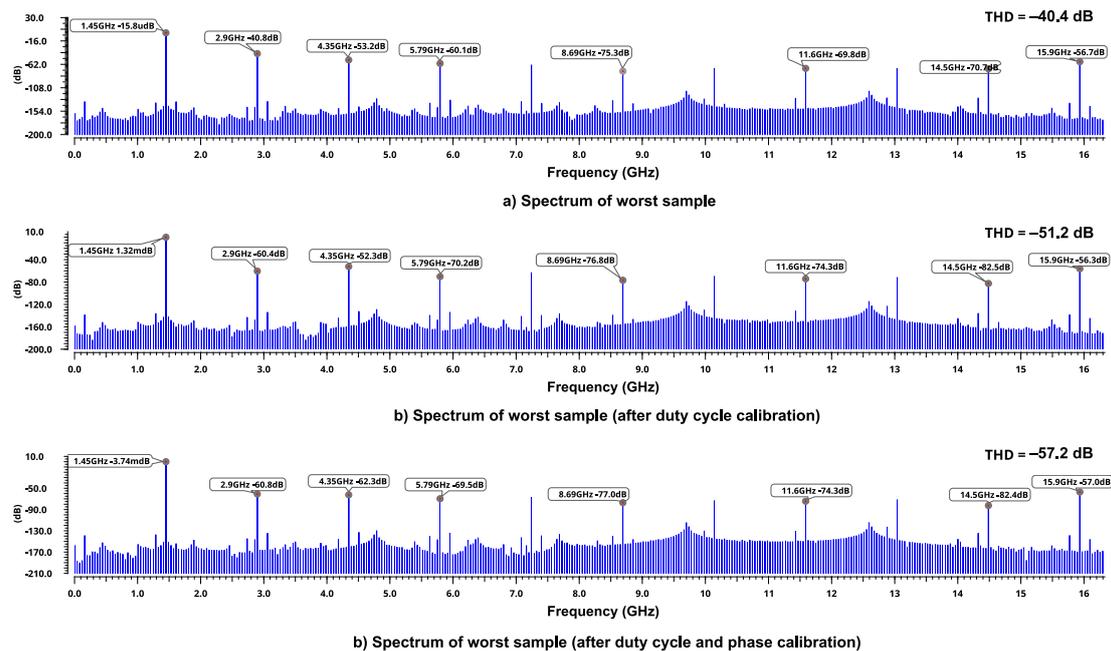


Figure 4.7: Frequency spectrum of the output signal for the worst sample of Monte Carlo simulation: a) Before optimization; b) After duty cycle correction; c) After duty cycle and phase correction

order harmonics are not that much affected by the phase correction and only odd order harmonics are improved.

4.1.4 Discussion and limitations

Most of the systems we deal with are differential systems, and the generator that has been discussed is not. This design can be converted to a differential design by replicating the mitigation circuit along with the scaling and the low pass filter circuits and the inverted signal will be driving the differential part. Now the number of signals that require calibration is going to double which is equal to 10. So, the number of calibration knobs will also double to 20 and the complexity of optimizing the signal generator will also increase. Not only the complexity of optimization but also the range of values of the capacitor bank for correcting the phase error will also decide the range of frequencies that can be optimized which is a similar bottleneck as in the case of [32].

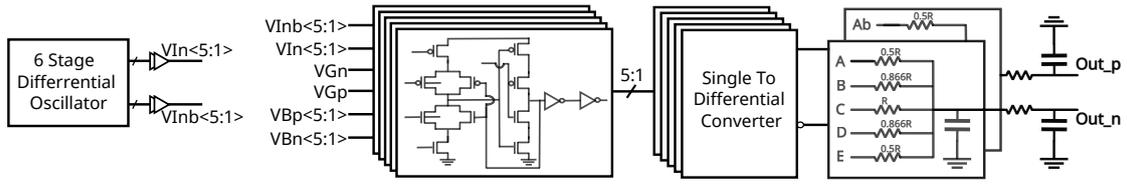


Figure 4.8: Block diagram of HC-based sinusoidal signal generator with calibration using coarse-fine delay cell

4.2 HC-based signal generator with calibration using coarse-fine delay cell

The first solution that is presented in the previous section shows some limitations in the case of differential sinusoidal signal generation. The first limitation is the large number of tuning knobs to correct the timing inaccuracies of square wave signals and the second limitation is the range of frequencies to which the phase correction can be done is limited by the minimum and the maximum value of the capacitor bank. To overcome these limitations, we propose a second practical implementation based on a coarse-fine delay cell-based timing correction circuit that can correct these timing inaccuracies for a wide range of mismatches and frequency ranges.

The complete sinusoidal signal generator based on a coarse-fine delay cell is shown in Fig.4.8. The 5 differential square wave signals (A to E) that are time-shifted by $\frac{T}{12}$ are generated by a 6-stage fully differential oscillator. Then these signals are first buffered with the help of an even number of inverters and then passed through 5 delay cells for the correction of timing inaccuracies. The delay cell produces the single-ended output, so, these signals are connected to a single-to-differential converter that generates the differential signals. These differential signals are then scaled with the help of a passive adder, then added to a capacitor, and with the help of a low pass filter the non-cancellable higher harmonics are attenuated.

4.2.1 6-Stage differential oscillator

There are two ways by which one can generate the time-shifted signal. One can use an external clock signal and then divide the clock frequency with the help of the circular shift register that requires 12 flip-flops also discussed in chapter 3. Any five consecutive outputs of the circular shift register are time-shifted by $\frac{T}{12}$ however the output frequency gets divided by 12. This means that in order to get an output frequency equal to 2 GHz, the input signal should be 24 GHz which is not practical from the design point of view.

4.2 HC-based signal generator with calibration using coarse-fine delay cell

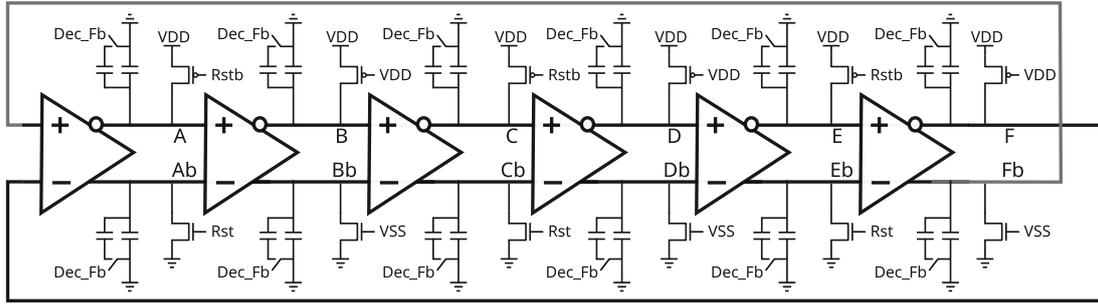


Figure 4.9: 6-stage differential oscillator

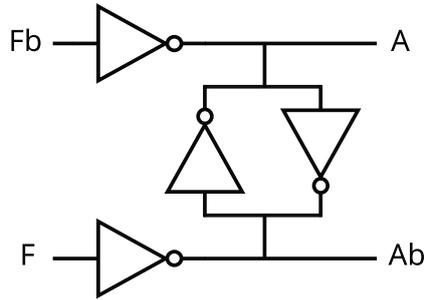


Figure 4.10: Single stage of a 6-stage differential oscillator

The other way to generate these phases is with the help of an on-chip ring oscillator. A classical ring oscillator has an odd number of inverter stages that can generate a time-shift between the signals equal to $\frac{T}{N}$, where T is the time period of the signal and N (odd) is the number of stages. However, the required time-shift between each signal is $\frac{T}{12}$, so a 6-stage fully differential oscillator is used which is shown in Fig.4.9. The oscillator consists of two rings with an even number of stages and these rings are coupled with latches in each stage. It can also be said that each stage of the differential oscillator has two inverters, the output of each inverter is coupled with the help of a latch also shown in Fig.4.10. The latch inverters are moderately weaker than the inverters of each stage such that the differential oscillator sustains the oscillations [79]. The timing diagram of all phases of a 6-stage differential oscillator is shown in Fig.4.11. The frequency of the oscillator is changed by changing the supply voltage of each stage. To achieve a wide range of frequencies, the load capacitor of the oscillator is kept programmable with the help of the digital signal, Dec_Fb. When Dec_Fb is high, the load capacitor of each stage increases which enables the low-frequency mode, on the other hand when it is low, a high-frequency mode is activated. The oscillator is designed to operate from frequency 170 MHz to 2.70 GHz in the schematic level.

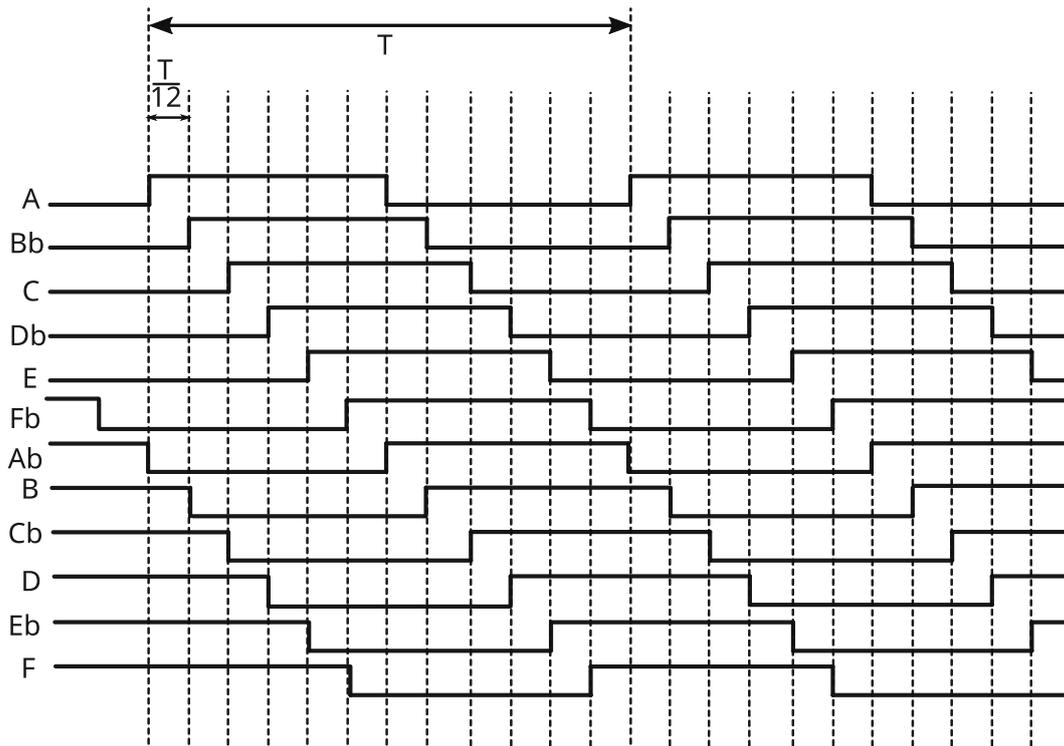


Figure 4.11: Timing diagram of all phases of a 6-stage differential oscillator

4.2.2 Mitigation of timing inaccuracies using a coarse-fine delay cell

The schematic view of the delay cell is shown in Fig.4.12 [80]. This delay cell presents a coarse-fine variable delay in which the coarse delay can be fixed with the help of a control gate voltage while the fine delay is controlled with the help of a body bias voltage. The transistors that are used in the design are LVT transistors of the FD-SOI technology which are fabricated in a flip well scheme. The NMOS is built on an n-well while the PMOS is built on a p-well. Because of this, when the body bias voltage on the NMOS transistor increases the threshold voltage of the transistor decreases. Similarly in the case of PMOS, when the body bias voltage decreases its threshold voltage decreases. An ultra-thin oxide layer is present under the source and drain in FD-SOI technology that gives more freedom for a wide range of body bias voltage, 0 to 2 V in the case of NMOS, and 0 to -2 V in the case of PMOS.

The first stage of the delay cell is a current-starved inverter and the second stage is a gated inverter. The output of the second stage (V_f) acts as a feedback signal to the

4.2 HC-based signal generator with calibration using coarse-fine delay cell

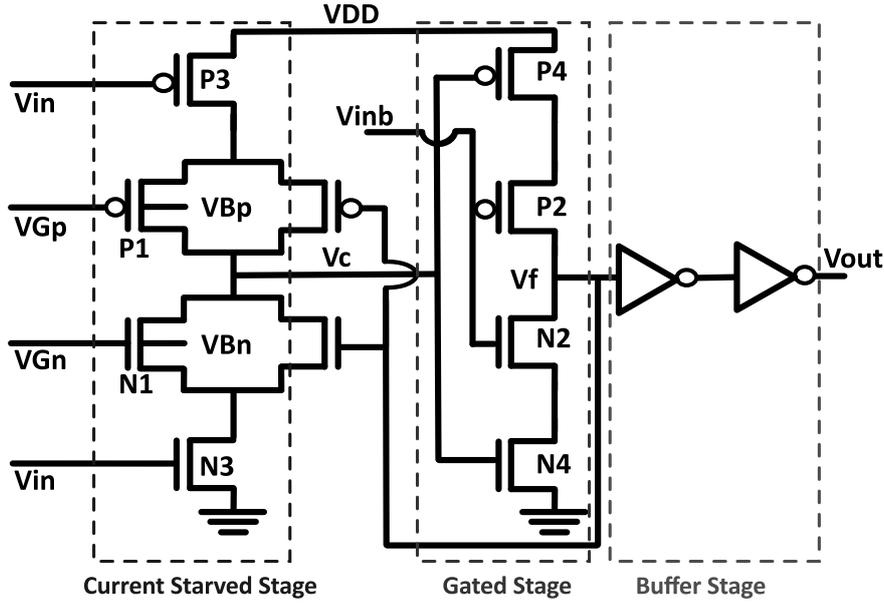


Figure 4.12: Coarse-fine delay cell based on body bias: Coarse tuning is done by gate voltages (V_{Gn} and V_{Gp}) and fine-tuning is done by body voltages (V_{Bn} and V_{Bp})

input of an inverter in parallel with the current starved inverter. Finally, inverters are cascaded after the second stage to drive the next stage.

The operation of the delay cell can be explained as follows. As the input of the delay cell rises from 0 to 1 also illustrated in Fig.4.13, the voltage of node V_c discharges slowly due to the current-starving nature of the inverter till it reaches the threshold of the gated inverter in the next stage. Once the input of the second stage crosses the threshold, the output of the second stage which is the feedback signal to the first stage cancels the current starving nature of the inverter by activating the inverter in parallel with it. The V_c node then discharges at a faster rate. The operation for the input voltage falling from 1 to 0 can be understood in a similar manner.

In the nominal state, the delay cell is biased by setting the gate input voltage of transistors $N1$ and $P1$ in the current starved stage in such a way that the rise and fall times are the same. Then, the delay can be fine-tuned to the required value by changing the body bias of the NMOS ($N1$). When the body bias voltage V_{Bn} is increased, the threshold voltage of the $N1$ transistor decreases which reduces the fall time of the signal V_c (which corresponds to the rising edge of the input signal), thus the input signal advances as shown in Fig.4.13. To illustrate the operation of the delay cell in the harmonic canceling generator, let us say the initial phase difference between signals A and B is less than the intended $\frac{T}{12}$. When the body bias of NMOS of the delay cell for signal

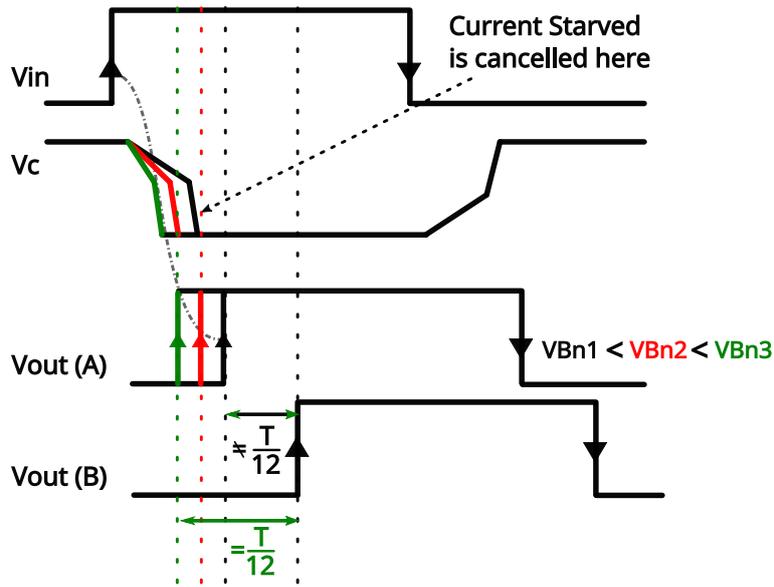


Figure 4.13: Operation of Delay cell when V_{Bn} is varied for phase correction

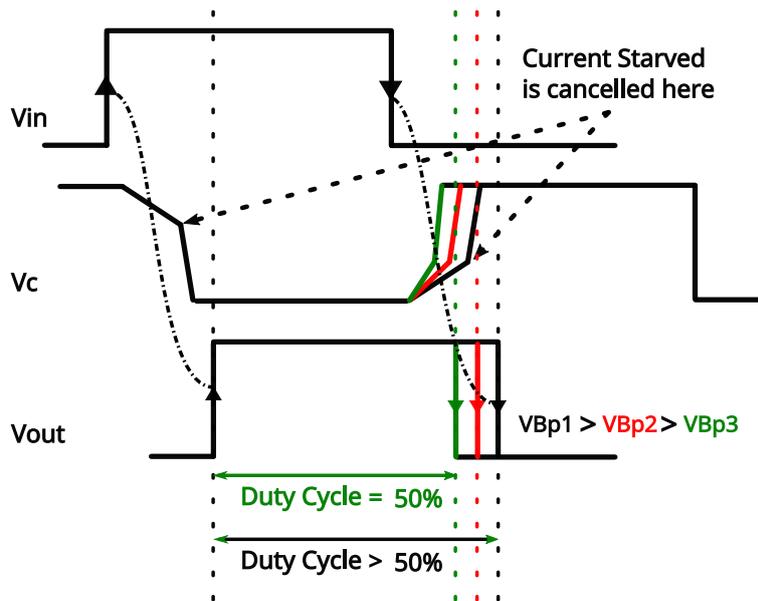


Figure 4.14: Operation of Delay cell when V_{Bp} is varied for duty cycle correction

As V_{Bn} is increased to V_{Bn3} the delay of the delay cell decreases and the phase difference between signal A and B can be tuned to the target value of $\frac{T}{12}$.

Similarly, when V_{Bp} is decreased, the falling edge of the input signal is advanced

4.2 HC-based signal generator with calibration using coarse-fine delay cell

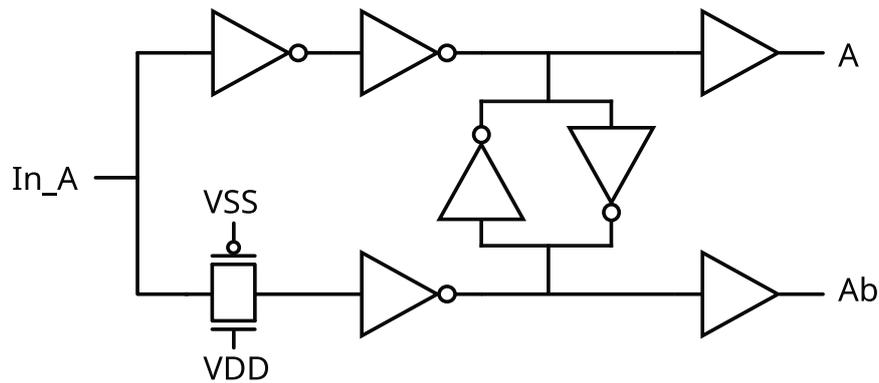


Figure 4.15: Single-to-differential converter

which changes the duty cycle of the input signal as shown in Fig.4.14. From these observations, it can be concluded that the timing errors can be corrected using this delay cell.

4.2.3 Single-to-differential signal converter

The calibrated signals can be added with the adder at the output but because these signals are not differential, the surrounding noise can affect these signals which can degrade the linearity of the output signal. To overcome this, the single-ended signals are passed through a single-to-differential converter circuit. It consists of two chains of inverters. One of the chains has an 'n' number of inverters whereas the other chain has an 'n-1' number of inverters. To reduce the skew between two signals, the two chains are connected using cross-coupled inverters along with a pass transistor at the input of the chain which has an n-1 number of inverters where n is an odd number, also shown in Fig.4.15.

4.2.4 Adder

The last step of the harmonic cancellation is to scale these time-shifted signals with their respective weights as discussed in chapter 3 followed by a LPF. One of the ways by which these signals can be added is by using a current steering DAC, but the current steering DAC suffers from dynamic errors, the distortion is higher for higher frequencies [74], and designing a DAC for such a high-frequency signal requires more area and power. To avoid these challenges, a weighted resistor-based summing network is used which is shown in Fig.4.16. The last inverter of the single-to-differential converter stage

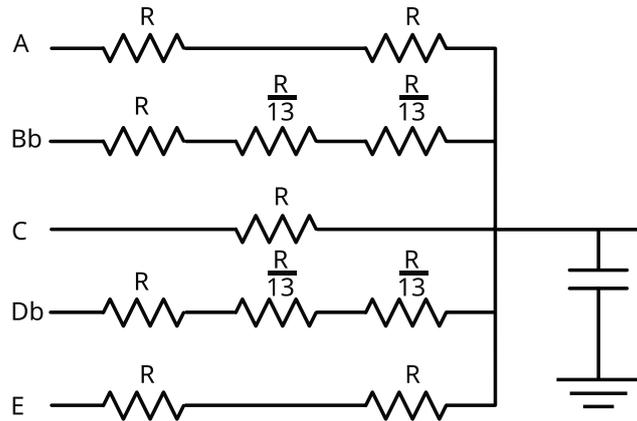


Figure 4.16: Adder circuit for scaling and adding the time-shifted signals

generates a current with respect to the signal. This current is inversely proportional to the weight. The weighted currents are then summed with the help of a load capacitor in the form of voltage. This summing network can be considered equivalent to a low-pass filter. The effective bandwidth of this low pass filter should be below the operating frequency such that the capacitor should be able to perform the integration of the signals for that particular operating frequency.

As discussed earlier for a perfect harmonic cancellation, signals A, and E should be scaled by $\frac{1}{2}$, signals Bb, and Db should be scaled by $0.866 (\frac{13}{15})$ and C should be scaled by 1. In this case, at steady state, signal C will charge the capacitor with a current proportional to $\frac{V_{DD}}{R}$ (this corresponds to scalar weight equal to 1), signals A, and E will charge the capacitor with a current proportional to $\frac{V_{DD}}{2R}$ (corresponds to scalar weight equal to 0.5), and signals Bb, Db will charge the capacitor with current proportional to $\frac{13V_{DD}}{15R}$ (this corresponds to scalar weight equal to $\frac{13}{15}$). It is important to ensure that the systematic mismatch from the adder should be as minimum as possible. This can be avoided by implementing these resistors with some combinations of a few resistors. Fig.4.17 shows one way that will reduce the systematic mismatch and the mismatch in the resistor due to routing [32].

Keeping linearity in mind a polysilicon-based resistor is used because of its highly linear nature and the load capacitor is a MOM capacitor. A first-order low pass filter is also added at the output of the adder circuit so that the higher-order harmonics can be attenuated.

4.2 HC-based signal generator with calibration using coarse-fine delay cell

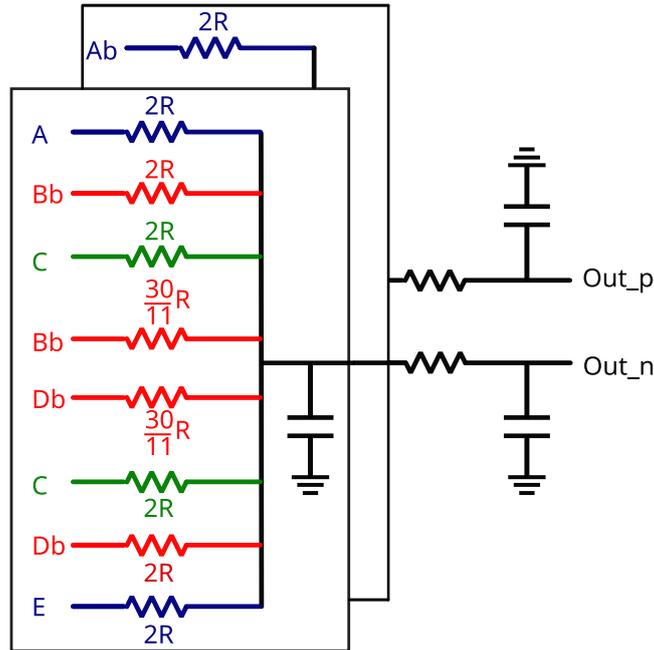


Figure 4.17: Adder circuit for scaling and adding the time-shifted signals

4.2.5 Simulation Results

The architecture of the complete sinusoidal signal generator is shown in Fig.4.8. The signal generator is simulated at the transistor level. The values of the control voltages in the coarse-fine delay cell are optimized to minimize the *THD* of the generated output signal. Firstly, to illustrate the capabilities of the delay cell to mitigate timing issues, Fig.4.18 shows the delay (ps) of one of the five phase-shifted square-wave signals in the y-axis and body bias voltage (V_{Bn}) in the x-axis for $V_{Gsn} = 1$ V and 0.5 V. It can be observed that once the coarse delay is fixed by V_{Gsn} , a range of delay can be achieved. For $V_{Gsn} = 1$ V the range of delay is 5.7 ps while it is 136 ps in the case of $V_{Gsn} = 0.5$ V.

Similarly, the duty cycle as a function of the V_{Bp} is shown in Fig.4.19 for $|V_{Gsp}| = 1$ V ($V_{Gsn} = 1$ V) and $|V_{Gsp}| = 0.5$ V ($V_{Gsn} = 0.5$ V). The gate to source voltage of P1 and N1 transistors are kept the same so that the sensitivity of duty cycle change and delay change are of the same order and the input and output duty cycle remain the same initially.

The simulation results of the complete signal generator at frequency 173.5 MHz before tuning and after tuning are illustrated in Fig.4.20 and 4.21 respectively. The simulations are done in this case while considering a $50\ \Omega$ GSGSG pads are present at

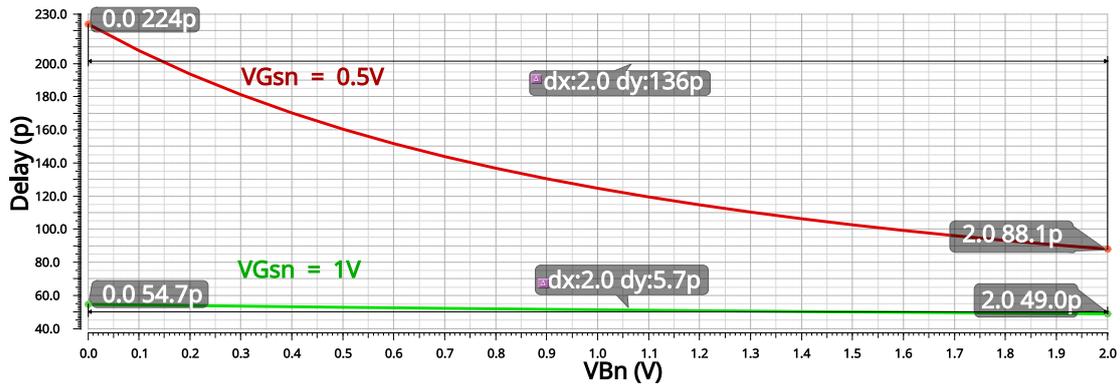


Figure 4.18: Simulation results of delay cell: Delay vs VB_n

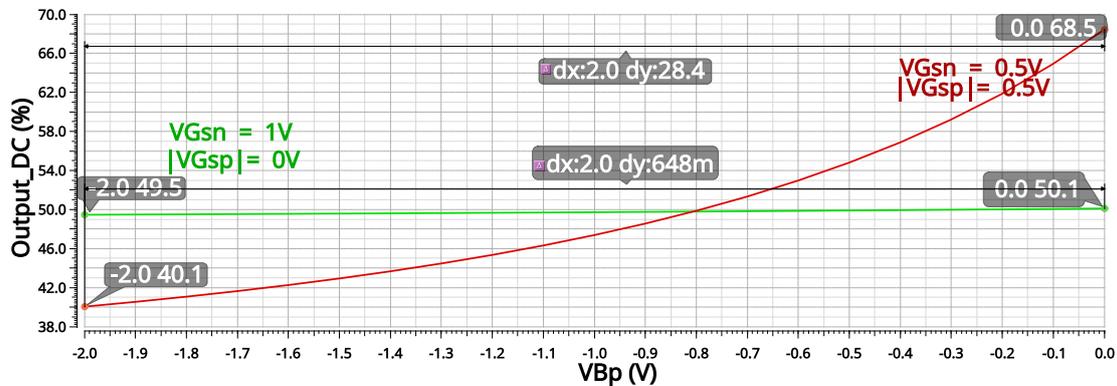


Figure 4.19: Simulation results of delay cell: Duty cycle vs VB_p

the output. Because of this, the power of the fundamental frequency is less than 0 dB. We will come back to this point in chapter 5. The observed *THD* of the signal before tuning is -20.11 dB which improved to -56 dB after tuning. Fig.4.22 and 4.23 show the spectrum of output sinusoidal signal at frequency 2.734 GHz before tuning and after tuning respectively. The observed *THD* of the signal before tuning is -32.2 dB which improved to -66 dB after tuning. The *THD* of the output signal in both frequencies was mainly limited by even harmonics and improved to a better value.

Fig.4.24 shows the *THD* as a function of the frequency of the output signal before (in red) and after tuning of the control voltages (in green), for frequencies ranging from 173 MHz to 2.73 GHz. It can be observed that the *THD* is improved to -56 dB at 173 MHz and improved to -66 dB at 2.73 GHz. This shows a significant improvement in all frequencies due to the calibration of timing issues. For frequencies greater than 500 MHz, the *THD* of the generated signal is consistently better than -60 dB. The

4.2 HC-based signal generator with calibration using coarse-fine delay cell

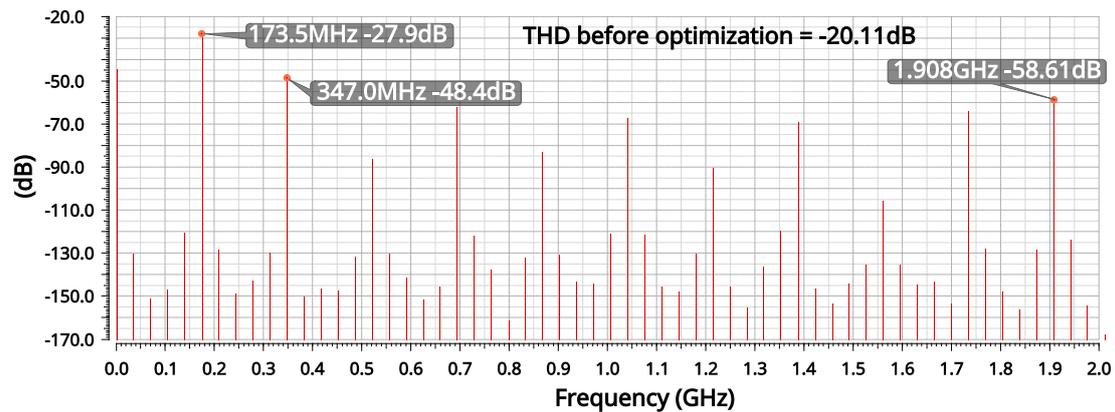


Figure 4.20: Spectrum of output signal at 173.5 MHz before tuning

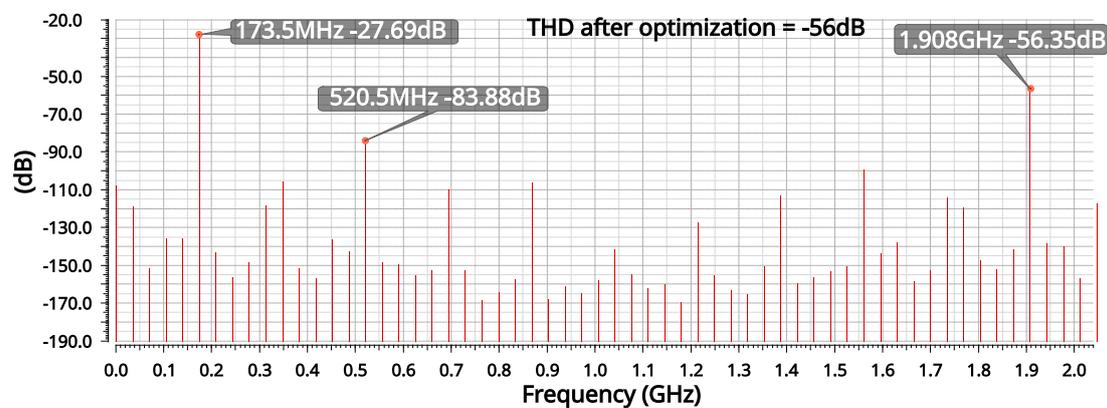


Figure 4.21: Spectrum of output signal at 173.5 MHz after tuning

tuning procedure is managed by an optimization algorithm that will be described in the next chapter.

4.2.6 Discussion and limitations

This type of signal generator addressed the challenges that one can face while implementing the first solution. Only 12 tuning knobs are required to optimize the timing inaccuracies which were 20 in the case of the first solution. Most importantly the tuning range can also be changed in this case which will be beneficial when a wide range of frequencies is being covered. For lower frequencies, the coarse delay can be increased by reducing the VGs voltage which will also change the sensitivity of the change in delay. However, this system also requires an external optimization so that the timing

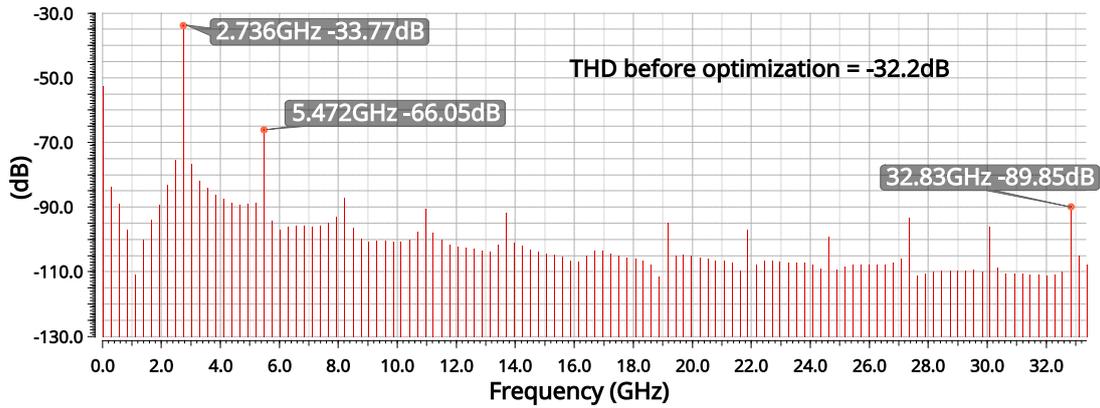


Figure 4.22: Spectrum of output signal at 2.73 GHz before tuning

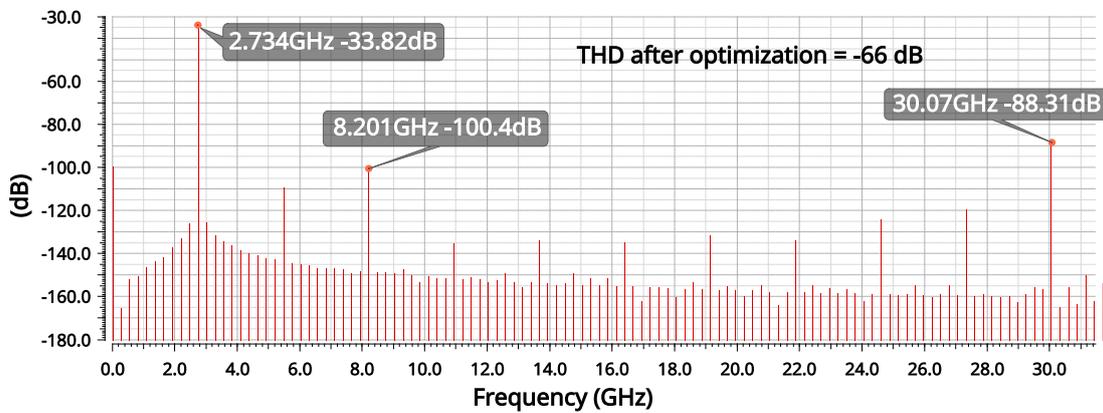


Figure 4.23: Spectrum of output signal at 2.73 GHz after tuning

inaccuracies can be corrected. These solutions may be interesting if the resources for implementing the optimization algorithm are available on-chip and can be repurposed for calibrating the generator. For reference, the needed resources should include some measurement capabilities to estimate the *THD* of the generated signal (for instance a high-speed digitizer, (ADC)) and some digital resources to implement the optimization algorithm. The third solution that we present in this chapter overcomes these needs by proposing a fully analog calibration solution.

4.3 HC-based signal generator with calibration based on negative feedback

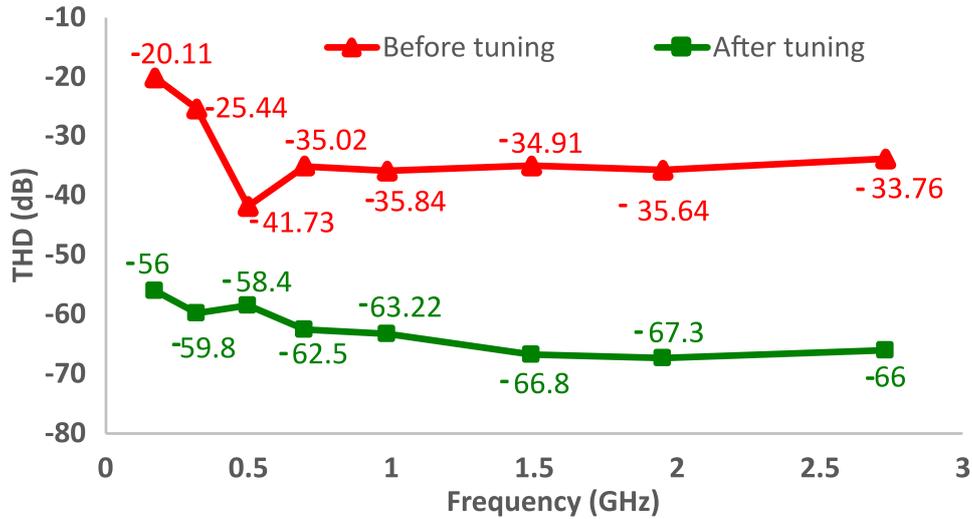


Figure 4.24: THD vs Frequency

4.3 HC-based signal generator with calibration based on negative feedback

The proposed architecture for a high-frequency harmonic canceling sinusoidal signal generator with an on-chip analog calibration is shown in Fig.4.25. The phase-shifted signals are generated from a 6-stage differential oscillator. Each signal is passed through a set of delay cells to correct the timing inaccuracies. The output of each delay cell is connected to a single-to-differential converter which generates the differential signals. The output signals of the single-to-differential converter are connected to the adder circuit where the signals are first scaled, added, and then followed by LPF to attenuate higher non-cancelable harmonics.

The calibration block consists of a set of negative feedback loops employed to monitor and correct the relative phase shifts between the square wave signals and their duty cycle. The goal of this calibration is first to convert the timing information of the signals to voltages. These voltages are then compared with the reference voltages calculated from the ideal configurations of the signals and with the help of the negative feedback the timing inaccuracies are corrected. The calibration block uses some of the mixed signal components such as AND gates, OPAMP, LPF, and switches (to reset some particular nodes in the circuits). In the calibration block, the output of a single-to-differential converter converts the timing information of these signals to voltages with the help of a LPF. These generated voltages are then compared with the reference voltages with the

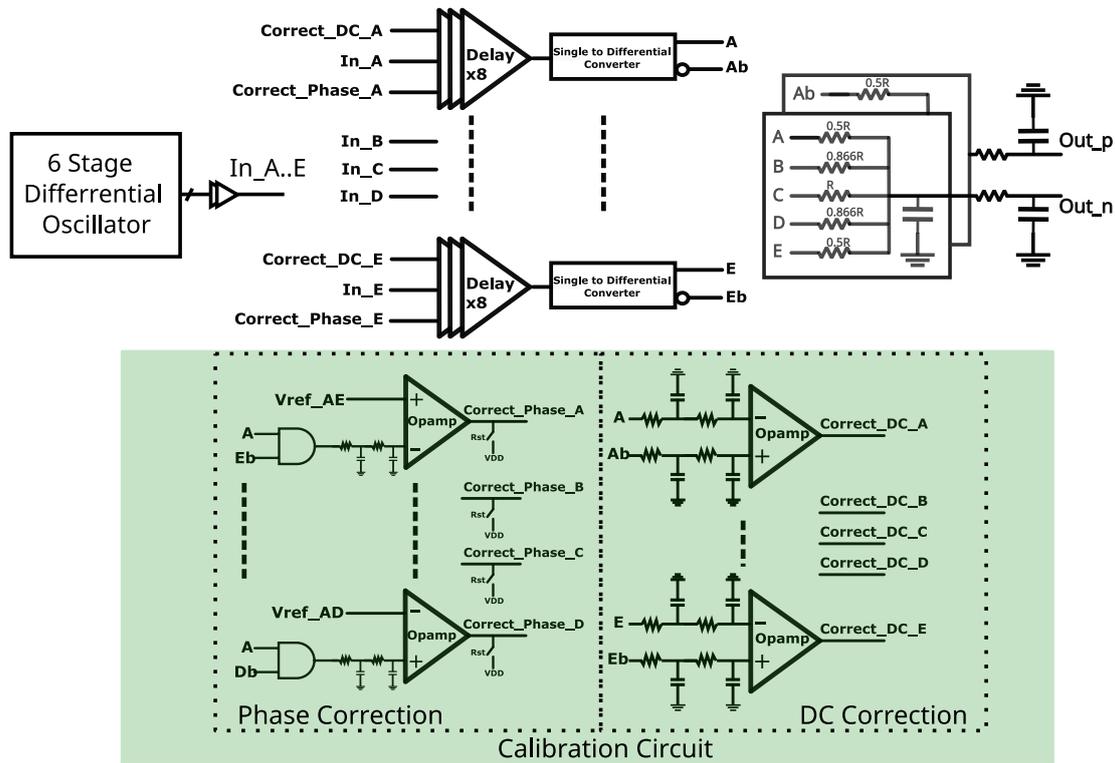


Figure 4.25: Block diagram of HC-based sinusoidal signal generator with calibration based on negative feedback

help of the OPAMP which controls the delay cell so that the timing information of the signals can be corrected.

The delay cell implemented in the previous solution is based on the change of threshold voltage of the transistor by changing the body-bias voltage. This implementation is based on the technological features of the FD-SOI technology. Although this delay cell can be used in the architecture in Fig.4.25, however, in this chapter, we propose an alternative implementation of a tunable delay cell suitable for bulk technologies.

4.3.1 Delay cell

The block diagram of the proposed delay cell is shown in Fig 4.26. It consists of two main blocks, a phase correction block and a duty cycle correction block. The phase correction block consists of two cascaded current-starved inverters, labeled I1 and I2, that introduce a tunable delay to the input signal by varying the control signal Correct_Phase. The duty cycle correction circuit is the same as discussed in section 4.1.1

4.3 HC-based signal generator with calibration based on negative feedback

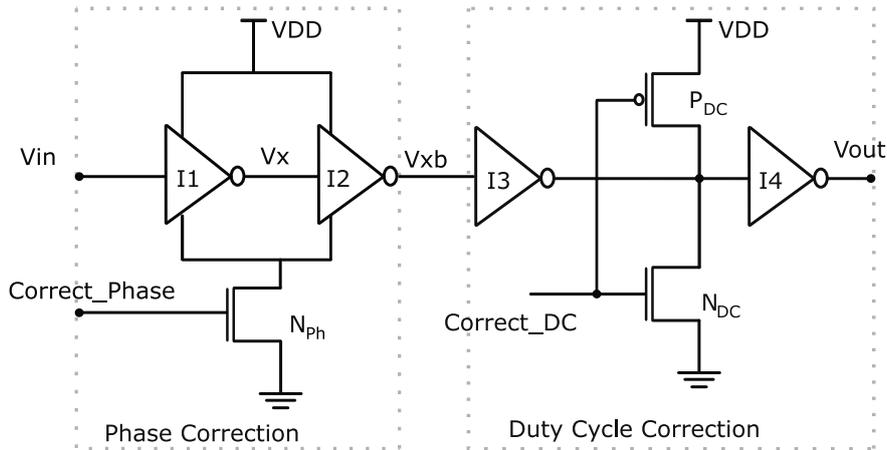


Figure 4.26: Modified delay cell

and will be discussed in detail in this section.

Phase correction

The functionality of the phase correction circuit is conceptually depicted in Fig 4.27. Fig 4.27.(a) represents the state of the phase correction circuit when the input signal transits from 0 to 1. During this phase, the V_x voltage changes from 1 to 0, and V_{xb} shifts from 0 to 1. For simplicity, we have ignored the transient states of transistors during the rising and falling edges. Transistor N_{ph} acts like a current source for inverter I1 and I2. Depending on the input state, only one of the nodes V_x or V_{xb} will be connected to the current source. C_x and C_{xb} are the equivalent parasitic capacitance at nodes V_x and V_{xb} respectively. The working of the phase change can be understood as follows: when the input signal transits from 0 to 1, the PMOS of inverter I1 and NMOS of inverter I2 are non-conductive while the NMOS of I1 and PMOS of I2 are conductive. The current source N_{ph} determines how quickly V_x discharges. By adjusting the Correct_Phase voltage, we can control this discharge rate. A lower Correct_Phase voltage results in a slower discharge, increasing the delay and thereby reducing the phase difference between the input signal and the reference signal, as shown in Fig.4.28. Conversely, a higher Correct_Phase voltage speeds up the discharge rate at the V_x node, advancing the signal. This increases the phase difference between the input signal and the reference signal. In essence, this circuit offers a mechanism to adjust the phase difference between signals.

Fig 4.27.(b) shows the phase correction circuit's behavior when the input transitions from 1 to 0. Here, V_x voltage changes from 0 to 1, while V_{xb} makes the opposite shift,

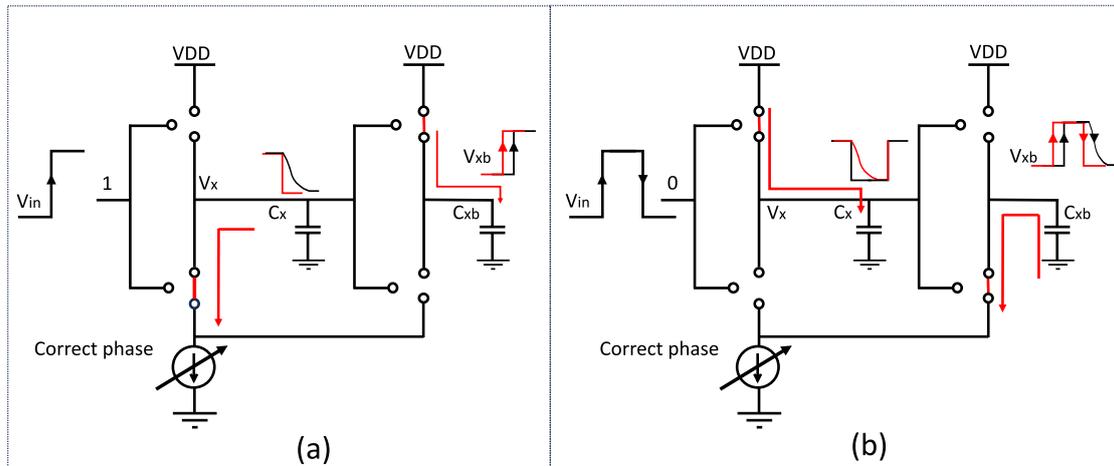


Figure 4.27: Conceptual diagram of phase correction: a) When V_{in} is changing from 0 to 1. b) When V_{in} is changing from 1 to 0.

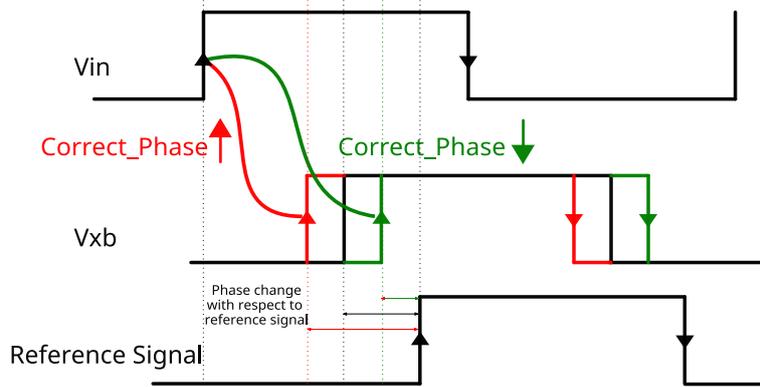


Figure 4.28: Timing diagram of change in delay with Correct_Phase

transiting from 1 to 0. In this case, the PMOS of inverter I1 and NMOS of inverter I2 are conductive while the NMOS of I1 and PMOS of I2 are non-conductive. The current source N_{ph} controls the falling edge of V_{xb} node by controlling the rate of discharge with the help of Correct_Phase voltage as discussed in the previous case. This ensures that the duty cycle of the input signal remains the same while changing the phase of the signal as shown in Fig.4.27. This can also be understood from the timing diagram illustrated in Fig.4.28. When the Correct_Phase voltage rises, the delay of the delay cell decreases, which essentially advances the signal's phase. Conversely, a drop in Correct_Phase results in the signal's phase delaying, yet the duty cycle at the output remains constant.

4.3 HC-based signal generator with calibration based on negative feedback

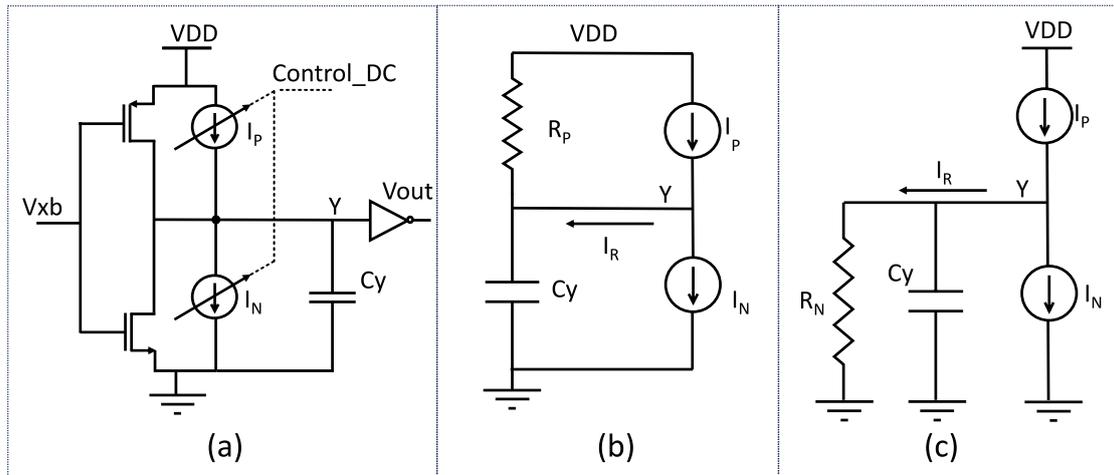


Figure 4.29: (a) Conceptual diagram of duty cycle correction circuit. (b) When input signal changing from 0 to 1 (c) When input signal changing from 1 to 0

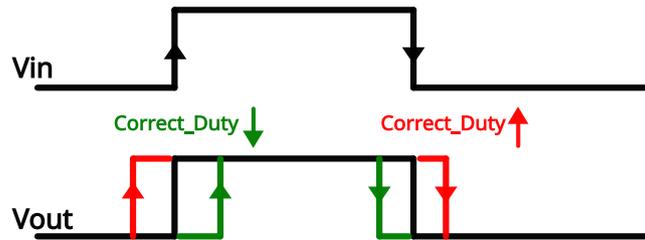


Figure 4.30: Timing diagram of change in duty cycle with $Correct_Duty$

Duty cycle correction

The conceptual diagram of the duty cycle correction circuit is illustrated in Fig.4.29.(a). This circuit is designed to modify the duty cycle of an input signal using a control voltage $Correct_DC$. It comprises three inverter stages in sequence. The output of the phase correction circuit, V_{xb} , feeds into the input of the first inverter stage. Following this, the output of the first stage is directly connected to the output of the second stage. C_y represents the total capacitance at node Y . Within the second stage, transistors P_{DC} and N_{DC} function as current sources, denoted as I_P and I_N respectively. By varying the $Correct_DC$ voltage, these transistors control the drive strength of the inverter in the first stage. As a result, the rise or fall time of the signal at node Y is adjusted by the second stage. The circuit's third stage acts as a comparator. It has a trip point approximating half of the supply voltage, ensuring the correction of the slewed rise or fall time of the signal. It is important to understand that the signals at node Y and

the output are 180 deg phase shifted. This implies that an increased duty cycle at node Y corresponds to a decreased duty cycle at the final output node. The duty cycle of the output signal contracts when the control voltage Correct_DC is decreased. On the other hand, increasing the Correct_DC voltage expands the duty cycle, as depicted in Fig.4.30.

Let us understand how the duty cycle changes when the control voltage Correct_Duty is changed. Consider the case when Vxb transits from 1 to 0, the voltage at node Y will transit from 0 to 1 as illustrated in Fig.4.29.(b). Ideally, PMOS will be in saturation for some time and then it will be in the triode region. But for simplicity, a constant resistance R_p is considered here. The capacitor Cy gets charged from two paths. One of the paths is from the supply (VDD), through the on-resistance of the PMOS (R_p). The other path is the residual current I_R which is the difference between the currents I_P and I_N as shown in equation 4.1.

$$I_R = I_P - I_N \quad (4.1)$$

When the voltage across node Y is 0, I_R will be dominated by I_P because the drain to source voltage of NMOS will be very small. The voltage across capacitor Cy will charge initially at a faster rate. As the voltage across Cy continues to rise up to a certain voltage, I_N increases and I_P decreases, and depending on Correct_DC voltage, I_R current will either remain positive for the whole time or get reduced to zero or can be negative for a particular control voltage. A similar will be the case when the voltage at node y transits from 1 to 0 as illustrated in Fig.4.29.(C). When the voltage across node Y is 1, I_R will be dominated by I_N . As the voltage across Cy continues to fall up to a certain voltage, and depending on Correct_DC voltage, I_R current will either remain positive for the whole time or get reduced to zero or can be negative for a particular control voltage.

When the control voltage is low, the current I_R remains positive. When the voltage at node Y transitions from 0 to 1, the rise time at node Y is reduced. Conversely, when the voltage changes from 1 to 0, the positive current I_R slows down the discharge rate of capacitor Cy, extending the fall time of the signal at node Y. This change in the rise and fall time impacts the subsequent comparator in the third stage. When the signal at node Y is on the rise, the comparator triggers earlier, advancing the falling edge of the output. Conversely, during a falling signal, the comparator triggers later, causing a delay in the rising edge of the output. This results in an increased duty cycle at node Y, which translates to a decreased duty cycle at the output, as evident in Fig.4.31.(a).

When the control voltage is high, I_R will be negative (I_R will be dominated by I_N). When the voltage at node Y transitions from 0 to 1, the rise time at node Y increases.

4.3 HC-based signal generator with calibration based on negative feedback

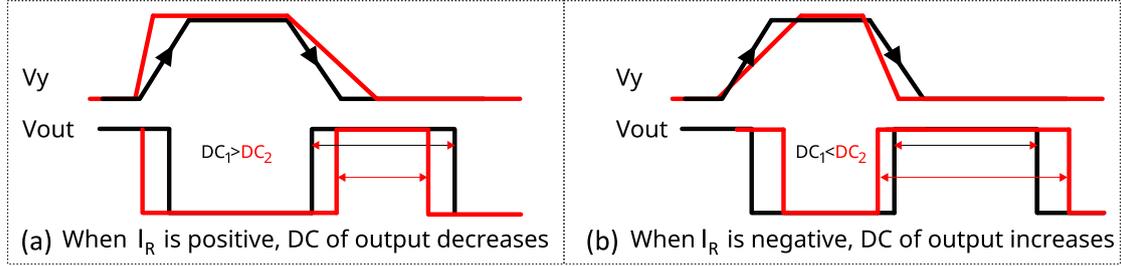


Figure 4.31: Timing diagram of change in duty cycle with Correct_Duty

Conversely, when the voltage changes from 1 to 0, the negative current I_R quickly discharges the capacitor C_y , decreasing the fall time of the signal at node Y. When the signal at node Y is on the rise, the comparator triggers later, delaying the falling edge of the output. Conversely, during a falling signal, the comparator triggers earlier, advancing the rising edge of the output. This results in a decreased duty cycle at node Y, which translates to an increased duty cycle at the output, as illustrated in Fig.4.31.(b). When the control voltage is around $\frac{V_{DD}}{2}$, the duty cycle of the signal will not change, as net I_R will be zero.

4.3.2 Monitoring and compensation of timing issues

The proposed on-chip calibration scheme uses the concept of negative feedback so that the DC control voltages Correct_Phase and Correct_DC are set to a required value such that the timing inaccuracies can be corrected with the help of a delay cell. First of all, the timing information of signals is converted to voltages and then compared with reference voltages so that the DC control voltages are set to the required voltages with the help of negative feedback loops.

Relative phase shifts

A simple technique to monitor the relative phase shifts between the square wave signals is implemented in this design. This technique uses an AND gate and a LPF to generate a voltage that is proportional to the phase difference between two signals. To illustrate the proposed technique, let us consider the ideal case where each of the 5 consecutive signals is time-shifted by $\frac{T}{12}$ (or phase-shifted by $\frac{\pi}{6}$), as illustrated in Fig.4.32.(a), where T is the time period of the signal and the maximum amplitude of the signal is $V_H = 1$. As can be observed, signal A and signal E are time-shifted by $\frac{4T}{12}$, so, from these two signals a pulse $A\bar{E}$ can be generated as shown in Fig.4.32.(b). The resulting pulse

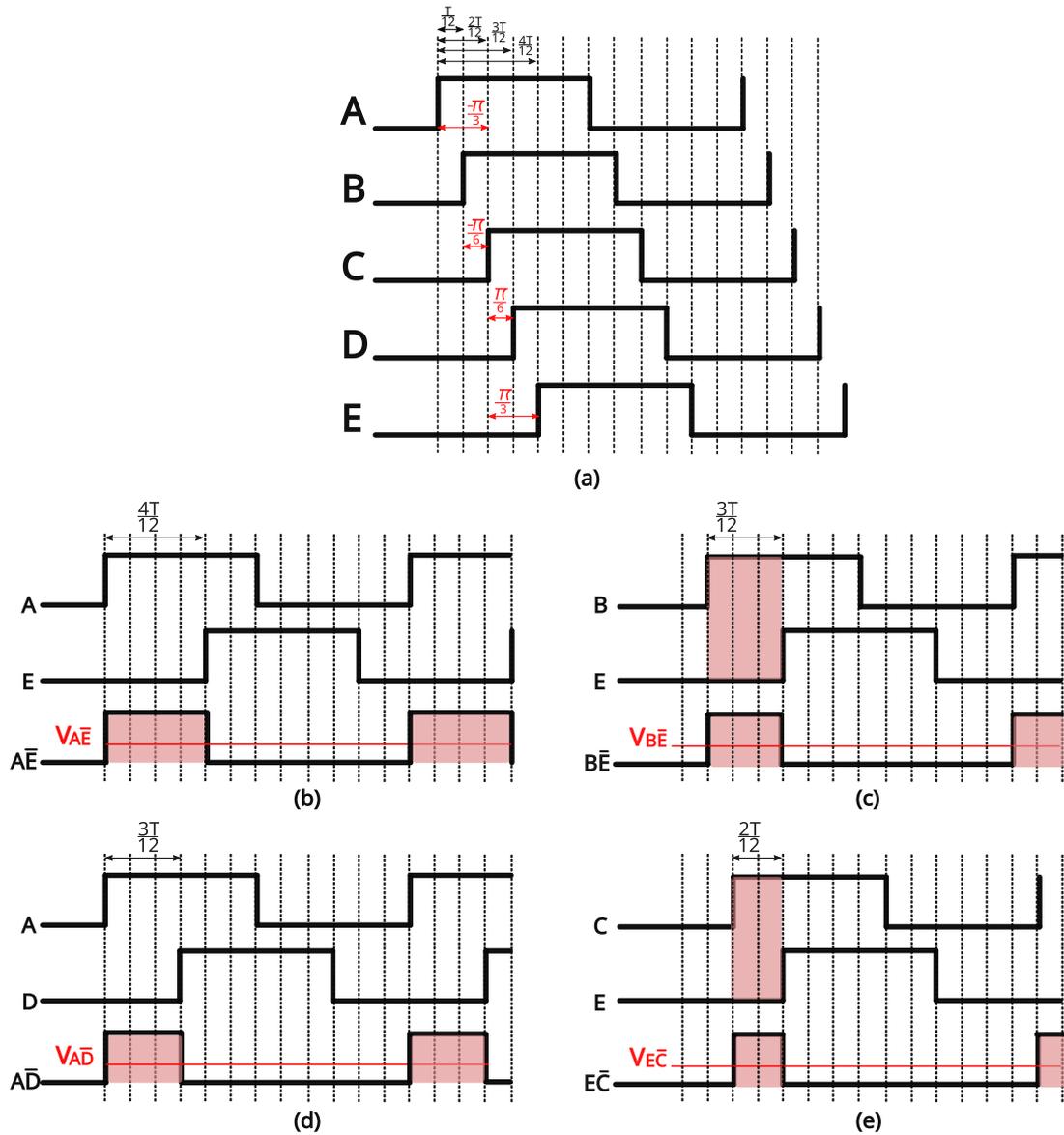


Figure 4.32: Timing diagram: (a) 5 time-shifted signals (b) Pulse generation of $A\bar{E}$ (c) Pulse generation of $B\bar{E}$ (d) Pulse generation of $A\bar{D}$ (e) Pulse generation of $E\bar{C}$

contains the phase difference information of signals A and E in the form of its average or DC value. The average of the generated pulse can be calculated as,

4.3 HC-based signal generator with calibration based on negative feedback

$$V_{\text{avg}_{A\bar{E}}} = \frac{1}{T} \int_0^T A\bar{E}(t) dt \quad (4.2)$$

$$= \frac{1}{T} \int_0^{\frac{4T}{12}} V_H dt \quad (4.3)$$

$$V_{\text{avg}_{A\bar{E}}} = \frac{V_H}{3} \quad (4.4)$$

The above equation 4.2 shows that a reference voltage can be calculated for an ideal phase difference between signals A and E. The calculated voltage can be used as a reference voltage for correcting the phase mismatch between signals A and E. Similarly, the reference voltages for correcting the phase difference between signals B, E, and A, D can be calculated which is equal to $\frac{V_H}{4}$ as shown in Fig.4.32.(c) and 4.32.(d). The reference voltage for correcting the phase difference between signals C and E is equal to $\frac{V_H}{6}$ as shown in Fig.4.32.(e). The pulses $A\bar{E}$, $B\bar{E}$, $A\bar{D}$, and $E\bar{C}$ are generated with the help of the AND gate. These pulses are then passed through a LPF. The output of the LPF is then connected to one of the inputs of the OPAMP in such a way that the whole loop is in negative feedback. The reference voltage is connected to the other end of the OPAMP.

Compensation of duty cycle

A 50% duty cycle ensures that there are no even harmonics present in the output sinusoidal signal. For differential signals, the duty cycle of the signal and its complementary should be the same. The difference in the duty cycle of two complementary signals can also be corrected by following the same technique as discussed in the case of phase correction. If differential signals are passed through two LPFs individually, the average voltages must be the same for the case when duty cycles are the same.

4.3.3 Implementation of negative feedback loops

A negative feedback system is an important building block in the realm of analog circuit design. The negative feedback system enhances the performance and reliability of other circuits by regulating and stabilizing the output. The most common circuit used for a negative feedback system is an operational amplifier (OPAMP). In our design, we have used the OPAMP circuit which has two stages, as shown in Fig.4.33.

The first stage is an OTA stage with PMOS as input transistors, and the second stage

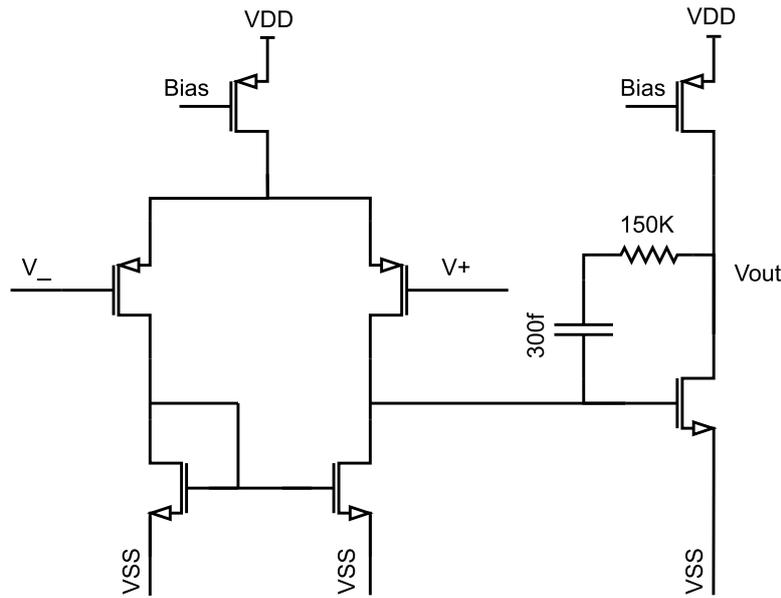


Figure 4.33: Two stage OPAMP

is a common source amplifier. The OPAMP is designed to operate at low power and the total current from the two stages is $2\mu\text{A}$. There are two poles in two stages and the second pole is nullified with the help of the zero that is present in between the output of the first stage and the output of the second stage. This ensures the overall system is a one-pole system. The unity gain bandwidth (UGB) of the OPAMP is 10 MHz.

The supply voltage of the whole system is 1 V. The reference voltages for correcting the phases can be calculated by placing the value of V_H in equation 4.2. When calculated, the reference voltage for the pulse $A\bar{E}$ is $V_{\text{avg},A\bar{E}}$ which is equal to 333.33 mV. The average voltage for pulses $B\bar{E}$ and $A\bar{D}$ is $V_{\text{avg},B\bar{E}} = V_{\text{avg},A\bar{D}} = 250\text{ mV}$. The average voltage for pulse $E\bar{C}$ is equal to $V_{\text{avg},E\bar{C}} = 166.66\text{ mV}$. These reference voltages for phase correction can be generated in multiple ways. For simplicity, the reference voltages are generated with the help of a resistor divider as shown in Fig.4.34.

The phase correction circuit consists of four OPAMPs, that are used for correcting the phases of signals A, B, C, and D using Correct_Phase_(A to D) control voltages respectively. The phase of the signal E is maintained at a constant value by keeping the control voltage, Correct_Phase_E, at a steady DC voltage, approximately 900, mV. The phase correction circuit for correcting the phase of signal A is shown in Fig.4.35.

The small signal equivalent of the phase correction circuit is shown in Fig.4.36. The small signal gain of the OPAMP is $g_m r_{O1}$, and the gain from the output of the OPAMP to the V- terminal of the OPAMP is represented by β . There are three poles in the loop, one

4.3 HC-based signal generator with calibration based on negative feedback

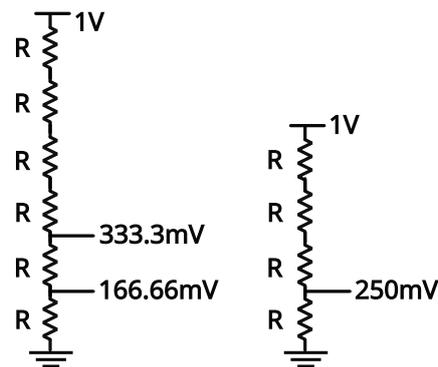


Figure 4.34: Small signal equivalent of the phase correction loop

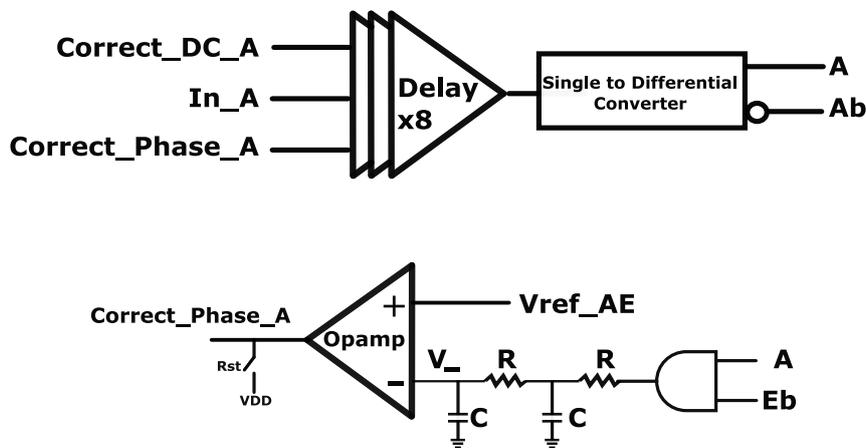


Figure 4.35: Negative feedback-based phase correction circuit: The output of OPAMP regulates the delay cell responsible for signal A

at the output of the OPAMP ($\frac{1}{r_{o1}c_{o1}}$), and two from the LPF ($\frac{1}{RC}$). The cutoff frequency of the LPF is around 100 MHz so that these two poles do not affect the stability of the whole system. The minimum phase margin of the loop is 60° , which also depends on different reference voltage values to correct different phases.

The duty cycle correction circuit for signals A and \bar{A} is shown in Fig.4.37. There are a total of five OPAMPs, used for correcting the duty cycle of all five signals and their complementary using Correct_Duty_(A to E) control voltages. The output of each single-to-differential converter is connected to a LPF that generates the average voltage of the signals. The average voltages of signals (A, B, C, D, and E) are connected to the negative terminal of the OPAMP. The average voltages generated by the complementary signals are used as reference voltages and are connected to the positive terminal of the

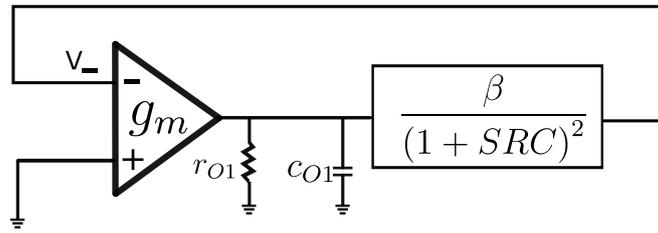


Figure 4.36: Small signal equivalent of the phase correction loop

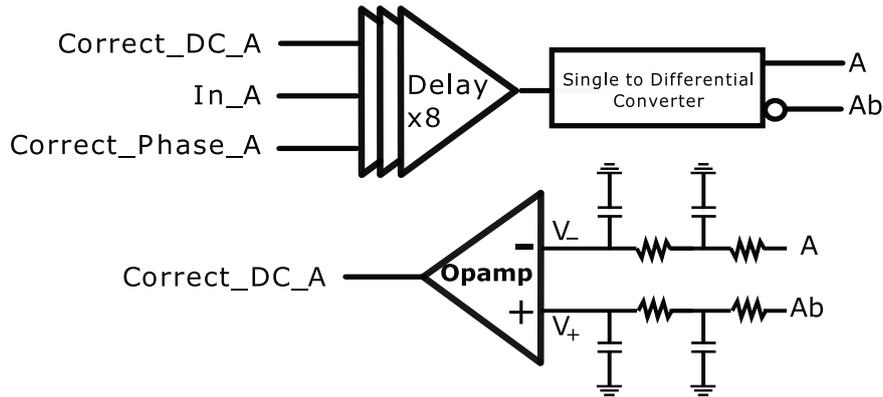


Figure 4.37: Negative feedback based duty cycle correction circuit: The output of OPAMP regulates the delay cell responsible for signal A

OPAMP. The output of the OPAMP is connected to the control voltage $Correct_DC$ of the delay cell responsible for duty cycle correction. The OPAMP that is used for duty cycle correction is the same as discussed in the case of the phase correction circuit. The average voltage generated by signal \bar{A} will act as the reference for the OPAMP. At a steady state, the average voltages at the input of the OPAMP will be the same.

4.3.4 Simulation Results

Delay cell characterization

To cover the correction for a wide range of output signal frequencies, eight delay cells are connected in series. These delay cells are programmed in such a way that only 4 delay cells are active when operating at a frequency range greater than 2 GHz while 8 delay cells are active when operating at a frequency below 2 GHz. To show the achievable correction range and the sensitivity of the tunable delay cell in the proposed architecture based on the feedback calibration loop, Fig.4.38 shows the delay of 8 delay cells

4.3 HC-based signal generator with calibration based on negative feedback

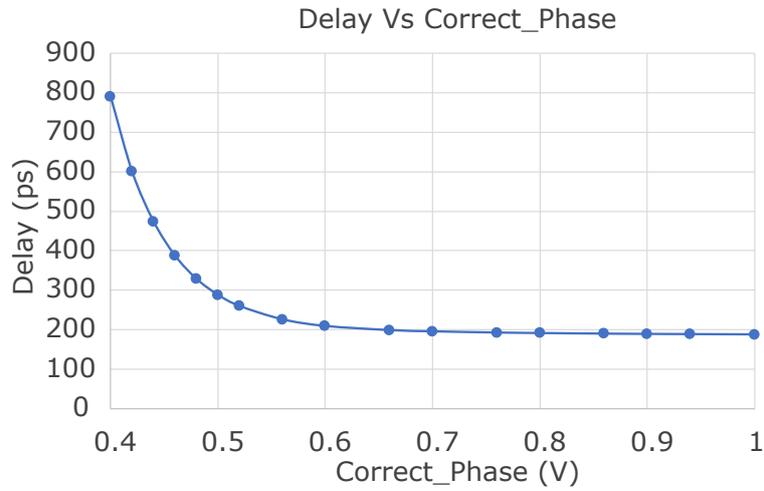


Figure 4.38

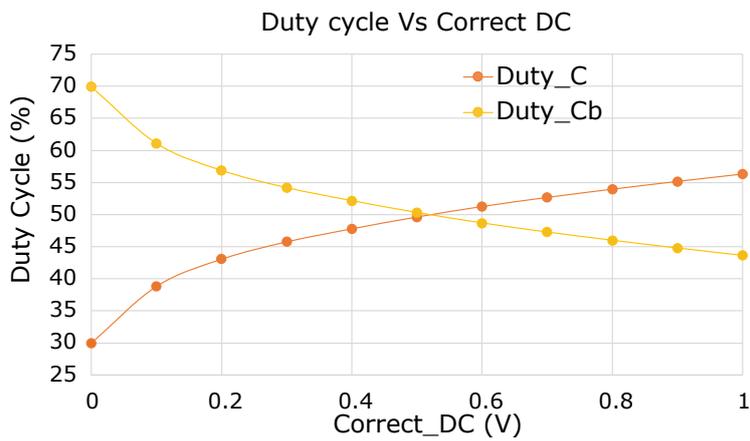


Figure 4.39

in the Y-axis and Correct_Phase in the X-axis. It can be observed that these delay cells offer a 600 ps delay range for an input control voltage varied from 400 mV to 1 V.

Fig.4.39 shows the duty cycle of the output signal in the Y-axis as a function of Correct_DC. The duty cycle correction spans roughly from +20% to -7% for a control signal varying from 0 V to 1 V. The variation ranges of the delay cell have been optimized to cover the maximum corner variations observed in a corner analysis according to the corner models in the process design kit (PDK) of the technology. The sensitivity to the control voltage and the range of the control voltages have been optimized together with the output swing of the OPAMPs in the feedback loop for correct behavior.

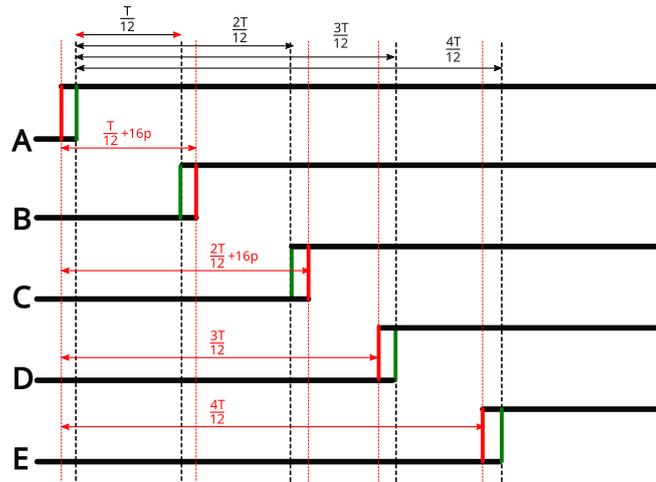


Figure 4.40: Worst case scenario of mismatch in phases in a 5-phase sinusoidal signal generator

To validate the functionality and the performance of the sinusoidal signal generator based on on-chip calibration, the worst-case mismatch (*SPE* and *DCV*) from the VCO and its signal path after the Monte Carlo simulation of 200 samples is considered. The absolute mismatch values were then added to the square wave sources in the test bench. The absolute value of the *SPE* is 8 ps when the worst-case scenario for harmonic cancellation is considered. The nonideal waveforms are shown in Fig.4.40, on the other hand, the worst-case duty cycle is around 46% which is kept for all signals. The *THD* of the output sinusoidal signal before optimization was -32 dB at 1 GHz frequency which improved to a value equal to -63.3 dB after the calibration loop was enabled. A reset signal (*Rst*) is used to initialize the nodes of the circuit in such a way that initially, the duty cycle correction starts while the phase correction circuit stays inactive so that both negative feedback loops must not affect each other. During the reset phase, all phase correction outputs of OPAMP (*Correct_Phase_X*) are fixed to VDD, at the same time the input of OPAMP responsible for duty cycle correction starts correcting the duty cycle of all signals. Fig.4.41 shows the transient behavior of the duty cycle correction circuit for signal C and its complementary when output frequency is 1 GHz. It is clear in the waveforms that the duty cycle of both signals converges close to 50% due to negative feedback. Once the duty cycle of the signal and its complementary part are approximately close to each other, the *Rst* is disabled (in this case at $1.2\mu\text{s}$) and the phase correction loop starts correcting the phases. Fig.4.42 shows the timing waveforms of the phase correction when output frequency is 1 GHz once *Rst* signal was disabled. In an ideal case, phase $Phase_{AE} = 333.33$ ps, $Phase_{A\bar{D}} = Phase_{\bar{B}E} = 250$ ps, and

4.3 HC-based signal generator with calibration based on negative feedback

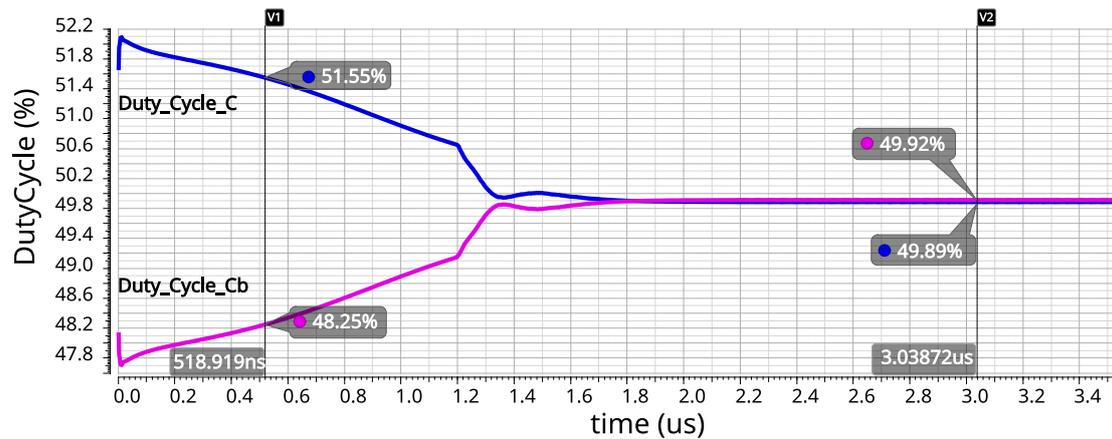


Figure 4.41: Transient simulation results of duty cycle calibration @ 1 GHz

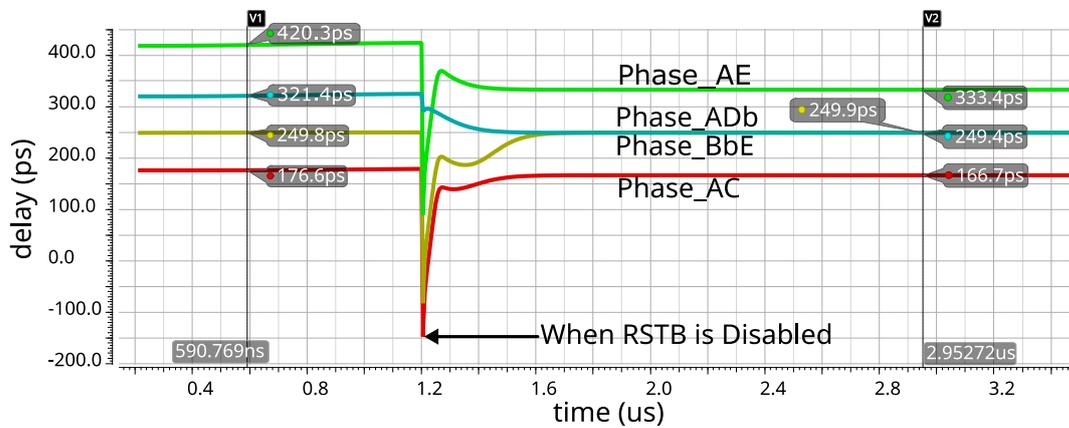


Figure 4.42: Transient simulation results of phase calibration @ 1 GHz

$Phase_AC = 166.66$ ps when output frequency is equal to 1 GHz. It is clear that the phases converge close to their ideal values with the help of negative feedback. Fig.4.43 shows the spectrum of the output signal after calibration is completed at 1 GHz frequency. The THD observed after calibration is -63.39 dB. The timing diagram of duty cycle calibration, phase calibration, and spectrum of output signal at 4 GHz is shown in Fig.4.44, Fig.4.45, and Fig.4.46 respectively. To give further insight into the feasibility of the proposed calibration approach, the calibration procedure was repeated for a wide range of generated output frequencies. The uncalibrated and calibrated THD across the considered frequency range are shown in Fig.4.47. It is clear to see that the proposed timing calibration loops enable a significant improvement in the linearity of the generated signals in the frequency range from 200 MHz to 4 GHz achieving a calibrated

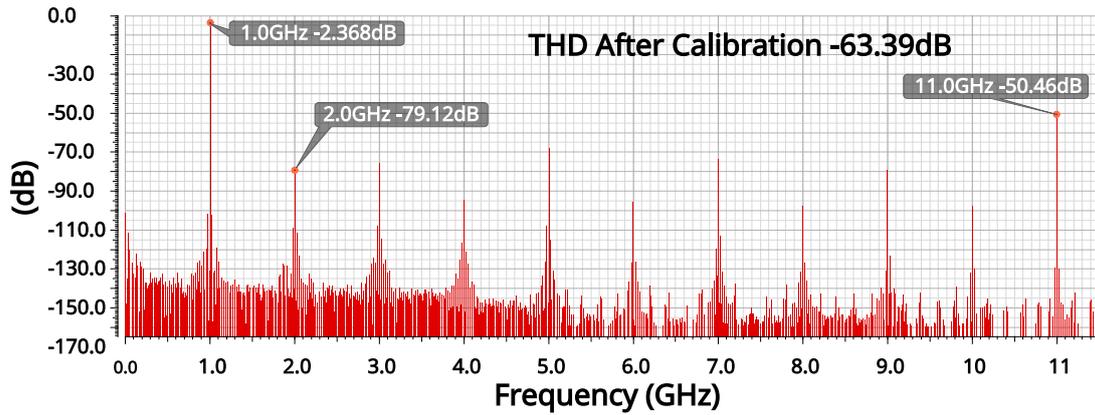


Figure 4.43: Spectrum of output signal after calibration @ 1 GHz; $THD = -63.39$ dB

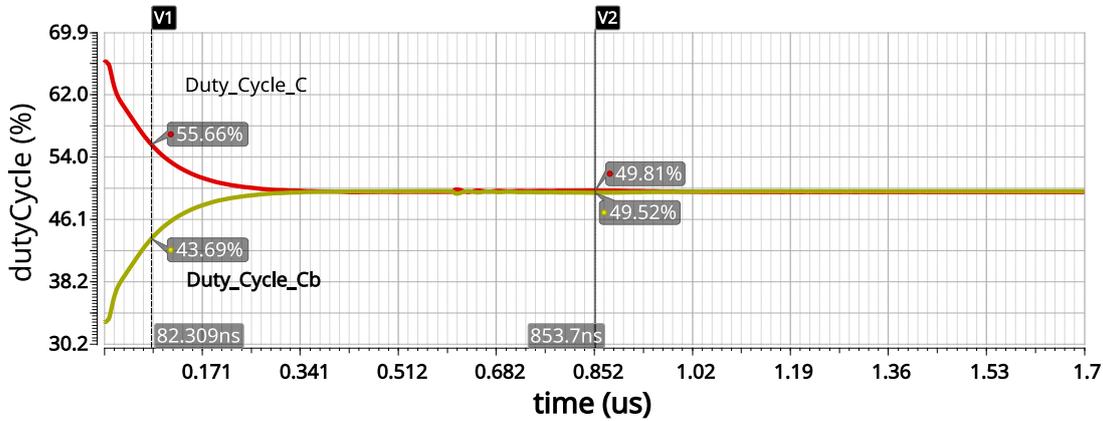


Figure 4.44: Transient simulation results of duty cycle calibration @ 4 GHz

THD consistently better than -60 dB.

4.3.5 Discussion and limitations

A sinusoidal signal generator based on an on-chip calibration that can generate a wide range of frequencies is discussed in this section. This signal generator uses multiple negative feedbacks for calibration. The negative feedback helped to correct the timing inaccuracies of the signals. It does not require any external optimization setup which reduces the complexity of testing. However, the cost of this solution is that it requires some area overhead to implement calibration circuitry. This solution has higher design complexity, keeping in mind that it needs to correct timing inaccuracies for a wide range of frequencies. In order to achieve a wide range, the programmability of delay cells and

4.3 HC-based signal generator with calibration based on negative feedback

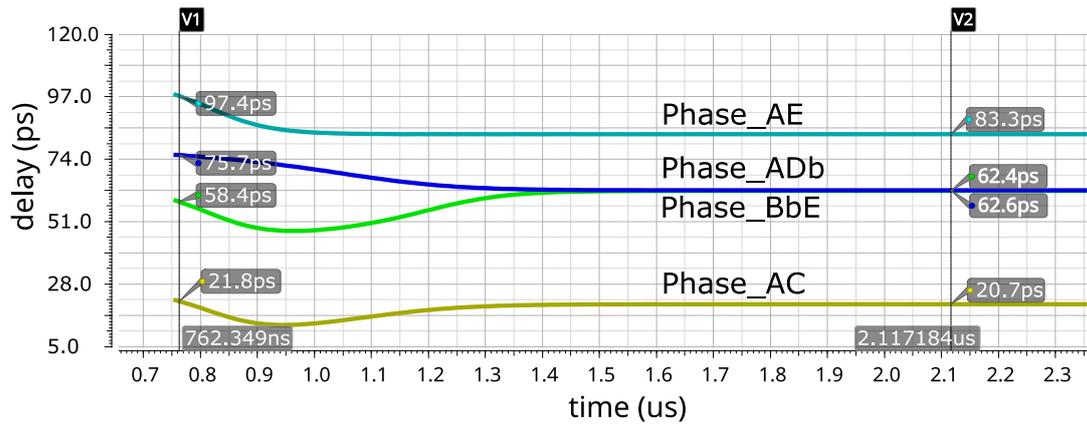


Figure 4.45: Transient simulation results of phase calibration @4 GHz

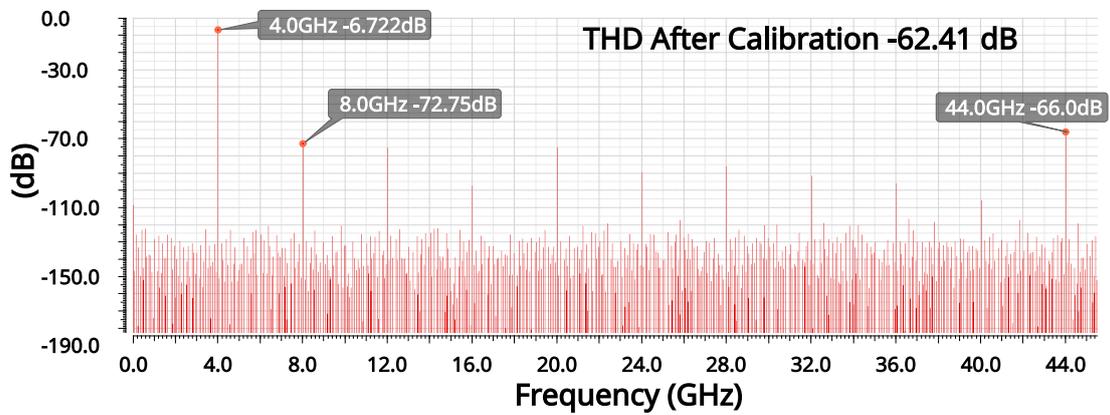


Figure 4.46: Spectrum of output signal after calibration @4 GHz; $THD = -62.41$ dB

the LPF can be done. The proposed calibration is sensitive to the process and mismatch variations on OMPAMPs employed in the feedback loops. In this regard, the mismatch within the OPAMP can be corrected by dynamic offset cancellation techniques since high-frequency clocks are already available within the system.

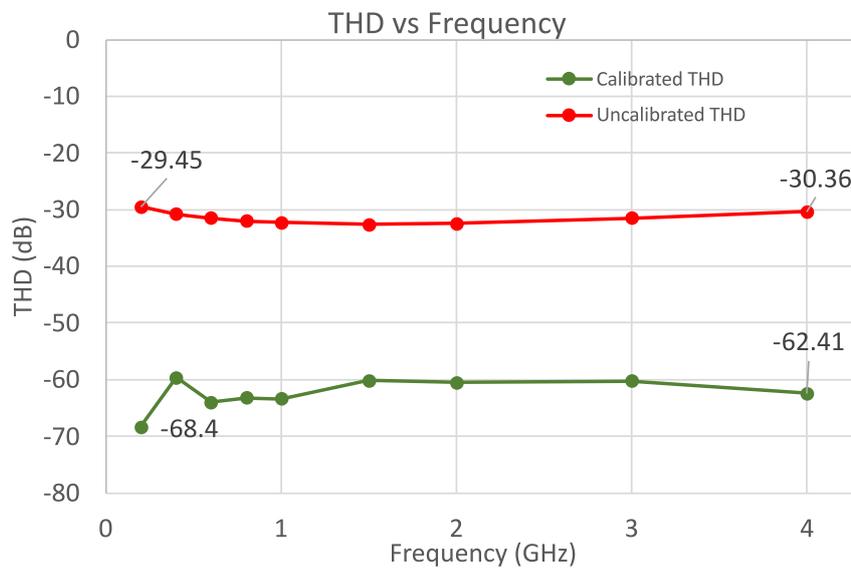


Figure 4.47: THD of the output sinusoidal signal before (Red) and after (Green) calibration

Measurement Results

In the previous chapter, we proposed three practical solutions that address the challenges of timing inaccuracies in conventional harmonic cancellation-based sinusoidal signal generators. For the proof of concept, we fabricated the signal generator based on a coarse-fine delay cell. The goal of this generator is to synthesize a high-quality sinusoidal signal for a wide range of frequencies. This work has been carried out in collaboration with STMicroelectronics Crolles in the framework of the Nano2022 program. The chip was designed in 28 nm FD-SOI technology and fabricated by STMicroelectronics.

5.1 Layout of the signal generator

The layout of the signal generator is shown in Fig. 5.1. The 6-stage fully differential oscillator is on the left side followed by the delay cells. The output of the delay cell is connected to the single-to-differential converter. Then these signals are added with the help of the adder. The layout of the oscillator is designed in such a way that each output has perfect symmetry. However, while routing the outputs of the oscillator, it is inevitable to have asymmetry in the paths, because some of the outputs are closer to the delay cells and some are not. This asymmetry will be reflected in the phase mismatch. The delay cell can take care of these mismatches during the calibration process.

As discussed in the last chapter, the transistors that are used in the design are LVT transistors of the FD-SOI technology which are fabricated in a flip well scheme. The

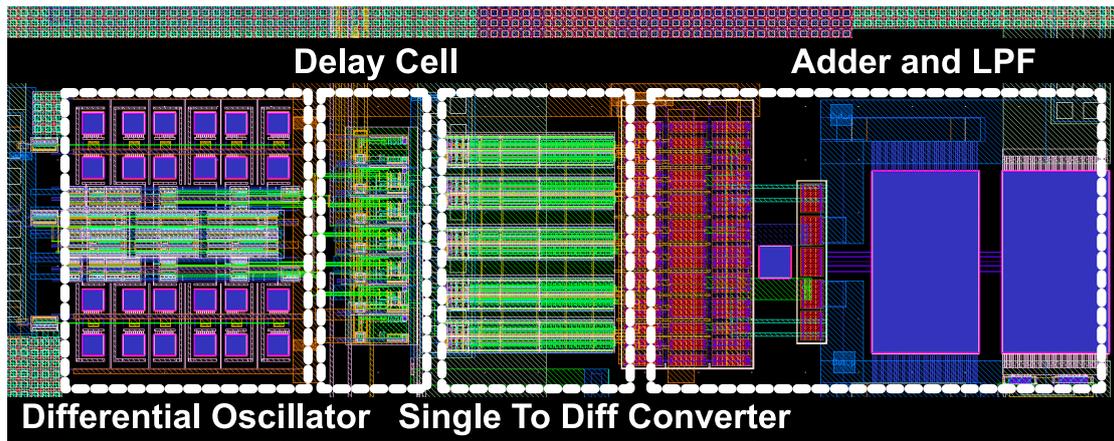


Figure 5.1: Layout of sinusoidal signal generator

NMOS is built on an n-well while the PMOS is built on a p-well. Transistors P1 and N3 in Fig.4.12 are designed to share the deep n-well. The deep n-well is biased to ground which will bias the substrate of N3 to ground, while the p-well of P1 is isolated and can be used for body biasing. The transistor N1 will be isolated from all transistors as it will be fabricated on n-well, and can be used for body biasing to correct the timing inaccuracies. The body of all other transistors is tied to the ground. There are a total of 7 delay cells out of which 5 are used for the correction of timing issues of 5 time-shifted signals and 2 delay cells are dummies. These delay cells are placed vertically and one of the two dummies is placed at the top and the other one is at the bottom. While routing the outputs of the delay cells to the single-to-differential converter, great care was taken to ensure that each signal path was of equal length to avoid timing inaccuracies attributable to these paths.

The resistors used in the adder circuit, shown in Fig.4.17, are polysilicon resistors, and the capacitors are MOM capacitors. Only two values of resistors ($2R$ and $\frac{30}{11}R$) are used to design the whole adder block to achieve minimal mismatch. The equivalent value of $2R$ is equal to $4\text{ K}\Omega$, and of $\frac{30}{11}R$ is equal to $5.463\text{ K}\Omega$. The value of the capacitor for integrating the signals is equal to 40.02 fF . The routing in the circuit contributes to the overall resistance, augmenting the resistance of the adder block. Consequently, resistors with higher values are chosen to ensure that the routing resistance contributes minimally. A system-level representation of the layout of the adder circuit is shown in Fig. 5.2.

The capacitors used at the output LPF have a value of 885.3 fF . In low-frequency mode operation of the signal generator, both capacitors are active. However, in high-frequency mode, only one capacitor is engaged.

5.2 Post layout simulation

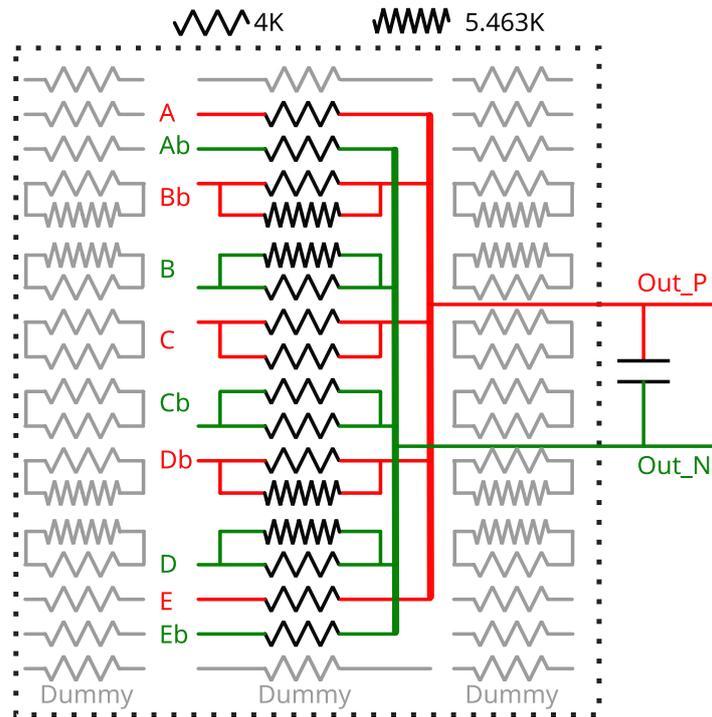
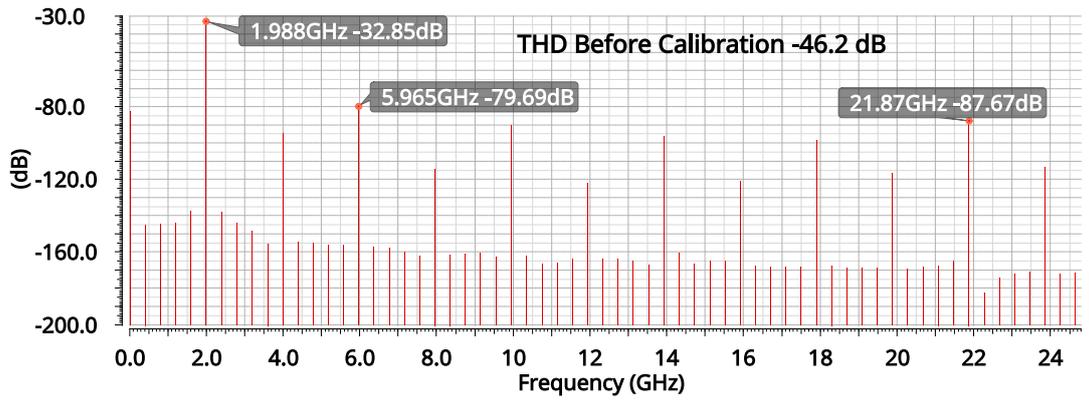


Figure 5.2: Layout of adder: System level representation

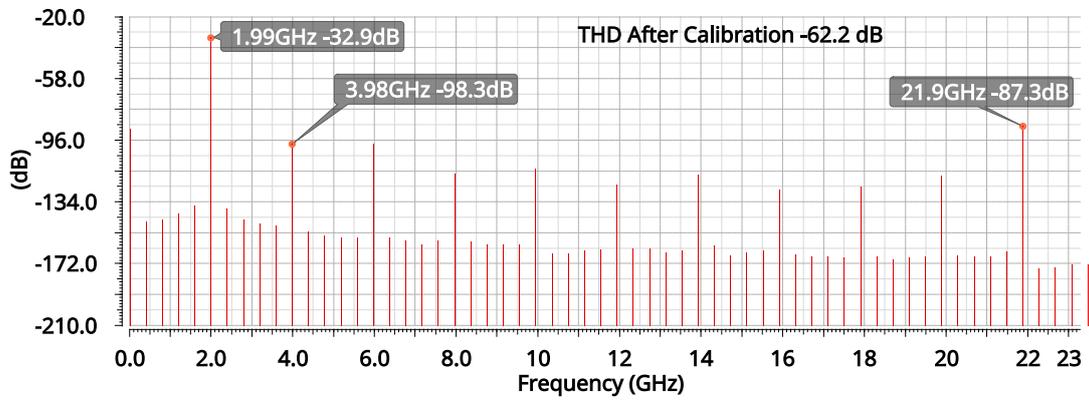
Ideally, an analog buffer should be placed at the output of the LPF to drive the output pads without significant loss of signal power. However, in our case, it isn't required as the focus of this work is to address the challenges associated with the generation of sinusoidal signals based on harmonic cancellation at higher frequencies. The inclusion of an analog buffer can be considered in future work.

5.2 Post layout simulation

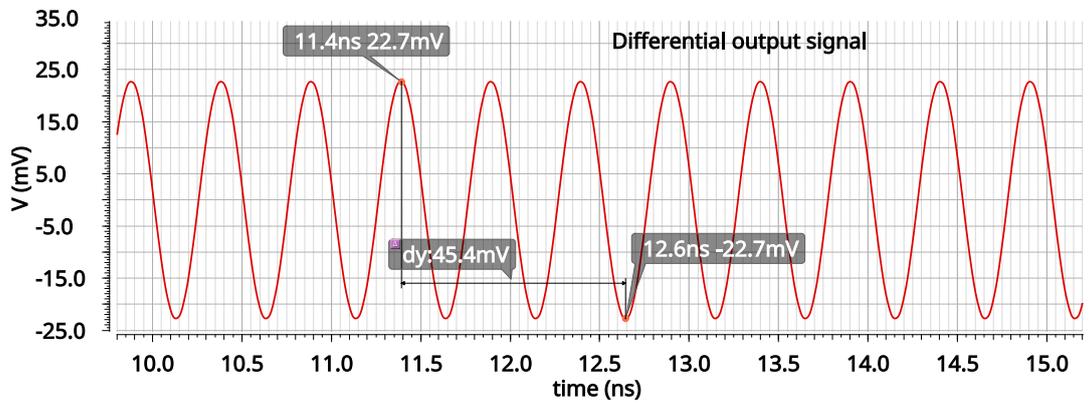
The schematic results presented in section 4.2.5 for this type of signal generator show that the *THD* of the output signal generated is better than -60 dB for frequencies greater than 500 MHz after calibration. The maximum achievable frequency in the schematic is 2.73 GHz with *THD* equal to -66 dB after calibration. However, after post-layout simulation, the maximum achievable frequency was reduced to 1.99 GHz due to parasitics. The layout of the whole generator was optimized so that a reasonably better *THD* could be observed at the output without calibration that can be improved to an acceptable value after calibration. Fig. 5.3a shows the spectrum of the output signal at



(a) Spectrum of the output signal before calibration



(b) Spectrum of the output signal after calibration



(c) Transient waveform of output signal after calibration

Figure 5.3: Output signal at 1.99 GHz

5.3 Prototype design

a maximum frequency which is 1.99 GHz before calibration, the *THD* of the signal is -46 dB. Once the calibration is carried out, the *THD* of the output signal is improved to -62 dB as shown in Fig. 5.3b. The transient waveform of the optimized output signal is also shown in Fig. 5.3c.

5.3 Prototype design

The contributions of two Ph.D. students were integrated onto a single chip. One of the contributions is a sinusoidal signal generator, which necessitates the sharing of some pads with the other contribution. This chip underwent bonding at the CIME facility. The block diagram of the full chip is shown in Fig. 5.4. The signal generator is on the right side, and pads in green color are used by signal generator. The part with grey color is dedicated to another contribution. A key requirement for bonding is that each pad must measure $53\ \mu\text{m} \times 53\ \mu\text{m}$. Additionally, it is essential to maintain a physical distance of $100\ \mu\text{m}$ between pads along the x-axis. The chip design includes two rows of pads, located at the top and bottom of the chip. Importantly, these two rows are not perfectly symmetrical along the horizontal axis. This deliberate design choice ensures that the bonding wires do not create short circuits when bonding the chip to the PCB. The physical distance between the pads along the y-axis is $118\ \mu\text{m}$.

There are a total of 30 pads out of which 18 pads are used for signal generator. The description of each pad is tabulated in Table 5.1. The sinusoidal signal generated at the output of the low pass filter is connected with the differential $50\ \Omega$ GSGSG pads which reduces the power of the generated signal. When the output is directly connected to GSGSG pads, the power of signal reduces to -32.8 dB. To avoid this power reduction, an analog buffer that can operate up to 3 GHz without introducing nonlinearity should be placed in between the LPF and the GSGSG pads. Because the focus of this thesis is to understand the challenges of generating high-frequency (a few hundred MHz to a few GHz) sinusoidal signals and mitigating those challenges, the design of a high-speed buffer is kept for future work. The layout of the chip is shown in Fig. 5.5, consisting of two contributions, one of them is a sinusoidal signal generator. The area of the whole chip including all pads is $1205 \times 1187\ \mu\text{m}^2$, whereas the area of the signal generator is $0.0113\ \text{mm}^2$.

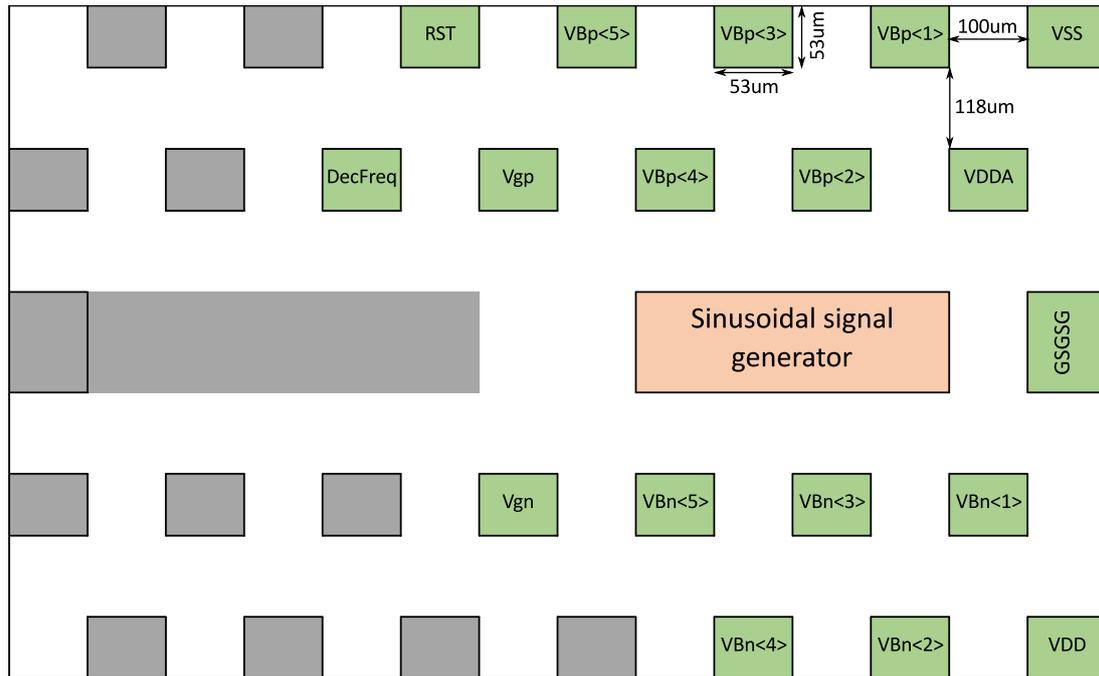


Figure 5.4: Block level representation of chip

5.4 Experimental Results

5.4.1 Test setup

The block level measurement setup is shown in Fig. 5.6 which consists of the NI-9264 DAC controlled from a computer for biasing the delay cells, the PCB on which the silicon die is mounted, the differential $50\ \Omega$ probes, a passive balun to convert the differential signal to single-ended, and spectrum analyzer for characterizing the *THD* of the output signal. A computer (optimizer) is used in the loop to automate the measurements. The optimizer runs a surrogate-assisted particle swarm optimization algorithm to predict the next input bias voltages so that the output signal can be optimized for the best THD. The layout of the PCB is shown in Fig. 5.7, where a DC connector is used to connect the NI DAC for biasing the delay cells. Level shifters are used for other parts of the chip which is the contribution from another Ph.D. student. Analog supply (VDDA) and digital supply (VDD) are supplied with external voltage sources. Fig. 5.8 represents the pin diagram of NI-9264 DAC which has 36 pins. 16 out of 36 pins are dedicated to DACs. However, only 12 pins are used in case of the signal generator. Each DAC has 16-bit inputs and it can generate an output ranging from $-10\ \text{V}$ to $10\ \text{V}$,

5.4 Experimental Results

Num	Pin Name	Type	Direction	Range	Description
1	Dec Frequency	DC	Input	1V	When 0, low-frequency range
					When 1, high-frequency range
2	VDD	DC	Supply	1V	Supply For Digital Blocks
3	VDDA	DC	Supply	1V	Supply for Oscillator
4	VSS	DC	Ground	0V	
9	VBp<5:1>	DC	Input	0 to -2V	For body biasing of PMOS transistors (Duty Cycle Correction)
14	VBn<5:1>	DC	Input	0 to +2V	For body biasing of NMOS transistors (Phase correction)
15	VGn	DC	Input	0 to 1V	For coarse tuning of delay
16	VGp	DC	Input	0 to 1V	For coarse tuning of duty cycle
17	RST	DC	Input	0 to 1V	Reset Signal
18	Out_p, Out_n	GSGSG	Output	0 to 1V	High-Frequency Analog Signal

Table 5.1: Pin Description

with a resolution output voltage equal to 0.305 mV. The picture of the die is shown in Fig. 5.9.

5.4.2 List of equipment

1. 1 x Dual GGB GSGSG 145 GHz Probe, 50 μ m, HKG68 & HKG70
2. 1 x Spectrum Analyzer FSW50, Maximum Frequency > 20 GHz, with 1.85 mm(V) and compatible 2.4 mm connectors
3. 1 x Balun (MARKI BAL26), Maximum Frequency > 20 GHz, with SMA connectors
4. 1 x RF cable for connecting the spectrum analyzer and the balun, spectrum side: V(F); balun side: SMA(F) (Diff to single converter)

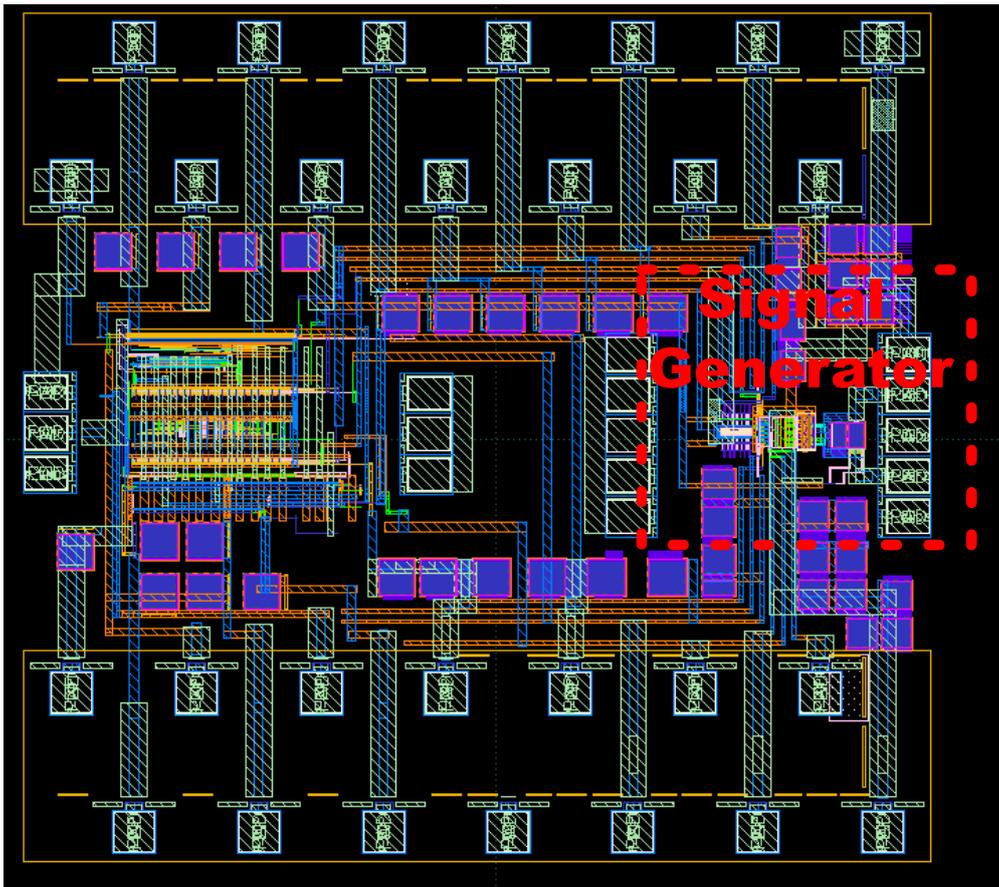


Figure 5.5: Layout of chip including pads

- Blue RF cable (V, M/M)
 - 1 x V(F) to SMA(M) adapter
5. 2 x RF cables, Balun (SMA) to 1 x 50 μm differential probes with maximum frequency > 20 GHz (GGB 145 GHz 0.8 mm)
- 2 x Blue RF cables (V, M/M) (W601-WM1WM1-03M)
 - 2 x SMA(M) to V(F) adapters for connecting to the balun
6. 2 x 1 mm RF cables (M/M) between the V cables and the RF probes
- 2 x approximately 10 cm transparent violet cables
 - 2 x V(F) to 1 mm(M) adapters
 - 2 x 1 mm(F) to 1 mm(F) adapters

5.5 Measurement procedure

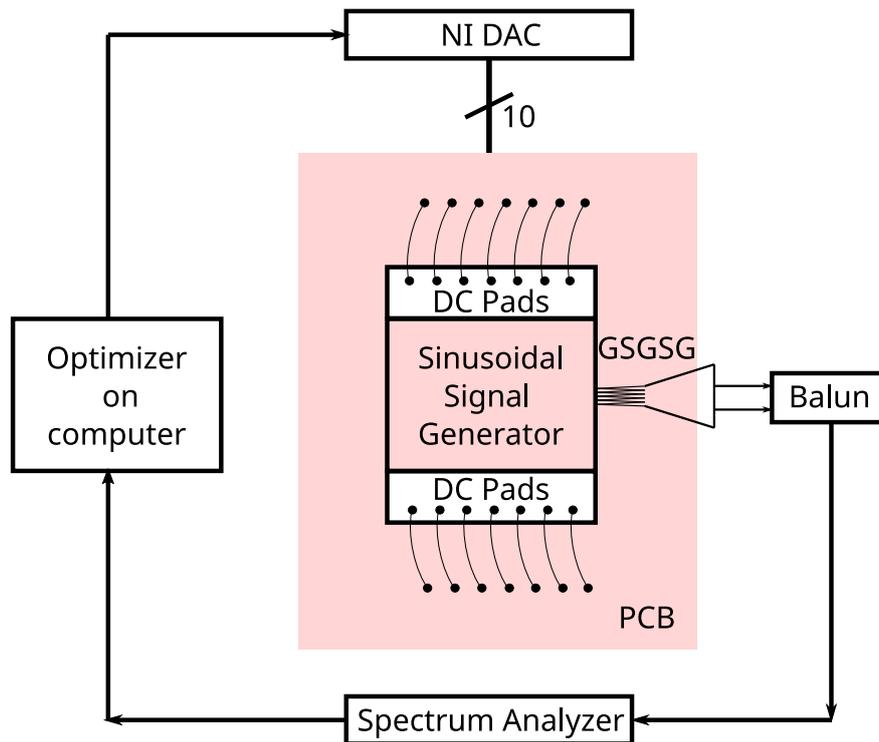


Figure 5.6: Block level representation of measurement setup

- 2 x 1 mm(F) to 0.8 mm(M) adapters
7. 2 x Power Supply Units (PSUs) for VDD and VDDA power supply: 2 x Keithley 2450
 8. 1 x NI DAQ 9264 with USB dock, SUB D37 cable, interface card, and ribbon cable
 9. 1 x PC for operating the NI DAQ

5.5 Measurement procedure

The goal of the measurements is to demonstrate the feasibility and performance of the proposed sinusoidal signal generator. The measurement setup is designed to manage the calibration process and measure the *THD* of the output signal. The whole measurement is automated with the help of an optimizer. The picture of the measurement setup is shown in Fig. 5.10. The optimizer regulates the bias voltages with the help of the

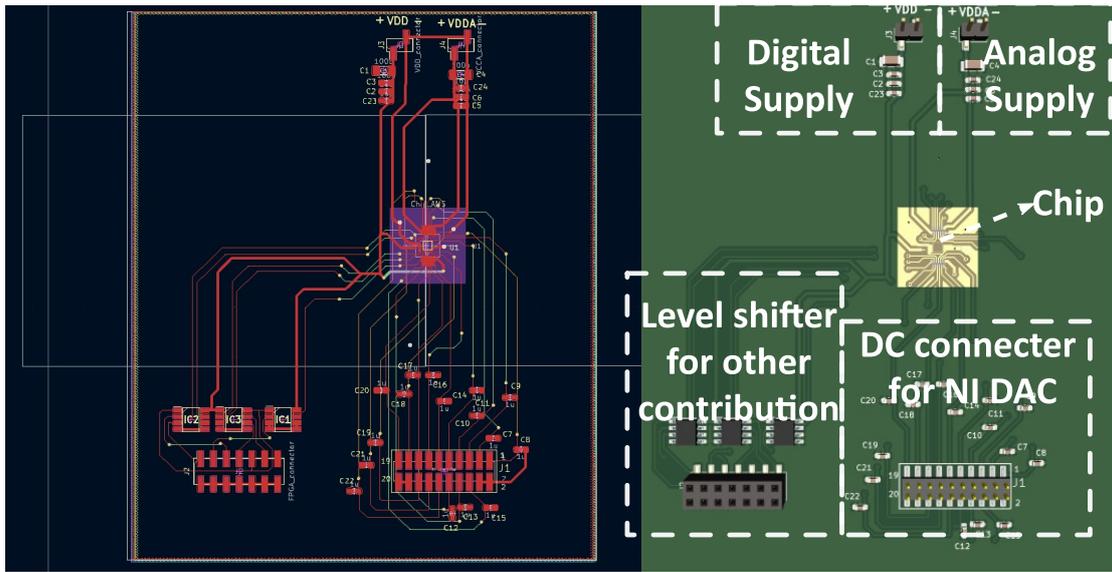


Figure 5.7: Layout of PCB

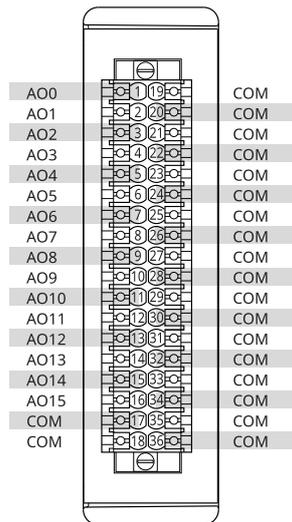


Figure 5.8: Pin diagram of NI-9264 DAC

NI DAC and optimizes the sinusoidal signal generator for the best *THD* of the output signal. The optimizer waits for some time (a few μs) so that the output signal transients are settled, then requests the spectrum analyzer to give the *THD* value of the output signal for a particular measurement. The optimizer runs an optimization algorithm that predicts the next set of bias voltages depending on the present and past *THD* values and their bias voltages. Multiple algorithms can be implemented to optimize a particular

5.5 Measurement procedure

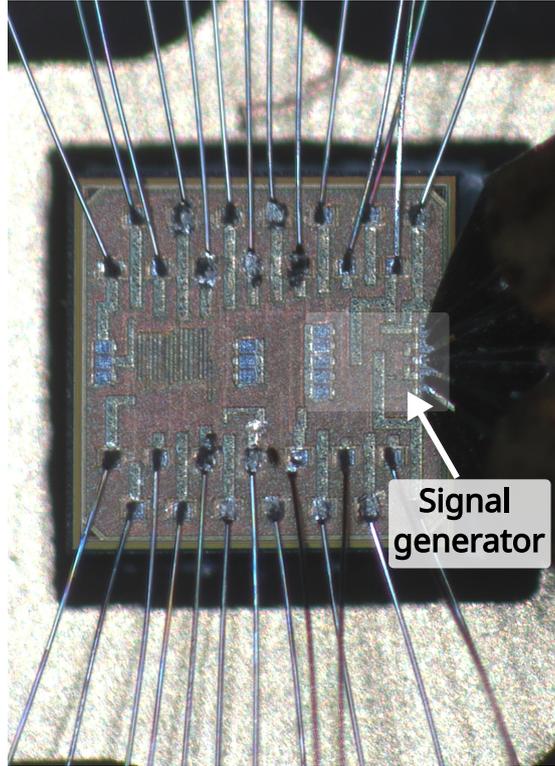


Figure 5.9: The photograph of the die of sinusoidal signal generator

problem. Optimizing the sinusoidal signal generator is a multi-variable problem, where the THD of the output signal is a function of 12 bias voltages having different ranges of values:

$$THD = f(VBp\langle i \rangle, VBn\langle i \rangle, VGn, VGp) \quad (5.1)$$

where, $\langle i \rangle = 1$ to 5 , $VBp\langle i \rangle = -1.8$ V to 0 V, $VBn\langle i \rangle = 0$ V to 1.8 V, $VGn = 0$ V to 0.6 V, $VGp = 0$ V to 0.4 V.

One of the optimization algorithms based on the Gradient Descent algorithm was implemented by [32] for optimizing the sinusoidal signal generator. In this work, the signal generator uses 10 3 – bit binary weighted capacitor banks, which are digitally controlled. 5 capacitor banks are used for correcting the phases of the signal and the other 5 capacitor banks are used for correcting the duty cycle of the signals. This algorithm iteratively tunes the phases and the duty cycle of the signals for the best THD value. However, concerning the proposed design, the 16-bit NI DAC and a wide range of calibration voltages increase the search space for the best solution that also increases the optimization time if the Gradient Descent algorithm is considered for optimization.

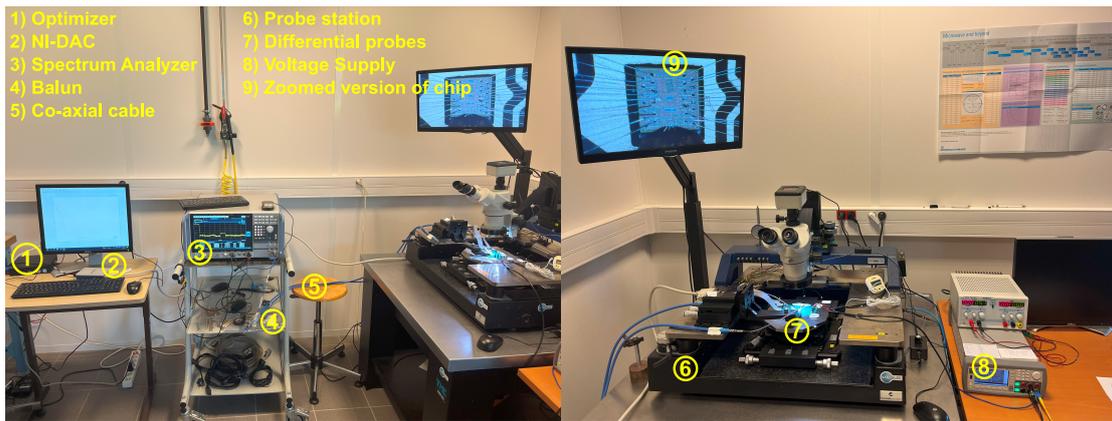


Figure 5.10: Measurement setup

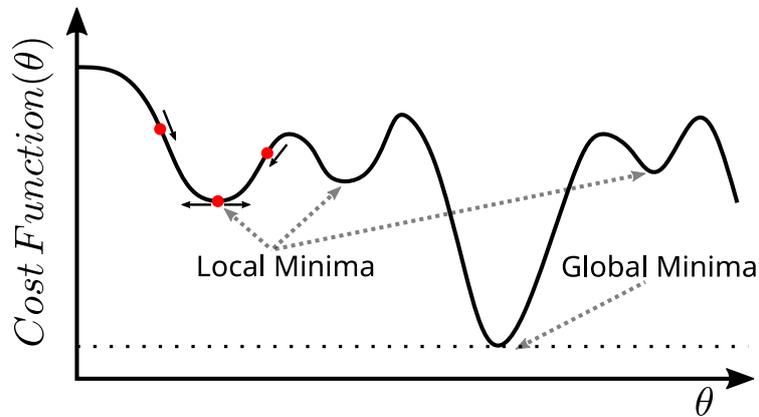


Figure 5.11: Gradient Descent Optimization for a particular optimization problem

Moreover, since this is a deterministic optimization algorithm, the best solution to any problem can sometimes stuck at the local best solution but not the global best solution. It can be understood from Fig. 5.11. This figure represents the cost function that needs to be minimized for a single variable problem. The cost function has multiple minimum values and if the minimization process does not start from the correct point then it can stuck at the local minima as shown in the figure by a red point. To overcome these problems, a surrogate-assisted Particle Swarm optimization algorithm is implemented which is discussed below.

5.5 Measurement procedure

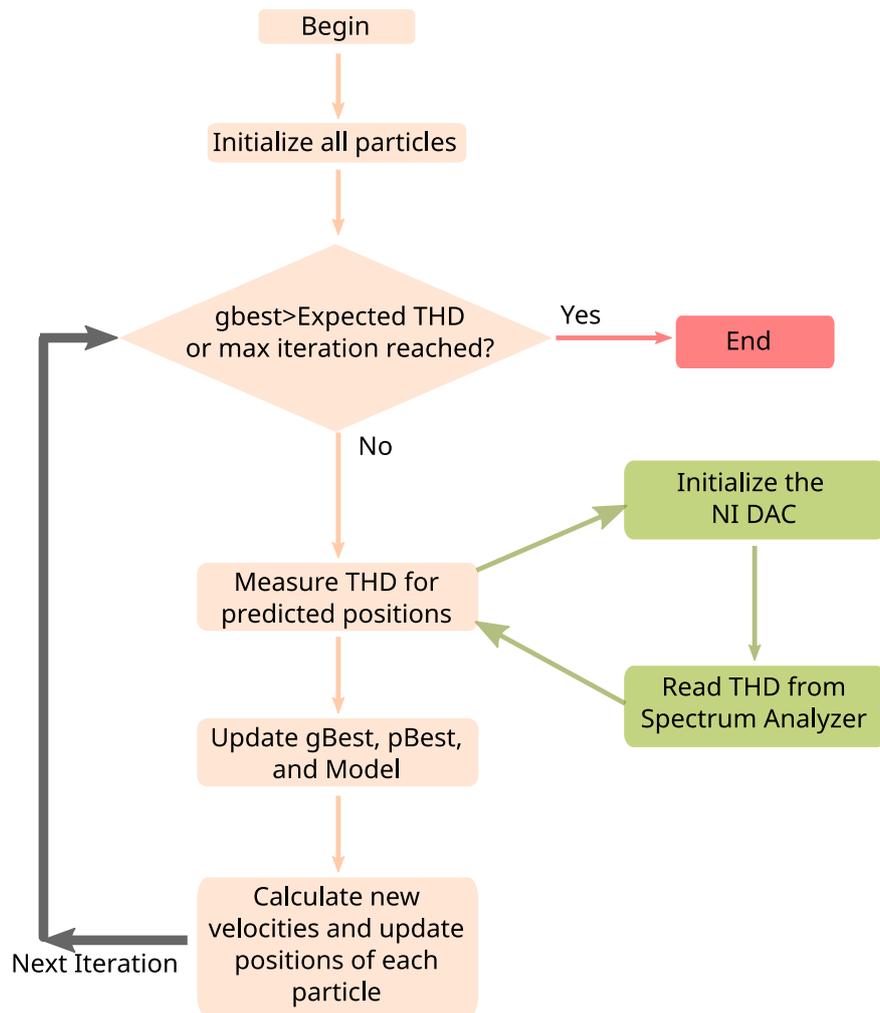


Figure 5.12: Flow chart of the Particle Swarm Optimization algorithm used in measurement

5.5.1 Surrogate-assisted particle swarm optimization algorithm

One of the popular algorithms for multi-variable problems is the Particle Swarm optimization (PSO) algorithm which was introduced in 1995 by Kennedy and Eberhart [81]. PSO is used to solve multi-variable optimization problems for finding either global minima or global maxima of the objective function of the problem. This algorithm is inspired by the nature that is the social behavior of fish schooling or bird flocking. A population in PSO is the collection of particles that moves along the search space to find the best solution by changing their positions and velocities. A particle can be a potential solution in a wide search space. The particles communicate with each other and share

their best-known positions which are also called personal bests and global bests from the optimum solution. The personal best (pBest) is the position of a particle in a population or swarm while the global best position (gBest) is the best position among all the particles in all the iterations. In each iteration, the velocity of the particle is updated keeping their pBest and gBest into account so that the best position from the solution can be achieved. The iteration process is terminated once the condition of either the maximum number of iterations is reached or the best solution is achieved. This can also be understood from the flow chart illustrated in Fig. 5.12, the part shown in green color is for external components other than the optimizer such as the spectrum analyzer and NI-DAC.

The PSO solves the problem of the gBest but at the cost of time [82] that can be critical in some applications, for example, if one wants to save the total optimization time. A surrogate-assisted PSO (SAPSO) solves this problem by utilizing a surrogate model (also known as a meta-model) for a given optimization problem. SAPSO approximates the objective function with negligible computation cost which is the measurement time in our case. A surrogate model is a simple machine learning-based model for example, a polynomial approximation model, an artificial neural network, a support vector machine, and a radial basis function network (RBFN), etc. An RBFN-based surrogate model performs best for problems with a great degree of nonlinearity on small training data and scales as well as the number of variables increase [83–85] which is the reason that RBFN is chosen in our case. In PSO, the evaluation is done for each particle in the population. However, in the case of SAPSO, only the particle with a higher possibility of having the local best (pBest) is evaluated for a given objective function. The operation principle is then similar to the statistical blockade proposed in [86, 87] for speeding up Monte Carlo simulation and test metric evaluation. The surrogate model predicts the value of the objective function for a particular position which is predicted from the PSO, and saves the measurement time by recognizing if the evaluation will be better than the previous pBest. This helps in avoiding the redundant positions generated from PSO and saves measurement time. The flow chart of the SAPSO-based optimization is shown in Fig. 5.13.

In context to the signal generator, a particle consists of a position which is the biasing voltage value of each delay cell. Particularly in this case, 20 particles are considered. Initially, 50 random positions are assigned within the voltage range of each DC pad. Then RBFN model is created with the help of these 50 positions. After that, the measurements are done for some number of iterations. In this, 20 positions are first predicted using PSO, then with the help of the RBFN model only those positions are proceeded for measurements for which the model predicts a better pBest. In each

5.5 Measurement procedure

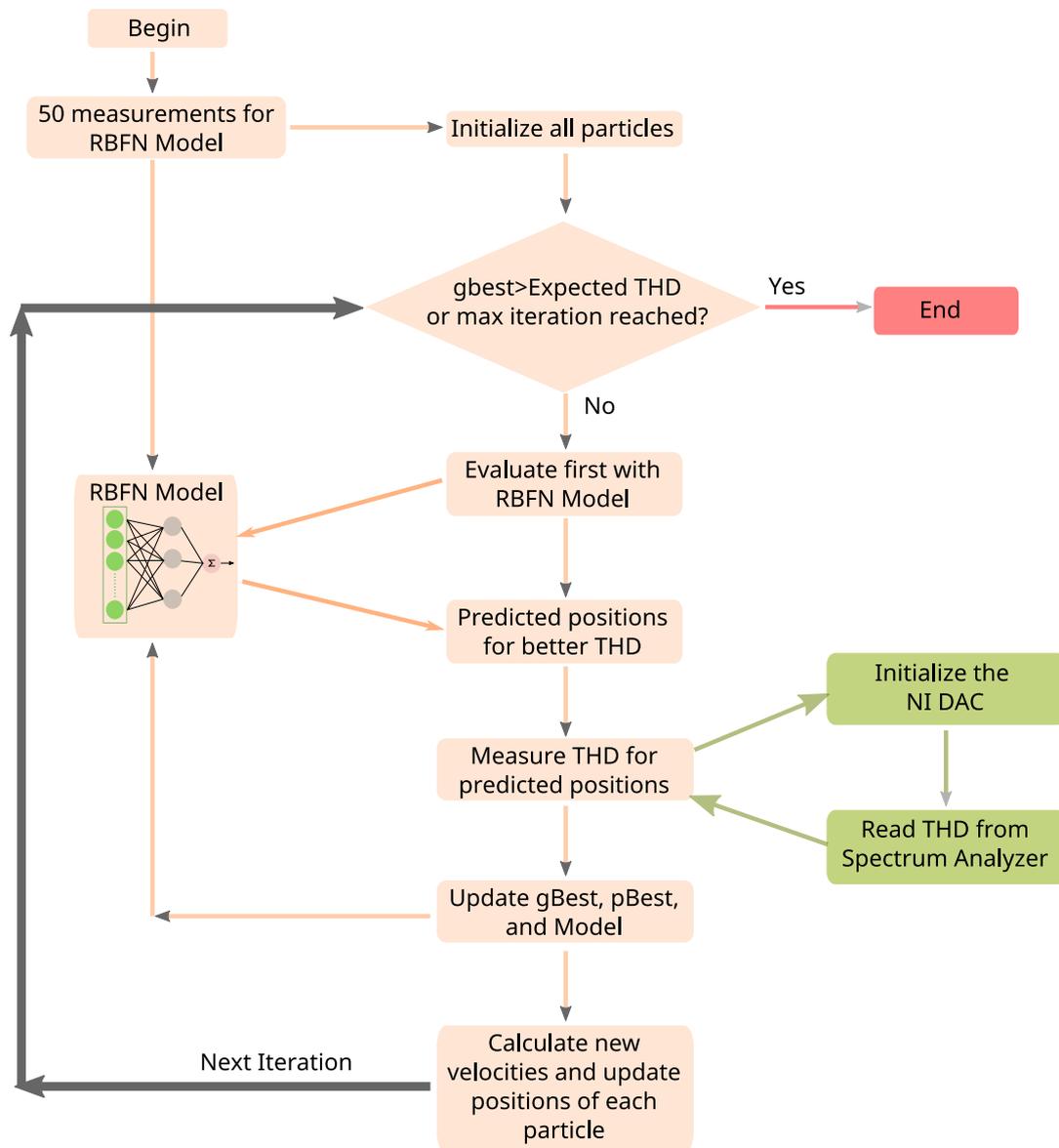


Figure 5.13: Flow chart of the Surrogate-Assisted PSO algorithm used in measurement

measurement, the optimizer first sends the position to NI-DAC, waits for some time to settle the transients, and then requests the spectrum analyzer for the THD. From these measurements, the $pBest$ and $gBest$ are updated for each position along with the RBFN model. Based on $gBest$ and $pBest$, new velocities of each particle are calculated and the positions are then updated. Following this a new set of measurements is done and this process keeps on going until the best THD is obtained or the maximum number of

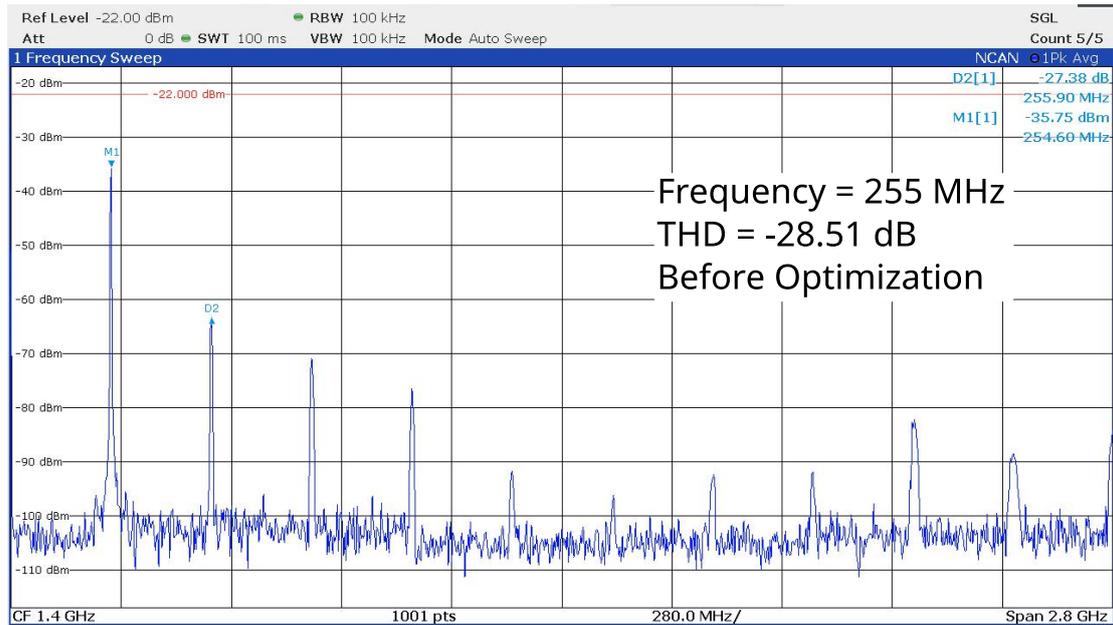


Figure 5.14: Spectrum of the measured signal before optimization (255 MHz)

iterations is reached.

5.6 Measurement results

The measurements are done for a range of frequencies. The minimum and maximum output signal frequencies that the signal generator can generate are 255 MHz and 1.95 GHz. The frequency spectrum of the signal at 255 MHz before and after optimization is shown in Fig. 5.14 and Fig. 5.15. The *THD* of the signal before optimization was equal to -28.51 dB which got improved to -41.53 dB after optimization. The frequency spectrum of the signal at 1.95 GHz before and after optimization is shown in Fig. 5.16 and Fig. 5.17 respectively. The *THD* of the signal was approximately equal to -38.34 dB before optimization which improved to -58.28 dB. Figures 5.18, 5.19, 5.20, 5.21, 5.22, 5.23, and 5.24 depict snapshots from the spectrum analyzer. These snapshots illustrate the *THD* measurements of the output signal at respective frequencies of 255 MHz, 524 MHz, 1 GHz, 1.27 GHz, 1.46 GHz, 1.63 GHz, and 1.95 GHz, both before and after the optimization. Each figure comprises 10 columns, where each column corresponds to the power of a harmonic. The first column indicates the power of the fundamental frequency, and the subsequent columns represent the power of the harmonics, extending up to the 10th harmonic.

5.6 Measurement results

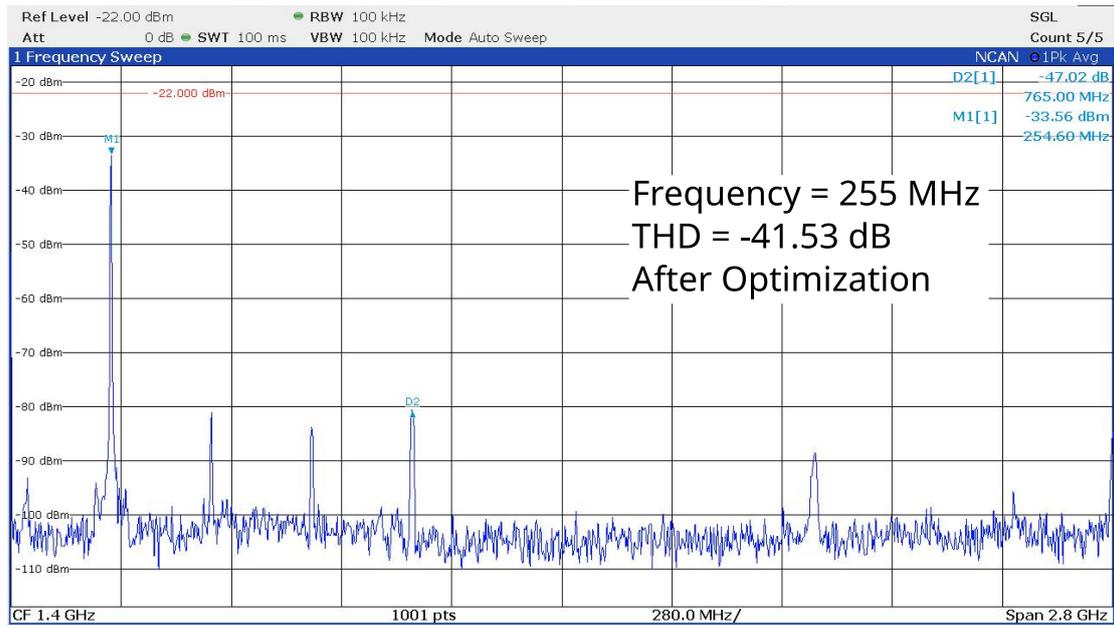


Figure 5.15: Spectrum of the measured signal after optimization (255 MHz)

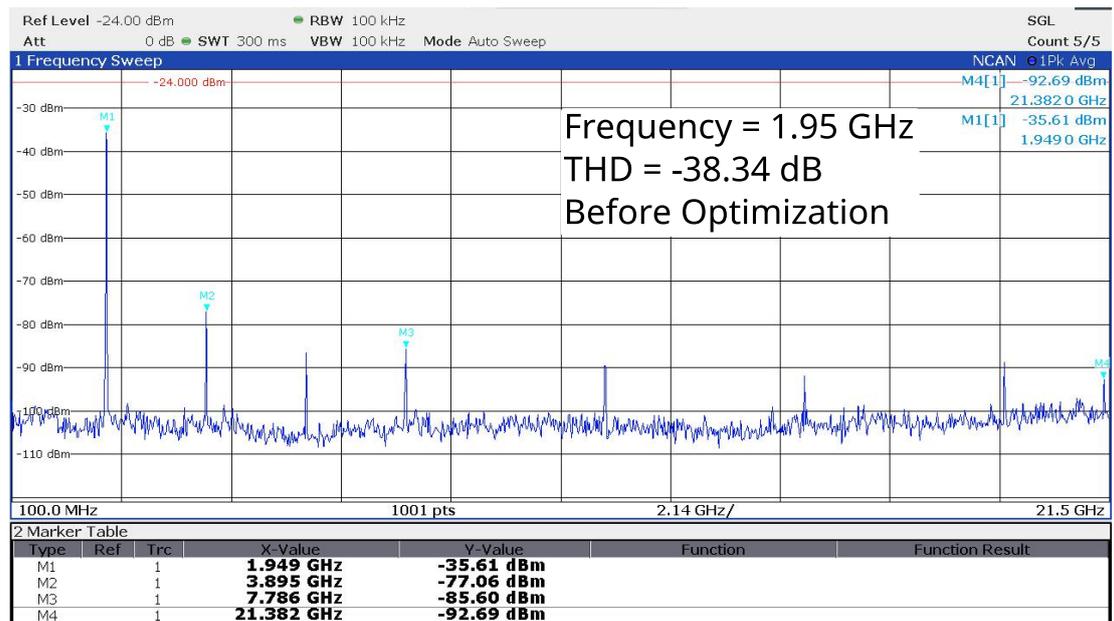


Figure 5.16: Spectrum of the measured signal before optimization (1.95 GHz)

Fig. 5.25 illustrates the *THD* and *SFDR* before and after optimization of the output signals for all frequencies ranging from 255 MHz to 1.95 GHz. The X-axis represents

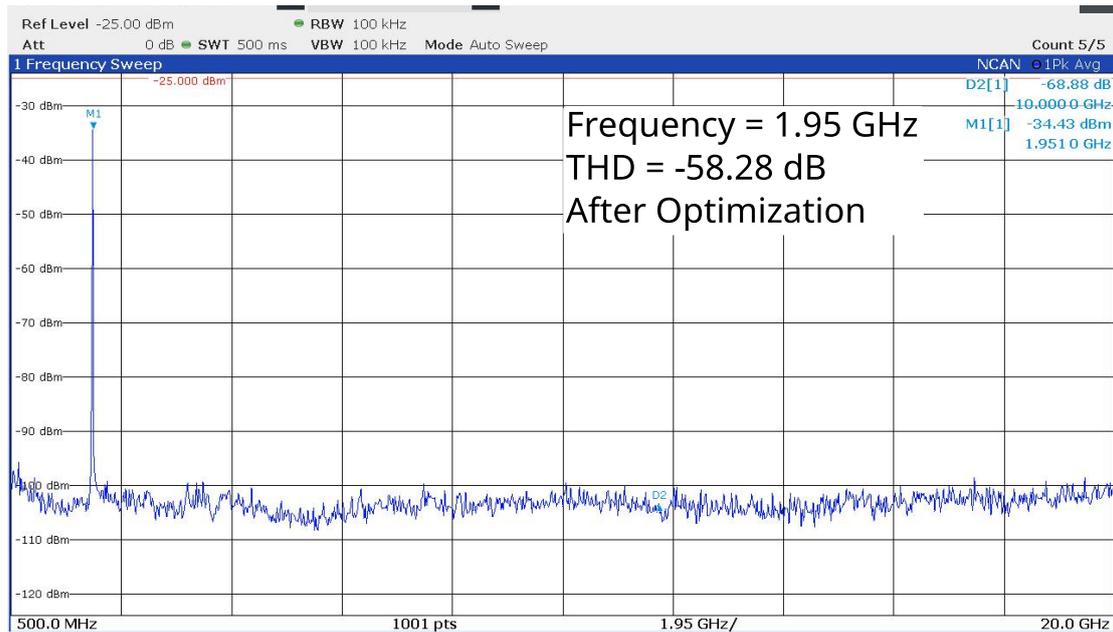
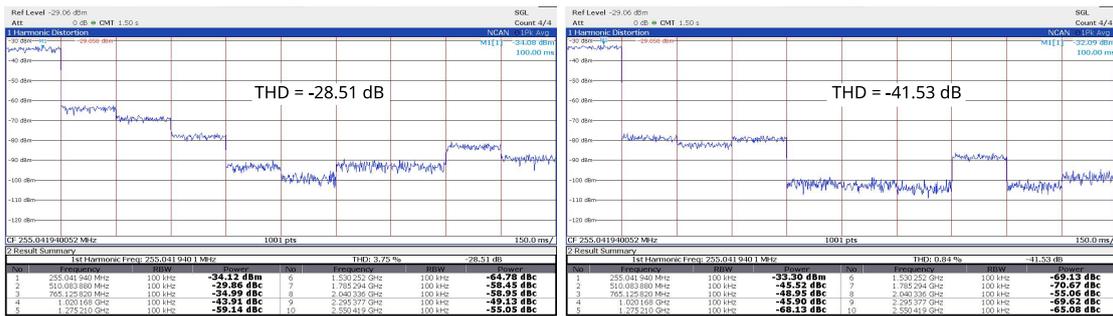


Figure 5.17: Spectrum of the measured signal after optimization (1.95 GHz)



(a) THD measurement of signal at 255MHz (Before Optimization) (b) THD measurement of signal at 255MHz (After Optimization)

Figure 5.18: Measured THD of signal at 255 MHz

the frequency range, the Y-axis in blue color represents the THD, and in red color represents the *SFDR* of the output signal. These frequencies are obtained by changing the supply voltage of the VCO (VDDA). The signal generator is designed to address the challenges that are faced when operating at higher frequencies (> 1 GHz). The cutoff frequency of LPF is around 1 GHz and is fixed. The cutoff frequency of the LPF has to be well below the operating frequency in such a way that it can be operated as an integrator. It can be observed that the optimized THD in frequencies less than 1 GHz is not as good as in the case of higher frequencies because of a fixed LPF. Even, the THD before optimization at 255 MHz is -28.5 dB, which is poor when compared to

5.6 Measurement results

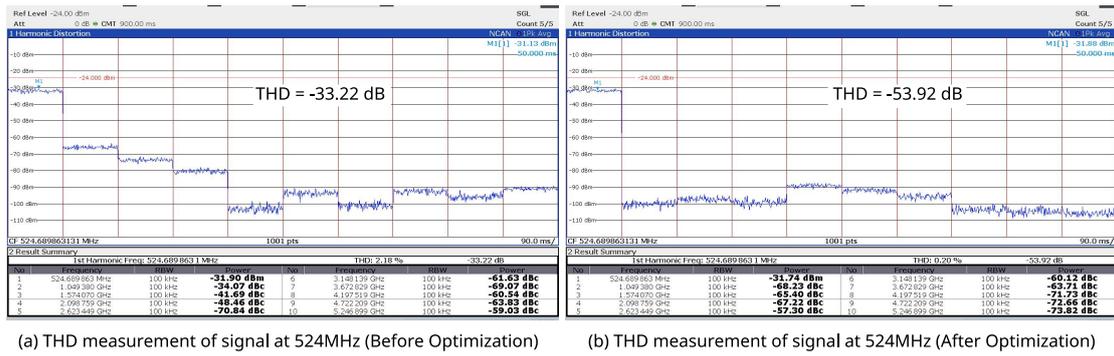


Figure 5.19: Measured *THD* of signal at 524 MHz

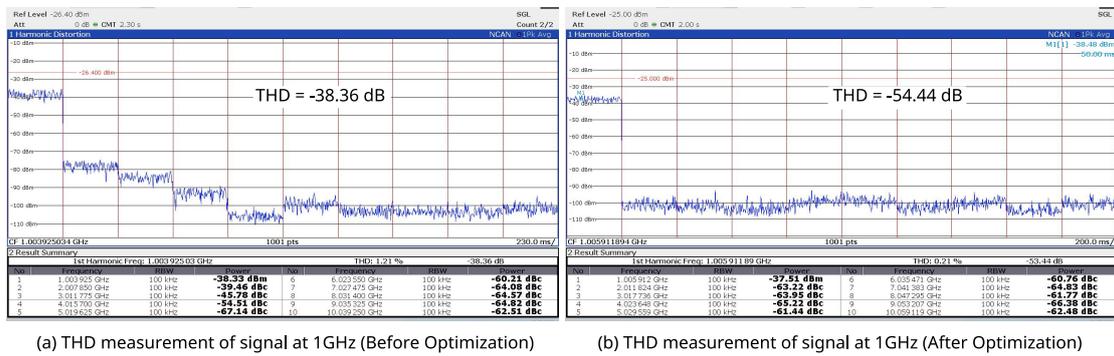


Figure 5.20: Measured *THD* of signal at 1 GHz

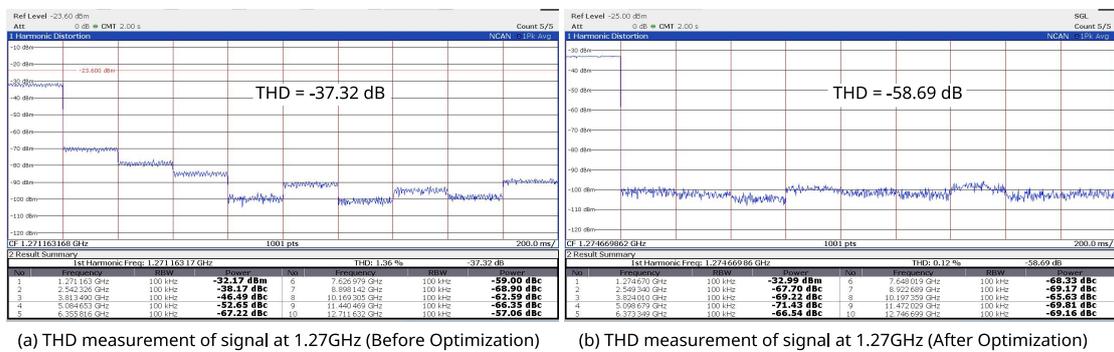


Figure 5.21: Measured *THD* of signal at 1.27 GHz

the samples at higher frequencies before optimization. However, the optimization algorithm works well in all the frequencies. The average *THD* gain after optimization for all frequencies is around 18.41 dB which shows the robustness of the signal generator. The variable LPF can be redesigned in future design with the help of the digital circuit so that it acts as an integrator in all frequencies. Moreover, the *SFDR* plot also shows

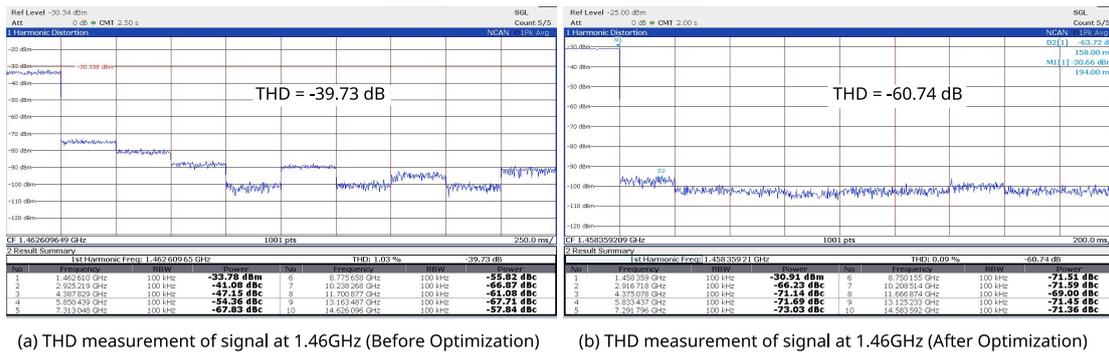


Figure 5.22: Measured THD of signal at 1.46 GHz

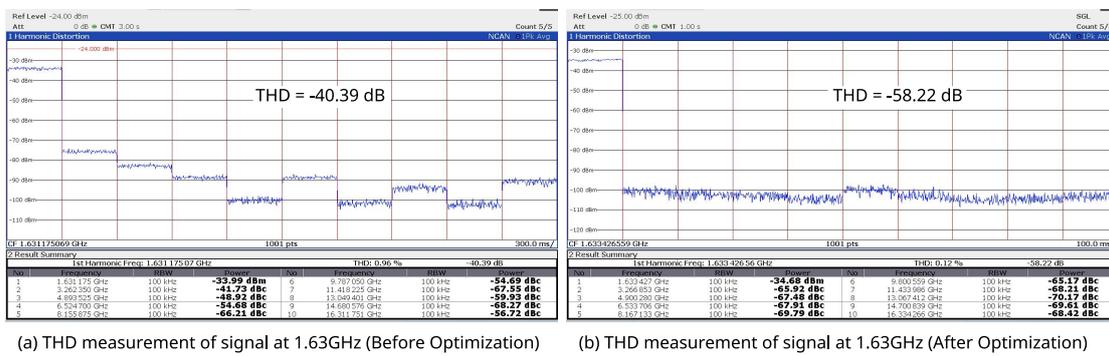


Figure 5.23: Measured THD of signal at 1.63 GHz

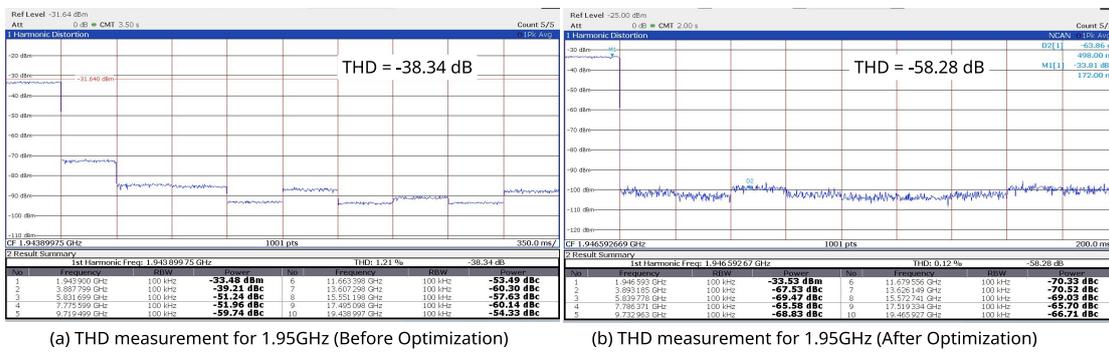


Figure 5.24: Measured THD of signal at 1.95 GHz

a significant improvement after optimization for frequencies at or above 1 GHz, achieving values greater than 60 dBc. Fig. 5.26 illustrates the THD as a function of frequency for both measured and simulated data. The red circles represent the measurement data, while the blue squares depict the schematic simulation results. Each data point is annotated with its corresponding frequency and THD value to provide a clear understanding

5.6 Measurement results

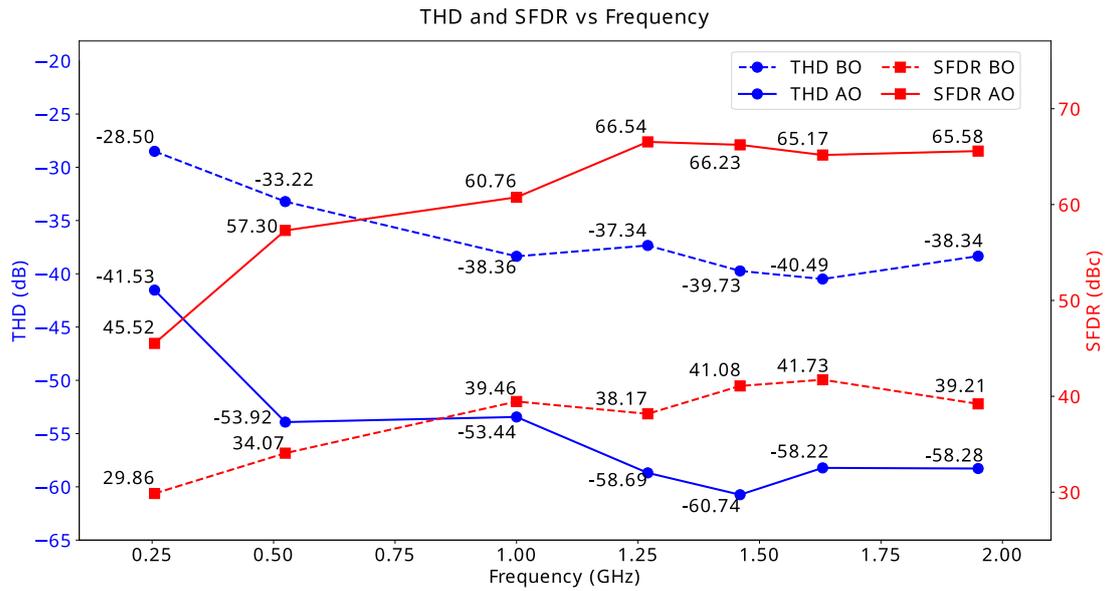


Figure 5.25: *THD* and *SFDR* vs frequency before and after optimization

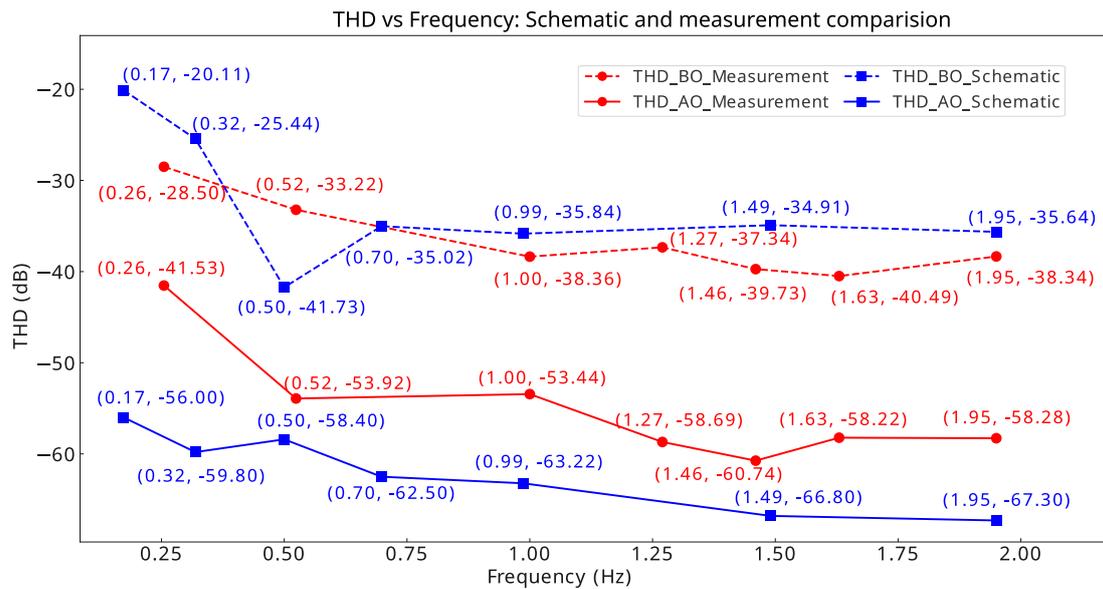


Figure 5.26: Comparison between schematic and measurement results of output *THD* vs frequency before and after optimization

of the relationship. The measurement data follows a similar trend when compared to the simulation results discussed in Fig. 4.24. In lower frequencies the *THD* of output

No.	Frequency (GHz)	VDDA (V)	Ivdda (mA)	VDD (V)	Ivdd (mA)	Dec_Fb	Total Power (mW)	THD (dB)		SFDR (dBc)	
								BO	AO	BO	AO
1	0.255	0.56	0.15	0.75	0.9	1	0.759	-28.5	-41.53	29.86	45.52
2	0.524	0.65	0.35	1	1.7	1	1.928	-33.22	-53.92	34.07	57.30
3	1	0.8	0.85	1	2.3	1	2.980	-38.36	-53.44	39.46	60.76
4	1.27	0.803	0.893	1	2.639	0	3.356	-37.34	-58.69	38.17	66.54
5	1.46	0.855	1.1	1	2.887	0	3.828	-39.73	-60.74	41.08	66.23
6	1.63	0.903	1.316	1	3.1	0	4.288	-40.49	-58.22	41.73	65.17
7	1.95	1	1.78	1	3.8	0	5.580	-38.34	-58.28	39.21	65.58

BO= Before Optimization
 AO= After Optimization

Figure 5.27: Measurement results

signal is limited by the non-programmable LPF. The absence of an analog buffer also degrades the power of the output signal, resulting in lower THD values compared to the simulation results. Integrating a programmable LPF and an analog buffer can ensure a better THD across the wide range of frequencies.

All measurement data are tabulated in Table 5.27. As discussed earlier, VDDA and I_{VDDA} are supply voltage and the current consumption of the oscillator. VDD and I_{VDD} are the supply voltage and current consumption of all digital circuits. Dec_Fb is a digital signal, when it is high, the VCO operates in low-frequency mode and when it is low, the VCO operates in high-frequency mode. The total power consumption is 0.759 mW at 255 MHz which increases to 5.58 mW at 1.95 GHz.

Table 5.2 presents a comparison of the proposed sinusoidal signal generator’s performance against other state-of-the-art designs. This table offers a side-by-side look at various key metrics, including the range of output frequencies, power consumption, process technology, supply voltage, and the quality of output sinusoidal signals such as SFDR and THD, across different architectures. To facilitate a fair and comprehensive comparison of these different systems, we employ two distinct figures of merit. The first figure of merit (FOM1), as introduced in [32], is described by equation 5.2.

$$FOM1 = \frac{f_o(\text{MHz}) \cdot 2^{\frac{SFDR_{best}(\text{dBc})}{6}}}{P_{total}(\text{mW}) \cdot A(\text{mm}^2)} \quad (5.2)$$

5.6 Measurement results

f_o is the frequency of the output sinusoidal signal in MHz, $SFDR_{best}$ represents the best $SFDR$ value achieved at the particular frequency, P_{total} is the total power consumption at that frequency, and A is the area of the signal generator.

The second FOM which is more generalized is given by the equation 5.3:

$$FOM2 = \frac{f_o(\text{MHz}) \cdot SFDR_{best}}{P_{total}(\text{mW}) \cdot A(\text{mm}^2)} \quad (5.3)$$

Upon reviewing the table, it becomes evident that the proposed sinusoidal signal generator exhibits outstanding performance in comparison to its counterparts, highlighting the robustness and efficiency of our design. The generator consumes extremely little power, uses supply voltage less than equal to 1 V, can generate sinusoidal signals for a wide range of frequencies, and has a smaller area when compared with the state-of-the-art.

Table 5.2: Comparison of sinusoidal signal generator performance

Ref.	Year	Fout (MHz)	Power (mW)	Area (10^{-3}mm^2)	Process (nm)	Supply (V)	SFDR/-THD* ((dBc/dB))	Circuit Type	FOM1	FOM2
This work	2023	255	0.759	11.3	28 FD-SOI	0.56	45.52/41.53*	HC	5715.24	1353.39
		1950	5.58			1	65.58/58.28*		60336.46	2028.12
[43]	2022	0.8	6.8	505	180	1.8	66.4/NA	HC-SCM	0.50	0.02
		100	8.7				38.4/NA		1.92	0.87
[47]	2019	1	NA	11.2	28 FD-SOI	1	50/45*	HC	NA	NA
		166.67					52/46*			
[88]	2016	2000	NA	167.5	SiGe	2.5	52.3/NA 3rd Harmonic	HC	NA	NA
		15000								
[32]	2015	150	9.1	80	180	1	60.3/54.9*	HC	218.43	12.42
		750	57			1.8	70.0/62.6*		534.70	11.51
[63]	2014	DC	130	100	55	1 - Digital 2.5 - Analog	55/NA	DDFS	44.21	4.23
[62]	2011	DC	460	2100	350 (SiGe)	3.3	45.7/NA	DDFS	0.51	0.12
[61]	2010	1300	350	2000	90	NA	52/NA	DDFS	0.75	0.10

Conclusion and future work

This Ph.D. thesis is carried out in the framework of the NANO2022 program in collaboration with STMicroelectronics Crolles. The main goal of this thesis is to develop an on-chip sinusoidal signal generator, capable of generating spectrally pure sinusoidal signals of frequencies in the GHz range. We looked into different types of architectures that are used to generate the sinusoidal signal. We discussed their advantages and disadvantages, and based on this we understood that generators based on the harmonic cancellation technique offer an efficient and flexible alternative for achieving clean and precise sinusoidal signals without the limitations associated with some other generator types. In this chapter, we summarize the main contributions of this thesis and outline the future research perspectives related to this work.

6.1 Thesis contribution

1. We developed a quantitative understanding using mathematical derivations and a qualitative understanding using behavioral simulations to understand the implications of mismatches (SPE , DCV , and MV) on the signal generator. We figured out that when the frequency of the output signal is increased, the quality of the output signal (THD or the linearity of the output signal) degrades when the absolute values of SPE and DCV at a particular frequency are constant.
2. We proposed three calibration-based architectures that effectively mitigate the

impact of timing inaccuracies (*SPE* and *DCV*) on signal generators based on the HC principle. Transistor-level simulation results show that each architecture can produce a sinusoidal signal of frequencies > 1 GHz. The first two architectures are based on an optimization algorithm that is done post-fabrication. The third architecture uses multiple feedback to correct the timing inaccuracies.

3. One of the proposed solutions based on a coarse-fine delay cell that can mitigate the timing inaccuracies of a square wave signal was fabricated using ST 28-nm FDSOI technology and validated. Measurements are done for frequencies ranging from 250 MHz to 2 GHz. A surrogate-assisted particle swarm optimization algorithm is used for optimizing the signal generator's tuning voltages. After optimization, the measurement results show an SFDR greater than 60 dBc for frequencies greater than 1 GHz. The proposed signal generator outperforms in comparison to other architectures. This shows the potential of the proposed sinusoidal signal generator in enhancing the reliability and effectiveness of on-chip sinusoidal signal generation for AMS-RF BIST applications.

6.2 Future work

1. In the future, this signal generator should be integrated with an analog buffer designed to operate over a wide frequency range. Designing a buffer for such a low supply voltage and a wide range of frequencies will be an interesting problem.
2. This generator can also be integrated into a complete BIST prototype for testing a state-of-the-art ADC or an RF system to validate the proposed generator.
3. In the future, a signal generator based on an on-chip calibration discussed previously with transistor-level simulation results can also be fabricated and validated.
4. These generators can also be explored for applications in silicon-based Quantum computers, where the Q-bits are read with the help of sinewave-based pulses.

List of publications

- A. Mamgain, M. J. Barragan and S. Mir, "Analysis and mitigation of timing inaccuracies in high-frequency on-chip sinusoidal signal generators based on harmonic cancellation," 2021 IEEE European Test Symposium (ETS), Bruges, Belgium, 2021, pp. 1-6, doi: 10.1109/ETS50041.2021.9465424.
- A. Mamgain, S. Mir, J. N. Tripathi and M. J. Barragan, "On-chip calibration for high-speed harmonic cancellation-based sinusoidal signal generators," 2022 IEEE 31st Asian Test Symposium (ATS), Taichung City, Taiwan, 2022, pp. 43-48, doi: 10.1109/ATS56056.2022.00020.
- A. Mamgain, S. Mir, J. N. Tripathi and M. J. Barragan, "Special Session: A high-frequency sinusoidal signal generation using harmonic cancellation," 2023 IEEE 24th Latin American Test Symposium (LATS), Veracruz, Mexico, 2023, pp. 1-2, doi: 10.1109/LATS58125.2023.10154502.
- A. Mamgain, S. Mir, J. N. Tripathi and M. J. Barragan, "A harmonic cancellation-based high-frequency on-chip sinusoidal signal generator with calibration using a coarse-fine delay cell," 2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, 2023, pp. 1-5, doi: 10.1109/ISCAS46773.2023.10181742.
- A. Mamgain, M. Madhvaraj, S. Mir, M. J. Barragan and J. N. Tripathi, "A sub-picosecond resolution jitter instrument for GHz frequencies based on a sub-sampling TDA," 2023 21st IEEE Interregional NEWCAS Conference (NEWCAS), Edinburgh, United Kingdom, 2023, pp. 1-5, doi: 10.1109/NEWCAS57931.2023.10198132.

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