Design methodology based on the inversion coefficient for RF and mmW circuits optimization using 28 nm FD-SOI CMOS technology

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Méthode de conception basée sur le coefficient d'inversion pour l'optimisation énergétiques des circuits RF et millimétrique, en technologie 28 nm FD-SOI CMOS

Design methodology based on the inversion coefficient for RF and mmW circuits optimization using 28 nm FD-SOI CMOS technology

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Abstract - EN

In response to the flourishing market demands for the new generation of IoT devices, this work addresses the design and optimization of Low Noise Amplifiers (LNAs). The LNA serves as the main building block of low-power LNA-first sub-6 GHz receivers dedicated to 5G Long-Term Evolution for machines (LTE-M) and Narrowband IoT (NB-IoT) cellular standards. Recognizing the escalating challenges in ultra-low power IoT device connectivity, the significance of optimizing LNAs lies in enhancing overall receiver performance and meeting the strict low noise and reduced power budget requirements of LTE-M and NB-IoT applications. Besides, it requires the utilization of cost-efficient, high-performing, and extensively integrated technology for Very Large Scale Integration. In this thesis, we employ the 28 nm *FD-SOI* CMOS technology provided by STMicroelectronics.

To improve power efficiency, the LNA is designed using a comprehensive analytical methodology. This methodology leverages the transistor inversion level as a key design parameter, providing insights into the design space. Employing a proposed simple 6-parameter advanced compact model (ACM) introduced in this work, applicable across all transistor regions and operation regimes, the methods enable preliminary LNA sizing through analytical equations. This simple model, an adaptation of previous ACM versions accommodating various physical parameters, is made suitable for both bulk and *FD-SOI* technology, incorporating the fourth terminal.

The primary contribution lies in the design of a wideband, low-noise sub-6 GHz tunable multimode inductorless LNA, utilizing an active g_m-boosting Common-Gate (CG) architecture. Tunability is achieved through discrete coarse mode selection and continuous fine-tuning the back-gate of *FD-SOI* CMOS technology, showcasing the adaptability of body-bias for finely tunable architectures, specifically addressing the dynamic demands of IoT environments.

The transistor model, coupled with the analytical LNA description, guides the design algorithm, exploring various performance trade-offs against the specified requirements. Implemented in STMicroelectronics' 28 nm *FD-SOI* CMOS Technology with an active area of 0.0059 mm^2, the measured performance demonstrates over 30 dB voltage gain with a dynamic range exceeding 20 dB across modes for a frequency range of 400 MHz to 5 GHz. The noise figure (NF) varies from a stringent value of 1.8 dB to 7 dB, while the Input-referred third-order Intercept Point (IIP3) spans from -24.5 dBm to -6.5 dBm based on the selected mode. The maximum power consumption is 1.86 mW from a 0.9 V supply. Fine-tuning the LNA performances across modes achieves extensive coverage of the design space.

Furthermore, the proposed design methodologies are applied to different LNA architectures, including Resistive feedback common-source, common-gate, and g_m-boost common gate LNAs, showcasing the simplicity and applicability of the analytical approach in addressing diverse design scenarios. This paves the way to future energy-efficient implementations targetting ULP ULV IoT receiver front-end solutions.

Kyewords: Low-Noise-Amplifier (LNA), Internet-of-things (IoT), Low-power, Long-Term-Evolution for Machines (LTE-M), Narrowband IoT (NB IoT), 28 nm CMOS *FD-SOI*, transistor model, design-methodology, inversion coefficient, g_m/I_D, wideband.

Abstract - FR

En réponse à la demande croissante sur le marché des objets connectés (IoT), cette thèse explore la conception et l'optimisation d'amplificateurs à faible bruit (LNA) en tant que composants essentiels des récepteurs fonctionnant en dessous de 6 GHz et dédiés aux normes cellulaires Long-Term Evolution for Machines (LTE-M) et Narrowband IoT (NB-IoT). Face aux défis croissants de la connectivité des dispositifs IoT à ultra-basse consommation, l'importance de l'optimisation des LNAs réside dans l'amélioration des performances globales des récepteurs, en répondant aux exigences strictes en termes de faible bruit et de consommation énergétique réduite propres aux applications LTE-M et NB-IoT. De plus, cela nécessite l'utilisation d'une technologie de très grande échelle d'intégration, économique et performante. Dans cette thèse, nous utilisons la technologie 28 nm *FD-SOI* CMOS fournie par STMicroelectronics.

Afin d'accroître l'efficacité énergétique, le LNA est conçu en utilisant une méthode analytique complète. Cette approche exploite le niveau d'inversion du transistor comme paramètre de conception clé, offrant ainsi des perspectives sur l'espace de conception. Grâce à l'utilisation d'un modèle compact avancé (ACM) simple à 6 paramètres développé dans cette thèse, applicable à toutes les régions et tous les régimes de fonctionnement du transistor, cette méthode permet d'obtenir un dimensionnement préliminaire du LNA à travers des équations analytiques. Ce modèle simple, une adaptation de versions ACM antérieures prenant en compte divers paramètres physiques, convient à la fois à la technologie bulk (à substrat massif) et à la technologie *FD-SOI*, incluant la quatrième borne (grille arrière).

La contribution majeure de ce travail consiste en la conception d'un amplificateur à faible bruit (LNA) multimode sans inductance, accordable, basé sur une architecture de grille commune (CG) à renforcement actif du g_m (g_m-boost). L'accordabilité est obtenue par une sélection grossière discrète du mode suivie d'un réglage fin continu grâce à la grille arrière de la technologie *FD-SOI*. Il démontre la capacité offerte par la polarisation de la grille arrière à mettre en œuvre des architectures finement ajustables, répondant spécifiquement aux exigences dynamiques des environnements IoT.

Le modèle du transistor ainsi que la description analytique du LNA nous permettent d'implémenter un algorithme de conception afin d'explorer les différents compromis de performance face à un ensemble de spécifications. Implémenté dans la technologie *FD-SOI* 28 nm de STMicroelectronics avec une surface active de 0,0059 mm^2, les performances mesurées démontrent un gain en tension de plus de 30 dB avec une plage dynamique dépassant 20 dB entre les modes. Le facteur de bruit varie de 1,8 dB à 7 dB, tandis que le Point d'Interception du Troisième Ordre référé à l'entrée (IIP3) s'étend de -24,5 dBm à -6,5 dBm en fonction du mode sélectionné. La consommation électrique maximale est de 1,86 mW avec une alimentation de 0,9 V. Le réglage fin des performances du LNA entre les modes permet une couverture étendue de l'espace de conception.

De plus, les méthodologies de conception proposées sont appliquées à différentes architectures de LNA, notamment la source commune avec rétroaction résistive, la grille commune et le LNA à grille commune avec g_m-boost, mettant en évidence la polyvalence et l'applicabilité de l'approche analytique pour aborder divers scénarios de conception.

Mots clés: amplificateur à faible bruit, Internet des objets, basse consommation, Long-Term-Evolution for Machines (LTE-M), Narrowband IoT (NB IoT), 28 nm CMOS *FD-SOI*, modèle du transistor, méthode de conception, niveau d'inversion, g_m/I_D, large bande.

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Chapter 1

General Introduction

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1.1 Research context

The Internet of Things (IoT) stands out as a highly significant emerging technology today, having evolved into one of the most largest network of networks. Its applications are diverse, ranging from industrial uses to the development of smart cities. IoT combines smart production processes with the impressive advance in embedded systems to launch a new era of inter-connectivity and digitization. It aims to connect multiple devices to offer innovative smart services. Hence, a tremendous number of things, objects and sensors are connected to improve our lifestyle. The exponential growth of IoT applications, with new smart objects, home and robots opens the door for the 4th industrial revolution “Industry 4.0”(Pilati et al., 2024) combining real and virtual worlds. This drives a continuously demand on communication technologies and various wireless standards such as the different generations of cellular (2G/3G/4G/5G. . .), UWB, Bluetooth and WiFi. These wireless standards operate mostly in the sub-6 GHz frequency bands, as shown in Fig. 1.1.

The new generation of IoT devices, including applications like smart cities, connected greenhouses, and medical assistance, brings in significant changes and new challenges to classical technologies. These challenges primarily center on ensuring adequate coverage in areas that were previously inaccessible, extending the operational lifespan of devices’ batteries, and managing overall costs efficiently (Jörke et al., 2018). As these IoT applications become increasingly integral to daily life and industry, the need for ultra-low power, low-cost, reliable and efficient communication technologies becomes essential.

In response to these challenges, 5G cellular technologies have evolved, leading to the introduction of Long-Term Evolution for Machines (LTE-M) and Narrow-Band IoT (NB-IoT) with the third Generation Partnership Project (3GPP) releases 13 to 16. These cellular standards are specifically tailored to address the requirements of IoT applications, providing enhanced coverage, improved energy efficiency, and cost-effective connectivity solutions (3GPP, 2023).

Despite the evolution of multi-standard radiofrequency (RF) architectures optimized for these new cellular technologies, the design of ultra-low power sub-6 GHz wideband receivers remains a critical aspect. These receivers play a principal role in facilitating communication between IoT devices and networks. They must adhere to a complex set of requirements dictated by diverse standards, encompassing sensitivity, selectivity, and power budget considerations. One key component within the receiver chain that is particularly crucial in meeting these requirements is the Low Noise Amplifier (LNA). The LNA plays a significant role in amplifying weak signals received by the antenna while introducing minimal additional noise, while complying with significant linearity and blocker immunity requirements. Consequently, the performance of the LNA significantly influences the overall effectiveness and reliability of the communication link, making its design a crucial factor in addressing the challenges posed by the new generation of IoT devices.

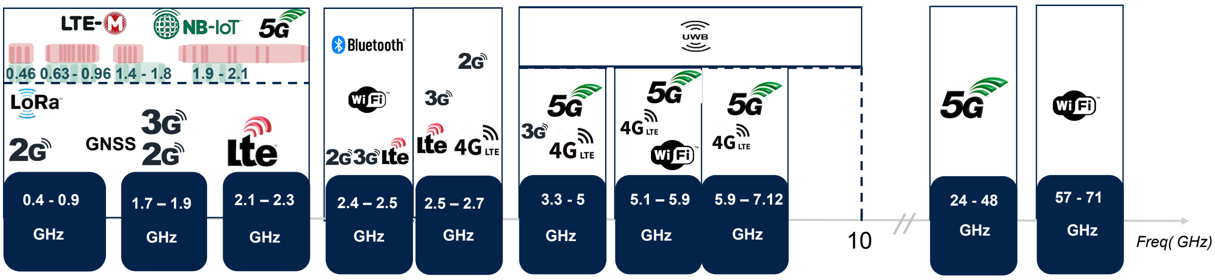

Figure 1.1: Illustration of main wireless standard frequency band distribution (3GPP, 2023).

1.2 Thesis objective

This thesis aims to design an energy-efficient, ultra-low-power, low-voltage, sub-6 GHz Low Noise Amplifier (LNA). The design methodology is centered on the g_m/I_D ratio and transistor inversion coefficient, striving for the optimal energy-efficient solution. This approach provides a systematic means to explore the design space, facilitating a nuanced understanding of trade-offs among various metrics and enabling the rapid identification of an optimal design point, always with the ultimate goal of maximizing energy efficiency.

The main objective of the LNA design is to achieve state-of-the-art performance and this applied to a specific use-case dedicated to the LTE-M and NB-IoT receivers. This requires meticulous consideration of requirements such as low noise, reduced power budget, wideband operation, high linearity, and resilience to blockers. To accomplish this, the study extensively reviews contemporary main architectures and design techniques, guiding the selection of an appropriate topology through a comprehensive analysis of the current state-of-the-art.

Subsequently, the design methodology demands a design-oriented simple transistor model equipped with a complete set of comprehensive DC and small-signal equations valid in all regions of operation. This guides the sizing of components with intuitive insights. The methodology advantage lies in achieving power efficiency throughout the design flow. The selected solution is implemented in the advanced 28 nm *FD-SOI* CMOS technology from ST-Microelectronics, leveraging the technology's advanced features to meet the specified performance requirements. Notably, the objectives of this thesis extend beyond the design phase to include the comprehensive realization of the LNA, together with the subsequent stages of measurements and characterizations. This approach ensures that the proposed LNA design is not only theoretically sound but also practically validated and positively compared to the state-of-the-art, aligning with the overarching objectives of this thesis efforts.

1.3 Main original contributions

The main contributions of this thesis work are listed below :

- **Sub-6 GHz wideband LNAs review:** The state-of-the-art of Sub-6 GHz wideband LNAs has been surveyed. In Section 2.3, common architectures, along with design enhancement solutions that are challenging to describe and compare through simple analytical considerations, have been examined. Design trends have been identified, and the performance graphical representations have helped condense the list of potential topologies for a given set of specifications.

- **Design-oriented transistor model:** A simple transistor model, based on the advanced compact model (ACM) formalism and set of equations, is proposed and detailed in Section 3.3. It relies on 5-DC physical parameters for bulk technologies and an additional parameter adapted for the *FD-SOI* specificity. It is a single-piece, all-region, all-regime model validated with respect to measurement results. It includes a small-signal set of equations very suitable for comprehensive design methods.

- **Comprehensive design-Methodologies for LNAs:** Three LNAs are designed, consisting of a wideband LNA following the complete design, fabrication, and characterization flow (Chapter 4), and two circuits at the schematic level (Section 3.4). The design method, based on an inversion-coefficient approach, enables navigation in the design space and exploration of various performance trade-offs. This method focuses on the non-linearity effects and performance dependencies, not only in the inversion region but also at saturation levels, thanks to the proposed model. A simple analytical model and a design-oriented transistor description enable accurate initial sizing for the LNA, ensuring compliance with a set of specifications.

- **Low power sub-2dB NF LNA design:** A multimode continuously tunable LNA, based on an active g_m-boosted Common-Gate (CG) topology, is implemented in STMicroelectronics' 28 nm *FD-SOI* CMOS Technology. It targets sub-6 GHz NB-IoT and LTE-M standards with a wideband implementation. The LNA performances are fine-tuned across the modes, achieving extensive coverage of the design space through the use of the body-bias feature. The dual performance-tuning strategy, comprising both coarse and fine steps, ensures a continuity which is necessary for channel-aware applications and continuous reconfiguration, preventing abrupt discrete mode-switching and is optimized in terms of power consumption. For the same implemented circuit, two biasing strategies are used to target sub-2 dB of NF and sub-mW ultra-low power design, respectively.

1.4 Thesis overview

This PhD manuscript is divided in five chapters as follows.

The second chapter contains an overview of the LNA main architectures and the state-of-the-art analysis. It allows to select the adequate topology for our targeted specifications.

The third chapter revisits the existing g_m/I_D and inversion coefficient based design methodologies for LNAs. It also presents a generic method based on a proposed transistor model compliant with advanced technologies such as the 28 nm CMOS *FD-SOI* used in this work. As a proof of concept, the analytical design methodology is applied on basic LNAs such as the resistive feedback common source and the common gate topologies.

The fourth chapter presents in detail the proposed wideband continuously tunable multimode sub-6 GHz LNA. The circuit description and explanation of architecture choices are provided. The design methodology steps are described based on our proposed model.

In addition, the layout and validation techniques for the implementation are detailed including the process corners verification to ensure the robustness. Silicon measurements of two versions of the fabricated LNA are analyzed and positively compared with the state-of-the-art.

Finally, the fifth chapter states the conclusions and proposes some perspectives for IoT sub-6 GHz solutions. This will set future works and improvements that can be considered for the system implementation,the LNA and the model.

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Chapter 2

LNA main architectures and state-of-the-art

Contents

2.1 Introduction

There are numerous options available for designing a wideband sub-6 GHz LNA, given the variety of topologies and design techniques proposed in recent years, as well as the development of advanced integrated technologies. The optimal design choice for a given set of specifications should leverage the raw performance of the technology and the design complexity of the topology.

Generally, there are two ways in which designers can evaluate a priori the potential performance of a given LNA architecture. First using analytical formulas describing the amplifier behavior or based on some Figures of Merits (FoM) to directly compare state-of-the-art designs already published and used. In order to select the most adapted architecture to the LNA specifications, the basic architectures and their theoretical operation principles are studied. Besides, the state-of-the-art of LNAs proposed in literature are reviewed to understand the design trends and evaluate the challenges. Based on the data in (Belostotski & Jagtap, 2020a) the performance of the wideband LNA topologies published in the last twenty years are directly compared. Towards this goal, more than 200 sub-6 GHz wideband LNAs are revisited from IEEE publications such as ISSCC, JSSC, TMTT, RFIC, MWCL, TCAS, ISCAS and NEWCAS. Some articles are added to the database, and the LNAs are sorted by the technology and the topology (Bouchoucha et al., 2021).

2.2 Theoretical Analysis

In literature (Razavi, 2011), the basic LNA architectures are identified based on the ways to realize the input matching for proper operation of the amplifier with respect to the 50 Ω filters termination and for maximum power gain. Besides, ensuring good trade-off between gain, noise figure for the sensitivity and linearity performance for the selectivity is determined by the choice of the architecture. Moreover, the targeted frequency band dictates some design choices. Hence, for wideband operation, four common LNA topologies are identified as represented in Fig. 2.1 namely common source with resistive feedback (CS RF), inductive degeneration CS, complementary CS RF and the common gate (CG). The theoretical descriptions of these topologies are briefly reported in this chapter followed by the analysis of the statistical data from published works and comparison with theoretical predictions.

2.2.1 Common source with resistive feedback LNA (CS RF)

A real input matching is provided by the feedback resistance and the gain of the resistive feedback topology shown in Fig. 2.1.a. The main characteristic metrics equations, for instance voltage gain, input impedance and noise factor, are detailed in (2.1), (2.2) and (2.3) respectively.

$$A_V \approx \frac{|g_{m1}R_F - 1|R_L}{R_L + R_F}. \tag{2.1}$$

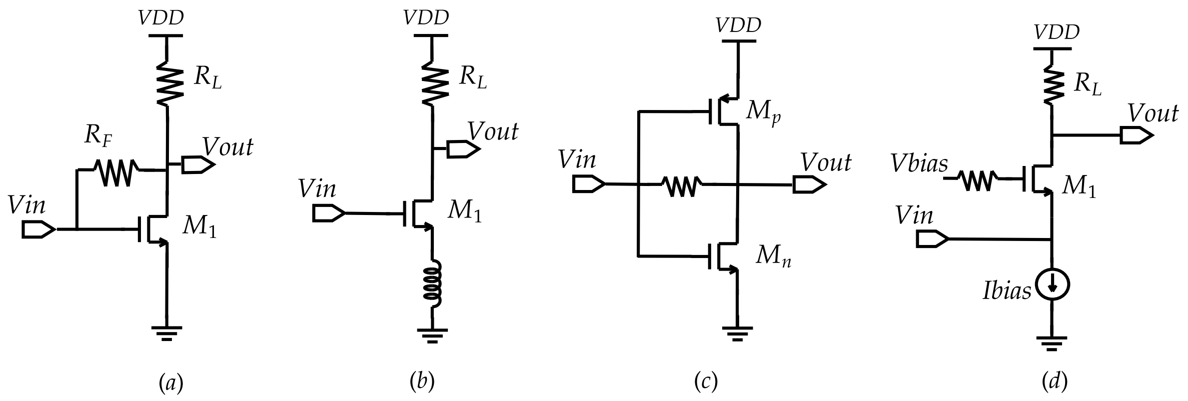


Figure 2.1: .a) Common source with resistive feedback, b) Common source with inductive source degeneration c) complementary common source with resistive feedback d) common gate.

$$R_{in} = \frac{R_L + R_F}{1 + g_{m1}R_L}. \tag{2.2}$$

$$F = 1 + \frac{(1 + g_{m1}R_S)^2 R_F}{R_S(1 - g_{m1}R_F)^2} + \frac{\gamma g_{m1}(R_S + R_F)^2}{R_S(1 - g_{m1}R_F)^2} + \frac{(R_S + R_F)^2}{R_S R_L(1 - g_{m1}R_F)^2}. \tag{2.3}$$

Where g_{m1}, γ and R_S are the transistor M_1 transconductance, the excess noise factor and the source resistance respectively. The matching condition in (2.4) is verified when $R_{in} = R_S$.

$$R_F = \frac{(g_{m1}R_L + 1)R_S - R_L}{2}. \tag{2.4}$$

While wideband operation could be ensured using this architecture, it suffers from reduced output impedance which affects the gain.

2.2.2 Common source with inductive degeneration LNA

From the circuit topology described in Fig. 2.1.b and by adding a series gate inductor L_g at the input node, the input impedance, the gain and the noise figure are expressed as functions of the main circuit parameters in (2.5), (2.7), (2.6) and (2.8).

$$Z_{in} = \frac{(L_S g_{m1})}{C_{gs1}} + j\frac{(w^2 C_{gs1}(L_g + L_S) - 1)}{C_{gs1}}. \tag{2.5}$$

With C_{gs1} being the transistor M_1 gate to source equivalent capacitance. The matching occurs at resonance where $Z_{in}(jw_0) = R_S$ with the resonance frequency expressed as,

$$f_0 = \frac{w_0}{2\pi} = \frac{1}{2\pi\sqrt{C_{gs}(L_S + L_g)}}. \tag{2.6}$$

The voltage gain A_v can be expressed as,

$$A_v = \frac{|(-g_{m1}R_L)|}{|(1 + jg_{m1}L_S w_0)|}. \tag{2.7}$$

Then the noise factor taking into account main contributors is expressed as,

$$F = 1 + \frac{(R_L + \gamma g_{m1}R_L^2)}{(R_S A_v^2)}. \tag{2.8}$$

2.2.3 Complementary Common source with Resistive Feedback LNA

The complementary common source LNA is based on the push-pull configuration of the NMOS and PMOS common source transistors. It benefits from the current reuse technique and the active load components. The main performance metrics are detailed in (2.9), (2.10) and (2.11).

The voltage gain and input impedance are expressed in terms of the parallel configuration of the small signal metrics of the NMOS and PMOS transistors as,

$$A_v = \frac{(Y_{C_{GD(n+p)}} - 1/R_F - g_{m(n+p)})}{(g_{ds(n+p)} + Y_{C_{GD(n+p)}} - 1/R_F)}, \tag{2.9}$$

$$Z_{in} = \frac{1}{\left(\frac{(1+g_{m(n+p)}/g_{ds(n+p)})}{(1/g_{ds(n+p)}+1/(Y_{C_{GD(n+p)}}-1/R_F))} + Y_{C_{GS(n+p)}}\right)}, \tag{2.10}$$

where $Y_{C_{XY}}$ is the equivalent admittance of the capacitance between the transistor nodes X and Y. The NMOS and PMOS parallel metrics are represented by the index (n+p) for simplicity.

The minimum achievable noise factor is expressed as,

$$F_{min} = 1 + \frac{(1 + R_{g(n+p)}A_v^2)}{(R_S A_v^2)}. \tag{2.11}$$

2.2.4 Common Gate LNA CG

The main advantage of common gate topologies is the wideband input matching through the $1/g_m$ real impedance at the source terminal. Hence, the input matching condition can be easily expressed as,

$$g_m = \frac{1}{R_S}. \tag{2.12}$$

This sets directly the value of the gain (2.13) and the noise factor (2.14).

$$A_v = g_m R_l. \tag{2.13}$$

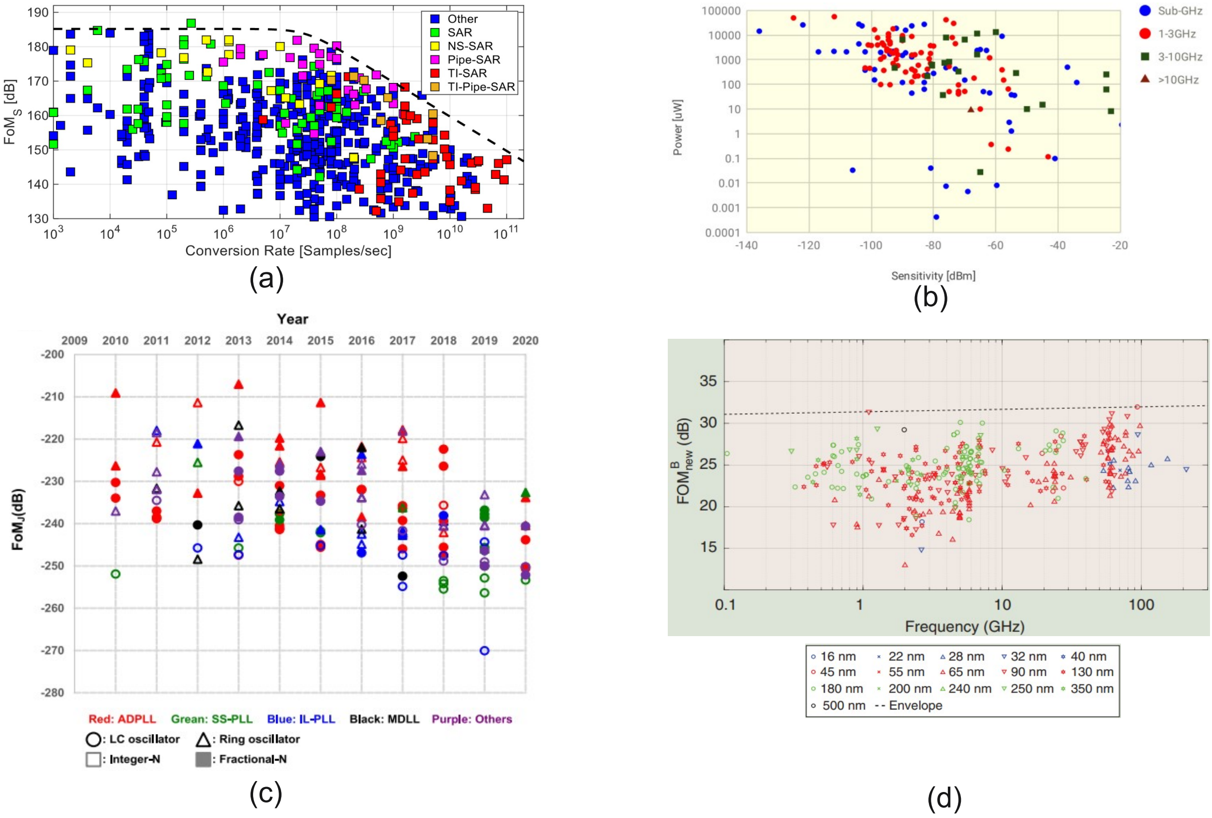
$$NF = 1 + \frac{\gamma}{R_s g_{m1}} + \frac{R_S}{R_L}(1 + \frac{1}{g_{m1} R_S})^2. \tag{2.14}$$

Under matching condition, (2.14) becomes,

$$F = 1 + \gamma + \frac{4R_S}{R_L}. \tag{2.15}$$

2.3 Statistical analysis

The analysis of the aforementioned equations describing the different architectures reveals an increase in the complexity of the equations as the circuit complexity and the number of devices increase. Additionally, an analytical comparison requires a certain number of calculations and the solving of these equations, taking into account various parameters. Consequently, the direct prediction of the ranges, limits, and main improvements of the LNA performance figures for these configurations, as well as building a comparison among them, becomes a challenging task. Furthermore, for the advanced architectures outside these common topologies, a complete analytical derivation for all the metrics is complex. It's worth noting that some performances could be technology-dependent, and the comparison in different technology nodes could also be challenging. To save time and gain insights into the performance of these circuits, a statistical analysis of state-of-the-art LNAs is conducted based on published figures. This approach proves valuable when deciding on the appropriate topology to meet a specific set of specifications. It serves as a powerful tool for benchmarking available solutions concerning target performance, which has been particularly useful for ADCs (Murmann, 1997-2023), receivers (Wentzloff et al., 2020), PLLs (Bae, 2022), and other crucial building blocks. The statistical analysis is always illustrated by a 2D distribution, depicting the trends of some topologies with respect to a Figure of Merit (FoM), as shown in Fig. 2.2.



(a) (b) (c) (d)

Figure 2.2: Examples of State-of-the-art surveys for a. ADCs (Murmann, 1997-2023), b. receivers (Wentzloff et al., 2020), c. PLLs (Bae, 2022) and d. LNAs (Belostotski & Jagtap, 2020b).

When it comes to LNAs, a FoM is proposed in (Belostotski & Jagtap, 2020a; Belostotski & Jagtap, 2020b) to compare the collected circuit performances as,

$$FoM_{(Belostotski\&Jagtap,2020a)} = \frac{(L_{(nm)}B_r^{0.32}(f_{0(GHz)}+17.4)^{2.3})}{(T_{cas(K)}P_{dc(mW)}^{0.31})} \tag{2.16}$$

Where B_r is the relative bandwidth to the center frequency f_0 and T_{cas} is cascaded noise temperature to express noise and gain. As shown in Figure 2.2.d, the LNAs are sorted by the technology node. However, wideband and narrowband solutions are presented together and RF and millimetric wave are compared for the same FoM without indicating the topology. Also, some empiric factors and offsets are introduced in (2.16) to improve the regression R^2 value and push towards a general trend from multiple nodes and topologies addressing different applications and frequency bands.

In this thesis, from (Bouchoucha et al., 2023), more than 200 sub-6 GHz wideband LNAs are collected and classified in terms of topologies with respect to the main performances to guide the design choice.

2.3.1 LNA Performance Technology Trends

First, to get a sense of the lay of the land, the collected wideband LNAs are classified according to the technological nodes to emphasize the appearance of trends for some performance parameters. Fig. 2.3 shows the distributions of the main parameters of the LNA, namely the gain, the power consumption, the input-referred third order intercept point (IIP_3) and the noise figure (NF) using a box plot format.

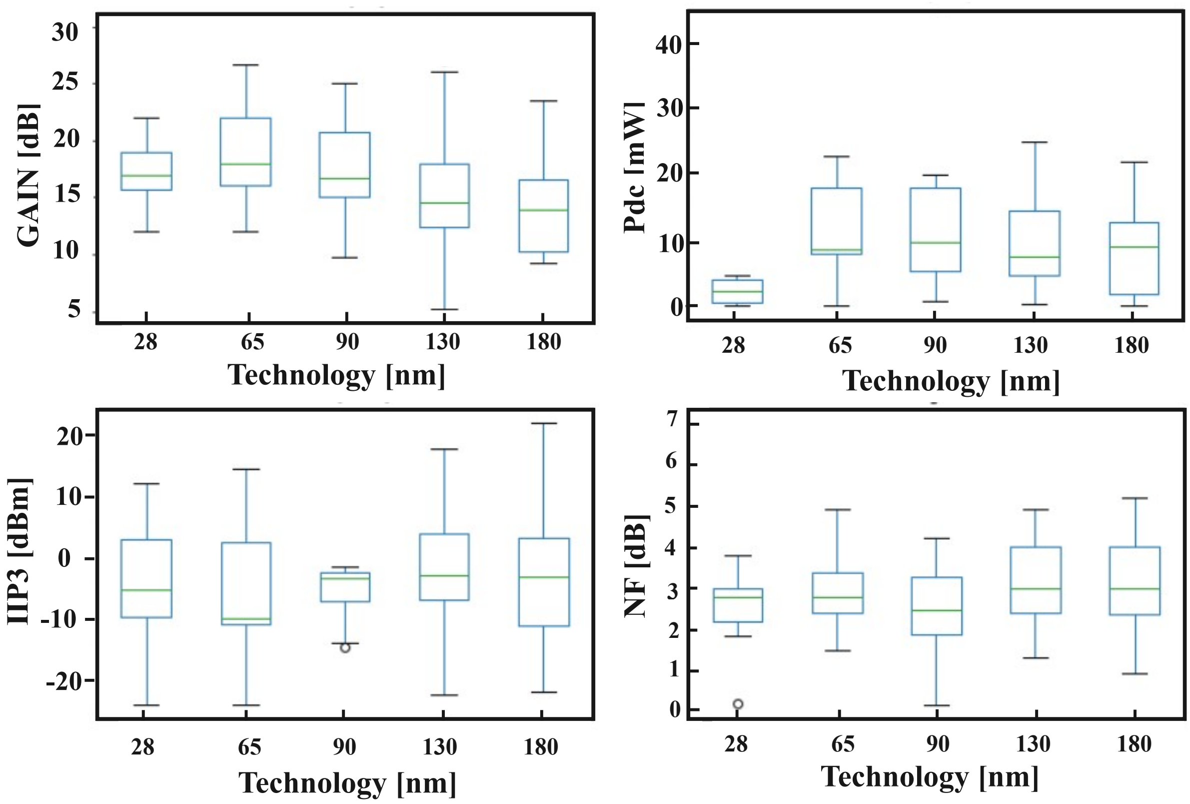


Figure 2.3: Box plots of the gain (dB), power consumption (mW), $IIP3$ (dBm) and noise figure (dB) grouped by technology (nm) from 56 papers in 180 nm, 43 papers in 130 nm, 23 papers in 90 nm, 31 papers in 65 nm and 13 papers in 28 nm.

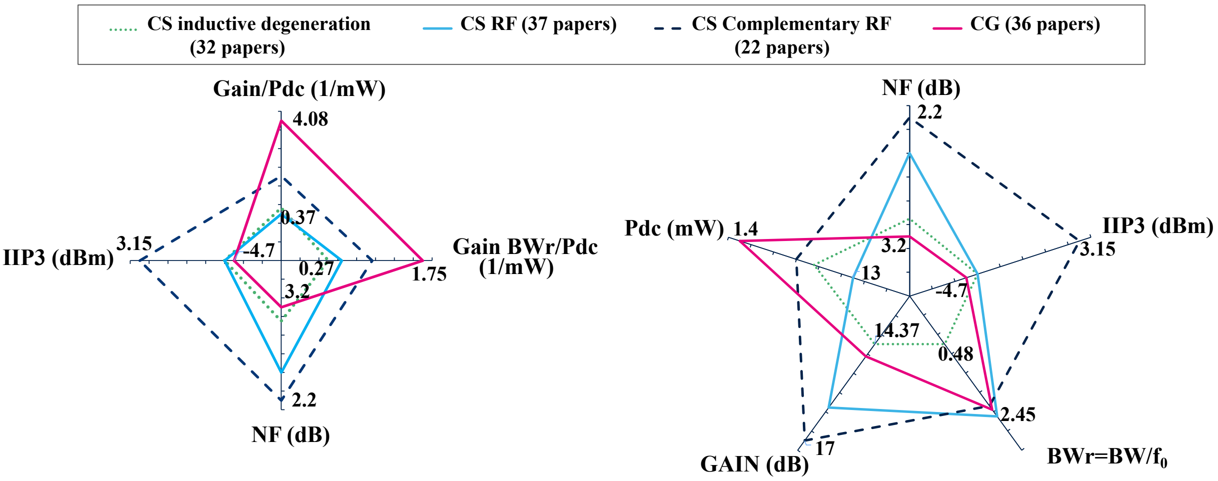
The technology, with the corresponding f_T and f_{max}, often sets the achievable bandwidth of the architecture (Yang et al., 2011). Also, with some design techniques, one can take advantage of advanced nodes to improve some performances, for instance the power consumption and the maximal achieved gain as shown in Fig. 2.3. Moreover, there is a breackthrough in power consumption for LNAs designed in 28 nm (including 22 nm technology nodes). This could be explained by the particularly good energy efficient performances of the *FD-SOI* CMOS technology which represents more than 60% of the 28 nm-based articles in our analysis. However, the relatively small number of publications in more recent nodes compared to older technologies could also push them aside from the trends. As previously reported in (Belostotski & Jagtap, 2020b), there are low correlations between NF, $IIP3$ and the technology. Actually, the NF relies on the sensitivity requirements from the standards as well as the design techniques employed. The selectivity of the receiver chain towards blockers sets its linearity accordingly and both mainly rely on the design technique and the architecture selection. In this regard we provide a statistical comparison of common wideband LNA topologies.

2.3.2 Comparison of Common LNA topologies

Instead of using FoM based comparisons for which particular performances are not captured, the trade-offs, strengths, and weaknesses of each particular topology, in terms of gain, bandwidth, power consumption, linearity and noise, are evaluated based on a statistical analysis of the database. This analysis allows to put the theoretical performance predictions into perspective and to allow designers to gain insight when choosing the optimal design style for a given set of specifications. Four common LNA topologies are identified as represented in Fig. 2.1. These topologies are compared among themselves based on the average value of each performance considering the number of associated papers in the database. In this way, for the same target application and frequency range, the above topologies are compared according to the achieved Gain, Noise figure (NF), Power consumption (Pdc), Input-referred third order Intercept Point (IIP_3) and the relative bandwidth (BWr) which is the bandwidth (BW) normalized to the center frequency (f_0) leading to $BWr = BW/f_0$. Furthermore, some metrics are regrouped to highlight the LNA efficiency such as the normalized gain defined by the ratio of the linear gain by the power consumption ($Gain/Pdc$), and the ratio of the gain, relative bandwidth product by the power consumption ($GainBWr/Pdc$).

Fig. 2.4.a compares the identified LNA topologies regarding their gain-power ratio, relative gain bandwidth product normalized by the power consumption, NF and IIP_3. Since the gain, the bandwidth and the power consumption are correlated and depend on specific design methodologies, investigating the ratios seems to be relevant for a fair comparison between different architectures. We illustrate the comparison using radar charts, with best performance situated on the top of each axis. This statistical analysis reveals that the complementary CS circuits yield the best trade-off in terms of energy efficiency, noise and linearity. It is expected that this topology presents the highest gain since this topology takes advantage of the current-reuse technique between both main transistors which finally leads to higher efficiency. Nevertheless, when comparing the topologies with respect to the gain-power ratio, Fig. 2.4.a demonstrates that the CG topology achieves the highest values. This is due to the reduced power consumption as

it will be highlighted in the next section. It is also clear that CG architectures privilege a different trade-off than CS ones, offering the best gain-power ratio and gain-bandwidth product normalized to the power consumption, at the expense of worse linearity and noise than their CS counterparts.



a) b)

Figure 2.4: a) Wideband LNA's topologies comparison from averaged results of previous published works, b) Performance comparison of the different LNA topologies from the collected data.

Certainly, the FoMs such as the two relative ratios introduced in Fig. 2.4.a state a clear comparison among the architectures. However, this does not reflect a complete comprehensive comparison concerning all its parameters. Considering separately each performance metric provides additional insight to compare the topologies even though the circuits are not designed under the same conditions and are implemented with different technologies. Fig. 2.4.b shows the comparison of the LNA's topologies according to the gain, power consumption, NF, $IIP3$ and BWr. This direct comparison reveals that CG LNAs achieve, in average, the lowest power consumption but not the highest gain which is difficult to highlight through the gain-power ratio since the variation ranges are different. This demonstrates that using only FoM can be useful to extract some trends but can also lead to incomplete conclusions. On the other hand, the complementary CS architecture, with its transistor pair, enhances inherently the equivalent transconductance of the LNA which allows better amplification as seen through the gain axis in Fig. 2.4.b. Besides, compared to a basic CS RF topology, through the current reuse technique, it achieves low power consumption occupying the second position behind the CG. The CG topologies are characterized by weak noise performances compared to other topologies. Actually, in this topology, the transconductance, which is a major contributor in the noise mechanism, can't be controlled separately from the matching condition. In most of the cases, as described in section 2.3.3, many techniques are associated to CG-based

LNA to improve the noise figure such as the g_m-boosting architectures. On the other hand, CS topologies, especially CS complementary structure exhibit a very good noise performances. We focused our survey on wideband LNAs. As shown in Fig. 2.4 most of the topologies achieve large bandwidths in average. It is shown that the CG, RF CS and complementary CS allow wideband operation, however, the inductive degenerated CS architectures, which are better suited for narrowband applications, succeed to achieve wideband LNA. Nevertheless, Fig. 2.4, shows their poor performances especially in terms of gain and bandwidth which is not expected with such topologies (Razavi, 2011). This can be explained in part by the fact that increasing the bandwidth requires a lower quality factor at the input stage, which has negative consequences on the gain and noise figure and consequently on power consumption. The $IIP3$ is conventionally used to express the linearity of LNAs. The nonlinearity of MOSFET drain current comes from the nonlinear transconductance g_m as well as the nonlinear drain conductance g_{ds} (Razavi, 2011). The complementary CS configuration has inherently good linearity performances (Nam et al., 2005). In fact, with properly matched transistors by setting equal g_m's, the CMOS pair output current could be second order distortion free. However, a general conclusion could not be driven out from the other topologies since many techniques are added to conventional architectures to boost the linearity performances. The trade-off between the linearity, gain and power consumption is analytically expected, although, not considered statistically. Considering all the performance metrics, the complementary CS topologies potentially present an appealing structure that satisfies the different trade-offs by achieving, in average and according to the set of analyzed papers, the lowest NF, highest gain, $IIP3$ all together with acceptable relative bandwidth and relatively low power consumption.

2.3.3 Design-enhanced solutions

For IoT applications, reduced power consumption is a major requirement to increase the battery lifetime of the solutions. The CG is attractive for its power and bandwidth characteristics; however, it suffers from inherent limitations in noise figure affecting the sensitivity of the receiver. Many efforts have been focusing on enhancing the CG topology to optimize the LNA performances ((Blaakmeer et al., 2008), (Bozorg & Staszewski, 2021), (Liu et al., 2021)). In the literature, two main techniques are introduced: the common gate-common source (CGCS) topology known as noise canceling (NC), and the transconductance boosting g_m-boost CG topology. The generic circuits of both architectures are shown in Fig. 2.5.

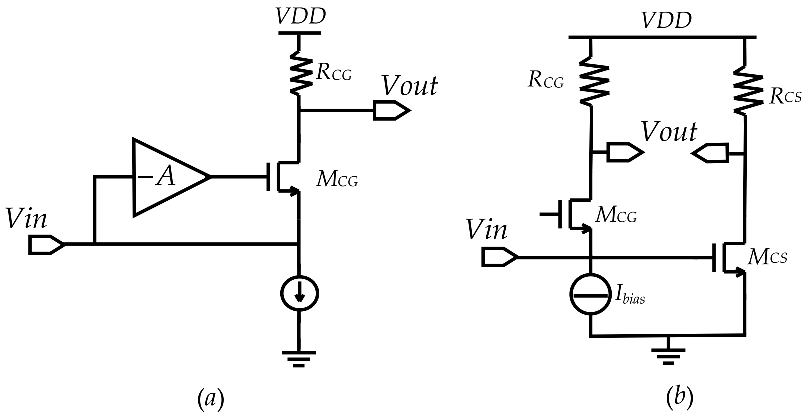


Figure 2.5: Generic circuits for a) g_m-boost CG LNA and b) CGCS LNA.

Working principle and examples

The CGCS principle consists in sensing the CG noise contribution and canceling it through an auxiliary out of phase forward path based on CS amplifier (Blaakmeer et al., 2008). As shown in 2.5.b, the CG as input stage is used for wideband input matching and a balancing condition is applied on the CS branch to allow the noise canceling and operate as active single to differential structure. Recently, further modifications of the CGCS cell are proposed (Bozorg & Staszewski, 2021), (Liu et al., 2021) to improve the LNA performance. The circuit in (Liao & Liu, 2007) belongs to one of the first CGCS NC techniques that were introduced to lower the NF of wideband common-gate amplifier. However, the achieved NF was still high (4.5 dB), even higher than that of LNAs without the use of noise cancelling. Recently, modified CGCS circuit (Bozorg & Staszewski, 2021) using advanced technology and design techniques to reduce the noise contribution of the auxiliary path, can achieve state-of-the-art NC noise figure comparable to the performance achieved by some complementary resistive feedback circuits with the current reuse technique.

The g_m-boost CG principle consists in introducing a gain of $(-A)$ in the RF path between the CG transistor source and gate terminals to improve the vgs swing and thus, improve the effective transconductance g_m of the device by a factor of $(1 + A)$. Hence, the choice g_m is decorrelated from the input matching condition allowing performance enhancement of the classic CG circuit. Many techniques are introduced in literature to improve the CG-based amplifier especially by boosting the transconductance of the main transistor in order to achieve good power to noise trade-off. For power consideration, passive methodologies were attractive (Cho et al., n.d.; Han et al., 2015; Sobhy et al., 2011; Zhuo et al., 2000) using the cross-coupled capacitor (CCC) pair for gain enhancement and ensure the matching (Cho et al., n.d.). Although restricted to fully differential topologies, this technique was widely used to serve as passive negative feedback and boost the transconductance of the CG transistor pair by a factor of 2. Besides, many improvements are added to this architecture employing multiple gain loops for different considerations and satisfy good trade-off between noise, power consumption and linearity. However, some of these proposals need external components, transformers and or inductors (Han et al., 2015; Zhuo et al., 2000) which is area consuming. Inductorless circuits, to compensate for the low transconductance boosting factor and to improve the linearity, use additional active feedback loops. In fact, dual negative feedback between the two CG branches boosts the gain but at the cost of high-power consumption due to the active part (J. Kim et al., 2010), a positive loop is added in (Woo et al., 2009) to bridge the link between gain, matching and linearity conditions while in (Sobhy et al., 2011) a triple feedback loops are needed to bring good trade off between the main performances. However, these improved solutions tend to be more complex compared to the basic simple common gate architecture, and the minimum achieved noise is limited to 2 dB. Recent works have been focusing on active g_m-boosted CG-based LNAs. In (Bozorg & Staszewski, 2021) a common source transistor inserted between the source and gate nodes of the CG main transistor performs active boosting by a factor $1 + g_{m_{aux}} R_{aux}$ where $g_{m_{aux}}$ is the transconductance of the auxiliary transistor and R_{aux} its load resistance. The proposed LNA uses noise canceling and current reuse techniques by adding second stage to lower the noise of the CG transistor and uses an inductor peaking to improve the bandwidth. A power of 4.5 mW is consumed to achieve 2.1 dB of noise figure. Nevertheless, these single-gain-mode solutions implemented using bulk technologies do not include tuned components in the architectures which makes them less suitable for multi-standard multi-band applications. In (Tamura et al., 2020) a multimode tunable LNA with a passive boosted complementary CG architecture is proposed to reduce the noise penalty. Three discrete gain modes are defined through variable load resistances. The gain varies from 43 dB to 3 dB with a 6 dB step using a switched C-2C capacitor attenuator in the feedback of the CG transistor. Besides, the transconductance boosting is performed using an on-chip transformer. The circuit operates in 3 gain modes while changing the steps of the gain and the configuration to maintain low power and good linearity. The LNTA consumes only 240 μW from 0.5 V despite the complexity of the architecture. In fact, additional circuitry is needed for the attenuator control with an additional supply voltage 1.8 V, also the load resistors and the configuration switching to CS for low gain mode need additional control signals.

Statistical Analysis of state-of-the-art

Despite the performance enhancement of classic CG topology, both techniques have a variety of proposed architectures and sometimes are difficult or complex to be described with analytical derivations. In such cases, the state-of-the-art can be helpful to work out some trends for a given configuration. In Fig. 2.6, CGCS and g_m-boost topologies are compared among themselves and with respect to CG based circuits considering the LNA main performances: NF, gain, $IIP3$, power consumption and bandwidth. As expected, both the CG enhanced topologies increase the gain of the basic CG with small power penalty for the g_m-boost technique. Although the CGCS topology is usually introduced as a noise cancelling architecture (Blaakmeer et al., 2008), it does not achieve the best noise performance among other CG LNA types. This is explained by the fact that the additional CS transistor in the noise cancelling structure, eliminates the noise contribution of the CG transistor but, in a practical implementation, it is difficult to reduce its contributions sufficiently to challenge the g_m-boost CG topologies especially passive based without extra-noise penalty. On the other hand, the noise cancelling architectures CGCS performs a good linearity enhancement of the CG circuit. In fact, the design conditions leading to the absorption of the thermal noise of the main CG transistor are valid for distortion reduction (Blaakmeer et al., 2008). However, the g_m-boost architectures $IIP3$ performances are affected by the large voltage swing of the CG transistor.

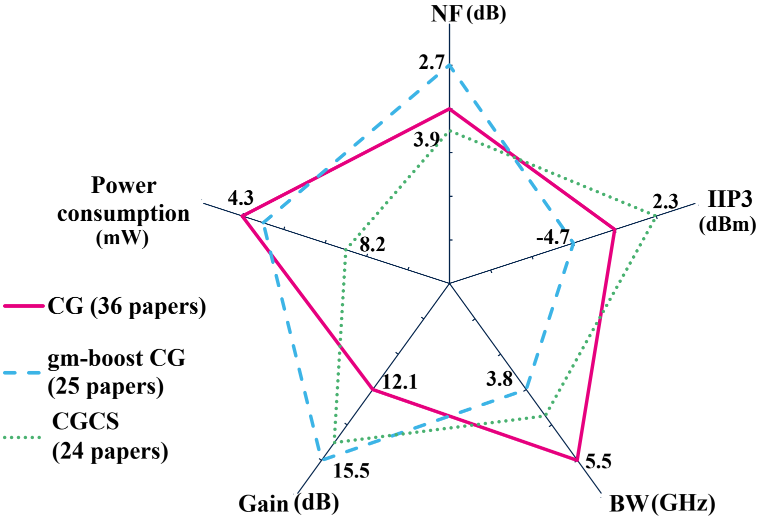


Figure 2.6: Performance comparison of the CG, CGCS and g_m-boost CG LNA topologies from the collected data.

2.3.4 Noise-Reduction Architectures

One of the main characteristics for receivers benchmarking is their sensitivities, that relies on the noise performances. Since the LNA is the dominant building block among the noise contributors in the receiver chain, reducing its NF has been an attractive topic for RF designers. In Fig. 2.7, a comparison of 60 state of the art ultra-wideband noise reduction LNAs in terms of power consumption and NF is shown. As it can be observed, most of the published works are based on the CGCS topology (> 35%), represented by green squares. However, these topologies are not dominating the extremely low noise solutions. As an example, sub−2dB NF, which is challenging for wideband, is achieved by different topologies such as the CS enhanced by transformers, the g_m-boost CG and other complex noise-oriented propositions using fancy circuits. This distribution as presented breaks with the general idea assuming that decreasing the noise figure has a big power consumption penalty. It is shown that, for a NF value, the power consumption depends on the topology, the used technique, and also intrinsic technology-related properties. Besides, it is shown another time that CG-based topologies are adequate for limited power budget requirements.

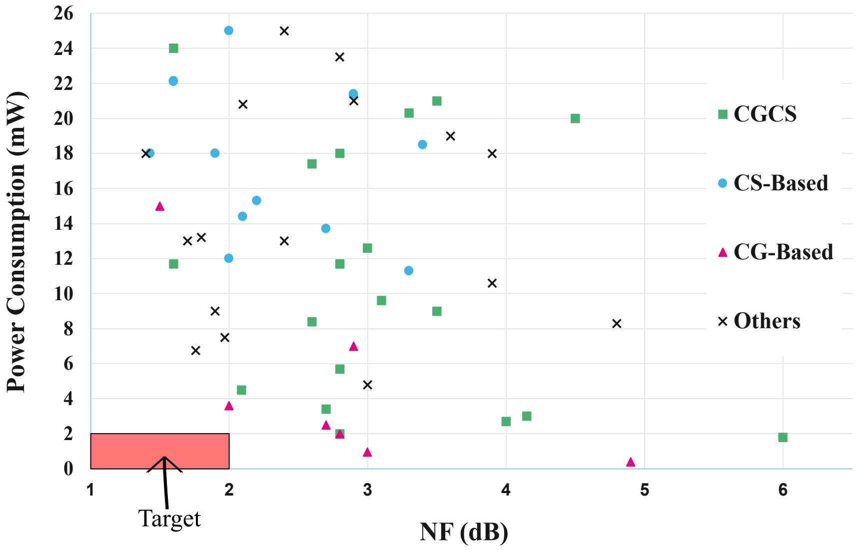


Figure 2.7: State of the art of Sub-6-GHz wideband noise-reduction LNAs sorted by power consumption-noise figure trade-off.

The relevant state-of-the-art published LNAs at the beginning of the PhD (Early 2021) are regrouped in Table 2.1. This comparison highlights numerically some design trade−offs in terms of linearity, noise and power consumption. As it is discussed in this chapter, many efforts are dedicated to decrease the noise of the amplifier. Sub−2 dB NF is achievable with extra power consumption for wideband amplifiers or larger area for the narrowband LNAs due to the need for inductors with good quality factor. In the context of IoT applications, reducing the area and the power consumption to the minimum are the main design claims. These devices exist massively in a huge multiple-node network, they should be compact with a long battery lifetime for better efficiency. The main objective is to select the right topology with the adequate design techniques and take advantage of the technology raw performances in order to satisfy a good trade off between the performances and address the application specifications correctly with a competitive solution.

Table 2.1: Comparison of different LNA topologies and technologies.

	Topology	**Tech. (nm)**	**BW (GHz)**	**NF (dB)**	**Power (mW)**	**VDD (V)**	**Gain (dB)**	**P1dB (dBm)**	***IIP*3 (dBm)**	**#Inductor**	**Area (mm²)**	**Fully intg.**	**S-E/ Diff.**
Specs		28 *FD-SOI*	0.4-2.2	<2	<2	1	>20	>-10	>-15	0	<0.01	Y	SE
(Belmas et al., 2011)	g_m-boost CG	130	0.1-2.7	4	1.32	1.2	20	-21	-12	0	0.007	Y	Fully Diff.
(Parvizi et al., 2016)	Compl CGCS	130	0.1-2.2	5.5	0.4	1	12.3	-20	-11.5	0	0.0052	Y	S-E
(Parvizi et al., 2015)	Compl. CS RF	90	0.1-7	6.5	0.75	0.5	12.6	-18	-8	2	0.23	Y	S-E
(Sobhy et al., 2011)	g_m-boost CG	90	0.1-1.77	1.85	2.8	2	23	-	-2.85	0	0.03	Y	F-D
(El-Nozahi et al., 2011)	Diff RF	90	0-2.3	1.4	18	1.8	21	-	-1.5	0	0.06	N	F-D
(Zaini et al., 2017)	g_m-boost CG	28 *FD-SOI*	0.4-6	6.3-7.3	0.9-0.3	1-0.6	21.5-16.8	-	-16	0	0.0015	Y	S-E
(Bozorg & Staszewski, 2021)	g_m-boost NC CG	28	0.02-4.5	2.09	4.5	1	15.2	-	-4.6	2	0.03	N	S-E
(S. Kim & Kwon, 2020)	g_m-boost CGCS	65	0.05-1.3	2.3	5.7	1	27.5	-	-4	1	0.046	N	S-D
(Yu et al., 2019)	R-feedback NC	65	0.5-7	2.87	11.3	1.2	16.8	-	-4.5	2	0.044	N	S-E
(Zhang et al., 2022)	g_m-boost CG	65	2.2-13.2	3.3	3.2	1	16.3	-16	-5.2	8	0.48	Y	F-D

Compl.: Complementary, Intg.: Integrated, S-E: Single-Ended, F-D: Differential, S-D: Single-to-differential, Y:Yes, N:No

2.4 Design specifications and PhD goals with respect to the state-of-the art

The objective of this study is to design a Low-Noise Amplifier (LNA) operating in the sub-6GHz frequency range, employing a design methodology based on the g_m/I_D relationship and the transistor inversion coefficient. This method not only facilitates navigation through the intricate design space but also brings to light various trade-offs existing in the multiple metrics, enabling a swift determination of the optimal design point. The LNA targets state-of-the-art performance as part of an LTE-M and NB-IoT receiver. The objective is to comply with the different requirements in terms of low noise, limited power budget, high linearity and resilience to blockers. The design space can be represented in Fig. 2.7 by the colored rectangle to show the challenge achieving such strict requirement. Hence, we refer to the state-of-the-art main architectures and design techniques in order to select the adequate topology. Then, thanks to the design methodology, the analytical description will lead the components sizing with good intuition in a complete comprehensive flow. Besides, the solution is implemented in the 28 nm *FD-SOI* CMOS technology from STMicroelectronics, and takes advantages from the advanced features of the technology to fulfill the specifications.

2.4.1 Design specifications

As part of a sub-6 GHz wideband receiver, the LNA has to operate over a wide frequency range to target multiple applications. For the particular case of LTE-M and NB-IoT standards, the minimal required bandwidth ranges from 440 MHz to 2.2 GHz to cover the communication downlink bands (stand-alone band, in-band and guard-band frequencies (3GPP, 2023)).

These applications impose strict challenges on the radiofrequency receivers (RX) to target good sensitivity at reduced power budget. From the RX point of view, as illustrated in Fig. 2.8, the sensitivity is expressed as,

$$\text{Sensitivity (dBm)} = 10\log_{10}\left(\frac{k \cdot T \cdot BW}{10^{-3}\,(\text{W})}\right) + \text{IL}_{(\text{dB})} + \text{NF}_{(\text{dB})} + \text{SNR}_{\text{BB}}. \tag{2.17}$$

The first term represents the thermal noise power (P_n) where, BW is the signal bandwidth (in Hz), I_L is the insertion between the antenna input and the RF receiver input. NF is the noise figure of the RF receiver referred to its input. SNR_{BB} is the SNR in the required bandwidth by the baseband (BB) receiver to pass the specs defined in the 3GPP 36.101 and (ECC-Report-266, 2017).

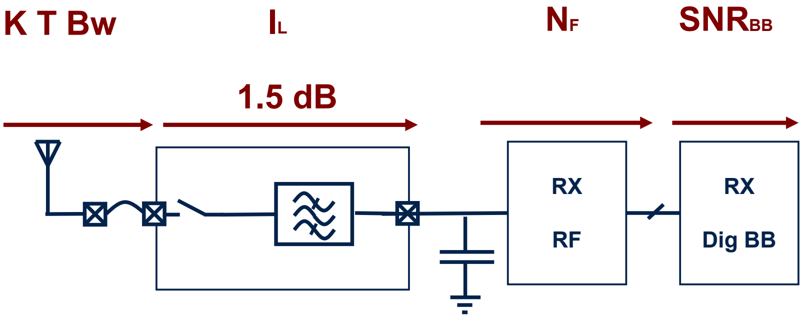


Figure 2.8: Sensitivity contributors in the RX chain.

For the NB-IoT standard, the P_n can be computed as,

$$P_n = 10\log_{10}\left(\frac{k.T.BW}{10^{-3}}\right) = 10\log_{10}\left(\frac{1.38064852 \times 10^{-23} \times 298.15 \times 180000}{10^{-3}}\right) = -121.3\ \text{dBm}, \tag{2.18}$$

where k is the Boltzmann constant, T is the temperature in Kelvin, and BW is the signal bandwidth in Hz. Correspondingly, the P_n for LTE-M can be estimated as $P_n = -113.6\,\text{dBm}$. According to 3GPP requirements, the standard sensitivities for LTE-M and NB-IoT are $-103.7\,\text{dBm}$ and $-108.2\,\text{dBm}$, respectively (3GPP, 2023). The standard-related specifications are highlighted in Table. 2.2 for both applications. To meet high coverage and penetration requirements with best-in-class performance concerning the state-of-the-art RX (Semiconductor, 2021), (S.A, 2019), (STMicroelectronics, 2022), a challenging sensitivity of $-115\,\text{dBm}$ is essential (6 dB below the standard requirements).

Table 2.2: Standard-related specifications.

Specification	**LTE-M**	**NB-IoT**
Channel BW (kHz)	1080	180
Thermal noise P_n (dBm)	-113.6	-121.3
Minimum sensitivity (dBm) (from 3GPP)	-103.7	-108.2
RX noise figure (dB)	6.5	9.6
Best-in class sensitivity (dBm)	-108	-115
LNA Noise Figure (dB)	<2	<2
Input Power Dynamic Range (dBm)	-108 to -25	-115 to -25

Considering the classical receiver chain as in Fig. 2.8, with an insertion loss $I_L = 1.5\,\text{dB}$ and an $SNR < 2\,\text{dB}$, the required RX noise figure (NF) should be less than 3 dB for the minimal input level ($P_{in} = -115\,\text{dBm}$) at maximum gain. While a NF of 8 dB is sufficient for the maximal input level ($P_{in} = -25\,\text{dBm}$) at minimal gain. Since the LNA is the main noise contributor as the first block in the RX chain (Appendix.B.1), it must comply with a minimal NF of 2 dB at the maximum gain.

Additionally, to accommodate the large input power dynamic range, various solutions have been implemented using an adaptive receiver with a multi-path chain of switched LNAs and mixers. Each path targets a frequency range or a sensitivity range by adjusting the gain, noise, power, and linearity performance (Bardeh et al., 2023), (T. W. Kim et al., 2009).

In this work, a single-path solution is proposed. A multi-mode wideband LNA with adaptive performance can be used to reduce the area and expand the design space through performance tunability. This proposed solution addresses multiple sensitivity modes depending on the input signal to trigger different behaviors of the single LNA as illustrated in Table 2.3.

Table 2.3: Table showing different sensitivity modes and their corresponding parameters.

Mode	High-Sensitivity	Medium Sensitivity	Low-Sensitivity
P_{in} (dBm)	-115 to -60	-60 to -40	-40 to -25
Gain	High	Medium	Low
Sensitivity	High	Medium	Low
Selectivity	Low	Medium	High

Furthermore, the selectivity and resilience towards RX blockers impose specific requirements on the LNA linearity performance. This mainly concerns the low-sensitivity mode since it targets highest input signals. Therefore, due to high blocker levels, a compression point P_{1dB} of $-15\,\text{dBm}$ and an IIP_3 of $-10\,\text{dBm}$ are required.

In addition to these requirements, an aggressive power consumption below 2 mW is targeted and a compact inductorless single-ended solution is preferable for seamless integration into IoT SoC. A comprehensive summary of the LNA's main specifications is provided in Table 2.4.

Table 2.4: Multimode LNA design specifications in the 28 nm *FD-SOI* CMOS technology.

Mode	High-Sensitivity	Medium Sensitivity	Low-Sensitivity
P_{in} (dBm)	-115 to -60	-60 to -40	-40 to -25
Minimum Signal level Channel BW	-115 dBm (NB-IoT), -108 dBm (LTE-M) 180 kHz (NB-IoT), 1080 kHz (LTE-M)		
Frequency (GHz)	$[0.44, 2.2]$	$[0.44, 2.2]$	$[0.44, 2.2]$
NF (dB)	<2	<5	<8
Power (mW)	<2	<2	<2
Return loss (dB) (50Ω)	<-10	<-10	<-10
Gain (dB)	>20	>15	>10
$IIP3$ (dBm)	>-40	>-20	>-10
$P1dB$ (dBm)	>-50	>-30	>-15

2.5 Technology consideration

In this thesis, the focus is on designing an energy-efficient LNA. To achieve this objective, the 28 nm *FD-SOI* CMOS technology from STMicroelectronics has been chosen. The utilization of *FD-SOI* technology provides distinct advantages for our design, including reduced footprint, energy optimization, and an additional tuning mechanism. The incorporation of the Body Bias feature introduces a novel approach to controlling LNA performance, enhancing the overall flexibility of the design.

The 28 nm *FD-SOI* CMOS technology features a planar device, similar to conventional bulk devices but with a distinctive innovative fabrication process. The channel, formed as a thin silicon film, lies on an Ultra-thin Burried oxide (BOX) layer. This process effectively reduces parasitic effects between the drain and source terminals of the transistor and the channel, consequently minimizing the impact of the short-channel effect (SCE) in comparison to bulk devices. Furthermore, channel controllability is significantly enhanced through the incorporation of the BOX layer over the substrate. This technological advancement not only mitigates parasitic challenges but also facilitates the implementation of the Body Bias feature, enabling dynamic variations in the transistor's threshold voltage (V_T). This innovation opens new possibilities to integrated circuit design, offering enhanced performance and adaptability for diverse applications (Clerc et al., 2020).

The 28 nm *FD-SOI* CMOS technology provides two families of devices, each exhibiting varying threshold voltages (V_T) based on their physical construction. These families are categorized as Regular-V_T (RVT) and Low-V_T (LVT), and their detailed structures are illustrated in Fig. 2.9. The impact of Body Voltage varies depending on the device family.

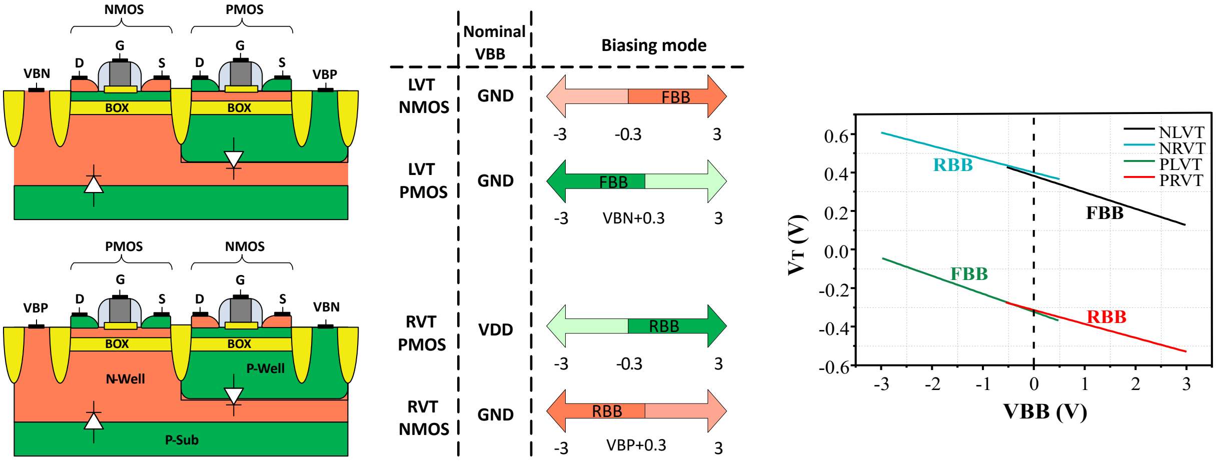


Figure 2.9: Cross section of 28 nm *FD-SOI* CMOS transistors: LVT transistors and RVT transistors with threshold voltage (V_T) variation versus the body-bias voltage (V_{BB}) for RVT and LVT transistors.

In the case of the LVT devices, the NMOS transistor is built over an N-well, necessitating a positive voltage at its body terminal. This configuration, known as Forward Body Biasing (FBB), decreases the V_T. On the other hand, for the RVT family, the PMOS transistor is built over an N-well, requiring a negative voltage at the body terminal. In this scenario, the V_T increases, and this configuration is denoted as Reverse Body Biasing (RBB).

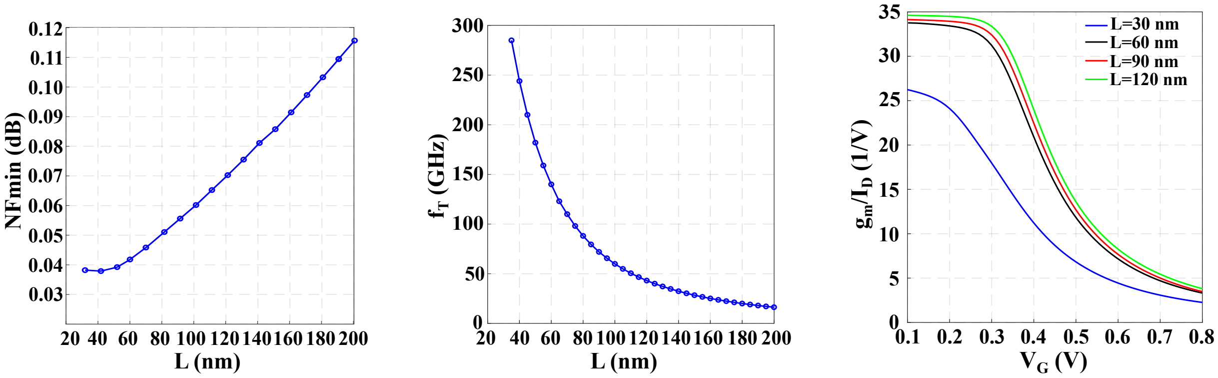
The choice of the Device Family is related to the utilization of the Body Bias feature and the benefits it can offer to the design process. This selection is dictated by the specifications and intended function of the circuit to be designed. In the context of this thesis, where the primary objective is the development of energy-efficient Low-Noise Amplifier (LNA) with optimal performance, the advantages presented by the LVT family align most favorably with this implementation. Leveraging FBB within the LVT family enables the efficient operation of ultra-low-power (ULP) and ultra-low-voltage (ULV) circuits. Additionally, fine-tuning the characteristics of NMOS transistors helps to avoid the generation of negative voltage sources.

Advanced nanometric technologies such as *FD-SOI* are geared towards VLSI applications. To address variability-related concerns in an analog anf RF application as the one presented in this thesis, it is recommended that both PMOS and NMOS transistors share a uniform length (L). In the context of the design examples presented in this manuscript, the appropriate transistor length is chosen based on specific technological characteristics, such as the minimal noise figure (NF_{min}), the transition frequency (f_T) and the g_m/I_D efficiency factor. In (Dickson et al., 2006), it is demonstrated through experimental results that the optimal NF_{min} current density is approximately $J_{opt} = 0.15\,\mathrm{mA}/\mu\mathrm{m}$, invariant over the frequency and technology node. The variation of the corresponding NF_{min} values as function of L at 1 GHz of a $W = 1\ \mu\mathrm{m}$ NMOS LVT transistor that is biased under these conditions is shown in Fig. 2.10.a. For $L < 60\,\mathrm{nm}$, the NF_{min} vary less around the minimal value. However, while L increases, the device noise increases exponentially.

The transition frequency f_T variation with L is shown in Fig. 2.10.b. for the same transistor current density. It illustrates that f_T decreases as L increases. For $L = 60\,\mathrm{nm}$, f_T exceeds 100 GHz, demonstrating suitability for the targeted application. Meanwhile, for a biasing targeting to improve f_T (Dickson et al., 2006), higher values up to 300 GHz can be achieved.

Additionally, Fig. 2.10.c highlights that the g_m/I_D efficiency factor is lower for $L = 30\,\mathrm{nm}$ compared to higher L values. Moreover, for $L \geq 60\,\mathrm{nm}$, g_m/I_D exhibits low variation over the V_G range with respect to transistor length.

Based on this analysis, $L = 60\,\mathrm{nm}$ is chosen as the uniform length for all implemented transistors, as it shows good balance between transition frequency, noise, power-efficiency and area trade-offs.



(a) NF_{min} as a function of L for NMOS LVT, with $W = 1$ µm and $J_{opt} = 0.15\,\mathrm{mA}/\mu\mathrm{m}$.

(b) Transition frequency f_T as a function of L for NMOS LVT, with $W = 1$ µm and $J_{opt} = 0.15\,\mathrm{mA}/\mu\mathrm{m}$.

(c) g_m/I_D as a function of V_G for different L for NMOS LVT.

Figure 2.10: 28 nm *FD-SOI* NMOS LVT transistor characteristics.

2.6 Conclusion

In this chapter the state-of-the-art of wideband sub-6GHz LNAs is revisited. More than 200 circuits published in the literature are reviewed and compared in terms of their performance metrics. We explore the trends related to the technology advance. Direct performance comparisons between the most common LNA topologies are provided. These comparisons, based on simple efficiency figures as well as on individual performances, clearly show the strengths, weaknesses, and trade-offs of each LNA topology and highlight design trends that could not be intuitively anticipated otherwise in the context of wideband LNA especially through the analysis based on compact FoMs. Finally, design enhancement solutions are explored for different topologies to show the performance boosting thanks to advanced techniques that are hard to be described and compared by simple analytical systems. For low power applications, advanced techniques are applied to the CG topology to improve its noise figure. It is shown that the g_m-boosting common-gate (CG) structure achieves a good trade-off between noise, power consumption, and gain, and better performance on average than the conventional noise-canceling structure CGCS. The outcome of these theoretical analysis and statistical first comparison results can shorten the list of choices of the possible topologies of the LNA when targeting a set of specifications dedicated to a challenging application.

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Chapter 3

Design Methodologies

Contents

3.1 Introduction

Taking advantage of the advanced CMOS technologies with their high transition frequency f_T and maximal frequency f_{max}, RF designs outside the classical strong inversion regime (Shaeffer & Lee, 1997) become possible. However, designing in moderate and weak inversion regimes, for which the transistor efficiency g_m/I_D is maximized, is a challenging task for advanced nanometric technologies. Usually, these designs rely on lengthy simulation-based optimization loops due to the complexity of the short channel transistor behavior and the lack of simple analytical models covering these regions. In this regard, different simplified design methodologies for RF circuits in general, and specifically for LNAs have been proposed in literature for exploring the moderate and weak inversion regions of operation. The rest of the chapter is organized as follows. Section 3.2 introduces the state-of-the-art of g_m/I_D design methodologies. In Section 3.3, a complete design-oriented transistor model that will be employed to build our proposed design methodology is detailed. Then, some design examples using common LNA architectures are described to illustrate our design methodology in Section 3.4. Finally, Section 3.5 concludes the chapter.

3.2 State-of-the-art of g_m/I_D design methodologies

Multiple RF analytical design methodologies have emerged in literature to assist designers in meeting specified requirements. These methodologies not only aid in achieving design targets but also provide valuable insights into the relationship between design performance and parameters. Among the numerous strategies proposed, the g_m/I_D efficiency factor have played an important role for the last two decades, reflecting both power/speed efficiency and the inversion region characteristics. This factor indicates the power consumption required to attain a specific gain, and its virtue lies in being independent of process parameters and scaling. To bridge the gap between system level and transistor level, the g_m/I_D and similarly, the inversion coefficient, are used to express the circuit performances as functions of the sizing parameters. In the context of IoT applications, designing at the maximal g_m/I_D in weak inversion is the optimal choice for low power circuits. Although working at high g_m/I_D improves the MOS transistor energy efficiency it implies a larger size (W) to reach a target gain (transconductance) for a low current I_D.

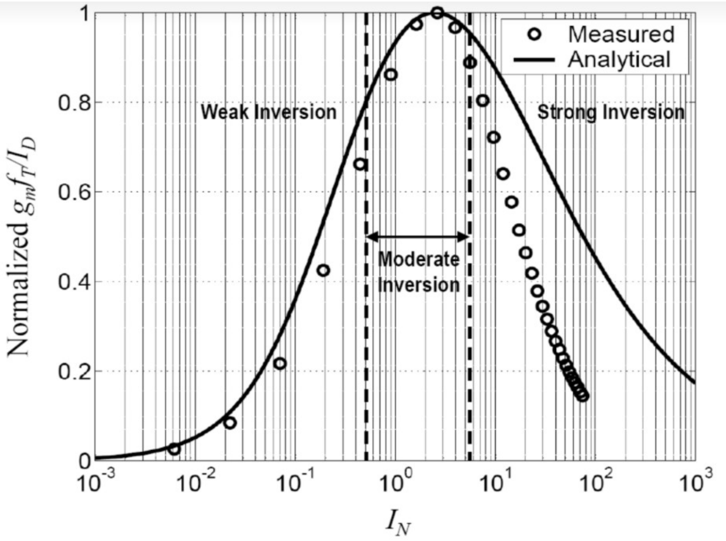


Figure 3.1: Normalized $(g_m f_T)/I_D$ function of I_N (inversion coefficient) for both theoretical expression and measurement result of a fabricated $NMOS$ with $W = 10$ µm and $L = 0.18$ µm (Shameli & Heydari, 2006).

Hence, larger parasitic capacitances start to dominate the transfer function of the device at higher frequencies, which finally reduces the bandwidth of the circuit. In this regard, a device figure of merit (FoM) is introduced in (Shameli & Heydari, 2006) to take f_T into consideration. The FoM is defined as,

$$FoM_{\text{(Shameli \& Heydari, 2006)}} = \frac{g_m.f_T}{I_D}. \tag{3.1}$$

As can be seen in Fig. 3.1, this FoM has a maximum in the moderate inversion region, that corresponds to the best efficiency-bandwidth trade-off.

While enabling the maximization of the efficiency-bandwidth product in RF IC design, this approach may not be optimal in certain cases, and its optimal region is technology-dependent. Additionally, this metric exhibits limitations when employed as a generic parameter for comprehensive design, as it represents a device-specific FoM and lacks direct relevance to the circuit topology.

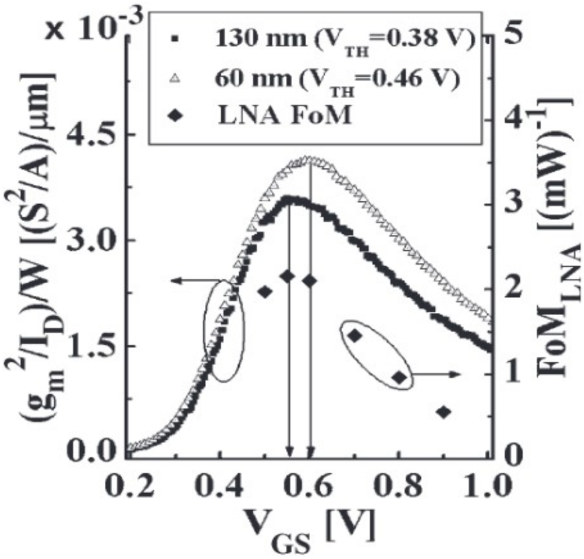


Figure 3.2: FoM for LNA and transistor (g_m^2/I_D): Similar trends for both characteristics, good estimation of corresponding V_{GS} for the maximum of FoM for the LNA for different technology nodes (Song et al., 2008).

In (Song et al., 2008), based on a small-signal analysis of a simple inductive degeneration common source topology, it is shown that the noise factor F-1 is proportional to $I_D/(g_m^2)$, and the gain G is proportional to $(g_m^2)/I_D$. Thus, the gain optimum point and the noise optimum point of nanoscale MOSFETs can be easily derived using a FoM based on the $(g_m^2)/I_D$ factor to predict the close optimum gate bias voltage as shown in Fig. 3.2. It is concluded that maximizing this factor successfully predicts the close optimum gate bias voltage which maximizes the LNA FoM expressed as,

$$FoM_{(\text{Song et al., 2008})} = \frac{G}{(F-1)P}. \tag{3.2}$$

In (Fadhuile et al., 2014), the design of a narrowband complementary common source with a resistive feedback is also optimized based on a circuit figure of merit defined by,

$$FoM_{\ (\text{Fadhuile et al., 2014})} = \frac{G.f_{req}}{(F-1)P}. \tag{3.3}$$

This design methodology aims to derive the optimal inversion coefficient I_C and uses an iterative loop and the EKV formalism to determine the component sizes that satisfy the design specifications. The optimal point is determined graphically as shown in Fig. 3.3. In the same context, a three-step design methodology for a LNA based on g_m/I_D and inversion coefficient was introduced in (Guitton et al., 2019). Starting from the small-signal circuit of the shunt feedback current reuse LNA, and based on the EKV formalism, the topology is described by expressing the normalized active, passive and noise parameters in terms of the inversion level IC. As a second step, main equations are derived and the definition of RF metrics in terms of sizes and ICs of the transistors are defined. Finally, depending on the application, a figure of merit is defined as follows,

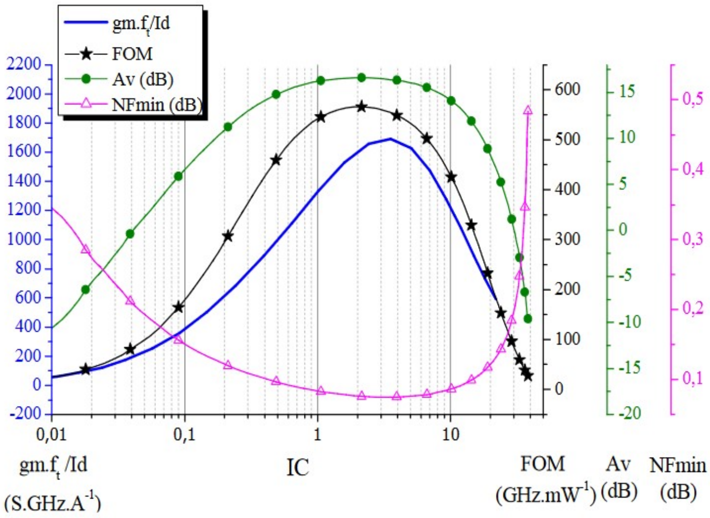


Figure 3.3: Gain, Minimum Noise Figure, FoM at 2.4 GHz and $g_m.f_t/I_D$ versus IC (Fadhuile et al., 2014).

$$FoM_{\ (\text{Guitton et al., 2019})} = \frac{G.Bw}{(F-1)P_{dc}}. \tag{3.4}$$

The optimal sizes and working points are derived by mapping the local and global maxima of (3.4) as function of an input set of variables. This methodology allows to efficiently navigate in the design space, in particular for LNA blocks. The accuracy was proven through the design of five state-of-the-art LNAs (2019) for two typical set of specifications in three different CMOS nodes 28 nm *FD-SOI* CMOS, 65 nm and 130 nm bulk CMOS. However, the proposed design space exploration method does not take into account the linearity performance of the amplifier at early stage and evaluates it as a design consequence. Besides, these methodologies ((Song et al., 2008), (Fadhuile et al., 2014), (Guitton et al., 2019)) aim to optimize a particular figure of merit and do not allow a systematic design targeting particular optimization points.

To cover the limitation of some design-oriented transistor model that are not taking into account the short channel and the non-linearity effects, some design strategies combine the g_m/I_D methodology with specified Look-Up Tables (LUT) (P. Jespers & Murmann, 2017). The LUTs are databases that list a range of characteristics of a transistor as function of design variables, such as transistor size or circuit components. These tables can also include circuit performance estimations based on the variation of other performance or transistor characteristics. It is crucial to note that LUTs are primarily useful for providing a comprehensive view of the circuit design space under various variable changes. For instance, in (Siniscalchi et al., 2020), a strategy based on the Advanced Compact Model (*ACM*) (Galup-Montoro & Schneider, 2007) associated with a LUT for the output conductance g_{ds} inclusion, allows the extraction of the main parameters of the

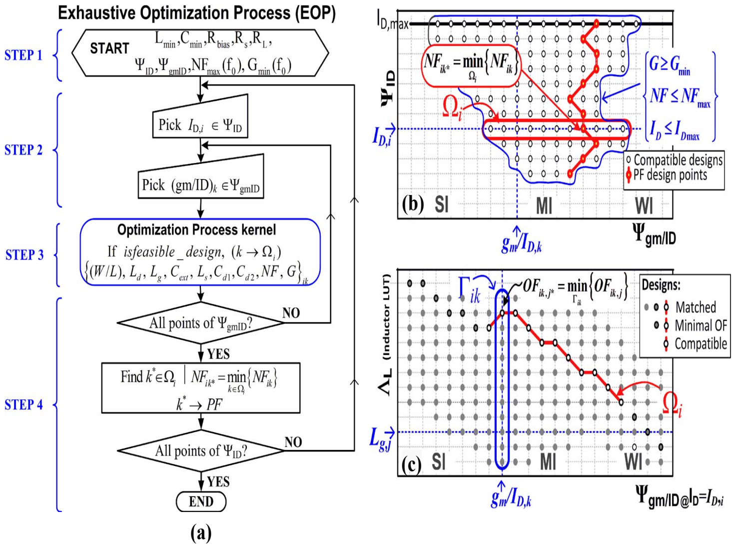


Figure 3.4: a. Flow diagram of the proposed CS-LNA optimization process. b. Conceptual representation of outputs and sets involved in EOP. c. Conceptual representation of outputs and sets involved in EOP Kernel (Fiorelli et al., 2014).

transistor simply and very accurately using the 28 nm *FD-SOI* CMOS technology. In the same context, the authors in (Fiorelli et al., 2014) investigate the weak to moderate inversion region to design a low power CS LNA based on LUT which accurately describe the behavior of the transistor and on design space maps, as shown in Fig. 3.4, to determine the adequate design.

In order to reduce the complexity of using LUT and to have comprehensive design procedure, some design methodologies are fully-based on design-oriented transistor models such as the *ACM* and *EKV* with their different versions. A capacitive feedback LNA (Liu et al., 2018) designed using a g_m/I_D algorithm in *ACM* model succeeds to achieve good measurement results in agreement with the analytical predictions. In (Bourdel et al., 2021), a resistive feedback LNA is also designed in the 28 nm *FD-SOI* CMOS technology. The main LNA performance equations are expressed as function of the transistor parameters and inversion coefficient i_f. This links, in a direct way, the targeted metrics to the design variables. The methodology is fully analytical and does not rely on optimizing a specific *FoM*. Although the used transistor model is simple, it does not cover all the short channel effects, which limits the exploration of a wide design space.

A novel methodology is reported in (Castagnola et al., 2020) based on a unified analysis. As shown in Fig. 3.5, this analysis extracts the metrics in terms of g_m/I_D parameter based on the ACM model and equations and links these parameters to the scattering matrix. The S-parameters are used independently to verify if the target specifications are reached at each iteration loop.

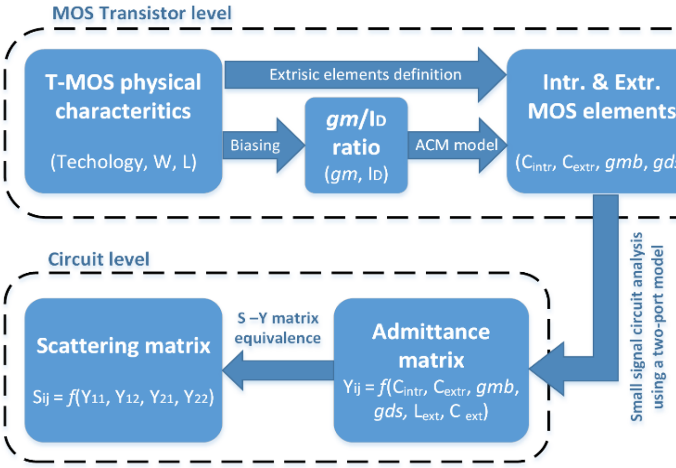


Figure 3.5: Procedure for obtaining S-parameters by means of the MOS physical characteristics (Castagnola et al., 2020).

Although these strategies focus on the transistor's behavior with respect to the gate voltage and inversion coefficient, they are based on models that do not explicitly capture the metrics dependent on the drain voltage. In advanced technologies, the transistor's behavior varies with the drain voltage, which impacts circuit performance, especially non-linearity effects. In this chapter, we present a design-oriented transistor model that will allow us to overcome the aforementioned limitations, while keeping a reduced level of complexity.

3.3 Transistor model

3.3.1 Introduction

The design of integrated circuits relies on theoretical calculations and simulations to set the adequate component sizes and operation points that comply with the design targets. However, in the usual practice these simulations are based on complex models included in the technology design KIT (PDK), while theoretical analysis require simple equations modeling the behavior of the circuit for fast design. Since the MOSFET is one of the main building blocks in current ICs, lots of works have been focusing on accurately modeling the MOSFET since 1960s (Sah & Jie, 2005). Following the Moore's law (Moore, 2006a), (Moore, 2006b) with the increase of circuits complexity and density, the transistor's feature size has been continuously reduced over time, which has led to the appearance of new physical effects with respect to the traditional long-channel transistor. Thus, many designers and modeling papers have focused on these short-channel effects and their introduction to transistor models in order to maintain the accuracy of simulations and calculations. As an example, BSIM (Chauhan et al., 2012), BSIM-IMG (Agarwal et al., 2020; Kushwaha et al., 2016), UTSOI2 (Poiroux, Rozeau, Scheer, Martinie, Jaud, et al., 2015; Poiroux, Rozeau, Scheer, Martinie, Jaud, et al., 2015) and their respective versions are the most used compact models for simulations using EDA tools related to the technology set including *FD-SOI* technologies. In order to fit the measured transistor characteristics across all the operation regions and regimes, an extremely large number of parameters and multiple fitting functions are used in these models. Although the precision and the accuracy are high, the complexity of these models make them not suitable for hand calculation and fast theoretical design. Besides, the correlation between the phenomena behind short-channel effects and the correction parameters is hard to be explicitly interpreted. Hence, simple design-oriented descriptions of the MOSFET are needed for theoretical design methodologies. For instance, the EKV model introduced by C. Enz, F. Krummenacher and E.A. Vittoz (Christian C. Enz, 2006; C. C. Enz et al., 1995) and the Advanced Compact MOSFET (ACM) model (Cunha et al., 1998; Galup-Montoro & Schneider, 2007) describe the transistors' DC and small-signal behavior with good accuracy and reduced complexity. Both models are inversion charge linearization-based models and model the drain current as a continuous function of the device terminal voltages. They share most of the equations set except for some definitions such as the normalization charge and the pinch-off voltage. Basic versions of ACM and EKV employ three parameters to model the transistor: the specific current I_S, the threshold voltage V_{T0} and the slope factor n, which are compliant with standard circuits design for different applications (Cunha et al., 1998; P. G. Jespers & Murmann, 2015). These models offer an accurate description of a long-channel transistor's DC behavior. Taking into account the short-channel effects in more advanced technologies require the introduction of additional model parameters, which, ultimately, increase the model complexity. Thus, in (C. Enz et al., 2017) and (Da Silva et al., 2008) the carrier velocity saturation effect in strong inversion region is taken into account for the EKV and ACM formalisms respectively. Besides, a recent version of the ACM model is introduced in (Adornes et al., 2022) to describe symmetrically the Drain-Induced-Barrier-Lowering (DIBL) effect. Despite of being simple and more accurate especially for short-channel transistors, the 4-parameter models do not cover the effects on the linear region of the transistor characteristic. On the other hand, a complete all-region all-regime design-oriented model is introduced in (Pino-Monroy et al., 2022). It is based on a 7-parameter version of ACM. It accurately models the main short-channel effects and the dependence of the transistor drain current on the drain voltage, at the cost of increasing the model complexity.

In this thesis, we have developed a design-oriented model that offers a good trade-off between accuracy and complexity for low-power analog and RF design applications. Indeed, for these applications, transistors are often biased in moderate-weak regions, while some short-channel effects only manifest for strong inversion. The proposed model is described in the next subsection.

3.3.2 5(6)-parameter design-oriented transistor model

The proposed design-oriented transistor model describes the transistor's behavior using 5 (6 for *FD-SOI*) DC parameters directly linked to physical effects. This model introduces novel specificities that augment the classical versions. Notably, velocity saturation is addressed at an early stage through the integration of single-piece equations, as demonstrated in (Neto, Bouchoucha, et al., 2023; Neto, Adotnes, et al., 2023). An innovative contribution in this model is its adaptability to both bulk and SOI-based technologies. Besides, our model offers a comprehensive framework, capturing static features and aiding in the analysis and synthesis of small-signal responses, making it very useful in design. In the following, the model is denoted as 5PM/6PM. The 5PM/6PM is based on the charge-controlled model of the drain current proposed by (Maher & Mead, 1987), that considers both the drift and diffusion components of the current as well as the saturation velocity phenomenon, yielding (3.5).

$$I_D = I_S \frac{(q_S + q_D + 2)}{1 + \zeta |q_S - q_D|} (q_S - q_D) . \tag{3.5}$$

The normalized inversion charge densities at source (q_S) and drain (q_D) are defined as the inversion charge densities $Q_{S(D)}$ normalized to the thermal charge density $-nC_{ox}\phi_t$ as given in (3.6).

$$q_{S(D)} = \frac{Q_{S(D)}}{-nC_{ox}\phi_t}, \tag{3.6}$$

where C_{ox} is the oxide capacitance per unit area, n is the slope factor and ϕ_t is the thermal voltage. The specific current I_S, given in (3.7), is related to the gate width W and length L, and to technology parameters. μ is the carrier mobility.

$$I_S = \mu n C_{ox} \frac{\phi_t^2}{2} \frac{W}{L}. \tag{3.7}$$

Parameter ζ is a short-channel parameter associated with the velocity saturation (v_{sat}) phenomenon. It is defined by (3.8) as the ratio of a diffusion-related velocity to the saturation velocity.

$$\zeta = \frac{\frac{\mu \phi_t}{L}}{v_{sat}}. \tag{3.8}$$

For a sufficiently large L, the denominator in (3.5) is approximately unity, thus we can ignore velocity-saturation effects and (3.5) reduces to,

$$I_D = I_S \left[q_S^2 - q_D^2 + 2(q_S - q_D) \right], \tag{3.9}$$

where the quadratic terms arise from drift while the linear terms arise from diffusion (da Costa Gouveia-Filho et al., n.d.; Galup-Montoro & Schneider, 2007; Maher & Mead, 1987). Comparing (3.5) and (3.9) we observe an important consequence of velocity saturation in the drain current expression. For long-channel transistors, $\zeta \to 0$ and (3.9) holds; thus, an increase in the drain-to-source voltage reduces the normalized drain charge; consequently, the drain current increases. In contrast, for short-channel devices (3.5) holds and the drain current can attain a maximum, as shown in Fig. 3.6.

The extremum condition for (3.5),

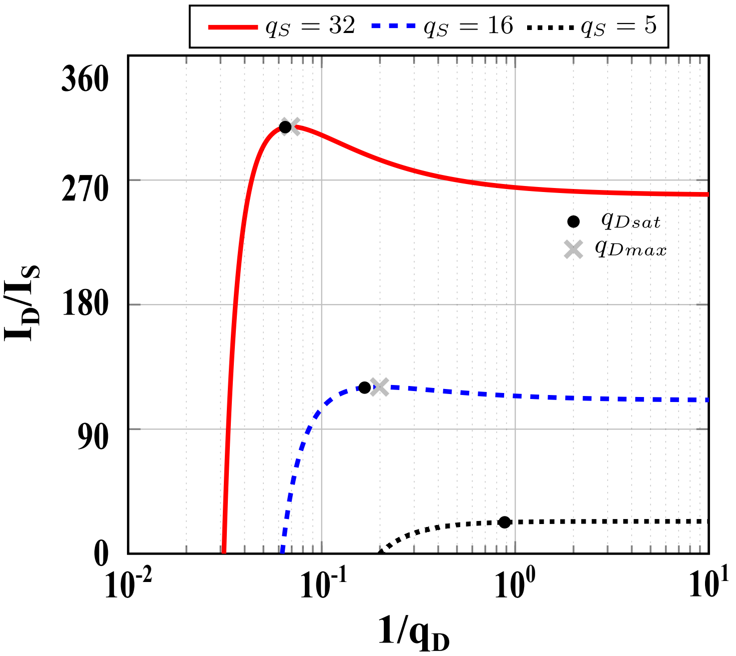


Figure 3.6: Characteristic of the drain current, eqn. (3.5), for a velocity saturation parameter $\zeta = 0.1$. The $1/q_D$ horizontal axis is chosen in order to plot saturation as usual in the right direction of the output characteristics.

$$I_D = \left.\frac{dI_D}{dq_D}\right|_{q_{Dmax}} = 0, \tag{3.10}$$

gives,

$$q_{Dmax} = q_S + \frac{1}{\zeta} - \frac{1}{\zeta}\sqrt{1 + 2\zeta(q_S + 1)}. \tag{3.11}$$

Multiplying and dividing (3.11) by the algebraic conjugate we obtain:

$$\frac{q_{Dmax}}{q_S} = \frac{\zeta q_S - \frac{2}{q_S}}{1 + \zeta q_S + \sqrt{1 + 2\zeta(q_S + 1)}}. \tag{3.12}$$

Thus, we have a maximum in the I_D vs. q_D $(1/q_D)$ curve for

$$q_S > \sqrt{\frac{2}{\zeta}}. \tag{3.13}$$

The bump in the output characteristics has no physical meaning, but even when the output characteristics increases monotonically (e.g., in weak inversion), the saturation for q_D going to zero has no physical meaning either. In effect, due to the saturation velocity of the carriers, the absolute value of the carrier charge at the drain end has a minimum, given by (da Costa Gouveia-Filho et al., n.d.; Galup-Montoro & Schneider, 2007), as,

$$I_{Dsat} = -W v_{sat} Q_{sat}, \tag{3.14}$$

or, using normalized variables, as,

$$i_{Dsat} = \frac{I_{Dsat}}{I_S} = \frac{2}{\zeta} q_{Dsat}. \tag{3.15}$$

From (3.5) and (3.15), the drain charge density normalized to the thermal charge density is given by,

$$q_{Dsat} = q_S + 1 + \frac{1}{\zeta}\sqrt{\left(1 + \frac{1}{\zeta}\right)^2 + \frac{2q_S}{\zeta}}. \tag{3.16}$$

Comparing (3.11) and (3.16) it is easy to verify that,

$$q_{Dsat} > q_{Dmax}. \tag{3.17}$$

Thus, physical saturation occurs always in the triode region (before the bump) of the output characteristics. It is interesting to observe that for the strong inversion model, $q_{Dmax} = q_{Dsat}$, as shown in page 248 of (Tsividis, 2012). Thus, in the strong inversion model, saturation velocity occurs at the maximum of the output curve.

The unified charge-control model (UCCM) (da Costa Gouveia-Filho et al., n.d.; Galup-Montoro & Schneider, 2007) expresses the relationship between the terminal voltages and the normalized charge densities for all inversion levels of a long-channel transistor. In the UCCM, the source and drain normalized charge densities q_S and q_D are calculated using (3.18).

$$\frac{V_P - V_{S(D)B}}{\phi_t} = q_{S(D)} - 1 + \ln q_{S(D)}. \tag{3.18}$$

The pinch-off voltage V_P is linearly approximated by (3.19), where V_T is the threshold voltage (C. C. Enz et al., 1995).

$$V_P = \frac{V_{GB} - V_T}{n}. \tag{3.19}$$

Applying (3.18) to the source and drain we obtain the symmetrical expression (3.20), that links q_S and q_D with the potential drop V_{DS} along the channel.

$$\frac{V_{DS}}{\phi_t} = q_S - q_D + \ln\left(\frac{q_S}{q_D}\right). \tag{3.20}$$

For a long channel transistor, it is clear from (3.20), that $q_D \to 0$ when $V_{DS} \to \infty$. The classical way to deal with velocity saturation using (3.18) is to calculate the drain-to-source saturation voltage substituting q_D by its saturation value. In the present model we avoid the definition of a saturation voltage substituting $q_{S(D)}$ by $q_{S(D)} - q_{Dsat}$ in (3.20), getting (3.21).

$$\frac{V_{DS}}{\phi_t} = q_S - q_D + \ln\left(\frac{q_S - q_{Dsat}}{q_D - q_{Dsat}}\right). \tag{3.21}$$

Equation (3.21) has the necessary properties to model the effect of the velocity saturation of the carriers using single-piece equations. In effect, $V_{DS} = 0$ for $q_S = q_D$, $q_D \to q_{Dsat}$ when $V_{DS} \to \infty$, and if we interchange q_S and q_D, V_{DS} changes sign.

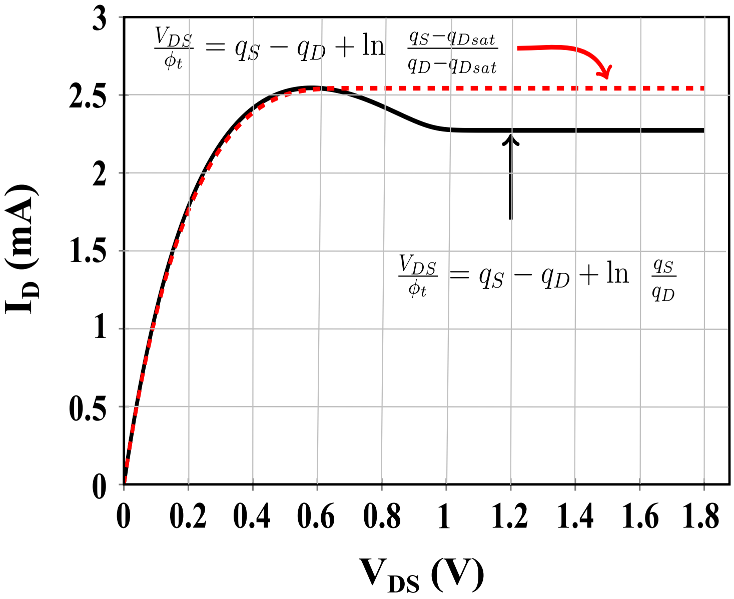


Figure 3.7: Effect of the maximum of $I_D(q_D)$ on the output characteristic $I_D(V_D)$.

MOS transistors are symmetrical devices; therefore, their models must also be symmetrical, *i.e.* the drain and source terminals can be chosen arbitrarily, but the transistor characteristics must remain the same regardless of the choice that has been taken. Furthermore, the transition between forward ($V_{DS} > 0$) and reverse ($V_{DS} < 0$) operations must be continuous.

In the 5PM (Only for Bulk technologies), UCCM and the pinch-off definition are modified to include saturation velocity and DIBL (drain-induced barrier lowering) effects preserving the symmetry of the MOSFET in its model. This is a all-region, all-regime continuous model in contrast with (Pino-Monroy et al., 2022) that uses the interpolation function introduced in (Joardar et al., 1998) to obtain the continuity between the triode and the saturation regions. In effect, substituting $q_{S(D)}$ by $[q_{S(D)} - q_{Dsat}]$ in (3.18), we obtain the modified UCCM (3.22), with asymptotic saturation.

$$\frac{V_P - V_{S(D)B}}{\phi_t} = q_{S(D)} - q_{Dsat} - 1 + \ln q_{S(D)} - q_{Dsat}. \tag{3.22}$$

It is important to remark that (3.5) and (3.22) preserve the symmetry of the transistor, i.e., if we interchange q_S and q_D, both I_D and V_{DS} change sign.

As shown in Fig. 3.7, the uses of the modified UCCM (3.21), (3.22) avoids the bump in the output characteristic without the need of an interpolation function. The commonly used interpolation functions between the triode and saturation regions not only complicate the code of the model but also produce glitches in the derivatives and don't preserve the so-called Gummel symmetry (Xia, 2020).

Finally, the introduction of σ, the drain-induced barrier lowering (DIBL) coefficient, at both source and drain, keeps the device symmetry (da Costa Gouveia-Filho et al., n.d.; Galup-Montoro & Schneider, 2007). V_{T0} is the equilibrium threshold voltage.

$$V_T = V_{T0} - \sigma(V_{SB} + V_{DB}). \tag{3.23}$$

Transistors in Silicon On Insulator (SOI)-based technologies have a fourth terminal, the back gate, that can be used as a tuning knob to control the channel (Clerc et al., 2020). The back gate is coupled to the channel with an insulator thicker than that between the main gate and the channel. The back gate acts as a secondary gate that allows for a fine-tuning of the device characteristics, especially through the modulation of the threshold voltage. The transistor model of SOI-technologies is completed, then, through the introduction of parameter δ, which models the threshold voltage variation with the body-bias voltage V_{BB}. For a SOI N-type transistor in which $V_{BB} = 0$ V, the model coincides with that of the bulk technology. Hence, the additional 6th parameter δ characterizes exclusively the *FD-SOI* features and allows to have the model of the bulk technologies to be adapted to SOI technologies and be denoted $5PM/6PM$. This extended (6PM) version of the 5PM model shares the same aforementioned equations; however, the terminal charge densities are solved for the modified expression of the threshold voltage, given by,

$$V_T = V_{T0} - \sigma(V_S + V_D) - \delta V_{BB}. \tag{3.24}$$

The sign of δ can address the forward and reverse modes for both channel types.

For the 28 nm *FD-SOI* CMOS technology, the variation of the threshold voltage V_T as a function of the body-bias voltage is explicitly explained in (Clerc et al., 2020) and reported in Fig. 3.8. Note that, for 4 transistor types, the linear approximation in (3.24) of the threshold voltage with the body-bias voltage fits very well the experimental results.

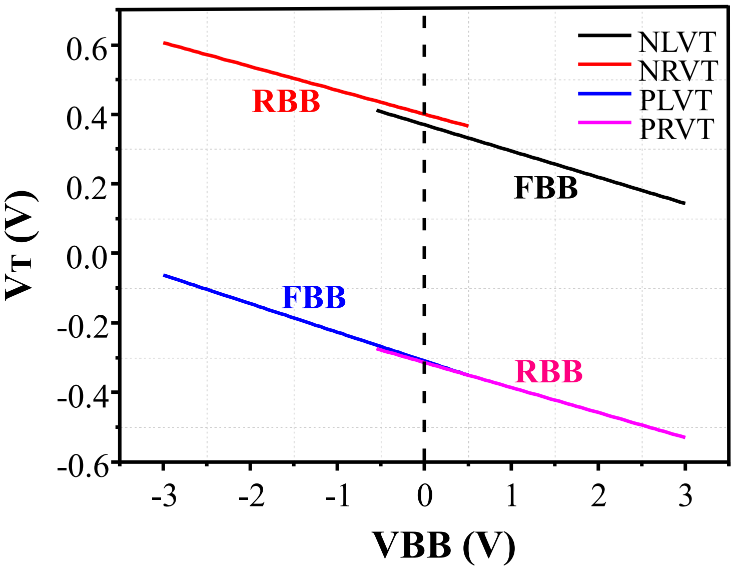


Figure 3.8: Threshold voltage variation as function of the body bias voltage for NMOS (N) and PMOS (P) transistors using the regular threshold voltage flavor (RVT) and the low threshold voltage flavor (LVT) from the 28 nm *FD-SOI* CMOS tehnology (Clerc et al., 2020).

The PMOS model can be easily expressed using the generic formalism defined for the NMOS transistor with minor changes. It maintains the same charge densities and currents definitions as well as the effect of the short channel parameters. The terminal voltages, since they are referred to a higher potential (V_{DD}), can be defined with a negative sign to be implemented using the same charge-voltage equations (3.18), (3.19), (3.21), (3.24).

Fig. 3.9 summarizes the 6 model parameters and their physical meaning to give an overview of the proposed model.

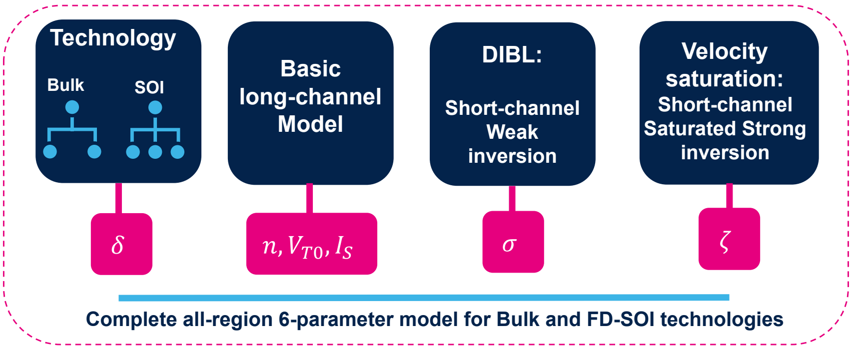


Figure 3.9: Simple representation of the complete all-region ACM MODEL.

3.3.3 Parameter extraction

The procedure to extract the 6 main parameters used in this model is detailed below. It can be based on simulation or measured data for a specific type of transistor. The extraction procedure assumes a fixed channel length L. In this section, we detail the case for the n-channel low threshold voltage *LVTNFET-RF* from the 28 nm *FD-SOI* CMOS technology of STMicroelectronics with a channel length of $L = 60\,\text{nm}$ using simulation results. These parameters are essential for accurate modeling of the transistor behavior and performance. The extraction procedure involves fitting the simulated or measured data to the appropriate equations to obtain the parameter values. The accuracy of the extracted parameters is critical for the reliability and predictability of the model, and great care must be taken to ensure that the extraction procedure is performed correctly.

To extract the basic 3 parameters first introduced in long-channel models, we use the g_m/I_D curve as explained in (Adornes et al., 2022). Using the basic 3-parameter version of the ACM model V_{DS} expression (3.25), a specific point can be identified. Where i_f and i_r are the forward and reverse inversion levels respectively. The extraction method is based on identifying the particular point $i_f = 3$, $i_r = 2.12$ for $V_{DS} = \phi_t/2$. The testbench used to apply this extraction methodology for n, V_{T0} and I_{S0} is shown in Fig. 3.10. At constant V_{DS}, the V_{GS} is swept and the current I_D, its derivative g_m and g_m/I_D are plotted as functions of V_{GS} as shown in Fig. 3.11.

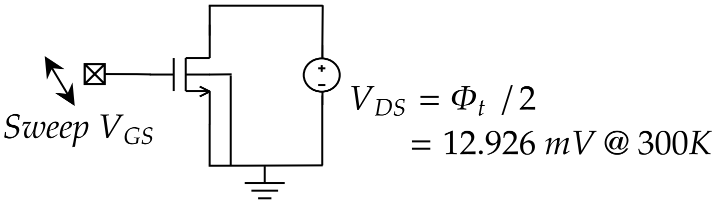


Figure 3.10: Simplified testbench to extract n, I_{S0} and V_{T0}.

$$V_{DS} = \phi_t \left[\sqrt{1+i_f} - \sqrt{1+i_r} + \ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right)\right] \tag{3.25}$$

Under this specific condition, the gate voltage V_G coincides with the threshold voltage at equilibrium V_{T0} when g_m/I_D reaches 0.531 times its maximal achievable value in weak inversion as,

$$\frac{\frac{g_m}{I_d}}{\max\left(\frac{g_m}{I_d}\right)} = \frac{2}{\sqrt{1+i_f}+\sqrt{1+i_r}}, \tag{3.26}$$

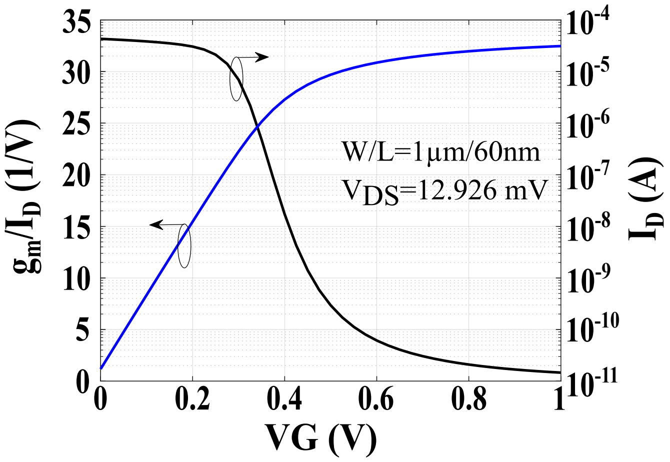


Figure 3.11: g_m/I_D and I_D variations with the gate voltage V_G for $L = 60\,\text{nm}$, $W = 1\mu\text{m}$ and $V_{DS} = \phi_T/2$.

where the normalized specific current (I_{S0}) corresponds to the value of the drain current I_D when $V_{GS} = V_{To}$, divided by 0.88 and obtained by computing Eq. (3.27). Thus, V_{To} and I_{S0} are extracted assuming that the variation of the slope factor n is negligible while the V_{GS} is swept. For instance,n is extracted using the maximal value of the g_m/I_D which is identified as $(g_m/I_D)_{max} = 1/n\phi_t$.

$$I_{S0} = I_D \frac{L_{eff}}{W} \frac{1}{i_f - i_r}. \tag{3.27}$$

The DIBL coefficient is a small-signal parameter that could be extracted following different methods. A simple method consists in computing the ratio between the variation of the gate voltage over the variation of the drain voltage for the same current (I_{D0}) in weak inversion as,

$$\sigma = -\frac{\Delta V_G(I_{D0})}{\Delta V_D} = \frac{V_{G1}(I_{D0}) - V_{G2}(I_{D0})}{V_{D2} - V_{D1}}. \tag{3.28}$$

As an example, the current is plotted for two different values of V_{DS} as function of V_G as shown in Fig. 3.12.

The velocity saturation parameter ζ (Galup-Montoro & Schneider, 2007) that completes the 5PM can be extracted from the combination of (3.15) with (3.16), which gives,

$$\zeta = \frac{2\left(q_S + 1 - \sqrt{1 + i_{Dsat}}\right)}{i_{Dsat}}. \tag{3.29}$$

The normalized source charge q_S can be calculated using parameters (V_{T0}, n, σ) and (3.18). The value of i_{Dsat} is equal to the drain current, normalized to the specific current I_S. The drain current is either measured or simulated, for a given operation point

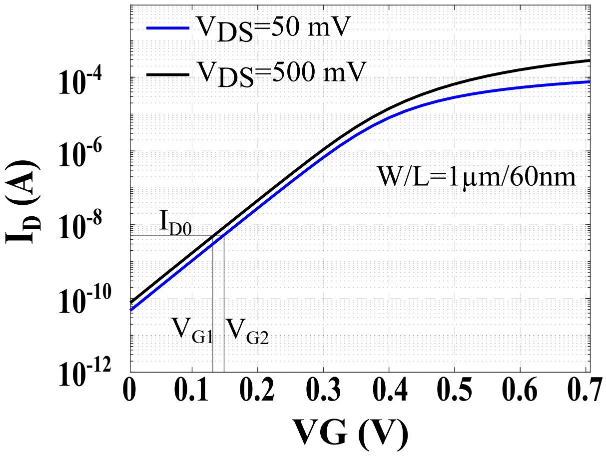


Figure 3.12: I_D vs V_G characteristics for $V_{DS} = 50$ mV and 500 mV for $L = 60$ nm.

(V_G, V_D, V_S, V_B) in the saturation region. For the extraction of ζ in the NMOS transistor, the operation point was set to $V_G = V_D = V_{DDmax}$ and $V_S = V_B = 0\,\text{V}$.

For the extraction of parameter δ, a plot of the threshold voltage versus the body-bias voltage, similar to that of Fig. 3.8 can be used. The line slope corresponds to δ.

Table 3.1 presents the extracted parameters of the NMOS and PMOS transistors low threshold voltage (LVT) of the 28 nm *FD-SOI* CMOS technology.

Table 3.1: Extracted parameters.

Technology	**28 nm**	
Transistor	**NMOS**	**PMOS**
W/L (μm/μm)	1/0.06	1/0.06
$\boldsymbol{V_{T0}}$ **(mV)**	389	-404
$\boldsymbol{I_S}$ **(μA)**	3.15	0.76
$\boldsymbol{n}$	1.15	1.01
$\boldsymbol{\zeta}$	0.039	0.024
$\boldsymbol{\sigma}$	0.018	0.029
$\boldsymbol{\delta}$	0.082	0.079

3.3.4 DC characteristics

The proposed 5PM/6PM design-oriented model was implemented in MATLAB® using the 443 Algorithm (Fritsch et al., 1973) (appendix A) to solve the UCCM equation as detailed in the flowchart in Fig. 3.13. The obtained results are compared to the UT-SOI2 compact model implemented in the design KIT and measured results for different bias conditions and transistor sizes. For sake of simplicity, the comparison is done for a low threshold voltage RF “*LVTNFET-RF*” of the 28 nm *FD-SOI* CMOS technology from STMicroelectronics with length $L = 60\,\text{nm}$ and width $W = 1\,\mu\text{m}$ for which the corresponding parameters were extracted.

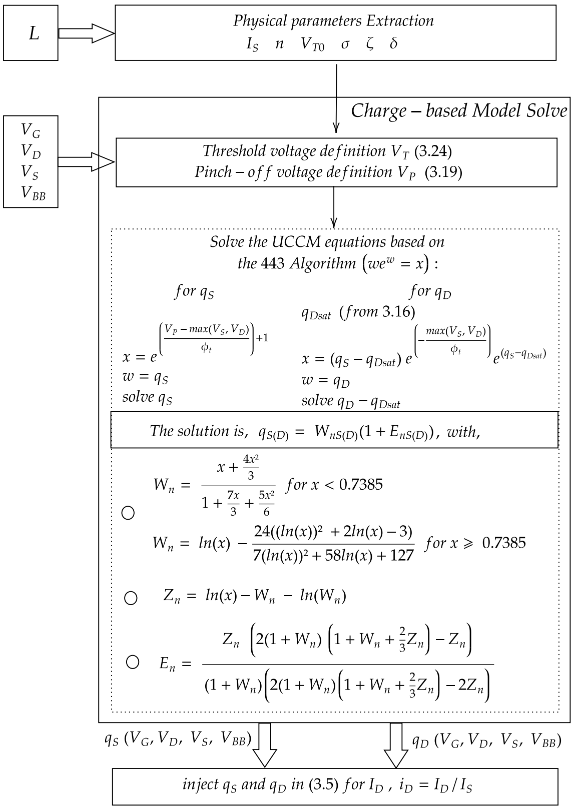


Figure 3.13: flow diagram to solve q_S and q_D using the 443 algorithm.

Fig. 3.14 shows the transistor's DC drain current as a function of the gate voltage evaluated for different drain voltages. Fig. 3.14 compares the proposed model, UTSOI2-based simulations and measurements data for a drain voltage V_D swept from $50\,\text{mV}$ to $1\ \text{V}$ ((a) to (e)) for $V_{BB} = V_{BN} = 0\,\text{V}$ and $V_D = 500\,\text{mV}$ with $V_{BB} = V_{BN} = 1\,\text{V}$ (f). In a secondary y-axis, the relative error of the 5PM/6PM model with respect to the measurements is shown. The x-axis sweeps the different inversion regions of the device since it covers the allowed range of V_G in the technology ($0\,\text{V}$ to $V_{DDmax} = 1\,\text{V}$). Besides, the different curves are shown for different saturation region to track the effect of V_{DS}.

Fig. 3.14.a ($V_{DS} = 50\,\text{mV}$) shows the current characteristic in linear region. For $V_{GS} < 0.7\,\text{V}$, which covers subthreshold, weak inversion, moderate inversion and early strong inversion regions, the relative error with respect to the measurements is less than 20% and the model captures the behavior of the current with a small deviation in the high V_{GS} region. For higher V_{DS} values the transistor enters in saturation region, and the relative error is reduced to close to 0%. Since the model is design-oriented and is used as a simple tool to predict the transistor behavior analytically, the most interesting regions for which a

good fitting is required are mostly the weak to moderate inversion regions in saturation. In fact, these regions are required for low-power design, and saturation region is important for some circuits to control the DC biasing. Using the introduced 5PM version, the obtained ($I_D(V_G)$) curves are very close to the transistor characteristic obtained from the PDK model and direct characterization measurements. Hence, the simple model is well adapted to short channel transistors as well as large drain to source voltages that were not captured in most models in literature. The complementary parameter δ, is implemented to compare the transistor description with measured results in presence of body voltage $V_{BN} = 1\,\mathrm{V}$ as an illustrative example.

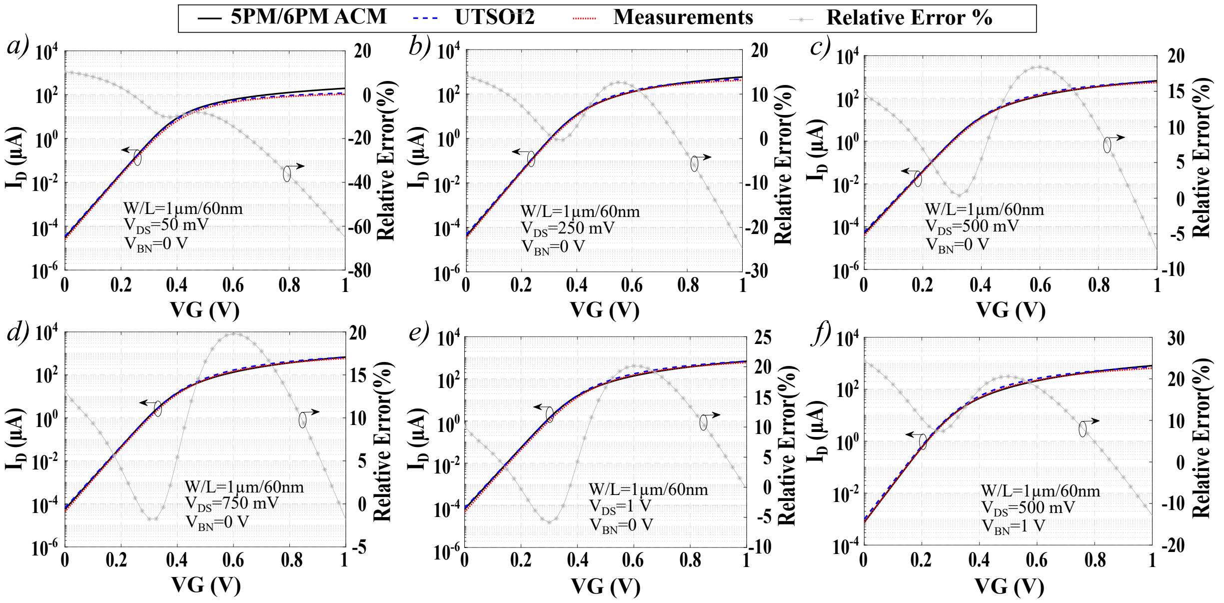


Figure 3.14: $I_D - V_G$ Characteristics for a NMOS LVT *FD-SOI* transistor with $W/L = 1µm/60\,\mathrm{nm}$ for different V_{DS} and body bias voltages VBN over the nominal dynamic of V_G.

As shown in Fig. 3.14.e the measured results of the drain current to gate voltage characteristic are compared to the model with applying the body-bias voltage $V_{BB} = V_{BN}$ for this NMOS transistor. This verification is followed for different V_{DS} values to cover all operation regions. The current relationship is well fitted and the model prediction is in good agreement with the measured values in all regions with a relative error below 20%. The accuracy of the 5PM/6PM model estimations is validated through measurements and in comparison with the PDK compact model. Besides, the inclusion of the body bias voltage in the model effectively reshapes the characteristic curve of the transistor as predicted by lowering the threshold voltage and follows accurately the measured current.

The DC drain current as a function of the DC drain voltage ($I_D(V_D)$) is plotted in Fig. 3.15 for different inversion regions at $V_G = \{100\,\mathrm{mV}, 400\,\mathrm{mV}, 700\,\mathrm{mV}\}$ for the 5PM and $V_G = 0.4\,\mathrm{V}$ and $V_{BN} = 1\,\mathrm{V}$ as an illustrative example for the 6PM version. In

Fig. 3.15, a comparison between the 5PM/6PM ACM model, the UTSOI2 model and measurement is presented. The relative error between the model and measurements is shown in the corresponding right y-axis of the curves. From the transistor output characteristics, we can derive the same conclusion as for the $(I_D(V_G))$. The model reproduces accurately the measurement data in saturation region with a relative error below 10% over the different inversion regions. In linear region, the model captures well the transistor behavior for low V_{GS}. Then, as V_{GS} increases, the relative error gets higher while the shape of the curve is well captured and the absolute difference is low. The body-bias parameter is implemented to compare the transistor description with measured results in presence of body voltage $V_{BN} = 1\,\mathrm{V}$ as an illustrative example. As shown in Fig. 3.15.d, the model captures well the effect of the body in reducing the threshold voltage and the obtained results are in good agreement with the measurements.

The 5PM/6PM model offers a good approximation of the transistor's behavior across all regions and regimes, as shown in Fig. 3.14 and Fig. 3.15. The observed differences with respect to the complete UTSOI2 model and measurements are due to other short-channel effects that have not been taken into account to keep the simplicity of the model. In fact, the carrier mobility reduction dominates the SCEs for transistors operating in linear regime (Galup-Montoro & Schneider, 2007).

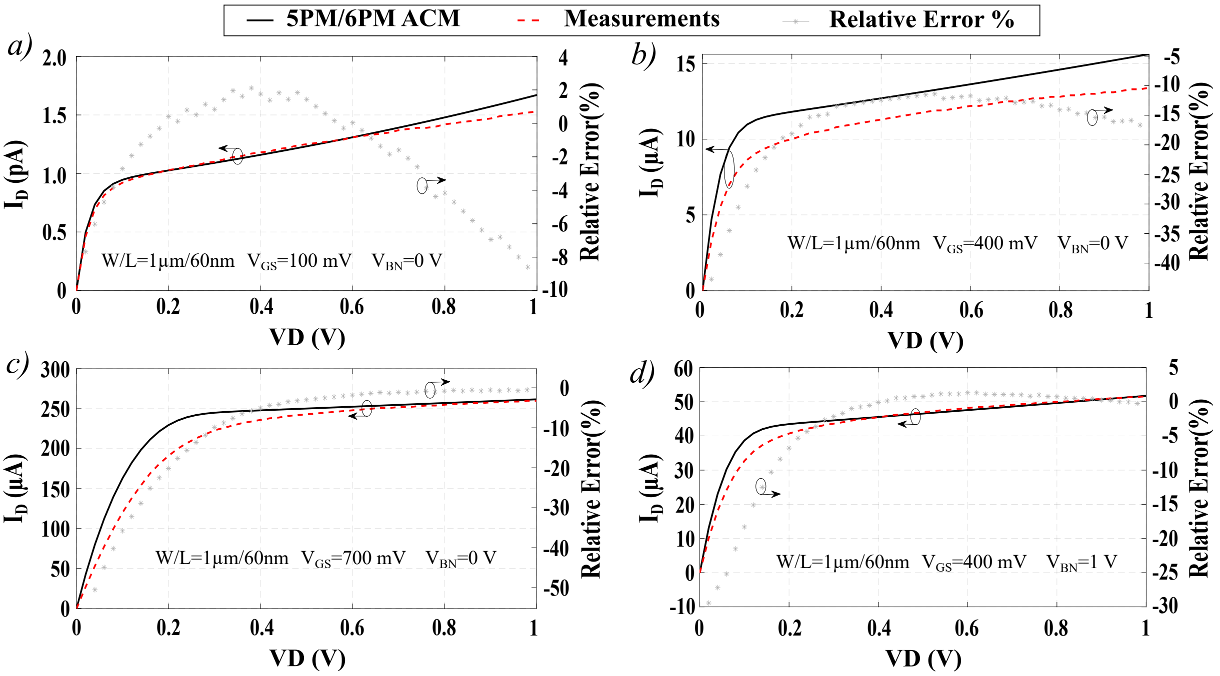


Figure 3.15: $I_D - V_D$ Output characteristics for a NMOS LVT *FD-SOI* transistor with $W/L = 1\mu m / 60$ nm for different V_{GS} and body bias voltages VBN over the nominal dynamic of V_D.

3.3.5 Small-signal model

The expressions of the small-signal transconductances complete the 5PM/6PM model and bridges the gap between transistor level description and system level, allowing systematic design methodologies for ICs. Fig. 3.16 shows the equivalent quasi-static small-signal circuit to describe the MOSFET transistor and show the transconductances between different nodes that are linked through the expression of the drain current I_D as,

$$I_D = g_m v_G - g_{ms} v_S + g_{ds} v_D + g_{mb} v_B, \tag{3.30}$$

where g_m, g_{ms}, g_{ds} and g_{mb} are the gate, source, drain and bulk transconductances respectively, and v_G, v_S, v_D and v_B represent small variations in the gate, source, drain and bulk voltages, respectively. The transconductances are given by (3.31), (3.32), (3.33) and (3.34),

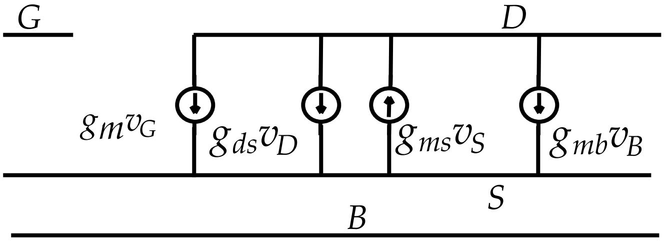


Figure 3.16: Small-signal equivalent circuit of a transistor.

$$g_m = \frac{\partial I_D}{\partial V_G}, \tag{3.31}$$

$$g_{ms} = -\frac{\partial I_D}{\partial V_S}, \tag{3.32}$$

$$g_{ds} = \frac{\partial I_D}{\partial V_D}, \tag{3.33}$$

$$g_{mb} = \frac{\partial I_D}{\partial V_B}. \tag{3.34}$$

The gate transconductance, g_m, is one of the main characteristics of the transistor since it is key for describing critical analog performance figures such as, voltage and current transfer functions, gain, noise expressions, filtering, and impedances. In the same way, the drain conductance is a key part of the small-signal description of the circuit, especially for small node technologies in which it is playing an important role and cannot be neglected anymore as done classically in the large technology nodes.

In addition, the accurate modeling of the second and third derivatives of I_D with respect to the gate voltage, denoted as g_{m2} and g_{m3} respectively, plays a crucial role in early-stage linearity studies during circuit design. Specifically, g_{m2} and g_{m3} are directly associated with the linearity performance, spanning from harmonic distortion to the compression point and intermodulation products in weak nonlinear circuits where the small-signal approximation holds (e.g., LNAs). As a design-oriented model, the proposed version, available in both bulk and *FD-SOI* variants, facilitates the derivation of simple expressions for transconductances and their derivatives. This provides designers with a comprehensive analytical toolkit that is both easy to handle and capable of supporting quick calculations or the development of systematic design algorithms

In this subsection, generic expressions of the first, second, and third-order derivatives of the current are derived as a function of the drain and source charge densities, taking into account the main short-channel effects covered by this model.

For X standing for one of the transistor terminals, and v_X for the corresponding potential normalized by the thermal voltage ϕ_T, a generic expression of the first derivative of the inversion factor i_D can be expressed as (3.35).

$$g_X = \frac{\partial i_D}{\partial v_X} = \frac{2\left(1+q_s\right)\,\frac{\partial q_s}{\partial v_X} - 2\left(1+q_d\right)\,\frac{\partial q_d}{\partial v_X} - i_d\,\zeta\left(\frac{\partial q_s}{\partial v_X} - \frac{\partial q_d}{\partial v_X}\right)}{1+\zeta\left(q_s - q_d\right)}, \tag{3.35}$$

where $\partial q_s/\partial v_X$ and $\partial q_d/\partial v_X$ are the charge density derivatives expressed as,

$$\frac{\partial q_{s(d)}}{\partial v_G} = \frac{1}{n}\frac{q_{s(d)}}{1+q_{s(d)}}, \tag{3.36}$$

$$\frac{\partial q_s}{\partial v_{D(S)}} = \frac{\sigma}{n}\frac{q_s}{1+q_s}, \tag{3.37}$$

$$\frac{\partial q_d}{\partial v_{D(S)}} = \left(\frac{\sigma}{n} - 1\right)\frac{q_d}{1+q_d}. \tag{3.38}$$

Considering the gate transconductance, $X = G$ and denormalizing the current and voltage, the g_m expression, valid in all regimes and all regions can be derived as (3.39).

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{I_S}{\phi_T} g_G = \frac{I_S}{n\phi_T}\frac{2(q_s - q_d) - i_D\,\zeta\left(\frac{q_s}{1+q_s} - \frac{q_d}{1+q_d}\right)}{1+\zeta\left(q_s - q_d\right)}. \tag{3.39}$$

Correspondingly, by denormalizing the current and voltage and setting $X = D$, the expression for g_{ds} can be derived, which is valid in all regimes and regions as,

$$g_{ds} = \frac{I_S}{n\phi_T}\frac{\left(2(q_S\sigma - q_d(\sigma - n)) - i_d\zeta(\sigma\frac{q_s}{(1+q_s)} - (\sigma - n)\frac{q_d}{(1+q_d))}\right)}{1+\zeta(q_s - q_d)}. \tag{3.40}$$

To account for the significant impact on the device's output impedance, the g_{ds} model's accuracy was tested at different bias points, to capture the variation in inversion regions. Fig. 3.17 displays the comparison results for a NMOS transistor with $L = 60$ nm. The relative error of the 5PM/6PM analytical model was computed with respect to the measurements and shows acceptable estimation especially for V_D close to half-dynamic (0.3 V $<V_D<$0.7 V) that is interesting for design. The shape of the g_{ds} variation is well-captured at different bias voltages, particularly in the saturation region, where the output conductance agrees well with the measurements. This enables designers to swiftly and accurately determine the initial sizing of circuit operation points using a simple equation.

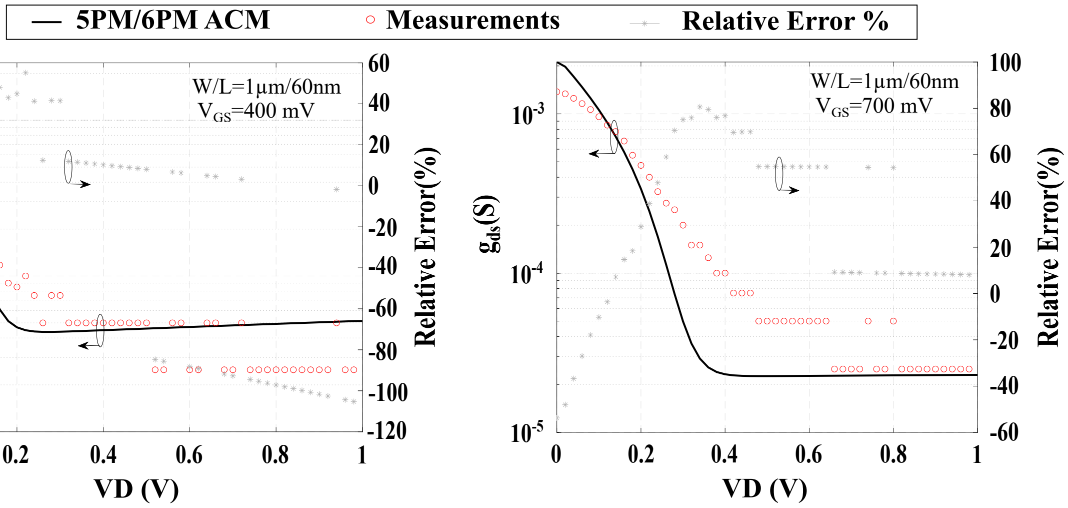


Figure 3.17: output conductance g_{ds} as function of V_{DS} for $V_{GS} = 400\,\text{mV}$ and $V_{GS} = 700\,\text{mV}$.

The current efficiency g_m/I_D of the transistor that define the operation region of the device, can also be derived as function of the charge densities as (3.41).

$$\frac{g_m}{I_D} = \frac{1}{n\phi_T}\left(\frac{2}{2+q_s+q_d} - \frac{q_s - q_d}{(1+\zeta(q_s-q_d))(1+q_s)(1+q_d)}\right). \tag{3.41}$$

Similarly, the generic expression of the second derivative can be easily derived as,

$$g_{X2} = \frac{\partial^2 i_D}{\partial {v_X}^2} = \frac{2\left(\frac{\partial q_s}{\partial v_X}\right)^2 + 2\left(1+q_s\right)\frac{\partial^2 q_s}{\partial {v_X}^2} - 2\left(\frac{\partial q_d}{\partial v_X}\right)^2}{1+\zeta\left(q_s-q_d\right)} - \frac{\left(2\left(1+q_d\right)\frac{\partial^2 q_d}{\partial {v_X}^2} - \zeta\left[g_X\left(\frac{\partial q_s}{\partial v_X} - \frac{\partial q_d}{\partial v_X}\right) + i_D\left(\frac{\partial^2 q_s}{\partial {v_X}^2} - \frac{\partial^2 q_d}{\partial {v_X}^2}\right)\right]\right)}{1+\zeta\left(q_s-q_d\right)}, \quad (3.42)$$

where,

$$\frac{\partial^2 q_{s(d)}}{\partial {v_G}^2} = \frac{1}{n^2 q_{s(d)}(1+q_{s(d)})^3}. \quad (3.43)$$

Hence, by referring to the gate node, the current second derivative g_{m2} can be expressed as,

$$g_{m2} = I_S(n\phi_T)^2 \frac{2q_s^2 + q_s(1+q_s)^2 - 2q_d^2 + q_d(1+q_d)^2}{(1+\zeta(q_s-q_d))^2} - \frac{\zeta n g_G(q_s-q_d) + i_D(q_s^3 - q_d^3 + 3q_s^2 - 3q_d^2)}{(1+\zeta(q_s-q_d))^2}. \quad (3.44)$$

For the third order derivative, the generic expression can also be driven following the same procedure,

$$g_{X3} = \frac{\partial^3 i_D}{\partial {v_X}^3} = \frac{6\frac{\partial q_s}{\partial v_X}\frac{\partial^2 q_s}{\partial {v_X}^2} + 2\left(1+q_s\right)\frac{\partial^3 q_s}{\partial {v_X}^3} - 6\frac{\partial q_d}{\partial v_X}\frac{\partial^2 q_d}{\partial {v_X}^2} - 2\left(1+q_d\right)\frac{\partial^3 q_d}{\partial {v_X}^3}}{1+\zeta\left(q_s-q_d\right)} - \frac{\zeta\left[g_{X2}\left(\frac{\partial q_s}{\partial v_X} - \frac{\partial q_d}{\partial v_X}\right) + 2g_X\left(\frac{\partial^2 q_s}{\partial {v_X}^2} - \frac{\partial^2 q_d}{\partial {v_X}^2}\right) + i_D\left(\frac{\partial^3 q_s}{\partial {v_X}^3} - \frac{\partial^3 q_d}{\partial {v_X}^3}\right)\right]}{1+\zeta\left(q_s-q_d\right)}, \quad (3.45)$$

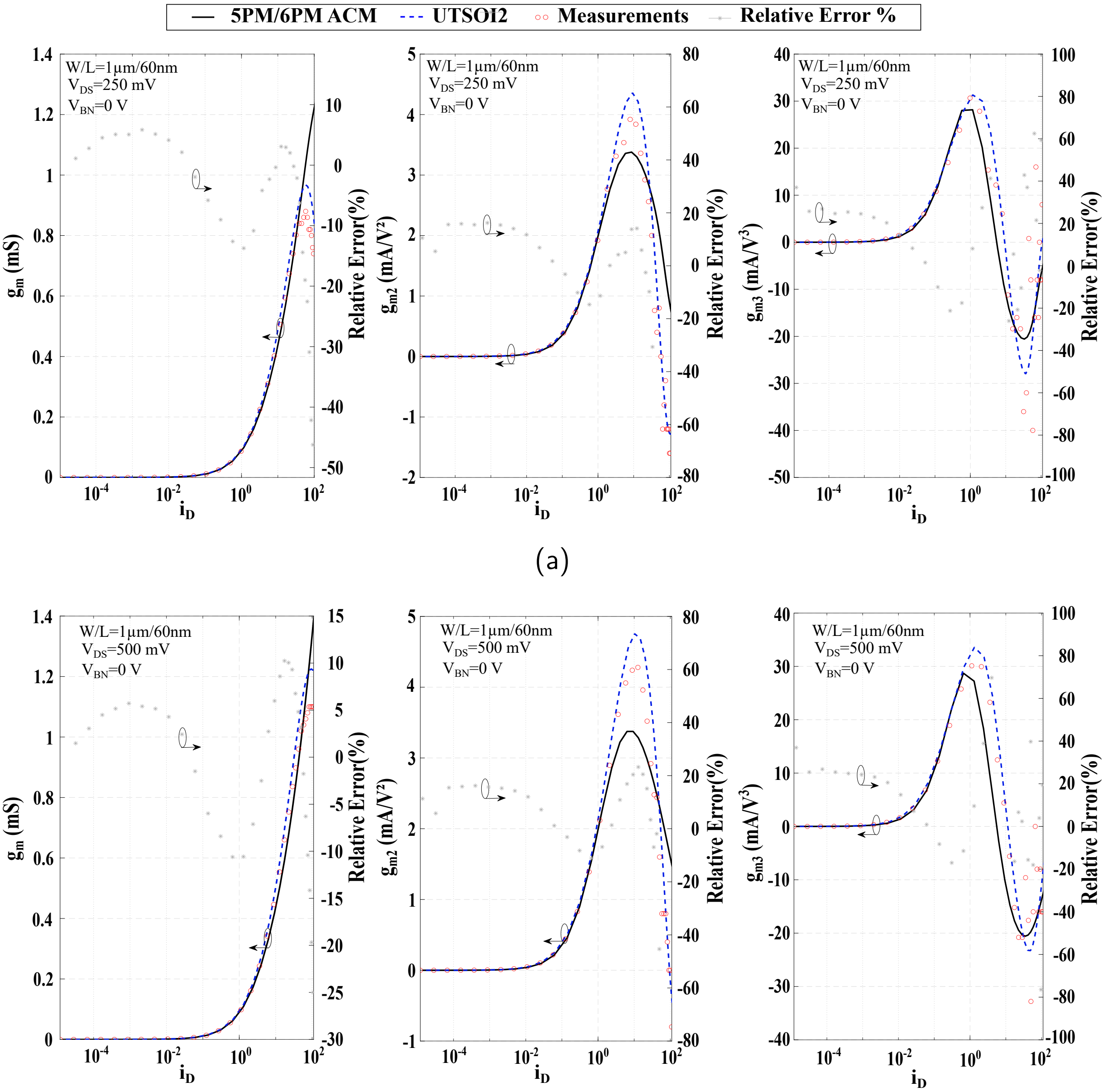
where,

$$\frac{\partial^3 q_{s(d)}}{\partial {v_G}^3} = \frac{1}{n^3}\frac{q_{s(d)}(1-2q_{s(d)})}{\left(1+q_{s(d)}\right)^5}. \quad (3.46)$$

By referring to the gate node, the current third derivative g_{m3} can be expressed as,

$$g_{m3} = \frac{I_S}{(n\phi_t)^3}\left\{\frac{\frac{2q_S}{(1+q_S)^3} - \frac{2q_D}{(1+q_D)^3} - \zeta n^2 g_{G2}\left(\frac{q_S}{1+q_S} - \frac{q_D}{1+q_D}\right)}{1+\zeta\left(q_S-q_D\right)}\right\} - \frac{\zeta\left[2ng_G\left(\frac{q_S}{(1+q_S)^3} - \frac{q_D}{(1+q_D)^3}\right) + i_D\left(\frac{q_D(1-2q_D)}{(1+q_D)^5} - \frac{q_D(1-2q_D)}{(1+q_D)^5}\right)\right]}{1+\zeta\left(q_S-q_D\right)}. \quad (3.47)$$

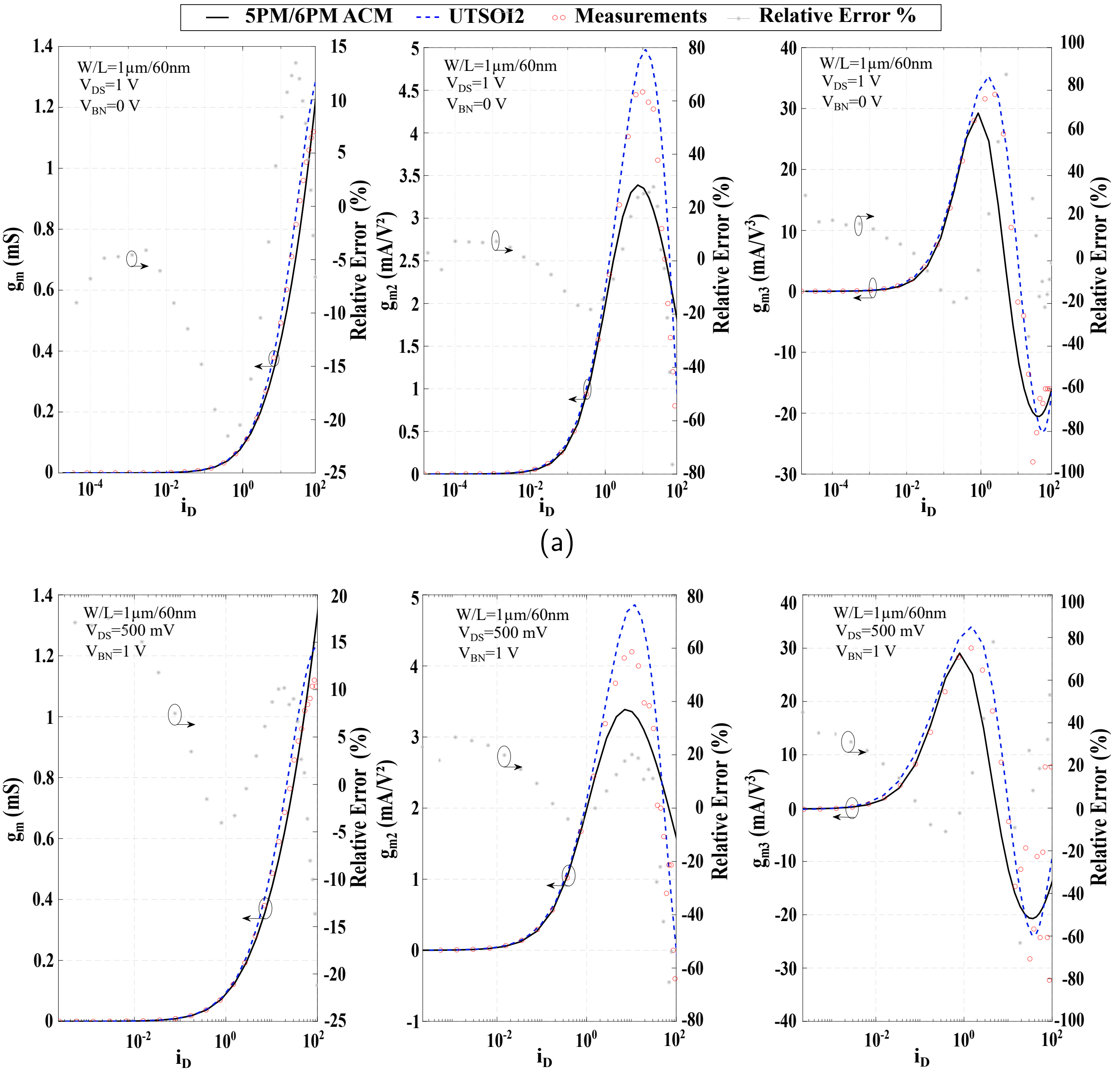
The analytical drain current's derivative equations are verified and compared to the measured characteristics. The different order derivatives g_m, g_{m2} and g_{m3} were considered concerning the gate voltage ((3.39), (3.44), (3.47)). The model's accuracy is tested for different bias points ($V_{DS} = 250$ mV, 500 mV, 1 V) to capture the variation with the saturation regions since the small-signal quantities will be implied in some design methodologies targeting simple and fast sizing of circuits such as amplifiers. It is important for



(a)

(b)

Figure 3.18: g_m, g_{m2} and $g_{m3} - i_D$ for a NMOS LVT *FD-SOI* transistor with $W/L = 1\mu\text{m}/60$ nm for different V_{DS} over the different inversion regions: a. $V_{DS} = 250$ mV, $V_{BN} = 0$V b. $V_{DS} = 500$ mV, $V_{BN} = 0$V.



(a)

(b)

Figure 3.19: g_m, g_{m2} and $g_{m3} - i_D$ for a NMOS LVT *FD-SOI* transistor with $W/L = 1\text{µm}/60\text{ nm}$ for different V_{DS} and body bias voltages VBN over the different inversion regions: a. $V_{DS} = 1$ V, $V_{BN} = 0$ V b. $V_{DS} = 500$ mV, $V_{BN} = 1$ V.

these kind of circuits to have a first approximation that is close to the reality using simple and intuitive equations. This allows the designers to tune specifically a parameter to improve the performance in a comprehensive way thanks to the detailed analytical derivation and the accurate device description. Fig. 3.18 and 3.19 display the comparison results for the transistor with $L = 60\,\text{nm}$. The 5PM/6PM analytical model's relative error with respect to the measurements is computed and shown in the right y-axis. The current derivatives are plotted with respect to the inversion coefficient (normalized drain current) i_D that is directly linked to the inversion region. As shown in Fig. 3.18 and 3.19, the shape of all the derivations is well captured by the model for different bias conditions including the effect of the body bias voltage (Fig. 3.19.b). For the transconductance g_m, which is critical for many analog performances as a first order parameter, a maximal relative error of 15% is noticed with respect to the measurements with very small deviation in weak to moderate inversion regions ($i_D < 10$) that are interesting for low power design. Also, the g_{m2} and g_{m3} are well estimated in the different inversion regions especially the linearity sweet spot for which the $g_{m3} = 0$ is well approximated by the model.

The complete procedure of the DC and small-signal set of equations solving for the transistor description is detailed through the flow-chart shown in Fig. 3.20.

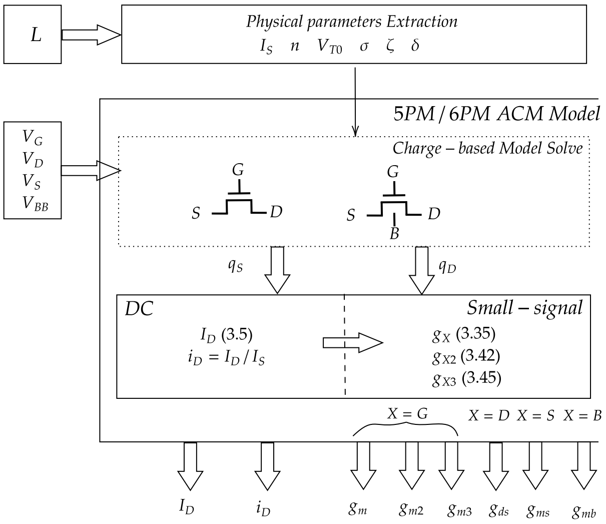


Figure 3.20: flow diagram of the complete DC and small-signal algorithm.

In the context of analog and RF design methodologies targeting to investigate the linearity behavior of a circuit and model analytically the nonlinearity effects, simple equations can be derived for the harmonic distortion by considering the non-linearity of I_D at constant drain voltage (Chicco et al., 2019), (Silveira & Reyes, 2023). For a sinusoidal input signal of amplitude A_0 the second and third harmonic distortion terms can be expressed as function of the derivatives of the current as,

$$HD_2 = |\frac{2\ A_0\ g_{m2}}{8\ g_m + g_{m3}A_0^2}|, \tag{3.48}$$

$$HD_3 = |\frac{A_0^3 g_{m3}}{24 g_m + 3 g_{m3} A_0}|. \tag{3.49}$$

Employing the obtained analytical expressions for the different order current derivatives, the harmonic distortion quantities HD_2 (from 3.48) and HD_3 (from(3.49)) are computed and compared to characterization measurements and UTSOI2 simulations. The

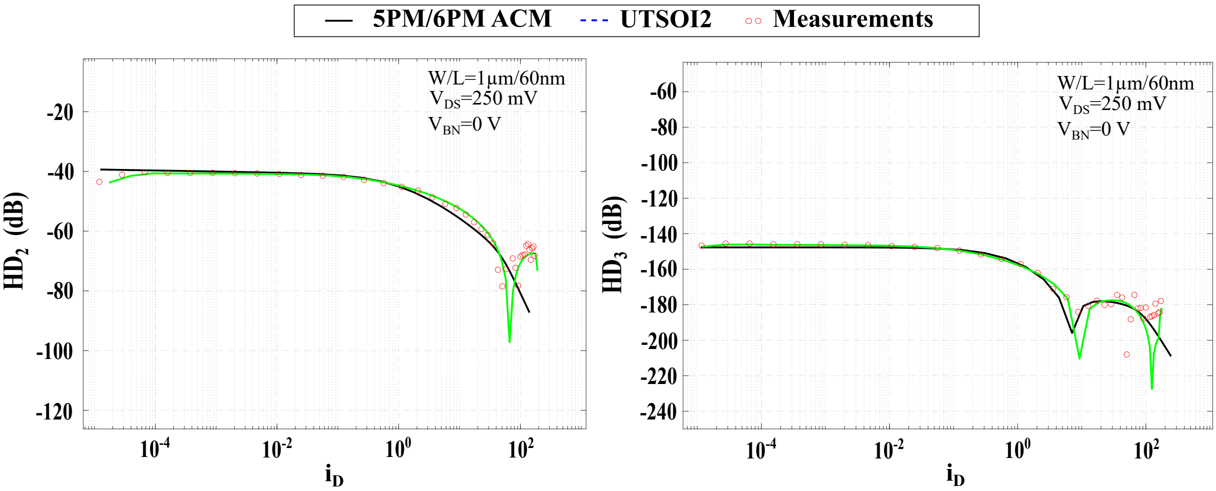


Figure 3.21: Second Harmonic distortion HD_2 (from 3.48) and third Harmonic distortion HD_3 (from(3.49)) for $V_{DS} = 250\,\text{mV}$, $V_{BN} = 0$ and $A_0 = 1\,\text{mV}$.

obtained results are shown in Fig. 3.21. Good agreement is shown between the proposed model, the PDK model and the measurements that opens the door for non-linearity improvement based design methodologies.

3.3.6 Conclusion

In this section a simple model of the N-channel and P-channel transistor is proposed based on the ACM formalism and set of equations. It simplifies some previous propositions introducing a large number of parameters and extend the simple design-oriented models based on 3 to 4 parameters to take into consideration critical short-channel effects such as the velocity saturation. The analytical expressions are compared to the model implemented in the PDK and measurements of a NMOS RF LVT 28 nm *FD-SOI* transistor. Besides, an additional parameter is implemented in this model to account for the effect of the body-bias voltage on SOI technologies. Both versions of the model, that is, the 5-parameter and the 6-parameter, are compared with measured results to validate their accuracy. The comparison results show that the proposed models approximate well the simulated and measured values of the transistor main characteristics, the transconductance, their derivatives and the conductance. This effective approximation, achieved through simple equations, enables designers to rapidly establish their initial design points via manual calculations for a set of specifications. Subsequently, a quick fitting step is employed to enhance the accuracy of the results. The implementation of the 5PM/6PM is simpler than a state-of-the-art 7-parameter version of ACM (Pino-Monroy et al., 2022). In fact, the inclusion of the saturation region is operated through the charge densities definition by modifying the UCCM equations, which avoids the use of a fitting function on the drain voltage to model a smooth transition between linear and saturation regions (Neto, Bouchoucha, et al., 2023). In addition, one simple equation for the current and its derivatives valid in all region is presented preventing the use of i_D and i_{Dsat} separately to address linear and saturation regions.

3.4 Examples of design methodologies for LNA design

In this thesis we propose an analytical design methodology based on the design-oriented model, presented in the previous section. Compared to previous analytical methodologies, by using our proposed model we have the advantage of the inclusion of the transistor behavior dependency on the drain voltage together with the main short-channel effects in the different inversion regions. The methodology is conceptually depicted in Fig. 3.22. The illustrative chart Fig. 3.22 details the steps of this general method which allows to analytically design a LNA but can be adapted to any analog/rf circuit. First, depending on the application and the targeted frequency band, the potential architecture is selected following the method applied for wideband sub-6GHz LNAs presented in chapter. 2. In a second step, we adapt the design-oriented model to the used technology by extracting the 5/6 parameters. The LNA architecture is then analytically described through the derivation of the main performance expressions. In this step, the small-signal model equations are used to bridge the gap between LNA performance equations and the transistor inversion coefficient that can be used as a main design parameter. This parameter is directly linked to the inversion region definition and the g_m/I_D transistor efficiency factor. The fourth step consists in building a simple exploration algorithm based on a reduced number of variables and a set of equations that can be easily analyzed. The designer can navigate in the design space and explore different trade-offs to optimize the working points and the inversion coefficient. A verification loop based on simulations using the PDK models completes the pre-sizing analytical steps in order to optimize the circuit for the targeted specifications.

In this section, we apply the generic steps described in Fig. 3.22 on simple LNA topologies such as the resistive feedback common-source (R-feedback) and the common-gate (CG) LNAs. Detailed analytical derivation of the circuits is provided. The proposed model is used to describe the transistors and allows to use the inversion coefficient i_D as a design variable to explore the design-space. Sub-mW low-power applications at 2.4 GHz are targeted. As it will be shown, analytical performance estimations are compared with the PDK simulations to validate the efficiency of the methodology.

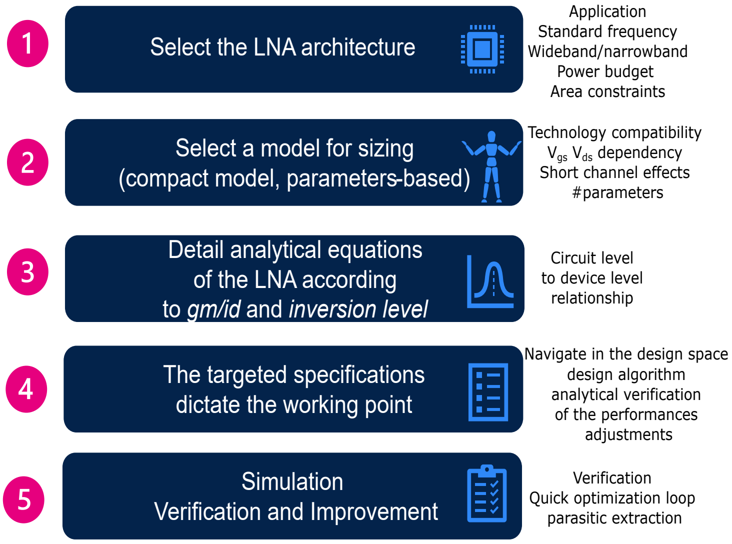


Figure 3.22: Illustrative flow chart for LNA design based on design-oriented model.

3.4.1 R-feedback LNA

Analytical description

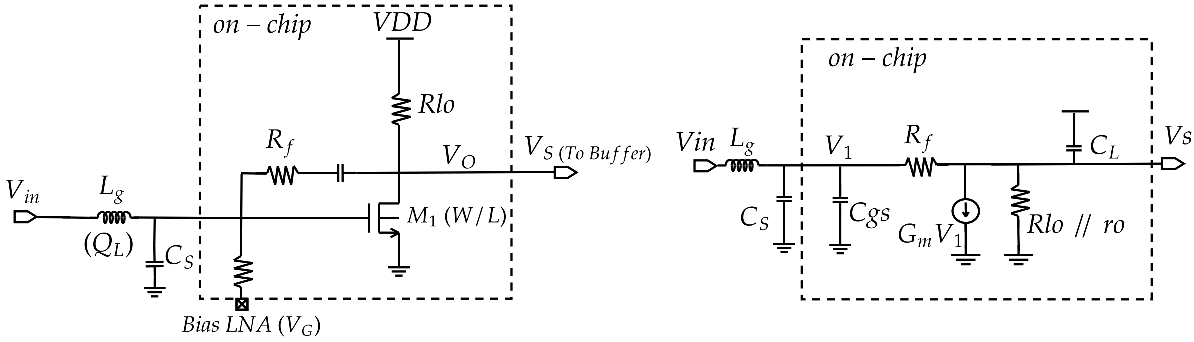
The basic architecture of the R-Feedback LNA is shown in Fig. 3.23.a. It is composed of a NMOS transistor M_1, a load resistor R_{lo} and a feedback resistor R_f. This topology can be described through a set of performance equations based on the small-signal equivalent circuit shown in Fig. 3.23.b. The NMOS is represented by the DC-mode equivalent voltage induced current source characterized by the transconductance g_m and a parallel resistor r_o with equivalent admittance equal to the conductance g_{ds}. The gate voltage is denoted V_1 and the drain voltage, which is the output voltage, is denoted by V_S. The equivalent load resistor R_L corresponds to R_{lo} in parallel with r_o.

Whereas the feedback resistor, R_f is mainly used to synthesize a real part in the input impedance, an $L-$type matching network composed of L_g and C_S is added to null the imaginary part while controlling the input Q factor, Q_{IN}. The input impedance of the circuit, Z_{IN} is given by:

$$Z_{IN} = L_g s + \left(\frac{1}{(C_{GS} + C_S)s} // Z_P \right), \qquad (3.50)$$

where Z_P in the input impedance seen at the gate due to the resistive feedback which is expressed as follows:

$$Y_P = \frac{1}{Z_P} = \frac{1}{R_P} + C_P s, \qquad (3.51)$$



(a) (b)

Figure 3.23: R-feedback LNA with its small-signal equivalent circuit.

where

$$R_P = \frac{1 + \left(\frac{f_0}{f_c}\right)^2}{\frac{1+G_mR_0}{R_0+R_f} + \frac{1}{R_f}\left(\frac{f_0}{f_c}\right)^2}, \tag{3.52}$$

and

$$\frac{1}{C_P} = \left(1 + \frac{R_f}{R_L}\right)^2 \frac{1 + \left(\frac{f_0}{f_c}\right)^2}{C_L(G_mR_f - 1)}, \tag{3.53}$$

with

$$R_L = \frac{R_{lo}r_o}{R_{lo} + r_o}, \tag{3.54}$$

and

$$f_c = \frac{R_L + R_f}{2\pi R_L R_f C_L}. \tag{3.55}$$

For an operating frequency, f_0, well bellow the cutting frequency, f_c (i.e $f_c > 3f_0$), we can simplify R_P and C_P as,

$$R_P = \frac{R_L + R_f}{1 + G_mR_L}, \tag{3.56}$$

and

$$C_P = \frac{R_L^2C_L(G_mR_f - 1)}{(R_L + R_f)^2}, \tag{3.57}$$

with G_m the transconductance of the MOS.

Defining Q_P as follows:

$$Q_P = R_PC_T\omega_0, \tag{3.58}$$

with

$$C_T = C_{GS} + C_S + C_P, \tag{3.59}$$

the matching conditions are,

$$\Re(Z_{IN}) = R_S = \frac{R_P}{(1+Q_P^2)}, \tag{3.60}$$

$$\Im(Z_{IN}) = 0 = L_g s + \frac{Q_P^2}{C_T s(1+Q_P)^2}, \tag{3.61}$$

with R_S the impedance of the source generator which, for a LNA, corresponds to the antenna impedance.

The total voltage gain can be defined according to the operating frequency and the cutting frequency as,

$$|G_o| = \left|\frac{V_S}{V_{in}}\right| = \frac{|G_T|}{\sqrt{\left(1+\left(\frac{f_0}{f_c}\right)^2\right)}}, \tag{3.62}$$

where

$$|G_T| = |G_v|Q_{IN} = \frac{(G_m R_f - 1)R_L}{(R_0 + R_f)}\sqrt{1+Q_P^2}, \tag{3.63}$$

with $Q_{IN} = V_1/V_{in}$ the input Q factor which, for $f_0 << f_c$, can be simplified from (3.60) and (3.56) as,

$$Q_{IN} = \sqrt{1+Q_P^2} = \sqrt{\frac{R_L + R_f}{R_S(1+G_m R_L)}}. \tag{3.64}$$

Hence, by introducing the series inductor L_g the quality factor expression becomes,

$$Q_P = \frac{L_g w}{R_{in}}. \tag{3.65}$$

As for the gain, the noise factor F in matched conditions depends on Q_{IN} and can be expressed as,

$$F = 1 + \frac{4\left(\frac{R_f}{Q_{IN}^2} + R_S\right)^2}{Q_{IN}^2 G_m R_S \left[\frac{R_f}{Q_{IN}^2} + R_S + \frac{G_m R_S R_f R_L)}{R_f + R_L}\right]^2}\left[\gamma + \frac{1}{G_m R_L} + \frac{\left(1 + \frac{Q_{IN}^2 G_m R_S R_f}{R_f + Q_{IN}^2 R_S}\right)^2}{G_m R_f}\right], \tag{3.66}$$

where γ is the MOS transistor excess noise factor. Note that the input quality factor improves both gain and noise figure, we can define a minimum gain G_{vmin} and a maximum noise factor f_{max} that are the performance of the on-chip circuit without the effect of the $L-C$ matching network as,

$$G_{vmin} = \frac{(G_m R_f - 1)R_L}{(R_L + R_f)}, \tag{3.67}$$

and,

$$F_{max} = 1 + \frac{(1 + G_m \ \ R_S)^2 \, R_f}{R_g \ \ (1 - G_m \ \ R_f)^2} + \frac{\gamma \, G_m \ \ (R_S + R_f)^2}{R_S \ \ (1 - G_m \ \ R_f)^2} + \frac{(R_S + R_f)^2}{R_S \ R_{lo} \, (1 - G_m \ \ R_f)^2} \tag{3.68}$$

The linearity performances of the on-chip circuit can be evaluated through the input referred third intercept point IIP_3 at V_1. The equivalent V_{IIP3} voltage can be approximated using the transistor metrics by,

$$V_{IIP3_{on-chip}} = 2\sqrt{\frac{2G_m}{G_{m3}}}. \tag{3.69}$$

While considering the total circuit, the linearity is degraded as,

$$V_{IIP3} = \frac{2}{Q_{IN}}\sqrt{\frac{2G_m}{G_{m3}}}. \tag{3.70}$$

Design Methodology

The design methodology relies on the analytical expressions of the LNA main characteristics shown in Section 3.4.1 together with the 5/6−parameter transistor equations that capture the device behavior across all regimes while varying V_{DS}. Considering linearity, gain, noise figure and power budget requirements, the strategy allows for navigation in the design space until reaching the optimal component sizes and working points. In the context of low power application, sub−1 mW operation is targeted. For a minimum intrinsic gain $G_{vmin} = 10$ and maximal noise figure F_{max} close to 2 (before improvement using Q_{IN}), the resistances values and the transistor sizes are determined for a maximum of IIP_3. The complete flow chart of the design methodology is shown in Fig. 3.24. Actually, with the current constraint, a direct relationship can be derived between R_{lo} and the drain voltage V_{DS} as,

$$R_{lo} = \frac{V_{DD} - V_{DS}}{I_D}. \tag{3.71}$$

On the other hand, the IIP_3 is directly related to G_m and G_{m3} (3.69), while the gain (3.67) and noise figure (3.68) set conditions on G_m, R_f and R_L. In this section, the analytical expressions derived from the 5PM/6PM model and shown in Section 3.3.2, are used to link the transistor parameters G_m (3.39), G_{ds} (3.40), G_{m3} (3.47) and G_m/I_D (3.41) to the inversion level i_D taking into account the dependency on V_{DS}, which, in turn, allows a direct extraction of the optimal design parameters V_{GS} and W. As a result, the IIP_3 can be expressed as function of i_D for the selected drain voltage and transistor length as illustrated in Fig. 3.25.a. In the second step of this methodology, the linearity requirements sets the inversion coefficient and the efficiency factor of the common source

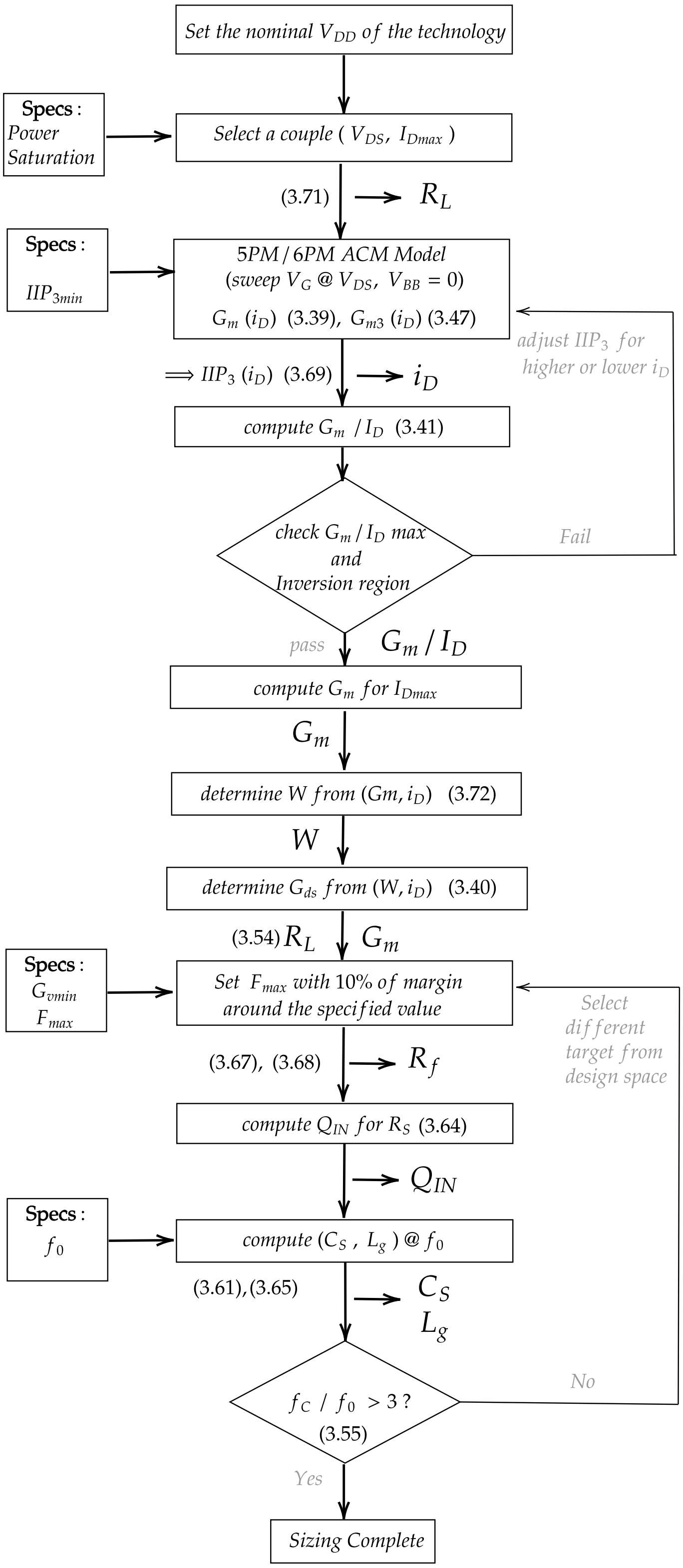


Figure 3.24: Flow chart of the complete design methodology of the R-feedback LNA.

transistor M_1 as shown in Fig. 3.24. This is directly related to the g_m/I_D efficiency factor that is independent from bias and size conditions (3.41). Under the power consumption constraint, the adequate G_m is then determined based on the Gm/ID factor which gives a preliminary size W of M_1 as,

$$W = \frac{I_D}{I_{S1\mu m} i_D} (\mu m), \tag{3.72}$$

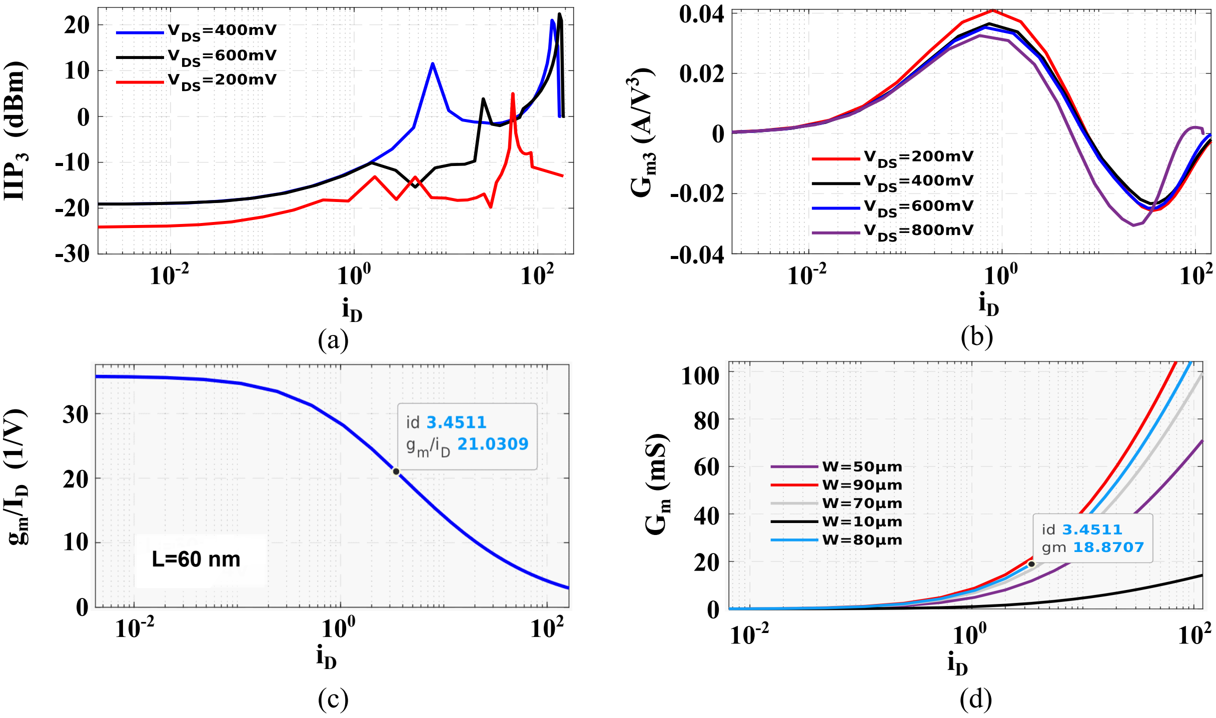
with $I_{S1\mu m}$ is the specific current extracted for the unit transistor with W=1μm and $L = 60\,\text{nm}$. At this step, the load resistance R_L is computed and for the gain and noise requirements the feedback resistance R_f is directly determined. However, in orger to explore different design possibilities possible resistive feedback values are analyzed for the required G_{vmin} within a 10% tolerance range around the targeted F_{max}. This allows a design flexibility and the possibility to refine the choice of G_m.

For the matching network, the input impedance R_p is computed following (3.56). The value of the quality factor to match the LNA to $50\,\Omega$ is derived from (3.64). At the target working frequency $f_0 = 2\pi\omega_0$, the inductor L_g value is selected from (3.65). And the adequate parallel capacitance C_s completes the sizing for a given load capacitance. Then the cutoff frequency and the total gain are evaluated from (3.55) and (3.63) respectively and are compared to the specifications. This allows to rapidly decide on relaxing some constraints when no solution is found and repeat the procedure until the sizing is completed.

Design Cases

To demonstrate the efficiency of the model and its ability to deal with different drain voltages (which is appealing for ultra-low voltage design) three design case studies are described in this chapter. Thus, three different LNA designs with a V_{DS} of 200 mV, 400 mV and 600 mV while $V_{DSsat} = 160\,\text{mV}$ in the 28 nm *FD-SOI* CMOS technology with $V_{DD} = 1\,\text{V}$ and $L = 60\,\text{nm}$, are targeted. The corresponding circuits are denoted as circuit I, circuit II and circuit III respectively. To illustrate the methodology, the sizing procedure for circuit II is detailed in this section.

In this case study we target a power consumption of 0.9 mW, a gain higher than 20 dB with $NF < 2$ dB. Also, an $IIP_3 > -10$ dBm and a $f_c > 3\,\text{GHz}$ are required.
Thus, for $V_{DD} = 1\,\text{V}$ it follows that $I_{Dmax} = 0.9\,\text{mA}$ and $R_{lo} = 660\,\Omega$ (3.71).
The minimal IIP_3 requirement of $-10\,\text{dBm}$ sets the inversion level i_D, as shown in Fig. 3.25.a. For $IIP_3 = -8.7\,\text{dBm}$, $i_D = 3.45$ and the G_m/I_D factor that is independent on geometrical sizes is verified and equals $21\,V^{-1}$ as illustrated in Fig. 3.25.c.



(a) (b) (c) (d)

Figure 3.25: a. IIP_3 as function of i_D for different V_{DS},b. G_{m3} as function of i_D for $W = 1\,\mu$m and $L = 60\,$nm for different V_{DS}. c. g_m/I_D relationship for $L = 60\,$nm. d. G_m as function of i_D for different W at $V_{DS} = 0.4\,$V.

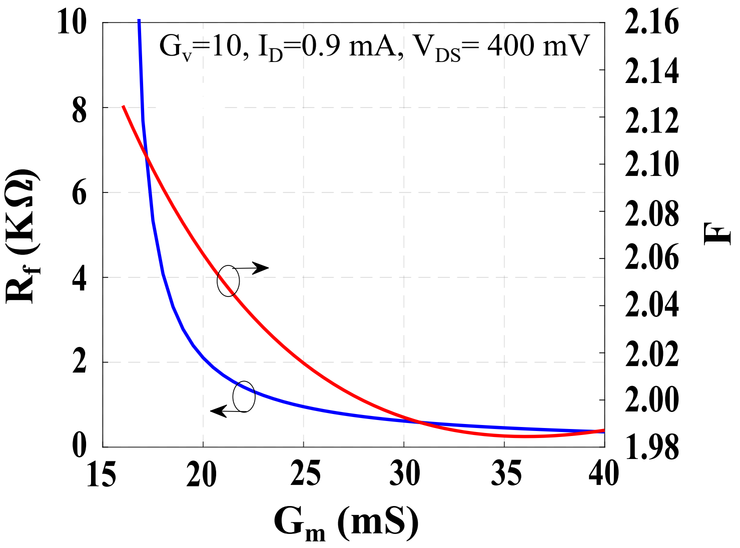


Figure 3.26: R_f and G_m for $G_V = 10$, $I_D = 0.9\,$mA and $V_{DS} = 0.4\,$V.

As a result, $G_m = 18.9\,$mS is selected for $W = 80\,\mu$m as shown in Fig. 3.25.d.

For an intrinsic voltage gain higher than 10 ($G_{vmin} = 10$) so that the total gain G_t could exceed 25 dB and a 10% variation of the maximal noise factor close to 2 (without the effect of Q_{IN}) will set the relationship between G_m and R_f as shown in Fig. 3.26

allowing to explore the design space. Selecting $G_m = 18.92\,\mathrm{mS}$ and $R_f = 2650\ \Omega$ results in an intrinsic gain $G_v = 10.2$ and $F = 2.089$. The feasibility of the obtained Gm/ID

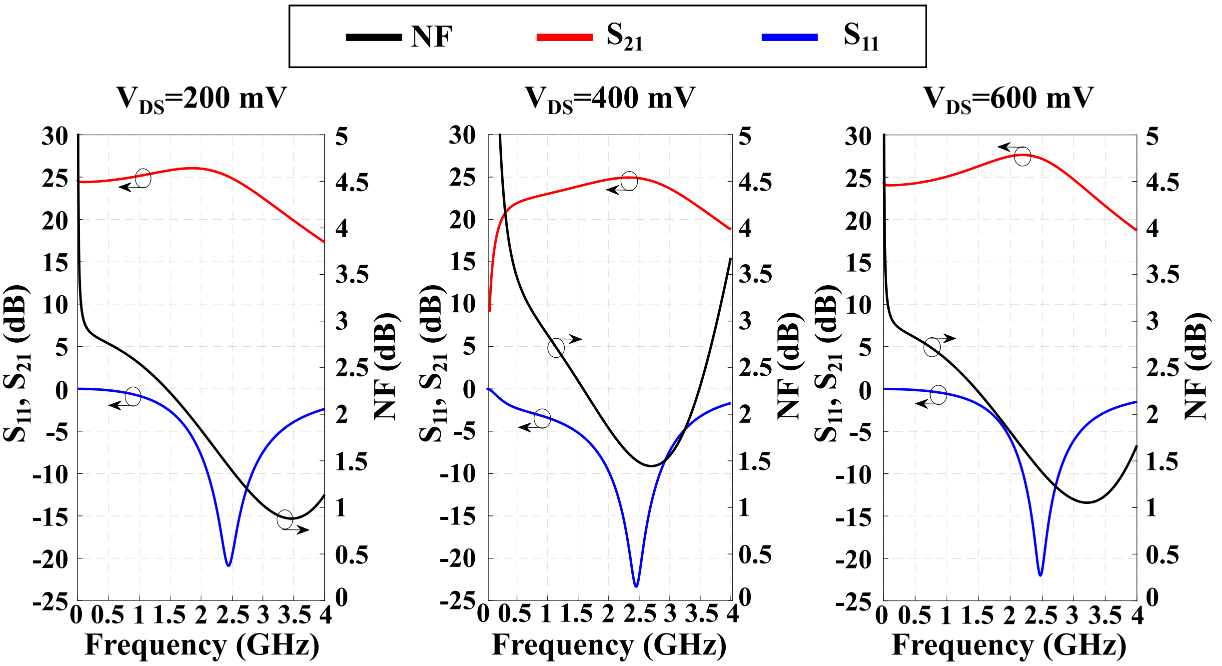


Figure 3.27: $UTSOI2$ simulation results of S_{21}, S_{11} and NF for V_{DS} = 200 mV, 400 mV and 600 mV over frequency with sizes from the design methodology.

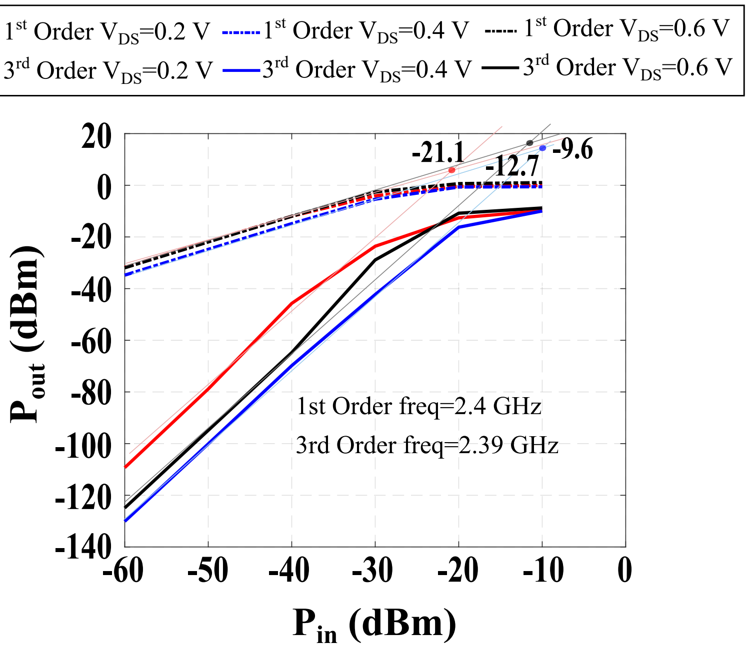


Figure 3.28: $UTSOI2$ simulation results for V_{DS} = 200 mV, 400 mV and 600 mV at 2.4 GHz with sizes from the design methodology.

Table 3.2: Component values for the three circuits with noise, gain and current requirements.

	Circuit I	Circuit II	Circuit III
V_{DS} (mV)	200	400	600
$Idmax$ (mA)	0.8	0.9	0.8
(Gvmin, Fmax)	(10,2)	(10,2)	(10,2)
R_{lo} (Ω)	1000	660	500
R_f (Ω)	1825	2650	5360
G_m (mS)	18.1	18.9	19.1
R_p (Ω)	147.2	248.5	555.5
Q_P	1.39	1.99	3.17
L_g (nH) (Q_L=23, 2.4 GHz)	4.6	6.6	5.8
C_S (pF)	0.22	0.34	0.32
G_T	19.4	22.7	28.8
G_m/I_D (1/V)	22.62	21	23.87
W (μm)	110	80	110

and the G_{m3} of 2.8 A/V^3 by the same transistor is verified and the LNA on chip sizing can be considered complete.

The input impedance is $R_p = 248.5\,\Omega$. Hence, the required quality factor Q_P of the input matching network is $Q_P = 1.99$. Then the inductor L_g and the capacitor C_s are derived at 2.4 GHz. The obtained values are $L_g = 6.6$ nH and $C_s = 0.34$ pF for a load capacitance $C_l = 0.1$ pF. The total gain G_T is computed and equals 22.7 which results in 27 dB for perfect matching without input attenuation.

For the three design cases, the sizing parameters and the analytical performance values are reported in Table. 3.2. The S parameters and total noise figure are shown in Fig. 3.27. The IIP_3 simulation results at 2.4 GHz are also shown in Fig. 3.28. Based on the design methodology and the 5PM/6PM model, our first analytical sizing using analytical calculations show good agreement with simulation results using the $UTSOI2$ (Poiroux, Rozeau, Scheer, Martinie, Jaud, et al., 2015) model of the technology. A comparison between analytical and simulated LNA performances are reported in Table. 3.3. As it is shown, the LNAs are well matched at the frequency of interest with good gain and bandwidth performance. The noise figure is optimized using the analytical constraints and the input matching network leading to good performances at the limited sub-1mW power budget. Also, the variation of the linearity performances through the drain voltage is captured. As it can be observed, low V_{DS} (0.2 V) results in poor linearity ($IIP_3 = -21.2$ dBm), for V_{DS} close to the half range dynamic (0.4 V) the linearity is optimized and the IIP_3 reaches -9.6 dBm. However, higher V_{DS} (0.6 V) and larger Q_{IN} push the transistor to early saturation since IIP_3 decreases to -12.7 dBm.

Table 3.3: Performance comparison between analytical method and simulation for the three circuits.

Performances	Circuit I	Circuit II	Circuit III
Analytical @ 2.4 GHz	$I_D = 0.8$ mA $G_T = 25.7$ dB NF < 1.5 dB $IIP_3 = -19$ dBm	$I_D = 0.9$ mA $G_T = 27.1$ dB NF < 1.5 dB $IIP_3 = -8.7$ dBm	$I_D = 0.8$ mA $G_T = 29.1$ dB NF < 1.5 dB $IIP_3 = -11$ dBm
Simulation @ 2.4 GHz	$I_D = 0.776$ mA $G_T = 24.9$ dB NF$= 1.42$ dB $IIP_3 = -21.1$ dBm	$I_D = 0.88$ mA $G_T = 25.6$ dB NF$= 1.5$ dB $IIP_3 = -9.6$ dBm	$I_D = 0.81$ mA $G_T = 28.4$ dB NF$= 1.39$ dB $IIP_3 = -12.7$ dBm

3.4.2 Common-Gate LNA

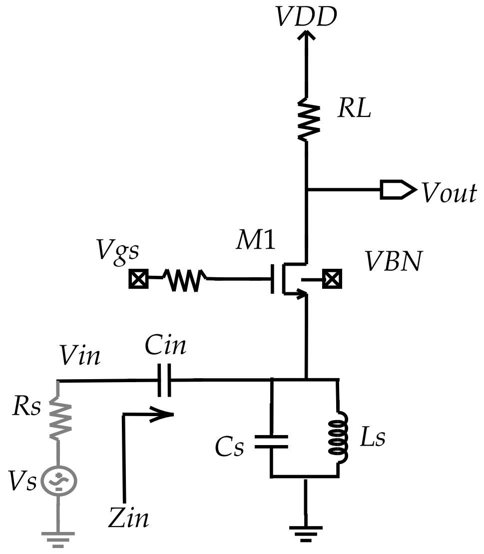


Figure 3.29: Simplified schematic of the CG LNA.

In order to further validate the proposed design-oriented model and its small-signal set of equations, a CG LNA circuit is designed in the 28 nm *FD-SOI* CMOS technology based on analytical equations followed by a comparison with the UTSOI2 PDK model. As it will be shown, the simplicity of the proposed design-oriented model allows us to analytically explore the LNA design space to find an optimum solution. Common-source-based LNA topologies have been used as demonstrators for other versions of the model (Bouchoucha et al., 2023; Bourdel et al., 2021; Liu et al., 2018), in this part the LNA shown in Fig. 3.29, consists in a single-stage common gate (CG) single-ended amplifier.

The CG transistor transconductance g_{m1} is set to match the real part of the input impedance, that can be expressed as,

$$Zin = \frac{1}{g_{m1} + \frac{1+L_s(C_s+C_{gs1})s^2}{L_S s}}, \tag{3.73}$$

to the source resistance $R_S = 50\ \Omega$. On the other hand, a degenerative LC network is inserted at the source node to cancel out the impedance imaginary part together with the effect of C_{gs1} at the desired frequency f_0. Finally, a load resistance sets the voltage gain, expressed as,

$$Av = R_L \frac{g_{m1}}{1 + R_L g_{ds1}}, \tag{3.74}$$

while maintaining enough headroom for the CG transistor and less impact on the noise figure NF. The noise figure NF considering the MOS transistor and Load resistor thermal noise sources is expressed as,

$$NF = 1 + \frac{\gamma}{R_s g_{m1}} + \frac{R_S}{R_L}(1 + \frac{1}{g_{m1} R_S})^2. \tag{3.75}$$

The noise figure under matching condition(Liu et al., 2009) can be simplified as,

$$NF = 1 + \gamma + \frac{4R_S}{R_L}, \tag{3.76}$$

where γ is the excess noise factor defined in (Cui et al., 2007). Finally, regarding the LNA linearity, the CG IIP_3 considering the non-linearity contribution from g_{m1}, that is, assuming small-signal operation and hence weak non-linearity conditions, is expressed as,

$$IIP_3 = 20 \log \left(\sqrt{\left| \frac{8 g_{m1}}{g_{m3}} \right|} \right). \tag{3.77}$$

As can be seen in equations (3.73)-(3.77), the small-signal performance of the CG LNA in Fig. 3.29 can be analytically expressed as a function of the transistor transconductance, g_{m1} (3.39), output conductance g_{ds1} (3.40), transconductance third-order non-linearity coefficient, g_{m3} (3.47), the transistor parasitic capacitances, and the value of the passive elements (resistors, capacitors and inductor) in the circuit. Using the proposed design-oriented model to bridge the gap between small-signal parameters and the transistor's dimensions and bias conditions, we can analytically evaluate equations (3.73)-(3.77) to find a solution to a given design target.

The M_1 transistor is designed in order to have a maximal g_{m1} slightly above 20 mS (up to 25 mS) to select a bias point as close as possible to the linearity sweet spot. In fact, in close proximity to the maximum g_{m1}, an inflexion point appears in the g_{m3} characteristic (Fig. 3.18) and it crosses 0 (the sweet spot), first in weak inversion, then in moderate to strong inversion regime. In this work, we take advantage of the accurate small-signal description of the transistor together with the 28 nm *FD-SOI* features (the body bias voltage) to finely tune the inversion coefficient in order to flatten the design space around the input matching points and target the highest linearity through the selection of minimal g_{m3} while consuming a limited power budget.

The circuit is designed at 2.4 GHz based on the small-signal characteristics from the model and a simple LUT to extract C_{gs1}. The transistor inversion coefficient i_D is selected as the design variable. Based on the design considerations and the analytical description in (3.74)−(3.77), the circuit sizes are obtained and reported in Table 3.4. The design method is similar to the R-feedback one presented in Section 3.4.1. The design space can be analytically explored thanks to the inversion coefficient i_D which is directly related to the overdrive voltage ($V_G - nV_S - V_T$). In effect, thanks to the UCCM equation solving with the 443 algorithm, the charge densities q_S and q_D are expressed as functions of the bias conditions. Correspondingly, using (3.5) and $i_D = I_D/I_S$, a direct relationship can be derived as function of the inversion-coefficient. $L = 2Lmin = 60\,\text{nm}$, for which the model was validated, is selected for high f_T and less variability and area trade-off.

Table 3.4: LNA component sizes for $V_{DD} = 1\,\text{V}$ and $f_0 = 2.4\,\text{GHz}$.

component	M1	RL	Cs	Ls	Cin
size	$75\mu m/60\ nm$	500 Ω	2.8 pF	1.5 nH	10 pF

In this example, the model accuracy to track the transistor performance variation as a function of the four terminals including the SOI-based technology is demonstrated. Applied to the LNA, two methods are shown to explore the bias voltage range and select the optimal operating point for the best linearity, power, noise and gain performance while controlling the input matching. In Fig. 3.30, the direct relationship between i_D and V_G and V_{BN} is shown. First, the transistor is biased for $V_{BN} = 0\,\text{V}$. The LNA performance variations at the matching frequency $f_0 = 2.4\,\text{GHz}$ are shown in Fig. 3.31.a from simulations using the UTSOI2 PDK and our ACM model based on equations (3.73)-(3.77). Setting $S_{11} < -10\,\text{dB}$ as matching condition, the design space is limited to 200 mV of gate voltage control (350 mV −550 mV). As expected, within this operation range, two perfect matching points can be selected ($g_{m1} = 20\,\text{mS}$) and also two local linearity sweet spots can be addressed. However, the power consumption varies through a very sharp slope. Moreover, a fast alteration between the maximum and minimum IIP_3 points

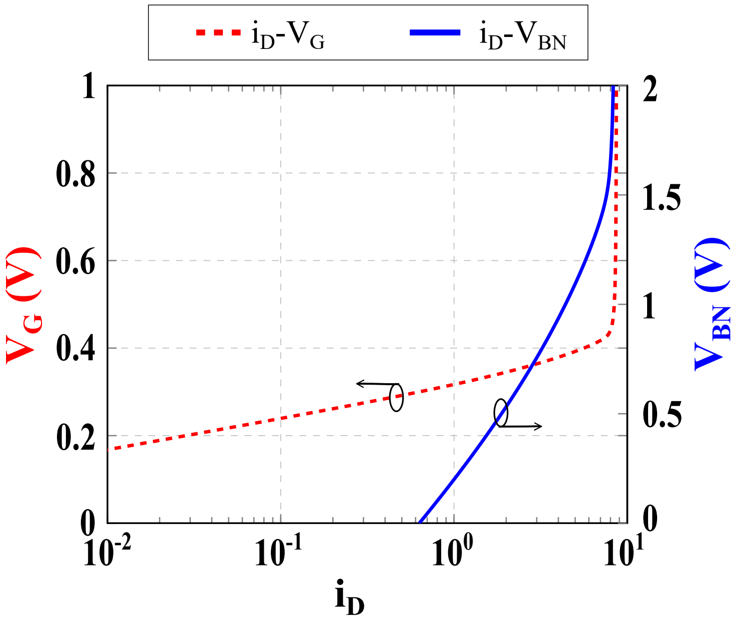
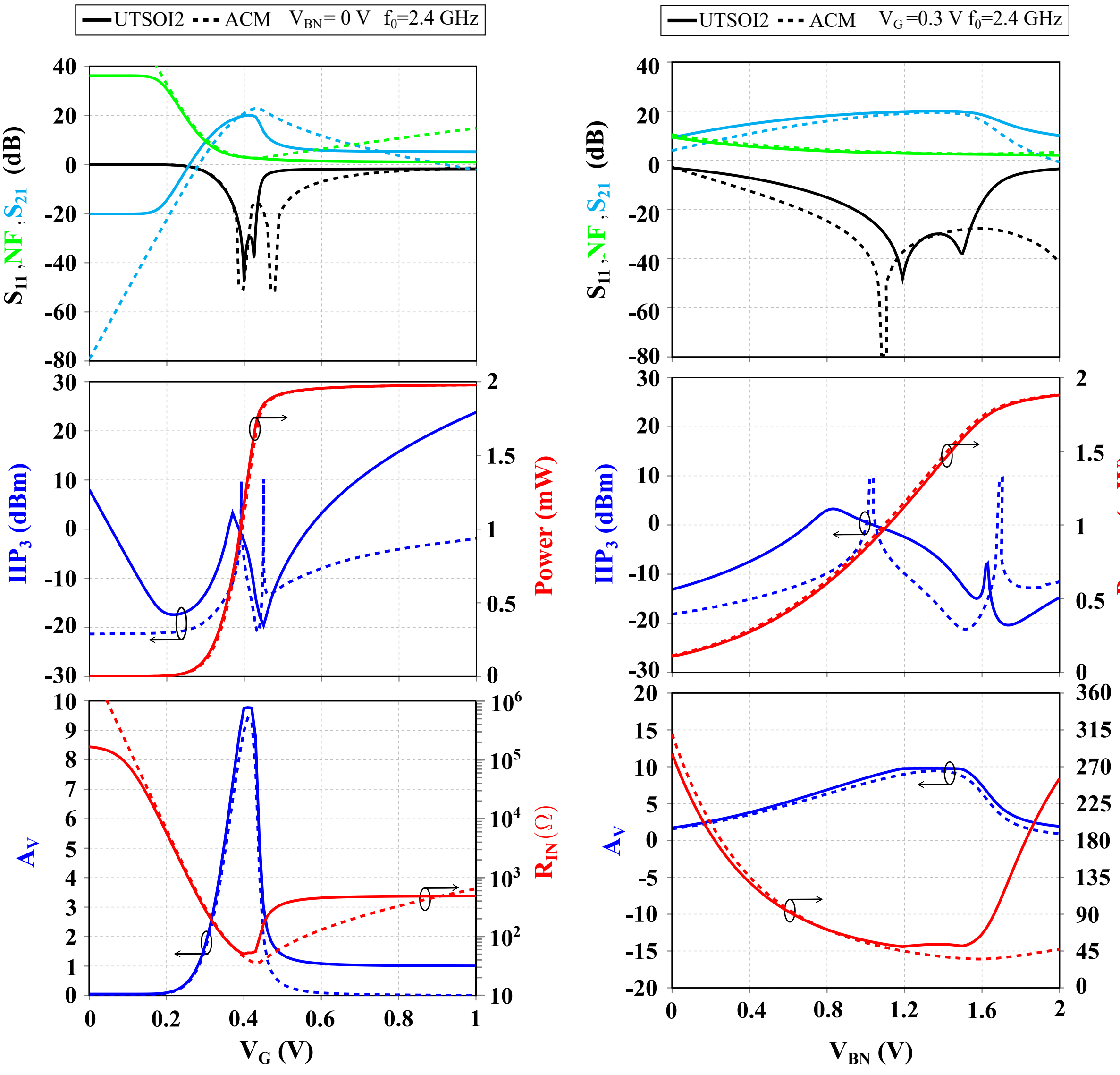


Figure 3.30: $V_G - i_D(V_{BN} = 0\,\mathrm{V})$ and $V_{BN} - i_D(V_G = 0.3\,\mathrm{V})$ for $V_{DS} = V_{DD} - R_L I_D$.

occurs within a few V_G millivolts for which 4 dB of gain and NF variations are noticed. The weak performance controlability together with the ACM model accuracy are validated when comparing the analytical results to the simulated results using the PDK UTSOI2 model as shown in Fig. 3.31.a.

The second alternative consists in exploring the same design space through the fine-control of the body bias voltage to tune the threshold voltage as in (3.24). Hence, the gate voltage is maintained constant at 300 mV for which the amplification operation starts. The LNA performance variations at $f_0 = 2.4\,\mathrm{GHz}$ are shown in Fig. 3.31.b. For the same matching criteria, the targeted design space is obtained through more than $1V$ tuning range. This allows to finely select the bias point for the maximum IIP_3 while maintaining good noise and gain results. In addition, different trade-offs can be easily addressed for a given power budget. As it is shown in Fig. 3.31, the proposed model, based on a simple set of DC parameters, accurately tracks the LNA RF performance variations over wide tuning ranges for both bulk ($V_{BN} = 0\,\mathrm{V}$) and SOI cases using an advanced technology such as the 28 nm CMOS *FD-SOI*. Asymptotic behavior of the IIP_3 sweet spots and S_{11} perfect matching are obtained with the analytical results since they are based on ideal calculations. In the real case, these values do not tend to infinite and achieve defined extrema as shown using the PDK simulations. The results obtained with the ACM model are in good agreement with the UTSOI2 results despite local discrepancies outside the amplification range of V_G. This is mainly due to the validity of the simple analytical description of the circuit.

In order to verify the frequency performance, a particular operating point is selected



(a)

(b)

Figure 3.31: LNA S-parameters variation with the frequency (a) and IIP_3 (b) at 2.4 GHz, $V_G = 0.3\,\mathrm{V}$, $V_{BN} = 0.9\,\mathrm{V}$ and $V_{DD} = 1\,\mathrm{V}$.

at $V_G = 300\,\mathrm{mV}$ and $V_{BN} = 0.9\,\mathrm{V}$. As shown in Fig. 3.32. a, the $S11 = -18.35\,\mathrm{dB}$ at $f0 = 2.4\,\mathrm{GHz}$ while the $S21 = 18.7\,\mathrm{dB}$ and the $NF = 3.5\,\mathrm{dB}$. As indicated in Fig. 3.32. b, the $IIP3$ is as high as 2.48 dBm and the power consumption is 716 μW only. It is noticed that a different trade-off can be addressed based on the analytical analysis targeting 2.4 dB of NF with more than 20 dB of gain while relaxing the linearity and power requirements.

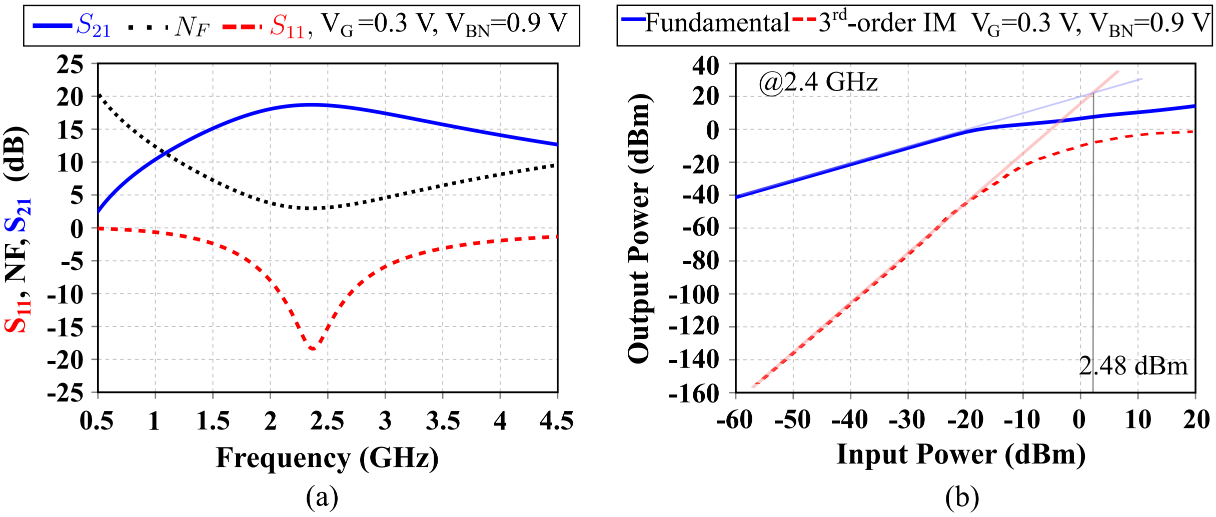


Figure 3.32: LNA S-parameters variation with the frequency (a) and IIP3 (b) at 2.4 GHz, $V_G = 0.3\,\mathrm{V}$, $V_{BN} = 0.9\,\mathrm{V}$ and $V_{DD} = 1\,\mathrm{V}$.

3.5 Conclusion

In this chapter, the g_m/I_D and inversion coefficient based design methodologies for RF LNA circuits are reviewed. Despite the efficiency of the methods proposed in the state-of-the-art, the lack of a sufficiently simple design-oriented model to describe the transistor's operation appears as a key limitation that has to be addressed. In this regard, we have presented a generic method based on a complete circuit description together with an accurate but simple transistor model taking into account main short-channel effects. A new model is proposed consisting of single-piece equations, derived from physics. The new 5PM for bulk and 6PM for *FD-SOI* are validated against experimental results and circuit simulations for RF LNA circuits in 28 nm *FD-SOI* technology. The simplicity of the model equations and the reduced number of parameters make the new model attractive for newcomers in the design area, as well as for the experienced ones in the pre-simulation phase of a design flow.

As a proof of concept, this chapter presents a simple design method using a g_m/I_D and inversion level approach suited for low power LNAs in advanced technologies. It allows a fast and first-time right design of the LNA, based on a simple analytical study by using the proposed model of the MOS transistor. The proposed methodology directly links the transistor bias conditions and size to the main LNA performances, including for the first time the analytical modeling of the LNA nonlinearity. Two common architectures are used as design examples in 28 nm *FD-SOI* CMOS technology. First a resistive feedback LNA with three implementation cases for different drain voltages are detailed. Then, a common gate LNA is considered to show how a good linearity can be achieved thanks to the design space exploration with the body-bias feature. Using the proposed methodologies, the adequate inversion level of the transistor and the sizes of the passive components are determined systematically to fulfill gain, noise figure and linearity performances with a limited sub-1mW power budget. The analytical and simulated performances are compared showing the accuracy of the proposed methodology. This fast strategy based on simple analytical calculations shortens the design time in comparison with the CAD-based approaches that are generally used for such advanced technologies.

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Chapter 4

Proposed LNA architecture: Wideband Continuous tunable active gm-boost LNA designed with the g_m/I_D methodology

Contents

4.1 Introduction

This chapter presents the design of a wideband sub-6 GHz inductorless Low-Noise Amplifier (LNA) tailored for advanced IoT applications. Taking advantage of a comprehensive analytical design method together with the 28 nm *FD-SOI* CMOS technology features, a large design space is explored, achieving performance fine-tunability. This adaptability enables the consideration of different trade-offs through two distinct biasing options for the same circuit as illustrated in Fig. 4.1. The first biasing aligns with the strict specifications of NB-IoT and LTE-M 5G cellular standards, detailed in Chapter 2, particularly addressing the challenging sub-2 dB noise figure. On the other hand, the second biasing

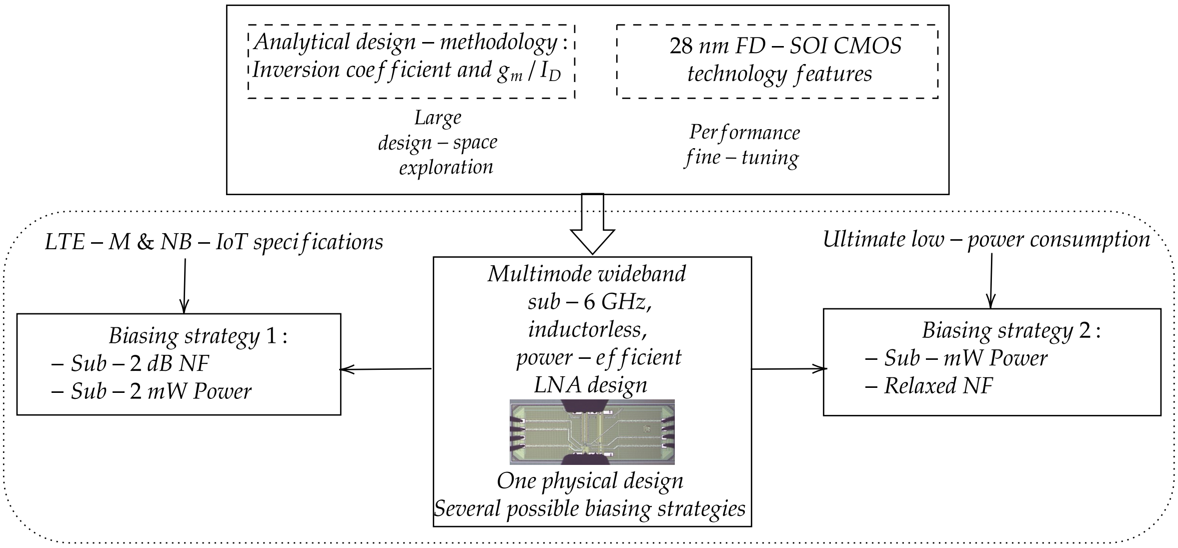


Figure 4.1: Illustrative representation of the wideband LNA design with the two biasing strategies.

option tailors the circuit for ultimate low-power consumption, aiming for a sub-mW power budget to comply with various deployment bands of the NB-IoT (ECC-Report-266, 2017).

Following the steps outlined in Fig. 3.22, the adequate architecture is first selected through the analysis of the state-of-the-art, focusing on the most demanding specifications for biasing strategy 1. Subsequently, a proposed topology is presented to overcome the design challenges, and extensively described through analytical expressions.

In this chapter, the *FD-SOI* technology is leveraged to introduce novel design features, emphasizing continuous tunability in performance. The LNA design methodology relies on the g_m/I_D efficiency factor and the inversion coefficient, using the 5PM/6PM accurate transistor model introduced in Chapter 3.

The design process initiates with preliminary LNA sizing based on analytical equations and design-space exploration, followed by an iterative improvement step involving simulations and sizing refinements to meet specified requirements. Finally, the implementation of the LNA, along with measured results in both cases, are detailed and compared with the state-of-the-art.

4.2 Architecture selection

Based on the theoretical and statistical analysis detailed in Chapter 2, the circuit's topology is selected to meet most of the design specifications outlined in Section 2.4.1 and summarized in Table. 4.1.

Table 4.1: Multimode LNA design specifications.

Mode	High-Sensitivity	Medium Sensitivity	Low-Sensitivity
P_{in} (dBm)	-115 to -60	-60 to -40	-40 to -25
Frequency (GHz)	$[0.44, 2.2]$	$[0.44, 2.2]$	$[0.44, 2.2]$
NF (dB)	<2	<5	<8
Power (mW)	<2	<2	<2
Return loss (dB) (50Ω)	<-10	<-10	<-10
Gain (dB)	>20	>15	>10
IIP_3 (dBm)	>-40	>-20	>-10
P_{1dB} (dBm)	>-50	>-30	>-15

Although inductive degenerated circuits have good noise and power consumption performance (Lee et al., 2006), integrated inductors do not comply with low-cost radios, as shown in Chapter 2. The common-gate-based topologies are wideband and power-efficient, but they suffer from a NF higher than $2-3\,\text{dB}$ (Zhang et al., 2022) under matching conditions, which does not meet the specifications. Nevertheless, the CG topology has a distinct advantage over the CS-based ones, as it has an additional gate terminal that can receive an extra RF signal. With proper DC biasing and filtering, this RF signal applied to the gate of a CG topology can enhance its performance without affecting the amplifier behavior. For example, applying unbalanced signals to both the source and gate terminals can improve the gate-to-source voltage swing (V_{GS}), thereby enhancing the effective transconductance of the device. Consequently, g_m-boost CG topologies exhibit great potential in reducing CG noise at low power levels, as they decorrelate the input impedance selection from the CG transconductance. The principle, as detailed in Section 2.3.3, is based on introducing an auxiliary inverting amplifier with a modulus gain of (A) between the source and the gate terminals. This technique multiplies the transconductance of the classic CG by ($A+1$). This allows for an improvement in noise performance independent of input impedance matching. Moreover, this solution is widely used in the literature for wideband discrete multimode LNAs based on active (Taris et al., 2021) and passive (Tamura et al., 2020) boosting amplifiers.

Additionally, as shown in Section 2.3.2, the complementary common-source topology achieves a good trade-off between noise, linearity, and power. In this work, it is employed as the auxiliary inverting amplifier cell to boost CG performance and to combine the advantages of both topologies to meet the strict requirements.

The proposed solution combines the advantages of the g_m-boosted CG architecture to meet the challenging performances along with the *FD-SOI* CMOS technology features allowing circuit tunability thanks to the body control bias.

4.3 Circuit Description

The schematic of the proposed Low-Noise Amplifier (LNA) is illustrated in Fig. 4.2. It is based on an inductorless single-ended wideband LNA utilizing the active g_m-boost Common Gate (CG) architecture.

The CG transistor's drain is connected to a switched load resistor R_L for gain level tuning. The source goes to a switched degeneration resistor R_D, determining as well the input matching. The active boosting is achieved with an auxiliary inverting complementary common-source amplifier, composed of the NMOS transistor M_n and the PMOS transistor M_p, to feed the amplified input signal to the gate of M_1. The coupling capacitances are denoted Cc_i.

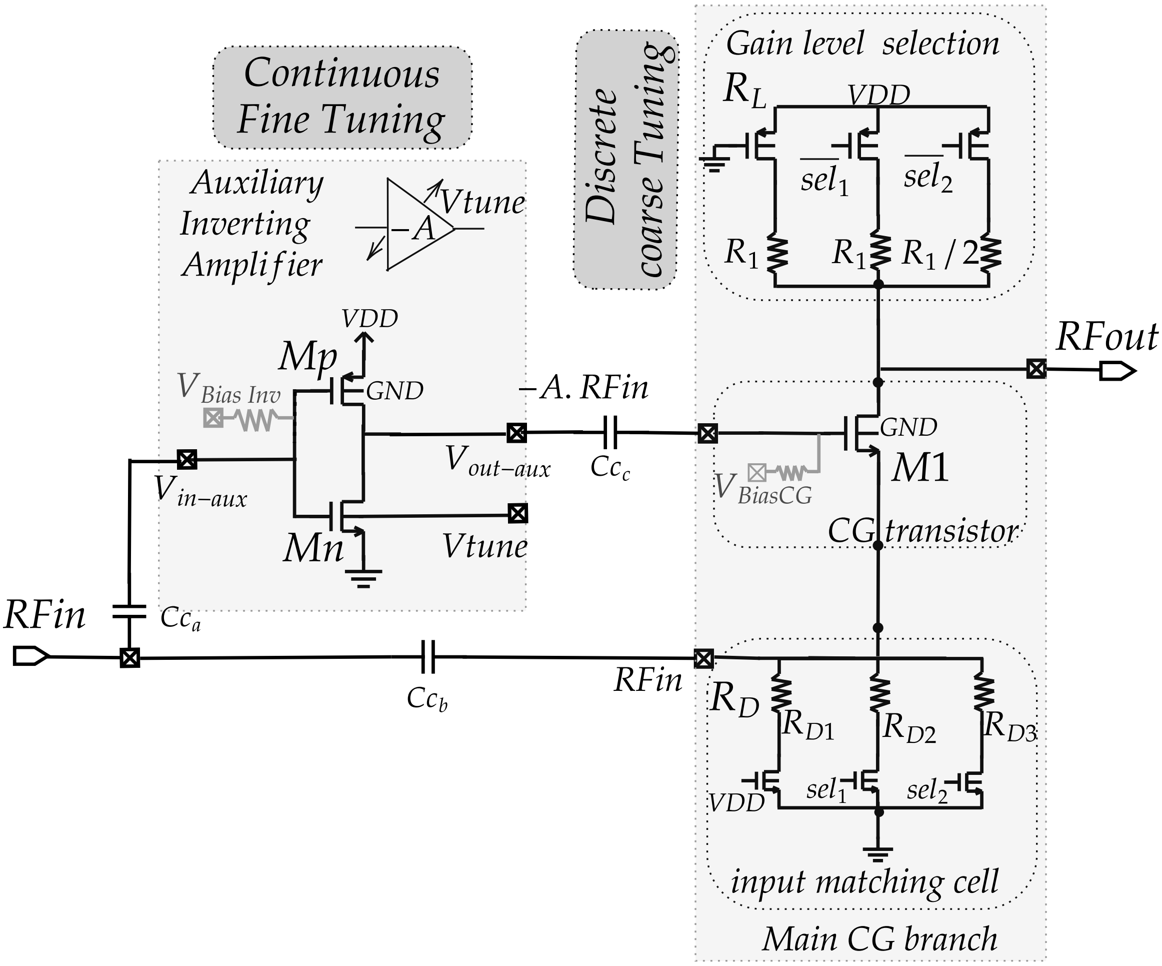


Figure 4.2: Simplified schematic of the proposed multi-mode LNA.

4.3.1 Small-signal analysis

The main performance equations for the LNA are derived from the small-signal equivalent circuit, depicted in Fig. 4.3.

For the inverting amplifier, the equivalent components are expressed through the NMOS and PMOS relative characteristics in parallel expressed as,

$$C_{GS} = C_{\text{gsn}} + C_{\text{gsp}}, \tag{4.1}$$

$$C_{GD} = C_{\text{gdn}} + C_{\text{gdp}}, \tag{4.2}$$

$$C_{DS} = C_{\text{dsn}} + C_{\text{dsp}}, \tag{4.3}$$

$$g_{meq} = g_{\text{mn}} + g_{\text{mp}}, \tag{4.4}$$

$$R_{DS} = \frac{1}{g_{dseq}} = \frac{1}{g_{\text{dsn}} + g_{\text{dsp}}}. \tag{4.5}$$

In fact, the C_{GS} capacitance should take into account C_{gbn} and C_{gbp}, also C_{DS} could include C_{dbn} and C_{dbp}. For sake of simplicity, these capacitances are not taken into account as a first order approximation. The transfer function of the boosting amplifier is expressed as,

$$A(j\omega) = \frac{V_{\text{out,aux}}(j\omega)}{V_{\text{in,aux}}(j\omega)} = -g_{\text{meq}}R_{\text{DS}}\frac{1 - j\omega\frac{C_{GD}}{g_{meq}}}{1 + j\omega(C_{GD} + C_{DS} + C_{L1})R_{DS}}, \tag{4.6}$$

with C_{L1} is the equivalent load capacitor at the output $V_{out-aux}$ and C_L is the load capacitor of the LNA.

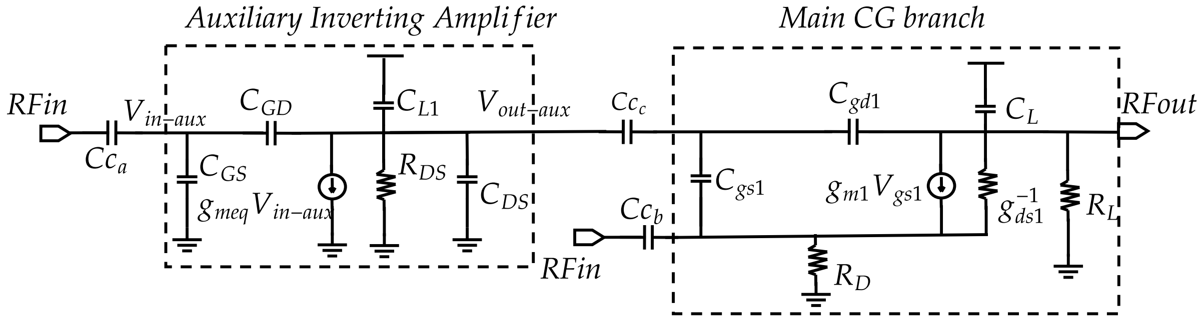


Figure 4.3: Equivalent small-signal model of the proposed multi-mode LNA.

The DC auxiliary gain depends on the ratio of the effective transconductance and the effective conductance of the complementary common source amplifier which is easily scaled by simple design methodologies. The LNA input impedance can be expressed as,

$$Z_{in} = \frac{1 + \frac{(C_{DS}+C_{GD}+C_{gs1})j\omega}{g_{dseq}}}{g_{m1}(1 + A + \frac{j\omega C_{DS}}{g_{dseq}}) + \frac{1}{R_D} + \omega^2\frac{C_2^*}{g_{dseq}} + j\omega C_3}, \tag{4.7}$$

with g_{m1} is the M_1 transistor transconductance and,

$$C_2^* = C_{GS}C_{DS} - C_{DS}(C_{GS} + C_{gs1}) + C_{GS}(C_{GD} + C_{gs1}), \tag{4.8}$$

and,

$$C_3 = (C_{GD} + C_{gs1})(1 + A) - C_{GS}, \tag{4.9}$$

which can be approximated for DC analysis to

$$R_{in} = \frac{1}{g_{m1}(1 + A) + \frac{1}{R_D}}. \tag{4.10}$$

This equation guides the selection of the (g_{m1},R_D) pair for the main CG branch to achieve an auxiliary gain range while maintaining the matching condition to R_s (with R_s

is the source resistance at the LNA input estimated conventionally at 50Ω). The matching can be evaluated using either the impedance or the scattering parameter S_{11}, which is the input port voltage reflection coefficient expressed as,

$$S_{11} = \frac{R_{in} - Rs}{R_{in} + Rs}. \tag{4.11}$$

Ideally $S_{11} = 0$ at perfect matching, however, for good transmission $S_{11\ (\log)} < -10\,\mathrm{dB}$ is acceptable (Appendix B).
The voltage gain of the active g_m-boosted CG LNA can be derived as,

$$G_v = \frac{\frac{g_{m1}(1+A+\frac{C_{DS}j\omega}{g_{dseq}})}{1+\frac{(C_{DS}+C_{GD}+C_{gs1})j\omega}{g_{dseq}}} + g_{ds1} + C_{ds1}j\omega}{g_{ds1} + \frac{1}{R_L} + C_{ds1}j\omega}. \tag{4.12}$$

The static voltage gain expression can be simplified as,

$$G_o = g_{m1}R_L(1 + A). \tag{4.13}$$

The gain is also evaluated by the forward voltage gain of the S-matrix S_{21} expressed as,

$$S_{21} = \sqrt{\frac{R_{in}}{R_S}}\,(1 + S_{11})\,G_o. \tag{4.14}$$

From the small-signal analysis, the LNA noise factor can be expressed as in (4.15) by taking into account the main noise contributors in addition to the source resistance ($V_{nosource}$), for instance, the CG transistor M_1 (V_{noM1}), the auxiliary cell by its NMOS and PMOS transistors (V_{noA}) and both resistances R_L (V_{noRL}) and R_D (V_{noRD}).

$$F = 1 + \frac{(V^2_{noM1} + V^2_{noA} + V^2_{noRL} + V^2_{noRD})}{V^2_{nosource}}. \tag{4.15}$$

From the small signal derivation (Appendix C), the main noise contributions can be expressed by the circuit parameters as,

$$\begin{aligned} F = 1 + &\frac{\gamma(A^2/g_{meq} + 1/g_{m1})}{((1 + g_{m1}(1 + A)R')^2(1 + A)^2R_S)} \\ &+ \frac{(R_S/R_D)}{(1 + R_S(1 + A)g_{m1})^2} + \frac{1}{(R_LR_S(g_{m1}(1 + A))^2)}, \end{aligned} \tag{4.16}$$

with $R' = R_D//R_S$ and γ is the excess noise factor that we consider the same for the three transistors for simplification.

4.3.2 Non-linearity analysis

The non-linearity performance is evaluated through the input referred third order intermodulation factor (IIP_3). Assuming two signals with adjacent frequencies (f_1) and (f_2) at the LNA input. The amplifier third order non-linearity generates a third order intermodulation product IM3 at ($2f_1 - f_2$) and ($2f_2 - f_1$) that should be minimized in order to prevent the signal desensitization at these frequencies.

Transistor non-linearity

In a transistor, the distortion can be generated from the transconductance and the output conductance (Sansen, 1999) which can be expressed through the two-dimensional Taylor expansion of the drain current with respect to v_{gs} and v_{ds} voltages as,

$$i_{ds} = g_m v_{gs} + \frac{g_{m2}}{2} v_{gs}^2 + \frac{g_{m3}}{6} v_{gs}^3 + g_{ds} v_{ds} + \frac{g_{ds2}}{2} v_{ds}^2 + \frac{g_{ds3}}{6} v_{ds}^3 + \gamma_2 v_{gs} v_{ds} + \gamma_3 v_{gs}^2 v_{ds} + \gamma_4 v_{gs} v_{ds}^2, \quad (4.17)$$

with γ_2, γ_3, and γ_4 being the second and third-order cross terms. Considering a resistive load R_L (that is assumed linear) the v_{ds} can be directly linked to i_{ds} as $v_{ds} = -R_L i_{ds}$. Hence, the complete i_{ds} function can be expressed in v_{gs} as,

$$i_{ds} = \alpha_1 v_{gs} + \alpha_2 v_{gs}^2 + \alpha_3 v_{gs}^3, \quad (4.18)$$

with,

$$\alpha_1 = \frac{g_m}{1 + R_L g_{ds}} = \alpha_1(i_D, W, R_L), \quad (4.19)$$

$$\alpha_2 = \frac{\frac{g_{m2}}{2} + \frac{g_{ds2}}{2}\alpha_1^2 R_L^2 - \gamma_2 \alpha_1 R_L}{1 + R_L g_{ds}} = \alpha_2(i_D, W, R_L), \quad (4.20)$$

$$\alpha_3 = \frac{\frac{g_{m3}}{6} - \frac{g_{ds3}}{6}\alpha_1^3 R_L^3 + g_{ds2}\alpha_1 \alpha_2 R_L^2 - \gamma_2 \alpha_2 R_L}{1 + R_L g_{ds}} + \frac{\gamma_4 \alpha_1^2 R_L^2 - \gamma_3 \alpha_1 R_L}{1 + R_L g_{ds}} = \alpha_3(i_D, W, R_L). \quad (4.21)$$

Thanks to the 6PM model, these coefficients can be easily expressed as a function of the transistor inversion coefficient i_D and width.

Considering the single transistor case (as the case for the CG transistor branch), the IIP_3 can be expressed as,

$$IIP_3 = 20 \log \left(\sqrt{\left| \frac{4\alpha_1}{3\alpha_3} \right|} \right) = IIP_3(i_D, W, R_L). \quad (4.22)$$

Assuming that the current distortion is mainly generated from the nonlinearity of the transconductance for simplicity, the IIP_3 can be reduced to,

$$IIP_3 = 20\log\left(\sqrt{\left|\frac{8g_m}{g_{m3}}\right|}\right) = IIP_3(i_D). \tag{4.23}$$

Hence, it is expressed by one variable independently from the width and directly derived from the 6PM set of equations.

Gm-boosted CG LNA non-linearity

In the active g_m-boosted CG LNA, the distortion sources are mainly the three gain transistors, the CG M_1, M_n, and M_p. From the two branches, two current sources can be defined to express the circuit IM3 current as $i_{IM3,cg}$ and $i_{IM3,M_{n,p}}$ (Appendix B). The output IM3 due to the common gate transistor is given by $v_{out,IM3cg} = R_L i_{IM3,cg}$. The IM3 output resulting from the complementary common-source configuration is derived from two distinct sources (as shown in the IIP_3 expression (4.27)). The first source is the equivalent third-order non-linear coefficient contributed by both transistors. In fact, when considering the parallel configuration of NMOS and PMOS transistors in small-signal equivalent signal, the equivalent current can be expressed as,

$$\begin{aligned} i_{ds,MnMp} &= (\alpha_{1Mn}v_{gs} + \alpha_{2Mn}v_{gs}^2 + \alpha_{3Mn}v_{gs}^3) - (-\alpha_{1Mp}v_{gs} + \alpha_{2Mp}v_{gs}^2 - \alpha_{3Mp}v_{gs}^3) \\ &= \alpha_{eq1}v_{gs} + \alpha_{eq2}v_{gs}^2 + \alpha_{eq3}v_{gs}^3, \end{aligned} \tag{4.24}$$

with $\alpha_{eq1} = \alpha_{1Mn} + \alpha_{1Mp}$, $\alpha_{eq2} = \alpha_{2Mn} - \alpha_{2Mp}$, and $\alpha_{eq3} = \alpha_{3Mn} + \alpha_{3Mp}$. As it can be noticed, the non-linearity in the current from the complementary common source branch can be reduced through a proper sizing of the NMOS and PMOS transistors in order to cancel the second-order non-linear effects ($\alpha_{eq2} = 0 \Leftrightarrow \alpha_{2Mn} = \alpha_{2Mp}$).

The second origin is induced by a factor of two second-order non-linear effects. The second-order harmonic voltage at the source of the common-gate transistor $V_{in,2f_1,cg}$ is fed to the gate of the complementary CS cell. This voltage, with the fundamental input signal, generates an IM3 product through the second-order non-linear coefficient α_{eq2}. Hence, the IM3 current due to the complementary CS transistors is given by,

$$\begin{aligned} i_{IM3_{MnMp}} &= \frac{3}{4}\alpha_{eq3}v_{in,f_1}^3 + \alpha_{eq2}v_{in,f_1}(v_{in,2f_1,cg} + v_{in,2f_{1MnMp}}) \\ &= \left(\frac{3}{4}\alpha_{eq3} + \alpha_{eq2}\left(\frac{R_{in}R_S}{R_{in}+R_S}\frac{\alpha_{2cg}}{2}(1+A)^2 + \frac{\alpha_{eq2}}{\alpha_{eq1}}\frac{A}{2(A+2)}\right)\right)v_{in_{f1}}^3. \end{aligned} \tag{4.25}$$

As a result, the IIP_3 of the g_m-boosted CG LNA can be expressed as,

$$V_{IIP_3} = \sqrt{\frac{1}{\frac{(1+A)^2}{IIP_{3cg}^2} + \frac{A}{(1+A)IIP_{3MnMp}^2} + \frac{3}{2}\frac{A}{IIP_{2cg}IIP_{2MnMp}}}}. \tag{4.26}$$

Assuming that the current distortion is mainly generated from the non-linearity of the transconductance for simplicity, the CG inversion coefficient is selected using the 6PM model to maximize the IIP_{3cg}. Also, the sizes and inversion coefficients of the complementary common source are chosen in order to cancel the second-order non-linearity (maximum IIP_{2MnMp}) and maximize the IIP_{3MnMp} while keeping the current and noise constraint.

Moreover, considering a linear buffer inserted at the output of the LNA for the output matching with a $IIP_{3buffer}$ high enough, the equivalent V_{IIP3} voltage can be derived as,

$$\frac{1}{V_{IIP3}^2} = \frac{(1+A)^2}{IIP_{3cg}^2} + \frac{A}{((1+A)IIP_{3MnMp}^2)} + \frac{3}{2}\frac{A}{(IIP_{2\_cg}IIP_{2MnMp})} + \frac{G_0^2}{IIP_{3buffer}^2}. \tag{4.27}$$

4.4 Design considerations and performance-tunability strategy

4.4.1 Multimode Operation

To meet the high coverage and penetration requirements of both standards with best-in-class performance, a multi-mode solution is chosen. This multimode operation enables the satisfaction of various performance trade-offs depending on the input signal power, allowing for channel-aware configuration. The design space can be categorized into three main sensitivity modes. Each mode corresponds to an input power range with distinct requirements, as detailed in Table. 4.2.

Table 4.2: Choice of the sensitivity-modes operation zones.

Mode	**High-Sensitivity**	**Medium-Sensitivity**	**Low-Sensitivity**
P_{in} (dBm)	-115 to -60	-60 to -40	-40 to -25
Gain	High	Medium	Low
Sensitivity	High	Medium	Low
Selectivity	Low	Medium	High

In high-sensitivity mode, characterized by a low input signal amplitude, a high gain is required and the lowest noise figure is targeted to reach the sensitivity. However, the linearity requirements can be relaxed thanks to the $-60\,\text{dBm}$ filtering (i.e. high gain mode used only up to $-60\,\text{dBm}$ input signal). On the other hand, the low-sensitivity mode addresses higher input levels, the gain can be then reduced while the linearity performance should be maintained high to avoid the signal compression.

The multimode operation of the proposed LNA combines coarse and fine tuning, as shown in Fig. 4.2. This approach ensures extensive coverage of the design space and maintains continuity in performance variation. Discrete gain steps of 6 dB are obtained by selecting different resistances forming R_L, through the switches commanded by the signals $\overline{(\text{sel}_1)}$ and $\overline{(\text{sel}_2)}$. The voltage gain, proportional to R_L as indicated in (4.13), determines the operation mode, as summarized in Table. 4.3.

Table 4.3: Mode description for each configuration.

Mode	**High-sensitivity**	**Medium-sensitivity**	**Low-sensitivity**
P_{in} (dBm)	-115 to -60	-60 to -40	-40 to -25
R_L	R_1	$R_1/2$	$R_1/4$
sel_1, sel_2	$sel_1 = sel_2 = V_{DD}$	$sel_1 = 0$ $sel_2 = V_{DD}$	$sel_1 = sel_2 = 0$
Voltage Gain	G_0	$G_0 - 6\,\text{dB}$	$G_0 - 12\,\text{dB}$

Within each mode, the inverting amplifier boosting factor (A) is finely tuned through a continuous control offered by the 28 nm body-bias feature applied to the CS transistor M_n ensuring the continuity between adjacent modes. As demonstrated in the analytical derivations (4.7)-(4.27), the variation in (A) allows for sweeping LNA main performances. The body-bias voltage V_{tune} adds in variations of the inverting amplifier characteristics atop the coarse control setting. Besides, it allows to compensate corner variations. While varying (A), the input matching condition is maintained by setting R_{in} within values that assure a return loss $S_{11} < -10\,\text{dB}$ for each discrete mode. Hence, this condition is satisfied through the choice of g_{m1} and the degeneration resistance R_D within each sensitivity mode.

4.4.2 Auxiliary inverting amplifier

The Auxiliary inverting amplifier provides the active boosting factor A for the CG branch and allows through the fine-tuning control step, to continuously tune the performances within each sensitivity-mode. As in (Tamura et al., 2020), the circuit is designed for the highest gain and power (highest sensitivity). Then, the performance decrease to allow higher linearity. In this regard, the complementary common source inverting amplifier is biased first at the maximum gain value with the output at the NMOS and PMOS drains being at half dynamic $(V_{DD}/2)$. A combination between the body-bias voltage of the NMOS ($VBN = Vtune$) and the gate voltage VG allows to get this condition while ensuring the performance tunability. The gate voltage is provided by a complementary diode-connected transistors (auto-zero) and designed in close proximity to the complementary CS to avoid mismatch.

Fine-tuning strategy:

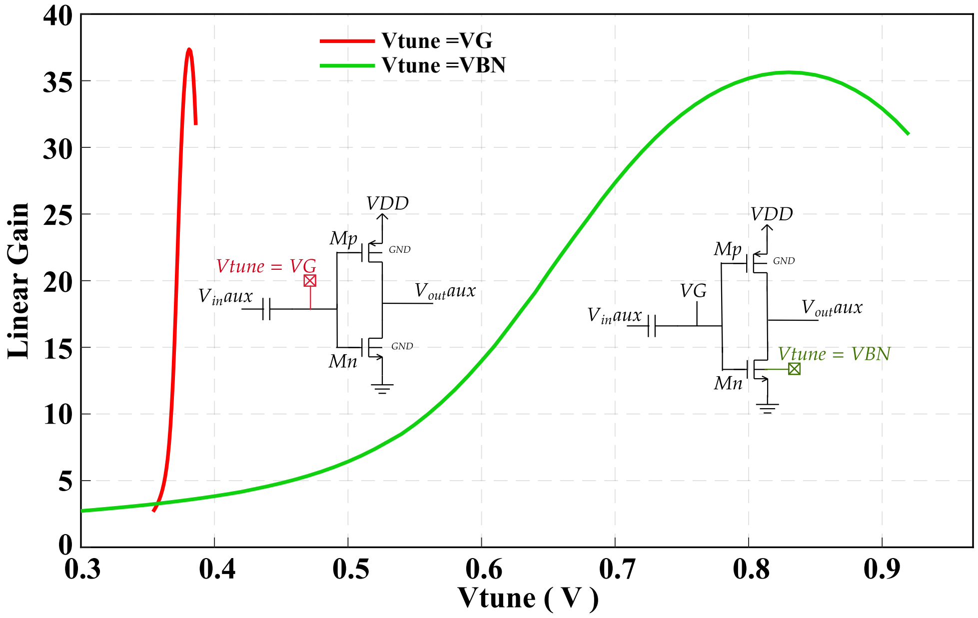


Figure 4.4: Small signal gain variation of the inverting amplifier as function of $Vtune$. Comparison with tuning using the gate voltage and using the body-bias voltage.

In order to illustrate the fine−tunability offered by the technology's features, the auxiliary gain of the complementary common source stage is investigated. In Fig. 4.4, for the same targeted gain range, the voltage tuning (V_{tune}) is compared using two control mechanisms: gate control through the gate voltage V_G for $V_{BN} = 0\,\text{V}$, and body bias knob control (V_{BN}) for a constant V_G. The gain range in the first scenario is achieved for 32 mV tuning range of V_G. However, the second case provides more than 17 times the voltage control range, achieving the same gain sweep with 550 mV NMOS transistor body-bias variation.

In the initial case, the inverting amplifier characteristics (gain and current) directly change through V_G, which linearly modifies the overdrive voltage with a unit factor (slope $1\,V/V$). In contrast, the second scenario tunes the overdrive voltage through the threshold voltage, which linearly varies with the body bias voltage at a slope of around $85\,mV/V$. This slope is much smaller than in the initial case, offering better control over the characteristics. This feature is a key design technique in our proposed circuit, and since it is accurately reproduced by our simple model, it is implemented in our analytical design methodology. In Fig. 4.5.a, the intrinsic gain A is compared for three different NMOS body bias voltages ($V_{BN} = \{0\,V,\ 0.45\,V,\ 0.9\,V\}$), while the LVT PMOS transistor is at the nominal bias ($V_{BP} = 0\,V$). The 5PM/6PM ACM model accurately reproduces the PDK simulation results using transistors with $L = 60\,nm$, for which the DC and small-signal characteristics were validated in Section 3.3.

While the gain region of the complementary CS amplifier is critical, using body-bias voltage as a tuning knob allows better control of this region, avoiding abrupt transitions between the inverting states. Moreover, employing body-bias control on both transistors, NMOS and PMOS, enables navigation into a larger design space, exploring regions inaccessible with the shared gate voltage. However, it's worth noting that in this work, for simplicity, we solely utilize body-bias for the LVT NMOS transistor ($VBN = Vtune$) to avoid the generation of negative voltage. During the fine-tuning step, $Vtune$ is decreased, leading to an increase in the CS NMOS threshold voltage VTH_n. Consequently, the overdrive voltage ($VG - nVS - VTH_n$) decreases. This has several consequences: the g_m/I_D efficiency factor increases, tending toward the weak inversion region, and the current I_D is lower with a reduced g_{mn}. In this scenario, the NMOS drain voltage VDS will increase. The variation range of $Vtune$ is controlled to maintain sufficient headroom for the CS PMOS transistor to operate in the saturation regime. Accordingly, the VDS of the PMOS will decrease from $VDD/2$. Since the current is decreasing, the overdrive voltage will decrease, lowering the value of g_{mp}. As a result, the boosting factor A will decrease while decreasing $Vtune$. There are multiple conditions and challenges related to the variation range of this boosting factor A that should be considered in this design:

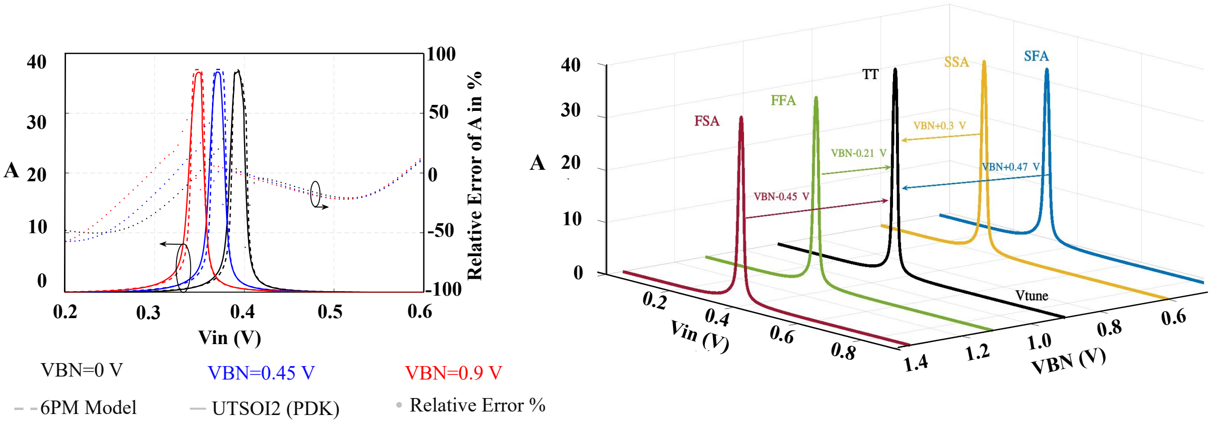
1. First, the ratio between the highest (A_{up}) and lowest (A_{low}) values of A should exceed the ratio of the load resistance steps (2 in this case) to ensure overlapping between adjacent modes.

2. The lowest value of A is limited by the $Vtune$ value that ensures the operation of both CS transistors in saturation regime.

3. While tuning A, the input impedance of the LNA is also tuned. The couple (A,R_D) is selected in order to have a $S_{11} < -10\,\text{dB}$ within the complete variation range of A.

4.4.3 Tuning control voltage and Process compensation

The NMOS body-bias feature in this circuit serves two purposes as illustrated in Fig. 4.6. Firstly, it enables fine-tuning of performance with higher control resolution compared to

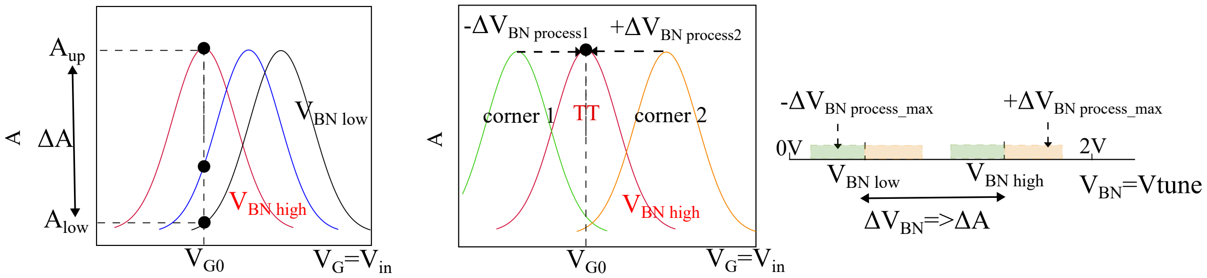


(a) (b)

Figure 4.5: a. Complementary CS transfer function. b. Variation across the process corners and possible correction using V_{BN}.

control obtained through the transistor gate. This fine-tuning affects the boosting factor A, allowing precise control of the LNA's main performance when the complementary common source cell is employed as the active boosting cell for the CG transistor. This control assumes typical functionality of the devices.

However, due to process variations, maintaining the selected operation point of the complementary CS cell becomes crucial. In this context, NMOS and PMOS transistor body-bias voltages can be used to compensate for these deviations. For simplicity, we focus solely on the NMOS device in this work. For an NMOS LVT transistor, with a nominal body-bias between 0 V and 2 V, the dual operation of this feature imposes conditions on the choice of the applied ΔV_{BN}. Assuming from Fig. 4.5.a that $\Delta V_{BN} = V_{BN_{\text{high}}} - V_{BN_{\text{low}}} = 0.4\,\text{V}$ is sufficient for a monolithic boosting factor variation that allows fine-tuning within a sensitivity mode and continuity between adjacent modes, given by $(1 + A_{\text{up}})/(1 + A_{\text{low}}) > 2$.



Typical process: Fine-tuning Correction across process corners

Figure 4.6: Illustration of the double usage of the body-bias voltage $V_{BN} = Vtune$.

For a given operational point, depending on the process corner (SS, SF, TT, FS, FF), the complementary CS characteristics deviate, and a correction $\Delta V_{BN\,\text{process}}$ is applied to obtain typical performance. An example of complementary CS cell characteristic process variation and the correction using body bias is shown in Fig. 4.5.b. This example is demonstrated for a typical operation point with $Vtune = VDD = 0.9\,\mathrm{V}$. As indicated, the process corners behavior can be corrected by modifying the body bias voltage with $|\Delta V_{BN\,\mathrm{process}}|_{\mathrm{max}} = 0.47\,\mathrm{V}$ in extreme cases.

Hence, the aforementioned conditions can be expressed as,

$$\begin{aligned} V_{BN_{\mathrm{low}}} - |\Delta V_{BN\,\mathrm{process}}|_{\mathrm{max}} &> 0\,\mathrm{V} \\ V_{BN_{\mathrm{high}}} + |\Delta V_{BN\,\mathrm{process}}|_{\mathrm{max}} &< 2\,\mathrm{V} \end{aligned} \tag{4.28}$$

Several characterization iterations have demonstrated that $|V_{BN}\,process|_{max} = 0.47\,\mathrm{V}$ is considered the worst-case scenario. Hence, for the typical functionality that allows tuning while providing enough margin to compensate for process variations, $V_{BN_{\mathrm{low}}} = 0.5\,\mathrm{V}$ and $V_{BN_{\mathrm{high}}} = 0.9\,\mathrm{V}$ can be selected. In this case, for each sensitivity mode, the complementary CS is biased for the maximum gain with $Vtune = V_{BN_{\mathrm{high}}} = V_{DD}$ then decreased up to $Vtune = V_{BN_{\mathrm{low}}} = V_{DD}/2$ for the tunability.

4.4.4 Common-gate amplification branch

The common-gate branch is composed of the switched load resistors R_L, the CG transistor and a degenerative switched resistor R_D. To enhance matching and minimize potential mismatch sources, a relative condition can be first set on R_L and R_D in order to design both resistances from a common unit resistance R_u. Hence $R_L{=}NR_D = NPR_u$ with N and P are integer numbers. The (g_m, R_L) pair contributes to the gain together with A, while the (g_m, R_D) pair sets the input impedance for a given A. The design sizes (g_m, R_L, R_D) can be solved for a given gain, input impedance and noise figure. Ideally, the preliminary component values addresses the optimal design point which corresponds to the highest specifications. The bias and size of the CG transistor M_1 are obtained by considering the IIP_3. The linearity requirement will set the ratio of g_m and g_{m3} for a boosting factor A. This can be directly linked to the inversion coefficient i_D using the $5PM/6PMACM$ formalism and set of equations derived in Section 3.3 and (Neto et al., 2023). As it will be shown in Section 4.5.1, the IIP_3 sets then the i_D, which gives information about the CG efficiency factor g_m/I_D. Knowing g_m, the adequate current is determined and from the denormalization of i_D the CG transistor size is obtained.

4.5 Design methodology based on the g_m/I_D and inversion coefficient

The main objective of the proposed design methodology is to achieve comprehensive sizing based on the inversion coefficient, employing a simple set of analytical iterations. These iterations serve as a valuable tool for effective navigation within the design space, facilitating the exploration of optimal solutions that align with the required specifications. The methodology follows the generic flow outlined in Fig. 3.22. In Section 4.2, the architecture was selected for the LTE-M and NB-IoT applications. A detailed set of analytical equations is provided in Section 4.3.

To bridge the gap between circuit-level performance and transistor-level sizes, this methodology takes advantage of the accurate design-oriented 6PM transistor model described in Chapter 3. This application is particularly relevant to NMOS (M_n) and PMOS (M_p) transistors within the complementary common-source boosting cell, as well as NMOS CG transistor (M_1).

Specifically tailored to the selected length, the NMOS and PMOS toolboxes derived from the 6PM model provide all the necessary small-signal expressions for design. These expressions are directly tied to the inversion coefficient and the g_m/I_D efficiency factor. Importantly, these parameters are normalized concerning the transistor width, that can be easily integrated as a design variable. To further enhance the methodology's credibility, rigorous verification against measurements was conducted, using a reference transistor with a unitary configuration and a width of $W = 1\ \mu$m.

While the full version of the ACM $5PM/6PM$ model includes transistor capacitances (Neto et al., 2023), this aspect was not developed during the course of this thesis and remains unvalidated for the 28 nm *FD-SOI* CMOS technology. Hence, to properly design a wideband LNA circuit, this method combines the design-oriented model set of equations with LUT that allows for the estimation of the circuit's frequency behavior, enabling the evaluation of bandwidth.

4.5.1 Design flow

The design algorithm followed to design the multimode continuously tunable CG LNA is explained in Algorithm 1 and depicted in the flow chart in Fig. 4.7. Initially, a uniform length for all transistors is chosen ($L = 60\,$nm), ensuring a sufficiently high transition frequency f_T relative to the targeted frequency bands and low device $NFmin$ (Section. 4.4.2). This selection is made to minimize variability and achieve a compact area.

Algorithm 1 g_m-boost CG LNA design.

```
FOR (GAIN, NF, S11, POWER) TRADE-OFF (Select Mode)
    FOR THE HIGH BOOSTING FACTOR $A_{up}$
        solve $\mathbf{g_{m1}, R_L = NR_D, g_{meq}}$
FOR ($IIP_3$ )
    solve $(\mathbf{g_m/g_{m3}})_1$ $for\ M_1$
    Using ACM model derive $\mathbf{i_{D1}}$
    deduce $(\mathbf{g_m/I_D})_1$
        Evaluate $\mathbf{I_{D1}}$
         $\mathbf{W_1 \leftarrow I_{D1}/(I_{S1\mu m} i_{D1})}$
            (LUT) Evaluate $\mathbf{C_{gs1}}$ and $\mathbf{C_{ds1}}$
FROM POWER BUDGET, $A_{up}$, $\alpha_{eq}$ AND $g_{meq}$
            Using ACM derive $\mathbf{W_n}$, $\mathbf{W_p}$ $(i_{Dn}, i_{Dp})$
                (LUT) Evaluate $\mathbf{C_{GS}}$ and $\mathbf{C_{DS}}$
                Compute $\mathbf{BW}$
            for the obtained Wn and Wp
                select $\Delta V_{tune}$ for $\Delta A$
```

The initial step involves the selection of a suitable operating mode with the corresponding desired performance objectives. This includes evaluating trade-offs among important performances like gain (S_{21}), noise figure, input reflection coefficient (S_{11}), and power consumption. The outcomes of this analysis serve as crucial inputs for guiding subsequent design decisions.

In this phase, we focus on a high boosting factor (A_{up}) to tailor the fabricated sizes to the highest targeted specifications. The algorithm solves for key parameters such as g_{m1}, R_L, R_D and g_{meq} based on (4.6)-(4.16) to establish a foundation for further calculations.

Next, from the required IIP_3 (4.27) and the output buffer characterization, the algorithm targets to maximize IIP_{3cg} and to reduce the complementary-common source contribution through the $\alpha_{eq2} = 0$ condition. For the CG transistor M_1, the linearity requirement set the $(g_m/g_{m3})_1$ ratio (4.23). Thanks to the 5PM/6PM small-signal derivation, this ratio can be expressed independently from the transistor sizes as function of the inversion coefficient i_{D1} (3.39), (3.47). The g_m/I_D coefficient is then directly deduced (3.41) and from the previous derivation of g_{m1}, the required current I_{D1} is computed. If it satisfies the requirements of the power budget, the biasing condition is obtained and the size W_1 is evaluated through the unitary transistor model as,

$$W_1 = \frac{I_{D1}}{I_{S1\mu m}\, i_{D1}}, \tag{4.29}$$

with $I_{S1\mu m}$ is the specific current from the 1μm transistor (3.27). The algorithm evaluates then the capacitances (C_{gs1} and C_{ds1}) using a lookup table (LUT) based on the obtained size, providing critical insights into the transistor's dynamic behavior.

The subsequent step refines the design by determining the sizes and bias of NMOS (W_n, i_{Dn}) and PMOS (W_p, i_{Dp}) transistors. This process takes into account power budget constraints, the high boosting factor (A_{up}), equivalent second-order non-linearity factor (α_{eq}), and the equivalent transconductance (g_{meq}).

For A_{up} the transistor pair is biased at equilibrium for an output DC voltage $V_{DSn} = V_{DSp} = V_{DD}/2$. Following this condition, both transistors drive the same current I_D such as,

$$I_{Dn} = W_n\, I_{S0n}\, i_{Dn} = I_{Dp} = W_p\, I_{S0p}\, i_{Dp}. \tag{4.30}$$

Consequently, the inversion coefficients of both transistors are linked to the size ratio, and the current can be expressed as, $I_D = I_D(W_p, W_n, i_{Dn})$.

The boosting factor exhibits lower sensitivity to changes in sizes and current at $V_{DD}/2$. It is expressed by the transconductance (g_{mn},g_{mp}) and the output conductances (g_{dsn},g_{dsp}), as in (4.6). Consequently, it can be simplified to $A = A(W_p, W_n, i_{Dn})$, similar to the current expressions, using (3.39) and (3.40). In the same way, $g_{m,eq}$ can be represented as $g_{m,eq} = g_{m,eq}(W_p, W_n, i_{Dn})$.

For achieving linearity improvements (maximizing IIP_{2MnMp}), α_{eq2}, dependent on second-order transconductances (g_{mn2}, g_{mp2}), should be minimized (3.44), (3.48). This introduces an additional condition on the solution triplet, $\alpha_{eq2} = \alpha_{eq2}(W_n, i_{Dn}, W_p) = 0$. The system, characterized by as many unknowns as equations, can be then, systematically solved while exploring various possibilities.

These determined transistor sizes (W_n and W_p) are then utilized in LUT to capture the dynamic behavior of the transistors and extract the corresponding capacitance values. In cases where the bandwidth requirements are not met, a redesign loop is initiated. This loop involves the re-selection of solutions from the design-space or readjustment of specifications to identify a new set of preliminary design variables.

Once the transistors final sizes are determined, the values of W_n and W_p are incorporated into the unitary transistor model. This evaluation is important for determining the appropriate body-bias voltage range, ΔV_{tune}, applied to the NMOS transistor, as discussed in Section 4.4.3. This process allows for the targeting of the necessary boosting

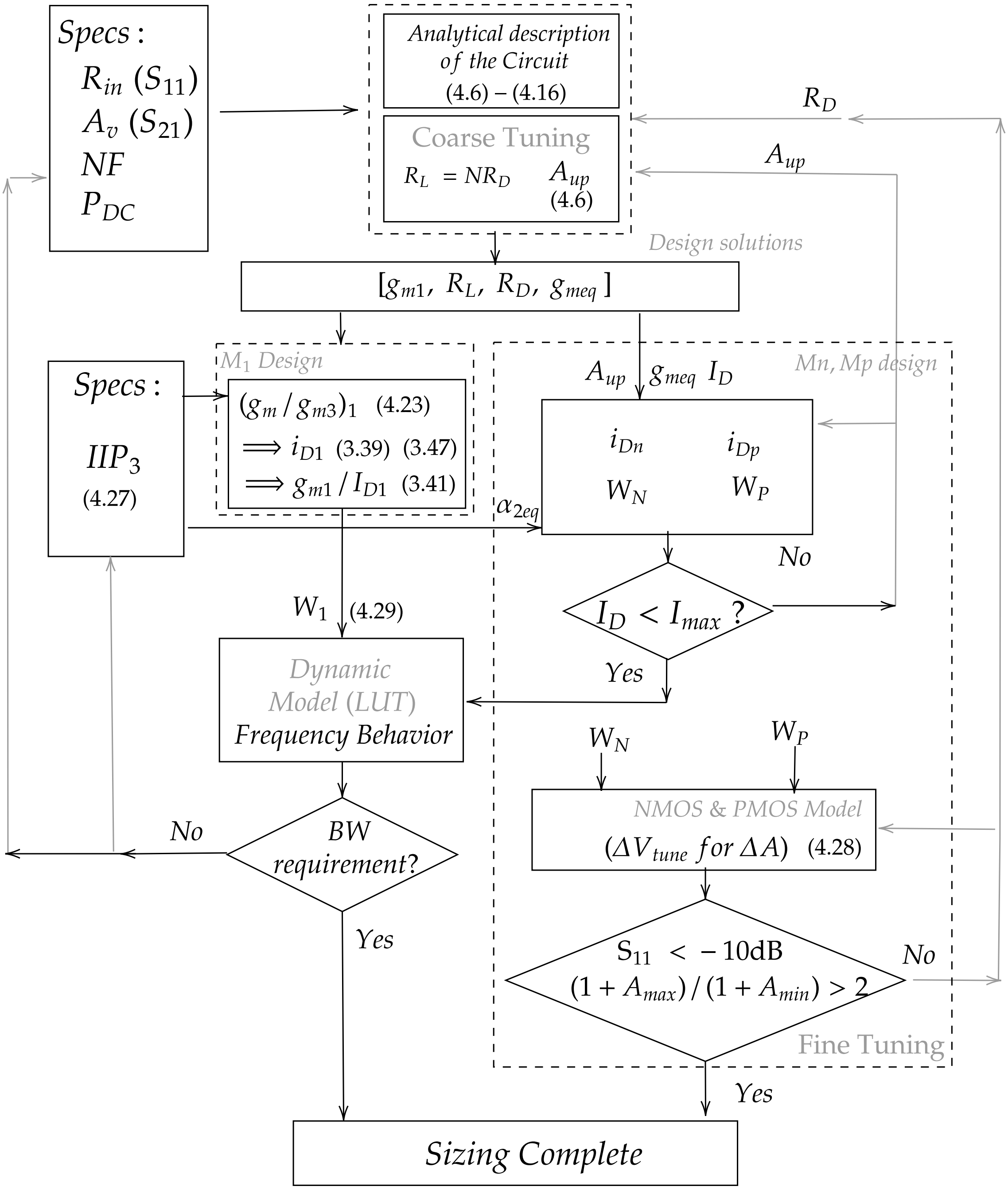


Figure 4.7: Complete design methodology flow diagram.

factor variation to achieve gain tuning within each sensitivity mode and maintain the matching condition corresponding to the selected R_D. In cases where these conditions are violated, a redesign loop is activated to find a more optimal solution.

This analytical analysis demonstrates that the complete sizes of the devices are obtained through straightforward iterations based on a simplistic 6-DC parameters design-oriented model and an accurate analytical description, all derived from circuit-level RF specifications. Additionally, these sizes and bias points can be easily adjusted to meet a set of specifications or favor a different trade-off, targeting extremely low-power applications (as demonstrated in the second scenario) or highly linear circuits. The solution is facilitated by incorporating the body-bias voltage of the *FD-SOI* CMOS technology, as discussed in Section 4.4.3.

This iterative and analytical design methodology, deeply rooted in the g_m/I_D and inversion-coefficient based approach, ensures a systematic exploration of the design space, leading to an LNA that meets the specified requirements for 5G cellular standards, specifically targeting the NB-IoT and LTE-M applications. The inclusion of body-bias voltage in the *FD-SOI* CMOS technology further enhances the adaptability of the design to varied operational scenarios. This process of sizing and tuning achieves a balance between performance metrics, making it a robust and versatile methodology for wideband LNA design.

4.5.2 Biasing strategy 1, high-sensitivity mode

This section provides a detailed exploration of the high-sensitivity mode, which specifically targets the lowest noise figure (NF) while requiring a substantial power consumption. The design method focuses on the hardest set of specifications. It aims to determine the sizes and bias for the upper working point A_{up} within this mode, then tune the boosting factor A to cover larger design space. For $NF < 2\,\mathrm{dB}$ and a power budget limited to $2\,\mathrm{mW}$ while maintaining $S_{11} < -10\,\mathrm{dB}$ the higher gain value can be determined as shown in Fig. 4.8 obtained from the system solving of the first step $(A, g_{m1}, R_L, R_D, g_{meq})$. A good compromise can be obtained for a $S_{21} = 33\,\mathrm{dB}$, $NF = 1.56\,\mathrm{dB}$ while maintaining the matching condition and a power consumption of $2\,\mathrm{mW}$ from $V_{DD} = 0.9\,\mathrm{V}$. These values are aligned with the specifications in Table. 4.6.

It's worth noting that a lower noise figure can be achieved, as demonstrated in Fig. 4.8, by relaxing the power constraints while maintaining the targeted gain. This flexibility allows for a fine-tuned adjustment of performance metrics based on specific application requirements.

Following the design algorithm outlined in Fig. 4.7 and detailed in Algorithm 1, the 6PM Model is employed to determine the inversion coefficient i_{D1} and size W_1 of the common gate transistor M_1 for optimizing linearity performance. Fig. 4.9 illustrates the computed IIP_3 values for both the common gate transistor and the LNA, considering

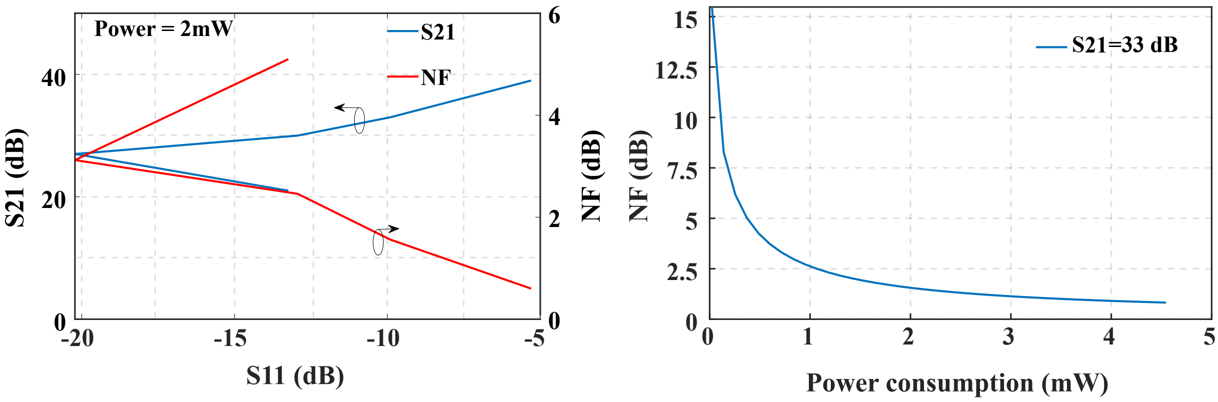


Figure 4.8: Example of design space exploration for the high sensitivity mode and performance trade off.

higher and lower gains within the high-sensitivity mode. These values, independent of the transistor size, provide insights into achievable trade-offs in the circuit.

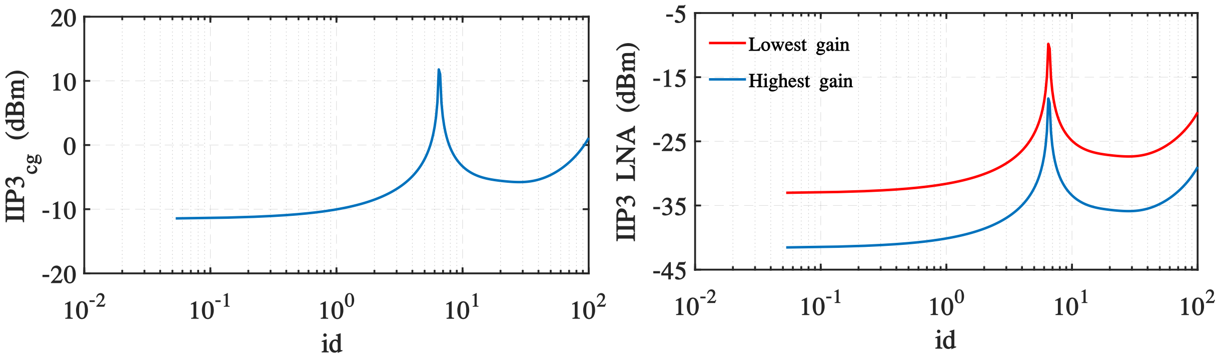


Figure 4.9: IIP_3 of the CG transistor IIP_{3cg} and of the LNA IIP_{3LNA} as function of the CG inversion coefficient.

The boosting factor A enhances gain and noise figure but notably degrades the linearity of a simple common gate (CG) configuration. By biasing for the sweet spot inversion coefficient (where $g_{m3} = 0\ A/V^3$) and minimizing A, the LNA achieves its best attainable IIP_3. This configuration is particularly suitable for the low-sensitivity mode, where lower gain is expected due to higher input signal amplitudes. In this scenario, with relaxed noise requirements, the CG branch is biased to improve linearity by selecting the CG inversion coefficient i_D and corresponding pairs (g_{m1},R_D) and (g_{m1}, R_L). A target IIP_3 of -20 dBm is chosen to size the CG transistor. An initial value of $i_{D1} = 5.8$ is selected, and further adjustments are made through multiple design loops in the algorithm.

In the subsequent step, the design space of the complementary common-source cell is explored by analyzing the inversion coefficients and sizes of both transistors. Characteristics such as current, boosting factor, equivalent g_{meq}, and second-order nonlinear coefficient α_{eq2} are depicted in Fig. 4.10. Initial sizing conditions on the NMOS and PMOS

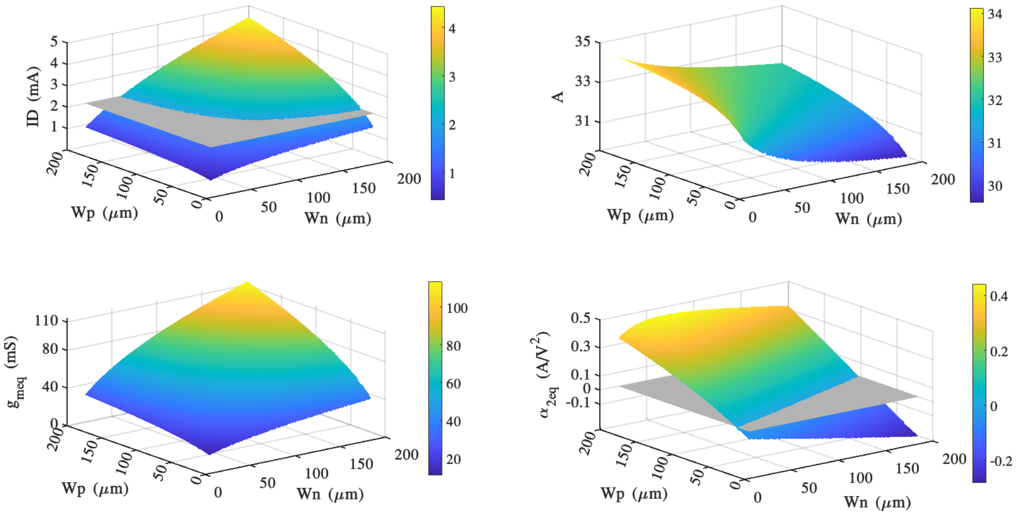


Figure 4.10: Main performance variation of the complementary common CS amplifier. a. The total current ID, b. The boosting factor A, c. the equivalent gm g_{meq} and d. The second order non-linear term α_{eq2}.

transistors are determined by the required values of $A_{up} = 31.5$ and $g_{meq} = 72\,\text{mS}$. Selection areas defined by the maximal current consumption of 2 mA and the non-linearity reduction ($\alpha_{eq2} = 0$), as represented in Fig. 4.10 for ID and α_{eq2}, guide the optimal sizing together with the corresponding inversion coefficients, establishing the bias points. This representation facilitates addressing various trade-offs, such as achieving a lower power solution with higher noise (lower A and lower g_{meq}) while maintaining good linearity ($\alpha_{eq2} = 0$).

The transistor sizes, reported in Table. 4.4, are obtained through iterative exploration loops, taking advantage of the 6PM model. The dynamic behavior is validated by extracting corresponding capacitances from the LUT to assess the frequency response. This ensures adjustments of transistor sizes and inversion coefficients around the optimal space for all three transistors, meeting bandwidth requirements while maintaining targeted performance ($W_n = 105\,\mu m$,$W_p = 124\ \mu m, W_1 = 20\ \mu m$ are the final sizes after layout and parasitics reduction). For the higher gain point in the high-sensitivity mode, a comparison of S_{21} and S_{11} elements from analytical calculations and frequency simulations is

Table 4.4: LNA Sizing based on the design algorithm for VDD=0.9 V.

A	M1	Mn	Mp	R_L	R_D
31.5 - 11.2	W1=40μm L1= 60 nm $i_{D1} = 5.2$	Wn=106μm Ln= 60 nm $i_{Dn} = 4.7 - 1.9$	Wp=98μm Lp= 60 nm $i_{Dp} = 17 - 7$	2640Ω	1320Ω

shown in Fig. 4.11. The pre-sized LNA achieves a 3-dB bandwidth exceeding 4 GHz, with $S_{11} < -10\,\text{dB}$ satisfied across the entire band. The analytical expressions using the DC transistor model demonstrate good agreement with PDK simulations.

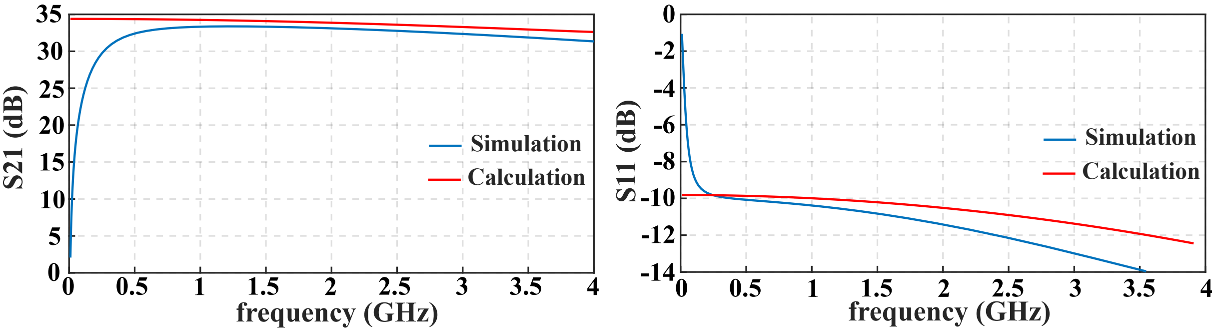


Figure 4.11: Performance variation in frequency of the highest gain working point of the high sensitivity mode: comparison between simulation and analytical derivation.

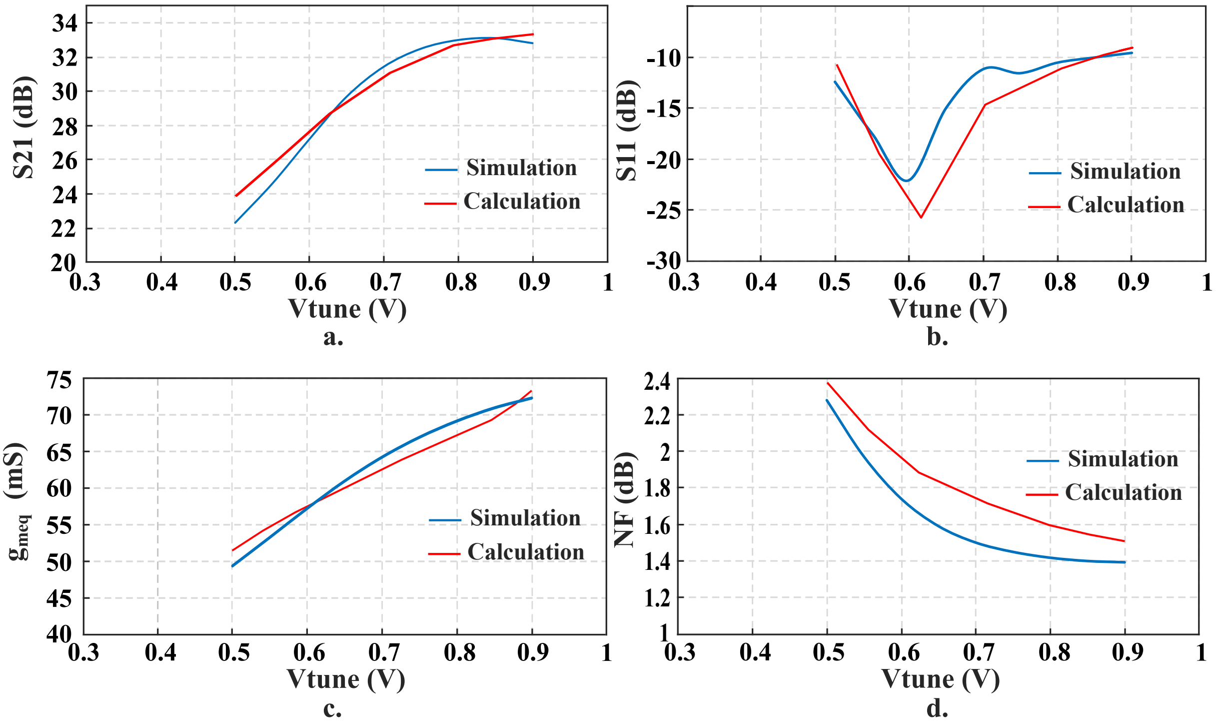


Figure 4.12: Simulated performance variation with the tuning voltage $Vtune$ (boosting factor A) in the high sensitivity mode.

To complete the design of the high-sensitivity mode, the fine-tuning step is executed to adjust performance and ensure continuity with adjacent modes. This involves applying the appropriate V_{tune} voltage range to transistor M_n according to the conditions described in Section 4.4.3. Key performance variations are illustrated in Fig. 4.12. While maintaining the input matching condition with $S_{11} < -10\,\text{dB}$ (as shown in Fig. 4.12.b), the equivalent transconductance of the boosting cell is linearly fine-tuned over a 400 mV voltage swing of V_{tune}. Correspondingly, the gain and NF are finely controlled, with S_{21} tuned over 8 dB (> 6 dB) to ensure overlap with the medium-sensitivity mode. The NF ranges from 2.4 dB to 1.56 dB, aligning with sensitivity requirements.

As depicted in Fig. 4.12, the analytical estimation of LNA performance using the simplistic 6PM Model aligns well with simulation results obtained through the 28 nm *FD-SOI* CMOS PDK model. The V_{tune} range, as described in Section 4.4.3, provides ample margin for compensating process variations, extending beyond the edges of the required range. This ensures robust performance in the face of potential process fluctuations.

4.6 Design robustness to process variations

The circuit's robustness is validated through simulations accounting for process and mismatch variations, providing insights into potential extreme scenarios post-fabrication. The key LNA performance metrics within each mode are assessed using process corners and Monte Carlo simulations. Statistical analysis involving gain, noise figure (NF), and compression point is conducted for the three sensitivity modes, considering random variations of V_{tune} based on 200 samples. This randomness includes variations in process, mismatch for transistors, resistors, and capacitors. The resulting distributions are illustrated in Fig. 4.13.

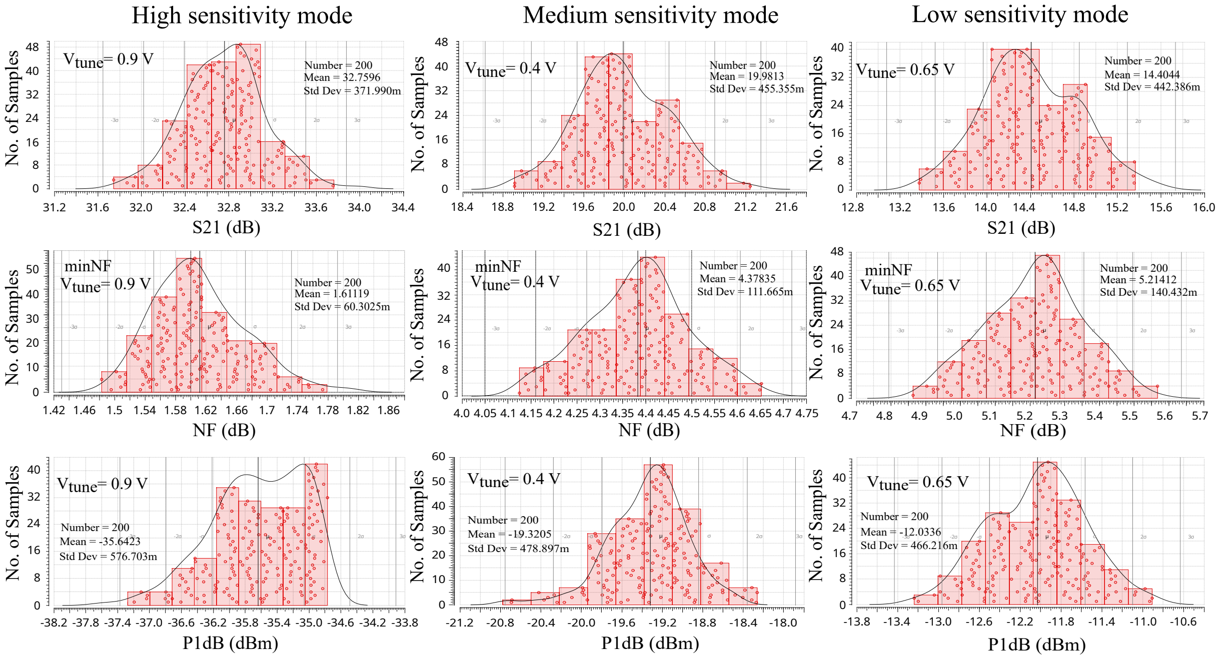


Figure 4.13: Monte Carlo simulation results of the gain, noise figure and P_{1dB} for the three sensitivity modes at random $Vtune$ values.

The circuit's appropriate biasing of the common gate branch, achieved through a current mirror based on the common centroid technique, coupled with the miniaturized self-biased complementary common-source configuration implemented in close proximity to the boosting amplifier, leads to performance distributions that are well-centered around typical values. The variations in extreme cases remain minimal. Additionally, the implemented dummy layout, placing all devices in an equivalent environment, contributes to mismatch reduction.

As depicted in Fig. 4.13, the variation in S_{21} remains below 6% in absolute terms around the nominal value, with a mere 3% **for the high-sensitivity mode**. Moreover, the NF exhibits **less than** 6% **variation**, and the $P_{1\text{dB}}$ experiences less than 7% variation. This robust statistical performance analysis underscores the reliability and stability of the LNA across various operating conditions and potential fabrication variations.

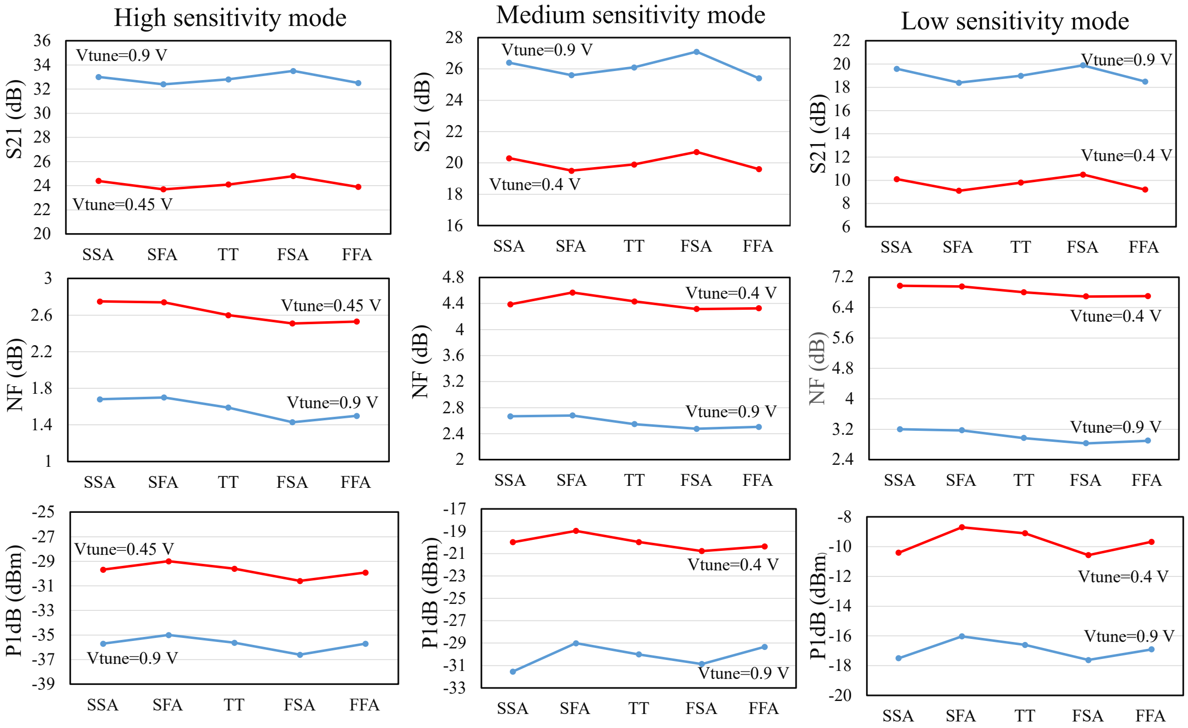


Figure 4.14: Corners simulation results of the gain, noise figure and IIP_3 for the three sensitivity modes for different $Vtune$ values.

Furthermore, the LNA's performance is assessed across various process corners, including SSA, SFA, TT, FSA, and FFA, at room temperature. In Fig. 4.14, the gain, noise figure, and $P_{1\text{dB}}$ for the high, medium, and low-sensitivity modes are presented for both upper and lower boosting gains ($V_{\text{tune}} = 0.9\,\text{V}$ and $V_{\text{tune}} = 0.4\,\text{V}$, respectively).

The performance remains relatively stable across corner variations, with deviations from the typical value **limited to** 10% **at most in extreme corners**. Additionally, the variations along the working points in all sensitivity modes exhibit similar trends, evident in the parallel lines representing different boosting gains (i.e., V_{tune} body bias values).

As discussed in Section 4.4.3, more consistent variations can be achieved by fine-tuning the body-bias voltage for each working point to converge towards the typical value.

4.7 Design for testability

The floorplan of the circuit is illustrated in Fig. 4.15, detailing the key building blocks of the SUGAR GLIDER chip. Despite the circuit's single-ended configuration at both the input and output, a Ground-Signal-Ground-Signal-Ground (GSGSG) topology is employed for de-embedding purposes. This configuration allows the placement of a GSG probe initially on "RF_{in1}", representing the primary signal path injecting into the LNA. Which is then measured at "RF_{out1}", the buffer output, incorporated only for measurement convenience and output matching. Simultaneously, the design incorporates a dedicated de-embedding path on silicon ("RF_{in2}", "RF_{out2}"), streamlining the extraction of noise, gain and linearity parameters.

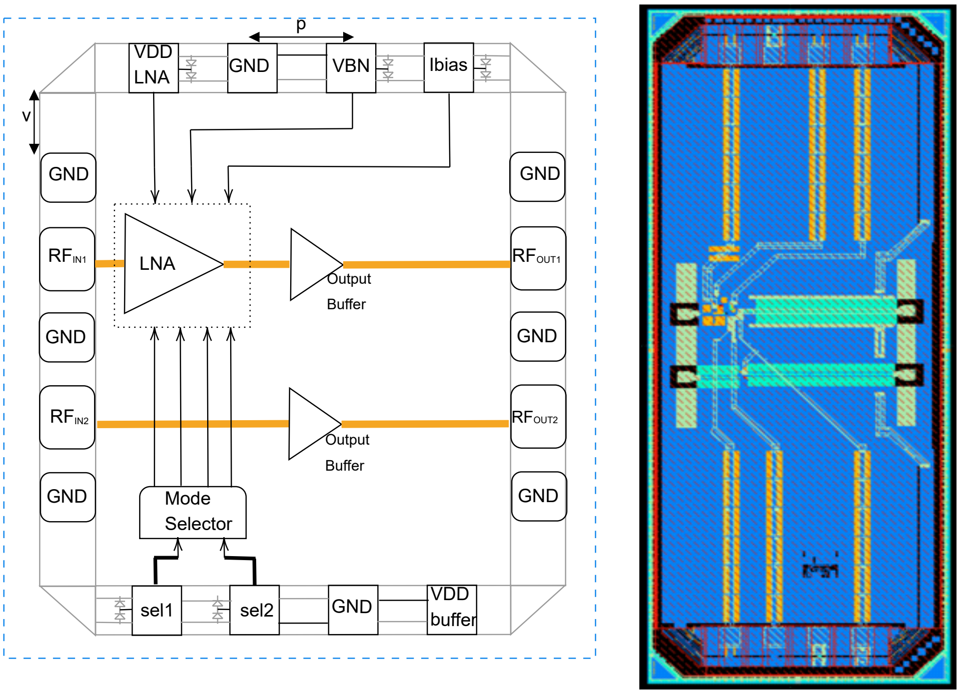


Figure 4.15: Floorplan of Sugar Glider LNA detailing building blocks locations, I/O pins and external and internal signals and the implemented Layout.

4.7.1 Output buffer

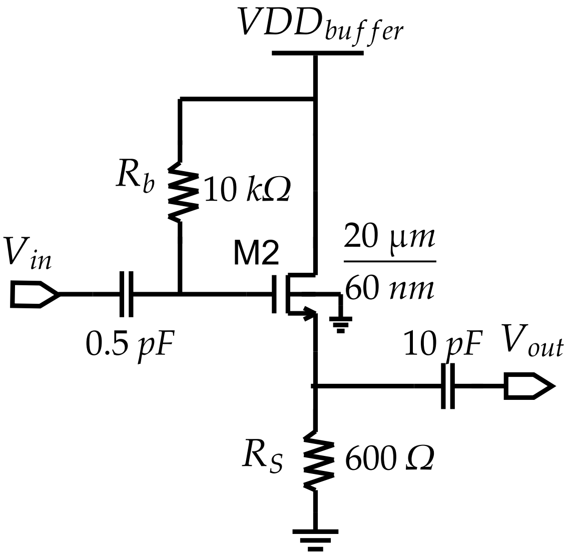


Figure 4.16: Schematic of the output buffer.

The integration of a source follower output buffer within the LNA design serves a dual role. First, ensuring a 50 Ω match at the output for precise measurements and second, establishing an efficient de-embedding path on silicon. As depicted in Fig. 4.16, the source follower transistor M_2 includes a source resistor (Rs) providing degeneration, which helps in stabilizing the gain and improving linearity. The gate resistor (Rb) is added to enhance stability and prevent unwanted oscillations.

The output buffer is carefully designed for optimized linearity. This optimization is particularly critical given the inherent difficulty in de-embedding linearity compared to parameters like gain and noise figure. The configuration, characterized by its output voltage closely following the voltage at the source terminal, facilitates direct access to the LNA's output, ensuring accurate measurements.

In Fig. 4.17, the characterization results of the output buffer are presented. Fig. 4.17.a illustrates a wideband output matching with $S_{22} < -10\,\text{dB}$ from 200 MHz up to 6 GHz, covering the frequency bands of interest. The linearity performance is depicted in Fig. 4.17. b. The high IIP_3 of 4.3 dBm does not compromise the linearity of the LNA, enabling straightforward measurements of the LNA's linearity performance. Both Figures demonstrate good agreement between simulation and measurements.

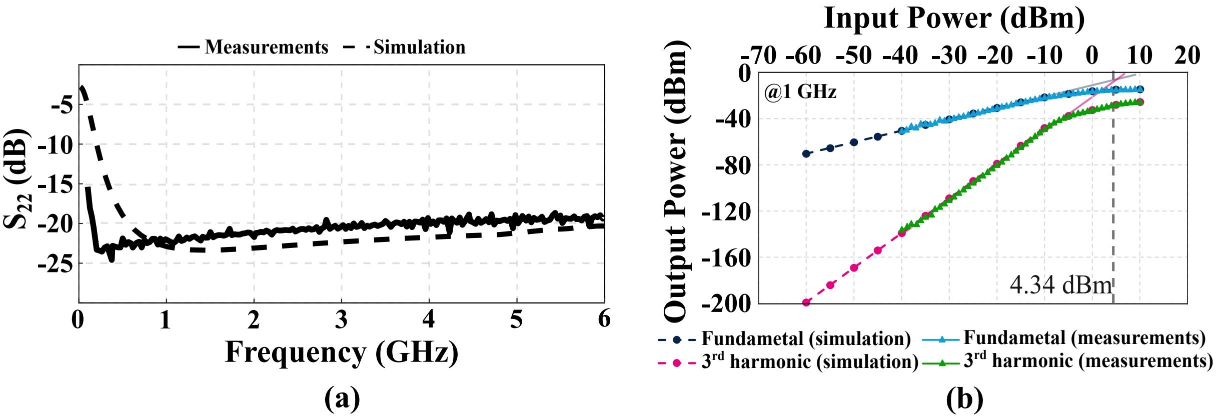


Figure 4.17: Output buffer characteristics. a. S_{22} over frequency. b. IIP_3 at 1 GHz.

4.7.2 Mode selector

The mode selector block has the main objective of receiving two external DC control signals and generate 4 DC signals that command the 4 switches in the CG branch to set the gain level and adapt the LNA. Following a simple truth table, a basic solution is proposed based on inverters and buffers with minimal delays. The implementation of a 2-to-4 decoder in this mode selector architecture introduces an area-efficient design. By utilizing fewer DC pads, the overall footprint of the circuit is reduced, contributing to a more compact layout. Consequently, from sel_1 and sel_2, we obtain four signals (sel_1, sel_2, $\overline{\mathrm{sel}_1}$, and $\overline{\mathrm{sel}_2}$). Each mode corresponds to a pair of values for (sel_1, sel_2), as presented in Table. 4.5.

It is important to note that, in certain use cases, an intermediate mode can be employed with this architecture. This mode can either replace the low-performance mode for irregular steps implementation when G_0 is low or reinforce the overlapping between modes. In this intermediate mode, the load resistance is $R_L = R_1/3$, and the discrete gain level is $G_0 - 9.5\,\mathrm{dB}$ instead of $G_0 - 12\,\mathrm{dB}$.

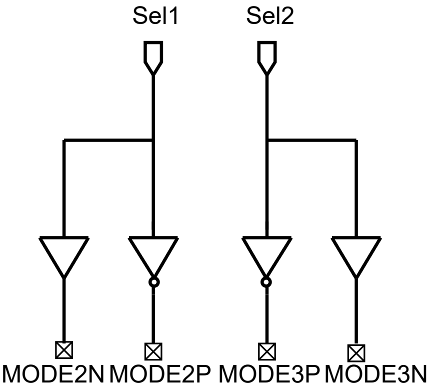


Figure 4.18: Circuit diagram of the mode selector block.

Input		Output				mode
sel1	sel2	MODE2P	MODE2N	MODE3N	MODE3P	
0	0	1	0	0	1	Low sensi.
0	1	1	0	1	0	Mid sensi.
1	1	0	1	1	0	High sensi.
1	0	0	1	0	1	Intermediate Mode (R/3)

Table 4.5: Truth table of mode selector block.

This circuit is designed using the technology standard cells, for which all transistors are Poly biased by 16 nm, with LVT process. This choice is led by the good performances in terms of power, density and area.

4.8 Physical LNA implementation

4.8.1 Top cell Layout

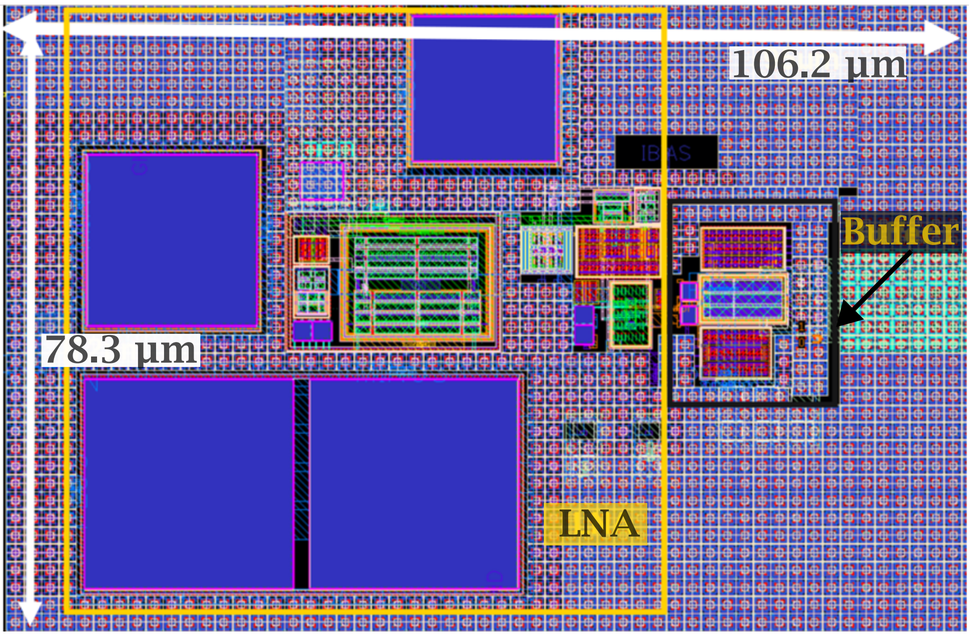


Figure 4.19: layout representation of LNA followed by the output buffer.

In order to challenge the state of the art LNAs, a compact layout in designed. It achieves 75.9 μm x 78.3 μm only which yields 0.0059 mm^2 less than best in class published LNA (Z. Liu et al., 2022) which achieves 0.0078 mm^2. The layout of the LNA followed by the output buffer is shown in Fig. 4.19. The RF signal is collected as close as possible at the input at “RF_{in1}” to avoid losses, parasitics and additive resistive noise contributors. The ground pins and the RF pad shield are designed using the same unit cell, which is also used to build the ground plane. This approach ensures a continuous and homogeneous ground environment, reducing the likelihood of potential differences at different "GND" connections on the chip.

The output buffer is strategically placed close to the LNA output, connected through a coupling capacitor to maintain isolation of DC signals and preserve the RF component. The output connects to a 50 Ω transmission line to minimize signal losses. The width of the output connection gradually increases to match the width of the transmission line.

Simultaneously, the connection is shielded using the same unit cell of the ground, avoiding disruptions in the mesh.

Coupling capacitors are positioned at the circuit periphery, promoting a uniform environment for transistors, surrounding dummies, resistors, and dummy resistors.
While each circuit part is laid out separately, they are designed to ensure close inter-sub-block connections and minimize additional parasitics that could lead to increased noise and reduced bandwidth. Each sub-part is enclosed by a guard ring tied to the ground floor plan, enhancing the distribution of ground connections and ensuring a common ground potential.

4.8.2 Complementary common source cell Layout

The g_m-boost cell is composed of the complementary common source NMOS and PMOS transistors. The bias circuit is composed of a replica of the amplifier but with diode connected NMOS and PMOS with smaller sizes in order to reduce its contribution to the power consumption. A low-pass RC filter isolates the bias circuit from the amplifier's gate, as illustrated in Fig. 4.20. The NMOS transistor is wide with a $W = 105\,\mu$m to satisfy bandwidth, noise, gain and power consumption trade off and to ensure the wanted transconductance and conductance of the device. To minimize the noise contribution, a finger width of 0.8 μm is selected. The device is obtained from the duplication of a unit small cell composed of 1 finger transistor. All the drains of the small unit transistors are connected in metal 6 through a large plate that serves as output path shared with the PMOS transistor. The gates, connected at metal 3 are routed in a shape of a ring surrounding all devises to have good access to all fingers with the same potential. The

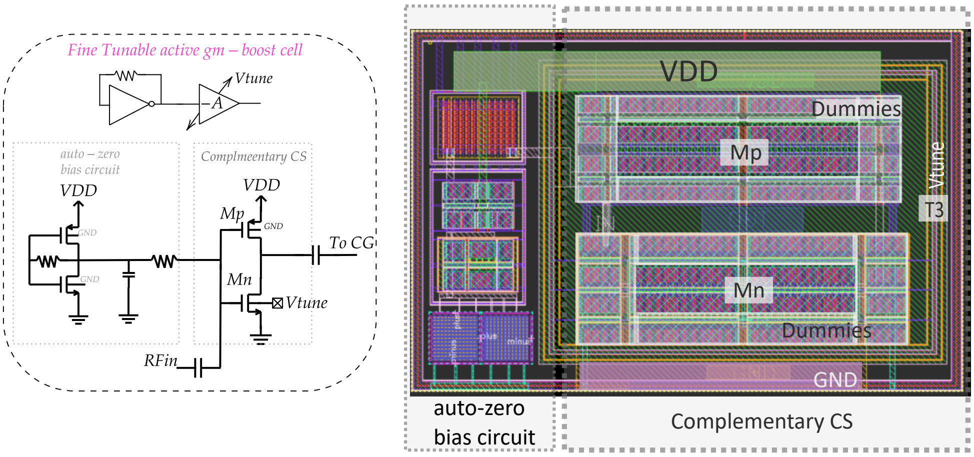


Figure 4.20: Layout representation of the g_m-boost cell.

ground node is the common node of all the sources connected at metal 5 and tied to the guard ring protecting the g_m-boost cell.

The PMOS transistor follows a similar design strategy, using four transistors for symmetry with the NMOS part. Surrounded by dummies on all sides, the PMOS transistor is created from the duplication of a unit small cell. A guard ring for $T3$ is used to connect the deep $NWELL$ and to distribute equally the DC signal of $Vtune$. The line supplying the g_m-boost cell is a large stack of M1-M8 to enhance shunt capacitance and minimize resistance access.

The bias circuit is composed of a diode-connected miniaturized duplicate of the complementary common source to set the gate voltage to a fixed value. Placed close to the amplifier, this circuit follows the same layout strategy to ensure a consistent environment and uniformity. A RC low-pass filter is used to isolate the RF signal feeding the gate of the amplifier from the DC component from the bias circuit. While the values of the passive devices in this circuit are less critical for functionality, aiming for a compact solution, no network surrounds these components to address problems related to resistance and capacitance variability.

4.8.3 Common gate cell Layout

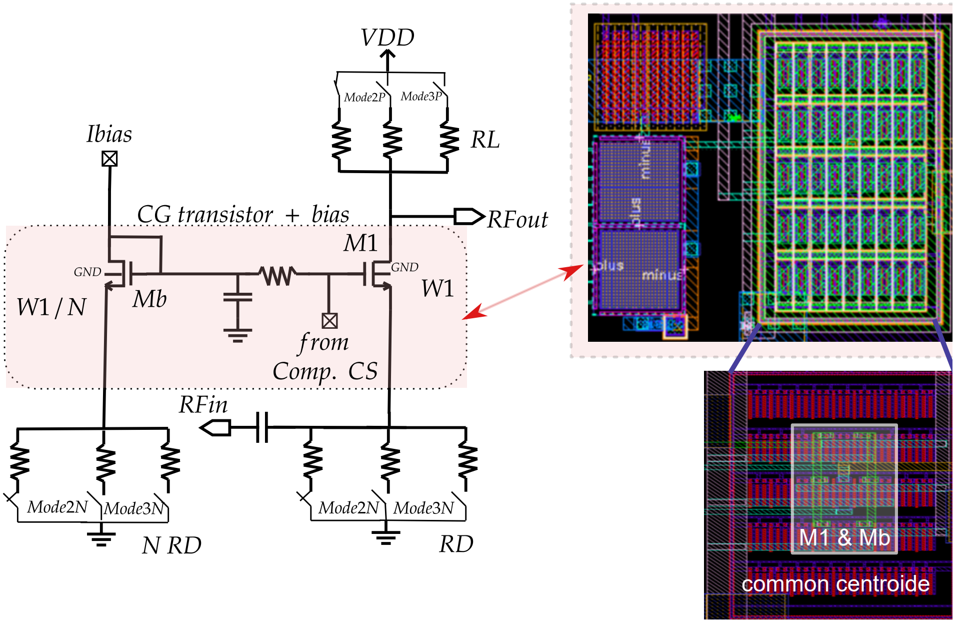


Figure 4.21: Layout representation of the common gate transistor with its bias.

The common gate sub-cell is composed of a common gate transistor with a biasing current mirror having a current amplification factor of 10. This sub-cell is composed of 11 small units arranged using the common centroid methodology for optimal matching, as illustrated in Fig. 4.21. To enhance the contact surface and facilitate various connection possibilities for the coupling capacitor and filter resistor terminals, the gates are locally connected within a ring formed by M4 surrounding the transistors. The layout design prioritizes matching and symmetry, while minimizing gate resistance to mitigate its impact on noise performance. Dummies transistors, sharing the same unit cell and shorted to ground, surround the main transistors. The RC filter is strategically placed close to the guard ring, isolating the transistor block for simplified connections and a compact cell layout. Special attention has been given to minimizing parasitic capacitance in the drain connection to preserve the output pole and, consequently, the amplifier bandwidth.

4.8.4 Switched resistors Layout

The circuit employs six blocks of switched resistance, as illustrated in Fig. 4.22. The three load resistances (R_L) for the common gate are connected via PMOS switches ("PSw"), controlled by signals from the mode selector block to VDD. Conversely, the three degeneration resistances (R_D) are connected through NMOS switches ("NSw") to ground.

In Fig. 4.22, R_D and R_L are designed using the same unit resistance (R_u) of 0.4 μm x 1 μm to mitigate variability issues. Both resistances are enclosed by a ring of 1 μm resistance, acting as a dummy. Additionally, a guard ring is positioned at the periphery of the resistors to facilitate shield connection.

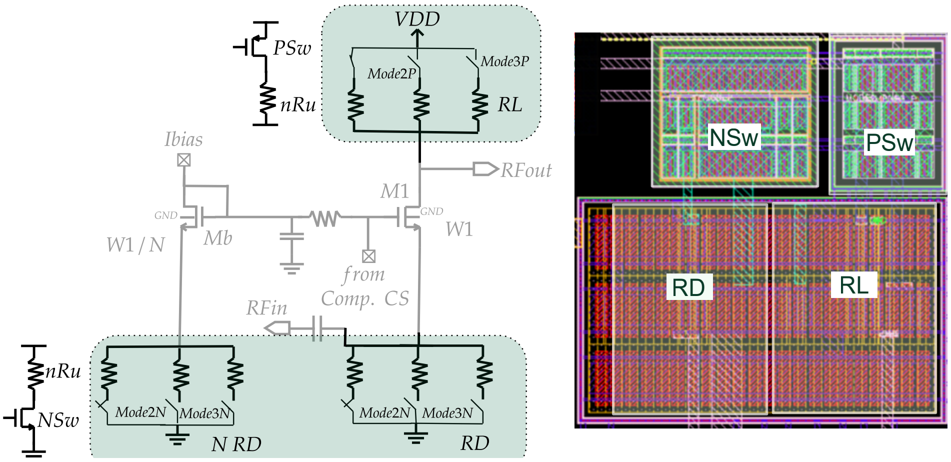


Figure 4.22: Layout representation of the switched resistors.

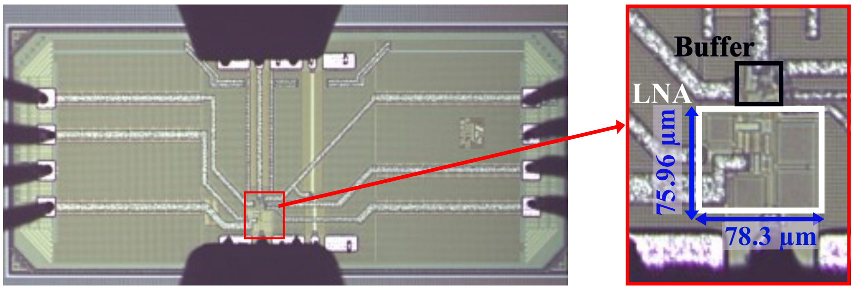


Figure 4.23: Chip micrograph.

4.9 Measurement results

Fig. 4.23 presents the microphotograph of the fabricated chip in 28 nm *FD-SOI* CMOS 8ML technology. The active area of the LNA is 0.0059 mm^2. The implemented circuit includes an output buffer based on a source follower for measurement purposes. The buffer contribution is de-embedded from the reported results using a stand-alone on-chip test path.

The same implemented circuit is employed for two distinct applications, each targeting different trade-offs. Utilizing the biasing adjustability and the extensive design space through the inversion-based methodology, two distinct use scenarios are presented. Firstly, the biasing strategy aims to minimize the noise figure (sub-2 dB) in the high-sensitivity mode, as illustrated in Section 4.5.1 to meet the specifications outlined in Table. 4.1. In the second scenario, the objective is to achieve extremely low power consumption (sub-mW) with a lower supply voltage.

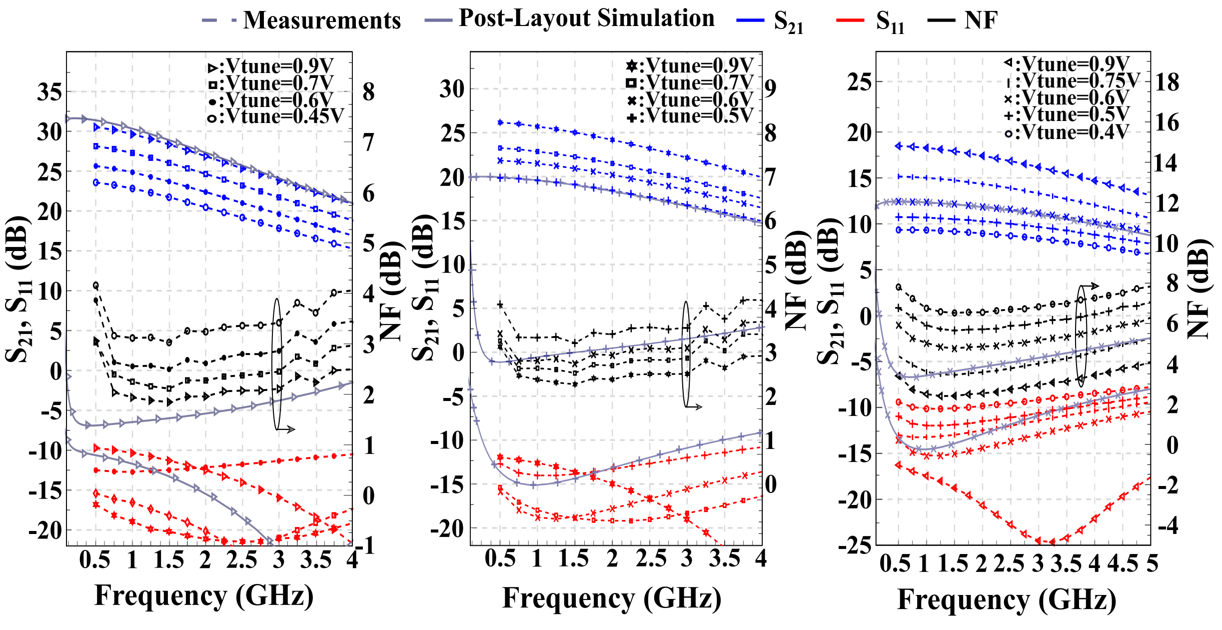
To demonstrate the feasibility and performance of the proposed LNA in both scenarios, the following section presents measurement results along with LNA post layout simulations (PLS). These results showcase the tunability of performance within each mode.

4.9.1 Biasing strategy 1

In this scenario, the supply voltage is fixed at 0.9 V, and the bias points are set to meet the design parameters obtained through the design flow, as outlined in Table. 4.4.

Fig. 4.24 presents the small-signal measured performances of the three modes. Thanks to the CG branch, a 4 GHz wideband matching ($S_{11} < -10\,\mathrm{dB}$) is achieved over all the gain values.

The measured performances of the high-sensitivity mode are illustrated in Fig. 4.24.a. The LNA successfully achieves a sub-2 dB NF in line with the specified target. Within the fine-tuning range, the minimum noise figure ranges from 3 dB to a remarkable 1.84 dB.

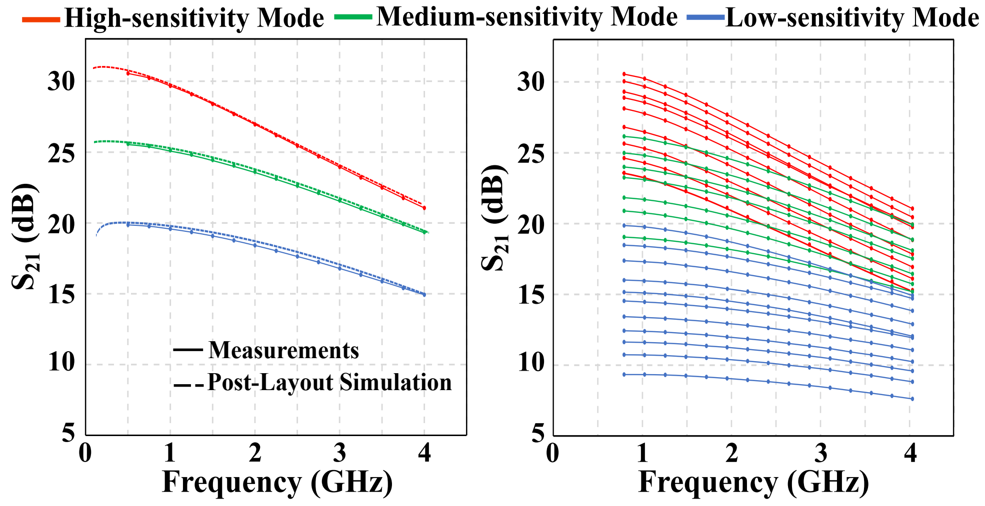


(a) (b) (c)

Figure 4.24: LNA main performances: S21, S11 and NF for different values of V_{tune} in: (a). High-sensitivity mode, (b). Medium-sensitivity mode and (c). Low-sensitivity mode.

The NF is then degraded at very low and higher frequencies because of the flicker noise and respectively the LNA bandwidth limitation.

A 500 mV $Vtune$ tuning range enables a 7 dB gain variation without impacting the 3-dB bandwidth, which remains at 2.2 GHz as meeting the requirements. The LNA exhibits a maximum gain ranging from 23.5 dB up to 30.5 dB.



(a) (b)

Figure 4.25: LNA main performances S21 for High-sensitivity, Medium-sensitivity and Low-sensitivity mode using coarse (a) and fine tuning (b).

Good agreement between post-layout simulations (PLS) and measurements is observed across the three coarse operation modes. The continuous tunability performance facilitates coverage of a broad design space, including corners variation, aligning with standard requirements.

Fig. 4.25 vividly illustrates the coarse and fine tunability of gain over the modes, clearly showing the extensive and continuous coverage.

In Fig. 4.25.a, the coarse tuning step reveals three distinct 6 dB gain levels. Subsequently, within the fine-tuning step, the gain varies in fine steps, ensuring an overlap between adjacent sensitivity modes. This results in an impressive gain dynamic range of 20 dB as targeted.

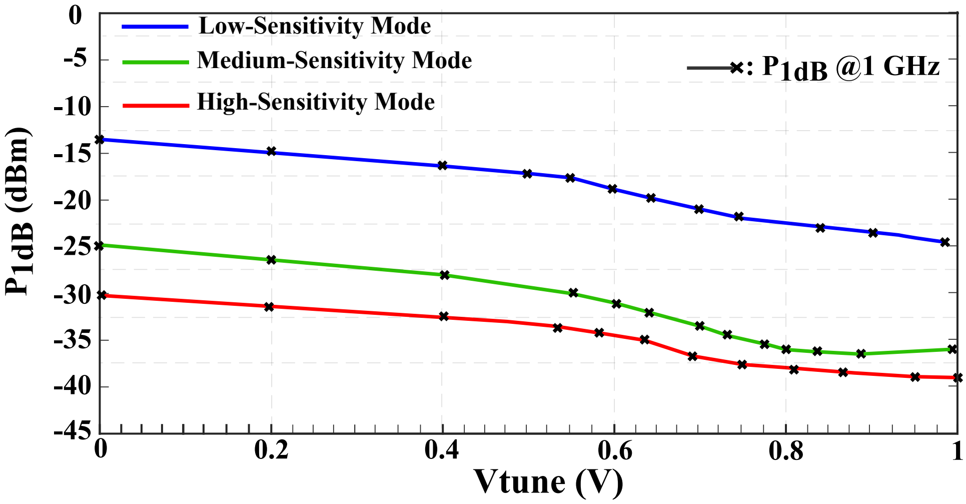


Figure 4.26: Measured P_{1dB} variation with $Vtune$ and tone-frequency across the modes.

To assess the linearity performance, the input compression point P_{1dB} at 1 GHz is measured across a 1 V tuning range of V_{tune}. The intricate details of these measurements are depicted in Fig. 4.26, where the three operational modes showcase their respective P_{1dB} characteristics.

Notably, the low-sensitivity mode, benefiting from its relaxed NF and gain requirements, exhibits the best linearity performance. At the lowest gain setting, achieved with the lowest V_{tune}, this mode demonstrates a P_{1dB} of -15 dBm, aligning with the specified specifications. Fig. 4.27 illustrates the continuous tuning of performance and trade-offs within each sensitivity mode. The use of V_{tune} provides effective control. In discrete operational scenarios, this study aids in selecting the appropriate biasing point to meet corresponding specifications. Remarkably, the measured results highlight the correlation between noise performance, power consumption, gain, and compression point. It clearly indicates that better noise figure can be achieved with higher current consumption, corresponding to higher gain and a lower compression point, as expected analytically.

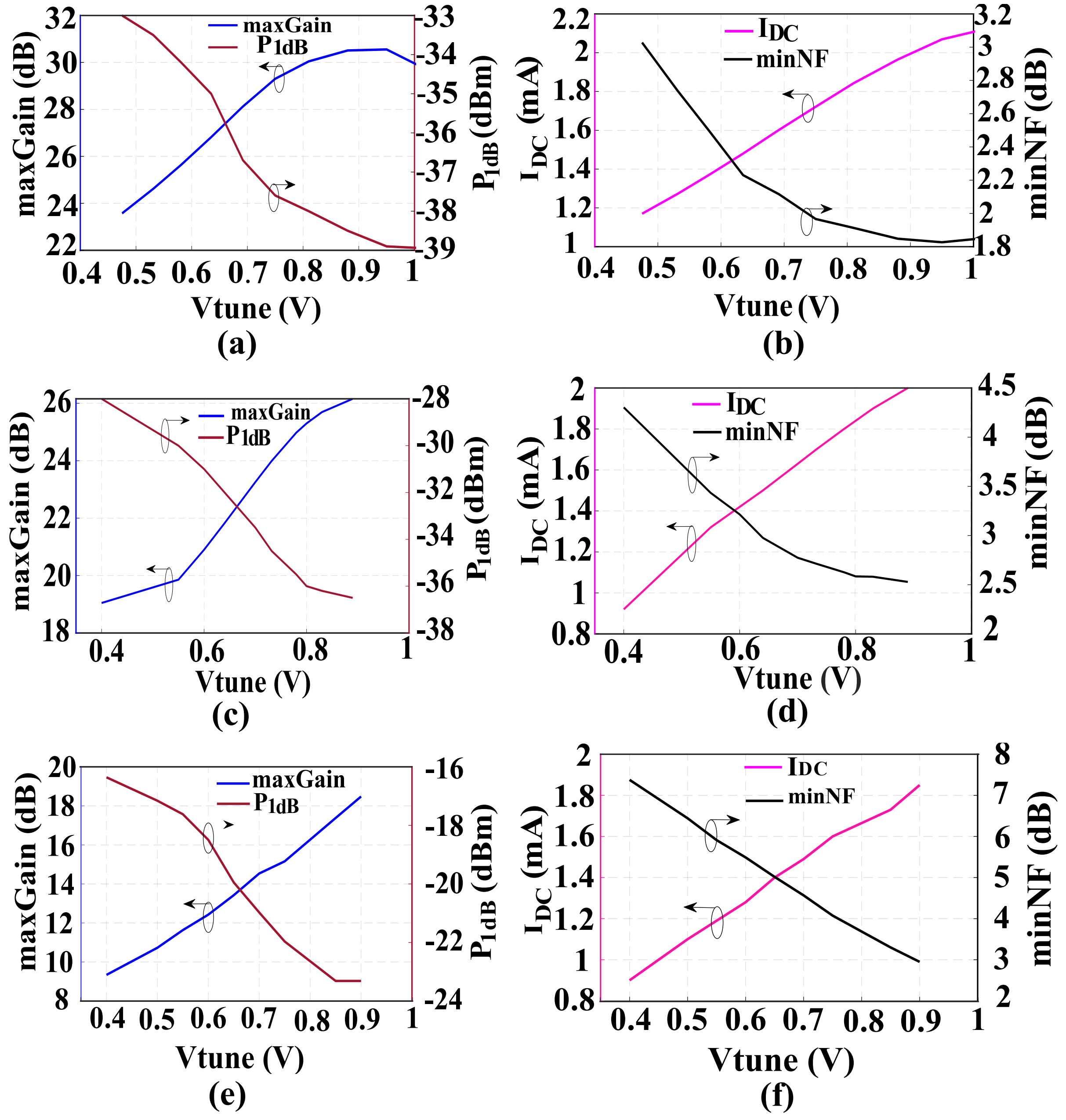


Figure 4.27: Measured performance variation with $Vtune$ over the sensitivity modes. Maximum Gain and P_{1dB} for the high (a), medium (c) and low (e) sensitivity modes, and the minimal noise figure minNF and current consumption IDC for the high (b), medium (d) and low (f) sensitivity mode.

Furthermore, utilizing the V_{tune} voltage as a performance tuning range enables navigation through the design space, exploring different trade-offs.A noteworthy saturation effect becomes apparent at $V_{tune} = 0.9\,\mathrm{V}$, consistent with our design methodology. In fact, the circuit is optimized at 0.9 V for the best achievable performance. For the IIP_3 measurements, a two-tone test at frequencies from 0.5 GHz up to 6 GHz is applied at the LNA input for the three configurations. The variation of IIP_3 concerning both frequency and

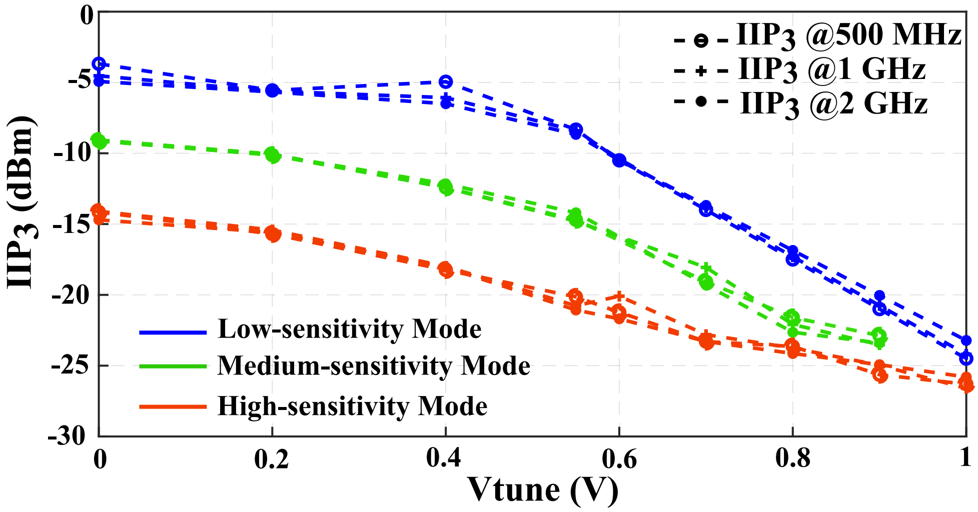


Figure 4.28: Measured IIP_3 variation with $Vtune$ and tone-frequency across the modes.

V_{tune} is depicted in Fig. 4.28. Notably, IIP_3 remains constant across the input frequency spectrum in all three operation modes, affirming the LNA's capability for wideband operation.

The observed decrease in IIP_3 with increasing V_{tune} (corresponding to gain variations) aligns with the relationship described by (4.27). In the low-sensitivity mode, the lowest gain setting exhibits an IIP_3 as high as -6.4 dBm, consistent with the specified selectivity requirements. Conversely, the highest gain point within the high-sensitivity mode represents the worst-case scenario. Fig. 4.29 presents the IIP_3 curves alongside the fundamental and third-order output powers. The obtained IIP_3 value of -25 dBm exceeds the input power amplitudes for which this mode is active ($-115\,\text{dBm} < P_{in} < -60\,\text{dBm}$).

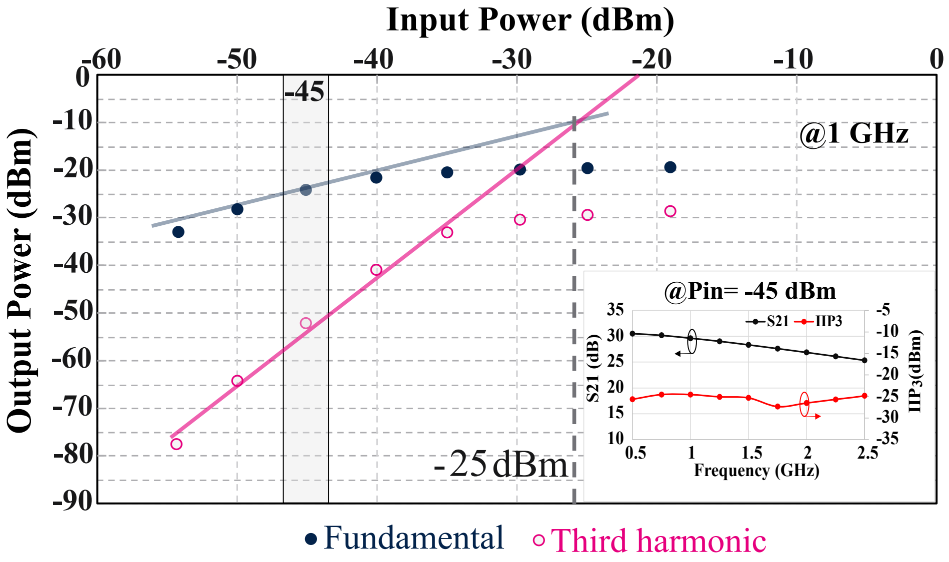


Figure 4.29: Measured IIP_3 @1 GHz for the highest gain point of the LNA.

Consequently, the LNA demonstrates adherence to the linearity requirements across all operational modes.

To verify the stability of the fabricated LNA, Fig. 4.30 shows the K-factor (Kf) derived from the measured S-parameters (LNA plus buffer) for the highest gain (Appendix B.3). The circuit is unconditionally stable as $Kf > 1$.

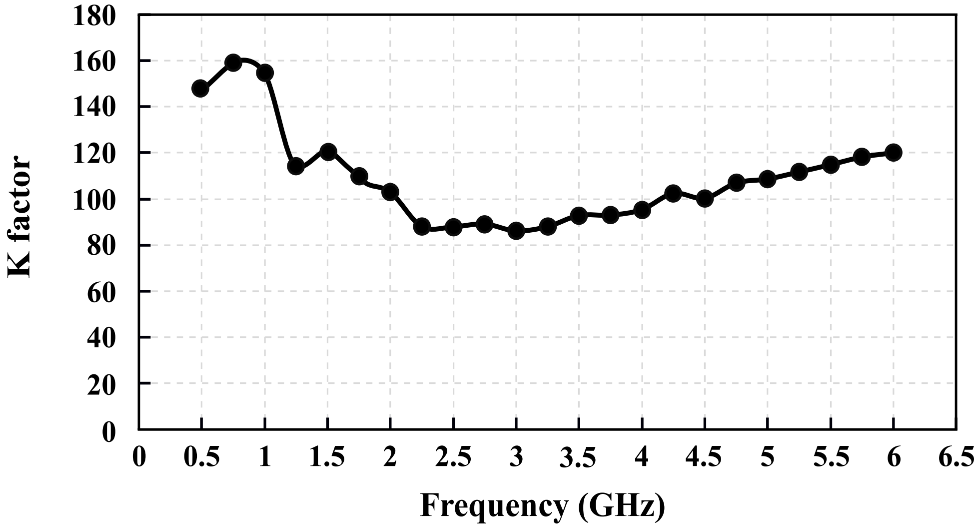


Figure 4.30: Stability factor for the highest gain point of the LNA.

4.9.2 Compatibility with the NB-IoT and LTE-M standards

In this section, we analyze the LNA specifications outlined in Section 4.2 to align with the receiver requirements necessary for adherence to the LTE-M and NB-IoT cellular standards. To validate these specifications, verification tests, assessing the sensitivity and selectivity of the implemented wideband multimode LNA biased according to the first scenario, are conducted.

Sensitivity

The LNA specifications outlined in Section 2.4.1 are detailed based on receiver sensitivity requirements to conform to the LTE-M and NB-IoT cellular standards (Table. 2.2). Deriving from the relationship between the noise figure and sensitivity (2.17), the NF requirements are presented in Table. 4.6.

The minimum measured noise figure is 1.84 dB for the high-gain point in the high-sensitivity mode, and the maximum NF is 7.3 dB obtained for the lowest gain point in the low-sensitivity mode. Notably, even in the LNA configuration addressing high input levels, the NF performance satisfies the sensitivity requirements of both standards across

Table 4.6: Sensitivity-related noise specifications.

Sensitivity/NF	3GPP 36.101 (dBm) / NF (dB)	Best-in-class (dBm) / NF (dB)
NB-IoT	−108.2/ 9.6	−115 / 2.8
LTE-M	−103.7 / 6.5	−108 / 2.3

all measured points. Moreover, it enables achieving sensitivities as low as −115.96 dBm and −108.26 dBm for NB-IoT and LTE-M, respectively.

Selectivity

To ensure adherence to industry standards use cases, the implemented wideband multi-mode LNA undergoes rigorous testing, focusing on selectivity requirements mandated by 3GPP analog specifications. Specifically tailored for LTE-M and NB-IoT receivers, these tests evaluate the receiver's robustness against interference scenarios.

One of the main evaluations is the XMOD test, encompassing both NB-XMOD and CATM1-XMOD standards. This test, conducted in the presence of two blockers, serves as a crucial measure to determine if the receiver satisfies the stringent selectivity requirements outlined by 3GPP.

The detailed test scenarios, reported in Table. 4.7, provide insight into various aspects, including frequencies, power levels, and bandwidths. Notably, fdw represents the down-link frequencies of different bands from both standards, each with distinct bandwidths (0.18 MHz for NB-IoT and 0.72 MHz for LTE-M).

Table 4.7: Selectivity scenarios according to the 3GPP Analog Specifications.

	Blocker 1		Blocker 2		Wanted Signal	
	freq.	power (dBm)	freq.	power (dBm)	freq.	power (dBm)
NB-XMOD	fdw+2.2 MHz	-46	fdw+4.4 MHz	-46	fdw	-96.2
CATM1-XMOD	fdw+2.2 MHz	-46	fdw+4.4 MHz	-46	fdw	-91.7

An indicative criterion for selection is maintaining a third-order intermodulation product ($IM3$) at 16 dB below the required signal. This criterion drives the requirement for the Input Third Order Intercept Point (IIP_3), set at −15.56 dBm and −12.9 dBm for CATM1 and NB-IoT, respectively.

These exhaustive tests are executed in the low-sensitivity mode, designed to meet linearity requirements and to showcase resilience against blockers. The measurements of IIP_3 in the presence of blockers, performed for the frequency bands fdw of the standards, are illustrated in Fig. 4.31. Results for both the lowest gain point (9.3 dB) and the highest gain point (17 dB) within this mode offer a comprehensive view of the receiver's performance under different conditions. This approach demonstrates the versatility and robustness of our wideband multimode LNA.

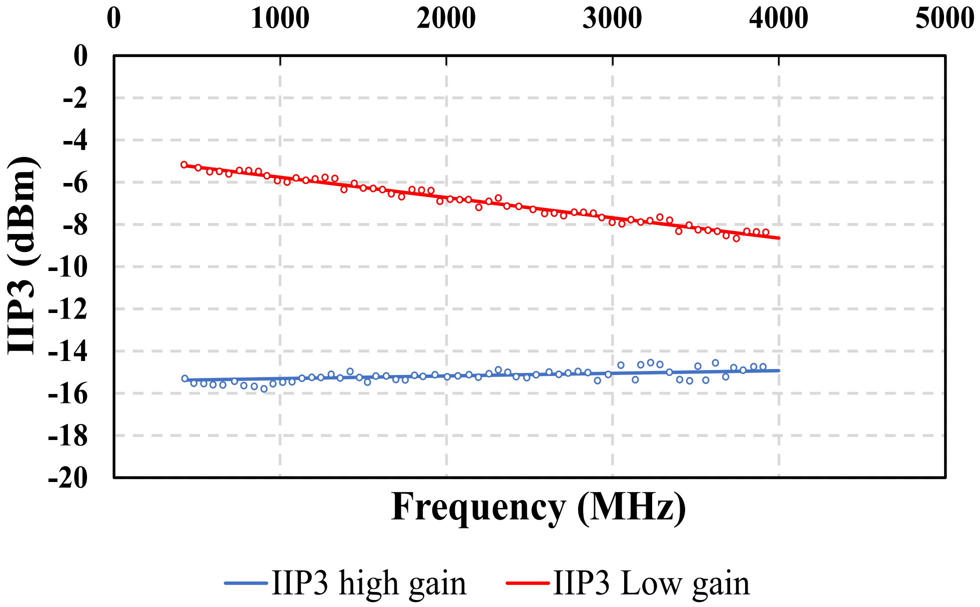


Figure 4.31: Measured IIP_3 within the low-sensitivity mode in XMOD configuration.

As shown in Fig. 4.31, in the worst case scenario (highest gain) the achieved IIP_3 in average is -15 dBm while reaching for some frequencies -17 dBm and -12 dBm, in line with both standards specifications. In the best case scenario, where the gain is lowered to the minimum, the IIP_3 over the frequency bands ranges from -5 dBm to -8 dBm in average, in line with the requirements. As illustrated in Fig. 4.31, under the most demanding conditions (highest gain), the average IIP_3 stands at -15 dBm. Notably, these values align seamlessly with the stringent specifications of both standards.

Conversely, in the optimal scenario where the gain is minimized, the IIP_3 across the frequency bands maintains an average ranging from -5 dBm to -8 dBm. Remarkably, these results of the wideband multimode LNA consistently meet the specified selectivity requirements.

4.9.3 Biasing strategy 2

Working principle

In the context of IoT and sub-6 GHz cellular standards applications, power consumption plays an important role in evaluating receiver performance, alongside sensitivity and noise levels. As detailed in the earlier discussion (Section 4.4), the initial LNA design prioritized achieving the best possible noise figure within a restricted power budget of 2 mW. In this section, the focus shifts towards further minimizing power consumption to mainly target the main deployment bands of the NB-IoT standard with the minimal power budget. This effort is directed towards the development of a sub-mW LNA.

Using the same circuit implementation (Section 4.8), a straightforward approach to achieving the power reduction goal involves adjusting the bias points. By reducing the supply voltage V_{DD}, less current flows through the circuit branches. Consequently, bias adjustments for transistors (M_1, M_n, and M_p) are made to meet saturation conditions, the inversion regime, and small signal parameter values, ensuring proper functionality.

This adjustment is feasible within the fabricated circuit, as per the design methodology, which primarily targeted transistor performance in weak to moderate inversion regions, making them less sensitive to supply reduction.

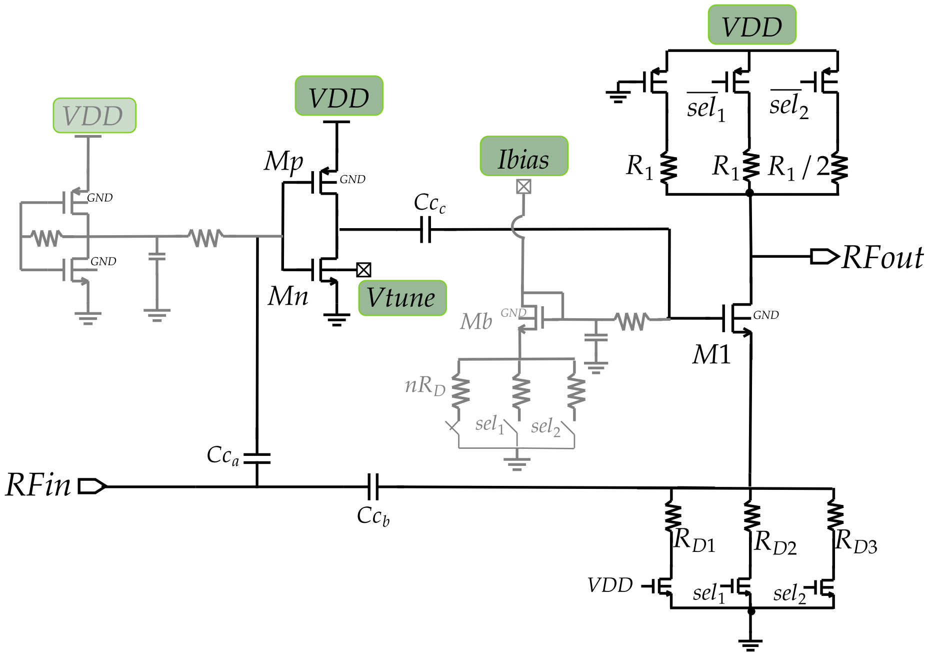


Figure 4.32: LNA complete circuit with highlighted bias tuning knobs.

As depicted in Fig. 4.32, in this design, the bias and inversion coefficient of the CG transistor are controlled externally through the current mirror $M_b - M_1$, modulated by the current *Ibias*. Additionally, the bias and boosting factor (A) of the complementary common source cell (M_n, M_p) are tunable by adjusting the NMOS body-bias voltage $Vtune$. Opting for a V_{DD} of 0.8 V in this phase, ensures sufficient headroom thanks to the intrinsic architecture (maximum stack of 2 transistors) and prevents signal compression at the output, which could negatively impact linearity performance.

However, it is important to note that, as indicated in equations (4.6) and (4.12), reducing the supply voltage not only lowers power consumption but also constrains the bandwidth of the complementary common source and CG branches. The solution can be suitable for ultra-low power NB-IoT receivers since the main deployment bands are in the sub-1.8 GHz (ECC-Report-266, 2017). However, when the same topology targets larger bandwidth specifications (LTE-M) with a single-path wideband circuit, it may be necessary to consider transistor redesign to reduce parasitic capacitances and align with the limited power budget. Alternatively, one can leverage the low power and compact size of our implemented circuit to address different frequency bands of the standards by implementing a multi-path solution.

To explore this modification option, we conducted analytical and post-layout simulations, adjusting the bias for the same gain target. Both coarse and fine tuning steps were verified across three sensitivity modes. Given the reduction in V_{DD}, the ΔV_{BN} range was set to $[0.4, 0.8]$ V to confirm the conditions outlined in (4.28).

Measurement results

The measurement results, along with LNA post-layout simulations (PLS), are detailed to illustrate the performance tunability within each operation mode. By adjusting the $Vtune$ within the specified range, the measured power consumption is reduced to 0.66 mW at $Vtune = V_{DD} = 0.8\,\mathrm{V}$ and as low as 0.37 mW at $Vtune = 0.4\,\mathrm{V}$, which reflects a remarkable power reduction exceeding 60%.

Fig. 4.33 presents the S-parameter measured performances for the three modes at $V_{DD} = 0.8\,\mathrm{V}$, with extreme values of $Vtune$, demonstrating good agreement with PLS. The effectiveness of the bias strategy adjustment is evident in achieving consistent gain values, particularly in comparison to the first biasing scenario. During the fine-tuning step, a gain tuning of more than 6 dB is realized within each mode. Remarkably, a gain dynamic range exceeding 20 dB is observed, ranging from 31 dB to 10.5 dB, similar to the case when $V_{DD} = 0.9\,\mathrm{V}$.

Additionally, a wideband input matching, with $S_{11} < -10\,\mathrm{dB}$, is measured for all gain values across the frequency spectrum beyond 3 GHz. The output matching ($S_{22} < -20\,\mathrm{dB}$) is favorable, thanks to the output buffer, and is less sensitive to LNA performance tuning. The reverse transmission is impressively low at -70 dB. However, it is noteworthy that the 3-dB bandwidth experiences a reduction, as expected, specifically to 1.54 GHz and 3.1 GHz in the high and low sensitivity modes, respectively.

The noise figure measurements, depicted in Fig. 4.34 for three different $Vtune$ values across the three sensitivity modes, exhibit a higher discrepancy in comparison to the PLS

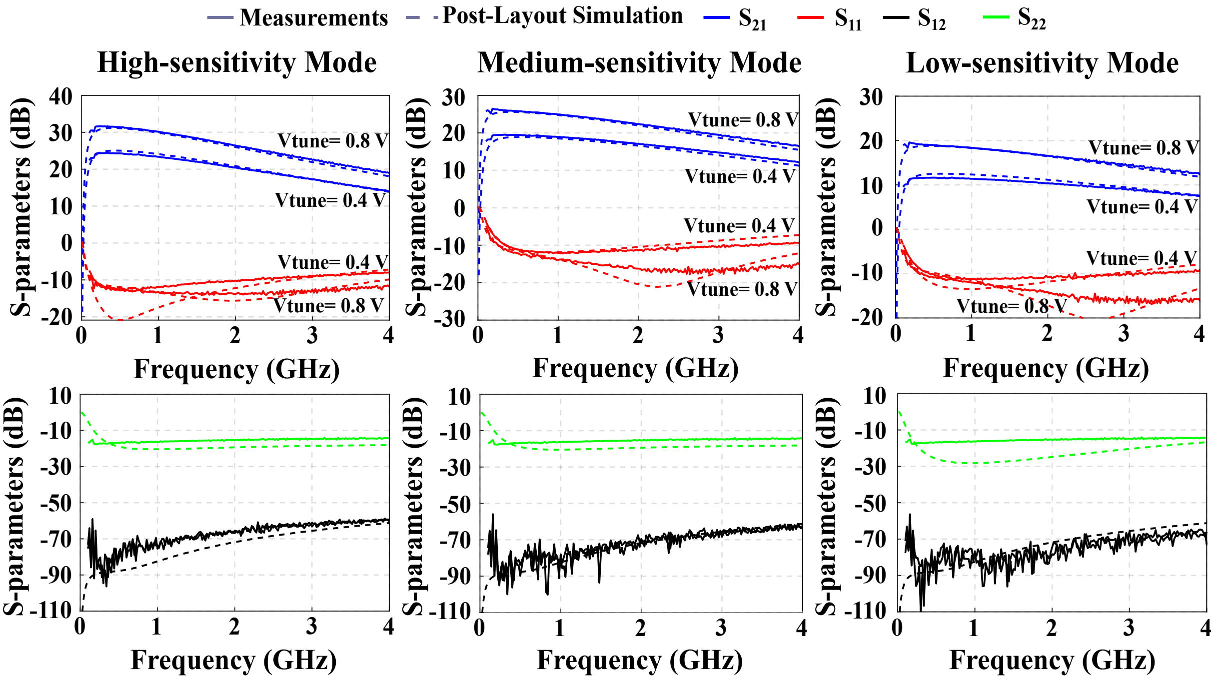


Figure 4.33: PLS and measured Sparameters for the three sensitivity modes with different $Vtune$ values and at $V_{DD} = 0.8\,\mathrm{V}$.

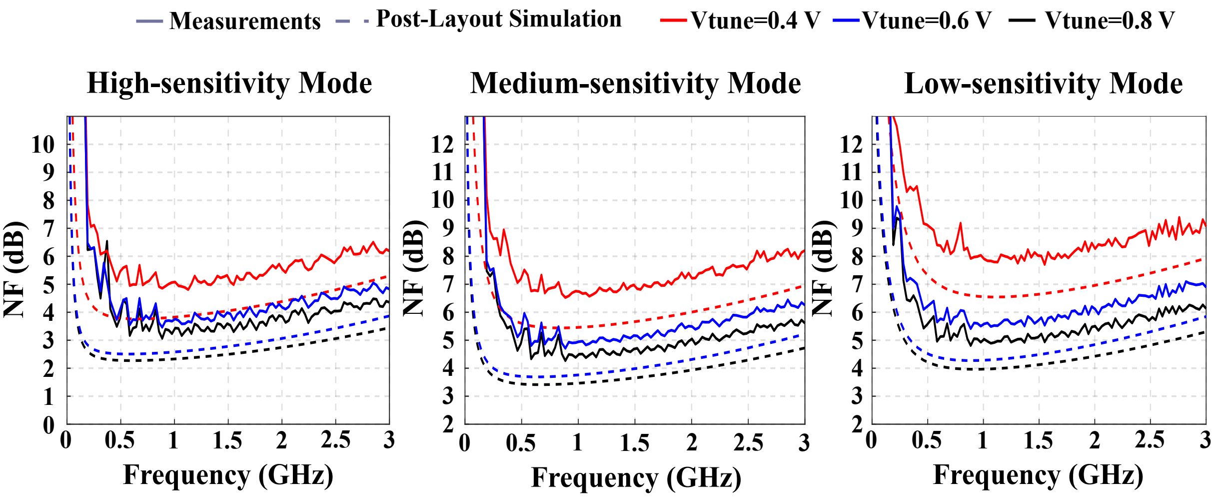


Figure 4.34: PLS and measured NF for the three sensitivity modes with different $Vtune$ values and at $V_{DD} = 0.8\,\mathrm{V}$.

results, particularly when compared with the $V_{DD} = 0.9\,\mathrm{V}$ scenario. This discrepancy can be attributed to a change in equipment between the two sets of measurements. It's important to note that the NF in Fig. 4.24 was measured concurrently with the S-parameters using a PNA-X VNA, while in Fig. 4.34, a Spectrum Analyzer was employed solely for NF measurements.

Despite the equipment change and potential variations, the lowest measured NF stands at 2.95 dB in the high sensitivity mode, increasing to 7.4 dB in the low sensitivity mode.

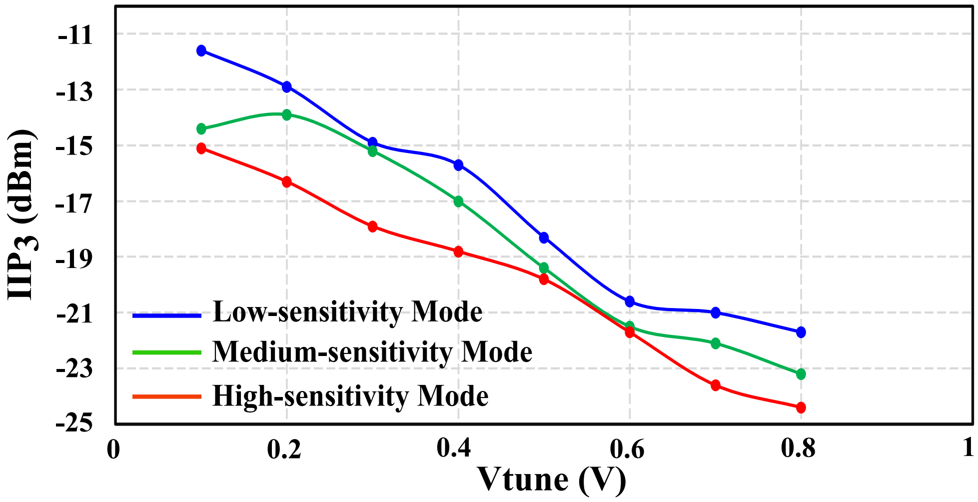


Figure 4.35: Measured IIP_3 @1 GHz for the sensitivity modes for different $Vtune$ at $V_{DD} =$ 0.8 V.

These measured results are deemed acceptable, especially considering the power and gain performance. This establishes a compelling trade-off, maintaining noise within acceptable limits as outlined in Table. 4.6.

For the IIP_3 measurements, we conducted a two-tone test applying frequencies ranging from 0.5 GHz to 6 GHz at the LNA input for the three configurations. Fig. 4.35 shows the variation of IIP_3 concerning V_{tune} at 1 GHz. According to (4.27), IIP_3 decreases with V_{tune} (i.e., with gain), as observed in the first scenario shown in Fig. 4.29. In the low-sensitivity mode, the lowest gain yields an IIP_3 of -11.6 dBm, aligning with the selectivity requirements. The worst-case scenario corresponds to the highest gain point within the high-sensitivity mode.

Fig. 4.36 illustrates the IIP_3 curves with the fundamental and third-order output powers. The resulting $IIP_3 = -24.4$ dBm is higher than the input power amplitudes for which this mode is active (-115 dBm $< P_{in} < -60$ dBm). Hence, also for this ultra-low-power version, the LNA meets the linearity requirements for all the modes.

The measured performance variation with V_{DD} for the same gain, including the bandwidth, is depicted in Fig. 4.37 for three selected gain values. Through careful biasing, maintaining constant g_{m1} and boosting factor A, the complementary common-source characteristics, g_{meq} and g_{dseq}, change along with the current. This phenomenon explains the observed reduction in bandwidth (BW) and an increase in the noise figure. Additionally, as less headroom is allocated for each branch, and the CG inversion coefficient (i.e., g_m/I_D) decreases, it leads to the early compression of the signal for the same power inputs when V_{DD} decreases. The power consumption is aggressively reduced with the decrease in supply voltage, allowing the achievement of the same gain value within each mode for a power consumption as low as 0.27 mW.

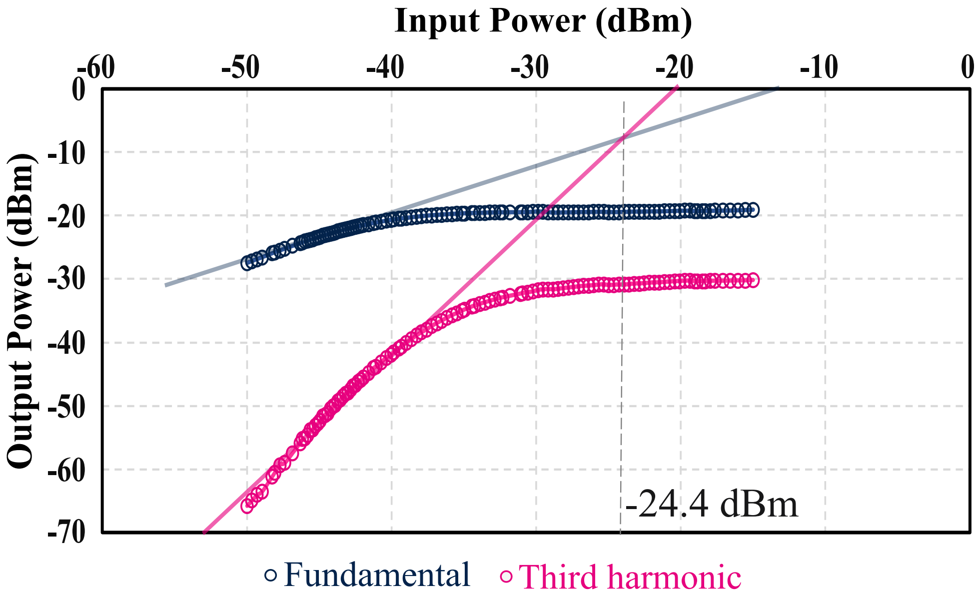


Figure 4.36: Measured IIP_3 @1 GHz for the highest gain point of the LNA at $V_{DD} = 0.8\,\text{V}$.

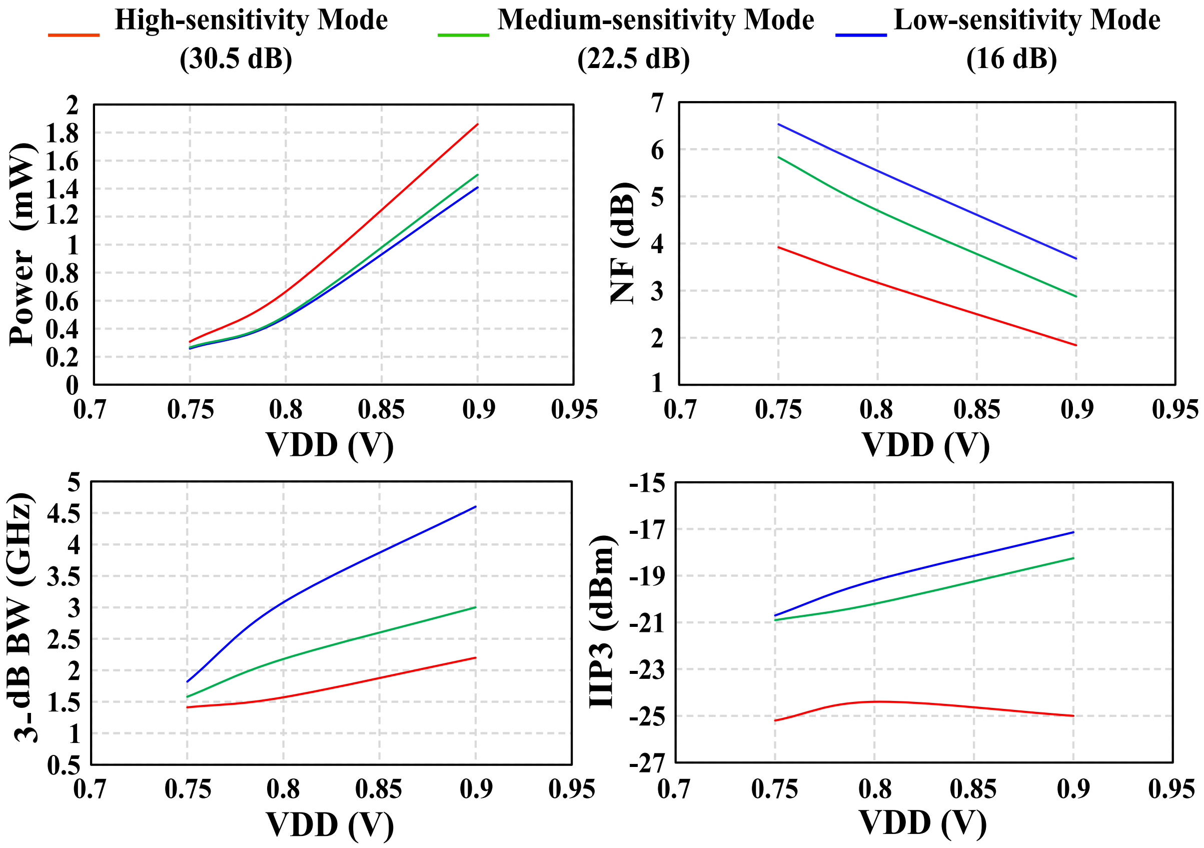


Figure 4.37: Measured performance variation with the supply voltage for the three sensitivity modes at constant gain.

This highlights the potential to implement Multiband LNA circuits with sub-mW power consumption, catering to both NB-IoT and LTE-M and covering all relevant bands.

As illustrated in Fig. 4.37, the 3−dB bandwidth and power consumption decrease but saturates around $V_{DD} = 0.75\,\mathrm{V}$. Further reduction in V_{DD} targeting energy harvesting solutions as a supply source can be explored, at the expense of redesigning the circuit to ensure proper amplifier performance. This aspect is discussed in more detail in Section 5.2.

4.10 Synthesis and comparison with state-of-the-art

4.10.1 Biasing strategy 1

In addition to the circuits discussed in Section 2.3.3, several state-of-the-art solutions incorporating g_m-boost CG LNAs were investigated towards the conclusion of the PhD work in January 2024.

(Zhang et al., 2022) introduced a differential CG LNA using the cross-coupled capacitor (CCC) pair technique and multiple gain loops to increase A. While this approach shows promise in increasing gain, it comes at the cost of requiring the design of multiple inductors, a feature incompatible with the goal of achieving a compact and inductorless circuit.

In the case of (Z. Liu et al., 2023), an inductorless fully differential active g_m-boosted architecture was presented, aiming to reduce the noise figure through a dual feedforward architecture. This design, an extension of the single-ended version in (Z. Liu et al., 2022), incorporates a complementary current-reuse common-source (CS) stage as a boosting amplifier with noise-canceling techniques. The circuit has a compact area of $0.0078\,\mathrm{mm}^2$, reduced power consumption of 3.4 mW, and a minimum NF of 2.7 dB. However, these single-gain-mode solutions do not align with our LNA requirements, which require performance tunability.

In contrast, (Tamura et al., 2020) proposed a multi-mode architecture with a passive boosting circuit to reduce the NF. Another approach is presented in (Taris et al., 2021), featuring an active g_m-boost CG with three discrete gain steps achieved through a transistor switching technique, taking advantage of the *FD-SOI* body-bias feature. Despite a power budget limited to 2 mW, the minimum NF exceeds 3 dB, necessitating multiple control signals for mode switching.

In this work, for the first biasing scenario, a compact wideband single-ended LNA based on a continuously tunable multimode g_m-boost CG architecture is presented. This design achieves a significantly reduced NF in the high-sensitivity mode (sub-2 dB) with a power consumption below 2 mW, while also meeting linearity requirements for the low-sensitivity mode.

Table 4.8: Comparison with State-of-the-art wideband LNAs.

Reference	**This Work (Biasing strategy 1)**			**Access '21 T. Taris et al**			**ISSCC'22 Z. Liu et al**	**JSSC'21 A. Bozorg et al**	**TMTT'11 A. Sobhy et al**	**ESSCIRC'23 Z. Liu et al**
	Mode1	Mode2	Mode3	Mode1	Mode2	Mode3				
Architecture	Active g_m –boost CG			Active g_m –boost CG			Positive feedback CGCS with CM and active feedforward	CGCS with current reuse	CCC CG with positive and negative feedback	Dual-feedforward CGCS
Multimode	Continuous Tunable			Discrete Modes			No	No	No	No
Freq. Band (GHz)	0.5 ... 2.2	0.5 ... 3.1	0.5 ... 5.2	0 ... 4.5	0 ... 5.2	0 ... 4.5	0.2 ... 3	0 ... 4.5	0.1 ... 1.7	0.25...3.7
S11 (dB)	<-10	<-10	<-10	<-7	<-7	<-7	<-12	<-10	<-10	<-10
Gain (dB)	23.5 ... **30.5**	19 ... 26.1	9.3 ... 19	22.9	19.4	16.8	18.6	15.2	23	10.2*
NF (dB)	3 ... **1.84**	4.3 ... 2.5	7.3 ... 3.2	3.6	5.4	6.6	2.7	2.09	1.85	2.4
IIP3 (dBm)	-16 ... -24.5	-13.2 ... -23.4	-6.5 – -20.5	-17.2	-16.8	-16.4	-8.5	-4.6	-2.85	4.1
Power (mW)	1.05 ... **1.86**	1 ... 1.8	0.81 ... 1.68	2	0.9	0.35	3.4	4.5	2.8	7.9
VDD (V)	0.9			1.2	0.9	0.6	1	1	2	1.2
Techno. (nm)	28 FD-SOI			28 FD-SOI			28 CMOS	28 CMOS	90 CMOS	28 CMOS
Silicon Area (mm²)	0.0059			0.0015			0.0078	0.03	0.03	0.021
Biasing condition	Current source and Body bias			Current source and transistor switching			Current source	Off-chip inductor	-	Current source
Type/Nb. Inductors	Single-ended / 0			Single-ended / 0			Single-ended / 0	S.-ended / 1	Diff. /0	Diff. /0
FoM1 (dB)	37.1 ... 29.5	32.7 ... 24	28.5 ... 12.3	27.7	26.8	28	18.2	19.4	23.6	5.64
FoM2 (dB)	80.6 ... 73	76.2 ... 67.4	72 ... 55.8	84.2	83.2	84.4	60.36	49.8	54	39.2

*: $R_L = 25\Omega$

A summary and comparison of the proposed LNA's performance with relevant wideband LNAs from the state-of-the-art are presented in Table. 4.8, where $FoM1$ and $FoM2$ are expressed as,

$$FoM1 = 20log10(\frac{Gain_{(abs)}BW_{GHz}}{Power_{(mW)}(F_{min}-1)}), \tag{4.31}$$

$$FoM2 = 20log10(\frac{Gain_{(abs)}BW_{GHz}}{Power_{(mW)}(F_{min}-1)Area_{(mm^2)}}). \tag{4.32}$$

This work addresses the challenging requirements of minimizing both noise figure (NF) and power consumption, while ensuring adherence to critical linearity specifications. The presented LNA achieves an impressive NF of 1.84 dB, matching the performance of the best-in-class work (Sobhy et al., 2011), but with a remarkable 33% reduction in power consumption. Notably, the inductorless solution competes favorably with the lowest area solution (Taris et al., 2021), demonstrating enhancements in both noise and power consumption features.

The linearity performance of the proposed active g_m-boost CG LNA is on par with the state-of-the-art, particularly in the low-sensitivity mode. This LNA attains a substantial voltage gain of up to 30.5 dB, all while maintaining the previously mentioned low power consumption. To the best of the authors' knowledge, this work marks the first presentation of a wideband sub-6 GHz continuously tunable LNA featuring a gain dynamic range of 20 dB and a sub-2 dB NF.

4.10.2 Biasing strategy 2

Table 4.9: Comparison with State-of-the-art wideband ULV Ultra-low power LNAs.

Reference	**This Work (Biasing strategy 2)**			**Access '21 T. Taris et al**			**TMTT'16 M. Parvizi et al**	**VLSI'15 M. Parvizi et al**	**ISLPED'17 J. Zaini et al**	**LMWC'17 H. Liu et al**
	Mode1	Mode2	Mode3	Mode1	Mode2	Mode3				
Architecture	Active g_m –boost CG			Active g_m –boost CG			Compl. CGCS	Compl. CS RF	Active g_m –boost CG	Triple CCC CG
Multimode	Continuous Tunable			Discrete Modes			No	No	Discrete	No
Freq. Band (GHz)	0.1 … 1.62	0.1 … 2.4	0.1 ... 3.3	0 … 4.5	0 … 5.2	0 … 4.5	0.1 … 2.2	0.1 … 7	0.4 … 6	0.4…1
S11 (dB)	<-10	<-10	<-10	<-7	<-7	<-7	<-10	<-10	<-10	<-10
Gain (dB)	23 … **30.5**	19.5 … 25.5	11.6 … 19.5	22.9	19.4	16.8	12.3	12.6	16.8 … 21.5	18
NF (dB)	4.5 … **2.9**	6.3 … **3.9**	7.4 … 4.5	3.6	5.4	6.6	5.5	6.5	7.3 … 6.3	4.2
IIP3 (dBm)	-18.8 … -24.4	-17 … -23.2	**-11.4 –** -21.5	-17.2	-16.8	-16.4	-11.5	-8	-16	-14
Power (mW)	**0.36 … 0.66**	**0.37** … **0.66**	**0.37** … **0.66**	2	0.9	0.35	0.4	0.75	0.3 … 0.9	0.2
VDD (V)	**0.8**			1.2	0.9	0.6	1	0.5	0.6 … 1	1
Techno. (nm)	28 FD-SOI			28 FD-SOI			130 CMOS	90 CMOS	28 FD-SOI	180 CMOS
Silicon Area (mm²)	0.0059			0.0015			0.0052	0.23	0.0015	0.27
Type/Nb. Inductors	Single-ended / 0			Single-ended / 0			S-E / 0	S.-E/ 2	S-E /0	Diff. /0
FoM1 (dB)	**31.1 … 38.2**	**25.1… 32.9**	**18.2 … 28**	27.7	26.8	28	18.57	21.2	29.4…27	23.3
FoM2 (dB)	76…82.8	**70.7… 77.6**	**62.8… 72.6**	84.2	83.2	84.4	64.25	34	85.8…83.5	34.7

Compl.: Complementary, CCC: Cross-Coupled Capacitor, S-E: Single-Ended

The performance of the sub-mW power consumption version of the continuously tunable multimode wideband LNA is summarized and compared with relevant ultra-low-power wideband LNAs in Table. 4.9.

This inductorless design aligns with the lowest reported power consumptions (Parvizi et al., 2016), (Parvizi et al., 2015), (Zaini et al., 2017) while achieving higher gain and lower noise figure, thanks to the g_m-boosting technique and performance tunability. In (H.-J. Liu & Zhang, 2017), power consumption of up to 0.2 mW is measured, but this comes at the expense of a narrower bandwidth, limited to 1 GHz. Through a comprehensive comparison based on figures of merit ($FoM1$ and $FoM2$), this ultra-low-power version stands out favorably relative to the state-of-the-art.

4.11 Conclusion

This part presents the design and implementation of an inductorless wideband continuously tunable LNA, achieving state-of-the-art performance. A comprehensive design methodology and analytical description, are used to navigate through a large design space. The approach is based on a simple $6-$DC parameters-based transistor model, effectively addressing the short channel effects of advanced technologies together with the non-linearity aspects.

A distinctive feature of this design lies in its utilization of the body bias terminal within the 28 nm *FD-SOI* CMOS technology. This enables fine-tuning of the LNA's performance across a broad operational range. The proposed LNA is strategically designed to cater to the NB-IoT and LTE-M 5G cellular standards, aligning with the demands of contemporary communication systems.

Two versions of the multimode LNA are introduced, both targeting a 20 dB gain dynamic. Through proper bias adjustment, this device proves versatile, accommodating varied applications. In the first scenario, the focus is on achieving a low noise figure over a wideband, all within a power budget limited to 2 mW. In the second scenario, the emphasis shifts to sub-mW power consumption for lower bandwidth (sub-2 GHz) applications such as the main deployment bands of NB-IoT.

The silicon measurements affirm the success of the approach, showing positive comparisons with the state-of-the-art in both cases. This confirms the effectiveness of the design methodology and the practicality of the inductorless wideband continuously tunable LNA in addressing the evolving requirements of modern wireless communication standards.

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Chapter 5

General conclusions and perspectives

Contents

5.1 General conclusions

The main objective of this thesis consisted in the design of a wideband tunable multi-mode inductorless Low Noise Amplifier (LNA) in the 28 nm *FD-SOI* CMOS technology, targeting the strict requirements of 5G LTE-M and NB-IoT cellular standards. To fulfill this goal, the design strategy involved various steps as follows:

At the beginning of the thesis, a comprehensive review of wideband sub-6 GHz LNAs was conducted, including an analysis of over 200 circuits from the literature (Bouchoucha, Coustans, et al., 2023). Theoretical analyses and statistical comparisons of relevant LNA topologies were performed to narrow down the choices for architectures suitable for challenging applications such as the NB-IoT and LTE cellular standards receivers.

The analysis involved direct performance comparisons between common wideband LNA topologies and complex design enhancement solutions, that are hard to be described and compared by simple analytical systems. For low power applications, advanced techniques are applied to the common-gate (CG) topology to improve its noise figure. It is shown that the gm-boosting CG structure achieves a good trade-off between noise, power consumption, and gain, and better performance on average than the conventional noise-canceling structure CGCS. Also the complementary common source circuit achieves an interesting compromise between linearity, gain and noise together with the current reuse technique.

Then, to target the best energy-efficient optimized circuit for the given set of specifications, a design methodology based on the g_m/I_D and the inversion coefficient has been proposed.

This generic design method, requires a complete circuit description complemented by an accurate and simple transistor model that considers the main short-channel effects and performance variations dependent on drain voltage.

Hence, a new version of a charge-based, design-oriented model (Neto, Adotnes, et al., 2023), (Neto, Bouchoucha, et al., 2023) based on 5 to 6 DC parameters (5PM/6PM), was introduced. This model comprises single-piece DC and small-signal equations derived from fundamental physics. Notably, the impact of velocity saturation is incorporated into the charge control equation through the saturation carrier charge. This design choice aims to eliminate the need for defining a saturation voltage and employing interpolation functions to link the triode and saturation regions, a characteristic of previous versions (Pino-Monroy et al., 2022), (Pino-Monroy et al., 2023). The proposed 5PM for bulk and 6PM for *FD-SOI* has been rigorously validated with respect to measurement results and circuit simulations, specifically for RF LNA circuits implemented in the 28 nm *FD-SOI* CMOS technology.

A proof of concept was presented through a design method using a g_m/I_D and inversion level approach suitable for low-power LNAs in advanced technologies. This methodology directly linked transistor bias conditions and size to key LNA performances thanks to the 5PM/6PM model, introducing analytical modeling of LNA non-linearity for the first time. Two common architectures have been employed as demonstrators. First, a resistive feedback LNA (Bouchoucha, Pino-Monroy, et al., 2023a) (Bouchoucha, Pino Monroy, et al., 2023b) with three design examples for different drain voltages were detailed. Then, a common-gate LNA (Neto, Bouchoucha, et al., 2023) achieved a good linearity thanks to the design space exploration with the body-bias feature. Employing these methodologies, the suitable inversion level of the transistor and the sizes of passive components were systematically determined to meet gain, noise figure, and linearity specifications within a constrained sub-1mW power budget. Comparative analysis of analytical and simulated performances validated the accuracy of the proposed methodology.

This efficient strategy, rooted in simple analytical calculations, significantly reduced design time compared to CAD-based approaches typically used in advanced technologies. As articulated in the main objectives, the design methodology fulfilled the target of the best energy-efficient optimized circuit for a given set of specifications.

The design and implementation of an inductorless wideband continuously tunable

LNA have been presented (Bouchoucha, Barragan, et al., 2023), based on the comprehensive design methodology together with analytical description. The method employed the simple 6PM proposed model to fully describe the transistor. This design takes advantage of the body bias terminal in the 28 nm *FD-SOI* CMOS technology to fine-tune the LNA performance over a wide operation range. The design covers an extensive design space through the implementation of both coarse and continuous fine-tuning mechanisms. Coarse tuning caters to three sensitivity modes, while the *FD-SOI* body biasing feature enables continuous fine-tuning for each mode. Notably, the LNA had a highly compact area without the need for external components. Proper bias adjustment has allowed multiple use of this device targeting different trade-offs. In effect, two biasing strategies were presented. In terms of performance, the measurements for both versions reveal state-of-the-art results, including a gain dynamic exceeding 20 dB, from 10 dB to 30 dB. In the first biasing scenario, the circuit achieves a sub-2 dB noise figure with a power consumption of less than 2 mW, and linearity on par with current state-of-the-art LNAs. Consequently, the LNA enables a RX sensitivity ranging from -115 dBm to -25 dBm. While the second case targeted sub−mW power consumption for lower bandwidth (sub-2 GHz) applications such as the main deployment bands of NB-IoT and ultra-low power IoT systems. Furthermore, the presented 28 nm *FD-SOI* CMOS LNA stands as a versatile and robust solution for advanced sub-6 GHz wireless communication in modern applications such as IoT thanks to its adherence to 5G NB-IoT and LTE-M specifications.

5.2 Perspectives

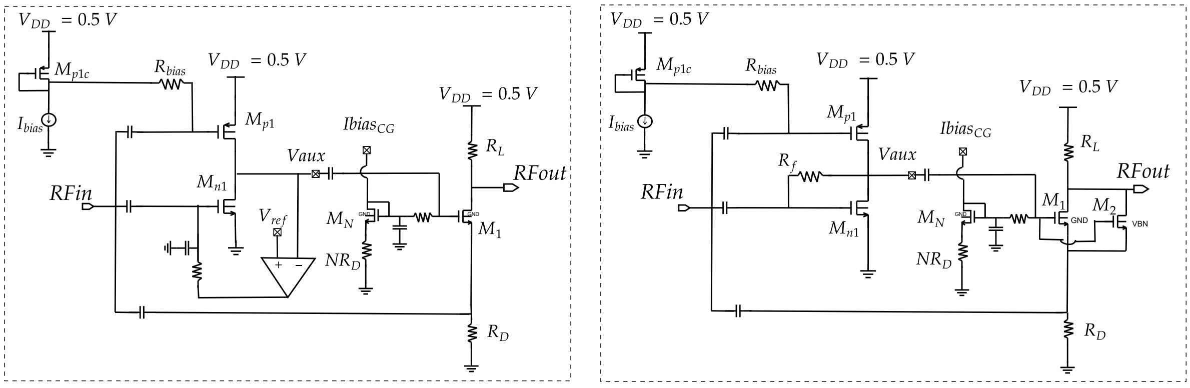
- **Complete transistor Model**

Many efforts are dedicated to implement the dynamic behavior of the transistor in the proposed model. It is validated for bulk technologies. As an improvement axis to complete the model cell used for our RF design methodologies and simulations in 28 nm *FD-SOI* technology, the model of the capacitances including the intrinsic and extrinsic ones should be validated. This will open the door for comprehensive fully analytical methodologies for analog and wideband RF circuits avoiding the need for LUT. Moreover, the inclusion of inversion-coefficient noise analysis completes this charge-based model.

Besides, a review of the implemented parameters could be considered to cover other regions for different applications. A possible combination between the proposed model and the 7PM version could provide a solution convenient with full scale usage.

- **Ultra low voltage LNA version with DC control loop**

In the context of ultra-low power and ultra-low voltage applications using energy harvesting sources, a further reduction in the supply voltage of the LNA can be considered. The proposed gm-boost LNA can be redesigned for $V_{DD} = 0.5\,\mathrm{V}$ which is half the nominal value of the technology. For accurate functionality and performance control, different bias techniques can be used.

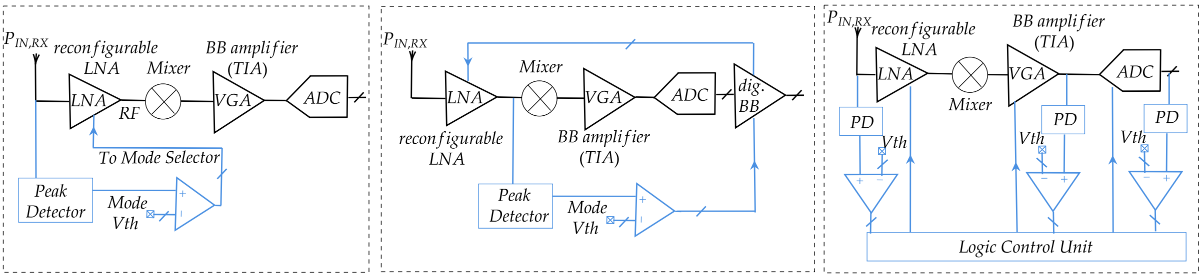


(a) (b)

Figure 5.1: Possible implementations of the ULV LNA. a. using an OTA as DC control loop. b. Using resistive feedback for bias and CG multiple gate control for linearity.

Several solutions exist as DC control loop to set the complementary common source bias at a nominal voltage. The PMOS amplifier is biased through a current source, while the NMOS is set through the DC feedback. A simple option consists in using a PMOS differential pair 5T OTA. It compares the DC output of the complementary CS to $V_{ref} = V_{DD}/2$ to give the appropriate gate voltage as shown in Fig. 5.1.a. Due to the stack of 3 transistors and to satisfy the functionality of the differential pair under a low supply voltage of 0.5 V extreme body bias is applied to the transistors to reduce V_T. Also we can bias the OTA with higher supply assuming that a higher source exists in the SoC or a charge pump provides a higher voltage in proximity. An alternative option consists in biasing the NMOS through the resistive feedback configuration as shown in Fig. 5.1.b. This will reduce the area and complexity of the solution while relaxing a little the precision constraints of the DC control. Both solutions were verified at schematic level together with corners and process variation simulations. The designed solution can achieve a gain as high as 26 dB with a NF of 3.1 dB. The power consumption is $530\,\mu\mathrm{W}$ only while the $IIP_3 = -20\,\mathrm{dBm}$. As shown in Fig. 5.1.b, further improvement of the linearity performance could be obtained by implementing a multiple gate CG transistor. The idea consists in implementing the CG transistor with 2 equally-sized transistors in parallel sharing the 3 terminals. However, the body bias voltage is different to bias them in two different inversion regions. The dominant transistors sets the g_m and current while the second cancels the g_{m3} of the former.

- **Automatic gain control AGC**



(a) (b) (c)

Figure 5.2: Block diagram of the wideband receiver. a. analog gain control. b. digital gain control. c. Analog-Digital gain control.

As a continuity of this work, the design of the full wideband receiver including our continuous multimode LNA could be considered. Several block diagrams can be proposed including automatic gain control (AGC) mechanisms. This relies on designing a peak detector that senses the signal level to be compared to the mode's threshold voltages to directly control the mode selector cell. Several solutions can be investigated for this concern as shown in Fig. 5.2. A direct analog solution is shown in Fig. 5.2.a. consists on adding a LNA replica at the input. The noise and power penalty should be carefully considered. A digital solution in Fig. 5.2.b. relies on signal sensing at the output of the LNA to reduce the noise effect and control through a digital baseband amplifier. In Fig. 5.2.c, a combination between analog and digital implementation. A logic control unit can be used to generate the appropriate feedback signals to the LNA, baseband amplifier and ADC.

5.3 List of publications

The contributions from this work have resulted in several journal and conference publications, covering several topics ranging from the state-of-the-art analysis to different versions of the transistor model and design methodologies applied to specific LNAs (Bourdel et al., 2021), (Bouchoucha, Pino-Monroy, et al., 2023a), and the full gm-boost CG circuit implementation.

- **M. K. Bouchoucha**, M. J. Barragan, A. Cathelin and S. Bourdel, "A wideband sub-6GHz continuously tunable gm-boosted CG Low Noise Amplifier in 28 nm FD-SOI CMOS technology," *IEEE 49th European Solid State Circuits Conference, ESSCIRC 2023*, Lisbon, Portugal, 2023, pp. 381-384.

- **M. K. Bouchoucha**, D. A. Pino-Monroy, P. Scheer, P. Cathelin, J.-M.Fournier, M. J. Barragan, A. Cathelin, and S. Bourdel, "Resistive Feedback LNA design using a 7-parameter design-oriented model for advanced technologies," *56th IEEE International Symposium on Circuits and Systems (ISCAS 2023), Monterey, CA, USA*, 2023, pp. 1-5.

- **M. K. Bouchoucha**, M. Coustans, M. Barragan, A. Cathelin, A. and S. Bourdel, Performance benchmark of State-of-the-art Sub-6-GHz wideband LNAs Based on an Extensive Survey, *56th IEEE International Symposium On Circuits And Systems (ISCAS 2023).* pp. 1-5, Monterrey, CA, USA, May 2023.

- D.Neto, C. Adornes, G. Maranhao, **M. K. Bouchoucha**, M. J. Barragan, A. Cathelin, M. C. Schneider, S. Bourdel and C. Galup-Montoro , "A 5-DC-parameter MOSFET model for circuit simulation in QucsStudio and SPECTRE," *21st IEEE Interregional NEWCAS Conference (NEWCAS 2023)*, Edinburgh, United Kingdom, 2023, pp. 1-5. **Best Paper Award**.

- D. Pino-Monroy, P. Scheer, **M. K. Bouchoucha**, C. Galup-Montoro, M. J. Barragan, P. Cathelin, J-M. Fournier, A. Cathelin and S. Bourdel, "Design-oriented model for short-channel MOS transistors based on inversion charge," *IEEE 14th Latin America Symposium on Circuits and Systems (LASCAS 2023)*, Quito, Ecuador, 2023, pp. 1-4.

- D. Pino-Monroy, P. Scheer, **M. K. Bouchoucha**, C. Galup-Montoro, M. J. Barragan, P. Cathelin, J-M. Fournier, A. Cathelin and S. Bourdel, "Design-oriented all-regime all-region 7-parameter short-channel MOSFET model based on inversion charge". *IEEE Access.* **10** pp. 86270-86285, 2022.

- S. Bourdel, S. Subias, M. K. Bouchoucha, M. J. Barragan, A. Cathelin and C. Galup, "A gm/ID Design Methodology for 28 nm FD-SOI CMOS Resistive Feedback LNAs," 2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Dubai, United Arab Emirates, 2021, pp. 1-4.

Submitted to journals and under review:

- **M. K. Bouchoucha**, D.A.PinoMonroy, P.Scheer, J.M.Fournier, P.Cathelin, C.Galup, M.J.Barragan, A.Cathelin, S.Bourdel “Analytical Design Methodology for Resistive Feedback LNAs using a Charge-Based Transistor Model Accounting for gm Non-Linearity”, *Submitted for IEEE TCAS-I 2023*, (14 pages).
- D.Neto, **M. K. Bouchoucha**, G. Maranhao, M. J. Barragan, A. Cathelin, M. C. Schneider, S. Bourdel and C. Galup-Montoro, "Design-oriented single-piece 5-DC-parameter MOSFET model", *Accepted: IEEE Access June 2024*, (19 pages).

Appendix A

Appendix A: 443 Algorithm

Here is shown an example of a MATLAB and a Verilog-A code that can be easily implemented in cadence for simulation comparison between the proposed model and the PDK characteristics. The example showns the implementation for a common source NMOS transistor. **Matlab code**

```
function[ID,qs,qd,id]=model5PM6PM_443algo_DC(n,Is0,vt0,sigma,zeta,delta,vg,vd,vs,vb)
ut=25.85e-3;
for g=1:length(vg)
for d=1:length(vd)
for b=1:length(vb)
vp=(vg(g)-vt0+sigma*vd(d)+delta*vb(b))/n;
%eq.1 pinch off voltage
vds=vd(d)-vs;
if (vds>0)
% qs solving
XS = exp (((vp-vs)/ut)+1);
else
XS = exp (((vp-vd(d))/ut)+1);
end
if(XS < 0.7385)
numXS = XS + (4/3)* XS*XS;
denomXS = 1 + (7/3)* XS +(5/6)* XS*XS;
Wns = numXS / denomXS ;
else
numXS = 24*(log(XS)* log(XS)+2* log(XS) -3);
denomXS = 7* log(XS)* log(XS) + 58* log(XS) +127;
Wns = log(XS) - ( numXS/ denomXS );
end
```

```
%Calcul Zns
Zns = log (XS) - Wns - log(Wns);
% Calcul Ens
Ens = (Zns/(1+Wns)) *( ((2*(1+ Wns)*(1+ Wns +(2/3)* Zns) -Zns)) / (2*(1+ Wns)*(1+
Wns +(2/3)* Zns ) -2* Zns));
% Find qs
qsi(g)= Wns *(1+ Ens );
%Find qsat
qdsat(g)=qsi(g)+1+1/zeta-sqrt((1+1/zeta)2̂+2*qsi(g)/zeta);
if (vds>0)
% qs solving
XD = (((qsi(g)-qdsat(g)))*exp(-vds/ut)*exp(qsi(g)-qdsat(g)) );
else
XD = (((qsi(g)-qdsat(g)))*exp(vds/ut)*exp(qsi(g)-qdsat(g)) );
end
if(XD < 0.7385)
numXD= XD + (4/3)* (XD).*(XD);
denomXD = 1 + (7/3)* XD +(5/6)* (XD)*(XD);
Wnd = numXD / denomXD ;
else
numXD = 24*(log(XD)* log(XD)+2* log(XD) -3);
denomXD = 7* log(XD)* log(XD) + 58* log(XD) +127;
Wnd = log(XD) - ( numXD / denomXD );
end
%Calcul Znq
Znd = log (XD) - Wnd - log(Wnd);
% Calcul Enq
End = (Znd/(1+Wnd)) *( ((2*(1+ Wnd)*(1+ Wnd +(2/3)* Znd) -Znd)) / (2*(1+ Wnd
)*(1+ Wnd +(2/3)* Znd ) -2* Znd));
% Find qd
qdi(g) = Wnd *(1+ End )+qdsat(g);
if (vds>0)
qs(g)=qsi(g);
qd(g)=qdi(g);
else
qs(g)=qdi(g);
qd(g)=qsi(g);
```

```
end
% ID
ID(g,d,b)=Is0*(qs(g)-qd(g))*(qs(g)+qd(g)+2)/(1+zeta*(qs(g)-qd(g)));
id(g,d,b)=ID(g,d,b)/Is0;
end
end
end
```

Verilog-A code

```
module nmos_5_6PM(D, G, S, B); // pinout definition inout D,G,S,B; // electrical nodes definition electrical D,G,S,B; // user parameters
(*desc= “Channel width”, units = “m”, type = “instance”*) parameter real W = 1e-6 from [0:inf];
(*desc= “Channel length”, units = “m”, type = “instance”*) parameter real L = 1e-6 from [0:inf];
(*desc= “Slope factor”, type = “instance”*) parameter real n = 1.2 from [1:3];
(*desc= “Specific current”, units = “A”, type = “instance”*) parameter real IS = 1e-6 from [0:inf];
(*desc= “Threshold voltage”, units = “V”, type = “instance”*) parameter real VT0 = 0.5 from [0:inf];
(*desc= “Sigma”, type = “instance”*) parameter real sigma = 0.02 from [0:inf];
(*desc= “Zeta”, type = “instance”*) parameter real zeta = 0.02 from [0:inf];
(*desc= “Delta”, type = “instance”*) parameter real delta = 0.0 from [0:inf];
(*desc= “LVTorRVT”, type = “instance”*) parameter real lvt =1 from [-1:1] ;
// Intern variables
real VP, PhiT, ut, VX;
real X,numeratorS, denominatorS, TermC, numeratorES, denominatorES, ZnS, EnS, WnS, q1, qS;
real qsat, qidsat, vsat;
real Y, numeratorD, denominatorD, TermD, numeratorED, denominatorED, ZnD, EnD, WnD, q2, qD;
real id, ID;
real mob, Cox, tox, e0, eox;
real gm_frac1, gm_frac2, gm_frac3;
real gms,gmd, gm, gg, gg2, gm2, gm3, gmsat;
real alpha;
real alpha_frac, alpha_frac2, alpha_frac3;
real QI, QD, QS, QG, QB;
```

```
real Cgso, Cgdo, Cgbo, Cbso, Cbdo, Cdso, Csdo;
real Cgd, Cgs, Cgb, Cbs, Cbd, Cds, Csd, Cm;
real epsi;
real qdfin, qs;
analog begin
PhiT = $vt($temperature);
ut= $vt($temperature);
VP = (V(G,S) - VT0 + sigma*V(D,S) + sigma*V(S,S)+ lvt*delta*V(B,S) )/n;
tox = 3.98e-9;
e0 = 8.85e-12;
eox = 3.9;
Cox = (eox*e0)/tox;
mob = (IS*L)/(Cox*n*PhiT*PhiT*W*0.5); //mobility [m^2/V.s]
vsat = (mob*PhiT)/(L*zeta); //[m^2/s]
//epsi = 0.1;
epsi=0;
////qS from algorithm 443 and UCCM
if (V(D,S) >= 0) begin
X = exp(((VP - V(S,S))/PhiT)+1.0);
end
else begin
X = exp(((VP - V(D,S))/PhiT)+1.0);
end
if(X < 0.7385) begin
numeratorS = X + (4.0/3.0)*X*X;
denominatorS = 1.0 + (7.0/3.0)*X+(5.0/6.0)*X*X;
WnS = numeratorS/denominatorS;
end
else begin
numeratorS = ln(X)*ln(X)+2.0*ln(X)-3.0;
denominatorS = 7.0*ln(X)*ln(X) + 58.0*ln(X) +127.0;
WnS = ln(X) - 24.0*(numeratorS/denominatorS);
end
ZnS = ln(X) - WnS - ln(WnS);
TermC = ZnS/(1.0 + WnS);
numeratorES = 2.0*(1.0+WnS)*(1.0+WnS+(2.0/3.0)*ZnS)-ZnS;
denominatorES = 2.0*(1.0+WnS)*(1.0+WnS+(2.0/3.0)*ZnS)-2.0*ZnS;
```

```
EnS = TermC*(numeratorES/denominatorES);
q1 = WnS*(1.0+EnS);
//Calculating qdsat
qsat = q1 + 1.0 + (1.0/zeta) - sqrt(((1+(1/zeta))*(1+(1/zeta)))+((2*q1)/zeta));
////qD from algorithm 443 and UCCM
if (V(D,S) >= 0) begin
Y = (((q1-qsat))*exp(-V(D,S)/(PhiT))*exp(q1-qsat));
end
else begin
Y = (((q1-qsat))*exp(-V(S,D)/(PhiT))*exp(q1-qsat));
end
if(Y < 0.7385) begin
numeratorD = Y + (4.0/3.0)*Y*Y;
denominatorD = 1.0 + (7.0/3.0)*Y+(5.0/6.0)*Y*Y;
WnD = numeratorD/denominatorD;
end
else begin
numeratorD = ln(Y)*ln(Y)+2.0*ln(Y)-3.0;
denominatorD = 7.0*ln(Y)*ln(Y) + 58.0*ln(Y) +127.0;
WnD = ln(Y) - 24.0*(numeratorD/denominatorD);
end
ZnD = ln(Y) -WnD - ln(WnD);
TermD = ZnD/(1.0 + WnD);
numeratorED = 2.0*(1.0+WnD)*(1.0+WnD+(2.0/3.0)*ZnD)-ZnD;
denominatorED = 2.0*(1.0+WnD)*(1.0+WnD+(2.0/3.0)*ZnD)-2*ZnD;
EnD = TermD*(numeratorED/denominatorED);
q2 = (WnD*(1+EnD)) + qsat;
//Normalized densities charges for a symmetric model
if (V(D,S) >= 0) begin
qS = q1;
qD = q2;
end
else begin
qD = q1;
qS = q2;
end
///////////// Calculating Drain Current ID //////////////////////
```

```
id = ((qD+qS+2.0)/(1.0+ sqrt((zeta*(qS-qD))*zeta*((qS-qD))+(epsi*epsi))))*(qS - qD);
ID = IS*id;
I(D,S) <+ ID;
```

Appendix B

Main definitions and characteristics

B.1 Noise Figure

The objective of a (RX), is to down-convert the received RF signal to the baseband with the maximal signal-to-noise ratio SNR in order to distinguish the low amplitude signals (sensitivity levels) from the noise floor. The noise figure (NF) measures the SNR degradation while the signal travels the RX. It is defined as,

$$NF = 10log(F) = 10log(\frac{SNR_{in}}{SNR_{out}}) \tag{B.1}$$

with F is the noise factor that is minimal at 1.

In this regards, the first active block in the receiver should be carefully designed as stated by the Frii's Formula,

$$F_{tot} = 1 + (F_1 - 1) + \frac{(F_2 - 1)}{G_1} + \frac{(F_3 - 1)}{G_1 G_2} + ... + \frac{(F_N - 1)}{G_1 G_2 ... G_{N-1}} \tag{B.2}$$

For a LNA-first receiver, the amplifier NF adds directly to the total NF of the receiver, while the following stages have their NF divided by the total gain before them. Hence, the LNA gain is responsible to reduce the following stages noise contributions. Correspondingly, the LNA should add the minimal amount of noise to not deteriorate the SNR (which explains the notation low noise amplifier).

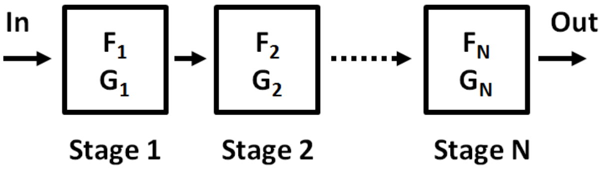


Figure B.1: N stage cascade, with G_i and F_i are the gain and noise factor of stage-i respectively

B.2 Input Matching

The quality of the input matching of the LNA is expressed by the input return loss S_{11} defined as,

$$S_{11} = 20log(\Gamma) = 20log\left(\left|\frac{Z_{in} - R_S}{Z_{in} + R_S}\right|\right) \tag{B.3}$$

with Z_{in} is the LNA input impedance and R_S is the standard termination impedance from the filtering stage following the antenna which is typically set to $R_S = 50\Omega$. This features the capability of the LNA to absorb the majority of the signal power with minimal reflections. When defining an impedance mismatch as $\Delta R = Z_{in} - R_S$, a return loss of $-10\,\text{dB}$ corresponds to $\Delta R = 23\Omega$ which is acceptable.

B.3 Stability

The presence of feedback paths from the output node to the input one inherently by the topology or caused by the drain to source or drain to gate intrinsic capacitances of the transistor, together with the presence of a high gain, may lead the circuit to an unstable state. The Stern stability factor, also known as the K-factor, is usually used to characterize the circuits stability and defined as,

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \tag{B.4}$$

with $\Delta = S_{11}S_{22} - S_{12}S_{21}$ and S_{ij} are the scattering parameters from a two-port network defined as the power from port i to port j. S_{11} and S_{22} refer to the reflection coefficients at the input (Port 1) and the output (Port 2) respectively. S_{21} represents the power gain which is the amount of power transmitted to (Port 2) with respect to the power received in (Port 1) and is referred as forward transmission coefficient. Correspondingly, the S_{12} represents the reverse transmission coefficient.

B.4 Linearity

Real systems, including amplifiers, are not ideally linear. For an input signal $x(t)$, the output from the transfer function of a non-linear system can be expressed as,

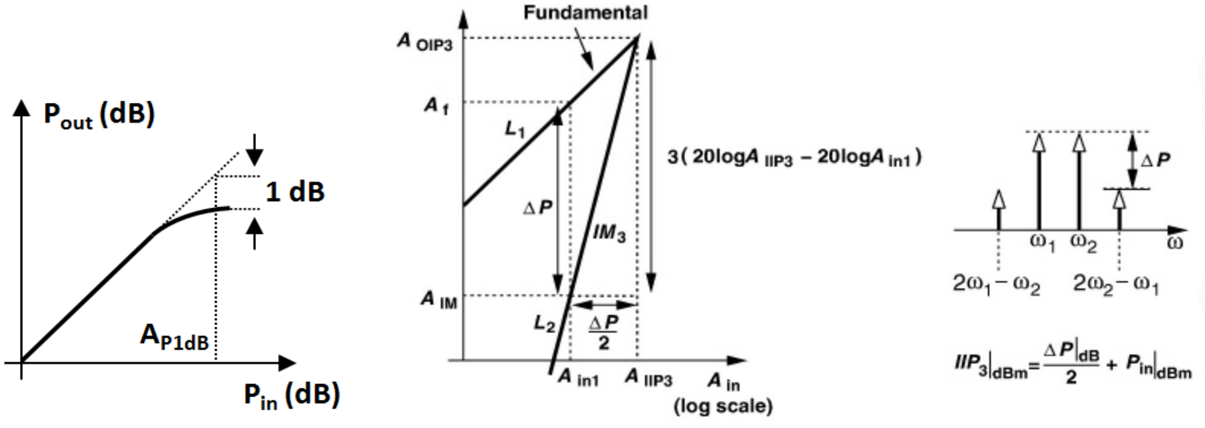
$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + ... + \alpha_n x^n(t) \tag{B.5}$$

with α_i are the non-linear coefficients of order i. From the LNA point of view, several non-linearity effects can be produced. For instance, the gain saturation (compression), the harmonic distortion (HD) and the intermodulation products (IP) that desensitize the fundamental component.

For $x(t)$ applied as a sinusoidal signal $x(t) = A_{in}cos(\omega t)$, the output $y(t)$ (limited to the third order, $n = 3$) from the LNA can be expressed as,

$$\begin{aligned} y(t) &= \alpha_1 A_{in}cos(\omega t) + \frac{\alpha_2 A_{in}^2}{2}(1 + cos(2\omega t)) + \frac{\alpha_3 A_{in}^3}{4}(3cos(\omega t) + cos(3\omega t)) + ... \\ &= \frac{\alpha_2 A_{in}^2}{2} + (\alpha_1 A_{in} + \frac{3\alpha_3 A_{in}^3}{4})cos(\omega t) + \frac{\alpha_2 A_{in}^2}{2}cos(2\omega t) + \frac{\alpha_3 A_{in}^3}{4}cos(3\omega t) + ... \end{aligned} \tag{B.6}$$

For large input signals, the term $\frac{3\alpha_3 A_{in}^3}{4}$ becomes comparable to the small signal fundamental coefficient $\alpha_1 A_{in}$. Depending the the α_3 sign, the fundamental gain can be increased or decreased. In the case where it is negative, we can talk about gain compression. It is characterized by the 1-dB compression point (P_{1dB}) or the compression point. It corresponds to the input signal power from which the fundamental gain decreases by 1 dB from its small-signal value. The corresponding input level A_{P1dB} can be expressed as,



(a) (b)

Figure B.2: a. Illustration of the 1-dB compression point. b. Illustration of the IIP3 calculation.

$$A_{P1dB} = \sqrt{0.145|\frac{\alpha_1}{\alpha_3}|} \tag{B.7}$$

In order to characterize the effect of the harmonics and the intermodulation products generated close to the useful frequency band, a two-tone test consisting of two adjacent channels $x(t) = Acos(\omega_1 t) + Bcos(\omega_2 t)$ is applied to the non-linear circuit input. The output $y(t)$ can be expressed as,

$$\begin{gathered}
y(t) = \frac{\alpha_2(A^2+B^2)}{2} \\
+ (\alpha_1 A + \alpha_3(\frac{3A^3}{4} + \frac{3AB^2}{2}))cos(\omega_1 t) + (\alpha_1 B + \alpha_3(\frac{3B^3}{4} + \frac{3BA^2}{2}))cos(\omega_2 t) \\
+\alpha_2 AB(cos((\omega_1-\omega_2)t)+cos((\omega_1+\omega_2)t))+\frac{3\alpha_3 AB}{4}(Acos((2\omega_1-\omega_2)t)+Bcos((2\omega_2-\omega_1)t)) \\
+ \frac{\alpha_2 A^2}{2}cos(2\omega_1 t) + \frac{\alpha_2 B^2}{2}cos(2\omega_2 t) + \frac{\alpha_3}{4}(A^3 cos(3\omega_1 t) + B^3 cos(3\omega_2 t)) \\
+ \frac{3\alpha_3 AB}{4}(Acos((2\omega_1+\omega_2)t) + Bcos((2\omega_2+\omega_1)t)) + ... \quad \text{(B.8)}
\end{gathered}$$

The second-order intermodulation products (IM2) are situated at $\omega_1 - \omega_2$ while the third-order (IM3), situated at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, which are close to the fundamentals can cause signal corruption. Hence, the different order intermodulation distortion IMD_i can be expressed as in (B.9) while considering equal amplitudes of the two tones ($A = B$),

$$\begin{aligned}
IMD_2 &= \frac{\alpha_2 A}{\alpha_1} \\
IMD_3 &= \frac{3\alpha_3 A^2}{4\alpha_1}
\end{aligned} \quad \text{(B.9)}$$

The harmonic distortion terms (HD_i) can be also expressed as function of the IMD_i as,

$$\begin{aligned}
HD_2 &= \frac{IMD_2}{2} \\
HD_3 &= \frac{IMD_3}{3}
\end{aligned} \quad \text{(B.10)}$$

The IIP_3 is one of the most important and used parameters to characterize the receiver chain linearity. It represents the input power for which the IM3 crosses the fundamental (or their extrapolations) in a log-log plot as functions of the input signal power as shown in Fig. B.2.b .

The second and third order input intercept points are defined then as,

$$\begin{aligned}
\alpha_1 A_{IIP2} = \alpha_2 A_{IIP2}^2 \text{ gives } IIP2 = 20log(A_{IIP2}) = 20log(\frac{\alpha_1}{\alpha_2}) \\
\alpha_1 A_{IIP3} = \alpha_3 A_{IIP3}^3 \text{ gives } IIP3 = 20log(A_{IIP3}) = 20log(\frac{4\alpha_1}{3\alpha_3})
\end{aligned} \quad \text{(B.11)}$$

Appendix C

LNA noise contributions calculation

The objective of this appendix is to explicitly show the noise figure of the proposed gm-boost CG LNA. All the noise contributors are isolated one by one and the superposition principle is applied for the final derivation.

C.1 CG output noise, transistor M_1

In Fig. C.1 is shown the small-signal equivalent circuit to calculate the output noise V_{noM1} (V_S) generated from the noise source i_{nM1} considering that,

$$i_{nM1} = \sqrt{4kT\gamma g_{m1}} \tag{C.1}$$

$$\begin{aligned}
&V_S = \frac{(1+A)g_{m1} + g_{ds1}}{\frac{1}{R_L} - g_{ds1}} V_{in} - \frac{i_{nM1}}{\frac{1}{R_L} - g_{ds1}} \\
&V_{in} = \frac{R'}{1 + g_{m1}(1+A)R'} i_{nM1} \\
&\text{Hence, } V_S = \left(\frac{(1+A)g_{m1} - g_{ds1}}{\frac{1}{R_L} + g_{ds1}} \frac{R'}{1 + g_{m1}(1+A)R'} - \frac{1}{\frac{1}{R_L} - g_{ds1}}\right) \sqrt{4kT\gamma g_{m1}} \\
&V_S \approx \frac{R_L\sqrt{4kT\gamma g_{m1}}}{1 + g_{m1}(1+A)R'} = V_{noM1}
\end{aligned} \tag{C.2}$$

with, $R' = R_D // R_S$

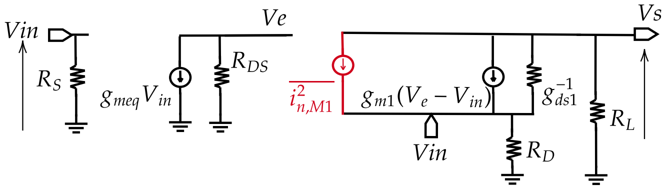


Figure C.1: Small-signal circuit to calculate the output noise generated by transistor M1.

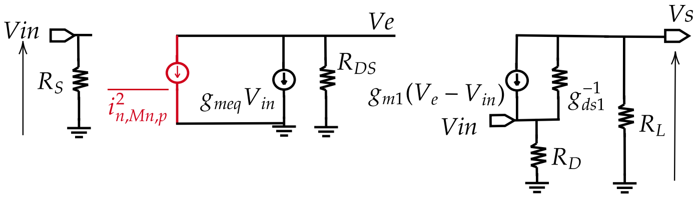


Figure C.2: Small-signal circuit to calculate the output noise generated by transistors Mn and Mp.

C.2 Complementary common source output noise, transistors M_n and M_p

In Fig. C.2 is shown the small-signal equivalent circuit to calculate the output noise V_{noA} (V_S) generated from the noise source $i_{nMn,p}$ considering that,

$$i_{nMn,p} = \sqrt{4kT\gamma g_{meq}} \tag{C.3}$$

$$\begin{aligned} &V_S = \frac{-gm1R_L}{1 - R_L g_{ds1}} V_e + \frac{g_{m1}R_L - g_{ds1}}{1 - R_L g_{ds1}} V_{in} \\ &V_e = -R_{DS}(g_{meq}V_{in} + i_{nMn,p}) \\ &V_{in} = \frac{V_S R'}{R_L} \\ &\text{Hence, } V_S \approx \frac{R_L g_{m1} R_{DS}\sqrt{4kT\gamma g_{meq}}}{1 + g_{m1}(1+A)R'} = V_{noA} \end{aligned} \tag{C.4}$$

C.3 Load resistance output noise, resistor R_L

In Fig. C.3 is shown the small-signal equivalent circuit to calculate the output noise V_{noRL} (V_S) generated from the noise source v_{nRL} considering that,

$$v_{nRL} = \sqrt{4kTR_L} = V_S = V_{noRL} \tag{C.5}$$

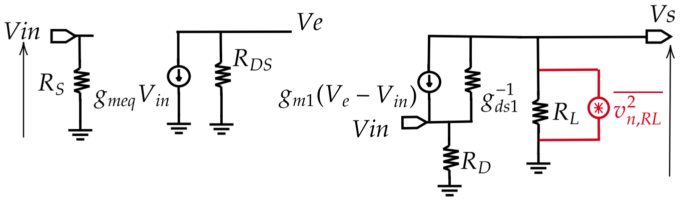


Figure C.3: Small-signal circuit to calculate the output noise generated by resistor RL.

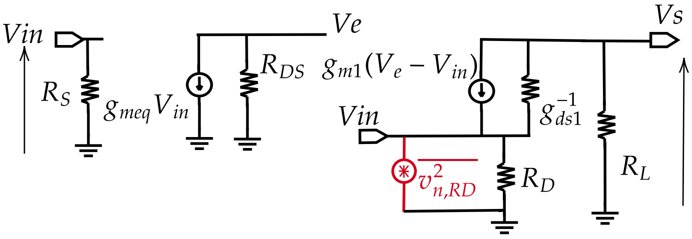


Figure C.4: Small-signal circuit to calculate the output noise generated by resistor RD.

C.4 Degeneration resistance output noise, resistor R_D

In Fig. C.4 is shown the small-signal equivalent circuit to calculate the output noise V_{noRD} (V_S) generated from the noise source v_{nRD} considering that,

$$v_{nRD} = \sqrt{4kTR_D} \tag{C.6}$$

$$v_S = R_L(1 + A)g_{m1}\sqrt{4kTR_D} = V_{noRD} \tag{C.7}$$

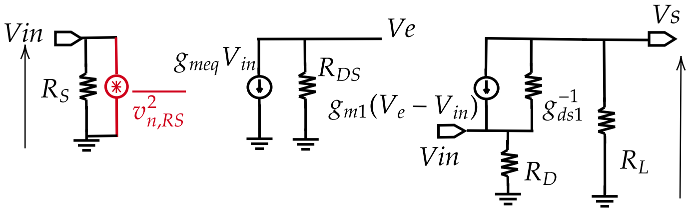


Figure C.5: Small-signal circuit to calculate the output noise generated by resistor RS.

C.5 Source resistance output noise, resistor R_S

In Fig. C.5 is shown the small-signal equivalent circuit to calculate the output noise $V_{nosource}$ (V_S) generated from the noise source v_{nRS} considering that,

$$v_{nRS} = \sqrt{4kTR_S} \tag{C.8}$$

$$v_S = R_L(1 + A)g_{m1}\sqrt{4kTR_S} = V_{nosource} \tag{C.9}$$