# Development of a self-sustained wireless sensor node.

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THÈSE PRÉSENTÉE

POUR OBTENIR LE GRADE DE

**DOCTEUR DE**

**L'UNIVERSITÉ DE BORDEAUX**

ÉCOLE DOCTORALE DES SCIENCES PHYSIQUES ET DE L'INGÉNIEUR

SPÉCIALITÉ ELECTRONIQUE

Par **Sébastien Guigue**

# Développement, intégration et prototypage d'un noeud-capteur autonome à récupération d'énergie pour réseaux de capteurs sans fils

Sous la direction de :
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Soutenue le 02 Mai 2024

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# ACKNOWLEDGMENTS

The completion of this thesis would not have been possible without the contribution of many individuals who played an important role in this work. Hence, this manuscript could not begin without some acknowledgments.

First of all, I express all my gratitude to Thierry Taris, Jean-Baptiste Begueret and Camille Leroux, my thesis advisors without whom this thesis would not have been possible. Thank you for your time, your patience, all the knowledge you brought me, and most of all, for your constant good mood. It has been a pleasure working with you during these three years.

I would like to thank all the member of the IMS Laboratory with whom I exchanged during these thesis. Working in the company of really kind people helped to make this journey more pleasant. Thus, I would like to thank Corentin, Anais, Maxime, Salime, Rémi, Martin, JC, Timothée, Sujeevan, Samir, Clement, Paul, Guillaume, Virgile, Henrique, Jonathan. I had a great time with all of you.

I would like to thank Leo, for your kindness, your sense of humour and all the climbing sessions we had together.

Thank you Nicolas for all the fun I had with you, great climbing moments and some discussions with had during hard moments. Spending time with you is always a pleasure.

Thank you Pierre for sharing my extreme humour since now 5 years, I have good memories of some great meals we had together and I promise, I will not forget our pact...

Thank you Maxandre for the fun we had together, the climbing sessions, for playing with me in the best band(IMHO), hope we will do some stuff together in the future.

Thank you Antoine(Saaaaaam) for sharing the early mornings in the lab with me. I have a special appreciation for your delightful taste in music but excepting this point, I am really happy for meeting you and sharing three years with of you.

Finally I want to thank my parents, my brother and my sister for encouraging me in my studies, for giving me the taste of well-done job, and for giving me values that contributed to who I am now.

*Tired of lying in the sunshine, staying home to watch the rain*
*You are young and life is long, and there is time to kill today*
*And then one day you find ten years have got behind you*
*No one told you when to run, you missed the starting gun*

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Roger Waters

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# GLOSSARY

AC: Alternative Current
ACCU: Accumulator
ALU: Arithmetic Logic Unit
BL: Boot Loader
COTS: Components Off The Shelf
CU: Control Unit
DARPA: Defense Advanced Research Projects Agency
DSN: Distributed Sensor Networks
DC: Direct Current
ED: Envelope Detector
FPGA: Field Programmable Gate Area
FRAM: Ferroelectric Random Access Memory
FSM: Finite State Machine
I2C: Inter-Integrated Circuit
IC: Integrated Circuit
IoT: Internet of Things
IPTO: Information Processing Techniques Office
MEMS: Microelectromechanical System
MCU: Microcontroller Unit
PCB: Printed Circuit Board
PLS: Post Layout Simulation
PU: Processing Unit
QoS: Quality of Service
RAM: Random Access Memory
RF: Radio-Frequency
SOSUS: Sound Surveillance System
SPI: Serial Peripheral Interface
UART: Universal Asynchronous Receiver Transmitter
WuRx: Wake-Up Radio
WSN: Wireless Sensor Network

# GENERAL INTRODUCTION

There has been an upsurge in the number of connected devices in the IoT(Internet of Things) context. The multiplication of Wireless Sensor Networks (WSNs) lead to an increase of the number of batteries and of waste generated. In a context of green electronics, the development of self-sustained circuits supplied with energy harvesting has to be managed.

Chapter I will give an overview of wireless sensor networks, including a brief history these systems, the different fields of application, the challenges and some possible solutions to overcome these issues.

Chapter II will present the design of a custom Microcontroller Unit (MCU) which runs the WSN with a minimum power consumption. The architecture of the microcontroller, the instruction set, the interfacing and all the design choices will be presented.

Chapter III describes the design of a Wake-Up Radio (WuRx), an always-on circuit which switches on the WSN when a request is sent. The choice for the architecture of each block Will be explained, while detailing the different aspects of each block.The blocks are as follows:

- An envelope detector for data reception,
- A comparator for data demodulation,
- An oscillator to provide a clock for the system,
- A correlator to compare the received message with a reference,
- A current source to provide temperature robustness.

Chapter IV provides an analysis of the entire wireless sensor node. An estimation of the node autonomy is presented and a comparison with a node designed with market components is presented. Perspectives of improvement for future works will also be presented.

# INTRODUCTION GÉNÉRALE

Il y a eu une recrudescence du nombre de dispositifs connectés dans le contexte de l'Internet des objets. La multiplication des réseaux de capteurs sans fil a conduit à une augmentation du nombre de batteries et de déchets générés. Dans un contexte d'électronique verte, le développement de circuits autonomes alimentés par la récupération d'énergie doit être géré.

Le premier chapitre donnera un aperçu des réseaux de capteurs sans fil, y compris une brève histoire de ces systèmes, les différents domaines d'application, les défis et quelques solutions possibles pour surmonter ces problèmes.

Le second chapitre présentera la conception d'un microcontrolleur sur mesure pour l'application qui controle le noeud capteur avec une consommation minimale d'énergie. L'architecture du microcontrôleur, le jeu d'instructions, l'interfaçage et tous les choix de conception seront présentés.

Le troisième chapitre décrit la conception d'une radio de réveil, un circuit toujours actif qui active le noeud capteur lorsqu'une requête est envoyée. Le choix de l'architecture de chaque bloc sera expliqué, en détaillant les différents aspects de chaque bloc. Les blocs sont les suivants :

- Un détecteur d'enveloppe pour la réception des données,
- Un comparateur pour la démodulation des données,
- Un oscillateur pour fournir une horloge pour le système,
- Un corrélateur pour comparer le message reçu avec une référence,
- Une source de courant pour assurer la robustesse thermique.

Le dernier chapitre fournit une analyse de l'ensemble du nœud de capteur sans fil. Une estimation de l'autonomie du nœud est présentée et une comparaison avec un nœud conçu avec des composants du marché est également présentée. Des perspectives d'amélioration pour les travaux futurs seront également exposées.

# CHAPTER 1

# INTRODUCTION TO WIRELESS SENSOR NETWORKS

## 1.1 What is a Wireless Sensor Network?

Wireless Sensor Networks (WSNs) have become a prevalent technology in the context of the Internet of Things (IoT). This section provides a brief historical overview of WSNs, their design principles, and delves into the issue of power management. It also includes a description of their application fields and concludes by highlighting the challenges and future prospects of this technology.

### 1.1.1 Introduction

The increasing pursuit of having connected devices leads to a need of smaller low power systems, with cheaper costs to be massively manufactured, and a minimal low human intervention for maintenance. However, this continuous increase faces the actual environmental problematic, which brings designers to create sustainable systems, particularly concerning products lifetime, recycling and green power management.

WSNs are the ones of the most impacted systems by these issues, because of the important amount of devices that are and will be deployed in the upcoming years. This makes it very challenging to combine the endless connectivity expansion with the energy sobriety obligation.

The Internet of Things (IoT) refers to the interconnected network of physical devices, vehicles, buildings, and other objects that are embedded with sensors, software, and network connectivity, enabling them to collect and exchange data. This network of interconnected devices can communicate with each other and with other systems, allowing for greater automation, control, and efficiency. Domains covered by IoT are described in Fig.1.1.

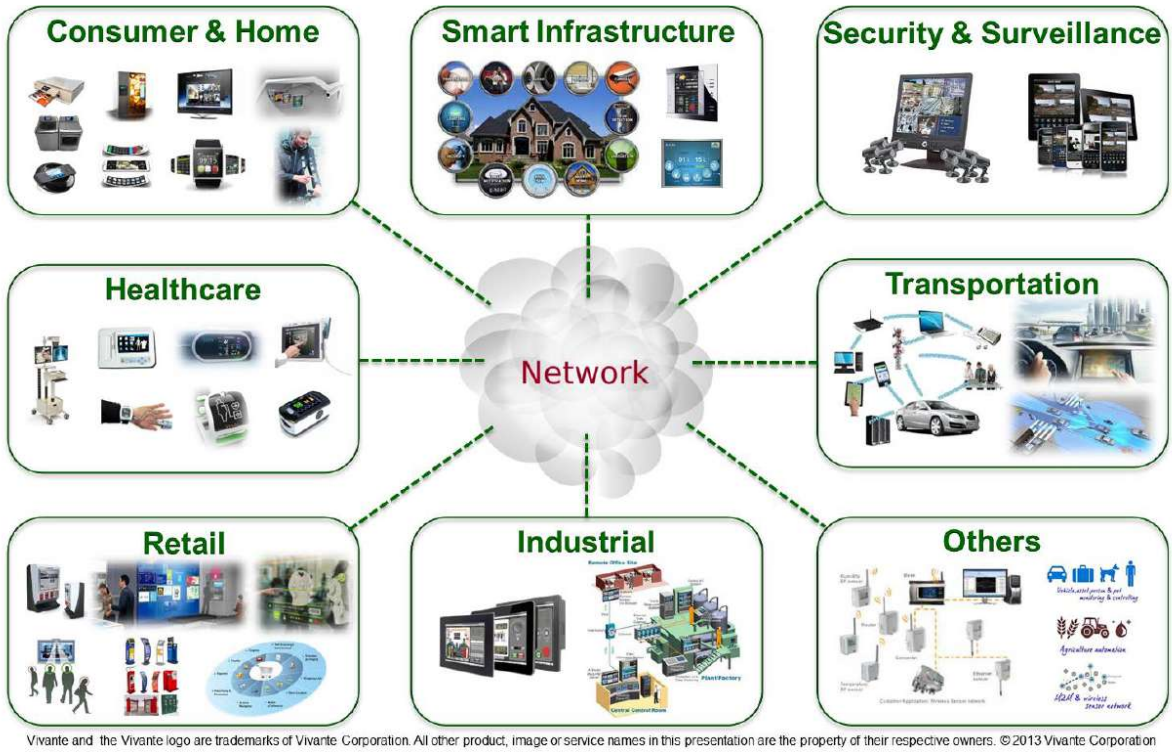



Figure 1.1: Applications covered by IoT[1].

Current research in IoT has generated a significant interest in deploying systems that are ultra low power and low maintenance. However, this state of affairs is inadequate in light of the present environmental context, and it is crucial to have systems that consume such low power that they can be batteryless and self-sustained solely through ambient energy harvesting.

### 1.1.2 Wireless Sensor Network Architecture

WSNs are a type of network that consists of small devices called wireless sensor nodes, which are equipped with sensors to collect data from their environment, process that data, and communicate the information to other nodes in the network or to a central server called gateway.

Wireless sensor nodes can be deployed in a variety of environments, including indoor and outdoor settings, and are used in many different applications, such as environmental monitoring, industrial control, healthcare, and security systems. They can measure a wide range of physical parameters, such as temperature, humidity, light, sound, motion, and pressure.

The nodes in a WSN can communicate with each other through different wireless communication protocols, such as Wi-Fi, Bluetooth, Zigbee, or LoRaWAN to name a few. The nodes can also be configured to form a mesh network, where they can relay information to other nodes in the network, extending the network's coverage and increasing its reliability and Quality of Service(QoS).

Overall, wireless sensor nodes are an important technology for collecting and transmitting data from various environments and can help automate processes, increase efficiency, and provide valuable insights for decision-making in many different fields. Fig. 1.2 shows different topologies of WSNs.

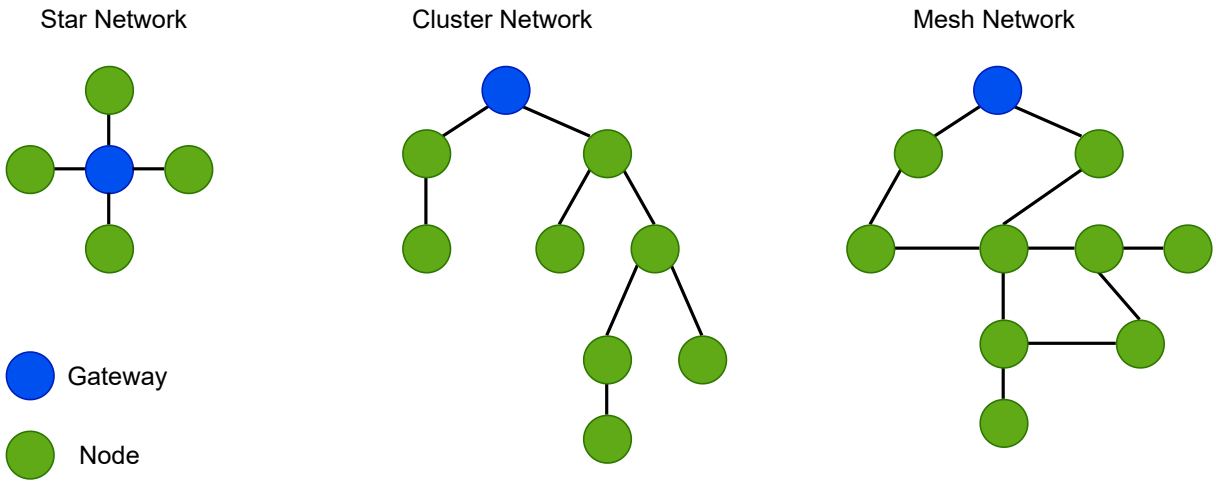



Figure 1.2: Wireless Sensor Networks Topologies[2].

In a wireless sensor network, a gateway is a device that serves as a bridge between the wireless sensor nodes and a central server or the internet. The gateway typically has a more powerful processor and communication capabilities than the individual sensor node, enabling collecting and processing data from multiple nodes. The gateway transmits these data to a central server or the cloud.

One of the main functions of a gateway in a wireless sensor network is to manage the network and its nodes. It can perform tasks such as node registration, network configuration, and software updates. It can also monitor the health and status of the nodes, such as battery level and connection status.

The gateway can also provide additional features and functionalities, such as data encryption and security, data aggregation and analysis, and integration with other systems and applications.

Overall, the gateway is an essential component of a wireless sensor network that enables the efficient collection, processing, and transmission of data from the sensor nodes to a central server or the internet.

### 1.1.3 Wireless Sensor Node

A wireless sensor node is a compact device designed to collect and transmit data wirelessly from the environment it is deployed in. It typically consists of four main components as illustrated in Fig. 1.3:

- A sensor which is the primary component of the node, responsible for measuring the physical or environmental parameter of interest, such as temperature, humidity, or light intensity to name a few.

- A microcontroller which acts as the brain of the node, responsible for processing the data received from the sensor and controlling the wireless communication module.
- The wireless communication module is responsible for transmitting the data collected by the sensor to a central hub or gateway, typically over a radio frequency band.
- A power source to supply the entire system, the power source can be either a battery or an energy harvesting system, depending on the application and the expected lifetime of the node.

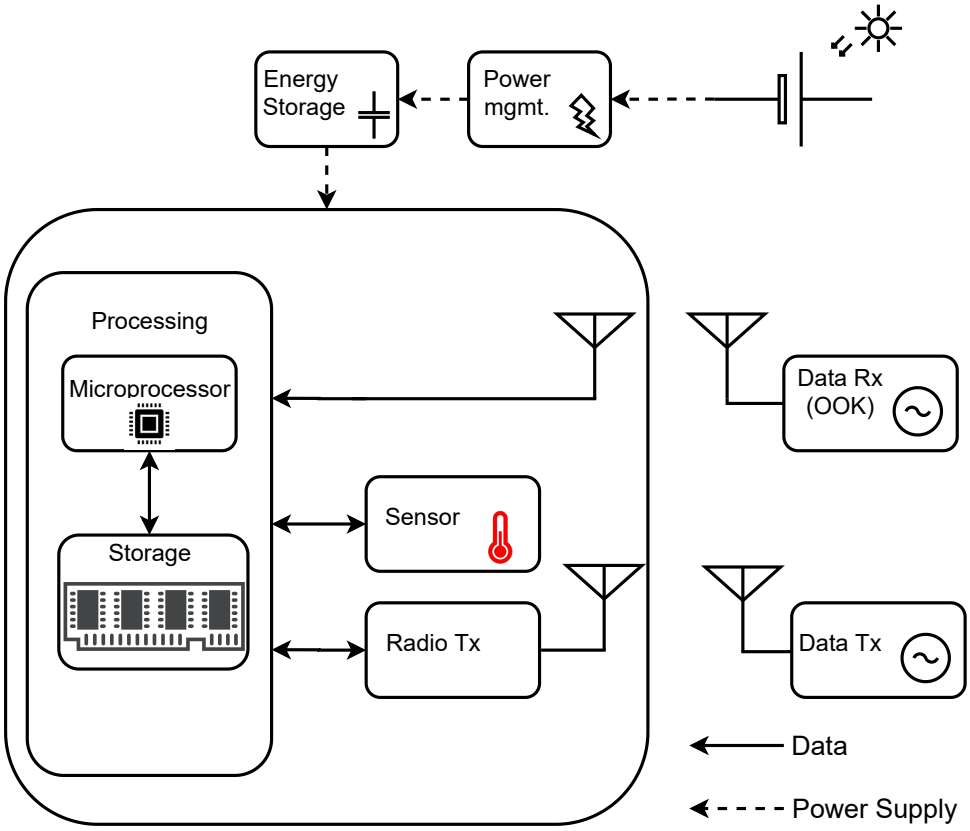



Figure 1.3: Typical architecture of a Wireless Sensor Node.

The compact size and wireless communication capability of sensor nodes are critical for deployment in various environments, including indoor and outdoor settings. They can be used for a wide range of applications, including environmental monitoring, smart buildings, healthcare, agriculture, and industrial automation. The flexibility and scalability of these devices make them a crucial component of the IoT ecosystem.

### 1.1.4 Wireless Sensor Network History

Since most of new technology inventions emerge from military research, it is difficult to exactly determine the exact introduction of an innovation. However, the predecessor of WSNs can be found back in the 1950s. Sound Surveillance System (SOSUS) was a classified US Navy program that operated during the Cold War for the detection of Soviet submarines. The system consisted of a network of underwater microphones or hydrophones that were deployed at various locations in the world's oceans to detect the sound signatures of submarines[3], [4]. Fig. 1.4 presents the principle of SOSUS system.

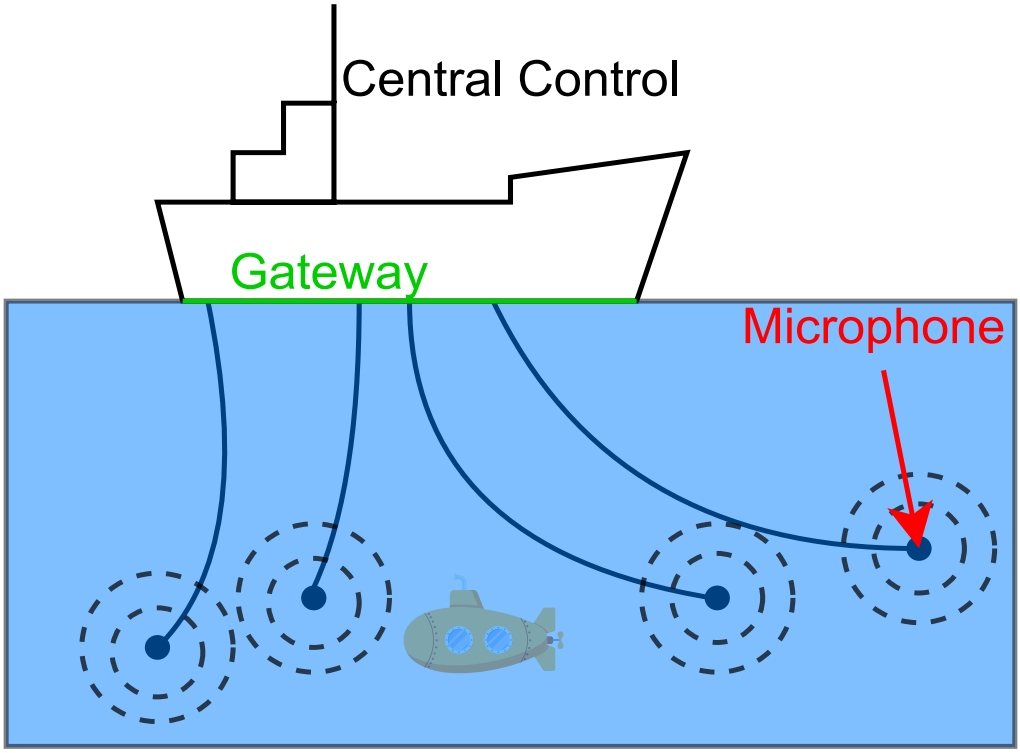



Figure 1.4: Principle of Sound Surveillance System.

While SOSUS was not a wireless sensor network in the modern sense, it could be considered as a precursor to modern underwater acoustic sensor networks, which are wireless sensor networks designed for underwater applications.

The study of sensor networks originated in 1980 when the Defense Advanced Research Projects Agency (DARPA) launched the Distributed Sensor Networks (DSN) program[5]. At that time, the Arpanet, a forerunner of the Internet, had been functioning for several years and was being used by approximately 200 hosts located in universities and research institutions. R. Kahn, one of the co-inventors of the TCP/IP protocols and a major figure in the development of the Internet, was the director of the Information Processing Techniques Office (IPTO) at DARPA. He sought to investigate whether the Arpanet approach to communication could be applied to sensor networks. The sensor network was envisioned as having numerous low-cost sensing nodes spread across different locations, which would work collaboratively but independently, with information being routed to the most suitable node.

Considering the technological limitations of the time, the DSN program was a highly ambitious initiative. This was an era before personal computers and workstations were widely available, and most processing was done using minicomputers. Modems were operating at speeds ranging from 300 to 9600 Bd, and Ethernet was only just starting to gain popularity.

At Carnegie Mellon University, researchers aimed to create a network operating system that would provide flexible and transparent access to distributed resources required for a fault-tolerant DSN. To achieve this, they developed a communication-oriented operating system called Accent[6], which has primitives that facilitate transparent networking, system reconfiguration, and rebinding. The Accent operating system later evolved into the Mach operating system[7], which enjoyed significant commercial success. In addition, these

researchers also worked on developing protocols for network inter process communication to support dynamic rebinding of active communicating computations, an interface specification language for building distributed system software, and a system for dynamic load balancing and fault reconfiguration of DSN software. They demonstrated all of these concepts in an indoor test bed with signal sources, acoustic sensors, and VAX computers connected via Ethernet.

MIT researchers in Cambridge conducted a study on tracking helicopters using a distributed array of acoustic microphones by applying knowledge-based signal processing techniques. They utilized signal abstractions and matching techniques and developed SPLICE and Pitch Director's Assistant for DSN data analysis and algorithm development. Tracking multiple targets in a distributed environment is much more challenging than centralized tracking since the association of measurements to tracks and the estimation of target states must be distributed over the sensor nodes. Advanced Decision Systems developed a multiple-hypothesis tracking algorithm for dealing with challenging scenarios involving high target density, missing detections, and false alarms, and decomposed the algorithm for distributed implementation. MIT Lincoln Laboratory developed a real-time test bed for acoustic tracking of low-flying aircraft for demonstration. The sensors used were acoustic arrays arranged in three concentric triangles, and the test bed was successfully demonstrated with low-flying aircraft tracked using acoustic sensors and TV cameras. This was the state-of-the-art technology in the early 1980s.

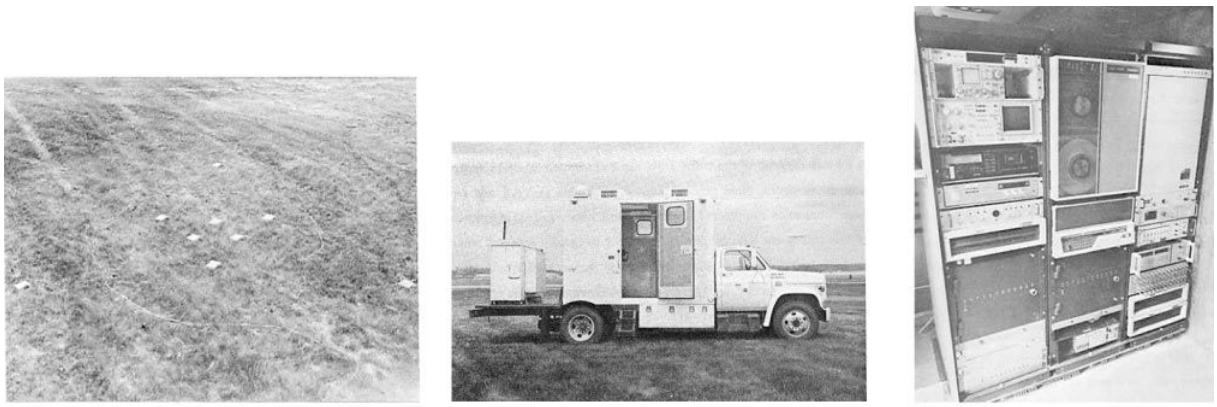



Figure 1.5: Pictures of the System Developed by the MIT[8].

Until the 2000's, researches were mainly focused on communication protocols, recent advances in computing and communication have caused a significant shift in sensor network research and brought it closer to achieving the original vision. Small and inexpensive sensors based upon microelectromechanical system (MEMS) technology, wireless networking, and inexpensive low-power processors allow the deployment of a wide number of sensors and extended the field of applications.

## 1.2 Applications of Wireless Sensor Networks

The expansion of WSNs opens a wide range of applications, from military applications to domestic applications with innovative systems. This section will present WSNs application in the following fields: healthcare, environment, industry and urban applications.

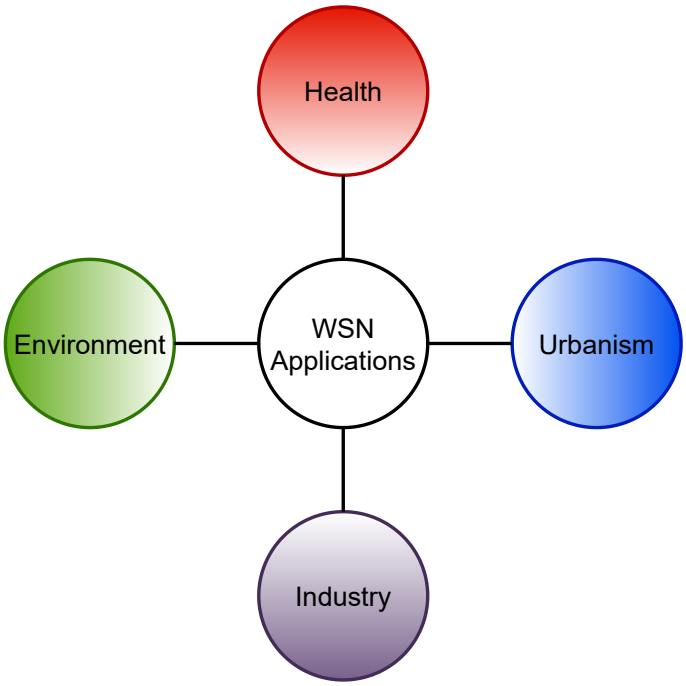



Figure 1.6: Application Field of WSNs.

### 1.2.1 Health Applications

WSNs in healthcare context already exist with the massive development of smart watches that can give information such as heart rate or average body activity. Currently with the miniaturization of devices, it becomes easier to develop wearable devices and the field of application becomes wider. An overview is given in Fig. 1.7.

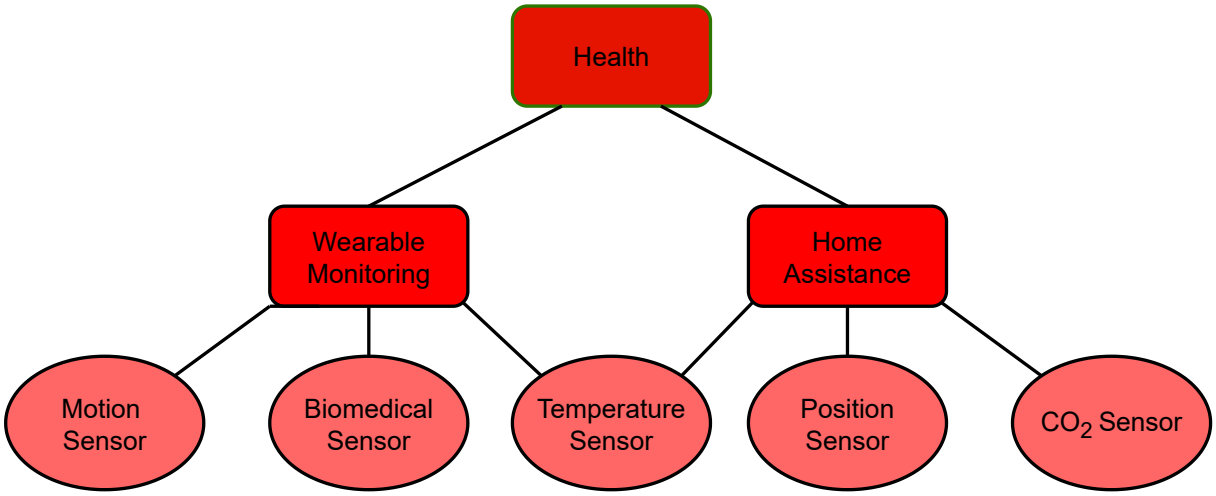



Figure 1.7: WSNs in Healthcare Overview.

Several applications already exist about healthcare[9]. Some of them focus on elder's safety such as fall detectors[10], posture detectors and location tracking. Some use biological sensors to monitor patient's health. Some applications are dedicated to continuous sensing for patients suffering from cognitive disorders such as Parkinson or Alzheimer. There is also significant research effort in developing small sensor devices which can be implanted in human body. Other researches are more related to smart homes[11] which will be presented in a next part.


Figure 1.8: Example of Wearable Device with Multiple Sensors[12].

The main challenge of WSNs in healthcare, in addition of low power consumption and small footprint is data security. Because personal data can be handled, more security must be added to preserve people's privacy thus requiring more computing capabilities.

### 1.2.2 Environmental Applications

WSNs are used in environmental sensing to monitor parameters such as air or water quality, or even in agriculture applications. Fig. 1.9 gives an overview of the possible use of WSNs in the environment context.

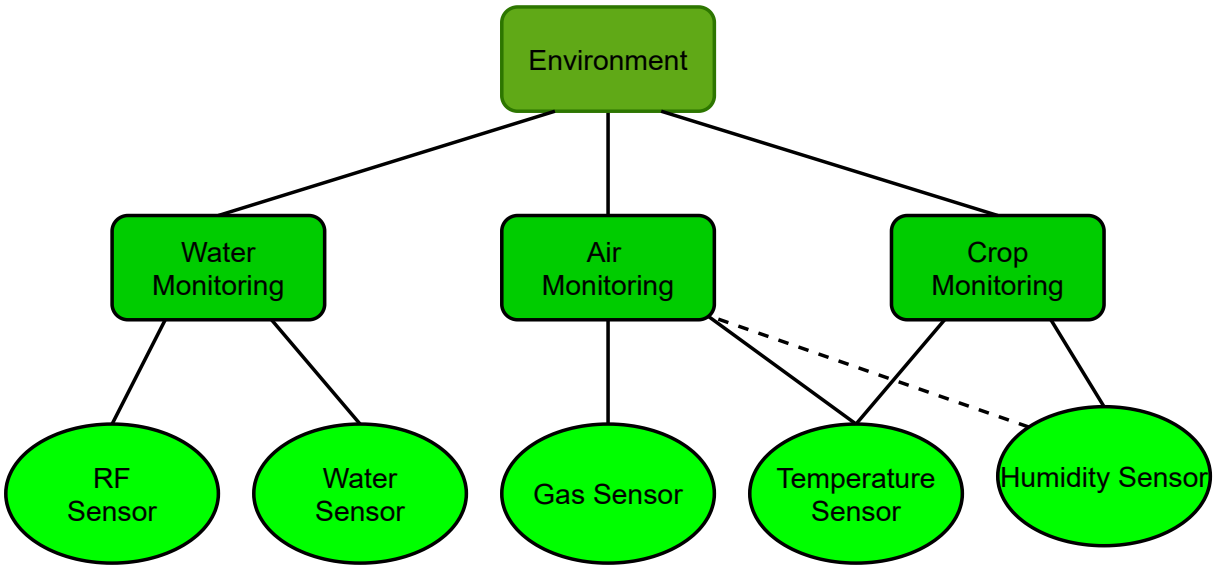



Figure 1.9: WSNs in Environment Applications Overview.

In this context, WSNs can harvest data from their environment for several applications such as pollution control, natural disasters prevention (earthquakes for example)[13] or to serve for smart agriculture[14]. Fig. 1.10 gives an example of an acoustic sensor called audiomoth which can have several uses such as the monitoring of species, soundscape analysis or environmental surveillance.

Figure 1.10: Acoustic Sensor for Environmental Monitoring[15].

The main challenge in this application context is the distance from infrastructures which reinforce the need of energy autonomy and the use of green energy for more sustainability.

### 1.2.3 Industrial Applications

WSNs are widely used in the industry particularly with the automatising of some tasks and so the increasing use of robots by industrialists. Several use of WSNs can be imagined as depicted in Fig. 1.11.

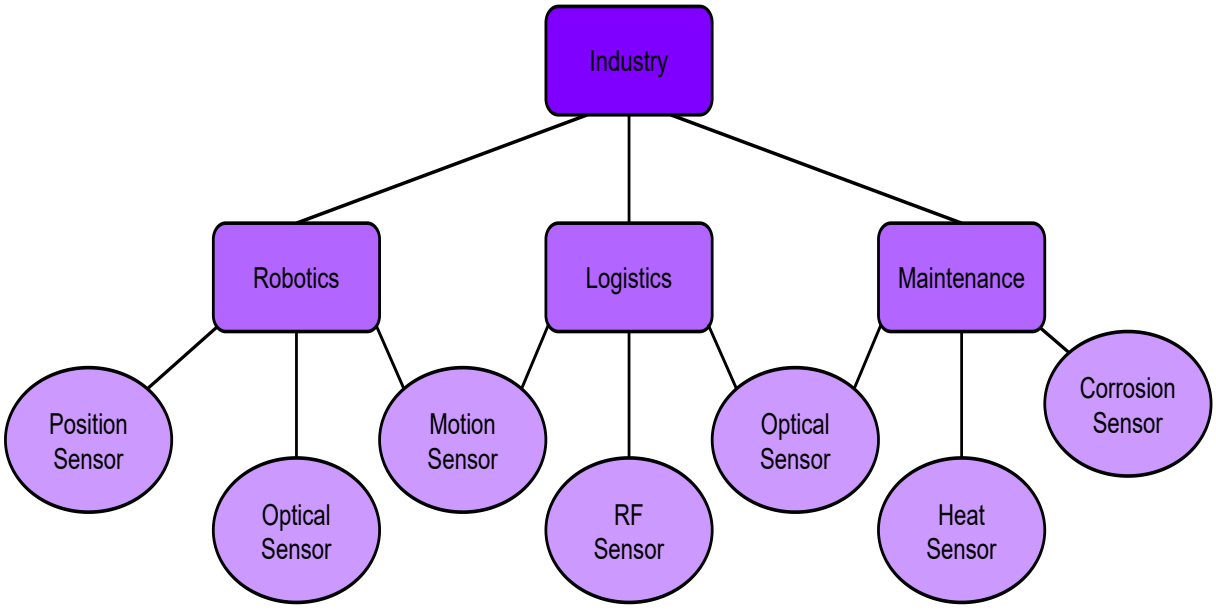



Figure 1.11: WSNs in Industry Applications Overview.

Sensors are already widely exploited on line work machines to increase the production rate. If these sensors can be made autonomous in energy, the gains would be significant. WSNs can also be used in logistics, if each package is associated with a tag that is checked automatically with a WSN, time can be saved.

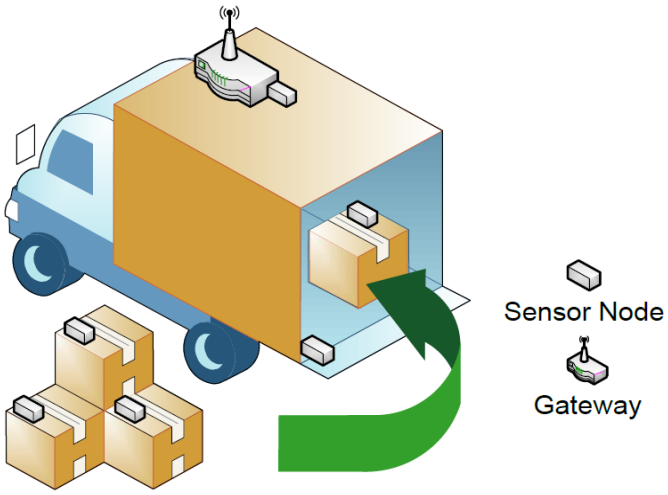



Figure 1.12: Example of WSNs Use in Logistics[16].

The main constrains in the development of WSN dedicated to industrial application are the reliability and the cost of the solutions.

### 1.2.4 Urban Applications

With the upcoming development of smart cities, smart homes and autonomous cars, the number of uses of WSNs continuously increases. Several possible applications are presented by Fig. 1.13.

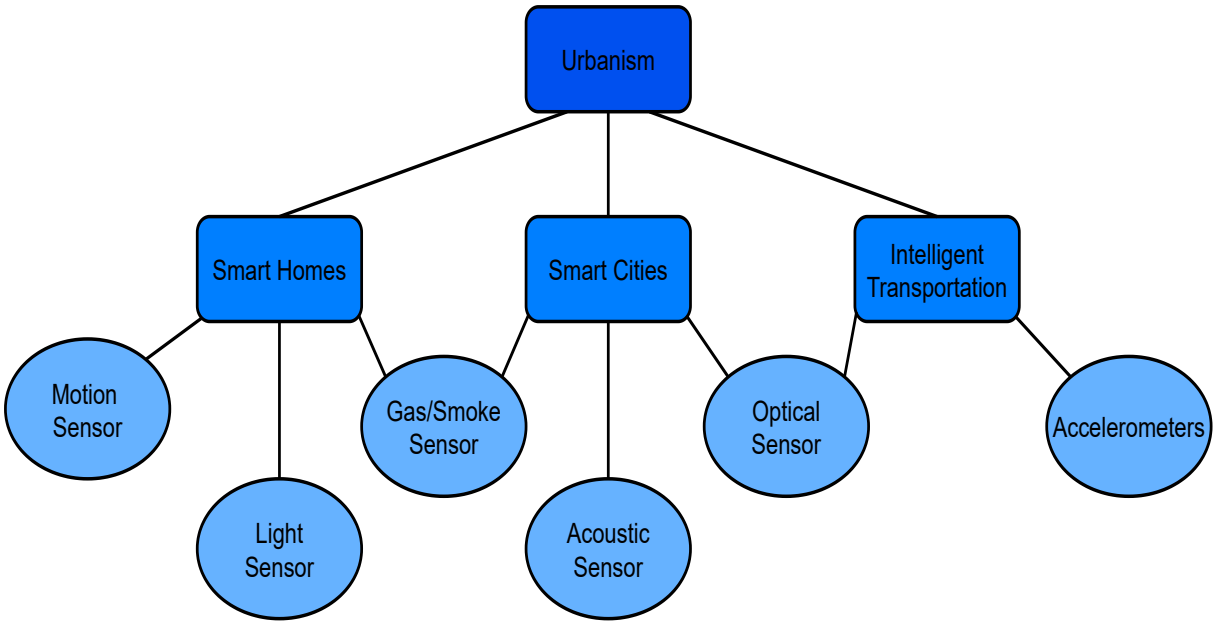



Figure 1.13: WSNs in Urban Applications Overview.

The development of WSNs has increased for smart homes use[17], [18]. The objective with the concept of smart cities in the upcoming years is to have a full connectivity that can be compliant with autonomous vehicles that will also use WSNs[19]. Indeed, autonomous cars will need to communicate with the external environment to function correctly, the development of this technology is therefore dependent on the development of infrastructures for smart cities. Fig. 1.14 gives an example of the connected objects that will be foundable in smart cities.


Figure 1.14: WSNs in Smart City[20].

### 1.2.5 Conclusion

The extension possibilities for WSNs are continuously increasing with more upcoming applications. The use of WSNs can go from basic temperature sensors to industrial or healthcare applications, each field having its specific constraints. The common point is that the multiplication of the number of devices will lead to ecological concerns particularly with power consumption and batteries manufacturing. The subject of power management is critical for any application.

## 1.3 Power Management

### 1.3.1 Introduction

The expansion of IoT leads to a continuous increase in the number of connected devices. The forecasts tend to 30 billions of devices by the end of the decade[21] as presented by Fig. 1.15 and all these devices need to be supplied.

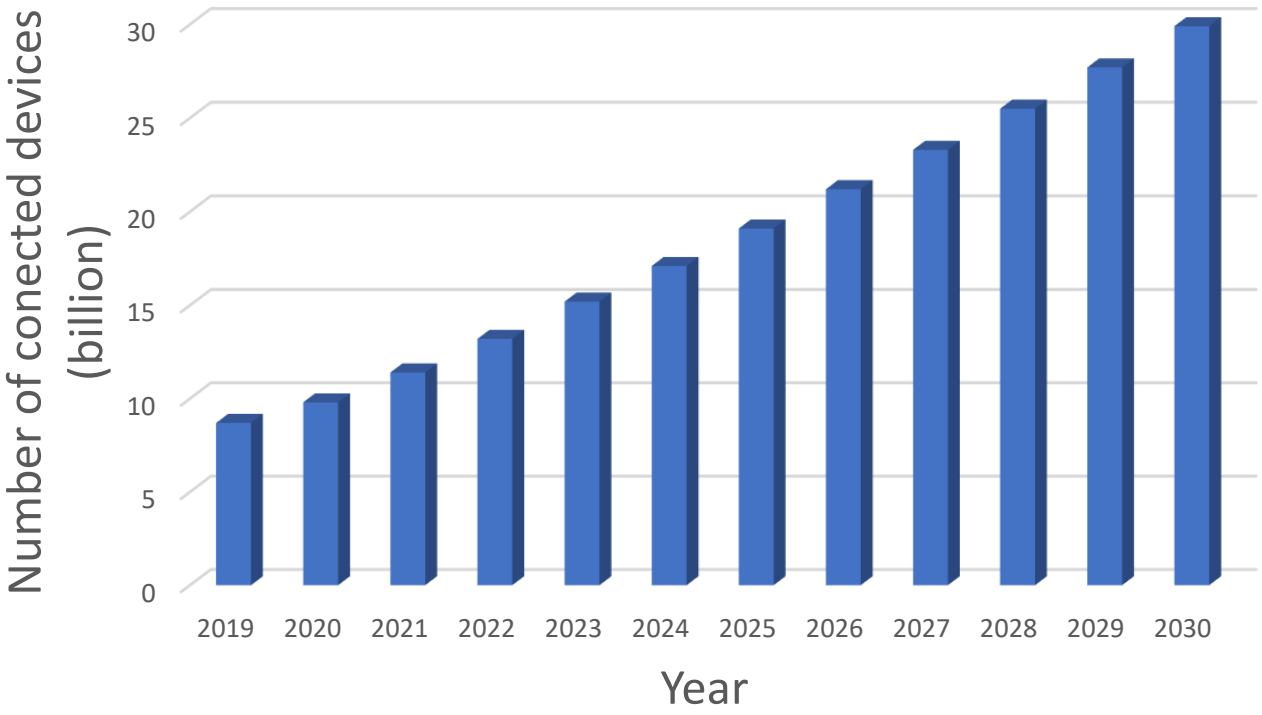



Figure 1.15: Connected Devices Forecast[21].

Depending on the application, several typed of batteries can be deployed, considering an ideal case where all the devices are powered by a 3V coin battery which is the smaller format. 30 billions battery would weight more than 80 million kilograms which represents the weight of an aircraft carrier. Moreover, considering the cost of these batteries around 1€, it would represent the price for 5 warships. Finally, 30 billions of coin batteries would circle the Earth more than 40 times[22].

To conclude, the costs, natural resources and human resources for batteries replacement cannot support this amount of batteries and the ecological impact would be too important to be sustainable. This is the reason why a solution to maximize batteries lifetime or even remove batteries from connected devices needs to be found.

### 1.3.2 Power sources

To replace batteries, some alternative sources of energy have to be found. This part presents different sources that are available, their advantages and drawbacks, and if there are usable or not in a WSN context.

Depending on the amount of energy required by a system, and the cost involved in implementing powering such devices, different power sources may be adapted for different implementations, scenarios or schemes. Analyzing different sources will also permit to check which method is the most suitable to the application. Fig. 1.16 presents a variety of different energy sources for IoT devices:

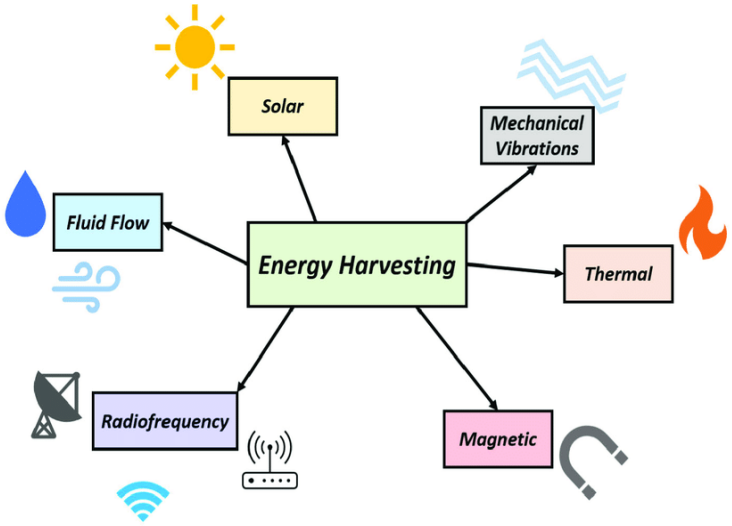



Figure 1.16: Different Sources for Energy Harvesting[23].

Table 1.1 presents typical energy range for each methods, the advantages and the drawbacks for each method.

Table 1.1: Typical Characteristics from Different Sources.

| Energy | Available Power | Advantages | Drawbacks | Sources |
|---|---|---|---|---|
| Mechanical | 100µW-mW | Continuous energy in some context | Expensive, need to have device in movement | [24], [25], [26], [27] |
| Thermal | mW | Can harvest large amount of power | Always need temperature variations | [23], [28], [29], [30], [31] |
| Magnetic | - | - | Need magnetic source | [23],[32],[33] |
| Fluid | mw - 100mW | Large amount of energy | Expensive, dependent on the environment | [34],[35],[36],[37] |
| RF | ~100µW | RF waves everywhere | Not a lot of power, dependent on the source | [25],[38],[39] |
| Solar | ~100µW-100mW | Good efficiency, mature technology | Dependent on the light | [27],[40],[41],[42] |

Among the various sources of harvestable energy, wind and solar energies typically exhibit the highest power output per unit area. Additionally, thermoelectric, electromagnetic, and vibrational energy sources offer intriguing energy densities. However, it is important to acknowledge that implementing these energy harvesting technologies can often be costly due to overhead expenses, infrastructure requirements, and maintenance. Furthermore, it is worth mentioning that certain harvesting methods can be combined synergistically.

For this thesis RF and solar harvesting are chosen because of their ease of installation, low cost and their dependency on external parameters is less restrictive than the other methods.

## 1.4 Challenges for Wireless Sensor Networks

The future perspective of a fully connected society becomes more and more realistic but in this context, several challenges appear and have to be tackled to keep on increasing the use of WSNs. The issue of power consumption has been discussed in the previous section, but other challenges must be considered.

### 1.4.1 Security

As previously mentioned, data security is one of the main issues for WSNs. If personal or sensitive data are handled, a higher level of encryption must be used to ensure that these data cannot be recovered. Another security issue is denial-to-service attack which consists in making the device nonoperational[43]. A higher level of data coding needs to be used to overcome these issues, however, this leads to more complex and more power hungry systems which will have a lower lifetime. A trade-off needs to be found when considering this issue.

### 1.4.2 Robustness

The robustness is the ability of a system to function with an invariant behaviour when external disturbances occur. WSNs are highly subject to robustness issues[44] because of its low cost, low power and so low complexity design. In this context, the sensor nodes must have as low false wake up as possible and need to miss requests as few as possible. Besides, if the nodes are placed in harsh environment, the system needs to be robust enough so that it is not degraded with time by its environment and its functioning still be accurate.

### 1.4.3 Management

Up to now, WSNs designs were based on small size networks applied to only one application and so WSNs were designed with no really consideration for management. Because future WSNs are supposed to have hundreds or even thousands of nodes, it is important to manage the good operation of the whole group[45].

Sensor management can be described as a dynamic system that aims to manage and coordinate sensor nodes in order to improve performance while minimizing energy consumption. There is a wide range of applications for sensor networks, each with different requirements. These applications can be classified as follows:

- Scavenging parameters of the physical environment such as the temperature in a room for example.
- Detecting events and assessing their impact: is there a sudden evolution of a parameter and what is the impact?
- Being able to make the different between objects that are analysed
- Tracking moving objects.

These four application types have different performance metrics, such as detection probability, identification accuracy, and probability of loss-of-track. Additionally, certain performance metrics, such as lifetime and latency, should also be considered. Energy efficiency is crucial in WSNs, and all network operations should be performed with minimal energy consumption. In some applications, the collected data is only valuable if it reaches the observer in a timely manner. Hence, the main objective of sensor network management is to balance these performance metrics in order to maximize overall performance.

### 1.4.4 Power Consumption

Because the node is functioning only when a request occurs, it spends a major part of the time in idle state waiting for an event. This leads to a power consumption used for no activity. To avoid this waste of energy, actual nodes integrate an other block called Wake-Up Radio (WuRx). The purpose of this block is to be always on when the rest of the node is shutdown, and when an action is intended, it sends a signal to switch on the node to perform the measurement, and then go back in shutdown mode as illustrated in Fig. 1.17.

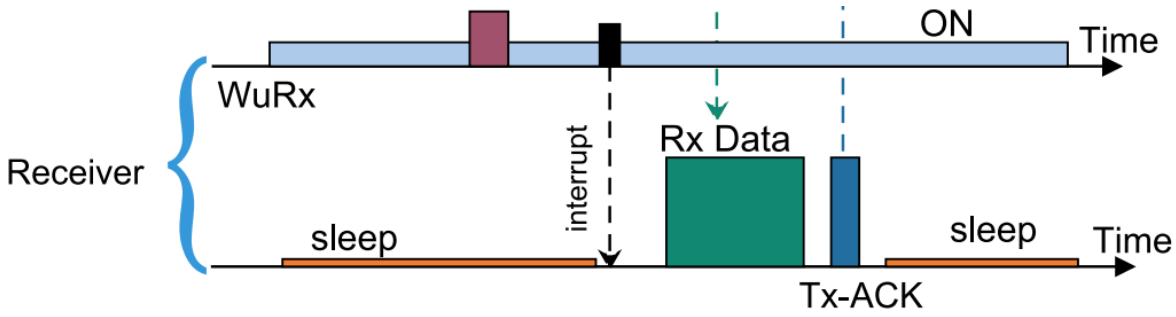



Figure 1.17: Wireless Sensor Node Duty Cycling[46].

This solution allows to have only one low power circuit active during higher amount of time and so save an important quantity of energy. Fig. 1.18 shows the architecture of a wireless sensor node including the WuRx module.

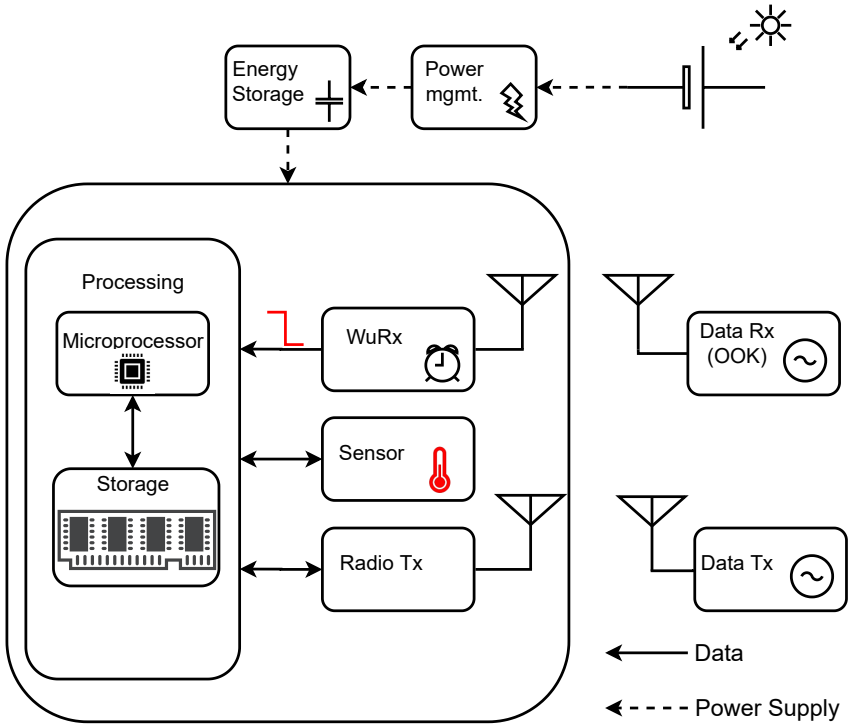



Figure 1.18: Wireless Sensor Node with Wake-Up Radio.

Concerning the MCU, an issue is that actual circuits are designed to cover as many applications as possible. This leads to extra features that are useless for this application and so extra power consumption. A sober design must be done to save as much energy as possible.

## 1.5 System Overview

This thesis is meant to be the continuity of [47] starting from the final results. The conclusion of this work is that designing a wireless sensor node powered by energy harvesting is doable, and a full system designed with Component Off The Shelf(COTS) and market component was developed. Fig. 1.19 shows the manufactured wireless sensor node with the components soldered on Printed Circuit Boards(PCB) and the schematic view of this node.

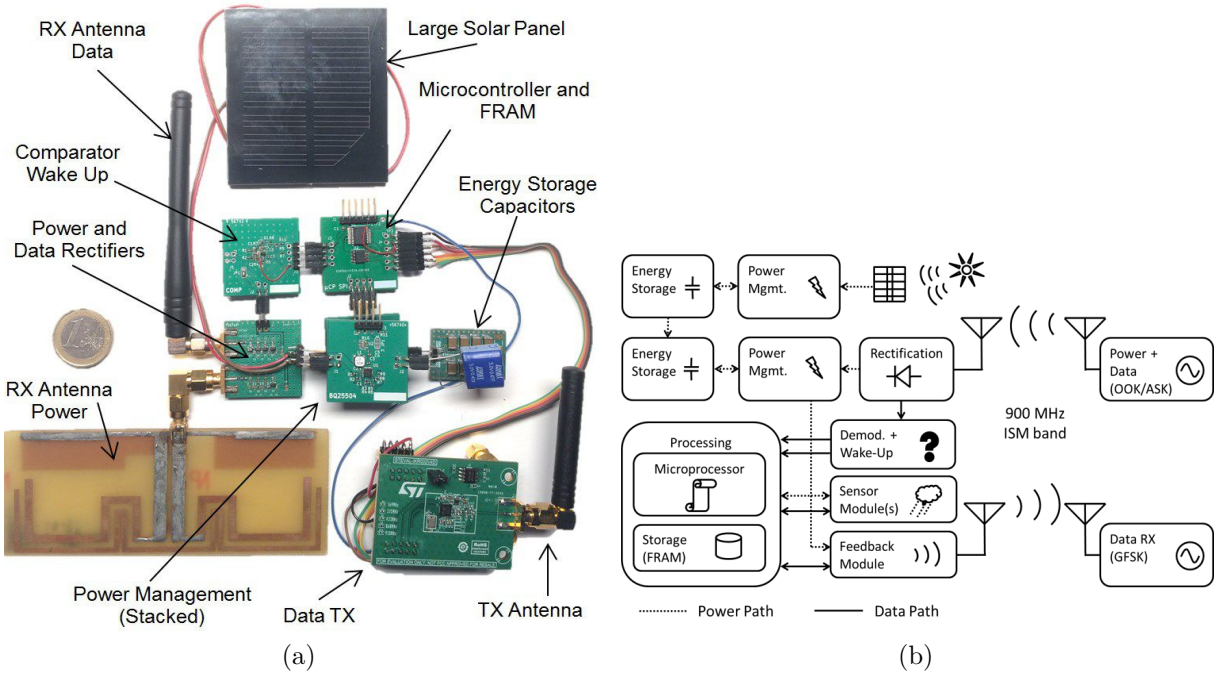



Figure 1.19: (a) COTS Wireless Sensor Node, (b) Schematic View of the Node[47].

The more challenging blocks of this system will be briefly presented with their role, their performances and limitations. Finally the axes of improvement will be presented and will determine the research directions for this thesis.

### 1.5.1 Rectification

The incoming RF energy and data go through two rectifiers in parallel that are used to demodulate incoming data on a one hand, and to harvest RF energy on the other hand. The circuit was designed using HSMS-285C diodes[48].
Fig. 1.20 presents the output of the rectifier depending on the input power. A slight amount of energy can be harvested at the maximum sensitivity of -30dBm while integrated rectifiers in WuRx can easily go under -60dBm. The sensitivity of the circuit is limited by COTS diodes which exhibit a high threshold voltage(typically 200mV). To overcome this limitation, the solution will be to develop an integrated circuit using diode-connected transistors featuring circuit technics to compensate for intrinsic device threshold voltage and to reach better sensitivities.

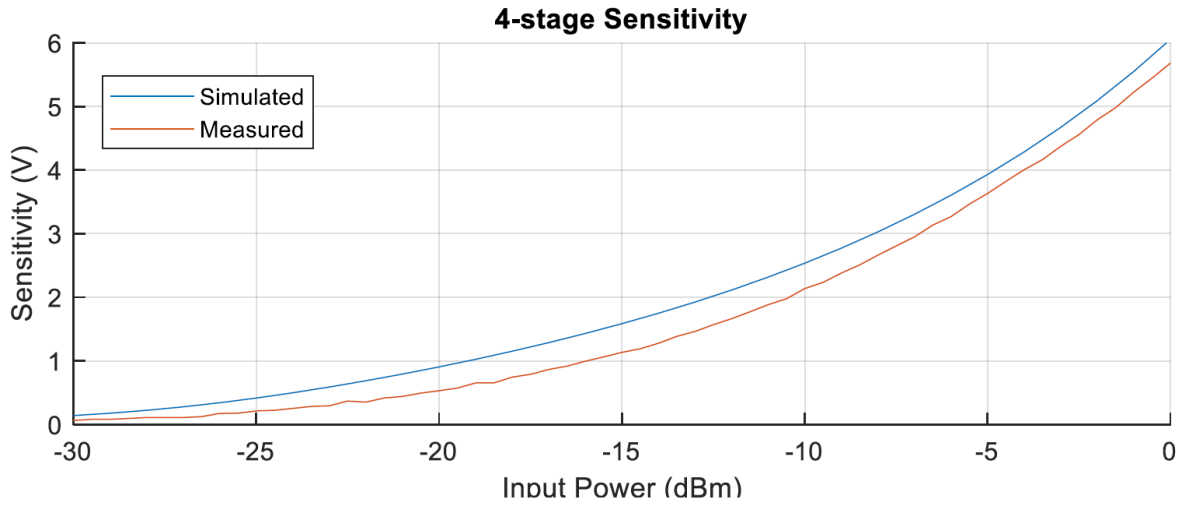



Figure 1.20: Measurement Results of the Rectifier[47].

### 1.5.2 Power Management

The energy harvested from RF or solar sources is then handled by power management modules Texas Instrument bq25504[49] and bq25570[50] respectively. Fig. 1.21 shows the measurement of RF energy harvesting with this circuit.

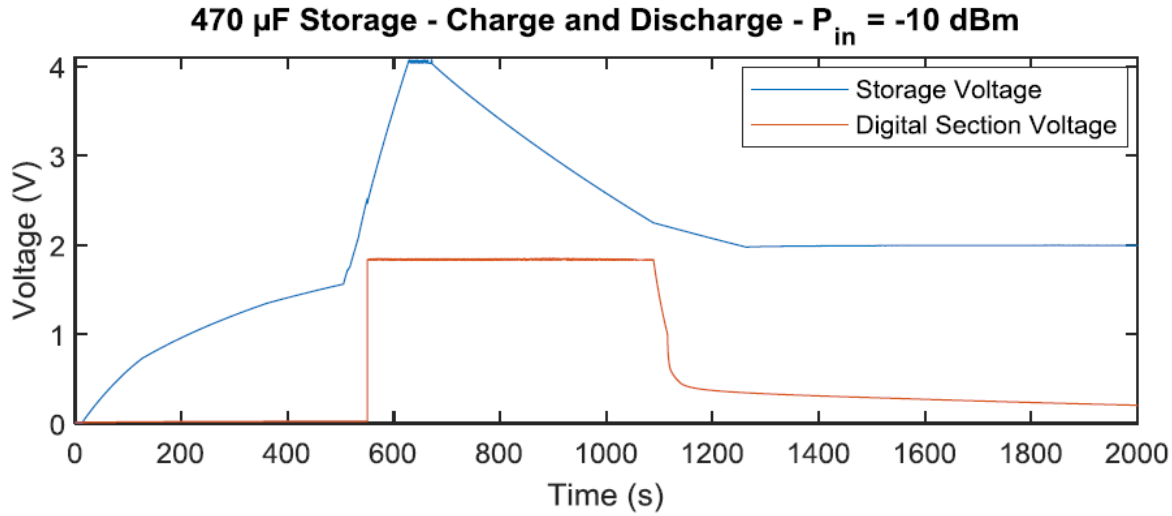



Figure 1.21: Measurement Results of the Energy Harvester[47].

It appears that the circuit is able to charge a $470\mu F$ capacitor and deliver the current drawn by the node during its operating phase. However, the remark can be done that the circuit operates with an input power of -10dBm which is not the range of value that is met in energy harvesting.

This principle limitation for these circuits is their cold stat voltage i.e the minimum voltage needed to engage the power management. In this thesis, the choice was made to test products from the company E-Peas which presents lower cold start voltage and so should afford better performances.

### 1.5.3 Wake Up Generation

To use the node only when needed, a wake up radio was also designed. It is composed of a band-pass filter, a comparator and a rectifier. Fig. 1.22 shows the generation of the wake up signal after a request. The power consumption for the demodulation is around 800nW which is quite significant. Comparatively, most of state-of-the-art circuit have a power consumption ranging from 10nW to 100nW for these applications. This limitation is here again due to the use of COTS components. To overcome this issue, this thesis focuses on implementing a full custom wake up Radio in CMOS technology. This WuRx module is further detailed in Chapter 3.

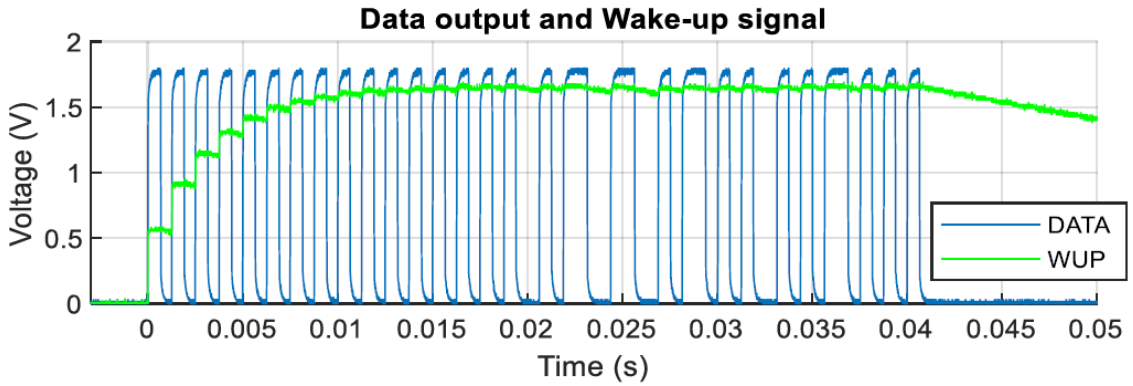



Figure 1.22: Generation of the Wake-Up Signal[47].

### 1.5.4 Data Processing and Data Sending

The data are gathered from the sensor(BME280 from Bosch[51]) and processed with a PIC16LF1559 microcontroller[52] to be further stored in a Ferroelectric Random Access Memory(FRAM)[53]. The data are then sent back with the STMicroelectronics Spirit1 transmitter[54]. Table. 1.2 summarizes the power consumption of the node for each operation. It can be noticed that both devices are not optimized for low power applications. Concerning the radio transmitter, the choice is made to use a new market component dedicated for low power applications. The same direction will be taken for the sensor, a market component will be used because they already fit well low power applications. On the other hand, the MCU has much more features than the ones needed for the required task and the same drawback can be found with most of market components. This is why in this thesis the choice was made to design a dedicated MCU with the minimum functionalities to save the maximum amount of energy.

Table 1.2: Power Consumption Summary of the Node[47].

| Command | Duration(ms) | Power(µW) | Energy(µJ) |
|---|---|---|---|
| Sleep Mode | - | 0.92 | - |
| False Wakeups | 16.8 | 416 | 7 |
| Temperature Measurement | 40.6 | 422 | 17.1 |
| FRAM Data Storage | 42.1 | 420 | 17.7 |
| FRAM Data Retrieval | 42.2 | 417 | 17.6 |
| Data Transmission | 55.9 | 1750 | 97.8 |

### 1.5.5 Full System

The designed system managed to work with energy harvesting and could achieve an autonomy up to 50 hours depending on the time interval between measurements.
Fig. 1.23 presents the autonomy of the system in function of the measurement intervals.

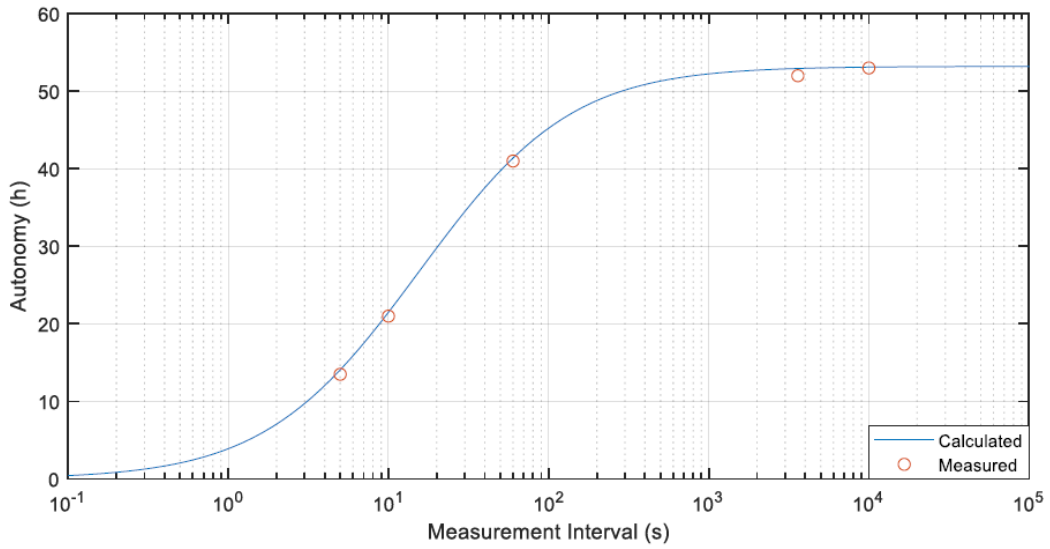



Figure 1.23: Autonomy of the Node[47].

The conclusions of this thesis pointed out some limitations. Firstly the use of COTS for the design of the WuRx significantly reduces its performances in term of sensitivity and power consumption due to the components limitations. An integrated design would allow to gain sensitivity and lower the global consumption. Moreover, the microcontroller used in this work is a generic market components which has a quite high power consumption to perform the required operations and the idea of having an application specific circuit was proposed. Working on these two aspects would enhance the performances of the node and increase its lifetime.

## 1.6 Conclusion

This chapter presents an overview of WSNs, how it works, the different fields of application and the upcoming challenges. It brings out the fact that power consumption will be the limiting factor in most applications and this performance is for now the main point for improvements.

To demonstrate the feasibility of an autonomous IoT node, a first development based on COTS devices had been realized by Dr J. Nicot during his PhD at the IMS lab. This first demonstrator was fully autonomous and included the main features of an IoT node. Pointing out the limitations of a COTS implementation, it served as a starting point of this PhD work.

This work will focus on the design of a low power WuRx and MCU that will be integrated into a WSN with the objective of having an autonomous system. The circuit will be designed to be connected with market components concerning the sensor, the radio module and the power management unit.

# CHAPTER 2

# MINIMALIST LOW POWER MICROCONTROLLER DESIGN

## 2.1 Introduction

The previous chapter presented the interest of having a purpose-designed microcontroller to limit extra power consumption. Fig. 2.1 shows the position of the MCU in the node.

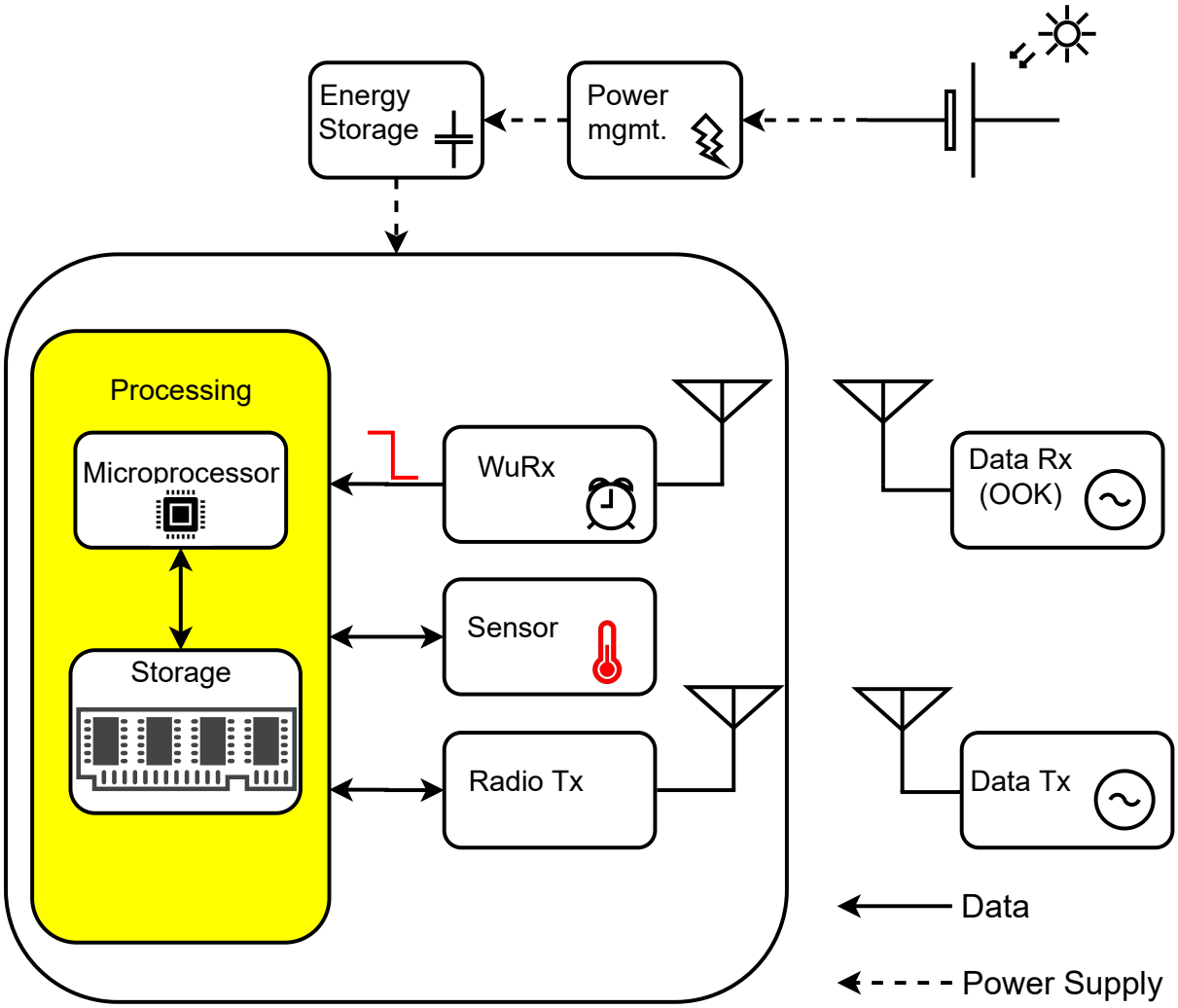



Figure 2.1: Position of the MCU in a Node.

The MCU acts as the brain of the WSN, its function is to communicate with the peripherals, handle the data and perform some calculation if necessary. The necessary features in the MCU are those which allow to perform the mentioned functionalities.

The actual trend with market components is to have multi-purpose circuit that are able to cover a wide range of applications. This implies having many peripherals, multiple communication protocols, different types of memories and many other features. To illustrate this, Fig. 2.2 shows an example of an IoT-oriented microcontroller. The counterpart is that the MCU becomes larger, its static power consumption increases and the high number of pads also increases the leakage current. The objective in this thesis is to present an MCU design which limits the number of features to function and so save the maximum power.

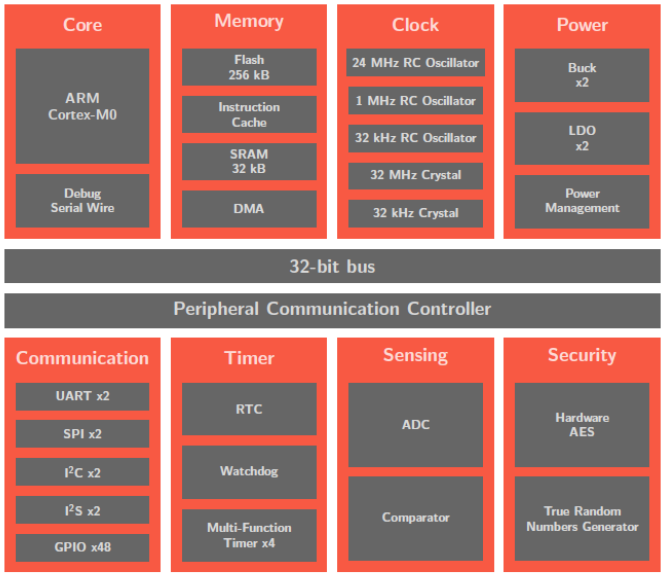



Figure 2.2: Example of an IoT Oriented MCU[55].

Table. 2.1 presents the main features of some IoT oriented MCUs. This allows to have an overview of the design trends in this field. It can be seen that all the circuits share the same voltage supply range which is a standard range for microcontrollers. All the circuit are in 32-bit topology, which is actually the most widespread configuration for microcontrollers.

Table 2.1: Features of IoT Oriented MCUs.

| | [56] | [57] | [58] | [59] | [55] |
|---|---|---|---|---|---|
| Data Size | 32 bits | 32 bits | 32 bits | 32 bits | 32 bits |
| Voltage Supply(V) | 3.8 | 1.7-3.6 | 1.6-3.6 | 1.65-3.6 | 1.8-3.3 |
| Core | Arm Cortex M0+ | Arm Cortex M4 | Arm Cortex M23 | Arm Cortex M0+ | Arm Cortex M0 |
| Memories | 512kB flash/128kB RAM/32kB ROM | 1-MB application flash/ 32-KB auxiliary flash/32-KB supervisory flash/ 16kB flash cache/288-KB SRAM | 512kB flash/64kB SRAM /32kB ROM | 64kB flash/8kB RAM/ 2kB EEPROM | 256kB flash/ SRAM |
| Clock Sources | 4 | 3 | 4 | 5 | 4 |
| Communication Peripherals | 3 SPI/3 I2C/3 UART/ 2USB | 9 SPI/I2C/UART | 6 SPI/I2C/UART USB | 1 USB/3 UARTs/4 SPI/ 2I2C | UART / 2 SPI / 2 I2C |

It is important to note the wide variety of memories, clocks and peripherals. This choice allows the circuits to cover many applications, communicate with several peripherals and operate at various frequencies. The counterpart is that it generates non negligible power consumption that can be considered wasted if the MCU does not operate at full potential.

Besides, in a low requirement application such as sensor networks, the amount of memory in the MCUs can be questioned. The presented circuits have two or three types of different memories, the entirety representing dozens of kilobytes of data. This high amount of memory allows the microcontrollers to be versatile and cover a wide area of applications. Indeed, from the industrial point of view, developing only one circuit doing different tasks instead of having multiple circuits is more lucrative.

On the other hand, this amount of memories appears to be oversized in WSNs applications considering the fact that the node just has to send few instructions and stores a small amount of data. Limiting the memory size of the circuit would decrease the power consumption and leakage to benefit for an increased autonomy of the circuit. Besides, less memory means a lower footprint for the circuit which will reduce the cost for manufacturing.

This chapter presents the design of a custom 32-bit MCU. It goes through the architecture of the system and the choices that are made to design this architecture. Finally a logical synthesis of the MCU is introduced in which the performance and power consumption of the MCU is presented.

## 2.2 Technology Choice

The choice of the technology has to suit for both the design of the WuRx and the MCU. The global power consumption of the MCU in the IoT is usually in the milliwatt range[60] while WuRx are in the nanowatt or microwatt range. The choice of the technology is focused on limiting the MCU power consumption.

In digital design, the power consumption comes from switching transistors. Eq. 2.1 presents the dynamic power consumption for transistors when switching[61].

$$P_{dynamic} = C_L \times V_{DD}^2 \times f \times \alpha \tag{2.1}$$

Where $C_L$ is the load capacitance, $V_{DD}$ is the voltage supply, $f$ is the frequency and $\alpha$ is the switching activity.

This equations shows that with smaller transistors, the capacitance $C_L$ is reduces and so, if all the others parameters are unchanged, the power consumption will be reduces. This is one of the reasons why small technological nodes are preferred for digital designs. Although smaller technological nodes are preferred because of their lower dynamic power consumption, leakage current tends to increase while the node size decreases[62] which can be a limitation for low energy requirements. A the technology with the best trade off between these two parameters must be found.

Typically in low power applications, the most critical part of a MCU is the memory, mainly because it occupies a wider area, and also because it may need to be always powered on to keep data, which will lead to continuous leakage current.

The choice of the technology is done after a study on the available memories. The studied technologies are 28nm FDSOI, 65nm Bulk and 130nm from STMicroelectronics.

The main parameters of a memory are the size, the density i.e. the number of bits per area unit, the access time, the dynamic and static power consumption. Here the parameter to be optimized is energy consumption. The memory is selected depending on this parameter. More specifically, because the MCU will be off most of the time, the memory with the lowest static power consumption is aimed.

The studied shows that for similar memory size, memories with leakage around few hundreds of nanowatts can be used with the 65nm technology while the other technologies presents memories with current leakage in the microwatt range. For this reason, the chosen technology is the 65nm Bulk technology from ST Microelectronics, this technology presents the lowest current leakage and so the impact of the memory is minimised during the off phases of the MCU.

## 2.3 Microcontroller Architecture

### 2.3.1 Microcontroller Specifications

Before digging into the core of the MCU, the specifications of the circuit must be listed. The target is the design of a low power MCU for a wireless sensor node. The main optimization scope for the entire design is to present a power consumption as low as possible. The MCU is hard coded to reduce its complexity and the code is executed when an enable is sent by the WuRx. Concerning the function of the microcontroller, the circuit must be able to communicate with two peripherals, a radio and a sensor, and perform basic computations. The voltage supply comes from the energy harvesting block.

### 2.3.2 Initial Architecture

The design of the MCU is inspired by the design presented in [63] which is a minimal 8-bit microcontroller design with a function centered on only on register(ACCU). This reference circuit is given with only four instructions(NOR, ADD, STORE, JUMP) and a 64 byte memory.

The design goal is to minimize the utilization of macrocells exclusively for combinational logic, with the objective of maximizing the availability of usable registers. To achieve this, structures such as multiplexers between registers and the address/data output must be avoided at all costs. As a result, the data path is divided into one path for the address and another for the data.

Unlike other small CPUs, the address generation is not performed by the main ALU. Instead, a separate incrementer is necessary for the PC. Fortunately, the PC incrementer can still fit into the macrocells(i.e. a functional block or unit within the microcontroller that typically performs a specific task or set of tasks) that house the PC register, enabling the entire address-data path to fit within 12 macrocells.

The data-path represents 14 macrocells: eight for the accumulator, one for the carry flag and five combinational cells for the carry propagation.

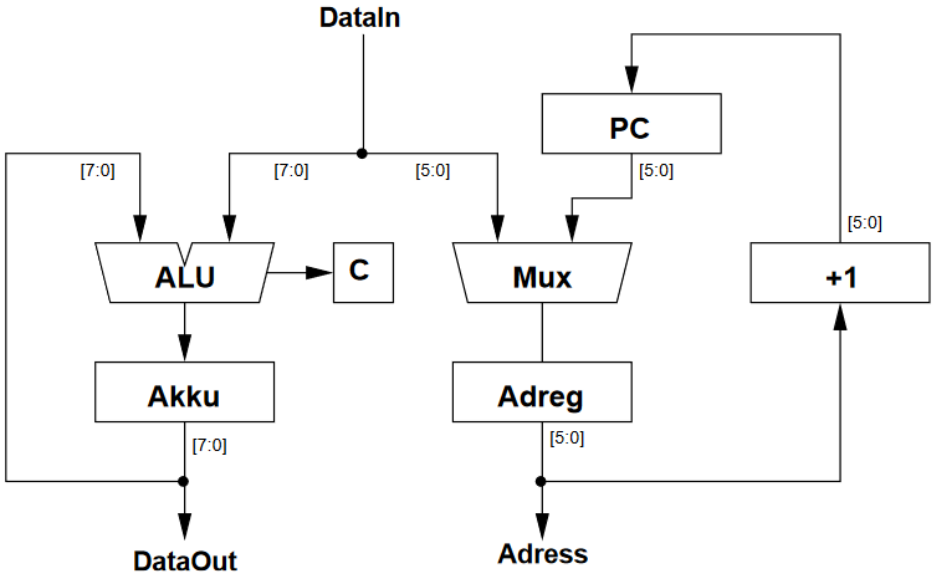



Figure 2.3: Data-Path of the 8-bit CPU[63].

The data-path operates under the influence of a straightforward state machine featuring 5 states. The encoding of these states is thoughtfully selected to minimize the necessary macrocells for storage and decoding. In total, 5 macrocells are utilized for control.

Table. 2.2 outlines the state encoding for the state machine. The majority of instructions are executed within a concise two-clock cycle time frame.

Table 2.2: State Machine of the 8-Bit CPU.

| State | Function |
|---|---|
| S0 | Fetch Instruction/Operand address |
| S1 | Write ACCU into memory |
| S2 | Read operand, ADD |
| S3 | Read operand, NOR |
| S4 | Clear carry, Read PC |

Because the purpose in this design is to save as much energy as possible, the idea is to start with this minimalist circuit, and then add features only if necessary, and so limit the energy consumption increase.

The next section presents the design of the MCU, decisions that were made and the justifications of these choices.

### 2.3.3 Global Architecture

The architecture of the designed MCU is presented in Fig. 2.4. It can be divided in four parts:

- The Control Unit (CU) fetches the instructions from the memory and then decodes them. The relevant control signals are then generated for the Processing Unit and the MU.
- The Processing Unit (PU) loads the operands from the memory, executes the instruction through the Arithmetic and Logic Unit(ALU) and finally stores the result in the ACCU register.
- The Memory Unit (MU) stores instructions and data following a Von Neumann architecture. This allows an easier implementation and less connections in comparison with an Harvard architecture.
- The Boot Loader (BL) first loads the program stored in the memory and then launches the execution. In Fig. 2.4, it can be noticed that the BL has additional pins $T_x$, $R_x$ and $Scan\_Memory$. These pins allows to send the program from a computer and give back the content of the MCU memory. This method is used for testing the circuit on board and debugging.

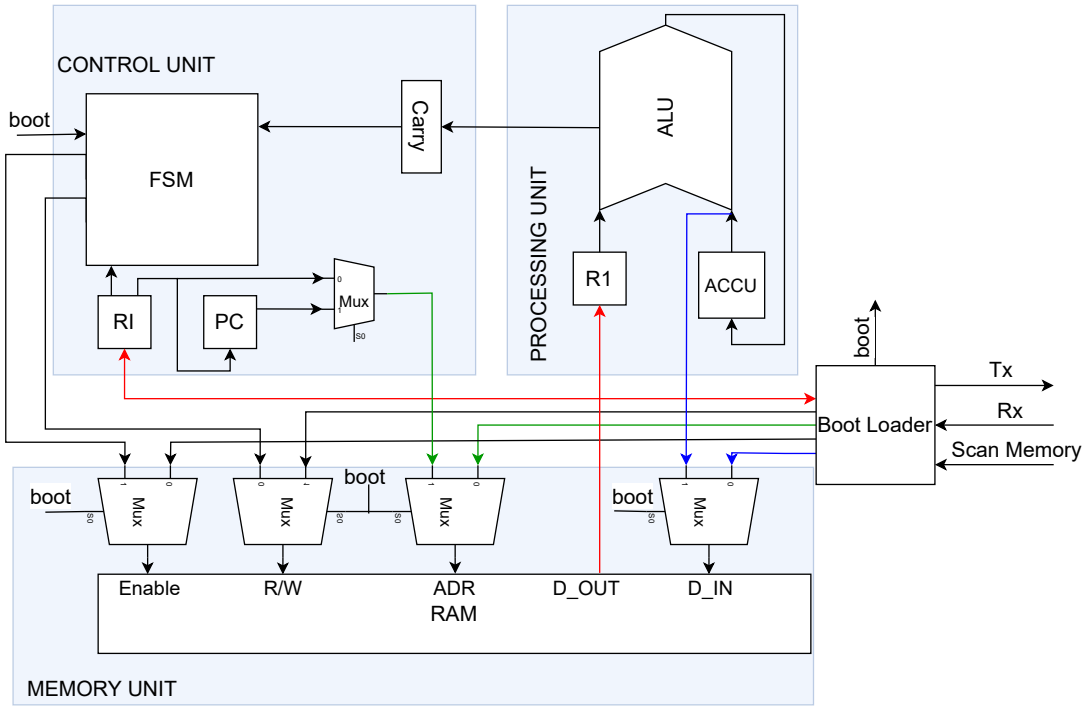



Figure 2.4: Architecture of the MCU.

The CPU functioning can be described as follows: the CU fetches the instruction in the memory and stores it in the RI register. The instruction is decoded to tell which task is loaded in the register. After that the operands are fetched and sent to the Processing Unit. The execution is performed by the Arithmetic Logic Unit and finally the result of the operation is stored in the memory by the Control Unit.

### 2.3.4 The Control Unit

The Control Unit fetches the instructions and controls the Processing Unit. This block can be separated in different parts:

- A register that takes the instructions from the RAM and sends them to the Finite State Machine (FSM) and the Program Counter (PC).
- A program counter that increments at each instruction and sends the address of the next instruction to be executed.
- A Finite State Machine that takes the instructions from the RAM, decode them, fetches the operands related to the instruction and drives the Processing Unit depending on the instruction to execute. This FSM contains ten different states.
- A multiplexer that selects if the address in the memory is driven by the value of the program counter or the value of the instruction register. The condition is given by the FSM depending on its actual state.

### 2.3.5 Processing Unit

The Processing Unit is the module that executes the instructions included in the instruction set and coming from the Control Unit. It can be decomposed in three parts:

- A register loads the value from the memory and send this value to the Arithmetic Logic Unit.
- The ALU performs the instructions and stores the value in an accumulator (ACCU). In this architecture, the first operand is always the value stored in the ACCU, and the result is the new value of this register. An operation can be described as follows :

$$ACCU <= f(ACCU, operand) \tag{2.2}$$

- The content of the register ACCU is reused by the ALU if necessary or is stored in the memory at the address specified by the instruction.

The Processing Unit loads the data at the address mentioned in the instruction and stores its content into the register R1. Then the operands go through the ALU to execute the instruction. Eventually, the result is stored into a memory location.

The advantage of this design is that the Processing Unit operates with two 32-bit registers which are the ACCU and the R1 registers. The resources needed for this block are therefore reduced. The consequent disadvantage is that the instructions are executed one after another, there is no possibility to perform instructions in parallel, so the execution will be longer.

### 2.3.6 The Boot Loader

The boot loader allows the MCU to be reprogrammed, and consequently be adapted depending on the use case or the connected peripherals. The boot loader first loads the program, and then activates the CU to launch the program execution. A signal *scan_memory* is used to send the memory content back to the computer. This allows to reprogram the MCU via the computer and having access to its memory for debugging.

The boot loader is composed of an Universal Asynchronous Receiver Transmitter (UART) and a Finite State Machine. The UART is used to communicate with a computer.

Fig. 2.5 presents the FSM of the boot loader with its consecutive states and the conditions to go from one state to one other.

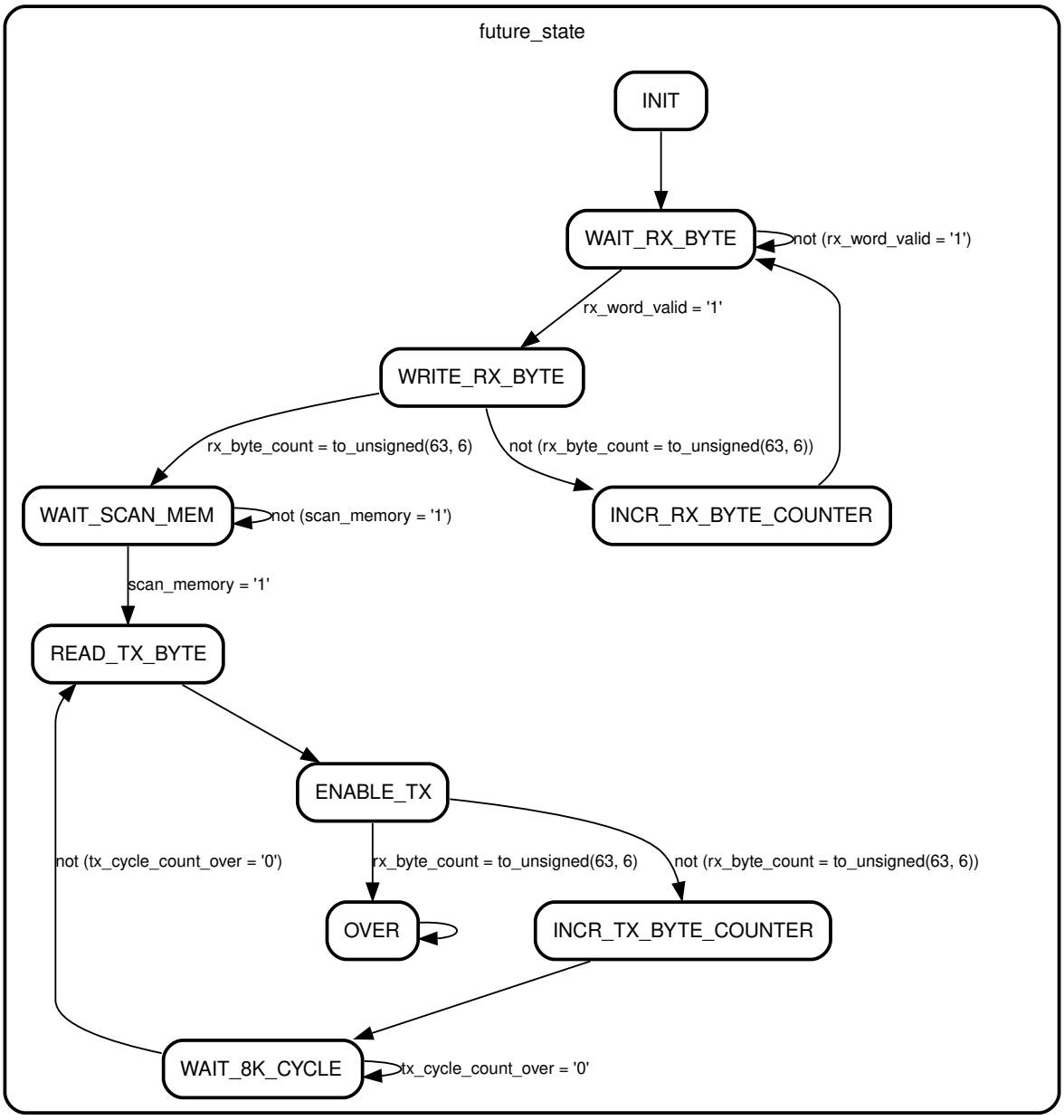



Figure 2.5: Finite State Machine of the Boot Loader.

The boot loader is in the *Init* state, waiting for the program and the data from the computer and then write them into the memory. During this phase, a counter is increasing at each step and the boot loader continues until all the instructions are written in the memory. Once all the data are stored, the boot loader tells the Control Unit to execute the program. The program is running and at the end, if the signal *scan_memory* is set to '1', the content of the memory is sent back to the computer. After that, it goes in an *over* mode to inform that the routine is finished.

It can be noticed than in this configuration, the MCU can carry out only one routine and stops after that. This setting is kept during the design because it is the easier way for debugging. To have a more realistic configuration, the MCU must be configured so that when the boot loader is in the *over* state, it loops back to the initial state and executes the routine when receiving an enable signal. This new configuration requires to modify the state machine in the MCU.

### 2.3.7 Data size

The size of the data the MCU can handle is a key parameter for the circuit design. Depending of the choice that is made, all the instructions, data and operations will have to be coded with a fixed number of bits. It is possible to find MCU with 8-bit to 32-bit architectures. An 8-bit architecture would be simpler, with a smaller footprint and would have a lower power consumption. On the other hand, a 32-bit architecture allows faster execution and more complex computation. In our application, the data given by the sensor are coded on 32 bits and a compensation calculation needs to be executed to have the correct value. Fig. 2.6 presents the temperature compensation calculation necessary to convert the data coming from the sensor.

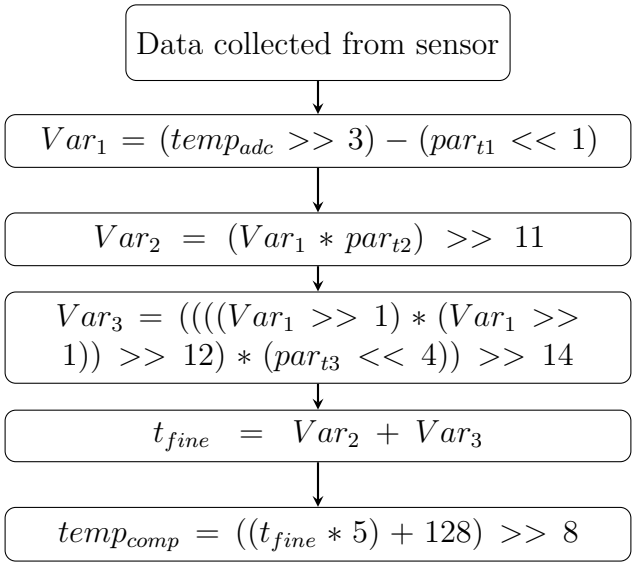



Figure 2.6: Compensation Calculation for Temperature Measurement[64].

Fig. 2.7 presents the assembly calculation for the temperature compensation with a 16-bit and 32-bit architecture. It can be seen that the number of steps with the 16-bit architecture is almost four times more than with the 32-bit architecture. The same ratio can be expected from a 16-bit to an 8-bit architecture. The number of cycles to perform this calculation is therefore much lower with a 32-bit MCU. In an application where the circuit needs to be powered on as few as possible, the minimum calculation time is favored. This is why a 32-bit architecture is chosen.

| | A | B | C | D |
|---|---|---|---|---|
| 1 | 16-bit temperature compensation | ADD CARRY | STA ADDR32 | mov ADDR38,5 |
| 2 | mov ADDR1, ADDR19 | STA ADDR12 | mov ADDR7,ax | mov ADDR38,ax |
| 3 | shr ADDR19,3 | mov ADDR9, ADDR23 | mul ADDR32 | mul ADDR15 |
| 4 | mov ADDR2,ADDR20 | shr ADDR23,1 | mov ax,ADDR33 | mov ax,ADDR39 |
| 5 | shrl ADDR20,13 | mov ADDR10,ADDR24 | mov ADDR8,ax | mov ADDR38,ax |
| 6 | mov ADDR2,ADDR21 | shrl ADDR24,15 | mul ADDR31 | mul ADDR16 |
| 7 | shrr ADDR21,3 | mov ADDR10,ADDR25 | LDA ax | mov ax,ADDR40 |
| 8 | LDA ADDR20 | shrr ADDR21,1 | ADD CARRY | mov ADDR41,128 |
| 9 | ADD ADDR19 | LDA ADDR24 | STA ADDR34 | LDA ADDR39 |
| 10 | STA ADDR22 | ADD ADDR13 | mov ADDR33, ADDR35 | ADD ADDR41 |
| 11 | CLR | STA ADDR26 | shr ADDR35,14 | STA ADDR42 |
| 12 | LDA ADDR3 | mov ADDR26,ax | mov ADDR34,ADDR36 | LDA ADDR40 |
| 13 | NOT | mul ADDR26 | shrl ADDR36,2 | ADD ADDR41 |
| 14 | ADD ADDR21 | mov ax,ADDR27 | mov ADDR34,ADDR37 | STA ADDR43 |
| 15 | STA ADDR9 | mov ADDR25,ax | shrr ADDR37,14 | mov ADDR42, ADDR44 |
| 16 | CLR | mul ADDR25 | LDA ADDR36 | shr ADDR44,8 |
| 17 | LDA ADDR4 | LDA ax | ADD ADDR35 | mov ADDR43,ADDR45 |
| 18 | NOT | ADD CARRY | STA ADDR13 | shrl ADDR35,8 |
| 19 | ADD ADDR22 | STA ADDR28 | mov ADDR37,ADDR14 | mov ADDR43,ADDR46 |
| 20 | STA ADDR10 | mov ADDR27, ADDR29 | LDA ADDR11 | shrr ADDR37,8 |
| 21 | CLR | shr ADDR29,12 | ADD ADDR13 | LDA ADDR45 |
| 22 | mov ADDR9,ax | mov ADDR28,ADDR30 | STA ADDR15 | ADD ADDR44 |
| 23 | mul ADDR5 | shrl ADDR28,3 | CLR | STA ADDR17 |
| 24 | mov ax,ADDR11 | mov ADDR28,ADDR31 | LDA ADDR12 | mov ADDR46,ADDR18 |
| 25 | mov ADDR10,ax | shrr ADDR31,12 | ADD CARRY | |
| 26 | mul ADDR6 | LDA ADDR30 | ADD ADDR14 | |
| 27 | LDA ax | ADD ADDR29 | STA(ADDR16) | |
| 28 | | | | |

(a)

| | A |
|---|---|
| 1 | 32-bit temperature compensation |
| 2 | LDA ADDR1 |
| 3 | SHR ACCU,3 |
| 4 | STA ADDR10 |
| 5 | LDA ADDR2 |
| 6 | NOT |
| 7 | ADD ADDR10 |
| 8 | STA ADDR5 |
| 9 | mov ADDR3,ax |
| 10 | lea ADDR5,ADDR5 |
| 11 | mov ADDR2,ADDR11 |
| 12 | SHR ADDR11,1 |
| 13 | mov ADDR11,ax |
| 14 | lea ADDR12,ADDR11 |
| 15 | SHR ADDR12,12 |
| 16 | mov ADDR4, ax |
| 17 | lea ADDR7,ADDR12 |
| 18 | SHR ADDR7,14 |
| 19 | LDA ADDR6 |
| 20 | ADD ADDR7 |
| 21 | STA ADDR8 |
| 22 | mov 5,ax |
| 23 | lea ADDR13,ADDR8 |
| 24 | LDA ADDR13 |
| 25 | ADD 128 |
| 26 | STA ADDR9 |
| 27 | SHR ADDR9,8 |

(b)

Figure 2.7: Size of Assembly Code in (a)16 and (b) 32 bits.

### 2.3.8 Instruction Set

The instruction set is restricted to the minimum number of instructions to perform the routine presented previously. By doing this, it avoids extra power consumption and current leakage due to additional unused area. The operations needed are those to perform compensation computation to the data coming from the sensor as depicted by Fig. 2.6, and storing data or moving from one instruction to another. Table. 2.3 summarizes the instruction set for the MCU and the detail of the implemented operations.

Table 2.3: Instruction Set of the MCU.

| Instruction | Opcode | Operation |
|---|---|---|
| *NOR* | *000* | ACCU = ACCU NOR Mem[Addr] |
| *ADD* | *001* | ACCU = ACCU ADD Mem[Addr] |
| *LOGICAL RIGHT SHIFT* | *010* | ACCU = ACCU » Mem[Addr] |
| *LOGICAL LEFT SHIFT* | *011* | ACCU = ACCU « Mem[Addr] |
| *MULTIPLICATION* | *100* | ACCU = ACCU * Mem[Addr] |
| *SUBTRACTION* | *101* | ACCU = ACCU - Mem[Addr] |
| *STORE* | *110* | Mem[Addr] = ACCU |
| *JCC* | *111* | if Carry=1 then PC = Addr |

In the 32-bit instructions, the three most significant bits are dedicated to the instruction opcode. The address related to the instruction is indicated in the eight least significant bits.

The accumulator is a special register, where the results of the ALU are stored. The absence of this register would force to store the ALU result in the memory, and then load it back in this memory to perform the next operation. This would slow the operations because the access time to the memory are longer than the access to an internal register. The energy consumption would be also larger.

In the MCUs with an ACCU register, all the instructions will operate on the ACCU and a second register, and all the results are stored in the ACCU. This way, there is no addressing for the result because it stays in the ACCU, except for an explicit *STORE* instruction.

In some architectures containing an ACCU register, other registers can be added to store operands limiting the number of memory accesses and so increasing the instruction execution speed. In this design, the topology with only one ACCU register is preferred to keep the design as simple as possible.

### 2.3.9 Memory

The data in an MCU can be stored into two different types of memory: volatile or non volatile memories. With a volatile memory, if the memory is switched off, the stored data are lost. On the contrary, non volatile memories keep the data even if disconnected from the voltage supply. Usually non volatile memory is used to store the main program while volatile memory is used for temporary variables. All these data are lost when the power supply is disconnected.

Memory is one of the main power consumption factor in a MCU, for reading/writing operations but also for keeping data during shutdown phases. Moreover, memories occupies a large silicon area, which is responsible of non-negligible leakage current. This is the reason why many researches are steered to reduce footprint, dynamic and static power consumption of memories.

In the context of this thesis, the MCU will be regularly disconnected so the main program needs to be kept when the power supply is off. The main program is therefore written in a non volatile memory. A separation can be done between the fixed program and the data, in this application, the instructions are executed on after another, there is no possible access conflict between the instructions and the data. Thus, all the data will be stored into a single memory.

## 2.4 Peripherals

### 2.4.1 Communication Protocols

In order to be able to exchange instructions and data with its peripherals, the MCU needs to have a communication interface, the two more prevalent protocols are Inter-Integrated Circuit (I2C) and Serial Peripheral Interface (SPI). The two communication will be briefly explained, and the interface between the MCU and the chosen protocol will be presented.

#### 2.4.1.1 I2C Protocol

The I2C protocol consists in two wires connecting the master and the several slaves as depicted in Fig. 2.8. One for the Serial Data Line (SDA) and the other for the Serial Clock Line (SCL). The master sends the address of the slave it wants to communicate with, and tells if the operation asked is a read or write operation. After a return of the slave telling that the correct address is received, the master send or receive the data frame accordingly to the operation determined earlier. At each data frame that is sent, a confirmation bit is sent to confirm the correct reception of the frame.

The main advantage of this protocol method is that it needs only two wires to connect several slaves. Nevertheless, the two pull-up resistors draw a high amount of current that can easily go to several milliamperes which is not compliant with ultra-low power applications.

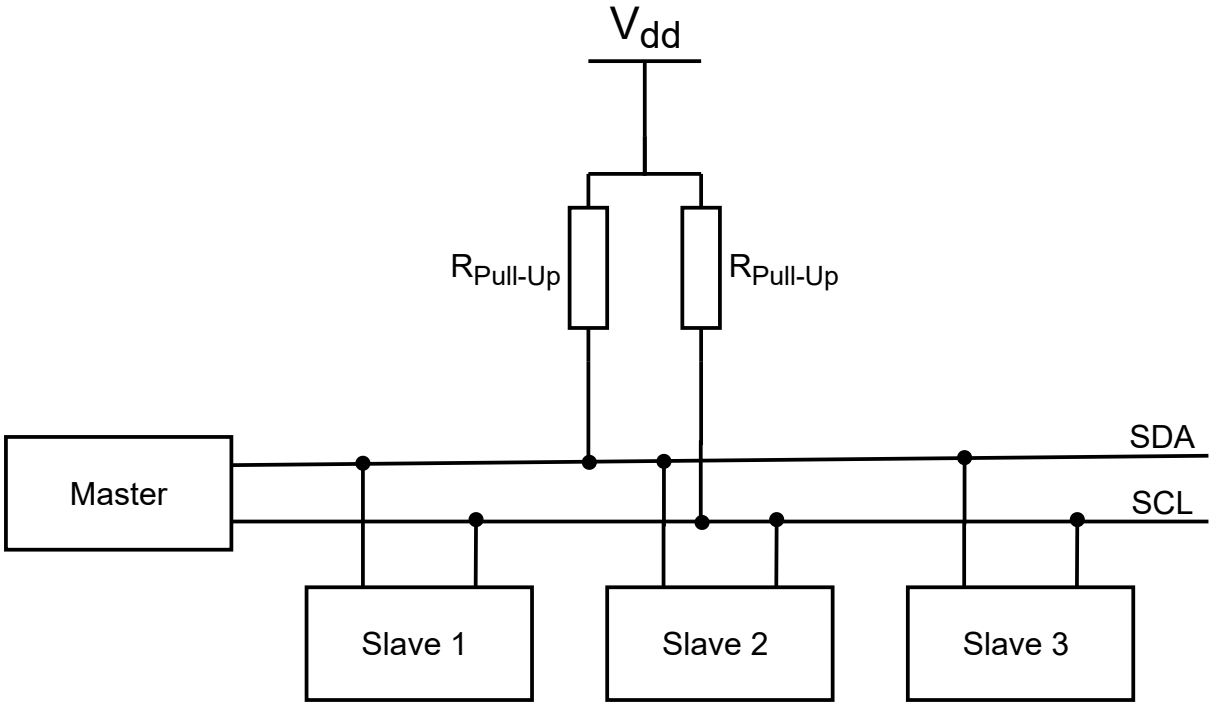



Figure 2.8: Schematic of an I2C Communication.

#### 2.4.1.2 SPI Protocol

The SPI protocol consists in 3 fixed wires: a clock signal (SCLK) a Master Out Slave In (MOSI) signal and a Master In Slave Out (MISO) signal then a Chip Select (CS) wire is added for each slave connected to the master. The wiring of an SPI communication is presented in Fig. 2.9. The functioning of the SPI communication is the following, the master select the slave to communicate with by setting the corresponding chip select to 1 and the others to 0, then the communication is done through the MOSI and MISO wires with the corresponding slave. The advantage of this communication method is that it can support higher communication speed, but most of all, the consumption of this protocol is much lower than the I2C[65]. This is why the SPI communication is chosen for the MCU design.

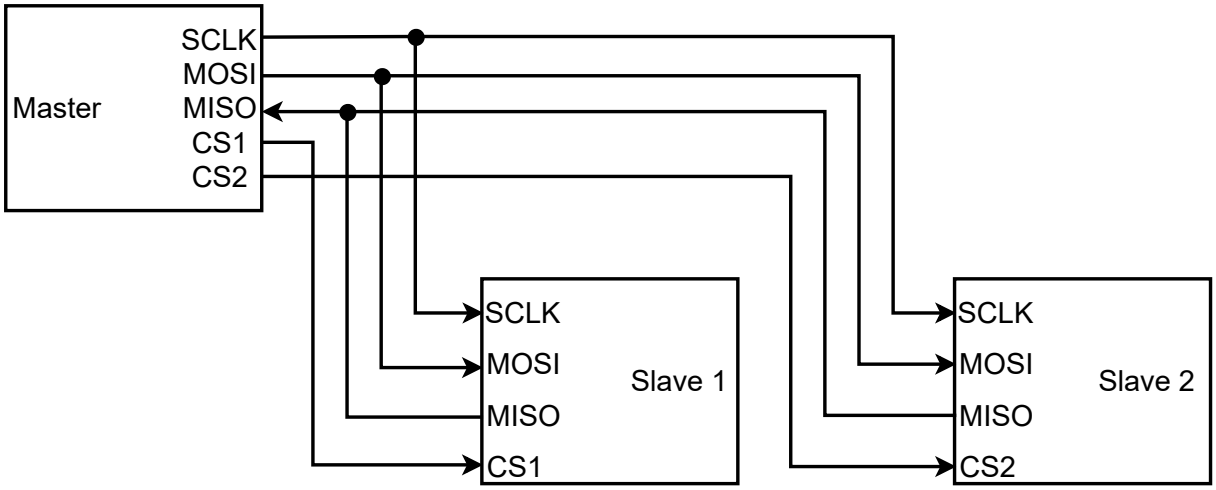



Figure 2.9: Schematic of an SPI Communication.

### 2.4.2 Peripherals Interfacing

The used peripherals for sensing and sending data are the Bosch BME680 sensor [64] and the radio module Spirit1 from STMicroelectronics [66] respectively. Both peripherals support SPI communication and can be interfaced with the proposed MCU.

The peripheral used for power management is the solar energy harvester AEM10941 from E-Peas [67]. This circuit can provide 2 voltage supplies, one at 1.8V and one at 1.2V. These supplies can be set on or off with an enable signal. In this application, the WuRx and the MCU are supplied with the 1.2V output, and the radio and the sensor with the 1.8V. To save power consumption, the MCU sets the 1.8V enable bit to 1 when it is woken up to switch on the peripherals, and when the data gathered from the sensor is sent with the transceiver, the MCU sets the enable to zero to switch off the peripherals.

Fig. 2.10 presents the connection of the SPI with the peripherals, it also shows how an SPI command is organized.

The first two bits are here to determine which peripheral is selected, then seven bits are allocated to tell the number of bytes to send, seven others for the number of bytes to read and finally the data to be sent fill the last eight bits.

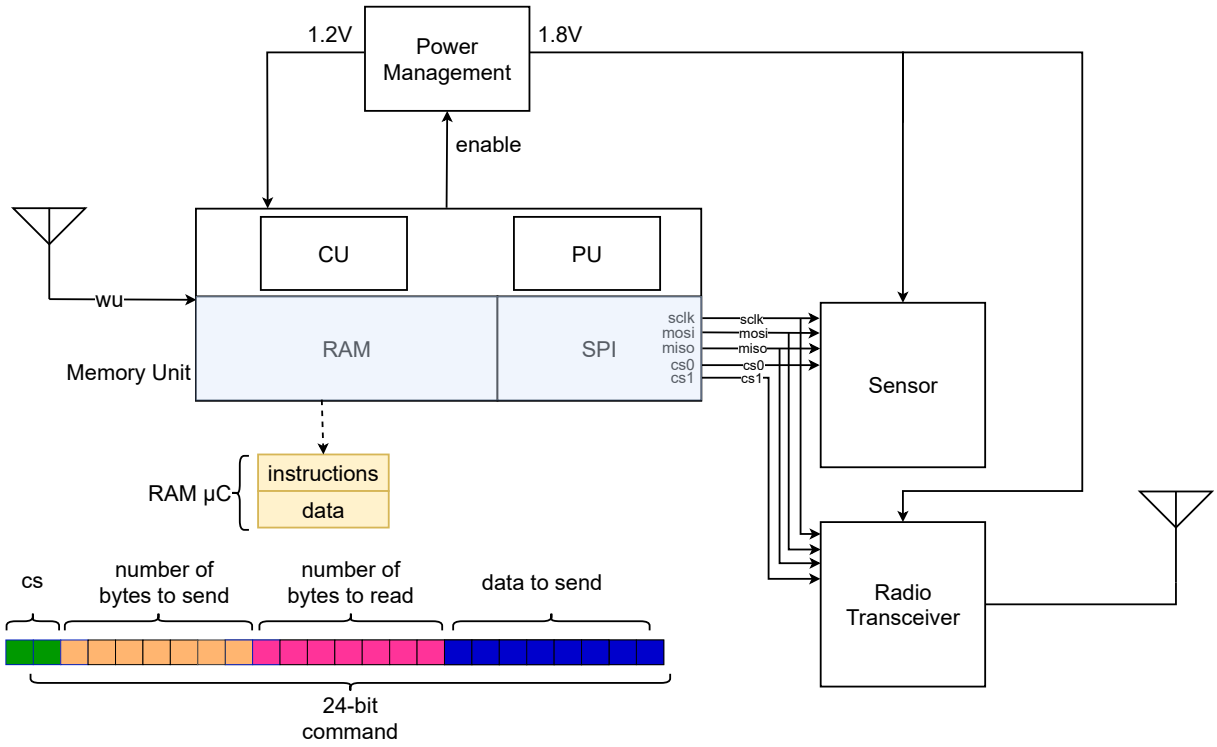



Figure 2.10: Integration of the SPI into the MCU.

From the MCU, there is no difference between the memory and the SPI block, everything is seen as the memory unit. The instructions related to the SPI block are stored as standard data that are loaded in the ACCU. If an instruction needs to go to the SPI, a *STORE* instruction is performed, from here, if the sixteenth bit of the instruction is set to 1, the instruction goes into the SPI block, if the bit is set to 0, the instruction goes into the memory. Fig. 2.11 summarizes the mechanism to differentiate both blocks.

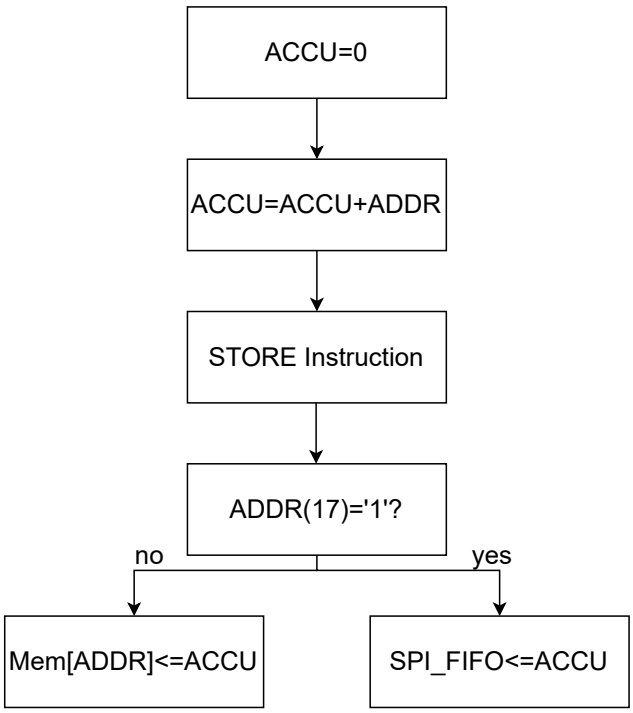



Figure 2.11: Differentiation Between SPI and RAM.

In the SPI block, the instructions are stored into a FIFO until all the instructions are stored. Fig. 2.10 shows that in one instruction, 8 bits are dedicated to the number of bytes to send. For example, if the MCU has to send 3 consecutive bytes, the first instruction mentions that there are three bytes to send with these 8 bits, the second instruction tells that there are two bytes to send and finally the last instruction tells that there is one byte to send. When the SPI sees that the last byte to send is in the FIFO, all the data are sent one after the other. This method allows to send multiple bytes without discontinuity. The same method is used to receive information coming from the peripherals.

It can be seen that 4 peripherals can be used with the microcontroller if needed, and because only 24 bits are needed for one command, a more complete 32-bit command can be imagined to cover more applications. Naturally, this modification would cost a slight increase in the overall power consumption.

## 2.5 MCU Duty Cycling

As it was presented earlier, the purpose of the designed node is to be active only when a request occurs, every time the MCU is switched on, it has a fixed routine to execute. Fig. 2.12 summarizes all the steps of the microcontroller routine after receiving a wake up signal.

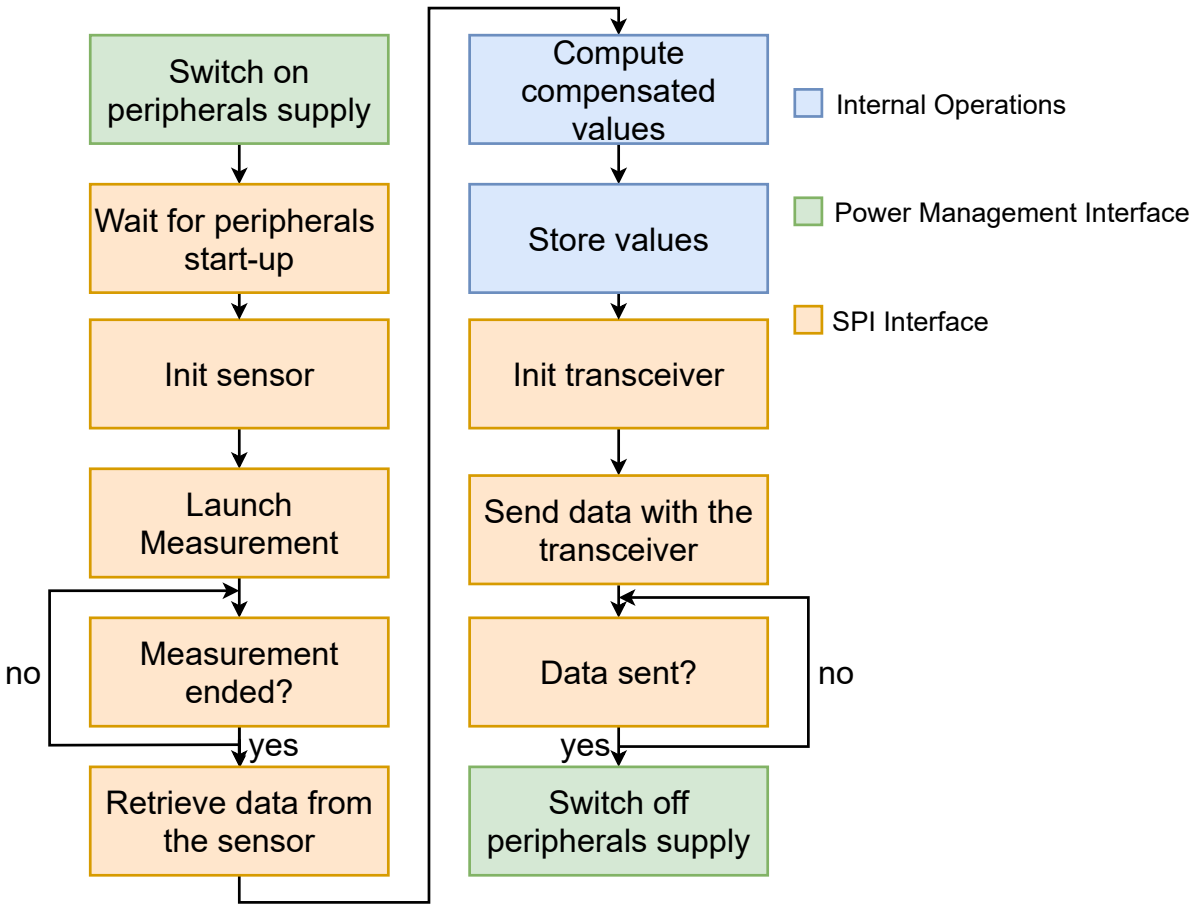



Figure 2.12: MCU Routine.

It must be noticed that after switching on and off the peripherals, the MCU has to check that the sensor is ready to operate and the data are sent by the radio respectively. The first option would be to engage a first communication to see if the sensor is ready, but the SPI is not available during the start-up time. The solution is to add a timer based on the start-up time given by the data-sheet of the component before the SPI communication to ensure the peripherals are on, and then start the routine.

## 2.6 Synthesis

The synthesis of the MCU is performed with Synopsys Design Vision software. At this step, the VHDL description of the MCU in synthesized with digital cells from the ST65nm library. The synthesis is performed for different versions of the design. This allows to have an estimation of the energy cost for each modification. The different power consumption estimations are presented in Table. 2.4.

Table 2.4: Power Consumption Estimation.

| MCU version | Dynamic Power ($\mu W$) | Leakage Power ($nW$) |
|---|---|---|
| **8 bit** | 8.5 | 45.09 |
| **16 bit** | 9.80 | 76.48 |
| **32 bit** | 10.9 | 123.40 |
| **32 bit with instructions** | 10.9 | 129 |
| **32 bit with instructions and SPI** | 13.2 | 170.1 |

It can be seen that the shift from the 8-bit design to the 16 and then 32-bit design lead to an increase of the dynamic and leakage power consumption of 15/10% and 70/60% respectively. The main increase comes from leakage current which increases with the size of the circuit. As explained previously, it can come to mind to use an 8-bit architecture due to the low difference with the 32-bit architecture, but the on-time would be too long and the overall energy consumed for one routine would be higher. Considering the difference between the 16 and 32-bit architectures, the dynamic power consumption with the 32-bits MCU is 10% higher but as presented by Fig. 2.7 it needs almost four times less instructions to perform the same routine. So for this routine this energy consumption is more than 70% with the 32-bit design. This shows the advantages of increasing the size of the MCU.

The same estimation is performed for the MCU area. The results are shown in Table. 2.5.

Table 2.5: Area Estimation.

| MCU version | Area($mm^2$) | CU | PU | BL | RAM | SPI |
|---|---|---|---|---|---|---|
| **8 bit** | 0.011 | 3.9% | 3.4% | 28.6% | 63.4% | – |
| **16 bit** | 0.019 | 2.4% | 3.9% | 19.3% | 73.8% | – |
| **32 bit** | 0.033 | 1.4% | 4.5% | 9.9% | 83.7% | – |
| **32 bit with instructions** | 0.035 | 1.2% | 9.3% | 9.4% | 79.6% | – |
| **32 bit with instructions and SPI** | 0.043 | 1.09% | 6.75% | 8.16% | 64.83% | 17.6% |

With the increase of the data size, the Processing Unit and the RAM occupy more space than the other blocks. The SPI bloc occupies 17.6% of the area itself, it can be reduced by sizing the FIFO at the exact size for the application but at the cost of a lower flexibility. It can be noticed that the major part of the area is dedicated to the memory, this confirms the decision that was made to choose the technology depending on the memory performance.

The MCU designed was implemented on a Nexys 4 DDR FPGA to validate the architecture, the schematic of the demonstrator is presented in Fig. 2.13. For the demonstration, the MCU is implemented in the FPGA, the code is sent by the computer through the UART, the FPGA gathers the data from the sensor, performs the compensation calculation and sends them with the radio. The received data can easily be recovered thanks to a software linked to the radio. In case of debugging, an access to the memory is possible with the UART to send its content to the computer and check the mistakes.

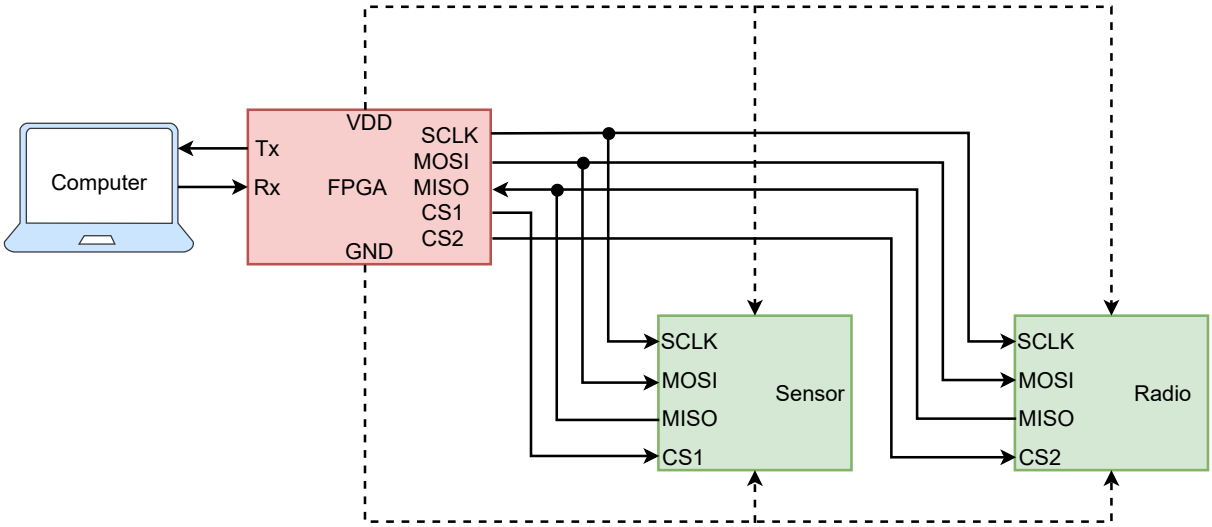



Figure 2.13: Schematic of the Demonstrator.

The demonstrator is presented in Fig. 2.14.

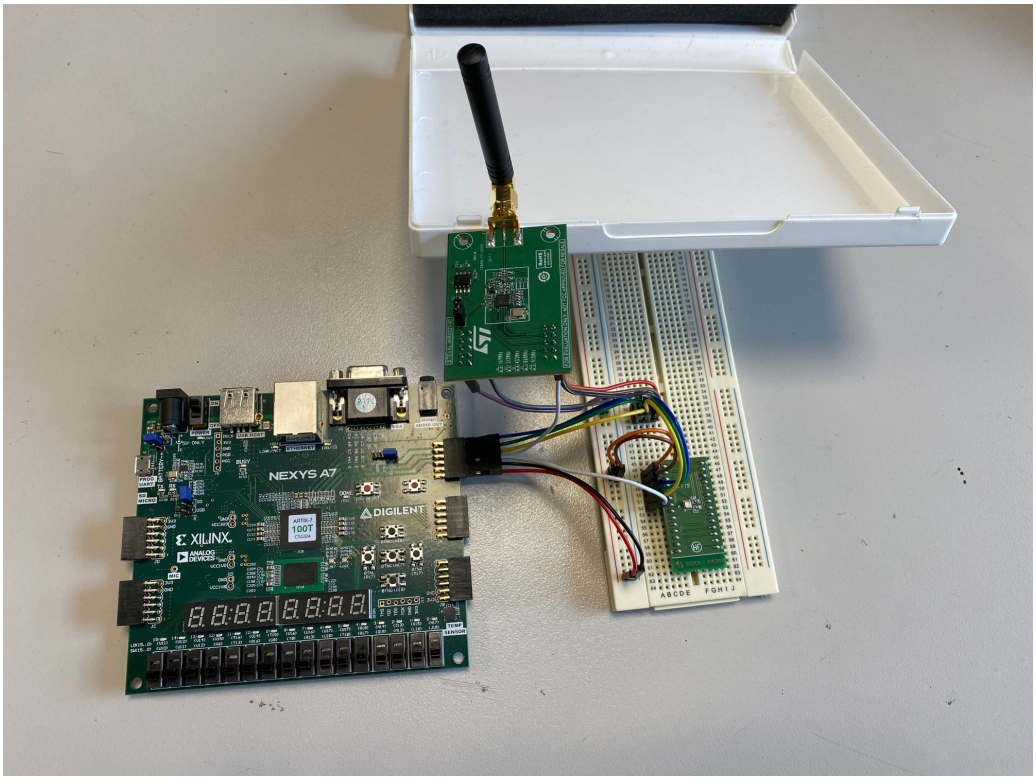



Figure 2.14: Demonstrator (on the left) with Sensor (on the right) and Transceiver (on top).

A comparison of the performance of the designed MCU is done with 3 high performance MCUs, by Microchip Technology, STMicroelectronics and E-Peas respectively. The results are summarized in Table. 2.6.

Table 2.6: Power Consumption Comparison.

| | This Work* | [[68]] | [[69]] | [[55]] |
|---|---|---|---|---|
| **Dynamic Power**($\mu W$) | 13.2 | - | - | |
| **Active current**($\mu A/MHz$) | 0.1 | 500 | 88 | 18 |
| **Active power**($\mu W/MHz$) | 0.11 | 1150 | 145.2 | 32.4 |
| **Voltage Supply**($V$) | 1.2 | $2.3-3.6$ | $1.65-3.6$ | $1.8-3.3$ |
| **Frequency**($MHz$) | 100 | 40 | 32 | 24 |
| **Current in Sleep Mode**($nA$) | – | 673 | 800 | 340 |
| **Leakage Current**($nA$) | 142 | $\approx 500$ | $\approx 500$ | – |
| **Number of peripherals** | 2 | $8-11$ | 10 | $8-48$ |

(*) PLS Results

The designed MCU presents a power consumption much lower than other markets components mainly due to a sober design and also a lower voltage supply. It can also be noticed that the leakage is also reduced almost three times compared to other circuit, here again, this is the consequence of a design occupying a smaller silicon area. One of the counterparts of this design is that it can address only 2 peripherals while other market components can easily go up to 10 peripherals. It must be said that even if the results in term of power consumption are very good, what really matters is the energy consumption. The other MCUs can do tasks in parallel what the designed MCU cannot do, so the execution time will probably be longer with the proposed MCU. On the other hand, the proposed MCU has a clock more than twice the clock frequency of the other circuit, so the instructions will be executed faster. The differences of architectures implies many parameters making hard to depict a clear difference. To have a perfect comparison, it is necessary that all the MCUs perform the same task with the same optimization level, and then the comparison would be the most accurate. Another important point is that the synthesis tool does not generate the clock signal, so the results here are the results of the MCU without its clock while it is included in the other MCUs, if we look at the state of the art, we can say that a 100MHz clock can be generated for less than 100µW, this parameter thins the difference between the circuit down.

The layout is done using Cadence Encounter. Thanks to the verilog file of the synthesized design, the layout is made following drawing rules. A power ring is drawn around the core circuit and filler cells are added to fill the gaps. Fig. 2.15 presents the layout of the designed MCU. The dimensions of the circuit without the pads are $340 \times 190 \mu m^2$

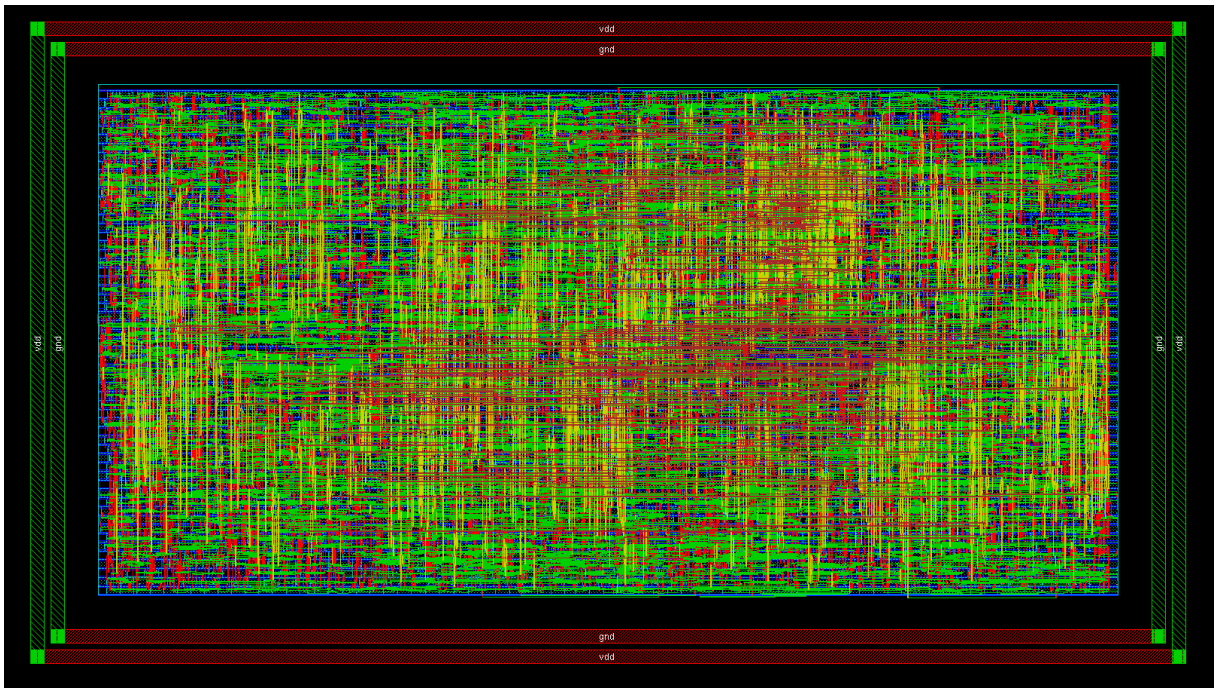



Figure 2.15: Layout of the MCU Core.

## 2.7 Conclusion

This chapter has presented the design of a custom low-power MCU for a wireless sensor node. The approach for the design of this circuit is as follows:

1. Use of a minimalist design as a basis,
2. Resizing of the circuit in a 32-bit format,
3. Addition of the relevant instructions for the application,
4. Design of the interfacing with the peripherals,
5. Demonstration of the design on FPGA,
6. Layout and synthesis of the circuit.

This approach led to the design of a 32-bit MCU in 65nm technology with 8 instructions and an SPI communication peripheral. The core of the designed MCU presents a dynamic power of 13.2$\mu$W and 142nA of leakage current when supplied at 1.2V. The circuit operates with a clock frequency of 100MHz and can be connected with two peripherals with a communication frequency up to 10MHz. The circuit can also switch on and off a power management unit thanks to an enable output signal.

This design allows to have a circuit with a lower power consumption than market components, functioning at a clock frequency more than twice the frequency of these market products.

An improvement that can be considered is the addition of a compiler to convert the code from a higher level language. This would allow more flexibility and more ease than coding in assembly by hand. But this modification would be at the cost of a larger circuit, more consumption and more leakage current. Moreover, adding some ACCU registers to store data and avoid memory access could improve the MCU performance at small costs.

Another point of questioning is the use of an other architecture. This work presents a specific design but others can be considered such as the RISC V architecture which is very popular nowadays. It would be interesting to compare the presented designed with a refined MCU based on a RISC V.

The next step of this work is the manufacturing of this circuit to be implemented in a real wireless sensor node. To do that, the UART interface with the computer can be removed and the program can be written into a hard memory. A co-integration with the Wake-Up Radio that will be presented in the next chapter will be considered.

# CHAPTER 3

# WAKE-UP RADIOS

## 3.1 Introduction

The first chapter showed that the idle power consumption represents a bottleneck in wireless sensor nodes lifetime. This is why WuRx are added. This block is always on and switches on the node when a request occurs. Fig. 3.1 reminds the position of the WuRx in the node.

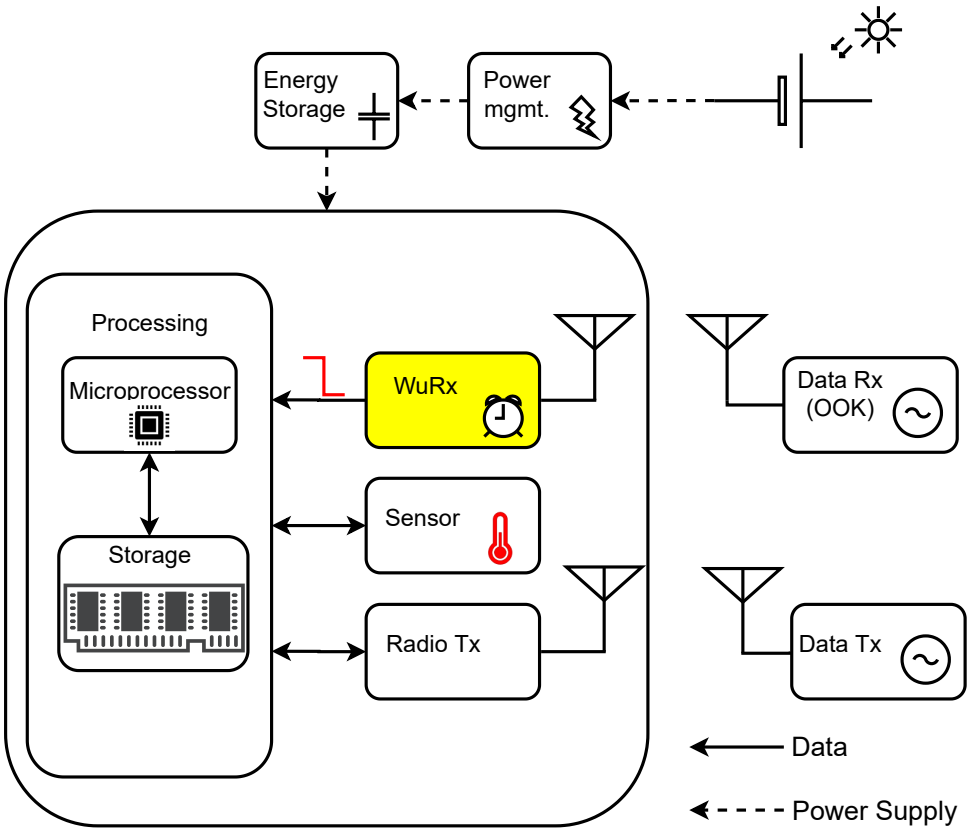



Figure 3.1: Position of the WuRx in a Node.

A WuRx is composed of different consecutive blocks as illustrated in Fig. 3.2:

- A matching network which also performs filtering after the antenna ,
- An envelope detector to convert the AC incoming signal into DC signal,
- A comparator to convert the output of the envelope detector into digital signal,
- A correlator to compare the incoming code with a reference code,
- An oscillator to clock the comparator and the correlator.

This chapter will present the implementation of these functions, including: the concept of operation, the circuit schematic and the Post-Layout Simulation (PLS).

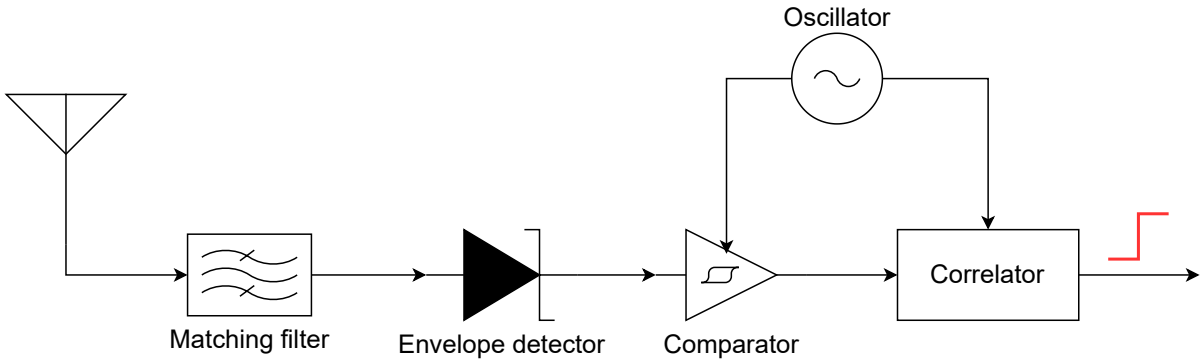



Figure 3.2: Schematic of a WuRx.

## 3.2 Envelope Detector

### 3.2.1 Overview

The first active block of the WuRx is the Envelope Detector (ED) which follows the variations of the input signal's envelope. Because the signal is an OOK -i.e a signal is sent or not- the output of the ED will be a positive DC voltage or 0 voltage respectively. The main metric defining an ED in this application is the sensitivity which is the minimum input power required by the ED to properly detect the OOK modulated signal.

The target is to design a circuit which can reach enough output voltage to trigger the next comparator block at the lowest sensitivity. Several topologies exist for EDs, from totally passive to clocked circuits. For the purpose of this thesis which is to reduce as much as possible the power consumption, a focus was made on passive topologies.

State of the art circuits use pseudo-differential topologies[70],[71],[72],[73],[74],[75] and some use active biasing. The advantages of these topologies is that the differential structure allows an inherent 3dB gain of sensitivity.

However the negative excursion of a modulated signal rectified by a pseudo differential architecture can be an issue for the comparison stage following the ED. Indeed the negative part of the signal biases the transistor parasitic diodes and increases the current consumption. Besides the circuits require a trimming process to adjust the performance. The target here is to provide a robust and simple circuit so the active-based differential topologies are left aside for fully passive operation.

### 3.2.2 Envelope Detector topology

The proposed design is a cross-coupled envelope detector. The purpose is to cascade several stages likewise voltage multipliers but combined with a cross coupling technique. The cross coupling allows to improve the performance of traditional topologies[76]. As presented in Fig. 3.3, one stage consists in four transistors operating in pair to form two voltage multipliers.

The fundamental operational principle is as follows: during the positive half cycle of the input signal, $V_{CG+}$ is set to a high level, while $V_{CG-}$ is kept low. Consequently, $M_2$ and $M_3$ transistors are activated, while $M_1$ and $M_4$ remain off. As a result, the current passes through $M_2$, leading to the accumulation of charges into $C_{IN-}$ via $M_3$.

In the subsequent half of the cycle, $M_2$ and $M_3$ are turned off, and $M_1$ and $M_4$ are switched on. At this point, the current flows through $M_4$, causing the charge to be stored into $C_{IN+}$ via $M_1$. To turn the transistors on, the $V_{GS}$ voltage must be greater than the

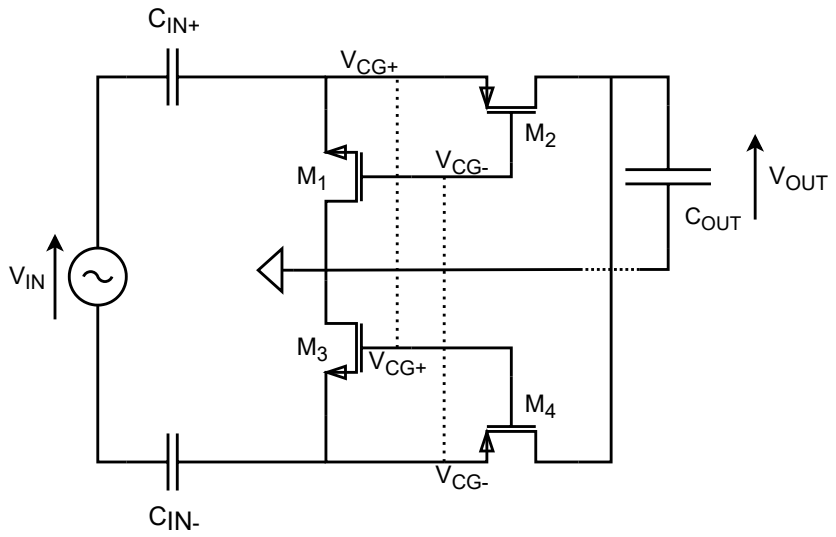



Figure 3.3: Schematic of a Single Stage Cross-Coupled Envelope Detector.

threshold voltage. The gate and source terminals of M1 and M2 follow $V_{CG+}$ and $V_{CG-}$, which are out of phase. Then, when source voltage is slightly below $-\frac{V_{Th}}{2}$, gate voltage is slightly above $\frac{V_{Th}}{2}$, making a $V_{GS}$ required for transistor conduction . Thanks to this technique the threshold voltage is decreased by 50% in comparison with standard voltage multiplier[77]. The available output voltage can be expressed as:

$$V_{out} = 2V_{in} - V_t \tag{3.1}$$

If n stages are stacked as shown in Fig. 3.4, the output voltage is

$$V_{out} = n * (2V_{in} - V_t) \tag{3.2}$$

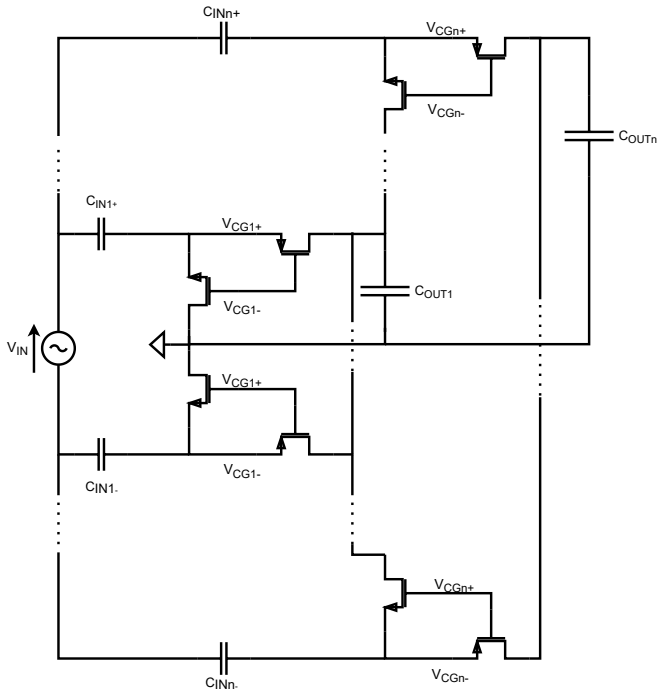



Figure 3.4: n-Stage Cross-Coupled Envelope Detector.

Whereas the output voltage increases by cascading the stages, the overall efficiency does not. Indeed, with more transistors, a higher amount of signal will be lost in leakage.

With this topology, the impact of the threshold voltage of the transistors is limited, which contributes to increase the efficiency and the sensitivity of the ED. The targeted performance is an output voltage of 45mV, eight cascaded stages are needed.

### 3.2.3 Design and implementation

Fig. 3.5 presents the layout of the envelope detector, the dimensions of the core are $117\mu m \times 100\mu m$. The input capacitors can be seen on the matrix on the left, the inter-stage capacitors are located on the bottom right and the transistors are put in a matrix on the up right. The layout for each stage is identical to ensure more robustness for the circuit.

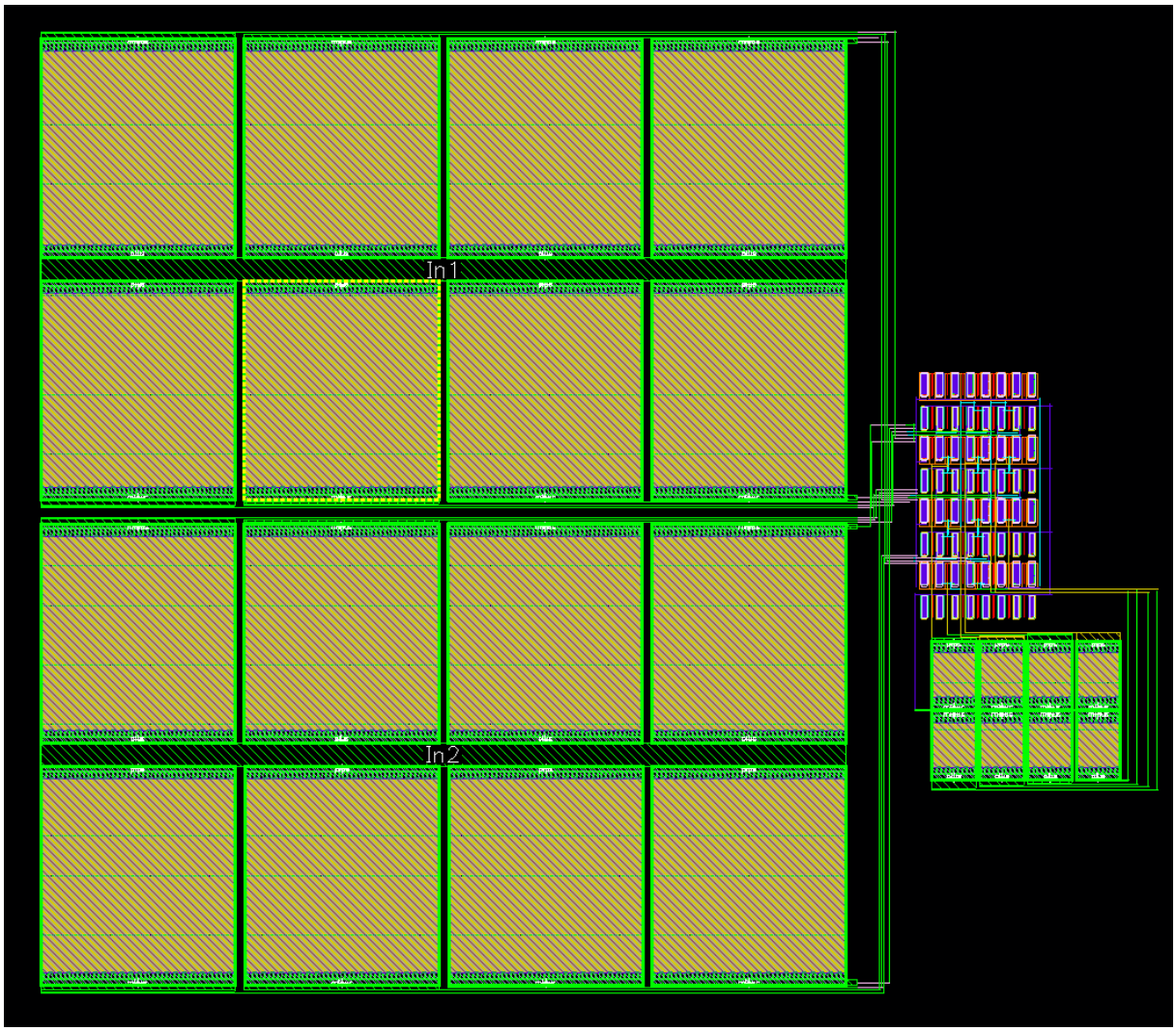



Figure 3.5: Layout of the Envelope Detector.

Fig. 3.6 presents the output voltage of the envelope detector for an input power of -26dBm. The target output voltage of 45mV is reached by the circuit. It can be noticed that the time to reach this value is under $100\mu s$, this will cause no issue because the period of the input signal is 1ms. There is enough time to rectify the signal correctly.

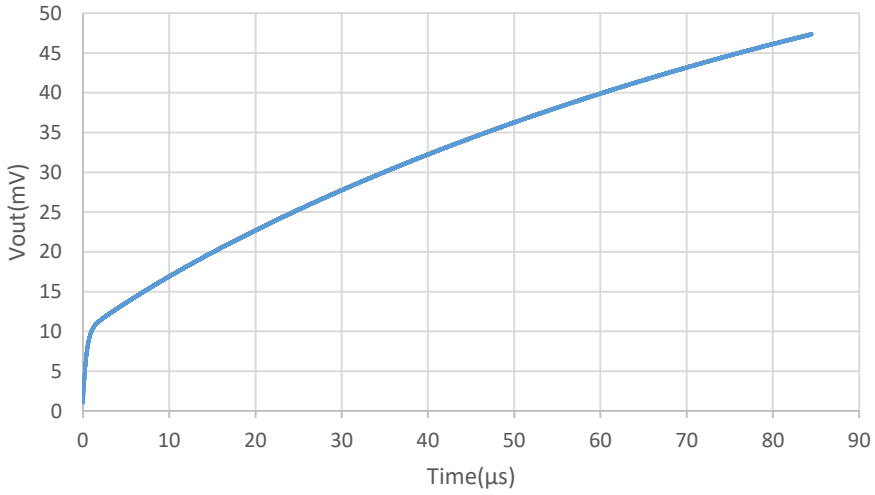
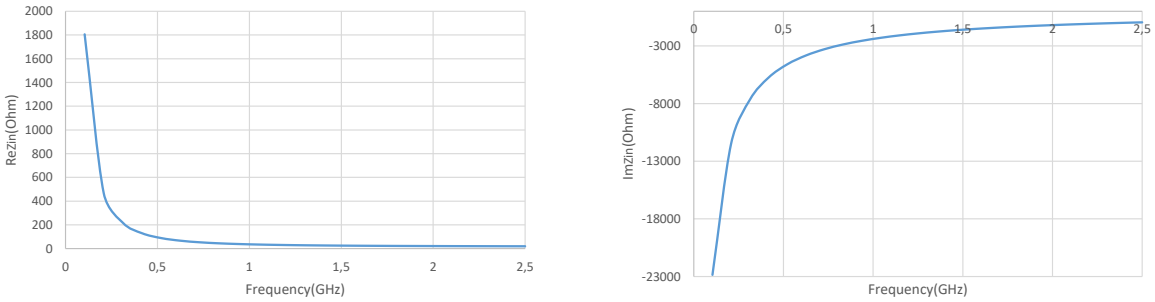



Figure 3.6: Output Voltage of the Envelope Detector.

### 3.2.4 Matching Network

Fig. 3.7 presents the input impedance of the envelope detector depending on the frequency. The circuit has a capacitive behavior with an important imaginary part at low frequency, below 500MHz.




(a) (b)

Figure 3.7: Impedance of the Rectifier (a) Real Part (b) Imaginary Part.

The ED can be matched by adding two serie inductors at the input of the circuit. A resonance is created at the targeted frequency, which provides a passive voltage gain thus increasing the sensitivity of the circuit. To reduce the footprint of the circuit, the real part will be matched directly with an antenna adapted for each frequency, this allows to have better performances than with a 50 Ohms antenna, at the cost of a narrower matching bandwidth.

Fig. 3.8 shows the schematic of the envelope detector with the matching inductances at the input. The value of inductors required to perform the matching is large. To ensure a high quality factor we will use off-chip inductors.

Table. 3.1 presents the sensitivity of the envelope detector with matching inductances for an input frequency of 400MHz, 900MHz and 2.4GHz. The sensitivity decreases from -59dBm to -54dBm mainly due to the lower passive voltage gain of the input matching network at higher frequency.

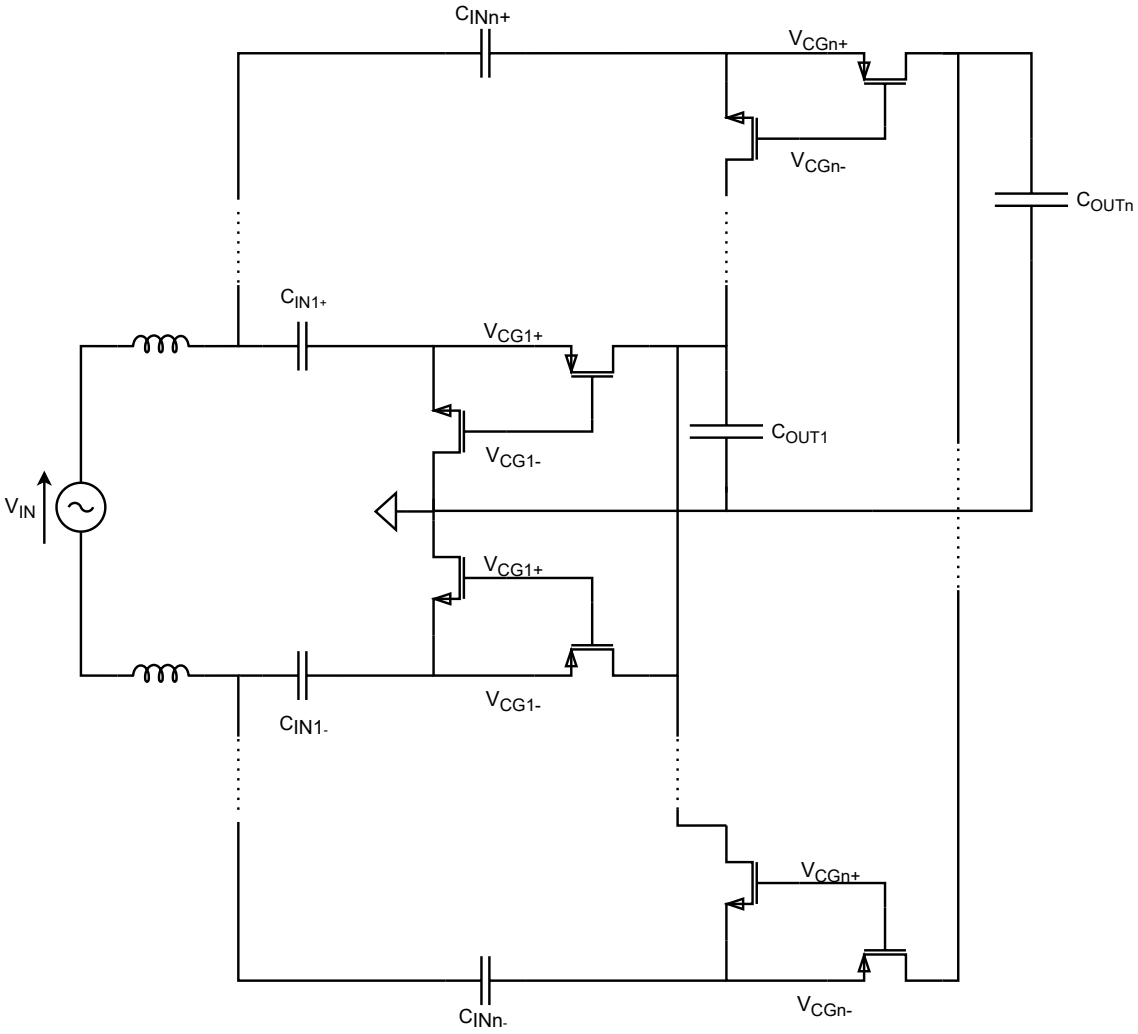



Figure 3.8: Envelope Detector with Matching.

Table 3.1: Envelope Detector Sensitivity at Different Frequencies.

| Frequency (GHz) | 0.4 | 0.9 | 2.4 |
|---|---|---|---|
| Matching inductance (nH) | 1200 | 240 | 33 |
| Sensitivity @ 50 Ohms (dBm) | -55 | -53 | -50 |
| Sensitivity with Custom Antenna | -59 | -57 | -54 |

Fig. 3.9 shows the input matching of the envelope detector for the three different operating frequencies. With the suitable inductance values, the circuit exhibits an $S_{11}$ of -16dB, -22dB and -25dB at 400MHz, 900MHz and 2.4GHz respectively.

It can be noticed that the circuit is very narrow-band with a -10dB bandwidth of 10MHz for the first two frequencies and 30MHz for the latter. This narrow bandwidth is explained by the high resonance generated by the matching network.

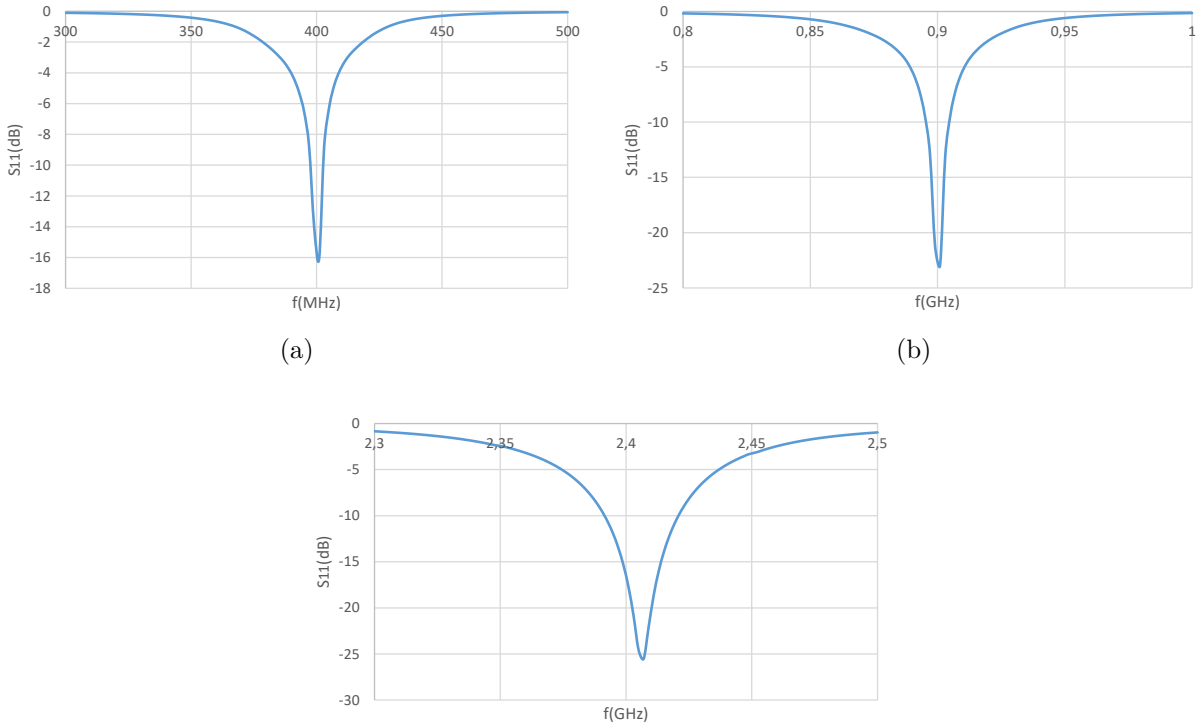



Figure 3.9: Envelope Detector $S_{11}$ Parameter at (a) 400MHz (b) 900MHz (c) 2.4GHz.

## 3.3 Comparator

### 3.3.1 Overview

After detecting the envelop of the modulated RF input signal with the ED, the base-band OOK signal must be converted into a digital signal. The digitization is performed by the comparator stage.

The metrics of interest for the comparator in this application are: the delay, the offset voltage and the power consumption. The delay corresponds to the time the comparator needs after the clock signal to set the output at the correct value. The delay needs to be lower than the clock rate to ensure handling all the incoming bits. The offset voltage is the threshold to exceed between the two inputs to make a decision on a ”1” or a ”0”. Ideally this value is zero but due to non ideal conditions this value is higher. The target is to have an offset as low as possible to increase the sensitivity. And finally the power consumption is a combination of static and dynamic power consumption. The static consumption corresponds mainly to current leakage and the dynamic consumption is generated by switching events during the comparison. The power consumption is the main parameter to consider in this work and it will be minimized in this circuit. Eq. 3.3 shows the power consumption of the comparator, which depends on the clock frequency, the supply voltage, the load capacitance and the current leakage.

$$P_{total} = f_{CLK}.C_L.V_{DD}^2 + V_{DD}.I_{LEAKAGE} \tag{3.3}$$

### 3.3.2 Comparator topology

Here again, a huge amount of designs can be found, the scope is limited to dynamic comparators. These topologies are driven by a clock signal and do the comparison only when the clock signal is high. In such manner, the comparison is performed only at a certain rate and the circuit is disconnected from the power supply during the rest of the time, which allows to save an important amount of energy. With a clocked comparator the second term of the power consumption in Eq. 3.3 can be neglected.

The designed comparator is inspired from [78]. As presented in Fig. 3.10, it consists in a two-stage comparator with a clocked differential pair for the first stage and a latch for the second stage. The operation is as follows : when a high level comes at the comparator input, it will unbalance the output between the two stages, which will trigger the latch at the second stage and force its output to one or zero depending on the node.

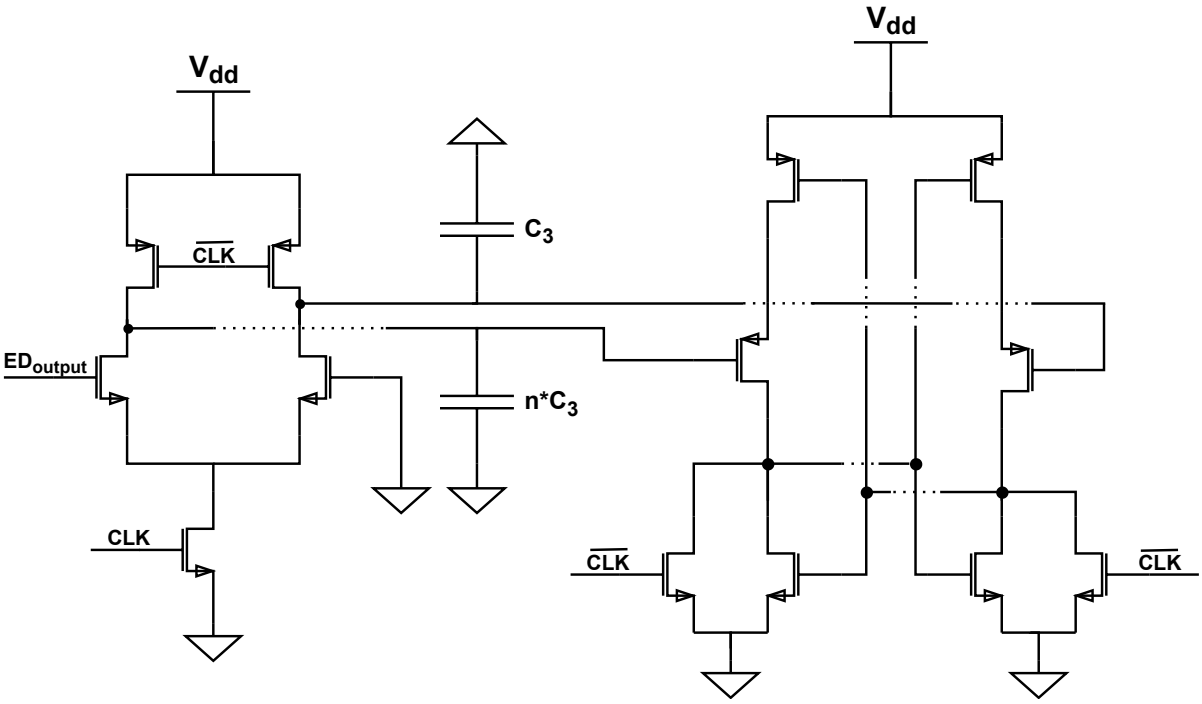



Figure 3.10: Schematic of the Comparator.

The main issue of such arrangement arises when the two inputs are both set to zero. In this case, the behavior of the circuit is uncertain, and the outputs are not correctly established, which can result into false zeros or false ones. To overcome this issue, a solution is to connect two capacitances of different values between the two stages (C3 and n*C3 here). To this extent, if the first input is at high level and the second connected to the ground, the comparator will work as previously. But when the two transistors have the same input (i.e are connected to the ground), they will draw the same amount of current and the capacitors will not charge at the same speed because one capacitor is smaller. The latter (C3 in Fig. 3.10) will charge faster and so trigger the second stage first and force the comparator decision. This way it allows to ensure the decision of the comparator when it has a zero input without adding extra power consumption.

### 3.3.3 Design and implementation

Fig. 3.11 presents the layout of the comparator, the dimensions of the core are $26\mu m \times 8\mu m$. The capacitors between the two stages are on the right and the transistors are in the matrix on the left. The ratio between the two capacitors is 1:3, to have a better matching and more robustness, capacitors of the same size are used and connected in parallel.

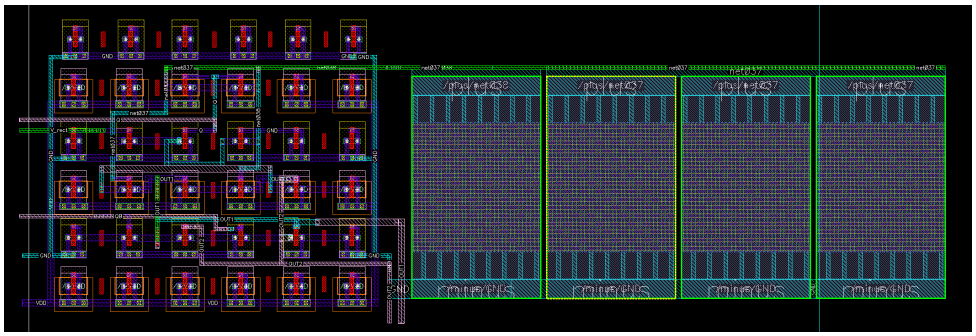


Figure 3.11: Layout of the Comparator.

Fig. 3.12 presents the response of the comparator in Post-Layout Simulation.

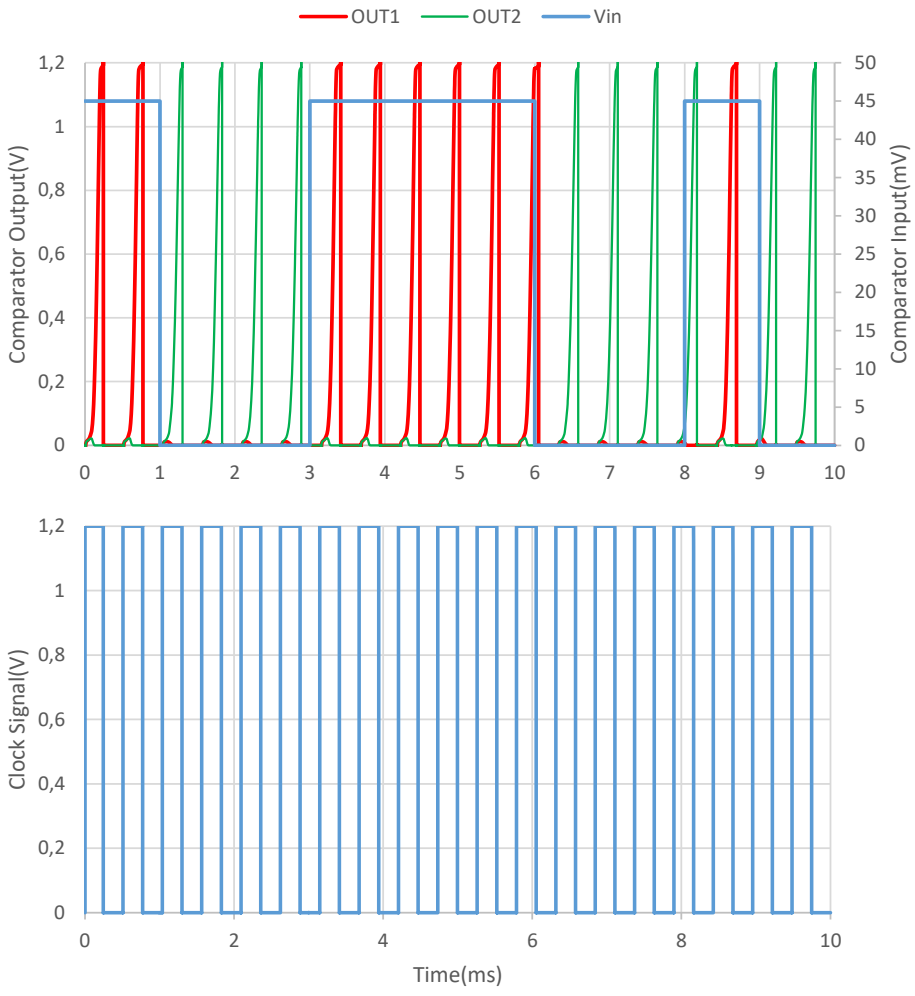



Figure 3.12: Comparator Response.

The input is a square wave with an amplitude of 45mV which is slightly above the comparator offset. The output 1 corresponds to the correct demodulation i.e it gives high level when the input is at 47mV and low level when it is zero. The other output gives the correct complementary, when the input is zero the decision is always forced to the second output. This figure proves the operation of the comparator in PLS. To workout the comparison delay a focus on the rising edge is reported din Fig. 3.13. The observed delay is approximately 0.15ms. In this application, because the signal switches with a period of 0.5ms, this is not an issue, there is enough time to do the comparison including this delay. If the circuit has to be designed for higher data rates, this delay should be considered. It is possible to increase the speed by increasing the tail current of the first stage[79] but this will increase the average power consumption.

The falling edge has near zero delay. The time response of the circuit is suitable with the frequency of the oscillator and the charge or discharge time will not corrupt the data stream. However the interfacing of the correlator with coppartor can be an issue, this will be discussed in the following section.

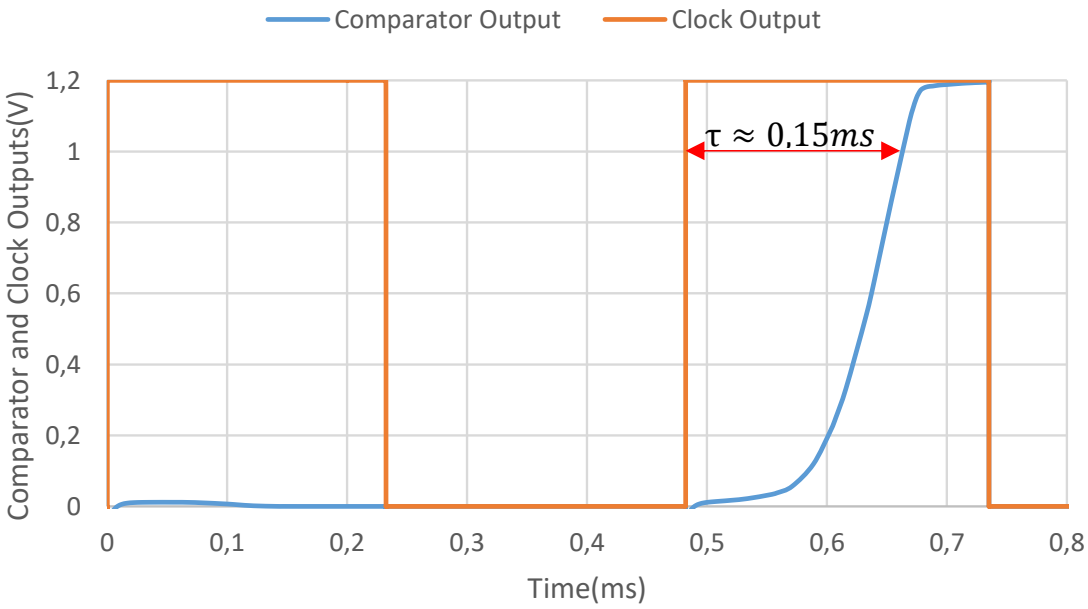



Figure 3.13: Comparator Delay.

Concerning the input offset voltage, [79] demonstrates that this offset depends on the inverse of the square root of the transistor size. The expression of the offset is given:

$$\Delta V_{th} = \frac{A_{vth}}{\sqrt{WL}} \tag{3.4}$$

Where $A_{vth}$ is a constant and $W$ and $L$ are the dimensions of the input transistors. According to [80], the parameter $A_{vth}$ in 65nm technology should be between 4 and 4.5mVµm. In this design, the transistor width is 10µm and the length is 100nm. This leads to an offset between 34 and 39mV. The comparator having a sensitivity of 45mV, the result is close to the theory. The difference can be explained by the parasitic components extracted from the layout.

Eq. 3.4 shows that with larger transistors, this offset should be lower, and so the sensitivity can be increased. Naturally, this would be at the cost of a higher power consumption.

In this application the target is to reach the lower power consumption, the sizing with the smaller transistors is preferred.

## 3.4 Correlator

### 3.4.1 Overview

Now that the input signal is digitized into a bit sequence, the circuit has to check if the incoming signal corresponds to a request or not. To perform this operation, a correlator is designed. The incoming signal is compared to an established code word and if the two codes have a number of bits in common higher than a fixed threshold, the wake-up signal is generated.

### 3.4.2 Correlator topology

Usually, correlators are used to identify different codes or message in channel coding for example, this allows to decode different words or instructions during a communication. For example in this application, this could be used to allocate different scenarios for different codes. The increase of the number of codes leads to more complex architectures. In the context of this thesis, the purpose is to implement a single code word to minimize the design complexity and the power consumption. The architecture of the correlator is presented in Fig. 3.14. The reference code is a 32-bit word. The input signal goes into 32 shift registers and at each clock edge, a comparison is done between the content of the registers and the reference word.

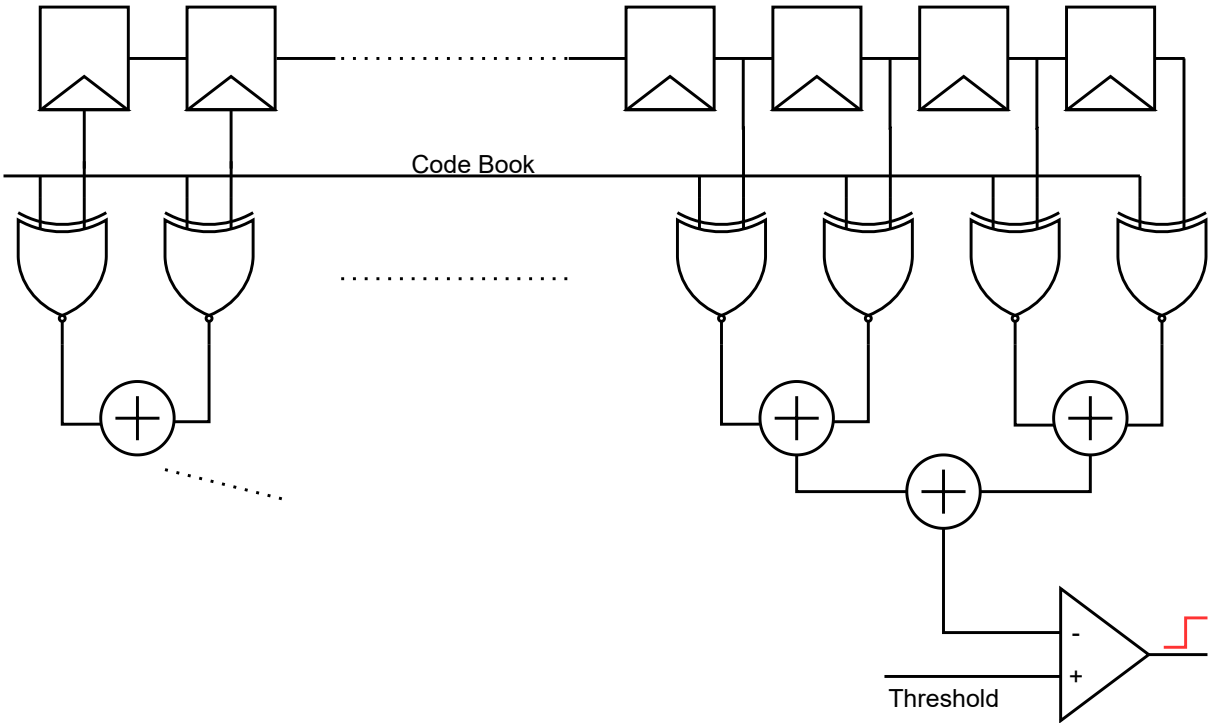



Figure 3.14: Correlator Schematic.

To do the comparison between the bits, XNOR gates are used. Indeed the output of this gate is one only if the two input bits are similar as reminded by Table. 3.2. After that, the outputs of all the gates are added and compared to a fixed threshold. This circuit is designed in VHDL. To avoid false wake-ups, it is important that the code word cannot be confused with its shifted versions. To do so, the words has to be designed to have the

Hamming distance(i.e the number of non corresponding bits) as high as possible between the word and its shifted versions.

Table 3.2: Truth Table of a XNOR Gate.

| $IN_1$ | $IN_2$ | $OUT$ |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

The synchronisation with the comparator was mentioned in the previous section, because the comparator has a rising time delay after a clock rising edge, the correlator which is triggered by the same clock will probably miss the data. The solution to avoid this problem is to use the complementary clock, indeed the rising edge of the complementary corresponds to the falling edge of the first clock and so if the comparator is supposed to give a 1, the output will be high at this moment. This solution allows not to lose any data at zero cost because the complementary clock will be also generated by the oscillator.

Fig. 3.15 illustrates the impact of the choice of the clock for the correlator. It can be seen that if the correlator is set with the same clock than the comparator($pclk\_correlator\_input$), some data in the correlator are missed because of the comparator delay. On the other hand, if the circuit is triggered with the complementary clock($nclk\_correlator\_input$), the data are the same than those at the input. The incoming bitstream remains therefore correct.

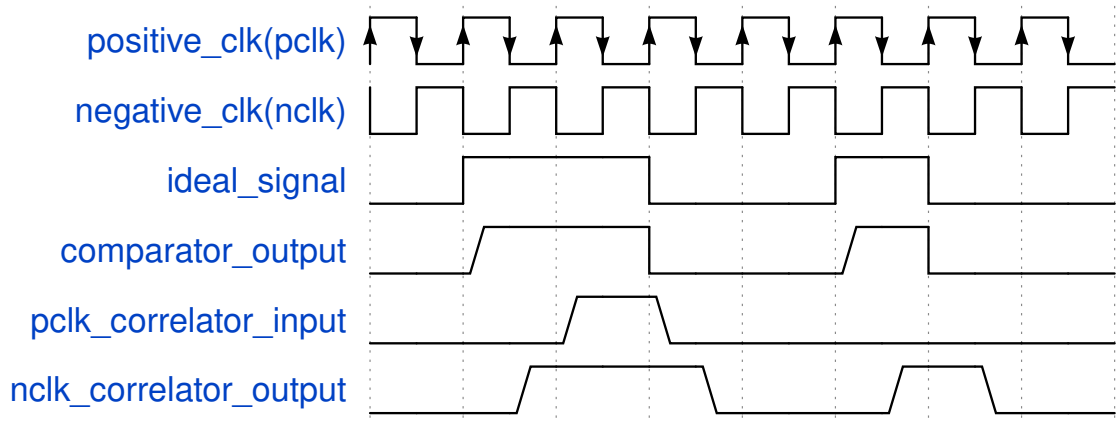



Figure 3.15: Choice of the Correlator Clock.

The synthesis of the circuit is done with Design Compiler. The circuit presents an overall power consumption of 1 nW for the dynamic consumption and 2nW of leakage power consumption. It must be noticed that the leakage represents a higher part in the power consumption than the dynamic power consumption which can happen in low power designs. One reason is the use of high threshold voltage transistors to minimize the dynamic power consumption, these devices have more leakage than the standard devices. Transistors with higher threshold voltage will have more power consumption but less leakage, the best trade off has to be found depending on the use case.

### 3.4.3 Design and implementation

Fig. 3.16 presents the layout of the designed correlator, the dimensions of the core are $45\mu m \times 40\mu m$ without the power rails and $85\mu m \times 80\mu m$ with the power rails. The layout generation is the same as the method presented for the MCU in the previous chapter. The power consumption estimation after the layout is similar to the one estimated during the synthesis.

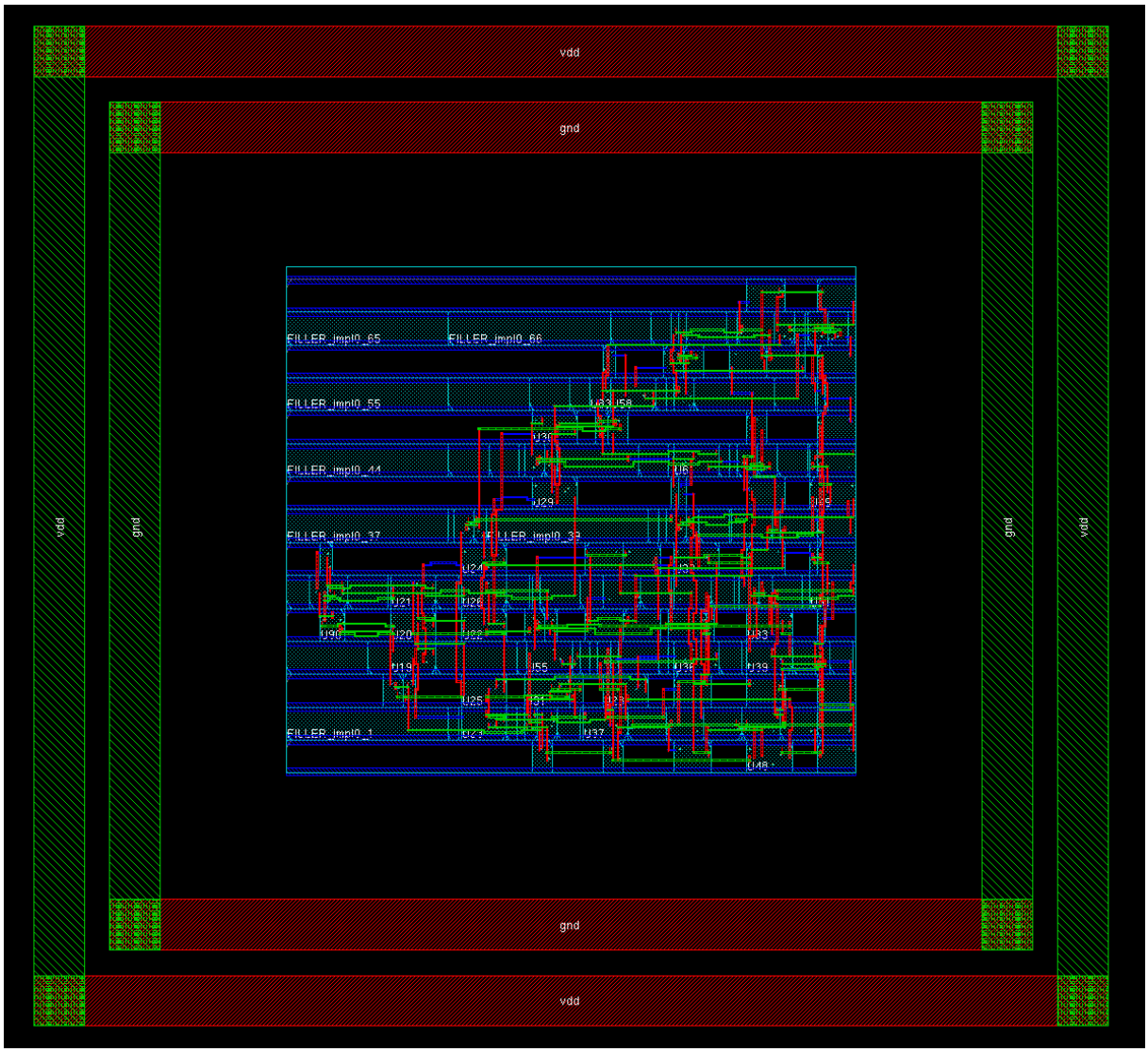



Figure 3.16: Layout of the Correlator.

The next step will be to be able to interface the correlator with the rest of the WuRx. Indeed, due to the fact that two different software are used, it is complicated to simulate the whole layout. The netlist of the correlator is generated in a Verilog file, which is not the way Cadence generates the netlist. A solution has to be found to simulate the entire circuit. However, the interfacing between the two different parts are only logical signals, at low frequency and with no power, so the interfacing can be be presumed with no big issue.

## 3.5 Oscillator

### 3.5.1 Overview

To drive the comparator and the correlator, an oscillator is needed to generate the clock. We target an oversampling of the demodulated signal at twice the maximum data rate, the oscillator frequency is so fixed to 2kHz. Usually for this frequency range, relaxation oscillators are used in WuRx publications. The disadvantage of this topology is that it needs large values of resistance and capacitors to oscillate in this frequency range which will require a large area on the chip. The same remark can be done with LC oscillators, the inductance value would be too large for this frequency. Likewise with ring oscillators, the number of inverters needed to have the correct frequency is too important. WuRx in the state of the art usually use relaxation oscillators because they suit more to this frequency range[70],[71],[72],[73],[74],[75].

### 3.5.2 Oscillator topology

The chosen design is an RS-based oscillator[81] which consists in an RS latch with its outputs looped to the inputs as depicted by Fig. 3.17.

The principle relies on the RS latch truth table shown in Table 3.3. If the circuit is in a defined state with a couple of values $Q$ and $\overline{Q}$, the circuit is looped so that the values of R and S will switch to the other combination, this will change the values of $Q$ and $\overline{Q}$, thus commuting $R$ and $S$ etc... The advantage of this topology is that it provides a clock signal and its complementary, which is required by the comparator topology in our case.

Table 3.3: Truth Table of a RS latch.

| $S$ | $R$ | $Q$ | $\overline{Q}$ |
|---|---|---|---|
| 0 | 0 | 1<br>0 | 0<br>1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

To demonstrate the oscillation frequency of the circuit, we assume that at the initial time $t = 0$, $Q = 0$ and $\overline{Q} = 1$. This means that $P_2$ and $N_1$ are on while $P_1$ and $N_2$ are off.

We can write the equation at $C_2$ node:

$$I_{BIAS} = C_2 \frac{dV_{C_2}}{dt} \tag{3.5}$$

This equation can be written

$$\frac{dV_{C_2}}{dt} = \frac{I_{BIAS}}{C_2} \tag{3.6}$$

$I_{BIAS}$ and $C_2$ are constant values, by integrating the previous equation we obtain :

$$V_{C_2}(t) = \frac{I_{BIAS}}{C_2} t + k \tag{3.7}$$

With k a constant, assuming that the capacitors are discharged at the initial state, we can write $k = 0$.

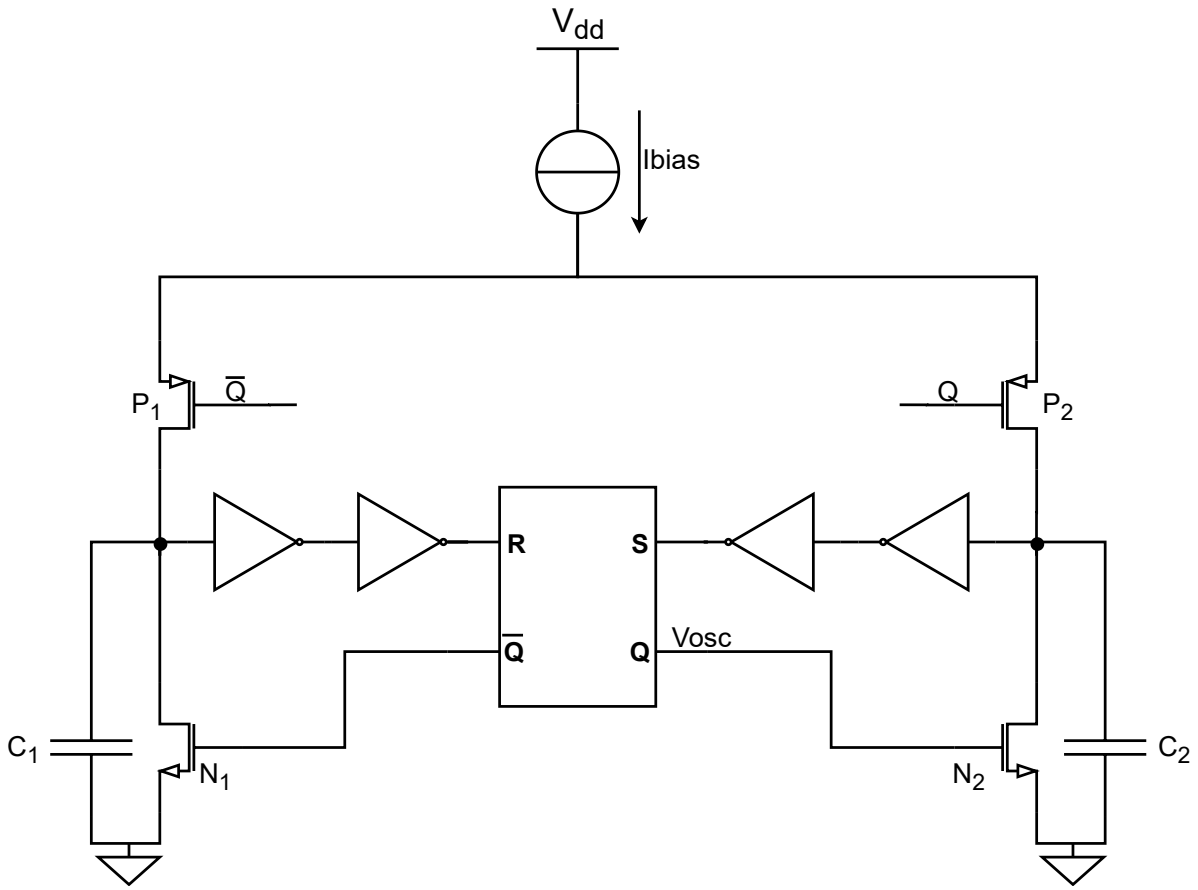



Figure 3.17: RS Oscillator Schematic.

We name $t_1$ the time when the voltage of the capacitor reaches the threshold voltage of the inverters to make the latch switch. We can write:

$$V_{C_2}(t_1) = V_{th_{INV}} = \frac{I_{BIAS}}{C_2} t_1 \tag{3.8}$$

At this moment, the latch will switch, meaning that $Q = 1$, $\overline{Q} = 0$ and so $P_1$ and $N_2$ are on while $P_2$ and $N_1$ are off.

We can write the same equation for $C_1$ as previously, we obtain:

$$V_{C_1}(t) = \frac{I_{BIAS}}{C_1} t \tag{3.9}$$

If we name $t_2$ the time for the voltage to reach the inverters threshold we have again:

$$V_{C_1}(t_2) = V_{th_{INV}} = \frac{I_{BIAS}}{C_1} t_2 \tag{3.10}$$

And then the oscillator goes back to its state at $t = T$. We can define the oscillator period as :

$$T = t_1 + t_2 = \frac{V_{th_{INV}} C_2}{I_{BIAS}} + \frac{V_{th_{INV}} C_1}{I_{BIAS}} \tag{3.11}$$

The duty cycle of the oscillator can be expressed as :

$$\alpha = \frac{t_1}{t_1 + t_2} = \frac{\frac{V_{th_{INV}} C_2}{I_{BIAS}}}{\frac{V_{th_{INV}} C_2}{I_{BIAS}} + \frac{V_{th_{INV}} C_1}{I_{BIAS}}} = \frac{C_1}{C_1 + C_2} \tag{3.12}$$

Because we want a duty cycle of 50% the two capacitors have the same value $C_1$=$C_2$=$C$. We can rewrite the equation of the period:

$$T = \frac{2V_{th_{INV}} C}{I_{BIAS}} = 1/f \tag{3.13}$$

Assuming the inverters symmetrical their threshold voltage is equal to $\frac{V_{DD}}{2}$, we finally obtain the expression of the oscillation frequency:

$$f = \frac{I_{BIAS}}{CV_{DD}} \tag{3.14}$$

To stay at a low power consumption the bias current is initially fixed at 1.5nA which leads for a power supply of 1.2V and an oscillation frequency of 2kHz to a capacitor value of 600fF.

### 3.5.3 Design and implementation

Fig. 3.18 shows the layout of the oscillator, the dimensions of the core are $34\mu m \times 31\mu m$.

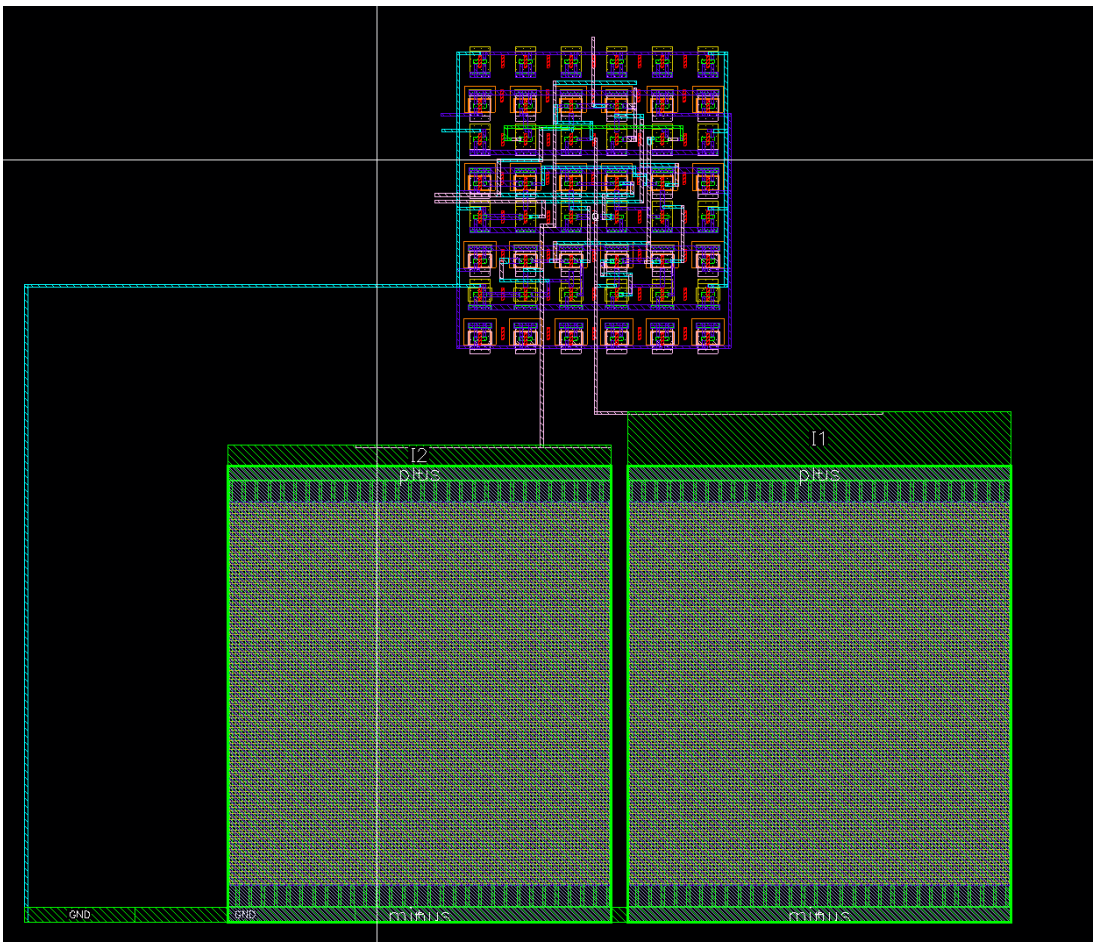



Figure 3.18: Layout of the Oscillator.

Fig. 3.19 shows the two clock signals generated by the oscillator. The circuit delivers two square signals oscillating at 2kHz and correctly out of phase. There is no deformation or delay induced by parasitic contributions of the layout.

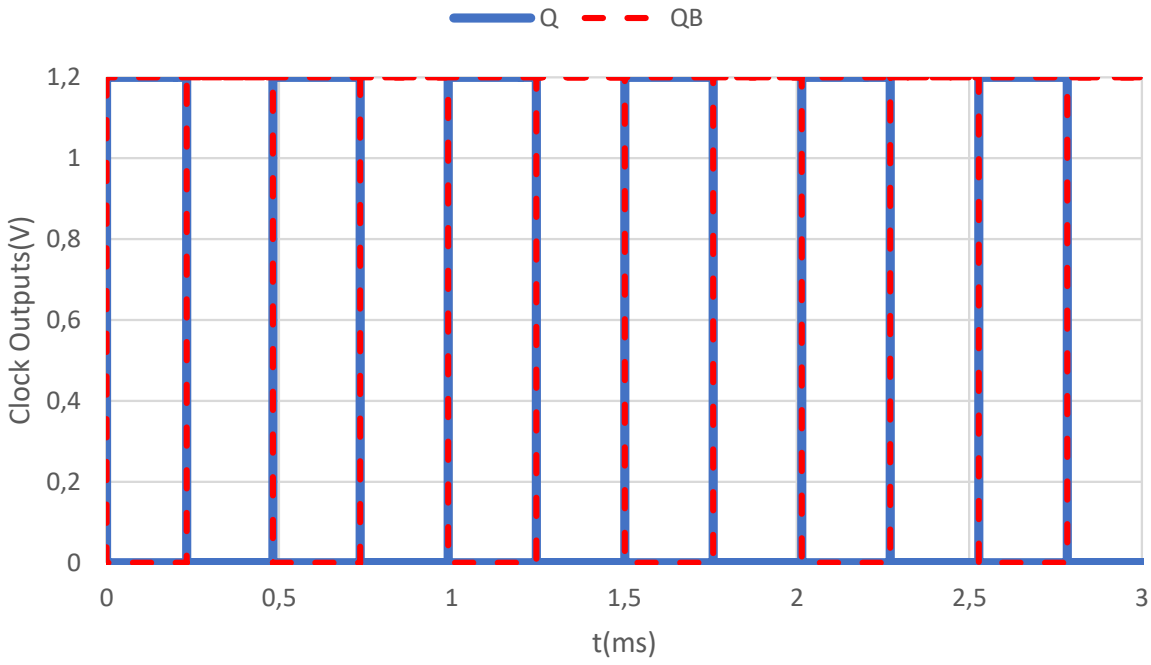



Figure 3.19: Clock Signals of the Oscillator.

An important parameter of free running oscillator is the drift with temperature or voltage supply variations. Indeed, if the variation of the oscillation frequency is too large, this will degrade the performances of the system. To address this issue, the current source steering the oscillator in Fig. 3.17 must be robust to the drift. The next section presents the design of this current source, the study of the oscillator will be addressed at this moment.

## 3.6 Current Source

### 3.6.1 Overview

The oscillator presented in the previous section needs a current source to perform the charge and discharge of the capacitors. To ensure a stabilized operation of the oscillator the temperature drift of the current source is critical. The current source also needs to be robust to supply voltage variations. This part will present the design of a nanoampere current source for the oscillator.

### 3.6.2 Current source topology

The proposed circuit is a resistor-less current source[82] that can deliver current at nanoampere range. The circuit is presented in Fig. 3.20.

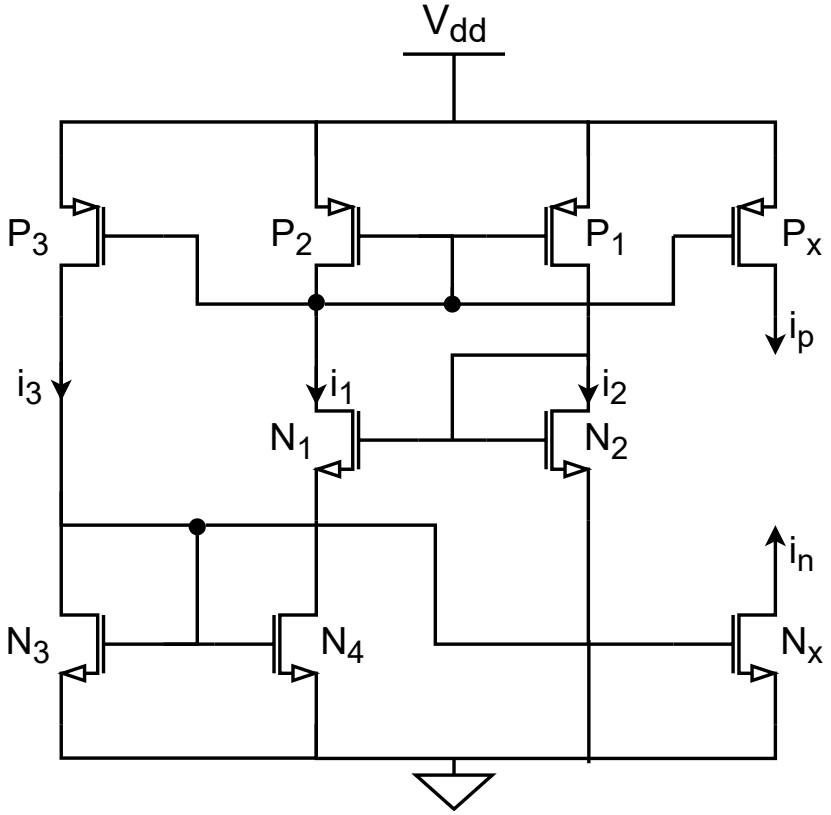



Figure 3.20: Schematic of the Current Source.

For the following demonstration, $U_T$ is the thermal voltage which is proportional to the temperature, $V_S$ is the source voltage of the transistor equal to $-V_{GS}$, $S_{Nx}$, $S_{Px}$ are W/L ratios of the respective transistors, $\beta_{nx}$ is a constant equal to $\mu C_{ox}\frac{W}{L}$ with $\mu$ the charge-carrier effective mobility and $C_{ox}$ the gate oxide capacitance per unit area.

The proposed circuit is only composed of MOS transistors. $P_1$ and $P_2$ forms a current mirror. Assuming $N_1$ and $N_2$ in subthreshold biasing, the drain current can be expressed as:

$$I_D = I_{D0}\frac{W}{L}\exp\left(\frac{-V_S}{U_T}\right) \tag{3.15}$$

Assuming the perfect equality between $i_1$ and $i_2$, we can write

$$\frac{i_1}{i_2} = \frac{S_{N1}}{S_{N2}} \exp\left(\frac{-V_S}{U_T}\right) \tag{3.16}$$

This equation leads to:

$$V_S = U_T \ln\left(\frac{i_2}{i_1}\frac{S_{N1}}{S_{N2}}\right) \tag{3.17}$$

The ratio between $i_1$ and $i_2$ depends on the size ratio between $P_1$ and $P_2$, it can be expressed as:

$$\frac{i_2}{i_1} = \frac{S_{P2}}{S_{P1}} \tag{3.18}$$

Injecting this into Eq. 3.17, the source voltage $V_{SN1}$ can be expressed as:

$$V_{sN1} = U_T ln\left(\frac{S_{N1}S_{P2}}{S_{N2}S_{P1}}\right) = U_T ln(K_1), \tag{3.19}$$

This voltage value does not depend on the current as long as the transistors stay in the subthreshold region. Transistor $N_3$ acts as a resistor and $P_3$ and $N_4$ provide gate voltage. The current $i_1$ is generated by $N_3$ and can be duplicated by the current mirrors formed with $N_x$, $P_x$. The expression of $i_1$ can be given by the following equation:

$M_{N3}$ is in the saturation region, its drain current can be written as:

$$i_3 = \frac{1}{2}\beta_N 3(V_{gN3} - V_{TN})^2 \tag{3.20}$$

As previously, the ratio between $i_3$ and $i_1$ can be described depending on the dimensions of $P_3$ and $P_1$ such as:

$$\frac{i_3}{i_1} = \frac{S_{P3}}{S_{P1}} \tag{3.21}$$

Which leads to:

$$V_{GN3} = \sqrt{\frac{2i_3}{\beta_{N3}}} + V_{TN} \tag{3.22}$$

$N_4$ has the same gate voltage than $N_3$ but its drain voltage is under the saturation voltage, the current $i_1$ through $N_4$ can be expressed as:

$$i_1 = \beta_{N4} V_{SN1}(V_{GN3} - V_{TN} - \frac{1}{2}V_{SN1}) \tag{3.23}$$

Combining with Eq. 3.22, $i_1$ can be expressed as:

$$i_1 = \beta_{N4} V_{SN1}(\sqrt{\frac{2i_3}{\beta_{N3}}} - \frac{1}{2}V_{SN1}) \tag{3.24}$$

Introducing the constant $K_2 = \frac{S_{P3}S_{N4}}{S_{P4}S_{N3}}$, Eq. 3.24 can be written:

$$i_1 = \beta_{N4} V_{SN1}^2[K_2 - \frac{1}{2}\sqrt{K_2(K_2-1)}] \tag{3.25}$$

Finally, writing $K_{eff} = [K_2 - 0.5\sqrt{K_2(K_2-1)}]ln^2(K_1)$, we obtain:

$$i_1 = \beta_{n4} U_T^2 K_{eff} \tag{3.26}$$

The gain factor of the transistor varies with temperature the same way as the mobility. We can write:

$$\beta_{N4} = \beta_{N4_0}(\frac{T_0}{T})^m = \beta_{N4_0}(\frac{U_{T0}}{U_T})^m \tag{3.27}$$

Injecting into Eq. 3.26, the output current can be expressed as:

$$i_1 = K_{eff} \beta_{N40} U_{T0}^2 (\frac{T}{T_0})^{2-m} \tag{3.28}$$

With $\beta_{N40}$ and $U_{T0}$ set at ambient temperature $T_0$ and $m$ is a value between 1.5 and 2.

This resistorless design allows for a easier control of the temperature drift since the modeling of MOS thermal dependence is well known. Besides it allows for a compact implementation as illustrated in the next section.

### 3.6.3 Design and implementation

Fig. 3.21 presents the layout of the current source, the dimensions of the core are $143\mu m \times 52\mu m$.

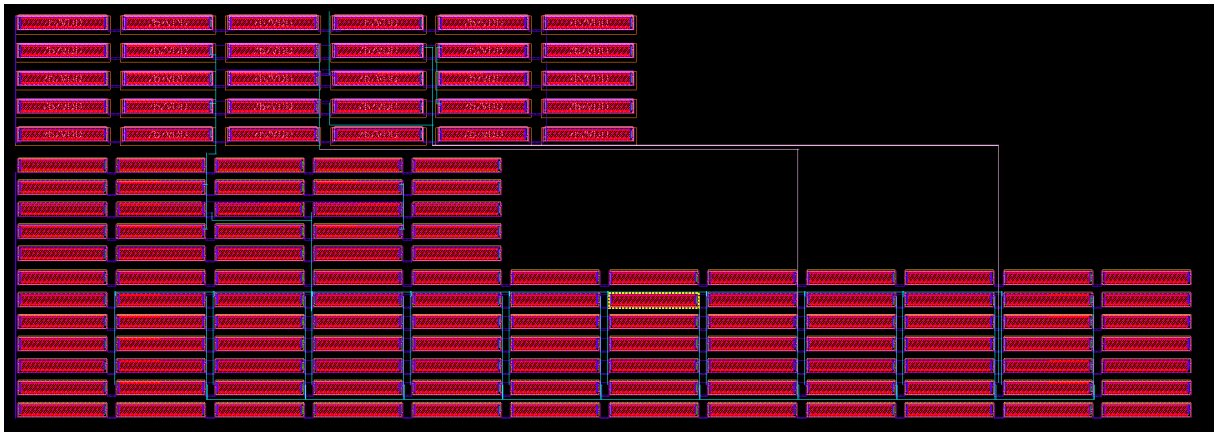


Figure 3.21: Layout of the Current Source.

Fig. 3.22 shows the circuits power consumption variations depending on the temperature from 0°C to 40°C.

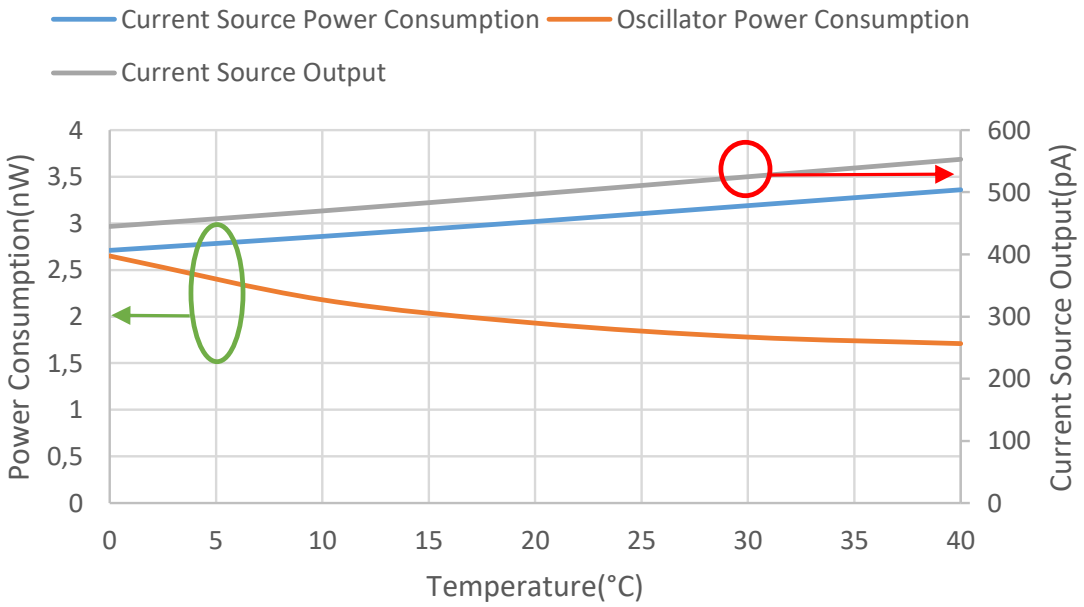



Figure 3.22: Power Consumption of the Current Source with Temperature Variations.

The power consumption of the current source goes from 2.7nW to 3.35nW which represents a variation of 14% and 7% at 27°C. The current delivered by this source varies from 445pA to 553pA which represents a variation of approximately 11% from the value at 27°C. Eq. 3.26 shows that the current depends on the thermodynamic voltage, which depends on the temperature. Assuming that the other parameters are rather constant, it comes that the current increases with the temperature. The power consumption of the oscillator goes from 2.65nW to 1.71nW which represents a variation of 40% and 8%.

Fig. 3.23 presents the variation of the clock frequency over the same range of temperature.

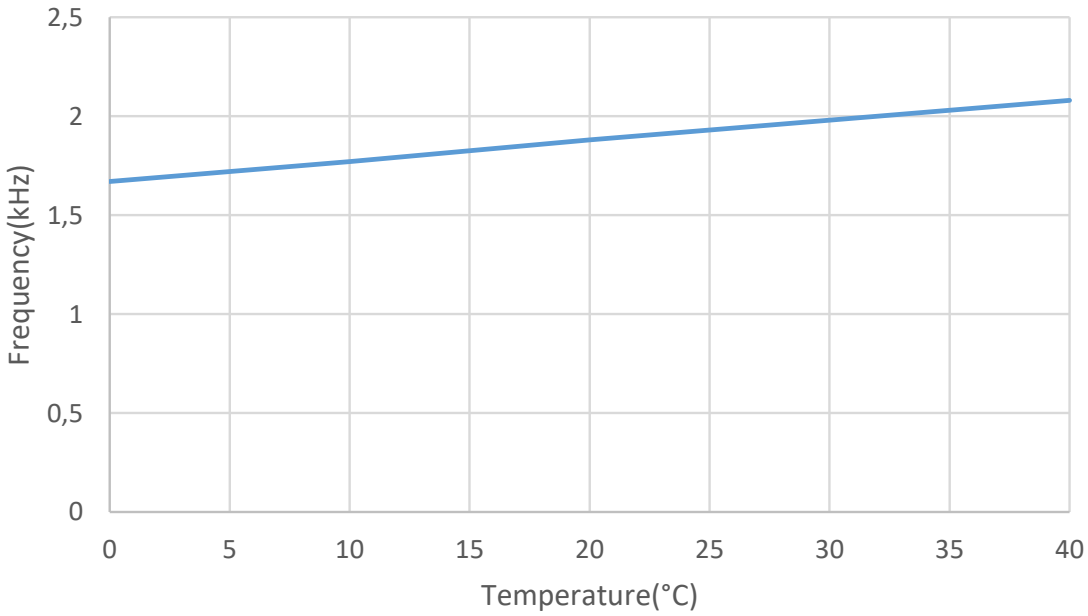



Figure 3.23: Frequency Clock with Temperature Variations.

The frequency varies from 1.67kHz to 2.08kHz which represents a variation of 14.5% and 7% respectively. It can be noticed that the variation of the oscillation frequency follows the variations of the current source output and does not depend on its own power consumption variations. This result is consistent with Eq. 3.14.

Concerning the frequency variation, the oscillation stays in a range under 20% from the central frequency which is the target to keep the communication feasible at the same data rate.

A question can be pointed out that the power consumption of the oscillator does not increase as the oscillation frequency increases. Normally if the frequency increases, there is more switching in the circuit leading to a higher power consumption.

Fig. 3.24 presents the clock falling edge time variations with temperature. The time the oscillator needs to go from its high level to the low level decreases when the temperature increases. This means that the transistor is conducting during a shorter amount of time and so the overall energy consumption is lower.

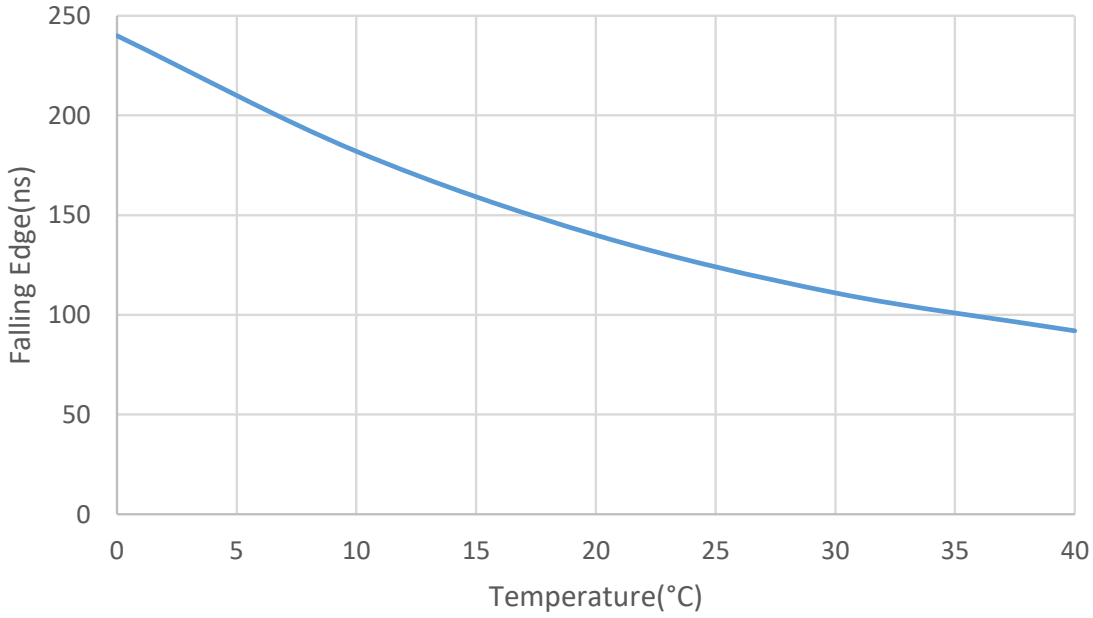



Figure 3.24: Falling Edge of the Oscillator with Temperature Variations.

An other parameter that can be considered is the robustness of the circuit to voltage supply variations. The output current needs to vary as few as possible to ensure the oscillator a stable frequency. Fig. 3.25 presents the variations of the output current of the current source, the current source and the oscillator power consumption with power supply variations from 1V to 1.4V.

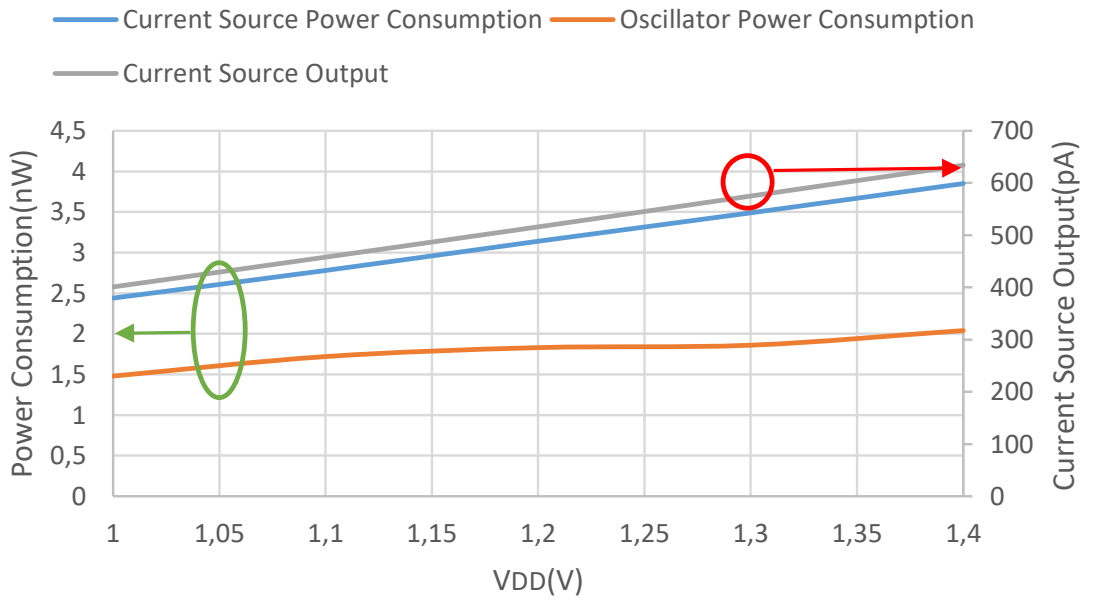



Figure 3.25: Power Consumption of the Current Source with Voltage Supply Variations.

The power consumption of the current source goes from 2.44nW to 3.85nW which makes a variation of 23% from the central value at 1.2V. The output of the current source varies from 401pA to 634pA which is again a variation of 23%, the variation of the output current follows the power consumption. The oscillator power consumption goes from 1.45nW to 2.04nW which makes a variation of 20% and 11% from the nominal value at 1.2V.

Fig. 3.26 presents the clock frequency depending on the voltage supply.

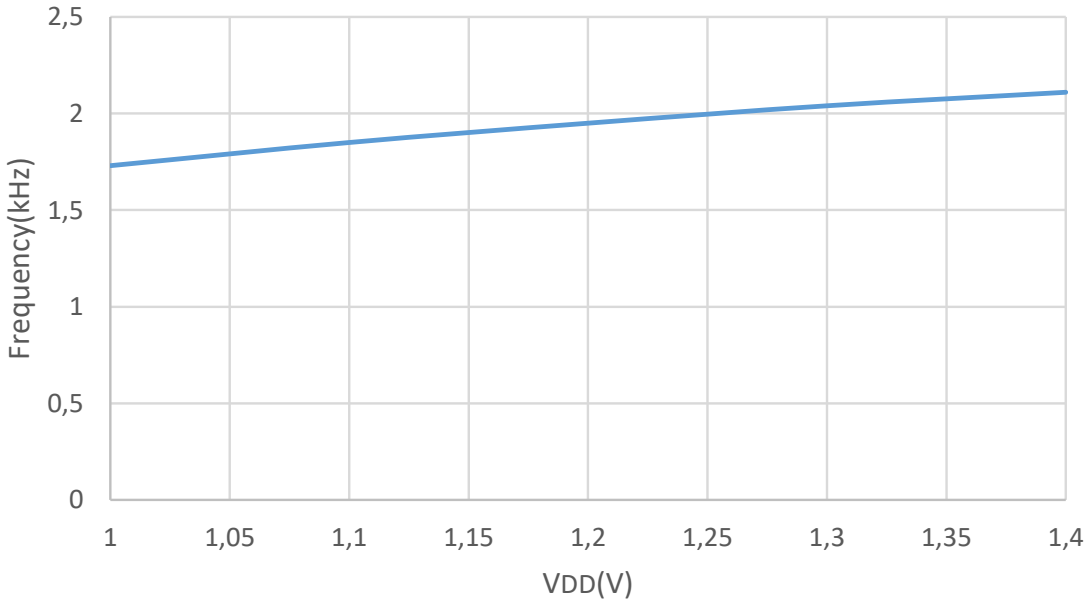



Figure 3.26: Oscillator Frequency with Voltage Supply Variations.

The oscillation frequency goes from 1.73kHz to 2.11kHz. The central frequency is 1.95kHz, there is a variation of 12% and 8% respectively. The oscillator remains steady enough around the central frequency to have a proper communication. This results is consistent with the theory, Eq. 3.14 shows that the oscillation frequency is proportional to the bias current and inversely proportional to the voltage supply. Fig. 3.25 shows that the current source output is proportional to the voltage supply meaning that both variations compensate each other and this allows to keep the oscillation frequency rather constant. According to its datasheet the E-Peas solar harvester has an output voltage variation of few percents. The voltage supply variation can be assumed with no impact over the oscillator performances.

In brief, the combination of the current source and the oscillator can be considered robust enough to temperature and voltage supply variations.

## 3.7 Demodulation

Fig. 3.27 presents a schematic view of the demodulation part that is simulated in post layout simulation.

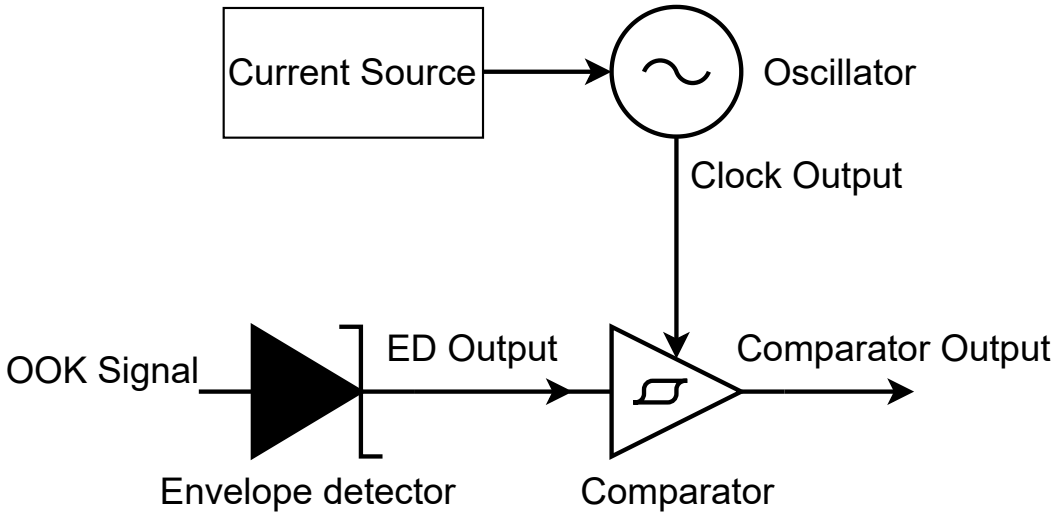



Figure 3.27: Schematic of the Simulated Circuit in PLS.

Fig. 3.28 presents the layout of the demodulation part of the WuRx. The dimensions without the pads are $242\mu m \times 127\mu m$.

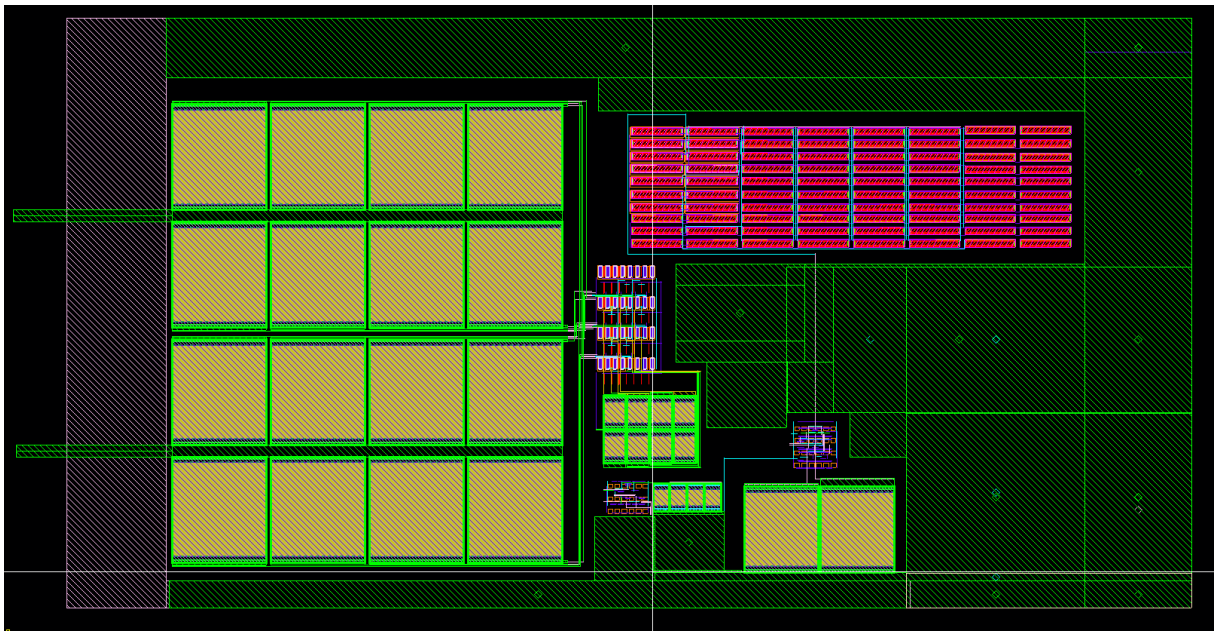


Figure 3.28: Layout of the Demodulation Block.

Fig. 3.29 presents the PLS results of the different blocks. The input signal is an OOK modulated signal with a data rate of 1kbs. The observed signals are the following, from the top to the bottom:

- The OOK signal entering the circuit,
- The signal at the output of the envelope detector,
- The clock signal set at 2kHz,
- The output of the comparator.

The OOK signal is generated like a ”random” signal, meaning that there is no pattern to ensure the circuit is not working in a particular case. Here the input presents the frame 1011001010. The envelope detector follows correctly the input signal, the falling edge is almost immediate so there is no risk of interpreting a one instead of a zero. The generated clock oscillates correctly at 2kHz. The comparators does not miss any information or does not inverse two values. The input signal is recovered at the output with the oversampling.

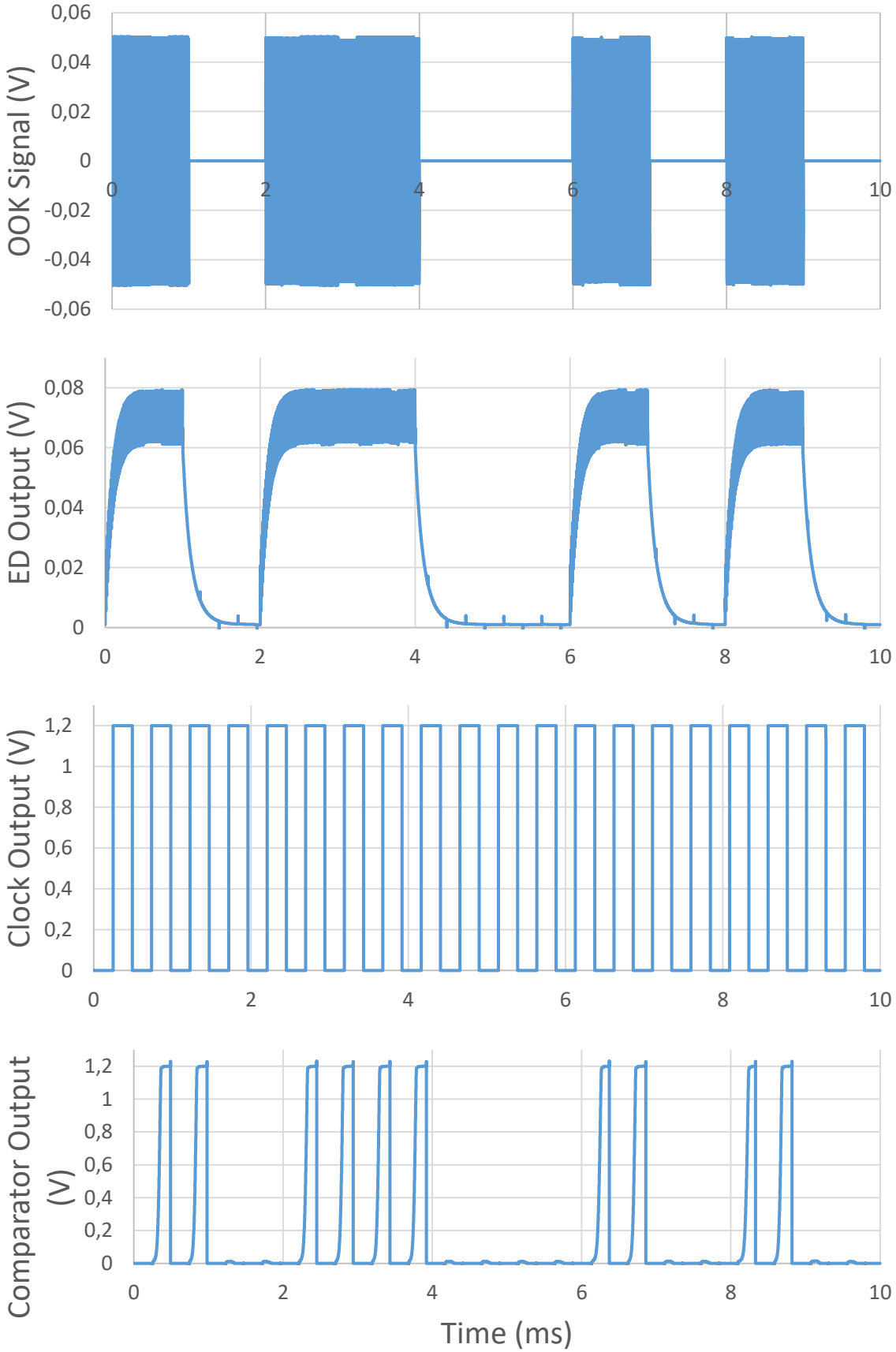



Figure 3.29: Simulation of the Demodulation.

It is important to remind that the main target is to reduce the power consumption as low as possible for this circuit. Fig. 3.30 presents the power consumption of each stage, these results are averaged over a high number of cycles for more accuracy. It blends the power consumption of the demodulation part in PLS and the correlator estimation after routing.

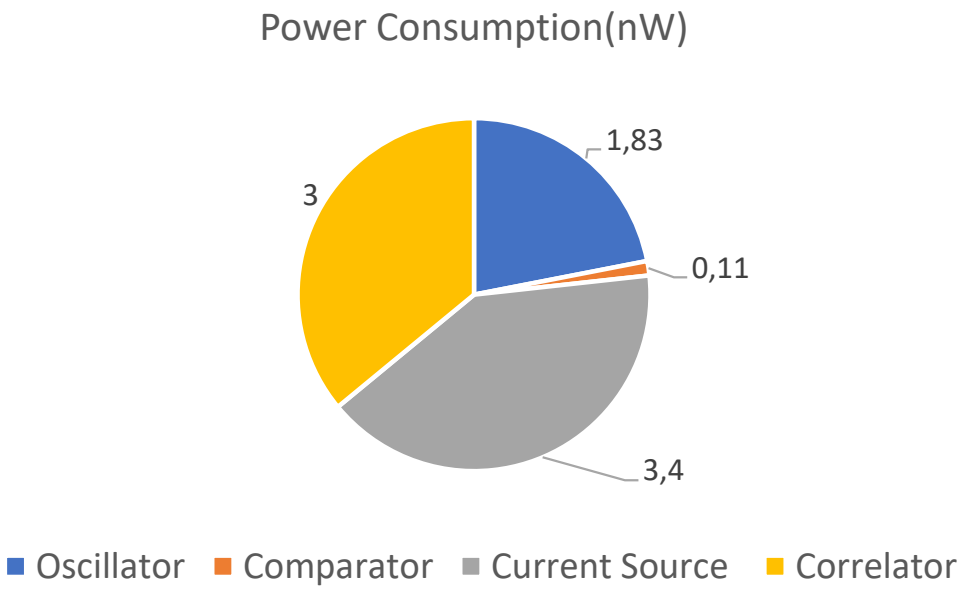



Figure 3.30: Power Consumption of the Circuit.

The circuit presents an overall power consumption of 8.34nW. The limiting factor is the current source which represents 40.8% of the consumption. Hence a reduction of the power consumption would be trade off with the temperature robustness. The second most consuming function is the correlator. As it was presented in the corresponding section, most of this power is lost in the leakage current of the high threshold voltage transistor used for this design. Other devices available in the technology such as low leakage transistors have been tested. It resulted in a larger dynamic power consumption.

An other solution to reduce the power consumption is simply to reduce the voltage supply. Concerning the demodulation part, this method works correctly, only an adjustment needs to be done to recover the correct oscillation frequency. The uncertainty is on the correlator, the model is given to operate at 1.2V. It can be assumed that it would work with a lower power supply but the question is to know the minimum level requested to enable the transistors switch. It also important to note that a supply voltage below 1.2V is not compatible with standard value provided by power cells.

The previous section showed the robustness of the oscillator with respect to the temperature variations. Fig. 3.31 reports power consumption of the whole demodulation block with temperature variations.

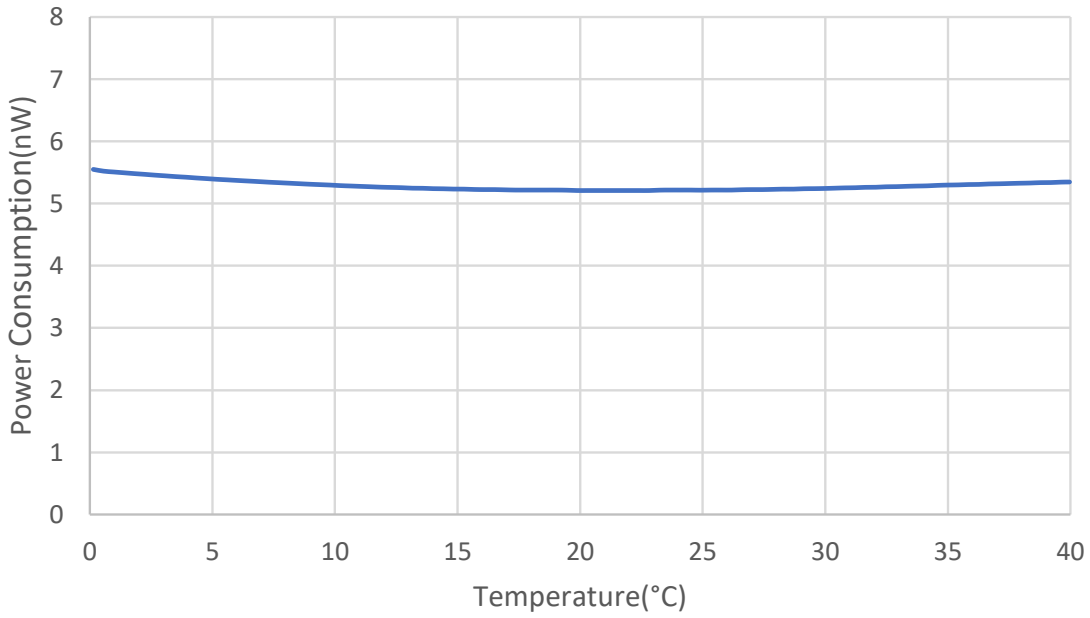



Figure 3.31: Power Consumption Variations of the Demodulation Block.

The power consumption has a nominal value of 5.2nW at 25°C, it does not exceed 5.5nW over the entire temperature range. The variation is smaller than with the current source alone because some adjustments were done to compensate the parasitic effects generated by the layout.

Table 3.4: Comparison with State-of-the-Art.

| | [70] | [71] | [72] | [73] | [74] | [75] | This Work* | | |
|---|---|---|---|---|---|---|---|---|---|
| Carrier Frequency (GHz) | 9 | 0.4 | 0.4 | 0.109 | 0.434 | 0.113 | 0.4 | 0.9 | 2.4 |
| Supply Voltage (V) | 0.4 | 0.4 | 0.4 | 0.4 | 0.3 | 0.4 | 1.2 | 1.2 | 1.2 |
| Oscillator | Relax. osc. | Relax. osc. | Relax. osc. | Relax. Osc. | - | Relax. Osc. | Relax. Osc. | Relax. Osc. | Relax. Osc. |
| Passive Gain (dB) | 18.5 | 18.5 | 25 | 30.6 | - | 26.6 | 29 | 27 | 24 |
| Data Rate (kbps) | 0.033 | 0.3 | 0.25 | 0.033 | 0.25 | 0.3 | 1 | 1 | 1 |
| Energy/bit (pJ/bit) | 670 | 15 | 25.6 | 183 | 27.84 | 15 | 8.34 | 8.34 | 8.34 |
| Sensitivity (dBm) | -69.5 | -63.8 | -75 | -80.5 | -75.8 | -69 | -55 | -53 | -50 |
| Power Consumption (nW) | 22.3 | 4.5 | 6.4 | 6.1 | 6.96 | 4.5 | 8.34 | 8.34 | 8.34 |
| Technology | 65/180nm | 180nm | 65nm | 180nm | 65nm | 180nm | 65nm CMOS | 65nm CMOS | 65nm CMOS |

(*) PLS Results

Table. 3.4 proposes a comparison with the state of the art. The proposed WuRx is the most efficient solution with an energy per bit of only 8.34pJ/bit. The papers reported here achieve an ultra low power consumption, typically between 4.5nW to 7nW, thanks to a reduced supply voltage 400mV. This unconventional voltage requires an extra power consumption to be generated from the nominal supply -i.e. 1.2V in 65nm and 1.8V in

180nm. In the proposed design, the nominal voltage is 1.2V and the power consumption remains below 9nW for a data rate of 1kbps. The sensitivity of the SoA ranges from -70 to -85dBm which is almost 20dB better than the proposed WuRx. The lower sensitivity is due to the limited number of rectification stages compared to the other works. A system study has demonstrated that a sensitivity ranging from -50 to -60dBm allows for few meters of wake up coverage for indoor applications. To address this specification the number of rectification stages is limited to eight in the envelope detector. The papers of the state of the art cascade a lot of rectification stages, up to 22, which improves the sensitivity. This choice really depends on the scenario of application.

## 3.8 Conclusion

This chapter has presented the design of a low-power WuRx for a wireless sensor node. It includes:

- A cross coupled envelope detector and its matching network for 400MHz, 900MHz and 2.4GHz. The circuit achieves a sensitivity of -55dBm, -52dBm and -50dBm at these frequencies.
- A dynamic comparator. The comparator achieves an input sensitivity of 45mV.
- A 32-bit correlator, the circuit operates at 2kHz and consumes 3nW.
- A 2kHz oscillator and its nanoampere current source, the two circuits together present a power consumption of 5.23nW.

The proposed system implemented in 65nm CMOS technology is compatible with 3 different ISM Bands (400MHz, 900MHz and 2400MHz). The PLS demonstrate a data rate of 1kbps for an entire power consumption below 10nW. The circuit is robust to temperature (0 to 40°C range) and voltage supply (1 to 1.4V range) variations.

The proposed WuRx presents good performances compared with the state-of-the-art. Based on post layout simulations, the system exhibits the lowest energy/bit reported so far in the literature to our knowledge. The next step is the manufacturing of the chip to make the comparison with measurement results.

# CHAPTER 4

# FULL SYSTEM STUDY

## 4.1 Introduction

The previous chapters presented the WuRx and the MCU designed during this thesis to improve the original autonomous wireless sensor node(WSN#1) developed with COTS devices by Dr. J. Nicot. In this chapter, the modifications that are done concerning the other peripherals are presented and discussed. At last, a comparison with the previous system is done through different scenarios of operation.

## 4.2 Radio Transceiver and Sensor

In order to make the new version of the wireless senor node (WSN#2) compatible with the 2.4GHz band, the radio module has been changed. It is now a BlueNRG from STMicroelectronics, originally the SPIRIT1 in WSN#1. The general features of each radio are reported in Table. 4.1.

Table 4.1: Comparison of the Radio Transceivers.

| | BlueNRG | SPIRIT1 |
|---|---|---|
| Voltage Supply(V) | 1.7-3.6 | 1.8-3.6 |
| Freq(MHz) | 2400 | 150-956 |
| Standby Current(nA) | 500 | 600 |
| TX Current(mA) | 6.5 @ -8dBm | 7.45 @ -8dBm |

The two devices present similar performances in terms of power consumption. In details, the BlueNRG exhibits a reduction of 15% of standby current whereas the SPIRIT1 needs 15% less current in transmission mode.

Concerning the sensor, the Bosch BME680 is selected instead of the BME280. This devices allows to extend the measurement set to pressure, humidity, temperature and gas with the same power consumption. The performance in comparison with the former sensor are the same, so the global energy consumption should not change with the use of this sensor.

## 4.3 Energy Harvester

The first chapter showed that the energy harvesting module could present a limitation to the performances of the system mainly due to a limited efficiency at lower power levels. A new circuit is proposed and the results are presented in this section.

Table. 4.2 gives examples of typical light exposure depending on the external conditions. This gives an overview of the functioning conditions of the circuits that are used.

Table 4.2: Light Range Example.

| Light Condition | Typical Lux |
|---|---|
| Summer Sunshine | 50000 |
| Ambient Daylight | 10000 to 25000 |
| Overcast Daylight | 1000 to 5000 |
| Well-lit Office | 500 |
| Sunset & Sunrise | 400 |
| Family Living Room | 120 |
| Lifts | 100 |
| Street Lightning | 15 |
| Moonlight (Full Moon) | 1 |
| Night (No Moon) | <0.01 |

Table. 4.3 presents the performance comparison between the E-Peas and the Texas Instrument circuits. The two circuits can handle the same input voltage range, the Texas Instrument circuit can provide a higher output voltage and current. It suits more for higher power applications. The main advantage of the E-Peas circuit is the cold-start voltage which is five times lower, so the circuit is able to harvest lower power levels which is better suited for energy harvesting.

Table 4.3: Performance Comparison for Energy Harvesters.

| | E-Peas | Texas Instrument |
|---|---|---|
| Input Voltage(V) | 0.05-5 | 0.1-5.1 |
| Cold-Start Power(µW) | 3 | 15 |
| Storage Unit Voltage(V) | 0-4.5 | 0-5.5 |
| Output Voltage(V) | 1.2-3.3 | 2-5.5 |
| Maximum Output Current(mA) | 80 | 110 |

Fig. 4.1 shows the PCB of the circuit for solar energy harvesting. The circuit uses a $4 \times 3.2$cm solar cell and loads a supercapacitor. The measurements are performed for a light exposure from 500 to 10000 lux to cover all the possible scenarios.

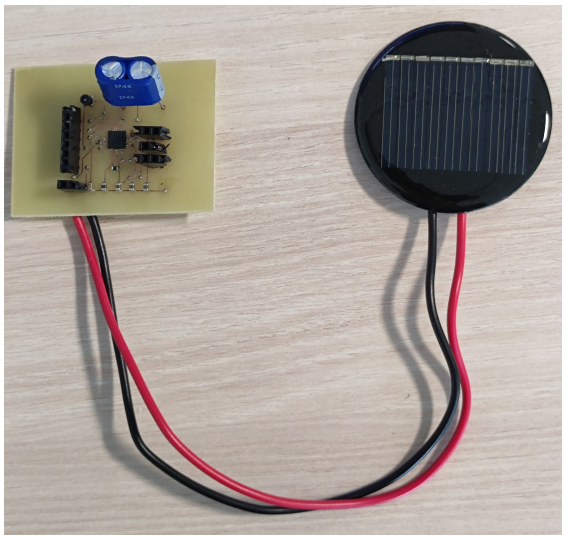


Figure 4.1: PCB of the Solar Harvester.

Fig. 4.2 presents the charge of a 470mF capacitor at 10000lx. The full charge time is around 15 minutes. The LDO outputs of the circuit are activated when the capacitor charge reaches a voltage $V_{chrdy}$. Here, the outputs of the circuit are available when the capacity is charged at 2.3V over the maximum voltage($V_{ovch}$) which is 2.7V in the actual configuration.

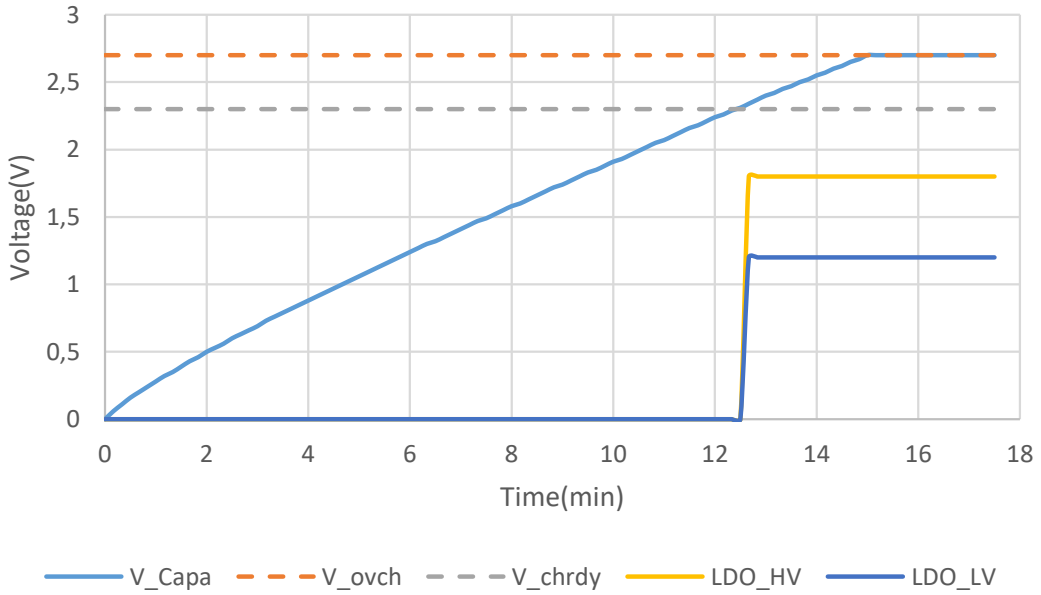



Figure 4.2: Charge of the Supercapacitor at 10000 Lux.

Fig. 4.3 shows the capacity charge time depending on the luminosity. The luminosity range goes from daylight to an office exposure which can cover most of the application scenarios.

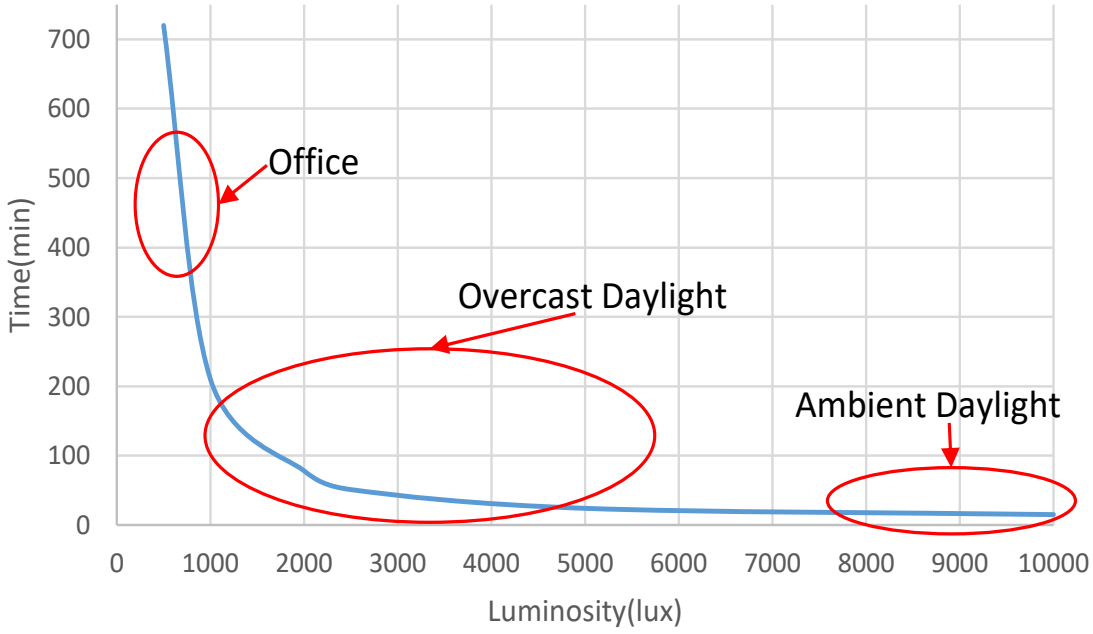



Figure 4.3: Charge Time Depending on the Luminosity.

Fig. 4.4 shows the discharge of the capacity for an output current of 1mA at different light intensities. The measurements are performed until the capacity voltage reaches 2.2V which is the voltage for which the outputs of the circuit are switched off($V\_ovdis$). It can be seen that the circuit can provide this current during 5 to 30 minutes depending on the light intensity. Of course, the functioning time of the MCU with its peripherals during an operation is much lower than this range as we will see in the next sections.

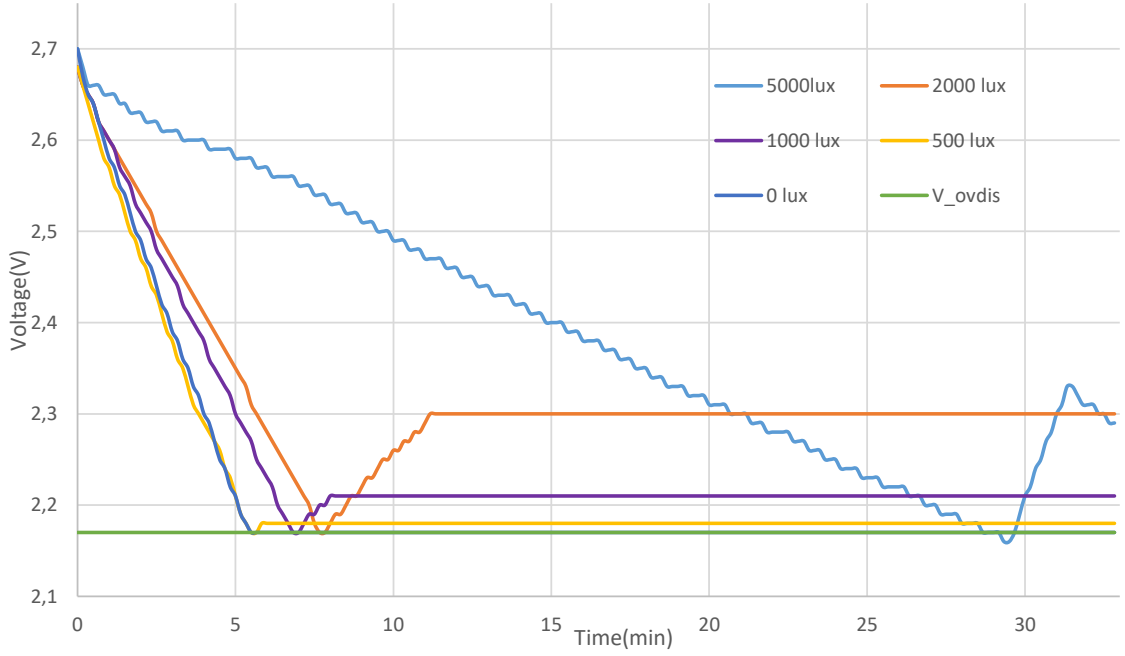



Figure 4.4: Capacity Discharge at 1mA Output Current.

When fully charged, the 470mF capacitor voltage is 2.7V. The amount of stored energy in a capacitor is defined by the following equation:

$$E = \frac{1}{2}CV^2 \tag{4.1}$$

So the amount of energy stored is 1.7J. Considering the power consumption of the WuRx of 8.34nW, the amount of time needed to discharge the capacity only with this circuit would be $2.10^8$s which represents approximately six years. The circuit can be considered without impact on the node performances because the leakage of the capacitor would be higher than this. And so the contribution of the WuRx can be removed from the consumption considerations.

## 4.4 Full System Autonomy Estimation

This section presents the autonomy estimation for the entire node, a comparison is performed with the previous node designed with COTS (WSN#1). This allows to estimate the possible gains with the IC version (WSN#2). The simulation is performed based on various scenarios of operation.

The simulation is done assuming that the storage capacitor is fully charged at the beginning of the operation. The desired scenario is selected at the beginning of the simulation. Then, the amount of needed energy is calculated for each operation involved in the scenario. The amount of energy left in the capacitor is computed, if there is enough energy left for an other routine, the simulator continues, otherwise the autonomy is computed. The autonomy of the node is calculated for different interval times between consecutive measurements. It can be noticed that the contribution of the energy harvester can be considered by adding energy to the capacitor at each routine.

Fig. 4.5 presents the flow of the simulator to compute the autonomy of the node.

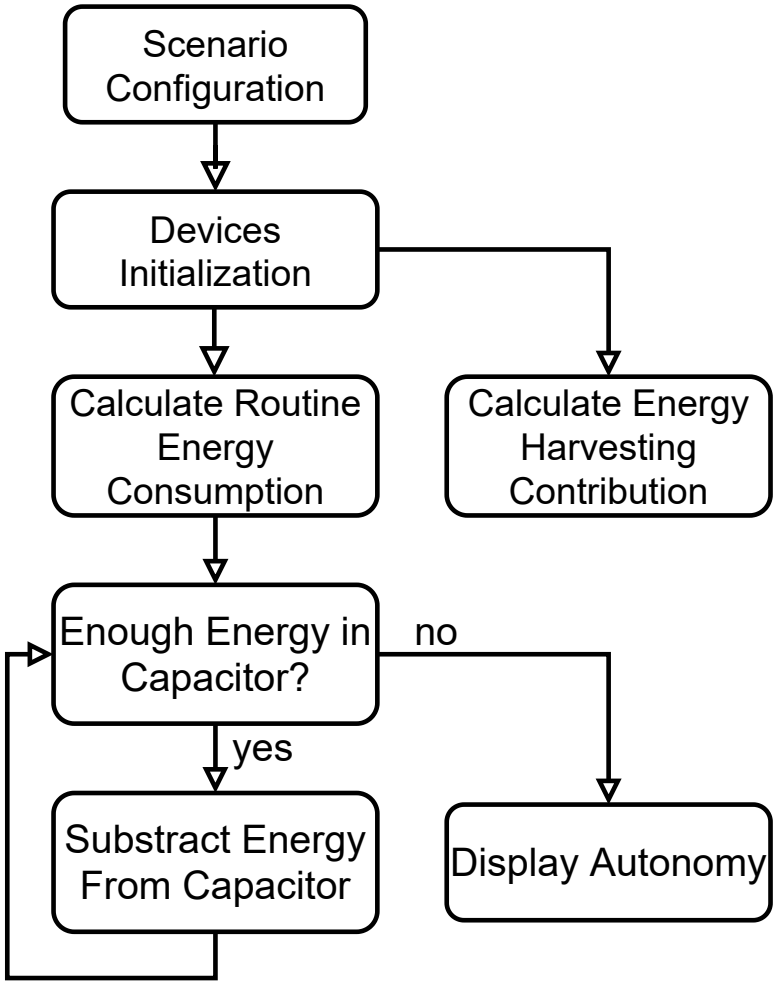



Figure 4.5: Flow of the Simulator.

Fig. 4.6 presents the comparison between the simulator and measurements for WSN#1. We observe the simulator provide a very good estimation of the autonomy whatever the measurement interval. The simulator can therefore be used confidently to estimate the autonomy of the future node.

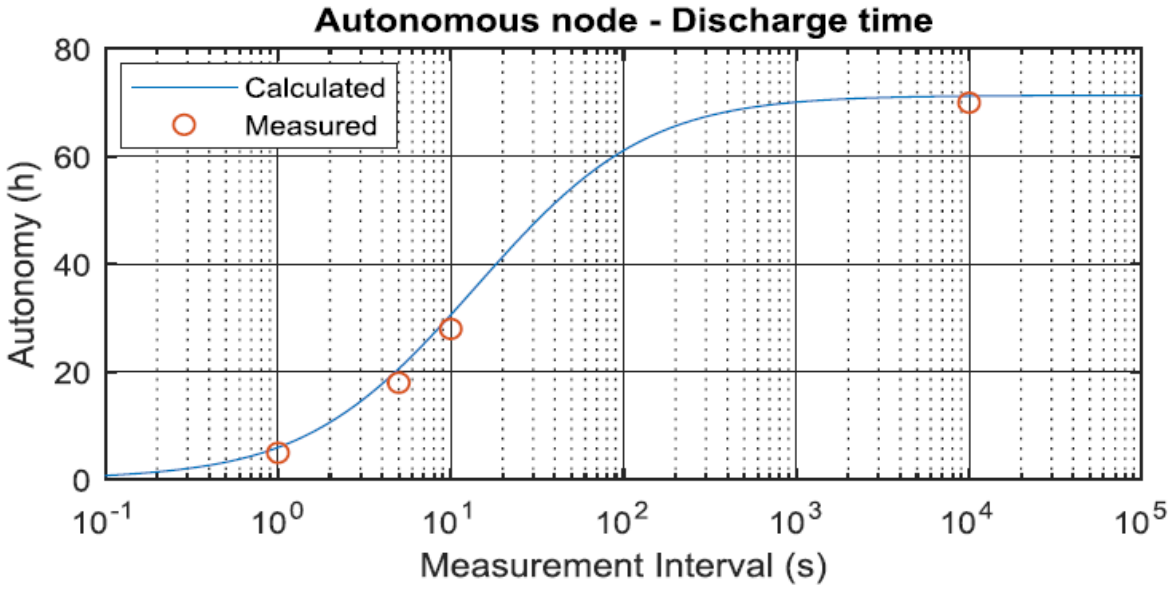



Figure 4.6: Comparison of the Simulator with Measurements[83].

In this section, the supercapacitor is considered loaded at 3.8V to be consistent with the previous thesis. The different scenarios will be reviewed and the improvements in terms of autonomy and minimal input power will be presented. The impact of the energy harvesting circuit will also be considered.

### 4.4.1 RX/TX Mode

The first scenario is called the RX/TX Mode. In this case, after the reception of a request, the node performs the measurement and broadcasts the result through the radio(blueNRG). In this application, all the peripherals of the node are involved.

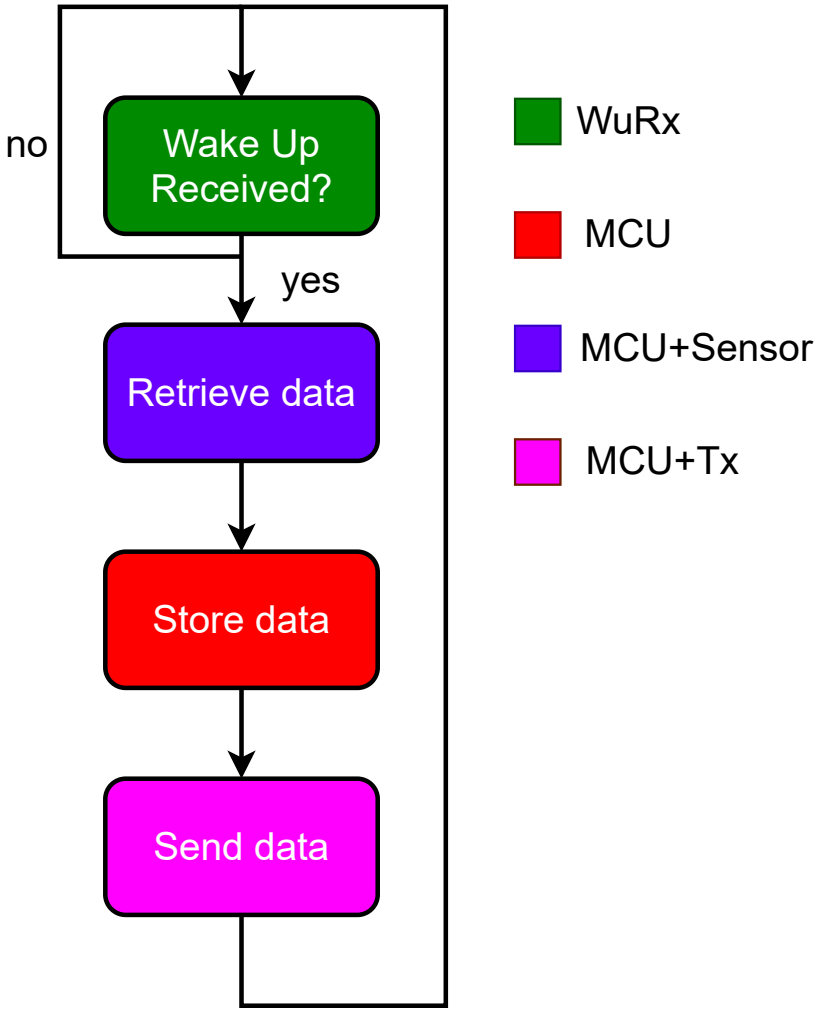



Figure 4.7: RX/TX Mode Illustration.

Fig. 4.8 presents the input power required to supply the node as a function of the measurement intervals with the node functioning in RX/TX Mode. On average, WSN#2 allows to reduce the required RF input power by 20% (-1dB). This improvement comes from the energy saved by the WuRx and the MCU. When the measurement interval exceeds 1000s, the requirement is the same for both nodes because the activity of the peripherals dominates the overall power consumption.

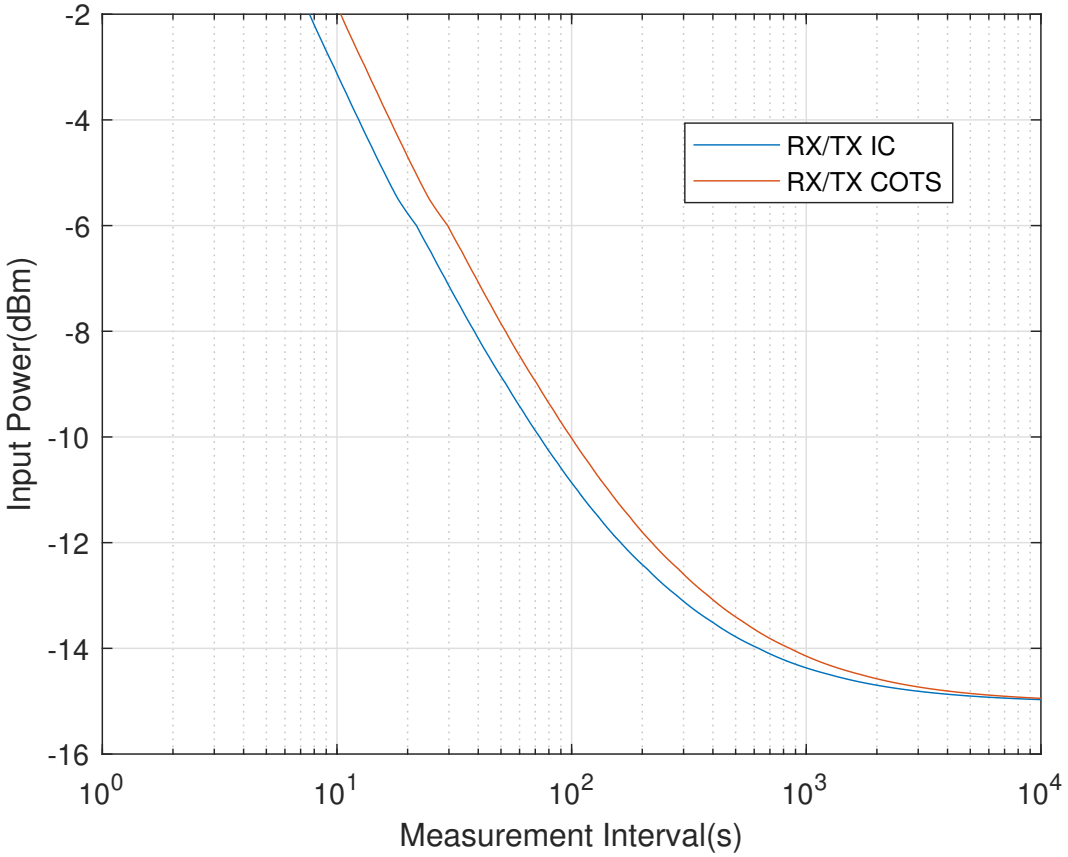



Figure 4.8: Input Power Requirements in RX/TX Mode.

Fig. 4.9 shows the autonomy of the COTS and IC nodes in RX/TX mode depending on the time interval between the measurements. WSN#2 achieves a higher autonomy when the time between the measurements decreases. The autonomy improvement represents 40% for a measurement interval of 1s, 29% at 10s and 20% at 20s. The two curves meet for longer measurement intervals and stabilise around 53 hours of autonomy.

It can be noted that as measurement intervals increase to be longer than one hour($3.610^3$s), the static power consumption of the system, including the storage element's leakage current, overtakes that of the power used during normal operations, and therefore the autonomy varies little past this measurement interval. Using a larger supercapacitor, or higher maximum storage element voltages, would increase the autonomy of the node. However, larger storage elements would come at a cost of a longer cold start times.

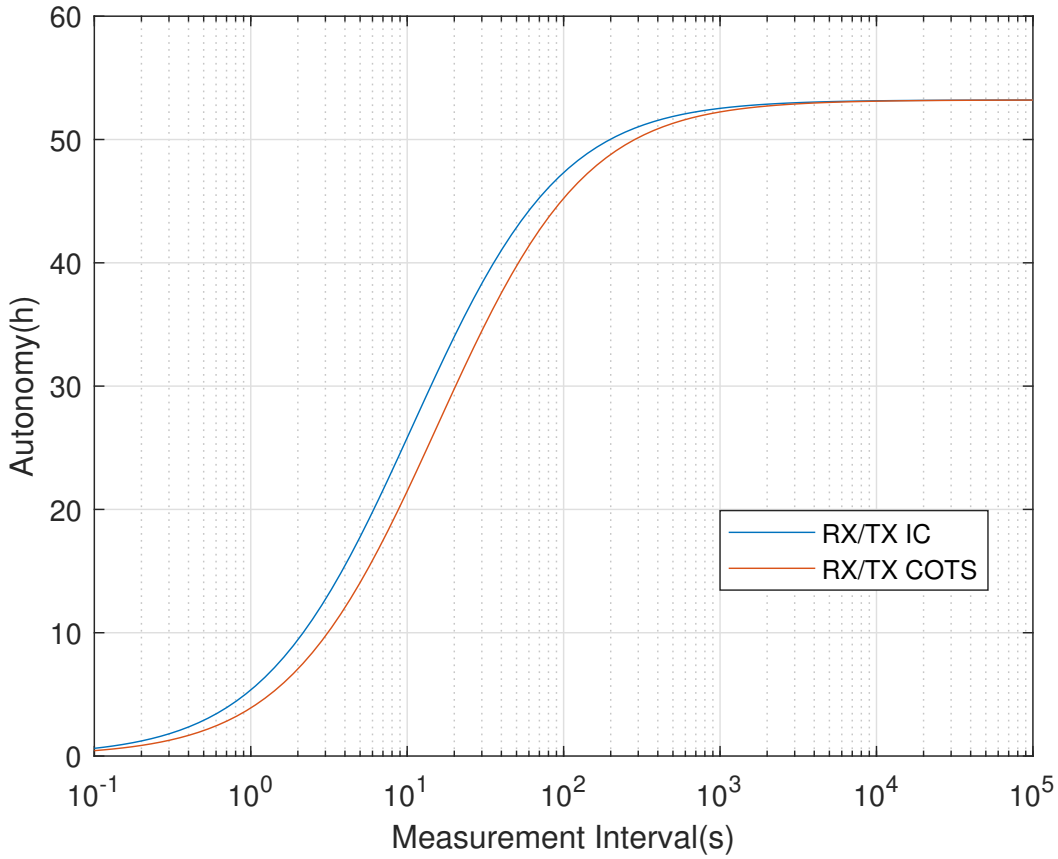



Figure 4.9: Autonomy of the Node in RX/TX Mode.

### 4.4.2 RX Only Mode

The second possible functioning mode is the RX Only configuration. As depicted in Fig. 4.10, when a request occurs, the node only performs the measurement and stores the value. The main radio is not used in this scenario.

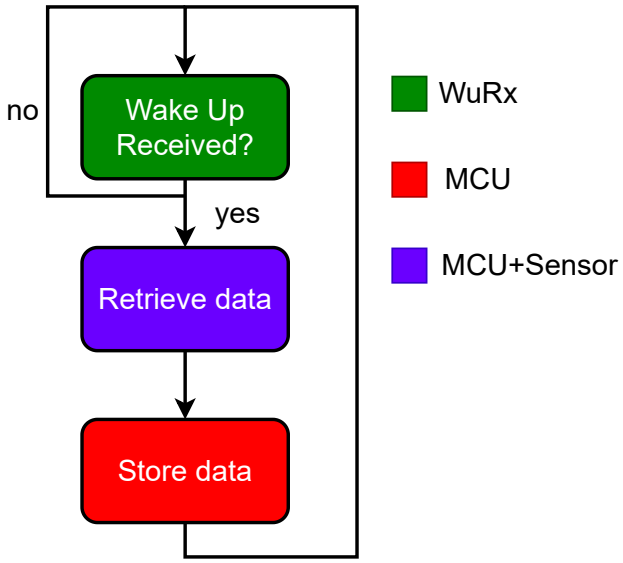



Figure 4.10: Rx Only Mode Illustration.

Fig. 4.11 shows the input power requirements for the two nodes in RX Only Mode. In RX Only Mode, the IC node needs 37% (2dB) less power than the COTS node for measurement interval under 10s, there is a difference of 17% (0.8dB) for an interval of 100s, then the power requirements are the same. The difference between the two nodes is 1dB better in this configuration than in RX/TX Mode due to the absence of the radio transceiver. The power requirement is therefore lighter.

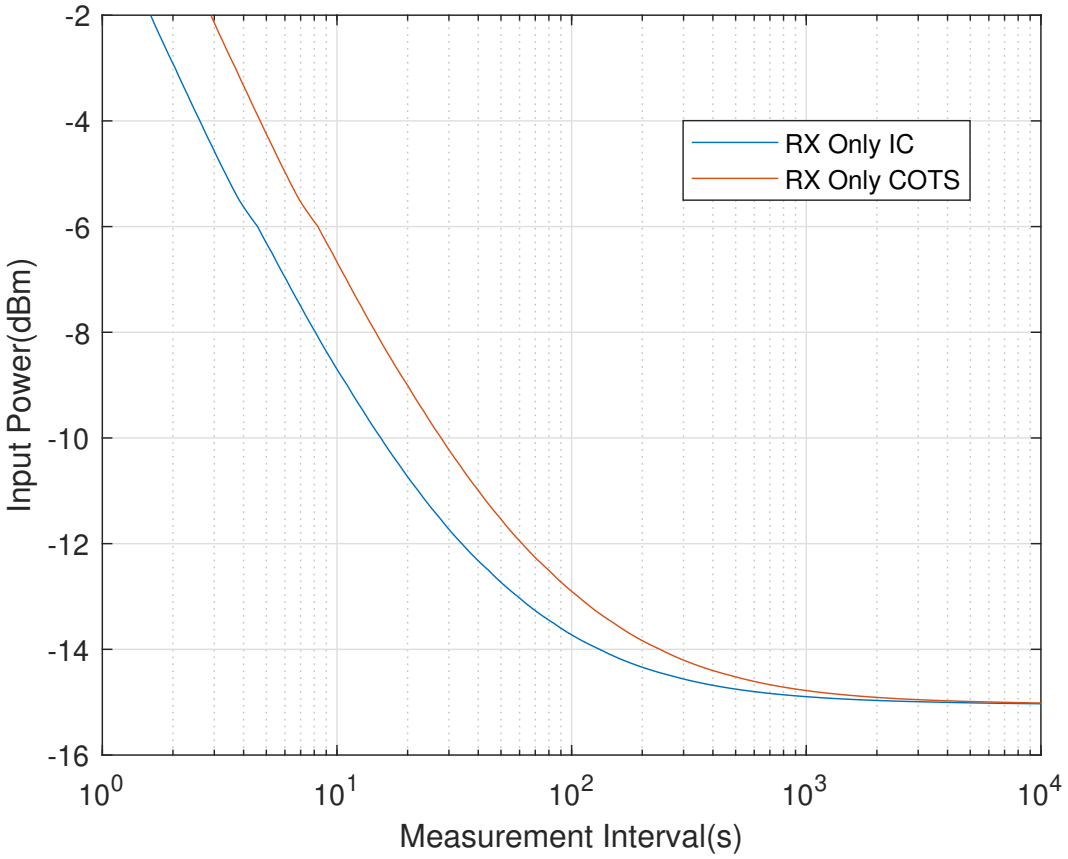



Figure 4.11: Input Power Requirements in RX Only Mode.

Fig. 4.12 presents the autonomy of the COTS and IC node in RX Only mode. The autonomy for a measurement interval of 1, 5 and 10s is 30, 46 and 49 hours respectively with the IC version of the node. The COTS version presents autonomy of 12, 30 and 38 hours for the same measurement intervals. This represents an improvement of 150%, 50% and 29%.

This results first demonstrates that the radio transceiver has an important impact on the autonomy. Here the gap between the two estimations is wider for lower measurement intervals, it shows that the radio contribution narrows the difference between the nodes. This results leads to the idea that it would be interesting to limit the use of the main radio to save energy, especially when the measurements are very close to each other. This consideration opens to an other scenario of operation namely "Burst Mode" presented in the next section.

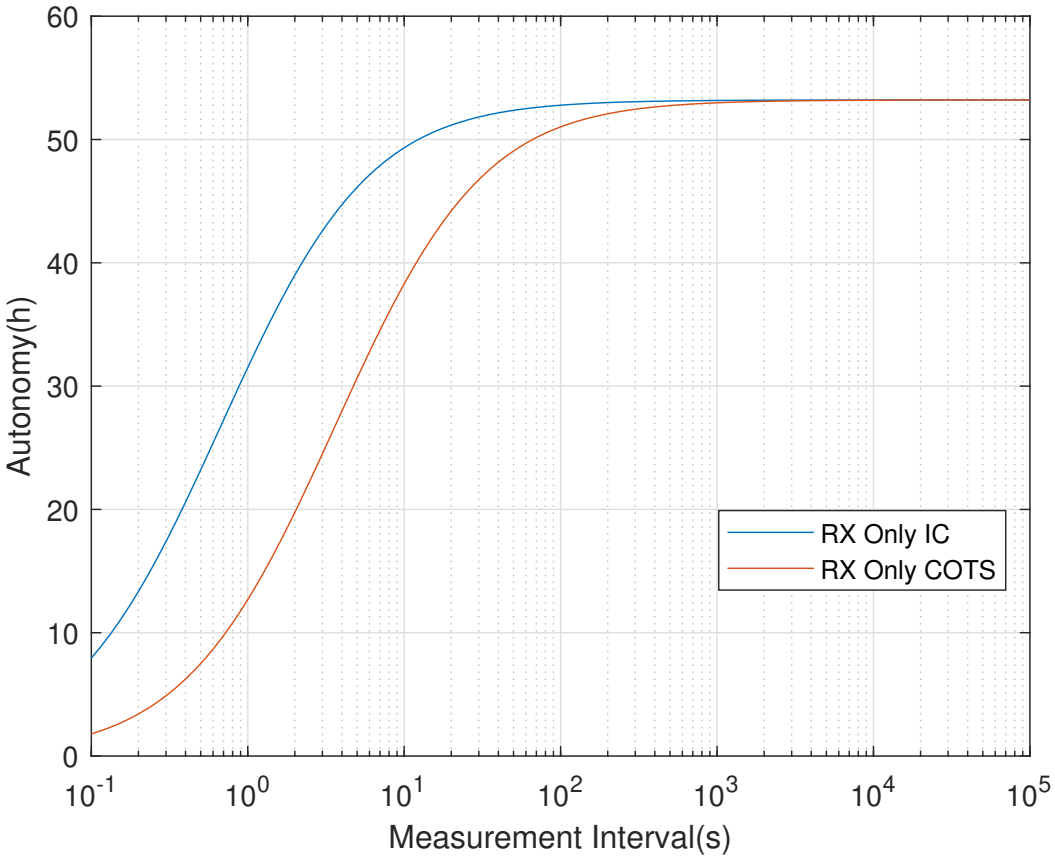



Figure 4.12: Autonomy of the Node in RX Only Mode.

### 4.4.3 Burst Mode

The next possible mode is the Burst Mode. In this scenario, the node is set to perform measurements spaced by a fixed interval, and once a day, the data are sent by the radio. In this scenario, the MCU is programmed to do this task, so the WuRx is deactivated as presented in Fig. 4.13.

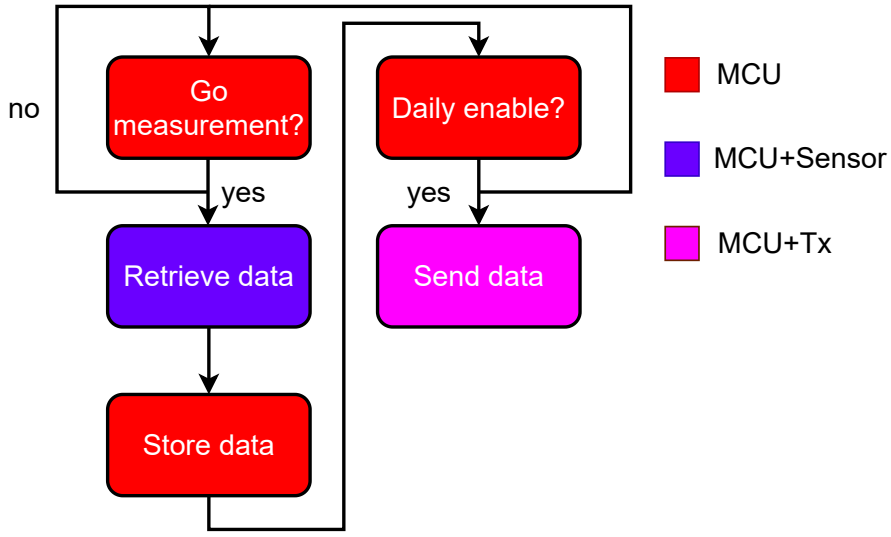



Figure 4.13: Burst Mode Illustration.

Fig. 4.14 presents the autonomy of the COTS and IC nodes in Burst Mode. For the same measurement intervals than previously, the COTS node presents an autonomy of 25, 43 and 47 hours. The results with the IC node are the same as in RX Only Mode. The improvement in this scenario is reduced to 20%, 7% and 4%.

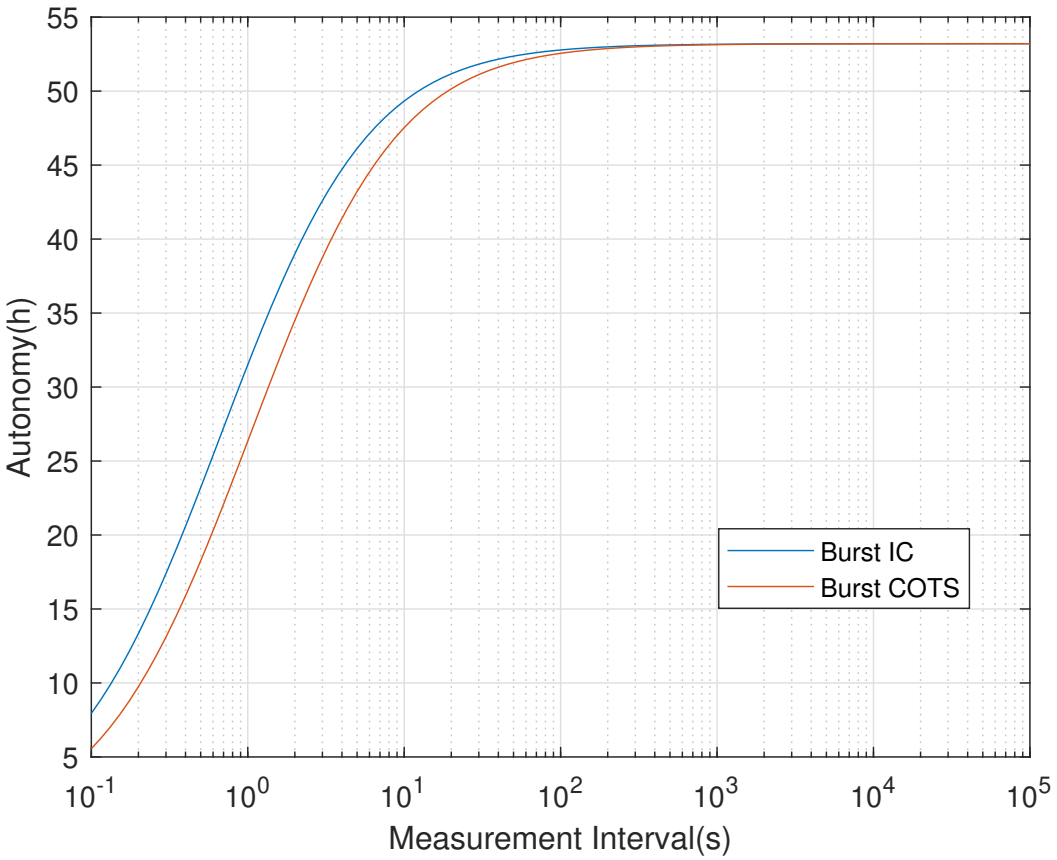



Figure 4.14: Autonomy of the Node in Burst Mode.

In WSN#1, there is a significant difference between RX Only and Burst Modes because the WuRx power consumption was 1µW. The contribution of this circuit was not negligible.

In WSN#2, the power consumption of the WuRx is so low that the scenario shift from Rx Only to Burst does not bring a significant improvement in term of autonomy. This shows that the WuRx power consumption has been decreased enough so that its impact becomes insignificant in the entire system. The Burst mode has no real interest now while it was a good option in WSN#1, this illustrates the contribution of the work in WSN#2.

### 4.4.4 Energy Harvesting Contribution

The results presented in the previous sections are based only on the discharge of the capacitor, it does not take into account the contribution of the energy harvester which loads the capacitor during the node operation. This circuit should therefore contribute to increase the autonomy of the node with a more important impact at higher light intensities.

Fig. 4.15 presents the variations of the node autonomy in RX/TX Mode for different levels of light intensity to cover various application possibilities.

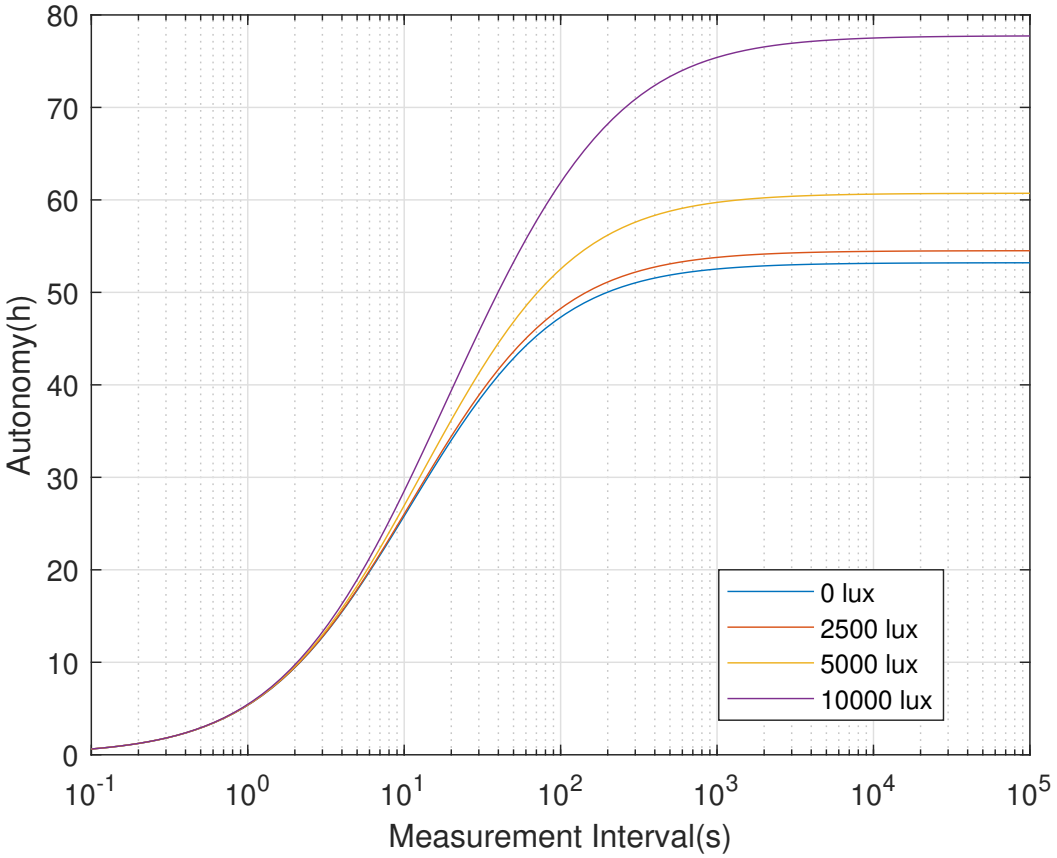



Figure 4.15: Autonomy of the Node in RX/TX Mode with Light Variations.

The maximum autonomy goes from 53 hours at 0 lux to 55.5, 61 and 77 hours at 2500, 5000 and 10000 lux respectively. This represents an increase of 4.7, 15 and 45%. At lower measurement intervals, there is no difference between the curves because the amount of energy spent is so high that the energy harvesting block has no significant impact. The contribution of the energy harvesting begins to appear from a measurement interval of 10s.

Fig. 4.16 presents the variations of the node autonomy in RX Only Mode depending on the light intensity. These results can also stand for the Burst Mode.

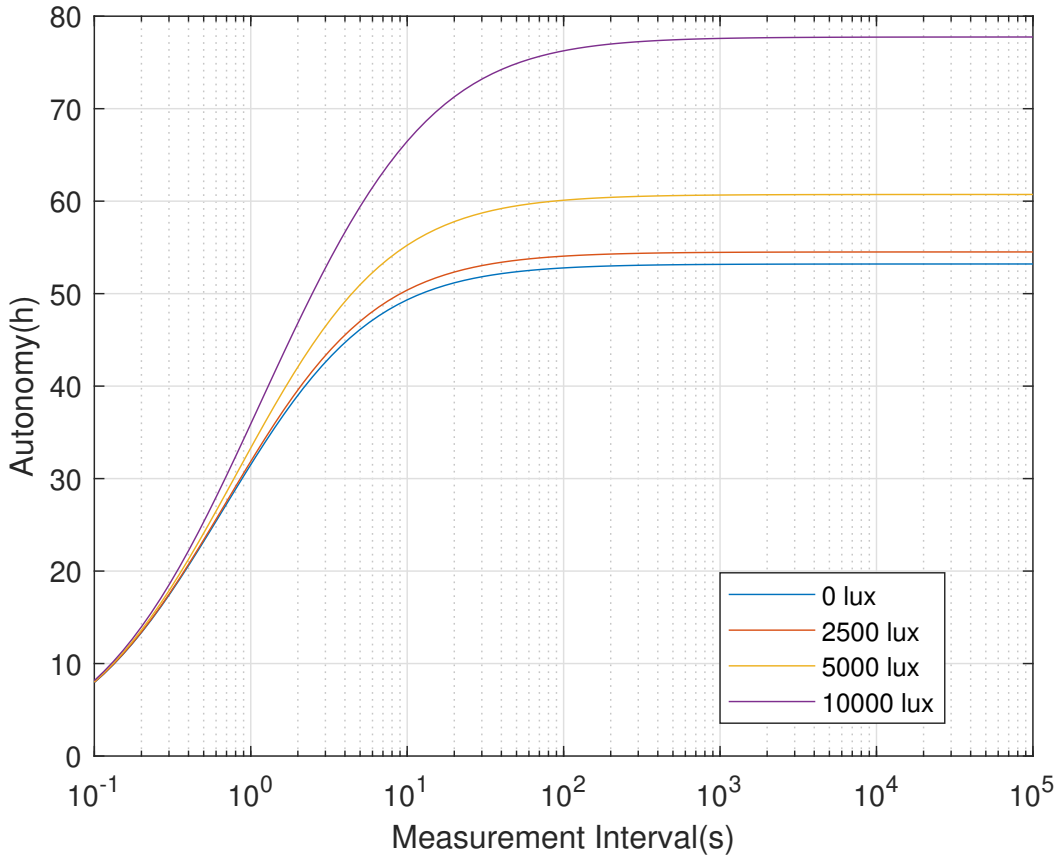



Figure 4.16: Autonomy of the Node in RX Only Mode with Light Variations.

The performance in term of maximum possible autonomy is the same in RX/TX Mode. The difference can be noticed in the measurement interval at which the impact of the harvester appears. In RX Only Mode, the curves separate from a measurement interval of 1s while in RX/TX Mode the separation occurs after 10s. This is due to the activity of the radio which affects the autonomy of the operating routine.

Another idea of improvement is to increase the number of peripherals in the node, although with many peripherals, the performance gap between the IC and COTS nodes become lighter. Fig. 4.17 presents the comparison of the required power to function in continuous mode between the IC and COTS node. The comparison is performed with several number of peripherals. In the first case, the MCU is running alone, after that, a temperature sensor and then, a pressure sensor are added. It can be noticed that with a higher number of sensor, the interest of an IC node is restrained. This shows that it seems better to use the IC node for dedicated applications or for footprint management.

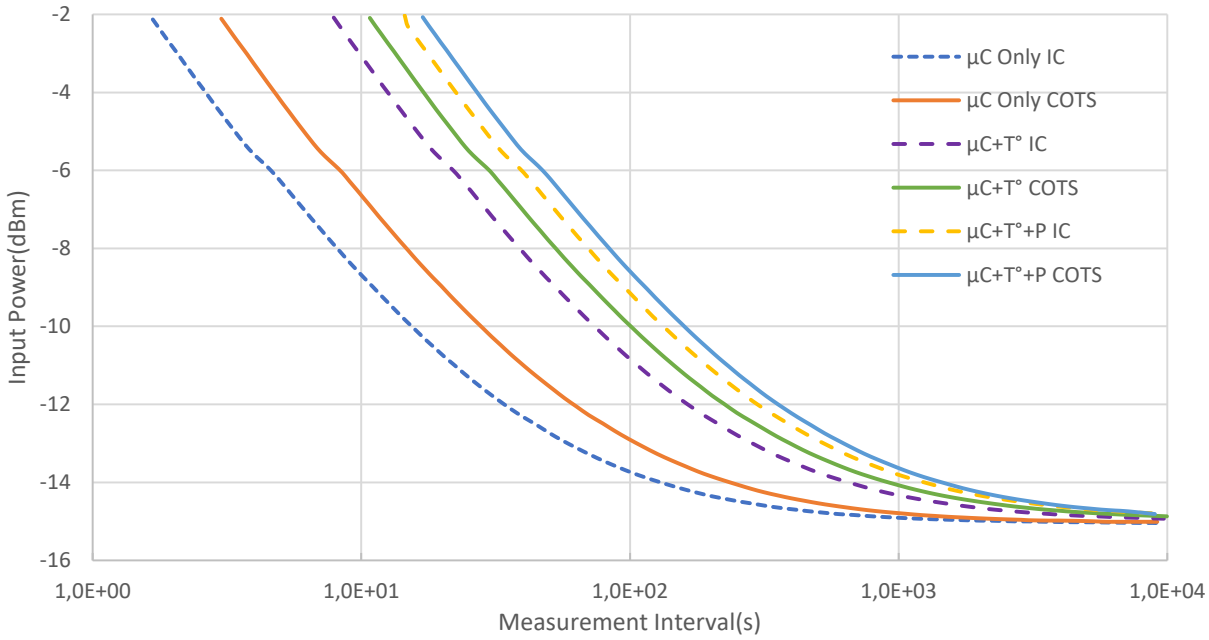



Figure 4.17: Input Power Requirement for the Nodes with Several Sensors.

## 4.5 Conclusion

This chapter has presented an analysis of the node performance for various scenarios of application. The estimation of the performance is worked out by a Matlab script developed by Dr. John Nicot during his PhD. The accuracy of the script results has been verified over many measurement results with the COTS node WSN#1.

Table. 4.4 summarizes the differences between WSN#1 and WSN#2 concerning continuous RF operation and autonomy.

Table 4.4: Comparison Between WSN#1 and WSN#2.

| Scenario | Subscenario | Results | Details |
|---|---|---|---|
| Continuous RF | RX | -12.2dBm$^{(1)}$/ $-13dBm^{(2)}$ | 1-minute measurement interval |
| | RX/TX | -9.1dBm$^{(1)}$/ $-9.5dBm^{(2)}$ | |
| Autonomous | RX | Every 4s$^{(1)}$/$0.6s^{(2)}$ | 24 hour autonomy |
| | RX/TX | Every 15s$^{(1)}$/$1s^{(2)}$ | |
| | Burst | Every 1s$^{(1)}$/$0.6s^{(2)}$ | |

$(^1)WSN\#1$ $(^2)WSN\#2$

With continuous RF source, operation is possible every minute, with power levels of -13 dBm and -9.5 dBm for RX Only and RX/TX Modes, respectively. Operating at higher speeds would be theoretically feasible. However this situation would face practical limitations due to the substantial RF power required to maintain the node on operation. Such demands might not be realistic due to emission constraints, particularly when considering the node's distance from the power source.

The possible addition of multiple sensors would increase the minimal amount of power required for operation, and for a high number of peripherals, the usefulness of the IC version of the node instead of the COTS version is questionable.

With solar harvesting, the node presents a maximum autonomy ranging from 53 to 77 hours depending on the lighting conditions. The autonomy estimation is performed for various scenarios, RX/TX, RX Only and Burst Modes. This allows to moderate the solicitations on the node and save as much energy as possible depending on the application for the node. For a measurement interval of 1s, the autonomy of the node in RX/TX, Rx Only and Burst Mode is 5 hours, 30 hours and again 30 hours respectively.

# CHAPTER 5

# CONCLUSION

## 5.1 Introduction

This chapter will conclude this work. Firstly, the node will be compared to other works and the results will be analyzed. Then, possible improvements to the node, and discussion of possible future research, will be discussed. Finally, a brief conclusion over the whole work will be presented.

## 5.2 Comparison to Other Works

Given the varied topologies and diverse solutions employed in works within the same domain, as shown in Table 5.1, it remains difficult to provide a fair comparison according common metrics. Nevertheless, it is feasible to categorize the various systems and to ascertain the node's placement within these categories.

Table 5.1: Node Comparison with State-Of-the-Art.

| | Energy Source | Freq | Sensitivity | Type | RX/TX? | Load |
|---|---|---|---|---|---|---|
| This Work | RF/Solar | 400MHz/900MHz/2.4GHz | -55dBm | IC/COTS | RX/TX | WuRX,MCU,Sensor,Transceiver, PMU |
| [47] | RF/Solar | 900MHz | -15dBm | COTS | RX/TX | $\mu C$ (PIC), FRAM 2x PMU (bq255XX) RF Transceiver Sensor(s) |
| [84] | RF/Solar | 2.4GHz | -15dBm | COTS | RX/TX | PMU,$\mu C$,Transceiver,Sensor |
| [85] | RF/Solar | 2.4GHz | -15dBm | COTS | RX/TX | PMU,$\mu C$ |
| [86] | RF/Solar | 800MHz-2.5GHz | -15dBm | COTS | - | - |
| [87] | RF/Solar | 900MHz | >24dBm | COTS | RFID | Class E Oscillator |
| [88] | RF/Solar | 900MHz | - | COTS | RFID | WISP 4.1 or RFID IC |
| [89] | RF/Solar | 1GHz | -17dBm | IC | - | - |
| [90] | Multi RF | UHF DTV/2GHz/3GHz | -10/-29dBm | COTS | - | PMUs |
| [91] | RF | Multi Channel UHF DTV | -4dBm | COTS | - | $\mu P$ (PIC) PMU |
| [92] | RF | 2.4GHz | -20dBm | COTS | - | Custom solar-powered RF-boosting PMU |
| [93] | RF | 900MHz, 2.5GHz | -20dBm | IC | RX | - |
| [94] | RF | 2.4GHz | -7dBm | COTS | RX | WuRx |

The novel aspect of this work is the combination of integrated circuits with market components to assembly a full node. This node is able to function with solar or RF harvesting and can work as a receiver and a transmitter.

The node is able to send data with the transceiver on request coming into the WuRx. The sensitivity of the node is drastically better than the other works, which confirms the interest of the integration for the WuRx.

The node proposed node includes five different sub-circuits, which is more than most of the works presented in the state of the art.

These features allows the node to: receive orders, measure data and broadcast them on request or according different scenario.

To evaluate the performance of the node in according a case of application, a simulator developed on Matlab is exploited. The accuracy of this simulator has been formerly

proven with the COST demonstrator (WSN#1) based on a large set of measurement. The only limitation of this method is that measured values of the power consumption of the different part of the node are preferable to estimate the overall performance than data sheets for the COTS devices embedded in the system. The simulation of the node brings two major advantages: a) it gives the opportunity to evaluate the interest of new scenario without constrains on its set up b) it dramatically reduces the time dedicated to evaluate a scenario compared to an actual test of each possible configuration. Only the meaningful and promising set up would be considered for measurement.

The choice was made not to rely on RF harvesting only because the levels of power required to properly operate the node would be too large. This option will be evoked in the next section. Concerning solar harvesting, this solution is implemented at various illumination levels, ranging from low-light indoor environments up to full sunlight. The electrical power harvested from solar modules ranges from several dozens of microwatts up to several milliwatts.

Most COTS systems exhibit a similar size, ranging from several $cm^2$ to approximately 500 $cm^2$ in diameter. ASICs development, such as the one proposed in this work, allows for a reduced silicon footprint, and so a better integration in the environment of application.

## 5.3 Future Perspectives

Although the node presents encouraging results, it is always possible to improve different aspects of the system. The first parameter to improve is the autonomy to extend the system lifetime. This leads to diminish the power consumption of the node and to increase the efficiency of the energy harvesting. The robustness of the node can also be discussed.

It was pointed out that COTS components limit the node performance, particularly concerning sensitivity and power consumption. The design of the WuRx and the MCU with custom design allowed to improve the node.

The sensitivity of the WuRx has drastically improved in comparison with COTS topologies as it was expected. Some topologies in the state of the art present better sensitivities than what was achieved, which shows that gains are still reachable. The study of rectifiers is very active in the literature, hopefully, new topologies can be found blended with new technological nodes to continue increasing the rectification sensitivity and efficiency.

Solar power harvesting is still the most popular and powerful method to gather energy from an external source of energy. The solar panel used in this demonstrator are cheap devices, their efficiency and sensitivity are not optimized. Besides solar panels are difficult to recycle and their manufacturing generates a lot of pollution. It would be interesting to encourage work in novel methods such as organic photovoltaic cells that are currently under development. Finally the autonomy of the node under very low duty cycling operation remains limited by the self-discharge of the supercapacitors. The reduction of supercapacitor leakage is maybe the first point of improvement for long time autonomy.

It would be interesting to develop an harvesting module capable of collecting the power from various source of energy. This approach was tested by J. Nicot during his PhD by combing solar and RF harvesting. Interestingly a similar combination is now under development in E-Peas company[95].

The proposition to have a custom MCU only designed for one application has presented promising results. To have a more versatile node, the interfacing can be designed to connect multiple sensors to extend the range of measurement. The correlator in the WuRx would feature several code words in parallel corresponding to different sensors, and one output for each word, then the MCU receives the wake up signal corresponding to the requested sensor. This modification would come at an extra power consumption and an additional complexity to the MCU. Exploring more advanced CMOS technologies for the MCU could be interesting, in terms of computing performance. But it is important to keep in mind that computing skills are first balanced with power saving in WSN applications. This lead to the development of the minimalist MCU proposed in this work. CMOS shrink comes at the cost of extra leakage current which could crippling for (ultra) low power power applications such as WSN. This point must really discussed at the early stage of a node development. Besides advanced CMOS nodes exhibit increased device leakage which could be crippling for ultra low power concerns.

Several scenarios were presented in the previous part, here again the MCU can be programmed to function in the different modes, this implies to be reconfigured. This means having an external access with a computer to set the MCU, this is a possible modification for the circuit.

The demodulation of the incoming data suffers from a non negligible probability of false wake-ups. This is due to two factors, the first one is that there is a lot of activity at 900MHz or 2.4GHz that can corrupt the received signal. The second factor is that the OOK modulation is not a robust method and presents a high risk of failure. To overcome this issue, more complex modulation method can be used such as BPSK in a first time. This will inevitably increase the power consumption and so have an impact on the node autonomy, but it is necessary to achieve more robustness for the WuRx.

The WuRx can be used in other applications than WSNs. Basically, it can be exploited in any device requiring a wake up system to save energy. With a power consumption of 10nW, the WuRx can bring an interesting feature at almost "zero power cost".

The presented results show that the limiting factors to reach a higher autonomy are the peripherals particularly the main radio which draws a high amount of power and the supercapacitor because of its internal leakage.

One possible solution would be to do the same work on the peripherals that what is proposed for the MCU, i.e. designing custom devices which fits the targeted application without additional features. Considering the sensor as an example, the design of an integrated sensor can be of course envisioned. This would avoid the SPI communication, the setting before the measurement and would probably increase the speed. Of course, this leads to no configurability and less flexibility. The same remark can be done with the radio module. A simpler radio without multiple functioning options could be considered, and this would help to reach a better autonomy.

Concerning the simulator, results presented in Dr. Nicot's thesis showed that the simulator is reliable. An interesting improvement is to reshape the code to a more system study version. The idea would be to design an interface with components and peripherals performances, the user chooses the devices he wants to implement and the software gives the autonomy estimation. Such interface could be compatible with some existing platform of device development such as[96].

## 5.4 Conclusion

The purpose of this work was to analyze the benefits of implementing integrated circuits in an IoT node instead of using market components. The performance using RF/solar energy harvesting were also studied. It was determined that the Wake-Up Radio and the microcontroller could present good improvements for the node performances.

The design of the WuRx and the MCU was done in 65nm technology. After PLS simulations, the WuRx which is the always active part of the node presents a power consumption of 8.34nW, the core of the MCU has a dynamic power consumption around $15\mu W$(without its clock).

The WuRx is compatible with different band of operation: 400MHz, 900MHz or 2.4GHz. The node has a sensitivity of -55dBm, -53dBm and -50dBm at these frequencies. The WuRx is able to function at a data rate of 1kbps and is relatively robust to temperature variation over a range of 0 to 40°C.

The designed MCU is a 32-bit MCU with a minimalist instruction set working at a clock frequency of 100MHz. It contains a SPI interface to communicate with its peripherals.

Considering continuous operation with a RF source, the node can function with RF power levels from -3dBm to -15dBm for a measurement interval from 10s to 10000s respectively.

When using solar energy, the device presents an autonomy from 53 hours to 77 hours depending on the light intensity. The maximum autonomy is limited by the internal leakage of the supercapacitor.

Several operational scenarios that can be implemented in IoT nodes were described and studied, providing further perspective on the capabilities and constraints achievable within a specific range of operational contexts.

The final step is the manufacturing of the integrated circuits and the assembly of the node. Knowing that the simulator results were checked positively before, the performances of the upcoming node promise to be convincing, opening a door to new research activities.

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# SCIENTIFIC PRODUCTION

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