Development and characterization of novel electronics for the search of dark matter for DAMIC-M

Georgios Papadopoulos

Sorbonne Université

École doctorale des Sciences de la Terre et de l'environnement et Physique de l'Univers, Paris - ED 560

Laboratoire de Physique Nucléaire et de Hautes Énergies (LPNHE) - UMR 7585

Development and characterization of novel electronics for the search of dark matter for DAMIC-M

Thèse présentée par

Georgios Papadopoulos

Dirigée par

Antoine Letessier Selvon & **Romain Gaïor**

Mme. Christine Marquet, D.R. Université de Bordeaux	**Rapportrice**
M. Konstantinos Nikolopoulos, Prof. University of Birmingham	**Rapporteur**
M. Bertrand Laforge, Prof. Sorbonne Université	**Président**
M. Thomas Papaevangelou, I.R. CEA	**Examinateur**
M. Paolo Privitera, Prof. University of Chicago & Sorbonne Université	**Examinateur**

Sorbonne University

Doctoral school of Earth and Environment Science and Physics of the Universe, Paris - ED 560
Nuclear and High Energy Physics Laboratory (LPNHE) - UMR 7585

Development and characterization of novel electronics for the search of dark matter for DAMIC-M

Thesis presented by
Georgios Papadopoulos

Supervised by
Antoine Letessier Selvon & **Romain Gaïor**

Mme. Christine Marquet, D.R. Université de Bordeaux	**Referee**
M. Konstantinos Nikolopoulos, Prof. University of Birmingham	**Referee**
M. Bertrand Laforge, Prof. Sorbonne Université	**President**
M. Thomas Papaevangelou, I.R. CEA	**Examiner**
M. Paolo Privitera, Prof. University of Chicago & Sorbonne Université	**Examiner**

"Ένα μονάχα λαχταρίζω: να συλλάβω τι κρύβεται πίσω από τα φαινόμενα,
τι είναι το μυστήριο που με γεννάει και με σκοτώνει,
κι αν πίσω από την ορατή ακατάπαυστη ροή του κόσμου
κρύβεται μια αόρατη, ασάλευτη παρουσία."

Ασκητική, Νίκος Καζατζάκης

(English translation)

"I have one longing only: to grasp what is hidden behind appearances,
to ferret out that mystery which brings me to birth and then kills me,
to discover if behind the visible and unceasing stream of the world
an invisible and immutable presence is hiding."

The Saviours of God, Nikos Kazantzakis

Acknowledgements

Besides a report of a ∼4-year-long work for my PhD, this manuscript is the epilogue of the second "book" of my adult-life during my 5 years in Paris. Nothing came easy and required much effort to stand where I am today. Fortunately, I was lucky enough to have some people by my side that helped me, stood by me, believed in me, and I am grateful to them.

I want to thank my mother Φρόσω for everything she sacrificed to raise me and for constantly believing in me. I only hope she looks at the result and feels proud of herself.

I thank the Σεϊταρίδης and Λαζαρίδης families for the invaluable support, without which I cannot imagine where I would have been today. My aunt Χαρίκλη† and her son uncle Κώστας stood up when I was in need and financially supported me without much unnecessary discussion. Μελίνα has been the best older "sister" one could ask for, always caring for my personality development and my looks. She has been an inspiring person that I always looked up to, who financially supported me when I was in need and she was only 22 years old (who does that?!). No amount of money can be repaid for what they did to me. I only hope they will always feel happy about their investment.

I want to thank Miranda who has been by my side for most of the duration of my PhD and never stopped supporting me.

I thank Julianna for all the bureaucratic help, all the deep conversations, and for putting up with me despite my weird taste of humor. You were one of the first and few who made my unwelcome arrival in France much welcome.

I give credits to Nefeli for her help with some of the figures in this thesis.

I thank all the PhDs of LPNHE for all the great moments that we shared and for creating such a wonderful working environment, with coffee breaks, beers, illegal parties, trips, and even a wedding. I hope I have given back to you all the smiles you gave to me. (Un)fortunately, there are many photos and videos to keep these memories alive.

A special thanks to my supervisor Antoine who I managed to persuade to give me this opportunity and I only hope he does not regret it today, to Romain for being the person I worked with for guiding and advising me, to Hervé who has taught me a lot about electronics, to David who always treated me as an equal colleague, to Julien for teaching me how to make my life easier and not burn my hands while soldering, to Marc for all the laughs at the lab, and to Philippe for the help in the electronics and their

control. I thank Latifa, Joao, Ariel, Michelangelo, Julie, Jean-Philippe, Claudia, Lounes, Georgia, who are interns/PhDs/post-docs/collaborators, of DAMIC or not, that I worked with, shared my office, and taught by during this long period. They all motivated me, they inspired me with their personal work and effort, they recognized me for my skills, and each one individually has their name behind some paragraph in my thesis.

Everything I have achieved has been a personal effort, but with the help of the people above and also more who, with or without knowing it, motivated and inspired me to continue, try harder, and want more for myself. I owe Miltos Ts., Theodosis Ch. and fam, Kostas Sk., Fragkiskos M., Stergios Ch., and more a special thanks as a sign of gratitude.

Contents

Acknowledgements **ii**

Introduction **1**

1 Dark Matter **3**

1.1 Prehistory . . . 3
1.2 First evidences in the 20^{th} century . . . 4
1.3 Modified gravity theories . . . 5
1.4 Evidence up-to-date . . . 6
1.4.1 Galaxy rotation curves . . . 6
1.4.2 Gravitation lensing . . . 7
1.4.3 Cosmic Microwave Background . . . 9
1.5 Dark matter candidates . . . 10
1.5.1 (Primordial) Black holes as dark matter . . . 10
1.5.2 (Sterile) Neutrinos as dark matter . . . 11
1.5.3 Weakly Interacting Massive Particles (WIMPs) . . . 11
1.5.4 Hidden/Dark sector . . . 13
1.5.5 Axion . . . 13
1.6 Dark matter detection approaches . . . 14
1.6.1 Production . . . 14
1.6.2 Indirect search . . . 14
1.6.3 Direct search . . . 15

2 Charge Coupled Device **19**

2.1 CCD structure . . . 20
2.2 Charge Generation . . . 23
2.3 Charge Collection . . . 25
2.4 Charge Transfer . . . 29
2.5 Charge Measurement . . . 33
2.5.1 Noise sources . . . 36
2.5.2 Measuring techniques . . . 37

2.6 Scientific CCD operating conditions 38

3 DAMIC-M **40**
3.1 DAMIC at SNOLAB 40
3.2 The future with DAMIC at Modane 42
3.2.1 The heart of the detector 43
3.2.2 Near-CCD Background 43
3.2.3 Detector shielding and LSM 45
3.3 DAMIC-M new electronics 46
3.4 CCD testing at surface level in LPNHE, Paris 48
3.5 Low Background Chamber 53
3.6 DAMIC-M expected sensitivity 54

4 Control board **55**
4.1 CABAC2 chip 55
4.1.1 Single CABAC chip evaluation 56
4.2 4CABAC control board 59
4.2.1 CCD sequencer 60
4.2.2 4CABAC evaluation - Test sequencer board 64
4.3 ProtoCABAC: one CABAC - one DAC prototype board 68
4.3.1 ProtoCABAC biases characterization 69
4.3.2 ProtoCABAC clocks characterization 70

5 Front-end amplification **75**
5.1 CROC: CCD ReadOut Chip (version 1) 75
5.1.1 CROC block diagram 76
5.1.2 Programming CROC 79
5.1.3 CROC evaluation setup 80
5.1.4 CROC v1 gain calibration in Transparent mode 81
5.1.5 CROC v1 input noise measurement in Transparent mode 86
5.1.6 CROC v1 *RC* time constant calibration in DSI mode 87
5.2 CROC v2 90
5.2.1 CROC v2 in Transparent mode 90
5.2.2 CROC v2 in DSI mode 92
5.3 DCA: Differential CCD Amplifier 94
5.4 CCD testing with Leach and CROC v1 97

6 Analog-to-Digital Converter **102**
6.1 AD5791 Digital-to-Analog Converter characterization 102
6.2 Rapide 4-ADC prototype board 105
6.2.1 Input noise 106

6.2.2 Linearity study with DC input signal 108
6.2.3 ADC evaluation for AC input signals 109
6.2.4 ADC cross-talk evaluation for AC input signals 109
6.3 New ODILE-compatible ADC boards for DAMIC-M 111

Conclusions **112**

A CABAC chip programming **115**

B Fully differential integrator **116**

Introduction

The understanding of the universe and what it consists of has been a subject of interest especially after discovering that everything that we see is only a small portion of the whole. We consider a universe filled with invisible substances that can only be observed from their effect on large structures, from galactic scales and above. The hypothesized dark matter is expected to account for about 25% of the universe's energy-mass content. There is evidence connected to phenomena that cannot be explained by the current theory of gravity, from the orbital velocities of outer stars in galaxies, to the structure of the whole universe. An introduction to dark matter and a brief review of the different approaches that are adopted for its hunt are presented in Chapter 1.

The DAMIC collaboration is dedicated to the search for dark matter candidates through their direct interaction with ordinary matter. DAMIC pioneered this search using scientific-grade silicon Charge-Coupled Devices (CCDs). Chapter 2 provides a detailed description of the CCD operation, which was crucial to understanding the tasks I undertook during the last few years. The upcoming experiment, DAMIC-M, will employ CCDs with skipper readout that allow for multiple non-destructive pixel charge measurements leading to an excellent resolution of a fraction of a single electron in charge units. This will offer a low detection energy threshold down to a few electrons, which corresponds to about 10 eV. About 50 CCDs with a total target mass of ∼1 kg will be installed in the underground laboratory at Modane (LSM), with its installation expected to start in 2023. This detector will be sensitive to low-mass dark matter candidates and particularly for dark matter-electron interactions and other hidden sector candidates. Prior to the DAMIC-M experiment, a test detector has been installed in LSM and started its operation in 2022, called Low Background Chamber (LBC). The LBC will test the new DAMIC-M CCDs and measure their dark current with a skipper amplifier, measure their intrinsic activity and the background of LSM as well, and test the new acquisition system designed for DAMIC-M. Chapter 3 reviews the present and future of the DAMIC detectors, as well as the status of the DAMIC group in LPNHE, Paris.

A new custom acquisition system is designed by the collaboration for the control and readout of the CCDs. A CCD requires bias voltages and alternating signals (clocks) that control the device, provided by the control board. The output of the CCD passes from two stages: front-end amplification and conversion from the analog to the digital domain.

The CCD signal is very small and sensitive to any introduced noise, so a preamplification as close as possible to the CCD is necessary. The readout techniques can be supported by sophisticated pieces of hardware to allow for optimal configuration. The analog-to-digital converter must be fast with high resolution and compatible with the output of the front-end amplifier and several options were considered before a final choice for DAMIC-M. My work during this thesis was focused on the new electronics, the development of their control software, their evaluation, and their integration into a complete system, and was undertaken in the LPNHE lab in Paris. The progress of the three different modules is extensively described in Chapters 4, 5, and 6 respectively. There are also results presented of individual parts integrated in a CCD setup or a complete, yet preliminary, system operating with a skipper CCD on surface level. My work on the electronics allowed me to develop a more profound understanding of how integrated chips and other electronic components work in terms of programming, control, automatization, analog $\leftrightarrow$ digital conversion, and signal analysis.

Chapter 1

Dark Matter

1.1 Prehistory

The journey to understanding and explaining the physical world arguably started in ancient Greece [1]. Between the 6^{th} and 3^{rd} centuries BC, many theories were given birth by Greek philosophers based on reason and experience, in an attempt to explain the nature of the universe, and subsequently the matter. These theories contend that everything is composed of four fundamental elements: earth, fire, water, and air. Later, Aristotle included the fifth element of aether, which is related to the "sky", or what they were seeing in the sky, i.e. the universe. This philosophical attempt, since there was no means to test the hypotheses, may be considered the very first ancestor of the modern elementary particle physics. Every object, despite its size and structural complexity, must be made out of a handful of elements in various combinations.

Even though far from correct as we know it today, this model managed to survive until the 16-17^{th} century. The alchemists, as a first kind of experimental scientists, tried to manipulate certain materials in order to convert worthless metal into gold or discover the mythical philosopher's stone. The Islamic world rescued and developed Alchemy which later evolved into the modern science of Chemistry. In the early 19^{th} century, John Dalton discovered the building blocks of matter, the atoms. The etymology of atom comes from the ancient greek ἄτομον: "α-" (not) + "τέμνω" (cut), in other words the "uncuttable". This has been indeed what centuries ago was hypothesized to be the smallest amount of matter which constitutes every physical object, without being able to be further divided. One of the first historical atomic models was introduced by J. J. Thomson about a century later, who discovered the electron and proposed the "plum pudding model". This model describes a volume of positive charge with electrons spread, like negatively charged "plums" embedded in a positively charged "pudding". In their famous experiment in 1911, Hans Geiger and Ernest Marsden under the direction of Ernest Rutherford, bombarded a thin gold foil with, at that time called, alpha particles (today known as He^{2+} ions), only to observe that some of the particles are scattered backward. This would abrogate Thomson's

atomic model and proved that the atom is composed of a small dense positively-charged central region, the nucleus, with the negative charged electrons floating around it. This has been a breakthrough that led to the genesis of the Nuclear Physics, which was followed by a lot more discoveries until the establishment of the Standard Model (SM), a theory that unifies the electromagnetic and weak interactions, includes the strong interaction and describes the interactions among the known elementary particles (fermions and bosons).

Gravity is the first mathematically introduced interaction by Isaac Newton at the end of the 17^{th} century as the instant attractive force between two massive objects. Almost two centuries later, Albert Einstein changed completely the perception of gravity with his theory of General Relativity. What we experience as gravitational force is in fact the curvature of space-time. The more massive an object is, the more it bends the space-time around it and attracts other massive bodies. In the particle physics scale, the gravitational interaction is negligible and immeasurable in the presence of the other three interactions.

Despite all the great advancements that have been achieved and all the knowledge that has been gained, we are able to describe only a small portion of the universe. The Standard Model and General Relativity theories combined cannot explain all the observed phenomena. The latest measurements result in a universe consisting of ∼5% of ordinary-luminous matter, while ∼95% of it is unknown, made of *dark* substances [2]. Ordinary matter accounts only for ∼15% of the total matter in the universe with the rest of it generally called *dark matter*. To describe the whole 95% of the universe, alongside dark matter, an unknown form of energy must be introduced, generally called *dark energy*. The term "dark" is used because it is non-luminous, i.e. does not appear to interact electromagnetically. Only their effect on large scales is visible, like in distant galaxies, galaxy clusters, even the whole observable universe.

1.2 First evidences in the 20^{th} century

Henry Poincaré was the first to ever use the term "dark matter", originally "matière obscure" in French, in 1906 [3]. There might have been earlier mentions referring to the idea of undiscovered astrophysical objects though [4, 5, 6]. Studies on the stellar motions by Jacobus Kapteyn [7] and Jan Oort [8] predicted larger mass galaxies that were in conflict with the gravitational theory and the observed mass. Despite earlier mentions, that were proven to be wrong [9], Fritz Zwicky is usually credited for being the first who made correct arguments for the existence of dark matter. In his publications in 1933 and 1937, Zwicky provided a new technique for estimating the total mass of a galaxy based on the observed mass-to-luminosity ratio [10, 11]. He applied the virial theorem to the Coma Cluster to calculate its velocity dispersion and found that the observed one is about an order of magnitude higher. In his 1933 article, he explicitly quotes that:

"*Resultat ergeben, dass dunkle Materie in sehr viel grösserer Dichte vorhanelen ist als*

leuchtende Materie."

(English translation) *"The result shows that dark matter is present in much greater density than luminous matter."*

In 1937, he published a new article, this time in English, in which he extends his analysis on the Coma Cluster. He set a lower limit for the mass of the cluster at 4.5×10^{13} $M_\odot$ containing 1000 galaxies and estimated a surprisingly high mass-to-light ratio. Later results would find a smaller ratio [12, 13]. Even though his results were not accurate, as he over-estimated the mass-to-light ratio, his technique was valid and is still used today by observing the light of the X-ray emissions of interstellar gases.

Another estimation was provided by Sinclair Smith, in 1936, who studied the Virgo Cluster [14]. From the observed distribution function of the radial velocity, he calculated the total mass of the cluster to be equal to 10^{13} $M_\odot$, which he then divided by the 500 observed galaxies. As a result, he predicted an average mass per galaxy two orders of magnitude higher than Hubble's estimation for an average galaxy. He quotes (by "nebulae" they used to refer to what is known nowadays as galaxy):

"It is also possible that both values (the observed mass and the estimated one) *are essentially correct, the difference representing internebular material, either uniformly distributed or in the form of great clouds of low luminosity surrounding the nebulae."*

Not much later, Horace Babcock studied the Andromeda Galaxy, also known as Messier 31 (M31) or NGC 224, reporting unexpected orbital velocities for high radial distances [15]. The breakthrough was yet to come with the discovery of the 21-cm Hydrogen-I emission line. This particular photon emission of hydrogen atoms with a frequency of 1.42 GHz [16] can penetrate the large clouds of interstellar cosmic dust and is used for astronomical observations of distant objects. In the 1970s, a series of studies provided more detailed results on the rotational curves of the Andromeda and other galaxies by Vera Rubin & Kent Ford [17, 18], Rogstad & Shostak [19], Morton Roberts & Rots [20, 21], revealing a flat behaviour of the rotational curves for a radius beyond the radial distance in which most of the observed mass is concentrated. Based on the Newtonian mechanics, the rotational velocity should decrease with the square root of radius above the solid disc. This flatness indicates that there must be a gravitational effect higher than the expected one based on the luminous matter, for the galaxy to maintain its integrity. The existence of additional, invisible matter spread around the galaxies was established by the mid-70s.

1.3 Modified gravity theories

In 1982, in order to refute the idea of dark matter, Mordehai Milgrom proposed an alternative theory known as Modified Newtonian Dynamics, or MOND. This idea suggests a new expression for the Newtonian acceleration of gravity that depends on a scaling function which is effective only when the acceleration gets much lower than a new meant-to-be

constant a_0=1.2×10^{-10} m/s^2 [22]. In its preliminary state, MOND was violating many laws of physics, like the conservation of momentum or energy. Other models were developed in an attempt to keep untouched the fundamental laws and be compatible with the general theory of relativity. In 2004, Jacob Bekenstein proposed a relativistic theory of MOND containing three fields: a Tensor, a Vector, and a Scalar, known as TeVeS [23]. The TeVeS is the leading theory of MOND and has managed to survive until this day. However, it remains unclear if it can explain, at any level, certain observations, such as the anisotropies of the cosmic microwave background or the position of the center of mass in merging galaxy clusters with respect to the visible matter distribution (both are explained in the next section). Moreover, the recent discovery of gravitational waves sets new constrains for MOND theories [24].

1.4 Evidence up-to-date

In this section, I summarize the phenomena that cannot be explained by the current theories of Standard Model or General Relativity and indicate the existence of something beyond them. Moreover, I will explain how the proposal for a dark matter is derived as a solution for them.

1.4.1 Galaxy rotation curves

One of the first inconsistencies with the theory and a strong indication for something yet undiscovered is the study of the rotation curves of galaxies. In general, astronomical objects bound in orbit $\mathbf{r}(r)$ around a massive center follow the Keplerial velocity:

$$v(r) = \sqrt{\frac{G\,M(r)}{r}} \tag{1.1}$$

where G is the gravitational constant, r the radial distance, and $M(r)$ the mass included in the disk of radius r. In our solar system, the sun accounts for more than 99% of the total mass. Thus, the orbital velocity of the planets will approximately follow the $r^{-1/2}$, since the contribution of any mass other than the sun is not significant. This relation is confirmed by the experimental measurements of the orbital velocities of the planets. In galactic scales, the velocity should follow the distribution shown in Figure 1.1 left with the short-dashed red curve, given as an example for the M33 galaxy. The galactic disk is the area where most of the luminous mass of a galaxy is found. Outside of it there is the galactic halo, which contains much less stars and so the mass contribution becomes lower. This explains the decreasing velocity shape in Figure 1.1 left short-dashed line, where the distance increases but the mass does not as much. An extended study of the rotational velocities of several galaxies is shown in Figure 1.1 right. The majority of the curves have a consistent flat shape far from the galactic center.

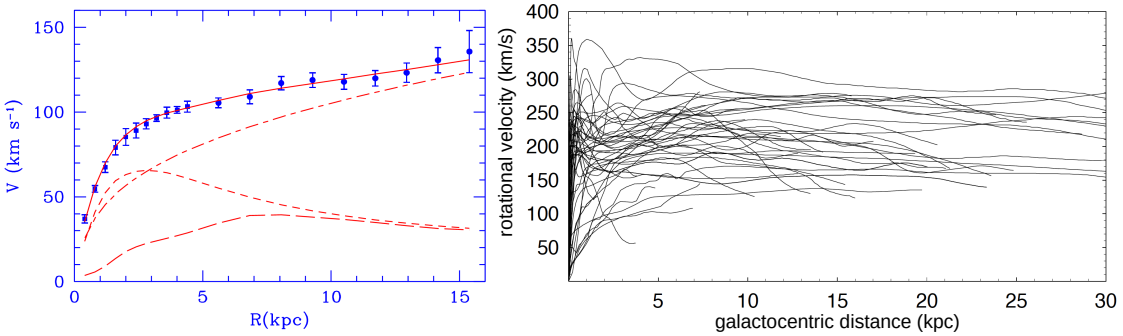

Figure 1.1: Left: The rotation curve of M33 (blue points) with the best fit model (continuous red line), the halo contribution (dashed-dotted line), the galactic disk (short dashed line) and the gas contribution (long dashed line). [25] Right: Rotation curves of several galaxies. [26]

However, the observations do not agree with that. Contrarily to the Keplerian model, the velocity of the stars far from the galactic disk is flat. With the known gravitation theory and the experimental data, the outer stars should have high enough speed to escape the galaxy, and yet they do not. Some other source of force should keep these stars attached, like extra gravity. The existence of non-luminous matter spread around the galaxy, denser in its center but reaching its far edges, can change the mass term in equation 1.1 and may explain the orbital velocity.

1.4.2 Gravitation lensing

Instead of looking directly at the galaxies, it is possible to look at the influence they exert to the image of galaxies "behind" them. Similar to an optical lens, the light is bent by the gravity of large structures it meets until it reaches the Earth, such as galactic clusters. The light deflection is called gravitational lensing and it is predicted by the theory of the general relativity.

Strong gravitational lensing causes far away objects to be observed distorted, elongated or even duplicated in telescope images. A special case of gravitational lensing is the Einstein ring, which is formed when a luminous galaxy is collinear with the gravitational lens and the Earth, resulting to a symmetrical image of the far object like a ring around the massive interfering mass. An example of this fascinating phenomenon is presented in Figure 1.2.

Weak gravitational lensing is a more systematic and statistical approach in studying the matter distribution at large scales [28]. An example of weak lensing and one of the most direct evidence for the existence of dark matter is the discovery of the ongoing galactic cluster merger 1E 0657-56 in 1995 [29], which was given the name *Bullet Cluster* (see Figure 1.3). The cluster consists of two colliding sub-clusters [30], containing galaxies, X-ray emitting gas as ionized atoms at very high temperatures in a plasma state, and potentially dark matter. The gas is about 10 times more massive than the galaxies in a cluster. The galaxies behave like collisionless particles is such a large volume of interaction

Figure 1.2: Hubble Space Telescope image of the *Cosmic Horseshoe*, the light of a much more distant blue galaxy gravitationally distorted by a giant luminous red galaxy (LRG 3-757 [27]) into a nearly complete Einstein ring. Image credit: ESA/Hubble & NASA.

and they practically pass through the cluster intact, while the hot gas slows down as it experiences ram pressure due to the attractive force between the two fluids. The detection of the X-ray emission of 1E 0657-56 by Chandra telescope shows the density of the hot gas in Figure 1.3 right [31, 32]. At the same time, the green contours show the reconstructed mass distribution using weak gravitational lensing. The peaks of the mass distribution (white contours) are outside of the dense gas area and agrees with the galaxy density as shown in the photo of Figure 1.3 left, which indicates the presence of additional non-luminous and collisionless matter, the dark matter. In the absence of dark matter, the center of mass would be expected to follow the peaks of the gas distributions, which is clearly not the case. Considering the mass ratio of the gas and the galaxies, the dark matter should be multiple times greater than the total visible mass of each galaxy cluster in order to shift the lensing center that far from the gas. A similar observation was recorded in 2008 of the merging cluster MACS J0025.4-1222 [33].

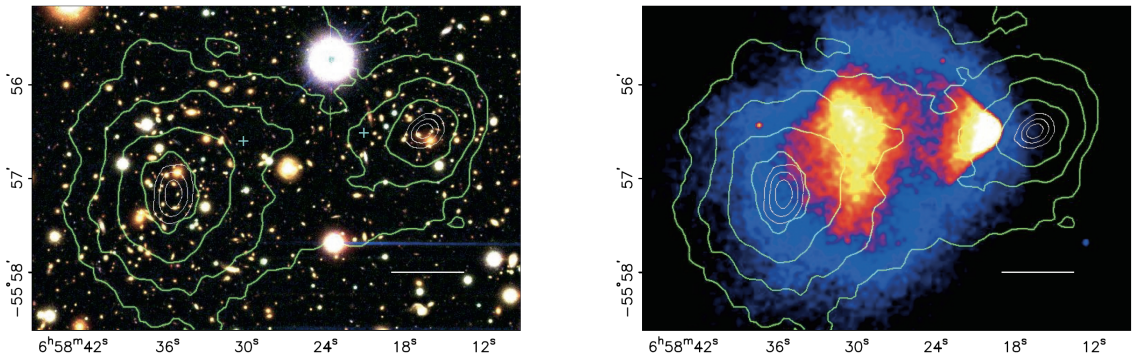

Figure 1.3: Images of the 1E0657-56 merging cluster with the reconstructed mass distribution using weak gravitational lensing (green contours) and on the right the X-ray image of the bullet cluster, taken by Chandra (color scale). [32]

1.4.3 Cosmic Microwave Background

In 1965, Arno Penzias and Robert Wilson discovered accidentally a "relic" electromagnetic radiation from the early universe known as *Cosmic Microwave Background* (CMB) [34]. In its very beginning, the universe was too hot to allow the photons to travel freely. As it cooled down, the electrons and protons started to bound to atomic states and photons were liberated and are detected today from that era.

The CMB spectrum has been measured by several experiments and telescopes, like NASA's Cosmic Background Explorer (COBE) [35] and Wilkinson Microwave Anisotropy Probe (WMAP) [36], with the most recent provided by the European Space Agency's (ESA) Planck spacecraft. Its operation lasted approximately 4 years until 2013 and the final results were published in 2018[1]. The CMB temperature spectrum is almost isotropic and consistent with a black body of temperature $2.72548 \pm 0.00057\,\mathrm{K}$ [37]. However, this spectrum presents small variations in the order of μK. A map of the whole sky of the CMB temperature fluctuations is shown in Figure 1.4.

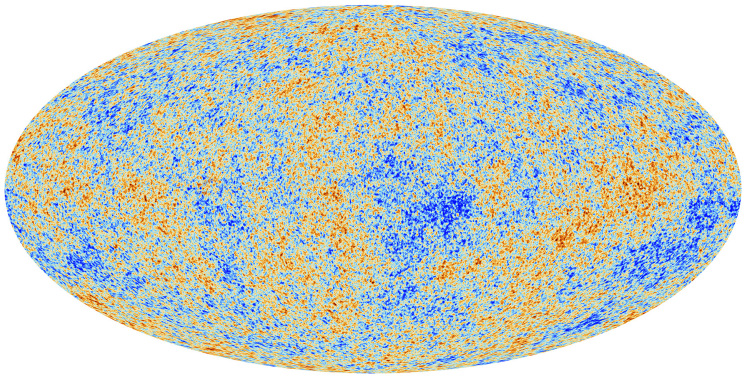

Figure 1.4: Temperature anisotropies map of the CMB as observed by Planck. Image credit: ESA and the Planck Collaboration.

The angular power spectrum of the thermal anisotropies in Figure 1.5 reveals important information about the cosmological parameters of the universe. The best fit of the Λ-CDM model is shown with the light blue line. The Λ-CDM is a cosmological model describing the evolution of the universe since the Big Bang, with parameters such as the cosmological constant Λ connected to the dark energy and the baryonic and the cold (referring to non-relativistic) dark matter (CDM) densities. The first peak is related to the curvature of the universe and the result is consistent with a flat universe. The second and third are associated to the baryonic and cold dark matter densities (Ω_{baryon}, Ω_{CDM}). The fit on the data of the most recent data of Planck [2], derives a universe that consists of:

$$\Omega_{baryon} \approx 4.9\%,\ \Omega_{CDM} \approx 26.2\%,\ \Omega_{\Lambda} \approx 68.9\%$$

where Ω_{Λ} is the proportion of dark energy in the universe. So, given this model, the dark matter is expected to be 5 times more abundant than ordinary matter.

[1]The series of papers published in 2018 can be reached in the official ESA website here.

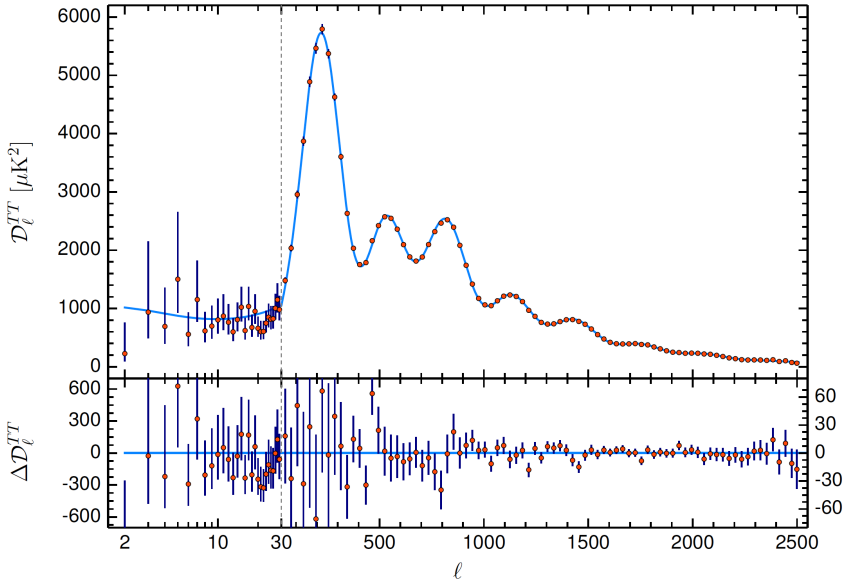

Figure 1.5: Planck 2018 temperature power spectrum (red points) with the a Λ-CDM model best fit (light blue line) (top plot) and the residuals of the data from the fit line (bottom plot). [2]

1.5 Dark matter candidates

The evidence for the existence of dark matter have been presented. Yet, the question of what is the nature of dark matter is not answered. There are several theories proposing candidates with various properties but one is common for all of them, dark matter must be massive. Additionally, numerical simulations of the structure formation in the early universe suggest that dark matter has to be non-relativistic at the epoch of structure formation, which is in agreement with the results of the Λ-CDM model fit on the CMB power spectrum. The rest of the properties rely on the different proposed models, some of which are presented below. The list here is, of course, incomplete as there has been a plethora of ideas in the last decades for the nature of the dark matter and the subject of this thesis is not primarily to inform on all of them.

1.5.1 (Primordial) Black holes as dark matter

Could black holes be dark matter? Black holes are the most massive objects in the universe absorbing anything that passes their event horizon, even light. So, first of all, the black holes are accounted as matter in the calculations that indicate a missing component. In addition, a black hole is composed of baryonic matter and from the CMB results for the Λ-CDM fit, the baryonic and dark matter are dissociated quantities. So, the black holes cannot be dark matter. Could then be the yet undiscovered Primordial Black Holes (PBHs)? The PBH is a hypothetical type of black holes that formed after the Big Bang, while common black holes are formed after the death of large stars. The PBH is one of the most massive candidates of dark matter, although it can be multiple orders of magnitude

lighter than ordinary black holes, depending on the model. Even if the PBH exists, there is no compelling evidence that it could replace the whole dark matter, but maybe only a fraction of it [38], in which case dark matter still remains a mystery.

1.5.2 (Sterile) Neutrinos as dark matter

In the form of particles, could SM neutrinos be dark matter? The *cold* dark matter refers to non-relativistic particles, while neutrinos have a velocity nearly the speed of light. They could be a potential candidate in the *Hot* dark matter scenario, which means that dark matter was created and still is relativistic. However, even though it was discovered that neutrinos have mass, it is simply too small to constitute the whole missing matter [39]. Could the as of yet undiscovered sterile neutrinos be dark matter? The sterile neutrinos are theoretically well-motivated, since SM neutrinos are only left-handed and all other known fermions have been discovered with both left- and right-handed chirality. They are electromagnetically neutral, but contrary to SM neutrinos, they do not interact weakly. That means they cannot interact with any other know particle, but only through gravity. Their mass is much higher than the SM neutrino, $\mathcal{O}$(keV), and although they were relativistic at their creation, they are not anymore, making them *Warm* dark matter candidates [39].

1.5.3 Weakly Interacting Massive Particles (WIMPs)

One of the most theoretically favoured dark matter candidates emerges naturally from the supersymmetric extension of the SM. The supersymmetric theory introduces a class of hypothetical Weakly Interacting Massive Particles, or WIMPs. The dominant candidate is the neutralino as the lightest supersymmetric particle. A WIMP's mass ranges in a very wide scale from GeV to TeV. WIMPs and SM particles are theoretically assumed to be created in the primordial universe in thermal equilibrium, with creation and annihilation from both sides. As the universe expanded, the temperature decreased and the WIMPs could no longer be created, only annihilate. After a certain period, the WIMP annihilation stopped ("freeze-out") and their density remained essentially constant until this day [40].

The WIMP is one of the most attractive candidates for direct detection experiments. The WIMPs can directly interact with the target material of the detector through elastic scattering with a nuclei, that will cause the atom to move in the lattice ionizing other atoms. This phenomenon is called nuclear recoil. The recoil energy deposited by a WIMP with mass $\mathcal{O}$(GeV) with a speed in the order of $10^{-3}c$, where c is the speed of light in vacuum, is expected to be $\mathcal{O}$(keV). The WIMP predictions depend strongly on several parameters depending on the interaction, such as the mass of the mediator of the interaction. The Migdal effect was been recently applied to the dark matter interactions [41], predicting an additional ionization channel through WIMP-nucleus scattering. The electrons of the recoiled nucleus may not follow the motion immediately and individual ones

can potentially be left behind which will lead to the ionization of the recoiling atom [42]. The Migdal effect increases the sensitivity of the detection of lighter WIMP candidates.

Since WIMP is one of the the dark matter candidates searched by the DAMIC experiment, it is worth mentioning the formula for the expected events rate of its scattering off nuclei of a detector's target for sufficiently high WIMP velocities v to produce a recoil with energy E [43]:

$$\frac{dR(E)}{dE} = \frac{\rho_0}{m_\chi \cdot m_A} \cdot \int v \cdot f(\mathbf{v}) \cdot \frac{d\sigma(E,v)}{dE}\, d^3v \tag{1.2}$$

where ρ_0 is the local dark matter density, with a benchmark value of $0.3\,\mathrm{GeV/cm^3}$ used [43], m_χ and m_A are the masses of the WIMP and the nucleus of the target material respectively, $f(\mathbf{v})$ is the distribution of velocity of the DM particles in the rest frame of the detector, described by an isotropic Maxwell-Boltzmann distribution, accounting for the average speed of the Solar system around the galactic center and the average orbital velocity of the Earth around the Sun, and $\frac{d\sigma}{dE}$ is the differential cross-section, which is developed as:

$$\frac{d\sigma}{dE} = \frac{m_A}{2\mu_A^2 \cdot v^2} \cdot (\sigma_0^{SI} \cdot F_{SI}^2(E) + \sigma_0^{SD} \cdot F_{SD}^2(E)) \tag{1.3}$$

where, μ_A is the WIMP-nucleus reduced mass, σ_0 and $F^2(E)$ are the cross-section at zero momentum transfer and the form factor correction for spin-independent (SI) and spin-dependent (SD) interactions. For a target atom with an even number of protons and neutrons, such as silicon[2], the expectation values of the nuclear spin operator is close to zero, thus $F_{SD}^2(E)$ is negligible, and:

$$\sigma_0^{SI} = \sigma_n \frac{\mu_A}{\mu_n} A^2$$

where μ_n is the WIMP-nucleon[3] reduced mass, A is the mass number of the target nucleus, and σ_n is the zero momentum transfer cross-section for a WIMP-nucleon scattering. In the formula 1.2 we can see the role of various physics scales playing in the direct detection of WIMPs:

- the astrophysical scale through the velocity distribution of dark matter in the galactic dark matter halo,
- the nuclear physics scale through the form factor describing the interaction of the WIMP with the nucleus,
- the particle physics term through the cross-section describing the scattering of the WIMP off the nucleon.

[2] ${}^{28}_{14}\mathrm{Si}$ has an abundance of 92.23% among the stable (3) isotopes of Si

[3] the nucleon is the common description of the proton and the neutron as an isospin doublet with which the WIMP interacts.

1.5.4 Hidden/Dark sector

Hidden sector particles are supposed to interact with the SM matter only gravitationally, making their direct detection quite difficult. It is hypothesized that a similar to the visible photon that belongs to the hidden sector may exist, called *hidden* or *dark photon* [44]. Like the visible photon, the hidden photon is supposed to be a gauge boson of a U(1) group. This allows the kinetic mixing of the two, which can be a potential portal for the detection of the hidden photon. Unlike the visible one, the hidden photon may be massive. The discovery of a hidden photon can open the door to a whole new hidden sector or it could be the only particle of it, in which case it must be massive.

The formula of the expected event rates of hidden sector candidates scattering off bound electrons in the detector's target atoms is given by the formula [45]:

$$\frac{dR}{dE_{ee}} = N_T \frac{\rho_0}{m_\chi} \sum_{n,l} \frac{d\langle \sigma^{nl}_{ion} \cdot v \rangle}{dE_{ee}} \tag{1.4}$$

where N_T is the number density of atoms in the target and the only difference with the differential cross-section with respect to the WIMP case is that the DM particle here will scatter coherently off the electronic orbitals (described by the quantum numbers n and l).

The absorption rate of the hidden photon as a massive non-relativistic particle with rest mass $m_{A'}$ is given by [45]:

$$R = -\frac{1}{\rho_T} \frac{\rho_0}{m_{A'}} \epsilon^2_{eff} \frac{\mathrm{Im}\Pi(m_{A'})}{m_{A'}} \tag{1.5}$$

where ρ_T is the density of the target material, ϵ^2_{eff} is the effective mixing parameter which is the mixing parameter inside a dielectric target medium, and $\mathrm{Im}\Pi(m_{A'})$ is the imaginary part of the polarization tensor of the target describing in-medium dispersion effects dependent on the mass of the hidden photon.

1.5.5 Axion

The CP-symmetry (C: charge, P: parity) states that the laws of physics remain intact if a particle is exchanged with its antiparticle and its spatial properties are mirrored, and was considered absolute until 1964 [46]. The hypothetical axion particle was initially introduced by Roberto Peccei and Helen Quinn in 1977 [47] as a solution to the strong CP problem, the lack of observation of the expected violation of the CP-symmetry [40, 48]. The axion is theorized to be non-relativistic and is a well motivated CDM candidate, with a mass below the eV scale. Although it is expected to interact electromagnetically, due to its very low mass it could have easily dodged detection until today.

1.6 Dark matter detection approaches

There are 3 experimental approaches to discover the true nature of the dark matter (DM): by production, indirectly and directly.

1.6.1 Production

In the case of production, the methodology is using ordinary matter to produce dark matter. Colliding accelerated SM particles increase the center of mass energy and allows the production of heavier particles than the reactants.

$$SM + SM \longrightarrow DM$$

Currently, the Large Hadron Collider (LHC) of CERN is the highest energy particle accelerator in the world with a maximum center of mass energy of 13 TeV. The various experiments/detectors of the LHC can reconstruct the products of a collision with a certain coverage and resolution. In each collision, it is possible to estimate the missing transverse energy. The total initial and final transverse momentum as considered equal to zero. Any imbalance between of the detected energy in the transverse direction indicates missing energy. The total missing energy cannot be calculated, as the initial momentum of the colliding particles along the beam axis is unknown. Components of the missing energy can be neutrinos or any other particles that escaped detection, including potentially dark matter. As a result, LHC experiments can place limits for dark matter candidates that may be created with a mass related to the missing energy [49]. The lack of detection of any resonance has led the search of dark matter to follow other approaches.

1.6.2 Indirect search

The indirect approach searches for anomalies in the flux of photons, neutrinos, and cosmic rays that are related to dark matter particles decay to SM particles [50]. Neutrino experiments, such as IceCube [51] and ANTARES [52], although not particularly specifically to dark matter, search for neutrino fluxes from the galactic center or the sun as dark matter decay products. Another important running experiment is the Alpha Magnetic Spectrometer (AMS). The AMS-02 [53] was installed on the international space station in 2011 and is a multitask module featuring several detecting capabilities with a transition radiation detector, a Cherenkov detector, and an electromagnetic calorimeter among others. Its purpose is the measurement of cosmic particle flux and with a magnetic field of 0.15 T in its tracker is able to identify the sign of the electric charge separating particles from antiparticles. A detected excess of positrons, also observed previously by the PAMELA experiment [54], could potentially be associated with dark matter annihilation.

1.6.3 Direct search

Indicated by the title, the third approach for searching for dark matter is the attempt to directly observe dark matter interactions with ordinary matter.

$$SM \; + \; DM \; \longrightarrow \; SM \; + \; DM$$

This section will be more extended than the previous two as it includes the DAMIC experiment and is important to present the different techniques and methods that are used by several experiments of this category. The common goal for every experiment here is the measurement of the result of the dark matter interaction in a detector, usually as energy deposition in the form of phonon, light from scintillation or charge through ionization in the active medium. To suppress the cosmic ray induced background, the direct experiments are located below large volumes of mass, in underground laboratories.

Cryogenic detectors: CDMS, EDELWEISS, CRESST

A bolometer device measures the heat (phonons) produced in a semiconductor from an incident particle. It utilizes semiconductor crystals, such as germanium or silicon, which are cooled at a very low temperature, in the order of 10 mK above absolute zero. This allows for very precise measurements of the energy deposited in the crystal from an incident particle through nuclear recoil. An array of several bolometers is usually commissioned to increase the total target mass of the experiment. Bolometers are preferred for light dark matter-nucleon scattering search (below $10\,\mathrm{GeV/c^2}$), due to their great energy resolution and low energy threshold down to the eV scale. Recent results for such detectors are presented in Figure 1.6 from CDMSlite-Soudan [55] and EDELWEISS-III [56]. The CRESST-III detector [57] combines an additional measurement of scintillation light signal in its crystal which strongly depends on the particle interaction and can lead to discrimination between background (β/γ interactions) and nuclear recoils.

Charge Coupled Devices (CCDs): DAMIC, SENSEI

The advancements in the CCD technology have reached to detectors with exquisite low noise and high readout resolution, built with radiopure materials, allowing for applications in rare event searches, such as dark matter. The DAMIC collaboration [58] has pioneered in this field and the SENSEI [59] adopted the same approach. They both provide competitive limits in the low mass dark matter-nucleon scattering and completely dominate the low mass dark matter-electron scattering and the hidden photon search. Contrary to the cryogenic detectors, they operate at temperatures $\sim$100 K allowing for the detection of the ionization of atoms. Future upgrades of both are on the way. The CCD is the protagonist of this thesis and is described extensively in the following chapter.

Liquid TPCs: XENON, LUX, PandaX, DarkSide

Other detectors operate with liquid noble gases target mass, such as liquid Xenon (XENON1T [60, 45], LUX [61], PandaX-II [62]) or Argon (DarkSide-50 [63]), in large dual-phase Time Projection Chambers (TPCs). A TPC is a cylindrical chamber with an applied electric field between its two ends. An incident particle that interacts with the active material produces light from scintillation and charge through ionization. The light and charge are read by photo-multipliers on both ends of the TPC and from their time difference the depth of the event can be calculated, leading to 3D reconstruction of the position of the event. In addition, the ratio of the two signals allows for great separation between electron and nuclear recoils. Contrarily to solid state detectors, liquid Xenon or Argon can be treated in much larger quantities. Most modern TPCs utilize large amounts of liquid in the order of 1 t, giving them a great advantage in terms of cross-section interaction with dark matter. The detectors of this category are sensitive to heavy dark matter candidates in the mass range of $\sim$10-10^3 GeV/c^2.

Gaseous chambers: NEWS-G

NEWS-G [64] is a direct detection experiment using Spherical Proportional Counters (SPCs) filled with noble gas mixtures at a higher than atmospheric pressure, for the search of low-mass WIMPs through nucleon scattering. Energy deposition from an incident particle can produce primary ionizations in the gas. These primary electrons will drift towards an anode at the center of the sphere and close to it the electrons will gain enough kinetic energy to create secondary ionizations. The SPCs can achieve great sensitivity of the primary ionizations and a low energy threshold of $\mathcal{O}(10\,\mathrm{eV}_{ee})$ (electron equivalent recoil energy).

Axion Solar Telescope: CAST

The CERN Axion Solar Telescope (CAST) is an experiment dedicated to the search of axions. The method used here is quite different than the previously described experiments. Axions may be produced in the core of hot stars, like the Sun. The CAST uses a 9 T refurbished LHC test magnet directed to the Sun. Solar axions can be converted into X-rays in this strong magnetic field which are then recorded by X-ray detectors. The last run of CAST has provided constraints of the axion-photon coupling strength ($g_{\alpha\gamma}$) for an axion mass up to $\sim$0.02 eV/c^2 [65]. The International Axion Observatory (IAXO), successor of CAST, is the next generation helioscope that will extend further the search for solar axions and other axion-like particles (ALPs) with an expected signal to background ratio higher by 5 orders of magnitude [66].

Current limits and results

There are various plots that present the current exclusion limits for different dark matter candidates, interactions and detection approaches. The exclusion limits of the spin-independent dark matter-nucleon cross-section are presented in Figure 1.6. There are several experiments of no less importance, but this plot is meant to be representative of the current dominant limits rather than a complete review. The dark matter-electron cross-section for a heavy and an ultralight mediator are presented in Figure 1.7 left and right respectively, and the constraints on the dark photon dark matter absorption in Figure 1.8 [67].

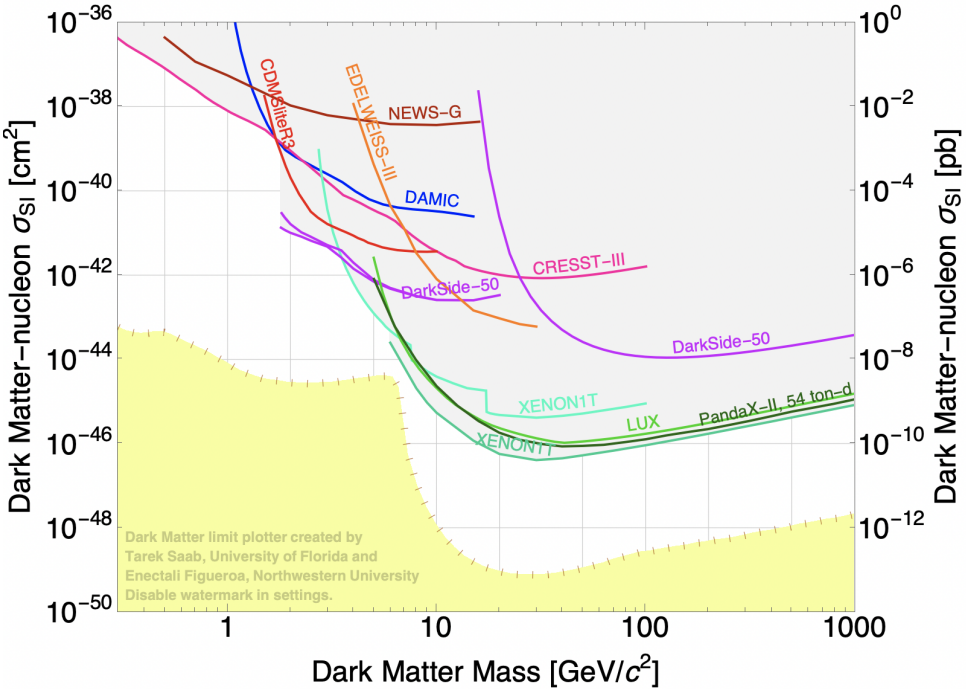

Figure 1.6: Dominant exclusion limits of spin-independent WIMP-nucleon cross-section as a function of the WIMP mass. All Nuclear Recoil limits are scaled to a local dark matter density of $0.3\,\mathrm{GeV/c^3}$. The *Dark Matter Limit Plotter* application was used to produce this plot. The source of each experimental limit: DAMIC (blue) [68], NEWS-G (brown) [64], CDMSliteR3 (red) [55], EDELWEISS-III (orange) [56], CRESST-III (pink) [57], DarkSide-50 (purple) [63], XENON1T (light aquamarine, dark aquamarine) [60, 45], LUX (light green) [61], PandaX-II (dark green) [62].

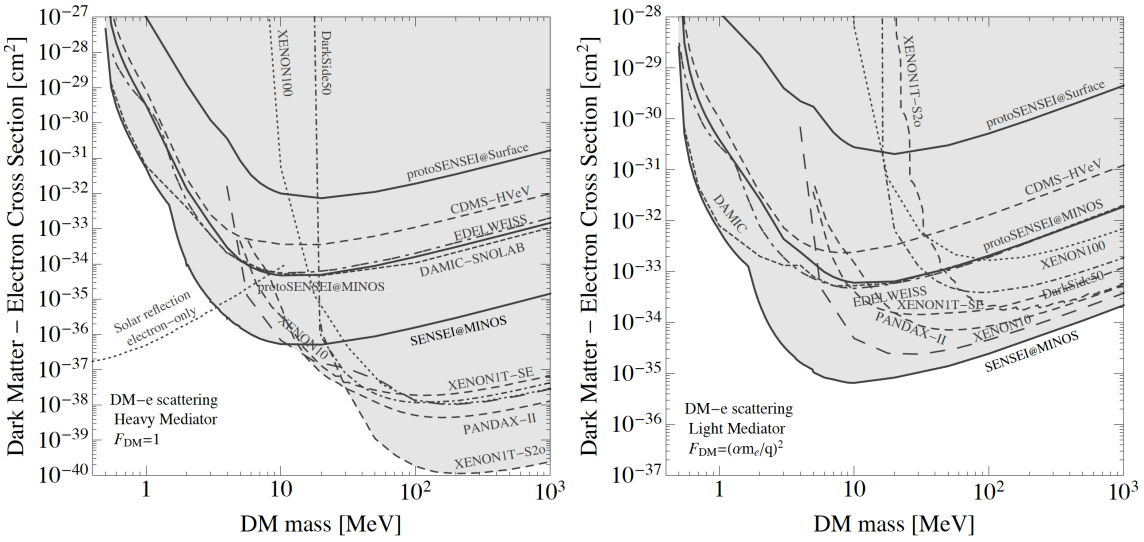

Figure 1.7: Current 90% c.l. limits on DM-electron scattering through a heavy (left) and an ultralight (right) mediator [67].

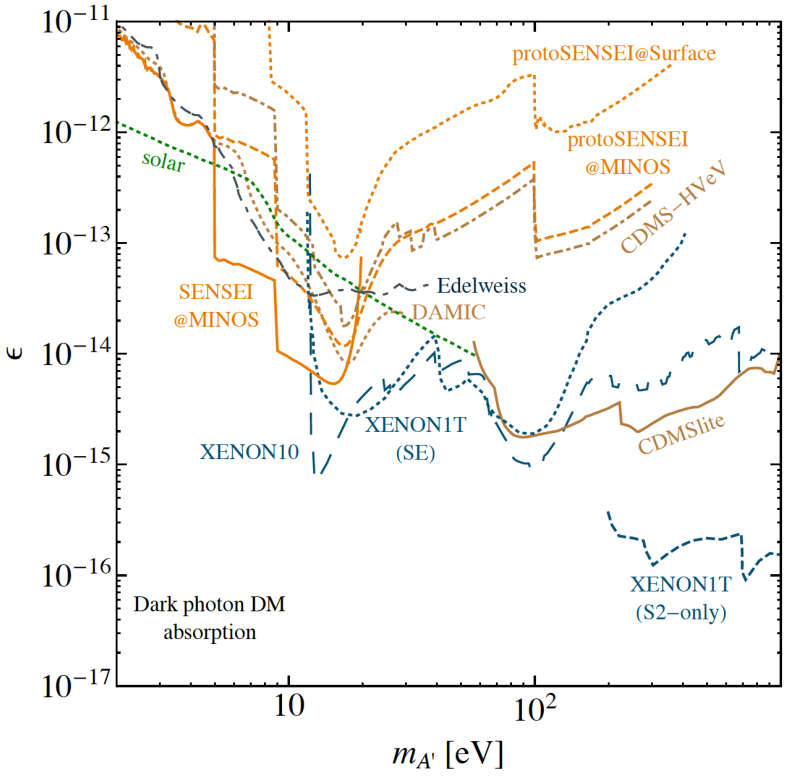

Figure 1.8: Constraints on dark photon dark matter absorption [67].

Chapter 2

Charge Coupled Device

The Charge-Coupled Device, or CCD, was invented in 1969 by Willard S. Boyle and George E. Smith at Bell Telephone Laboratories. The two inventors were awarded with a Nobel price in 2009, among others. A CCD is a semiconductor-based imaging detector. It consists of an array of pixels, with a fixed number of gates at the top surface of each. The applied clock signals through the gates, also called phases, and a bias substrate voltage on the bottom create an electric field in the pixel, that allows the induced charge collection. The pixel can hold the charge until it is transferred to a readout circuit to be measured. A simple analogy of its operation is the bucket brigade, as is shown in Figure 2.1.

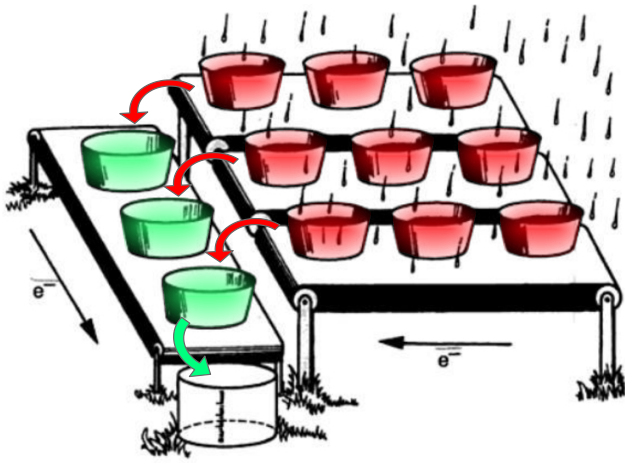

Figure 2.1: Bucket brigade equivalent of a CCD operation. [69]

The red buckets are collecting the rain water during the exposure phase. After the rain, to measure the water in every bucket, the red buckets transfer the water to the green ones line-by-line (red arrows), and they in their turn bucket-by-bucket to a measuring instrument (green arrow). After recording the measurement, the water is no more useful or interesting and must be dumped. In a system like this, one can measure the water of a large array of buckets, always knowing the initial position of the bucket. The respective steps of a CCD operation will be discussed extensively in the following sections: Charge Generation, Charge Collection, Charge Transfer and Charge Measurement.

2.1 CCD structure

In this subsection, I will describe a CCD architecture based on the patent of Steven Holland (2001) [70], similar to what the DAMIC-M experiment will employ. I will mention several applied techniques that were developed through time to improve various CCD characteristics.

It all starts with the production of a pure monocrystalline silicon ingot with a diameter up to a few tens of centimetres. For the reference, the main steps of producing a silicon ingot with the Czochralski method are shown in Figure 2.2 left. The ingot is then cut in thin disks from 10 μm to 1 mm, called wafers (see Figure 2.2 right). Silicon

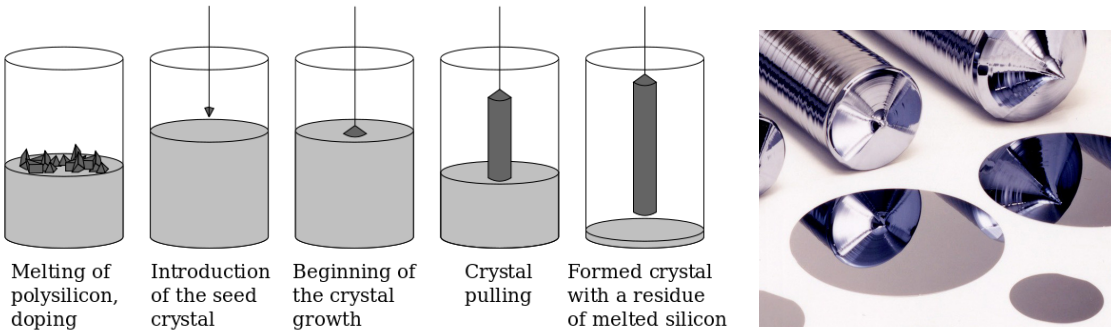

Figure 2.2: Left: Main steps of Czochralski method producing silicon ingot. [71] Right: Sumco's silicon ingots and wafers.

is a semiconductor which defines its electrical properties to fall between a conductor, like copper, and an insulator, such as glass. The CCDs are almost exclusively made of Silicon, which is a common and relatively cheap material, even though other semiconductor CCDs exist, made of Germanium or Gallium Arsenide [72, 73]. Each semiconductor atom has four outer (valence) electrons and in a "perfectly" pure crystal every two atoms form a covalent bond, resulting to a non-conductive material (at room temperature) due to the lack of free charge carriers. Introducing small quantities of atoms with one less (three) or one more (five) outer electrons as impurities, could drastically change the conductivity of the crystal. This process is called doping. The amount of the dopant atoms define the electrical resistivity of the semiconductor. Boron, Aluminum, Gallium, Indium and Phosphorus, Arsenic, Bismuth atoms are usually used as *acceptors* and *donors* respectively. A dopant atom which acts as acceptor will form a *p-type* semiconductor with electron holes$^+$ (or just holes) as free charge carriers. A dopant atom which acts as donor will form an *n-type* semiconductor with electrons$^-$ as free charge carriers.

For the sake of this example and similarly to the type of CCDs used by the DAMIC collaboration, the silicon bulk is doped with donor atoms, thus n-type CCDs. A much thinner layer at the top of the silicon is doped with acceptors as p-type silicon, called buried channel. The thicker region of the n-type silicon beneath the buried channel, is called substrate silicon.

This silicon structure is then separated in strips with linear spacers, or channel stops. The channel stops are n-type electrically floating silicon implanted deep, deeper than the buried-channel, reaching the substrate silicon [70]. They act as an insulator preventing the collected charges to diffuse among the strips. The distance between two successive channel stops defines one of the physical dimensions of the pixel size.

Top side

On the top surface of the silicon plate and perpendicular to the strips, a repeating pattern of N electrodes/gates are fabricated. In the early years, aluminum gates were used, but later were replaced by polycrystalline-silicon gates, which are much less conductive and so the interelectrode short became less catastrophic [74]. A thin layer of gate insulator, such as SiO_2 or Si_3N_4 or even more than one layers of them combined, is placed between the gates and the buried channel. The gates themselves are usually electrically isolated by SiO_2. Commonly, the CCD architecture is based on a 3-phase technology, which means that there are 3 individual clock signal sources, or simply clocks, but 2- or 4-phase technology also exist. The repeating pattern of these 3 gates defines a single pixel. The cross section of the pixel geometry can be seen in Figure 2.3. The longitudinal size of the pixels is defined by the distance of two successive gates of the same phase.

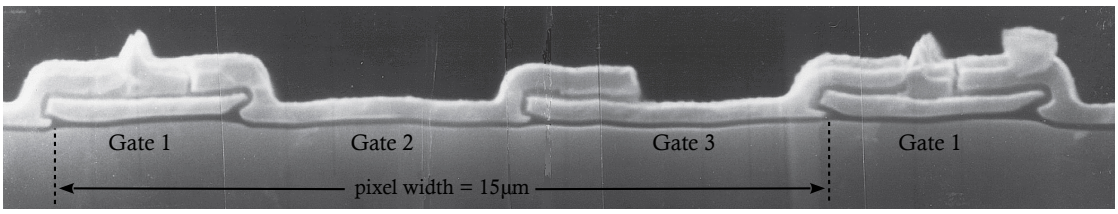

Figure 2.3: Scanning electron microscope cross-section image of CCD pixel gates. [74]

Each of the pixel-gates corresponds to an individual clock. The gates are connected to the perpendicular main electrodes located at some side of the CCD. The clock signals are provided to the CCD by external electronics with soldered wires on pads on the silicon (see Figure 2.4). A clock is an alternating signal between a high and a low levels, called rails. The sequencing of the clocks defines the precise periods of which clock rests at which state (low or high). The CCD can break down into 3 regions: parallel or vertical register, serial or horizontal register, and the output amplifier. All the individual clocks, similarly to the regions of the CCD, can be grouped in 3 categories: parallel or vertical clocks, serial or horizontal clocks, and readout clocks respectively. The vertical and horizontal gates are perpendicular extensions from the main electrodes labeled as V1, V2, V3, TG on the left image and H1, H2, H3 on the right one of Figure 2.4 respectively. Surrounding the active region, grounded p+ guard rings are formed on the frontside, to collect leakage current generated outside the active volume of the CCD.

Bottom side

On the backside of the silicon, a gettering layer can be fabricated [75]. The gettering techniques have been developed to counteract the presence of harmful impurities in the

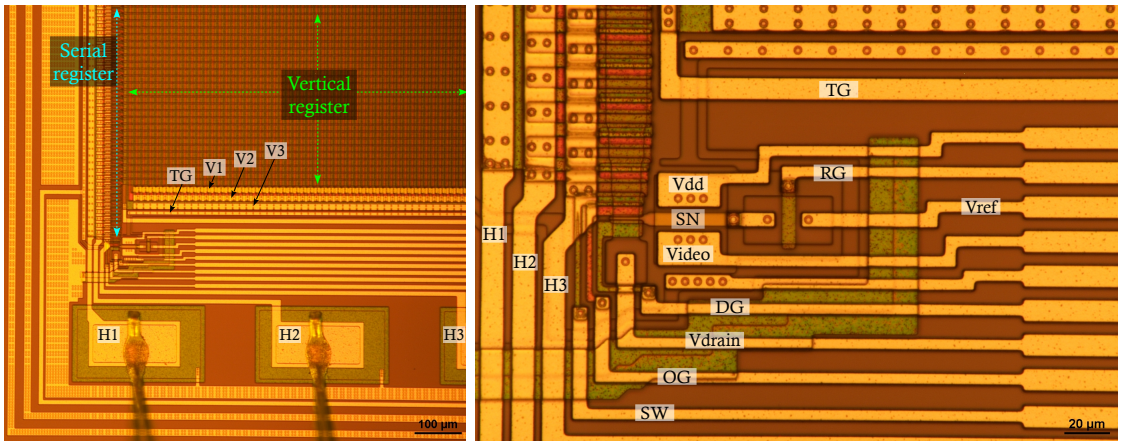

Figure 2.4: Photos of a DAMIC CCD with a zoomed shot on one of the readout amplifiers.

active volume of the device. About 1 μm of in-situ doped polysilicon (ISDP) is deposited on the back side of the wafer. For n-type substrate silicon, the gettering layer is heavily doped with phosphorus (P+). This n^+ layer serves both as the gettering layer and as the backside contact. Its gettering properties are due to the presence of both the polysilicon and the phosphorus. Polysilicon consists of small grains of single crystal material separated by highly disordered regions called grain boundaries. These grain boundaries act as impurity sinks and as a result polysilicon itself is an efficient gettering material. In addition, phosphorus also getters impurities by an ion-pairing mechanism and the combination of both methods has been shown to yield synergistic results [75]. After the deposition of the gettering layer, the backside is capped by a Si_3N_4 layer in order to be protected from additional particles that are added during the remainder of the fabrication. As shown in [75], the leakage-current in a CCD with a gettering layer is reduced by at least two orders of magnitude compared to a non-gettered. In both cases, the leakage current is quite stable for an applied substrate bias voltage above a certain value.

As mentioned in the previous paragraph, the ISDP layer can serve as an n+ electrical contact to provide the *substrate bias voltage*, or V_{sub}. In the case of the absence of this particular layer for gettering purposes, since it is optional, another ohmic contact made of any other electrically conducting material should be formed at the bottom of the CCD. In general, its thickness must be from 10 nm to 1 μm and must be transparent for backside illumination imaging applications. Even though possible, a direct physical connection of V_{sub} on the backside can bring several issues in keeping the uniformity of the backside layers [70]. Instead, the contact of the V_{sub} is actually located on the frontside plane, outside of the guard rings, as a single pad or a ring around the active region of the CCD. Several floating p+ guard rings are formed on the frontside between the grounded guard ring and the V_{sub} contact to drop the voltage from V_{sub} to the ground in well-controlled steps [70].

Another optional implementation is the anti-reflection layer below the substrate plane for backside illuminated CCDs. This again applies to CCDs for imaging applications, to

improve the detection efficiency. The anti-reflection layer may also be conducting, like Indium Tin Oxide (ITO). Finally, an insulator layer made of SiO_2, Si_3N_4 or other is deposited to protect the backside from additional particles that are added during the rest of the processing [76].

2.2 Charge Generation

This section concerns mainly the energy deposition of an incident particle, but also charge generation due to other, possibly unwanted, processes. CCDs started and are still mostly used as imaging sensors, today finding application in large telescopes for astrophysical purposes. This means that the incoming particle flux is photons, mostly in the visible spectrum. So, it would only be reasonable to open this discussion with points related to photogenerated signals.

When the CCD is exposed (*exposure phase*), a photon enters the detector and interacts with the silicon bulk producing electron-hole pairs. The silicon band gap energy[1] is ∼1.1 eV, with an average single electron-hole pair production energy at ∼3.65 eV (at room temperature) [77]. Figure 2.5 based on a Monte Carlo simulation study [78], shows that the silicon pair creation energy slightly increases as the temperature goes down.

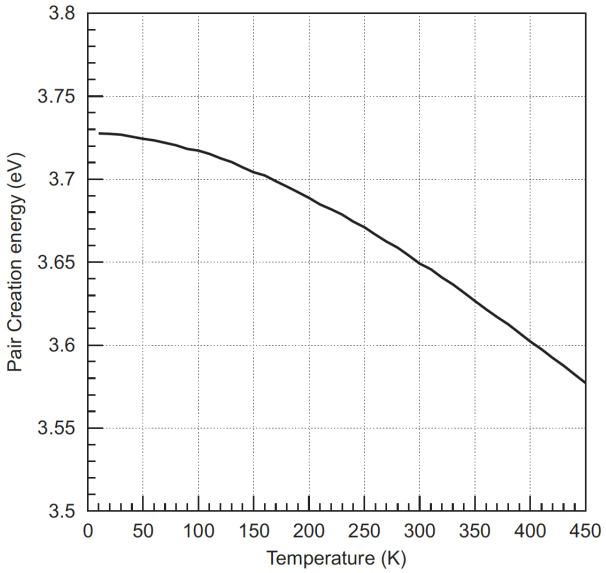

Figure 2.5: Electron–hole pair creation energy in silicon as a function of the temperature for 5.9 keV incident photons. [78]

A major CCD characteristic is the quantum efficiency (QE), which describes the ability of the silicon to produce electrons from incident photons. It is defined as [77]:

$$QE = \eta_I \cdot QE_I = \eta_I \frac{P_I}{P} \tag{2.1}$$

where η_I is the quantum yield, QE_I is the interacting QE equal to the fraction of the

[1]The band gap is the energy difference between the conduction band and the valence band.

average number of interacting photons per pixel (P_I) over the average number of incoming photons per pixel (P). The quantum yield for interacting photon energies above 10 eV is given by the relation [77]:

$$\eta_I = \frac{h\nu}{E_{e-h}} = \frac{12390}{E_{e-h}\lambda} \tag{2.2}$$

where E_{e-h} is the energy required to generate an electron-hole pair in eV and λ is the photon wavelength in nm. For photon energies higher than 3.65 eV (or a wavelength below $\sim$400 μm), the quantum yield starts to getting greater than 1. An incident photon with energy higher than 3.65 eV will produce an energetic electron which will collide with other silicon atoms and create multiple electron-hole pairs. The QE_I is measured for each CCD as a percentage and depends on the silicon reflection coefficient factor, the thickness of silicon, and the silicon photon absorption length. The reflection can be handled by backside illumination (next subsection) and application of anti-reflecting coatings.

In p-type substrate silicon CCDs, the backside surface develops a potential that attracts and traps the generated electrons [79]. As a result, the QE of such a CCD is low and drops further as the temperature is lowered. In n-type substrate silicon CCDs, where the charge carrier is the hole, the trapped electrons at the backside are not a problem. Thus, the QE is better and stable at different operating temperatures.

Frontside vs backside illumination

In order to capture an image, the CCD can be placed in an orientation to receive the photons from its front or back side. It was shown that CCDs that are illuminated at the frontside have poor quantum efficiency, especially in the blue region of the visible light spectrum, due to the strong absorption and reflection of photons in the polysilicon gates [80]. Back-illumination has the advantage of receiving the photons directly to the silicon bulk of the device. As mentioned earlier, the bottom side substrate contact can be quite thin and transparent and additionally, anti-reflecting coatings can also be applied. Nevertheless, the substrate silicon must be thinned from the backside to avoid high charge diffusion. A comparison of the quantum efficiency for frontside and backside illuminated CCDs is presented in Figure 2.6.

Thick CCDs

A typical thinned low-resistivity in the order of $\mathcal{O}(10\,\Omega\cdot\text{cm})$ CCD could be a few tens of μm thick [81]. For long-wavelength photons in the visible spectrum (red), this thickness becomes comparable to the absorption length in silicon, which lowers the quantum efficiency for these wavelengths. These photons can penetrate the silicon without interacting and reach the frontside, where they can pass through it or be reflected, leading to *fringing*. A CCD thickness in the order of a few 100 μm improves the absorption of photons, especially near red and infrared, but needs a high substrate voltage application to maintain a good spacial resolution, which can only be applied in high-resistivity silicon (see next section).

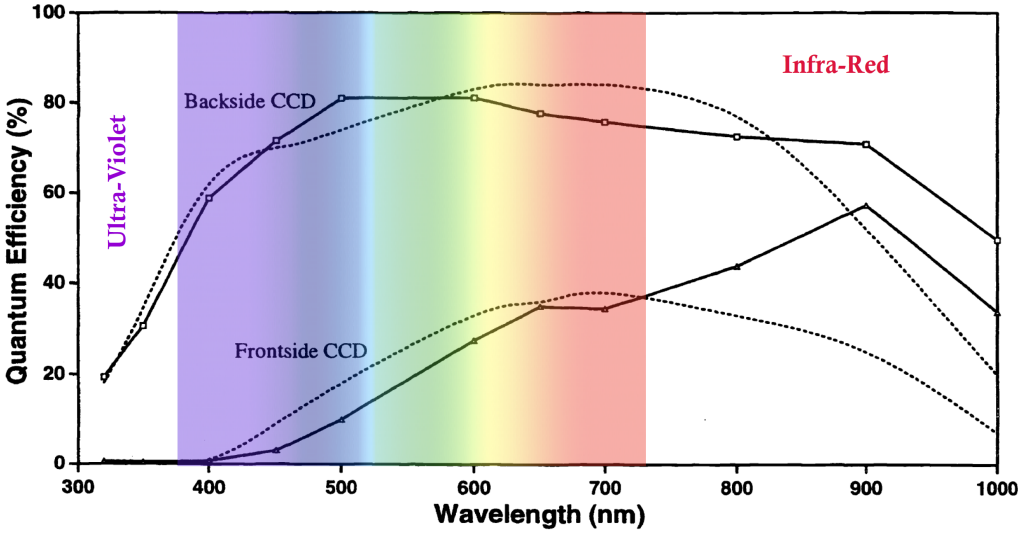

Figure 2.6: An example of interacting quantum efficiency measurements for frontside and backside illuminated CCDs. Solid lines with points represent the measured values and dotted lines illustrate typical low-resistivity commercial CCD quantum efficiency. [81]

2.3 Charge Collection

In the n-type substrate silicon there are plenty free electrons. A positive applied substrate bias voltage attracts these electrons, depleting the silicon from any free carriers. Similarly, the electrons of the electron-hole pair creation will be directed to the substrate plate by the electric field, where they will travel to the frontside contact and finally be drained by the V_{sub} source. The holes will drift towards the gates to be collected. Specifically, during the exposure phase, the gates rest at fixed potentials; usually one of the three (could also be two) is at a lower value. This will create an electric field that will force the holes to drift under the lowest potential. The other two gates rest at a higher voltage and act as barriers. The potential distribution presents a minimum which is where the charges are collected, called *potential well*). Once the charge is collected at the potential well, it cannot spread to other pixels because of the gate-barriers in the one direction and the channel-stops in the other.

Potential well

A simulation of the potential well during the exposure phase is shown in Figure 2.7 [80]. The CCD pixel considered here is 300 μm-thick, high-resistivity, p-channel with an area of $(15\,\mu\text{m})^2$. The substrate doping is $6{\cdot}10^{11}\,\text{cm}^{-3}$ (corresponding to a resistivity of about $7\,\text{k}\Omega{\cdot}\,\text{cm}$) and the buried-channel implant dose is $1.5{\cdot}10^{12}\,\text{cm}^{-2}$. The collecting gate (blue) is at -5 V and the barrier gates (green and red) at +5 V. The substrate bias voltage generates a drift field that extends to the backside contact (y-axis). The potential minimum is located in the buried channel silicon area. This is the goal of the buried channel all along. Its presence allows the potential well minimum to be a bit further than the silicon-SiO_2 interface [82, 74].

In the case of a surface channel CCD, i.e. without a buried channel, the potential well

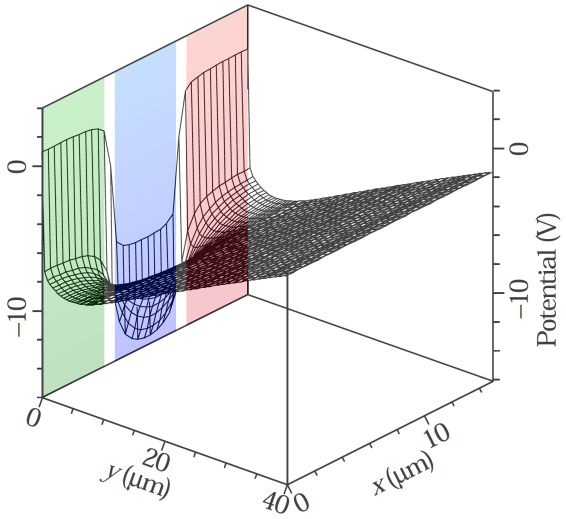

Figure 2.7: Simulated potential distribution for a 15 μm pixel. The substrate doping is $6{\cdot}10^{11}\,\mathrm{cm}^{-3}$ and the buried-channel implant dose is $1.5{\cdot}10^{12}\,\mathrm{cm}^{-2}$ [80]. The green, blue, red stripes represent the 3 individual gates of the pixel, where the charge is collected under the blue while green and red act like barriers.

is minimum at the polysilicon gate surface and drops with the squared distance from the gate, as it is shown in Figure 2.8 left. In such a CCD, the charge-packets are collected close to the silicon-SiO_2 interface [74]. Atomic mismatch at the silicon-SiO_2 interface causes unpaired silicon electrons describes as "dangling bonds" [83]. This allows the generation of trapped holes as interface states that decay in time and affect the collected pixel charge like a residual image [82]. Traps can also appear as bulk states due to imperfections in the silicon, possibly caused by radiation damage [84]. The interface states are a function of area, while the bulk states are a function of volume. Figure 2.8 shows the potential well shape in a CCD pixel with and without a buried channel.

Thermally generated charge in the CCD that does not occur due to incident particles, such as interface or bulk states, is called *intrinsic dark current*, or often referred as dark current [85]. It depends on the temperature and the number of holes collected for a given time follows a Poisson distribution. The accumulation of these traps lowers the resolution of the CCD. Low energy events that cannot be separated from the dark current are lost.

Gate inversion

Another technique to lower the interface charge collection is to operate the collecting gate at *inverted state*. A qualitative visualisation of the potential well for different values of the collecting gate potential (V_G) for a CCD with buried-channel is shown in Figure 2.8 right. Starting from the gate surface, the shape of the potential well for a V_G lower than the V_{sub} will start decreasing in the SiO_2 area and will continue until it reaches a minimum inside the buried channel, which is the preferred area for the holes to collect. As it goes deeper in the CCD it will start increasing until it reaches the applied voltage on the substrate plane, V_{sub}.

The V_G can also be higher than the V_{sub}. The critical V_{INV} is the value of the

V_G where the potential at the silicon-SiO_2 interface is equal to V_{sub}. For $V_G \geq V_{INV}$, the interface potential becomes attractive to the electrons of the floating n-type channels stops. Hence, the electrons will flow at the interface preventing the interface potential to go higher than V_{sub}. The potential well is not influenced by the voltage gate in this state, because the thin layer of electrons that accumulate at the interface is conductive and shields the area beneath it, so the potential well at the interface is fixed for any $V_G \geq V_{INV}$ and is considered *pinned* (see dashed line of Figure 2.8). This results to very low dark current caused by the interface states [74, 86]. This technique however makes the CCD vulnerable to spurious charge generation, an important clock induced noise source that will be discussed in the next section. For the reference, non-inverted clocking implies that neither the barrier or the collecting gates are inverted, partially inverted clocking is when the barrier gates are inverted, and inverted clocking is when all gates, barrier and collecting, are inverted.

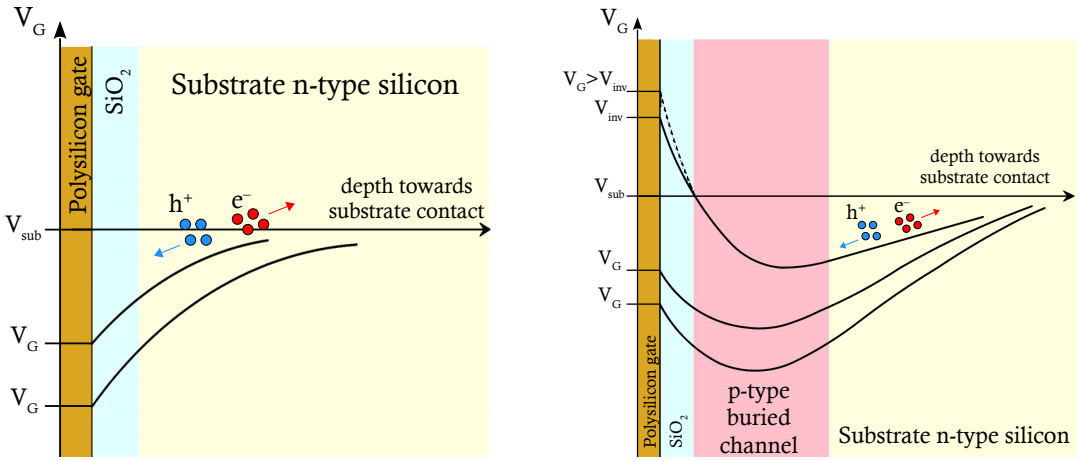

Figure 2.8: Potential well shape under the collecting gate for a CCD without (left) and with (right) a buried-channel.

Diffusion and Point Spread Function

During their transition to the potential well, the charge carriers spread laterally. This spread is described by the *Point Spread Function* (PSF) [87]. When the V_{sub} is not high enough, the silicon will present an undepleted area. In such a region, there is no electric field or it is not strong enough (field-free) to drive the charges and so they will diffuse in random directions. The ones that will be directed towards the gates will eventually meet the potential well and will be collected but highly diffused. The rest that will follow an opposite direction will be lost. The necessity for thick CCDs for higher QE warns of a large field-free space for the charge to diffuse. In order to minimize these regions that can deteriorate the spatial resolution of the device, one needs to apply a sufficiently high enough substrate bias voltage (V_{sub}). The substrate voltage needed for *full depletion* depends on the substrate silicon doping and the square of the substrate silicon width [76]. Highly doped silicon (low resistivity) thick devices cannot support high electric fields. Therefore, high-resistivity silicon ($>1\,k\Omega\,cm$), in which the break down voltage is high,

started being used to build thick and fully depleted CCDs.

An example of a 500 μm thick CCD fabricated on ~20 kΩ·cm silicon is shown in Figure 2.9 [76]. The two images were acquired after a 30 minute exposure in dark conditions. On the left, the image was taken at a substrate voltage of 30 V. The CCD is not fully depleted as can be seen from the spatial blooming on the tails of the background cosmic ray and radiation events. The diffusion is clear in the long-line tracks, possibly by muons that cross the CCD without stopping. On the one end they look fine, indicating that the charge was created by the particle close to the front-side. As the line extends, the width of the track grows, until the other end where the particle reaches closer to the bottom of the detector where the electric field is not strong. These highly diffused tracks are absent on the right image, where the substrate voltage is at 60 V, implying full depletion [87]. Figure 2.10 shows the PSF as a function of the substrate bias voltage for a high-resistivity 200 μm thick CCD. One can notice that the x-axis extends up to 120 V, but other CCDs have been designed for even higher voltages, above 200 V.

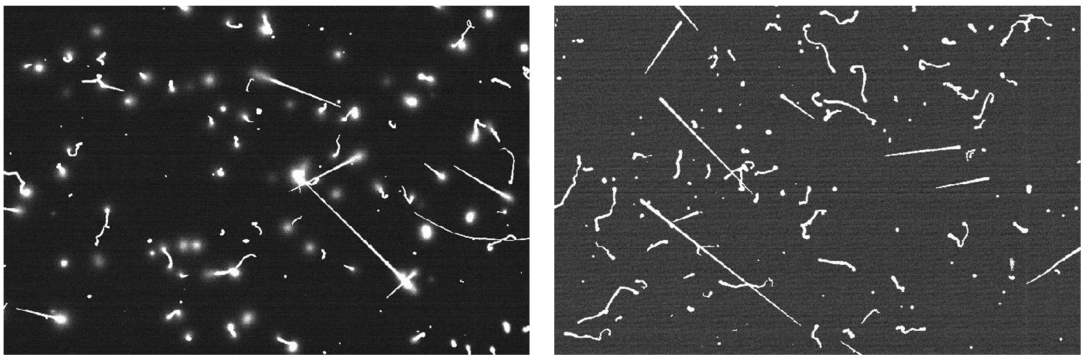

Figure 2.9: Images of 30 min dark exposures taken at -140 C on a 500 μm-thick, 4k $\times$ 2k, $(15\,\mu\text{m})^2$-pixel CCD fabricated on ~20 kΩ·cm silicon. The size of the sub-image is approximately 650 rows by 770 columns. Left: $V_{sub} = 30$ V. Right: $V_{sub} = 60$ V. [76]

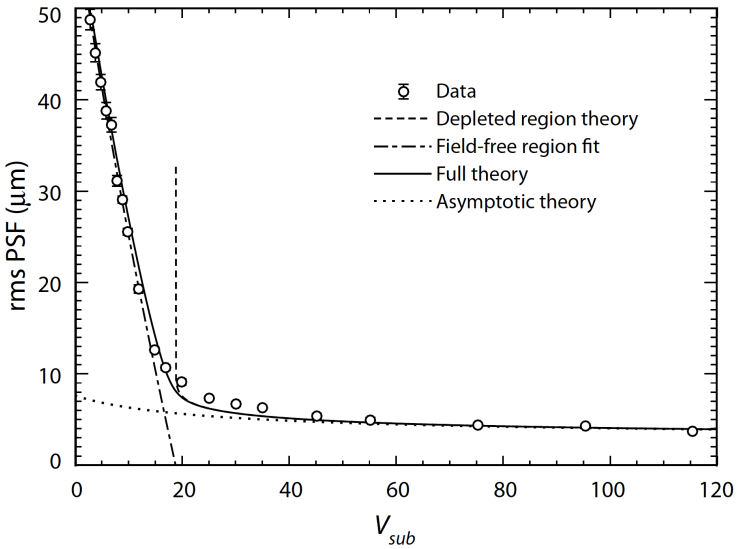

Figure 2.10: Measured rms diffusion (PSF) as a function of V_{sub} for a CCD with 3512^2 pixels of $(10.5\,\mu\text{m})^2$ area and 200 μm thick. [87]

The potential well also defines the capacity of the pixel in terms of charges. The full-well capacity is the maximum number of electrons a pixel can hold [88]. It depends on the pixel size and structure. Pixel capacity is a function of area, so bigger pixels usually hold more charge. If a pixel is saturated with charge, the additional generated charge will spill to neighbor pixels.

2.4 Charge Transfer

After the exposure phase when the charge generation and collection take place, the readout phase follows with the charge transfer and measurement. The exposed CCD pixels are the ones in the vertical register. First, I will describe the charge transfer from one pixel to another. Figure 2.11 left shows the state of a vertical pixel at the end of the exposure phase, where the charge is collected under the collecting gate, V2. Gates V1 and V3 rest at a higher potential and act as barriers to keep the charge confined to the pixel. Lowering gate V3, the potential well will expand under both V2 and V3 gates and the pixel charge will be shared under the two, as it is shown in Figure 2.11 middle. Then, raising the V2 gate will force the charge to gather under gate V3 only (Figure 2.11 right). The holes will always follow the lowest potential. In the same principle, the pixel charge is moved gate by gate to the next pixel's V2. This circle describes the single-pixel charge transfer.

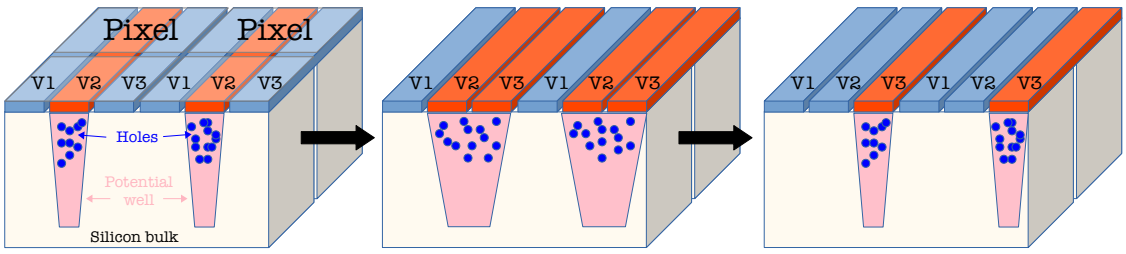

Figure 2.11: Charge transfer from gate to gate in a CCD pixel.

Using the single-pixel transfer described above as a single action, I will present now the pixel transfer to the readout amplifier. Looking at Figure 2.12, the pixel charge from the vertical register needs first to be transferred to the horizontal register and from there to the amplifier. A single vertical transfer is basically a line of pixels transferred one row closer to horizontal register. Between the last vertical row and the horizontal register there is an additional electrode called Transfer Gate (TG), which belongs to the vertical clocks. The charge is never kept under this gate, though TG will operate more as a step, allowing the charge to jump from the vertical to horizontal register. The gates of the horizontal register operate in the same principle as the vertical ones. In order to collect the charge from the vertical register and the TG, one or two horizontal clocks should be low. In fact, the rails of the horizontal clocks are lower than the vertical ones. As soon as the charge is collected in the horizontal register, the TG goes high to forbid the charge to go back to the vertical register and a pixel-by-pixel horizontal transfer moves the charge towards the

readout amplifier. The last horizontal pixel-charge falls in the Summing Well gate (SW), which belongs to the readout clocks and will be discussed in the next section.

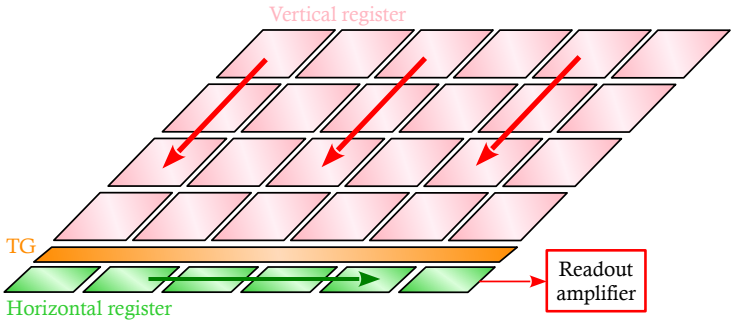

Figure 2.12: Charge transfer from the vertical to the horizontal register until the readout amplifier for a simple CCD configuration.

The quality of the pixel transfer is described by the *Charge Transfer Efficiency* (CTE). Ideally (CTE = 1), the pixel charge collected in a pixel would remain intact when it arrives at the readout amplifier. However, various sources may introduce charge loss or leakage during the transfer phase. The effect of non-local noise sources depends linearly on the number of pixel-transfers. As a result, pixels that are located close to the amplifier would not suffer much from this *Transfer Noise* compared to pixels far away. An experimental method to measure the CTE is by irradiating the CCD with a well-known radioactive X-ray source, such as Fe^{55} [82, 89] or Cd^{109} [84]. These photons will interact uniformly in the silicon and will produce $\mathcal{O}(1000)$ electron-hole pairs, confined in a few-pixels area. The measured signal as a function of the number of pixel-transfers shows a linear distribution with negative slope. This slope will define the CTE. In terms of Charge Transfer Inefficiency (CTI), it will be CTI = 1 - CTE [74]. The residual image of the charges trapped in the silicon-SiO_2 interface or the silicon bulk is an example of transfer noise [74].

Clock Induced Charge - spurious charge

Another noise source depending on the total pixel-transfer number is the *Clock Induced Charge* (CIC). Generally, the clocks to transfer the pixel-charge create electric fields that can free trapped holes or generate new electron-hole pairs. Moreover, there is an additional noise source, specifically when the CCD is operated in partial inversion. Of course, the CCD cannot operate in full-inversion, because there would be no potential well to collect the charge, as both resulting rails would be at the same potential. Partial inversion means that the gates change between inverted and non-inverted potential when they act as barriers and collectors respectively. During the transition from inverted to non-inverted, the accumulated electrons in the silicon-SiO_2 interface drift back to the channel-stops. The acceleration due to high electric fields can make them sufficiently energetic to create electron-hole pairs by colliding with silicon atoms [74]. The *spurious holes* are then collected in the nearest potential well. Thus, this spurious noise is only produced during the gate transition from the inversion to non-inversion state, the falling edge of the clocks for a p-channel CCD. When the gate goes from non-inversion to inversion state, the electrons

from the channel-stops populate the interface, depending on the substrate and channel stop resistivity. The potential difference between the channel-stop and the surface is small when electrons begin to move, therefore, there is no spurious charge in this transition. CIC decreases exponentially with the clock falling time and increases with the time the clock spends in the non-inverted state immediately after inversion. For lower temperatures the impact ionization becomes more efficient, due to carrier mobility, so the CIC increases.

As expected, the CIC depends linearly on the total number of pixel transfers. CIC should not be confused as intrinsic dark current and can be easily separated by changing the amplitude of the clocks. If the noise level changes along side with the clock amplitude, then spurious charge is likely the source. The most effective solution to decrease CIC is to wave-shape the clocks with smooth rising and falling edges. In addition, optimisation of the clock rails and amplitude is required.

Blocking pixels

A much more distinct effect can occur by small local deformations or damages during or after the fabrication and can cause pixels to behave in an undesired way. Blocking pixels have always an extreme behaviour, either consistently much charge and can reach saturation or complete lack of charge. For example, in a pixel that much current is generated (for some reason) linearly in time may be seen saturated for a long exposure and may create a tail, without saturation necessarily, as the rest of the pixel-charge packets are passing for a limited amount of time from that position. During the charge transfer, any pixels located "behind" a blocking pixel will also behave similarly. An example is shown in Figure 2.13 left. For this particular image, the problem was found to be a defect due to the ISDP gettering process. Figure 2.13 right picture was taken with a Scanning Electron Microscope (SEM), showing the defect on the top surface of the CCD.

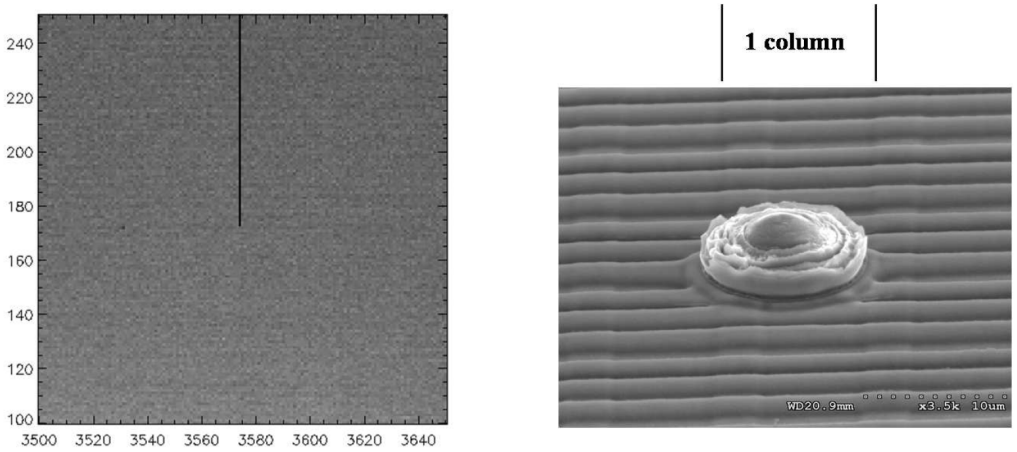

Figure 2.13: Left: CCD sub-image showing one blocked column as a vertical dark line on the background due to uniform light exposure. The readout direction is to the bottom of the image. Right: SEM showing a defect due to the ISDP gettering process. The image was taken on a fully processed CCD. The horizontal lines in the picture are the polycrystalline silicon gate electrodes. The vertical stripes are the channel stops. [90]

Pixel binning

Instead of reading out a single pixel at a time, it is possible to merge several pixels and measure their charge at once. There are several advantages using this method. The readout time depends linearly on the total number of measured pixels, considering the readout time of a single pixel being much larger than a single vertical- or horizontal-pixel transfer, and so it is effectively decreased with binning. The contribution of the charge measurement noise, that will be discussed in the next section, will only apply once for the several binned pixels and not to each pixel individually. However, this approach lowers the spacial resolution of the device, according to the desired binning. Moreover, the uniform noise sources, like dark current or CIC, are added, increasing the noise floor linearly for the number of binned pixels. A relatively small noise in a single pixel will result to a measurement of a noise N-times higher for N-binned pixels.

A point of attention concerns the full-well capacity of the pixels. Pixels with little charge can be combined together without causing any issues, concerning the total charge. If the binned charge is greater than the full-well capacity of any pixel in the readout sequence, then the pixel will be saturated and charge will flow to neighbor pixels. In practice, to bin vertical pixels, one needs to perform several vertical-pixel transfers before starting the horizontal transfer. The charges will accumulate in the horizontal register pixels. Similarly, to bin horizontal pixels, one needs to perform several horizontal pixel transfers before moving to the charge measurement. In other words, the vertical binning should not exceed the capacity of the horizontal pixel and both vertical and horizontal binning should not exceed any of the readout amplifier gates' well capacity.

Frame modes and multiple readout amplifiers

The simple configuration of a CCD that was described earlier s called full-frame mode and can become much more sophisticated with several sets of vertical/horizontal clocks and readout amplifiers in one device.

As a first example in the simple configuration described, the vertical section can be separated vertically into two equal sections with individual clocks. By doing so, the CCD could operate in full-frame mode or frame-store mode. In the latter, only the farther vertical section from the horizontal register is really exposed and afterwards the collected charge is quickly transferred to the store-section and is readout slowly, so that the exposed-section can start a new exposure right away. The benefit of the frame-store mode is that the dead time between two CCD images is minimized. However, this reduces the number of exposed pixels in half and requires twice as many vertical clocks. A CCD fabrication like this does not forbid the full-frame mode, which is when all the pixels are exposed. The two sets of vertical clocks can perform the same exact transfer, which practically leads to the previously described simple configuration.

Additionally, several readout amplifiers can be fabricated on a CCD. For example, the horizontal register of the simple configuration can be separated in two individual

halves with each having its own set of clocks. As a vertical line is moved to the horizontal register, it can be transferred to opposite directions, not towards the middle of the register, where at each end there is a readout amplifier. The great advantages of this concept are the linearly reduced readout duration, in this particular case halved, and the offer of an alternative readout amplifier in the case that one amplifier is damaged. As individual sets of clocks, there are no restrictions to operate the clocks to drive to the same side. So, in this example, there is the ability to readout the CCD with the one or the other amplifier or with both at the same time (see Figure 2.14). The charge transfer principle is always the same. This concept can be extended to multiple readout amplifiers by separating the vertical and/or the horizontal registers in two or more segments.

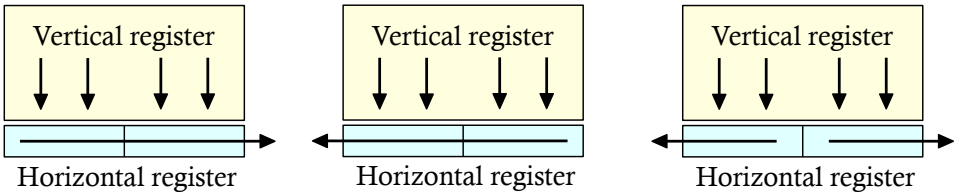

Figure 2.14: An example of the readout modes of a CCD with segmented horizontal register, using one amplifier (left and middle) or both (right).

2.5 Charge Measurement

The charge measurement is the final operation a CCD can perform [74]. The CCD outputs an analog signal, also know as *video signal*. It is then passed to the external electronics where it is usually amplified and measured by an Analog-to-Digital Converter. In this section, I will describe the steps to the video signal and some of its important characteristics.

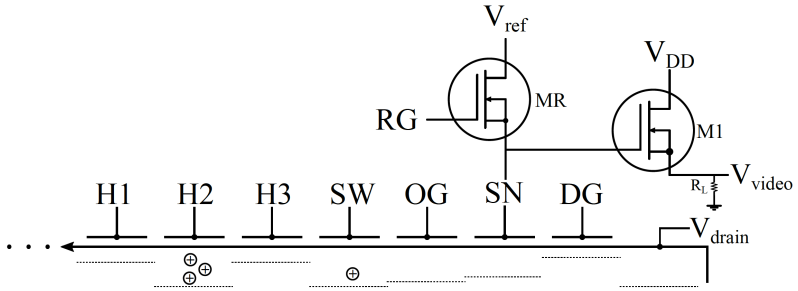

Figure 2.15: Readout amplifier of a CCD. OG can be either a bias for convectional readout or a clock for skipper readout. [85]

The charge-packet, from a single pixel or after binning, ends up to the SW gate at the end of the charge transfer step. The SW rests at its low rail during the charge transfer, which is lower than the horizontal clock low rail, to collect the charge from the last horizontal pixel. The next gate after SW is the Output (transfer) Gate. In conventional CCDs, the OG is a bias voltage (V_{OG}) with a value somewhere between the upper and lower rails of SW. When the SW is low, the charge is collected and cannot pass the V_{OG}

whose potential is higher. To measure the charge, the SW changes to high and the charge jumps through the V_{OG}, which is now lower than the SW high, to the Sense Node (SN), which is practically a small floating capacitor (C_{SN}). The potential of the SN is set by a bias voltage reference, V_{ref} or V_r, lower than the V_{OG}. The V_{ref} is applied to the SN through a N-channel Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) whose source and drain are connected to the SN and V_{ref} bias respectively, and its gate is connected to the Reset Gate (RG) clock. When the RG is low, the SN is floating. When it is high, it shorts the SN to the V_{ref}, through MOSFET MR in figure 2.15. The RG operates more like a logic pulse than a CCD clock as the previously discussed vertical, horizontal or SW.

So, the RG allows the SN to (re)set its potential to V_{ref}. When the SW goes high and the charge-packet Q is driven to the SN, its potential changes by:

$$V_Q = \frac{Q}{C_{SN}} \tag{2.3}$$

which is measured in V. The sensitivity of the SN is defined by:

$$S_{SN} = \frac{|e^-|}{C_{SN}} \tag{2.4}$$

where e^- is the electron charge, and S_{SN} is measured in $[\frac{V}{e^-}]$. The conversion factor is $\mathcal{O}(1\,\mu V/e^-)$ [82]. The SN potential after the reset and before the moving the charge is the *pedestal* and after moving the charge is the *signal* level (see Figure 2.16). A dent is shown at the video signal caused by the reset pulse. Ideally, the pedestal would be equal to the V_{ref} bias. However, this is not true due to the reset noise (discussed later) and the pedestal comes with an uncertainty after every reset. Therefore, one needs to measure the difference of the signal and pedestal ΔV in order to find the voltage due to the charge-packet ($V_Q = \Delta V$). Two ways to perform this measurement are explained below: Correlated Double Sampling and Dual Slope Integration.

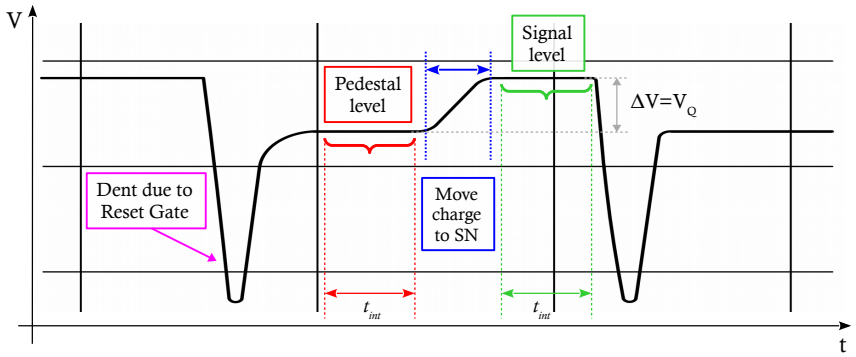

Figure 2.16: Simplified CCD video signal vs time.

After the charge is measured and the information is recorded, the final step is to dump the charge. Next to the SN there is the Dump Gate (DG) which rests at its high rail.

When it changes to low, it is lower than the SN potential and the charge is transferred through the DG to a drain bias voltage (V_{drain}). A new cycle of resetting the SN takes place and the next charge-packet is moved to be measured. This is the repeating sequence of steps to readout a whole CCD. All the signals mentioned here can be physically seen in the photos of Figure 2.4.

Skipper readout

An improvement to the conventional CCDs is the Skipper amplifier [85, 91]. The Skipper technique allows for multiple non-destructive measurements of the charge-packet. This is achieved by using a floating gate as sense node and replacing the bias V_{OG} with the OG clock. The floating gate allows the charge to change the potential of the sense node by V_Q without being in contact with the gate, so non-destructive contrarily to the conventional CCD, while the OG clock allows to move the charge back and forth from the SN to the SW. Both high and low rails of the OG are between the high and low rails of SW. Let the charge under the SW while the OG is high. The SW, then, goes high (higher than OG) for a very short period and the charge is transferred through the OG to the SN. After the measurement, the OG goes low for a short period, lower than the SN but not the SW, and so the charge moves back to the SW. This cycle can be performed as many times as desired, up to several thousands. Then, the charge is dumped the same way as before.

With the skipper readout, the statistics are increased and so the error of the pixel measurement will decrease with the inverse of number of the non-destructive charge measurements (NDCM) with respect to a single skip measurement. Figure 3.11 shows a the pixel charge distribution of a CCD for different NDCM numbers. For a sufficiently high NDCM the resolution reaches below a single electron. The readout time of a skipper CCD depends linearly to the NDCM, but further discussion around that will be done later (see next chapter).

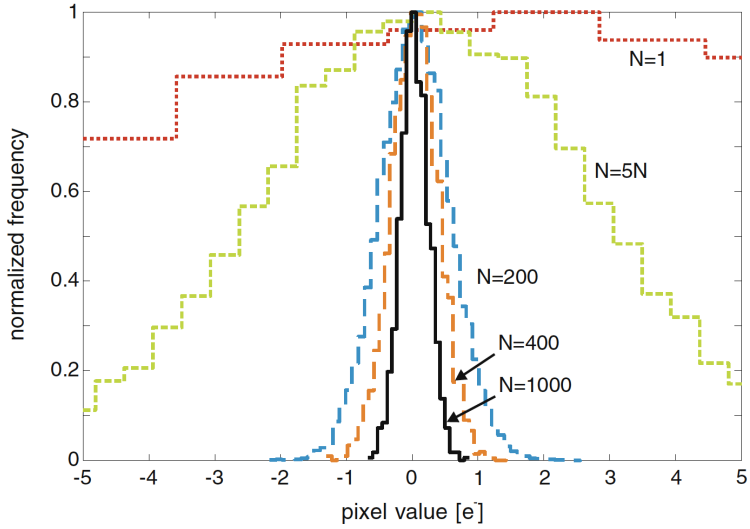

Figure 2.17: Sample histogram of the background pixels from the final images of a Skipper CCD for different numbers of averaged samples per pixel N. The histograms are normalized to their maximum values and the pixel value is in electrons [91]

2.5.1 Noise sources

There are several noise sources during the charge measurement. These do not include the intrinsic dark current or the CIC which are measured and define the quality of the CCD operation.

Reset or kTC noise

The Reset noise, also known as "kTC" noise, is a thermally generated noise by the reset MOSFET on the SN [74]. The noise is expressed in volts or in charge units as:

$$N_R(V) = \sqrt{\frac{kT}{C_{SN}}},\ N_R(e^-) = \frac{\sqrt{kTC_{SN}}}{|e^-|} \tag{2.5}$$

where k is the Boltzmann constant ($1.38 \cdot 10^{-23}$ J/K), T is the temperature in K, C_{SN} is the SN capacitance in F, and $|e^-|$ is the electronic charge ($1.6 \cdot 10^{-19}$ C). Note that it depends on the temperature and the C_{SN}, which is quite small, usually in the order of fF. This noise is responsible for the uncertainty of the mean value of the pedestal level after the reset of the SN.

Output amplifier white noise

A thermal white noise is caused by the output amplifier MOSFET described by Johnson's white noise equation [74]. The white noise has a flat distribution in the frequency spectrum (see Figure 2.18).

Flicker or 1/f noise

The Flicker noise or 1/f noise is generated in the output MOSFET and is generally accepted that is originated by random trapping and emission of charge carriers near the oxide interface and fluctuation of the carrier mobility [74, 89, 92]. The 1/f noise is dominant at low readout frequencies, as can be seen in Figure 2.18.

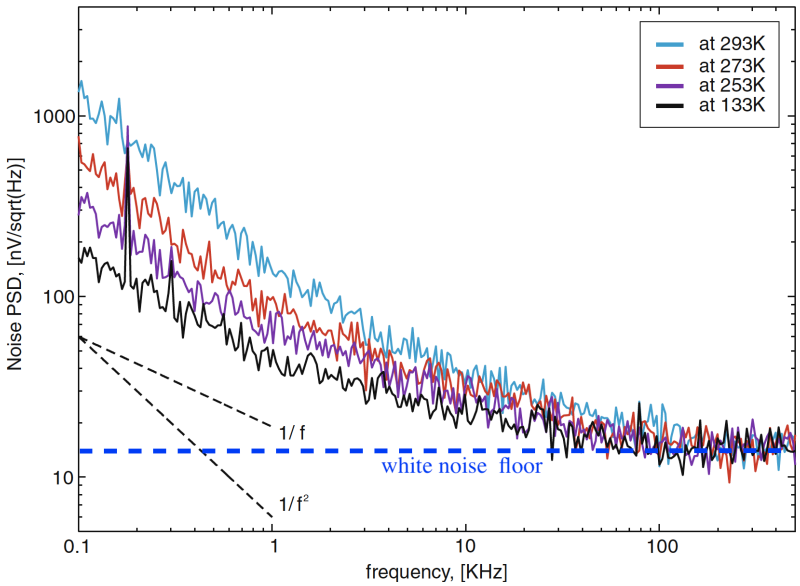

Figure 2.18: Power spectrum density (PSD) of CCD output amplifier noise. [91]

2.5.2 Measuring techniques

The charge to voltage conversion is performed when at the charge transfer to the SN and the CCD outputs the analog video signal. This signal is then measured by external electronics, usually consisting of a *front-end chip* to amplify the video signal and an *Analog-to-Digital Converter* (ADC). Both of these components are developed for the DAMIC-M experiment by the collaboration and will be further discussed in the following chapters. For the moment it is necessary to mention that a single measurement from the ADC is called sample and as soon as the pixel information is digitized it is stored to a computer memory. I will explain the two measuring techniques that are most commonly used.

Correlated Double Sampling

One way to measure the pedestal and signal levels of the video signal is by simply sample each level once, record the two values and subtract them offline to find:

$$V_Q = V_{signal} - V_{pedestal} \tag{2.6}$$

Each single measurement will have a relatively high error due to the readout resolution and will also lose any information about the stability of each level. As a solution, sampling several times each level and averaging them will reduce the error of each level individually and the final difference will be more accurate. The higher frequency of the signal (the upper limit of its bandwidth) is half of the Nyquist rate, which is the minimum frequency at which a signal must be sampled to record all of its information. Recording data at a frequency higher than the Nyquist rate is called oversampling. Oversampling a signal leads to Digital CDS (DCDS) which offers several advantages. Besides the averaging and subtracting the two levels, it improves the Signal to Noise ratio, and allows processing the stored data digitally, applying filtering, Fourier transformation etc. In principle, after the reset and the charge transfer to the SN, there must be some delay for the pedestal and signal levels to stabilize. DCDS allows recording the shape of the settling periods for further studies. On the other side, the volume of data increase significantly, which can be troublesome in terms of data transfer and memory. A major requirement of this mode is using a quite fast ADC in order to keep the readout time at minimum.

Dual Slope Integrator

Another system to measure the video signal is the Dual Slope Integrator (DSI). Instead of sampling once or multiple times, the DSI integrates both the pedestal and signal levels for the exact same time t_{int} (*integration time*) with reversed polarities (see Figure 2.16). The integration is achieved in a hardware way with an RC integrator circuit. This results to:

$$\frac{1}{\tau_{RC}}(-\int_0^{t_{int}} V_{pedestal}\, dt + \int_0^{t_{int}} V_{signal}\, dt) =$$

$$= \frac{1}{\tau_{RC}}\left(\int_0^{t_{int}} (V_{pedestal} + V_Q)\, dt - \int_0^{t_{int}} V_{pedestal}\, dt\right) = \frac{1}{\tau_{RC}} \int_0^{t_{int}} V_Q\, dt = \frac{t_{int}}{\tau_{RC}} V_Q$$

where $\tau_{RC} = RC$ is the integrator time constant in seconds ($1\,\mathrm{s} = 1\,\Omega{\cdot}\mathrm{F}$). The +/- signs in front of the integrals arrive from the polarity with which each level is integrated and they could also be inverted. The t_{int} is set by the user and the τ_{RC} results from hardware, so the amplification factor $\frac{t_{int}}{\tau_{RC}}$ is well known. After the integration, the ADC needs to sample only once.

Considering a fixed τ_{RC}, the only parameter in this readout mode is the t_{int}. Note that a single charge measurement will last at least $2t_{int}$ plus any delays for the reset bump to decay and the signal level to stabilize. The t_{int} in scientific CCDs is chosen usually $\mathcal{O}$(0.1-10 μs). The plot of the CCD readout noise versus t_{int} is often the reference from which the optimal t_{int} is chosen. The measured noise however depends on many parameters, such as temperature, dark current, etc, and so its absolute amplitude is not universal. In several scientific CCDs, a plateau starts to appear for an integration time of about 10-20 μs with a readout noise of a few electrons [92, 93]. The integration practically increases the statistics of the measurement, minimizing the white noise. The noise plateaus instead of keep decreasing for longer integration time, because the 1/f noise dominates and equates the profit.

More about technical specifications of both ways of measurement are provided in the following chapters where I discuss the progress of DAMIC-M on front-end electronics and ADCs.

2.6 Scientific CCD operating conditions

I will close this chapter mentioning some conditions under which a scientific CCD operates properly and briefly describing the hardware necessary for this. It has been well established by now that temperature plays a major role in the dark current and other noise sources production. As a result, the CCD needs to be operated at low temperatures. Yet, there is a low limit around $\sim$70 K (or $\sim$-200 C) at which the dopant will no longer give or capture electrons. The structure of the crystal is frozen and any created electron-hole pairs will recombine. This condition is called *freeze-out* and is the point where the CCD will cease to work [74]. Close to this temperature but still in operating conditions, the CCD starts presenting a reduced CTE.

The scientific CCDs are usually operated at 100-140 K. It is not possible to cool down a CCD in an open-air environment due to thermal loss and additionally the humidity in the air would condensate and freeze on surfaces. The CCD is operated inside a metallic chamber called *cryostat*, from which a vacuum pump removes the air. The cryostat must be strong enough to withstand a nominal low pressure usually down to 10^{-9} bar. The CCD should not make contact with any surfaces of the cryostat and rests on thermal insulating

structures. The only other contact to the CCD is the *cold finger* or *plate* that provides the low temperature to the CCD from a cryocooler. A non-imaging use of a CCD, such as dark matter search, requires also a dark environment. Of course it requires way more protection from background radiation than just a black cover for the given example, but this will be further discussed in the next chapter specifically for the DAMIC-M experiment.

Chapter 3

DAMIC-M

The DAMIC (Dark Matter in CCDs) collaboration is dedicated to the search for dark matter through its direct interaction with the nucleus or the electrons of silicon atoms in the bulk of scientific-grade CCDs. This rare event search requires extremely low (ideally zero) background, excluding any source of light, cosmic and radioactive background. Therefore, the use of the CCDs is different than in astrophysical applications that focus on receiving light from sources far away. The illumination direction and the anti-reflecting techniques are no more relevant. uch effort is put in protecting the raw materials the detector is built with (not only the CCDs but the whole structure), minimizing their radioactive contamination, and provide shielding from all kinds of external background (neutrinos excluded). Of course, the CCD must be operated in an optimal configuration to reduce the dark current and other noise sources, as they were described in the previous chapter.

A last yet equally important point is the detection energy threshold and the energy resolution of the detector. The energy threshold defines the limit below which possible events are mixed with noise and cannot be separated. For a lower energy threshold, the search extends to lower dark matter masses. The energy resolution on the other side defines the measurement accuracy of the detector. A large readout noise means low resolution and this leads to higher energy threshold. In a full CCD setup, the units of energy, charge, voltage, and Analog-to-Digital Units (ADUs)[1] are all connected and the results can be converted to any of them for convenient presentation.

3.1 DAMIC at SNOLAB

The DAMIC experiment had been running at SNOLAB at its previous version from 2017 until the fall of 2021. The SNOLAB underground laboratory is located in Sudbury, Canada, under 2 km of rock (6010 m.w.e.[2]) protecting the detector from cosmic radiation. DAMIC at SNOLAB employed 7 high resistivity, n-type silicon with p-type buried

[1] the units in which the output of an Analog-to-Digital Converter is expressed
[2] m.w.e. = metre water equivalent

channel, fully depleted, $4\text{k} \times 4\text{k}$ pixel CCDs with $15 \times 15\,\mu\text{m}^2$ pixel area and an active thickness of $665 \pm 5\,\mu\text{m}$ [68]. In these thick CCDs, induced charges have enough distance to drift until reaching they are collected at the potential well and using their diffusion it is possible to calculate the depth of the creation of the charge packet and reconstruct the particle track in 3-dimensions. This great spacial resolution leads to particle identification based on the shape of the pixel-cluster/track (see Figure 3.4). Straight linear tracks correspond to cosmic muons crossing the detector without stopping. Worm-like tracks are electrons. α-particles, that are much heavier than the previous two, produce a lot of charge that is spilled in neighbour pixels in the same column. Large round clusters correspond to highly diffused α-particles that interact in the bulk of the substrate silicon, called *plasma* [94]. When an α-particle interacts close to the frontside, the channel-stops restrict the generated charge and the cluster appears elongated in the vertical direction, *bloomed* [74]. Using the diffusion of the track in both x and y directions, one can successfully identify a cluster as plasma or bloomed α [95].

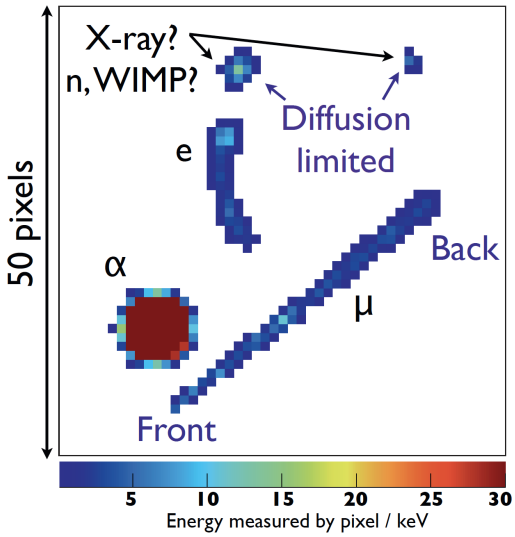

Figure 3.1: Particle identification from a CCD image. [96]

The detector's total target mass of DAMIC at SNOLAB was 42 g, but depending on the analysis, a subset of the 7 CCDs can be chosen which results to a lower mass [95]. The CCDs had 4 conventional (non-skipper) amplifiers and the device could be read from all of them at the same time. A pixel readout noise of $1.6\,e^-$ was achieved [68]. The minimum dark current level that has been measured is $2{\cdot}10^{-22}$ A/cm$^2 \approx 10^{-3}\,e^-$/pixel/d. The background of DAMIC at SNOLAB is measured equal to 11.8 d.r.u.[3]. Besides its own contribution to the dark matter search, DAMIC at SNOLAB had produced great knowledge and experience on the CCDs for the follow-up upgrade.

In 2020, DAMIC at SNOLAB published results for the low-mass WIMP search with an 11 kg·d exposure [68]. The observed energy spectrum for electron-equivalent energies

[3] 1 d.r.u. = 1 event/(keV·kg·day)

above 200 eV_{ee} [4] in the DAMIC CCDs is consistent with the well-studied background from natural radioactivity [97]. The energy threshold of DAMIC at SNOLAB is $50\,eV_{ee}$. An excess of 17.1 ± 7.6 events was reported in the energy range 50-200 eV_{ee} above the background model expectation [98, 97]. These events are consistent with an exponential energy spectrum with a decay constant of $67 \pm 37\,eV_{ee}$.

In order to verify the existence of this excess, a search with a lower energy threshold is necessary. For this reason, DAMIC at SNOLAB has been upgraded in the last quarter of 2021 by replacing the old conventional CCD with new skipper ones (see Figure 3.2). DAMIC and SENSEI[5] in collaboration have installed 2 skipper CCDs each in the detector of DAMIC at SNOLAB and will be operated independently, even though the setups are quite similar. Additionally, the acquisition system has been changed to the Low Threshold Acquisition (LTA) controller [99], to support the skipper readout and also to improve the electronic noise.

Figure 3.2: DAMIC detector at SNOLAB before (left) and after (right) the upgrade of 2021. Left: Tower of 8 CCDs (36 g target mass). Right: DAMIC and SENSEI new skipper CCDs.

3.2 The future with DAMIC at Modane

DAMIC at Modane (DAMIC-M) is scheduled to start its installation in 2023. It will be located at the Modane Underground Laboratory (LSM, in french: Laboratoire Souterrain

[4] The energy transfer from a nuclear recoil in eV to the electrons for ionization production is not fully efficient. The electron-equivalent energy (eV_{ee}) is the pure energy absorbed by the electrons and measured in the clusters. The quenching factor of silicon describes how much of the energy is transferred. They are nearly the same at high eV_{ee}.

[5] The official webside of SENSEI can be reached at https://sensei-skipper.github.io/

de Modane). The detector will be composed of several skipper CCDs with a total target mass of the order of 1 kg. With the skipper readout it will achieve sub-electron resolution with a goal of 0.1 e^-. DAMIC-M is expected to have a detection energy threshold of 10 eV which corresponds to 3 e^- in terms of charge. This will be an improvement of a factor of 5 compared to DAMIC at SNOLAB. One of the major requirements for the experiment is the suppression of the background down to $\mathcal{O}$(0.1 d.r.u.).

3.2.1 The heart of the detector

The CCD devices of DAMIC-M will have a very unique design. In fact, 4 individual 1.5k $\times$ 6k pixel CCDs will be packaged together. They will be fabricated on n-type high resistivity silicon wafers with a buried channel and 3-phase technology, $15 \times 15\,\mu m^2$ pixel area and 675 μm thick with a target mass of 20 g per package. A thin substrate contact will allow the full depletion of the pixels by applying a potential higher than 40 V [58]. Two skipper amplifiers will be fabricated on each CCD. About 50 CCD packages will be assembled vertically in a structure shown in the concept design in Figure 3.3, resulting to a total target mass of 1 kg. The low temperature to the CCDs will be delivered through the copper holder. Each CCD will receive the control signals and output the video signal through a connector on the top of the package. The detector will be placed in an L-shape cryostat, shown in Figure 3.3 right. The CCDs will be cooled at a temperature around 100 K using liquid nitrogen. Small modifications are still applied to the design that can affect the expected background model, however, the idea and the numerical scales are representative of the final one.

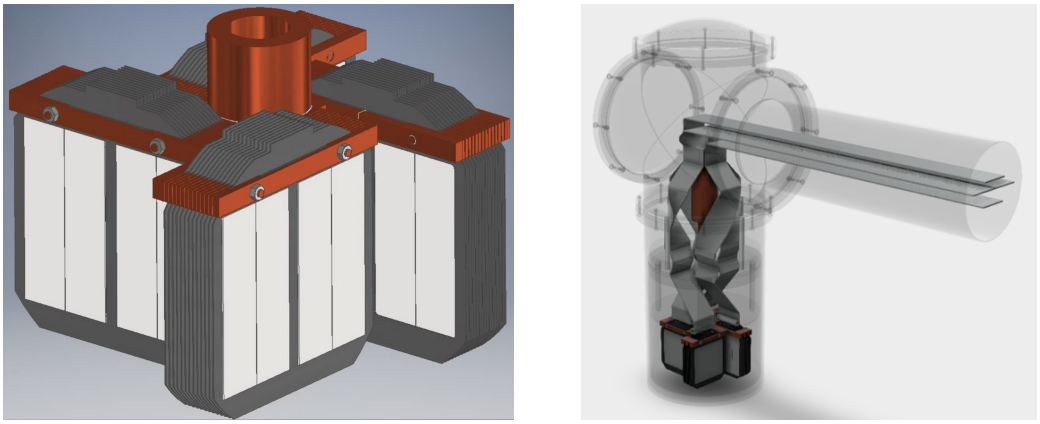

Figure 3.3: Left: Concept design of DAMIC-M 50 CCDs assembly. Cold is delivered through the copper structure. Right: CCDs in the L-shape cryostat with cables delivering the signals

3.2.2 Near-CCD Background

Close to the CCDs, there are several components that can introduce background. The CCD holder and the part of the cryostat very close to the CCDs will be made of ultra-pure

electroformed copper. On top of the CCDs, the cables will pass through holes in a three-layer shielding of ancient Roman lead - electroformed copper - ancient Roman lead. The rest of the cryostat will be made of oxygen-free copper (OFC), which is very pure but not as much as electroformed [100]. The cables and the adapters on the CCD packages will significantly contribute to the background. In addition, the CCD itself can be a source of background.

Silicon-32

The great spatial resolution of DAMIC at SNOLAB CCDs allowed the search for inner silicon bulk radioactive contaminants. Primarily, the study is based on the assumption that a radioactive atom will decay without changing its position. The reconstructed cluster of the events, using the diffusion of the track, reveals the two end-points of a decay projectile, without always deducing the information of which is the start or the end. A follow-up decay will occur at the very same area with one of the two, giving away the position of the radioactive atom. A tool has been developed by the DAMIC collaboration to correlate the position and the energy of events in a long-time period and identify them as steps of decay chains [95]. The results for the radioactive isotope Silicon-32 (^{32}Si) showed a contamination that needs to be reduced for the DAMIC-M experiment. The ^{32}Si is produced by cosmic spallation. Its decay chain is:

$$^{32}\mathrm{Si}\,(153\,\mathrm{yr}) \xrightarrow[\beta\text{-decay}]{227\,\mathrm{keV}} {}^{32}\mathrm{P}\,(14.3\,\mathrm{d}) \xrightarrow[\beta\text{-decay}]{1.71\,\mathrm{MeV}} {}^{32}\mathrm{S}\,(\mathrm{stable})$$

So, trying to spatially correlate two events with energies related to those above within a period relative to the half-life of ^{32}P can result to a probability of those events originating from a ^{32}Si atom. An example of such a coincidence is shown in Figure 3.4. A correction for accidental spatially correlated events is also applied. Surface exposure is minimized for the ultra-pure silicon wafers for DAMIC-M produced by TOPSIL[6]. When necessary, they are transported from place to place in a special container with $\approx 15\,\mathrm{t}$ of iron shielding and whenever there is a waiting period, they are stored in underground laboratories.

Similar studies took place to set limits on bulk contamination from ^{238}U and ^{232}Th chains. Additionally, a surface contamination of ^{210}Pb dominates. ^{210}Pb is a long-live daughter (22.2 yr) of ^{222}Rn (Radon). Radon is in gaseous form and tends to stick on the surfaces of the CCD when it is open to air. The LSM offers a lab air purification system to reduce the Radon level by a factor of 1000.

Tritium

Tritium (Hydrogen-3, ^{3}H) is a radioactive isotope of hydrogen and decays into Helium-3 through β-decay releasing $\sim$18 keV energy with a long half-life of $\sim$12 years [101]. Tritium

[6]The official website of the company can be reached at www.topsil.com

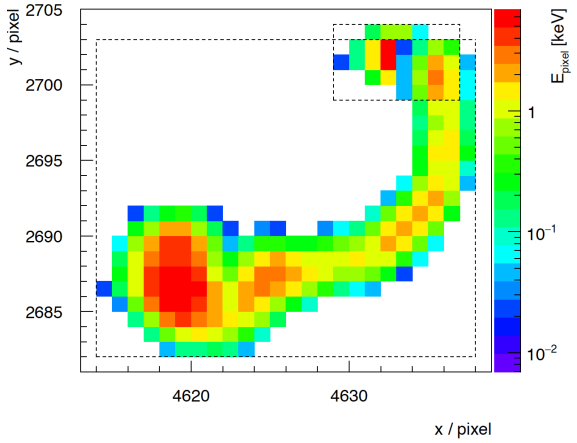

Figure 3.4: A spatially-correlated $\beta - \beta$ candidate of a ^{32}Si decay chain. The first and second decays have energies of 77 keV and 399 keV respectively with a time separation of 13.7 d.

is produced in silicon at sea-level mostly by spallation of high-energy cosmogenic neutrons with silicon nuclei [102]. Additionally, a very detailed study on a DAMIC at SNOLAB CCD showed a concentration of hydrogen of at least two orders of magnitude higher in the 1 μm-thick ISDP gettering layer than the rest of the volume. The contamination of the gettering layer is a result of its fabrication on the CCD where hydrogen is present in a several forms, such as deionized water. For this reason, the ISDP layer for DAMIC-M CCDs will be thinned down to the minimum thickness for the substrate contact ($\mathcal{O}$(10 nm)).

3.2.3 Detector shielding and LSM

The cryostat of Figure 3.3 right will be surrounded -from inside to outside- by lead, to stop external gamma radiation, and polyethylene shielding, to protect from neutrons. The amount of both the inner and external shielding materials have to be just sufficient to balance protecting the detector, but not introduce additional background. For example, lead has the ^{210}Pb isotope which is radioactive and use of too much of it may have the opposite results. The DAMIC-M detector will be placed in the LSM [103] which is located in the middle of Fréjus Road Tunnel in the borders of France and Italy, at an altitude of 1200-1300 m. Despite being above sea-level, the laboratory is located right below the peak of the mountain with around 1800 m (4800 m.w.e.) of rock protecting from cosmic radiation. The muon flux is reduced by a factor of at least 10^6 compared to sea-level [104] to 4-5 $\mathrm{m}^{-2}\,\mathrm{day}^{-1}$ [103, 105, 106]. The lab air purification system allowed a radon concentration of 5-10 $\mathrm{Bq/m}^3$, lower by more than a factor of 10^3 compared to atmospheric air. The overall background study anticipates an activity of 0.6 d.r.u. Major contributors are the external lead shielding and the kapton cable option to deliver the signals to and from the CCDs. This model is not final as there are still modification of the detector and its shielding.

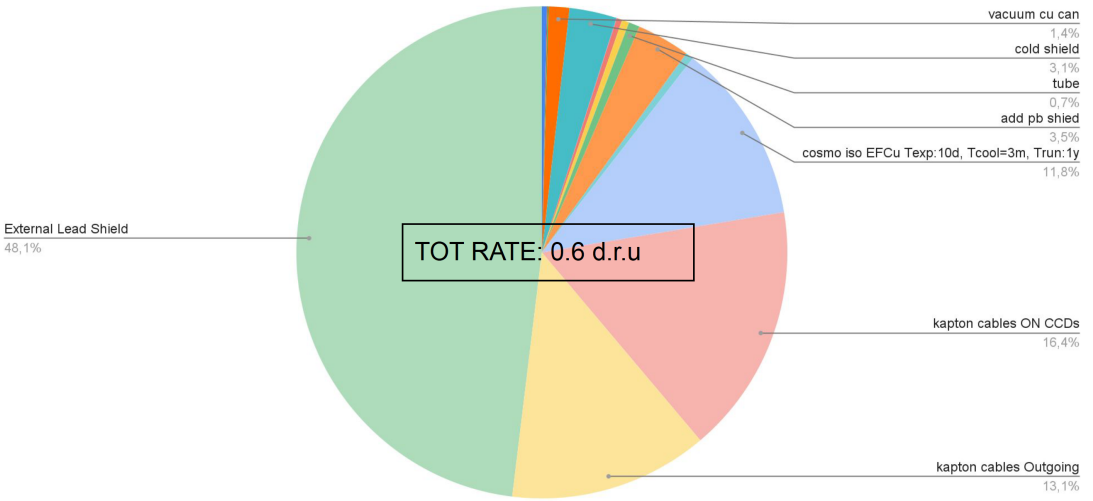

Figure 3.5: Expected background of DAMIC-M at LSM. Model not final.

3.3 DAMIC-M new electronics

The CCD controlling system will be far from the detector. A-few-meter long cables as mentioned before will deliver the signals to and from the CCDs. My personal contribution to the DAMIC-M experiment has been on the R&D of the new electronics system and most of my work is presented in detail in the following chapters. Here, I am going to introduce namely the necessary pieces in an integrated apparatus that compose the acquisition system.

All the CCD control signals, biases and clocks, for the exposure and readout phases are provided by a control board. The output signal of the CCD is delivered to a front-end circuit (chip or board) that amplifies the signal to improve the Signal-to-Noise Ratio (SNR). It is more efficient to perform the amplification stage as close as possible to the CCD output to minimize any thermal noise that might be introduced to the very small video signal until its digitization with an ADC, which is far from the detector. So, the front-end circuit is often located inside the cryostat. An option for DAMIC-M is to have a chip soldered directly on the CCD package. Additionally, operating at the same low temperature as the CCD results in lower electronic noise introduced by the chip itself. In such a case, the chip must be radiopure and not emit thermal radiation when operating. A balanced point for its placement should be found. Finally, the amplified video signal is delivered to an ADC where it is measured. In a DSI readout, the integration of the video signal can be performed either at the front-end circuit or at a circuit right before the ADC sampling. DAMIC-M develops all parts of this three-stage acquisition system. The R&D tasks were allocated to several groups/labs of the collaboration.

A *Clocks And Biases Asic for CCD* (CABAC) originally developed for the Large Synoptic Survey Telescope (LSST)[7] is planned to be used for the control board. A design where the biases for the CCD, the rails (also bias voltages) for the clocks and the clocks

[7]renamed to "Vera C. Rubin Observatory" in June 2019

themselves are all produced by a set of 4 CABAC chips (*4CABAC board*) was developed. Due to several hardware issues that were faced during the evaluation of the board, an alternative design was proposed using a 16-channel 16-bit Digital-to-Analog Converter (DAC) to produce the biases and rails and use CABACs only for the clocks as a more robust solution. A prototype board with one DAC and one CABAC was designed and evaluated, called *ProtoCABAC*. The Paris group of DAMIC-M at LPNHE took over the development and testing of the control board.

For the front-end chip, two versions of the *CCD Read-Out Chip* (*CROC*) were developed, yet revealing several problems. A third simplified version of the front-end chip was additionally developed called *Differential CCD Amplifier* (*DCA*). Their development and testing were also taken over by the Paris group.

As for the ADC, three chips were initially proposed of different resolution and sampling speed (see details in Chapter 6). A prototype board with the 18-bit 15 MHz LTC2387-18 chip was developed by the Paris group called *Rapide 4ADC board*, but the Zurich group took over the development and evaluation of all the different ADC options. The complete study and comparison lead to a final decision of using the fast LTC2387-18 ADC among the other two which have higher resolution but lower speed.

The Chicago group took over the development of the motherboard with an FPGA[8] through which the communication of the user and the electronics is achieved. This board's name is *Online Digital Interface for Low-noise Electronics* (*ODILE*). The protocols of the ODILE board have been developed in C++ language, executing basic actions. The user, however, controls the acquisition system through a Python software, based on a software developed for the LSST, modified for the needs of DAMIC-M by the LPNHE group. The control board, the front-end chip and the ADC are defined as separate objects in the Python software and communicate with ODILE through individual ports.

A concept schematic of the DAMIC-M new acquisition system is shown in Figure 3.6. The control and the ADC boards are plugged on opposite sides of the ODILE board

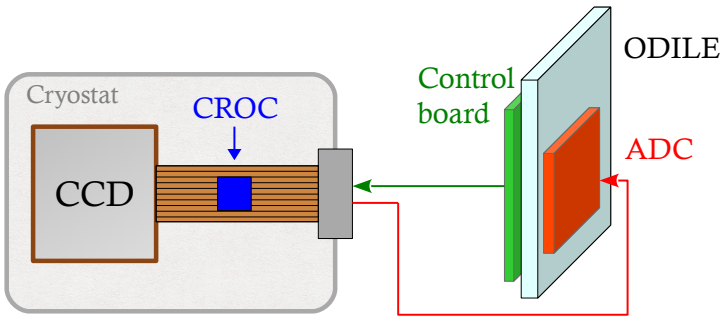

Figure 3.6: Concept schematic of the new DAMIC-M acquisition system for one CCD.

through HSMC[9] connectors and are located far from the detector. The front-end chip integration is not yet fixed. Several options such as placing the bare chip on the CCD

[8]Field-Programmable Gate Array
[9]High Speed Mezzanine Card

package, or on the flex cable (as is shown here), or soldering the packaged chip on a board were considered depending on the requirements on the radio active background. There will be one complete system for each of the CCD packages, the control of which will be achieved using a central server, with each CCD package being an individual client.

3.4 CCD testing at surface level in LPNHE, Paris

A complete CCD setup has been installed at LPNHE, Paris, France, at the end of 2017, using a commercial CCD controlling system, called Leach (Gen III[10]), provided by Astronomical Research Cameras, Inc.[11], and has been operating DAMIC CCDs at surface level for testing purposes. The Leach system employs several electronic boards in the same principle as described in the previous section. It is composed of a bias (ARC-33 - LBNL Bias Board) and a clock (ARC-32 - IR and CCD Clock Driver Board) board, a video board (ARC-45 - Dual Readout CCD Video Board) and 2 boards for communication between the controller (ARC-22 - 250 MHz Fiber Optic Timing Board) and the host computer (ARC-66 - PCIe Interface Board). All of the boards are connected to a controller housing (ARC-70 - 6-Slot Controller Housing), except for the ARC-66 which is installed inside the host computer (see Figure 3.10). The Leach system is accompanied by a bias substrate voltage source and a video preamplification board.

I will mention a couple of hardware details of the Leach system as a reference for comparison with the new electronics. The bias board has 16 outputs produced by 4 12-bit DAC (Analog Devices DAC8420ES) chips. The clock board provides up to 24 clocks with programmable high and low rails produced by 8-bit DACs (MAXIM MAX529CAG). The rising and falling slopes of the clocks are fixed for the board and can be adjusted by the values of the resistors and capacitors, or the RC time constant, of the output circuit on the board, thus cannot be programmed and can only change by hardware modification. The video board has 2 single-ended input 16-bit and 1 MS/s ADCs (DATEL ADS-937). The board can be configured to receive either single-ended or differential signals using a couple of jumpers. In the latter case, there is a circuit that converts the differential signal into single-ended. The board can be programmed to perform simple sampling of the video signal or DSI measurement.

The V_{sub} is produced by several 9 V batteries connected in series. The batteries are a low noise bias voltage source. A total of 12×9 V batteries are used for the battery pack that I have put together. Each battery is connected to a manual switch as is shown in Figure 3.7, which also shows an example of the connectivity of 4 batteries. The switch, depending on its position, connects the middle node to either A or B poles. The way the batteries are connected together and to the switches, allows the user to choose which batteries will join the series to produce the V_{sub}. This isolates each battery and keeps a

[10] A more recent Gen IV version of the Leach system exists
[11] ARC can be reached at https://www.astro-cam.com/

functional battery pack in case one battery is not working for some reason. The battery pack outputs a voltage equal to a multiple of 9 V at the lemo connector on the left. The shielding of the lemo connector and the centre contact are connected to the negative and the positive poles of the battery pack respectively (see Figure 3.7 left). The battery pack

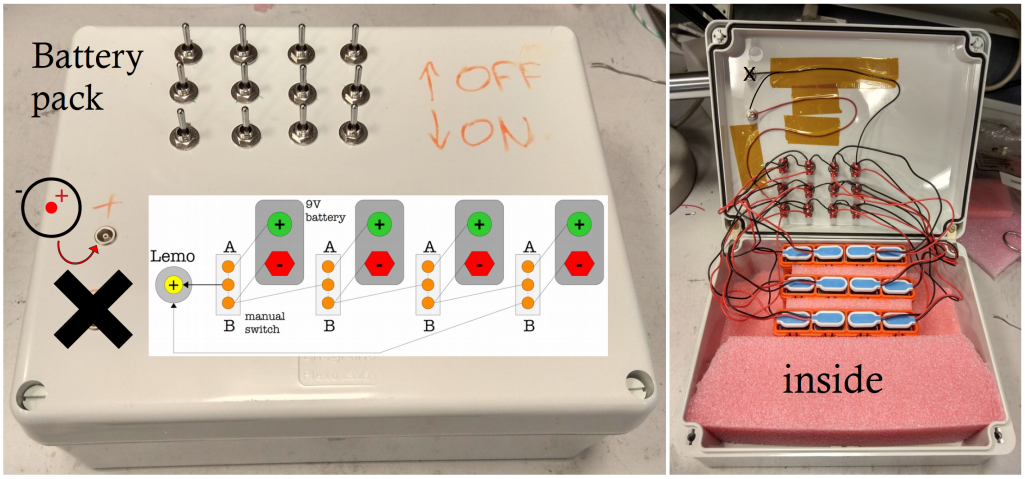

Figure 3.7: Photo of the battery pack for the V_{sub} closed (left) and open (right).

voltage is then passes through a circuit with a general manual switch, a relay (electronic switch) and an RC filter (see Figure 3.8). The general switch can simply cut off the voltage manually. Normally the switch stays on for long periods, since the relay is also a general switch but controlled in a software way. The relay (AXICOM P1 Relay V23026) allows the input voltage to reach the output controlled by an analog input that behaves like a logic pulse; for the used component logic low/high is 0/5 V. A signal from the bias board of the Leach controls the relay of the filter box. The V_{sub} can be as high as $12 \times 9\,V = 108\,V$, so a smooth ramp up/down is required. An RC filter is placed right before the output of the filter box (see Figure 3.8), composed of a 10 kΩ resistor and a 50 μF capacitor resulting to a time constant of 0.5 s, in accordance with the suggested value of 75 V/s ramp rate of the Lawrence Berkeley National Laboratory (LBNL) *4k × 2k and 4k × 4k CCD Users Manual* [107] A study of the dark current dependence on the V_{sub} of the CCD operated in LPNHE has shown a plateau for values above ∼40 V. High diffusion is observed when operating the V_{sub} below this value indicating that the CCD is not fully depleted.

A general switch (manual or not) for the V_{sub} is essential for the *erase* procedure of the CCD. The relay is optional although it makes this procedure automatic and precise timewise. The erase is an in-vivo procedure in order to eliminate the trapped holes in the silicon-SiO_2 interface that was described in the previous chapter [82]. The idea is to lower the V_{sub} to 0 V in order to flood the silicon bulk with electrons. At the same time, the vertical clocks are all raised to high, sometimes even higher than their upper rail during exposure, in order to attract electrons to the interface. The electrons recombine with the holes "erasing" the residual image at the interface. The V_{sub} then can go high again and the vertical clocks return back to normal sequencing. The erase procedure usually lasts a

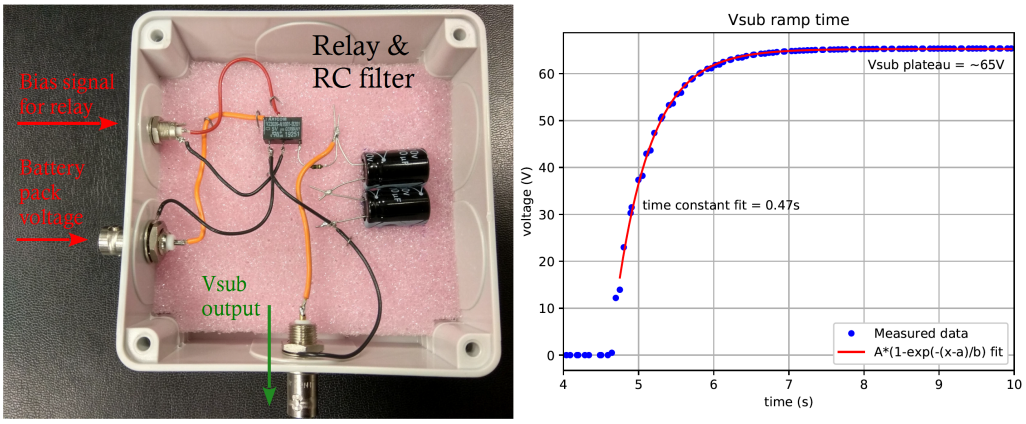

Figure 3.8: Left: Photo of the relay and RC filter for V_{sub}. Right: Plot of V_{sub} ramp with fit.

few seconds. An erase is recommended to be executed when a CCD is first turned on and after a long time of CCD operation that holes could collect at the interface.

Final hardware piece in the CCD acquisition system is the so called *second stage board*. This board is quite simple and has two tasks: front-end amplification of the video signal and shaping the delivered clocks to the CCD by introducing RC filters with a different time constant for different groups of clocks. The shaping of the clocks is necessary, as described in the previous chapter, for the reduction of the clock induced charge during the charge transfer. The waveforms of a full set of clocks for a 3-phase skipper CCD are presented in Figure 3.9. The indication "$\_X$" in the names of the clocks concerns the side in which the clocks are delivered. Since the operated CCD has 4 readout amplifiers, the vertical register is segmented to sides 1/2 and the horizontal one in Upper/Lower. This allows to read the CCD from any of the amplifiers or a combination of them for faster readout.

I would like to point out a few characteristics of the clock waveforms. The V2 of the vertical clocks (middle gate in a pixel) is usually low which means that it is the gate under which the charge is collected during the exposure phase. In the presented sequencing of the readout phase clocks, the V1 is the first to go low and share the charge with V2. So, the direction of the charge transfer for the set of vertical clocks shown in Figure 3.9 top will be V2 $\rightarrow$V1 $\rightarrow$V3 $\rightarrow$V2 for side 2. The width of the vertical clocks is in the order of a few tens of μs. The horizontal clocks operate in the same principle with a direction H2 $\rightarrow$H3 $\rightarrow$H1 $\rightarrow$H2 for side L (Figure 3.9 middle). They are quite faster than the vertical clocks, with a width of a 1-2 μs. As for the readout clocks, they are very fast and sharp. The conditions the clock rails must fulfil, described briefly in the previous chapter, can be verified on the waveform plots. For example, both of the OG rails are in between the SW rails. Of course, there is not a single configuration in which a CCD is properly operated. However, it is important to perform studies to find an optimal configuration that introduces the lowest possible CIC.

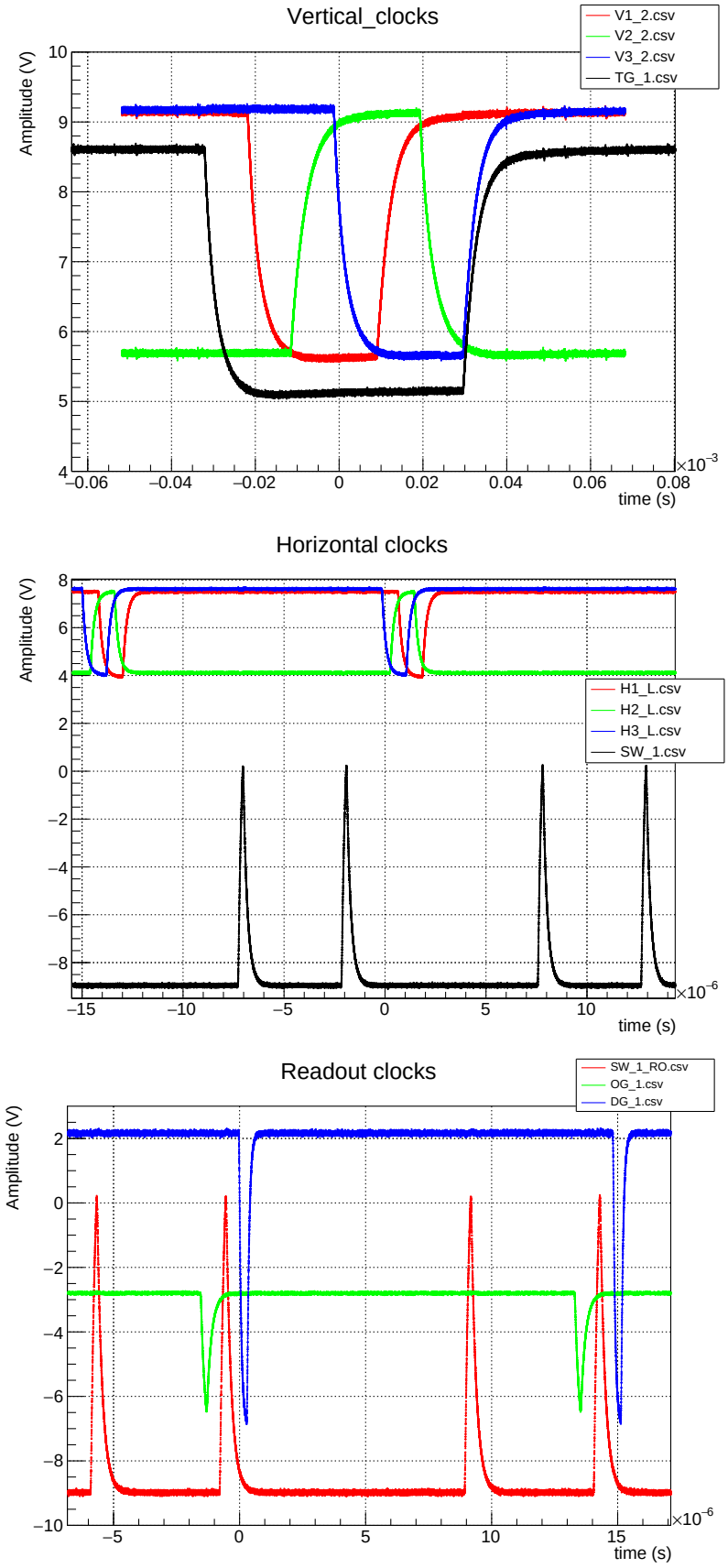

Figure 3.9: Clock waveforms for a skipper CCD with 4 readout amplifiers.

A full CCD setup requires special cables or a single complicated one to deliver all the external signals to CCD though one single connector and the video signal of the CCD to the Leach, without introducing additional undesired noise. Flex cables are usually used inside the cryostat to connect the CCD to the vacuum-side feedthroughs. It has been observed that the bad common ground of the individual modules can cause significant increment in the readout noise, so great attention must be paid in this. This excludes the vacuum pump and the cryocooler that are considered to increase the noise when they are not electrically isolated. For this reason, the vacuum pump has been electrically isolated from the cryostat with plastic junction components in the LPNHE setup. A simplified schematic of the CCD setup using the Leach controller at LPNHE, not including the cryocooler and vacuum pump, is shown in Figure 3.10.

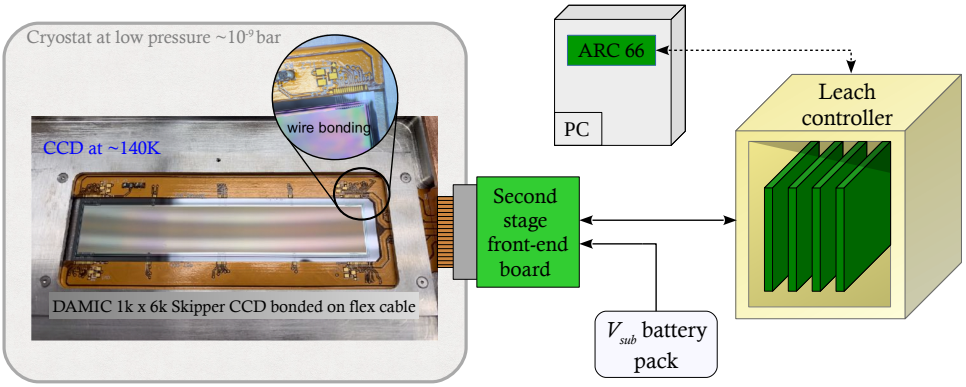

Figure 3.10: Simplified schematic of a CCD setup at LPNHE using the Leach controller, not including the cryocooler and vacuum pump.

Most recently, an $1\text{k} \times 6\text{k}$ pixel skipper CCD was installed in the LPNHE setup. The CCD was placed in a vertical cryostat operating at a temperature of $\sim$145 K. Figure 3.11 shows an example of the sub-electron resolution that is achieved with that DAMIC-M CCD, with a very good separation of the single electron peaks. The coefficient constant

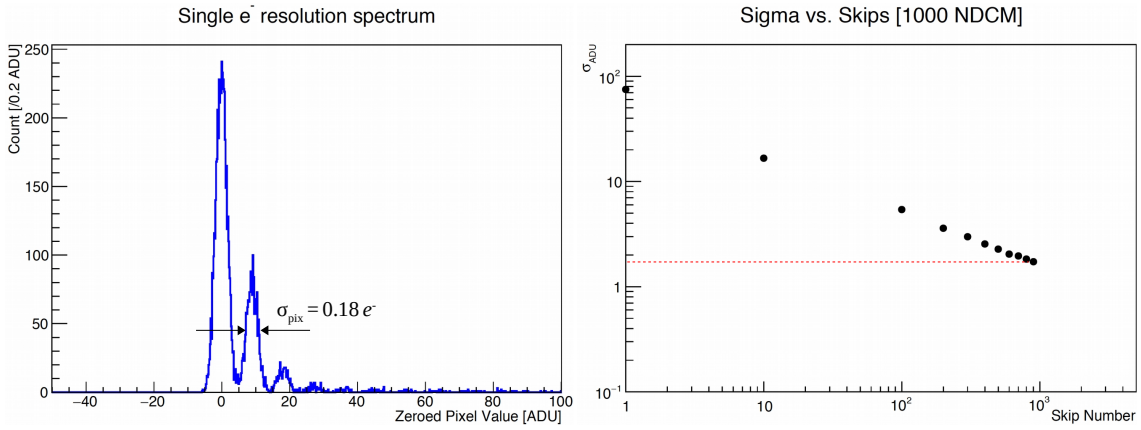

Figure 3.11: Sub-e^- resolution achieved with a skipper CCD at LPNHE. The CCD data of this figure were acquired with a 10 μs integration time and a 1000 NDCM. Left: Single electron peaks with a sigma of 0.18 e^-. Right: σ_{pix} as a function of the NDCM in ADU.

that converts the measured electrons to ADU is obtained by the distance of two successive electron peaks, and in the LPNHE setup is usually $\sim$10 ADU/e^-. These plots result from an integration time of 10 μs and 1000 NDCM. The pixel noise for a single-skip image is about 7-8 e^-, but for 1000 skips it becomes 0.18 e^-. The best pixel-noise that has been achieved in LPNHE with a skipper CCD and 1000 NDCM is 0.07 e^-. A dark current level $\sim$0.03 e^-/pixel/d was measured in this setup and stands the best among the DAMIC-M prototype CCDs that are operated in the different labs of the collaboration at surface level.

On March 31, 2022, a complete, yet only a preliminary version of the DAMIC-M acquisition system with a 4CABAC board, a DCA and an LTC2387-18 ADC board recorded the first CCD images with visible particle tracks; further discussion in Chapter 4.

3.5 Low Background Chamber

Prior to the DAMIC-M detector, the collaboration decided to install a smaller test detector at LSM, called Low Background Chamber (LBC). The detector preliminarily started its operation in February 2022 (see Figure 3.12). Two new large 4k $\times$6k pixel DAMIC-M CCDs are installed in the detector with a total mass of 18 g. Each CCD has 4 skipper amplifiers. Two Leach acquisition systems, similar to the one in LPNHE described in the previous section, control the CCDs in this first round. The goal of the LBC in terms of background is to achieve about 1 d.r.u., 1/10 of that in DAMIC at SNOLAB. The objectives of this detector is to characterize the new DAMIC-M CCDs, measure their intrinsic background and their readout noise with the skipper amplifier for the first time in an underground laboratory, test the new electronics, and produce the first scientific results of the DAMIC-M collaboration.

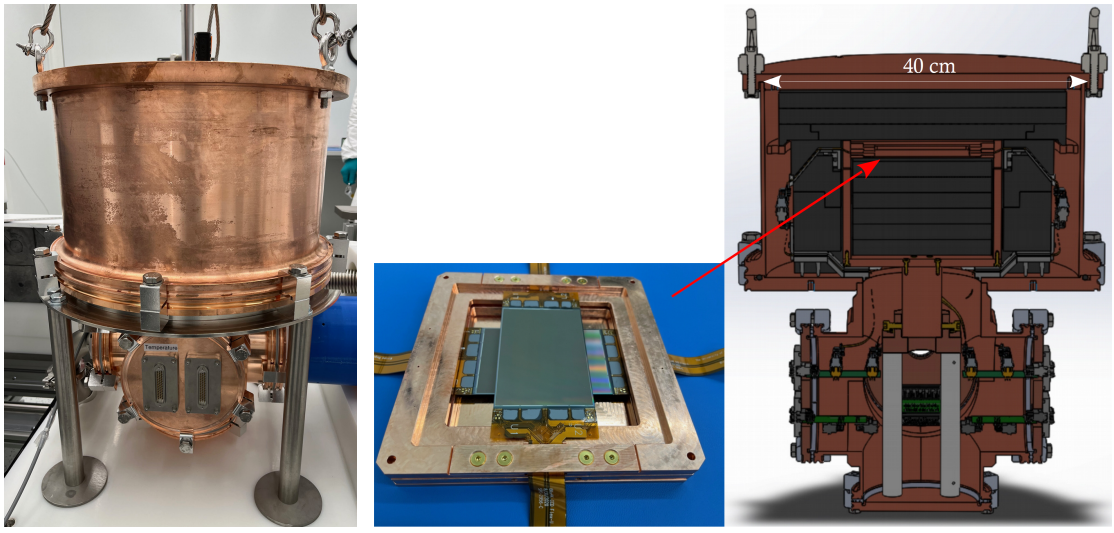

Figure 3.12: Left: Photo of the LBC detector closed. Right: Photo of the two 4k $\times$6k pixel CCDs that are installed in the detector and their position shown in a cross section of the LBC design.

3.6 DAMIC-M expected sensitivity

The DAMIC-M expected sensitivity has been calculated for a full year of exposure. Considering 1 kg of target mass, it results to an exposure of 1 kg·y. The expected sensitivities for this exposure for spin-independent WIMP-nucleon interaction, including the Migdal effect sensitivity, WIMP-electron interaction for a light or heavy mediator, and the kinetic mixing parameter vs the mass of the dark photon, assuming that the dark photon constitutes all of the dark matter, are presented in Figures 3.14, 3.13, 3.15 respectively.

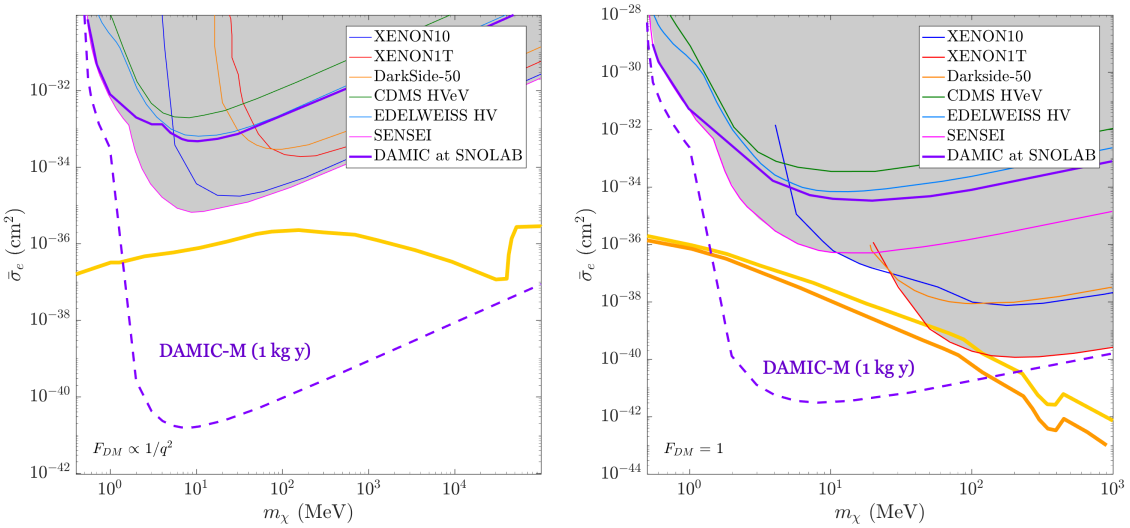

Figure 3.13: DM-electron cross-section vs the DM mass for light (top) and heavy (bottom) mediator.

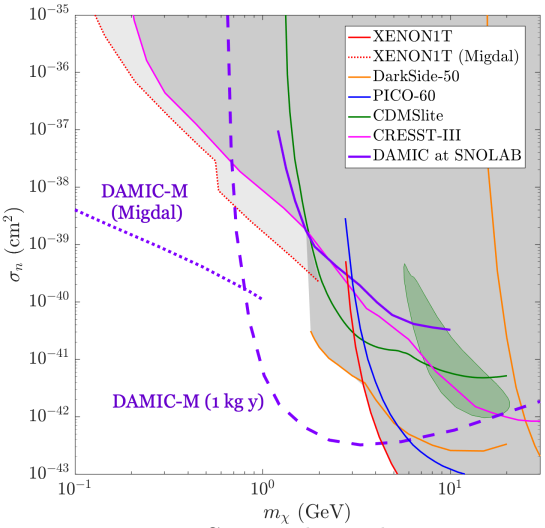

Figure 3.14: Spin-independent WIMP-nucleon cross-section vs the WIMP mass.

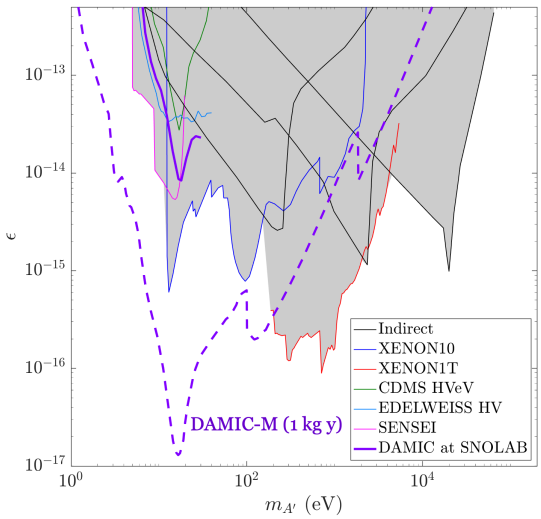

Figure 3.15: Kinetic mixing parameter vs $m_{A'}$ assuming that the dark photon constitutes all of the dark matter.

Chapter 4

Control board

The control board provides all the necessary signals to a CCD for its operation. The design of this component was taken over by the Paris group of the collaboration. The *CABAC2* (*Clocks And Biases ASIC*[1] *for CCD v2*) chip was chosen to be used for the production of these signals on an electronic board with a sufficient number of chips to support a skipper CCD with 4 amplifiers.

4.1 CABAC2 chip

The CABAC2 (or simply CABAC) chip was originally designed for the LSST experiment to control the CCDs of the telescope, even though it was not used at the end. Figure 4.1 shows a synoptic schematic of the inputs and outputs of a CABAC chip. There are four power supply input voltages for the chip that can vary depending on the necessities of its output. The are not shown in the schematic below. Starting from the chip output, it

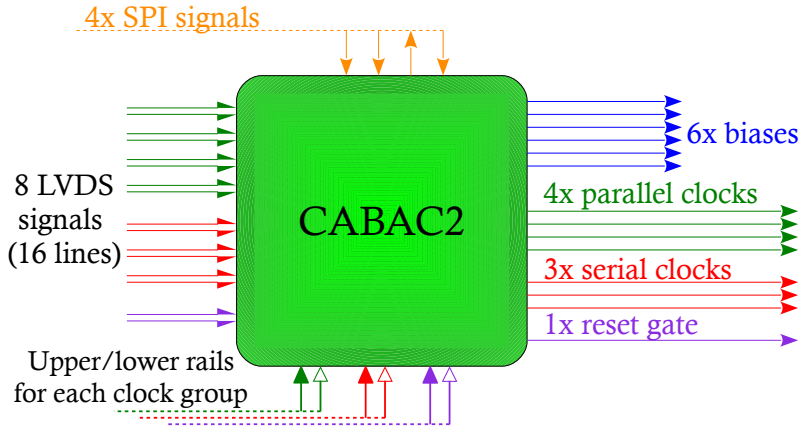

Figure 4.1: CABAC chip input and output, not including power supply

can produce 3 groups of single-ended clocks: 4x parallel (PC0/1/2/3), 3x serial (SC0/1/2) and 1x reset gate (RG). These groups differ in the current capability, which is related to the rise and fall slopes of the clock. The current for each clock is programmable with an

[1] ASIC: Application-specific integrated circuit

8-bit DAC, with a maximum of 400 mA for the parallel clocks and 60 mA for the serial and RG clocks. The clocks of a group all share the same rails that must be provided to the chip as input. The extreme acceptable values of the rails depend on the power supply. Usually, we let them span in the range of ±20 V. The upper rail must strictly be higher than the lower for every clock and the amplitude cannot fall under 4 V[2], or the chip can be damaged. To produce lower than 4 V amplitude clocks, an amplification circuit can be included at the output of the CABAC clocks on a control board with a gain below 1. This way, even though the chip outputs a clock of a minimum 4 V amplitude, the output of the board can be for example 2 V with a gain equal to 0.5. Each clock is individually triggered with Low Voltage Differential Signaling (LVDS) [108]. Finally, the CABAC chip outputs 6 bias voltages sourced by 10-bit DACs. Namely the 6 biases are called *OD_0*, *OD_1*, *GD*, *RD*, *OG*, and *SPARE*. The range is again defined by the power supply, and usually spans in the +/-20 V range.

The chip communicates and is programmed through a Serial Peripheral Interface (SPI) protocol [109]. The SPI is based on 4 logic signals which are single-ended with levels of 0 V and +3.3 V. 3 of them are inputs and 1 is output:

- SCLK (input): serial clock driven by the master
- MOSI (input): Master-Out Slave-In, serial data input driven by the master
- MISO (output): Master-In Slave-Out, serial data output driven by the CABAC
- nSS (input): Slave Select (aka CS: Chip Select), when low allows the master to write a new command in the slave register or returns the slave's status

A detailed description of the programming of the CABAC chip can be found in Appendix A.

4.1.1 Single CABAC chip evaluation

Before soldering any single CABAC chip to a board, first we test it in an evaluation setup to characterize its performance. At this R&D phase the evaluation is quite general, looking for a consistent behaviour of each chip that is in agreement with what the expected, without too detailed measurement of noise or calibrating small variations from chip to chip. Later on, more than a hundred of chips will be used for the final setup, and a new evaluation setup will be built to make precise and consistent measurements in an automatic way. The current setup utilizes a digital multimeter to measure the bias outputs and two oscilloscopes to record the waveforms of the clocks in order to measure the rising and falling edges. Some representative plots for the different measurements for 3 chips (namely 9,10,11) are shown below.

In the evaluation setup of a single CABAC chip, the biases span between -15 V and +20 V. Figure 4.2 shows the calibration of the biases for a given DAC code. Above a DAC code of 700, the CABAC bias output is saturated because of the power supply that is

[2]The minimum 4 V amplitude is a chip specification and not a CCD operating condition.

voltage used. The lowest value around -15 V is excluded from the linear fit, only to make sure that it is not affected by any saturation.

Figures 4.3, 4.4, 4.5 show the calibration of the current capability for the rise and fall slopes of the clocks for 3 CABAC chips, with representative capacitors to mimic the CCD gate capacitance of 22 nF for the vertical clocks, 180 pF for the horizontal, and 100 pF for the RG. The parallel clock slopes can be as long as a few μs. About one order of magnitude lower are the slopes of the serial and RG clocks that can vary from a few 10 ns up to a few 100 ns. The vertical clocks in a CCD support significantly more pixels than the horizontal clocks, which means higher capacity and more charge and as a result requires higher current capabilities. Moreover, slower slopes can suppress the CIC noise. The readout clocks are repeated more often and require sharp rising and falling edges to keep the readout period brief. The slopes follow quite well the $\frac{1}{x}$ law. The current depends on the inverse of time, and so as expected, the higher the current capability the faster the ramp of the clocks. A small difference is observed between the rise and fall times. This is not a major issue since for the final setup everything will be calibrated and the slopes will be set in time units and not as DAC input.

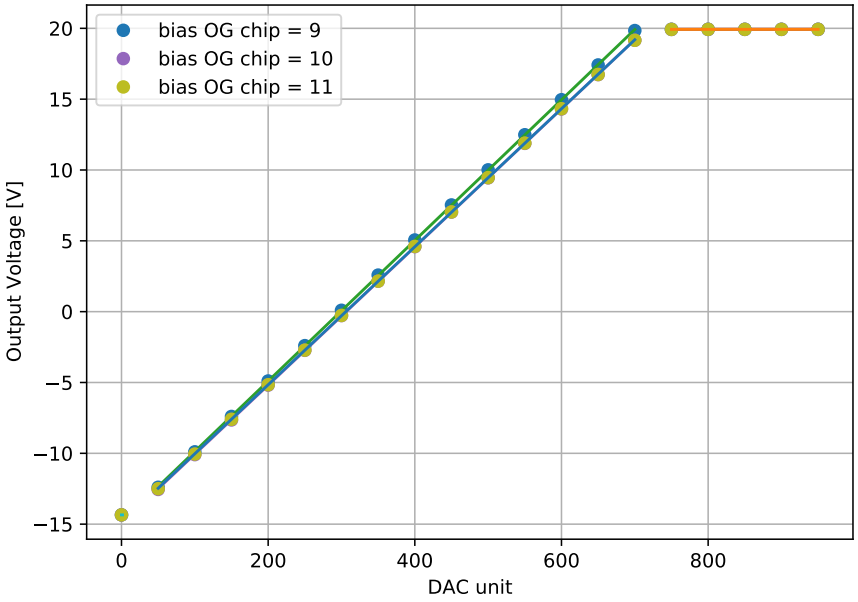

Figure 4.2: OG bias measurement as a function of the 10-bit DAC input code for 3 CABAC chips, fitted with a linear function. (Chip#10 data are barely visible due to overlap with Chip#11 data.)

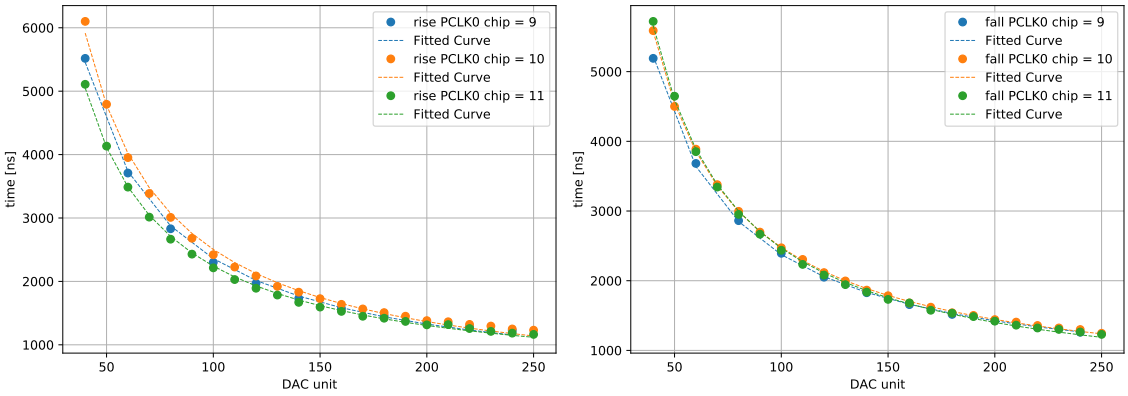

Figure 4.3: Parallel clock #0 rise (left) and fall (right) slopes measurement as a function of the 8-bit DAC input code for 3 CABAC chips, fitted with an ($\frac{a}{x}$+b) function.

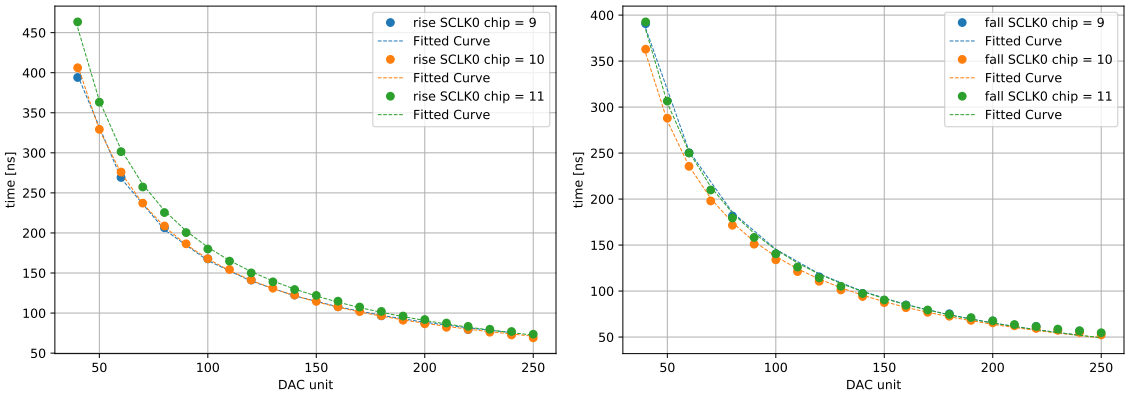

Figure 4.4: Serial clock #0 rise (left) and fall (right) slopes measurement as a function of the 8-bit DAC input code for 3 CABAC chips, fitted with an ($\frac{a}{x}$+b) function.

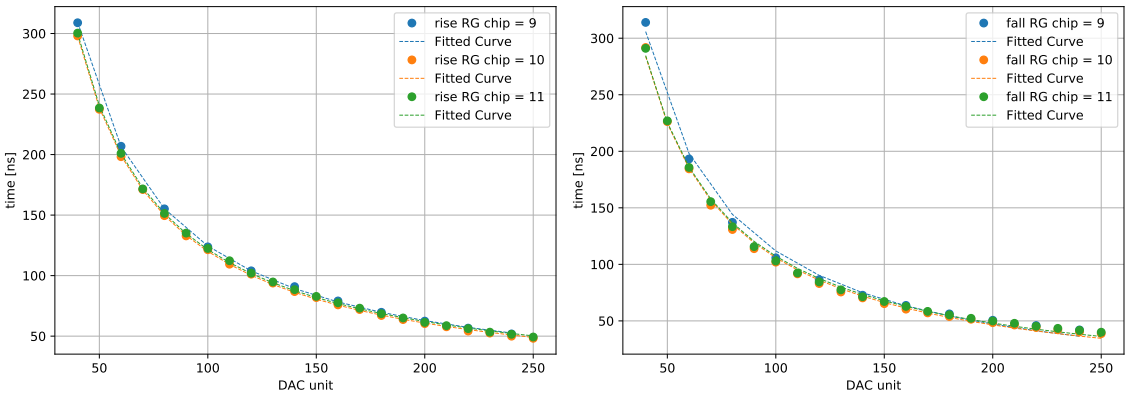

Figure 4.5: Reset Gate clock rise (left) and fall (right) slopes measurement as a function of the 8-bit DAC input code for 3 CABAC chips, fitted with an ($\frac{a}{x}$+b) function.

4.2 4CABAC control board

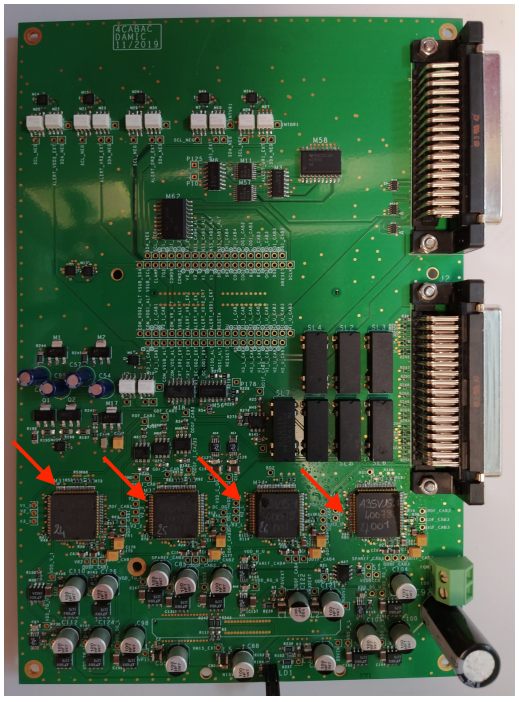

Figure 4.6: Front side photo of the 4CABAC board. The red arrows are pointing to the CABAC chips

The 4CABAC board is quite sophisticated with many capabilities utilizing 4 CABAC chips. The 4CABAC was designed to be plugged on the ODILE board with 2 HSMC connectors. Its power supply is delivered also through these connectors. The initial goal of DAMIC-M was to use 6k $\times$ 6k pixel CCDs, separated in half in both vertical and horizontal directions with a total of 4 skipper amplifiers. This design required a new control board to produce a total of 22 clocks for full control. For example, 2 triplets of vertical clocks are necessary in order to drive the charge to 2 different sides of the CCD at the same time. Given the fact that the CABAC can produce 3 groups of clocks with the clocks of each group sharing the same rails, the minimum number of CABAC chips to be used is 4. The 4 chips produce the biases for the CCD, but also the rails for the clocks. The biases from one chip are provided as rails to another or even the same one. Due to the low current capability of the bias output, however, the produced biases for rails pass through a regulator which supports the current requirements. A schematic is shown in Figure 4.7. This representation uses two layers of the 4 CABACs to show where the rails are produced and where they are delivered. The top layer concerns the bias and the bottom the clock production. Note that there are only 4 chips, not 8, and this schematic is only a mapping among the 4 chips. The necessary LVDS signals for the clock triggering are provided by the FPGA of the ODILE board and are delivered to each CABAC chip. The 4CABAC board was originally designed to allow for the production of the V_{sub} as well and monitor of the bias voltages during the operation. However, these functionalities were not properly implemented and these parts were isolated from the rest of the board. To finish with the hardware and design, the control signals are delivered to the CCD through 2 50-pin Dsub connectors on the side of the board (Figure 5.3 on the right). One of the connectors is dedicated to the 4CABAC signals going to the CCD, while the other is for the control and programming of the front-end chip (see next chapter).

The FPGA of the ODILE board communicates with each CABAC chip individually. Each CABAC chip has its own Slave Select line from the FPGA, and so only one CABAC chip is programmed at a time. The message that is sent by the user is a 28-bit word, where the last 24-bit word is the message for the CABAC as described in the previous section. The first 4 bits are devoted to defining which of the four CABACs is the message

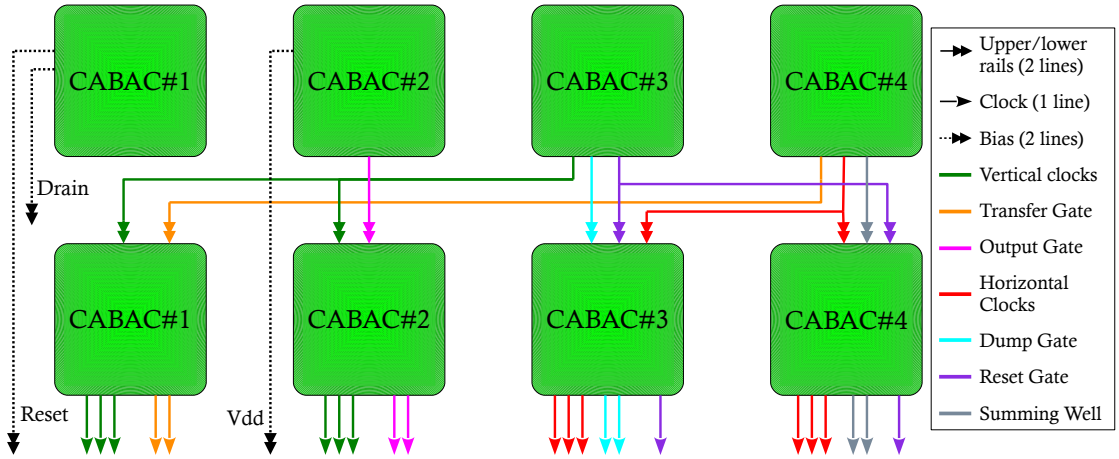

Figure 4.7: Complete mapping of the 4CABAC board in a two-layer representation of the bias (top) and clock (bottom) production.

referred to. The FPGA decodes this information and then allows the communication with the right chip.

As mentioned before, the user communicates with the 4CABAC board with an interface software written in Python. The development of this code required deep understanding of the programming of the CABAC chip, in order to create a user friendly top-level communication to control the hardware. The Python software allows the user to program the 4CABAC board, readback what is written in the register of each CABAC chip or the 4CABAC-related memory in the ODILE FPGA and load a sequencer file which basically defines a set of functions for the CCD operation. I contributed a lot in the development of the Python software and the production of the sequencer file. To create a sequencer requires knowledge of the CCD operation in detail as described in the second chapter.

4.2.1 CCD sequencer

A unique language for the sequencer was developed originally for LSST[3]. The sequencer file defines how the clocks will alternate in order to control a CCD. During my work, I have prepared several files for our current systems and a preliminary version to control a DAMIC-M CCD. It consists of a few basic fields. First, constant variables can be defined as integer numbers or with time units, which can help keeping a highly organized environment. Then, there is the definition of a maximum of 32 clocks. This is a software mapping where each of the 0 to 31 channels is named after a CCD clock. The main blocks of the sequencer file are the functions and the subroutines. The functions are the most basic bricks where the sequencing of the clocks is defined. Each can have a maximum of 16 slots with a time duration and a 32-bit word that determines the state of the clocks for the respective period. For a bit at 0 or 1, the clock rests at the low or high rail respectively. Some basic functions are the single-pixel vertical or horizontal transfer,

[3]The documentation of the LSST REB Sequencer Language can be reached here.

single charge measurement, pixel-charge dump etc. There is an optional group of variables, called pointers, that point to a function or subroutine, or to an integer repetition number of a function or a subroutine. Contrary to the constants, they can change while running the software and operating the system. An example of a vertical transfer is presented in Figure 4.8. The active clocks in this function are defined first and their state changes

```
Vtransfer12:    # One pixel vertical transfer towards both sides 1 and 2
    clocks:     V11, V21, V31, TG1,   V12, V22, V32, TG2
    slices:
        100 ns =  1,   0,   1,   0,     1,   0,   1,   0    # side_1: V2 to V1 to V3 to V2 to V1
        TVpart =  0,   0,   1,   0,     1,   0,   0,   0    # side_2: V2 to V3 to V1 to V2 to V3
        TVpart =  0,   1,   1,   0,     1,   1,   0,   0
        TVpart =  0,   1,   0,   0,     0,   1,   0,   0
        TVpart =  1,   1,   0,   0,     0,   1,   1,   0
        TVpart =  1,   0,   0,   0,     0,   0,   1,   0
        TVpart =  1,   0,   1,   1,     1,   0,   1,   1
    constants: H1L=1, H2L=0, H3L=1, SW1=0, OG1=1, RG1=1, DG1=1,   H1U=1, H2U=0, H3U=1, SW2=0,
    OG2=1, RG2=1, DG2=1
```

Figure 4.8: An example of a sequencer function that performs a single pixel vertical transfer to both directions of the vertical register.

depending on the following time-slices. The duration of a time-slice is defined before the equal sign either as a value with time units or by the name of a predefined constant, here "TVpart". The time unit/resolution of the time-slice is 10 ns for the ODILE board. There is a fixed deterministic latency 10 ns and 20 ns on the execution of first and last timeslice of each function respectively. The sequencer file must be written with this information taken into account or a short loss in the duration of each function will be observed. The clocks that are not alternated in the function can be defined in the last line of "constants". The sequencer certainly requires knowledge of the physical orientation of the clocks/gates in order to have a proper sequencing and drive the charge successfully to the amplifier.

The subroutines can call on these functions creating a more complete operation. The subroutines can also call on other predefined subroutines. An example is shown in Figure 4.9 with the name "ReadHregister". A vertical line is transferred to the horizontal register which is readout pixel by pixel. The subroutine "ReadHpixel" performs of a single pixel horizontal transfer which is followed by a single charge measurement repeated *Column*-times (NDCM) and finally the charge is dumped. A maximum of 16 functions and 16 subroutines can be defined.

```
# Move a line from the V-register to the H-register and perform readout
pixel by pixel.
ReadHregister:
    CALL @Vtransfer                # Call a function using a pointer.
    JSR ReadHpixel repeat(Columns)  # Call and repeat a subroutine.
    RTS # return to the "Main" sequence.
```

Figure 4.9: An example of a sequencer subroutine that performs a vertical line transfer and then the readout of the horizontal register.

There are four types of pointers: function pointers, function repetition pointers, subroutine pointers, and subroutine repetition pointers. The function or subroutine pointers are practically variables that substitute the original names of the respective object and

can change at any time during operation. The repetition pointers are integers, do not belong in the constant variables, and can only be used to loop functions or subroutines. For example, when there are several amplifiers on a skipper CCD, like ours, and there is more than one function that describes the vertical transfer defined in the sequencer file, a pointer can easily change the direction of the charge transfer from one side to another or change the number of NDCM repetitions in a skipper readout. Irrespectively of the type, a pointer is always called using an before the name, like the example of $Vtransfer$ in Figure 4.9. There is a special predefined subroutine pointer in the software called "Main", which can point to one subroutine at a time. The system always executes by default this "Main" sequencer when requested by the user to "start exposure" with the respective command.

Overall, there are very few states at which a CCD can be. Let us consider a CCD setup that has been just turned on. At first, it is suggested to perform an erase procedure to remove any residual image in the CCD. The CCD should not remain in a still state or charge due to incident particles and dark current will accumulate in the pixels reaching saturation. For this reason, whenever the CCD is not exposed or readout, the charge in the pixels should be flushed. This clocking state is very similar to the readout, just faster since there is no actual measurement and as soon as the charge reaches the amplifier it is dumped. The software allows for the execution of a subroutine in an infinite loop. Of course, there is also a way to stop the infinite loop and continue with another subroutine. A CCD can remain in the infinite-flush for several days, even though it is recommended to power down the system if it is not used for long periods. The main purpose of a CCD is the image acquisition, which is accomplished by the exposure and the readout. After a single (or multiple) image acquisition, the CCD can return to the infinite flush state until the user decides to record a new one.

The sequencer file can be visualized and at the same time be checked for bugs at a website[4] that simulates the clocks. Such an example is shown in Figure 4.10. Note that the sequencer file is only able to define the state of the clocks, but not their rail levels. This part of the sequencer shows the readout of a single vertical line with 2 horizontal pixel transfers and 5 NDCM. After each pixel measurement, the charge is dumped. The time scale is also in the correct order. There is no y-axis to show the rails of the clocks because this information is not implemented in the sequencer file. Recall that only the state (high or low) of the clocks is defined here. As mentioned in a previous discussion, the measurement is achieved by an ADC and additionally there is a front-end amplifier, the CROC for the DAMIC-M new acquisition system. The necessary signals for the CROC are produced by the FPGA and are also defined in the sequencer, but they are missing from this figure.

A full sequencer file for the original concept of a 6k $\times$ 6k pixel CCD with 4 amplifiers

[4]https://lsst-camera-dev.slac.stanford.edu/SequencerWebLibrary-1.0-SNAPSHOT/

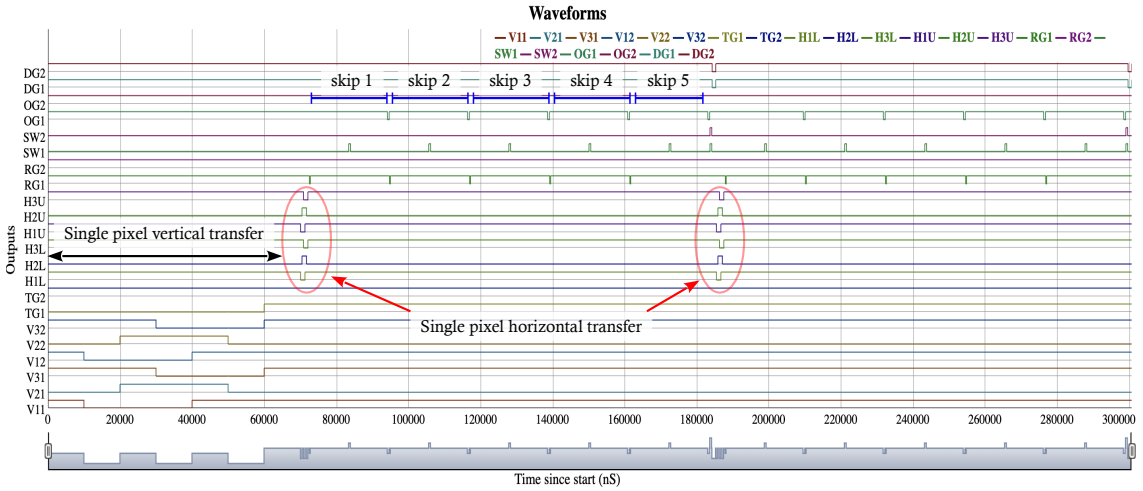

Figure 4.10: Visualization of a sequencer file with one vertical pixel transfer, two horizontal and 5 NDCM, based on a skipper CCD with 4 readout amplifiers.

contains 3 functions for vertical transfer: towards side 1, side 2 and both sides at the same time. Similar case stands for the horizontal transfer and the readout sub-functions with one or more amplifiers performing readout at the same time. The use of only a handful of pointers allows the user to keep all the options available without re-uploading new sequencer files. Still, the maximum of 16 functions must never be exceeded. The readout is performed with a single function that moves the charge from the SW to the sense node and after the measurement it sends it back. After the requested number of measurements, another function takes the charge from the SW to the drain voltage for dumping. The continuous flush is defined as a function because only function can be executed infinitely. So, there are only 16-slots to define the steps of an infinite loop and this it is impossible to flush the charge pixel by pixel in a single function. Therefore, the infinite flush function performs a single pixel vertical transfer and single horizontal one. As a result, the charge of several pixels will merge in the horizontal register before it is flushed completely. This is not problematic in normal conditions, since the charge in a continuously flushed CCD is not much and this overlap of charges should not in principle reach pixel saturation. In any case, after a period of infinite flushing, there is a subroutine defined that flushes properly the whole CCD once. This subroutine can be used to make sure the CCD is cleared from any charges. There are certainly different sequencers that can be tested with a CCD. Unfortunately, there was not a complete and robust 4CABAC board until the very end of my thesis and so I was not able to perform tests and try several ideas for the sequencer. I will only present here the waveforms that we have managed to produce.

After a sequencer file is loaded to ODILE's FPGA, the pointers, as well as all functions, can be readback from the FPGA's memory to verify that the sequencer is loaded correctly. This is done through commands that are sent through the C++ part of the software[5]. Some of the most often used commands are the *start exposure* ("SEX") or *abort exposure*

[5]The full list of the C++ commands can be reached here.

("AEX") that execute the sequencer or stop a running infinite loop respectively.

Most of the technicalities of the Python software are ignored from this report. There are several functionalities built in an attempt for an efficient and simple as possible code to operate the 4CABAC board. For example, the user can set a 4CABAC parameter to a desired value, and behind this process, a binary message is created with the parameter address and the given value information and is sent to the right direction through a certain port. Several safety levels exist in the code and warning messages to the user when needed. In addition, the 4CABAC board has presented multiple hardware issues that took time to be understood. From a failed resistor to missed signals and from a misunderstood functionality detail of a component to a possible bug in the software, everything required extensive investigations to be revealed and corrected.

4.2.2 4CABAC evaluation - Test sequencer board

The outputs of the 4CABAC board have test-points before reaching the 2x 50-pin connectors. However, in order to minimize accidental shortcuts and allow for automatic, repeatable and consistent tests, with or without a CCD plugged to the system, we have developed a board that connects to the 4CABAC and allows the user to program which signals to output to a measuring device or a scope. On the so called *test sequencer board* (see Figure 4.11), there are 5 output channels, 4 for the clocks and 1 for the biases. For each of the line, a programmable multiplexer receives the signals and outputs a single one to a lemo connector. An oscilloscope records the 4 clock outputs and the bias can be measured by an ADC or a multimeter. All the clocks could be acquired with 6 combinations of them.

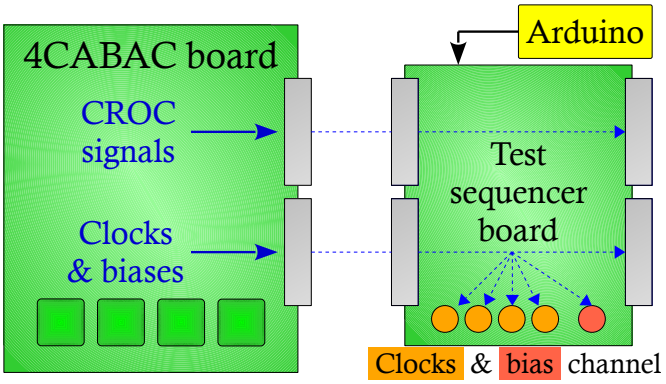

Figure 4.11: Schematic of the test sequencer board connectivity with the 4CABAC board.

The control of the multiplexers is achieved with a total of 19 logic signals sent as inputs by an Arduino Mega 2560. A .ino file is developed and loaded to the Arduino with a mapping of the signals and the logic signals, and simple functions for the choice of the signals. A specific port is opened for the Arduino communication, through which commands written in Python can call the basic functions that are implemented in the .ino file. This very convenient tool helps the evaluation of the 4CABAC board, but also can

be integrated in a CCD setup. This board can output the received signals from 4CABAC and at the same time spy on them when controlling a CCD. On the one side, there are two 50-pin Dsub connectors to plug to the 4CABAC and on the other side two more, with identical pinout to the 4CABAC, that can be used to connect a CCD (see Figure 4.11). Moreover, there are places for resistors and capacitors to test RC filters for noise reduction on the bias lines.

On 27 October 2021, we acquired an almost complete set of waveforms produced by the 4CABAC board, half of which are presented in Figures 4.12, 4.13, 4.14. Half in a sense that there are 2 identical sets of clocks for each of the sides of the CCD. The rails are not representative of an operative CCD, however the sequencing of the clocks is. Unfortunately, by that time, the production of the OG clock (referred as VOG) was not possible due to hardware issues. This is why the VOG rests at a fixed value. The symmetric to the clocks presented here, like the triplets V12,V22,V32 or H1L,H2L,H3L, have indeed the same response. The choice of driving the charge to some direction is done by the sequencing order of the clocks. The sequencing of Figure 4.12 drives the charge as V21 →V31 →V11 →V21. Similarly, in Figure 4.13, in the horizontal register the charge goes H2U →H3U →H1U →H2U.

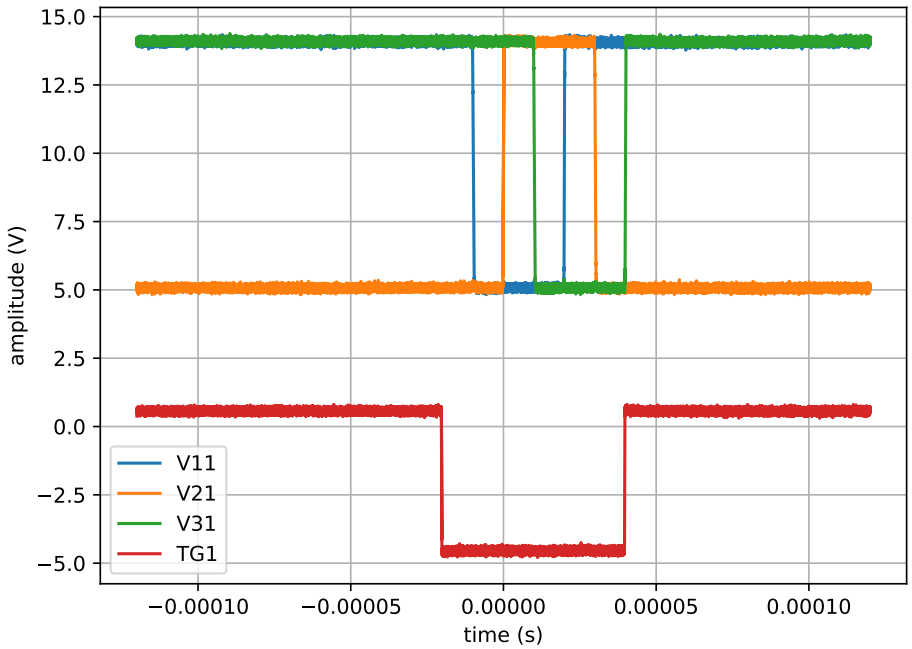

Figure 4.12: Vertical clock waveforms produced by the 4CABAC board, representing a single pixel vertical transfer.

A preliminary study on the noise of the 4CABAC outputs showed a noise level below 1 mV for all channels. The biases and rails are set in the realistic range for a CCD operation. The noise of the rails is measured from the clock output, without executing any sequencing. A capacitor is connected in series to remove the DC component of the signals. The zero-centered noise of the signals has to pass through an amplifier to become

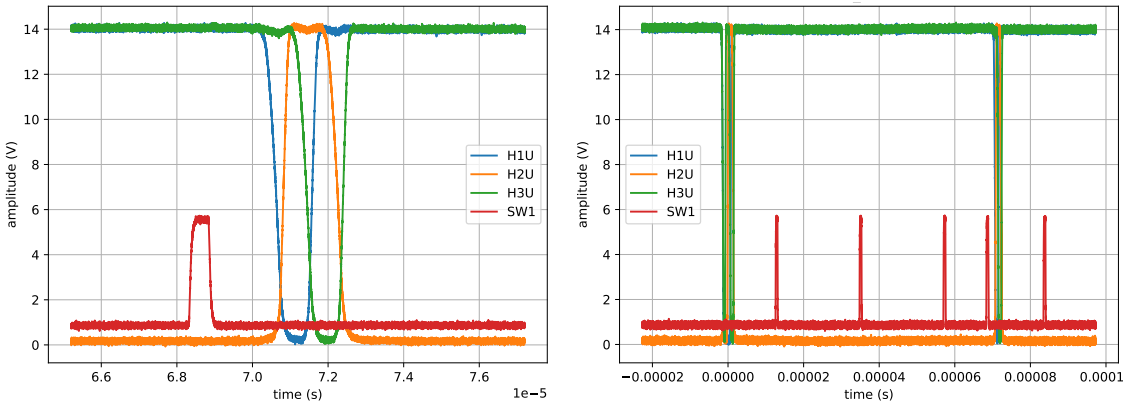

Figure 4.13: Horizontal clock waveforms produced by the 4CABAC board, representing a single pixel horizontal transfer (left) and two horizontal transfers and a pixel measurement with NDCM=3 (right). The fourth SW pulse between the horizontal clocks is only to move the charge to the sense node for the dumping.

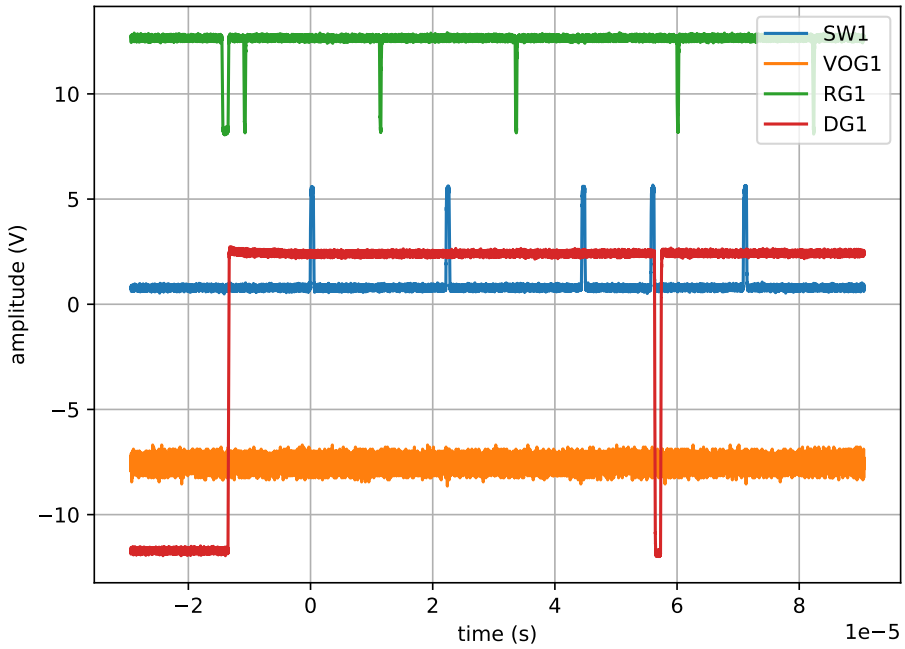

Figure 4.14: Readout clock waveforms produced by the 4CABAC board, representing a pixel charge measurement with 3 NDCM which then is dumped. OG clock is not working in this case.

larger and easier to measure with high accuracy. For this preliminary test, a CROC v1 board was plugged to the output of the test sequencer board and one new DAMIC-M 20-bit ADC (MAX11905) board was used to measure the amplified and filtered signals. The gain provided by the CROC in the mode it was operated (CF1) cannot be accurately calibrated (see next chapter) and an approximate value of 160 was considered in the analysis. Only a preliminary noise study was performed since it was accepted by the collaboration that the final design of the control board will not be the 4CABAC concept due to the many implications concerning the hardware. The noise of the individual components in the sequence, like the test sequencer board, CROC ($\mathcal{O}(1\,\mu\text{V})$), and ADC ($\mathcal{O}(1\,\mu\text{V})$), was not

subtracted from the overall noise, yet resulting to values that span from a few tens to a few hundreds of μV, without ever passing the limit of 1 mV.

All these results are at least acceptable to let the 4CABAC board drive a CCD. However, the most important result is to measure the dark current of a CCD with the new control board and compare with older systems that are used to derive a definite conclusion. A CCD setup was installed using a preliminary, yet complete, new acquisition system with the 4CABAC board, the DCA and the new 18-bit 15 MHz ADC developed by DAMIC (the last two modules are discussed in the next chapters). In April 2022, this acquisition system has successfully managed to record CCD images with visible tracks. The measured readout noise is not yet competitive to prior systems, but this setup is new and is still under optimization. Figure 4.15 shows a CCD image obtained with this prototype acquisition system. I will not dive in to any further details as the results are still very preliminary. This image is presented for the sake of the achievement of controlling a CCD purely with DAMIC-M electronics.

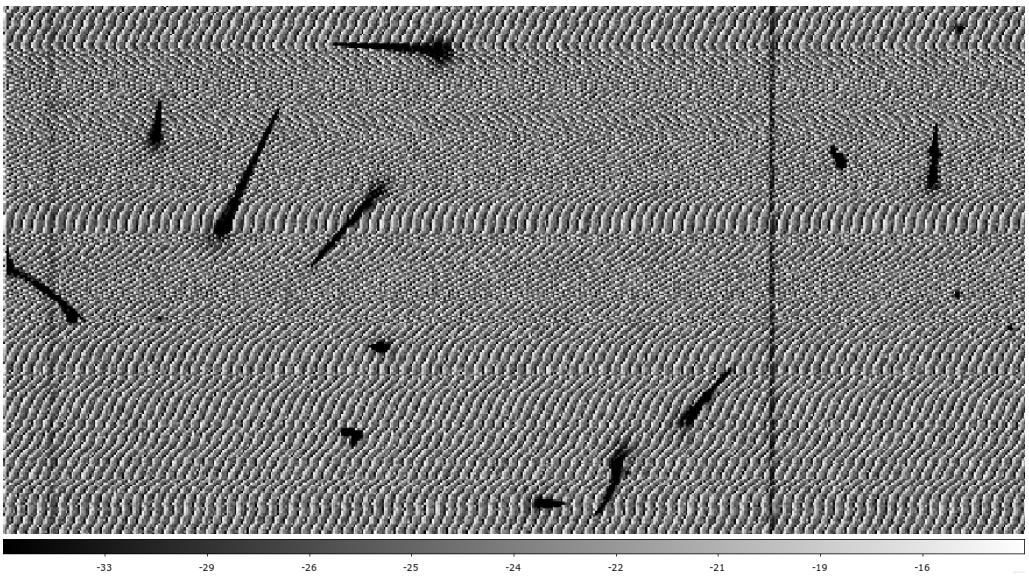

Figure 4.15: A CCD sub-image acquired using DAMIC-M new electronics: 4CABAC board, DCA front-end chip, and a new fast ADC board.

4.3 ProtoCABAC: one CABAC - one DAC prototype board

The complexity of the 4CABAC board due to recycling the produced biases for clock rails lead to a sensitive piece of hardware with several issues coming up quite often. This has forced the group to consider developing a new design where the biases as well as the rails of the clocks are produced by a 16-channel, 16-bit DAC81416[6]. This DAC was considered having the potential of being more robust and less noisy.

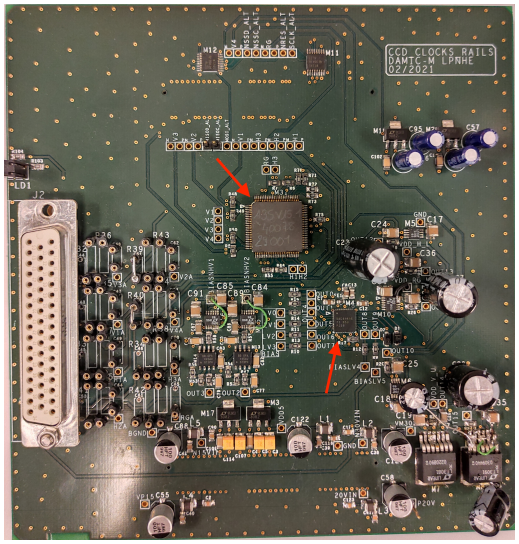

Figure 4.16: Front side photo of the ProtoCABAC board. The red arrows are pointing to the CABAC and DAC chips.

A prototype board was designed using one CABAC2 and one DAC to test the capabilities of their combination. The *ProtoCABAC* board, similar to the 4CABAC, has 2 HSMC connectors to be plugged on the ODILE board. The Python software was properly modified for the single CABAC chip and a new block was implemented for the control of the DAC. A new sequencer file was also created to match the new clocks. A new firmware was developed, adapted to the different programming of the two chips. Both are programmed through an SPI protocol, but their phases are opposite. The CABAC register captures the MOSI value at the rise edge of the SCLK while the DAC does on the fall one. This disaccord was handled with a new firmware developed for the ProtoCABAC.

The output range of the DAC is programmable and was set to the maximum ±20 V. 6 channels of the DAC are supplied to the CABAC as rails for the 3 groups of clocks, namely VDD_V_U/L, VDD_H_U/L, VDD_RG_U/L. Another 6 channels are used for normal biases directly to the output of the board, namely biaslv0/.../5. Two of the channels are used for high negative bias production, namely biasnhv1/2. Each of the DAC outputs for the negative biases pass through an amplifier with a gain of 2. With the help of a regulator after the amplifier, the output range of this channel is shifted and can span from the lowest voltage supplied to the ProtoCABAC (∼-30 V) up to +36 V with respect to that one, resulting in a range from ∼-30 V to +6 V. The two remaining channels are not used and are kept powered down. The DAC channels can be powered up/down individually. While powered down, they are connected to ground through a 10 kΩ internal resistor. This allows for safely programming the biases before powering up the channels, especially for the clock rails that a minimum difference rule must be followed. The CABAC chip as described in the previous sections, receives a total of 6 rails and a 8 LVDS signals to produce the clocks. Its biases are not used and are powered down.

[6]The reference of the DAC81416 can be reached here.

A single 50-pin Dsub connector delivers the clocks and biases. The output of this connector is compatible with the respective test sequencer board connector. A modification on the Arduino code and the respective part in the Python software allowed the use of the test sequencer board for the evaluation of the ProtoCABAC.

4.3.1 ProtoCABAC biases characterization

For the measurement of the biases, a Keysight 34470A Digital Multimeter[7] was used. With the chosen sampling configuration, the theoretical accuracy provided by the device is 30 ppm[8]. The absolute noise, then, depends on the set input range. A representative plot of a single measurement is shown in Figure 4.17. On the right side, a histogram of the distribution is presented with the mean value (red line) and the ±1 standard deviation (orange lines). The data are recorded with a frequency of 5kHz. The Fast Fourier Transform (FFT) of the acquired data presented on the bottom shows a quite flat behaviour. However, in order to acquire more detailed information, the biases must be sampled at a higher frequency to extend the x-axis of the FFT, which is limited by the Nyquist frequency. The Nyquist frequency is half of the sampling frequency.

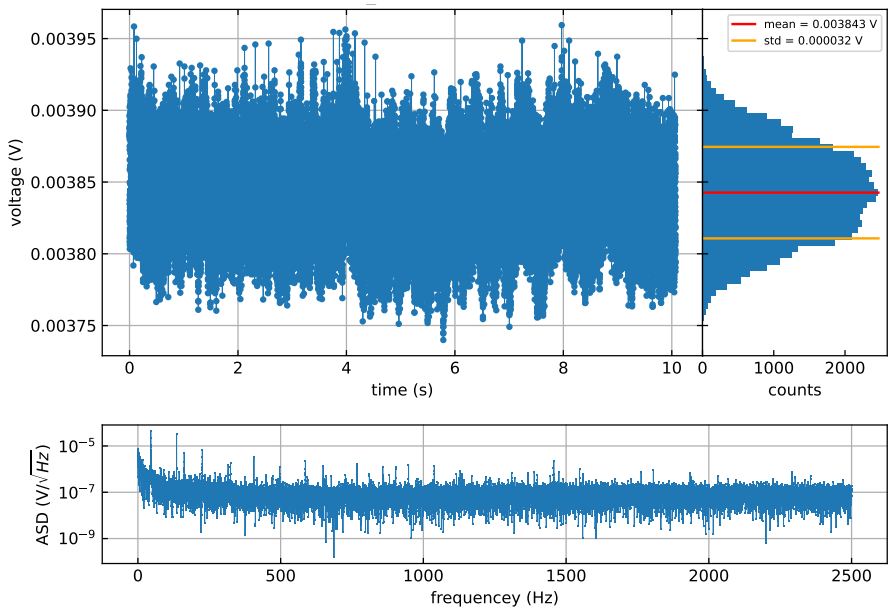

Figure 4.17: A single ProtoCABAC bias measurement with a digital multimeter. The recorded channel is biaslv5 set at 0 V. The data are presented in the top left subplot with the histogram of their distribution on the right and the amplitude spectral density using FFT plot on bottom.

Figure 4.18 shows the linearity plot of both the biaslv# and biasnhv#. Recall that the two bias types have a different output range. The distance of the measurements from the $y = x$ red dotted line is also presented in the bottom plot. The residuals of all channels show a small deviation with a linear behaviour that can be easily fitted with a function

[7] The official webpage of the product can be reached here.
[8] ppm = parts per million

and a correction applied in the software can result to a more accurate output.

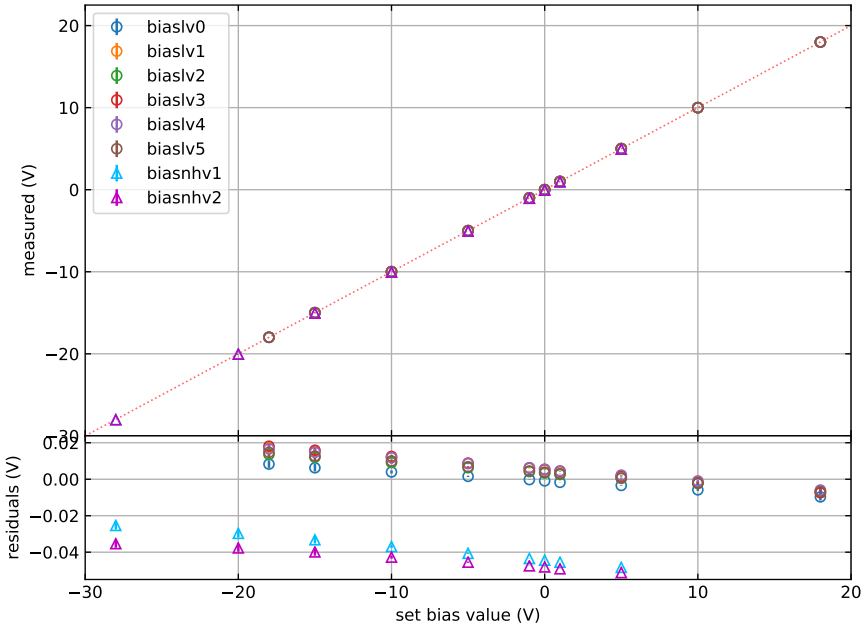

Figure 4.18: ProtoCABAC board bias linearity study. The red dotted line is a $y = x$ function, which is the reference for the residuals on the bottom plot.

The noise of the biases is also measured as the standard deviation of the distribution, shown in Figure 4.19. The resolution of the multimeter depends on the adjusted input voltage range of $\pm 10^n$ V, n = -1,0,1,2. It was measured by shorting the two inputs together with or without a 50 Ω resistor in between, without any significant difference (less than 1%). The measured resolution, shown by red dashes in Figure 4.19, is in agreement with the expected values provided by the manufacturer. The noise seems quite high, in the scale of the mV. It follows the resolution of the multimeter, but for some values it is higher than the minimum expected value. The resolution is measured when the inputs are shorted, so 0 V input, while the measured values are far from that, so it could potentially be some effect from the device and not the actual noise of the biases. For the smallest input range of ± 100 mV, all biases are set at 0 V and come with a noise below 100 μV. For a more precise study, it would have been more efficient to use a filter to remove the DC component of the biases, amplify the noise and measure it with a high resolution and high speed ADC.

4.3.2 ProtoCABAC clocks characterization

The clocks of the ProtoCABAC were evaluated primarily for the rail response with respect to the programmed value. Using the test sequencer board, the clocks are grouped in two sets: the four vertical clocks and the three horizontal ones plus the RG clock. The clocks were recorded by a Rohde & Schwarz RTM3004 oscilloscope which has four input channels. The ADC used by the oscilloscope has a 10-bit resolution, which is not sufficient for a detailed noise study, yet is enough to measure the clocks with an amplitude up to 10 V

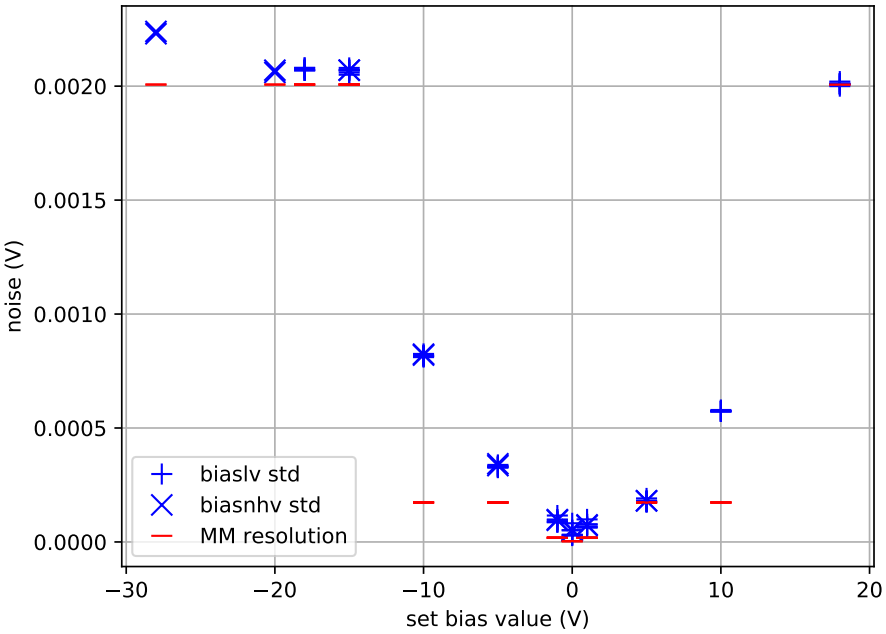

Figure 4.19: ProtoCABAC board noise study. With red dashes is presented the measured resolution of the multimeter for different input ranges, and with + and x the measurements of the biaslv# and biasnhv# respectively.

and rails in various levels in the nominal range. A typical raw plot of a measurement is shown in Figure 4.20. Unfortunately, the H1 clock was not working probably to some damage caused to the CABAC chip, but since this is a prototype board, the group agreed to proceed without changing it. The functional H2 and H3 clocks are sufficient for the characterization of the H-clocks. The low and high rails in Figure 4.20 are set to -3 V and 1.1 V respectively, with an amplitude of 4.1 V. The sequencing is similar to a vertical pixel transfer where V4 plays the role of TG and a horizontal pixel transfer with a reset pulse in every transfer. On the right, there is the histogram of the distributions with a double Gaussian fit, from which the mean value and the sigma of each clock are extracted. These values are then put in the graphs of Figure 4.18 without specifying the clock, only labelled as upper or low rails. Figure 4.21 shows the linearity response of the rails and the amplitudes for the 2 clock sets. The large error bars are due to the poor resolution of the oscilloscope. The residuals represent the distance of the measured points from the $y = x$ line. The rails have a small deviation in the order of 0.1 V, while the amplitude seems to have a quite stable offset around 0.1 V as well. A more precise study may offer the ability to calibrate all these values and correct for any deviations, if necessary. Overall, this study shows that all the clocks behave similarly and as expected from the CABAC calibration, and are accepted for a CCD control.

As for the noise of the rails, in order to measure it precisely, one needs to remove the DC component and record the rails with a high speed and resolution ADC like the new ones meant for DAMIC-M. This study is planned, yet as of April 2022 has not yet been realized. As mentioned before, the low resolution of the oscilloscope dominates and the

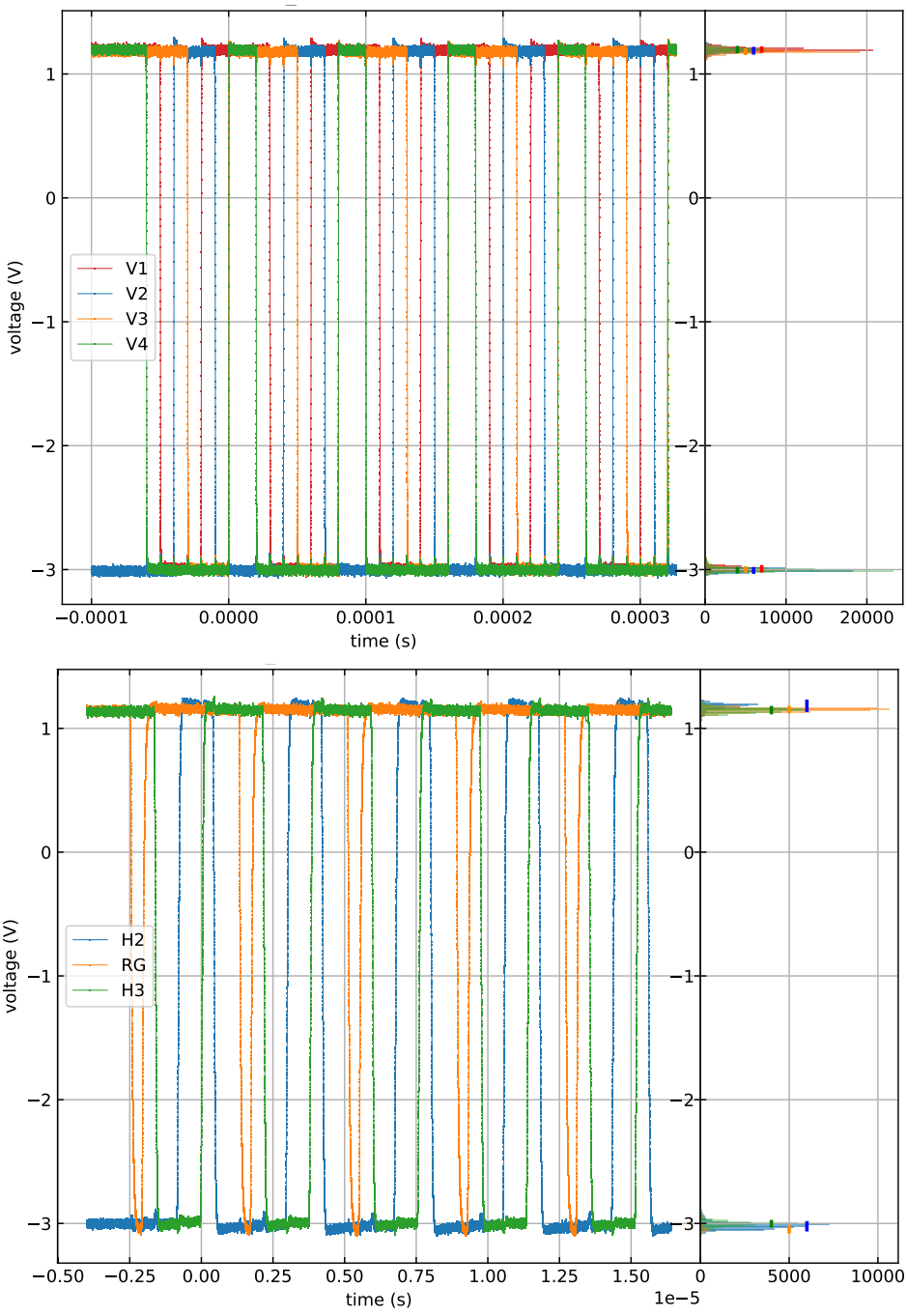

Figure 4.20: Typical plots of V-clocks (top) and HRG-clocks (bottom).

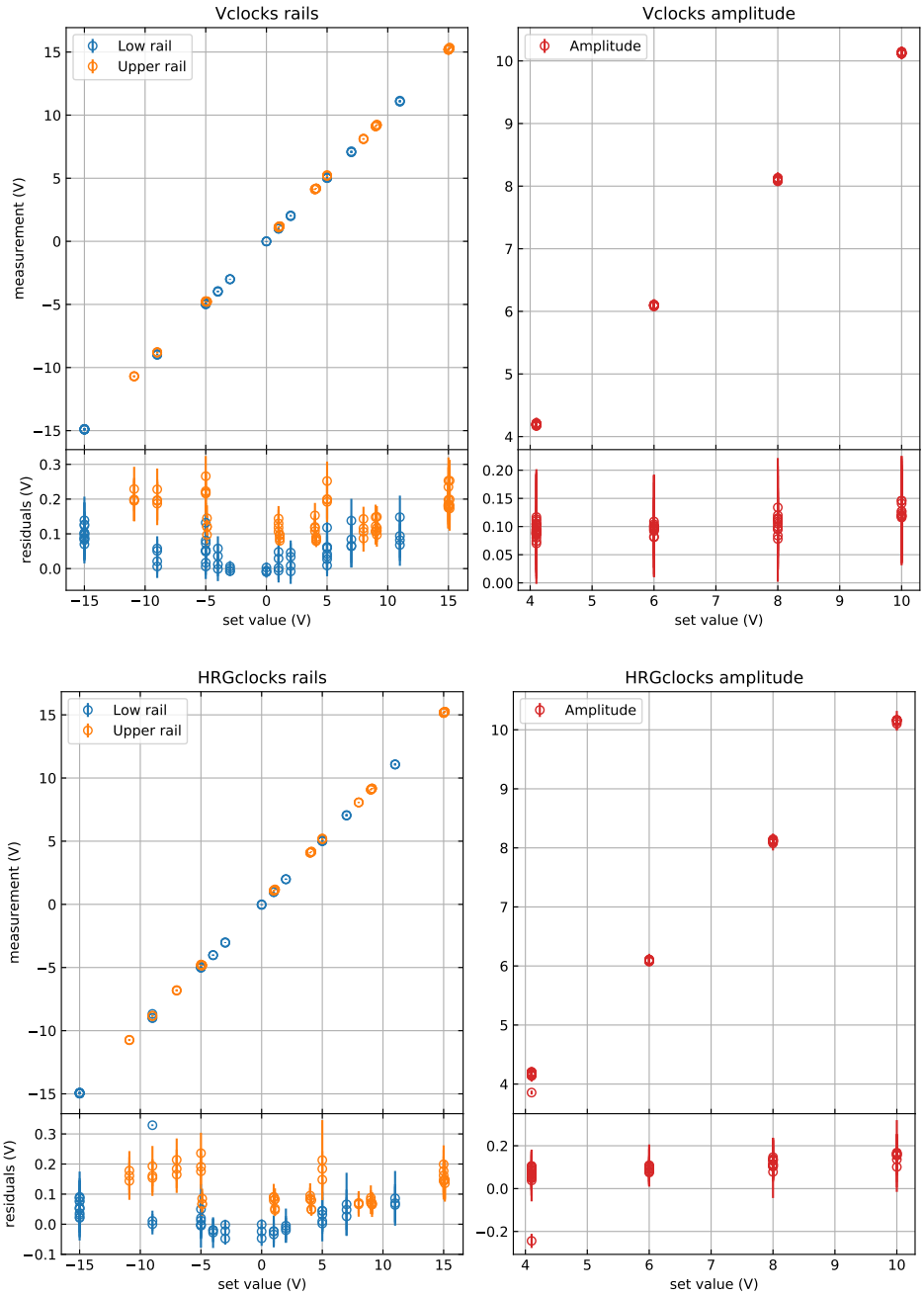

Figure 4.21: Rail (left) and amplitude (right) linearity plots of V-clocks (top) and HRG-clocks (bottom) with residuals.

noise of the rails cannot be measured accurately. Nevertheless, the highest resolution of the oscilloscope for the data presented in Figure 4.21 is for a clock amplitude below 5 V while both rails are in the range of ±5 V. The standard deviation of the distributions of these rails for suck clocks is ∼0.015 V, which is about 3 ADU for a 10-bit DAC in this range. It is definitely a hardly representative and precise result, however it can be considered a very preliminary upper limit with the actual noise expected to be even lower.

The ProtoCABAC board has places for resistors and capacitors at the output of the clocks for a divider circuit and filtering. The main goal of this circuitry is to produce clocks of amplitude lower than 4 V by attenuating the clock output, while keeping the its low rail fixed. For example, an output CABAC clock with lower/upper rails at 4/8 V, can become 4/6 V after this output stage. It will be interesting to test lower amplitude clocks with a CCD for lower dark current and thus it is necessary to make this possible with the CABAC. As of April 2022, the study of the ProtoCABAC clocks with this option applied is still pending.

Chapter 5

Front-end amplification

The CCD video signal is usually very small, in the order of $1\,\mu\mathrm{V}/e^-$, and thus it needs to be amplified to be read by an ADC accurately. In addition, during the transfer of the signal to the ADC, it can pick up noise, mainly thermal or from random electric fields. In order to minimize its impact and increase the SNR, the video signal is amplified as early as possible. This way, the effect of any introduced noise up to the digitization is reduced by a factor equal to the amplification, including the noise of the ADC itself. Such a front-end amplifier is found usually close to the CCD. This circuit adds its own noise to the signal, and so it must be very well designed for optimal results. Moreover, it must also be radio-pure to not introduce additional background. Besides this stage, the rest of the electronics can be further away from the CCD.

The front-end amplifier for DAMIC-M was named *CCD ReadOut Chip* or *CROC* and was designed by the Paris group of the collaboration. I have contributed much to the evaluation of the chip as well as to its integration in a CCD setup. However, the first CROC chip revealed some issues in its design during its evaluation that led to a second version. The v2 was designed in the same principle as v1, but actually was proved to be more problematic than the first. Despite its issues, CROC v1 was quite robust and was tested in a CCD setup. Finally, a preliminary third version of the front-end chip was designed as a much simpler amplifier and by March 2022 it was evaluated and integrated as well in a CCD setup. As a reference, recall that the CCD front-end amplifier in several surface level lab setups of the DAMIC collaboration has been a simple 4-channel board made of operational amplifiers, resistors and capacitors with a fixed amplification depending on the values of the components.

5.1 CROC: CCD ReadOut Chip (version 1)

The design of the CROC is quite sophisticated with respect to a simple amplifier, with many capabilities in an integrated chip to process the video signal in a flexible way. The first version of the CROC was developed and tested in 2019. A brief visualization of its

inputs and outputs is shown in Figure 5.1. The CROC is a 4-channel single-ended input to

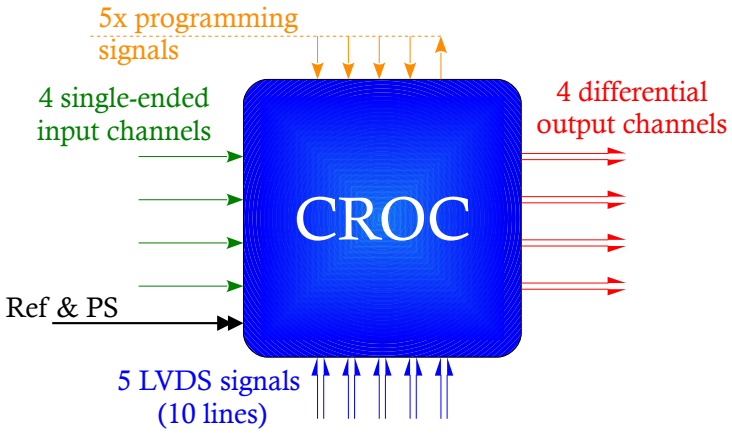

Figure 5.1: CROC chip input and output

differential output chip with programmable gain. It can operate in Transparent and Dual Slope Integrator (DSI) modes. A single power supply of 5 V, a 3.3 V digital voltage to define the logic high level and a precise and low-noise 2.5 V reference (V_{ref}) are provided to the chip externally. A total of 5 LVDS *timing signals* trigger internal switches with different actions, namely Clamp, Reset Amplifier, Ramp Up, Ramp Down, and Reset Integrator. The programming of the chip is performed through a 96-bit shift register.

5.1.1 CROC block diagram

A detailed internal look of the CROC is presented in the block diagram of Figure 5.2.

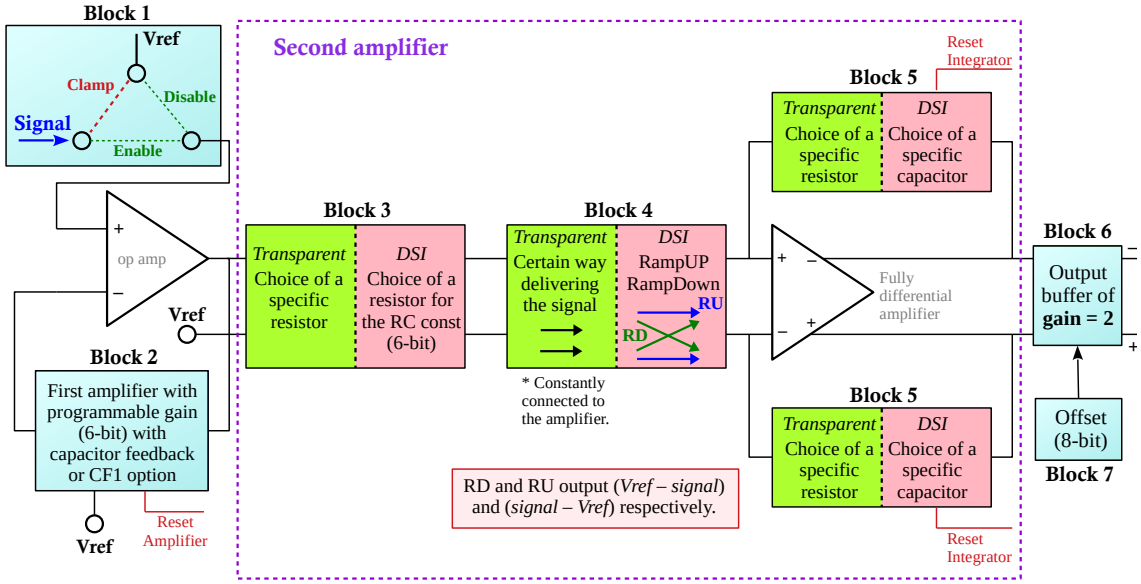

Figure 5.2: Block diagram of the CROC for a single channel.

First stage amplifier

In Block 1 on the top left corner, there is the single-ended input "signal" to the CROC. A single bit for each channel specifies if the input will be enable/disable (in green) by connecting the rest of the circuit to the input or the reference voltage respectively. This bit is presented with the name *NEN*. In normal operation this bit is fixed at the enable state. In the same block there is a switch controlled by the Clamp LVDS signal (in red), that can short the input to the reference voltage and restore the input DC of the first amplifier.

The signal then passes through the first non-inverting amplifier, which can be programmed to operate in two modes: *6-bit Gain* (referred to as Gain^{6bit}) or *CF1*. The 6 bits of Gain^{6bit} correspond to the switches of 6 capacitors connected in parallel with values of 4, 8, 16, 32, 64, 128 pF, inside Block 2. Additionally, there is always a small 2 pF capacitor connected in parallel in case none of the 6-bit capacitors is chosen (Gain^{6bit}=0). At the input of the amplifier there is a 2 pF capacitor connected in series with the Gain^{6bit} capacitors. The absolute gain of the first amplifier, G, is theoretically calculated as:

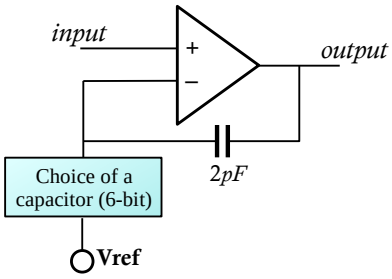

Figure 5.3: Schematic of the first amplifier in Gain^{6bit} mode.

$$G = \frac{C[\text{Gain}^{6bit}] + 2\,\text{pF}}{2\,\text{pF}} \tag{5.1}$$

The maximum absolute gain of the first amplifier theoretically will be G_{MAX}=127 for Gain^{6bit}=63, when all capacitors are connected. The capacitors can accumulate charge during operation and so there is the Reset Amplifier (RA) signal to restore the DC of the amplifier's output by shorting the negative input to the output. In CF1 mode, the first amplifier is a non-inverting follower with an expected absolute gain of 1, where its negative input is shorted to its output. Since the RA is necessary only when capacitors are involved, it is useless in CF1 mode.

Second stage amplifier

A second fully differential amplifier receives as inputs the signal and the V_{ref}. It can be programmed to operate in Transparent or DSI mode. When in Transparent mode, the second amplifier simply converts the signal from single-ended to differential, with an amplification factor of 1. A specific resistor is chosen in Blocks 3 and 5 when the CROC channel bit is set to this mode and Block 4 becomes transparent.

In DSI mode, the functionality of the second amplifier becomes more complicated. Block 3 is a 6-bit programmable resistor and Block 5 is a fixed capacitor. In this mode, the second amplifier is an *RC* integrator with a time constant equal to the product of the

resistor and capacitor of Blocks 3 and 5 respectively. With RC^{6bit} I will be referring to the option of the resistor of the integrator, while RC will correspond to the actual time constant, whose values are expected to span from 200 ns to 50 μs. The Reset Integrator (RI) signal shorts the inputs of the amplifier to V_{ref} to restore the DC level of the capacitors. Right before the amplifier, Ramp Down (RD) and Ramp Up (RU) signals control two switches in Block 4 that choose how the signals are delivered to each of the inputs of the differential amplifier. RD connects the signal and the V_{ref} to the positive and negative poles of the amplifier respectively, resulting in an input of (signal-V_{ref}). RU reverses this polarity to an input of (V_{ref}-signal). As explained in Chapter 2, the DSI measurement of the CCD pixel charge requires integrating the pedestal and the signal levels with reversed polarities. CROC has the advantage of integrating the 2 phases in a symmetric way with the same RC, so that any introduced effect from each side of the amplifier will be eliminated. The alternative would be to have two independent integrator circuits with fixed opposite polarities with a switch to choose where the signal is sent. When both RU and RD are not active, the inputs of the second amplifier are isolated from the first amplifier. The potential of the capacitors of Blocks 5 does not change, and so the output of CROC remains the same during the isolation. In a CCD operation terms, this is the moment to transfer the charge to the sense node. When both are active, the two inputs are shorted together. In transparent mode, the RD, RU and RI are of no use. The absolute gain of the second amplifier in DSI mode for DC input signals is equal to T_{int}/RC, where T_{int} is the integration time or the duration of each of the RD and RU timing signals. For more details, the gain of a fully differential integrator is explained in Appendix B.

Output buffer

After the second amplifier, there is an output buffer (Block 6) that provides an additional fixed amplification of 2. At this final stage, there is Block 7 that can provide an offset to the output signal in order to optimize the CROC output for the following ADC input range. The 8-bit Offset is a global parameter. The absolute gain of the CROC in the two modes is expected to be:

$$\text{abs gain}^{Transp} = 2G \ , \ \text{abs gain}^{DSI} = \frac{2G \times T_{int}}{RC}, \tag{5.2}$$

where G is the programmable absolute gain of the first amplifier in either 6-bit Gain or CF1 modes.

The chip was designed to control the bias current of the first and second amplifiers with two global 8-bit parameters, POL and POLIB respectively. Moreover, there has been also the option to disable the second amplifier by disconnecting the bias current of each individual channel; this 1-bit option will be referred to as V in the next paragraph. These options would allow lowering the power consumption of the CROC during the CCD exposure phase. Unfortunately, they did not seem to work properly, with no clear negative

impact to the operation of the chip.

5.1.2 Programming CROC

The CROC has no addresses, only a single 96-bit register. There are 6 parameters to program per channel with a total length of 16 bits and 3 global parameters, 8 bits each. There are also 8 bits that must be zero (MBZ). The three tables below present the structure of the 96-bit word (top), the syntax of the 16-bit word for every channel and the global parameters (middle and bottom). For the multi-bit parameters, such as RC^{6bit} or POLIB, the Least Significant Bit (LSB) is the bit <0> and the Most Significant Bit (MSB) is the maximum bit-number of each parameter.

Channel 3	Channel 2	Channel 1	Channel 0	MBZ	Global params
16-bit	16-bit	16-bit	16-bit	8-bit	3×8-bit

Channel X					
G<0-1-2-3-4-5>	CF1	NEN	RC<0-1-2-3-4-5>	Transparent/DSI	V

Global parameters		
POL<0-...-7>	Offset<0-...-7>	POLIB<0-...-7>

Table 5.1: Programming of CROC: 96-bit CROC register structure (top), 16-bit word per channel (middle), and the total 24-bit word of the global parameters.

The programming of the CROC is achieved through 5 signals, 4 sent to and 1 received by CROC. Similar to the SPI protocol, there is a serial clock (SCLK), a Master Out-Slave In (MOSI), and Master In-Slave Out (MISO) signals, but no Slave Select. The 96-bit word is sent through MOSI and the CROC captures the value at the rising edge of the SCLK at an intermediate register. At the end of the 96 clock pulses, a single pulse through the LOAD signal commands the CROC to change its internal main register with what is written in the intermediate one. In order to read the CROC register, a single pulse is sent through the READ signal and stays high during a single SCLK pulse, followed by 96 more SCLK pulses, where MISO delivers the 96-bit information.

The importance of understanding in detail the 96-bit word and how the programming signals should alternate was essential for the development of the CROC block in the Python software of the ODILE board and its integration to the new acquisition system. In addition, unless the CROC parameters need to change, programming the chip once is sufficient. In fact, the programming signals could be even disconnected. It is important to mention that the programming signals of CROC are produced from the ODILE board and delivered to CROC independently of the timing signals, such as Clamp. The last ones are defined in the sequencer of the control board. This paragraph is relevant to the CROC integration to the Leach acquisition system and the test that was performed with a CCD that is presented in section 5.4.

To offer a simple alternative for the CROC programming, I have developed a Python

code for a Raspberry Pi 4 Model B device[1]. This allows a user to program the CROC successfully and then remove the Raspberry with no issues and operate the CROC with external triggering signals. The serial clock frequency of the programming does not have to be very fast and the logic CMOS signals provided by the particular Raspberry Pi were sufficient. However, this model is not powerful enough to produce fast and robust signals, with a speed of 1 MHz for example, to be converted to LVDS and fully control a CROC chip. It may be interesting to investigate if a similar commercial and easily programmable device can be used for full control, to open the way for potential future applications.

Even with only the programming achieved, the profit can be significant. For instance, operating CROC in transparent mode requires only Clamp and RA signals or 1 LVDS signal if they are connected together, as it was the case for the CROC evaluation. As a result, an acquisition system like the Leach can implement one such signal in its sequencer and easily integrate the CROC. A more powerful piece of hardware using an FPGA was used for the evaluation of the CROC, but the development of a firmware was not trivial, and for sure not as straightforward as in Python, which allows easy access to the source code.

5.1.3 CROC evaluation setup

In the last quarter of 2019, an evaluation setup was put together for the CROC characterization at room temperature (see Figure 5.4). The CROC is placed on a board in a

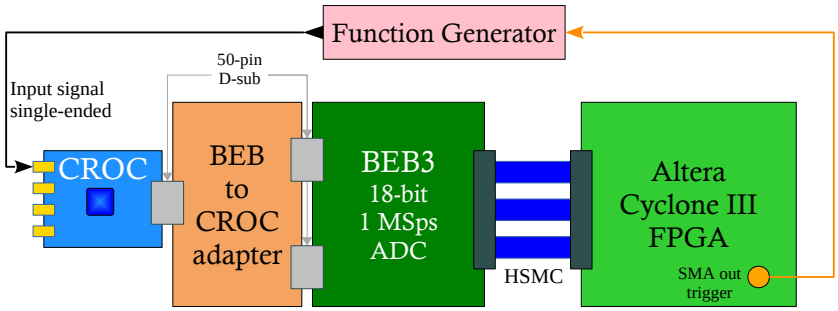

Figure 5.4: Schematic of the evaluation setup of the CROC.

convenient socket to easily change the chip, instead of soldering it. The CROC board has 4 SMA connectors to receive the input signal for each channel. It is a quite simple board with an external +5 V voltage supply and very few components besides the CROC chip. A low-dropout regulator produces the +3.3 V from the +5 V supply as a digital voltage for CROC. The +2.5 V reference voltage is produced by an LTC6655 precision reference chip, also powered by the supply voltage. The CROC board current consumption, with a v1 chip, is about 60 mA, 50% higher than expected. The CROC v1 was designed to have a consumption of 40 mA, which is already high enough to allow the chip to be very close to the CCD. Infrared photons emitted could potentially be a dominating background for

[1]The code is publicly available and can be reached here by the name "CROCsoft_v4.py".

the CCDs. Later on, the concept of placing the CROC right next to the CCD was abandoned and this level of power consumption is no longer an issue in terms of physics. The triggering and programming signals as well as the power supply of the board are received through a 50-pin Dsub connector.

The BEB3 ADC board, designed and used extensively by the group, was used to readout the CROC. It is an 8-channel differential input board using the 18-bit 1 MSps AD7982 ADC with an input range of ± 5 V. The calibration constant of the board was measured to be 21.6 μV/ADU. The +5 V power supply, the programming and triggering LVDS signals, all pass from BEB3 to CROC, through an adapter board in between, without any electronic components, which merges the signals of the two 50-pin Dsub connectors of BEB3 to a single one for CROC. The BEB3 requires 3 supply voltages of +12 V, -5 V, and +3.3 V. The CROC consumption is observed at the +12 V supply. The BEB3 is controlled by an Altera Cyclone III FPGA board[2] through an HSMC connector. An application in LabView was developed to control the FPGA board and the whole system. The sequencing of the CROC LVDS signals as well as the sampling trigger of the BEB3 ADCs are set in a user friendly interface matrix in the LabView app, similar to the sequencer described in the previous chapter, defining the duration of the time-slices and the state of the signals in each one. There are two loop levels, TS1 and TS2, with TS2 nested to TS1. Each level is repeated for an individual given number. Usually, to keep it simple, TS1 is repeated once and TS2 in the order of 100-1000 times. Each TS2 loop is considered one period of the data-taking and more details are given later for each individual study. In this particular setup, the Clamp and RA are shorted together on the CROC test board, because BEB3 can deliver up to 4 LVDS pairs. In the sequencer of the LabView app, the single controlled signal is referred to as Clamp/RA.

A Keysight 33600A Series waveform generator is used to produce signals for CROC. The generator is triggered by a signal produced by the Cyclone III board, defined as well in the sequencing. In order to mimic the video signal of a CCD, the produced signals are square pulses with programmable rails, usually in the order of few mV amplitude, and pulse width. The low and high rails of the pulse represent the pedestal and signal levels of the video signal respectively. It was shown that an attenuator after the generator or an oscilloscope spying on the injected signal may introduce significant noise to a small signal of a few mV. After synchronizing the signal with the CROC timing signals with the help of an oscilloscope, the generator is connected directly to the CROC board.

5.1.4 CROC v1 gain calibration in Transparent mode

Primarily, the CROC was tested in Transparent mode in order to calibrate the gain of the first amplifier. A square pulse of fixed amplitude of $\mathcal{O}$(mV) is injected in every period. The amplitude here is calculated with CDS. The sequencer time-slices are limited by the

[2]The user guide of the FPGA board can be reached here.

firmware and allow for a maximum of 6 samples per loop. Each level of the pulse is sampled 3 times. At the beginning of the loop, a 2 μs Clamp/RA pulse is sent to CROC. After a Clamp/RA the input of the CROC should be at the V_{ref}. It was observed not to be the case, as a great distortion similar to the reset noise of the CCD results to a changing the reference level in every loop. A visualisation of this effect is shown in the timing diagram of Figure 5.5. This effect occurs only in the 6-bit Gain option, and not when CF1 is chosen. In CF1 mode, the RA is useless since the gain of the amplifier does not use any capacitors. As a result, the problem is sourced by the RA and not the Clamp, even though they are shorted together in this test setup. The issue in the design was understood, coming from a second misplaced switch also controlled by RA.

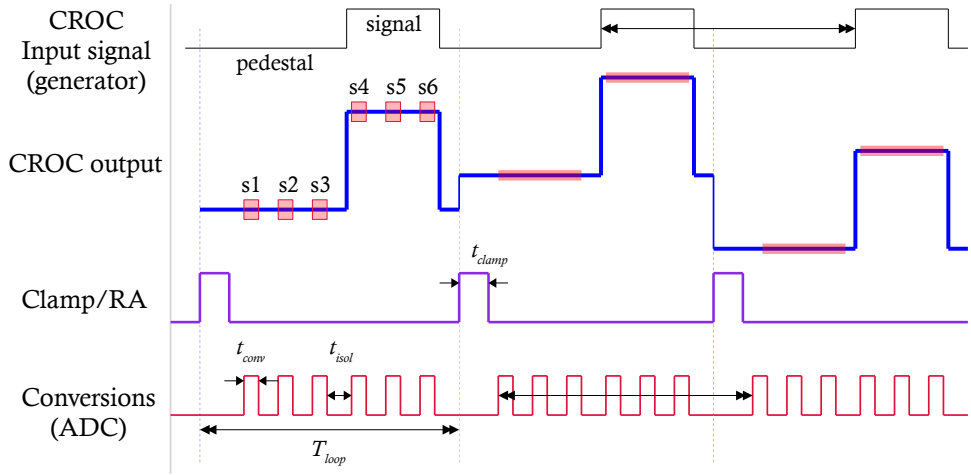

Figure 5.5: Timing diagram of CROC in Transparent mode.

First, the 8-bit Offset option (from 0 to 255) of CROC was optimized for the BEB3 input. For an Offset<100, one of the differential inputs of BEB3 is at least partially saturated. A value of Offset=120 was chosen. An example of the raw data recorded with CROC in Transparent mode and $Gain^{6bit}$ for an input square pulse signal from 0 V to 5 mV and a frequency of 50 kHz is presented in Figure 5.6 left. The first amplifier gain is small ($Gain^{6bit}$=5) to have both the pedestal and signal quite close to see clearly the previously described RA defect. On the right there is a histogram of the full distribution of the data, not only the ones presented on the left. The reference distortion results to an extremely extended distribution with a span of a few thousand ADUs and a histogram shape of a sinus wave. However, in the data analysis the pedestal is subtracted from the signal in every loop. The average of the 3 samples defines the two levels which are subtracted to obtain the pure amplitude of every pulse. Fortunately, the distribution of the amplitude is much better and Gaussian-like, with the moving RA defect removed (see Figure 5.7). The standard deviation is expressed in both volt and ADU for comparison with Figure 5.6. This behaviour is consistent for all Gain values, and the highest Gain=63 is also presented in Figure 5.7 (bottom triplet). The standard deviation of the distribution is the output noise of the measurement and will depend on the number of samples per level. Considering

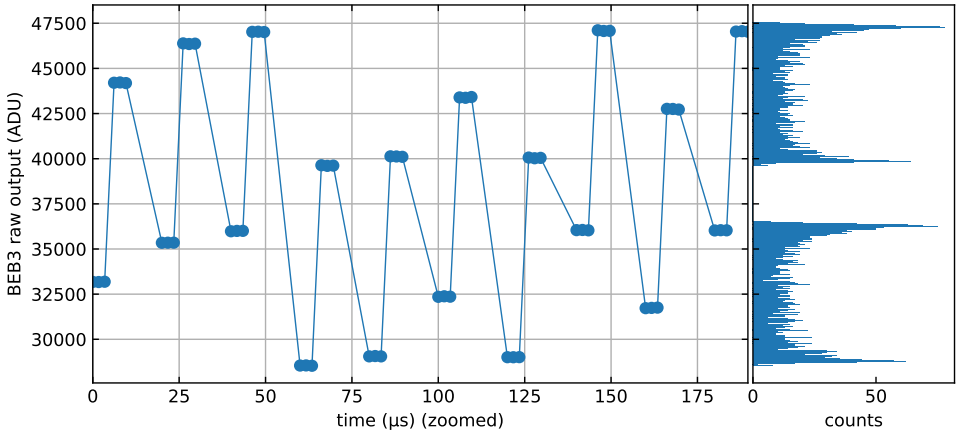

Figure 5.6: Raw data of the CROC v1 output (left) and the full distribution on a histogram (right) for an input square pulse signal of 5 mV amplitude and CROC operating in Transparent mode with Gain^{6bit}=5.

as reference noise the standard deviation of the calculated amplitude when sampling once per level, the noise will decrease as the inverse of the square root of the number of samples per level. However, in this particular test, the goal is a precise measurement of the mean value of the amplitude distribution to calculate the gain of CROC. The mean value of each measurement is converted into volts by multiplying with the calibration constant of BEB3. The amplitude spectral density of the raw data using FFT (bottom plots) shows a flat distribution. Note that the frequency used in the FFT is not the sampling frequency, because the single samples are not recorded periodically. However, each loop provides an amplitude measurement from a set of 6 samples, whose period is constant, and so this is the frequency used here.

The absolute gain of a single measurement is calculated as the ratio of the output amplitude divided by the input one. The calibration of the CROC absolute gain in transparent mode as a function of the Gain^{6bit} of the first amplifier is presented in Figure 5.8. This calibration was realized with channel 0 of the evaluated chip, but all channels had similar results. Recall that the gain of the first amplifier alone is expected to be half of the total absolute gain of CROC. However, since the factor 2 is also present in DSI mode, the calibration refers to the complete $2G$ gain in transparent mode. Signals with several input amplitudes were chosen for this test, with their low rail always at 0 V. Not all signals were tested for the same gain options due to too small amplitude to separate the rails or saturation of BEB3. Nevertheless, a wide range is covered from nearly the minimum value Gain^{6bit}=0 to the maximum one. Each measurement is repeated 3-4 times, which is not clearly visible because of overlapping points.

The maximum absolute gain of CROC for Gain^{6but}=63 is ∼350, about 40% higher with respect to the theoretical one from equation 5.2. A linear dependence on the Gain^{6bit} was expected, which is not the case. The source of these unexpected results is not clear, but it could be related to the flaw in the design of the first amplifier. A second degree polynomial fit is applied on all the measurements irrespectively of the input amplitude.

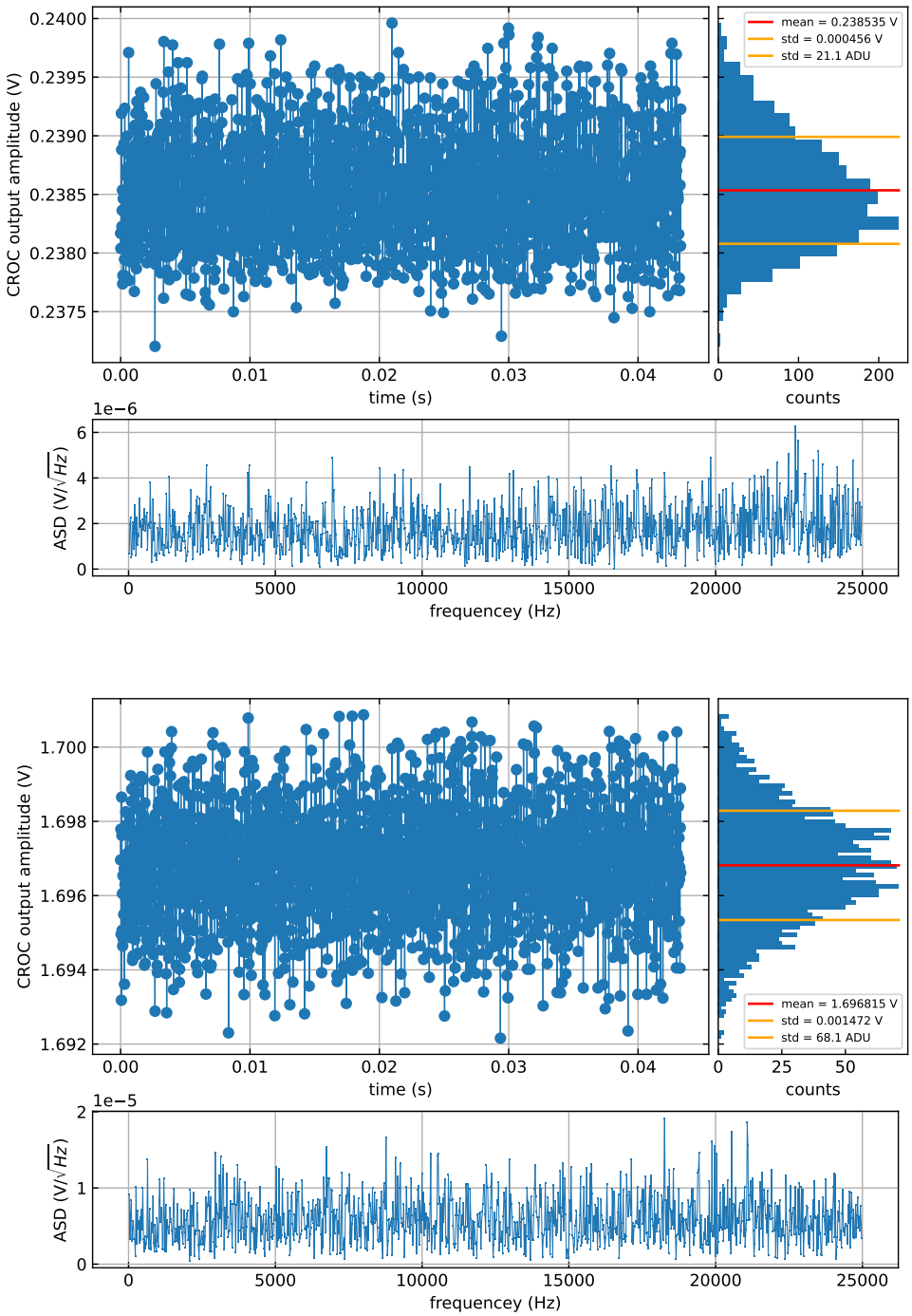

Figure 5.7: CROC v1 output amplitude (top left), its distribution (top right) with the mean and std values noted, and its amplitude spectral density (ASD) using FFT (bottom), for an input signal of 5 mV amplitude, operating in Transparent mode with Gain=5 (top triplet) and Gain=63 (bottom triplet).

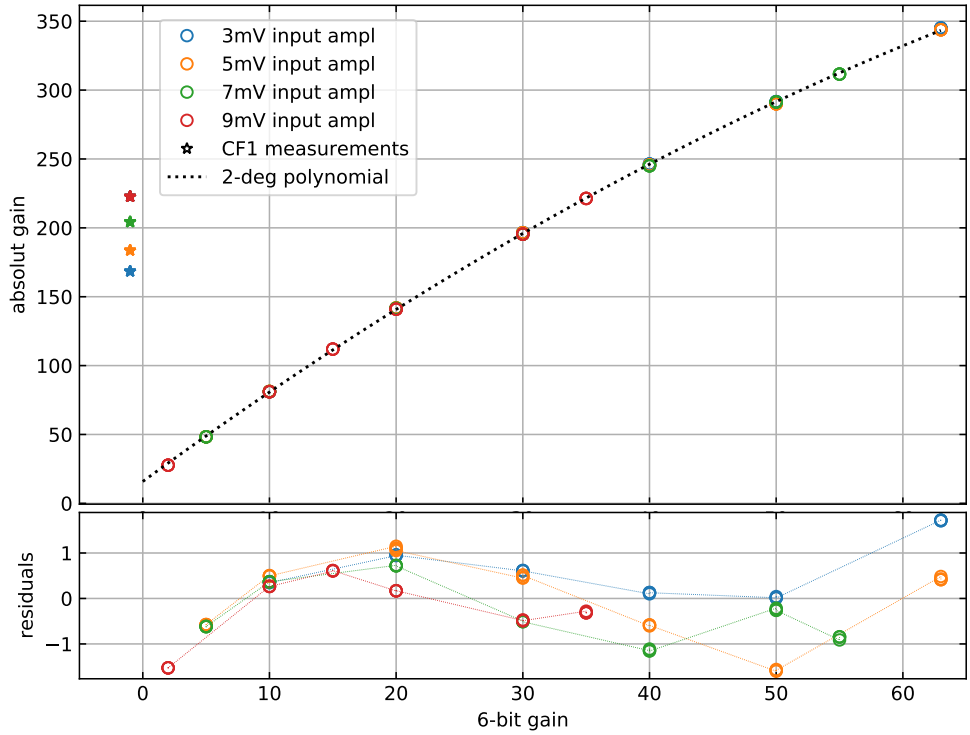

Figure 5.8: CROC gain calibration in transparent mode for various input amplitudes of channel 0. CF1 mode option is represented by $x = -1$. The black dotted line is a 2nd degree polynomial fit over all the measurements. On the bottom plot are presented the residuals of the points from the fit line.

The resulted $f(x) = -0.024x^2 + 6.731x + 15.852$ fit function, where x is the Gain^{6bit} parameter, is presented with the black dotted line in Figure 5.8. This fit function was chosen as an approximate model only to parameterize the measured data and is not predicted theoretically. Variations lower than 1% of the absolute gain of CROC are observed for the different input amplitudes for fixed values of the Gain^{6bit}. This is quite low to indicate any dependence of the absolute gain on the input amplitude and the testing can continue. It is important to note that the output noise of a measurement, like the ones shown in Figure 5.7, divided by the absolute gain, is lower than 1 ADU of BEB3, even multiplied by the square root of the number of samples per level. This shows that the input noise of BEB3 is eliminated and indicates that the noise of the input signal combined with the input noise of CROC will be of the order of 1 μV, which is in agreement with the specifications of the waveform generator for amplitudes of the order of 1 mV.

The star-points represent the CF1 option, using -1 for the x-coordinate to distinguish it from the Gain^{6bit}. The absolute gain of CROC in CF1 mode is completely off, higher than 100 with respect to the expected 1. Additionally, it presents a great dependence on the input amplitude. Because of the design mistake that led to the RA issue, the first amplifier gain in CF1 mode is in fact made with non-linear resistors (the transistors of the switches act as resistors), which explains the higher gain that is measured and the dependence on the input signal. As the CF1 gain is made with resistors, the RA still

does not affect the reference level, like in the Gain^{6bit} mode. A linear and an exponential fit are applied on the CF1 points, both with a coefficient of determination (R^2) greater than 99.6%. Again, these fit models are not predicted theoretically and their goal is to approximately parameterize the CF1 gain. The exponential fit is better by 0.1% and the extrapolated value for 0 V input amplitude is ∼145.9. The absolute gain of CROC in CF1 mode is stable for a specific input amplitude and could only be calibrated as a function of the input amplitude, which was not the goal of the design.

5.1.5 CROC v1 input noise measurement in Transparent mode

After calibrating the gain in transparent mode, the noise introduced by CROC can be quantified. In terms of hardware, the input of CROC is terminated to the ground with a 50 Ω resistor. The exact same sequencer can be used as for the gain calibration for consistency. As shown previously, the raw plot of such a measurement would be packets of 6 points at a non-fixed reference level after every Clamp/RA pulse, as it is shown in Figure 5.9 top. The exact same analysis as before would give processed results, which is not the intention of this study. In order to remove this defect, the mean value of every 6 samples per loop is calculated and subtracted from each one of them. The repositioning of all the raw samples around zero (see Figure 5.9 middle) results in a Gaussian-like distribution.

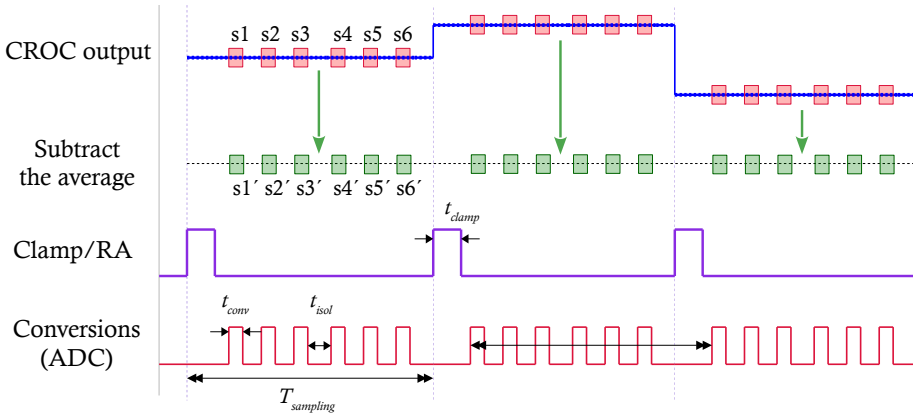

Figure 5.9: Timing diagram of CROC input noise measurement in Transparent mode.

The input noise is taken as the estimated sigma of the Gaussian fit on the distribution divided by the absolute gain of CROC. The gain calibration of Figure 5.8 is used for all 4 channels. The approximate value of 145.9 is used for the CF1 mode. The results are presented in Figure 5.10. The noise gets lower as the gain grows and becomes flat above an absolute gain of ∼150, which corresponds to Gain^{6bit} ≈20. The noise is very low, 3.0-3.5 μV, consistent for all channels. This value is about 1 e^- in charge units for the DAMIC-M CCDs. For the reference, the noise of a single-skip CCD image is usually of the order of a few e^-. With such a low noise, CROC is acceptable to provide the front-end amplification in a CCD setup. A relative test will be described later in section 5.4.

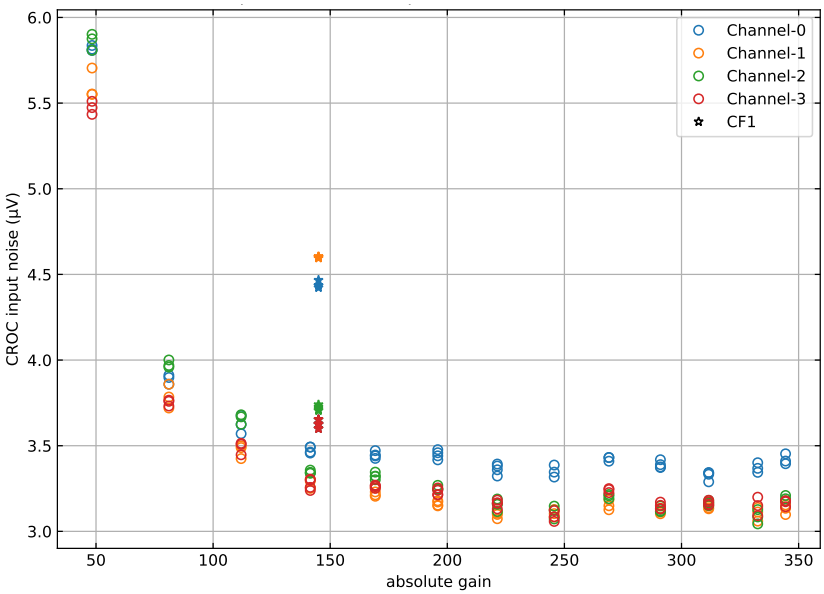

Figure 5.10: CROC input noise measurement in volt units as a function of the absolute gain of CROC in transparent mode for all channels. The Gain^{6bit} measurements are shown with open circles and an approximate calculation of CF1 option with star points.

5.1.6 CROC v1 *RC* time constant calibration in DSI mode

With the gain of the first amplifier calibrated, next follows the evaluation of CROC in DSI mode, starting with the calibration of the *RC* time constant as a function of the RC^{6bit}. In this mode, the total gain depends on 2 parameters, the Gain^{6bit} or CF1 and the RC^{6bit}. All triggering signals must be included in the sequencer. A timing diagram in Figure 5.11 describes the operation of CROC in DSI. The injected signal to CROC is again a square

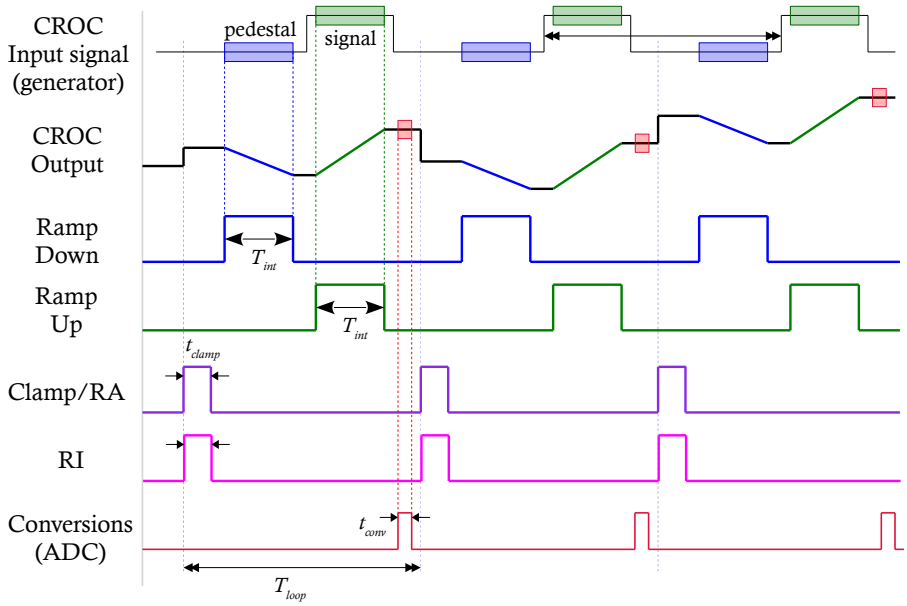

Figure 5.11: Timing diagram of CROC in DSI mode.

pulse with a fixed amplitude of 5 mV. Its width is adjusted based on the sequencing of the timing signals. The period of every loop is 15 μs. In the beginning of every loop there is a 2 μs long Clamp/RA pulse (purple signal in Figure 5.11). Although, the RA defect still causes some significant uncertainty on the pedestal level, this should not affect the measurement in DSI mode as it is subtracted from the signal level. Synchronous to the Clamp/RA, a RI pulse is sent (pink signal) as well. Then, follows the measurement of the input square pulse. The pedestal level is integrated with RD for a T_{int} = 1 μs window. None of the RD and RU are active for a short *isolation time* afterwards, in order to allow the input signal to change from low to high, equivalent to charge transfer under the sense node in a CCD. The signal level is also integrated in the opposite polarity of the pedestal with RU for the exact same duration, T_{int}. The slope of the CROC output during RU and RD depends on the RC time constant that is chosen. The resulting voltage level is equal to the amplified amplitude of the input square pulse, following equation 5.2, and it is sampled once at the end of the period. In terms of analysis, the DSI mode is much simpler than the Transparent. The data do not need any processing and they directly correspond to the measured amplitude. An example is shown in Figure 5.12, for a Gain^{6bit}=63 and RC^{6bit}=3. The raw data converted in voltage units are presented on the top left plot with their distribution on the top right one. The mean value corresponds to the amplified amplitude and the std to the error of the measurement. On the bottom, there is the amplitude spectral density of the raw data using FFT. A consistent shape is observed for every tested Gain^{6bit} and RC^{6bit} combination with an increase in the frequencies between 1 and 5 kHz and a spike at ∼20.3 kHz, for unspecified yet reasons.

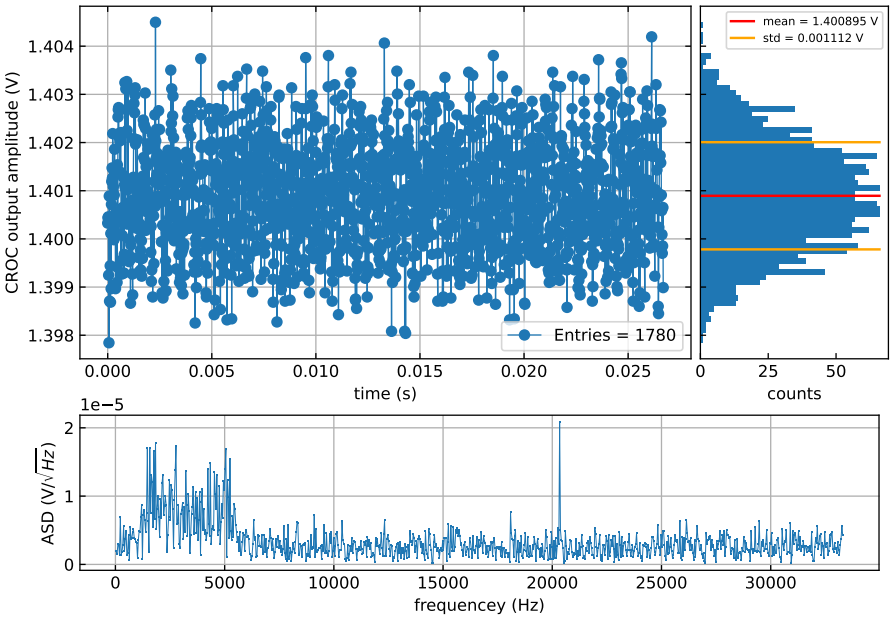

Figure 5.12: CROC output amplitude (top left), its distribution (top right) with the mean and std values noted, and its amplitude spectral density (ASD) using FFT (bottom), for an input signal of 5 mV amplitude and CROC operating in DSI mode with Gain^{6bit}=63 and RC^{6bit}=3.

The absolute gain of the set parameters is derived by the ratio of the measured amplitude over the input one. It is presented in Figure 5.13 left for several Gain^{6bit} and RC^{6bit} combinations. Since there are two parameters contributing to the absolute gain, the pure RC needs to be calibrated. Using the calibration of the first amplifier $2G$ in transparent mode, the RC time constant as a function of the RC^{6bit}, derived from the equation 5.2 solved for RC, is presented in Figure 5.13 right. Since the amplitude of the input signal is fixed, the CF1 option is also presented here for completeness.

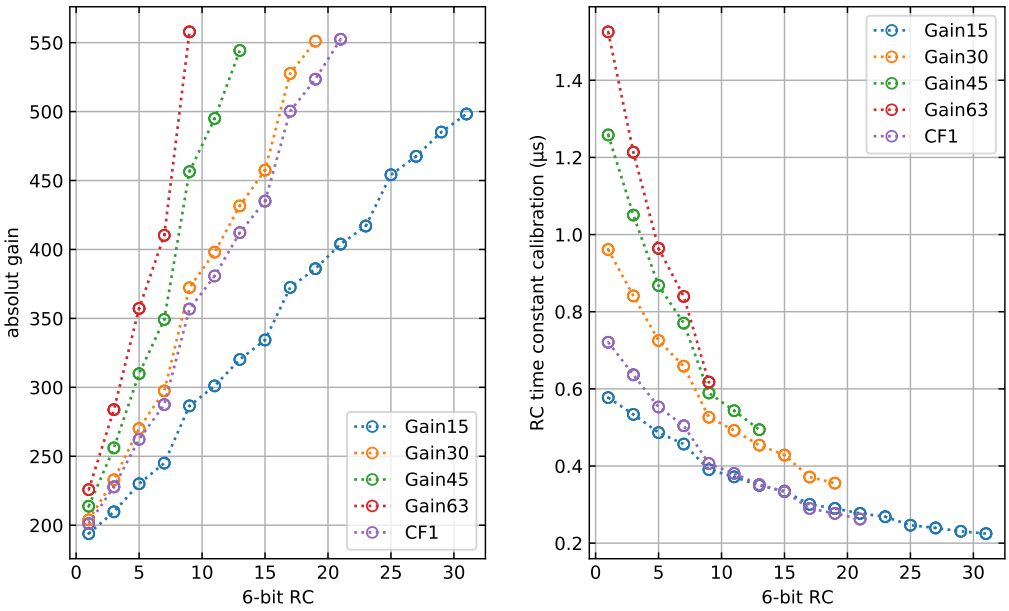

Figure 5.13: CROC absolute gain in DSI mode (left) and RC time constant calibration (right) as a function of the RC^{6bit} option for a square pulse input signal with fixed 5 mV amplitude.

The RC calibration shows a very strong dependence on the first amplifier Gain^{6bit}, varying by a factor 2 from Gain^{6bit}=15 to Gain^{6bit}=63. The CROC was tested in Transparent mode and Gain^{6bit} mode for different input amplitudes leading to consistent results, that do not show any input amplitude dependence. So, it seems to be the second stage of CROC in DSI mode that causes the non-linearity and depends on the input amplitude. In principle, the RC time constant could be calibrated as a function of the RC^{6bit}, the Gain^{6bit} and the input amplitude, for all the combinations of different sets of parameters, even though it is quite inconvenient. Additionally, the scale of the time constant calibration does not correspond to the theoretical values expected to be up to 50 μs. Due to this input amplitude dependence, the calibration of the RC will not continue and thus, the DSI mode will remain incomplete due to dysfunctionality issues.

CROC v1 characterization conclusion

The first version of CROC has been evaluated presenting several issues. Nevertheless, CROC v1 has a quite consistent response, even though there are undesired effects that

cannot be overlooked. The CF1 gain mode of the first amplifier and the absolute gain of CROC in DSI mode were not able to be calibrated properly, presenting a dependence on the input signal amplitude. The Transparent mode with the Gain^{6bit} option suffers from the defect of the Reset Amplifier timing signal, but can be treated in the data analysis. This preliminary study is sufficient and later the CROC will be evaluated as well by the new ADC boards in a complete DAMIC-M setup, with higher precision and faster sampling frequencies. In a next section, the work with this chip used in a CCD setup will be presented. We successfully managed amplifying the video signal and readout images with particle tracks.

5.2 CROC v2

A second version (v2) of CROC was designed in an attempt to fix the problems we observed in the first one. The chip was received and started being characterized in the fall of 2020. The two versions have identical physical layout, pin arrangement and operation principles. The same evaluation setup and LabView control software were used.

The first major difference that was noticed, was the much higher current consumption of the +12 V supply of BEB3 with a CROC v2. In order to make sure the source of this increment is the chip, the +5 V voltage supply was disconnected from the BEB3 and both the +3.3 V and +5 V were provided by an external power supply. The +5 V was still provided to the+ 2.5 V reference chip, with a negligible expected consumption, as was verified with CROC v1 as well. By doing so, the BEB3 consumption returned to the expected levels. The +3.3 V digital input had a low consumption of 8 mA. Indeed the consumption of the +5 V supply was above 200 mA and it was not stable in time. The CROC was not designed to have such a high power consumption. Therefore, we started questioning the robustness of the chip in long-time operation. We performed non-stop measurements for up to 30 min periods, while changing nothing at the setup, which led to the clear conclusion that the CROC v2 is unstable.

5.2.1 CROC v2 in Transparent mode

First, the chip was evaluated in transparent mode. A sequencer similar to the CROC v1 test was used, with a Clamp/RA pulse for 2 μs and 6 ADC samples in every period. The new version fixed the problem of the moving reference level after every RA pulse that was observed in CROC v1. Furthermore, the CF1 mode was fixed as well with an absolute gain of the first amplifier of ∼1.7, while 1.0 is theoretically expected. In Figure 5.14, the raw output of CROC v2 is presented for Gain^{6bit}=4 and an input amplitude of 5 mV. Compared to the plot of Figure 5.6, where the span of the pedestal and signal levels of CROC v1 is a few thousand ADUs, for v2 it is only 50-60 ADU. A Gaussian fit is applied on the two levels, on the right plot. Nevertheless, in the analysis the pedestal is

still subtracted from the signal level in every period. The amplitude of the data of Figure 5.14 is presented in Figure 5.15. The std of the amplitude distribution in ADU is even lower than the one of the raw plot, which means that the Clamp/RA still introduces some uncertainty, yet it is much less than CROC v1. Recall that for G=5, the amplitude std of CROC v1 was measured ∼20 ADU, not very different from the one in CROC v2 with Gain^{6bit}=4.

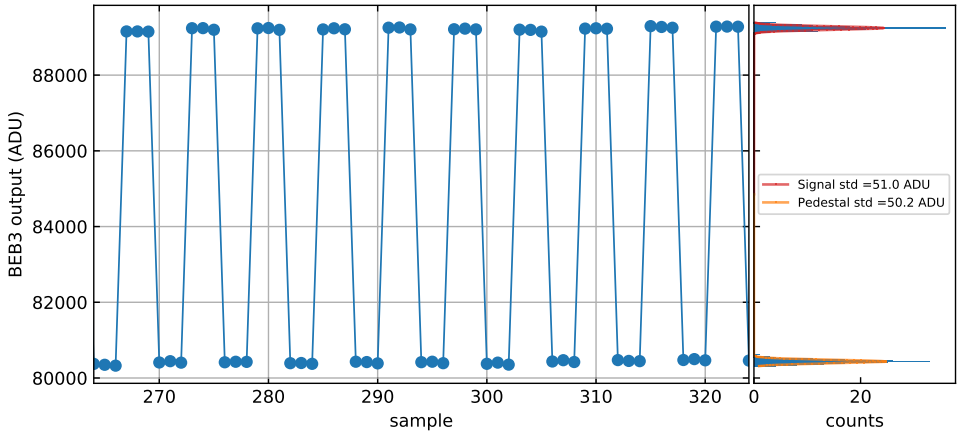

Figure 5.14: Raw data of the CROC v2 output (left) and the full distribution on a histogram with Gaussian fit curves (right) for an input signal of 5 mV amplitude and CROC operating in Transparent mode with Gain^{6bit}=4.

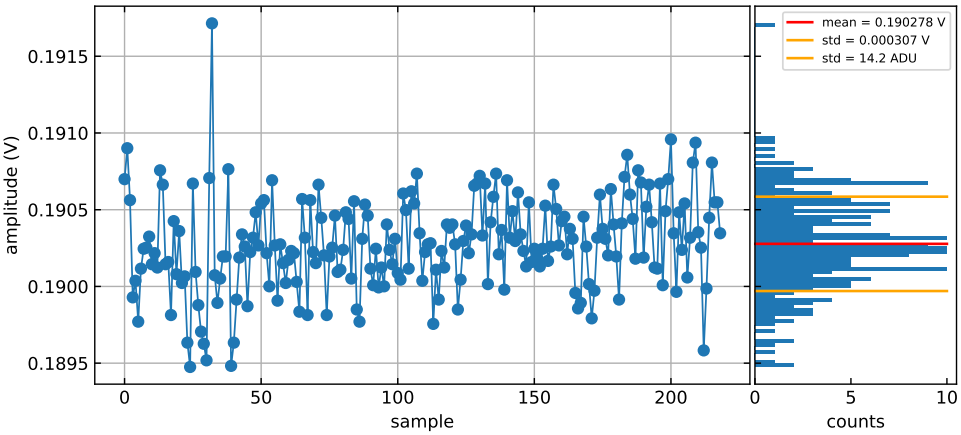

Figure 5.15: CROC v2 output amplitude (left) and its distribution (right) with the mean and std values noted for an input signal of 5 mV amplitude, operating in Transparent mode with Gain^{6bit}=4.

Inconsistencies in time were observed with CROC v2. The amplification of the chip seemed to change after a few minutes of operation. So, a long non-stop data-taking was performed the same way as the previous measurement was described. The results are presented in Figure 5.16. On top, there are the pedestal (blue) and signal (orange) levels versus time, where it is clear that they shift. If the levels were going to stabilize at some point and their difference was stable, this behaviour of the chip may be handled. However, in the middle plot, the amplitude does not have a stable value, and after ∼15 min it becomes completely unstable quite abruptly. The std of the pedestal and signal levels are

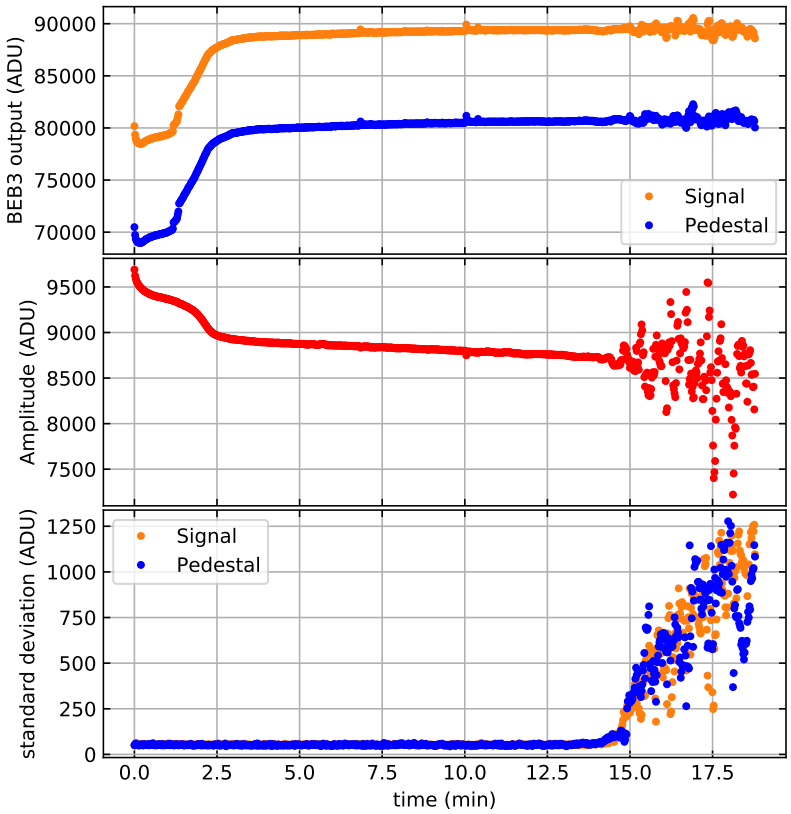

Figure 5.16: CROC v2 long-time data-taking operating in Transparent mode with Gain^{6bit}=4 with an input signal of 5 mV amplitude. The raw pedestal and signal levels (top), the amplitude (middle) and the std of the pedestal and signal measurements (bottom).

also presented on the bottom plot, and they make clear that the raw data lose their good shape. Several datasets were recorded like this one and the same response was observed in all of them, with slightly different duration after which the chip becomes unstable. In all attempts, the data-taking starts immediately after powering up the chip. The same instability after time is observed even when there is no input signal and the input of the CROC is terminated. In conclusion, the CROC v2 is not robust in transparent mode and after some time it stops operating normally. It cannot be calibrated since the gain changes in time and so, it cannot be used in this mode. A probable instability of the common mode voltage of the second amplifier was perceived later from the design that could explain the high power consumption. The high consumption can indicate that some internal component of the CROC v2 becomes hot during operation, until too hot and the chip ceases working.

5.2.2 CROC v2 in DSI mode

To verify if the CROC v2 still has some potential, it was evaluated in DSI mode. This time a slightly more complicated sequencer than for CROC v1 was used in order to extract as much information as possible. The timing diagram of Figure 5.17 shows in detail the

whole sequence. There are in total 3 samples per period, one right after the Clamp/RA and RI pulses and before the RD to measure the pedestal, one after the RD and a final one after the RU. In addition, a square pulse is injected into the CROC every other period. By doing so, one can measure the amplitude of the input signal and integrate the pedestal twice with reverse polarities and, theoretically, result in a 0 V measurement. The Gain^{6bit} and RC^{6bit} are both chosen at 4 and the integration time is 1 μs. This kind of testing was recorded for several minutes without changing anything in the configuration during this period. The results are presented in Figure 5.18.

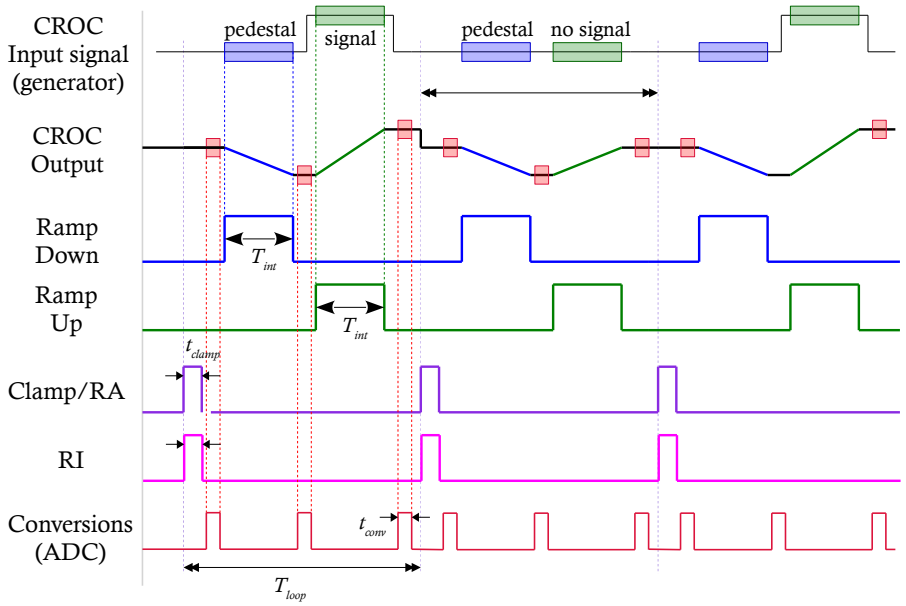

Figure 5.17: Timing diagram of CROC v2 testing in DSI mode

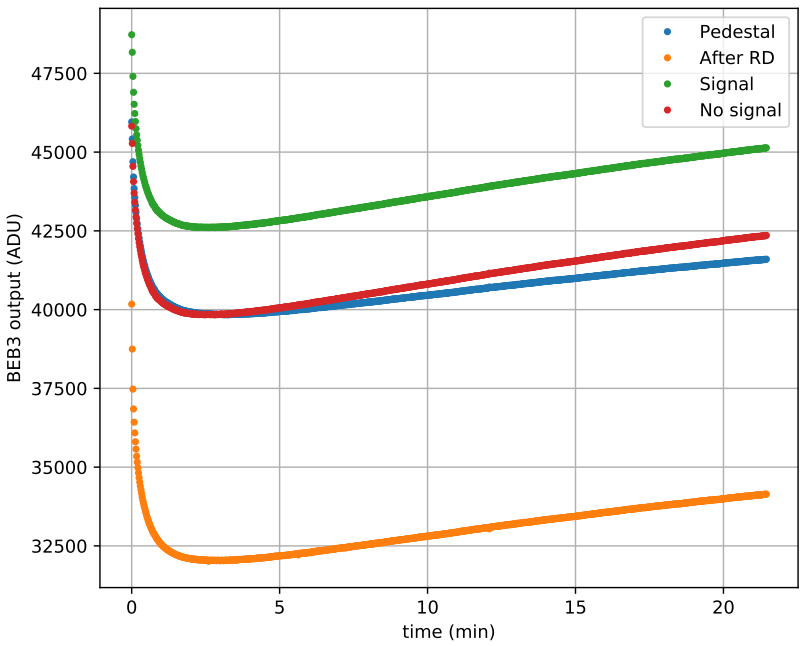

Figure 5.18: CROC v2 testing in DSI mode for a long-time period for Gain^{6bit}=4, RC^{6bit}=4 and an integration time of 1 μs with an input signal of 5 mV amplitude.

First of all, it is clear that there is a very significant drift of all measurements with time, which does not seem to stop even after 20 min of operation. The data-taking starts again right after the power up of CROC. The pedestal (blue points) is not stable and probably after a longer time it would cause saturation to the ADC. If the instability of the pedestal was the only issue, it could probably be handled, since what is measured is the difference of the signal level from the pedestal. As expected based on the pedestal shape, the measurements after RD (orange points) and RU (green points - "Signal") also follow the same curvature. Most importantly, however, the no-signal level also behaves similarly to the others. Since the duration of both RD and RU is the same, it should result to a 0 V measurement.

There is a short period at the beginning, where the pedestal is higher than the no-signal, yet in time this changes. This could probably be explained by some strange asymmetry of the two inputs of the second amplifier and their gain is not the same. Moreover, this asymmetry should be time dependent. This means that the gain of the CROC v2 in DSI mode changes significantly in time, and thus cannot be calibrated.

CROC v2 characterization conclusion

In conclusion, the attempt of CROC v2 to fix the issues observed in v1, such as the introduced uncertainty after every RA or the high CF1 mode gain depending also on the input amplitude, was indeed an improvement, although new major issues appeared. Much time and effort were invested in trying to understand the source of the malfunctioning and hopefully fixing these problems with no success. The high power consumption and the unstable response in time that consistently lead to dysfunctionality (at least in transparent mode), render the CROC v2 a problematic chip unable to be used in any future system.

5.3 DCA: Differential CCD Amplifier

A third version of a front-end chip was developed, this time a much simpler one. The *Differential CCD Amplifier (DCA)* is a 4-channel single-ended input to differential output ASIC with a 2-bit gain option. A block diagram of the DCA is presented in Figure 5.19. The chip requires a single +5 V power supply and a +2.5 V reference (V_{ref}) voltages. No digital voltage is necessary like in CROC, since DCA requires no programming. The 2-bit gain is chosen for all channels by 2 digital inputs that control switches with 5 V as logic high. The input signal first passes from a non-inverting amplifier with capacitor feedback and then is split to produce the differential output. There are 2 LVDS signals, Clamp and Reset Amplifier, that can short the input to the V_{ref} and restore the DC of the first amplifier output respectively. The maximum absolute gain of the chip is expected to be equal to ∼170 from simulations at room temperature.

The DCA is soldered on a board with no other components than resistors and capaci-

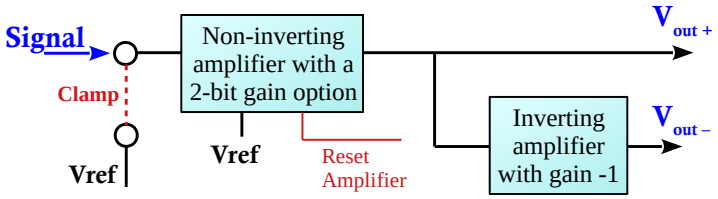

Figure 5.19: Block diagram of the DCA for a single channel.

tors. In addition, the board offers the ability to "program" the 2-bit gain with bias signals or set it manually with jumpers that short the input to a 5 V bias voltage. The DCA is evaluated in a similar setup as for the CROC, with a BEB3 ADC board and an identical transparent mode sequencer with a Clamp/RA pulse in the beginning of every period and 3 samples per level of an input square signal. A representative plot of the amplitude distribution for a square pulse input signal with ∼0.5 mV amplitude and Gain<0,1>=00 is shown in Figure 5.20. A peak at ∼26.8 kHz and two more ∼14-15 kHz are consistently presented as well as an increased amplitude in a band of frequencies between 32.5 kHz and 34 kHz, but their origin is not yet specified. Despite that, no strong unexpected effects are observed.

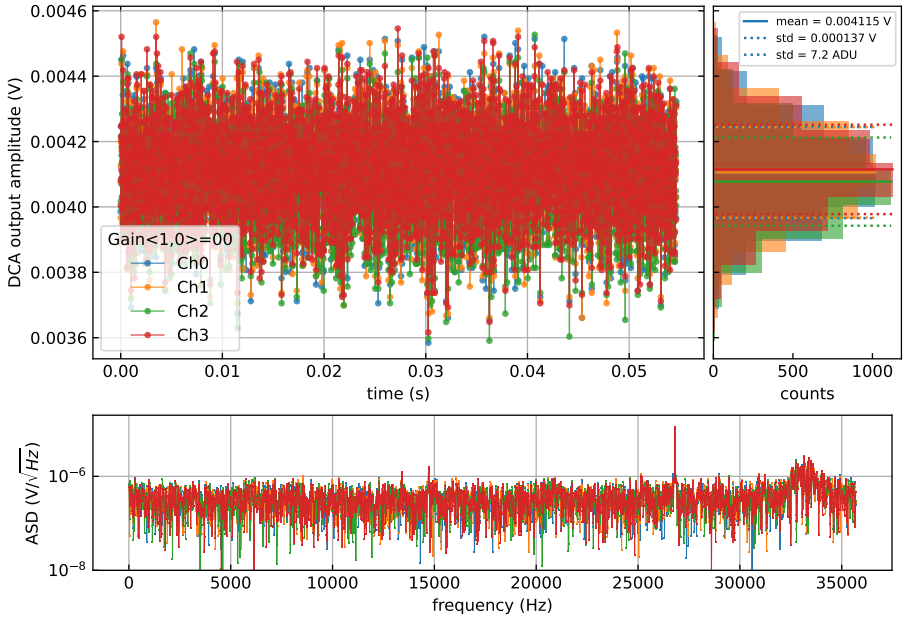

Figure 5.20: Raw amplitude measurements of all 4 channels of the DCA (top left) and their distribution with the mean and the standard deviation values noted (top right), and the amplitude spectral density using FFT (bottom) for an input signal of ∼0.5 mV amplitude and Gain<0,1>=00.

The calibration of the 2-bit gain (Gain< $bit1 - bit2$ >) of all 4 channels, with a varying input amplitude in a quite extended range, is presented in Figure 5.21. All channels have similar results with a maximum absolute gain at Gain<0,1>=11 around 150, about 12% lower than expected. The far-right measurement of the bottom plot for Gain<0,1>=11 indicates saturation of the ADC of BEB3. An input amplitude dependence is observed on the

left side of the input amplitude for the two lowest gain options, ∼30% for Gain<0,1>=00, and on the right side for the two highest ones, up to ∼10% for Gain<0,1>=11. For the right side non-linearity is seen in simulations when the chip operates at room temperature, but disappears at 100 K. The left side non-linearity is not clear and is not seen in the simulations, and from the distribution of the several recordings for each amplitude, the source could potentially be non-linear response or/and noise from the signal generator or the attenuator devices that are used for the evaluation.

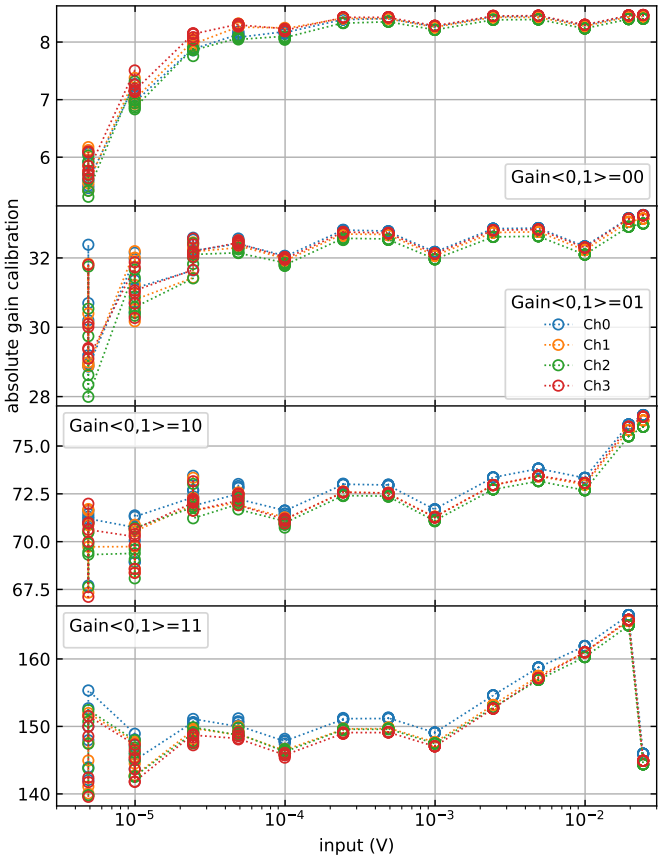

Figure 5.21: DCA gain calibration of all 4 channels versus the amplitude of the square pulse input signal.

The input noise of the DCA is also measured. The inputs of the chip are terminated to the ground and thousands of data are recorded. The input noise of each channel and each gain option is estimated as the standard deviation of the distribution divided by the average of the absolute gain. The results are presented in Figure 5.22. The input noise goes below 6 μV for the highest gain, which is an acceptable value to allow the chip to operate with a CCD. This noise is higher than CROC v1 almost by a factor of 2, and corresponds to about 2 e^- in charge units for DAMIC CCDs. Recall that the noise of a single skip CCD image is measured equal to a few e^- with other acquisition systems.

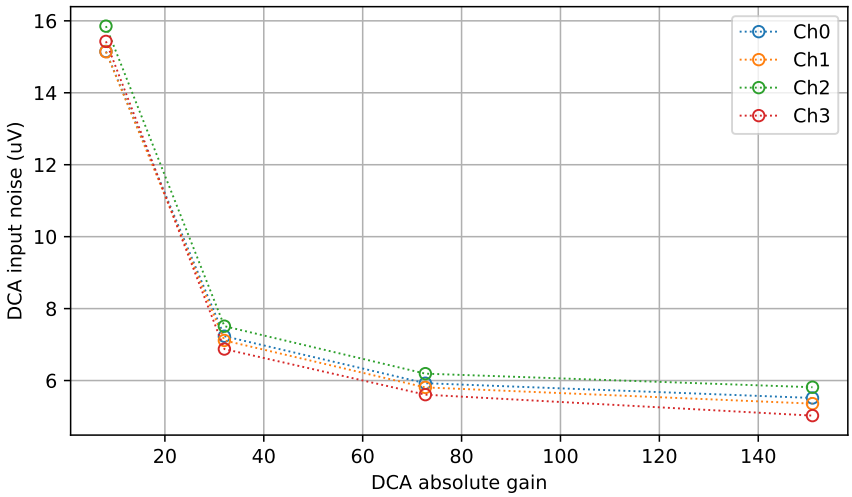

Figure 5.22: DCA input noise as a function of the absolute gain for all 4 channel.

DCA characterization conclusion

The DCA chip was evaluated at room temperature without presenting any major defects. The amplification it can offer is high enough and similar to prior front-end electronics that have been used, such as the second stage board described in Chapter 3. The measured input noise is low, $\sim 6\,\mu$V, and is considered acceptable for further testing and integration in an acquisition system. As described in the previous chapter, the DCA was used in a purely DAMIC-M preliminary acquisition system to control a skipper CCD and successfully managed to record images with visible tracks.

5.4 CCD testing with Leach and CROC v1

After the unsuccessful attempt of CROC v2 to produce an improved and reliable front-end chip, and before the production of DCA, we turned to CROC v1 to test it with a skipper CCD, in spring 2021. The v1 may have presented some issues, but is robust in Transparent mode with the 6-bit gain option. The uncertainty due to RA is undesired, yet can be treated in the data analysis. A new CROC "cold" board was designed for operation at the same low temperature as the CCD with a v1 chip soldered on it. The CROC is to replace the front-end second stage board (see Chapter 3) in a CCD setup operated by the Leach system.

Several modifications in hardware, firmware and software were necessary for this updated system. A brief schematic with all the major components is shown in Figure 5.23. The clocks and biases for the CCD are provided by the Leach. The second stage board must remain in the setup for clock shaping and bias filtering. The programming and triggering signals of CROC are provided by the Altera Cyclone III through the BEB3 board. An output signal from the Leach, synchronous to the RG pulse, which is sent to the CCD at every skip, is used to trigger the Clamp/RA pulse for CROC. The video signal after passing from CROC is delivered to the video board of the Leach, which is now configured

for differential input. Recall from Chapter 3 that the Leach video board can receive single-ended or differential signals, but the ADC of the board is single-ended input. The CROC is used in Transparent mode with Gain^{6bit}=20. This corresponds to an absolute gain of ∼141, of the same order of the ∼120 that the previous setup with the second stage board provides. Even though we managed to cool the CCD at 160 K, about 20 K higher than the usual and proper temperature, the temperature of the CROC did not fall below ∼5 °C. This could probably be an issue of bad thermal contact delivering the cold or, less likely, high heat emission from the chip during operation that did not allow the temperature to go lower.

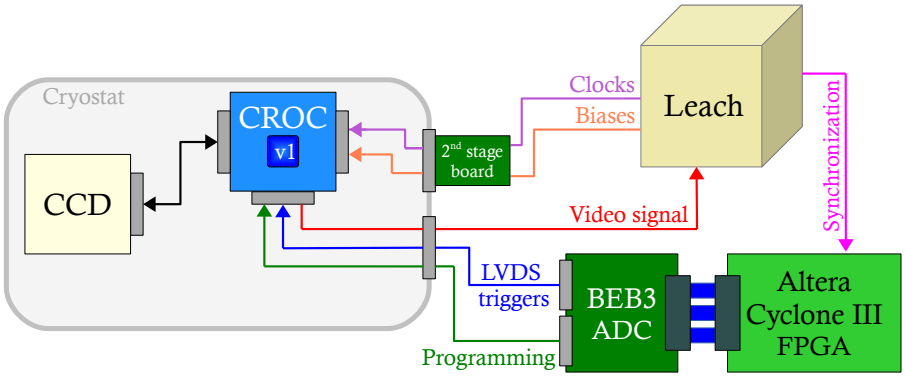

Figure 5.23: Schematic of the CCD setup controlled by the Leach system and the CROC v1 for the front-end amplification.

As an alternative, it was proposed to use a Raspberry Pi for the programming of the CROC, an application that has been verified, and send the Leach synchronization signal, converted into LVDS, directly as the Clamp/RA pulse. This concept was not tested and is only mentioned here for possible future use.

The video board has a test point for each of the 2 channels, after converting the input signal (or the CROC output) from differential to single ended before sending it to the ADC. A screenshot from an oscilloscope probing the test points during CCD operation is shown in Figure 5.24. The yellow and green signals are the two channels of the video board of two different amplifiers of the CCD. The purple one is a Cyclone III board output signal synchronous to the Clamp/RA only for visualization. The dent on the video signal at the same time as the Clamp/RA is the effect of the RG on the CCD output. The spike in the middle of each period is the effect of the SW. Additionally, the distorted pedestal is due to the RA defect. Even though the CROC operates in Transparent mode, the Leach video board performs the measurement as a DSI, integrating the video signal before and after the SW signal for 10 μs. This means the raw data correspond to the pure amplitude, like in the case of CROC in DSI mode, and they need no pre-processing.

This has been the first test I have performed with a CCD, which gave me the chance to understand deeper the image analysis and see in detail the effects that occur. There has already been an existing data-analysis software, but I decided to go for a personal attempt

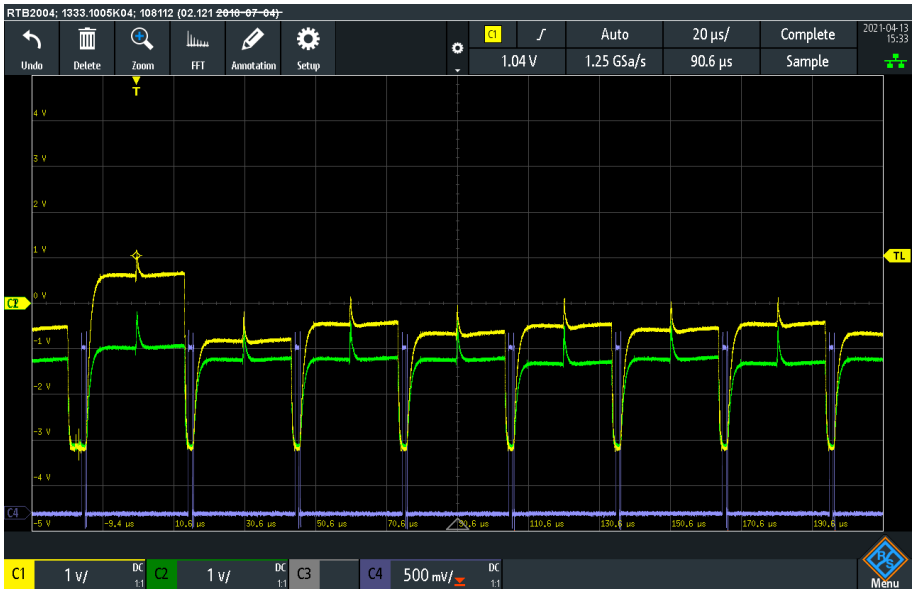

Figure 5.24: Oscilloscope screenshot of the two Leach video board channels and a synchronous signal of the Clamp/RA pulse. Several periods (skips per pixel) are shown here.

to acquire the experience of the image processing. After all, this test took place to evaluate the integration of CROC in the system and measure the electronic noise. Finding clusters and identifying them as specific particles were not the goal of this particular study.

The produced files carry the information of all the parameters used for the CCD operation, such as clock rail values and sequencing details, and the raw data in the correct order as they were recorded. An image can be displayed as a 2-d histogram with the x and y axes representing the coordinates of the pixel and the value of each pixel is the ADC measurement. The image can be visualized as a heat-map where the pixel values are represented on a color scale. The scaling of the color is not trivial, as the interesting pixels are not the ones that belong to some particle track cluster, but the ones with "no-charge" which define the noise. Finding all the clusters and a sensitive threshold to define the borders of the clusters is useful but not necessary here.

A single-skip image needs no particular processing for the visualization, but for an NDCM>1 an averaging can be applied to flatten the noise. Nevertheless, N single-skip images can be extracted from an N-skip image. Figure 5.25 shows an image with NDCM=10, averaged between skips 4 to 10 on top, and the skip #10 image on the bottom for comparison. First of all, with the CROC integrated in the acquisition system, we have successfully managed to acquire images and see particle tracks. This image was taken with a 6k $\times$ 1.1k DAMIC skipper CCD. Smaller frames of 100 $\times$ 1k pixels are recorded, to have files not too heavy for the analysis and to save time during readout. The output values are measured in ADU of the video board of the Leach. The color-scale represents the Leach video board output in ADU. Note that the higher the charge in a pixel, the lower the value of the ADC, with a minimum pixel value of around 20000 ADU.

The pixel values of the averaged image are then inserted in a histogram, see Figure

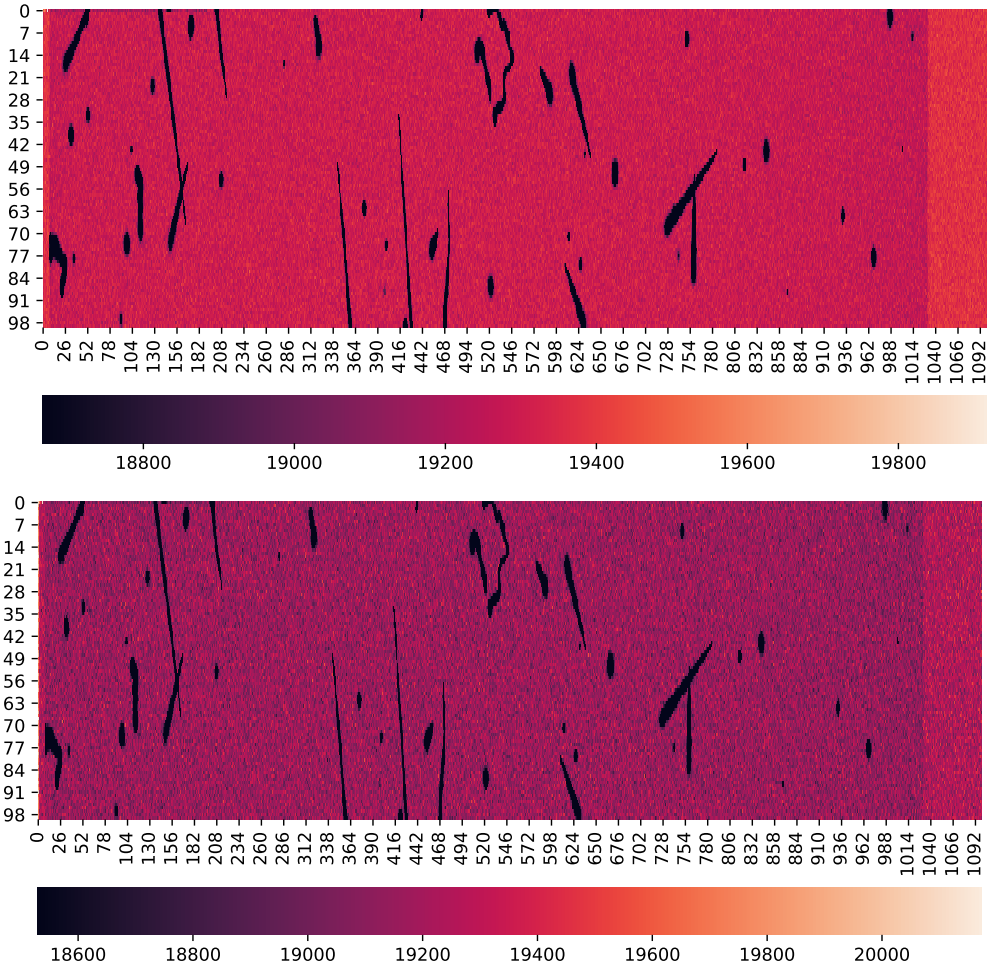

Figure 5.25: CCD image using the CROC v1. An averaged image between skips #4-#10 (top) and (single skip) skip #10 image (bottom). The color-scale represents the Leach video board output in ADU.

5.26, which reveals a major peak that corresponds to the "no-charge" pixels or only dark current, with a mean value of ∼19300 ADU. The distribution of these pixels is Gaussian-like, though as charge can be generated by other sources, the peak is Gaussian mainly on the low-charge side (on the right side of the mean value). So, the Gaussian fit is applied in an asymmetric region around the mean value, as in Figure 5.26. The sigma of this fit represents the noise of the image and subsequently of the CCD operated with the particular acquisition system. For a high enough NDCM and with a low-noise system, the single-electron peaks should be revealed in the histogram of the average image, as is shown in Figure 3.11. This is not the case due to probably high electronic noise.

Despite all the effort and adjustments, this system has achieved a noise of $\sim 10\, e^-$ for a single-skip image, which is 1.5-2 times higher than the prior setup. The dark current is expected to be higher with respect to the compared data due to the temperature difference, but not enough to explain the noise we measure. The second stage board, described in Chapter 3, has been operated for a long time and was optimized with the CCD and the Leach, while the CROC cold board used here is only the first version. A possible reason for

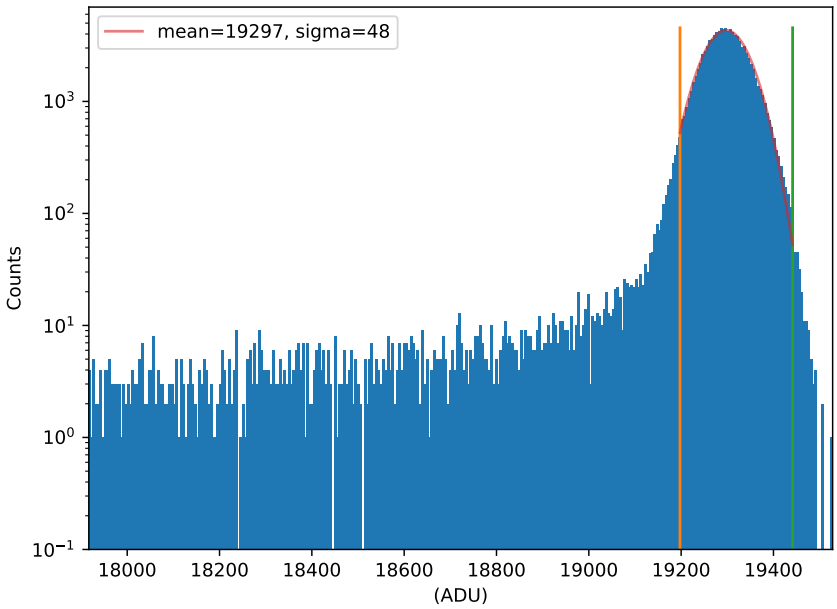

Figure 5.26: Histogram of the pixel distribution of the averaged image of Figure 5.25, zoomed close to the "no-charge" peak.

the higher noise may be the fact that the video signal of the CCD is split before the CROC and is delivered to the second stage board as well. This way, one can bypass the CROC and use the second stage board for the amplification and practically operate the whole system as originally. The very small video signal may pick up noise from this extension that can act as an antenna. So, it could be the CROC board that causes a higher noise and not the chip itself.

Overall, the CROC has given promising results. It is decided by the collaboration that CROC v1 will not be used in the final experiment, so a too detailed evaluation in a CCD setup will probably not offer much more useful information. A similar board with the DCA chip was developed and integrated successfully to a CCD setup. The next steps will be to optimize the front-end chip for the CCD video signal and the rest of the acquisition system to provide a comparable noise, or better, with respect to the previous electronics.

Chapter 6

Analog-to-Digital Converter

The final stage in a CCD acquisition system is converting the analog signal to the digital domain. The information is stored in the memory of the controlling PC which can be processed off-line. I will not dive deep in the functionality of an ADC, although I am going to introduce its top level operating principle.

There has been 3 proposed candidates for DAMIC-M:

- AD4020, 20-bit, 1.8 MS/s[1], 10 V_{pp} input range
- MAX11905, 20-bit, 1.6 MS/s, 6 V_{pp} input range
- LTC2387-18, 18-bit, 15 MS/s, 8.192 V_{pp} input range

A prototype board with the LTC2387-18 chip was developed by the Paris group called *Rapide 4ADC board*, but the Zurich group took over the development and evaluation of all the different ADC options. One of my first objectives was to characterize the Rapide board. In this chapter, I will present the progress towards this study and I will mention the final results from all ADC boards and their comparison that lead to the final choice.

6.1 AD5791 Digital-to-Analog Converter characterization

At the beginning of my thesis, I was not very familiar with the analog-to-digital or digital-to-analog converters. My very first project was the evaluation of a 20-bit AD5791 Digital-to-Analog Converter (DAC). Opposite of the ADC, the DAC receives an input code within a specific range and outputs a voltage. The number of input codes of a DAC is 2^N, where N is the number of bits. The range of the input code is by convention either from 0 to $(2^N - 1)$ or from $-(2^N/2)$ to $(2^N/2 - 1)$. This high-precision DAC was meant to be used for the characterization of the new ADC boards for DAMIC-M, specifically for the prototype Rapide board. The LTC2387-18 ADC has an theoretical ADU equal to 31.25 μV. The output resolution of a DAC in volt units must exceed the resolution of the ADC in order to provide a proper input for its characterization. The theoretical smallest step of a DAC output in volt units is called Least Significant Bit (LSB) and depends on the low and high

[1] S/s = samples per second readout speed

voltages references. These references correspond to the minimum and maximum output voltage of the DAC respectively and can also be referred as negative (V_{refN}) and positive (V_{refP}), not necessarily referring to the polarities of the voltages, as for example both can be positive. The LSB is theoretically calculated by the relation:

$$LSB_{theor} = \frac{V_{refP} - V_{refN}}{2^N} \tag{6.1}$$

The $V_{refP/N}$ must be stable at a level that exceeds the resolution of the DAC. A DAC chip also requires power supply and programming.

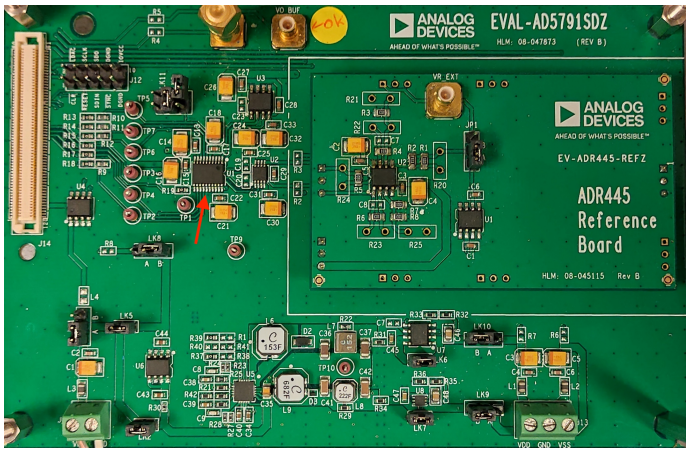

Figure 6.1: Photo of the EVAL-AD5791 board using the ADR445 daughter board. The red arrow points to the DAC chip.

The AD5791 DAC is operated on a commercial evaluation board EVAL-AD5791 (see Figure 6.1). The board can be powered externally with a single +3.3 V. Low-dropout regulators (LDOs) produce the rest of the necessary voltages for the elements on the board. Alternatively, it can be supplied externally with ±15 V, bypassing the LDOs. A daughter board plugged on the EVAL is producing the reference voltages from an ADR445 ultra-low noise voltage reference LDO. The ADR445 has an output of +5 V which is split and amplified to provide low noise ±10 V voltages for the DAC. With a 20 V output range and 20 bits resolution, the expected LSB will be equal to theoretical value of the Least Significant Bit (LSB) is $LSB_{theor} = 20\,\text{V}/2^{20} = 19.073486\,\mu\text{V}$. This is the default configuration of the EVAL board, but other reference values can be used as well. The single-ended output of the DAC can be reached directly or after passing from an output buffer, which gives the ability to output current. The DAC is compatible with a standard SPI. The chip can be controlled with a System Demonstration Platform (SDP) controller board with an application for a Windows operating system provided by the vendor. There is also an easily accessible set of pins to provide the SPI signals.

The DAC was characterized in the default configuration of EVAL-AD5791 proposed by its datasheet, with a single +3.3 V power supply, using an SDP-B controller board and the Windows application. The output is read by a high resolution Keysight 34470A

digital multimeter. The DAC is programmed to output voltage levels for a given input range from -2 V to +6 V with a fixed step and a delay between steps long enough so that the multimeter can record several measurements of the same level. Each level is averaged and the DAC output is presented on the top plot of Figure 6.2 as a function of the DAC input code (about 100 points).

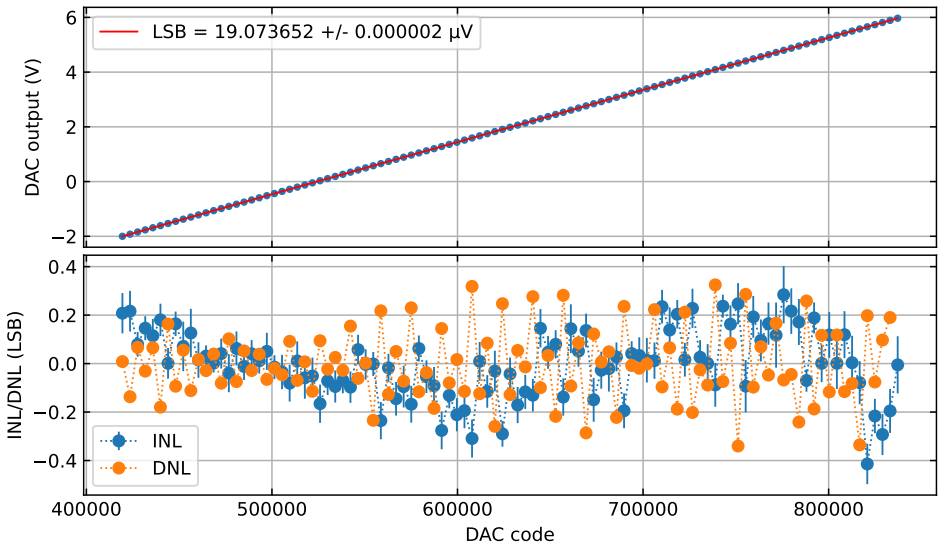

Figure 6.2: DAC output vs input code (top) and the INL/DNL (bottom).

A linear fit is applied where the slope of the curve is the LSB in volts. The experimental value of the LSB is measured:

$$LSB_{meas} = 19.073652 \pm 0.000002\,\mu V$$

The error of this value is derived from the linear fit. The experimental LSB is precisely measured and is in agreement with the expected value, as they differ at the 4th decimal digit, which may come from the inaccurate convention that the output range of DAC is exactly 20 V. The references to the DAC are indeed low noise, but they may be slightly off the theoretical values and for a 20-bit resolution it can result to a small deviation of the LSB. Just for the information, with a small hardware modification, the +5 V of ADR445 was used directly for the DAC high reference, while the low one was shorted to the ground (0 V). This has successfully worked with an LSB of ∼4.77 μV. In both cases, the output resolution of the DAC is better than the LTC2387-18 ADC.

The bottom plot of Figure 6.2 shows the Integral Non-Linearity (INL), calculated as the residuals of the points from the fit line, and the Differential Non-Linearity (DNL), calculated as the deviation of the measured step from the defined one for the scan, expressed in DAC code units, or LSB:

$$DNL_i = \frac{V_{i+1}^{out} - V_i^{out}}{LSB_{meas}} - step \tag{6.2}$$

Based on the datasheet of the DAC, both are in agreement with the expected values, below 0.5 LSB and their mean values are very close to 0. This means that there are no codes missing and the DAC outputs all the voltages it is supposed to accurately. The fit also finds correctly the $\sim\pm10$ V reference levels, even though a smaller output range is used here. Finally, the DAC has been tested for its robustness and output stability in time, with the programmed value fully restricted within 1 LSB range for the few-minute duration of the recording.

EVAL board control with Arduino

The control application of the DAC provided by the vendor is indeed easy to use, but there is no access to its source code and thus there is no way to achieve synchronization with another device. Moreover, most of our PCs operate with Linux systems, while the app is exclusively for Windows. In order to solve this issue, I developed a new way to control the DAC. It may be trivial as an application, or even a simple one for me at the end of my thesis, but it required much effort great to understand how to program an integrated chip through SPI.

An FPGA is a powerful tool, yet quite complicated. So, I turned to a much simpler and user friendly piece of hardware, the Arduino. I successfully developed a piece of software[2] for an Arduino Mega written in C++ to control the DAC. The code is flexible and allows for the programming of the DAC and all the functionalities offered by the Windows application. Most of the user interface that was developed for DAMIC-M is in Python, and so, I have developed a code that allows calling the Arduino function the control of the DAC through Python. As a future idea, a similar code could be developed for a Raspberry Pi as well to directly control the evaluation board with its GPIO pins. However, this project was not realized since the Arduino is simpler, cheaper and sufficient.

In the end, this project managed to replace a powerful and more expensive piece of hardware with something easier to use and more flexible in terms of programming, especially for future users that may not have prior experience. Most importantly, it introduced the ability and opened the way of using such tools for testing purposes in our setups. It actually found good use later (chronologically) as an easy solution for the control of the test sequencer board (see Chapter 4).

6.2 Rapide 4-ADC prototype board

A prototype board with the LTC2387-18 ADC was developed and evaluated by the Paris group, to measure its input noise and characterize its overall response. The so called *Rapide* board has 4 identical channels, as many as the CROC outputs, with an input range of ±4.096 V, 0-4.096 V for each differential input. The output range of the ADC is

[2]The Arduino code for the EVAL-AD5791 control can be reached here.

from $(-2^{18}/2)$ to $(+2^{18}/2-1)$ in ADU.

A schematic of the evaluation setup with a photo of the ADC board is shown in Figure 6.3. An Altera Cyclone III FPGA board is used for the control of the board with a user interface developed in LabView. Due to FPGA speed limitations, a maximum sampling frequency of 9.091 MHz is achieved instead of the 15 MHz that the ADC can reach. There is a single 50-pin Dsub connector on the board through which the inputs of the ADC channels are reached. For the evaluation, the 20-bit DAC board was used for DC and a function generator for AC input. An LMH730154 board converts the single-ended output of both the DAC and the function generator to differential, using an LMP8350 ultra-low distortion fully differential precision ADC driver. Unfortunately, channel 2 of the prototype board was not functional, but for this preliminary design and evaluation of the board it was not considered problematic.

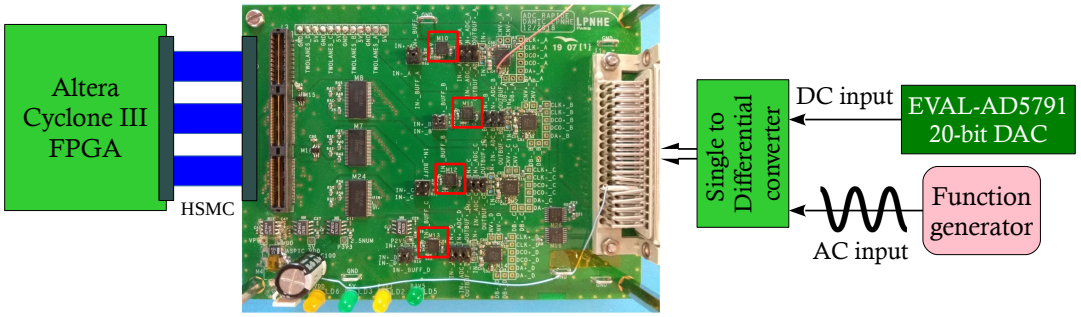

Figure 6.3: Schematic of the Rapide board evaluation setup with DC and AC input signal sources. The ADC chips are marked on the board photo in the red squares.

6.2.1 Input noise

The noise of each ADC channel was measured by shorting both inputs to a low noise reference voltage. The chip itself produces a low-noise 2.048 V output that is used for the common mode output voltage. About 10 k samples are acquired per channel. The results for channels 0, 1, 3 are presented in Figure 6.4. The input noise of the ADC is calculated as the sigma of the Gaussian fit on the raw data distribution, shown with a solid line on the histogram top right. The results:

$$\sigma(\text{Ch0}) = 1.577 \pm 0.010\,\text{ADU},\ \ \sigma(\text{Ch1}) = 1.611 \pm 0.013\,\text{ADU},$$
$$\sigma(\text{Ch3}) = 1.474 \pm 0.007\,\text{ADU}.$$

The expected noise based on the datasheet of the chip is 1.4 LSB_{RMS} (referred as transition noise). The slightly higher noise that is measured here could come from the fact that there are many electronic components on the prototype board, maybe not in the optimal orientation. Yet, the measured values with a maximum of ∼1.6 LSB is close to the expected one, about 15% higher, and is considered acceptable. This value will be converted into voltage units after the following linearity study. The deviation of $\mathcal{O}(1\,\text{ADU})$ of the data

from the expected zero is not yet understood. As the two inputs are shorted, the ADC should output 0 ADU. The amplitude spectral density on the bottom plot is flat, indicating no extreme oscillating noise affecting the ADCs.

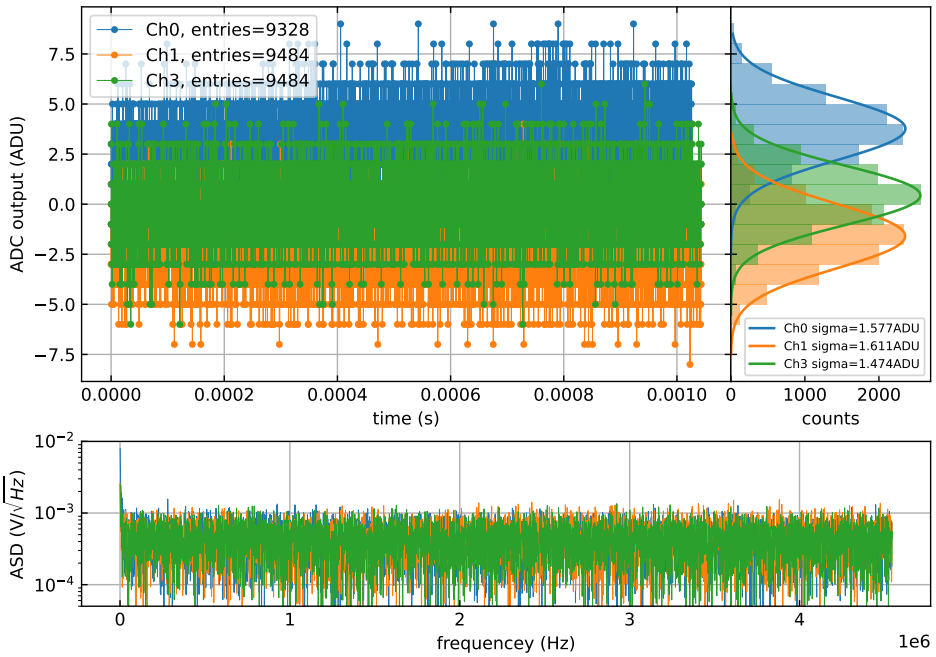

Figure 6.4: Rapide board input noise study. Raw data (top left) and their distribution on a histogram with a Gaussian fit (solid line) applied (top right) and the amplitude spectral density using FFT (bottom).

DAC single-ended output converted into differential

The following tests require some input signal to the ADC that must first be converted into differential. So prior to them, a characterization of the converter board at the output of the EVAL-AD5791 is necessary. The execution of this test is identical to the evaluation of the DAC itself, with the only difference being that the multimeter receives the voltage as differential. The gain of the fully differential amplifier of the converter board is equal to 1, so the differential output value should be equal to the DAC output. The results are shown in Figure 6.5. About 200 points cover a range of ±4 V, which is the input range of the ADC board. From the linear fit on the data, there seems to be a slight change in the value of the LSB and the error of this value is significantly higher than what was measured directly from the DAC. In addition, the INL on the bottom plot (blue points) shows a strongly shaped curve that spans in a range of about ±20 LSB. In order to correct for this unspecified defect, a 7th degree polynomial fit is applied (black line) and the corrected INL is also shown (orange points). The correction suppresses the INL in a less than ±2 LSB span in almost the whole range excluding the edges where it is not as effective. This will be taken into consideration for the ADC evaluation in the following section.

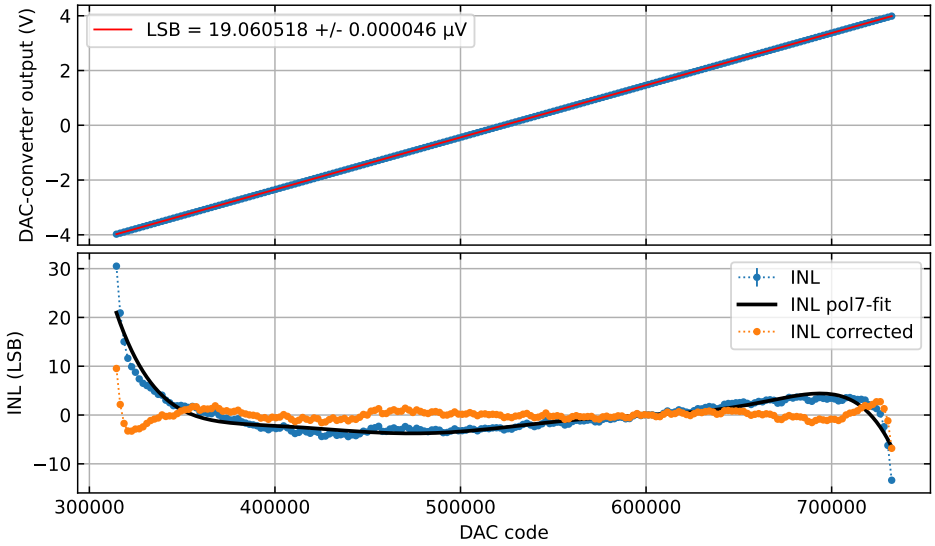

Figure 6.5: Converter board output vs DAC input code (top) and the INL (bottom).

6.2.2 Linearity study with DC input signal

The linearity response of the ADC is measured experimentally to calibrate the 1 ADU in volts. DC signals with a fixed step using the EVAL-AD5791 being converted to differential are sent to the ADC. This test is similar to the evaluation of the previous one, but this time the DAC/converter output is calibrated and instead of the multimeter we are using the Rapide board. A representative characterization dataset for each channel is presented in Figure 6.6. About 100 different input levels cover the whole range of the ADC.

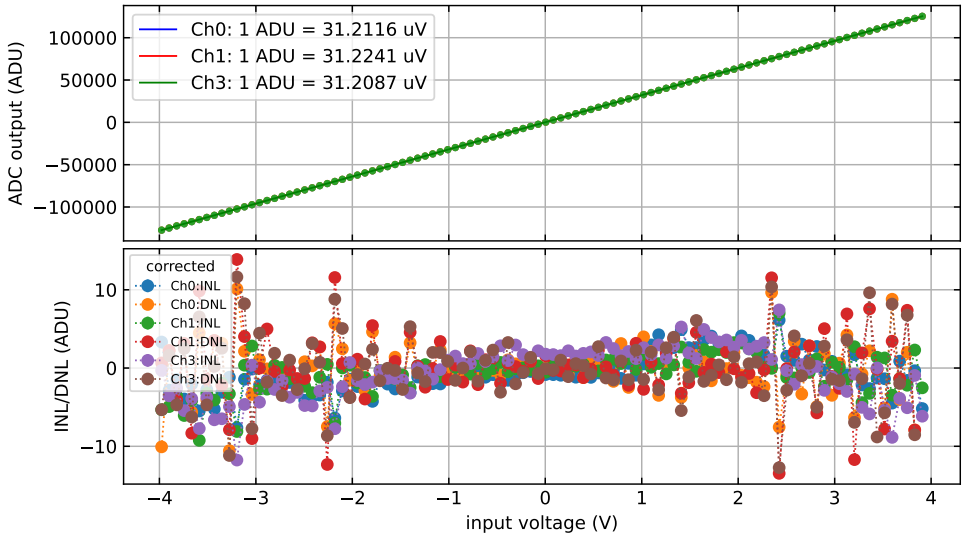

Figure 6.6: ADC output vs input voltage (top) and the INL/DNL (bottom).

A linear fit is applied on the top plot, from which is derived the value of the ADU. The data of all channels are not visible because of overlapping.

$$1\,\text{ADU(Ch0)} = 31.2116 \pm 0.0001\,\mu\text{V},\ 1\,\text{ADU(Ch1)} = 31.2241 \pm 0.0001\,\mu\text{V},$$

$$1\,\text{ADU(Ch3)} = 31.2087 \pm 0.0001\,\mu\text{V}.$$

The error of values above is derived from the linear fit. As a reminder, the theoretical value of the ADU is $8.192\,\mathrm{V}/2^{18} = 31.25\,\mu\mathrm{V}$. The experimental values are measured ∼0.1% lower than expected. On the bottom plot of Figure 6.6, the INL and DNL of the data are shown in ADU. The correction for the converter board is applied on these variables resulting to a maximum range for the INL/DNL of ±10 ADU, while in the input range of ±2 V they are lower than 5 ADU. In any case, the INL and DNL are expected to have a typical value lower than 1 ADU. The measured values differ from the expected ones with an factor of up to 10. This is not a surprise if one considers that the Rapide board is a prototype and there is a converter board that knowingly introduces noise and some defect to the ADC input signal.

6.2.3 ADC evaluation for AC input signals

A function generator produces sinusoidal signals of given amplitude and frequency which are injected as input to the Rapide board. The amplitude of the signal is high enough to cover almost the full range (>99%) of the ADC input. The input frequency is specifically chosen as $\mathrm{f}_{sampling}/2^7$, so that the samples on every period of the signal are more or less at the same phase. The number of samples per period is equal to 2^7 as the product of the input signal period and the sampling frequency. Figure 6.7 top shows a typical set of data in the timescale of one period, which is ∼14 μs for this example. The total number of recorded periods is indicated on the plot. A sinus function is fitted on the raw data. The residuals from the fit line are overlapped in a single-period time and are presented in the middle plot. The shaping defect of the converter board is observed. A shape similar to Figure 6.5, which corresponds to the full input range, can be seen between 4 μs and 11 μs. The residuals span ∼ ±100 ADU, which is higher by a factor of 10 with respect to the linearity study. No correction is applied here since it is mainly the "thickness" of the residuals rather than the shape that is large. The signal generator can potentially introduce the extra noise that is observed, which is shaped and amplified by the converter board. The amplitude spectral density using FFT is also presented on the bottom plot, showing a high peak at a frequency that agrees with the input signal one and lower ones that correspond to the harmonics of the signal at multiples of the input frequency.

6.2.4 ADC cross-talk evaluation for AC input signals

Finally, the cross-talk between the ADC channels is measured. The previous section's analysis focuses on the data of the channel to which the AC input signal is injected. The differential inputs of the other channels are shorted together and at the low noise voltage reference as in the input noise study. An example of this analysis is shown in Figure 6.8, where the signal is sent to channel 3 (aggressor) and the cross-talk on channels 0 and 1 (victim) is measured. The cross-talk values for all channels are presented in Table 6.1. Recall the input noise measured in section 6.2.1. The cross-talk is in agreement with the

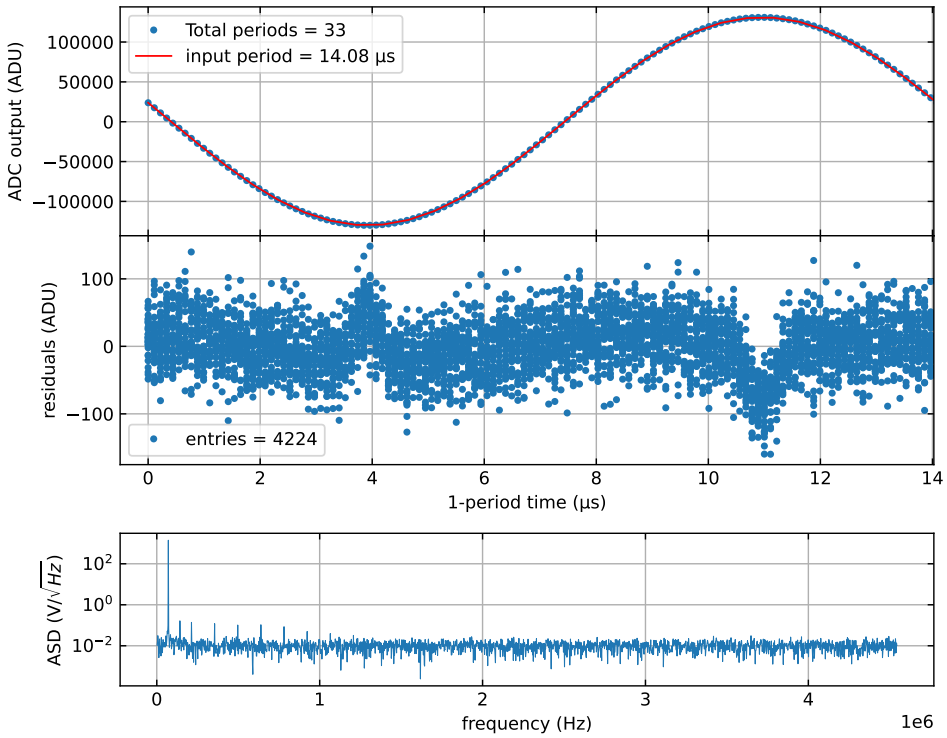

Figure 6.7: A typical example of the ADC output for a sinus input signal in a timescale of one period, with the raw data and a fit applied (top), the residuals from the fitted curve (middle) and the amplitude spectral density using FFT (bottom).

input noise measured for channels 0 and 1 and <5% higher for channel 3. The amplitude spectral density is also flat and on the same scale as the input noise spectrum.

The cross-talk depends highly on the physical configuration of the electronic components on a board. That channel 2 of the board is not working for unspecified reasons, which could potentially be a source of noise or even a noise-protecting barrier between the channels, so this result is only preliminary. Additionally, this prototype design is not compatible with the specifications of an ADC board to be plugged to the ODILE and so a completely new physical design is necessary. However, this study indicates the absence of any extreme cross-talk between the channels, which is promising for the next version of the ADC board for DAMIC-M.

signal to\noise of	Ch0	Ch1	Ch3
Ch0	x	1.611 ± 0.031 ADU	1.504 ± 0.032 ADU
Ch1	1.569 ± 0.031 ADU	x	1.532 ± 0.009 ADU
Ch3	1.567 ± 0.019 ADU	1.619 ± 0.012 ADU	x

Table 6.1: Complete cross-talk study for all (functional) channels of the Rapide board.

Conclusion on the 4-channel LTC2387-18 ADC Rapide board

The prototype Rapide board has been successfully developed and was evaluated in Paris. The results seem to follow to some extend what was expected and they are promising, with

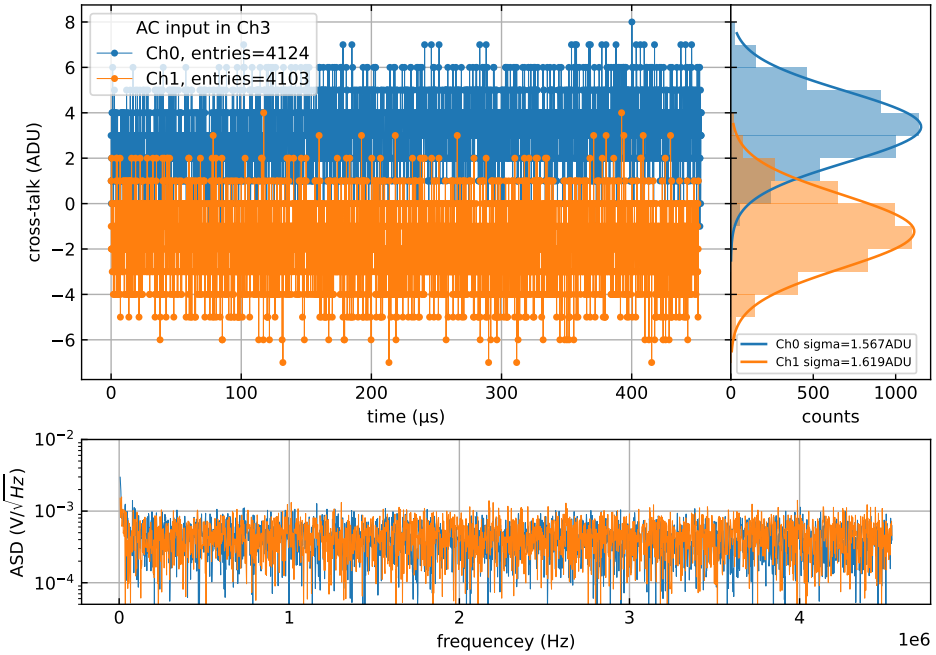

Figure 6.8: An example of the Rapide board cross-talk study, sending an input signal to channel 3 and measuring the noise of channels 0 and 1. Raw data (top left) and their distribution on a histogram with a Gaussian fit (solid line) applied (top right) and the amplitude spectral density using FFT (bottom).

a quite good noise of about 1.6 ADU. Yet, the ADC was not tested at its full potential due to FPGA limitations. A new design of the LTC2387-18 ADC board is required compatible with the ODILE specifications. The next section summarizes briefly the work done on all ADC candidates that lead to the final decision.

6.3 New ODILE-compatible ADC boards for DAMIC-M

The Zurich group of DAMIC-M took over the production of the boards for the 3 ADC candidates. ODILE-compatible boards were developed with 4 identical channels to readout the 4 CROC outputs, and they were characterized thoroughly. Figure 6.9 shows a photo of the LTC2387-18 board. The other two boards look identical to this one. The ADC board is designed to connect to the ODILE through a single HSMC connector. Even though the power supply voltages can be delivered by the ODILE, it is also possible to power up the board with an external source through the pins on the left side of the photo. A single 15-pin Dsub or an HDMI connector is used to deliver the signal to the board.

Table 6.2 shows some characteristics and the typical input noise measured of each ADC board, where f_S is the sampling frequency and 1 ADUth is the expected value of the ADC output code. In an absolute value, the LTC2387-18 seems to have the highest noise. However, in a sampling period $1/f_S$ of the slowest ADC, MAX11905, the other ADCs will acquire more samples. From the statistics, the noise will go down as $1/\sqrt{f_S/f_S^{min}}$. In the last column of Table 6.2, there is the normalized input noise for a sampling frequency equal

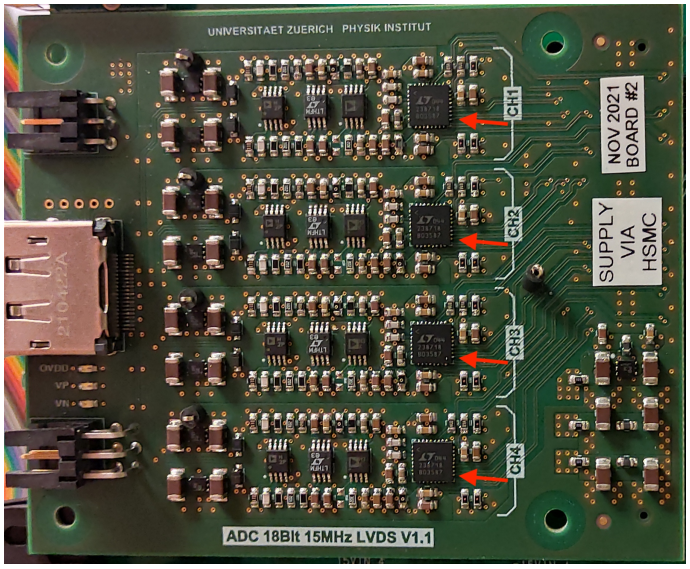

Figure 6.9: Photo of the LTC2387-18 ADC board design compatible with ODILE. The red arrows are pointing to the ADC chips.

ADC	f_S (MHz)	N-bits	in. range (V_{pp})	theor. 1 ADU	in. noise (ADU)	in. noise (μV)	normalize for f_S (μV)
LTC2387-18	15	18	8.192	31.25	1.7	53.1	17.35
AD4020	1.8	20	10	9.54	3.5	33.4	31.48
MAX11905	1.6	20	6	5.72	8	45.8	45.76

Table 6.2: Summary of all 3 ADC candidate boards measured input noise.

to MAX11905's, $f_S^{min} = 1.6\,\text{MHz}$. As a result, the high sampling speed of LTC2387-18 can surpass the resolution of the 20-bit ADCs by more than 40%. Additionally, the multiple raw data may allow a deeper analysis of the video signal of the CCD, although they occupy more memory and are more difficult to process. Nevertheless, it remains available as an option. All the boards have been integrated in the ODILE system. A preprocessing block in the firmware of ODILE for the LTC2387-18 is averaging the acquired samples for given periods, reducing the volume of the raw output data. In conclusion, the collaboration has decided to continue with the LTC2387-18 option for the final DAMIC-M experiment.

Conclusions

The DAMIC-M is an experiment dedicated to the search for dark matter through its direct interaction with the silicon bulk of scientific-grade CCDs. The detector will commission about 50 CCD packages with a total target mass of $\sim$1 kg. Compared to the previous experiment of DAMIC, the new detector will feature skipper readout that will allow for a resolution of a fraction of an electron, will have a low background in the order of 0.1 dru, and will improve the control and readout of the CCD with a new custom made acquisition system.

This work summarized the R&D progress toward the new electronics I contributed to during my thesis at the LPNHE lab in Paris. It was focused on developing the control software and the new sequencer files, the evaluation of several modules that were produced, and the overall assembly of an integrated new system. In order to achieve this, a deep understanding of the CCD operation was necessary as well as the requirements of a system to support a detector for such a rare event search with the goal of a very low detection energy threshold. The electronics-oriented tasks enhanced my skills in working with integrated chips and electronic boards.

In particular, there has been great progress in each of the individual parts of this new system. A preliminary version of the control board, providing the necessary signals for the CCD exposure and readout, has been evaluated and was able to operate in a CCD setup and successfully acquired images with visible tracks. Three front-end chip versions have been developed and evaluated. Due to the several problems that were observed, a simpler preamplifier compared to the original sophisticated with many capabilities design, will most likely be used for the final setup. The noise that was achieved by these chips is as low as 1-2 e^- in charge units for the DAMIC-M CCDs. The choice for the ADC to be used is already made, with the 18-bit 15 MS/s LTC2387-18 being the most efficient and low-noise option, and the new board has been extensively used at surface labs by the different groups of the collaboration. A preliminary system constituted exclusively by the new electronics was tested with a CCD and successfully recorded images with visible particle tracks.

Although not final, there has been a great advancement in the DAMIC-M acquisition system. I have contributed with my work to this progress with the evaluation of the various modules, proving them capable or not to be used for the final DAMIC-M setup.

The development of the top-level control software I have worked on allows the current and future users to perform tests with the CCDs in a relatively easy and flexible way. Moreover, new sequencer files are prepared for use and can be easily adjusted to the necessities of future tests. A final acquisition system for DAMIC-M is not far from complete and my work was essential to reach this point. However, it must be continued in order to achieve the goals set for this novel CCD control system for the dark matter search.

Appendix A

CABAC chip programming

The CABAC chip has a 24-bit register. This means that the user communicates with the chip with messages of 24-bit or 6-digit hexadecimal (1 hex = 4 bit), sent with MOSI or received by MISO. This word follows the syntax:

BBBB BBBB BBBB BBBB BBBB BBBB
Write/Read=1/0 address 00:MBZ data

The *write/read* bit defines if the master will change the register of the chip or if the chip will return what is already written in its register, respectively. The 5-bit *address* offers a total of 32 codes to communicate with each of the CABAC's sources, like the bias outputs and the current control of the clocks. There is an additional address that sets each clock individually in a readout or exposure mode. Practically, the exposure mode puts the clocks to sleep lowering their consumption by a factor of 10. This optional mode may find application in the final experiment where there will be long periods of exposure. If DAMIC-M decides to operate the CCD with continuous readout, this option will not be useful. *MBZ* stands for "Must Be Zero" and the two bits should simply always be zero. The 16-bit last part of the word holds the information to write to or read from the address of the chip.

The CABAC register captures the value of the MOSI at the rising edge of the SCLK pulse. MOSI changes to the next bit state at the falling edge of the SCLK pulse. This is the phase the CABAC is designed to be controlled with. The MISO signal is only generated at a read request. This is achieved by the first bit of MOSI requesting a readback from the given address and the chip ignores the rest which is the data part. The MISO signal follows after the MOSI as a 24-bit word returning the written value in the requested address. When the 10-bit DACs are programmed for bias production, only the last 10 bits of the data part are important; the first 6 can stay at zero. The current of a clock is set by changing both the rise and fall slopes at the same time. The 16 bits of the data part are divided in half with the first 8 bits concerning the rising edge and the last 8 the falling edge. One can change a single slope only by obtaining the latest value of the other slope first and then using this as input for the word to write. The readout/exposure mode uses the last 8 bits of the data, each bit dedicated to one clock.

Appendix B

Fully differential integrator

The schematic of Figure B.1 represents an RC integrator using a fully differential operational amplifier [1,2]. The two resistors (R) and the two capacitors (C) are considered to be equal for symmetry.

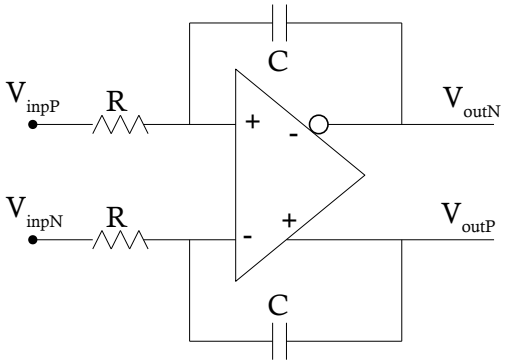

Figure B.1: Schematic of a fully differential integrator.

For an integration time equal to T_{int}, the differential output (V_{out}) will generally be equal to [110]:

$$V_{out} = V_{outP} - V_{outN} = -\frac{T_{int}}{RC}(V_{inpP} - V_{inpN}) \tag{B.1}$$

In the case of CROC (both v1 and v2), one of the input signals is always at a fixed reference voltage. The other is the single-ended video signal from the CCD, amplified by the first stage of CROC. The input signal and the reference cannot be labeled as $V_{inpP/N}$, because their connection to the amplifier is not fixed. Two logic timing signals, Ramp Down (RD) and Ramp Up (RU), control switches that connect the right side of the resistors to the inputs of the amplifier, as it is shown in Figure B.2.

The RD and RU timing signals are send synchronously to the *pedestal* and *signal* levels of the video signal. For equal integration times T_{int}, the differential output following the equation B.1 for the two levels will be:

$$V_{out}(pedestal) = \frac{T_{int}}{RC}(V_{ref} - pedestal) \;\; \& \;\; V_{out}(signal) = \frac{T_{int}}{RC}(signal - V_{ref})$$

Between the two integration phases, none of the RD and RU is active and the inputs of

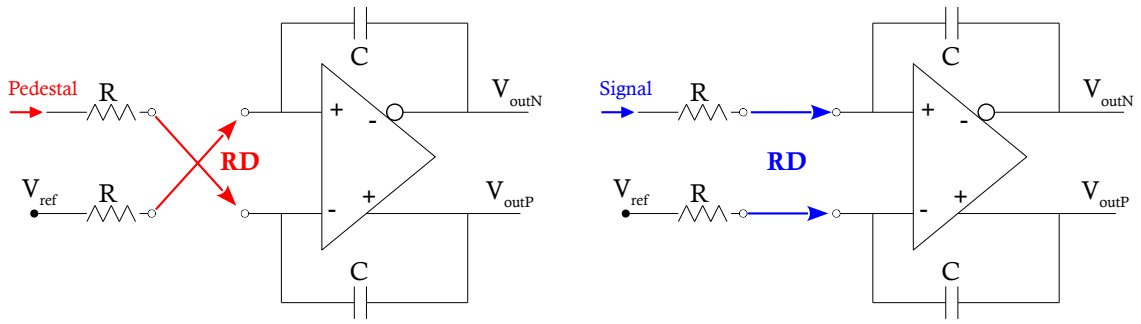

Figure B.2: Connectivity of the second amplifier of CROC when RD (left) and RU (right) signals are high.

the amplifier are isolated. As a result, the potential at its output will remain intact. In the end, the total output after both RD and RU results to:

$$V_{final} = V_{out}(pedestal) + V_{out}(signal) = \frac{T_{int}}{RC} V_Q$$

where $signal = pedestal + V_Q$, and V_Q is the pixel charge that changed the potential of the sense node of the output amplifier of the CCD.

Bibliography

[1] P. Ball, The Elements: A Very Short Introduction, Press Monographs, Oxford University Press, 2004.

[2] Planck Collaboration, Planck 2018 results. VI. Cosmological parameters, 641 (2020) A6. arXiv:1807.06209, doi:10.1051/0004-6361/201833910.

[3] H. Poincaré, La Voie lactée et la théorie des gaz, Bulletin de la société astronomique de France 20 (1906) 153–165.

[4] F. Bessel, On the variations of the proper motions of Procyon and Sirius, 6 (1844) 136–141. doi:10.1093/mnras/6.11.136.

[5] A. Secchi, L' Astronomia in Roma nel pontificato di Pio IX. Memoria, Tipografia della Pace, Roma, 1877.

[6] W. Thomson, Baron Kelvin, Baltimore Lectures on Molecular Dynamics and the Wave Theory of Light, Cambridge Library Collection - Physical Sciences, Cambridge University Press, 1904. doi:10.1017/CBO9780511694523.

[7] J. Kapteyn, First Attempt at a Theory of the Arrangement and Motion of the Sidereal System, 55 (1922) 302. doi:10.1086/142670.

[8] J. Oort, The force exerted by the stellar system in the direction perpendicular to the galactic plane and some related problems, 6 (1932) 249.

[9] P. van der Kruit, Lessons from the milky way: The kapteyn universedoi:10.1007/978-3-319-10614-4_2.

[10] F. Zwicky, Die Rotverschiebung von extragalaktischen Nebeln, Helvetica Physica Acta 6 (1933) 110–127.

[11] F. Zwicky, On the Masses of Nebulae and of Clusters of Nebulae, The Astrophysical Journal 86 (1937) 217. doi:10.1086/143864.

[12] J. P. Hughes, The Mass of the Coma Cluster: Combined X-Ray and Optical Results, 337 (1989) 21. doi:10.1086/167084.

[13] K. Rines, M. Geller, M. Kurtz, A. Diaferio, T. Jarrett, J. Huchra, Infrared Mass-to-Light Profile throughout the Infall Region of the Coma Cluster, 561 (1) (2001) L41–L44. arXiv:astro-ph/0109425, doi:10.1086/324457.

[14] S. Smith, The Mass of the Virgo Cluster, 83 (1936) 23. doi:10.1086/143697.

[15] H. W. Babcock, The rotation of the Andromeda Nebula, Lick Observatory Bulletin 498 (1939) 41–51. doi:10.5479/ADS/bib/1939LicOB.19.41B.

[16] H. Hellwig, et al, Measurement of the unperturbed hydrogen hyperfine transition frequency, IEEE Transactions on Instrumentation and Measurement 19 (4) (1970) 200–209. doi:10.1109/TIM.1970.4313902.

[17] V. Rubin, K. Ford, Rotation of the Andromeda Nebula from a Spectroscopic Survey of Emission Regions, 159 (1970) 379. doi:10.1086/150317.

[18] V. Rubin, W. Ford, N. Thonnard, Rotational properties of 21 SC galaxies with a large range of luminosities and radii, from NGC 4605 (R=4kpc) to UGC 2885 (R=122kpc)., 238 (1980) 471–487. doi:10.1086/158003.

[19] D. Rogstad, G. Shostak, Gross Properties of Five Scd Galaxies as Determined from 21-centimeter Observations, 176 (1972) 315. doi:10.1086/151636.

[20] M. S. Roberts, A High-Resolution 21-CM Hydrogen-Line Survey of the Andromeda Nebula, 144 (1966) 639. doi:10.1086/148645.

[21] M. Roberts, A. Rots, Comparison of Rotation Curves of Different Galaxy Types, 26 (1973) 483–485.

[22] M. Milgrom, A modification of the Newtonian dynamics as a possible alternative to the hidden mass hypothesis., 270 (1983) 365–370. doi:10.1086/161130.

[23] J. D. Bekenstein, Relativistic gravitation theory for the mond paradigm, Physical Review D (2004) 083509.

[24] S. Boran, S. Desai, E. Kahya, R. Woodard, GW170817 falsifies dark matter emulators, Physical Review D 97 (4). doi:10.1103/physrevd.97.041501.

[25] E. Corbelli, P. Salucci, The extended rotation curve and the dark matter halo of M33, Monthly Notices of the Royal Astronomical Society 311 (2) (2000) 441–447. doi:10.1046/j.1365-8711.2000.03075.x.

[26] Y. Sofue, Distribution of Dark Matter in Bulge, Disk and Halo Inferred from High-Accuracy Rotation Curves, in: F. Combes, G. A. Mamon, V. Charmandaris (Eds.), Dynamics of Galaxies: from the Early Universe to the Present, Vol. 197 of Astronomical Society of the Pacific Conference Series, 2000, p. 83. arXiv:astro-ph/9910004.

[27] V. Belokurov, et al, The cosmic horseshoe: Discovery of an einstein ring around a giant luminous red galaxy, The Astrophysical Journal 671 (1) (2007) L9–L12. doi:10.1086/524948.
URL https://doi.org/10.1086/524948

[28] M. Bartelmann, P. Schneider, Weak gravitational lensing, Physics Reports 340 (4-5) (2001) 291–472. doi:10.1016/s0370-1573(00)00082-x.

[29] W. Tucker, H. Tananbaum, R. Remillard, A Search for "Failed Clusters" of Galaxies, 444 (1995) 532. doi:10.1086/175627.

[30] W. Tucker, P. Blanco, S. Rappoport, L. David, D. Fabricant, E. Falco, W. Forman, A. Dressler, M. Ramella, 1E 0657-56: A Contender for the Hottest Known Cluster of Galaxies, 496 (1) (1998) L5–L8. arXiv:astro-ph/9801120, doi:10.1086/311234.

[31] M. Markevitch, et al, A Textbook Example of a Bow Shock in the Merging Galaxy Cluster 1E 0657-56, 567 (1) (2002) L27–L31. arXiv:astro-ph/0110468, doi:10.1086/339619.

[32] D. Clowe, et al, A direct empirical proof of the existence of dark matter, The Astrophysical Journal 648 (2) (2006) L109–L113. doi:10.1086/508162.

[33] M. Bradač, S. W. Allen, T. Treu, H. Ebeling, R. Massey, R. G. Morris, A. von der Linden, D. Applegate, Revealing the properties of dark matter in the merging cluster MACS j0025.4-1222, The Astrophysical Journal 687 (2) (2008) 959–967. doi:10.1086/591246.
URL https://doi.org/10.1086/591246

[34] A. Penzias, R. Wilson, A Measurement of Excess Antenna Temperature at 4080 Mc/s., 142 (1965) 419–421. doi:10.1086/148307.

[35] G. F. Smoot, COBE observations and results, in: Conference on 3K cosmology, ASCE, 1999. doi:10.1063/1.59326.

[36] G. Hinshaw, et al, Nine-year Wilkinson Microwave Anisotropy Probe WMAP observations: Cosmological parameter results 208 (2) (2013) 19. doi:10.1088/0067-0049/208/2/19.

[37] D. Fixsen, The Temperature of the Cosmic Microwave Background, 707 (2) (2009) 916–920. arXiv:0911.1955, doi:10.1088/0004-637X/707/2/916.

[38] B. Carr, F. Kühnel, Primordial black holes as dark matter: Recent developments, Annual Review of Nuclear and Particle Science 70 (1) (2020) 355–394. doi:10.1146/annurev-nucl-050520-125911.

[39] A. Boyarsky, M. Drewes, T. Lasserre, S. Mertens, O. Ruchayskiy, Sterile neutrino dark matter, Progress in Particle and Nuclear Physics 104 (2019) 1–45. doi:10.1016/j.ppnp.2018.07.004.

[40] L. Roszkowski, E. M. Sessolo, S. Trojanowski, WIMP dark matter candidates and searches—current status and future prospects, Reports on Progress in Physics 81 (6) (2018) 066201. doi:10.1088/1361-6633/aab913.

[41] M. Ibe, W. Nakano, Y. Shoji, K. Suzuki, Migdal effect in dark matter direct detection experiments, Journal of High Energy Physics 2018 (3) (2018) 194. doi:10.1007/JHEP03(2018)194.

[42] M. J. Dolan, F. Kahlhoefer, C. McCabe, Directly detecting sub-gev dark matter with electrons from nuclear scattering, Phys. Rev. Lett. 121 (2018) 101801. doi:10.1103/PhysRevLett.121.101801.

[43] T. M. Undagoitia, L. Rauch, Dark matter direct-detection experiments, Journal of Physics G: Nuclear and Particle Physics 43 (1) (2015) 013001. doi:10.1088/0954-3899/43/1/013001.

[44] M. Fabbrichesi, E. Gabrielli, G. Lanfranchi, The Physics of the Dark Photon, Springer International Publishing, 2021. doi:10.1007/978-3-030-62519-1.

[45] E. Aprile, et al, Emission of single and few electrons in XENON1T and limits on light dark matter (2021). doi:10.48550/ARXIV.2112.12116.

[46] J. H. Christenson, J. W. Cronin, V. L. Fitch, R. Turlay, Evidence for the 2π decay of the k_2^0 meson, Phys. Rev. Lett. 13 (1964) 138–140. doi:10.1103/PhysRevLett.13.138.

[47] R. D. Peccei, H. R. Quinn, Constraints Imposed by CP Conservation in the Presence of Instantons, Phys. Rev. D 16 (1977) 1791–1797. doi:10.1103/PhysRevD.16.1791.

[48] M. Kuster, Axions - Theory, Cosmology and Experimental Searches, Vol. 741, 2008. doi:10.1007/978-3-540-73518-2.

[49] M. Felcini, Searches for dark matter particles at the lhc (2018). doi:10.48550/ARXIV.1809.06341.

[50] C. P. d. l. Heros, Status of direct and indirect dark matter searches (2020). doi:10.48550/ARXIV.2001.06193.

[51] N. Iovine, J. A. Aguilar, Indirect search for dark matter in the galactic centre with icecube (2021). doi:10.48550/ARXIV.2107.11224.

[52] A. Albert, et al, Search for dark matter towards the galactic centre with 11 years of ANTARES data, Physics Letters B 805 (2020) 135439. doi:10.1016/j.physletb.2020.135439.

[53] M. Aguilar, et al, The Alpha Magnetic Spectrometer (AMS) on the international space station: Part II — Results from the first seven years, Physics Reports 894 (2021) 1–116. doi:https://doi.org/10.1016/j.physrep.2020.09.003.

[54] O. Adriani, et al, An anomalous positron abundance in cosmic rays with energies 1.5-100 gev, Nature 458 (2009) 607–9. doi:10.1038/nature07942.

[55] R. Agnese, et al, Search for low-mass dark matter with CDMSlite using a profile likelihood fit, Physical Review D 99 (6). doi:10.1103/physrevd.99.062001.

[56] E. Armengaud, et al, Constraints on low-mass WIMPs from the EDELWEISS-III dark matter search, Journal of Cosmology and Astroparticle Physics 2016 (05) (2016) 019–019. doi:10.1088/1475-7516/2016/05/019.

[57] A. Abdelhameed, et al, First results from the CRESST-III low-mass dark matter program, Physical Review D 100 (10). doi:10.1103/physrevd.100.102002.

[58] N. Castelló-Mor, DAMIC-M experiment: Thick, silicon CCDs to search for light dark matter, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 958 (2020) 162933. doi:10.1016/j.nima.2019.162933.

[59] L. Barak, et al, Sensei: Direct-detection results on sub-gev dark matter from a new skipper ccd, Phys. Rev. Lett. 125 (2020) 171802. doi:10.1103/PhysRevLett.125.171802.

[60] E. Aprile, et al, Light dark matter search with ionization signals in XENON1t, Physical Review Letters 123 (25). doi:10.1103/physrevlett.123.251801.

[61] D. Akerib, et al, Extending light WIMP searches to single scintillation photons in LUX, Physical Review D 101 (4). doi:10.1103/physrevd.101.042001.

[62] C. Cheng, et al, Search for light dark matter–electron scattering in the PandaX-II experiment, Physical Review Letters 126 (21). doi:10.1103/physrevlett.126.211803.

[63] P. Agnes, et al, DarkSide-50 532-day dark matter search with low-radioactivity argon, Physical Review D 98 (10). doi:10.1103/physrevd.98.102006.

[64] Q. Arnaud, et al, First results from the NEWS-G direct dark matter search experiment at the LSM, Astroparticle Physics 97 (2018) 54–62. doi:10.1016/j.astropartphys.2017.10.009.

[65] New CAST limit on the axion–photon interaction, Nature Physics 13 (6) (2017) 584–590. doi:10.1038/nphys4109.

[66] J. Galan, Exploring the sun's core with BabylAXO, Journal of Physics: Conference Series 2156 (1) (2021) 012014. doi:10.1088/1742-6596/2156/1/012014.

[67] R. Essig, G. K. Giovanetti, N. Kurinsky, D. McKinsey, K. Ramanathan, K. Stifter, T.-T. Yu, Snowmass2021 cosmic frontier: The landscape of low-threshold dark matter direct detection in the next decade (2022). doi:10.48550/ARXIV.2203.08297.

[68] A. Aguilar-Arevalo, et al, Results on low-mass weakly interacting massive particles from an 11 kg d target exposure of DAMIC at SNOLAB, Physical Review Letters 125 (24). doi:10.1103/physrevlett.125.241803.

[69] R. Chun, A high voltage charge-coupled device (ccd) controller asic for the large synoptic survey telescope (lsst), Modeling Identification and Control - MODEL IDENT CONTR Master's Thesis, University of Tennessee (2010).
URL https://trace.tennessee.edu/utk_gradthes/613

[70] S. Holland, Fully depleted back illuminated CCD Patent number: 6259085.
URL https://patents.justia.com/patent/6259085

[71] M. Komperød, B. Lie, Empirical modeling of heating element power for the czochralski crystallization process, Modeling Identification and Control - MODEL IDENT CONTR 31 (2010) 19–34. doi:10.4173/mic.2010.1.2.

[72] C. Leitz, et al, Germanium CCDs for large-format SWIR and X-ray imaging, Journal of Instrumentation 12 (2017) C05014–C05014. doi:10.1088/1748-0221/12/05/C05014.

[73] I. Deyhimy, W. Hill, R. Anderson, Continuously clocked 1 GHz GaAs CCD, IEEE Electron Device Letters 2 (3) (1981) 70–72. doi:10.1109/EDL.1981.25344.

[74] J. Janesick, Scientific Charge-Couple Devices, Bellingham, WA: SPIE Optical Engineering Press, 2001, xvi, 906 p. SPIE Press monograph, PM 83. ISBN 0819436984 83. doi:10.1117/12.7974139.

[75] S. Holland, Fabrication of detectors and transistors on high-resistivity silicon, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 275 (3) (1989) 537–541. doi:https://doi.org/10.1016/0168-9002(89)90741-9.

[76] C. Bebek, et al, CCD research and development at Lawrence Berkeley National Laboratory, in: A. D. Holland, J. W. Beletic (Eds.), High Energy, Optical, and Infrared Detectors for Astronomy V, Vol. 8453, International Society for Optics and Photonics, SPIE, 2012, pp. 27 – 42. doi:10.1117/12.926606.

[77] J. Janesick, Photon transfer: DN → λ, Bellingham, WA: SPIE Press, 2007, xiv, 258 p. SPIE monograph, PM 170. ISBN 0819467227doi:https://doi.org/10.1117/3.725073.

[78] M. Mazziotta, Electron–hole pair creation energy and fano factor temperature dependence in silicon, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 584 (2) (2008) 436–439. doi:https://doi.org/10.1016/j.nima.2007.10.043.

[79] R. Stover, et al, High-performance CCD on high-resistivity silicon, in: M. Wei, X. Yi, J. Han, F. F. Sizov (Eds.), Imaging System Technology for Remote Sensing, Vol. 3505, International Society for Optics and Photonics, SPIE, 1998, pp. 13 – 18. doi:10.1117/12.317844.

[80] S. Holland, et al, A 200 × 200 CCD image sensor fabricated on high-resistivity silicon, International Electron Devices Meeting. Technical Digest (1996) 911–914.

[81] R. J. Stover, et al, Characterization of a fully depleted CCD on high-resistivity silicon, in: M. M. Blouke (Ed.), Solid State Sensor Arrays: Development and Applications, Vol. 3019, International Society for Optics and Photonics, SPIE, 1997, pp. 183 – 188. doi:10.1117/12.275174.

[82] S. Holland, et al, Fully depleted, back-illuminated charge-coupled devices fabricated on high-resistivity silicon, IEEE Transactions on Electron Devices 50 (1) (2003) 225–238. doi:10.1109/TED.2002.806476.

[83] D. Burt, et al, Improving radiation tolerance in e2v CCD sensors, in: P. G. Warren, C. J. Marshall, J. B. Heaney, E. T. Kvamme, R. K. Tyson, M. Hart (Eds.), Astronomical and Space Optical Systems, Vol. 7439, International Society for Optics and Photonics, SPIE, 2009, pp. 15 – 24. doi:10.1117/12.825273.

[84] G. Hopkinson, Cobalt60 and proton radiation effects on large format, 2-D, CCD arrays for an Earth imaging application, IEEE Transactions on Nuclear Science 39 (6) (1992) 2018–2025. doi:10.1109/23.211399.

[85] L. Barak, et al, SENSEI: Characterization of single-electron events using a skipper charge-coupled device, Physical Review Applied 17 (1). doi:10.1103/physrevapplied.17.014022.

[86] N. Saks, A technique for suppressing dark current generated by interface states in buried channel CCD imagers, IEEE Electron Device Letters 1 (7) (1980) 131–133. doi:10.1109/EDL.1980.25259.

[87] S. Holland, et al, High-voltage-compatable fully depleted CCDs, Proceedings of SPIE - The International Society for Optical Engineering 6276. doi:10.1117/12.672393.

[88] M. Lesser, A summary of charge-coupled devices for astronomy, Publications of the Astronomical Society of the Pacific 127 (957) (2015) 1097–1104. doi:10.1086/684054.

[89] M. Robbins, Radiation damage effects in charge coupled devices, Master's Thesis, Brunel University (1992).

[90] S. Holland, et al, Technology development for 4k × 4k, back-illuminated, fully depleted scientific CCD imagers, Vol. 3, 2007, pp. 2220 – 2225. doi:10.1109/NSSMIC.2007.4436592.

[91] G. Fernandez Moroni, et al, Sub-electron readout noise in a Skipper CCD fabricated on high resistivity silicon, Experimental Astronomy 34. doi:10.1007/s10686-012-9298-x.

[92] M. Haro, et al, Measurement of the read-out noise of fully depleted thick CCDs, in: 2016 Argentine Conference of Micro-Nanoelectronics, Technology and Applications (CAMTA), 2016, pp. 11–16. doi:10.1109/CAMTA.2016.7574083.

[93] G. Cancelo, et al, Low Threshold Acquisition controller for Skipper CCDs (2020). doi:10.48550/ARXIV.2004.07599.

[94] J. Estrada, J. Molina, J. Blostein, G. Fernández, Plasma effect in silicon charge coupled devices (CCDs), Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 665 (2011) 90–93. doi:10.1016/j.nima.2011.10.060.

[95] A. Aguilar-Arevalo, et al, Measurement of the bulk radioactive contamination of detector-grade silicon with DAMIC at SNOLAB, Journal of Instrumentation 16 (06) (2021) P06019. doi:10.1088/1748-0221/16/06/p06019.

[96] A. Chavarria, et al, DAMIC at SNOLAB, Vol. 61, 2014. doi:10.1016/j.phpro.2014.12.006.

[97] A. Aguilar-Arevalo, et al, Characterization of the background spectrum in DAMIC at SNOLAB, Physical Review D 105 (6). doi:10.1103/physrevd.105.062003.

[98] P. Adari, et al, Excess workshop: Descriptions of rising low-energy spectra (2022). doi:10.48550/ARXIV.2202.05097.

[99] G. F. Moroni, et al, Low threshold acquisition controller for skipper charge coupled devices, in: 2019 Argentine Conference on Electronics (CAE), 2019, pp. 86–91. doi:10.1109/CAE.2019.8709274.

[100] K. Kobayashi, Identification of 210Pb and 210Po in the bulk of copper samples with a low-background alpha particle counter, AIP Conference Proceedings 1921 (1) (2018)

030002. arXiv:https://aip.scitation.org/doi/pdf/10.1063/1.5018989, doi:10.1063/1.5018989.

[101] F. T. Porter, Beta decay energy of tritium, Phys. Rev. 115 (1959) 450–453. doi:10.1103/PhysRev.115.450.

[102] R. Saldanha, et al, Cosmogenic activation of silicon, Phys. Rev. D 102 (2020) 102006. doi:10.1103/PhysRevD.102.102006.

[103] F. Piquemal, Modane underground laboratory: Status and project, Eur. Phys. J. Plus 127 (2012) 110. doi:10.1140/epjp/i2012-12110-3.

[104] N. Ramesh, et al, Flux variation of cosmic muonsdoi:10.48550/ARXIV.1203.0101.

[105] C. Berger, et al, Experimental study of muon bundles observed in the fréjus detector, Phys. Rev. D 40 (1989) 2163–2171. doi:10.1103/PhysRevD.40.2163.

[106] B. Schmidt, et al, Muon-induced background in the EDELWEISS dark matter search, Astroparticle Physics 44 (2013) 28–39. doi:10.1016/j.astropartphys.2013.01.014.

[107] C. Bebek, N. Roe, 4k x 2k and 4k x 4k CCD Users Manual Rev. 3b, (2011).
URL https://www.astronomy.ohio-state.edu/martini.10/osmos/LBNL4kxnkmanual.pdf

[108] N. Holland, Interfacing Between LVPECL, VML, CML, and LVDS Levels, SLLA120, Texas Instruments (2002).
URL https://www.ti.com/lit/an/slla120/slla120.pdf?ts=1651352708346

[109] SPI Block Guide V03.06, S12SPIV3/D, Motorola Inc. (2003).

[110] D. Kamath, Overview of opamp and ota based integrators, International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering (IJIREEICE) 3 (2015) 2321–2004. doi:10.17148/IJIREEICE.2015.3915.