Contribution to the development of sub-harmonic mixer above 200 GHz on silicon targeting high data rate applications

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Contribution au Développement de Mélangeur Sous-Harmonique au-delà de 200 GHz sur Silicium visant des Applications Haut-Débit

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Abstract

Nowadays, the number of connected electronic devices is facing an exponential growth which is driven by the never-ending demand of users for more mobility, resulting in an increase of global mobile data traffic. In this logic, the improvement of wireless connectivity is crucial to support the forecasted data rate required for emerging applications. Therefore, the IEEE 802.15.3d standard has defined a continuous frequency band between 252-321 GHz to support the future 6G technology, achieving high data rate transmission in a power-efficient way by using low-complexity modulations. Concerning the literature, above 200 GHz most receiver architectures are based on III-V Schottky diode Sub-Harmonic Mixers (SHMs), thanks to outstanding electrical performances. However, these solutions are pricy, going in contradiction with required mass-deployment of future 6G technology. Therefore, in this thesis we evaluate Silicon (Si) based BiCMOS and innovative packaging technologies to enable cost-effective Si-based Schottky diode SHM solutions at 268 GHz. Simulated diode conversion loss of ~11.7 dB and passive circuit losses of ~5.1 dB (low-resistivity Si substrate) have been achieved by following an innovative hybrid packaging solution with organic substrate and metallic split-block module, showing promising perspectives to enable cost-effective SHM alternatives. In a practical case, a real-time wireless links of 15 Gb/s using OOK modulation and 30 Gb/s using PAM-4 could be achieved with the proposed circuit.

Keywords: Schottky diode, Sub-harmonic mixer, Silicon technology, Organic substrate, Metallic split-block

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Résumé

Aujourd'hui, le nombre d'appareils électroniques connectés fait face à une croissance exponentielle motivé par la demande constante d'utilisateurs pour plus de mobilité, donnant lieu à une croissance du trafic de débit de données global. C'est pourquoi l'amélioration de la connectivité sans-fil est cruciale pour appuyer les débits de donnés nécessaires pour les applications émergentes. En conséquence, le standard IEEE 802.15.3d a fixé une bande continue entre 253-321 GHz pour supporter la future technologie 6G, en attendant des transmissions de débits de donnés élevés à faible consommation par l'utilisation de modulations peu complexes. Par rapport à l'état de l'art, les architectures de réception préférées au-delà de 200 GHz sont basées sur des mélangeurs sous-harmoniques (SHMs) à diode Schottky en technologie III-V grâce aux bonnes performances électriques. Cependant, ces solutions sont couteuses, en rendant difficile le déploiement massif requis pour la technologie 6G. En conséquence, dans cette thèse la technologie silicium et la mise en boitier associée est évaluée afin de proposer des SHMs à diode Schottky en technologie Silicium à 268 GHz. Des pertes de conversion de ~ 11.7 dB et pertes de circuit passif de ~5.1 dB (substrat silicium à faible résistivité) ont été achevés en simulation sur une mise en boitier hybride en utilisant du substrat organique intégré dans un module split-block métallique. Ces résultats donnent des bonnes perspectives pour proposer des alternatives peu couteuses aux SHMs conventionnels. Dans un cas pratique, une liaison sans fils de 15Gb/s utilisant modulation OOK et 30 Gb/s utilisant PAM-4 peuvent être atteints avec le circuit développé.

Mots clés : Diode Schottky, Mélangeur sous-harmonique, Technologie silicium, Substrat organique, Split-block métallique

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Glossary

µBGA: Micro Ball Grid Array
4G: Fourth Generation
5G: Fifth Generation
6G: Sixth Generation
ABF: Ajinomoto Build-up Film
AI: Artificial Intelligence
AiP: Antenna in Package
Al2O3: Alumina
AlN: Aluminum Nitride
APD: Antiparallel Diode
AR: Augmented Reality
ARI: Aerial-Radio Interface
ASIC: Application Specific Integrated Circuit
ASK: Amplitude-Shift Keying
AWGN: Additive White Gaussian Noise
B2B: Back-to-Back
BDTI: Buried Deep Trench Isolation
BEM&T: Back-End Manufacturing & Technology
BEOL: Back-End-of-Line
BER: Bit-Error-Rate
BGA: Ball Grid Array
BiCMOS: Bipolar Complementary Metal-Oxide-Semiconductor
BJ: Blinder Jetting
BSF: Band-Stop Filter
BT: Bismaleimide-Triazine
BW: Bandwidth
CCL: Copper Clad Laminate
CMOS: Complementary Metal-Oxide-Semiconductor
CMP: Chemical-Mechanical Polishing
CMR: Compact Microstrip Resonators
CNC: Computer Numerical Control
CPW: Coplanar Waveguide
CSP: Chip Scale Package
Cu: Copper
DC: Direct Current
DET: Detector
Df: Loss tangent
DFR: Dry Film Resist
Dk: Dielectric constant
DOE: Design of Experiment

DRIE: Deep Reactive Ion Etching
DSB: Double-Sideband
EDFA: Erbium Doped Fiber Amplifier
EHD: Extreme-High-Definition
EM: Electromagnetic Field
ENEPIG: Nickel Electroless Palladium Immersion Gold
ENIG: Electroless Nickel Immersion
EOM: Electro-Optic Modulator
EVM: Error Vector Magnitude
FEOL: Front-End-of-Line
FET: Field Effect Transistors
GC: Grating Coupler
GCPW: Grounded Coplanar Waveguide
GDM: Global Design Method
Ge: Germanium
GPS: Global Positioning System
HASL: Hot Air Solder Leveling
HBT: Heterojunction Bipolar Transistor
HEMT: High Electron-Mobility-Transistor
HFSS: High-Frequency Structure Simulator
HPF: High-Pass Filter
HR: High-Resistivity
HS-HGDM: Half-Global Design Method
I/O: Input/Output
I/Q: In-phase/Quadrature
IC: Integrated Circuit
IEEE: Institute of Electrical and Electronics Engineers
IEMN: Institut d'Electronique, de Microélectronique et de Nanotechnologie
IF: Intermediate Frequency
IL: Insertion Loss
InAlAs: Indium Aluminium Arsenide
InGaAs: Indium Gallium Arsenide
InP: Indium Phosphide
IoE: Internet-of-Everything
IoT: Internet-of-Things
IPD: Integrated Passive Devices
ITU: International Telecommunication Unit
JPL: Jet Propulsion Laboratory
LHA: Lensed-Horn Antenna
LNA: Low-Noise Amplifier
LO: Local Oscillator
Low-R: Low-Resistivity
LPF: Low-Pass Filter

LSA: Lensed-Horn Antenna
LSB: Lower-Sideband
LSM: Longitudinal Section Magnetic
LTCC: Low-Temperature Cofired Ceramic
MAC: Medium Access
MCM: Multi Chip Modules
mHEMT: Metamorphic High-Electron-Mobility Transistor
MIMO: Multiple-Input Multiple-Output
ML: Metal Level
MLS: Micro Laser Sintering
MMIC: Microwave Monolithic Integrated Circuit
MR: Mixed Reality
MTOP: Metal Top
N/A: Not Available/Not Apply
NDR: Nonradiative
NEP: Noise Equivalent Power
NF: Noise Figure
NSA: Non-Standalone
OOK: On-Off Keying
ORI: Ocean-Radio Interface
OSP: Organic Solderability Preservative
P2P: Point-to-Point
PA: Power Amplifier
PAM: Phase-Amplitude Modulation
PC: Personal Computer
PCB: Printed Circuit Board
PD: Photodiode
PE: Perfect Electric
PGA: Pin Grid Array
PHY: Physical
PIC: Photonic Integrated Circuit
PIN-PD: Positive Intrinsic Negative Photodiode
QAM: Quadrature-Amplitude Modulation
QPSK: Quadrature Phase-Shift Keying
R&D: Research and Development
RF: Radiofrequency
RoHS: Restriction of Hazardous Substances
Rx: Receiver
SA: Standalone
SC: Semiconductor/Short Circuit
SDM: Subdivision Design Method
SF6: Sulfur Hexafluoride
SHD: Super-High-Definition

SHM: Sub-Harmonic Mixer
Si: Silicon
SiGe: Germanium on Silicon
SINDR: Substrate Integrated Nonradiative
SiO2: Silicon Oxide
SiP: System in Package
SiPho: Silicon-Photonic
SIW: Substrate Integrated Waveguide
SLA: Stereo Lithography Apparatus
SLM: Selective Laser Melting
SMP: Subminiature version P
SMS: Suspended Microstrip
SNR: Signal-to-Noise Ratio
SoC: System on Chip
SOI: Silicon-on-Insulator
SOTA: State-of-the-Art
SRI: Satellite-Radio Interface
SSB: Single-Sideband
SSL: Suspended Stripline
SSLIN: Suspended Stripline (ADS notation)
STI: Shallow Trench Isolation
TBD: To be done
TIA: Transimpedance Amplifier
TSV: Through Substrate Vias
TV: Television
Tx: Transmitter
UHD: Ultra-High-Definition
USB: Upper-Sideband
UTC-PD: Unitraveling Carrier Photodiode
V2X: Vehicle-To-Everything
VATT: Variable Attenuator
VCO: Voltage-Controlled Oscillator
VR: Virtual Reality
WG: Waveguide
Wi-Fi: Wireless Fidelity
WiGig: Wireless Gigabit Alliance
WLAN: Wireless Local Access Network
WR: EIA Waveguide standard

General Introduction

Nowadays, the number of connected electronic devices is facing an exponential growth which is driven by the never-ending demand of users for more mobility, resulting in an increase of global mobile data traffic (+133.5% in 2023 with respect to 2022). In this logic, the improvement of the associated devices and wireless connectivity is crucial to support the forecasted data rate required by emerging applications. Therefore, 5G technology appears like an appealing solution, targeting peak data rates of 2 Gb/s and experienced data rate of 100 Mb/s. Going even further, the 6G technology for the next decade targets peak data rates of 1 Tb/s and experienced data rates up to 10 Gb/s for future applications which will require even higher amounts of data rates.

Current high data rate solutions focus on exploring the frequency bands in the upper part of already deployed 5G spectrum (E-band) to enable higher data dates leveraging available larger bandwidths. However, associated power consumption of digital processing when using high-complexity modulations to achieve such high data rates is a cause of concern. This challenge leads to explore even higher frequency bands (with larger bandwidth) to achieve targeted data rates in a power efficient manner by using low-complexity modulations, which will eliminate the necessity of power-consuming digital processing. In this trend, an interesting candidate is the 252-321 GHz continuous frequency band defined by the IEEE 802.15.3d standard, which is considered for future 6G technology. In this logic, broadband wireless links solutions operating above 200 GHz is today a key Research and Development (R&D) topic in the wireless communications community.

Exploring the recent wireless link solutions above 200 GHz we can notice that photonic Transmitter (Tx) solutions is a good candidate to support the targeted ~69 GHz band due to their inherent broadband operation. Concerning the Receiver (Rx) part, Mixer-first GaAs Schottky diode sub-harmonic receiver architecture is the favorite solution due to its good sensitivity and large bandwidth compared to other Rx architectures. However, GaAs Schottky diode Sub-Harmonic mixers (SHMs) are expensive since they rely on GaAs technology, and they are packaged on expensive metallic split-block modules. Another inconvenience is the lack of automated assembling process in the considered package since the GaAs circuit is wire-bonded and attached to the metallic module manually.

Fortunately, innovative Silicon Schottky diode solutions have been enabled in BiCMOS technology, achieving cutoff frequencies ~1 THz, paving the way for the proposition of cost-effective Silicon-based Sub-Harmonic Mixer (SHM) solutions at THz frequencies. Moreover, the potential of cost-effective packaging solutions using organic laminate substrates has been evaluated above 200 GHz, enabling improved assembling process of integrated circuit into metallic split-block modules. Therefore, the main question of this thesis is to determine if we can achieve high-performance and cost-effective SHM design operating in the 253-321 GHz

band using Silicon-based technology. To address this challenge, the work carried out in the thesis is presented using the following chapters organization:

The **first chapter** exposes the context of the thesis. Here, the problematic concerning the achievement of high data rates (~100 Gb/s) in a power-efficient manner is discussed. After, a special focus is given to Rx block solutions, being the main axis of improvement for wireless links above 200 GHz. Then, favorite Rx SHM in GaAs architecture is briefly presented, highlighting its advantages and drawbacks. Finally, our work is positioned in relation to the mentioned Rx solutions.

The **second chapter** explains what a SHM is, giving a special focus on the main element: the Schottky diode, which is placed in antiparallel configuration. After reviewing the physical principles of Schottky diode operation, we present the state-of-the-art of GaAs and Silicon Schottky diodes. Then, the previously developed Schottky diode in BiCMOS 55 nm technology is presented, highlighting the axis of improvement in terms of analytical modeling. Finally, an updated model is proposed leveraging previous diode measurements and preliminary W-band SHM design.

The **third chapter** illustrates the evolution of packaging for operating frequency above 200 GHz, focusing on cost-effective packaging solutions, such as organic laminate substrate, which is traditionally used for RF applications but have been used here beyond 200 GHz. Then, previous work concerning hybrid integration strategies (metallic split-blocks + organic substrate) is reviewed and new axis of improvement are identified. Finally, an innovative packaging integration strategy is proposed and deployed to design a WR3 Back-to-Back Waveguide-to-Suspended Stripline (WR3 B2B WG-to-SSL) transition in Silicon BiCMOS 55 nm and BiCMOS 130 nm technologies.

The **fourth chapter** presents SHMs state-of-the-art above 200 GHz and proposes a Rx receiver architecture to support the IEEE 802.15.3d overall frequency band. In this logic, the Schottky diode studied in the second chapter and the innovative packaging solution proposed in the third chapter are considered to develop a Schottky diode SHM operating at 268 GHz in 55 nm BiCMOS technology.

Finally, an overall conclusion of the developed work in this thesis is presented, leading to some perspectives at short and long term.

Chapter 1
6G High Data Rate Wireless Communications: Towards THz Links

1.1 Wireless Applications & Mobile Data Traffic

1.1.1 Evolution of connected devices

In today's rapidly evolving world, people are always looking for ways to simplify their day-to-day life. A convenient solution is the use of electronic devices aligned with the user requirements which are interconnected together to a common network (such as the internet) to share and update information in real-time. These devices have been introduced in a dynamic market, where the associated technologies are in constant evolution, proposing more and more innovative and performant devices that helps to manage our lives in a more efficient way in term of security (video security, smart homes, etc.), transportation (GPS, automated cars, etc.), health care (medical implants, smart watches, etc.) or communications and social comfort (smartphones, laptops, tablets). In this logic, each year the number of devices connected to the internet increases, as can be illustrated in Fig. 1. (study and projection made at end of 2023) [1].

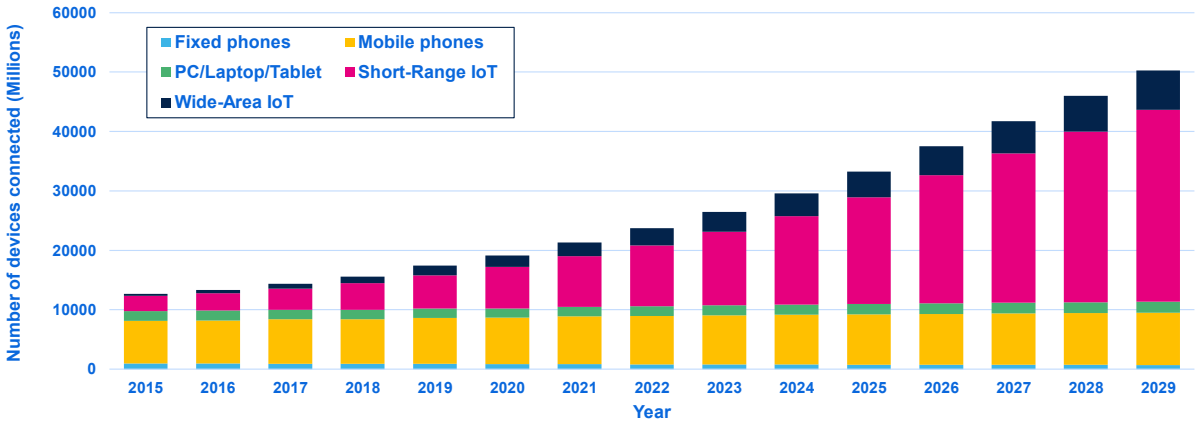


Fig. 1. Number of devices connected per year (with forecast after 2023). Adapted from [1].

From the previous figure we can notice that the increase of connected devices each year from 2015 to 2023 is mainly driven by the Internet-of-Things (IoT) market, following an exponential growth until achieve a forecasted total number of ~50 billion connected devices for 2029. This fact highlights that more and more devices are being used and interconnected together for a final interaction with the user, leading to a seamless and integrated ecosystem between humans and electronics devices.

1.1.2 Consequence on the mobile data traffic

However, the mentioned increase of the number of connected devices translates to an augmentation of global data traffic. Moreover, if we focus only on mobile data traffic (smartphones, mobile PCs, tablets, and routers) an increment of the global data traffic of 34.42 % is expected for the end of 2023 (130 Eb/month) [1] in comparison with 2022, despite the constant evolution in time of the number of connected mobile devices found in Fig. 1.

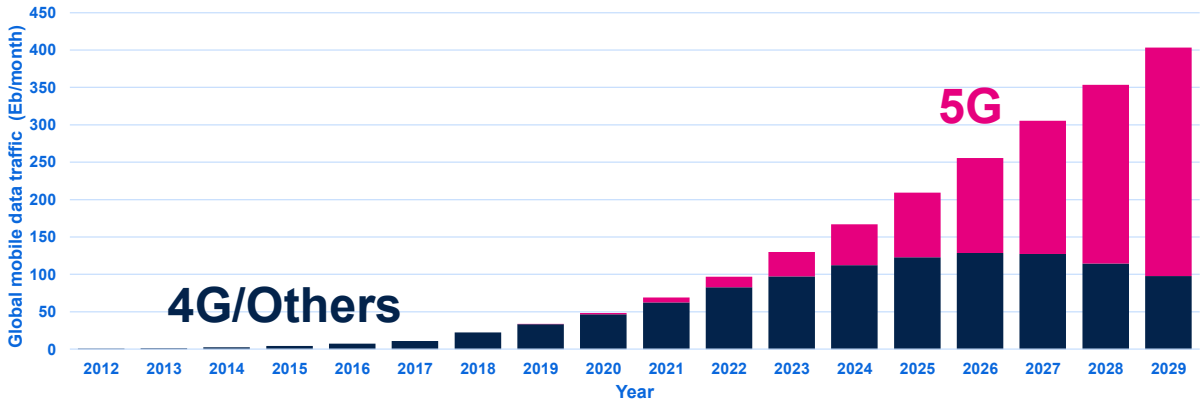


Fig. 2. Global mobile data traffic per year (including forecast after 2023). Adapted from [1].

In fact, observing the most recent Ericsson data report, a total global data traffic of 129.92 Eb/month has been achieved at November 2023 [1], demonstrating the accuracy of the forecast. Moreover, the last report shows that from all the data traffic of 2023, a 25,2 % is due to the devices using the fifth generation (5G) technology, which represents an increment of 133.5% in relation of 5G mobile traffic in 2022 (14.02 Eb/month) [1]. In long-term, an exponential increase of global mobile data traffic is expected until 2029, as illustrated in Fig. 2. For 2025, it is expected that half of the total data traffic will be related to the 5G connectivity, leaving behind their predecessors (4G technology and others) and continue to increase in long-term. In addition, the predicted traffic growth assumes that data-consuming applications such as Augmented Reality (AR), Virtual Reality (VR) and Mixed Reality (MR) will fully emerge at the end of the illustrated forecast, leading to an explosion of the global mobile data rate [1].

1.1.3 5G technology overview

In this logic, the improvement of devices and associated wireless network is a priority for the telecommunications operators to support the forecasted data rate growth required for the emerging communication technologies such as 5G. In fact, in terms of mobile devices, 5G technology is starting to be more and more present in our everyday life since first deployments of this technology in the end of 2019, especially in terms of the vast smartphone offers that already supports the technology. Some recent examples are the iPhone 15, the Samsung Galaxy S23, the Huawei Mate 40E and the Google pixel 8. In addition, this technology promise to improve the mobile device performances, especially in terms of data rates achieving 20 Gb/s under certain scenarios and 100 Mb/s for users in urban and sub-urban areas [2].

Like its predecessor (4G technology), 5G technology works at low-frequency bands (below 1 GHz) and medium frequency bands (between 1 – 6 GHz, also called the sub-6G band), which are mainly supported by the previous infrastructure of the 4G technology. This type of operation is called 5G non-standalone (NSA). However, to improve the data rate of devices compared to 4G in a power-efficient manner, larger frequency bands are explored. Therefore, frequency bands above 24 GHz and 37 GHz are used with expected frequency bands higher

than 57 GHz. The use of a unique infrastructure for 5G enables standalone (SA) operation. In fact, the use of specific 5G bands will enable high data rates especially for crowded areas. Concerning the mentioned bands, the state of spectrum allocation for different countries (in May 2023) is presented in Fig. 3.

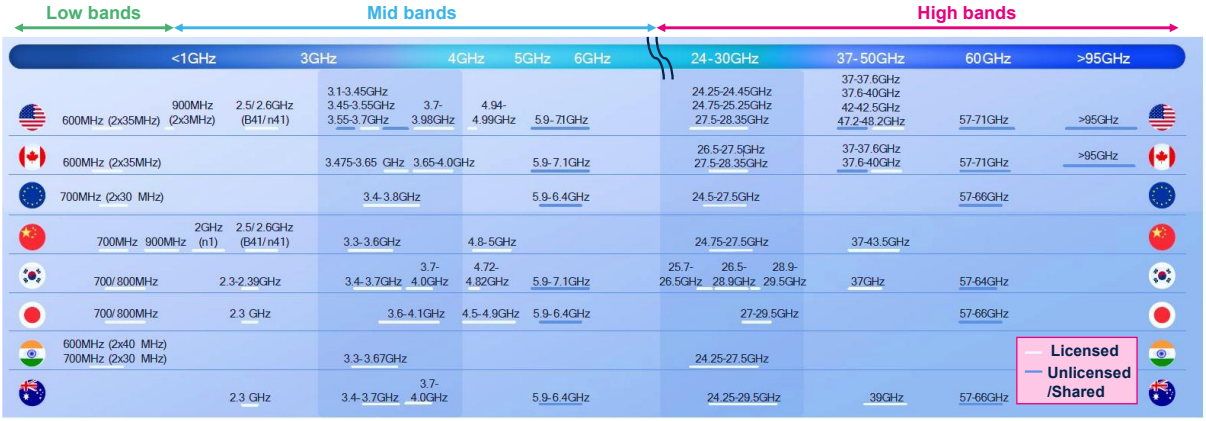


Fig. 3. Current state of spectrum allocation for 5G in different countries. Adapted from [3].

On the above figure we can notice that most world economic powers have already achieved the licensing of the 24-30 GHz band and part of the 37-50 GHz band for 5G purposes. Concerning the European Union, just the United Kingdom has achieved the license for using the 40.5-43.5 GHz band. In the case of France, the recent status is the approval of the 3.4-3.8 GHz band and test licenses are ongoing for the approval of the 26 GHz band.

Concerning the global 5G availability[1], the United States is leading the market with a 56% insertion according to data from Q4 2022 [4]. In the same report, it has also been highlighted that Cyprus (49.8%), Switzerland (46.1%) and Denmark (42.7%) leads in the European region in terms of 5G deployment/adoption. A main component for the adoption of 5G is the affordability of the 5G smartphones, in fact, in terms of sales, Europe sold 26.8 million 5G smartphones in 2022, equivalent to 67% from the total sales of Europe mobile phones, whereas in the United States and China, percentages of 84% and 87% are achieved respectively. Consequently, Europe still needs to catch up to remain aligned with the dynamic 5G market.

Although the strong effort that is given to massive deploys the 5G as well as the enablement of specific spectrum allocations, this technology will be limited in the next decade for specific applications which will require huge amount of data rates (higher than 100 Mb/s per user [2], like holographic images) and low-power consumption (like the Internet of Bio-Nano-Things). To reinforce this point, as illustrated in Fig. 3, most lower frequency bands are fractionated, limiting the enablement of large and continuous frequency bands for higher data rates in a power efficient manner. Consequently, higher frequency bands must be explored to pave the way for future sustainable wireless communications.

[1] *Availability* refers to what percent of users on 5G-capable devices spent most of their time on 5G [4].

Another recent inconvenience of 5G technology is the lack of real global coverage. In fact, 5G just covers 20% of total land and 5% of the ocean [5]. Finally, is the lack of "intelligence". In fact, thanks to the recent outcoming of Artificial Intelligence (AI), future devices can be incorporated with intelligent algorithms and machine learning to improve their performance. In conclusion, the complete 5G infrastructure that is recently in development must be further improved to enable the next generation of communications: the sixth-generation (6G) technology, expected to be deployed in 2030 timeframe.

1.1.4 Evolution towards 6G technology

6G technology is still in the early stage of exploration. In terms of standardization, the International Telecommunication Union (ITU) has already released the 6G schedule in February 2020, expecting that the research on the vision and technical propositions of 6G are likely to be completed by 2023. In this idea, European projects such as the 6GStart [6] in 2022 and the TERA6G (TERAhertz integrated systems enabling 6G Terabit-per-second ultra-massive MIMO wireless networks) [7] in 2023 have been initiated to support the research on the 6G technology development in Europe.

Despite the 5G technology which is more IoT-oriented, 6G vision (in a holistic point of view) is enclosed into a philosophy of global massive connectivity and interaction between humans and devices, enabling the Internet of Everything (IoE). To achieve this vision, unlimited full wireless global connectivity is targeted, going from space to the ocean. To achieve full connectivity, 6G technology expects to integrate all functions such as communications, radar, sensing, computing, navigation, and imaging to support full-vertical applications. Moreover, thanks to the evolution of machine learning and AI, 6G will be an autonomous system, evolving from a human-centric ecosystem into a both human and machine environment [8].

Characteristic	**4G**	**5G**	**6G**
Service objects	People	Connection (people and Things)	Interaction (People and World)
Applications	• High-Definition Videos • Voice • Mobile TV • Mobile Internet • Mobile Pay	• VR/AR/360° Videos • UHD (4K) Videos • V2X • IoT • Smart City/Factory/Home • Telemedicine • Wearable Devices	• Holographic Verticals and Society • Tactile/Haptic Internet • Full-Sensory Digital Sensing and Reality • Fully Automated Driving • SHD (8K), EHD (16K) video • Space Travel • Deep-Sea Sightseeing • Internet of Bio-Nano-Things

Table 1. Supported (recent and expected) applications for 4G, 5G and 6G. Taken from [8].

The usage scenarios of 4G and 5G, as well as expected applications of 6G are illustrated in Table 1. As mentioned before, the main differential aspect of 6G technology compared to 5G

is the IoE, which will enable holographic experiences and high-precision communications for *Haptic*[2] internet applications, leading to a full-immersive and sensorial experience while entering in contact with the internet. Evermore, 6G also targets to support Super-High-Definition (SHD) and Extreme-High-Definition (EHD) videos, which will also help to improve the user experience into the haptic internet. Concerning the connectivity of devices, the global connectivity will be improved by including ocean and spatial networks, by one side by supporting oceanic networks and by the other side by including the recent deployment of low earth orbit satellite constellation (including non-terrestrial network in current cellular infrastructure on ground). Finally, to go even further in device connectivity, the concept of Internet of Nano-Things will be introduced using smart wearable devices and intrabody implants with extremely low-power consumption [8].

Characteristic	4G	5G	6G
Peak Data rate	100 Mb/s	20 Gb/s	$\geq$ 1 Tb/s
Experienced data rate	10 Mb/s	100 Mb/s	1 Gb/s
Latency	10 ms	1 ms	0.1 – 0.01 ms
Connectivity density	10^5 Devices/Km²	10^6 Devices/Km²	10^7 Devices/Km²
Energy efficiency	1 ×	$10 - 100 \times$ that of 4G	$10 - 100 \times$ that of 5G
Spectrum efficiency	1 ×	3 × that of 4G	$5 - 10 \times$ that of 5G

Table 2. Technical characteristics (recent and expected) for 4G, 5G and 6G. Taken from [8].

Although the future of 6G applications seems promising, this will require to improve most of the technical technology aspects in comparison to the already deployed 5G technology. Some of these points are illustrated in Table 2. To support most applications, extreme high data rates are required, going from experienced data rates (in terms of individual user) of 1 Gb/s (10 Gb/s in indoor hotspots) and maximal peak data rates of 10 Tb/s for specialized applications such as fronthaul/backhaul communications [8], [9]. Moreover, for applications where low-latency is required (such as the industrial internet [10]), 6G targets a latency $100 \times$ lower than 5G. In the target to interconnect the major quantity of devices possible and support coverage in high-density areas, 6G technology targets to increase by ten times (compared to 5G) the connectivity density, going from 10^6 Devices/Km² to 10^7 Devices/Km². Finally, concerning efficiency in terms of power and spectrum, 6G aims to improve to support applications where high data rates and low-power consumption are required [8].

[2] *Haptic* relates to the perception and manipulation of objects using the senses of touch.

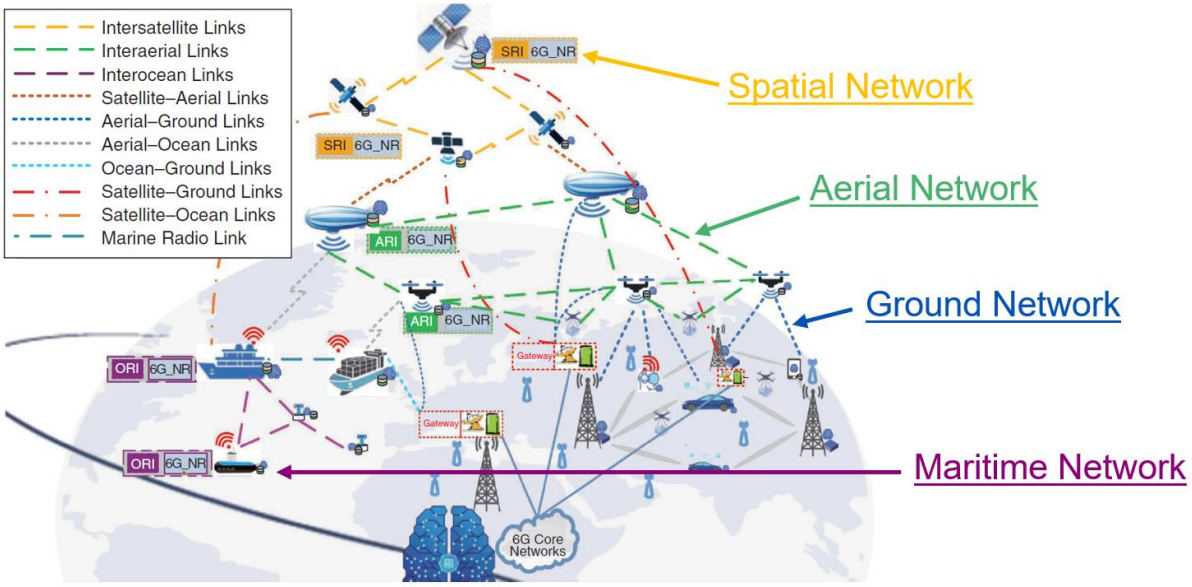


Fig. 4. The expected 6G network. SRI: Satellite-Radio Interface, ARI: Aerial-Radio Interface, ORI, Ocean-Radio Interface. Adapted from [8].

If we explore the recent capabilities of the global network, we can notice that it is far from being aligned with the network requirements of 6G, specifically in terms of coverage. To reinforce this point, we illustrate in Fig. 4 the targeted 6G network capabilities. We can notice that spatial, aerial, ground, and maritime network tiers co-exist and interconnect one into-another mainly by wireless links. To help to manage and improve the performance of the network, the network is expected to be autonomous, taking advantage of the innovations of the AI.

As noticed, such large network will need to deal with extreme data rates, especially for transfer of information between the central information cores. That is why the deployment of THz ultra-high-capacity front/backhaul communications is starting to being promoted as an attractive solution to support future 6G communications [8]. Following this idea, we propose firstly to review the recent state-of-the-art of different mmW transceivers (aligned with 5G technology) to define demonstrated data rate and open a discussion concerning associated power efficiency and the implication it may have from system point of view.

1.2 Power Efficient & High Data Rate mmW Wireless Links State-of-the-Art

1.2.1 State-of-the-art of wireless links in lower part of mmW domain & real-time communications problematic

To increase the carrier frequency and improve data rates to support 5G and incoming 6G, the lower part of the mmW band, more specifically, the E-band (60 – 90 GHz) has been explored. Around 60 GHz, different real-time wireless links have been demonstrated and commercially used to support indoor WLAN links based on the WiGig standard [11], [12], [13]. In [11] for example, a data rate of 5.4 Gb/s is achieved with 16QAM modulation using an IF-based transceiver. Evermore, in [12], data rates of 11 Gb/s are achieved using 16QAM modulation by direct conversion to reduce power consumption. However, it must be considered that despite the effort to reduce Rx power consumption from the analogic part, the digital signal processing also plays an important role in the total power consumption, especially if high data rates are targeted because of the signal processing involved in the demodulation, as well as required high-speed serial digital interface. That is why in [13] the power consumption of commercial commodity devices operating at 60 GHz is evaluated, showing that the power consumption is a cause of concern (2.3 W for WiGig compared to 287 mW in Wi-Fi 802.11.ac) due to the initial digital processing necessary to support the targeted high data rates.

In consequence, the wireless links demonstrators found in the literature struggles to present real-time high data rate solutions due to the complexity of implementation of required digital modems which also translates in higher power consumption. If we go higher in frequency, we can notice that real-time high data rate wireless links demonstrators use low/moderate complexity modulations. As illustration, in [14] at a frequency of 83 GHz, a data rate of 16 Gb/s are achieved using QPSK modulations. If we go even higher in frequency, for example the D band (110 – 170 GHz) we can notice the same trend. For instance, in [15] at a frequency of 120 GHz, a data rate of 22.2 Gb/s is achieved using 2ASK.

When higher high data rates are reported in literature, the demodulation and Bit-Error-Rate (BER) computation are generally performed offline, i.e. by storing the received analogic information and then processing it for further decoding. We can see that with these approach we can achieve at 75 GHz data rates of 40 Gb/s using PAM-4 modulation [16] and at 120 GHz data rates of 60 Gb/s using 64QAM modulations [17]. Above 200 GHz even higher data rates have been reported using offline post-processing, going up to 100 Gb/s, as will be illustrated in section 1.3. However, offline operation remains just as a laboratory demonstration. Therefore, keeping in mind that the overall system complexity and power consumption has to consider real-time constraints, high data rate wireless system definition must consider this problematic and not just focus on the power consumption of the analog wireless frond-end. In fact, this point could severely limit achievable data rates as illustrated in Fig. 5.

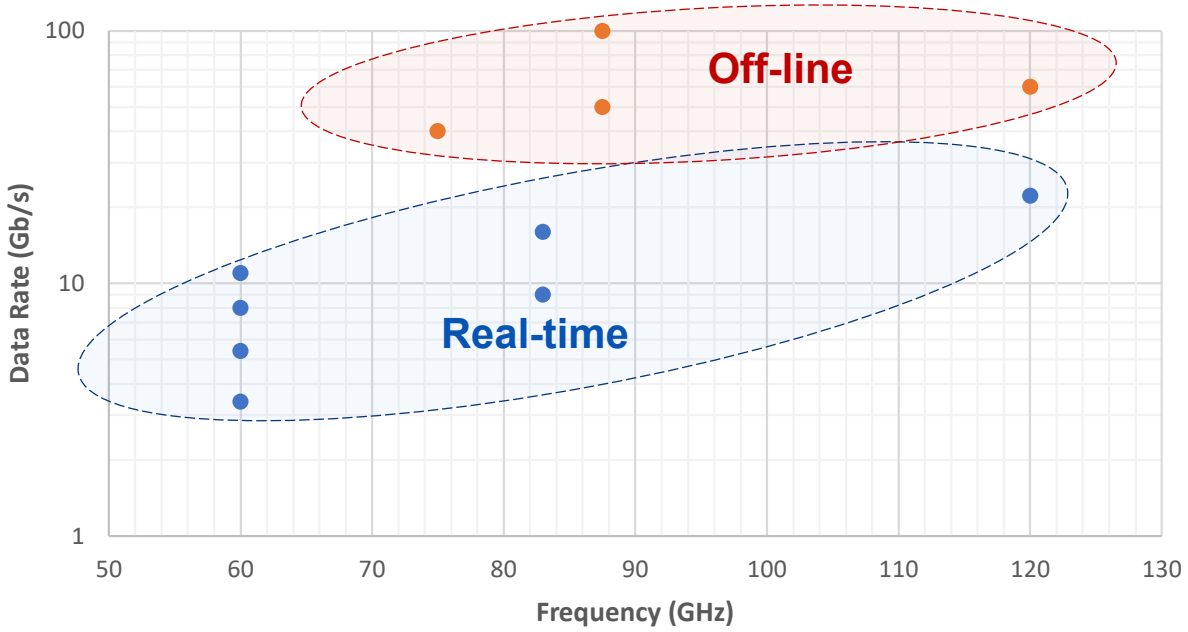


Fig. 5. State-of-the-art of in the lower part of the mmW domain illustrating real-time [11], [12], [14], [15] and off-line [16], [17], [18] wireless links.

A good strategy is to consider the point mentioned in [11], where low-complexity modulations limit the challenge to the RF front-end design. Moreover, since large bandwidth is available at higher operation frequencies (> 200 GHz), the use of low-complexity modulations to reduce as much as possible the total wireless system power consumption seems like a natural evolution (even if it is counter intuitive for most RF engineers since high modulation complexity and limited frequency have been historically used to guarantee high quality of services). In this logic, low-complexity modulations such as OOK can be used thanks to simple digital manipulation since the information is modulated purely by amplitude, added that no carrier frequency generation is required when incoherent detection is made. For example, high data rates (48 Gb/s) have been achieved using OOK modulation in real-time using a simple pair of transceivers operating at a carrier frequency of 300 GHz [19].

1.2.2 THz opportunities: The IEEE 802.15.3d standard, 220-325 GHz band normalization

As mentioned previously, to achieve the desired low-power consumption, low-complexity modulations must be used, which translates into a simpler signal processing circuitry. However, this means that a larger bandwidth is required to achieve the targeted high data rate. To illustrate this point, one can refers to Shannon's capacity theorem, expressed as

$$C = B\log_2\left(1+\frac{S}{N}\right) = B\log_2\left(1+\frac{E_b}{N_0}\times\frac{R}{B}\right) \qquad \text{Equation 1}$$

Where C is the channel capacity (bits/s), B is the channel bandwidth (Hz), and S/N is the signal-to-noise ratio SNR (W/W). Further, the SNR can be expressed in terms of the Energy-per-bit in the signal E_b, the noise power spectral density N_0 (W/Hz), the signal data rate R (bits/s) and the associated bandwidth B. The E_b/N_0 ratio is called the *SNR-per-bit* and the

ratio R/B is called the *spectral efficiency* in bits/s/Hz, and they are parameters given by the used modulation scheme. In conclusion, this equation express the theoretical maximal data rate for a given bandwidth and SNR in additive white gaussian noise (AWGN) channel.

In the case of low-complexity modulations such as OOK, a low SNR-per-bit value (for a typical comparative bit error rate (BER) of 10^{-5}) is expected (~12 dB) compared to other high-complexity modulations such as 64 QAM (~18.5 dB). This translates in lower energy required for modulation (in the analogic part) compared to more complex modulation strategies such as QAM. However, OOK modulation is not performant in terms of spectral efficiency R/B (1 bit/s/Hz) compared to 64 QAM (6 bits/s/Hz). In consequence, for a targeted data rate, OOK modulation will require a larger bandwidth compared to high-complexity modulations to accommodate the desired signals.

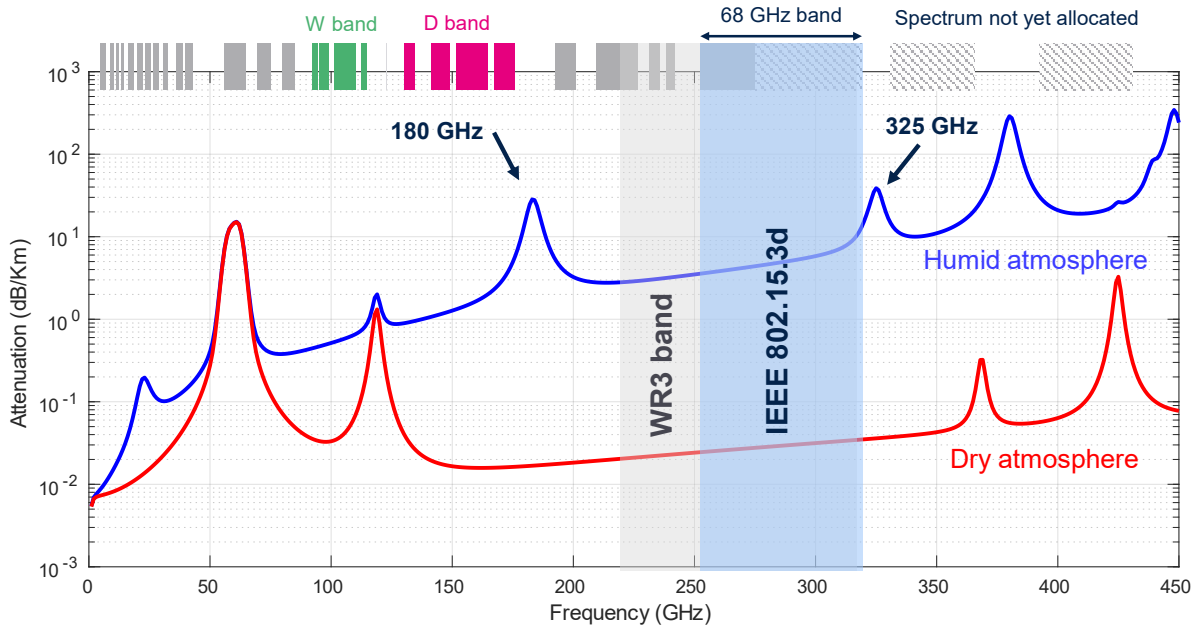


Fig. 6. Atmospheric attenuation under different weather conditions and IEEE 802.15.3d band. Adapted from [20].

Therefore, the electromagnetic spectrum must be explored to find propitious and continuous frequency bands to enable signal transmission via low-complexity modulations. However, the wireless link quality depends on the physical channel characteristics where the information is transmitted, thus the earth atmosphere attenuation. In this order, spectral windows must be identified to reduce the effect of transmission path in the associated wireless link. In Fig. 6, the atmospheric attenuation (temperature of 15° and atmospheric pressure of 101.3 kPa) in dry (water vapor density of 0 g/m³) and humid (water vapor density of 7.5 g/m³) atmospheres is calculated using the ITU atmospheric gas attenuation model [21].

We can notice that some spectral windows are already been used for wireless communications purposes such as the W and D frequency bands. Moreover, one can observe a large window between two absorption peaks placed at 183 GHz and 325 GHz respectively. Therefore, this band seems like an interesting option to enable large and continuous

bandwidth to support low-complexity modulation schemes. In addition, the WR3[34] frequency band (220-320 GHz) is enclosed and illustrated in this spectral window since it will be further mentioned in the following thesis chapters. For this reason, the mentioned spectral window is attracting the attention of the research and development community.

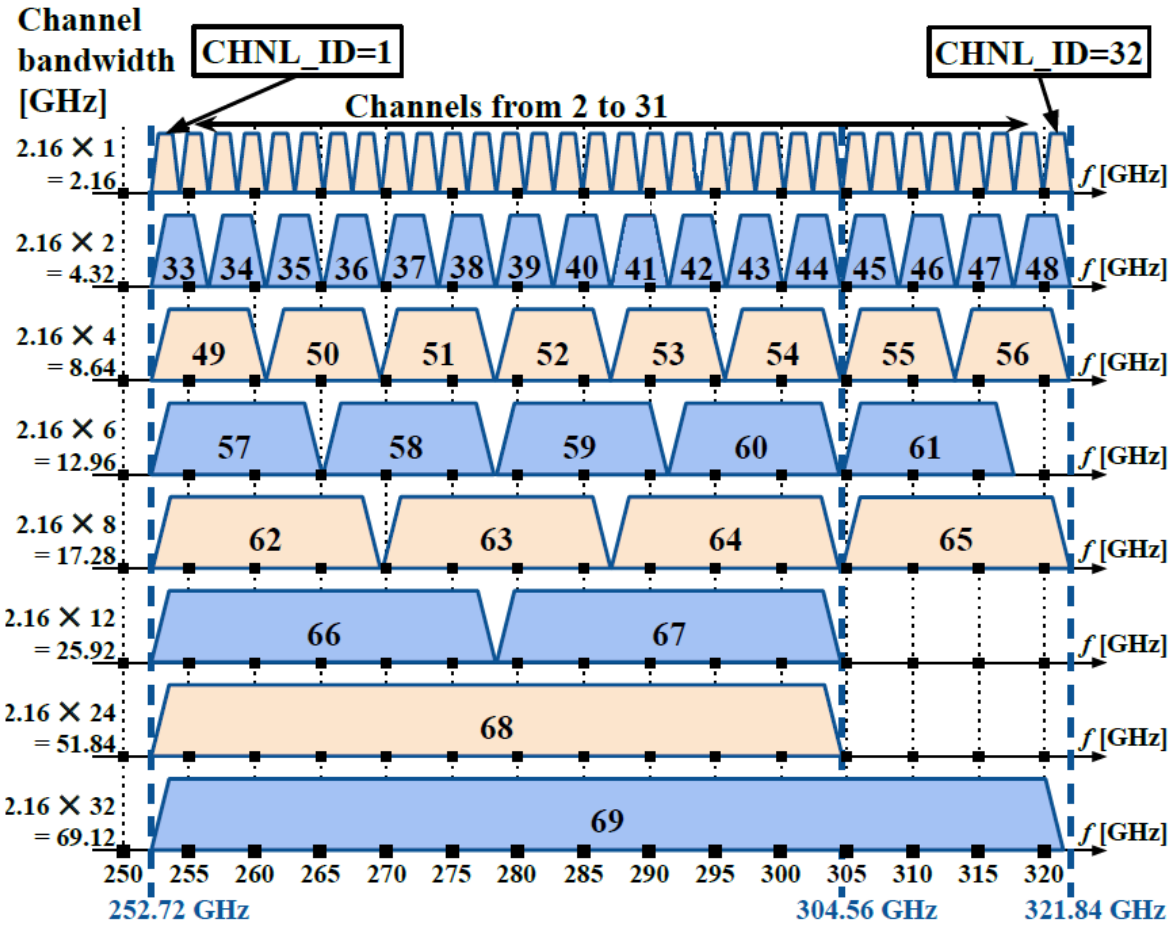


Fig. 7. Channel definition for the IEEE.802.15.3d standard. Taken from [22].

To reinforce this point, in a first effort of frequency band standardization, in 2017 the IEEE 802.15.3d standard has been presented to enable the standardization of Physical (PHY) and Medium Access (MAC) layers for consumer wireless communications in the sub-THz frequency band [22]. This set of rules targets high data rates up to 100 Gbps in short distance range by either using different channel division or a unique channel of 69.12 GHz between 252.72 and 321.84 GHz, as illustrated in Fig. **7**. Moreover, the IEEE.802.15.3d standard mainly targets the connection between two devices, i.e., point-to-point (P2P) communications, to support applications such as wireless fronthaul and backhaul links which are presented as a complement of optical fiber connections when challenging installation

[3] The WR3 frequency band (220-320 GHz) is defined by the monomodal recommended operation frequency of WR3 waveguides.

[4] As well as the WR3 frequency band, the H-band will be mentioned in the overall thesis, which has a very similar frequency range (220-325 GHz) band. In fact, waveguide frequency range is mentioned mainly in the literature for waveguide transitions whereas the H-band is mainly mentioned in SHM literature.

setups are required [23]. Therefore, the research community has been motivated to propose either electronics or optics wireless links solutions above 200 GHz.

1.3 Typical Architecture & Link Budget in the Upper Part of mmW Domain

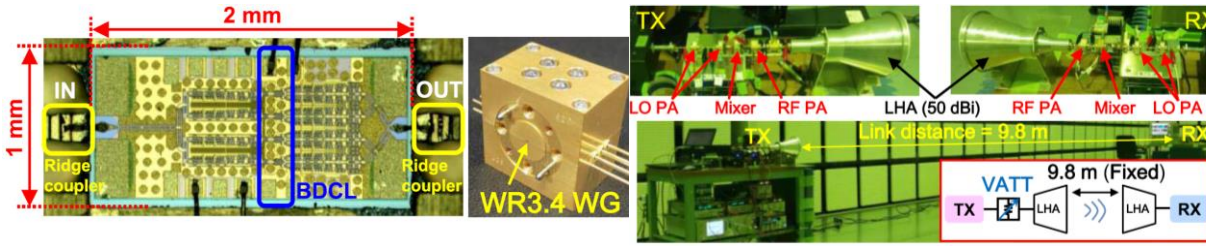
1.3.1 Tx above 200 GHz

1.3.1.1 All-electronics Tx above 200 GHz

A large part of reported Tx/Rx architectures at frequencies above 200 GHz are supported by III-V technologies due to their intrinsic improved semiconductor properties compared to Silicon-based technologies, especially in terms of higher electron mobility. As example, Indium Gallium Arsenide (InGaAs) semiconductor achieves an electron mobility of $8000\ \mathrm{cm^2(V.s)^{-1}}$ in contrast of Silicon with a constant of $1500\ \mathrm{cm^2(V.s)^{-1}}$ [24]. This allows the design of devices for high-frequency applications. In this logic, the Fraunhofer Institute of Applied Physics has developed a Microwave Monolithic Integrated Circuit (MMIC) technology based on 35 nm InGaAs Metamorphic High-Electronic-Mobility (mHEMT) transistors [25].

The introduction of this technology has led to the creation of multiple MMICs targeting wireless links at a carrier frequency of 240 GHz, which have enabled wireless link up to distances of 40 meters using 8PSK modulation achieving data rates of 30 Gb/s (EVM = 16%) [26] and 96 Gb/s (EVM = 21.6%) [27] respectively. Both solutions use in Tx a three-stage LNA design preceded by a quadrature resistive SHM using a transistor. These first demonstrators have paved the way for the enablement of long-range wireless links in III-V technology at a carrier frequency of 300 GHz. Firstly, in [28] a long-range wireless link has been demonstrated by using a parabolic antenna, achieving a distance of 850 meters and a data rate of 64 Gb/s using QPSK modulation. Evermore, in [29], a distance of 1 Km has been achieved, enabling a data rate of 76 Gb/s using 16-QAM modulation in offline mode. For more detail, the Tx module based on cascaded LNAs [30] is illustrated in chapter 3 in the Fig. 56 as a packaging example.

On the other side, different wireless links using MMIC achieved in 80 nm InP HEMT technology have been demonstrated at a carrier frequency of 300 GHz. In [31], a data rate of 100 Gb/s have been achieved at a distance of 2.2 meters. Moreover, with the same technology, even higher data rates and larger distance have been achieved in [32]. More details of the Tx module and the measurement setup are given in the Fig. 8.

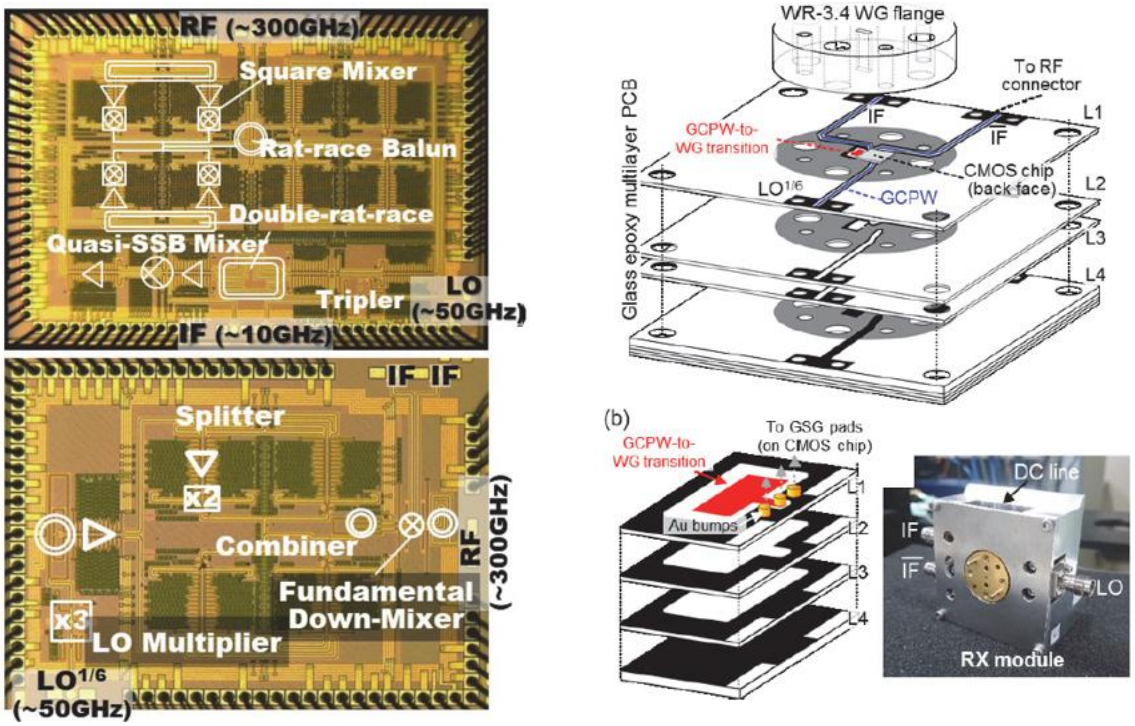


(a) (b)

Fig. 8. (a) Photograph of a 300 GHz PA in InP HEMT technology and the associated integration in split-block metallic module. (b) Complete Tx/Rx setup for wireless link. Taken from [32].

To perform the RF signal amplification, multiple PAs stages are necessary to provide enough power for transmission. Moreover, one can notice from Fig. 8 (a) that in the overall InP substrate (50 µm thickness), multiple Through Substrate Vias (TSV) have been placed to avoid substrate mode excitation [32]. Moreover, the complete amplification stage is packaged in a metallic split-block module. The same integration strategy is applied for each block that takes apart into the Tx. These points will be further discussed in chapter 3 where the packaging of III-V-based high-frequency circuits is explored. Concerning the wireless link setup, (Fig. 8 (b)), both Tx and Rx are separated from 9.8 m apart. Also, Lensed-Horn Antennas (LHA) with a 50 dBi gain and a Variable Attenuator (VATT) after Tx are included. This setup achieved at 300 GHz a data rate of 120 Gb/s with a 16QAM signal (in offline mode) [32].

In addition, other technologies based on Silicon have also been explored to support Tx and Rx circuits above 200 GHz. In fact, Silicon technologies compared to III-V based are less expensive to manufacture and provides higher-lever of functionalities integration, specially concerning digital control and biasing circuits. In this logic, Silicon technologies such as CMOS, which are traditionally used for digital processing and memories, have been studied as a potential candidate for high-frequency wireless links. Therefore, in [33] a 300 GHz CMOS solution using separated Tx and Rx chips is presented, targeting operation in the IEEE 802.15.3d frequency band. However, since the unity-gain power frequency f_{max} is below 300 GHz for the mentioned technology, ($f_{max} = 280$ GHz precisely [33]), it means that PA and LNA cannot be designed. Therefore, mixer-last (in Tx) and mixer-first (in Rx) architectures seems to be an alternative to operate at those frequencies. More precisely, in transmission, gate-pumped mixers are used. The mentioned ICs fabricated on 40 nm CMOS technology are illustrated in Fig. 9 (a).



(a) (b)

Fig. 9. (a) A 300 GHz Tx (top) and Rx (bottom) ICs in 40 nm CMOS technology. (b) Rx associated integration in split-block metallic module using H-plane probes. Taken from [33].

To provide the proper interconnections for RF, LO and IF signals, the ICs are flip-chip mounted on a Glass-Epoxy multilayer PCB. For the RF signal, a Grounded Coplanar Waveguide (GCPW) to waveguide transition is made at PCB level to further route the signal via a Computer Numerical Control (CNC)-machined waveguide which is adapted to the metallic module that encloses both IC and PCB. This solution enabled a wireless link at 300 GHz with a data rate of 20 Gb/s using a 16QAM modulation achieving a link distance of 10 cm (EVM = 12.2 %).

Furthermore, in [34] it is proposed to integrate both Tx and Rx functionalities in the same IC. This led at 300 GHz to a wireless link of 3 cm with a data rate of 80 Gb/s with a 16QAM modulation. However, both presented solutions faced has been demonstrated for very short-range communications. In this logic, in [35] Cassegrain antennas are used (Antenna Gain = 40 dBi @ 300 GHz) to enhance the distance up to 1 meter. In this configuration, a data rate of 36 Gb/s with QPSK modulation is achieved at 300 GHz. Having in mind the limitations in CMOS technology in terms of emitted power due to mixer-last architectures (Psat = -1.6 dBm @ 265.68 GHz [34]), one can take advantage of BiCMOS technology which compared to CMOS provides a higher f_T/f_{max} of 300/500 GHz, enabling the realization of PAs for the targeted frequencies. In this logic, different solutions have been presented in BiCMOS following the conventional PA-last architecture in Tx [36], [37], [38], [39] around 240 GHz (Psat = 7 dBm @ 240 GHz [39]).

More in detail, in 130 nm BiCMOS technology, a wireless link of 100 Gb/s at a distance of 0.8 meters [37] and 0.6 meters [39] have been achieved respectively using 16QAM modulation at 240 GHz. The Tx and Rx ICs from [39] are illustrated in Fig. 10 (a). In Tx, as

mentioned before, an actual PA is used. However, in contrast to CMOS, the integration strategy to allow emission and reception is quite different. In [36], [37] a double folded dipole antenna is integrated followed by polyethylene lens. By the other hand, in [38], [39] on-chip slot antenna are used followed by Silicon lens, as illustrated in the example from Fig. 10 (b).

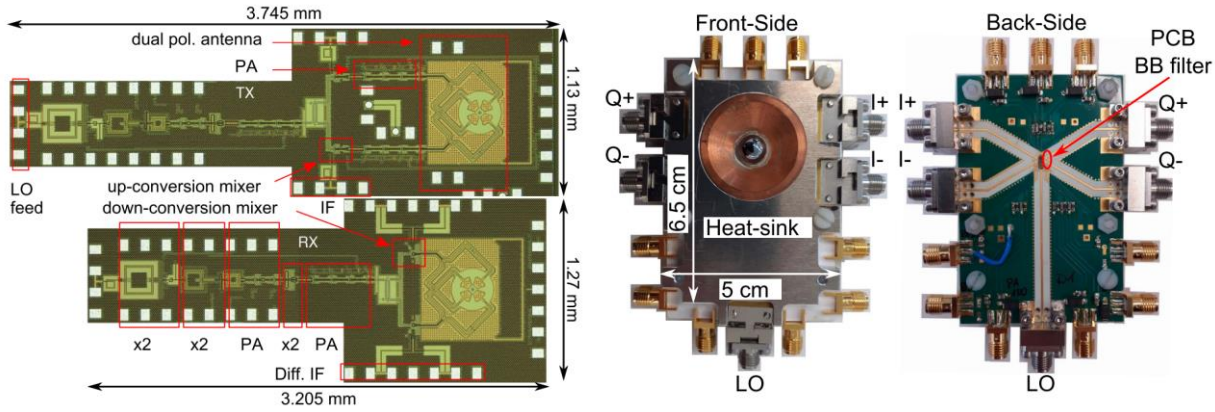


Fig. 10. A 215-240 GHz Tx (top) and Rx (bottom) ICs in 130 nm SiGe BiCMOS technology. (b) Rx integration in a PCB with Silicon lens. Taken from [39].

1.3.1.2 All photonics Tx above 200 GHz

Despite the high-integrability potential of electronics-based solutions used in wireless links, they still face limitations in terms of achievable bandwidth and power consumption, going in contradiction with the required large bandwidth (> 50 GHz) for more energy-efficient wireless communications above 200 GHz. Therefore, photonics technology is an appealing alternative when targeting wideband wireless communication thanks to their inherent broadband nature. Photonics can be divided into two groups: Wired (optical fiber communications) and wireless photonics. Traditionally, optical fiber communications is widely used since very long-distance physical links can be achieved. However, as highlighted in section 1.2.4, wired-fiber links faces high costs when difficult installation setups are required [23]. In consequence, wireless and low-cost photonic solutions are being under investigation to enable short range and high data rate communications [40].

The main component used to enable wireless photonics transmission is the photomixer. Unlike solid-state electronics where two signals with frequencies below the emitted RF signal frequency f_{RF} are mixed to generate the required RF signal (up-conversion), in photonics domain two optics signals with frequencies much higher than RF frequency f_{RF} are used (but exactly separated by targeted f_{RF} frequency), leading to a down-conversion to the desired RF signal. The mechanism of RF signal generation in a photomixer is illustrated in Fig. 11.

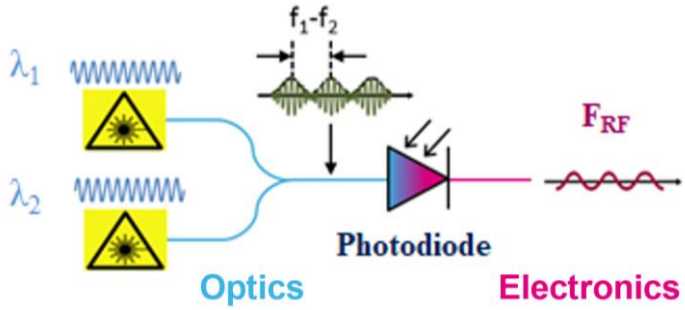


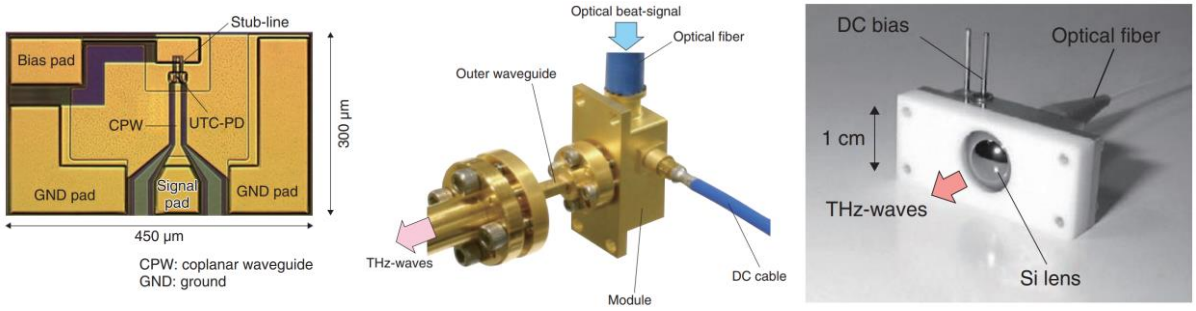
Fig. 11. RF generation by photomixing. Adapted from [41].

Basically, two slightly-separated (in frequency) optical signals with wavelengths λ_1 and λ_2 are injected to a photodiode which then down-convert to the RF signals. The frequency and wavelength relation is expressed in the following equation:

$$f_{RF} = f_1 - f_2 = \frac{C(\lambda_1 - \lambda_2)}{\lambda_1 \lambda_2} \qquad \text{Equation 2}$$

Where C is the speed of light (3×10^8 m/s). The RF signal is generated thanks to the mechanism of optical-to-electrical conversion in the photodiode. Here, electrons are generated by the photon's absorption. In terms of technologies that are being used for the integration of photomixers, two main families can be found: The III-V and IV-IV technologies. For the creation of photomixers in III-V technology, usually Indium Gallium Arsenide (InGaAs) on InP is used, whereas in IV-IV technology they are based on SiGe. The main characteristic that makes III-V materials suitable for optical applications is the fact that they have a direct bandgap in contrast with Silicon and Germanium, thus increasing their quantum efficiency (or photon-absorption efficiency) [24]. Although the mentioned inconvenient, Silicon-on-Insulator (SOI) based technologies enables the integration of optical waveguides with better confinement compared to III-V technology, thus allowing high-level of integration and cost-effective integrated solutions [40].

The two main devices used as photomixers are the Positive Intrinsic Negative (PIN) Diode and the Unitraveling Carrier Photodiode (UTC-PD). The first one is an interesting solution since it is a conventional alternative in terms of semiconductor junctions (less fabrication steps compared to UTC-PD). However, this is translated in lower photomixer performances. In fact, PIN diode optical-to-electrical conversion resides in the fact that the photon absorption and electrons/holes separation happen in the same intrinsic region, thus restraining the photodiode speed (response dominated by electrons and holes current). By adding an additional P-type neutral absorber (as in UTC-PD), photon absorption and electron drift mechanism are physically separated, thus the diode response is only dominated by the electron's velocity. This translates in larger saturation currents and larger bandwidths compared to a PIN diode [40], but under certain frequencies. To have a more precise vision, recent comparative studies between both III-V photomixers in a larger frequency band have shown that commercial III-V PIN-PDs are comparable to UTC-PD in terms of saturation currents under certain frequency ranges [42].



(a) (b) (c)

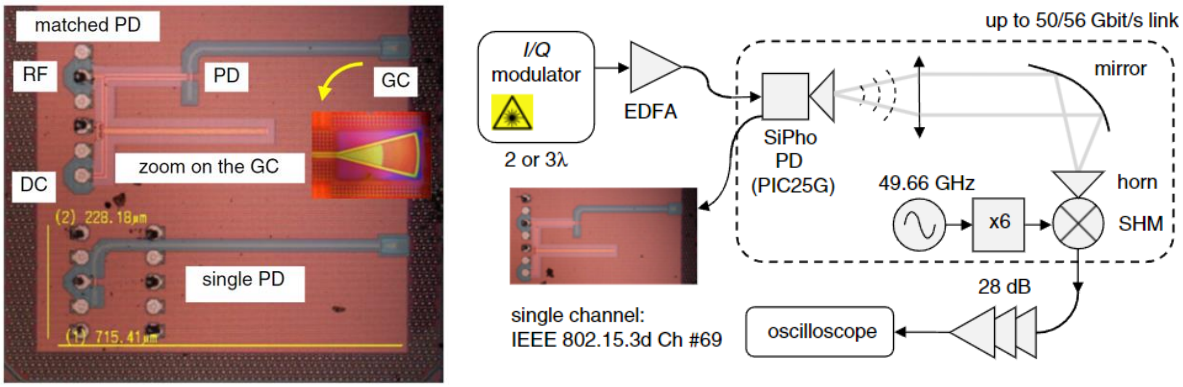
Fig. 12. Different commercials UTC-PD photomixers developed by NTT laboratories. (a) The UTC-PD, (b) Waveguide-Couple photomixer module and (c) Antenna-integrated photomixer module. Taken from [43], [44].

In Fig. 12 (b), (c), different packaged UTC-PD commercial solutions developed in 2012 [43] and 2005 [44] are illustrated. The IC integrating the photodiode and fabricated in III-V technology is presented in Fig. 12. (a). These packaged solutions have been developed to facilitate the interconnection of the proposed photomixer with the test equipment. For the first packaged solution, the output RF/THz signal is adapted to being interconnected with different waveguides. This solution has been evaluated in the THz band in 2012 providing an output power of 0.5mW (-3 dBm) at 350 GHz and a -10 dB bandwidth of 260 GHz [43]. The second package solution provides free-space radiation using a log-periodic antenna which is then coupled to a Silicon lens to improve directivity. This second solution has been evaluated at 1.04 THz, leading to an output power of 2.3 µW [44]. Despite more recent solutions that can be found in the literature, no solution above 200 GHz outperforms the output power which has been previously illustrated [45].

If we explore the literature, different photomixer solutions used as transmission element to support wireless links above 200 GHz can be found based on III-V UTC-PDs [46], [47], [48], [49] and III-V PIN diodes [50], [51]. In [48], a wireless link of 0.5 m has been enabled at 425 GHz, achieving a data rate of 106 Gb/s with 16-QAM modulation. At lower carrier frequencies, in [47] a 300 GHz wireless link of 100 m has been achieved with a data rate of 70 Gb/s using QPSK modulation. Also, In [46] a solution around the same carrier frequency has been presented supporting the IEEE.802.15.3d band, arriving to 100 Gb/s data rate using 16-QAM modulation at a distance of 0.5 m. Concerning III-V PIN-PD detectors, in [51] also at 300 GHz at a distance of 0.5 m, a 100 Gb/s wireless link in 16 QAM modulation has been demonstrated. As an interesting fact, most receivers that has been found to support the mentioned wireless links using photonic-based transmission are based on III-V Schottky diode SHMs due to their high sensitivity [49]. This will be further discussed in the next section.

Despite the variety of photomixers solutions that can be found in the state-of-the-art (independent from III-V UTC-PD and III-V PIN diodes) [45], they fully rely on III-V based technologies. Therefore, if high-level integration and low-cost solutions are required, one can think of Silicon-based solutions instead. In fact, the first THz link using Silicon Photonic transmitter was demonstrated in 2018 [52] achieving 10 Gb/s data rate at a distance of 0.3 m and a frequency of 297.6 GHz using OOK modulation. Here, a SiGe PIN-PD is proposed

using STMicroelectronics Silicon photonics technology. Furthermore, the same Silicon technology has been used to create photonic circuits to achieve even higher data rates (56 Gb/s) by relying on more complex modulations such as 16-QAM [53]. More detail concerning the associated circuit and the measurement setup can be found in Fig. 13.



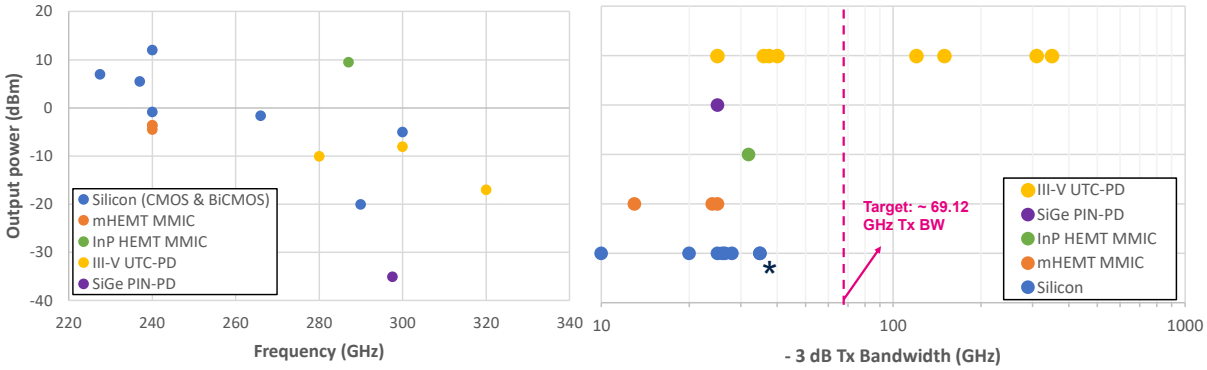
(a) (b)

Fig. 13. (a) A 300 GHz Silicon PIN-PD integrated Tx. (b) Measurement setup using a III-V SHM. Taken from [53].

The modulated optical signal is injected to the module after being previously past through an Erbium Doped Fiber Amplifier (EDFA) where the power into the diode is controlled. The signal is coupled to the IC by using a Grating coupler which is illuminated by the incoming optical fiber. The signal is then emitted in free space by using an antenna adapted to a probe and focused into the receiver, which is composed of a SHM followed by an amplifying chain.

1.3.1.3 All-electronics/photonics Tx above 200 GHz benchmark

Based on the previous review of electronics and photonics Tx architectures state-of-the-art above 200 GHz, one can evaluate which one is the more suitable to support high data rates in a power efficient manner by using low-complexity modulation. Therefore, a comparison of achievable output power and bandwidth is proposed in Fig. 14.



(a) (b)

Fig. 14. Illustration of (a) Tx output power and (b) Tx -3 dB RF bandwidth for different Tx architectures in Silicon (CMOS and BiCMOS) [34], [35], [36], [37], [38], [39], [54], [55], mHEMT MMIC [26], [27], [28], [29], InP HEMT MMIC [31], III-V UTC-PD [43], [46], [47], [48], [49], [56], [57], [58], [59] and SiGe PIN-PD [52] technologies that have been used in wireless links above 200 GHz. *-6 dB Tx bandwidth.

Firstly, one can notice that in terms of output power (in saturation), between 220-320 GHz, electronics Tx solutions (more specifically Silicon) are comparable to III-V UTC-PD. Moreover, concerning III-V MMIC technologies, InP HEMT technology seems to take the lead in terms of achievable output power at higher frequencies. Finally, one can also notice that SiGe-based PIN-PD emitters are far from the observed power trend (20 dB lower). Therefore, it seems that in terms of output power in the targeted frequency window, electronics, and photonic solutions (especially III-V one) should achieve similar output power. Moreover, for moderate distance link a higher gain antenna can enhance the wireless link achievable distance, which could help to mitigate Silicon PIN-PD solution low output power.

However, to remain aligned with our objective to transmit the signal using low-complexity modulations in the IEEE 802.15.3d band, we must search for the Tx solutions that has the largest RF bandwidth. As mentioned before, optical solutions have an inherent broadband nature, which can be confirmed by pursuing the same comparative study with the mentioned Tx solutions, as illustrated in Fig. 14 (b). If we place the desired bandwidth of 69.12 GHz, one can notice that only photonics-based solutions can be able to support such bandwidth and use low-complexity modulation scheme to achieve high data rates.

1.3.2 Rx above 200 GHz

From the previous section, we showed that in terms of transmitted power, the electronics and optical solutions are comparable in the explored frequency window. However, an optical Tx strategy will be taken into advantage due to improved bandwidth. Concerning the overall wireless link, the Tx and Rx performances can be related by the Friss equation:

$$d = \frac{\lambda}{4\pi}\sqrt{\frac{G_{TX} \times G_{RX} \times P_{TX}}{P_{RX}}} \qquad \text{Equation 3}$$

Where d is the distance between the Tx and Rx, λ the wavelength, G_{TX}, G_{RX} are the Tx and Rx antenna gains and P_{TX}, P_{RX} are the emitted and received power. This equation will be our reference to improve the budget link of our proposed solution. As mentioned, in Tx all the studied solutions are comparable in terms of emitted power. Moreover, if there is a difference in power it can be compensated by high-directivity antennas, as shown in the previous section. Therefore, it seems that the axis of improvement of the wireless links comes from the receiver part, i.e. the minimal power that can be detected from the receiver. This can be calculated by the receiver sensitivity (at room temperature, $T_o = 290.5$ K):

$$P_{RXmin}[\text{dBm}] = -174 + 10\log(B) + NF[\text{dB}] + SNRo_{min}[\text{dB}] \qquad \text{Equation 4}$$

Where B is the bandwidth of the Rx, NF is the noise figure and $SNRo_{min}$ the minimal signal-to-noise ration required at the output of the Rx. Since the required SNR is given by the type of modulation that will be used, there are two factors that remains to improve the sensitivity of the receiver: The bandwidth and the noise factor. However, since large BW operation is mandatory for our application, we target large BW Rx with the smallest possible noise figure.

Therefore, we will explore the different Rx architectures that are used above 200 GHz that can satisfy these conditions.

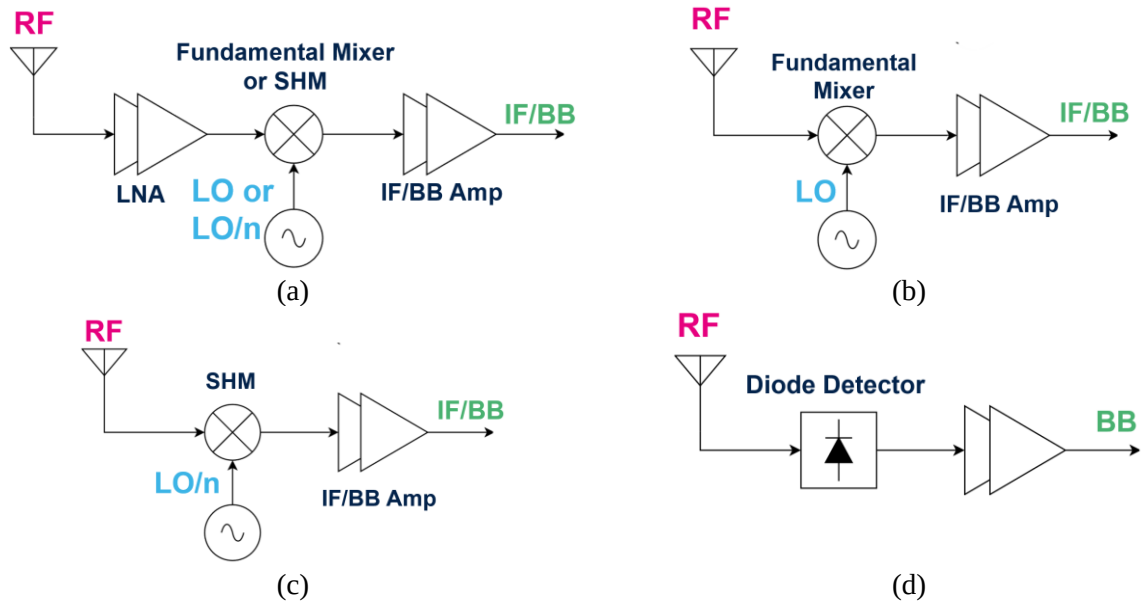


Fig. 15. Different electronics Rx architectures above 200 GHz found in the literature: (a) LNA-first, (b) Fundamental Mixer first, (c) SHM first and (d) Diode detector.

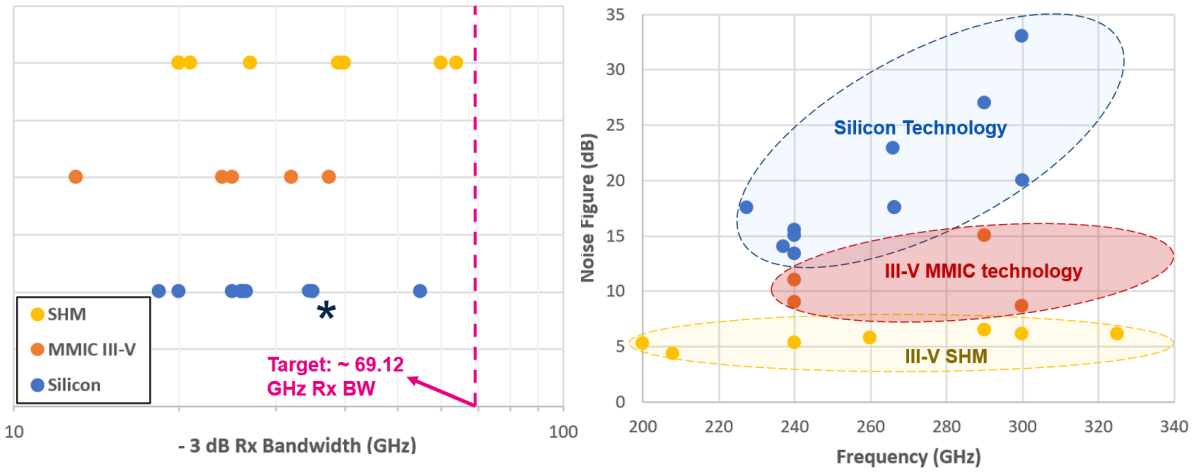
In this section, a special focus will be made to electronics receivers since it has been the traditional way to support wireless links above 200 GHz whether the Tx is optics-based or electronics-based. Nevertheless, in 2019 it has demonstrated the first purely optical Tx and Rx wireless link at a carrier frequency of 310 GHz, achieving a data rate of 10 Gb/s over a distance of 58 meters [60]. At the receiver part an ultra-fast photoconductor coupled to a bow-tie antenna is used to realize the down-conversion thanks to an optically-generated LO signal.

Coming back to electronic-based Rx, the different architectures that can be found in the literature are presented in Fig. 15. The most traditional receiver is the LNA-first architecture, which is widely used for Rx circuits below 200 GHz. The LNA is used as the first block since it provides low noise figure, thus improving the receiver sensibility. However, the integration of a LNA is mainly conditioned by the associated f_{max} of the technology. Therefore, is more usual to find LNA-first architectures above 200 GHz in high f_T/f_{max} technologies such as mHEMT [26], [27], [28], [29], [30] and InP HEMT [31], [32]. In the presented mHEMT circuits, the LNA chain is followed by a balanced resistive SHM which uses transistors as voltage-controlled resistors. For InP HEMT Rx, the LNA chain is followed instead by a fundamental resistive mixer. In fact, the choice between the use of a sub-harmonic or a fundamental mixer is mainly justified by the available LO power.

Moreover, thanks to relatively-high f_T/f_{max} $(300/500\,\text{GHz})$ of Silicon-based technologies such as BiCMOS, one can think of the integration of a LNA in the Rx part also. In this logic, in [37] a LNA is integrated before a gilbert fundamental mixer. However, due to limitations in terms of the LNA bandwidth and noise factor above 200 GHz [39], some BiCMOS

solutions opted instead to eliminate the LNA, leading to a mixer-first architecture [38], [39], which is illustrated in Fig. 15 (b). All the studied references use Gilbert-cell fundamental mixers in 130 BiCMOS technology. Moreover, one can find more mixer-first architectures in CMOS Rx above 200 GHz due to the limited f_{max} (280 GHz [33]). Here, balanced passive gate-pumped transistor mixers operating in fundamental LO frequency are used, which has improved gain compared to a sub-harmonically pumped mixer in CMOS technology [33], [34], [35].

Another Rx architecture that is widely used above 200 GHz is the SHM first. More specifically, SHMs based on Schottky diodes and packaged in metallic split-block modules. Chapter 4 explains more in detail this Rx block architecture. This solution is used mainly in the Rx block of wireless links when the Tx is generated optically due to their low noise figure and large bandwidth. In fact, this can be confirmed more in detail by comparing the Rx bandwidth and the noise figure of the presented solutions, as illustrated in Fig. 16.



(a) (b)

Fig. 16. Different -3 dB bandwidth and noise figures reported for Rx modules in Silicon technologies (CMOS, BiCMOS) [33], [34], [35], [36], [37], [38], [39], [54], [55], [61], [62], III-V MMIC (mHEMT and InP HEMT) [27], [28], [32], [56] and III-V GaAs SHMs [63], [64], [65], [66], [67], [68], [69], [70], [71] in the explored frequency window. *-6 dB Rx bandwidth.

We can notice firstly that based on the studied Rx blocks; no solution achieves an Rx bandwidth in line with targeted value. Therefore, this implies splitting the received signal into at least two sub bands. This will be further discussed in chapter 4. In addition, the higher BW reported is using Schottky diode SHM (64 GHz) [68]. Moreover, if we observe the reported noise figures, the solution that has the lowest NF values is again the III-V Schottky diode SHM. In consequence, SHM solution seems the most interesting one for Rx operative above 200 GHz.

In addition, since we are targeting direct conversion and low-complexity modulation (OOK/PAM4), as discussed in section 1.2, one can think also of a simple receiver using a Schottky diode detector (DET), as illustrated in Fig. 15 (d). However, this solution is limited by the receiver noise figure. This can be verified by a simple calculation considering

commercial zero bias detector with a typical Noise Equivalent Power NEP of 11 $\mathrm{pW}/\sqrt{\mathrm{Hz}}$ [72]. The NF can be calculated in function of the NEP and the bandwidth B as:

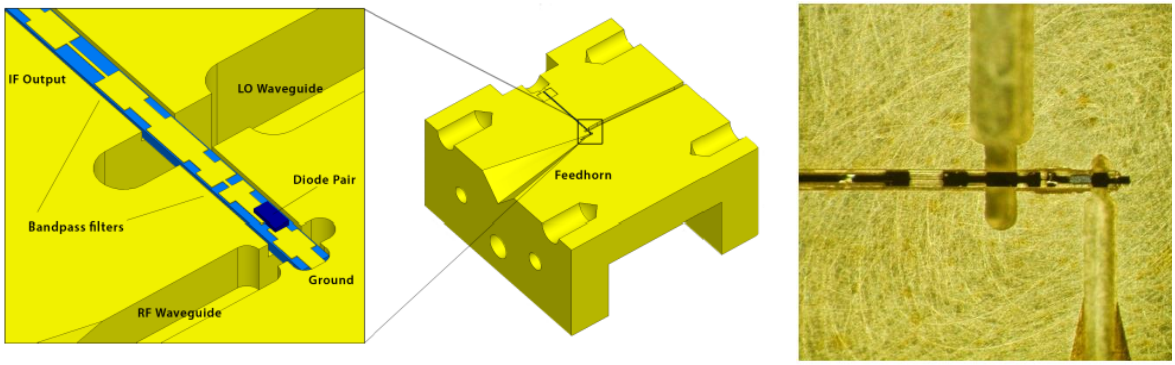
$$\mathrm{NF\,[dB]} = 10\log(\mathrm{NEP}) - \frac{1}{2}\log(\mathrm{B}) + 174 \qquad \text{Equation 5}$$

Which leads to a noise figure of 59.4 dB, assuming a bandwidth of 13 GHz (lowest bandwidth value reported in the literature, as observed in Fig. 16 (a)). Considering an SNR = 10 dB, one can calculate the sensitivity of the detector using the Equation 4, as shown in Table 3.

Ref.	Rx first block	Technology	Conversion Gain (dB)	Noise figure (dB)	Sensitivity (dBm)
[56]	LNA	III-V	6.5	8.6	-54.3
[73]	LNA	SiGe BiCMOS	10.5	16	-46.9
[39]	Gilbert-Cell fundamental Mixer	SiGe BiCMOS	7.5	17.5	-45.4
[74]	Schottky diode SHM[5]	III-V	-6.1	6.13	-56.7
[72]	Schottky DET	III-V	N/A	59.4	-3.46
NA	LNA + Schottky DET	III-V	N/A	52.9	-9.96

Table 3. Different first Rx blocks found in the literature (at 240 GHz), which are potential candidates for direct detection including possible LNA + Schottky detector arrangement to improve sensitivity. N/A: Not available/ Not apply.

We can notice that for a given bandwidth value (worst case for better sensitivity) and SNR, a simple DET exhibits the worst noise figure i.e. a less sensitivity compared to the other studied solutions. In this logic, one can include a LNA operating at 240 GHz (III-V LNA precisely) to improve the noise figure. However, even with this approach, a simple detection by diode is not possible. Therefore, it seems that of all the electronic-based Rx architectures the III-V Schottky diode SHM is the best option to achieve large bandwidth with the lowest possible noise figure.



(a) (b)

[5] NF calculated from the DSB noise temperature observed in the curves of the WR3.4SHM model @ 270 GHz, which is ~900 °K at the reference [74]. CL obtained at the same frequency.

Fig. 17. Illustration of a 664 GHz SHM in GaAs III-V technology [75]. (a) 3D model of the circuit integrated in a metallic split-block module and (b) Top view of the actual module.

However, III-V Schottky diode SHMs are expensive, since they rely on GaAs technology and they are packaged inside a full metallic split-block module, as illustrated in Fig. 17. In this example, the LO and RF signals are routed via CNC-machined waveguides from the exterior of the module until a Quartz substrate where the passive functionalities (in this case filters) are made. Finally, the main element is the Schottky diode which is arranged into an antiparallel configuration. This block is the non-linear element that will produce the mixing of RF and LO frequency. The IF signal is then extracted from the other side of the GaAs substrate. This leads to the second inconvenience related to the lack of package assembling automated process since the die attach and wirebond of the GaAs circuit is made manually.

The high-performances of the III-V Schottky diode SHM are due to the high cut-off frequency of GaAs Schottky diodes, which is traduced into low diode series resistance and junction capacitance. This can be confirmed by the state-of-the-art of the cutoff frequency of different Schottky diodes in III-V and Silicon technologies, as illustrated in Fig. 18. We can notice that III-V vertical Schottky diodes takes the lead, achieving maximal cut-off frequencies of ~3 THz. Moreover, we can notice that in previous work (Gidel, V) Schottky diodes based on BiCMOS technology have been developed achieving cutoff frequencies around 1 THz [41], paving the way for the proposition of cost-effective Silicon SHM solutions at THz frequencies. The mentioned Silicon Schottky diode is presented in chapter 2.

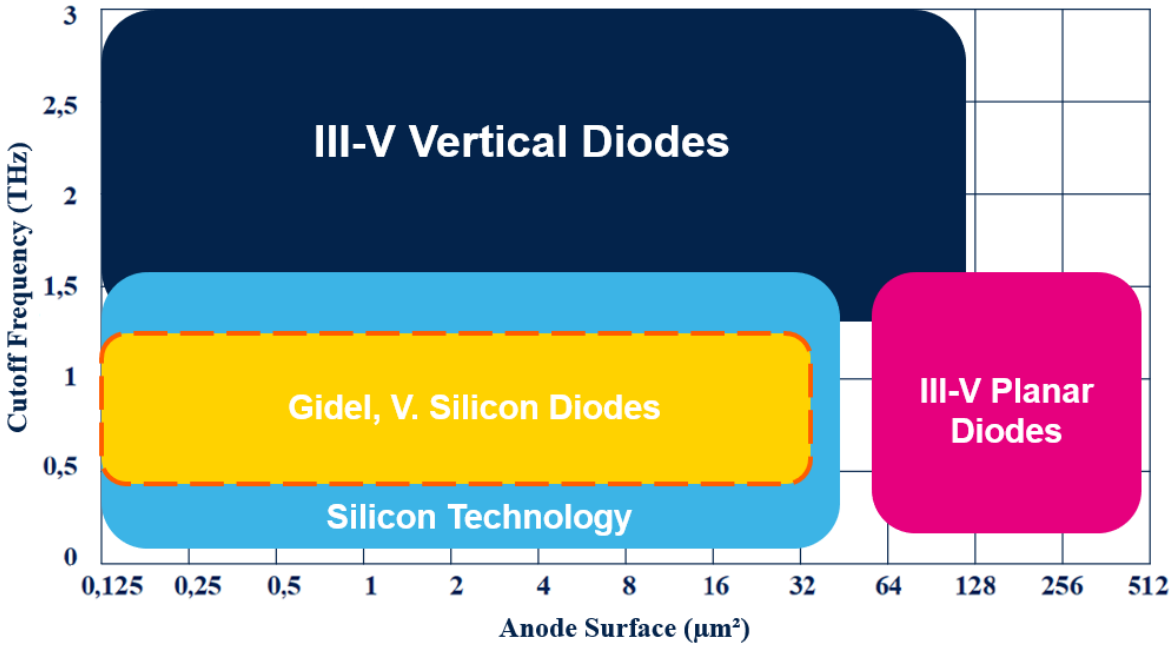


Fig. 18. State-of-the-art of Schottky diodes in different technologies and achieved performances. Adapted from [41].

Moreover, the potential of cost-effective packaging solutions such as organic substrate integration has been leveraged in previous work (Fiorese, V) above 200 GHz [76]. The integration strategy is detailed in Chapter 3. This solution enables packaging alternatives to improve the assembling process of integrated circuit into metallic split-block modules.

1.4 PhD Scientific Objective

According to the previous discussion, the design of the receiver should be the main challenge to enable high data rate wireless links in a power efficient manner. Since high cutoff frequencies have been demonstrated using BiCMOS Schottky diodes [41] and innovative integration strategy using organic laminate substrate and metallic split-blocks [76], the question is now to determine if we can achieve high-performance and cost effective SHM design operating between 253-321 GHz using Silicon technologies. To address this challenge, we defined the following objectives for this thesis:

- **Improvement of Silicon based Schottky diode modeling**

Leverage previous Schottky diode design in BiCMOS technology and improve the modeling of extrinsic elements. Validation to be performed leveraging previous SHM W-band design.

- **Proposition of innovative integration strategy for Silicon circuits above 200 GHz**

Leveraging previous integration strategy developed in the context of Fiorese V. PhD [76] and identifying new axis of improvements.

- **Design of 268 GHz BiCMOS Schottky diode SHM**

Based on the leveraged Silicon Schottky diode and the proposed innovative packaging technology, we initiate the design of a packaged Silicon SHM solution operating at 300 GHz.

1.5 Conclusions & Perspectives

In this chapter, a review of the evolution of communication generations is given, which is driven by the consumers' never-ending demand of more and more connectivity. In fact, this is translated into an exponential augmentation of global data traffic each year. In this logic, the improvement of devices and associated wireless network is essential to support the forecasted data rate growth required for the emerging communication technologies such as 5G and even further the 6G which is expected to be deployed in the next decade, targeting peak data rates higher than 100 Gb/s, and up to 1 Tb/s.

To achieve those high data rates, the increase of the carrier frequency of wireless links is necessary, targeting larger frequency bands to achieve higher data rates in a power efficient way. Therefore, higher frequency solutions are explored in the upper band of allocated 5G technologies: more specifically, the E-band (60 – 90 GHz). However, it has been noticed that the associated power consumption to achieve data rates higher than 2 Gb/s in commercial solutions at 60 GHz is too high, due to the required digital processing to support complex modulation schemes. Moreover, the highest reported wireless links data rate are achieved using offline demodulation post-processing due to the complexity of required digital Application Specific Integrated Circuit (ASIC). Consequently, even if high-complexity modulation such as 64QAM can be considered it seems clear that such system will not be practical at high frequency from a system complexity and power consumption point of view.

Therefore, we propose to use low-complexity modulations which eliminate the necessity of power-consuming complex digital processing. However, this approach requires to use higher frequency spectrum where a larger bandwidth is available. In this logic, the 252-321 GHz spectrum defined by the 802.15.3d standard for future 6G communications is targeted as a promising solution to achieve high data rates in a power efficient way. Exploring recent wireless link above 200 GHz we can notice that photonic Tx solutions seem to be a good candidate to support the targeted frequency bandwidth (~69 GHz) due to their inherent broadband operation. Concerning the Rx part, Mixer-first GaAs Schottky diode sub-harmonic receiver architecture is the favorite solution due to its low sensitivity and good bandwidth compared to other Rx architectures.

However, GaAs Schottky diode SHMs are expensive since they rely on GaAs technology, and they are packaged in metallic split-block modules. Fortunately, innovant Schottky diodes integrated in BiCMOS technology with cutoff frequencies above 1 THz have been demonstrated as well as cost-effective packaging solutions with organic laminate substrates above 200 GHz. Therefore, the main objective of this thesis is to investigate if we can achieve high-performance and cost effective SHM design operating between 253-321 GHz using Silicon technologies.

Chapter 2
BiCMOS Schottky Diode & W-band SHM Preliminary Design

2.1 The SHM

2.1.1 Mixer description

A mixer is a three-port device that uses a non-linear or time varying block to achieve frequency conversion [77]. In communication systems it is used to translate a signal in frequency without modifying the carried information. Specifically, the mixer shifts the information signal to a higher frequency (f_{RF}) to be emitted wirelessly in free space and inversely it is used to transpose the received signal into a lower frequency (f_{IF}) to be treated easily with conventional electronics. In consequence, two operating modes can be distinguished: up-conversion and down-conversion. In this thesis, we will focus on mixers in down-conversion configuration.

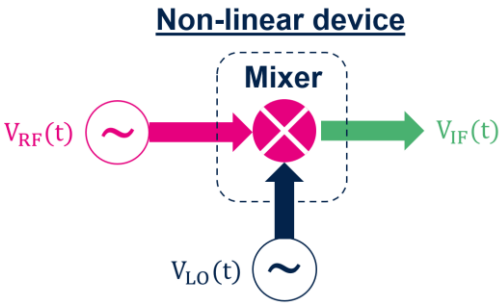


Fig. 19. Mixer schematic symbol in down-conversion configuration.

The schematic representation of a mixer in down-conversion configuration is presented in Fig. 19. The high-frequency incoming signal $V_{RF}(t)$ with frequency ω_{RF} contains the information signal thanks to previous amplitude, frequency, or phase modulation. This RF signal is injected at one of the inputs of the mixer. Then, a local oscillator (LO) reference signal $V_{LO}(t)$ with frequency ω_{LO} close to the frequency ω_{RF} is injected at the other input port. Both mentioned signals can be represented as

$$V_{RF}(t) = V_{RF}\cos(\omega_{RF}t) \quad \text{Equation 6}$$

$$V_{LO}(t) = V_{LO}\cos(\omega_{LO}t) \quad \text{Equation 7}$$

In an ideal mixer, these signals are then multiplied in the time domain to result in an intermediate signal (IF) $V_{IF}(t)$ composed of two signals by the form of $A\cos(\omega t)$ placed at $\omega_{RF} - \omega_{LO}$ and $\omega_{RF} + \omega_{LO}$ respectively

$$V_{IF}(t) = V_{RF}(t)V_{LO}(t) = \frac{V_{LO}V_{RF}}{2}(\cos((\omega_{RF} - \omega_{LO})t) + \cos((\omega_{RF} + \omega_{LO})t)) \quad \text{Equation 8}$$

Then, the modulated information can be extracted from the IF signal by filtering the high-frequency or the low-frequency component. It must be noticed that the Equation 8 is the multiplication result of an ideal mixing device. However, due to the non-linear behavior of the mixer (which is usually made with diodes or transistors), it is expected the generation of parasitic harmonics which are multiple of a fundamental frequency. In that sense, the mixing block must be treated instead as a non-linear network with an associated distortion of the input signals.

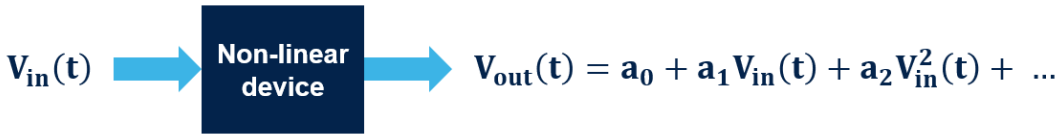


Fig. 20. Non-linear distortion of an input signal caused by a non-linear device.

In Fig. 20, the expected distortion of an input signal entering to a non-linear circuit is illustrated. The output response can be represented as a Taylor series in terms of the input signal:

$$V_{out}(t) = \sum_{i=0}^{\infty} a_i V_{in}^i(t) \qquad \text{Equation 9}$$

In the case of a mixer, we can represent the input signal $V_{in}(t)$ as the addition of the mixer input signals $V_{RF}(t)$ and $V_{LO}(t)$ as follows

$$V_{in}(t) = V_{RF}(t) + V_{LO}(t) = V_{RF}\cos(\omega_{RF}t) + V_{LO}\cos(\omega_{LO}t) \qquad \text{Equation 10}$$

By replacing Equation 10 into Equation 9, and by expanding the series using standard trigonometrical identities, we obtain multiples cosine signals with a spectral response of harmonics of the form $m\omega_{LO} \pm n\omega_{RF}$ with m and n positive integers. These combinations of frequencies are called *intermodulation products* and the order is defined as $|m| + |n|$ [77]. Moreover, by expanding Equation 9, and when $i = 1$, we obtain the following expression:

$$a_1 V_{RF}\cos(\omega_{RF}t) + a_1 V_{LO}\cos(\omega_{LO}t) \qquad \text{Equation 11}$$

Which are the intermodulation products of order 1, also called the fundamental harmonics of the input signals since their response corresponds to ω_{RF} and ω_{LO} frequencies. If we continue to expand at $i = 2$ we obtain:

$$\frac{a_2}{2}\left(V_{RF}^2 + V_{LO}^2\right) + \frac{a_2}{2}V_{RF}^2\cos(2\omega_{RF}t) + \frac{a_2}{2}V_{LO}^2\cos(2\omega_{RF}t) + a_2 V_{RF}V_{LO}\cos((\omega_{RF} - \omega_{LO})t) + a_2 V_{RF}V_{LO}\cos((\omega_{RF} + \omega_{LO})t) \qquad \text{Equation 12}$$

Which are the intermodulation products of order 2. from an ideal mixer, which are presented also in Equation 8. If we continue to expand, for example for $i = 3$ we can obtain more products that are multiples of fundamental frequencies ω_{LO} and ω_{RF}. We can notice that in these products, it is contained the expected signals at frequencies $\omega_{LO} \pm \omega_{RF}$

$$\left(\frac{3a_3}{4}V_{RF}^3 + \frac{3a_3}{2}V_{RF}V_{OL}^2\right)\cos(\omega_{RF}t) + \left(\frac{3a_3}{4}V_{OL}^3 + \frac{3a_3}{2}V_{OL}V_{RF}^2\right)\cos(\omega_{LO}t) + \frac{a_3}{4}V_{RF}^3\cos(\omega_{RF}t) + \frac{a_3}{4}V_{OL}^3\cos(3\omega_{LO}t) + \frac{3a_3}{4}V_{OL}^2V_{RF}\left[\cos((2\omega_{RF} + \omega_{LO})t) + \cos((2\omega_{RF} - \omega_{LO})t)\right] + \frac{3a_3}{4}V_{RF}^2V_{OL}\left[\cos((2\omega_{OL} + \omega_{RF})t) + \cos((2\omega_{OL} - \omega_{RF})t)\right] \qquad \text{Equation 13}$$

Which are the intermodulation products of order 3. A special attention must be given to the products at $2\omega_{LO} \pm \omega_{RF}$ due to their proximity to the fundamental frequencies ω_{LO} and ω_{RF}. In fact, if we continue to expand Equation 9 it will appear more products close to the fundamental frequencies, perturbing the wanted operation of the mixer. In addition, it must be noticed that the amplitude of the intermodulation products decreases as the intermodulation order increases.

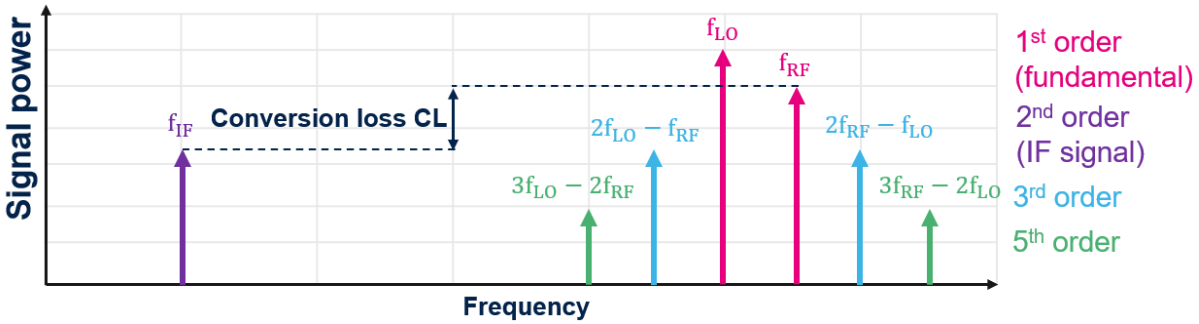


Fig. 21. Representation of intermodulation products in the vicinity of LO and RF frequencies. Adapted from [41].

We represents some intermodulation products of order 1, 2, 3 and 5 which are in the vicinity of fundamental frequencies in Fig. 21 ($\mathbf{f\ [Hz] = \omega/2\pi\ [rad]}$).The 4th order intermodulation products are not illustrated since they are far from $\mathbf{f_{LO}}$ and $\mathbf{f_{RF}}$ frequencies. The lower frequency intermodulation product of 2nd order is also presented and corresponds to one of the expected IF frequencies defined by the addition and subtraction of the fundamental frequencies as shown in the following equation:

$$f_{IF} = f_{RF} \pm f_{LO} \qquad \text{Equation 14}$$

Due to the mixing operation, the amplitude of the IF signal will be reduced. This amplitude is traditionally compared with the amplitude of the input RF signal leading to the Conversion Loss (CL) of the mixer. Multiples devices can be used as non-linear element for the generation of the mentioned IF signal. In this logic, two categories of mixers can be identified: resistive and active mixers. The resistive mixers uses mainly diodes or cold Field Effect Transistors (FETs) whereas the active mixers uses mainly bipolar transistors or a type of FETs previously polarized [78]. Concerning diode resistive mixers, the Schottky diode is one of the most used non-linear devices for mixing in mmW and THz frequencies thanks to higher speed of operation compared to other types of diodes [78]. This will be further discussed in section 2.2.

Diode-based mixers can be classified by simple diode mixers, single and double-balanced diode mixers or even higher-level balanced mixers [79]. The choice of the type of diode-mixer is mainly conditioned by the required signals isolations and the targeted complexity of the circuit. However, these topologies are mainly driven by the LO fundamental frequency, which is close to the RF frequency. In consequence, for operations at mmW and THz frequencies they are not suitable since at those frequencies the available LO power is a main

concern [80]. One solution is to pump the diodes with the harmonics of the LO power, leading to a sub-harmonical mixing operation.

2.1.2 The SHM

The SHM differs from a "fundamental harmonic mixer" since the n harmonic of the LO frequency is used to place the IF signal at the desired frequency f_{IF}

$$f_{IF} = f_{RF} \pm nf_{LO} \qquad \text{Equation 15}$$

This allows the use of a LO signal with a lower frequency to pump the mixer. Sub-harmonic mixing can be achieved by using just a simple diode. However, the RF signal will mix with all the harmonics of the LO frequency. This behavior is required for applications such as the input of spectrum analyzers, where a wide range of LO harmonics is necessary. However, this configuration is not suitable for telecommunication applications since it will require the implementation of additional filters to reject the non-desired harmonics [79]. In consequence, an Antiparallel Diode (APD) configuration is definitely a more effective way of mixing the RF signal with the desired LO harmonic. In this thesis we choose to operate the mixer by using the 2nd harmonic of the LO signal (n = 2).

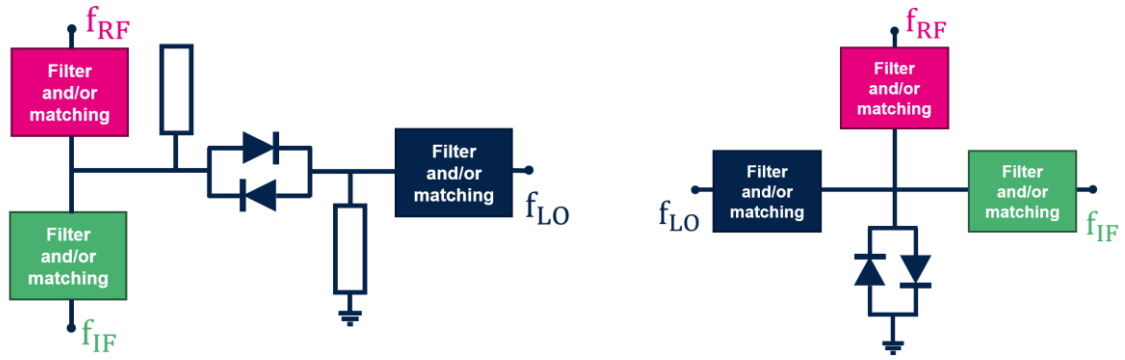


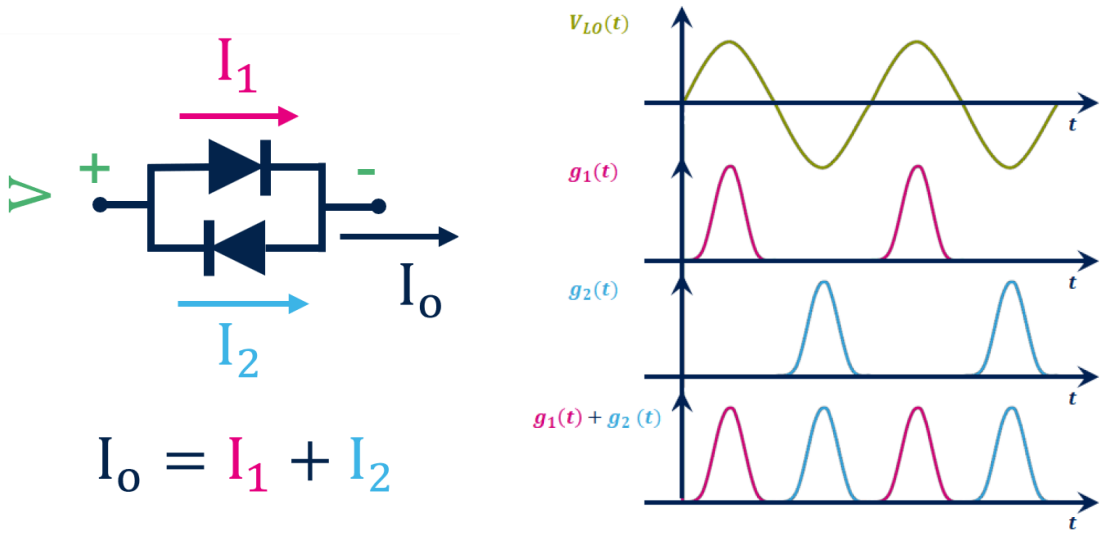
Fig. 22. Series and shunt configuration of the APDs in the SHM.

An APD configuration consists of two diodes interconnected in antiparallel directions. The APD can be used in series or in parallel (shunt) configuration in the SHM as illustrated in Fig. 22. Despite the variations of the circuit topology, the working principle is the same. The first presented architecture as the series topology (Fig. 22 (a)), inserts and extracts the RF and IF frequencies by one side of the diodes and inserts the LO frequency by the other. It uses a short-circuited stub with 180º electrical length at RF frequency to short the RF frequency after passing through the diodes while being transparent for the LO frequency. There is also an open-circuit stub with 90º electrical length at LO frequency providing a short circuit for the LO frequency after passing through the diodes. In fact, this architecture is widely used for MMIC SHMs where the RF frequency is close to the 2nd LO harmonic, leading to an IF frequency around the units of GHz [41].

In addition, one can think in the series architecture to extract the IF signal from the LO port instead (and invert the position of the stubs). However, this architecture is less popular in

MMIC SHMs since it requires additional measures to isolate the LO signal from the IF port [79]. In fact, this architecture is more aligned with waveguide-based configurations since the LO and IF frequencies are mainly extracted by the same port of the diodes.

The second architecture (Fig. 22 (b)) is the shunt configuration, where one of the terminals of the APD is connected directly to ground, whereas the other side is connected to all three RF, LO and IF ports. The proper routing of the signals is ensured thanks to the network of filters in the input diode's port. However, this architecture is rarely used in MMIC due to the difficulty to separate the RF, LO and IF signals at the same port [78].



(a) (b)

Fig. 23. (a) The APD configuration and (b) the non-linear conductance pumped by LO signal. Taken and adapted from [41].

The SHMs generate the required mixing harmonics thanks to the mentioned APDs. A detailed description of this element is illustrated in Fig. 23 (a). If we calculate the currents I_1 and I_2 passing through each diode versus an applied tension V we have

$$I_1 = I_S\left(e^{\frac{qV}{\eta KT}} - 1\right) \quad \text{Equation 16}$$

$$I_2 = -I_S\left(e^{-\frac{qV}{\eta KT}} - 1\right) \quad \text{Equation 17}$$

Where I_S is the saturation current of the diode, q the electron charge, η the ideality factor, K the Boltzmann constant and T the temperature. If we calculate the output current we obtain

$$I_o = I_1 + I_2 = I_S\left(e^{\alpha V} - e^{-\alpha V}\right) = 2I_s \sinh(\alpha V) \quad \text{Equation 18}$$

Where "α" is known as the diode slope parameter and represents the effect of the ideality factor η and the temperature T of the diode [79]. As we notice, this leads to a hyperbolic sine function that can be represented by his Taylor series as

$$I_O = 2I_S \sum_{i=0}^{\infty} \frac{\alpha^{2i+1}}{(2i+1)!} V^{2i+1} = AV + BV^3 + CV^5 + \cdots \quad \text{Equation 19}$$

Where A, B, C … are the coefficients related to the function expansion. By replacing the applied voltage V by the addition of the input signals $V_{LO}(t)$ and $V_{RF}(t)$ (Equation 10) we can notice than the APD configurations suppress the products of $m\omega_{LO} \pm n\omega_{RF}$ when $m + n$ is an odd integer. In conclusion, the DC component, and the following frequencies $2f_{LO}$, $2f_{LO} + 2f_{IF}$ and $4f_{LO}$ are filtered. Concerning the junction conductance of the APD, it is modulated by only the LO signal, therefore the driving voltage over the diodes V can be reduced to

$$V(t) \approx V_{LO}\cos(\omega_{LO}t) \qquad \text{Equation 20}$$

To calculate the junction conductance, we derivate the currents passing through the diodes with respect to the applied voltage $V(t)$

$$g(t) = g_1(t) + g_2(t) = \frac{dI_1}{dV} + \frac{dI_2}{dV} = \alpha I_s\left(e^{\alpha V} + e^{-\alpha V}\right) = 2\alpha I_s \cosh(\alpha V) \qquad \text{Equation 21}$$

By replacing Equation 21 with Equation 20, we can obtain the total conductance modulated by the LO signal. The non-linear behavior of the conductance is illustrated in Fig. 23. (b). Here we assume that both diodes are identical. The final output spectrum with the filtered frequencies is illustrated in Fig. 24.

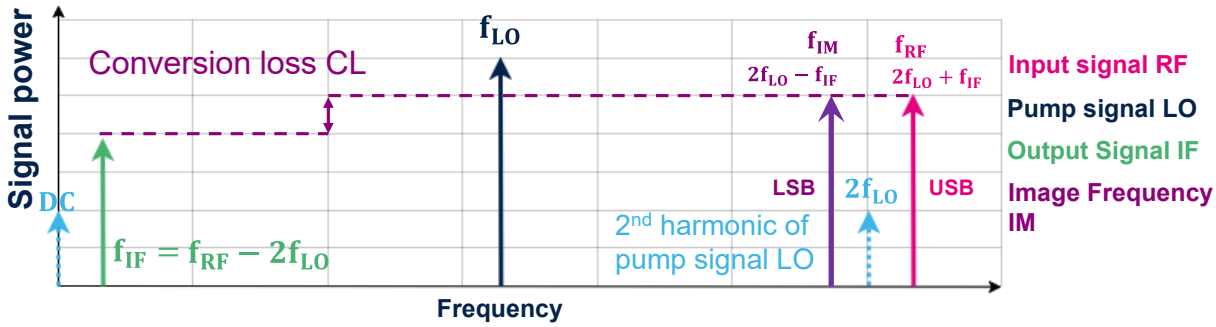


Fig. 24. Spectrum of a 2nd order SHM. Adapted from [41]

The frequencies that have been filtered thanks to the APD (DC and $2f_{LO}$) are illustrated as dotted arrows. Moreover, the RF signal at f_{RF} is called the Upper-Sideband USB and an image signal at f_{IM} which is symmetrically placed in relation to the 2nd harmonic of LO signal at $2f_{LO}$ is called the lower-sideband LSB. In practice, just the USB is required, which corresponds to a mixer operating in Single-Sideband (SSB). However, when both bands are used, it is said that the mixer operates in Double-Sideband (DSB). In SSB operation, the required signal is called RF signal and the other one corresponds to the image frequency. The second one is not needed and must be filtered [41].

2.1.3 Figures of merit of a down-conversion SHM

The operation of down-conversion ensures that the RF Incoming signal is transposed to the desired frequency IF. However, in this process, there are losses associated to the frequency translation. This can be quantified by the power difference (in dB) between the input RF signal P_{RFin} and the output signal IF P_{IFout}

$$\mathrm{CL\ (dB)} = \mathrm{P_{RFin}\ (dBm)} - \mathrm{P_{IFout}\ (dBm)} \qquad \text{Equation 22}$$

Which is a positive quantity. Moreover, one can express this parameter in terms of a conversion gain G_C (dB), which is basically the negative value of the conversion loss (in dB). Even more, we can quantify the capacity of the mixer to avoid the leakage of a certain signal from one port into another [41], [78]. This is represented by the isolation parameters. Concerning the 2nd order SHM, one defines the isolation of the 2LO harmonic in the RF port as

$$\mathrm{Isolation}\left.\frac{2LO}{RF}\right|_{dB} = \mathrm{P_{LO}(dBm)}|_{\mathrm{LO\ port}} - \mathrm{P_{2LO}(dBm)}|_{\mathrm{RF\ port}} \qquad \text{Equation 23}$$

It must be noticed that this is not strictly considered as an isolation parameter since the LO and 2LO signals in both accesses does not have the same frequency [78]. Moreover, we can quantify the difference of power between two spectral signals into a given port. This is represented by the rejection parameter. In the case of a down-conversion mixer, the rejection of the image frequency is critical since this signal is transposed to the f_{IF} frequency in the same way than the RF signal. In this logic, we define the image rejection parameter by Equation 24. The updated frequency spectrum illustrating the mentioned rejection of the image frequency is illustrated in Fig. 25.

$$\mathrm{Rejection\ IM}|_{dB} = \mathrm{P_{IF[RF]}(dBm)} - \left.\mathrm{P_{IF[IM]}(dBm)}\right|_{\mathrm{IF\ port}} \qquad \text{Equation 24}$$

Another aspect that must be evaluated in the SHM is linearity. In fact, the linear operation of the device is limited by the non-linear distortion behaviors such as the saturation of the output power and the intermodulation distortion [77], [78]. The first one, also called gain compression, is caused by high levels of input power. This figure of merit is described by the *1 dB compression point*, which represents the power level for which the output power has decreased by 1 dB from the ideal linear characteristics [77].

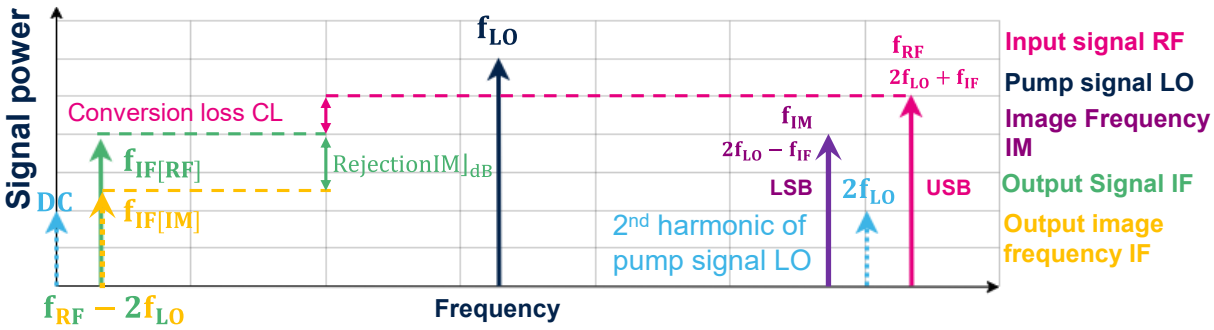
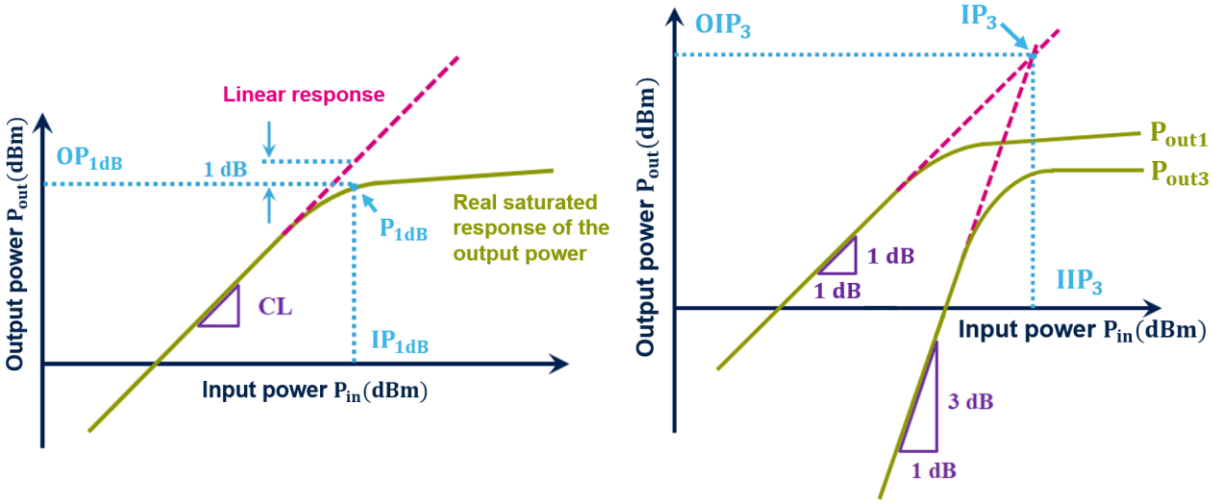


Fig. 25. Output spectrum of a 2nd order SHM illustrating the image rejection. Adapted from [41].

The saturation of the output power versus the input signal is illustrated in Fig. 26 (a). We can see that the output power will follow the desired linear response until get to a point where it gets 1 dB saturated with respect to the expected linear response. The saturated power level is denoted as P_{1dB} and it can be stated in terms of the input power IP_{1dB} or the output power OIP_{1dB}. For mixers, it is usually represented by the input power IP_{1dB}. Finally, the

relationship between the input and output 1 dB saturation powers can be expressed as in the Equation 25, where CL_0 is the conversion loss of the mixer in linear operation.

$$OP_{1dB}(dB) = IP_{1dB}(dB) - CL_0(dB) - 1dB \qquad \text{Equation 25}$$



(a) (b)

Fig. 26. 1 dB compression point P_{1dB} and determination of third order interception point IP_3 of a mixer. Adapted from [41].

The second limiting point for the linearity of the mixer is the intermodulation distortion. It must be noticed that the device is exposed to a series of frequencies in the vicinity of the mixer RF operation band [78]. This will generate intermodulation products, due to the mixing of those non-desired frequencies with the desired input signal. It must be noticed that the 3rd order intermodulation products are the most critical due to their proximity to the fundamental signal.

The output powers of the fundamental signal P_{out1} and the 3rd order intermodulation product P_{out3} in function of the input power are illustrated in Fig. 26. (b). The 2nd order intermodulation product is not represented since it is far from the operation band of the mixer. The fundamental signal product is proportional to the input power, so the line describing the response has a slope of 1 dB/dB. Also, the line describing 3rd order product has a slope of 3 dB/dB. In must be noticed that both signals will intersect in a point since they have different slopes. In this logic, we define the third-order intercept point IP_3 as the intersection of both lines [77], [78]. The relation between the intercept point and the corresponding input and output power at this point can be expressed as:

$$OIP_3(dB) = -CL_0(dB) + IIP_3(dB) \qquad \text{Equation 26}$$

To extract the value of IIP_3 by measurements, one can measure the power difference between the output power of the fundamental signal P_{out1} and the power of the generated intermodulation product P_{out3} for a given input power. In the case of a mixer, the output fundamental signal corresponds to the intermediate frequency IF output and the input power is the RF signal [41], [78].

$$C/I3(dB) = P_{IFout}(dBm) - P_{out3}(dBm)$$ Equation 27

This difference $C/I3$ is then replaced in the following equation to obtain the IIP3 value

$$IIP3\ (dB) = \frac{C/I3\ (dB)}{2} + P_{RFin}(dB)$$ Equation 28

We must consider that the input power P_{RFin} must be set to a low value to remain in linear operation but also not too small to obtain a good measurement of the 3rd intermodulation product P_{out3}.

2.2 The Schottky Diode

As mentioned before, the Schottky diode is used as the non-linear element for generating the harmonics of the SHM thanks to high switching speeds and low forward resistance compared to other types of diodes [79]. In this section, a special focus will be made on this element since it is the main element of the SHM.

A diode is a device that allows current flow easily in just one direction. Different as PN diodes made by the union of a P type semiconductor (SC) and an N semiconductor, Schottky diodes are made by the union of an N or P semiconductor with a metal, as shown in Fig. 27. The main Schottky diode's characteristic is that conduction is due to majority carriers instead of conduction achieved by both majority and minority carries in PN diodes. This characteristic allows high-frequency operation capability and low forward voltage drop [79]. Thanks to the two mentioned characteristics, Schottky diodes have multiple applications in electronics domain more than the SHMs, such as in active and passive imaging, far infrared detection, low noise VCOs, charge pump, low voltage reference circuits, etc.…

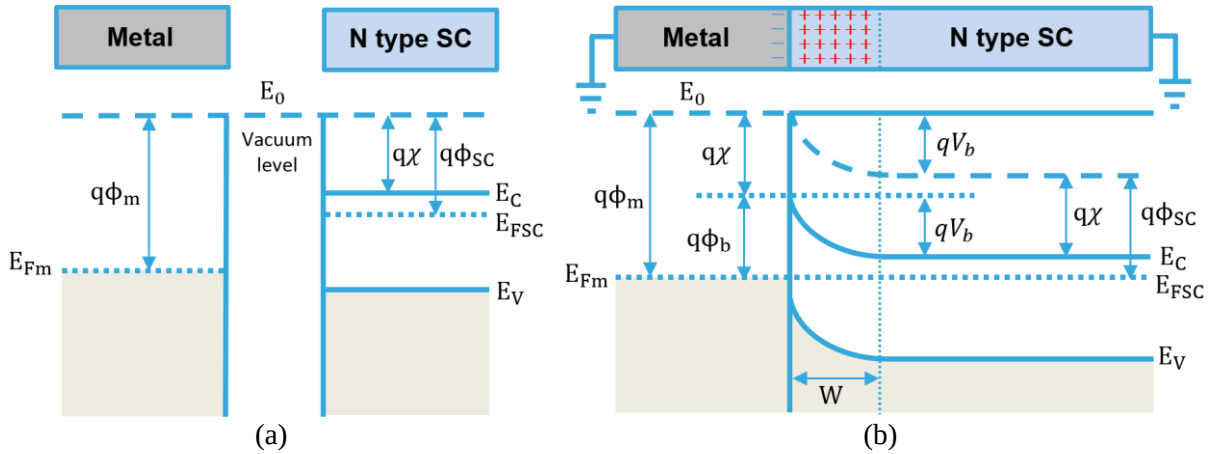


Fig. 27. Energy band of N-type Schottky diode with $q\varphi_m > q\varphi_{SC}$ (a) before contact and (b) after contact.

As explained, Schottky diodes are formed by the junction of a metal with an N or P-type semiconductor. However, not all union of this two material forms a Schottky junction [81]. In the energy band model, the metal is characterized by his *fermi level* E_{Fm} and *work function* $q\phi_m$. On the other hand, the semiconductor is characterized by the *conduction band* E_C, his fermi level E_{FSC}, the *valence band* E_V, the *electronic affinity* $q\chi$, and his work function $q\phi_{SC}$.

These parameters are illustrated in Fig. 27. (a) for a N-type SC and in Fig. 28. (a) for a P-type SC. Work function is defined as the energy needed in a material to shift an electron from his fermi level to the vacuum. Comparing both work functions of metal and semiconductor we can determine if the junction creates a Schottky junction or a *ohmic junction* [81]. N-type SC can be differentiated from P-type SC in energy band model based on *intrinsic fermi level* E_i, defined as $(E_C + E_V)/2$. If $E_{FSC} > E_i$, SC is N-type, whereas if $E_{FSC} < E_i$, SC is P-type.

On one hand, when a metal and a N-type SC are put in contact with $q\varphi_m > q\varphi_{SC}$, a N-type Schottky diode is created. The resulting energy bands are presented in Fig. 27. (b). Before contact, the system stabilizes by alignment of both fermi levels. Since the N-type SC work function $q\phi_{SC}$ is smaller than the metal work function $q\phi_m$, a migration of electrons from the semiconductor into the metal occurs, forming a depletion zone of width W defined by the Equation 29. The depletion zone width depends on the electron charge q, the dielectric permittivity ε_s, the applied voltage V, the doping density N_D and the SC-metal barrier potential V_b. This migration leaves behind a positive charged space in semiconductor side and a narrow negative charge accumulation in metal surface since electron density is already important. Due to this, depletion zone width W is just defined by semiconductor side. Also, this contact forms two barriers: the metal-SC barrier $q\phi_b$ and the SC-metal barrier qV_b, called also in this thesis as the Schottky Barrier potential [81], [82].

$$W = \sqrt{\frac{2\varepsilon_s(V_b - V)}{qN_D}} \qquad \text{Equation 29}$$

When a positive voltage is applied between metal and N-type SC's, the SC-metal barrier is reduced. This allow easy electron flow from the SC into the metal. However, when a negative voltage is applied, the SC-metal barrier qV_b increases so electrons cannot flow easily. For both polarizations, the Schottky barrier remains the same. Finally, if an N-type ohmic junction wants to be formed instead of an N-type Schottky diode, the metal work function $q\phi_m$ must be smaller than the SC work function $q\phi_{SC}$.

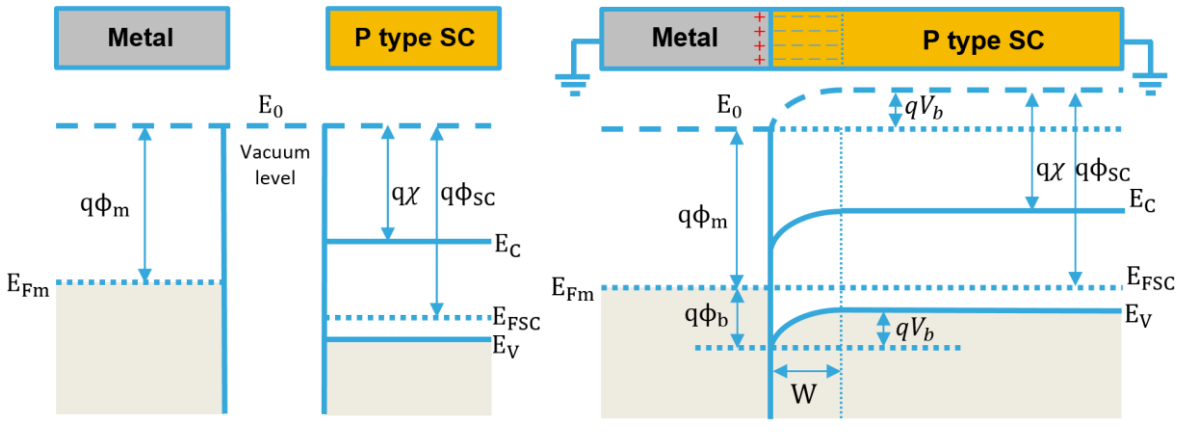
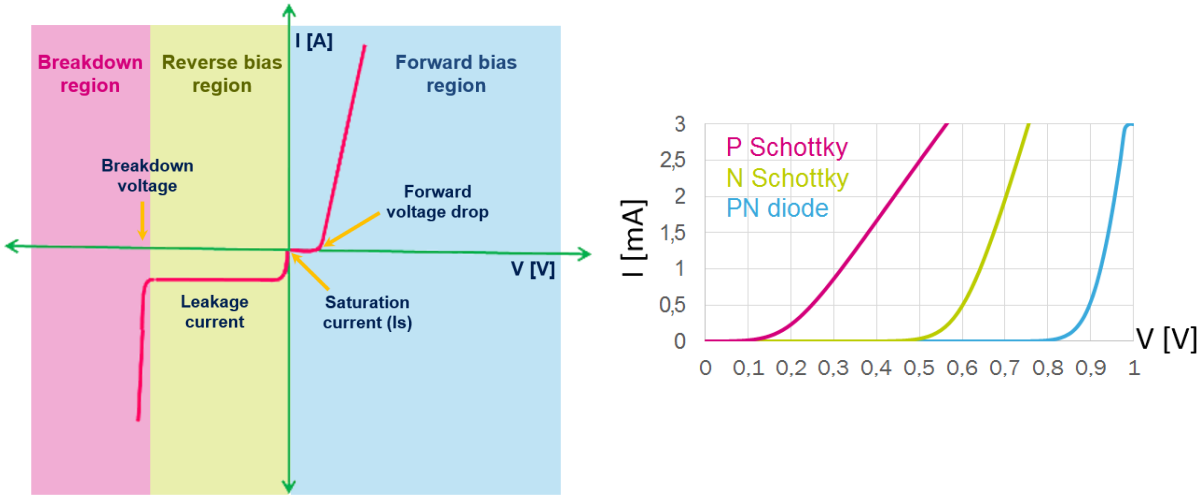


Fig. 28. Energy band of P-type Schottky diode with $q\varphi_m < q\varphi_{SC}$ (a) before contact and (b) after contact.

On the other hand, when a metal and a P-type SC are put in contact with $q\varphi_m < q\varphi_{SC}$, a P-type Schottky diode is created. Energy bands are presented in Fig. 28. Before contact, similar as N-type Schottky diodes, both fermi levels are aligned. Since P-type SC work function is bigger than metal work function, the electrons move from the metal into the semiconductor also forming a depletion zone of width W. This migration leads to a narrow deficit of electrons in the metal surface (positive charge accumulation) and a negative charged space in the SC.

Polarization in P-type Schottky diode is like N-type Schottky diode; it must only be inverted. When a positive voltage is applied between P-type SC and metal, the SC-metal barrier is reduced. This allow easy hole flow from the SC into the metal. However, when a negative voltage is applied, the SC-metal barrier increases so holes cannot flow easily. For both polarizations, the metal-SC barrier remains the same. Finally, similar as N-type Schottky diode, if a P-type ohmic junction wants to be formed instead of a P-type Schottky diode, the metal work function $q\phi_m$ must be bigger than the SC work function $q\phi_{SC}$ [81], [82]. Comparing Fig. 27 and Fig. 28 we notice that both N-type metal-SC and SC-metal barriers are bigger than P-type barriers for the same metal.



(a) (b)

Fig. 29. Description of I-V curve for the Schottky diode and (b) I-V curves' comparison of N-type and P-type Schottky diodes and PN diode.

Ideally diodes are meant to allow current flow when a forward bias voltage is applied ($V \geq 0$) and block current flow in reverse polarization ($V < 0$), similar as ideal switches [79]. In real model, Schottky and PN diodes must cross a potential barrier formed by the junction of the two materials to allow significant current flowing in forward bias. This voltage is called *forward voltage drop* and corresponds to the same V_b in energy band diagrams. When applied voltage is zero, the current is not zero as expected; this current is called the *saturation current* I_s and represents the effects of the junction area and the potential barrier between metal and semiconductor [79]. On the other hand, when real Schottky is reverse polarized, a small value current allows to flow; this current in called *leakage current* I_{leak} and tends to increase when higher reverse voltage is applied until this voltage is big enough to allow reverse current

flow. This final voltage is called *breakdown voltage* B_V. Finally, Schottky I-V behavior can be divided into three regions: forward, reverse and breakdown region, as presented in Fig. 29 (a).

When bias is applied, the current as a function of voltage can be expressed as:

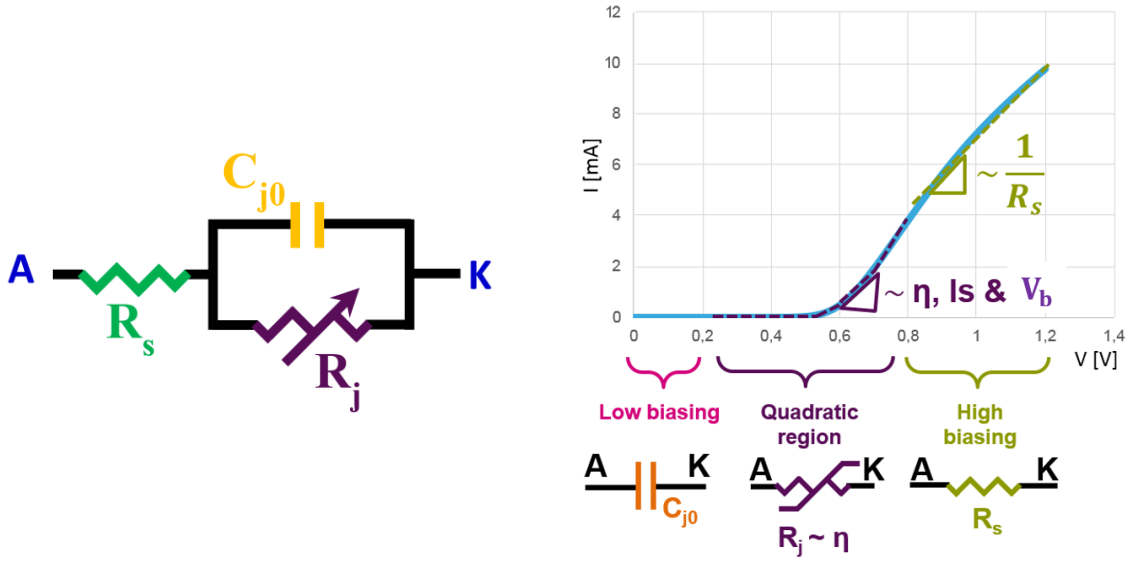
$$I(V) = Is\left(e^{\frac{q}{\eta kT}(V - R_s I)} - 1\right) \qquad \text{Equation 30}$$

Where I_s is the saturation current, q is the electron charge, η is the non-ideality factor, k is the Boltzmann constant, T is the temperature and R_s is the series resistance.

Compared with PN diodes, Schottky diode has some advantages and disadvantages. This can be noticed by comparing both I-V characteristic curves. First, Schottky diodes achieve less forward voltage drop than PN diodes, i.e., less applied forward voltage is needed to allow conduction. However, leakage current increases and breakdown voltage reduces, which are non-suitable characteristics in reverse polarization region. If N-type and P-type Schottky diodes are compared as presented in Fig. 29 (b), we see first that P-type Schottky diodes have smaller forward voltage drop compared to N-type Schottky diodes. Also, P-type Schottky diodes have a less step slope meaning higher series resistance due to lower mobility of holes compared to mobility of electrons [83]. It should be noted that a smaller forward voltage drop reflects a smaller breakdown voltage in reverse bias region, compared to N-type Schottky diodes [83].

2.2.1 Schottky diode intrinsic model

To use the diode as a building component for electronic circuits, the behavior is modeled by lumped elements such as resistances, capacitances, and inductances. The most common Schottky diode intrinsic model is presented in Fig. 30 (a). Since this model is due to intrinsic effects, parasitic capacitances and resistances are not considered. Complete intrinsic model is formed by a series resistance R_s modeling the losses in metal and semiconductor, a non-linear voltage dependent resistance called junction resistance R_j and a non-linear voltage dependent capacitance called the junction capacitance C_j [79].



(a) (b)

Fig. 30. (a) Schottky Diode intrinsic model and (b) its contribution in I-V curve. Adapted from [41].

The series resistance R_s can be computed using square resistance equation considering the current paths in semiconductor and metal. This is the same method used for calculation of extrinsic parasitic resistance that will be described in section 2.4.2. The junction capacitance, produced by the charge stored in the depletion zone, can be computed deriving the depletion charge Q_j with respect to the applied voltage V, obtained by Equation 29 [79]:

$$C_J(V) = \frac{dQ_j}{dV} = \frac{C_{j0}}{\left(1 - \frac{V}{V_b}\right)} \qquad \text{Equation 31}$$

Where C_{j0} is the junction capacitance at $V = 0$ (zero-bias). This junction capacitance can be computed as follow:

$$C_{j0} = S\sqrt{\frac{q\varepsilon_s N_D}{2V_b}} \qquad \text{Equation 32}$$

Where S is the area of the Schottky junction, ε_s is the dielectric permittivity of the Silicon semiconductor and N_D is the average doping density seen at metal-SC interface. On the other hand, junction resistance R_j can be computed with the junction conductance g(V), which is the derivation of the diode current from Equation 30 with respect to voltage [79]:

$$\frac{1}{R_j} = g(V) = \frac{dI(V)}{dV} = \frac{q}{\eta kT}(I(V) + I_s) \approx \frac{qI(V)}{\eta kT} \qquad \text{Equation 33}$$

Where η is the ideality factor. The equation can be approximated since the saturation current I_s is small enough to not be considered. The influence of these lumped components can be noticed in the I-V curve as shown in Fig. 30 (b). First, since current conduction is very low (low biasing), C_J takes the lead. After applying enough biasing, R_j is small enough to allow current flow (entering in quadratic region), continuing to reduce until R_s takes the lead (at high biasing region).

2.2.2 Figures of merit of a Schottky diode

To evaluate the Schottky diode performances, the figures of merit are defined and used in the state-of-the-art to evaluate their improvement. The most described parameters are shown in Table 4.

Figure of merit	Equation	Label
Cutoff frequency $f_c(R_s, C_{j0})$ [Hz]	$f_c = \frac{1}{2\pi R_s C_{j0}}$	Equation 34
Ideality factor η	$\eta = \frac{q}{kT}\left(\frac{dV}{dLn(I)}\right)$	Equation 35
Schottky barrier potential V_b[V]	$V_{bN} = \phi_{bN} - \frac{E_C - E_{FSC}}{q}$ $V_{bP} = \phi_{bP} - \frac{E_{FSC} - E_C}{q}$	Equation 36
Breakdown voltage B_V [V]	$B_V = 60\left(\frac{E_g}{1.1eV}\right)^{\frac{3}{2}}\left(\frac{N_D}{10^{16}cm^{-3}}\right)^{-3/4}$	Equation 37
Saturation current I_s [A]	$I_s = A^* S T^2 e^{-\frac{qV_b}{kT}}$	Equation 38
Responsivity $\mathcal{R}$ [V/W] or [A/W]	$\mathcal{R} = \frac{V_{out}}{P_{in}}$	Equation 39
Noise Equivalent Power NEP [$W/\sqrt{Hz}$]	$NEP = \frac{V_{noise}}{\mathcal{R}}$	Equation 40

Table 4. Figures of merit of Schottky diodes.

One of the most important figure of merit is the cutoff frequency f_c. It evaluates the high-frequency behavior of Schottky diodes. Nowadays, researchers pay special attention to this parameter in order to evaluate if these diodes are suitable for recent millimeter wave and Terahertz applications [84]. So, to have faster diodes, this parameter must be optimized. Based on the definition we see that it is inversely proportional to the series resistance R_s and the zero-bias junction capacitance C_{j0}. So, we always look to have the best tradeoff between junction capacitance C_{j0} and series resistance R_s to obtain the smallest product of this quantities.

The second one is the ideality factor η, which represent the non-ideality effects of the Schottky diode due to imperfections on the Schottky junction, quantum tunneling of electrons and non-constant barrier height when bias is applied [79]. Typically, this parameter is close to 1.0 and reflects how close is the diode to the ideal I-V curve. When η is far from 1.0 (near to 2.0), the majority carriers' concentration at the metal-SC interface is more important. This behavior can reduce the barrier height V_b and the breakdown voltage B_V. However, It can also increase noise and conversion loss [79].

The third, fourth and fifth figure of merit can be qualified as DC figures of merits and reflect more the behavior of the I-V curve. First, the Schottky barrier potential V_b is made by the interface of the metal deposition on moderate doped area. In some applications such as

detectors, this potential must be as little as possible in order to achieve a good frequency response and bandwidth [85]. Second, the breakdown voltage is the tension in reverse polarization where the diode allows conduction. Finally, the saturation current I_s, which is the current at zero bias depends on Richardson constant A^*, the Schottky contact area S, the temperature T, the electron charge q, the Boltzmann constant k, and the Schottky barrier potential V_b.

Finally, we have the *responsivity* $\mathcal{R}$ and the *noise equivalent power* NEP, which are used to evaluate detectors' performance. First, the responsivity is defined as the relation between the detected voltage (or current) and the input power of the detector. Second, the noise equivalent power is defined as the input power that achieves a signal to noise ratio of 0 dB with a 1 Hz output bandwidth [86]. For diode detectors, this figure of merit (NEP) is used to evaluate their sensitivity [86], as the example illustrated in Table 3.

2.3 State-of-the-Art of Integrated Schottky Diodes

2.3.1 III-V planar Schottky diode

In this section, the evolution of the Integrated Schottky diodes is presented. Concerning III-V Schottky diodes, two categories can be distinguished: vertical and planar Schottky diodes. The first one corresponds to the Schottky diodes based on whisker contacts, which are one of the first diode architectures developed by Walter Schottky in the early 1900s. However, whisker diodes face several limitations in terms of repeatability, withstanding of high vibrations and cryogenic temperatures, inability to use multiple anodes and difficulty of integration with conventional RF components [87]. To overcome these problems, planar Schottky diodes have been introduced.

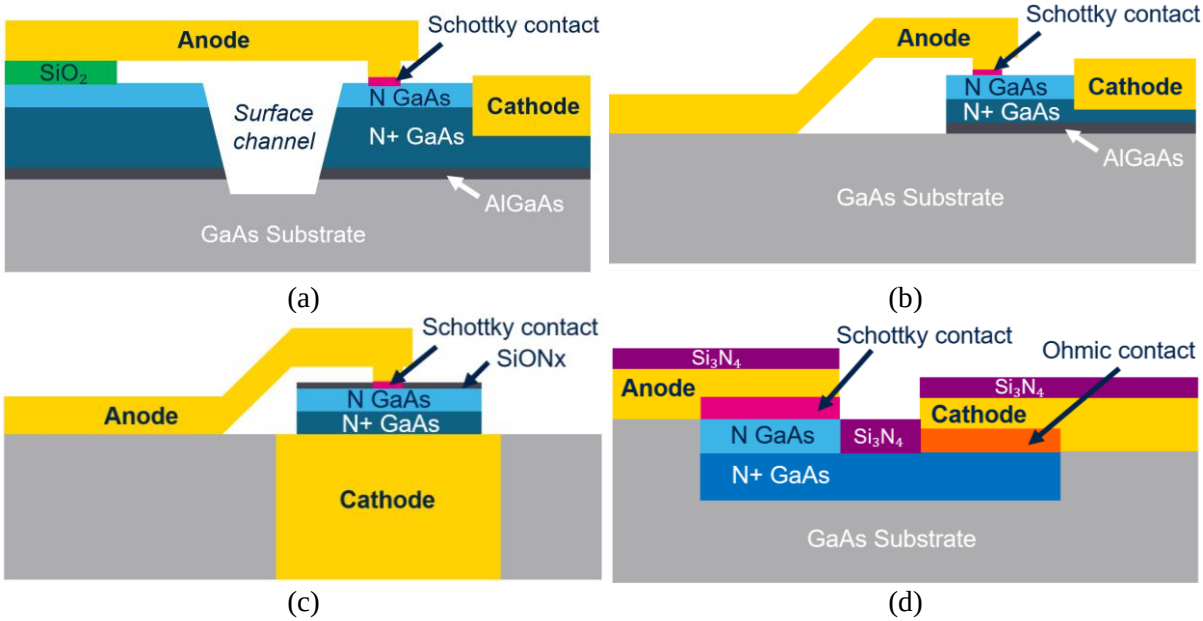


Fig. 31. Simplified cross-sectional view of different III-V planar Schottky diodes. (a) Surface-channel etch diode, (b) Air-bridged diode, (c) Quasi-vertical diode and (d) Buried Epitaxial Schottky (BES) diode. Adapted from [88].

One of the first planar Schottky diode architectures is the surface-channel etch diode developed by the university of Virginia in 1996. The diode structure is illustrated in Fig. 31 (a). It is characterized by the surface channel below the anode finger which is made to reduce the parasitic capacitance between anode and cathode, creating two *mesas*[6] structures. Moreover, the geometry of the channel walls is controlled thanks to dry or wet etching and the width by the lithography process. This type of architecture has demonstrated SHMs operating at more than 3 THz [89].

To improve the assembly process and mass-production using wafer batch processing, a novel Schottky diode fabrication process has been applied by the Jet Propulsion Laboratory (JPL) and named Air-Bridged planar diodes. The device structure is illustrated in Fig. 31 (b). The main characteristic of this diode is the air bridge, which is made thanks to a metal layer placed over a specialized reflowed photoresist. After removing the photoresist, the metallization layer remains suspended over an empty air space [90]. In addition, the anode and air bridge is made simultaneously, thus minimizing misalignments [87]. Another key improvement of this fabrication process is the mesa structure fabrication, which unlike wet-etching, is made by reactive ion etching process (RIE). This allows the fabrication of smaller mesas, better control of their dimensions and the sidewall's profile, reducing parasitic resistance and capacitance [87].

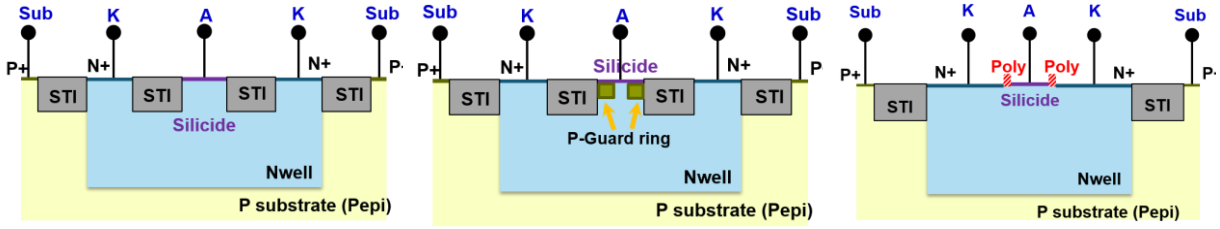
Another proposed architecture is the called Quasi-vertical Schottky diodes. The device is illustrated in Fig. 31 (c). This type of topology promises to reduce additional parasitic resistance and capacitance that appears in a fully planar III-V Schottky diode. The Schottky contact is made at one face of the structure and the ohmic contact is made in the backside of the structure, ensuring a vertical current flow which leads to a smaller equivalent series resistance since the phenomena of current crowding is not present [87]. In addition, this type of architecture have been used to support SHMs working at frequencies higher than 600 GHz [91]. Finally, the Buried Epitaxial Schottky (BES) diodes are introduced using standard foundry process for III-V MMIC at United Monolithic Semiconductors (UMS). The mentioned diode is shown in Fig. 31 (d).

2.3.2 Silicon Schottky diode

2.3.2.1 Silicon Schottky diode state-of-the-art

Thanks to Silicon-based technologies, we can integrate Schottky diodes that compete with III-V technology thanks to higher integration capability and low costs [92]. We introduce then the integrated CMOS and BiCMOS Schottky diodes. Some classic lateral CMOS N-type Schottky diode configurations are shown in Fig. 32.

[6] *Mesa* word is used commonly in semiconductor technology referring to structures with a material elevation having a flat top. It means "table" in Spanish, and it also refers to geographic accidents with the same characteristics.



(a) (b) (c)

Fig. 32. Cut view of different CMOS Schottky diodes architectures using (a) STI, (b) STI and p-guard ring and (c) polyspacer.

The Schottky junction is formed by the contact of the silicide layer with an N-type well moderately doped, forming the anode (A); then, the ohmic contact is formed by doping the N-type well forming an N+ doping region to then apply another silicide layer, forming the diode cathode (K). To isolate the anode from the cathode a Shallow Trench Isolation (STI) or a polyspacer is placed. To isolate the Nwell from the substrate (P-type in this case) the same STI is used.

One of the main goals of integrated Schottky diodes is the increment of cutoff frequency. To achieve this, series resistance R_s and junction capacitance C_{j0} must be reduced to achieve the best tradeoff between these parameters. First attempt is changing the Schottky contact surface area S since the junction capacitance is proportional to his value ($C_{j0} \propto S$) and the series resistance is proportional to $S^{-0.5}$ [93].

In order to reduce the junction capacitance C_{j0} depending on the Schottky junction area S, some authors fix the anode surface area to the minimal dimension allowed by the technology, taken into account the impact on increment of parasitic back-end capacitances [93]. Others even remove the silicide layer to define anode area by just metal finger access; however, this technique strongly increases the series resistance R_s [94].

To reduce the series resistance R_s, it is important to notice that the resistance does not depend only on anode area S, but also on the current path [95]. This can be optimized by minimizing the space between the ohmic junction (cathode) and by increase the Schottky junction area S (anode). Moreover, it can be reduced by increasing N+/P+ diffusion [93]. Best attempt to reduce anode-cathode spacing is by using polyspacer instead of STI [96], [97], as shown in Fig. 32 (c). Also, layout optimization such as four-sided cathode leads to reduction of the series resistance [96].

In other applications, it is important to reduce the leakage current I_{leak}. This current can be reduced by using a guard ring[7] below the Schottky contact, as presented in Fig. 32 (b). However, use of guard ring reduces the average doping N_D under Schottky junction

[7] In the case of a p-guard ring, it is typically formed relying on standard p-channel FET source/drain ion implant [99].

increasing the series resistance R_s. Commercial technology fixes the used silicide material, which must be wisely chosen since a proper material can reduce the Schottky barrier potential. Moreover, some authors arrive to modulate the Schottky barrier potential by carrier injection [92], reducing also the series resistance R_s. However, junction capacitance C_{j0} increases and breakdown voltage B_V and leakage current I_{leak} also increases.

2.3.2.2 BiCMOS and B55X Schottky diode architecture

In this thesis, special attention will be made on Bipolar-CMOS (BiCMOS) Schottky diodes. The BiCMOS technology combines the advantages of two different processes into a same component: the high gain and speed of bipolar transistors and the simplicity and low-power consumption of logic gates [98]. A type of BiCMOS Schottky diode architecture found in the literature [95], [99] is illustrated in Fig. 33.

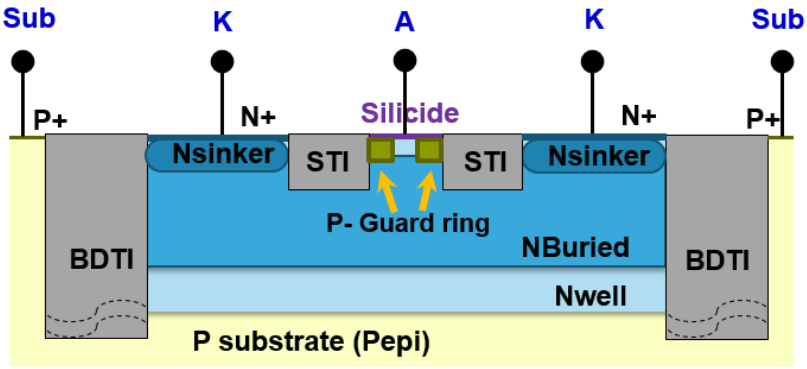


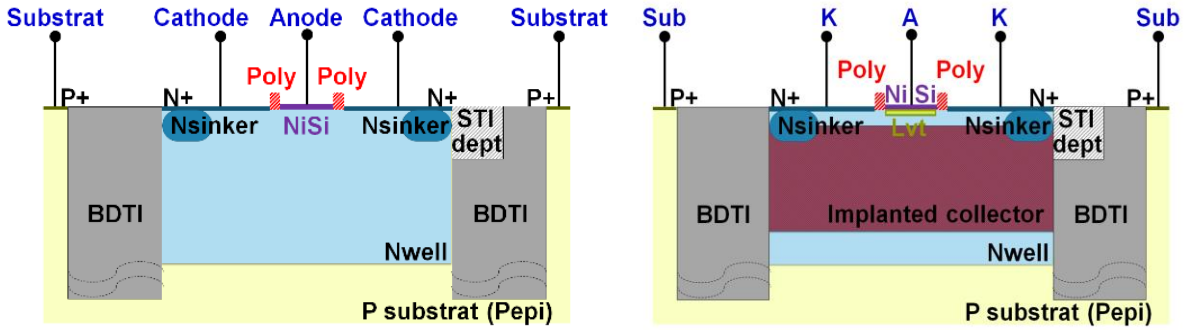
Fig. 33. Cut view of a BiCMOS Schottky diode using STI and guard ring. Adapted from [41].

The first difference between CMOS and BiCMOS architecture is the presence of a BiCMOS Deep Trench Isolator (BDTI), which is approximately ten times deeper than the STI. This leads to a reduction of the parasitic capacitance between the cathode and substrate. Moreover, the BDTI helps to reduce the parasitic coupling between diodes in antiparallel configuration, which is practical for SHMs. The second difference is the use of implantations coming from the Heterojunction Bipolar Transistor (HBT) design process. The highly-doped Nburied layer ($N_D \approx 10^{20}\,cm^{-3}$) is originally used to reduce the resistance in the current path between collector and emitter. Also, the Nsinker implantation ($N_D \approx 10^{19}\,cm^{-3}$) is used to interconnect the collector with the mentioned Nburied layer. In the case of a Schottky diode, both implantations help to reduce the series resistance from the current path between anode and cathode. However, the Nburied can modify the junction capacitance C_J if it is close enough to modify the doping profile in the Schottky junction.

In this logic, in [41] a Schottky diode structure has been proposed in BiCMOS 55 nm (B55) technology inspired by the polyspacer used in the mentioned CMOS architectures [96], [97] and the BiCMOS implantations Nsinker and Nburied. The study concluded that only the Nsinker implantations are required to reduce the series resistance R_S of the diode. In fact, since the polyspacer is less deep than the STI, the current flow is mainly lateral, and since the Nburied is deep enough (verified by the invariability of the junction capacitance C_{J0} by

adding Nburied) the mentioned implantation does not have a relevant impact in the improvement of the series resistance R_S .

So, in this thesis, we propose to work with the mentioned B55 diode using only the Nsinker implantation. The mentioned architecture is illustrated in Fig. 34 (a). The performances of this architecture in terms of the junction capacitance C_{j0} and the series resistance R_S will be illustrated in section 2.4.2.

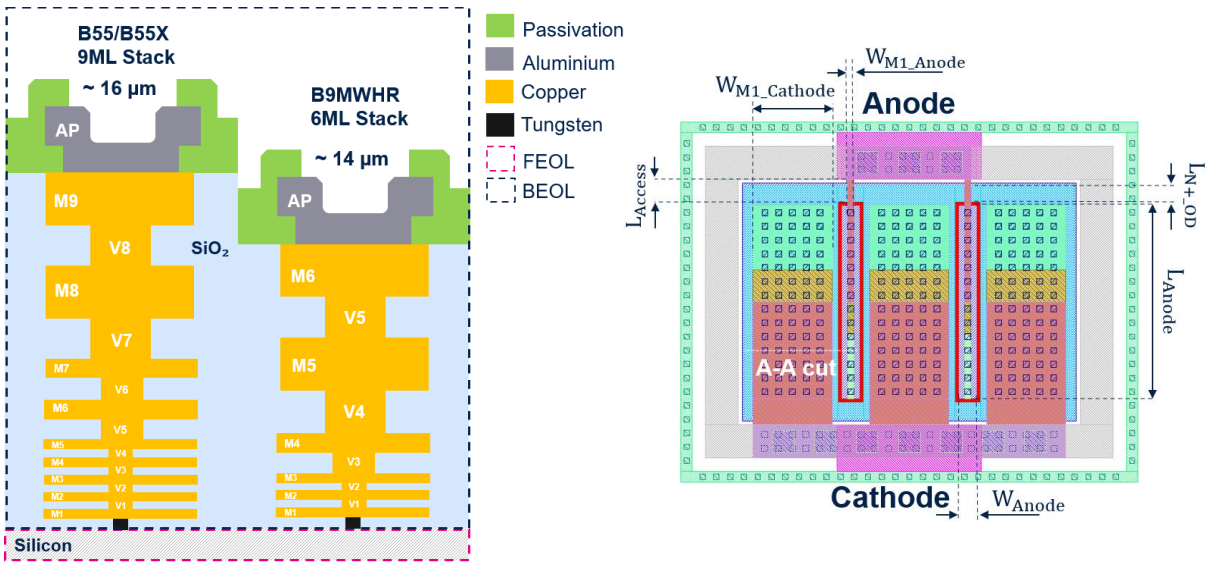


(a) (b)

Fig. 34. (a) B55 and (b) B55X architectures explored in this thesis.

Moreover, with the arrival of the B55X technology, other types of Schottky diode architectures can be formulated. In fact, the main objective of the B55X technology is to improve the Ft/Fmax of HBT in B55 by proposing a new bipolar transistor architecture called *Epitaxial eXtrinsic Base Isolated from the Collector* (EXBIC). An equivalent architecture of a B55X Schottky diode is illustrated in Fig. 34 (b). We can notice that most all elements from the front-end maintains their denominations but the Nburied layer, which has been replaced by an implanted collector (IMCO). Since both Nburied and IMCO layers are supposed to be equivalents from one technology to another, the performances of B55X Schottky diodes are expected to be like those achieved with the B55 technology. In the context of [41], a design-of-experiment (DOE) containing B55X Schottky diodes has been completed with future expected measurement to validate the mentioned hypothesis.

Concerning the mentioned diodes, the previous description has been given in terms of their Front-End-of-Line (FEOL), which corresponds to the device part in the Silicon die where the doping implants are made. It is also called the active or intrinsic part of the diode. However, to connect the active part of the diode with the exterior of the Silicon IC, signal routing with conducting materials must be made. The part where this routing is made is called the Back-End-of-Line (BEOL), and in Silicon technology correspond to the part where the passive components (inductors, transmission lines, etc.) and interconnections at IC level are made. In this part, multiple metallic levels are placed in function of the required interconnection and passive devices complexity. For the B55 and B55X technologies the associated BEOL is illustrated in Fig. 35 (a).



(a) (b)

Fig. 35. (a) Metal stack of the ST 9ML B55/B55X and B9MWHR BiCMOS technology. (b) Top layout view of a 2-finger B55 Schottky diode.

Firstly, it must be highlighted that the BEOL from B55 and B55X technologies is the same, achieving a total heigh of ~16 µm. As illustrated in Fig. 34, the difference between both technologies is at the FEOL part. To interconnect the active part with the metallic stack, a Tungsten via called *contact* is placed. Then, copper metallic levels interconnected thanks to metallic vias are placed. Finally, an aluminum metallic layer is placed at the last metal level. To fulfill the empty spaces, led by the metallic stack, different isolation layers (being the Silicon Oxide SiO_2 the predominant dielectric) are used. These layers are optimized to have the smallest capacitive coupling between two metallic columns. As mentioned, the number of metallic levels is determined by the required application complexity. In the case of B55 and BB5X technologies, 9 metallic levers (9ML) with different thickness are used. In addition, in BiCMOS technology nodes such as the 130 nm BiCMOS High-Resistivity (HR) variant (B9MWHR), 6 Metal levels are used, giving a BEOL heigh of ~14 µm. The main difference between B55/B55X and B9MWHR is the FEOL Silicon resistivity, being 15 Ω.cm for B55/B55X and 150 Ω.cm for B9MWHR. Thanks to this characteristic, this last technology node will be exploited for the design of full passive THz circuits in chapter 3.

Based on the previous defined FEOL and BEOL for the B55 and B55X Schottky diodes, the final Schottky diode structure can be illustrated, as in Fig. 35 (b). Despite the III-V Schottky diodes, Silicon diodes are interdigitated, meaning that multiple Schottky junctions and ohmic contacts are made for a unique anode and cathode. The number of Schottky junctions determines the number of anode fingers N_{fing}. Based on this, the final anode surface area can be determined as

$$S = L_{Anode} \times W_{Anode} \times N_{Fing} \qquad \text{Equation 41}$$

Where W_{anode} is the anode width and L_{anode} is the anode length. These dimensions will be part of the elements to be used for the construction of a Schottky diode analytical model in section 2.4.2.

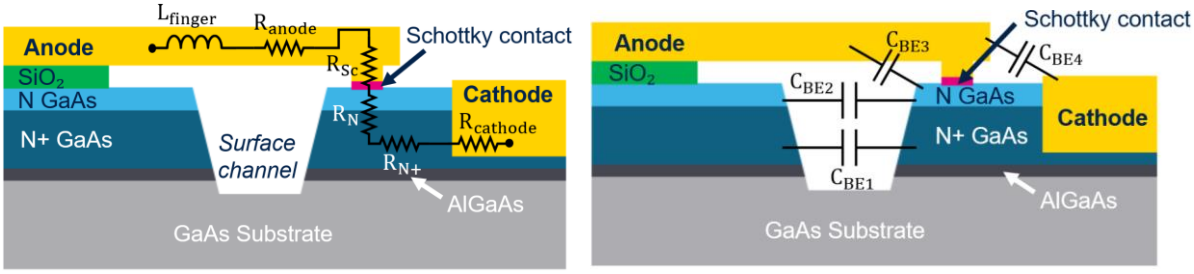
2.4 Modeling of Schottky Diodes for mmW & THz Applications

2.4.1 III-V planar Schottky diode modeling

The total series resistance of the Schottky diode can be calculated considering the average current path between anode and cathode. The total equivalent series resistance is composed of the intrinsic resistive contribution in the FEOL (active part) $R_{S\_Intrinsic}$ and the extrinsic resistive contribution in the BEOL $R_{S\_Entrinsic}$

$$R_S = \sum R_{S\_Intrinsic} + \sum R_{S\_Entrinsic} \qquad \text{Equation 42}$$

The resistive contributions in III-V Surface-Channel Schottky diodes are illustrated in Fig. 36 (a). In the FEOL, the resistances due to the silicide resistivity R_{SC}, the epitaxial N GaAs layer R_N and the Buffer N+ GaAs layer R_{N+} are considered. In the BEOL, the resistances due to the anode finger and cathode pad are represented. Moreover, for THz applications, the inductive contribution due to the diode fingers of III-V Schottky diodes is not negligeable ($L_{finger} \approx 10 - 100$ pH) [75], leading to a considerable impact in the conversion loss of SHMs. In consequence, 3D electromagnetic simulations are made to have an accurate representation of the III-V Schottky diode Back-End considering this inductive contribution and even going further by the optimization of the finger geometry [75]. Therefore, the associated series inductance is included.



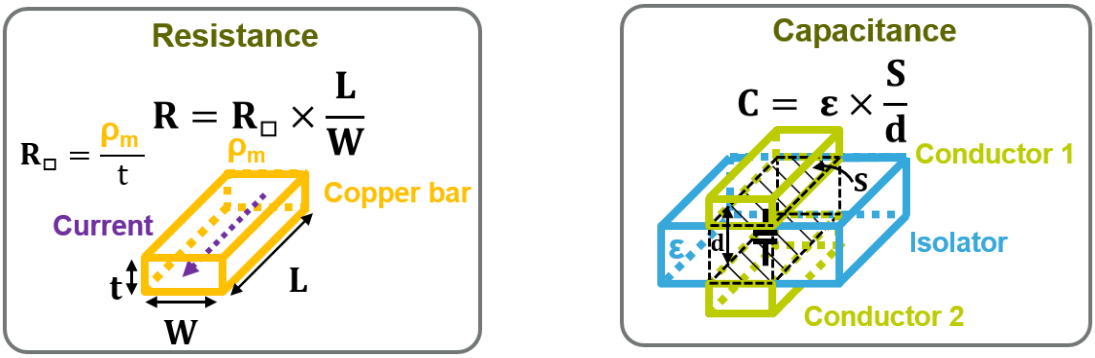
(a) (b)

Fig. 36. (a) Resistive, inductive and (b) capacitive contributions in a surface-channel III-V Schottky diode. Adapted from [41], [100].

The associated capacitive contributions in the previous III-V Schottky diode architecture are illustrated in Fig. 36 (b). In this case, just the extrinsic capacitive contributions are shown, which correspond to the parasitic capacitances formed in the BEOL. The only capacitance considered as an intrinsic contribution is the junction capacitance C_J, which has been defined by the Equation 31. It the case of this architecture, the back-end capacitance C_{BE4} is the most important due to the proximity between the anode and the cathode. Therefore, it cannot be neglected. Moreover, the other back-end capacitances C_{BE1}, C_{BE2} and C_{BE3} can be even more minimized by the use of an Air-finger Schottky diode architecture, as illustrated in Fig. 31 (b).

2.4.2 BiCMOS Schottky planar Schottky diode modeling

Similar as the method illustrated for III-V Schottky diodes where the average current path between anode and cathode has been identified to obtain the diode series resistance, one can think to follow the same strategy for the calculation of the series resistance from the Silicon diodes. In this logic, the series resistance can be calculated considering the circulation of the current inside a rectangular copper bar, as illustrated in Fig. 37 (a).



(a) (b)

Fig. 37. Illustration of (a) extrinsic resistance calculation and (b) extrinsic capacitance calculation. Adapted from [41].

To calculate the series resistance, we consider the dimensions of a rectangular bar with length L, width W and thickness t, and we apply the following equation

$$R_S = R_{\square} \times \frac{L}{W}, \text{being } R_{\square} = \frac{\rho_m}{t} \qquad \text{Equation 43}$$

Where $R_{\square}$ is the square resistance and ρ_m the conductivity of the material. For the capacitance calculation, we consider the capacitance formed between two parallel conductor plates, as illustrated in. This capacitance can be calculated as

$$C_{BE} = \varepsilon \times \frac{S}{d} \qquad \text{Equation 44}$$

Where ε is the effective dielectric constant between both parallel plates and d is the distance between them. For the calculation of both series resistance and the BEOL capacitance C_{BE}, we must identify the dimensions that describes the Schottky diode physically. A preliminary representation of the diode dimensions can be found in Fig. 35 (b). However, a most accurate dimensions description must be made in terms of the FEOL. Therefore, a cut-view of the Schottky diode layout is presented in Fig. 38

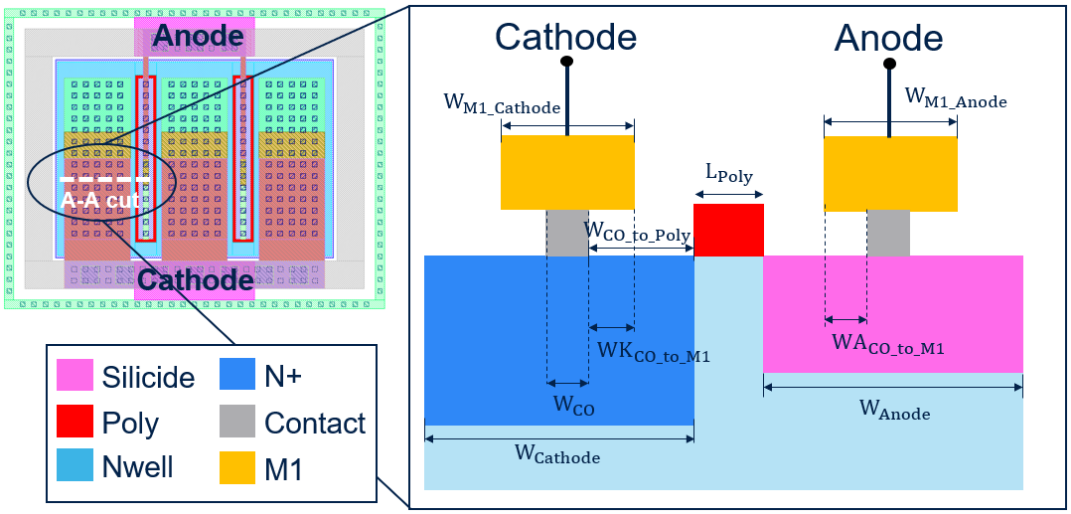


Fig. 38. cut-view illustrating the main dimensional parameters for Schottky diode modeling.

A practical aspect that must be considered for the technology that will be used for the fabrication of the Schottky diodes (B55 and B55X) is the Shrinking factor. This means that the physical dimensions will be ~90% smaller than the design footprint. Although the Shrinked dimensions have been considered for the calculation of the series resistance and BEOL capacitance C_{BE}, no huge impact in their calculations has been found.

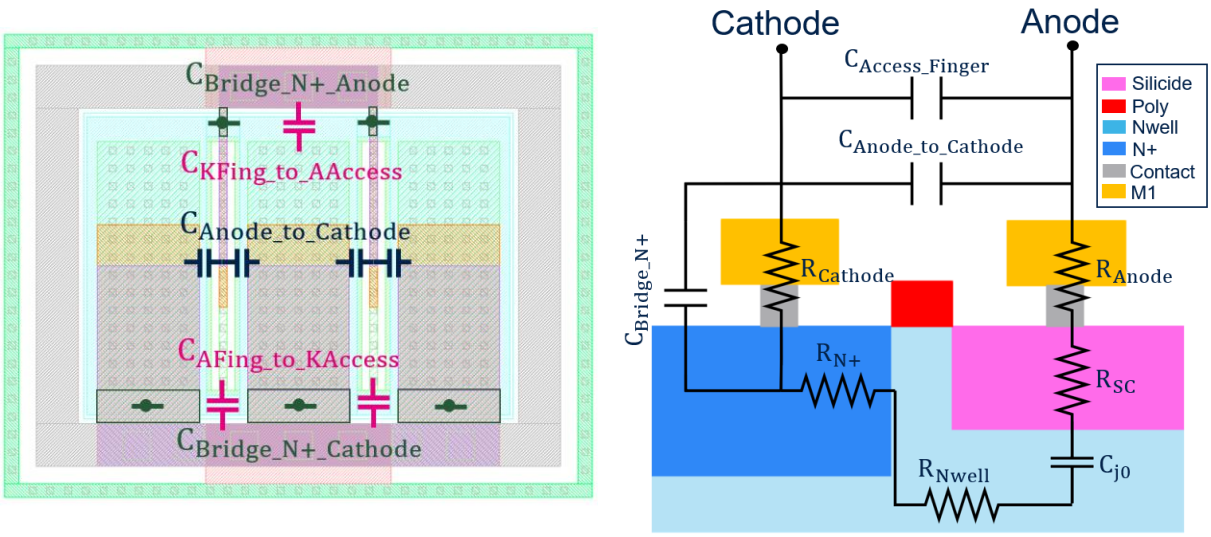
2.4.2.1 Updated total capacitance Schottky diode modeling

In this section, the description of the analytical calculation of the back-end capacitance C_{BE} and junction capacitance C_{j0} will be presented. Reviewing previous works concerning the analytical modelization of 55 nm BiCMOS Schottky diodes [41], it has been found that the model does not match properly with the measurements in terms of the Back-end capacitance C_{BE} and the junction capacitance C_{j0} since the hypotheses of the BEOL structure and doping levels in the FEOL are not valid for the BiCMOS 55 nm technology. This has led to an incorrect preliminary W-band SHM design [41]. Therefore, in this thesis we propose to update the mentioned analytical model with the correct BEOL and FEOL hypotheses to enable the design of an accurate W-band SHM.

Firstly, the zero-voltage junction capacitance can be calculated by replacing Equation 41 into Equation 32

$$C_{j0} = L_{anode} \times W_{anode} \times N_{fing} \sqrt{\frac{q \times \varepsilon_s \times N_D}{2V_b}} \qquad \text{Equation 45}$$

The parameters L_{anode}, W_{anode} and N_{fing} are obtained by the layout fixed dimensions whereas the Schottky barrier potential V_B and the average doping density (seen at metal-SC interface) N_D are taken from DC measurements. Finally, the Silicon dielectric constant ε_S is given by the fabrication process. This capacitance corresponds to the unique intrinsic capacitance in the diode. However, in terms of the extrinsic parasitic capacitance, multiple contributions can be identified, as illustrated in Fig. 39 (a).



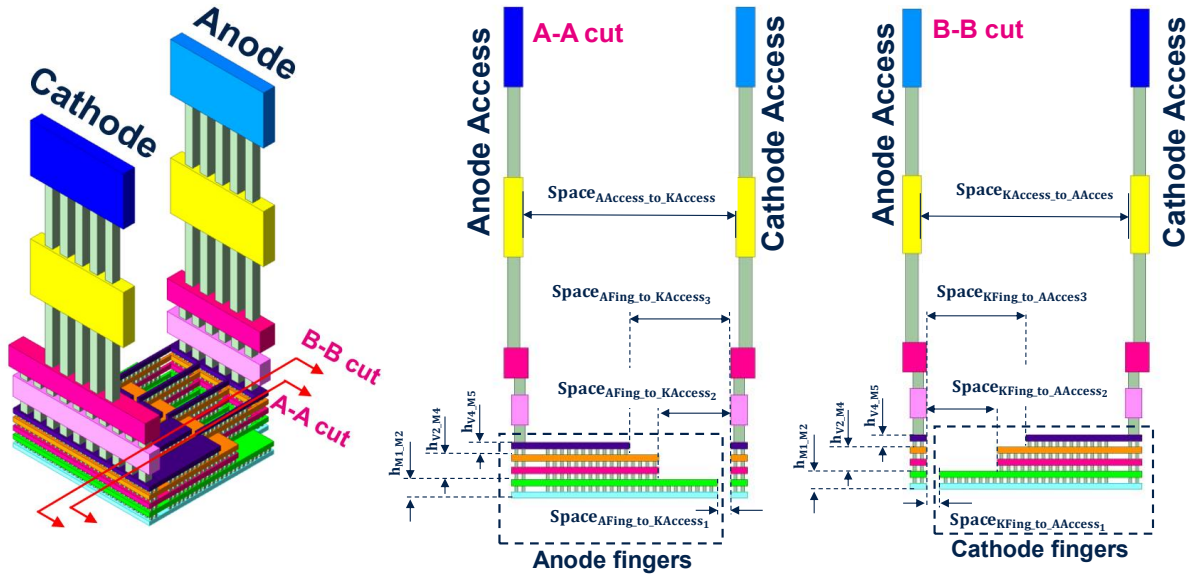
(a) (b)

Fig. 39. (a) Representation of the extrinsic parasitic capacitances in the Schottky diode layout. (b) Cut view of the diode illustrating the mentioned extrinsic capacitances, the junction capacitance $\mathbf{C_{j0}}$ and the series resistances.

All these parasitic capacitive contributions will be considered in parallel to obtain a total back-end capacitance defined by the following equation

$$C_{BE} = C_{Anode\_to\_Cathode} + C_{Access_{Finger}} + C_{Bridge\_N+} \qquad \text{Equation 46}$$

In addition, in this thesis, we consider the escalated metallization profile of anode and cathode between M1 and M5. The mentioned anode and cathode profile can be identified by observation of the 3D model of the BEOL of the Schottky diode. For a 4-finger Schottky diode an example is presented in Fig. 40 (a).



(a) (b) (c)

Fig. 40. (a) 3D model of BEOL of a 4-finger 9-metal levels BiCMOS Schottky diode. (b) A-A cut-view and (c) B-B cut-view.

The first capacitive element represented in Equation 46 is the capacitance formed between the anode fingers and cathode fingers $C_{Anode\_to\_Cathode}$. Due to the anode and cathode fingers proximity, $C_{Anode\_to\_Cathode}$ is one of the main contributors of parasitic capacitance. In fact, this distance is fixed by the condition of minimal distance between anode and cathode for the reduction of the series resistance. To calculate this distance, the dimensions defined in Fig. 35 (b) and Fig. 38 are taken into consideration. The final model for this capacitance is presented in Equation 47. We can notice that the escalated back-end profile has been considered for the capacitance calculation.

$$C_{Anode\_to\_Cathode} = \frac{\varepsilon_0 \times \varepsilon_r \times L_{Anode} \times 2 \times N_{Fing} \times \left(h_{M1\_M2} + \frac{h_{V2\_M4}}{3}\right)}{\frac{W_{Anode}}{2} + L_{Poly} + W_{CO\_to\_Poly} - WK_{CO\_to\_M1} - \frac{W_{co}}{2} - WA_{CO\_to\_M1}} \quad \text{Equation 47}$$

Moreover, we define the second capacitance contribution represented in Equation 46, which is the capacitance formed between the anode and cathode accesses and fingers. In fact, the BEOL is composed of escalated anode and cathode fingers from M1 to M5 that interconnects directly into the Schottky junction formed at the FEOL level, as well as anode and cathode accesses to interconnect the mentioned fingers to the top metal level at M9. This can be seen in detail in the cut-view in Fig. 40 (b), (c). These capacitive contributions between access and finger can be decomposed as

$$C_{access\_finger} = C_{AFing\_to\_KAccess} + C_{KFing\_to\_AAccess} \quad \text{Equation 48}$$

Where $C_{AFing\_to\_KAccess}$ is the capacitance between the anode fingers and the cathode access, and $C_{KFing\_to\_AAccess}$ is the capacitance formed between the cathode fingers and the anode access. The first capacitive contribution can be calculated as

$$C_{AFing\_to\_KAccess} = \varepsilon_0 \times \varepsilon_r \times W_{M1\_Anode} \times N_{Fing} \times \left(\frac{h_{M1\_M2}}{space_{AFing\_to\_KAccess_1}} + \frac{h_{V2\_M4}}{space_{AFing\_to\_KAccess_2}} + \frac{h_{V4\_M5}}{space_{AFing\_to\_KAccess_3}}\right) \quad \text{Equation 49}$$

In the same way, the second capacitive contribution of C_{access_finger} can be calculated as

$$C_{KFing\_to\_AAccess} = \varepsilon_0 \times \varepsilon_r \times W_{M1\_Cathode} \times (N_{Fing} - 1) \times \left(\frac{h_{M1\_M2}}{space_{KFing\_to\_AAccess_1}} + \frac{h_{V2\_M4}}{space_{KFing\_to\_AAccess_2}} + \frac{h_{V4\_M5}}{space_{KFing\_to\_AAccess_3}}\right) \quad \text{Equation 50}$$

It must be noticed that the calculated capacitance has just considered the capacitive contributions formed at the finger levels (between M1 – M5) since they are the closest metal stacks between the fingers and accesses. In fact, the capacitance formed between the Anode and Cathode accesses can also be included in the model. However, it just adds ~0.45 fF to the total calculation of C_{access_finger}, considering the anode surfaces explored in the preliminary BiCMOS 55 nm DOE presented in [41]. In conclusion, this contribution has not been considered in the model.

Also, we defined the third and last capacitive contribution from Equation 46. This capacitance C_{Bridge_N+} is formed between the anode/cathode bridges at M1 level (used to interconnect the fingers with the accesses) and the ohmic contact formed by the N+ implant. The total associated capacitance can be decomposed versus the anode and cathode bridges as follows:

$$C_{Bridge\_N+} = C_{Bridge\_N+\_Anode} + C_{Bridge\_N+\_Cathode} \quad \text{Equation 51}$$

where $C_{Bridge\_N+\_Anode}$ is the capacitance between the anode bridge and the N+ implantation, and $C_{Bridge\_N+\_Cathode}$ is the capacitance formed between the cathode bridge and the N+ implantation. Both capacitances can be calculated as follows:

$$C_{Bridge\_N+\_Anode} = \frac{\varepsilon_0 \times \varepsilon_r \times L_{N+\_OD} \times W_{M1\_Anode}}{h_{M1\_N+}} \times N_{Fing} \quad \text{Equation 52}$$

$$C_{Bridge\_N+\_Cathode} = \frac{\varepsilon_0 \times \varepsilon_r \times L_{N+\_OD} \times W_{M1\_Cathode}}{h_{M1\_N+}} \times (N_{Fing} + 1) \quad \text{Equation 53}$$

2.4.2.2 Total resistance Schottky diode modeling [41]

Based on the work presented in [41], it has been identified a fair accuracy between the analytical model and measurements in terms of the total series resistance. In consequence, no update is proposed initially for the resistance calculation. For a Silicon Schottky diode the series resistive contributions can be modeled as presented in Equation 54, considering the resistive path illustrated in Fig. 39 (b).

$$R_S = R_{Anode} + R_{Silicide} + R_{Nwell} + R_{N+} + R_{Cathode} \quad \text{Equation 54}$$

Based on the dimensions illustrated in Fig. 35 (b) and Fig. 38, the total resistance can be calculated taking into account the average current path between anode and cathode and the square. The equations for the calculation of the total series resistance are shown in the Table 5.

Parameter	Equation	Label
R_{Anode}	$\frac{L_{Access} + \frac{L_{Anode}}{2}}{\left(\frac{1}{R_{\square_{M1}}} + \frac{4}{R_{\square_{Mx}}}\right) \times W_{M1\_Anode} \times N_{Finger}}$	Equation 55
$R_{Silicide}$	$\frac{R_{\square\_Silicide} \times W_{Anode}}{2 \times L_{Anode}}$	Equation 56
R_{Nwell}	$\frac{R_{\square\_Nwell} \times (L_{Poly} + W_{Anode})}{L_{Anode} \times N_{Finger}}$	Equation 57
R_{N+}	$\frac{R_{\square\_N+} \times W_{Cathode}}{2 \times L_{Anode}}$	Equation 58

$R_{Cathode}$	$\frac{1}{\frac{W_{M1\_Cathode}}{R_{\square\_M1} \times \left(L_{Access} + \frac{L_{Anode}}{2}\right)} + \frac{N_{Contact} \times N_{Finger}}{R_{Contact}}}$	Equation 59

Table 5. Equations for calculation of total Schottky diode series resistance $\mathbf{R_S}$.

To apply the following equations, it is required the square resistance of each implantation and the metal levels where the current flows. The $R_{\square_{M1}}$ corresponds to the square resistance of the M1 level whereas the $R_{\square_{Mx}}$ parameter is the square resistance of the MiX levels (M2 to M5 in our case). $R_{\square\_Silicide}$, $R_{\square\_N+}$, $R_{\square\_Mx}$ and $R_{\square\_Nwell}$ corresponds to the silicide, N+, MiX and Nwell implantations and metal layers square resistances. A summary of these values can be found in Table 6 associated with the B55 technology.

$R_{\square\_Silicide}$	$R_{\square\_N+}$	$R_{\square\_Nwell\_min}$	$R_{\square\_Nwell\_typ}$	$R_{\square\_Nwell\_max}$	$R_{\square\_Mx}$
12 Ω/□	12 Ω/□	250 Ω/□	500 Ω/□	650 Ω/□	145,8 mΩ/□

Table 6. Square resistances for the analytical model.

2.4.2.3 Analytical model validation

To take profit of the previous analytical model of B55 Schottky diodes for SHM design, it must be validated from individual diode measurements. In fact, in [41] Schottky diodes in 9ML stack with the same BEOL illustrated in Fig. 34 (a) have been previously characterized via DC and S-parameters measurements. The parameters that have been variated in this DOE are illustrated in Table 7.

#	N_{Fing}	$W_{anode}(\mu m)$ layout	$L_{anode}(\mu m)$ layout	S (μm^2) layout	$W_{anode}(\mu m)$ shrinked	$L_{anode}(\mu m)$ shrinked	S (μm^2) shrinked
1	2	0.31	3.23	2	0.28	2.91	1.6
2	4	0.31	3.23	4	0.28	2.91	3.2
3	4	0.31	6.45	8	0.28	5.81	6.5
4	8	0.31	6.45	16	0.28	5.81	13.0

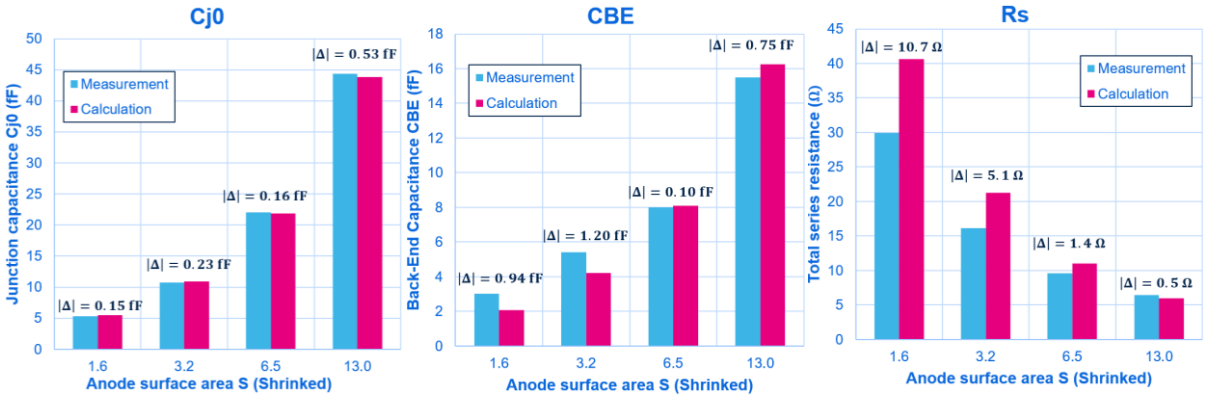
Table 7. DOE of B55 Schottky diodes previously measured.

With S-parameters measurement at zero bias, and by using open structures for de-embedding, the extraction of junction capacitance C_{j0} and back-end capacitance C_{BE} is realized. Moreover, with DC sweep, the forward voltage V_B can be extracted. More details on the extraction methods can be found at [41]. Having these extracted parameters, one can calculate the doping profile at the Schottky junction by the following equation:

$$N_D = \frac{C_{j0}}{S^2} \times \frac{2V_b}{q\varepsilon_s} \qquad \text{Equation 60}$$

q corresponds to the electron charge and ε_s to the Silicon dielectric constant in the technology ($\varepsilon_s = 10^{-10}\mathrm{F.m^{-1}}$). For these DOE, an average of $N_D \approx 9 \times 10^{23}\mathrm{cm^{-3}}$ has been extracted. With the other extracted parameters and by using Equation 45, one can calculate the junction capacitance based on the analytical model. In the case of the back-end capacitance C_{BE}, it can be calculated directly by the previous equations presented in section 2.4.2.1. We must consider that $\varepsilon_r = 4$. In the same logic, we calculate the series resistance

from the equations from section 2.4.2.2. However, in the context of [41], some brief modifications have been made to the series resistance model presented in 2.4.2.2. to improve the match with measurements in B55 technology. The final comparison between the measurements and the analytical model is illustrated in Fig. 41.



(a) (b) (c)

Fig. 41. Comparison of measurements and analytical model results to obtain (a) C_{j0}, (b) C_{BE} and (c) R_S.

We can notice that firstly, the model match well in terms of the junction capacitance C_{J0}, with an achieved difference between measured and calculated C_{j0} below 0.53 fF. By the other hand, in terms of the back-end capacitance C_{BE} we can notice that the agreement between measurements and calculation is acceptable considering an error margin of $\pm$ 1 fF (due to measurements). In fact, we achieve a difference below 1.2 fF for the four studied diodes. Finally, the series resistance is calculated based directly on the adaptation of the equations from Table 5. We can notice that the models struggle to reproduce the measured series resistance for small anode areas (assuming an acceptable difference between measurements and calculations of ~5 Ω). However, the model is considered acceptable since in practice the SHM will not work at small anode areas since it leads to an important series resistance thus increasing the conversion loss.

2.5 W-band SHM Demonstrator in BiCMOS Technology

2.5.1 Model validation via previous SHM design

In this section, we propose to evaluate first the validity of the updated model in a previously designed W-band SHM [41]. Second, a preliminary re-optimized SHM at the same frequencies is illustrated. The choice of architecture is the one presented in Fig. 22 (a), which as mentioned before, is one of the most used architectures for MMICs. The final architecture is illustrated in Fig. 42. The circuit has been simulated in ADS using harmonic balance analysis, with an RF frequency of 92 GHz and a LO frequency of 45 GHz, leading to an IF frequency of 2 GHz. The LO power P_{LO} has been optimized to 2.7 dBm and RF input power $P_{RF} = -2.5$ dBm.

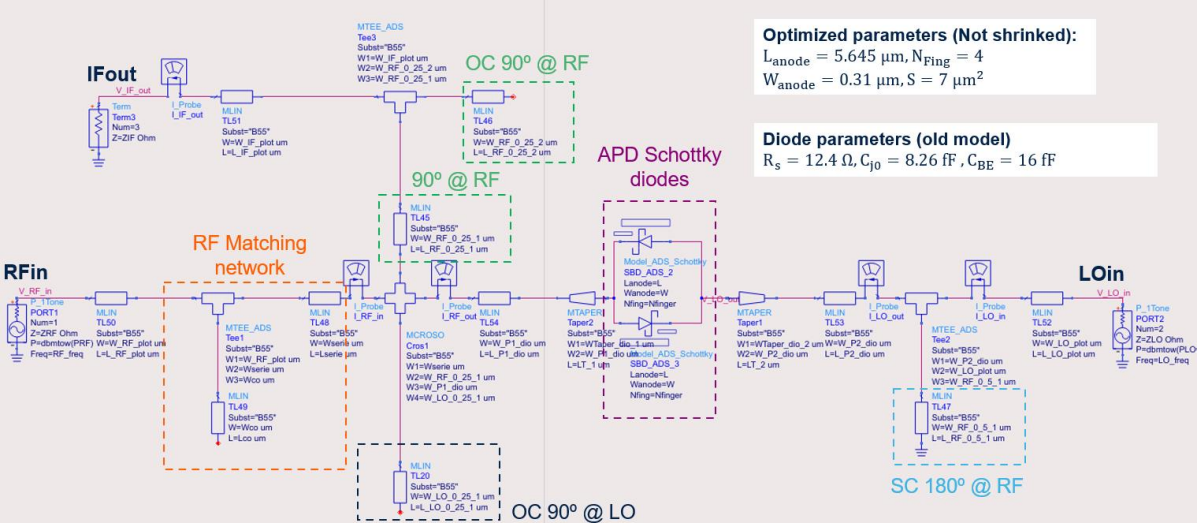


Fig. 42 Preliminary W-band SHM design in [41].

Firstly, we can identify the short-circuited (SC[8]) and open circuit (OC) stubs, typical from this type of architecture, as illustrated in Fig. 22 (a). As mentioned before, the first 180° OC stub is used to avoid RF leakage into the LO port and the 90° OC stub to avoid leakage into the RF port. In the same logic, after the IF port, a 90° transmission line as well as an OC 90° at RF frequency are placed to avoid leakage of the RF input signal into the IF port. In addition, it must be noticed that the best conversion loss that can achieve the SHM is conditioned to the optimal impedances presented to the diodes at RF, LO and IF frequencies. However, in practice, to present those impedances it will be required to use multiple matching networks at each input port, which will lead to a more complex circuit. Moreover, it is conditioned by the possible synthesizable impedances of the technology. Therefore, a tradeoff must be found.

In [41], just the optimal RF impedance is presented to the diodes thanks to an impedance transformer since the required LO and IF frequencies are not synthesizable by the technology. Finally, the transmission lines which are not enclosed in dotted squares correspond to the access lines. For simulations, microstrip lines have been used. The circuit has been integrated in a 9ML B55 technology, with expected performances (simulated) in Fig. 43. To calculate the conversion loss, Equation 22 has been used.

[8] Do not confuse with semiconductor (SC) abbreviation

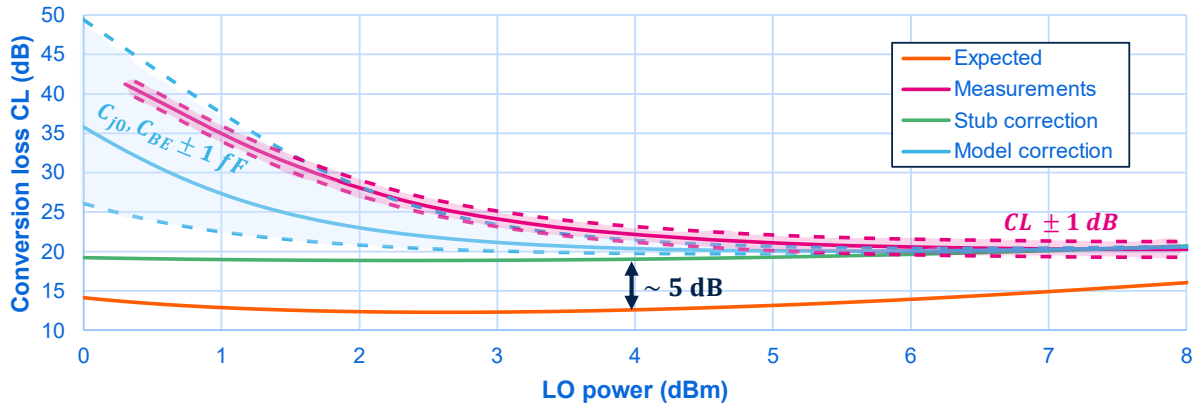
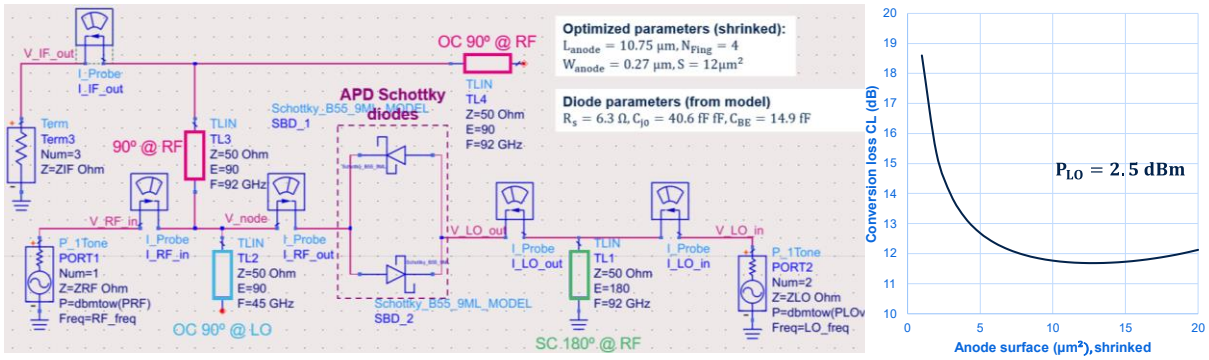


Fig. 43. Conversion loss in function of LO power for the preliminary SHM in [41] with the associated stub and model corrections made in this thesis.

However, we notice that the expected simulated performances do not match with measurements. In the context of this thesis, the real causes of mismatching have been studied. Firstly, we found a layout error in terms of the position of the stubs. By retrosimulation, we found that by considering this effect, the agreement between simulation and measurements is improved, but the preliminary model struggles to reproduce the behavior at low LO power input. Since the predominant intrinsic element at low diode biasing in the junction capacitance C_{j0} (as illustrated in Fig. 30 (b)), a first insight leads to explore the model capacitive contributions. In fact, by using the updated capacitive analytical model, we achieve to further match the measurements and simulations at LO power. Moreover, if we consider the error associated with the extraction of C_{j0} and C_{BE} capacitances in measurements ($\pm$ 1 fF for each one), one can obtain a large confidence interval which encloses the expected conversion loss performances at low LO power. These facts highlight the sensitivity of the SHM to the value of capacitive contributions from the Schottky diodes at low LO power. However, it is not a point of concern since the expected LO power level are out from this power region (> 3 dBm). This will be validated by state-of-the-art SHMs presented in chapter 4.

2.5.2 Preliminary W-band SHM design

As seen before, the updated analytical model has been validated by verification with the extracted diode parameters and also with retrosimulations of previous W-band SHM design. In this logic, we propose to design a new W-band SHM following the same design flow presented in [41]. Firstly, based on this updated model, one can optimize the anode surface and the injected LO power to find the lower conversion loss due to the APD diode configuration. However, to quantify this conversion loss, an ideal circuit setup must be made to route the RF and LO signals into the diode and extract the IF signal. The ideal setup implemented in ADS simulator is presented in Fig. 44 (a).



(a) (b)

Fig. 44. (a) Ideal W-band SHM circuit (b) Diode anode area optimization for a given optimized LO power.

In this simulation setup, just ideal transmission lines (TLIN) are used. The only elements that have been considered compared to the previous structure in Fig. 42 are the RF diplexer, the LO OC stub, and the RF SC[9] stub. The transmission lines accesses are not included. The anode surface is swept (by varying the anode length L_{anode}) as well as the LO input power to find a tradeoff between both parameters. The RF frequency is set to 92 GHz and the LO frequency to 45 GHz, leading to an IF frequency of 2 GHz. The RF input power P_{RF} is set to -2.5 dBm. In the end, an optimal anode surface of 12 µm² and LO power P_{LO} of 2.5 dBm has been found, as illustrated in Fig. 44 (b). This leads to a conversion loss of 11.7 dB.

Based on the optimized anode surface and LO power, one can lead a second optimization in terms of the impedances presented to the APDs at RF, LO and IF frequencies. In fact, the lowest conversion loss can be achieved by finding these optimal impedances. In Fig. 45, conversion losses are plotted with all the ports impedances at 50 Ω and to the respective optimal impedances. The values are presented in Table 8. We can notice that with the optimized port impedances we achieve optimal conversion loss of 7.3 dB when a LO power of 2.82 dBm is applied.

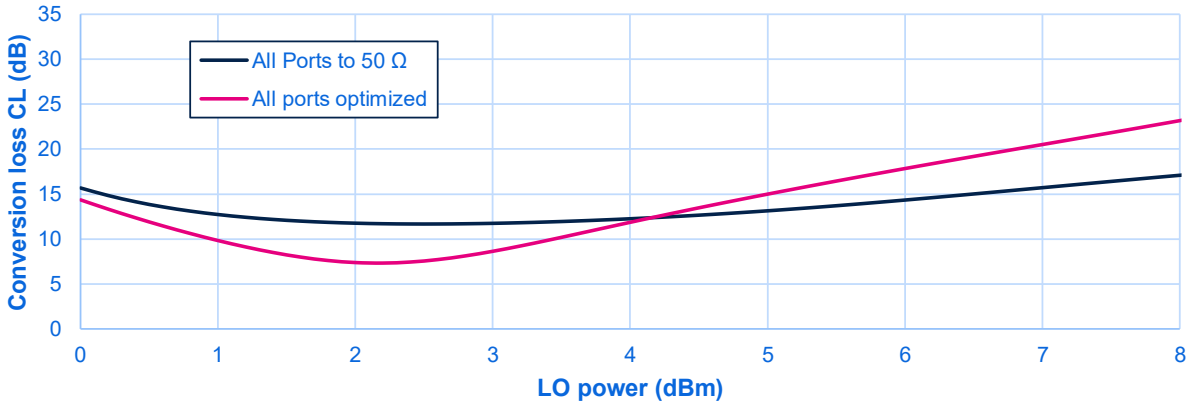


Fig. 45. SHM conversion loss vs LO power for different impedances at RF, LO and IF ports.

[9] Do not confuse with semiconductor (SC) abbreviation

Configuration	$Z_{RF}[\Omega]$	$Z_{LO}[\Omega]$	$Z_{IF}[\Omega]$	$P_{LO}(dBm)$
All ports to 50 Ω	50	50	50	2.50
All ports optimized	17.0 – j51.6	27.9 + j42.3	22.6 + j16.5	2.82

Table 8. Port impedances used for the optimization of conversion loss.

Although the new W-band SHM design will enable the complete validation of the updated model, the following of the circuit design has not been pursued since a strong energy has been lead in this thesis to enable packaging solutions and SHM design above 200 GHz, as will be illustrated in chapter 3 and 4.

2.6 Conclusions & Perspectives

In this chapter, a first vision of the SHM has been given by explaining the principle of operation compared to a fundamental mixer. Moreover, the non-linear element that generated the desired harmonics, which is the diode in antiparallel configuration has been presented doing a focus on its advantages compared to a fundamental single Schottky diode SHM. The type of diode that is used is the Schottky diode thanks to high switching speeds and low forward resistance compared to other types of diodes. In this order, the Schottky diode is presented and described in function of its energy diagram bands and its figures of merit.

Moreover, the evolution of the Schottky diode architectures in III-V and Silicon technologies is presented. This leads to the presentation of the FEOL and BEOL of the Schottky diodes that will be explored in this thesis integrated in 9ML B55 and B55X Silicon technologies. In this chapter, just the architecture in B55 technology is used. Based on the presented Schottky diode architecture, an updated analytical model focusing on the modeling of the junction capacitance C_{j0} and back-end capacitance C_{BE} is presented. The model has been validated firstly by the comparison between the extracted parameters from previous DOE in B55 technology. In fact, the difference between measured and modeled C_{J0} and C_{BE} is just of ± 1 fF that seems acceptable considering the measurements error. At a second time, the model has been validated via the retrosimulation of a W-band SHM designed and fabricated in [41]. Considering the associated measurement error and the layout stub corrections, a fair agreement between simulations and measurements of the conversion loss is achieved, leading to promising performances for the design of a new W-band SHM with expected optimal conversion loss of 7.3 dB (assuming an ideal circuit).

Chapter 3
Innovative Packaging Solutions for Silicon Circuits Operating above 200 GHz

3.1 The RF & mmW Package Technology

We define electronic packaging as the interface between the core devices and the electronics' system, providing at the same time physical support and protection to environmental loads such as humidity, heat, electromagnetic interference, and thermomechanical stress [101], [102], [103]. For mmW and lower frequency packages, the core device consists generally of the integrated circuit (IC) chip. Fig. 46 Illustrates a conceptual relationship between the package and the core device. Between the IC and the outside, there are interconnections that allow the core device to interact with the exterior using Input/Output (I/O) ports for signal, monitoring and bias, which are embedded in the package.

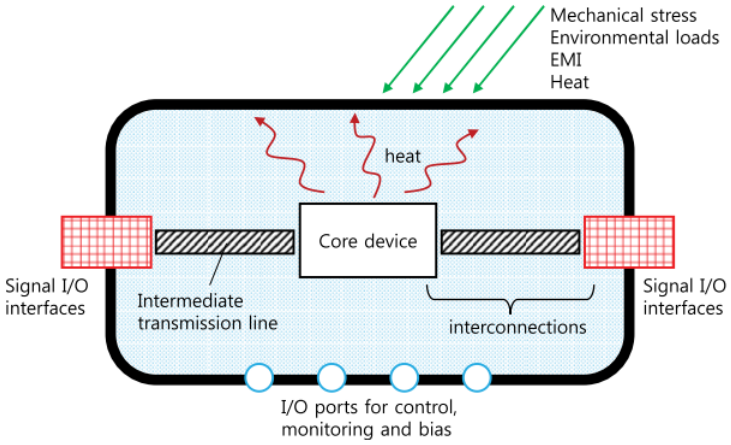


Fig. 46. Conceptual schematic of package. Taken from [101].

The most traditional packages for a simple chip are lead-frame packages. The fabrication flowchart of this type of packages is illustrated in Fig. 47 for a Silicon IC. The flow starts from a Silicon wafer containing multiple IC chips, then the wafer is diced while cutting all IC chips separately. The Silicon chip is then extracted from the diced wafer and attached to the lead-frame using a die-attach adhesive which can be electrically conductive or insulative. After attachment, the chip is wire-bonded to the leads and encapsulated into an epoxy molding compound. Finally, the excess lead material is trimmed and shaped to the desired final mounting (type of pins), as illustrated in Fig. 48.

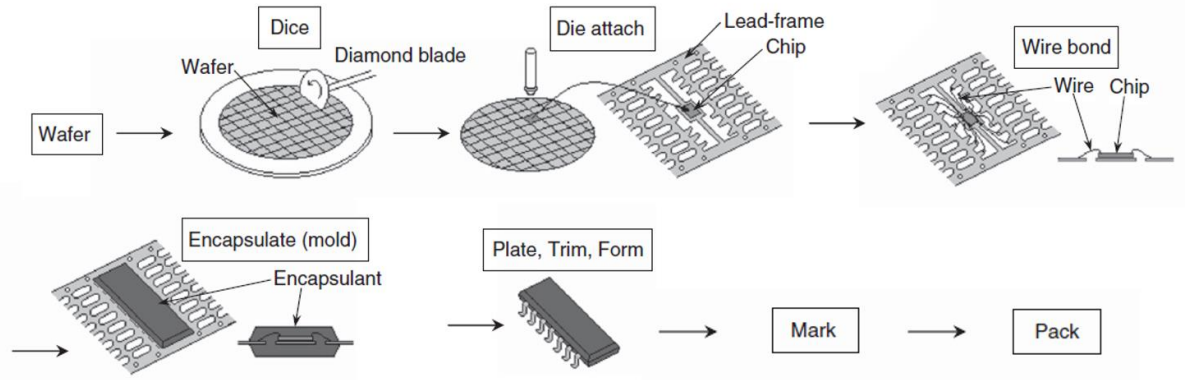
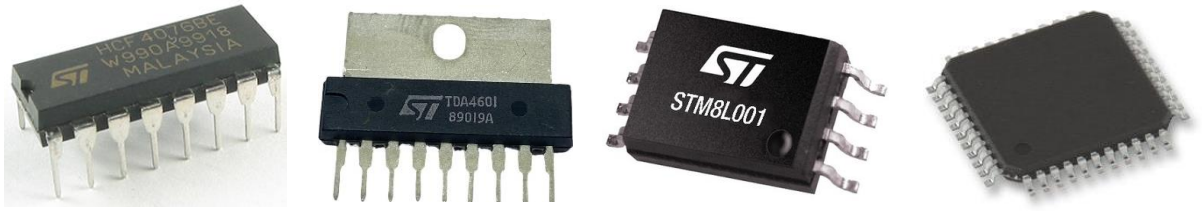


Fig. 47. Plastic package assembly flowchart. Taken from [102].

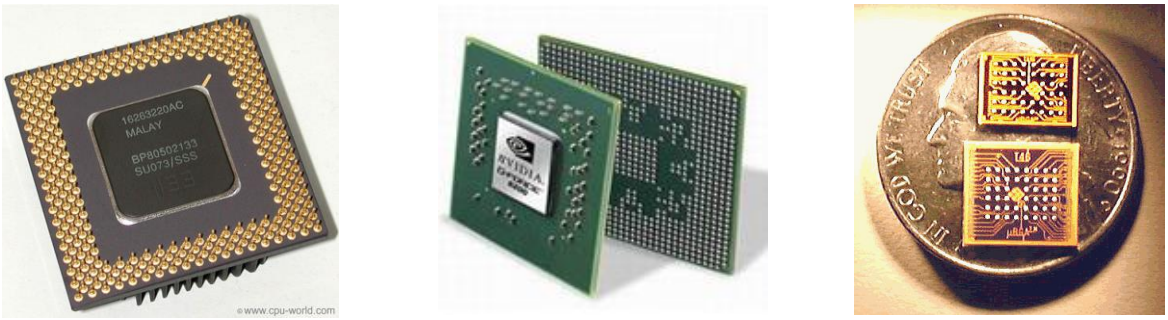


(a) (b) (c) (d)

Fig. 48. Single-chip lead-frame packages: Through-hole (a) dual in-line package from [104], (b) single in-line package from [105], and surface-mounted (c) small outline package from [106] and (d) quad flatpack package from [107].

For through-hole mounting, as illustrated in Fig. 48 (a), (b), the printed circuit board (PCB) must be drilled and platted making the manufacture of the board more expensive. An alternative is the use of surface-mounting technology where the package is surface soldered to the board. The use of this technology allows smaller package size compared to through-hole technology increasing package density. However, for both solutions, if I/O pins need to be increased and since the pins are placed in the periphery of the package, it will require the increment of the surface area of the package which is not used for interconnections. One possible solution is to place the pins on the bottom surface of the package. This type of package can be achieved by replacing the lead frame with a substrate.

One of the first package technologies following this strategy was the Pin Grid Array (PGA) package. Thanks to 100 mil pitch pins distributed in the bottom of substrate, PGA increase the I/O pins density compared to lead-frame packages. However, to be attached to the board, through-holes must be made, or sockets must be integrated. In consequence, the cost of manufacturing increases to accommodate the package. That is why the Ball Grid Array (BGA) package has been introduced as an alternative to replace the pins with solder balls. This type of package is compatible with surface-mounting and achieves a higher number of I/O interconnections compared to PGA thanks to smaller pitch (typically around 20 mil). Both mentioned packages are illustrated in Fig. 49 (a), (b).



(a) (b) (c)

Fig. 49. Some area-array single-chip packages examples. (a) PGA with ceramic substrate package from [108], (b) BGA with organic laminate substrate package from [109] & (c) µBGA package from [110].

Furthermore, a smaller version of the BGA package has been developed (the µBGA) following the rule of Chip Scale Package (CSP), where package is not larger than 1.2 times the area of the die. With this technology, interconnections pitch below 400 µm can be achieved. This package is illustrated in Fig. 49 (c).

Single-chip package strategy is suitable for System-on-chip (SoC) configuration when the complete system is integrated on a unique chip. However, RF design generally requires a diversity of technologies (Silicon, III-V, etc.), and consequently multiple dies which makes System-in-Package (SiP) configuration a more suitable alternative. The evolution of system integration in package is illustrated in Fig. 50.

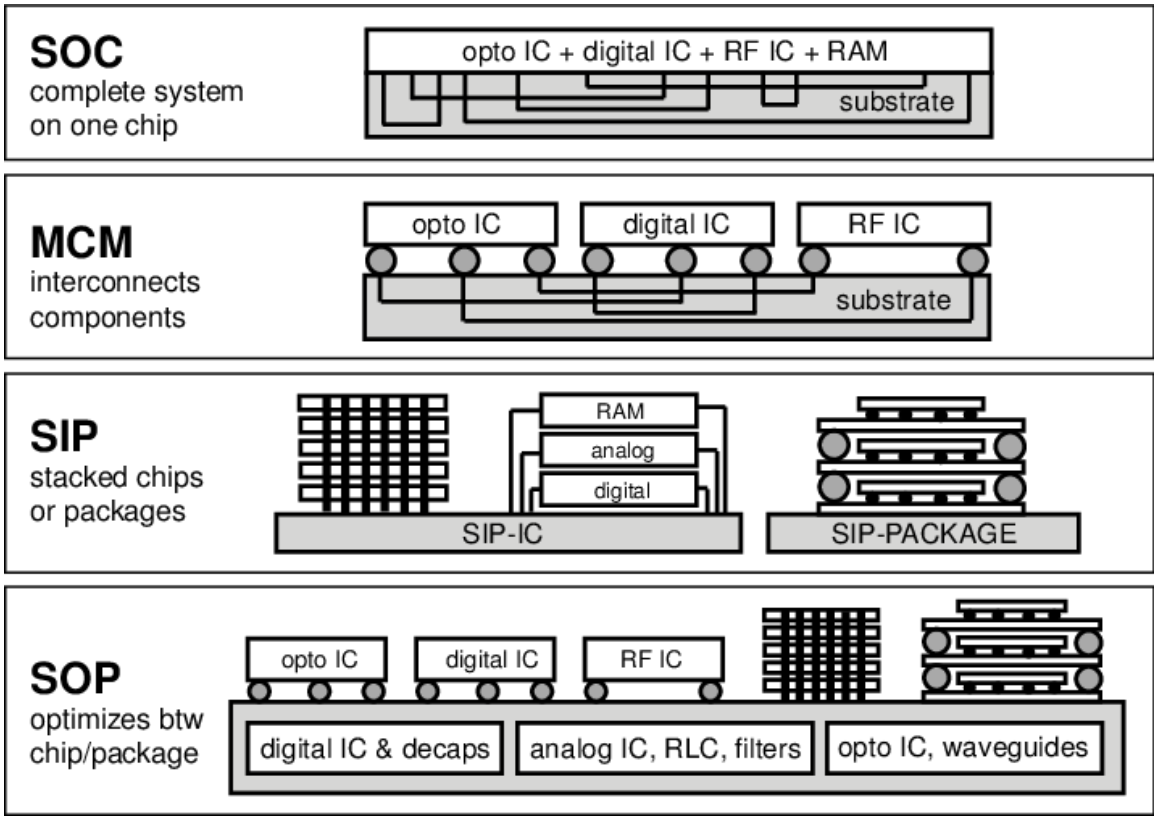


Fig. 50. Comparison of System on Chip (SoC), multichip modules (MCM), System in Package (SiP) and System on Package (SoP). Taken from [111].

One of the first solutions is to simply attach different ICs into the same package following a 2D X-Y common plane, resulting in a multichip module (MCM). The substrate serves as an interface to interconnect the ICs between them. However, the ongoing demand to increase functionality within the smallest absolute possible volume drove the generalization of 2D package to 3D, taking advantage of Z-axis. This opens the possibility to stack multiples ICs vertically thanks to 3D ICs technology using through-silicon via interconnections and ultimately to stack multiple packages. These approaches are known as system-in-package (SiP). Same as MCM approach, the substrate is used to interconnect the other blocks attached over it.

Nowadays, with the demand of more complex system integration and miniaturization, the potentialities of package are exploited by the integration of, for example, passive functions

such as filters, waveguides and antennas, and even thermal cooling mechanisms inside the package. With the System-on-package (SoP) approach, the package substrate is not only used as an interconnection interface but as an integral element to develop internally diverse passive devices, as illustrated in Fig. 50.

3.1.1 RF package substrate overview

As noticed previously, most of the ICs are attached over a substrate, which are used mainly as interface of interconnection between the functional blocks of the package or even more for the integration of other functionalities. Three main families are identified for rigid substrates: Glass substrates, ceramic substrates, and organic laminate substrates.

On one hand, glass substrates are mainly composed of Silicon Oxide/Silica (SiO2). These substrates can be found in their borosilicate form, also as fused silica [112] or even in their natural form (quartz). In fact, thanks to its high insulator properties and low dielectric constant Dk, as well as low loss tangent Df, it is an interesting material for passive devices such as integrated passive devices (IPD) [113]. Nowadays, glass substrates have attracted interest as interposers for 3D Integration and 2.5-D Through Silicon Via (TSV) package thanks to reduced warpage compared to organic substrates [114], [115]. In fact, this material is being recently exploited by companies such as Intel [116]. Although the raw material cost is low, associated processing increases notably the cost of this kind of package [113].

On the other hand, ceramic substrates are mainly made using alumina (Al2O3) or aluminum nitride (AlN). A common type of ceramic is the Low-Temperature Co-fired Ceramic (LTCC). Ceramic materials are interesting thanks to their high hermeticity and thermal conductivity, leading to being widely used for harsh outdoor environments such as military applications. However, due to their cost, nowadays they are mainly used for specialized low-volume and high-performance applications [102].

Finally, there is also the organic laminate substrate, which is presented in Fig. 51.

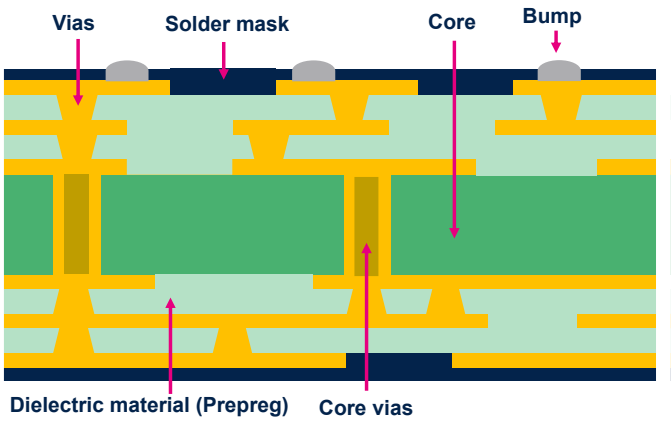


Fig. 51. Cut-view of an organic laminate substrate build-up.

This type of substrate is composed of multiple stacked layers of woven glass/epoxy dielectrics such as FR-4 materials, Bismaleimide-Triazine (BT) epoxies or specialized films

such as Ajinomoto Build-Up Film (ABF) [117]. The central dielectric, also called core, is enclosed in a copper clad laminate (CCL), serving as seed element to place the other dielectric layer at the top or the bottom of the core (which imposes a symmetrical build-up with an odd number of layers). The core can be found at a large variety of thickness options, even as small as 30 µm [118]. At the top and bottom of the core, more dielectric layers called prepreg (pre-impregnated) are placed. Moreover, thanks to possible prepreg thickness as aggressive as 15 µm [118], a multiple variety of total substrate thicknesses can be found, and high density routing of metal traces (thanks to aggressive design rules) can be achieved. Concerning metal layers, common thickness around ½ oz (18 µm) or 1 oz (36 µm) can be found [103]. For some applications where total thickness is critical, coreless substrates can also be fabricated (generally leveraging ABF material). The detailed fabrication of an organic substrate is illustrated in Fig. 52.

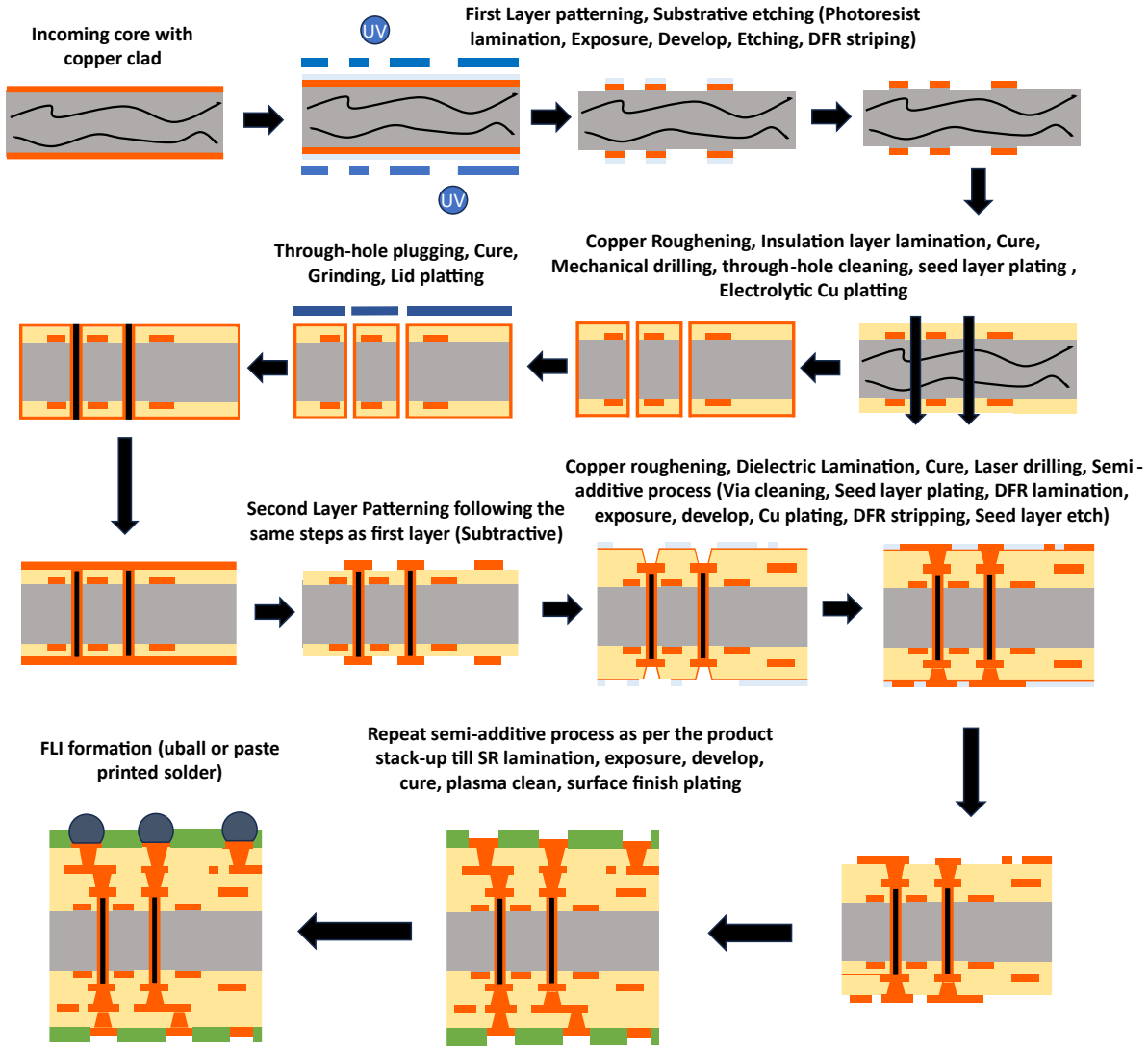


Fig. 52. Process flow to fabricate an organic laminate substrate. Adapted from [103].

First, the desired core and prepreg dielectrics are chosen in function of the desired application (high speed, high reliability, high power, etc.). After considering this aspect, the fabrication

of the organic substrate is started. The CCL core is covered at both sides by a photosensitive resist. Then, a film with the desired artwork is placed over the core and exposed to ultraviolet light (or Laser Direct Insulation can be used to realize the artwork). After that, the unexposed resin is rinsed away, and the exposed copper is etched, leading to the desired metal patterns. Finally, the remaining resin is retired, and the remaining metal is chemically prepared for the prepreg multilayer integration [103].

The top and bottom prepreg layers are then bonded to the core material by high-temperature vacuum press. In function of the lamination step, the interconnecting vias are fabricated by mechanical or laser drill. After the holes have been cleaned from the remaining debris of the drilling process, the metal patterns are imaged following the same process as for the CCL core etching. The only difference is that an electroless copper seed is deposited and then an electrolytic plating is made to achieve the desired metal thickness. The process is repeated until the desired quantity of metal layers is achieved. Finally, solder mask is applied, exposed, and cured at the top and bottom side of the substrate [103].

To protect the exposed top and bottom metal pads from environmental deterioration such as oxidation, and to facilitate the wirebond and soldering of components, a surface finish is made over the exposer copper. Some of the commonly used surface finishes are presented in Fig. 53.

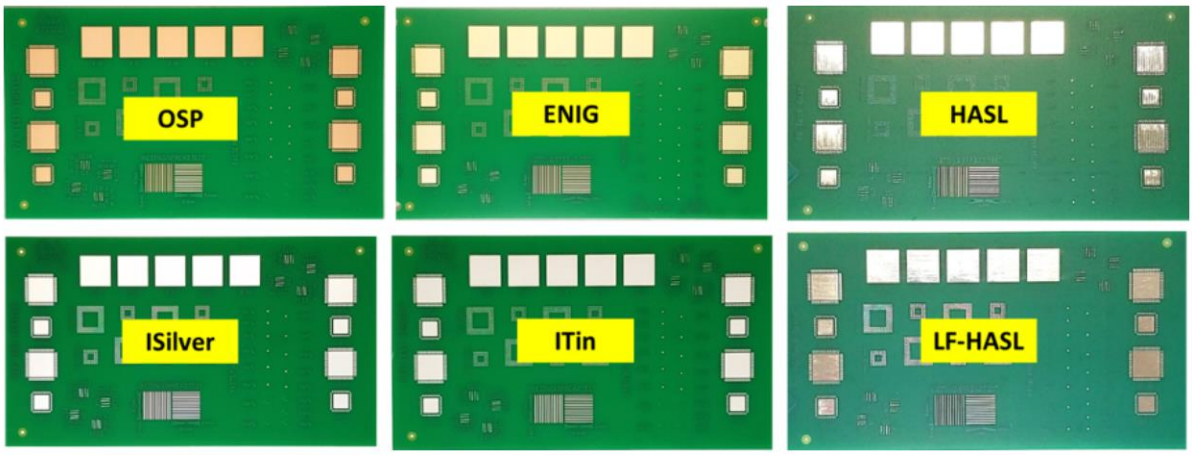


Fig. 53. Somme commonly used surface finishes. Taken from [119].

The Organic Solderability Preservative (OSP) method bonds a water-based organic compound over the bare copper surface, providing an organo-metallic protection layer. This finish is known to be more environmentally friendly in comparison with other surface finish options thanks to either being less toxic or to consume less energy in fabrication. In terms of planarity, this finishing is interesting but with less robustness compared to the other following options [120], [121].

For the Hot Air Solder Leveling (HASL) surface finishing, the circuit board is submerged in a molten tin/lead alloy and then the alloy excess is removed, and the remaining solder is leveled by blowing hot air over the surface of the board. One advantage of this solution is that is cost-effective, however, the resulting surface is not completely plain, making it difficult the

assembly of certain surface components. Another inconvenience is the use of lead, leading to a circuit board incompatible with the Restriction of Hazardous Substances (RoHS) normative. To solve this, pure tin or tin/copper or tin/silver/copper alloys are used, resulting in a Lead-Free HASL finishing [120], [121].

Also, immersion finishings can be found such as the immersion Tin (ITin) process. Here, the Tin finishing is deposited by a chemical displacement reaction over the copper metal. Moreover, immersion silver (ISilver) can be used when less finish thickness is required compared to ITin. Here, the copper board is submerged into a tank of silver ions [120], [121].

Moreover, the Electroless Nickel Immersion ENIG is a two-layer metallic coating of gold over nickel. The first nickel layer acts as a diffusion barrier to the copper, and it is the layer where the soldering occurs. This layer is applied via autocatalytic process, and then recovered by a thin gold layer deposed by immersion. The gold layer serves as protection for the nickel and provides at the same time low contact resistance. Nowadays, it is one of the most used finishing for circuits boards thanks to their alignment with the RoHS regulation. However, this surface finishing could result in unwanted ‘‘Black Pads’’ when the process is not controlled properly, leading to corrosion of the gold in the nickel, reducing the rate of solderability. By placing a middle palladium layer this problem can be solved, leading to an Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG) surface finishing [120], [121].

Finally, a circuit board can also be finished by Hard Gold plating, where a layer of gold is placed over a coat of nickel. This solution differs from ENIG finishing since the gold layer thickness can be controlled [120], [121]. Even though gold is one of the most expensive surface finishing, it is one of the favorites for robust applications when temperatures are lower than 150°C. In the end, when the surface finishing is applied to the board regarding the desired applications, the final organic laminate substrate passes reliability tests before being delivered as the final product.

In this thesis, special attention will be made to the organic laminate substrate to be aligned by the proposition on cost-effective packaging solutions. In fact, this packaging solution has been widely used to support large manufacturing volumes, reducing notably the costs of the final substrate. In Table 9 a comparison of the three types of substrates mentioned in this section is given versus their electrical performance and prices.

Parameter	Organic laminate substrate	Glass substrates	Ceramic substrates (LTCC)
Dielectric constant Dk	3.5 - 4.9	4.7 - 5.3	3.8 - 9.2
Loss tangent Df	0.002-0.012	0.006-0.011	0.0007-0.006
Coefficient of thermal expansion CTE (ppm/°K)	12-16 (FR4)	3.0 - 9.8	4.7 - 7.5
Thickness	Large variety	25 - 1000	20 - 100 per layer
Min. Width/Space (µm/µm)	6/6	15/15	76/76
Min. Via diameter (µm)	20	40	102

Cost	-	++	+

Table 9. Comparison of the 3 types of substrates found in literature [76], [118], [122], [123], [124] .

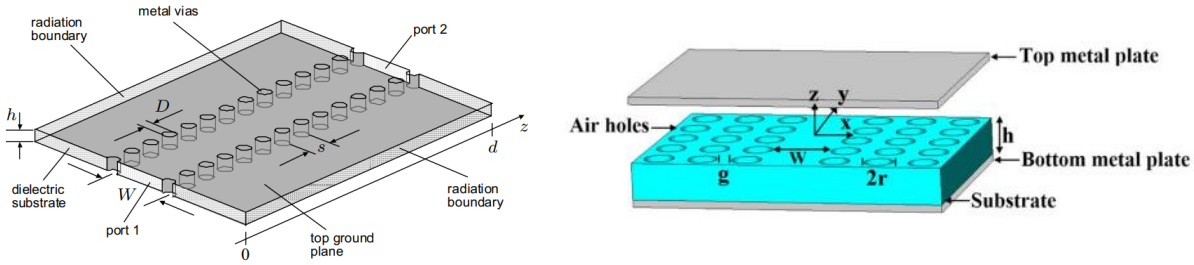
We can notice that in terms of dielectric constant values, all presented solutions are comparable considering achievable low dielectric constant values. However, we can notice that organic substrate seems to take the lead in terms of aggressive design rules and cost. As an example, in previous work [76], a price of $ 500 have been estimated for 8000 pieces (2 panels) of a two-layer organic substrate. As a comparison, an equivalent-size quartz substrate costs $1335 for 50 pieces. If we compare by unitary price, an organic substrate cost $0.07 compared to $27 for a quartz substrate [76].

In conclusion, in this section, three types of materials have been presented as reported packages for circuits working below ~20 GHz. However, certain limitations will be found in the packaging technology when frequency increases, especially in terms of interconnections. This will be discussed in the next section.

3.1.2 Pushing RF package's technology at higher frequencies

Usually, the problem concerning the increase in frequency on package technologies has been aborded by scaling the traditional packaging techniques used at RF frequencies. Concerning interconnections, wirebond geometry, such as diameter, loop height and length is modified to reduce the associated inductance which can cause significant reflections at high frequencies. In fact, with proper scaling, wirebond can work up to 300 GHz. Even more, wirebonds can be interconnected in parallel to reduce their inductance. Another attractive interconnection technique is the use of flip-chip bonding, thanks to low-parasitics associated to pillar bumps. However, for THz frequencies, the substrate of the IC must be thinned (in the case of technologies where the ground is below the substrate), in order to avoid substrate mode excitation. The more the substrate is thinned, the more complicated it is to avoid the cracking of the wafer during flip-chip process. To avoid this, a shielding pad can be included (allowing a thicker substrate) but it will increase the parasitic capacitance of the pads [101], [125].

Concerning the interfaces between the IC and the exterior of the package module, planar transmission lines such as coplanar waveguides and microstrip lines are not suitable solutions for routing at THz frequencies. In fact, when the frequency increases, the mentioned planar transmission lines can be scaled to the desired frequency for IC internal routing leading to manageable Insertion Loss (IL) [125]. However, in package routing, the distances between components (inside the package) are much larger due to required standard package interfaces. Consequently, other alternatives such as non-planar structures are explored to achieve lower-loss routing at package level while retaining at the same time the benefits of planar transmission lines such as compactness and ease of integration.



(a) (b)

Fig. 54. (a) Substrate Integrated Waveguide description from [126]. (b) Substrate integrated non-radiative dielectric waveguide description from [127].

A type of non-planar transmission line is the Substrate Integrated Waveguide (SIW), which is basically the synthesis of rectangular waveguides for standard PCB or other planar integration technique. The mentioned structure is illustrated in Fig. 54 (a). SIWs are fabricated using two densely-periodic arrays of metallic vias which replace the metallic sidewalls to enclose the electromagnetic field as in conventional rectangular waveguides. However, the EM field is guided through a dielectric substrate which is enclosed in a top and bottom metallic ground. The main advantage of this solution is its simple fabrication process and ease of integration with ICs and other components in a single substrate. However, in contrast to conventional waveguides, SIW suffers from dielectric losses (due to filled waveguide) and radiation losses (since the waveguide is not completely shielded by vias). Moreover, at high mmW and THz frequencies, SIWs also suffers from high conductor losses [126], [128].

On the other hand, nonradiative dielectric (NDR) waveguides were proposed. This solution consists of an enclosed dielectric slab into two metallic plates. Moreover, NDR waveguides exhibit low conductor losses while operating in longitudinal section magnetic (LSM) mode, which leads to an interesting solution for THz routing. To synthetize these waveguides in a planar conventional integration strategy, the substrate is filled with air holes by laser drilling in the regions where the dielectric material is not desired. This leads to the Substrate integrated NDR (SINDR) waveguide configuration illustrated in Fig. 54 (b). Compared to SIWs, SINDR waveguides get rid of the metallization process, being a critical factor to achieve competitive mmW and THz circuits. This type of configuration has demonstrated measured total losses of ~3.5 dB compared to SIW with ~5.5 dB losses at 300 GHz [127], [128]. In conclusion, although a special effort has been made to propose low-losses non-planar transmission lines at mmW and THz frequencies, rectangular waveguides continues to lead as a routing strategy at THz frequencies [101], [125].

3.2 THz Package Technology State-of-The-Art

3.2.1 Traditional THz packaging technology: the metallic split-block package

Historically, most ICs working at mmW, and THz frequencies are packaged in metallic split-blocks modules [125]. These blocks are fabricated separately using CNC machining technology, where they are drilled creating the desired cavities. The most common used metals are aluminium and brass. An example of a fabricated metallic split-block module for a 664 GHz SHM is illustrated in Fig. 55. The IC is attached manually to one of the splitted blocks with epoxy glue. This method allows the fabrication of rectangular waveguides, which are splitted generally following the peak of the E-field inside the waveguides. Splitting the metal blocks (and waveguides) in this way reduces the losses due to current leakage across the split plane and simplify the machining of waveguides and other cavities (such as feedhorn antennas) respecting the fabrication aspect ratios. Finally, alignment pins are used to orient both blocks when they are enclosed. Enclosing led to the high-frequency (waveguide flange) transitions for external interconnections.

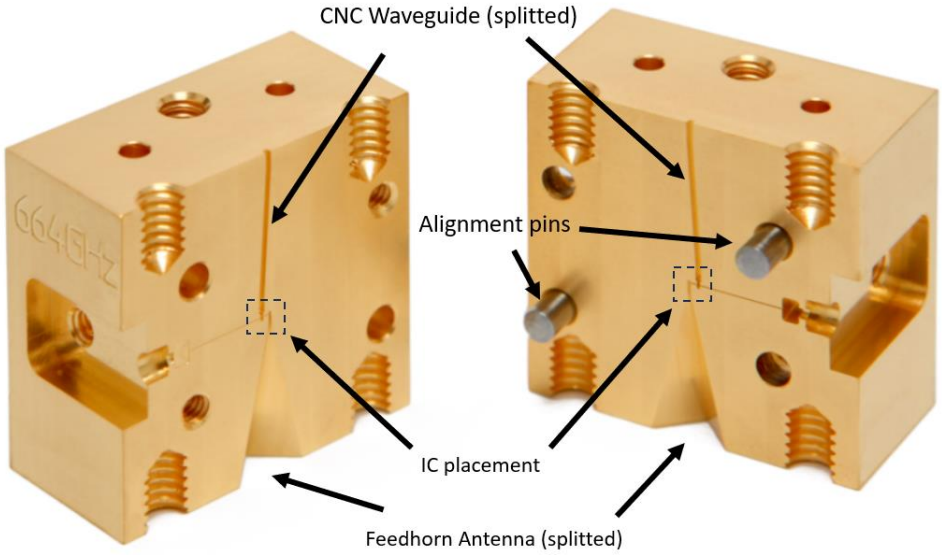
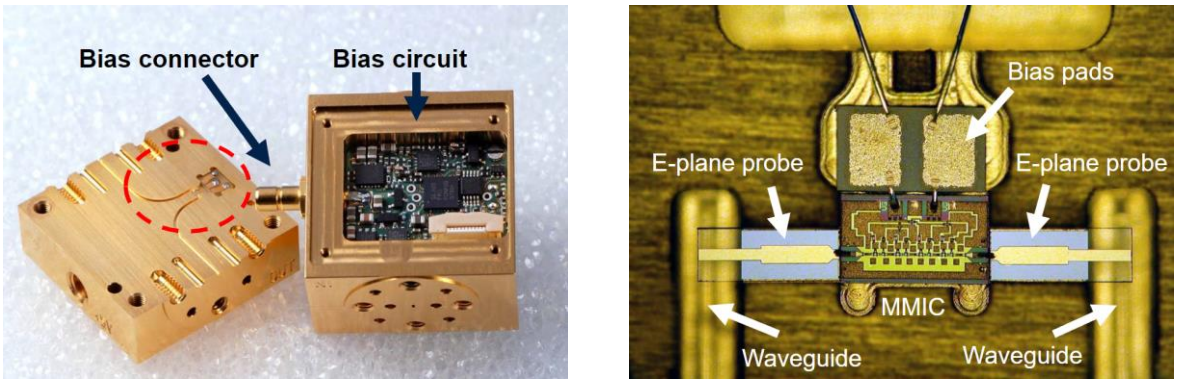


Fig. 55. Metallic split-block package for a 664 GHz GaAs SHM. Taken from [75].

The use of waveguide routing has the advantage of lower wave's path loss and higher power handling compared to conventional planar transmission lines routing [125]. Moreover, with recent advanced milling machines and micro tooling, as well as software improvements, 5 µm wide channels and aspect ratios higher than 10:1 are now possible, allowing waveguide machining to operate at frequency as high as 4.7 THz [129]. Another advantage of metallic split-blocks is the ease of device integration with rectangular waveguides [125]. In a E-plane metallic split-block, E-probe transitions are the favourites to couple the waveguide to planar transmission lines thanks to their wideband performance and simplicity [125], [130]. However, special attention must be given to the E-probe substrate material, thickness and

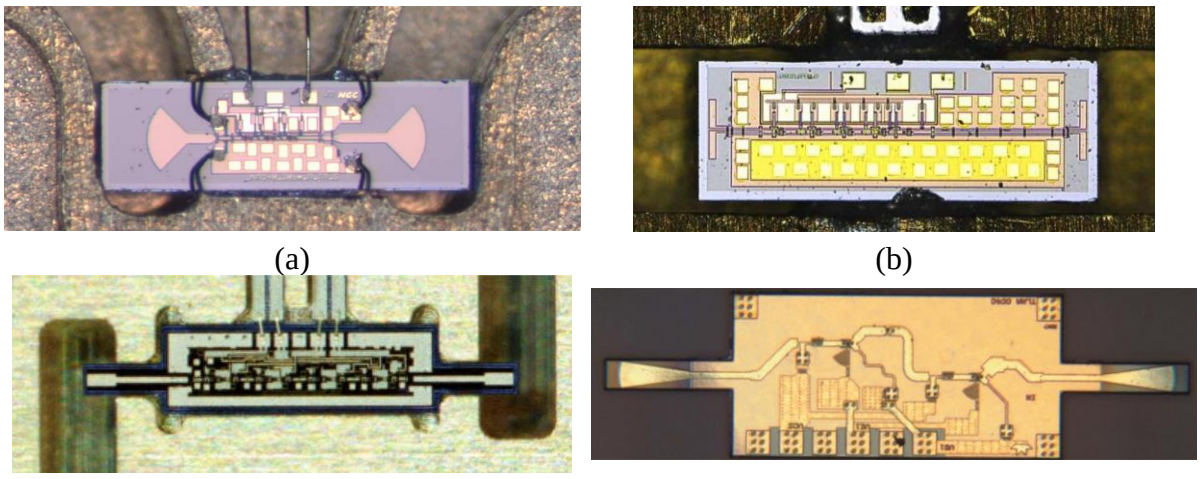
surrounding cavity dimensions to avoid unwanted excitation of waveguide modes into the integrated circuit [101].



(a) (b)

Fig. 56. (a) Picture of a metallic split-block package containing bias circuitry and waveguide flanges. (b) Picture of a 300 GHz III-V based MMIC integrated in an E-plane metallic split-block package. Taken from [131].

An example of a 300 GHz InGaAs mHEMT amplifier packaged in a metallic split-block module is illustrated in Fig. 56 (a). If we zoom inside, we can notice how the IC is coupled to the waveguides thanks to E-plane rectangular probes made from a 50 µm quartz substrate. The choice of substrate (Dk ~ 4.4) as well as its thickness are made to avoid the leakage of waveguide modes into the IC. To interconnect the E-plane probe to the IC, very short 25 µm diameter gold wirebonds have been used. However, due to the wirebond interconnection, this integration approach is limited to 300 GHz [101]. To minimize the effect of the wires, some approaches opted to interconnect different wirebonds in parallel to minimize their impact. However, this solution is not practical when performance reproducibility between different modules are required [101].



(a) (b)

(c) (d)

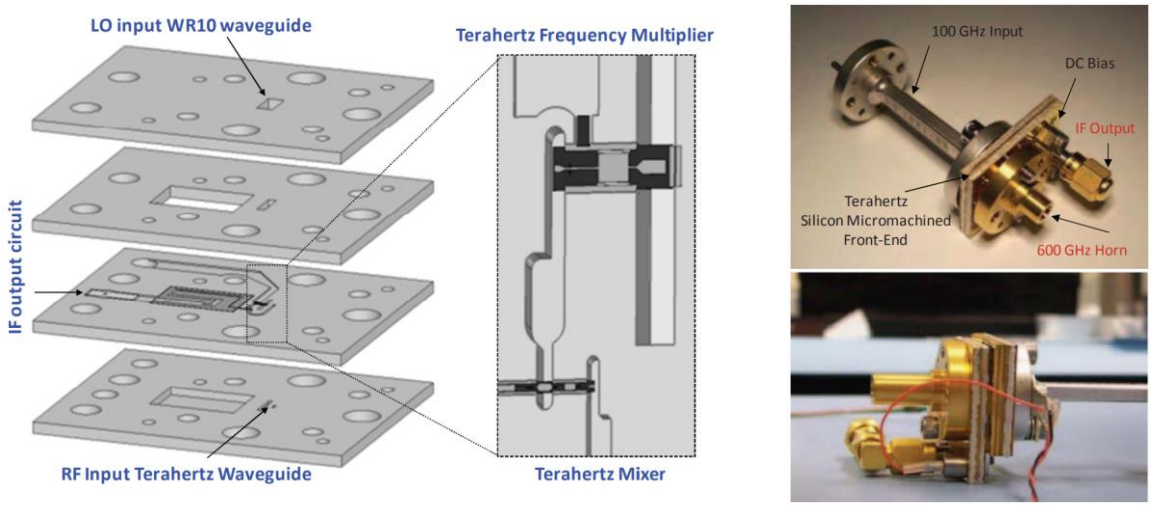
Fig. 57. Some ICs with E-plane probe integrated directly into the chip. Rectangular IC configurations: (a) 300 GHz amplifier with radial E-plane probes from [132] and (b) 480 GHz low noise amplifier (LNA) from [133]. Nonrectangular ICs: (c) 650 GHz power amplifier from [30] and (d) 300 GHz LNA from [134].

Consequently, the possibility to directly integrate the E-plane probe into the IC has been explored. Some examples of this approach are illustrated in Fig. 57. We can notice that for (a) and (b) examples, the E-plane probe is integrated in the IC. However, when large-chip-width ICs must be integrated in the split-block module and working frequency increases, the E-plane probes could cause energy leaking from the waveguide to the chip channel. One solution is to add Silicon absorbers at the top of the MMIC to accumulate the parasitic energy or to add periodic metal pin structure to create an artificial magnetic conductor to avoid the propagation of unwanted modes [130], [135].

Another solution is to change the geometry of the IC. By removing the corners of the E-plane probe, the chip becomes electrically narrow in the transition region. These chips' geometries can be achieved by chemical etching or laser ablation [101]. Some examples are illustrated in Fig. 57 (c) and (d) by using rectangular and radial probes.

3.2.2 Cost-effective THz packaging solutions

Even though metallic split-block technology remains promising in terms of performances thanks to low-loss machined waveguides, this solution is not compatible with high-volume manufacturing required by consumer market due to high cost of manufacturing. In consequence, several solutions have been proposed to be aligned with large scale production. One of them is Silicon micromachined technology, where ordinary semiconductor fabrication processes can be used with excellent tolerance and productivity [101]. Since this process relies on photolithography, this packaging technology produces batches of devices in a simple run, reducing the cost per device when produced in mass [125].



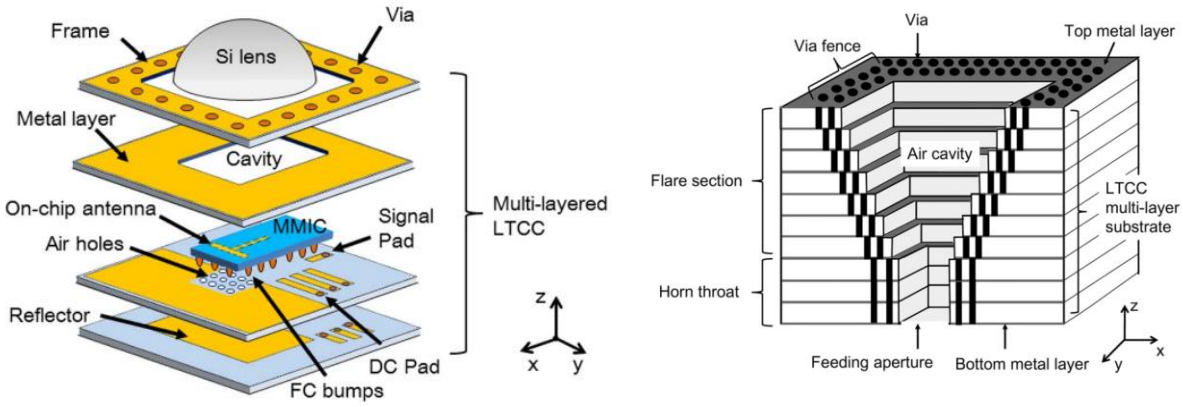
(a) (b)

Fig. 58. (a) Silicon micromachined wafers staked together to form a (b) 600 GHz heterodyne receiver front-end. Taken from [136].

This technology consists of multiple Silicon wafers with thickness of around few hundred microns which are etched separately and staked vertically. The used etching technique is the Deep Reactive Ion Etching (DRIE) which relies on bulk Silicon plasma etching. For THz devices, the Bosch process which works at room temperature may also be used. This process

relies on fluor-based plasma (Sulfur Hexafluoride, SF6) for etching and Octafluorocyclobutane gas to deposit a chemically inert passivation layer. The silicon depth etch, and the etching process selectivity determines generally the silicon layer thickness that must be used [125].

An example of a 600 GHz III-V front-end receiver is illustrated in Fig. 58. For this package, different Silicon layers have been used to package the different ICs conforming the receiver front end such as 100 GHz amplifiers, 300 GHz frequency multiplier, and a 600 GHz SHM. To inject LO and RF frequencies, metallic feed-horn antenna and waveguide flange have been used.



(a) (b)

Fig. 59. (a) LTCC multilayered package for MMIC with 300 GHz on-chip antenna [137]. (b) 300 GHz corrugated horn antenna in LTCC technology. Taken from [138].

One can also use ceramic LTCC substrates to support THz package, which are commonly used for package mmW ICs below 60 GHz. By stacking multiple substrate layers, we can create suitable packages for Antenna-in-package (AiP) solutions, such as the example illustrated in Fig. 59 (a) where a 300 GHz receiver IC is packaged in a multiple-layer LTCC substrate, facilitating the integration of a Silicon lens used to increase the directivity of the antenna [101]. We can notice that the package structure follows a vertical integration strategy like the Silicon micromachining technology. For this example, the antenna is integrated directly into the ICs and a reflector is made using the lower LTCC layers. In other solutions, step-profile corrugated horns antennas have been designed and fabricated (Fig. 59 (b)) using 27 LTCC layers, achieving an antenna with a18 dBi peak gain [138].

As noted, since ordinary LTCC technology does not provide internal metallization of sidewalls, via walls are used to guide properly the desired waveguide modes from one point to another. So, fabrication limitations are critical for the performance of the package since waves experience the material properties at the corrugations (having a direct impact on the signal loss) [101]. A widely known packaging technology that allows surface metallic coating is the plastic molding technique (commonly known as Plastronics), leading to expected performances similar as that for metallic blocks [101]. This could be an interesting alternative to metallic split-block package when low-power management is required. Since arbitrary

shapes can be molded, this option has been used to support the packaging of passive devices such as 77 GHz antennas [139] and even active circuits such as 585 GHz SHMs [140].

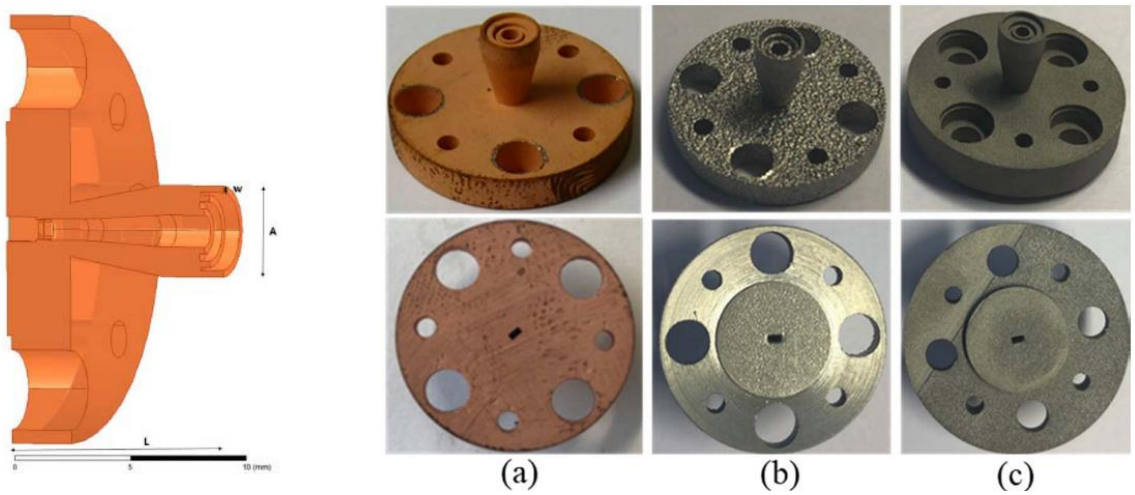
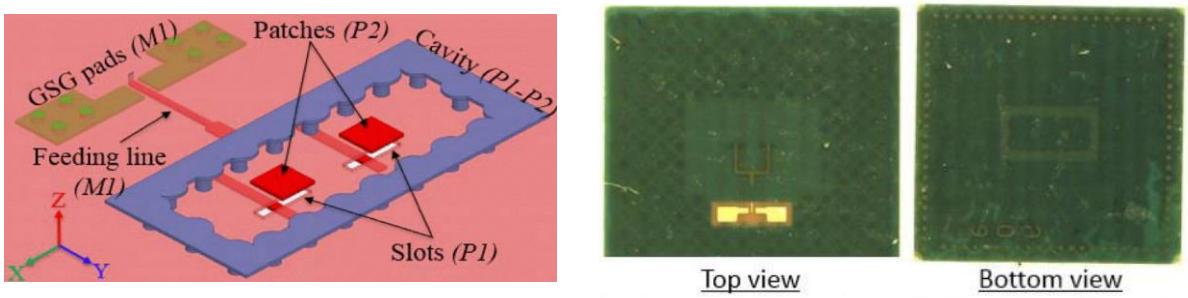


Fig. 60 A 240 GHz horn antenna prototyped using different 3D printing technologies: Stereo Lithography Apparatus (SLA), Selective Laser Melting (SLM) and Micro Laser Sintering (MLS). Taken from [141].

Even more, one can think of the possibility of using 3D metallic printing to support THz package. Three main technologies exist today: Blinder Jetting (BJ), Selective Laser Sintering (SLS) and Selective Laser Melting (SLM). With those technologies, metal powder is joined (BJ) using a binding agent or even melted (SLS and SLM) with the help of high- power lasers to form the desired structure. In terms of roughness, SLS and SLM achieves lower surface roughness (below 2 µm) compared to BJ technology with 4 µm. However, for frequencies higher than 200 GHz, more aggressive surface roughness are needed (< 1 µm), leading to metal-coated dielectric 3D printed devices using Stereo Lithography Apparatus (SLA) or metal 3D printed devices relying on Micro Laser sintering (MLS) technology [141] to achieve promising performances. In Fig. 60, different 3D printing technologies are compared versus a 240 GHz horn antenna fabrication.

Finally, other technologies of packaging have been evaluated to support THz applications at even higher frequencies such as the organic laminate substrate, which is described in section 3.1.1. In fact, 220 GHz E-plane Back-to-Back (B2B) transitions in organic substrate has been evaluated [142] as well as 240 GHz patch antennas, where promising performances can be achieved with more aggressive design rules [143]. The mentioned patch antennas are illustrated in Fig. 61. In this configuration, a cavity is used around the antenna to reduce the impact of surface waves and also to improve directivity.

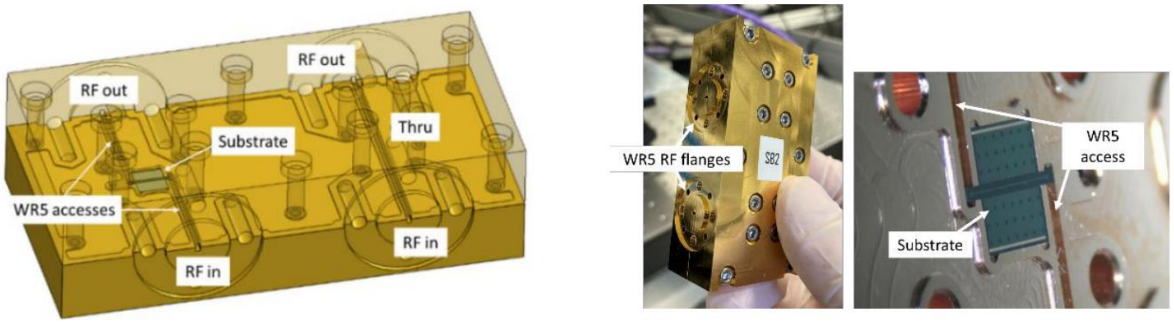


(a) (b)

Fig. 61. 240 GHz antenna integrated on organic laminate substrate. (a) 3D layout view and (b) top and bottom view. Taken from [143].

3.3 Hybrid Packaging solutions: Metallic Split-block & Organic Substrate

On one hand, the potential of organic laminate substrate to enable large manufacturing production packaging solutions has been highlighted. In addition, organic laminate substrates have already been evaluated for applications above 200 GHz showing promising performances when a good control of manufacturing tolerances is achieved [143]. On the other hand, even though diverse THz low-cost packaging solutions can be found in the state-of-the-art, metallic split-block solutions continue to lead in terms of performances thanks to CNC-machined waveguides [101]. In this logic, we could wonder about the possibility to take advantage of the confirmed good performances of metallic split-block package as well as high-volume manufacturing and process automation of organic laminate substrate to propose a hybrid packaging solution leveraging laminated-based packaging integrated in metallic split-block modules.

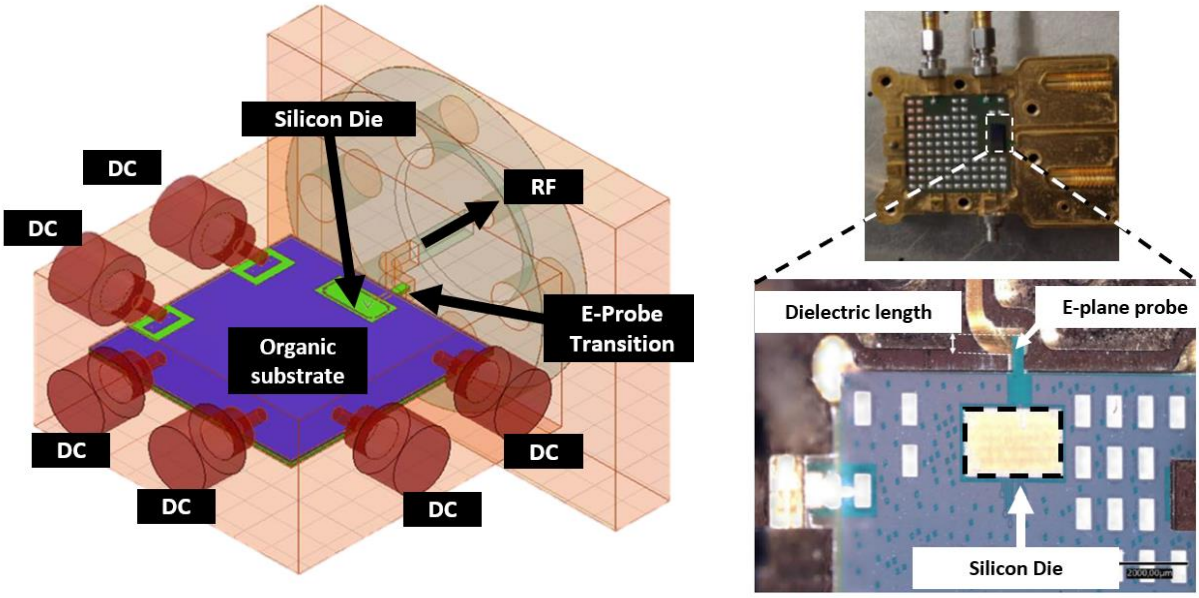


(a) (b)

Fig. 62. (a) 3D CAD view and (b) photo of a 220 GHz B2B transition in organic laminate substrate encapsulated in a metallic split-block module. Taken from [142].

In fact, this approach has already been explored in previous works. Firstly, by the integration of an E-plane radial B2B WG-to-SSL transition in an organic laminate substrate enclosed in a metallic split-block module. This approach is illustrated in Fig. 62. To reduce the costs of metallic split-block, THRU waveguide connections for de-embedding purpose were integrated directly into the same split-block module. To connect properly the ground of the top metal layer to the top split-block, bendable wirebonds were used at the borders of the

organic substrate. This work led to B2B insertion loss of 2.5 dB around 200 GHz, drawing the first perspectives for low-cost sub-THz Silicon packaging.

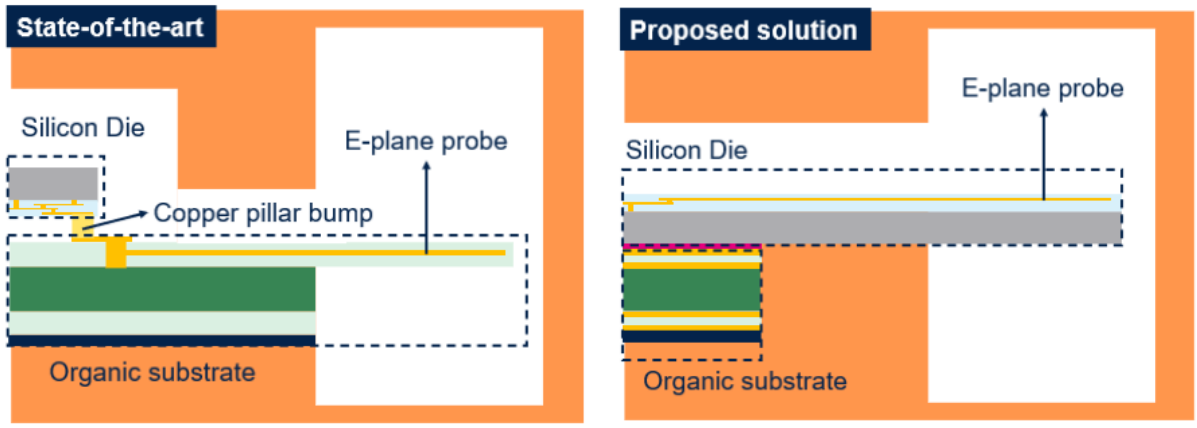


(a) (b)

Fig. 63. (a) 3D view of a 130-260 GHz Silicon Noise source integrated in an organic substrate and metallic split-block. (b) Top zoomed view of the Silicon die attached to the organic substrate. Taken from [76].

Secondly, the integration strategy was complexified by the integration of a Silicon Noise source at 130-260 GHz. This example is illustrated in Fig. 63. The circuit is controlled via DC ports which are soldered to the organic substrate. Moreover, the Silicon die is attached to the organic substrate by copper pilar bumps. Noise RF output is transmitted by metallic CNC waveguides thanks to E-plane probes integrated in the organic laminate substrate. Finally, to ensure proper grounding of the organic substrate, graphene paper has been placed below and above the substrate. Compared to traditional packaging of III-V based ICs in full metallic split-blocks, this solution enables low-cost volume manufacturing of Silicon-based packages, since die attach, wirebond, and copper pilar bumps can be performed using automated production line.

3.4 Proposed Package Integration Strategy for Full Passive Silicon Circuits



(a) (b)

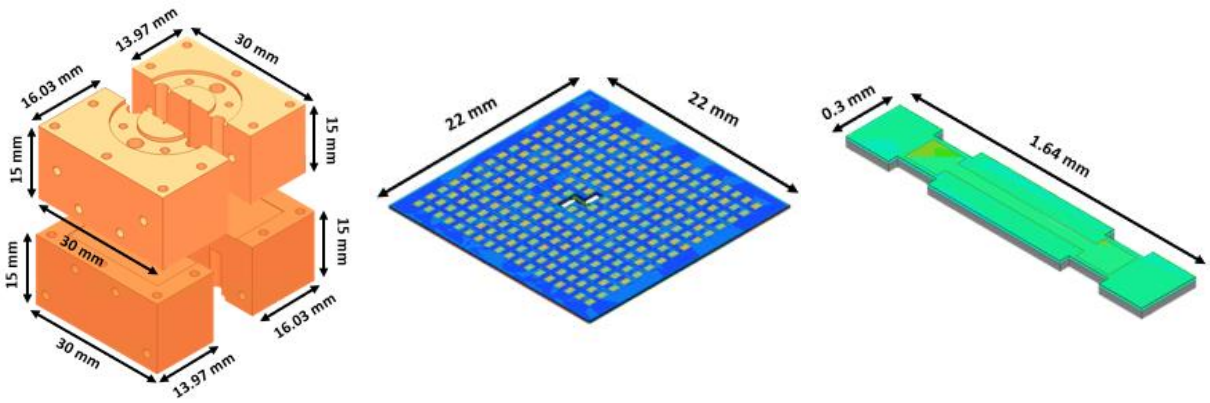
Fig. 64. (a) E-plane integration proposition from state-of-the-art [76] and (b) proposed E-plane integration. The figures are not in scale.

In Fig. 64 (a). A cut view to illustrate how the E-plane probe is integrated on the organic substrate from the previous noise source [76] is presented. For this circuit, a six metal-level organic laminate substrate has been used. Firstly, the remaining dielectric below the probe has been retired using laser ablation to reduce the quantity of dielectric material inside the waveguide to improve the insertion loss of the transition. Then, the probe is routed at the second metal level to be interconnected at the first metal level with the Silicon die, which is assembled using flip-chip technology to enable copper pilar bump junction. However, this option requires the use of copper pillar bumps to route the E-plane signal to the Silicon die, adding complexity to the circuit thus increasing the fabrication costs due to an additional fabrication step.

One can think then to follow a similar approach as in [30], [132], [133], [134], where the E-plane probe is integrated inside the III-V IC, simplifying the integration strategy by elimination of copper pilar bumps and wirebonds which limits also the frequency of operation of the transition. To adapt this solution to a Silicon automated packaging process, we propose to follow the integration strategy illustrated in Fig. 64 (b), where the probe is integrated into the Silicon chip. Here, we suggest routing the E-plane probe at the top-metal level of the Silicon BEOL to reduce losses associated to the Silicon substrate as well as reduction of conduction losses thanks to thick metal levels. As well as in III-V transitions, a reduction of die thickness is mandatory to avoid excitation of unwanted modes due to Silicon high dielectric constant (Dk ~11). Finally, the organic laminate substrate will serve just as a support element for the Silicon die.

3.4.1 Solution description

As a proof-of-concept, we propose to demonstrate the mentioned solution firstly by the integration of a full passive circuit. Later, in chapter 4, a more complex integration strategy will be proposed targeting a Silicon-based SHM design. Here, the proposed circuit to be embedded in the Silicon IC is a WR3 B2B WG-to-SSL transition, operating at 220 – 320 GHz (frequency band determined by the monomodal TE10 operation band for WR3 waveguide).



(a) (b) (c)

Fig. 65. Main blocks composing the proposed integration strategy: (a) Metallic split-blocks, (b) organic laminate substrate and (c) Silicon integrated circuit.

The first package element is the metallic split-block module, which is mainly used to provide the waveguide routing from the external waveguide flanges into the E-plane probes integrated on the IC. The proposed metallic package is illustrated in Fig. 65 (a). At first sight, one can notice that the metallic block is split into four pieces instead of two as in previous examples. In fact, a straight-forward horizontal waveguide routing (which leads to a two-pieces metallic block module) will cut through the thin organic laminate substrate (192 µm), letting all mechanical stability to the machined microchannel, increasing the risk of substrate rupture. In consequence, both input and output of the waveguides are initially routed vertically and then coupled to the E-plane probes thanks to H-plane bends with rectangular corners. However, due to the high aspect ratio between the width of the vertical waveguides and the metallic split-block heights, it seems reasonable to split the top and bottom blocks vertically to facilitate the fabrication.

The second package element is the organic laminate substrate, illustrated in Fig. 65 (b), which will allow the Silicon IC (Fig. 65 (c)) to be attached properly. A more detailed description of the circuit on the Silicon die will be provided in section 3.6. Finally, the enclosing of the organic laminate substrate and the Silicon die in the metallic split-block is illustrated in Fig. 66. The final dimensions of the metallic module as well as the organic substrate width and length were chosen to facilitate the manual manipulation[10].

[10] The pieces have been sized big enough to be hold (manipulated) easily by hand.

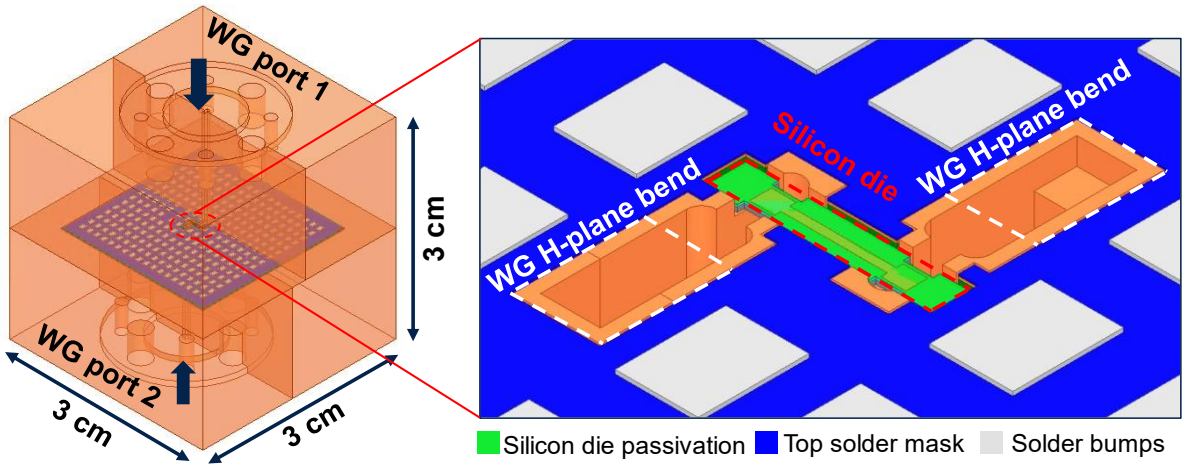


Fig. 66. Representation of the proposed package module for a WR3 B2B WG-to-SSL transition.

To interconnect properly the waveguide input and output of the metallic block, WR3 flange transitions are integrated at the top and bottom of the block. If we zoom into the IC, we can notice firstly how the vertical waveguide is interconnected to the horizontal waveguide by the H-plane rectangular bends. In fact, the distance between the H-plane corner and the beginning of the reduced-heigh horizontal waveguide has been chosen as higher than the WR3 nominal width to ensure wave's propagation. The reduced-height horizontal waveguide (half of the WR3 nominal height) is used to improve the impedance matching between the waveguides and the E-plane probes. Finally, 100 µm metallic walls are placed around the horizontal waveguides to avoid interaction with the organic substrate.

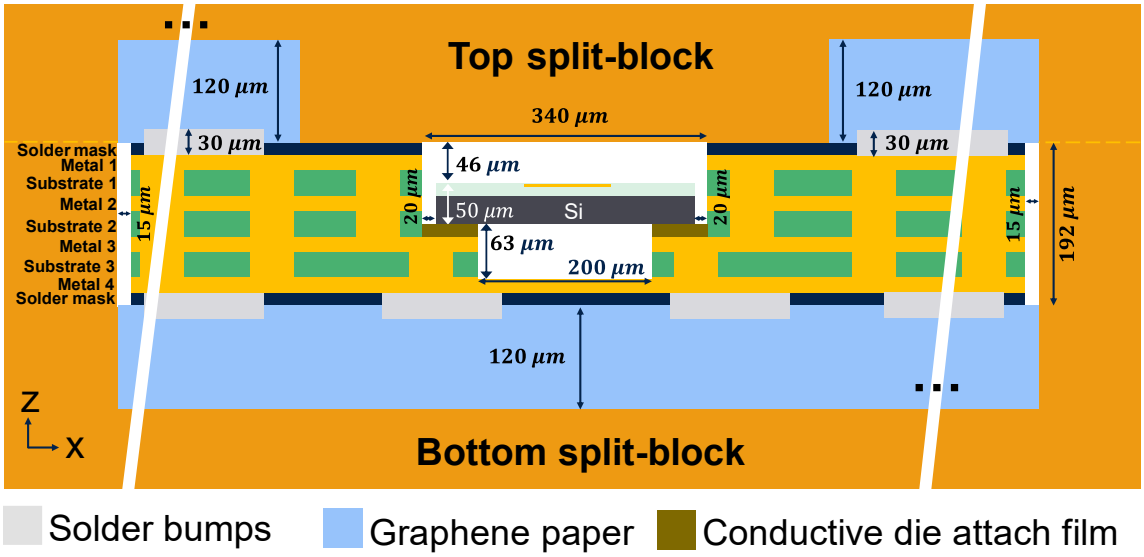


Fig. 67. Cut-view of a Silicon-based suspended stripline integrated on industrial laminate substrate.

A cut-view of the Suspended Stripline (SSL) that interconnects both E-plane probes is illustrated in Fig. 67. To form the channel that encloses the SSL, a four-metal levels coreless laminate substrate is used, giving more freedom to control the height of the required channel. As prepreg material, a 30 µm Mitsubishi GHPL-830NS laminate is used. Moreover, metal levels have a thickness of ½ oz (18 µm) and solder mask resin of ~15 µm, giving a total

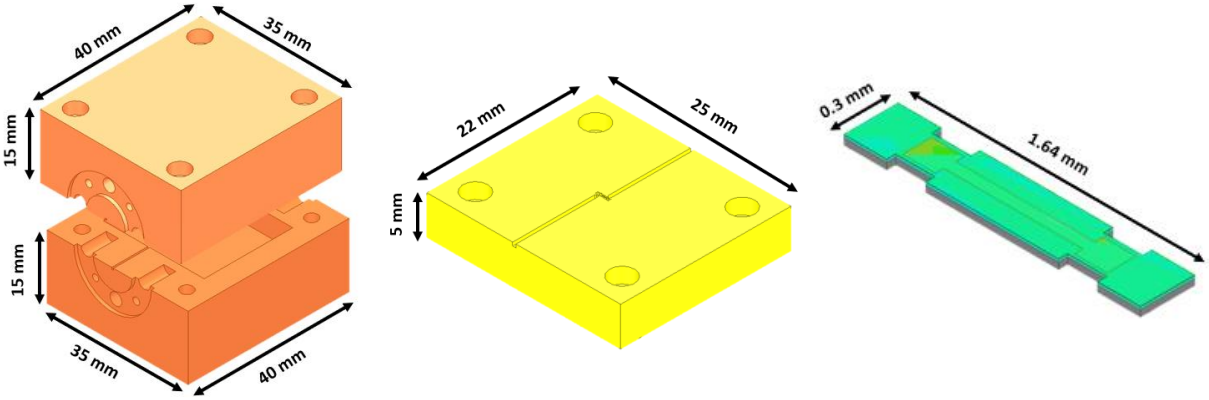
organic substrate thickness of ~192 µm. Due to aggressive dimensions, substrate channel will be made using laser ablation.

To ensure that the Silicon die fits the laser-machined channel, 20 µm of space is led between the Silicon die borders and the channel prepreg walls. This distance has been calculated considering a ±5 µm laser ablation error when the Silicon die is shaped, and the organic substrate channel is formed. The same principle is applied to the space between the outer border of the laminate organic substrate and the borders of the CNC machined (assumed CNC error of ±5 µm), which is fixed to 15 µm.

Also, metallic vias are placed between all metal levels to ensure ground distribution in all the board. Furthermore, solder bumps with a height of around 30 µm and 800 x 600 µm² dimensions are placed at the top and bottom of the board to ensure the contact of the board's ground to the bottom and top metallic split-blocks. However, since a fine control of the height of the solder bumps is difficult (leading to some substrate areas disconnected from the ground), a 120 µm graphene paper is used, which is deformable and conductor, and it will adapt to the high variability height of the solder bumps. Finally, the Silicon die is thinned to 50 µm using laser ablation and attached to the organic substrate using conductive die attach film. Even more, to improve the attaching of the thin die to the organic substrate, the Silicon substrate is extended after the E-plane probes to avoid bending and cracking during manipulation.

3.5 Full Metallic Split-block Integration Adapted for Full Passive Silicon Circuits

To have a reference point to compare the previous integration strategy, we propose to package the mentioned Silicon IC into a traditional full metallic split-block module.



(a) (b) (c)

Fig. 68. Main blocks composing the full metallic split-block strategy: (a) Metallic split-blocks, (b) standalone metallic block and (c) Silicon integrated circuit.

The elements that conform the package are illustrated in Fig. 68. For this IC, we propose to use three metallic pieces instead of two: one main metallic block which is split in two forming a top and bottom metallic block (Fig. 68 (a)), and a standalone metallic block (Fig.

68 (b)). The independent standalone block is used to allow testing of multiple circuit versions and it will be inserted into a cavity previously formed in the bottom split-block. Moreover, since no thin organic substrate is present, the waveguides can be routed horizontally as in traditional III-V split-block integration. In consequence, the metallic split-block is split into two pieces instead of four. To interconnect properly the waveguide input and output of the metallic block, WR3 flange transitions are integrated at the left and right sides of the block.

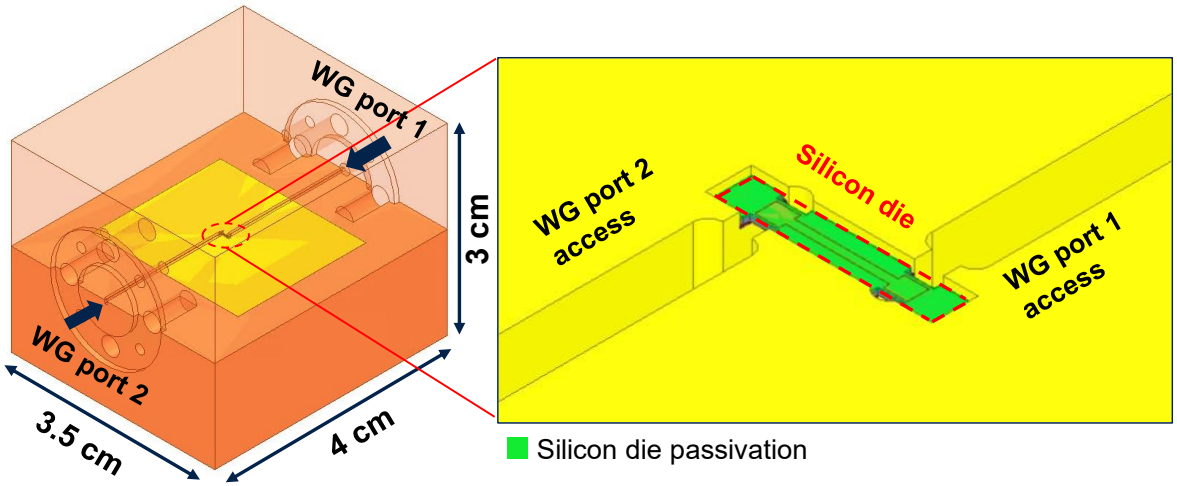


Fig. 69. 3D-view of the proposed full-metallic package module for a WR3 B2B WG-to-SSL transition.

The placement of the waveguide flanges is illustrated in Fig. 69. Following the previous integration strategy, all metallic pieces were dimensioned to facilitate manual manipulation. If we zoom into the standalone split-block we can notice how the Silicon die is attached. A cavity has been made with the same dimensions as the organic substrate to properly place the Silicon IC.

A cut-view of the SSL that interconnects both E-plane probes is illustrated in Fig. 70. The dimensions of the channels that encloses the SSL are the same as those of the previous integration strategy (Fig. 67). In the full metallic split-block integration the organic laminate substrate has been replaced by the standalone metallic block. Moreover, to remain in the same logic as traditional III-V integration, conductive epoxy glue is suggested to attach the Silicon die into the metallic piece. Finally, as similar as the previous integration strategy, enough space has been provided between each piece to ensure proper enclosing of all parts.

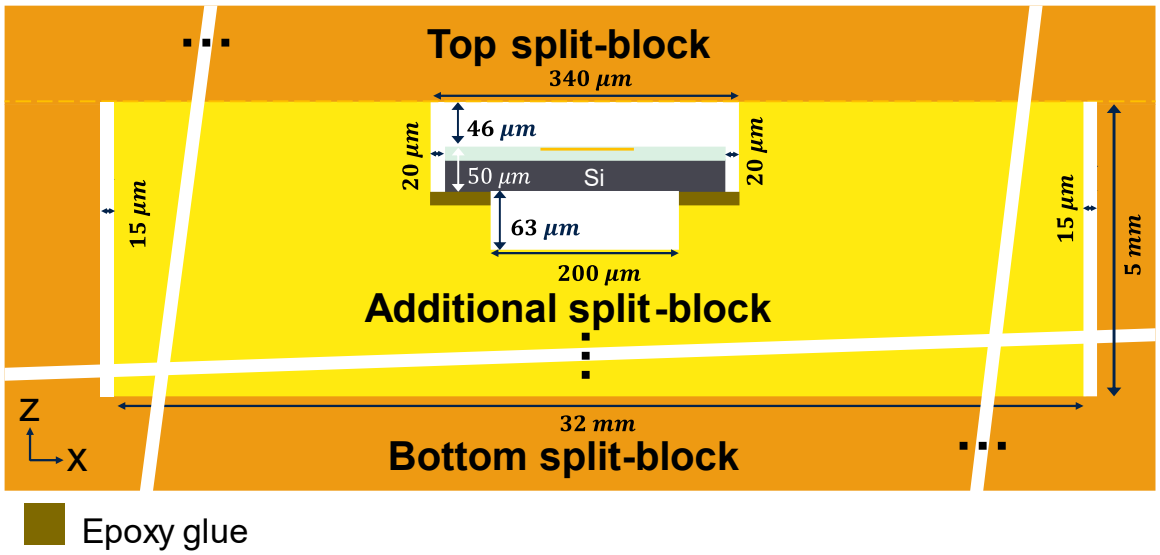


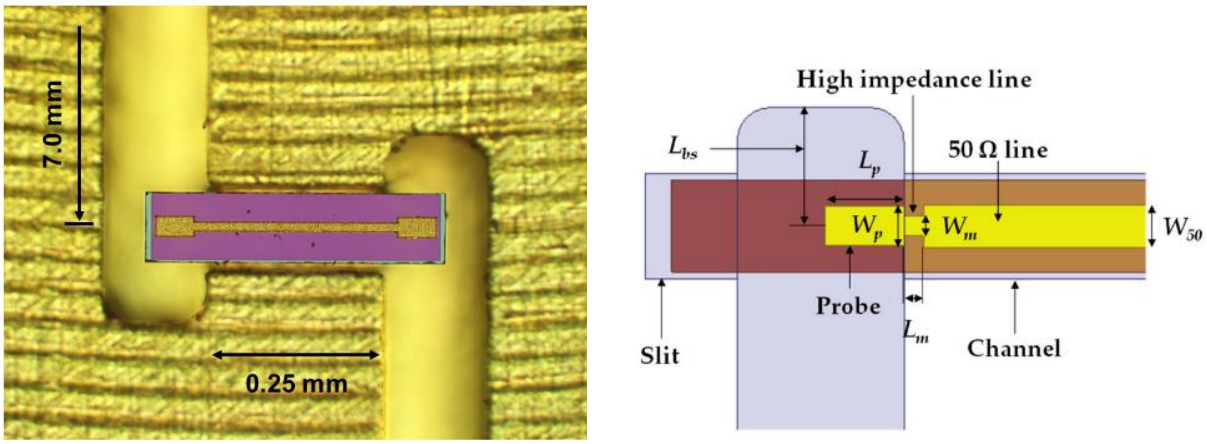
Fig. 70. Cut-view of a Silicon-based SSL integrated on a metallic split-block module.

3.6 WR3 B2B WG-to-SSL Transition Demonstrator design & Simulations

3.6.1 The B2B transition

In this section, a more detailed description of the IC circuit used as a demonstrator for the presented packaging strategies is given, which corresponds to a WR3 B2B transition. The circuit consists of two probes (radial, rectangular, or antipodal finlines), which are interconnected together via a transmission line. These probes are generally inserted through the waveguide H-plane and oriented parallel or perpendicular to the waveguide E-plane. Normally, when the probe is oriented parallel to the waveguide E-plane, it is called E-plane probe. In full metallic split-block integration, this probe orientation is mainly used due to IC ease of integration. An example of a waveguide B2B transition is illustrated in Fig. 71 (a). Concerning integration, some solutions propose the use of extended slits to improve mechanical stability for thin and soft substrates which can easily bend [144]. An example of an extended E-plane probe is illustrated in Fig. 71 (b).

Moreover, diverse solutions propose the use of high-impedance transmission line (that behaves as a series inductor) to compensate the capacitive behavior of the probe to adapt it properly to a 50 Ω transmission line [144], [145], [146]. Other configurations where an IF/DC return path is needed will be explored in detail in the next chapter for the design of a H-band SHM.



(a) (b)

Fig. 71. Some examples of non-DC return path B2B transitions. (a) WR1.5 GaAs B2B transition from [147] and (b) WR10 TLY-5 B2B transition from [144].

In Table 10, a recompilation of different waveguide-to-planar circuits transitions packaged in full metallic split-block module is presented. Here, we focus mainly on the reported E-plane transitions in B2B configuration at mmW and THz frequencies (> 110 GHz). We can notice that, excluding organic substrate transition, the single transition loss is around 1-1.5 dB independently from frequency. This value can be extracted by de-embedding the probe losses from the transmission line and waveguides.

Ref.	Frequency (GHz)	Probe type	Substrate type	Transmission line	IL per probe (dB)	Total IL (dB)
[148]	110-170	Rectangular	Quartz	Stripline	N/A	1.0
[142]	140-220	Radial	Organic	CPWG	4.5	11.0
[149]	185-225	Double dipole	InP	CPWG	1.2	5.0
[150]	220-325	Rectangular	Quartz	Microstrip	1.0	3.0
[150]	220-325	Rectangular	GaAs	Microstrip	1.5	~4.0
[151]	220-325	Radial	InP	GCPW	N/A	1.5
[152]	240-320	Dipole	InP	CPW	~1.0	N/A
[153]	260-320	Dipole	InP	CPW	1.0	7.5
[154]	340-380	Dipole	InP	CPW	~1.0	~7.0
[147]	500-720	Rectangular	GaAs	Microstrip	~1.0	~2.0

Table 10. Waveguide-to-planar circuit transitions state-of-the-art at mmW and THz frequencies.

In conclusion, to remain aligned to the mentioned H-band state-of-the-art, a goal of ~1.3 dB insertion loss for a single probe transition seems reasonable. As a starting point, the total B2B losses must be around ~2.8 dB considering the average reported WR3 B2B losses [150], [151], [152], [153].

3.6.2 B2B transition design & simulations

The final choice of type of probe and transmission line is motivated by the transitions and SSL used in the proposed 268 GHz SHM in chapter 4. Here, the probes that have been used are based on extended probe architectures where the rectangular probe width (Wprobe) occupies mostly all the waveguide height to then provide a proper IF/DC return path. Moreover, GaAs SHM state-of-the-art propose to reduce the waveguide height to improve the matching between the probe and waveguide, thus improving the bandwidth of the transition [155], [156]. For the proposed WR3 B2B transition, we opted to use the same extended rectangular probe as in state-of-the-art SHM, but with the elimination of the IF/DC return path.

Concerning the choice of the transmission line, a SSL was selected. In WR2.8 GaAs SHM design, this choice of transmission line is preferred due to the improved attenuation constant compared to a non-suspended configuration (microstrip), leading it interesting for filters' design [157]. In chapter 4, a more detailed description of this transmission line for Silicon substrate will be given and will be applied for the design of stepped low-pass filters. Finally, the mentioned probes and SSLs are illustrated with their main dimensions in Fig. 72.

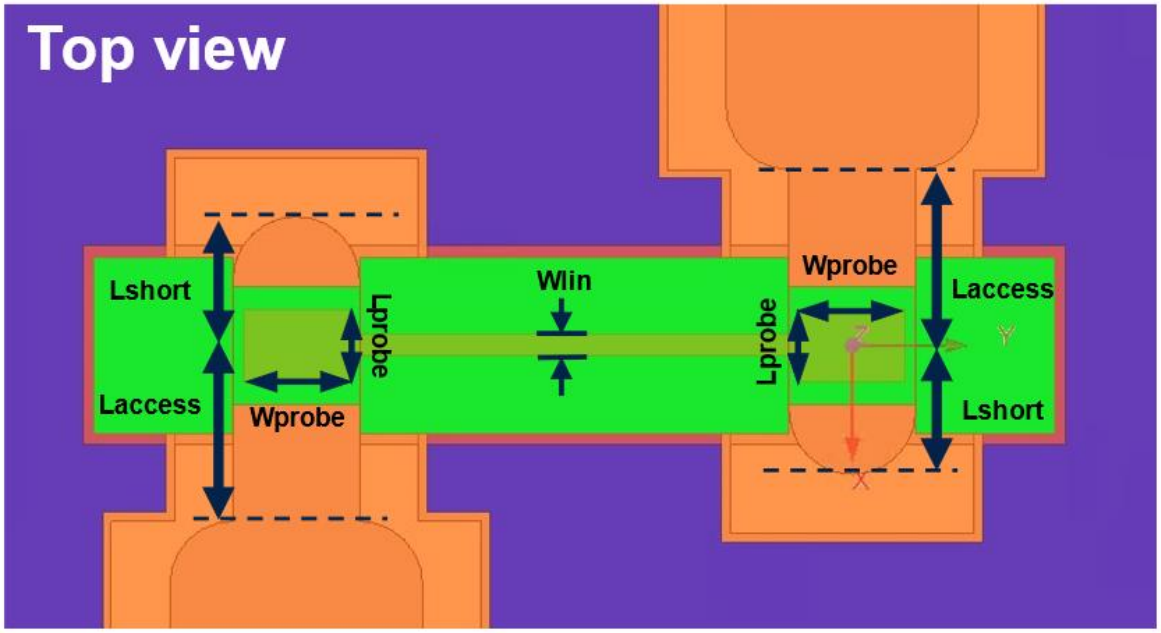


Fig. 72. Top view of WR3 B2B WG-to-SSL transition integrated on the proposed package.

Wprobe	Lprobe	Wlin	Lshort	Laccess
124	180	36	220	300

Table 11. Dimensions of the designed transition (in µm).

The probe dimensions (Wprobe and Lprobe), waveguide backshort (Lshort) and distance between the probe and the waveguide (Laccess) were optimized to improve the insertion loss in the operating band (220 – 320 GHz). The fine tuning was executed via HFSS Ansys EM simulation software using a simplified 3D model where just the Silicon circuit, part of the organic substrate and part of split-blocks were considered to reduce simulation time. Then, when targeted performances were achieved, the complete size of the metallic split-block and

organic substrate was considered for the final simulation. For the full metallic split-block circuit, the optimization strategy was similar, but just replacing the organic substrate by the metallic module. The final optimized values for a Silicon ~50 µm substrate are presented in Table 11.

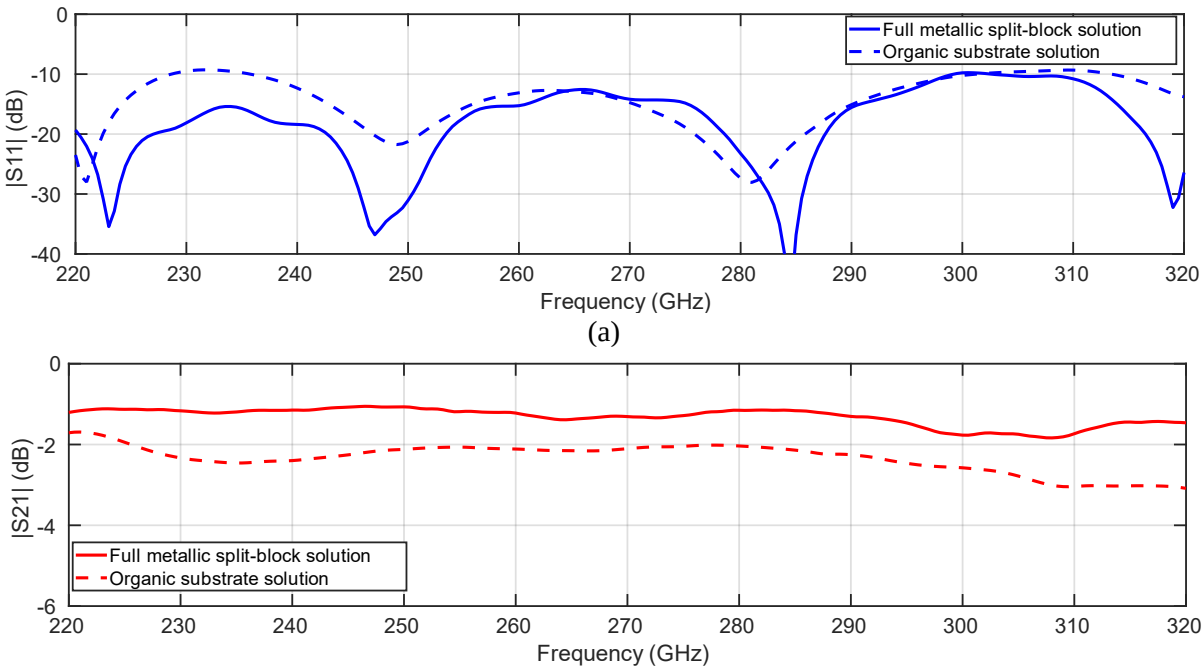


Fig. 73. Simulation of $|S_{11}|$ (a) and $|S_{21}|$ in dB versus frequency for the WR3 B2B Silicon circuit (HR substrate) integrated in Hybrid integration strategy (organic laminate solution) and full metallic split-block integration.

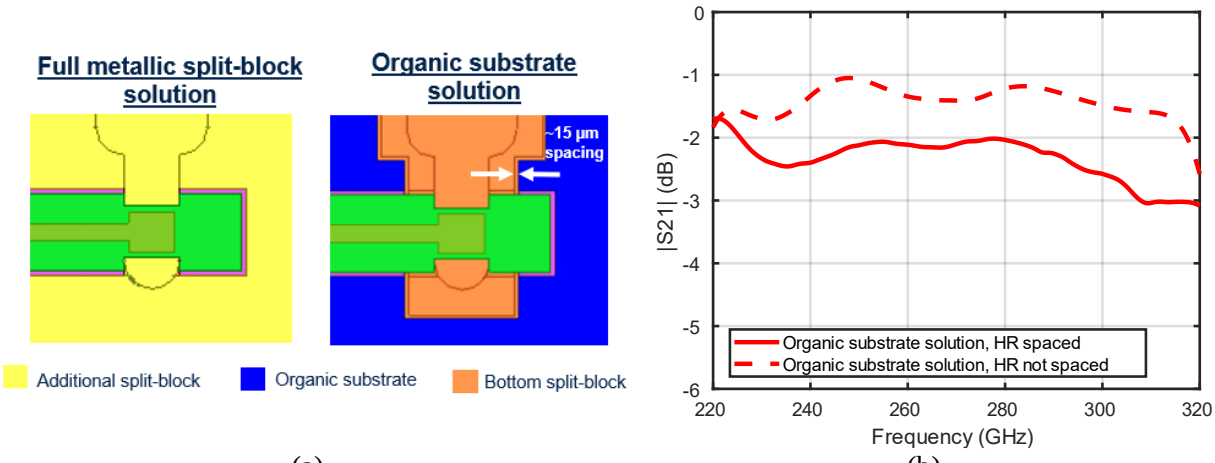


Fig. 74. (a) Top view of simple WR3 WG-to-SSL transitions in Hybrid integration strategy (organic laminate solution) and full metallic split-block integration. (b) Simulation of $|S_{21}|$ in dB versus frequency of the hybrid solution adding and removing the spacing between split-block and organic substrate.

The final achieved performances in terms of $|S_{11}|$ and $|S_{21}|$ are illustrated in Fig. 73. For this simulation, a high-resistivity (125 Ω.cm) substrate based on BiCMOS 130 nm process was used. We can firstly notice that in terms of bandwidth, the $|S_{11}|$ parameters stay below ~-10 dB in the overall WR3 band for both solutions. This shows, at first instance, that the probe impedance has been matched properly with the reduced waveguide impedance. In terms of insertion loss, the $|S_{21}|$ parameter stays above -1.8 dB for the full metallic split-block solution and above -3 dB for the hybrid solution in the overall WR3 band. This difference of 1.2 dB is mainly due to energy leaking between the organic substrate and the bottom split-block spacing of 15 µm, as illustrated in Fig. 74 (a). In fact, if this spacing is eliminated, we could reduce by ~1 dB the insertion loss, as shown in Fig. 74 (b). But unfortunately, this spacing is mandatory to ensure proper enclosing of both elements in the package, as discussed in section 3.4.1.

3.6.3 Silicon DOE description

Based on the previously designed B2B transition, different parameters will be explored to define a Design of Experiment (DOE), taking profit of the different multi-project wafers (MPWs) during the development of this PhD. In this section, the BiCMOS 130 nm process will be mainly explored. However, the WR3 B2B transition integrated in BiCMOS 50 nm (which have been previously presented) will be used also to be compared with the results of BiCMOS 130 nm technology. For this DOE, performances will be evaluated in the first 30 GHz of the 253-321 GHz band standardized by the IEEE 802.15.3d norm. For the following simulations, the surface roughness was neglected but will be considered in the post-simulation study, since reports highlight the importance of this effect in performances [158]. Also, a simplified 3D model of the circuit has been considered to reduce simulation times.

3.6.3.1 Substrate resistivity impact

Firstly, a comparison of the performance of the transition is evaluated considering the resistivity of the different Silicon technologies used for this DOE. The Silicon substrate resistivity (ρ) for the BiCMOS 55 nm technology is 15 Ω.cm and 125 Ω.cm for the BiCMOS 130 nm. The final thickness of the BEOL in SiO2 and the FEOL in Silicon is illustrated in Fig. 75 (a), (b) considering a final total thickness of 50 µm. The passivation layer that is created at the top of the metal layer is also considered for simulations.

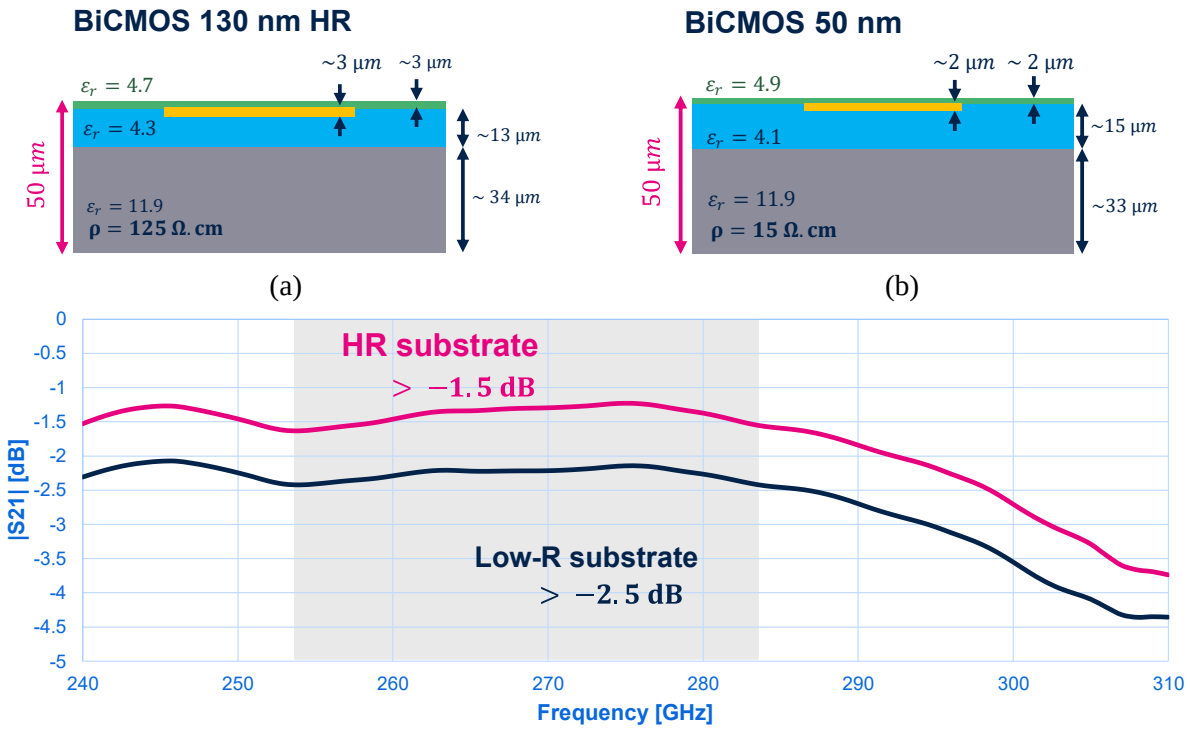


Fig. 75. Description of the SSL and E-plane probe substrate for the (a) BiCMOS 55 nm low-resistivity substrate and BiCMOS 130 nm high-resistivity (HR) substrate. (b). Comparison of simulated $|S_{21}|$ (dB) versus frequency for both solutions.

In Fig. 75 (c) the results of $|S_{21}|$ of the B2B transition is illustrated. For both simulations, we assume that the dielectric constant Dk (~11.9 [101]) is independent from the resistivity of the substrate. We can notice that a reduction of 1 dB in insertion loss is achieved using high-resistivity substrate (in 253 - 283 GHz). For this reason, the HR substrate is prioritized for the design of the B2B transition.

3.6.3.2 Substrate thickness impact

On the other hand, the impact of substrate thickness is evaluated. Thanks to femtosecond laser ablation techniques, we expect to evaluate three substrate thicknesses that can fit properly in the fabricated channel: 75 µm, 50 µm and 25 µm. To achieve this, just the part below the FEOL will be removed. The cut view of the three-substrate thicknesses evaluated in this study is illustrated in Fig. 76 for a BiCMOS 130 nm HR substrate.

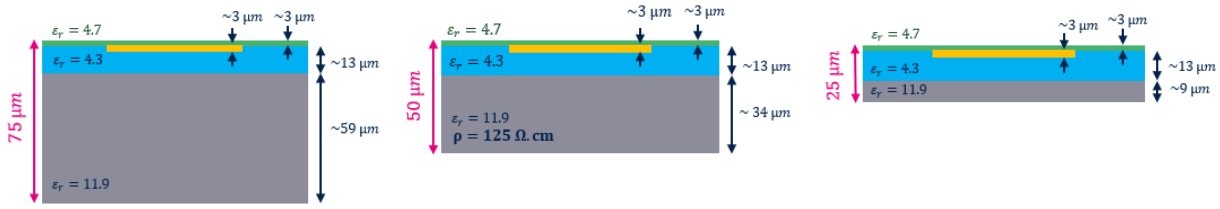


Fig. 76. Cut-view of the transmission line for different substrate thickness: 75µm (a), 50 µm (b) and 25 µm (c).

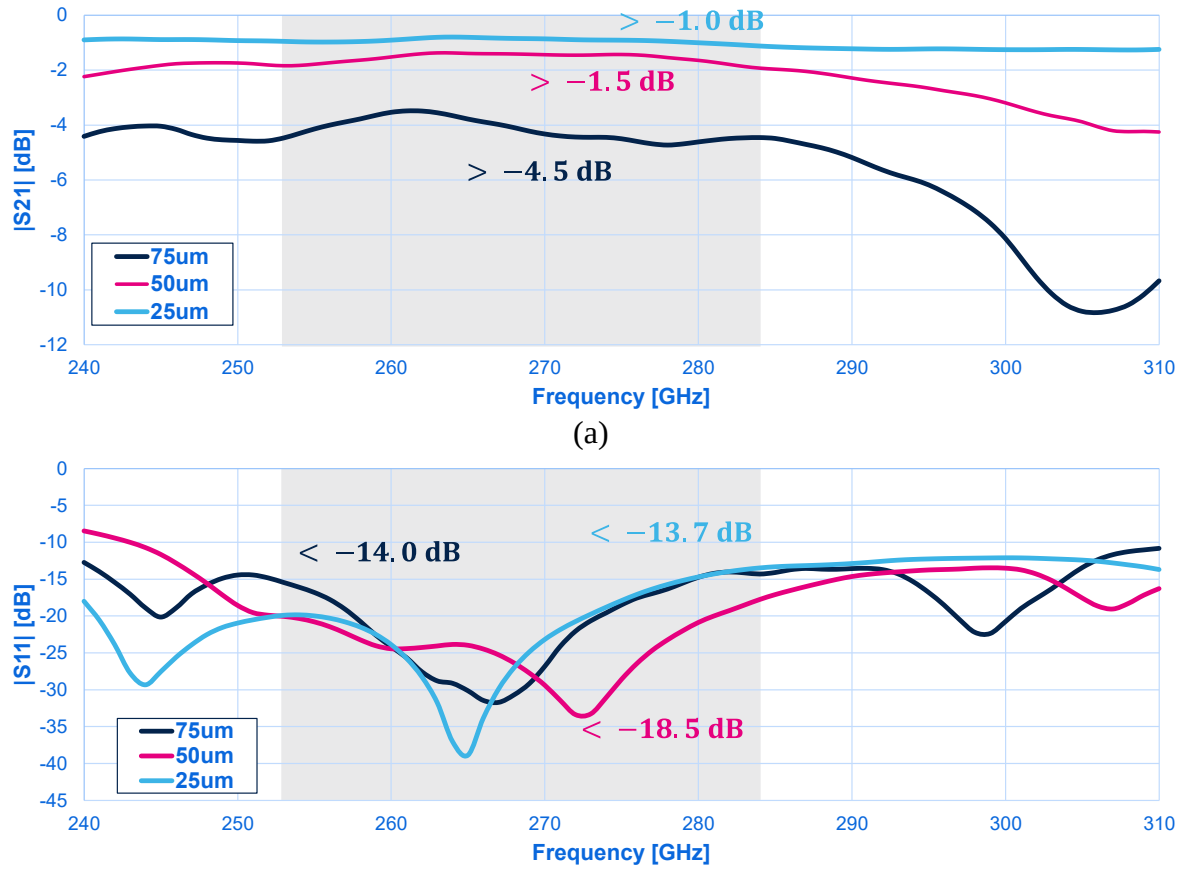
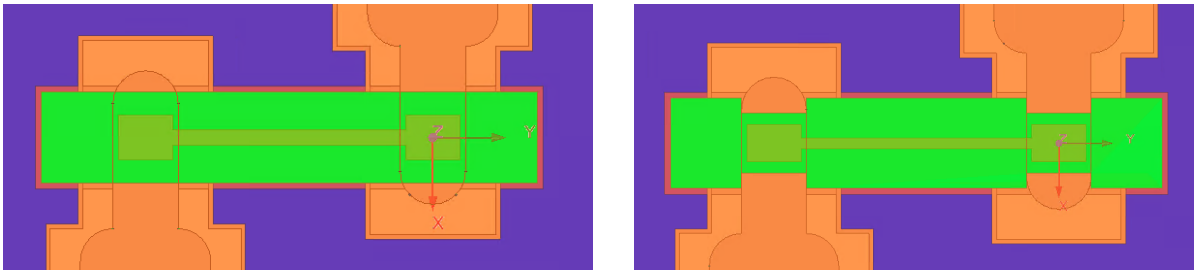


Fig. 77. Simulation of (a) $|S_{21}|$ (a) and $|S_{11}|$ (b) in dB for different substrate thicknesses (HR). Line and probe widths have been optimized for each substrate's thickness.

The simulated $|S_{21}|$ and $|S_{11}|$ parameters for each substrate thickness are illustrated in Fig. 77. The lines and probe dimensions are scaled to present the same impedance independently from the substrate thickness. First, we can notice from the $|S_{11}|$ curve that good matching can be achieved for both simulations ($|S_{11}|$ < 13.7 dB for all cases). Also, we can notice that the reduction of substrate thickness from 75 µm to 50 µm have a positive impact regarding the reduction of the insertion loss (less lossy substrate in probe and in transmission line compared to SiO2). Moreover, reducing from 50 µm to 25 µm show few improvements in terms of insertion loss. However, it allows improvement in bandwidth (less dielectric charge in the channel). In the end, the discussion about the manipulation of a 25 µm substrate is opened and will be answered during the circuit implementation.

3.6.3.3 Extra substrate elimination impact

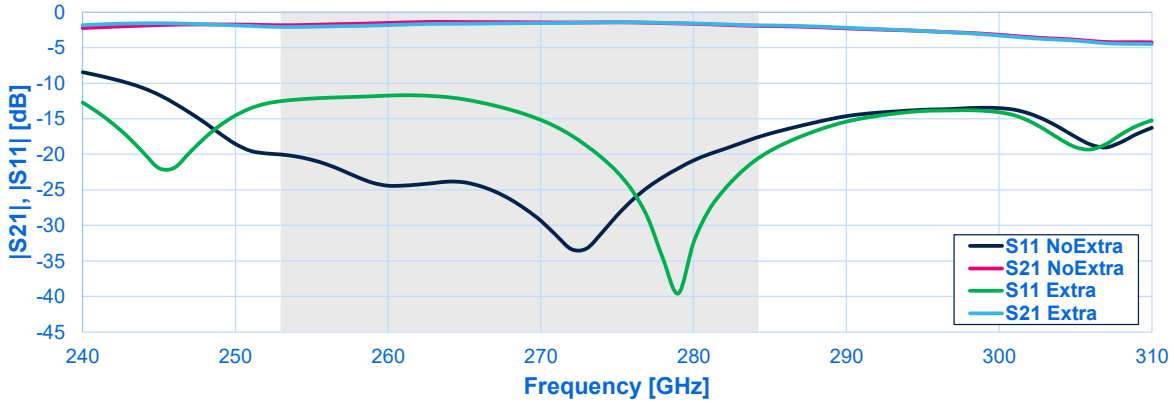
Moreover, the impact on the performance by the elimination of the extra substrate around the probe is explored. In section 3.2.1., it is explained the interest of this technique to avoid excitation of unwanted modes in the IC channel coming from the waveguide [101]. Here, we leverage the impact of this strategy in terms of performance. The configurations that will be compared are shown in Fig. 78. The extra substrate will be retired using laser ablation.



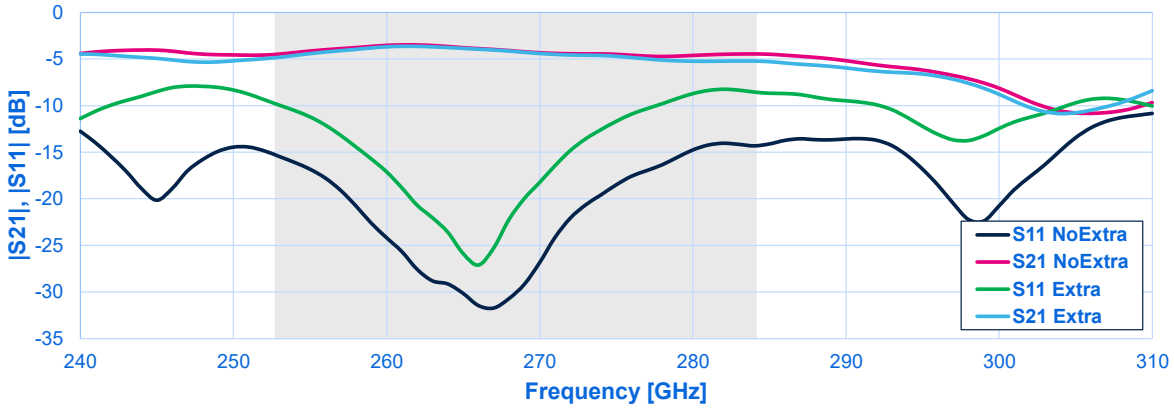
(a) (b)

Fig. 78. (a) Extra substrate configuration and (b) non-extra substrate configuration for the proposed WR3 B2B transition.

The results of simulations for three substrate thickness are shown in Fig. 79. We can notice that the elimination of extra substrate improves the matching between the probe and the reduced-height waveguide, as seen from $|S_{11}|$ parameter. However, this improvement is slightly reflected at the $|S_{21}|$ since the $|S_{11}|$ parameter remains below -10 dB (just 10% of power is reflected) for the 25 µm and 50 µm substrates thickness. However, the elimination of extra substrate seems like an interesting solution to improve the insertion loss for high thickness substrates. In fact, for the 75 µm substrate, an insertion loss reduction of 1 dB is achieved.



(a)



(b)

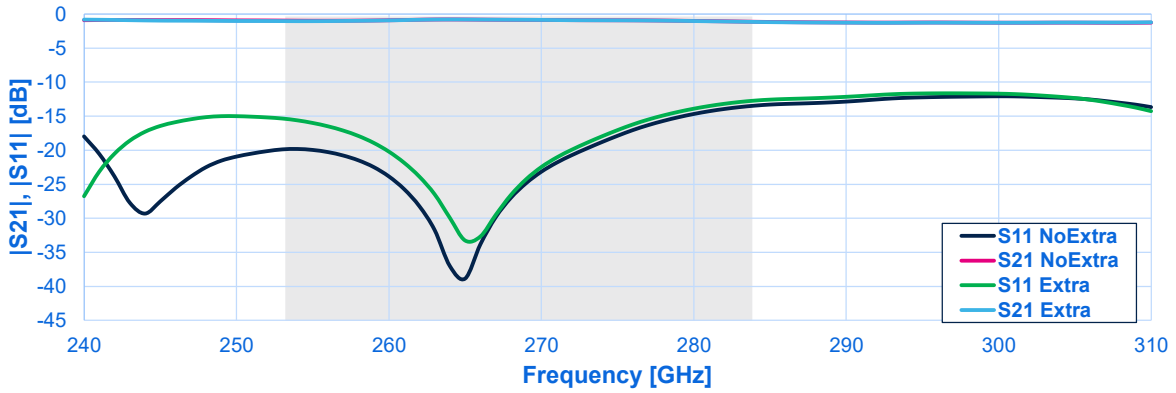


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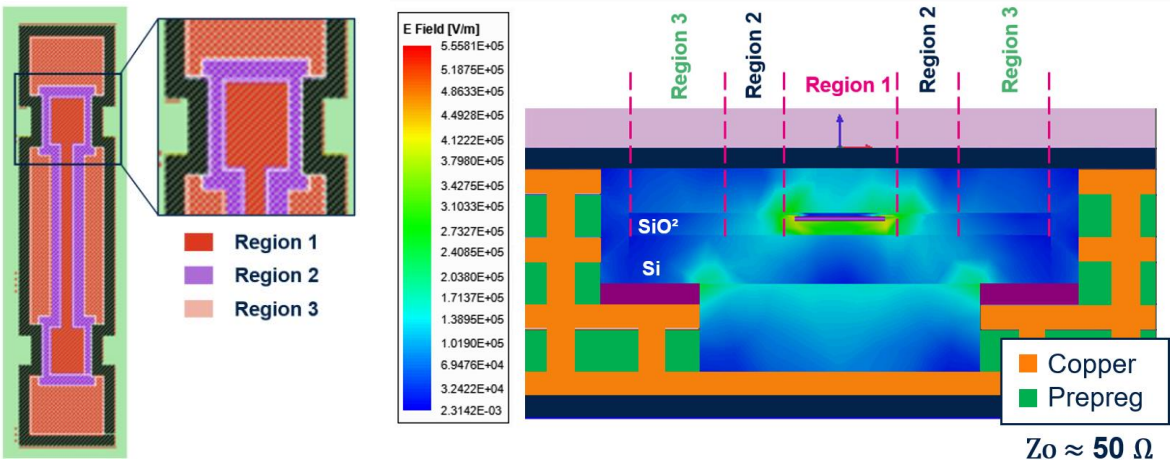
Fig. 79. Simulation of $|S_{21}|$ and $|S_{11}|$ in dB for different substrate thickness (HR) in extra substrate and non-extra substrate configurations. (a) 75 µm, (b) 50 µm and (c) 25 µm.

3.6.3.4 Tiling distribution simulation strategy & impact

To ensure metal layer thickness uniformity when the Chemical-Mechanical polishing (CMP) process is made at wafer fabrication, proper metal area density at each metal layer must be ensured in the overall wafer [159]. In consequence, metal dummies (also called metallic tiles) must be placed in certain regions (especially where metal area density is too low) to respect the design rules of the process. However, the dummies distribution can affect the electrical performances of passive devices such as transmission lines. In fact, the impact of dummies becomes significantly stronger if they are placed in the regions where E-field is stronger. This generates parasitic capacitances and, for frequencies above 10 GHz, it can also affects the resistance and the inductance of the transmission line due to eddy currents [159].

In consequence, a rule of thumb in BiCMOS integrated microstrip lines design is to create a tiling gradient starting from the more critical part (where tiling density is led to the minimum permitted at the technology) and finishing by a high-density tile percentage where the E-field is less intense. Thus, three tiling density regions have been defined. They are illustrated in Fig. 80 (a).



(a) (b)

Fig. 80. (a) Tiling gradient definition for a non-extra substrate configuration. (b) cut-view of the SSL showing the E-field distribution in channel and substrate.

The first region encloses all the BEOL that is below the transmission line and probes with an extra 10 µm area to consider the fringing effect of the electromagnetic fields. Then, a second region of 50 µm is defined around the first one. Finally, a third region encloses the remaining area. For an optimal tiling distribution and respecting as much as possible the design rules, a gradient of tile density has been chosen as illustrated in Table 12 (Proposition 1). The Oxide Diffusion (OD) layer corresponds to the active region's definition. In fact, all that is not OD will be filled with Buried Deep Trench Isolation (BDTI) in the FEOL. However, we must consider that this tiling gradient has been optimized considering that the passive device is a microstrip line, which is not the case. For the implemented SSL configuration, the E-field distribution is illustrated in Fig. 80 (b).

Proposed tiling densities for BiCMOS 130 nm DOE						
Layer	**Proposition 1 (Initial)**			**Proposition 2**		
	Region 1	**Region 2**	**Region 3**	**Region 1**	**Region 2**	**Region 3**
OD	75	75	75	20	20	20
POLY	0	0	0	0	0	0
M1	25	40	60	25	25	40
M2	25	40	60	25	25	40
M3	25	40	60	25	25	40
M4	25	40	60	25	25	40
M5	0	25	35	25	25	40
M6	0	0	40	0	0	40
ALU	0	0	0	0	0	0

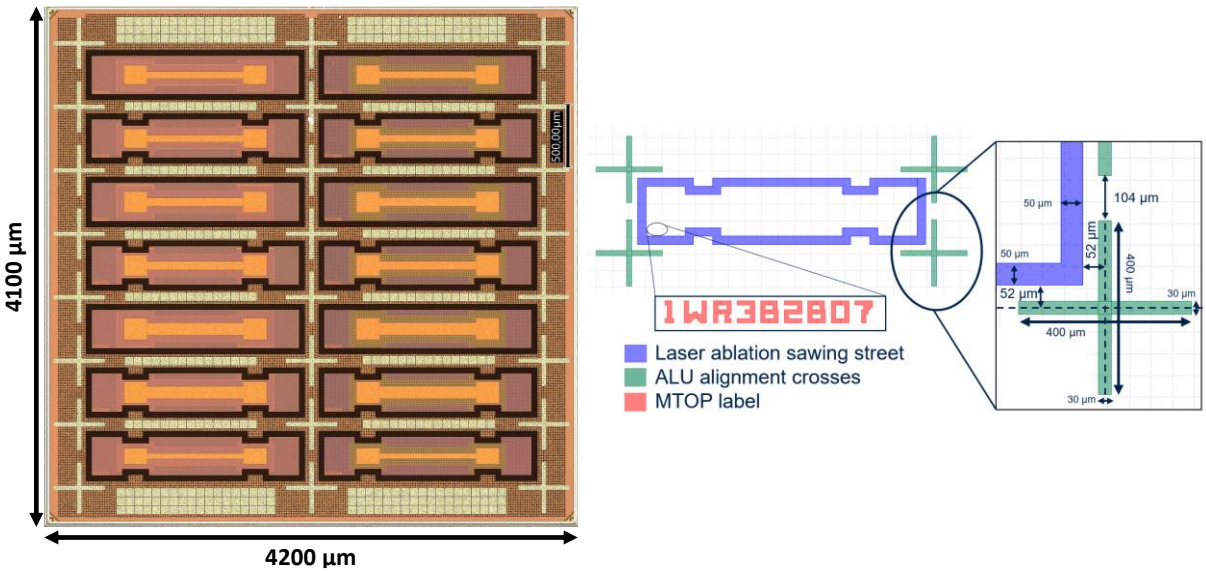
Table 12. Different proposed tiling densities (in %) for the different density regions.

We can notice from Fig. 80 (b) that an important part of the E-field enters region 2. This is due to the conductive die attaching material corner, which lead that the E-field priories a diagonal path from the transmission line to the ground. For the E-plane probe, the E-field is much stronger in the narrower border of the probe, also following a diagonal patch from the probe border to the metallic waveguide border. In consequence, we propose to fix region 2 also with the minimum tiling density permitted by the technology, which corresponds to the second tiling proposition in Table 12.

Finally, the simulation of tiling impact in the SSL and in probe has been a challenge. Due to the high quantity of tiles (~5 millions) in the complete circuit, we are obviously limited by the memory that can be used in simulation due to the size of tiles compared to the overall structure. One strategy is to divide the transmission line into small parts and cascade the S-parameters of simulations results. However, we will need a SSL much longer than ~λ/10 to establish wave transmission in simulation. This leads to a line length of ~100 µm which is still complex and time-consuming to simulate (more than one week). In conclusion, we propose to evaluate the impact of tiling directly by measurements.

3.6.3.5 Final top cell

Finally, the mentioned aspects such as impact of Silicon substrate resistivity, substrate thickness, extra substrate elimination and tiling distribution are explored by the integration of all these variables in a BiCMOS 130 nm HR substrate. The final top cell is illustrated in Fig. 81 (a). 12 WR3 B2B circuits have been integrated considering three substrate thickness (75 µm, 50 µm and 25 µm), two substrate configurations (extra and non-extra substrate) and two tiling distributions. Also, two identical circuits to the WR3 B2B transition integrated in BiCMOS 55 nm (low-resistivity) with the two mentioned tiling distributions have been added to the top cell to compare the impact of the resistivity on the substrate.



(a) (b)

Fig. 81 (a) Top cell of BiCMOS 130 nm DOE. (b) Circuit layout description.

In total, 14 circuits have been integrated in a 17.22 µm² surface area. It must be noted that the circuit width (300 µm) is much smaller than the minimal dimensions allowed for conventional wafer dicing at this technology (~400 µm). Thus, femtosecond laser ablation will be used to singulate the circuit contributions from the Silicon die. To facilitate the laser ablation process, free-dummies sawing street paths have been traced in the top cell. To calibrate the laser position, aluminum alignment crosses have also been included. A more detailed description of laser sawing street and alignment crosses is shown in Fig. 81 (b). Finally, metal top labels have been made in MTOP (M6) layer to facilitate the identification of circuits after laser ablation.

3.7 Conclusions & Perspectives

In this chapter, state-of-the-art packaged solutions at RF frequencies have been firstly presented, highlighting the two main substrates used for packaging: organic and ceramic, which are used to enable high density packaging solutions aligned with the System-on-chip integration strategy. In terms of tight design rules and costs, the organic substrate seems to

take the lead thanks to high-volume production. In fact, this substrate has been massively used to support RF circuits below 100 GHz.

However, when further increasing in frequency, the associated packaging technology performance is limited. On one hand, interconnections such as wirebonds can be used up to 300 GHz and solder bumps are limited to the minimal thickness that can be achieved in substrate without cracking it. Concerning planar transmission lines, in IC routing, their insertion losses at high frequencies are manageable but for packaging routing it is not ideal. In consequence, non-planar structures such as SIW and SINDR waveguides have been studied but still rectangular waveguide routing seems to perform in terms of insertion loss. In fact, rectangular waveguide integration using CNC-machined metallic split-blocks is traditionally used to support most low-loss and high-power circuits at mmW and THz frequencies.

Nonetheless, the limitation associated with metallic module integration technology is firstly its high cost. In consequence, lower-cost packaging solutions have been proposed such as Silicon micromachining, 3D metallic impression, LTCC substrates and plastic molding. Secondly, is the lack of packaging automated process, since wirebond and die attach is made manually into the module. To solve this, previous works have proposed to integrate an organic laminate substrate on the metallic split-block, which is aligned with automated process and low cost. This leads to a Hybrid integration strategy using at the same time metallic split-block and organic laminate packaging technologies.

In this chapter, we have proposed to reduce the complexity of this integration strategy by elimination of copper pilar bumps, thus reducing costs since an extra fabrication step is removed. To validate the proposed integration strategy, a WR3 B2B WG-to-SSL transition was proposed, designed, and evaluated at BiCMOS 55 nm low-resistivity and BiCMOS 130 nm high-resistivity substrates. By comparing the proposed integration strategy to an equivalent full metallic split-block strategy, we noticed a difference of 1.2 dB in insertion loss due to spacing between the organic substrate and bottom split-block. Concerning the individual performances, both full metallic split-block package (IL ~1.8 dB) and hybrid package (IL ~3 dB) using HR substrate performances are competitive regarding the average insertion loss (complete module) reported in state-of-the-art publications (~2.8 dB).

In the end, a DOE is proposed to evaluate performances at IC level. We noticed the importance of the use of high-resistivity substrates, low thickness solution and concerning high thickness substrates the elimination of extra substrate. The tiling impact evaluation is limited due to the simulation capabilities, and it will be further evaluated at the measurement stage. Finally, the perspectives of this chapter are the implementation of the proposed integration strategy as well as the full metallic split-block integration to validate both packaging solutions.

Chapter 4
Design of 268 GHz BiCMOS SHMs

4.1 State-of-the-Art of Schottky SHMs > 200 GHz

In chapter 3, the use of metallic split-block integration strategy including CNC-machined rectangular waveguides has been recommended as the package solution of choice for ICs working at frequencies > 200 GHz due to low attenuation compared to planar transmission lines. In fact, this packaging solution is one of the favorites for THz frequencies due to the mentioned performances. One of the circuits that are packaged following this integration strategy is the Schottky diode SHM, which is the main element of the terahertz receiver front-end, widely used for applications such as remote sensing of the earth atmosphere, biomedical care, military security and wireless high speed communications [63]. An example of a conventional SHM using metallic split-block integration is illustrated in Fig. 82.

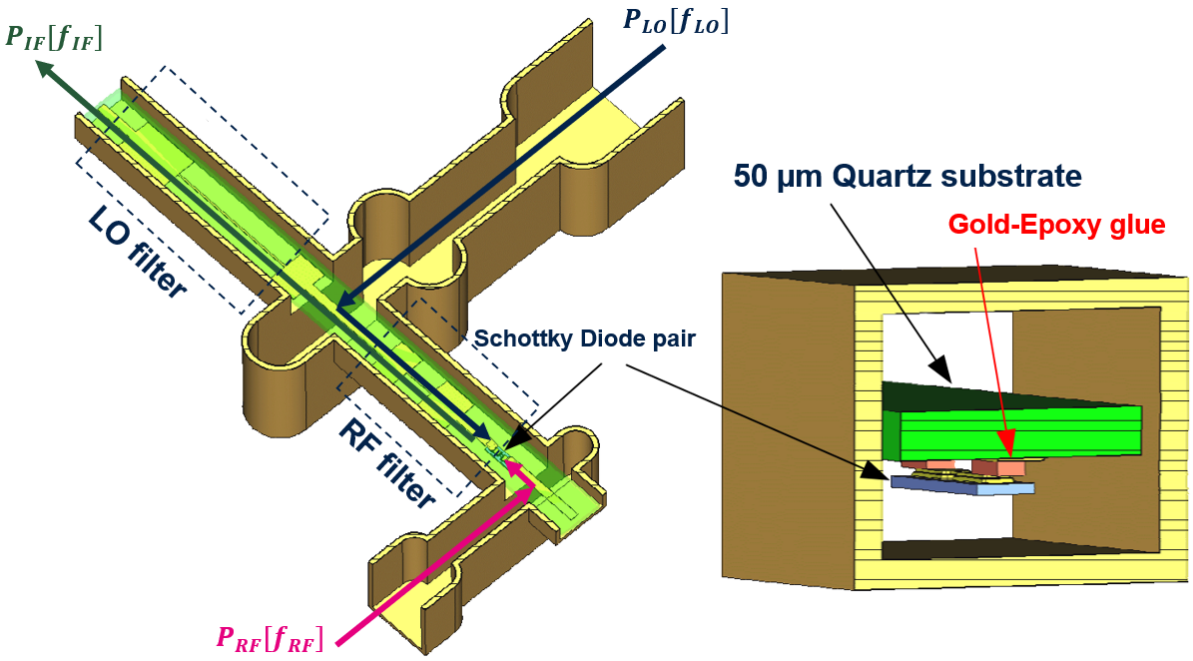


Fig. 82. A Flip-chipped 330 GHz GaAs Schottky diode SHM. Taken from [157].

Compared to Schottky diode SHMs below 100 GHz where planar transmission lines are used for RF and LO injection, the use of rectangular waveguides requires the modification of the overall integration strategy, starting by the addition of LO and RF waveguide-to-transmission line transitions in the circuit. For ease of integration with split-block metallic modules, E-plane extended RF and LO probes are used and integrated directly into the substrate [157]. Then, to ensure the proper guidance of RF and LO signals towards the Schottky diodes and IF signal to the output, two filters are integrated on the substrate: The RF and LO low-pass filters. The first one ensures that the RF signal is rejected just after coming out from the Schottky diodes. The second one ensures that the LO signal is rejected from the IF output and enters directly to the Schottky diodes. Finally, the IF signal can pass through both RF and LO filters (low-pass filters), and through LO waveguide since waveguides are naturally high-pass filters. Finally, thanks to high-pass RF waveguide behavior, the LO signal cannot leak into the RF waveguide. The block schematic illustrating the mentioned signal paths is presented in Fig. 83.

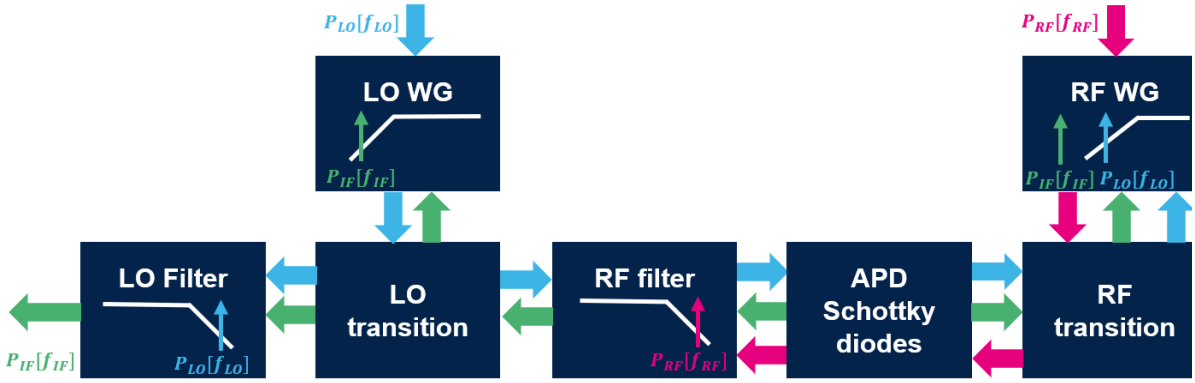


Fig. 83. Schematic block representation of different filters to form the desired RF, LO and IF signal path.

Due to improved performances, GaAs Schottky diodes are traditionally used as the non-linear element to generate the harmonics of THz Schottky SHMs. However, to take advantage of this aspect, the Schottky diode must be integrated carefully into the substrate. In fact, in order to optimize the whole mixer, the Schottky diode must be placed as close as possible to the RF waveguide to reduce the RF losses associated to the RF signal path in the planar transmission line, as illustrated in Fig. 82. Here, the Schottky diodes are flip-chipped attached to the quartz substrate thanks to epoxy conductive glue. To reduce even more the distance between the waveguide and the Schottky diodes, in [157] they have also proposed to insert the Schottky diode directly into the RF waveguide. However, this study showed that following this integration strategy the mixer is much more sensible to shift and epoxy glue thickness variations compared to a diode pair attached after the waveguide [157].

Another solution is to take advantage of GaAs monolithic integration technology to include the Schottky diode, filters, and waveguide transitions into the GaAs substrate achieving then monolithic integration. This eliminates the need of flip-chip anti-parallel Schottky diode integration. A description of reported SHM solutions between 170-400 GHz are presented in Table 13.

Ref.	Origin	f_{RF} (GHz)	P_{LO} (dBm)	RF BW (GHz)	FBW (%)	SSB CL (dB)	DSB T_{Noise} (K)	P1dB (dBm)
[63]	Research	198 - 238	4.9	40	18.3	< 10	692-924	0.6
[64]	Research	199-238	4.9	39	17.8	< 12.4	580-1059	0.9
[65]	Research	200-240	4.8	40	18.2	< 8.12	688 - 1034	-0.6
[66]	Research	208-229	6.3	21	9.60	< 9	500-1500	-1.5†
[67]	Research	290-310	4.8	20	6.67	< 10	1000 - 1500	N/A
[68]	Research	292-356	4.8	64	19.8	< 10	N/A	N/A
[69]	Research	300-360	4.0	60	18.2	< 7(DSB)	< 900	N/A
[70]	Research	320-340	4.0	20*	6.06	< 14*	N/A	N/A
[71]	Research	325-352	7.8	27	7.98	< 9	900-1500	N/A
[74]	Commercial	170-260	3.0-6.0**	N/A	N/A	< 8 (DSB)	600-1200	N/A
[74]	Commercial	220-330	3.0-6.0**	N/A	N/A	<8.5 (DSB)	700-1400	N/A
[74]	Commercial	260-400	3.0-6.0**	N/A	N/A	< 9 (DSB)	800-1500	N/A

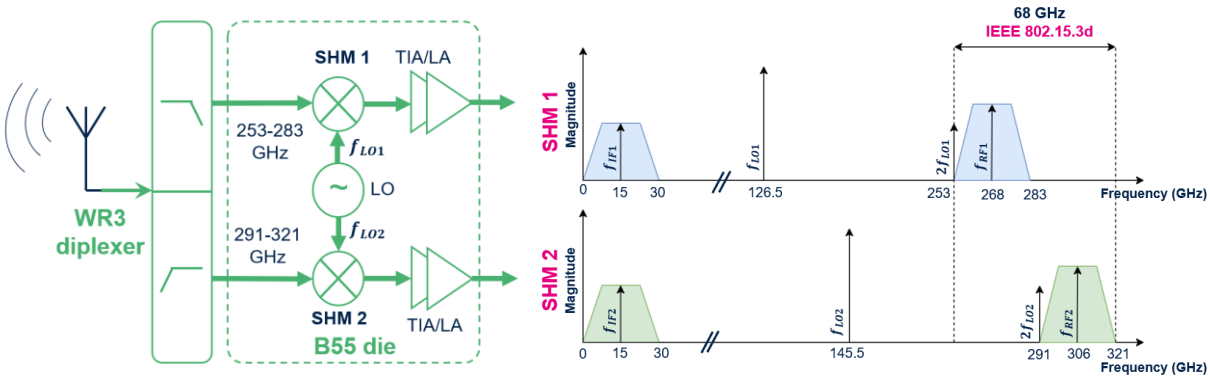
Table 13.Some state-of-the-art and commercial Schottky diode SHM above 200 GHz. *SHM with integrated image rejection filter. **Recommended LO power range. † Simulated.

Firstly, it must be highlighted that, to our knowledge, no Silicon Schottky diode SHMs have been reported at frequencies above 200 GHz. In consequence, only III-V based technologies have been reported so far. Moreover, the conversion loss of the different solutions is summarized in Table 13. However, this value is reported as SSB or DSB conversion loss. To simplify the comparation, SSB conversion loss is usually 3 dB higher than DSB conversion loss [64]. We can notice then that state-of-the-art SSB conversion loss is around ~8-14 dB with optimized LO power in the 4 dBm to 8 dBm range. Evermore, commercial Virginia Diodes SHMs achieves SSB conversion loss around 11-12 dB (adding 3 dB to the reported DSB value) with recommended LO powers around ~3-6 dBm [74]. This shows that recent state-of-the-art SHMs are aligned with reported commercial mixers in terms of achievable conversion loss.

4.2 SHM specifications targeting IEEE 802.15.3d

As mentioned in chapter 1, this thesis targets mixer-first receiver architectures to support the IEEE 802.15.3d standard, which fixes a continuous 68 GHz band that enables the transmission at high data rates in a power efficient manner. The choice of architecture, compared to a LNA + mixer topology has been justified based on the comparison of different budget link scenarios according to reported state-of-the-art performances of LNAs and mixers above 200 GHz. Hence, in chapter 1, we have demonstrated that based on the budgeted link, the addition of an LNA does not bring any improvement in comparison with a mixer first GaAs SHM architecture. Based on this logic, we propose to follow the same strategy but with the enablement of low-cost solutions by the integration of Silicon-based SHM, that have been previously presented in chapter 2.

Our starting point is the reported state-of-the-art GaAs SHMs. As noticed in Table 13, no GaAs Schottky SHM that supports the entire IEEE 802.15.2d band (253 - 321 GHz) has been reported so far. In addition, according to the state of the art, beyond 200 GHz the maximum achievable bandwidth of GaAs SHM is ~37 GHz. In consequence, this induces that a mixer-first receiver architecture requires to split the 68 GHz bandwidth of IEEE 802.15.3d standard into two sub-bands of 30-40 GHz each.



(a) (b)

Fig. 84. (a) Proposed circuit architecture to support the overall IEEE 802.15.3d band. (b) Demodulation strategy of 68 GHz band split into two sub-bands.

Consequently, the RF signal must be split via a diplexer, which is a passive component that realizes signal multiplexing in the frequency domain. It is composed of a power divider followed by two bandpass filters. In fact, a WR3 diplexer has already been reported based on coupled resonator structures in SU-8 machining technology [160]. However, due to imperfections of metal coating and the possibility of gaps inside the SU-8 layers, there is a difference of 7.6 dB (first bandpass) and 8.0 dB (second bandpass) between the simulations and measurements in terms of insertion loss, as well as a bandwidth narrower than expected. In consequence, we could think about the possibility to integrate a diplexer using metallic module technology with CNC machining which has been reported operating at lower frequencies such as D band (110 – 170 GHz) [161], or even at G band (110-300 GHz) [162], where a good agreement between simulations and measurements has been achieved.

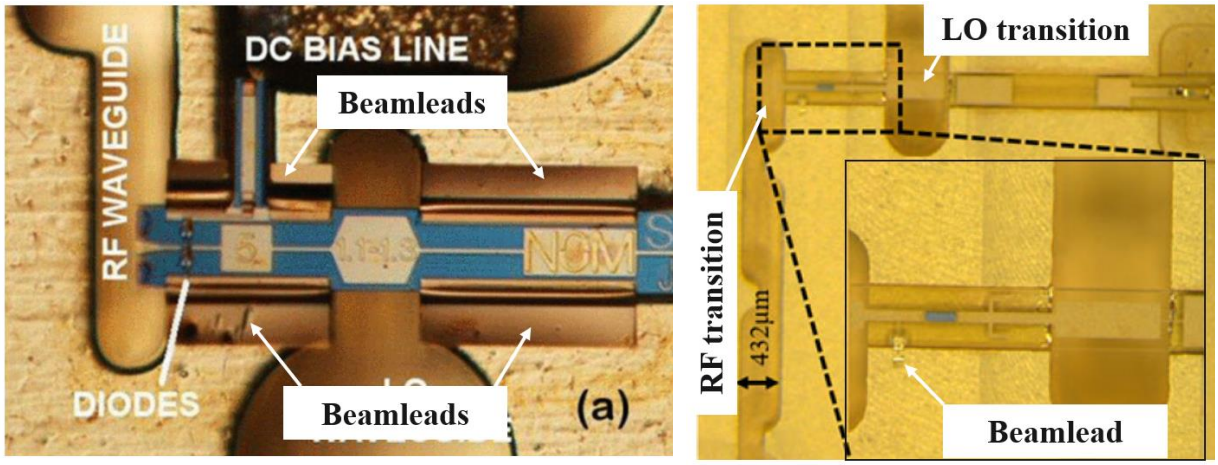
To integrate the diplexers with the SHMs, we propose to split the first 30 GHz band of IEEE 802.15.3d standard (253-283 GHz), which we will call the Low-band signal, and the last 30 GHz band (291-321 GHz), which we will call the high-band signal. An 8 GHz spacing between both bands has been defined to ensure proper transition between the low-band and high-band signals, targeting a reasonable isolation within the bandpass higher than 30 dB [160]. Then, two carrier LO signals are used at fundamental frequency of 126.5 GHz and 145.5 GHz with an expected LO power of ~5 dBm that can be easily achieved using multiplication chains for testing purposes or in a future fully integrated solution. This LO frequencies will enable to achieve 2x harmonics placed at 253 GHz and 291 GHz respectively, as illustrated in Fig. 84. Finally, both signal bands are shifted and downconverted in frequency between 0-30 GHz. To further extract the signals, a transimpedance amplifier (TIA) is used to amplify and convert the incoming diodes current signals into a manageable voltage level. As the starting point, we propose to study in this thesis just the first sub-harmonic mixer (SHM1).

4.3 Targeted SHM Module Integration Overview

4.3.1 GaAs SHMs traditional integration strategy

In this section, a more detailed description of state-of-the-art GaAs SHMs ICs integration on metallic split-block modules is presented. One of the first integration challenges is the DC/IF grounding of the circuit, which is necessary to ground the antiparallel Schottky diodes. One way to ground the Quartz/III-V substrate is by taking advantage of beamlead technology. This technology has been developed in the early 1960s by M.P Lepselter from bell systems [163][164].

Here, the "beams" are usually developed by electroforming a thick and self-supporting gold pattern on a thin film TiPtAu base. The supporting extra substrate below the beams was then etched leading to self-supporting beamleads. The advantage of this solution is that it serves at the same time as electrical structural and protective element. Concerning THz circuits such as frequency multipliers and SHMs (where beamleads are placed in the border of substrate), it simplifies the assembly procedure when mounting the IC into the metallic split-block [164], [165]. An example of the mention solution is illustrated in Fig. 85. (a) Here, the beamleads were fabricated using NASA Jet Propulsion Laboratory (JPL) planar diode process technology. Moreover, a ~5 µm GaAs substrate has been used. Furthermore, at lower frequencies, a much smaller beam-lead contact has been reported, as presented in Fig. 85. (b).



(a) (b)

Fig. 85. Different lateral-grounding strategies based on beamlead technology. (a) A 1.2 THz SHM with DC bias from [165] and (b) a 300 GHz SHM from [67].

As noticed, these grounding strategies are using lateral placement of the ground. However, one can think of placing the ground also at the longitudinal borders or inside the RF waveguide transition. In fact, in [155], they have shown an integration strategy solution compatible with metallic split-block integration where a built-in DC/IF return path is interconnected to the backshort of the RF waveguide and demonstrated for a 140 GHz frequency doubler. Other strategies go further by extending the substrate in the RF transition. However, for an extended waveguide probe it is better to use a half-reduced height waveguide to facilitate the matching between the extended probe and the waveguide [156]. In

fact, the use of an extended probe in a full-height waveguide have shown to not be useful for broadband transitions [166].

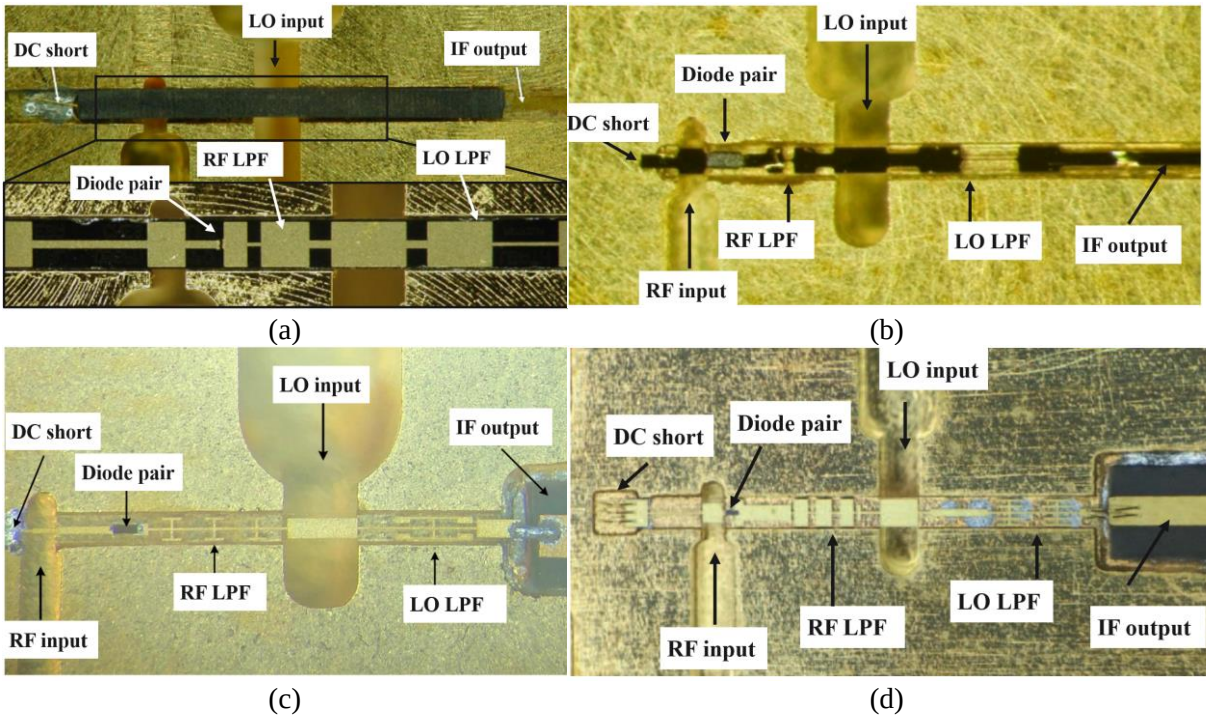


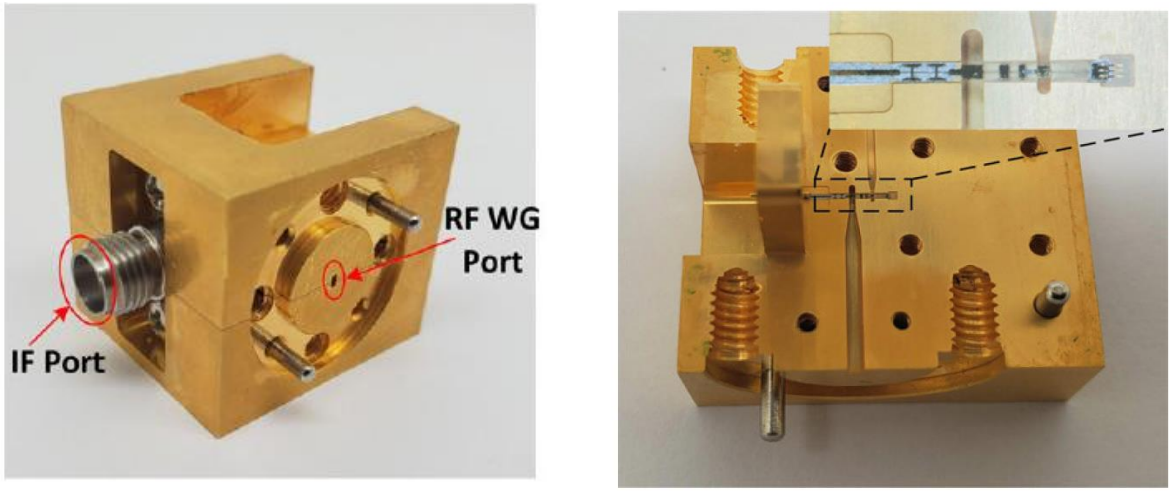
Fig. 86. Different longitudinal-grounding strategies for extended E-plane probes. (a) An inverted-chip 300 GHz SHM from [157], (b) A 664 GHz SHM using beamlead from [75], A 340-490 GHz SHM using epoxy glue from [167] and (d) A 220 GHz SHM using wirebonds for grounding from [66].

Following this ground placement strategy, different solutions have been presented in the state-of-the-art. Some SHMs providing a DC ground after the extended RF transition are illustrated in Fig. 86. Firstly, at the Fig. 86 (a) we can find a SHM integration in inverted configuration. One of the advantages of this solution is to provide a precise DC ground placement compared to its first counterpart where a mobile DC ground has been integrated in a non-inverted chip to optimize the position of the SHM [157]. Here, the SHM ground is connected to the bottom metallic split-block thanks to a conductive (gold) epoxy glue. Secondly, as presented previously in Fig. 85 (a), we can take advantage of beamlead technology to provide DC grounding before the RF transition (Fig. 86 (b)). Here, the beamlead is trapped between the top and bottom split-block without the use of glue and the chip has not been inverted.

Moreover, one can apply glue directly over the ground in a non-inverted position to facilitate the integration of the IC with the IF output. An example of this approach is showed in Fig. 86 (c). This solution remains like the one presented in [157] but in a non-inverted position. However, the inconvenience is that the quantity of conductive epoxy is complicated to control and have an impact in the impedance and electrical length characteristics of the line that interconnects the RF probe to the ground. This leads to deterioration of conversion loss, bandwidth and return loss [168]. In fact, in a SHM working between 170-190 GHz [168] this effect has been studied, leading to conversion loss variation between –3.758 dB and -0.018 dB in the overall RF band (in simulation). In consequence, it is proposed to integrate a low-

pass filter (LPF) close to the DC ground with the same cutoff frequency as the RF LPF. This leads the DC ground invisible for the RF transition. With this strategy, the conversion loss variation is reduced to -0.015 dB – -0.01 dB [168].

Finally, other solutions are proposed using bond gold wires which are also manually assembled between the metal ground pad in the substrate and the bottom split-block [63]. Moreover, the wires are placed in parallel to reduce the series inductance [101]. An example of this ground strategy is illustrated in Fig. 86 (d). The same bonding strategy can be used to interconnect the IC substrate with an exterior IF circuit. This IF circuit is used as an interface between the final connector in the split-block module to extract the IF signal and the IF output of the IC. When the circuit is monolithically integrated, an additional quartz transmission line is added since the IF/DC feeder is too small, leading it impractical to be interconnected with the exterior connector [71], [169]. However, other circuits which are already been made in Quartz can be interconnected directly to the IF connector, as illustrated in Fig. 87.



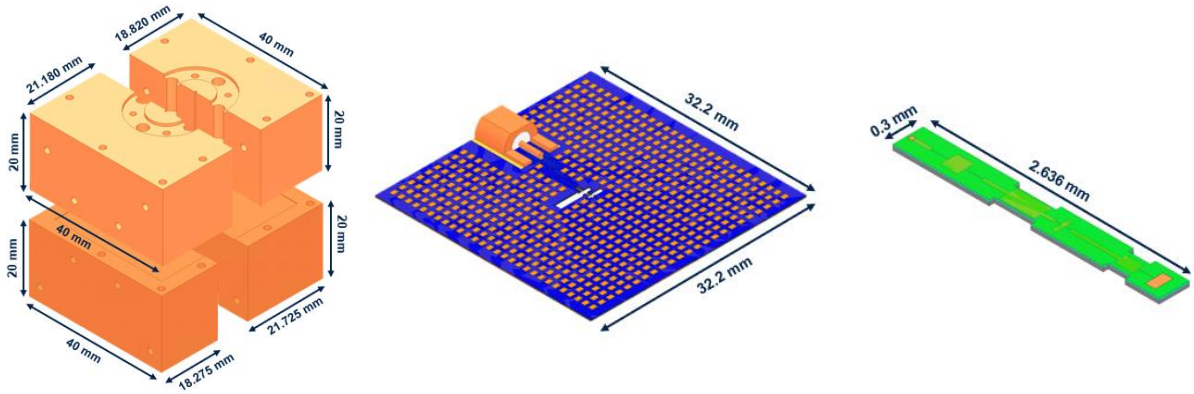
(a) (b)

Fig. 87. (a) Metallic split-block module for a 200-240 GHz SHM. (b) Bottom split-block and SMA connector. Taken from [65].

Usually, the connector used to extract the IF signal are flange-mounted jacks, due to the facility of integration with a split-block metallic module. This connector is fixed to the split-block by screws and interconnected to the circuit by a soldered pin [168]. Moreover, in function of the coaxial connector type, flange-mounted connectors can be used up to 110 GHz (1.0 mm connector) [170]. Although this connector is suitable for metallic split-block integration and show good performances, it is not aligned for applications where multiple testing of ICs are required, since the pin that interconnects the interface and the circuit must be soldered and desoldered multiple times from the module, resulting in a tedious maneuver [76]. In the next section we propose to solve this problem by replacing the type of connector.

4.3.2 Proposed hybrid integration strategy adapted for H-band Silicon SHMs

Motivated by the challenge of full metallic split-block integration high-volume manufacturing, in chapter 3, a hybrid integration strategy using organic laminate substrate has been proposed to leverage automation of die attach and wirebond process while preserving the split-block module advantage (good performances associated with machined-CNC waveguides). In fact, this integration strategy has shown promising performances by the integration of a full passive circuit where the organic laminate substrate has been used as a support element for die attachment. In this section, we propose to complexify even more the hybrid integration strategy with the integration of a 268 GHz SHM. Compared to the WR3 B2B transition, here the organic laminate substrate is required for the extraction of IF signal and DC grounding. In Fig. 88, the main elements constituting the mentioned integration strategy are presented.



(a) (b) (c)

Fig. 88. Main blocks composing the proposed integration strategy adapted for a SHM: (a)Metallic split-blocks, (b) organic laminate substrate and (c) Silicon integrated substrate.

Firstly, the main split-block module is illustrated in Fig. 88 (a). As the proposed integration strategy from chapter 3, the metallic module is split into 4 pieces to allow vertical and horizontal routing of waveguides while reducing the mechanical stress of the organic laminate substrate and ensure proper aspect ratio for ease of CNC machining. The top metallic block is split following the E-plane symmetry of the vertical RF waveguide and the bottom module following the vertical LO waveguide. The coupling of both types of waveguide routings (vertical and horizontal) are achieved thanks to H-plane bends.

The second element of proposed packaging assembly is the organic laminate substrate, illustrated in Fig. 88 (b) which will allow the Silicon SHM illustrated in Fig. 88 (c) to be attached properly and to extract the IF signal and fix the circuit ground. A more detailed description of the SHM circuit will be illustrated in section 4.4. To achieve the ground connection, four RF pads are placed in parallel (pitch of ~50 µm) to allow standard automated RF bonding and reduced parasitic inductance, contrary to the wire-bonded solutions presented in [63], [64], [65], [66], [171], where the wirebonds are attached manually from the IC to the split-block. An epoxy-glued DC ground has not been considered

either for this integration strategy since it is not compatible with standard Silicon package process. To remain compatible with Silicon assembly process, the wirebonds connected to the Silicon IC must be attached to an organic substrate and not directly to the metallic module. In consequence, open pads have been integrated in the organic substrate. The grounding process is illustrated in Fig. 89, where also the complete integration of all package elements is presented.

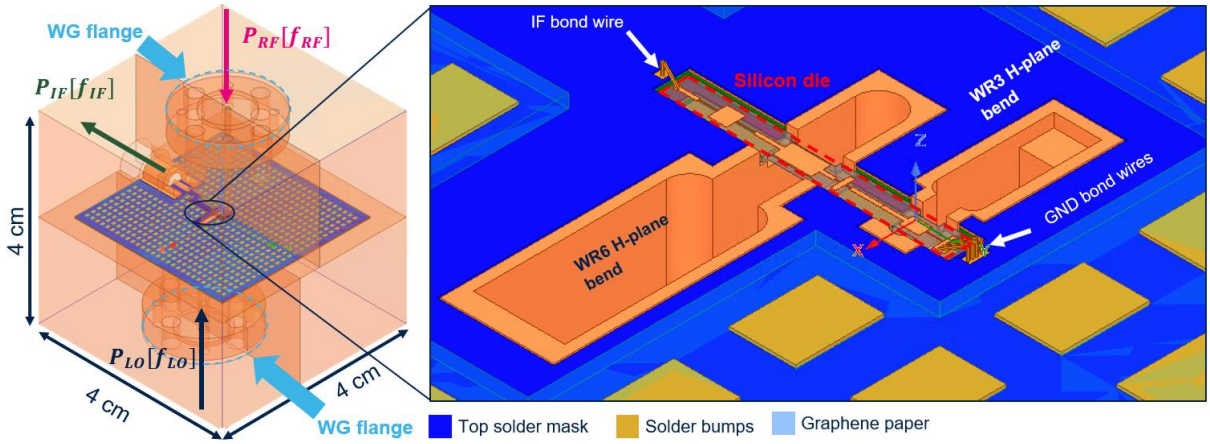


Fig. 89. Representation of the proposed integration strategy applied for a 268 GHz SHM.

The total dimensions (4cm x 4cm x 4cm) of the metallic module have been chosen to simplify its manipulation (more compact form factor was feasible). For the RF signal, a WR3 flange has been used, which covers the 220-320 GHz band, and for the LO signal, a WR6 flange transition is integrated covering the 110 – 170 GHz band. The RF signal is injected at the top of the metallic module and the LO signal at the bottom. For the IF extraction, since the IF connector cannot be directly assembled on the Silicon IC, we require an intermediary passive circuit to solve this interconnection issue. In this case, we use the organic substrate to create this interface. Firstly, a 100 µm x 100 µm pad is integrated on the laminate to allow wirebonding between the Silicon pad and the organic substrate pad. Then, a planar transmission line is synthesized between the IF pad and the associated connector footprint.

To extract the IF signal from the package module, a SMP (female) connector (reference 19S202-40ML5 [172]) is used. This connector has been chosen since it is a low-cost surface-mounted solution, which is ideal for a thin organic substrate and automated assembly. The fact that the connector is directly integrated on the substrate compared to flange-mounted connectors (which are fixed to the metallic module) allows the testing of multiples circuits easily, since no soldering-desoldering of the connector pin (when flange-mounted connector is used) is required. However, the metallic split-block module must be adapted to ensure the proper enclosing of the organic substrate with the soldered SMP connector. For this reason, a circular cavity has been added in the top split-block considering the SMP connector diameter error and the diameter of the SMP (male) incoming connector. Finally, the center of the SMP connector has been aligned to the cut-plane of the RF waveguide to facilitate the CNC machining process. In terms of performance, this connector is suitable for the targeted IF band of ~30 GHz since the band of operation is between 0 to 40 GHz [172].

Concerning the IF line, a microstrip line has been chosen. However, this requires the creation of a cavity at the top of the metallic split-block to avoid capacitive coupling between the top ground and the transmission line. In the same logic, the grounded top metal level has been placed far apart (~500 µm) from the microstrip line to avoid capacitive coupling, which will lead to modification of the characteristic impedance. These aspects were evaluated via electromagnetic simulations. The final IF line integrated into the organic substrate is illustrated in Fig. 90. Like the proposed solution in chapter 3, a 4-metal layer coreless organic substrate is used to create the channel that encloses the SSLs made in Silicon. To create the microstrip line, just the first and second metal levels are used to avoid large microstrip line widths.

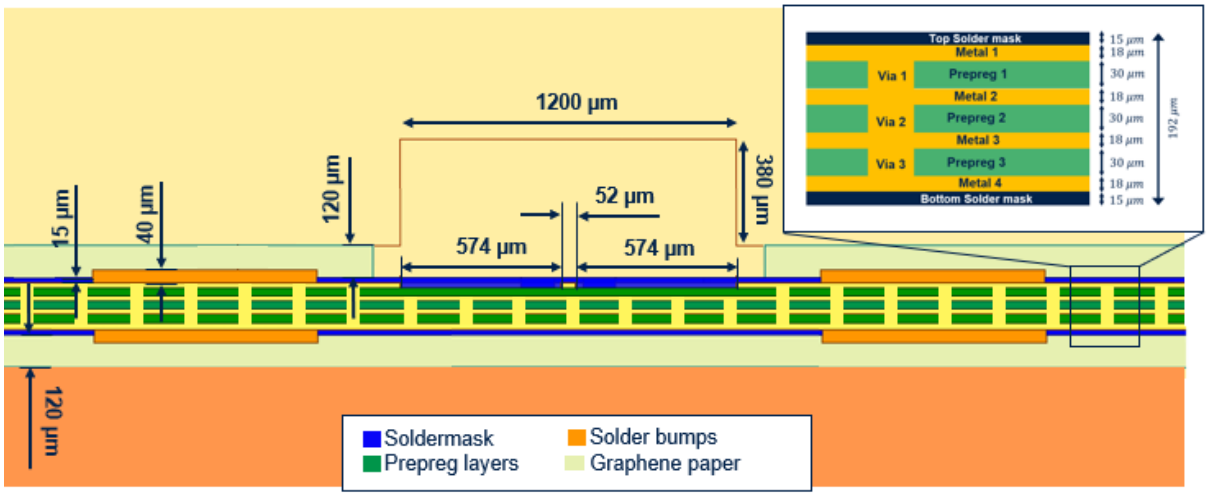


Fig. 90. Cut view of SHM module illustrating the IF line integration in a hybrid packaging solution.

Using synthesis equations of microstrip lines and considering a 30 µm Mitsubishi GHPL-830NS prepreg (Dk = 3.9, Df = 0.007 @ 10 GHz), a width of ~52 µm is required for a 50 Ω line. The impact of the microstrip line in terms of IF transmission will be evaluated in the design section. Finally, as the organic substrate from chapter 3, metallic vias are placed all around the board to ensure proper ground distribution. Also, solder bumps are placed in the top and bottom of the organic substrate as well as 120 µm deformable graphene paper to ensure proper grounding between the metallic module and the organic substrate.

4.3.3 Full metallic split-block integration adapted for H-band Silicon SHMs

For the SHM, we propose also a full metallic split-block integration like the one that has been presented in Chapter 3. The module is composed with several elements, that are illustrated in Fig. 91. Similar as in the WR3 B2B circuit, three metallic pieces are used: One main metallic split-block which is split following the E-plane symmetry of the horizontal waveguide (this forms the top and bottom split-block for the overall package, Fig. 91 (a)), and a standalone metallic block (in yellow, Fig. 91 (b)). The standalone blocks have been dimensioned to ensure that they can enter a wire-bonding machine (height ~5 mm). In addition, multiple of these blocks are fabricated to simplify the multiple testing of the SHMs.

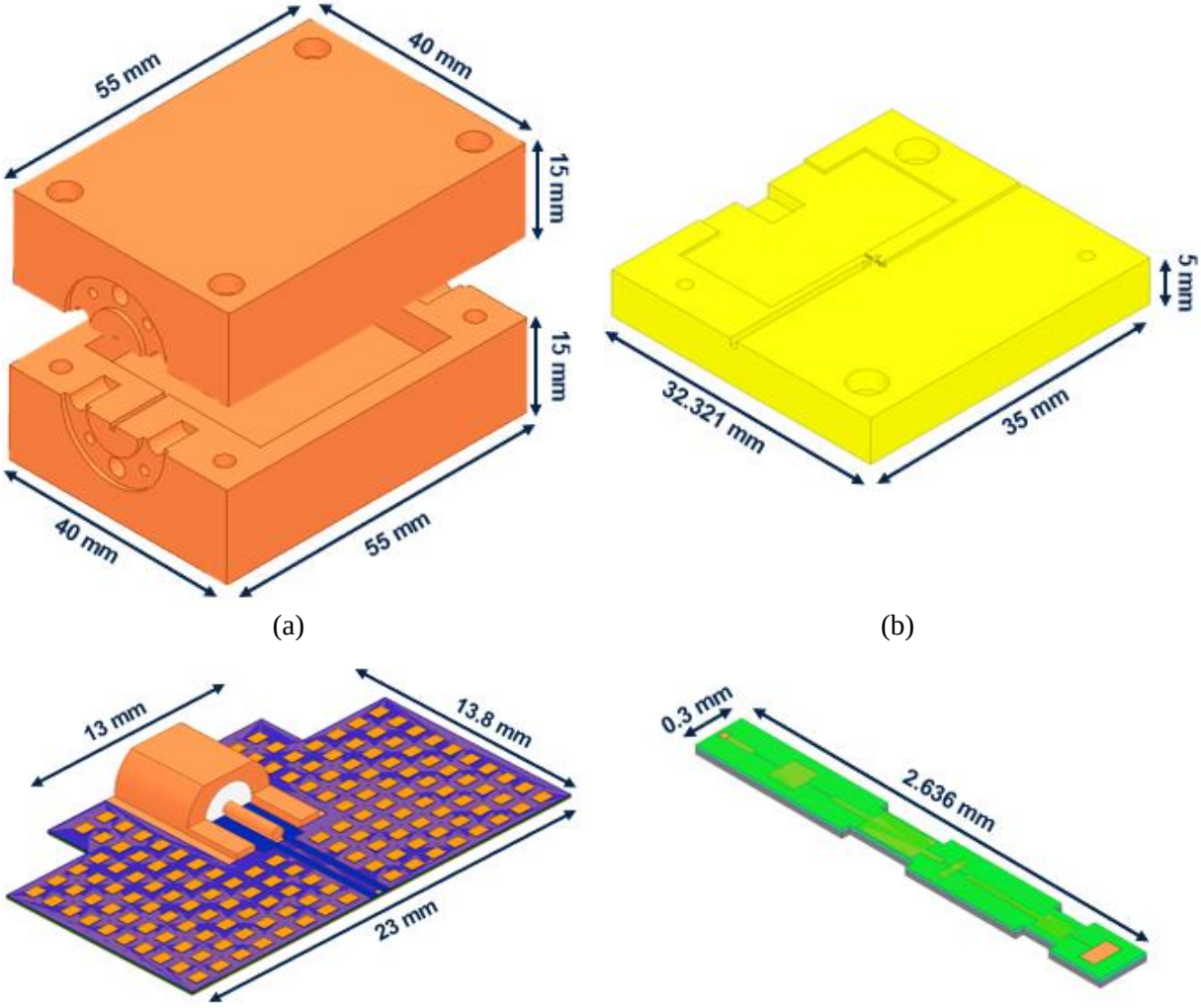


Fig. 91. Main blocks composing the full metallic split-block strategy adapted for a Silicon SHM: (a) Metallic-split-blocks, (b) standalone metallic block, (c) IF extraction PCB and (d) Silicon SHM.

To extract the IF signal, a PCB is used as illustrated in Fig. 91 (c). The difference between a PCB and an organic laminate substrate is the resolution of the design rules. For example, a commercial PCB can achieve dielectric thickness as small as 100 µm (~4 mils) [173] whereas an organic substrate can achieve much smaller thicknesses (in prepreg), such as 15 µm [118]. Concerning via diameters, smaller via hole (laser blind/buried vias technology) diameters in PCB in the range of 75-100 µm [173] can be obtained whereas in organic substrate (using laser µvia technology) via diameter down to 20 µm can be realized [124]. This explains the reason for using an organic laminate substrate to create the channel that encloses the Silicon SSL instead of a multi-layer PCB in the hybrid integration strategy. However, since the channel in full metallic split-block integration is made directly into the standalone metallic block, there is no need for a laminate substrate. In consequence, a simple two-layer PCB is used for routing the IF signal.

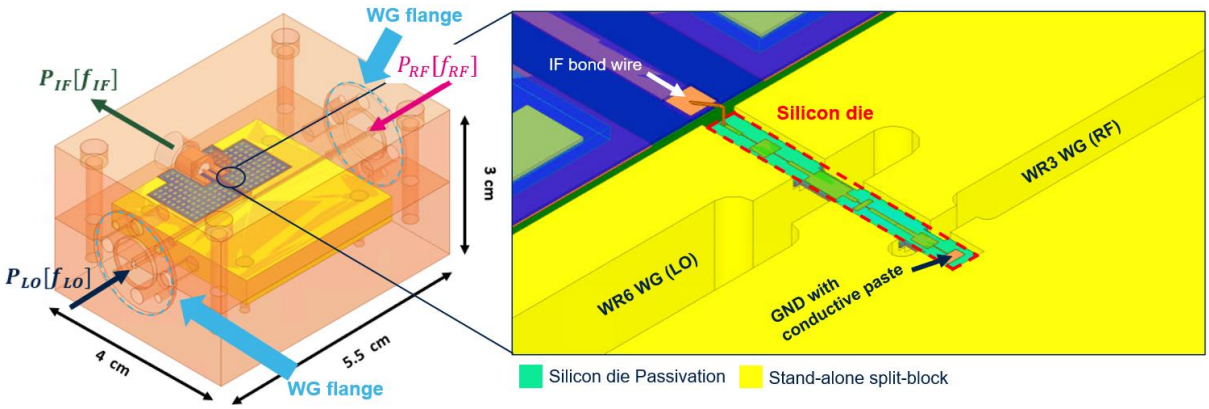


Fig. 92. Representation of the proposed full metallic package module[11] applied for a 268 GHz SHM.

To properly interconnect the waveguide inputs of the metallic block, a WR6 flange transition is integrated at the left of the main block (for LO signal) and a WR3 flange at the right (for RF signal). The placements of these flanges are illustrated in Fig. 92. Zooming into the split-block we can notice how the Silicon SHM is attached into the standalone split-block. For simplicity, we opted to fix the ground using conductive epoxy glue, as in [168], since a wire-bonding automated process as in hybrid package solution will be complicated (no organic substrate), as well as with manual bonding (wire-bonding pads are too small). However, this will need to anticipate additional conversion loss in the SHM due to variation of glue thickness. This will be evaluated in the next section. To interconnect the Silicon IC with the IF line in PCB, a wirebond is made between the Silicon open pad (~50 µm X 50 µm) and the PCB IF pad (300 µm X 300 µm).

A cut view of the IF line is shown in Fig. 93. A VT-47 PCB (Dk =4.27, Df = 0.016 @ 1 GHz) has been used due to its availability for fabrication process. The substrate thickness has been chosen as small as possible to not increase too much the line width compared to the hybrid package, which will require a modification of the top split-block cavity. Using Keysight ADS microstrip line calculator, a width of ~238 µm is computed for a 50 Ω line. For this line, the grounded top metal levels surrounding the IF line has been set with the same distance between them as in the IF line for the hybrid package, as well as the top channel enclosing the line. The impact of these aspects was evaluated via electromagnetic simulations and showed no relevant impact in the modification of the characteristic impedance of the line.

[11] Split-block package is quite larger (5.5 cm instead of 4 cm) than the Hybrid SHM package due to required extra material to insert the waveguide flange screws horizontally.

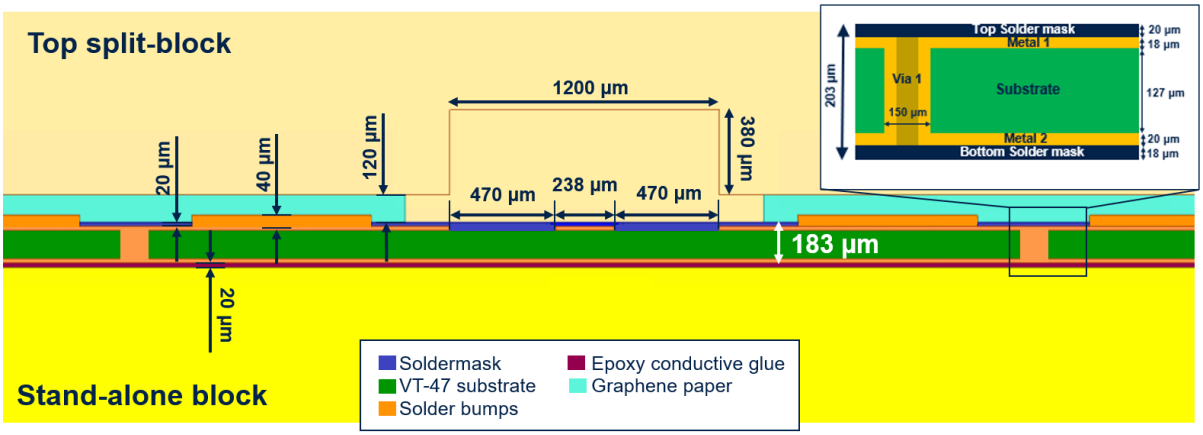


Fig. 93. Cut-view of SHM module following a full-metallic integration strategy, illustrating the IF line integration.

To ensure proper grounding between the PCB and the standalone block and top split-block, multiple vias have been stacked all around the board. Unlike hybrid package integration, the PCB is glued directly to the standalone block. This is necessary since the PCB and Silicon die must be fixed to a common non-mobile object (in this case the standalone block) to realize the wire-bonding process. However, the graphene is preserved as grounding strategy of the PCB at the top as well as the solder bumps.

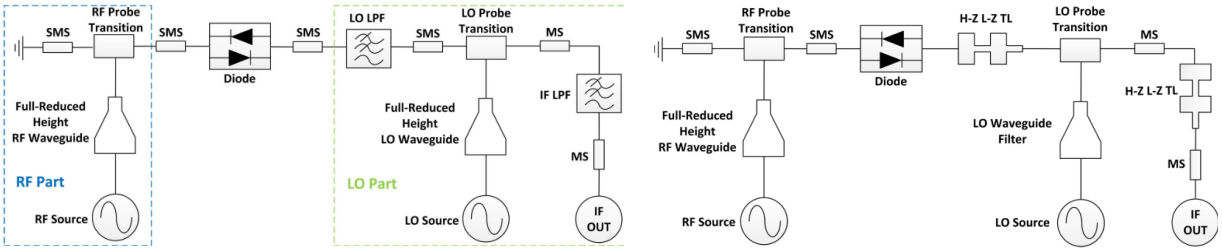
4.4 Design Methodology & Optimization Strategy

Exploring the literature on the design methods to achieve terahertz SHMs we can find different options. The most common ones are the Subdivision Design Method (SDM) and the Global Design Method (GDM), which are illustrated in Fig. 94. The first one requires initially the individual design of some passive functions such as the RF (or LO) and LO (or IF) filters[12]. Then, the complete RF and LO part are designed to achieve their specific desired performance. At the end, both blocks are matched to the diodes through suspended microstrip (SMS) transmission lines. Following this strategy, the impedance matching optimization variables are determined by the quantity of SMS in the circuit. The second one consists of the integration in simulation of basic circuits which are usually high/low characteristic impedance transmission lines and full/reduced height rectangular waveguides. Compared to the SDM, the GDM has more optimization variables which leads to longer optimization and simulation times [65].

In this logic, hybrid solutions [65] has been proposed leading to Half-Subdivision and Half-Global Design Methods (HS-HGDM) where a single functional unit circuit is designed (LO filter) by SDM and the rest of the circuit are designed by GDM. Depending on the optimization strategy, part of the passive functionalities/blocks are extracted from EM simulations and then integrated into an electrical simulator such as ADS for ease of optimization. However, all these design methods requires a diode model which represents the

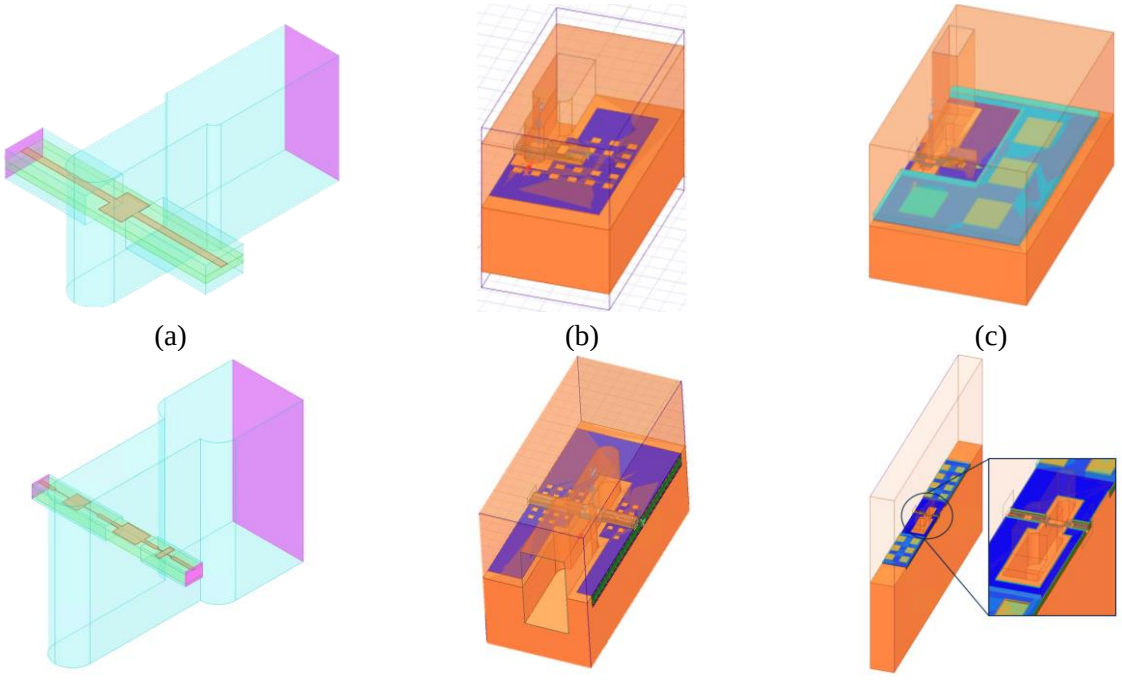
[12] In literature, sometimes it can be found the RF filter named as the LO filter, and the LO filter as the IF filter, as in the case of [65].

transition between the passive SHM functionalities and the antiparallel Schottky diode non-linear behavior. In the next section, the antiparallel Silicon Schottky diode integration into our SHM will be discussed.



(a) (b)

Fig. 94. Simplified model of state-of-the-art THz SHM based on the (a) SDM and the (b) GDM from [65].



(a) (b) (c)

(d) (e) (f)

Fig. 95. Different 3D models used for the optimization of the 268 GHz SHM. RF and LO blocks for preliminary model (a, d), preliminary package (b, e) and final hybrid package (c, f).

In this thesis we propose to follow an SDM strategy using preliminary EM 3D models of the RF and LO part. The mentioned structures are illustrated in Fig. 95. (a), (d). The first one consists of a grounded RF WG-to-SSL transition. To realize the ground, a perfect E boundary has been placed at one of the transition endings. The second one consists of the integration of the LO transition and the RF and LO filters. To achieve this structure, the RF and LO filters have been designed independently and then integrated into the LO transition. However, since the hybrid packaging process development has been made in parallel with the design of the SHM, different phases of circuit optimization have been performed to compensate the impact of the integration strategy on the performances of the final SHM. The different phases of optimization are shown in Fig. 96.

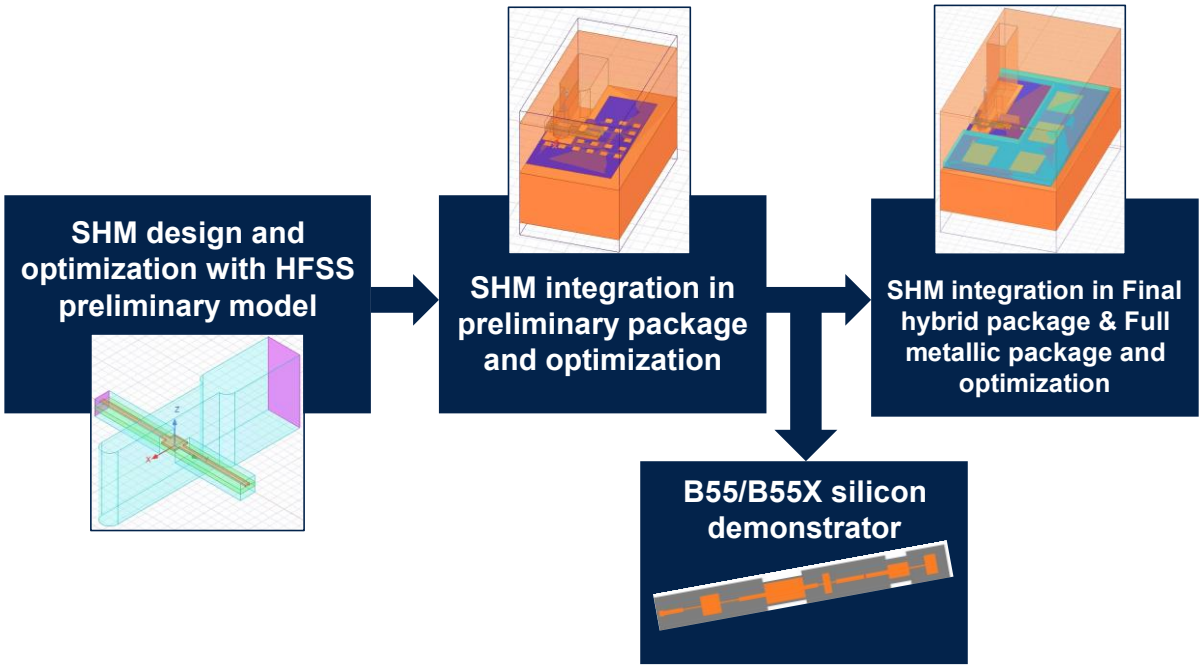


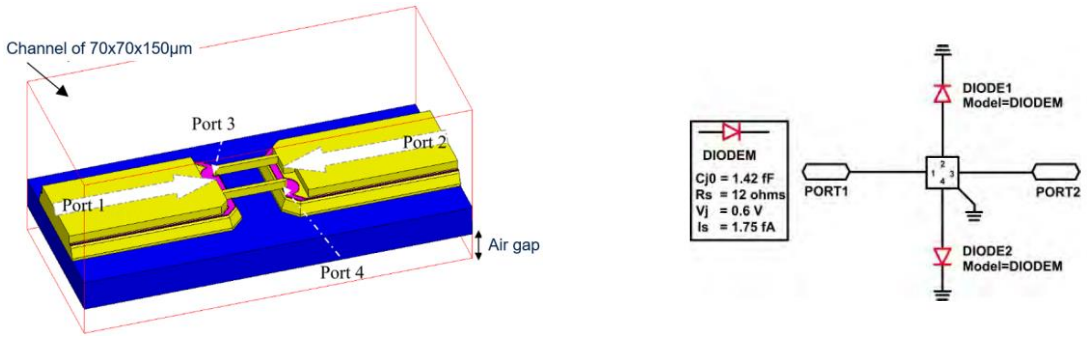
Fig. 96. Different phases of optimization realized for the design of the full SHM.

Firstly, a SHM optimization has been made considering the preliminary 3D model and a 100 µm HR substrate. Then, a preliminary integration strategy to support a first demonstrator in BiCMOS 55 nm technology considering a 100 µm low-resistivity substrate has been proposed. Here, elements such as extra Silicon substrate material for die attach, the integration of the DC ground and the elimination of the extra substrate in probes have been addressed. In the end, the final hybrid integration strategy defined in section 4.3.3 has been formalized and the final substrate thickness has been fixed to 50 µm. The difference between the optimization phase using the preliminary package and the final one concerns the optimization variables. In the preliminary package, the dimensions of the SSLs and the probes placement have been optimized whereas in the final package, since the SHM Silicon circuit was already delivered, just the probe placement has been modified.

Following the mentioned optimization strategy, a simplified 3D model for the RF and LO part has been developed for the preliminary and final hybrid integration strategy, as illustrated in Fig. 95. (b, e) and (c, f). The structure difference is that firstly the Silicon die is attached to the higher metal level of the organic substrate and the waveguides are routed horizontally.

4.4.1 Schottky diode integration in the proposed SHM

As mentioned, for the integration of the GaAs Schottky diodes into the SHM it uses an extrinsic EM diode model as interface. This model is used to capture the extrinsic parameters behavior at frequencies above 200 GHz [63]. An example of an extrinsic model for a Virginia Diode Anti-parallel diode configuration is illustrated in Fig. 97. (a). Here, ports 1 and 2 are used to interconnect the transmission lines and the other 2 (ports 3 and 4) to interconnect the anodes of the diodes to consider the non-linear behavior into the complete circuit. When it is possible, this structure is optimized to improve the conversion loss [75].



(a) (b)

Fig. 97. (a) 3D EM GaAs APD Schottky diodes peripheral model from [157] and (b) S4P electrical model and integration with diodes from [63].

After the simulation and extraction of the S parameters, the block is integrated into an electrical simulator (ADS for example) using classical diode models described in terms of their intrinsic parameters (zero-bias junction capacitance C_{j0} and series resistance R_s) and the forward voltage V_j and the saturation current I_S. Moreover, in GaAs technology the extrinsic parasitics of the diode are generally extracted using an EM simulation. However, applying the same strategy to the considered Silicon Schottky diodes is not straightforward. The main limitation is linked to the massively distributed nature of Silicon-based Schottky diodes.

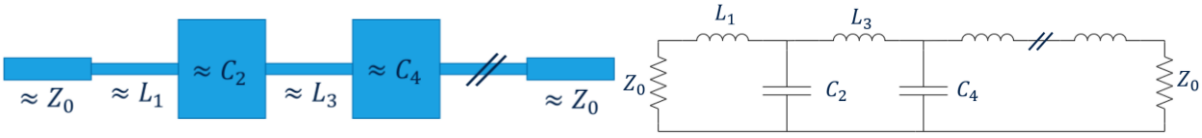
In Chapter 2, a description of the studied Silicon Schottky diodes has been presented and applied for a preliminary design of a W-band (75 – 110 GHz) SHM. Here, instead of using an EM model to reproduce the extrinsic parameters impact in performances, these parameters have been extracted from measurements and integrated into the electrical model. However, if an EM model is desired for applications above 200 GHz, we must consider that the presented Silicon Schottky diodes structures are interdigitated. This means that for a unique Silicon Schottky diode exist multiple Schottky junctions and ohmic contacts for a unique anode and cathode.

Consequently, the required EM simulation will need to support multiple anode and cathode fingers which leads to a far more complex set up that the one reported in Fig. 97 for GaAs technology (and one can raise the question of the validity of such a complex EM simulation keeping in mind the frequency of operation > 200 GHz). In contrast, a planar GaAs Schottky diode has a unique anode junction and a unique cathode junction which leads to a far simpler structure (even if one can wonder about the accuracy of such simulation at frequency > 200 GHz).

Moreover, in some cases [75], this Schottky diode integration strategy fails when it comes to comparing the simulation and measurements of the overall SHM, since it does not capture all the elements associated to the packaging process, such as the epoxy glue used and the eventual diode misalignments. In this logic, we can take advantage of our proposed hybrid integration strategy which allows the integration of multiple circuit version to propose a DOE including the same passive circuit and different Schottky diodes with different anode surfaces. This strategy has already been explored for the adaptation of Silicon Schottky diodes into rectennas working at 1.8 THz, 2.5 THz and 3.1 THz [41].

4.4.2 LO and RF filtering: SSL stepped-impedance low-pass filters

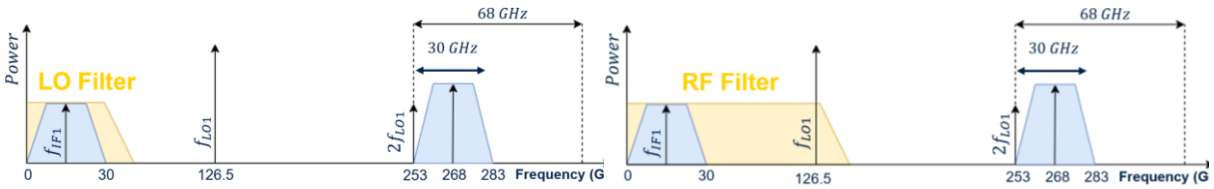
If we explore the different filters that are used for LO and RF signals management in Schottky diodes SHMs we can find diverse options. Traditionally, the low-pass step impedance filter is one of the most used thanks to its simple structure and simple design procedure [68], [75], [168]. However, due to their long size, other options such as low-pass compact microstrip resonators (CMRs) [168] and compact suspended microstrip resonators (CSMRs) [65] have been proposed as smaller physical-size solutions. Moreover, in some publications, they go even further by the use of band-stop filters (BSFs) and symmetrical open stubs [68], as well as hybrid solutions using RF BSF and LO step impedance filter [67]. In this thesis, we propose to start by the traditional filtering option using stepped-impedance filters due to the mentioned advantages.



(a) (b)

Fig. 98. The stepped impedance filter. (a) Distributed elements equivalence and (b) equivalent circuit with lumped elements.

The mentioned stepped-impedance filter is illustrated in Fig. 98 (a). The filter consists of alternated microstrip or striplines with different widths, which translates into sections of very high and very low characteristic impedances. The equivalent circuit of the filter is illustrated in Fig. 98 (b). A transmission line with a large characteristic impedance Z_H and short electrical length ($\beta l < \pi/4$) can be approximated by a series inductor. For the case of a short characteristic impedance Z_L and short electrical length it gives as equivalent element a shunt capacitor. This leads to a low-pass filter. To achieve the best performances, the values of characteristic impedances Z_H and Z_L are usually set to their maximal and minimal values that can be practically fabricable (considering the associated attenuation constants), which can be quantified by the Z_H/Z_L ratio. Finally, the length of the transmission lines can be optimized to have the best frequency response at the desired cutoff frequencies.



(a) (b)

Fig. 99. Desired (a) LO and (b) RF filtering in SHM1.

The first design step consists of identifying the required specifications aligned with our SHM1 circuit. An illustration of the desired filtering behavior is illustrated in Fig. 99. Considering that the stepped-impedance filter transition from passband to stop-band is not as sharp as other filtering solutions [77], we decided to anticipate any rejection issue by placing the cut-off frequency of the filters as close as possible to the signal that needs to pass. Another solution could be to increase the filter order. However, this will increase the filter

total length thus increasing insertion loss. In this logic, the LO filter cut-off frequency is placed around ~30 GHz (close to IF higher frequency) and the RF filter cut-off frequency at ~127 GHz (close to LO frequency). This defines our passbands. The starting rejection band values for LO frequency and RF band are obtained by the reported stepped-impedance filter performances in state-of-the-art [75]. The final specifications for both filters are resumed in Table 14 and Table 15. Based on reported state-of-the-art stepped-impedance filters for Schottky SHMs we found that a 3rd order filter in π configuration (High-Low-High) seems reasonable as a starting point.

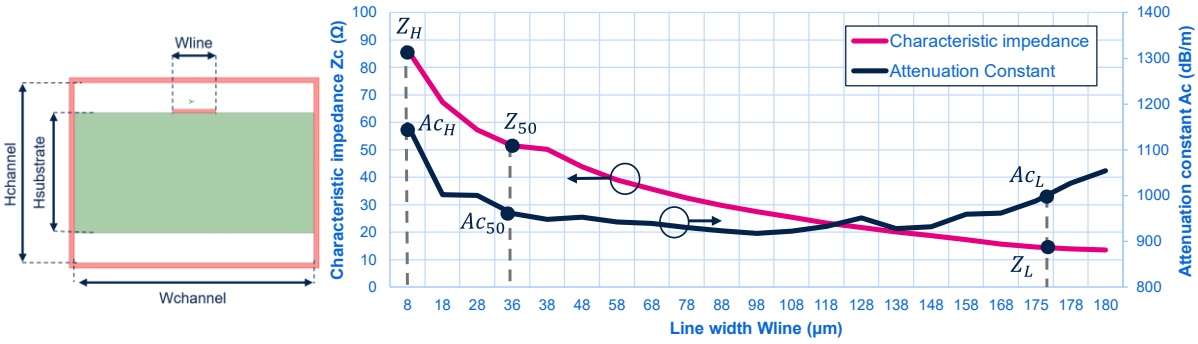
Passband	**$\|S_{21}\|$ @ passband**	**$\|S_{21}\|$ @ f_{LO}**	**$\|S_{11}\|$ @ passband**
0-30 GHz	> -0.5 dB	≤ -10 dB	< -10 dB

Table 14. LO filter preliminary specifications for SHM1.

Passband	**Stopband**	**$\|S_{21}\|$ @ passband**	**$\|S_{21}\|$ @ stopband**	**$\|S_{11}\|$ @ passband**
0-127 GHz	253-321 GHz	> -1 dB	≤ -10 dB	< -5 dB

Table 15. RF filter preliminary specifications for SHM1.

After the definition of the filter's specifications, the second step is to specify the type of transmission line to be used. Based on the defined integration strategy in chapter 3, a microstrip line can also be integrated instead of a SSL. However, in this thesis we are motivated to use SSLs compared to microstrip line since the associated losses are lower. The characteristic impedances that can be synthesized with the selected transmission line (assuming a 100 µm HR Silicon substrate) are illustrated in Fig. 100 (b). These values, as well as the attenuation constants (at 268 GHz) have been extracted by EM simulations using the model shown in Fig. 100 (a).



(a) (b)

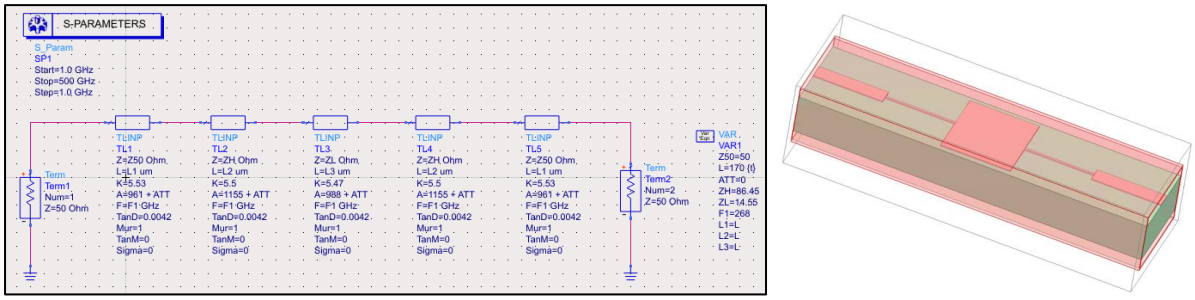
Fig. 100. (a) Front view of the SSL used for preliminary filters design. (b) Extracted characteristic impedance and attenuation constants at 268 GHz.

The third design step is to synthesize the filter. As mentioned before, the high and low characteristic impedances Z_H and Z_L are determined by the realizable transmission lines and their associated losses:

- In the one hand, the high transmission line width (Z_L) has been chosen considering the width of the channel that encloses the Silicon die (200 µm x 150 µm). This choice of channel dimensions will be explained in the next section concerning the RF block

optimization. In conclusion, a maximal width of 175 µm has been considered, leading to a space of 15 µm for eventual laser ablation.

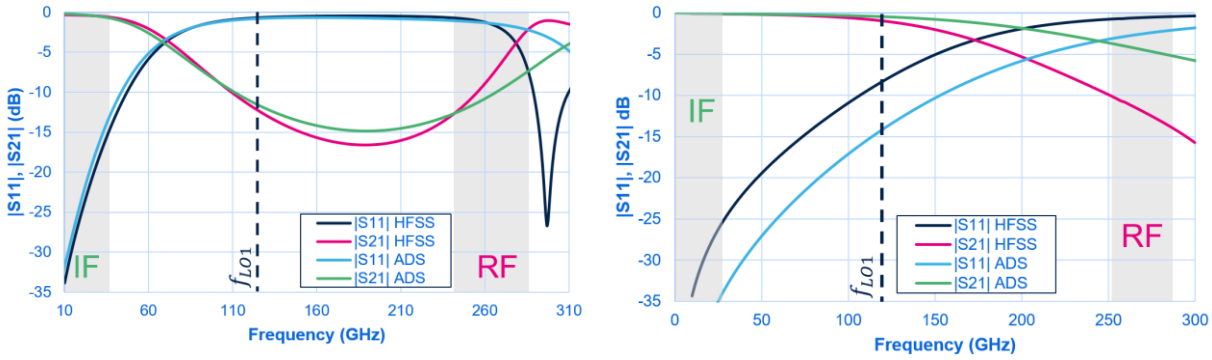
- On the other hand, the minimum line width (Z_H) has been considered in terms of losses. In fact, in BiCMOS 55 nm technology, the metal top level can achieve widths < 1 µm, which are scale comparable with a SiO2 substrate with ~18 µm of thickness. However, in SSL configuration where a ~100 µm Silicon substrate is used instead, the associated losses are much higher. Therefore, a width of 8 µm seems reasonable based on the presented attenuation in Fig. 100 (b). These final line widths lead to a $Z_H = 86.45\ \Omega$ and $Z_L = 14.55\ \Omega$ at 268 GHz. Moreover, for W = 36 µm, $Z_{50} \approx 50\ \Omega$.



(a) (b)

Fig. 101. (a) RF and LO filter model to extract optimal SSL lengths. (b) 3D model of LO filter in HFSS.

The fourth design step consist of making a preliminary simulation in ADS to tune the value of line lengths. For ease of optimization, all lines have the same length. The values of attenuation constant and characteristic impedance (Fig. 100 (b)) and the effective dielectric constant extracted from EM simulations are added to a complete transmission line model. One can directly use an SSL ADS model (SSLIN); however, it is lossless. In consequence, we opted for a TLINP model. The Df value was calculated based on the HR substrate resistivity. The final 3rd order filter model integrated in ADS is shown in Fig. 101 (a). After tuning, we found that the best value of line length L for LO filter is 170 µm. However, identifying a tradeoff between rejection and passband attenuation values is more complicated. In fact, the used ADS filter model does not reproduce all effects such as impedance dispersion and the steps between one line to another. In consequence, in the state-of-the-art [75] (following a GDM strategy), the extracted impedance steps models from EM simulations are extracted and integrated into the ADS filter, and the filter is divided into different bands of operation, leading to a complicate ADS final filter model. In consequence, we opted to reproduce directly both LO and RF filters in HFSS simulator, using the model illustrated in Fig. 101 (b) and the line lengths preliminary tuned.



(a) (b)

Fig. 102. Preliminary design using ADS and HFSS simulators for (a) LO filter and (b) RF filter.

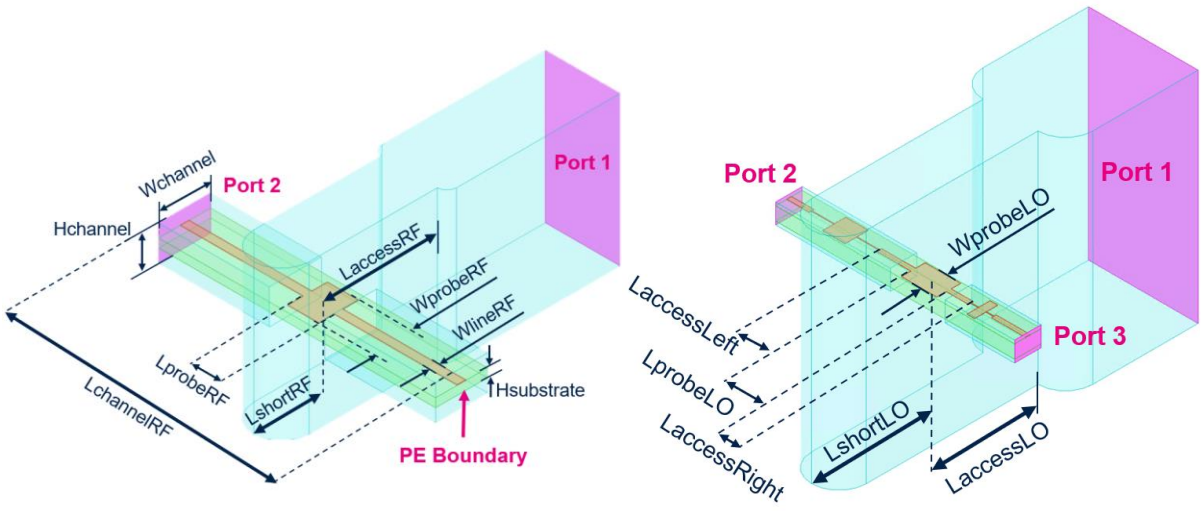
The final optimized values are illustrated in Fig. 102. Concerning the LO filter, in IF passband, $|S_{21}| > -0.47$ dB and $|S_{11}| < -18.6$ dB. At f_{LO}, $|S_{21}| > -12.52$ dB. Concerning the RF filter, $|S_{21}| = -1.15$ dB at f_{LO} and $|S_{21}| < -10.2$ dB at RF band. The mentioned values are obtained using HFSS simulation. The final line length for the RF filter is 48 µm. In conclusion, if we compare with Table 14 and Table 15, we can notice that we are aligned with the targeted performances.

Finally, the substrate thickness and resistivity used for filter design does not correspond to the final values defined for the integration strategy (50 µm). In fact, for the first SHM1 demonstrator, the complete design is based using a 100 µm Silicon substrate thickness since this first demonstrator is based on a preliminary integration strategy. However, in terms of filtering, this does not represent a major problem since the cutoff frequency position depends mainly on the transmission lines length. Concerning the values of characteristic impedance, their values will change, but the ratio Z_H/Z_L will remain barely constant since Z_H and Z_L will decrease at the same rate. However, the filter port impedance will change so a final optimization was made with the split-block mechanical model.

4.4.3 RF and LO WG-to-SSL extended transition design & filter integration

In this section, we will focus on the RF and LO blocks optimization, following the mentioned design method in Fig. 96. Based on the simplified model, we can illustrate in Fig. 103 the different optimization variables for both blocks. Firstly, we will start with the optimization of the RF block, illustrated at Fig. 103 (a). As mentioned before, the substrate thickness (parameter Hsubstrate) for the preliminary model simulations will be fixed to 100 µm. The LprobeRF parameter represents the distance between the center of the probe and the backshort and LaccessRF parameter represents the distance between the probe center to the reduced-height-full-height waveguide transition. To emulate the impact of the CNC machining process, the backshort has been modeled as a semi-circle. The E-plane RF probe dimensions are WprobeRF and LprobeRF respectively. To model the suspended line that interconnects the DC ground to the RF probe, two SSLs of length LaccessRF/2 have been integrated. Two waveguide ports (not normalized to 50 Ω) have been placed at the full height waveguide and to one of the channel ends. Finally, it must be noticed that the line that is

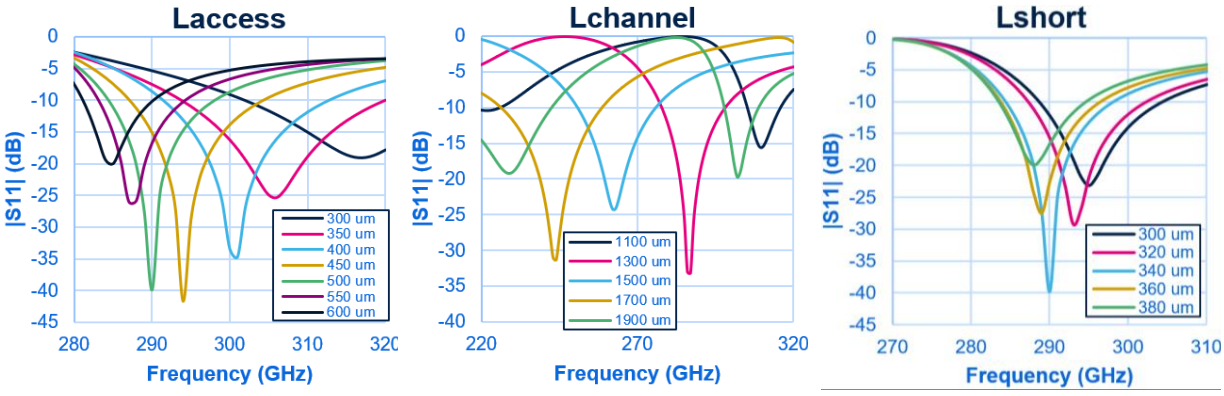
between port 2 and the E-plane RF probe is transparent for the simulation, as well as the full-heigh waveguide length.



(a) (b)

Fig. 103. Optimization variables for the preliminary (a) RF block and (b) LO block.

The first step is to identify the impact of each design variable in the transition performances. From simulations, it has been identified that Laccess and Lchannel have a considerably impact on the central frequency of operation and the setting of the bandwidth of the transition. On the other hand, Lshort impact is less important in terms of frequency placement, which allows a fine frequency matching. This can be illustrated by a preliminary simulation using a quartz substrate with thickness Hsubstrate of 100 µm enclosed in a 300 x 200 µm channel (Wchannel x Hchannel), in Fig. 104.

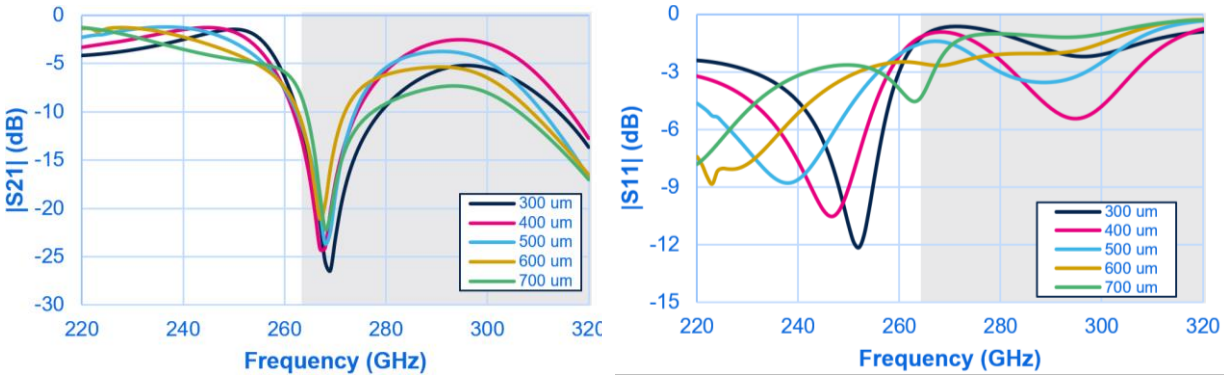


(a) (b) (c)

Fig. 104. Impact of $|S_{11}|$ (dB) of RF block while varying (a) LaccessRF, (b) LchannelRF and (c) LshortRF for a 100 µm Quartz substrate enclosed in a 300 x 200 µm channel.

However, while making the transition from quartz substrate to HR Silicon substrate, we can notice that the same optimization strategy using Lchannel, Laccess and Lshort to center the RF frequency is not enough while maintaining the same 300 x 200 µm channel dimensions. This can be illustrated in Fig. 105, where Laccess is swept between 300 µm – 700 µm. Although this variation, the centering of RF frequency to 268 GHz is not achieved. A similar behavior happens with Lchannel. This is due to the high equivalent dielectric constant in the

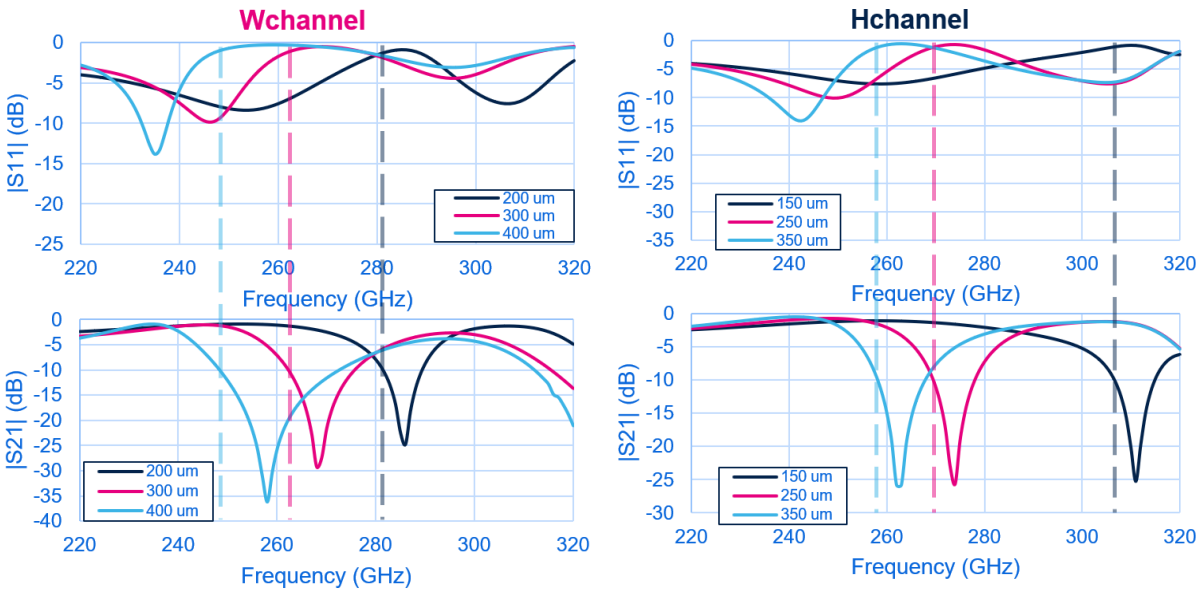
channel due to the Silicon substrate. To solve this problem, we decided to reduce the channel dimensions (Wchannel and Hchannel) which will lead to a smaller equivalent dielectric constant. It must be noted that other parameters play a key role in the variation of the effective dielectric constant such as the substrate thickness Hsubstrate and the line width WlineRF. However, the final substrate thickness will be determined to fit in the final channel configuration defined for the hybrid package (Fig. 67) and the line widths for the desired line impedances.



(a) (b)

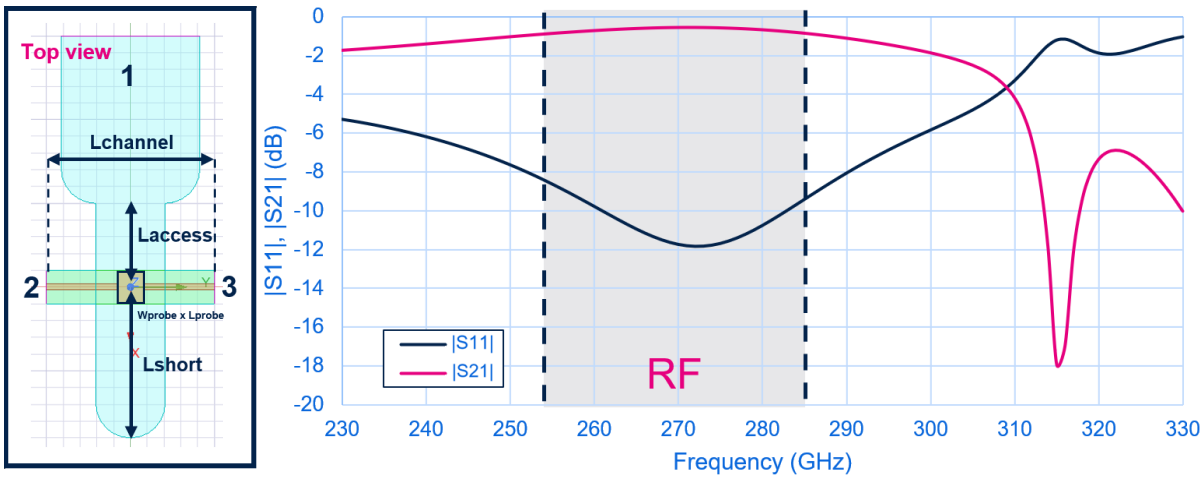
Fig. 105. Impact of (a) $|S_{11}|$ (dB) and (b) $|S_{21}|$ (dB) while varying Laccess for a 100 µm HR Silicon substrate enclosed in a 300 x 200 µm channel. LchannelRF = 400 µm.

The impact on $|S_{11}|$ (dB) and $|S_{21}|$ (dB) in the RF transition while varying the channel dimensions is illustrated in Fig. 106. As mode of illustration, if we define a $|S_{21}|$ reference limit of –10 dB (placement of dotted lines with respect to $|S_{21}|$ in Fig. 106), we can notice that the reduction of the channel width as well as the height increases notably the transition bandwidth. However, due to the modification of the effective dielectric constant, the quality of the impedance matching (value of $|S_{11}|$) is slightly reduced. This can be adjusted by the optimization of the probe dimensions, Lshort length and the line width. Based on these simulations, we decided to reduce the channel dimensions. However, a smaller channel will lead to a Silicon die geometry that is not practically realizable and complicated to package. Considering this aspect, we fixed Wchannel to 200 µm and Hchannel to 150 µm. These are the dimensions considered for the previous filters design, considering at the same time the excitation of non-desired waveguide modes in the channel.



(a) (b)

Fig. 106. Impact of channel width (Wchannel) and height (Hchannel) in the RF transition including a 100 µm HR Silicon substrate.



(a) (b)

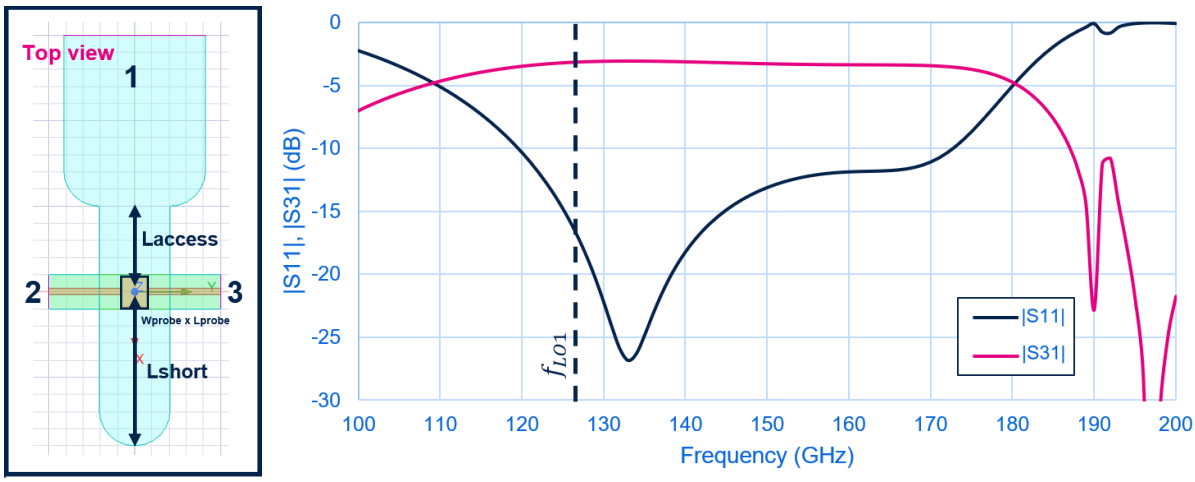
Fig. 107. (a) Top view of 3D preliminary model for the RF transition with a Silicon HR 100 µm substrate. (b) Simulation results.

Considering the selected channel dimensions, a final optimization has been performed leading to the preliminary RF transition performances illustrated in Fig. 107. (b). At the end of the optimization process, insertion loss below ~1 dB and $|S_{11}|$ below -8 dB have been achieved in the 253-283 GHz frequency band. If we extend the frequency band, insertion loss is below 2 dB between 230 – 300 GHz. The preliminary parameters for this first RF block optimization for Hsubstrate = 100 µm (Silicon die thickness) are illustrated in the Table 16. The height of the reduced-height waveguide remains ½ of the total waveguide height (216 µm) and has not been considered as an optimization variable since it is considered as a configuration already optimized for an extended E-plane to waveguide transition. Finally, WlineRF has been initially fixed to the corresponding width for a 50 Ω line.

LaccessRF	LshortRF	LchannelRF	WprobeRF	LprobeRF	WlineRF	Wchannel	Hchannel
350 µm	250 µm	450 µm	180 µm	180 µm	36 µm	200 µm	150 µm

Table 16. RF block final optimization values using the preliminary 3D model.

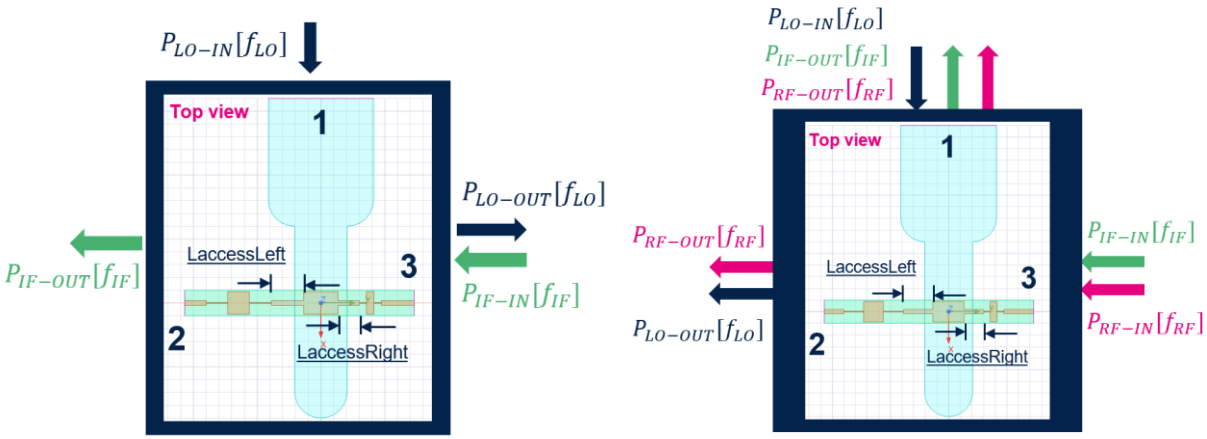
Secondly, we will focus on the optimization of the LO block. Following the SDM strategy, we start with the LO transition and then the LO and RF filters that have been previously realized will be integrated. The LO transition preliminary model is very similar to the RF transition, but it has two main differences: Firstly, it is scaled for a WR6 frequency band operation and three waveguide ports are integrated instead of one. For this reason, Laccess is not considered initially as an optimization variable since the lines between the port 2/port 3 and the reduced-height waveguide wall are transparent for the simulation. For this block, based on what has been observed from the previous one, LaccessLO has been optimized to center the LO frequency and the LshortLO, WprobeLO and LprobeLO to achieve a final $|S_{11}|$ < - 15 dB.



(a) (b)

Fig. 108. (a) Top view of 3D preliminary model for the RF transition with a Silicon HR 100 µm substrate. (b) Simulation results.

The results of the preliminary simulation of the LO transition are illustrated in Fig. 108. For this simulation, $|S_{31}|$ = -3.15 dB at LO frequency (~127 GHz). Due to symmetry, LO transmission from port 1 to port 2 and 3 ($|S_{31}|$ and $|S_{21}|$) are equal. In consequence, the LO power is divided into the two ports since no ground has been placed. This illustrates the difference in terms of simulations between the RF transition, which have a perfect E plane ground in one of the endings, whereas in LO transition this is not the case.

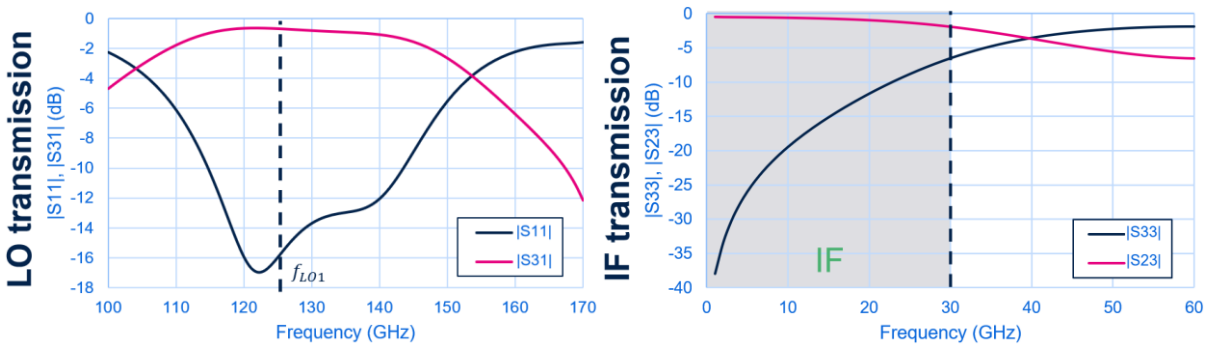


(a) (b)

Fig. 109. LO/RF filters + LO transition blocks in (a) transmission mode and (b) rejection mode for preliminary blocks.

Now, the RF and LO filters that have been previously designed in section 4.4.2 are integrated into the LO transition. This will lead to the complete LO block. The signals that will be evaluated in transmission and rejection mode in the LO complete block are shown in Fig. 109. Two SSLs are used to interconnect the probe to the filters. Their width has been fixed to 36 µm (50 Ω characteristic impedance) to match the filter impedance with the LO probe. Here, their respective lengths, LaccessLeft and LaccessRight are considered as optimization variables as well as LshortLO, LaccessLO, and the probe dimensions. Our optimization goal was to maintain a proper tradeoff between the transmission of LO and IF signal, while maintaining LO, IF and RF rejection below < -10 dB.

In transmission mode, $|S_{31}|$ and $|S_{23}|$ are evaluated to ensure the proper transmission of LO and IF signals. Concerning LO, $|S_{31}|$ and $|S_{11}|$ are illustrated in Fig. 110. (a). We obtained at f_{LO1} ~ 127 GHz a $|S_{31}|$ value of -0.74 dB and a $|S_{11}|$ value of -14.8 dB. Moreover, we can notice that $|S_{31}|$ > -2 dB in the ~110–148 GHz frequency range. Concerning the IF band (0-30 GHz), the results are shown in Fig. 110. (b). Here, $|S_{23}|$ > -1.91 dB and $|S_{33}|$ < -6.54 dB. At first insight, we could think that the LO block could be used also for the SHM2 mixer. However, a deeper exploration must be made in terms of the rejection properties of the mentioned block.



(a) (b)

Fig. 110. (a) LO transmission and (b) IF transmission in LO/RF filters + LO transition preliminary block.

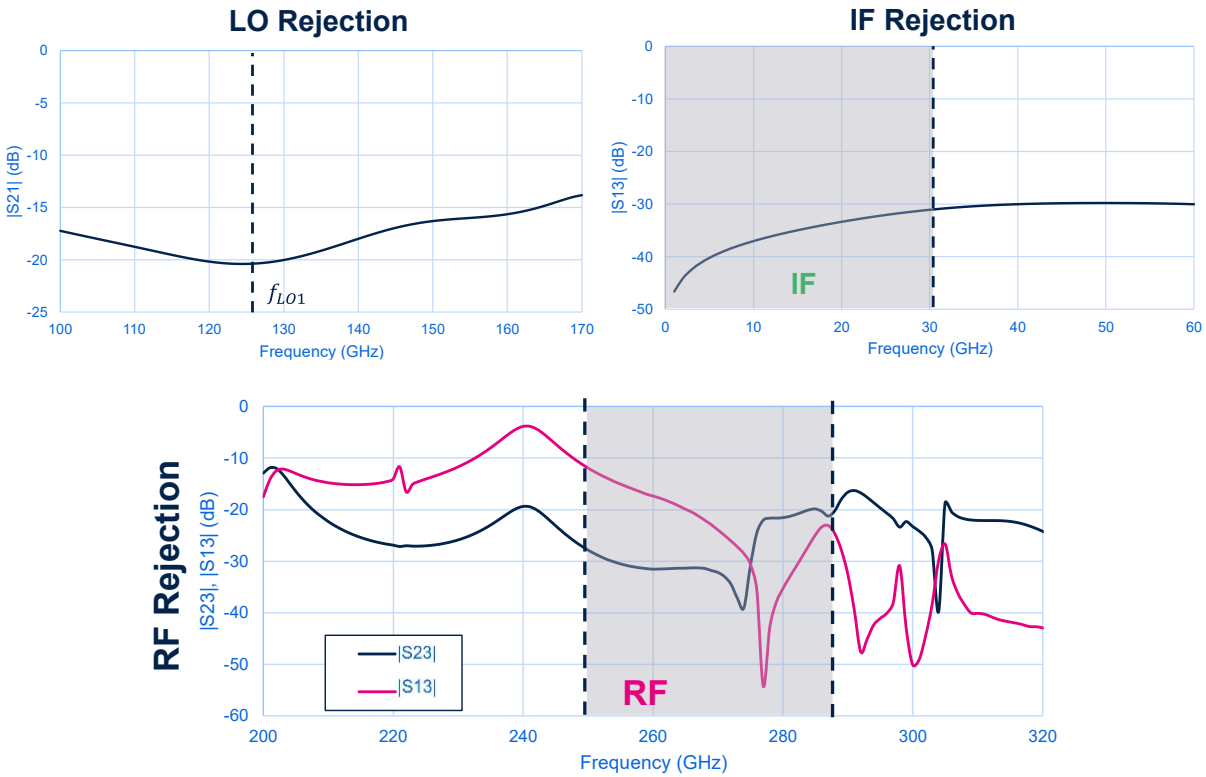


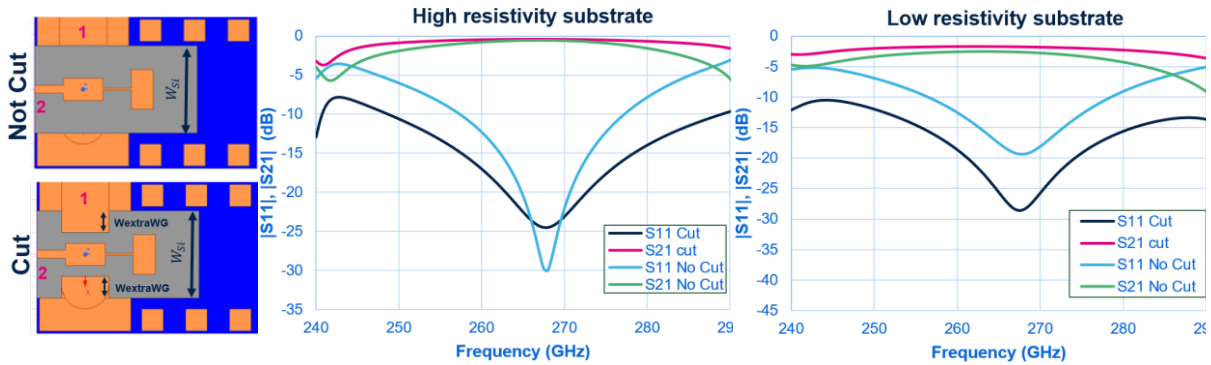
Fig. 111. (a) LO rejection, (b) IF rejection and (c) RF rejection in LO/RF filters + LO transition preliminary block.

In this perspective, we evaluated the capabilities of LO block to reject the RF band, IF and LO frequency. The signal paths that are wanted to be rejected are illustrated in Fig. 109 (b). Concerning LO signal rejection, we obtain $|S_{21}|$ = -20 dB. Moreover, $|S_{21}|$ is below -10 dB in the 100 – 170 GHz band. This shows that the LO filter is properly adapted to the LO overall block. Concerning RF band, $|S_{23}|$ < -20 dB and $|S_{13}|$ < -10 dB, validating the RF filter. Finally, the rejection of IF band is explored, giving a $|S_{13}|$ < -30 dB, which is expected due to the high-pass intrinsic behavior of the LO waveguide. In conclusion, we obtained the optimized values for the LO block that are presented in Table 17.

LaccessLeft	LaccessRight	LprobeLO	WprobeLO	LshortLO	LaccessLO
390 µm	370 µm	268 µm	180 µm	900 µm	600 µm

Table 17. LO block final optimization values using the preliminary 3D model.

Following the design method illustrated in Fig. 95 and Fig. 96 we integrated our preliminary design model into a preliminary package model. As mentioned, in this package we considered the actual integration of the DC ground, the increment of Silicon die width for die attaching and the Silicon resistivity for the desired DOE in BiCMOS 55 nm technology. As DC ground, a 180 µm x 100 µm patch has been realized and interconnected to the previously designed line in the RF block. Also, the Silicon die width has been increased from 200 µm to 300 µm. These aspects, as well as the modification of channel dimensions for die attach has required a new optimization of the design parameters.

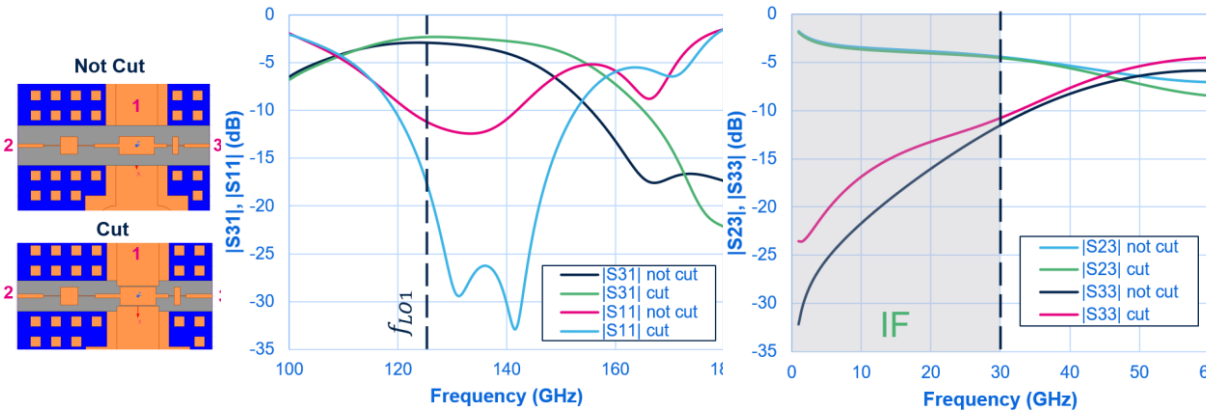


(a) (b) (c)

Fig. 112. RF transition integrated in preliminary integration strategy in (a) cut and not cut configuration and simulations using (b) high-resistivity 100 µm substrate and (c) low-resistivity 100 µm substrate.

Another aspect is the transition from high-resistivity to low-resistivity substrate, which is expected to increase the insertion losses of both RF and LO blocks. Moreover, we decided to explore the elimination of the extra substrate in the RF and LO E-plane probes, as concluded in section 3.6.3.3. as an interesting approach to improve the matching between the probe and the reduced-height waveguide for high thickness substrates.

We will start by exploring the RF block transition. This block has been re-optimized for improved insertion loss in the RF band considering the associated packaging modifications. It must be noticed that in this case, the SSL length between port 2 and the RF probe is not transparent. In consequence, this parameter has also been optimized. The impact of the substrate resistivity in the optimized RF block is illustrated in Fig. 112. (b) and (c). Using an HR substrate, we achieve $|S_{21}| > -2.2$ dB (No cut) whereas for low-resistivity substrate, $|S_{21}| > -5$ dB (No cut), leading to an increment of 2.8 dB in insertion loss. However, by eliminating the extra substrate around the E-plane RF probe in low-resistivity substrate, we reduce the insertion loss from 5 dB to 2.6 dB in the overall RF band. The same expected behavior can be found for the high-resistivity substrate.



(a) (b) (c)

Fig. 113. LO/RF filters + LO transition blocks integrated in preliminary integration strategy in (a) cut and not cut configuration and simulations of (b) LO transmission and (c) IF transmission in low-resistivity substrate.

Moreover, we also explore the impact of removing the extra substrate in the LO block, as shown in Fig. 113.(b) We can notice in terms of LO signal transmission that $|S_{31}|$ = 2.97 dB with the extra substrate and $|S_{31}|$ = 2.30 dB without it, leading to a 0.67 dB reduction of the insertion loss. However, no impact has been observed using this approach in terms of IF band, which is expected since this improvement is made at LO transition, which is transparent for the IF signal. We notice that IF insertion loss is around 4.5 dB, which is quite high due to the long signal path between port 3 to port 2 and the low-resistivity substrate.

Finally, this second optimization of RF and LO blocks led to a final dimensioning of the SSL and the RF and LO E-plane probes in the Silicon chip. However, the chip has always been considered in optimization as two separated blocks. In consequence, both pieces have been joined, leading an initial space of ~10 µm for the antiparallel Schottky diode structure. The final dimensions of the first demonstrator of SHM1 in 100 µm BiCMOS 55 nm low-resistivity substrate are illustrated in Fig. 114.

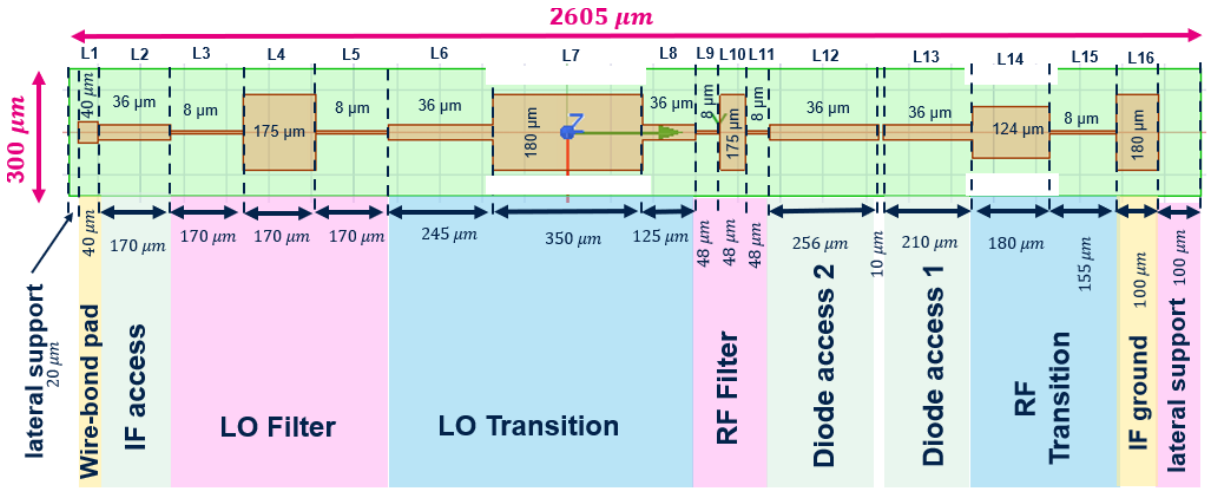
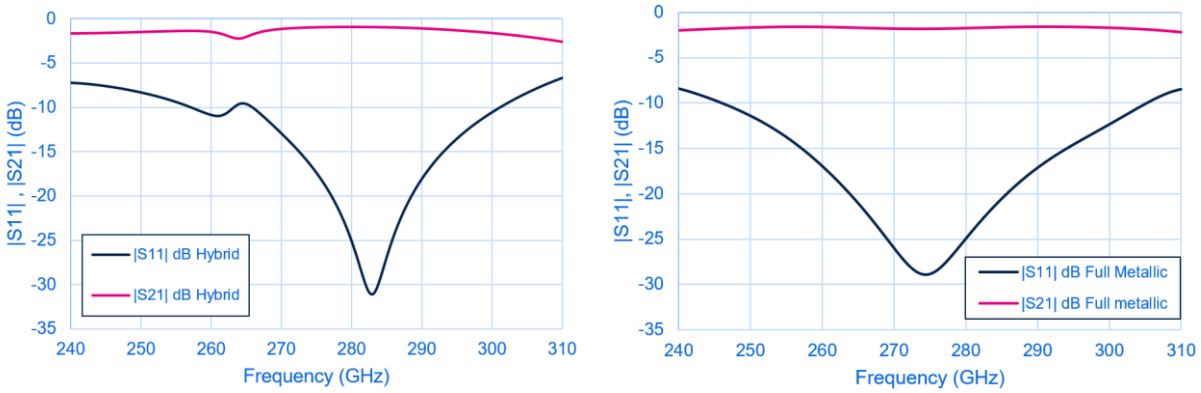


Fig. 114 Final dimensions of first SHM demonstrator in 100 µm Silicon substrate.

Two lateral supports (left and right) have been added with a length greater than 20 µm to leave a proper spacing between metallization and the Silicon sawing path for laser ablation. The left lateral support has been fixed to the minimal value to reduce the length of the IF wirebond. The right lateral support has been fixed to a larger value of 100 µm to lead proper spacing for die attach. The wirebond pad (L1) dimensions are consistent with those of the associated wirebond pad class for the BiCMOS 55 nm technology. The IF access line has been led to the same optimized length of the step lines of the LO filter (170 µm). The diode access 2 correspond to $\lambda_{channel}/2$ @ 268 GHz. Finally, the IF/DC ground pad dimensions had been approximated to the equivalent dimensions of 4 wirebond pad class in the associated technology. The other elements such as the LO filter, LO transition, RF filter, Diode access 1 and the RF transition have been previously optimized. In conclusion, using the conversion loss equation in chapter 2, we obtain a total loss of ~6 dB in low-resistivity substrate. The integration of the circuit in the BiCMOS 55 nm DOE will be explained in section 4.5.

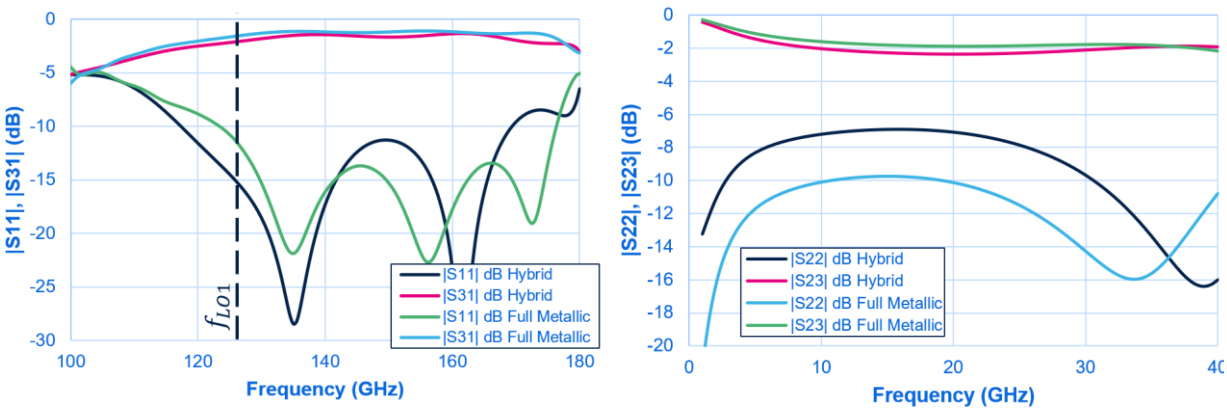
Finally, we evaluate the integration of the SHM in the final hybrid integration strategy proposed in section 4.3.3 as well as in the full metallic package from section 4.3.4. As mentioned, the main difference of these integration strategies compared to the preliminary package (in terms of Silicon die) is the reduction of substrate thickness from 100 µm to 50 µm and the consideration of the Silicon oxide dielectric. The final performances using simplified blocks, (as illustrated in Fig. 95) are shown in Fig. 115.



(a) (b)

Fig. 115. RF block final simulations considering the proposed (a) hybrid and (b) full metallic package.

From Fig. 115 (a) we can notice that, although the central frequency (illustrated as the lower value of $|S_{11}|$ in the figure) is not centered at 268 GHz, we succeeded to maintain the insertion loss below 2.25 dB in the overall RF band. Also, $|S_{11}|$ is below -8.9 dB in the mentioned band. Moreover, we can notice a small peak in $|S_{11}|$ at 265 GHz (reflected also at $|S_{21}|$ at the same frequency). This is caused by the channel that encloses the DC ground formed by the wirebonds due to capacitive coupling. In consequence, the mentioned top channel has been dimensioned to mitigate this impact as much as possible since this peak determines the higher value of insertion loss in the RF band. Regarding the RF block in the full metallic package, a straightforward equivalence in terms of package optimization variables (same LshortRF and LaccessRF for both packages) is not possible, since the channel wall is continuous (and not formed by periodic vias arrangement) and the die attach glue is closer to the probe. This causes a frequency shift in frequency. In consequence, a new optimization has been executed, leading to the performances illustrated in Fig. 115 (b). For this RF block, $|S_{21}| > -1.81$ dB and $|S_{11}| < -12.7$ dB.



(a) (b)

Fig. 116. LO block final transmission simulations considering the proposed (a) hybrid and (b) full metallic package.

Finally, the performances of the LO and IF signals in the LO block in both proposed packaging solutions are illustrated in Fig. 116. At LO transmission, we obtained in the hybrid package $|S_{31}|$ = -2.08 dB and in the full metallic integration $|S_{31}|$ = -1.56 dB. $|S_{11}|$ is below -11.8 dB in both cases. Concerning IF transmission, $|S_{23}|$ > 2.35 dB for the hybrid package and $|S_{23}|$ > 1.88 dB for the full metallic package. For the LO block, the optimization values Laccess and LshortLO remain the same in both packages since LO and IF performances are comparable. The final optimization values in both packages are shown in Table 18 and Table 19.

LshortRF	LaccessRF	LshortLO	LaccessLO
350 µm	450 µm	900 µm	600 µm

Table 18. RF and LO block final optimization values in the final hybrid integration strategy (package optimization variables)

LshortRF	LaccessRF	LshortLO	LaccessLO
400 µm	350 µm	900 µm	600 µm

Table 19. RF and LO block final optimization values in the full metallic integration strategy (package optimization variables)

The recompilation of the mentioned performances to obtain the estimated conversion losses are illustrated in Table 20. To calculate the insertion loss associated with the IF signal path, the losses of the IF line have been included. The IF line losses have been calculated using the Linecalc tool in ADS assuming a straightforward microstrip line and using the described PCB and organic substrate specifications in section 4.3.2 and 4.3.3. We can conclude that the total passive losses of both package solutions are comparable, showing a difference of just 0.86 dB. As expected, the major contributors of the total conversion loss are the diodes, with an estimated conversion loss value of ~11.7 dB based on the Schottky diode conversion loss extracted from the proposed diode model in chapter 2.

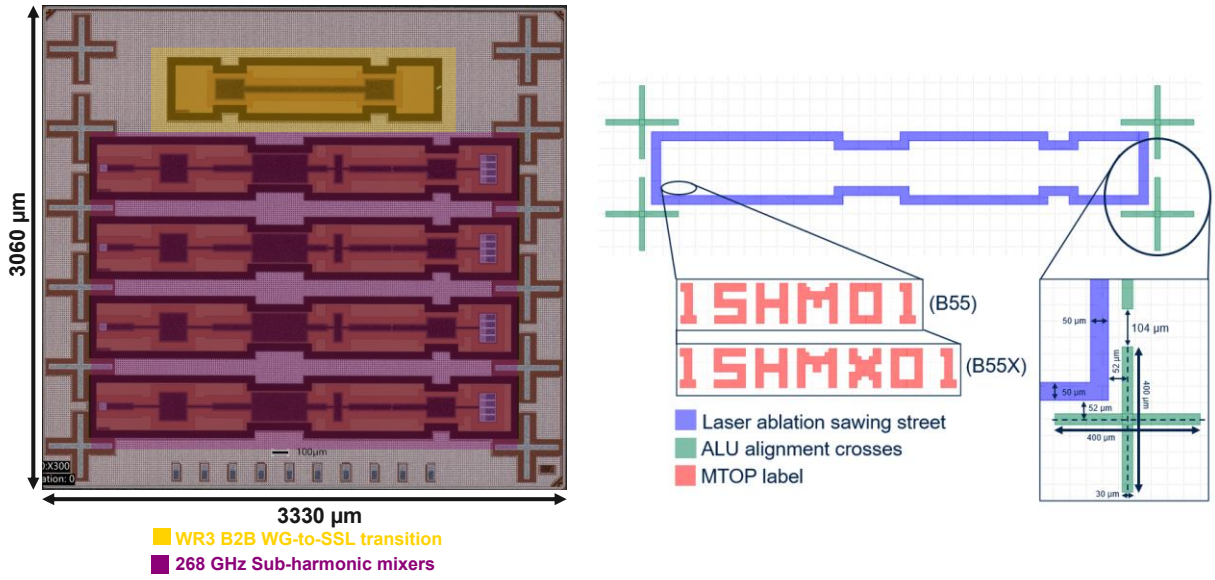
Integration strategy	ILRF (dB)	CLdiodes* (dB)	ILIF (dB)		Passive losses (dB)	CL (dB)
			LO block	IF line		
Hybrid package	2.25	11.7	2.35	0.47	5.07	16.77
Full Metallic package	1.81	11.7	1.88	0.52	4.21	15.91

Table 20. Comparison of passive and total conversion loss of the SHM1 in the hybrid and full metallic integration strategy. *Conversion loss assuming previous W-band Schottky diode

4.5 Silicon DOE description

As mentioned in section 4.4.1, we will take advantage of the hybrid integration strategy (which allows mass production of multiple circuit samples) to propose multiple SHM versions preserving the optimized passive circuit dimensions from Fig. 114 and varying the anode surface of the Schottky diode to modulate the presented impedances by the anti-

parallel diode structure to find an optimal surface for improved conversion loss. The technology used is the 9-metal layers BiCMOS 55 nm with the B55 and B55X variants, which will allow the use of the two Schottky diodes architectures that have been presented in chapter 2. As a reminder, the BEOL in B55 and B55X is the same but the FEOL is different. However, similar performances are expected. The final top cell integrated in both MPW variants is illustrated in Fig. 117 (a).



(a) (b)

Fig. 117. (a) Top cell of BiCMOS 55 nm DOE. (b) Circuit layout description for B55 and B55X technologies. Values in physical (shrinked) dimensions.

In total, 5 circuits have been integrated in a 10.19 µm surface area (shrinked). 4 circuits are the different SHMs and 1 corresponds to the WR3 B2B reference circuit to assess the impact of substrate resistivity on achievable performances in comparison with the BiCMOS 130 nm high-resistivity DOE from chapter 3. In Fig. 117 (b), the description of the alignment crosses and sawing street for laser ablation is presented, which follows a same dicing strategy as the BiCMOS 130 nm DOE. For the Schottky diode variations, 4 anode surfaces with steps of 1.5 µm² have been considered (to modulate the diode impedance), being the 7 µm² anode surface (unshrinked) the starting point since it has been extracted as the reference anode area for previous SHM design in W band from [41]. The associated anode length variations to achieve the desired surfaces are illustrated in Table 21, as well as the anode width and number of fingers. The 5SHM01 device corresponds to the WR3 B2B transition.

Device name	**Schottky diode**			
	Anode width (µm)	**Anode length L (µm)**	**Number of fingers**	**Anode area (µm²)**
1SHM01	0.31	4.44	4	5.5
2SHM01	0.31	5.65	4	7
3SHM01	0.31	6.85	4	8.5
4SHM01	0.31	8.06	4	10
5SHM01	N/A	N/A	N/A	N/A

Table 21. Final devices integrated in the BiCMOS 55 nm MPW (B55). Unshrinked dimensions. For B55X variant just replace “SHM” by “SHMX”.

For the layout, the associated shrinking factor of the BiCMOS 55 nm technology has been considered to ensure that the designed dimensions correspond to those physically manufactured. Moreover, to integrate the antiparallel Schottky diode architecture into the passive circuit, two tapered lines have been included. For the SSLs with a width larger than allowed by the MTOP design rules, hollow metallic layers with minimal empty square dimensions have been designed to replace the desired continuous metallic layers. The tiling distribution chosen for these circuits is like the “proposition 1” described in chapter 3.6.3.4, but with the changes associated with the design rules of the BiCMOS 55 nm BEOL.

4.6 Conclusions & perspectives

In this chapter, the state-of-the-art of SHMs above 200 GHz has been first presented. The non-linear element used for the design of those circuits is based on III-V technology thanks to GaAs Schottky diode performances at THz frequencies. Based on the reported SHMs, achievable SSB conversion loss is around ~8-14 dB and LO power between ~4-8 dBm can be expected for solutions operating between 170-400 GHz. In addition, to our knowledge, SHMs using Silicon Schottky diodes above 200 GHz has not been reported yet.

Motivated by the mixer-first receiver architectures explored in chapter 1, we proposed a receiver architecture that supports the IEEE 802.15.3d standard, enabling transmission at high data rates in a power efficient manner. The circuit consists of two SHMs (SHM1 and SHM2) with ~30 GHz band which are interconnected previously to a diplexer that splits the 68 GHz RF band. Then, both SHMs are pumped by two different LO frequencies to shift the RF splitted frequency bands to 0 - 30 GHz. In this thesis, we proposed to do a first demonstrator focusing on the SHM1 block, using BiCMOS 55 nm Schottky diodes.

Concerning packaging, these circuits are traditionally packaged following the CNC-machined metallic split-block integration strategy illustrated in Chapter 3, but with the addition of a DC ground and an IF connector. However, the limitation of this type of package is firstly its high cost and secondly the lack of automated process. To solve the issue related to the automation of package process, we propose to integrate the mentioned SHM following the previously explored hybrid integration strategy, by using at the same time metallic split-block modules and organic laminate substrate. A full metallic split-block package is proposed as reference for benchmarking purposes.

The circuit has been designed following an SDM optimization strategy, where the RF and LO blocks are made separately and then adapted to the antiparallel Schottky diodes. In our case, to adapt the Schottky diodes impedances to both blocks, we took advantage of mass production capability of the hybrid integration strategy to propose multiple SHM versions varying the diodes anode surface in steps of 1.5 μm^2. This approach enables to mitigate the risk associated to EM modelization of Silicon-based Schottky diodes since an adaptation of

the strategy used in GaAs is not straightforward due to the interdigitated structure of Silicon Schottky diodes.

In conclusion, simulated passive total losses using hybrid and full metallic package are 5.07 dB and 4.21 dB respectively (Table 20). Comparing the RF and LO blocks with the reported losses, we can see that the insertion losses of both blocks (in RF and LO transmission mode) are coherent with the state-of-the-art in both integration strategies. As first perspective, one can think to replace the low-resistivity Silicon substrate to a higher-resistivity one to improve passive circuit performances. At the time of the writing (Q4-2023), the prototyping of the full metallic split-block integration is ongoing. This will lead to a first evaluation of the SHM. In addition, the associated results will be presented at the PhD defense.

Chapter 5
Conclusions & Perspectives

5.1 General Conclusions

In this thesis, the potential of Silicon technologies and innovative packaging solutions have been investigated to achieve wireless solutions delivering high data rates in a power efficient manner. The development of such solution is driven by the never-ending demand of more and more connectivity to support emerging applications targeted by 6G technology. In this logic, different wireless links operating at frequencies above 200 GHz have been studied to leverage wider available frequency bands which will enable the use of low-complexity modulations while targeting high data rates. Therefore, the pursued research works has been oriented on the Rx part by exploring low-sensitivity and broadband Rx solutions above 200 GHz, which is dominated so far by mixer-first GaAs Schottky diode SHMs. In fact, thanks to innovative Silicon-based Schottky diodes with cutoff frequency of ~1 THz and cost-effective organic substrate package evaluated above 200 GHz, we targeted to enable high-performant and cost-effective SHM design in the 253-321 GHz band using Silicon-based technologies.

In this logic, our starting point was the previous work performed by Dr. Vincent Gidel concerning the development of innovative Schottky diodes in 55 nm BiCMOS technology since antiparallel Schottky diodes are the main element driving the performances of SHM design. In consequence, in chapter 2, we review this previous B55 Schottky diodes development. We proposed then an updated analytical model to calculate the zero-bias junction capacitance C_{j0} and the back-end capacitance C_{BE}, achieving measurement and modeling difference below 0.53 fF (C_{j0}) and 1.2 fF (C_{BE}). Moreover, by using the updated model and leveraging a previous W-band SHM design we demonstrate a good agreement between simulated and measured conversion loss. Finally, improving the previous design conversion losses of 11.7 dB (all ports to $50\ \Omega$) and 7.3 dB (all ports impedance optimized) are simulated. From this chapter, two perspectives can then be identified. Firstly, further validation of the proposed analytical model by leveraging measurement of B55X Schottky diodes achieved during Dr. Vincent Gidel thesis. Secondly, the optimization of the design of SHM in STMicroelectronics B55 technology and even going further in B55X technology by leveraging proposed models in those technologies.

Moreover, our second starting point was the previous work concerning cost-effective packaging solutions. In this logic, in chapter 3, previous hybrid integration strategies developed in the thesis of Dr. Victor Fiorese are reviewed and leveraged. We proposed to reduce the complexity of this packaging solution by eliminating the copper-pilar bumps and integrate the E-plane transition on the Silicon IC, thus reducing costs since an extra fabrication step is eliminated and required laminate substrate complexity is reduced. To validate the proposed integration strategy, a WR3 B2B WG-to-SSL transition is proposed and evaluated in BiCMOS 55 nm and BiCMOS 130 nm technologies. The presented hybrid innovative solution achieved simulated insertion loss around ~3 dB using HR substrate, being competitive to solutions presented in the literature. The perspectives associated to this work will be discussed in the next section.

Finally, the work developed in chapter 2 and 3 is leveraged to propose a 268 GHz Silicon SHM solution in B55 and B55X technologies which follows the previously presented hybrid integration strategy. Considering the simulated Schottky diode from chapter 2, we expect 16.8 dB of conversion loss, being 5.07 dB related to the low-resistivity substrate of the BiCMOS 55 nm technology. In this order, high-resistivity SHM can be targeted for future improvements to reduce the losses associated to the passive circuit. For benchmarking purposes, a Silicon SHM integrated in full metallic split-block package is also proposed, leading to comparable passive losses (4.21 dB) from the hybrid integration strategy. To have a vision of the proposed solutions compared to GaAs SHM we illustrate in Table 22 the main points that each solution improves in terms of costs and electrical performances.

Solution	**GaAs Schottky diode SHM in metallic split-block module**	**Silicon Schottky diode SHM in metallic split-block package**	**Silicon Schottky diode SHM in Hybrid package**	**Silicon Schottky diode in alternative package solution**
Status	NA	Package fabrication ongoing. Measurements to be presented in PhD defense	Package fabrication to be done. Measurements in perspectives.	Future Perspectives (section 5.2.1)
Conversion loss CL	CL=10.6 dB*	CL = 15.9 dB**	CL = 16.8 dB**	TBD
Assembling process	☹	☹	☺	☺
Package overall price	☹	☹	☹	☺
IC technology price	☹	☺	☺	☺

Table 22. Comparison of the different SHM solutions studied and developed in this thesis. *Average calculated from CL values in Table 13. **Simulated values.

We can notice firstly that the proposed benchmark solution, despite it relies fully on metallic split-block integration (which is pricy), is interesting from the point of view of associated IC technology price. However, there is a lack of automated assembling process of Silicon die in the package. That is why the hybrid solution is presented to solve this inconvenience. Finally, a packaging alternative could be further explored in the context of future work to reduce the cost of the overall packaging. However, from the proposed solutions, in terms of achieved performances, no conclusion can be obtained at the moment of delivery of this thesis since the full metallic split-block and hybrid package solutions have not been measured yet. Therefore, the prototyping of the full metallic split-block solution is ongoing, and the results will be presented in the defense of this PhD. The same is happening for the WR3 B2B circuit integrated in full metallic split-block module. The current status of the prototyping is illustrated in Fig. 118.

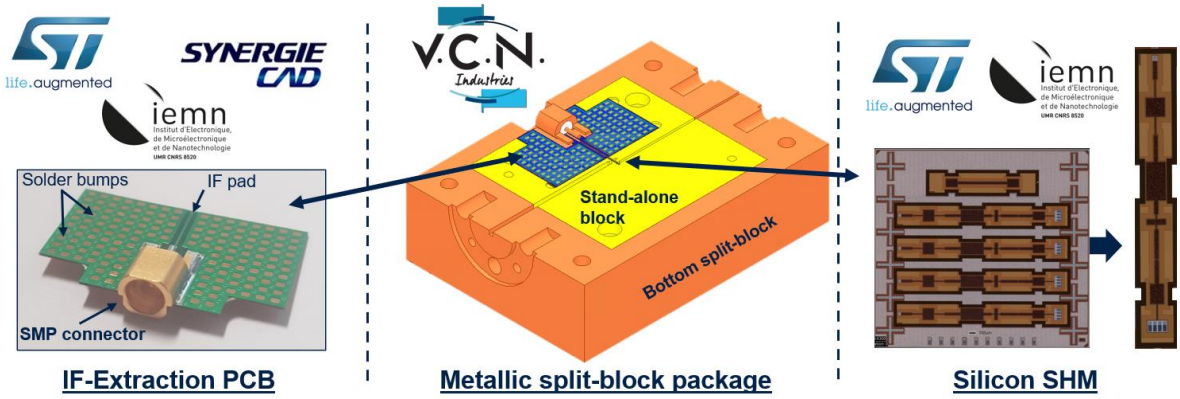


Fig. 118. Different entities that played/are playing in the fabrication of each component from full metallic split-block SHM module.

The circuit elements such as the IF PCB and the Silicon dies have already been fabricated. From one side, the PCB prototyping has been made with the aid of STMicroelectronics and Synegie CAD. The solder bumps will be placed at the IEMN Laboratory. By other side, the Silicon dies have been fabricated and the singularization and thickness reduction will be started soon at IEMN laboratory. However, the prototyping of the metallic split-block module had required more time, and the fabrication is still ongoing at VNC Industries, specialized in CNC machining process. Finally, the assembly of overall elements will be pursued at the IEMN laboratory. After characterization of the module in terms of conversion loss, bandwidth, and noise figure, one can think to pursue a first demonstration of a wireless link, expecting to achieve 15 Gb/s of data rate using OOK modulation and 30 Gb/s with PAM-4.

5.2 General Perspectives

5.2.1 From package point of view

As a first general perspective we target the fabrication of the presented innovative hybrid integration strategy. Despite the promising automated packaging process, the fabrication of each package block has not been pursued due to the long lead time of organic substrate prototyping because packaging supply chain was fully loaded after COVID-19 pandemic. Fortunately, the situation is now coming back to normal, thus allowing the fabrication of the organic substrate and split-block modules. The different entities involved in the prototyping of each block are illustrated in Fig. 119. For the fabrication of metallic split-block we target VCN industries also as the full metallic split-block integration. Also, the organic substrate fabrication will be led by BEM&T and laser ablation at IEMN are targeted to create the microchannel below the Silicon circuit. Finally, the Silicon dies have already been fabricated.

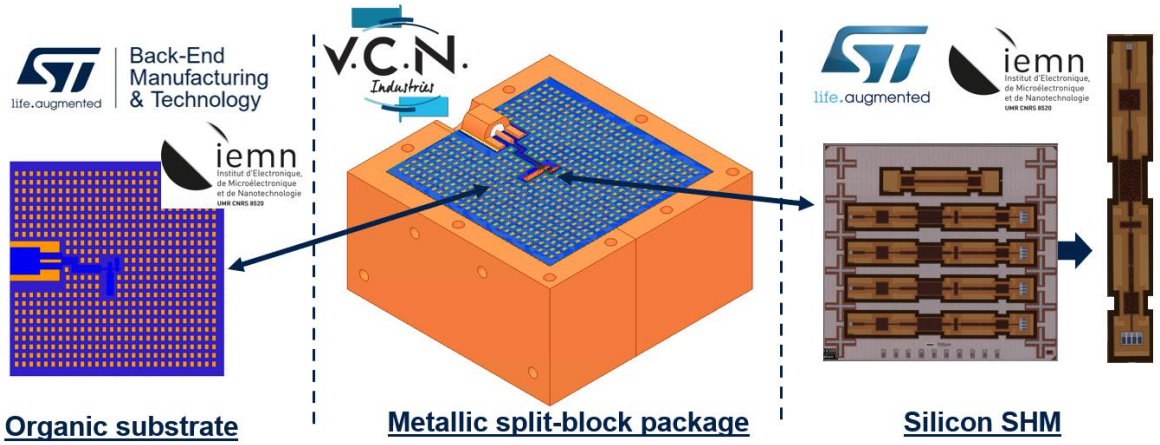


Fig. 119. Different entities that played/are playing in the fabrication of each component hybrid package SHM module.

However, as discussed before, both proposed solutions in full metallic integration and hybrid package rely on metallic split-block modules, which are expensive. In this logic, other alternatives can be explored to replace this element. From the discussed alternatives in chapter 3 we can opt for 3D metallic printing, which have showed promising perspectives for packaging above 200 GHz. However, this does not solve the problem in terms of the overall package price. Therefore, one can think of Plastronic technology, where electroplating process can be used where metallization deposition is required. However, this will apply just for consumer solutions and not for space applications, due to the limitations in terms of temperature management and reliability.

5.2.2 From overall system point of view

Concerning the overall Rx system, in this thesis just an individual SHM block has been studied. A future perspective could be the enablement of the complete system to support the complete 253-321 GHz band. The proposed block compared to the overall Rx is illustrated in Fig. 120. An individual B55/B55X IC could support all the analogic functionalities such as both SHMs, LO generation and TIA amplifiers. Concerning the diplexer, it could be fabricated directly into the split-block module. Moreover, the recent evolution of ST Silicon photonics technologies could enable the fabrication of innovative and effective Tx solutions (cleverly combining high speed modulator and frequency comb). This complete system could enable data rates of 30 Gb/s by using OOK modulations and 60 Gb/s using PAM-4.

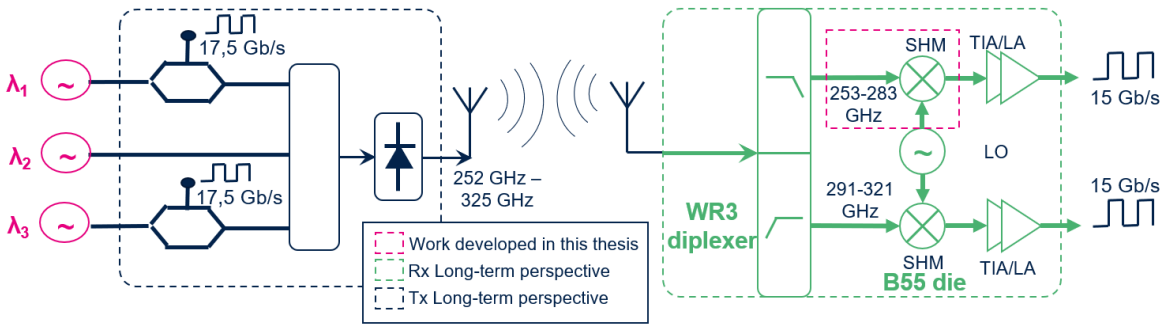


Fig. 120. Overall wireless link system to support the complete 253-321 GHz band.

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Publications

- **D. A. Ovalle-Taylor**, F. Gianesello, C. Luxey and G. Ducournau, "Innovative Packaging Integration Strategy for BiCMOS ICs Operating beyond 200 GHz," *2023 53rd European Microwave Conference (EuMC)*, Berlin, Germany, 2023, pp. 6-9.

- G. Simoncini, **D. A. Ovalle Taylor**, G. Orecchini, J. C. Azevedo Goncalves, F. Alimenti, "Millimeter Wave Avalanche Noise Diodes in SiGe BiCMOS Technologies: State-of-the-Art and Applications to Future Space Missions," *2023 1st Space Microwave Week (SMW)*, Noordwyk, Netherlands, 2023

- At the moment of the thesis delivery, a journal article has been accepted for the *International Journal of Microwave and Wireless Technologies (IJMWT)* (EuMW special issue)