RF reliability in SOI-CMOS technologies : device model and application to power amplifiers

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fiabilité rf en technologie soi cmos : modélisation et application à un amplificateur de puissance

rf reliability in soi cmos technologies: device model and application to power amplifiers

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General Introduction

Mobile telecommunications have steadily evolved with the launch of a new generation each decade. It started from the first generation (1G) mobile communication, developed in the 1980s, which offered basic voice calls. Since then, significant technological advancements have been made in terms of data rates, network capacity and latency, as well as security protocols. Currently, we are entering the fifth generation (5G) era which features enhanced user data-rates (20Gb/s), ultra reliable and low latency (50ms) and increased connectivity of Internet-of-Things (IoT) [1]. In order to achieve these goals, the 5G network operates in two carrier frequency ranges of the radiofrequency (RF) spectrum: sub-6GHz frequency bands and millimeter-wave frequency bands ranging from 24 – 40 GHz.

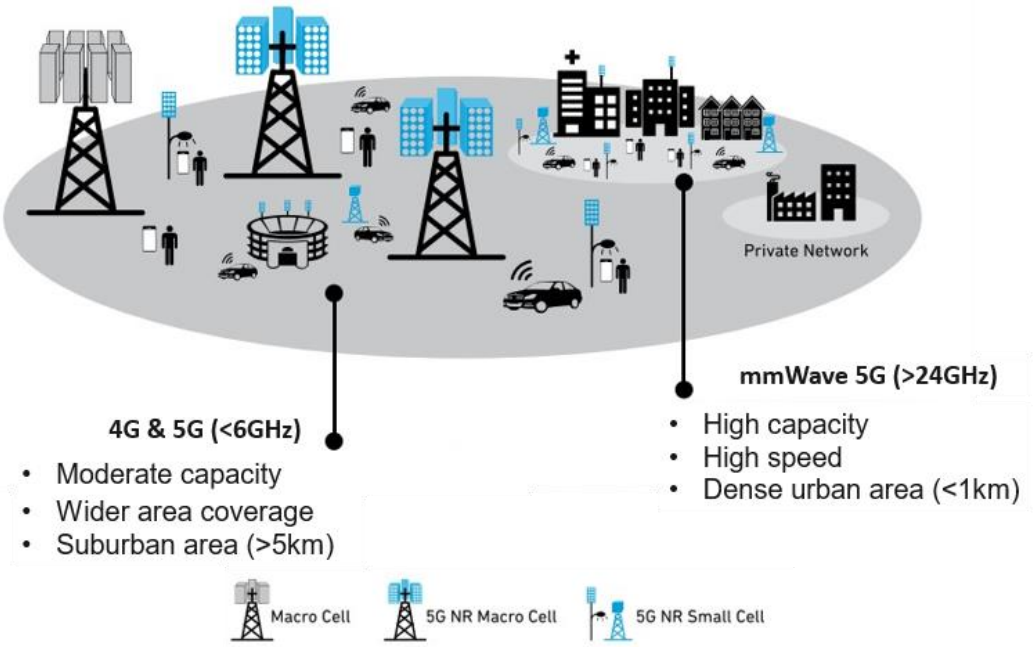

Figure 0-1 : 5G wireless communication is supported by mid (<6GHz) and high (>24GHz) frequency bands. Mid-range frequency bands offer a balance between performance and network coverage working in conjunction with 4G networks whereas high-range frequency bands target optimal performance at short distances enabled by small base station (small cells) for seamless connection. [2]

The usage of these frequency bands depends on the wireless communication range and data rates, as illustrated in Figure 0-1. For lower frequency bands, the RF signals can travel longer distances with lower data rates (low capacity) while high data rates (high capacity) are available at shorter distances due to lower bandwidth saturation at millimeter-wave frequencies. The communication range is determined by the performance specification of the transmitter and receptor in the RF/mmW front end transceiver. On the transmitter end, the transmission link is strongly driven by the amount output power that can be delivered from the power amplifier to the antenna. High output power ensures the strength of the signal transmission, which is attenuated proportionally to the square of the distance between two antennas.

Following the adoption of 5G, it is expected that the surge in global demand for low-cost and high-integration-level RF front-end modules (FEM) in user-end equipment will shift the current landscape of RF mobile devices towards CMOS-based technology. This trend has been encouraged by the downscaling of the dimensions in CMOS transistors which significantly improved the RF figure-of-merits, i.e., gain, linearity, and cut-off-frequency F_T/F_{MAX}, especially for silicon-on-insulators (SOI) CMOS technology. One of the main challenges to overcome in RF CMOS FEM implementation is the integration of RF PAs. Aside from high linearity and efficiency requirements related to channel bandwidth constraints, PA designers need to tackle reliability challenges brought on by large output voltage swings. In CMOS devices, RF PA operating conditions induce aging mechanisms such as hot-carrier injection (HCI) and time-dependent dielectric breakdown (TDDB) which lead to RF performance degradation and ultimately device failure. To ensure reliable operation of RF PAs, design margins are generally based on DC worst-case conditions, thus the optimal design point is sacrificed. Although CMOS downscaling worsens the HCI and TDDB phenomenon in deep submicron nodes, earlier research on RF PA reliability characterization has demonstrated that the impact of RF stress on degradation or failure is comparatively lower than DC stress. Over-design can be avoided by relying on accurate reliability simulation models in the design flow to estimate the performance-reliability trade-offs for a given operating point.

The motivation of this research is to investigate CMOS PA aging mechanisms for RF/mmW reliability prediction at device level which can be divided into three main parts. The first part concerns accurate modeling of RF HCI degradation behavior in reliability simulations by implementing RF stress characterization using specific test structures and measurement setup. In the second part, we attempt to examine off-state (non-conducting) RF reliability modeling which has not been extensively explored due to the lack of understanding on the frequency-dependent behavior of off-state hot carrier and TDDB mechanisms. The third part is focused on the design of an aging compensation strategy for worst-case RF HCI stress to explore opportunities in extending RF PA lifetime and reduce the trade-off between performance and reliability.

References

[1] 3GPP, "5G System Overview," 2022. [Online]. Available: https://3gpp.org/technologies/5g-system overview.

[2] D. Schnaufer, T. Nguyen, B. Thomas, A. Mariani, P. Cooper, B. Peterson and P. Warder, 5G RF For Dummies®, 2nd Qorvo Special Edition, John Wiley & Sons, Inc., 2020.

1. RF power amplifiers for wireless communication at mmW frequency

The first part of this chapter presents the fundamental concepts to understand the performance characteristics of RF power amplifiers (PA). In the context of the millimeter-wave (mmW) PA specifications for the fifth generation (5G) applications, the design strategies related to the challenges faced by PA designers to achieve high performance (linearity and efficiency) within the reliability limits of the device are discussed. The technology benchmark of silicon and III-V devices reveals that CMOS devices are capable of meeting the FT/Fmax requirements and present advantages in terms of cost and integration over the III-V devices. In the second part, the reliability mechanisms which are responsible for CMOS PA device aging are introduced briefly, with particular attention on the recent progress in reliability modeling. The limitations of current degradation modeling in aging simulation flow of RF/mmW PAs are then discussed. Finally, the outline of this thesis is given to set the scope of this work.

1.1 Fundamentals of RF/mmW power amplifiers

1.1.1 RF PA characteristics

Power amplifiers (PA) are transconductance devices that drive an output current proportional to its input voltage. In RF transceivers, RF PAs are designed to amplify the power of the transmitted signal to an antenna. The main characteristics, as shown in Figure 1-1, that determine the performance of RF PAs are described in the following:

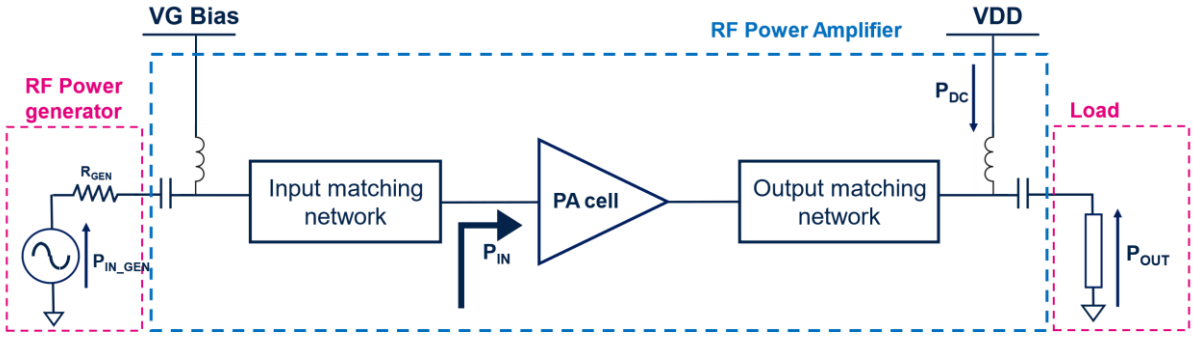

Figure 1-1 : General representation of an RF power amplifier

- **Gain**: The transducer gain (G_T) is represented by the ratio between the power delivered to the output load impedance (Z_L) and the available power delivered by the source generator. This is the "useful" gain since the power mismatch between the source generator and PA input is considered. Throughout this thesis, G_T is referred to as gain, linear gain or small-signal gain.

$$G_T[dB] = 10.\log\left(\frac{P_{OUT}\,[W]}{P_{IN\_GEN}\,[W]}\right) = P_{OUT}\,[dBm] - P_{IN\_GEN}\,[dBm] \qquad \text{(Eq.1-1)}$$

- **Power 1dB output compression point (P_{1dB})**: As the PA input power is increased, the output power increases linearly up to a point where it starts to saturate. The P1dB, as shown in Figure 1-2, corresponds to the output power level where the gain is reduced by 1dB. Beyond this point, the PA operates non-linearly and this region is referred to as gain compression.

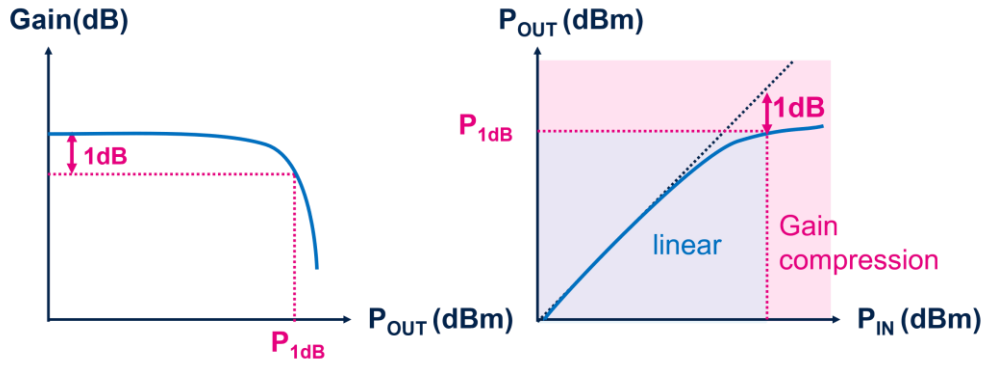

Figure 1-2 : (left) P_{1dB} is defined at the output power P_{OUT} where the gain drops by 1dB. (right) The linear and saturation (gain compression) amplification regions are separated by P_{1dB}

- **Power Added Efficiency** (PAE): The PAE is related to the power consumption (P_{DC}) of the PA device which draws its current from a DC supply voltage to provide gain amplification. This parameter is closely related to the different PA operating classes and the efficiency of the output matching network.

$$PAE[\%] = 100\% . \frac{(P_{OUT} - P_{IN})\ [W]}{P_{DC}[W]} \qquad \text{(Eq.1-2)}$$

- **Saturated output power** (P_{SAT}): This is the maximum output power achievable by the PA due to gain compression, and it is used as a design parameter to determine the bias operating point of the PA. For sinusoidal waveform, P_{SAT} is defined as the maximum power delivered to the load impedance (Z_L) at the fundamental frequency, where V_{DD} is the supply voltage while V_{DSAT} is equivalent to the overdrive voltage.

$$P_{SAT}[W] = \frac{(V_{DD} - V_{DSAT})^2}{2 \cdot Z_L} \qquad \text{(Eq.1-3)}$$

1.1.2 Review of PA classes

PAs are classified into linear (class A, B, AB, C) and non-linear (class D, E, F) PAs as distinguished by their conduction properties presented in the following:

- **Linear PAs** operate as current sources, where the conduction angle (θ_C) of the drain current waveform is dependent on the DC bias voltage level of the gate terminal as shown in Figure 1-3. Class A PAs are biased at $V_G \approx V_{DD}/2$ such that the drain current waveform remains a pure sinusoidal for the entire period of the input RF voltage swing. Class B PAs are biased at the threshold voltage, where the PA is switched off during half the period. For class C, the PA is switched off for more than half the period since the gate voltage bias is lower than the threshold voltage. Table 1-1 summarizes the θ_C for the different

linear PAs. It can be observed that the drain efficiency, which represents the ratio of the RF power at fundamental frequency to the DC power, decreases as θ_C increases. This is due to the higher power dissipation in the PA as a consequence of the increase in drain voltage and current waveforms overlap time. The linearity of the PA is proportional to the conduction cycle, thus achieving linearity and efficiency simultaneously is a challenge for the same RF output drive level. In general, RF CMOS PAs are designed in class AB as they offer a good compromise between linearity and efficiency by providing better linearity than class B and higher efficiency than class A. It should be noted that the efficiency values are theoretical, actual values are much reduced because of non-idealities and losses in the active (device) and passive components (matching networks) [1].

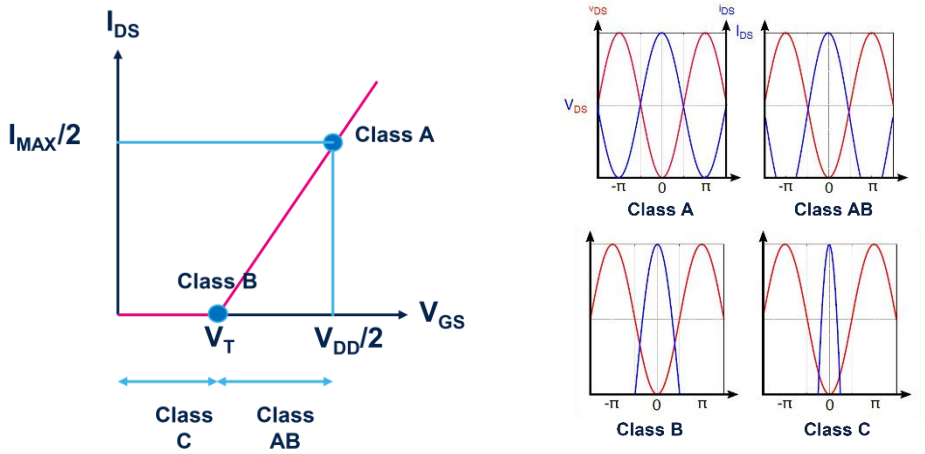

Figure 1-3: (left) The gate bias voltages determine the operation class of PAs. (right) The conduction angles of current waveform corresponding to each linear PA class [2]

Table 1-1 : Performance of linear PAs of class A, AB, B and C relative to their conduction angles.

Class	A	AB	B	C
Conduction angle	2π	π-2π	π	<π
Max drain efficiency	50%	50%-78.5%	78.5%	78.5-100%
Linearity	High	Medium	Low	Very Low

- **Non-linear PAs** are designed with the objective of enhancing efficiency. To reduce power dissipation, two conditions must be fulfilled: switching mode operation and minimal overlap between large drain voltage and current waveforms. As a consequence, the PA device no longer functions as a current source, but rather as a switching amplifier. Careful design of the output matching network is necessary to ensure that the voltage and current waveforms are out of phase. The drain voltage and current waveforms of class E and F PAs are illustrated in Figure 1-4. Theoretically, the 100% of maximum drain efficiency is achievable for both class E and F PAs since the output matching network can be tuned in the time-domain and frequency-domain respectively to obtain zero overlap between drain voltage and current.

Hot carrier stress is a reliability concern in linear RF power amplifiers as conduction current is present during high gate-to-drain voltage. This leads to time-dependent device

parametric degradation of the device, which is associated to RF performance degradation. Most PAs are designed using NMOS transistors to take advantage of their higher mobility properties, while hot carrier degradation is more severe in NMOS compared to PMOS. Switched mode PAs suffer from minimal hot-carrier stress due to the limited drain current flowing during its conduction period. Oxide breakdown is a problem for high efficiency PAs as the peak amplitude of the drain voltage can range between 2 (class AB) to (class E) 3.5 times of the supply voltage during non-conducting mode, resulting in a configuration of gate voltage near threshold voltage when the drain voltage is high. Further details on PA reliability issues are provided in Section 1.3.1.1.

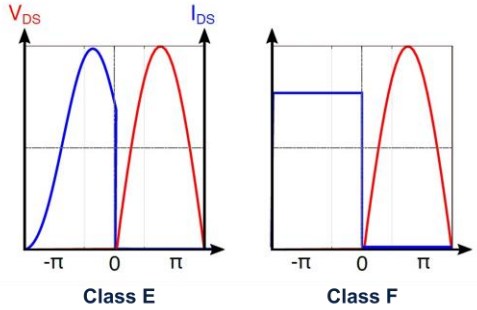

Figure 1-4 : Non-overlapping drain and current waveforms of non-linear PAs (Class E and class F) enable maximum efficiency. [2]

1.1.3 Design challenges of RF PA for mmW applications

Power amplifier design faces trade-off between efficiency and linearity due to the high data rate requirements for modern wireless communication standards. To increase the data rate transmission, higher order modulation such as quadrature amplitude modulation (QAM) is combined with multiple carrier transmission scheme, i.e. orthogonal frequency division multiplexing (OFDM), which results in high peak-to-average power ratio (PAPR) signals where the peak power is 10 – 12 dB greater than the average power [3]. This demands the PA to operate in the non-linear region (beyond P1dB) thus causing distortion to the transmitted RF signal and interference in the adjacent channels. The common approach to satisfy linearity requirements for high PAPR signal transmission is to operate at power back-off as illustrated in .

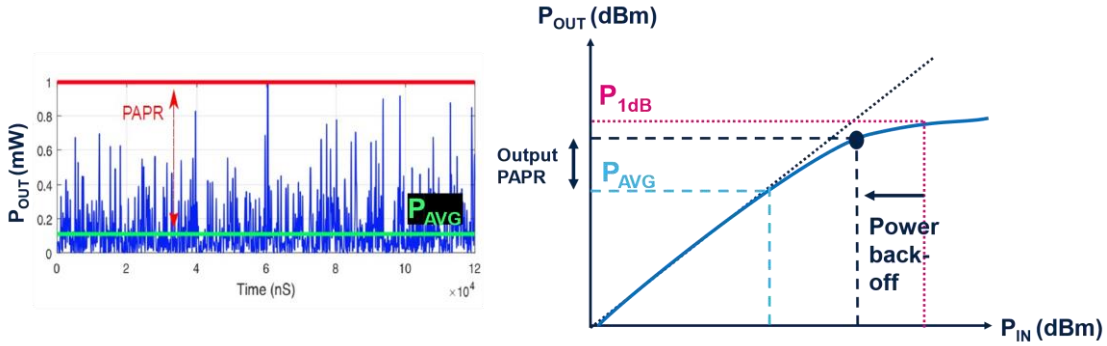

Figure 1-5 : (left) OFDM signals with high PAPR ≈8.5dB transmitted by an RF PA [2], (right) Power back-off scheme considering linearity-efficiency trade-off to limit high PAPR signal distortion.

However, this comes at the cost of reduction in efficiency, as the PAE in this operating region is typically much lower than the maximum PAE. At present, Doherty PA architectures offer efficiency enhancement in back-off power range and remains an active area of research to improve both efficiency and linearity metrics of PAs.

Besides high linearity and high efficiency, high output power is desired in mmW PAs. As an example, the estimated power requirement for 5G at 28GHz or 39GHz (taken from [4]) is shown in Table 1-2 to illustrate the power budget of mmW PAs in user-end handset equipment and base station. The Effective Isotropic Radiated Power (EIRP), which represents the strength of the transmitted signal in the direction of maximum antenna gain, is an important parameter to ensure the quality of service of wireless communication link. It is defined by the power transmitted by the PA (P_T), antenna gain (G_{ANT}) and the transmission loss between the transmitter and antenna (L_C), i.e., signal attenuation through RF switch, interconnects, and packaging. The beamforming antenna arrays (N_{ANT}) provide a higher directivity using multiple PAs thus boosting the effective radiated power of each array by N^2. The usage of a high number of antennas in base station enables large EIRP to provide wider coverage and more reliable link to a large number of users compared to handset devices. The power per PA (P_{T0}), expressed in eq.1-5, is expected to supply maximum P_{T0} between 20 dBm to 24dBm in the case of handset equipment as a consequence of implementing high PAPR modulations. This implies that each PA needs to handle approximately hundreds of milliwatts at maximum power which translates to V_{DD} of more than 3V (for Z_L=50Ω) to produce high output voltage swings.

$$EIRP[dBm] = P_T[dBm] + G_{ANT}[dB] - L_C[dB] \quad \text{(Eq.1-4)}$$

$$P_{T0}[dBm] = EIRP[dBm] - 20.\log_{10}(N_{ANT}) - G_{ANT}[dB] + L_C[dB] \quad \text{(Eq.1-5)}$$

Table 1-2 : 5G communication EIRP requirements for handset and base station at 28GHz/39GHz which determines the output power that each PA needs to supply to antenna arrays. Base stations are required to operate at higher EIRP to provide wider coverage, higher capacity, and improved connectivity.

	Handset	Base station
EIRP	30 dBm	55 dBm
N_{ANT}	4-6 (estimate)	64
Average P_{T0}	11-15 dBm	16 dBm
Maximum P_{T0}	20-25 dBm	25 dBm

As V_{DD} is strongly limited by the device technology breakdown voltage constraints, PA designers look to architectural solutions to reduce the high voltage swings that a single device needs to sustain and at the same time achieve high output power. One strategy is to use stacked or cascode PA structures compared to standalone common-source structures [5]. The cascode PA consists of stacking one common-source transistor on top of a common-gate transistor such that the maximum output voltage swing of each individual transistor (V_{MAX}) is proportional to nominal V_{DD} to enhance the overall output voltage by $2*V_{MAX}$. In stacked PAs, the overall output voltage swing of a stack of *N* devices is ideally increased by $N*V_{MAX}$ thus increasing output power by $(N*V_{MAX})^2$. In practice, the stack should not consist of more than 4 devices to avoid stability issues and also amplitude and phase imbalance between the transistors (due to intrinsic and extrinsic parasitic components) which lowers the efficiency comparable to that of a standalone PA [6].

Another design strategy to maximize output power delivered by PAs is to optimize output load impedance. Power matching, which is not necessarily conjugate matching, consists of presenting an optimal load impedance $ZL_{opt} = R_{opt} + jX_{opt}$ with a lower resistive part (R_{opt}) to maximize the current flowing across the load and a reactance part (X_{opt}) that increases either the voltage or current swings [7]. Determining ZL_{opt} by handbook calculations is not simple as it seems, since it is necessary to consider device non-idealities, layout and/or packaging effects which can rapidly complicate these calculations. In order to identify the optimal operating point (max gain/max PAE), load pull measurement systems provide a practical solution for large-signal characterization of active devices by synthetizing R_{opt} and X_{opt} for a fixed frequency. Large-signal PA characterization on a load pull setup will be introduced later on in Chapter 2.

1.2 Semiconductor technologies for RF/mmW PAs

1.2.1 F_T/F_{MAX} comparison in different technologies

The RF gain performance of a PA is strongly dependent on the transistor's figure of merits, i.e., transition frequency (F_T) and maximum oscillation frequency (F_{MAX}). F_T and F_{MAX} refer to the frequency at which the current gain and unilateral power gain reaches unity (gain=0) respectively. To achieve sufficient power gain and efficiency, F_T/F_{MAX} values should be greater than 3 to 5 times the operating frequency [3], implying that transistors targeting mmW applications need F_T and F_{MAX} greater than 150GHz. The comparison of F_T and F_{MAX} across different silicon (CMOS bulk and SOI, SiGe HBT) and III-V (GaAs, GaN, InP) technologies is shown in Figure 1-6 [8].

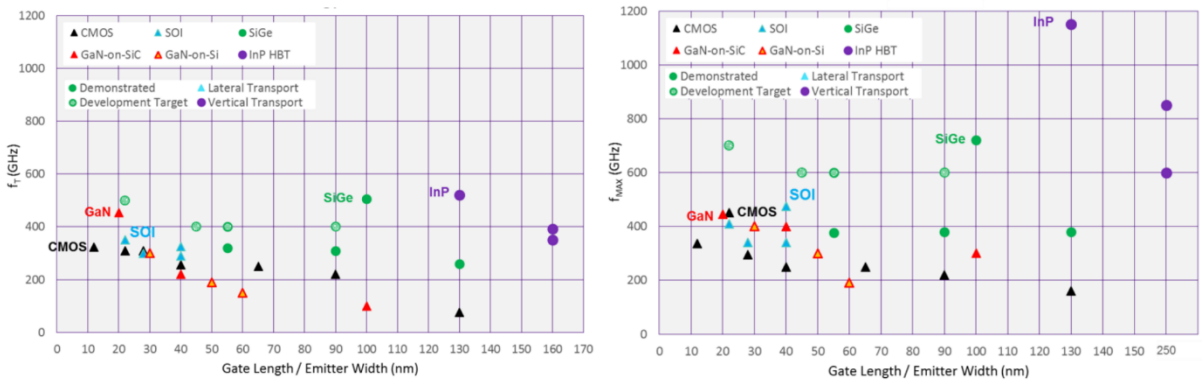

Figure 1-6 : RF performance benchmark of F_T and F_{MAX} for state-of-the-art silicon and III-V transistors [8]

In CMOS-based technologies (bulk and SOI), channel length downscaling has greatly improved F_T/F_{MAX} to the range of 200 – 450GHz for sub 100nm nodes. The limiting factor in enhancing the F_T/F_{MAX} beyond 400GHz is due to the impact of higher gate resistance and increased device parasitic capacitances which degrades the carrier mobility. The side effect of channel length scaling in CMOS devices is the power density limitation, arising from low breakdown voltages. F_T/F_{MAX} of SiGe heterojunction bipolar transistor (HBT) is reported to achieve 500GHz/700GHz (without CMOS integration), thus making it a viable choice for sub-THz applications.

For III-V technologies, F_T/F_{MAX} of GaN-based devices is at the same range of scaled CMOS devices but lower compared to InP HBTs. However, GaN devices are capable of handling higher power density since they have higher breakdown voltages (larger bandgap) than CMOS-based devices. Despite the promise that III-V technology holds, CMOS devices remain the popular candidate for most of the mmW applications, attributed to advantages such as integration of analog and digital circuits in front-end modules and cost-efficient manufacturing.

1.2.2 Power requirements for wireless communication standards

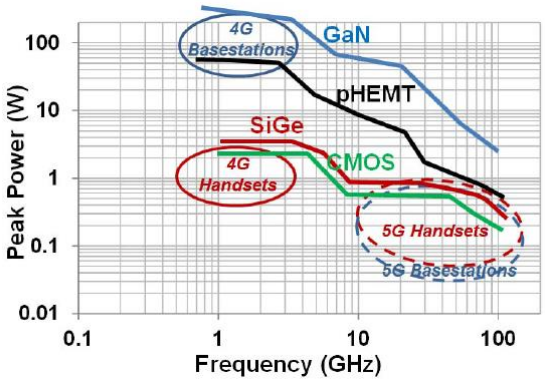

Figure 1-7 : Peak power specifications for 4G and 5G communication standards [4]

Another important criterion in technology choice for mmW PAs is the peak power requirement levels which have seen progressive reduction from 4G to 5G communication standards, as illustrated in Figure 1-7 [4]. This is the result of EIRP improvements brought on by beamforming antenna arrays. Historically, GaAs pHEMT served as the main technology for base station PAs before the emergence of GaN amplifiers. Both of these devices support higher power density to provide higher EIRP than that of handset units. Interestingly, CMOS becomes an attractive technology for mmW PAs in 5G handset and small cell usage, as the required peak power per power amplifier is scaled down to below 1W.

1.2.3 SOI CMOS devices for RF/mmW applications

Silicon-on-Insulator (SOI) based CMOS devices are fabricated on a buried oxide layer has many advantages as it reduces parasitic capacitances, substrate noise, leakage current, as well as providing natural latch-up immunity [9, 10]. As illustrated in Figure 1-8, there are two types of SOI CMOS transistors, which are known as Partially-Depleted SOI (PDSOI) and Fully-Depleted SOI (FDSOI) transistors. The major differences between the two SOI CMOS devices are based on the thickness of the active silicon (body) layer (t_{Si}) and the thickness of BOX layer (t_{BOX}). In PDSOI devices, the depletion region does not completely extend over the entire body region. When the body of a PDSOI device is tied to the source or the ground, it is known as a body-contacted device and has similar characteristics as a bulk CMOS device. This suppresses occurrence of floating body effects, which arise from the accumulation of minority carriers in the undepleted body region, since they are evacuated via the body contact [11]. Due to thinner body layer in FDSOI devices ($t_{Si} \leq$50nm), the active region is fully depleted. Combining this with thin BOX layer leads to full electrostatic control of the channel

and thus significantly reducing short-channel effects, which is one of the limiting factors in CMOS device scaling. PDSOI has found success in the RF front-end module market as it is compatible with high resistivity substrate which provides improved RF passive component performances and limits substrate coupling [12]. FDSOI technology mainly targets high-speed digital and ultra-low power applications by leveraging its body-bias tuning feature via a back-gate terminal [9].

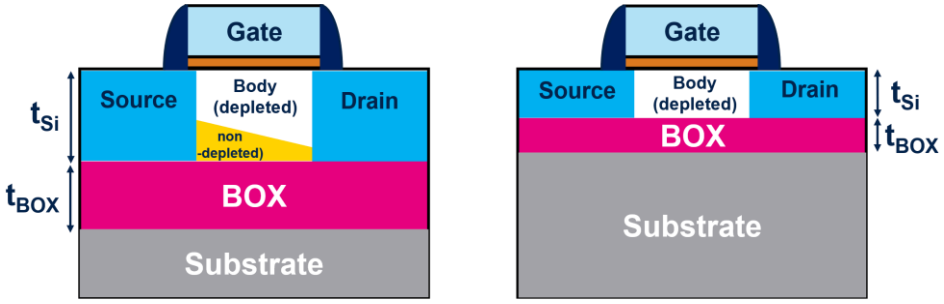

Figure 1-8 : Representation of an NMOS transistor in PDSOI (left) and FDSOI (right) technology.

1.3 Reliability challenges of RF/mmW PA applications

1.3.1 Introduction to CMOS reliability

Reliability of a semiconductor device refers to its ability to perform its intended function over an expected time duration in a specified use case such as voltage, temperature, duty cycle, and environmental factors, which is defined by the mission profile for a targeted application. Over the last few decades, the critical dimensions of the CMOS transistor have been continuously shrinking with the goal of gaining high performance and low power devices mainly implemented in VLSI technology. It was discovered that device scaling yields lower reliability margins thus significant research efforts were employed to understand and model the reliability physics in transistor aging [13]. This section presents the main reliability concepts of degradation and failure mechanisms concerning RF/mmW PAs, respectively associated to hot carrier injection (HCI) and time-dependent dielectric breakdown (TDDB).

1.3.1.1 CMOS reliability mechanisms concerning RF/mmW PAs

A. Hot carrier injection (HCI)

Hot carriers appear in the MOSFET channel when a high electric field is applied on the drain terminal which causes the carriers (holes or electrons) to acquire large kinetic energy across in the pinch-off region. For bias conditions in saturation mode with high V_{GD} ($V_T<V_{GS}<<V_{DSAT}$), the hot carriers can trigger the impact ionization (II) process located at the drain region by generating electron-hole pairs. The injection mechanism depends on the vertical electric field, determined by the gate bias voltage which modulates the energy barrier of Si/SiO2 interface. Subsequently, the “lucky” carrier, corresponding to the II-generated carriers that are able to surmount the Si/SiO2 energy barrier (~3.1eV for electrons and 4.7eV for holes), are injected into gate oxide which create defects in the oxide or at the Si/SiO2

interface along the channel. The formation of defects then leads to device parametric degradation and may contribute to device failure.

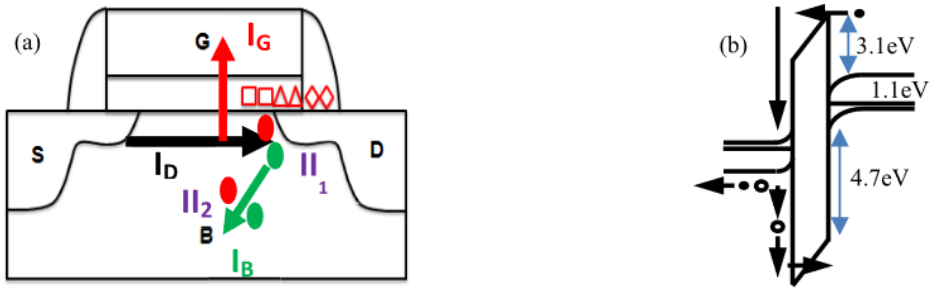

Figure 1-9 : (a) Impact ionization (II) process in an NMOS device localized at the drain region [14]. (b) The energy band diagram showing the amount of energy required for electron or hole injection at the Si/SiO2 interface [14]

Early HCI studies [15], [16], [17] on long channel devices (L>180nm) have reported that the carrier heating phenomenon is primarily driven by the high lateral electric field between the drain and channel pinch-off point (V_{DS}-V_{DSAT}). However, the downscaling of channel length and oxide thickness combined with the non-proportionate voltage scaling in advanced CMOS nodes introduced novel mechanisms of channel hot carrier transport in short-channel MOSFETs. The authors in [18] found that the energy exchange between carriers, known as carrier scattering, is responsible for the generation of hot carriers in ultra-scaled devices (gate length L<100nm). This is due to the quasi-ballistic transport of carriers in the case where the channel length is comparable or smaller than the mean free path of carriers, implying the lower probability of scattering events during carrier acceleration [19]. Among the different scattering mechanisms, it has been demonstrated in [20] using carrier energy distribution that electron-electron scattering (EES) leads to the enhancement of hot-carrier degradation in short-channel NMOS under high V_G stress conditions. The higher carrier density driven by V_G increases the probability of collision between the carriers under EES, resulting in the population of higher energy fractions beyond the lateral applied drain bias ~qVd, producing a high energy tail in the carrier distribution as shown Figure 1-10. Hence, the hot-carrier degradation models focusing on the energy-driven characteristics of hot carrier transport and defect generation have been adopted, which will be discussed later in this section.

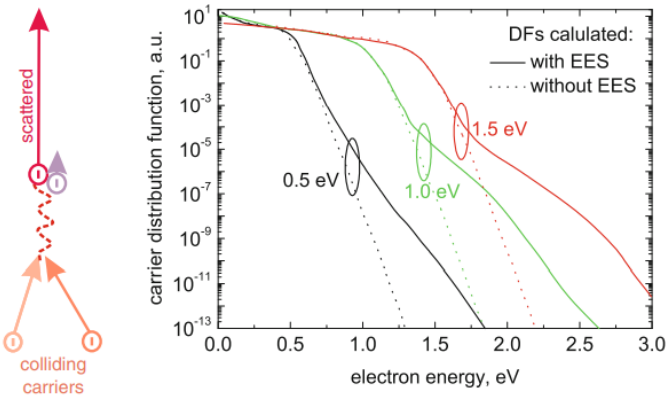

Figure 1-10: Under quasi-ballistic transport conditions, the EES mechanism may occur where an electron gains almost twice the kinetic energy (~2qVd) after collision. [21]

As mentioned previously, the injection of hot carriers, aided by the vertical field, contributes to the generation of defects at the Si/SiO2 interface (known as interface states) and in the gate oxide layer (known as oxide traps). Interface states are formed through a two-step process where the first step involves the Si3≡Si-H bond dissociation induced by hot carriers, followed by the release of the hydrogen species H* which produces a de-passivated Si3≡Si* dangling bond (commonly known as Pb centers). Thus, interface states act as trapping centers to capture electrons or holes to become positively or negatively charged which degrade the MOSFET electrical parameters. The creation of oxide defects, i.e., bulk and border traps have less influence on the HCI-induced electrical parameter drift in thin gate-oxide of scaled devices [22]. The Si-H bond dissociation concept has been reported by the Hess group as the competition between defect creation by single particle (SP) and multiple particle (MP) carriers [23]. Similar to the lucky electron concept, the SP process (also known as single vibrational excitation (SVE)) can be explained by the energy transfer of a single high-energy carrier to break the bond. The MP process consists of the multi-vibrational excitation (MVE) of the Si-H bond where the bond excitation occurs due to bombardment of several cold carriers with low energy.

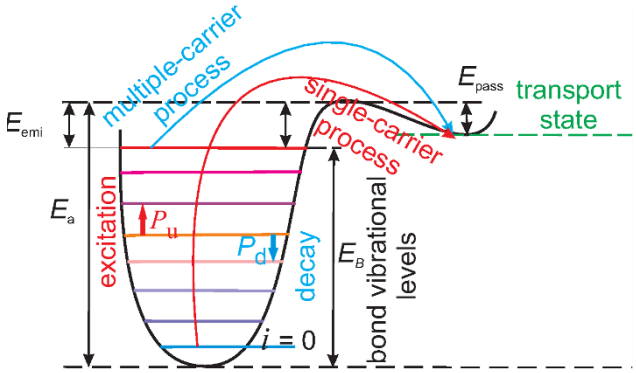

Figure 1-11 :SP and MP bond dissociation process [24]

As illustrated in

Figure 1-11, the bond excitation energy rate (P_u) rises as a result of the energy deposited by the increasing interaction between multiple cold carriers which weakens the bond. When the last bonded state is achieved, bond dissociation is eventually triggered (hydrogen release). In principle, it is assumed that the carrier flux instead of carrier energy is enough to create interface defects through the MVE bond dissociation mechanism.

From the current state-of-the-art, it is evident that the role of carrier transport contributing to interface state generation is fundamental in the HCI modeling approach. In the following, we will describe the HCI modeling evolution from field-driven to energy-driven approach.

- Field-driven model:

The lucky electron model (LEM) was proposed by the authors in [16] to relate the interface state generation threshold energy Φ_{IT} with the II process threshold energy Φ_{II}. The ratio of the substrate current to the drain current, used as a monitoring parameter of the impact-

ionization rate, is dependent on the energy gained by the hot carriers accelerated by peak lateral field E_{max} along the mean free path λ without collisions:

$$\frac{I_{SUB}}{I_D} \propto exp\left(-\frac{\Phi_{II}}{q\lambda E_{max}}\right) \quad \text{(Eq.1-6)}$$

The interface state generation rate can then be described as a time-dependent function of the lucky hot carriers having surmounted the Si/SiO2 barrier with an energy threshold of Φ_{IT}:

$$\Delta N_{IT} \propto \left[t.\frac{I_D}{W}.exp\left(-\frac{\Phi_{IT}}{q\lambda E_{max}}\right)\right]^n \propto \left[t.\frac{I_D}{W}.\left(\frac{I_{SUB}}{I_D}\right)^{\frac{\Phi_{IT}}{\Phi_{II}}}\right]^n \quad \text{(Eq.1-7)}$$

The device lifetime τ to achieve a given value of ΔN_{IT} is define with a constant m= Φ_{IT}/Φ_{II}.

$$\tau \propto \left(\frac{I_D}{W}\right)^{-1}\left(\frac{I_{SUB}}{I_D}\right)^{-m} \quad \text{(Eq.1-8)}$$

From eq.1-7, it is clear that the worst-case condition for HCI corresponds to the maximum substrate current (at $V_G \sim V_D/2$). However, for ultra-scaled devices, the interface state generation rate is no longer limited to only field-accelerated single-carrier mechanism, i.e., lucky hot carriers. As a result, the worst-case HCI condition shifts from $V_G \sim V_D/2$ (long channel NFET device) to $V_G \sim V_D$ (short channel device NFET and PFET) as observed from experimental data in [14].

- Energy-driven model:

The energy-driven approach introduced by [20] considers the contribution of EES in the II rate (r_{II}) dependence as shown in eq.1-9:

$$\tau \propto f(I_D)\left(\frac{I_{SUB}}{I_D}\right)^{-m} \propto f(I_D)\, r_{II}^{-m} \quad \text{(Eq.1-9)}$$

where $f(I_D)$ is a bias-dependent function that is determined by two different transport regimes. Considering that I_D increases with V_G for a given V_D, the first regime concerns the SVE degradation mode (similar to LEM) represented by low I_D and low V_G conditions, as a result of direct heating due to the strong lateral field. In this high-energy regime, $f(I_D)$ is a linear function of I_D such that $f(I_D) = (I_D/W)^{-1}$. The second medium energy regime covers the mid-V_G range in which $f(I_D) = (I_D/W)^{-2}$ exhibits a quadratic behavior owing to the moderate energetic carriers accelerated through the EES process to access energy levels required for bond dissociation. The authors in [25] extended the energy-driven approach to account for the low energy regime when entering the high V_G range where carrier transport is concentrated at the interfacial inversion layer. The HCI degradation in this regime is governed by the MVE process caused by the increased cold-carrier flux and is described as $f(I_D) = (I_D/W)^{-E_B/\hbar\omega}$. Finally, a complete device lifetime model is established as the contribution of three HCI modes competing in parallel:

$$\frac{1}{\tau} = \frac{K_{SVE}}{\tau_{SVE}} + \frac{K_{EES}}{\tau_{EES}} + \frac{K_{MVE}}{\tau_{MVE}} \quad \text{(Eq.1-10)}$$

The significant feature of HCI degradation is the strong damage localization at the drain region resulting in the time-dependent variation of MOSFET electrical characteristics. It has been widely documented that the hot carrier-induced defects cause threshold voltage (V_T) drift, transconductance (gm) and linear (I_{Dlin}) and saturation (I_{Dsat}) drain current reduction as presented in Figure 1-12.

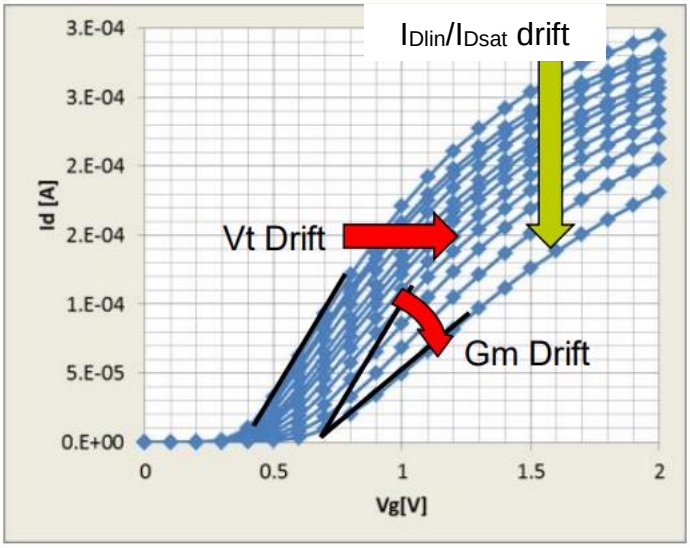

Figure 1-12 : Impact of hot carrier degradation on MOSFET I_DV_G characteristics [26]

Since these electrical parameters are representative of the HCI damage, the correlation between the parametric degradation and the bias dependence of the device can be made to empirically model HCI degradation. The authors in [15] presented a simple HCI model where the drift of a given parameter ΔD is fitted using a power law time dependence and a coefficient A which describes the V_D dependence of the impact ionization rate:

$$\Delta D = A.t^n \propto exp(-\alpha/V_D).t^n \quad \text{(Eq.1-11)}$$

The advantage of this modeling approach is that the device lifetime from the accelerated DC HCI stress conditions to real device operation voltages can be easily extrapolated. Another empirical model derived from the energy-driven paradigm was proposed by [27]. Similar to the model in Eq.1-12, a time power law is used to model the device parameter drift. Additional terms were incorporated to model the carrier energy proportional to $(V_D - V_{DSAT})$ while the injected carrier density is modulated by the term $(V_G - V_T)^p$.

$$\Delta D = A.t^n.exp[B.(V_D - V_{DSAT})].(V_G - V_T)^p \quad \text{(Eq.1-12)}$$

In comparison to the model of Eq.1-9 which is a function of I_B/I_D, this model is suitable for bulk and especially FDSOI devices which body is isolated from the substrate. As illustrated in Figure 1-13, the model is able to capture the device scaling properties as well as bias dependence from low to high V_G.

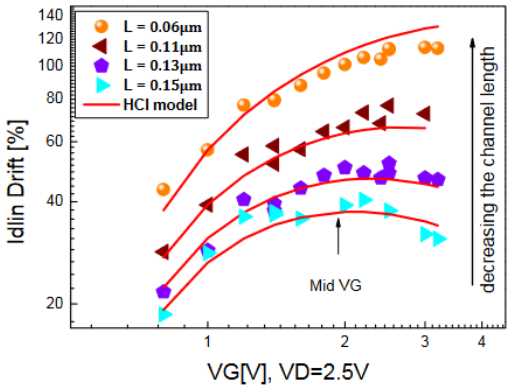

Figure 1-13:I_{Dlin} degradation computed by HCI model of Eq 1-12 shows good agreement with experimental data for different device channel length and gate stress bias [27]

Research in AC effects on HCI degradation started to gain interest as the reliability criterion imposed by DC stress on logic circuits became more restrictive with technology scaling. The pioneering work on AC lifetime modeling was done by [28] on the basis that it is computed by integrating the degradation over a sequence of short DC stresses. This quasi-static (QS) interpretation has evolved into the AGE function which is implemented in reliability simulators to predict AC and/or RF degradation for time-varying stresses under different bias conditions. The authors in [29] demonstrated the AGE function using the QS approximation for a time power-law type DC degradation ΔP that is given by:

$$\Delta P(t) = C.[f(V_i).t]^n \qquad \text{(Eq.1-13)}$$

where C is a constant, n is the power-law time exponent with values between 0 and 1, and $f(V_i)$ is a function of the MOSFET terminal voltages. The constant-bias degradation rate can be obtained as:

$$\frac{d\Delta P(t)}{dt} = n.f(V_i).C^{1/n}.[\Delta P(t)]^{1-1/n} \qquad \text{(Eq.1-14)}$$

such that the time dependence of $d\Delta P(t)/dt$ can be removed to provide a practical implementation of the QS approximation. In the case that the bias voltage varies slowly in a way that the degradation rate is assumed to remain constant over a given stress duration, the QS approach assumes that:

$$\frac{d\Delta P(t)}{dt} = n.f(V_i(t)).C^{1/n}.[\Delta P(t)]^{1-1/n} \qquad \text{(Eq.1-15)}$$

By separation of variables, eq.1-15 can be expressed as:

$$\frac{d\Delta P(t)}{n.[\Delta P(t)]^{1-1/n}} = f(V_i(t)).C^{1/n}.dt \qquad \text{(Eq.1-16)}$$

After integrating both sides of eq.1-16, the AGE function is defined as:

$$\Delta P(t) = C.\left[\int_0^t f(V_i(t')).dt'\right]^n \quad \text{(Eq.1-17)}$$

$$AGE(t) = \int_0^t f(V_i(t')).dt' \quad \text{(Eq.1-18)}$$

During circuit aging simulations, the age rate, which correspond to $f(V_i(t'))$, is calculated for each device in the circuit at each time step. Then, ΔP over one period of AC signal ($\Delta P(T_{period})$) is computed by the AGE function. To achieve device or circuit lifetime prediction for a longer simulation time frame, e.g., T_{SIM}=10 years, the total degradation of $\Delta P(T_{SIM})$ is generally extrapolated as shown in eq.1-19.

$$\Delta P(T_{SIM}) = \Delta P(T_{period}).\left(\frac{T_{SIM}}{T_{period}}\right)^n \quad \textit{(Eq.1-19)}$$

The QS approach for HCI degradation modeling has been confronted to experimental data for RF stress at the drain terminal with an amplitude of V_{DMAX} (gate terminal kept constant DC bias V_G=V_{DMAX} for on-state condition) of an NMOS device [30]. No frequency dependence was reported for ΔV_{TLIN} and Δ_{IDSAT} between 10MHz and 3.2GHz. By applying RF stress on both gate and drain terminals, the authors in [31] reported that the QS modeling approach is in good agreement with experimental data at 6GHz and 10GHz corresponding to class A PA operating conditions without any significant frequency dependence on ΔI_{DLIN}. In [32], the QS approach applied to the energy-driven HCI model (similar to eq.1-10) is able to reproduce ΔI_{DSAT} after RF HCI stress measurements at 60GHz of a class A PA. Based on these results, it is clear that HCI degradation modeling using the QS approach is applicable for NMOS PA devices subjected to on-state RF stress up to 60 GHz.

B. Time-dependent dielectric breakdown (TDDB)

Dielectric breakdown refers to the loss of the dielectric layer's insulating properties. TDDB is caused by the random defect creation when an electrical and/or thermal stress is applied, which results in the formation of a percolation path within the dielectric layer over time. For CMOS technology, the gate dielectric layer contains silicon-dioxide (SiO_2) based materials, thus the term oxide breakdown is commonly found. Figure 1-14 illustrates the gate (IG) and substrate (IB) current of a CMOS transistor, monitored under constant gate voltage stress. It can be observed from IG that the several breakdown events occur during stress, where the initial breakdown is known as soft breakdown (SBD), incurs an increase in noise level until the abrupt jump of several orders in magnitude of both IG and IB marks the hard breakdown (HBD). The transistor remains operational after SBD whereas the HBD is a catastrophic failure which renders the transistor non-operational. The time-to-breakdown (T_{BD}) in TDDB studies is usually defined by HBD.

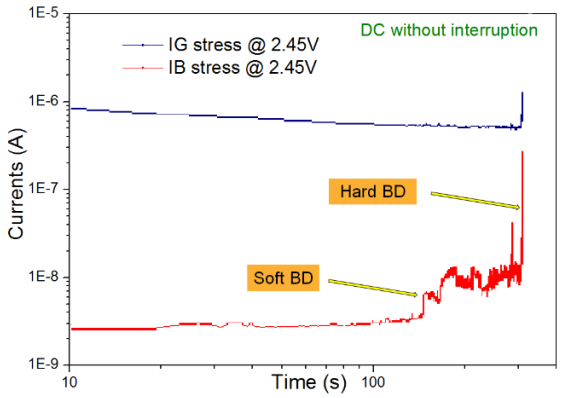

Figure 1-14 : During constant voltage stress, HBD can be detected by IG monitoring while both HBD and SBD can be detected by IB monitoring [33]

The stochastic nature of the TDDB is characterized by probability distribution functions which enable the representation of a large number of tested samples by a few parameters in order to perform statistical analysis of experimental data. The Weibull distribution has been widely applied in TDDB experimental data analysis due to its compatibility with the weakest link properties of hard breakdown. The cumulative distribution function F describes the failure rate of a population of tested devices given by eq.1-20. In order to obtain a linear relation between time (t) and F(t), eq.1-20 is transformed into eq.1-21, which is also known as the Weibull function (W). T_{63} denotes the characteristic time at which 63% of tested samples achieve hard breakdown. β represents the slope parameter of the Weibull distribution which can be easily extracted from the linear plot of eq.1-21. Higher β translates to a smaller T_{BD} dispersion of the samples, while smaller β means that the T_{BD} dispersion is large, with $\beta \leq 1$ indicating early device failure due to extrinsic defects (process-induced instead of intrinsic defects (stress-induced).

$$F(t) = 1 - e^{\left(-\frac{t}{T_{63}}\right)^{\beta}} \qquad \textit{(Eq.1-20)}$$

$$W(F) = \ln(-\ln(1 - F(t)) = \beta.\ln(t) - \beta.\ln(T_{63}) \qquad \textit{(Eq.1-21)}$$

The concept of critical defect density has been instrumental in explaining the breakdown statistics based on defect generation in the dielectric layer. The percolation model developed by [34] revealed that the oxide thickness T_{OX} and the lattice constant of a_0 (equivalent to defect diameter) is correlated to β according to eq.1-22, in agreement with experimental data. This points out that oxide thickness scaling results in a lower β value, which is the consequence of the decrease in critical defect density in thinner oxides. It should be noted that β is independent of stress voltage.

$$\beta = \alpha \frac{T_{OX}}{a_0} \qquad \text{(Eq.1-22)}$$

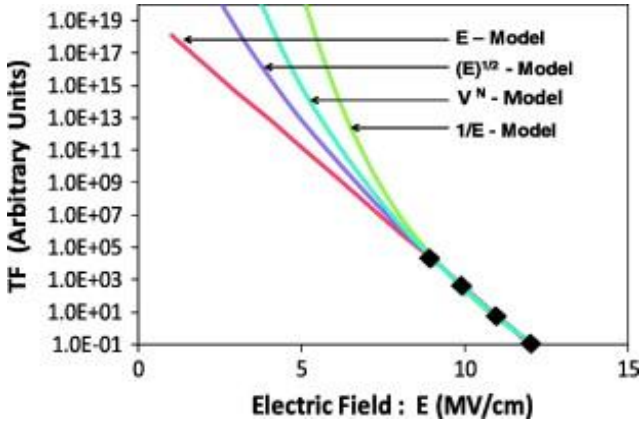

Figure 1-15 : Time-to-failure projections of different TDDB models [35]

Empirical TDDB models describe the oxide defect generation behavior to predict T_{BD} by using voltage or electric field (E-field) dependent acceleration factor, extracted from wafer level oxide breakdown tests under TDDB accelerated stress conditions, i.e., high stress voltages/temperatures. TDDB models provide oxide lifetime projections at lower voltages where prolonged stress durations (in the order of months/years) are required to achieve device breakdown. As shown in Figure 1-15, the extrapolation of time-to-failure at low E-fields/voltages can vary by several orders of magnitude depending on the choice of the TDDB model with the E-model being the most conservative model. Each model is based on different physical explanation of defect generation which is discussed in the following [35], [36], [37]:

- E-model (thermochemical model):

$$T_{BD} \sim \exp(-\gamma_V V) \sim \exp(-\gamma_E E) \qquad \text{(Eq.1-23)}$$

This is a field-driven model where the formation of defects in the oxide results from Si-O bonds broken by thermal activation which is strongly dependent on the electric field. Oxide breakdown is triggered when the critical number of broken bonds is locally achieved. However, this model assumes that neither carrier injection nor conduction current participates in the breakdown process, thus raising questions about its ability in providing realistic T_{BD} projections.

- 1/E model (anode hole injection model):

$$T_{BD} \sim \exp(G_V V) \sim \exp(-G_E/E) \qquad \text{(Eq.1-24)}$$

In this model, the oxide degradation process is associated with hole generation at the anode and injected back through the oxide (gate) due to Fowler-Nordheim tunneling. This current conduction mode dominates at large oxide fields (> 5MV/cm), which could not explain the hole generation rate and efficiency at low field/voltages [38].

- Power law model (anode hydrogen release model):

$$T_{BD} \sim V^{-n} \sim E^{-n} \quad \text{(Eq.1-25)}$$

The power law model is widely accepted in TDDB lifetime projections for ultra-thin dielectrics (T_{OX}<4nm) where the ballistic carrier transport dominates. The mobile hydrogen species released during the interface state creation diffuse towards the gate oxide under the applied field is believed to create traps within the oxide bulk [39].

- Square-root of E model:

$$T_{BD} \sim \exp\left(-m_V \sqrt[2]{V}\right) \sim \exp\left(-m_E \sqrt[2]{E}\right) \quad \text{(Eq.1-26)}$$

The model originates from the current-induced oxide degradation based on Poole-Frenkel conduction mechanism. This model has been adopted for TDDB modeling of low-k dielectrics, where the presence of shallow oxide traps, favoring the Poole-Frenkel effect, is due to the impurities found in low dielectric constant (low-k) dielectrics used for middle-end or back-end of line [40].

Supported by numerous experimental results reported in the literature, the voltage power law TDDB model provides realistic T_{BD} projections for thin-oxide devices at voltage below 3V. The complete T_{BD} model is given in Eq.27 which describe the dependence of NMOS dielectric properties (β), area (W, L) and temperature acceleration factor (T). The power law dependence of the stress voltage has strong implications on the predicted outcome of T_{BD} since the voltage acceleration factor (n) has a range between 30 and 44 (depending on stress conditions). As a consequence, it is necessary to ensure stress voltage integrity during TDDB stress measurements.

$$T_{BD} = A.\frac{1}{WL}^{1/\beta} e^{\frac{E_a}{kT}}.e^{\frac{\ln(-\ln(1-F))}{\beta}}.V_{stress}^{-n} \quad \text{(Eq.1-27)}$$

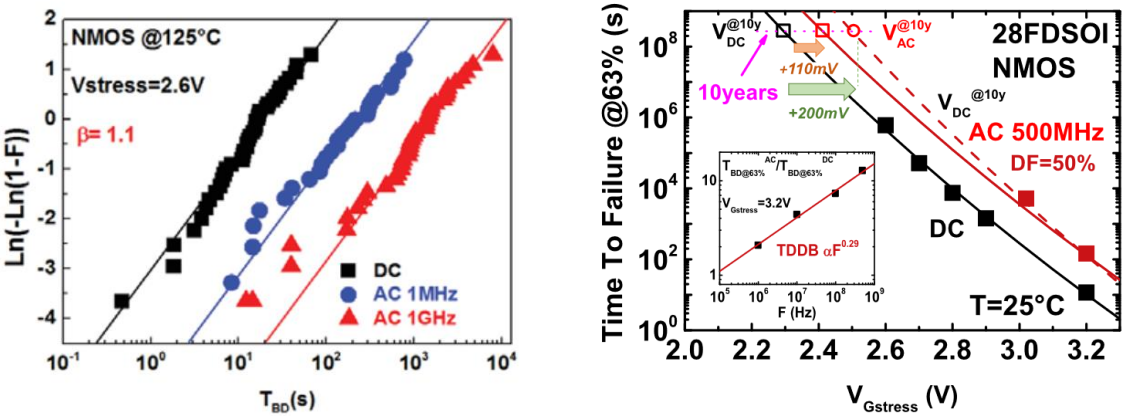

Figure 1-16 : (left) Experimental data from on-state AC TDDB shows an increase in T_{BD} compared to DC TDDB [41]. (right) For a targeted device lifetime of 10 years, the DC TDDB model shows a more conservative lifetime prediction compared to the AC TDDB model [42]

Considerable efforts have been dedicated into AC TDDB research in the last decade to assess the device lifetime enhancement at higher frequencies (Figure 1-16), which could potentially

benefit logic and RF circuits. AC TDDB characterization reported in the literature mostly involve high-k metal-gate (HKMG) transistors stressed at high gate voltage at a few Hz to 1MHz using standard test setup [43], [44], [45], [46]. Specific test setup and structures to guarantee AC TDDB stress signal integrity (voltage overshoots, transition time and duty cycle) at frequencies MHz to GHz range have been recently reported in [41], [42]. At present, the physical origin that causes T_{BD} improvement under AC TDDB is still under debate. The authors in [43] demonstrated through fast BTI measurements, where the stress interruption for IV characterization is performed within very short duration (1.5µs) to suppress charge de-trapping, that V_T drift doesn't show any frequency dependence with unipolar AC gate stress. This implies that the charge de-trapping mechanism during the relaxation part of the AC stress signal cannot explain the gain of AC/DC T_{BD}. Another physical theory reported by [47] states that the reduction of local electric field due to the lack of full dielectric polarization response (dielectric relaxation) is responsible for the AC TDDB enhancement. According to the results in [46], [48] different defect (interface state) generation rates have been reported for DC and AC stress cases following the different time exponent of stress-induced leakage current (SILC) measurements. Based on this hypothesis, the authors in [49] presented a frequency power law model with the following assumptions:

- T_{BD} increases uniquely as a function of the pulse duration of the stress part (independently of relaxation part) due to the non-constant defect generation rate.
- The number of defects cumulated at each stress pulse does not depend on the previous sequences, i.e., historical/recovery effects.

The T_{BD} model for AC stress waveform can then be described as the number of pulses *N*, each of a stress duration τ, to achieve the critical number of defects N_{BD} in the event of breakdown:

$$T_{BD} = N.\tau \quad \text{(Eq.1-28)}$$

where N_{BD} is related to *N* and the number of defects generated in a period N_{DEF} described by:

$$N_{BD} = N.N_{DEF} \quad \text{(Eq.1-29)}$$

and N_{DEF} is represented by a time power law dependence with the exponent n :

$$N_{DEF} = A.\tau^n \quad \text{(Eq.1-30)}$$

By inserting Eq.1-29 and Eq.1-30 into Eq.1-28, the expression of AC T_{BD} is given by:

$$T_{BD} = \frac{N_{BD}}{N_{DEF}}.\tau = \frac{N_{BD}}{A.\tau^n}.\tau = \frac{N_{BD}}{A}.\tau^{1-n} \quad \text{(Eq.1-31)}$$

which can be expressed as a function of the stress frequency F = 1/τ.

$$T_{BD} = \frac{N_{BD}}{A}.\mathrm{F}^{n-1} \quad \text{(Eq.1-32)}$$

The T_{BD} prediction of the proposed model (eq.1-32) is consistent with the on-state TDDB experimental results from 1 MHz to 1GHz stress frequencies for an NMOS device [41], by exhibiting a frequency exponent n - 1=0.3 (refer to inset graph of Figure 1-16(b)). Despite the model's limitations in justifying the physical origins of AC TDDB, it is capable of effectively modeling the AC dependence of crucial TDDB parameters such as frequency and temperature dependence as well as voltage acceleration factor [50].

1.3.2 Trade-off between performance and reliability for CMOS RF/mmW PAs

The aggressive scaling of channel length and oxide thickness, new device architecture and gate dielectric materials has drastically improved the DC and RF performance of CMOS transistors. The reliability challenges arising from these process engineering improvements demand the understanding of reliability physics of different failure modes. The traditional approach for reliability assessment is based on DC reliability models built from accelerated DC stress characterization data at wafer-level device testing for worst case conditions, which involve high voltage, current or temperature stress. The extrapolation of device or circuit lifetime by the acceleration models to real operation voltage or temperature is then evaluated against the failure criteria. For wear-out mechanisms such as HCI, it is generally defined by a targeted percentage of device parameter degradation for a fixed duration, e.g., $\Delta I_{DSAT} = 10\%$ for 10 years. For oxide TDDB failure, the criterion is determined by the failure rate for a given oxide area and duration, e.g., 100 ppm failure rate for 10 years at 0.1cm² of gate oxide area.

From the perspective of RF applications, the failure criteria based on DC reliability assessment are not representative of the device's mission profile where the lack of consideration in the time-dependency of the degradation or failure mechanisms lead to conservative design rules. Particularly in the case of RF PAs, increasing V_{DD} remains one of the key strategies to meet high power requirements. As the PA breakdown is dominated by off-state TDDB at high drain voltage swing during off-mode, the trade-off evaluation between V_{DD} and off-state TDDB requires in-depth characterization of the frequency dependence for off-state TDDB to establish frequency acceleration factor in TDDB models, similar to the on-state RF TDDB model discussed previously. During off-mode stress in short-channel devices, hot-carriers generated under strong gate-induced drain current (GIDL) and impact ionization conditions can be injected into the gate-oxide near the drain edge which result in oxide breakdown [51], [52], [53]. T_{BD} is generally lower for off-state compared to on-state TDDB due to the non-uniform E-field applied on the dielectric layer, while a higher β suggests a longer percolation path correlated to smaller defect size [54]. Otherwise, a relatively higher drain stress bias is required to trigger breakdown in off-mode for NMOS devices. For mmW PAs, it is expected that off-state TDDB would not be a limiting failure mode as PAs only operate at P_{SAT} for 0.01% of the time period, illustrated in Figure 1-17, in complex modulation schemes with high PAPR are applied [55].

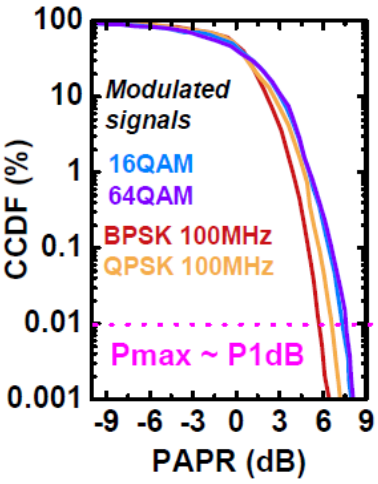

Figure 1-17 : CCDF (probability) represents the time spent at a specified power level PAPR. The PA operates at maximum power for 0.01% of the total time. [55]

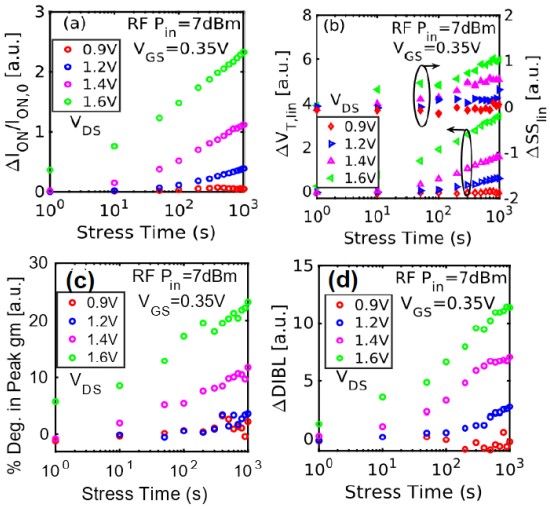

Figure 1-18 :Impact of RF HCI stress on the degradation of DC parameters. Worst-case degradation occurs for low V_G and high V_D [56].

However, in pushing the V_{DD} limits to improve the power performance in CMOS PA, HCI degradation is aggravated especially with ultra-scaled devices. Recently RF PA reliability studies mainly focus on HCI characterization using state-of-the-art load pull method to achieve large output voltage swings to obtain worst-case RF HCI stress on PA cell at various RF and mmW frequencies [55], [56], [57], [58], [59], [60], [61]. The worst case HCI degradation occurs at RF voltage swings with high V_{DS} and low V_{GS} (~V_T), usually at P_{SAT} or maximum PAE. In class A PAs, only on-state HCI degradation is present while in class AB and B PAs both on-state and off-state HCI degradation modes are present. In these studies, it has been revealed that RF HCI stress not only has a strong impact on the degradation of PA bias operating point, but also that RF performance drift is correlated with DC parametric degradation as presented in Figure 1-18. Hot-carrier DC stress investigations have demonstrated that on-state (V_{GS}>V_T) HCI degradation is more severe than off-state (V_{GS}≤V_T) HCI degradation [62]. However, it has been reported in [31] that the total hot carrier degradation is underestimated when the PA device is subjected to RF stress with on-state and off-state HCI degradation modes as shown in Figure 1-19. Thus hot carrier degradation under RF stress profile consisting on and off-state interaction merits further investigation.

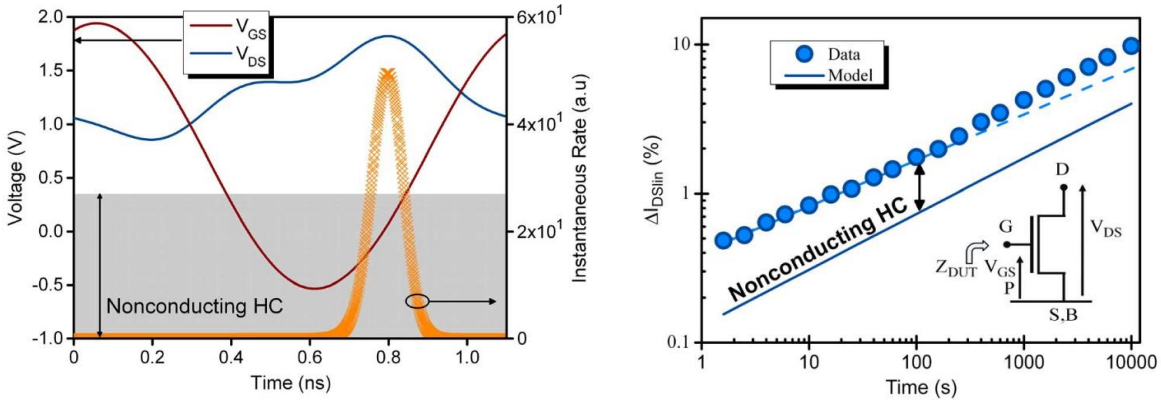

Figure 1-19 : (left) On-state and off-state HCI degradation modes in class AB PA voltage stress waveforms [31]. (right) In comparison with measurement data, HCI aging model, which only considers on-state degradation, underestimates the total degradation of the device [31].

1.3.3 PA Device lifetime modeling to circuit aging simulations

As discussed throughout this chapter, RF PA lifetime is governed primarily by on and off-state HCI degradation, as well as off-state TDDB failure mode. To accurately model RF PA degradation, it is essential that degradation models consider the different physical origins of each degradation or failure mechanism, as well as the interaction between different degradation modes, i.e., competing, or non-competing defect generation mechanisms, which could potentially introduce recovery behavior during aging. Aside from these DC degradation modeling challenges, RF modeling for mmW application is further complicated by the validity of the QS approximation that has laid the foundation of the AGE formalism in terms of frequency limitation. Currently, the QS approximation remains valid for RF and mmW frequencies until 60GHz for on-state RF degradation (as discussed in Section 1.3.1.1), whereas its validity for off-state RF degradation remains unclear.

Circuit aging simulations provide long-term reliability estimations for realistic circuit operating conditions. As reliability testing for product qualification under normal operating conditions consume a lot of time and resources, the evaluation of circuit or device aging using reliability simulators to optimize the performance and reliability trade-off can be done even at early design phases [63], [64]. Thus, the accuracy of aging models and their integration in reliability simulation flow play a pivotal role in delivering accurate lifetime predictions relevant to the product's mission profile description. The accuracy of aging models depends on their ability to capture stress dependent parameters of the device model related to the circuit FOM. In the context of PA degradation modeling, this involves mapping the adequate DC model parameters, i.e., V_T, mobility, DIBL, drain resistance, and subthreshold swing, which are correlated to the RF gain drift. Furthermore, the amount of degradation of each parameter is relative to the accuracy of the fresh device model, thus the model-to-hardware correlation should cover the V_{DS}/V_{GS} operating range of the mission profile. To summarize, degradation modeling approach for RF/mmW PAs still require further research in perspective of simulation model sensitivity.

1.4 Thesis organization

This work aims to address the reliability issues related to RF PAs in CMOS technology. In Chapter 2, the reliability modeling for RF HCI degradation is analyzed by means of a mission profile-based methodology. This methodology aims to investigate the impact of DC degradation models on the accuracy of RF performance drift modeling in an aging simulation flow. The frequency-dependence in off-state TDDB and hot-carrier degradation is characterized in Chapter 3 using an integrated test structure which generates on-chip dynamic stress stimuli at the drain terminal of an NMOS device at RF frequencies. Experimental results are presented to provide new modeling insights concerning the off-state behavior up to 1GHz, as well as interaction with on-state degradation, which contribute to the development of simulation modeling strategies encompassing the interplay between multiple degradation modes. Then, in Chapter 4, an aging compensation PA circuit design in FDSOI technology is proposed. The RF gain drift is mitigated by compensating the threshold voltage drift using an on-chip feedback system during aging measurements.

References

[1] T. Johansson and J. Fritzin, "A Review of Watt-Level CMOS RF Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 1, pp. 111–124, Jan. 2014, doi: 10.1109/TMTT.2013.2292608.

[2] K. Vivien, "Linearity and Efficiency of Load Modulated Power Amplifiers," École doctorale Mathématiques, Sciences et Technologies de l'Information et de la Communication, Université Paris-Est, 2020. [Online]. Available: http://www.theses.fr/2020PESC2026/document

[3] H. Wang, P. M. Asbeck, and C. Fager, "Millimete r-Wave Power Amplifier Integrated Circuits for High Dynamic Range Signals," *IEEE Journal of Microwaves*, vol. 1, no. 1, pp. 299–316, Jan. 2021, doi: 10.1109/JMW.2020.3035897.

[4] P. M. Asbeck, N. Rostomyan, M. Özen, B. Rabet, and J. A. Jayamon, "Power Amplifiers for mm-Wave 5G Applications: Technology Comparisons and CMOS-SOI Demonstration Circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 3099–3109, Jul. 2019, doi: 10.1109/TMTT.2019.2896047.

[5] J. Cui, S. Helmi, Y. Tang, and S. Mohammadi, "Stacking the Deck for Efficiency: RF-to Millimeter-Wave Stacked CMOS SOI Power Amplifiers," *IEEE Microwave Magazine*, vol. 17, no. 12, pp. 55–69, Dec. 2016, doi: 10.1109/MMM.2016.2608698.

[6] M. H. Montaseri, J. Aikio, T. Rahkonen, and A. Pärssinen, "Optimum Number of Transistors in Stacked CMOS Millimeter-Wave Power Amplifiers," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1–4. doi: 10.1109/ISCAS.2018.8351160.

[7] Steve Cripps, *RF Power Amplifiers for Wireless Communications, Second Edition*. Artech, 2006. [Online]. Available: http://ieeexplore.ieee.org/document/9101120

[8] N. Cahoon, P. Srinivasan, and F. Guarin, "6G Roadmap for Semiconductor Technologies: Challenges and Advances," in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, p. 11B.1–1. doi: 10.1109/IRPS48227.2022.9764582.

[9] S. Monfray, "UTBB FDSOI: Evolution and opportunities," in *Solid-State Electronics*, vol. 125, pp. 63–72, 2016. doi: 10.1016/j.sse.2016.07.003.

[10] B. Martineau, D. Belot, "Si and SOI CMOS technologies for millimeter wave wireless applications," in *2020 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2020, pp. 17.3.1–17.3.4. doi: 10.1109/IEDM13553.2020.9371997.

[11] X. Cai, C. Hai, "Study of body contact of partial depleted SOI NMOS devices," in *2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings*, 2006, pp. 212–214. doi: 10.1109/ICSICT.2006.306164.

[12] J.-P. Raskin, "SOI technologies for RF and millimeter-wave integrated circuits," in *2021 IEEE Latin America Electron Devices Conference (LAEDC)*, 2021, pp. 1–5. doi: 10.1109/LAEDC51812.2021.9437979.

[13] J. W. McPherson, "Scaling-induced reductions in CMOS reliability margins and the escalating need for increased design-in reliability efforts," in *Proceedings of the IEEE 2001. 2nd International Symposium on Quality Electronic Design*, Mar. 2001, pp. 123–130. doi: 10.1109/ISQED.2001.915216.

[14] S. Mahapatra and U. Sharma, "A Review of Hot Carrier Degradation in n-Channel MOSFETs—Part I: Physical Mechanism," *IEEE Transactions on Electron Devices*, vol. 67, no. 7, pp. 2660–2671, 2020, doi: 10.1109/TED.2020.2994302.

[15] E. Takeda and N. Suzuki, “An empirical model for device degradation due to hot-carrier injection,” *IEEE Electron Device Letters*, vol. 4, no. 4, pp. 111–113, Apr. 1983, doi: 10.1109/EDL.1983.25667.
[16] C. Hu, S. C. Tam, F.-C. Hsu, P. K. Ko, T.-Y. Chan, and K. W. Terrill, “Hot-Electron-Induced IMOSFET Degradation— Model, Monitor, and Improvement,” *IEEE Journal of Solid-State Circuits*, vol. 20, no. 1, pp. 295–305, Feb. 1985, doi: 10.1109/JSSC.1985.1052306.
[17] K. K. Ng and G. W. Taylor, “Effects of hot-carrier trapping in n- and p-channel MOSFET’s,” *IEEE Transactions on Electron Devices*, vol. 30, no. 8, pp. 871–876, Aug. 1983, doi: 10.1109/T-ED.1983.21229.
[18] S. E. Rauch and G. La Rosa, “The energy driven paradigm of NMOSFET hot carrier effects,” in *2005 IEEE International Reliability Physics Symposium, 2005. Proceedings. 43rd Annual.*, Apr. 2005, pp. 708–709. doi: 10.1109/RELPHY.2005.1493216.
[19] A. W. Strong *et al.*, *Reliability wearout mechanisms in advanced CMOS technologies*. in IEEE press series on microelectronic systems. Wiley, 2009. [Online]. Available: https://books.google.fr/books?id=68avDAEACAAJ
[20] S. E. Rauch, G. La Rosa, and F. J. Guarin, “Role of E-E scattering in the enhancement of channel hot carrier degradation of deep-submicron NMOSFETs at high V/sub GS/ conditions,” *IEEE Transactions on Device and Materials Reliability*, vol. 1, no. 2, pp. 113–119, Jun. 2001, doi: 10.1109/7298.956705.
[21] S. Tyaginov and T. Grasser, “Modeling of hot-carrier degradation: Physics and controversial issues,” in *2012 IEEE International Integrated Reliability Workshop Final Report*, South Lake Tahoe, CA, USA: IEEE, 2012, pp. 206–215. doi: 10.1109/IIRW.2012.6468962.
[22] S. Mahapatra, C. D. Parikh, V. R. Rao, C. R. Viswanathan, and J. Vasi, “Device scaling effects on hot-carrier induced interface and oxide-trapped charge distributions in MOSFETs,” *IEEE Transactions on Electron Devices*, vol. 47, no. 4, pp. 789–796, Apr. 2000, doi: 10.1109/16.830995.
[23] K. Hess, B. Tuttle, F. Register, and D. K. Ferry, “Magnitude of the threshold energy for hot electron damage in metal–oxide–semiconductor field effect transistors by hydrogen desorption,” *Applied Physics Letters*, vol. 75, no. 20, pp. 3147–3149, Nov. 1999, doi: 10.1063/1.125259.
[24] S. Tyaginov, M. Bina, J. Franco, Y. Wimmer, B. Kaczer, and T. Grasser, “On the importance of electron–electron scattering for hot-carrier degradation,” *Japanese Journal of Applied Physics*, vol. 54, p. 04DC18, Apr. 2015, doi: 10.7567/JJAP.54.04DC18.
[25] C. Guerin, V. Huard, and A. Bravaix, “The Energy-Driven Hot-Carrier Degradation Modes of nMOSFETs,” *IEEE Transactions on Device and Materials Reliability*, vol. 7, no. 2, pp. 225–235, Jun. 2007, doi: 10.1109/TDMR.2007.901180.
[26] R. Lajmi, “Caractérisation et modélisation du vieillissement des circuits analogiques et RF en technologie 28 nm FDSOI,” Ph.D thesis, Univ. Grenoble Alpes, 2019.
[27] W. Arfaoui *et al.*, “Energy-driven Hot-Carrier model in advanced nodes,” in *2014 IEEE International Reliability Physics Symposium*, Jun. 2014, p. XT.12.1-XT.12.5. doi: 10.1109/IRPS.2014.6861189.
[28] K. R. Mistry and B. Doyle, “AC versus DC hot-carrier degradation in n-channel MOSFETs,” *IEEE TRANSACTIONS ON ELECTRON DEVICES*, vol. 40, 1993.
[29] A. J. Scholten, D. Stephens, G. D. J. Smit, G. T. Sasse, and J. Bisschop, “The Relation Between Degradation Under DC and RF Stress Conditions,” *IEEE Transactions on*

Electron Devices, vol. 58, no. 8, pp. 2721–2728, Aug. 2011, doi: 10.1109/TED.2011.2153854.

[30] G. T. Sasse, "MOSFET Degradation Under RF Stress," *IEEE TRANSACTIONS ON ELECTRON DEVICES*, vol. 55, no. 11, 2008.

[31] L. Negre *et al.*, "Reliability Characterization and Modeling Solution to Predict Aging of 40-nm MOSFET DC and RF Performances Induced by RF Stresses," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 5, pp. 1075–1083, 2012, doi: 10.1109/JSSC.2012.2185549.

[32] V. Huard, T. Quemerais, F. Cacho, L. Moquillon, S. Haendler, and X. Federspiel, "Design-in reliability approach for Hot Carrier injection modeling in the context of AMS/RF applications," in *2011 International Reliability Physics Symposium*, Apr. 2011, p. 5A.5.1-5A.5.7. doi: 10.1109/IRPS.2011.5784517.

[33] A. Bezza, M. Rafik, D. Roy, X. Federspiel, P. Mora, and G. Ghibaudo, "New insight on the frequency dependence of TDDB in high-k/metal gate stacks," *2013 International Integrated Reliability Workshop Final Report*, Oct. 2013, pp.11-14.

[34] J. Sune, "New physics-based analytic approach to the thin-oxide breakdown statistics," *IEEE Electron Device Letters*, vol. 22, no. 6, pp. 296–298, Jun. 2001, doi: 10.1109/55.924847.

[35] J. W. McPherson, "Time dependent dielectric breakdown physics – Models revisited," *Microelectronics Reliability*, vol. 52, no. 9, pp. 1753–1760, Sep. 2012, doi: 10.1016/j.microrel.2012.06.007.

[36] J. H. Stathis, "Physical and predictive models of ultrathin oxide reliability in CMOS devices and circuits," *IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY*, vol. 1, no. 1, 2001.

[37] E. Y. Wu, "Facts and Myths of Dielectric Breakdown Processes—Part I: Statistics, Experimental, and Physical Acceleration Models," *IEEE TRANSACTIONS ON ELECTRON DEVICES*, vol. 66, no. 11, 2019.

[38] M. A. Alam, J. Bude, and A. Ghetti, "Field acceleration for oxide breakdown-can an accurate anode hole injection model resolve the E vs. 1/E controversy?," in *2000 IEEE International Reliability Physics Symposium Proceedings. 38th Annual (Cat. No.00CH37059)*, Apr. 2000, pp. 21–26. doi: 10.1109/RELPHY.2000.843886.

[39] P. E. Nicollian, W. R. Hunter, and J. C. Hu, "Experimental evidence for voltage driven breakdown models in ultrathin gate oxides," in *2000 IEEE International Reliability Physics Symposium Proceedings. 38th Annual (Cat. No.00CH37059)*, Apr. 2000, pp. 7–15. doi: 10.1109/RELPHY.2000.843884.

[40] R. C. J. Wang *et al.*, "Electrical conduction and TDDB reliability characterization for low-k SiCO dielectric in Cu interconnects," *Thin Solid Films*, vol. 517, no. 3, pp. 1230–1233, Dec. 2008, doi: 10.1016/j.tsf.2008.06.051.

[41] M. Arabi *et al.*, "New Insights on Device Level TDDB at GHz Speed in Advanced CMOS Nodes," *IEEE Transactions on Device and Materials Reliability*, vol. 19, no. 2, pp. 255–261, Jun. 2019, doi: 10.1109/TDMR.2019.2914362.

[42] M. Arabi, M. Rafik, X. Federspiel, and G. Ghibaudo, "A New Direct Measurement Method of Time Dependent Dielectric Breakdown at High Frequency", in *IEEE Electron Device Letters*, vol.41, no. 10, pp-1460-1463, Oct. 2020.

[43] A. Bezza, M. Rafik, D. Roy, X. Federspiel, P. Mora, and G. Ghibaudo, "Frequency dependence of TDDB & PBTI with OTF monitoring methodology in high-k/metal gate stacks," in *2014 IEEE International Reliability Physics Symposium*, Jun. 2014, p. GD.6.1-GD.6.4. doi: 10.1109/IRPS.2014.6861149.

[44] S. Knebel *et al.*, “Influence of Frequency Dependent Time to Breakdown on High-K/Metal Gate Reliability,” *IEEE Transactions on Electron Devices*, vol. 60, no. 7, pp. 2368–2371, Jul. 2013, doi: 10.1109/TED.2013.2264104.

[45] K. T. Lee *et al.*, “Frequency dependent TDDB behaviors and its reliability qualification in 32nm high-k/metal gate CMOSFETs”, in *2011 IEEE International Reliability Physics Symposium (IRPS)*, 2011, @A.3.1-2A.3.5 .

[46] M. Rafik, A. P. Nguyen, X. Garros, M. Arabi, X. Federspiel, and C. Diouf, “AC TDDB extensive study for an enlargement of its impact and benefit on circuit lifetime assessment,” in *2018 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2018, p. 4A.3–1. doi: 10.1109/IRPS.2018.8353576.

[47] J. W. McPherson, “Physical model for the frequency dependence of time-dependent dielectric breakdown (TDDB),” *AIP Advances*, vol. 13, no. 5, p. 055217, May 2023, doi: 10.1063/5.0150268.

[48] R. Ranjan, Y. Liu, T. Nigam, A. Kerber, and B. Parameshwaran, “Impact of AC voltage stress on core NMOSFETs TDDB in FinFET and planar technologies,” in *2017 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2017, p. DG-10.1. doi: 10.1109/IRPS.2017.7936367.

[49] M. Arabi *et al.*, “Frequency dependant gate oxide TDDB model,” in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, pp. P25-1. doi: 10.1109/IRPS48227.2022.9764503.

[50] M. Arabi, “Fiabilité des diélectriques des dispositifs CMOS pour les applications automobiles : caractérisation et modélisation de l’effet fréquentiel sur le claquage diélectrique,” Université Grenoble Alpes, 2021.

[51] E. Wu, E. Nowak, and W. Lai, “Off-state mode TDDB reliability for ultra-thin gate oxides: New methodology and the impact of oxide thickness scaling”, in *2004 IEEE International Reliability Physics Symposium (IRPS), April 2004, pp.84-94*.

[52] T. Garba-Seybou, X. Federspiel, A. Bravaix, and F. Cacho, “New Modelling Off-state TDDB for 130nm to 28nm CMOS nodes,” in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, p. 11A.3–1.

[53] I. K. Chen *et al.*, “The physical mechanism investigation of off-state drain bias TDDB and its implication in advance HK/MG FinFETs” in *2018 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2018, pp.4A.2-4A.2-6.

[54] T. Garba-Seybou *et al.*, “Location of Oxide Breakdown Events under Off-state TDDB in 28nm N-MOSFETs dedicated to RF applications,” in *2023 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2023, pp. 1–8. doi: 10.1109/IRPS48203.2023.10117725.

[55] A. Divay *et al.*, “65nm RFSOI Power Amplifier Transistor Ageing at mm W frequencies, 14 GHz and 28 GHz,” in *2021 IEEE International Electron Devices Meeting (IEDM)*, 2021, p. 39.3.1-39.3.4. doi: 10.1109/IEDM19574.2021.9720531.

[56] A. Rathi, A. Dixit, P. Srinivasan, O. H. Gonzalez, and F. Guarin, “RF Reliability of CMOS-Based Power Amplifier Cell for 5G mmWave Applications,” in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, p. 4B.3–1. doi: 10.1109/IRPS48227.2022.9764465.

[57] X. Garros *et al.*, “A Very Robust and Reliable 2.7GHz +31dBm Si RFSOI Transistor for Power Amplifier Solutions,” in *2019 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2019, p. 25.5.1-25.5.4. doi: 10.1109/IEDM19573.2019.8993649.

[58] P. Srinivasan, P. Colestock, T. Samuels, S. Moss, F. Guarin, and B. Min, “A novel methodology to evaluate RF reliability for SOI CMOS-based Power Amplifier mmWave applications,” in *2020 IEEE International Reliability Physics Symposium (IRPS)*, May 2020, pp. 1–4. doi: 10.1109/IRPS45951.2020.9129588.

[59] A. Rathi, P. Srinivasan, F. Guarin, and A. Dixit, “Large Signal RF Reliability of 45-nm RFSOI Power Amplifier Cell for Wi-Fi6 Applications,” in *2021 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2021, pp. 1–6. doi: 10.1109/IRPS46558.2021.9405158.

[60] P. Asbeck, S. Alluri, N. Rostomyan, and J. A. Jayamon, “Reliability of CMOS-SOI power amplifiers for millimeter-wave 5G: the case for pMOS (Invited),” in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, p. 4B.1–1. doi: 10.1109/IRPS48227.2022.9764417.

[61] X. Aragones *et al.*, “Aging in CMOS RF Linear Power Amplifiers: An Experimental Study,” *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES*, vol. 69, no. 2, 2021.

[62] T. Garba-Seybou, A. Bravaix, X. Federspiel, and F. Cacho, “Modeling hot carrier damage interaction between on and off modes for 28 nm AC RF applications,” *Microelectronics Reliability*, vol. 126, p. 114342, Nov. 2021, doi: 10.1016/j.microrel.2021.114342.

[63] A. Lange, “A general approach for degradation modeling to enable a widespread use of aging simulations in IC design,” *Microelectronics Reliability*, 2022.

[64] P. M. Lee, “Compact modeling for simulation of circuit reliability: Historical and industrial perspectives,” in *2013 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2013, p. 2A.1.1-2A.1.6. doi: 10.1109/IRPS.2013.6531941.

2. RF HCI reliability modeling methodology for RF/mmW PA at 28GHz

Power amplifiers are highly vulnerable to hot-carrier stress, as they are subjected to large drain voltage swings to achieve high gain and power added efficiency (PAE), which affects the device's RF performance after long-term stress. To meet PA reliability requirements, RF designers rely on aging models provided by the foundry's process design kit (PDK) to evaluate performance to reliability trade-off in CAD simulations. Most of the published research works concerning RF HCI reliability for PA applications are focused on RF load pull stress measurement methodology [1], [2], [3], [4], [5] to show correlation between RF and DC figure-of-merit (FOM) degradation. Meanwhile, the importance of aging models in PA device lifetime predictions using SPICE simulations have been demonstrated in [6], [7], [8].

In this chapter, the RF PA reliability evaluation methodology is demonstrated from DC to RF large-signal accelerated hot carrier stress in different PA architectures. The interest of this methodology is to establish a relationship between time-zero (T_0) mission profiles and RF hot-carrier injection (HCI) degradation rate. As this approach depends on the accuracy of PA device T_0 mission profile and aging models, it is imperative that to ensure model-to-hardware correlation (MHC) of the T0 and aging models. An in-depth analysis of RF HCI sensitivity via CAD simulations can then be investigated through various modeling factors which impact the accuracy of RF degradation lifetime estimation.

2.1 Time-zero (T_0) characterization of RF PA performance at 28GHz

Fresh device characterization is the first step to define the RF PA performance. This step is also known as T_0 characterization in the reliability field. In this section, the different PA structures are characterized at a given DC operating point and targeted output power using a load pull measurement setup. Then, the PA device model is optimized to validate MHC to extract accurate time-domain waveforms from RF simulations as T_0 mission profiles.

2.1.1 Description of RF PA test structures

Three different PA cells known as standalone, stacked and interstacked PA, used to investigate the RF HCI degradation at 28GHz are illustrated in Figure 2-1 :(a) Standalone, (b) Stacked and (c) Interstacked PA for HCI RF reliability studies at 28 GHz. These PA devices are designed with NMOS GO1 body-contacted transistors from STMicroelectronics 65nm partially-depleted SOI (PDSOI) process. The transistor width is W=400µm and gate length is L =65nm. The standalone PA consists of a common-source topology, usually implemented as a driver stage in multistage PA due to high linearity requrements. The stacked and interstacked PA consisting of acascode structure CS-CG, which presents a higher output power handling by sharing the output voltage swing between the top and bottom transistors

[9]. To equalize V_{DS} voltage excursions across each transistor, an integrated inductance-capacitance (LC) circuit is inserted between the top and bottom transistors. These devices are connected by back-end routing to GSGSG test pads for on-wafer RF characterization and stress measurements, providing direct access to DUT terminals important for reliability study. The sense terminal is added to compensate the voltage drop between the probe contact and routing to the drain terminal when the load current is high. In order to obtain accurate device degradation, it is also used to monitor the probe contact resistance during the stress measurements.

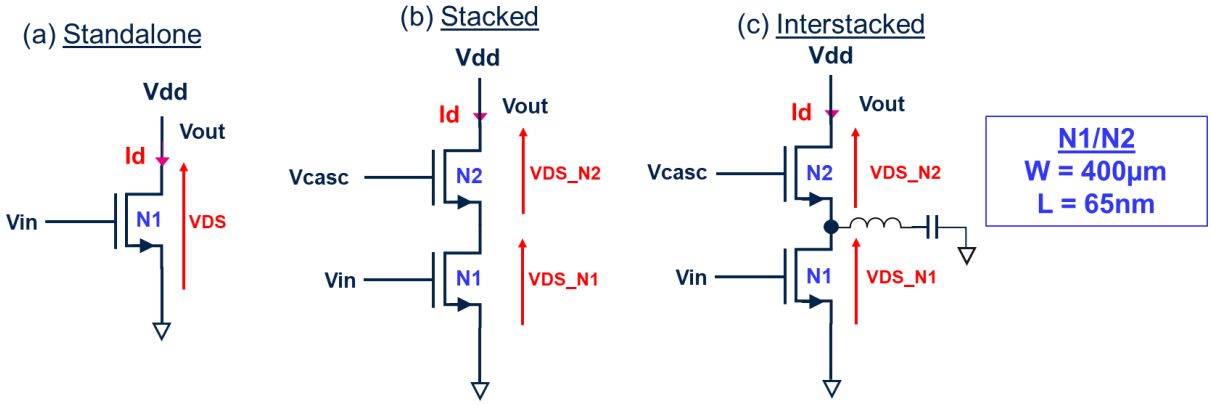

Figure 2-1 :(a) Standalone, (b) Stacked and (c) Interstacked PA for HCI RF reliability studies at 28 GHz.

2.1.2 Load pull measurement setup

On-wafer measurements are crucial for the development of RF devices. Indeed, the access to actual device performance is essential to achieve accurate modeling. The RF power performance of a PA at a given frequency is determined by the load impedance presented at the PA output (link to chapter 1 PA basics). In a load pull measurement setup, the variation of the load impedance tuner to determine the optimal performance (efficiency/linearity) can be controlled and measured precisely using a power sensor at the PA output. q shows the scalar load pull setup used in this work, calibrated for measurement frequencies ranging from 10GHz to 40GHz. The functionalities of the different apparatus of the setup are described in the following:

- **RF generator** provides input RF power at fundamental frequency 28GHz in continuous wave (CW) mode, amplified by a driver amplifier.
- **Directional coupler** used as a sampler for the injected input power.
- **Isolator** prevents power reflection towards RF generator in case of large impedance mismatch or high input reflection (Γ).
- DC voltage supply and current sensing by **semiconductor device analyzer (Keysight B1500)**, also used for DC characterization.
- **Bias Tee** used to combine the DC bias and the RF signal.
- **Power sensors** are used to read RF input and output power measurements.
- External **impedance tuners** (fundamental DELTA tuners from Focus Microwaves) with direct connection to the probes, ensuring low insertion losses i.e. reflection

coefficient Γ_{max}=0.8 at 28GHz. This enables an optimal tuning range of both source and load impedances for each PA.

- **RF infinity probes** to minimize insertion loss between test pads and tuners during device measurements.
- **Vector Network Analyzer (VNA)** for tuners calibration and S-parameter measurements (not shown in Figure 2-2).

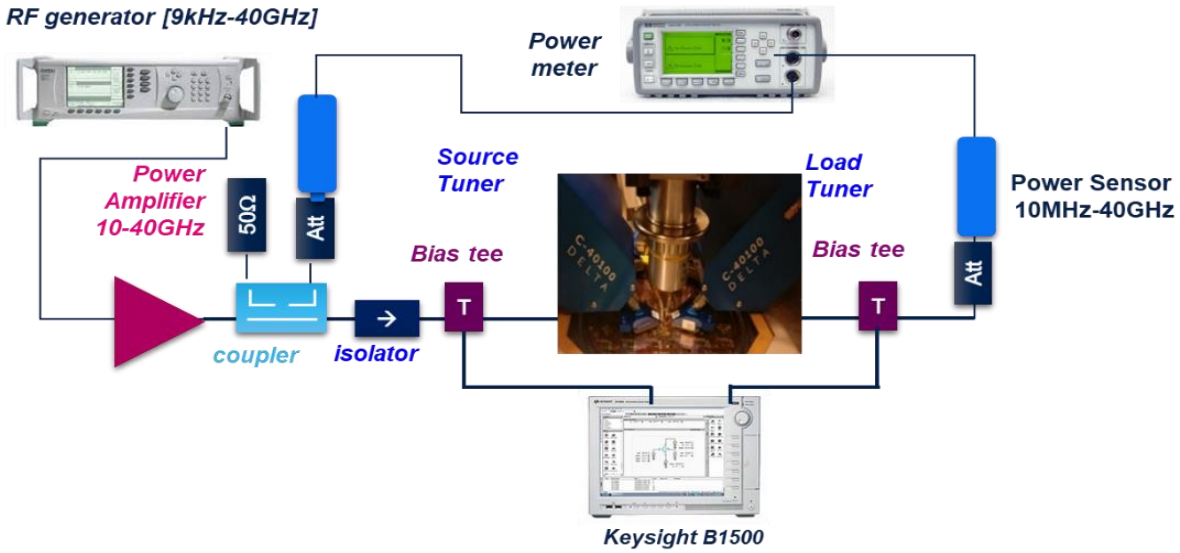

Figure 2-2 ; Load pull measurement setup used for RF characterization and aging measurements in this work. Source [2]

For this study, characterization & aging measurements for both DC and 28GHz have been performed on this load pull setup to optimize T0 and aging MHC that will be discussed in the following sections 2.1.4 and 2.2.1 respectively.

2.1.3 DC and large-signal RF on-wafer characterization of different PA structures

First, DC characterization is performed on the standalone PA to determine the bias conditions in class AB operation. Figure 2-3 shows the Id-Vg and Id-Vd measurements for different Vds and Vgs bias voltages respectively. The drain current for class AB operation is Id=10mA, for a gate voltage bias Vgs = 0.43V and drain voltage Vds = 1.3V. To achieve the desired saturated output power Psat=P_{1dB} around 15dBm and 16dBm for this DC bias point, the optimized source and load impedances ZSopt and ZLopt at 28GHz, are determined using the load pull technique [2]. The measured RF performance at 28GHz is presented in Figure 2-4. The linear gain of the standalone PA is 6.5dB and a maximum PAE of 41.32%, while the Psat is measured at 15.7dBm. Stacked and interstacked PA structures exhibit higher linear gain of 7.8dB and 8.4dB respectively thanks to the reduced parasitic capacitance Cgd resulting in a better gm [9]. The maximum PAE of both cascode PAs are 5%-10% lower than that of the standalone PA which can be explained by the output voltage swing misalignment due to the presence of device parasitics of the transistors in the stack [10]. From a RF FOM perspective, we can summarize that for a constant P_{sat}, the standalone PA offers the maximum PAE while the interstacked PA offers the highest gain. However, reliability requirements for the targeted PA operation lifetime needs to be considered as the HCI degradation is strongly accelerated

by Vds and Vgs. The RF FOM degradation of the different PA structures under RF HCI stress will be discussed in section 2.2.2.

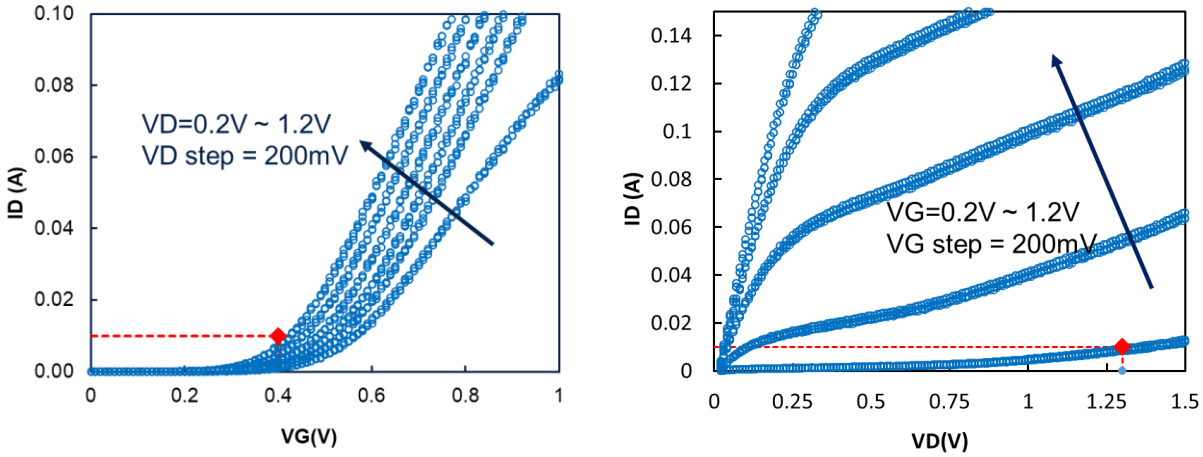

Figure 2-3: Id-Vg (left) and Id-Vd (right) characteristics of standalone PA (body-contacted NMOS GO1 W=400µm L=65nm). DC bias point for Class AB operation (I_D=10mA and V_D=1.3V) is shown by the red marker.

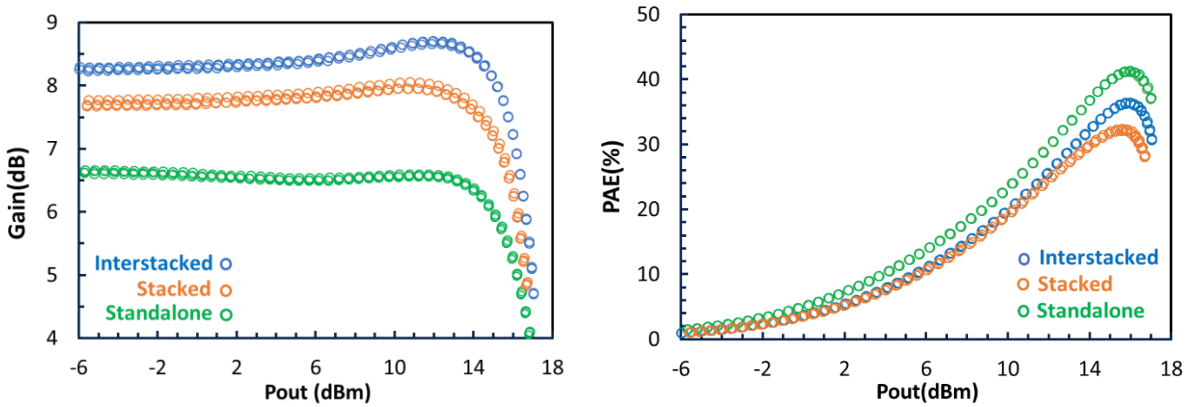

Figure 2-4 : RF Gain (left) and Power Added Efficiency (right) as a function of Pout extracted from large-signal RF measurements of standalone, stacked and interstacked PA.

2.1.4 Device Model-to-Hardware Correlation (MHC)

The development of MOSFET models is essential to enable automation of SPICE simulations from device to circuit and system level. The model must be able to accurately capture the core MOSFET operation physics as well as device-related behavior (i.e., short channel effects, current saturation effects, quantum-mechanical effects, etc.) [11]. Among the different types of compact models, the Berkeley short IGFET model (BSIM), which is a threshold voltage-based model, was implemented in the SPICE simulations of this section. This model was extended from the original BSIM model to incorporate PD and FD SOI device behavior [12].

2.1.4.1 DC and AC MHC Optimization

DC behavior of the BSIM SOI model was optimized based on standalone PA T0 measurements presented in the previous section 2.1.3. The selected DC model parameters (refer to Appendix A) were tuned to fit the device model to the IdVg and IdVd measurement data in the different MOSFET operation modes, from subthreshold to saturation regime.

Figure 2-5 shows the IV curves of the optimized DC model compared to the measurement data. It is clearly observed that the DC MHC is accurate for the subthreshold and linear regimes, however model accuracy at the saturation regime (Vgs=Vds >1V) is limited since additional Ib-Vg measurements are required to fully optimize the model's impact ionization parameters. The dynamic PA loadline is shown in Figure 2-5 to outline the time-domain voltages and currents at $P_{out}=P_{1dB}$. As these points are within the accurate range of the MHC optimization, the DC optimized model is sufficiently accurate for our reliability evaluation.

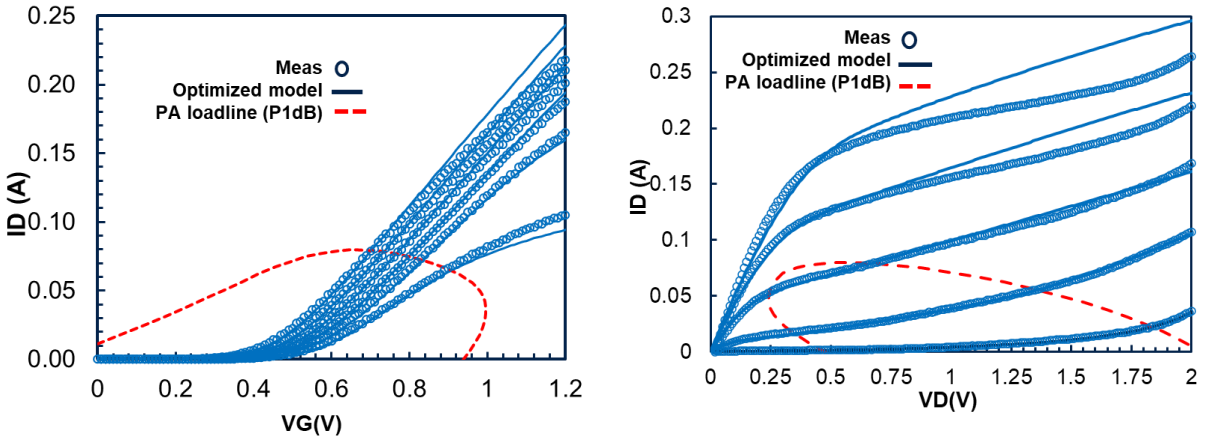

Figure 2-5 : Id-Vg (left) and Id-Vd (right) curves of optimized model compared with measurement data. PA loadline at Pout=P1dB is within the accurate range of optimized model

In terms of small-signal (AC) behavior, on-wafer S-Parameter measurements of the PA device up to 40GHz at different Vd and Vg bias conditions to verify AC MHC of the optimized model. From these measurements, the GSGSG pad de-embedding procedure is applied to remove pad parasitic effects from PA device measurements. This enables the extraction of the device's parasitic capacitances at a given DC bias point using the MOSFET small-signal equivalent circuit (SSEC). A detailed explanation of the capacitance extraction scheme is described can be found in [16]. The parasitic capacitances, i.e. gate-to-drain (Cgd) and gate-to-source (Cgs) capacitances, are composed of overlap capacitances (between gate oxide and the drain and source extensions) and fringing field capacitances, whereas the parasitic drain-to-source capacitance (Cds) represents the coupling between the source and drain terminals through the buried oxide and substrate [13]. The total capacitance seen by the gate (Cgg) is the sum of Cgs and Cgd.

Figure 2-6 compares the parasitic capacitance of the measured and optimized model as a function of frequency. We observe that the discrepancy between simulation and measurement data at 28GHz is less than 50fF which is within acceptable range.

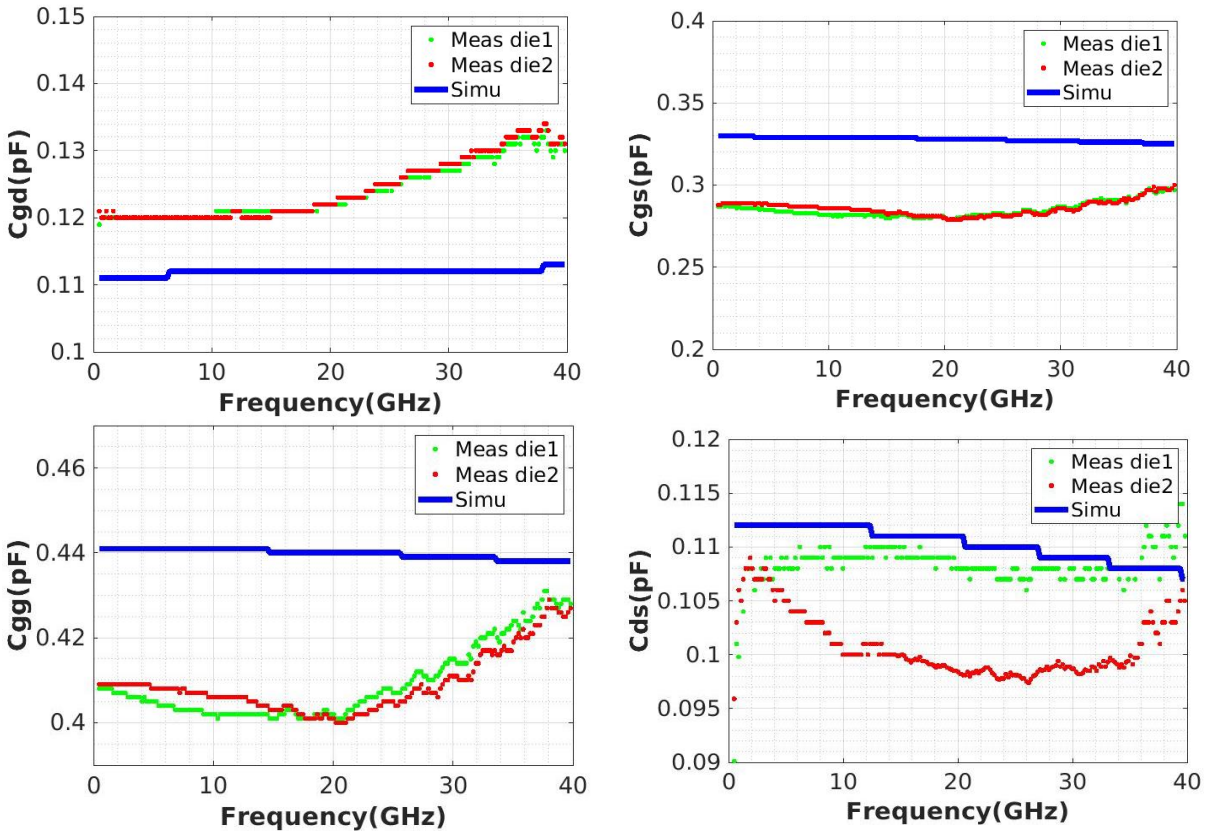

Figure 2-6 : Parasitic capacitances Cgd, Cgs, Cgg, Cds extracted from de-embedded S-Parameter measurements at DC bias operating point are compared to optimized device model data.

2.1.4.2 28GHz Large-signal MHC validation

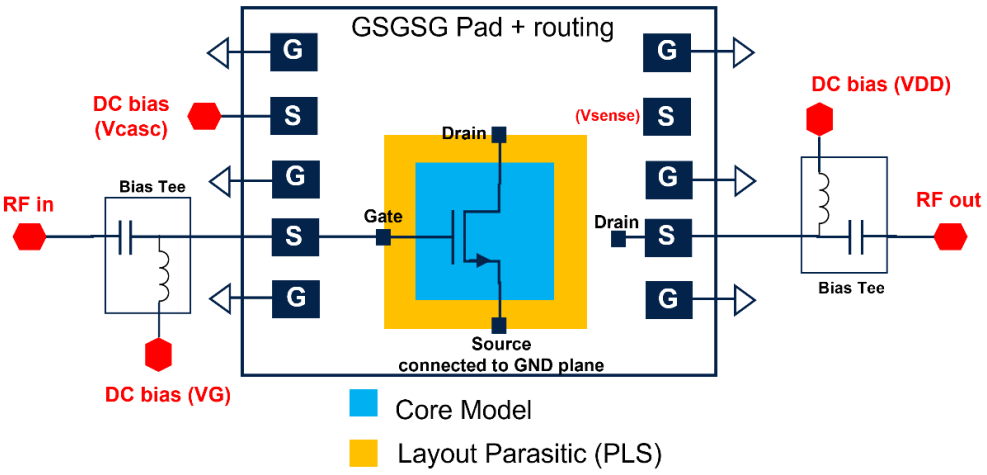

Figure 2-7 : 28GHz RF PA simulation test bench

The SPICE simulation testbench implemented in Cadence SpectreRF simulator for the different PA structures is shown in the schematic of Figure 2-7. To reflect RF measurement environment, different parasitic elements on the RF path need to be considered in the simulation. The post-layout extraction of the PA is added on top of the intrinsic optimized BSIM core model to include the layout parasitic effects and connections to back-end of line (BEOL) metallization. GSGSG pad and access lines are modeled with S-parameter data obtained via electromagnetic simulations using Momentum Virtuoso. At the RF input and

output ports, the LC network is used to model bias tee function. The optimal impedances ZS_{opt} and ZL_{opt} are defined in the input and output port setup.

Then, the RF simulation results of the different PA structures are compared with measurement data to validate the large-signal MHC at 28GHz. In Figure 2-8, The gain of the standalone PA with optimized model in the linear operation shows excellent correlation to the measured gain. When the gain approaches the PA compression, near P1dB, the optimized model data deviates from measurement data. At this compression region, the drain current is no longer a linear function of the transconductance gm and Vgs, but rather a non-linear gm function consisting of non-linearity coefficients of the higher-order gm derivatives [14], [15]. This requires the fitting of the small-signal model parameters in the range of gate and drain voltages covering different RF operating regions of the PA, which is defined by the mission profile. The mission profile of the standalone PA is plotted in Figure 2-8 by extracting the instantaneous voltages Vds(t) and Vgs(t) at Pout=P1dB from transient simulations using the same testbench. The maximum Vds of the original PDK model is higher than the optimized model at $Vgs \geq V_T$. As observed in Figure 2-9, the optimized model simulated in the stacked and interstacked PA configuration is accurate in both linear and non-linear PA operation compared to the measurement data. Likewise, their mission profiles are extracted as shown in Figure 2-9 with bottom (N1) and top (N2) transistors respectively. It is noted that the top transistor of both cascode PAs is subjected to higher V_{DS} excursions compared to the bottom transistor, which may cause them to be more vulnerable to HCI degradation.

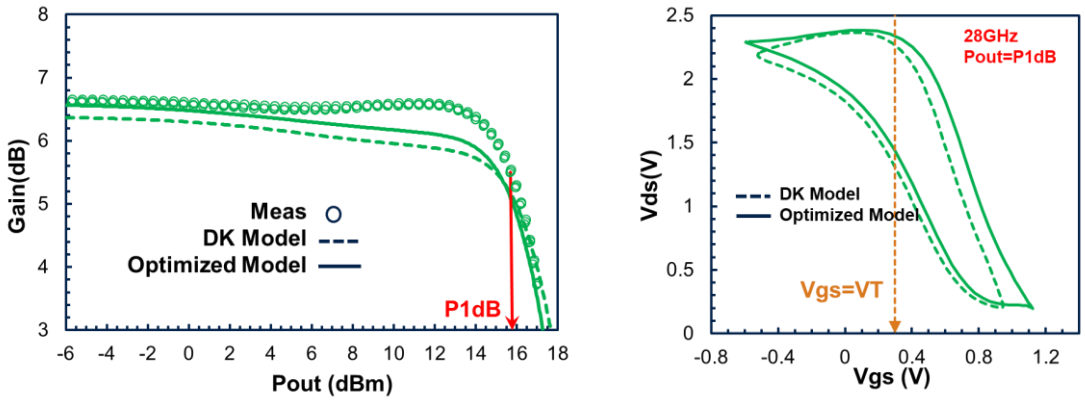

Figure 2-8 : (left) 28GHz Standalone PA T0 RF gain MHC before and after device model optimization. (right) Time-domain waveforms Vds(t) and Vgs(t) are extracted from 28GHz transient simulations at Pout=P1dB.

The DC and AC MHC optimization efforts have improved RF large-signal MHC to extract accurate time-domain waveforms or mission profiles in SPICE simulations. As HCI degradation has strong dependence on Vg and Vd, inaccurate T_0 mission profile would result in under- or over-estimation of device lifetime extrapolation. In the subsequent section, the optimized T_0 model for PA device is implemented in RF aging simulation flow to address RF PA HCI reliability at 28GHz.

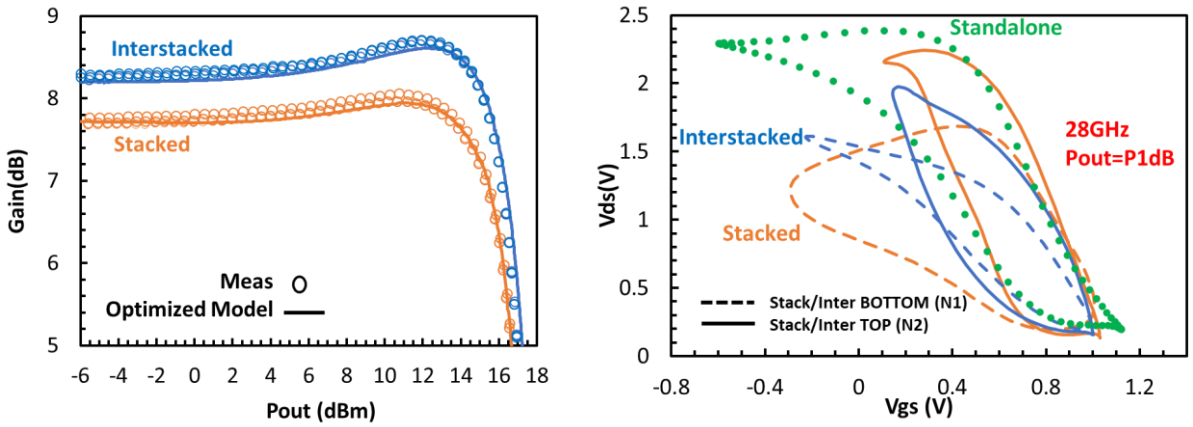

Figure 2-9 : (left) 28GHz Stacked and interstacked PA T_0 RF gain MHC. (right) Time-domain waveforms of bottom (N1) and top (N2) transistor of cascode configuration extracted from 28GHz transient simulations at Pout=P1dB.

2.2 RF PA HCI reliability at 28GHz

As mentioned previously in 1.3.1.1A, quasi-static approximations are typically applied for DC to RF degradation modeling in MOSFETs via the AGE function [16]. Therefore, two pre-requisites are necessary to perform this study: Firstly, an accurate DC HCI age model is calibrated based on DC stress measurements, and secondly, the validity of quasi-static approximations at the studied frequency of 28GHz. The latter is assumed to be valid based on the work of [8], reporting quasi-static validity up to 60GHz. We use RF PA stress measurements to confirm our RF degradation modeling approach via aging simulations. We also propose an RF HCI reliability evaluation method based on the different PA mission profiles discussed in section 2.1.4.2.

2.2.1 DC HCI age model calibration

DC stress measurements were conducted on the standalone PA device under HCI stress conditions with consideration to the standalone PA mission profile. DC stresses were interrupted periodically to perform IV measurements to monitor parametric degradation, i.e, ΔV_{Tlin}, ΔV_{Tsat}, ΔI_{dlin}, ΔI_{dsat}, against stress time as presented in Figure 2-10. Here, we are focused on-state hot-carrier stress data due to its higher sensitivity to parametric degradation, as opposed to off-state hot-carrier stress [17], [18]. Measured parametric degradation ΔV_T and ΔId follows a time power law dependence (Eq.2-1), with time exponent n=0.53, which is in the range of values typically found in the case of hot-carrier damage induced by creation of interface states (n=0.5-0.6) [19].

$$\Delta D = \alpha * t^n \qquad \text{(Eq.2-1)}$$

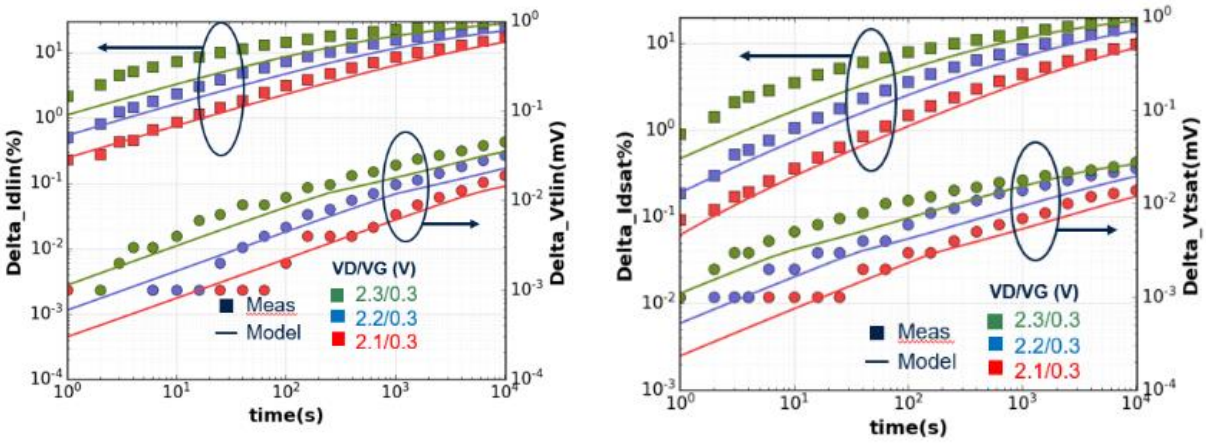

Figure 2-10 : Comparison of calibrated model and experimental DC parameter drift for DC hot-carrier stress at V_D=[2.1V;2.3V] and V_G=0.3V

Our age model is based on the energy-driven HCI model proposed by [20], taking into account the contribution from different carrier energy modes to accurately capture HCI degradation across various V_G/V_D biasing regimes. The parametric degradation ΔD is modeled by carrier energy and carrier density components, $(V_D - V_{Dsat})$ and $(V_G - V_T)^p$ respectively as described in Eq.2-2. A is a technology-dependent parameter.

$$\Delta D = A * t^n * e^{B(V_D - V_{Dsat})} * (V_G - V_T)^p \qquad \text{(Eq.2-2)}$$

After calibration, this DC age model shows good correlation with the measured DC parameter drift (refer to Figure 2-10), specifically at elevated V_D=[2.1V;2.3V] and V_G=0.3V, corresponding to peak V_{DS} swings of standalone PA. We note that ΔI_{dlin} and ΔI_{dsat} are more than 10% for V_D=2.3V after 10000s of stress time. ΔI_{dlin} and ΔV_{Tlin} are also observed to be higher than ΔV_{Tsat} and ΔI_{dsat}, considering that ΔI_{dlin} and ΔV_{Tlin} are more affected by the localization of defects due to HCI in the gate-oxide [21].

2.2.1.1 Mission-profile based HCI reliability evaluation of different PA architectures.

The AGE function (eq.2-3), introduced previously in Chapter 1, computes the total parametric degradation as the sum of the instantaneous age rate for a given stress duration and time-varying bias voltages or current of the RF waveform. The age rate can thus be solved by constant-bias conditions without time dependence [22]. In our reliability evaluation, eq.2-2 is implemented into eq.2-4 to obtain HCI age rate generated from our DC age model.

$$AGE = \int_t^{Tage} A^{1/n}(t)dt \qquad \text{(Eq.2-3)}$$

$$AGE\ rate = A^{1/n}(t) \propto \left[e^{B(V_D(t) - V_{Dsat})} * (V_G(t) - V_T)^p\right]^{1/n} \qquad \text{(Eq.2 -4)}$$

The 2D surface plot of HCI age rate estimated using the calibrated DC age model is shown in Figure 2-11. This plot shows the influence of V_G and V_D on the HCI degradation, where the age rate is maximum for $V_{GS} \geq V_T$ and $V_{DS} \geq 1.6V$. The distance between two contours (on the color scale), indicates the magnitude of the slope. The smaller the distance, the steeper the slope, the higher the HCI age rate. On the V_{DS} axis, the distance between two contours is

smaller by several orders of magnitude than that observed on the V_{GS} axis. This means that the age rate is strongly dependent on V_G than V_D. The profile mission of each PA are combined with the surface plot in Figure 2-11 using the V_G and V_D pairs of values within a period of $V_{GS}(t)$ and $V_{DS}(t)$ extracted waveforms from the transient simulations in section 2.1.4.2. Compared to the other PA structures, the standalone PA has the highest V_{DS} peak. By referring to the probability distribution of $V_{DS}(t)$ in one wave period of each PA structure in Figure 2-12, the highest occurrence of maximum V_{DS} is observed at V_{DS} ≈2.4V for the standalone PA, V_{DS} ≈2.3V for the stacked PA and V_{DS} ≈2V for the interstacked PA. In Figure 2-11, these occurrences are located at minimum V_{GS} and V_{DS} on the PA mission profiles. Although these pairs of V_{GS} and V_{DS} values do not fall in the range of the maximum age rate as illustrated in Figure 2-11, the total HCI degradation is still significant when integrated over total stress time due to their higher density occurrence within one wave period. Compared to the other PA structures, the interstacked PA has the smallest V_{DS} peak. Thus we can deduce that the interstacked PA suffers from the least HCI degradation compared to standalone and stacked PA due to its lower V_{DS} acceleration.

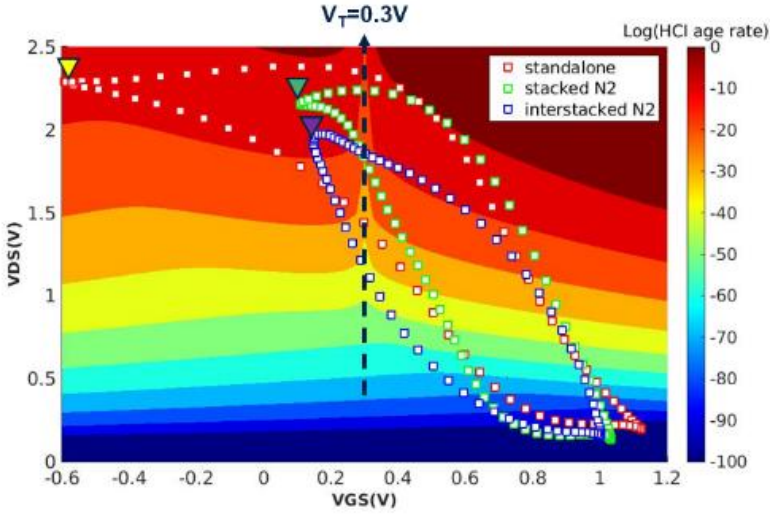

Figure 2-11 : Mission profiles of PAs with reference to HCI age rate which is strongly dependent on V_{DS} than V_{GS} . Critical aging rate occurs at V_{GS}>V_T and maximal V_{DS} on the 2D surface plot.

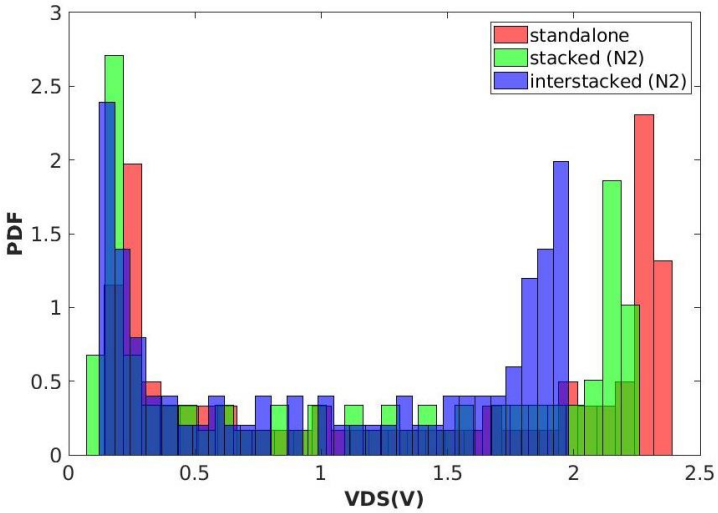

Figure 2-12 : Histogram showing probability distribution of VDS(t) in one period T=1/F. Highest occurrence of maximum V_{DS} ≈2.4V for standalone PA which corresponds to minimal V_{GS} and maximal V_{DS} on the mission profile in Figure 2-11.

2.2.2 Large-signal RF HCI stress

2.2.2.1 RF stress measurements

The large-signal RF stress conditions for each PA are presented in Table 2-1. The stress power level is fixed at $P_{out}=P_{1dB}$ as a compromise between high stress power level and gain compression. Due to the non-linear behavior in gain compression, signal distortion appears in time-domain voltage waveform which makes the waveform extraction challenging [23]. RF stress measurements were conducted in continuous wave (CW) mode at 28GHz for 9 hours (=32400s) to maintain probe contact stability within a reasonable stress duration at room temperature. The stress methodology based on quasi-static approximations is illustrated in Figure 2-13. Prior to the stress sequence at T_0, the fresh PA DC and large-signal RF characterization is recorded. Then, the stress sequence is launched with the corresponding DC bias and RF stress conditions. The stress sequence is interrupted periodically for I_D-V_G measurement (linear and saturation curves) and RF power measurements at P_{1dB} to monitor DC and RF degradation. At the end of the stress duration, another DC and RF characterization is done after new probe contact for contact resistance drift verification purposes. The results of the stress measurements will be discussed in section 2.2.2.2 with comparison to RF aging simulation results.

Table 2-1 : HCI stress conditions for large-signal RF stress measurements at 28GHz

PA	Vdd (V)	Id (mA)	Pin (dBm) @P1dB	Pout (dBm) @P1dB	ZSopt	ZLopt	Duration (s)	Temp (°C)
Standalone	1.3	10	9.3	15.7	5.72-j4.73	11.01+j7.52	32400	25
Stack	2	10	8.5	15.5	5.72-j4.73	18+j20.67	32400	25
Interstack	2	10	8.5	15.5	5.75-j2.93	18+j16.65	32400	25

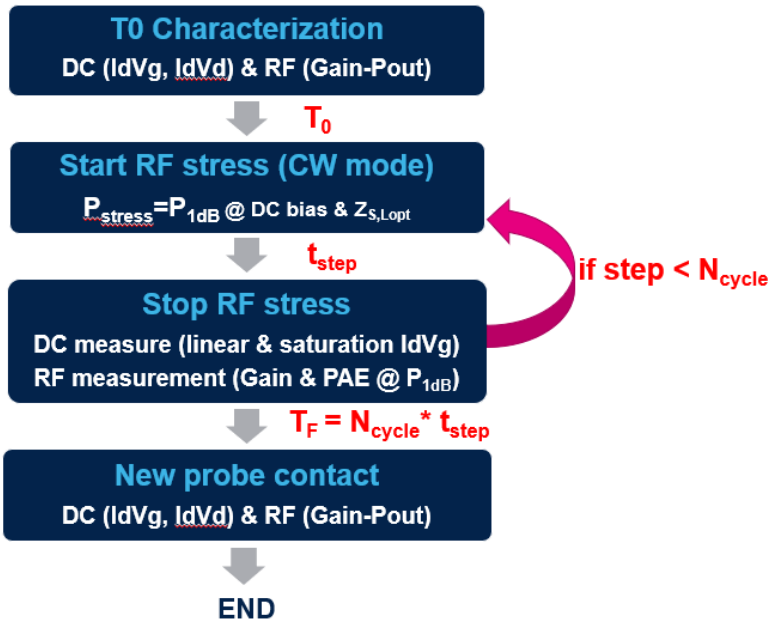

Figure 2-13 : RF stress methodology based on quasi-static approximations.

2.2.2.2 RF aging simulations

Aging models in SPICE reliability simulations can be implemented with two different approaches, either using physical approach where the aging model modifies the intrinsic transistor model, i.e. BSIM model, parameters based on physical effects or the empirical approach where the aging model is built using current or voltage-controlled sources without modifying the intrinsic transistor model parameters [24].

In this study, the calibrated DC age model takes the physical approach and is encoded in form of an aging model card. This aging model card is embedded into the Virtuoso Unified Reliability Interface (URI) that implements the aging-law equations and updates BSIM fresh model parameters following degradation under the applied stress conditions. The RF aging simulation flow performed using Cadence SPECTRE is presented in Figure 2-14. The flow consists of 3 simulation stages that are explained as follows:

- Fresh simulation: DC and RF simulations to determine T_0 device performance such as Id-Vg (linear and saturation) and Gain-Pout curves.
- Stress simulation: This simulation is performed in transient simulation mode at the corresponding stress condition, i.e. P_{1dB}. The URI computes the age rate based on the stress voltages or current for each simulation time-step, t_{step} << T=1/F. The total degradation at the end of transient simulation is computed based on the quasi-static approximation of the AGE function. BSIM model parameters are updated to register device degradation.
- Aged simulation: The lifetime extrapolation of the aged device is computed using the updated BSIM model parameters. DC and RF post-aging simulation are performed to extract degraded FOM such as ΔV_T, ΔI_D, ΔP_{OUT}, ΔGain.

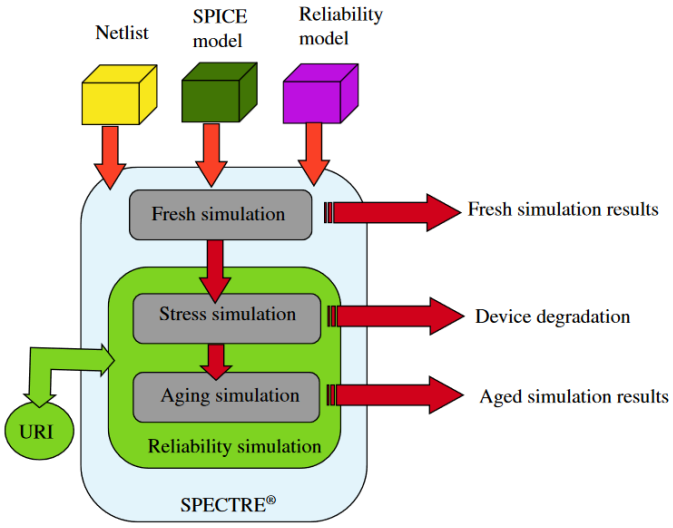

Figure 2-14 : SPECTRE Reliability simulation flow chart [25]

To predict the degraded device RF large-signal performance at 28GHz, stress and aging simulations are executed using the same stress conditions defined in Table 2.1. The aging simulation results for the standalone, stacked and interstacked PA are compared with the

stress measurements, shown in Figure 2-15. The standalone PA shows higher degradation in linear gain (8.4%) as opposed to gain compression P_{1dB} (6%). This difference in degradation behavior is attributed to the dynamic current drive level for different P_{out}. At lower P_{out} (linear gain), the current drive level is low and thus degradation is sensitive to the increase of ΔV_T. At higher P_{out} (compression), the current drive level is higher and is impacted by ΔR_{on} which decreases output voltage swing. This modifies the bias operating point which could lead to the change of PA class from class AB to B [26].

In comparison to the stacked and interstacked PA, it is revealed that the RF gain degradation is the highest in the standalone PA (0.47dB) while almost none is observed in the interstacked PA (0.01dB). This observation is in good agreement with our proposed mission profile-based reliability evaluation (refer to section 2.2.1.1). From a RF reliability modeling perspective, our DC to RF modeling approach can reproduce the RF degradations at 28GHz of stress measurements after 9 hours. The RF aging simulation results confirm that both accurate DC aging models and T_0 mission profiles are fundamental to achieve accurate RF performance degradation modeling in PAs. Further investigation on this subject is presented in the RF HCI sensitivity analysis in the next section.

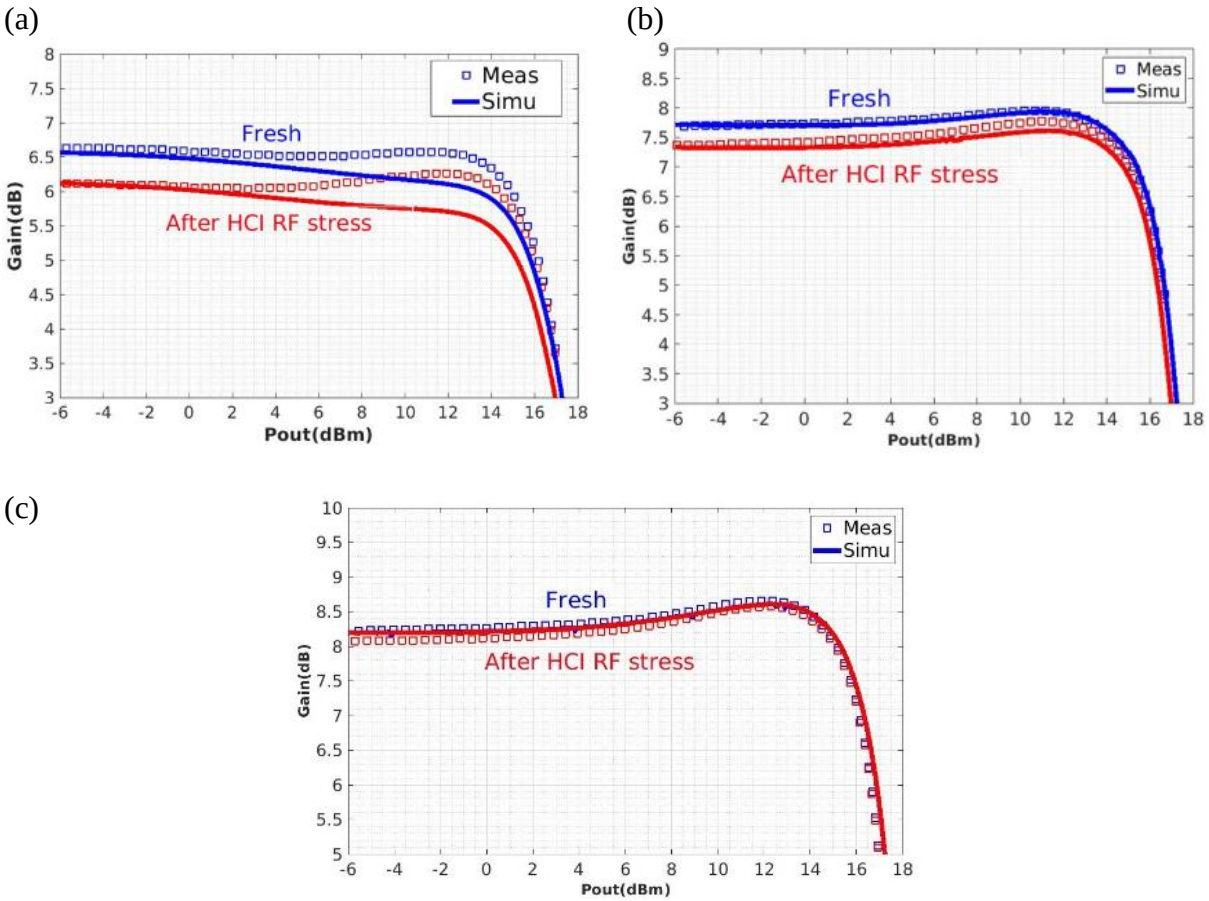

Figure 2-15 : (a) Standalone, (b) Stacked and (c) Interstacked PA fresh and post RF stress performance.

2.3 RF Hot carrier reliability sensitivity analysis

We have demonstrated that our HCI age model and reliability simulation approach provides accurate RF degradation predictions for PA applications. Next, we apply the same methodology to conduct an RF HCI sensitivity analysis using an empirical approach by identifying the different T_0 and age model parameters that affect the accuracy of RF HCI reliability predictions. In the following, the standalone PA fresh and aging simulation results represent the reference model as they demonstrate good alignment with experimental data.

2.3.1 Impact of SPICE model parameter degradation on RF PA degradation

A Pareto analysis is generally used to assess and identify the relation between outputs and inputs within a complex problem consisting of various parameters. We have applied the Pareto analysis to evaluate the contribution of input DC and AC SPICE model parameter drift on the output RF gain degradation modeling. These model parameters are chosen based on the drift of MOSFET device electrical parameters observed during RF HCI stress measurements which have been reported in the literature [1], [3], [27]. As discussed in section 1.3.1.1, the following DC SPICE model parameters are chosen: threshold voltage in linear regime (V_{Tlin}), carrier mobility (μ_0), drain resistance (Rd). For AC SPICE model parameter, the gate-to-drain capacitance (Cgd) representing the extrinsic (fringing and overlap) parasitic capacitance of the MOSFET is chosen due to its impact on small-signal behavior in RF devices. In addition, previous investigation concerning the impact of hot-carrier induced interface-states in [27] has pointed out that this extrinsic Cgd degradation can be correlated with the variation of local flat-band voltage at the poly/LDD overlap region and the increase of Rd.

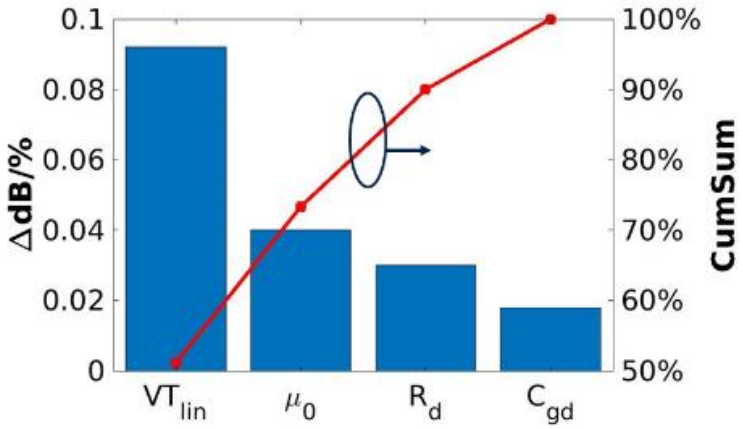

Figure 2-16 : Pareto chart illustrating contribution of different device parameters drift (%) on RF gain degradation (ΔdB).

In our analysis, the degradation level of these model parameters was varied linearly and independently of each other, i.e. variation between 3% to 10% for each input parameter to obtain acceptable RF gain degradation range (0.5dB to 1dB) in the context of linear PA class operation. The RF gain drift (ΔdB), obtained using RF aging simulation flow in 1.2.2.2, is then normalized to the degradation level of each model parameter, given by ΔdB/%. In Figure 2-16, the Pareto chart indicates that the largest contribution of RF gain degradation comes from V_{Tlin} drift, representing almost 50% of total gain degradation. This implies that V_{Tlin} drift modeling is the most important parameter for RF HCI degradation modeling.

2.3.2 Impact of T_0 model precision on RF PA degradation.

Previously in section 2.1.4, the importance of T_0 model optimization to obtain an accurate T_0 PA device model was presented. Here, we quantify the impact of T0 MHC precision on the RF gain degradation sensitivity. Two different T_0 PA models are studied: Model A and Model B which represent higher and lower gain respectively at T_0 compared to the reference model. For each model, the RF gain error at T_0 represented by $\Delta Gain[T_0]$ and the RF gain error at Tstress represented by $\Delta Gain[T_{stress}]$ are expressed as :

$$\Delta Gain[T_0] = Gain_{Model\ A/B}[T_0] - Gain_{Model\ Ref}[T_0] \quad \text{(Eq 2-5)}$$

$$\Delta Gain[T_{stress}] = Gain_{Model\ A/B}[T_{stress}] - Gain_{Model\ Ref}[T_{stress}] \quad \text{(Eq 2-6)}$$

where $Gain_{Model\ A/B}[T_0]$ and $Gain_{Model\ Ref}[T_0]$ are RF gain of model A (or B) and reference model respectively at T_0, while $Gain_{Model\ A/B}[T_{stress}]$ and $Gain_{Model\ Ref}[T_{stress}]$ are RF gain of model A (or B) and reference model respectively at different stress time (T_{stress}). The RF gain drift at different T_{stress} is shown to be dependent on T_0 MHC precision, as observed in Figure 2-17. $\Delta Gain[T_{stress}]$ increases as T_{stress} increases for a higher T0 gain (Model A) but decreases for a lower T_0 gain (Model B). In that case, a positive $\Delta Gain[T_0]$ results in a positive error accumulation over stress time and gives a more pessimistic RF gain degradation estimation. Instead, for a negative $\Delta Gain[T_0]$ a negative error accumulation over time is obtained, providing a more optimistic estimation of RF gain degradation.

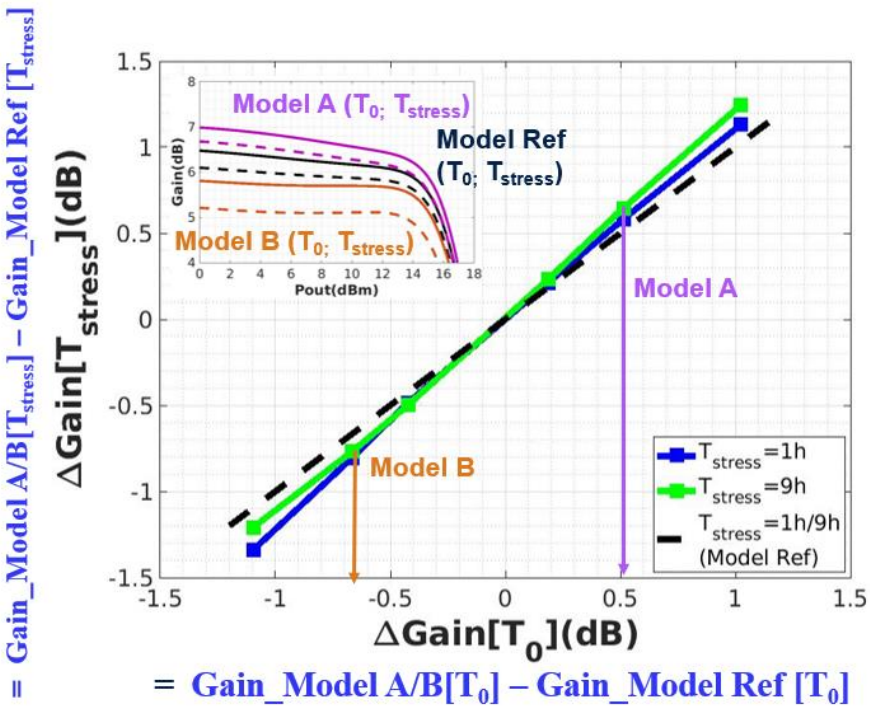

Figure 2-17 : RF gain degradation sensitivity dependence on precision of T0 MHC at different Tstress. Model A/B represents higher/lower gain at T0 compared to the reference model (Model Ref≈Measurement).

Through this sensitivity analysis, we have demonstrated the importance of accurate device modeling to obtain precise T_0 PA mission profiles. While it is particularly important for PA applications where gain performance is the essential figure-of-merit at a particular operating bias point, gain degradation mismatch does not have the same repercussions on logic circuits where it has less impact on circuit performance.

2.3.3 Impact of different physical effects on RF gain degradation

Another HCI sensitivity analysis to investigate the dependence of MOSFET physical effects i.e., drain-induced barrier lowering (DIBL), carrier mobility (μ) and velocity saturation (vsat), on RF gain degradation has been performed. In scaled MOSFET dimensions, these physical effects are known to have a significant impact on the device's I-V characteristics. Therefore, the quantification of DC parametric degradations, delta V_{Tlin}, delta V_{Tsat}, delta I_{dlin}, delta I_{dsat}, are dependent on mapping the degradation of the physical effect parameters in our age model.

Table 2-2 : Different DC Aging Model Cards describing MOSFET physical effects used for RF HCI sensitivity analysis

Aging Model Card	Aging Model Description
A1	Without DIBL, mobility and velocity saturation effects
A2	Without mobility and velocity saturation effects
REF	Complete aging model

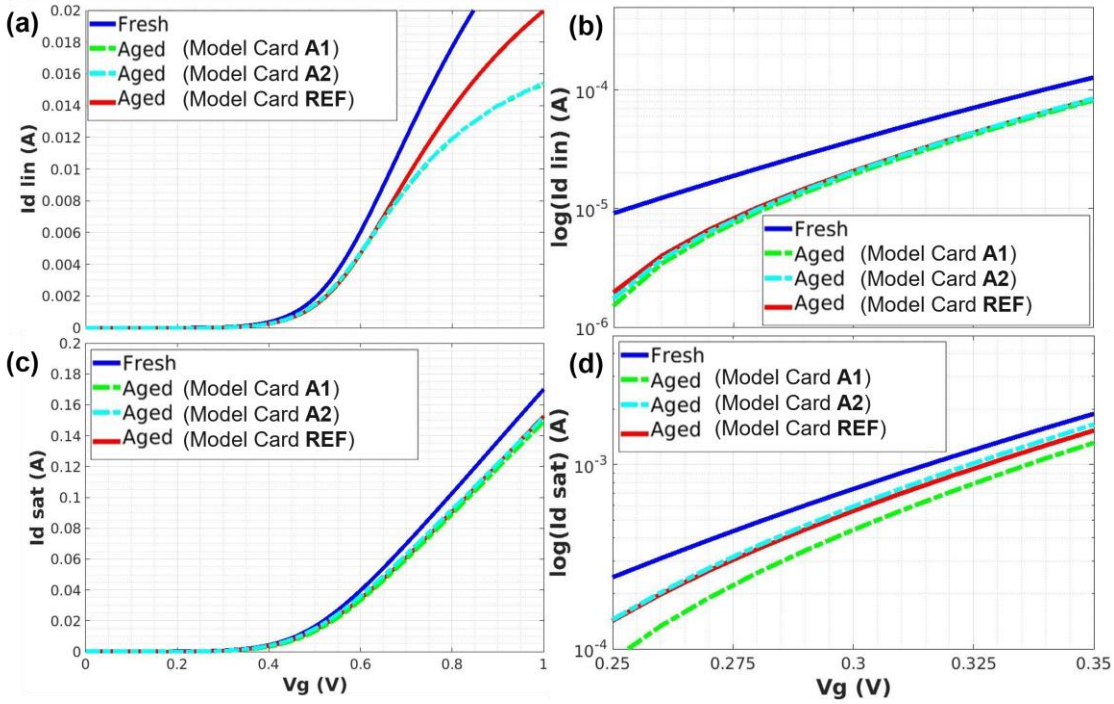

Figure 2-18 : Id-Vg (linear & saturation) extraction fresh and post-aging simulation showing the impact of different DC aging models associated to physical effects degradation modeling. DC measurements after standalone PA RF stress (from section *2.2.2.1*) are used to fit the complete aging model REF.

The different aging model cards in Table 2-2 describe the degradation modeling of the physical effects. The degraded IV curves from aging simulations of each aging model card are

illustrated in Figure 2-18, with Model REF being the complete aging model card (corresponding to DC measurements after standalone PA RF stress of 9 hours) used as the reference aging model. The absence of DIBL degradation modeling for A1 is observed in the log-scale plot of Id-Vg in saturation regime (see Figure 2-18(d)). Absence of μ_0 and vsat degradation modeling for A1 and A2 are observed in linear scale plot of Id-Vg at linear regime (see Figure 2-18(a)).

To analyze the impact of each aging model cards on RF performance degradation, the post-aging simulation results (9 hours of RF stress under same conditions for standalone PA in section 2.2.2) are presented in Figure 2-19. For the aging model card A1, we observe a mismatch of small-signal gain degradation due to the absence of DIBL degradation modeling, which is correctly modeled in aging model card A2. In both aging model cards A1 and A2 the mismatch in gain compression degradation is not correctly modeled due to partial modeling of mobility and velocity saturation degradation by R_{ON}, with comparison to the complete aging model REF. These results indicate that RF performance degradation is sensitive towards degradation modeling of physical effects in HCI aging models.

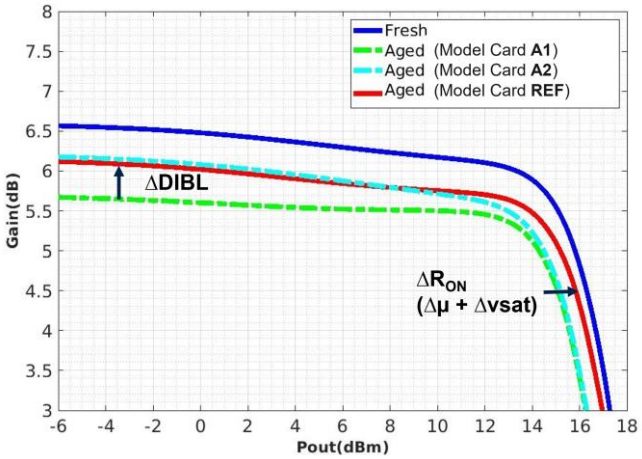

Figure 2-19 : RF gain from post-aging simulation of different aging models cards as described in Figure 2-18. Good fitting of degraded linear & saturation IdVg curves using DC aging model with physical effect modeling is required to accurately model RF HCI degradation.

2.4 Conclusion

In this chapter, we have demonstrated that HCI reliability analysis relies on accurate DC T_0 and aging parameter drift modeling established from PA device T_0 and stress measurements. The implementation of a mission profile-based reliability evaluation serves as a useful guideline for RF designers to achieve high efficiency and reliable PA design. This evaluation method allows RF PA designers to better estimate HCI reliability failures by avoiding critical aging zones. From a design perspective, the cascode PAs, subjected to lower RF HCI stress for the same stress duration, are more robust against HCI degradation. Unlike standard analog or mixed-mode circuits, in which worst-case HCI degradation usually occurs at $V_G \sim V_D/2$ for long channel devices or $V_G=V_D$ for short channel devices, it is now obvious that HCI degradation in PAs needs to be addressed according to their respective RF mission profiles. Therefore, it is also necessary to calibrate DC aging models especially Vd dependence for HCI stress to cater for PA-like RF stress conditions.

Performance-reliability trade-offs of RF PAs have been explored, indicating that cascode PA structures have an advantage over the standalone PA in terms of circuit performance and HCI reliability. In particular, the interstacked PA offers high RF performance (P_{SAT}, gain, linearity) and shows excellent reliability against accelerated RF HCI stress. Nevertheless, the standalone PA remains useful for T_0 and aging MHC validation.

By performing a simulation-based sensitivity analysis on the standalone PA, we have identified V_{Tlin} as the device parameter that is the most impacted by RF HCI degradation. As V_T reduction leads to transconductance gm reduction for a given bias point, which is an important design parameter directly linked to the PA RF performance, circuit design techniques to monitor and mitigate V_T shift is a viable solution to increase circuit reliability. PA RF degradation modeling accuracy also depends on T_0 MHC precision, as shown in this work, that it is possible to overestimate or underestimate RF stress degradation. Finally, we also covered the importance of building the aging model based on physical effects and how RF performance degradation is affected by different aging model parameters.

References

[1] X. Garros *et al.*, “A Very Robust and Reliable 2.7GHz +31dBm Si RFSOI Transistor for Power Amplifier Solutions,” in *2019 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2019, p. 25.5.1-25.5.4. doi: 10.1109/IEDM19573.2019.8993649.

[2] A. Divay *et al.*, “65nm RFSOI Power Amplifier Transistor Ageing at mm W frequencies, 14 GHz and 28 GHz,” in *2021 IEEE International Electron Devices Meeting (IEDM)*, 2021, p. 39.3.1-39.3.4. doi: 10.1109/IEDM19574.2021.9720531.

[3] A. Rathi, A. Dixit, P. Srinivasan, O. H. Gonzalez, and F. Guarin, “RF Reliability of CMOS-Based Power Amplifier Cell for 5G mmWave Applications” *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, pp. 4B.3-4B.3-6.

[4] P. Srinivasan, P. Colestock, T. Samuels, S. Moss, F. Guarin, and B. Min, “A novel methodology to evaluate RF reliability for SOI CMOS-based Power Amplifier mmWave applications,” in *2020 IEEE International Reliability Physics Symposium (IRPS)*, May 2020, pp. 1–4. doi: 10.1109/IRPS45951.2020.9129588.

[5] D. K. Huynh *et al.*, “Analysis of RF Stress Influence on Large-Signal Performance of 22nm FDSOI CMOS Transistors utilizing Waveform Measurement”.

[6] A. Lange, “A general approach for degradation modeling to enable a widespread use of aging simulations in IC design,” *Microelectronics Reliability*, 2022.

[7] S. Pazos, F. Palumbo, and F. Silveira, “Reliability-Aware Design Space Exploration for Fully Integrated RF CMOS PA,” *IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY*, vol. 20, no. 1, 2020.

[8] V. Huard, T. Quemerais, F. Cacho, L. Moquillon, S. Haendler, and X. Federspiel, “Design-in reliability approach for Hot Carrier injection modeling in the context of AMS/RF applications,” in *2011 International Reliability Physics Symposium*, Apr. 2011, p. 5A.5.1-5A.5.7. doi: 10.1109/IRPS.2011.5784517.

[9] J. Forest, “Architecture robuste avec ajustement de fréquence centrale et détection de phase et de tension pour des amplificateurs autonomes de puissance à base de coupleur hybride aux fréquences millimétriques.,” phd, Université de Bordeaux, 2020. [Online]. Available: http://www.theses.fr/2020BORD0027

[10] M. H. Montaseri, J. Aikio, T. Rahkonen, and A. Pärssinen, “Optimum Number of Transistors in Stacked CMOS Millimeter-Wave Power Amplifiers,” in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1–4. doi: 10.1109/ISCAS.2018.8351160.

[11] Y. S. Chauhan *et al.*, “BSIM compact MOSFET models for SPICE simulation”.

[12] D. W. Liu, D. X. Jin, D. Kanyu, D. Xuemei, and P. C. Hu, “BSIM4.3.0 MOSFET Model - User’s Manual.” UC Berkeley, 2003.

[13] M. Dehan, “Characterization and modeling of SOI RF integrated components,” PhD Thesis, UCL - FSA/ELEC - Département d’électricité, 2003. [Online]. Available: http://hdl.handle.net/2078.1/5015

[14] P. Wambacq, G. G. E. Gielen, P. R. Kinget, and W. Sansen, “High-frequency distortion analysis of analog integrated circuits,” *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS*, vol. 46, no. 3, 1999.

[15] E. P. Vandamme, D. Schreurs, C. van Dinther, G. Badenes, and L. Deferm, “Development of a RF large signal MOSFET model, based on an equivalent circuit, and comparison with the BSIM3v3 compact model,” 2002.

[16] L. Negre *et al.*, “Reliability Characterization and Modeling Solution to Predict Aging of 40-nm MOSFET DC and RF Performances Induced by RF Stresses,” *IEEE Journal*

of Solid-State Circuits, vol. 47, no. 5, pp. 1075–1083, 2012, doi: 10.1109/JSSC.2012.2185549.

[17] W. Arfaoui *et al.*, "A Novel HCI Reliability Model for RF/mmWave Applications in FDSOI Technology," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, May 2020, pp. 1–5. doi: 10.1109/IRPS45951.2020.9129479.

[18] T. Garba-Seybou, A. Bravaix, X. Federspiel, and F. Cacho, "Modeling hot carrier damage interaction between on and off modes for 28 nm AC RF applications".

[19] S. Mahapatra and U. Sharma, "A Review of Hot Carrier Degradation in n-Channel MOSFETs—Part I: Physical Mechanism," *IEEE Transactions on Electron Devices*, vol. 67, no. 7, pp. 2660–2671, 2020, doi: 10.1109/TED.2020.2994302.

[20] W. Arfaoui *et al.*, "Energy-driven Hot-Carrier model in advanced nodes," in *2014 IEEE International Reliability Physics Symposium*, Jun. 2014, p. XT.12.1-XT.12.5. doi: 10.1109/IRPS.2014.6861189.

[21] W. Arfaoui, "Experimental analysis of defect nature and localization under hot-carrier and bias temperature damage," 2013.

[22] A. J. Scholten, D. Stephens, G. D. J. Smit, G. T. Sasse, and J. Bisschop, "The Relation Between Degradation Under DC and RF Stress Conditions," *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2721–2728, Aug. 2011, doi: 10.1109/TED.2011.2153854.

[23] M. Abouchahine *et al.*, "Broadband Time-Domain Measurement System for the Characterization of Nonlinear Microwave Devices With Memory," *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES*, vol. 58, no. 4, 2010.

[24] A. Lange, F. A. V. Gonzalez, I. Lahbib, and S. Crocoll, "Comparison of modeling approaches for transistor degradation: model card adaptations vs subcircuits," in *ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC)*, Sep. 2019, pp. 186–189. doi: 10.1109/ESSDERC.2019.8901760.

[25] T.-P.-Y. Tran, "CMOS 180 nm Compact Modeling Including Ageing Laws for Harsh Environment," phd, L'UNIVERSITÉ DE BORDEAUX, 2022. [Online]. Available: http://www.theses.fr/2022BORD0185/document

[26] C. Yu and J. S. Yuan, "Electrical and Temperature Stress Effects on Class-AB Power Amplifier Performances," *IEEE Transactions on Electron Devices*, vol. 54, no. 6, pp. 1346–1350, Jun. 2007, doi: 10.1109/TED.2007.896601.

[27] L. Negre *et al.*, "Aging of 40nm MOSFET RF parameters under RF conditions from characterization to compact modeling for RF design," in *2011 IEEE Radio Frequency Integrated Circuits Symposium*, Jun. 2011, pp. 1–4. doi: 10.1109/RFIC.2011.5940645.

[28] L. Negre *et al.*, "Hot carrier impact on the small signal equivalent circuit," in *Proc. IEEE Int. Integr. Reliab. Workshop, 2010, pp. 72–75.*

3. Evaluation of frequency-dependent effects under RF off-state stress

Off-state leakage current (I_{off}) is becoming a critical reliability concern for both analog and digital circuits in deep sub-micron CMOS technologies. The downscaling of transistor dimensions has been necessary to accommodate the increasing chip density while enhancing the device's performance, precisely the on-current density I_{on}/W. The supply voltage V_{dd} and oxide thickness t_{ox} needs to be scaled accordingly to channel length and this incurs an increase in I_{off}. The I_{off} is composed of different contributions illustrated in Figure 3-1. As reported in [1], [2] the off-state drain current is dominated by I_{GIDL} arising from band-to-band-tunneling electrons and holes generated through impact ionization when $V_G<0$ under high drain electric field acceleration. During large V_{GD} stress in off-state configuration, the subsequently generated hot holes are injected into gate oxide creating interface states and/or bulk oxide defects resulting in device parametric degradations and oxide wear-out leading to breakdown at the drain-edge increasing with large V_{GD} stress [3], [4].

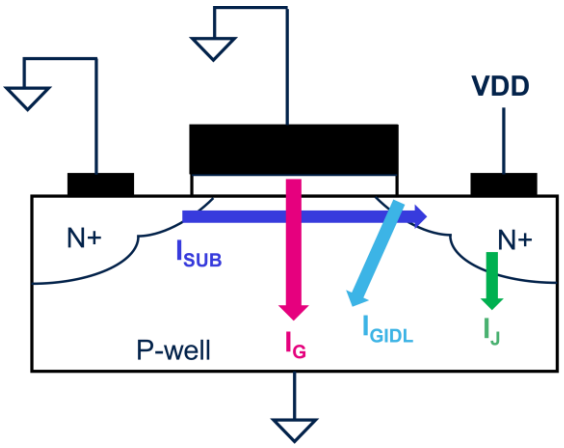

Figure 3-1 : Different contribution in off-state current in NMOS, I_G=gate leakage current due to direct tunneling, I_{SUB}=subthreshold current, I_J=junction leakage current, I_{GIDL}=gate induced leakage current.

The focus of this chapter is to investigate dynamic off-state reliability at GHz frequency. To evaluate the impact of the dynamic off-state stress, a dedicated test structure is designed in order to maintain the device under dynamic stress of 1GHz over a long time. This dedicated test structure generates pulsed waveform thanks to an integrated ring oscillator. The test structure design specifications are explained throughout the design process of the different building blocks. The integrity of the generated stress waveform is then demonstrated by means of experimental and simulation data. The purpose of this test structure design is to assess dynamic off-state reliability in relation to frequency dependence of TDDB, device parametric degradation and interaction with on-state hot carrier degradation. In the following, the design targets high temperature stress at 125˚C to accelerate off-state reliability mechanisms, especially TDDB, which is strongly activated by temperature.

3.1 Design of integrated test circuit for dynamic off-state stress evaluation

3.1.1 Challenges of dynamic off-state stress characterization

Extensive research has been conducted to investigate static (DC) off-state reliability in MOSFETs [1], [4], [5], [6], [7] and drain-extended MOS (DeMOS) [2], [8] devices, as well as their implications in digital circuit applications [9], [10], [11]. However, there is comparatively less research on RF off-state reliability. An explanation for this issue is that RF signal transmission constraints, such as propagation loss and insertion loss, arise beyond 1MHz due to the characteristics of coaxial cables, interconnects, and probes, as well as load impedance mismatch at these frequencies. RF signal generation is another challenge to address in order to fulfill high voltage amplitude and fast pulse transitions requirements during switching to create RF off-state stress conditions.

To overcome these limitations at higher RF frequencies, on-chip frequency generation using ring-oscillator-based test structures is one of the preferred approaches to directly apply RF test signal at the DUT input terminal. These test structures have been designed to provide dynamic stress stimuli (pulsed waveform) for on-state HCI, BTI [12] and on-state TDDB [13] analysis. In this section, the test structure design which targets off-state stress specifications at GHz level is described.

3.1.2 On-chip pulsed waveform generation based on ring oscillators

Ring oscillators (RO) are widely used as a simple and cost-effective solution to provide frequency synthesis in digital circuits up to several GHz. A simple RO topology which consists of N stages of CMOS inverters connected in a feedback loop is designed for our test structure. The frequency generated by the RO (F_{osc}) is determined by the propagation delay of each stage (τ_{inv}) and the number of stages (N) described in eq.2-1:

$$F_{osc} = \frac{1}{2N\tau_{inv}} \qquad \text{(Eq.3-1)}$$

An odd number of stages is required to produce oscillations with respect to the Barkausen condition. τ_{inv} depends on the load capacitance at each inverter output node which is attributed to the gate and parasitic depletion capacitances of the next inverter cell (related to the sizing of transistors in inverter cell) in addition to routing parasitic capacitance. To enable and disable oscillation, a NAND gate is added to apply RING_EN to toggle oscillating and open modes. A buffer stage is inserted between the RO output and the input of the next stage. This avoids the load capacitance imbalance between these two stages and ensures that the delay through each path is the same. Figure 3-2 shows the schematic of the RO design with N=43, NAND gate and buffer stage using standard cells consisting of thin-oxide transistors (GO1) with supply voltage Vdd=1V. The RO is designed to generate a pulsed waveform oscillating at a frequency of 1GHz with a 50% duty cycle, while rise and fall times are

compliant with 10% of the waveform period, i.e. 100ps. Another ring oscillator with oscillation frequency 500MHz was designed in the same manner to perform our studies at both 500MHz and 1GHz.

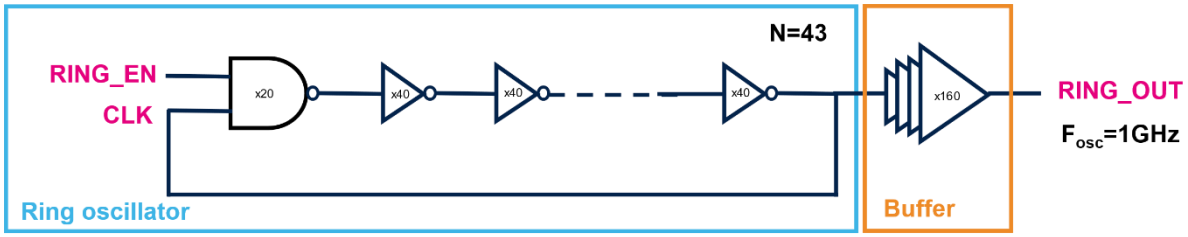

Figure 3-2 : Schematic of RO and buffer design to produce oscillations at F_{osc}=1GHz

The interface between the RO output and the drain terminal of the DUT is provided by a level shifter circuit and a set of transmission gates to alleviate design and reliability challenges of high frequency and large pulse amplitude of the oscillator. The specifications of this interface should fulfill the specifications for our off-state stress conditions which involves:

- High voltage level switching of at least twice of the nominal V_{DD}
- Rise and fall transition times within 10% of waveform period.
- 50% duty cycle

The level shifter was designed using the topology proposed in [14] suitable for low propagation delay and high speed switching applications. The output signal from the RO is upconverted from 1V to 2.5V via the level shifter circuit. The sizing of different GO1 and thick-oxide transistors (GO2) have been adapted to the performance of the transistors for voltage conversion with respect to foundry reliability margins. To enable multiple drain voltage stress levels, two transmission gates are implemented. The transmission gates act as a bi-directional switch between external DC voltage supply V_{HL} and V_{LL} without impacting level shifter speed performance. Each of them consists of a pair of NMOS and PMOS transistors connected in parallel (shown later in Figure 3-5(b)) using GO2 transistors with nominal V_{DD} of 2.5V. The full circuit operation is detailed in the next part.

Lastly, the DUT is designed using a body-contacted GO1 NMOS with gate width and length of W=100µm and L=60nm respectively. The large DUT width is consistent with analog/RF applications and to achieve device breakdown in a reasonable time frame for TDDB stress. However, the transition time depends on DUT width which is proportional to the equivalent intrinsic capacitance of the DUT. Figure 3-3 shows the transition times (rise and fall times) extracted from SPICE simulation results for W values ranging from 100µm to 400µm at fixed L=60nm and T=25°C at different V_{HL}. Both rise and fall times increase monotonically with W for minimum and maximum V_{HL} showing that larger W induces longer transitions. For values of W > 200µm, transition times for maximum V_{HL} = 2.5V exceed specification for 1GHz stress waveform conditions (>100ps), which justifies our choice of DUT W=100µm to ensure signal integrity. The layout implementation of the 1GHz test structure designed using STMicroelectronics 65nm partially depleted SOI (PDSOI) technology is shown in Figure 3-4, where the test structure is routed to DC probe pads for

wafer-level stress measurements. Comparison of post-layout simulations against SPICE simulations at T=125°C are presented in Table 3-1. These results show that the design specifications for off-stress state have been fulfilled. DUT and both 500MHz and 1GHz test structures characterization are described in the following section.

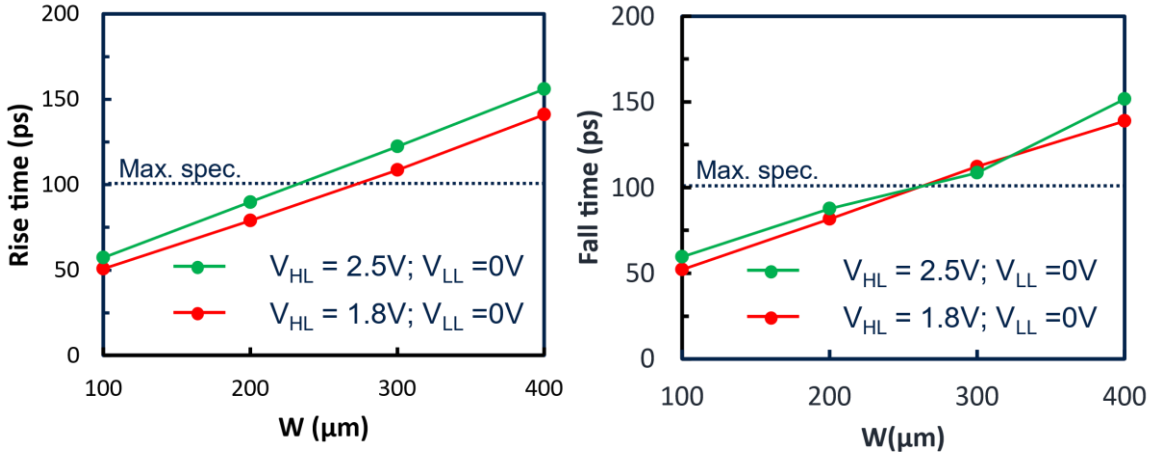

Figure 3-3 : Transition times (rise and fall times) increase monotonically as a function of DUT width.

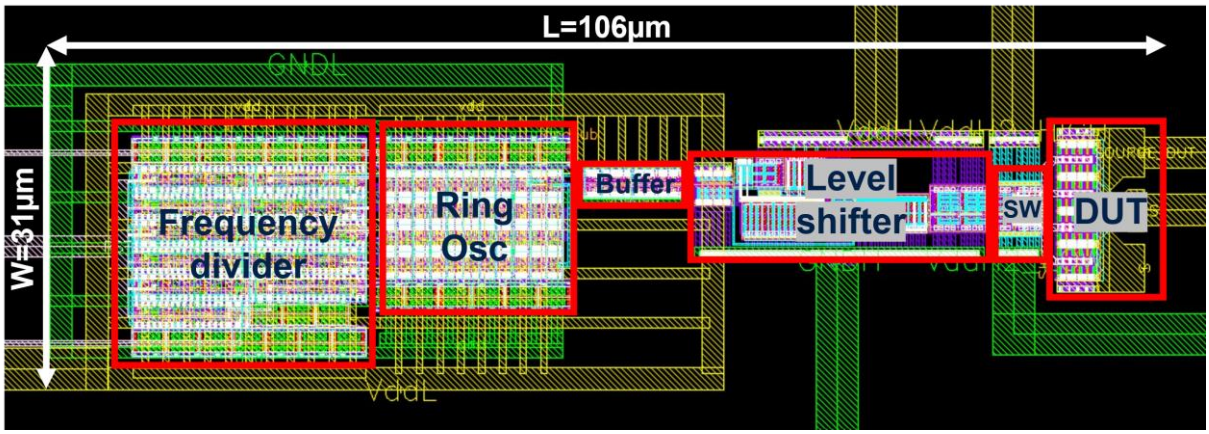

Figure 3-4 : Layout view of 1GHz test structure (connection to DC probe pads not shown here) implemented in STMicroelectronics 65nm PDSOI technology.

Table 3-1 : Performance of test structure from SPICE versus PLS simulations for DUT (NMOS GO1 L=65nm and W=100µm) at voltage and temperature conditions Vdd=1V; V_{HL}=2.5V; T=125°C

Test Structure	1GHz			500MHz		
	Specification	SPICE	PLS	Specification	SPICE	PLS
Frequency (GHz)	1	0.966	0.903	0.5	0.442	0.412
Trise (ps)	<100	75.04	84.3	<100	75.07	88.03
Tfall (ps)	<100	73.49	84.38	<100	73.68	87.73
Duty Cycle (%)	50	48.67	48.27	50	49.38	49.32

3.1.3 DUT description and operation modes

The different test structures are shown in Figure 3-5. $DUT_{standalone}$ in Figure 3-5(a) is used for DC and AC pulsed off-state stress with maximum frequency of 100kHz where the stress stimuli is applied directly to V_{Drain} via an external pulsed generator unit. In Figure 3-5(b),

$DUT_{Test\ structure}$ is used for AC pulsed waveform off-state stress generated by on-chip ROs with oscillation frequency of 500MHz or 1GHz. The same test structure using 500MHz RO was duplicated with direct drain access, shown as $DUT_{Test\ Structure\ Drain}$ in Figure 3-5(c). It is used to compare DUT standalone with and without direct drain access during DC characterization (discussed in Section 3.2.1) and to monitor transmission gate degradation during DC or AC stress (discussed in Section 3.4.2).

Off-state stress DC or AC pulsed waveform with maximum frequency of 100kHz can be applied directly to V_{Drain} of $DUT_{standalone}$ via an external pulsed unit generator. DC or AC off-state stress modes of $DUT_{Test\ structure}$ and $DUT_{Test\ structure\ drain}$ are controlled by the RO enable signal (Ring_EN) which is illustrated in Table 3-2. When Ring_EN ='0', DC mode is activated, so that the DC bias V_{HL} is applied at the drain node. AC mode is activated when Ring_EN='1', so that an AC pulsed signal oscillating between V_{HL} and V_{LL} at 500MHz or 1GHz with 50% duty cycle is applied at the drain node.

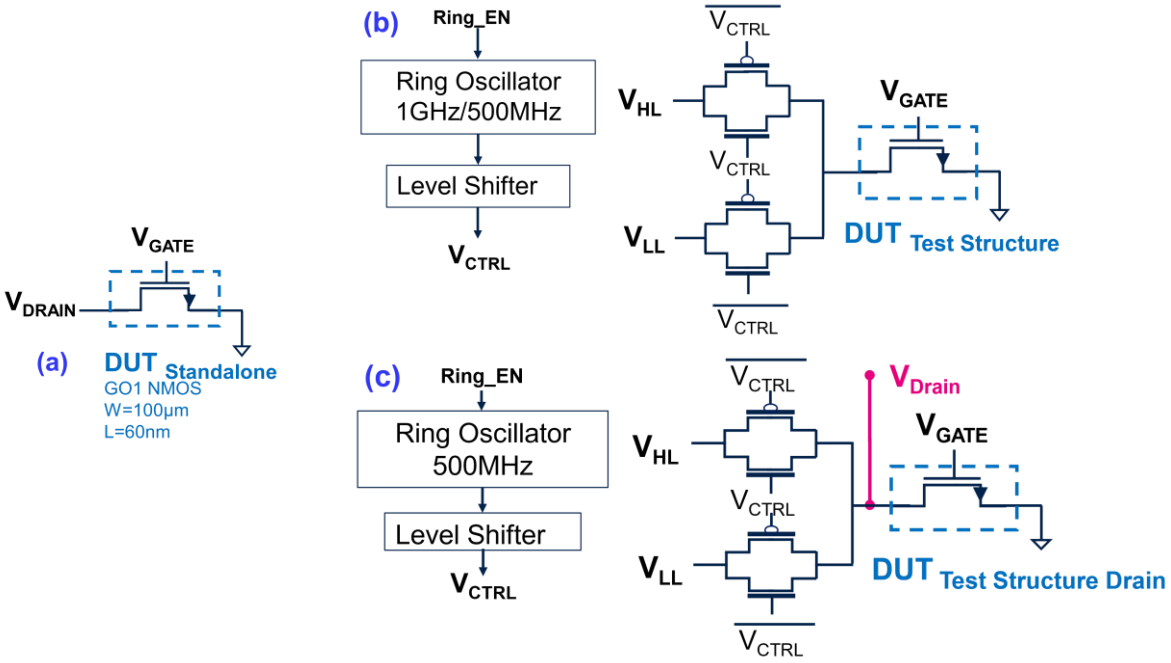

Figure 3-5 : (a) Standalone DUT consisting of a body-contacted GO1 NMOS in 65nm PDSOI technology, RO test structures (b) without direct drain access (c) with direct drain access. DC and AC stress modes are applied to DUT drain terminal via transmission gates controlled by RO oscillation mode (Ring_EN).

Table 3-2 : DC and AC operating modes of $DUT_{Test\ structure}$ and $DUT_{Test\ Structure\ Drain}$

Mode	Ring_EN	V_{CTRL}	$\overline{V_{CTRL}}$	V_{Drain}
DC	'0'	'1'	'0'	V_{HL}
AC	'1'	'1'	'0'	V_{HL}
		'0'	'1'	V_{LL}

3.2 Test structure characterization in DC and AC mode

3.2.1 IDVG characterization

Prior to off-state drain stress measurements, DC characterization was conducted on each test structure to ensure the signal integrity of the pulsed waveform at V_{Drain}. Firstly, linear I_DV_G DUT characterization in DC mode is performed for the three structures at V_{Drain} = V_{HL}= 50mV, which is illustrated in Figure 3-6 with good correlation to simulation data. The linear current I_{VHL} of $DUT_{Test\ structure}$ saturates from V_{Gate}=0.3V onwards due to the significant on-state resistance of transmission gates ($R_{onSwitch}$) in series with the DUT, observed for both measurement and simulation data. To explain this result, the equivalent schematic of test structures with and without direct drain access for linear I_DV_G characterization is illustrated in Figure 3-7. For $V_{Gate} > V_T$, the DUT on-state resistance (Ron_{DUT}) varies according to its ratio against $R_{onSwitch}$. When R_{onDUT} is smaller or equal compared to $R_{onSwitch}$, V_{Drain} is drastically reduced due to voltage dividing effect. On the other hand, for $V_{Gate} < V_T$ (subthreshold and

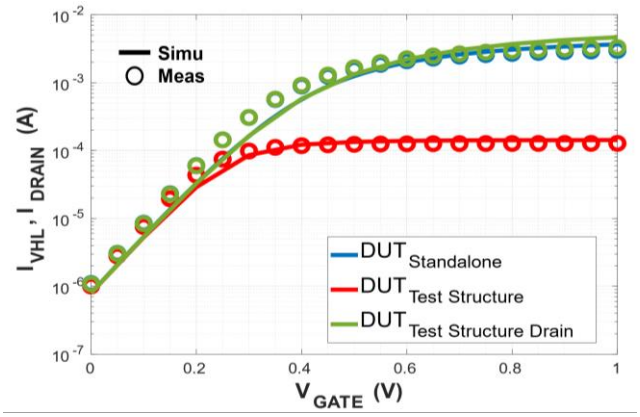

Figure 3-6 : log (I_{Drain})V_G DC characterization at V_{Drain}=V_{HL}=50mV. From V_{Gate}=0.3V onwards, saturation of linear I_{VHL} (red) is due to large $R_{onSwitch}$ in series with DUT (refer to Figure 3-7).

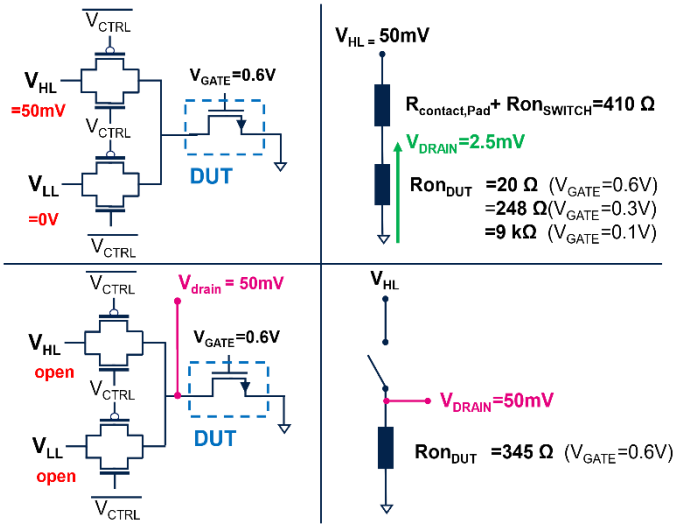

Figure 3-7 : Equivalent schematic of DUT test structures with (bottom) and without (top) drain access for linear I_DV_G characterization (VHL=50mV). V_{Drain} of DUT test structure without drain access is reduced when Ron_{DUT} is smaller or equal to Ron_{Switch} which occurs for $V_{Gate} > V_{T\ DUT}$.

off-state regime) I_{VHL} is aligned with I_{Drain} of DUT $_{Standalone}$ due to large off-state resistance of the DUT, i.e., 9kΩ at V_{Gate} = 0.1V, compared to $R_{onSwitch}$ =410Ω. In other words, it is not relevant to compare I_{Dlin} at V_{Gate} = 1V and V_{Drain} = 50mV across different structures, as per convention. In the following section 3.4, I_{VHL} of DUT $_{Test\ Structure}$ is extracted at V_{Gate}= 0.3V for equivalent I_{Dlin} degradation (ΔI_{Dlin}) comparison with I_{Dlin} of DUT $_{Standalone}$.

3.2.2 IDVD characterization

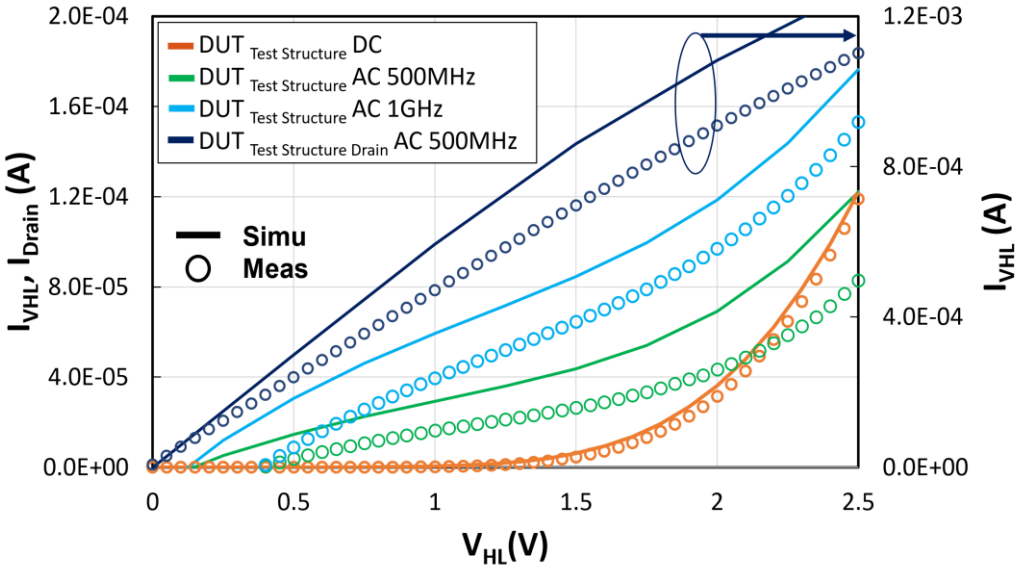

Figure 3-8 : I_DV_D characterization at V_{Gate}= -1V, corresponding to off-state stress conditions. A higher average I_{VHL} during AC mode is attributed to large current peaks during transmission gate switching (refer to Fig. 6). The measurement results show good correlation to simulation.

When these peak currents are neglected, the ratio of measured I_{VHL}(DC)/I_{VHL}(AC)=2.15 for V_{HL}= 2.3V, translating to a duty cycle of 46.5%. In the case of DUT$_{Test\ Structure\ Drain}$, V_{Drain}(t) AC 500MHz waveform shown in Figure 3-9 is altered due to capacitive loading of probes at drain access terminal, resulting in a larger I_{VHL}(AC) than that of AC 500MHz without drain access, which is supported by experimental results in Figure 3-8.

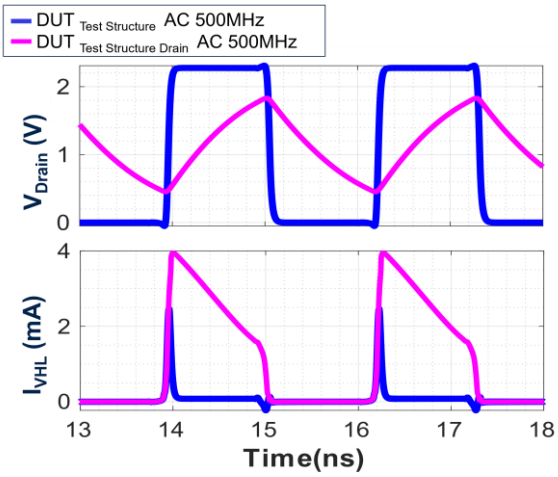

Figure 3-9 : Simulation results of DUT drain voltage (top) and current (bottom) waveforms during AC mode (V_{Gate}=-1V, V_{Drain}=V_{HL}=2.3V) of test structure with and without direct drain access.

3.2.3 DC and AC off-state breakdown characterization

Figure 3-10 shows the breakdown voltages (BV) of different test structures which are determined by conducting fresh (T_0) I_GV_D and I_DV_D characterization for off-state V_{Gate} = -1V while V_{Drain} is swept until device breakdown at temperature T=125°C. The BV of $DUT_{standalone}$ is at V_{Drain} =2.7V while in the case of $DUT_{Test\ Structure}$ under DC mode the BV is at V_{HL}=3.2V due to voltage drop across Ron_{Switch} as I_{VHL} increases with V_{HL}. In AC mode 500MHz and 1GHz, the BV of DUT $_{Test\ Structure}$ is higher at V_{HL}=3.75V due to the combined effects of Ron_{Switch} voltage drop and duty cycle factor.

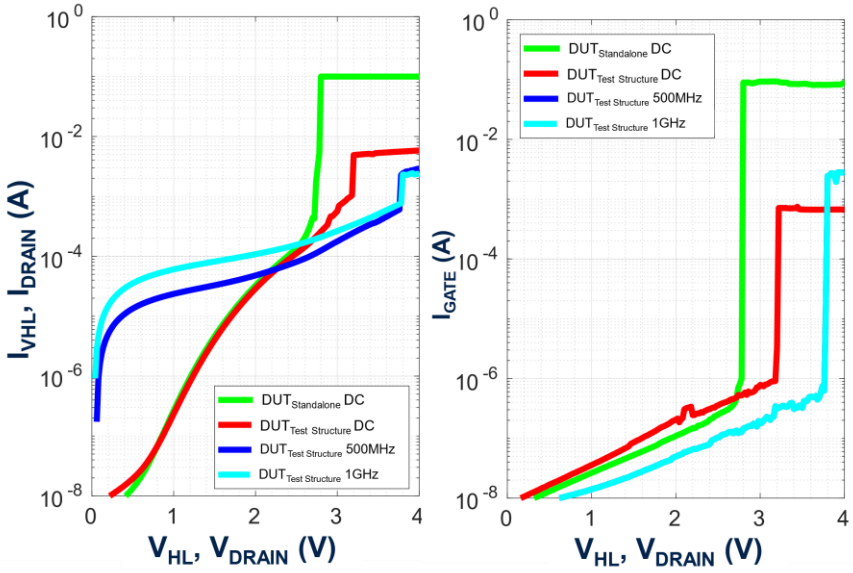

Figure 3-10 : Fresh device/test structure characterization of breakdown voltage (BV) for V_{Gate}= -1V at T=125°C. The BV for $DUT_{standalone}$ is 2.7V. For test structures in AC mode, BV is almost twice of the BV in DC mode.

Through the characterization of different test structures, we have concluded that the impact of $R_{onSwitch}$ on V_{Drain} signal integrity is negligible during off-state DC and AC modes due to the small leakage current flowing through $R_{onSwitch}$, making it suitable for off-state stress evaluation. The duty cycle factor (DF) determined from average current ratio I_{VHL}(DC)/I_{VHL}(AC) is an important tool for AC stress time scaling to obtain equivalent time stress to compare against the DC stress case. However, during linear I_{Dlin} characterization at V_{HL} =50mV and V_{Gate}>VT in DC mode, it is necessary to consider IR drop caused by on-state current flowing through $R_{onSwitch}$. For this reason, I_{Dlin} is extracted at V_{Gate} =0.3V instead of conventional V_{Gate} =1V definition for $DUT_{Test\ Structure}$. DC and AC breakdown characterization of the test structures indicate that the drain stress voltage should be lower than V_{Drain} = V_{HL} = 2.5V to avoid avalanche breakdown.

3.3 Off-state RF TDDB

3.3.1 Current studies in off-state DC and RF TDDB

Significant progress has been made in off-state DC reliability research to explain the physical origins and nature of damage of off-state DC TDDB. An experimental and modeling study by

[2] has demonstrated that the off-state damage by hot hole injection originates from broken Si-O bonds, also known as interface and oxide (bulk) defects, which are not recoverable upon the removal of the off-state stress. These defects, which have a peak concentration at the gate-drain overlap region, have been correlated to the formation of an asymmetric percolation path resulting in dielectric breakdown at the spacer region (outside the gate-oxide) for drain-extended NMOS transistors [15]. However, [7] reported that the breakdown spot is more likely to occur in the gate-oxide at drain edge for FDSOI 28nm NMOS transistor due to the non-power law dependence of spacer breakdown.

The frequency dependence of off-state TDDB has become an increasing topic of interest in the reliability of RF devices [16] and in particular power amplifiers [17], [18], [19] where the device is subjected to high drain voltage swings while operating in off-state. For example, class-E PA functioning as a switch in [20] has reported breakdown after 1ks at 1.8GHz under maximum RF stress V_{DG} = x2VDD_{NOM} using thick oxide device. On the other hand, RF TDDB experiments at 14GHz has been reported in [18], where no hard breakdown was evidenced after 50ks under maximum RF stress V_{DG} = x2VDD_{NOM} for CMOS SOI class-AB. These previous works involve sinusoidal stress waveform at both gate and drain terminals, where the interaction between different degradation modes is present and competes with off-state damage (this will be discussed in section 3.5). To isolate off-state RF TDDB from other potential degradation or recovery mechanisms, our test structure and stress methodology focuses on drain stress only DC/AC stimuli in off-mode which will be described in the following sections.

3.3.2 Stress methodology & experimental setup

DC and AC TDDB off-state stress measurements were conducted at 125°C on $DUT_{Standalone}$ and $DUT_{Test\ Structure}$ by applying stress voltages V_{Drain} = V_{HL} = 2.3V and V_{Gate} = -1V to achieve reasonable time-to-breakdown (T_{BD}) while the body terminal is tied to the source terminal which is kept grounded. The constant voltage stress method combined with on-the-fly monitoring of gate, drain and source currents during the stress without interruption. 15 samples were stressed for each condition until detection of hard breakdown by an abrupt increase in gate or drain current (simultaneously) of several orders of magnitude.

3.3.3 Results and discussion

The Weibull distribution in Figure 3-11 is plotted to illustrate the time-to-failure distribution of the stressed devices. The TBD of equivalent time stress for AC stress conditions are scaled by applying the duty cycle factor, DF=2.15, using the relation T_{BDeq} = T_{BDAC}/DF. The two representative indicators of the Weibull distribution (W), β which is the slope parameter and T_{63} which signifies T_{BD} at 63% corresponding to W=0 in the Weibull plot, are determined from eq.3-2 for each DC and different AC stress frequencies.

$$W \equiv ln(-ln(1 - F(t)) = \beta.ln(t) - ln(T_{63}) \qquad \text{(Eq.3-2)}$$

It is observed that T_{63} DC and AC 100kHz are similar while T_{63} increases with increasing stress frequency up to 1GHz. We found that the gain factor between T_{63} AC 1GHz and T_{63}

DC is 2.15 which points out that AC TDDB indeed exhibits longer lifetime than DC TDDB. In contrast, β =1.27 remains constant at different stress frequencies up to 1GHz. The similarity between our findings and those reported in [13], [21] regarding on-state RF TDDB at 1GHz frequency suggests that the power law model proposed by [22] can be applied to off-state RF TDDB. As explained in Chapter 1, This model describes the frequency acceleration factor as a function of power-law with exponent n-1 illustrated in eq.3-3, where N_{BD} represents the number of pulses to reach breakdown and A is a constant. This analytical model describes the T_{63} AC gain by the difference in DC and AC defect generation rate over time.

$$T_{63\,AC} = F^{n-1}\frac{N_{BD}}{A} \qquad \text{(Eq.3-3)}$$

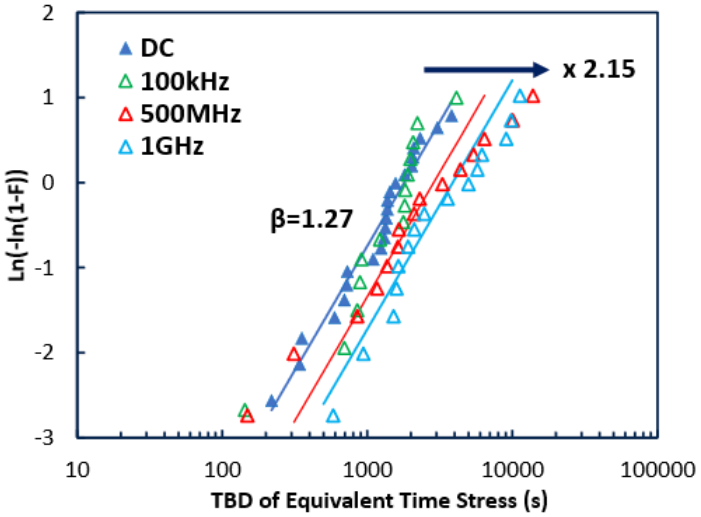

Figure 3-11 : Weibull distribution of DUT standalone and DUT test structures at V_{HL}=V_{Drain}=2.3V for DC, 100kHz, 500MHz and 1GHz stress at T=125°C. The Weibull slope β=1.27 remains constant for both DC and AC stress frequencies. A gain factor of 2.15 in time-to-breakdown (TBD) is observed at 1GHz stress compared to DC stress.

By applying the analytical model in eq.3-3, the experimental data from T_{63} AC 500MHz and 1GHz are used to fit the parameters of our off-state TDDB model in Eq.3 with an exponent n=1.76, shown in the plot of Figure 3-12(a). Interestingly, for the on-state RF TDDB model in [22] an exponent n=1.3 was reported, indicating that device lifetime gain is higher in off-state than on-state RF TDDB stress for identical A and N_{BD}. A "plateau" for frequencies lower than 100kHz is observed, which is not covered by the proposed model in [22]. Additional data is required to confirm T_{63} AC data trend for frequencies between 100kHz and 500MHz. Using this frequency model, it is possible to extrapolate T_{63} until 28GHz corresponding to the operating frequency for mmW applications to compare T_{63} gain factor. The T_{63} ratio between AC and DC is x25 larger at 28GHz, as shown in Figure 3-12(b). However, it is unclear whether the T_{63} improvement will reach a threshold frequency, as suggested by [23]. Without a doubt, experimental results are essential to prove model validity of T_{63} gain at frequencies beyond 1GHz in future works.

As V_{Dmax} margins for RF PA design are usually fixed by T_{BD} DC yielding conservative estimations of device time-to-failure, T_{BD} AC projections might be beneficial for RF PA design optimization by reducing V_{Dmax} overhead at higher frequencies. Still, the

impact of multiple failure modes including electromigration, on-state and off-state hot-carrier degradation combined with oxide wear out need to be analyzed to improve model accuracy of lifetime prediction for RF circuits.

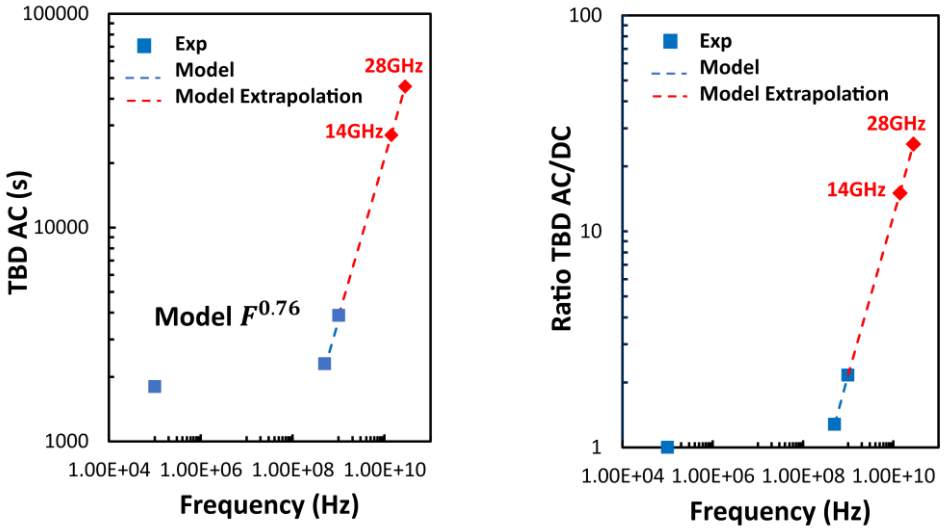

Figure 3-12 : (a) T_{BD} AC experimental data fitted to frequency power law model with an exponent of n=0.76. (b) T_{BD} AC Model extrapolation at 28GHz (mmW PA operating frequency) shows x25 estimated gain factor compared to T_{BD} DC.

3.4 Off-state degradation from DC to 1GHz stress

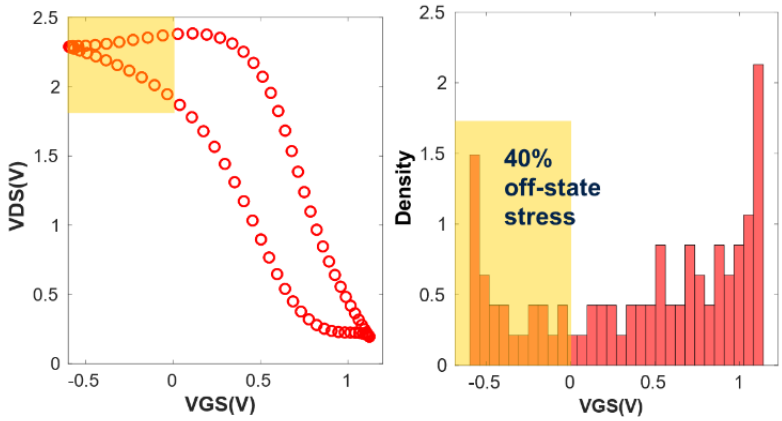

Figure 3-13 : Mission profile of RF linear power amplifier (left) with off-state region at VG<=0 highlighted. The probability density function of this region (right) represents 40% of the total time in RF cycle.

Previously in chapter 2, we have identified that the class AB PA device is subjected to alternatively on-state and off-state stress when driven near to saturation output power at 28GHz, as shown in the PA mission profile in Figure 3-13. In the case of on-state HCI, DC to RF degradations have been established via quasi-static approximations, enabling accurate estimations via RF reliability modeling approach. On the other hand, accurate estimations of RF off-state degradations are more difficult to reproduce, given the lack of understanding on the frequency-dependent behavior at GHz level. Our proposed study is focused on investigating parametric degradation such as linear threshold voltage V_{Tlin} and drain current I_{Dlin} at MHz and GHz frequency compared to the DC case.

3.4.1 Stress methodology and procedure

To study the impact of dynamic-off-state stress on ID_{lin} degradation, a Stress-Measurement-Stress methodology is used. During stress phase, stress bias conditions V_{Gate}=-1V and V_{Drain}= V_{HL}=V_{stress}=2.2V are applied on DUT at DC or AC stress frequency 100kHz, 500MHz or 1GHz while during measurement phase DC mode is activated to record linear I_DV_G measurements to enable extraction of ΔI_{Dlin} at V_{Gate} =0.1V, 0.3V,0.6V when using the $DUT_{standalone}$ or ΔI_{VHLlin} at V_{Gate}=0.3V when using the $DUT_{Test\ Structure}$. The total stress time is fixed depending on V_{stress} to avoid device breakdown during the experiment. The equivalent stress time for AC stress is scaled by the DF factor to compare AC against DC degradation results.

3.4.2 Results and discussion

The $DUT_{standalone}$ and $DUT_{Test\ Structure}$ were stressed at T=125°C under DC and AC off-state conditions via the stress-measurement-stress methodology for stress voltage V_{stress}=V_{Drain}=2.2V. In Figure 3-14, we show the evidence of off-state stress DC, AC 500MHz and 1GHz degradation of $DUT_{Test\ Structure}$ on linear I_DV_G characteristics compared to that of the fresh device T_0. An increase in the threshold voltage V_T for SiO2/SiON gate stack (due to charging of interface traps by hot holes), decrease in transconductance G_m (due to the increase in drain resistance caused by hot hole damage localized at gate-drain overlap region/LDD) and an increase of subthreshold slope (due to increase of interface traps).

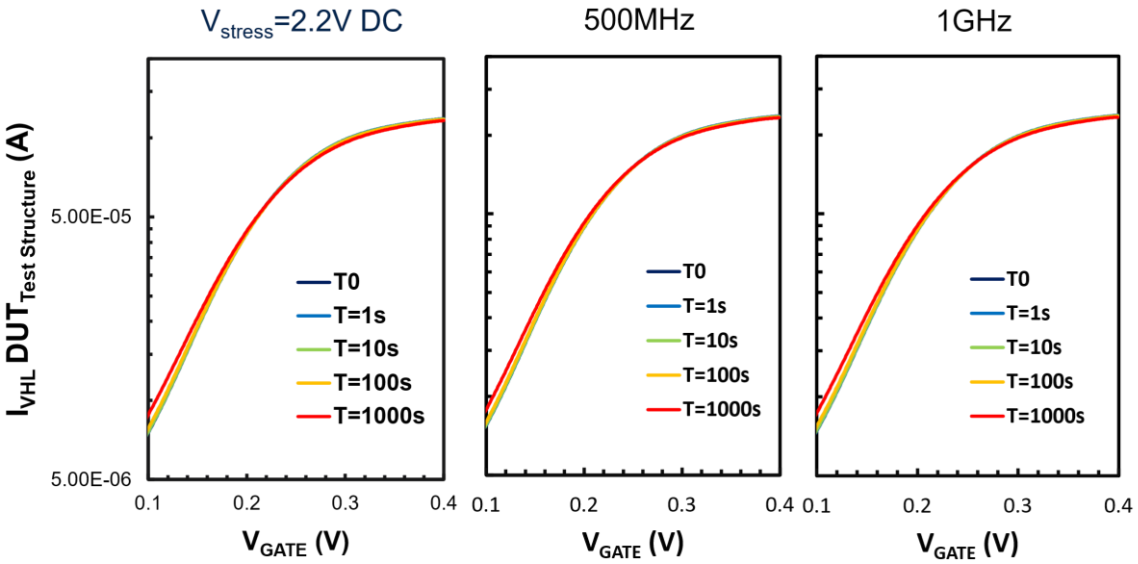

Figure 3-14 : Off-state degradation on linear I_DV_G characteristics of $DUT_{Test\ Structure}$ for DC and AC stress at V_{HL}=2.2V. AC stress pivot point (similar for both 500MHz and 1GHz) is at higher V_{Gate} compared to DC stress pivot.

For both DC and AC stress, a pivot effect between V_{Gate} = 0.1V and 0.3V is observed as I_{Dlin} is increased for V_{Gate}=0.1V (subthreshold current) while I_{Dlin} is decreased for V_{Gate} = 0.3V and 0.6V (weak inversion current). It has been reported in [1], [24] that the pivot effect resulting from off-state stress is due to the discharge of interface traps depending on V_{Gate} bias measurement conditions of device, from depletion to weak inversion. These traps are of

amphoteric nature in which the different charge states (donor or acceptor) are determined by the Fermi potential controlled by V_{Gate} bias during characterization.

To confirm that ΔI_{VHLlin} is not influenced by degradation of transmission gate device, we monitor Ron_{Switch} during the stress and measurement phase using $DUT_{Test\ Structure\ Drain.}$ The Ron_{Switch} characterization during stress and measurement phase is detailed in the configuration presented in Table 3-3. The high impedance (High Z) is defined to measure V_{Drain} (stress phase) and avoid current leakage via gate and source of DUT (measurement phase). Then, the Ron drift can be extracted by measuring the drain current I_{VHL} across voltage drop V_{HL} - V_{Drain}. The comparison of Ron_{Switch} degradation for DC and AC 500MHz at V_{stress}=2.2V condition is shown in Figure 3-15. No significant Ron_{Switch} degradation is observed during stress and measurement phase, which validates the test structure application for off-state stress experiments.

Table 3-3 : Configuration of different terminals for Ron_{Switch} characterization for stress and measurement phase

	Stress	Measurement
V_{HL} (V)	2.2	0.05
V_{Drain} (V)	High Z	GND
V_{Gate} (V)	-1	High Z
V_{Source}	GND	High Z

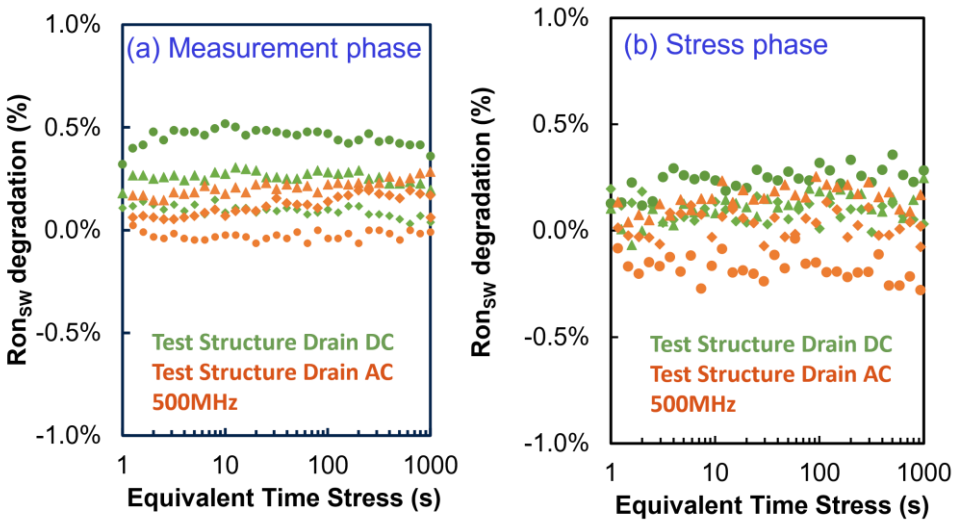

Figure 3-15 : Comparison of Ron_{Switch} degradation under DC and AC 500MHz stress extracted during (a) measurement phase (VHL=50mV) and (b) stress phase (VHL=2.2V) by using $DUT_{Test\ Structure\ Drain}$. No significant degradation is observed on all the 3 samples tested for each condition.

Up to this point, we have verified the off-state degradation characteristics under DC and AC stress. Our experimental data has demonstrated that AC off-state degradation exhibits the pivot effect as also observed in DC degradation (V_{Gate}=0.2V), where in the pivot point is located at higher V_{Gate} =0.23V for AC stress conditions. To continue investigations on dynamic off-state degradation behavior, MOSFET degradation parameter ΔI_{Dlin} ($DUT_{Standalone}$) and ΔI_{VHL} ($DUT_{Test\ Structure}$), which are relevant monitoring parameters due to their higher probing sensitivity towards interface traps, are extracted from the linear I_DV_G curves of Figure

3-14. The cumulative degradations of I_{Dlin} and I_{VHL} normalized to T_0 and plotted against the equivalent time stress.

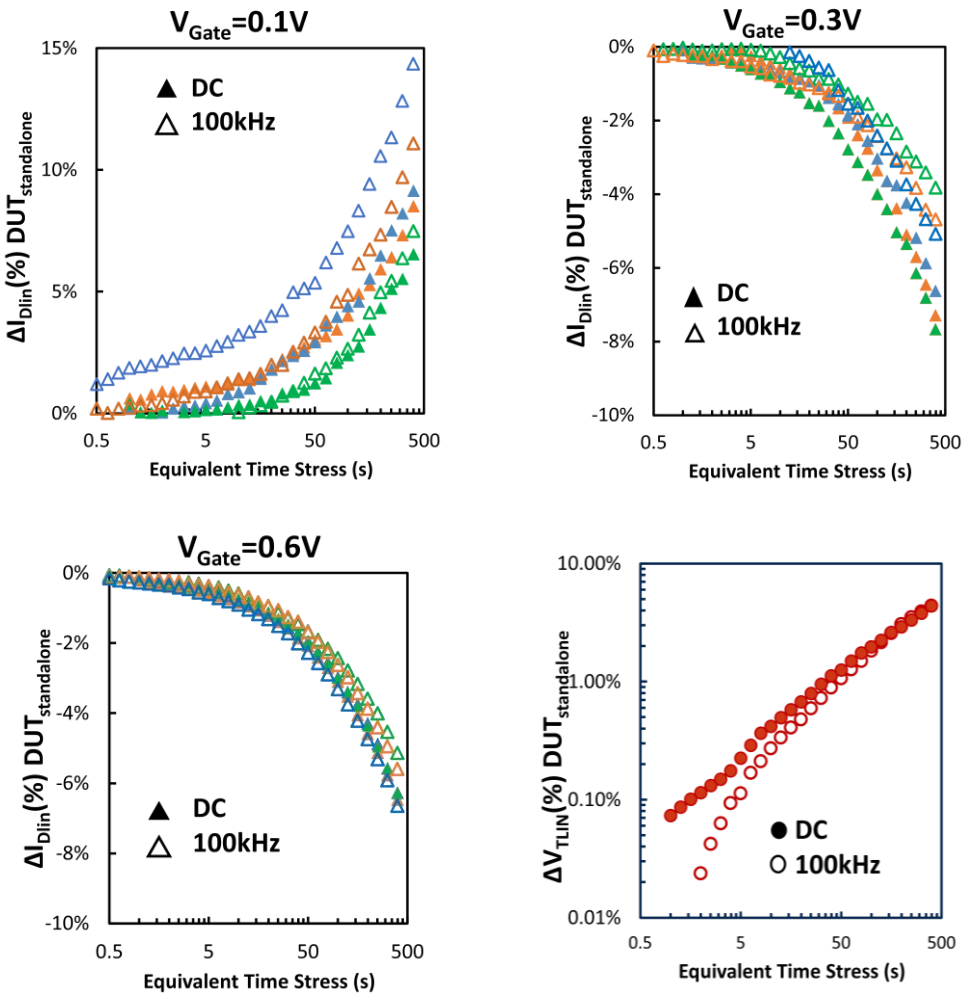

Figure 3-16: I_{Dlin} degradation (ΔI_{Dlin}) of DUT standalone extracted at different (a)V_{Gate}=0.1V, (b) V_{Gate}= 0.3V and (c) V_{Gate}=0.6V during measurement phase for V_{stress}=V_{Drain}=2.2V DC and 100kHz stress conditions. The pivot effect is located between measurement bias of V_{Gate}= 0.1V and 0.3V. (d) No significant difference is observed in V_{Tlin} degradation (ΔV_{Tlin}) of DUT standalone at DC and 100kHz stress.

In Figure 3-16(a), (b) & (c), we have plotted the cumulative ΔI_{Dlin} of $DUT_{Standalone}$ at various V_{Gate} characterization at V_{Drain}=50mV, for V_{stress}=V_{Drain}=2.2V, where it is observed I_D degrades for V_{Gate} =0.3V and V_{Gate} =0.6V but improves for V_{Gate} =0.1V due to the pivot effect. ΔI_{Dlin} is slightly higher for DC stress compared to AC 100kHz stress condition for V_{Gate} =0.3V but the difference becomes smaller as V_{Gate} moves further away from the pivot point. However, ΔV_{Tlin} in Figure 3-16(d) shows that there is no difference in AC stress compared to DC stress. We are presuming from the plot of ΔV_{Tlin} in Figure 3-16(d) that the interface trap generation rate ΔN_{IT} is unaffected by the drain relaxation sequence (V_{Gate} =-1V and V_{Drain}=0V during half of the stress period) for AC stress, which has also been reported in [24]. Likewise, to observe the ΔI_{VHL} at DC, 500MHz and 1GHz, ΔI_{VHL} of $DUT_{Test\ Structure}$ is extracted at V_{Gate} =0.3V, as shown in Figure 3-17(a). Δ I_{VHL} is frequency independent at both 500MHz and 1GHz, suggesting a quasi-static degradation behavior and consistent with the results observed for AC stress 100kHz. In Figure 3-17(b), the log-log plot of ΔI_{Dlin} and ΔI_{VHL} shows time-power law dependence with exponent n=0.56 and n=0.5 respectively, in agreement with DC off-state analysis for NMOS L=40nm GO1 device in [1].

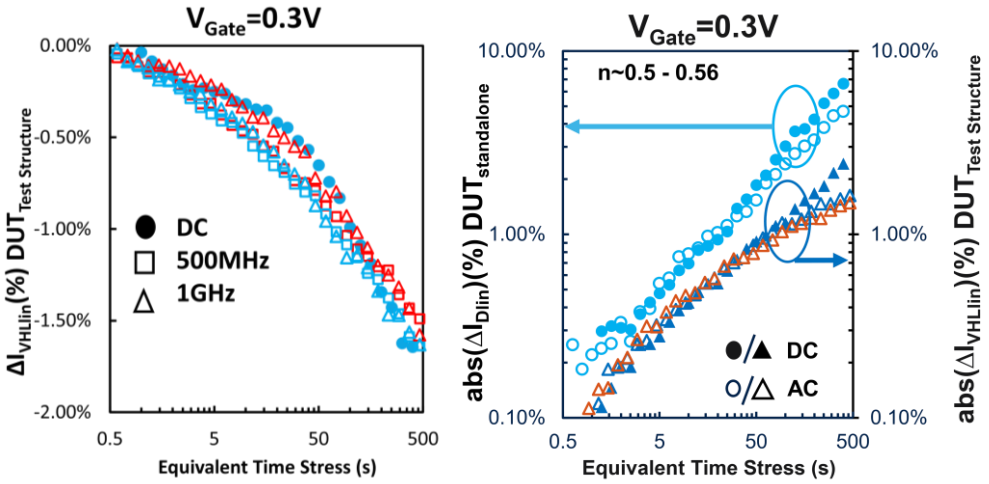

Figure 3-17(a): I_{VHLlin} degradation of $_{DUTTest\ Structure}$ (ΔI_{VHLlin}) extracted at V_{Gate}=0.3V during measurement phase for V_{stress}=V_{Drain}=2.2V at DC, 500MHz & 1GHz stress frequencies. (b) ΔI_{VHLlin} of AC stress follows ΔI_{VHLlin} trend of DC stress (n=0.5~0.56). ΔI_{VHLlin} is lower than ΔI_{Dlin} due to Ron_{Switch} during measurement phase

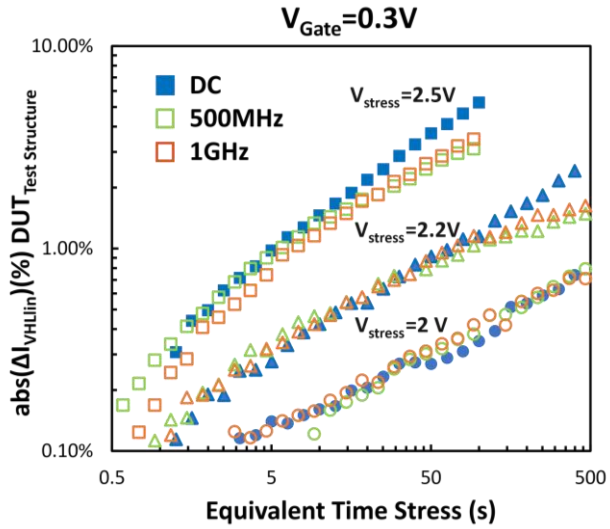

Figure 3-18 : Comparison of abs(ΔI_{VHLlin}) during measurement phase for different V_{stress}=V_{Drain}=2V, 2.2V & 2.5V at DC and AC stress frequencies

The V_D dependence of ΔI_{VHLlin} is then discussed based on the experimental results in Figure 3-18. The I_{VHLlin} degradation rate for V_{stress}=2.5V is slightly higher than V_{stress}=2.2V and 2V. This reflects the higher ΔN_{IT} governed by a higher hot hole injection efficiency when the stress bias V_{GD} is increased. A saturation behavior for 500MHz and 1GHz AC stress at higher V_{stress} is also observed but is not present in DC stress. A possible explanation for this behavior is the different defect generation time dynamics between DC and AC stress, as proposed in [22]. If this assumption holds true, it means that RF off-state degradation and TDDB are correlated and explain the increase of time-to-breakdown at 500MHz and 1GHz in Section 3.3.3. Another possible explanation would be the difference in spatial distribution of the interface defects due to the localized E-field at the gate edge overlapping with drain spreading into LDD, causing a variation in stress electric field which then reduces the defect generation rate [2]. Different defect probing methods such as stress induced leakage current

(SILC) or charge-pumping (CP) measurements could be performed in future work to confirm these assumptions.

To summarize, by studying the parametric degradation linear drain current of dynamic off-state stress results at 500MHz and 1GHz proportionally to ΔN_{IT}, we have demonstrated that no frequency dependence is observed compared to the DC stress. This allows us to model off-state degradation at RF frequencies using the quasi-static approach. To complete these off-state degradation investigations, the interaction between on-state and off-state degradation mechanisms at RF frequencies need to be determined to provide accurate RF PA reliability modeling.

3.5 Interaction between on-state and off-state degradation

3.5.1 Interaction modeling strategy

Modeling the interaction between different degradation mechanisms is pivotal for digital and RF devices that operate under mission profiles involving complex AC waveforms as the interaction between different degradations mechanisms can impact defect generation rate or carrier trapping/de-trapping dynamics. The experimental results in [3] using HKMG NMOS GO1 transistors reveals that the off-state degradation level depends on the pre-stress on-state hot carrier degradation mode (M1/M3), while no dependence of pre-stress off-state on on-state hot carrier degradation was observed. Furthermore, stress sequences comprising of on-state and off-state pulse trains at low frequency 1kHz and 1MHz were analyzed, which will be compared to our analysis for 500MHz stress sequences later in Section 3.5.3. The recovery behavior during off-state stress after on-state pre-stress has been attributed to the neutralization of traps with a strong V_G dependence of on-state hot carrier pre-stress. This behavior was shown to decrease when the applied off-state pulse duration decreases, thus it is assumed that hole trapping becomes less effective at RF frequencies if stress duration is smaller than time constant of the trap. Recovery trend analysis was then extended to 8MHz in [25] using similar on and off-state stress patterns and confirmed the results observed at 1MHz in [3]. Following these observations, we present an interaction model analysis for on-state hot carrier and off-state stress sequences based on two different interaction modeling strategies demonstrated by [26], [27]. The models, derived from the parametric degradation Δ which obeys a time power law in eq.3-4, are described in equations 3-5 to 3-7 using two arbitrary stress sequences with stress durations t_1 and t_2 as illustrated in Figure 3-19 :

- Sum of age: The interaction between different stress modes is taken into consideration in a sequential order (history effect). The total defects generated at the end of the second stress sequence Δ_2 depend on the defects generated after the first sequence Δ_1, as shown in eq.3-5. This dependence is considered by the equivalent pre-stress time t_{eq} defined in eq.3-6. In the generalized case of $n=n_1=n_2$, eq.3-5 is equivalent to the AGE function.

- Sum of degradation: The different stress modes do not interact with each other. The defects generated by different stress modes are modeled independently (no matter the sequential order) as shown in eq.3-7.

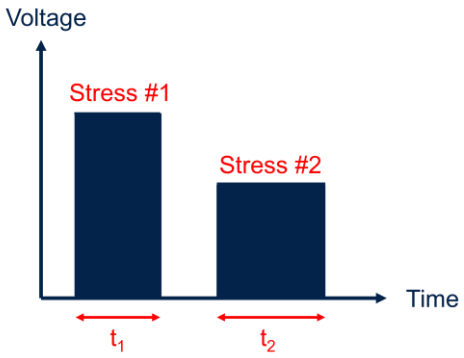

Figure 3-19 : Illustration of two arbitrary stress sequences 1 and 2 with their respective stress durations t_1 and t_2.

$$\Delta = A\,t^n \quad \text{(Eq.3-4)}$$

$$\Delta_{total\_age} = A_2\left(t_{eq} + t_2\right)^{n2} = \left(A_1^{1/n2} t_1^{n1/n2} + A_2^{1/n2} t_2\right)^{n2} \quad \text{(Eq.3-5)}$$

$$t_{eq} = \left(\frac{\Delta_1}{A_2}\right)^{1/n2} \quad \text{(Eq.3-6)}$$

$$\Delta_{total\_deg} = \Delta_1 + \Delta_2 = A_1 t_1^{n1} + A_2 t_2^{n2} \quad \text{(Eq.3-7)}$$

Among the two interaction models, the sum of age model (eq.3-5) provides a lower cumulative degradation than the sum of degradation model (eq.3-7), due to the n1/n2 exponent. Hence the interaction modeling strategy has a significant impact on the device lifetime estimations, especially in RF applications.

3.5.2 Stress conditions and methodology

We propose to study the on-state and off-state interactions through a combination of stress sequences comprising DC HCI on-state and DC/AC off-state stress applied on $DUT_{\text{Test Structure Drain}}$. Firstly, the stress conditions at T=125°C, shown in Table 3-4, for each on-state and off-state stress are determined to achieve ΔI_{Dlin} within 5% range. For the DC HCI on-state stress, DC stress voltage of 1.8V is applied using direct access to drain terminal V_{Drain} to bypass $R_{ONSwitch}$ of transmission gates while DC and AC off-state stress are applied via transmission gates at V_{HL} =2.2V. For each degradation mode, ΔI_{Dlin} was extracted without $R_{ONSwitch}$ and fitted to a time power law dependence model (eq.3-8) with a saturation component Δ_{max} using the fitting parameter values in Table 3-5.

$$\Delta = \frac{1}{\frac{1}{\Delta max} + \frac{1}{A \cdot t^n}} \quad \text{(Eq. 3-8)}$$

Table 3-4 : Stress conditions at T=125°C for on-state and off-state degradation modes applied on $DUT_{Test\ Structure\ Drain}$

Degradation mode / Stress conditions	DC HCI ON	DC OFF	AC OFF (F=500MHz)
V_{Gate}(V)	1.8	-1	-1
V_{Drain} (V); V_{HL} (V)	1.8 (V_{Drain})	2.2 (V_{HL})	2.2 (V_{HL})
Stress duration (s)	300	3000	6000

Table 3-5 : Time-power law model fit parameters for on-state and off-state degradation conditions corresponding to Table 3-4.

Degradation mode / Parameter	DC HCI ON	DC OFF	AC OFF
A	15.2E-4	4.2E-3	5.9E-3
n	0.71	0.31	0.55
Δ_{max}	0.16	1	0.015

The model fit shows that off-state degradation has a smaller degradation rate in contrast to on-state degradation, given by the smaller exponent n. It is important to remind here that the exponent n of AC off-state degradation is different than that of DC off-state degradation due to the stress waveform distortion that has been discussed previously in Section 3.2.2. The pre-stress and stress sequences in Table 3-6 are then applied at T=125°C, for which each stress sequence follows the stress-measurement-stress methodology. By using a total equivalent stress duration of 3.3ks, the final ΔI_{Dlin} is within acceptable range (<10%) without triggering device breakdown.

Table 3-6 : On-state and off-state modes combination for interaction model study

Stress sequence	Interaction mode 1	Interaction mode 2	Interaction mode 3	Interaction mode 4
Pre-stress	DC HCI ON	DC HCI ON	DC OFF	AC OFF
Stress	DC OFF	AC OFF	DC HCI ON	DC HCI ON
Pre-stress duration (s)	300	300	3000	6000
Stress duration (s)	3000	6000	300	300

3.5.3 Comparison of different interaction models against experimental results

Figure 3-20 shows ΔI_{Dlin} for the pre-stress DC HCI on-state and followed by DC/AC off-state stress (interaction modes 1 and 2). Experimental data is found to be well modeled by the sum of degradation of each mode, as opposed to the sum of age interaction model, indicating the absence of interaction between these two mechanisms. For comparison, ΔI_{Dlin} of the inverse stress sequences (interaction modes 3 and 4) are presented in Figure 3-21, with DC/AC off-state pre-stress which is then followed by DC HCI on-state stress. It is observed that both sum of degradation and sum of age models can fit final ΔI_{Dlin} of interaction modes 3 and 4. This is possibly due to the dominance of the DC HCI-on-state degradation compared to the pre-stress

degradation. ΔI_{Dlin} shows a slight recovery at the beginning of on-state stress for off-state HCI pre-stress. This could imply that the hot-hole induced defects originate from broken Si-H broken bonds as reported in Bravaix's work [1] instead of Si-O broken bonds which cause irreversible damage that was stated in Varghese's work [2]. We assume that this indicates the potential interaction between the two degradation modes in this specific order, also expected by the sum of age model data. The experimental results in Figure 3-20 showing zero recovery with on-state HCI pre-stress is different from the observations in [3] described earlier. Contrastingly, on-state HCI degradation with off-state pre-stress experimental data suggests the presence of recovery, which is not expected as reported by [3].

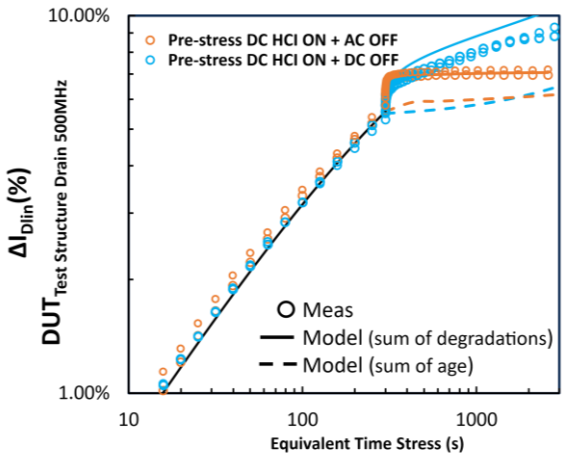

Figure 3-20 : ΔI_{Dlin} of interaction modes 1 (blue) and 2 (orange). Total ΔI_{Dlin} matches the sum of degradation model compared to sum of age.

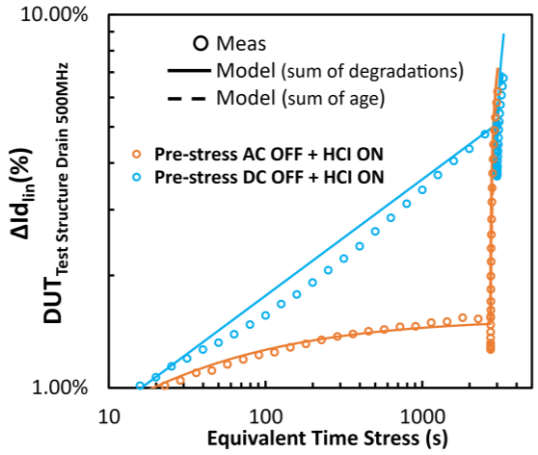

Figure 3-21 : ΔI_{Dlin} of interaction modes 3 (blue) and 4 (orange). Both models sum of degradation and sum of age are in good agreement with experimental data.

The interaction between degradation modes are linked to competition between occupation of defect creation sites [28], [29]. As the occupation of these sites depend on their species, localization, and density as well as carrier energy, it is difficult to obtain these defect characteristics solely through current-voltage (IV) measurements. To further understand the subject of interaction modes, the charge pumping technique [30], [31], [32] could be used in monitoring spatial and distribution of defect density.

In addition, a series of alternating DC HCI on-state and DC/AC off-state stress sequences, each with equivalent stress duration of 10s and 100s respectively for 30 cycles, are conducted to compare with the previous ΔI_{Dlin} results obtained in Figure 3-20 and Figure 3-21. As shown in Figure 3-22, the sum of degradation model is in good agreement with the experimental data. Interestingly, the final ΔI_{Dlin} of alternating DC HCI on-state to DC and AC off-state stress is the same as the final ΔI_{Dlin} of interaction modes 1 and 2 respectively (refer to Figure 3-20) given the same total stress duration. This result suggests that time kinetics of defect recovery depends on the off-state stress duration, which is consistent with the results reported in [25]. Thus interaction modeling of parametric degradation combining on-state HCI to off-state degradation is non-quasi static at high RF frequencies.

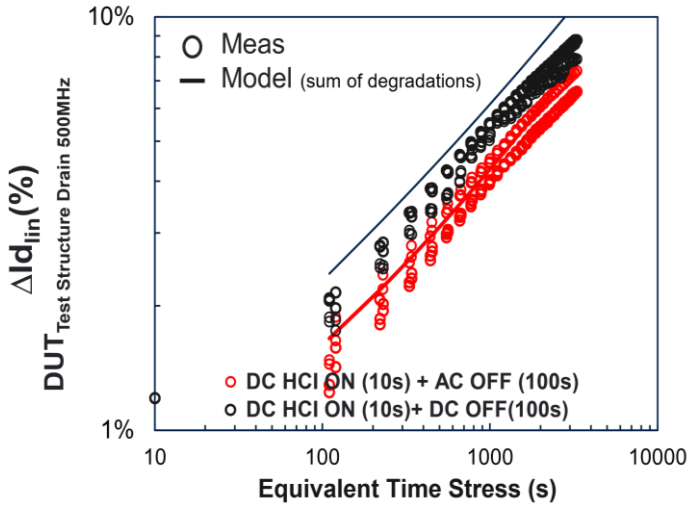

Figure 3-22 : ΔI_{Dlin} of alternating DC on-state HCI and DC/AC off-state stress sequences with total stress duration of 3.3ks. The sum of degradation model shows good agreement with measurement data.

Based on the comparison of the different interaction models, on-state to off-state interactions can be modeled by the sum of degradation model with good accuracy to experimental results. This modeling approach has low computational complexity and is also compatible with SPICE reliability simulation without large underestimation of device lifetime.

3.6 Conclusion

The test structure designed specifically for off-state reliability studies has been a key instrument to develop the understanding of frequency dependence at GHz level without compromising the integrity of the pulsed stress waveforms.

In terms of off-state RF TDDB, we have observed increasing T_{BD} at higher stress frequencies, particularly a gain factor of 2 at 1GHz stress compared to the DC stress, whereas β remains independent of stress frequency. The frequency power law TDDB model from on-state RF TDDB investigations in other works have been applied to the off-state case to extrapolate T_{BD} to mmW PA frequencies. This extrapolation offers significant advantage in design considerations for performance to reliability trade-offs. However, this model shows discrepancies at the lower frequency range 100kHz to 500MHz and additional experimental data is required to explain the observations. For future developments of off-state RF TDDB model, duty cycle and voltage acceleration dependencies should be explored to provide a complete model for RF/mmW reliability simulations.

Through the off-state stress measurements, degradation at 500MHz and 1GHz follows DC power law degradation curves, meaning that quasi-static modeling of parametric degradation is verified up to 1GHz. This important finding justifies the age modeling compatibility with current on-state modeling approach based on the age function in RF aging reliability simulations. We have proposed a few theories on the saturation behavior observed in RF off-state stress with increasing V_{GD} that should be confirmed by alternative defect characterization methods.

Based on our experimental observations obtained from RF off-state degradation, an interaction modeling study using the sum of age and sum of degradation models was compared against experimental data of on-state and off-state interaction sequences. The stress order analysis between the two degradation modes has led us to discover an asymmetric recovery in degradation, specifically in the case where on-state hot carrier degradation is preceded by off-state pre-stress. While the physical origins of this recovery are unclear and requires further investigations, it has been observed negligible at shorter pulse durations. The most important result from this study is that the experimental data using shorter off-state pulse duration (500MHz) converges towards sum of degradation model.

Following this modeling strategy and the quasi-static off-state degradation behavior, reliability models targeting RF applications should consider calibrating on-state and off-state aging models individually then consequently apply the sum of degradation model to estimate the total device degradation.

References

[1] A. Bravaix *et al.*, “Off state incorporation into the 3 energy mode device lifetime modeling for advanced 40nm CMOS node,” in *2010 IEEE International Reliability Physics Symposium*, May 2010, pp. 55–64. doi: 10.1109/IRPS.2010.5488852.

[2] D. Varghese *et al.*, “off-State Degradation in Drain-Extended NMOS Transistors: Interface Damage and Correlation to Dielectric Breakdown,” *IEEE Transactions on Electron Devices*, vol. 54, no. 10, pp. 2669–2678, Oct. 2007, doi: 10.1109/TED.2007.904587.

[3] T. Garba-Seybou, X. Federspiel, A. Bravaix, F. Cacho, and R. J. Monnet, “Analysis of the interactions of HCD under ‘On’ and ‘Off’ state modes for 28nm FDSOI AC RF modelling”.

[4] T. Garba-Seybou, X. Federspiel, A. Bravaix, and F. Cacho, “New Modelling Off-state TDDB for 130nm to 28nm CMOS nodes,” in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, p. 11A.3–1. doi: 10.1109/IRPS48227.2022.9764431.

[5] N.-H. Lee, D. Baek, and B. Kang, “Effect of off-State Stress and Drain Relaxation Voltage on Degradation of a Nanoscale nMOSFET at High Temperature,” *IEEE ELECTRON DEVICE LETTERS*, vol. 32, no. 7, 2011.

[6] A. Spessot *et al.*, “Impact of Off State Stress on advanced high-K metal gate NMOSFETs”.

[7] T. Garba-Seybou *et al.*, “Location of Oxide Breakdown Events under Off-state TDDB in 28nm N-MOSFETs dedicated to RF applications,” in *2023 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2023, pp. 1–8. doi: 10.1109/IRPS48203.2023.10117725.

[8] A. Bravaix, E. Kussener, D. Ney, X. Federspiel, and F. Cacho, “Hot-Carrier induced Breakdown events from Off to On mode in NEDMOS”.

[9] J. Kim, N. Lee, G.-J. Kim, Y.-Y. Lee, J. Seok, and Y. Lee, “Effect of OFF-state stress on reliability of nMOSFET in SWD circuits of DRAM,” *Microelectronics Reliability*, vol. 88–90, pp. 183–185, Sep. 2018, doi: 10.1016/j.microrel.2018.06.101.

[10] J. Trommer *et al.*, “Off-state Impact on FDSOI Ring Oscillator Degradation under High Voltage Stress,” in *2018 International Integrated Reliability Workshop (IIRW)*, Oct. 2018, pp. 1–5. doi: 10.1109/IIRW.2018.8727101.

[11] S. Kupke *et al.*, “Experimental Proof of the Drain-Side Dielectric Breakdown of HKMG nMOSFETs Under Logic Circuit Operation,” *IEEE ELECTRON DEVICE LETTERS*, vol. 36, no. 5, 2015.

[12] R. Fernández-García, B. Kaczer, and G. Groeseneken, “A CMOS circuit for evaluating the NBTI over a wide frequency range,” *Microelectronics Reliability*, vol. 49, no. 8, pp. 885–891, Aug. 2009, doi: 10.1016/j.microrel.2009.05.009.

[13] M. Arabi *et al.*, “New Insights on Device Level TDDB at GHz Speed in Advanced CMOS Nodes,” *IEEE Transactions on Device and Materials Reliability*, vol. 19, no. 2, pp. 255–261, Jun. 2019, doi: 10.1109/TDMR.2019.2914362.

[14] W. Liu, E. Salman, C. Sitik, and B. Taskin, “Enhanced level shifter for multi-voltage operation,” in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 1442–1445. doi: 10.1109/ISCAS.2015.7168915.

[15] D. Varghese *et al.*, “Multi-probe Two-Dimensional Mapping of Off-State Degradation in DeNMOS Transistors: How and Why Interface Damage Predicts Gate Dielectric Breakdown,” in *2007 IEEE International Electron Devices Meeting*, Dec. 2007, pp. 505–508. doi: 10.1109/IEDM.2007.4418985.

[16] G. T. Sasse, “MOSFET Degradation Under RF Stress,” *IEEE TRANSACTIONS ON ELECTRON DEVICES*, vol. 55, no. 11, 2008.
[17] X. Garros *et al.*, “A Very Robust and Reliable 2.7GHz +31dBm Si RFSOI Transistor for Power Amplifier Solutions,” in *2019 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2019, p. 25.5.1-25.5.4. doi: 10.1109/IEDM19573.2019.8993649.
[18] A. Divay *et al.*, “65nm RFSOI Power Amplifier Transistor Ageing at mm W frequencies, 14 GHz and 28 GHz,” in *2021 IEEE International Electron Devices Meeting (IEDM)*, 2021, p. 39.3.1-39.3.4. doi: 10.1109/IEDM19574.2021.9720531.
[19] P. Asbeck, S. Alluri, N. Rostomyan, and J. A. Jayamon, “Reliability of CMOS-SOI power amplifiers for millimeter-wave 5G: the case for pMOS (Invited),” in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, p. 4B.1–1. doi: 10.1109/IRPS48227.2022.9764417.
[20] L. Larcher, D. Sanzogni, R. Brama, A. Mazzanti, and F. Svelto, “Oxide Breakdown After RF Stress: Experimental Analysis and Effects on Power Amplifier Operation,” in *2006 IEEE International Reliability Physics Symposium Proceedings*, Mar. 2006, pp. 283–288. doi: 10.1109/RELPHY.2006.251229.
[21] M. Arabi, M. Rafik, X. Federspiel, and G. Ghibaudo, “A New Direct Measurement Method of Time Dependent Dielectric Breakdown at High Frequency”.
[22] M. Arabi *et al.*, “Frequency dependant gate oxide TDDB model,” in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, pp. P25-1. doi: 10.1109/IRPS48227.2022.9764503.
[23] J. W. McPherson, “Physical model for the frequency dependence of time-dependent dielectric breakdown (TDDB),” *AIP Advances*, vol. 13, no. 5, p. 055217, May 2023, doi: 10.1063/5.0150268.
[24] N.-H. Lee, D. Baek, and B. Kang, “Effect of off-State Stress and Drain Relaxation Voltage on Degradation of a Nanoscale nMOSFET at High Temperature,” *IEEE ELECTRON DEVICE LETTERS*, vol. 32, no. 7, 2011.
[25] T. Garba-Seybou, A. Bravaix, X. Federspiel, and F. Cacho, “Modeling hot carrier damage interaction between on and off modes for 28 nm AC RF applications,” *Microelectronics Reliability*, vol. 126, p. 114342, Nov. 2021, doi: 10.1016/j.microrel.2021.114342.
[26] W. Arfaoui, X. Federspiel, P. Mora, M. Rafik, D. Roy, and A. Bravaix, “Experimental analysis of defect nature and localization under hot-carrier and bias temperature damage in advanced CMOS nodes,” in *2013 IEEE International Integrated Reliability Workshop Final Report*, Oct. 2013, pp. 78–83. doi: 10.1109/IIRW.2013.6804163.
[27] X. Federspiel, F. Cacho, and D. Roy, “Experimental characterization of the interactions between HCI, off-state and BTI degradation modes,” 2011.
[28] F. Cacho, P. Mora, W. Arfaoui, X. Federspiel, and V. Huard, “HCI/BTI coupled model: The path for accurate and predictive reliability simulations,” in *2014 IEEE International Reliability Physics Symposium*, Jun. 2014, p. 5D.4.1-5D.4.5. doi: 10.1109/IRPS.2014.6860673.
[29] X. Federspiel, F. Cacho, and D. Roy, “Experimental characterization of the interactions between HCI, off-state and BTI degradation modes,” 2011.
[30] D. Varghese, S. Mahapatra, and M. A. Alam, “Hole energy dependent interface trap generation in MOSFET Si/SiO/sub 2/ interface,” *IEEE Electron Device Letters*, vol. 26, pp. 572–574, 2005.
[31] S. Mahapatra, C. D. Parikh, V. R. Rao, C. R. Viswanathan, and J. Vasi, “Device scaling effects on hot-carrier induced interface and oxide-trapped charge distributions in MOSFETs,” *IEEE Transactions on Electron Devices*, vol. 47, no. 4, pp. 789–796, Apr. 2000, doi: 10.1109/16.830995.

[32] G. T. Sasse and J. Schmitz, “Application and Evaluation of the RF Charge-Pumping Technique,” *IEEE Transactions on Electron Devices*, vol. 55, no. 3, pp. 881–889, Mar. 2008, doi: 10.1109/TED.2007.915088

4. RF PA HCI Aging compensation strategy in 28nm UTBB FDSOI technology

Presently, our aging studies on RF PA emphasize the modeling of RF degradation to obtain accurate device lifetime estimation. The RF aging modeling approach is critical in the early design cycle to deliver a risk assessment of the device's mission profile with regards to the reliability target. Another concept that can bridge the gap between the performance and reliability trade-off is the compensation of the device or circuit aging. In this chapter, the proof of concept of an automatic gain compensation technique to control aging effect on RF PA performance variation is demonstrated. It has been demonstrated in chapter 2 that V_T degradation is one of the parameters that significantly contributes to the gain degradation of a class AB PA during RF HCI stress. As a consequence, the proposed compensation scheme aims to compensate V_T degradation induced by RF HCI aging via the adjustment of the body bias voltage, a technique that is widely known as adaptive body biasing. In the following sections we will give a brief review of the known aging compensation techniques in RF PA applications. After analyzing the advantages and drawbacks of these previous works, a system level description of the continuous gain compensation flow is given based on the RF HCI aging behavior of the PA device. The design of the building blocks is then presented following the requirements of the compensation strategy. Finally, the simulation results of the different RF HCI degradation scenarios are illustrated and discussed.

4.1 RF Aging compensation strategy using adaptive bias technique

4.1.1 Adaptive bias compensation: techniques, performance gain and reliability considerations

4.1.1.1 Overview of adaptive bias techniques for RF PA reliability

Adaptive bias is one of the strategies implemented in reliability-aware design to compensate the degradation effects on circuit performance. The main feature of this technique is to dynamically adjust the bias voltage of the device/circuit based on the degradation level to recover its operating point. Several techniques focusing on the design of adaptive bias to address DC parametric degradation in PA RF HCI aging have been proposed in the literature, such as adaptive gate bias [1]–[3] and adaptive body bias [4]. Adaptive body bias schemes have the advantage of providing finer control on the V_T compensation. However, in terms of physical layout, adaptive gate bias schemes are easier to implement as they do not require the extra area overhead in well isolation structures, which are needed for body-bias applications.

In general, an adaptive bias circuit for aging compensation requires two functions, the detection of the related device aging parameter (voltage, current or power) followed by the

compensation of the bias voltage via gate or body terminal. The solutions proposed by [1], [2], [3] use DC voltage or DC current detectors to sense the drift in bias operating point. The design in [4] uses an RF power detector to sense the PA output power drift, which makes this a viable solution since the bias compensation is correlated to the RF degradation. Most importantly, the RF signal path must not be compromised by the loading of the detection circuit.

4.1.1.2 Performance and reliability of body-bias effect in UTBB 28nm FDSOI devices

The body-biasing technique is widely employed in analog and digital applications to boost performance, optimize power management and compensate PVT variations. The V_T modulation is controlled by applying a forward body-bias (FBB) and reverse body-bias (RBB) voltage to lower and increase the effective V_T respectively. FDSOI devices with ultra-thin body and buried-oxide (UTBB) offer a higher body biasing efficiency through its back-gate terminal, i.e., 85mV/V in contrast to substrate body biasing 25mV/V in bulk-Si devices, resulting in a larger V_T modulation to increase I_{ON}/I_{OFF} ratio in FBB mode thus reducing power consumption (higher I_{ON} for the same V_{DD}) [5], [6], [7].

From an NMOS reliability perspective, hot-carrier degradation of FDSOI devices share similarities in degradation dynamics as bulk-Si devices, i.e. time-power law with exponent of 0.3 for I_{DSAT} drift under worst case HCI stress $V_G=V_D$ [8]. Previous work in [9], [10] have reported higher I_{DSAT} drift in $V_G=V_D$ stress coupled with FBB stress while no significant influence on damage localization. Considering that the higher I_{DSAT} drift can be explained by a higher carrier density and lower pinch-off voltage in presence of FBB, the authors in [11], [12] demonstrated as shown in Figure 4-1 , that the degradation is less significant with FBB than without FBB for the same carrier density. In other words, it can be expected that adaptive body-bias via FBB improves device HCI reliability while providing the performance benefits that the FDSOI technology has to offer.

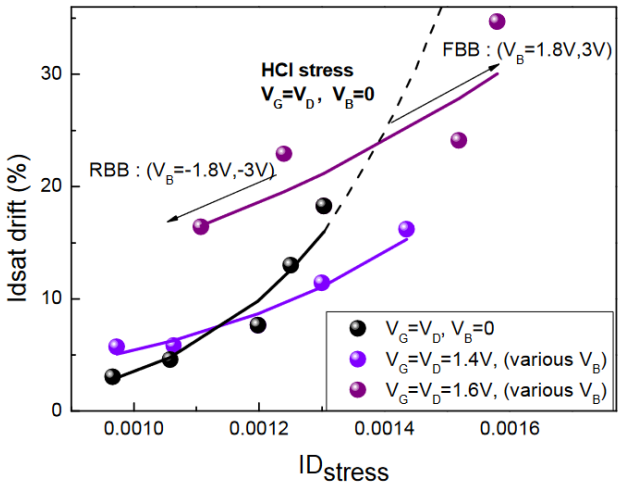

Figure 4-1: I_{Dsat} drift is plotted against the respective carrier density of different FBB/RBB stress in 28FDSOI NMOS LVT devices [11].

4.2 Proposed test structure design methodology in UTBB 28FDSOI technology platform

4.2.1 System level description

4.2.1.1 Conceptualization: Adaptive body biasing for PA gain compensation

Firstly, the concept of adaptive body bias via FBB on the designed NMOS LVT PA cell is analyzed. In the case of an NMOS transistor in inversion mode, when V_{FBB} is increased, V_T decreases and thus increasing the drain current as the overdrive voltage is increased. The V_T modulation effect, which is inversely proportional to V_{BB} (Figure 4-2), is illustrated in Figure 4-3 where the drain current is plotted as a function of gate voltage for a range of body bias V_{BB} values. In 28FDSOI process, the LVT devices are implemented in flipped-well configuration in favor of F_{BB} which emphasizes V_T reduction. Consequently, RBB (V_{BB}<0) is limited at -300mV for the NMOS transistor to prevent the n-well/p-well junction forward biasing [5], [6].

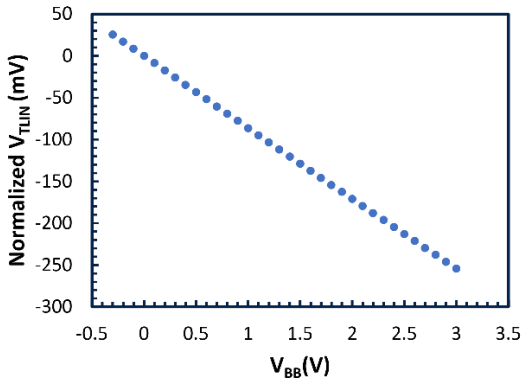

Figure 4-2: V_T modulation range from -250mV to 30mV. The maximum value is limited by VBB=-300mV to avoid leakage through forward biasing of p-n junction

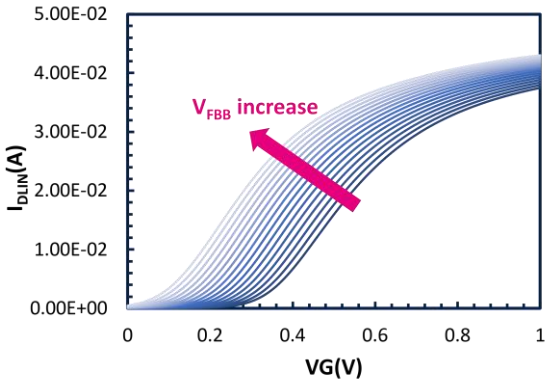

Figure 4-3: Linear IDVG curves of LVT NMOS PA cell showing lower V_T and higher drive current by increasing V_{FBB} (V_{BB}>0)

As the drain current and the overdrive voltage are directly related to the transconductance (gm) which determines the small-signal gain, the impact of V_T modulation on RF PA figure of merits is analyzed in Figure 4-4(a), (b) and (c). The increase of V_{FBB} shifts the PA gain towards higher values, as the bias operating point move towards large PA conduction angles (class A), that can be observed by the increase in DC bias current. Since V_{DD} bias remains constant, the PAE is penalized when approaching higher output power with increasing V_{FBB} higher power consumption when the conduction angle is increased.

From the HCI sensitivity analysis presented in section 2.3, we have observed that RF gain degradation induced by RF aging is mainly contributed by the DC drift of several device parameter such as V_T, mobility and R_D. Therefore, in this work, we propose to study the effect of V_T compensation on RF PA aging by implementing a feedback control loop to adjust FBB.

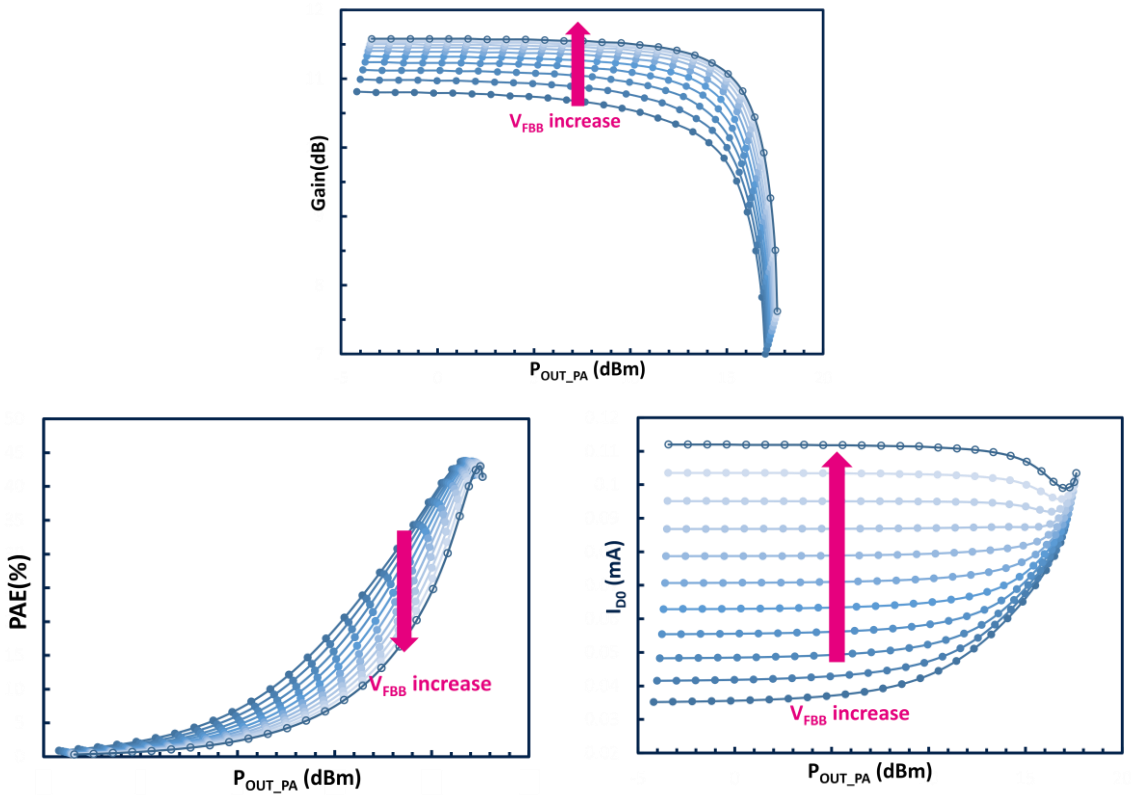

Figure 4-4: Effect of VFBB increase on the following RF PA figure of merits (a) Gain vs Pout, (b) PAE vs Pout, (c) DC bias current vs Pout

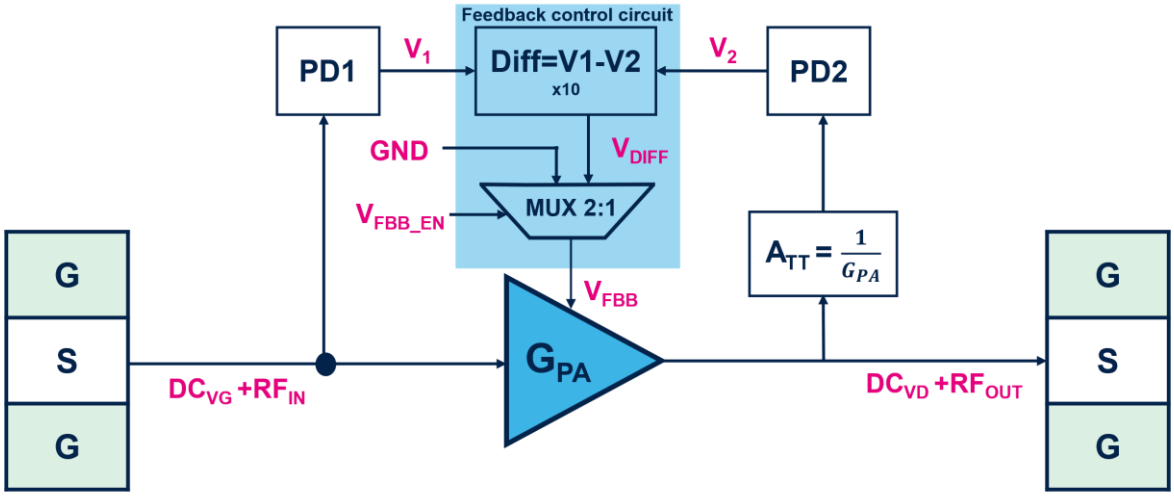

Figure 4-5 : Block diagram of PA compensation feedback system consisting of attenuator (ATT), power detectors (PD1/PD2), and a feedback control circuit. Back-gate terminal of the PA cell receives the voltage difference between PD1 and PD2 during closed-loop while it is connected to 0V (GND) in open-loop.

Figure 4-5 illustrates the block diagram of the system composed of an RF PA cell and a negative feedback loop integrating the following three main blocks: an attenuator (A_{TT}), power detectors (PD1 and PD2), and a feedback control circuit. At fresh condition, V_{DIFF} =0 due to the fact that gain compensation is not needed. To obtain this condition, the attenuator A_{TT} is designed to cancel the gain of the PA at a fixed RF output power, i.e., P_{1dB}, so that both inputs of the feedback circuit V1 and V2 are equal. After RF stress, with PA gain degradation and the fixed attenuation of A_{TT}, V2 decreases. This results in V1-V2>0 and thus V_{DIFF}>0 is required to compensate for V_T degradation. Here, the power detectors PD1 and PD2 are used

to detect the PA input power and the attenuated output power and convert them into DC output level. It is important to ensure that the RF signal path from the PA input to output is isolated from the loading effect of the attenuator and power detectors so that the PA gain is unaffected. The integrated feedback control circuit not only calculates the difference between the reference DC level (V1) and the regulated DC level (V2) but also provides the appropriate VFBB. A switch is used to break or close the feedback loop, by applying GND or V_{DIFF} respectively to VFBB. This feature adds a degree of freedom to apply compensation in continuous or discrete mode. The design of the different building blocks will be discussed later in section 4.2.2.

In comparison to [4], our proposed method has higher efficiency in applying the feedback control for gain compensation. It should be noted that this compensation technique addresses the recovery of the output amplitude but not the phase recovery, with the latter related to the input capacitance degradation of the device [13]. Since the output of the feedback loop only controls VFBB to compensate V_T drift, it is expected that the PA gain is not able to be fully compensated during RF HCI aging due to the presence of other DC degradation parameter, in particular the R_{DSAT} drift contribution. This solution can be coupled with a supply voltage regulator to regulate the voltage drop induced by R_{DSAT} drift.

4.2.2 Block level design

4.2.2.1 28GHz RF Power amplifier

To demonstrate our proposed solution, a PA is designed to operate at 28GHw with approximatively 10dB RF gain and P_{SAT} of 12.5dBm. The design is implemented in STMicroelectronics 28nm FDSOI process design kit (that is different from the previous 28GHz PA studied in chapter 2 due to the tapeout constraints). The PA cell is composed of a LVT NMOS transistor in common source configuration with channel width W=400µm and length L=30nm. A multi-finger geometry layout is chosen using gate finger width W_F=2.5µm for a total of 160 fingers to reduce the physical layout of the PA cell and optimize the gate resistance and capacitance parasitic. The first step in the design process consists in selecting the required output load impedance R_L to deliver an output saturation power P_{SAT}=12.5dBm=17.7mW, that can be approximated using eq.4-1 for V_{DD}=1.1V.

$$R_L = \frac{(V_{DD} - V_{DSAT})^2}{2 \cdot P_{SAT}} \quad \text{(Eq.4-1)}$$

The DC load line theory is then applied to determine the DC bias operating point of the PA with R_L=15Ω and V_{DD}=1.1V from the I_DV_D curves as shown in Figure 4-6. The DC load line is described by the relationship between V_{DS} and I_D where the slope of the load line is proportional to $-1/R_L$ and α represents the coefficient of different PA classes. The intercept point at V_{DS}=0 represents the maximum drain current I_{DMAX} that can be driven by the PA. On the other hand, the intercept point at I_D=0 represents the maximum drain voltage swing $V_{DS}(t)$ which is dependent on input gate voltage swing $V_{GS}(t)$. As we have chosen class AB operation in previous RF HCI aging studies, the same operation class will be implemented

here thus the drain bias current I_{D0} is fixed at 34mA at V_{GBIAS}=0.4V between the I_{D0} values of class A and class B.

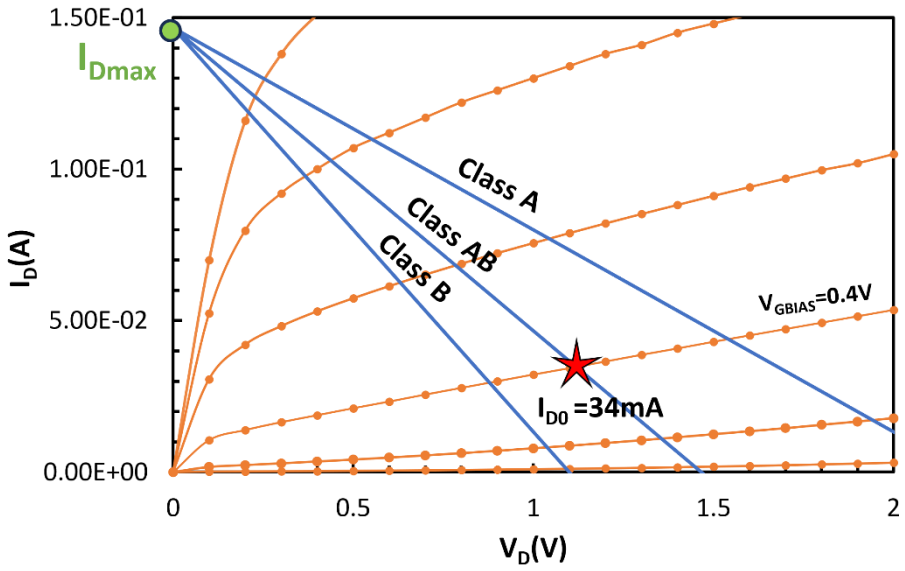

Figure 4-6: DC load line analysis of PA cell. Class AB operating point is fixed at I_{D0}=34mA for V_{DD}=1.1V.

Large-signal performance is analyzed by conducting load and source pull SPICE simulations in search of optimal ZS and ZL values to obtain maximum power gain at fundamental frequency. This is initially performed for ideal PA model and then adjusted to recover insertion loss introduced by post-layout, back-end routing, and RF pad parasitic extractions. The large-signal SPICE simulations at 28GHz were implemented by Cadence SpectreRF simulator using an RF testbench which is similar to that already presented in Chapter 2. As observed in the simulation results of Figure 4-7, a significant reduction of RF gain is observed for the PA core model combined with post-layout and pad parasitic effects

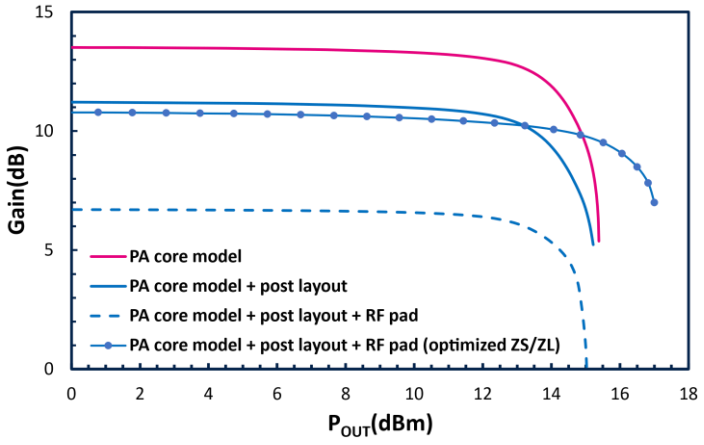

Figure 4-7: RF PA gain at different extraction levels. The PA core model gain is reduced by post-layout and RF pad parasitics. ZS and ZL are then optimized to readjust the gain level in consideration of load pull setup capability.

compared to the PA core model only. To reach the gain range specification for the feedback circuit, the RF gain is then increased to 10.5dB by optimizing ZS=10+j2.85 and ZL=10.7+j4.176. The RF gain level is important for the attenuator in the feedback path to effectively cancel the gain=9.5dB at P_{OUT}=P_{1dB}. Another important point which needs to be

considered when optimizing ZS and ZL is the impedance tuning range on load pull setup that in particular limits the value of the real part of ZS and ZL. The optimized ZS and ZL values is implemented in the simulation of the PA aging compensation system in section 4.3.

4.2.2.2 Attenuator

The role of the attenuator A_{TT} at the PA output is to provide a voltage attenuation (equivalent to the P_{1dB} gain) with minimal disruption on the RF signal path to the output load. A simple attenuator can be designed by using passive elements, either resistive or capacitive. Here, we choose to use a large resistive attenuator (>>50 Ω) instead of a capacitive attenuator so that the output impedance of the PA remains unchanged. Figure 4-8 shows an attenuator consisting of a single resistor with a large resistance value R_{ATT}=3.3kΩ. The input terminal is connected to the PA output (drain) while the output terminal is connected to the DC blocking capacitor of the power detector input. The attenuation level is given by the ratio between the output and input voltage of the attenuator. For our study, the attenuation is fixed at 9.5dB (PA gain at P_{1dB}) by R_{ATT}.

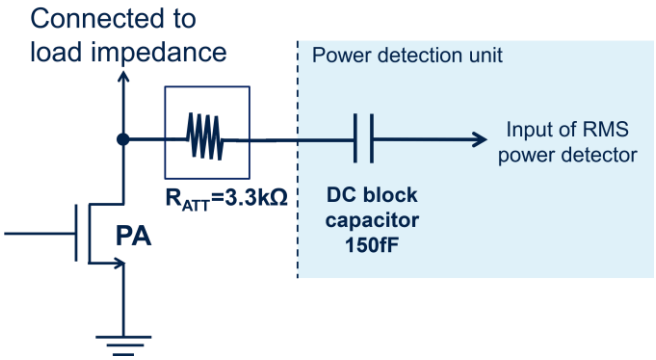

Figure 4-8 : Resistive attenuator to provide PA gain cancellation at P1dB. A small capacitor placed at the power detector input is used to block the DC bias of the RF output signal.

4.2.2.3 Power detector

RF power detection is one of the key functions in the gain compensation system as they are required both at the input and output of the PA cell to provide RF power level measurements. For RF or microwave power measurements, there are two categories of power detectors in terms of the type of measured power: peak detectors [14], [15] and root-mean square (RMS) detectors [16], [17]. An important question before embarking on power detector design is to find out whether peak or RMS power is representative of PA degradation. A qualitative analysis is conducted to assess the correlation between V_T degradation against RMS and peak output power during PA stress, as illustrated in Figure 4-9. The RMS output power shows a smaller slope for the same V_T degradation, which means a smaller input dynamic range for RMS power detection compared to peak power detection. This provides an advantage to relax the dynamic range constraints when designing the power detector. Besides its viability for this study, the fact that RMS power detectors measure the average power makes them less susceptible to any fluctuations to the detected signal compared to peak detectors, thus producing a more robust measurement result.

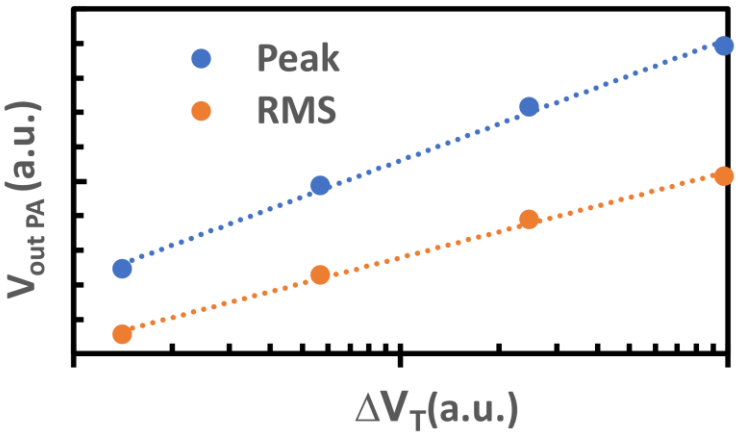

Figure 4-9: Qualitative analysis to study the relation between peak/RMS output power and V_T degradation due to RF HCI aging

An RMS detector performs two distinct functions to obtain the RMS value of an AC signal (V_{RMS}), squaring and averaging [18], as described by eq.4-2 where $V_{AC}(t)$ is the instantaneous voltage of an AC signal of periodicity T. It should be noted that V_{RMS} is a DC signal.

$$V_{RMS} = \sqrt{\frac{1}{T}\int_0^T V_{AC}(t)} = \sqrt{avg(V_{AC}^2)} \qquad \text{(Eq.4-2)}$$

The square-law characteristics of a MOS transistor in strong inversion region is a well-known RMS detection method, where the drain current of the MOS is proportional to the square of the gate voltage that is represented by the amplitude of $V_{AC}(t)$. The output is then low pass filtered to obtain the RMS value of V_{AC}. The main benefits of this method are its high dynamic range, low complexity and on-chip integration in standard CMOS technology compared to diode or bipolar transistor detectors.

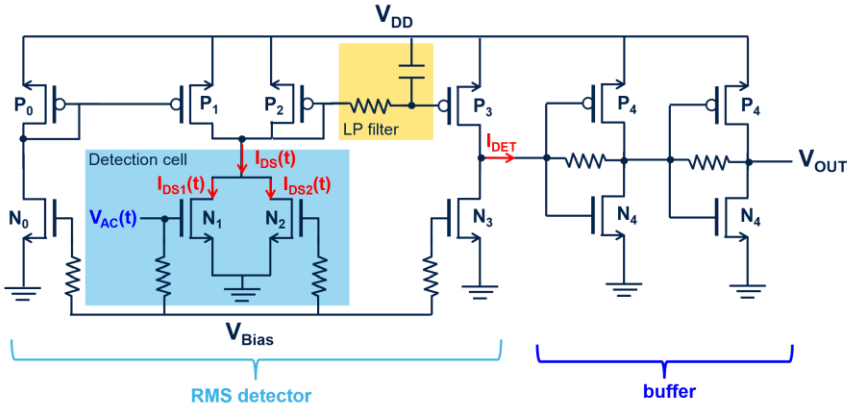

Figure 4-10 : Schematic design of RF power detection unit which consists of a RMS detector and a buffer [17]

We have implemented the design of a 28GHz RF power detection unit consisting of RMS detector and a buffer in 28FDSOI technology based on the design of a 60GHz power detector in [17]. As presented in Figure 4-10, the detection cell uses a differential input instead of a single-ended input to provide a higher immunity against offset errors due to process, voltage, and temperature (PVT) variations. Both N1 and N2 transistors are designed with minimum

width to obtain large input impedances, thus minimizing the signal leakage on the RF PA signal path. The biasing circuit (N0, N3, P1, P2, P3) is built using current mirrors to provide the required bias current for the detection cell. For more details on the sizing of transistors in the biasing circuit, readers can refer to [17].

Considering that the instantaneous RF signal $V_{AC}(t)$, of a frequency $F_0 = \frac{\omega_0}{2\pi}$, injected at the gate terminal of N_1 (given by eq.4-3) while the gate terminal of N_2 is kept constant. The DC bias points of N1 and N_2 are fixed such that the transistors operate in saturation mode to perform instantaneous to RMS voltage conversion, thus the drain currents of N_1 and N_2, I_{DS1} and I_{DS2}, are given by eq.4-4 and eq.4-5:

$$V_{AC}(t) = V_{GS\_bias} + V_{AC}\cos(\omega_0 t) \quad \text{(Eq.4-3)}$$

$$I_{DS1}(t) \propto \frac{K \cdot W}{2 \cdot L}(V_{AC}(t) - V_T)^2 \quad \text{(Eq.4-4)}$$

$$I_{DS2} \propto \frac{K \cdot W}{2 \cdot L}(V_{GS\_bias} - V_T)^2 \quad \text{(Eq.4-5)}$$

The total drain current I_{DS} which is the sum of I_{DS1} and I_{DS2}, contains the amplitude of $V_{AC}(t)$ and components of the first and 2nd order harmonics, F_0 and $2F_0$ (refer to eq.4-6). By using the RC low-pass filter with a cut-off frequency $F_C \ll F_0$ to remove the harmonic components, a DC current output I_{DET} linearly proportional to the square of the amplitude of $V_{AC}(t)$ is acquired, as illustrated by the simulation results at 28GHz in Figure 4-11. The transfer function characteristic is linear for an equivalent input power of -25dBm to -5dBm.

$$I_{DS}(t) \propto {V_{AC}}^2 + V_{AC}\cos(\omega_0 t) + (V_{AC}\cos(2\omega_0 t))^2 \quad \text{(Eq.4-6)}$$

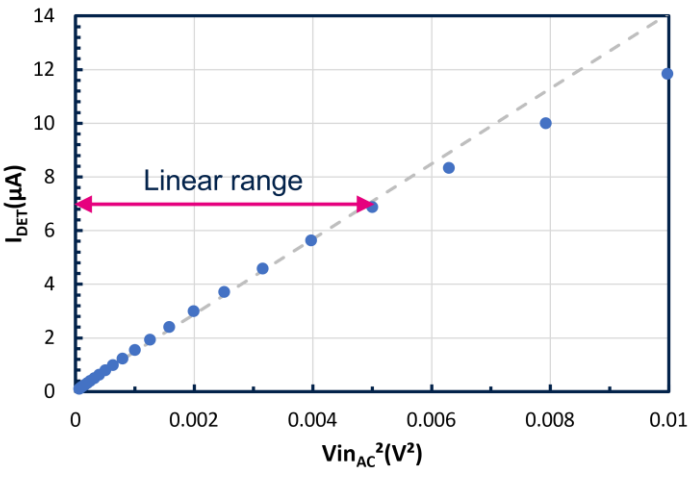

Figure 4-11: Transfer function of RMS detector. A linear detection range is defined for an equivalent input power Pin=-25dBm to -5dBm

A buffer stage, which is connected to the detector output, is essential for several reasons. Firstly, since the useful signal of the detector output I_{DET} is too weak to drive a load to be able to provide a large enough sense voltage for the subsequent stage, thus a buffer can act as a current to voltage converter. Secondly, a low impedance input of the subsequent stage is

necessary to conserve the signal integrity of I_{DET}. These issues can be solved by the implementation of a transimpedance amplifier (TIA) consisting of two cascaded resistive-feedback inverters as presented in Figure 4-10. The TIA gain is given by the feedback resistor so that the TIA output voltage is proportional to the amplified input current [19]. The transfer function of power detection unit at 28GHz is shown in Figure 4-12 using semi-log plot of the detected output RF voltage V_{OUT} against the input power Pin. A dynamic range of 20dB is obtained. Minimum dynamic range is limited by noise level of the input differential stage, whereas the maximum dynamic range is limited by the overdrive voltage (V_G-V_T) of the N1 and N2 transistors to keep them in saturation mode.

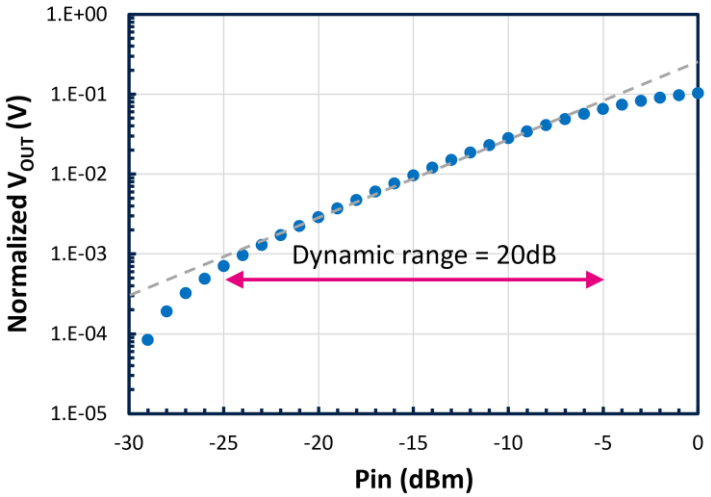

Figure 4-12 : Semi-log plot of the normalized detector output voltage against the injected input power. A linear dynamic range of 20dB is obtained. The minimum level is limited by the noise level of the detector input whereas the maximum level is defined by the maximum drain voltage swing of the input stage.

The functionality of the power detection unit in the feedback system is evaluated together with the PA cell and attenuator. By recalling the feedback system characteristics, the input and attenuated output power of the PA should be equal so that the voltage difference between the output of the two power detectors, V_{OUT_PD1}-V_{OUT_PD2}, is zero. The transfer characteristics obtained from post-layout simulation of the power detectors at the input of the PA (PD1) and the attenuated output of the PA (PD2) is presented in Figure 4-13(a) and (b). At low PA input power (Pin_{PA}), the voltage output of both PD1 and PD2 are identical due to the gain attenuation provided by R_{ATT}. As Pin_{PA} increases, the difference V_{OUT_PD1}-V_{OUT_PD2} increases, implying that V_{FBB}>0V. However, we expected that V_{FBB} remains at 0V up to P_{1dB} (Pin_{PA}= 5dBm) in fresh PA condition. To ensure this configuration, it is possible to correct this error during the calibration phase (refer to section 4.3.1). In the case of RF HCI degradation for PA aging, the V_{OUT_PD1}-V_{OUT_PD2} characteristics will be shifted vertically.

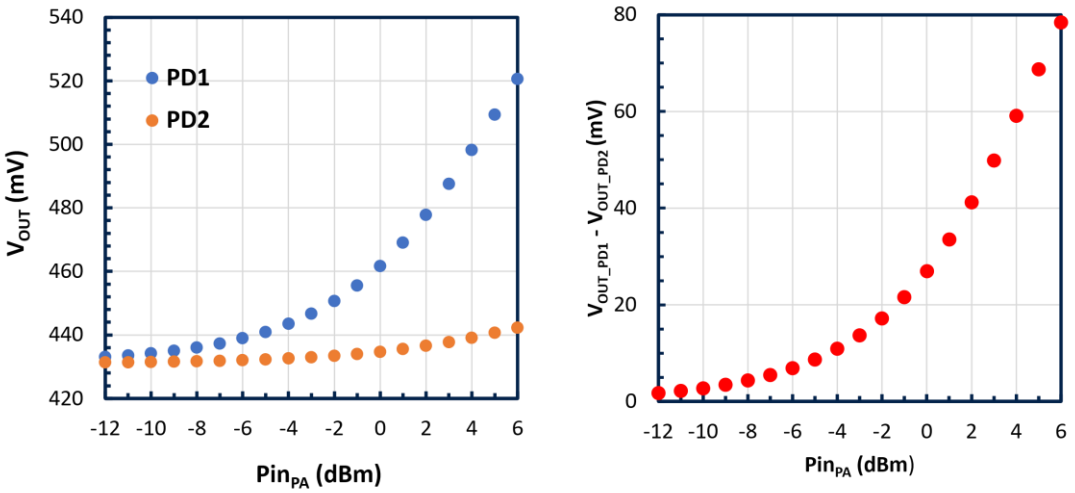

Figure 4-13 : left (a) Linear plot of the transfer function of power detectors PD1 and PD2. Right (b) The V_{OUT_PD1}-V_{OUT_PD2} characteristics which is proportional to the VFBB feedback control.

4.2.2.4 Feedback control circuit

The core of the feedback control circuit is made up of a differential amplifier shown in Figure 4-14, with V_{PLUS} and V_{MINUS} representing V_{OUT_PD1} and V_{OUT_PD2} respectively. The differential amplifier is designed using two differential input operational amplifiers (consisting of thick oxide transistors) that are connected to dual supply voltage $+V_{DD2}$=2.5V and $-V_{DD2}$=-2.5V. This cascaded configuration provides a high input impedance that is suitable for unbalanced voltage inputs. The output voltage of the differential amplifier (V_{OUT_DIFF}) is given by the voltage difference between V_{PLUS} and V_{MINUS}, amplified by a voltage gain G_V as described in eq.4-7 and eq.4-8.

$$G_V = 1 + \frac{R2}{R1} \qquad \text{(Eq.4-7)}$$

$$V_{VOUT\_DIFF} = (V_{PLUS} - V_{MINUS}) \cdot \left(1 + \frac{R2}{R1}\right) + V_{CAL} \qquad \text{(Eq.4-8)}$$

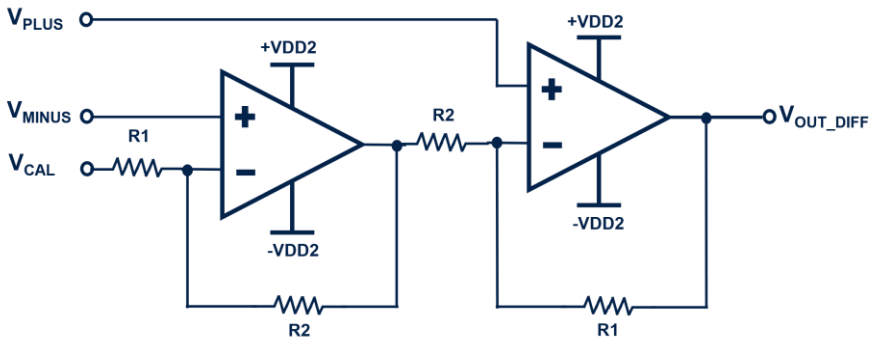

Figure 4-14 : Schematic design of the differential amplifier using differential input single-ended output operational amplifiers in cascaded configuration

By applying V_{CAL} which is generated from an external voltage supply, an offset voltage (positive or negative value) is applied to V_{OUT_DIFF} thus serving as a tuning knob to

calibrate the mismatch collectively produced by different components in the feedback chain as well as the differential amplifier itself. The transfer function of V_{OUT_DIFF} remains linear within the range of -2.3V to 2.2V for the differential input amplitude V_{PLUS} - V_{MINUS} of 450mV as illustrated in Figure 4-15, which is compatible with the output range of V_{OUT_PD1}-V_{OUT_PD2} (refer to Figure 4-13(b)) and also fits in the gain compensation range using VFBB (refer to section 4.3).

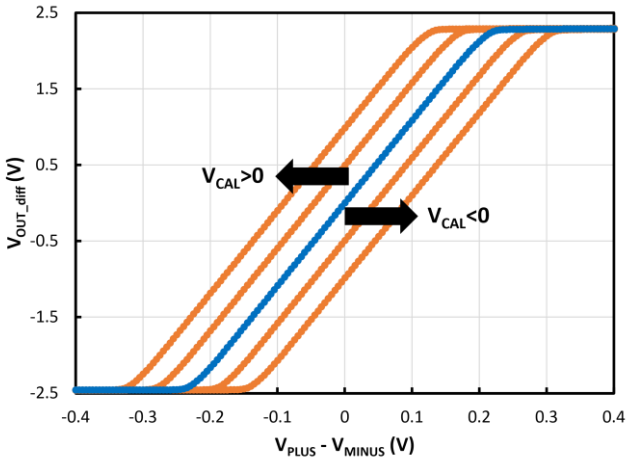

Figure 4-15: Transfer function of the differential amplifier in differential mode. The output range remains linear within the voltage range of VFBB for gain compensation. The corresponding input range is compatible with the previous stage output range.

Since there is no feedback path within the differential amplifier itself, the stability analysis can be performed individually on each operational amplifier by simulating its gain and phase margin. The operational amplifier is stable with a phase margin of 70 degrees, which is higher than the recommended stability margins to avoid amplifier output oscillations.

The feedback path connecting the differential amplifier output and the back-gate terminal of the PA cell can be open or closed using a pass gate (PG1) as a switch. The loop is controlled by the enable signal V_{FBB_EN}, such that the output of PG1 (V_{OUT_PG1}) applies 0V (GND) during open loop and V_{OUT_DIFF} during close-loop respectively to the PA back-gate terminal. To observe V_{OUT_DIFF} in either loop state (open or closed) and due to the limited number of DC probe pads, another pass gate (PG2) is implemented. PG2 provides the read-out of different signals on the same DC probe pad. The output of PG2 (V_{OUT_PG2}) corresponds to V_{OUT_DIFF} during open-loop (essentially for calibration step) while during close-loop V_{OUT_PG2} corresponds to the intrinsic voltage of the PA drain terminal (V_{D_SENSE}). The role of the different pass gates PG1 and PG2 is illustrated in Figure 4-16. The different outputs during open and close loop are presented in Table 4-1.

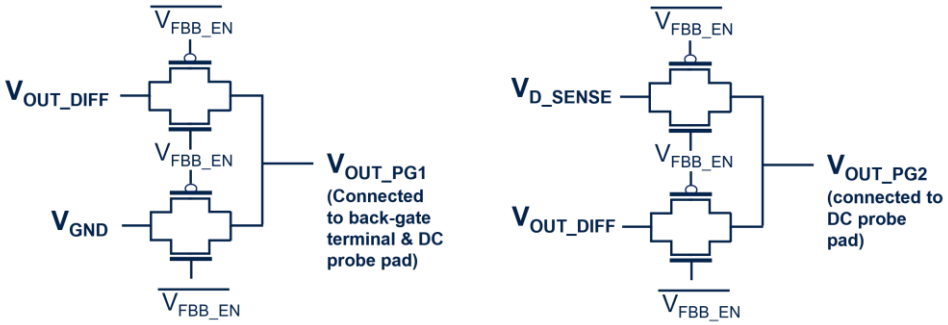

Figure 4-16: (left) PG1 controls the opening (V_{OUT_PG1} out_PG1=GND) and closing ($V_{OUT\_PG1} = V_{OUT\_DIFF}$) of the feedback loop. (right) PG2 provides the readout of probed DC signals V_{OUT_DIFF} and V_{D_SENSE}

Table 4-1 : Logic table for VFBB_EN signal which controls the feedback loop and the read-out of different outputs.

VFBB_EN	Vout_PG1	Vout_PG2
'1'	V_{OUT_DIFF}	V_{D_SENSE}
'0'	GND	V_{OUT_DIFF}

4.2.3 Test Structure Physical Implementation

The physical implementation of the test structure is essential to ensure compatibility of the test structure with the RF load pull measurement setup. One of the most critical steps in the design flow is floor-planning. It must be done before the place and route stage so that the routing between the different building blocks can be optimized and ensure their connections to the probe pads that allow probing of measured signals as well as voltage supply (bias) application. The floor-planning process involves arranging the different building blocks and probe pads within the test structure as described in the following:

- The two types of probe pads, DC and RF, determine the surface area of the test structure due to the distance constraints between DC and RF probe dimensions of the measurement setup. The DC probe pad provides interface between voltage supply of the analog blocks, PA cell bias and also measurements of V_{OUT_PG1} and V_{OUT_PG2} signals. The RF pad, designed with Ground-Signal-Ground (GSG) structure is used to provide on-wafer measurements of the PA cell.

- The input and output of the RF PA is connected to the GSG probe pad such that the routing from the drain terminal to the signal pad is minimized to reduce signal loss. The gate and drain terminals are routed to the DC pads for DC bias supply.

- The power detection unit and attenuator are placed in proximity to the input and output of the RF PA to minimize RF signal loss to the input of the power detectors, without inducing parasitic coupling with the RF PA.

- The feedback control circuit is isolated far away from the RF blocks to avoid signal coupling of the capacitors and at the same time close the distance to DC probe pads.

The layout of the complete test structure, illustrated in Figure 4-17, was implemented in 28nm FD-SOI CMOS technology with a 9-metal layer back-end of line (BEOL) process by STMicroelectronics. The effective surface area of the building blocks occupies 30% of the total silicon area, which could not be fully utilized due to the minimum distance limit between DC and RF probe pads. Aside from this main test structure, two other test structures containing parts of the circuit, i.e., the standalone RF PA with GSG pad and the power detection circuit without feedback control are included for characterization purposes.

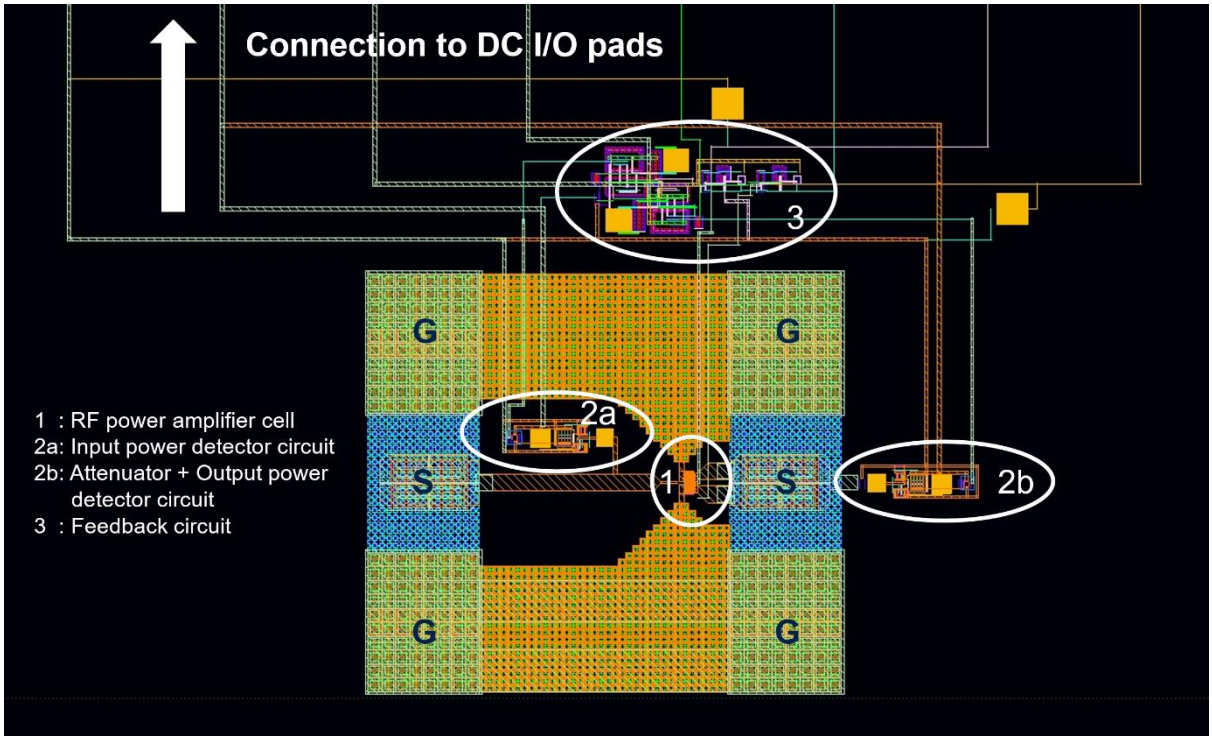

Figure 4-17 : Layout view of the complete test structure for PA aging compensation system designed in 28nm FDSOI CMOS technology with 9-metal layer BEOL process by STMicroelectronics.

4.3 Simulation results and discussion

In this section, the SPICE simulation results of the gain compensation based on adaptive body bias technique are presented at system level to demonstrate the proof of concept. First, the open loop simulations are verified under fresh PA device conditions to perform system calibration at the targeted stress power level. This is then followed by closed loop simulations to analyze the gain compensated according to the level of V_T degradation induced. The post-layout simulations are run in Cadence Spectre using RF testbench integrating EM modeling of RF pad parasitics (refer to section 2.1.4.2).

4.3.1 System calibration in open loop configuration

The calibration of the feedback system is conducted in open loop configuration (V_{FBB_EN}='0') as explained earlier in section 4.2.2.4. The goal of the calibration is to ensure that the feedback control signal is calibrated to a fixed reference value, which is essential to reduce the system error due to PVT variations and performance/design mismatch. In this case, the feedback adaptive bias, represented by V_{OUT_PG2} =V_{OUT_DIFF}, should be equal to 0V at the

targeted power level for RF HCI stress. The calibration tuning knob is given by V_{CAL} which is increased or decreased until V_{OUT_DIFF}=0 according to the initial V_{OUT_DIFF} reading before calibration. The calibration procedure concerning the RF HCI stress at P1dB condition is shown in Figure 4-18. Before calibration (V_{CAL}=0), the initial V_{OUT_DIFF} =+0.8V is obtained, implying a V_{FBB}=0.8V at T_0 when the loop is closed. V_{CAL} =-0.8V is applied to reach the calibration target of V_{OUT_DIFF} = 0V which results in V_{FBB}=0V at T_0 when the loop is closed. Thus, since the PA is stressed at P_{1dB}, the negative values of V_{OUT_DIFF} for P_{OUT} < P_{1dB} that lower the gain will not be an issue.

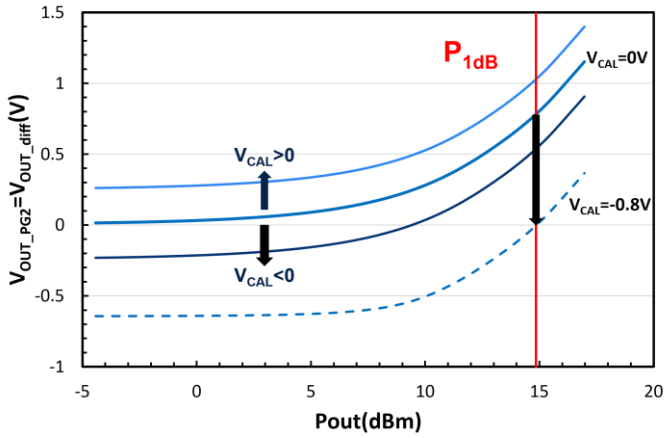

Figure 4-18 : Calibration of the feedback control signal V_{OUT_DIFF} by tuning V_{CAL}. At stress condition Pout=P1dB, the system is calibrated when V_{OUT_DIFF}=0V for V_{CAL} =-0.8V

4.3.2 Closed loop configuration for RF aging compensation

Considering the calibration state at P_{out}=P_{1dB}, the feedback loop is closed at T_0 (without aging). The transient simulation results demonstrating the system behavior from open to closed loop (T_0 =300 ns) is presented in Figure 4-19. V_{OUT_PG1} and V_{OUT_PG2} reach equilibrium after 33.5ns following the activation of V_{FBB_EN} signal. V_{OUT_PG1}, which is connected to V_{FBB} of the PA cell, shows oscillations at 28GHz as it follows the PA operating frequency. At this stage, no compensation of the PA gain is generated since that V_{FBB}=0V.

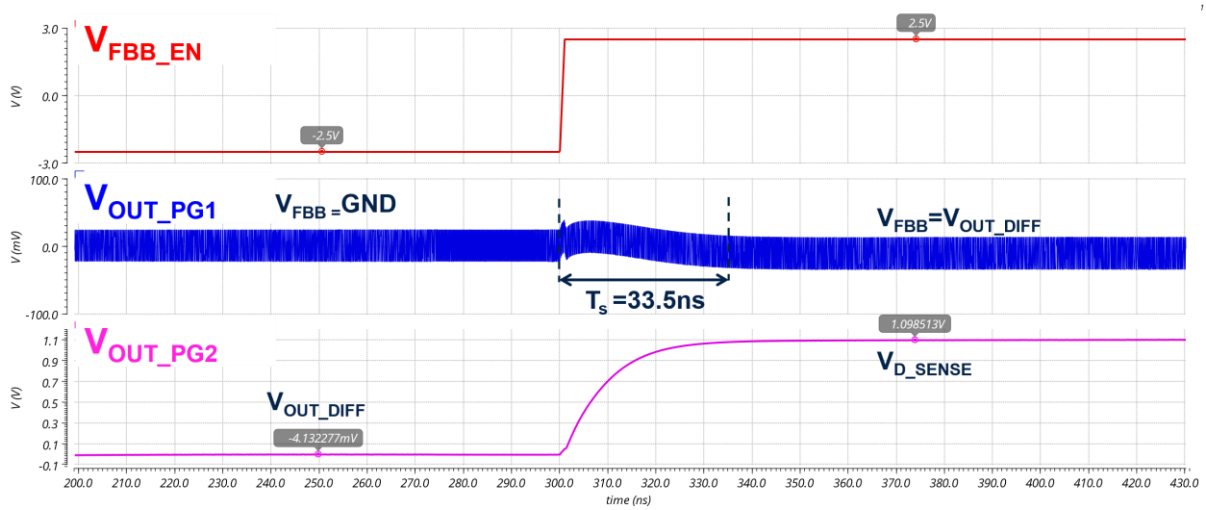

Figure 4-19 : Closed loop response analysis of system output signals V_{OUT_PG1} and V_{OUT_PG2} at T_0 before aging conditions are applied. Thanks to the system calibration, the PA gain at Pout=P1dB remains uncompensated as V_{FBB}=0V.

Subsequently, a transient analysis of the PA aging compensation scenario is provided using the same calibrated system at Pout=P1dB. A typical V_T degradation is emulated by decreasing the V_G DC bias of the PA (V_{G_biasPA}) of a step function with an amplitude of δ_{VG}=-50mV. The loop response of the feedback before and after V_T compensation is demonstrated in Figure 4-20. It is observed that the feedback loop delay is given by the time required for V_{OUT_PG1} stabilization, which is achieved after Ts=300ns. In fact, the stability of the feedback loop is essential as unwanted oscillations (known as ringing) could cause additional stress to the device. To visualize the gain compensation effect, large-signal RF performance is simulated for fresh, aged, and aging compensated PA test case. The results of gain, PAE and I_{DC} presented in Figure 4-21 imply that the PA performance degradation is partially compensated through the feedback loop.

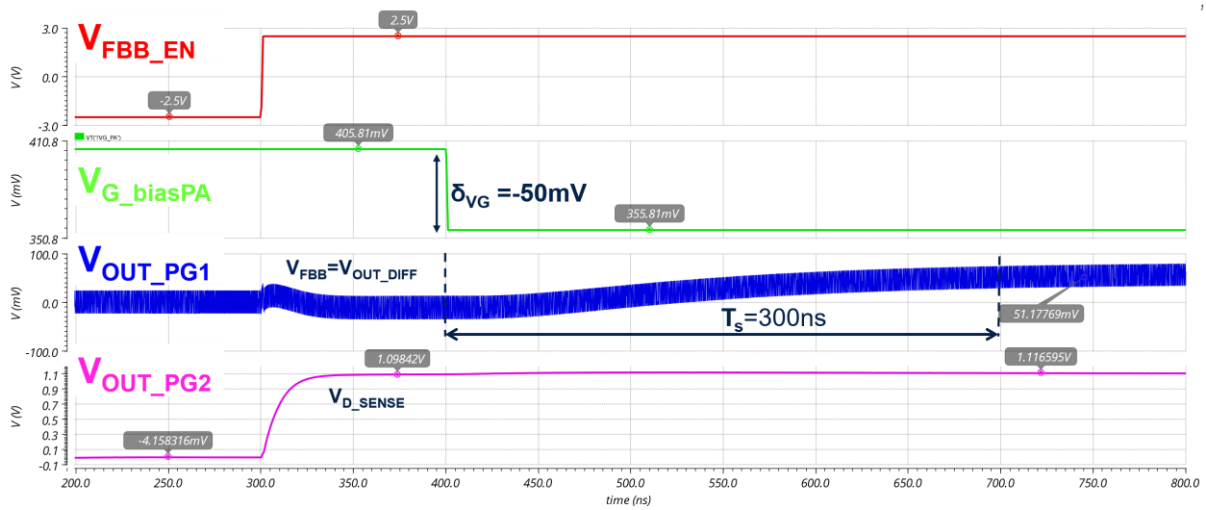

Figure 4-20 : Transient response of closed loop compensation of aged PA emulated by δ_{VG} =50mV step function at PA input bias. Loop stability is achieved after 300ns of delay across capacitive elements in the feedback chain (power detector RC filter and op amp stabilization capacitance).

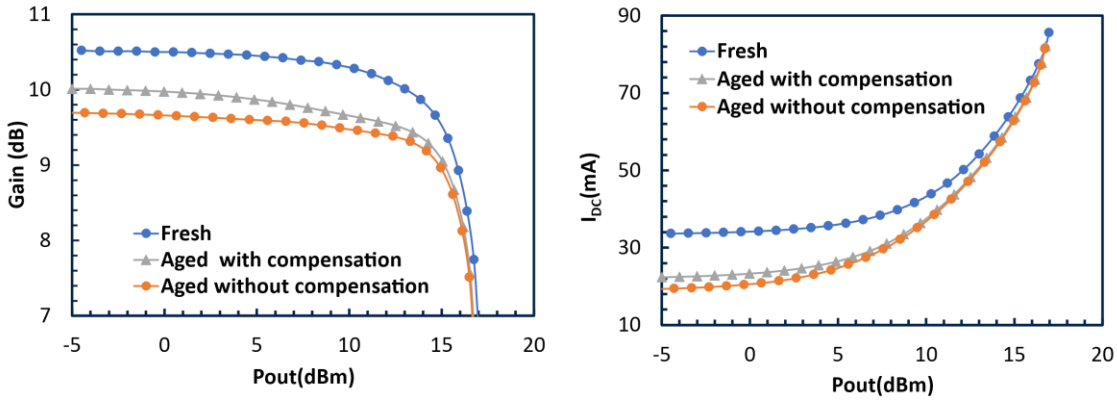

Figure 4-21 : Large-signal RF performance of fresh, aged (δ_{VG}=-50mV) and aging compensated PA. (a) RF gain (b) I_{DSAT}=I_{DC} is partially compensated.

The feedback loop stability is examined by applying a step function with δ_{VG} =-300mV. The amplitude of 300mV was chosen to reflect the V_T degradation of maximum V_{FBB} value that can be applied to increase ΔGain as observed from Figure 4-22. From the simulation results in Figure 4-23, it is observed that the feedback loop delay Ts=350ns, only slightly longer than the previous test case. Based on this observation, we can deduce that the amplitude of V_T degradation does not have a significant impact on Ts and the stability of the feedback loop.

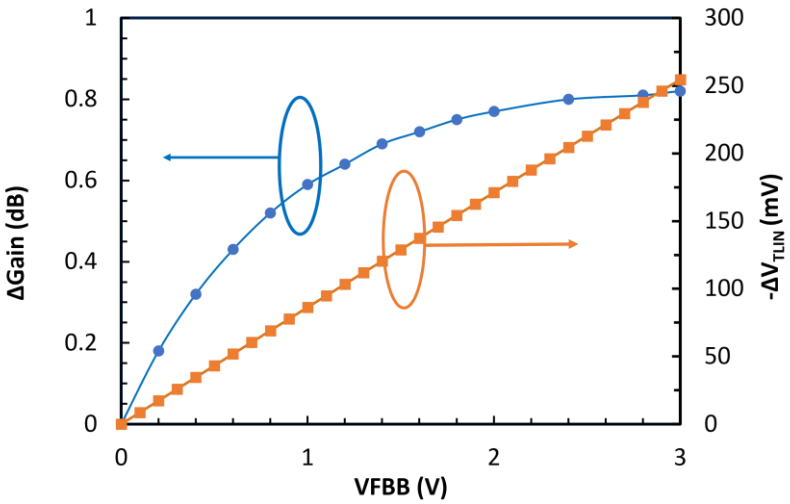

Figure 4-22 : RF gain increase by V_{FBB} where the ΔGain saturates beyond V_{FBB}=3V limit, corresponding to a ΔV_{TLIN} decrease of 250mV.

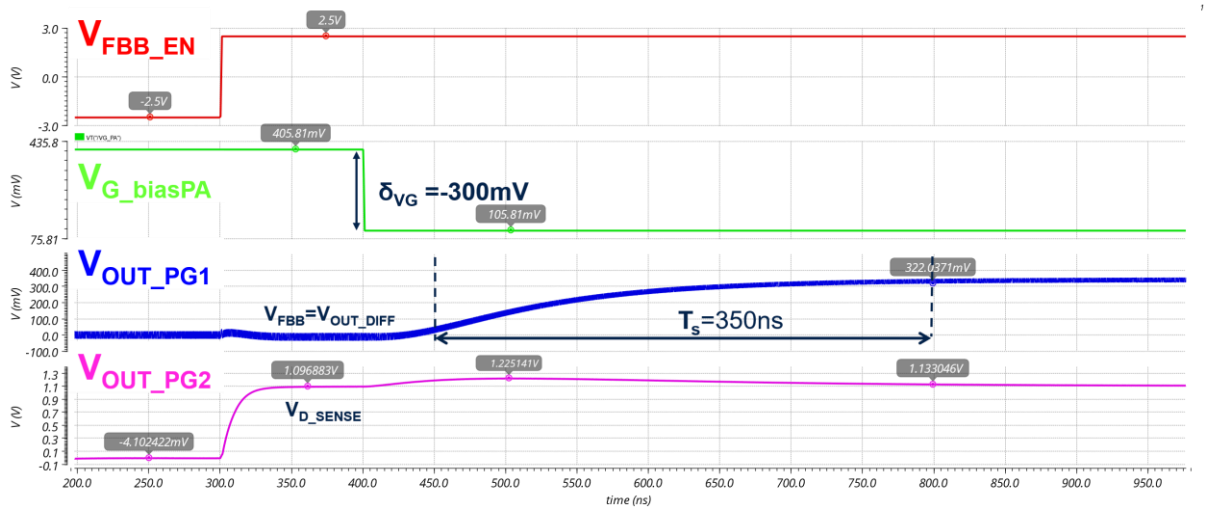

Figure 4-23 : Feedback loop stability analysis at maximum degradation condition δ_{VG} =-300mV. The stability of the loop is ensured, no significant feedback loop delay is observed as compared to Figure 4-20.

4.3.3 Impact of RF HCI degradation on the feedback control loop response

Previous simulations of the closed loop feedback have shown that the magnitude of V_T degradation plays an important role in defining the amplitude of V_{FBB} for gain compensation, although no significant impact on the loop delay is noticed. Another important point to consider is that the V_T degradation rate, corresponding to the slope of $\delta_{VG}(t)$, might be impacted by the compensation rate due to its impact on the feedback path delay. This has been reported in [20] for 28FDSOI I/O devices where the lower VFBB compensation rate results in a stronger reduction of hot-carrier damage. Until this point, this proof of concept has been verified through simulations for discrete aging compensation. For continuous aging compensation, demonstration has to be done by aging measurements on load pull setup to observe the impact of compensation rate on real time V_T degradation kinetics.

4.4 Conclusions

It is of interest to study the prospects of aging compensation in RF PAs to evaluate the lifetime gain estimation. Design, analysis, and simulation results of an automatic gain compensation system capable of counteracting RF HCI aging induced V_T degradation has been presented in this chapter. The compensation system leverages the FBB in FDSOI technology to perform V_T modulation against V_T degradation during device aging, with a higher efficiency compared to bulk-Si technology. The RF PA degradation is monitored by means of RMS power to compute the required body-bias voltage for V_T compensation in the feedback control loop. The main feature of the feedback loop is the gain cancellation function, realized by a fixed resistive attenuator, in order to track the RF gain degradation. On-chip integration of the feedback circuit is designed entirely using analog circuits and can be operated in continuous or discrete mode, thus making this solution highly attractive compared to other approaches involving off-chip controllers or specific self-healing algorithms. The simulation results have validated the proof of concept in different device degradation test cases. In the test case emulating RF HCI degradation at P_{1dB} stress condition, the gain degradation is partially compensated as the system is designed for compensation of the V_T drift component only. Some design improvements to increase the voltage gain of the differential amplifier in the feedback control circuit could be implemented, which can provide a higher V_{FBB} to compensate the large gain degradation. The parametric degradation of other components, i.e., mobility, I_D and R_D, should be compensated with other methods. RF HCI aging measurements on the fabricated prototype are planned for future work to obtain experimental data on the reliability of the V_T compensated PA. Based on the previous reports on DC HCI experimental data with the application of FBB during stress, it is expected that the device is subjected to reliability improvements which will pave the way for future reliable PA designs.

References

[1] J. S. Yuan, “CMOS RF Design for Reliability Using Adaptive Gate–Source Biasing,” *IEEE TRANSACTIONS ON ELECTRON DEVICES*, vol. 55, no. 9, 2008.

[2] T. Azadmousavi and E. N. Aghdam, “Adaptive Body Biasing Circuit for Reliability and Variability Compensation of a Low Power RF Amplifier,” *IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY*, vol. 19, no. 1, 2019.

[3] S. M. Pazos, F. L. Aguirre, F. Palumbo, and F. Silveira, “Hot-carrier-injection resilient RF power amplifier using adaptive bias,” *Microelectronics Reliability*, vol. 114, p. 113912, Nov. 2020, doi: 10.1016/j.microrel.2020.113912.

[4] R. Lajmi *et al.*, “Aging control of power amplifier using power detector,” in *2018 International Integrated Reliability Workshop (IIRW)*, Oct. 2018, pp. 1–4. doi: 10.1109/IIRW.2018.8727098.

[5] J. -P. Noel *et al.*, “Multi-V_{T} UTBB FDSOI Device Architectures for Low-Power CMOS Circuit,” *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2473–2482, Aug. 2011, doi: 10.1109/TED.2011.2155658.

[6] N. Planes *et al.*, “28nm FDSOI technology platform for high-speed low-voltage digital applications,” in *2012 Symposium on VLSI Technology (VLSIT)*, Jun. 2012, pp. 133–134. doi: 10.1109/VLSIT.2012.6242497.

[7] F. Arnaud *et al.*, “Enhanced design performance thanks to adaptative body biasing technique in FDSOI technolologies,” in *2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, Oct. 2017, pp. 1–5. doi: 10.1109/S3S.2017.8308754.

[8] X. Federspiel *et al.*, “28nm node bulk vs FDSOI reliability comparison,” in *2012 IEEE International Reliability Physics Symposium (IRPS)*, Apr. 2012, p. 3B.1.1-3B.1.4. doi: 10.1109/IRPS.2012.6241805.

[9] W. Arfaoui, X. Federspiel, P. Mora, M. Rafik, D. Roy, and A. Bravaix, “Experimental analysis of defect nature and localization under hot-carrier and bias temperature damage in advanced CMOS nodes,” in *2013 IEEE International Integrated Reliability Workshop Final Report*, Oct. 2013, pp. 78–83. doi: 10.1109/IIRW.2013.6804163.

[10] D. Angot, V. Huard, X. Federspiel, F. Cacho, and A. Bravaix, “Bias temperature instability and hot carrier circuit ageing simulations specificities in UTBB FDSOI 28nm node,” in *IEEE International Reliability Physics Symposium Proceedings*, Apr. 2013, p. 5D.2.5. doi: 10.1109/IRPS.2013.6532037.

[11] W. Arfaoui *et al.*, “Energy-driven Hot-Carrier model in advanced nodes,” in *2014 IEEE International Reliability Physics Symposium*, Jun. 2014, p. XT.12.1-XT.12.5. doi: 10.1109/IRPS.2014.6861189.

[12] C. Ndiaye, V. Huard, X. Federspiel, F. Cacho, and A. Bravaix, “Performance vs. reliability adaptive body bias scheme in 28nm & 14nm UTBB FDSOI nodes,” *Microelectronics Reliability*, vol. 64, pp. 158–162, Sep. 2016, doi: 10.1016/j.microrel.2016.07.085.

[13] J. Y.-C. Liu, R. Berenguer, and M.-C. F. Chang, “Millimeter-Wave Self-Healing Power Amplifier With Adaptive Amplitude and Phase Linearization in 65-nm CMOS,” *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES*, vol. 60, no. 5, 2012.

[14] R. G. Meyer, “Low-power monolithic RF peak detector analysis,” *IEEE Journal of Solid-State Circuits*, vol. 30, no. 1, pp. 65–67, Jan. 1995, doi: 10.1109/4.350192.

[15] A. Valdes-Garcia, R. Venkatasubramanian, J. Silva-Martinez, and E. Sanchez-Sinencio, “A Broadband CMOS Amplitude Detector for On-Chip RF Measurements,” *IEEE*

Transactions on Instrumentation and Measurement, vol. 57, no. 7, pp. 1470–1477, Jul. 2008, doi: 10.1109/TIM.2008.917196.

[16] U. R. Pfeiffer, “A 20 dBm Fully-Integrated 60 GHz SiGe Power Amplifier With Automatic Level Control,” vol. 42, no. 7, 2007.

[17] J. Gorisse, A. Cathelin, A. Kaiser, and E. Kerherve, “A 60GHz 65nm CMOS RMS power detector for antenna impedance mismatch detection,” in *2009 Proceedings of ESSCIRC*, Sep. 2009, pp. 172–175. doi: 10.1109/ESSCIRC.2009.5326027.

[18] Y. Zhou and M. Y.-W. Chia, “A Low-Power Ultra-Wideband CMOS True RMS Power Detector,” *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES*, vol. 56, no. 5, 2008.

[19] B. Razavi, “The Transimpedance Amplifier [A Circuit for All Seasons],” *IEEE Solid-State Circuits Magazine*, vol. 11, no. 1, pp. 10–97, Winter 2019, doi: 10.1109/MSSC.2018.2881860.

[20] A. Bravaix, F. Cacho, X. Federspiel, C. Ndiaye, S. Mhira, and V. Huard, “Potentiality of healing techniques in hot-carrier damaged 28nm FDSOI CMOS nodes,” *Microelectronics Reliability*, vol. 64, pp. 163–167, Sep. 2016, doi: 10.1016/j.microrel.2016.07.092.

Conclusions and recommendations for future work

Conclusions

The comprehension of aging mechanisms in RF PA extending to RF reliability modeling improvements have been made possible in this work through extensive collaboration between test structure design, stress characterization and aging simulation approach.

In chapter 2, we have studied the RF HCI degradation modeling approach to address circuit-level reliability simulation using worst-case HCI PA mission profile. The fresh and aged models were calibrated against RF HCI stress measurements in order to propose a reliability evaluation methodology based on the HCI degradation rate established in the VG/VD space of the RF mission profile. The two important factors affecting the accuracy of RF PA aging simulations were identified by performing an RF degradation sensitivity analysis on device modeling parameters (fresh and aged). The first factor involves the accuracy of large-signal MHC of the fresh PA, which relies on the device model optimization of DC and small-signal parameters. The second factor concerns the application of the degraded physical effects in DC aging models and the translation of RF degradation to the correct device model parameters.

In chapter 3, the characterization of frequency dependent effects due to off-state RF degradation and TDDB was conducted on an integrated test structure. On-chip off-state stress waveform was generated at 500MHz and 1GHz with detailed characterization protocol to ensure signal integrity during stress measurements and DC-IV characterization. The off-state TDDB stress measurements exhibited frequency dependence in TBD, with a TBD AC/DC ratio of 2 at 1GHz, while no frequency dependence was observed for β. Off-state degradation shows power law degradation behavior with no frequency dependence, thus indicating that quasi-static approximation is valid until 1 GHz. Although, the saturation of linear current degradation was observed, it only appears after stress time longer than stress waveform period (1ns). Alternating on-state and off-state stress modes provide evidence of strong interaction at low frequency (long stress pulse duration) and negligeable interactions at higher frequency (shorter stress pulse duration). To improve degradation modeling accuracy at low frequency, one should consider these two degradation modes as competing mechanisms in the quasi-static modeling approach.

Performance-reliability trade-off has been examined from a design perspective in chapter 4. An aging compensation proof of concept has been proposed to compensate RF PA performance drift using an adaptive body biasing control loop designed on-chip. The concept consists of compensating the threshold voltage drift contribution in RF degradation via the forward-bias tuning knob offered by the FDSOI technology. This study is to be completed with experimental data to evaluate PA lifetime gain opportunities.

To summarize, this thesis has contributed to improving RF PA reliability predictions that enable accurate device lifetime modeling subjected to RF mission profiles for design optimization considerations. Lifetime gain assessment of aging compensated analog/RF circuits may draw interest in exploring aging-resilient design strategies to combat increasing HCI degradation in short-channel CMOS devices where design optimization is marginal.

Recommendations for future work:

Following the contributions of this thesis, there are still some questions that remain unanswered:

- In this work, it has been observed that DC and RF off-state degradation behavior, caused by the build-up of Si/SiO_2 interface defects, diverge for longer stress periods. To provide a quantitative explanation to this difference, interface defect characterization techniques such as SILC and charge-pumping measurements should be applied. SILC measurements are used to measure defect (trap) density via gate current leakage monitoring, while charge-pumping measurements can provide information on the spatial position of the defects in the lateral and vertical direction of the channel.

- The lifetime enhancement of off-state RF TDDB at 1 GHz has been confirmed compared to the DC case. In the interest of reducing the design margins related to trade-off between high output voltage swings and oxide breakdown, new RF TDDB characterization methods beyond 1GHz should be developed to enable RF TDDB modeling at RF/mmW frequencies. Our characterization framework of RF off-state TDDB relies on square-wave stress pulse waveform to enable time-scaling on well-understood DC TDDB power law model. If non-square-wave stress waveform is used, the time-scaling law is no longer applicable, thus this would require the possibility of exploring another RF TDDB modeling approach.

- RF reliability characterization demonstrated in this work and the literature concern PA RF stress under continuous-wave operation, which is essential to establish the relation between measured RF degradation and DC aging model. The next step to approach actual RF PA use case is to conduct PA reliability evaluation under different wireless modulation schemes, in particular high PAPR modulation, to correlate with CW degradation. However, due to the PA operation at high PAPR for short duration, a longer stress duration is expected to achieve the same amount of degradation compared to CW stress. Therefore, a packaged PA module is required for long-term stress evaluation.

We also propose the following suggestions to extend the research area of RF PA device-level reliability towards system-level reliability in terms of aging-aware methodologies:

- In the design process, it is necessary to address aging effects at the start of the design flow. This is implemented through aging-aware design methods to provide

designers with design tuning knobs to determine the optimal operating point for a targeted reliability criterion. It can be established in the form of aging sensitivity maps of RF FOM (gain, PAE, P_{1dB}) against design parameters (P_{OUT}, I_D, V_{DD}, R_L) which are linked to the VG/VD mission profile. This would imply that the aging model card must accurately predict device degradation in reliability simulations.

- Efficiency and linearity enhanced RF PA architectures such as envelope tracking (ET) and digital pre-distortion (DPD) that make use of an auxiliary component in the system to dynamically adjust the PA operation can benefit from aging-aware compensation methods. The aging effect of the PA on the system performance can be controlled if the correlation between the monitored PA device degradation and the characteristic of the auxiliary component can be determined.

Appendix A: PA Device DC Model Optimization

To enable accurate large-signal PA simulations in Chapter 2, the BSIM DC model is optimized to fit the DC and small-signal measurement data of the PA device (NMOS LVT W=400µm L=60nm). The model optimization is performed to ensure the model accuracy in the different MOSFET DC operating regimes, from subthreshold to saturation regime. The IDVG curves of the NMOS PA device model before and after optimization with comparison to measurements is presented in Figure A-0-1. In the subthreshold regime ($V_G \leq V_T$), the model parameters, NFACTOR (subthreshold swing coefficient) and ETA0 (drain-induced barrier lowering coefficient), related to this regime were identified and optimized to fit the measurement data. The linear regime ($V_T < V_G < V_{DSAT}$) is optimized at different VD using the extrinsic drain (R_{Dext}) and source parameters (R_{Dext}) to consider voltage drop due to probe contact resistance during DC measurements. The saturation regime ($V_G - V_T \leq V_{DSAT}$) current is mainly optimized using the velocity saturation parameter VSAT.

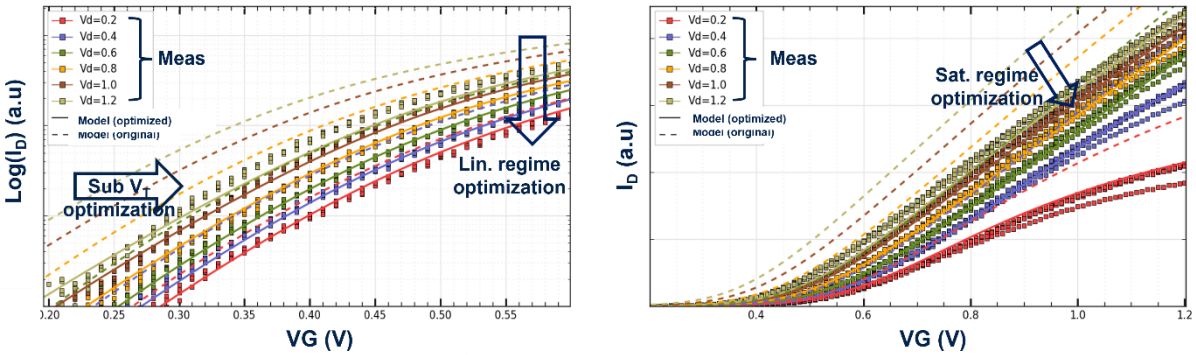

Figure A-0-1 : DC model optimization in the subthreshold (sub V_T), linear (lin) and saturation (sat) regimes.

To deal with the impact ionization (ii) current in the deep saturation regime (VD>1.2V), the ii parameters ALPHA0, BETA0, BETA1 and BETA2 in the BSIM model were adjusted based on the IdVd measurement data as shown in Figure A-0-2. Self-heating effect, which enhances the ii phenomenon, is accounted via thermal resistance parameter (RTH).

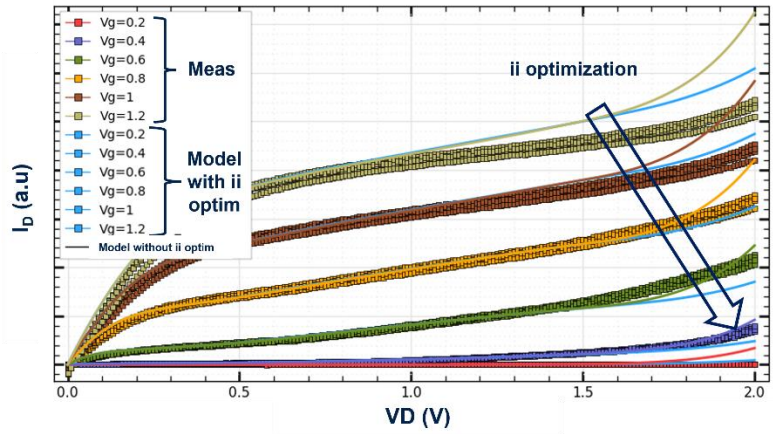

Figure A-0-2 : DC model optimization of impact ionization and self-heating effects

While the model fit shows good agreement to experimental measurements in subthreshold and linear regime, the deep saturation regime involving ii current modeling does not accurately fit the measurement data. To improve the DC model is this region, additional measurements of the body current (Ib) as a function of VG for various VD is required as the body current collects the carrier (holes) generated by ii. Thus, Ib has an exponential dependence on VG while the ii efficiency is driven by VD. Nevertheless, the DC model accuracy is guaranteed in the VG/VD operation space specified by the PA mission profile in Chapter 2.

List of publications

J. Hai, F. Cacho, X. Federspiel, T. Garba-Seybou, A. Divay, E. Lauga-Larroze, J.-D. Arnould, "Integrated Test Circuit for Off-State Dynamic Drain Stress Evaluation", 2023 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2023.

J. Hai, F. Cacho; A. Divay; E. Lauga-Larroze; J.-D. Arnould; J. Forest; V. Knopik, X. Garros, "Comprehensive Analysis of RF Hot-Carrier Reliability Sensitivity and Design Explorations for 28GHz Power Amplifier Applications," 2022 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 2022.

A. Divay, J. Forest; V. Knopik; **J. Hai**; N. Revil; J. Antonijevic; A. Michard; F.Cacho, E.Vincent, G.Gaillard, X.Garros , "65nm RFSOI Power Amplifier Transistor Ageing at mmW frequencies 14 GHz and 28 GHz", 2021 IEEE International Electron Devices Meeting (IEDM),San Francisco, CA, USA, 2021.

Abstract

The development of SOI CMOS technology has greatly contributed to the rapid evolution of RF/mmW communication systems which play a critical role in the deployment of 5G networks. To meet the performance targets of 5G specifications, complex modulation schemes use high peak-to-average-power (PAPR) levels that are generated by the power amplifier (PA). The high-power levels, in turn, impact the device reliability due to the voltage handling limits of modern CMOS technology. At early design stages, accurate aging models can be leveraged to assess the trade-off between performance and reliability in consideration of the targeted RF mission profile. The two dominant CMOS reliability mechanisms found in RF PA mission profiles are hot-carrier injection (HCI) and off-state time-dependent dielectric breakdown (off-TDDB). The first part of this thesis aims to consolidate the HCI aging model using well-established RF/mmW aging methodology by performing model-to-hardware correlation (MHC) at accelerated DC and 28GHz RF stress conditions for different PA cell topologies. The MHC, validated for fresh and degraded PA device, is then used to perform a simulation-based sensitivity analysis to evaluate the impact of different model card parameters on the accuracy of RF HCI modeling. The results showed that both fresh and degradation model precision affects the RF degradation estimation, which highlights the significance of a degradation model described by physical effects of the device. The second part of this thesis focuses on the validity of RF modeling approach for off-state reliability (HCI degradation and TDDB). An integrated test structure generating off-state RF stress waveforms at DC, 500MHz and 1GHz to evaluate the frequency dependence in off-state reliability modeling has been designed. Time-power law parametric degradation has been observed in DC and RF (500MHz and 1GHz) off-state HCI stress measurements, suggesting the validity of quasi-static modeling approach for off-state HCI degradation. On the other hand, off-state RF TDDB characterization demonstrates increasing time-to-breakdown with increasing frequency, in particularly a gain factor of x2 at 1GHz compared to DC TDDB. This study was then extended to on and off-state RF HCI stress sequences revealing negligible interaction between the two degradation mechanisms, resulting in an additive degradation modeling approach. The last part of this thesis provides proof of concept to demonstrate aging compensation of a 28GHz RF PA. This is done by implementing the design of a negative feedback loop for on-chip adaptive body bias control in FDSOI technology which partially compensates the threshold voltage drift induced by RF HCI stress.

Résumé de la thèse

Le développement de la technologie SOI CMOS a contribué à l'évolution rapide des systèmes de communication RF/mmW qui jouent un rôle critique dans le déploiement des réseaux 5G. Pour répondre aux objectifs de performance des spécifications 5G, des schémas de modulation complexes utilisent des niveaux de puissances crête sur puissances moyennes (PAPR) élevés qui sont générés par l'amplificateur de puissance (PA). Ces niveaux de puissance élevés ont un impact important sur la fiabilité du dispositif en raison des limites en tension de la technologie CMOS moderne. Dans les premières étapes de la conception, des modèles de vieillissement précis peuvent être utilisés pour évaluer le compromis entre les performances et la fiabilité en considérant le profil de mission RF spécifique. Les deux mécanismes de fiabilité CMOS principaux trouvés dans les profils de mission RF PA sont l'injection de porteurs chauds (HCI) et le claquage d'oxyde de grille en état « off » (off-TDDB). La première partie de cette thèse vise à consolider le modèle de vieillissement HCI en utilisant une méthodologie de vieillissement RF/mmW bien établie en effectuant une corrélation modèle-hardware (MHC) dans des conditions de stress DC accélérées et RF 28GHz pour différentes topologies de cellules PA. La MHC, validée pour le transistor PA avant (appelé « fresh ») et après la dégradation, est ensuite utilisée pour effectuer une analyse de sensibilité basée sur la simulation afin d'évaluer l'impact des différents paramètres de carte de modèle sur la précision de la modélisation RF HCI. Les résultats ont montré que la précision du modèle « fresh »et dégradé peut influencer l'estimation de la dégradation RF, ce qui souligne l'importance d'un modèle de dégradation décrit par les effets physiques du transistor. La deuxième partie de cette thèse se concentre sur la validité de l'approche de modélisation RF pour la fiabilité « off-state » (dégradation HCI et TDDB). Une structure de test intégrée générant des formes d'ondes de stress RF off-state à DC, 500 MHz et 1 GHz pour évaluer la dépendance en fréquence dans la modélisation de la fiabilité RF off-state. Une dégradation paramétrique suivant une loi en puissance a été observée suite aux mesures de stress HCI « off-state » en DC et RF (500 MHz et 1 GHz), suggérant la validité de l'approche de modélisation quasi-statique pour la dégradation HCI. D'autre part, la caractérisation off-TDDB RF montrent une augmentation du temps de claquage avec l'augmentation de la fréquence, en particulier un facteur de gain de x2 à 1 GHz par rapport à TDDB DC. Cette étude a ensuite été étendue aux séquences de stress HCI RF « on-state » et « off-state », révélant une interaction négligeable entre les deux mécanismes de dégradation, ce qui donne lieu à une approche de modélisation de dégradation additive. La dernière partie de cette thèse fournit une preuve de concept pour démontrer la compensation du vieillissement d'un PA RF de 28 GHz. Cela s'appuie sur la conception d'une boucle de rétroaction négative pour le contrôle de polarisation adaptatif « body-bias » sur puce en technologie FDSOI qui compense partiellement la dérive de tension de seuil induite par le stress HCI RF.