Design and characterization of readout ASICs for SiPM detectors in pico-second timing measurements for the CMS HGCAL experiment

José González Martínez

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Thèse de doctorat

Design and characterization of readout ASICs for SiPM detectors in pico-second timing measurements for the CMS HGCAL experiment.

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Résumé de la thèse en Français

La physique des particules a toujours recherché un modèle précis permettant de comprendre et de prédire le comportement de notre univers. L'humanité continue de s'approcher des modèles les plus précis et les plus complexes grâce au développement de nouvelles technologies. Nous recherchons la particule la plus petite et la plus générique qui forme tout ce que nous connaissons, contribuant ainsi à une meilleure compréhension de notre monde et de l'univers.

Cependant, la taille minuscule des particules subatomiques constitue un défi de taille. Au fil des ans, les physiciens ont réussi à détecter et à visualiser ces particules. Des détecteurs avancés peuvent désormais identifier et caractériser diverses particules en mesurant leur énergie, leur quantité de mouvement et leur temps. Les accélérateurs permettent d'étudier la composition de la matière en accélérant les particules élémentaires à des vitesses proches de celle de la lumière. La collision de ces particules les décompose, donnant naissance à d'autres particules qui constituent la matière observée. Des détecteurs à grande échelle mesurent l'énergie et étudient les particules issues de ces collisions. Initialement, la collecte d'événements photographiques était utilisée dans les détecteurs d'accélérateurs pour reconstruire les particules générées lors des collisions. Aujourd'hui, l'enregistrement de données électroniques ouvre de nombreuses possibilités, facilitant les expériences à haut débit qui mesurent les particules avec une résolution de l'ordre de la picoseconde et offrant la possibilité de découvrir de nouvelles particules ou interactions.

Les connaissances actuelles sur la composition et le comportement de la matière sont consolidées dans le modèle standard de la physique des particules, qui explique les particules élémentaires et leurs interactions. Au cours des 15 dernières années, nous sommes entrés dans une nouvelle ère de précision dans la mesure de l'énergie des jets de particules. Les calorimètres disposent désormais d'excellentes capacités d'imagerie, ce qui permet de reconstruire avec précision les particules produites lors d'une collision. Cependant, avec l'émergence de nouveaux projets de physique des particules, il existe une demande pour des systèmes encore plus précis et de nouvelles techniques pour répondre aux questions posées par le modèle standard. Les calorimètres ayant une durée de vie opérationnelle limitée, il devient nécessaire de les remplacer, ce qui permet aux nouveaux projets d'améliorer la précision des mesures et les capacités des calorimètres tout en optimisant les algorithmes de flux de particules.

L'expérience CMS (Compact Muon Solenoid collaboration) a permis des avancées et des découvertes significatives en caractérisant les particules fondamentales et leurs interactions telles qu'elles sont décrites par le modèle standard de la physique. Le détecteur fonctionne au sein du Grand collisionneur de hadrons (LHC) au CERN. Cependant, malgré les excellents résultats obtenus dans ce collisionneur, il est nécessaire d'améliorer les capacités de lecture de la luminosité d'au moins un ordre de grandeur tout en maintenant une grande précision afin de répondre aux exigences des expériences complexes à venir. Le calorimètre à haute granularité (HGCAL) est en cours de développement et devrait être pleinement opérationnel d'ici 2029 [1]. Le HGCAL augmentera le nombre de pièges à particules et améliorera la précision tout en

conservant le concept de détection des couches.

Les progrès réalisés dans le domaine des détecteurs suscitent également des attentes en matière d'électronique frontale, en particulier face à des niveaux de rayonnement anticipés qui pourraient être dix fois plus élevés que ceux initialement expérimentés dans la conception du CMS [2]. En conséquence, de nouveaux circuits intégrés à application spécifique (ASIC) sont en cours de développement pour détecter une gamme plus large de signaux, offrir une meilleure résolution de mesure et améliorer la précision des informations sur le temps d'arrivée. La tolérance aux rayonnements et la réduction du bruit des ASIC sont essentielles pour obtenir des mesures plus précises. En outre, le traitement des données après numérisation représente un ajout précieux aux ASIC, car il permet de sélectionner des données significatives parmi le nombre croissant d'interactions au niveau des détecteurs et d'atténuer la quantité excessive de données résultant d'une luminosité plus élevée.

La complexité de l'application exige une augmentation du nombre de fonctionnalités dans la puce. Dans le domaine analogique, des blocs précis doivent être ajustés en fonction de plusieurs paramètres, tandis que la partie numérique nécessite une mémoire et une logique complexe pour sélectionner des données significatives. En outre, les ASIC doivent améliorer la résistance aux radiations, en augmentant la taille des transistors les plus impactants dans les blocs analogiques et en triplant la logique numérique pour protéger le traitement des données au sein de la puce.

Dans la conception des ASIC, la technologie CMOS (complementary metal oxide semiconductor technology) s'impose comme la technologie la plus efficace et la plus largement utilisée, grâce à la flexibilité des transistors MOS en tant que blocs de construction fondamentaux. Chaque conception analogique commence au niveau transistor, impliquant la sélection de l'architecture et de la taille des transistors pour répondre aux exigences spécifiées. La conception d'un ASIC implique généralement la connexion de plusieurs modules, tels que des amplificateurs, des convertisseurs analogique-numérique (ADC), des discriminateurs, des shapers, des convoyeurs de courant (CC), etc.

L'électronique front-end est essentielle pour répondre aux spécifications de lecture des détecteurs photomultiplicateurs au silicium (SiPM). Un SiPM se compose d'un réseau de diodes à avalanche à photon unique (SPAD) intégrées dans un seul capteur, où chaque SPAD fonctionne comme un pixel. Lorsqu'il est exposé à des impulsions lumineuses, chaque pixel recevant un photon génère un pic de courant de la même magnitude. Alors que l'amplificateur de charge classique est un choix standard pour la lecture dans les environnements de rayonnement en raison de son faible bruit, il peut ne pas être la solution optimale pour les détecteurs SiPM.

Dans la littérature, trois configurations principales sont généralement employées pour la lecture des détecteurs SiPM : le préamplificateur de tension, l'amplificateur radiofréquence et le convoyeur de courant. Chaque architecture présente des avantages et des inconvénients, avec des innovations en matière de réduction du bruit, de précision de la synchronisation et de plage dynamique. Ces avancées reflètent la recherche constante de performances accrues en matière de lecture SiPM.

Les ASIC HGCROC sont des systèmes électroniques frontaux dédiés, conçus en technologie TSCM 130 nm pour la lecture des détecteurs au silicium et des SiPM du nouveau HGCAL. Au cours de la phase conceptuelle, il a été déterminé que l'utilisation d'un ASIC similaire ou identique pour les deux types de capteurs sur le détecteur serait avantageuse [2]. Cependant, cette décision a posé un défi important pour le développement du H2GCROC pour la lecture SiPM. Les capteurs SiPM présentent des avantages, notamment un gain plus élevé et un coût inférieur à celui des capteurs au silicium. Cependant, ils sont moins tolérants aux rayonnements et présentent des capacités plus importantes qui augmentent avec la taille du capteur. En ce qui concerne la charge, le signal d'entrée du H2GCROC sera environ 30 fois plus important

que le maximum attendu des capteurs au silicium.

Pour relever ce défi, il a été nécessaire de développer une variante du HGCROC qui adapte le signal d'entrée à la gamme de charges possible dans la limite de la capacité de la même architecture frontale. Le H2GCROC lit les SiPM couplés à des tuiles scintillantes dans les sections hadroniques arrière, où les contraintes de rayonnement sont moins sévères. La solution mise en œuvre utilise un convoyeur de courant conçu explicitement pour les SiPM, capable d'atténuer le signal de courant tout en maintenant une impédance compatible avec l'entrée du préamplificateur du frontal. Par la suite, les autres aspects de la puce conservent les mêmes fonctionnalités que le HGCROC, avec des ajustements mineurs dans les paramètres de configuration pour tenir compte des plages de charge des SiPM comme prévu. Le H2GCROC peut lire les données de charge à l'aide d'un ADC et d'un TDC pour la technique du temps sur seuil (time-over-threshold ou TOT). Un module TDC dédié fournit des informations temporelles pour les mesures du temps d'arrivée (time-of-arrival ou TOA) des particules [3].

L'une des contributions de cette thèse a été de modifier certains blocs pour rectifier la correction des dommages dus à l'irradiation avec des SiPMs irradiés. Les SiPMs irradiés génèrent un courant de fuite aux entrées du canal. La compensation du courant de fuite a été augmentée de 290 μA à 1,5 mA. Un dispositif de mesure et d'analyse des SiPM a également été proposé et construit pour évaluer l'injection de photons dans les installations d'OMEGA.

Des essais approfondis en laboratoire des deuxième et troisième versions de la puce sont en cours depuis 2020. La puce présente un haut degré de configurabilité, avec des paramètres permettant d'ajuster le gain, la forme et les seuils temporels, ce qui permet des mesures précises à la fois de la charge et du temps.

La puce peut lire des charges de 160 fC à 320 pC avec un bruit inférieur à 100 fC, en consommant 11,8 mW par canal. Les circuits d'étalonnage à l'intérieur de la puce permettent la lecture de spectres à photon unique en utilisant la configuration d'étalonnage tout en compensant les variations entre les canaux à l'aide d'un DAC pour la compensation de la tension continue aux entrées du canal. Compte tenu de l'environnement opérationnel de l'expérience, l'ASIC s'est avéré fonctionner efficacement à des températures allant de -39 °C à 50 °C. En ce qui concerne les mesures de temps, l'ASIC a une résolution inférieure à 100 ps. L'ASIC a été testé avec des SiPMs ayant des caractéristiques similaires aux SiPMs finaux de HGCAL avec des surfaces de 2 mm², 4 mm², et 9 mm². L'augmentation de la surface du SiPM produit un bruit electronique plus important, réduit le gain de charge et la résolution temporelle des mesures. Cependant, une plus grande surface de SiPM produit plus de photons à partir du MIP et génère un rapport MIP-bruit plus important. Le choix final des SiPM est à l'étude dans le cadre de l'expérience CMS qui analyse l'utilisation de SiPM de grande surface uniquement.

La caractérisation expérimentale des effets du rayonnement sur l'ASIC a été examinée avec des irradiations TID au CERN. En outre, des tests d'effets à événement unique (SEE) ont été réalisés à l'aide de tests aux ions lourds (effectués au cyclotron de l'UCL à Louvain) et de tests aux protons (effectués à Arronax à Nantes) spécifiquement sur la version Si de l'ASIC afin d'évaluer les blocs partagés avec H2GCROC. L'ASIC s'est avéré tolérant aux radiations jusqu'à 19 Mrad.

Le faisceau d'essai offre un environnement plus proche de ce qui sera rencontré dans HGCAL. Les mesures effectuées pendant le faisceau d'essai à DESY ont fourni des données expérimentales cruciales, permettant un examen détaillé des performances de l'ASIC dans un environnement opérationnel réaliste. H2GCROCv3 a lu avec succès les données MIP d'une carte entièrement équipée de SiPMs de 4 mm². La capacité de l'ASIC à mesurer les variations des différents SiPMs connectés à la puce a été analysée en lisant le spectre de photons uniques de chaque SiPM.

En résumé, l'ASIC H2GCROC a démontré sa capacité à répondre aux exigences de l'ex-

périence HGCAL. Cependant, quelques modifications seront nécessaires pour la prochaine version finale de l'ASIC (v3b).

Les travaux menés dans le cadre de ce programme de doctorat ont respecté l'organisation du projet et de la qualité du CERN, y compris les diverses séquences d'examen et les étapes du projet. De plus, les engagements des deux laboratoires, OMEGA et LLR, ont été suivis de près par le responsable de CMS France et la division de physique des particules du DAS de l'IN2P3.

Les recherches menées au cours de cette thèse ont permis de faire progresser de manière significative la compréhension des détecteurs SiPM et de leur conception ASIC dans le contexte de la physique des particules. Cette thèse analyse principalement l'ASIC H2GCROC, justifiant ses choix de conception tout en mettant en évidence ses forces et ses faiblesses. De plus, cette thèse offre des perspectives pour de futures conceptions d'ASIC pour des applications de lecture SiPM.

Chapter 1

Introduction

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1.1 Overview

In the last 15 years, we have entered a new era of precision in measuring particle jet energies. Calorimeters now possess excellent imaging capabilities, allowing us to capture precise information for reconstructing all particles produced in a collision [4]. Nevertheless, the new particle physics projects demand even more precise systems and novel techniques to address existing questions of the standard model of particle physics. Since calorimeters have a limited operational lifetime, replacement becomes necessary, allowing new projects to improve measurement precision and calorimeter capabilities while optimizing particle flow algorithms [5].

The Compact Muon Solenoid collaboration (CMS) experiment has made significant advances and discoveries by characterizing fundamental particles and their interactions as described by the standard model of physics. The detector operates within the Large Hadron Collider (LHC) at CERN. However, despite the excellent results achieved at this collider, there is a need to improve the luminosity reading capabilities by at least an order of magnitude while maintaining high precision to meet the requirements of upcoming complex experiments. The High Granularity Calorimeter (HGCAL) is developing and is expected to be fully operational by 2029 [1]. The HGCAL will increase the calorimeter granularity to enhance the precision while retaining the concept of layer detection.

However, pointing to better detectors also raises expectations for the performance of front-end electronics, particularly in the face of anticipated radiation levels that may be ten times higher than initially experimented in the CMS design [2]. As a result, new Application-Specific Integrated Circuits (ASICs) are under development to detect a broader range of signals, offer improved measurement resolution and enhance the precision of time-of-arrival information. Addressing radiation tolerance and reducing ASIC noise is essential to achieving more precise measurements [5]. Additionally, post-digitization data treatment represents a valuable addition to ASICs, assisting in selecting meaningful data from the increasing number of interactions at detectors and mitigating the data overload resulting from higher luminosity.

The HGCROC ASICs are dedicated very front-end electronics designed for reading out the

HGCAL, which will replace the current end-cap calorimeters in the CMS experiment at the LHC. The H2GCROC ASIC was specifically designed to read out the Silicon Photo Multipliers (SiPMs) coupled with scintillating tiles in the back hadronic sections, where radiation constraints are less severe. Within the chip, the front-end comprises a current conveyor and a preamplifier intended to capture the high signal levels from SiPMs, with expected charges falling in the range of pC per Minimum Ionizing Particle (MIP). Extensive laboratory testing of the second and third chip versions has been underway since 2020. This work contains an in-depth examination of the very front-end's design and performance, including irradiation campaigns and ASIC performance during beam tests.

The front-end architecture of HGCROC ASICs can read charge data using an ADC and TDC for the time-over-threshold (TOT) technique. A dedicated TDC module provides time information for particles' time-of-arrival (TOA) measurements [3]. The front-end electronics responsible for developing these techniques and modules must meet stringent requirements, including low noise, integral linearity, accurate timing, broad charge dynamic range, rapid shaping time and high radiation tolerance [6].

1.2 Objectives and Contributions

Among the two ASICs developed for reading out the HGCAL detectors, H2GCROC was designed for reading out SiPMs coupled with scintillating tiles in the hadronic calorimeter. The primary objective of this work is to provide insight into the design of this ASIC and to justify the decisions made in both the very front-end and the digital components of the chip. In this manuscript, the reader will gain an understanding of how calorimeters used in particle physics function and their connection to readout ASICs and associated electronics. Then, it will be possible to understand the planned HGCAL experiments that use the SiPM detectors, the H2GCROC ASIC and the primary challenges associated with their design.

From the numerous H2GCROC requirements, the experimental characterization of radiation effects on the ASIC will be deeply examined. Total Ionizing Dose (TID) irradiations for H2GCROC were conducted at CERN to assess the chip's performance in the presence of accumulated irradiation damage. Additionally, Single Event Effects (SEE) testing was performed using heavy-ion tests (conducted at the UCL cyclotron in Louvain) and proton tests (conducted at Arronax in Nantes) specifically on the Si-version of the ASIC to evaluate shared blocks with H2GCROC.

This thesis will delve into the analog design of the ASIC and analyze it using Cadence design tools. The work started with the second version of the chip, which had already been fabricated. Initially, the chip was analyzed to comprehend its structure, and subsequent improvements were implemented. One contribution of this dissertation was modifying certain blocks to rectify irradiation damage correction with irradiated SiPMs. A SiPM measurement and analysis setup was also proposed and constructed to assess photon injection at OMEGA using the fabricated chips. SiPMs with characteristics similar to those explicitly designed for HGCAL were employed in this evaluation.

The work conducted during this Ph.D. program adhered to CERN's project and quality organization, including various review sequences and project milestones. Furthermore, the CMS France manager and the DAS particle physics division of IN2P3 closely monitored the commitments of the two laboratories, OMEGA and LLR.

The research carried out during this Ph.D. program has significantly advanced the understanding of SiPM detectors and their ASIC design in particle physics. This dissertation primarily focuses on analyzing the H2GCROC ASIC, providing justification for its design choices while

highlighting its strengths and weaknesses. Moreover, it offers insights for future ASIC designs for SiPM readout applications.

1.3 Thesis outline

Chapter 2 provides a comprehensive overview of the physics involved in calorimeter detectors, offering insights into the fundamentals of particle physics. The chapter elaborates on the characteristics of the High Granularity Calorimeter (HGCAL) within the CMS experiment and the specific requirements for ASIC design tailored to the various sensors integrated into the detector.

Chapter 3 of this thesis delves into the comprehensive understanding of SiPM technology and its implications for designing a front-end readout ASIC. Furthermore, it analyzes state-of-the-art ASICs for reading Silicon Photo Multipliers (SiPMs). It explores various front-end techniques in the literature, providing insights into their results, advantages and disadvantages.

Chapter 4 delves into the architecture of the H2GCROC ASIC. It begins by explaining the primary structure of the chip, followed by an in-depth exploration of the very front-end of an H2GCROC channel, including the distinctive characteristics of different analog blocks. Additionally, the chapter analyzes the impact of a SiPM connected in a single channel. Simulation analyses are employed to assess the chip's performance at this stage. Subsequently, the chapter describes the differences between the last two versions of the chip, detailing the modifications made and the reasons behind them. Finally, it provides a comprehensive overview of the calibration processes necessary to utilize the ASIC effectively.

The principal contribution of this dissertation lies in the characterization of the chip. Chapter 5 initiates with an introduction to the various setups used for measuring the ASIC's performance. It then proceeds with an in-depth exploration of the calibration process, accompanied by quantified results before and after calibration. The chapter presents the performance of charge measurement and time resolution derived from measurements conducted on a dedicated test bench employing SiPMs of different sizes. Furthermore, it investigates the diverse functionalities of the chip, starting with charge and time measurements and exploring the diverse ASIC features. Lastly, the chapter offers an overview of the results obtained from irradiation campaigns, supported by corresponding analyses.

Chapter 6 starts with the ASIC's performance during beam tests. It consolidates the main components of the thesis, including the state-of-the-art analysis (Chapter 3), simulation results (Chapter 4) and ASIC characterization results (Chapter 5). It provides overall conclusions and compares the chip's characterization with simulations and project specifications. An analysis of the advantages and disadvantages is conducted by comparing the ASIC's performance with other SiPM readout techniques found in the literature, and avenues for potential improvements are explored.

Chapter 2

Background of the CMS HGCAL Experiment

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2.1 Introduction

Particle physics has always pursued a precise model that understands and predicts our universe's behavior. Humanity continues to approach the most accurate and complex models thanks to the development of new technologies. We seek the smallest and most generic particle that forms everything we know, contributing to a deeper understanding of our world and the universe.

However, a significant challenge with sub-atomic particles is their minuscule size. Over the years, physicists have successfully detected and visualized these particles. Early detectors relied on the human eye to observe traces left by particles passing through specific environments. In 1911, Charles Thomson Rees Wilson introduced the fog chamber [7], which made visible the trails of ions left by ionizing particles. During that era, the traces' distance, thickness, and curvature helped study the particles. Figure 2.1 displays a photograph of a fog chamber reading the traces of particles produced by a radioactive source.

Advanced detectors can now identify and characterize various particles by measuring their energy, momentum and time. Accelerators provide a tool to study the composition of matter.

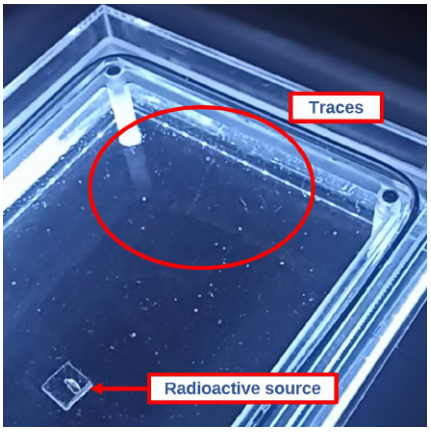

FIGURE 2.1 – *Photograph of a fog chamber and a trace made by a particle coming from a radioactive source.*

The fundamental principle involves accelerating elementary particles to speeds close to the speed of light. Consequently, the collision of these particles decomposes them, giving rise to other particles that constitute the matter we observe. Large-scale detectors measure the energy and study the particles created in these collisions. Initially, photographic event collection was utilized in accelerator detectors to reconstruct particles generated during collisions. Presently, recording electronic data opens up numerous possibilities, facilitating high-rate experiments that measure particles with picosecond resolution and offering the potential to discover new particles or interactions.

The existing knowledge about the composition and behavior of matter is consolidated in the Standard Model of particle physics, explaining elementary particles and their interactions. However, despite significant advancements in understanding matter, the Standard Model remains incomplete. Numerous unanswered questions persist, and theories are yet to be proven or refuted.

2.2 Standard Model of Particle Physics

The Standard Model of particle physics is a theory that describes the fundamental interactions and elementary particles. Its development started in 1970, resulting from various theories and experimental studies. The Standard Model's success lies in its ability to predict a broad range of phenomena, approximating the nature at distance scales as small as 10^{-18} m [8]. Much like the periodic table in chemistry enables predictions about the properties of unstudied elements, the Standard Model explains particle interactions and has successfully predicted particles discovered in experiments. Nevertheless, the Standard Model has limitations, forcing the exploration of new theories to achieve a more fundamental theory.

Particle physicists describe nature using four fundamental forces : gravity, the weak force, electromagnetism and the strong force [9].

Gravity defines the attraction between objects with mass, initially described by Isaac Newton in his book Principia Mathematica [10]. Albert Einstein later augmented these observations with his general theory of relativity in 1916 [11], conceptualizing gravity as the curvature of spacetime caused by the mass and energy of objects. While gravity influences the motion of planets, stars and galaxies, it is notably the weakest of the fundamental forces, especially at atomic scales, where other forces overshadow its effects.

The weak force, or weak nuclear interaction, is responsible for particle decay, transforming

one subatomic particle into another. For instance, when a neutrino interacts closely with a neutron, the neutron transitions into a proton, and the neutrino transforms into an electron. This force is also present in the nuclear fusion reactions powering the sun.

The electromagnetic force operates between charged particles, incorporating electric and magnetic forces. The magnetic component acts when opposite charges attract one another, and the same charges are repelled from each other. The electric component creates a field by which the charges can influence each other. Charged particles in motion generate a magnetic field. This force is responsible for friction, elasticity, the normal force and the force holding solids together [9].

The strong nuclear force binds fundamental particles to form larger particles, holding quarks together to create protons and neutrons. It is the strongest fundamental force and part of the force that keeps protons and neutrons within an atom's nucleus.

The Standard Model of particle physics describes all except gravity from the four fundamental forces in the language of quantum gauge field theories. The Standard Model sorts elementary particles based on their charges and outlines their interaction via the fundamental forces. The electromagnetic interaction, governed by quantum electrodynamics (QED), influences particles with an electric charge. The weak interaction, described by quantum flavor dynamics (QFD), influences particles with a weak charge. The weak and electromagnetic forces are unified in the Standard Model through a single electroweak gauge theory. Finally, the strong interaction, governed by quantum chromodynamics (QCD), influences particles with a color charge.

Particles in the Standard Model include fermions and their antiparticles, having equal charge quantities but opposite charges. Fermions, which exhibit half-integer spin, are categorized into quarks and leptons. A spin is the intrinsic angular momentum of a particle. Quarks, such as up (u), down (d), charm (c), strange (s), top (t) and bottom (b), have a color charge and interact with the strong force. Leptons, including the electron (e), muon (μ), tau (τ), electron-neutrino (ν_e), muon-neutrino (ν_μ) and tau-neutrino (ν_τ), have either a neutral charge (neutrinos) or a negative unity charge. Fermions are organized into three families, featuring two quarks and two leptons. The first family's fermions constitute matter in nature, such as electrons, protons (composed of two u quarks and one d quark) and neutrons (composed of two d quarks and one u quark). The heavier particles of the second and third families are short-lived, decaying into quarks and leptons of the first family via the weak force.

Massless particles called photons (γ) mediate interactions in QED. In QCD, gluons (g), also massless, facilitate interactions by carrying color charge and binding quarks to form hadrons. Baryons, consisting of three quarks with distinct colors, and mesons, comprising one quark and one antiquark, exemplify the particles created through the strong force. The weak force involves interactions mediated by charged W^+, W^- and neutral Z^0 bosons.

While characterized by a high degree of symmetry [8], the Standard Model exhibits symmetry breaking in certain particles due to the Higgs field. Particles interacting with the Higgs field acquire mass, as they cannot travel at the speed of light. The Higgs boson particle (H) couples to any mass particle, including itself [12]. Figure 2.2 illustrates the elementary particles of the Standard Model with their main known characteristics.

The mathematical formulation of the Standard Model is complex. However, it is encoded in a concise four-line description known as the Lagrangian (Equation 2.1). As a quantum field theory, the Standard Model revolves around quantum fields, with particle excitations representing the elementary particles [12]. The Lagrangian delineates the kinematics and dynamics of the quantum system, presented here in a simplified form. It underscores that the Standard Model is grounded in a mathematical framework capable of predicting the behavior of known quantum particles. A more detailed exposition of this formula is available in [12].

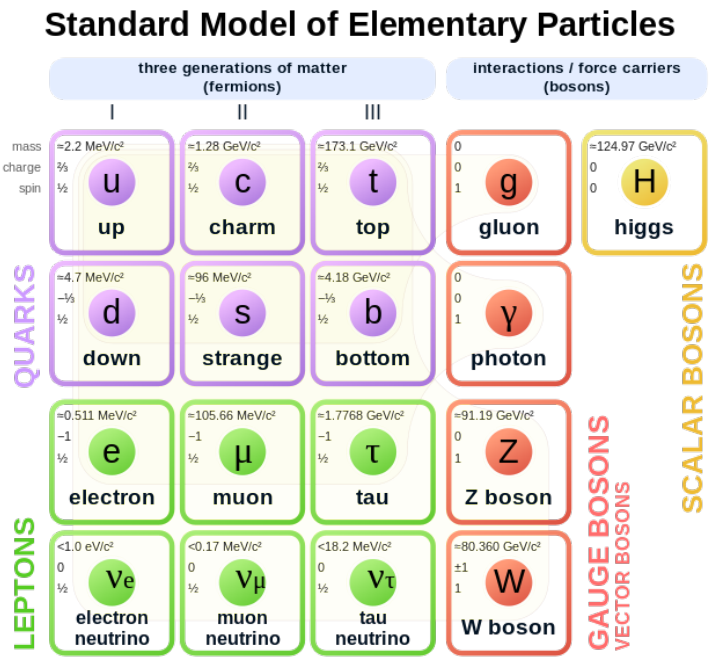

FIGURE 2.2 – *Summary of the Standard Model of particle physics [13].*

$$\begin{aligned}\mathcal{L} = & -\frac{1}{4}F_{\mu\nu}F^{\mu\nu} \\ & + i\bar{\psi}D\psi + h.c. \\ & + \psi_i y_{ij}\psi_j\phi + h.c. \\ & + |D_\mu\phi|^2 - V(\phi)\end{aligned} \tag{2.1}$$

The Standard Model is the most important high-energy physics theory but has several limitations. Notably, it lacks a particle for gravitational interactions and explains only 5% of the universe. Dark matter (25%) and dark energy (70%) remain unaccounted for in the Standard Model [12]. Physicists are actively exploring modifications or improvements, with Supersymmetry emerging as one of the theories under consideration. This theory declares a connection between bosons and fermions, introducing new particles that may address some of the Standard Model's problems [8].

2.3 Accelerators for Particle Physics

Particle accelerators play a crucial role in particle physics, taking charged particles to velocities near the speed of light and high energies. These accelerators enable the exploration of particle nature and behavior under extreme conditions, emulating conditions similar to those present in the early universe, such as high energies and low temperatures. Through collisions with targets or opposing particles, accelerated particles generate interactions that help physicists comprehend the properties of matter and the fundamental forces governing our universe.

When particles collide at high energies, they produce more primitive particles that compose the matter. These newly formed particles exist briefly before decaying into other, more common particles. Accelerators precisely measure these newly generated particles' mass, charge and

momentum.

There are two primary types of particle accelerators. Linear accelerators (LINACs) employ radiofrequency cavities to accelerate the particles in a straight line, often serving as injectors for larger accelerators. An example is the proposed International Linear Collider (ILC) [14]. Circular accelerators, such as cyclotrons and synchrotrons, utilize magnetic fields to bend particle trajectories in a circular path. As particles follow the same circuit, they gain energy with each revolution. However, the magnetic fields must be robust enough to maintain particles in their circular orbit ; otherwise, further energy boosts become unfeasible. Synchrotrons can accelerate particles in opposite directions, leading to collisions within large detectors for energy measurement.

In particle physics, Luminosity is a crucial parameter, characterizing the intensity of particle collisions in an accelerator. It quantifies the rate at which particles collide within a specific volume, offering insights into the performance and capabilities of particle colliders. Luminosity depends on factors such as beam energy, the number of particles in each beam and the cross-sectional area of the beams at the interaction point. Luminosity is measured in units of $cm^{-2}s^{-1}$, representing the number of collisions per second in a particle beam with a cross-sectional area. Integrated Luminosity measures the total number of particle collisions accumulated over a specific period in a particle physics experiment and is usually expressed in fb^{-1}, where 1 fb corresponds to $10^{-39}\ cm^2$.

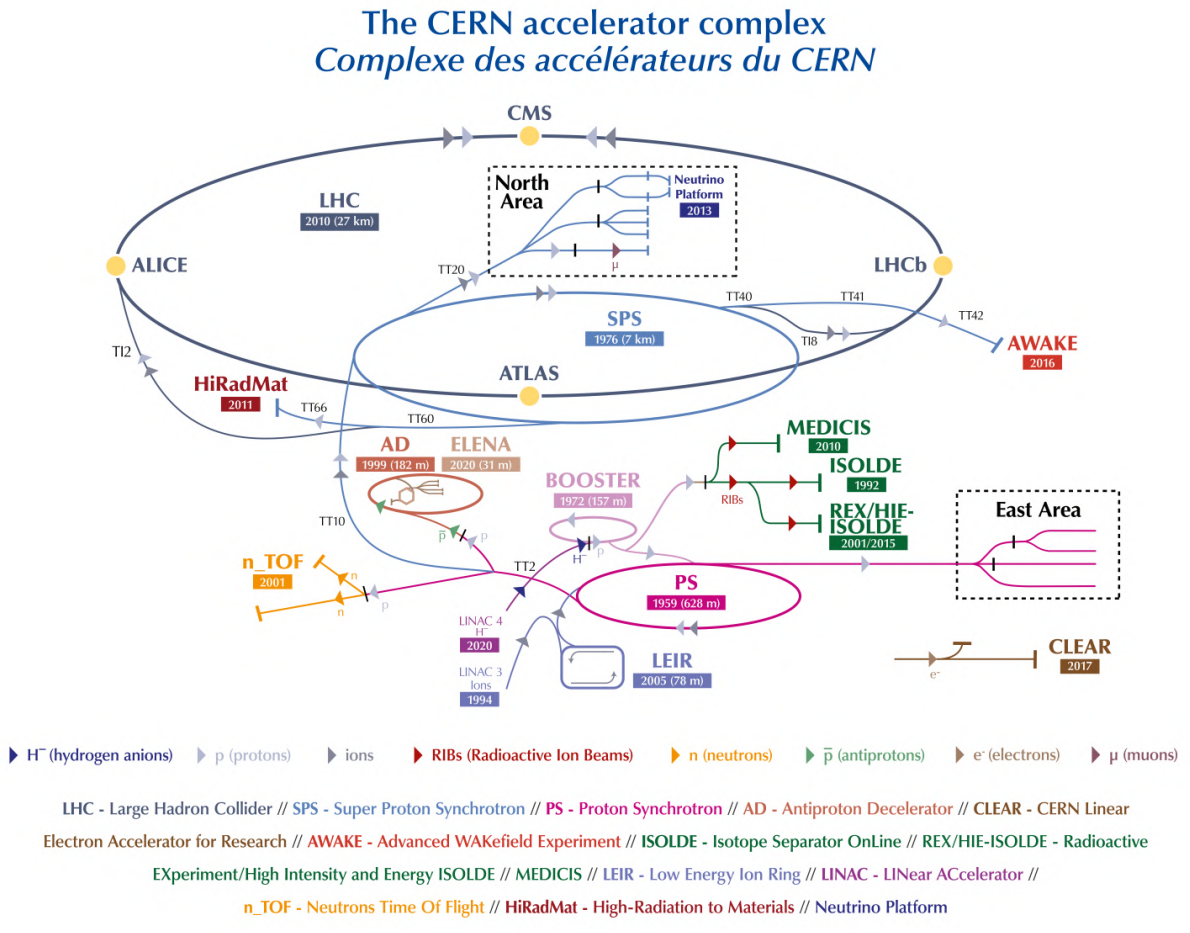

FIGURE 2.3 – *The CERN accelerator complex [19].*

One example of an accelerator is the Large Hadron Collider (LHC) [15] of CERN. Operational since 2010, the LHC accelerates proton beams in its underground ring with a diameter of 27 km to a beam energy of 7 TeV. Four main detectors (ALICE, ATLAS, CMS and LHCb) capture energy from proton-proton collisions. The collision energy produced is 13 TeV, with a nominal instantaneous luminosity of $L = 1 \times 10^{34}\ cm^{-2}s^{-1}$. In 2012, ATLAS and CMS discovered the Higgs boson, the last missing particle in the current Standard Model of particle physics ([16], [17]). In 2017, the beam cross-section was reduced by 40%, increasing collision probability and producing a luminosity of $L = 1.58 \times 10^{34}\ cm^{-2}s^{-1}$.

Figure 2.3 illustrates CERN's accelerator complex. The Linear Accelerator 4 (LINAC 4) [18] accelerates negative hydrogen ions to high energies, serving as the source for LHC's proton beams. Within LINAC 4, hydrogen ions, composed of a hydrogen atom with an additional electron, reach speeds of 160 MeV before proceeding to the Proton Synchrotron booster, which leaves only protons accelerated to 2 GeV to the Proton Synchrotron (PS). After passing through the PS, the particles advance to the Super Proton Synchrotron, reaching up to 450 GeV, ultimately arriving at the LHC, where particles are accelerated to 6.5 TeV and collisions occur at 13 TeV.

2.3.1 The High Luminosity Large Hadron Collider

The LHC stands as one of the most significant achievements in physics in recent years, particularly for its discovery of the Higgs boson. Although the LHC continues to contribute to in-depth investigations of the Higgs boson and the Standard Model, its operation is ending. To address this, the development of the new High Luminosity Large Hadron Collider (HL-LHC) is underway. The HL-LHC is prepared to enhance measurements within the Standard Model and facilitate explorations of physics beyond its confines.

The primary objective of the HL-LHC is to achieve a peak luminosity of $L = 5 \times 10^{34}\ cm^{-2}s^{-1}$. In its initial operations, the LHC achieved 20 collisions per bunch crossing (BX = 25 ns). Subsequently, the number of collisions per BX increased to 60 in 2017. Projections for the HL-LHC anticipate reaching 140 collisions per BX with a peak at 200 collisions. The goal is to reach an integrated luminosity of 300 fb^{-1} annually, accumulating to 3000 fb^{-1} after a decade of operation. These ambitious objectives necessitate upgrading key components, including new-technology superconducting magnets and current leads [20].

The anticipated increase in Luminosity will improve the precision of couplings between particles. This enhancement is crucial for meticulously measuring the properties of the Higgs boson, as any deviations from the Standard Model could indicate the existence of new physics. Additionally, the HL-LHC is pointed to investigate the rare decay $H \rightarrow \mu\mu$ involving particles of the second family. Moreover, the upgraded Luminosity opens avenues for exploring theories involving extra dimensions or Supersymmetry. There is considerable anticipation surrounding Supersymmetry studies, as it is believed to represent the next phase beyond the Standard Model, providing explanations for the light mass of the Higgs boson and offering a potential candidate for dark matter [20].

2.3.2 The Compact Muon Solenoid Experiment

The Compact Muon Solenoid (CMS) experiment is situated at CERN's LHC, approximately 100 meters underground near the French village of Cessy [21]. Its primary goal is to understand the nature of electroweak symmetry via the Higgs mechanism. Additionally, it actively seeks discoveries that could validate novel theories, such as Supersymmetry or those involving

extra dimensions. It investigates the particles that can be produced at the TeV energy scale to accomplish those objectives.

The CMS detector employs a trace detection concept featuring multiple layers to capture collisions-generated particles. Protons, accelerated by the LHC, collide at high energies near the CMS detector's focal point. Figure 2.4 provides a 3D view of the CMS detector. The initial LHC design aims to generate 20 collisions every 25 ns, producing approximately 1000 charged particles. Managing this amount of data and overcoming pileup effects needs high-granularity detectors with excellent time resolution. Consequently, the detector comprises millions of detector channels requiring meticulous synchronization [21].

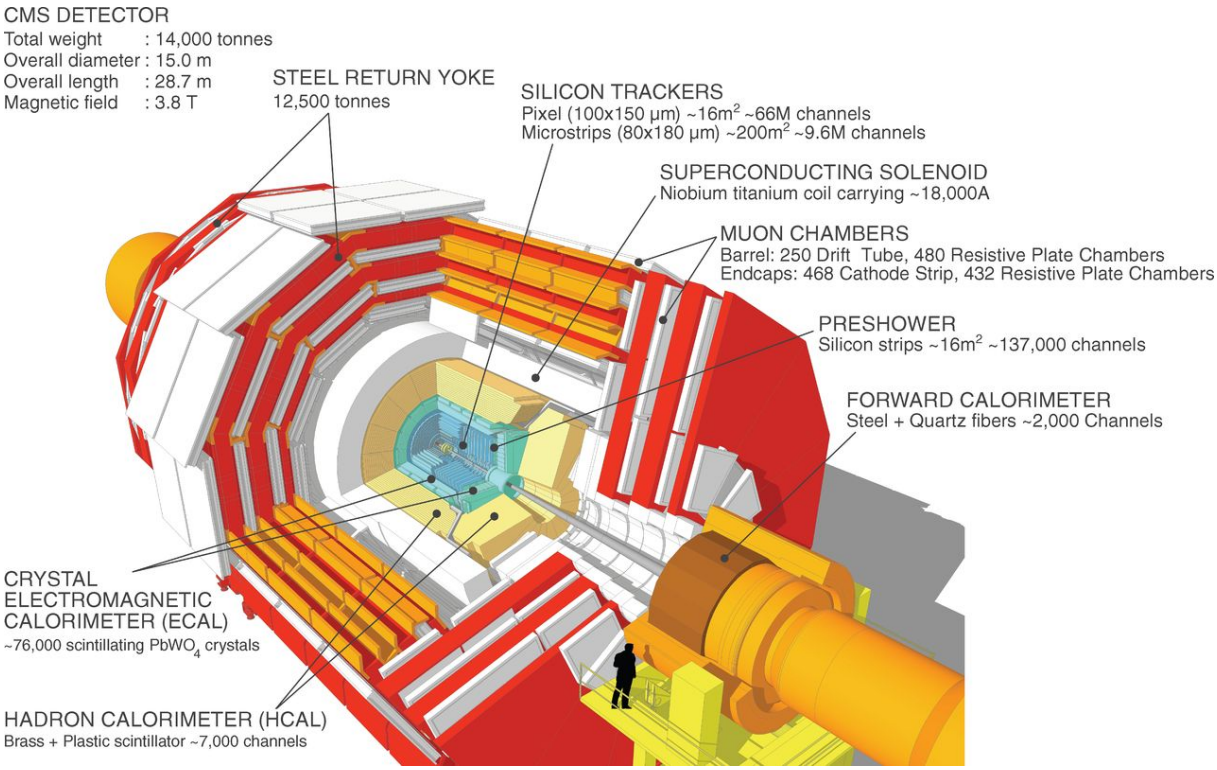

FIGURE 2.4 – *3D view of the CMS detector showing its main components [22].*

Figure 2.5 illustrates one slice of the CMS detector. A 4-T superconducting solenoid magnet is placed at the detector's center, bending the paths of charged particles to measure their momentum. At the magnet's core, the detector includes a Tracker detector, an Electromagnetic Calorimeter (CE-E) and a Hadron Calorimeter (CE-H). Surrounding the magnet are muon chambers and the Forward Calorimeter. In addition to particle energy, the pseudorapidity η is a valuable variable expressing the particle's trajectory angle relative to the beamline. The CMS tracking system aims for high-resolution and efficient reconstruction of electrons, hadrons and muons, achieving better than 98% efficiency with $|\eta| < 2.5$.

Given the LHC's collision rate of every 25 ns, the trigger system plays a crucial role in discriminating relevant data. Based on silicon detector technology, it quickly chooses relevant events for further analysis, reducing the vast data rate to approximately 100 events per second [21]. Figure 2.6 depicts the pseudorapidity coverage of the inner tracker.

The CE-E is a hermetic homogeneous calorimeter made of Lead-tungstate crystals. The configuration of the magnetic field and the radiation levels in the different parts of CE-E led to the use of Avalanche Photodiodes (APDs) in the central barrel part and vacuum phototriodes (VPTs) in the endcaps [21]. The CE-H employs plastic scintillators to measure hadron jets,

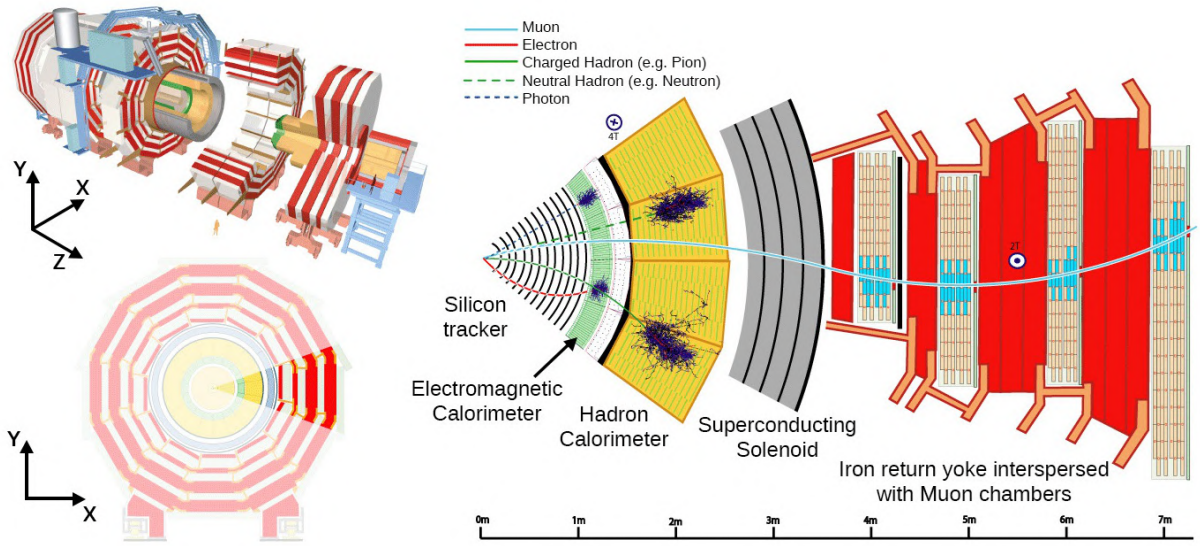

FIGURE 2.5 – *Summary of particle detection in one slice of the CMS detector [23].*

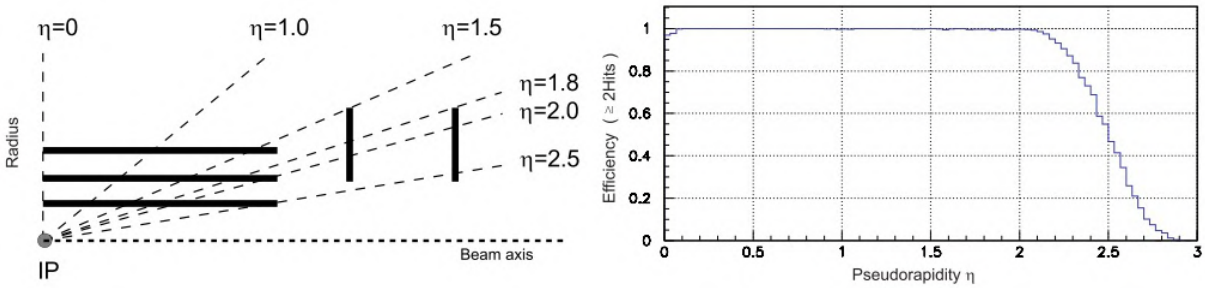

FIGURE 2.6 – *Geometrical layout of the pixel detector of the CMS tracker and hit coverage as a function of pseudorapidity η [21].*

neutrinos and exotic particles through missing transverse energy.

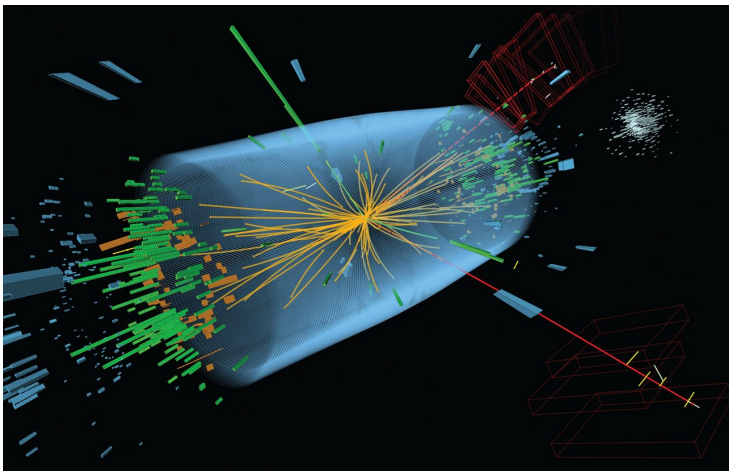

FIGURE 2.7 – *Event recorded with the CMS detector in 2012 from a proton-proton collision at the energy of 8 TeV. It shows an event of the Higgs boson decay to a pair of Z bosons that subsequently decay to a pair of electrons (green lines) and a pair of muons (red lines) [22].*

The muon system serves three primary purposes : muon detection, momentum measurement and participation in triggering. Gaseous particle detectors assist in muon identification, enabling the system to detect processes like the anticipated decay of $H \rightarrow ZZ$ or $H \rightarrow ZZ*$, resulting in four leptons. Figure 2.7 presents an example of an event recorded with the CMS detector in 2012 from a proton-proton collision at an energy of 8 TeV. It depicts an event of $H \rightarrow ZZ$ that subsequently decays into a pair of electrons, visible as green lines in the center, and a pair of muons passing through the detectors, presented as red lines.

2.4 Calorimeters for particle physics

Calorimeters are detectors designed to measure the energy of high-energy particles produced in particle collisions. Following a collision, particles deposit their energy in various detectors as they pass through the calorimeter. Different particles interact with different materials, and the measured energy reflects the total absorption in matter. When a high-energy particle interacts with the absorber material, it initiates a shower of secondary particles.

The absorber material is enveloped by an active medium sensitive to the produced secondary particles. The active medium absorbs the energy and simultaneously generates the measured signal. The active medium can be scintillating crystals, liquids, or gaseous detectors. The signals generated are proportional to the energy deposited by the incident particles. For example, calorimeters using scintillating crystals read the light emitted from the scintillation process, with the light's intensity being proportional to the deposited energy. These signals can then be detected by photomultiplier tubes or silicon photomultipliers (SiPMs) and converted into measurable quantities.

In high-energy physics detectors, a shower's energy is determined by the full jet measured in the calorimeter's active material. Both tracking detectors and calorimeters are essential for event reconstruction since neutral particles produce a signal only in calorimeters. Simultaneously, momentum measurements obtain the energy of all other charged particles in the tracker with better resolution than calorimeters. Ultimately, both detectors must combine the information of measured signals, and the total reconstructed energy is the sum of all particle energies [5].

Calorimeters require precise calibration to convert the produced signals into accurate energy measurements. Typically, the detector is calibrated using known energy sources or standard particle beams.

There are two types of calorimeters : Electromagnetic and Hadronic Calorimeters. Electromagnetic calorimeters are optimized to measure the energy of electrons and photons. They employ materials that interact strongly with these particles, leading to the production of electromagnetic showers. Electrons and positrons are generated in electromagnetic showers and create more through ionization and radiation, forming a cascade of particles or showers. In contrast, Hadronic Calorimeters are designed to measure the energy of hadrons such as protons, neutrons, or mesons. They utilize dense materials that interact strongly with hadrons.

The main interactions of particles measured by calorimeters are electromagnetic and hadron showers. Electromagnetic showers are initiated by a photon entering the calorimeter volume, as depicted in Figure 2.8 a). In this type of shower, secondary particles lose most of their energy through direct ionization, annihilation for positrons and Coulomb-scattering for photons. Afterward, no additional secondary particles are generated, and the electrons and positrons are captured within one radiation length. Contrarily, hadron showers (Figure 2.8 b)) involve strong interactions with the absorber nuclei. The initial energy produces secondary particles generated in nuclear reactions, traveling a longer distance than in electromagnetic showers [5].

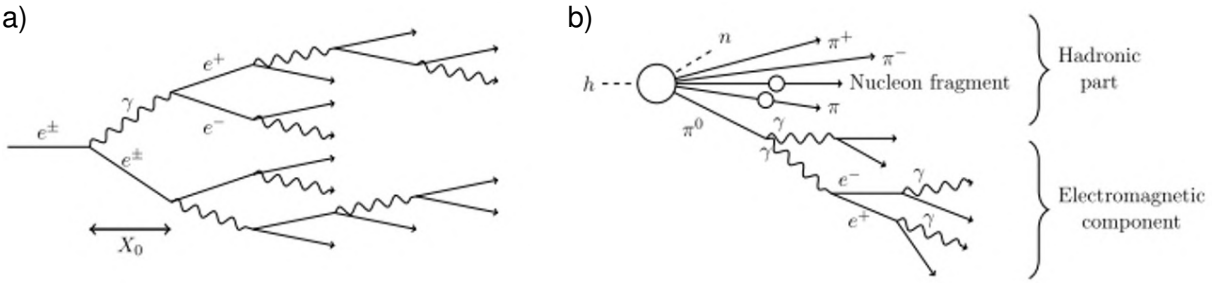

FIGURE 2.8 – *Formation of showers in the calorimeter. a) Electromagnetic shower. b) Hadronic shower with the electromagnetic component [5].*

2.4.1 The High Granularity Calorimeter of CMS

With excellent imaging capabilities, Calorimeters capture precise information to reconstruct all particles produced in a collision. However, new particle physics projects require even more precise systems with novel techniques and methods to address existing questions about the current Standard Model.

Electronic laboratories are actively developing more precise technology and circuit designs to enhance collider resolution in the search for new physics. As classical calorimeters become outdated, ongoing projects aim to improve measurement precision by optimizing particle flow algorithms. The new calorimeters must be highly granular in imaging detection, incorporated into compact systems [5].

The CMS experiment continues to make significant advances and discoveries, describing the observed fundamental particles and their interactions within the Standard Model. Currently, the detector is operating at the Large Hadron Collider at CERN. However, although this collider has achieved excellent physics results, the new HL-LHC points to developing better detectors that can manage the increasing Luminosity and read the collisions per bunch crossing to fulfill the specifications of the new and complex future experiments planned. The HL-LHC will have ten times more Luminosity than the current LHC, creating challenges such as higher radiation levels, more simultaneous interactions and increased particle fluxes [6]. The High Granularity Calorimeter (HGCAL) is currently under development and is expected to start operations in the new HL-LHC in 2029.

The HGCAL is an imaging calorimeter comprising an electromagnetic and hadronic compartment. The complexity of calorimetry provides substantial information for pattern recognition in experiments [1]. Figure 2.9 illustrates the simulated energy deposits from photon showers in a CMS simulation of HGCAL. The HGCAL offers information in five dimensions : energy, x, y, z and time. This information is ideal for particle-flow reconstruction, enabling the individual reconstruction of electromagnetic and hadronic showers. The tracker allows for the refinement of electron and converted photon reconstruction. The calorimeter's granularity also facilitates excellent identification of electrons, protons and muon performance [1].

One example of calorimeter performance is shown in Figure 2.10, where the reconstructed mass of photon pairs from $H \rightarrow \gamma\gamma$ is noticeable [1].

HGCAL plays a crucial role in identifying and measuring quarks, gluons and neutrinos by determining the energy and direction of jets and missing transverse energy flow in events. Silicon detectors will read the particle energy produced by the collision in the CE-E and front part of CE-H, and silicon photomultipliers will be used in the back hadronic part.

A photomultiplier consists of a photocathode and an electron multiplier. Photons absorbed in the photocathode release electrons proportional to the number of photons coming from the

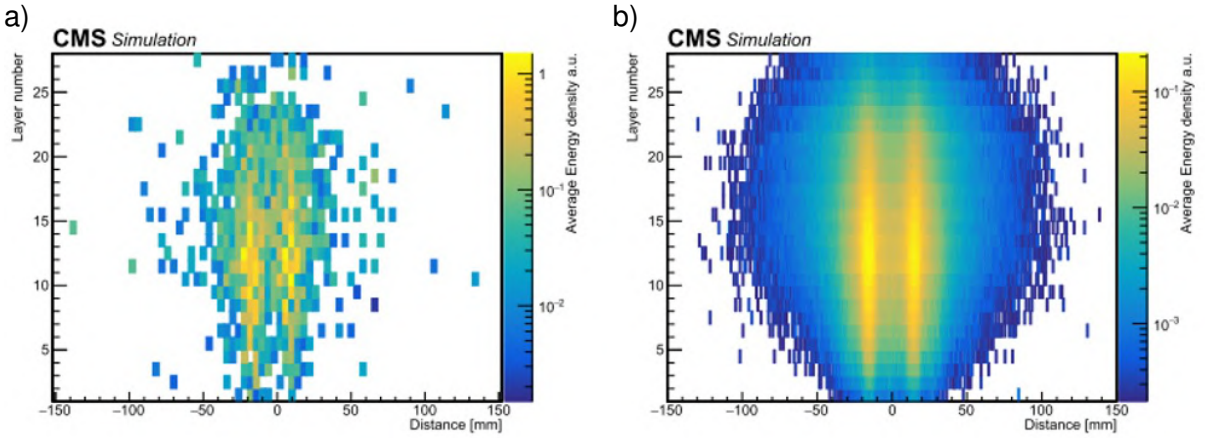

FIGURE 2.9 – *Energy deposited in HGCAL cells by pairs of unconverted photons ; a) a single event containing a pair of photons ; b) several thousand of such events [2].*

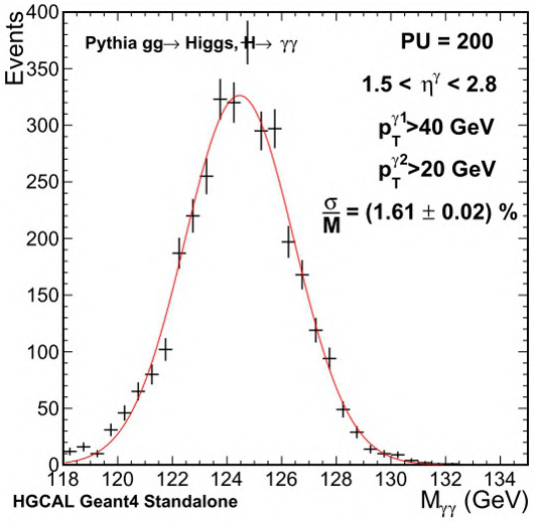

FIGURE 2.10 – *Reconstructed mass of photon pairs from $H \to \gamma\gamma$ [2].*

scintillator ; the electrical signal is a current pulse proportional to the particle's energy. This current pulse, integrated over time, contains the signal charge. The pulse shape does not change with the charge ; only the peak amplitude changes and provides information about the signal charge [24]. The two ASICs developed by OMEGA facilitate the readout of the HGCAL detectors. HGCROC reads out the silicon pads of the electromagnetic and front hadronic sections, while H2GCROC reads out the SiPMs coupled to the scintillating tiles of the back hadronic sections.

Table 2.1 details the number of channels and corresponding ASICs for each part of the calorimeter. The back hadronic part is expected to have around 9000 ASICs to read out the more than 380,000 SiPMs on the plastic scintillators [2]. Scintillation detectors use indirect detection, converting absorbed energy into visible light. The number of scintillation photons is proportional to the absorbed energy. Subsequently, the photomultiplier detects the scintillation light.

	CE-E	CE-H	
	Si	Si	Scintillator
Area [m²]	368	215	487
Channels [k]	3916	1939	389
Si modules (Tileboard)	16008	8868	(3960)
Partial modules	1008	1452	-
72 channel ASICs	60324	31596	8496

TABLE 2.1 – *HGCAL number of channels and ASICs. [2].*

2.5 Importance of Timing Measurements in High-Energy Physics

The time data can be used to implement software compensation for the calorimeter response, assisting in the event reconstruction. Simulations presented in [25] demonstrate how the time compensation may improve the shower decomposition in the particle algorithm, reducing the process's uncertainties.

Performing a time-of-arrival measurement in a calorimeter layer allows us to assign a precise time for both charged particles and photons. This information, coupled with energy measurements, reduces the inclusion of pileup particles in event reconstruction, as the spread of the collision time of pileup interactions is about 200 ps [26].

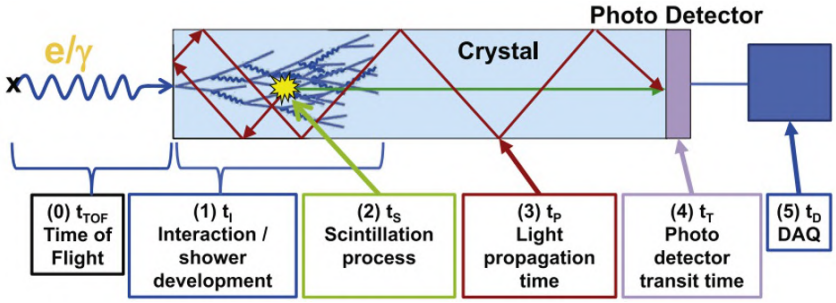

FIGURE 2.11 – *Schematic of the most relevant contributions of timing measurements in a monolithic, large scintillating crystal [26].*

The time scales associated with the timing measurement using a monolithic crystal calorimeter are displayed in Figure 2.11. When the photon or electron enters the crystal, it travels at the speed of light, interacting and creating a shower-producing scintillation light. The time t_l corresponds to the time between the entry of the photon and the first interaction. The scintillation process has a duration of t_S. The time t_P is associated with the propagation of the scintillation light from the point of interaction to the photodetector. After that, the photodetector converts the scintillation light into an electrical signal. The duration of this process corresponds to the photodetector signal transit time t_T. Finally, the time necessary for the data acquisition (DAQ) is the t_D. All these periods contribute to the total time resolution. The new information will improve the datasets necessary to perform precise measurements of the Higgs couplings, probe rare Higgs processes, study W bosons and search for physics beyond the standard model [26].

Challenges in timing measurements for particle physics are numerous, considering factors such as photon statistics, photon transport, rise time, decay time and the quantum efficiency of photodetectors. It has been observed [27] that a circuit, including an amplifier connected to a discriminator, can mitigate the effects of these factors, leading to improved timing measurements for SiPM.

However, timing measurements for particle physics face a unique challenge, as the delay and jitter of ASICs can be on the same order of magnitude as the timing resolution. Increasing the resolution of the next stage (time-to-digital converter) requires a significant increment in area and power consumption. A potential solution is to enhance the conditioning of the input signal, reducing noise and improving linearity in the first stage of the chain [28].

The jitter can be measured with the time difference between the chip's output signals and the trigger from the wave generator. The time resolution depends on the threshold level settings. Thus, the threshold must be lower than the Minimum Ionizing Particle (MIP). The noise of the readings sets the limitation for threshold position. The precision of timing measurement depends on the intrinsic performance of the complete chain, encompassing the sensor, amplifier, discriminator and TDC, together with the clock distribution system [1].

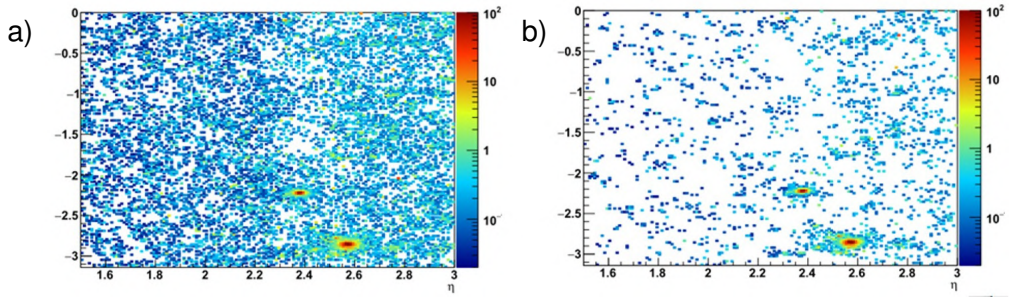

FIGURE 2.12 – *Hits of a vector boson fusion $H \rightarrow \gamma\gamma$ event with charge > 12 fC; a) without timing requirement and b) after removal of hits with $|\Delta t| > 90\ ps$. [2]*

In Higgs boson production, the vertex that decays into two photons poses a significant challenge to measure accurately. Timing information can be utilized to localize the vertex [29]. For example, Figure 2.12 illustrates the hits with charge > 12 fC of a vector boson fusion $H \rightarrow \gamma\gamma$ event. Figure 2.12 a) shows all the pileups without a timing requirement, and Figure 2.12 b) demonstrates the improved jet reconstruction and energy estimation after removing hits with $|\Delta t| > 90\ ps$ due to time discrimination, resulting in less impact from complete pileup [1].

2.6 Role of SiPM Detectors in the CMS HGCAL Experiment

The new HGCAL (Figure 2.13) comprises two endcaps, each with 26 electromagnetic layers and 21 layers of the hadronic calorimeter. The CE-E region and the first part of the CE-H will use hexagonal silicon modules with more than 6 million detector channels in approximately 620 m² of silicon. The layers combine silicon modules with trapezoidal scintillator modules in the back part of the hadronic calorimeter. The scintillator modules are composed of Tileboard printed circuit boards (PCBs) that use plastic scintillator tiles and SiPMs containing 380,000 detector channels in a scintillator area of approximately 480 m² [30].

The irradiation levels expected at the experiment defined the decision to use silicon detectors and SiPMs. SiPMs were placed in every part of HGCAL where they can operate and maintain good behavior after the expected radiation. Tileboards of different sizes are connected to form a 10° detector unit. Six units are placed next to each other and assembled with silicon modules into cassettes that cover 60°. Six cassettes complete the calorimeter around the beam. Figure 2.14 presents one of the 60° cassettes with silicon modules and Tileboards. In HGCAL, the detectors will be operated at -30 °C and have a magnetic field of up to 3.8 T. The cooling of the Tileboards is made by a copper layer where the boards are mounted [30].

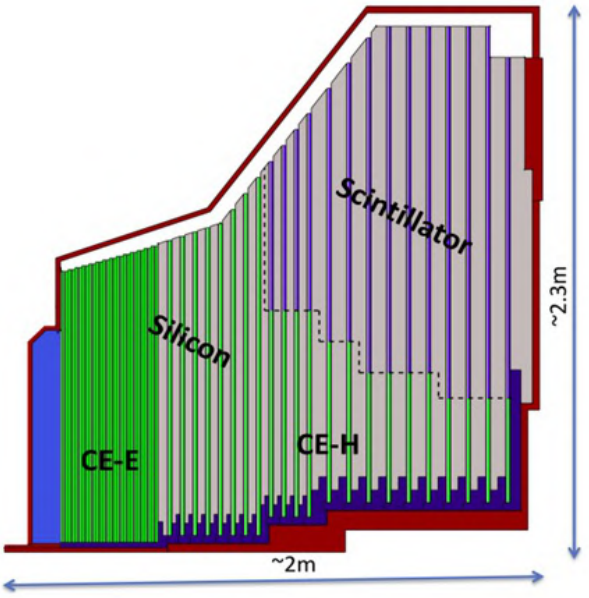

FIGURE 2.13 – *Side view of the High granularity calorimeter of CMS [31].*

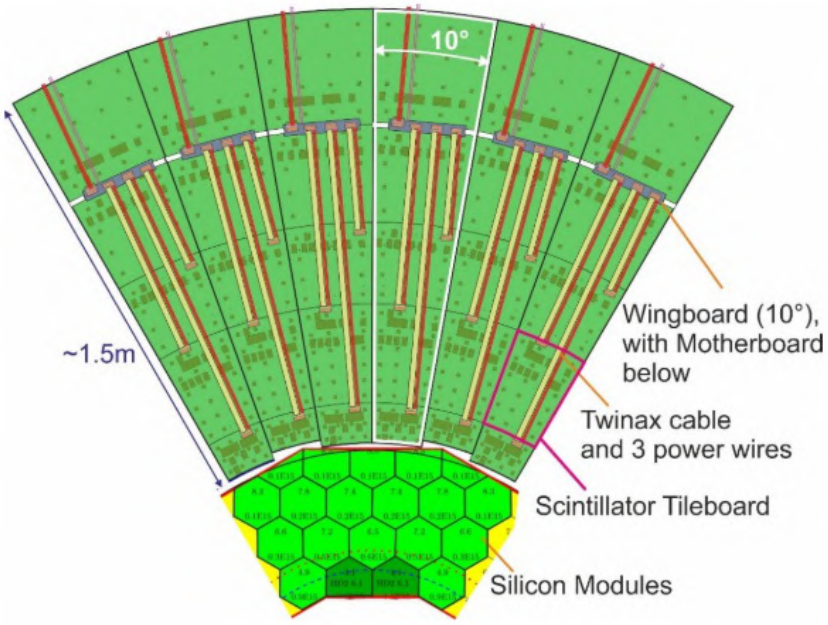

FIGURE 2.14 – *Top view to a mixed 60° cassette of a detector layer, including scintillator tileboards of the CE-H on top and the silicon modules of the CE-E at the bottom [30].*

The Tileboards are designed in 8 different sizes to build the cassettes. The number of SiPMs on a Tileboard varies from 48 to 96. The H2GCROC ASIC can read up to 72 channels so some Tileboards will use two H2GCROC ASICs. Linear regulators generate all noise-sensitive supply voltages of the chip. The power of the Tileboards is made thanks to two DC-DC converters (bPOL12 [32]) that take 10 V as input and provide voltages of 1.5 V and 3.3 V. The ASIC ALDO2 [33] generates the SiPM bias voltage. The Tileboard uses the GBT-SCA [34] that monitors all supply voltages, SiPM bias voltage and temperature, and communicates with the H2GCROC ASIC.

2.6.1 SiPM-on-Tile

The SiPM and the tile form the SiPM-on-tile detector ; Figure 2.15 presents the tile design. They have a cavity for the SiPMs and will be individually wrapped. Each detector on the board has an ultraviolet LED next to the SiPM. This LED is used for calibration and to monitor the SiPM gain. The H2GCROC can trigger the LED system to send an optical pulse of 6 ns into the scintillating tiles. An external DC voltage from the motherboard adjusts the LED's voltage amplitude to control the light intensity.

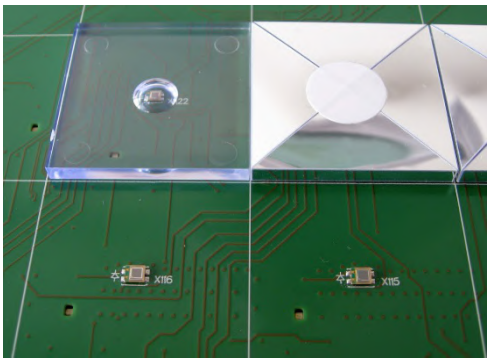

FIGURE 2.15 – *CALICE scintillator tiles with a central dimple, wrapped and unwrapped, mounted on SiPMs and used as a prototype for the HGCAL project [35].*

The measured noise depends on the gain configured in the H2GCROC ASIC and the capacitance of the SiPM, which increases with the area. In HGCAL, regions with higher radiation levels will experience more damage to the scintillator and the SiPM. Therefore, the detectors must capture as many photons from the scintillator as possible in these zones. The number of photons captured increases linearly with the SiPM area, while the noise increases only with the square root of the SiPM area.

Although larger SiPMs produce a higher signal-to-noise ratio (SNR), smaller SiPMs are cheaper. During the project definition stage, two SiPM areas were selected : 2 mm² and 4 mm². The smaller SiPMs were planned to be used in areas with lower radiation levels. The two SiPM sizes were compared by calculating the Light Yield of both detectors. The Light Yield utilizes the amplitude signal generated by the MIP and the SiPM gain obtained from calibration using the following equation :

$$Light\_Yield[p.e.] = \frac{MIP_{amplitude}[ADC]}{SiPMgain[ADC/p.e.]} \tag{2.2}$$

The system is designed to have a $SNR > 3$ for the MIP during the HGCAL lifetime [36]. From the H2GCROC ASIC, the MIP is measured in ADC counts, and the SiPM gain is the ADC counts produced by one photon. The SiPM-on-tile with SiPMs of the selected areas was analyzed in [30]. Figure 2.16 presents the Light Yield measured in photons ; The larger SiPM produces a higher Light Yield even with the noise increment coming from its higher capacitance. This increment comes from the large amount of light absorbed by the large detector area.

The increase in Light Yield observed in larger SiPM detectors led to a discussion on incrementing the selected SiPM areas for the calorimeter. Recent test measurements aim to use 9 mm² SiPMs for all scintillator tiles, as the price difference compared to 2 mm² and 4 mm² SiPMs was found to be relatively small [37].

The information from each H2GCROC is sent by two data e-links and four trigger e-links at 1.28 Gbps. The ECON-D reads the data links and performs zero suppression before trans-

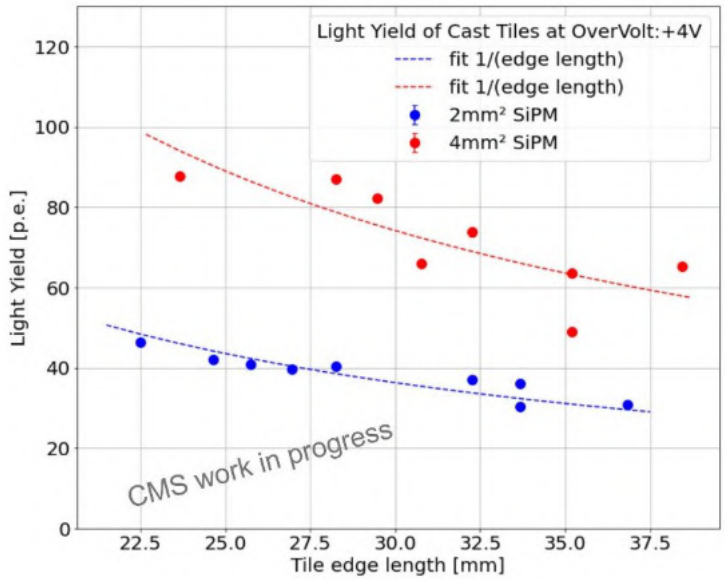

FIGURE 2.16 – *Light Yield of scintillator tiles using the 2 mm² and 4 mm² SiPMs [30].*

mission. The ECON-T takes the trigger information from H2GCROC to select and compress interesting data using preprogrammed trigger algorithms. One LpGBT ASIC [38] per ECON board collects the data.

2.7 Requirements for the very Front-End ASIC for SiPM Readout on HGCAL

Pointing to the best detectors also increases expectations for the behavior of front-end electronics, especially regarding radiation levels. For this reason, new chips are being developed to handle the increased amount of data at faster speeds, improving radiation tolerance and reducing noise for precise measurements. Application-specific integrated circuits (ASICs) for particle physics require an analog front-end to convert the charge signal to a voltage with a defined shape, enabling digitization with the use of analog-to-digital converters (ADCs) [5]. The front-end electronics must generate output signals with low noise, a large dynamic range, integral linearity and high-precision time measurements.

The ASIC design for calorimeters is a challenging task. Today, advanced technologies and components with small sizes and versatile functions can be combined to develop custom electronics with analog and digital designs, all on the same chip. Mixed-signal designs, which read analog signals and digitize information, are known as system-on-chip (SoC) when they integrate all functionalities required for a specific application.

The measurement of charged particle tracks requires the measurement of millions of pixels, imposing demanding requirements on front-end electronics. Achieving a large dynamic range and high-speed designs for pixel readout, especially in applications such as calorimeters, is crucial. The readout electronics follow the structure outlined in Figure 2.17. They use a preamplifier coupled with a shaper to read the energy transformed into data by an ADC. Time measurements are obtained from the preamplifier output, which reads the time through a discriminator and a time-to-digital converter. The SoC selects meaningful data, saves them in memories and sends them for further analysis.

Front-end electronics aim to receive the electrical signal from the detector as a short current

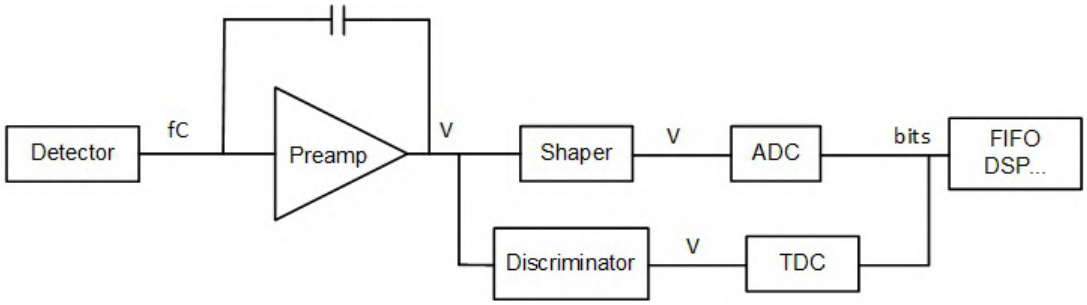

FIGURE 2.17 – *Common structure for front-end electronics in particle physics*

pulse and process the signal to obtain valuable data. The most critical parameters in front-end electronics design include the minimum detectable signal, energy measurement, time-of-arrival, linearity of measurements, radiation resistance and low power consumption [6]. Depending on the application, the design needs to optimize some requirements over others. The output signal must also be digitized and stored for subsequent analysis.

In the current mode, silicon sensors are good candidates for reconstructing the particles arriving at the calorimeter, thanks to their hard radiation tolerance. However, they suffer from poor linearity performance [39]. Additionally, the characteristics of silicon sensors add an extra dimension to event reconstruction. The fast response of silicon sensors and the front-end electronics allow for building a precise timestamp for each event.

In the CMS Experiment, the HGCROC is the electronic chip in development for the new HGCAL. The ASIC has two variants : the HGCROC reads the input charge from silicon sensors in the Electromagnetic calorimeter, and H2GCROC reads the larger current provided by Silicon Photomultipliers in the Hadronic calorimeter. Table 2.2 presents the HGCAL main requirements for both ASICs.

	HGCROC (Si-version)	**H2GCROC (SiPM version)**
Power supplies	1.2 V Analog 1.2 V Digital	1.2 V and 2.5 V Analog 1.2 V Digital
Number of channels	72	72
Charge dynamic range	0.2 fC to 10 pC	160 fC to 320 pC
Timing accuracy for pulses above 3 MIP	< 100 ps	< 100 ps
Leakage current compensation	50 μA	1 mA
Radiation resistance	200 MRad	300 kRad
Special features	DAC to tune input voltage	

TABLE 2.2 – *HGCROC ASIC requirements for HGCAL.*

2.8 Conclusion

The study of the fundamental particles of the Standard Model requires the design of complex detectors, in which ASICs assume a crucial role. This chapter has explained the application of the H2GCROC ASIC, giving the foundation for the subsequent design, analysis and characterization of the chip. The challenges presented by high radiation environments and the pursuit

of precision in measurements emphasize the critical task of developing and understanding advanced electronics. Consequently, the task of translating analog signals into digital information and enabling the extraction of valuable insights from the vast amount of data is a demanding effort that requires years of dedicated work.

In the upcoming sections, we will transition from the theoretical objectives of particle physics to the practical considerations involved in the ASIC design and characterization. The next chapters will explain the methodology employed and the decisions influencing the proposed architecture. Ultimately, the characterization of the last fabricated version of H2GCROC will offer insights into the future performance of HGCAL in 2029 following its installation.

Chapter 3

Analog Electronic design for SiPM detectors

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3.1 Introduction

Reconstructing particles from calorimeters poses a significant challenge in ASIC design. Advanced technologies and compact, multifunctional components can be placed together to develop custom electronics into a single chip, incorporating analog and digital designs. The application's complexity requires increasing the number of functionalities in the chip. In the analog domain, precise blocks need adjustments to several parameters, while the digital part requires memory and complex logic for selecting meaningful data. Additionally, the radiation hardness in an ASIC needs to increase the size of the most impactful transistors in analog blocks and triplicate the digital logic to protect data processing within the chip.

3.2 General Analog Electronic design for detectors

In analog design, complementary metal-oxide-semiconductor technology (CMOS) stands out as the most efficient and widely utilized technology, thanks to the flexibility of MOS transistors as fundamental building blocks. Every analog design starts at the transistor level, involving selecting architecture and transistor sizes to meet the specified requirements.

3.2.1 CMOS technology

MOS transistors are symmetrical four-terminal devices where the gate V_G, source V_S and drain V_D voltages are referenced to the substrate (bulk), as illustrated in Figure 3.1. However, the most common representation in schematics is a three-terminal symbol, where the bulk is typically ignored, assuming it is connected to the negative supply voltage in NMOS transistors and the positive supply voltage in PMOS transistors. Considering V_{Gt}, V_{St}, V_{Dt} and V_{Bt} as the voltages connected to the corresponding terminals, the formulas for those voltages are as follows :

$$V_G = |V_{Gt} - V_{Bt}| \tag{3.1}$$

$$V_S = |V_{St} - V_{Bt}| \tag{3.2}$$

$$V_D = |V_{Dt} - V_{Bt}| \tag{3.3}$$

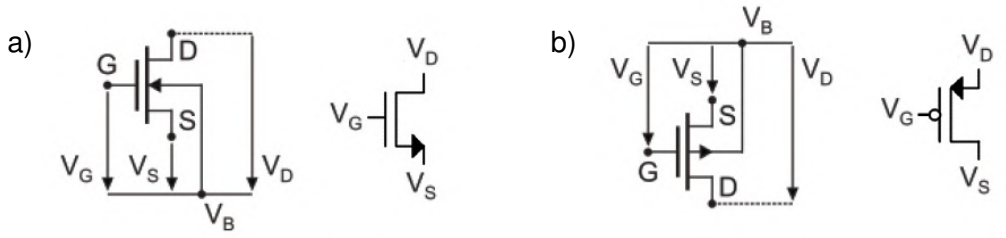

FIGURE 3.1 – *MOS four-terminal symbols with voltage definitions and its simplified three-terminal symbols. a) NMOS. b) PMOS [40].*

In a MOS structure, there are three principal regions : metal (or gate), oxide (insulator) and semiconductor (channel). In an NMOS transistor, the semiconductor material is n-type, meaning it has electrons as the majority of charge carriers or inversion charge. The amount of inversion charge determines the conductivity of the channel and, consequently, the current flowing through the NMOS transistor. In a PMOS transistor, the semiconductor material is p-type, meaning it has holes as the majority of charge carriers. The inversion charge in CMOS technology represents the carriers induced in the semiconductor channel, enabling the transistor to function as a switch or amplifier in electronic circuits. Figure 3.2 illustrates the cross-section of PMOS and NMOS transistors.

The PMOS is fully complementary to NMOS, with the difference that the source is at the highest potential. All formulas for the NMOS transistor have the same form as the PMOS. The only difference is that holes are now the channel's majority carriers.

MOS transistors behave like current sources between the drain and the source terminals and are controlled by the gate terminal with the potential difference between the gate and the source terminal (V_{GS}). Depending on the values of V_{GS} and the potential difference between

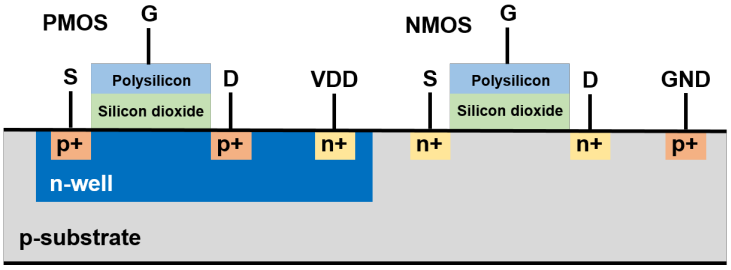

FIGURE 3.2 – *Cross section of PMOS and NMOS transistors [41].*

the drain and the source (V_{DS}), the transistor can work in different operating regions. In strong inversion, V_{GS} must exceed a specific value called the threshold voltage (V_{TH}) ; once this happens, a conductive channel between the drain and the source is formed. The threshold voltage V_{TH} is defined as the gate voltage for which the channel is at equilibrium and the inversion charge is equal to zero ($V_{ch} = 0$). The pinch-off voltage (V_P) is a channel potential for which the inversion charge becomes zero at a given gate voltage. As V_{DS} increases, the potential difference between the gate and drain decreases (V_{GD}), so the channel is pinched off when V_D exceeds $V_{DSmin} = V_G - V_{TH}$. The formula to calculate V_P is the following :

$$V_P = \frac{V_G - V_{TH}}{n} \tag{3.4}$$

The slope factor (n) is taken from the CMOS technology chosen. Figure 3.3 presents the relation of the pinch-off voltage and slope factor with the gate voltage.

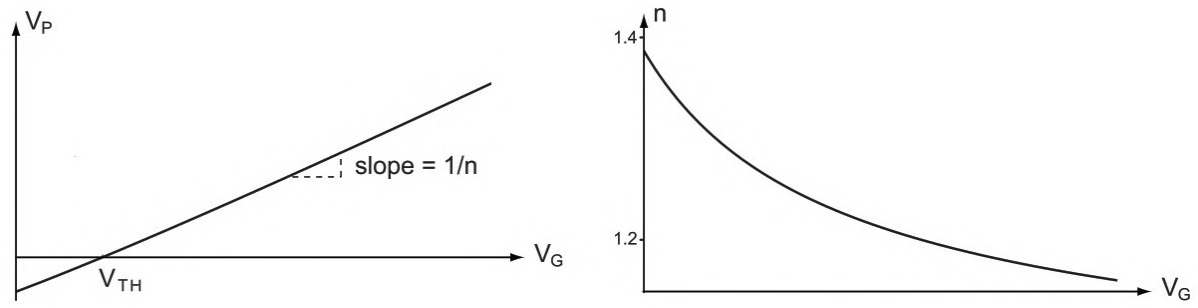

FIGURE 3.3 – *Pinch-off voltage and slope factor as functions of the gate voltage [41].*

When the channel potential becomes smaller than V_P, the inversion charge becomes much smaller than the depletion charge, and the channel is in weak inversion. As shown in Figure 3.4, when the source or the drain voltage is smaller than V_P, the transistor is working in the strong inversion operation ; when the source and drain voltages are larger than V_P, the transistor works in weak inversion.

The drain current can be calculated by integrating the inversion charge along the channel from $V_{ch} = V_S$ to $V_{ch} = V_D$. The drain current corresponds to the shaded surface in Figure 3.4 equal to I_D/β where β is the transconductance parameter that depends on technology and transistor geometry ; it can be calculated as :

$$\beta = \mu_0 C_{ox} \frac{W}{L} \tag{3.5}$$

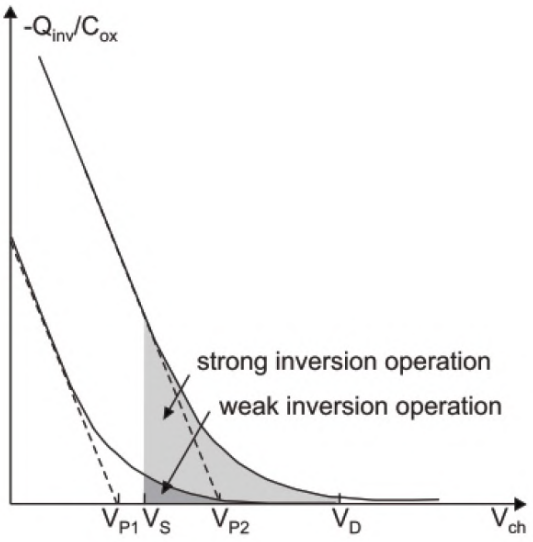

FIGURE 3.4 – *Strong and weak inversion operation of CMOS [40].*

Where μ_0 is the mobility, C_{ox} is the capacitance of the oxide layer, W is the transistor width, and L is the transistor length.

Low voltage circuits require designing the circuit with the CMOS transistors in weak or moderate operation regions. The specific current I_S is the drain current when the transistor operates in the center of moderate inversion, so $I_{Dsat} = I_S$; it depends on technology and transistor geometry. For analog design purposes, the technology gives the specific current as a function of transistor geometry. It is calculated as :

$$I_S = 2n\beta {V_{TH}}^2 \tag{3.6}$$

The transistor operating in strong inversion is in conduction if $V_S, V_D < V_P$. On the contrary, if $V_S < V_P < V_D$, the transistor is in saturation. Then, the saturation drain to source voltage V_{DSsat} can be calculated with the following equation :

$$V_{DSsat} = V_P - V_S \tag{3.7}$$

When the transistor operates in weak inversion, the drain current is considerably smaller than in strong inversion and $V_S, V_D > V_P$. Figure 3.5 shows the saturation voltage (V_{DSsat}) definition in strong and weak inversion, respectively. In weak inversion, the saturation voltage is determined with the acceptable error between the drain current and the expected saturation drain current.

The Inversion Factor (IF) parameter helps to find the inversion region of the transistor ; it is directly proportional to the mobile inversion charge along the channel :

$$IF = \frac{I_{Dsat}}{I_S} \tag{3.8}$$

It can define the weak, moderate and strong inversion operation regions with Table 3.1.

When the channel is formed, the voltage V_{DS} will create the current I_D flowing from the drain to the source. On the one hand, while V_{DS} is smaller than V_P, the transistor will be in

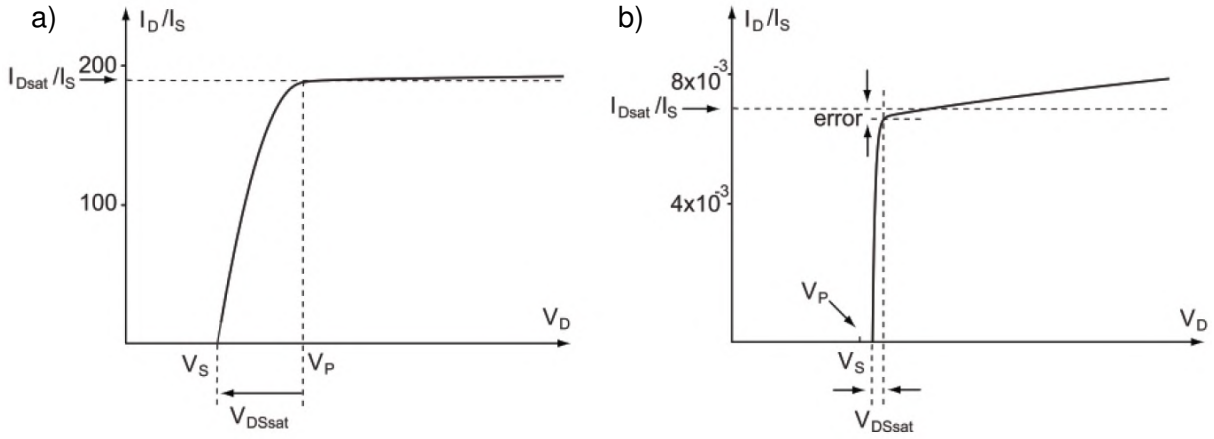

FIGURE 3.5 – *Saturation voltage definition, a) in strong inversion, b) in weak inversion [40].*

	Operation mode
IF < 0.1	Weak inversion
0.1 < IF < 10	Moderate inversion
IF > 10	Strong inversion

TABLE 3.1 – *Operation regions defined with the Inversion Factor.*

triode mode and behave as a resistor. On the other hand, if V_{DS} exceeds the value of V_P, the transistor will be in saturation. In the triode mode ($V_{DS} < V_{DSmin}$), the current through the channel is given by :

$$I_D = \mu_n C_{ox} \frac{W}{L}(2(V_{GS} - V_{TH})V_{DS} - nV_{DS}^2) \tag{3.9}$$

Where μ_n is the mobility of the carriers (electrons in the case of the NMOS transistor). Transistors operated in triode mode can be utilized as voltage-controllable resistors. When $V_{DS} > V_{DSmin}$, the current through the transistor channel is equal to :

$$I_D = C_{ox} \frac{W}{L_{eff}}(V_{GS} - V_{TH})^2 \tag{3.10}$$

L_{eff} is the effective length of the channel. This value is reduced when V_{DS} and I_D increase. This is called the channel length modulation effect, and the channel length modulation parameter (λ) reduces with the transistor size. In the saturation operation mode, the drain current is equal to :

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{3.11}$$

No channel is formed between the drain and the transistor source when the gate-to-source potential is below the threshold voltage. Still, a small current can flow since the transistor is operating in the weak inversion or sub-threshold region where the current is defined by :

$$I_D = I_S \, exp\left(\frac{V_{GS} - V_{TH}}{nU_T}\right) \tag{3.12}$$

Where U_T is the thermal voltage defined as :

$$U_T = \frac{kT}{q} \tag{3.13}$$

k is the Boltzmann's constant, T is the temperature in Kelvin, and q is the charge of an electron.

Figure 3.6 presents the small-signal model of a MOS transistor. It shows the small-signal transconductances defined as small variations in the drain current due to small variations of gate, source and drain voltages.

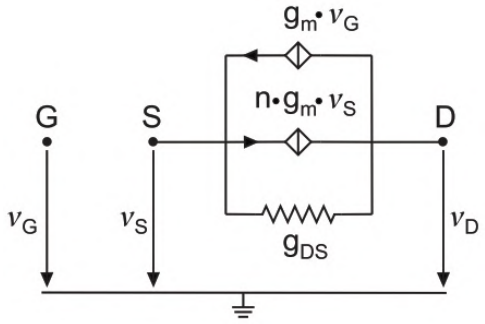

FIGURE 3.6 – *Small-signal MOS transistor scheme with transconductances [40].*

The gate transconductance g_m has units of an inverse resistance and corresponds to the maximum in the dynamic range of a transistor ; it is referred to as the transistor transconductance. In strong inversion, it can be calculated with the following formula :

$$g_m = \sqrt{\frac{2\mu_n C_{ox} \frac{W}{L} I_D}{n}} \tag{3.14}$$

The drain transconductance or output conductance is usually referred to as the drain-source transconductance g_{DS} ; it is represented as a resistor because the voltage on its terminals controls it :

$$g_{DS} = \frac{I_{Dsat}}{L \cdot U_a} \tag{3.15}$$

U_a is the early voltage defined by the CMOS technology, and the source transconductance g_{ms} is equal to :

$$g_{ms} = n \cdot g_m \tag{3.16}$$

Table 3.2 shows the most relevant parameters of the small-signal model for the weak and strong inversion regions in triode and saturation modes.

The intrinsic capacitances (C_{GS}, C_{GD}, C_{GB}) are the capacitances of the inversion layer, depletion region, oxide and the gate ; they determine the transistor behavior. The rest of the transistor is the extrinsic part that influences the parasitic effects, limiting overall behavior. The extrinsic capacitances are C_{GSov}, C_{GDov} and C_{GBov}. Figure 3.7 shows the complete small-signal model of a MOS transistor operating in saturation.

Operation mode	g_m	g_{DS}
Weak inversion	$\frac{I_D}{nU_T}$	0
Strong inversion, triode	0	$\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})$
Strong inversion, saturation	$\sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$	λV_{DS}

TABLE 3.2 – *Small-signal model parameters for the n-MOS transistor [5].*

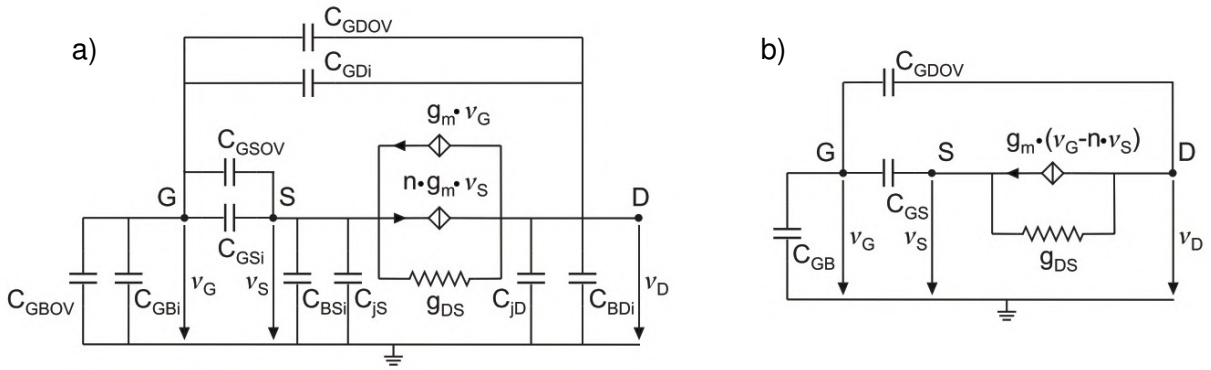

FIGURE 3.7 – *Complete small-signal MOS transistor model. a) Including all transconductances and capacitances. b) Simplified model [40].*

The transition frequency (f_t) is the frequency where the magnitude of the transistor current gain becomes one and represents the transistor speed or the maximal frequency for which the transistor can be used.

$$f_t = \frac{g_m}{2\pi(C_{GS}+C_{GB}+C_{GD})} \tag{3.17}$$

In transistor-level design, there are three basic single-stage configurations : the common source (CS) to convert the voltage into a current (transconductance), the common drain (CD) to convert voltage to voltage (voltage buffer), and the common gate (CG) to convert current to current (current conveyor). Those configurations refer to connecting the ground or reference voltage on the circuit. Additionally, the diode-connected transistor has the gate connected to the source.

3.2.2 Unity Gain Cells

A good approach for analog design is the separation of complex circuits into simpler cells or blocks that can be employed for many different applications. Consequently, analog circuits can be created by superimposing or cascading Unity Gain Cells (UGC), such as Current Mirror (CM), Voltage Follower (VF), Current Follower (CF), or Voltage Mirror (VM) [42]. These UGCs are constructed at the transistor level. A brief description of two UGCs is provided as an example of elementary blocks that can be utilized to construct analog circuits. Additionally, each UGC can assume various configurations based on specific design requirements.

Current Mirrors (CM) are fundamental building blocks for current-mode circuits, making them suitable for low-voltage and high-speed analog circuits. CM is indispensable in various

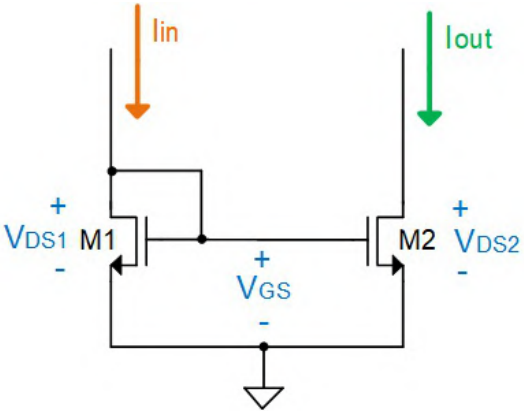

FIGURE 3.8 – *NMOS Current mirror [42].*

analog circuit applications, including opamps. The underlying principle of CM is that if the V_{GS} of two identical MOS transistors are equal, their channel currents should be similar. Figure 3.8 illustrates a basic CM implementation.

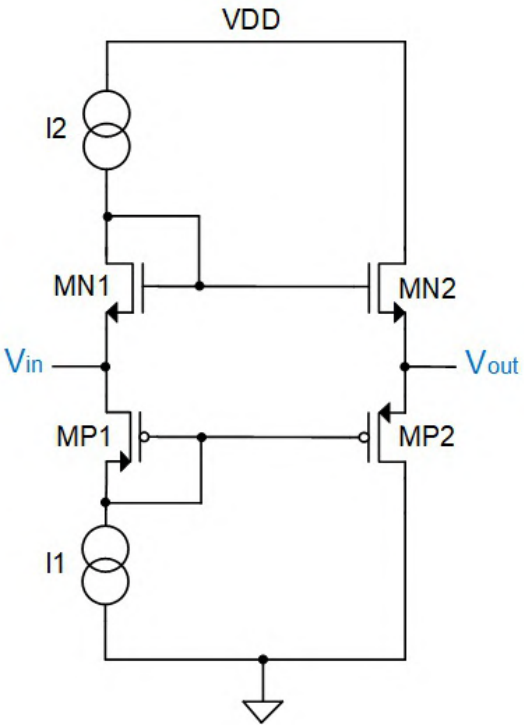

FIGURE 3.9 – *Conventional source follower [42].*

Voltage Followers (VFs) exhibit infinite input, zero output impedance, unity gain and no input signal distortion. Figure 3.9 depicts a typical source follower.

3.2.3 Amplifiers

Various electronic applications can be constructed using fundamental building blocks. ASIC design typically involves connecting multiple modules, such as amplifiers, analog-to-digital converters (ADC), discriminators, shapers, current conveyors (CC), etc.

One of the most commonly utilized modules is the amplifier. The primary purpose of an amplifier is to take an input signal and multiply it by a specified gain value. The gain of an amplifier can be set to be positive or negative, increasing or decreasing the magnitude of the input signal. Amplifiers can be configured as single-input and single-output, differential input and single-output, or differential input and output, among other configurations. Single-input, single-output amplifiers consist of a transconductance structure, such as common-source, common-drain, or cascode, with the appropriate load structure. Each amplifier is designed to meet specific requirements. Table 3.3 outlines the fundamental parameters that must be characterized in an amplifier.

Performance	**Symbol**	**Unit**	**Definition**
Gain	A_v	dB	Amplifier output voltage over the input voltage.
Gain-bandwidth	f_{GBW}	Hz	Frequency at which the amplifier gain is unity.
Dynamic range	-	-	Ratio between smallest and largest signal.
Offset voltage (Pedestal)	V_{os}	V	Amplifier output voltage when the input voltage is zero.
Noise (flicker or 1/f)	-	V/Hz	Random noise generated by trapping and release of charge carriers at the oxide-semiconductor interface.
Noise (thermal)	-	V/Hz	Noise generated by random thermal movement of electrons.
Power dissipation	P	W	Total power dissipated by the amplifier.
Slew rate	S_r	V/μs	Maximum current which can be delivered to the load.
Power Supply rejection ratio	$PSRR$	dB	Attenuation from the power supply to the output.

TABLE 3.3 – *Amplifier basic characteristics.*

The stability of the amplifier is analyzed through its frequency response. The poles and zeros in the transfer function are determined by analyzing the gain path. A pole corresponds to an equivalent resistance in parallel with an equivalent capacitance seen at each node in the gain path. In contrast, a zero corresponds to an equivalent resistance in series with an equivalent capacitance in the gain path. A positive zero may appear due to a possible feedback path. A system can be of the first order if it has only one pole and is usually unconditionally stable. However, if the amplifier has multiple poles, it is necessary to analyze stability by examining the phase shift. Crucial design parameters for frequency include the bandwidth frequency corresponding to the dominant pole frequency in the open-loop transfer function. The following formula defines the gain-bandwidth frequency (f_{GBW}) :

$$f_{GBW} = A_{DC} \cdot f_{dp} \tag{3.18}$$

A_{DC} is the DC gain, and f_{dp} is the frequency at the dominant pole. The phase margin represents the difference between the phase shift at the gain bandwidth frequency and the phase shift of -180°, calculated using this formula :

$$PM = 180° + \phi(f_{GBW}) \tag{3.19}$$

Figure 3.10 illustrates an amplifier's dominant and non-dominant poles, gain-bandwidth frequency and phase margin in an open unity-gain feedback loop.

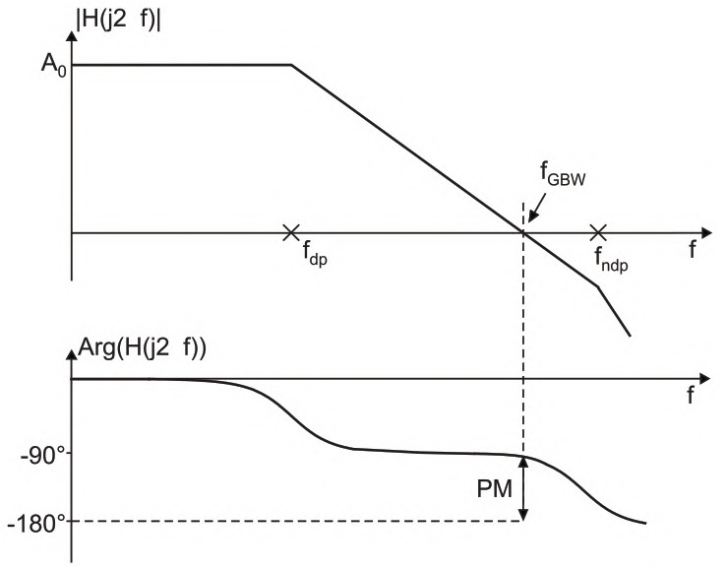

FIGURE 3.10 – *Dominant pole f_{dp}, non-dominant pole f_{ndp}, gain bandwidth frequency f_{GBW} and phase margin PM for the amplifier in open unity-gain feedback loop [40].*

For two-stage amplifiers, a compensation capacitance C_{miller} is typically required for stability. This capacitance, known as Miller capacitance, is introduced in a Miller amplifier structure to address poles in the output nodes of both the first and second stages. The C_{miller} splits these two poles but introduces a positive zero. There is no general rule for choosing the C_{miller} value. It is reasonable to start with half the value corresponding to the maximally allowed capacitance surface in the circuit layout. The final value for stability is determined during the design of the second stage, and it may require repeating some or all design steps to analyze all circuit-level parameters.

3.2.4 Charge High-speed Amplifiers

A charge amplifier integrates the current signal using a feedback capacitor C_f. The basic circuit is shown in Figure 3.11 where I_{in} is the input current signal coming from the detector, and C_{det} is the detector capacitance.

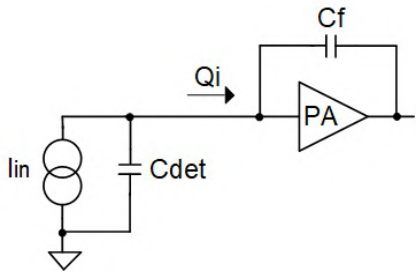

FIGURE 3.11 – *Charge amplifier.*

The charge amplifier transfer function is given by :

$$\frac{v_{out}(w)}{i_{in}(w)} = \frac{-1}{jwC_f}\left(1 + \frac{C_{det}}{AC_f}\right)^{-1} \tag{3.20}$$

Here, i_{in} is the current generated by the detector, v_{out} is the output of the amplifier in volts, and A is the amplifier gain. In the ideal case where the gain is infinite, the transfer function becomes :

$$\frac{v_{out}(w)}{i_{in}(w)} = \frac{-1}{jwC_f} \tag{3.21}$$

The output in the time domain is equal to :

$$V_{out}(t) = \frac{-1}{C_f}\int I_{in}(t)dt = \frac{-Q}{C_f} \tag{3.22}$$

Where the gain A is equal to $1/C_f$.

Since the feedback capacitance needs a way to discharge, a feedback resistance R_f is also required. Therefore, the finite op-amp gain can be expressed as :

$$\frac{v_{out}(w)}{i_{in}(w)} = \frac{-R_f}{jwC_f}\left(1 + \frac{jwC_{det}}{A_0 w_0 C_f}\right)^{-1} \tag{3.23}$$

Here, A_0 is the low-frequency gain, and $A_0 w_0$ is the gain-bandwidth product. The rise time can be found with the following equation :

$$t_{10-90\%} = 2.2\tau, \quad \tau = \frac{C_{det}}{A_0 w_0 C_f} \tag{3.24}$$

In the case of amplifier design for particle physics, the speed of the signal is crucial to improve the resolution of timing measurements. High-speed amplifiers need a low impedance of about 50 Ω or less [85]. The input impedance can be calculated with the following equation :

$$Z_{in} = \frac{1}{jwA_0C_f} + \frac{1}{A_0 w_0 C_f} \tag{3.25}$$

Since the gain in an ideal amplifier is infinite, its input impedance is equal to 0. Having a small input impedance is advantageous to minimize sensitivity to detector impedance and reduce crosstalk. Finally, the time constant is equal to :

$$t = R_f C_f \tag{3.26}$$

3.2.5 Current conveyor

When low power consumption, low voltage operation and a large bandwidth are required, amplifiers (or opamps) could be too complex to implement, taking up much area and resources. The current conveyor (CC) is chosen as an alternative, using current signals rather than voltage signals to design circuits [43]. In current-mode design, MOS transistors with their output current are well-suited for analog design, especially in common-source and common-gate amplifier configurations [44]. Current-mode circuits can be implemented with high speed and bandwidth accuracy using almost only transistors.

A current conveyor is a minimum three-terminal device that performs many useful analog signal processing functions. The first generation (CCI) was introduced in 1969 in [45] as a good

alternative in current-mode design. Figure 3.12 presents its basic structure. A voltage applied to the input Y-terminal is copied to the X-terminal. Suppose a current is injected flowing through the X-terminal. In that case, it generates an equal current into the Y-terminal and another equal current will be conveyed to the output Z-terminal. Those voltage and current are independent since a voltage follower and a current mirror process them.

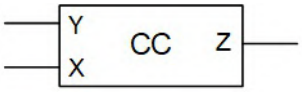

FIGURE 3.12 – *Simple structure of the current conveyor.*

The following matrix equation can describe the input-output characteristics of the CCI :

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ \pm 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.27}$$

Current conveyors can be classified by generation and as direct or inverse depending on the polarity of the voltage in the Y-terminal, positive or negative depending on the Z-terminal current direction, and can have single or multiple outputs.

The second-generation current conveyor (CCII) [46] does not have any current flowing through the Y-terminal, having an infinite input impedance on this terminal. The X-terminal has zero input impedance ; therefore, the X-terminal voltage is the same as in the Y-terminal. The current supplied to the X-terminal is conveyed to the high output impedance through the Z-terminal. The following matrix equation can describe the input-output characteristics of a CCII :

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \pm 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.28}$$

The third-generation current conveyor (CCIII) [47] operates similarly to the CCI. However, the current through the Y-terminal flows in the opposite direction to the X-terminal. The following matrix equation describes the input-output characteristics of the CCIII :

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ \pm 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.29}$$

Current conveyors can be designed with cascode connections of Unity Gain Cells like Voltage Followers or Current Mirrors. The great advantage of CCs is the higher voltage gain that can be provided over a larger bandwidth under small or large signal conditions.

3.2.6 Analog-to-Digital converter

An analog-to-digital converter (ADC) is an analog block that converts an analog signal into a discrete signal. It samples one analog voltage at a determined time. The number of bits defines the resolution of the ADC.

One way to implement an ADC is with parallel encoding, also known as flash, where comparators detect different voltage levels and output their switching state to an encoder. Flash ADCs are constructed with equally spaced comparators and voltage references. They are simple to construct and do not require any timing clocks.

One of the most common medium-to-high resolution ADCs is the Successive Approximation Register (SAR) ADC. The SAR architecture offers high performance low power consumption, and is packed in a small form. Figure 3.13 presents the basic architecture of a SAR ADC.

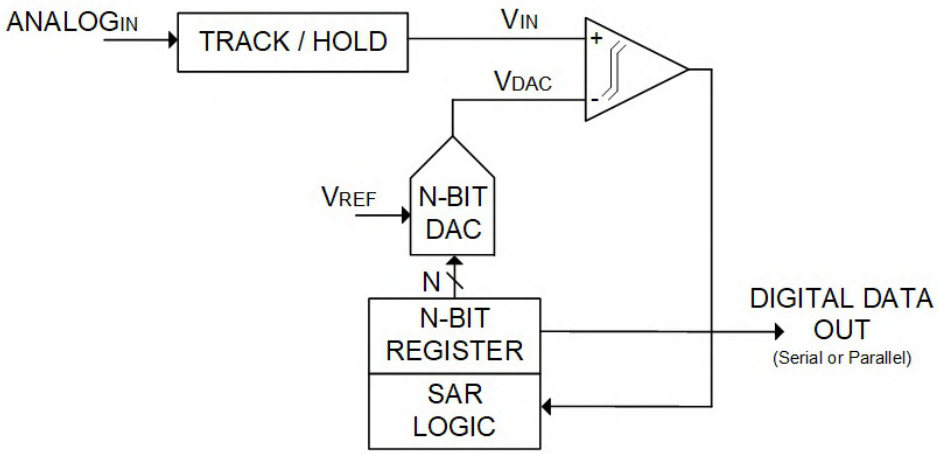

FIGURE 3.13 – *Simplified N-bit SAR ADC [48]*

The analog voltage V_{IN} is held on a track/hold. The N-bit register is initially set with the MSB = 1 and the rest of the bits to 0. This forces the DAC output V_{DAC} to be $V_{REF}/2$. The comparator determines whether V_{IN} is less than or greater than V_{DAC}. If V_{IN} is greater than V_{DAC}, the comparator outputs a 1, and the MSB of the register stays at 1. On the contrary, if V_{IN} is smaller than V_{DAC}, the comparator outputs 0, and the MSB bit changes to 0. The SAR control logic moves to the next bit for the following comparison. The sequence continues until the LSB. After the entire process, the N-bit digital output is available in the register. This type of logic requires one period per bit.

3.2.7 Time-to-Digital converter

A time-to-digital Converter (TDC) is an analog block that converts the time interval between two clock edges into a digital signal. These blocks must band-limit the continuous-time signal ; therefore, having a Phase-Locked Loop (PLL) in the TDC design is common.

The simplest way to design a TDC is with the single-counter TDC architecture (Figure 3.14). This architecture has two inputs (start and stop) ; the input time interval will be measured between the rising edges of those signals with a counter running with a high-frequency reference clock. The gate ensures the counter is enabled only when the two inputs differ. The reference clock's speed constrains the resolution on this architecture and cannot be higher than a single clock period [49].

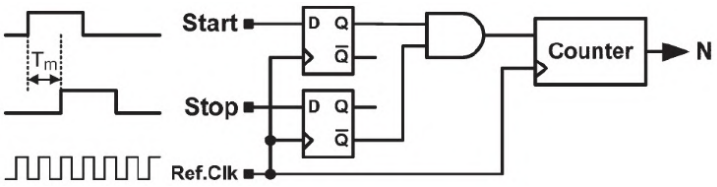

FIGURE 3.14 – *Single-counter TDC.*

High-demand applications, such as electronics design for particle physics, require more complex designs with faster speeds and better stability.

3.3 General Architecture design for detector readout

Measuring charged particle tracks requires the evaluation of millions of pixels, resulting in demanding requirements for front-end electronics. Achieving a large dynamic range and high-speed designs for pixel readout is crucial in applications such as calorimeters. Front-end electronics aim to receive the electrical signal from the detector, typically as a short current pulse, and manipulate and process the signal to obtain valuable data. Depending on the application, the design needs to optimize some requirements over others, aiming to perform at its best. Subsequently, the signal must be digitized and stored for further analysis. In Particle Physics, the most critical parameters in front-end Electronics design are :

- Minimum detectable signal
- Energy measurement
- Event rate
- Time-of-arrival
- Linearity of measurements
- Radiation resistance
- Low power consumption
- Cost

The most challenging requirements include precision in measuring energy and time, low power consumption and radiation hardness. The front-end design architecture for particle physics follows the basic structure shown in Figure 3.15.

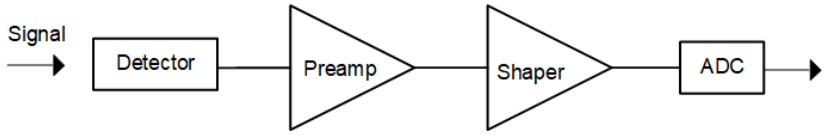

FIGURE 3.15 – *General structure of front-end electronics for detectors [24].*

The energy from the particle is absorbed in the detector and converted into an electrical signal. In semiconductor sensors, the signal charge is usually tiny, about 50 aC for 1 keV x-rays and 4 fC in a typical high-energy tracking detector. Therefore, the signal is amplified with a preamplifier. The preamplifier design is crucial to the system's noise because the first-stage noise will be multiplied by the following stages. Also, it needs to have a small input impedance and a large bandwidth to measure the incoming charge precisely. The input capacitance of the front-end is composed of the sensor capacitance and the input capacitance of the preamplifier. The signal-to-noise ratio (SNR) increases when decreasing this capacitance.

The shaper that follows the preamplifier determines the duration of the pulse and serves as noise filtering. Its design limits the bandwidth since too large of bandwidth will increase the noise without increasing the signal. Also, it transforms the pulse shape with a gradually rounded maximum at the peak time. The pulse width adjustment is necessary to avoid overlap of following signal pulses, reducing the pulse duration and increasing the rate and the electronic noise. Finally, the finite time signal goes to the ADC, which converts the analog signal into a bit pattern for digital storage and processing. The front-end electronics design defines the range of energy measurements, and its noise defines the minimum detectable Signal.

In front-end electronics for particle physics, time measurement is a necessary data that allows identifying particles. Time measurement techniques help to identify the charge energy of a particle detected in the sensor. The simplest method is with the use of discriminators or comparators. These blocks compare the input signal to a previously defined threshold value ; the output goes from low to high when the signal crosses the threshold. This information could

be digitized using a TDC to save the time stamp precisely. Assigning the hit to the correct bunch crossing is essential to ensure that the time assigned is correct for the particle measured. The basic behavior of the discriminator for time measurement is shown in Figure 3.16.

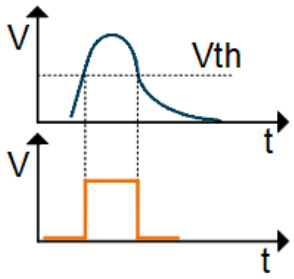

FIGURE 3.16 – *Discriminator behaviour.*

3.4 Noise

In demanding applications such as particle physics, noise affects the accuracy of energy and time information measurements. Noise refers to every unwanted signal that interferes with the system's primary reading signal, imposing limitations on the minimum detectable Signal and the linearity of measurements. The precision of these measurements is constrained by detector noise and the electronic noise within the system. The amplitude distribution of the overall noise follows a Gaussian pattern, with the width of this distribution, referred to as the noise level, equal to the standard deviation. This width is also expressed as the Full Width at Half Maximum (FWHM), equal to 2.355 times the standard deviation. Each noise source must be characterized by its power spectral density, representing the noise power per unit of bandwidth.

There are primarily two sources of noise in front-end electronics. The first, known as thermal noise (Johnson noise), is generated by the random thermal motion of electrons in resistors and is independent of frequency (often referred to as white noise). Its power spectral density of voltage sources can be expressed as :

$$S_v(f) = \frac{dv_n^2}{df} = 4kTR \tag{3.30}$$

The power spectral density of current sources is expressed as :

$$S_i(f) = \frac{di_n^2}{df} = \frac{4kT}{R} \tag{3.31}$$

The second noise source originates from the random trapping and recombination of electrons, often associated with imperfections in interface regions, and is known as flicker noise (1/f noise). Its power spectral density can be described as :

$$S_v(f) = \frac{dv_n^{-2}}{df} = K_v \frac{I^a}{f^b} \tag{3.32}$$

Here, I is the DC current, K_v is a device-dependent constant, and $a = 0.5/2$, $b = 1$. This type of noise depends on frequency and influences the system, particularly at lower frequencies.

The shot noise is generated from the electronics and the detector. It is related to the number of fluctuations of DC. The shot noise originates from the nature of the electric charge and also occurs in the photon counting from the optical detector that generates a leakage current. The power spectral density of shot noise is proportional to the average current I. Its power spectral density is :

$$S_i(f) = \frac{di_n^{-2}}{df} = 2ql \tag{3.33}$$

Noise sources in electronic systems could interfere with the signal of interest as voltage or current fluctuations. The total noise of the amplifier is simplified by calculating the signal-to-noise ratio (SNR). The SNR is the ratio between the noise spectrum at the amplifier's output compared with the output voltage generated by a known input signal. When we examine an amplifier with an input noise voltage denoted as V_n, the SNR can be expressed as :

$$SNR = \frac{V_s}{V_n} = \frac{Q_s}{V_n(C_{det} + C_i)} \tag{3.34}$$

In this equation, V_s represents the signal, Q_s represents the desired signal charge, C_{det} corresponds to the detector capacitance, and C_i encompasses the input capacitance, including the feedback capacitance. This equation underscores the importance of minimizing input capacitance to maximize the SNR, ensuring accurate and reliable electronic measurements.

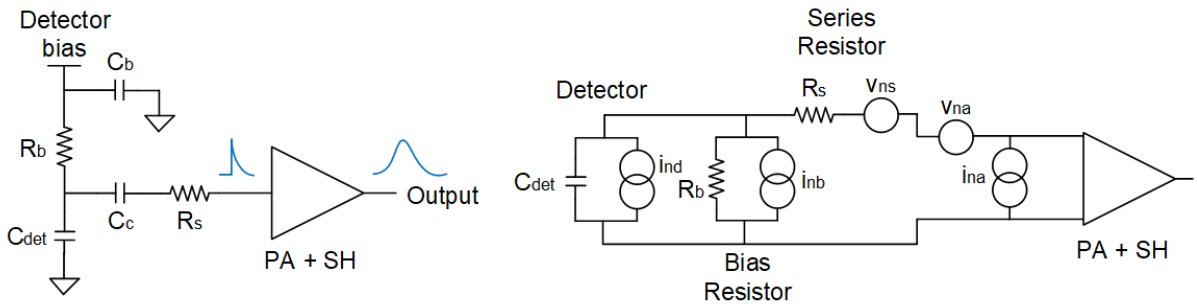

FIGURE 3.17 – *Noise sources at the input of the preamplifier [24].*

The noise sources of a detector front-end amplifier are shown in Figure 3.17. A current noise in parallel with the sensor capacitance represents the shot noise. For resistors, the noise could be modeled as current or voltage. Resistors shunting the input have a noise current source, and resistors in series with the input have a voltage source. Thus, the electronic noise of the preamplifier has a combination of voltage and current sources at its input. In summary, the noise sources are :

— Sensor bias current : ${i_{nd}}^2 = 2eI_d$
— Shunt resistance : ${i_{nb}}^2 = \frac{4kT}{R_b}$
— Series resistance : ${v_{ns}}^2 = 4kTR_s$
— Amplifier : v_{na}, i_{na}

Systems used in particle detection use the Equivalent Noise Charge (ENC). ENC is defined as the magnitude of the input charge required to produce an output amplitude equivalent to the system's root mean square (rms) noise, corresponding to an SNR of 1.

It is advantageous to employ a noiseless amplifier with a transfer function $h(t)$ and all noise sources at its input, including a series resistance and a parallel resistance with its noise sources. The power spectral density of the ENC can then be calculated as the sum of these noise contributions :

$$ENC^2 = \frac{2KTR_s \times {C_t}^2}{T_p} + \frac{2KT \times T_p}{R_p} + A_f {C_t}^2 A_2 \tag{3.35}$$

In this equation, T_p represents the peaking time of the amplifier. The first term characterizes the series noise, the second term accounts for parallel noise, and the final term consists of the flicker noise for MOSFET systems. Series noise is influenced by amplifier characteristics, notably the transconductance (g_m), and is impacted by C_{det} while inversely proportional to T_p. Parallel noise depends on external factors such as the feedback resistor or the shot noise generated by the detector and is subject to an increase with T_p. On the other hand, flicker noise tends to increase with C_{det} and remains independent of T_p. Understanding and quantifying these noise factors is crucial for optimizing the performance of amplifiers.

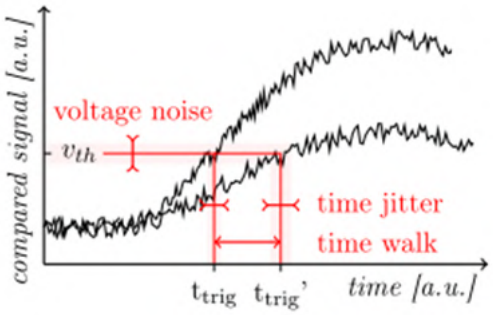

FIGURE 3.18 – *Types of noise in time measurement [5].*

Time measurements introduce two distinct forms of noise, as depicted in Figure 3.18. Time walk refers to the variation in voltage levels reached at different times for signals of varying amplitudes. This phenomenon comes from the natural signal formation. Its statistical representation, given as ${\sigma^{TW}}_t$, is expressed as :

$${\sigma^{TW}}_t = \left[\frac{t_{rise} V_{TH}}{S}\right]_{RMS} \tag{3.36}$$

Here, t_{rise} represents the signal's rise time, V_{TH} denotes the threshold voltage selected on the discriminator, and S accounts for the spectral noise of the system.

Time jitter refers to the noise added to a signal, resulting in amplitude variations due to electronic noise. This type of noise introduces uncertainty regarding the timing of a signal crossing the defined threshold. Its statistical representation, denoted as σ_t^J, is calculated as :

$$\sigma_t^J = \frac{t_{rise}}{SNR} \tag{3.37}$$

Accurate analysis of linearity in time measurements is essential. Usually, the Differential Nonlinearity (DNL) and the Integral Nonlinearity (INL) of the system are evaluated. DNL quantifies the relative difference in bin sizes, as seen in the equation :

$$DNL_i = \frac{w_i}{\langle w \rangle} - 1 \tag{3.38}$$

Here, w_i is the bin size corresponding to the code i derived from transition edges, and w represents the average bin size obtained through a linear fit. DNL normalization conveys the data in terms of Least Significant Bits (LSB) [5].

On the other hand, INL characterizes the absolute deviation from the expected code and is calculated as :

$$INL_i = \sum_{j=0}^{i} DNL_i \tag{3.39}$$

The DNL pattern can be used to correct nonlinearities in software. However, the presence of a significant DNL in the linearity of a system can lead to both noise contributions and errors in data analysis. Therefore, minimizing nonlinearities is essential to reduce overall system noise and enhance measurement accuracy.

3.5 Overview of SiPM Detectors and operating principles

A Silicon Photomultiplier (SiPM) consists of an array of single photon avalanche diodes (SPADs) integrated into a single sensor. In this context, each SPAD functions as a pixel. When exposed to light pulses, the sensor generates primary electron-hole pairs in response to incident photons, initiating an avalanche effect within the SiPM pixels.

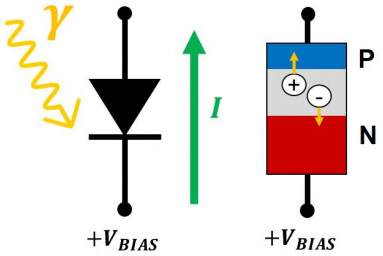

FIGURE 3.19 – *Silicon PN photodiode.*

Silicon PN or PN photodiodes (Figure 3.19) are the most basic of silicon photodetectors. When a photon arrives at the PN structure, it produces a current. Figure 3.20 shows the relation of the current I_{SiPM} produced for different V_{BIAS} in the photodiode.

If the V_{BIAS} is set beyond the breakdown voltage V_{BR}, the photodiode becomes an avalanche diode (APD). This configuration, known as the Geiger mode, produces an avalanche multiplication generating a current without stopping, as shown in Figure 3.21. In principle, the infinite current produced disables the APD from detecting the next photons.

A quenching resistor R_Q can be connected in series with the APD (Figure 3.22) to stop the avalanche multiplication quickly. After the photon produces a large current, the voltage drops across the resistor, which reduces the bias across the APD below V_{BR}, stopping the avalanche. The APD resets itself by recovering to the V_{BR} and is ready for the next photon.

An APD also has one quenching capacitor C_Q to create a fast output (Figure 3.23). The fast output signal is the derivative of the internal fast switching of the APD cell.

Each APD with its R_Q and C_Q is called a microcell or pixel in the SiPM. A SiPM is an array of Geiger mode APDs (Figure 3.24). Each microcell produces a current pulse at the same amplitude when it detects a photon independently. The number of output pulses per pixel is the

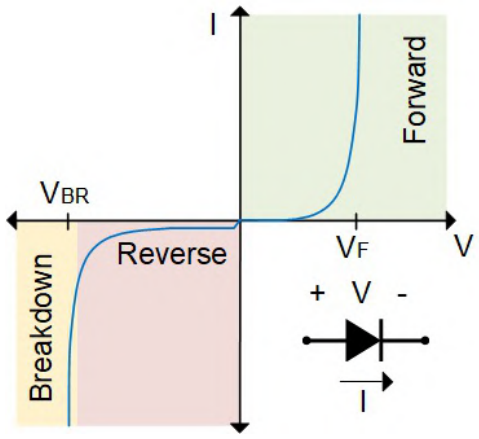

FIGURE 3.20 – *Current as a function of applied voltage into a photodiode.*

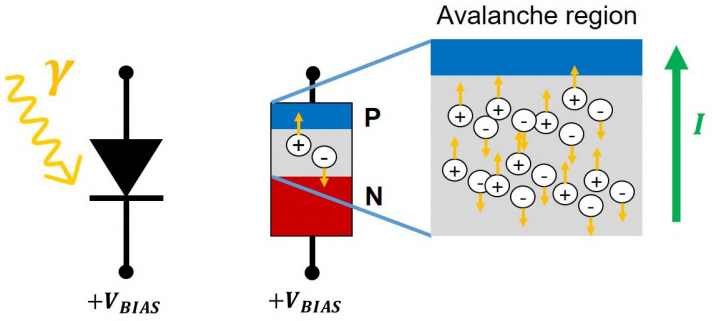

FIGURE 3.21 – *Photodiode avalanche region.*

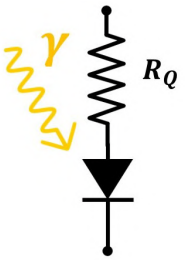

FIGURE 3.22 – *Quenching resistor R_Q connection in an APD.*

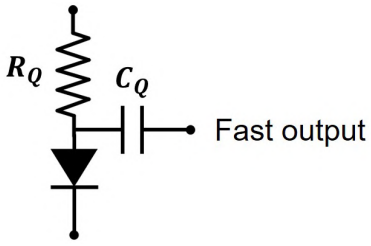

FIGURE 3.23 – *Quenching capacitor C_Q connection in an APD.*

same regardless of whether it receives one or more photons. If some pixels receive photons simultaneously, the SiPM produces a current equal to the sum of all photon pulses. The SiPM output linearity worsens with more photons incident into the SiPM because photons arriving at

the same pixel will not add to the total output current.

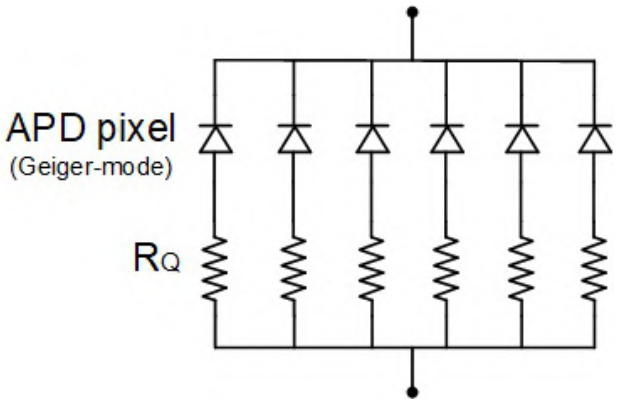

FIGURE 3.24 – *APD pixel array [50].*

Figure 3.25 illustrates the complete model of a SiPM with the junction capacitance C_D in each pixel and the total parasitic capacitance C_G associated with the extensive routing of interconnections for all the microcells. Figure 3.26 illustrates each SiPM pixel's model corresponding to an avalanche photodiode (APD). Figure 3.25 shows one pixel receiving a photon and then $N-1$ pixels without an incoming signal. The switch closing can be modeled as an ideal current source. The number of pixels and the pixel recovery time determine the dynamic range. Smaller pixels increase the SiPM dynamic range and the detector's fast response.

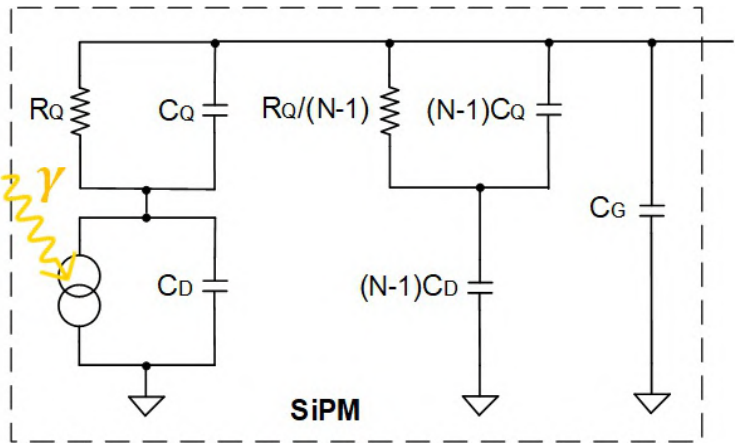

FIGURE 3.25 – *SiPM model with parasitic capacitances [51].*

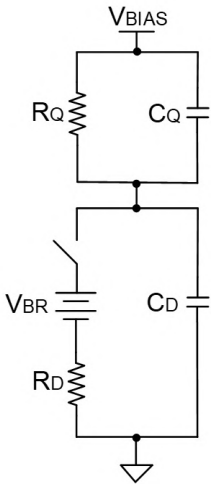

FIGURE 3.26 – *Avalanche photodiode circuit.*

The output current caused by the Geiger discharge is a pulse waveform with a short rise time and a relatively slow fall time when the Geiger discharges, thanks to R_Q. Figure 3.27 shows the output pulse of a SiPM pixel. The current amplitude depends on the difference between the bias voltage and the breakdown voltage of the SiPM; this difference is referred to as SiPM overvoltage OV. The rising and falling times depend on the SiPM capacitance that increases with the number of pixels and SiPM size.

The SiPM exhibits remarkably high gain and exceptional photodetection efficiency (greater than 30%). The primary characteristics of two different SiPMs are presented in Table 3.4. Larger SiPM areas have more pixels and higher detector capacitance. Additionally, the pixel-pitch

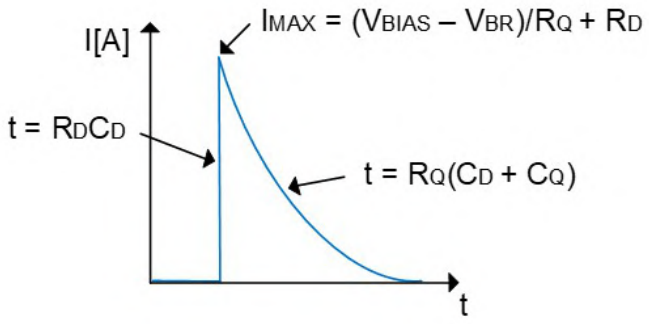

FIGURE 3.27 – *Output pulse characteristics from an APD pixel of a SiPM.*

influences the fill factor of the detector and the photon detection efficiency that increases with the pixel-pitch.

SiPM Model	**S14160-1310PS [53]**	**S16713-03 (ES1)**
Manufacturer	Hamamatsu	
Effective photosensitive area	2 mm²	9 mm²
Pixel pitch	10 μm	15 μm
No. of pixels	16663	39984
Geometrical fill factor	31%	49%
Spectral response range	290 - 900 nm	
Peak sensitivity wavelength	460 nm	
PDE at peak sensitivity	18%	32%
Gain	1.8x10^5	3.6x10^5
Breakdown voltage (V_{BR})	38 $\pm$ 3 V	
Operating Voltage ($V_{BR} + OV$)	V_{BR} + 4 V	
Terminal capacitance at Vop	100 pF	530 pF

TABLE 3.4 – *Example of general properties of two sizes of silicon photomultiplier (SiPM) from the Hamamatsu S14160 series [53].*

The dark current can significantly increase after the sensor is exposed to irradiation or variations in temperature. Working at low temperatures can reduce the sensitivity of SiPMs to irradiation damage. Therefore, using a low temperature, such as $-30\ ^{\circ}C$, can ensure the reliable operation of silicon sensors after irradiation and maintain a good margin of charge collection efficiency.

3.6 Challenges and Limitations in Timing Measurements with SiPMs

The single photon time resolution (SPTR) represents the precision with which a SiPM determines the arrival time of a single photon, a critical attribute for applications in particle physics, medical imaging and astrophysics. A well-designed electronic system is essential to achieve high SPTR in SiPMs.

Figure 3.28 illustrates a schematic for measuring the single photon spectrum (SPS) and SPTR using a frontend electronics setup. A fast, low-jitter laser, such as the 420 nm pico-second pulsed laser (PiLas) with a pulse width of 42 ps FWHM mentioned in [52], can serve as the photon source. Attenuation through diaphragms and neutral density filters ensures controlled

light intensity of one photon. The photon light level can be verified with an oscilloscope that reads the SiPM under appropriate bias conditions. Light injection into the SiPM can be achieved by focusing on a single pixel or using a diffuser to direct photons to a pixel randomly.

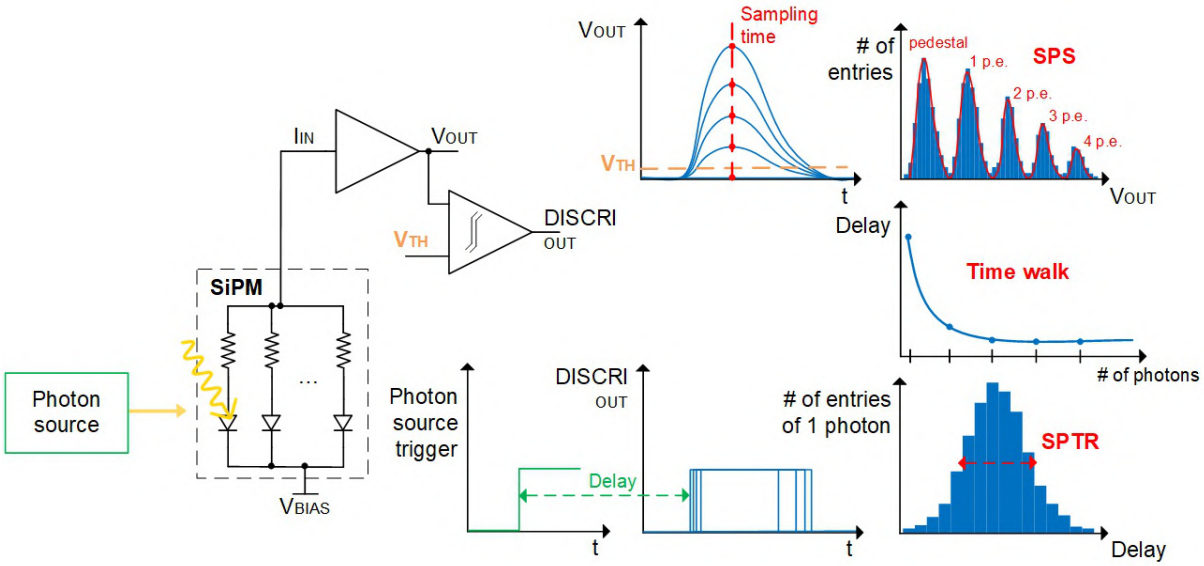

FIGURE 3.28 – *Schematic for SPS and SPTR measurement with photon injection and a basic frontend electronics readout.*

The basic frontend design involves two pathways : one for reading the SiPM charge and another for determining photon arrival times. An amplifier reads the charge, and ADC samples the data at fixed intervals, producing the SPS representing the number of photons arriving at the SiPM. The second pathway utilizes a discriminator to measure the signal duration above a defined threshold voltage. The time delay, measured from the laser trigger to the rising edge of the discriminator, forms the time walk. If we consider the time delays of one photon, we can create a histogram of delay times, ideally showing a Gaussian distribution with a Full Width at Half Maximum (FWHM) equal to the SPTR.

SPS measurements need events with 0 photons (pedestal) to ensure that the subsequent peak corresponds to the injection of one photon into the SiPM. Proper alignment of the SiPM with incident light focused at the pixel's center is crucial to avoid issues arising from multiple photons incident on the same pixel. Figure 3.29 a) illustrates a correct SPS measurement, and Figure 3.29 b) presents the effect of multiple photons incident into the same SiPM pixel.

SiPM characteristics, including the area, significantly impact SPS and SPTR measurements. Larger noise levels reduce peak visibility in SPS measurements. For timing resolution, a larger SiPM area can degrade SPTR due to increased capacitance affecting the rising edge with lower $\frac{dV}{dt}$ and a higher noise due to the higher crosstalk and afterpulsing. Higher overvoltage improves gain, enhancing photon separation in SPS and improving time resolution in SPTR. Focusing the light source at the pixel's center improves SiPM performance compared to injection at the edges.

SiPMs fabricated by various companies, as reported in [52], exhibit optimal SPTR ranging from 70 ps to 330 ps FWHM.

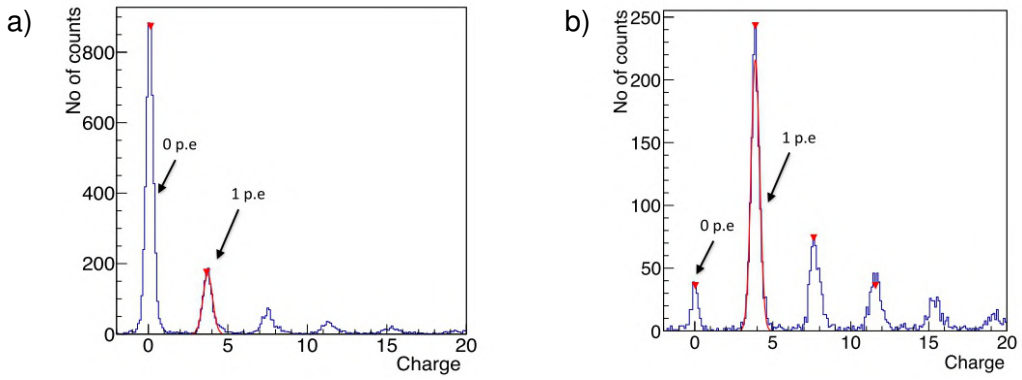

FIGURE 3.29 – *SPS example measurement with the light source focused in a single SiPM pixel. a) Incident light a single photon rate. b) Incident light as a multi-photon rate [52].*

3.7 Front-End Electronics for SiPM

A scintillation detector operates based on indirect detection principles. Initially, the absorbed energy is transformed into visible light. The quantity of scintillation photons produced is directly proportional to the absorbed energy. Then, the SiPM detects the scintillation light. The current pulse produced is integrated over time and contains the signal charge. The pulse shape does not change with the signal charge ; only the peak amplitude increases with the signal charge [24].

The sensor signal is a short current pulse $i_s(t)$. However, the deposited energy is the relevant physical quantity, so it is necessary to integrate it over the current pulse.

$$E \propto Q_s = \int i_s(t)dt \tag{3.40}$$

If we consider the preamplifier resistance, the time constant for discharging the sensor is the following :

$$\tau = R_i \left(C_{det} + C_i\right) \tag{3.41}$$

Where R_i is the preamplifier input resistance, τ is the time constant, and C_{det}, C_i are the detector capacitance and the input capacitance of the preamplifier, respectively. If R_i is very small, the time constant is short, and the preamplifier will read the signal current. Besides, suppose the time constant is significant compared to the duration of the current pulse. In that case, the current pulse will be integrated into the capacitance ; the input voltage of the preamplifier can be calculated as :

$$V_i = \frac{Q_s}{C_{det} + C_i} \tag{3.42}$$

Where Q_s is the charge, and V_i is the input voltage of the preamplifier. Therefore, the signal depends on the sensor capacitance.

The input impedance is a critical parameter in front-end design. It is especially critical in position-sensitive detectors like most detectors used for particle physics. Let us consider a silicon-strip sensor readout connected to each of them to an amplifier (Figure 3.30). Each strip electrode will have the detector capacitance and a capacitance C_n to the neighboring strips.

If the amplifier has an infinite input impedance, the charge in one strip will capacitively couple the neighbors, and several strips will share the signal. Front-end electronics reading several photomultipliers uses low impedance designs to avoid crosstalk between channels. Then, most of the signal will flow into the amplifier, and the neighbors will receive only a tiny part of the signal.

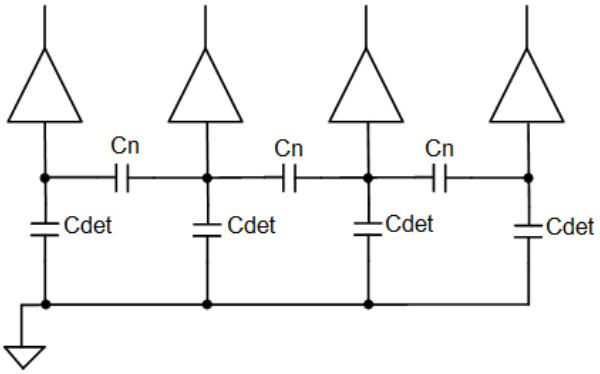

FIGURE 3.30 – *Strip Detector with capacitance between channels.*

The SiPM readout electronics requirements for particle physics experiments can be summarized in the following :

— Precise charge measurement over a large dynamic range.
— Be fully integrated and self-triggered.
— Good inter-cell calibration.
— The Noise should be as minimal as possible.
— Low power consumption of the front-end electronics.
— Specific radiation tolerance for the experiment duration.
— Good SNR for MIPs during the experiment lifetime.
— Precision measurement of time of high energy showers.
— High time resolution.
— Variable voltage at the input of the front-end design that compensates for the differences to calibrate for the different SiPMs.

The front-end electronics are crucial in meeting the readout specifications for Silicon Photomultiplier detectors. Electronic noise contributions influence the SiPM's ability to detect single photons. While the classic charge amplifier is a standard choice for readout in radiation environments due to its low noise, it may not be the optimal solution for SiPM detectors. The high gain of SiPMs makes direct charge integration in C_f impractical. Additionally, the charge amplifier is not the most suitable approach considering factors such as dynamic range, power consumption, stability and speed of response [51]. However, a charge amplifier can be used for specific SiPM readouts ; the ASIC design described in [54] utilizes the charge amplifier, as it involves a low-gain SiPM with a small micro-cell size and low detector capacitance.

In the literature, three main configurations are commonly employed for reading SiPM detectors : the voltage preamplifier (VPA), the Radio-Frequency Amplifier (RFA) and the current conveyor (CC).

3.7.1 Voltage amplifier for SiPM readout

The preamplifier must conserve the fast rise time of the input signal as much as possible to ensure good timing performance. Thus, it must have a large bandwidth and a high input impedance. A voltage amplifier is more suitable for large dynamic range applications when the

specifications on time accuracy are relaxed. Figure 3.31 shows a VPA used to read a SiPM with connections to an integrator and discriminator for energy and time measurements, respectively. To use a VPA, a R_{IN} is needed to transform the SiPM current into a voltage.

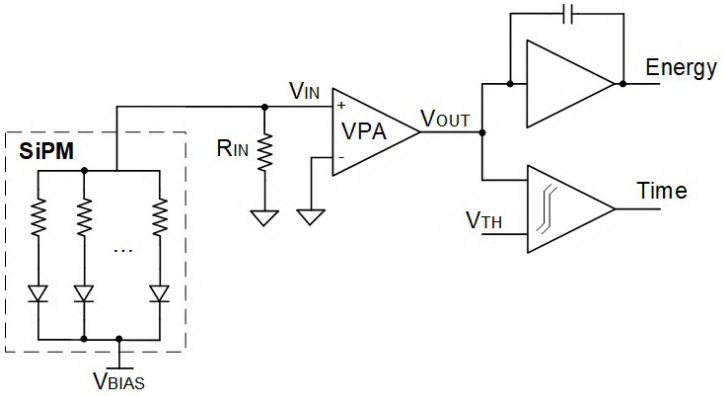

FIGURE 3.31 – *Voltage amplifier for SiPM readout.*

The literature describes different ASICs built for SiPM readout using the VPA approach.

The SPIROC ASIC [55] is a dedicated front-end electronics designed in 350 nm technology by OMEGA, that performs the readout of the Analog Hadronic Calorimeter for the International Linear Collider (ILC). The ASIC was designed to meet the following requirements :

— **Low power :** To avoid active cooling in the detection gap (25 μW per channel with 1% pulsing) with the electronics embedded inside the detection layer.

— **Auto trigger mode :** To reduce the data volume with a threshold of 1/3 of p.e. corresponding to a charge signal of 50 fC for a SiPM with a gain 10^6.

— **Time measurements :** Targeting a resolution of 1 ns.

SPIROC2 can measure charges from one p.e. to 2000 on its 36 channels with a time resolution of 1 ns RMS and power consumption of 25 μW per channel. The analog design (Figure 3.32) of each channel has two voltage preamplifiers, each with a specific gain (High = 10 and Low = 1) to read a dynamic range charge from 50 fC to 320 pC. Each preamplifier has an input NMOS transistor to reduce coherent noise. The variable feedback capacitor allows the adjustment of the gains independently to compensate for non-uniformities on the channels. The preamplifiers are connected to a dedicated trigger line with a fast shaper and a discriminator. Additionally, the ASIC has an 8-bit DAC at the preamplifier's input to adjust the SiPM bias voltage.

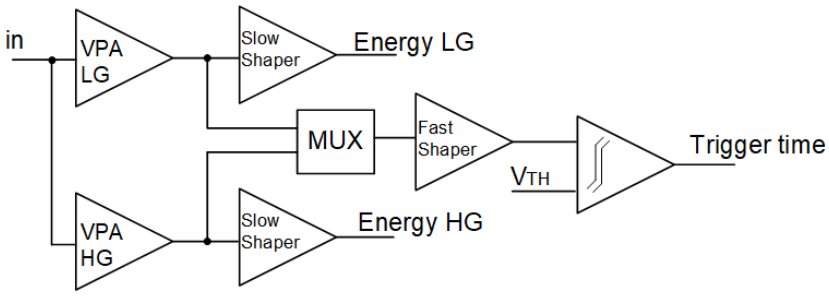

FIGURE 3.32 – *SPIROC front-end analog design.*

Measurements made during a test beam in DESY, with a 6 GeV electron beam, showed minimum ionizing particle (MIP) data. Figure 3.33 shows the difference in its signal against the pedestal. The SNR measured is 30 for the trigger channel with an input signal of 1 p.e.

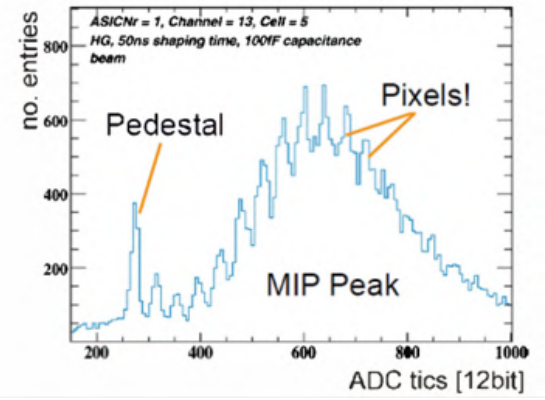

FIGURE 3.33 – *MIP signal and pedestals readed by SPIROC [55].*

Heidelberg University in Germany designed the PETA4 ASIC [56] aiming to read SiPM for the Positron Emission Tomography (PET) scanner in medical imaging. A PET scanner uses scintillator crystals and a light spreader to spread the light to many SiPMs. The time-of-flight (TOF) measurements help to improve image quality.

PETA4 was fabricated using 180 nm technology with 36 channels. It uses two pads for energy and time measurements, respectively. Energy is measured with a fully differential voltage amplifier composed of gain stages that use diode loads (5 low-gain and one high-speed differential gain). It has an input impedance of 7 Ω necessary for good time resolution for the TOF. The ASIC consumes less than 40mW per channel and has a time resolution of 200 ps FWHM.

3.7.2 RF amplifier for SiPM readout

The timing accuracy can be improved using low-noise Radio-Frequency amplifiers (RFA) designed for telecommunication and wireless applications. They feature a 50 Ω input and output impedance. However, their drawback lies in high power dissipation, making them impractical for systems with numerous channels. Two examples are presented in this Section.

PETIROC [57] is an ASIC designed by OMEGA built in 350 nm technology with 16 channels for particle TOF applications. The ASIC combines two measurement lines without interference to measure the time for the first incident photon and the charge integration on different paths with the best accuracy (Figure 3.34). The fast trigger line, designed to measure time precisely, has an RF preamplifier connected to a discriminator and a digital latch. The second line, designed to measure charge, integrates the input signal with a shaped preamplifier connected to an analog memory.

The charge measurement line has a vast dynamic range with a unique gain that measures high-energy signals around 511 KeV Gammas in a crystal that can produce several thousands of p.e. The system can measure up to 3000 p.e. with a linearity of 4%, maintaining 1% linearity up to 2000 p.e. measurement and noise below 600 μV RMS. On the timeline, adjusting the threshold of the discriminator to 1 p.e. produces a time walk lower than 100 ps. The time measurement overall bandwidth is around 877 MHz using a 10%-90% rising time. Figure 3.35 shows the single-photon measurement reading PETIROC output with an oscilloscope [57]. The time resolution measured was 16 ps RMS jitter with 3.6 mW power consumption per channel.

Another example is LIROC [58], a 64-channel ASIC for photon counting applications. Weeroc designed LIROC (Figure 3.36) in TMSC 130 nm technology for LIDAR, a distance and speed measurement device that uses reflection characteristics of emitted light. Usually, the

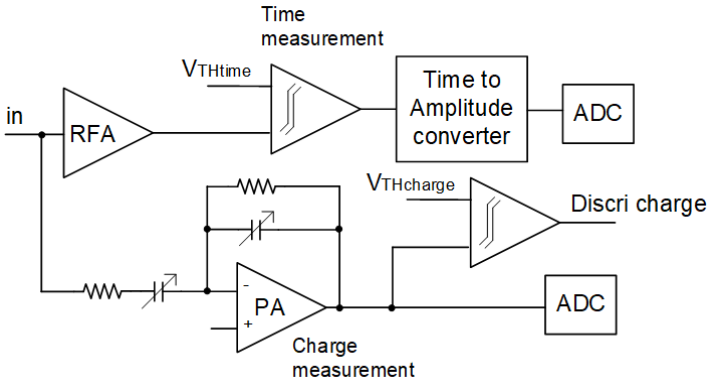

FIGURE 3.34 – *PETIROC front-end analog design.*

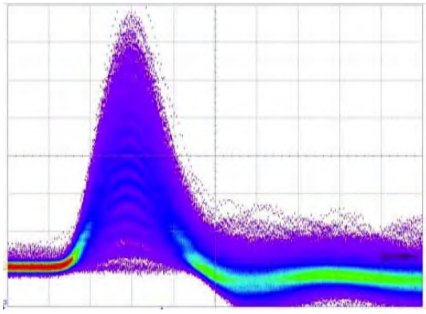

FIGURE 3.35 – *Single photon measurement measured from PETIROC with an oscilloscope [57].*

front-end readout for detectors uses analog integration to measure the energy signal. On the contrary, LIROC uses the technique of photon counting to reconstruct the energy. The preamplifier bandwidth is 1.4 GHz. It was specially designed to do fast photon counting over 100 MHz and can measure two consecutive 2 ns-separated photons with 100% efficiency on 5ns-separated single photons. The timing resolution was measured better than 20 ps FWHM. For high frequencies, the input impedance of the preamplifier is around 60 Ω, a relevant parameter to avoid bad transmission of photodetector signals.

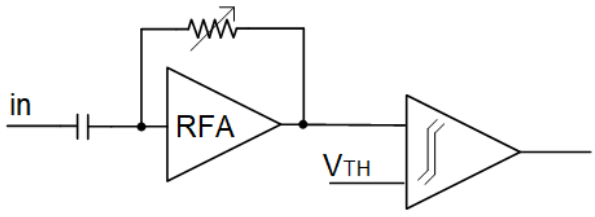

FIGURE 3.36 – *LIROC front-end analog design.*

3.7.3 Current conveyor for SiPM readout

A current conveyor can be designed with very low input impedance. Its output signal is a replica of the current pulse that can be reproduced with scaling factors and used to establish fast and slow signal paths optimized for charge or time measurements. They have high bandwidths because the output signal follows the high-speed current pulse generated by the SiPM. The

contribution of the input transistor to the total noise at the preamplifier's output appears only at high frequencies. In general, they exhibit better noise and better timing performance.

One example is the TOFPET2 ASIC [59], a 64-channel chip designed in standard CMOS 110 nm technology. It is optimized for time-of-flight measurement in Positron Emission Tomography (TOF-PET). Figure 3.37 presents its basic architecture. It has two low-impedance current conveyors at the input selectable to read positive or negative polarity input signals. The current conveyor design is based on a regulated common-gate topology and provides a high-impedance current at its output. The current conveyor output is transmitted to 3 branches. Two trans-impedance amplifiers (TIA) with configurable gains connected to dedicated discriminators are used for timing measurement and hit selection ; one TIA has a lower gain than the other. The third branch uses an integrator to read the charge of the current conveyor output.

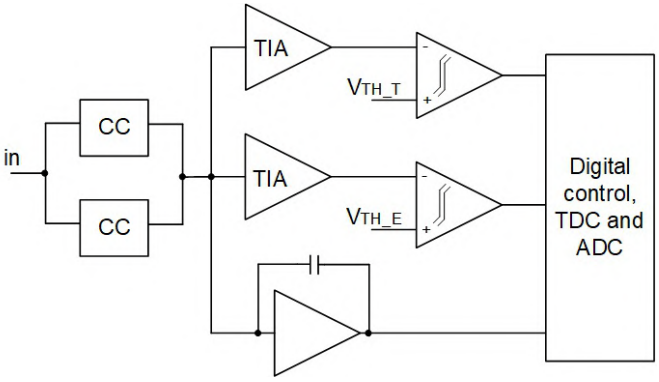

FIGURE 3.37 – *TOFPET2 one channel scheme [59].*

Each TOFPET2 channel has TDCs with 30 ps time binning and ADCs with linear response at the full scale. It has a time resolution better than 100 ps for one photoelectron signal generated by a SiPM, a dynamic range up to 3000 p.e. and a 10 mW power consumption per channel.

A second example is TRIROC [60], a 64-channel ASIC designed by OMEGA and WEEROC for PET prototyping with time-of-flight. This ASIC uses two lines of measurement that do not interfere with each other. One measures the time of the first incident photon, and the second measures the charge energy.

The front-end electronics of TRIROC (Figure 3.38) include a GHz preamplifier connected to a fast discriminator and a precise Wilkinson ADC. The preamplifier accepts both polarities on the input signal. The charge path uses a variable gain semi-Gaussian shaper connected to an ADC linear up to 2500 photoelectrons. The time measurement path uses a high-speed preamplifier with a design that maximizes the bandwidth and uses a discriminator to provide the fast trigger converted to stamp time by a TDC with a coarse and 40 ps fine time [60].

The ASIC includes two shapers using the same architecture but configured with low and large gains. The input on the low gain shaper comes directly from the SiPM to accept higher input charges.

3.8 Conclusion

This chapter has provided an overview of crucial concepts and considerations in front-end electronics design for particle physics, focusing on the requirements and challenges associated with SiPM readout systems. SiPMs offer unique advantages, including high gain, compact

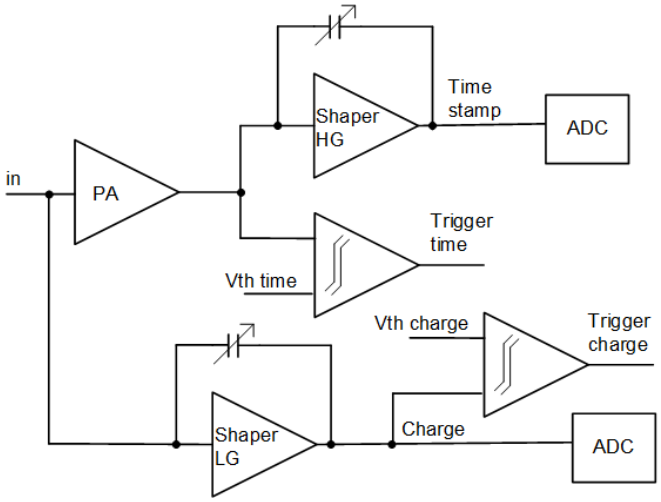

FIGURE 3.38 – *TRIROC front-end analog design [60].*

size and exceptional photon detection efficiency. However, their readout presents distinct challenges, necessitating specialized front-end electronics solutions. The text delved into the SiPM operation, the impact of noise and design considerations essential for achieving optimal performance.

The discussion extended to examining state-of-the-art ASICs designed for SiPM readout, showcasing examples of three main architectural designs with ASICs : SPIROC, PETA4, PETIROC, LIROC, TOFPET2 and TRIROC. Each architecture has its own advantages and disadvantages, featuring innovations in noise reduction, timing accuracy and dynamic range. These advancements reflect the continuous pursuit of enhanced performance in SiPM readout.

The next chapter will explore the selected architecture of H2GCROC, the ASIC designed for the new HGCAL. This ASIC utilizes a current conveyor in the front-end, incorporating energy and time information pathways. Its third fabricated version will be described in detail and characterized in Chapter 5.

Chapter 4

H2GCROC : The SiPM Readout ASIC of HGCAL

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4.1 Introduction

Two ASICs have been designed for the new HGCAL : HGCROC for reading the Silicon sensors in the front part of the calorimeter and H2GCROC for reading the SiPM-on-tile in the back hadronic section. During the conceptual phase, it was determined that using a similar or identical ASIC for both sensor types on the detector would be advantageous [2]. However, this decision posed a significant challenge for the development of H2GCROC. SiPM sensors offer advantages, including higher gain and lower cost than Silicon sensors. Nevertheless, they are less radiation-tolerant and exhibit larger detector capacitances that increase with sensor size. Regarding charge, the input signal at H2GCROC will be approximately 30 times larger than the maximum expected from Silicon sensors.

To address this challenge, it became necessary to develop a variant of HGCROC that adapts the input signal to the feasible range of charges within the capability of the same front-end architecture. The implemented solution employs a current conveyor designed explicitly for SiPMs, capable of attenuating the current signal while maintaining an output compatible with the preamplifier input of the front-end. Subsequently, the remaining aspects of the chip retain the same functionalities as HGCROC, with minor adjustments in the configuration parameters to accommodate the SiPM charge ranges as intended.

4.2 H2GCROC architecture overview

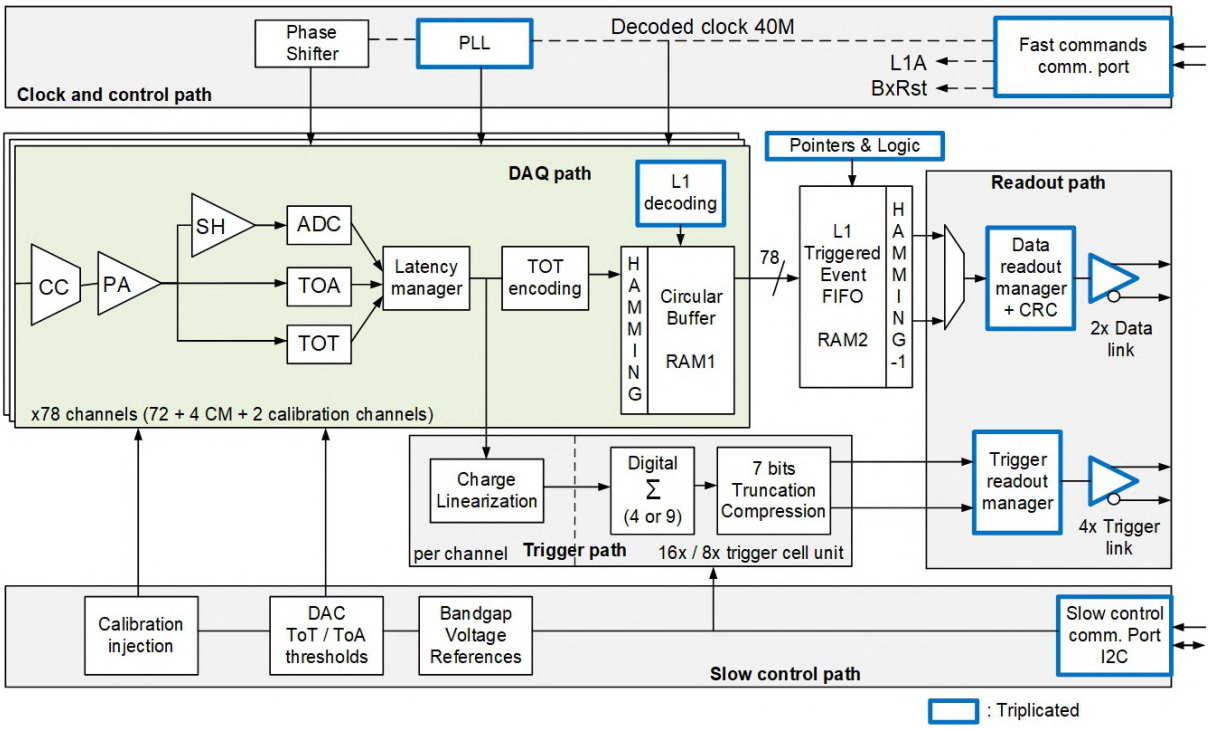

FIGURE 4.1 – *Front-end Architecture of H2GCROC ASIC version 3 [61].*

H2GCROC is a radiation-hardened CMOS chip developed by OMEGA AGH, CEA and CERN, fabricated using TSMC 130 nm CMOS technology [62]. Its primary purpose is to read energy and timing information from SiPM-on-tile detectors in the CMS HGCAL. This chip features 78 channels, each consuming less than 15 mW of power. Among these channels, 72

serve as standard cell readouts, two function as readout calibration cells, and the remaining four channels are not connected to any sensor cells, serving for common-mode noise estimation. Figure 4.1 presents an overview of its architecture and structure.

The layout with an area of 14.5 x 6.5 mm is symmetrically divided into two parts, with Bandgap and voltage references positioned near the chip's edge. The Bias, positive ADC reference and Master TDC components are situated in the central region. The layout of the third fabricated version of the chip is shown in Figure 4.2.

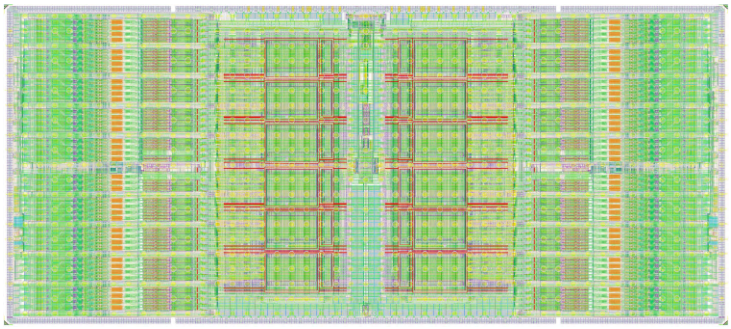

FIGURE 4.2 – *Layout of H2GCROC ASIC version 3.*

The chip was produced with a C4 bump bonding pattern, as shown in Figure 4.3. The layout accommodates a 120 μm height and prevents interference with sensitive analog electronics under the bumps. Four channels fit between two rows of pads, with the slow control system, common for the four channels, placed below the pads.

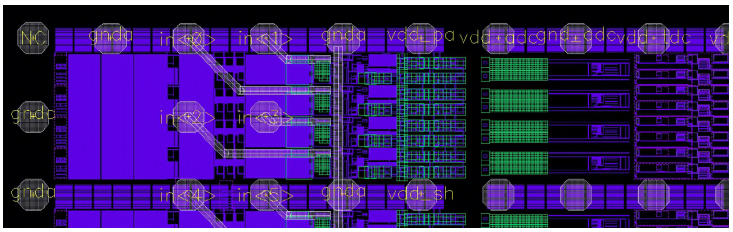

FIGURE 4.3 – *Bumb bonding pattern of H2GCROC [63].*

The front-end design of the chip directly reads the current generated by the SiPM detectors at a 40 MHz frequency. Each channel includes a current conveyor (CC), a low-noise preamplifier (PA) and a shaper connected to a 10-bit 40 MHz SAR-ADC, enabling charge measurement within the linear range of the preamplifier. Additionally, the ASIC incorporates a discriminator and a TDC to provide charge information based on time-over-threshold (TOT) within a dynamic range of 200 ns in the preamplifier's saturation zone. A fast discriminator and TDC also supply timing information with an accuracy of 25 ps.

The ASIC employs a DRAM memory to store charge and timing data, and it performs data processing to select and compress relevant data for trigger formation. The chip's configuration can be adjusted using an I²C protocol for slow control and communicates with the chip using fast commands at a rate of 320 MHz.

4.2.1 Interface blocks

The ASIC incorporates a PLL block for clock generation. It consumes less than 2 mW and uses a 40 MHz clock from the LHC as the input frequency. It produces frequencies of 1.28 GHz, 640 MHz, 320 MHz, 160 MHz and 40 MHz with low jitter, measuring less than 15 ps RMS for

an input jitter of 30 ps RMS. The reference 40 MHz clock is employed by the PLL and various components, including the I²C block, finite state machines (FSMs), counters, two RAMs and pointers. The PLL generates a 40 MHz clock for the ADC, a 160 MHz clock for the TDC, 640 MHz for the E-links and a 1.28 GHz clock for transmitting output data. To optimize the signal-to-noise ratio, the phase of the 40 MHz clock is adjustable at intervals of 640 MHz to be able to sample the maximum signal point with the shaper.

The Fast Command unit (FCU) generates internal fast commands and two triplicated 40 MHz clocks : one operates freely, and the other is synchronized with the incoming bitstream and LHC phase. The FCU decodes the 40 MHz clock from the 320 MHz links. The 40 MHz clock for the I²C is derived directly from the 320 MHz clock input, allowing the chip to be configurable even without fast commands. The second 40 MHz clock is used for the chip's PLL, digital and mixed parts. It is decoded from the 320 MHz and fast command links, so a correct fast command is necessary to provide this clock. The latency of the FCU, which applies to all fast commands, is less than three clock cycles, equivalent to 59.375 ns $\pm$ 3.125 ns for decoding a command since the arrival of the last serial bit of the command. The commands can be programmed in the ZYNQ's firmware and controlled using Python scripts. An example of a fast command is 'CMD_L1A,' which validates an L1A Event in the RAM1 circular buffer.

For chip configuration, slow control employs the I²C protocol. The chip's I²C circuits consist of eight internal registers. The ASIC offers numerous parameters that can be configured, thanks to 512 sub-addresses with a maximum of 32 configuration parameters. The frame for writing or reading the I²C protocol remains consistent and is illustrated in Figure 4.4. It requires the chip ID, the number of register, the Read/Write bit set to 0 for writing and 1 for reading and the 8-bit data frame for configuring the parameter. The first two registers select the appropriate parameter register address and must be configured before writing a specific 8-bit word to the chip.

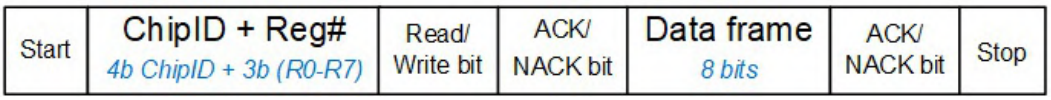

FIGURE 4.4 – *Frame of I²C protocol [63].*

Typically, a bandgap value provides an output voltage of approximately 280 mV. However, this ASIC multiplies the Bandgap output to provide a usable voltage reference of 1 V and a reference current. The bandgap voltage serves multiple purposes, including generating the upper reference voltage for the 12-bit calibration DAC, the reference voltage for the ADCs and TDCs, biasing and stabilizing the TOT against variations in power supply. The bandgap current produces the offset and steps for the 10-bit DACs.

Given that the circuit is symmetrically divided into two parts, there are two bandgaps and two sets of voltage references with DACs, each for the right and left sub-parts of the chip. All voltage references are derived from the Bandgap and use a 10-bit DAC and the preamplifier output of a common-mode channel to ensure the ASIC remains insensitive to temperature fluctuations. Consequently, the common-mode channels cannot be deactivated through configuration settings.

4.2.2 Power of the ASIC

The ASIC features a hard reset pin (ReHb) and a soft reset pin (ReSb). The hard reset resets all components within the ASIC, including the PLL, I²C, FSM, counters and parameters. The soft reset resets all components except the slow control parameters. When the chip is po-

wered on, the Power-On-Reset (POR) mechanism initiates a hard reset and begins the startup sequence. This sequence comprises four distinct modes :

- **Startup Mode :** This mode immediately follows the hard reset and awaits the locking of the PLL.
- **Ready Mode :** In this mode, the ASIC awaits the loading of parameters through the I²C interface. Once all parameters are successfully loaded, the ASIC transmits a forced 32-bit IDLE pattern through the four trigger links.
- **Operational Modes :** The following two modes depend on the configuration parameters of the ASIC :
  - ***Run Mode :*** This is the normal operational mode where the ASIC begins writing physics data into the DRAM.
  - ***Test Mode :*** In this mode, an extensive test of the DRAM functionality is enabled.

The chip allows operating in normal or low-power mode to manage power consumption. In low-power mode, the analog section of the chip, which includes the preamplifier, shaper and discriminators, is deactivated. However, the PLL remains operational, ensuring the ADC, TDC and AlignBuffer continue functioning.

4.3 Very Front-End ASIC design

Each channel (see Figure 4.5) incorporates a current conveyor (CC) at the input of the front-end ASIC. The current conveyor attenuates the current signal, adapting it to the dynamic range required for the following stages similar to the Si version with only a few modifications. The output of the current conveyor is then directed to a low-noise, high-gain preamplifier (PA), followed by a shaper (SH). These components are connected to a 10-bit, 40 MHz SAR-ADC, enabling charge measurement within the preamplifier's linear range. Furthermore, the channel includes a discriminator and a time-to-digital converter (TDC) to provide charge information based on time-over-threshold (TOT) measurements, covering a dynamic range of 200 ns within the saturation zone of the preamplifier [3]. A second discriminator and TDC provide the time-of-arrival (TOA) information. Charge and timing data are stored in a DRAM memory for subsequent processing.

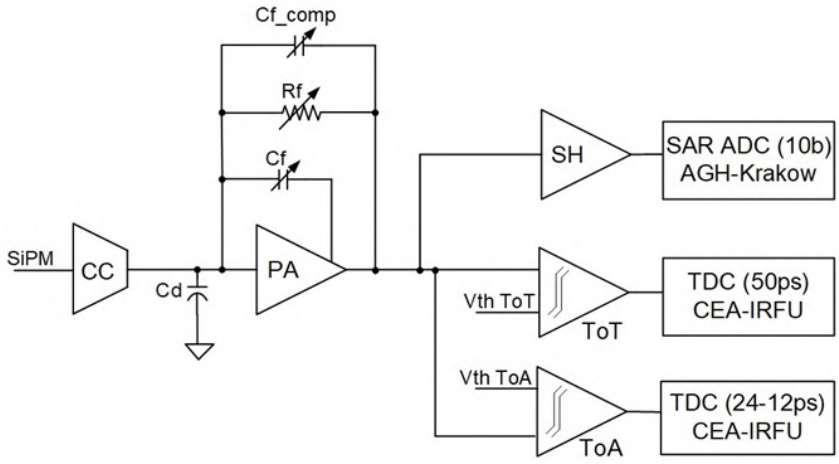

FIGURE 4.5 – *Front-end Architecture of one analog channel of H2GCROC [61].*

4.3.1 Current conveyor

The anticipated charges range from 160 fC to 320 pC, equivalent to 1 to 2000 photoelectrons (p.e.). A current conveyor attenuates the current before the preamplifier ; the current conveyor was designed based on the input stage of the KLauS chip [64] from Heidelberg University. The objective of the current conveyor is to accommodate the large signals generated by SiPMs, thus creating a more extensive dynamic range. The current conveyor attenuation can be adjusted through four bits, where the MSB is common to all channels, and the three LSBs can be configured channel-wise. This attenuation effectively reduces the amplitude while maintaining compatibility with the preamplifier designed for the HGCROC Si-version ASIC.

Figure 4.6 illustrates the schematic design of the current conveyor. The I_{bo} current is employed for coarse current compensation. Considering the current conveyor's gain, it automatically compensates the current I_{bi} of the current conveyor. This compensation input is derived from a signal originated from the common mode channel on a chip level to offset variations in I_{bi}. SiPMs may exhibit breakdown voltage variations due to temperature fluctuations and production tolerances ; the current conveyor can compensate for these fluctuations by configuring the DC voltage V_{dac} at the input.

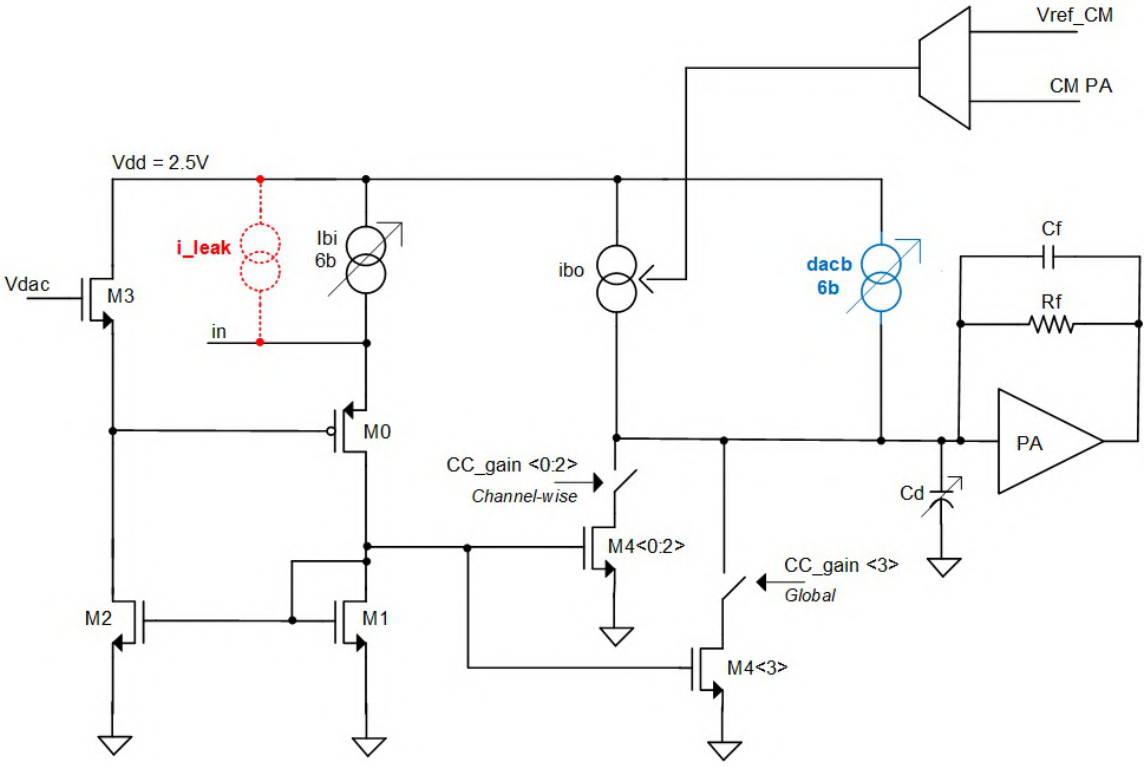

FIGURE 4.6 – *Current conveyor schematic for SiPM readout in H2GCROC ASIC.*

Additionally, the detector radiation is expected to increase the dark currents of SiPMs, producing leakage currents in the range of 1 mA. A 6-bit DAC ($dacb$) can inject an opposite current to compensate for these leakages. Two bits are allocated for adapting the current compensation dynamic range, allowing for compensation of up to 1.3 mA using a 0.1 attenuation in the current conveyor.

The current conveyor (see Figure 4.6) is designed with low input impedance to efficiently capture the sensor's charge signal, even for large-area sensors. The current conveyor employs a common-gate structure with voltage feedback to enhance the input impedance, with

an expected small input impedance of 25 Ω. The input impedance is reduced by elevating the transconductance (g_m) of the input transistor $M0$ through current-mode feedback. This feedback lowers the gate voltage of $M0$ as the input signal increases, injecting more current into the $M0$ transistor. The signal current is duplicated into a feedback path using transistors $M1$ and $M2$, causing a voltage shift at the gate of $M0$. Transistors $M0$ and $M3$ serve as source followers, permitting the DC input terminal voltage adjustment using the DAC input terminal of the conveyor (V_{dac}). The signal current is duplicated via the NMOS current mirror comprising $M1$ and $M2$, and it is further copied to the attenuation transistors scaled by a gain value configured by the 4-bit CC_gain parameter. The size of these attenuation transistors allows for signal attenuation ranging from 0.025 to 0.375, with a 0.025 step and a default attenuation of 0.1.

4.3.2 Preamplifier

The preamplifier (PA) is responsible for converting the output current of the current conveyor into a voltage output, optimizing the signal-to-noise ratio, and adjusting the gain to suit the MIP signal. Additionally, it must produce a brief output duration. The preamplifier is DC coupled to the output of the current conveyor and provides two outputs :

— **outpa** : is connected to the shaper and the TOT discriminator, operating with a DC level typically 160 - 200 mV.
— **outCf** : is connected to the TOA discriminator, with a typical DC operating point at around 500 mV.

The preamplifier gain and time constant can be customized using the feedback resistance (R_f) and the feedback capacitors (C_f and Cf_{comp}) to adapt to the MIP signal. The feedback capacitor is divided into C_f and Cf_{comp} to enhance the stability of the preamplifier. Table 4.1 lists all available values for these components within the ASIC.

$\boldsymbol{R_f}$ $[\boldsymbol{k\Omega}]$	25	50	66.66	100
$\boldsymbol{C_f}$ $[\boldsymbol{fF}]$	50	100	200	400
$\boldsymbol{C_{f\_comp}}$ $[\boldsymbol{fF}]$	50	100	200	400

TABLE 4.1 – *Configurable values for the feedback resistor and capacitors in H2GCROC.*

The capacitors and the feedback resistance contribute to the overall gain of the preamplifier. The configuration of the feedback resistor and capacitors is adjusted to maintain a constant $R_f \times C_{f_total}$ product and ensure the signal has a consistent duration.

The preamplifier gain must be configurable since the MIP signal varies depending on the sensor size and radiation exposure. This programmability allows adjusting the ADC range to accommodate different sensor characteristics or compensate for radiation-induced damage. The behavior of the preamplifier across the entire charge dynamic range can be divided into three distinct steps [63] :

— **Linear Mode :** In this mode, the preamplifier produces an output directly proportional to the input charge within a range of 300 mV.
— **Non-linear Mode :** After reaching around 500 mV at the output, the preamplifier enters the non-linear mode. In this regime, the preamplifier is no longer operating linearly, although it is not fully saturated.
— **Saturation Mode :** The saturation mode comes into play when the output exceeds 600 mV. In this region, the preamplifier pulse width becomes proportional to the input charge, optimized for time-over-threshold techniques. During this mode, an undershoot can affect the charge measurement in the following bunch crossing. The undershoot occurs

because, in saturation, the preamplifier operates in an open-loop configuration, resulting in a slower recovery of its typical behavior.

In saturation mode, the pulse width of the preamplifier becomes proportional to the input charge. However, the linearity of the width measurement deteriorates for larger signals, affecting the time-over-threshold measurements. To address this issue, a capacitor C_d is provided at the preamplifier's input, which is configurable through 3 bits. Each bit corresponds to a capacitance connected in parallel to the preamplifier input. Table 4.2 presents the different C_d values available for configuration. The purpose of C_d is to slow down the response to small charges and create a more uniform duration of the signals.

C_d configuration	Bit 0 [5 pF]	Bit 1 [11 pF]	Bit 2 [19 pF]	Total capacitance
0	-	-	-	0 pF
1	x	-	-	5 pF
2	-	x	-	11 pF
3	x	x	-	16 pF
4	-	-	x	19 pF
5	x	-	x	24 pF
6	-	x	x	30 pF
7	x	x	x	35 pF

TABLE 4.2 – *Capacitance C_d available at preamplifier's input.*

The primary design objectives of the preamplifier are to maintain low power consumption and fast amplification. Post-layout simulations of the preamplifier in the HGCROC reveal a power consumption of approximately 3 mW, offering a 90 dB open-loop gain and a gain-bandwidth product of 1 GHz.

When a large input signal is present, the preamplifier saturates and transitions into an open-loop circuit, entering the TOT mode. In this scenario, the preamplifier no longer functions as a low-impedance circuit. Thus, the input voltage decreases by I/C_{total}, where I represents the input current due to the charge, and C_{total} is the total capacitance at the preamplifier input. The TOT gain is adjusted by a constant current that discharges the feedback capacitor of the preamplifier.

The preamplifier schematic is displayed in Figure 4.7. The linear dynamic range is limited to 300 mV because the first stage of the preamplifier comprises four serial transistors necessary to achieve a significant open-loop gain of 90 dB. Consequently, the output amplitude of the first stage is restricted by the $V_{ds} - V_{ds\_sat}$ voltage of the cascode transistor. The input design has a boosted cascode with an NMOS transistor in the input ($M0$). The output stage has a source follower designed with an NMOS LVT transistor to provide fast output, therefore improving the timing measurement performance. The choice of LVT transistors reduces the output dynamic range, allowing for a larger dynamic range at the input. The output includes a level shifter to raise the output voltage and accommodate the negative output swing in the positive input current mode. Additionally, all CMOS switches are specially designed to have low impedance to maintain good linearity performance.

The preamplifier was analyzed at the transistor design level using Cadence to evaluate the small signal equivalent model. First, the transistors $M2$, $M3$, $M6$ and $M8$ are biased to provide the necessary currents to establish all the DC operating points, designed to deliver 25 μA, 200 μA, 500 μA and 50 μA respectively. With the formulas from Section 3.2.1, it is possible to deduce that transistors $M0$, $M5$, $M7$, $M10$, $M12$, $M13$ and $M15$ operate in weak inversion to

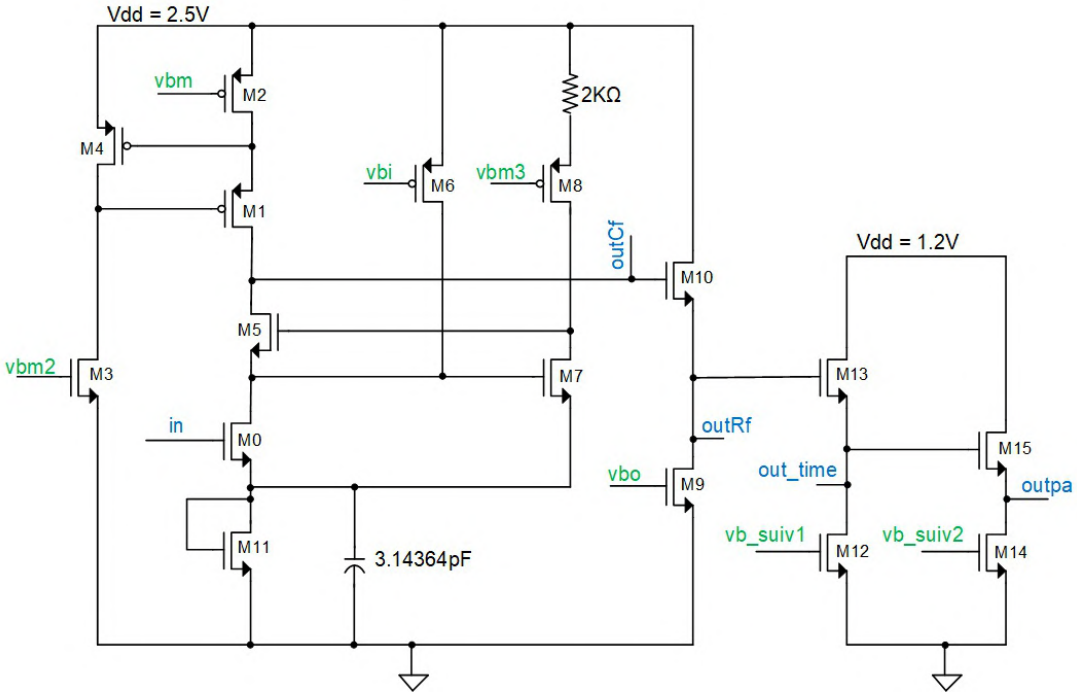

FIGURE 4.7 – *Preamplifier at transistor-level design.*

reduce power consumption, while the rest operate in saturation mode.

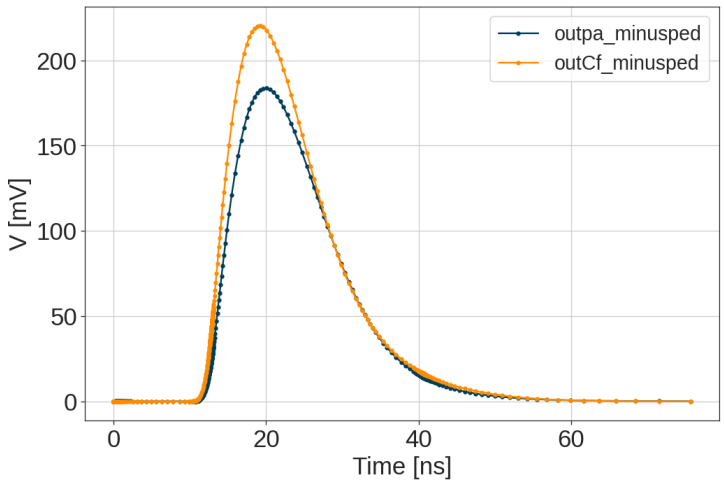

FIGURE 4.8 – *Difference between output signals of the preamplifier with pedestal subtracted : $outpa$ for energy measurements (Pedestal 190 mV) and $outCf$ for time measurements (Pedestal 670 mV).*

As mentioned earlier, two different preamplifier outputs are employed in the front-end. $outpa$ is linked to an ADC and a discriminator connected to a TDC for energy measurements, while $outCf$ is linked to a dedicated discriminator and TDC for timing measurements. Figure 4.8 illustrates the difference between these two outputs : $outCf$ is situated in the 2.5 VDD section of the preamplifier to generate a faster signal, whereas $outpa$ is in the shifter section to reduce noise and maintain compatibility with the rest of the design. Another distinction between the two outputs is the DC level, with simulation results showing 190 mV for $outpa$ and 670 mV for

$outCf$.

4.3.3 Shaper

The shaper (SH) consists of three stages :
— A Sallen-Key filter.
— An RC² filter.
— A unity gain amplifier to interface with the ADC.

First, the Sallen-Key filter is configured as a low-pass filter to attenuate all frequencies above 53 MHz. Then, two single-to-differential RC² shapers, each with a gain of 2, are employed before the differential signal is routed to a dedicated shaper and subsequently sent to the ADC inputs.

The overall structure comprises a fourth-order RC shaper with a typical peaking time set at around 23 ns and a shaping time of approximately 5 ns. This block is designed to improve the signal-to-noise ratio and effectively utilize the available dynamic range of 1 V. Optimally, the signal's duration should be short enough to ensure it remains below 20% after 25 ns, allowing it to be ready for the subsequent bunch crossing and minimizing out-of-time pileup. The preamplifier feedback determines the gain and decay time in the front-end. The shaper aims to achieve the optimal shaping time, typically between 20 and 25 ns.

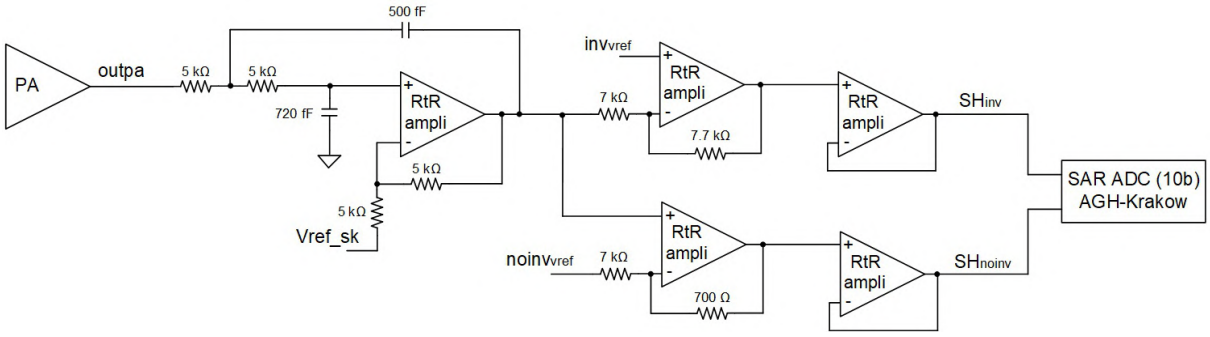

FIGURE 4.9 – *RC shaper schematic.*

Figure 4.9 presents the shaper circuit. To configure this module, two 10-bit DACs globally control the DC levels for the inverter (inv_{vref}) and non-inverter ($noinv_{vref}$) shapers. These two DC levels set the ADC pedestal. The 10-bit DACs typically have a 1 mV least significant bit (LSB). Additionally, per channel, there is a 6-bit DAC ($trim_{inv}$) with a 2 mV LSB that can reduce dispersion per channel. The DC level for the inverter shaper output is calculated using the following formula :

$$SH_{inv} = 3 * (inv_{vref} < 9:0 > -trim_{dac} < 5:0 >) - 2 * V_{in\_pa} \tag{4.1}$$

Similarly, the DC level for the non-inverter shaper is determined by :

$$SH_{noinv} = 2 * V_{in\_pa} - noinv_{vref} < 9:0 > \tag{4.2}$$

Here, V_{in_pa} represents the DC level of the preamplifier input, typically around 200 mV. The ADC converts the differential voltage ($SH_{noinv} - SH_{inv}$) with an ADC reference voltage V_{ref} around 1 V, and gives the following output :

$$ADC = \left(1 - \frac{SH_{noinv} - SH_{inv}}{V_{ref}}\right) * \frac{1024}{2} \tag{4.3}$$

The ASIC incorporates a circuit that automatically identifies the optimal configuration for inv_{vref} and $noinv_{vref}$. Initially, the ADC input is forced to 0.6 V to scan the voltage reference DAC of one branch, set to the value corresponding to a 256 code. Subsequently, the same procedure is performed for the other branch. This circuit is designed to optimize both the pedestal and the dynamic range.

4.3.4 Discriminators

The H2GCROC ASIC features two discriminators per channel : one for time-of-arrival measurement and another for time-over-threshold measurement. Each of these discriminators is linked to a distinct output of the preamplifier. The TOT discriminator is connected to the same output as the ADC ($outpa$) with a DC level ranging from 160 mV to 200 mV. The TOA discriminator is linked to a dedicated output ($outCf$) with a DC level of approximately 500 mV. The ASIC includes two global 10b-DACs that allow adjusting the discriminators' thresholds and two local trimming 6b-DACs that reduce the dispersion per channel as described in equations 4.4 and 4.5. The 10b-DAC has 1 mV LSB, and the 6b-DAC has 0.25 mV LSB.

$$TOA_{threshold} = TOA_{vref} < 9:0 > - Trim\_dac_{TOA} < 5:0 > \tag{4.4}$$

$$TOT_{threshold} = TOT_{vref} < 9:0 > - Trim\_dac_{TOT} < 5:0 > \tag{4.5}$$

These discriminators generate a trigger signal whenever the input pulse surpasses a predefined threshold value. This trigger signal locks a set of latches that capture the current timestamp. Subsequently, a dedicated TDC converts the time information from each discriminator into digital data [65].

4.3.5 ADC

AGH developed the ADC for H2GCROC in Krakow [66]. It is a 10-bit Successive Approximation Register (SAR) type ADC. The primary goal of its design was to achieve high resolution with a maximum power consumption of 1 mW at a 40 MHz frequency and a compact layout to facilitate use in multi-channel applications.

The architecture of the ADC is illustrated in Figure 4.10. It comprises input sampling circuitry, a digital-to-analog converter (DAC), a comparator and SAR control logic. The fully differential structure enhances immunity to disturbances such as digital cross-talk. The DAC was constructed with capacitors to eliminate static power and reduce overall power consumption. Power consumption was further minimized by implementing all transistor-based circuits as dynamic circuits and utilizing asynchronous control logic. As a result, the ADC power dissipation is frequency-dependent, consuming only leakage power when not actively converting.

The DAC of the ADC employs the Merge Capacitor Switching scheme. This scheme utilizes top-plate capacitance sampling and a common-mode voltage V_{cm} as the initial potential in capacitive DAC arrays. In the 130 nm technology, Metal-Insulator-Metal (MIM) capacitors offer the best capacitance matching but are relatively large. Therefore, the DAC employs a split capacitance scheme with six capacitances for the Most Significant Bits (MSB) and three for

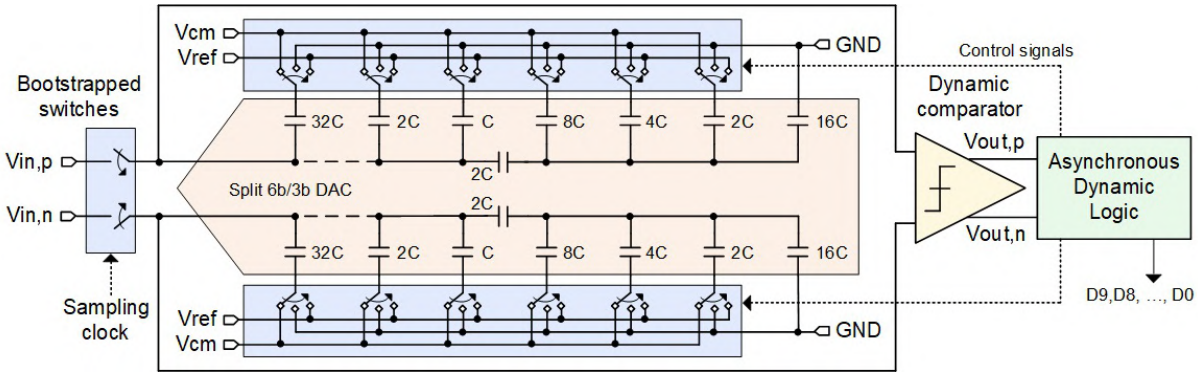

FIGURE 4.10 – *Architecture of 10-bit SAR ADC developed by AGH [66].*

the Least Significant Bits (LSB). A 16 C capacitance, not used for bit cycling, is necessary to achieve binary voltage scaling in the LSB part.

The ADC initiates its operation upon receiving a clock signal and begins conversion when the bootstrapped switches disconnect the input signal from the DAC. Initially, it compares $V_{in,p}$ and $V_{in,n}$ and stores the result in the MSB bit D_9, corresponding to the sign of the result. At this point, each capacitor of the DAC arrays is connected to V_{cm}. Subsequently, the capacitances of the DAC arrays are switched to V_{ref} or to GND based on the comparison result between $V_{in,p}$ and $V_{in,n}$ and equation 4.6.

$$V_{DAC}^{i} = \begin{cases} 0 & for\ i = 0, \\ \frac{V_{ref}}{2^{N-1}-1} \cdot \sum_{k=1}^{i} (2 \cdot D_{N-k} - 1) \cdot 2^{N-1-k} & for\ 0 < i < N-1 \end{cases} \tag{4.6}$$

In this equation, i is the comparison step index ranging from 0 to $N-1$ (where N equals 10, corresponding to the number of ADC bits), and the comparison result is denoted by D_{N-1-i} for each i output bit. The algorithm calculates the value of each bit sequentially and obtains the LSB bit D_0 without changing the DAC output voltage.

The ADC operates with analog and digital power supplies, the reference voltage V_{ref} and the common-mode voltage V_{cm}. The supply voltage is 1.2 V, equal to V_{ref}. The ADC design area is 0.088 mm². The ADC performance was measured, showing Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) within $\pm$ 0.5 LSB at a 40 MHz frequency.

The 10-bit output of the ADC is synchronized with TOT and TOA data using an Align Buffer. The ADC and the Align Buffer introduce a fixed latency of 11 bunch crossings. In the case of ADC sampling at BX = 1, the ADC data becomes available at BX = 2, while the Align Buffer transmits the output at BX = 11. The ASIC features a parameter (Clr_ADC = 1) that can force the ADC to output 0 when the TOT pulse is at 1 ; otherwise, it provides the actual ADC values. Additionally, to account for the time required for the pedestal to return to its baseline value after a TOT event, the parameter $Clr\_ShaperTail$ = 1 can force the ADC data to remain at 0 for three bunch crossings following the end of the TOT pulse.

4.3.6 TDC

The CEA IRFU group designed the TDC used in H2GCROC [67]. The TDC architecture is based on the time residue amplification method, employing three conversion blocks : a common Gray counter for the MSBs of all channels, a Coarse TDC (CTDC, 5 bits) providing intermediate bits and a Fine TDC (FTDC, 3 bits) for the LSBs. The CTDC incorporates a pulse residue

extractor, and the residue is multiplied into a train of pulses by a Pulse Replicator. Its structure utilizes delay lines, comprising a cascade of elementary digital delays.

The schematic of the TDC is presented in Figure 4.11. The TDC utilizes a 160 MHz clock generated by the ASIC PLL ; this clock sequences an 8-bit Gray counter sent to every TDC channel in the chip. When an event occurs in one channel, the counter output is captured in a register with a 25 ns coding range. A latched version of this signal (HIT) is provided by a delay flip-flop and synchronized by the 160 MHz clock to produce the FLASH signal. The Gray counter measures the time difference between the FLASH and HIT signals.

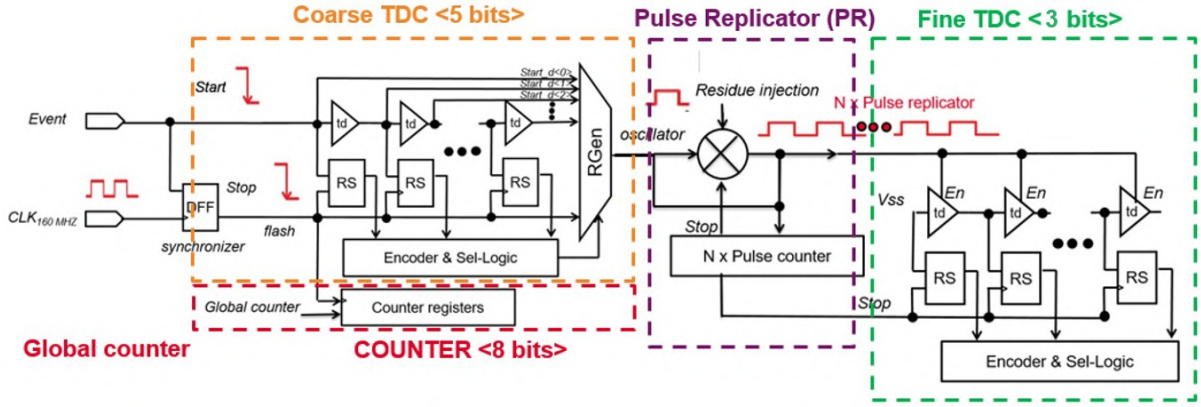

FIGURE 4.11 – *TDC schematic designed by IRFU [67].*

Subsequently, the CTDC, based on a 32-step delay line (CDL), provides 5 bits. A CDL consists of a chain of N identical digital delays with a propagation time tunable by a V_{ctrl} voltage. The first delay receives a start signal while RS latches, associated with each delay tap, capture the state of the delay line when the stop signals arrive, measuring the delay between the start and stop signals. At this point, the CDL length limits the jitter accumulation to 195 ps.

The next step improves the resolution, measuring the timing of the HIT signal inside a CDL element. First, the time residue between the HIT occurrence and the next step of the CDL is multiplied by 8 or 16 with a time amplifier before being coded by a 3-bit FTDC using another delay line (FDL). A digital block decodes and combines the data to form the TDC data in 10 bits corresponding to 25 ns with a 25 ps step. The TDC block guarantees that the conversion time will not exceed 25 ns. The radiation hardness of the block is achieved thanks to the triplication of the registers, Gray counter and the state machines, which are the most sensitive parts to single-event effects due to highly ionizing particles.

The same TDC design is configured to a 25 ps step to measure the time-of-arrival and a 50 ps step to measure the time-over-threshold. The specifications for both types of TDCs are detailed in Table 4.3. The ASIC's output sends the information of TOA in 10 bits and calculates the TOT TDC output minus the TOA information to create 12 bits of TOT information. Figure 4.12 presents how the TOT information is compressed to 10 bits before being sent to the ASIC output data. For the TOT discriminator, when it is triggered, it activates a constant current source that discharges the preamplifier. Consequently, the duration of the $outpa$ signal is directly proportional to the input charge. The current source can be adjusted using the 6-bit parameter i_tot to fine-tune the TOT signal's width (the SiPM ASIC's nominal specification is 200 ns for 320 pC).

Digital delays used in delay lines are usually sensitive to temperature, process parameter variations, voltage and irradiation damage. A delay line's stability is improved by locking the total delay of a delay chain to a reference time using a delay-locked-loop (DLL). In the ASIC, two Master DLLs control 36 channels each. Then, each channel delay line slave can be calibrated

	TOA TDC	TOT TDC
Resolution	25 ps RMS	< 50 ps RMS
Range	10 bits over 25 ns	12 bits over 2-200 ns
Power consumption	< 2 mW / channel	
Technology	TSMC 130 nm	
Area	Pitch 120 μm	
Temperature	-30° C to 65° C	

TABLE 4.3 – *TDC specifications*

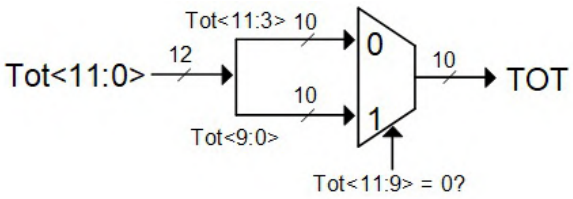

FIGURE 4.12 – *TOT compression of H2GCROC [63].*

to have the same delay as the Master DLL, reducing the dispersion between channels. In the ASIC, each channel has two TDCs, and each TDC can be calibrated, adapting first the master DLL reference voltage, then the CTDC, and finally, the FTDC [68]. The ASIC includes an asynchronous clock generator that can trigger channels for in-situ testing or calibration of the TDCs.

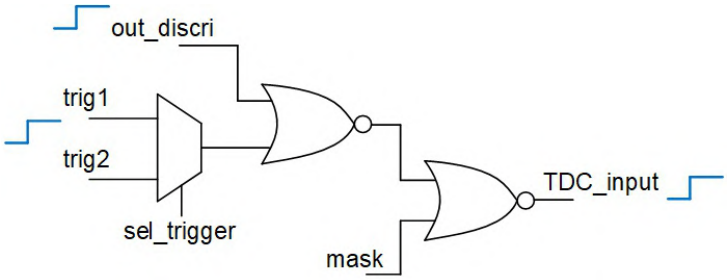

FIGURE 4.13 – *External trigger configuration for TDC calibration in H2GCROC [61].*

The ASIC has two external trigger inputs available for calibrating the TDCs. Figure 4.13 illustrates the configuration of these two inputs. Each trigger can be directed to a TOA or TOT discriminator, respectively. It's possible to inject into different channels using these two trigger signals. The ASIC also provides the option to mask the TDC outputs per channel. Since the calibration is performed channel by channel, the remaining channels must be masked when one trigger signal is injected into a particular channel.

4.3.7 Data and trigger paths

The channel information, containing the ADC, TOT and TOA data, is directed into the DAQ (Data Acquisition) path. The TOT data originates from the 12-bit output of the TOT TDC, which is compressed to 10 bits within the digital block, as depicted in Figure 4.12.

The data from each channel is continuously stored in 32-bit format at 40 MHz. The first bit indicates the T_c flag (TOT-complete), signaling that the charge information originates from

TOT. In contrast, the second bit represents the T_p flag (TOT-in-progress), indicating that a TOT event occurred in a previous BX, potentially causing ADC data corruption due to saturation or undershooting. The data content can be configured in 'Normal' or 'Characterization' modes. The characterization mode is primarily intended for debugging the chip during the development and testing phases. In this mode, after the two flags, the following 10 bits of a word contain ADC information, followed by 10 bits of TOT data and 10 bits of TOA data. In the Normal mode, the chip automatically selects the charge information source from the ADC or TOT data, transmitting 10 bits of the previous BX's ADC data, followed by 10 bits of charge information and 10 bits of TOA data. Table 4.4 summarizes the data information based on the configuration mode and the charge collected by the channel.

	Data type	Charge collection	Tc	Tp	ADC (t-1)	ADC (t)	TOT	TOA
1	Normal	$Q < TOA_{threshold}$	0	T_p	x	x		0
2	Normal	$Q < TOT_{threshold}$	0	T_p	x	x		x
3	Normal	$Q > TOT_{threshold}$	1	T_p	x		x	x
4	Characterization		T_c	T_p		x	x	x

TABLE 4.4 – *Data content of one channel for different configuration mode and charge collection [63].*

Within the ASIC, three internal counters serve to tag the data. The Bunch Crossing Counter (BX) is a 12-bit counter incremented every 25 ns cycle. It initially resets to a programmable 12-bit value (default is 1) and ranges from 1 to 3564 before wrapping around. The Event Counter (EC) is a 6-bit counter incremented after data processing for each L1A. It resets to 1 and has values from 0 to 63. The Orbit Counter (OC) is a 3-bit counter incremented with every BX wrap. It starts at 0 and ranges from 0 to 7. These three counters are triplicated to avoid errors in the information due to radiation damage.

The DAQ path starts with a 32-bit header, consisting of the BX counter, the EC to detect missed data due to RAM2 memory being full, the OC and the Hamming flags for error tracking during decoding. Subsequently, 38 words of 32-bit have the data information for each channel in one half. Among these 38 words, one contains the ADC information for the two common mode channels, and one carries the information for the calibration channel. The DAQ path structure is presented in Figure 4.14.

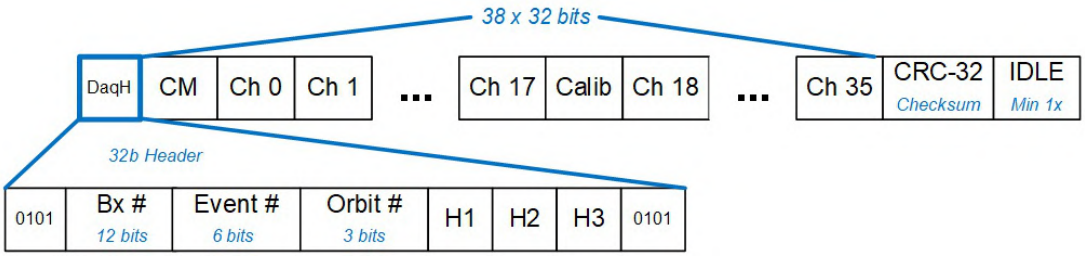

FIGURE 4.14 – *Content of a DAQ frame [63].*

For the DAQ path, the ASIC employs two DRAM memories. RAM1 is a circular memory, retaining data until an L1A command is received. Once an L1 trigger is received, the selected BX readout data is activated and synchronized with the corresponding L1 offset configured. On the other hand, RAM2 operates as a FIFO circular memory. Upon receiving the L1A command, the event data from a programmed number of bunch crossings earlier is copied into RAM2, along with the associated time tag and event counters. Subsequently, the event counter is

incremented. The chip transmits the data unless RAM2 is empty when it sends out the IDLE pattern. The serializer converts the parallel 32-bit words at 40 MHz into a serial bitstream transmitted at 1280 MHz. It also provides the Cyclic redundancy check (CRC) sum in an 8-bit counter value to check the integrity and count the number of bit shifts.

The trigger path is designed to detect significant events or conditions that serve as triggers for data acquisition. The data generated by high-energy collisions or interactions is extensive. Then, the trigger systems select and record only the most pertinent events based on energy, timing, or other characteristics for further analysis. The trigger path of the ASIC employs charge information obtained from the ADC and TOT. It contains a charge linearization block, a summing block for creating Trigger sum cells, and a charge compression component to suit the available bandwidth. Figure 4.15 illustrates how ADC2, TOT1 and charge values are determined. The six green parameters must be measured during calibration and configured through slow control.

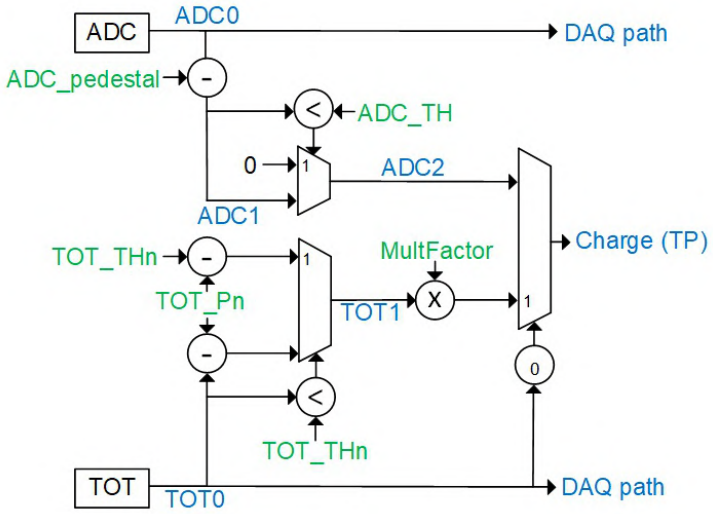

FIGURE 4.15 – *DAQ trigger path calculation [63].*

In the calibration phase, the ADC_pedestal is determined per channel. The TOT pedestal (TOT_Pn) establishes the TOT linear fit offset, while the TOT threshold (TOT_THn) sets the lower limit of the TOT linear region. Both of these parameters are established for each group of 9 channels. The ADC_TH parameter is employed for noise cancellation, and the MultFactor is utilized to convert time to charge, accounting for the ratio between TOT and ADC LSB. These parameters are configured separately for each half of the chip. Lastly, the user can choose whether to derive the charge information from the ADC or TOT data. The chip allows users to aggregate charge data from groups of 4 or 9 normal channels to generate trigger sums. Additionally, users can selectively force ADC and TOT data to zero per channel to eliminate noisy channels from the trigger sums.

4.4 Charge and time measuring techniques

The schematics and layout of H2GCROC were designed and tested using the software Cadence Virtuoso [69]. This section will present the results of the simulations performed using the tool to understand the behavior and limitations of the ASIC front-end.

Figure 4.16 summarizes the expected behavior of the front-end signal treatment after one charge injection event into the SiPM. The output data includes 30 bits, each 10 bits for the ADC, TOA and TOT information. The peak of the voltage output of the preamplifier is transformed into

a charge value by the ADC. The time measured by the discriminators is converted into digital data by the dedicated TDCs.

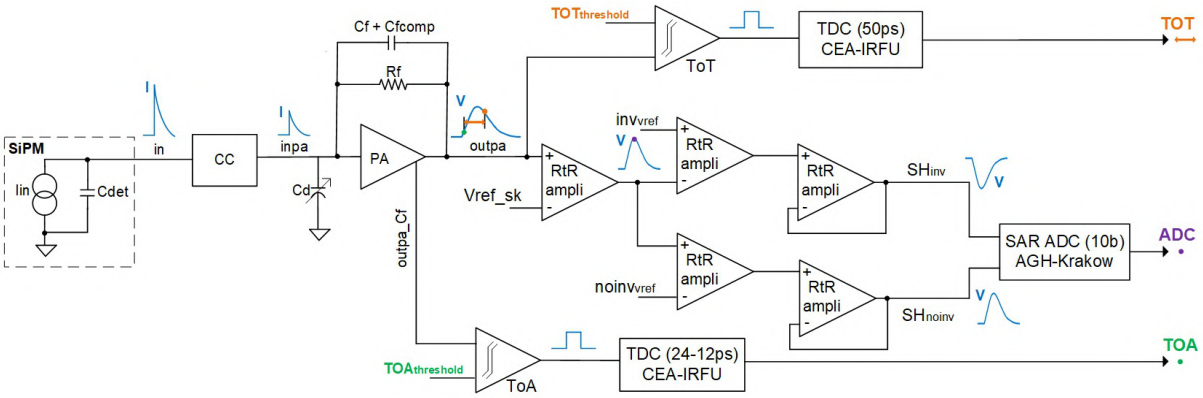

FIGURE 4.16 – *Summary of signals in the front-end after charge injection.*

The charge injection will be simulated using the ASIC's internal DACs and internal capacitors and simulating an external injection system. The charge injection response of the DACs available will be compared with simulated external charge injection. This external injection generates a voltage step with amplitude V_{inj} connected in series to a capacitor C_{inj}. The charge going into the ASIC can be calculated with the following formula :

$$Q_{inj} = V_{inj} \cdot C_{inj} \tag{4.7}$$

For this work, the SiPM will be studied in simulations with the model of Figure 3.25 and a simplified version shown in Figure 4.17, with a current proportional to the charge injected :

$$I_{in} = \frac{Q_i}{td} \tag{4.8}$$

Where Q_i is the charge of the input signal in Coulombs, and td is the pulse width of the signal.

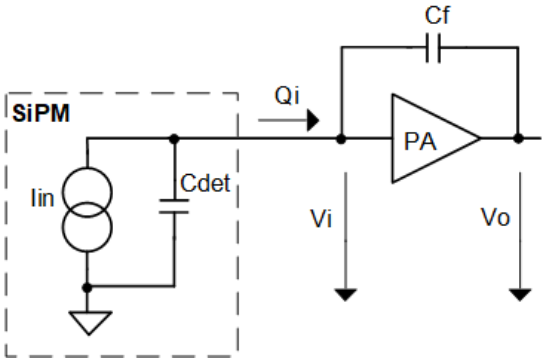

FIGURE 4.17 – *Simplified SiPM model used for Simulations.*

Most measurements will be done without the connected ADC and TDC blocks to reduce the simulation time. The calculation of ADC will be performed using equation 4.3. For time-of-arrival and time-over-threshold, the output of the corresponding discriminators will be used

to calculate the TOA and TOT. The TOT value will be the total time measured by the TOT discriminator minus the TOA time.

During the operation of HGCAL, two sets of configuration files will be used. First, the Calibration configuration with high gain is employed to detect single photons using an LED per SiPM available on the board, resulting in the gain measurement of each SiPM. Second, the Physics configuration with low noise fits the charge dynamic range. Table 4.5 presents the parameters of the two proposed configurations. The following simulations will be conducted using the physics mode configuration, and the full charge range (0 to 320 pC) will be analyzed.

Parameter	**Physics configuration**	**Calibration configuration**
Current conveyor attenuation (CC_gain)	0.075	0.3
Feedback Resistor (R_f)	11.76 $k\Omega$	16.6 $k\Omega$
Feedback Capacitor (C_f)	450 fF	300 fF
Feedback Capacitor complement (C_{f_comp})	400 fF	300 fF
Preamplifier input capacitor (C_d)	16 pF	0

TABLE 4.5 – *ASIC gain setup for the Calibration and Physics configurations.*

4.4.1 Small charge injection simulations

For small charge simulations, the output of the two shapers is converted to digital data by the differential ADC. The $outpa$ signal is not reaching the $TOT_{threshold}$; therefore, the TOT discriminator and TDC are not triggered.

The ADC receives the outputs of the shaper (SH). It has a differential input with a total range of 1 V, and it sends a 10-bit output corresponding to the charge measurement before the preamplifier saturation. The preamplifier saturation corresponds to an ADC measurement of 1023. This block works at 40 MHz and can be aligned with the peak point of the signal thanks to the phase shifter that allows correcting the frequency at 640 MHz. For ASIC calibration, the injection is repeated for several events, selecting different bunch crossings (BX) and all possible phases to find the signal's peak. Then, one BX and phase will be selected.

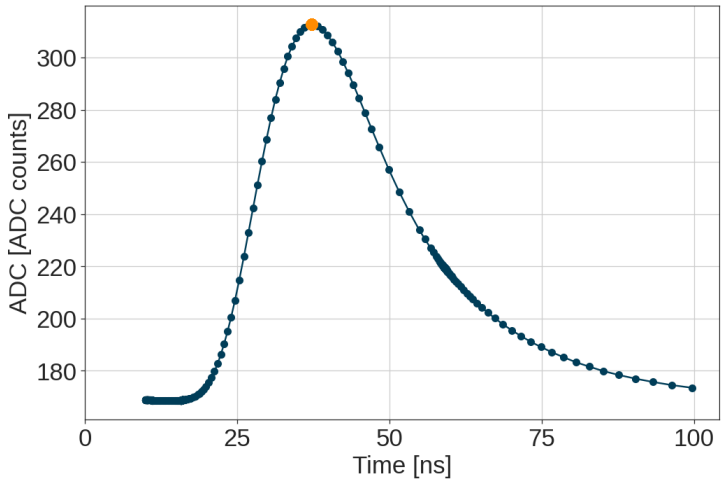

FIGURE 4.18 – *Simulation of ADC calculation to a charge injection through time using a C_{det} of 560 pF in the input of the front-end.*

Figure 4.18 shows the simulation of the calculation for one-channel ADC to a 2 pC charge injection using an injection capacitance of 3 pF and a 560 pF detector capacitance C_{det}. The total time corresponds to 4 BX, each of 25 ns and composed of 16 phases. The ASIC must configure the BX and phase closer to the peak point. In this case, it is marked with an orange point. In this plot, the pedestal was configured at a 150 ADC unit value, and the ASIC configuration produced a signal that lasted around 50 ns. After the time when the ADC reaches the peak point, the signal goes less than 20% for the next BX.

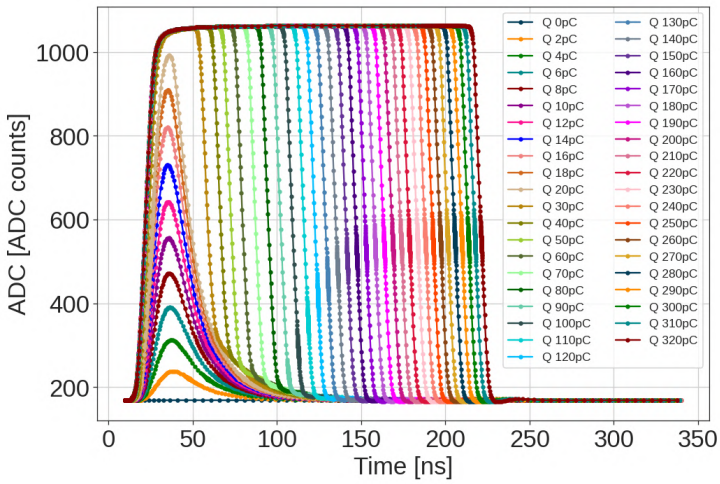

FIGURE 4.19 – *Simulation of ADC calculation to a charge injection scan using a C_{det} of 560 pF in the input of the front-end.*

Figure 4.19 presents a scan injection of different charges Q from 0 to 320 pC. The amplitude of the ADC measurement increases with charge until it reaches saturation at around 20 pC of charge injection. At this point, every charge produces saturation on the ADC, and the duration of the signal increases with the charge. It is noticeable that the duration is proportional to the charge for charges up to 150 pC and, after that, starts to reduce its increment range. For some configurations, the charge injection also produces an undershoot that lasts around 10 ns. So, in this range of charge injection, the undershoot provokes a wrong measurement on the next BX. The undershoot is produced because the preamplifier in saturation works in an open loop and takes some time to recover its normal behavior.

The charge injection scan with the sampling point selected (see Figure 4.18) generates one ADC signal per injection as seen in Figure 4.20. Charge injection above 40 pC was removed because it is in the TOT range. We can see that the ADC is producing a linear response with charge before reaching saturation.

4.4.2 Time-of-arrival simulations

The output of the TOA discriminator produces a square signal that goes to the input of the TOA TDC. The TOA calculation is taken directly from the dedicated TDC output. The TOA measurement starts when an event is triggered, passing the TOA threshold with a rising edge. The signal is stopped with the next rising edge of the 160 MHz clock from the chip's PLL. Figure 4.21 presents the discriminator response to the $outCf$ preamplifier signal output and the time measured by the TOA TDC. When the signal crosses the threshold, the discriminator passes from 0 to 1, and the TDC converts the time from the CLK signal to the trigger of the signal. The $TOA_{threshold}$ must be configured as low as possible to increase the number of events with TOA information.

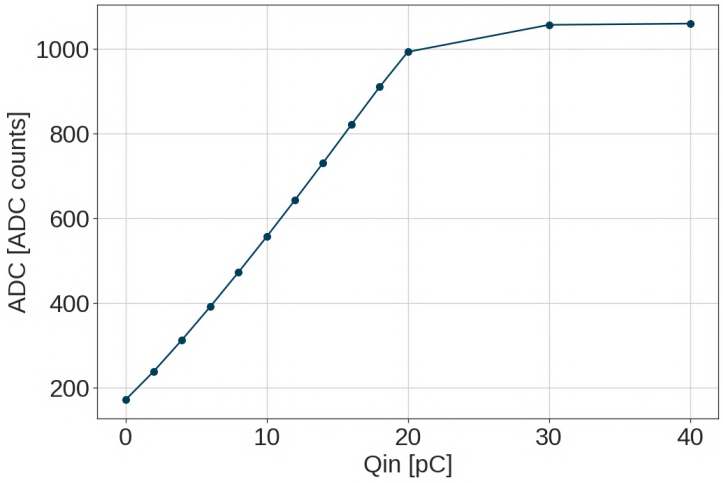

FIGURE 4.20 – *Simulation of ADC peak calculation to a charge injection scan using a C_{det} of 560 pF in the input of the front-end.*

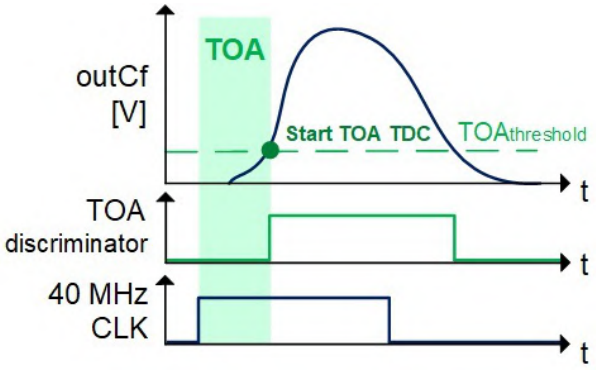

FIGURE 4.21 – *Point signals used for TOA calculation on H2GCROC [68].*

The simulation of a charge injection scan allows the TOA calculation from the TOA discriminator output. Figure 4.22 presents the time measured for charge injection from 0 to 320 pC using an injection capacitor C_{inj} of 3 pF and a detector capacitance C_{det} of 560 pF in the input channel.

Figure 4.22 a) presents a time walk of 8 ns. The rest of the TOA measurements remain stable. Figure 4.22 b) presents the jitter measured from the simulation before the TDC. The jitter calculation is performed with the following equation :

$$\sigma^{J}_{TOA} = \frac{t_{rise\_PA}}{SNR} \tag{4.9}$$

t_{rise_PA} is the time the preamplifier's output takes to pass the 10% of the total amplitude corresponding to the charge injected. SNR is the signal-to-noise ratio calculated as follows :

$$SNR = PA_{amplitude}/PA_{RMS} \tag{4.10}$$

It takes the corresponding $PA_{amplitude}$ calculated with the maximum voltage of preamplifier output minus the pedestal. PA_{RMS} comes from the simulation of rms noise at the preamplifier's output. However, these measurements correspond just to the TOA jitter of the electronics

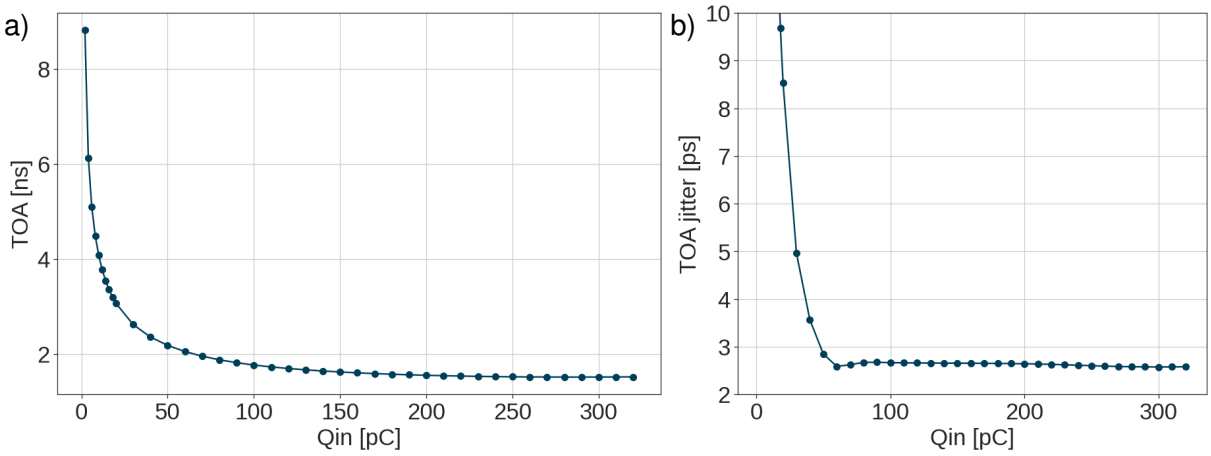

FIGURE 4.22 – *Simulation of TOA response to a charge injection scan using a C_{det} of 560 pF in the input of the front-end. a) Time measurement in ns. b) TOA jitter measured before the TDC.*

before the TDC. The total TOA jitter of one channel needs to consider the TDC contribution corresponding to $LSB/\sqrt{12}$ with an LSB of 25 ps.

4.4.3 Large charge injection simulations

The time-over-threshold technique measures the duration of a signal when the preamplifier is at saturation. The TOT value is proportional to the charge injected into the SiPM and has a time resolution of 50 ps [68]. Nevertheless, the use of the TOA data makes the calculation of TOT more precise. Contrary to the TOA calculation, the falling edge of the discriminator will trigger the TOT TDC. After that, the ASIC will subtract the TOT TDC time minus the TOA TDC measurement. Thus, the TOT available in the output data corresponds to the time from the TOA signal's rising edge to the TOT signal's falling edge. The $TOT_{threshold}$ needs to be configured as closely as possible to the saturation level of the preamplifier.

Figure 4.23 presents an example of the $outpa$ signal and the values measured by the TOA and TOT TDCs. The dotted lines show the respective thresholds configured for each discriminator. The two points in the signal mark the trigger signal for TDC calculations, and the orange shadow illustrates the time corresponding to the TOT data at the output of the ASIC.

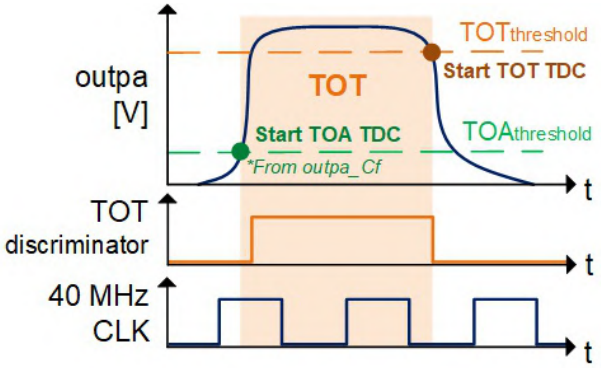

FIGURE 4.23 – *Point signals used for TOT calculation on H2GCROC [68].*

Figure 4.24 shows how the system works in the case of a pileup of different amplitude signals and the information available in the TOA or TOT TDCs. The minimal time between two

consecutive TOT events is 50 ns due to the discharge time of the preamplifier. It is possible to have an event with only TOT and not TOA data. This event happens when the preamplifier output signal does not return to its baseline after a following TOT event when a new charge arrives. Those events with TOT data that do not have a corresponding TOA event are ignored.

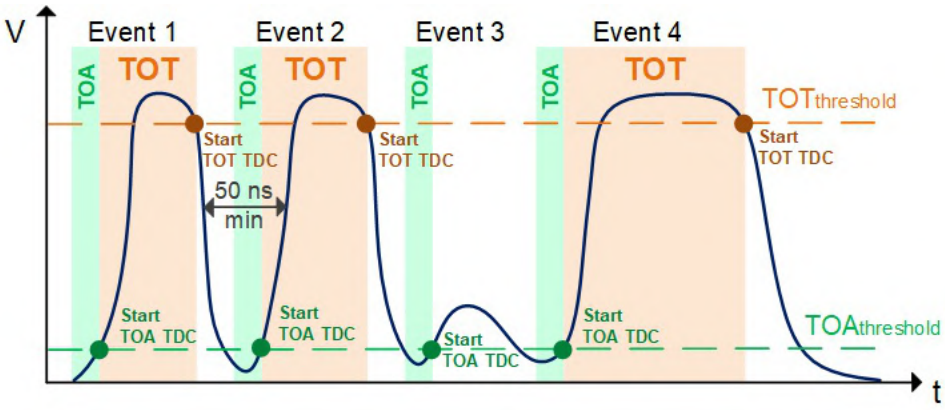

FIGURE 4.24 – *Point signals used for TOT calculation during signal pileup [68].*

The TOT measurement is part of the L1 trigger process. The information from ADC and TOA is available immediately after conversion. However, the signals producing TOT can have a duration of up to 200 ns. Therefore, the chip synchronizes the data, sending the ADC, TOA and TOT information together after a fixed delay of 12 clock periods (300 ns) since the TOA trigger.

The simulation of a charge injection scan and TOT calculation is presented in Figure 4.25. It has charge injection from 0 to 320 pC using an injection capacitor C_{inj} of 3 pF and a detector capacitance C_{det} of 560 pF in the input channel. Two effects are present : at the beginning of TOT measurements, the measurement is slow, then it becomes faster until it reaches a slow slope starting from 150 pC charge injection. The capacitance C_d connected in parallel at the preamplifier's input can improve the linearity of TOT measurements.

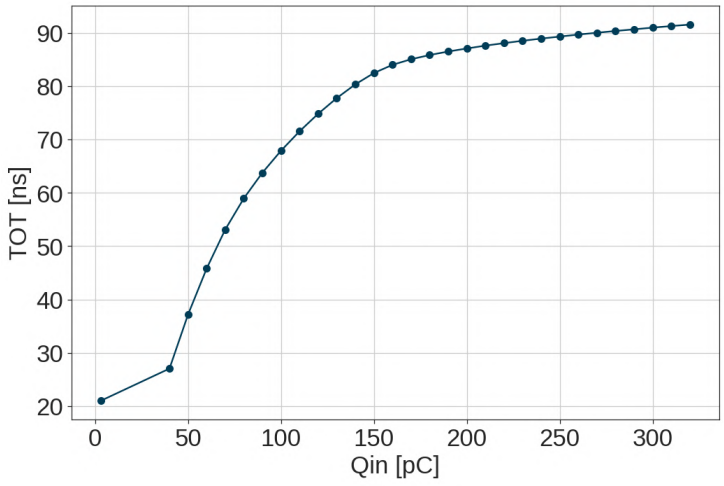

FIGURE 4.25 – *Simulation of TOT response to a charge injection scan using a C_{det} of 560 pF in the input of the front-end.*

Figure 4.26 presents the different TOT responses for the capacitance C_d available in the ASIC. We can see that higher capacitance at the preamplifier's input corrects to a better TOT linearity, especially for charges up to 200 pC. The C_d configuration must be selected to prevent

exceeding the 200 ns measurement window, ensuring good linearity across the entire TOT range. In this case, the C_d values from 5 to 7 exceed 200 ns and cannot be selected for the C_d parameter.

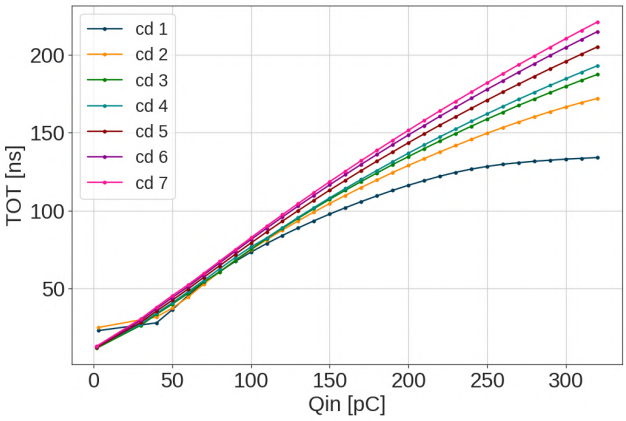

FIGURE 4.26 – *Simulation of TOT response to a charge injection scan with the different C_d values, using a C_{det} of 560 pF in the input of the front-end.*

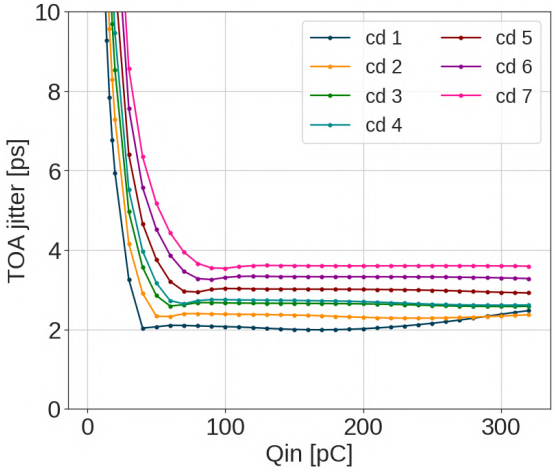

FIGURE 4.27 – *Simulation of TOA jitter to a charge injection scan with the different C_d values, using a C_{det} of 560 pF in the input of the front-end.*

Nevertheless, correcting for the TOT linearity has a price. The capacitance C_d increases the noise and can affect other measurements. Figure 4.27 presents the TOA jitter measured for a scan of C_d, increasing the jitter for higher capacitances C_d. It was found that $C_d = 3$ is a good compromise for improving linearity without significantly increasing the jitter. The simulation of a charge injection scan and TOT calculation using $C_d = 3$ is presented in Figure 4.28.

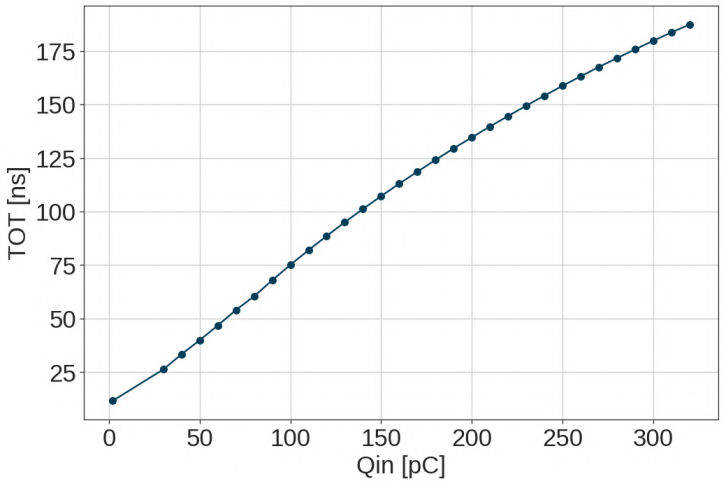

FIGURE 4.28 – *Simulation of TOT response to a charge injection scan using a C_{det} of 560 pF in the input of the front-end and C_d = 3.*

4.4.4 Noise of the system

The noise of the front-end depends mainly on two factors : the ASIC configuration and the inherent characteristics of the detector connected to the channel. The impact of the detector capacitance arises from the SiPM associated with it. Higher SiPMs will have larger detector capacitance C_{det}, leading to more noise. The ASIC design was built to read SiPMs with C_{det} of up to 1 nF. Figure 4.29 illustrates the simulated rms noise of the preamplifier for different C_{det} values and the two proposed configurations. In both configurations, larger capacitances increase the noise. However, the higher gain of the Calibration configuration results in a greater noise increment. Still, the Calibration configuration enhances the gain to characterize each SiPM during in-situ calibration, which will be performed just a few times per year during HGCAL operation.

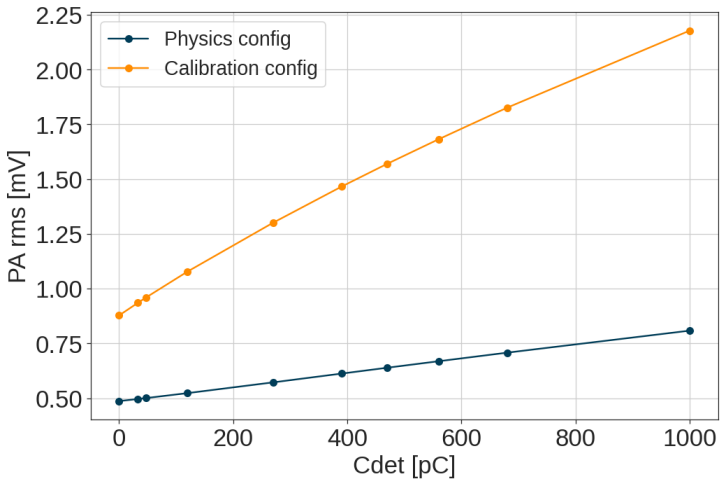

FIGURE 4.29 – *Simulation of the preamplifier rms noise for different detector capacitors C_{det} with the two proposed configurations of the ASIC.*

4.4.5 Integration of the Readout ASIC with SiPM Detectors

The current generated by a SiPM is directly proportional to the quantity of injected photons. From the different options of SiPM planned for HGCAL, two SiPM detectors were utilized. First, the Hamamatsu S14160-1315PS [53], a commercial 2 mm² SiPM with characteristics similar to those intended for use in HGCAL. This SiPM has a terminal capacitance of 100 pF. Second, the S16713 Hamamatsu pre-series SiPMs are available in three sizes (2 mm², 4 mm² and 9 mm²). These pre-series prototypes were specifically designed for HGCAL. The larger 9 mm² SiPM was chosen for testing, providing a more challenging scenario for the ASIC. Table 4.6 presents the main characteristics of the SiPM used for the simulations.

First, the influence of a single capacitor C_{det} was analyzed by connecting the equivalent capacitors of the three expected SiPM sizes of HGCAL. Table 4.7 presents the equivalent capacitance of HGCAL SiPMs.

The ADC simulation to charge injection of 2 pC using external injection with a $C_{inj} = 3pF$ is presented in Figure 4.30. Higher detector capacitances create two effects. First, they reduce the amplitude of the ADC measurement. Second, increase the rising and falling times of the measurement. Figure 4.31 presents the linearity of the peak measurement of every charge injection. We can see how larger C_{det} decreases the ADC gain of the measurements.

	S14160-1315PS	S16713-03 (ES1)	Unit
Effective photosensitive area	1.3 x 1.3	3 x 3	mm²
Pixel Pitch	15	15	μm
Number of pixels	7284	39770	pixels
Breakdown voltage	37.78	37.9	V
Gain	3.6 x 10^5	1.8 x 10^5	-
Terminal capacitance	100	530	pF

TABLE 4.6 – *Main parameters of the SiPM under test for H2GCROC characterization.*

SiPM area	Corresponding detector capacitance C_{det}
2 mm²	120 pF
4 mm²	270 pF
9 mm²	560 pF

TABLE 4.7 – *Corresponding detector capacitance for different SiPM detectors.*

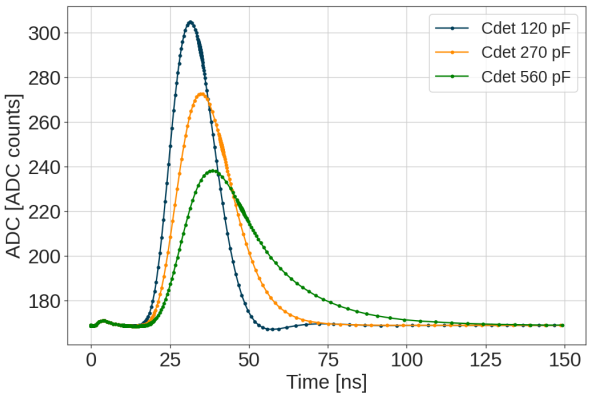

FIGURE 4.30 – *Simulation of ADC response to a 2 pC charge injection for different detector capacitances.*

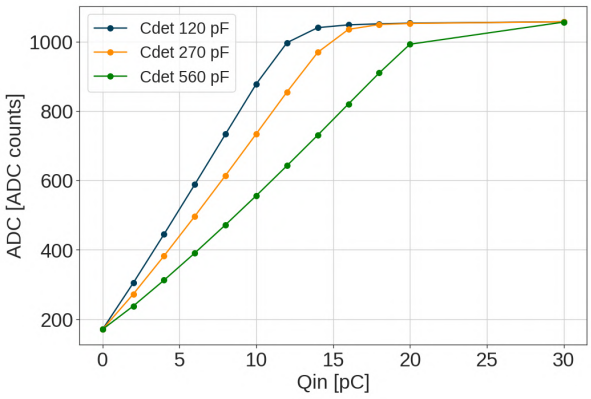

FIGURE 4.31 – *Simulation of ADC peak response to a charge injection scan for different detector capacitances.*

The TOA became slower for time measurement with the increase of C_{det}. Figure 4.32 present the TOA time walk measured. For large charge injection, all detector capacitances arrive at similar time measurements. However, small charge injection suffers the effect of rising edge reduction on larger C_{det}. The TOT measurement during preamplifier saturation has a contrary effect. As we saw before, the capacitor C_d in the preamplifier's input improves the linearity of TOT measurements, producing slower rising and falling times in the signal. Figure 4.33 presents the TOT measured with $C_d = 3$ to see the effect of the different detector capacitances.

If we simulate a current signal using the SiPM model (see Figure 3.25), we can see a closer effect of the expected at the HGCAL operation. The effects are the same as with the use of C_{det} but have an incremented effect, especially in the slow falling time of the signal. Figure 4.34 compares the shape of the signal response of the models of the two SiPMs under test. Figure 4.35 presents the linearity of the measurements and the different gains $ADC/Charge$ achieved.

For the rest of the charge dynamic range, both SiPMs create a prolonged end of the signal that takes around 2 BXs to recover the normal behavior of the preamplifier. Figures 4.36 and

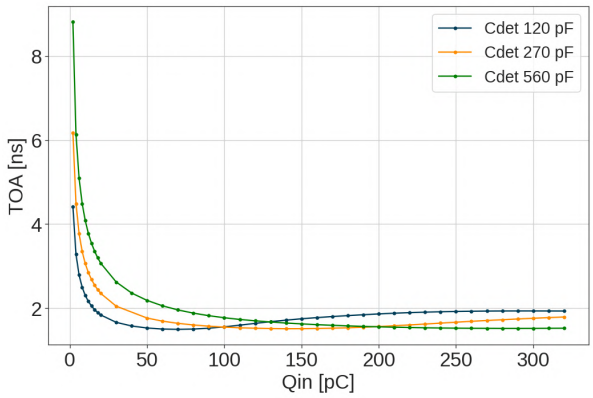

FIGURE 4.32 – *Simulation of TOA response to a charge injection scan for different detector capacitances C_{det}.*

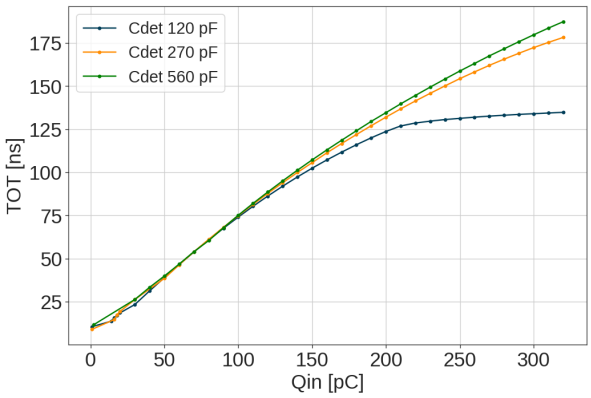

FIGURE 4.33 – *Simulation of TOT response to a charge injection scan for different detector capacitances C_{det}.*

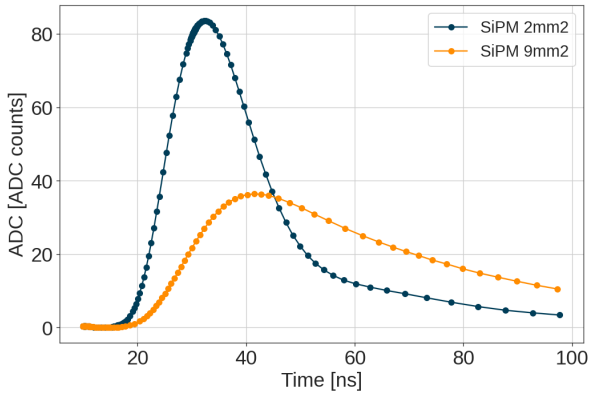

FIGURE 4.34 – *Simulation of the comparison of an ADC sampling scan for a 1 pC charge injection using the 2 mm² and 9 mm² SiPM models.*

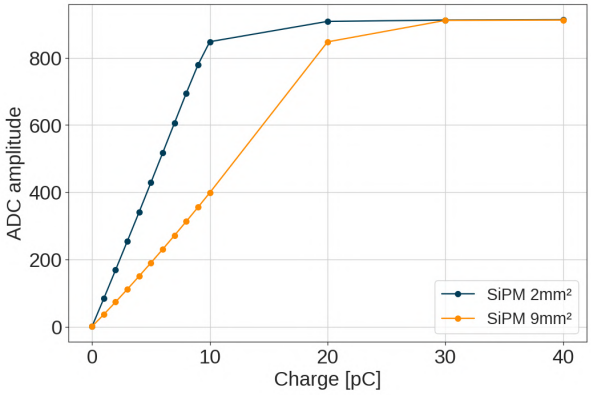

FIGURE 4.35 – *Simulation of the comparison of an ADC response to a charge injection scan using the 2 mm² and 9 mm² SiPM models.*

4.37 show the shape response of the ADC calculation for charge injection up to 320 pC. The time of the front-end to recover the DC level to the pedestal is more extensive with the 9 mm² SiPM.

Figure 4.38 compares the TOA simulated with both SiPMs. Although the time walk is larger with the 9 mm² SiPM, the 2 mm² SiPM presents a bump for signals larger than 100 pC. The TOT with the SiPMs (Figure 4.39) stays in the 200 ns limit and shows a clear difference with the starting charge injection that reaches the preamplifier saturation. The TOT measured with the 9 mm² SiPM has a slightly improved linearity compared to the 2 mm² SiPM.

The advantage of using the SiPM model, as opposed to just using a capacitor in parallel to the input, is that we can simulate the effect of the number of cells in a SiPM. Each cell has a dedicated parasitic capacitance that adds up to the total capacitance of the detector. Figures 4.40 and 4.41 illustrate the effect on ADC measurements while maintaining the total parasitic capacitance C_g of the detector constant and only changing the number of cells with their dedicated parasitic capacitance. In both detectors, we can see that even though the parasitic capacitance of a cell is small, the combined effect of all cells is not negligible and needs to be considered if we want to use an equivalent detector capacitance in the tests.

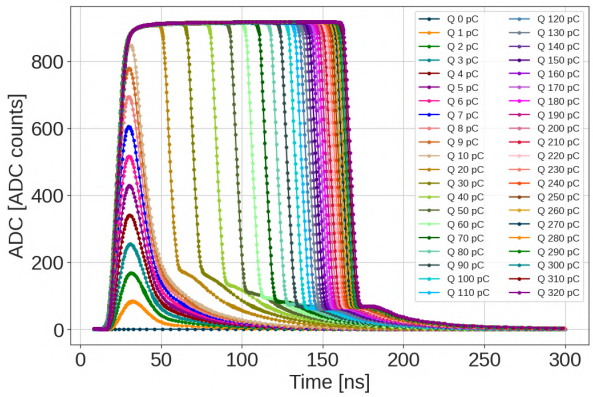

FIGURE 4.36 – *Simulation of an ADC sampling scan for different charge injection using the SiPM 2 mm² model.*

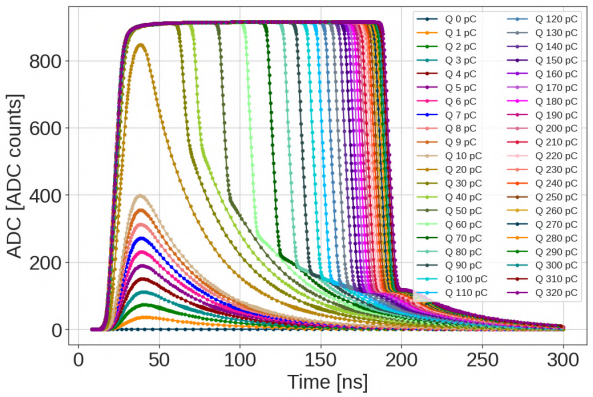

FIGURE 4.37 – *Simulation of an ADC sampling scan for different charge injection using the SiPM 9 mm² model.*

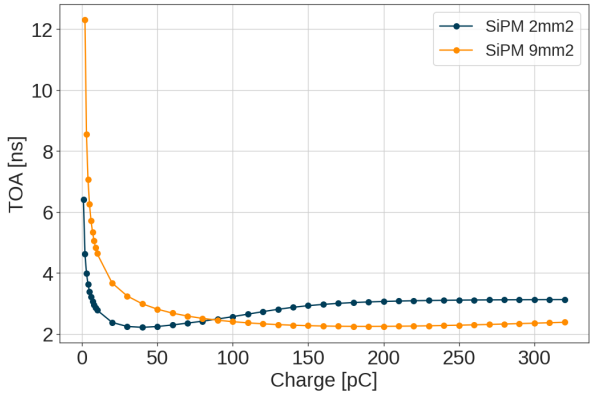

FIGURE 4.38 – *Simulation of the comparison of a TOA response to a charge injection scan using the 2 mm² and 9 mm² SiPM models.*

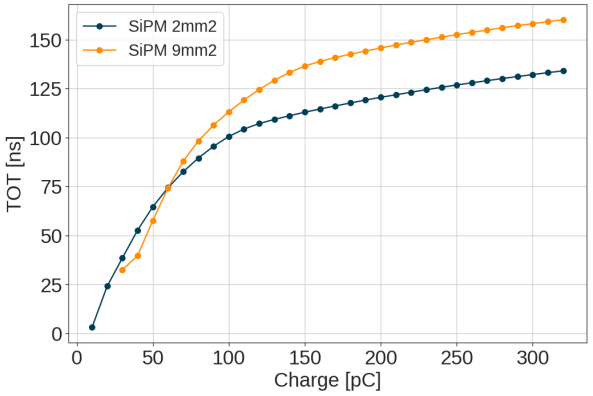

FIGURE 4.39 – *Simulation of the comparison of a TOT response to a charge injection scan using the 2 mm² and 9 mm² SiPM models.*

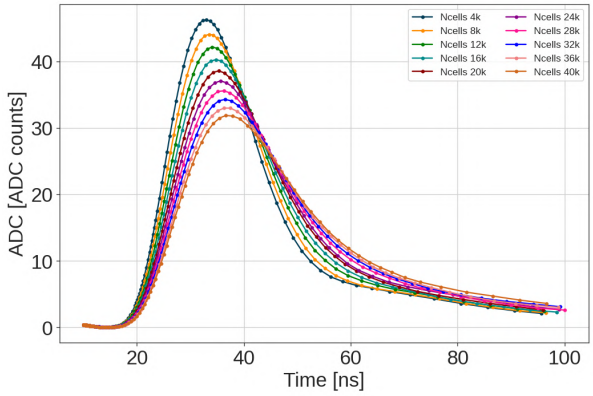

FIGURE 4.40 – *Simulation of the effect of the number of cells of a 2 mm² SiPM model in the ADC response.*

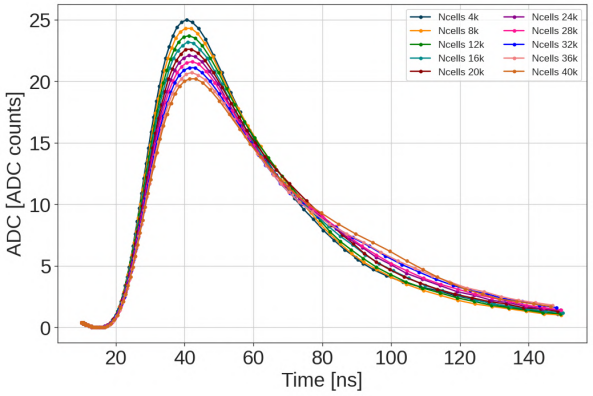

FIGURE 4.41 – *Simulation of the effect of the number of cells of a 9 mm² SiPM model in the ADC response.*

The results obtained from the simulation performance of the front-end appear promising. The ASIC demonstrates the capability to read SiPMs with different characteristics. The pur-

pose of these simulations is to comprehend the chip's performance under various conditions. The measurements conducted in this section will serve as the anticipated behavior for actual measurements on a fabricated chip.

4.5 Methodologies for Calibration of the ASIC

H2GCROC features a robust set of parameters that facilitate the configuration of gain, shape, time thresholds, reference voltages and more, allowing for precise measurements of charge and time. The ASIC is designed to adapt to incoming signals from SiPMs with varying characteristics while compensating for fabrication mismatches, irradiation damage and temperature variations. This section will present the calibration modules of the ASIC front-end, providing an in-depth exploration of the necessary calibration process required before the chip is prepared for operation in the experiment.

4.5.1 Analog and reference voltage probes

The initial step in ASIC calibration involves configuring the necessary reference voltages and currents to ensure the stability of the analog blocks and achieve the intended DC voltage ranges for the design.

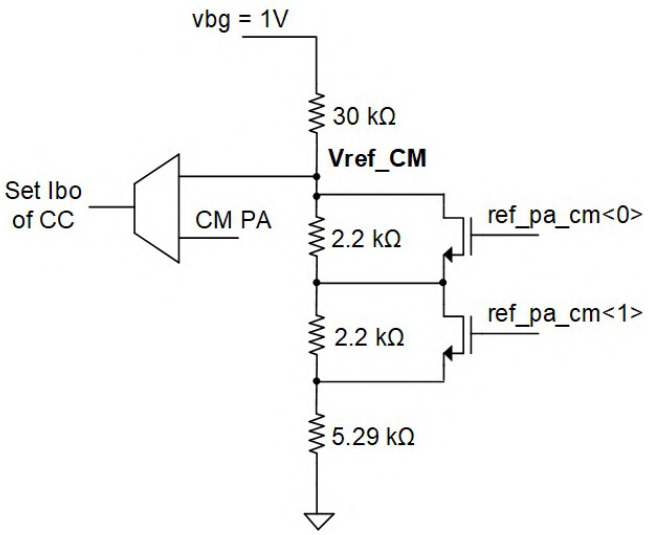

FIGURE 4.42 – *Reference voltage setting for I_{bo} compensation at the current conveyor.*

The current conveyor features the I_{bi} parameter, which sets the current into the input chip-wise. This parameter, consisting of six bits, utilizes the three most significant bits connected to 2.5 V, while the three least significant bits are configurable through slow control. The current I_{bo} from a common mode channel can compensate for this current ; its compensation range is tuneable by the 2-bit parameter, ref_pa_cm. The reference voltage $Vref\_CM$ can be configured to 150, 200, or 250 mV using ref_pa_cm. Figure 4.42 illustrates the circuit configuring common mode compensation for the current conveyor.

The preamplifier is equipped with a 6-bit parameter to configure its current bias. Furthermore, each amplifier within the total shaper block allows the configuration of its input and output currents using either 2 or 6 bits, as applicable. The current conveyor, preamplifier, shaper and TDC can be individually activated or deactivated through global parameters. For example, the

ON_pa parameter can deactivate all preamplifiers with one configurable bit. The ADC parameters, including input stage current and a 12-bit delay for ADC conversion tuning, can also be configured. Each TDC includes parameters for adjusting the Master DLL, gains, latency time, the replicator, CTDC and FTDC.

The internal DACs' outputs, used for calibration, reference voltages, or currents, can be monitored through two pins. $Probe\_DC1$ can be configured to read one of the 64 available probes, while $Probe\_DC2$ allows for the reading of the calibration DAC for charge injection into the preamplifier.

4.5.2 Channel trimming

After configuring the currents and reference voltages for the analog blocks, it is necessary to set the pedestal of each channel to the same ADC level. In the shaper configuration, the user is required to globally adjust the two 10-bit DACs (inv_{vref} and $noninv_{vref}$) to establish the DC levels of the inverter and non-inverter shapers, respectively. These parameters set the ADC pedestal. A 6-bit DAC per channel ($trim_{dac}$) can be employed to minimize dispersion per channel.

The channel trimming process initiates by establishing the two reference voltages for the shaper. This step can be automated using the available circuit on the chip that creates a dynamic range of 1 V between the two shaper outputs. This dynamic range ensures the pedestal is positioned close to 10% of the ADC dynamic range. Subsequently, the user can conduct a $trim_{dac}$ scan for each channel to determine the optimal value that results in the lowest pedestal level and less dispersion per channel. This process not only aligns the pedestals but also optimizes the noise levels of the analog front-end.

4.5.3 Internal Injection

The ASIC incorporates two 12-bit DACs for internal charge injection into each chip channel. Figure 4.43 illustrates the circuits controlling the charge injection within the ASIC. The $calib\_dac$ generates charge injection into the preamplifier, ranging from 0 to 1.2 V. The $calib\_dac$ converts the voltage in charge with an internal capacitor. It has two capacitors per channel : one with a capacitance of 500 fF and another with 8 pF, designated for low and high injection.

On the other hand, $calib\_dac\_2V5$ permits injection within the range of 0 to 2.5 V to the current conveyor. It relies on a single 3 pF capacitor per channel for charge conversion. For high-range injection into the current conveyor, the 3 pF capacitor of each channel within the 39 channels of one half is linked to the current conveyor input of the injected channel, resulting in a combined capacitance of 117 pF per half. It's important to note that injection directly into the current conveyor uses the capacitors associated with each channel and cannot be performed simultaneously in multiple channels.

Table 4.8 describes the parameters necessary to configure each injection mode of the chip. Two fast commands enable internal or external injection : The 'CalPulseInt' command sends the STROBE pulse to the internal calibration DAC with a length of 32 BX at 40 MHz (800 ns). To enable the external signal $SiPM\_calibration$, the 'CalPulseExt' fast command sends the STROBE pulse to the external pin with a duration of 100 ns. The phase of the STROBE pulse can be adjusted using slow control.

The $calib\_dac$ output was simulated, demonstrating good linearity and a 1 V dynamic range with a 3 mV offset (see Figure 4.44) ; this corresponds to a charge injection into the preamplifier of 0 to 500 fC for the low range and 0 to 8 pC for the high range. Figure 4.45 presents the simulation of the $calib\_dac\_2V5$. In this case, the results were not as good as expected. The

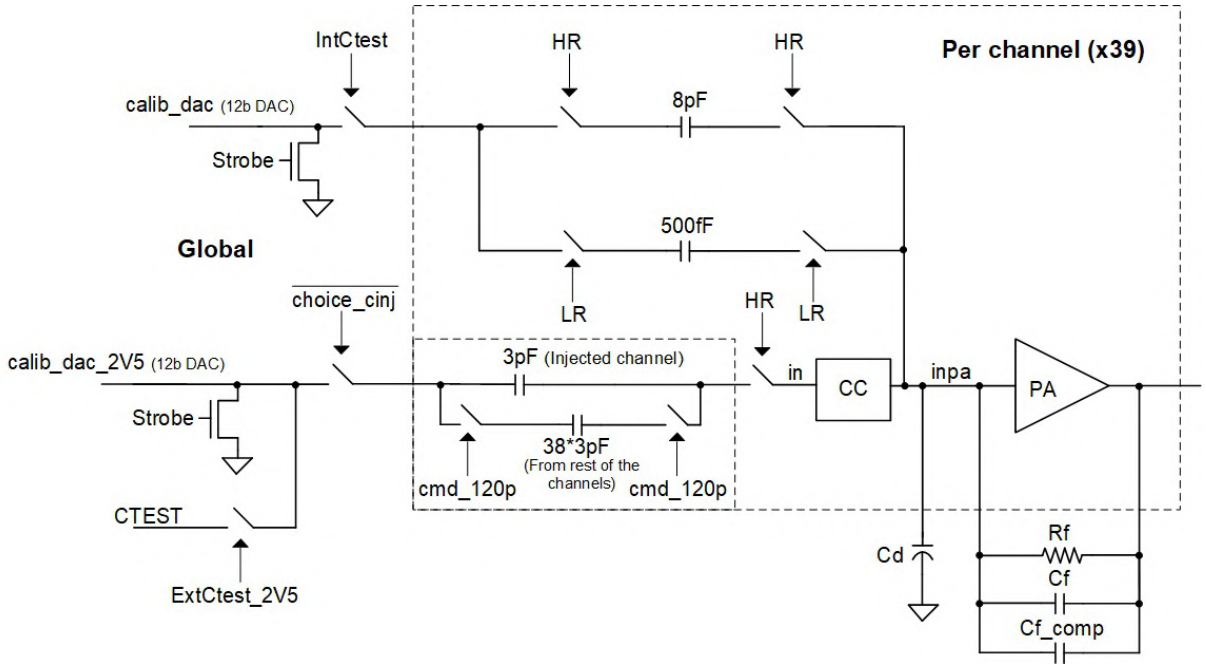

FIGURE 4.43 – *Internal and External injection schematic.*

IntCtest	ExtCtest_2V5	LR	HR	choice_cinj	cmd_120p	Injection type
1	0	1	0	1	X	preamplifier Low Range
1	0	0	1	1	X	preamplifier High Range
0	0	X	1	0	0	Current conveyor Low Range
0	0	X	1	0	1	Current conveyor High Range
0	1	X	1	0	0	Current conveyor external [CTEST · 3 pF]
0	1	X	1	0	1	Current conveyor external [CTEST · 117 pF]

TABLE 4.8 – *Logic to enable internal or external injection into the ASIC.*

dynamic range is limited from 2.5 V to 980 mV, corresponding to charge injection into the current conveyor of 0 to 4.56 pC for low-range and 0 to 177.84 pC for high-range injection.

Both DACs were tested in simulation to inject charge in one ASIC channel. Figure 4.46 presents the low-range injection into the preamplifier using $calib\_dac$ and the 500 fC capacitor of the chip. Figure 4.47 gives the results of the high-range injection into the pramplifier. Both measurements deliver good linearity and shape.

The $calib\_dac\_2V5$ DAC simulation of low-range is illustrated in Figure 4.48. Noticeably, the linearity of the measurements is decreasing, especially for $calib\_dac\_2V5$ values above 2000. Figure 4.49 presents the results of the high-range injection. The shape of both injections is good, but the high-range injection suffers from the higher injection capacitor (117 pF), causing a small bump for charges above the preamplifier saturation.

Additionally, the election of an injection capacitor impacts the charge injection, affecting the amplitude and speed of the injection. Figure 4.50 illustrates the simulated injection of the same charge, creating a voltage step that converts the charge using different injection capacitors C_{inj}.

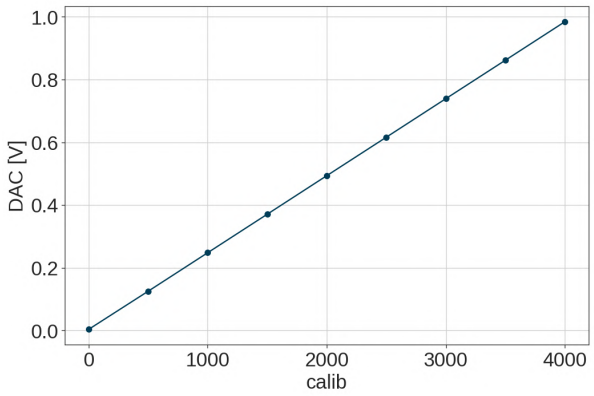

FIGURE 4.44 – *Simulation of the 1.2 V DAC for charge injection into the preamplifier.*

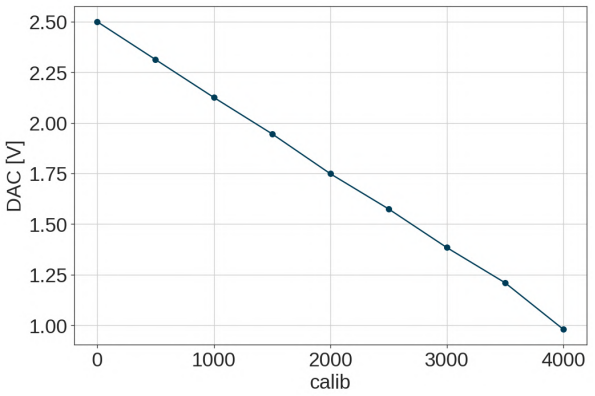

FIGURE 4.45 – *Simulation of the 2.5 V DAC for charge injection into the current conveyor.*

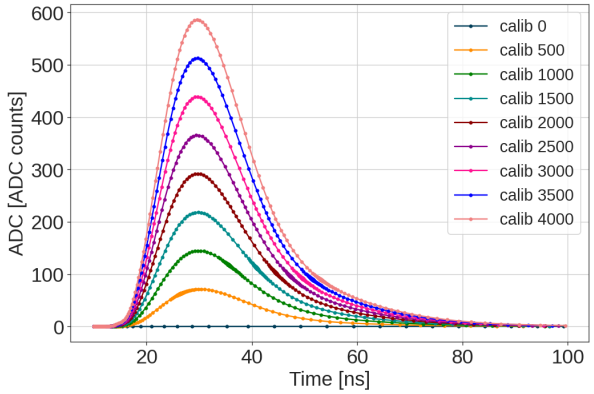

FIGURE 4.46 – *ADC simulation minus pedestal of the charge injection into the preamplifier using the Low Range of the 1.2 V DAC.*

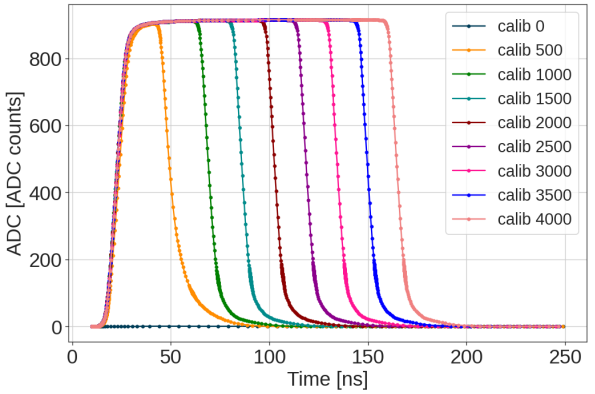

FIGURE 4.47 – *ADC simulation minus pedestal of the charge injection into the preamplifier using the High Range of the 1.2 V DAC.*

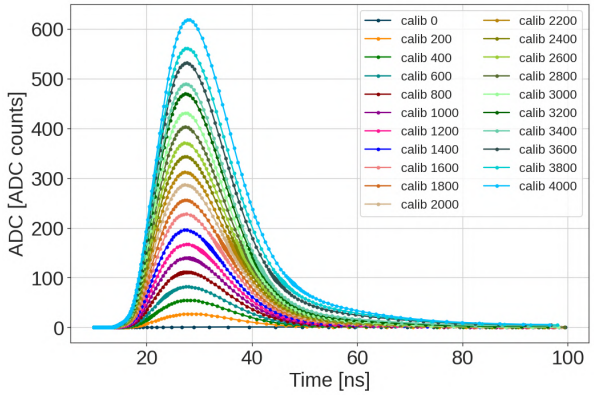

FIGURE 4.48 – *ADC simulation minus pedestal of the charge injection into the current conveyor using the Low Range of the 2.5 V DAC.*

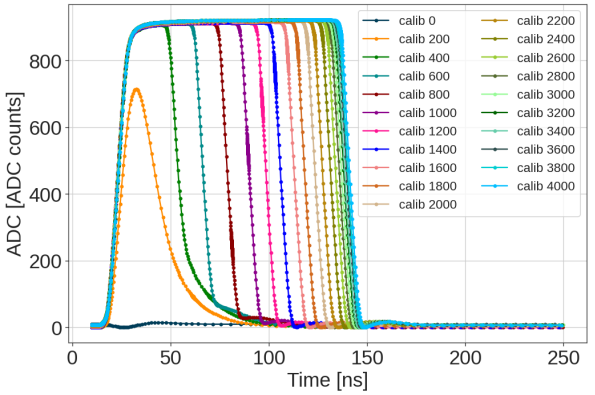

FIGURE 4.49 – *ADC simulation minus pedestal of the charge injection into the current conveyor using the High Range of the 2.5 V DAC.*

Charge injection that uses C_{inj} below 10 pC has less noise, leading to a more reliable injection. On the contrary, using a $C_{inj} = 117\ pF$, as in the high-range injection into the current

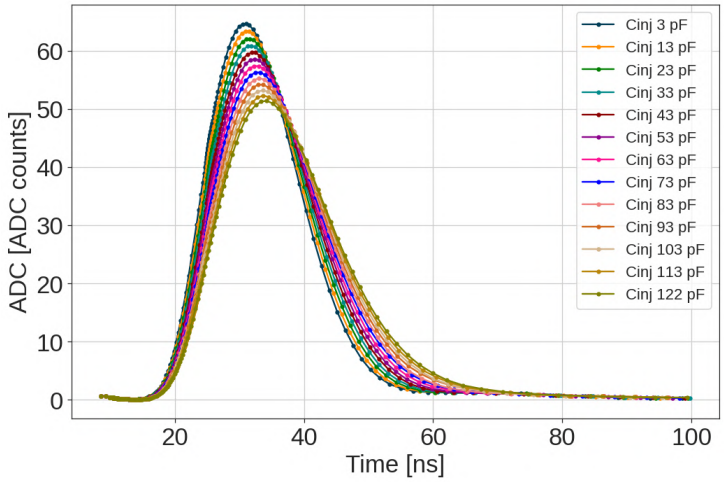

FIGURE 4.50 – *Simulation of the effect of the injection capacitor C_{inj} to the injection of the same charge in the front-end.*

conveyor, generates a considerable extra noise source. The signal also becomes slower, and the shaper cannot reduce the signal below 20% for the next bunch crossing. Therefore, the high-range injection can be used to test the chip's capability to read large charges. But, it will not present the real noise expectations or signal speed. The change in shape on the injection affects the ADC gain, the time walk of TOA and the TOT measurements.

4.5.4 Gain calibration of the FE

The gain of the front-end is configurable in two steps. First, the current conveyor can attenuate the current generated by the detector with a 4-bit parameter CC_gain. The attenuation factor goes from 0 to 0.375 with a 0.025 step. Figure 4.51 shows the ADC response with the different attenuations available.

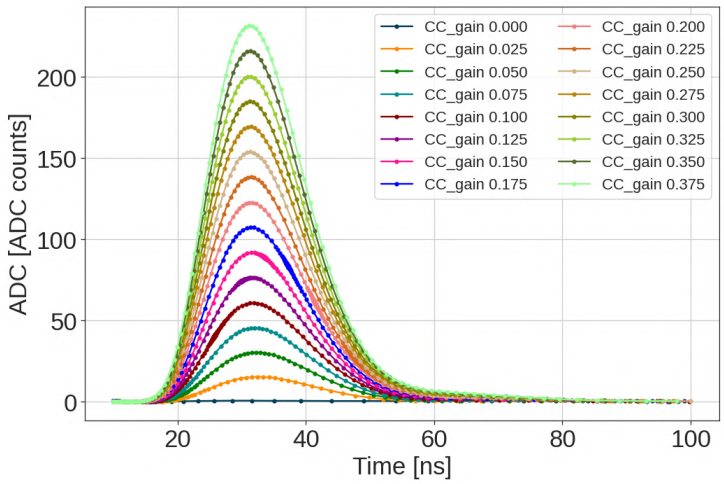

FIGURE 4.51 – *Simulation of the ADC response to a 553 fC injection for the different attenuation configurations of the current conveyor.*

The output of the current conveyor is coupled with the preamplifier's input. The preamplifier converts the current to a voltage and amplifies it using one feedback resistor R_f and two feed-

back capacitors C_f and C_{f_comp}. The total feedback capacitance is the sum of the two feedback capacitors that are connected in parallel :

$$C_{f\_total} = C_f + C_{f\_comp} \tag{4.11}$$

The time of the preamplifier's output is calculated with the time constant $R_f \times C_{f\_total}$. If the $R_f \times C_{f\_total}$ is maintained stable, the values of R_f determine the preamplifier gain. Figure 4.52 presents an R_f scan using a $R_f \times C_{f\_total} = 25ns$. Reducing the preamplifier's time constant reduces the signal's time and increases its amplitude. The selection of feedback resistors and capacitors needs to be done carefully. Increasing the gain will also amplify the rms noise of the preamplifier.

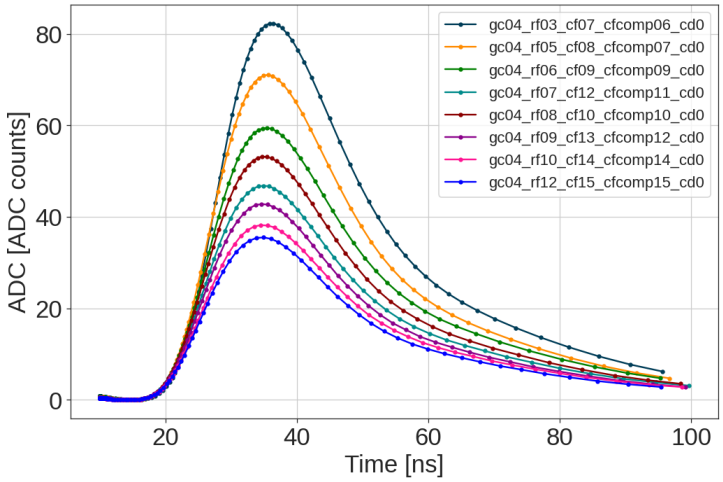

FIGURE 4.52 – *Simulation of the ADC response to a 553 fC injection for different preamplifier's gain configurations maintaining an* $R_f \times C_{f\_total} = 25ns$.

4.5.5 Calibration for SiPM detectors

The gain of the SiPM can vary significantly with slight adjustments in the applied voltage over breakdown voltage, with potential deviations of up to 7% for a 100 mV variation [83]. Consequently, it is advisable to incorporate an adjustable voltage input within the front-end design. This voltage input compensates for the disparities in SiPM characteristics and temperature variations, facilitating calibration across different SiPMs.

The calibration of SiPMs connected to the ASIC channels is performed first with a photon injection in every channel, resulting in the $ADC/p.e.$ measurement. The V_{dac} is an internal DAC available channel-wise that configures the DC level of the channels with a variation range going from -1.4 V to +750 mV. The V_{dac} is configurable with 6 bits and is configured first to its middle value $V_{dac} = 31$. After measuring the SiPM gain, we can perform an V_{dac} scan in every channel to select the value that creates the same $ADC/p.e.$ gain in all SiPMs. Figure 4.53 illustrates the simulation of the input voltage for the different configuration values of the V_{dac} of one channel. The correction in the DC level corrects the high voltage of the SiPM that affects the detector's gain.

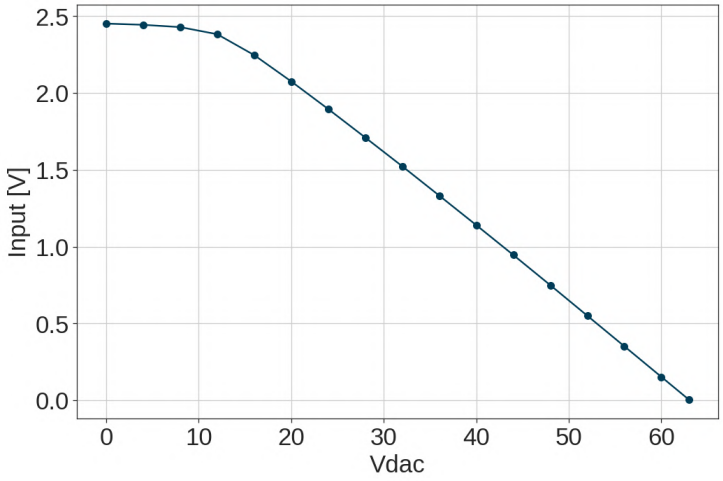

FIGURE 4.53 – *Simulation of input voltage for a scan of the V_{dac} DAC values.*

4.5.6 SiPM Leakage current compensation

An irradiated SiPM will maintain its performance but create a leakage current that increases with time under irradiation. This current in the SiPM goes to the channel's input and is reduced by the same attenuation factor configured in the current conveyor. Then, if not corrected, it passes through the feedback resistor of the preamplifier, and the DC level of the preamplifier output follows this leakage current, reducing the dynamic range. The 6-bit DAC ($dacb$) can create an opposite current that compensates for this effect, maintaining the same behavior previously obtained with a non-irradiated SiPM.

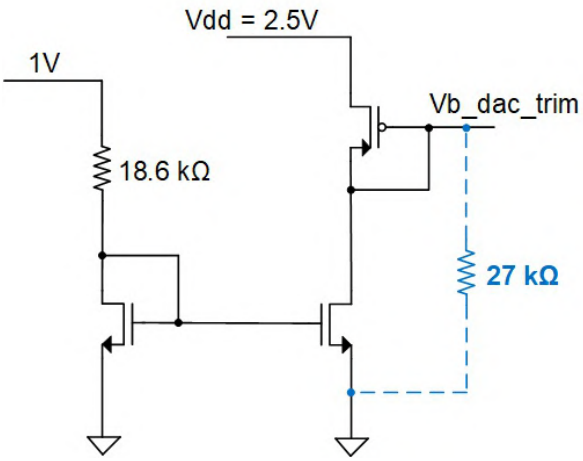

FIGURE 4.54 – *Circuit of the use of Vb_dac_trim and the external resistor connected to adapt the $dacb$ dynamic range of H2GCROCv2.*

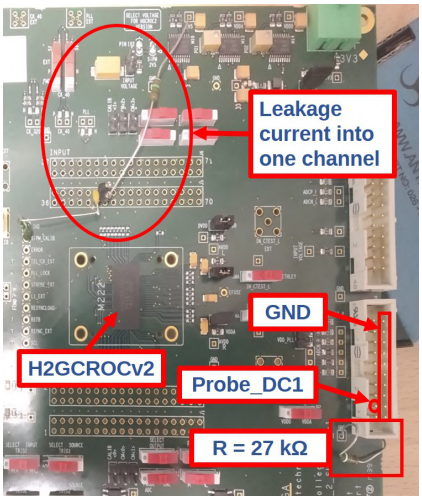

FIGURE 4.55 – *Photograph of the H2GCROCv2 testbench with external leakage current and an external resistor connected to Vb_dac_trim to adapt the $dacb$ dynamic range.*

In the second version of H2GCROC, the $dacb$ could compensate up to approximately 290 μA. Studies on irradiated SiPMs present leakage currents larger than 1 mA. Therefore, the leakage current compensation of the front-end was not sufficient. A contribution of this thesis

was understanding the circuit present in H2GCROCv2 and making the necessary modifications to increase the range of leakage current compensation.

First, a resistor was connected from a voltage source to the channel input of the second version of the ASIC to inject an external current. Larger leakage currents increase the pedestal level of the front-end. As mentioned in section 4.5.1, the chip has a $Probe\_DC1$ pin that can read some reference voltages. The $Probe\_DC1$ output of the ASIC was configured to read the Vb_dac_trim voltage. Vb_dac_trim controls the step of the DAC used to create the $dacb$ current. Then, an external resistor was connected from the $Probe\_DC1$ pin to the ground to increase the dynamic range of the DAC. Figures 4.54 and 4.55 illustrate how the external resistor was connected in the test bench of H2GCROCv2. It was found that a resistor value of 27 kΩ allows the leakage current correction of values up to 1.3 mA.

The test with H2GCROCv2 showed that increasing the $dacb$ dynamic range was possible with an extra resistor that changes the Vb_dac_trim voltage. The solution was to add two additional resistors configurable with the 2-bit parameter $Dacb\_dynran\_config$. Figure 4.56 presents in green the changes implemented for the third fabricated version of the chip.

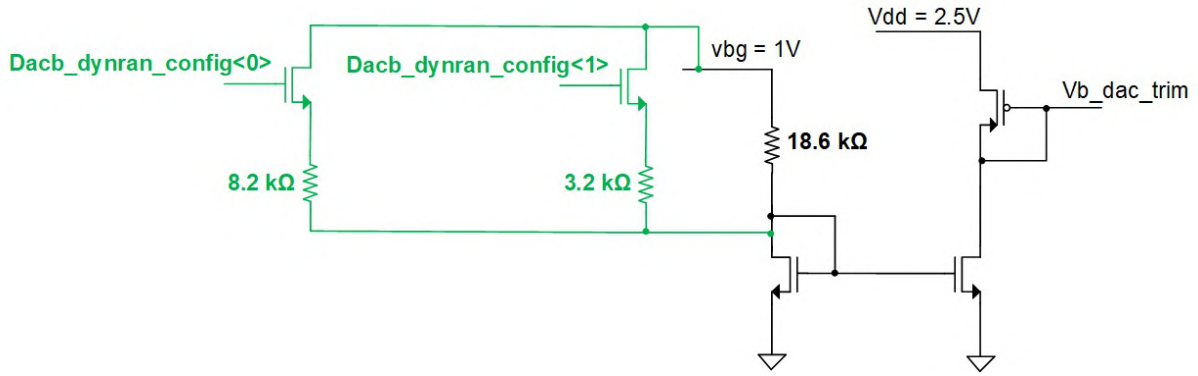

FIGURE 4.56 – *Leakage compensation schematic. In black is the circuit of H2GCROCv2, and in green is the additional circuit added to H2GCROCv3.*

If $Dacb\_dynran\_config = 3$, the $dacb$ correction has the same range as in the second ASIC version. Connecting the extra resistors increases the leakage current correction range but decreases the $dacb$ resolution. The work to implement this correction included the simulation tests and the layout design modifications on the new chip version.

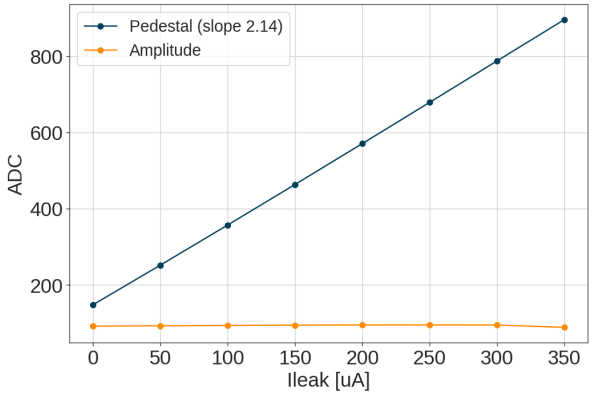

FIGURE 4.57 – *Simulation of the leakage current effect at the input of one channel.*

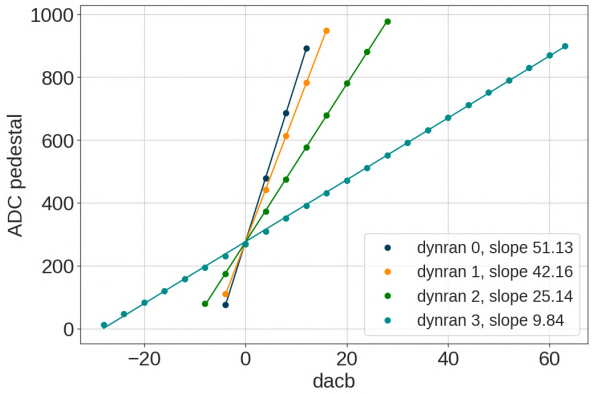

FIGURE 4.58 – *Simulation of pedestal slope variation for the different $dacb$ and $Dacb\_dynran\_config$ parameters.*

A simulated current was connected to one channel input to understand the impact of leakage currents on the ADC amplitude and pedestal and test the new solution. Figure 4.57 shows that the current increases the pedestal and maintains a constant amplitude on the signal. Using the Physics configuration of the chip, the preamplifier stays before saturation with currents up to 350 μA. Figure 4.58 illustrates how $dacb$ can inject a current that oppositely moves the pedestal. The slope of the $dacb$ correction increases when adding resistors with $Dacb\_dynran\_config$, allowing for more leakage current correction. The $sign\_dac$ parameter is used to configure the direction of the $dacb$ current.

The results are summarized in Table 4.9. The solution implemented increases the leakage current compensation from 290 μA to 1.31 mA using the Physics configuration in the ASIC.

Dacb_dynran_config	$dacb$ slope	Leakage current correction range	Max $dacb$ current	OUTPA pedestal step
0	51.13	0 to 1.31 mA	$\sim$ 109 μA	$\sim$ 32.96 mV
1	42.16	0 to 1.09 mA	$\sim$ 90 μA	$\sim$ 27.2 mV
2	25.14	0 to 660 μA	$\sim$ 54 μA	$\sim$ 16.4 mV
3	9.84	0 to 270 μA	$\sim$ 21 μA	$\sim$ 6.45 mV

TABLE 4.9 – *Calculations for leakage compensation from the different configurations available in H2GCROCv3.*

4.6 Conclusion

The H2GCROC architecture presented in this chapter underscores its robust design and capabilities. The ASIC has demonstrated fulfilling the HGCAL requirements in simulation, showing its proficiency in reading SiPMs with diverse characteristics. The chip has a high degree of configurability, with parameters to adjust the gain, shape and time thresholds, allowing for precise measurements of both charge and time. The simulation results provide insight into the chip's behavior under different conditions, helping in the configuration and analysis of its performance.

In summary, the robustness demonstrated in the ASIC reflects its ability to meet the demanding requirements of SiPM readout in high-energy physics experiments. The next chapter will explore the performance of the third fabricated version of the ASIC. The knowledge gained from this chapter will form the basis of the testing strategy and provide a benchmark against which the actual performance can be evaluated.

Chapter 5

H2GCROC ASIC Characterization

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5.1 Introduction

Characterizing an Application-Specific Integrated Circuit (ASIC) is crucial in developing a chip, especially in fields like particle physics, where precision and reliability are essential for detecting and measuring particles. Characterization helps ensure that the ASIC performs as expected within acceptable limits and meets the desired performance criteria. During the development of the ASIC, understanding the chip's performance characteristics enables engineers to fine-tune its design for better efficiency, reduced power consumption, or improved signal processing capabilities. Through characterization, it is possible to identify potential issues such as power consumption irregularities, temperature sensitivities, or timing violations to validate the final product's reliability and robustness.

Particle accelerators create challenging environments for the ASIC. Characterization assesses the ASIC's performance under varying conditions, such as temperature extremes or radiation exposure, to ensure the chip's reliability in such environments. Additionally, ASICs may exhibit slight variations from one another due to manufacturing differences. Characterization helps establish calibration factors or correction techniques to account for these differences.

This chapter will present the methodologies and techniques employed to evaluate the functionality of the H2GCROC ASIC, as presented in Chapter 4. During HGCAL operation, the chip will use two calibration setups : the Calibration configuration for in situ calibration and the Physics configuration for regular operation. This manuscript will evaluate the performance of these two configuration modes. It will evaluate charge measurement, timing characteristics, noise margins, spread between channels, power consumption, performance after radiation exposure, performance at different temperatures and calibration efficiency. The performance evaluation of the ASIC is vital for ensuring its reliability, optimizing its performance and achieving accurate and precise results in scientific experiments.

This thesis work began with the arrival of the second fabricated ASIC version at the laboratory. However, due to the chip's complexity, this dissertation will exclusively present the characterization of the third fabricated version, H2GCROCv3. It also explains the main improvements in H2GCROCv3 to its predecessor, H2GCROCv2, and mentions expected future enhancements in the final version, H2GCROCv3b.

5.2 Measurement Setup and Procedures

The chip's performance was characterized in the laboratory using two types of test benches, both controlled by an FPGA developed at CERN. These test benches communicate with the ASIC and read its response using Python scripts. Figure 5.1 shows the mezzanine board with one H2GCROCv3 connected to a PCB, while Figure 5.2 displays the socket board with one ASIC in place. The socket on the board allows for easy removal of the ASIC, enabling the interchange of ASICs and facilitating the testing of the entire production process using a robot.

Figures 5.1 and 5.2 showcase the ZYNQ/Hexacontroller card developed at CERN. This board is used to configure and read the ASIC's output. The ZYNQ is programmed with C code, enabling I^2C control and fast command execution for communication through Ethernet with the PC. Subsequently, Python scripts can activate the trigger signal to inject charge internally using a DAC within the chip or introduce external charges synchronized with the trigger. All configuration parameters are modifiable through slow control via the I^2C protocol.

For characterization, the ASIC was fabricated by two companies, NCAP and SERMA, using the same TSMC 130 nm technology. Different grounding types were explored during the chip fabrication, connecting digital and analog block power supplies in various ways. These variations

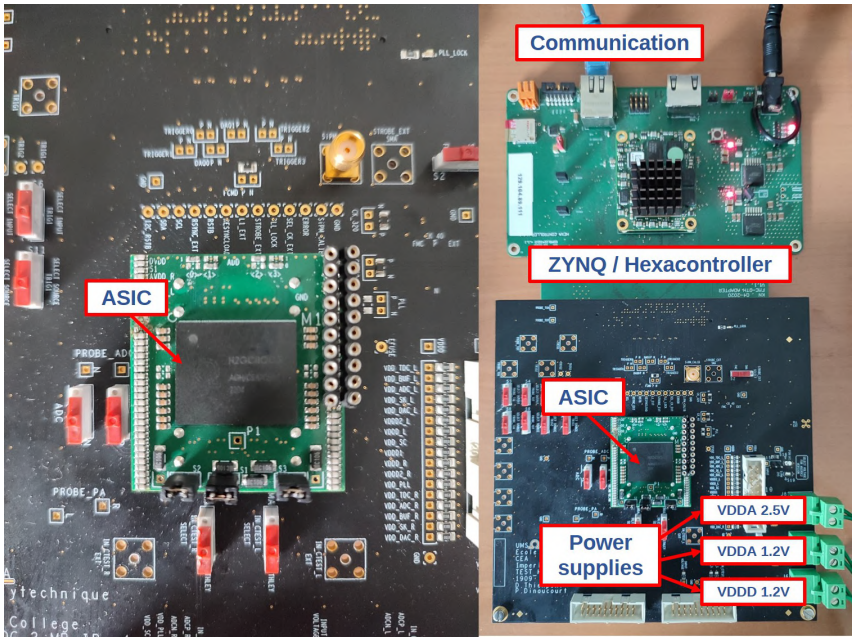

FIGURE 5.1 – *Mezzanine board for tests.*

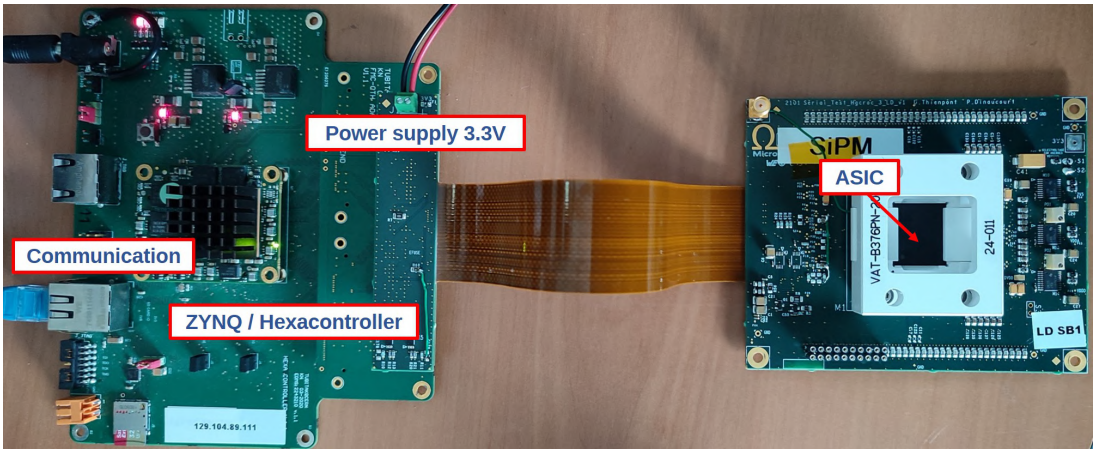

FIGURE 5.2 – *Socket board for tests.*

allowed for the selection of the ground configuration with the optimal balance between the performance and noise of the ASIC's analog and digital components. Most of the characterization results of the ASIC will be presented using the mezzanine board with the SERMA-fabricated version of the chip, as it exhibited the most favorable noise-performance characteristics. However, the socket board allows for easy interchange of the ASIC under test without requiring soldering. Consequently, the signal spread between chips was analyzed using this test bench.

The injection of signals into the ASIC was performed using three different methods :

— Internal injection using the internal DACs and capacitors of the chip.
— External injection using a signal generator and external capacitor to inject an input signal.
— Injection of photons sending a 405 nm laser signal to SiPM detectors.

5.2.1 Internal and External injection setup

Internal and external charge injection follow the same principle : creating a voltage step with a defined amplitude converted to charge using a capacitor. The injected charge is determined by multiplying the voltage amplitude by the capacitance. The voltage step can be generated in two ways : using the two internal 12-bit DACs of the chip or with an external signal generator. Figure 4.43 in Chapter 4 presented the different forms to inject into the channels for characterization. For external injection, using a smaller external capacitor is preferred over the 117 pF available in the ASIC to reduce noise from the injection capacitor.

Figure 5.3 illustrates the measured performance of the $calib\_dac$ that injects into the preamplifier. It exhibits an offset of 2.65 mV and demonstrates excellent linearity, with a maximum residual of 1.4 mV. The DAC's maximum voltage output aligns with the ASIC's bandgap voltage, set to 1.05 V for these measurements. These values, converted by the available capacitors, generate charge injections ranging from 0 to 500 fC and 0 to 8 pC for low and high-range injection, respectively.

In contrast, Figure 5.4 displays the performance of the $calib\_dac\_2V5$ used for injecting into the current conveyor. It has an offset of 18.9 mV and exhibits more non-linearities than the $calib\_dac$, particularly noticeable for higher voltages. The DAC's maximum voltage, which depends on the bandgap value, was measured at 1.67 V, lower than the anticipated 2.5 V. Therefore, the current conveyor DAC for the chip's 3b version will be corrected to enhance the maximum voltage and reduce the residuals. The available charge injections from the internal DAC $calib\_dac\_2V5$ range from 0 to 5 pC using only the 3 pF capacitor of the selected channel, or 0 to 200 pC using all the 3 pF capacitors of one half of the ASIC connected in parallel, producing a total capacitance of 117 pF.

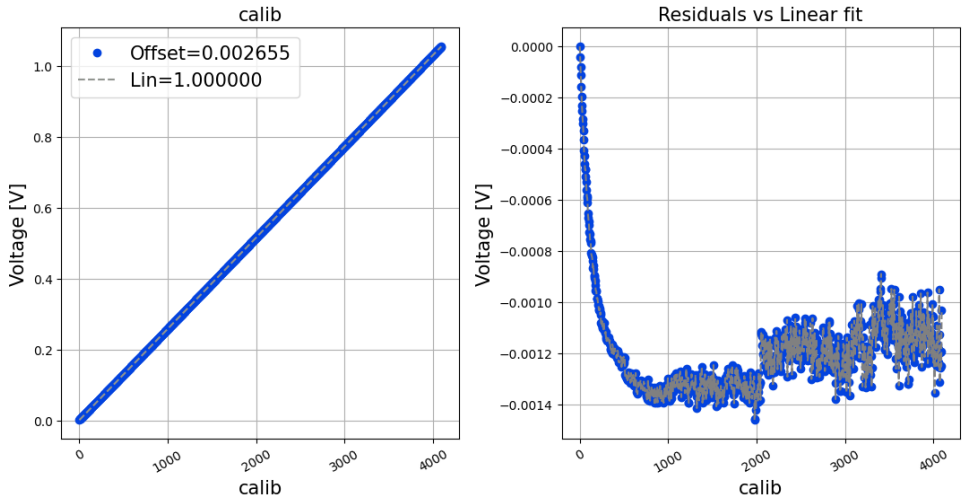

FIGURE 5.3 – *1.2V DAC response for calibration injection into the preamplifier.*

A 'Tektronix AFG3102' (Figure 5.5) voltage generator was employed for external injection. The trigger alignment can be accomplished through two methods. The $SiPMcalib$ output signal from the chip generates a trigger signal on the generator to transmit the voltage pulse through the capacitor connected to one of the chip's channels. The level amplitude of the $SiPMcalib$ signal is 1.2 V, while the voltage generator's input trigger requires a 2.5 V level. Consequently, additional amplification is necessary to convert the 1.2 V signal to 2.5 V before sending the trigger to the voltage generator. Figure 5.6 portrays the external injection diagram using the ASIC's SiPM calib output signal.

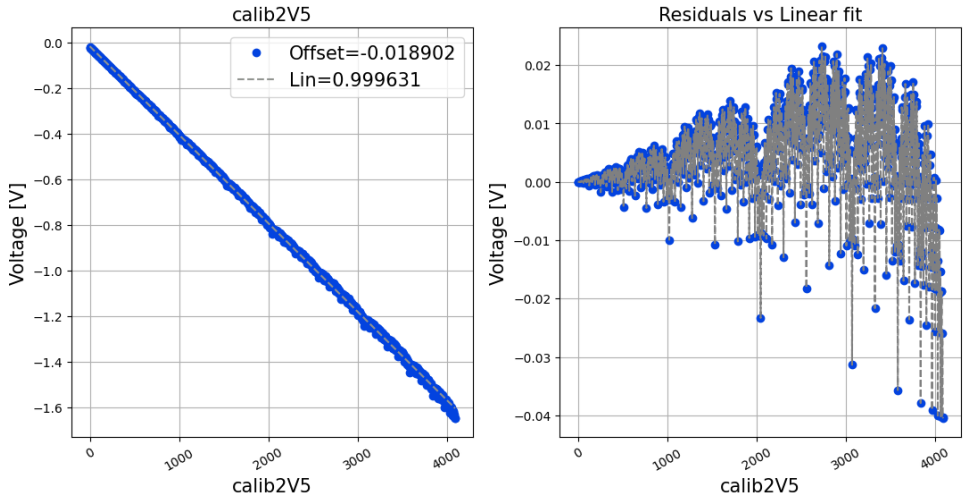

FIGURE 5.4 – *2.5 V DAC response for calibration injection into the current conveyor.*

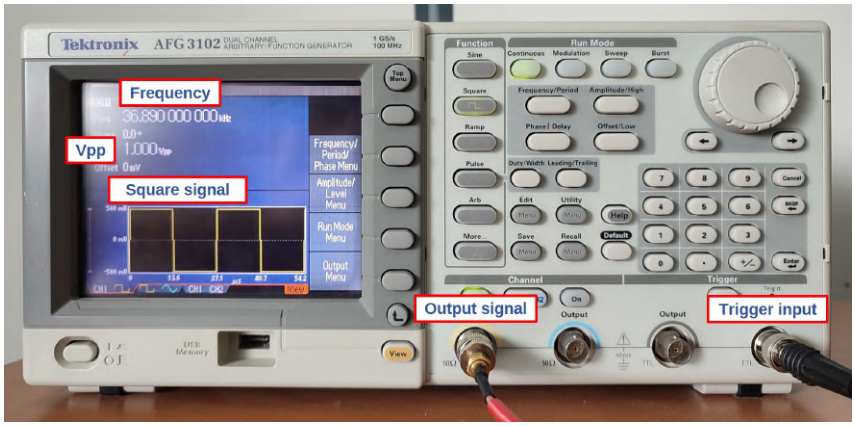

FIGURE 5.5 – *Tektronic voltage generator.*

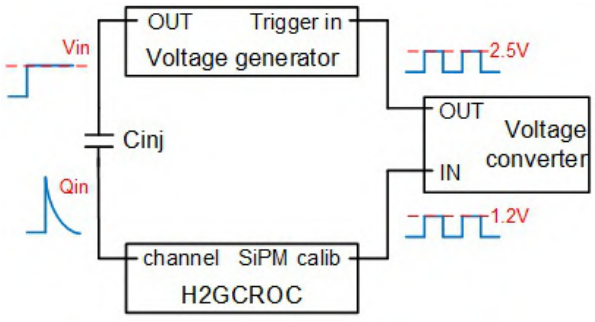

FIGURE 5.6 – *Tektronic diagram for external injection.*

The second option is to send an external trigger signal first to the voltage generator's input trigger and then to the external L1A input of the ASIC. In both trigger alignment methods, finding the correct delay and selecting the proper Bunch Crossing (BX) to identify the signal entering the channel is necessary. The voltage generator chosen can generate pulses up to $V_{inj} = 10V$ peak to peak. Using an external capacitor C_{inj} connected in series allows the conversion of the voltage step into charge injection. Employing a 33 pF capacitor allows for charge injection within the expected charge dynamic range from 0 to 330 pC.

5.2.2 SiPM under test

For preliminary tests, a detector capacitance connected from the input to the ground was used to investigate the impact of the detector capacitance on the ASIC inputs. The capacitor value was chosen to simulate the capacitance of the SiPM. Therefore, the SiPM model's capacitance value (C_G in the SiPM model of Figure 3.25) produces an approximate equivalent signal.

However, as discussed in Section 4.4.5, it was demonstrated that the number of pixels must be considered, introducing additional capacitance in parallel. The sum of these two capacitances in parallel will be referred to as the equivalent detector capacitance, C_{det}. Since only a limited number of SiPMs were available in the laboratory, the C_{det} value was used for several tests. This approach was more practical than individually connecting a SiPM to each channel, allowing simultaneous injections in multiple channels.

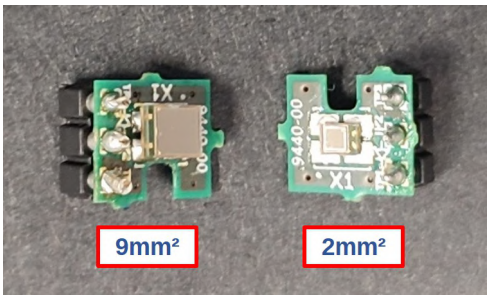

FIGURE 5.7 – *PCBs with SiPM under test.*

For the remaining tests, two SiPM detectors selected were utilized. Table 4.6 outlines the primary characteristics of the two SiPMs used (Figure 5.7) for the ASIC characterization. Both types of SiPMs were tested with the maximum over-voltage ($OV = 6V$) allowed by the SiPM. Due to the higher noise of the 9mm² SiPM, the 6V over-voltage was necessary to enhance the signal-to-noise ratio and observe the single-photon spectrum.

5.2.3 Photon injection

The injection of photons in the laboratory was conducted using a laser signal and a SiPM connected to one of the ASIC channels. The configuration from [52] was taken as a reference for photon injection to a SiPM and the H2GCROC ASIC. The setup consists of a high-speed laser that can be externally triggered, optical attenuation using a diaphragm, diffusers and absorptive lenses, and a SiPM sensor mounted in a structure that offers precise 3-axis manipulation. The SiPM was connected to the structure in Figure 5.8. Figure 5.9 displays the detector card positioned within the structure for precise manipulation.

The selected laser was the PILAS Picosecond Pulsed diode PiL040-FS [70], configured with a 405 nm wavelength. This laser aligns with the application's requirements due to its ultra-low timing jitter (< 3 ps rms), a pulse width of less than 45 ps, a maximum repetition rate of 40 MHz and a beam size of 2.5 x 1.2 mm.

Figure 5.10 illustrates the laser pulse measurement configuration. Absorptive lenses attenuate light transmission, while the diffuser disperses the light, directing only a minimal portion to the center. The diaphragm eliminates diffused light and reduces the beam size to its smallest dimensions. Precise alignment of the SiPM is essential for proper beam reception. The system is enclosed within a black box to shield against ambient light and reflections. Figure 5.11 displays the constructed injection setup using components from Thorlabs.

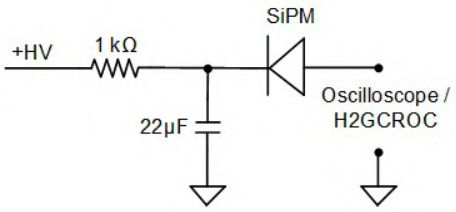

FIGURE 5.8 – *Diagram of the Detector card for SiPM reading.*

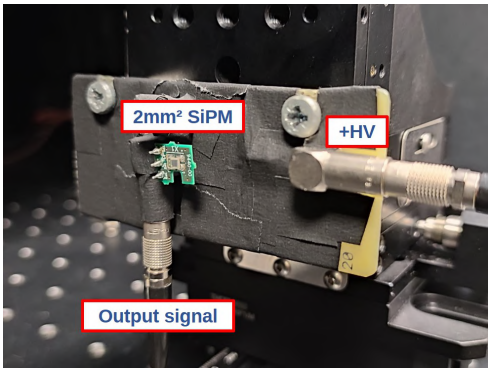

FIGURE 5.9 – *Detector card for SiPM reading with interchangeable SiPM.*

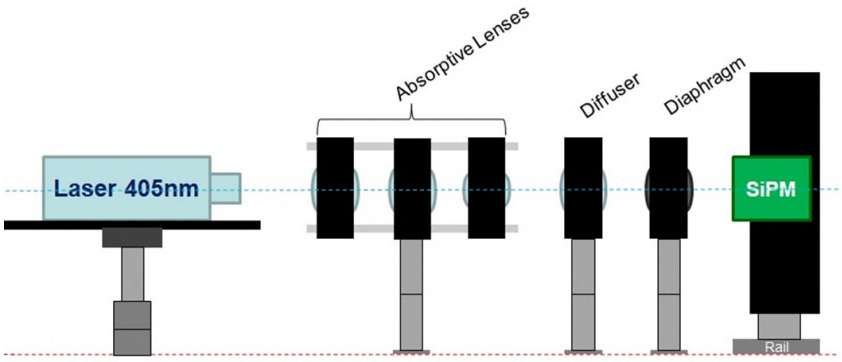

FIGURE 5.10 – *Laser injection setup diagram.*

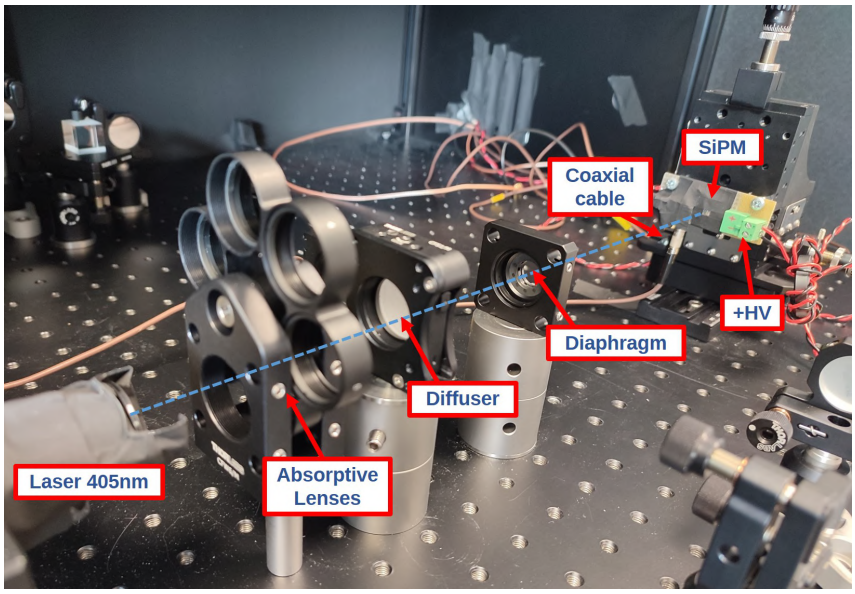

FIGURE 5.11 – *Laser injection setup.*

In this setup, the signal output from the SiPM detector can be connected to one of the ASIC channels or an oscilloscope via a coaxial cable. The objective is to attenuate the light and achieve light injection, ranging from 0 to a few photons on the oscilloscope, while maintaining low noise to ensure clear photon separation. Figure 5.12 demonstrates the oscilloscope

responses to photon injections from the 2 mm² and 9 mm² SiPMs, respectively. Due to the relatively low amplitude of the detector's output signal, an additional negative gain of 5 was applied from the SiPM output to the oscilloscope measurement. Both oscilloscope figures display the SiPMs' negative voltage output, with green lines indicating photon events. The event counts are highlighted in yellow, illustrating the achieved photon separation. The 2 mm² SiPM exhibits photon injections ranging from 0 to 6, while the 9 mm² SiPM demonstrates injections of 0 to 4 photons with an amplitude approximately half that of the 2 mm² SiPM. Increased noise in the 9mm² SiPM can be attributed to the high detector capacitance and number of pixels.

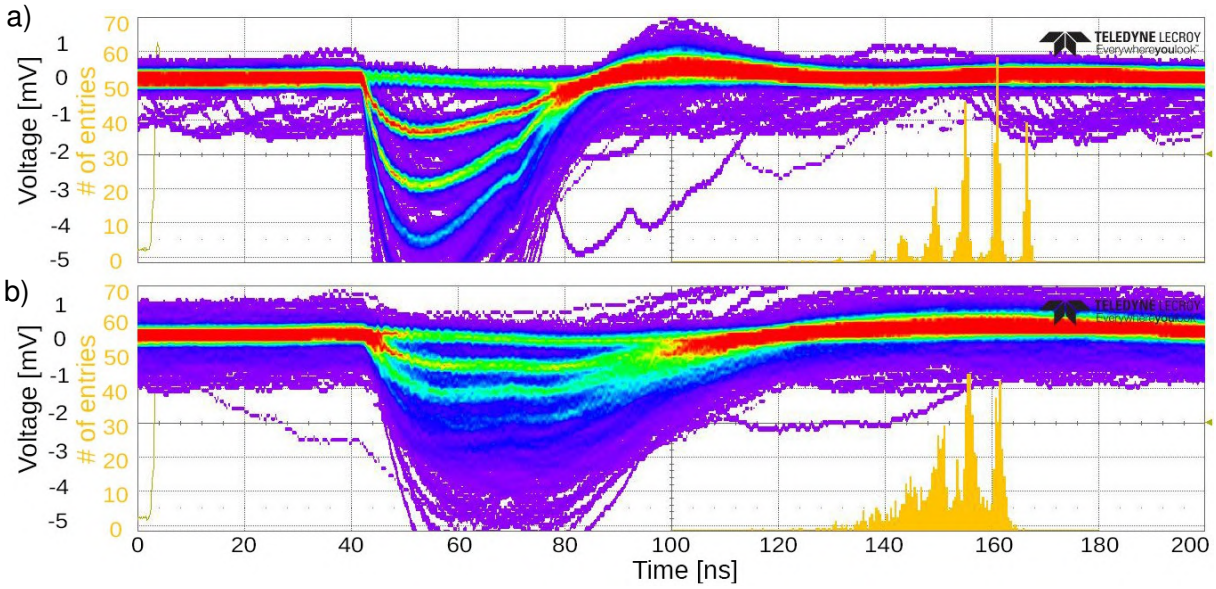

FIGURE 5.12 – *SiPM response to injecting 0 to 5 photons using an oscilloscope and an extra 20 dB gain. a) 2 mm² SiPM. b) 9 mm² SiPM.*

Three main effects are observed : a larger SiPM area decreases the falling time of the signal, increases noise and reduces the amplitude, resulting in decreased gain and diminished photon separation during single-photon spectrum measurements. Once the injection parameters are set, the coaxial cable is disconnected from the oscilloscope and connected to one channel of the ASIC for signal injection, maintaining the same photon injection configuration.

5.3 Methodologies for calibration of the ASIC

One of the key features of the H2GCROC ASIC is its versatility in adapting to diverse scenarios. The ASIC design incorporates configurable parameters to address various aspects, including setting DC levels, mitigating radiation-induced damage, compensating for dispersion from SiPM detectors, minimizing variations between channels, establishing the minimum threshold for timing measurements, and adjusting the system's gain to match the signal from the minimum ionizing particle. Moreover, every block of the ASIC can be configured to maintain consistent performance across channels, even in the presence of potential discrepancies resulting from the chip's manufacturer and the selected technology.

5.3.1 Gain configuration of the ASIC

The system's gain can be globally configured within the chip using the current conveyor (CC) attenuator and the preamplifier's feedback resistance (R_f) and capacitors (C_f, C_{f_comp})

(see Section 4.5.4). The current conveyor attenuates the detector-generated current proportional to the charge with minimal alteration to rise/fall times. Figure 5.13 demonstrates the ADC response over time for a 1 pC injection with a gain variation on the current conveyor, where attenuation can be set from 0 to 0.325. The linearity in current conveyor measurements exhibits less than 1% error but shows higher rms noise in ADC measurements when less attenuation is applied.

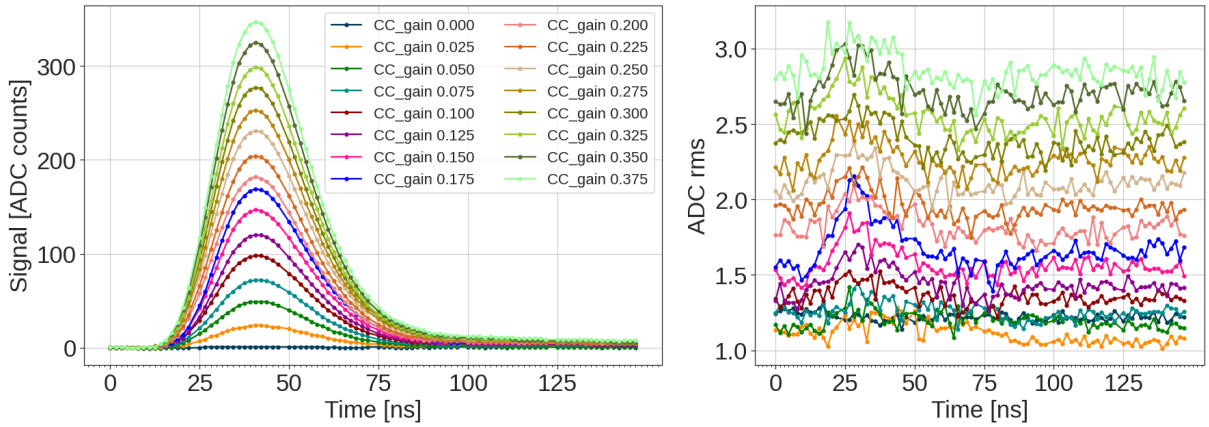

FIGURE 5.13 – *ADC response to 1 pC charge injection and its ADC rms, scanning the different attenuation values of* CC_gain.

The preamplifier (PA) gain can be configured by selecting the feedback resistor and feedback capacitors. The preamplifier gain enhances the signal's amplification and controls its duration. Default parameters use $R_f = 25\ k\Omega$ and $C_{f\_total} = 1\ pF$ resulting in $R \times C = 25\ ns$ and a slow output signal. The large capacitance of SiPM detectors produces slow rising and falling times that cannot be measured efficiently with the default configuration. Then, to accelerate measurements, signal duration shaping can be achieved by configuring the $R \times C$ value. Figure 5.14 illustrates the variations in preamplifier gain while maintaining $R \times C = 5\ ns$ with the same current conveyor attenuation. It is noticeable that higher gains introduce instabilities and increase the noise, particularly when the parameter R_f equals 12 (16.67 $k\Omega$) or for larger feedback resistors. Increasing the $R \times C$ reduces the instabilities but at the cost of slowing down the measurements. Figure 5.15 presents the variations in preamplifier gain with $R \times C = 10\ ns$ and the same current conveyor attenuation. The reduced instability led to selecting $R \times C = 10\ ns$ as the minimum viable value for stable performance.

This manuscript presents two configurations for HGCAL. The 'Calibration' configuration is designed for measuring the single-photon spectrum (SPS) of the SiPM for in-situ calibration. This configuration requires a high gain with a good signal-to-noise ratio to detect photon separations and read the gain of the SiPM connected to each channel. The 'Physics' configuration measures the required dynamic charge range (ranging from 160 fC to 320 pC) for regular HGCAL operation with minimal noise. It aims for optimal linearity in charge measurements and the highest achievable time measurement resolution.

Figure 5.16 displays the performance of a single channel for both proposed configurations with a 2.47 pC charge injection. Gain per ADC and rms noise vary with SiPM characteristics. When operating HGCAL, creating a set of these two configuration files may be necessary for each different SiPM utilized.

The only difference between these configurations lies in the front-end gain settings. A 0.1 attenuation is applied to the current conveyor gain in the Physics configuration. On the contrary, the Calibration configuration has less attenuation on the current conveyor gain (0.3) to increase

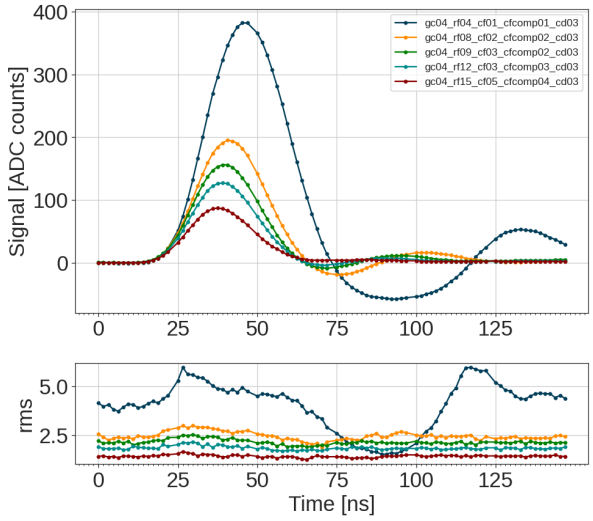

FIGURE 5.14 – *Preamplifier gain scan of R_f and C_{f_total} maintaining a $R \times C$ = 5 ns.*

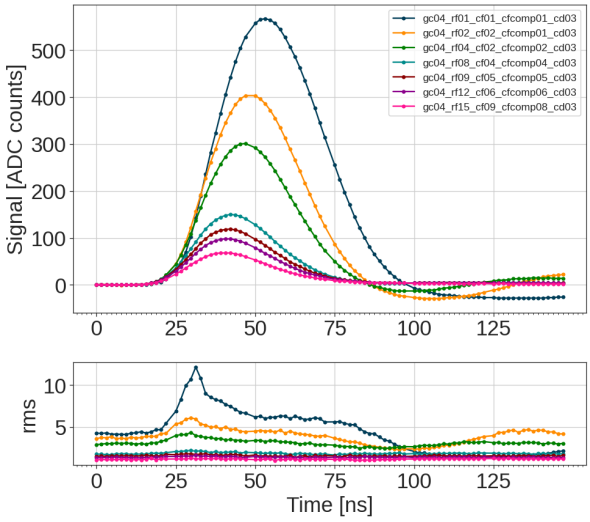

FIGURE 5.15 – *Preamplifier gain scan of R_f and C_{f_total} maintaining a $R \times C$ = 10 ns.*

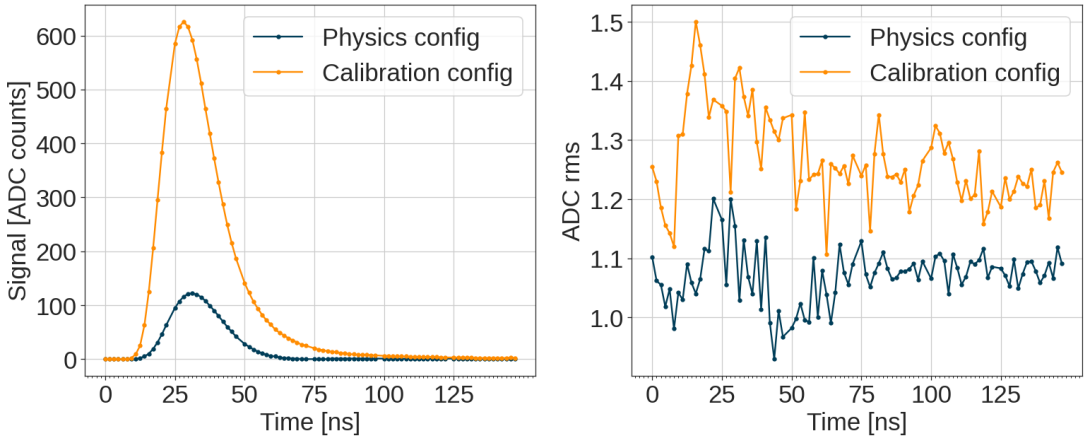

FIGURE 5.16 – *ADC response (left) and ADC rms noise (right) for calibration and physics modes to 2.47 pC charge injection to one channel of H2GCROC.*

the gain while maintaining the same feedback resistance on the preamplifier. The calibration configuration reduces the feedback capacitance to increment the gain and speed up the output response. Table 4.5 provides key parameter configurations for the two proposed configurations.

5.3.2 Pedestal adjustment

Once the system's gain is configured, the initial step in ASIC calibration involves setting the pedestal value for each channel to the same ADC level, minimizing noise and ensuring a lower variation between channels.

The process consists of reading each channel's pedestal value and using the $dacb$ DAC of each channel to adjust the pedestals to fall within the same ADC's selected range. Subsequently, a scan of the $trim\_inv$ parameter allows for selecting the optimal value per channel to mitigate channel dispersion. Then, the global voltages for the inverter and non-inverter shapers ($vref\_inv$ and $vref\_noinv$) are calibrated to achieve a 1V range at the ADC input. Finally, a second trimming of the channels is performed using the $trim\_inv$ parameter.

Figure 5.17 illustrates the pedestal readings before and after calibration. During these measurements, two channels in the second half had a different external input capacitance added. These channels exhibit increased noise above the 1 ADC rms, as shown in Figure 5.17 b). Therefore, pedestal adjustment can be performed across the entire chip, even if it has different SiPM detectors connected to its channels.

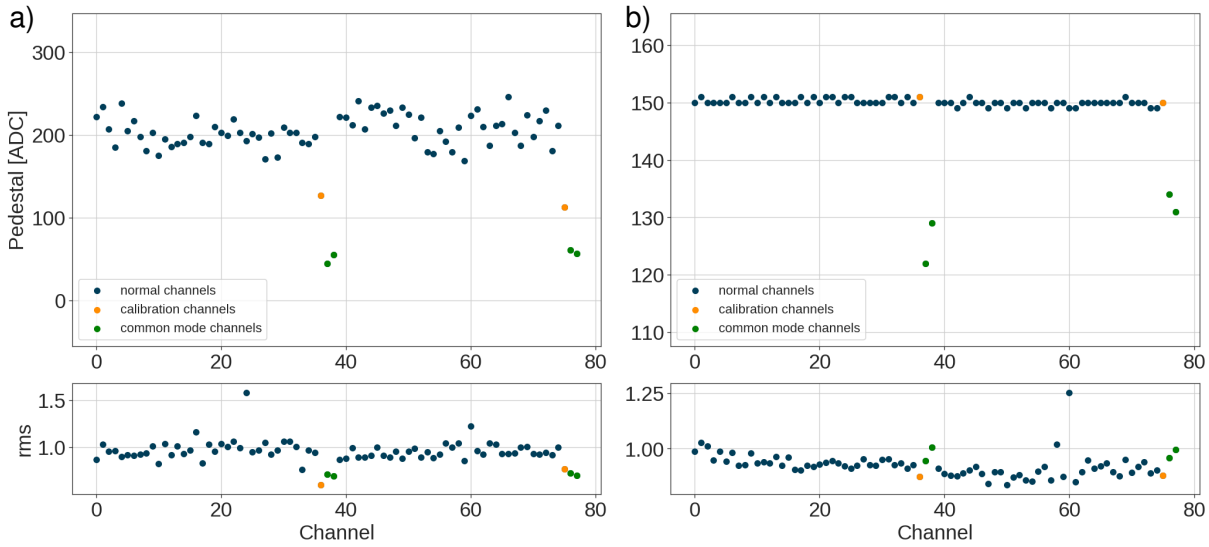

FIGURE 5.17 – *Pedestal trimming. a) Pedestal reading of each channel with its ADC rms noise before pedestal calibration. b) Pedestal reading of each channel with its ADC rms noise after pedestal calibration.*

5.3.3 Time threshold calibration

The thresholds of the two discriminators can be configured per half and adjusted channel-wise to minimize dispersion among channels. The time-of-arrival (TOA) threshold should be set just above the pedestal noise level to ensure accurate data acquisition timing for most events. The time-over-threshold (TOT) threshold needs to be configured below the saturation point of the preamplifier (PA) to cover the full dynamic range of measurements. The process of establishing the threshold voltages is similar for both discriminators.

First, a small charge is internally injected into each channel to calibrate the TOA threshold. The TOA efficiency, defined as the ratio of TOA triggers to the number of injection events, is computed for varying threshold voltages. Subsequently, the minimum TOA threshold that achieves a TOA efficiency of one for all channels is selected. Since the TOA is expected to trigger at different points for each channel, a channel-wise scan of the $trim\_toa$ parameter is performed to mitigate variations. Once again, the minimum value producing a TOA efficiency of one is chosen. This process aligns the minimum charge with TOA triggers across all channels. Finally, a final TOA threshold scan is performed without any injection. This scan will produce TOA data when the threshold is at the noise level, selecting the minimal TOA threshold without any TOA data triggered from the noise for each channel in any configuration phase.

For example, Figure 5.18 a) presents a TOA threshold scan with a small charge injection for one channel. The smallest Toa_vref configuration with TOA efficiency equal to 1 will be selected. After choosing the first TOA threshold, Figure 5.18 b) shows the $trim\_toa$ scan performed for every channel. Again, the smallest value to generate a 100% TOA efficiency is selected. Finally, Figure 5.18 c) presents a second TOA threshold scan. No charge injection exists on that

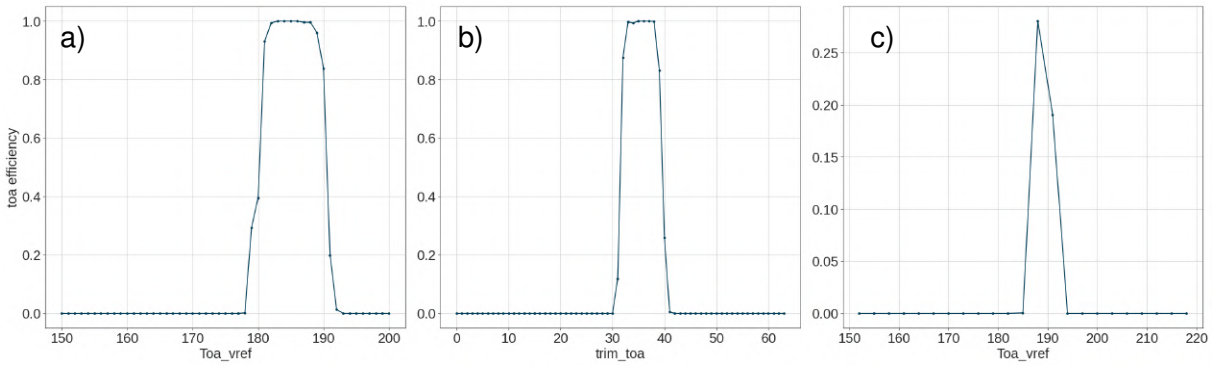

FIGURE 5.18 – *TOA calibration process for one channel. a) First scan of TOA threshold with a small charge injection. b)* $trim\_toa$ *scan to adjust the dispersion per channel. c) Second scan of TOA threshold with TOA triggers from the noise.*

step to see TOA triggers from the noise level. Here, the TOA threshold will be placed just above the value that generates noise-related TOA triggers. Figure 5.19 presents the TOA efficiency of the channels of one half before calibration. In contrast, Figure 5.20 presents the TOA efficiency of the channels after calibration, showing a minimal charge injection with time information of around 350 fC for all channels.

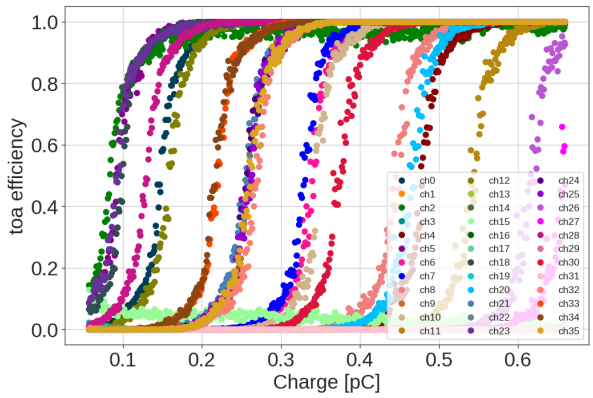

FIGURE 5.19 – *TOA efficiency response of the channels of one ASIC half to a charge injection scan. The ASIC was configured with the physics mode.*

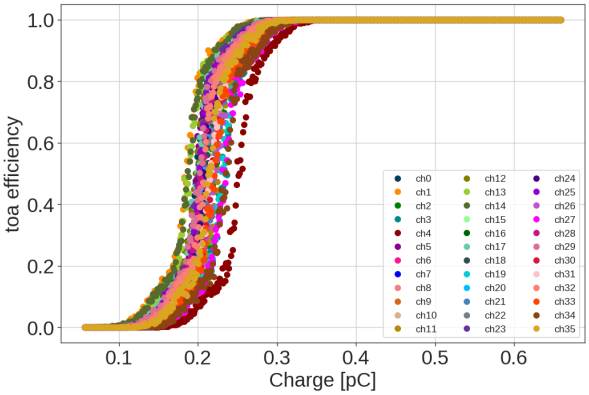

FIGURE 5.20 – *TOA efficiency response of the channels of one ASIC half to a charge injection scan. The ASIC was configured with the physics mode and trimming between channels was applied.*

5.3.4 Single photon counting

The single-photon counting technique is commonly used to characterize SiPM detectors. It measures the detector's response to a few photons with sufficient resolution to determine the separation of photon peaks equal to the SiPM's gain. Before the normal operation of HGCAL, the gain of each detector will be measured in situ using the single-photon spectrum (SPS), and an LED will be available on the board to perform photon injection.

To calibrate the SiPM effectively, the ASIC must be configured to increase the signal-to-noise ratio, allowing for accurate measurements of the photon peaks. The characteristics of

the SiPMs must be considered to find the correct configuration. Using the model from Figure 3.25, we can identify the parasitic capacitances present in a SiPM and calculate an equivalent detector capacitance for each SiPM under test. This equivalent detector capacitance (C_{det}) is helpful for faster testing using the internal injection feature of the ASIC. Table 4.7 presents the equivalent detector capacitances for each area of SiPM used in HGCAL.

By connecting these capacitors to different channels of the ASIC, we can analyze the capacitance's influence on charge measurements. Figure 5.21 illustrates the ADC response with different C_{det}. Two main effects can be observed : larger capacitances increase the rising and falling times of the signal and increase the RMS noise. Additionally, larger capacitances reduce the ADC's amplitude, which results in a lower ADC-to-charge gain and separation of photons during SPS measurements. These results align with similar effects in the oscilloscope measurements presented in Figure 5.12, using two detectors with different capacitances.

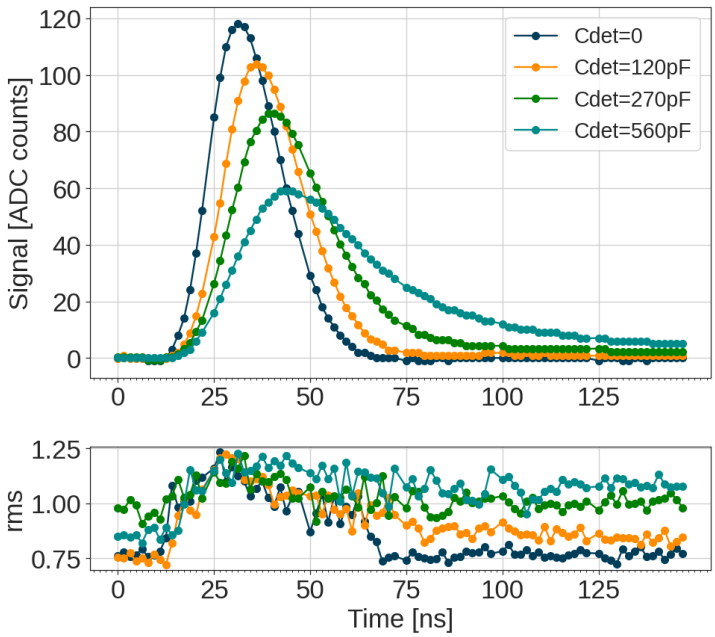

FIGURE 5.21 – *ADC response through time for a 2.5 pC internal injection using different detector capacitances C_{det} and the physics configuration mode.*

The setup explained in Section 5.2.3 allows for injecting a few photons into a single channel of the ASIC. The Hamamatsu SiPM S14160-1315PS, with an effective photosensitive area of 1.3 x 1.3 mm², was employed to detect photons from the 405 nm fast laser and send the charge response into the ASIC. The single-photon spectrum was recorded (Figure 5.22) using the calibration configuration of the H2GCROC ASIC. The measurement demonstrates the successful separation of photons with the optimal ADC delay setting. However, if we want to measure the SPS from the 9 mm² SiPM, the configuration used for the 2 mm² SiPM does not provide enough gain. The difference in capacitance is not negligible and has led to the need for specific configuration files for SiPM with different areas.

The oscilloscope measurement of the 9 mm² SiPM (Figure 5.12 b)) shows an increase in noise. This increment is evident from the histogram of voltage entries, which indicates that the noise affects the separation of photon peaks. Therefore, the configured gain was adjusted to compensate for the gain decrease in the 9 mm² SiPM. The changes included reducing the attenuation of the current conveyor from 0.3 for the 2 mm² SiPM to the minimum possible (0.375) for the 9 mm² SiPM and halving the feedback capacitance of the preamplifier to speed

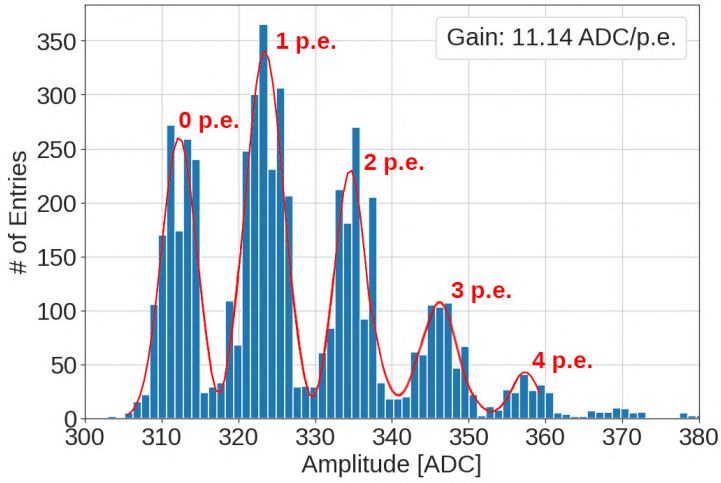

FIGURE 5.22 – *H2GCROCv3 SPS response of 2 mm² SiPM using injection with laser.*

up the rising and falling times of the 9 mm² SiPM's response. Table 5.1 provides the different gain configurations for the two SiPM detectors.

Parameter	**Calibration configuration**	
	for 2 mm² SiPM	for 9 mm² SiPM
Current conveyor attenuation (CC_gain)	0.3	0.375
Feedback Resistor (R_f)	16.6 $k\Omega$	16.6 $k\Omega$
Feedback Capacitor (C_f)	300 fF	150 fF
Feedback Capacitor complement (C_{f_comp})	300 fF	150 fF
Preamplifier input capacitor (C_d)	0	0

TABLE 5.1 – *Gain ASIC setup differences for the Calibration configuration of different areas of SiPM.*

This configuration resulted in similar gains for both SiPMs. Figure 5.23 presents the ADC response to the two proposed calibration configurations to a 2.5 pC injection. We can observe how the configuration for the 9 mm² SiPM has a lower signal-to-noise ratio (SNR) than the 2 mm² SiPM configuration. However, the increased gain permits clarifying the separation of photon peaks.

The Hamamatsu 9 mm² pre-series of HGCAL was employed to detect the photons from the 405 nm fast laser and send the charge response into the ASIC. The SPS was recorded (Figure 5.24) using the dedicated calibration configuration of the H2GCROC ASIC. The measurement demonstrates that the gain increment successfully separates photons with the optimal ADC delay setting.

However, the increased noise introduced another effect on the ADC response. Figure 5.25 shows the first SPS measured from the 9 mm² SiPM. The noise obstructs the separation of single photon peaks. Therefore, the 9 mm² SPS was measured with three datasets configured with different pedestal settings on the ASIC. Figure 5.24 presents the aligned data minus the pedestal from the three data sets, improving the separation of photon peaks. This technique is not time-consuming and will be feasible during the in-situ calibration of HGCAL.

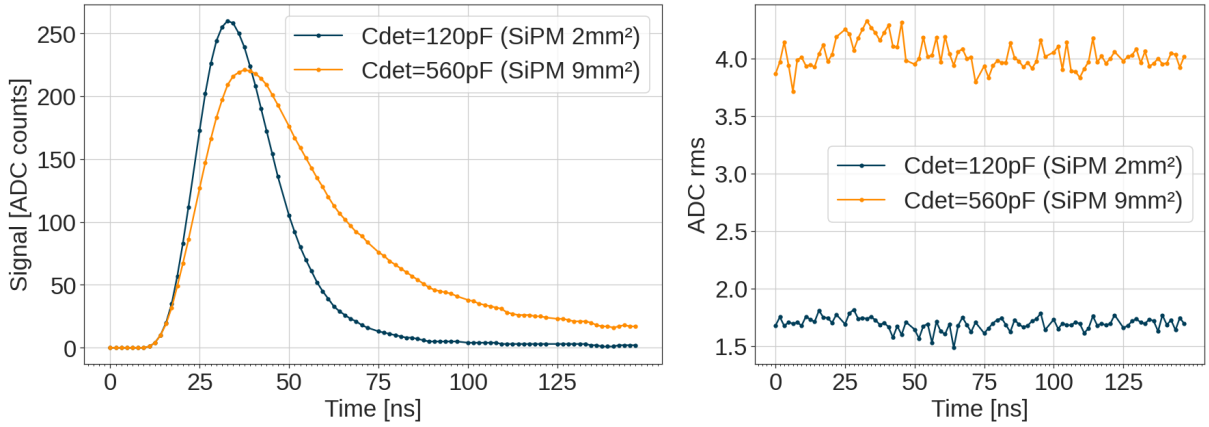

FIGURE 5.23 – *ADC response through time for a 2.5 pC internal injection, using the dedicated Calibration mode for a 2 mm² and 9 mm² SiPMs.*

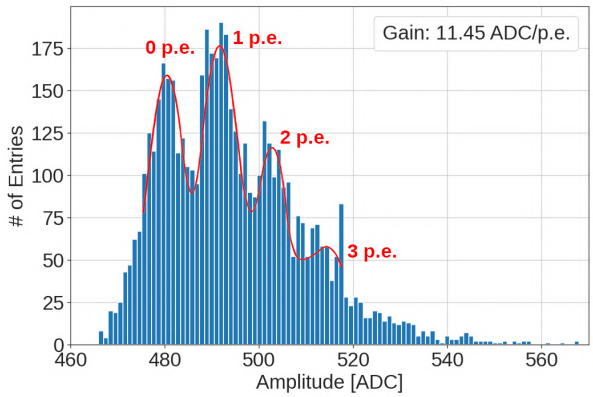

FIGURE 5.24 – *H2GCROCv3 SPS response of 9 mm² SiPM using injection with a laser and three aligned datasets configured with a different ADC pedestal.*

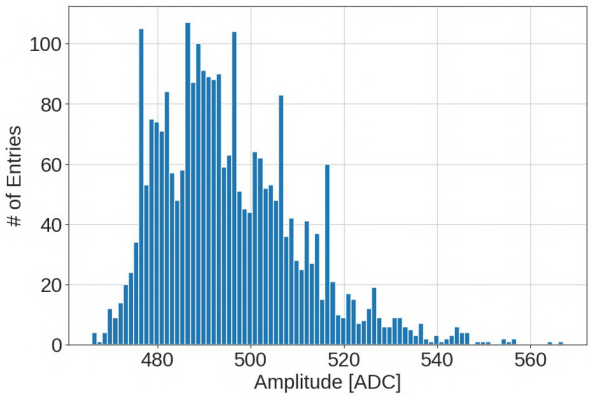

FIGURE 5.25 – *H2GCROCv3 SPS response of 9 mm² SiPM using injection with a laser before correction from datasets with different ADC pedestals.*

5.3.5 SiPM gain calibration

Once the chip is fully calibrated, variations in the signal from the SiPMs can occur due to differences in high voltage ($+HV$) levels of the detectors, disparities in the SiPM manufacturing process, changes in pedestal levels on the ASIC, or connections on the PCB. As explained in Section 4.3.1, these variations can be compensated for using a 6-bit DAC in the current conveyor, which injects the V_{dac} voltage to adjust the $+HV$ voltage seen by the SiPM. Figure 4.53 illustrates that this compensation can be achieved within a range of ±750 mV.

The calibration of SiPM gain begins with single-photon injections into all channels using the calibration configuration of the ASIC and applying a high overvoltage to the detectors. This injection allows for observing each sensor's single-photon spectrum (SPS) information and calculating ADC/p.e. gain. Subsequently, a V_{dac} scan is conducted in every channel to determine the voltage value that results in the same ADC/p.e. gain across all channels. Figure 5.26 demonstrates the differences in SPS across the minimum, midpoint and maximum values of V_{dac} voltages, highlighting the ASIC's capability to configure consistent SiPM gains across all channels. The available voltage range can significantly impact gain, leading to variations ranging from 4 $ADC/p.e.$ to 11 $ADC/p.e.$ for the 2 mm² SiPM SPS measurements, for example.

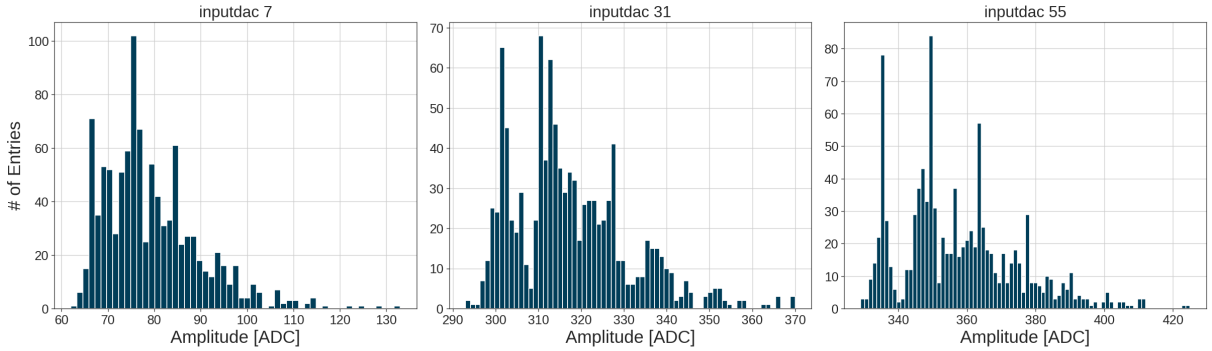

FIGURE 5.26 – *SPS for V_{dac} scan for SiPM.*

The SPS measurements for each channel will utilize the maximum overvoltage allowed by the SiPM to enhance photon separation during the measurements. The SiPM's overvoltage significantly impacts the SiPM gain. Therefore, a precise SiPM characterization is necessary to extrapolate from the maximum overvoltage used for calibration to the selected overvoltage in the physics configuration to reduce system noise. For instance, Figure 5.27 illustrates variations in SiPM gain from overvoltage of 4V to the maximum overvoltage of 6V, which is necessary to distinguish between photons in SPS measurements for SiPM detectors with high capacitance. The $ADC/p.e.$ gain for different overvoltage values, using the 2 mm² SiPM, ranges from approximately 3 to 9 for the different overvoltage configurations with the same V_{dac} setting.

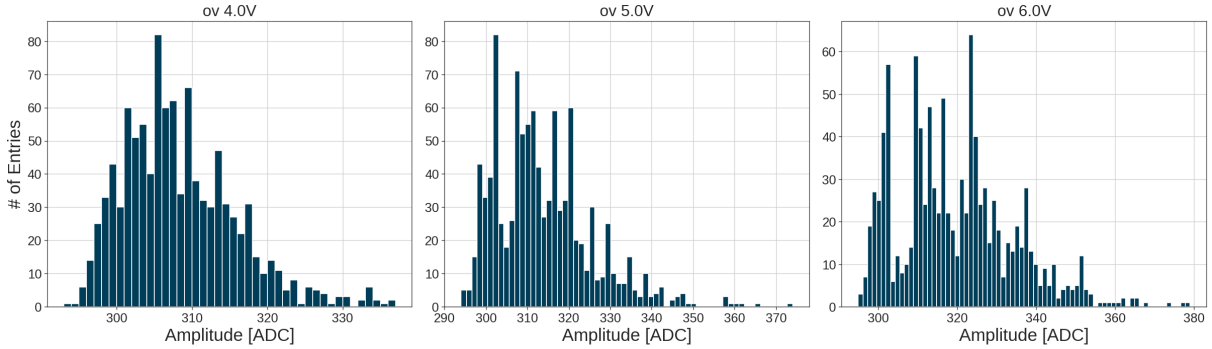

FIGURE 5.27 – *SPS for overvoltage scan of SiPM.*

5.3.6 TDC calibration

The TDC of the ASIC can be calibrated in three steps, as detailed in section 4.3.6. The TDC's performance is displayed in Figures 5.28 and 5.29, illustrating integral non-linearities (INL) and timing resolution of the TDC. Calibrating this block externally before calibrating time discriminators and channel trimming is essential. Figure 5.29 demonstrates an initial timing resolution of 35 ps with a variation range around $\pm$5 ps that becomes smaller than 20 ps after calibration.

5.4 Charge and time measurement performance

The ASIC utilizes the Physics configuration to measure charges ranging from 160 fC to 320 pC. The preamplifier's output is connected to a shaper linked to an ADC for low-range

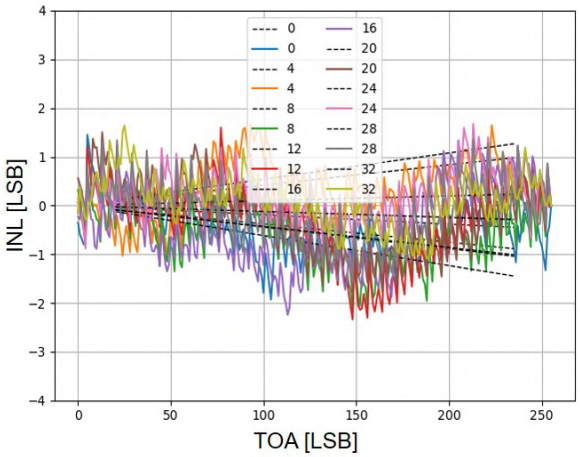

FIGURE 5.28 – *INL of TOA TDC for different channels after calibration.*

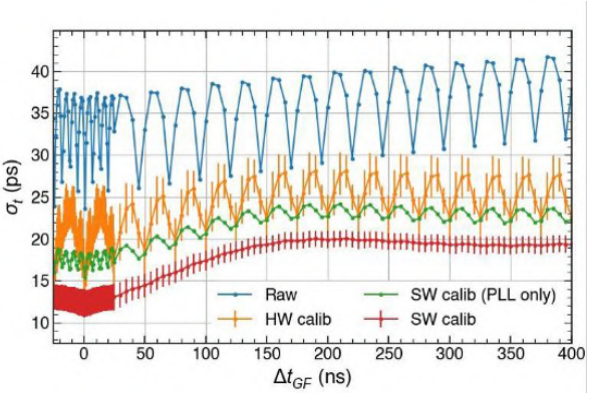

FIGURE 5.29 – *Resolution of TDC before and after calibration.*

charge measurements. The same output from the preamplifier is directed to a discriminator connected to a TDC to capture the remaining portion of the charge range. The ADC is calibrated to accurately read charges up to the point just before preamplifier saturation occurs. Once saturation is reached, the time-over-threshold (TOT) technique measures signal duration during saturation. A second discriminator, linked to a dedicated preamplifier output, records time-of-arrival (TOA) data of charge injections. The TOA threshold is kept as low as possible to capture timing information across most measurements.

Given that the new CMS hadron calorimeter will utilize SiPMs of varying sizes, it is crucial to establish configurations that can accommodate the injection range while considering differences in signal shape, rise time, decay time and phase selection on the signal peak. Additionally, configurations with higher noise levels or detectors with larger capacitance impact the minimum time threshold setting available for configuration.

5.4.1 ADC performance for charge measurement

The front-end ADC operates at 40 MHz, processing both the positive and negative outputs of the shaper to convert the analog signal into a value corresponding to the charge measured by the SiPM. The ADC phase can be configured with 4 bits. Initially, the internal charge injection is used to identify the correct phase and bunch crossing (BX) that measures the signal's peak. Figure 5.30 illustrates a 5 pC injection measurement in one channel, providing data for 6 BXs across all 16 possible phases. Equation 5.1 represents the equation used to fit the ADC output shape. The BXs and phase can be translated into time, considering a sampling time of 25 ns divided by the 16 phases. Once the peak phase and BX are identified, the ASIC is configured to consistently read the same point upon receiving a trigger signal.

$$f(t) = A_0 e^{-at}\left[e^{-ct}\left(\frac{t^3}{c} - \frac{3t^2}{c^2} + \frac{6t}{c^3} - \frac{6}{c^4}\right) + \frac{6}{c^4}\right], \qquad a = \frac{1}{\tau_p}, \qquad c = \frac{1}{\tau_p} - \frac{1}{\tau_s} \tag{5.1}$$

High linearity is crucial for the ADC to accurately measure the signal's peak and ensure precise charge measurements. Figure 5.31 presents the ADC peak output for different charges injected into the input channel using the chip's internal injection. The output shows a linearity of 99.92% calculated with a linear fit. However, the capacitance of the detector connected to

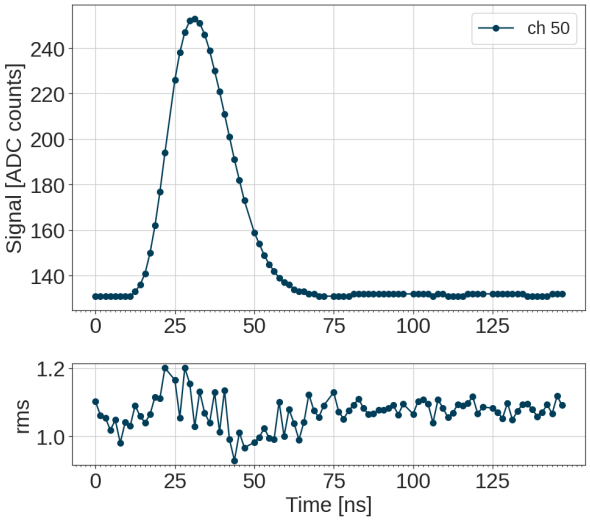

FIGURE 5.30 – *ADC response through time for a 2.5 pC internal injection and its rms values.*

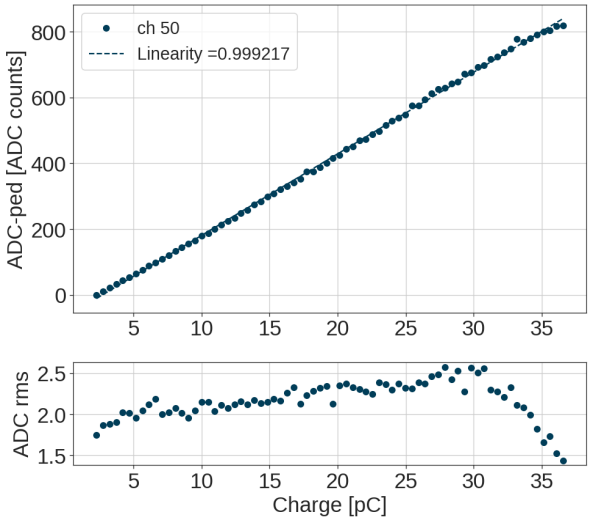

FIGURE 5.31 – *ADC peak value minus pedestal for a charge injection scan using the Physics configuration.*

the channel influences the shape of the ADC output response. Therefore, the slope of the ADC varies with different detector capacitances. Figure 5.32 shows the difference in ADC gain for the capacitors that correspond to the different SiPM sizes of HGCAL. The measured charge ranges were 22.1 pC for the 2 mm² SiPM, 28 pC for the 4 mm² SiPM and 39.9 pC for the 9 mm² SiPM. The rms noise measured from the ADC corresponds to 26 fC, 33 fC and 47 fC for the different SiPM sizes, respectively.

5.33

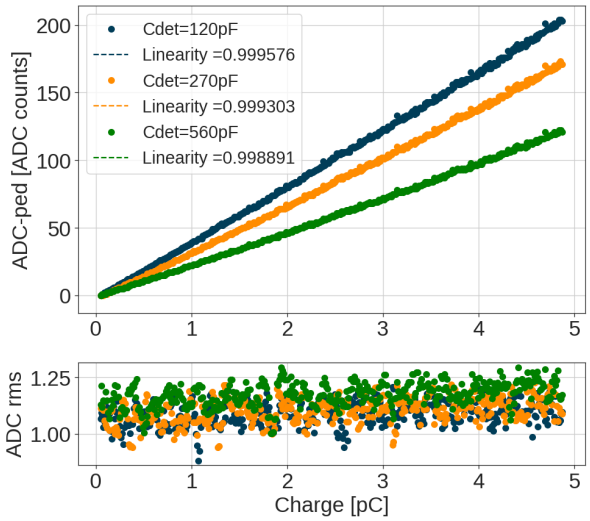

FIGURE 5.32 – *ADC measurement from charge scan using different detector capacitances and the low range internal injection.*

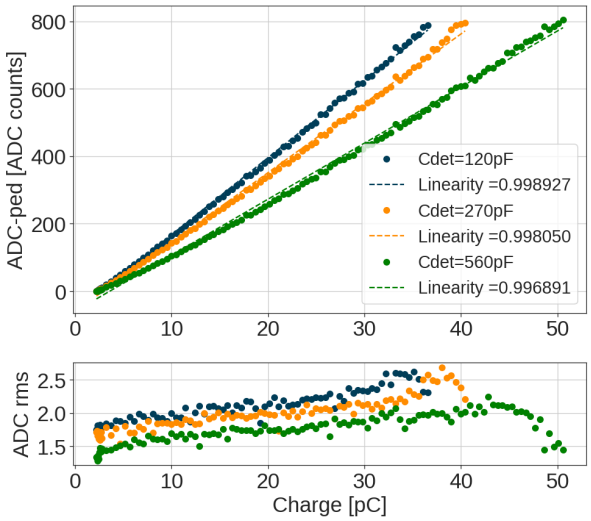

FIGURE 5.33 – *ADC measurement from charge scan using different detector capacitances and the high range internal injection.*

These plots illustrate the impact of detector capacitance : higher capacitance results in longer charging times, reducing the ADC per charge gain and increasing the ADC RMS noise.

Figure 5.33 presents the ADC measurements using the high-range internal injection. An

effect is observed : a large detector capacitance C_{det} creates a slow effect at the beginning of ADC measurements, noticeable in measurements up to 10 pC. This effect arises from the large injector capacitance $C_{inj} = 117pF$ used in this type of charge injection (see Figure 4.50). Moreover, the noise measured from the high-range injection shows a significant increase that does not reflect the real noise levels expected from SiPM measurements.

For ADC measurements, the pedestal value was adjusted to the 150 ADC level to enhance the linearity of charge measurements at the cost of a slight reduction in the ADC range. By selecting an ADC level of 150, non-linearities for small charge injections are significantly reduced. Figure 5.34 displays the resulting integral non-linearities (INL) of the ADC output for different detector capacitances, represented as a percentage of the ADC scale.

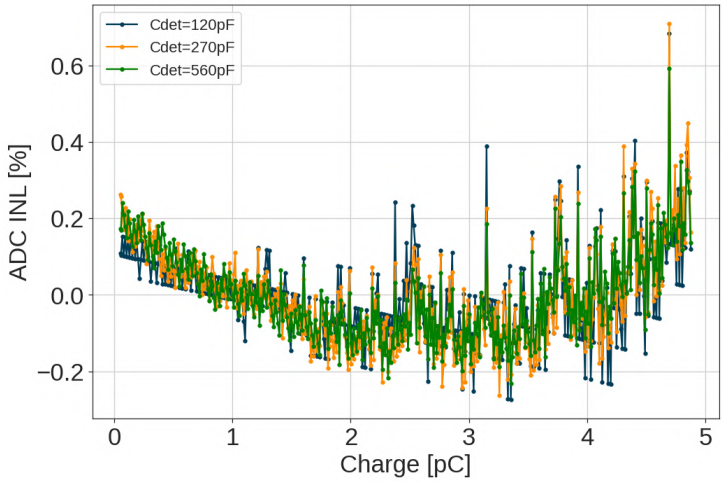

FIGURE 5.34 – *ADC INL percentage measurement for different detector capacitors* C_{det}.

5.4.2 Time-over-threshold technique for charge measurement

When the preamplifier enters the saturation region, the signal duration becomes proportional to the injected charge. The time-over-threshold (TOT) technique reads charge by comparing the preamplifier output to a defined threshold voltage via a discriminator. Upon crossing the threshold, a TDC measures the time until the signal drops below the threshold again. The ASIC subtracts the time measured by the TOT TDC from the time-of-arrival (TOA) TDC. The resulting time corresponding to the signal's duration is sent to the output data.

Figure 5.35 illustrates TOT measurement with the physics configuration using internal injection. Figure 5.35 presents the injection performed with the internal DAC available in the chip, limited to up to 200 pC charge injection. The rest of the charge range (200 pC to 320 pC) was analyzed by injecting externally and it will be presented in the following sections. The TOT performance demonstrates 99.84% linearity up to a charge injection of 200 pC ; until that point, the TOT response follows the linear fit of Equation 5.2. Beyond this point, there is a decrease in the signal duration coming from the preamplifier output. A careful characterization allows software-based correction post-measurement from 200 pC to 320 pC.

$$f(t) = ax + b \tag{5.2}$$

The reason for the non-linear part of the TOT derives from the input shape generated by the SiPM and the coupling between the current conveyor and the preamplifier. The ASIC incorpo-

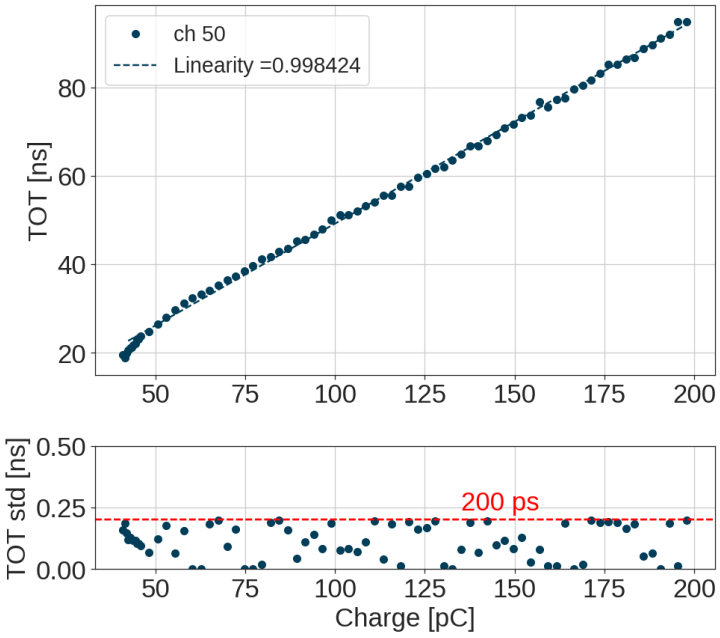

FIGURE 5.35 – *TOT measurement and its rms noise.*

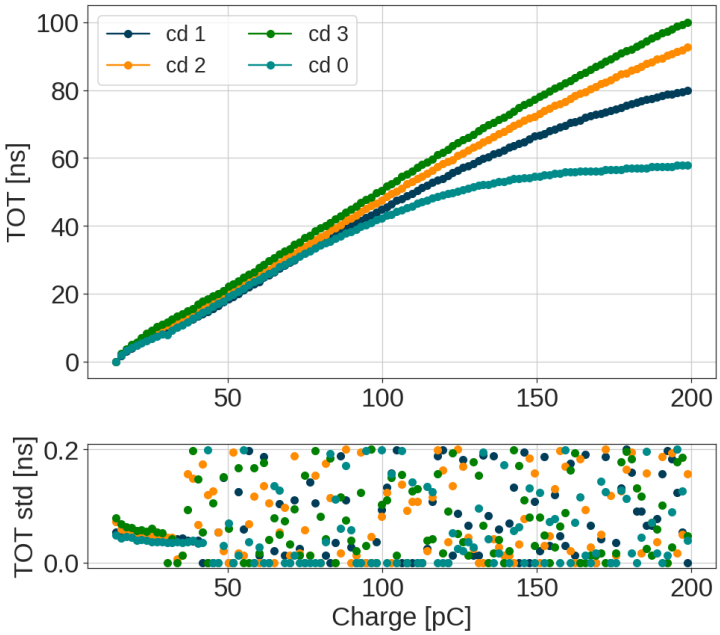

FIGURE 5.36 – *TOT measurement for different C_d capacitors to improve linearity.*

rates a variable capacitor C_d between the current conveyor and the preamplifier. The charging of this capacitor slows down the TOT measurements for charge injection up to 200 pC, resulting in linear measurements. This adjustment enhances the signal's shape at the preamplifier's input but increases the noise levels. The capacitor C_d can be configured with values ranging from 0 to 35 pF. Figure 5.36 illustrates the impact of C_d on TOT linearity. However, considering the significant rise in noise, a value of C_d = 3 (16 pF) was chosen as a good compromise between linearity correction and noise increment for the physics configuration. The calibration configuration maintained $C_d = 0$ for low noise, considering that the SPS signal is expected to

stay within the ADC range.

Figure 5.37 presents the TOT measurements using different detector capacitances C_{det} equivalent to 2 mm², 4 mm², and 9 mm² SiPMs. The three SiPMs exhibit variations in the start of charge injection in the TOT data due to the ADC gain decrement caused by larger detector capacitances. Additionally, all three measurements yield the same TOT resolution below 200 ps.

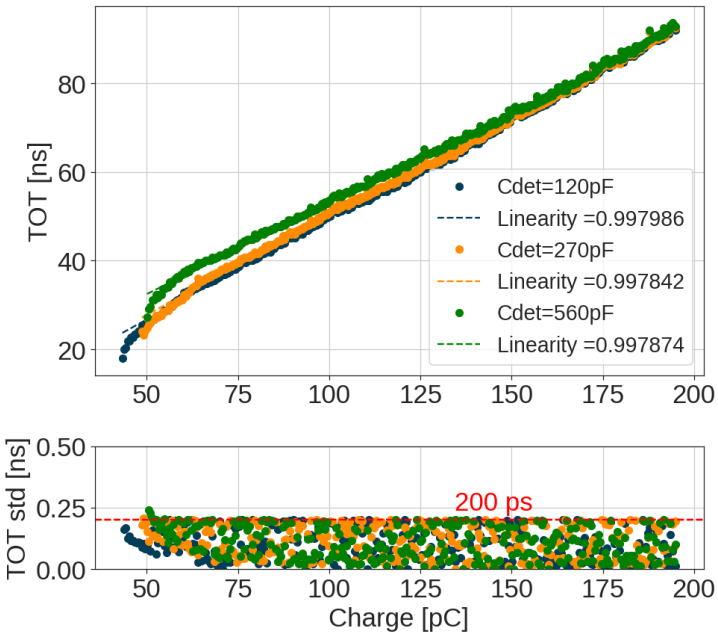

FIGURE 5.37 – *TOT measurement for different detector capacitors* C_{det}.

An additional effect during TOT measurement is observed at the beginning of TOT measurements. Initially, the TOT value exhibits a faster slope until it linearly correlates with the charge. This effect can be reduced using the preamplifier 6-bit DAC $dacbPA$, which adjusts one of the preamplifier currents, enhancing the output signal shape.

5.4.3 Time-of-arrival measurement

TOA measurements are crucial in discriminating pileup events and improving particle identification in collision scenarios. Time measurements aim to achieve accurate timing alongside most of the charge information. The H2GCROCv3 ASIC allows configuring a single global phase and bunch crossing (BX) for data acquisition. Figure 5.38 presents TOA values for different BX and phases and the corresponding ADC values for each time measurement. As observed, the time data depends on the sampling time. Ideally, the TOA measurement is more effective and linear when taken in the middle of the rising slope of the ADC signal. However, to measure charge efficiently, it is necessary to select the peak of the ADC signal. This selection significantly impacts time measurements for slower signals from large SiPM detectors.

The 40 MHz frequency selected requires configuring the ASIC to produce a TOA time walk below 25 ns. If the signal starts within one BX and reaches its peak two BX later, the time walk of the measurement will exceed the 25 ns limit, making it challenging to correlate with the correct charge measurement. Detectors with lower capacitance exhibit shorter time walks, while those with higher capacitance approach the 25 ns limit due to their slower signal generation. Figure 5.39 depicts the system's time walk and associated jitter without any capacitor or detector

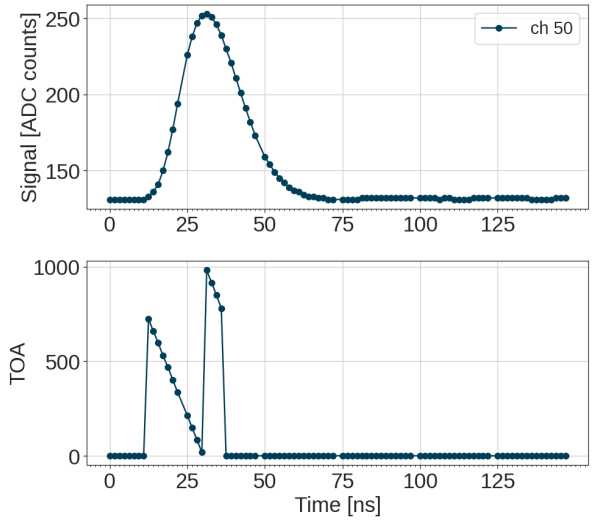

FIGURE 5.38 – *ADC response through time for a 2.5 pC internal injection and its TOA values per sampling scan.*

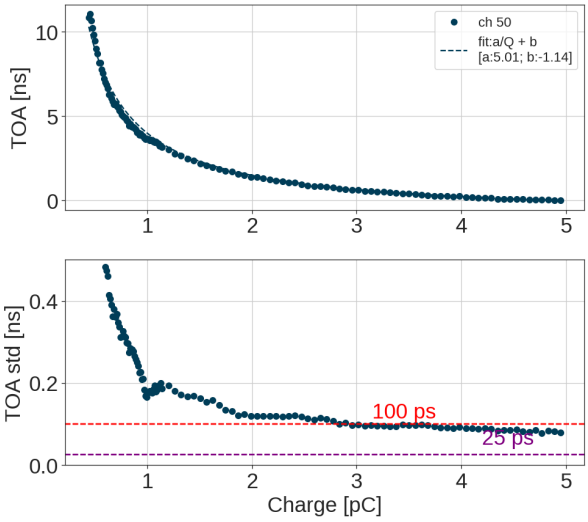

FIGURE 5.39 – *TOA time walk and jitter response from internal injection.*

connected at the input. The time walk generated is approximately 11 ns, producing a jitter below 100 ps for charge values of around 3 pC or higher. The fit of the time walk follows the following equation :

$$f(t) = \frac{a}{t - t_0} + b \tag{5.3}$$

The fit of the jitter follows the following equation :

$$f(t) = \sqrt{\left(\frac{a}{t - t_0}\right)^2 + b^2} \tag{5.4}$$

When the signal duration is extended, the optimal phase for charge measurement may result in poorer jitter performance. The capability to set different measurement phases for TDCs and ADCs will address BX information discrepancies in the future ASIC version. Finally, Figure 5.40 presents the TOA performance with the correct phase for time measurements, demonstrating the performance variations for different detector capacitances corresponding to SiPM sizes in HGCAL.

Furthermore, the increase in noise caused by larger detector capacitances impacts the minimum threshold value available for configuration and significantly affects the resolution of small charge injections. Figure 5.41 illustrates the TOA efficiency for a charge injection scan using different detector capacitances. The minimal charge that achieves TOA data with an efficiency of one varies for each SiPM size (see Figure 5.42). The three SiPM sizes allow for TOA data measurements from minimal charges of approximately 220 fC, 270 fC and 380 fC, respectively. The system achieves a resolution of less than 100 ps, reaching a floor of 25 ps with all detectors. Nevertheless, increasing the detector capacitance affects the jitter for small charge injection and delays achieving 100 ps and 25 ps resolutions.

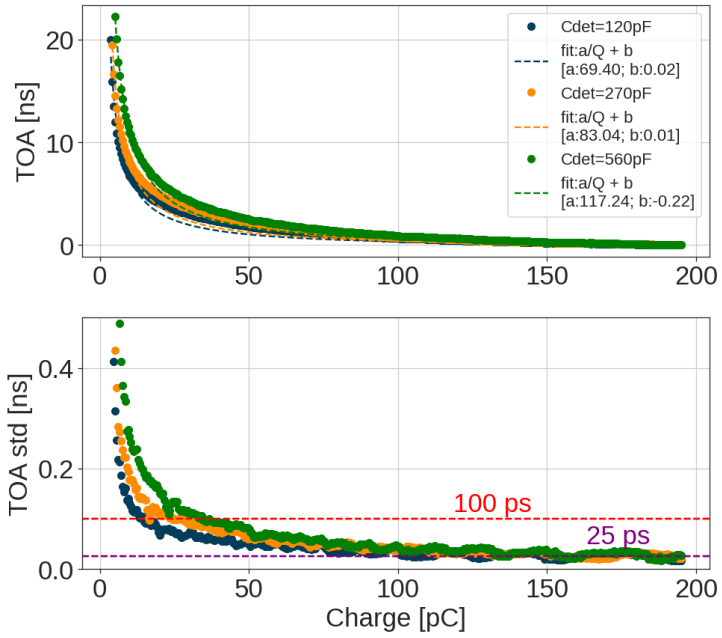

FIGURE 5.40 – *TOA time walk and jitter for different detector capacitors* C_{det}.

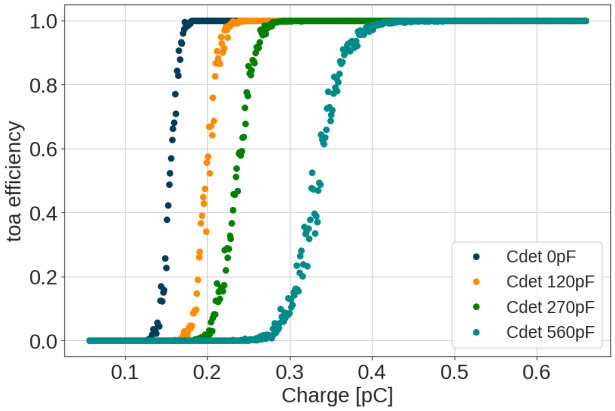

FIGURE 5.41 – *TOA efficiency for charge injection from 0 to 650 fC for different* C_{det}.

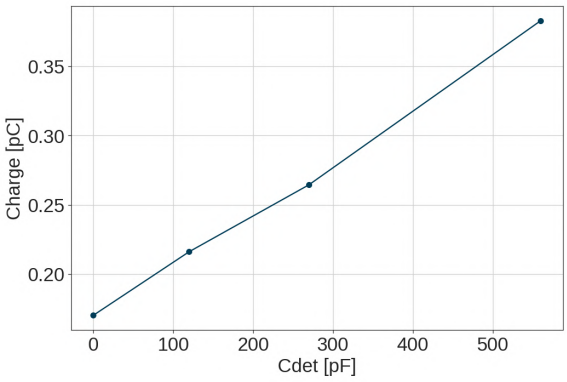

FIGURE 5.42 – *Minimal charge with TOA data for different* C_{det}.

5.5 Noise Analysis and cross-talk evaluation

The noise originating in the front-end chain affects both charge and time measurements. The SiPM detector is the predominant noise source, sensitive to variations in temperature, configured over-voltage and possible background injections. Noise is further amplified by analog and digital blocks within the system, ultimately contributing to the overall noise. Factors like cross-talk between channels, digital coupling and other sources can also impact the measurements. Characterizing the system's noise is crucial for understanding the measurement limitations achievable with the ASIC and implementing necessary corrections in the physics data analysis.

5.5.1 Coherent and correlated noise

The coherent noise refers to all unwanted signals displaying a repetitive and synchronized pattern across the channels of the ASIC. This noise can impact the performance and precision of the ASIC's measurements. Common sources of coherent noise include power supply fluctuations, clock signals, interference from nearby electronic components and external electromagnetic interference. To characterize the coherent noise in the ASIC, we calculate the direct sum (DS) and alternate sum (AS) of the ASIC channel pedestals :

$$DS = \sum ped[i] \tag{5.5}$$

$$AS = \sum (-1^i) ped[i] \tag{5.6}$$

Next, the incoherent noise (IN) considers the noise in the alternate sum, normalized by the number of channels (N) to provide a per-channel noise. The coherent noise (CN) measures the interference between channels, also normalized by the number of channels. It quantifies how much variance in the direct sum differs from that in the alternate sum. The equations to calculate IN and CN are as follows :

$$IN = \frac{rms(AS)}{\sqrt{N}} \tag{5.7}$$

$$CN = \frac{\sqrt{(var(DS) - var(AS)}}{N} \tag{5.8}$$

Characterizing this noise is crucial for understanding the ASIC's trigger data output, which employs the sum of several channels as trigger information. The chip incorporates two common-mode channels per half for physics data measurement to mitigate the effects of coherent noise.

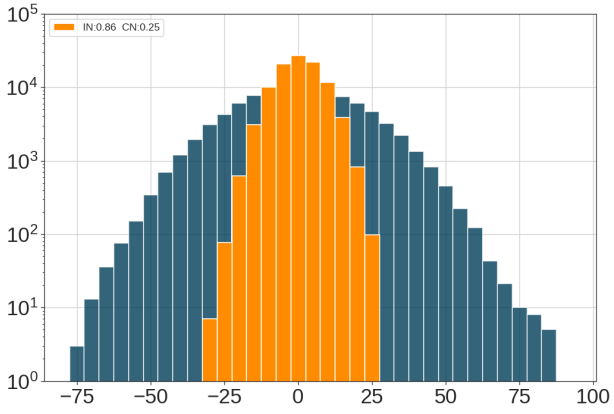

FIGURE 5.43 – *ASIC's Coherent noise extracted by comparing the direct and alternate sums of N channels.*

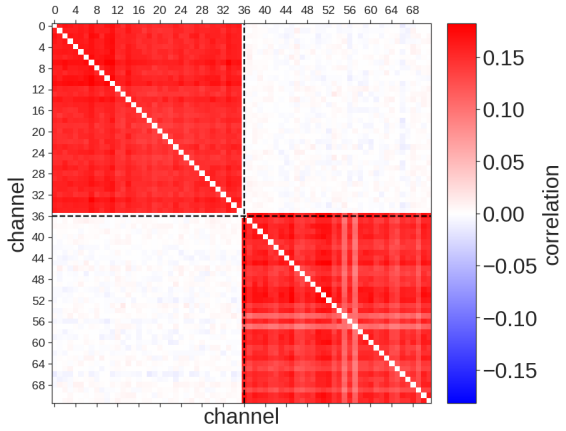

FIGURE 5.44 – *Correlation matrix of the channels of one H2GCROCv3 ASIC.*

The coherent noise of the chip is illustrated in Figure 5.43. The calculated CN is approximately 0.35 ADC units (0.34 % of ADC range), indicating low coherent noise for the ASIC.

Figure 5.44 presents the correlation matrix, illustrating the relationship between channels. It shows that the correlation per half is less than 0.15, revealing a minimal correlation between the ASIC's independent halves.

5.5.2 Charge measurements noise

H2GCROC was designed to maintain low noise levels, with the detector noise dominating the overall system noise. Analyzing the noise formula of a SiPM reveals a considerable impact from the detector capacitance. Initially, a capacitor connected to the ASIC's input was used to emulate noise generated by SiPMs of various sizes. Figure 5.45 illustrates the ADC RMS noise measured with the two proposed ASIC configurations and detector capacitance C_{det} up to 1 nF. Markers indicate the expected system noise for 2 mm², 4 mm² and 9 mm² detectors.

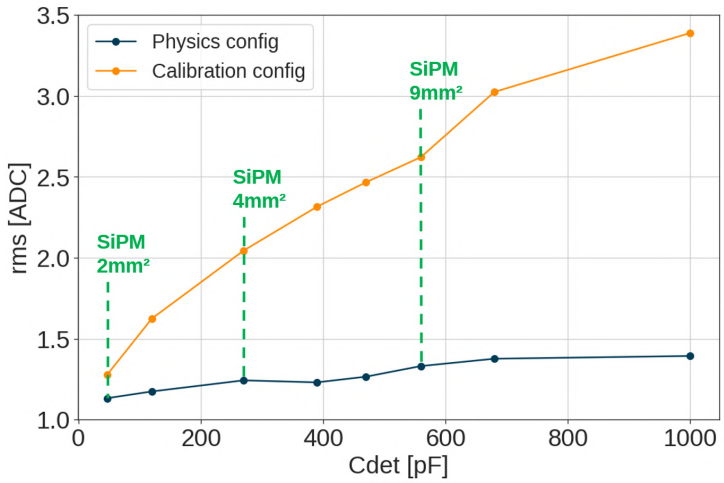

FIGURE 5.45 – *ADC rms for different detector capacitors C_{det} with the Physics and Calibration configurations.*

The difference in noise between the two configurations derives from their distinct purposes. On the one hand, physics configurations aim to minimize noise for precise measurements, optimal linearity and coverage of the full range of charge measurements. On the other hand, calibration configurations seek to maximize the photon separation to improve SiPM gain measurements.

Next, the noise was measured using laser injection into the 2 mm² and 9 mm² SiPMs. The injected signal was approximately 15 photons corresponding to one MIP from the scintillator tile. Figure 5.46 presents the signal of around 15 photons measured with both detectors and the proposed configurations. As expected, the signal measured with the 9mm² SiPM is slower, and the gains of the Calibration configuration are more significant.

The noise levels of the 2 mm² and 9 mm² SiPMs can be evaluated by connecting them to one channel and measuring the ADC's pedestal response. Figure 5.47 illustrates the RMS noise of the ADC measurements. There is an increment compared to the measurements made with the injection capacitor at the input. This increment comes from the high voltage applied to the SiPMs and the measurement of the dark current. Both SiPMs have similar noise in the Physics configuration, but the larger capacitance of the 9 mm² produces a larger noise for the Calibration configuration, as expected. Figure 5.48 shows the MIP injection's signal-to-noise ratio (SNR) with both configurations.

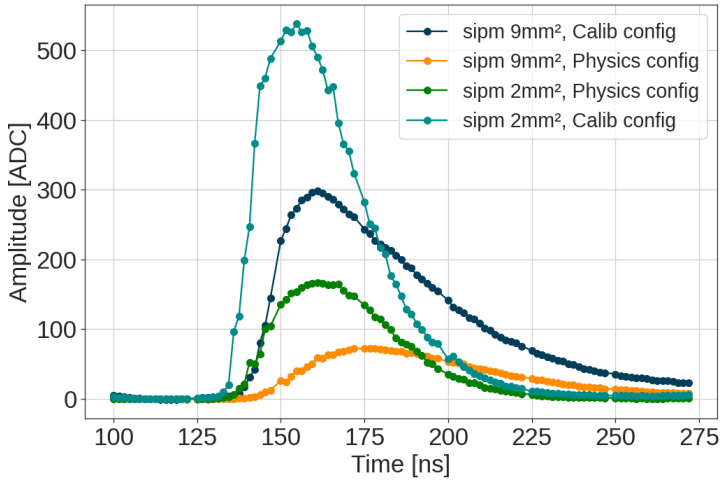

FIGURE 5.46 – *ADC mean signal minus pedestal to a MIP injection of around 15 p.e. for the two SiPM of HGCAL with 2 mm² and 9 mm² areas.*

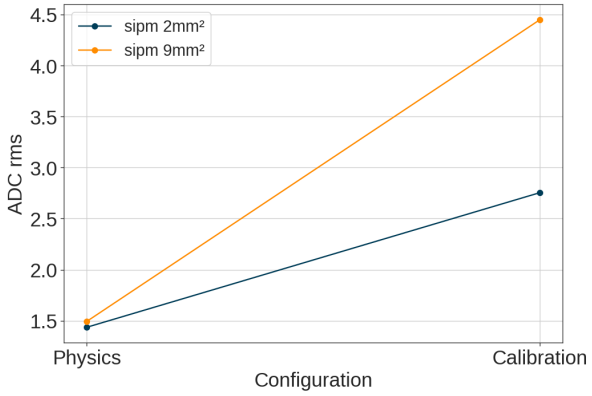

FIGURE 5.47 – *ADC rms for the two SiPM of HGCAL with 2 mm² and 9 mm² areas.*

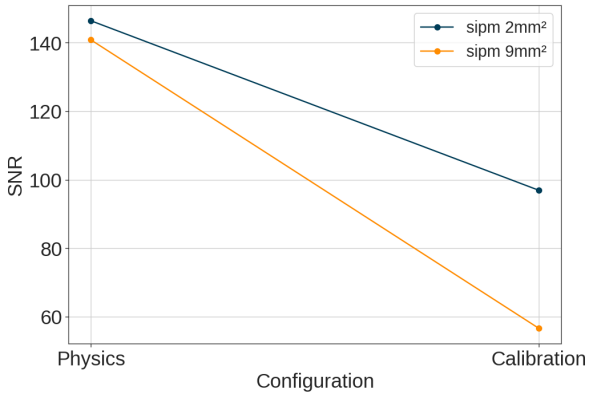

FIGURE 5.48 – *Signal-to-noise ratio (SNR) measured with the two SiPMs for the physics and calibration configurations.*

5.5.3 Cross-talk

From the coherent noise analysis, a minimal correlation is observed between the two independent halves of the chip. However, independent signals arriving at one channel are expected to affect other channels, particularly neighboring ones. Figure 5.49 illustrates the ADC signal of the two closest channels and one from the other half after a MIP signal injection corresponding to 15 photons injected into one ASIC channel using the Physics configuration and a 2mm² SiPM. The results show no crosstalk in the other half of the chip and reduced crosstalk that diminishes for the farthest channels. Figure 5.50 presents the same measurements but using the Calibration configuration of the chip. In this case, the crosstalk effect increases by around 0.5 ADC units.

After performing the MIP injection using a 9 mm² SiPM, Figure 5.51 presents low crosstalk using the Physics configuration, and Figure 5.52 shows a bit increment for the Calibration configuration. In summary, the crosstalk on the chip corresponds to less than 1% of the ADC range.

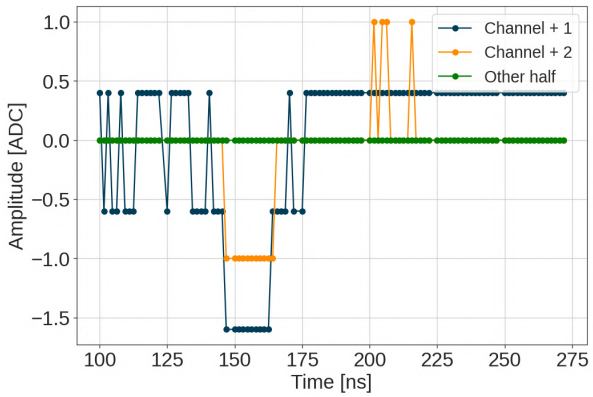

FIGURE 5.49 – *Cross-talk measurements after one MIP injection using the 2 mm² SiPM and the Physics configuration (MIP ≃ 160 ADC counts).*

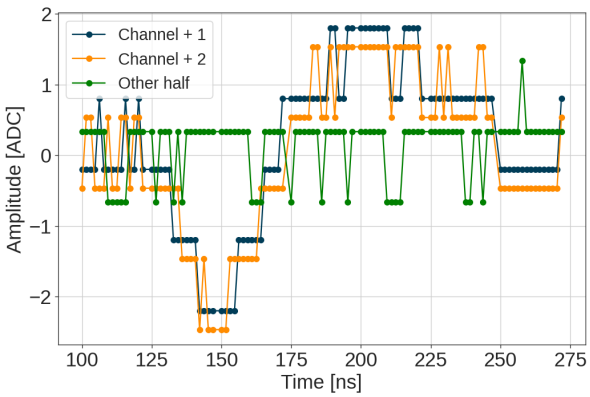

FIGURE 5.50 – *Cross-talk measurements after one MIP injection using the 2 mm² SiPM and the Calibration configuration (MIP ≃ 520 ADC counts).*

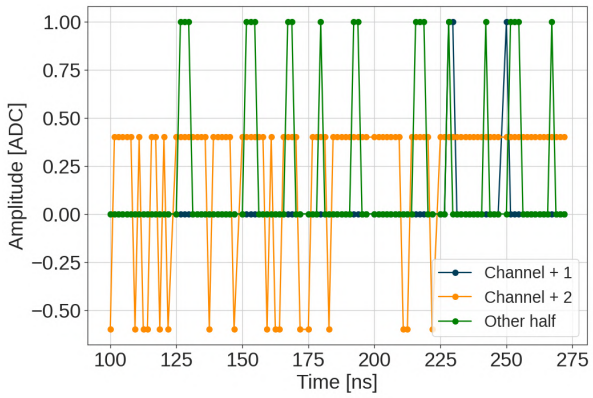

FIGURE 5.51 – *Cross-talk measurements after one MIP injection using the 9 mm² SiPM and the Physics configuration (MIP ≃ 80 ADC counts).*

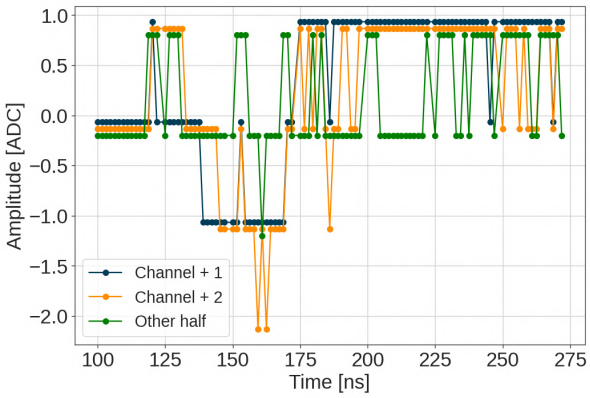

FIGURE 5.52 – *Cross-talk measurements after one MIP injection using the 9 mm² SiPM and the Calibration configuration (MIP ≃ 300 ADC counts).*

5.5.4 Trigger path measurements

As mentioned in Section 4.3.7, the ASIC sends its measurements through two outputs : the data path provides information on the charge and time of each readout channel. In contrast, the trigger path performs the sum of 4 or 9 channels and linearizes the charge data from ADC and TOT measurements.

To configure the trigger path, first, the FIFO latency is adjusted to ensure the correct bunch crossing for charge sums. Second, the parameters shown in Figure 4.15 can be configured via slow control to adjust the channel pedestal, TOT threshold, and ADC/TOT noise. This ensures a linear response of charge measurements at the trigger path output. Figure 5.53 illustrates the output of the trigger path, measured from the sum of 9 channels after injecting charges up to 200 pC into one channel of the ASIC.

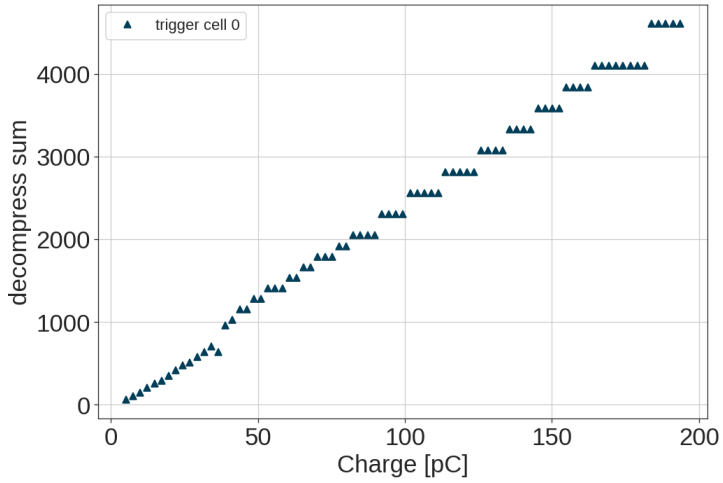

FIGURE 5.53 – *Trigger path output measured from the sum of 9 channels after internal injection in one channel of H2GCROC3 ASIC.*

5.6 Temperature analysis

In the HGCAL experiment, the ASIC is designed to operate at temperatures as low as -30 ℃. Consequently, the chip must maintain its normal functionality over a wide temperature range, from the anticipated -30 ℃ to slightly above room temperature. The ASIC was tested inside the climatic chamber Kambic TK-105 CKLT [71] to assess its performance under such conditions.

The test involved decreasing the temperature to -40 ℃ and raising it to 50 ℃. During the cooling and warming of the chip, the chip performance was analyzed by collecting data on pedestals, the ASIC's DACs, the current of the three power supplies of the ASIC, and every reference voltage available at the DC outputs. Charge injection scans were also conducted to assess the linearity of the analog-to-digital converter (ADC) and the performance of time-over-threshold (TOT) and time-of-arrival (TOA). Among the most relevant tests were those examining pedestal variations with temperature and readings of the bandgap voltage. Characterizing the bandgap voltage with temperature is crucial as it serves as the reference voltage for various configurations within the chip.

Figure 5.54 depicts the pedestal variation observed in four selected channels, with detector capacitors C_{det} of 0, 120 pC, 270 pC and 560 pC, respectively, throughout the temperature scan ranging from -40 ℃ to +50 ℃. Figure 5.54 a) displays the pedestal increment for the Physics mode configuration, while Figure 5.54 b) illustrates the increment for the calibration mode configuration. In both configurations, an increase in pedestal level is noticeable as temperature rises. Notably, the calibration mode experiences the most significant impact, with an approximate increment of about 60 ADC counts. On the contrary, the physics mode exhibits a lower increment of approximately 20 ADC counts. Across both configurations, a larger C_{det} mitigates the rise in pedestal level as temperatures increase.

Figure 5.55 highlights the consistent pedestal variations observed across channels throughout the temperature range. Notably, there is a variance in ADC per ℃ in the calibration configuration between the two halves of the chip. During testing, the first half of the chip, composed of channels 0 to 35, had no C_{det} at their inputs, while channels 36 to 71 on the second half of the chip had at least $C_{det} = 47\,pF$ at the input. This effect was expected, as the capacitor at the input reduces the channel's gain, consequently mitigating the impact of temperature on the ADC per ℃ variation.

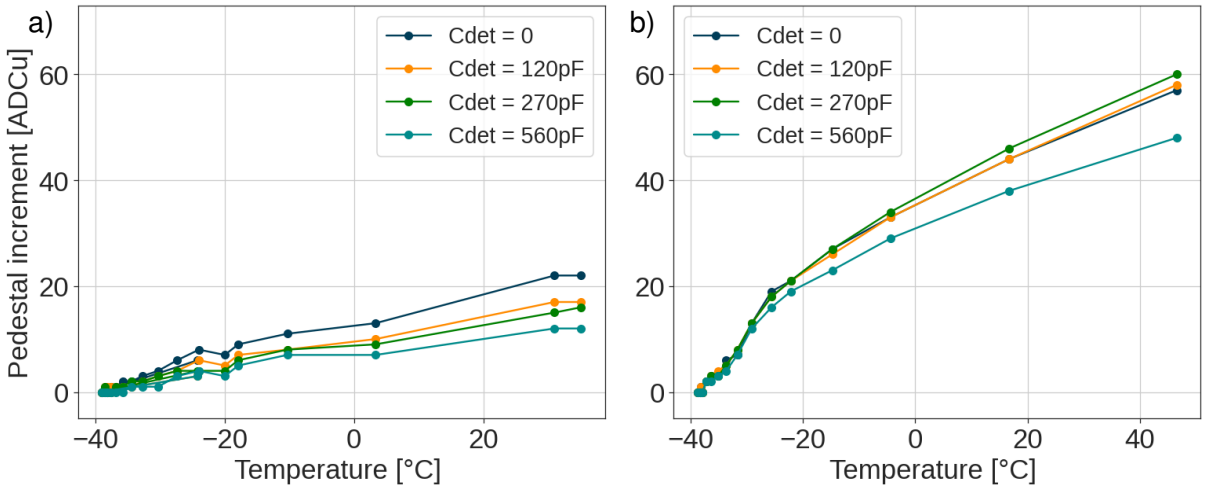

FIGURE 5.54 – *Pedestal variation for different temperatures in channels with different detector capacitors C_{det} ; a) For Physics configuration and b) for Calibration configuration.*

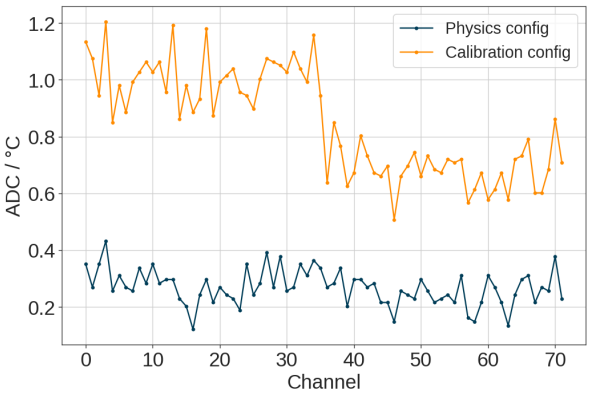

FIGURE 5.55 – *ADC variation per °C for all channels in Physics and Calibration configurations.*

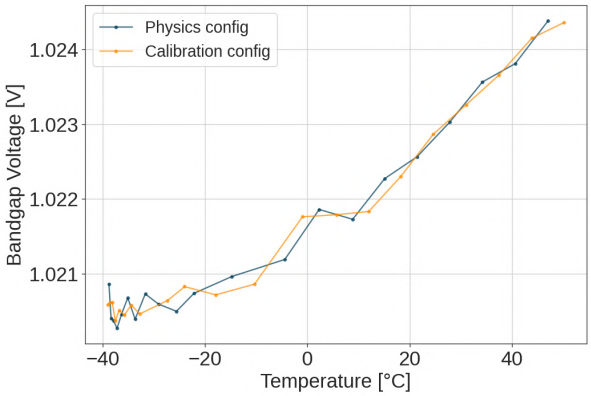

FIGURE 5.56 – *Bandgap voltage measurements for different temperatures.*

Figure 5.56 additionally illustrates the variation in bandgap voltage at different tested temperatures. Noticeably, the values obtained using the two chip configurations demonstrate that the bandgap voltage remains unaffected by the gain settings of the chip. From the plot, the bandgap value displays two distinct slopes for temperature variation : an approximate variation of 12.5 μV/°C for cold temperatures up to -10 °C and 65 μV/°C for temperatures from -10 °C to 50 °C.

Additionally, Figure 5.57 provides insights into the chip's performance during charge injection at extreme cold and hot temperatures. The tests delivered no observable change in noise levels at the different measured temperatures. However, the ADC shape response to the charge injection has a slight variation that is considered negligible because it maintains its good performance. For the HGCAL project, it will work at a maintained temperature of -30 °C.

The results conclusively demonstrate that the H2GCROCv3 ASIC maintains its performance across a broad temperature range from -39 °C to 50 °C. This temperature characterization enables the necessary corrections in case of temperature fluctuations during measurements in regular HGCAL operation.

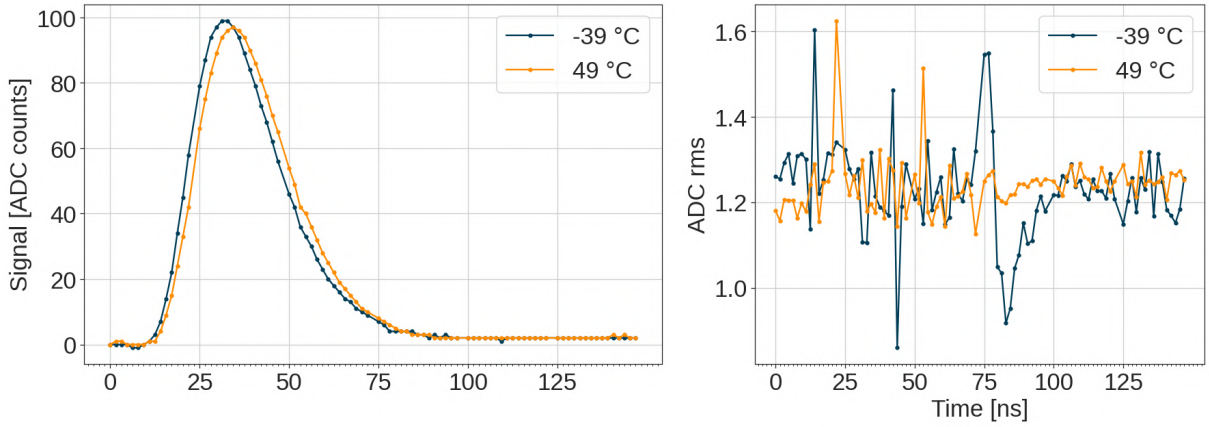

FIGURE 5.57 – *Comparison of the ADC response through time and its rms noise for -39 ℃ and 49 ℃.*

5.7 Radiation tolerance of H2GCROC

The increase in luminosity of HGCAL will also result in higher irradiation exposure for both the detectors and the calorimeter's ASICs. During the initial design of HGCAL, the dose of ionizing radiation accumulated (Figure 5.58) and the fluence of 1 MeV equivalent neutrons accumulated (Figure 5.59) after an integrated luminosity of $3000 fb^{-1}$ were simulated using the FLUKA program [72] [73]. This simulation accounted for the number of particles reaching different parts of the calorimeter from each collision and considered the expected 10-year lifetime of the detector.

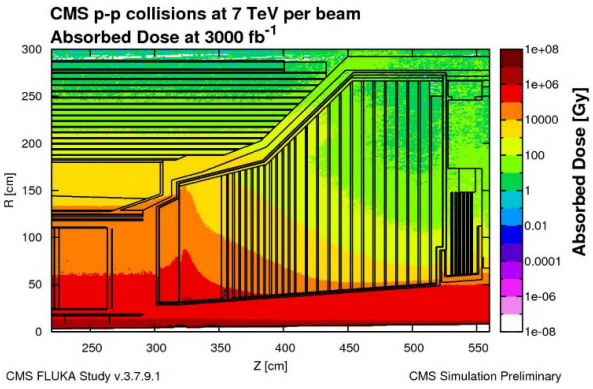

FIGURE 5.58 – *Dose of ionizing radiation accumulated in HGCAL after an integrated luminosity of* $3000\ fb^{-1}$*, simulated using the FLUKA program [72] [73] and shown as a two-dimensional map in the radial and longitudinal coordinates, r and z. [2]*

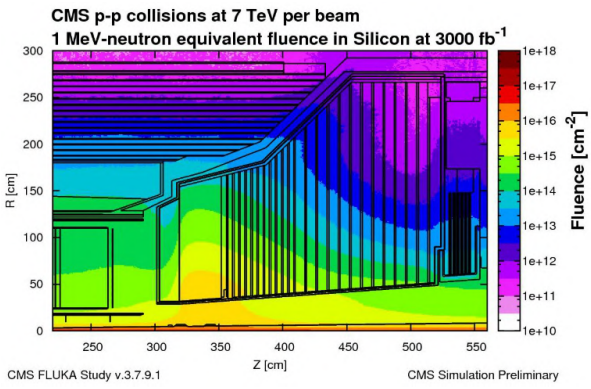

FIGURE 5.59 – *Fluence, parameterized as a fluence of 1 MeV equivalent neutrons, accumulated in HGCAL after an integrated luminosity of* $3000\ fb^{-1}$*, simulated using the FLUKA program [72] [73] and shown as a two-dimensional map in the radial and longitudinal coordinates, r and z. [2]*

Anticipated radiation will result in an accumulated dose of 200 MRad for the Electromagnetic calorimeter and the first section of the Hadronic calorimeter, where Silicon detectors will be used. In contrast, the back part of the Hadronic calorimeter is expected to accumulate a maximum dose of 300 kRad.

The simulated radiation of HGCAL led to select Silicon sensors, where significant radiation damage is expected, and SiPMs, where the radiation levels are less severe. On the other hand, Silicon detectors are less sensitive to radiation and offer higher measurement precision. Even with a high accumulated dose and fluence, the damage to the Silicon sensors is expected to result in less than 50 μA of leakage current at the end of the calorimeter's lifetime. On the other hand, SiPMs are more susceptible to radiation damage. Irradiated SiPMs, even with a lower accumulated dose and fluence expected, can produce leakage currents in the mA range at the end of the detectors' lifetime. Nevertheless, these detectors were selected for the back hadronic section of the calorimeter due to their high accuracy and cost-effectiveness.

Additionally, radiation can lead to malfunctions in electronics and errors in digital memory or data processing. The Total Ionizing Dose (TID) comes from sources of particles like X-rays and causes cumulative damage. Continuous exposure to this type of radiation can impact the behavior of electronics. However, when the electronics or detectors are not used, the annealing process can slowly repair some malfunctions. Accumulated dose radiation damage typically affects analog electronics more severely and less impacts digital memories, PLLs, or data processing. Among the characteristics of analog electronics, it is known from the literature that radiation can increase noise levels and, at high doses, stop electronic functionality.

Regarding the expected radiation fluence, it results in radiation damage induced by a single particle to electronic devices and is non-cumulative. This type of radiation produces what is known as Single Event Effects (SEE), which can occur any time from the start of HGCAL's operation. There are three types of SEE :

— Single Event Upset (SEU) causes a bit flip from 0 to 1 or 1 to 0.
— Single Event Transient (SET) produces a bit shift.
— Single Event Latchup (SEL) results in permanent damage where the particle is impacted.

This irradiation predominantly affects the digital part of the ASIC, leading to changes in memory, data transfer, or PLL.

The objective of the ASIC is to maintain front-end performance, memory integrity and data processing capabilities throughout the entire lifetime of HGCAL, considering the anticipated radiation. Furthermore, it must compensate for the maximum expected leakage current from the detectors.

Several tests were conducted to demonstrate that both ASICs are radiation-resistant and meet the specifications by injecting high particle doses to simulate the expected radiation damage at the end of the detector's lifetime. For SEE testing, different particles induce damage in various parts of the electronics. Therefore, two types of tests were performed by injecting heavy ions and protons. Additionally, the DESY laboratory in Hamburg was responsible for testing the irradiation damage on SiPMs, which needed to be considered for leakage current compensation in the ASIC design.

The family of HGCROC ASICs was tested involving three different types of particle injections :

— **TID Campaign :** This test aimed to assess the accumulated dose at a rapid injection rate, reaching 345 Mrad for the Silicon version and 20 Mrad for the SiPM version of the ASIC.
— **Injection of Heavy Ions :** This test evaluated the Single Event Effects (SEE) damage caused by different ions : Ne, Al, Ar, Cr, Ni, Kr and Xe.
— **Injection of Protons :** This test was specifically performed to examine SEE damage where protons can potentially induce more severe damage, such as to the PLL of the ASIC.

5.7.1 TID Setup

The TID campaigns were carried out at CERN facilities using two different X-ray machines : Obelix (Figure 5.60) and Asterix (Figure 5.61). Both X-ray machines are placed inside a chamber that allows temperature reduction using a cooling system and maintains a controlled humidity level for optimal electronic performance.

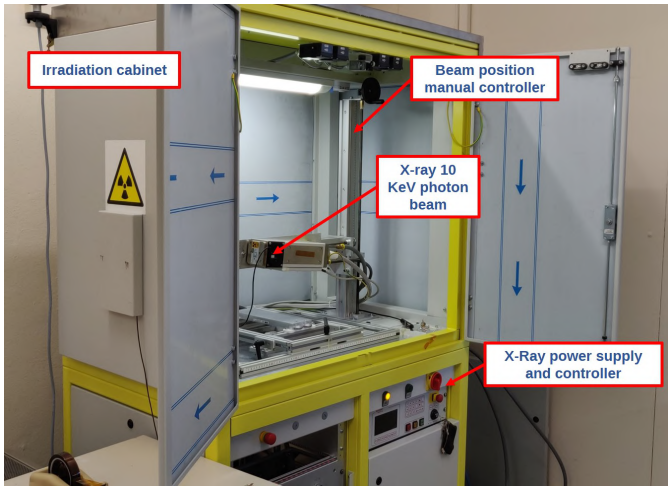

FIGURE 5.60 – *ObeliX system composed of an X-ray machine Seifert RP149, a rectangular thermal plate, a Huber Unistat 705 cooling element to set the temperature of the device under test and a system to lower the dew point inside the cabinet using dry air. [74]*

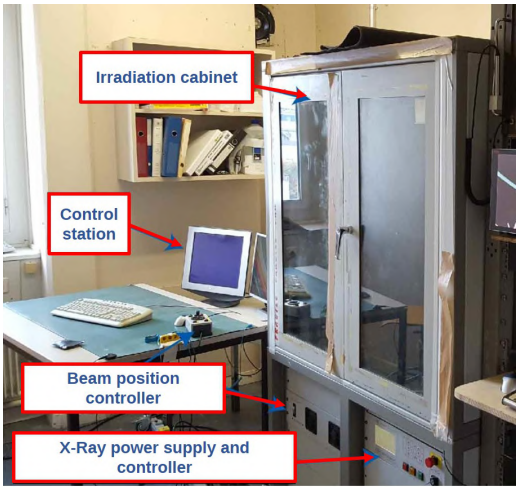

FIGURE 5.61 – *AsteriX system composed of an X-ray machine Seifert RP149, a cooling element to set the temperature of the chuck and a system to lower the dew point inside the cabinet using dry air. [75]*

Removing a significant part of the ASIC's package in irradiation tests helps to expose the chip design to irradiation. Figure 5.62 displays the material that needs to be eliminated from the package to expose the ASIC. This process involved sanding the chip to expose the silicon top part of the ASIC while avoiding damage to the transistors and connections. Figure 5.63 presents one ASIC with the package on the left and another ASIC after the thinning procedure.

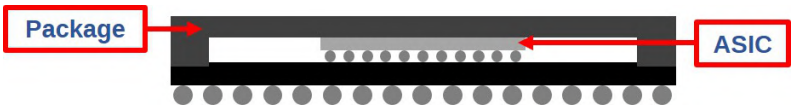

FIGURE 5.62 – *Bumb bonding and package of H2GCROC.*

From the available H2GCROC test bench, the socket boards are excellent for chip exchange and testing multiple chips. The strength of the socket was carefully designed, considering the density of the entire ASIC package. The thinning procedure significantly reduced the package's density. Consequently, the socket's strength was excessive, leading to breaks in the chip circuits and producing a short circuit on sanded chips placed into the socket. Therefore, it was decided to irradiate SiPM ASICs without removing anything from the package. The attenuation due to the packaging material was measured to be approximately 0.4, reducing the dose reaching the ASIC.

Figure 5.64 illustrates the Obelix machine injecting particles with a 10 keV photon beam into an H2GCROC ASIC with a socket board. The X-ray source was configured to inject 2.375 Mrad/h, targeting the entire electronics area within the Low-density package of the ASIC. The

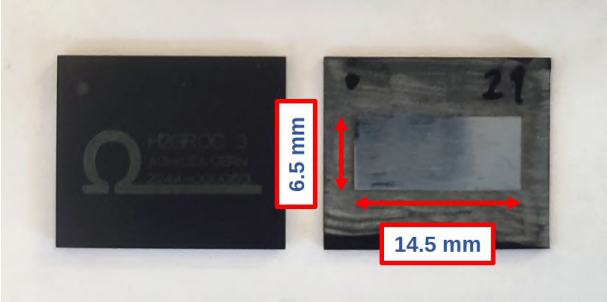

FIGURE 5.63 – *ASIC package before and after sanding process.*

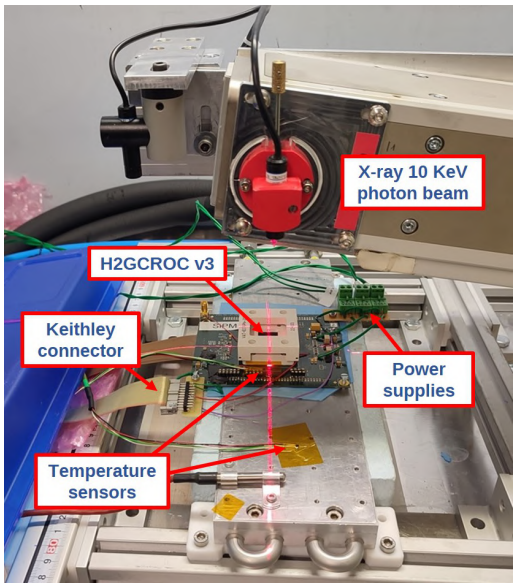

FIGURE 5.64 – *Setup for TID campaign using ObeliX X-ray machine at CERN.*

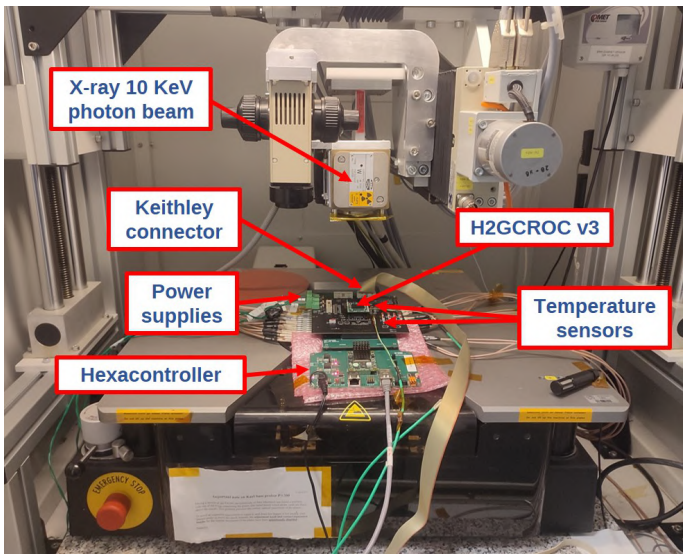

FIGURE 5.65 – *Setup for TID campaign using AsteriX X-ray machine at CERN.*

ASIC's packaging material between the X-ray source and the ASIC reduced the particle count by a 0.4 attenuation, resulting in an injection speed of 0.95 Mrad/h. Figure 5.65 presents the Asterix machine with an H2GCROC mezzanine board and an X-ray injection rate of 0.98 Mrad/h, corresponding to 0.392 Mrad/h after accounting for the reduction caused by the ASIC package.

During X-ray irradiation, the chip's performance was analyzed, including data collection for pedestals, a time scan with the injection of a selected charge value using the internal capacitor and DAC of the ASIC, and an injection scan utilizing the same internal injection for the entire range of charges available from the DAC and injection capacitor. Figures 5.64 and 5.65 display the connection of a Keithley multimeter to measure the reference voltages of the chip and two voltage sources (2.5 V VDDA, 1.2 V VDDA) originating and measured using an Agilent power source. The digital voltage (1.2 V VDDD) was provided by another power source not measured during the test. Only the voltage and current variation of the two analog sources (VDDA) were measured. Since both the Si and SiPM versions of the ASIC share the digital part in their designs and because of the limited power sources available for reading, it was decided to analyze the VDDD only in the TID campaigns of the Si version of the chip.

Both setups employed two PT100 temperature sensors for temperature measurements : one close to the ASIC and a second within the structure containing the test bench. The chamber's cooling system could lower the plate's temperature with the test bench to -30 °C. However,

when the cooling system was activated at the lowest temperature, the temperature near the ASIC remained at around -7 ℃ due to the separation between the ASIC and the cooling plate.

5.7.2 TID campaigns

Figures 5.65 and 5.64 show the setups at Obelix and Asterix machines, respectively. Both tests were designed similarly, with only three differences. The first test conducted at the Obelix machine had a higher available dose rate, irradiating the chip up to 19 Mrad. In contrast, the second test conducted at the Asterix machine irradiated the ASIC up to 6.4 Mrad. The second difference is that the Asterix test included an additional assessment to check the performance of the ASIC's DACs. Finally, the second test used two different configuration files during the data taking of the ASIC measurements, corresponding to Calibration and Physics configuration modes.

The initial step in configuring the X-ray machines for radiation injection is to set the beam size and align it in the correct position to irradiate the entire ASIC layout area at the maximum possible rate. For example, Figure 5.66 shows the expected radiation dose at the Asterix beam target configured to inject the area of the H2GCROCv3 layout (14.5 x 6.5 mm). The ASIC's area is highlighted in yellow, indicating a maximum dose rate of 1.07 Mrad/h, a minimum of 0.88 Mrad/h and an average dose rate of 0.98 Mrad/h.

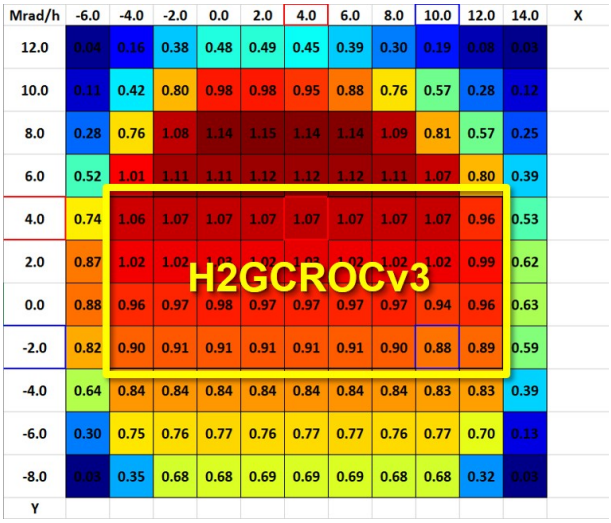

FIGURE 5.66 – *Calibration map of Asterix X-ray machine at CERN.*

The first test at the Obelix machine consisted of irradiation at the maximum dose available (0.95 Mrad/h after attenuator factor) with the cooling activated. The PCB had a temperature of -7 ℃, and the cooling plate's temperature was -26 ℃.

After continuous irradiation for around 20 hours, the chip reached an accumulated dose of 19.5 Mrad. Figure 5.67 presents measurements of the VDDA power sources. The technology anticipates a peak in the voltage sources at around 5 Mrad. This peak is evident in the current of the 1.2 V VDDA. In contrast, the current of the 2.5 V VDDA exhibits a linear decrease during the total irradiation exposure. Figure 5.67 c) shows an increment of around 165 mA at the peak of the curve at cold temperature, and Figure 5.67 d) shows a total decrement of 15 mA. The red dotted line marks the total accumulated dose expected during the lifetime of HGCAL. Within this range, the changes due to irradiation are not considerable. Similarly, the chip's performance and noise levels remain stable for an accumulated dose of up to 300 kRad. However, the total irradiation studied in the test does have an impact on the electronics.

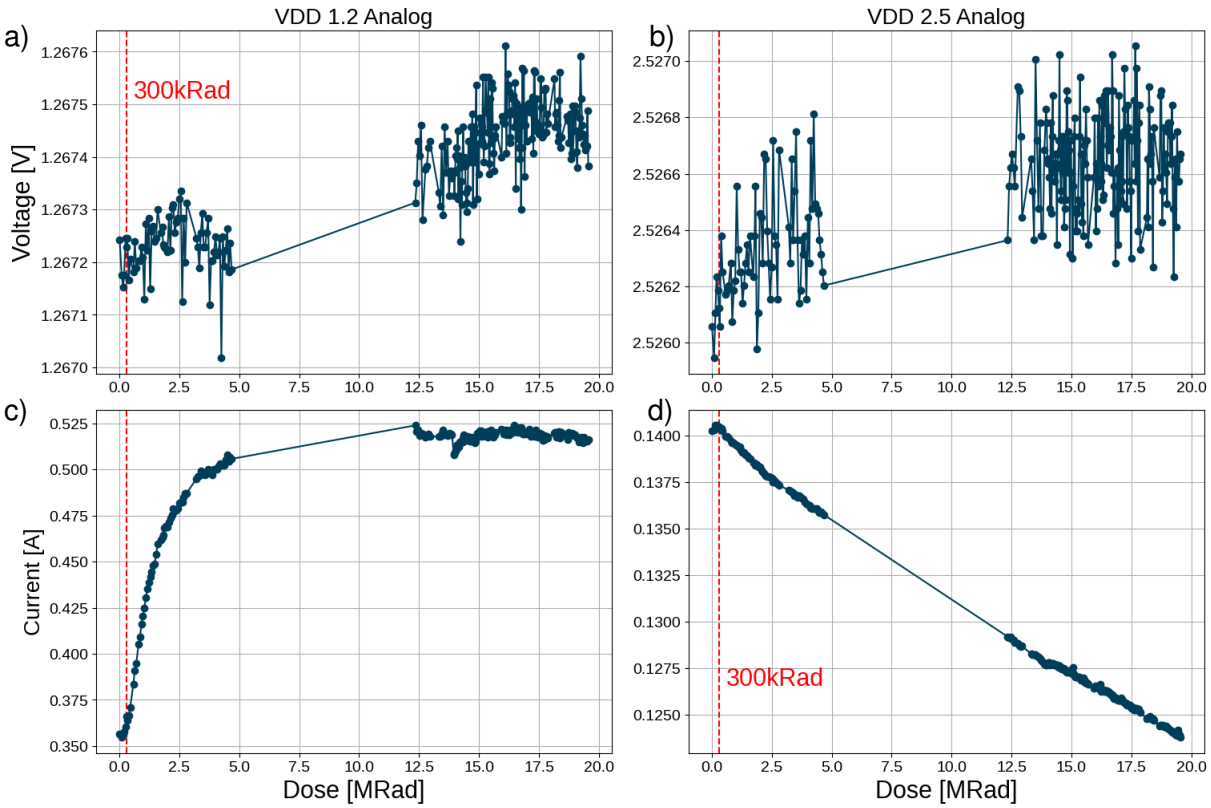

FIGURE 5.67 – *Power supplies measurements of H2GCROC after 19 Mrad accumulated dose. a) 1.2 VDDA voltage, b) 2.5 VDDA voltage, c) 1.2 VDDA current, d) 2.5 VDDA current.*

Comparing the irradiation results of the SiPM version of the ASIC with the Si version, both versions face the same issue of current increment on the analog current. Figure 5.68 shows the VDDA and VDDD power source measurements on the HGCROC TID campaign. Both voltages are stable with minor variations up to 20 Mrad. The current of the VDDD does not suffer a considerable increment with the exposed radiation. Figure 5.69 compares the current increment from both versions of the ASIC with an accumulated dose of around 20 Mrad, both at cold temperatures, using the Obelix machine. From the power supplies results, we can conclude that although the chips continue performing after 20 Mrad of accumulated dose, an increment of around 150 mA is unacceptable for power consumption.

Therefore, the source of the problem was investigated to understand this current increment and find a solution for the next ASIC version. The first approach to finding the problem was to conduct a dedicated TID campaign at different dose rates, disabling some parts of the ASIC front-end and reading the current with three different configurations on the chip :

— **Standard :** All the front-end of the ASIC enabled.
— **noDiscri :** Turn off the discriminators.
— **noRtR :** Turn off the discriminators and shapers.
— **noPreamp :** Turn off the discriminators, shapers and preamplifiers.

Moreover, this new test was planned with different dose rate irradiation to check the effect of the dose rate on the current increment. The peak of the current maintains its previous behavior, reaching the peak at around 5 Mrad, showing no effect coming from the change of dose rate irradiation. Moreover, the results presented in Figure 5.70 show that turning off the analog blocks of the front-end does not eliminate the problem.

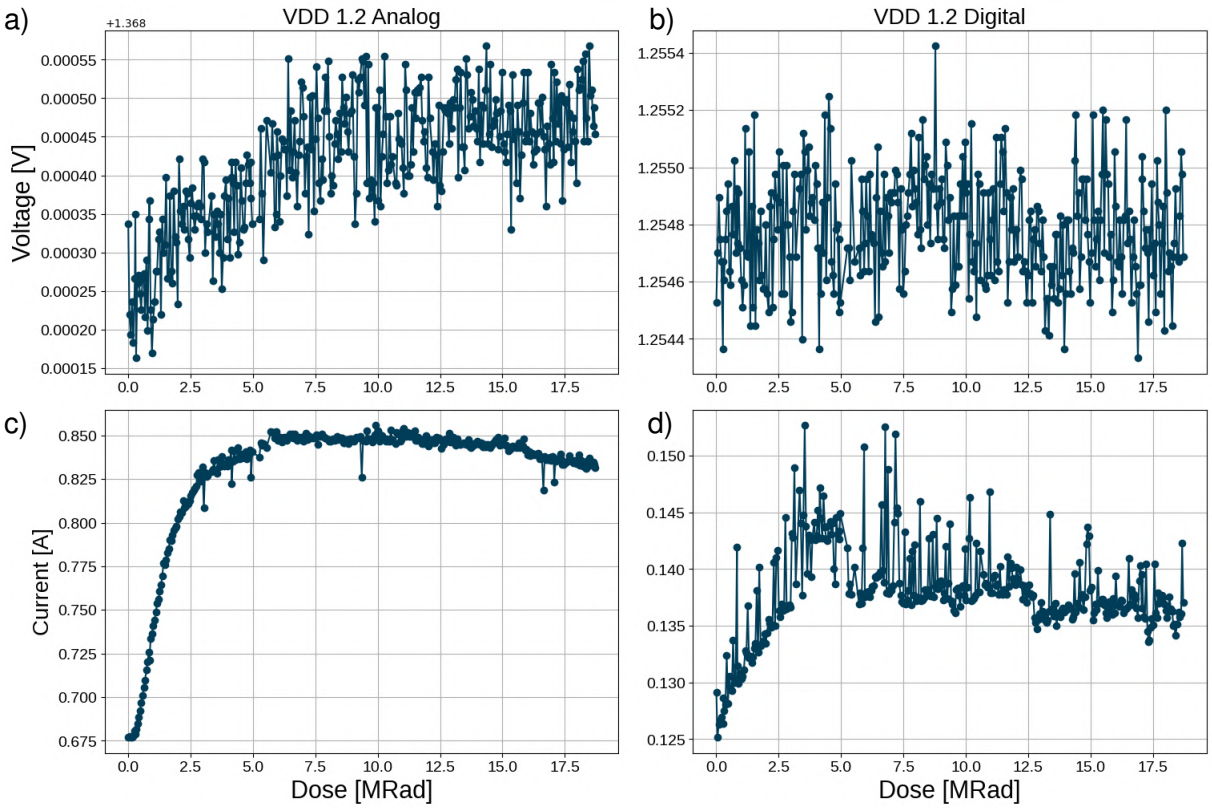

FIGURE 5.68 – *Power supplies measurements of HGCROC Si version after 19 Mrad accumulated dose. a) 1.2 VDDA voltage, b) 1.2 VDDD voltage, c) 1.2 VDDA current, d) 1.2 VDDD current.*

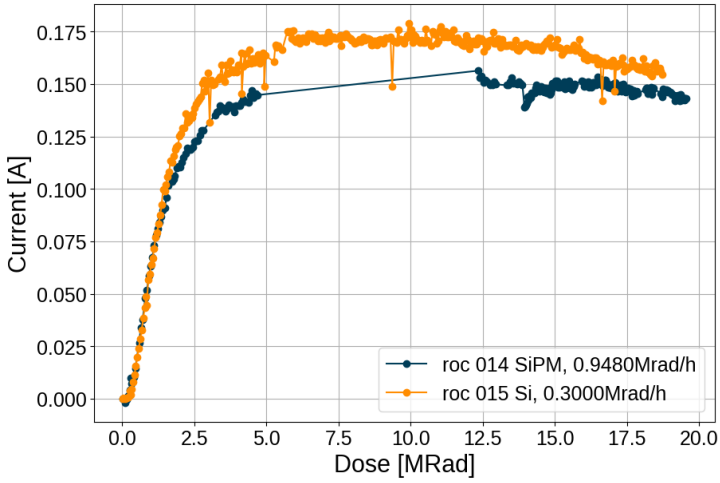

FIGURE 5.69 – *Analog current measurement comparison between H2GCROC and HGCROC for irradiation up to 19 Mrad.*

These test results led to continuing the tests at the Lab, finding that ASICs without irradiation present a leakage current when the analog part is not connected. The conclusion was to look for specific circuits with floating nodes. Finally, the problem was found inside the TDC design (Figure 5.71). The $EN\_ENCODER$ and HIT inputs must have opposite values ; this is configured by default or forced when a soft reset is activated or the TDC is deactivated. During

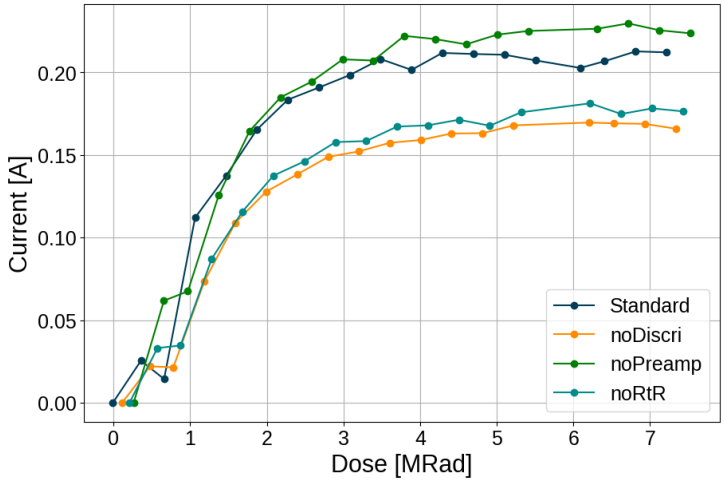

FIGURE 5.70 – *VDDA current variation after 7.5 Mrad of accumulated dose with different configurations disabling the different analog blocks of the front-end.*

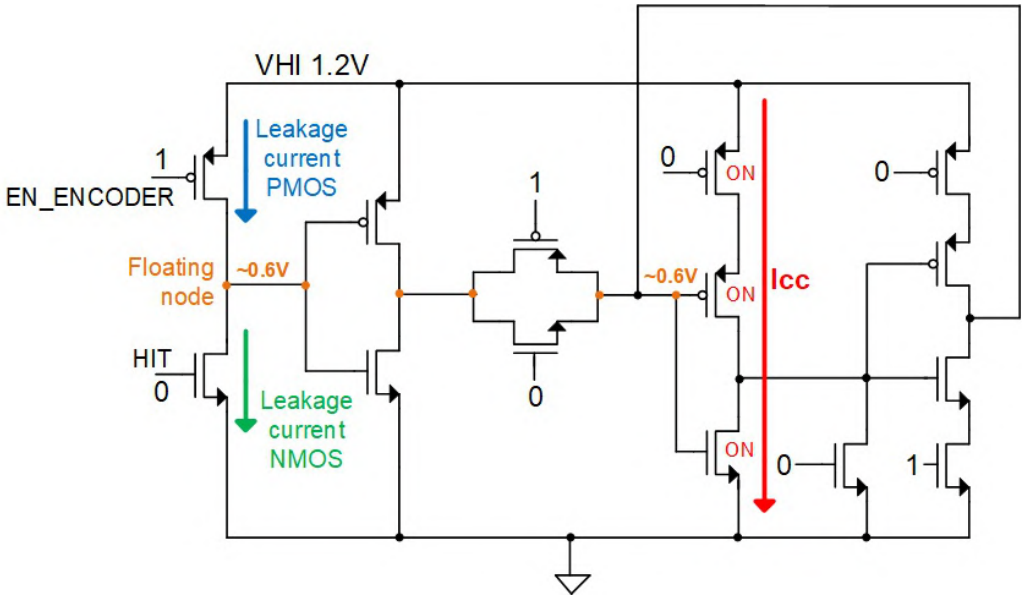

FIGURE 5.71 – *Schematic of a floating node inside the TDC design.*

irradiation, the leakage current of PMOS and NMOS of the inputs causes the floating node to be in the middle of VHI (1.2 V) and ground ($V_{floating\_node} = 0.6\ V$), activating both input transistors and creating a short circuit. This activation propagates and generates a high leakage current (I_{CC}) sensitive to irradiation. After 5 Mrad of irradiation, the total current increment corresponds to the sum of leakage currents generated in each structure with a floating node at the TDC multiplied by the 144 TDCs in every ASIC. After finding the problem, the circuit was corrected for the final version of the ASIC.

Following the H2GCROC ASIC test results, the pedestal of ADC and its rms noise is presented in Figure 5.72 using the Physics mode configuration on the chip. Although the 300 kRad level of irradiation is too low to affect the noise or performance of the chip considerably, the characterization of the ASIC studied a higher total accumulated dose (19.5 Mrad) that produced a small increment in the noise of the ADC and a slight decrement in the pedestal level of every ASIC channel (see Figure 5.73). This effect is expected in this technology at lower levels and

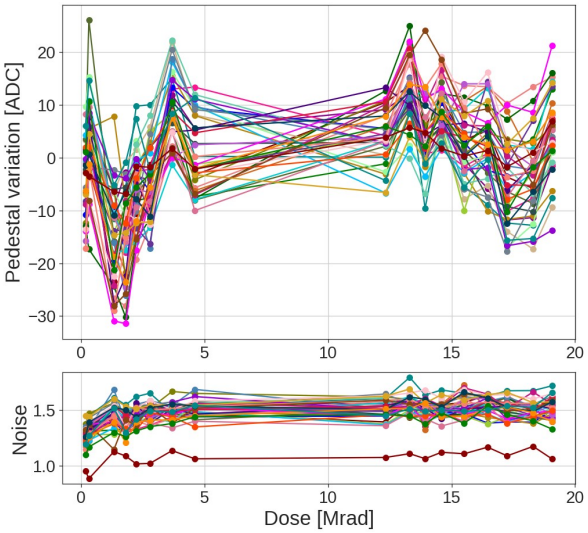

FIGURE 5.72 – *Pedestal variation of all channels of H2GCROC during irradiation up to 19 Mrad.*

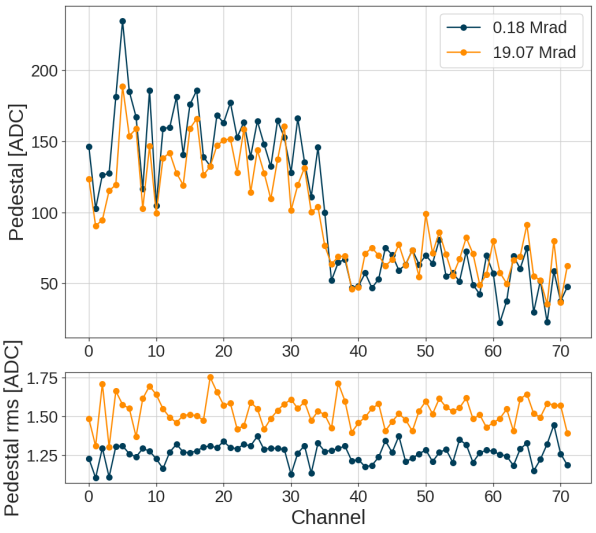

FIGURE 5.73 – *Measured pedestals of H2GCROC and its rms noise before and after irradiation up to 19 Mrad.*

may be reduced after the correction of the leakage current of VDDA on the next ASIC version.

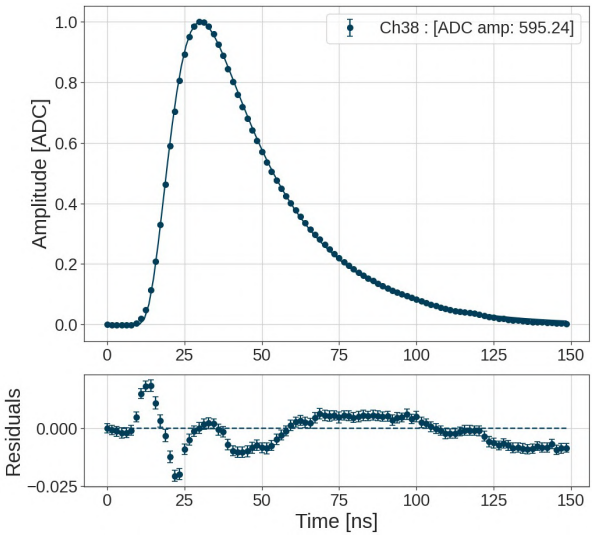

FIGURE 5.74 – *ADC scan through time before irradiation.*

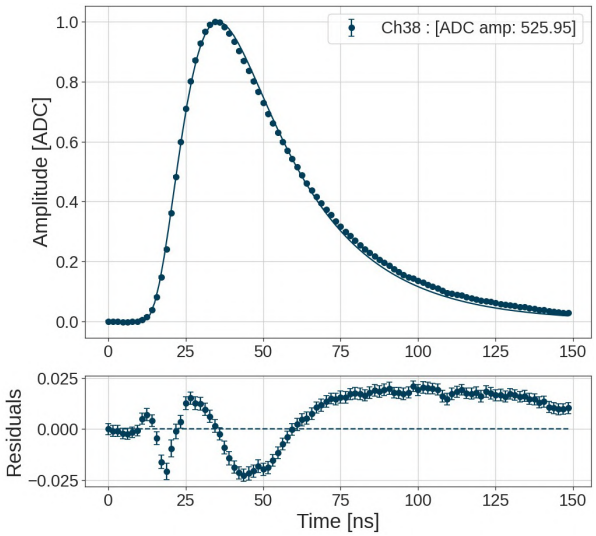

FIGURE 5.75 – *ADC scan through time after 19 Mrad of accumulated dose.*

Figures 5.74 and 5.75 present the ADC response for charge injection performance. The shape of the output maintains good stability after 19 Mrad of accumulated dose. However, Figure 5.76 presents a decrement in the amplitude of the charge measurement of around 100 ADC counts after 19 Mrad. This type of variation was also observed in the tests of the Si version of the chip (Figures 5.77 and 5.78). However, those ASICs exhibited a variation in amplitude of around 18 ADC counts after 345 Mrad. Therefore, the current conveyor gain configuration is more sensitive to irradiation and produces a higher range of variation than the Si version.

Studying the parameters of the ADC fit formula (see Equation 5.1), we can see in Figure 5.79 that the most affected parameter is the shaper characteristic time (τ_s) corresponding to the signal's decay time. The preamplifier characteristic time (Figure 5.80) has a more stable

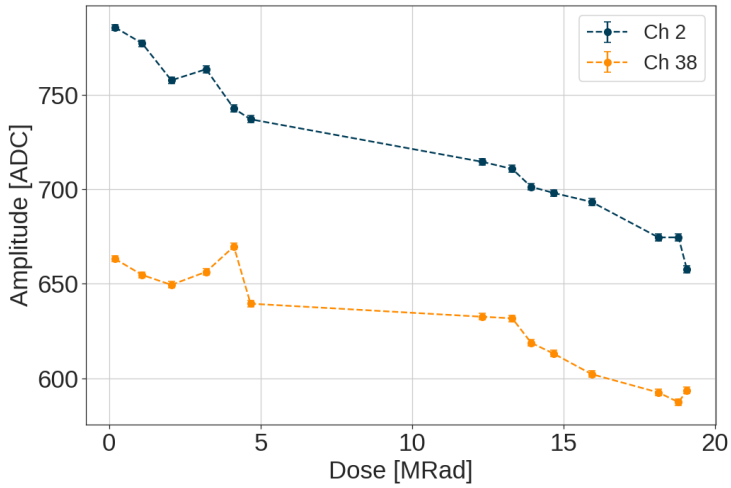

FIGURE 5.76 – *ADC amplitude decrement during irradiation up to 19 Mrad.*

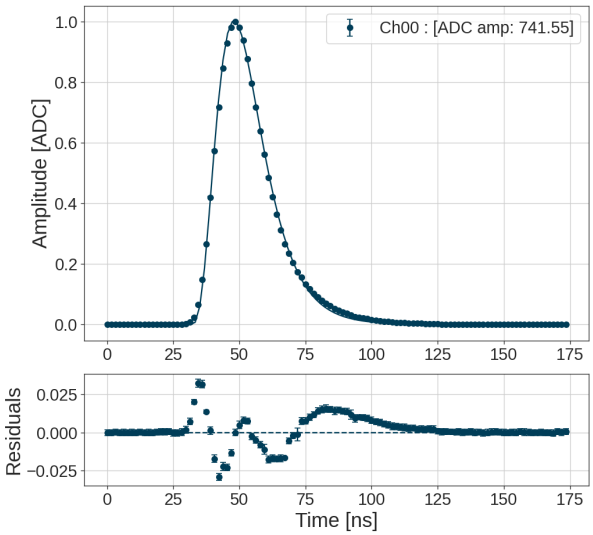

FIGURE 5.77 – *HGCROC Si-version ADC scan through time before irradiation.*

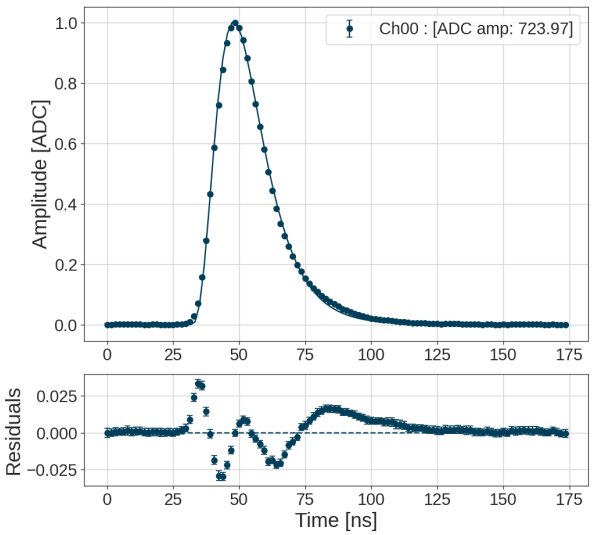

FIGURE 5.78 – *HGCROC Si-version ADC scan through time after 345 Mrad of accumulated dose.*

behavior.

From the charge injection scan measurements, Figures 5.81 and 5.82 present good linearity on the ADC measurements. The same effects seen before in pedestal and ADC shape analysis can be seen with the maximum charge read before saturation and the increment in rms noise.

Figures 5.83 and 5.84 demonstrate the stability of TOA time walk in a channel without detector capacitance. However, the same increment in the noise impacts the jitter that slightly increases.

The second TID campaign was performed at room temperature at the Asterix machine. It consisted of irradiating the chip without cooling at a low dose of 0.102 Mrad/h until reaching 1 Mrad and then changing to the maximum irradiation dose (0.392 Mrad/h). The PCB had a temperature of 33 ℃, and the temperature below the mezzanine was 44 ℃.

After continuous irradiation for 10 hours at 0.102 Mrad/h, the chip reached an accumulated dose of 1 Mrad. Subsequently, the test continued at the maximum dose rate for another 11

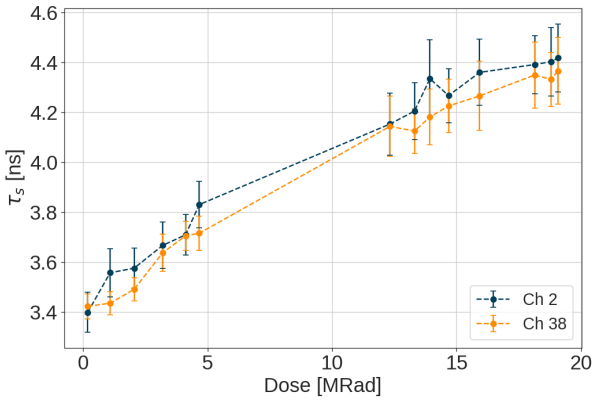

FIGURE 5.79 – *ADC τ_s response during irradiation up to 19 Mrad.*

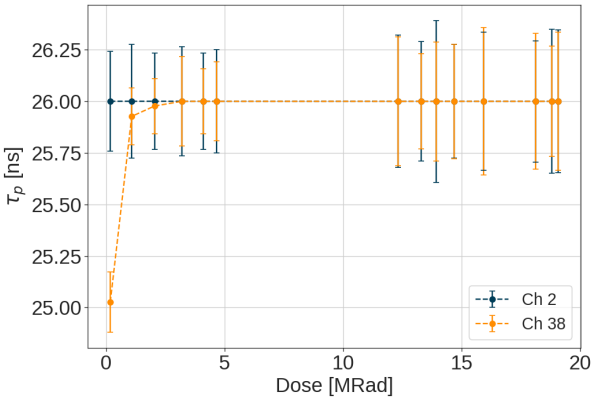

FIGURE 5.80 – *ADC τ_p response during irradiation up to 19 Mrad.*

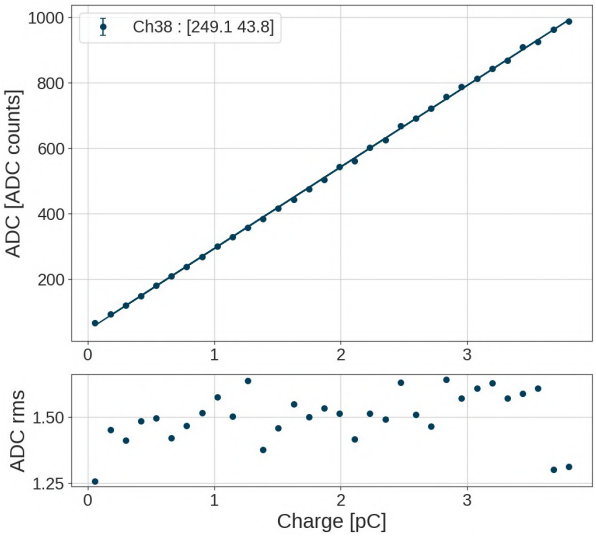

FIGURE 5.81 – *ADC response of charge injection scan before irradiation.*

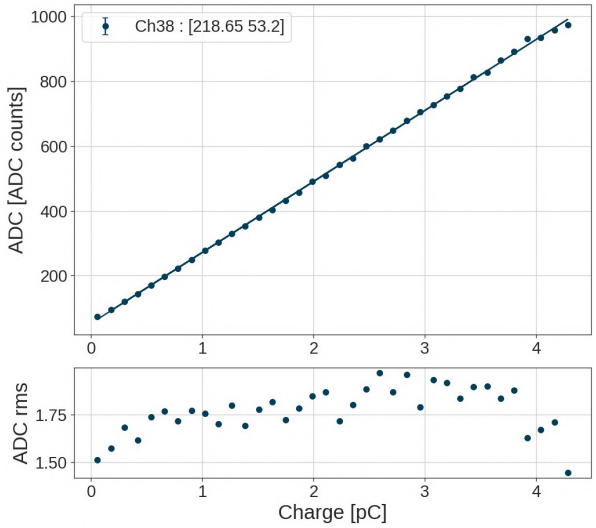

FIGURE 5.82 – *ADC response of charge injection scan after 19 Mrad of accumulated dose.*

hours to reach more than 5 Mrad, resulting in a total accumulated dose of 6.43 Mrad. Figure 5.85 presents measurements of the VDDA power sources. The same current peak is present in 2.5 V VDDA, but the current increment is noticeably reduced compared to the measurements at cold. Figure 5.85 c) illustrates a different slope in the current increment corresponding to the change in dose rate during the test after 1 Mrad irradiation at a low dose rate.

Figure 5.86 compares the irradiation measurements at cold for roc 014 and at room temperature for roc 029. Both current measurements exhibit the same shape, with a peak occurring at the same moment of irradiation dose. This indicates that cooler temperatures increase the sensitivity of electronics to irradiation effects. This effect arises because the ASIC at higher temperatures, generates a mechanism for discharging the particles trapped by radiation. One method to remove radiation damage is by increasing the temperature of sensors and chips, a process known as annealing, which occurs when the chip is polarized in a free radiation environment and is more efficient at higher temperatures. The expected working temperature of the ASIC at HGCAL (-30℃) will represent the more challenging scenario for radiation effects on the chip.

This second TID campaign included a stability analysis of the two main DACs in the ASIC.

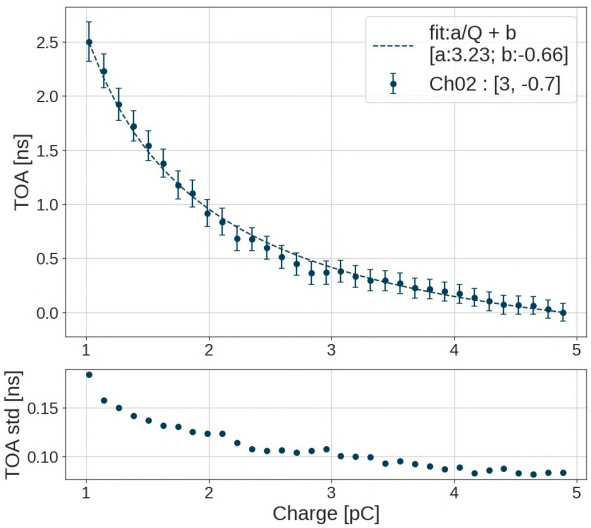

FIGURE 5.83 – *TOA time walk response of charge injection scan before irradiation.*

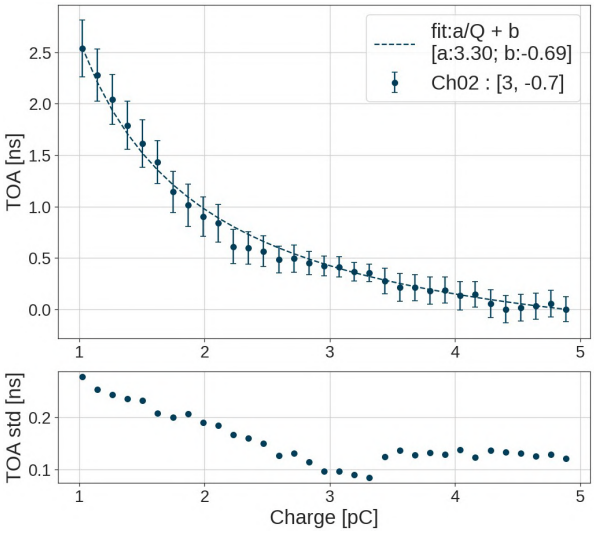

FIGURE 5.84 – *TOA time walk response of charge injection scan after 19 Mrad of accumulated dose.*

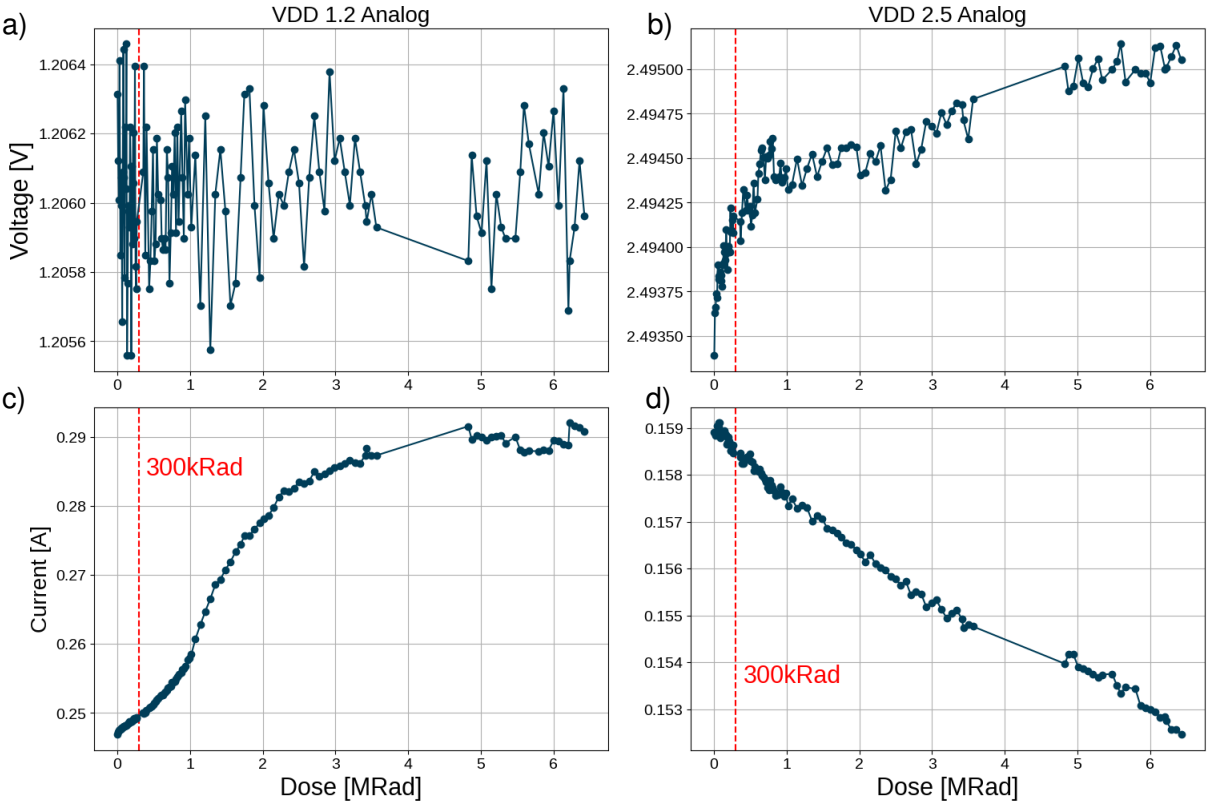

FIGURE 5.85 – *Power supplies measurements of H2GCROC after 6 Mrad accumulated dose at room temperature. a) 1.2 VDDA voltage, b) 2.5 VDDA voltage, c) 1.2 VDDA current, d) 2.5 VDDA current.*

Tests of other ASICs designed by OMEGA showed some damage after a small injection of irradiation in a few DACs with a similar design as the one used in H2GCROC. Therefore, it

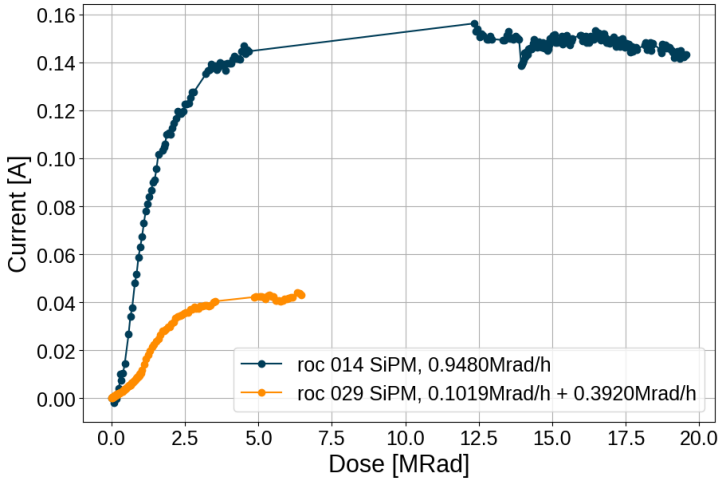

FIGURE 5.86 – *Power supplies measurements of H2GCROC at Cold temperature (-7 °C) for roc 014 and room temperature (33 °C) for roc 029.*

was necessary to test the chip at a low-dose injection to see the effects of the low irradiation dose. Figure 5.87 presents the variation of the 2.5 V DAC used for injection; it maintains its performance during the test with a slight decrement of 2.5 mV after 6.4 Mrad of accumulated dose.

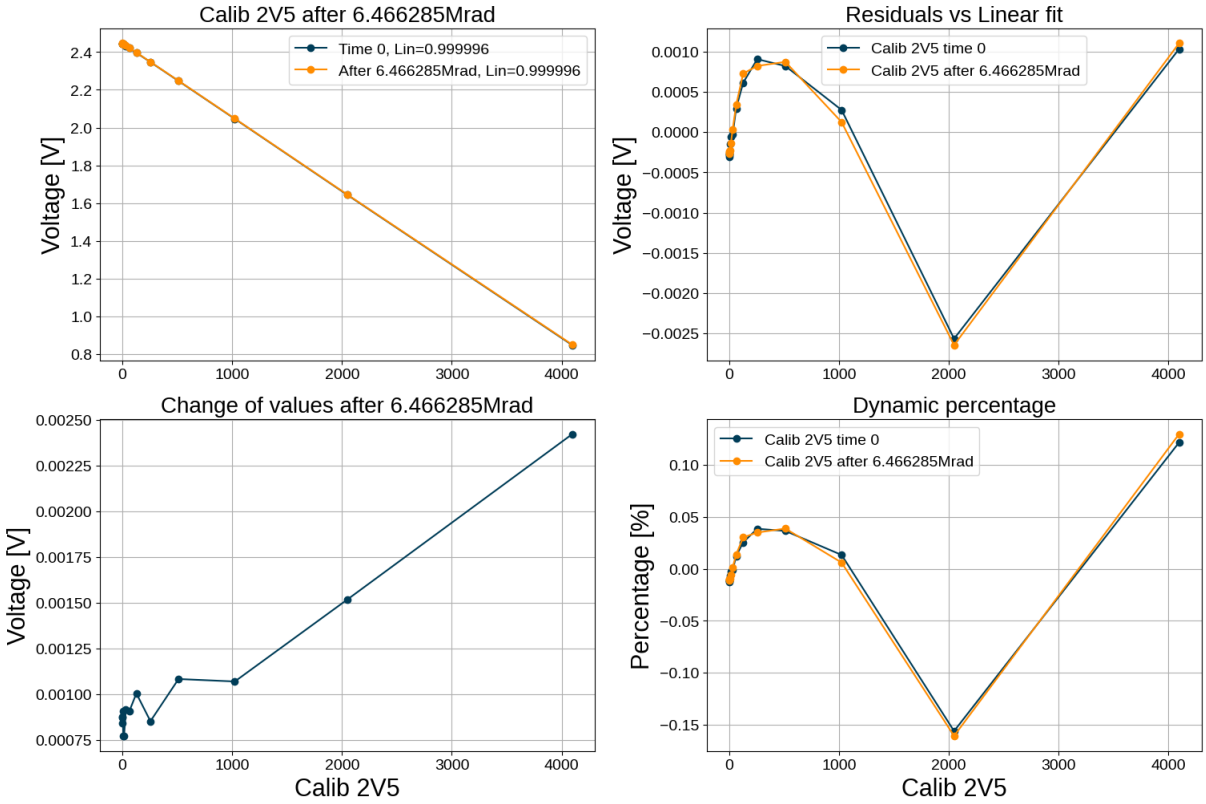

FIGURE 5.87 – *2.5 V DAC for charge injection stability after 6.4 Mrad.*

The performance of the $dacb$, used to compensate for the leakage current produced by irradiated SiPMs, is present in Figure 5.88 before and after 6.4 Mrad of irradiation. It has a

good linearity after the total irradiated dose, and contrary to the injection DAC, this DAC has a slight slope increment after 6.4 Mrad. The objective of the test was fulfilled since both DACs maintained their typical performance during the whole test duration and did not present damage at the first stages of irradiation, even with a slow dose rate. After researching the literature, we found in Faccio's analysis of the TSMC 130 nm technology [76] that the fabrication company influences the irradiation hardness of the fabricated chip. That research tested three samples manufactured in different plants. One of the three presented significant leakage current at low irradiation doses, while the rest did not have these problems. We concluded that the errors seen in the other similar DACs are present due to the influence of the fabrication company selected, even in the same technology. For the H2GCROC ASIC, the only effect present in DACs is illustrated in Figure 5.89. The $dacb$ slope variation spreads between channels for higher accumulated irradiation doses.

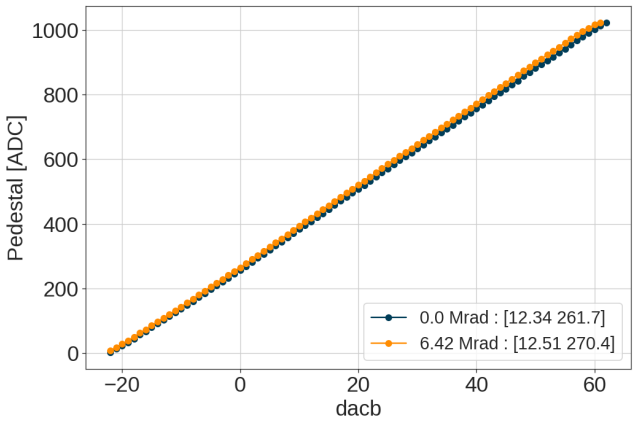

FIGURE 5.88 – *ADC pedestal measurement in a $dacb$ scan for irradiation up to 6 Mrad using the Physics mode configuration on H2GCROC.*

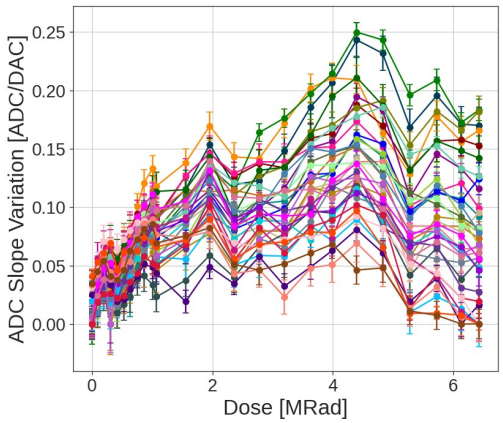

FIGURE 5.89 – *$dacb$ slope variation for irradiation up to 6 Mrad using the Physics mode configuration on H2GCROC.*

Each ASIC channel has dedicated DACs to perform pedestal compensation between channels. In the first TID campaign, these 6-bit DACs were configured at their default value of 0. In the regular operation of HGCAL, these DACs are expected to be configured to their middle value ($input\_dac = 31$) to compensate for reductions and increases in the DC level of each channel. The second TID campaign used a configuration where every $input\_dac$ was set to 31 to determine if they could produce a constant voltage throughout the applied irradiation dose. The stable charge and time measurements indicate that the $input\_dac$ maintains its behavior after irradiation.

The last thing to analyze in the second TID campaign was the performance of the ASIC under irradiation using the Calibration and Physics mode. The pedestal and rms noise from the ADC measurements are presented in Figures 5.90 and 5.91 for the Physics and Calibration configurations, respectively. Although the 300 kRad level of irradiation does not affect the noise considerably, the total accumulated dose produces a small increment in noise in both configurations. The increment in noise is slightly more significant in the Calibration mode due to the gain configured. The Physics mode attenuates the current at the input three times more than the Calibration mode and mitigates the irradiation effects on the electronics.

Both tests concluded that the H2GCROC is a radiation-hard ASIC capable of maintaining its typical behavior up to 300 kRad, corresponding to the total expected operation time of HGCAL. It exhibits an increase in noise and a reduction in ADC amplitude with radiation exposure up to 20 Mrad, which should be considered if the ASIC is exposed to higher accumulated doses.

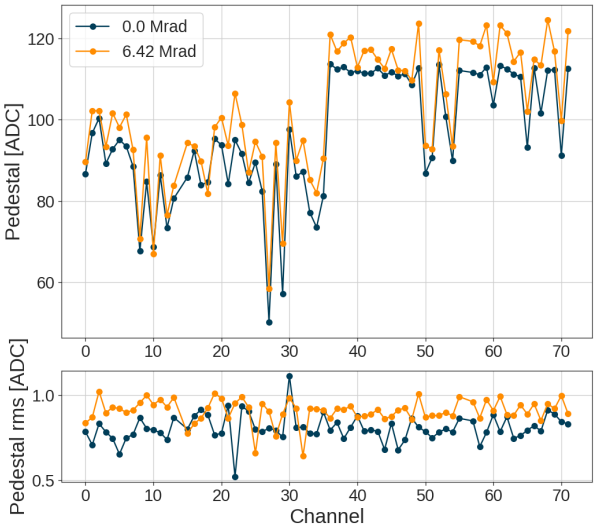

FIGURE 5.90 – *Pedestal and rms noise from ADC measurement before irradiation and after irradiation, using the Physics mode configuration of the ASIC.*

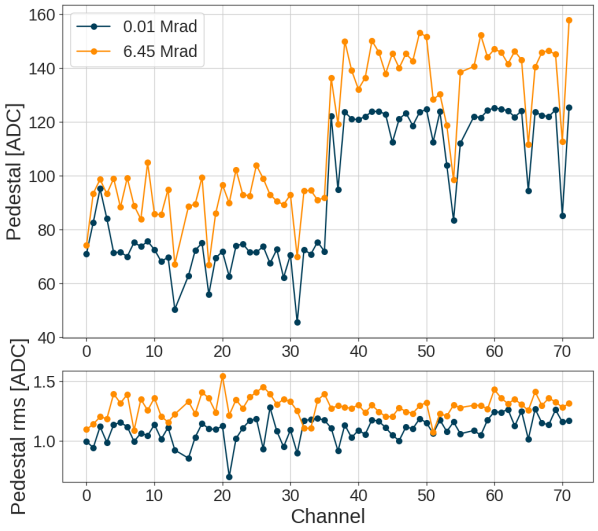

FIGURE 5.91 – *Pedestal and rms noise from ADC measurement before irradiation and after irradiation, using the Calibration mode configuration of the ASIC.*

However, after a few days of annealing, the chip recovered its normal functionality.

5.7.3 SEE Setup

Heavy-ion tests were conducted using the UCL cyclotron in Louvain, Belgium (Figure 5.92), and proton injections were performed at Arronax in Nantes, France (Figure 5.93) for Single Event Effects (SEE) damage analysis. As mentioned in Chapter 4, the only differences between the Si and SiPM versions of the ASIC are in the front-end analog part of the chip. Therefore, it was determined that testing SEE only for the Si version would save time and serve as a good indicator of the expected behavior for the SiPM version of the chip. These tests included evaluating front-end performance, similar to the Total Ionizing Dose (TID) campaigns, including measuring reference voltages. However, a new test was introduced to evaluate the performance of the PLL of the chip and the impact of SEE on it.

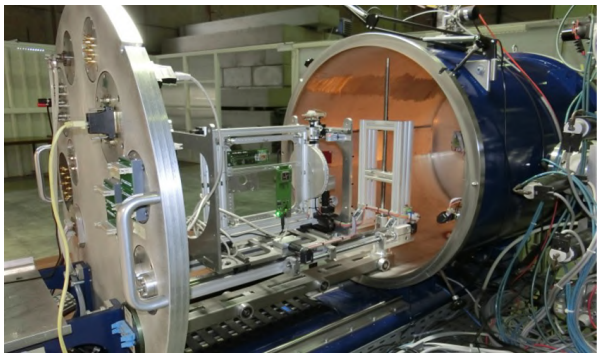

FIGURE 5.92 – *Heavy Ion Facility (HIF) of the Cyclotron Resources Centre of UCL in Louvain, Belgium [77].*

FIGURE 5.93 – *Cyclotron C70 at Arronax in Nantes [78].*

The SEE analysis was performed with the injection of heavy ions and protons. The ASIC

performance was checked in I²C, Data Acquisition (DAQ) and PLL tests. The I²C test checks the static registers of the chip configuration containing 2573 parameters in 8956 bits. The I²C parameters are constantly compared with the first set of parameters configured in the chip. The known use of triplication helps reduce errors produced by SEE. Therefore, the same analysis was made with the triplication circuits enabled or not. The DAQ test consisted of reading a fixed data pattern that typically contains each channel's charge and time information (see Figure 4.14). The output data was constantly compared with the expected pattern to check for bit flips. The chip data is processed with Hamming encoding that can correct if a 1-bit flip happens, and if 2-bit flips happen, it stores a corruption flag. The PLL test checked the frequency provided. In the case of a Single Event Transient (SET), the frequency is changed and induces a link misalignment. It can happen in two ways : as a short SET when the data transmission fails for just one bit. This kind of SET can be detected when the CRC fails. Alternatively, as a long SET, the data transmission is constantly shifted when there is a link loss. In this case, the Header pattern is not recognized, and it is necessary to do a link reset.

In summary, seven types of errors of the ASIC were tested during irradiation :

— **I²C** : Bit flips in the ASIC configuration parameters.
— **Counters** : Digital-type error when there is a bit flip in the counters of the DAQ path header.
— **Trigger (TRIG)** : Digital-type error causing errors in the trigger path.
— **Cyclic Redundancy Check (CRC)** : Digital-type error in the sum of all channels of the DAQ path.
— **Memory (MEM)** : Digital-type error in the ASIC memory.
— **Short SET** : Analog-type data transmission error.
— **Long SET** : Analog-type data transmission error requiring a link reset.

5.7.4 Single Event Effect Campaigns

The first campaign involved the injection of Heavy Ions from the UCL cyclotron's Heavy Ion Facility (HIF). This cyclotron can inject a variety of ions with an energy of 9.3 MeV per nucleon to cover a large Linear Energy Transfer (LET) range for the material under irradiation. The irradiations were conducted inside a vacuum chamber. This beam can produce the particles presented in Table 5.2. It includes the M/Q (mass-to-charge ratio), Energy in MeV, the LET and the range, indicating the distance the ion travels in the material before losing its energy.

Ion	M/Q	Energy [MeV]	Range [μm]	LET [$MeV/(mg/cm^2)$]
$^{22}Ne^{7+}$	3.14	238	202	3.3
$^{27}Al^{8+}$	3.37	250	131.2	5.7
$^{36}Ar^{11+}$	3.27	353	114	9.9
$^{53}Cr^{16+}$	3.31	505	105.5	16.1
$^{58}Ni^{18+}$	3.22	582	100.5	20.4
$^{84}Kr^{25+}$	3.35	769	94.2	32.4
$^{124}Xe^{35+}$	3.54	995	73.1	62.5

TABLE 5.2 – *Available particles at the UCL cyclotron in Louvain and its characteristics.*

Figure 5.94 illustrates the first test setup with one HGCROC Si-version placed in a mezzanine and controlled by a ZYNQ Hexacontroller. A cooling system cools down the ASIC, achieving a temperature of 7.2 °C close to the chip. The flux of particles available was 10^4 particles/(s· cm²). Table 5.3 shows the results of heavy ion injection and the number of errors

produced with and without triplication activated. As expected, the triplication technique can correct the data and eliminate errors in the triplicated parts. However, the number of short and long sets in the non-triplicated part is not negligible.

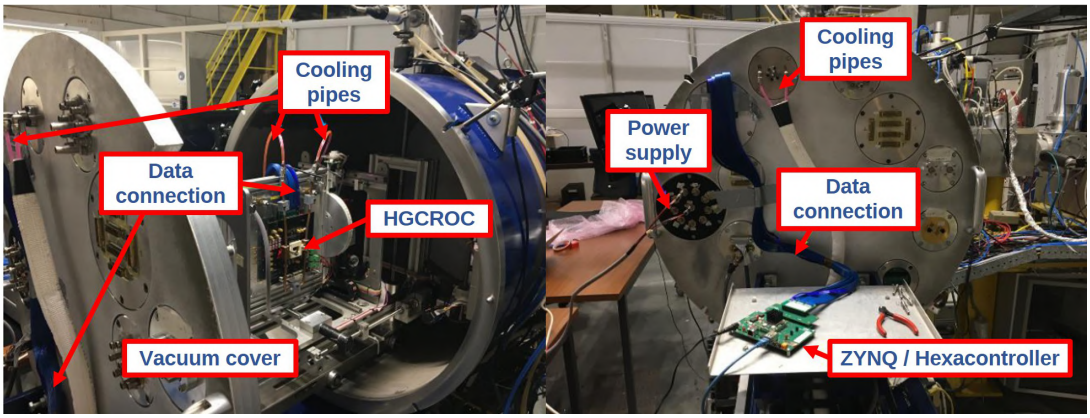

FIGURE 5.94 – *Irradiation chamber from the UCL cyclotron in Louvain, Belgium [79].*

Ion	Time [s]	I²C	Counters	TRIG	CRC	MEM	Short SET	Long SET	Time TR [s]	Errors
Ne	1512	55	-	-	-	-	-	-	1515	-
Al	932	213	-	-	1	-	-	-	1291	-
Ar	934	316	-	1	1	-	1	-	1184	-
Cr	873	559	-	-	-	1	3	1	879	-
Ni	911	662	-	-	-	2	8	2	1289	-
Kr	457	502	-	-	-	-	5	13	661	-
Xe	128	130	-	-	-	-	1	8	127	-
# of errors :		2437	0	1	2	3	18	24	-	0

TABLE 5.3 – *Errors during SEE tests at the UCL cyclotron in Louvain, Belgium (TR = Triplicate mode active) [79].*

The HGCAL radiation environment will be dominated by light hadrons (protons and neutrons). The difference from heavy ions is that protons produce hadronic interactions in the silicon substrate and generate a nuclear recoil ; the charged silicon recoil induces ionization, and the charge collection temporarily modifies the circuit. Heavy ions can simulate this ionization but with a larger energy deposit. Figure 5.95 illustrates this effect, where protons produce ionization within a range of less than 10 μm, contrary to a more extensive range of ionization produced by heavy ions. Depending on the sensitive volume, this damage can affect the digital or analog electronics ; for digital electronics, fast large signals can produce a bit flip (SEU). All signals can affect analog electronics, but larger signals produce more significant damage that can lead to a bit shift. The heavy ions test is reliable for the digital part of the ASIC but too pessimistic for the analog part.

Therefore, a second campaign of SEE was necessary, this time with proton injection, to test the PLL performance. Figure 5.96 illustrates the setup of the HGCROC ASIC at the Arronax facilities. This cyclotron can inject 30 to 70 MeV protons with a flux of particles of $2.2 \cdot 10^{10}$ $s^{-1} \cdot cm^{-2}$). The test was performed for 13 hours, corresponding to the fluence expected in 10 years at the HL-LHC.

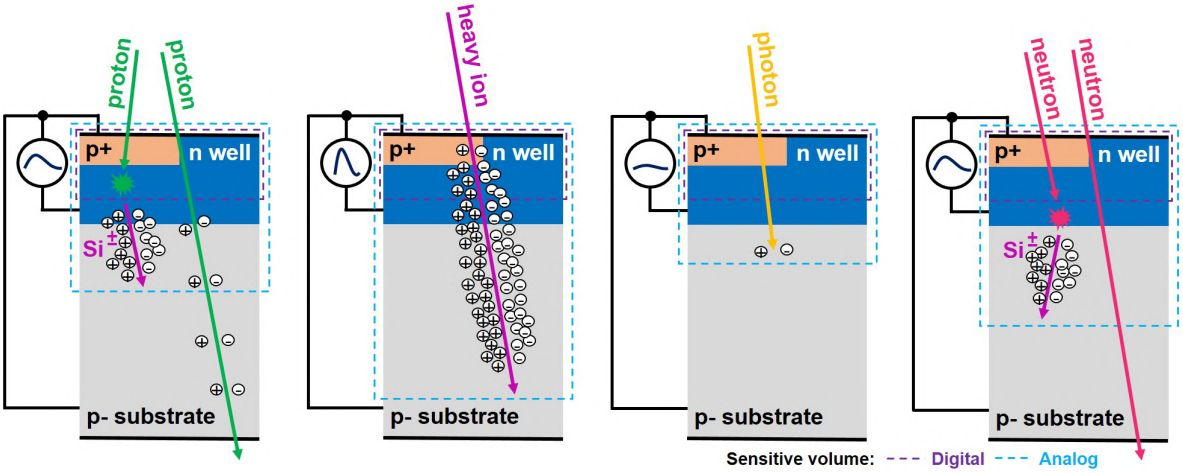

FIGURE 5.95 – *Ionisation of the substrate difference for different particles and the sensitive volume for digital or analog electronics [80].*

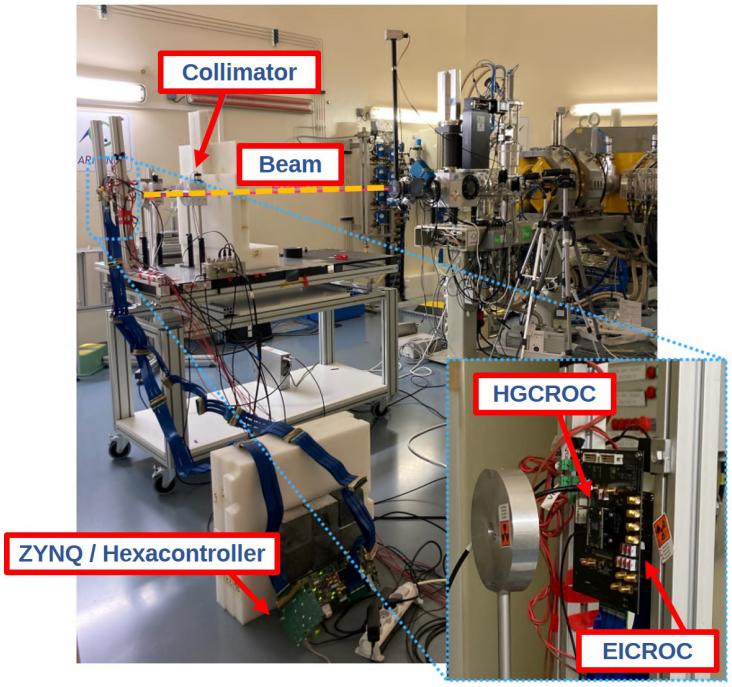

FIGURE 5.96 – *Irradiation setup at Arronax in Nantes, France [80].*

The test results are presented in Table 5.4. The number of SEE events was also present with proton injection, significantly affecting the short and long SETs from link misalignment in the PLL. An analysis of the number of errors, the fluence injected and the test time allows for extrapolating the expected number of errors during the lifetime of HGCAL. This number of errors corresponds to a link loss every 2.5 years in each HGCROC, equivalent to a link loss every 2 minutes in HGCAL.

Together with HGCROC, Figure 5.96 shows that the ASIC EICROC was also present in the tests at Arronax. This ASIC has a new triplicated version of the PLL. The triplication in this new PLL version avoided most link losses due to Long SET. Consequently, the EICROC tests pointed to improving the amount of triplicated blocks in the PLL of HGCROC. These

	Counters	TRIG	CRC	MEM	Short SET	Long SET
# of errors	-	38	30	127	85	190

TABLE 5.4 – *Errors during SEE tests at Arronax in Nantes, France [80].*

corrections will also be included in the last version of the chip HGCROCv3b and also for the SiPM version H2GCROCv3b. For the data path of the ASIC, good results are achieved thanks to the Hamming structure that can correct errors not solved by the triplication technique.

5.7.5 SiPM irradiation effects

The hadronic calorimeter anticipates different irradiation levels on its front and back sides. This difference motivated the selection of SiPM detectors, which have larger gains than Silicon sensors and reduced costs, in the back part of the calorimeter. However, SiPMs are less radiation-tolerant. The leakage current produced by irradiated SiPMs is in the range of mA, a significant increment compared to the expected leakage current from Silicon sensors (50 μA).

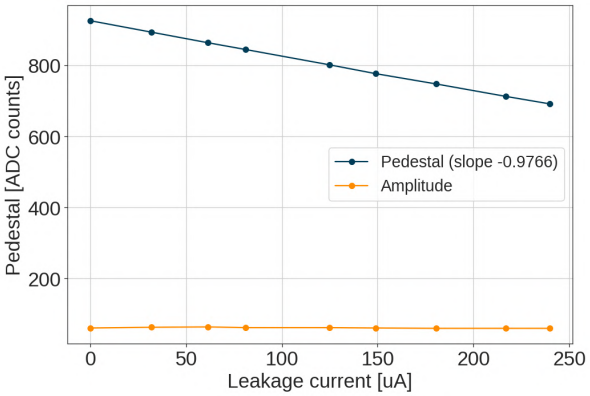

FIGURE 5.97 – *ADC pedestal and amplitude for a 1 pC charge injection for different leakage currents at the input of one ASIC channel using the Physics configuration of the ASIC.*

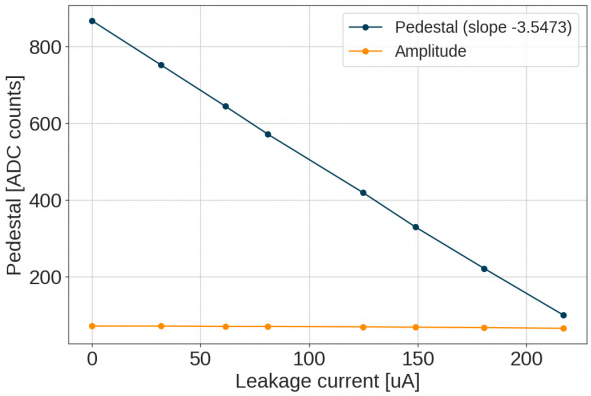

FIGURE 5.98 – *ADC pedestal and amplitude for a 1 pC charge injection for different leakage currents at the input of one ASIC channel using the Calibration configuration of the ASIC.*

The leakage current compensation of H2GCROC was characterized by injecting external currents to simulate the irradiation damage from SiPMs. One resistor was connected from a voltage source to one channel input to inject the additional current. Different resistor values produce external current injection of different values. The test consisted of injecting different values of leakage current while maintaining a constant charge injection on that channel. Figure 5.97 presents the ADC measurement for different leakage currents injected externally at the channel's input using the Physics configuration of the chip. This artificial leakage current alters the channel's pedestal but leaves the amplitude of the ADC response unaffected. If we use the Calibration configuration of the ASIC, the current attenuation of the current conveyor is less, and therefore, the leakage current is less attenuated. Figure 5.98 presents the ADC measurement for different leakage currents injected externally at the channel's input using the Calibration configuration of the chip. We can see that now the current going to the input channels is higher, and therefore, the $dacb$ will be able to compensate for less leakage current.

The ASIC needs to counterbalance the leakage current from irradiated SiPMs by injecting supplementary current in the opposite direction of the leakage current. Figure 5.99 shows a

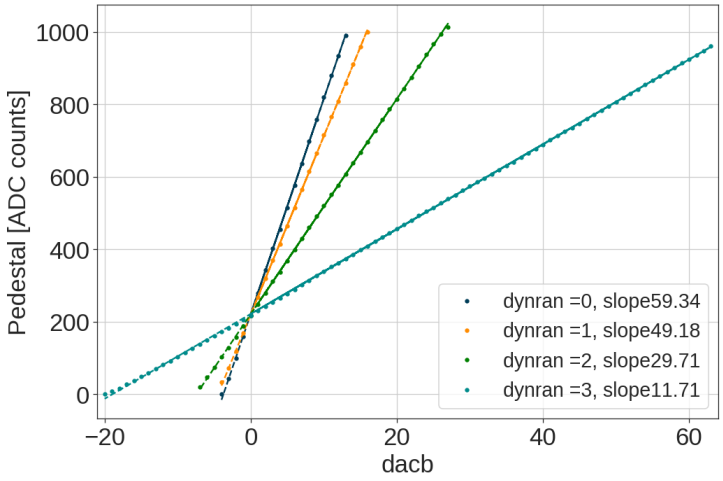

FIGURE 5.99 – $dacb$ *correction range for the different dynamic range configurations.*

$dacb$ scan enclosing the four dynamic range configurations for $dacb$ current injection. With one bit to adjust the current's direction, the ASIC can compensate for the leakage current with 128-bit values. The slope of $dacb$ measurements can be used to calculate the maximum leakage compensation. As discussed in Section 4.5.5, this compensation depends on the attenuation of the current conveyor that will also attenuate the leakage current coming from the SiPM. Table 5.5 presents the equivalence from the $dacb$ slopes to leakage current compensation corresponding to a maximum of 1.5 mA of compensation using the Physics configuration.

Dacb_dynran_config	$dacb$ slope	$dacb$ step	Max $dacb$ current	Leakage current correction range
0	59.34	7 μA	126 μA	0 to 1.5 mA
1	49.18	4.9 μA	104 μA	0 to 1.26 mA
2	29.71	1.7 μA	62 μA	0 to 765 μA
3	11.71	0.3 μA	24 μA	0 to 310 μA

TABLE 5.5 – *Leakage current correction range measured using the Physics configuration of H2GCROCv3.*

5.8 Power consumption and robustness of the chip

HGCAL will be an enormous detector with millions of sensors, each connected to one ASIC readout channel. The energy needed to power the detector will be significant, so it is crucial to minimize power consumption. The ASIC consumption varies with the activation of different blocks. When the ASIC is powered on, it operates in low-power mode to reduce energy consumption when not in use. For regular operation, it transitions to a different configuration that increases the ASIC's consumption. In this regular mode, some electronic blocks initiate normal behavior and readings. However, other blocks, like the TDCs, require a trigger event to start their functionality. Despite the massive number of collisions expected at HGCAL, it is less likely to have every channel triggered by a particle simultaneously.

Table 5.6 presents the power measured with different modes. It used two different configuration modes : one with the lowest current conveyor attenuation possible (CC gain = 15) and

CC gain	Configuration	Analog 1.2 V		Analog 2.5 V		Digital 1.2 V	
		[mA]	[mW]	[mA]	[mW]	[mA]	[mW]
15	Low Power mode	104.3	125.16	27.9	67.24	112.7	135.24
	Default	353.2	423.84	136.8	329.69	123	147.6
	vbi_pa = 48	356.3	427.56	116.8	281.49	125.9	151.08
	vbi_pa = 63	356.5	427.8	94.8	228.47	127	152.4
	10 chan with TOA	357	428.4	136.6	329.21	124.8	149.76
	all chan with TOA	359	430.8	136.5	328.97	126.3	151.56
2	Default	376	451.2	128.6	309.93	135.3	162.36
	vbi_pa = 48	374	448.8	108.9	262.45	134.5	161.4
	vbi_pa = 63	366.5	439.8	87.3	210.39	135.4	162.48
	10 chan with TOA	375.2	450.24	128.6	309.93	135.3	162.36
	all chan with TOA	376.2	451.44	128.8	310.41	131.1	157.32

TABLE 5.6 – *Power consumption measured for VDDA 1.2 V, VDDA 2.5 V and VDDD 1.2 V on H2GCROC version 3.*

	Test characteristics [V]			Measurements after take pedestals [mA]			
Event	**VDDD**	**2.5 VDDA**	**1.2 VDDA**	**DI**	**2.5 AI**	**1.2 AI**	**Comments**
1	1.2	2.5	1.2	128	142	358	-
2	1.3	2.5	1.2	144	142	359	-
3	1.2	2.6	1.2	131	145	357	-
4	1.2	2.5	1.3	128	142	375	-
5	1.3	2.6	1.3	142	145	377	-
6	1.1	2.5	1.2	114	142	357	-
7	1.2	2.4	1.2	128	139	359	-
8	1.2	2.5	1.1	128	137	335	-
9	1.1	2.4	1.1	113	134	336	-
10	off	2.5	1.2	0	0.17	0.07	Need to restart the ZYNQ
11	1.2	off	1.2	0.092	0	315	-
12	1.2	2.5	off	0.044	0.036	0	-
13	off	off	1.2	0	0	0.058	Need to restart the ZYNQ
14	off	2.5	off	0	0.02	0	Need to restart the ZYNQ
15	1.2	off	off	0.044	0	0	-

TABLE 5.7 – *Scenarios tested to prove the robustness of the H2GCROCv3 ASIC.*

one with 0.05 attenuation (CC gain = 2). The lowest attenuation has a total consumption of 12.65 mW/channel when every TOA TDC is active. On the contrary, the 0.05 current conveyor attenuation consumes 12.76 mW/channel in the same scenario. Both results are below the specifications of 15 mW/channel.

Moreover, a test of the robustness of the chip was performed to ensure that the chip will maintain standard functionality even if it encounters voltage increments, drops, or parts of its blocks become powered off. Table 5.7 presents the different events tested with the voltage se-

lected for each ASIC power source. The current produced by the ASIC was measured with different configurations, and a general test of every functionality was performed. Every functionality of the ASIC worked with the different variations of power supplies when all of them were active. Half of the time, the chip recovered its functionality after reconnecting the power for the cases with one or more power supplies turned off. However, in three events, it was necessary to restart the ZYNQ, and after the reconnection, the chip recovered its functionality.

5.9 Conclusion

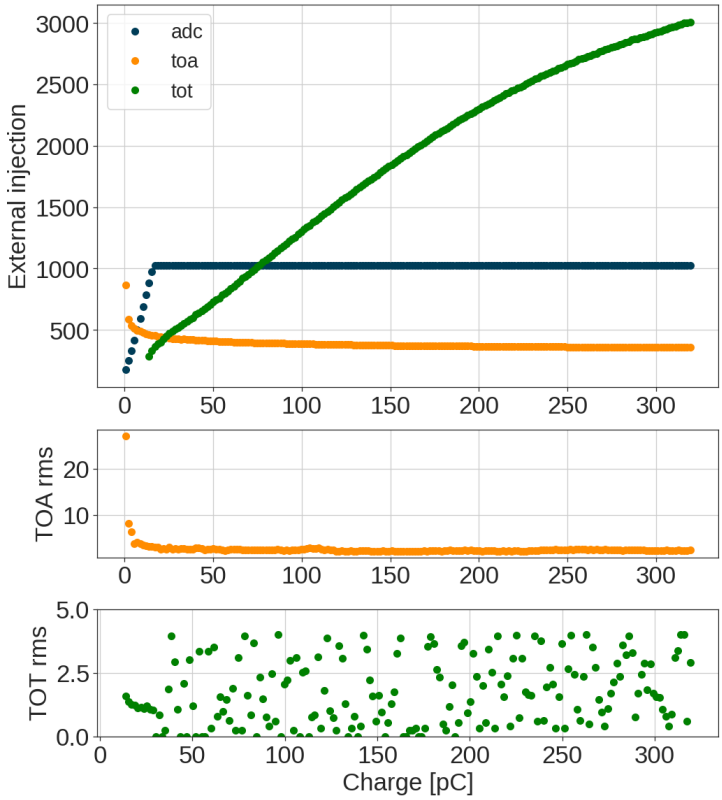

FIGURE 5.100 – *H2GCROC3 external charge injection response for up to 320 pC using a voltage generator and a 33 pF capacitor for charge injection and a C_{det} of 120 pF that corresponds to a 2 mm² SiPM. TOA unit = 25 ps, TOT unit = 50 ps.*

The H2GCROC ASIC has demonstrated its capability to meet the requirements of the HGCAL experiment. However, a few modifications will be necessary for the upcoming and final version of the ASIC (v3b). The chip's characterization confirmed its strong performance within the range required for the HGCAL experiment, and any deviations arising from parasitic and technological design factors remained within acceptable limits according to the HGCAL requirements.

Figure 5.100 summarizes the charge and time measurements. The chip can read charges from 160 fC to 320 pC. The calibration circuits within the chip enable the reading of single-photon spectra using the calibration configuration while compensating for variations between channels. Considering the operating environment of the experiment, the ASIC proved to be able to operate effectively at temperatures as low as -30 ℃ and exhibit radiation resistance of 300 kRad. Regarding time measurements, the resolution was less than 100 ps. The time

walk of the 9 mm² SiPM was close to the 25 ns limit ; therefore, the next and last version of the ASIC will include the ability to set a different phase for the ADC and TDCs simultaneously. This technique will prevent data from being assigned to the previous bunch crossing and reduce the time walk.

The next chapter will study the performance of the ASIC under beam tests and compare its performance with simulations and requirements in detail.

Chapter 6

ASIC Validation and Verification

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6.1 Introduction

As mentioned in Section 2.6, the ASIC will read the signal responses of the SiPM from various particles interacting with the hadron calorimeter. Chapters 4 and 5 analyzed the chip's performance with different SiPMs in simulation and under light injection conditions. However, the Test Beam offers an environment closer to what will be encountered in HGCAL. This chapter presents the results of the test beam conducted with H2GCROCv3, comparisons with expectations from requirements and an analysis of the ASIC's performance relative to the state-of-the-art in SiPM ASIC readouts.

6.2 Performance of the ASIC with electron injection from test beam

Tests conducted at an accelerator facility provide an opportunity to analyze the ASIC performance in a more realistic environment, allowing reading of the signals produced by particles absorbed by the SiPM-on-tile. Several test beams were carried out for both versions of the HGCROC ASIC at DESY and CERN. This dissertation focuses on presenting and analyzing the data from the DESY test beams, as their experiments are specifically tailored to the H2GCROC ASIC.

A contribution of this thesis involves actively participating in test beams for both ASIC versions at CERN and DESY. Additionally, communication was maintained with the DESY team for test beams that could not be attended to in person. The measurements leading to the results in this Section were conducted at the Test Beam Facility at DESY Hamburg, Germany, a Helmholtz Association (HGF) member.

6.2.1 Setup

The beam test took place at the DESY campus in Hamburg, Bahrenfeld. DESY II, the electron-positron synchrotron, generates electron or positron beams by directing them through carbon fiber targets (Figure 6.1). These beams comprised up to 1000 particles per cm² with energies ranging from 1 to 6 GeV. The energy spread was approximately 5%, and the divergence was around 1 Mrad.

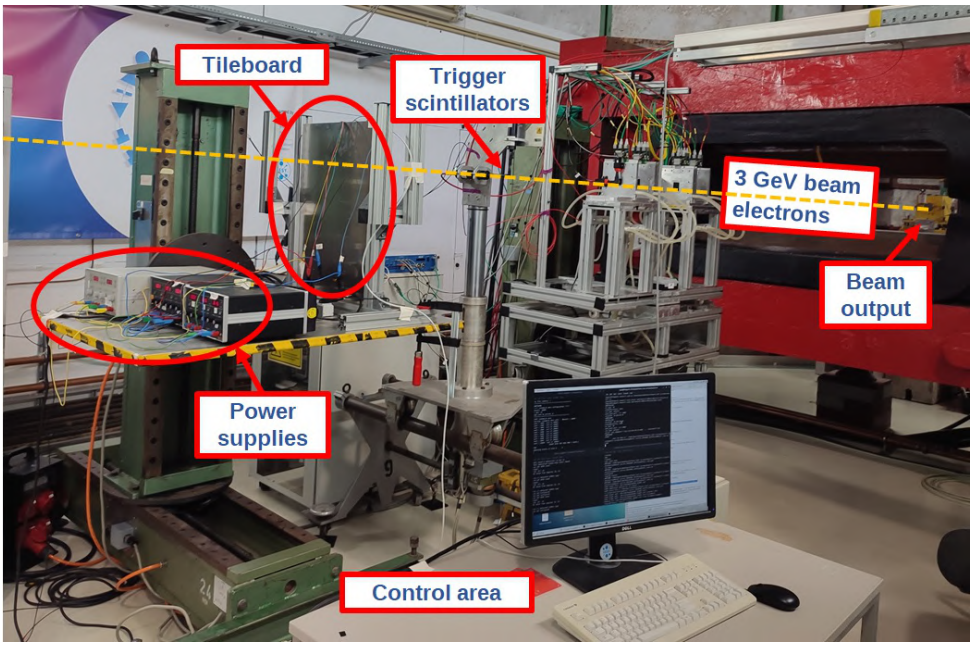

FIGURE 6.1 – *DESY test beam area setup of one Tileboard TB3.*

The initial beam test using the third fabricated version of the chip was conducted with an energy of 3 GeV. This test involved the injection of particles into two types of Tileboards :

— **Tileboard version 3 (TB3) :** A 64 SiPM board equipped with one H2GCROC ASIC, fully equipped with 4 mm² SiPMs and scintillator tiles in every detector without holes or components requiring a specific version of the scintillator tile. Two such boards were available (TB3-1 and TB3-2), configured with the same SiPMs and scintillators.

— **Mini Tileboard (MiniTB) :** A smaller PCB version with six connected SiPMs, featuring two of each size (2 mm², 4 mm² and 9 mm²) intended for use in the HGCAL project. The MiniTB can be fitted with scintillator tiles on two SiPMs simultaneously.

During the beam test, three different types of tests were executed :

— **TB3 measurements :** Data collection for each available TB3 board, capturing MIP and SPS data using the ASIC's calibration mode.

— **TB3 measurements with Shower creation :** TB3 measurements involved using a brick to generate a particle shower, triggering the time-over-threshold (TOT) of the chip.

— **MiniTB measurements :** MIP and SPS measurements on MiniTB using both ASIC configuration modes : calibration and physics.

6.2.2 Beam test of Tileboard 3 equipped with 4mm² SiPMs

Tileboard Version 3 was equipped with a single H2GCROCv3 ASIC, a TB-Tester v2 DAQ system and 64 4 mm² SiPMs from the S16713 Hamamatsu pre-series (Figures 6.2 and 6.3). These SiPMs were connected to 64 ASIC channels ; however, eight channels lacked a scintillator tile installation on the SiPM and did not receive electron injections.

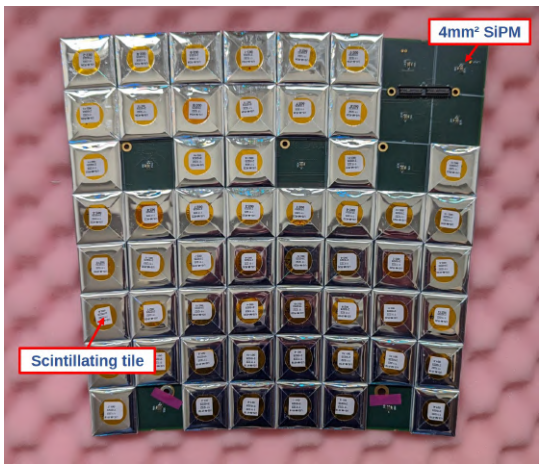

FIGURE 6.2 – *Front side of one Tileboard TB3 with 64 4 mm² SiPMs and scintillator tiles in every SiPM except spaces with holes or components.*

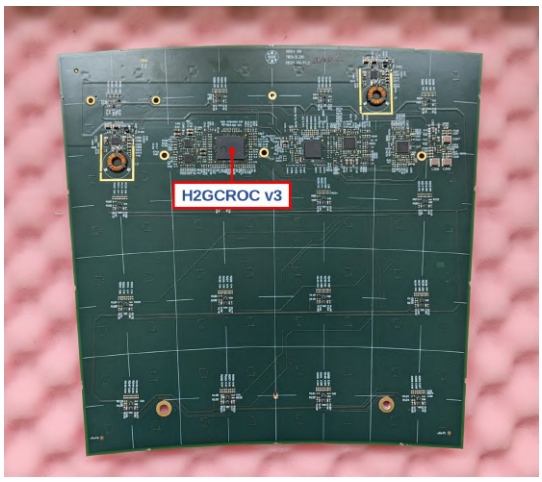

FIGURE 6.3 – *Back side of one Tileboard TB3 with one H2GCROCv3 ASIC for SiPM readout.*

We scanned every channel with a SiPM and a scintillator tile from the TB3. The ASIC Calibration mode configuration (see Section 5.3.1 for configuration modes information) was selected to read the SPS data for SiPM calibration and the MIP signal from the beam. In the regular operation of HGCAL, both configurations ensure optimal performance for each task. Maintaining a single configuration file for these tests simplifies data analysis and enhances understanding of ASIC performance.

Both TB3 boards had an LED per SiPM that could inject photons into the SiPMs. These LEDs allow each detector's reading of SPS data to determine gain variations between SiPMs. The LED power was configurable from 5.7 to 6.2 V to control light intensity. Since the calibration configuration has a high gain, saturation data was expected after the MIP signal. The time-of-arrival (TOA) and time-over-threshold (TOT) thresholds were set to maximum values to avoid triggering and focus on ADC measurements of MIP and SPS. The data from each SiPM-connected channel were compared to analyze the signal spread generated by the SiPM-ASIC setup.

Tileboard v3 was positioned on a platform in front of the beam and enclosed with fabrics to prevent external light sources. Figure 6.4 illustrates TB3 in the beam position before being covered, and Figure 6.1 presents the position of TB3 with scintillator tiles facing back the beam. The platform's positioning was managed from the control room to ensure precise alignment with the SiPM-on-tile's location for each channel.

For each fully equipped channel, the platform with TB3 was moved precisely to the same target tile point during each measurement. The target point was intentionally offset from the center of the tile crystal to simulate a realistic particle injection scenario and analyze crosstalk between neighboring channels. Figure 6.5 pictures the coordinate system used, where smaller, darker points represent the SiPM's position, and larger, lighter points represent the beam target. The Tileboard used for testing exhibited minor size variations among its tiles due to the conic

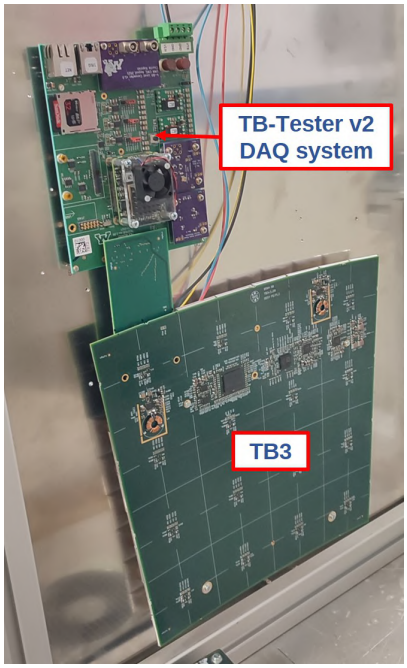

FIGURE 6.4 – *Tileboard TB3 connected to its DAQ system and placed in front of the beam.*

shape of the HGCAL.

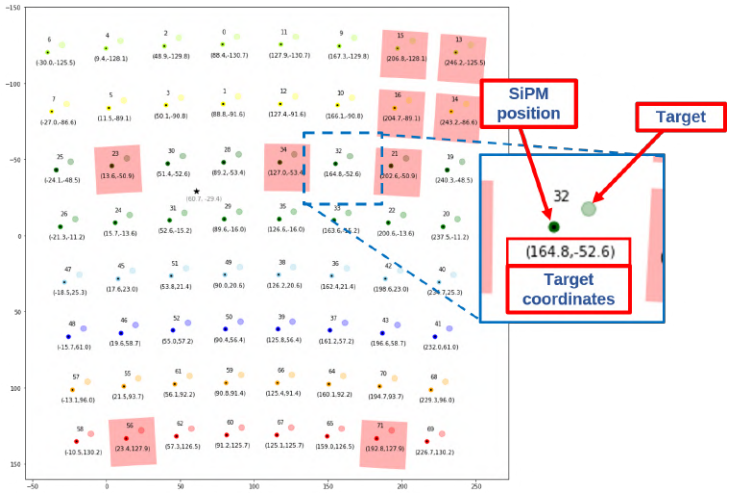

FIGURE 6.5 – *Tileboard coordinates used to calculate the beam position for MIP injection [81].*

Figure 6.6 displays the MIP signal measurement of a single channel. It shows two saturation zones : one at approximately 400 ADC units corresponding to the pedestal and one at 1023 ADC units corresponding to preamplifier saturation. The time, constructed with the delay measured from the trigger phase from the trigger scintillators, displays the MIP peak inside a 1.5625 ns window.

The ADC spectrum is shown in Figure 6.7. The MIP exhibits data in the preamplifier saturation zone due to the high gain configured in the ASIC. With two distinct Tileboards, satisfactory MIP responses were observed in every equipped channel. Since this was a preliminary test, the ASIC's configuration was not a primary focus, and most default values were retained, resulting in a considerable spread between channels. In normal operation, this spread will be rectified

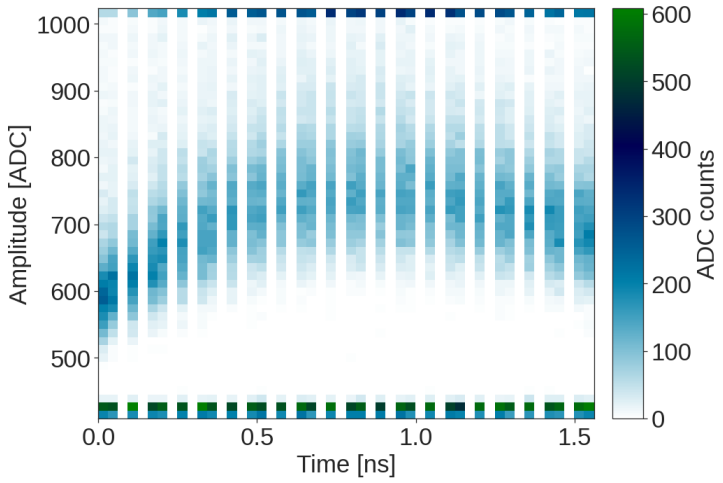

FIGURE 6.6 – *MIP response through time of one channel of TB3-1 equipped with a 4 mm² SiPM, using the Calibration Mode configuration of H2GCROC.*

through chip calibration of each channel, which is demonstrated in Section 4.5.5.

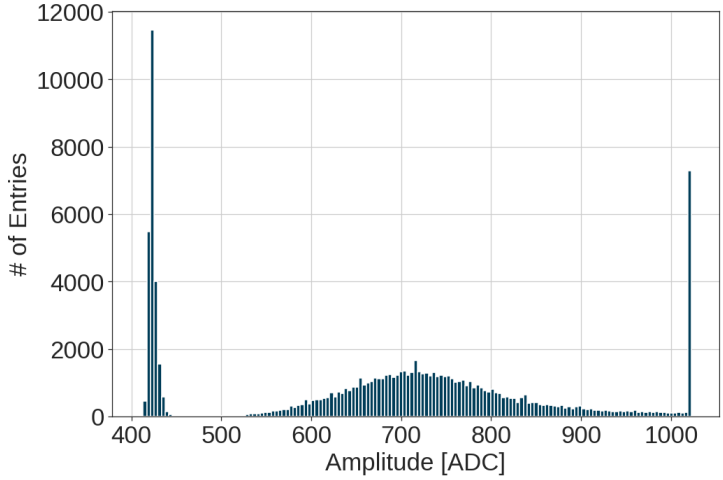

FIGURE 6.7 – *MIP histogram of one channel of TB3-1 equipped with a 4 mm² SiPM, using the Calibration Mode configuration of H2GCROC.*

Figure 6.8 shows the MIP response of a 4 mm² SiPM-on-tile after finding the correct L1A and phase on the chip's configuration. The pedestal and saturation data are removed to clarify the MIP response. Plotting the average amplitude minus the pedestal of each MIP data yields the plot of Figure 6.9. The plot includes data from just the first ASIC half, as the second half encountered some corrupted data, likely due to a faulty chip. The small spread between channels suggests two factors : the lack of previous configuration of the channels to reduce the spread between SiPM responses and the low resolution of the test bench position that caused discrepancies between the real injection point and the calculated points of Figure 6.5.

Figure 6.10 illustrates the signals generated in the eight neighboring channels after a MIP injection into the SiPM-on-tile of channel 1. The channels' position corresponds to the tiles on the board. As mentioned before, the beam target is not in the center of the tile ; it was placed more to the right and top position. The injection used the Calibration configuration of the ASIC, expecting increased crosstalk due to the high-gain configuration. However, in the ASIC, the

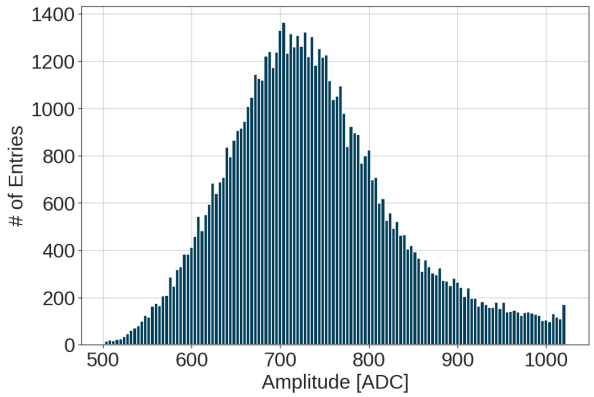

FIGURE 6.8 – *MIP histogram of one channel of TB3-1 equipped with a 4 mm² SiPM with pedestal and saturation subtraction, using the Calibration Mode configuration of H2GCROC.*

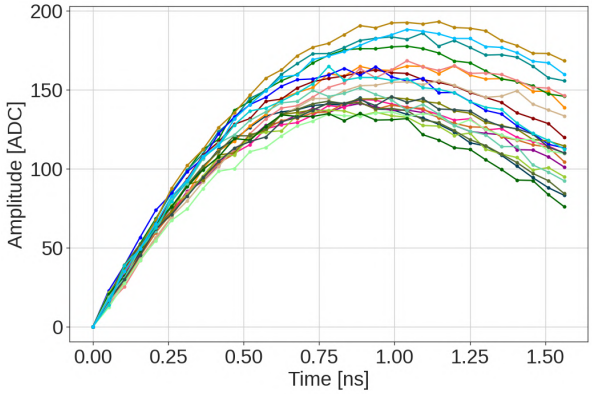

FIGURE 6.9 – *MIP mean amplitude response through time of TB3-1 of one half channels equipped with a 4 mm² SiPM, using the Calibration Mode configuration of H2GCROC.*

two closer neighbors, channels 0 and 2, have signals of 30 and 40 entries, similar to the other channels close to the beam.

In contrast, channel 12 has the highest signal, and channel 3 has the lowest. In this example, the beam's position was the primary source of crosstalk, indicating the beam was closer to the center of channel 1 but closer to channel 12. As discussed in Section 5.5.3, anticipated crosstalk using the proposed Physics mode configuration is expected to be significantly reduced compared to these observed results.

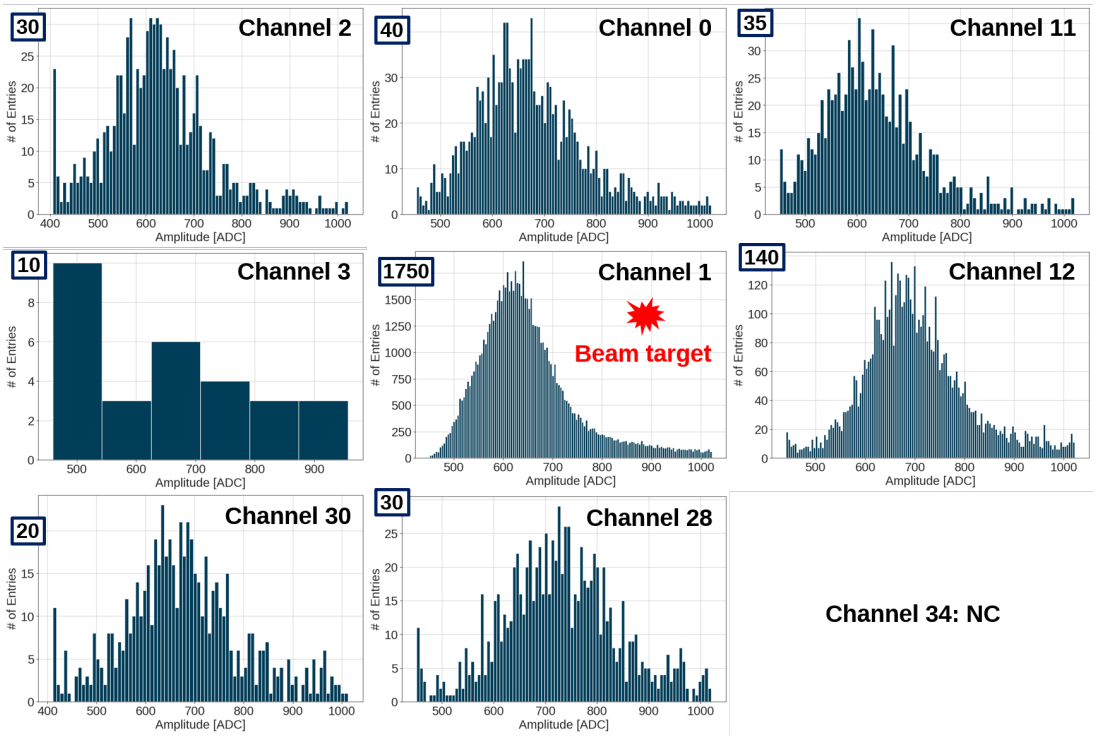

FIGURE 6.10 – *Crosstalk on the eight neighboring channels of the channel 1 after a MIP injection.*

Following the MIP measurement, the Tileboard's LED system injects photons into each

channel, enabling the Single Photon Spectrum (SPS) measurement. The SPS assessed the variation in gain among the different SiPMs connected to the ASIC. Adjustments were made to the light intensity and the overvoltage (OV) applied to the SiPM to achieve improved photon separation and approximate an SPS response similar to the one obtained under optimal laboratory conditions. Then, with the beam off, the LED power was configured to read photons on every channel and the gain difference between SiPMs. The measurement was conducted in three bunch crossings and all ASIC phases.

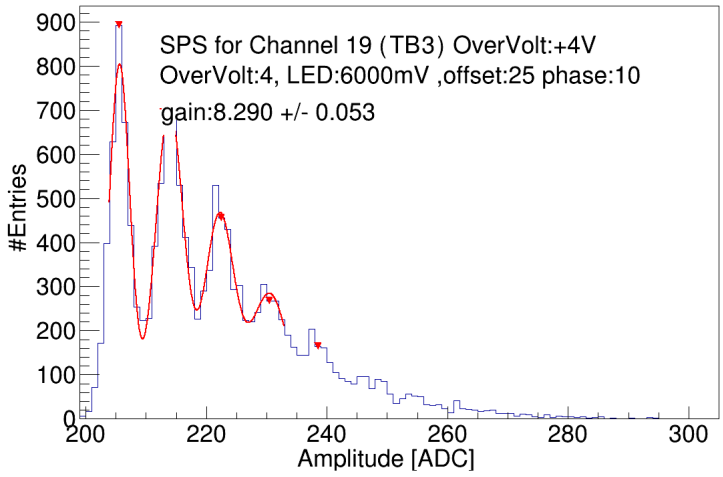

FIGURE 6.11 – *SPS of one channel with a 4 mm² SiPM from the TB3 with an overvoltage of 4V, a led intensity of 6V and ASIC configured phase of 10 [81].*

Figure 6.11 illustrates the SPS response of a channel equipped with a 4 mm² SiPM from the Tileboard, placed at the beam area under the same conditions as the previous MIP results. The gain of each SPS can be extracted with the difference in ADC from the photon peaks. The gain per ADC unit was determined to be 8.37 $ADC/p.e.$, with slight variations across channels. Figure 6.12 shows the gain variation from SiPM of one Tileboard, reflecting differences in SiPM manufacturing or temperature variations. During the operation of HGCAL, the V_{dac} of the current conveyor presented in Section 4.5.5 will compensate for the gain difference between SiPM detectors.

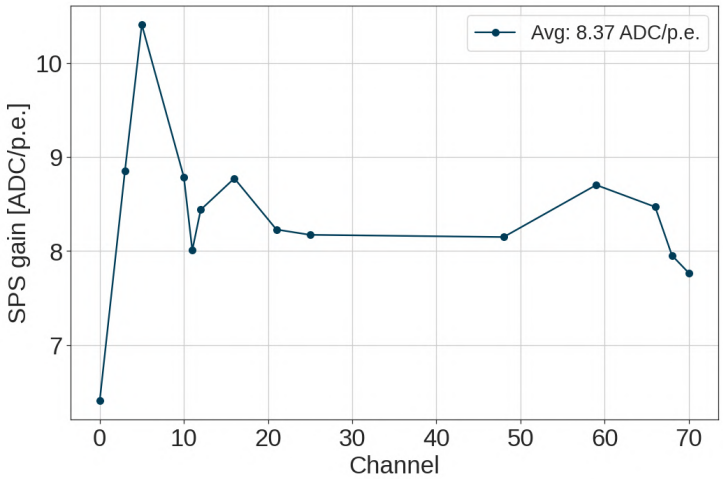

FIGURE 6.12 – $ADC/p.e.$ *gain measured from the SPS of some channels of the TB3-2.*

6.2.3 Beam test using a brick to produce a shower of particles

After successfully recording MIP and SPS data from all available channels, a 5 cm Steel brick was placed in front of the beam input to amplify the particles directed towards the detector and generate a shower. The Steel brick absorbs excess energy, reduces reflections and enhances the injected energy. The large energy released by the shower enables charge injection within the time-over-threshold range.

For this test, the threshold values were chosen without optimizing for the minimal charge needed for efficient TOA data. The $TOA_{threshold}$ was set above the pedestal of each channel without applying any trimming, ensuring the preservation of time information in the channels. Similarly, the $TOT_{threshold}$ value was selected to obtain TOT data in all channels despite slight variations in SiPM gain and pedestals.

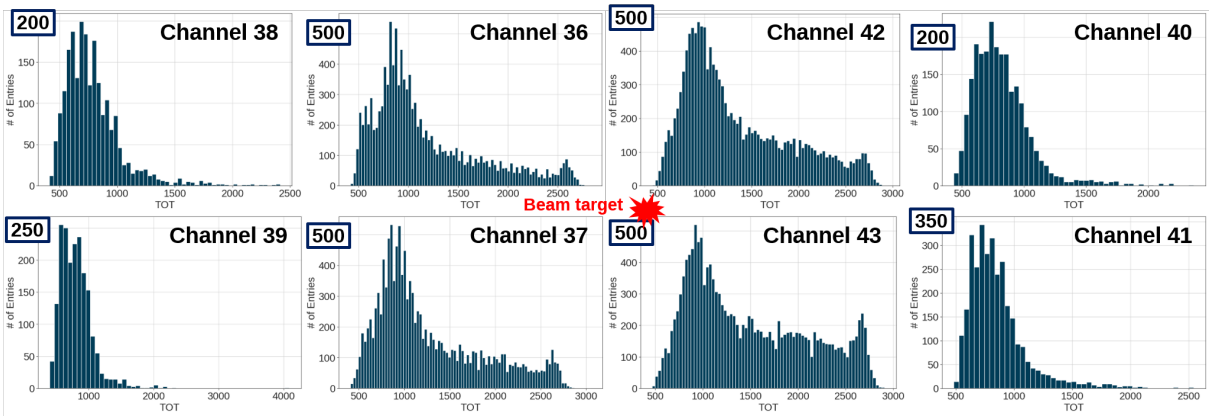

FIGURE 6.13 – *TOT data produced by a shower of particles from a 5 cm Steel brick absorber in front of the beam.*

The produced shower saturates the preamplifier, making the ADC saturated and unusable for reading charge energy. Figure 6.13 presents the corresponding TOT data of an injection taken at 5 GeV. The absorber produces TOT data in more than one channel. The extensive spread of light generated results in the following two channels on each side having TOT data but fewer events.

6.2.4 Beam test of the Mini Tileboard equiped with 2 mm², 4 mm² and 9 mm² SiPM.

As both Tileboards were exclusively equipped with 4 mm² SiPMs, the mini-tileboard was employed to evaluate the MIP signal read by other SiPMs. The mini-tileboard featured a combination of Hamamatsu pre-series SiPMs, including two of each 2 mm², 4 mm² and 9 mm² sizes. Figure 6.14 illustrates the setup of the mini-tileboard connected with the six SiPM sensors. The spatial arrangement of the detectors on the mini-tileboard required testing only two SiPMs at a time.

Despite the mini-tileboard having three different sizes of SIPM for HGCAL available, a few channels were inactive due to bad connections in the board, rendering it impossible to collect any data using the 2 mm² SiPM. Two tile crystals were positioned over 2 SiPMs, as depicted in Figure 6.14. Following the data collection of MIP and SPS, the crystal tile was repositioned to enable testing of the other sensors. The same alignment process allowed us to inject MIP data into the selected detectors. The measurements were performed with both configuration types : calibration and physics modes.

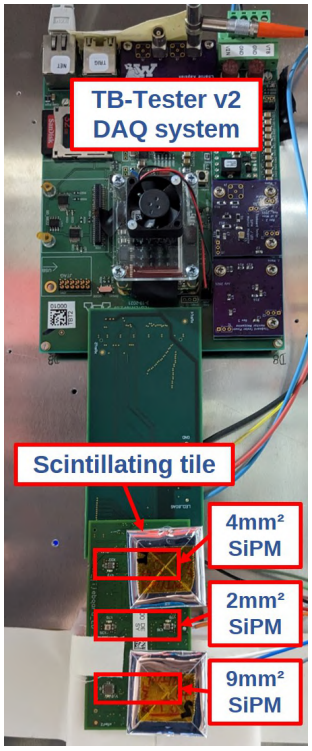

FIGURE 6.14 – *Mini-Tileaboard with its DAQ system placed in the beam area.*

The MIP response of the 4 mm² SiPM on the mini-tileboard configured with the Physics mode is illustrated in Figures 6.15 and 6.16. Both figures have the pedestal removed to clarify the MIP injection. The physics configuration, which will be used in regular HGCAL operations, reads the MIP charge without reaching ADC saturation.

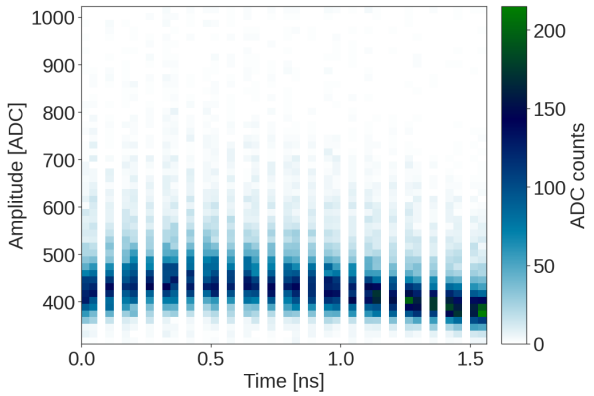

FIGURE 6.15 – *MIP response through time of one channel of the miniTB equipped with a 4 mm² SiPM with pedestal subtraction, using the Physics Mode configuration of H2GCROC.*

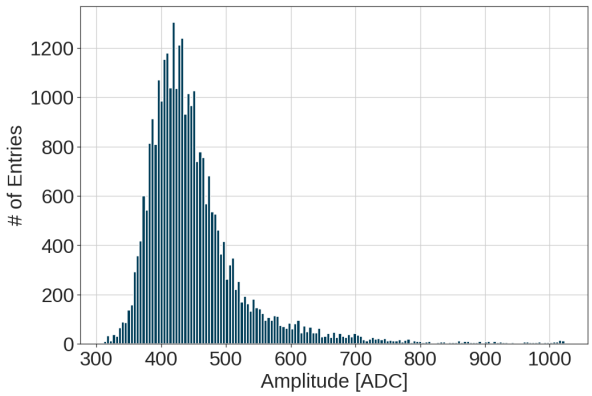

FIGURE 6.16 – *MIP histogram with pedestal subtraction of one channel of the miniTB equipped with a 4 mm² SiPM, using the Physics Mode configuration of H2GCROC.*

Subsequently, the Calibration configuration was used to read the SPS data and the 4 mm² SiPM gain in the MiniTB. Figure 6.17 presents the 4 mm² SiPM SPS that produced a $ADC/p.e.$ gain larger than that measured with the TB3. The gain increment comes from an increase of 2 V in the overvoltage, which elevates the gain. For comparison, the Calibration configuration

selected is optimal for reading SPS from the 9 mm² SiPMs. This Calibration configuration file has a more considerable preamplifier gain than typically used to read the 4 mm² SiPM SPS.

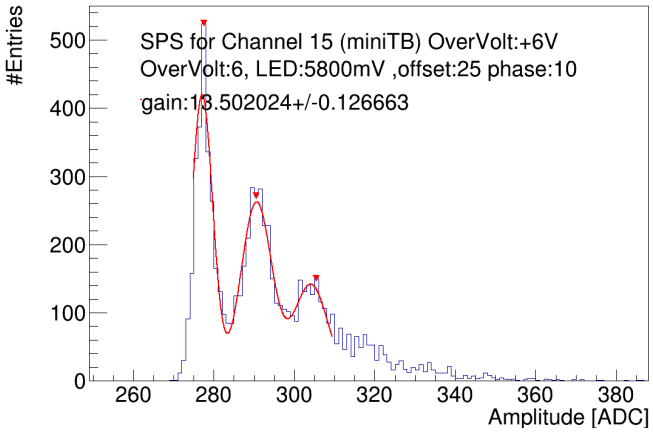

FIGURE 6.17 – *SPS of one channel with a 4 mm² SiPM from the MiniTB with an overvoltage of 6 V, a led intensity of 5.8 V and ASIC configured phase of 10 [81].*

The SPS of the 9 mm² SiPM was successfully measured with the MiniTB LED (Figure 6.18). The $ADC/p.e.$ gain measured is less than that measured with the 4 mm² SiPM. This gain reduction is a consequence of the reduction in amplitude produced by 9 mm² SiPMs.

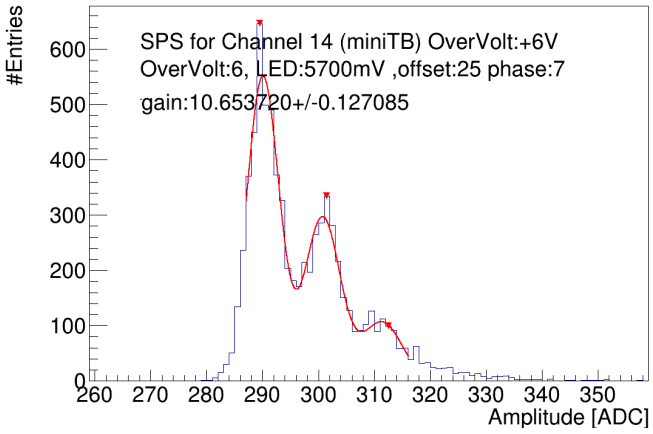

FIGURE 6.18 – *SPS of one channel with a 9 mm² SiPM from the MiniTB with an overvoltage of 6 V, a led intensity of 5.7 V and ASIC configured phase of 7 [81].*

Using the Physics configuration, the MIP was injected into the 9 mm² SiPM (Figures 6.19 and 6.20). The MIP response produces more light into the SiPM, resulting in a more significant signal that reaches ADC saturation. Interestingly, a detector with less gain per photon produces more charge injection from the MIP.

In this case, both SiPMs are using the same scintillator tile. The quantity of photons produced by a scintillator tile depends on the size ; the MIP signal changes with the number of photons produced and the photons captured by the SiPM. Large-area SiPMs capture more photons from the tile and increase the MIP signal measured by the front-end. For example, the same scintillator size will produce approximately 17 or 38 photons using a 4 mm² SiPM or a 9 mm² SiPM, respectively. The number of photons per MIP and the electronic noise increase

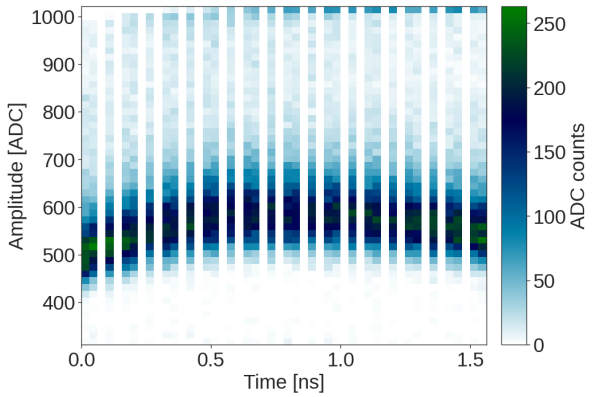

FIGURE 6.19 – *MIP response through time of one channel of the miniTB equipped with a 9 mm² SiPM with pedestal subtraction, using the Physics Mode configuration of H2GCROC.*

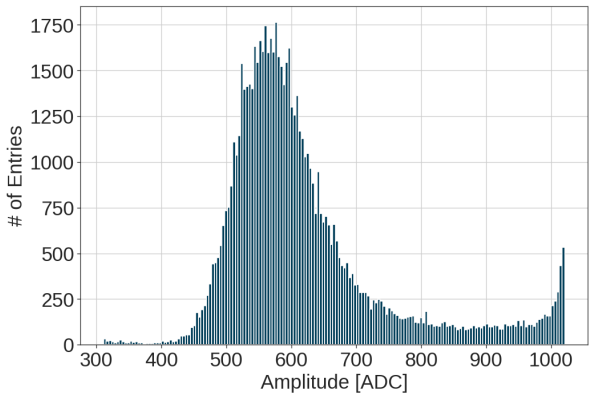

FIGURE 6.20 – *MIP histogram of one channel of the miniTB equipped with a 9 mm² SiPM with pedestal subtraction, using the Physics Mode configuration of H2GCROC.*

with the SiPM area. Therefore, the SNR_{MIP} measurement is more beneficial to understanding which SiPM leads to better HGCAL performance.

The SNR_{MIP} is necessary to calibrate HGCAL signals using MIPs. The MIP peak must be fitted to extract the calibration, and if the noise makes it wider, it will be necessary to take more events. For example, to track muons, they are propagated through the HGCAL material. We can follow the muon trajectory from the tracker track to the calorimeters and the muon chambers. The simulations performed in [36] present that the noise distribution of a MIP that passes through the SiPM-on-tile, preamplifier, shaper and ADC follows a Gaussian distribution even for low SNR_{MIP}. It is also noted that the number of entries improves the MIP fitting. An $SNR_{MIP} = 3$ needs around 175 entries to achieve a 5% precision. 175 entries correspond to 12.5 hours of running to achieve a correct calibration. Therefore, the objective will be to maintain an $SNR_{MIP} > 3$ for the entire operation of HGCAL.

Given this requirement, extensive discussions were held in the CMS collaboration to determine if the use of 9 mm² SiPMs in all scintillator tiles of the hadron calorimeter could enhance the Signal-to-Noise Ratio (SNR_{MIP}). Previous measurements indicate the signal and noise scale with the SiPM area. The Light Yield (Equation 2.2 [82]) serves as a better metric for comparing different SiPMs.

It has been demonstrated that the SiPM gain can be calculated from the 9 mm² SiPM SPS measurements. The MIP_{max} is determined from the highest peak of the MIP histogram data, subtracting the pedestal. Thus, even with the highest electronic noise produced by the 9 mm² SiPM, the Light Yield increases, resulting in an improved SNR_{MIP}. Furthermore, the noise in photons measured with the 9 mm² SiPM is reduced compared to the 4 mm² SiPM.

6.3 ASIC performance compared with specifications

The sizes of Tileboards used in HGCAL will incorporate scintillator tiles of varying dimensions. Larger scintillator sizes, employed in bigger Tileboards, convert energy into fewer photons than smaller tiles due to the extended space for reflection that reduces the number of photons reaching the SiPM. In contrast, smaller scintillator sizes can capture the same amount of energy, but the produced photons are more effectively directed toward the detector, producing a higher photon count. Thus, the photons produced by a MIP depend on the scintillator

tile size and the SiPM area. Table 6.1 provides an overview of the expected MIP photon and charge quantities for different SiPM and tile configurations in HGCAL.

	SiPM 4 mm²	**SiPM 9 mm²**
Larger scintillator tile MIP	17 p.e. (500 fC)	38 p.e. (1.1 pC)
Smaller scintillator tile MIP	67 p.e. (2 pC)	150 p.e. (4.4 pC)
SiPM gain	1.8×10^5	
Charge 1 p.e.	58.32 fC	

TABLE 6.1 – *MIP calculation for different scintillator tiles and the two proposed SiPM of HGCAL.*

The MIP calculations were used to analyze the MIP specifications of the H2GCROC ASIC. Table 6.2 summarizes key parameters of H2GCROC reading 4 mm² and 9 mm² SiPMs, the most likely choices for the final HGCAL design. The 9 mm² SiPM exhibits lower gain for energy measurements and a slight increase in noise. Time resolution decreases, and the time walk is slightly larger than the 4 mm² SiPM time walk.

	SiPM 4mm²	**SiPM 9mm²**
ADC gain	27.64 fC / ADC	44.88 fC / ADC
Charge ADC noise	1.2 (33 fC)	1.25 (47 fC)
Min charge with TOA	280 fC	420 fC
Time walk	18 ns	20 ns
Time resolution at 3 MIP small tile	240 ps	250 ps
Time resolution at 3 MIP large tile	370 ps	400 ps
Time resolution floor	25 ps	
Dynamic range	60 fC to 320 pC	
Radiation Hardness	Tested up to 20 Mrad	
Leakage compensation	1.3 mA	
Internal charge injection	Up to 200 pC	
Temperature operation	-39 °C to 50 °C	

TABLE 6.2 – *H2GCROC ASIC performance with the two proposed SiPM of HGCAL.*

The chip meets charge dynamic range requirements for both detectors compared to specifications. Charge measurement noise also stays within specified limits. Moreover, the chip demonstrates stability under radiation up to 20 Mrad and temperatures ranging from -39 °C to 50 °C. While the chip achieves up to 1.3 mA of leakage current compensation, further analysis is required for irradiated SiPMs. Alternative chip configurations can be explored if the 9 mm² SiPM yields leakage currents exceeding 1.3 mA. Increasing current conveyor attenuation would reduce frontend gain but allow for more extensive leakage current correction.

The chip was designed with internal charge injection close to the required dynamic range limit (320 pC). However, the 2.5 V DAC's charge injection capability is limited to 200 pC due to suboptimal DAC design and dependency on the chip's bandgap voltage. Optimizing the DAC design can enhance the maximum charge injection to 270 pC.

Regarding time measurements, H2GCROC has limitations, particularly in time resolution. The time jitter floor reached the expected 25 ps, but the significant detector capacitance impacted time walk and jitter more than anticipated. The slow peak produced by the 9 mm² SiPM resulted in time walks approaching the 25 ns limit. Selecting a time window corresponding to the ADC measurements' peak produces time walks exceeding 25 ns and misaligns some time

information with the wrong bunch crossing. However, the time window of H2GCROCv3 is shared by the ADC and TDCs of the ASIC, and different time windows cannot be configured in the third version of the chip.

6.3.1 Improvements for the next H2GCROC version

The results from the comprehensive testing of all modules integrated into the H2GCROC ASIC demonstrate that it fulfills CMS's new High Granularity Calorimeter (HGCAL) requirements. However, the H2GCROC is currently in its third fabricated version, and minor adjustments have been made for the upcoming final version of the ASIC intended for the HGCAL. The test results presented in Chapter 5 were made with a selected chip due to its good performance. However, certain errors were identified in other ASICs from both versions of HGCROC ; those errors will be addressed in the subsequent version, 3b. Table 6.3 summarizes the identified errors and their corresponding corrections for H2GCROCv3b.

H2GCROCv3	**H2GCROCv3b correction**
Bitflips in the RAMs	1. Add capacitance on one RAM's node. 2. Possibility to set the voltage of the node to VDDD.
ADC1 : Flat ADC ADC2 : Multiple ADC	Change the latency of the ADC clock.
TOA data in the wrong BXs	Correction in the start of the latency buffer of the TDC FiFo.
TOA data of one half stuck at 504 value	Correction in the locked of the Master DLL.
Faster TDC measurement	Change the startup sequence of the TDC.
TOA and TOT data in the wrong BX	Capacity to configure independently the ADC and TDC phases.
Calib2V5 DAC has nonlinearities and low dynamic range	Improve the robustness of the DAC and increment dynamic range.
High rate of SEU events	Increase of triplicated parts in the PLL.

TABLE 6.3 – *H2GCROCv3 malfunctions and H2GCROCv3b corrections.*

Some chips exhibited bitflips in the RAMs, particularly at high temperatures. The bitflips were created because one node of RAM2 was configured with a VDD of 1V and had lower capacitance. An option to force the VDD of the node to VDDD (1.2 V) was incorporated, and the node capacitance was incremented. These solutions were implemented and tested in another ASIC with the same RAM design, successfully eliminating the bitflips.

Some chips displayed malfunctioning channels, leading to two types of wrong ADC measurements : some channels exhibited flat ADC readings at the pedestal level, and others produced the ADC signal multiple times. It was determined that the ADC did not convert at 40 MHz, and though ADC settings sometimes corrected the issue, the ADC latency clock was modified for the subsequent ASIC version. This correction was also implemented and validated in another ASIC and proved to remove the errors.

The TDCs exhibited diverse errors : incorrect TOA data in different bunch crossings, all TOA data equal to 504, or channels with faster TDC measurements resulting in strange readings.

Simulations revealed an error in the startup sequence of the TDC FIFO's latency buffer and a failure in correctly locking the master TDC. The startup sequence was modified, and the latency of the TDC FIFO was corrected.

In the SiPM HGCROC version, slower signals generated by larger SiPMs produced more than 25 ns signal duration, causing TOA and TOT data to be associated with the wrong bunch crossing. This time walk error can be rectified by selecting a more optimal window for time measurements, as illustrated in Figure 6.21, which also contributes to improved jitter-in-time measurements. Optimal window selection for energy measurements produces a lower slope for time measurement, resulting in suboptimal time-of-arrival performance. Choosing a different window where the signal exhibits a higher slope would be more favorable to enhance jitter performance and reduce the time walk. This feature was added to the H2GCROCv3b ASIC.

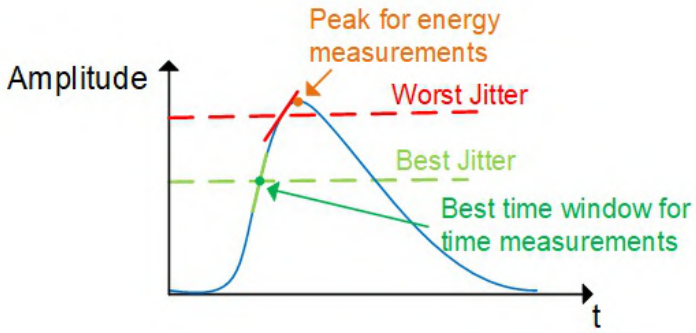

FIGURE 6.21 – *Jitter measurement dependency in the slope of energy signal measurement.*

An analysis of the internal charge injection of the chip revealed differing performances in the two DACs responsible for injecting charge into the current conveyor or the preamplifier. The DAC design for charge injection into the current conveyor was modified to increase the dynamic range and address the non-linearities observed in the third version.

The irradiation test for Single Event Effects in Section 5.7.4 indicated a higher rate of Single Event Upsets (SEUs) in the PLL section of the ASIC than anticipated. The new ASIC version includes incrementing the triplicated parts of the PLL to reinforce the affected areas.

6.4 Comparison of ASIC designs for SiPM Readout

The state-of-the-art front-end electronics for SiPM readout in particle physics have seen significant advancements, featuring various ASIC designs designed to meet the strict requirements of particle detectors. Table 6.4 provides a comprehensive summary of the performance of H2GCROC and various SiPM readout ASICs from the state-of-the-art (Section 3.7). This table outlines the key characteristics of different ASICs employed in SiPM readings. However, it also underscores the boundaries of the ASIC designed for HGCAL, which can be limited for other applications, especially for high-resolution time measurements of single photons.

The variation in ASIC performance derives from the distinct requirements of specific applications. Each front-end technique for SiPM readout has its advantages and disadvantages. The Voltage preamplifier (VPA) architecture excels in noise performance for energy measurements and is suitable for very low-power applications, consuming less than 1 mW per channel. However, this very low power comes at the expense of low time resolution. The PETA4 ASIC demonstrates that improved time resolution can be achieved with VPA at the cost of higher power consumption per channel.

ASIC (Arch.)	Tech	# of chan	BW $[Hz]$	Z_{in}	C_{det}	Dyn Range	Power consu.	Time Reso.
SPIROC (VPA)	350 nm	36	800 M	100 Ω	10 pF - 100 pF	50 fC - 320 pC	25 μW (1% pulsing)	1 ns RMS
PETA4 (VPA)	180 nm	36	900 M	7 Ω	100 pF - 1 nF	10 fC - 100 pC	40 mW	148 ps RMS
PETIROC (RF)	350 nm	16	900 M	200 Ω	10 pF - 100 pF	100 fC - 300 pC	3.6 mW	16 ps RMS
LIROC (RF)	130 nm	64	1.4 G	60 Ω	10 pF - 100 pF	10 fC - 100 pC	3.28 mW	15 ps RMS
TOFPET2 (CC)	110 nm	64	330 M	11 Ω	320 pF - 1 nF	10 pC - 1500 pC	8.2 mW	100 ps RMS
TRIROC (CC)	350 nm	64	80 M	100 Ω	10 pF - 100 pF	100 fC - 320 pC	10 mW	100 ps RMS
H2GCROC (CC)	***130 nm***	***72***	***80 M***	***25 Ω***	***100 pF - 1 nF***	***60 fC - 320 pC***	***11.8 mW***	***100 ps RMS***

TABLE 6.4 – *Comparison of state-of-the-art performance of ASICs for reading of SiPM detectors. *The time resolution corresponds to the measurement obtained with the minimum C_{det} within the acceptable range of the chip.*

The radio frequency (RF) approach is best for low-power and high-time resolution. Even innovative designs like the LIROC ASIC showcase their utility in multi-channel applications. However, this approach has limitations regarding the size of SiPMs it can use. RF amplifiers may encounter difficulties reading high capacitances associated with larger SiPMs ; the examples presented struggle to read detector capacitances larger than 100 pF with high resolution.

Incorporating the current conveyor at the input reduces the input impedance, increments the dynamic range and lowers the system's bandwidth. This strategy effectively conveys the fast current generated by the SiPM to subsequent stages in the front-end design. These systems achieve an extensive dynamic range of measurements and time resolution on the order of 100 ps RMS, making them suitable for reading SiPMs with detector capacitances up to 1 nF.

The strengths of H2GCROC lie in its multi-channel capability, enabling the reading of various SiPMs with a high dynamic range and timing resolution below 100 ps. As previously outlined, its design aligns with its application requirements, reading the SiPM-on-tile in the rear hadronic part of HGCAL. Some state-of-the-art ASICs incorporate digital processing within the chip but increase power consumption. H2GCROC integrates complex trigger algorithms, memories, PLL and high configurability without significantly elevating power consumption. Consequently, it stands out as a highly efficient, low-power front-end design.

However, H2GCROC has limitations, particularly in the domain of time measurements. The MIP expected at HGCAL will surpass 15 photon electrons, with the time resolution requirement being less than 100 ps for signals equivalent to 3 MIP. Therefore, the ASIC's time resolution cannot match other ASICs' Single Photon Time Resolution (SPTR). Other chips in the literature employ dedicated amplifiers with a lower dynamic range to achieve superior timing resolution. On the other hand, the specifications of H2GCROC demanded a simplified design based on the Si-version of the ASIC, with both time and energy paths utilizing the same current conveyor and preamplifier. This design proved not to be suitable for SPTR measurements with high resolution.

6.5 Recommendations for further improvements and developments

When selecting an ASIC for SiPM readout in particle physics, the choice depends on the specific requirements of the experiment, including considerations of power, precision and the nature of the detected signals. Ongoing advances in ASIC technology continuously push improvements in SiPM readout systems, enhancing performance and reliability in particle physics experiments.

While the performance of H2GCROC aligns with the requirements of HGCAL, it exhibits some limitations due to the requirement to re-use the ADC/TOT architecture of HGCROC, the Si version of HGCAL ASICs. By requirement, the ASIC needs a preamplifier optimized for a different charge dynamic range and the adaptation of its input signal using a current conveyor. The chip's time measurements could be enhanced by optimizing the current conveyor and preamplifier for reading SiPM detectors with some modifications. The current design, involving signal attenuation followed by amplification during voltage conversion, introduces errors from the current conveyor block. This approach of attenuating the small signal from the detector and subsequently amplifying it is not optimized for SiPM readings, leading to a significant increase in noise that adversely affects the time resolution of the ASIC. The modification at the input of the channels enables charge measurements within a range of up to 320 pC but compromises the time measurement resolution, making it challenging to perform Single Photon Time Resolution (SPTR) measurements for time-of-flight applications using this chip.

The literature features interesting designs with higher time resolutions that could influence modifications to the current design. In some cases, dedicated energy and time measurement branches have been employed to improve time resolution. Another potential approach is to modify the preamplifier design to a differential or fully differential configuration, which could further reduce front-end noise.

The switching capacitor architecture could be suitable for reading a wide range of charges from SiPMs with large areas. By switching between different capacitor sizes or gain configurations, the architecture can effectively handle a broad spectrum of input signals, ranging from small to large charges. The time resolution is notably improved, particularly for lower charge measurements. In this architecture, the system dynamically adjusts to the most suitable gain configuration depending on the input charge. This selection of a dedicated gain configuration based on the input charge optimizes the front-end readings for precise timing measurements, necessary for reading the single-photon time resolution from the SiPM.

When a large charge arrives at the input, the front-end switches to a different gain. However, the reduction in time resolution is not critical for large charge injections, as they have a faster rising edge. Additionally, the signal-to-noise ratio is not compromised due to the large charge injection. This architecture can offer more than two gains in its configuration with the drawback of losing some information when the system switches to the next available gain. Moreover, switching capacitor architectures can achieve high efficiency in terms of power consumption.

For the H2GCROC ASIC design, the 130 nm TSMC technology was selected because it has been proven to be suitable for hard radiation environments and has delivered good results as a readout for high-energy physics experiments. However, smaller technologies such as 65 nm or 28 nm have started to be tested in hard radiation environments and are beginning to be chosen for the next state-of-the-art designs. An example is the FASTIC ASIC [88] designed by CERN in 65 nm technology. This ASIC features 8 channels, each consuming 12 mW. It is capable of reading SiPMs using positive or negative polarity and operates with a power supply of 1.2 V. Its design incorporates a low input impedance ($\sim 20\ \Omega$) current mirror with three outputs :

— **Time measurement :** Utilizes a discriminator and can measure a SPTR of 140 ps and a jitter of 30.9 ps with the S13360-3050CS Hamamatsu 9 mm² SiPM at a 10.6 V over-

voltage.

— **Energy measurement :** Employs a Transimpedance Amplifier with selectable gain, a shaper with configurable pole-zero cancellation, a peak detector, and a discriminator for the time-over-threshold technique, producing measurements with a 3% linearity error.

— **Trigger :** Configured with a low-level set just above the SiPM dark count.

The FASTIC ASIC is currently undergoing evaluation for potential use at the LHCb experiment at CERN. Its performance has shown promising results, serving as a strong indicator that smaller technologies, such as 65 nm, should be considered for future projects in high-energy physics experiments.

6.6 Conclusion

This chapter delved into the performance of H2GCROC within a realistic environment closely resembling the intended conditions of the HGCAL to highlight its capabilities and behavior. The measurements carried out during the test beam at DESY yielded crucial experimental data, enabling a detailed examination of the ASIC's performance in a realistic operating environment.

Subsequently, a comprehensive comparison of the ASIC's performance against specifications underscored its strengths and identified areas for improvement addressed for the new and final ASIC version H2GCROCv3b.

Additionally, evaluating the ASIC against state-of-the-art designs in SiPM readout systems provided valuable context and benchmarks for its performance. This comparative analysis delineated the ASIC's position in SiPM front-end electronics, highlighting its merits and suggesting areas where further advancements or modifications could be beneficial.

The combined insights derived from the test beam measurements, performance analysis, state-of-the-art comparison and ASIC modifications form a robust foundation for ongoing developments and optimizations in SiPM readout electronics. The outcomes of this chapter contribute significantly to the continuous progress of detector technologies, ultimately supporting the success of particle physics experiments and our understanding of the fundamental principles of the universe.

Chapter 7

General Conclusions

This thesis has presented a comprehensive exploration of the H2GCROC ASIC, designed for the readout of SiPM detectors in the context of the CMS HGCAL experiment. The journey began with an overview of the experiment's background, objectives and contributions, setting the stage for a detailed investigation into the analog electronic design for SiPM detectors.

The exploration of the CMS HGCAL experiment and the specific requirements for SiPM readout were the foundation for understanding the challenges and design considerations addressed in the subsequent chapters. The analog electronic design section introduces CMOS technology and its critical components for readout in particle physics applications, such as amplifiers, current conveyors, analog-to-digital converters and time-to-digital converters. The challenges associated with SiPM detectors, the importance of timing measurements and the limitations in achieving precise timing with SiPMs were discussed.

The heart of the thesis is the detailed examination of the H2GCROC ASIC, the very front-end ASIC for SiPM-on-tile readout on HGCAL. The ASIC's architecture, design and functionalities were meticulously presented, focusing on charge and time measurement performance. Moreover, the calibration capabilities of the ASIC were offered, addressing gain configuration, pedestal adjustment, time threshold calibration and trimming between channels.

The subsequent chapter has the characterization of the H2GCROC ASIC, presenting a comprehensive analysis of its performance. Measurements of charge and time, noise analysis, cross-talk evaluation, temperature dependency, radiation tolerance, power consumption and overall robustness of the chip were shown. These analyses provided valuable insights into the ASIC's behavior under various conditions, contributing to a thorough understanding of its capabilities and limitations.

The ASIC's validation and verification were addressed through its performance in a test beam to assess its functionality. The thesis further evaluated the ASICs to specifications, compared their design with other SiPM readout ASICs and provided recommendations for future improvements and developments.

The key contributions of this work include an understanding of ASIC architecture and its characterization. The thesis started with the architecture design completed and the second fabricated version of the ASIC ready for testing. Through this work, we gained insights into the impact of SiPM detectors on the chip design. Subsequently, a modification for the third fabricated version was proposed, implemented, tested in simulation, incorporated into the layout and validated using the third fabricated version of the chip.

In conclusion, this work has contributed to the specific domain of SiPM readout for HGCAL and provided insights and methodologies that can be extended to other particle physics experiments. This manuscript provides an overall understanding of the SiPM-on-tile readout, starting with the basic principles and details of the ASIC design proposed. The meticulous analysis

of the H2GCROC ASIC, its performance in realistic conditions and the recommendations for future enhancements collectively contribute to the continuous advancement of detector technologies and our understanding of fundamental principles in the universe. As the CMS experiment evolves and new challenges emerge, the outcomes of this thesis serve as a solid foundation for ongoing research and development efforts in the realm of SiPM readout electronics.

Bibliography

[1] A. Lobanov, “Electronics and triggering challenges for the CMS High Granularity Calorimeter,” *Journal of Instrumentation. Calorimetry for High Energy Frontier*, vol. 13, no. 02, p. C02056, 2018.

[2] CMS collaboration, “The Phase-2 Upgrade of the CMS endcap calorimeter,” *Technical Design Report*, no. CERN-LHCC-2017-014. CMS-TDR-018, 2017. [Online]. Available : https://cds.cern.ch/record/2283193

[3] P. Aspell, C. De La Taille, F. Dulucq, M. Noy, D. Thienpont, S. Extier, M. El Berni, and A. Lobanov, “Working document on Specification. HGCROC3,” *CMS - EDMS 2324379*, vol. CMS-CE-ES-0029, 2021. [Online]. Available : https://edms.cern.ch/ui/file/2324379/1/HGCROC3_Spec_Working_Document_v2.0.pdf

[4] F. Sefkow, A. White, K. Kawagoe, R. Pöschl, and J. Repond, “Experimental tests of particle flow calorimetry,” *Reviews of Modern Physics*, vol. 88, no. 1, pp. 1–55, 2016.

[5] Konrad Briggl, “Silicon Photomultiplier Readout Electronics for Imaging Calorimetry Applications,” Ph.D. dissertation, Combined Faculties of the Natural Sciences and Mathematics of the Ruperto-Carola-University of Heidelberg, 2018. [Online]. Available : http://archiv.ub.uni-heidelberg.de/volltextserver/24088/

[6] L. Mastrolorenzo, “The CMS High Granularity Calorimeter for HL-LHC,” *International Journal of Modern Physics : Conference Series*, vol. 46, no. Panic 2017, p. 1860075, 2018.

[7] C. T. R. Wilson, “On a method of making visible the paths of ionising particles through a gas,” *Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character*, vol. 85, no. 578, pp. 285–288, 1911.

[8] M. K. Gaillard, P. D. Grannis, and F. J. Sciulli, “The standard model of particle physics,” *Reviews of Modern Physics*, vol. 71, no. SUPPL. 2, pp. 1–25, 1999.

[9] J. Rehm and B. Biggs, “The four fundamental forces of nature,” SPACE.com, Tech. Rep., 2021. [Online]. Available : https://www.space.com/four-fundamental-forces.html

[10] I. Newton, *Principia. The Mathematical Principles of Natural Philosophy. Vol. 1 The Motion of Bodies.*, 1962.

[11] A. Einstein, “Die Grundlage der allgemeinen Relativitätstheorie (The basis of the general theory of relativity),” *Annalen der Physik*, vol. 354, no. 7, pp. 769–822, 1916.

[12] J. Woithe, G. J. Wiener, and F. F. Van Der Veken, “Let’s have a coffee with the Standard Model of particle physics !” *Physics Education*, vol. 52, no. 3, 2017.

[13] Cush, “File :Standard Model of Elementary Particles.svg,” Tech. Rep., 2019. [Online]. Available : https://commons.wikimedia.org/wiki/File:Standard_Model_of_Elementary_Particles.svg

[14] ILC, “About the International Linear Collider,” ILC International Development Team, Tech. Rep., 2021. [Online]. Available : https://linearcollider.org/

[15] CERN, “The Large Hadron Collider,” CERN, Tech. Rep., 2008. [Online]. Available : https://www.home.cern/science/accelerators/large-hadron-collider

[16] CMS collaboration, “Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC,” *Physics Letters, Section B : Nuclear, Elementary Particle and High-Energy Physics*, vol. 716, no. 1, pp. 30–61, 2012.

[17] ATLAS collaboration, “Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC,” *Physics Letters, Section B : Nuclear, Elementary Particle and High-Energy Physics*, vol. 716, no. 1, pp. 1–29, 2012.

[18] CERN, “Linear accelerator 4,” CERN, Tech. Rep., 2020. [Online]. Available : https://home.cern/science/accelerators/linear-accelerator-4

[19] E. Lopienska, “The CERN accelerator complex,” Tech. Rep., 2022. [Online]. Available : https://cds.cern.ch/images/CERN-GRAPHICS-2022-001-1

[20] CERN, “The High-Luminosity LHC (HL-LHC) Project,” no. May, 2016.

[21] G. Petrucciani, “The CMS experiment at the CERN LHC,” *The Search for the Higgs Boson at CMS*, pp. 15–58, 2013.

[22] CMS collaboration, “A new boson with a mass of 125 GeV observed with the CMS experiment at the Large Hadron Collider (Science (2012) (1569)),” *Science*, vol. 339, no. 6125, p. 1275, 2013.

[23] J. Williams, “General Physics Objects and POET,” CMS, Tech. Rep., 2007. [Online]. Available : https://cms-opendata-workshop.github.io/workshop2022-lesson-physics-objects/aio/index.html

[24] Helmuth Spieler, “Analog and Digital Electronics,” *Physics Division, Lawrence Berkeley National Laboratory*, vol. 1, no. C, pp. 1–3, 2014.

[25] A. Benaglia, E. Auffray, P. Lecoq, H. Wenzel, and A. Para, “Space-Time Development of Electromagnetic and Hadronic Showers and Perspectives for Novel Calorimetric Techniques,” *IEEE Transactions on Nuclear Science*, vol. 63, no. 2, pp. 574–579, 2016.

[26] D. Anderson, A. Apresyan, A. Bornheim, J. Duarte, C. Peña, M. Spiropulu, J. Trevor, S. Xie, and A. Ronzhin, “Precision timing calorimeter for high energy physics,” *Nuclear Instruments and Methods in Physics Research, Section A : Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 824, pp. 670–673, 2016. [Online]. Available : http://dx.doi.org/10.1016/j.nima.2015.11.129

[27] F. Powolny, E. Auffray, S. E. Brunner, E. Garutti, M. Goettlich, H. Hillemanns, P. Jarron, P. Lecoq, T. Meyer, H. C. Schultz-Coulon, W. Shen, and M. C. Williams, “Time-based readout of a silicon photomultiplier (SiPM) for time of flight positron emission tomography (TOF-PET),” *IEEE Transactions on Nuclear Science*, vol. 58, no. 3 PART 1, pp. 597–604, 2011.

[28] M. Oulmane and G. W. Roberts, “A CMOS time amplifier for femto-second resolution timing measurement,” *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 1–4, 2004.

[29] J. A. McCubrey, L. S. Steelman, W. H. Chappell, S. L. Abrams, E. W. Wong, F. Chang, B. Lehmann, D. M. Terrian, M. Milella, A. Tafuri, F. Stivala, M. Libra, J. Basecke, C. Evangelisti, A. M. Martelli, and R. A. Franklin, “Technical proposal for a MIP timing detector in the CMS experiment Phase 2 upgrade,” *Biochim Biophys Acta*, vol. 1773, no. 8, pp. 1263–1284, 2017.

[30] M. Reinecke, “The CMS High Granularity Calorimeter Scintillator/SiPM Tileboards,” *Journal of Physics : Conference Series*, vol. 2374, no. 1, pp. 0–5, 2022.

[31] CMS collaboration, “Handling large data volumes of CMS High Granularity Calorimeter,” *CERN*, 2020. [Online]. Available : https://www.niser.ac.in/daehep2020/talkposter/Alpana_Alpana_TLK_124_195.pdf

[32] F. Faccio, S. Michelis, G. Blanchot, G. Ripamonti, and A. Cristiano, “The bPOL12V DCDC converter for HL-LHC trackers : Towards production readiness,” *Proceedings of Science*, vol. 370, no. September 2019, pp. 1–5, 2019.

[33] P. Carniti, C. Gotti, and G. Pessina, “ALDO2, a multi-function rad-hard linear regulator for SiPM-based HEP detectors,” *Nuclear Instruments and Methods in Physics Research, Section A : Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 1039, pp. 4–7, 2022.

[34] A. Caratelli, S. Bonacini, K. Kloukinas, A. Marchioro, P. Moreira, R. De Oliveira, and C. Paillard, “The GBT-SCA, a radiation tolerant ASIC for detector control and monitoring applications in HEP experiments,” *Journal of Instrumentation*, vol. 10, no. 3, pp. 557–560, 2015.

[35] F. Sefkow and F. Simon, “A highly granular SiPM-on-tile calorimeter prototype,” *Journal of Physics : Conference Series*, vol. 1162, no. 1, 2019.

[36] A. Martelli, C. Seez, P. Silva, and S. Kim, “Study of HGCAL SiPM-tile intercalibration using muons. Detector Note,” *The Compact Muon Solenoid Experiment*, no. September, pp. 1–20, 2022. [Online]. Available : https://icms.cern.ch/tools-api/restplus/relay/piggyback/notes/DN/2022/10/files/3/download

[37] L. M. S. deSilva and CMS collaboration, “Scintillator Section of the CMS High Granularity Calorimeter Upgrade (HGCAL),” *The European Physical Society Conference on High Energy Physics (EPS-HEP2023)*, no. August 2023, pp. 21–25, 2024.

[38] CERN, “LpGBT-FPGA Documentation,” CERN, Tech. Rep., 2023. [Online]. Available : https://lpgbt-fpga.web.cern.ch/doc/html/

[39] X. Wu, M. Zhang, and J. Van Der Spiegel, “High linearity current mode image sensor,” *2012 IEEE International Conference on Electron Devices and Solid State Circuit, EDSSC 2012*, no. Cc, pp. 3–6, 2012.

[40] D. Stefanović and M. Kayal, *Structured Analog CMOS Design*, 2008.

[41] Y. Moisiadis, I. Bouras, and A. Arapoyanni, “Charge pump circuits for low-voltage applications,” *VLSI Design*, vol. 15, no. 1, pp. 477–483, 2002.

[42] D. Moro Frias, “Design and Applications of CMOS Current Conveyors,” Master Thesis, National Institute for Astrophysics, Optics and Electronics, INAOE., 2008.

[43] S. S. Rajput and S. S. Jamuar, “Low voltage, low power and high performance current conveyors for low voltage analog and mixed mode signal processing applications,” *Analog Integrated Circuits and Signal Processing*, vol. 41, no. 1, pp. 21–34, 2004.

[44] K. Koli, *CMOS Current Amplifiers : Speed Versus Nonlinearity*, 2000.

[45] K. Smith and A. Sedra, “The Current Conveyor - A New Circuit Building Block,” *Proceedings of the IEEE*, vol. 56, no. 8, pp. 1368–1369, 1968.

[46] ——, “A Second-Generation Current Conveyor and its applications,” *Ieee Transactions on Circuit Theory*, vol. 17, no. February, pp. 132–134, 1970.

[47] A. Fabre, “Third-generation current conveyor : a new helpful active element,” *Electronics Letters*, vol. 31, no. March, pp. 338–339, 1995.

[48] M. Integrated, “Understanding SAR ADCs : Their Architecture and Comparison with Other ADCs,” pp. 1–7, 2001.

[49] G. Roberts, “A Brief Introduction to Time-to-Digital and Digital-to-Time Converters,” no. September, 2014.

[50] Hamamatsu, “What is MPPC (SiPM)? | Multi- Pixel Photon Counters (MPPCs / SiPMs),” Hamamatsu, Tech. Rep., 2023. [Online]. Available : https://www.hamamatsu.com/eu/en/product/optical-sensors/mppc/what_is_mppc.html

[51] P. Calò, F. Ciciriello, S. Petrignani, and C. Marzocca, “SiPM readout electronics,” *Nuclear Inst. and Methods in Physics Research*, vol. A, no. 926, pp. 57–68, 2019.

[52] M. Nemallapudi, S. Gundacker, P. Lecoq, and E. Auffray, “Single photon time resolution of state of the art SiPMs,” *Journal of Instrumentation*, vol. 11, no. P10016, 2016.

[53] Hamamatsu, “MPPC (multi-pixel photon counter) S14160-1310PS/-1315PS/-3010PS/-3015PS,” Hamamatsu, Tech. Rep., 2020. [Online]. Available : https://www.hamamatsu.com/resources/pdf/ssd/s14160-1310ps_etc_kapd1070e.pdf%0A

[54] D. Meier, S. Mikkelsen, J. Talebi, S. Azman, G. Mahlum, and B. E. Patt, “An ASIC for SiPM/MPPC readout,” *IEEE Nuclear Science Symposium Conference Record*, pp. 1653–1657, 2010.

[55] S. Di Lorenzo, Conforti, S. Callier, J. Fleury, F. Dulucq, C. De La Taille, G. M. Chassard, L. Raux, and N. Seguin-Moreau, “SPIROC : Design and performances of a dedicated very front-end electronics for an ILC Analog Hadronic CALorimeter (AHCAL) prototype with SiPM read-out,” *Journal of Instrumentation*, vol. 8, no. 1, 2013.

[56] I. Sacco, P. Fischer, and M. Ritzert, “PETA4 : A multi-channel TDC/ADC ASIC for SiPM readout,” *Journal of Instrumentation*, vol. 8, no. 12, 2013.

[57] J. Fleury, S. Callier, C. De La Taille, N. Seguin, D. Thienpont, F. Dulucq, S. Ahmad, and G. Martin, “Petiroc, a new front-end ASIC for time of flight application,” *IEEE Nuclear Science Symposium Conference Record*, pp. 0–4, 2013.

[58] J. Fleury, S. Ahmad, C. De La Taille, S. Callier, and L. Raux, “LIROC : Novative RadHard Front-End ASIC for Lidar,” *ATTRACT Final Conference*, 2021. [Online]. Available : https://phase1.attract-eu.com/showroom/project/novative-radhard-front-end-asic-for-lidar-liroc/

[59] PETsys Electronics, “TOFPET2 : a high-performance ASIC for time and amplitude measurements of SiPM signals in time-of-flight applications,” 2020. [Online]. Available : https://www.petsyselectronics.com/web/website/docs/products/product1/TOFPET2_Overview.pdf

[60] S. Ahmad, C. De La Taille, J. Fleury, N. Seguin-Moreau, L. Raux, S. Callier, G. Martin-Chassard, F. Dulucq, and D. Thienpont, “Triroc, a versatile 64-channel SiPM readout ASIC for time-of-flight PET,” *2016 IEEE Nuclear Science Symposium, Medical Imaging Conference and Room-Temperature Semiconductor Detector Workshop, NSS/MIC/RTSD 2016*, vol. 2017-Janua, pp. 1–5, 2017.

[61] D. Thienpont, “H2GCROC3 Datasheet,” *CMS - EDMS 2608576*, vol. CMS-CE-ES-, 2022. [Online]. Available : https://edms.cern.ch/ui/file/2608576/1/H2GCROC3_datasheet_1_4.pdf

[62] J. González-Martínez, “Nuclear Inst . and Methods in Physics Research , A H2GCROC : Design and performance of a dedicated very front-end ASIC for SiPM readout of the CMS High Granularity Calorimeter,” *Nuclear Inst. and Methods in Physics Research, A*, vol. 1047, p. 167863, 2023.

[63] D. Thienpont, “HGCROC3-Si Datasheet,” *CMS - EDMS 2608576*, vol. CMS-CE-ES-, pp. 1–95, 2022. [Online]. Available : https://edms.cern.ch/ui/file/2608576/1/HGCROC3_datasheet_v1.pdf

[64] K. Briggl, H. Chen, D. Schimansky, W. Shen, V. Stankova, and H. C. Schultz-Coulon, “KLauS : A low power Silicon Photomultiplier charge readout ASIC in 0.18 UMC CMOS,” *Journal of Instrumentation*, vol. 11, no. 3, 2016.

[65] P. Fischer, I. Peric, M. Ritzert, and M. Koniczek, “Fast self triggered multi channel readout ASIC for time- and energy measurement,” *IEEE Transactions on Nuclear Science*, vol. 56, no. 3, pp. 1153–1158, 2009.

[66] M. Firlej, T. Fiutowski, M. Idzik, S. Kulis, J. Moron, and K. Swientek, “A fast, ultra-low and frequency-scalable power consumption, 10-bit SAR ADC for particle physics detectors,” *Journal of Instrumentation*, vol. 10, no. 11, 2015.

[67] F. Bouyjou, E. Delagnes, F. Couderc, D. Thienpont, and J. D. Gonzalez-Martinez, “A 3-step Low-latency Low-Power Multichannel Time-to-Digital Converter based on Time Residual Amplifier,” *IEEE Transactions on Nuclear Science*, pp. 1–16, 2023.

[68] F. Bouyjou, “Multi-channel TDC for HGROC : ToA and ToT proposed architecture,” *Institute of Research into the Fundamental Laws of the Universe*. *CEA-Saclay*, pp. 1–9, 2018. [Online]. Available : https://gitlab.cern.ch/CMS_HGCROC_tests/CMS_HGCROC_test_FW/-/blob/HGCROCv2/_Documentation/HGCROCv2/PLL_and_TDC/HGCROC_TOA_TOT_PLL_SPECIFICATIONS.pdf

[69] Cadence, “Virtuoso Layout Suite,” Cadence, Tech. Rep., 2023. [Online]. Available : https://www.cadence.com/en_US/home/tools/custom-ic-analog-rf-design/layout-design/virtuoso-layout-suite.html

[70] NKT Photonics, “PILAS DX. Picosecond pulsed diode lasers,” NKT Photonics, Tech. Rep., 2021. [Online]. Available : https://contentnktphotonics.s3-eu-central-1.amazonaws.com/Datasheets/PILAS/ALS_Pilas_DX.pdf?1615815852%0A

[71] Kambic, “Kambic Temperature Chamber TK-105 CKLT,” Kambic, Tech. Rep., 2016. [Online]. Available : https://kambicmetrology.com/wp-content/uploads/2016/03/Technical-data-sheet-TEMPERATURE-CHMBER-LOW-TEMPERATURE.pdf

[72] A. Fassò, A. Ferrari, J. Ranft, and P. Sala, “FLUKA,” INFN, Tech. Rep., 2005. [Online]. Available : http://www.fluka.org/fluka.php

[73] A. Ferrari, P. R. Sala, A. Fasso, and J. Ranft, “FLUKA : A multi-particle transport code (Program version 2005),” 10 2005.

[74] CERN, “ObeliX EP-ESE irradiation system,” CERN, Tech. Rep., 2017. [Online]. Available : https://espace.cern.ch/project-xrayese/_layouts/15/start.aspx#/ObeliX/Forms/AllItems.aspx

[75] ——, “AsteriX EP-ESE irradiation system,” CERN, Tech. Rep., 1997. [Online]. Available : https://espace.cern.ch/project-xrayese/_layouts/15/start.aspx#/AsteriX/Forms/AllItems.aspx

[76] F. Faccio, “Nuclear Inst . and Methods in Physics Research , A ASIC survival in the radiation environment of the LHC experiments : 30 years of struggle and still tantalizing,” *Nuclear Inst. and Methods in Physics Research, A*, vol. 1045, no. October 2022, p. 167569, 2023. [Online]. Available : https://doi.org/10.1016/j.nima.2022.167569

[77] UCLouvain, “Heavy Ion Facility (HIF),” UCLouvain Cyclotron Resource Centre, Tech. Rep., 1971. [Online]. Available : https://uclouvain.be/en/research-institutes/irmp/heavy-ion-facility-hif.html

[78] A. Nantes, “CYCLOTRON C70 ARRONAX,” Arronax Nantes, Tech. Rep., 2011. [Online]. Available : https://www.arronax-nantes.fr/production-des-radionucleides/equipement/cyclotron-c70/

[79] E. Vernazza, “Irradiation testing of HGCROC3 : TID and SEE performance,” LLR / CNRS / CMS, Tech. Rep., 2022. [Online]. Available : https://indico.cern.ch/event/1228307/contributions/5168477/attachments/2563488/4419608/PRR_HGCROCv3_TID-SEE.pdf

[80] ——, “Proton irradiation testing of HGCROC3,” LLR / CNRS / CMS, Tech. Rep., 2023. [Online]. Available : https://indico.cern.ch/event/1258903/contributions/5287985/attachments/2601542/4492136/SEE%20Proton%20Irradiation.pdf

[81] M. De Silva and G. Milella, “DESY March Data Taking Log,” DESY, Tech. Rep., 2023. [Online]. Available : https://readthedocs.web.cern.ch/pages/viewpage.action?spaceKey=HBT&title=DESY+March+Data+Taking+Log

[82] M. de Silva, J.-H. Li, G. Milella, and D. Selivanova, “Studies with 9mm² SiPM on Tileboards,” DESY, Tech. Rep., 2023. [Online]. Available : https://indico.cern.ch/event/1334650/contributions/5637242/attachments/2740720/4767320/hgcal_week_9mm_studies_2510.pdf

[83] C. De La Taille, G. Martin-Chassard, and L. Raux, “FLC-SIPM : Front-end chip for SIPM readout for ILC analog HCAL,” *LCWS 2005 - 2005 International Linear Collider Workshop*, pp. 3–10, 2005.

[84] M. Reinecke, “Tileboards for CMS HGCAL.” *HGCAL workshop*, 2021. [Online]. Available : https://indico.cern.ch/event/977902/contributions/4137069/attachments/2159659/3643462/HGCAL_workshop_Dec20_reinecke.pdf

[85] C. De la Taille, “Front-End Electronics for timing,” Omega Microelectronics. IEEE/NSS-MIC short course, Tech. Rep., 2023. [Online]. Available : https://cernbox.cern.ch/pdf-viewer/public/ZK5lRelOXZX9Rya/CdLT_IEEE_2023C.pdf

[86] V. Stankova, W. Shen, K. Briggl, H. Chen, P. Fischer, A. Gil, T. Harion, V. Kiworra, Y. Munwes, M. Ritzert, and H. C. Schultz-Coulon, “STIC3 - Silicon Photomultiplier Timing Chip with picosecond resolution,” *Nuclear Instruments and Methods in Physics Research, Section A : Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 787, pp. 284–287, 2015. [Online]. Available : http://dx.doi.org/10.1016/j.nima.2014.12.073

[87] “The time structure of hadronic showers in highly granular calorimeters with tungsten and steel absorbers,” *Journal of Instrumentation*, vol. 9, no. 7, 2014.

[88] S. Gomez, J. M. Fernandez-Tenllado, J. Alozy, M. Campbell, R. Manera, J. Mauricio, A. Mariscal, C. Pujol, D. Sanchez, A. Sanmukh, A. Sanuy, R. Ballabriga, and D. Gascon, “FastIC : A Highly Configurable ASIC for Fast Timing Applications,” *2021 IEEE Nuclear Science Symposium and Medical Imaging Conference Record, NSS/MIC 2021 and 28th International Symposium on Room-Temperature Semiconductor Detectors, RTSD 2022*, pp. 9–12, 2021.

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Acronyms

ADC - Analog-to-digital converter
ALICE - A Large Ion Collider Experiment
APD - Avalanche photodiode
ASIC - Application-Specific Integrated Circuit
ATLAS - A Toroidal LHC Apparatus
BX - Bunch crossing
CALICE - Calorimeter for Linear Collider Experiments
CC - Current conveyor
CD - Common drain
CEA - Alternative Energies and Atomic Energy Commission
CE-E - Electromagnetic End-Cap calorimeter
CE-H - Hadronic End-Cap calorimeter
CERN - The European Organization for Nuclear Research
CF - Current Follower
CG - Common gate
CM - Current Mirror
CMOS - Complementary metal-oxide-semiconductor
CMS - Compact Muon Solenoid
CRC - Cyclic redundancy check
CS - Common source
DAC - Digital-to-Analog converter
DAQ - Data acquisition
DESY - Deutsches Elektronen-Synchrotron
DLL - Delay-locked loop
DNL - Differential Non-linearity
EC - Event Counter
ENC - Equivalent Noise Charge
eV - electron Volt
FCU - Fast Command Unit
FIFO - First-in First-out
FPGA - Field-programmable gate array
FSM - Finite state machine
FWHM - Full Width at Half Maximum
GBW - Gain Bandwidth
H2GCROC - High granularity calorimeter Read-out Chip SiPM version
HCAL - Hadronic calorimeter
HGCAL - High granularity calorimeter
HGCROC - High granularity calorimeter Read-out Chip
HIF - Heavy Ion Facility
HL-LHC - High Luminosity Large Hadron Collider
I²C - Inter-Integrated Circuit
IF - Inversion Factor
ILC - International Linear Collider
IN2P3 - The National Institute of Nuclear and Particle Physics
INL - Integral Non-linearity
IRFU - Institute for Research on the fundamental laws of the universe
L1A - Level 1 Accept
LED - Light emitting diode
LHC - Large Hadron Collider
LHCb - Large Hadron Collider beauty
LINAC - Linear accelerator
LIROC - Lidar Read-out Chip
LLR - Laboratoire Leprince-Ringuet
LpGBT - Low power GigaBit Transceiver
LSB - Less-significant Bit
MIM - Metal-Insulator-Metal
MIP - Minimum Ionizing particle
MOS - Metal-oxide-semiconductor
MSB - Most-significant Bit
NMOS - Metal-oxide-semiconductor N-type
OC - Orbit Counter
OMEGA - Organization for Micro-Electronics Design and Applications
p.e. - photo-electron
PA - Preamplifier
PCB - Printed Circuit Board
PET - Positron Emission Tomography
PM - Phase margin

PMOS - Metal-oxide-semiconductor P-type
POR - Power-On-Reset
QCD - Quantum Chromodynamics
QED - Quantum Electrodynamics
QFD - Quantum Flavour dynamics
RAM - Random-access memory
RC - Resistor-capacitor
RF - Radio-Frequency
RFA - Radio-Frequency Amplifier
RMS - Root Mean Square
SAR - Successive Approximation Register
SEE - Single Event Effect
SEL - Single Event Latchup
SET - Single Event Transient
SEU - Single Event Upset
SH - Shaper
SiPM - Silicon Photo-Multiplier
SNR - Signal-to-noise Ratio
SoC - System-on-chip
SPAD - Single-photon Avalanche Diode
SPIROC - SiPM Integrated Read-out Chip
SPS - Single photon spectrum
SPTR - Single photon time resolution
TB - Tileboard
TDC - Time-to-digital converter
TIA - Trans-impedance Amplifier
TID - Total Ionizing Dose
TOA - Time of arrival
TOF - Time-of-flight
TOT - Time over threshold
TSMC - Taiwan Semiconductor Manufacturing Corporation
UGC - Unity Gain Cell
VF - Voltage Follower
VM - Voltage Mirror
VPA - Voltage preamplifier
VPI - Vacuum phototriodes

ECOLE
DOCTORALE

Titre : Conception et caractérisation d'ASIC de lecture des détecteurs SiPM dans des mesures de temps pico-seconde pour l'expérience CMS HGCAL

Mots clés : ASIC, SiPM, Front-end analogique, CMS, HGCAL, Physique des particules

Résumé : Les ASIC HGCROC sont des composants électroniques frontaux dédiés, conçus pour lire le calorimètre à haute granularité (HGCAL), qui remplacera les calorimètres actuels du Grand collisionneur de hadrons (LHC) dans le cadre de la collaboration sur le solénoïde compact à muons (CMS). Ce travail met l'accent sur les caractéristiques spécifiques de la conception du HGCAL qui ont influencé la conception de l'ASIC de lecture du photomultiplicateur au silicium (SiPM).
H2GCROC est un ASIC 130 nm CMOS conçu pour lire les SiPM couplés aux tuiles scintillantes des sections hadroniques arrière de CMS HGCAL. Le préamplificateur frontal à l'intérieur de la puce est adapté au niveau de signal plus élevé du SiPM, anticipant les pC par particule ionisante minimale (MIP) au lieu des gammes fC/MIP. Cette thèse présente l'architecture ASIC et sa caractérisation en laboratoire et en faisceau d'essai. Elle démontre une bonne adaptabilité dans l'étalonnage, la tolérance au rayonnement et la capacité de mesurer le spectre de photons uniques du SiPM et l'énergie du MIP avec une haute résolution. Ce travail illustre également les améliorations proposées, développées et testées entre la deuxième et la troisième version imprimée de l'ASIC et les changements futurs de la prochaine et dernière version de l'ASIC.

Title : Design and characterization of readout ASICs for SiPM detectors in pico-second timing measurements for the CMS HGCAL experiment

Keywords : ASIC, SiPM, Analog front-end, CMS, HGCAL, Particle physics

Abstract : The HGCROC ASICs are dedicated very front-end electronics designed to read out the High Granularity Calorimeter (HGCAL), which will replace the current end-cap calorimeters of the Large Hadron Collider (LHC) for the Compact Muon Solenoid collaboration (CMS). This work emphasizes the specific features of the HGCAL design that influenced the Silicon Photo Multiplier (SiPM) readout ASIC design.
H2GCROC is a 130nm CMOS ASIC designed to read out the SiPMs coupled to the scintillating tiles of the back hadronic sections of CMS HGCAL. The front-end preamplifier inside the chip is tailored for the SiPM's higher signal level, anticipating pC per Minimum Ionizing Particle (MIP) instead of fC/MIP ranges. This thesis presents the ASIC architecture and its characterization in the lab and test beam. It demonstrates good adaptability in calibration, radiation tolerance, and the ability to measure SiPM single-photon-spectrum and MIP's energy with high resolution. This work also illustrates the improvements proposed, developed, and tested from the second to the third fabricated version of the ASIC and the future changes of the following and last ASIC version.

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