Evaluation of Electromagnetic Hazards due to Environmental Stresses, Obsolescence and/or Ageing, Evaluation at the IC Level

Qazi Mashaal Khan

To cite this version:

Qazi Mashaal Khan. Evaluation of Electromagnetic Hazards due to Environmental Stresses, Obsolescence and/or Ageing, Evaluation at the IC Level. Electronics. INSA de Rennes, 2023. English. NNT : 2023ISAR0025 . tel-04695989

HAL Id: tel-04695989
https://theses.hal.science/tel-04695989v1

Submitted on 12 Sep 2024

COLLEGE DOCTORAL BRETAGNE
MATHS, TELECOMS
INFORMATIQUE, SIGNAL
SYSTEMES, ELECTRONIQUE

INSA INSTITUT NATIONAL DES SCIENCES APPLIQUÉES RENNES

THESE DE DOCTORAT DE

L'INSTITUT NATIONAL DES SCIENCES APPLIQUEES RENNES

ECOLE DOCTORALE N° 601
Mathématiques, Télécommunications, Informatique , Signal, Systèmes, Electronique
Spécialité : *Electronique*

Par
Qazi Mashaal KHAN

Evaluation of Electromagnetic Hazards due to Environmental Stresses, Obsolescence and/or Ageing, Evaluation at the IC Level

Thèse présentée et soutenue à l'ESEO Angers, le 31 janvier 2023
Unité de recherche : IETR – ESEO Angers
Thèse N° : 23ISAR 04 / D23 - 04

Rapporteurs avant soutenance :

Davy PISSOORT	Professeur (Hoogleraar), KU Leuven, Bruges Campus (Belgique)
Alexandre BOYER	Maître de Conférences (HDR), INSA Toulouse – LAAS-CNRS

Composition du Jury :

Président :	Bruno CASTANIER	Professeur des Universités, Université d'Angers – LARIS
Examinateurs :	Davy PISSOORT	Professeur (Hoogleraar), KU Leuven, Bruges Campus (Belgique)
	Alexandre BOYER	Maître de Conférences (HDR), INSA Toulouse – LAAS-CNRS
	Sonia BEN DHIA	Professeur des Universités, INSA Toulouse – LAAS-CNRS
	Philippe BESNIER	Directeur de Recherche CNRS, INSA Rennes – IETR
	André DURIER	Senior Expert CEM, Continental Automotive (QL-EMC)
	Mohammed RAMDANI	Enseignant-chercheur (HDR), ESEO – IETR
Co-Encadrant :	Hugo PUES	Senior Development Engineer EMC, Melexis NV (Belgique)

Invité(s)

Dir. de thèse :	Richard PERDRIAU	Enseignant-chercheur (HDR), ESEO – IETR
Co-Encadrant :	Mohsen KOOHESTANI	Enseignant-chercheur, ESEO – IETR

Pan-European Training, research and education network
on ElectroMagnetic Risk management.

Title of the thesis:

Evaluation of Electromagnetic Hazards due to Environmental Stresses, Obsolescence and/or Ageing, Evaluation at the IC Level

Qazi Mashaal Khan (ESR 7)

This project has received funding from the European Union's EU Framework Programme for Research and Innovation Horizon 2020 under Grant Agreement No. 812.790

ACKNOWLEDGEMENTS

First and foremost, my most profound appreciation goes to my two supervisors, Dr. Richard Perdriau and Dr. Mohsen Koohestani from ESEO, for many ideas behind this work, their invaluable guidance, encouragement, advise and support throughout this dissertation. It is entirely due to them that I have achieved such milestones during my PhD journey. I would also like to acknowledge Dr. Mohamed Ramdani for his help and feedback on my work during my time at ESEO.

I extend my gratitude to the assessors of my PhD dissertation; Prof. Davy Pissoort (KU Leuven) and Dr. Alexandre Boyer (INSA Toulouse), who thorougly reviewed my manuscript and provided constructive feedback improving the quality of the dissertation. Furthermore, I acknowledge the input and valuable comments provided by remaining members of the doctoral examination committee - Prof. Bruno Castenier (Univ. of Angers), Prof. Philippe Besnier (INSA Rennes), Prof. Sonia Ben Dhia (INSA Toulouse), and Dr. André Durier (Continental).

My warmest thanks to my fellow PETER ESR Lokesh Devaraj from HORIBA MIRA, for his collaboration and support in my PhD work. We were able to successfully combine our expertise in probabilistic models and EMC IC design, which lead us to publish several journal and conference publications. Further, I would like to thank his supervisor Dr. Alastair Ruddle from HORIBA MIRA for all the fruitful exchanges and technical discussions we had.

I am gratefully thankful to the entire EU Horizon 2020 MSCA ETN PETER consortium for letting me be a part of this innovative project focusing on a risk-based EMC approach.

I also acknowledge the help of my secondment supervisors Dr. Hugo Pues from Melexis and Dr. Tim Claeys from KU Leuven for providing me the opportunity to use the test facilities at their respective institutions.

I wish to thank all my PETER fellow ESRs especially Hasan Habib, Pejman Memar (KU leuven), Oskari Leppäaho (Valeo) and Zhao Chen (Barco) for all the good times we have spent together in our PETER journey. It was a pleasure to attend social and technical activities together as a team.

I am most thankful for all the help and unconditional support that I have received from my parents Ahmed and Aisha throughout these years. They always believed in me and despite the distance have always been with me. My appreciation also goes to my two sisters Shandana and Laiba for their love, support and unwavering belief in me. Without you all I would not be the person I am today.

Finally and most importantly, I wish to say a heartful thank you to my dearest wife Shahzadi Hyda for supporting me in every aspect of my work and everyday life. This thesis would not have been possible without her love and support. I dedicate my PhD and all its related achievements to her.

ABSTRACT

Within the lifetime of an integrated circuit (IC), critical environmental conditions can strongly influence its electromagnetic compatibility (EMC) behavior. At the time being, there is no fast, cost-effective method to guarantee that a system can maintain its EMC performance over its full life-time. Further, the conducted continuous-wave EM immunity of ICs is currently being characterized by single-tone EM disturbances. In practice, however, an uncertain EM environment includes multiple disturbance frequencies that could couple into the IC pins, simultaneously causing soft or hard failures.

To accurately characterize and analyze conducted immunity and emission levels at the IC level and utilize a simulation-based transistor-level approach to find the root cause of a failure, a custom-designed IC was developed. For a risk-based EMC approach, multitone EM immunity testing was adopted with the aid of Bayesian network (BN) based probabilistic models and simulations/measurements to characterize the causal interactions and investigate the influence of temperature on these immunities. For the considered case studies, the probability of three-tone failures was predicted using the single-tone and two-tone failure probability values, by a newly proposed improved adaptive recursive noisy-OR (I-ARNOR) model. Additionally, the transient EM immunity of analog IC blocks with similar functionality but different topologies were compared and investigated under the impact of thermal stress.

Existing IC emission model for conducted emisson (ICEM-CE) and IC immunity model for conducted immunity (ICIM-CI) have already been proposed for the anticipation of conducted EMC issues. However, these IC models do not take into account environmental stresses such as aging and thermal stress. Highly accelerated life tests and thermal cycling were performed to validate the effect of aging and thermal stress, respectively, causing deviations in the passive and/or active blocks of these standard models, which were identified and characterized. This paves the way to the inclusion of such deviations in future revised versions of those standards.

RÉSUMÉ ÉTENDU EN FRANÇAIS

Introduction

Pendant le cycle de vie d'un circuit intégré (CI), les conditions environnementales (température, humidité, surtension, etc.) peuvent fortement influencer son comportement en matière de compatibilité électromagnétique (CEM). En outre, l'utilisation de circuits intégrés de différents fabricants (lorsque le circuit intégré d'origine n'est plus disponible pour réparer un équipement) peut également perturber ce comportement, ce qui peut entraîner des défaillances soudaines. à l'heure actuelle, il n'existe pas de méthodes rapides et bon marché pour garantir qu'un système puisse maintenir ses performances en matière de CEM, et plus encore ses exigences de sécurité, lorsque ses caractéristiques EM sont sujettes à des changements dans le temps.

L'immunité EM conduite des CIs peut être actuellement caractérisée par l'injection directe de puissance (DPI) fréquence par fréquence. Dans la pratique, cependant, l'environnement EM comprend des perturbations à de multiples fréquences, qui peuvent se coupler aux broches du CI simultanément et provoquer des défaillances plus ou moins sérieuses. On sait que l'étude de l'effet de deux ou plusieurs perturbations simultanées, c'est-à-dire des perturbations EM multifréquences, bien que connue, n'est utilisée dans l'industrie que pour réduire le temps de test global. Néanmoins, pour une approche de la CEM basée sur le risque ("risk-based"), les essais multifréquences peuvent potentiellement être plus représentatifs de l'environnement EM réel.

En raison de la réduction de la taille des transistors, un CI moderne peut être sensible aux décharges électrostatiques (ESD), ce qui peut entraîner une réduction de sa robustesse intrinsèque. Par conséquent, tous les CI comprennent des dispositifs de protection ESD pour les protéger contre les perturbations EM transitoires. Les variations de température peuvent également influer sur la capacité de protection des dispositifs ESD et, par conséquent, sur les caractéristiques d'immunité des CI. Par conséquent, la stabilité face aux changements de température et l'immunité aux perturbations EM transitoires nécessitent d'être considérées pour garantir un fonctionnement fiable des CI analogiques/numériques.

Afin de prédire le niveau de CEM des CI à l'aide de modèles de simulation, des normes de la Commission électrotechnique internationale (IEC) (c'est-à-dire IEC 62433-4 et IEC 62433-2) ont été proposées pour anticiper les problèmes de CEM en mode conduit. Cependant, ces modèles de CI présentent plusieurs limites car ils ne prennent pas en compte les contraintes environnementales telles que le vieillissement, les contraintes thermiques et l'humidité. Des tests de durée de vie accélérée, tels que les essais de stress hautement accéléré (HAST), pourraient être adoptés pour valider l'effet du vieillissement et du stress thermique spécifiquement sur les blocs passifs et/ou actifs de ces modèles standard.

Cette thèse a pour but de développer des méthodes innovantes et pertinentes pour évaluer le risque EM conduit dû à un changement de comportement au niveau du CI. Ces méthodes doivent inclure des modèles de simulation multiphysiques associés aux mesures en tenant compte des contraintes physiques. De plus, les modèles précités doivent permettre d'étudier l'influence de contraintes environnementales représentant des cas industriels typiques. Les objectifs de cette thèse peuvent être résumés comme suit :

- Conception d'une puce de recherche en technologie silicium sur isolant (SOI), comprenant plusieurs structures analogiques/numériques telles qu'un capteur de tension, un circuit générateur de bruit, des oscillateurs intégrés, des cellules de mémoire vive statique (SRAM) et des verrous (latches), afin d'évaluer son immunité et son émission conduites en simulation et en mesure.

- Caractérisation des immunités EM multifréquences mesurées des oscillateurs intégrés en fonction de la température.

- Validation des modèles probabilistes proposés pour prédire la probabilité de défaillance d'un CI pour les perturbations EM multifréquences d'ordre supérieur.

- Etude de l'effet du boîtier du CI sur l'immunité aux transitoires électriques rapides (EFT) d'oscillateurs intégrés ayant les mêmes dispositifs de protection ESD.

- Caractérisation de l'influence de la température sur l'immunité aux EFT des oscillateurs conçus; identification de la cause racine de la défaillance par le biais de simulations.

- Développement et validation de modèles d'émission et d'immunité conduites des CI, y compris l'effet du vieillissement fortement accéléré et du stress thermique.

Conception de CI

Pour caractériser avec précision les niveaux d'immunité et d'émission conduites au niveau du CI et adopter une approche de type boîte blanche pour trouver la cause racine de la défaillance, un CI spécifique appelé PETER_ESEO a été développé. De dimensions 1.52 mm × 1.52 mm, la puce a été fabriquée en technologie SOI CMOS 180 nm 5 V du fondeur XFAB. La conception et le layout du CI ont été réalisées avec Cadence Virtuoso. Le CI comprend plusieurs structures analogiques telles qu'un capteur de tension avec échantillonneur/bloqueur, un arbre d'horloge en H, des oscillateurs commandés en tension déplétés en courant à 3 et 5 étages (CSVCO), un oscillateur en anneau à 3 et 5 étages (RO), des cellules SRAM de 6T et 9T, des verrous (latches) RS analogiques et numériques, des pads court-circuités et un condensateur de 106 pF. Le circuit PETER_ESEO (qui présente toutes les structures CI avec leurs pads de connexion) est illustré sur la Fig. 1.

La puce est placée dans un boîtier céramique de 64 broches (CQFP). Tous les pads d'alimentation et de masse ont été connectés aux broches du boîtier en les espaçant pour minimiser l'effet de couplage inductif mutuel, ce qui permet d'injecter plus de puissance dans les pads d'alimentation.

Comportement en température des technologies Si bulk et SOI

Afin de caractériser le comportement des technologies Si bulk et SOI, une étude a été effectuée sur le capteur de tension et les cellules de SRAM (6T et 9T) en fonction du process et de la température. Il a été constaté que le capteur en SOI était plus stable et consommait moins, au détriment d'une plus grande sensibilité

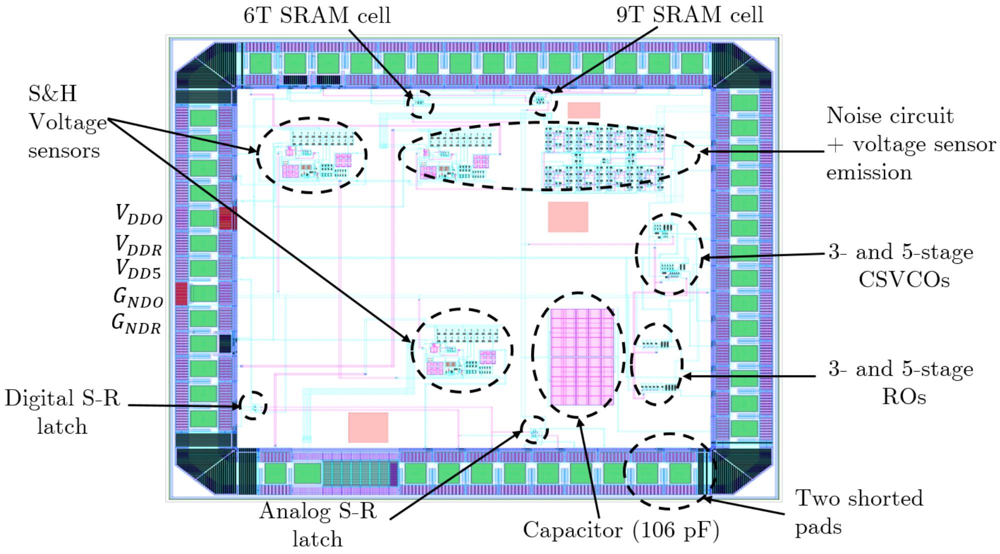


Figure 1: Schéma du CI spécialisé PETER_ESEO conçu en technologie SOI 180 nm 5 V.

aux variations de process et d'une taille plus importante. En ce qui concerne les SRAM, les versions en SOI présentent une plus grande stabilité des données, un courant de fuite et une dissipation plus faibles ainsi qu'une plus grande résilience aux changements de température; par contre, elles sont également plus sensibles aux variations de process et plus encombrantes que leurs contreparties en bulk Si. Les meilleures spécifications ont été observées sur la SRAM 9 transistors en SOI.

Ces résultats démontrent que la plus grande résilience des structures SOI aux stresses thermiques ainsi que leur dissipation de puissance plus réduite semble les rendre prometteuses pour le développement de structures électromagnétiquement robustes.

Analyse de l'immunité EM conduite en multifréquences

Une méthode actuellement utilisée pour le test CEM des CI en immunité conduite est la DPI (injection de perturbations monofréquence dans les broches du CI). Cependant, comme des perturbations sont susceptibles de se produire simultanément à plusieurs fréquences dans un système réel, des effets supplémentaires

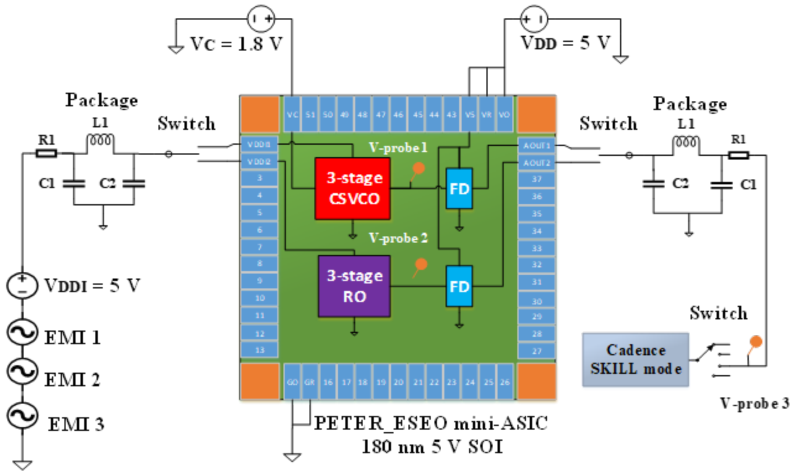


Figure 2: Configuration de la simulation EMI multifréquences pour les circuits CSVCO et RO.

d'intermodulation entre ces perturbations EM multifréquences doivent sans doute être pris en compte dans les évaluations d'immunité. Le principal défi de l'analyse de l'immunité multifréquences est le nombre potentiellement infini de combinaisons de fréquences qui peuvent être considérées. Pour les mesures multifréquences, cependant, le nombre de fréquences simultanées qui peuvent être utilisées est limité en raison de la saturation de l'amplificateur et aussi de l'étalonnage nécessaire pour compenser l'atténuations des câbles, qui peut conduire à des incertitudes de mesure supplémentaires. Par conséquent, la simulation et les modèles probabilistes offrent une approche plus pratique pour étudier des ensembles relativement importants de combinaisons de fréquences, ainsi que des ordres supérieurs de multifréquences.

Les oscillateurs intégrés dans des sous-systèmes électroniques tels que les générateurs de fonctions, les boucles à verrouillage de phase (PLL) sont susceptibles d'être soumis à un environnement EM multifréquences. Par conséquent, il est souhaitable d'étudier l'immunité multifréquences de ces blocs afin d'avoir confiance dans leurs performances effectives. L'analyse des niveaux d'immunité d'un CSVCO et d'un RO (intégrés dans le CI PETER_ESEO) va donc prendre en compte les menaces multifréquences et les modèles probabilistes basés sur les réseaux bayésiens (BN). La fréquence de fonctionnement des oscillateurs testés a été utilisée comme critère d'évaluation des performances du circuit vis-à-vis des EMI multifréquences.

Le modèle de simulation consiste en trois sources d'interférences électromagnétiques monofréquence connectées à l'alimentation isolée (V_{DDI}) du bloc simulé (Fig. 2). Des perturbations EM mono ou multifréquences sont injectées dans la broche V$_{DDI}$ de chaque circuit afin de matérialiser la possibilité de leur occurrence simultanée dans l'environnement EM du système réel. Dans les simulations, les perturbations EM multifréquences sont générées par la superposition de fréquences pures. Un circuit diviseur de fréquence numérique (FD) est inclus dans l'étage de sortie des deux oscillateurs pour réduire la fréquence fondamentale du signal généré. Cela permet de surveiller plus facilement la fréquence au niveau de la broche de sortie analogique sans les effets de filtrage dus aux éléments parasites du boîtier. Le circuit FD est alimenté par le V$_{DD}$ principal et est entièrement isolé de l'injection EMI.

Le modèle noisy-OR a été utilisé pour identifier la dépendance causale entre les perturbations EM monofréquence survenant simultanément. Toute différence entre les valeurs de probabilité dérivées des simulations multifréquences et les estimations du modèle noisy-OR indique une violation de l'hypothèse d'indépendance causale. Toute dépendance résultant d'interactions entre des fréquences pures appliquées simultanément peut avoir un impact positif ou négatif sur la probabilité de défaillance du CI.

Si la probabilité de défaillance de la perturbation EM multifréquences est inférieure à l'une des probabilités de l'un des contributeurs fréquentiels purs, alors les fréquences simultanées interagissent pour produire un effet d'annulation, qui est classé comme une interaction de type *inhibition.* En revanche, si la probabilité d'une perturbation EM multifréquences est supérieure à l'une des probabilités de l'une des fréquences pures, alors les fréquences simultanées interagissent pour produire un effet de renforcement, classé comme *causalité positive.* La causalité positive se subdivise en *synergie* et *asynergie.* La première est vraie lorsque la probabilité de perturbation EM multifréquences est supérieure à celle estimée à l'aide du modèle noisy-OR, la seconde dans le cas contraire.

La stabilité face aux variations de température et la sensibilité aux perturbations EM multifréquences nécessitent une attention considérable pour garantir le fonctionnement fiable d'un oscillateur intégré. Les interactions causales dues aux multifréquences et aux contraintes thermiques ont été analysées par des simulations/mesures et par de nouveaux modèles BN proposés. La configuration de mesure en multifréquence est représentée sur la Fig. 3. Des perturbations EM à une, deux et trois fréquences pures ont été injectées dans le composant sous test (DUT) avec une phase initiale choisie aléatoirement entre $-180°$ et $180°$. La sortie de chaque oscillateur a été surveillée, pour les perturbations EM d'entrée ayant la même phase aléatoire, à température ambiante et à des températures extrêmes. La puissance injectée pour chaque fréquence a été maintenue constante à 10 dBm (niveau minimum auquel les deux oscillateurs présentaient un changement observable de la fréquence du signal de sortie) pour limiter le nombre de combinaisons globales de multifréquences. Les proportions des types d'interaction causale pour le CSVCO et le RO à la suite de perturbations EM à deux et trois fréquences à des températures nominales (25 °C) et extrêmes (−40 °C et 120 °C) sont résumées dans les Fig. 4a et 4b, respectivement.

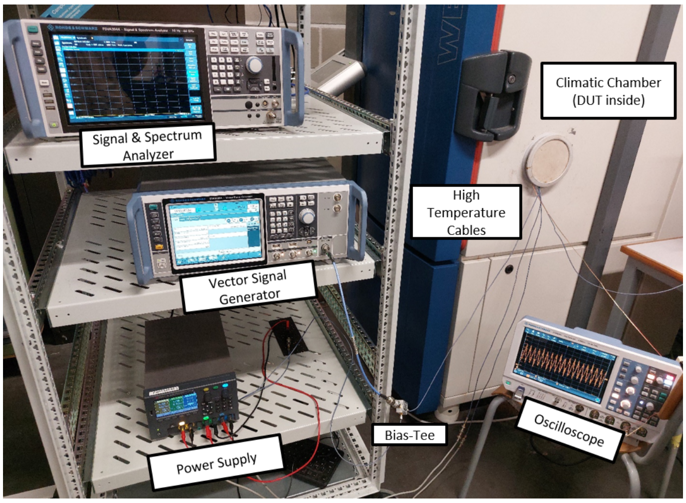
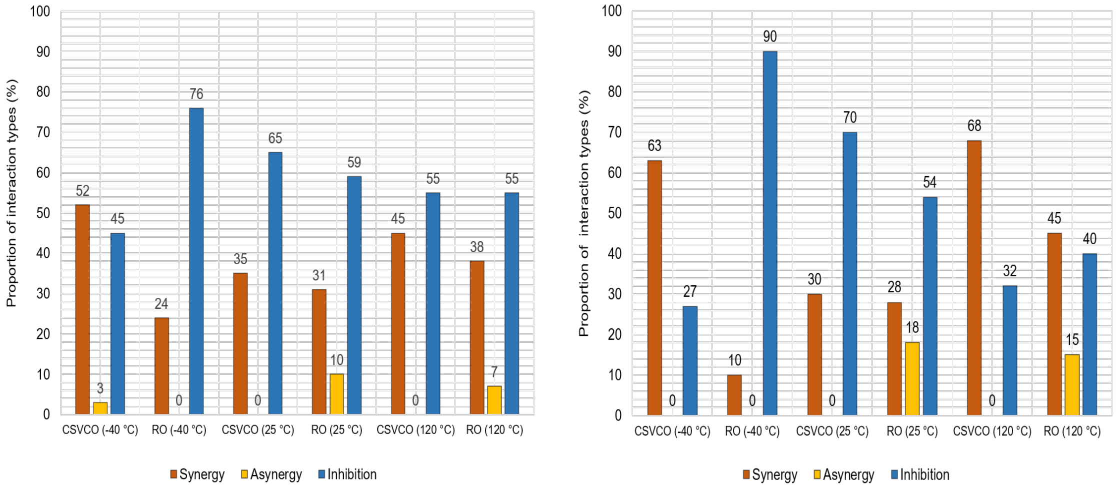


Figure 3: Configuration expérimentale en multifréquences.

à température ambiante, les performances du CSVCO se sont avérées supérieures à celles du RO en raison des proportions d'inhibition légèrement plus élevées pour les perturbations EM à deux et trois fréquences. La plupart des interactions synergiques résultent du verrouillage de la fréquence de sortie sur l'une des fréquences injectées, en particulier pour le CSVCO. Avec l'augmentation du nombre de fréquences, l'effet d'intermodulation s'est traduit par l'augmentation de la proportion d'inhibition pour le CSVCO et d'asynergie pour le RO. Les points d'asynergie ont été principalement observés pour le RO sur l'ensemble du spectre de fréquences testé.

Les variations de température ont entraîné une déviation de la fréquence de sortie des deux oscillateurs, le CSVCO étant plus robuste que le RO. Cependant, les résultats étaient complètement inversés lorsque les effets des EMI multifréquences et de la température étaient combinés. Le CSVCO était nettement plus sensible aux

EMI multifréquences que le RO à des températures extrêmes. En tenant compte de la température, la probabilité de défaillance s'est avérée être la plus faible pour les interactions de type inhibition. Cela a permis de vérifier que la température avait une influence significative sur le boîtier, la capacité du pad d'E/S et le circuit FD du CI.



(a) (b)

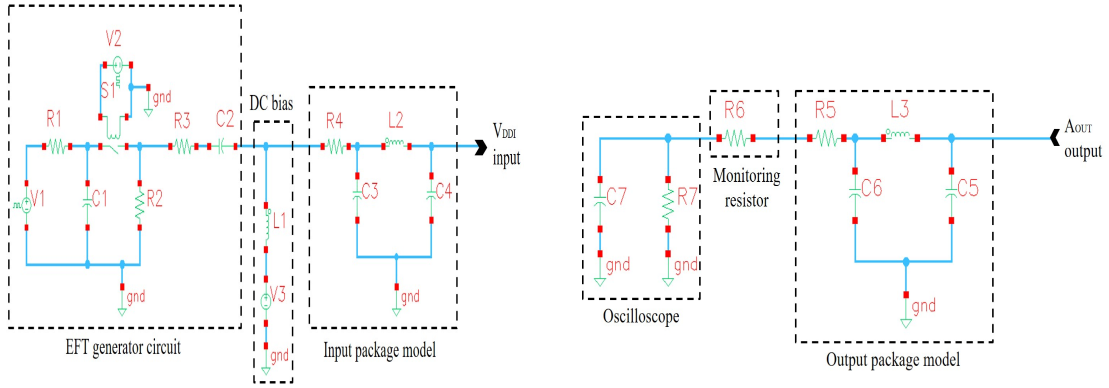
Figure 4: Comparaison des proportions entre les types d'interaction du CSVCO et du RO causée par une perturbation EM multifréquences avec effet cumulé de la température : (a) deux fréquences; (b) trois fréquences.

De plus, l'application de modèles probabilistes tels que le noisy-OR et ses descendants, le adaptive-RNOR (ARNOR), et le improved-ARNOR (I-ARNOR) récemment proposé, a été validée pour la prédiction de la probabilité de défaillance à trois fréquences à partir des valeurs de probabilité de défaillance à une et deux fréquences à des températures nominales et extrêmes. Les valeurs d'erreur de prédiction moyenne et d'écart type obtenues par les modèles ont été appliquées à toutes les interactions multifréquence des oscillateurs à des températures extrêmes. Il a été vérifié que I-ARNOR était le plus précis dans la plupart des cas, avec une erreur de prédiction moyenne et un écart type minimaux. L'utilisation de ces fonctions déterministes complétera et améliorera les normes CEM actuelles qui comprennent des tests d'immunité multifréquences visant uniquement à réduire le temps de mesure, en permettant la prédiction des types d'interactions causales multifréquences et l'estimation des niveaux d'immunité des CI pour des combinaisons non testées de perturbations EM multifréquences.

Analyse de l'immunité EM conduite par EFT

Les tests d'immunité transitoire tels que les transitoires électriques rapides (EFT) définis dans la norme IEC 61000-4-4, sont généralement réalisés dans l'industrie pour vérifier la robustesse des dispositifs ESD. Le signal EFT, constitué d'une série de salves, peut être injecté dans l'alimentation ou les broches fonctionnelles d'un CI par couplage magnétique ou électrique. Cela peut interférer avec le comportement fonctionnel du CI, provoquant par exemple un effet de verrouillage induit par des transitoires ou même des dommages irréversibles.

L'immunité EFT des CSVCO à 3 et 5 étages et d'un RO à 3 étages intégrés) a été comparée et analysée à des températures ambiantes et extrêmes par le biais de simulations et de mesures au niveau du transistor. L'effet du boîtier du CI sur les niveaux d'immunité EFT observés pour chaque oscillateur a également été étudié. En outre, des simulations au niveau du transistor ont été mises en œuvre pour identifier le changement de fréquence de l'oscillateur dû à l'injection EFT et analyser l'effet de l'EFT et du stress thermique sur les caractéristiques des MOSFET.



(a) (b)

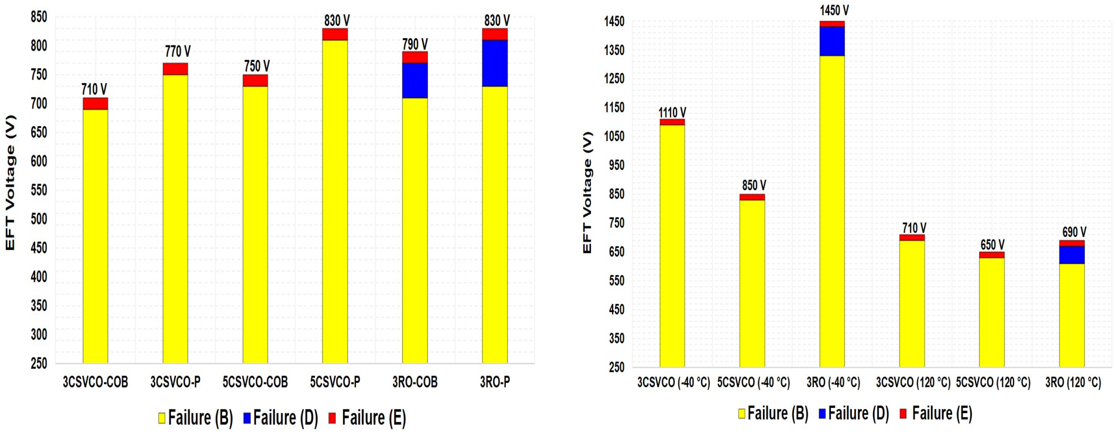
Figure 5: Configuration de la simulation EFT pour la version en boîtier : (a) chemin d'entrée; (b) chemin de sortie.

Dans cette thèse, l'EFT est seulement injecté dans le V_{DDI} de chaque oscillateur. Le banc d'essai de simulation EFT est illustré à la Fig. 5. La simulation a été utilisée pour analyser l'effet du signal EFT sur le comportement en fréquence ainsi que les caractéristiques des MOSFET des oscillateurs considérés à des températures extrêmes.

L'une des alimentations est connectée au coupleur interne du générateur EFT, ce qui permet de superposer la perturbation avec la tension continue (5 V) alimentant la broche V$_{DDI}$ de chaque oscillateur. La V$_{DD}$ est l'alimentation globale qui alimente le padring et le circuit FD. Les deux V$_{DD}$ et V$_{C}$ sont complètement isolés des perturbations EFT injectées. Un capteur de courant, avec une sensibilité nominale de 0.5 V/A, est connecté en série avec le générateur EFT pour surveiller le courant d'entrée injecté au DUT. Le DUT est placé à l'intérieur d'une étuve et la broche de sortie de l'oscillateur testé est connectée à l'un des canaux de l'oscilloscope (1 MΩ) via des câbles haute température. Les tensions de polarité positive et négative de l'EFT varient de 250 V à 2 kV par pas de 20 V, respectivement. Un temps de mesure de 15 s a été donné à chaque niveau EFT afin d'acquérir la tension de sortie et le courant d'entrée de chaque oscillateur à température ambiante.

La fréquence de fonctionnement d'un oscillateur est généralement utilisée pour évaluer sa sensibilité aux perturbations EM harmoniques et peut également être considérée pour caractériser son immunité transitoire. Dans cet article, le critère de défaillance est un écart de $\pm 10\%$ par rapport aux fréquences de sortie nominales des CSVCO et du RO à des températures ambiantes et extrêmes. Les modes de défaillance EFT (A,B,C,D, et E) définis dans la norme IEC-61000-4-4 ont été redéfinis pour évaluer l'immunité EFT des oscillateurs intégrés. En raison de l'utilisation d'alimentations isolées, une défaillance de type E n'a endommagé que le pad d'alimentation de l'oscillateur testé, laissant les autres pads d'alimentation de l'oscillateur non affectés. De plus, les défaillances de type A n'ont jamais été observées, car même à la tension EFT minimale appliquée, tous les oscillateurs fonctionnaient au-delà des limites de tolérance. Par conséquent, la plupart des cas ont donné lieu à des défaillances de type B.

Les résultats des niveaux d'immunité EFT pour les CI encapsulés et COB, et aux températures extrêmes pour les CI encapsulés, sont illustrés dans les Fig. 6a et 6b, respectivement. Selon la topologie de l'oscillateur, des modes de défaillance distincts sont apparus; les types B et E ont été observés pour tous les oscillateurs considérés, tandis qu'une défaillance de type D n'a été constatée que pour le RO, principalement en raison de la limitation de fréquence du circuit FD. De plus, l'analyse a révélé l'importance du boîtier sur les niveaux d'immunité EFT de tous les oscillateurs testés, en raison de l'atténuation de la tension crête EFT injectée. Il a été démontré



(a) (b)

Figure 6: (a) Immunité EFT du CSVCO multi-étages et du RO à température ambiante : en boîtier et COB. (b) Immunité EFT du CSVCO multi-étages et du RO (en boîtier) à des températures extrêmes.

que l'augmentation de la température réduit les niveaux absolus d'immunité EFT pour tous les oscillateurs testés en affectant la capacité de protection des dispositifs ESD. L'oscillateur CSVCO à 5 étages s'est avéré être le plus résistant aux variations de température par rapport aux deux autres oscillateurs. Cependant, les résultats ont été entièrement différents lorsque les oscillateurs ont été soumis à des contraintes combinées d'ESD et de température. Le CSVCO à 5 étages s'est avéré être le plus sensible à l'EFT à des températures extrêmes. De plus, la variation de température sous la contrainte EFT n'a eu aucun impact sur le type de modes de défaillance.

Afin de trouver la cause racine de la défaillance, les caractéristiques des MOSFET de l'étage d'inverseur de sortie, telles que les courants de drain, la résistance drain-source à l'état passant, la dissipation de puissance, μ_{eff} (mobilité effective) et V$_{th}$ (tension de seuil), ont été analysées de manière approfondie en faisant varier la température et la contrainte EFT dans les simulations. La résistance à l'état passant des MOSFETs varie considérablement lorsque la contrainte EFT et les variations de température sont combinées. Cela conduit à une dissipation de puissance accrue, qui peut endommager l'oscillateur par emballement thermique, en particulier pour le CSVCO à 5 étages.

Émission et immunité EM conduites tenant compte du vieillissement et du stress thermique

L'IEC a proposé plusieurs modèles pour évaluer les performances CEM des CI, tels que ICEM-CE (IC Emission Model - Conducted Emission) et ICIM-CI (IC Immunity Model - Conducted Immunity), qui sont publiés sous les références IEC62433-2 et IEC62433-4, respectivement. Comme le montre la Fig. 7a, le modèle ICEM-CE se compose d'un bloc passif appelé réseau de distribution passif (PDN) et d'un bloc actif appelé activité interne (IA). Le premier décrit le réseau d'alimentation d'un CI et montre les chemins de couplage significatifs entre la source de bruit (IA) et les broches externes du CI, tandis que l'IA décrit l'activité du bloc interne du CI en tant que source de courant. Comme on peut le voir sur la Fig. 7b, le PDN du modèle ICIM-CI est identique à celui du modèle ICEM-CE et peut être modélisé par des éléments passifs localisés. De plus, le modèle d'immunité comprend également le bloc comportemental d'immunité (IB) qui est généralement décrit par une table de correspondance entre la puissance injectée et un critère d'immunité prédéfini. Les principales limites de ces modèles sont qu'ils n'incluent ni le vieillissement ni le stress thermique qui peuvent causer une dérive dans les niveaux d'émission conduite et de susceptibilité EM.

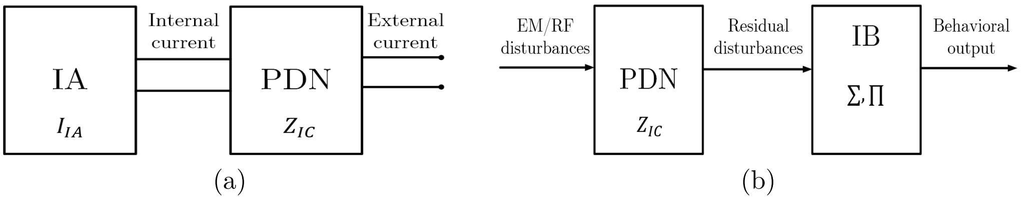


Figure 7: Schémas-blocs des modèles : (a) ICEM-CE ; (b) ICIM-CI.

En raison du vieillissement naturel, les CI peuvent être affectés par des mécanismes de défaillance intrinsèques, tels que l'injection de porteurs chauds (HCI) et l'instabilité négative en température de la polarisation (NBTI). Ces deux derniers sont les effets de dégradation permanente les plus répandus et peuvent être analysés par des tests de durée de vie accélérée. En outre, les variations de température peuvent influencer temporairement les paramètres des MOSFET tels que les niveaux de V$_{th}$ et μ_{eff}, la transconductance et les courants de saturation. Ces variations peuvent déclencher des défaillances et avoir un impact significatif sur les paramètres de stabilité (courant de fuite, marge de bruit, jitter, fréquence de fonctionnement, etc.) du CI. Dans la présente étude, les modèles ICIM-CI et ICEM-CE ont été développés pour des blocs analogiques indépendants intégrés dans le CI. Grâce à des mesures et des simulations au niveau des transistors, l'effet des écarts de température extrêmes et du vieillissement fortement accéléré a été inclus dans les blocs passifs et actifs des modèles proposés.

Pour caractériser l'effet du vieillissement sur le CI considéré, des tests HAST ont été effectués sur plusieurs échantillons. Le test HAST est une version plus accélérée du test de biais température-humidité (THB) (provoquant des modes de défaillance équivalents) et a été réalisé à 130 °C et 85% HR en continu pendant 96 heures. Pour analyser l'effet du stress thermique sur l'émission conduite et l'immunité du CI, des échantillons frais ont été testés à des températures extrêmes (-40 °C et 120 °C) en utilisant une étude.

Pour l'analyse d'émission de l'arbre d'horloge, le générateur de bruit a été utilisé et le modèle ICEM-CE a été extrait par des simulations et des mesures. Un analyseur de réseau vectoriel (VNA) a été utilisé pour mesurer le paramètre (S_{11}) de la broche V_{DDI} de l'arbre d'horloge. Le profil d'impédance Z_{11}, calculé à partir du S_{11}, représente le PDN. Le CI testé ayant été conçu spécifiquement, le courant interne (IA) a été extrait à l'aide de Cadence Virtuoso (approche boîte blanche). Il a ensuite été utilisé sous forme de netlist pour représenter la source de courant du bloc IA du modèle ICEM-CE. La configuration de la simulation ICEM-CE utilisant la méthode 1-Ω est présentée sur la Fig. 8. L'activité du courant externe extraite de la configuration de simulation ICEM-CE et mesurée à l'aide de la méthode 1 Ω est illustrée sur la Fig. 9. Une corrélation significative entre le courant extrait et le courant mesuré a été remarquée. Le courant maximal crête à crête du premier était supérieur de 2,6% au second.

Pour l'analyse d'immunité réalisée, deux blocs analogiques indépendants, une bascule RS et un CSVCO à 3 étages intégrés dans le CI ont été testés. L'extraction de deux PDN distincts via des mesures de paramètres S et de blocs IB par la technique de table de correspondance DPI a été mise en œuvre. Le critère de défaillance considéré pour la bascule RS était de ±10% de l'offset DC avec un temps de mesure de 1 seconde. De même, les variations de 10% de la fréquence ou de la tension crête à crête du CSVCO ont été considérés comme des critères de défaillance DPI.

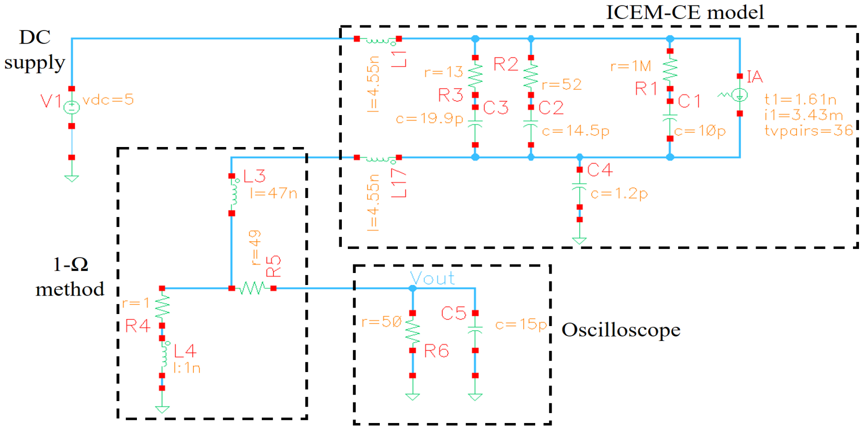


Figure 8: Configuration de la simulation ICEM-CE.

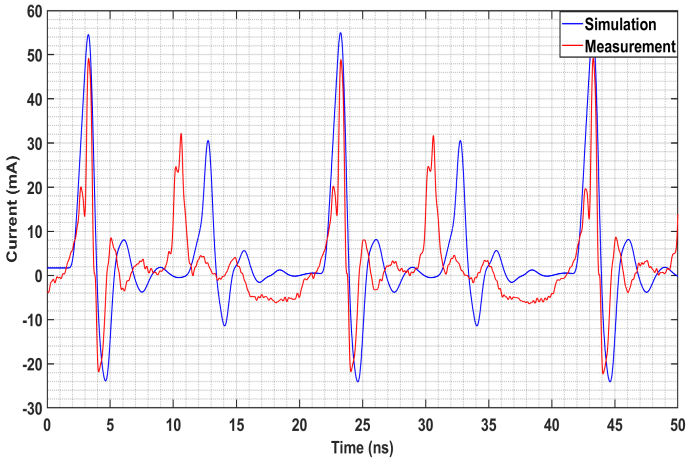


Figure 9: Comparaison du courant externe extrait par la configuration de simulation ICEM et la mesure 1-Ω.

Contrairement au vieillissement HAST, le bloc PDN des modèles développés a été influencé par le stress thermique provoquant des variations dans ses éléments passifs, qui doivent être incluses dans les modèles pour une meilleure précision. Cependant, le vieillissement a provoqué des mécanismes de dégradation permanente (NBTI/HCI), tandis que le stress thermique a eu un impact temporaire sur les caractéristiques des MOSFET qui pourraient provoquer des défaillances du CI. Il a été démontré que ces mécanismes influençaient presque exclusivement les blocs actifs (c'est-à-dire IA et IB) des modèles d'émission et d'immunité conduites.

En appliquant des mesures d'émission conduite par la méthode 1- Ω sur l'arbre d'horloge, il a été démontré que les niveaux d'émission de courant externe se dégradent avec le vieillissement et l'augmentation de la température. Cet effet a été relié à la variation du courant interne (IA) en cas de stress thermique. Il a donc été démontré que des coefficients de proportionnalité constants extraits des simulations (température) et des mesures (vieillissement) pouvaient être inclus dans les blocs IA des modèles. à l'aide de mesures DPI sur deux circuits analogiques indépendants (latch RS et CSVCO), il a été démontré que le vieillissement dû au HAST augmente les niveaux de susceptibilité conduite en fonction de la fréquence, différemment selon la fonctionnalité du bloc analogique. De plus, il a été constaté que le stress dû à la haute température réduit également leurs niveaux d'immunité conduite en fonction des dérives des niveaux V_{th} et μ_{eff}. Des déviations spécifiées dans les tables de correspondance peuvent être appliquées pour inclure l'influence du vieillissement et de la contrainte thermique sur le bloc IB.

Conclusion

Un CI SOI CMOS spécifique (ainsi que des variantes de PCB de mesure) ont été développés afin d'analyser son immunité et son émission en harmonique/transitoire sous contraintes environnementales. En outre, la combinaison de modèles de réseaux bayésiens probabilistes avec des tests multifréquences a été introduite. La probabilité d'une défaillance d'ordre supérieur (nombre de fréquences simultanées) a été prédite à l'aide d'un ordre inférieur, montrant une bonne précision dans les résultats. En outre, l'effet du stress thermique sur le boîtier du CI, la capacité de protection ESD et l'immunité EFT des oscillateurs intégrés avec différentes topologies a été exploré. Enfin, des modèles ICEM-CE et ICIM-CI ont été développés sous l'influence du vieillissement HAST et du stress thermique, ce qui a mis en évidence leur effet sur la partie passive ou active de ces modèles. Cela ouvre la voie à l'inclusion de telles variations dans les futures révisions de ces normes.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

AC	Alternating Current
BN	Bayesian Network
BW	BandWidth
CMOS	Complementary Metal Oxide Semiconductor
COB	Chip On Board
CPD	Conditional Probability Distribution
CQFP	Ceramic Quad Flat Package
CSVCO	Current Starved Voltage Controlled Oscillator
DC	Direct Current
DoS	Degree of Synergy
DPI	Direct Power Injection
DRC	Design Rule Check
DUT	Device Under Test
E/E	Electrical/Electronic
EFT	Electrical Fast Transient
EMC	ElectroMagnetic Compatibility
EMD	ElectroMagnetic Disturbance
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FD	Frequency Divider
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
GCPW	Grounded CoPlanar Waveguide
HAST	Highly Accelerated temperature and humidity Stress Test
HCI	Hot Carrier Injection
HTOL	High Temperature Operating Life
I/O	Input/Output
IA	Internal Activity
I-ARNOR	Improved-Adaptive Recursive Noisy OR

IB	Immunity Behavior
IC	Integrated Circuit
ICEM-CE	Integrated Circuit Emission Model−Conducted Emission
ICIM-CI	Integrated Circuit Immunity Model−Conducted Immunity
ICIM-CPI	Integrated Circuit Immunity Model−Conducted Pulse Immunity
IEC	International Electrotechnical Commission
LTOL	Low Temperature Operating Life
LVS	Layout Versus Schematic
MMCX	Micro Miniature CoaXial
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPD	Marginal Probability Distribution
NBTI	Negative Bias Temperature Instability
PCB	Printed Circuit Board
PDN	Passive Distribution Network
PLL	Phase Locked Loop
PVT	Process Voltage Temperature
RF	Radio Frequency
RO	Ring Oscillator
S&H	Sample and Hold
IA	Internal Activity
SMA	SubMiniature version A
SNM	Static Noise Margin
SoC	System on Chip
SOI	Silicon On Insulator
SOLT	Short Open Load Thru
SR	Slew Rate
S-R	Set−Reset
SRAM	Static Random Access Memory
THB	Temperature Humidity Bias
TRL	Thru Reflect Line
TRM	Thru Reflect Match
VNA	Vector Network Analyzer
WP	Worst Power
WS	Worst Speed

Chapter 1

INTRODUCTION

This chapter deals with the motivation for the research done in this thesis. It is followed by the description of electromagnetic compatibility (EMC) methodology adopted at the integrated circuit (IC) level and the introduction of several terms relevant to EMC. Then, research objectives of this manuscript are highlighted. Afterwards, the organization of the thesis is described. Finally, a list of associated publications, in scientific journals and conferences, is provided.

1.1 Motivation

Current advancements in semiconductor technologies have enabled designers to efficiently design ICs with increasingly improved performance [1]. These ICs have smaller volume, higher density, and increased switching speed, which increase the likelihood for system critical EMC issues due to radiation and conduction [2]. The high-frequency currents and voltages during IC switching activities are often responsible for unintentional emissions or coupling. Further, ICs are also very often the victim of electromagnetic interference (EMI) [3].

Conducted EM immunity of ICs is currently being characterized by direct power injection (DPI), i.e., single-tones [4]. In practice, however, the EM environment include multiple disturbances that could couple into the IC pins simultaneously causing soft or hard failures. The significance of investigating the effect of two or more simultaneously occurring single-tone disturbances, i.e., multitone EM disturbances is only used in industry to reduce the overall test time and is not involved in the conventional EM standards such as DPI [5]. Nevertheless, for a risk-based EMC approach multitone testing may potentially be more representative of the uncertain/real-world EM environment.

Within the lifetime of an IC, environmental conditions (including temperature, humidity, overvoltage stress etc.) can strongly influence its EMC behavior. Moreover, the use of ICs from different manufacturers (when the original IC is not available anymore for repairing a piece of equipment) may also disturb that behavior, which may lead to sudden failures. At the time being, there are no fast and cost-effective methods to guarantee that a system can maintain its EMC performance, even more, so its safety requirements when its EM characteristics are subject to changes over time [6].

Due to downscaling of transistors, a modern IC can be sensitive to electrostatic discharge (ESD) stress, which may lead to the reduction of its intrinsic robustness. Hence, all ICs include ESD protection devices to protect them from transient EM disturbances. Temperature variations can also influence the protection capability of the ESD devices, hence, affecting the IC immunity characteristics [7]. Therefore, stability against temperature changes and immunity to transient EM disturbances, require reasonable attention to ensure reliable operation of analog/digital ICs.

In order to predict the EMC level of ICs using simulation models, existing international electrotechnical commission (IEC) standards (i.e., IEC 62433-4 [8] and IEC 62433-2 [9]) have been proposed for the anticipation of conducted EMC issues. Those models are mainly of interest in case of obsolescence and second sourcing, aiding IC manufacturers to anticipate conducted EMC issues in the design stage and, hence avoiding costly re-design. Beside the prediction of conducted emission and immunity level at the printed circuit board (PCB) level, those models can help to assess and improve the effect of decoupling and filtering networks, the PCB design and the IC configuration. However, such IC models have several limitations since they mainly depend on measurement de-embedding and do not take into account environmental stresses such as aging, themal stress, and humidity [10], [11]. Accelerated life tests, such as highly accelerated temperature and humidity stress testing (HAST), could be adopted to validate the effect of aging and thermal stress specifically on the passive and/or active blocks of those standard models.

1.2 EMC at IC Level

The evolution of the complementary metal oxide semiconductor (CMOS) technology scaling has a major impact on the overall electrical performance of ICs. This is related to the threshold voltage which decreases more slowly than the historical trend and leads to an aggressive design of MOS devices with a very high electric field in the gate oxide. Thereby, in the last decades, manufacturers of devices for critical applications such as automotive, military, naval etc., have contributed to the development of the semiconductor reliability field [12].

The main challenges that can hinder the transistors scaling can be depicted by different categories [13]:

- The physical challenge comes from the increase of the leakage current which induce a negative leverage on the CMOS device functionalities.
- The thermal challenge is due to the rise in the transistor count, which leads to the increase of the power consumption and the need of a higher thermal dissipation.
- The material challenge is mainly related to the ability of the dielectric and the wiring materials to ensure a reliable insulation and conduction.
- The technological challenge results from the lack of competence of lithography-based techniques to afford a resolution below the wavelength of light to manufacture CMOS components.
- The economical challenge related to the increase of the cost of manufacturing more scaled transistors.

The fast operating frequencies and the increased complexity of ICs through the evolution of packaging, the transistors scaling and the wafer process are at the origin of the increase of the noise generated by internal switching events of the circuit which make the device a major source of noise [14]. Advanced research studies are carried on to assess and control the increase of the noise generated by analog/digital components and the study of long-term EMC qualification of ICs has become a major qualification step for semiconductor manufacturers and component vendors.

Before elaborating the topic of EMC at the IC level further, it is important to introduce some relevant terminologies [15]:

- **Electromagnetic environment**: Totality of electromagnetic phenomena existing at a given location.
- **Electromagnetic energy**: It is a form of energy that is reflected or emitted from objects in the form of electrical and magnetic waves that can travel through space.

- **Electromagnetic Disturbance (EMD)**: Electromagnetic phenomenon that can degrade the performance of a device, equipment or system, or adversely affect living or inert matter.

- **Electromagnetic Interference (EMI)**: Degradation in the performance of equipment or transmission channel or a system caused by an electromagnetic disturbance.

- **Electromagnetic Compatibility (EMC)**: It is the ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances that could impair the proper functioning of the devices or systems located in its environment.

- **Electromagnetic resilience**: Techniques and measures adopted to manage functional safety and other risks caused by unforeseeable EM disturbances.

- **Rule-based EMC approach**: It is the compliance with established EM standards for testing the emission and immunity performance of electrical and electronic systems.

- **Risk-based EMC approach**: It follows a systems engineering approach for managing EM risk throughout the life cycle of a device/product/system [16]. It consists of EMC management, control, implementation and verification. This approach provides assurity that a device works safely in its actual EM environment over its entire lifetime. Further details are described and accessible in [17].

Fig. 1.1 illustrates the source-victim model commonly used in EMC studies. It consists of three fundamental blocks which are described as:

- **Source**: the origin of the electromagnetic energy that causes the disturbances (lightning, ESD, high speed data trace, IC, etc.);

- **Coupling path**: the coupling mode that drives the disturbance from the source to the victim (cables, parasitic inductance, parasitic capacitance, antenna, power rails, ground plane, etc.). The coupling path could be either conducted or radiated;

- **Victim**: the receptor of the disturbance that cannot function properly due to the EMI (electronic device, IC, high speed data trace, etc.).

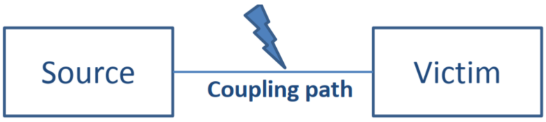


Figure 1.1: Elements causing EMC issues [18].

The two aspects dealt with by EMC studies are:

1. **Emission**: It is the disturbance generated by the component, equipment or the electronic system.
2. **Immunity**: It is the disturbance levels that can cause a malfunction of an electronic device.

These are further divided into four categories:

- **Conducted emission**: where the disturbance produced by the device or an equipment is transmitted to the victim through the wires/cables;
- **Radiated emission**: where the disturbance produced by the device or an equipment is transmitted to the victim through the air;
- **Conducted immunity**: where the disturbance produced by the aggressor is transmitted to the victim through the wires/cables;
- **Radiated immunity**: where the disturbance produced by the aggressor is transmitted to the victim through the air.

To ensure sufficient EMC of the different electronic devices, it is vital to ensure a low emission and high immunity profile. Moreover, ICs degradation due to environmental stress (temperature, humidity, overvoltage, aging, etc.) can have a significant impact on the EMC performance [19]; therefore it is essential to understand the origin and the consequences of both emission and immunity of ICs. Only the conducted modes of the mentioned phenomena is focused on in this manuscript.

1.2.1 EM Emissions of ICs

In electrical systems, different electronic devices can be the source of parasitic emissions. These systems operate in different frequency bands and could alter the radio frequency (RF) communication systems through conducted coupling. ICs are at the core of such complex systems and the origin of the parasitic emissions is mainly due to the variable current consumed during the activation of each logic gate integrated into the IC. The rapid deviation of the amplitude of the current conducted through the supply rails causes large fluctuations in the supply voltage due to the parasitic inductance of the internal IC traces, the bonding wires, the package lead frames, and the PCB traces [18].

The miniaturization of the CMOS circuits over the years has led to an increase in the current consumed when the transistor is in the on-state and a higher leakage current flowing when the transistor is off. In an IC embedded application, a combination of hundreds of thousands logic gates are switching at the same time. This leads to very high current consumption, which is at the origin of the increase of the parasitic emission of the IC [20]. The frequent use of high-performance microcontrollers with several clocks and different frequencies as well as the increase in the operating frequencies of the ICs create a high-frequency parasitic emission spectrum that may disturb sensitive applications [21]. The evaluation of future IC developments is necessary to illustrate the evolution of parasitic emissions to meet the requirements of both manufacturers and customers of ICs. If we do not integrate any EMC optimization strategy, parasitic emissions will tend to increase in the future with advancement in circuit designs.

1.2.2 EM Immunities of ICs

The EM immunity is the ability of an electrical device, equipment, system or IC to perform without error, loss of performance or degradation in the presence of an EM disturbance. It is vital to recognize the difference between immunity and susceptibility, where the latter has the opposite meaning but can be used interchangeably to describe the same phenomenon as the former. Several physical phenomena may be at the origin of the immunity of the IC. The main sources of EM disturbances produced by the electronic components, cell phones, radars, and the ICs themselves can cause interference/malfunction in the surrounding/adjacent ICs [22]. These EM aggressions may also cause functional problems and eventually lead to the integral deterioration of the IC. In some cases, the energy of the generated noise is not sufficient to permanently modify the electrical/technological characteristics of ICs. Hence, the effect of the EMI on the IC could be distinguished by two types of failure i.e., soft and hard failures [23]. The latter occur when a coupled EM disturbance exceeds the acceptable limit of the IC and generates a temporary malfunction of the circuit and only recovers when the EMI is interrupted or the IC is reset. A hard failure happens when the coupled EM disturbance causes a permanent damage or the destruction of the IC.

The EM disturbances that determine the immunity profile of the IC comprise of continuous-wave, pulse and high energy stress [24]. In digital ICs, the switching that occurs from the pulse stress can be generated in different ways and can cause various malfunctions/errors in the reception and the transmission of data on the inputs/outputs (I/Os) of the IC. This can lead to the interruption of the digital IC operation and the loss of the data stored in memory. Continuous stress may result from exposure to a high frequency signal that has small amplitude in a sinusoidal waveform and that can be modulated in amplitude. As a consequence, the IC disturbance level increases which can lead to an alteration of the functioning of the component in different ways, depending on the nature of the internal blocks. Additionally, these continuous EM disturbances may also cause shift in threshold voltages of the transistors in the internal mixed-signal circuits [25].

In contrast, high energy stress results from overvoltage coupling that can trigger specific non-linear elements of the IC such as ESD protection devices, eventually clamping the signal between the supply rail and/or ground rails. The disturbance could occur through the application of sufficient energy to cause a local heating of the IC [26]. The application of a high energy perturbation on a transistor may cause an avalanche effect due to the exceeding of the operating voltage limit at the terminals of the junctions or the channel of the circuit. This phenomenon may either cause premature aging of the internal transistors or the complete destruction of the IC pads/pins.

The reduction of the power supply and the operating frequencies of the ICs tends to reduce the noise margins and the switching thresholds of the analog/digital circuits, which makes them very sensitive to conducted EM disturbances. The EMI can be induced by direct coupling of the EM disturbance on the I/Os or on the

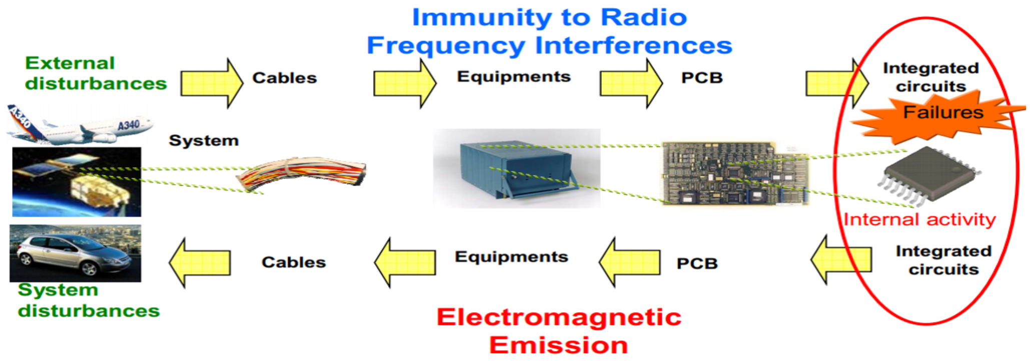


Figure 1.2: External disturbances effecting the conducted EM immunity and emission of ICs [27].

power or ground pins. Hence, IC performances without EMC optimization have very reduced immunity levels that decreases with the technology evolution [27]. The application of EMC design rules can help develop robust ICs with higher immunity margins.

To summarize, with the significant evolution in IC technology, the performance of electronic devices has considerably improved these past decades. At the same time, ICs have become an important source of EMC problems for electrical and electronic systems. Moreover, semiconductor devices are usually the source and also simultaneously the victim of EM disturbances. Since the interference could be coupled through cables and PCB tracks, troubleshooting EMC at the circuit level should consider not only the IC but also the PCB and other filtering/decoupling passive devices as shown in Fig. 1.2. This manuscript focuses only on conducted EM emission and immunity of ICs.

1.3 Thesis Objectives

This thesis aims to develop relevant innovative methods to assess the conducted EM risk due to a change of behavior at the IC level. Those methods should include multiphysics simulation models associated with the measurements considering physical constraints. Moreover, the aforementioned models should make it possible to study the influence of environmental stresses representing typical industrial cases. The objectives of this thesis can be summarized as follows:

- Design a research chip in silicon-on-insulator (SOI) technology, including several analog/digital structures such as a voltage sensor, noise generator circuit, integrated oscillators, static random access memory (SRAM) cells, and latches, in order to evaluate its conducted immunity/emission in simulations and measurements.

- Investigate through simulations the robust stability characteristics of circuits designed in SOI compared to the conventional bulk technology. That work aims to demonstrate why circuits designed in SOI have low power dissipation and higher endurance to temperature variations in comparison to bulk ICs.
- Provide the theoretical framework for the Bayesian network (BN) based analysis of multitone immunity and validate proposed probabilistic models to predict the probability of IC failure for higher order multitone EM disturbances.
- Investigate and characterize the effect of multitone (compared to single-tone) EM interactions in two different oscillator designs under the influence of temperature deviations.
- Clarify the EMC risk due to obsolescence of pin compatible microcontrollers and their respective transient EM immunity.
- Explore and characterize the influence of temperature on the electric fast transient (EFT) immunity of integrated oscillators having the same ESD protection devices and identify the root cause of failure through simulations.
- Improve and validate IC conducted emission and immunity models including the effect of highly accelerated aging and thermal stress.

1.4 Organization of the Thesis

The thesis is organized in seven chapters, the present chapter being Chapter 1.

Chapter 2 describes the custom-designed IC fabricated in 180 nm 5 V SOI technology. The IC includes analog structures such as sample and hold (S&H) voltage sensor, integrated oscillators, SRAM cells, and S-R latches with isolated power supplies benefiting from SOI technology. Furthermore, this chapter includes the design of PCB variants for conducted immunity/emission measurements and S-parameter testing to extract the impedance profile of the IC.

Chapter 3 presents two independent case studies (S&H voltage sensors and 6T/9T SRAM cells) designed in SOI and bulk technologies with the aim to compare their robustness to process variations in transistor parameters during fabrication, electrical overstress and temperature deviations. The stability metrics such as power consumption, leakage current, slew rate and noise margins are extensively analyzed for each technology.

Chapter 4 highlights the importance and challenges of multitone EM testing and introducing BN based probabilistic models to identify the type of causal interactions. Moreover, the conducted multitone EM immunity of integrated oscillators with different topologies are characterized in simulations and measurements. Additionally, the impact of extreme temperatures on the causal interactions and multitone immunity levels is explored. A new derivative of the noisy-OR model is introduced to accurately predict the probability of IC failure for higher order EM multitones.

Chapter 5 investigates about EFT immunity of microcontrollers and the importance of obsolescence in EMC risk management with the aim to show if a modern pin compatible microcontroller is more prone to transient EM disturbance than the previous one. Moreover, the EFT immunity of integrated oscillators having the same ESD protection devices but different topologies is compared and analyzed. The latter study also includes the influence of thermal stress and root cause analysis of oscillator failures due to EFT.

Chapter 6 gives an overview on conducted EM immunity and emission models, with their limitations. The concept of environmental stresses particularly aging and temperature is involved in validating these models. This study paves the way of including aging and thermal stress in future versions of those standards.

Chapter 7 summarizes the main conclusions of the thesis and gives a perspective of possible future research directions.

1.5 Publications

The results of the research presented in this dissertation have led to the following peer reviewed journal and conference publications. Figures and results from these publications are clearly referenced and marked by a © to show that they are the author's own work.

Journal Papers (peer-reviewed)

1. L. Devaraj, **Q. M. Khan**, A. Ruddle, A. Duffy, R. Perdriau, and M. Koohestani, “Improvements proposed to noisy-OR derivatives for multi-causal analysis: A case study of simultaneous electromagnetic disturbances,” *International Journal of Approximate Reasoning*, 2023, (accepted with revision).

2. **Q. M. Khan**, M. Koohestani, J. -L. Levant, M. Ramdani, and R. Perdriau, “Validation of IC conducted emission and immunity models including aging and thermal stress,” *IEEE Transactions on Electromagnetic Compatibility*, 2023, doi: 10.1109/TEMC.2023.3253385.

3. **Q. M. Khan**, M. Koohestani, and R. Perdriau, “Influence of temperature on the EFT immunity of multistage integrated oscillators,” *IEEE Transactions on Electromagnetic Compatibility*, 2022, doi: 10.1109/TEMC.2022.3225540.

4. L. Devaraj, **Q. M. Khan**, A. Ruddle, A. Duffy, R. Perdriau, and M. Koohestani, “Application of probabilistic models for multitone electromagnetic immunity analysis,” *IEEE Transactions on Electromagnetic Compatibility*, 2022, doi: 10.1109/TEMC.2022.321145.

5. **Q. M. Khan**, L. Devaraj, R. Perdriau, A. Ruddle, T. Claeys, M. Ramdani, and M. Koohestani, “Experimental characterization of multitone EM immunity of integrated oscillators under thermal stress,” *IEEE Access*, 2022, doi: 10.1109/ACCESS.2022.3197659.

6. **Q. M. Khan**, L. Devaraj, M. Koohestani, A. Ruddle, M. Ramdani, and R. Perdriau, “Synergistic effect of multitone EMI on the conducted immunity of integrated oscillators,” *IEEE Letters on Electromagnetic Compatibility Practice and Applications*, 2022, doi: 10.1109/LEMCPA.2022.3175433.

7. **Q. M. Khan**, R. Perdriau, M. Ramdani, and M. Koohestani, “A comparative performance analysis of 6T & 9T SRAM integrated circuits: SOI vs. Bulk,” *IEEE Letters on Electromagnetic Compatibility Practice and Applications*, 2022, doi: 10.1109/LEMCPA.2022.3163963.

Conference Papers (peer-reviewed)

1. **Q. M. Khan**, A. Ramezani, M. Koohestani, M. Ramdani, and R. Perdriau, “A comparison among DPI immunities of multi-stage CSVCOs and ring oscillators,” *13th International Workshop on the EMC of Integrated Circuits (EMC Compo)*, 2022, doi: 10.1109/EMCCompo52133.2022.9758599.

2. L. Devaraj, **Q. M. Khan**, A. Ruddle, and A. Duffy, “Comparing simulated impact of single frequency and multitone EMI for an integrated circuit,” *13th International Workshop on the EMC of Integrated Circuits (EMC Compo)*, 2022, doi: 10.1109/EMCCompo52133.2022.9758612.

3. A. Ramezani, **Q. M. Khan**, and H. Pues, “A new TRL/TRM PCB-based calibration method for on-board devices under test (DUTs),” *13th International Workshop on the EMC of Integrated Circuits (EMC Compo)*, 2022, doi: 10.1109/EMCCompo52133.2022.9758617.

4. L. Devaraj, A. Ruddle, **Q. M. Khan**, and A. Duffy, “Knowledge-based approach for system level electromagnetic safety analysis,” *31st European Safety and Reliability Conference (ESREL)*, 2021, doi: 10.3850/978-981-18-2016-8_203-cd.

5. **Q. M. Khan**, R. Perdriau, M. Ramdani, and M. Koohestani, “A comparative study of on-chip CMOS S&H voltage sensors for power integrity: SOI vs. Bulk,” *2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, 2021, doi: 10.1109/EMC/SI/PI/EMCEurope52599.2021.9559242.

6. **Q. M. Khan**, M. Koohestani, M. Ramdani, and R. Perdriau, “Obsolescence in EMC risk assessment: A case study on EFT immunity of microcontrollers,” *2020 International Symposium on Electromagnetic Compatibility—EMC EUROPE*, 2020, doi: 10.1109/EMCEUROPE48519.2020.9245783.

Chapter 2

IC DESIGN FOR CONDUCTED EMC ANALYSIS

The chapter describes the analog structures integrated into a custom-designed IC fabricated in SOI technology, for conducted EM immunity and emission analyses. It is followed by the detailed explanation of the IC layout and the design of the PCB variants utilized for conducted EM immunity and S-parameter testing.

2.1 Integrated Analog Structures

2.1.1 S&H Voltage Sensor

The propagation of the RF/EM disturbances through the package and inside the IC can not only modify the internal amplitude of the coupled disturbance but also induce parasitic non linear effects, which are not accurately characterized by external measurements, especially at high frequencies [28]. Hence, An on-chip voltage sensor based on deep-downsampling has already been proposed to characterize these coupled disturbances [29]. It is able to measure induced internal voltage fluctuations, determining the actual sensitivity to EM disturbances [30].

In order to improve the characterization of penetration of external EM disturbances in an IC and their parasitic effects, a robust on-chip S&H voltage sensor was designed, to be able to characterize internal noise (e.g in the power suppy) upto 1 GHz by aliasing it down to much lower frequencies. The voltage sensor is made up of the following blocks (Fig. 2.1 from input to output):

- a resistive divider including compensation capacitors and an attenuation ratio fixed to 0.1. It downscales the input voltage within 0 to 5 V range;

- a sampler cell composed of a storage capacitor, a CMOS pass gate driven by an external clock, with a 1 GHz bandwidth;
- a unity gain differential Miller amplifier including a current source with a start-up circuit ensuring a 100 MHz bandwidth.

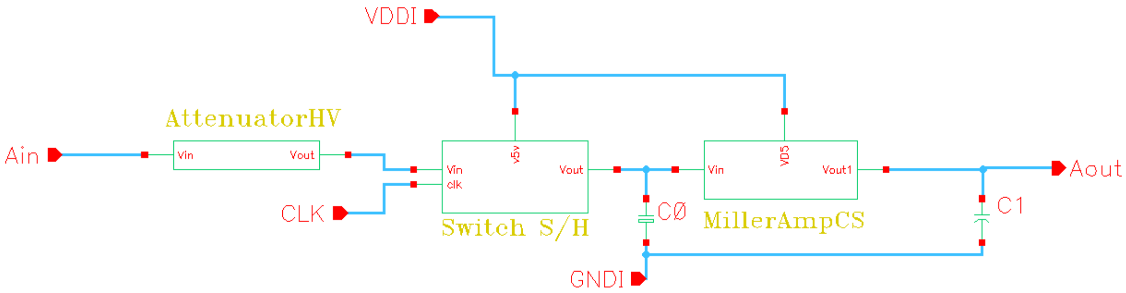


Figure 2.1: Schematic of the S&H voltage sensor.

The voltage sensor's fundamental principle is based on intentional aliasing, operating in sub-sampling conditions well below the Nyquist criteria, enabling transpose of high frequency signals (upto 1 GHz) down to a few MHz. Copies of the input signal spectrum are created around each multiple of the clock frequency. For example, a 0.9999 MHz sampling frequency would transform a 1 GHz input sinewave signal into a 100 kHz one. We can exclude the influence of parasitic elements caused by the package, bonding, and PCB trace at such a low frequency [31]. The signal amplitude observed at the output behaves as a linear function of the input signal amplitude. Note that this sensor can also be used in random sampling mode for non-sinusoidal signals.

The first stage is the input attenuator, a resistive divider with an attenuation ratio fixed at 1/10 to measure any voltage ranging from 0 to 50 V. Compensation capacitors were added to include the effect of the resistors' parasitic capacitance and the load of the sampler stage. These capacitors were appropriately sized to keep the high-frequency response flat. Metal-Insulator-Metal (MIM) capacitors are used in 180 nm XFAB SOI technology since they have high breakdown voltages and can withstand more than 50 V. The schematic of the attenuator is visible in Fig 2.2. The resistors and compensation capacitors are connected to the isolated ground of the voltage sensor.

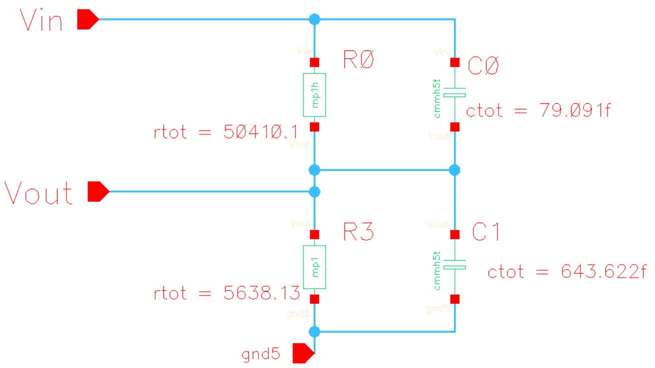


Figure 2.2: Schematic of the attenuator with compensation capacitors.

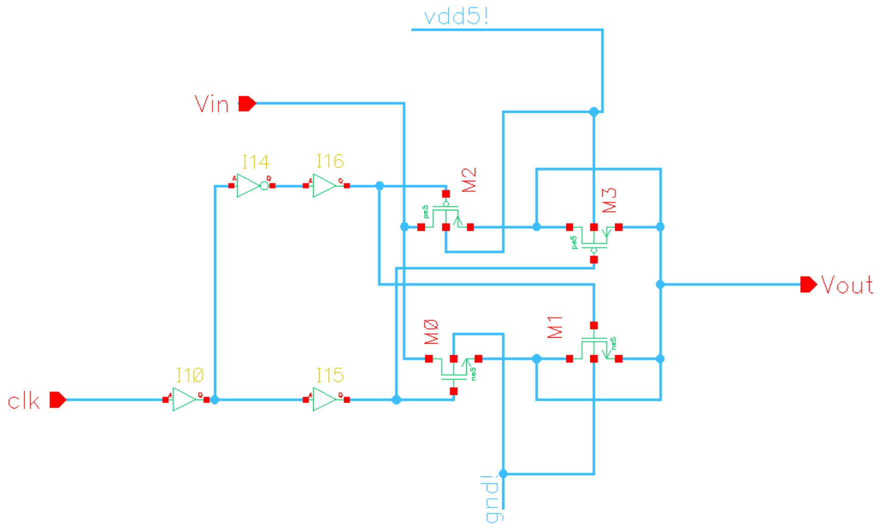


Figure 2.3: Schematic of the S&H switch cell.

The second stage is the sampler cell, which includes a switch and a holding capacitor. It is designed to have a 1 GHz bandwidth. To maintain this bandwidth, the switch's on-state resistance is reduced by increasing the MOSFETs' widths and keeping the holding capacitor value as minimum as possible. In the XFAB (XT018) SOI technology kit in Cadence Virtuoso, the minimum capacitor value is limited to 11 fF. Therefore, the latter value was kept for the holding capacitor to maintain the highest on-state resistance. Further, to ensure an almost constant resistance in the whole voltage range, the PMOS transistors are sized five times wider than the NMOS. Dummy transistors were added to the switch to compensate for parasitic

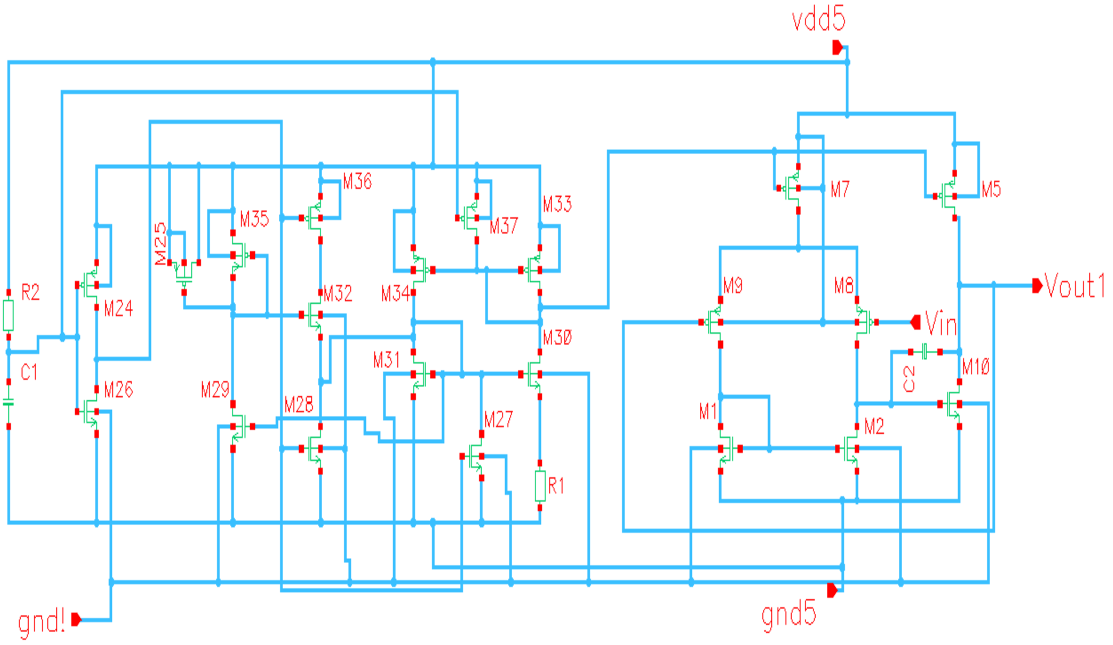


Figure 2.4: Schematic of the Miller amplifier with current source and startup circuit

capacitances. The schematic of the S&H switch cell is depicted in Fig 2.3.

The output stage is a differential, 5 V supply, Miller amplifier with unity gain up to 100 MHz. Its primary function is to provide isolation of the sensor from all noise sources to ensure accurate measurements. The Miller amplifier was designed to keep the gain constant, improve bandwidth, decrease output impedance, and mitigate stability problems. The 1 pF load capacitance at the output of the amplifier represents the capacitance of the output pad of the die (Fig. 2.1). The designed unity gain Miller amplifier consists of three blocks: differential amplifier, common source amplifier, and the current source with a start-up circuit, as demonstrated in Fig. 2.4. The common source amplifier ensures a maximum output swing, and a Miller capacitor (C2) connects it to the differential circuit [32], aiming to stabilize the circuit by improving the phase margin. In order to minimize the chip area, the current source provides a small reference current, which is replicated by duplicating the unit transistor M33 of the current source as many times as needed in transistors M5 and M7 to obtain the desired currents in the amplifier with proper matching. A start-up circuit (M24 to M37, R1 and C2) is added to ensure that the current source reaches a non-zero quiescent operating point when the power supply is turned on.

Table 2.1: Miller Amplifier Characteristics

Miller amplifier parameters	**XFAB-SOI**
W1 / L1 (μm)	70.6 / 0.6
W2 / L2 (μm)	125.2 / 0.5
W3 / L3 (μm)	25.3 / 0.6
W4 / L4 (μm)	483.1 / 1.0
W5 / L5 (μm)	115.9 / 1.0
W6 / L6 (μm)	30.0 / 1.0
W7 / L7 (μm)	8.34 / 1.0
W8 / L8 (μm)	4.83 / 1.0
Miller capacitance, C_m (pF)	1.90
Biasing current, I_4 (mA)	1.56
Biasing current, I_5 (μA)	390
Limiting resistor, R_c (kOhm)	6.07
Bandwidth, BW (MHz)	111.7
Phase margin, PM (deg.)	76.6
Slew rate, SR (V/μs)	83.4

The Miller amplifier's aspect ratios (W/L) were optimized using Jespers's and Murmann's sizing methodology [33] using pre-computed SPICE generated look-up tables and specific Matlab functions. It makes it possible to quantify trade-offs among transconductance efficiency, power consumption, gain, and area. Table 2.1 shows the unity gain Miller amplifier specifications for SOI technology. It includes parameters such as the W/L ratios, bandwidth (BW), slew rate (SR), etc., which ensures the stability of the miller amplifier.

The on-chip S&H voltage sensor was designed for operation in random mode, which includes under-sampling the input signal without any synchronization. Although it is not possible to reconstruct the shape of the input signal, each amplitude value taken by the signal can be ranked if a sufficient number of points are acquired and if the measured interference and the sampling command frequencies are not locked. Therefore, no calibration is required, which is usually the concern to compensate the linearity and offset errors of the sensor. The layout of the S&H voltage sensor is depicted in Fig. 2.5.

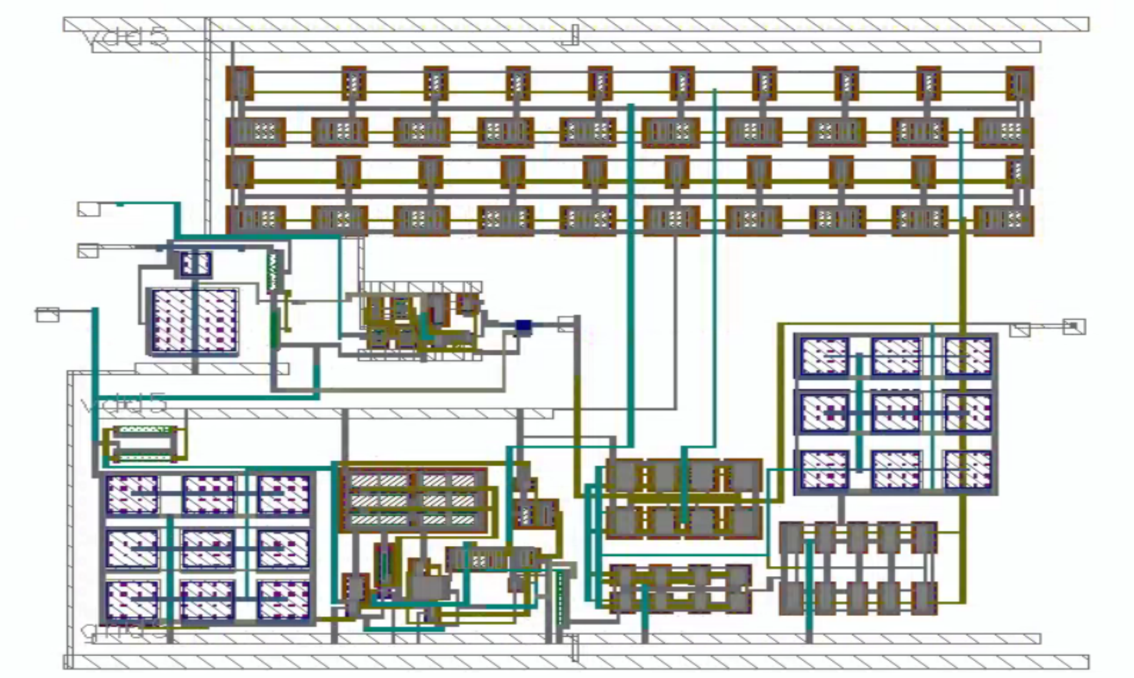


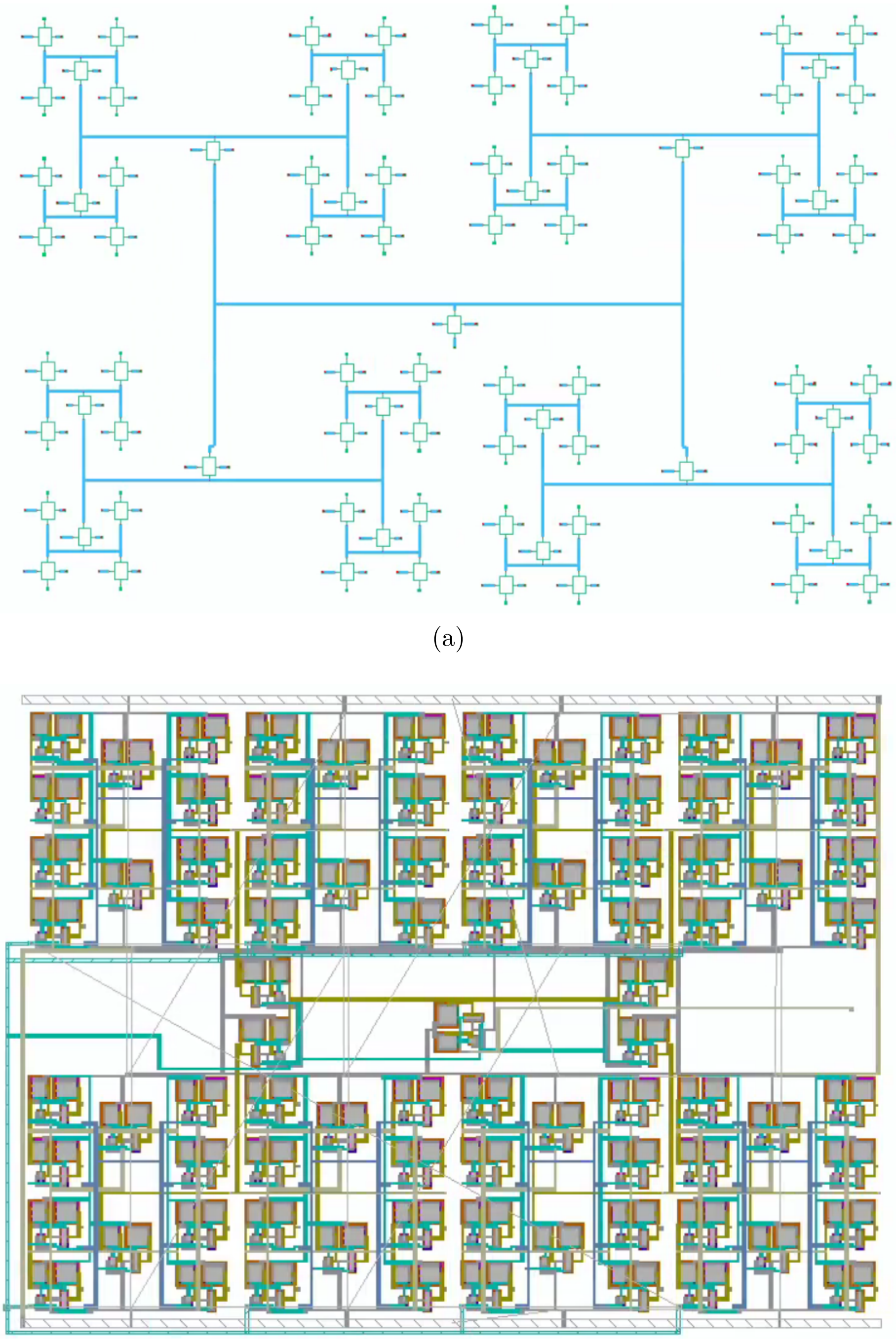
Figure 2.5: Layout of the S&H voltage sensor.

2.1.2 H-Clock Tree Noise Circuit

To investigate the conducted EM emissions at IC level, the H-clock tree noise circuit was designed. It consists of 85 analog non-inverting buffers with identical aspect ratios. It has a total of 4 stages and 64 output branches which were left floating. The schematic and the layout of the H-clock tree are displayed in Fig. 2.6.a and 2.6.b, respectively. One branch of the tree was connected to the input analog pad and provided the clock signal for the critical paths. The routing of the circuit was kept highly symmetrical in order to maintain equal propagation delays in each branch of each level. Non-inverting buffers were used instead of simple inverters to provide better sensitivity and ensured that all routed signals remained in-phase, avoiding noise cancellation [34].

2.1.3 SRAM Cells

The speed of microprocessors primarily depends on the cache memory that it incorporates, which predominantly consists of SRAM cells [35]. The SRAM stores each bit by using bi-stable latching circuitry [36]. The measure of data stability



(a)

(b)

Figure 2.6: H-clock tree noise circuit: (a) schematic; (b) layout.

of the SRAM is defined by the static noise margin (SNM), which is the minimum voltage noise that can flip its state [37]. A larger SNM ensures that the contents of the cell are unaltered during the read access, while allowing the cell to rapidly change its state across the write operation. In chip design, these conflicting requirements are overcome by balancing the relevant aspect ratios. Up to 70% of the systems on chip (SoC) area is occupied by embedded memories, which can limit the reliability improvement [38]. Different topologies are adopted for SRAMs [39], but the most conventional implementations in industry are the six-transistor (6T) and nine-transistor (9T) cells. The former comprises MOSFETs which can store 1-bit of data with minimum aspect ratios, whereas the latter has a higher data stability and lower power consumption at the expense of occupying a larger area leading to a smaller package density [40]. The main concerns for the SRAM cell design involve maintaining a higher data stability as well as reduced power dissipation and leakage current. Therefore, the 6T and 9T SRAM cells were designed to study there robustness to EMI and compare their respective stability parameters (e.g. SNM).

A conventional 6T SRAM works in three modes of operations: read, write and hold. It contains two cross-coupled inverters forming a latch with two access transistors to read and write the data stored in the memory cell [41]. The load and drive transistor pairs make up the inverter. The SRAM cell was designed to provide an effective read operation and an acceptable write margin. The cell is written by driving the desired value and its complement into the bit line (BL) and bit line-bar (BLB) when the word line (WL) is enabled. For reading data, the two bit lines are pre-charged to a floating state and once the WL is raised, the appropriate bit-line is pulled down while the other remains high. The schematic and the layout of the 6T SRAM cell are depicted in Fig 2.7.a and 2.7.b, respectively.

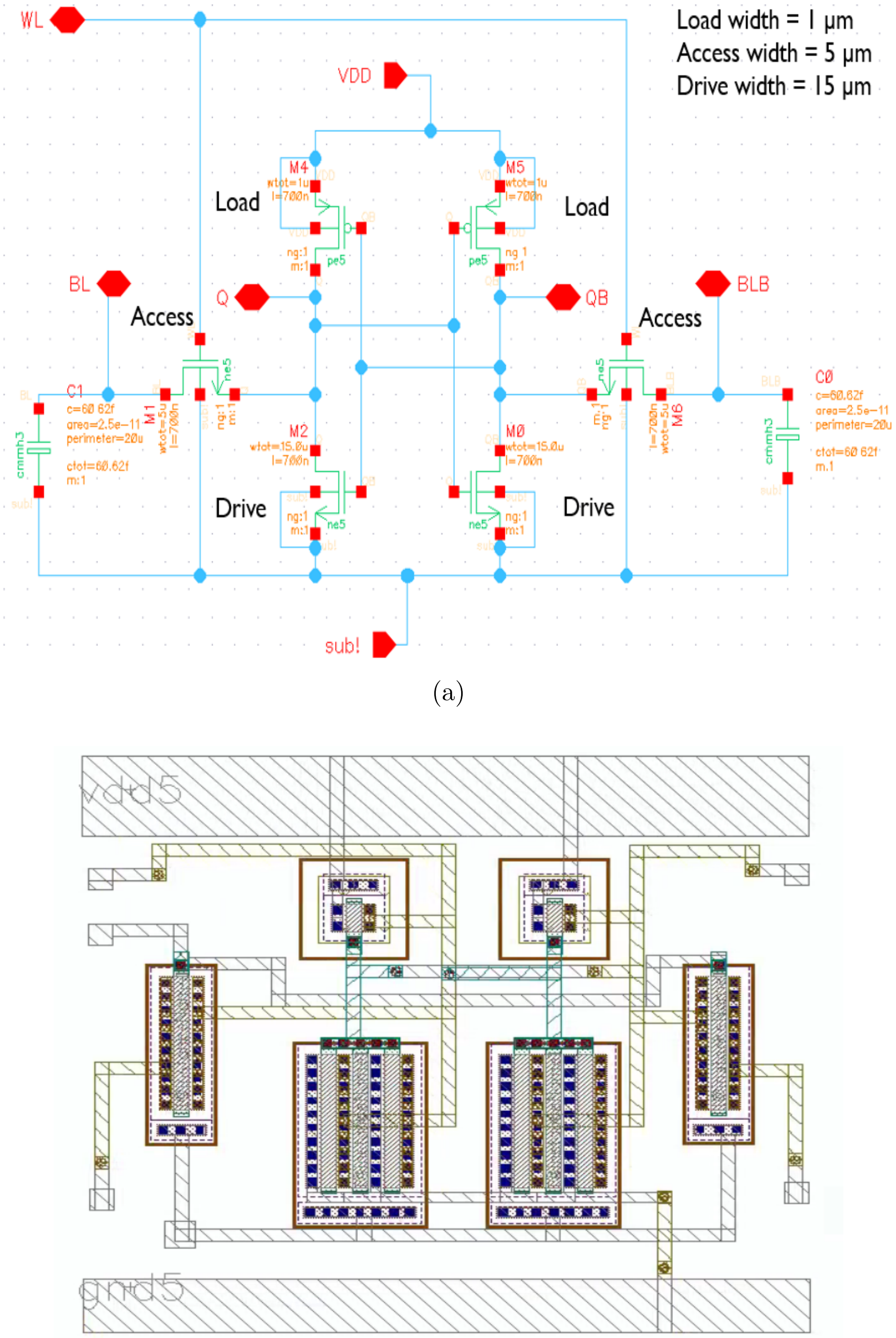
For a proper read operation, the access and drive NMOS transistors are sized such that the value of voltage rise at the node never exceeds the threshold value for the other inverter [42]. The cell ratio is the aspect ratio of the drive with respect to the access transistors. A higher value results in a better data stability; it is kept at 3.0 for all circuits. Similarly, ensuring proper write operation requires access and PMOS load transistors to be sized so that a zero may be written into the cell. The pull-up ratio is the aspect ratio of the load to the access transistors, which determines the write ability of the SRAM. It is kept at 0.20 for all circuits, so that they are easily writable. During the hold mode, the WL is disabled, consequently switching off the access transistors. This results in the load transistors continuing to reinforce each other and the contents of the coupled latch remain unchanged until the supply voltage remains on. In a standard memory block of an IC, the pins Q and QB of the SRAM cell are connected in parallel to a sense amplifier which pulls the desired data. Additionally, there are row and column decoders which select the appropriate cell where the data is written or read [43].

The designed 9T SRAM cell employs a differential read operation for better read access times. Its operation differs from the 6T SRAM, where the three added transistors create a strong pull-down effect in the read mode [44]. The aspect ratios of the read and pull-down transistors are identical to the drive-NMOS to maitain symmetry and decrease switching losses. When the read word line (RWL) is enabled, the differential pull-down of the drive transistors results in a lower resistance between data storage nodes to ground. When the RWL is disabled, it behaves as a 6T SRAM in the write and hold mode. However, since the extra transistors are switched off, the leakage current is extensively reduced. The schematic and the layout of the 9T SRAM cell are outlined in Fig 2.8.a and 2.8.b, respectively.

2.1.4 Integrated Oscillators

Integrated oscillators are a vital part of analog/digital IC blocks such as phase-locked loops (PLLs) and function generators [45]. From an EMC perspective, it is critical to study their performance and susceptibility to conducted/transient EMI [46]. Hence, four conventional oscillators, a 3- and 5-stage current starved voltage controlled oscillator (CSVCO); a 3- and 5-stage ring oscillator RO were integrated into the research IC. They were designed to have matching aspect ratios and generate sinusoidal signals with stable output frequencies. The main difference in their topology is that the CSVCO has externally biased MOSFETs that control the current provided to its delay stage. The biasing supply (V_C) is connected to those MOSFETs, to reduce the output power and maintain a wider frequency range [45]. On the contrary, for the RO, the output frequency is only dependent on the delay cell stages and the voltage supply. A buffer is added at the output stage of the RO to stabilize the generated sinusoidal signal.

Each oscillator has an isolated power supply pad (V_{DDI}) and a single separate ground (G_{NDI}), due to the use of SOI technology. A multi-stage digital frequency divider (FD) circuit is added at the output stage of each oscillator to reduce the fundamental frequency of the generated signal [45]. The FD is powered by the global power supply, which is isolated from each oscillator's individual power supply and

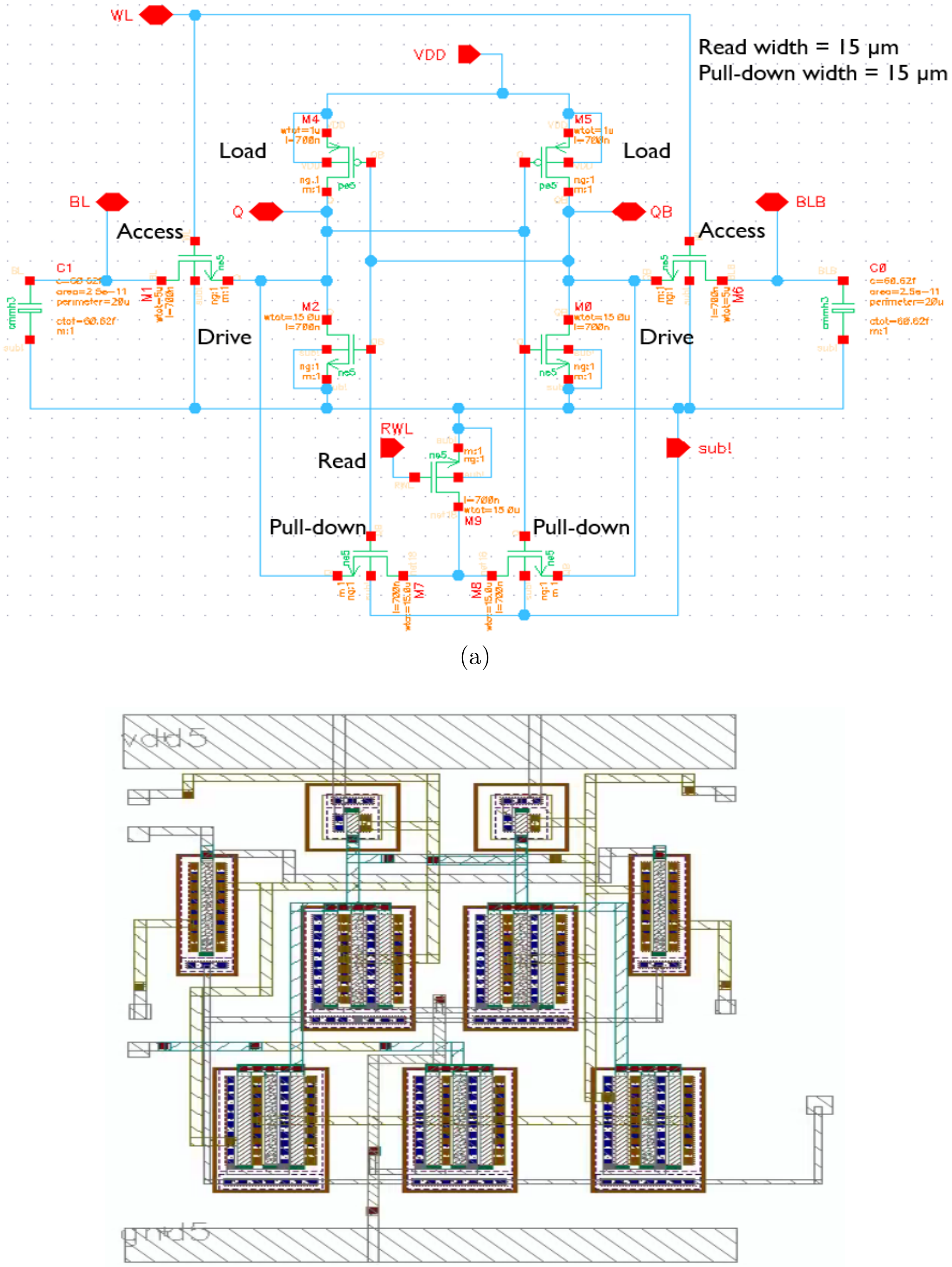


(a)

(b)

Figure 2.7: 6T SRAM cell (a) schematic; (b) layout.

aids in monitoring the frequency at the analog output pin without filtering effects due to package parasitics. The schematic and layout of the 3-stage CSVCO and RO

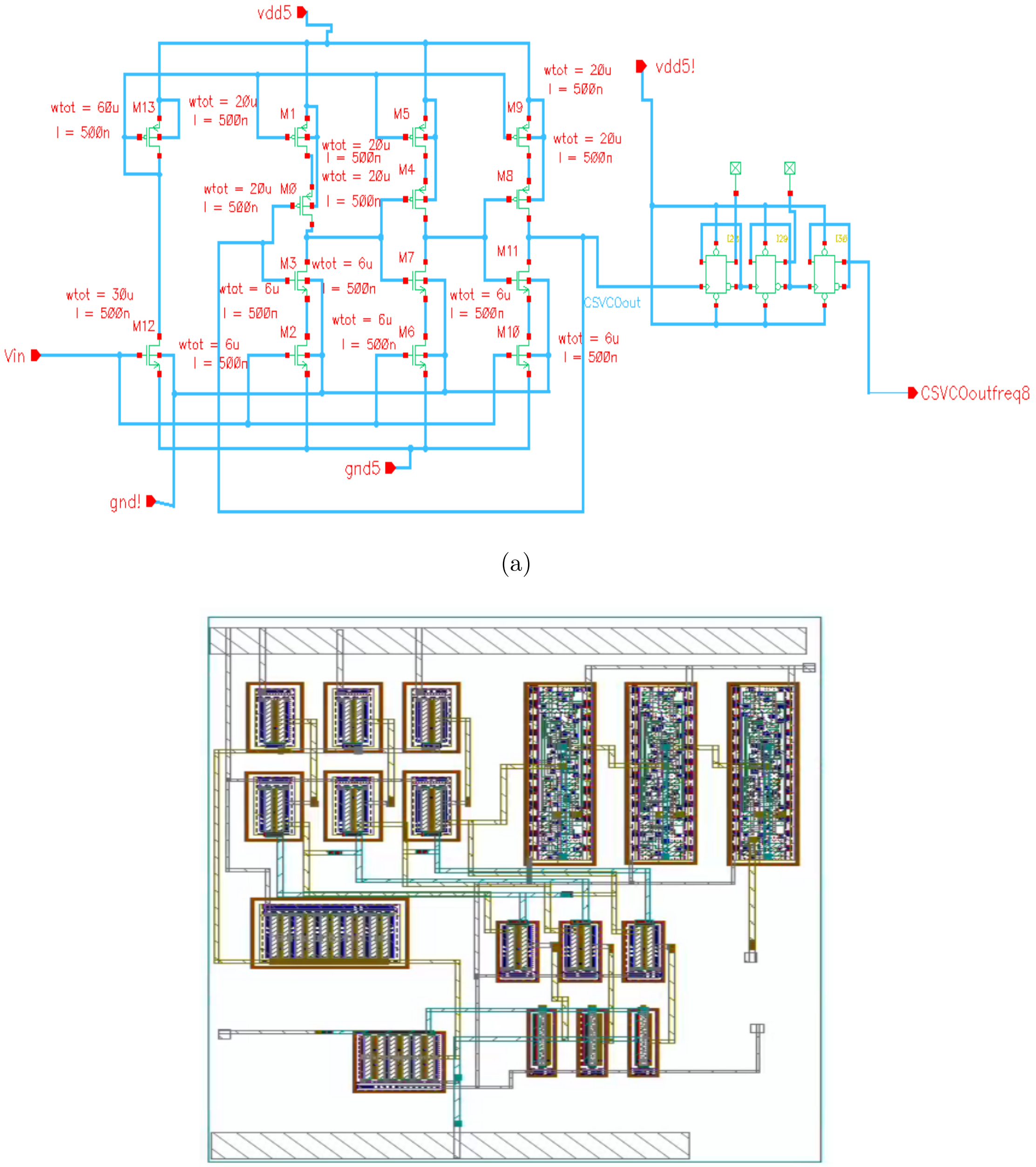


(a)

(b)

Figure 2.8: 9T SRAM cell (a) schematic; (b) layout.

including a 3-stage digital FD circuits at the output states are illustrated in Fig. 2.9 and Fig. 2.10, respectively. The 5-stage versions of the oscillators are designed in

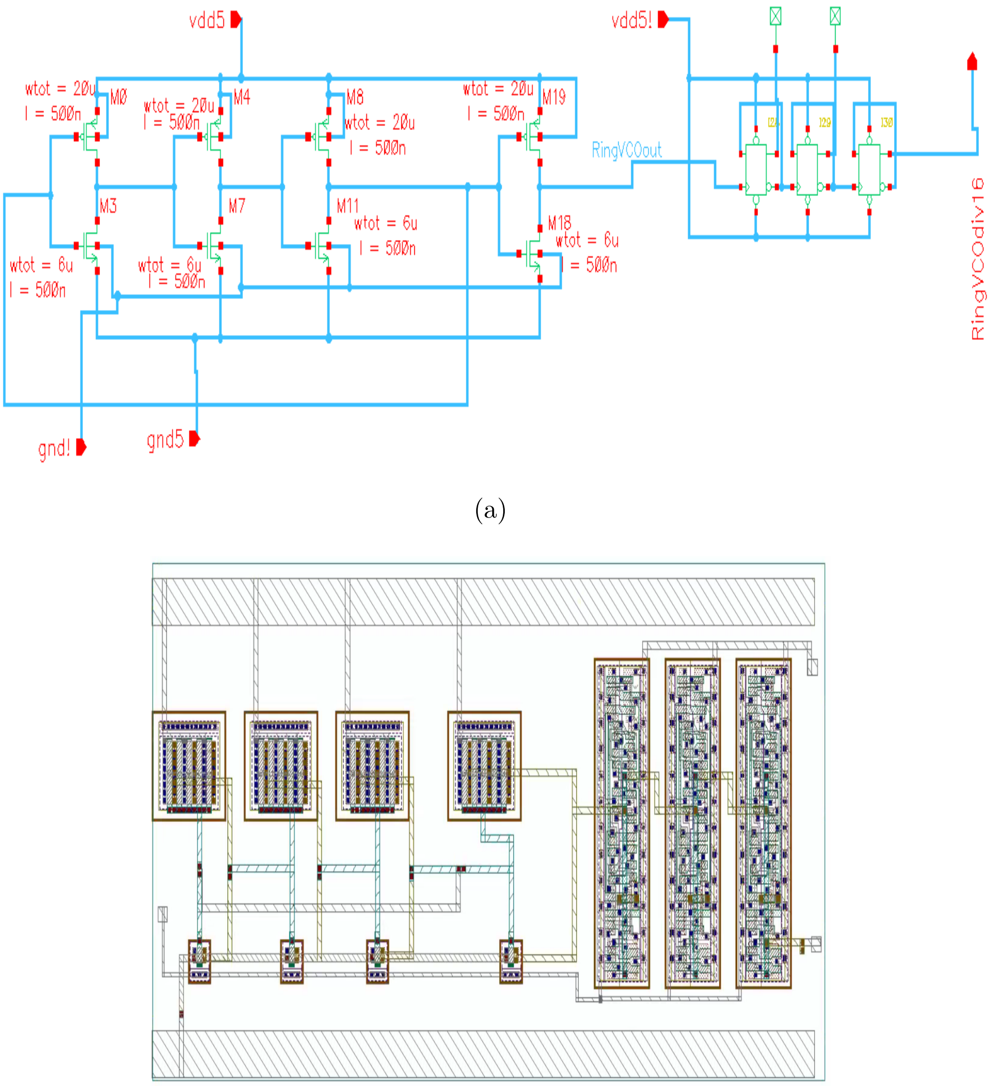


(a)

(b)

Figure 2.9: 3-stage CSVCO with FD circuit at the output stage (a) schematic; (b) layout.

a similar way, the only difference being the number of stages of the FD circuit. It was made sure that the aspect ratios of the MOSFETs at the inverter stage were identical to ensure they have the same threshold voltage levels. This was important



(a)

(b)

Figure 2.10: 3-stage RO including buffer and FD circuit at the output stage (a) schematic; (b) layout.

in the analysis of EMC testing, when characterizing their stability to transient and continuous wave conducted EMI.

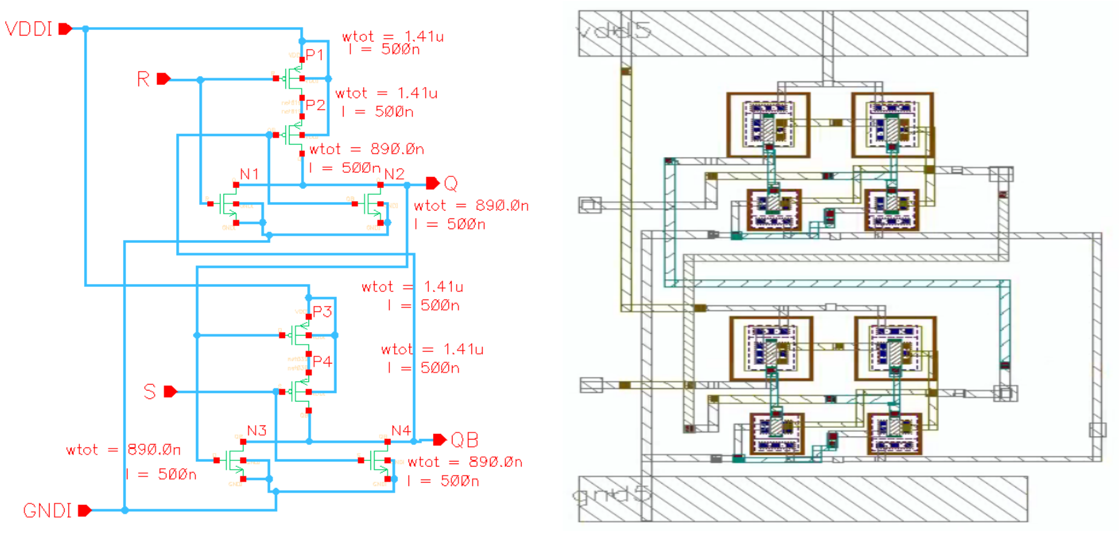
The conducted EM immunity of oscillators can be characterized by its operating frequency, peak-to-peak voltage, DC-offset voltage, and phase noise [47]. Since, the oscillator is driving a divider input, the variation of the output peak-to-peak voltage becomes crucial. Furthermore, the parameter that affects the stability of an oscillator is the output frequency of the output signal, which needs to be constant. Taking this into consideration the output frequencies of the oscillators were normalized close to each other (MHz range) by placing different stages of FD circuits. Table 2.2 illustrates the characteristics of the multi-stage CSVCOs & ROs at their nominal values. Interesting, the peak-to-peak voltages were considerably lower for all oscillators, since the output was monitored after the output pad & package. The pad capacitance reduced the peak voltage for high frequency signals above 50 MHz.

Table 2.2: Multi-stage CSVCOs and ROs Characteristics

Type of oscillator	Operating frequency	Frequency divider (FD)	Output frequency	Peak-to-peak voltage	DC offset voltage
3-Stage CSVCO Vc = 1.8 V	703 MHz	8 (FD =3)	87.9 MHz	325 mV	2.55 V
3-Stage RO with buffer	955 MHz	8 (FD =3)	79.5 MHz	280 mV	2.62 V
5-Stage CSVCO Vc = 1.6 V	271 MHz	4 (FD =2)	68.1 MHz	362 mV	2.49 V
5-Stage RO with buffer	815 MHz	16 (FD =4)	50.8 MHz	311 mV	2.57 V

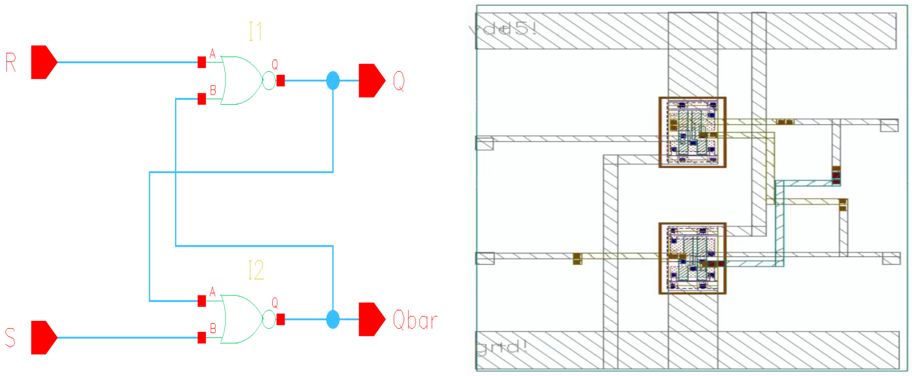
2.1.5 S-R Latches

Latches are single bit storage elements used in computing and data storage. The set/reset (S-R) latch is an asynchronous bistable multivibrator which works independently of the control signals and relies only on the S and R inputs [48]. The latch comprises of two NOR gates with a cross-feedback loop from the outputs Q and QB. All MOSFETs used have identical aspect ratios. An analog version of the S-R latch was designed to be able to utilize an isolated power supply and ground. To test the conducted immunity of the latch, continuous-wave conducted EM dis-



(a) (b)

Figure 2.11: Analog S-R latch (a) schematic; (b) layout.



(a) (b)

Figure 2.12: Digital S-R latch (a) schematic; (b) layout.

turbances were injected into the power supply and both the outputs were monitored to check if the latch went into a metastable state. The schematics and layouts of the analog and digital versions of the S-R latches are depicted in Fig. 2.11 and Fig. 2.12, respectively.

2.2 PETER_ESEO IC Layout

To accurately characterize conducted immunity and emission levels at the IC level and adopt a simulation-based transistor-level approach in order to find the root cause of failures, a custom-designed IC named PETER_ESEO was developed. All designed structures were integrated into the 1.52 mm × 1.52 mm research die, that was fabricated in SOI (XT018) CMOS 180 nm 5 V technology through the XFAB foundry. The design and layout of the IC was performed using Cadence Virtuoso. The XT018 series is X-FAB's Modular high-voltage SOI CMOS technology. It combines the benefit of SOI wafers with deep trench isolation and a state-of-the-art six metal layers 180 nm process. The platform is specifically designed for next generation automotive, industrial and medical applications operating in the temperature range of -40 to 175 °C.

The die is surrounded by a core-limited padring that is powered by the global power supply (V_{DDO}). It consists of 52 pads with N-MOS type ESD protection devices to both the V_{DDO} and ground. The V_{DDO}, V_{DDR} and V_{DD5} pins power up the padring and the digital blocks with reduced noise coupling. Likewise, the G_{NDO} and G_{NDR} pins are ground references for the padring and the digital blocks, respectively. Each analog/digital integrated structure has an isolated power supply pad (V_{DDI}) and a single separate ground (G_{NDI}), due to the use of SOI technology. The 52-pad 1.52 mm × 1.52 mm PETER_ESEO die (showcasing all IC structures with their pads) is illustrated in Fig. 2.13.

The output of each analog structure is connected to an analog pad having a parasitic capacitance, and an ESD protection circuit which will clamp the generated signals that are not within the 0 to 5.5 V range. The internal ESD circuits of the V_{DDI}/G_{NDI} and analog I/O pads include N-MOS transistors with gate to source resistors to reduce the overall gate leakage current. In case of the analog I/O pad, a resistor is also included in series between the pad and the internal rail. Almost all power supply/analog pads are identical with a passivation opening of 53 μm × 66 μm and bond pad pitch of 84 μm. This was intentionally done in order to characterize accurately the EM immunity of the independent analog structures. The only distinct pad is the high voltage (50 V) pad utilized for the input of the S&H voltage sensor (left-bottom in Fig. 2.13). Schematics and extensive details of the ESD protection devices are not included in the manuscript due to strict non-disclosure agreement

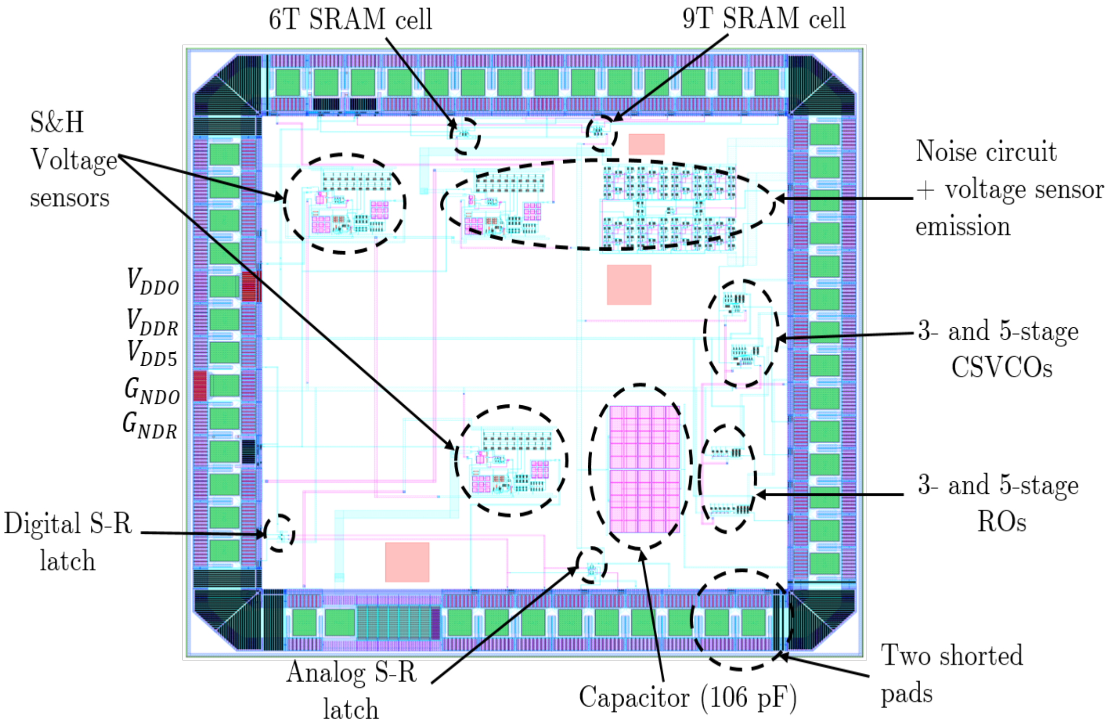


Figure 2.13: Layout of the PETER_ESEO research IC designed in 180 nm 5V SOI technology.

with XFAB.

Three versions of the S&H voltage sensor were included in the mini-ASIC. The first two variants had an identical attenuator (K=1/10) with the only difference being the analog input pad being different (low and high voltage). Both variants were included to find the internal noise power coupling path for low and high voltage signals. The third variant of the S&H voltage sensor (K=1/2) is used for characterizing the conducted emissions of the H-clock tree. The supply rail of the *H*-clock tree noise circuit is connected to the analog input of the S&H voltage sensor. This will be later discussed in detail in Chapter 6. The custom designed IC also includes two identical shorted pads and a 106 pF capacitor (Fig. 2.13). The objective of the shorted pads and the capacitor was to analyze the *S*-parameters and the equivalent series resistance with respect to thermal stress and aging. However, these mentioned structures were not analyzed further in this manuscript and can be used for future work.

The research die was packaged in a 64-pin ceramic quad flat package (CQFP).

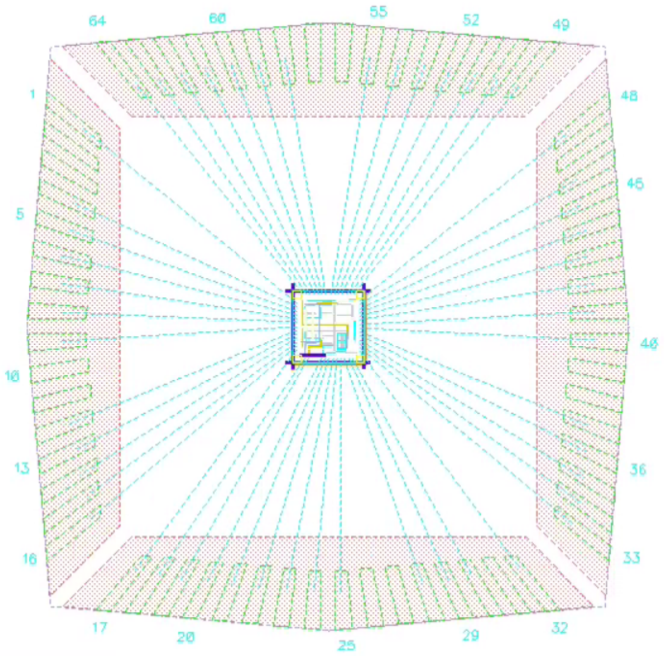


Figure 2.14: PETER_ESEO research die bonding diagram in CQFP64 package.

All power supply and ground pads were bonded to the package pins with spacing between them to minimize the effect of mutual inductive coupling, that makes it possible not only to inject more power into the supply pads but also monitor high frequency signals. The packaging schematic of the IC is depicted in Fig 2.14. The width and the maximum length of all the bonding wires are equal to 30 μm and 6.07 mm, respectively. The pincount of the PETER_ESEO research die packaged in CQFP64 is depicted in Table 2.3. Since the number of pins (64) were greater than the number of supply, digital, and analog pads (52), the remaining pins were unconnected and are denoted as NC (Table 2.3).

There are various inter/intralayer rules to follow when performing layout to ensure reliable fabrication of the circuit. Using Calibre and Assura in Cadence Virtuoso, a successful design rule check (DRC) and layout versus schematic (LVS) verification were executed, respectively. Furthermore, a hierarchical parasitic extraction (RCX) was carried out to approximate the RLC parasitics that may occur in the layout/traces paths of all MOSFETs in the designed IC.

Table 2.3: The pincount of the 52-pad PETER_ESEO IC packaged in CQFP64

Pin No. (Left)	**Pin Name**	**Pin No. (Bottom)**	**Pin Name**	**Pin No. (Right)**	**Pin Name**	**Pin No. (Top)**	**Pin Name**
1	Aout (VS) Emm	17	Aout Q Dig-L	33	Ain Shorted 2	49	VDDI Noise G
2	VDDI (VS) Imm	18	Aout QB Dig-L	34	Cap ESR	50	Ain BLB 9T
3	NC	19	VDDI (VS) Cal	35	Aout 5RO	51	Ain BL 9T
4	NC	20	Ain (VS) Cal	36	Aout 3RO	52	Aout QB 9T
5	GNDI (VS) ALL	21	Aout (VS) Cal	37	Aout 5CSVCO	53	Aout Q 9T
6	Aout (VS) Imm	22	Ain S-L	38	Aout 3CSVCO	54	Aout QB 6T
7	Ain (VS) Imm	23	Ain R-L	39	GNDI Osc all	55	Aout Q 6T
8	VDDO	24	Aout Q An-L	40	NC	56	GNDI 6T/9T
9	VDDR	25	Aout QB An-L	41	NC	57	NC
10	VDD5	26	GNDI An-L	42	VDDI 5RO	58	NC
11	NC	27	NC	43	VDDI 3RO	59	VDDI 9T
12	NC	28	NC	44	VDDI 5CSVCO	60	VDDI 6T
13	GNDO	29	VDDI An-L	45	VDDI 3CSVCO	61	Ain BLB 6T
14	GND R	30	NC	46	Ain CSVCO	62	Ain BL 6T
15	Din CLK (VS)	31	NC	47	Ain Noise G	63	Din RWL 9T
16	VDDI (VS) Emm	32	Ain Shorted 1	48	GNDI Noise G	64	Din WL 6T / 9T

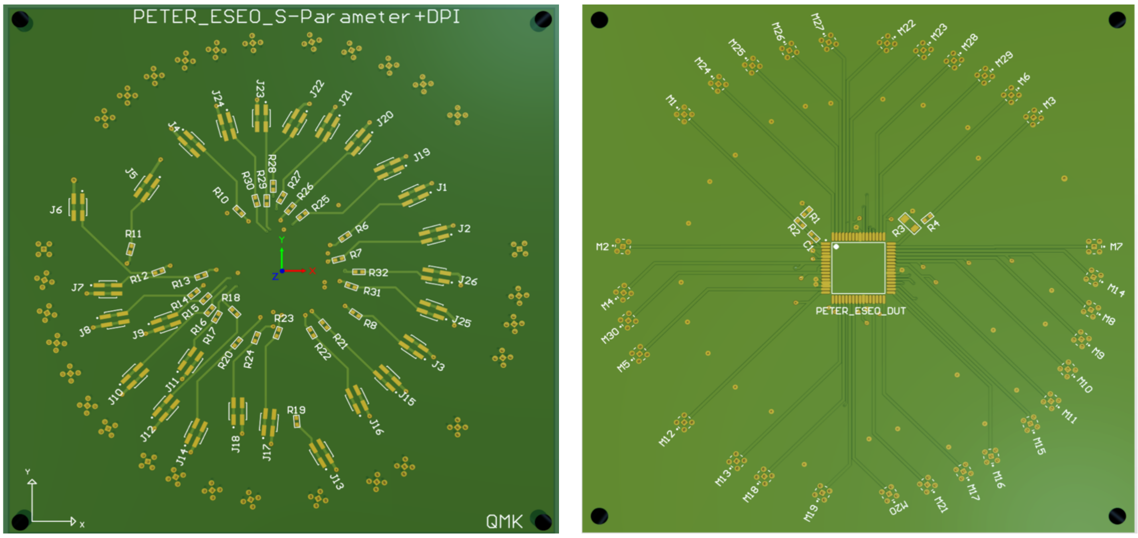
2.3 PCB Variants Design

2.3.1 Conducted Immunity and Emission PCBs (Packaged & COB)

To test the conducted emission and immunity of the PETER_ESEO IC, a 13 cm × 13 cm 4-layer FR4 PCB, was designed according to IEC 62132-4 [4] using Altium Designer. Several PCBs were manufactured through Eurocircuits and their layouts/schematics are displayed in Fig. 2.15.a and 2.15.b. It was made sure that the PCB does not contain non-essential circuitry (i.e. active or non-linear components) that could overload the PCB and result in uncontrolled RF behavior. This helps in measuring the immunity of the IC-under-test only. All the isolated grounds of the

IC were connected to the global ground.

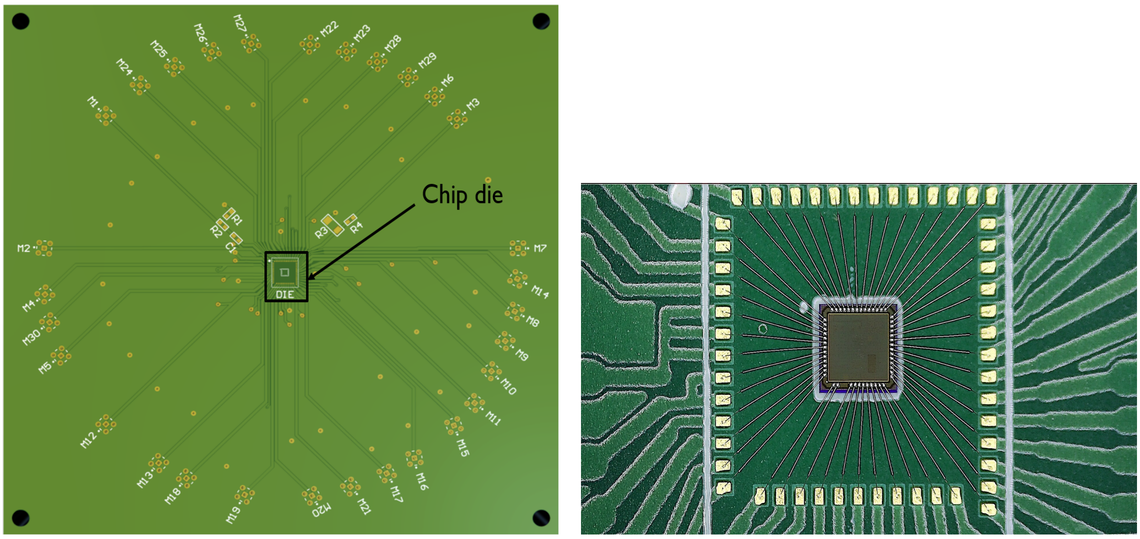
The bottom layer of the PCB includes the IC mounted in the middle and several micro-miniature coaxial (MMCX) through-hole female connectors to provide RF injection with a characteristic impedance of 50 Ω covering a frequency range from DC to 6 GHz (Fig. 2.15.b). The reason to use MMCX instead of the standard subminiature version A (SMA) connectors is due to their smaller size, which makes it possible to test all IC pins on the same PCB. The injection paths on the bottom layer were placed radially in a circle to keep the distance between the MMCX and the pin under test equal for all pins. The trace length from each MMCX to the DUT pin on the bottom layer was set to 47 mm. The traces were implemented as grounded co-planar wave-guides (GCPW); the latter being the variation of the CPW trace, which is usually preferred to a microstrip (MS) trace due to the field confinement inside the PCB substrate [49], [50], was selected to minimize the mutual coupling between the RF connectors as well as the components in different layers.



(a) (b)

Figure 2.15: 13 cm × 13 cm 4-layer FR-4 PCB conducted immunity variant (packaged) (a) top; (b) bottom.

As shown in Fig. 2.15.a, the top layer is mounted with multiple RF decoupling networks comprising a surface mount 4-pin male connector and a 470 Ω resistor in series. The resistor limits high power RF signals from being re-injected into the IC or the oscilloscope. The connectors are routed to the IC pin through MS and signal vias. The middle two layers serve as a ground plane for the MS and the GCPW on the top and bottom layers, respectively. The total thickness of the PCB layers was set to 1.6 mm, while the copper thickness of each layer was fixed to 36 μm.



(a)

(b)

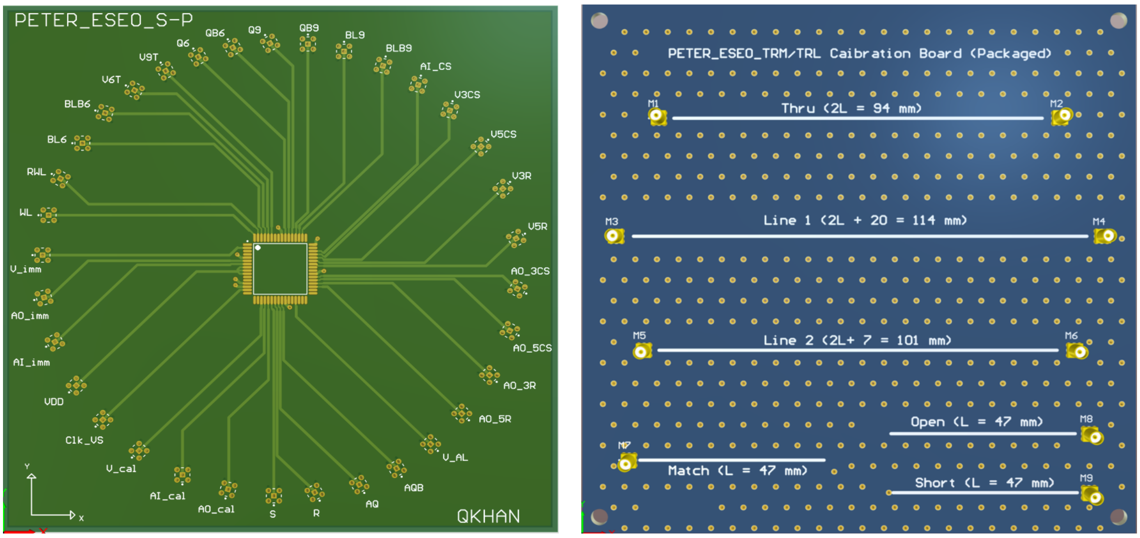
Figure 2.16: (a) 13 cm × 13 cm 4-layer FR-4 PCB conducted immunity variant (COB) bottom side. (b) Microscopic picture of bonding wires connecting the die pads to the PCB bond pads.

An additional PCB variant known as the chip-on-board (COB) was also designed. In this version the die was mounted directly on the PCB using a conductive epoxy resin (LOCTITE ECCOBOND EO1016) and aluminium bonding wires. The objective to design this PCB variant was study the effect of the IC package on the transient conducted immunity of integrated test structures which will be further highlighted in Chapter 5. The schematic of the COB is shown in Fig. 2.16.a. In this case, the trace length from each MMCX to the IC pin on the bottom layer was set to 53 mm. The microscope picture of the die bondpads connected to bonding pads of the PCB is shown in Fig. 2.16.b. The thickness of these bonding wires was equal to 17.5 μm.

2.3.2 S-Parameter and Calibration PCBs

S-parameters allow a device to be treated as a black box with inputs and resulting outputs, making it possible to model a system without having to deal with the complex details of its actual structure. As the bandwidth of current ICs increases, it is important to characterize their performance over wide frequency ranges. Traditional low frequency parameters such as resistance, capacitance, and gain can be frequency dependent, and thus may not fully describe the performance of the IC at the desired frequency. In addition, it may not be possible to characterize every parameter of a complex IC over frequency, so system-level characterization using S-parameters may provide better data.

A 13 cm × 13 cm 4-layer FR4 PCB variant was designed to measure the S-parameters of the PETER_ESEO IC pins. The IC was mounted at the center of the PCB with its I/O pins connected to several MMCX through-hole female connectors with a characteristic impedance of 50 Ω covering a frequency range from DC to 4 GHz. Similar to the conducted immunity PCB variant, MMCX were also used here due to their compact size, which makes it practicable to test all IC pins on the same PCB. The injection traces were placed radially in a circle, with a 47 mm individual primary length, to keep the distance between each MMCX and IC pin equal. The S-parameter PCB design is shown in Fig. 2.17.a. Only the top layer is utilized for the IC, traces and connectors. The PCB does not include any active/passive components to efficiently characterize the S-parameters of all IC pins.



(a) (b)

Figure 2.17: (a) 13 cm × 13 cm 4-layer FR-4 PCB S-parameter variant (COB) top side. (b) Calibration board adopting the SOLT/TRL/TRM method.

For accurate S-parameter measurements, it is essential to design a calibration board. This makes it possible to extract the impedance profile of the IC pin without the effect of the PCB traces. Among a variety of calibration methods, the most commonly known are short-open-load-thru (SOLT) [51] and thru-reflect-line (TRL) [52] methods which are based on 8-term or 12-term error models. The former method measures one transmission (T) and three reflection (SOL) standards to calculate the S-parameters. On the other hand, the latter method determines two transmission (T,L) and one reflection (R) standards to determine the error coefficients. Several calibration techniques such as thru-reflect-match (TRM) and line-reflect-line (LRL) are the derivatives of the TRL technique [53]. Each of these calibration techniques has its advantages and drawbacks depending on the frequency range and application. While the calculation behind SOLT is simpler than the TRL, the latter has a better accuracy. Hence, SOLT needs well defined standards whereas limited knowledge of the calibration standards does not impact the accuracy of the TRL method. The main limitation of the TRL method is the inaccuracy at lower frequencies below 500 MHz. Hence, a new technique combining the TRL & TRM methods was introduced in [54]. The latter method gave accurate transmission and reflection coefficients upto 4 GHz.

A 13 cm × 13 cm 4-layer FR4 calibration PCB was designed and panelized with the same PCB substrate as the S-parameter board (Fig. 2.17.b). The calibration techniques adopted were the SOLT and TRM/TRL methods. The primary length of the short, open, and load traces was set to 47 mm, while the thru trace was fixed to 94 mm. As far as the load is concerned, a high precision 50 Ω (0402) [55] resistor was used for termination. A dense grid of ground vias were placed on the PCB having 5 mm spacing between the traces and signal vias. This arrangement reduced the change in the characteristic impedance value and hence the reflections. The SOLT method was eventually selected to characterize the impedance profile of the power supply pins up to 1 GHz frequency (to be discussed in Chapter 6).

2.4 Conclusion

This Chapter explained the detailed design of a custom-designed IC that was fabricated in SOI 180 nm 5 V technology, comprising of several independent analog CMOS structures such as the H-clock tree noise circuit, S&H voltage sensors, S-R latches, multi-stage integrated oscillators, and SRAM cells. Further, the design of the PCB variants for conducted immunity and S-parameter testing was extensively described. The robustness of the S&H voltage sensor and the SRAM cells developed in SOI, with respect to process and temperature are investigated in Chapter 3. The integrated oscillators will be further explored for conducted EM multitone and transient immunity analysis in Chapters 4 and 5, respectively. Finally, in Chapter 6, the H-clock tree and other analog structures of the designed IC are tested and analyzed for the development of conducted EM immunity and emission models. The main benefit of SOI technology is its ability to isolate internal IC blocks from one another, making it possible to carry out individual conducted immunity experiments on those blocks. This is the reason why the PETER_ESEO IC was fabricated in SOI technology. However, bulk technology is much more widely used in industry and may exhibit a different behavior in terms of process and temperature variations. Hence, the upcoming chapter will describe the resilience of SOI analog structures to such variations in comparison to the ones developed in the bulk CMOS process.

CHAPTER 3

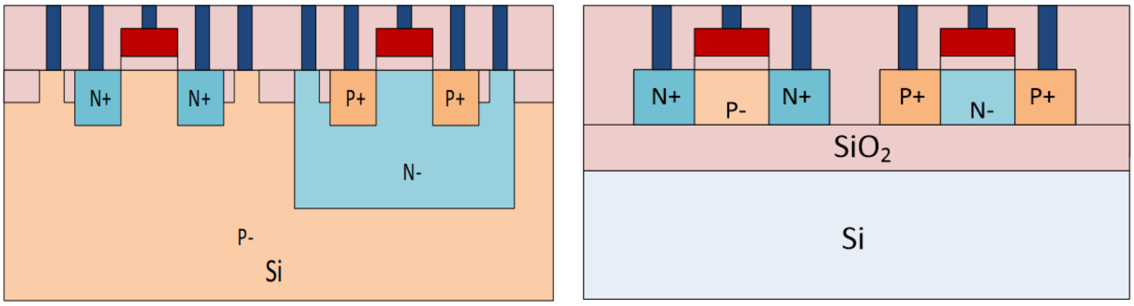
PROCESS AND TEMPERATURE BEHAVIOR OF SOI AND BULK ICS

3.1 Introduction to SOI and Bulk Technologies

The semiconductor technology has been progressing enormously these last decades, such evolution has been driven by the continuous look for the increase of the operation speed and the integration density of complex analog/digital circuits. In standard industries, bulk CMOS is a very mature technology having high performance and lower manufacturing costs. However, increasing integration degree and signal transmission rates highlight some challenging aspects for bulk ICs. The most promising technology to overcome those limitations is the SOI CMOS process [56]. From its early development phase till recent years, SOI has grown from a mere scientific curiosity into a mature technology.

The unique feature of SOI process is that it has a buried silicon oxide (BOX) insulator layer which separates the integrated-circuit structure from the bulk substrate [57]. The cross sections of the conventional bulk and SOI MOSFETs are displayed in Fig. 3.1.a and 3.1.b, respectively. SOI can reduce the capacitance at the source and drain junctions significantly by eliminating the depletion regions extending into the substrate. This results in a reduction in the RC delay due to parasitic capacitance and, hence, resulting in faster switching compared to bulk CMOS ICs [58]. Owing to the BOX structure, the source/drain regions of the SOI NMOS/PMOS devices can be placed against each other without worrying about the possibility of latch up. Therefore, SOI devices have a much higher device density [59].

ICs designed with SOI have several vital advantages over bulk technology: faster performance, lower power dissipation, low leakage effect, and high integration [60]. In terms of RF/EMC, SOI provides better latch up immunity compared to bulk, by eliminating the inter-device leakage. Furthermore, in mixed-signal ICs it is proven



(a) (b)

Figure 3.1: Cross-section of devices [58]: (a) bulk; (b) SOI.

to reduce interference and cross-talk between devices [61]. The most important reason why SOI was selected over bulk CMOS to fabricate the PETER_ESEO IC, was the fact that the former provides lateral and vertical isolation of active devices from the substrate. It allowed us to test independent blocks integrated in to the IC, for conducted EM immunity testing.

The main disadvantages/challenges of SOI compared to bulk are the higher costs of SOI wafers, uncertainty of the material quality and the floating body effects [62]. These will be further highlighted in the upcoming sections.

The main results of Sections 3.2 and 3.3 have been published by the author in [63] and [64], respectively. The results of these sections draw of course on the relevant publications.

3.2 Case Study 1: S&H Voltage Sensor

SOI has also demonstrated its potential for RF applications [65]. An on-chip S&H voltage sensor based on deep-downsampling/aliasing has been integrated into the PETER_ESEO research (developed in SOI) chip to characterize RF coupled disturbances. It measures induced internal voltage fluctuations, determining actual sensitivity to EMI [66]. Developing this sensor in SOI, benefits from from reduced substrate losses and can withstand harsh environments (high temperature, radiations) [67].

For the purpose of this case study, the S&H voltage sensor was designed and simulated in both 5 V 180 nm XFAB-SOI and AMS-bulk technologies. Process, supply voltage, temperature (PVT) variation tests were carried out on both sensors to compare their performance. These tests represent an integral part of modern chip design flows and accurately characterize a circuit's worst-case behavior. Transient analysis runs were executed at extreme corners and essential electrical parameters: power consumption, leakage current, and output voltage were analyzed. Consequently, this case study aims to demonstrate that a voltage sensor designed with equivalent specifications can function better in SOI compared to bulk technology when exposed to critical conditions.

All circuits were designed using Cadence Virtuoso, and the simulations were obtained in Spectre. Two identical sensors were simulated in SOI and bulk CMOS 5 V using 180 nm technology kits, provided by XFAB and AMS foundries, respectively. The sensors are designed to have similar characteristics and matching size dimensions. The voltage sensor consists of a resistive attenuator, a sampler cell and a unity gain differential Miller amplifier with its own start-up circuit. For more details on the design of the S&H voltage sensor refer to Section 2.2.2.

Table 3.1: Miller Amplifier Characteristics (SOI vs. bulk) © [63]

Miller amplifier parameters	**XFAB-SOI**	**AMS-bulk**
W1 / L1 (μm)	70.6 / 0.6	59.2 / 0.7
W2 / L2 (μm)	125.2 / 0.5	110.8 / 0.7
W3 / L3 (μm)	25.3 / 0.6	16.2 / 0.7
W4 / L4 (μm)	483.1 / 1.0	357.2 / 1.0
W5 / L5 (μm)	115.9 / 1.0	89.1 / 1.0
W6 / L6 (μm)	30.0 / 1.0	25.0 / 1.0
W7 / L7 (μm)	8.34 / 1.0	6.3 / 1.0
W8 / L8 (μm)	4.83 / 1.0	3.57 / 1.0
Miller capacitance, C_m (pF)	1.90	1.33
Biasing current, I_4 (mA)	1.56	1.10
Biasing current, I_5 (μA)	390	275
Limiting resistor, R_c (kOhm)	6.07	9.12
Bandwidth, BW (MHz)	111.7	121.3
Phase margin, PM (deg.)	76.6	74.3
Slew rate, SR (V/μs)	83.4	90.8

The Miller amplifier's aspect ratios (W/L) were optimized using Jespers's and

Murmann's sizing methodology [33] using pre-computed SPICE generated look-up tables and specific Matlab functions. It makes it possible to quantify trade-offs among transconductance efficiency, power consumption, gain, and area [68]. Table 3.1 shows the unity gain Miller amplifier specifications for both technologies. The W/L ratios of the SOI are larger than bulk due to its MOSFETs' having higher transconductance, more current, lower parasitic junction capacitance, and higher gate oxide thickness [69]. The bandwidth (BW) and slew rate (SR) of the bulk amplifier are slightly larger than SOI, but having a lower phase margin. The biasing current of the SOI is higher than bulk.

3.2.1 PVT Corner Analysis

This section presents all PVT, transient and alternate current (AC) simulations related to the S&H voltage sensor in 5 V 180 nm XFAB-SOI and AMS-bulk. All transient simulations were timed to 10 μs since it represents the single 100 kHz aliased output wave. All AC simulations have a frequency range of 10 GHz, in a logarithmic scale, with a 25 V DC offset at the attenuator input. While the nominal temperature is 27 °C, the temperature and voltage ranges for PVT simulations are (-40 °C to 80 °C in 5 °C steps) and (4.4 V to 5.6 V in 0.1 V steps), respectively, as indicated by the foundries. For process variations, only extreme corners, worst power (WP), and worst speed (WS) are considered.

PVT variations can increasingly affect the sensitivity of the CMOS circuit performance. A significant number of possible corners are applied to examine circuit timing. The process variation accounts for deviations in the semiconductor fabrication process. Traditionally, it is reviewed as a percentage change in the performance calculation. Considerable variations in its specifications can be oxide thicknesses, impurity concentration densities, and diffusion depths. These adversely affect the sheet resistance, threshold voltage, and aspect ratios of CMOS transistors [70].

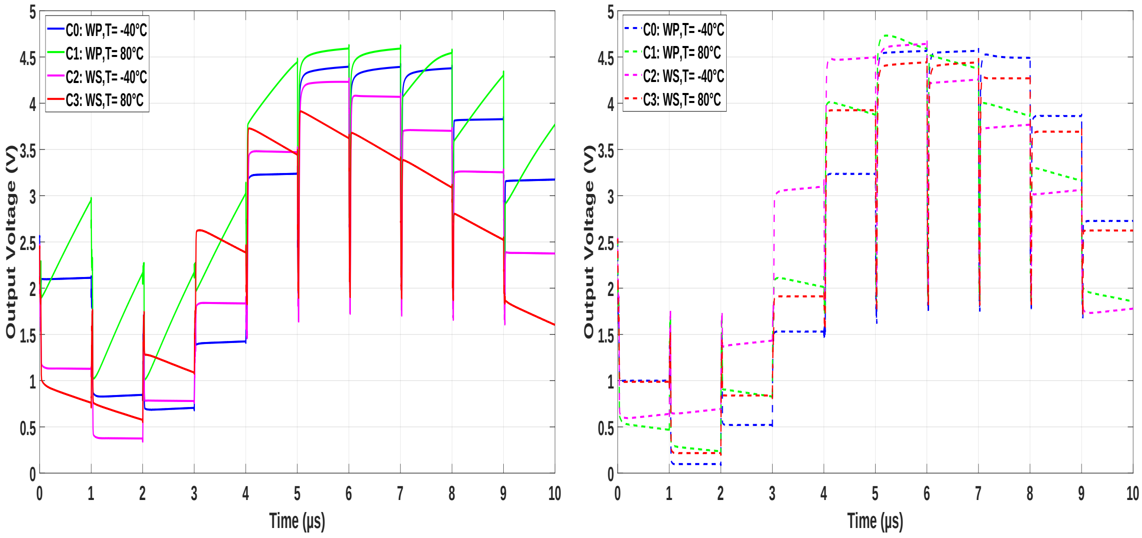
During standard operation, the supply voltage can typically vary from the nominal value. The saturation current and the delay of a cell are dependant on the power supply. When the power is not constant in an IC, each cell operates quicker with rising supply voltage, consequently reducing the delay. All circuits have temperature variations, because of the power consumption linked to the switching of the CMOS transistors. Excessive temperatures will reduce the mobility of the transistors resulting in an increased propagation delay. However, the temperature surge also decreases the threshold voltage and leads to higher current and accelerated performance. Hence, the equivalent change produces adverse effects that will highly depend on the circuit's supply voltage. For bulk CMOS circuits, the robustest performance is reached at the fastest process (worst power), high supply voltage, and reduced temperature [71]. Therefore, a PVT corner analysis was performed on both S&H voltage sensors in SOI and bulk CMOS technologies to compare the effects.

A 4-corner transient SR simulation was performed on each Miller amplifier with extreme temperature and process variations while keeping the supply voltage constant at 5 V. The amplifier in each technology was operated by a dedicated 5 V power supply, separated and isolated from the circuit's other power supplies. Thus, we are only monitoring the effects of process and temperature in this case. The results are displayed in Table 3.2. The SR of each Miller amplifier, at corners C1 and C2, is at its maximum and minimum, respectively, for both technologies. This result is due to the slew rate being directly related to both process and temperature. A faster process results in quicker switching of the transistors, and higher temperature increases the current coming from the differential pair. Moreover, it can be noticed that the SR of SOI amplifier is more sensitive to either process or temperature. Comparatively, the SR of both amplifiers was either increased or decreased slightly on corners C0 and C3, respectively, with the effects of process and temperature competing against each other.

Table 3.2: Slew rate (SR) vs. PVT corners © [63]

PVT Corners (V_{DD}=5V)	SOI (SR, V/μs)	bulk (SR, V/μs)
C0 (WP, T = −40 °C)	85.8	94.9
C1 (WP, T = 80 °C)	150.1	119.3
C2 (WS, T = −40 °C)	52.1	66.7
C3 (WS, T = 80 °C)	79.9	85.6

Transient simulations on the same corners were implemented for the output voltage of each S&H voltage sensor. The peak-to-peak output voltages (V_{p-p}) of the sensor, in bulk and SOI CMOS technologies, at nominal conditions are 4.4 V and 3.8 V, respectively (Fig. 3.2.a & 3.2.b). The latter was not expected, since the output swing is related to the transconductance efficiencies of the output transistors [33], which are the same in both designs. The V_{p-p} and waveform remained unchanged at corner C0 for both technologies. Corner C1 displayed different responses for both technologies. For SOI (Fig. 3.2.a), the V$_{p-p}$ reduced by 0.2 V, and the SR of the output voltage signal changed abruptly. The curve was deformed at the falling end. This could be due to the process variation in the holding capacitor or the switches (the same behavior being observed at the amplifier input node). For bulk (Fig. 3.2.b), V$_{p-p}$ reduced by 0.1 V, and the SR of the output signal slightly reduced at the rising end. At corner C2, SOI V$_{p-p}$ remained the same, only the curve faced a negative offset of 0.2 V, and the waveform remained unchanged. For bulk, V$_{p-p}$ lowered by 0.4 V and the curve had a positive DC offset of 0.2 V. At corner C3, the overall V$_{p-p}$ of SOI and bulk were reduced by 0.4 V and 0.2 V, respectively. For SOI, the effect was more severe as the overall SR of output signal reduced and the output voltage graph was deformed at the rising end. This could be due to the holding capacitor discharging slowly while, for bulk, the output SR and the waveform remained unaltered.

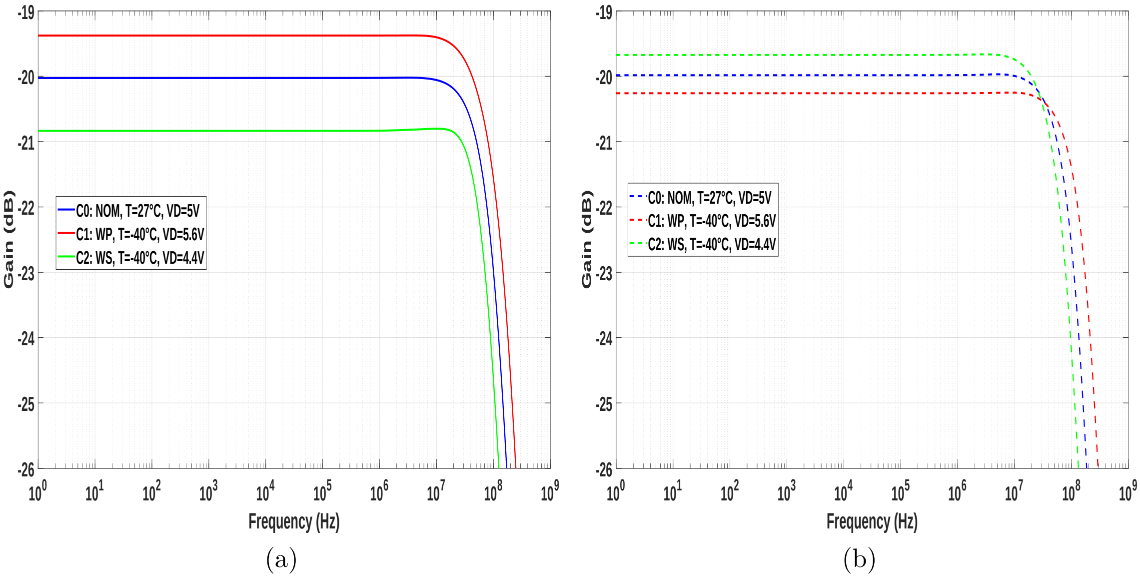


(a)

(b)

Figure 3.2: Transient PVT simulation (V$_{DD}$ = 5 V) of the S&H sensor's output voltage for an input frequency of 1 GHz © [63]: (a) SOI; (b) bulk.

To sum up, both technologies' best transient response was observed when the temperature was low, and the process was fast. Contrarily, the worst output response (lowest V$_{p-p}$ and highest offset) for bulk was at corner C2, which means that the threshold voltages of the MOSFETs significantly increase with a slower process. Also, at this corner, Miller amplifier in AMS technology had the minimum SR, which is related to V_{p-p}; however, the latter had no effect on the waveform shape. For SOI, the worst output response was observed at both C1 and C3 corners. Since the SR of the output was reduced at both corners, as was V_{p-p}. As described earlier, the waveform of the output signal is affected more by the holding capacitor charging speed, while the amplifier's SR had little effect on the output voltage signal. This uncertainty remained to be clarified, by analyzing the influence of process and temperature variations on the overall SOI S&H voltage sensor.



(a) (b)

Figure 3.3: AC PVT simulation of gain response of S&H voltage sensor © [63]: (a) SOI; (b) bulk.

A 64-corner PVT AC simulation was performed on both sensors, and the corners resulting in the largest divergence from nominal values were plotted in Fig. 3.3. The gain of the sensors was −20 dB due to the 1/10 attenuator. The bandwidth of SOI and bulk CMOS voltage sensors at nominal conditions is 100.5 MHz and 110 MHz, respectively. Including process and temperature, the supply voltage was varied from 4.4 V to 5.6 V, which are the maximum limits of the MOSFETs used in both technologies. The two extreme corners were observed at the constant lowest temperature (−40 °C): the extreme process (WP, WS) and supply voltages (4.4 V, 5.6 V). However, the behavior of SOI compared to bulk was quite different. At corner C1 (fast process, high voltage), the SOI sensor's bandwidth and gain were increased to 200 MHz and −19.3 dB, respectively (Fig. 3.3.a). Moreover, for bulk, the bandwidth was increased to 180 MHz, but the gain dropped to −20.4 dB. At corner C2 (slow process, low voltage), the SOI sensor's bandwidth was lowered to 80 MHz, and its gain reduced to −20.8 dB (Fig. 3.3.b). Furthermore, the bulk sensor's bandwidth was reduced to 85 MHz but its gain increased to −19.6 dB.

To summarize, at higher supply voltages and faster processes, the bandwidth of both sensors was increased. This is due to an increase in the DC operating current of the amplifier stages, which is even more significant for SOI. At the same corner, the gain of the SOI sensor was increased, while it was reduced for bulk. The reason could be due to variations in the attenuator, the amplifier itself being put in a unity gain closed loop.

3.2.2 Temperature Effect and Power Consumption

This section demonstrates the effect of temperature only on the voltage sensor's essential parameters: output voltage, average current from the current source and the leakage current from the supply when the circuit is powered off.

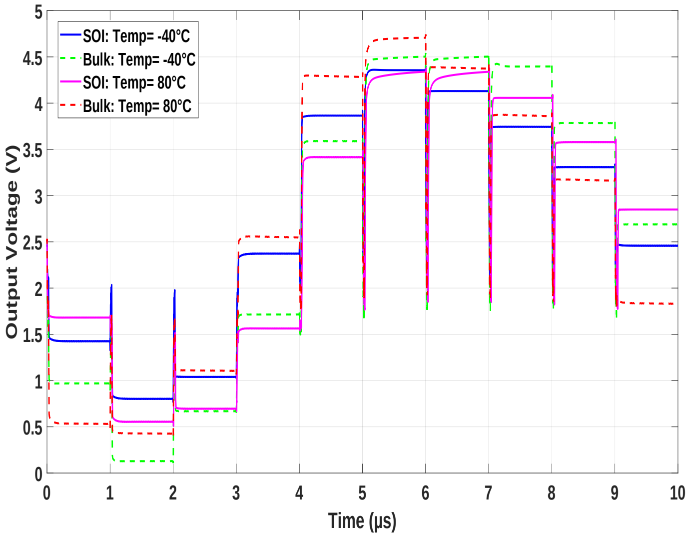


Figure 3.4: SOI vs. bulk: S&H output voltage as a function of temperature © [63].

After a parametric simulation of the output voltage with a temperature change, the extreme corners are plotted in Fig. 3.4. In bulk technology, there was a 0.25 V rise in the offset voltage with an increase in temperature, but the V_{p-p} value remained constant. Contrarily, for SOI, there was hardly any rise in the offset voltage with a temperature change, but the V_{p-p} value was increased by 0.2 V. This transient analysis shows the SOI sensor provides a more robust result at elevated temperatures, as expected. This result further explains the previous effects on waveforms caused by process variations, not by temperature, for SOI technology, since the waveform is not altered. To sum up, SOI seems to be very sensitive to process variations.

The Miller amplifier's current source generates 15.6 μA and 11 μA in SOI and bulk, respectively, at ambient temperature. Both currents were proportional to temperature change. The rate of current change with temperature for SOI (62.5 nA/°C) was higher compared to that of bulk (29.1 nA/°C), as observed in Fig. 3.5. One reason for that behavior is the steeper reduction of the threshold voltages of SOI MOSFETs with temperature compared to bulk, resulting in higher current and faster performance. As far as the leakage current is concerned, at the nominal temperature, a higher current was monitored in bulk (12.4 pA) compared to SOI (2.88 pA) S&H sensors, as expected. One interesting observation was the exponential increase of the leakage current for bulk compared to SOI with rise in temperature; e.g. at 80°C, the amount of leakage current was 80 pA and 3.8 pA in bulk and SOI sensors, respectively.

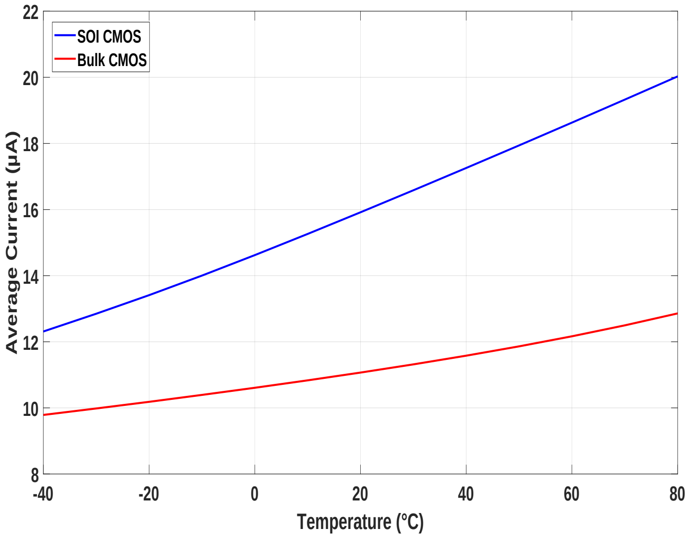


Figure 3.5: SOI vs. bulk: Miller amplifier source average current as a function of temperature © [63].

SOI technology lowers the junction capacitances and allows the circuits to work at a more reduced power maintaining identical speeds [72]. Lower power consumption seems to be the most distinguished advantage SOI has over bulk. The power consumption of the sensors was evaluated at the output node of the S&H voltage sensor. The consumed power (4.5 mW) was lower in SOI technology than in bulk

(6.8 mW), even though output impedances were the same. Fig.3.6 shows the variation of power consumption as a function of temperature. It can be seen that power is inversely proportional to temperature, showing a gradual reduction of 0.6 mW in the considered temperature range for both technologies. However, for SOI, power consumption remains constant between 0 and 20 °C. The decrease in power consumption with temperature is linked to reducing mobility in MOSFETs, hence their drain current.

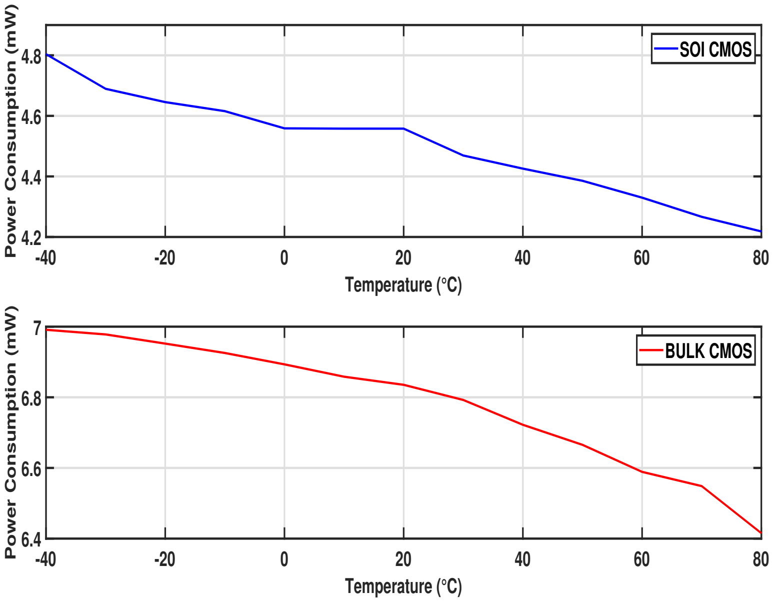


Figure 3.6: SOI vs. bulk: power consumption of the S&H voltage sensor as a function of temperature © [63].

To summarize, this case study investigates a S&H voltage sensor, designed in SOI and bulk technologies, when subjected to process, voltage and temperature variations. Compared to bulk technology, the SOI on-chip sensor has lower power consumption (by 2.2 mW in average) and leakage supply current (by 9.5 pA at 27°C), higher sensitivity to process variations (up to 88% additional slew rate versus 39% at 80°C), higher resilience to temperature changes (6% in output voltage), and a larger occupied area.

3.3 Case Study 2: 6T & 9T SRAM Cells

With the rapid pace of ICs technologies to reduce their dimensions and power consumption, they are more susceptible to conductive EM disturbances, and consequently, maintaining improved EMC characteristics has become much more challenging. SRAM cells are in integral part of ICs and memory circuits. The main concerns for the SRAM cell design include maintaining a higher data stability as well as a lower power dissipation and leakage current [73]. A suitable technology for such characteristics is the SOI CMOS process. ICs designed with SOI can have faster performance, lower switching losses and higher integration. In literature, there exists several works reporting the stability and performance of different architectures of SRAM cells designed in various nanometer bulk CMOS technologies [74], [75]. However, those designs have not yet been implemented in SOI benefiting from reduced substrate losses and withstanding harsh environments (e.g. high temperature and humidity).

In this case study, both 6T & 9T SRAM cells were designed and simulated in 5 V 180 nm SOI and bulk technologies. Process & temperature (PT) variation simulations were carried out on both SRAM cells in each technology to comparitively study their performance. Parametric analysis was performed at extreme corners with the aim to show robustness of SRAM cells in SOI compared to bulk under extreme conditions, sweeping the relevant electrical parameters such as current, voltage and power noise margins, static power dissipation and leakage current. The voltage and current transfer characteristics were monitored using the SNM butterfly curve and the N-curve metric, respectively. Details of the design and parameters of 6T & 9T SRAM cells intergrated into the PETER_ESEO IC can be found in Seciton 2.2.3.

3.3.1 SRAM Cell Stability Metrics

The SNM metric helps to determine the data stability of the SRAM cell. It is modelled by plotting the butterfly curve and measuring the side of the longest square created between the cross-coupled inverters [76]. For the considered SRAM cells, the SNM was monitored at the Q and QB output pins by subjecting the inputs of the inverter circuits to two equal and opposite independent DC voltage sources ranging from 0 V to 5 V. The disadvantage of measuring the SRAM stability through the SNM metric is that it does not support the characterization of the supply current and the write ability.

In comparison, the N-curve metric provides information about the current and voltage of the SRAM cell in a single plot [77]. In the simulation setup, an independent DC voltage was connected between the QB and ground pins. The DC voltage sweep was performed and the supply current, voltages and power were monitored for each operational mode of the SRAM. These results were extended to power metrics from which the data stability and write ability of the SRAM is calculated. The variables derived from the N-curve are the following:

- read current noise margin (RINM) & read voltage noise margin (RVNM) indicate the peak current and the maximum tolerable voltage, which can alter the contents of the SRAM cell in read mode.
- write trip current (WTI) & write trip voltage (WTV) are the minimum current and voltage required to write data into the SRAM and are found from the read N-curve.
- critical current (CI), derived from the write N-curve, is needed to write data in the SRAM cell without failure.
- read power noise margin (RPNM), the product of the RINM & RVNM, shows the highest power necessary to make the SRAM fail to read the data.

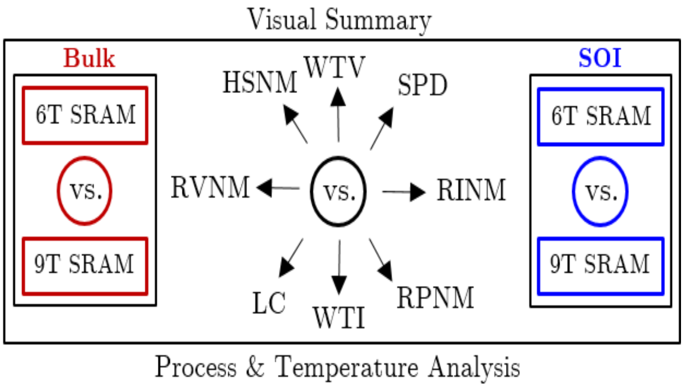


Figure 3.7: Visual summary of the stability and PT analysis of 6T & 9T SRAM cells (SOI vs. bulk) © [64].

The rise in leakage current (LC) and the resulting static power dissipation (SPD), are also important to determine the stability of SRAMs and are increasingly becoming a significant source of the total power consumption [78]. SOI technology lowers the junction capacitances and allows the circuits to work at a more reduced power preserving identical speeds [79]. Lower power dissipation and leakage current seem to be the most distinguished advantage SOI has over bulk. For all SRAM circuits, the LC is measured between the supply voltage and ground while all the access MOSFETS are turned off, retaining data for a particular period of time. The SPD is calculated from the leakage current and the variation in power supply. The comparison of these stability parameters for 6T & 9T SRAM cells in SOI and bulk technologies are summarized in Fig. 3.7.

3.3.2 Stability Analysis

This section presents all DC sweep, transient, process and temperature parametric simulations related to the 6T & 9T SRAM circuits in 5 V 180 nm bulk and SOI. The transient simulations were timed to 1 μs. The voltage for DC simulations was swept from 0 V to 5 V with a step size of 0.1 V. While the nominal temperature is 27 °C, the temperature ranges for PT simulations are −40 °C to 80 °C with 5 °C steps. The lowest temperatures recommended by both foundries are identical (−40 °C) whereas the highest temperature for SOI and bulk are 175 °C & 80 °C, respectively. The latter was selected as the maximum temperature limit to have a fair comparison between both processes. For process variations only extreme corners, WS and WP were considered and compared to the nominal (N) process.

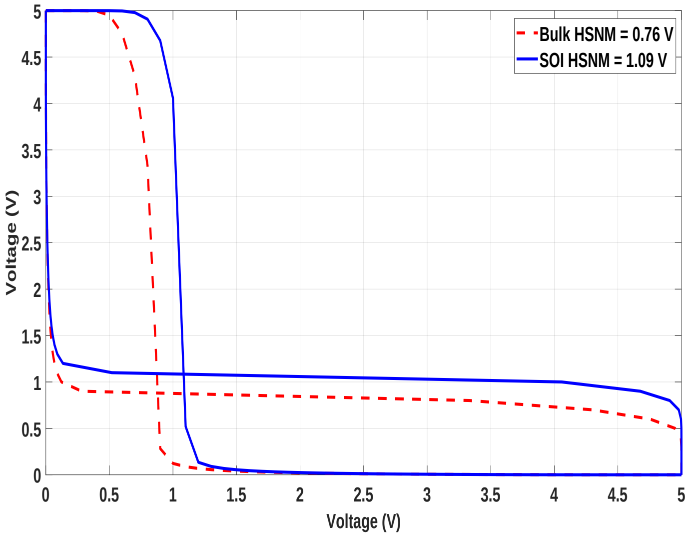


Figure 3.8: SOI vs. bulk: HSNM of 6T & 9T SRAM cells © [64].

The 6T & 9T SRAM circuits are identical during the hold and write operations. To characterize the SRAM cells designed in SOI and bulk, the hold SNM (HSNM) is plotted using the butterfly curve as seen in Fig. 3.8. The blue and red curves represent the HSNM for both 6T & 9T SRAM cells designed in SOI and bulk, respectively. It is observed that the HSNM of the SOI SRAM (6T & 9T) surpasses that of bulk by 0.33 V. Even though both circuits have identical dimensions, the SRAMs designed in SOI perform more efficiently than bulk in the retention mode. The reason behind this is that the former has lower parasitic junction capacitances in its cross-coupled inverters [80].

For a comparison in the write mode, the write N-curve metrics of both 6T & 9T SRAM cells designed in SOI and bulk are plotted in Fig. 3.9. The parameter to analyze is the CI, which is monitored at the lowest peak of the curve before it becomes stable. A lower CI ensures that a smaller current is required to write the data into the SRAM without failure. The CI of the bulk SRAM (6T & 9T) is higher compared to that of SOI by 0.83 mA. The cause of this variation is that the sub-threshold voltage swing of the SOI MOSFETs is lower than bulk, resulting in a reduced gate current required for switching [81].

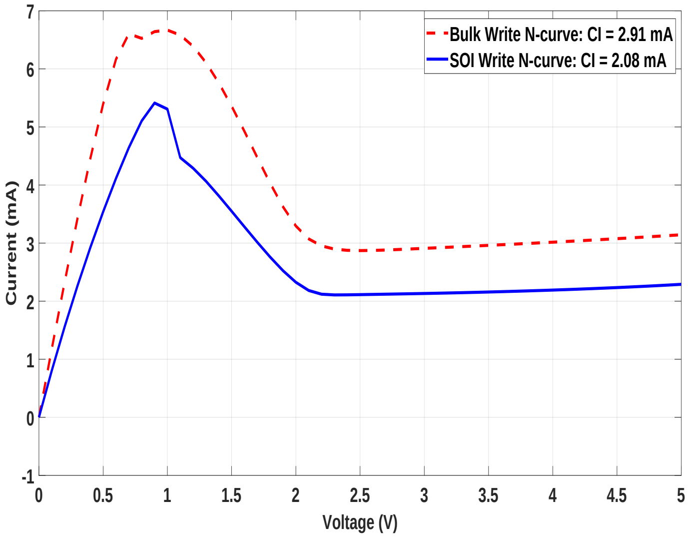


Figure 3.9: SOI vs. bulk: write N-curve metric of 6T & 9T SRAM cells © [64].

The significant difference between the 6T & 9T SRAM cells is in the read operation. Fig. 3.10 illustrates four distinct read N-curves for the SRAM cells designed in bulk and SOI at nominal conditions. It is evident that the RINM, RVNM, WTI and WTV parameters are higher for the 9T compared to the 6T for both SOI and bulk processes. These results prove that the 9T SRAM has better tolerance to DC noise as well as enhanced write ability than the 6T SRAM due to the isolation of the read current path by using MOSFETs of minimum feature size. However, the response of both SOI and bulk is divergent when it comes to the topology of the SRAM circuits. For the 6T SRAM, the SOI version has larger RINM & RVNM but lower WTI & WTV than the bulk version. This demonstrates that in the case of the 6T SOI SRAM, higher data stability is achieved with a lower write ability than bulk. Alternatively, for the 9T SRAM, the bulk version has a predominantly larger RINM, WTI & WTV but a smaller RVNM compared to SOI. To better analyze the results, the RPNM is calculated for all four circuits. The 9T SOI SRAM has the most significant value of RPNM among all circuits, which indicates the highest tolerance to DC noise during the read operation.

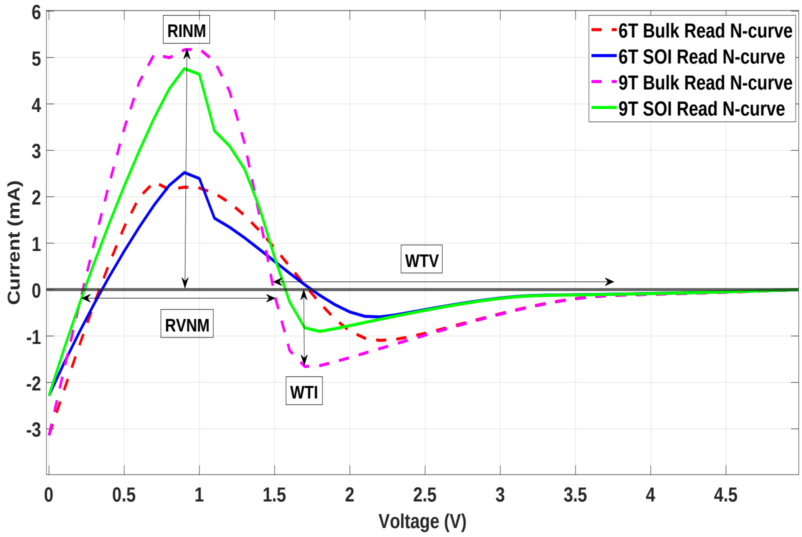


Figure 3.10: SOI vs. bulk: read N-curve metric for 6T & 9T SRAM cells © [64].

The values of LC and SPD are notably lower for SOI than bulk (6T & 9T) SRAM cells. This observation is due to the SOI process allowing fewer leakage effects and ensuring better power consumption. Whatever the technology, the 9T has a smaller LC & SPD in comparison to the 6T SRAM.

A summary of the results are given in Table 3.3. The following observations were made:

- SRAMs designed with SOI has enhanced data stability and power metrics but a worse write ability than the bulk versions.

- 9T SRAM has better noise metrics than the 6T SRAM and combining it with SOI shows a more robust performance.

Table 3.3: SOI vs. Bulk: Parameters of 6T & 9T SRAM Cells at Nominal Conditions (T = 27 °C, P = N) © [64]

Parameter	6T SRAM (bulk)	6T SRAM (SOI)	9T SRAM (bulk)	9T SRAM (SOI)
RINM	2.32 mA	2.54 mA	5.17 mA	4.89 mA
RVNM	1.31 V	1.39 V	1.35 V	1.45 V
WTI	1.09 mA	0.64 mA	1.65 mA	0.98 mA
WTV	1.95 V	1.91 V	2.50 V	2.44 V
LC	2.73 μA	1.61 μA	1.45 μA	0.77 μA
RPNM	3.04 mW	3.53 mW	6.92 mW	7.09 mW
SPD	13.65 μW	8.06 μW	7.23 μW	3.82 μW

3.3.3 PT Corner Analysis

PT variations can rapidly affect the sensitivity of the CMOS circuit performance. The process variations are the critical design parameters (die-to-die) in the semiconductor design technology that precisely controls the functionality of the design at the nanometre level [82]. These include film thickness, impurity concentration densities, lateral dimensions and diffusion depths. These variations causes a mismatch, which results in a reduced yield of SRAM arrays in different technologies. All circuits have temperature variations because of the power consumption linked to the switching of the CMOS transistors. A rise in temperature will reduce the mobility, threshold voltage and increase the propagation delay of the MOSFETs. However, the temperature surge will also result in the faster switching of the transistors and accelerate performance. This will impact the voltage and current noise margins for the SRAM cells. Therefore, a PT corner analysis is performed on both 6T & 9T SRAM designs in SOI and bulk CMOS technologies to compare the effects.

Table 3.4: 6T SRAM Bulk Parameters Change with PT © [64]

Parameter	T = −40 °C P = N (C1)	T = −40 °C P = WS (C2)	T = 80 °C P = N (C3)	T = 80 °C P = WP (C4)
RINM	3.61 mA	3.68 mA	1.49 mA	1.44 mA
RVNM	1.41 V	1.47 V	1.25 V	1.22 V
WTI	1.52 mA	1.25 mA	0.87 mA	0.99 mA
WTV	2.26 V	2.11 V	1.62 V	1.74 V
LC	2.02 μA	1.94 μA	3.85 μA	3.91 μA
RPNM	5.09 mW	5.40 mW	1.86 mW	1.76 mW
SPD	10.11 μW	9.70 μW	19.39 μW	19.62 μW

Table 3.5: 6T SRAM SOI Parameters Change with PT © [64]

Parameter	T = −40 °C P = N (C1)	T = −40 °C P = WS (C2)	T = 80 °C P = N (C3)	T = 80 °C P = WP (C4)
RINM	3.11 mA	3.69 mA	2.12 mA	1.44 mA
RVNM	1.46 V	1.44 V	1.37 V	1.23 V
WTI	0.78 mA	0.66 mA	0.59 mA	0.63 mA
WTV	2.01 V	1.94 V	1.87 V	1.90 V
LC	1.52 μA	1.10 μA	2.15 μA	3.06 μA
RPNM	4.54 mW	5.45 mW	2.90 mW	1.77 mW
SPD	7.60 μW	5.52 μW	10.75 μW	15.31 μW

A DC parametric simulation was performed on each SRAM circuit with extreme temperature and process variations while keeping the supply voltage constant at 5 V. Only at four specific corners reasonable changes in the stability parameters of each design were observed. C1 & C3 corners characterize the effect of extreme

Table 3.6: 9T SRAM Bulk Parameters Change with PT © [64]

Parameter	T = −40 °C P = N (C1)	T = −40 °C P = WS (C2)	T = 80 °C P = N (C3)	T = 80 °C P = WP (C4)
RINM	7.53 mA	7.71 mA	4.00 mA	3.84 mA
RVNM	1.52 V	1.57 V	1.10 V	1.04 V
WTI	1.84 mA	1.67 mA	0.98 mA	1.05 mA
WTV	2.98 V	2.11 V	1.62 V	1.79 V
LC	0.93 μA	0.90 μA	1.99 μA	2.24 μA
RPNM	11.44 mW	12.10 mW	4.41 mW	3.99 mW
SPD	4.65 μW	4.48 μW	9.96 μW	11.13 μW

Table 3.7: 9T SRAM SOI Parameters Change with PT © [64]

Parameter	T = −40 °C P = N (C1)	T = −40 °C P = WS (C2)	T = 80 °C P = N (C3)	T = 80 °C P = WP (C4)
RINM	5.56 mA	6.85 mA	4.14 mA	3.92 mA
RVNM	1.49 V	1.66 V	1.38 V	1.12 V
WTI	1.11 mA	1.67 mA	0.91 mA	1.05 mA
WTV	2.87 V	2.23 V	2.06 V	2.38 V
LC	0.62 μA	0.49 μA	1.23 μA	1.55 μA
RPNM	8.28 mW	11.37 mW	5.72 mW	4.40 mW
SPD	3.09 μW	2.46 μW	6.15 μW	7.74 μW

temperatures only and the C2 & C4 show the combined effect of process and temperatures for each SRAM cell. Here follows a summary of the obtained results given in Table 3.4 to Table 3.7.

Monitoring C1 & C3 shows that the RINM, RVNM, RPNM, WTI & WTV are inversely proportional to temperature for all SRAM cells. The rise in temperature increases mobility and reduces the threshold voltage of individual MOSFETs, thus, resulting in a lower noise margin and trip voltages for bulk & SOI processes. When comparing both the topologies (Table 3.4 & Table 3.6), the read noise margins and write trip metrics for 9T SRAM cells are more impacted by temperature than the 6T SRAM cells. The reason is that the former has more NMOS transistors leading to a higher variation in the differential pull-down effect. An interesting observation is that the deviation of these stability parameters is more prominent in bulk than SOI versions of the 6T & 9T SRAM circuits (Table 3.4 & Table 3.5). This demonstrates that, compared to bulk technology, the SRAM cells designed in SOI are more resilient to DC noise and write failure when subjected to drastic temperature changes.

The LC and SPD parameters were found to increase for the SRAM circuits at the same corners with the temperature rise. This behavior is due to the decrease of the threshold voltage of NMOS transistors at higher temperatures, which leads to a substantial increase in gate leakage. As described previously, those mentioned parameters are higher for bulk compared to SOI. In contrast to SOI, there is an exponential surge in the LC & SPD of bulk 6T and 9T SRAM cells with temperature (Table 3.4 & Table 3.6). This is due to the fact that bulk does not have a buried insulation layer, which decreases the effect of temperature on leakage path associated with the drain and source of MOSFETs.

At corners C2 & C4, the combined effect of process and temperature is analyzed for all read noise margins and write trip parameters. As expected, RINM, RVNM & RPNM are inversely proportional to process and temperature for all four circuits (Table 3.4). A faster process (WP) and greater temperatures result in quicker switching of the MOSFETs, escalating their mobility and further diminishing the threshold voltages. Contrarily, the WTV and WTI are either increased or decreased slightly at C2 & C4 corners, respectively, with the effects of process and temperature competing against each other. A quicker process (WP) improves the write ability of the SRAM cells. All read and write parameters of the SOI versions of the SRAM cells are more sensitive to process variations compared to bulk. The 9T SOI SRAM cell shows the highest variation with respect to process among all circuits due to the higher number of MOSFETs (Table 3.6). As far as the LC and SPD are concerned at C2 & C4, the variation in SOI SRAM cells is higher compared to that in bulk. The power dissipation of the SOI version of the SRAM cells (6T & 9T) is less impacted by temperature and is more susceptible to process changes (Table 3.5 & Table 3.7).

To summarize, the read data stability, write ability and power metrics of the 6T & 9T SRAM cells designed in SOI are more resistant to changes in temperature and sensitive to process variations compared to bulk technology. The read parameters and power metrics are inversely and directly proportional to the combined process & temperature changes, respectively. Nevertheless, the write ability of all SRAM cells improves with a faster process. The read noise margins and power dissipations of 9T SOI SRAM are the most immune metrics to temperature changes. As far as the 6T bulk SRAM is concerned, it is the least susceptible to process variations among all schematics.

3.4 Conclusion

With the aim to compare SOI and bulk, two case studies (S&H voltage sensor and SRAM cells) were analyzed under extreme conditions (process and temperature variations). Compared to bulk technology, the SOI based S&H voltage sensor had better power/stability metrics but was susceptible to process variations and occupied a larger size. As far as the 6T & 9T SRAM cells are concerned, the ones designed in SOI exhibited better data stability, lower leakage supply current and power dissipation and a higher resilience to temperature changes. However, the SOI SRAMs have reduced write ability and greater sensitivity to process variations in comparison with bulk SRAMs. The SOI version of the 9T SRAM cell was found to have the best specifications among both topologies.

The results from these independent case studies demonstrates that the analog structures developed in SOI are more resilient to thermal stress and have lower power dissipation compared to bulk. This makes SOI a promising approach to develop robust structures for mixed-signal/RF applications.

CHAPTER 4

MULTITONE CONDUCTED EM IMMUNITY ANALYSIS

The main results of the study in Sections 4.1, 4.2 and 4.3 have been published in [83]–[85]. For Section 4.4, results are presented in [86]. The study of multitone conducted EM immunity analysis of ICs was a collaborative work between the author and Lokesh Devaraj from HORIBA MIRA/De MontFort University under the Horizon 2020 MSCA ETN PETER project. All results in this chapter have been published jointly in those respective journals.

Lokesh Devaraj's contribution was developing and providing the theoretical framework behind the proposed BN-based probabilistic models. The author's main work includes simulation based transistor modelling and experimental validation of the proposed BN models to predict the multitone EM immunity of specific ICs for higher order tones. Further, the author carried out experimental characterization in order to analyze the influence of thermal stress on the multitone EM immunity of integrated oscillators with different topologies.

4.1 Importance of Multitone EM Analysis

The EM immunity performance of electrical and electronic (E/E) systems generally varies with the frequency of coupled EM disturbances. The standard testing procedure to verify the immunity of E/E systems currently includes the use of *single-tone* (i.e., single frequency) continuous waveforms. However, in the real world, most complex systems operate in a dynamic multitone environment i.e., simultaneously occurring EM disturbances with different frequencies.

For multitone immunity of the E/E systems, the components at different hierarchical levels of the system are tested with single-tone disturbances at an amplitude equivalent to, or higher than, the net amplitude of all reasonably foreseeable noise sources that are expected to occur simultaneously in the EM environment of the system [87]. To check the validity of this assumption, a case study of an IC simulation model was considered in [88] to compare the EMI impact due to single-tone and multitone disturbances. In that study, the amplitude of each single-tone was considered equal to the net amplitude of the multitone disturbances. The results showcased that single-tone disturbances have a higher probability malfunction due to EMI when compared to multitone disturbances for a specific IC. Thus, indicating that the ICs/systems which pass single-tone immunity testing can be expected (but not certain) to have adequate immunity to multitone disturbances that may in practice be encountered in its operational environment.

However, it should be noted that it is technically and economically impracticable to determine the exact (or even the worst case) net amplitude of all possible EM disturbances for those systems which have a dynamic EM environment (e.g., systems in road vehicles). Other reasons to why the current single-tone immunity testing (at field strength equal to, or higher than the multitone disturbances) approach will be insufficient or fail for complex system like road vehicles are given as follows:

- there can be new technologies (emerging over the lifetime of the system) acting as external noise sources, which are unknown during system design and development phase;
- increase in the proportion of E/E components integrated in to a system, leading to higher number simultaneous noise sources. Thus requiring manufacturers to consider a much higher field strength for single tone immunity testing over the entire RF spectrum;
- expensive and time consuming process of EMC design of E/E components to satisfy the stringent single-tone immunity verification requirements [89];
- the need to include inter-modulation products of the multitone disturbances during the single-tone immunity testing;

In literature, several researches have discussed the importance of multitone immunity testing [90], [91] and its benefits [92]. It is worth mentioning that, the international standard IEC 61000-4-3 [93] has recently included multitone testing for reducing the dwell-time during immunity testing, which can also potentially represent the real world system EM environment.

4.1.1 Types of Multi-Causal Interactions

The significance of multi-causal EMI analysis (or *multitone analysis*) is very clear for all system-critical E/E that must operate in a multitone environment. Hence, to study the variations in multitone performance due to the intrinsic non-linear behaviour of some E/E systems, inter-modulation effects and other uncertainties, it is important to identify the type of interactions between simultaneously occurring single-tone disturbances. In general, causal interactions between multiple causes leading to a common effect can be classified in to two main groups. Those multi-causal interactions which increase the probability of observing an effect when compared to their individual probability values are of type *positive causality*, whereas, when the probability of observing the multi-causal effect is less than at least one of the individual causes, then the interaction is classified as type *inhibition* [94].

Recent studies involving both simulations [85] and experimental measurements [86] of ICs have demonstrated the possibility of both positive causality and inhibition type interactions of multitone disturbances to cause EMI failures. The former may mean that systems that pass a single-tone test may still be susceptible to multitone EMI, whereas, the latter case may mean that systems are less susceptible to multitone EMI than to single-tone EMI, which could lead to over engineering and unnecessary expenses for EMC design.

4.1.2 Challenges

Current standards that are relevant for the measurement of conducted or radiated EM immunity of E/E systems recommend testing with disturbances having frequencies that are linearly or logarithmically distributed within a specific range of frequencies. Hence, with respect to the number of frequencies considered, the single-tone immunity testing is a linear problem in terms of cost and measurement time, whereas, multitone testing is an exponential problem. This is because, multiple EM disturbances occurring simultaneously superimpose with each other constructively and/or destructively in time, and depending on the parameters of the waveform i.e., frequency, initial phase and amplitude of each simultaneously occurring disturbance, there is an infinitely large number of possible multitone waveforms that could be considered for the analysis.

Multitone immunity analysis using experimental measurements becomes impractical due to amplifier saturation, for a potentially infinite number of simultaneous single-tone EM disturbances. The use of simulation tools offers some advantages over the measurements in that aspect. However, it is still not possible to consider all possible multitone combinations.

The application of BNs to overcome some of those challenges will be discussed in this chapter. The case studies of two oscillator circuits with different topologies have been considered for verification and validation of the proposed BN models for multitone EM immunity analysis.

4.2 Multi-Causal Baysian Network Models

In many domains, discrete BNs are used to model the relationship between multiple causes and a common effect by considering the occurrence of causes as the parent node variables and observed effect as a child node variable. A fundamental problem of using such multi-causal BNs is the exponential growth of conditional probability distribution (CPD) entries that are required to be elicited by the expert. For multitone analysis, if occurrence of (n) EM disturbances having different frequency values are considered as the set of binary causes, $\mathcal{X}$, and the observed impact due to EMI (e.g., failure or no failure) as the binary effect, E, then, an IC/system expert needs to provide the probability of EMI failures due to all possible non-repeating combinations. For n singletone frequencies that are considered for multitone analysis, the total number of all possible non-repeating combinations of multitone disturbances C_r^n, generated with superposition of r simultaneously occurring singletone disturbances can be simply calculated using:

$$C_r^n = \frac{n!}{r!(n-r)!} \tag{4.1}$$

where, $n!$ denotes the factorial of an integer n. For example, r simultaneous tones, i.e., $\sum C_r^n$, for $r = 2$ to n, would require $2^n - n - 1$ multitone immunity analyses, making multitone immunity verification testing economically impracticable. A possible way to limit the total number of tests required for multitone analysis without compromising the number of frequencies analysed could be to predict the impact of untested multitone disturbances from the tested ones. Some of the existing prediction techniques that have been used in multi-causal BN analysis are discussed further.

4.2.1 Noisy-OR Model

The *noisy-OR* model is a very popular deterministic function that was introduced by Pearl [95], [96] to reduce the exponential blow up CPD entries for the effect node in multi-causal BNs to a linear problem. This was achieved based on the assumption of *causal independence*, according to which the causal mechanisms of simultaneously occurring causes are independent of each other. Hence, to estimate the probability of observing the common effect due to higher order combination of causes, the probability values corresponding to each individual cause leading to the effect are sufficient.

Consider a set of t binary-variables, $\mathcal{X} = \{X_1, X_2, ..., X_t\}$, where each variable $X_i \in \mathcal{X}$ represent the presence ($X_i = x_i$) or absence ($X_i = \bar{x}_i$) of a cause (a unique single-tone disturbance), and a binary-variable E, that corresponds to observing an effect ($E = e$, a failure) or no effect ($E = \bar{e}$, no failure). Using the causal independence assumptions of the noisy-OR model [97], the deterministic function to estimate the conditional probability of observing an effect (failure) for a given subset of causes (single-tone disturbances) $\mathbf{X} \subseteq \mathcal{X}$ that are assumed to be occur simultaneously is given by:

$$\mathcal{N}(e|\, \mathbf{X}) = 1 - \{(1 - \lambda) \prod_{t=1}^{n} [1 - \mathcal{P}(e|\, x_t)]\} \tag{4.2}$$

where n is an integer, equal to the number of simultaneous causes (i.e., the size of $\mathbf{X}$), $\mathcal{P}(e|\, x_k)$ is the individual probability of each cause $x_k \in \mathbf{X}$ leading to the effect (obtained from an expert) and λ is the *leak probability* [98], which corresponds to the probability of observing an effect when all causes are absent (i.e., $\mathbf{X} = \emptyset$). Hence, during multitone analysis it possible to include the overall probability of system failure due to other causes of failure (obtained from functional safety or cybersecurity analysis) using the leak probability of the noisy-OR model. The noisy-OR estimated probability values are denoted using $\mathcal{N}$. In the remaining parts of the manuscript, the conditional probability of observing a failure given the set $\mathbf{X}$ of simultaneous single-tone disturbances, i.e., $\mathcal{N}(e|\, \mathbf{X})$ is denoted using the short-hand notation $\mathcal{N}_{\mathbf{X}}$.

The probability of any multi-causal effect estimated using the causal independence assumption (using noisy-OR model) is always of type positive causality. The latter state is attained, if the probability of multitone EMI failure is estimated to be greater than the probability of EMI failure due to each individual single-tone disturbance considered. This property of the noisy-OR model can be used to estimate multitone failure probabilities with a reliable margin when the interactions between single-tone disturbances are of type inhibition.

An additional benefit of using the noisy-OR model is to identify the existence of *causal dependence* between simultaneously occurring single-tone disturbances. Since the noisy-OR model assumes causal independence to calculate the probability of multitone failure, any inequality between the noisy-OR estimate and the multitone probability values obtained by the expert from simulations/experiments, $\mathcal{P}(e|\,\mathbf{X})$ denotes existence of causal dependence between simultaneously occurring single-tone disturbances.

Multi-causal interactions of type positive causality are further classified in [94] as *synergy* and *interference* upon comparison with the noisy-OR estimates. The former is when $\mathcal{P}(e|\,\mathbf{X}) > \mathcal{N}(e|\,\mathbf{X})$ and the latter is when $\mathcal{P}(e|\,\mathbf{X}) < \mathcal{N}(e|\,\mathbf{X})$. In this thesis, the term interference is replaced with *asynergy* to avoid confusion with the *electromagnetic interference* effects that are the subject of multi-causal prediction and analysis.

4.2.2 Recursive Noisy-OR Model

As an extension of the noisy-OR model, Lemmer and Gossink proposed the recursive noisy-OR (RNOR) model in [94] to allow any known causal dependence information between multiples causes that is provided by the expert to be included during the multi-causal prediction, in addition to the noisy-OR assumptions. For more than two simultaneously occurring causes, $n > 2$, the RNOR rule is given by:

$$\mathcal{R}_{\mathbf{X}} = \begin{cases} \mathcal{P}_{\mathbf{X}}, \\ \text{if available} \\ 1 - \displaystyle\prod_{j=0}^{n-1} \left[\frac{1 - \mathcal{R}_{\mathbf{X}\setminus\{x_{j+1}\}}}{1 - \mathcal{R}_{\mathbf{X}\setminus\{x_{j+1}, x_{\mathrm{mod}\,(j+1,n)+1}\})}} \right], \\ \text{otherwise} \end{cases} \tag{4.3}$$

where $\mathrm{mod}(a,b)$ denotes the modulo operation on integers a and b, '$\mathbf{X}\setminus$' denotes set-subtraction from $\mathbf{X}$, and $\mathcal{R}_{\mathbf{X}}$ indicates the probabilities that are estimated using the RNOR. Use of the modulo function requires an index j running from 0 in the product, but the resulting indices are incremented by 1 to maintain consistency with the cause numbering $\{X_1, X_2.., X_n\}$. The RNOR model simply reduces to the noisy-OR model if no causal dependence information is available or if $n = 2$.

There are two limitations of using the RNOR rule. First, the $\mathcal{R}_{\mathbf{X}}$ estimates can be out of range $[0, 1]$ if the causal dependence information provided by an expert is/are of type inhibition, thus leading to the violation of the probability theory. The second limit is due to the *asymmetry problem* of the RNOR model discussed in [99].

According to the RNOR deterministic function given in (4.3), to predict the probability of an effect due to n simultaneous causes, the probability values corresponding to non-repeating combinations of $(n-1)$ causes in the numerator and $(n-2)$ causes in the denominator have to be used. For example, assume that the probability values corresponding to the lower-order combination of causes $(n-1, n-2)$ are provided by the expert, then the RNOR function for any four causes, $\mathbf{X} = \{x_1, x_2, x_3, x_4\}$ using (4.3) is given as:

$$\mathcal{R}_{x_1,x_2,x_3,x_4} = \\ 1 - \left[\frac{(1-\mathcal{P}_{x_1,x_2,x_3})(1-\mathcal{P}_{x_1,x_3,x_4})(1-\mathcal{P}_{x_1,x_2,x_4})(1-\mathcal{P}_{x_1,x_2,x_3})}{(1-\mathcal{P}_{x_3,x_4})(1-\mathcal{P}_{x_1,x_4})(1-\mathcal{P}_{x_1,x_2,})(1-\mathcal{P}_{x_2,x_3})}\right] \quad (4.4)$$

In this example, where $n = 4$, the number of non-repeating combinations, C_r^n (where r is an integer denoting the number of lower-order combinations of n) for any two of the four causes is $C_{r=n-2}^n = 6$. Notice that the two of those six possible combinations, i.e., $\{x_1, x_3\}$ and $\{x_2, x_4\}$ are missing in the denominator of (4.4). Since the number of terms in the numerator and denominator of (4.3) is always equal, for any integer $n > 2$, the number of combinations that will not be included is equal to $C_{r=n-2}^n - C_{r=n-1}^n$. The asymmetry problem is because of the inconsistencies of RNOR estimates arising due to the fact that the combinations that are not included in (4.3) purely depend on the arrangement of causes in $\mathbf{X}$. In the previous example, if the arrangement of $\mathbf{X} = \{x_2, x_1, x_3, x_4\}$, then the missing combinations would have been $\{x_2, x_3\}, \{x_1, x_4\}$ instead of the previously missing terms $\{x_1, x_3\}$ and $\{x_2, x_4\}$. So, unless the probabilities corresponding to all non-repeating combinations of lower-order causes $(r = n-2)$ are equal, the RNOR estimates will be inconsistent. Hence, the asymmetry problem of RNOR rule exists for values of

$n > 3$ multitone frequencies.

4.2.3 Adaptive-RNOR Model

The RNOR rule was validated in [100] for the application of asthma prediction. To avoid the first limitation of the RNOR rule, the inhibition type interactions provided by the expert were replaced with corresponding noisy-OR estimates in [100] to ensure the validity of the predictions made using the RNOR rule. That approach was called as the *adaptive-RNOR* (ARNOR) rule, which is given by:

$$\mathcal{A}_{\mathbf{X}} = \begin{cases} \mathcal{P}_{\mathbf{X}}, \\ \text{if available and } \mathbf{X}\text{: positive causality} \\ \mathcal{N}_{\mathbf{X}}, \\ \text{if } \mathcal{P}_{\mathbf{X}} \text{ is available and } \mathbf{X}\text{: inhibition} \\ \mathcal{R}_{\mathbf{X}}, \\ \text{otherwise} \end{cases} \tag{4.5}$$

Similar to the RNOR rule, the ARNOR rule also reduces to the noisy-OR model when causal dependence information is unavailable, which is also the case if all the available information that is provided by the expert are of type inhibition. Note that, the ARNOR-rule shares the second limitation of its predecessor, i.e., the asymmetry problem.

This was evident when we analysed immunity of multitone of order 4 to 10 in [84]. Further to fix this issue, first, we considered a similar approach used to fix the RNOR rule, i.e., to use the Noisy-OR estimated probability values whenever the lower order multitone disturbances of type inhibition were used to calculate the higher order probability of failure. Hence, a new approach based on the ARNOR model is considered for the multitone analysis in upcoming case studies.

4.3 Case Study of Integrated Oscillators (Simulations)

In recent years, IC technology has increasingly challenged manufacturers with EMC issues. These include maintaining the desired performance of an IC in the presence of conducted and radiated EM disturbances [101]. Based on the guidelines provided in IEC 62132-4 [4], ICs are currently verified using DPI of conducted single-tone RF disturbances into the IC pins. At each frequency, forward power is incrementally raised until reaching the lower of the immunity requirement or the level at which the circuit fails due to loss of its functionality and/or degradation of performance to intolerable levels [102]. However, in the uncertain EM environment, single-tone disturbances can occur simultaneously, hence, additional inter-modulation effects of the resulting multi-tone EM disturbances should perhaps be considered in immunity evaluations.

Simulation techniques, which are routinely used in industry in early stages of IC design, can help investigate and anticipate its susceptibility to multitone EM disturbances [103]. More importantly, the main challenge of multi-tone immunity analysis is the potentially infinite number of single-tone combinations that can be considered. For multitone measurements, however, the number of simultaneous tones that can be used is limited due to amplifier saturation, and also the calibration required for compensating the cable loss / attenuation factor, can lead to additional measurement uncertainties. Consequently, simulation techniques taking into account external parasitics/uncertainties, offer a more practicable approach to investigate relatively large sets of tone combinations, as well as higher orders of multitones.

Oscillator circuits that are integrated into electronic subsystems such as function generators, PLLs etc. [45], are likely to experience a multitone EM environment. Their performance with respect to EM disturbances is not readily predictable due to their non-linear behavior. Hence, the evaluation of IC designs with respect to multitone immunity is desirable to gain confidence in the achievement of their intended performance characteristics. The analysis of the immunity levels of two distinct 3-stage oscillator circuits (i.e. CSVCO & RO), integrated into the PETER_ESEO research mini-ASIC (described in Chapter 2) are investigated using single and multitone disturbances using the probabilistic *noisy-OR* model [85]. Further, to validate the capabilities of the previously described prediction models for multitone immunity analyses, these circuits have been utilized [83].

4.3.1 Simulation Model

The simulation model including the CSVCO and RO circuits included in the PETER_ESEO research chip is illustrated in the Fig. 4.1. The EMI simulations were implemented in the Spectre tool [104]. The CQFP package of the chip was modelled using the IC-EMC software [105], to extract the approximated package model consisting of passive lumped elements found through IC parameters such as die size, pitch, lead frame and cavity sizes.

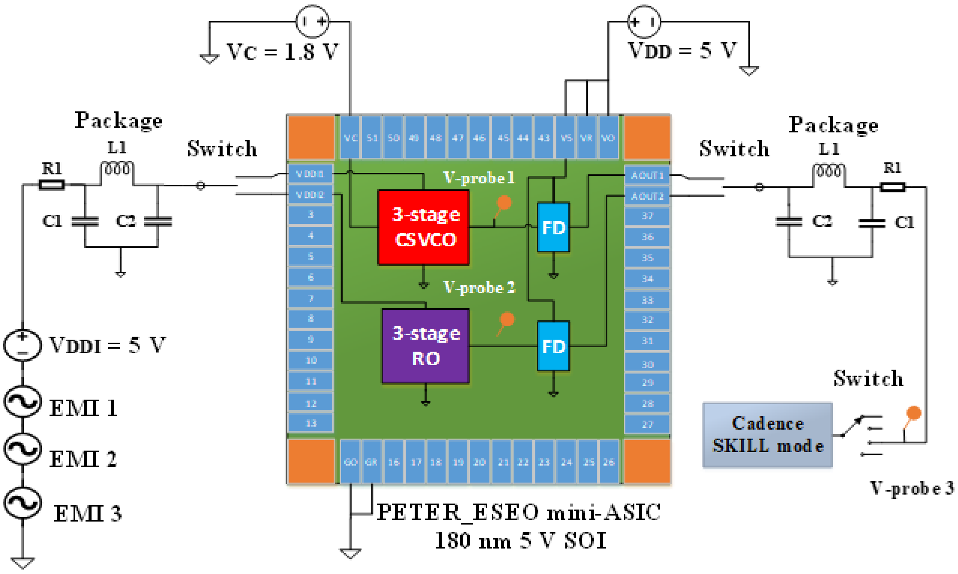


Figure 4.1: Multitone EMI simulation setup for the CSVCO and RO circuits © [85].

The ICs are surrounded by a padring, which includes ESD protection structures to both the supply and ground rails (Fig. 4.1). The global power supply (V_{DD} = 5 V) is connected to the feeding ports V_O, V_R, & V_5 to power up the padring. Hence, to isolate the global feeding ports from injected EM disturbance(s), an isolated biasing supply V_{DDI} that powers up the oscillator circuit was used.

The functions of both oscillators are to provide an output voltage at a nominal frequency F_i, for a given isolated supply voltage $V_{DDI} = 5$ V. To tune the output frequency, the CSVCO is provided with a biasing control supply $V_C = 1.8$ V, whereas, the RO has a buffer at the output stage to stabilize the oscillating signal. Single or multi-tone EM disturbances are injected to the V$_{DDI}$ pad of each circuit to emulate the possibility of simultaneous occurrence of these EM waveforms in the real-world system EM environment. In the simulations, the multi-tone EM disturbances are generated by superposition of single-tones. A digital FD circuit is included in the output stage of both oscillators to reduce the fundamental frequency of the generated signal. The FD circuit is powered by the global V$_{DD}$. The switches ensure that the RF signals injected into the V$_{DDI}$ pad of each oscillator do not interfere with any other inputs. The multitone EMI simulation setup (Fig. 4.1) allowed for up to three simultaneous sinusoidal waveforms or single-tone disturbances (tones 1 to 3) to be injected through the V_{DDI}. To monitor the fluctuations in the output voltages of each VCO without the filtering effects, virtual voltage probes were placed before the FD circuit blocks. For single-tone EMI simulations, the amplitudes of tones 2 and 3 were set to 0 V, and for two-tone EMI the amplitude of tone 3 was set to 0 V. For all simulations, the V_C and V_{DD} pins were assumed to be isolated from EM disturbances.

Each simulation was carried out for a time period of 1 μs, however the EMI noise was added to the input supply after the initial transient response for the duration of 300 ns for both oscillator circuits. The transient response time is the minimum time required for the output voltage of the oscillators to stabilize. The Cadence *SKILL* mode function was then applied to get the fast Fourier transform (FFT) at discrete-time steps of 1.5 ns to obtain the oscillator's output frequency, F_E under EMI conditions. Hence, for the steady-state period of 700 ns, 500 time-steps were collected for each EM disturbance simulation, which took around 7 minutes, including setup, on a high-performance workstation. To investigate the multitone immunity of the two oscillators, 15 different frequencies were chosen in the range of 50−950 MHz. This frequency band was chosen based on IEC 62132-4 [4] and previously identified susceptible frequencies of the tested oscillators [106].

The operating frequency of an oscillator is generally used to evaluate the performance of the circuit with respect to injected EM disturbances [45]. The nominal operating frequency (F_i) of the CSVCO and RO is equal to 703 MHz and 950 MHz, respectively. To determine the performance of each circuit, the output frequency under EM disturbances is monitored at the connecting node before the frequency divider (BFD), as well as at the analog output pin after the frequency divider, output pad and package (AFD).

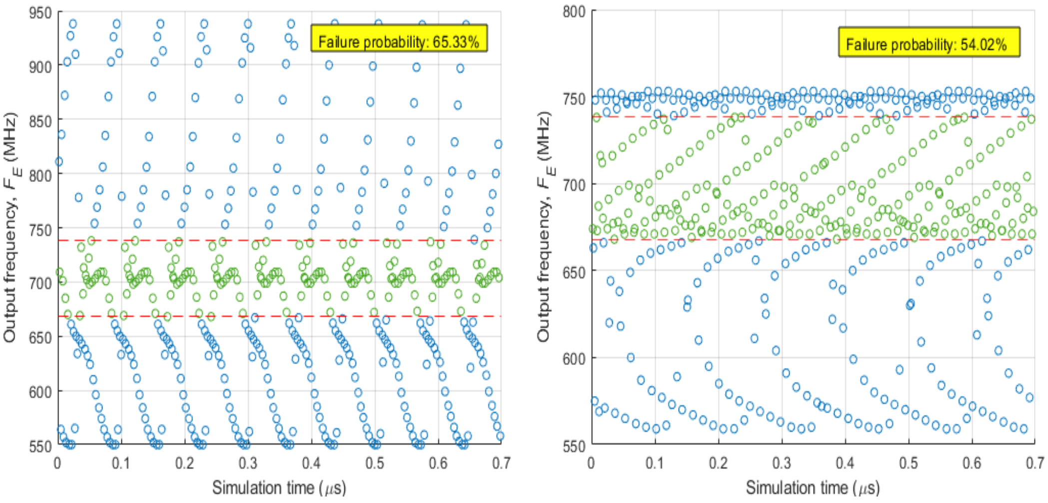
The relative deviation of F_E from the desired F_i is then simply calculated as a percentage value by:

$$\Delta F = 100 \left| \frac{F_E - F_i}{F_i} \right| \tag{4.6}$$

The integrated oscillators were considered to have failed every time the ΔF exceeded the acceptable tolerance of ±5%. The probability of EMI failure is then estimated by dividing the number of such failures by the total number of time-steps under EMI condition. A rise in the number of time-step is proportional to the accuracy to estimate the failure probability from simulations.

4.3.2 Single-Tone EMI Simulations

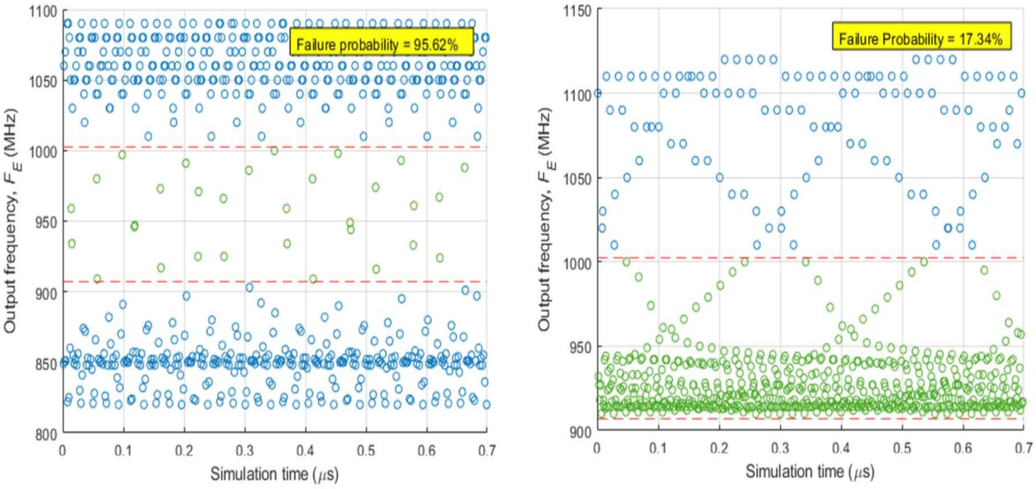
Superposition of up to three single-tone disturbances were considered for this the multitone analysis. To avoid exceeding the maximum conducted immunity requirements of [4], the peak-to-peak amplitude of all single-tone disturbances was fixed as 2 V. The latter value was considered in order to avoid triggering the ESD protection structures which would clamp the injected signal to 5.5 V. The initial phase for single-tone disturbances was zero degrees. Note that, the impact of initial phase is negligible if the monitored period of time is long enough to encompass multiple EM disturbance cycles.



(a) (b)

Figure 4.2: CSVCO output frequency responses for single-tone EM disturbances at a) 450 MHz; b) 800 MHz © [83].

As samples, the output response of the CSVCO and RO circuits upon injection of single-tone disturbances at frequencies 450 MHz and 800 MHz are depicted in Figs. 4.2 and 4.3, respectively. Using the failure criterion in (4.6), the corresponding probabilities of EMI failure for the CSVCO are estimated as, $\mathcal{P}(e|\ 450) = 0.653$ and $\mathcal{P}(e|\ 800) = 0.540$ and similarly, for the RO they are, $\mathcal{P}(e|\ 450) = 0.956$ and $\mathcal{P}(e|\ 800) = 0.173$. Due to the non-linear behaviour of the oscillators, the F_E varies over the duration of the steady-state EMI response. This effect is visible in



(a) (b)

Figure 4.3: RO output frequency responses for single-tone EM disturbances at a) 450 MHz; b) 800 MHz © [83].

Fig. 4.2 and 4.3, which are minor for CSVCO and major for the RO output frequency between successive cycles of EM disturbance, respectively.

Using the specified failure criterion, the probabilities of EMI failure with respect to 15 different frequencies that were obtained for both CSVCO and RO circuits are given in Table 4.1. In this case study, the amplitude of all the single-tone disturbances are considered constant to limit the number of possible multitone combinations. However, the results may vary for different amplitude values. Note that, for calculation purposes the probability values corresponding to *no failure* and a *complete failure* are approximated as 0.0001 and 0.9999 (respectively), and the corresponding entries are displayed in Tables as 0.0 and 1.0. This was done for two reasons; first, to avoid potential errors when applying probabilistic rules [107], [108]; and second, because finite data-sets cannot guarantee that failures are impossible or certain.

Other uncertainties that could affect the EM immunity performance of ICs, in addition to their non-linear behaviour e.g., the environmental factors such as temperature, humidity etc. have to be considered for a comprehensive assessment. However, the effort to collect the relevant data grows exponentially with respect to the number of uncertain factors and single-tone frequencies considered and it becomes impracticable if all possible combinations of multitone disturbances are also

Table 4.1: Probability of CSVCO and RO EMI failure due to single-tone disturbances obtained from simulations © [83]

Single-tone (MHz)	50	100	200	300	350	450	500	550	600	650	700	750	800	900	950
CSVCO															
$\mathcal{P}_\mathbf{X}$	0.849	0.902	0.9	0.854	0.790	0.653	0.679	0.805	0.904	1.0	0.010	0.309	0.540	0.593	0.614
RO															
$\mathcal{P}_\mathbf{X}$	0.786	0.821	0.824	0.796	0.833	0.956	0.934	1.0	1.0	1.0	1.0	0.614	0.173	0.062	0.0

taken in to account; more details on number of combinations is discussed in the following section.

4.3.3 Multitone EMI Simulations

According to C^n_r, the number of non-repeating multitone combinations can rapidly become unmanageable as n and r increase, which is the main reason for limiting the number of frequencies to $n = 15$ and the highest multitone order to $r = 3$. Hence, using (4.1), for $n = 15$ and $r = \{1, 2, 3\}$, a total of 575 simulations consisting of 15 single-tone ($r = 1$), 105 two-tone ($r = 2$) and 455 three-tone combination of disturbances were done for each oscillator circuit, which are sufficient for the practical illustration of multitone analysis and prediction using probabilistic models. Note that, for the analyses of the remaining higher-order combinations, i.e., $3 < r < n$, each oscillator circuit would require additionally 32313 ($2^n - [C^n_1 + C^n_2 + C^n_3]$) simulations, which is computationally intensive and demands high memory requirements.

The generalized expression for the disturbance waveforms having an order r used in the simulations is:

$$V(t, r) = A \sum_{k=1}^{r} \sin(2\pi f_k t + \phi_k) \tag{4.7}$$

where, t is the time, A represents the 2 V amplitude of each of the tones and the initial phase, ϕ_k, was $\phi_1 = 0$ for single-tones (i.e. $k = 1$). To reduce the number of simulations for this study, a random initial phase value was assigned from the range $0 < \phi_k < 360°$ for each superimposed tone (i.e. $k > 1$). It is important to note that the initial phase difference between the simultaneous single-tone disturbances was found to have an impact on the multitone EM failure probability values. In

Fig. 4.4, the impact of initial phase difference between two simultaneous single-tone disturbances on the probability of CSVCO EM failure are illustrated for three different two-tone combinations: $\{50, 60\}$ MHz, $\{450, 800\}$ MHz, & $\{750, 900\}$ MHz.

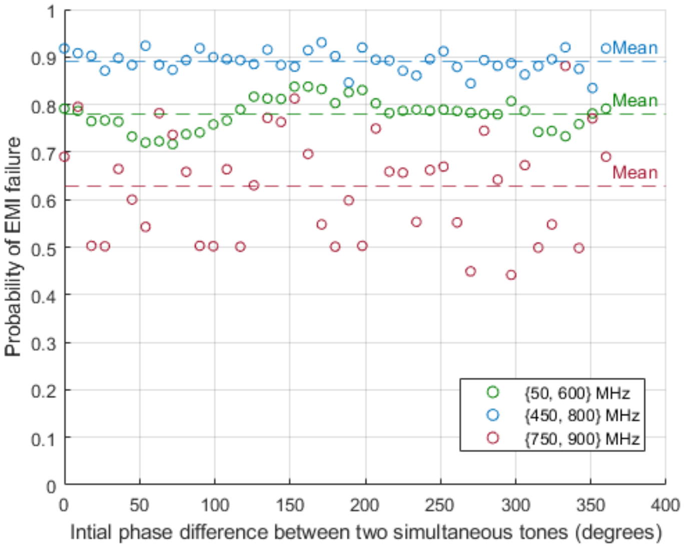


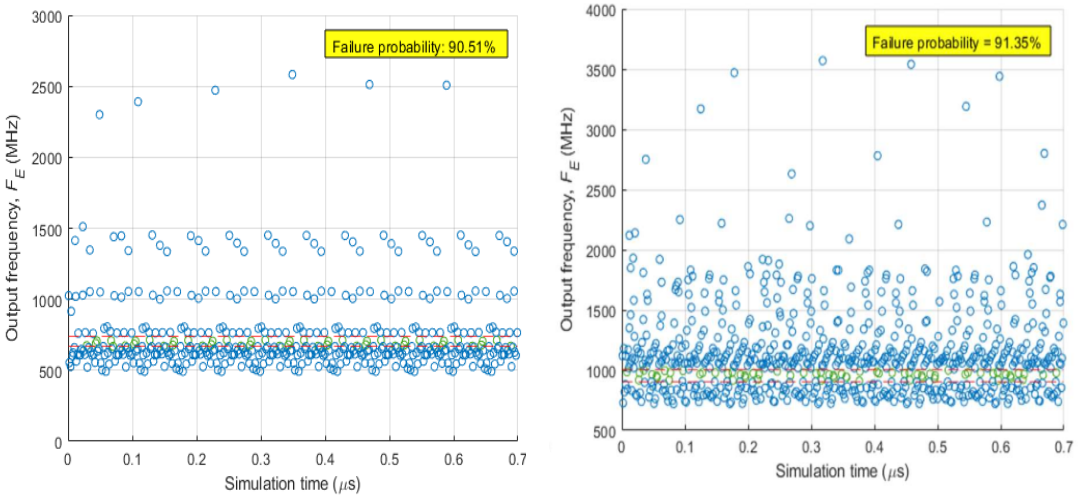
Figure 4.4: Impact of initial phase difference between multitone disturbances on probability of CSVCO EMI failure © [83].

It can be observed from Fig. 4.4 that the variation in the probability of EMI failures with respect to initial phase can depend significantly on the combinations of the frequencies used to generate the multitone disturbances, e.g., the variation of probability values (red circles) for the two-tone $\{750, 900\}$ MHz with respect to the mean failure value (red dashed line) is much higher when compared to the variations observed for the other two-tone combinations.

Sample output responses of the CSVCO and RO circuits with respect to an arbitrary two-tone disturbance $\{450, 800\}$ MHz are shown in Fig. 4.5.a and 4.5.b, respectively. Using the failure criteria given in (4.6), the probabilities of EMI failure of CSVCO and RO circuits upon injection of the two-tone disturbance are determined as 0.905 and 0.914, respectively.

4.3.4 Multitone Immunity Analysis

Based on the simulation results of the oscillators, the probability of EMI failures were estimated for all two-tone and three-tone combinations of the 15 single-tones disturbances. The failure probability values associated with some of those multitone



(a) (b)

Figure 4.5: Output frequency response of a) CSVCO and b) RO when injected with two-tone disturbance having frequencies $\{450, 800\}$ MHz © [83].

samples (for both oscillator topologies) can be found in Table 4.2 for two-tone cases and in Table 4.3 for three-tone cases (see entries in rows with respect to $\mathcal{P}(e|\ \mathbf{x})$). It can be seen from Tables 4.1–4.3 that the EMI failure probabilities for the multitone cases can be lower or higher than the single tone cases.

For example, the individual probability of CSVCO failures corresponding to disturbances 450 MHz and 800 MHz are 0.653 and 0.540, respectively (Fig. 4.2), whereas, when these two tones were superimposed more failures were observed, i.e., $\mathcal{P}(e|\ 450, 800) = 0.905$ (see Fig. 4.5.a). However, for the RO circuit, less failures were observed due to the same two-tone disturbance, i.e., $\mathcal{P}(e|\ 450, 800) = 0.914$ (see Fig. 4.5.b), when compared to one of the singletone disturbances, i.e., $\mathcal{P}(e|\ 450) = 0.956$ (see Fig. 4.3.a). Hence, for the above two-tone example, the superposition of two single-tone disturbances increased the likelihood for an EM failure (i.e., positive causality) for CSVCO, whereas, it resulted in a cancelling effect (i.e., inhibition) for the RO circuit. The observed enhancement and cancelling out of the multitone EM disturbance impact may be due to the inter-modulation products of the two single-tone frequencies.

Table 4.2: Probability of EMI failure due to two-tone disturbances obtained for CSVCO and RO circuits (simulations) © [83]

Two-tone (MHz)	50, 450,	50, 600,	50, 750,	50, 800,	50, 900,	450, 600,	450, 750,	450, 800,	450, 900,	600, 750,	600, 800,	600, 900,	750, 800,	750, 900,	800, 900,
CSVCO															
$\mathcal{P}_{\mathbf{X}}$	0.761	0.779	0.681	0.93	0.79	0.939	0.933	0.905	0.8	0.667	0.812	0.828	0.582	0.78	0.564
$\mathcal{N}_{\mathbf{X}}$	0.948	0.986	0.896	0.931	0.939	0.967	0.761	0.840	0.859	0.934	0.956	0.961	0.682	0.719	0.813
DoS (%)	-19.8	-20.9	-24.1	-0.1	-15.8	-2.9	**22.7**	**7.7**	-6.9	-28.5	-15	-13.9	-14.7	**8.4**	-30.6
Causality	I	I	I	A	I	A	S	S	A	I	I	I	I	S	I
RO															
$\mathcal{P}_{\mathbf{X}}$	0.843	0.895	0.926	0.912	0.850	0.854	0.859	0.914	0.822	0.727	0.611	0.759	0.603	0.528	0.332
$\mathcal{N}_{\mathbf{X}}$	0.990	1.0	0.907	0.820	0.795	1.0	0.980	0.961	0.956	1.0	1.0	1.0	0.646	0.598	0.225
DoS (%)	-14.8	-10.5	**2.1**	**11.3**	**6.9**	-14.6	-12.3	-5	-14	-27.3	-38.9	-24.1	-6.7	-11.8	**47.6**
Causality	I	I	S	S	S	I	I	I	I	I	I	I	A	I	S

Table 4.3: Probability of EMI failure due to three-tone disturbances obtained for CSVCO and RO circuits (simulations) © [83]

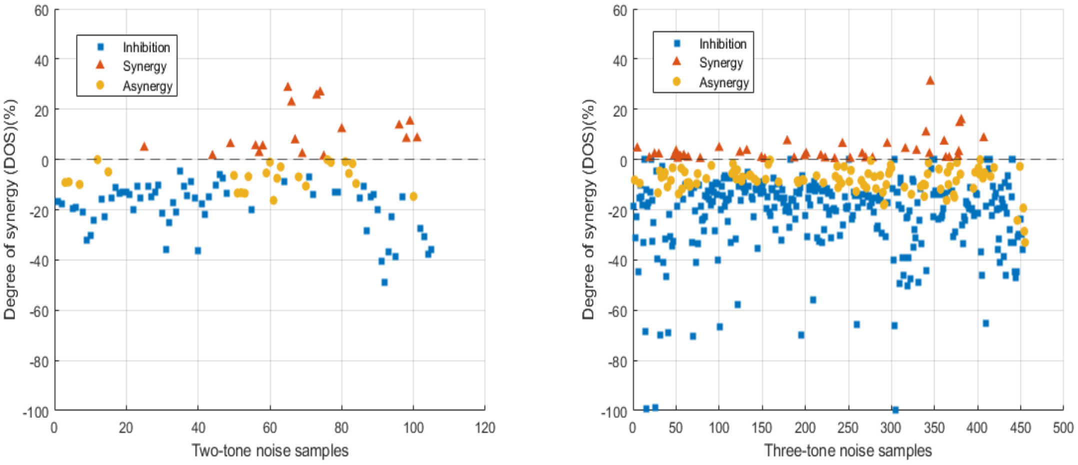
Three-tone (MHz)	50, 450, 600,	50, 450, 800,	50, 600, 750,	50, 600, 900,	50, 750, 900,	50, 800, 900,	450, 600, 750,	450, 600, 800,	450, 600, 900,	450, 750, 900,	450, 800, 900,	600, 750, 800,	600, 750, 900,	600, 800, 900,	750, 800, 900,
CSVCO															
$\mathcal{P}_{\mathbf{X}}$	0.691	0.522	0.996	0.809	1.000	0.667	0.744	0.846	0.863	1.000	0.798	0.572	0.785	0.630	0.622
$\mathcal{N}_{\mathbf{X}}$	0.995	0.976	0.990	0.994	0.958	0.972	0.977	0.985	0.987	0.903	0.935	0.970	0.973	0.982	0.871
DoS (%)	-30.5	-46.5	**0.6**	-18.6	**4.4**	-31.4	-23.9	-14.1	-12.5	**10.8**	-14.7	-41.0	-19.3	-35.8	-28.6
Causality	I	I	S	I	S	I	I	I	I	S	A	I	I	I	A
$\mathcal{R}_{\mathbf{X}}$	0.350	0.934	-1.360	-0.362	0.651	0.774	0.940	0.928	0.843	0.970	0.872	0.141	0.531	0.213	0.690
$\mathcal{A}_{\mathbf{X}}$	0.991	0.986	0.990	0.994	0.967	0.972	0.988	0.983	0.965	0.970	0.945	0.960	0.979	0.982	0.867
$\mathcal{I}_{\mathbf{X}}$	0.857	0.921	0.748	0.826	0.838	0.821	0.8949	0.934	0.920	0.970	0.849	0.821	0.841	0.787	0.779
RO															
$\mathcal{P}_{\mathbf{X}}$	1.0	1.0	0.936	0.864	1.0	1.0	0.909	0.952	0.955	1.0	0.91	0.714	0.705	0.726	0.474
$\mathcal{N}_{\mathbf{X}}$	1.0	0.992	1.0	1.0	0.912	0.831	1.0	1.0	1.0	0.981	0.964	1.0	1.0	1.0	0.668
DoS (%)	0	**0.8**	-6.4	-13.6	**9.6**	**20.4**	-9.1	-4.8	-4.5	**1.9**	-5.6	-28.6	-29.5	-27.4	-29
Causality	-	S	I	I	S	S	I	I	I	S	I	I	I	I	I
$\mathcal{R}_{\mathbf{X}}$	<-100	0.858	<-100	<-100	0.94	0.948	<-100	<-100	<-100	0.371	0.717	<-100	<-100	<-100	0.622
$\mathcal{A}_{\mathbf{X}}$	1.0	0.996	1.0	1.0	0.949	0.948	1.0	1.0	1.0	0.981	0.969	1.0	1.0	1.0	0.679
$\mathcal{I}_{\mathbf{X}}$	0.867	0.93	0.874	0.885	0.912	0.948	0.819	0.805	0.825	0.857	0.907	0.779	0.789	0.79	0.652

4.3.4.1 Identification of Causal Dependence

One of the main applications of the noisy-OR probabilistic model discussed in Section 4.2, is to identify the existence of causal dependence between multi-causal interactions. For multitone immunity analyses of the oscillator circuits, the noisy-OR model is used to estimate the two-tone (where, $\mathbf{X} = \{x_1, x_2\}$ MHz) and three-tone (where, $\mathbf{X} = \{x_1, x_2, x_3\}$ MHz) failure probabilities, $\mathcal{N}_{\mathbf{X}}$, using k single-tone failure probabilities obtained from the simulations i.e., $\mathcal{P}(e|\ x_k)$, where $x_k \in \mathbf{X}$. Samples of two-tone and three-tone EMI failure probability estimated using the the noisy-OR equation (4.2) are provided for both oscillators in Tables 4.2–4.3. Note that, the leak probability λ, was considered as zero (4.2) for all the noisy-OR estimates during multitone immunity analyses. For comparison of probabilities obtained from EMI simulations, i.e., $\mathcal{P}_{\mathbf{X}}$ and the noisy-OR estimates i.e., $\mathcal{N}_{\mathbf{X}}$ a metric *degree of synergy* (DoS) was used, which is given in percentage as:

$$DoS = 100\left[\frac{\mathcal{P}_{\mathbf{X}} - \mathcal{N}_{\mathbf{X}}}{\mathcal{N}_{\mathbf{X}}}\right] \tag{4.8}$$

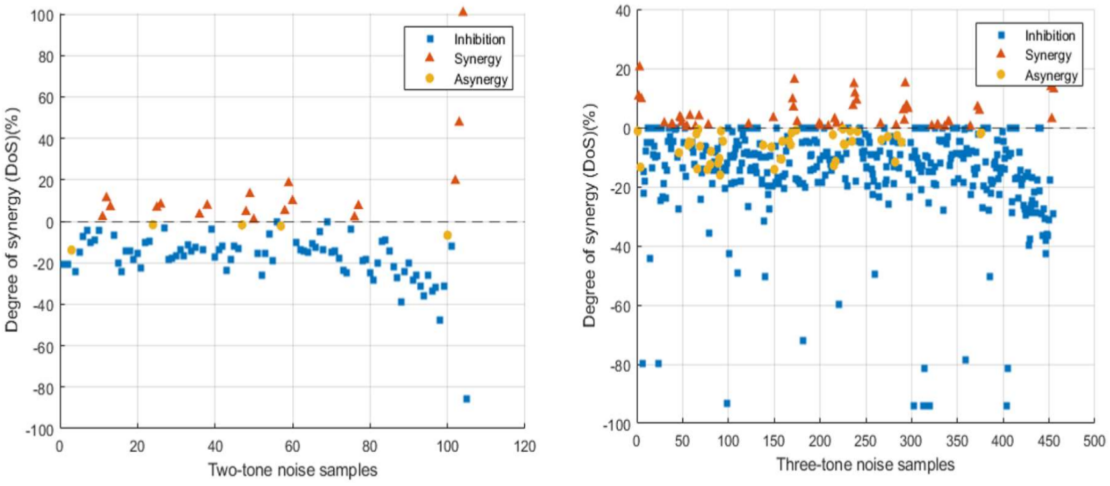
A non-zero DoS indicates the existence of causal dependence. More specifically, a negative DoS indicates either inhibition or asynergy, whereas, a positive DoS indicates synergy. For the two-tone example, $\mathbf{X} = \{450, 800\}$ MHz, as given in Table 4.2, the $DoS = 7.7\%$ for the CSVCO, indicating synergy and the $DoS =$ -5% for the RO, thus indicating inhibition or asynergy. Other examples of DoS estimated for two-tone and three-tone cases are provided in Tables 4.2–4.3, where the identified type of causality are marked as I, S and A, denoting inhibition, synergy and asynergy type interactions, respectively. The DoS corresponding to all the two-tone and three-tone combinations are shown in Fig. 4.6.a and 4.6.b, respectively for CSVCO, and Fig. 4.7.a and 4.7.b, respectively for the RO.



(a) (b)

Figure 4.6: Observed types of causal interactions due to (a) two-tone and (b) three-tone EM disturbances for the 3-stage CSVCO (BFD) © [83].

As noticed in Fig. 4.6–4.7, three types of multitone interactions exist for both



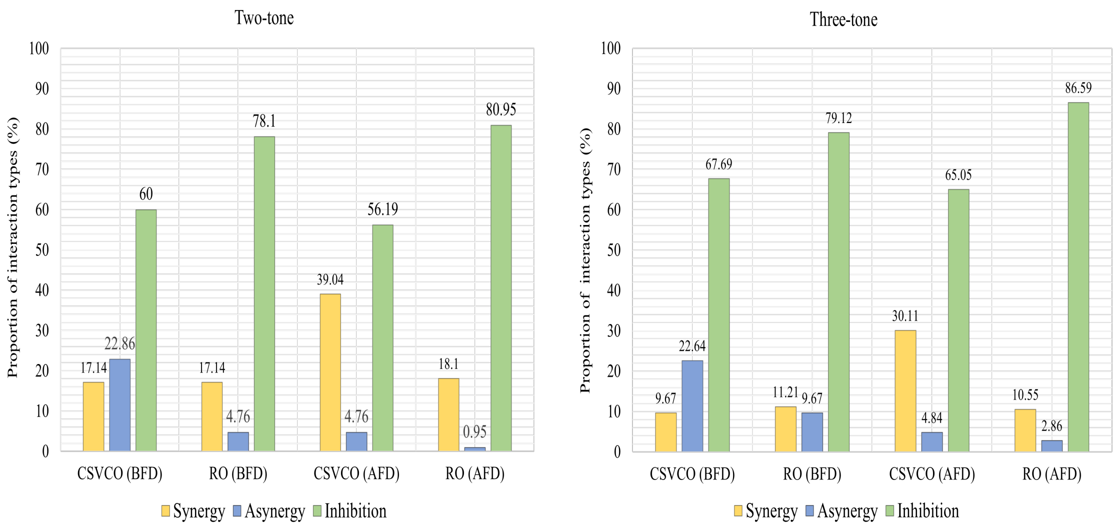
(a) (b)

Figure 4.7: Observed types of causal interactions due to (a) two-tone and (b) three-tone EM disturbances for the 3-stage RO (BFD) © [84].

the CSVCO and RO, despite having distinct architectures. However, since reduced probability of EMI failure is more desirable from an IC designer's perspective, the inhibition type multitone interactions are less of a concern when compared to positive causality. Similarly, within positive causality, although asynergy type multitone interactions increase the probability of failure when compared all the superimposed singletone disturbances, their impact is less than the predictions made by the noisy-OR model, which uses causal independence assumptions. Conversely, the synergy type interactions (highlighted bold in Tables 4.2–4.3) between simultaneous singletone disturbances leads to a higher probability of EMI failure than predicted by the noisy-OR model, thereby making the causal independence assumptions unreliable for multitone immunity predictions.

4.3.4.2 Comparison of Two-tone and Three-tone EMI

The proportion of interaction types associated to two-tone EMI for CSVCO and RO (BFD and AFD) are illustrated in Fig. 4.8.a. When comparing BFD, the inhibition interactions are higher by 18.1% for the RO than the CSVCO. Furthermore, by observing the positive causality, the RO has 18.1% lower asynergy interaction points than the CSVCO, but their synergistic proportions are the same. This observation shows that the probability of failure due to two-tone disturbances for the RO is lower



(a) (b)

Figure 4.8: Comparison of CSVCO & RO multitone EM disturbance effect © [85]: (a) two-tone; (b) three-tone.

than for the CSVCO. A similar comparison for AFD shows that the proportion of inhibition was reduced by 3.81% for the CSVCO and increased by 2.85% for the RO. The synergy interactions are increased by 21.9% and 0.95% for the CSVCO and RO, respectively, which means that the immunity levels of the CSVCO to two-tone disturbances were reduced with the addition of the FD. Nevertheless, for the RO, the immunity levels are observed to have slightly improved. In common, for both oscillators the proportion of asynergy reduces with the addition of a frequency divider. The differences in the proportion of interaction types between circuits demonstrate that the EMI performance of ICs can vary depending on their design and architecture.

While maintaining the same operating conditions, the steady-state response of both oscillators was also monitored for three-tone EM disturbances. As shown in Fig. 4.8.b, increasing the number of tones from two to three resulted in enhanced inhibition proportions for both oscillators. This change was due to the inter-modulation effects rising with more tones and eliminating the impact of each other. Thus, the probability of failure is reduced due to three-tone disturbances. Similar to the two-tone case, after the FD, the inhibition type interactions decreased by 2.64% for the CSVCO, whereas they increased by 7.47 % for the RO. It is deduced that the added effect of digital frequency dividers, analog output pad (i.e. pad capacitance and ESD structures) and package increases the synergistic proportion of interactions caused by the multi-tone disturbances for both oscillators.

Each of the synergy type interactions identified during the multi-tone analysis was further assessed by calculating the mean (DoS), which is defined in [83]. It can be seen in Fig. 4.9 that the mean DoS of the CSVCO is lower than the RO by 4.32% for two-tone disturbances (BFD). This is due to the architecture of the CSVCO, as the multi-tone RF signal initially disturbs the biasing transistors before eventually reaching the inverter stage. Thus, the CSVCO is resisting a change in frequency and causes the mean DoS to be decreased.

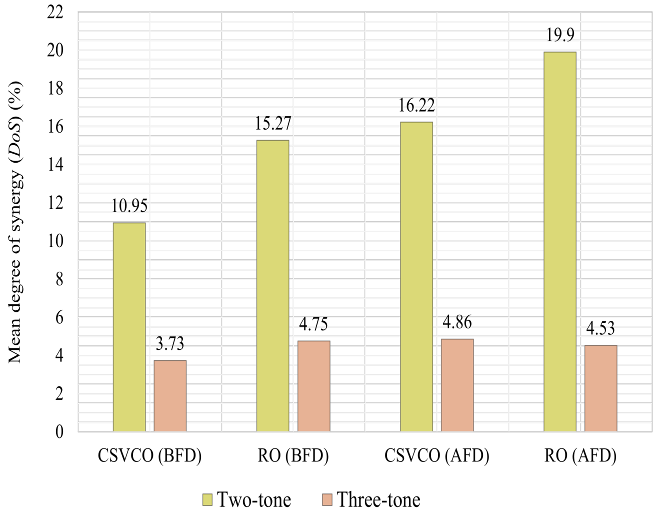


Figure 4.9: Mean DoS of two-tone and three-tone disturbances: CSVCO vs. RO © [85].

To summarize, by using frequency deviations as the failure criterion, the causal dependence between multi-tone disturbances was observed to vary the probability of EMI failures of integrated oscillators. The performance of the CSVCO could be regarded better than the RO due to the relatively lower mean DoS. However, the higher proportion of synergy type interactions for the CSVCO AFD cases suggests otherwise. By comparing the BFD and AFD results, it is clear that the FD, output pad and package have an impact on the perceived EM immunity levels of the oscillator circuits for this particular case study.

4.3.4.3 Higher Order Multi-Causal Interactions

The simulation setup in Fig. 4.1 was utilized to characterize the causal interactions of the RO (BFD) for up to 10 simultaneous tones with equal amplitudes, different frequencies and random phases. This was done in order to analyze if synergistic interactions exist for more than 3 injected tones. The pie charts in Fig. 4.10 show the change in the proportion of causal interactions as the number of injected tones rise. It was noticed that around 70% of all higher order multitone interactions result in inhibition. Further, the proportion of synergistic interactions decreased from 26.67% for 2-tone to 0% for 6-tone and higher order combinations. This trend asserts that use of the noisy-OR model in higher order multitone immunity analysis will overestimate the probability of failure. Fig. 4.10 does not include the *DoS* for 10-tones, since the latter only results in a single combination which was of type inhibition.

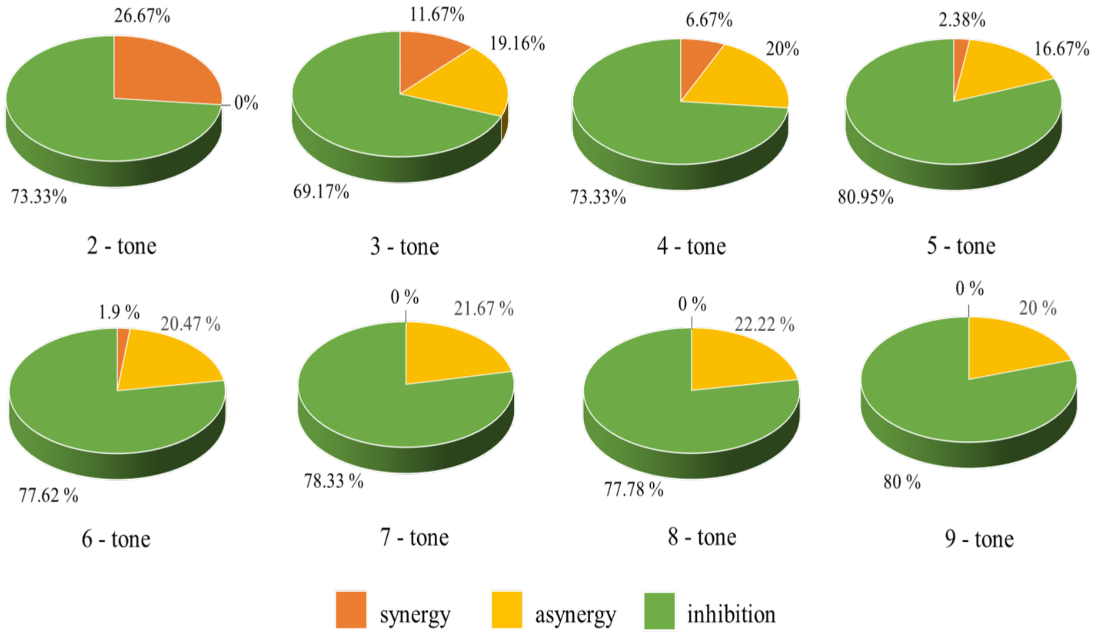


Figure 4.10: Variation in the proportion of multi-causal interaction types due to higher order multitones © [84].

The higher number of asynergy and inhibition interactions for higher order tones (greater than three) indicates that the noisy-OR model can be utilized for EMI risk reduction including a safety margin. However, this will lead to overestimation which can be regarded as a conservative approach. These results also illustrate that up to three tones were adequate to characterize multi-causal EM interactions for an IC.

4.3.5 Multitone Immunity Prediction

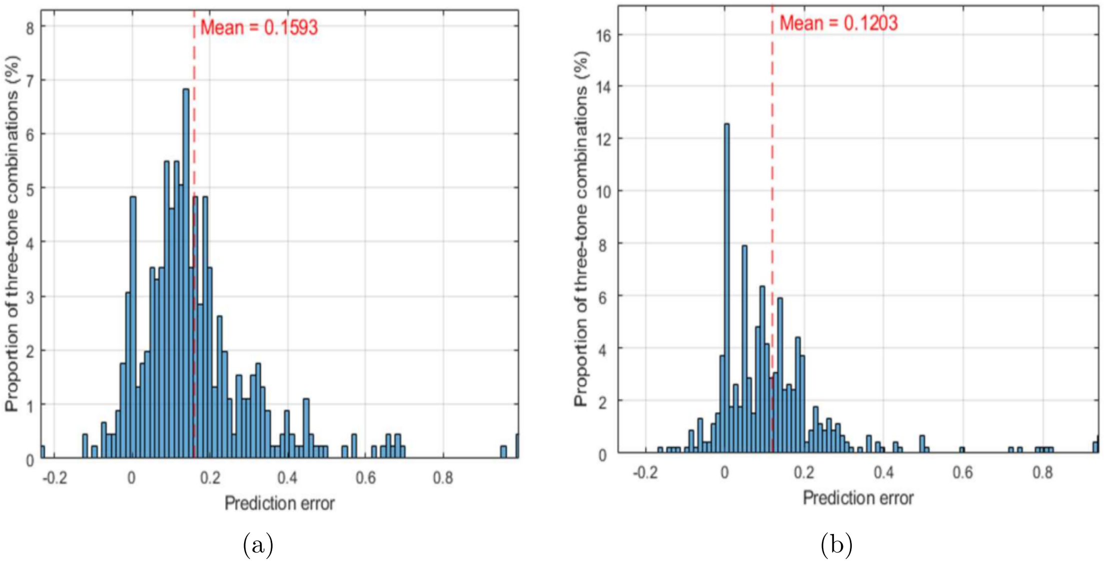
Two of the main limitations of multitone immunity analysis are the number of simultaneous tones that can be considered during measurements and the exponentially high number of possible multitone combinations for increasing samples of single-tone frequencies. It is possible to overcome both of those limitations if higher-order multitone effects are predictable. In this section, the probabilistic models discussed in Section 4.2 of this Chapter have been evaluated for their capability of predicting three-tone EMI failures using the assumption that the lower-order multitone combinations, i.e., single-tone and two-tone probabilities are available.

4.3.5.1 Evaluation of the Noisy-OR Model and its Derivatives

As discussed in the previous section, the causal independence assumptions between the simultaneous disturbances were already used in the noisy-OR model to predict the multitone EMI failure probability for the identification of causal dependence. Although, predictions using the noisy-OR model can significantly reduce the burden of an expert (exponential to linear) to collect data for EM immunity performance, the causal independence assumptions will undermine the effects of those multitone disturbances whose interactions are of type synergy. For example, the probability of CSVCO EMI failure predicted using the noisy-OR rule for two-tone combination $\mathbf{X} = \{450, 750\}$ MHz is $\mathcal{N}_{\mathbf{X}} = 0.761$. However, the probability obtained from simulations is much higher, i.e., $\mathcal{P}_{\mathbf{X}} = 0.933$ (Table 4.2). In addition, the noisy-OR estimates can also lead to overestimation of the effect caused by multitone EM disturbances. For examples, see in respective Tables 4.2 –4.3 for the overestimated probabilities of two-tone and three-tone combinations, which are marked with causality types I (inhibition) and A (asynergy).

Hence, for the evaluation of the noisy-OR model, the prediction errors (i.e., deviation from the mean value) made by the causal independence assumptions for all the three-tone combinations simulated are shown in the histograms of Fig. 4.11.a–4.11.b for the CSVCO and RO cases, respectively. The mean prediction error (μ) and the standard deviation (σ) for the three-tone samples using the noisy-OR model for the

CSVCO are $\mu_N = 0.1593$ and $\sigma_N = 0.1528$, respectively, and for the RO they are $\mu_N = 0.1203$ and $\sigma_N = 0.1576$.



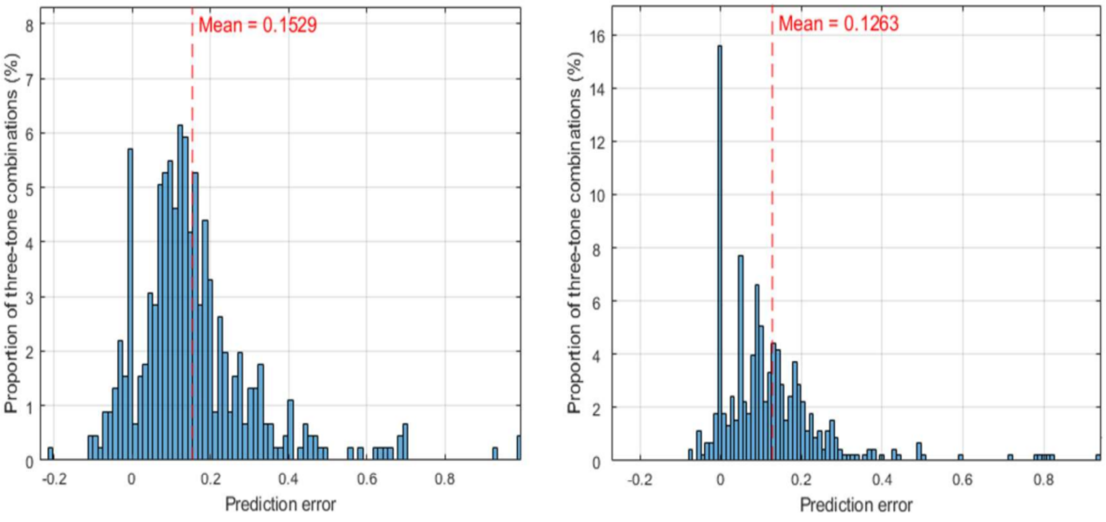
(a) (b)

Figure 4.11: Evaluation of noisy-OR rule for prediction of multi-causal effect © [83]; a) CSVCO: $\mu_N = 0.1593$ and $\sigma_N = 0.1528$, b) RO: $\mu_N = 0.1203$ and $\sigma_N = 0.1576$.

To improve the prediction accuracy of the noisy-OR model any available causal dependence information of type positive causality in addition to the causal independence assumptions of the noisy-OR can be used in the RNOR rule given in (4.3). For example, to predict the probability of RO failure due to the three-tone EMI combination, $\mathbf{X} = \{50, 750, 900\}$, where, $n = 3$, the causal dependence information of its lower-order combinations i.e., $r = \{n-1, n-2\}$ can be used in (4.3) as:

$$\begin{aligned}\mathcal{R}_{\{50,750,900\}} &= 1 - \left[\frac{(1-\mathcal{P}_{\{50,750\}})(1-\mathcal{P}_{\{750,900\}})(1-\mathcal{P}_{\{900,50\}})}{(1-\mathcal{P}_{\{750\}})(1-\mathcal{P}_{\{900\}})(1-\mathcal{P}_{\{50\}})}\right] \\ &= 1 - \left[\frac{(1-0.926)(1-0.528)(1-0.850)}{(1-0.614)(1-0.062)(1-0.786)}\right] = 0.932 \quad (4.9)\end{aligned}$$

For the above example, where $n = 3$, the lower order combinations, $r = n - 2 = 1$ corresponds to single-tone EM disturbance. Hence, there is no causal dependence information. Nevertheless, the probabilities of two-tone combinations, $r = n-1 = 2$, of type positive causality were used in (4.9) to decrease the prediction error relative to the noisy-OR estimate (see Table 4.3, $\mathcal{P}_{\mathbf{X}} = 1.0$, $\mathcal{N}_{\mathbf{X}} = 0.912$ and $\mathcal{R}_{\mathbf{X}} = 0.932$).



(a) (b)

Figure 4.12: Evaluation of ARNOR rule for prediction of multi-causal effect © [84]; a) CSVCO: $\mu_A = 0.1529$ and $\sigma_A = 0.1552$, b) RO: $\mu_A = 0.1263$ and $\sigma_A = 0.1544$.

However, the RNOR predictions becomes invalid if the causal dependence information available (provided by an expert) included inhibition type interactions. See examples of the invalid RNOR estimates for three tone predictions for both CSVCO and RO circuits in Table 4.3. For both oscillators, the proportion of inhibition was observed to be much larger than the proportion of positive causality, thereby making the RNOR model very limited for multitone EM prediction. Moreover, the predictions made by RNOR model becomes unreliable for four-tone or higher, i.e., when $n > 3$ due to the asymmetry problem discussed in [84], even if causal dependence information available is of type positive causality.

For cases where the causal dependence information provided by the expert consists of both inhibition and positive causality, the ARNOR rule can be used instead of the RNOR rule, in which any inhibition type causal dependence information is simply replaced with the noisy-OR estimate (which is always of type positive causality), thus making use of only the positive causality information. Hence, whenever the RNOR rule may not be applicable, the ARNOR rule given in (4.5) was used to calculate the three-tone probability of EMI failures for both circuits. For example, the RNOR estimate of the CSVCO failure probability for the three-tone combination, $\mathbf{X} = \{50, 600, 750\}$ MHz is $\mathcal{R}_{\mathbf{X}} = -1.360$, which is due to the inhibition type interactions between all of its lower-order two-tone combinations. However, using

(4.5), the failure probabilities corresponding to those two-tone combinations are replaced with noisy-OR estimates to get a valid probability of $\mathcal{A}_{\mathbf{X}} = 0.990$. It shall be noted that whenever RNOR is applicable, $\mathcal{A}_{\mathbf{X}} = \mathcal{R}_{\mathbf{X}}$. Furthermore, due to the high proportion of inhibitions observed for the simulation case study, the prediction accuracy of the three-tone failures using the ARNOR rule is almost equal when compared to the noisy-OR estimates. The prediction errors when using the ARNOR rule for CSVCO and RO circuits are shown in Fig. 4.12.a & 4.12.b, respectively. The ARNOR mean prediction error and standard deviation corresponding to CSVCO are $\mu_A = 0.1529$, $\sigma_A = 0.1552$ and for the RO they are $\mu_A = 0.1263$, $\sigma_A = 0.1544$, respectively.

4.3.5.2 Proposed Improvements to ARNOR Model

To improve the prediction capability of the ARNOR model, which ignores any valuable causal dependence knowledge of type inhibition, a new model called improved-ARNOR (I-ARNOR) is proposed. In this model, the a correction factor is used to obtain a revised probability estimate. The correction factor is derived from the degree of synergy (4.8) and is calculated using:

$$W_{\mathbf{X}} = \frac{1}{C^n_{r=n-g}} \sum_{j=1}^{C^n_{r=n-g}} \frac{\mathcal{P}_{\mathbf{X}\setminus\{C^n_g\}_j} - \tilde{P}_{\mathbf{X}\setminus\{C^n_g\}_j}}{\tilde{P}_{\mathbf{X}\setminus\{C^n_g\}_j}}. \tag{4.10}$$

In the above expression, $\tilde{P}_{\mathbf{X}\setminus\{C^n_g\}_j}$ depends on the type of causal dependence information available; for the type positive causality, $\tilde{P}_{\mathbf{X}\setminus\{C^n_g\}_j} = \mathcal{P}_{\mathbf{X}\setminus\{C^n_g\}_j}$, and for inhibition type interactions $\tilde{P}_{\mathbf{X}\setminus\{C^n_g\}_j} = \mathcal{N}_{\mathbf{X}\setminus\{C^n_g\}_j}$.

In (4.10), the upper-limit of the summation, $C^n_{r=n-g}$ corresponds to the number of all non-repeating combinations of $n-g$ simultaneous causes in $\mathbf{X}$ and for every j^{th} term of the sum '$\{C^n_g\}_j$' corresponds to the set subtraction of a non-repeating combination of g cause(s) from $\mathbf{X}$. The value of g (which is a positive integer) is based on the highest $(n-g)^{th}$ order causal dependence information (which can be in range $[2, n-1]$) available. For example, if $\psi\{\mathbf{X}\} = 4$ and the highest order of causal dependence information available is 3, i.e., $n-g=3$, then $g=1$. Including the correction factor, $W_{\mathbf{X}}$ the I-ARNOR expression is given as:

$$\mathcal{I}_{\mathbf{X}} = \mathcal{A}_{\mathbf{X}}(1 + W_{\mathbf{X}}) \tag{4.11}$$

where $\mathcal{I}_{\mathbf{X}}$ denotes the probability estimated using the I-ARNOR function. Note that for positive causality the summation always reduces to zero, thereby including only the inhibition information, which the RNOR and ARNOR models omit during multi-causal prediction. As an example, consider the prediction of RO failure probability for the three-tone EM combination $\mathbf{X} = \{50, 600, 900\}$ MHz ($n = 3$) with the assumption that all the lower-order combinations of two-tone EM failure probabilities are available, then using (4.5) in (4.10):

$$\begin{aligned}\mathcal{I}_{\mathbf{X}} = \left(1 - \left[\frac{(1-\mathcal{N}_{\{50,\,600\}})(1-\mathcal{N}_{\{600,\,900\}})(1-\mathcal{P}_{\{900,\,50\}})}{(1-\mathcal{P}_{\{600\}})(1-\mathcal{P}_{\{900\}})(1-\mathcal{P}_{\{50\}})}\right]\right)(1+W_{\mathbf{X}}) \\ = \left(1 - \left[\frac{(1-1.0)(1-1.0)(1-0.85)}{(1-1.0)(1-0.062)(1-0.786)}\right]\right)(1+W_{\mathbf{X}}) \\ = (1.0)(1+W_{\mathbf{X}})\end{aligned} \tag{4.12}$$

The values of all the two-tone and single-tone probability entries in (4.12) are available from Tables 4.1–4.2. Further, to calculate the correction factor in (4.12) for the three-tone combination ($n = 3$), the highest order causal dependence information known is $n - g = 2$, which gives the value of $g = 1$ and $r = 2$. Then, using (4.10) the correction factor is calculated as:

$$\begin{aligned}W_{\mathbf{X}} &= \frac{1}{C^3_2}\left[\frac{\mathcal{P}_{\mathbf{X}\backslash\{C^3_1\}_1} - \tilde{P}_{\mathbf{X}\backslash\{C^3_1\}_1}}{\tilde{P}_{\mathbf{X}\backslash\{C^3_1\}_1}} + \frac{\mathcal{P}_{\mathbf{X}\backslash\{C^3_1\}_2} - \tilde{P}_{\mathbf{X}\backslash\{C^3_1\}_2}}{\tilde{P}_{\mathbf{X}\backslash\{C^3_1\}_2}} + \right. \\ &\qquad \left. \frac{\mathcal{P}_{\mathbf{X}\backslash\{C^3_1\}_3} - \tilde{P}_{\mathbf{X}\backslash\{C^3_1\}_3}}{\tilde{P}_{\mathbf{X}\backslash\{C^3_1\}_3}}\right] \\ &= \frac{1}{3}\left[\frac{\mathcal{P}_{\mathbf{X}\backslash\{50\}} - \tilde{P}_{\mathbf{X}\backslash\{50\}}}{\tilde{P}_{\mathbf{X}\backslash\{50\}}} + \frac{\mathcal{P}_{\mathbf{X}\backslash\{600\}} - \tilde{P}_{\mathbf{X}\backslash\{600\}}}{\tilde{P}_{\mathbf{X}\backslash\{600\}}} + \frac{\mathcal{P}_{\mathbf{X}\backslash\{900\}} - \tilde{P}_{\mathbf{X}\backslash\{900\}}}{\tilde{P}_{\mathbf{X}\backslash\{900\}}}\right] \\ &= \frac{1}{3}\left[\frac{\mathcal{P}_{\{600,900\}} - \tilde{P}_{\{600,900\}}}{\tilde{P}_{\{600,900\}}} + \frac{\mathcal{P}_{\{50,900\}} - \tilde{P}_{\{50,900\}}}{\tilde{P}_{\{50,900\}}} + \frac{\mathcal{P}_{\{50,600\}} - \tilde{P}_{\{50,600\}}}{\tilde{P}_{\{50,600\}}}\right]\end{aligned} \tag{4.13}$$

The two-tone combinations {600, 900} MHz and {50, 600} MHz are of type inhibition. Thus, $\tilde{P}_{\{600,900\}}$ and $\tilde{P}_{\{50,600\}}$ terms are replaced with their corresponding noisy-OR estimates, $\mathcal{N}_{\mathbf{X}}$, whereas, the two-tone disturbance {600, 900} MHz is of type positive causality, so $\tilde{P}_{\{50,900\}} = P_{\{50,900\}}$. Substituting the above entries in

(4.13):

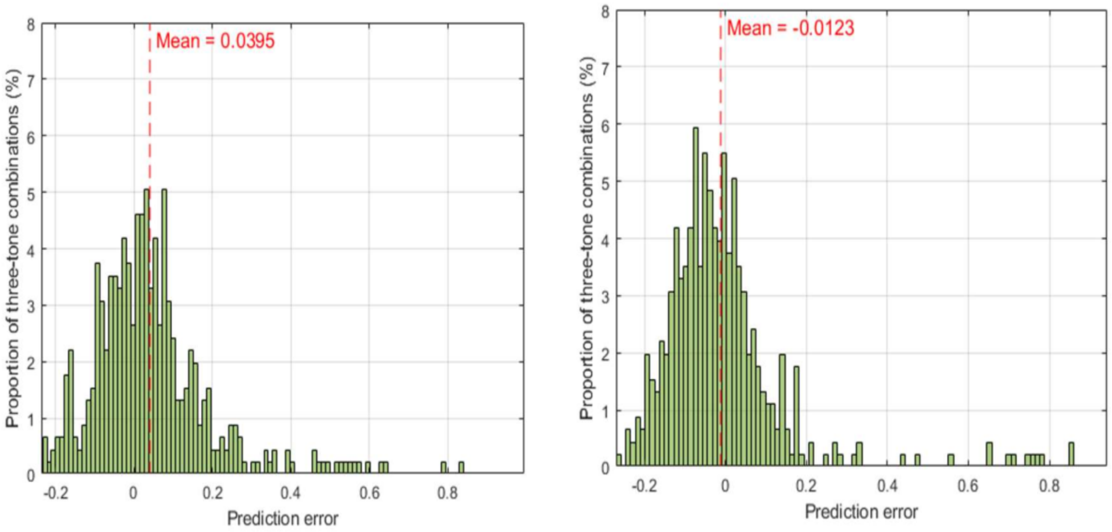
$$W_{\mathbf{X}} = \frac{1}{3}\left[\frac{\mathcal{P}_{\{600,900\}} - \mathcal{N}_{\{600,900\}}}{\mathcal{N}_{\{600,900\}}} + \frac{0}{\mathcal{P}_{\{50,900\}}} + \frac{\mathcal{P}_{\{50,600\}} - \mathcal{N}_{\{50,600\}}}{\mathcal{N}_{\{50,600\}}}\right]$$
$$= \frac{1}{3}\left[-0.241 + 0 - 0.105\right] = -0.1153 \quad (4.14)$$

Using the correction factor obtained from (4.14) in (4.12), the I-ARNOR estimate is finally obtained as:

$$\mathcal{I}_{\mathbf{X}} = (1.0)(1 - 0.1153) = 0.8846 \quad (4.15)$$

which when compared to the probability obtained from simulations i.e., $\mathcal{P}_{\mathbf{X}} = 0.864$, has a prediction error of just 0.02. On the other hand, the noisy-OR and ARNOR estimates of EMI failure probability obtained for the three-tone example are $\mathcal{N}_{\mathbf{X}} = \mathcal{I}_{\mathbf{X}} = 1.0$, which leads to a prediction error of 0.136. The I-ARNOR estimates for several other multitone combinations are provided in Table 4.3 for further comparison with probability estimated using noisy-OR and its existing derivatives. For an overall evaluation of the prediction accuracy the probability errors estimated for all the three-tone failure predictions using single and two-tone probability values for both CSVCO and RO circuits are given in Fig. 4.13. a & 4.13 .b, respectively. The mean I-ARNOR prediction error and standard deviation for all the three-tone samples obtained for the CSVCO are correspondingly $\mu_I = 0.0395$ and $\sigma_I = 0.1566$, for the RO, they are $\mu_I = -0.0123$ and $\sigma_I = 0.1595$, respectively.

Compared to the mean prediction errors for the same set of three-tone disturbances obtained for the noisy-OR and its derivative ARNOR, the predictions made by the newly proposed I-ARNOR model is several magnitudes more accurate. Especially, a lower mean prediction error was observed for the RO case than the CSVCO because of the relatively high proportion of inhibition type interactions between multitone EM disturbances causing failures in the RO circuit. Although, the standard deviations estimated for the I-ARNOR predictions for both the oscillators, are slightly greater than those obtained for the noisy-OR and ARNOR estimates, this represents a very small loss in precision compared to the marked improvement in terms of reduced bias in the mean value, thus delivering greater accuracy overall. Experimental validation of the prediction models discussed in this chapter for multitone immunity analysis of the oscillator circuits is implemented in the next



(a) (b)

Figure 4.13: Evaluation of I-ARNOR rule for prediction of multi-causal effect © [84]; a) CSVCO: $\mu_A = 0.1529$ and $\sigma_A = 0.1566$, b) RO: $\mu_A = 0.1263$ and $\sigma_A = 0.1595$.

section.

4.4 Case Study of Integrated Oscillators Under Thermal Stress (Measurements)

In order to better emulate a real world EM environment, multitone testing can be considered an integral approach to characterize the immunity of non-linear ICs and quantify the effects of inter-modulation. The IEC 61000-4-3 [93] standard describes the benefits and applications of multitone testing from the point of view of reducing the overall testing duration. From a practical perspective, the major economic limitation of multitone immunity analysis is the infinite number of possible single-tone combinations that could be tested [91]. Additionally, technical challenges such as the amplifier saturation and bandwidth of the vector signal generators, limit the number of simultaneous tones. Simulation tools complemented by predictive models such as the *noisy-OR* model [96] and its descendants have been discussed in the previous section to overcome some of these limitations.

Over the past years, researchers have focused on characterizing the effect of single-tone EMI on specific ICs and extracting their susceptibility profiles [109]–

[111]. In addition, some authors' work aim to improve the application of EM susceptibility testing methods and predict IC immunity through analytical modeling and numerical simulation [112], [113]. The significance of radiated and conducted multitone immunity testing in reducing the cost and testing time has been discussed in [5], [114]. Recent studies have also been carried out to examine the EM susceptibility of ICs excited by different interference waveforms [115]. In Section 4.3, simulation techniques and probabilistic models have been used to characterize the combined effect of multitone interactions for a test chip. To the best of the author's knowledge, the experimental characterization of multitone interactions at the IC level has not been investigated.

Integrated oscillators are a crucial part of mixed-signal ICs such as RF transceivers and are indeed prone to conducted EMI, which affects their performance characteristics [116]. Furthermore, faster transistor switching in the oscillator's inverter stages can significantly increase junction temperatures and degrade its functionality [117]. Stability against temperature variations and susceptibility to multitone EM disturbances need considerable attention to ensure the reliable operation of an integrated oscillator. The analysis of the EM immunity levels of a CSVCO and a RO, previously studied for multitone threats using simulations in Section 4.3, will be validated in this section. Further, the existence of the three different types of multitone causal interactions will be experimentally verified for different levels of thermal stress. Additionally, the application of probabilistic models such as the noisy-OR and its descendants RNOR, ARNOR and, I-ARNOR will be validated for the prediction of three-tone failure probability from the single and two-tone failure probability values at respective extreme temperatures.

4.4.1 Effect of Temperature on Integrated Oscillators

Temperature variations can increasingly degrade the performance of CMOS based circuits such as oscillators. It can affect the transconductance, mobility and the threshold voltage of the CMOS transistors in the oscillator inverter stage [118]. The device under test (DUT), (i.e., the oscillators integrated into the IC which is mounted on the DPI variant PCB) is placed in a climatic chamber (Weiss Technik WK180/40) with voltage biasing applied through high temperature cables (Amphenol-RF 095-902-466-004). While maintaining the nominal temperature for the DUT at 25 °C, the output frequency of each oscillator at the output pin (after the FD) was monitored through an oscilloscope with 1 MΩ input impedance. To see the dependence of the output frequency on temperature, the latter was increased from −40 °C to 120 °C with 5 °C step size and an accuracy of ±1 °C. Although the IC developed in SOI can withstand temperatures up to 175 °C compared to the conventional bulk CMOS technology, the mentioned range was selected as it complies with the temperature limit of all the components soldered on the PCB.

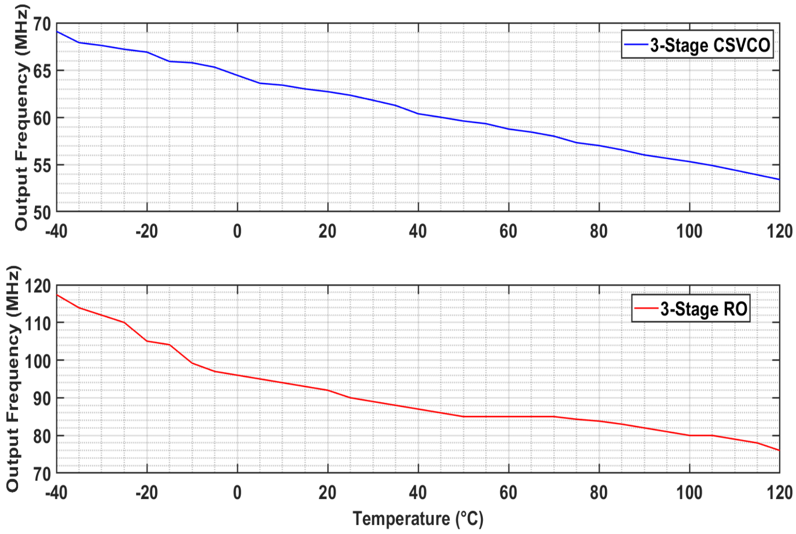


Figure 4.14: Measured frequency deviation as a function of temperature for the CSVCO and RO © [86].

The variation of the output frequency with temperature for the CSVCO and the RO are shown in Fig. 4.14. For both oscillators the output frequency is inversely proportional to temperature. The reason for this change in frequency is due to

Table 4.4: Measured output frequencies of the CSVCO & RO at nominal and extreme temperatures © [86].

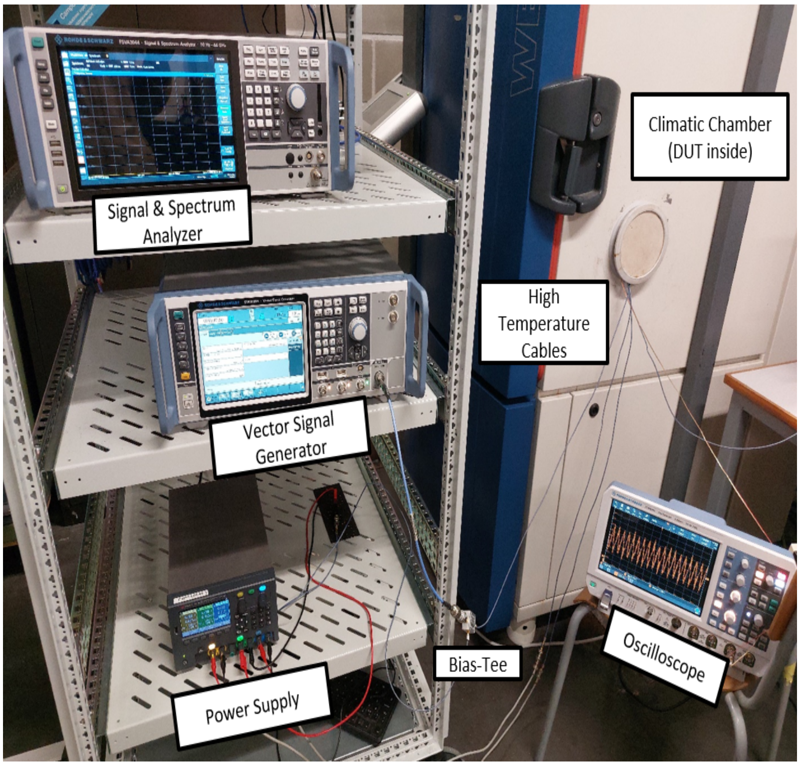
Type of Oscillator	Operating frequency	Output frequency (−40 °C)	Output frequency (25 °C)	Output frequency (120 °C)
CSVCO	703 MHz	68.3 MHz	62.5 MHz	53.8 MHz
RO	955 MHz	117.4 MHz	97.7 MHz	78.2 MHz

the reduction of the effective mobility and the drain currents of the MOSFETs in the inverter stage with rise in temperature [116]. The output frequencies for both oscillators (after the 3-stage FD) at the output pins were recorded at nominal and extreme temperatures as seen in Table 4.4. It was observed that the deviation of output frequency from the nominal frequency for the CSVCO and RO over the entire temperature range was ±11.68% & ±20.06%, respectively. Subsequently, it is deduced that the output frequency of CSVCO is more resilient to change in temperature compared to the RO. In the upcoming sections it will be explained how the multitone EM immunity of each oscillator can vary at severe temperatures.

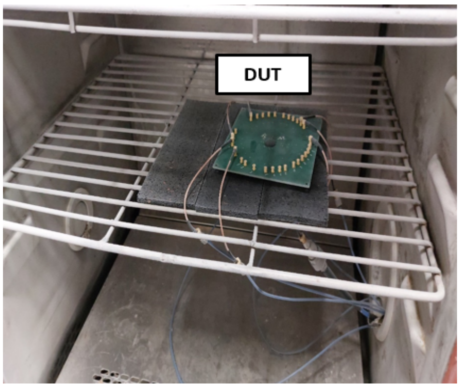
4.4.2 Multitone Experimental Setup

The multitone EM susceptibility experiment test bench includes a vector signal generator (R&S SMM100A), a signal & spectrum analyzer (R&S FSVA3044), a tracking DC regulated power supply (KEYSIGHT E36313A), a bias-tee (ZFBT-6GW+), an oscilloscope (R&S RTM3004), and a climatic chamber (Weiss Technik WK180/40). The setup is depicted in Fig. 4.15.a. The vector signal generator was set in the arbitrary function mode, and was able to generate high order multitone signals. The signal and spectrum analyzer was used to monitor the generated multitone signal in the frequency domain. The multitone disturbance was superimposed over the 5 V provided by one of the DC power supply channels via a bias-tee into the V_{DDI} pin of each oscillator. The remaining two channels of the power supply were connected to the V_{DD} and V_C pins of the DUT with a constant voltage of 5 V and 1.8 V, respectively. The V_{DD} is the global supply which powers the padring and the FD circuits in the IC. Both V_{DD} and V_C supplies were completely isolated from the injected EM disturbances. The DUT was placed inside the climatic chamber (Fig. 4.15.b) and the output pin of the tested oscillator was connected to the oscilloscope through 50 Ω high temperature cables.

One, two and three tone EM disturbances were injected into the DUT with an initial phase randomly selected between $-180°$ to $180°$. The output of each oscillator was monitored, for the input EM disturbances having the same random phase, at ambient and at extreme temperatures. The oscillators under study were susceptible to single-tone EM disturbances from 100 MHz to 1 GHz [106]. Within this range a total of 10 single-tone EMI frequencies were selected with a step size of 100 MHz. The number of frequencies selected for multitone analysis were restricted in order



(a)



(b)

Figure 4.15: Multitone experiment (a) test setup and (b) DUT inside climatic chamber © [86].

to limit the computational and test time. The maximum clock frequency of the vector signal generator is 44 GHz but the bandwidth for generating multitone EM disturbances, was limited to 600 MHz. Hence, to cover the entire bandwidth under test, two sets of multitone EM frequencies were chosen, which were $S_1 = [100\text{ MHz to } 600\text{ MHz}]$ & $S_2 = [500\text{ MHz to } 1\text{ GHz}]$. The total number of CPD entries required for n frequencies is 2^n. Furthermore, the total number of non-repeating combinations for multitones up to order r is given by $C(n, r)$.

A total of 29 two-tone and 40 three-tone cases were obtained from combinations of the 10 selected frequencies as shown in Table 4.5 (Section 4.4.8). All combinations of EM disturbances were applied to each oscillator independently at temperatures of −40 °C, 25 °C, and 120 °C. The injected power of each tone was kept constant at 10 dBm to limit the overall combinations of multi-tones. The selected power was the minimum level at which both oscillators exhibited an observable change in the frequency of the output signal.

4.4.3 Multitone Test Procedure

This section proposes a realistic and generic test procedure for the multitone EM susceptibility analysis. The flowchart is presented in Fig. 4.16. Prior to initiating the multitone test, it has to be checked that the DUT is operating under nominal conditions and generating a stable output signal. The procedure steps are the following:

1. Choose the number of single-tone EM frequency samples within the susceptibility range of the DUT and assign a power step in dBm.
2. Select the injected power assigned to each single-tone EM disturbance sample.
3. Select the number of multitone EM disturbances (e.g. 2 / 3 / 4 etc.) to be applied to the DUT.
4. Generate the mutlitone EM disturbance combinations according to $C(n, r)$.
5. Select the dwell time in which the output signal stabilizes and then inject the multitone EM disturbance into the specific supply or I/O pin.
6. Monitor & record the specific parameters of the output signal (i.e. frequency, DC offset, peak-to-peak voltage etc.) and compare it with the relevant failure criterion.
7. Increase the number of combinations of multitone EM disturbances. If all combinations are assessed, then go to the next step.
8. Increment the power level of all the single-tone EM disturbances. Restart the process until the maximum power is reached.

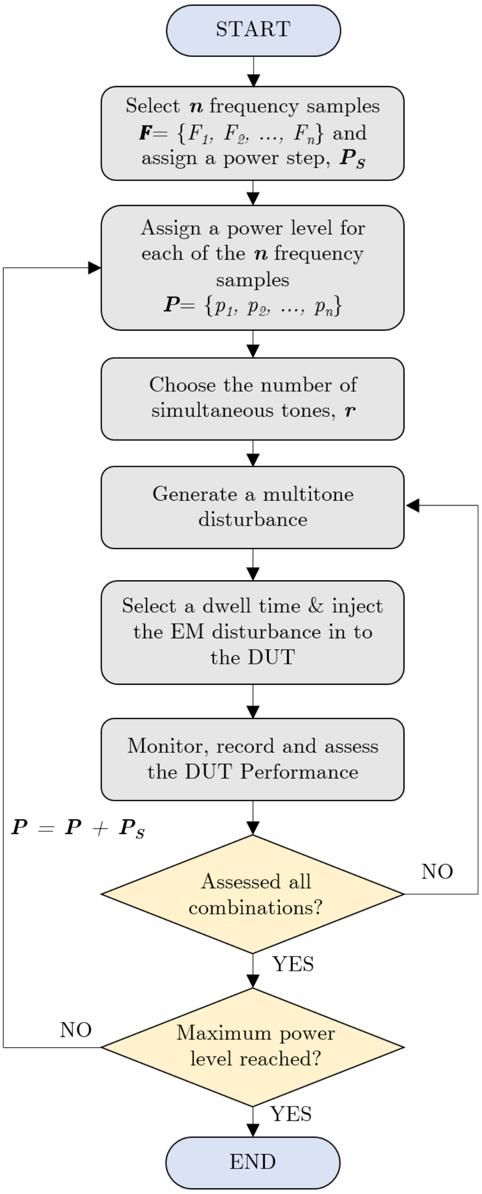


Figure 4.16: Flowchart of the single-tone (r = 1) and multitone (r > 1) immunity test procedure © [86].

9. At maximum power limit, save all input frequencies and output signal parameters & finish the test.

Although, the proposed flowchart was not utilized for multitone testing in this study, it can be included in the conventional DPI testing to more precisely characterize the conducted EM immunity of an IC.

4.4.4 Application of Failure Criterion

The operating frequency of an oscillator is conventionally used to evaluate its performance with respect to the injection of single-tone EM disturbances. However, stability parameters such as the peak-to-peak voltage and the mean DC offset could also be used to characterize the conducted immunity of oscillators [119]. To determine the performance of each circuit, the frequency observed at the output pin was monitored while being subjected to single and multitone EM disturbances under the influence of thermal stress. The failure criterion is the relative frequency deviation of ±5% from the nominal output frequencies of the CSVCO & RO, at nominal and extreme temperatures (Table 4.4). The tolerance limit is similar to industrial standards, which helps in characterizing the immunity of a VCO due to fluctuations in the supply voltage [120].

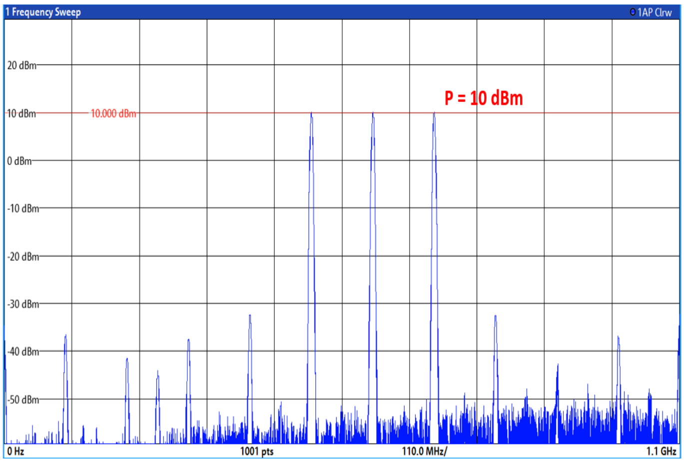
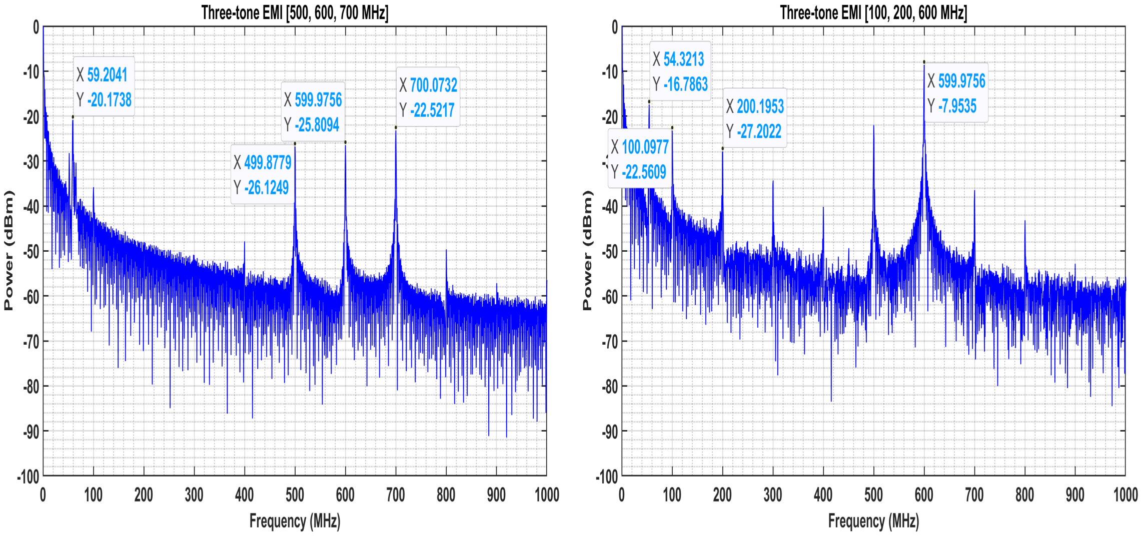


Figure 4.17: Three-tone input spectrum with injected power of 10 dBm at frequency [500, 600, 700 MHz] © [86].

All the EMI measurements were recorded for a time-period of 6 μs. A dwell time of 30 s was selected as the duration between two consecutive injected EM disturbances. That makes it possible for the tested oscillator to stabilize and reach its nominal operating frequency. The FFT was applied to measure the output frequency of the oscillators at discrete time steps (window size of 40 ns) over the steady-state period (6 μs). To illustrate how multitone EM disturbance can vary the output frequency of the CSVCO & RO, different cases were considered. For example, Fig. 4.17 displays the input frequency spectrum of the three-tone EM disturbance at 500 MHz, 600 MHz, and 700 MHz injected into the V$_{DDI}$ pin of the DUT. The vector signal generator was connected to the signal and spectrum analyzer to observe this specific waveform. It was verified that the injected power level of each tone was constant at 10 dBm by taking into account the 1.5 dB attenuation caused by the high temperature cables. Other peaks, due to intermodulation within the generator, were also observed in the input spectrum but were considered negligible since their power levels were less than −30 dBm.



(a) (b)

Figure 4.18: Measured output frequency of the CSVCO at 25 °C due to three-tone EM disturbance © [86]: (a) [500, 600, 700 MHz]; (b) [100, 200, 600 MHz]

Fig. 4.18.a shows the measured output response in the frequency domain of the CSVCO at 25 °C. It corresponds to the same input frequency spectrum as observed in Fig. 4.17. It is clearly seen that the highest frequency peak was shifted to 59.2 MHz from the nominal frequency of the CSVCO which is 62.5 MHz. The injected three-tone EM disturbances were observed at 500 MHz, 600 MHz, and 700 MHz but with power levels lower than that of the nominal frequency of 59.2 MHz. To apply the failure criterion, the frequency with the highest individual power was considered as the true shift in frequency for all tests. In this case, the CSVCO does not fail as the output frequency is still within the tolerance limit of ±5%. Moreover, other inter-modulating frequencies were also observed in the output spectrum but with negligible power levels.

Another example displays the output spectrum of the CSVCO with a three-tone EM disturbance of 100 MHz, 200 MHz and 600 MHz (Fig. 4.18.b). In this case, the nominal frequency was shifted to 54.32 MHz and was outside the tolerance limit of ±5%, thus, resulting in the CSVCO failure due to EMI. However, it was noted that the power level of 600 MHz is higher than that of 54.32 MHz by 8.83 dB. Hence, the output frequency is being locked to one of the frequencies of the injected multitone EM disturbance making the CSVCO very susceptible. Although in both cases the circuit is failing, the latter case shows the true shift in frequency from which the probability of failure can be acquired. Interestingly, it is observed that inter-modulating frequency of 500 MHz has a higher power than the remaining two (100 MHz & 200 MHz) injected EM disturbances. This is due to the injected EM disturbances being out of phase and cancelling each other.

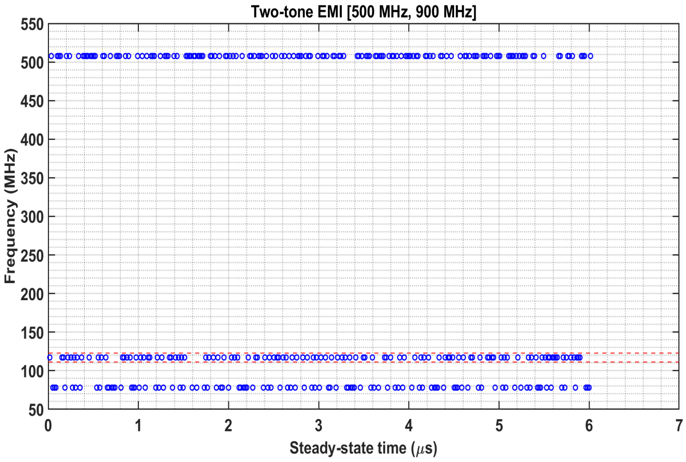


Figure 4.19: Steady-state output frequency of the RO at −40 °C, for two-tone EM disturbance [500, 900 MHz] (probability of failure = 0.6955) © [86].

The failure criterion is applied for each time-step in the steady state period, allowing the probability of EMI failure to be calculated by dividing the number of time steps with failure by the total number of time steps. For example, the failures due to two-tone EM disturbance at 500 MHz and 900 MHz are visualized in Fig. 4.19 for the RO at −40 °C, where the dashed lines represent the ±5 % tolerance. In this case, the output frequency under EMI is found to be beyond the tolerance at several instances from the nominal frequency of 117.4 MHz. Hence, the probability of EMI failure using the measurement data, P_M is calculated as 0.6955.

4.4.5 Application of Multi-Causal Bayesian Network

The probabilistic BN model is applied to facilitate the probability estimation of an IC failure due to EMI, when being operated in its system environment at a given temperature. Moreover, it aids in predicting the probability of EMI failure due to untested combinations of multitone disturbances. The former can be achieved by combining the following probability values:

- $P(\mathbf{F})$: the probability of an *EM disturbance* ($\mathbf{F}$), occurring in the system environment. Where, $\mathbf{F}$ is a set consisting of n different single-tones, $\{F_1, F_2, ..., F_n\}$ that can occur in the system environment;
- $P(T)$: the probability of the *operating temperature* (T);
- $P(E|\,\mathbf{F}, T)$: the conditional probability of *EMI failure* (E) due to a given EM disturbance at a given operating temperature.

In the BN shown in Fig. 4.20, $\{\mathbf{F}, T, E\}$ are considered as node variables. Such that, T is assumed to have three possible states $\{t_1, t_2, t_3\}$ corresponding to operating temperatures {−40 °C, 25 °C, 120 °C}. For each node variable $F_i \in \mathbf{F}$ (where $i =$ 1 to n), two possible states $\{f_i, \bar{f_i}\}$ are assumed, that denote their occurrence, i.e., present or absent respectively. Similarly, the node variable E is also considered to have two-states $\{e, \bar{e}\}$ that correspond to failure and no failure, respectively.

The directed edges in the BN depict the causal influence, i.e., from temperature and the EM disturbances on the IC failure using the directed edges $T \rightarrow E$, and $F_i \rightarrow E$, for $F_i \in \mathbf{F}$. Hence, by using the chain rule [107], the factorization for the joint probability distribution of the variables in the BN, which is also the probability of IC failing due to EMI in its system environment, is given by:

$$P(E,\ \mathbf{F}, T) = P(E|\,\mathbf{F}, T) \times P(T) \times \prod_{F_i \in \mathbf{F}} P(F_i) \tag{4.16}$$

However, in order to answer all possible probability queries using (4.16), the BN needs to be complete. This is the case only if each node variable is assigned with a CPD table that consists of probability entries corresponding to each variable state conditioned on the Cartesian product of the states of its parent node variables (i.e., the nodes from which directed edges originate). Hence, the CPD table of the node variable E has to be filled with $3^1 \times 2^{10} = 3072$ conditional probability entries.

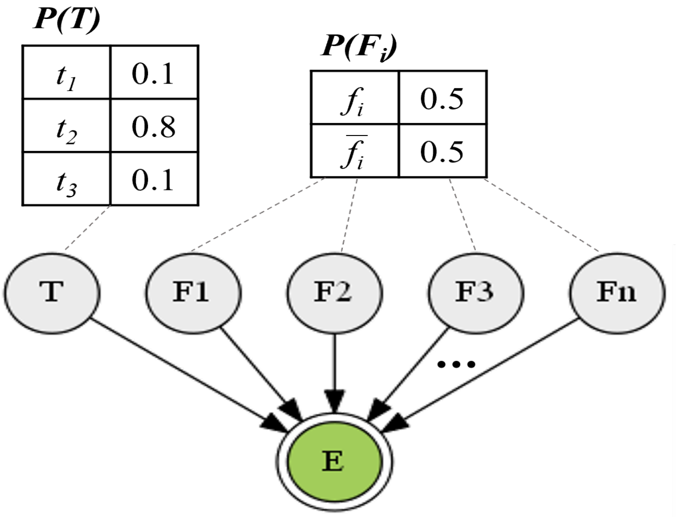


Figure 4.20: Bayesian network structure to map the influence of temperature and the causal effect of multitone EM disturbances on IC failure © [86].

However, the probability entries corresponding to just 79 combinations (10 single-tones, 29 two-tones and 40 three-tones) of the total 2^{10} multitone combinations are known for all three temperature states. The use of a deterministic CPD function for node E in the BN is denoted by a double-line notation in Fig. 4.20. Remaining node variables of the BN, i.e., T and $\mathbf{F}$ do not have any parents (i.e., the nodes having no incoming directed edges). Hence, the CPD table for each node reduces to a marginal probability distribution (MPD) as shown in Fig. 4.20.

It should be noted from the probability distribution of node T, that a higher probability value is assumed for the IC operating in the ambient temperature, when compared to the extreme temperatures. This is based on the assumption that the temperature of the target system environment is mostly ambient and rarely extreme. On the other hand, the MPDs of all node variables in set $\mathbf{F}$ are considered uniform, based on the assumption that the EM disturbances with frequencies corresponding to variables in $\mathbf{F}$ occurring in the target system environment are usually unknown. Nevertheless, the CPDs for T and F can be provided by collecting statistical data or by simply relying on expert knowledge of the system.

When a BN is used to map multiple causes of a single effect, the number of probability entries required to complete the CPD table increases exponentially with the number of parent nodes. The elicitation of such large number of conditional probability entries could become impracticable for many real-world applications, including the current investigation of estimating the IC failure probability due to multitone EM disturbances. To avoid the exhaustive elicitation of probability entries in the CPD table for E, deterministic functions for the conditional probabilities $P(E|\, T,\, \mathbf{F})$ can be used. The different deterministic CPD functions, namely the noisy-OR model, which is based on causal independence assumptions between multiple causes, and its descendants the ARNOR and the I-ARNOR, which inherit the noisy-OR model is applied again at various temperatures. Including the influence of T, the probability of an IC failure due to the multitone disturbance can be estimated using the noisy-OR CPD expression as:

$$P_N(e|\, \tilde{\mathbf{f}}, T) = 1 - \{(1-\lambda_0) \prod_{F_i = f_i \in \tilde{\mathbf{f}}} (1 - P_M(e|\, f_i, T))\} \tag{4.17}$$

where e is simply the evidence of failure, i.e., $E = e$, $\tilde{\mathbf{f}}$ indicates the assignment of a respective state for each of the n variables in set $\mathbf{F}$, e.g., if $n = 5$, then for a three-tone disturbance $\{F_1, F_2, F_4\}$, $\tilde{\mathbf{f}} = \{f_1, f_2, \bar{f}_3, f_4, \bar{f}_5\}$. As a shorthand, only the frequencies that are present (i.e., $F_i = f_i$) are included in $\tilde{\mathbf{f}}$. So, for the previous example, $\tilde{\mathbf{f}} = \{f_1, f_2, f_4\}$. In (4.17), $P_M(e|\, F_i, T)$ are the failure probabilities for single-tone EMI obtained from measurements and λ_0 represents the probability of failure in the absence of EMI (assumed to be zero).

Ideally, in the absence of EMI, i.e., when $\tilde{\mathbf{f}} = \emptyset$, the individual impact of temperature T on the IC failure due to EMI is considered to be constant with time. From Table 4.4, it can noted that at extreme temperatures ($T = t_1$ or t_3) the output frequencies are not within the the tolerable limits and vice versa for ambient temperature (t_2). Hence, $P(e|\, \tilde{\mathbf{f}}, t_1) = P(e|\, \tilde{\mathbf{f}}, t_3) = 1.0$ and $P(e|\, \tilde{\mathbf{f}}, t_2) = 0.0$.

As an example of using the noisy-OR CPD function, the probability of EMI failure of RO given $T = t_1$ (−40 °C) due to a two-tone disturbance, $\tilde{\mathbf{f}} = \{f_1, f_2\}$, where node variables $\{F_1, F_2\}$ correspond to frequencies $\{100, 200\}$ MHz respectively is calculated using (4.17) as:

$$\begin{aligned} P_N(e|\, \tilde{\mathbf{f}}, t_1) &= 1 - \{(1-0) \times (1 - P_M(e|\, f_1, t_1)) \times (1 - P_M(e|\, f_2, t_1))\} \\ &= 1 - \{1 \times (1 - 0.282) \times (1 - 0.951)\} = 0.965 \end{aligned} \tag{4.18}$$

Further, to calculate the probability of EMI failure due to two-tone disturbance, $\tilde{\mathbf{f}} = \{f_1, f_2\}$ in the system environment at a temperature, $T = t_1$, the result of noisy-OR

CPD function from (4.18) and the MPDs of $P(t_1)$, $P(f_i)$ and $P(\bar{f}_j)$ are used in (4.16) as:

$$\begin{aligned} P(E=e,\mathbf{F}=\tilde{\mathbf{f}},T=t_1) &= P_N(e|\,\tilde{\mathbf{f}},t_1)\times P(t_1)\times\prod_{f_i\in\tilde{\mathbf{f}}}P(f_i)\times\prod_{\bar{f}_j\in\tilde{\mathbf{f}}}P(\bar{f}_j) \\ &= 0.965\times 0.1\times 0.5^2\times 0.5^8 = 9.423\times 10^{-5} \end{aligned} \tag{4.19}$$

where $P(f_i)$, for $i=1,2$ and $P(\bar{f}_j)$, for $j=3$ to 10 are probability of the EM disturbances present and absent in the system environment, respectively. Since, the system environment is unknown, $P(f_i)=P(\bar{f}_j)=0.5$. Which in addition to the assumption of a low probability for extreme temperature $P(t_1)=0.1$, has reduced the probability of EMI causing failure in system environment significantly. Similarly, if the CPD value of $P(e|\,\tilde{\mathbf{f}},t_1)$ is taken from measurements, i.e., if $P_M(e|\,\tilde{\mathbf{f}},t_1)$ from Table 4.6, RO at -40 °C for {100, 400}MHz is used in (4.19), then $P(e,\tilde{\mathbf{f}},t_1)$ further reduces to 8.1112×10^{-5}. Several such probabilistic queries can be answered using the BN shown in Fig. 4.20.

Using the noisy-OR expression given in (4.17), the probability of IC failure due to two-tone and three-tone EM disturbances that were considered in measurements are calculated with independence assumptions. The probability values obtained using the measurement data, P_M, and the causal independence assumptions, P_N are provided in Tables 4.6 and 4.7 (Section 4.4.8), for some of the two-tone and three-tone examples, respectively. Based on the updated *DoS*, which is calculated by:

$$DoS = 100\left[\frac{P_M(e|\,\tilde{\mathbf{f}},T)-P_N(e|\,\tilde{\mathbf{f}},T)}{P_N(e|\,\mathbf{f},\tilde{T})}\right] \tag{4.20}$$

All the multitone disturbances are classified into the three types of causal interactions, namely: *synergy* ($DoS>0$) and *asynergy* or *inhibition* ($DoS<0$). Note that for some multitone combinations, e.g., for the two-tone frequencies (in MHz) $\{100,200\}$ (CSVCO at 120 °C), the *DoS* is greater than 100 (approximately, 9.99×10^5). This occurs mainly when either one or more of the single-tones in the multitone combination has no failures, but there is a probability of failure observed from the corresponding multi-tone measurement. For instance, using the previous example of two-tone combination $\{100,200\}$, $P_M(e|\,\tilde{\mathbf{f}}=\{100\})=P_M(e|\,\tilde{\mathbf{f}}=\{200\})=0.0001)$, whereas $(P_M(e|\,\tilde{\mathbf{f}}=\{100,200\})=1.0)$. Several other examples of

DoS greater and less than zero are given in Tables 4.6 and 4.7. A detailed discussion on the observed proportion of causal interaction types for two distinct oscillators at different temperatures is described in the upcoming section.

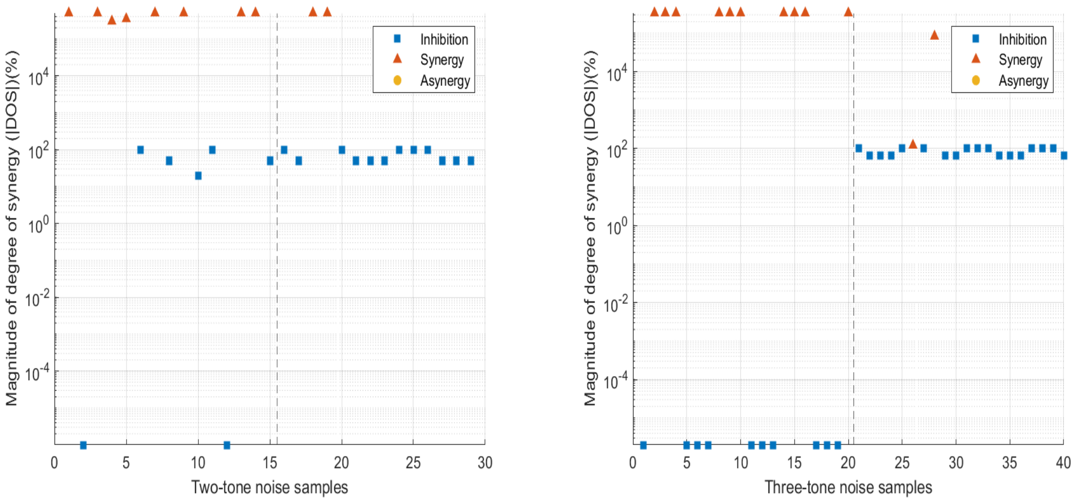
4.4.6 Multitone Immunity Analysis at Nominal Temperature

For injected single-tone EMI frequencies greater than 600 MHz at 10 dBm power level, there were fewer failures for both oscillators irrespective of the thermal stress. It is deduced that the combined effect of the CQFP package and the capacitance of the input pad results in filtering effects, hence, attenuating the power of higher injected frequencies. Furthermore, for all measurement results, no clamping by the ESD structures in the padring was observed at the output pin. The reason for that is the injected power level of 10 dBm for all single and multitone EM frequencies being insufficient to trigger the ESD structures.

Inhibition interactions are less of a concern to the multitone EM immunity of an IC due to the cancelling effect of inter-modulations. Conversely, interactions with positive causality, either synergy or asynergy, are significant as they increase the probability of EMI failure. From a risk perspective, interactions between multitone disturbances that are identified as synergistic or asynergistic should be assessed further, especially if multitone disturbance is likely in the intended system environment where the IC is functioning. The interaction types of 29 two-tone and 40 three-tone combinations are displayed for the CSVCO & RO at 25 °C, -40 °C, and 120 °C from Fig. 4.21 to Fig. 4.26. Relevant information that need to be considered before analyzing all multitone interaction plots (ambient and extreme temperatures) are as follows:

- For all inhibition interactions, the magnitude of *DoS* is less than or equal to 100.
- The y-axis is represented in logarithmic scale in order to highlight the extreme deviations in magnitude of *DoS* caused by synergistic interactions.
- The rise in the number of two and three-tone noise samples corresponds to the increase in the frequency of the EM disturbances.

- The dashed vertical line located in the middle of the plots represents the transition in multitone EMI frequencies from S_1 ([100 MHz - 600 MHz]) to S_2 ([500 MHz - 1 GHz]).



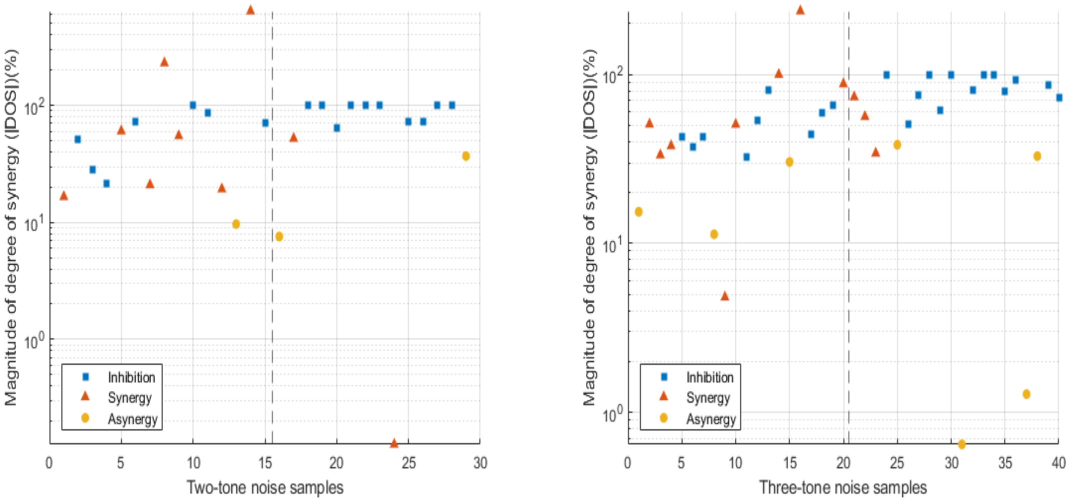
(a)

(b)

Figure 4.21: Observed causal interactions of CSVCO at ambient temperature © [86]: (a) two-tone; (b) three-tone.

To start with, the CSVCO subjected to two-tone EM disturbances at ambient temperature was analyzed (Fig. 4.21.a). It was noticed that most synergistic interactions occur within S_1 frequency set. The magnitude of DoS corresponding to these synergy points is substantially greater than 100, implying that the probability of EMI failure due to two-tone is much higher than the individual single-tone. Moreover, such a very high DoS means that the new output frequency is being locked to one of the sub-harmonics of the injected multitone EM disturbances.

Inhibition interactions are observed mostly for higher frequency combinations (S_2) with the magnitude of DoS close to 100. This indicates that the probability of EMI failure due to two-tone is marginally lower than single-tone. The behavior of causal interactions for three-tone EM disturbance (Fig. 4.21 .b) is essentially similar to two-tone except that the number of inhibition interactions have increased in both S_1 & S_2. Moreover, all inhibition noise samples in S_1 have their respective magnitude of DoS dropped to 0. This is the result of higher order tones causing a rise in inter-modulation effects, hence, eliminating the impact of each other. Consequently,



(a) (b)

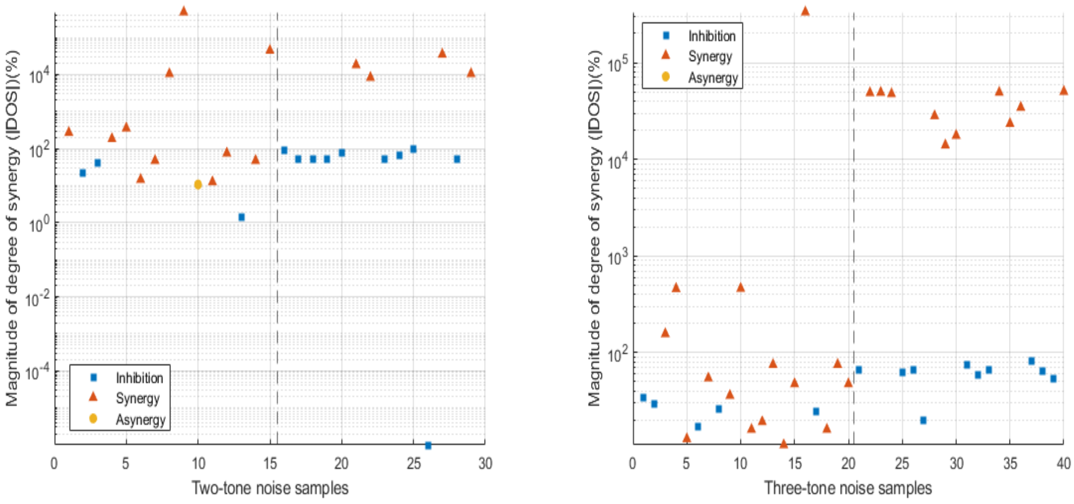
Figure 4.22: Observed causal interactions of RO at ambient temperature © [86]: (a) two-tone; (b) three-tone.

the probability of EMI failure due to higher order disturbances tends to be significantly lower than that of the individual single-tones. No asynergistic interactions were exhibited by the CSVCO at ambient temperature for two and three-tone EM disturbances, meaning that all positive causality interactions are causally dependent.

In contrast, the RO shows a distinct behavior to two and three-tone EM disturbances (Fig. 4.22 .a and 4.22.b). All possible multitone interactions (i.e synergy, asynergy & inhibition) were monitored over the entire frequency range (S_1 & S_2). The magnitude of *DoS* for all synergistic interactions is lower by the order of 10^2 when compared to the CSVCO. This conveys that the output frequency is not always locked to the injected two-tone EMI. In contrast to the CSVCO, all of the inhibition interactions for two and three-tone EM disturbances for the RO are close to 100. Further evaluation of multitone immunity for the RO at ambient temperature shows that, by increasing the number of tones from two to three, the proportion of asynergy type interactions tend to increase for both frequency sets S_1 and S_2. Thus, reducing the inhibition and synergy type interactions. This signifies that the probability of EMI failure rises with the increase in the number of simultaneous disturbances (due to increase in asynergistic proportion). However, approximation in such cases using the noisy-OR model serves as a conservative approach.

4.4.7 Multitone Immunity Analysis at Extreme Temperatures

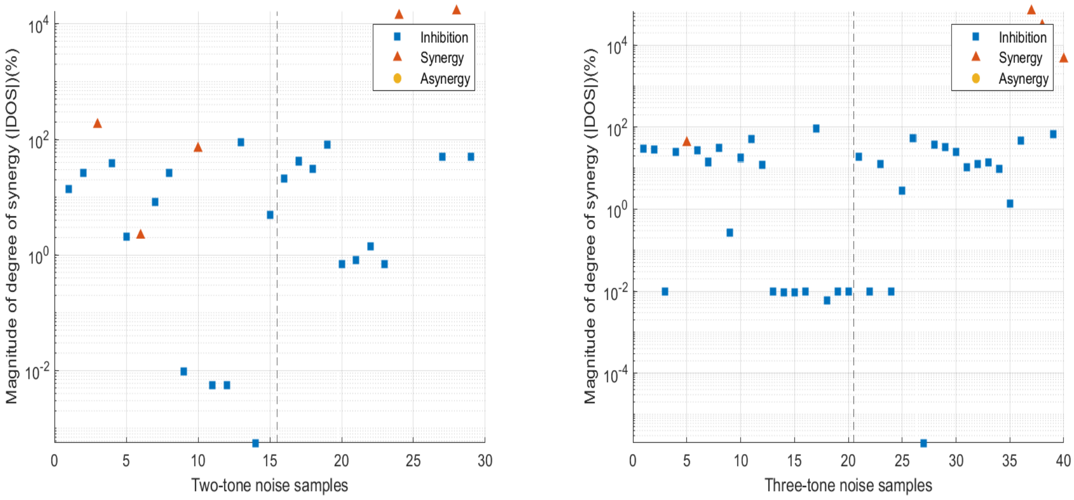
In Section 4.4.1, it was demonstrated that the output frequency of both oscillators was inversely proportional to the surge in temperature whereas the frequency of the CSVCO was more resilient to temperature changes compared to the RO. In this section, the multitone EM immunity of the CSVCO and RO is characterized including the effect of temperature variation.



(a) (b)

Figure 4.23: Observed causal interactions of CSVCO at −40 °C © [86]: (a) two-tone; (b) three-tone.

The interaction types associated to two and three-tone EMI for CSVCO at −40 °C are illustrated in Fig. 4.23.a and 4.23.b, respectively. At the minimum temperature, the overall synergistic interactions were increased and shifted to higher frequencies (S_1 to S_2), specifically for three-tone EM disturbances. However, the respective magnitude of DoS for synergy points at lower frequencies (S_1) is substantially reduced. The DoS for higher frequencies (S_2) has remained unaffected by temperature. Consequently, the inhibition interactions are reduced when increasing the order of tones from two to three with the DoS always being greater than 0. These results demonstrate that the CSVCO is truly susceptible to multi-tone EM disturbances at −40 °C. Only one asynergistic point was detected in S_1 for two-tone EMI, implying that the reduction in temperature does not primarily change the type



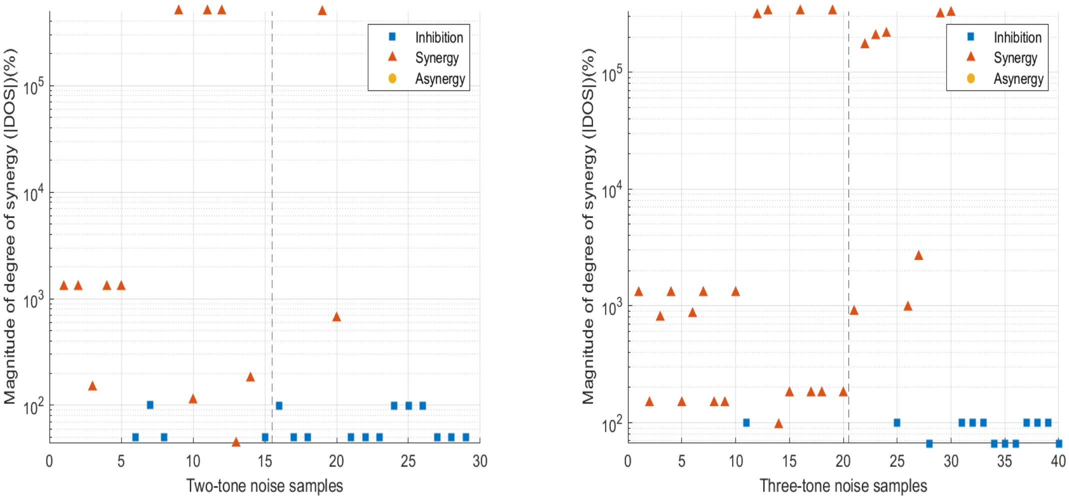
(a) (b)

Figure 4.24: Observed causal interactions of RO at −40 °C © [86]: (a) two-tone; (b) three-tone.

of positive causality for the CSVCO. When analyzing the effect of multitone EM disturbances on the RO at −40 °C (Fig. 4.24.a & 4.24.b), the inhibition interactions are relatively higher than previously noticed at ambient temperature. Synergistic interactions were less frequent and shifted to higher frequencies S_2. No asynergistic interactions were monitored for all multitone EMI corresponding to the RO at that temperature. In divergence to the CSVCO, the RO was found to be more immune to multitone EM disturbances at −40 °C. Moreover, the asynergistic interactions tend to diminish for the RO with the decrease in temperature. For both oscillators, a shift from low to high frequency for synergistic interactions was observed while lowering the temperature. Since both oscillators have different topology, the observed shift in frequency could be due to the effect of the package, the I/O pad capacitance, and the FD circuit at minimum temperature.

Fig. 4.25.a and 4.25.b represents the causal interactions of the CSVCO at maximum temperature. The number of synergistic interactions was significantly increased in S_1 with the rise in temperature. Although, the *DoS* for the synergy points has reduced and no shift in frequency is noticed for either two or three-tone EMI. With the increase in number of tones, inhibitions tend to decrease, meaning that inter-modulation effects result in positive causality. The RO also has more synergistic interactions at the elevated temperature due to two and three-tone EMI

as seen in Fig. 4.26.a and 4.26.b, respectively. Moreover, the magnitude of DoS of synergy points has lowered in S_1 with no visible shift in frequencies. Interestingly, most asynergistic interactions were shifted from S_2 to S_1. For higher EM multitone frequencies (S_2), nearly all interactions are inhibition with a constant DoS close to 100. It can be outlined that at maximum temperature the probability of failure due to multitone EMI increases for both oscillators, being more pronounced for the CSVCO. The RO was found to be more immune compared to the CSVCO at 120 °C.

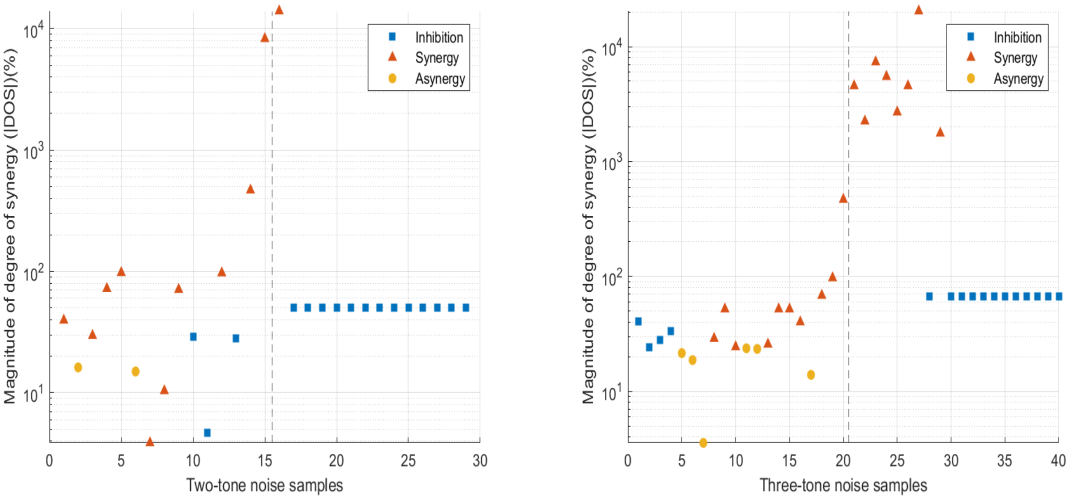


(a) (b)

Figure 4.25: Observed causal interactions of CSVCO at 120 °C © [86]: (a) two-tone; (b) three-tone.

4.4.8 Comparison of Causal Interactions with Temperature Variations

The proportions of causal interaction types for the CSVCO & RO as a result of two and three-tone EM disturbances (nominal and extreme temperatures) are compiled in Fig. 4.27.a and 4.27.b, respectively. For two-tone EMI at 25 °C, the inhibition interactions are 6% higher for the CSVCO in comparison to the RO. Furthermore, by observing the positive causality, the RO has 10% higher asynergy interaction points and 4% lower synergy interactions than the CSVCO. That observation shows that the probability of failure due to two-tone EM disturbance at ambient temperature for the RO is slightly lower than the CSVCO due to having a higher overall positive

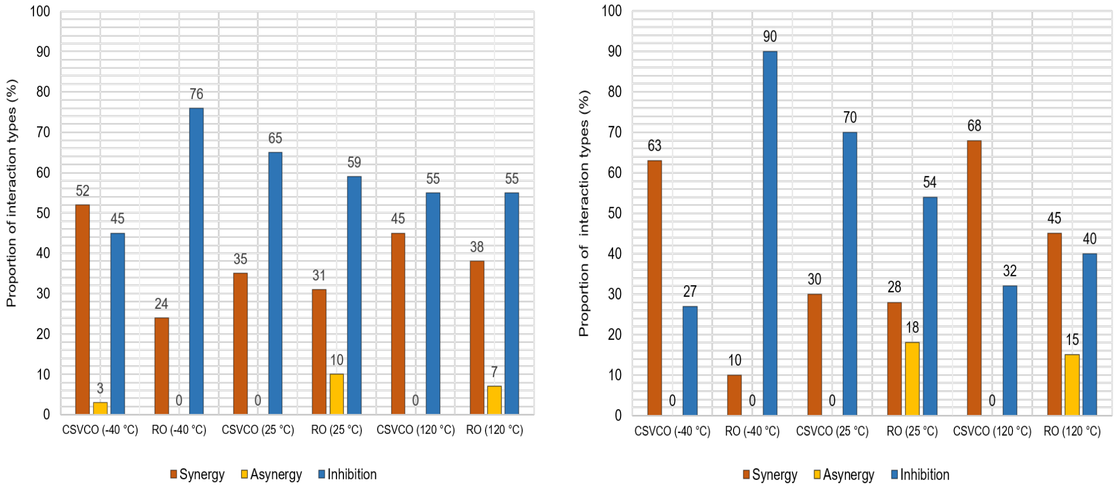


(a) (b)

Figure 4.26: Observed causal interactions of RO at 120 °C © [86]: (a) two-tone; (b) three-tone.

causality. When evaluating the temperature effect for two-tone EMI on both oscillators (Fig. 4.27.a), the multitone EM immunity of the CSVCO is drastically affected. At −40 °C, the inhibition proportions for the CSVCO were reduced by 20% , while raised by 11% for the RO when compared to ambient temperature. Additionally, at that temperature, the inhibition for the RO was 31% higher than the CSVCO. Unlike the CSVCO where the two-tone EM immunity was deteriorated, the RO had improved immunity at −40 °C.

Compared to ambient temperature, for two-tone EMI at 120 °C , the proportion of inhibition was reduced by 10% and 4% for the CSVCO and RO, respectively. When comparing both oscillators, the synergy interactions of the CSVCO were 7% higher than the RO, while their inhibition proportions were equivalent at the highest temperature. Consequently at 120 °C, the probability of failure of the CSVCO was found to be higher to two-tone EMI than the RO. For three-tone EMI at ambient temperature (Fig. 4.27.b) the proportion of inhibition interactions for the CSVCO was 16% higher than the RO. Additionally, the asynergical points were 18% lower for the CSVCO compared to the RO. At the nominal conditions, the probability of failure for multitone EM disturbance is lower for CSVCO than RO. This is due to the architecture of the CSVCO, as the multitone RF signal initially disturbs the biasing transistors before eventually reaching the inverter stage.



(a) (b)

Figure 4.27: Comparison of proportion of interaction types of the CSVCO and RO caused by multitone EM disturbance with the added effect of temperature © [86]: (a) two-tone; (b) three-tone.

Table 4.5: Probability of the EMI failure of CSVCO and RO due to single-tone disturbances (measurements) © [86].

Single-tone (MHz)	100	200	300	400	500	600	700	800	900	1000
CSVCO (−40 °C)	0.179	0.0	0.571	0.679	0.0	0.0	1.0	0.0	0.0	0.0
CSVCO (25 °C)	0.0	0.0	1.0	0.0	0.0	0.0	0.329	0.0	0.0	0.0
CSVCO (120 °C)	0.071	0.0	0.0	0.357	0.0	0.0	0.036	0.0	0.0	0.0
RO (−40 °C)	0.282	0.951	0.564	0.056	1.0	1.0	0.0	0.0	0.0	0.0
RO (25 °C)	0.33	0.011	0.606	0.063	0.017	0.059	0.042	0.031	0.092	0.095
RO (120 °C)	0.317	0.585	0.507	0.176	0.0	0.0	0.0	0.0	0.0	0.0

When increasing the tones from two to three, the inhibition interactions rise by 5% for the CSVCO whereas it drops by 5% for the RO. For the CSVCO the, intermodulation frequencies are cancelling each other out leading to inhibition, while they increase the positive causality for the RO. Similarly to two-tone, for three-tone EMI at extreme temperatures, the CSVCO is more prone to failure. In comparison to ambient temperature, at −40 °C, the synergistic proportions increase considerably by 33% for the CSVCO, while reducing by 18% for the RO. At that temperature, the

RO has significantly higher (63%) inhibition points than the CSVCO. Moreover, by raising the temperarure to 120 °C, for three-tone EMI, the synergistic interactions for the RO and CSVCO increase by 17% and 38%, respectively. Nevertheless, the synergistic points of the RO are 23% less than those of the CSVCO at maximum temperature. That clearly suggests that at extreme temperatures the RO is more resilient to multi-tone EMI compared to the CSVCO.

Table 4.6: Probability of the EMI failure of CSVCO and RO due to two-tone disturbances (measurements) © [86].

Two-tone (MHz)	100	100	100	200	200	300	400	500	500	600	600	700	800	900
	200	300	500	300	600	500	600	600	800	700	1000	800	900	1000
CSVCO (−40 °C)														
P_M	0.662	0.507	0.507	0.655	0.965	0.643	1	0.089	0	0.225	0	0.352	0.07	0.021
P_N	0.179	0.648	0.179	0.571	0	0.571	0.679	0	0	1	0	1	0	0
DOS (%)	>100	-21.7	>100	14.6	>100	12.6	47.3	>100	-50	-77.5	-50	-64.8	>100	>100
Causality	S	I	S	S	S	S	S	S	I	I	I	I	S	S
CSVCO (25 °C)														
P_M	1	1	0.6	0	1	0	1	0	0	0	0	0	0	0
P_N	0	1	0	1	0	1	0	0	0	0.329	0	0.329	0	0
DOS (%)	>100	0	>100	-100	>100	-100	>100	-50	-50	-100	-50	-99.97	-49.997	-49.997
Causality	S	I	S	I	S	I	S	I	I	I	I	I	I	I
CSVCO (120 °C)														
P_M	1	1	1	0	1	1	1	0	0	0.271	0	0	0	0
P_N	0.072	0.072	0.072	0	0	0	0.357	0	0	0.036	0	0.036	0	0
DOS (%)	>100	>100	>100	-50	>100	>100	>100	-50	-50	>100	-50	-99.7	-50	-50
Causality	S	S	S	I	S	S	S	I	I	S	I	I	I	I
RO (−40 °C)														
P_M	0.831	0.508	0.617	1	1	1	1	0.951	0.567	0.993	0.993	0.028	0	0
P_N	0.965	0.687	1	0.979	1	1	1	1	1	1	1	0	0	0
DOS (%)	-13.9	-26	-38.3	2.2	0	0	0	-4.9	-43.3	-0.7	-0.7	>100	-50	-50
Causality	I	I	I	S	I	I	I	I	I	I	I	S	I	I
RO (25 °C)														
P_M	0.393	0.357	0.268	0.162	0.107	0.085	0.875	0.021	0.071	0.036	0	0.071	0	0.113
P_N	0.337	0.736	0.341	0.61	0.069	0.612	0.118	0.074	0.047	0.098	0.148	0.071	0.12	0.178
DOS (%)	16.5	-51.5	-21.4	-73.4	54.9	-86.2	>100	-71.6	52.1	-63.6	-99.9	0.1	-99.9	-36.8
Causality	S	I	I	I	S	I	S	I	S	I	I	S	I	A
RO (120 °C)														
P_M	1	0.556	0.546	0.676	1	0.483	1	0.017	0	0	0	0	0	0
P_N	0.716	0.663	0.317	0.795	0.585	0.507	0.176	0	0	0	0	0	0	0
DOS (%)	39.6	-16.2	72.2	-15	71.1	-4.7	>100	>100	-50	-50	-50	-50	-50	-50
Causality	S	A	S	A	S	I	S	S	I	I	I	I	I	I

To summarize, the multitone EM immunity of a CSVCO and RO was experimentally compared and analyzed. The differences in the proportion of interaction types between both oscillators demonstrate that the EMI performance can vary depending on their design and architecture. At nominal temperature the CSVCO was found to be less susceptible to two and three-tone EMI than the RO. With the rise in the order of tones, the inter-modulation effects cause an increase in the proportion of inhibition interactions for the CSVCO while raising the positive causality for the RO. At extreme temperatures, the probability of failure for the RO due to multi-tone EMI is lower than the CSVCO. This means that even though the output frequency of the CSVCO was more resilient to temperature changes compared to the RO (analyzed in Section 4.4.1), it is still more susceptible to multitone EM disturbances under thermal stress.

All possible frequency combinations, the associated probability of failures, the *DoS*, and the interaction proportions (i.e. synergy (S), asynergy (A), and inhibition (I)) of the CSVCO & RO at −40 °C, 25 °C, and 120 °C are included in Tables 4.5, 4.6, & 4.7 for single-tone, two-tone and three-tone EM disturbances, respectively.

4.4.9 Evaluation of Multitone Immunity Prediction Models

The deterministic CPD functions discussed in Section 4.2 to predict the probability of multitone disturbances are verified by comparing the estimated probability values corresponding to the 40 three-tone EM disturbances considered for this particular case study. As the verification is done both for CSVCO and RO at all three temperatures, the generality of the reliability of deterministic CPD functions is also verified in measurements.

The noisy-OR model CPD functions are purely based on the causal independence assumptions, and the expression uses only the failure probabilities of single-tones to predict multitone failure probabilities. Which means, having a low value of prediction error, i.e., $P_M - P_N$ for three-tone disturbances will indicate that the independence assumptions are true. However, taking the mean prediction error for all 40 known three-tone disturbances into account, it was observed that the noisy-OR model prediction is in general, not very reliable. This is because, for some combinations, e.g., for CSVCO at −40 °C, the independence assumptions are not valid, hence leading to a higher standard deviation of 0.44. At higher temperatures, e.g., for CSVCO at 120 °C, where 68% of the combinations are of the synergistic type, the noisy-OR CPD function underestimates the probability of failure.

The expressions of the deterministic functions of ARNOR and I-ARNOR that were used in Section 4.3, were modified for this case study to include the temper-

Table 4.7: Probability of the EMI failure of CSVCO and RO due to three-tone disturbances (measurements) © [86].

Three-tone (MHz)	100, 200, 300	100, 200, 600	100, 300, 600	100, 500, 600	200, 300, 600	200, 500, 600	300, 500, 600	500, 600, 800	500, 700, 800	500, 800, 900	600, 700, 800	600, 800, 900	700, 800, 900	800, 900, 1000
CSVCO (−40 °C)														
P_M	0.428	0.996	1	1	1	1	1	0.146	0.383	0.085	0.254	0.148	0.182	0.151
P_N	0.648	0.179	0.648	0.179	0.572	0	0.572	0	1	0	1	0	1	0
DOS (%)	-34	>100	54.3	>100	75	>100	75	>100	-61.7	>100	-74.6	>100	-81.8	>100
Causality	I	S	S	S	S	S	S	S	I	S	I	S	I	S
CSVCO (25 °C)														
P_M	1	1	1	1	1	1	1	0	0	0.25	0	0.0	0.0	0.0
P_N	1	0	1	0	1	0	1	0	0.329	0	0.329	0.0	0.329	0.0
DOS (%)	0	>100	0	>100	0	>100	0	-66.7	-100	>100	-100	-66.7	-100	-66.7
Causality	I	S	I	S	I	S	I	I	I	S	I	I	I	I
CSVCO (120 °C)														
P_M	1	1	1	1	1	1	1	0.514	0	0	0	0	0	0
P_N	0.072	0.072	0.072	0.072	0	0	0	0	0.036	0	0.036	0	0.036	0
DOS (%)	>100	>100	>100	>100	>100	>100	>100	>100	-99.7	-66.7	-99.7	-66.7	-99.7	-66.7
Causality	S	S	S	S	S	S	S	S	I	I	I	I	I	I
RO (−40 °C)														
P_M	0.687	0.751	0.858	0.817	1	1	1	1	0.972	0.62	0.894	0.901	0.204	0.014
P_N	0.985	1	1	1	1	1	1	1	1	1	1	1	0	0
DOS (%)	-30.2	-24.9	-14.2	-18.3	0	0	0	0	-2.8	-38	-10.6	-9.9	>100	>100
Causality	I	I	I	I	I	I	I	I	I	I	I	I	S	S
RO (25 °C)														
P_M	0.625	0.518	0.429	0.571	0.125	0.286	0.214	0.161	0.054	0	0.125	0	0.155	0.056
P_N	0.739	0.376	0.751	0.38	0.633	0.085	0.635	0.103	0.087	0.135	0.126	0.172	0.157	0.204
DOS (%)	-15.4	37.7	-42.9	50.6	-80.3	>100	-66.3	56.2	-38.4	-99.9	-0.6	-99.9	-1.3	-72.3
Causality	A	S	I	S	I	S	I	S	A	I	A	I	A	I
RO (120 °C)														
P_M	0.513	0.478	0.64	0.394	1	0.819	1	0.007	0.008	0	0	0	0	0
P_N	0.86	0.716	0.663	0.317	0.795	0.585	0.507	0	0	0	0	0	0	0
DOS (%)	-40.4	-33.3	-3.6	24.4	25.7	40.1	97.2	>100	>100	-66.7	-66.7	-66.7	-66.7	-66.7
Causality	I	I	A	S	S	S	S	S	S	I	I	I	I	I

ature effects, and are given in (4.22) and (4.23), respectively. Both ARNOR and I-ARNOR are descendants of the noisy-OR model and are based on the RNOR model expression, represented as a (4.21). The deterministic CPD functions of RNOR (P_R), ARNOR (P_A) and I-ARNOR (P_I), including the temperature node variable T, are given as:

Table 4.8: Summary of the prediction accuracy of deterministic CPD functions for the IC failures due to three-tone EMI © [86].

IC	Temperature	Method	Mean Prediction Error	Standard Deviation
CSVCO	−40 °C	Noisy-OR	-0.010	0.44
		ARNOR	-0.193	0.29
		I-ARNOR	-0.040	0.17
	25 °C	Noisy-OR	0.192	0.50
		ARNOR	-0.213	0.35
		I-ARNOR	0.019	0.33
	120 °C	Noisy-OR	0.47	0.41
		ARNOR	-0.028	0.22
		I-ARNOR	0.105	0.23
RO	−40 °C	Noisy-OR	-0.137	0.22
		ARNOR	-0.150	0.21
		I-ARNOR	-0.002	0.22
	25 °C	Noisy-OR	-0.100	0.18
		ARNOR	-0.186	0.23
		I-ARNOR	-0.035	0.21
	120 °C	Noisy-OR	0.04	0.22
		ARNOR	-0.092	0.17
		I-ARNOR	-0.075	0.18

$$P_R(e|\,\tilde{\mathbf{f}},T) = \begin{cases} P_M(e|\,\tilde{\mathbf{f}},T), \\ \text{if available} \\ 1 - \displaystyle\prod_{k=0}^{r-1}\left[\frac{1-P_R(e|\,\tilde{\mathbf{f}},T\setminus\{c_{k+1}\})}{1-P_R(e|\,\tilde{\mathbf{f}},T\setminus\{c_{k+1},c_{\mathrm{mod}\,(k+1,r)+1}\})}\right], \\ \text{otherwise} \end{cases} \tag{4.21}$$

$$P_A(e|\,\tilde{\mathbf{f}},T) = \begin{cases} P_M(e|\,\tilde{\mathbf{f}},T), \\ \text{if available and,}\,\tilde{\mathbf{f}},T\text{: positive causality} \\ P_N(e|\,\tilde{\mathbf{f}},T), \\ \text{if } P_M(e|\,\tilde{\mathbf{f}},T) \text{ is available and, } \tilde{\mathbf{f}},T\text{: inhibition} \\ P_R(e|\,\tilde{\mathbf{f}},T) \\ \text{otherwise} \end{cases} \tag{4.22}$$

$$P_I(e|\,\tilde{\mathbf{f}},T) = P_R(e|\,\tilde{\mathbf{f}},T)\left[1 + \frac{0.01}{m}\sum_{i=1}^{m} DoS_m\right]. \tag{4.23}$$

The invalidity of RNOR to predict multitone failure probability has already been discussed. Thus, it is not used for the current EMI prediction. Note that, when using the I-ARNOR CPD function given in (4.23), the weighting parameter DoS_m corresponding to any multitone interaction of type synergy and asynergy is considered as 0.

The mean prediction error and standard deviation values obtained by applying the CPD functions in (4.22) and (4.23), for the 40 known three-tone disturbances are summarized in Table 4.8. In general, lower mean prediction error and standard deviation are observed for I-ARNOR model when compared to the ARNOR and the noisy-OR model. Even for the two exceptional cases where the noisy-OR has a relatively lower mean prediction error than I-ARNOR, i.e., for CSVCO at −40 °C and RO at 120 °C, the respective standard deviation is still relatively higher for the noisy-OR. For almost all cases except (CSVCO at 120 °C) the I-ARNOR has lower mean prediction error and slightly lower or higher standard deviation when compared to the ARNOR model. This implies the significance of using the mean DoS for more accurate results. Consequently, this verifies the general prediction capability of the I-ARNOR deterministic CPD function is limited to three-tone EMI failure probability.

4.5 Conclusion

In this chapter the importance of multitone testing was highlighted and was regarded as a risk-based approach due to the uncertain EM environment. Various types of causal interactions (synergy, asynergy and inhibition) were demonstrated to co-exist within multi-tone testing of a two independent integrated blocks. Furthermore, in real-world systems, positive causality of multitone EM disturbances means that unexpected component failures could be more likely in the systems' lifetime than standard (single-tone) immunity tests might suggest. However, for multitone interactions that are identified as inhibition, the traditional single-tone immunity verification techniques can be considered as a conservative approach.

Using simulation and measurement data for a CSVCO and RO circuit, the proposed I-ARNOR model was shown to have superior prediction accuracy to existing probabilistic models (i.e., the noisy-OR and ARNOR models). The simulations offered advantages, such as higher sampling rate and bandwidth as well as freedom to monitor signals at inaccessible traces. Measurements, however, are subject to practical limitations, such as PCB trace parasitics, cable losses, and other uncertainties, that are not included in the simulations. For these reasons, as well as to demonstrate wider applicability, experimental validation of the I-ARNOR probabilistic model was carried out on the 3-stage CSVCO and RO, and accurately validated the probability of failure due to higher order multitones.

Another environmental factor, i.e., temperature variation, indicated a deviation in the output frequency of both oscillators, with the CSVCO being more robust compared to the RO. However, the results were completely reversed when the effects of multi-tone EMI and temperature were combined. The CSVCO was substantially more susceptible to multitone EMI than the RO at extreme temperatures (-40 °C and 120 °C). While taking into account temperature, the probability of EM failure was found to be the lowest for the the inhibition type interactions. The variation in temperature impacted in the transition of synergistic frequency combinations to greater than 600 MHz for both oscillators, especially at the minimum temperature. Further, even with the influence of temperature the I-ARNOR model was able to predict the probability of three-tone EM disturbances, with slightly higher standard deviations, which could be due to the measurement uncertainty.

As demonstrated in this chapter for several case studies, through either simulations or measurements, the application of BN based models to include the uncertainties associated to the occurrence of multitone EM disturbances and other environmental factor(s) such as the temperature, can facilitate an expert to determine the risk of IC or component failure due to EMI in the system environment.

Chapter 5

EFT CONDUCTED EM IMMUNITY ANALYSIS

5.1 Introduction to EFT Testing

Similar to multitone disturbances, transient EM disturbances are also very uncertain and can occur in the system/IC. One common case of transient EMI is ESD, which occur as a result of the accumulation of electrostatic potential. It is a very sudden current flow that propagates through metallic or non-metallic materials, electrical systems and is a very short event, involving large currents, extremely high voltages, and durations in the range of a few hundred nanoseconds [121]. Currents can reach tens of amperes and voltage levels may surge up to several kilovolts. However, the total discharge energy remains low, around a few hundred millijoules (mJ). The power on the other hand is extremely high because the waveforms are changing extremely rapidly.

Consequently, ESD protection devices are necessary to divert current discharge before it reaches sensitive circuitry at the system and IC level. By offering a low impedance path to ground, they clamp input voltages to avoid crossing the maximum allowable levels. Those protections can absorb significant amounts of current for very short periods of time, but are not designed to sustain DC currents [122].

The robustness of electronic systems and ICs are tested against ESD using different methods and standards. System level tests reproduce discharge events encountered by a system deployed in the field. These involve higher voltage and current amplitudes, and are more harmful for electronic devices than IC level tests. In contrast, silicon level tests target ESD events happening during IC manufacturing [123]. This chapter will focus on EFT testing for characterizing digital/analog ICs and their ESD protections.

EFT/burst testing, defined in IEC-61000-4-4 [124], was developed to take into account the maximum switching repetitive transient cases at a relatively high frequency. It involves procedures for assessing susceptibility of electronic devices subjected to transient EM disturbances such as interruption of inductive loads and relay contact bounce [125]. Moreover, it concerns all kinds of inputs such as power supply, signal and control lines.

The defined waveform of EFT is a double exponential pulse with a width of 50 ns at 50% of the peak amplitude. Rise time is comprised between 4 ns and 6 ns. It is defined for a 50 Ω/1 kΩ load, with a pulse period of 15 ms/0.75 ms and a burst period of 300 ms. The peak EFT voltges levels can vary from 0.25 kV to 4 kV. These features are illustrated in Fig. 5.1.

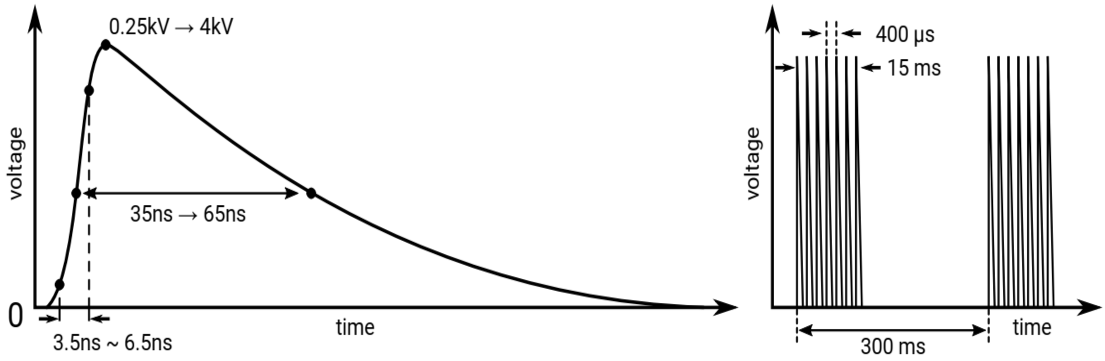


Figure 5.1: IEC 61000-4-4 waveform on a 50 Ω load [124].

Manufacturers use EFT testing to improve the quality of their products and to maintain industry standards and compliance. These bursts are applied at certain injection points in various methods of EFT testing. To test AC or DC supply ports, a coupling and decoupling network is required in the test setup. On the other hand for signal, data, control, or I/O ports, a capacitive coupling clamp is used [126]. The former method is applied in this manuscript on the individual power supplies of IC blocks. In the subsequent sections, EFT testing is adopted to evaluate and compare the transient conducted EM immunities of microcontrollers and integrated oscillators.

The results related to the case studies discussed in Sections 5.2 and 5.3 have been published by the author in [125] and [126], respectively. The results of these sections draw of course on the relevant publications.

5.2 Case Study 1: Obsolescence and EFT Immunity of Microcontrollers

Microcontrollers (μCs) build up the core of embedded systems [127]. Therefore, their specific EMC characteristics and, in particular, their immunity to EMI, are crucial for proper operation over the entire lifetime of a system. Conducted immunity testing of μCs can be carried out either in continuous wave or in transient mode. Among the latter, EFTs are among the most widely used for industrial EMC testing [128]. The EFT signal can be injected into either functional or power supply pins of an IC using magnetic or electric coupling. This interferes with the standard behavior of the μC, causing temporary malfunction or even irreversible damage.

In comparative literature, there are several works reporting information on EFT testing of μCs with different architectures [129]–[131]. However, apart from repeatability, the reasons for the observed failures still have to be clarified in terms of root cause for the ICs selected in those studies. Unfortunately, transient immunity testing is often performed only on a brand new product, not taking into account how the EMC behavior of an IC could evolve within the lifetime of that product. This may result in high risk factors due to EMC-related reliability issues. For example, the following could influence that behavior:

- technological dispersion in IC characteristics (effective channel length, doping, etc);
- ageing due to environmental characteristics (temperature, humidity, vibration, etc);
- obsolescence (replacing an IC by another functionally identical or pin-to-pin compatible IC).

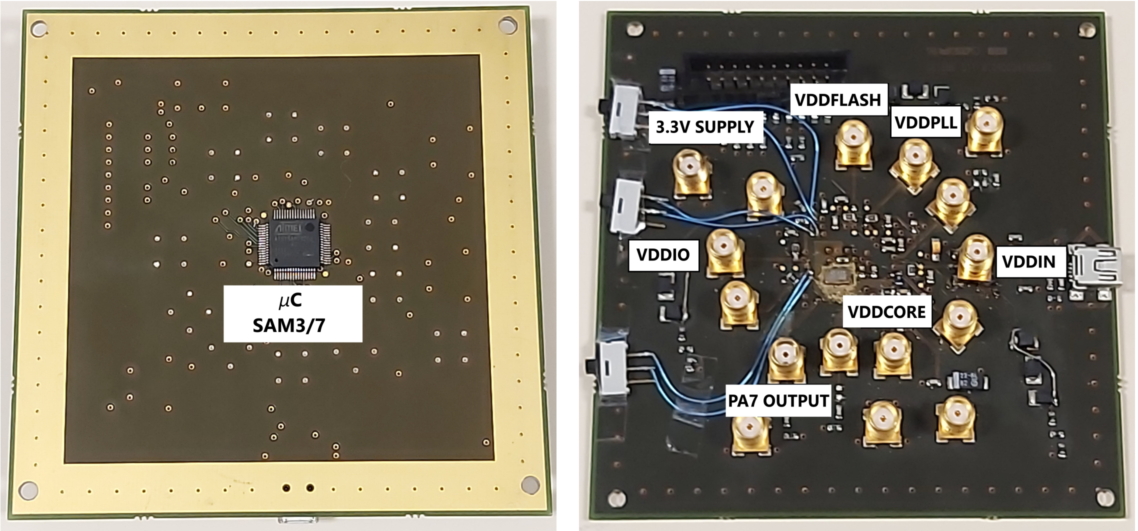
This case study only focuses on obsolescence of ICs to provide the contribution to the very vast domain of EMC risk assessment. Manufacturers are regularly searching for practical and time-efficient techniques for reducing the potential limitations of IC obsolescence [132]. If an IC has become obsolete, it should be verified that its successor will not be more susceptible, in order to ensure that the whole system complies with at least the same performance level according to EMC standards. To study the obsolescence of ICs, EFT testing was performed on two 32-bit μCs

(Microchip SAM7S256 [133] and SAM3S4B [134]), the latter being the a more recent version ideal for migration from SAM7 [134]. These tests were carried out to identify and further clarify the failure caused by the EFT injection into the individual voltage supply pins of the μCs. Both μCs have identical peripherals and pinouts, but with different core architectures (ARM7TDMI and Cortex-M3, respectively) and flash memory voltages; software can be ported from SAM7 to SAM3 with only minimal changes.

5.2.1 Test Boards Description

The two SAM3 and SAM7 μCs selected for this case study are pin-to-pin compatible, having similar internal oscillators, external bus interfaces, peripherals and packaging. They require a 3.3 V supply voltage (and, optionally, another 1.8 V supply voltage) to operate reliably and are mounted on identical test boards. Both μCs use separate 3.3 V power supplies for I/O buffers (V$_{DDIO}$) and for their internal 1.8 V regulator (V$_{DDIN}$). Only for SAM7, a third 3.3 V power supply is used to power the Flash memory array (V$_{DDFLASH}$), which is replaced by an I/O on SAM3. Either the output of the internal voltage regulator (V$_{DDOUT}$) or an external supply can be used for the 1.8 V power supplies. Those supplies consist of V$_{DDPLL}$ (powering the PLL and the internal oscillator) and V$_{DDCORE}$ (powering the CPU core and, for SAM3 only, the Flash memory array). Moreover, another difference can be noticed between both μCs: SAM7 uses an external PLL loop filter, while that filter is integrated in the SAM3 (the filter pin is also replaced by an I/O).

Each testboard (Fig. 5.2) is a 10 × 10 cm standard IEC 62132-2 [135] printed circuit board (PCB) fitted with modular SMA connectors for different power supplies and I/Os. The PA7 pin will be used to monitor the immunity of both μCs. Fig. 5.3 summarizes the connections that can be set up among all power supplies on both PCBs. As can be seen, each power supply pin is equipped with a zero-ohm series resistor, making it possible to either connect it to the general power supply (J33 for 3.3 V, J34 for 1.8 V) or to the dedicated power supply of an EFT generator to test it individually. Decoupling capacitors are connected to each pin, in order to put the μC in the standard operating conditions recommended by the manufacturer. Since the objective of the study is only a functional comparison, those capacitor values are not critical. Finally, CV1 and CV2 make it possible to switch the 1.8 V supply between the internal voltage regulator output and an external supply. Both



(a) (b)

Figure 5.2: EFT Test Board (SAM3/7) © [125]: (a) front; (b) back.

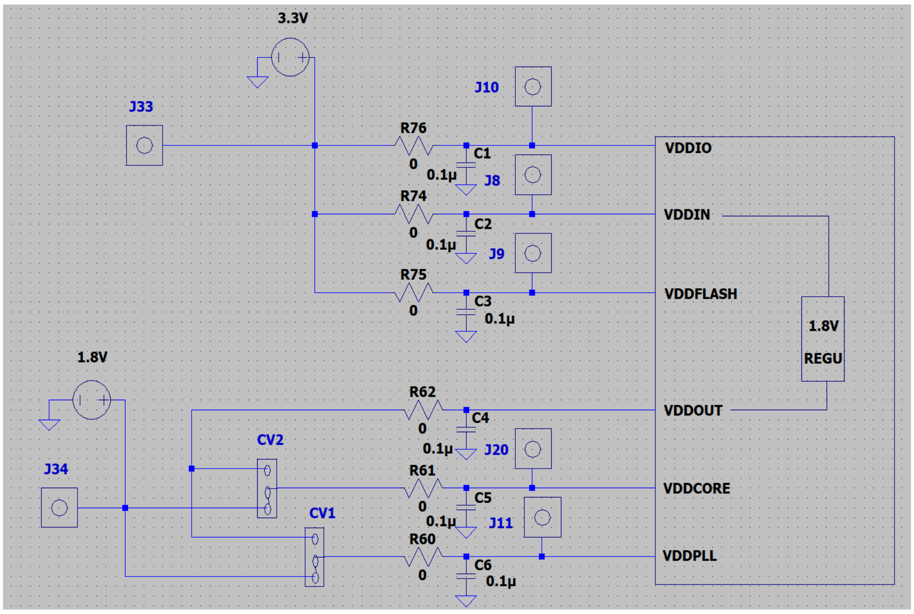


Figure 5.3: Schematic of SAM3/7 © [125].

SAM3 and SAM7 are programmed to generate a square wave through PA7. The observed frequency of the wave generated by SAM3 (200 Hz) is twice as that of SAM7 (100 Hz) due to a difference in PLL configurations. Likewise, that difference is not crucial for functional testing.

5.2.2 Hardware Setup and Procedure

EFT is a low-energy test, usually (but not always) non-destructive, having a wide spectral frequency content creating problems with sensitive sensors and μCs. During the EFT test, a repetitive voltage transient is induced over either a DC supply line or a functional signal. For this case study, only injection into DC supplies was considered for each μC. Each individual EFT pulse was characterized by a 5 ns rise time, 50 ns pulse width, 300 ms burst repetition, 5 kHz spike frequency, and 15 ms burst duration. The positive polarity EFT signal was ramped from 250 V to 4 kV in 100 V steps [124].

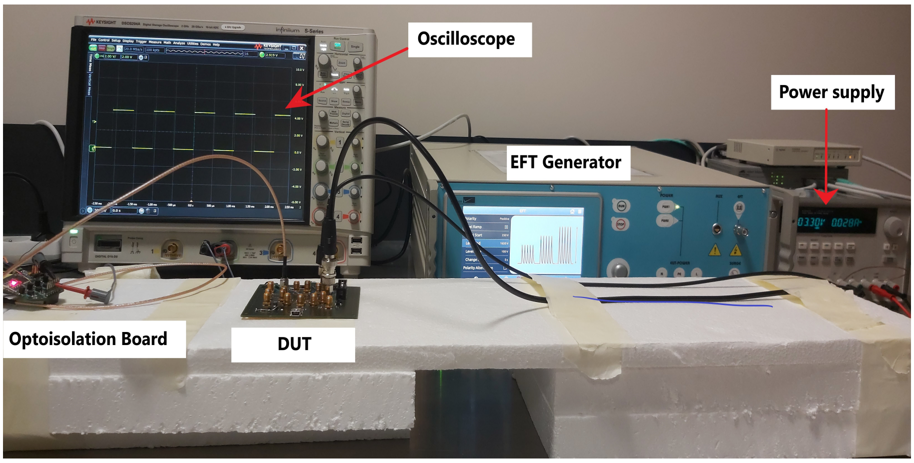


Figure 5.4: EFT Test Setup for μC immunity testing © [125].

The test bench for EFT primarily included the adapter board for the DUT, an EMC-Partner IMU4000 EFT generator [136], a dual-channel Agilent E3631A DC power supply with current monitoring, a Keysight DSOS0204A oscilloscope to monitor the PA7 signal, and a custom optoisolation board. This setup is exhibited in Fig. 5.4. One channel of the power supply is connected to the internal coupler of the EFT generator (making it possible to superimpose the disturbance with the DC voltage), while the other channel is used as an auxiliary supply to power IC pins that should remain undisturbed. Both current limits were set to 1 A. The customized optoisolation board shown in Fig. 5.5 is designed with optocouplers to avoid reinjection of high-voltage EFT signals into the oscilloscope. The optocouplers chosen for that board are low-current (1 mA) with inverting 5 V digital outputs. The PA7 output of either μC is connected to the input of one of the optocouplers through a cable connected to the corresponding SMA connector of the DUT. Since that output only delivers around 1.2 mA for both μCs, it can be noted that a slight variation of that current due to injection may dramatically change the low output level of their outputs, and the voltage-to-voltage transfer function is totally non-linear. Consequently, the analog behavior of the I/O due to the EFT voltage cannot be accurately monitored by the signal observed on the oscilloscope, and the output voltage of the optocouplers can not be considered as a valid immunity criterion.

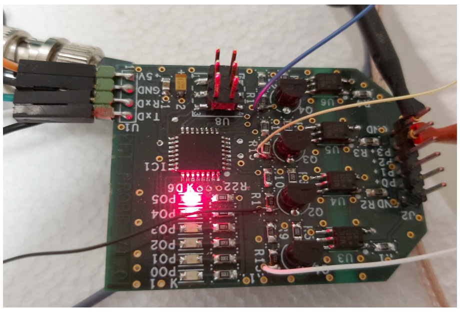


Figure 5.5: Custom optoisolating board © [125].

After a first EFT injection into the common 3.3 V power supply (powered through the EFT generator), all resistors were removed one by one and a separate power supply was used on J33 for the remaining tests (performed through J8 to J10). Then, all resistors were fitted again in the 3.3 V supplies, and the same operation was repeated for 1.8 V supplies, using V_{DDOUT} as the separate power supply when required.

5.2.3 EFT Failure Modes for Microcontrollers

As discussed previously, the only immunity criterion to monitor a failure in the practical EFT tests performed is the μC crash, i.e. the square wave from PA7 being no longer observable on the oscilloscope, due to the embedded software not running properly. Table 5.1 shows apparent failure types classified from A to E.

No failure (A) occurs when the supply pin is completely immune to EFT and causes no malfunction in the μC.

Self-recovery (B) is likely to be due to the power-on-reset (POR) or low-voltage detector (LVD) blocks [124]. POR maintains an internal RESET while the core power supply is below a given threshold when the the supply voltage is applied from zero, while LVD maintains the internal RESET when the supply voltage drops

Table 5.1: Specification of EFT Failure modes for μCs © [125].

Classification	Failure Type	Description
A	No Failure	The μC does not crash and remains operational during EFT exposure
B	Self-Recovering	The μC crashes and resumes operation as soon as EFT exposure is removed
C	Soft Failure	The μC crashes and is only operational after EFT exposure is removed and a manual reset is performed
D	Repower Recovering	The μC crashes and is only operational after EFT exposure is removed and power cycling is performed
E	Damaged	The μC is permanently deteriorated due to EFT exposure

below another threshold, until it rises back to its nominal value. In both cases, that automated RESET makes it possible for the μC to restart from a well-known state.

Soft failure (C) usually occurs when the state machine of the μC core crashes into an unknown state due to interference, which can be recovered by an explicit (external) RESET of the core.

Repower-recovering (D) implies that the core is unable to restart by itself when reset. This may be due, for example, to a crash in the Flash memory controller or an internal signal maintained at an incorrect level due to latch-up. This can only be resolved by power cycling. Sometimes, a slight increase in DC current may be observed due to that incorrect state.

The E-type failure encompasses “soft” and “hard” damage which, in both cases, prevent the μC from restarting when power is cycled. “Soft” damage refers, for example, to a spurious erasure of a Flash memory block (or a change in Flash contents) due to the interference triggering the state machine of the Flash controller. “Hard” damage reflects a permanent, physical damage in the IC structure; in that case, a significant rise in the DC supply current is often observed.

5.2.4 Experimental Results and Discussion

This section deals with the direct impact of EFT disturbances on the performance of the SAM3 and SAM7 μCs. Each mentioned pin was subjected to a specified range of EFT and the square wave generated through PA7 is monitored in real time. An apparent failure was reported when the μC crashed and a constant high/low logic level was detected. This depends on the current state of the logic level when the μC software stops running. A comparison was drawn depending on the types of failure of each supply pins of both boards and their specific causes are explained.

The first practical test involved ramping the EFT signal on the 3.3 V (J33) main supply of SAM3 and SAM7. The lowest value of the EFT signal was 250 V due to the limits of the EFT generator. The maximum value of the EFT signal was intentionally limited to 1.65 kV. The abrupt increase in DC current was the deciding factor to be limited to this voltage not to damage the test boards. For SAM3, when the EFT signal was injected at 250 V, the square wave instantly began to oscillate and flickers were visible on each rising and falling level. The oscillations increased with constant rise in EFT voltage and maximum amplitude levels at the optocoupler output were reduced by 21% (3.4 V) compared to the original signal; it should be remembered that this reduction in amplitude is due to a reduction in the optocoupler input current and, therefore, can not be considered a significant immunity criterion. There was no failure observed on the main supply of SAM3. Similar to the main supply, V$_{DDIO}$ and V$_{DDIN}$ were immune to EFT up to 1.65 kV (Fig. 5.6).

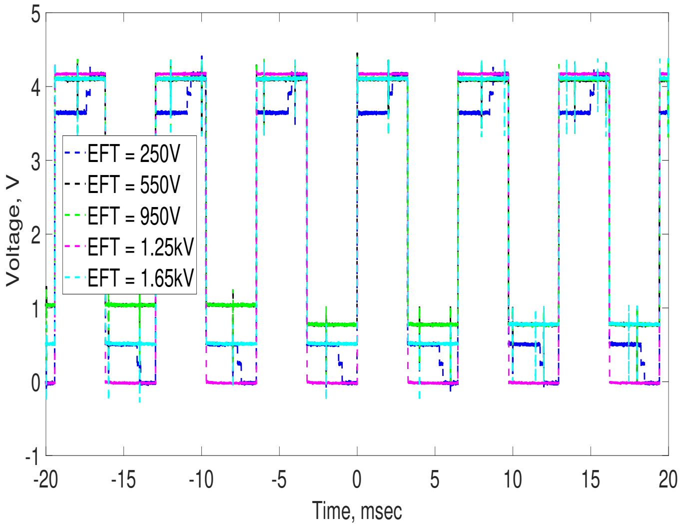


Figure 5.6: Output of SAM3 after EFT injection to main supply (Equivalent results with SAM3 V$_{DDIO}$ and V$_{DDIN}$) © [125].

Different results were obtained for SAM7. The μC crashed for an EFT voltage as low as 250 V on the global 3.3 V supply, delivering a low logic level at the optocoupler output (i.e. high on the PA7 pin), as shown in Fig. 5.7. A D-type failure was observed, and the signal was recovered after power cycling. When EFT was injected into V$_{DDFLASH}$, the SAM7 crashed for the same injection level (250 V). Prominently displayed in Fig. 5.8, the V$_{DDIO}$ of SAM7 crashed at 450 V, resulting in a soft failure (C). The DC current experienced an abrupt rise from 21 mA to

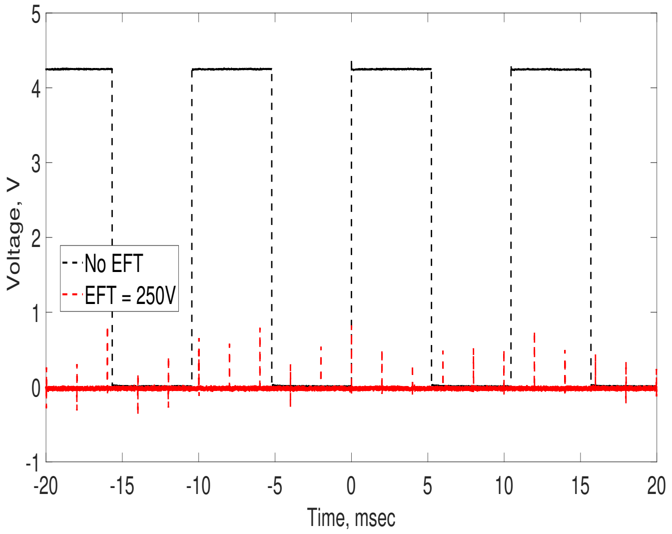


Figure 5.7: Output of SAM7 after EFT injection to main supply (Comparable results with SAM7 V$_{DDFLASH}$) © [125].

289 mA. Interestingly, that increase did not seem to come from permanent damage to the chip, since the current returned to its nominal value after resetting the chip.

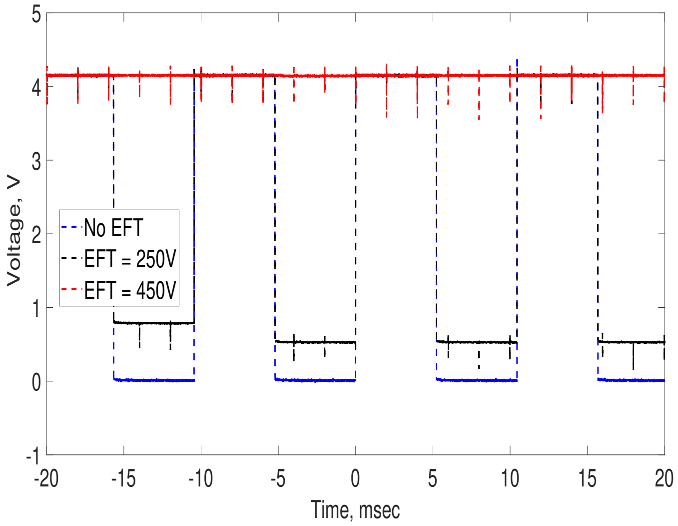


Figure 5.8: Output of SAM7 after EFT injection to V$_{DDIO}$ © [125].

The V$_{DDIN}$ of SAM7 was immune to a higher EFT voltage level, with increasing harmonics and oscillations. However, at exactly 1.05 kV, the DC supply current drastically increased from 37 mA to 854 mA. This time, the DC current remained at the same value after power cycling. The SAM7 was permanently degraded (E),

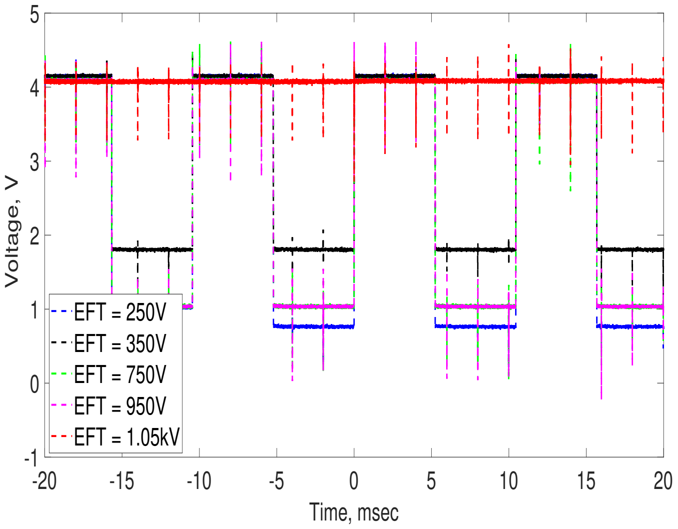


Figure 5.9: Output of SAM7 after EFT injection to V_{DDIN} © [125].

as shown in Fig. 5.9, and had to be replaced by a new IC for subsequent tests, since it was not even possible to reprogram its Flash memory. The sole matching results for both μCs were obtained when EFT was injected into the V_{DDCORE}. In that context:

- the DC power supply connected to the EFT generator was adjusted so that the V_{DDCORE} pin was supplied with 1.8 V.
- the internal 1.8 V regulator was powered from the secondary power supply channel connected to all 3.3 V pins, and its output was connected to the V_{DDPLL} pin.

This pin was susceptible to EFT on both SAM3 and SAM7. As displayed in Fig. 5.10, a self-recovering (B) failure was encountered by both μCs at 250 V, with no sudden change in current. The V_{DDPLL} pins were tested using a similar procedure as above. The SAM7 PLL was more immune (1.45 kV) to EFT than that of SAM3 (550 V). Those results are compared in Fig. 5.11.a and 5.11.b.

All the mentioned experimental EFT failure voltages and their respective pins are summarized in Table 5.2. To sum up, the SAM3 μC is generally more immune to EFT than the SAM7, except on the V_{DDPLL} pin where a significantly lower EFT voltage triggers a recoverable failure (550 V compared to 1.45 kV). note that all those results were verified to be repeatable, even when SAM7 was changed due to permanent damage after V_{DDIN} injection.

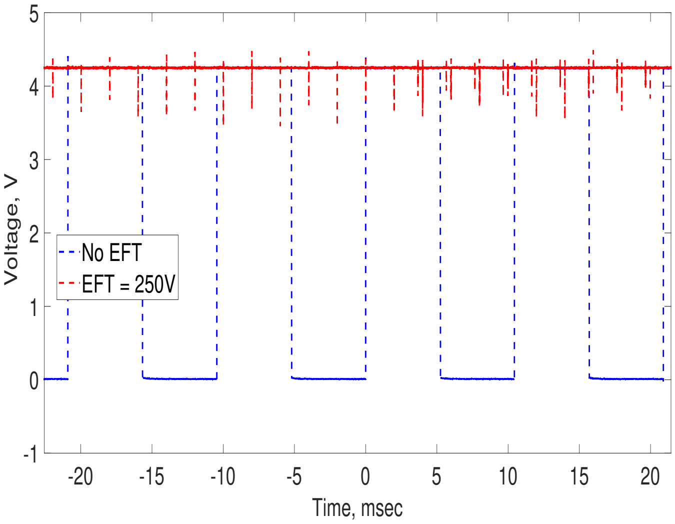
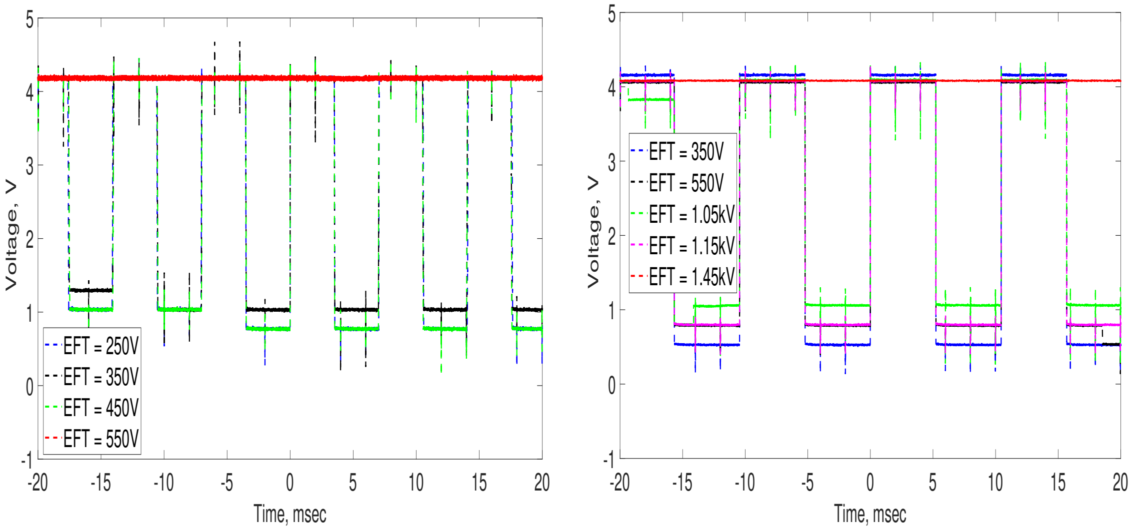


Figure 5.10: Output of SAM3 after EFT injection to V$_{DDCORE}$ (Matching results with the SAM7 V$_{DDCORE}$) © [125].



(a)

(b)

Figure 5.11: EFT applied to V$_{DDPLL}$ © [125]: (a) SAM3; (b) SAM7.

Both SAM3 main supplies (V$_{DDIO}$ and V$_{DDIN}$) were immune to EFT up to the limit (1.65 kV) determined by a change in DC current. However, this was not the case for SAM7. With only global injection results, that failure could be attributed to almost any block of the SAM7. It was later verified that the main supply failure (D) was due to V$_{DDFLASH}$, since equivalent results were obtained for the same voltage

Table 5.2: Maximum Applied EFT Voltage (Failure Type) © [125].

Pin No.	**SAM3**	**SAM7**
Global Supply	1.65 kV (A)	250 V (D)
V_{DDIO}	1.65 kV (A)	450 V (C)
V_{DDIN}	1.65 kV (A)	1.05 kV (E)
$V_{DDFLASH}$	Not Applicable	250 V (D)
V_{DDCORE}	250 V (B)	250 V (B)
V_{DDPLL}	550 V (C)	1.45 kV (C)

when that pin was subjected to EFT, while all other power pins were susceptible to higher voltages. As mentioned earlier, only the SAM7 Flash memory is susceptible to such a level. This can be corroborated by the type of failure, which suggests a defect in the operation of the Flash controller. The V_{DDIO} of SAM7 was shown to be more susceptible to EFT when compared to that of SAM3. The root cause may be a defect in the port controller or the buffers themselves. It can be noted that V_{DDIO} is a dual-range (1.65 V to 1.95 V, or 3.0 V to 3.6 V) power supply, which might make the port architecture more complex and, possibly, less immune than the wide-range (1.62 V to 3.6 V) supply used in the SAM3. As far as V_{DDIN} is concerned, the probable cause for the SAM7 failure could be due to the internal regulator or the input clamp being destroyed, leading to a permanent high current and an unusable chip.

The B-type failures noticed for the V_{DDCORE} of both SAM3 and SAM7 are likely due to the brown-out detector (BOD) block, which monitors only V_{DDCORE}, being triggered and holding the cores under RESET until the disturbance stops (that would explain how two different cores have the same behavior despite different internal architectures). This could be confirmed by examining, by software, registers containing the latest RESET source of the μC, making it also possible to design specific defensive software capable of recovering from soft failures. Finally, it can be observed that the PLL of the SAM3 is less immune than that of the SAM7. In both cases, a C-type failure is triggered. It can be noted that the cores enter an idle state when a clock failure is monitored, from which is it possible to exit through a hardware RESET. This is consistent with the observed type of failure. As mentioned in Section 5.1.2, a visible difference between both μCs is the inclusion of the PLL loop filter in the SAM3. This might explain the difference in immunity, since the EFT disturbance could be attenuated by the package parasitics of the loop filter pin driving the external RC filter of the SAM7.

5.2.5 EMC Risk Assessment of Obsolescence

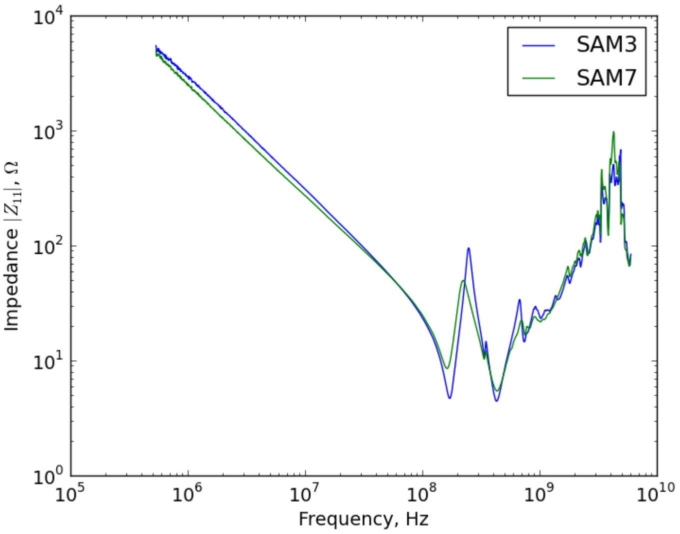


Figure 5.12: Input impedance Z_{11} of V$_{DDPLL}$ for SAM3 and SAM7 © [125].

From the obtained results, it can be concluded that replacing a SAM7 μC by a pin-compatible SAM3 μC can result in a better EFT immunity, except for the PLL. This highlights the need for a detailed EMC study when dealing with obsolescence, since a more recent IC does not necessarily mean a higher immunity. It can be noted, as expected, that very simple EMC measurements in the linear operating region of the IC do not provide significant hints about the expected EMC behavior of an IC to transient disturbances. For example, Fig. 5.12 plots the magnitude of the input impedance (Z_{11}) of both V$_{DDPLL}$ pins, extracted from S-parameter measurements with a vector network analyzer (VNA). It can be seen that impedance profiles are very comparable, whereas immunity levels are not. This calls for the implementation of extensive EMC testing and/or modeling to verify the compliance of possible replacement ICs compared to existing ones; this has already been corroborated in

[137] for memories subject to CW injection.

The use of non-linear transient immunity models such as ICIM-CPI (integrated circuit immunity model - conducted pulse immunity) [138] can be a valuable help to the simulation of EMC risk assessment for whole PCBs and/or systems. However, at the time being, they still do not take into account the evolution of immunity parameters as functions of ageing and/or obsolescence.

To summarize, a comparative study was conducted between two pin-compatible SAM3 and SAM7 μCs, the former being a more recent version suitable for upgrade, to investigate the EFT immunity of their individual voltage supply pins. The μC crash was considered as the immunity criterion to monitor the failure due to the injected EFT bursts with respect to the IEC 61000-4-4 standard. Results show that, except for the PLL supply pin, SAM3 had higher EFT immunity compared to SAM7 on all the considered supply pins. The core supply pin was found to be the least immune to EFT injection in both μCs (except for the Flash supply pin which is present only on SAM7). Moreover, regardless of the failure type, the obtained results were verified to be entirely reproducible.

5.3 Case Study 2: EFT Immunity of Oscillators Under Thermal Stress

Due to the downscaling of CMOS transistors, a modern IC can be sensitive to the ESD stress, which leads to the reduction of its intrinsic robustness [139]. Therefore, all supply and I/O pads of an IC include ESD protection circuits. Transient conducted immunity testing such as EFT, as defined in IEC 61000-4-4 [124], is typically performed in industry to check the robustness of ESD devices. EFT induced transients act as an exponential voltage pulse, in contrast to the underdamped sinusoidal voltage waveforms generated in system-level ESD tests [140]. The EFT signal can be injected into the power supply or functional pins of an IC through magnetic or electric coupling. This can interfere with the functional behavior of the IC, causing for example a transient induced latch-up effect or even irreversible damage [141].

Integrated oscillators are a vital part of analog/digital IC blocks such as PLLs and are vulnerable to transient EM disturbances, even if protected by ESD devices. Temperature variations can also influence the protection capability of the ESD devices, hence, affecting the immunity of the oscillator. Additionally, faster transistor switching in the oscillator's inverter stages can raise junction temperatures and diminish its performance. Therefore, stability against temperature changes and immunity to transient EM disturbances, such as EFT, require reasonable attention to ensure reliable operation of an oscillator.

In literature, researchers have focused on analyzing and improving the latch-up immunity of CMOS ESD devices [142], [143]. In addition, some authors have specifically studied the latch-up behavior of ESD circuits under EFT stress [144]. The importance of analytical EFT modelling to investigate the immunity of an IC has been discussed in [145]–[147]. Furthermore, the characterization and prediction of EFT immunity through numerical simulations have been highlighted in [148], [149]. The susceptibility to conducted EM disturbances (continuous wave and transient) in the power supply of ring oscillators has been analyzed in [150], [151]. Moreover, some work has been performed to observe the effect of temperature variations on the behavior of ESD devices in an IC [152]–[154]. The comparison of EFT immunities of integrated oscillators, having the same ESD protection devices but different topologies, has not been investigated. Moreover, the influence of temperature on such immunities has not yet been addressed.

In the current case study, the performance of three oscillator circuits, namely 3- and 5-stage CSVCOs and a 3-stage RO, is compared with respect to EFT under the influence of thermal stress through measurements. The effect of the IC package on the observed EFT immunity levels of each oscillator is also investigated. Furthermore, simulations at transistor level are implemented to identify the change in oscillator frequency due to EFT injection and analyze the effect of EFT and thermal stress on relevant MOSFET characteristics. The oscillators integrated, among other structures, into the 1.52 mm × 1.52 mm PETER_ESEO research chip, which was fabricated in SOI CMOS 180 nm 5 V technology. Each oscillator has an isolated power supply pad (V_{DDI}) and a single separate ground (G_{NDI}). The output of each oscillator is connected to an analog pad having a parasitic capacitance, and an ESD protection circuit which will clamp the generated signals that are not within the 0 to 5.5 V range.

A multi-stage digital FD circuit is added at the output stage of each oscillator to decrease the fundamental frequency of the generated signal [85]. The FD is powered by the global power supply V_{DD}, which is isolated from each oscillator's individual power supply and enables monitoring the frequency at the analog output pad without filtering effects caused by the parasitic pad capacitance. The simulated maximum operating clock frequency of the FD was found to be 900 MHz. Further details on the oscillator schematic, layout ESD pads and packaging can be found in Section 2.2.4 and 2.3.

To test the conducted immunity of the IC, two similar 13 cm × 13 cm 4-layer FR4 PCBs, referred to as packaged and chip-on-board (COB), were designed according to IEC 62132-4 [4]. The former PCB variant consisted of the CQFP package, while in the latter version the die was mounted directly on the PCB using a conductive epoxy resin (LOCTITE ECCOBOND EO1016). The PCBs were not overloaded with non-linear components, to precisely measure the immunity of the IC. For both versions, all isolated grounds of the IC were connected to the global ground. Additionally, a 470 Ω resistor was added in series to the output of each tested oscillator, in order to limit high voltage signals from being re-injected into the IC or the oscilloscope [86].

5.3.1 Effect of Temperature on Oscillator's Frequency

Deviations in temperature can progressively impact the performance of CMOS circuits such as oscillators. It can effect the drain current, effective mobility (μ_{eff}) and the threshold voltage (V_{th}) of the CMOS transistors in the oscillator inverter stage [126]. The packaged PCB variant was placed in a SATIMO thermal oven with voltage biasing applied through high temperature cables (Amphenol-RF 095-902-466-004). While maintaining the ambient temperature at 25 °C, the output frequency of each oscillator at the output pin was monitored through an oscilloscope with 1 MΩ input impedance. To verify the dependency of the output frequency on temperature, the former was recorded at extreme temperatures (−40 °C and 120 °C) for all tested oscillators as shown in Table 5.3. Although the operating and output frequencies of each oscillator are different, the gate size in the inverter stage is identical for all oscillators for a fair comparison. Hence, the temperature variation will equally affect on the transistors' V_{th} levels. Moreover, the respective minimum and maximum temperatures were chosen since it corresponds to the temperature limits of all the components soldered on the tested PCB.

For all oscillators, the output frequency was found to be inversely proportional to temperature (Table 5.3), which is due to altering the μ_{eff} and drain currents of the MOSFETs in the inverter stages as a function of frequency. For the FD circuit, temperature changes only affected the DC offset (±0.2 V) of the output voltage and

Table 5.3: Measured Operating (before FD) and Output Frequencies (after FD) at Nominal and Extreme Temperatures © [126]

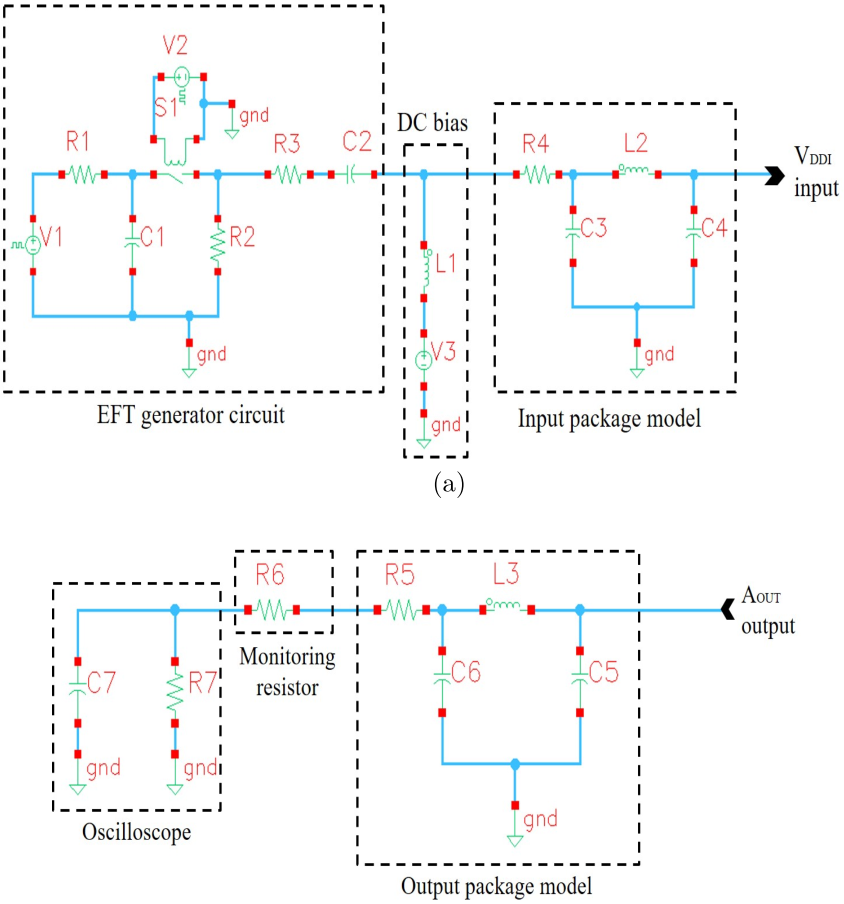
Type of Oscillator	Operating frequency	Output frequency (−40 °C)	Output frequency (25 °C)	Output frequency (120 °C)
3CSVCO	703 MHz	68.3 MHz	62.5 MHz	53.8 MHz
5CSVCO	271 MHz	71.6 MHz	66.1 MHz	61.4 MHz
3RO	955 MHz	117.4 MHz	97.7 MHz	78.2 MHz

not the frequency. However, with the rise in temperature, for input frequency signals greater than 900 MHz, the propagation delay in the FD becomes higher than the oscillator's period, and the measured output frequency is thus considerably reduced.

It was found that the deviations of output frequency from the nominal frequency for the 3- and 5-stage CSVCO and 3-stage RO over the entire temperature range were +9.3%, +8.3%, +20.2% (at −40 °C), and −13.9%, −7.1%, −19.9% (at 120 °C), respectively. Comparing the 3-stage CSVCO and RO, the former has a higher on-state drain-to-source resistance in the inverter stage (5.8 kΩ compared to 1.6 kΩ at the ambient temperature) due to the inclusion of the biasing transistors. That reduces the drain current in the CSVCO inverter stage resulting in a lower frequency deviation with thermal stress. As far as the RO is concerned, the FD circuit was found to have an impact on the observed output frequency at extreme temperatures due to the operating frequency (955 MHz) being higher than the maximum clock frequency (900 MHz). For the CSVCO, the increase in the number of stages from 3 to 5 improved the resilience of the output frequency to temperature variations (Table 5.3) due to a higher number of stages. In fact, due to the external biasing voltage being different for both CSVCOs (1.8 V and 1.6 V for 3- and 5-stage CSVCOs), the $V_{GS} - V_{th}$ term, to which the drain current is proportional, does not vary over temperature in the same proportion for both CSVCOs.

5.3.2 EFT Simulation Setup

EFT is a low energy test having a wide spectral frequency content creating problems in sensitive analog circuits such as integrated oscillators. In this case study, EFT was only injected into the V_{DDI} of each oscillator. The equivalent circuit for the EFT transient noise generator (Fig. 5.13.a) defined in IEC-61000-4-4 [124], was simulated in Cadence Virtuoso.



(a)

(b)

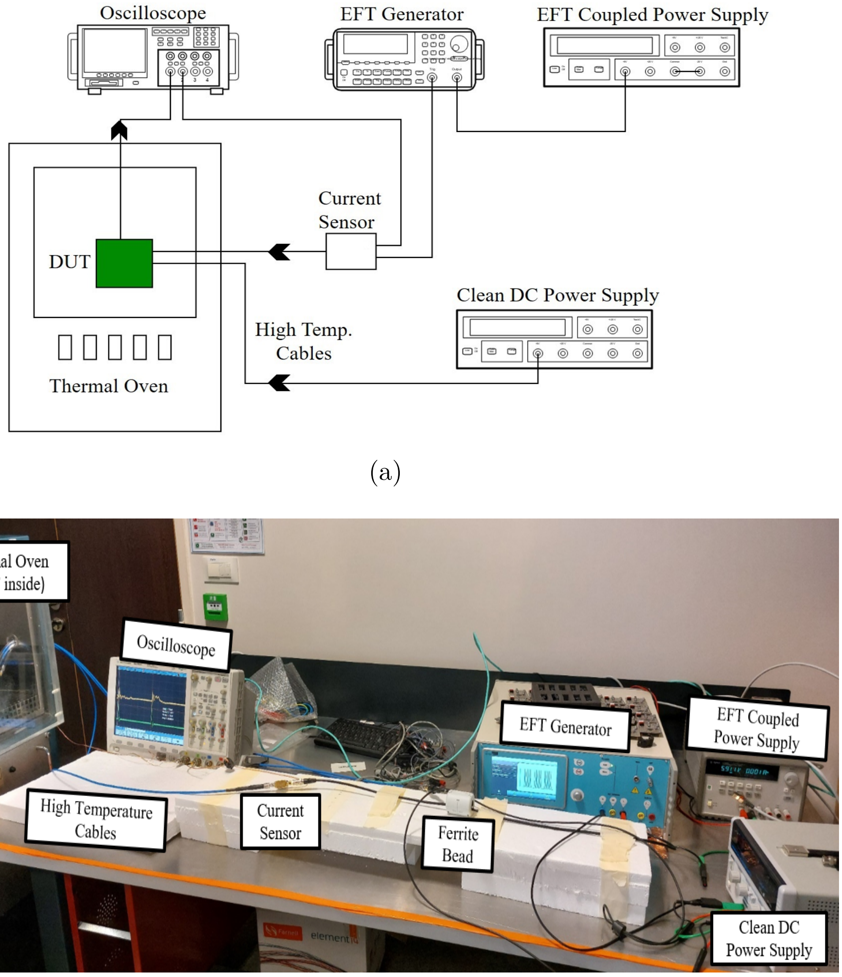
Figure 5.13: EFT simulation setup for the packaged version © [126]: (a) input path; (b) output path.

Only the impedance-matching resistor R3 (50 Ω) and the DC-blocking capacitor C2 (10 nF) are fixed by the standard. The charging resistor R1 and the capacitor C1, used to store the charging energy, were set to 5 Ω and 6 μF. The resistor R2 (12 mΩ) was used to shape the pulse duration of the EFT signal. According to [124], each individual pulse was characterized by a 5 ns rise time, 50 ns pulse width, 100 kHz spike frequency, 0.75 ms burst duration and 300 ms burst repetition. The positive polarity EFT signal is ramped from 250 V to 2 kV.

As seen from Fig. 5.13.a, the EFT signal input path includes the generator circuit, the biasing power supply V3 (5 V) in series with a choke inductor L1 (100 μH), and the IC package model feeding the V_{DDI} pad of the oscillator. The inductor ensures that a high impedance path is created for the EFT disturbances so that they are not absorbed by the supply. The output path is composed of the analog output pad (A_{OUT}), the output package model, monitoring resistor and the oscilloscope model (Fig. 5.13.b). The monitoring resistor R6 (470 Ω) has a temperature coefficient of 100 ppm/°C. The oscilloscope model includes a high impedance resistor R7 (1 MΩ) and its parasitic capacitance C7 (16 pF) which only affects the peak voltage of the oscillating output signal. The CQFP package of the chip was modelled using the IC-EMC software [105], to extract the approximated package model consisting of passive lumped elements found through IC parameters such as die size, pitch, lead frame and cavity sizes. The I/O package model elements are R5 (4.5 Ω), C6 (10.2 pF), L3 (9.1 nH) and C5 (1.7 pF). No decoupling capacitor were included in the simulation setup or the tested PCBs. This was specifically done to avoid any additional effects caused by external components when subjected to thermal stress, seeing that no external components were required to ensure proper operation of the integrated blocks. The simulation setup will be used in Section 5.3.8 to analyze the effect of the EFT signal on the frequency behavior as well as relevant MOSFET characteristics of the considered oscillators at extreme temperatures.

5.3.3 EFT Measurement Setup

The test bench includes an EFT generator (EMC-Partner IMU4000), two dual-channel DC power supplies (Agilent E3631A), a pulse current sensor (HPPI CS-0V5-A), an oscilloscope (Agilent MSO7104A), and the SATIMO oven. The EFT measurement block diagram and the test setup are depicted in Fig. 5.14a and 5.14b, respectively. One of the power supplies is connected to the internal coupler of the EFT generator, making it possible to superimpose the disturbance with the DC voltage (5 V) feeding the V_{DDI} pin of each oscillator. The channels of the other power supply are connected to the V_{DD} and V_C of the DUT providing a constant voltage of 5 V and 1.8 V, respectively. The V_{DD} is the global power supply that powers up the padring and the FD circuit. Both V_{DD} and V_C are completely isolated from the injected EFT disturbances.



(a)

(b)

Figure 5.14: EFT measurement © [126]: (a) block diagram; (b) test setup.

The current sensor, with a nominal sensitivity of 0.5 V/A, is connected in series with the EFT generator to monitor the input current being injected into the DUT. A ferrite bead is also connected to the EFT generator cable to filter out high frequency RF signals being re-injected into the power supply. The DUT is placed inside the oven and the output pin of the tested oscillator is connected to one of the channels of the oscilloscope (1 MΩ) via high temperature cables. The second channel of the oscilloscope is connected to the current sensor's 50 Ω monitoring output.

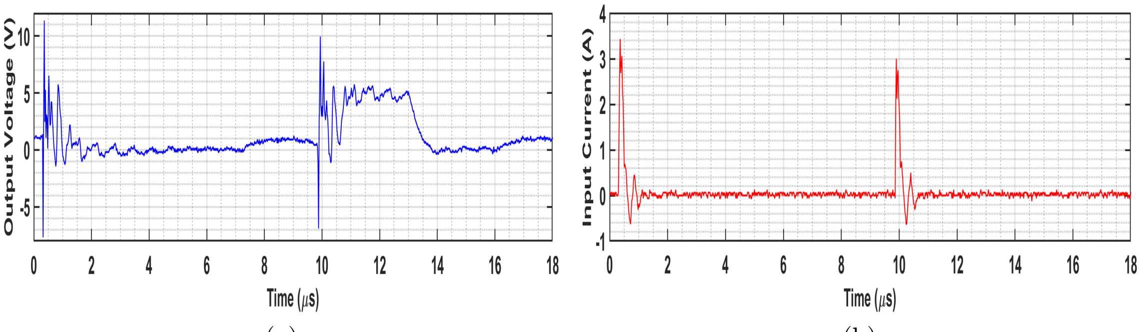
5.3.4 EFT Failure Modes for Oscillators

The operating frequency of an oscillator is typically used to evaluate its susceptibility to continuous wave EM disturbances and can also be considered to characterize its transient immunity. For this case study, the failure criterion is a ±10% deviation from the nominal output frequencies of the multi-stage CSVCO and RO at ambient and extreme temperatures. EFT failure modes, previously defined in [125] for μCs, are redefined here to evaluate the EFT immunity of the integrated oscillators. The apparent failure types classified from A to E are the following:

- **A-type**: no failure occurs, and the frequency of the oscillator remains within the defined tolerance limit.
- **B-type**: the oscillator's frequency exceeds the tolerance limit but self-recovers to its nominal frequency as soon as EFT is removed.
- **C-type**: this soft failure usually occurs in microcontrollers when the state machine crashes into an unknown state due to EFT disturbance and can only be recovered by an external reset of the core. This type of failure is not applicable for purely analog devices such as oscillators.
- **D-type**: the oscillator's frequency goes beyond the tolerance limit and only recovers to its nominal frequency after EFT is removed and power cycling is performed.
- **E-type**: the oscillator's frequency crosses the tolerance limit and never recovers to its original frequency even with power cycling.

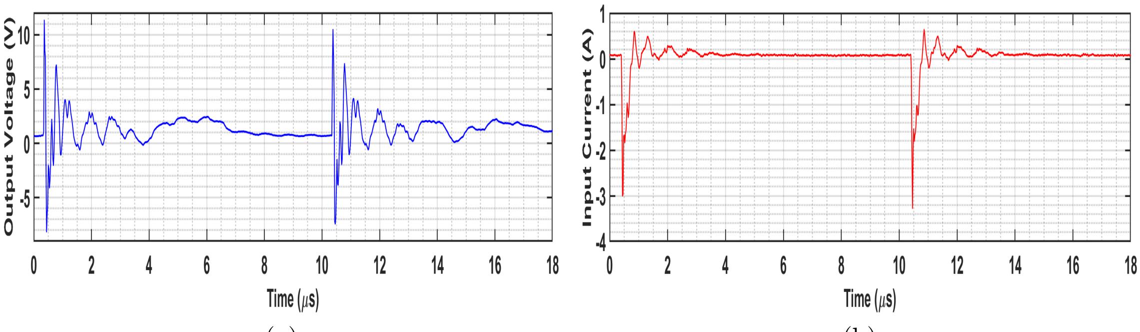
5.3.5 EFT Immunity Analysis: Packaged vs. COB

This section deals with the comparison of measured EFT immunities of multi-stage CSVCOs and RO with and without the IC package at nominal temperature. The positive and negative polarity EFT voltages were ramped from 250 V to 2 kV and −250 V to −2 kV in 20 V steps, respectively. A dwell time of 15 s was given at each EFT level in order to acquire the output voltage and input current of each oscillator at ambient temperature. The test was terminated when an E-type failure occurred and the oscillator was permanently damaged. Due to the use of isolated power



(a) (b)

Figure 5.15: Measured output voltage (a) and input current (b) for the 5-stage CSVCO at EFT = 600 V © [126].



(a) (b)

Figure 5.16: Measured output voltage (a) and input current (b) for the 5-stage CSVCO at EFT = −600 V © [126].

supplies, an E-type failure only damaged the supply pad of the tested oscillator, leaving the other supply oscillator pads unaffected. Additionally, A-type failures were never observed in any case, since even at the minimum applied EFT voltage (250 V or −250 V), all oscillators were operating beyond the tolerance limits. Hence, most cases resulted in B-type failures. All EFT immunity level measurements were reproducible with other samples.

To start with, positive polarity EFT disturbances were applied to packaged and COB versions of the oscillators at 25 °C. As an example, the output response and the injected EFT current for the 5-stage CSVCO are displayed in Fig. 5.15.a and 5.15.b, respectively. The response is shown for a 18 μs duration displaying two consecutive peaks of EFT injection (600 V). It should be noted that the steady-state oscillating output voltage of the 5-stage CSVCO was found to have a peak-to-peak voltage, DC-offset, and frequency of 232 mV, 1.17 V, and 66.1 MHz, respectively. It was observed that since the pulse width of each EFT spike was only 50 ns, the ESD protections were triggered after some delay, allowing the EFT voltage to be re-injected to the output. The latch-up effect of the ESD structures can be seen between the two consecutive EFT spikes, limiting the output voltage between 0 and 5.5 V and eventually stabilizing. That effect had a random final output level (clamped to either 0 or 5.5 V) for each EFT injection (75 peaks in each burst) and showed a damped oscillation due to the resonance between the output pad capacitance and the bonding/package parasitics. As expected, it can be noticed that the pseudo period of that oscillation is higher for the packaged version in comparison to the COB, due to the added package inductance. In case of the injected EFT input current, all waveforms were repeatable.

Similarly, a negative polarity EFT voltage of −600 V was injected into the V_{DDI} pin of the 5-stage CSVCO while operating in steady state. The output response and the injected EFT current of the latter are shown in Fig. 5.16.a and 5.16.b, respectively. The output voltage response was comparable to the positive polarity EFT test, since the V_{DDI} pad includes identical N-MOS based ESD protections to both the supply rail and ground. The latch-up effect of the ESD structures remains entirely random and the output voltage eventually stabilizes. The observed input current was inverted, with its absolute peak-to-peak value similar to that of the positive polarity EFT current.

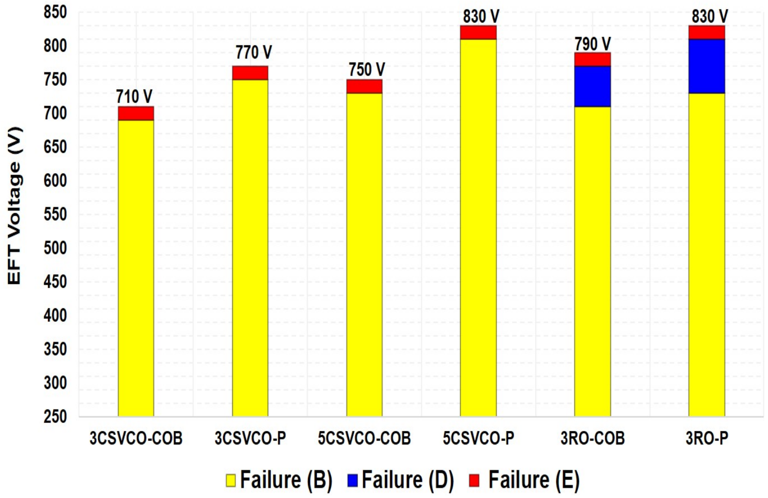
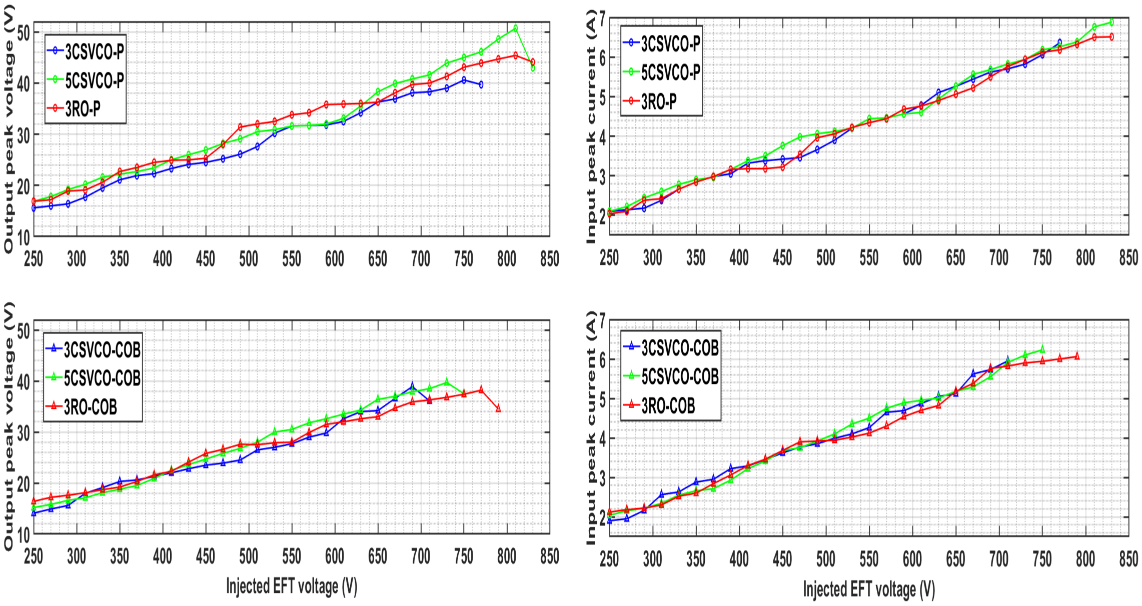


Figure 5.17: Positive polarity EFT immunity of multistage CSVCO and RO at ambient temperature: packaged vs. COB © [126].

Fig. 5.17 shows the positive EFT immunity levels, with their specific failure modes, of all tested oscillators for packaged and COB ICs at ambient temperature. When comparing the packaged 3- and 5-stage CSVCOs, the latter was found to be more immune with an E-type failure detected at 830 V. In both CSVCOs, the output was able to self recover before eventually being damaged at their maximum bearable EFT voltage. Contrarily, in the packaged 3-stage RO, D-type failure started to occur at 730 V, before eventually turning to E-type at 830 V. The EFT immunity level of the 3-stage RO was found to be higher compared to the 3-stage CSVCO.

When analyzing the positive EFT immunity levels for the tested COB oscillators, all levels were reduced compared to the packaged ones. This was due to the package parasitics attenuating the injected EFT voltage and current going into the V_{DDI} pad of each oscillator. Moreover, the behavior of the oscillators to EFT and their respective failure modes were unaffected by the package. The 5-stage CSVCO was still more immune (750 V) than the 3-stage CSVCO (710 V). D-type was observed (similar to the packaged version) only for the RO at 670 V, ultimately becoming E-type at 790 V. The D-type failure effects in the RO for both packaged and COB may be due to the FD circuit being sensitive to EFT at its input above its maximum clock frequency (900 MHz) and locking up in a stable state, thus resulting in re-injection of the EFT voltage to the global power supply which was observed in simulations and measurements. Similarly to the packaged version, the 3-stage CSVCO EFT immunity was lower than the RO.

The output peak voltage and input peak current of each oscillator (packaged and COB) were further analyzed and are shown in Fig. 5.18.a and 5.18.b, respectively. As it can be observed in Fig. 5.18.a the output peak voltage increases with the rise in EFT voltage in all the considered cases. Conversely, a drop in the output peak voltage can be observed when an E-type failure occurs. The output peak voltages for increasing EFT injected voltage were greater for the packaged IC than for the COB. The highest output peak voltage was observed for the 5-stage CSVCO, close to its maximum EFT immunity level, for both packaged (51.2 V) and COB (40.3 V) cases. As indicated in Fig. 5.18.b, the injected input current was also proportional to the increase in the applied EFT voltage for all tests at 25 °C. Similarly to the output voltage, the input peak currents for the packaged oscillators were slightly higher than the COB. Moreover, the largest peak input current was noted for the 5-stage CSVCO, near its maximum EFT immunity level for both with (6.9 A) and



(a) (b)

Figure 5.18: Effect of EFT disturbances on multi-stage CSVCO and RO (packaged vs. COB) at ambient temperature © [126]: (a) output peak voltage; (b) input peak current.

without (6.1 A) the package. Thus, the 5-stage CSVCO can withstand more injected EFT peak current than the remaining oscillators.

5.3.6 EFT Immunity Analysis at Extreme Temperatures

In this section, the positive and negative polarity EFT immunity of all the packaged oscillators are characterized including the effect of temperature variation. The positive polarity EFT immunity levels of the packaged oscillators at extreme temperatures are displayed in Fig. 5.19. It was found that the immunity levels of all oscillators had reduced at 120 °C and improved at −40 °C, compared to the ambient temperature. Since all integrated oscillators have the same ESD protection devices, the temperature variation is affecting the performance of the latter. The temperature increase during the EFT stress reduces the ESD devices' protection capability, triggering current and holding voltages, hence reducing the overall transient immunity levels of each oscillator.

When comparing the 3- and 5-stage CSVCOs, the former had a better EFT immunity at −40 °C (1.1 kV) and at 120 °C (710 V). Even though the output

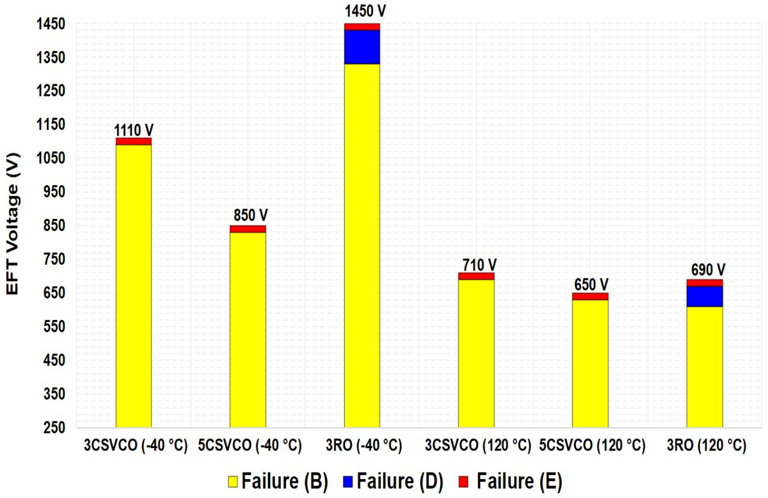
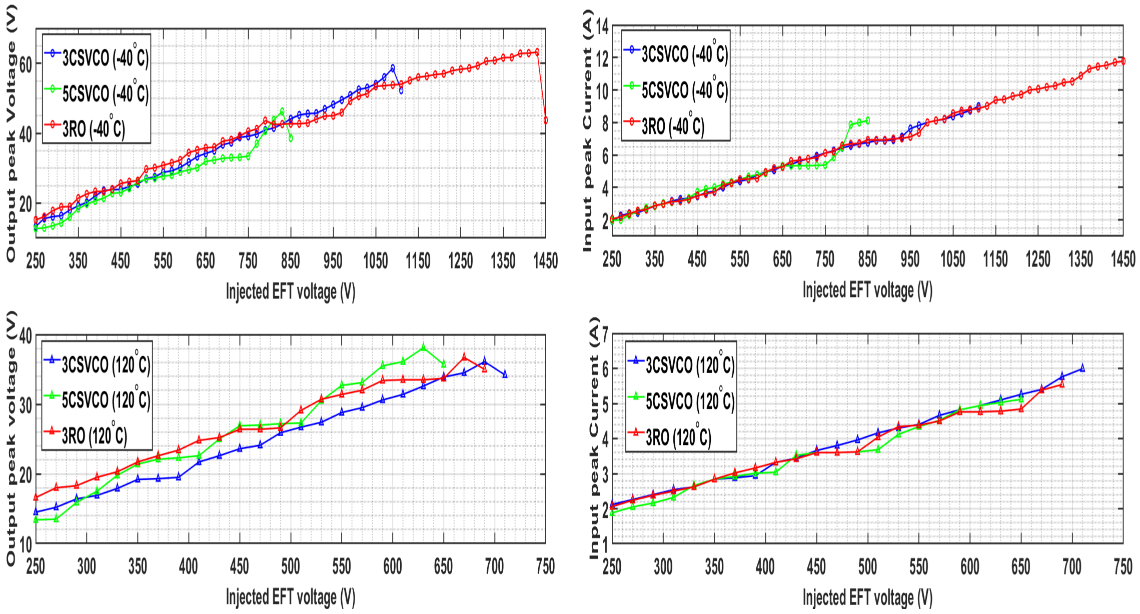


Figure 5.19: Positive polarity EFT immunity of multi-stage CSVCO and RO (packaged) at extreme temperatures © [126].

frequency of the 5-stage CSVCO was found to be more resilient to temperature variations, its immunity to EFT disturbances was reduced at higher temperatures. This could be due to the reduction of the V_{th} levels of the higher number of biasing transistors due to temperature, resulting in lower levels of EFT immunity. The RO was found to be the most immune at −40 °C, compared to all other oscillators, with D-type failure occurring from 1.33 kV and E-type failure at 1.45 kV. The FD circuit plays a vital role in the case of the RO (operating frequency greater than 900 MHz), as lowering the temperature improved the performance of the FD and switched the output frequency to its expected value. When comparing the 3-stage CSVCO and RO at 120 °C, the latter's immunity was slightly lower (610 V (D) and 690 V (E)). The reason behind this is that the FD circuit is unable to function properly at elevated temperatures for the RO. Temperature variations did not influence the type of failure modes, and the D-type failure was still only noticed for the RO, due to the FD circuit.

The output peak voltage and input peak current of each oscillator at extreme temperatures were also examined and are given in Fig. 5.20.a and 5.20.b, respectively. Similarly to the results obtained at ambient temperature, the output peak voltage drops for all oscillators in the case of an E-type failure (Fig. 5.20.a). The output peak voltages for increasing EFT injected voltage at −40 °C were substantially greater than at 120 °C for all oscillators. The maximal output peak voltages at



(a)

(b)

Figure 5.20: Effect of EFT disturbances on multi-stage CSVCO and RO (packaged) at extreme temperatures © [126]: (a) output peak voltage; (b) input peak current.

−40 °C and 120 °C were obtained for the 3-stage RO (64.7 V) and 5-stage CSVCO (37.8 V), respectively. As observed in Fig. 5.20.b, the injected EFT input current was also reduced at elevated temperatures. At the lowest temperature, the largest EFT peak input current was noted for the 3-stage RO (12 A). However, at the maximum temperature, the highest peak input current was measured for the 3-stage CSVCO (5.9 A). Consequently, the 3-stages RO and CSVCO can withstand more injected EFT peak current than the 5-stage CSVCO at −40 °C and 120 °C, respectively.

The negative polarity EFT immunity levels of the packaged oscillators at nominal and extreme temperatures are illustrated in Fig. 5.21. As expected, the absolute EFT immunity levels were comparable with the positive polarity test (Fig. 5.19) and the overall trend with respect to thermal stress remained the same for all packaged tested oscillators. This is due to the padring having identical ESD protection structures to both the supply rail and ground. Furthermore, changing the polarity did not have an impact on the EFT failure modes, as a D-type failure was still observed only for the 3-stage RO instigated by the FD circuit.

To physically demonstrate the destructive effect of EFT disturbances at the package and die level, a few images of the tested ICs were captured using a high

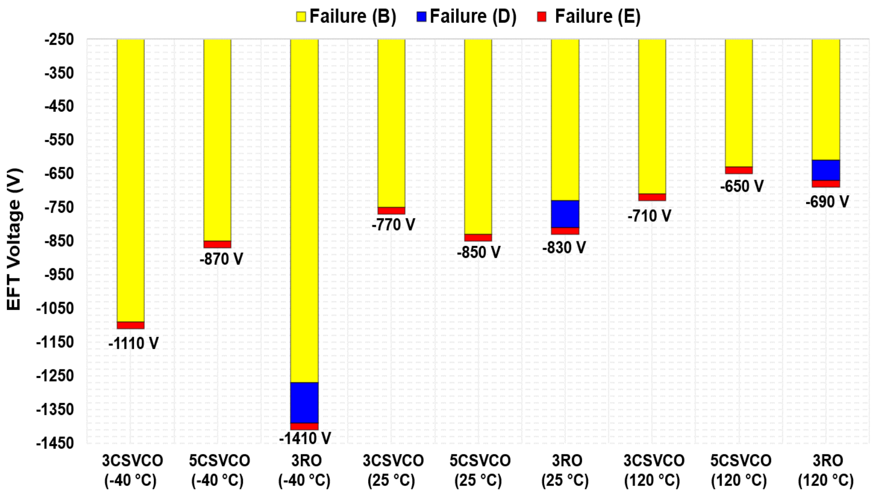


Figure 5.21: Negative polarity EFT immunity of multi-stage CSVCO and RO (packaged) at nominal and extreme temperatures © [126].

resolution microscope (Leica MZ125). As an example, Fig. 5.22.a and 5.22.b show the packaged IC subjected to EFT at −40 °C at the bonding and die level, respectively. It can be noticed in Fig. 5.22.a that two bonding wires, that were previously connected to the 3-stage CSVCO and RO voltage supply pads, were burnt. Both wires were damaged due to the overvoltage caused by the EFT disturbances, in this case being greater than 1.1 kV. However, only the voltage supply bondpad of the 3-stage RO was entirely destroyed (Fig. 5.22.b). Therefore, the maximum EFT voltage that the ESD devices in the supply pads could handle was found to be 1.45 kV. At ambient (25 °C) and elevated (120 °C) temperatures the highest EFT immunity levels for all oscillators were 830 V and 710 V, respectively. These EFT levels were considerably lower than 1.45 kV and none of the ICs' ESD bond pads or wires were destroyed. The root cause of failure was found to be from within IC itself, which will be discussed in the upcoming section.

5.3.7 Frequency Response due to EFT Injection Under Thermal Stress

The simulation setup previously introduced in Section 5.3.2 was used to determine the frequency behavior of the considered oscillators before and after the FD circuit when subjected to EFT at nominal and extreme temperatures. The transient sim-

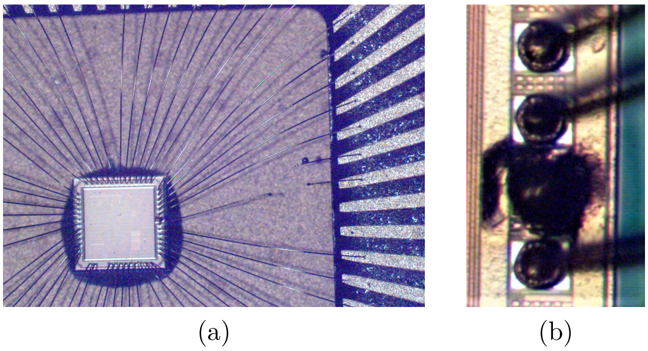
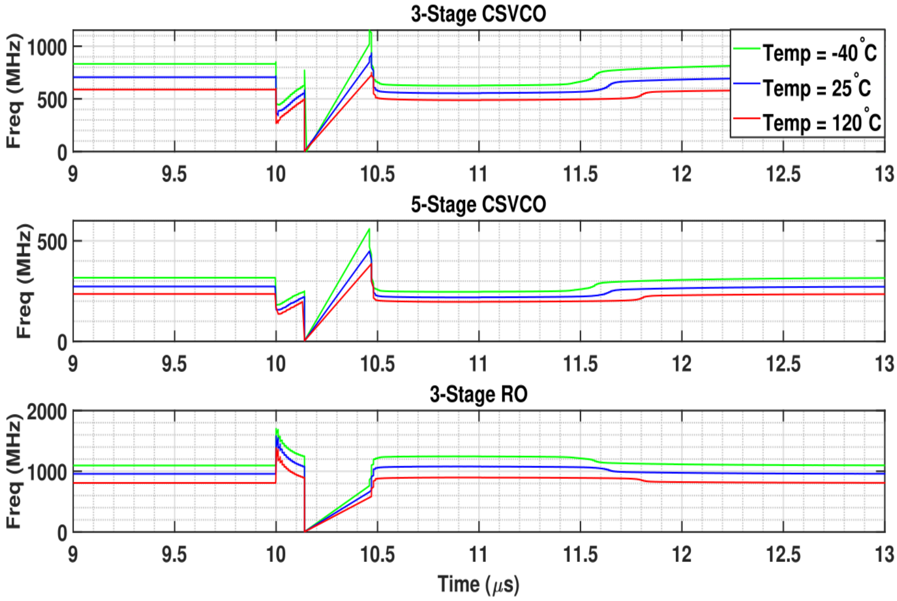

(a) (b)

Figure 5.22: Images of the damaged IC due to EFT disturbances at −40 °C © [126]: (a) bonding wire; (b) bond pad.

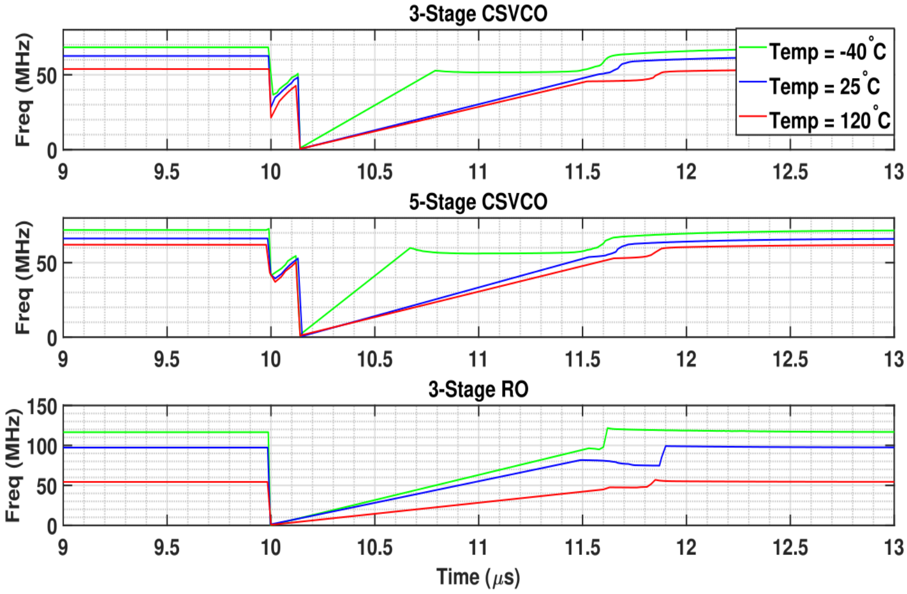
ulations were recorded for a time-period of 13 μs in order to monitor the oscillator frequency deviation due to one EFT spike. It was verified that the EFT disturbance (600 V) was injected when all tested oscillators' output signals were in-phase (rising edge) at 10 μs whatever the temperature, in order to draw a sensible comparison among all transient effects (Fig. 5.23.a and 5.23.b). The Cadence SKILL mode function, which takes the fast Fourier transform in discrete time-steps (1.5 ns) over the steady-state period (13 μs), was applied to measure the operating and output frequency of the oscillators.

As illustrated in Fig. 5.23.a, excluding the effect of the FD and output pad, an identical frequency response to EFT injection was observed for the considered multi-stage CSVCOs. However, the 3-stage RO exhibited a distinct operating frequency behavior, which is likely to be due to the topologies of the CSVCO and RO. At 10 μs, when the EFT disturbance is injected into the supply V_{DDI} pad, the ESD structures are triggered after 100 ns, clamping the EFT voltage to 0 V. Before that clamping, the increase in supply voltage reduces the propagation time of the RO's inverter stages, thus momentarily increasing its frequency. Conversely, for the CSVCOs, the EFT spike is capacitively coupled to the gate of the PMOS biasing transistors, resulting in a reduction of the bias current, which in turn increases the propagation delay and reduces the output frequency. Both phenomena tend to stabilize before the ESD structures are triggered.

After 100 ns, when all the oscillators start recovering to their nominal frequency, the CSVCO has a faster slew rate compared to the RO (Fig. 5.23.a). However, unlike the RO where it smoothly stabilizes to its nominal frequency, the CSVCO frequency



(a)



(b)

Figure 5.23: Frequency variation of multi-stage CSVCO and RO (packaged) at extreme temperatures before (a) and after (b) the FD circuit when an EFT voltage of 600 V is applied © [126].

sharply increases and then falls down due to the discharge of the parasitic gate-source capacitances of the CSVCO's PMOS bias transistors (verified in simulations). Moreover, it was observed that with the rise in temperature, the time to recover after the EFT injection gradually increased for all oscillators due to the higher peak voltages. For a better understanding of the measured results, the frequency response of all tested oscillators, including the effect of the FD, output pad and package, was further analyzed in simulations (Fig. 5.23.b). At 10 μs, when the EFT disturbance is injected, the CSVCOs exhibit similar behavior to the case before the FD, where the output frequency momentarily reduces before being clamped to ground by the ESD structures.

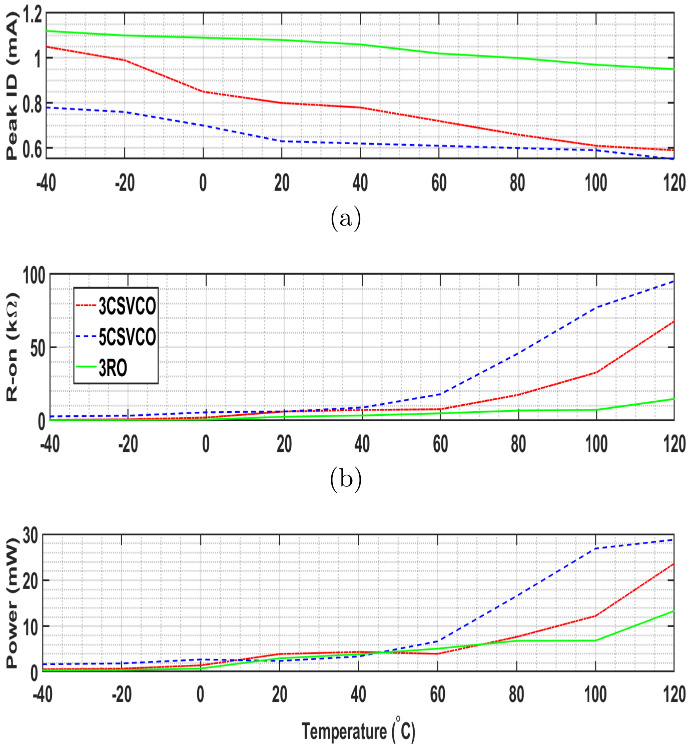
After 100 ns, compared to the former case, the frequency tends to stabilize but with a reduced slew rate due to the added effect of the FD. The latter also explains the difference in the simulated slew rate at extreme temperatures. Conversely, in the case of the RO, once the EFT is applied, the output frequency abruptly drops to 0 Hz. The latter is attributed to the fact that the RO is operating (955 MHz) above the maximum clock frequency of the FD (900 MHz) and a further increase in the RO frequency results in the FD circuit crashing at 10 μs. It gradually tries to recover to its nominal output frequency but with a lower slew rate compared to the CSVCOs, which is due to the higher propagation delay caused by the FD circuit. Similar to the CSVCO, the slew rate is observed to be inversely proportional to temperature.

To sum up, temperature variations do not impose any change in the transient latch-up mechanism of the ESD structures, which explains the unchanged behavior in the output frequency curves for all oscillators before the FD. A rise in temperature only accounts for the decrease in the nominal operating frequency (Fig. 5.23.a) and a reduction in the slew rate of the output frequency (Fig. 5.23.b) for all tested oscillators. The simulated operating frequency deviations from the nominal frequency for the 3- and 5-stage CSVCO and 3-stage RO (before the FD) at extreme temperatures are +15.1%, +14.3%, +15.6% (at −40 °C), and −16.7%, −13.2%, −17.4% (at 120 °C), respectively. The output frequency deviations (after the FD) at extreme temperatures are in line to those obtained in measurements (Section II-B), with the 3-stage RO showing the highest deviation due to the added effect of the FD circuit. Consequently, the 5-stage CSVCO was found to be the most resilient to temperature variations compared to the other two oscillators mainly due to the reason previously explained in the last paragraph of Section II-B. However, the 5-stage CSVCO was the most susceptible to the combined effect of temperature and EFT injection. The latter and the root cause of failure were verified through transistor-level simulations and reported in the upcoming section.

5.3.8 Failure Analysis due to Combined EFT and Thermal Stress

To investigate the root cause of the EFT susceptibility of the oscillators at extreme temperatures, a transient simulation was carried out for the EFT disturbance (600 V) peak (dwell time of 50 ns) by varying the temperature from -40 °C to 120 °C with a 20 °C step size. Relevant MOSFET characteristics such as peak drain current, on-state drain-to-source resistance and power dissipation were calculated at the output stage (before the FD circuit) of the considered oscillators as a function of temperature (Fig. 5.24). As observed in Fig. 5.24.a, the peak drain current in the inverter output stage reduces with the increase in temperature for all the tested oscillators even when subjected to EFT disturbance. This is due to the μ_{eff} of the MOSFETs being inversely proportional to temperature. The multi-stage CSVCOs have a lower drain current than the RO since the biasing MOSFETs limits the current to the inverter stage. When comparing the 3- and 5-stage CSVCOs, the former has higher peak drain current because of different external biasing voltages. It is noted that the 3-stage RO's peak drain current is more resilient to changes in temperature in comparison to the multi-stage CSVCOs. A reasonable explanation for this observation can be found by analyzing the on-state drain-to-source resistance of the output stage (Fig. 5.24.b).

Temperature variation and transient electrical overstress such as EFT cause the on-state resistance of the MOSFETs in the inverter stage of oscillators to substantially increase. The on-state resistance rises due to the reduction in μ_{eff} and V_{th} with the combined effect of temperature and EFT. These changes cause the switching characteristics of the oscillator to change, resulting in higher power dissipation and causing premature failure [155]. When the EFT disturbance is injected into the V_{DDI} of each oscillator, a transient path is created between V_{DDI} and G_{NDI}. Hence, the total on-state resistance of each oscillator is calculated by the summation of the individual on-state resistance of each P-MOS and N-MOS in the output branch with temperature variations. As illustrated in Fig. 5.24.b, the on-state resistance of the multi-stage CSVCOs is greater than the RO due to the added resistance of the biasing MOSFETs. For the former, the total on-state resistance abruptly rises above



(a)

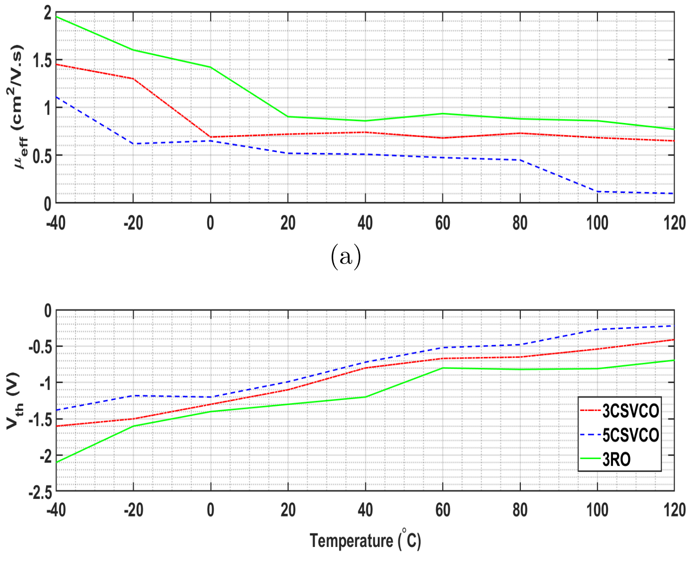
(b)

(c)

Figure 5.24: Dependency of the relevant MOSFET characteristics of multi-stage CSVCO and RO (packaged) as a function of temperature for an EFT applied voltage of 600 V © [126]: (a) peak drain current; (b) on-state resistance; (c) power dissipation.

60 °C. When comparing the 3- and 5-stage CSVCOs, the latter has an elevated resistance over the entire temperature range, which is due to the combined effect of lower μ_{eff} and V_{th}, elevating the on-state resistance when EFT is applied. In contrast, the 3-stage RO has a lower variation in the on-state resistance to temperature and EFT stress.

All the analyzed characteristics are directly influenced by the decrease of the μ_{eff} and V_{th} levels of the MOSFETs due to rise in temperature and EFT stress. For example, the behavior of these characteristics for a P-MOS in the inverter output stage as a function of temperature for all tested oscillators is illustrated in Fig. 5.25.a and 5.25.b, respectively. The μ_{eff} of the 5-stage CSVCO was found to be the least resilient to the combined effect of temperature and EFT; it drops sharply for temperatures above 80 °C. In comparison, the 3-stage CSVCO and RO have limited reduction in μ_{eff}. Moreover, the absolute V_{th} levels of the 5-stage CSVCO are also lower than the other oscillators over the entire temperature range. The root



(a)

(b)

Figure 5.25: P-MOS relevant characteristics in the inverter output stage of multi-stage CSVCO and RO (packaged) as a function of temperature for an EFT applied voltage of 600 V © [126]: (a) μ_{eff}; (b) V$_{th}$.

cause for the lowest EFT immunity of the 5-stage CSVCO is the increase on-state resistance due to the above-mentioned factors.

The power dissipated at the output stage of all oscillators is derived from the peak drain current and the on-state resistance. As displayed in Fig. 5.24.c, the power dissipation follows a similar trend and is influenced more by the on-state resistance and increases at elevated temperatures for all oscillators. The maximum power dissipation is observed at 120 °C for the 3-stage (23 mW), 5-stage (29 mW) CSVCO and 3-stage RO (14 mW). It is important to note that when the EFT is applied at nominal temperature, the 5-stage CSVCO has a reduced power dissipation (2.4 mW) compared to the 3-stage CSVCO (3.9 mW) and the 3-stage RO (3.1 mW). Although the self-heating phenomenon due to that power dissipation is not taken into account by the simulator, that may explain why E-type failures can be observed in measurements due to thermal runaway.

To verify the assertion that the integrated oscillators do not exhibit abnormal behavior at elevated temperatures, the power dissipation of the output stage was monitored with change in temperature (-40 °C to 120 °C with a 20 °C step size) without applying EFT stress. As shown in Fig. 5.26, with rise in temperature the output power dissipation decreased for all integrated oscillators. This is due

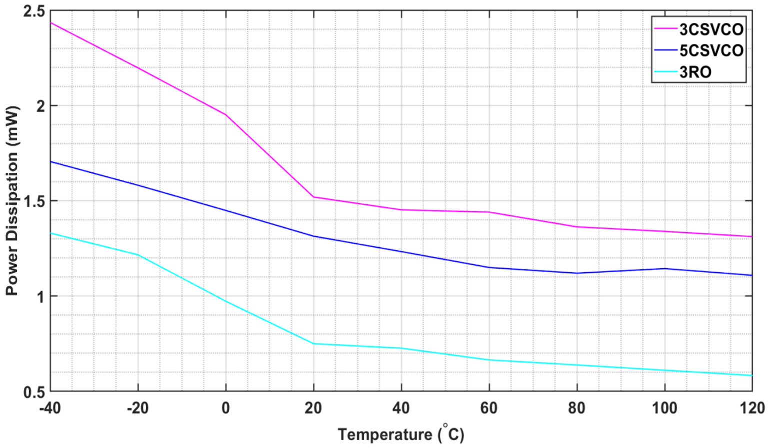


Figure 5.26: Dependence of output power dissipation on temperature of tested integrated oscillators.

to the drain currents being inversely proportional to temperature and the on-state resistance does not vary considerably. The 3-stage RO has lower power dissipation compared to the other oscillators. No anomaly or abnormal behavior was observed at extreme temperatures, verifying that the combined effect of EFT and temperature caused thermal runaway.

5.4 Conclusion

In this chapter two independent case studies on the EFT immunities of μCs (having different cores, but pin-compatible) and integrated oscillators (having diffrent topologies but same ESD protection devices) were carried out. For the case study 1, related to the μCs, results show that, except for the V_{DDPLL} pin, SAM3 (newer version) had higher EFT immunity compared to SAM7 (older version) on all the considered supply pins. Since, not all pins were immune to EFT for SAM3, further study is required (such as IC modeling) to predict the transient EM immunity of each μC.

In case study 2, the transient immunity of three multi-stage SOI integrated oscillators, i.e., CSVCO and RO, having the same ESD protection structures, was assessed under EFT and temperature. By considering output frequency as the failure criterion, EFT failure modes were proposed for such oscillators. Depending on oscillator topology, distinct failure modes were observed. The failure modes defined for digital μCs were extended to purely analog devices to characterize the EFT immunity of the osicllators. Moreover, the analysis revealed the importance of the package on the EFT immunity levels of all the tested oscillators, due to the attenuation of the injected EFT peak voltage.

Transistor level simulations were also conducted to accurately monitor the output frequency response of each oscillator to EFT injection under thermal stress, with and without the effect of the FD, the analog output pad and the package. A distinct behavior in oscillator frequency was observed for the same in-phase EFT injections depending on the topology of the circuit. The positive and negative polarity EFT immunity levels for all tested oscillators were found to be similar since the IC's padring includes the same ESD protection circuits to the supply and ground. The rise in temperature was demonstrated to reduce the absolute EFT immunity levels for all the tested oscillators by affecting the protection capability of the ESD devices.

The 5-stage CSVCO was found to be the most susceptible to EFT at extreme temperatures (-40 °C and 120 °C). Conversely, at the minimum and maximum temperatures, the 3-stage RO and CSVCO were shown to be the most immune to EFT, respectively. The temperature variation under the EFT stress resulted in no impact on the type of failure modes. The output inverter stage MOSFET characteristics such as drain currents, on-state drain-to-source resistance, power dissipation, μ_{eff} and V_{th} were extensively analyzed while varying temperature and EFT stress. It was found that the on-state resistance of the MOSFETs varies considerably when EFT stress and temperature variations are combined, which could cause thermal runaway and substantially reduce the EFT immunity, in particular for integrated oscillators with greater number of stages.

Chapter 6

CONDUCTED EM EMISSION & IMMUNITY ANALYSIS WITH AGING AND THERMAL STRESS

The results related to the this entire Chapter 6 about conducted EM emission and immunity analysis under the influence of aging and temperature are published by the author in [156].

6.1 Introduction to ICEM-CE & ICIM-CI Models

A vital factor in the design process of ICs is estimating if their functionality and EMC characteristics can be guaranteed over their entire lifetime. In that context, both EM emission and immunity of ICs are critical for reducing interference risks at the system level, where several mitigation techniques to lower emission and susceptibility of PCBs are reported in literature [157]. Further, it is necessary to analyze and predict the EMC of ICs in harsh environments (e.g. extreme temperatures, humidity, and electrical overstress) before the manufacturing stage [158].

The IEC has proposed several models to assess the EMC performances of ICs, such as the IC emission model for conducted emission (ICEM-CE) and the IC immunity model for conducted immunity (ICIM-CI), which are published in IEC62433-2 [9] and IEC62433-4 [8], respectively. Those models can be generated either through a black box or a white box approach. The former does not require the knowledge of the internal structure of the IC, while the latter approach provides the models in a simulatable form [159]. As shown in Fig. 6.1.a, the ICEM-CE model consists of a passive block called the passive distribution network (PDN) and an active block

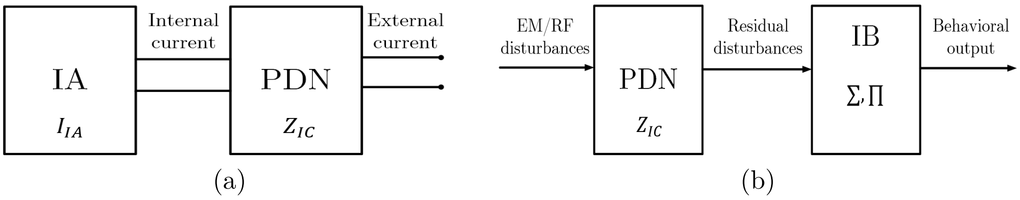


Figure 6.1: Modeling framework of © [156]: (a) ICEM-CE; (b) ICIM-CI.

known as the internal activity (IA). The former describes the power supply network of an IC and shows the significant coupling paths from the noise source to the external pins of the IC, whereas the IA describes the activity of the internal block of the IC as a current source.

As observed in Fig. 6.1.b, the PDN of the ICIM-CI model is similar to that of the ICEM-CE and can be modeled using lumped passive elements. Additionally, the immunity model also comprises the immunity behavior (IB) block which is usually characterized as a look-up table that can be coupled to a comparator to output a pass/fail criterion based on the injected power [160]. The main limitations of these models are that they do not include the relevance of aging and thermal stress that can cause a drift in the EM conducted emission and susceptibility levels.

Due to natural aging, ICs can be affected by intrinsic failure mechanisms, such as gate oxide defect, electromigration, hot carrier injection (HCI) and negative bias temperature instability (NBTI) [161]–[163]. The latter two are the most prevalent permanent degradation effects and can be analyzed by accelerated life tests [164]. Furthermore, temperature variations can temporarily influence MOSFET parameters such as V_{th} levels, μ_{eff}, transconductance, and saturation currents [64]. These can trigger soft failures and can have significant impact on the stability parameters (leakage current, noise margin, jitter, operating frequency etc.) of the IC [165].

In comparative literature, researchers have developed conducted emission models using de-embedding measurement techniques [166] and simulation tools [167] for microcontrollers [168] and PLLs [169]. Few researchers have also introduced an alternative approach to model the IA block for oscillators [170]. In addition, some works have been carried out to develop ICEM models up to 3 GHz and the impact of high temperature on the emission levels has been analyzed [171], [172]. The effect of aging on the conducted emission of switches were studied in [11] and reliability models for FPGAs were developed in [173] and [174] to predict failures over their entire life cycle. As far as immunity is concerned, some researchers developed multi-port models to extract the conducted immunity profiles of analog circuits such as operational amplifiers [175]–[177]. The ICIM-CI model has also been extended to include the effect of transient EM disturbances [138]. Moreover, conducted immunity models were proposed to predict the long-term immunity of PLLs using accelerated life tests [10]. A recent study proposed an EM-thermal model to characterize the conducted immunity of an input/output element for FPGAs [178].

To the best of the author's knowledge, the influence of highly accelerated aging and thermal stress on the conducted emission and immunity models, has not been investigated so far. Therefore, in the current study, the ICIM-CI and ICEM-CE models were developed for independent analog circuits that were integrated into a custom-designed IC. Through measurements and transistor level simulations, the effect of extreme temperature deviations and highly accelerated aging were included into either the passive or active blocks of the proposed models.

The analog circuits included in the PETER_ESEO research chip [106] were used to analyze the influence of temperature and aging on conducted emission and immunity levels. All structures have an isolated power supply pad (V_{DDI}) and a separate ground (G_{NDI}), due to the use of SOI technology. The die samples were packaged in a 64-pin CQFP. All power supply and ground pads were bonded to the package pins with spacing in between them to minimize the effect of mutual inductive coupling. More details on the design of the PETER_ESEO die used in this case study can be found in Chapter 2 of this manuscript.

To test the conducted emission and immunity of the IC, a PCB variant, was designed according to IEC 61967-4 [179] and IEC 62132-4 [4]. All isolated grounds of the IC were connected to the global ground. Specifically, for the circuits tested for immunity, a 470 Ω resistor was added in series to its output pin in order to limit high voltage signals from being re-injected into the oscilloscope. Only for the conducted emission circuit, the G_{NDI} pin was connected to 49 Ω and 1 Ω resistors in compliance with the $1-\Omega$ method of IEC 61967-4 [179]. In addition, a PCB variant along with its calibration board were designed to accurately measure the S-parameters of the IC pins. The calibration technique adopted was the SOLT method, generally providing an accuracy of up to 4 GHz [54]. More details on the design of all PCBs are mentioned in Chapter 2 of this manuscript.

To investigate conducted EM emission at IC level, a H-clock tree noise circuit and S&H voltage senor were used (integrated in the PETER_ESEO die). When a clock signal is provided to the input (A_{in}) of the *H*-clock tree, it generates high frequency conducted EM disturbances, specifically in its power supply (V_{DDI1}) and ground G_{NDI1} rails. As illustrated in Fig 6.2, the V_{DDI1} of the *H*-clock tree noise circuit was connected to the analog input of the S&H voltage sensor. The latter was able characterize these coupled EM emissions by transposing them to much lower frequencies [180]. When a square signal with a constant frequency was injected into the input of the *H*-clock tree, the switching activity of the buffers produces conducted noise which propagates to its V_{DDI} or G_{NDI}. Conducted emission measurements were carried out using the 1 Ω probe [179] placed at the G_{NDI} pin of the *H*-clock tree. Furthermore, the *S&H* output peak voltage is directly proportional to the conducted emission generated in the V_{DDI}. The The V_{DDI2} and G_{NDI2} of the voltage sensor were entirely isolated from the conducted noise and was verified to have no impact on the conducted emission analysis. More over the voltage sensor was operated in random sampling mode.

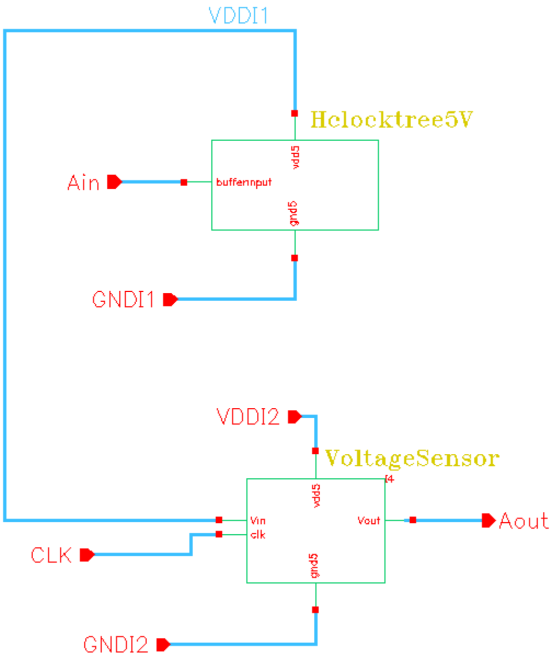


Figure 6.2: Combined schematic of *H*-clock tree and S&H voltage sensor utilized for EM conducted emission analysis © [156].

To analyze the conducted EM immunity, two independent analog blocks integrated into the IC were selected. Those are a 3-stage CSVCO including a FD circuit at the output stage and an analog (S-R) latch. The former is an integral part of mixed-signal ICs such as PLLs, and the latter is utilized in sequential memory circuits. The power supply of the mentioned structures are prone to conducted EMI, which affects their performance characteristics. Both circuits have separated V_{DDI} and G_{NDI} rails to avoid any interference or coupling during immunity testing. Design details and schematics/layouts of all conducted immunity (CSVCO, (S-R) latch) and emission (H-clock tree, S&H voltage sensor) blocks are explained in Chapter 2 of this manuscript.

6.2 IC Aging due to HAST

To investigate the impact of aging on the emission and immunity behavior of ICs, accelerated life tests are usually performed in industry. High-level stress conditions such as extreme high temperature or voltage, are applied for a short period of time to accelerate the damage rate for relevant wear-out failure mechanisms such as NBTI and HCI [181]. The most frequently used accelerated tests to induce such degradation mechanisms are high and low temperature operating life tests (HTOL and LTOL) [182], and temperature humidity bias test (THB) [183]. The latter is a method of electronic reliability testing using temperature and relative humidity (RH) as the environmental parameters. The test is carried out at 85 °C and 85% RH continuously for 1000 hours to predict the operational lifetime of the device up to 25 years.

The highly accelerated temperature and humidity stress test (HAST) is a more accelerated version of the THB test (causing equivalent failure modes) and is performed at 130 °C and 85% RH continuously for only 96 hours [184]. The purpose of HAST is to evaluate the humidity resilience of a component or an encapsulated IC by increasing the water vapor pressure to an extremely high level above the partial water vapour pressure inside the IC. Hence, this test causes a rise in component contact resistance due to moisture corrosion and insulation deterioration.

HAST was selected herein as the accelerated life test to evaluate the effect of aging on the conducted emission and immunity of the PETER_ESEO IC. As illustrated in Fig. 6.3, the immunity/emission and S-parameter PCB variants along with several packaged ICs were placed in a HAST chamber (ESPEC EHS-412M) at a constant 130 °C temperature and 85% RH for 96 hours. For the entire duration

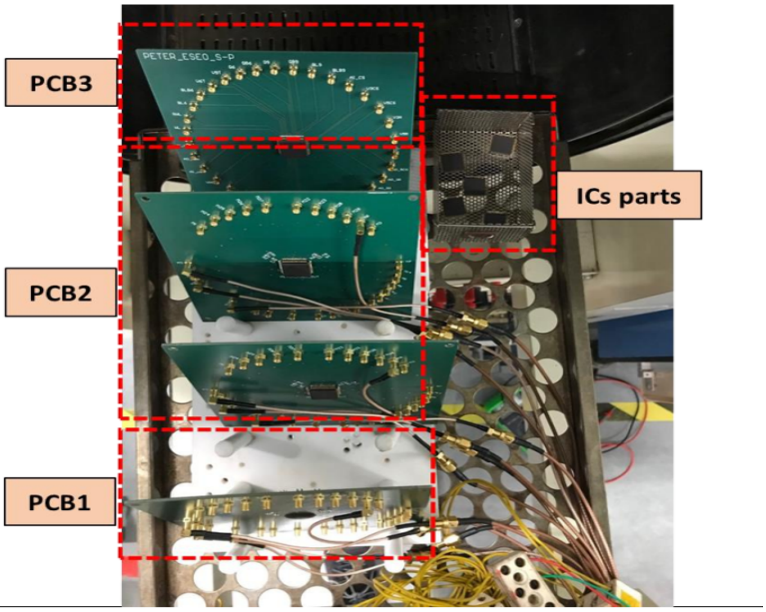


Figure 6.3: Aging of ICs in HAST chamber © [156].

of the test, the global power supply and the isolated supplies of the *H*-clock tree, S&H voltage sensor, *S*-*R* latch and the CSVCO circuits in the IC were biased to 5 V using external DC power supplies through high temperature cables. To isolate the impact of aging only on the test chip itself, several (10 samples) unbiased ICs were also aged in the HAST chamber. At the end of the test, all PCBs and ICs were still operational with no visible damages. The only noticed observable effect was that the PCB traces connected to the biased IC pins had different colors changing from green to black due to corrosion.

6.3 Conducted Immunity and Emission Test Setup

The DPI method is commonly used to characterize the conducted immunity of the IC from 150 kHz to 1 GHz frequency spectrum [4]. The immunity behavior of ICs is established based on the minimum transmitted power level that is required at a specific frequency within a given RF range to cause IC failure [185]. The DPI measurement setup is depicted in Fig. 6.4. The test bench includes a RF generator (Agilent N5183A), a series power meter (Agilent E4419B), a bi-directional coupler, a RF power amplifier (Prana AP32DT120), a multi-channel DC power supply (N6700B), a bias-tee (ZFBT-6GW+), an oscilloscope (Keysight DSOS204A), an arbitrary waveform generator (Agilent 33250A), a signal analyzer with a LabView interface (Agilent N9010A), extreme temperature cables (Amphenol-RF 095-902-466- 004), and a SATIMO thermal oven.

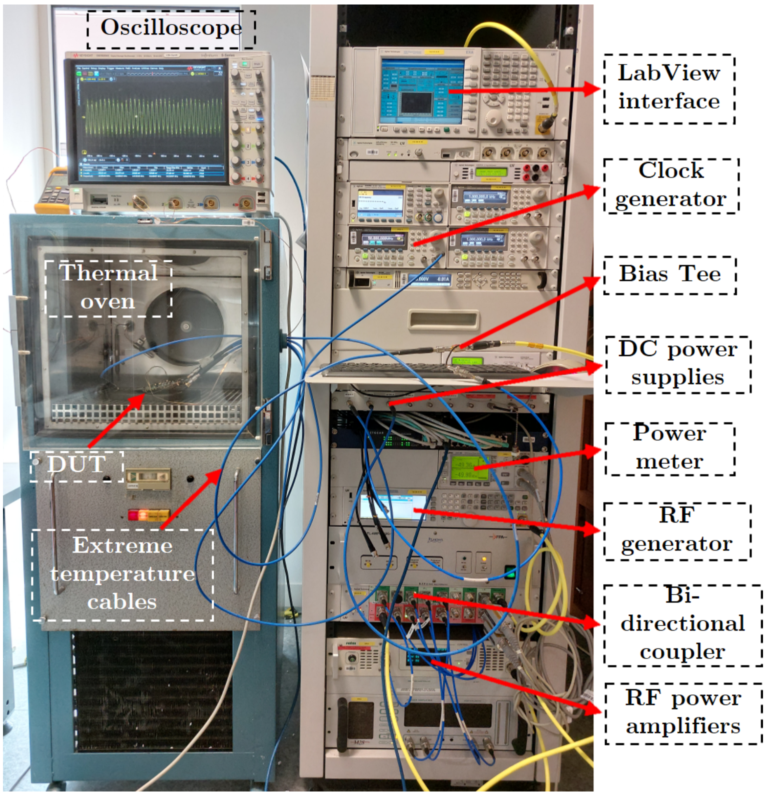


Figure 6.4: DPI experimental test setup © [156].

The analog *S*-*R* latch and the CSVCO were tested using this setup in order to analyze their conducted immunity behavior. The RF generator produces the continuous wave EM disturbance that flows through the bi-directional coupler and is superimposed over the 5 V provided by one of the DC power supply channels via a bias-tee into the V_{DDI} pin of the tested circuit. The remaining channels of the DC supply were connected to the global V_{DDO} and the V_C of the CSVCO at 5 V and 1.8 V, respectively. The power meter provided the injected power from the measured forward and reflected power magnitudes. The amplifier was used to stabilize the injected signals at higher power levels (above 20 dBm). The device under test (DUT) was placed inside the oven and the output pin of the tested circuit was connected to the oscilloscope (1 MΩ) via high temperature cables. The LabView interface was used to control the entire test setup and apply a failure criterion on the output signal using mask testing. The latter involved fixing a mask up to a tolerance limit on the output signal in both directions (lower and higher). Then, the statistical failure rate i.e., the output signal leaving the area of the oscilloscope mask, was averaged over a specific time slot.

The above-mentioned measurement setup was also utilized for conducted emission testing. The V_{DDI} rails of the H-clock tree and voltage sensor were biased to 5 V. One of the channels of the arbitrary wave generator was utilized to inject a square wave into the analog input pin of the H-clock tree and the second channel generated the clock signal for the *S&H* voltage sensor. The current activity of the G_{NDI} of the noise circuit and the output peak voltage of the S&H sensor were monitored through the oscilloscope channels at 50 Ω and 1 MΩ, respectively.

6.4 Conducted Emission Results and Discussion

This section deals with the conducted emission analysis of the H-clock tree and the extraction of the ICEM-CE model, comprising the PDN and IA blocks. Further, the effect of aging and thermal stress are analyzed in measurements and included in the emission model. The H-clock tree was subjected to a square wave input of 50 MHz frequency, 50% duty cycle, 10 ns rise/fall times and 5 V amplitude. The clock of the S&H voltage sensor was set to 999 kHz frequency, 3% pulse width, and 5 V amplitude. The voltage sensor with these clock characteristics transformed the 50 MHz switching activity emitting from the H-clock tree into to a 50 kHz output voltage signal. To characterize the effect of aging, all measurements of the fresh and aged DUTs (biased and unbiased) were carried out at nominal temperature (25 °C). Aged ICs were soldered on a fresh PCB and were tested to exclude the influence of aging on the PCB trace, 1 Ω, 49 Ω resistors and MMCX connectors. Conversely, to analyze the effect of thermal stress on the conducted emission of the noise circuit, measurements were performed on fresh DUTs at ambient and extreme temperatures (i.e., −40 °C and 120 °C). The respective minimum and maximum temperatures were chosen since they conform to the temperature limits of all the components soldered on the tested PCBs.

6.4.1 Extraction of ICEM-CE Model

For the ICEM-CE modeling of a commercial IC, where the latter is considered a black box, an image of the internal current is extracted using measurement tools and impedance profiles from the external current. However, since the IC under test is custom-designed, the internal current was extracted using Cadence Virtuoso (simulation-based transistor-level approach). A hierarchical parasitic extraction was performed for the IC to better approximate the realistic behavior of the dynamic current. The switching of the analog buffers in the *H*-clock tree generates a conducted noise emitted through its V_{DDI} or G_{NDI} rail. Due to a stable input frequency of 50 MHz, the IA dynamic current emission waveform consists of periodic spikes having the same fundamental frequency. The internal current profile of the *H*-clock tree is shown in Fig. 6.5. The IA time domain characteristics exhibit a 1 ns rise time (t_r), a 20 ns period, a 2.5 ns pulse width and an overall peak-to-peak current of 94.5 mA. Each period has two consecutive current spikes with an amplitude of 78.4 mA and 61.3 mA. The extracted internal current was then fed as a netlist to the independent current source to model the IA block of the ICEM-CE model.

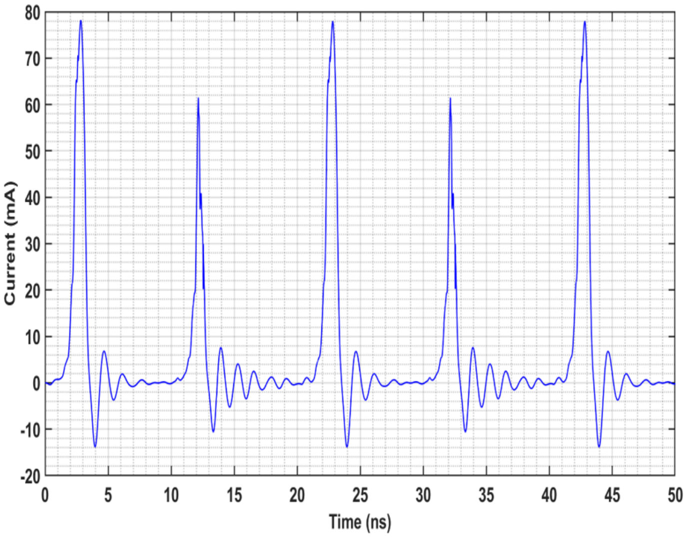


Figure 6.5: Simulated internal transient current (IA) generated by the *H*-clock tree and monitored at the V_{DDI} © [156].

The electrical behavior of the PDN is given by its complex impedance and can be modeled using lumped passive R, L, and C elements. To determine which passive elements are required to model the PDN upto a certain frequency, the t_r of the internal current is a critical parameter. The bandwidth capable of dealing with this t_r can be determined using [166]:

$$F_{max} = \frac{0.35}{t_r} \tag{6.1}$$

Harmonics above F_{max} are considered low enough not to generate considerable emission levels. Hence, the frequency limitation of the PDN is equal to 350 MHz.

A VNA was used to measure the one-port S-parameters (S_{11}) of the V_{DDI} pin of the H-clock tree. Furthermore, a calibration board, adopting the SOLT method, was utilized to accurately measure the correct S_{11} profile (including magnitude and phase) between 10 MHz to 3 GHz. The results were then converted to impedance parameters (Z_{11}) using:

$$Z_{11} = Z_0 \left(\frac{1 + S_{11}}{1 - S_{11}} \right) \tag{6.2}$$

where, Z_0 is the characteristic impedance that is equal to 50 Ω. The impedance profile of the H-clock tree power supply network is shown in Fig. 6.6. The frequency response of the impedance up to 350 MHz is divided into several parts. Below 120 MHz, the impedance is capacitive (C1). The impedance becomes resistive at 150 MHz (R1) and 315 MHz (R2). The latter has a lower value and is the actual impedance at the resonant frequency, where the phase crosses zero. Between 150 to 300 MHz a steeper capacitive (C2) impedance effect is observed. The reason for the parasitic resonance is due to the V_{DDI} rail of the H-clock tree connected inside the IC to the input of the voltage sensor. The first stage of the sensor includes an attenuator with compensation capacitors, which causes the parasitic resonances noticed in the impedance profile. From 320 MHz until 400 MHz the impedance becomes inductive (L1) and can be computed at a given frequency with in this range.

The ICEM-CE simulation setup is depicted in Fig. 6.7. It includes an independent current source, which represents the IA block of the ICEM model. The block capacitance (C1) was measured through the VNA when the V_{DDI} rail of the H-clock tree was biased with 5 V. The difference in the capacitance from the unbiased version was found to be 10 pF. The first order R, L, and C parameters (R2, C2, R3, C3, L1, L2) were extracted from the Z_{11} profile and they make up the PDN of the ICEM model. Further, to have a better correlation between the conducted

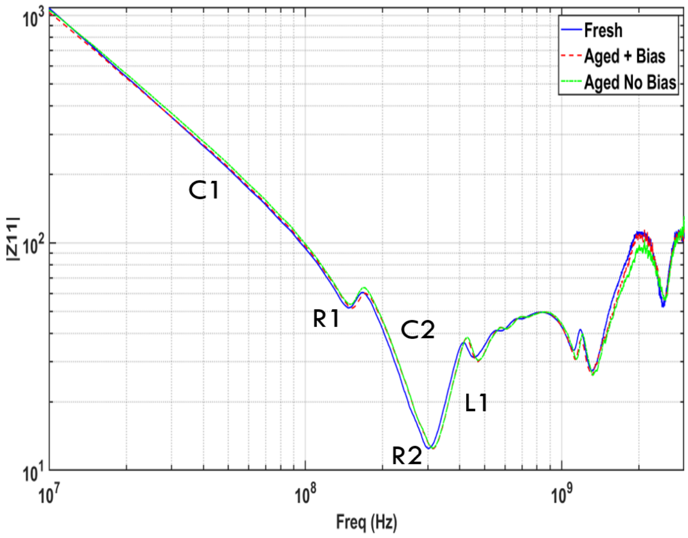


Figure 6.6: Measured impedance profile of V_{DDI} of H-clock tree with aging © [156].

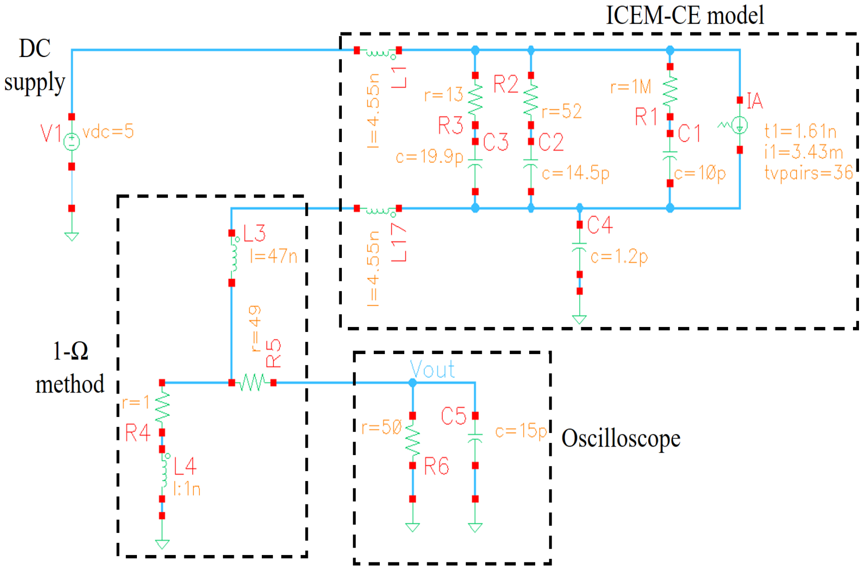


Figure 6.7: ICEM-CE simulation setup © [156].

emission measurements and model, the die to ground capacitance (C4) of 1.2 pF was included in the latter. The ICEM-CE simulation setup also includes a 5 V DC source and a 1 Ω resistor (R4) in series with its 1 nH parasitic inductance (L4) connected to the ground. Since the PCB trace has a length of 47 mm, it can generate a 47 nH (1 nH/mm) parasitic inductance (L3), which was added in series to the 49 Ω resistor (R5). Finally, the oscilloscope was modelled by a 50 Ω resistor (R6) and its 15 pF parasitic capacitance (C5) which affects the peak of the output signal in measurements.

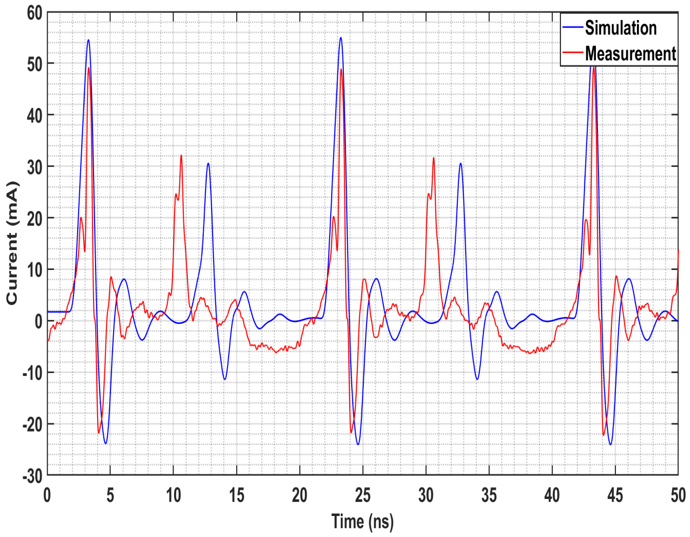


Figure 6.8: Comparison of the external current extracted through the ICEM simulation setup and 1-Ω measurement © [156].

The external current activity extracted from the ICEM-CE simulation setup and through measurement using the 1 Ω method are illustrated in Fig. 6.8. A significant correlation for the amplitudes of the two consecutive peaks between the extracted and measured current was noticed. The maximum peak-to-peak current of the former was 2.6% higher than the latter. However, the measured current included some minor parasitic inductance effects noticed at the consecutive spikes which could be due to measurement uncertainty. Moreover, a delay of 1.5 ns is observed for the second consecutive peak of the simulated external current compared to the measured one. According to simulations, it was deduced that this anomaly is due to the IA block of the ICEM-CE model, which may include additional L and C parasitics in the internal traces and were excluded by the transistor-level extraction tool. Interestingly, the peak-to-peak internal current (Fig. 6.5) was only 20.3% (16 mA) higher than the measured external peak-to-peak current (Fig. 6.8). This implies that the power supply network does not have a significant filtering effect on the internal switching current.

6.4.2 Influence of Aging on Conducted Emission

As discussed in Section 6.2, HAST testing was performed on the DUT (biased and unbiased) to evaluate the effect of aging on the conducted emissions generated by the H-clock tree. All S-parameter and conducted emission measurements were carried out at ambient temperature on fresh and aged ICs to find out if the PDN or/and the IA blocks of the ICEM model are impacted by aging. As observed from Fig. 6.6, the Z_{11} profile is hardly affected by aging (biased/unbiased) over the entire frequency range. There exists a minor variation in the Z_{11} for frequencies above 1 GHz but this can be discarded due to measurement uncertainty. These results demonstrate that aging due to HAST has no considerable impact on the PDN of the ICEM-CE model.

Contrarily, the conducted emission measurement results using the 1-Ω method revealed the induced effect by aging due to HAST on the external maximum peak-to-peak current levels. Two biased (Aged 1, Aged 2) and two unbiased (Aged 3, Aged 4) aged ICs were tested for the sake of repeatability. The time domain characteristics of the fresh and aged samples were the same but with reduced peak current levels for the aged ones (Table 6.1). The average external peak-to-peak current of all the aged samples (71.52 mA) was 9.8% lower than the fresh version (78.54 mA). Since, aging had no impact on the PDN, the only possible explanation for the reduced external conducted emission levels is due to the decreased amplitude of the internal current. Aging due to HAST triggered degradation mechanisms (NBTI), impacting the switching activity of the buffers in the H-clock tree, and hence, impacting the internal current emission levels. As indicated in Table 6.1, the peak-to-peak internal current values of the aged samples were extrapolated from measurements.

The S&H voltage sensor was used in random acquisition mode and intentionally under-sampled the 50 MHz current switching activity of the H-clock tree down to 50 kHz. Although, it was not possible to reconstruct the shape of the input signal in random acquisition mode, the histogram type output voltage signal could indicate RF distortions in the conducted emission signal. The output voltage waveform of the fresh and aged sensors is shown in Fig. 6.9. No such distortions were observed in the output waveform. More importantly, the average output peak-to-peak voltage of the aged samples (1.40 V) was 60 mV lower than the fresh samples (1.46 V) (Table 6.1).

To validate that aging only affected the internal switching activity of the H-

Table 6.1: Variation in Conducted Emissions with Aging (HAST); the *italic* values are extracted by extrapolation from measurements © [156].

Sample	**External peak-to-peak current**	**Internal peak-to-peak current**	***S&H* sensor peak-to-peak voltage**
Fresh	78.54 mA	94.50 mA	1.46 V
Aged 1	70.95 mA	*85.35* mA	1.39 V
Aged 2	71.81 mA	*86.39* mA	1.40 V
Aged 3	72.32 mA	*87.01* mA	1.42 V
Aged 4	72.03 mA	*86.66* mA	1.41 V

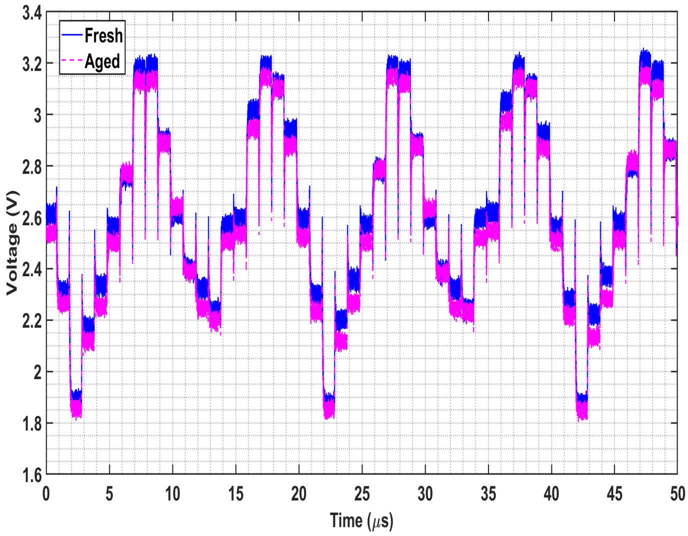


Figure 6.9: Effect of aging on the clocked output voltage of the S&H sensor © [156].

clock tree, a separate/identical S&H voltage sensor (integrated into the IC) was tested after aging. A DC offset of 0.1 V was found in the output voltage signal which was due to the compensation capacitors of the input attenuator being aged. However, no considerable variation in amplitude was observed in the output signal when subjected to a 50 MHz input sine wave. Hence, this verified that the reduction in peak output voltage amplitude was due to the H-clock tree. It was checked that the spectral content of the external current did not vary with aging. Since the PDN does not change with aging either, a constant coefficient of proportionality can be established between the external and the internal (IA) peak values whatever the IC state (fresh/aged). This coefficient can be extracted from simulations of the fresh IC and reused for aged ICs which cannot be simulated. Therefore, the IA block could be modified to include that coefficient of aging.

6.4.3 Influence of Thermal Stress on Conducted Emission

In comparison with aging, thermal stress can temporarily raise junction temperatures of CMOS transistors in the tested circuit and create a drift in their V_{th}, μ_{eff}, and drain current levels [126]. Although no permanent degradation mechanisms occur, these drifts can cause unexpected conducted emission levels. S-parameter measurements were performed on fresh PCBs at ambient and extreme temperatures (−40 °C and 120 °C) to characterize the effect of thermal stress on the Z_{11} profile of the V_{DDI} of the H-clock tree. This time, the VNA was calibrated by placing the calibration board at extreme temperatures as well, to exclude thermal influence on the cables, the PCB traces and external I/O connectors. Interestingly, the effect of thermal stress on the Z_{11} over the entire frequency range was significant (38% span for R2), which could not be discarded. As seen in Fig. 6.10, the R, L, and C values of Z_{11} change with temperature variations. With the rise in temperature, the values of passive elements increased up to 400 MHz. This implies that thermal stress has an impact on the PDN of the ICEM model and all extreme values (shown in Table 6.2) of the passive elements need to be included.

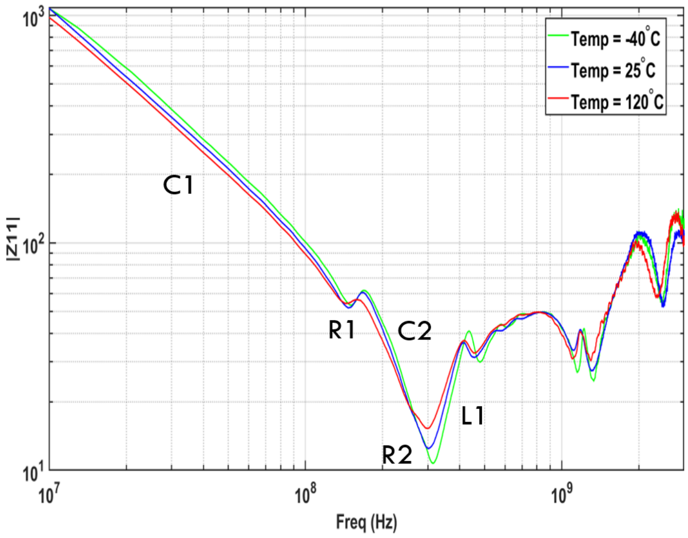


Figure 6.10: Influence of temperature on the measured impedance profile of the V_{DDI} of the H-clock tree © [156].

Table 6.2: Deviations in PDN Parameters Extracted at the V_{DDI} of the H-clock Tree due to Thermal Stress © [156].

Component	**T = -40 °C**	**T = 25 °C**	**T = 120 °C**
C1	13.2 pF	14.5 pF	15.9 pF
R1	51.5 Ω	52 Ω	54 Ω
C2	17.7 pF	19.9 pF	21.5 pF
R2	11 Ω	13 Ω	16 Ω
L1	8.6 nH	9.1 nH	9.7 nH

Similar to aging, the conducted emission measurement results using the 1-Ω method revealed a variation of the maximum external peak-to-peak current levels due to thermal stress. The 1-Ω probe resistors have a temperature drift coefficient of 50 ppm/°C. This was included in the ICEM simulation to accurately quantify the effect of thermal stress on the emission spectrum generated by the H-Clock tree. As noticed from Table 6.3, a rise in temperature substantially decreased the external peak current levels. With respect to ambient temperature, a deviation of +14% and −26% of the external peak-to-peak current was observed at −40 °C and 120 °C, respectively.

Table 6.3: Variation in Conducted Emissions with Thermal Stress © [156].

Temperature	**External peak-to-peak current**	**Internal peak-to-peak current**	***S*&*H* sensor peak-to-peak voltage**
-40 °C	89.55 mA	99.71 mA	1.49 V
25 °C	78.54 mA	94.50 mA	1.46 V
120 °C	58.09 mA	83.44 mA	1.38 V

To further verify that thermal stress affects not only the PDN but also the IA block of the ICEM model, transistor level simulations were carried out in Cadence Virtuoso for different temperatures including the thermal behavior of external passive elements. The internal current at the V_{DDI} node of the H-clock tree was monitored at nominal and extreme temperatures. As illustrated in Fig. 6.11, the amplitude of the internal current was found to have an inverse variation with thermal

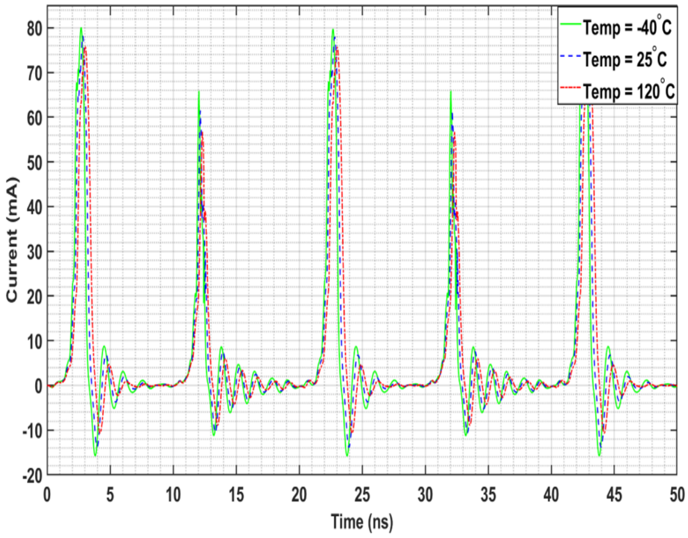


Figure 6.11: Influence of temperature on the simulated internal transient current (IA) generated by the H-clock tree and monitored at the V_{DDI} © [156].

stress. Further, the internal current peak-to-peak found at extreme temperatures through simulations are included in Table 6.3. Although variations in the internal current exist due to temperature, the deviations are lower compared to the externally measured current. Therefore, the dependence of the PDN and the 1 Ω output resistor on temperature enhances the effect of thermal stress on the external peak current levels. Indeed, the same method as the one related to aging can be applied for thermal using another coefficient of proportionality for extreme temperatures.

The output voltage waveform of the S&H voltage sensor is shown in Fig. 6.12. Similar to aging, no distortions were noticed in the output signal. The output peak-to-peak voltage levels were 30 mV higher and 80 mV lower compared to that of the nominal temperature, at −40 °C and 120 °C, respectively. Further simulations were performed on the voltage sensor to analyze how thermal stress caused variation in the output voltage in steady state conditions. It was found that the output DC offset of the voltage sensor varied with temperature only by ±150 mV for input frequencies lower than 550 MHz.

Moreover, it was verified in Cadence Virtuoso that the input attenuator was the root cause for the DC offset. Fig. 6.13 shows the simulated output response of the DC attenuator when subjected to a sine wave input signal of 500 MHz frequency and 1 V peak voltage at nominal and extreme temperatures. It can be observed that thermal stress causes only a DC offset (±65 mV) and there is no observable change in

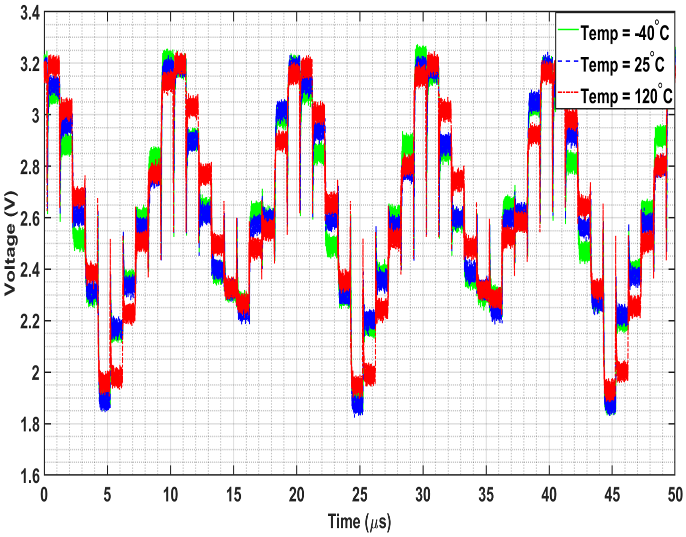


Figure 6.12: Influence of thermal stress on the clocked output voltage of the S&H sensor © [156].

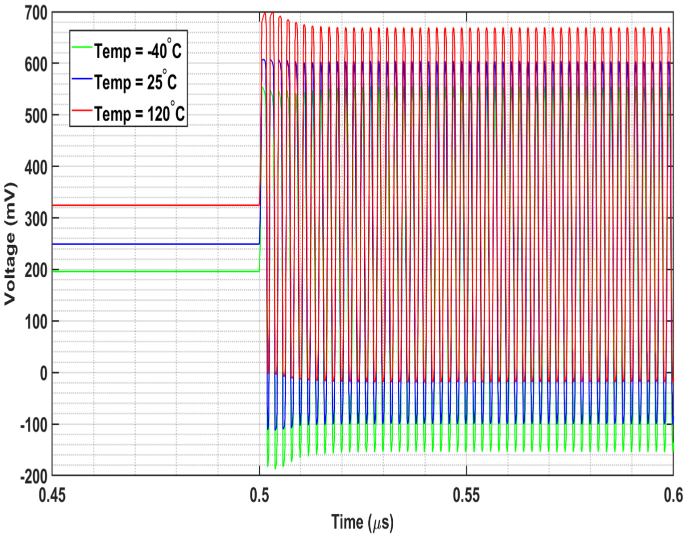


Figure 6.13: Influence of thermal stress on the *S&H* voltage sensor attenuator for an input sine wave of 500 MHz © [156].

the peak output voltage. Furthermore, it was found out that for input frequencies above 550 MHz, the peak output voltage was reduced at 120 °C. This is due to the filtering effect of the compensation capacitors. Since conducted emission tests were performed at much lower frequencies, thermal stress did not affect the peak output voltage of the sensor. Although there exists a DC offset due to temperature variation, it was checked that the reduction of the output peak-to-peak voltage levels of the sensor at maximum temperature was due to decreased internal peak-to-peak current levels of the H-clock tree.

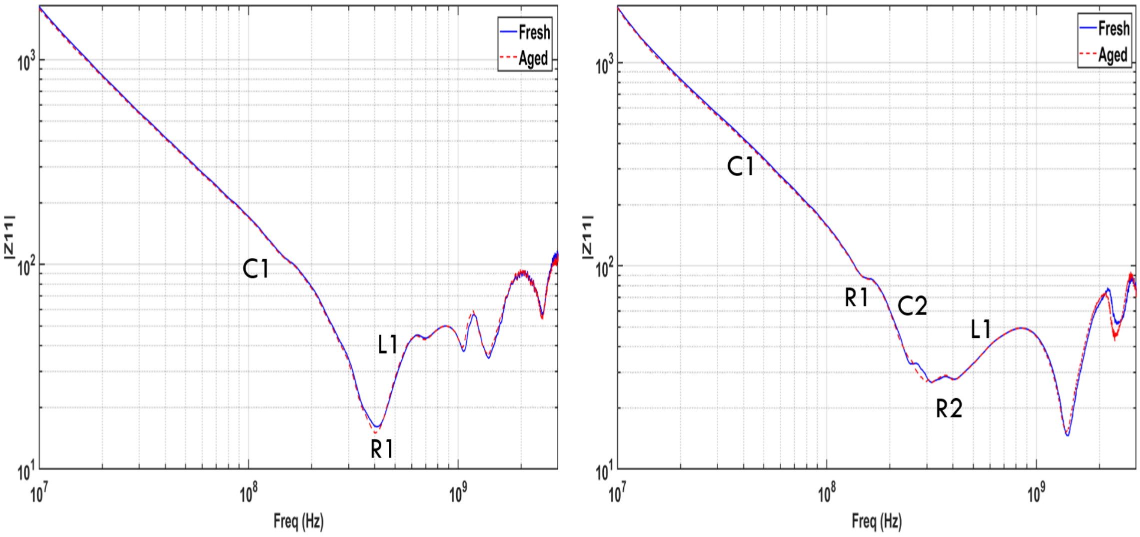
To sum up, in this case study, the PDN of the ICEM model is not influenced by HAST aging. However, thermal stress does have an impact on the PDN, causing deviations in its lumped passive elements. The IA block of the ICEM model is influenced by both aging and thermal stress, due to different physical mechanisms, though. Aging reduces the IA amplitude, and the conducted emission levels demonstrate an inverse variation with temperature.

6.5 Conducted Immunity Results and Discussion

This section deals with the conducted immunity analysis of two independent analog blocks, i.e., S-R latch and 3-stage CSVCO integrated into the tested IC. The extraction of two separate PDNs via S-parameter measurements and IB blocks through the DPI look-up table technique are explained. Moreover, the effects of HAST aging and thermal stress at −40 °C and 120 °C are analyzed in measurements and incorporated in the ICIM-CI model. The DPI measurement setup illustrated in Section 6.3 was used to evaluate the susceptibility profiles of each tested circuit. The incident power was varied from 1 dBm to 30 dBm with a step size of 1 dBm while the frequency was changed from 1 MHz to 1 GHz in 10 MHz steps. For both tested structures, the continuous wave EM disturbance was superimposed over a 5 V DC bias only into its isolated power supply. The failure criterion considered for the S-R latch was ±10% of the DC offset with a dwell time of 1 second. Similarly, the ±10% changes in frequency or in the peak-to-peak voltage of the CSVCO were considered as its DPI failure criteria. All selected tolerance limits were similar to industry standards. Moreover, a dwell time of 3 seconds was set for the latter in order to allow it enough time to stabilize after each power/frequency increment.

6.5.1 Influence of Aging on Conducted Immunity

The PDN block of the ICIM-CI and the ICEM-CE are identical and were extracted from S-parameter measurements. Two independent Z_{11} impedance profiles of the V_{DDI} of the analog S-R latch and the 3-stage CSVCO are shown in Fig. 6.14.a and 6.14.b, respectively. Even though both circuits have identical pads their impedance profiles are entirely different. The reason for this could be due to the distinct mutual coupling, since the V_{DDI} pad of the *S*-*R* latch is closer to its G_{NDI} pad compared to the CSVCO. Similar to the Z_{11} profile of the *H*-clock tree, the impedance profiles of the two immunity test circuits were not impacted by aging.



(a)

(b)

Figure 6.14: Impact of aging on measured impedance profile of V_{DDI} of © [156]: (a) analog *S*-*R* latch; (b) 3-stage CSVCO.

The IB block of the ICIM-CI model was constructed using look-up tables which correspond to the amount of transmitted power in the IC pin that can cause its malfunction. This can be extracted using DPI measurements and is analyzed in the frequency domain. The power meter in the DPI setup gives the transmitted power (P_t) from the measured forward (P_{fwd}) and reflected (P_{ref}) power magnitudes. This can be represented using:

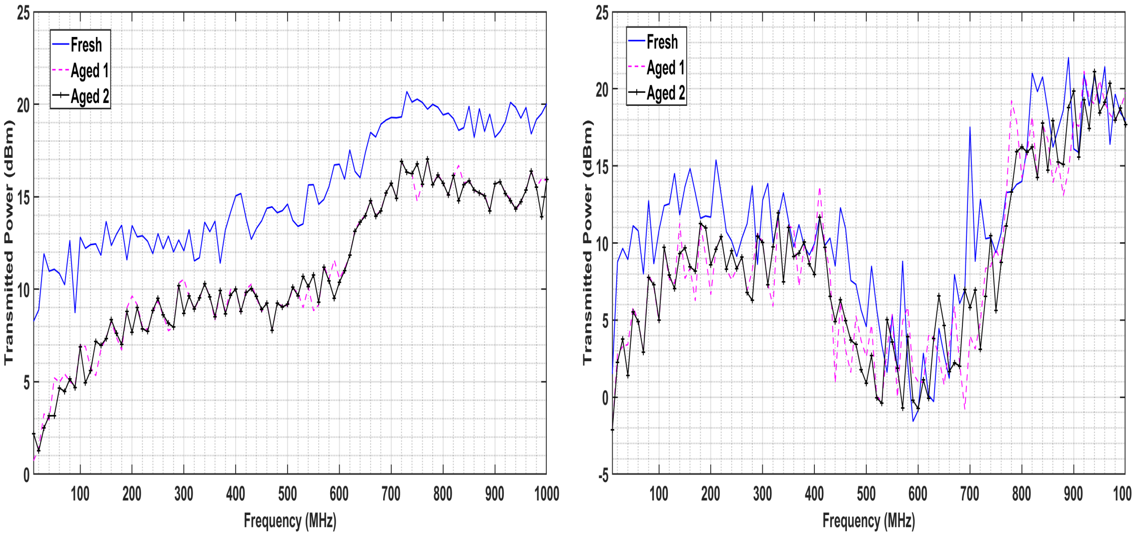
$$P_t = P_{fwd} - P_{ref} \tag{6.3}$$

The P_{fwd} comes from the source and is not dependent on the load. The P_{ref} is attained due to the mismatch between the source and the load. The P_t injected into the IC is depended on the input pin impedance and can also be calculated using:

$$P_t = P_{fwd}\left(1 - |S_{11}|^2\right) \tag{6.4}$$

Hence, P_t is the actual power that couples into the IC pin and can cause eventual failure of the tested circuit and can be used to determine its conducted immunity profile.

To construct two separate IB blocks, DPI testing was performed by injecting conducted EM disturbances into the V$_{DDI}$ pins of the S-R latch and the CSVCO. The power P_t to induce malfunction was determined using each circuit S-parameters. Fig. 6.15.a shows the conducted immunity profile of the analog S-R latch. The failure criterion applied for the S-R latch was the DC-offset of the output signal monitored at the Q pin. The immunity profile for the fresh DUT shows a gradual increase in P_t from 8 dBm at 1 MHz to 20 dBm at 1 GHz. This behavior demonstrates that the S-R latch is more susceptible at lower frequencies. Therefore, the combined effect of the package and the capacitance of the input pad results in filtering effects, hence attenuating power in higher frequency.



(a) (b)

Figure 6.15: Impact of aging on the conducted EM immunity profile of © [156]: (a) analog S-R latch; (b) 3-stage CSVCO.

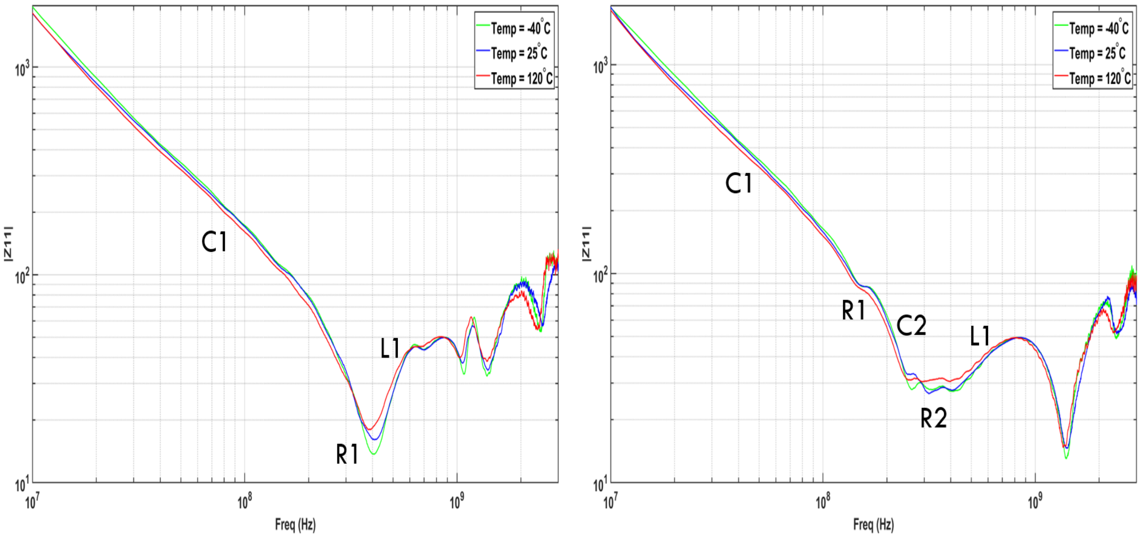
The frequency and the peak-to-peak voltage of integrated oscillators are important parameters to determine their stability. Thus, for DPI testing of the CSVCO, both parameters were considered as the failure criteria. The conducted immunity profile of the CSVCO is visible in Fig. 6.15.b. The immunity behavior of the CSVCO is very different compared to the S-R latch. Overall, the package and input pad capacitance effect is demonstrated here as well, since the highest conducted immunity is observed above 850 MHz. However, the CSVCO is the most susceptible between 600 to 700 MHz. The reason for this could be due to the injected frequency being close to the operating frequency (703 MHz) of the CSVCO. As mentioned in Section II-C, the FD circuit is added at the output stage of the CSVCO in order to reduce the output frequency (62.5 MHz). Although the power supply of the FD is entirely isolated from EMI, it may still impact the conducted immunity evaluation.

DPI testing was performed on several aged DUTs, at ambient temperature, having the same failure criteria for both tested blocks. In general, aging due to HAST induced a decrease in the conducted immunity levels of both tested circuits. The immunity profile waveforms remained the same with reduced immunity power levels. As seen in Fig. 6.15.a, the average P_t levels of the aged samples were 6 dB lower than the fresh sample within the tested frequency spectrum. Hence, aging only impacted the IB block of the ICIM-CI model of the S-R latch. The lower P_t and corresponding frequency values were then updated in the IB look-up table to include the effect of aging in the ICIM-CI model.

To verify the assertion that aging affects the IB block and lowers the P_t levels that can trigger a failure, the conducted immunity of the CSVCO was compared with respect to aging (Fig. 6.15.b). In this case, the aged P_t levels were slightly reduced (4.5 dB), compared to the fresh version, in particular in frequencies below 200 MHz. At higher frequencies, the immunity levels of the fresh and aged samples were comparable. The degradation mechanisms (NBTI) occurring in the CSVCO and the S-R latch are not the same. Since both circuits have different functionalities and failure criteria, the impact of aging is distinct. However, it can be concluded that aging due to HAST reduces conducted immunity levels in a given frequency range for both tested analog blocks. These aged power levels can be updated in the IB block of each ICIM model to include the effect of aging. This may be achieved by the means of specified deviations on IB look-up tables, or different IBs according to the fresh/aged state of the block.

6.5.2 Influence of Thermal Stress on Conducted Immunity

To validate the impact of thermal stress on the PDN of both the S-R latch and the CSVCO, S-parameter measurements were performed on fresh PCBs at extreme temperatures (-40 °C and 120 °C). As expected, the Z_{11} profiles of the V_{DDI} of the S-R latch (Fig. 6.16.a) and the CSVCO (Fig. 6.16.b) exhibited variations with thermal stress over the entire frequency range. Those deviations could not be neglected and all tolerances were involved in the PDN block of the individual ICIM-CI models of the S-R latch (Table 6.4) and the 3-stage CSVCO (Table 6.5).



(a) (b)

Figure 6.16: Influence of thermal stress on measured impedance profile of V_{DDI} of © [156]: (a) analog S-R latch; (b) 3-stage CSVCO.

Thermal stress influences the MOSFET characteristics in ICs and can vary the robustness of an analog circuit. For the analog S-R latch the 5 V (25 °C) DC level of the output was increased to 5.3 V (−40 °C) and 4.7 V (120 °C) with temperature variations. Hence, it was considered that the V_{th} levels of the MOSFETs in the latch were the root cause of the change in DC output levels. For the CSVCO, the operating frequency was verified in simulations to be inversely proportional to temperature. Its output frequency after the FD, was found to be 62.5 MHz at nominal temperature and varied to 68.3 MHz and 53.8 MHz at −40 °C and 120 °C, respectively. For the CSVCO, the shift in frequency meant that the V_{th} and the μ_{eff} were influenced by temperature.

To authenticate the effect of thermal stress on the IB block, multiple fresh DUTs were subjected to DPI testing at nominal and extreme temperatures, by injecting into the V_{DDI}s of the S-R latch and the CSVCO. Similar failure criteria considered for the nominal temperature were applied at extreme temperatures for both circuits. The influence of thermal stress on the conducted immunity profiles of the S-R latch and the 3-stage CSVCO is illustrated in Fig. 6.17.a and 6.17.b, respectively. For the S-R latch, the increase in temperature lowered the conducted immunity P_t levels. As observed in Fig. 6.17.a, compared to the nominal temperature, the average P_t

Table 6.4: Deviations in PDN Parameters Extracted at the V_{DDI} of the Analog *S-R* Latch due to Thermal Stress © [156].

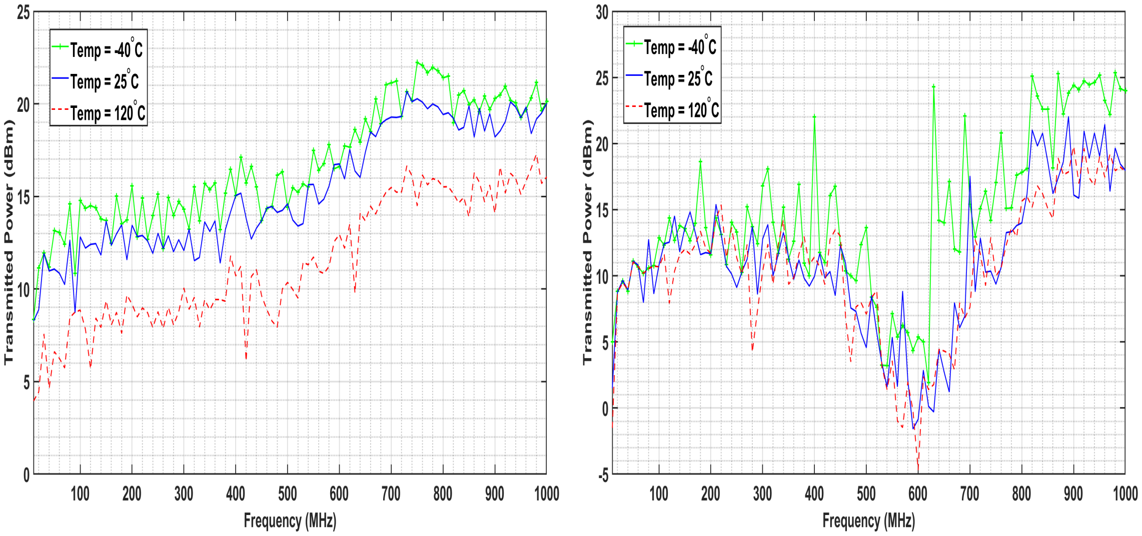
Component	**T = -40 °C**	**T = 25 °C**	**T = 120 °C**
C1	8.6 pF	9.2 pF	10.1 pF
R1	15 Ω	17 Ω	19 Ω
L1	8.4 nH	9.1 nH	10 nH

Table 6.5: Deviations in PDN Parameters Extracted at the V_{DDI} of the 3-Stage CSVCO due to Thermal Stress © [156].

Component	**T = -40 °C**	**T = 25 °C**	**T = 120 °C**
C1	8.8 pF	9.6 pF	10.6 pF
R1	87 Ω	88 Ω	89 Ω
C2	12.2 pF	13.3 pF	15 pF
R2	27 Ω	28 Ω	32 Ω
L1	9.2 nH	10.6 nH	11.9 nH

levels were improved by 1.8 dB at minimum temperature while they were lowered by 5.1 dB at maximum temperature. Due to the drift in V_{th} levels of the MOSFETs in the latch, the conducted immunity of the latter was extensively influenced by the thermal stress.

In the case of the CSVCO (Fig. 6.17.b), the conducted immunity profile approximately remained the same at 120 °C across the entire frequency spectrum. However, at -40 °C, the average P_t levels improved substantially by 9.2 dB between 600 to 700 MHz. It continued to be slightly higher (1 dB) than the P_t levels at 25 °C for frequencies between 700 MHz to 1 GHz. The conducted immunity of the CSVCO was found to be resilient to higher temperatures, however, lower temperatures had an impact on its conducted immunity due to the drift in μ_{eff} and V_{th} levels. Hence, for both circuits, the thermal stress influenced their respective IB blocks of the ICIM-CI models. Similarly to aging, deviations can be applied to the IB look-up tables as a function of temperature.



(a) (b)

Figure 6.17: Influence of thermal stress on the conducted EM immunity profile of © [156]: (a) analog *S*-*R* latch; (b) 3-stage CSVCO.

6.6 Conclusion

The concept of involving environmental effects such as aging and thermal stress in the conventional conducted emission (ICEM-CE) and immunity (ICIM-CI) models was put into practice herein through measurements and transistor level simulations. The PETER_ESEO IC in SOI technology, comprising several independent analog CMOS structures such as *H*-clock tree, S&H voltage sensor, *S*-*R* latch, and 3-stage CSVCO, was employed for conducted emission and immunity measurements. HAST and extreme temperature tests were performed on several packaged ICs in order to extensively analyze the influence of aging and thermal stress on the immunity and emission levels. Unlike with HAST aging, the PDN block of the developed models was influenced by thermal stress causing variations in its lumped passive elements, which must be included in the models for improved accuracy. However, aging caused the permanent degradation mechanisms (NBTI), while thermal stress temporarily impacted the MOSFET characteristics (i.e., μ_{eff} and V_{th}) that could cause IC soft failures and influenced the active blocks of the models.

A simulation-based transistor-level approach was used to develop the IA block of the ICEM-CE model, providing comparable current amplitude levels with measurements. By applying conducted emission measurements using the 1- Ω method on the H-clock tree, it was demonstrated that the external current emission levels would degrade with aging and temperature increase. This effect was traced back to the variation in the internal switching current (i.e., IA block of the ICEM-CE model) in case of thermal stress. Therefore, it was shown that constant proportionality coefficients extracted from simulations and/or measurements could be included into the IA blocks of the models. Using DPI measurements on two independent S-R latch and CSVCO circuits, it was demonstrated that aging due to HAST decreases the conducted immunity levels as a function of frequency depending on the functionality of the analog block. Moreover, high temperature stress was found to also increase their conducted susceptibility levels depending on the drifts in μ_{eff} and/or V_{th} levels.

Chapter 7

CONCLUSIONS AND PERSPECTIVES

7.1 Conclusions

Within the lifetime of an IC, critical environmental conditions can strongly influence its EMC behavior. At the time being, there is no fast, cost-effective method to guarantee that a system can maintain its EMC performance. Further, the conducted continuous-wave EM immunity of ICs is currently being characterized by single-tone EM disturbances. In practice, however an uncertain EM environment includes multiple disturbances that could couple into the IC pins simultaneously causing soft or hard failures.

To accurately characterize and analyze conducted immunity and emission levels at the IC level and adopt a white-box approach to find the root cause of failure, a custom-designed IC was developed. For a risk-based EMC approach, multitone immunity testing was adopted in simulations and measurements to characterize the causal interactions and investigate the influence of temperature on these immunities. Additionally, the transient EM immunity of analog blocks with similar functionality but different topologies were compared and investigated under the impact of thermal stress.

Existing IEC models have been proposed for the anticipation of conducted EMC issues. However, these IC models have several limitations as they do not take into account environmental stresses such as aging and thermal stress. Highly accelerated life tests and thermal cycling were performed to validate the effect of aging and thermal stress, respectively, causing deviation in the passive and/or active blocks of these standard models. To highlight the final outcomes and findings of each specific chapter, they are briefly summarized as follows:

Chapter 1 introduces the outline of this thesis including the background of EMC at IC level and motivations, the objectives, and its organization.

Chapter 2 describes the details of both the developed custom-designed IC fabricated in 180 nm 5 V SOI CMOS technology and conducted immunity/emission PCB variants for the purpose of the research works conducted in the manuscript. The main benefit of SOI technology is its ability to isolate internal IC blocks from one another, making it possible to carry out individual conducted immunity experiments on those blocks. However, bulk technology is much more widely used in industry and may exhibit a different behavior in terms of PVT variations.

Therefore, in Chapter 3, with the aim to compare SOI and bulk technologies, an integrated S&H voltage sensor was characterized when subjected to those variations. It was demonstrated that compared to bulk technology, the SOI on-chip sensor has lower power consumption and leakage supply current, higher sensitivity to process variations (in particular the slew rate of the Miller amplifier, sub-block of the sensor), higher resilience to temperature changes, but a larger occupied area.

Then, the data stability, write ability and power metrics of 6T & 9T SRAM cells were investigated when exposed to process and temperature variations. Compared to bulk technology, the SRAM cells designed in SOI demonstrated better data stability, lower leakage supply current and power dissipation as well as a higher resilience to temperature changes. However, the SOI SRAMs showed reduced write ability and greater sensitivity to process variations in comparison with bulk SRAMs.

To sum up, this chapter shed light on the SOI technology as the promising approach to build more temperature resilient analog ICs such as on-chip S&H sensor and SRAM cells, highlighting their limitations such as susceptibility to process variations.

At the time being, continuous-wave conducted immunity testing standards only consider single-tone injection. However, in a real world environment, multiple frequencies can be present, thus making those injection tests unrealistic. A ”risk-based” EMC approach needs to consider the possibility of multitone EM disturbances. Therefore, in Chapter 4, the application of various existing (noisy-OR, RNOR and ARNOR) and newly proposed (I-ARNOR) probabilistic models was demonstrated through simulations and measurements for two different case studies to identify the multi-causal interaction types between simultaneous EM disturbances and predicting the immunity performance of a component with respect to untested higher-order multitone disturbances. The maximum number of tones that need to be considered for multitone immunity investigations as well as the change in the proportion of synergy type interactions with increasing multitone were analyzed in detail to provide a safety margin if the interactions are asynergy or inhibition. The limitations of such analyses, such as the exponential rise in the number of possible multitone combinations due to the impracticality in experiments, were also highlighted, where the newly developed I-ARNOR model in this chapter was shown to predict the IC failure probability of untested third or higher-order multitone combinations at an accuracy much better than the existing models.

Then, steady-state simulations and probabilistic models were compared to assess the multi-tone immunity levels of two conventional 3-stage SOI-integrated RO and CSVCO. Even with similar functionality, an increased failure probability was observed due to the causal synergy between simultaneous single-tone EM disturbances. Contrarily, the increase in the number of simultaneous tones (e.g., from two to three tones) demonstrated a relative decrease in the probability of EM failures due to higher incidence of inhibition, which indicates that the noisy-OR model immunity verification can be regarded as a conservative approach.

Finally, the combined effect of multitone EM disturbances and temperature variations on the conducted immunity of those oscillators was examined. The performance of the CSVCO was shown to outperform the RO at ambient temperature, due to the slightly higher proportions of inhibition for both two and three-tone EM disturbances. Most of the synergistic interactions were found to come from the output frequencies being locked to one of the injected multitone EM disturbances. More importantly, the rise in the number of tones highlighted the effect of intermodulation leading to the increase of the proportion of inhibition for the CSVCO, and of asynergy for the RO. Moreover, temperature variation demonstrated a deviation in the output frequency of both oscillators, with the CSVCO being more robust compared to the RO. However, completely reversed results were obtained under the combined effects of multi-tone EMI and temperature, where the CSVCO was found to be more susceptible to multitone EMI than the RO at extreme temperatures. Moreover, the variation in temperature was also found to impact the transition of synergistic frequency combinations to higher frequencies for both oscillators, demonstrating that thermal stress caused a significant influence on the package, the I/O pad capacitance and the FD circuit of the IC.

To summarize, the application of a BN model to include the uncertainties associated to the occurrence of the EM disturbances and temperature was shown to make it convenient for an expert to determine the EM risk of IC or component failure in the system environment. By comparing the obtained measurement results, it was verified that the I-ARNOR model was the most accurate at most occasions with a minimal mean prediction error and standard deviation. Indeed, it was shown that by combining probabilistic models and measurement techniques, multitone EM testing can be involved in the conventional DPI, to more precisely characterize the conducted immunity of a circuit at the IC level.

After studying multitone continuous wave EM immunity, the transient conducted immunity of ICs still remains to be determined for a proper evaluation of EM risks. Consequently, in Chapter 5, the transient immunity of ICs and the importance of obsolescence in EMC risk management were studied. As a showcase, a comparative study was first conducted between two pin-compatible SAM3 and SAM7 μCs (the former being the upgraded version of the later) to investigate the EFT immunity of their individual power supply pins. Even with having identical input impedance profiles, SAM3 was demonstrated to have a higher EFT immunity compared to SAM7 on all the considered supply pins except the PLL supply pin. Such a study clearly highlighted that a more modern version of a μC does not necessarily ensure a higher EFT immunity in all power supply pins and further EMC analyses are to be performed, particularly when dealing with obsolescence.

Then, three multi-stage CSVCOs and ROs from the PETER_ESEO IC, protected by the same ESD devices, were assessed under EFT and thermal stresses. Depending on oscillator topology, distinct B- and E-type failure modes were observed for all the considered oscillators, whereas a D-type failure was only noticed for the RO mainly due to the frequency limitation of the FD circuit. The latter was found to cause an overall reduction in the slew rate increasing the recovery times of each oscillator once the EFT disturbance was applied. Additionally, temperature elevation was found to decrease the output frequency of each oscillator while the transient latch-up behavior of the ESD devices remained unaffected.

Finally, the rise in temperature was demonstrated to reduce the absolute EFT immunity levels for all the tested oscillators by affecting the protection capability of the ESD devices. The 5-stage CSVCO was found to be the most resilient to temperature variations when compared to the other two oscillators. However, an entirely different performance was observed when the oscillators were subjected to the combined EFT and temperature stresses; the 5-stage CSVCO was found to be the most susceptible to EFT at extreme temperatures. Conversely, the 3-stage RO and CSVCO were shown to be the most immune to EFT, respectively. The on-state resistance of the MOSFETs varies considerably when EFT stress and temperature variations are combined. The root cause for the latter is the combined reduction of μ_{eff} and absolute V_{th} levels with EFT stress at extreme temperatures. This leads to enhanced power dissipation, which may damage the oscillator by thermal runaway particularly for the 5-stage CSVCO.

In Chapter 6, ICIM-CI and ICEM-CE models were developed for several independent analog CMOS structures of the PETER_ESEO IC (i.e., *H*-clock tree, *S*-*R* latch, and 3-stage CSVCO) under HAST and thermal stresses. The PDN block of the developed models was found to be only influenced by thermal stress causing variations in its lumped passive elements, which must be included in the models for improved accuracy. The HAST aging was shown to cause permanent degradation mechanisms, while thermal stress temporarily impacted the MOSFET characteristics (i.e., μ_{eff} and V_{th}) that could lead to soft failures. Those mechanisms were demonstrated to almost exclusively influence the active IA and IB blocks of the conducted emission and immunity models, respectively.

Then, it was shown that the external current emission levels of the *H*-clock tree degrade with aging and temperature increase, which was traced back to the variation in the internal current. Therefore, the need for defining constant proportionality coefficients extracted from simulations (temperature) and measurements (aging) was found to be necessary to model the IA blocks.

Finally, the impact of aging due to HAST as well as elevated temperatures was shown to decrease the conducted EM immunity levels in a given frequency range depending on the functionality of the tested analog block. Specified deviations in the power look-up tables need to be applied to include the influence of aging and thermal stress on the IB block of the ICIM-CI model.

To sum up, for the considered scenarios, those models were demonstrated to quantify the conducted EM emission and immunity levels with enough accuracy under HAST aging and thermal stresses. That paves the way to the inclusion of such deviations in future revised versions of those standards.

7.2 Perspectives

In this manuscript, several aspects related to the conducted EM immunity and emission at the IC level have been addressed. However, there are improvements and open issues that should be further investigated. The following are some of the prospects for future work:

- Through two separate cases studies analyzed (S&H voltage sensor and 6T/9T SRAM cells) in this manuscript, it was verified that SOI is more resilient to temperature variations and has lower power dissipation than bulk technology. However, the mentioned analog structures can be further explored via simulations/measurements to compare their conducted EM immunities (specifically in the power supply) designed in the same size SOI and bulk processes.

- The stability of 6T and 9T SRAM cells relies on power metrics (i.e., SNM and N-curve) which are dependent on the signal integrity of their individual power supplies. The latter topology was proven to be more immune to process and temperature variations. Since both cells are protected by identical ESD protection devices in the designed IC, their conducted immunities can be explored to determine which topologies are more affected by transient EM disturbances such as EFT.

- By comparing two pin-compatible μCs, it was demonstrated that a more modern version of a μC does not necessarily ensure a higher EFT immunity and further EMC analyses are to be performed, particularly when dealing with obsolescence. Non-linear transient immunity models (such as ICIM-CPI) as function of aging and/or obsolescence can be developed to precisely predict the susceptible voltages/currents that may cause failure.

- In this dissertation, multitone conducted EM immunity analysis based on proposed BN models and IC simulations/measurements was successfully carried out for integrated oscillators to characterize and predict the probability of failure. This work can further be extended to other analog/digital blocks of the PETER_ESEO IC such as SRAM cells and latches, in order to validate the scalability of the proposed models for higher order multitone prediction.

- It was proven that environmental stresses such as accelerated aging and temperature were able to cause deviations in the passive/active elements of the ICIM-CI and ICEM-CE models. Reliability characterization and modelling can be carried out to identify the specific degradation mechanisms and transistor parameters that are the most vulnerable to environmental effects.

BIBLIOGRAPHY

[1] M. Ramdani, E. Sicard, A. Boyer, *et al.*, "The electromagnetic compatibility of integrated circuits—past, present, and future", *IEEE Transactions on Electromagnetic Compatibility*, vol. 51, no. 1, pp. 78–100, 2009. DOI: `10.1109/TEMC.2008.2008907`.

[2] S. R. Rao, N. Ishibashi, B. Nayak, *et al.*, "Black-box behavioral DC-DC converter IC emission model", *in 2022 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI)*, 2022, pp. 570–574. DOI: `10.1109/EMCSI39492.2022.9889598`.

[3] J. Xiong, Z. Chen, M. Raginsky, and E. Rosenbaum, "Statistical learning of IC models for system-level ESD simulation", *IEEE Transactions on Electromagnetic Compatibility*, vol. 63, no. 5, pp. 1302–1311, 2021. DOI: `10.1109/TEMC.2021.3076492`.

[4] IEC 62132-4: 2006, *Integrated circuits — Measurement of electromagnetic immunity 150 kHz to 1 GHz — Part 4: Direct RF power injection method.* IEC, 2006.

[5] D. Pommerenke, "Methods for speeding up radiated and conducted immunity tests", *in IEEE International Symposium on Electromagnetic Compatibility. Symposium Record (Cat. No.00CH37016)*, vol. 2, 2000, 587–592 vol.2. DOI: `10.1109/ISEMC.2000.874686`.

[6] Y. Sun, M. Ouyang, X. Sun, and C. Hwang, "Prediction of power supply induced jitter with PDN design parameters", *IEEE Transactions on Electromagnetic Compatibility*, pp. 1–11, 2022. DOI: `10.1109/TEMC.2022.3201899`.

[7] P. Galy and W. Schoenmaker, "In-depth electromagnetic analysis of ESD protection for advanced CMOS technology during fast transient and high-current surge", *IEEE Transactions on Electron Devices*, vol. 61, no. 6, pp. 1900–1906, 2014. DOI: `10.1109/TED.2014.2314485`.

[8] IEC62433-4:2016, *EMC IC modelling – part 4: Models of integrated circuits for RF immunity behavioural simulation – conducted immunity modelling (ICIM-CI)*. IEC, 2016.

[9] IEC62433-2:2017, *EMC IC modelling – part 2: Models of integrated circuits for EMI behavioural simulation – conducted emissions modelling (ICEM-CE)*. IEC, 2017.

[10] A. Boyer, S. Ben Dhia, B. Li, C. Lemoine, and B. Vrignon, "Prediction of long-term immunity of a phase-locked loop", *Journal of Electronic Testing*, vol. 28, no. 6, pp. 791–802, 2012.

[11] A. Boyer, A. C. Ndoye, S. Ben Dhia, L. Guillot, and B. Vrignon, "Characterization of the evolution of IC emissions after accelerated aging", *IEEE Transactions on Electromagnetic Compatibility*, vol. 51, no. 4, pp. 892–900, 2009. DOI: `10.1109/TEMC.2009.2033577`.

[12] N. Z. Haron and S. Hamdioui, "Why is CMOS scaling coming to an end?", *in 2008 3rd International Design and Test Workshop*, 2008, pp. 98–103. DOI: `10.1109/IDT.2008.4802475`.

[13] M. White, "Scaled CMOS technology reliability users guide", Pasadena, CA: Jet Propulsion Laboratory, National Aeronautics and Space . . ., Tech. Rep., 2010.

[14] R. Rodriguez, J. Stathis, and B. Linder, "Modeling and experimental verification of the effect of gate oxide breakdown on CMOS inverters", *in 2003 IEEE International Reliability Physics Symposium Proceedings, 2003. 41st Annual.*, 2003, pp. 11–16. DOI: `10.1109/RELPHY.2003.1197713`.

[15] IEC 60050-161, *International Electrotechnical Vocabulary (IEV) - Part 161: Electromagnetic Compatibility.* IEC standard, 1990.

[16] F. Leferink, J.-K. van der Ven, H. Bergsma, and B. van Leersum, "Risk based EMC for complex systems", *in 2017 XXXIInd General Assembly and Scientific Symposium of the International Union of Radio Science (URSI GASS)*, 2017, pp. 1–4. DOI: `10.23919/URSIGASS.2017.8105016`.

[17] ETN-PETER, [Online] Available: `https://etn-peter.eu/`.

[18] S. Huang and L. Tsang, “Fast electromagnetic analysis of emissions from printed circuit board using broadband green’s function method”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 58, no. 5, pp. 1642–1652, 2016. DOI: `10.1109/TEMC.2016.2565584`.

[19] S. B. Dhia, M. Ramdani, and E. Sicard, *Electromagnetic Compatibility of Integrated Circuits: Techniques for low emission and susceptibility*. Springer Science & Business Media, 2006.

[20] J. Cordi, A. Alaeldine, J.-L. Levant, R. Perdriau, M. Ramdani, and P. Pinel, “Automated extraction of the passive distribution network of an integrated circuit for the assessment of conducted electromagnetic emission”, *in 2008 Asia-Pacific Symposium on Electromagnetic Compatibility and 19th International Zurich Symposium on Electromagnetic Compatibility*, 2008, pp. 36–39. DOI: `10.1109/APEMC.2008.4559805`.

[21] R. Perdriau, M. Ramdani, J.-L. Levant, and A.-M. Trullemans, “EMC evaluation in integrated circuits using VHDL-AMS”, *in 2004 IEEE International Symposium on Industrial Electronics*, vol. 1, 2004, 193–198 vol. 1. DOI: `10.1109/ISIE.2004.1571806`.

[22] T. Ordas, A. Alaeldine, P. Maurine, *et al.*, “Evaluation of countermeasures against electromagnetic analysis”, *in 2009 International Symposium on Electromagnetic Compatibility - EMC Europe*, 2009, pp. 1–4. DOI: `10.1109/EMCEUROPE.2009.5189724`.

[23] J. P. Leca, N. Froidevaux, P. Dupré, G. Jacquemod, and H. Braquet, “EMI measurements, modeling, and reduction of 32-bit high-performance microcontrollers”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 56, no. 5, pp. 1035–1044, 2014. DOI: `10.1109/TEMC.2014.2304744`.

[24] T. Steinecke, H. Koehne, and M. Schmidt, “Behavioral EMI models of complex digital VLSI circuits”, *in 2003 IEEE International Symposium on Electromagnetic Compatibility, 2003. EMC ’03.*, vol. 2, 2003, 848–851 Vol.2. DOI: `10.1109/ICSMC2.2003.1429040`.

[25] L. Dražan, R. Križan, and M. Popela, “Design and testing of a low-tech DEW generator for determining electromagnetic immunity of standard electronic circuits”, *Energies*, vol. 14, no. 11, p. 3090, 2021.

[26] A. Hosseinbeig, O. H. Izadi, S. Shinde, *et al.*, "A study on correlation between near-field EMI scan and ESD susceptibility of ICs", *in 2017 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI)*, 2017, pp. 169–174. DOI: `10.1109/ISEMC.2017.8077861`.

[27] J.-M. Redouté and M. Steyaert, *EMC of analog integrated circuits*. Springer Science & Business Media, 2009.

[28] M. Deobarro, B. Vrignon, S. B. Dhia, and A. Boyer, "Use of on-chip sampling sensor to evaluate conducted RF disturbances propagated inside an integrated circuit", *EMC Compo*, vol. 9, 2009.

[29] S. Delmas-Bendhia, F. Caignet, and E. Sicard, "A new method for measuring signal integrity in CMOS ICs", *Microelectronics international*, 2000.

[30] B. Vrignon and S. B. Dhia, "On-chip sampling sensors for high frequency signals measurement: Evolution and improvements", *in Proceedings of the Fifth IEEE International Caracas Conference on Devices, Circuits and Systems, 2004.*, IEEE, vol. 1, 2004, pp. 270–275.

[31] S. Dhia, A. Boyer, B. Vrignon, M. Deobarro, and T. V. Dinh, "On-chip noise sensor for integrated circuit susceptibility investigations", *IEEE Transactions on Instrumentation and Measurement*, vol. 61, no. 3, pp. 696–707, 2012. DOI: `10.1109/TIM.2011.2172116`.

[32] V. Bendre and A. Kureshi, "Performance analysis of operational transconductance amplifier at 180 nm technology", *in 2016 Second International Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH)*, 2016, pp. 271–276. DOI: `10.1109/CIPECH.2016.7918781`.

[33] P. G. A. Jespers and B. Murmann, *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables*. Cambridge University Press, 2017. DOI: `10.1017/9781108125840`.

[34] F. Fiori and F. Musolino, "Investigations on the correlation between IC-conducted emission and chip-level power supply current", *IEEE Transactions on Electromagnetic Compatibility*, vol. 47, no. 1, pp. 28–33, 2005. DOI: `10.1109/TEMC.2004.842203`.

[35] B.-J. Bang, H. Kwon, Y. H. Kim, K. Cho, and H.-S. Kim, “Statistical modeling of read static noise margin for 6-Transistor SRAM cell”, *in 2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2019, pp. 1–4. DOI: `10.1109/ISCAS.2019.8702663`.

[36] K. Agarwal and S. Nassif, “Statistical analysis of SRAM cell stability”, *in Proceedings of the 43rd annual design automation conference*, 2006, pp. 57–62.

[37] G. Prasad, B. chandra Mandi, P. Ramu, T. V. Sowrabh, and A. H. Kumar, “Statistical analysis of 5t SRAM cell for low power and less area SRAM based cache memory for IoT applications”, *in 2020 First International Conference on Power, Control and Computing Technologies (ICPC2T)*, IEEE, 2020, pp. 368–372.

[38] R. Saeidi, M. Sharifkhani, and K. Hajsadeghi, “Statistical analysis of read static noise margin for near/sub-threshold SRAM cell”, *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 12, pp. 3386–3393, 2014. DOI: `10.1109/TCSI.2014.2327334`.

[39] V. K. Joshi and H. C. Lobo, “Comparative study of 7T, 8T, 9T and 10T SRAM with conventional 6T SRAM cell using 180 nm technology”, *in Advanced Computing and Communication Technologies*, Springer, 2016, pp. 25–40.

[40] I. Rizvi, Nidhi, R. Mishra, and M. S. Hashmi, “Design and analysis of a noise induced 6T SRAM cell”, *in 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*, 2016, pp. 4209–4213. DOI: `10.1109/ICEEOT.2016.7755510`.

[41] V. P.-H. Hu, “Reliability-tolerant design for ultra-thin-body GeOI 6T SRAM cell and sense amplifier”, *IEEE Journal of the Electron Devices Society*, vol. 5, no. 2, pp. 107–111, 2017. DOI: `10.1109/JEDS.2016.2644724`.

[42] A. Bhaskar, “Design and analysis of low power SRAM cells”, *in 2017 Innovations in Power and Advanced Computing Technologies (i-PACT)*, 2017, pp. 1–5. DOI: `10.1109/IPACT.2017.8244888`.

[43] S. S.R., B. R. S., Samiksha, R. Banu, and P. Shubham, “Design and performance analysis of 6T SRAM cell in 22 nm CMOS and FINFET technology nodes”, *in 2017 International Conference on Recent Advances in Electronics and Communication Technology (ICRAECT)*, 2017, pp. 38–42. DOI: `10.1109/ICRAECT.2017.65`.

[44] A. K. Gupta and A. Acharya, “Exploration of 9T SRAM cell for in memory computing application”, *in 2021 Devices for Integrated Circuit (DevIC)*, 2021, pp. 461–465. DOI: `10.1109/DevIC50843.2021.9455838`.

[45] B. Razavi, “Chapter 14 - Oscillators”, *in Design of Analog CMOS Integrated Circuits*, New York, NY 10121: McGraw-Hill Education, 2001, ISBN: 978-0-07-252493-2.

[46] T. Dubois, J.-J. Laurin, J. Raoult, and S. Jarrix, “Effect of low and high power continuous wave electromagnetic interference on a microwave oscillator system: From VCO to PLL to QPSK receiver”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 56, no. 2, pp. 286–293, 2014. DOI: `10.1109/TEMC.2013.2280670`.

[47] J.-J. Laurin, S. Zaky, and K. Balmain, “EMI-induced failures in crystal oscillators”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 33, no. 4, pp. 334–342, 1991. DOI: `10.1109/15.99115`.

[48] K. Mbarek, S. Ghedira, F. O. Rziga, and K. Besbes, “Design and analysis of nonvolatile memristor-based S-R latch”, *in 2020 IEEE International Conference on Design Test of Integrated Micro Nano-Systems (DTS)*, 2020, pp. 1–5. DOI: `10.1109/DTS48731.2020.9196039`.

[49] M. Koohestani, N. Pires, A. K. Skrivervik, and A. A. Moreira, “Bandwidth enhancement of a wearable UWB antenna near a human arm”, *Microwave and Optical Technology Letters*, vol. 55, no. 12, pp. 2965–2967, 2013.

[50] M. Koohestani, A. A. Moreira, and A. K. Skrivervik, “Feeding structure influence on performance of two UWB antennas near a human arm”, *in The 8th European Conference on Antennas and Propagation (EuCAP 2014)*, 2014, pp. 834–836. DOI: `10.1109/EuCAP.2014.6901891`.

[51] S. Basu and L. Hayden, “An SOLR calibration for accurate measurement of orthogonal on-wafer DUTs”, *in 1997 IEEE MTT-S International Microwave Symposium Digest*, vol. 3, 1997, 1335–1338 vol.3. DOI: `10.1109/MWSYM.1997.596575`.

[52] G. Engen and C. Hoer, “Thru-Reflect-Line: An improved technique for calibrating the dual six-port automatic network analyzer”, *IEEE Transactions on Microwave Theory and Techniques*, vol. 27, no. 12, pp. 987–993, 1979. DOI: `10.1109/TMTT.1979.1129778`.

[53] A. Rumiantsev and N. Ridler, “VNA calibration”, *IEEE Microwave Magazine*, vol. 9, no. 3, pp. 86–99, 2008. DOI: `10.1109/MMM.2008.919925`.

[54] A. Ramezani, Q. M. Khan, and H. Pues, “A new TRL/TRM PCB-based calibration method for on-board devices under test (DUTs)”, *in 2021 13th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, 2022, pp. 112–116. DOI: `10.1109/EMCCompo52133.2022.9758617`.

[55] T. F. S. M. C. High Frequency (Up to 40 GHz) Resistor, [Online] Available: `https://4donline.ihs.com/images/VipMasterIC/IC/VISH/VISH-S-A0010804029/VISH-S-A0010804029-1.pdf?hkey=6D3A4C79FDBF58556ACFDE234799DDF0`.

[56] X. Li, M. Wang, J. Wu, *et al.*, “Impact of SOI and SI technologies on EMC of CAN controller”, *in Proc. 12th Int. Workshop on the Electromagn. Compat. of Integr. Circuits (EMC Compo)*, 2019, pp. 102–104.

[57] B. Li, K. Zhao, J. Wu, *et al.*, “Electromagnetic susceptibility characterization of double SOI device”, *Microelectronics Reliability*, vol. 64, pp. 168–171, 2016.

[58] Y.-H. Koh, J.-H. Choi, M.-H. Nam, and J.-W. Yang, “Body-contacted SOI MOSFET structure with fully bulk CMOS compatible layout and process”, *IEEE Electron Device Letters*, vol. 18, no. 3, pp. 102–104, 1997. DOI: `10.1109/55.556094`.

[59] R. K. Singh, A. Saxena, and M. Rastogi, “Silicon on insulator technology review”, *International Journal of Engineering Sciences & Emerging Technologies*, vol. 1, no. 1, pp. 1–16, 2011.

[60] L. Franca-Neto, P. Pardy, M. Ly, *et al.*, "Enabling high-performance mixed-signal system-on-a-chip (SoC) in high performance logic CMOS technology", *in 2002 Symposium on VLSI Circuits. Digest of Technical Papers (Cat. No. 02CH37302)*, IEEE, 2002, pp. 164–167.

[61] J. Ankarcrona, L. Vestling, K.-H. Eklund, and J. Olsson, "Low resistivity SOI for substrate crosstalk reduction", *IEEE transactions on electron devices*, vol. 52, no. 8, pp. 1920–1922, 2005.

[62] G. K. Celler and S. Cristoloveanu, "Frontiers of silicon-on-insulator", *Journal of Applied Physics*, vol. 93, no. 9, pp. 4955–4978, 2003.

[63] Q. M. Khan, R. Perdriau, M. Ramdani, and M. Koohestani, "A comparative study of on-chip CMOS S&H voltage sensors for power integrity: SOI vs. bulk", *in 2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, 2021, pp. 911–916. DOI: `10.1109/EMC/SI/PI/EMCEurope52599.2021.9559242`.

[64] Q. M. Khan, R. Perdriau, M. Ramdani, and M. Koohestani, "A comparative performance analysis of 6T & 9T SRAM integrated circuits: SOI vs. bulk", *IEEE Letters on Electromagnetic Compatibility Practice and Applications*, vol. 4, no. 2, pp. 25–30, 2022. DOI: `10.1109/LEMCPA.2022.3163963`.

[65] P. Simonen, A. Heinonen, M. Kuulusa, and J. Nurmi, "Comparison of bulk and SOI CMOS technologies in a DSP processor circuit implementation", *in ICM 2001 Proceedings. The 13th International Conference on Microelectronics.*, 2001, pp. 107–110. DOI: `10.1109/ICM.2001.997499`.

[66] M. Deobarro, B. Vrignon, S. Ben Dhia, and J. Shepherd, "On-chip sampling and EMC modeling of I/Os switching to evaluate conducted RF disturbances propagation", *in 2010 Asia-Pacific International Symposium on Electromagnetic Compatibility*, 2010, pp. 1032–1038. DOI: `10.1109/APEMC.2010.5475756`.

[67] J.-P. Raskin, "SOI technology: An opportunity for RF designers?", *in Proceedings of Technical Program - 2014 International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, 2014, pp. 1–2. DOI: `10.1109/VLSI-TSA.2014.6839644`.

[68] A. Alaeldine, L. Bouchelouk, R. Perdriau, and M. Ramdani, “A study of the conducted interference induced by near-field injection in integrated circuits”, *in EMC Compo 2009*, 2009.

[69] S. Sigroha and B. Krishan, “A high bandwidth low power supply CMOS operational amplifier”, *IJSRD Int. Jrnl. Scientific Res. & Development*, vol. 3, no. 02, 2015.

[70] N. Baptistat, K. Abouda, G. Duchamp, and T. Dubois, “Effects of process-voltage-temperature (PVT) variations on low-side MOSFET circuit conducted emission”, *in 2019 12th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, 2019, pp. 213–215. DOI: `10.1109/EMCCompo.2019.8919728`.

[71] S. Onaissi, F. Taraporevala, J. Liu, and F. Najm, “A fast approach for static timing analysis covering all PVT corners”, *in 2011 48th ACM/EDAC/IEEE Design Automation Conference (DAC)*, 2011, pp. 777–782.

[72] J. B. Kuo and S.-C. Lin, *Low-voltage SOI CMOS VLSI devices and circuits.* John Wiley & Sons, 2004.

[73] P. Athe and S. Dasgupta, “A comparative study of 6T, 8T and 9T decanano SRAM cell”, *in 2009 IEEE Symposium on Industrial Electronics & Applications*, vol. 2, 2009, pp. 889–894. DOI: `10.1109/ISIEA.2009.5356318`.

[74] S. Akashe, N. K. Tiwari, and R. Sharma, “Simulation and stability analysis of 6T and 9T SRAM cell in 45 nm era”, *in 2012 2nd International Conference on Power, Control and Embedded Systems*, 2012, pp. 1–6. DOI: `10.1109/ICPCES.2012.6508061`.

[75] V. Choudhary and D. S. Yadav, “Analysis of power, delay and SNM of 6T & 8T SRAM cells”, *in 2021 5th International Conference on Electronics, Communication and Aerospace Technology (ICECA)*, 2021, pp. 78–82. DOI: `10.1109/ICECA52323.2021.9676022`.

[76] E. Grossar, M. Stucchi, K. Maex, and W. Dehaene, “Read stability and writeability analysis of SRAM cells for nanometer technologies”, *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2577–2588, 2006. DOI: `10.1109/JSSC.2006.883344`.

[77] G. K. Reddy, K. Jainwal, J. Singh, and S. P. Mohanty, "Process variation tolerant 9T SRAM bitcell design", *in Thirteenth International Symposium on Quality Electronic Design (ISQED)*, 2012, pp. 493–497. DOI: `10.1109/ISQED.2012.6187539`.

[78] A. Gaadhe, U. Shirode, and R. Kanphade, "The stability performance analysis of SRAM cell topologies in 90 nm and 130 nm CMOS technology", *in 2021 International Conference on Emerging Smart Computing and Informatics (ESCI)*, 2021, pp. 733–736. DOI: `10.1109/ESCI50559.2021.9396973`.

[79] K. Samsudin, B. Cheng, A. Brown, S. Roy, and A. Asenov, "Impact of random dopant induced fluctuations on sub-15 nm UTB SOI 6T SRAM cells", *in 2005 IEEE International SOI Conference Proceedings*, 2005, pp. 61–62. DOI: `10.1109/SOI.2005.1563533`.

[80] P. Roche, G. Gasiot, K. Forbes, V. O'Sullivan, and V. Ferlet, "Comparisons of soft error rate for SRAMs in commercial SOI and bulk below the 130-nm technology node", *IEEE Transactions on Nuclear Science*, vol. 50, no. 6, pp. 2046–2054, 2003. DOI: `10.1109/TNS.2003.821588`.

[81] M. A. Aziz, F. Salehuddin, A. Zain, K. Kaharudin, and S. Radzi, "Comparison of electrical characteristics between bulk MOSFET and silicon-on-insulator (SOI) MOSFET", *Journal of Telecommunication, Electronic and Computer Engineering (JTEC)*, vol. 6, no. 2, pp. 45–49, 2014.

[82] G. Prasad, D. Tandon, Isha, B. C. Mandi, and M. Ali, "Process variation analysis of 10T SRAM cell for low power, high speed cache memory for IoT applications", *in 2020 7th International Conference on Signal Processing and Integrated Networks (SPIN)*, 2020, pp. 891–895. DOI: `10.1109/SPIN48934.2020.9070999`.

[83] L. Devaraj, Q. M. Khan, A. R. Ruddle, A. P. Duffy, R. Perdriau, and M. Koohestani, "Application of probabilistic models for multitone electromagnetic immunity analysis", *IEEE Transactions on Electromagnetic Compatibility*, vol. 64, no. 6, pp. 2067–2079, 2022. DOI: `10.1109/TEMC.2022.3211458`.

[84] L. Devaraj, Q. M. Khan, A. R. Ruddle, A. P. Duffy, R. Perdriau, and M. Koohestani, "Improvements proposed to noisy-OR derivatives for multicausal analysis: A case study of simultaneous electromagnetic disturbances", *International Journal of Approximate Reasoning*, 2023, (under review).

[85] Q. M. Khan, L. Devaraj, M. Koohestani, A. R. Ruddle, M. Ramdani, and R. Perdriau, “Synergistic effect of multitone EMI on the conducted immunity of integrated oscillators”, *IEEE Letters on Electromagnetic Compatibility Practice and Applications*, vol. 4, no. 3, pp. 77–82, 2022. DOI: `10.1109/LEMCPA.2022.3175433`.

[86] Q. M. Khan, L. Devaraj, R. Perdriau, *et al.*, “Experimental characterization of multitone EM immunity of integrated oscillators under thermal stress”, *IEEE Access*, vol. 10, pp. 83 898–83 915, 2022. DOI: `10.1109/ACCESS.2022.3197659`.

[87] K. Armstrong, “Testing for immunity to simultaneous disturbances and similar issues for risk managing EMC”, *in 2012 IEEE International Symposium on Electromagnetic Compatibility*, 2012, pp. 121–126. DOI: `10.1109/ISEMC.2012.6351798`.

[88] L. Devaraj, Q. M. Khan, A. R. Ruddle, and A. P. Duffy, “Comparing simulated impact of single frequency and multitone EMI for an integrated circuit”, *in 2021 13th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, 2022, pp. 107–111. DOI: `10.1109/EMCCompo52133.2022.9758612`.

[89] K. Armstrong, “Validation, verification and immunity testing techniques for EMC for functional safety”, *in 2007 IEEE International Symposium on Electromagnetic Compatibility*, 2007, pp. 1–6. DOI: `10.1109/ISEMC.2007.64`.

[90] A. Biondi, H. Rogier, D. Vande Ginste, and D. De Zutter, “Multi-tone EMC testing strategy for RF-devices”, *in Proc. 2012 IEEE Elect. Des. of Adv. Packag. and Syst. Symp. (EDAPS)*, 2012, pp. 89–92. DOI: `10.1109/EDAPS.2012.6469385`.

[91] M. Mardiguian, “Combined effects of several, simultaneous, EMI couplings”, *in Proc. IEEE Int. Symp. on Electromagn. Compat. Symp. Record (Cat. No.00CH37016)*, vol. 1, 2000, 181–184 vol.1. DOI: `10.1109/ISEMC.2000.875559`.

[92] G. Barth, “Benefits of multitone EMC immunity testing”, *Int. Jrnl. RF Microw. Comput.-Aided Eng.*, vol. 26, pp. 355–358, May 2016. DOI: `10.1002/mmce.20986`.

[93] IEC 61000-4-3:2020-09 (EN), *Electromagnetic compatibility (EMC) - Testing and measurement techniques. Radiated, radio-frequency, electromagnetic field immunity test.* British Standards Institute, 2020.

[94] J. Lemmer and D. Gossink, “Recursive noisy OR - a rule for estimating complex probabilistic interactions”, *IEEE Transactions on Systems, Man, and Cybernetics, Part B (Cybernetics)*, vol. 34, no. 6, pp. 2252–2261, 2004. DOI: `10.1109/TSMCB.2004.834424`.

[95] J. Pearl, “Chapter 4 - belief updating by network propagation”, *in Probabilistic Reasoning in Intelligent Systems*, J. Pearl, Ed., San Francisco (CA): Morgan Kaufmann, 1988, pp. 143–237, ISBN: 978-0-08-051489-5. DOI: `https://doi.org/10.1016/B978-0-08-051489-5.50010-2`. [Online]. Available: `https://www.sciencedirect.com/science/article/pii/B9780080514895500102`.

[96] P. Judea, “Fusion, propagation, and structuring in belief networks”, *Artificial Intelligence*, vol. 29, no. 3, pp. 241–288, 1986, ISSN: 0004-3702. DOI: `https://doi.org/10.1016/0004-3702(86)90072-X`. [Online]. Available: `https://www.sciencedirect.com/science/article/pii/000437028690072X`.

[97] BS EN 61508-1:2010, *Functional safety of electrical/electronic/programmable electronic safety-related systems.* British Standards Institute, Jun. 2010.

[98] D. Ward, I. Ibarra, and A. Ruddle, “Threat analysis and risk assessment in automotive cyber security”, vol. 6(2), SAE Int. J. Passeng. Cars – Electron. Electr. Syst., 2013, pp. 507–513. DOI: `https://doi.org/10.4271/2013-01-1415`.

[99] F. Díez and M. Druzdzel, “Canonical probabilistic models for knowledge engineering”, May 2007.

[100] V. Anand and S. M. Downs, “An empirical validation of recursive noisy OR (RNOR) rule for asthma prediction”, *in Proc. AMIA Annu. Symp.*, Nov. 2010, pp. 16–20.

[101] M. Koohestani, R. Perdriau, J.-L. Levant, and M. Ramdani, “A novel passive cost-effective technique to improve radiated immunity on PCBs”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 61, no. 6, pp. 1733–1739, 2019. DOI: `10.1109/TEMC.2018.2882732`.

[102] A. Lavarda and B. Deutschmann, “Direct power injection (DPI) simulation framework and postprocessing”, *in 2015 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2015, pp. 1248–1253. DOI: `10.1109/ISEMC.2015.7256349`.

[103] O. Aiello and P. Crovetti, “Characterization of the susceptibility to EMI of a BMS IC for electric vehicles by direct power and bulk current injection”, *IEEE Letters on Electromagnetic Compatibility Practice and Applications*, vol. 3, no. 3, pp. 101–107, 2021. DOI: `10.1109/LEMCPA.2021.3085765`.

[104] Cadence, *Spectre Simulation Platform*, `https://www.cadence.com/ko_KR/home/tools/custom-ic-analog-rf-design/circuit-simulation/spectre-simulation-platform.html`, Accessed: 2021-04-12, 2021.

[105] A. Boyer and É. Sicard, *Basis of Electromagnetic Compatibility of Integrated Circuits: A Modelling Approach Using IC-EMC* (Pour l’ingénieur). Presses Universitaires du Midi, 2017, ISBN: 9782810705221. [Online]. Available: `https://books.google.co.uk/books?id=LewxswEACAAJ`.

[106] Q. M. Khan, A. Ramezani, M. Koohestani, M. Ramdani, and R. Perdriau, “A comparison among DPI immunities of multi-stage CSVCOs and ring oscillators”, *in Proc. 2021 13th Int. Workshop on the Electromagn. Compat. of Integr. Circuits (EMC Compo)*, 2022, pp. 123–127.

[107] D. Koller and N. Friedman, *Probabilistic Graphical Models: Principles and Techniques - Adaptive Computation and Machine Learning.* MIT Press, 2009, ISBN: 0262013193.

[108] J. Lemmer and D. Gossink, “Recursive noisy OR - a rule for estimating complex probabilistic interactions”, *IEEE Transactions on Systems, Man, and Cybernetics, Part B (Cybernetics)*, vol. 34, no. 6, pp. 2252–2261, 2004. DOI: `10.1109/TSMCB.2004.834424`.

[109] T. Hino and H. Watanabe, “Analysis of RF noise in LDO and establishment of noise immunity”, *in 2019 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2019, pp. 508–512. DOI: `10.1109/EMCEurope.2019.8872083`.

[110] M. Magerl, C. Stockreiter, and A. Baric, “Influence of RF disturbance phase on amplifier DPI characteristics”, *in 2017 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2017, pp. 1–5. DOI: `10.1109/EMCEurope.2017.8094756`.

[111] J. Wu, H. Zhang, H. Wang, L. Zheng, H. Ma, and B. Li, “DPI immunity of bandgap in Si and SOI technologies”, *in 2017 11th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMCCompo)*, 2017, pp. 197–199. DOI: `10.1109/EMCCompo.2017.7998110`.

[112] A. Ayed, T. Dubois, J.-L. Levant, and G. Duchamp, “Immunity measurement and modeling of an ADC embedded in a microcontroller using RFIP technique”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 57, no. 5, pp. 955–962, 2015. DOI: `10.1109/TEMC.2015.2422140`.

[113] H. Pues and C. Gazda, “A black-box measurement-based modeling method for the RF emission and immunity behavior of ICs”, *in 2015 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2015, pp. 1002–1006. DOI: `10.1109/ISEMC.2015.7256303`.

[114] A. Biondi, F. Declercq, D. De Zutter, H. Rogier, and L. Vallozzi, “Electromagnetic compatibility aware design and testing of intermodulation distortion under multiple co-located sources illumination”, *IET Science, Measurement & Technology*, vol. 6, no. 2, pp. 105–112, 2012.

[115] L. Fu, Z. Yan, C. Fu, and D. Su, “Extraction and analysis of conducted electromagnetic susceptibility elements of integrated circuits”, *IEEE Access*, vol. 9, pp. 149 125–149 136, 2021. DOI: `10.1109/ACCESS.2021.3125051`.

[116] I. P. Tolić, J. Mikulić, G. Schatzberger, and A. Barić, “Design of CMOS temperature sensors based on ring oscillators in 180-nm and 110-nm technology”, *in 2020 43rd International Convention on Information, Communication and Electronic Technology (MIPRO)*, 2020, pp. 104–108. DOI: `10.23919/MIPRO48935.2020.9245244`.

[117] R. A. WaIunj, S. D. Pable, and G. K. Kharate, “Design of robust ultra-low power CMOS voltage controlled ring oscillator with enhanced performance”, *in 2018 International Conference On Advances in Communication and Computing Technology (ICACCT)*, 2018, pp. 235–239. DOI: `10.1109/ICACCT.2018.8529360`.

[118] N. Baptistat, K. Abouda, G. Duchamp, and T. Dubois, “Effects of process-voltage-temperature (PVT) variations on low-side MOSFET circuit conducted emission”, *in 2019 12th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, 2019, pp. 213–215. DOI: `10.1109/EMCCompo.2019.8919728`.

[119] P. Baros, P. Horsky, and P. Kamenicky, “Introduction to EMC simulations of analog ICs”, *in 2008 International Symposium on Electromagnetic Compatibility - EMC Europe*, 2008, pp. 1–6. DOI: `10.1109/EMCEUROPE.2008.4786902`.

[120] J. Hwang, Y. Han, H. Park, W. Nah, and S. Kim, “Radiated electromagnetic immunity analysis of VCO using IC stripline method”, *in 2015 10th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, 2015, pp. 147–151. DOI: `10.1109/EMCCompo.2015.7358347`.

[121] W. Greason, “Analysis of electrostatic discharge for the human body and an automobile environment”, *IEEE Transactions on Industry Applications*, vol. 36, no. 2, pp. 517–525, 2000. DOI: `10.1109/28.833769`.

[122] W. Stadler, S. Bargstadt-Franke, T. Brodbeck, *et al.*, “From the ESD robustness of products to the system ESD robustness”, *in 2004 Electrical Overstress/Electrostatic Discharge Symposium*, 2004, pp. 1–8. DOI: `10.1109/EOSESD.2004.5272634`.

[123] Z. Lixia and L. Wenfei, “Study on the forming mechanism and safeguard procedures of electrical fast transient burst”, *in The 2nd International Conference on Information Science and Engineering*, 2010, pp. 2399–2402. DOI: `10.1109/ICISE.2010.5689644`.

[124] IEC 61000-4-4, *EMC-Part 4-4: Testing and Measurement Techniques-Electrical Fast Transient/Burst Immunity Test.* IEC, 2004.

[125] Q. M. Khan, M. Koohestani, M. Ramdani, and R. Perdriau, “Obsolescence in EMC risk assessment: A case study on EFT immunity of microcontrollers”, *in 2020 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2020, pp. 1–6. DOI: `10.1109/EMCEUROPE48519.2020.9245783`.

[126] Q. M. Khan, M. Koohestani, and R. Perdriau, “Influence of temperature on the EFT immunity of multistage integrated oscillators”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 65, no. 1, pp. 138–148, 2023. DOI: `10.1109/TEMC.2022.3225540`.

[127] S. Bauer, B. Deutschmann, and G. Winkler, “Prediction of the robustness of integrated circuits against EFT/BURST”, *in 2015 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2015, pp. 45–49. DOI: `10.1109/ISEMC.2015.7256130`.

[128] J. Wu, Y. Li, H. Zhang, H. Li, A. Zhang, and P. Wang, “Impulse immunity of interfaces between intelligent media processors and DDR3 SDRAM memory”, *in 2019 12th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, 2019, pp. 150–152. DOI: `10.1109/EMCCompo.2019.8919806`.

[129] J. Wu, B. Li, W. Zhu, H. Wang, and L. Zheng, “Investigations on the EFT immunity of microcontrollers with different architectures”, *Microelectronics Reliability*, vol. 76, pp. 708–713, 2017.

[130] J. Wu, C. Li, B. Li, W. Zhu, and H. Wang, “Microcontroller susceptibility variations to EFT burst during accelerated aging”, *Microelectronics Reliability*, vol. 64, pp. 210–214, 2016.

[131] J. Su, J. Li, J. Wu, and C. Wang, “Investigation of reproducibility and repeatability issue on EFT test at IC level to microcontrollers”, *in CCF National Conference on Computer Engineering and Technology*, Springer, 2013, pp. 171–179.

[132] C. Leveugle and T. Weyl, “Implementation methodology of industrial and automotive ESD, EFT and surge generator models which predict EMC robustness on ICs and systems”, *in 2017 39th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)*, 2017, pp. 1–9. DOI: `10.23919/EOSESD.2017.8073453`.

[133] M. A. datasheet., [Online] Available: `https://www.microchip.com/www.products/en/AT91sam7s256`.

[134] M. A. datasheet., [Online] Available: `https://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-6500-32-bit-Cortex-M3-Microcontroller-SAM3S4-SAM3S2-SAM3S1_Datasheet.pdf`.

[135] IEC 62132-2, *Integrated circuits, measurement of electromagnetic immunity, 150 kHz to 1 GHz, Measurement of radiated immunity - TEM cell and wideband TEM cell method.* IEC, 2010.

[136] U. M. IMU4000., [Online] Available: `https://www.eltest.hu/pdf/IMU4000.pdf`.

[137] M. Amellal, M. Ramdani, R. Perdriau, M. Medina, M. Drissi, and A. Ahaitouf, "The conducted immunity of SPI EEPROM memories", *in 2013 International Symposium on Electromagnetic Compatibility*, 2013, pp. 926–930.

[138] A. Durier, P. Fernandez-Lopez, J.-L. Levant, and C. Marot, "ICIM-CPI: Integrated circuits immunity model: Conducted pulse immunity: Description, extraction and example", *in 2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC)*, 2018, pp. 695–700. DOI: `10.1109/ISEMC.2018.8393871`.

[139] Y.-S. Shen and M.-D. Ker, "The impact of holding voltage of transient voltage suppressor (TVS) on signal integrity of microelectronics system with CMOS ICs under system-level ESD and EFT/Burst tests", *IEEE Transactions on Electron Devices*, vol. 68, no. 5, pp. 2152–2159, 2021. DOI: `10.1109/TED.2021.3063208`.

[140] C.-C. Yen and M.-D. Ker, "The effect of IEC-like fast transients on *RC* -triggered ESD power clamps", *IEEE Transactions on Electron Devices*, vol. 56, no. 6, pp. 1204–1210, 2009. DOI: `10.1109/TED.2009.2017625`.

[141] H.-N. Lin, T.-H. Ho, Y.-C. Huang, *et al.*, "EFT transient noise model and protection analysis from chip to system level on power distribution", *in 2020 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2020, pp. 1–4. DOI: `10.1109/EMCEUROPE48519.2020.9245631`.

[142] R. Troutman and H. Zappe, "A transient analysis of latchup in bulk CMOS", *IEEE Transactions on Electron Devices*, vol. 30, no. 2, pp. 170–179, 1983. DOI: `10.1109/T-ED.1983.21091`.

[143] C.-C. Chen and M.-D. Ker, "Optimization design on active guard ring to improve latch-up immunity of CMOS integrated circuits", *IEEE Transactions on Electron Devices*, vol. 66, no. 4, pp. 1648–1655, 2019. DOI: `10.1109/TED.2019.2898317`.

[144] C.-C. Yen, M.-D. Ker, and T.-Y. Chen, "Transient-induced latchup in CMOS ICs under electrical fast-transient test", *IEEE Transactions on Device and Materials Reliability*, vol. 9, no. 2, pp. 255–264, 2009. DOI: `10.1109/TDMR.2009.2015938`.

[145] J. Zhang, J. Koo, R. Moseley, *et al.*, "Modeling injection of electrical fast transients into power and IO pins of ICs", *IEEE Transactions on Electromagnetic Compatibility*, vol. 56, no. 6, pp. 1576–1584, 2014. DOI: `10.1109/TEMC.2014.2332499`.

[146] J. Koo, L. Han, S. Herrin, *et al.*, "A nonlinear microcontroller power distribution network model for the characterization of immunity to electrical fast transients", *IEEE Transactions on Electromagnetic Compatibility*, vol. 51, no. 3, pp. 611–619, 2009. DOI: `10.1109/TEMC.2009.2023670`.

[147] P. Galy and W. Schoenmaker, "In-depth electromagnetic analysis of ESD protection for advanced CMOS technology during fast transient and high-current surge", *IEEE Transactions on Electron Devices*, vol. 61, no. 6, pp. 1900–1906, 2014. DOI: `10.1109/TED.2014.2314485`.

[148] M. Fontana and T. H. Hubing, "Characterization of CAN network susceptibility to EFT transient noise", *IEEE Transactions on Electromagnetic Compatibility*, vol. 57, no. 2, pp. 188–194, 2015. DOI: `10.1109/TEMC.2014.2377235`.

[149] S. Bauer, W. Renhart, O. Bíró, *et al.*, "Investigation of SPICE models for overvoltage protection devices with respect to fast transients", *IEEE Letters on Electromagnetic Compatibility Practice and Applications*, vol. 1, no. 1, pp. 20–25, 2019. DOI: `10.1109/LEMCPA.2019.2912587`.

[150] K. Kim and A. A. Iliadis, “Critical upsets of CMOS inverters in static operation due to high-power microwave interference”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 49, no. 4, pp. 876–885, 2007. DOI: `10.1109/TEMC.2007.908820`.

[151] X. Gao, C. Sui, S. Hemmady, *et al.*, “Modeling static delay variations in push–pull CMOS digital logic circuits due to electrical disturbances in the power supply”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 57, no. 5, pp. 1179–1187, 2015. DOI: `10.1109/TEMC.2015.2428272`.

[152] C. Furbock, N. Seliger, D. Pogany, *et al.*, “Backside laserprober characterization of thermal effects during high current stress in smart power ESD protection devices”, *in International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217)*, 1998, pp. 691–694. DOI: `10.1109/IEDM.1998.746451`.

[153] C. Furbock, D. Pogany, M. Litzenberger, *et al.*, “Interferometric temperature mapping during ESD stress and failure analysis of smart power technology ESD protection devices”, *in Electrical Overstress/Electrostatic Discharge Symposium Proceedings. 1999 (IEEE Cat. No.99TH8396)*, 1999, pp. 241–250. DOI: `10.1109/EOSESD.1999.819067`.

[154] M. Miao, Y. Zhou, J. A. Salcedo, J.-J. Hajjar, and J. J. Liou, “A new method to estimate failure temperatures of semiconductor devices under electrostatic discharge stresses”, *IEEE Electron Device Letters*, vol. 37, no. 11, pp. 1477–1480, 2016. DOI: `10.1109/LED.2016.2608328`.

[155] X. Zheng, L. Wu, Y. Guan, and X. Li, “Analysis of the degradation of MOSFETs in switching mode power supply by characterizing source oscillator signals”, *Mathematical Problems in Engineering*, vol. 2013, 2013.

[156] Q. M. Khan, M. Koohestani, J.-L. Levant, M. Ramdani, and R. Perdriau, “Validation of IC conducted emission and immunity models including aging and thermal stress”, *IEEE Transactions on Electromagnetic Compatibility*, 2023. DOI: `10.1109/TEMC.2023.3253385`.

[157] M. Koohestani, A. K. Skrivervik, and M. Ramdani, “An analytical approach for the estimation of the far-field reduction obtained by placing closed conductor loops in proximity to a chip”, *IEEE Transactions on Electromagnetic*

Compatibility, vol. 63, no. 5, pp. 1384–1394, 2021. DOI: `10.1109/TEMC.2021.3072235`.

[158] N. Czepl, B. Deutschmann, and A. Michalowska-Forsyth, “Influence of ionizing radiation on the conducted electromagnetic emission of integrated circuits”, *Microelectronics Reliability*, vol. 126, p. 114 335, 2021.

[159] S. R. Rao, N. Ishibashi, B. Nayak, *et al.*, “Black-box behavioral DC-DC converter IC emission model”, *in 2022 IEEE International Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMCSI)*, 2022, pp. 570–574. DOI: `10.1109/EMCSI39492.2022.9889598`.

[160] W. Mao, W. Li, Y. Tian, B. Vrignon, J. Shepherd, and R. Wang, “A pad ICIM model for EMC immunity simulation”, *in 2012 Asia-Pacific Symposium on Electromagnetic Compatibility*, 2012, pp. 397–400. DOI: `10.1109/APEMC.2012.6237993`.

[161] E. A. Amerasekera and F. N. Najm, *Failure Mechanisms in Semiconductor Devices.* Wiley, 1997.

[162] M. White, D. Vu, D. Nguyen, R. Ruiz, Y. Chen, and J. B. Bernstein, “Product reliability trends, derating considerations and failure mechanisms with scaled CMOS”, *in 2006 IEEE International Integrated Reliability Workshop Final Report*, 2006, pp. 156–159. DOI: `10.1109/IRWS.2006.305234`.

[163] H. Huang, A. Boyer, and S. B. Dhia, “Analysis and modeling of passive device degradation for a long-term electromagnetic emission study of a DC-DC converter”, *Microelectronics Reliability*, vol. 55, no. 9-10, pp. 2061–2066, 2015.

[164] W. Parker, W. Tustin, and T. Masone, “The case for combining EMC and environmental testing”, *in ITEM 2002*, 2002, pp. 54–60.

[165] X. Gao, C. Sui, S. Hemmady, *et al.*, “Modeling static delay variations in push–pull CMOS digital logic circuits due to electrical disturbances in the power supply”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 57, no. 5, pp. 1179–1187, 2015. DOI: `10.1109/TEMC.2015.2428272`.

[166] J.-L. Levant, M. Ramdani, and R. Perdriau, “ICEM modelling of microcontroller current activity”, *Microelectronics journal*, vol. 35, no. 6, pp. 501–507, 2004.

[167] L. Yuanhao, X. Shuguo, and C. Yishu, “A new methodology to build the ICEM-CE model for microcontroller units”, *in 2021 IEEE International Workshop on Electromagnetics: Applications and Student Innovation Competition (iWEM)*, vol. volume1, 2021, pp. 1–3. DOI: `10.1109/iWEM53379.2021.9790696`.

[168] J.-L. Levant, M. Ramdani, R. Perdriau, and M. Drissi, “EMC assessment at chip and PCB level: Use of the ICEM model for jitter analysis in an integrated PLL”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 49, no. 1, pp. 182–191, 2007. DOI: `10.1109/TEMC.2006.888181`.

[169] A. Boyer and S. B. Dhia, “Effect of aging on power integrity and conducted emission of digital integrated circuits”, *Journal of Low Power Electronics*, vol. 10, no. 1, pp. 165–172, 2014.

[170] N. Berbel, R. Fernández-García, I. Gil, B. Li, S. Ben-Dhia, and A. Boyer, “An alternative approach to model the internal activity of integrated circuits”, *in 2011 8th Workshop on Electromagnetic Compatibility of Integrated Circuits*, 2011, pp. 88–92.

[171] N. Berbel, R. Fernandez-Garcia, and I. Gil, “Characterization and modeling of the conducted emission of integrated circuits up to 3 GHz”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 56, no. 4, pp. 878–884, 2014. DOI: `10.1109/TEMC.2013.2294256`.

[172] N. Berbel, R. Fernández-García, and I. Gil, “Characterization of conducted emission at high frequency under different temperature”, *in 2013 9th International Workshop on Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, 2013, pp. 147–151. DOI: `10.1109/EMCCompo.2013.6735190`.

[173] C. Ghfiri, A. Boyer, A. Durier, and S. Ben Dhia, “A new methodology to build the internal activity block of ICEM-CE for complex integrated circuits”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 60, no. 5, pp. 1500–1509, 2018. DOI: `10.1109/TEMC.2017.2767084`.

[174] C. Ghfiri, A. Boyer, A. Bensoussan, A. Durier, and S. Ben Dhia, “A new methodology for EMC prediction of integrated circuits after aging”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 61, no. 2, pp. 572–581, 2019. DOI: `10.1109/TEMC.2018.2819722`.

[175] S. H. Airieau, T. Dubois, G. Duchamp, and A. Durier, “Multiport ICIM-CI modeling approach applied to a bandgap voltage reference”, *in 2016 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2016, pp. 526–531. DOI: `10.1109/EMCEurope.2016.7739248`.

[176] Z. Dongyao, Z. Changlin, Y. Daojie, L. Shuang, H. Kai, and Z. zhilong, “Immunity model of the embedded CAN controller to conducted interferences”, *in 2019 12th International Workshop on the Electromagnetic Compatibility of Integrated Circuits (EMC Compo)*, 2019, pp. 186–188. DOI: `10.1109/EMCCompo.2019.8919788`.

[177] H. Huang, A. Boyer, S. Ben Dhia, and B. Vrignon, “Prediction of aging impact on electromagnetic susceptibility of an operational amplifier”, *in 2015 Asia-Pacific Symposium on Electromagnetic Compatibility (APEMC)*, 2015, pp. 86–89. DOI: `10.1109/APEMC.2015.7175235`.

[178] J. Cheng, C. Zhou, D. Yu, Z. Xu, and D. Zhang, “An ICIM-CI-T model for EMI prediction of IO element on typical FPGA with temperature effect considered”, *IEEE Transactions on Electromagnetic Compatibility*, vol. 62, no. 3, pp. 755–764, 2020. DOI: `10.1109/TEMC.2019.2919710`.

[179] IEC 61967-4, *Integrated circuits — Measurement of electromagnetic emissions — Part 4: Measurement of conducted emissions 1 ohm/150 ohm direct coupling method*. IEC, 2021.

[180] S. Delmas-Bendhia, F. Caignet, and E. Sicard, “A new method for measuring signal integrity in CMOS ICs”, *Microelectronics international*, 2000.

[181] H. Liu, T. Claeys, D. Pissoort, and G. A. E. Vandenbosch, “Characterizing EMI-filters’ deviations caused by the capacitors ageing based on complex impedance analysis”, *in 2020 International Symposium on Electromagnetic Compatibility - EMC EUROPE*, 2020, pp. 1–5. DOI: `10.1109/EMCEUROPE48519.2020.9245776`.

[182] W.-T. K. Chien, J. X. Luo, and M. Zhang, “The competing aging effects on SRAM operating life tests”, *IEEE Transactions on Device and Materials Reliability*, vol. 19, no. 2, pp. 416–425, 2019. DOI: `10.1109/TDMR.2019.2916481`.

[183] C. Zorn and N. Kaminski, "Acceleration of temperature humidity bias (THB) testing on IGBT modules by high bias levels", *in 2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2015, pp. 385–388. DOI: `10.1109/ISPSD.2015.7123470`.

[184] IEC60749-4:2017, *Semiconductor devices mechanical and climatic test methods part 4: Damp heat, steady state, highly accelerated stress test (HAST).* IEC, 2017.

[185] A. Boyer, "A low-cost RF detector to enhance the direct power injection conducted immunity setup", *IEEE Letters on Electromagnetic Compatibility Practice and Applications*, vol. 4, no. 4, pp. 108–113, 2022. DOI: `10.1109/LEMCPA.2022.3210876`.

INSA INSTITUT NATIONAL
DES SCIENCES
APPLIQUÉES
RENNES

INSA RENNES
Service de la Recherche

AVIS DU JURY SUR LA REPRODUCTION DE LA THESE SOUTENUE

Titre de la thèse:
Evaluation of Electromagnetic Hazards due to Environmental Stresses, Obsolescence and/or Ageing, Evaluation at the IC Level

Nom Prénom de l'auteur : KHAN QAZI MASHAAL

Membres du jury :
- Monsieur PISSOORT Davy
- Monsieur BOYER Alexandre
- Madame BEN DHIA Sonia
- Monsieur CASTANIER Bruno
- Monsieur DURIER André
- Monsieur BESNIER Philippe
- Monsieur RAMDANI Mohamed
- Monsieur PUES Hugo

Président du jury :

Date de la soutenance : 31 Janvier 2023

Reproduction de la these soutenue

☒ Thèse pouvant être reproduite en l'état
☐ Thèse pouvant être reproduite après corrections suggérées

Fait à Rennes, le 31 Janvier 2023

Signature du président de jury

Le Directeur,

Vincent BRUNIE

COLLEGE DOCTORAL BRETAGNE
MATHS, TELECOMS
INFORMATIQUE, SIGNAL
SYSTEMES, ELECTRONIQUE

INSA INSTITUT NATIONAL DES SCIENCES APPLIQUÉES RENNES

Titre : Evaluation des risques électromagnétiques dus aux stresses environnementaux, à l'obsolescence et/ou au vieillissement dans les circuits intégrés

Mots clés : Circuit intégré, CEM, multi-fréquences, immunité conduite, émission conduite, stress thermique, vieillissement

Résumé : Pendant le cycle de vie d'un circuit intégré (CI), des conditions environnementales critiques peuvent fortement influencer son comportement en matière de compatibilité électromagnétique (CEM). A l'heure actuelle, il n'existe aucune méthode rapide et bon marché pour garantir les performances d'un système en matière de CEM pendant ce cycle. De plus, l'immunité EM conduite harmonique des CI est actuellement étudiée en utilisant des perturbations EM mono-fréquence. En pratique, cependant, un environnement EM quelconque peut comprendre des perturbations à de multiples fréquences, qui peuvent se coupler simultanément aux broches du CI et provoquer des défaillances plus ou moins sérieuses. Afin de caractériser et d'analyser avec précision les niveaux d'immunité et d'émission conduites au niveau du CI et d'adopter une approche boîte blanche pour trouver la cause racine de la défaillance, un CI a été spécialement développé. En vue d'une approche CEM basée sur les risques (risk-based), des essais d'immunité multi-fréquences ont été réalisés en simulation et en mesure pour caractériser les interactions entre ces fréquences et étudier l'influence de la température sur cette immunité. De plus, l'impact du stress thermique sur l'immunité EM transitoire de blocs analogiques ayant une fonctionnalité similaire mais des topologies différentes a été comparé et étudié. Des modèles IEC ont déjà été proposés pour anticiper les problèmes de CEM conduite. Cependant, ces modèles ont plusieurs limites car ils ne prennent pas en compte les contraintes environnementales telles que le vieillissement et le stress thermique. Des tests de durée de vie hautement accélérés et des cyclages thermiques ont été réalisés pour valider l'effet du vieillissement et du stress thermique, causant des variations dans les blocs passifs et/ou actifs de ces modèles standard.Ces travaux ouvrent la voie à l'inclusion de telles variations dans les futures révisions de ces normes.

Title: Evaluation of Electromagnetic Hazards due to Environmental Stresses, Obsolescence and/or Ageing, Evaluation at the IC Level

Keywords: IC, EMC, multitone, conducted immunity and emission, thermal stress, ageing

Abstract: Within the lifetime of an integrated circuit (IC), critical environmental conditions can strongly influence its electromagnetic compatibility (EMC) behavior. At the time being, there is no fast, cost-effective method to guarantee that a system can maintain its EMC performance. Further, the conducted continuous-wave EM immunity of ICs is currently being characterized by single-tone EM disturbances. In practice, however, an uncertain EM environment includes multiple disturbance frequencies that could couple into the IC pins, simultaneously causing soft or hard failures. To accurately characterize and analyze conducted immunity and emission levels at the IC level and adopt a white-box approach to find the root cause of failure, a custom-designed IC was developed. For a risk-based EMC approach, multitone immunity testing was adopted in simulations and measurements to characterize the causal interactions and investigate the influence of temperature on these immunities. Additionally, the transient EM immunities of analog blocks with similar functionality but different topologies were compared and investigated under the impact of thermal stress. Existing IEC models have already been proposed for the anticipation of conducted EMC issues. However, these IC models do not take into account environmental stresses such as aging and thermal stress. Highly accelerated life tests and thermal cycling were performed to validate the effect of aging and thermal stress, respectively, causing deviations in the passive and/or active blocks of these standard models, which were identified and characterized. This paves the way to the inclusion of such deviations in future revised versions of those standards.