Experimental study of Si and InGaAs FETs operating at deep cryogenic temperatures

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Étude expérimentale de FET Si et InGaAs fonctionnant à des températures cryogéniques profondes

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Alla mia famiglia
e a coloro che non ho potuto fare a meno di amare

Abstract

This thesis investigates the behavior of Si and InGaAs FETs down to 10 K. The study is born to answer impending question for the design of future quantum computers, particularly for what concerns processing electronics. Within this framework, it is important to remember that processing electronics is needed to work as close as possible to the qubits, at an ambient temperature of a few Kelvin units. Moreover, as this work shows, the noise generated in the device, either due to device-induced mechanism or to self-heating, needs to be maintained crucially low so not to distort the signals of the qubits.

Therefore, starting from the standard of an industrial 28nm Si technology, the thesis analyzes the effects of deep cryogenic temperatures on this class of MOSFETs and compares the results with what is already in literature or might still be under present study. Furthermore, in order to separate the effects that are induced by the material (Si in the first case) and the technology, the thesis proceeds to study devices relying on InGaAs. As a first bridge to FDSOI, InGaAs MOSFETs with a buried oxide were studied, already highlighting both differences induced by the different quality of the oxide interface (higher Interface states) and new effects introduced by the new material under study (conduction in the satellite valleys). Finally, with a particular interest for low-noise amplifiers, InGaAs-based high electron mobility transistors were studied.

The thesis has worked on both experimental and modeling topics. For what concerns characterization of the studied devices, DC performances, flicker noise, capacitance behavior, self-heating and conduction in the satellite valleys of InGaAs were the topics under study. Starting from the data and knowledge collected through the experimental analysis, the thesis also studied the applicability of the Lambert W-function and of the Kubo-Greenwood integral on the 28nm Si FDSOI devices down to deep cryogenic temperature.

Finally, this work allowed to understand how each technology can be better suited for different purposes of processing electronics in quantum computers. It moreover grants understanding on how MOSFETs and similar work when brought to cryogenic temperature, according to both their structure and material. The conduction in the satellite valleys of InGaAs has been a deeply investigated topic and, although the thesis produced very interesting results, it opened up the doors for further research in the future.

Resume

Cette thèse étudie le comportement des FET Si et InGaAs jusqu'à 10 K. L'étude est née pour répondre aux questions imminentes concernant la conception des futurs ordinateurs quantiques, en particulier en ce qui concerne l'électronique de traitement. Dans ce cadre, il est important de rappeler que l'électronique de traitement est nécessaire pour travailler au plus près des qubits, à une température ambiante de quelques unités Kelvin. De plus, comme le montre ce travail, le bruit généré dans le dispositif, soit en raison d'un mécanisme induit par le dispositif, soit en raison d'un auto-échauffement, doit être maintenu à un niveau extrêmement bas afin de ne pas déformer les signaux des qubits.

Par conséquent, à partir du standard d'une technologie industrielle Si 28 nm, la thèse analyse les effets des températures cryogéniques profondes sur cette classe de MOSFET et compare les résultats avec ce qui existe déjà dans la littérature ou pourrait encore être à l'étude. De plus, afin de séparer les effets induits par le matériau (Si dans le premier cas) et la technologie, la thèse procède à l'étude de dispositifs s'appuyant sur l'InGaAs. Comme premier pont vers le FDSOI, des MOSFET InGaAs avec un oxyde enterré ont été étudiés, mettant déjà en évidence à la fois les différences induites par la qualité différente de l'interface de l'oxyde (états d'interface supérieurs) et les nouveaux effets introduits par le nouveau matériau étudié (conduction dans les vallées satellites).). Enfin, avec un intérêt particulier pour les amplificateurs à faible bruit, des transistors à haute mobilité électronique à base d'InGaAs ont été étudiés.

La thèse a travaillé sur des sujets expérimentaux et de modélisation. En ce qui concerne la caractérisation des dispositifs étudiés, les performances DC, le bruit de scintillement, le comportement des capacités, l'auto-échauffement et la conduction dans les vallées satellites d'InGaAs étaient les sujets étudiés. À partir des données et des connaissances collectées grâce à l'analyse expérimentale, la thèse a également étudié l'applicabilité de la fonction W de Lambert et de l'intégrale de Kubo-Greenwood sur les dispositifs Si FDSOI de 28 nm jusqu'à des températures cryogéniques profondes.

Enfin, ce travail a permis de comprendre comment chaque technologie peut être mieux adaptée à différents objectifs de traitement électronique dans les ordinateurs quantiques. Il permet en outre de comprendre comment fonctionnent les MOSFET et similaires lorsqu'ils sont amenés à une température cryogénique, en fonction à la fois de leur structure et de leur matériau. La conduction dans les vallées satellites d'InGaAs a été un sujet profondément étudié et, bien que la thèse ait produit des résultats très intéressants, elle a ouvert la porte à de futures recherches.

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Four years of PhD thesis are a journey, and not the kind I could have made alone. Arriving as inexperienced as I was, there are a few people within the lab i really have to thank for standing by me through these years.

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Contents

1 Introduction **1**
- 1.1 About quantum computers . . . 1
- 1.2 Fundamentals of MOSFETs . . . 3
  - 1.2.1 Structure and basic principles of operation . . . 3
  - 1.2.2 Short-channel effects . . . 6
  - 1.2.3 mobility attenuation . . . 7
  - 1.2.4 Noise: Carrier Number Fluctuation and more noise models . . . 9
- 1.3 Low Temperature Effects . . . 11
  - 1.3.1 Swing decrease and threshold increase . . . 12
  - 1.3.2 Phonon reduction and mobility in shorter channels . . . 12
  - 1.3.3 Mobility power law . . . 13
- 1.4 Satellite valleys in III-V . . . 13
- 1.5 State of the Art . . . 14
  - 1.5.1 DC characterization of cryogenic Si FETs . . . 14
  - 1.5.2 DC characterization of cryogenic III-V FETs . . . 15
  - 1.5.3 DC characterization of cryogenic HEMTs . . . 16
  - 1.5.4 Low-frequency noise . . . 16
  - 1.5.5 Magnetoresistance analysis . . . 16
  - 1.5.6 Self-Heating Effect (SHE) . . . 17
- 1.6 Objectives . . . 18

2 Methods **19**
- 2.1 Equipment . . . 19
  - 2.1.1 Cryoprober . . . 19
  - 2.1.2 DC measurements . . . 21
  - 2.1.3 Noise measurements . . . 21
- 2.2 Extraction methods . . . 22
  - 2.2.1 Mobility attenuation factors . . . 22
  - 2.2.2 Y function for V_t and μ_0 extraction . . . 22
  - 2.2.3 Source-to-Drain resistance . . . 24

3 FDSOI MOSFETs **25**
- 3.1 C-V analysis . . . 25
- 3.2 I-V analysis . . . 28
- 3.3 Low-frequency noise . . . 33
- 3.4 Lambert-W modeling . . . 35
- 3.5 Kubo-Greenwood . . . 46
- 3.6 Conclusions . . . 54

4 InGaAs MOSFETs **55**
4.1 Cryogenic DC analysis . . . 57
4.2 Low-frequency noise . . . 61
4.3 L valley . . . 63
4.3.1 Experimental results and discussion . . . 63
4.3.2 Numerical calculations . . . 65
4.4 Conclusions . . . 66

5 InGaAs HEMTs **68**
5.1 Cryogenic DC analysis . . . 69
5.1.1 Initial observations . . . 69
5.1.2 Extraction of DC parameters . . . 70
5.1.3 Impact of access region length . . . 72
5.2 Noise . . . 75
5.3 Self-Heating Effect . . . 77
5.4 Conclusions on LNA for QC . . . 80
5.5 Satellite vlleys . . . 81
5.5.1 C-V measurements . . . 82
5.5.2 Magnetoresistance measurements . . . 83
5.5.3 X valley . . . 85

6 Conclusions **88**
6.1 Synthesis . . . 88
6.1.1 motivation and structure . . . 88
6.1.2 DC analysis . . . 89
6.1.3 Low-frequency noise analysis . . . 93
6.2 conclusions on cryo for QC . . . 95
6.3 Outlook for future research . . . 96

List of Symbols **110**

1. *Introduction*

1.1 Quantum computing and cryogenic electronics

In present days, we hear the words "Quantum Computing" more and more frequently. As a matter of fact, both industry and research institutions are deploying on daily basis and increasing effort in developing a quantum computing technology that could outperform present classical computers

Let us though analyze why it is so. At the core of every computational machine there is an element directly responsible for its computational power: the bit. The computers we work with in our everyday life rely on bits that are either set on '0' or '1', in fact, corresponding to the electrical values of OFF or ON, respectively. If on one hand, classical computing machines present bits that work like switches, on the other hand, quantum computer have bits (quantum bits or qubits) that operate like knobs. These qubits in fact, poses a ground ('0') and an excited ('1') state like classical bits; yet, their actual state is a combination of both, induced by their quantum mechanical nature [1]. As we regard how the computational power depends on the combination of the states of the single bits in a machine, we readily see the advantage offered by quantum computing machines. Indeed, in classical machines, the combination of states of the bits grows a power of 2 for the number of bit. Conversely, as each qubit can theoretically have an infinite number of states, the number of the combinations will increase with much faster rate, allowing to solve problems that cannot indeed be approached by the latter.

Over the past twenty years, different research institutions have experimentally demonstrated the functioning of numerous qubit technologies: Josephson junction qubits [2, 3], spin-based Silicon qubits [4, 5], qubits based on nuclear magnetic resonance (NMR) [6, 7], qubits based on ion traps [8, 9] or on defects in a diamond crystal [10] and, finally, superconducting semiconductor-based qubits [11, 12, 13, 14, 15]. Particularly, superconducting qubits have been shown to be successfully implemented within a CMOS-compatible process [16].

Although, these several qubit technologies rely on different working principles, they all share two common grounds. The first is, as their name suggest, their quntum nature. The second, as also explained by IBM [17], is the need for very cold operating temperatures: indeed, this is a mandatory requirement for qubits to maintain their quantum states and 'avoid decoherence'.

Yet, the idea of quantum computers [18] relies on much more than just the entanglement of qubits, requiring a complex architecture that combines together different electronics that have to work at different temperature stages, as shown in Figure1.1. When considering the output signal of the qubits, we have to understand it is very low in power ($\sim$-19dB) and therefore needs to be amplified (and processed) before risking to be distorted at the higher temperature stages. For this very reason, readout electronics and the

ones responsible for signal amplification have to be physically as close as possible to the qubit stage, with particular attention to interconnections going from room temperature down to 4.2K, as shown by [19].

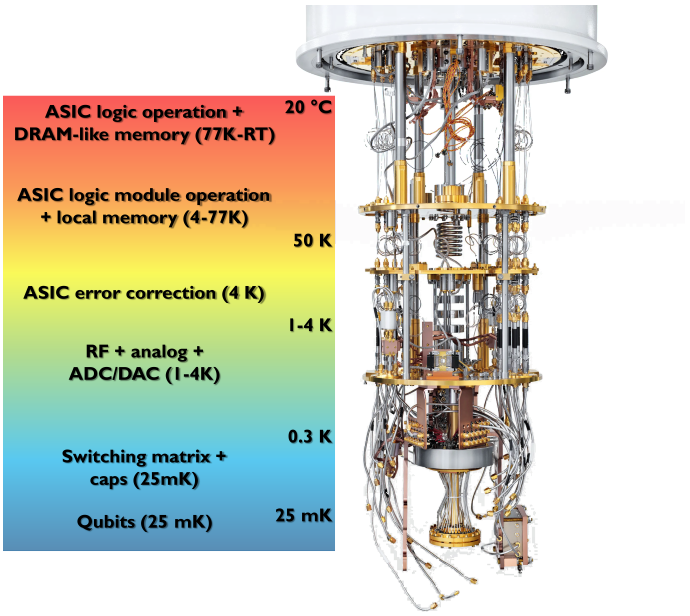


Figure 1.1: *Structure of a Righetti Computing's quantum computer with different thermal stages as reported in [20]*

Recently, the global interest in Quantum Computers (QC) and related technologies and applications has significantly increased. On one side, there are many efforts in developing new and more refined technologies for the actual qubits. On the other, there is also a rising interest in integrating cryogenic electronics to enhance the scalability and performance of the QC. When considering the nature of a QC and its architecture [18], one has to consider the fact that some qubit technologies only operate well below 1 K and have a very low output signal power which needs to be amplified in order to increase the signal-to-noise ratio (SNR) before reaching the digitization circuits that operate at higher temperatures.

In order to find suitable control electronics, the first possible answer came form the devices already in use today in modern room temperature electronics. Out of these, we surely cannot avoid naming Silicon-based Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs), which are widely spread across all the fields of electronics. Moreover, there is the possibility for III-V semiconductor (and other types) alloys, which secured their ground in high-power (such as GaN and SiC) and low-power and photonics (such as InGaAs ad more).

With all these possible candidates for the control electronics, some questions/challenges remain to be answered still. Firstly, when going down to low temperature, there is a whole cumbersome setup that needs to be put in function: this yields the need for high-vacuum pumps and pipes capable of handling the transport of cryogenic fluid. Secondly, the evolution of the physics of these devices has to be properly understood with respect to a decreasing temperature. Therefore, if on one hand the physics itself is changing, on the other hand, the measuring setup can pose further challenges. A clear example of this is the measurement of low-frequency noise, that see the noise spectral densities affected by the vibrations of the vacuum and cryogenic pumps.

Recently many efforts have been made to characterize this type of processing (or control) electronics down to deep cryogenic temperatures, such as [21, 22, 23, 24]. Within this context, the work of this thesis revolves around the experimental study of different types of devices used in control electronics (MOSFETs and MOSFET-like) down to deep cryogenic temperatures.

The present chapter follows with a description of the fundamental functioning of the MOSFET device, the main effects induced by low temperature on the operation of these devices, and a brief explanation of satellite valleys in III-V semiconductor alloys and how they differ from Si. The second chapter will address the characterization and modeling of an industrial 28nm Si FDSOI technology. The third will follow the characterization of a InGaAs-based similar technology and how it behaved down to 10K, inspecting its potential advantages with respect to Si. Finally the fourth chapter will look at a class of InGaAs-based high-electron mobility devices (HEMTs), in order to investigate their potential as readout electronics in place of FDSOI or as amplifiers to place right at the output of qubits.

1.2 Fundamentals of MOSFETs

When looking at the electronics employed in information and communication technologies (ICTs), the MOSFET is that one element that seems to be present everywhere: as a matter of fact, its simplicity and solid functionality were optimized through decades of research to reach the present state-of-the-art, making it so hard to rethink electronics out of a CMOS-compatible process. Due to this, the MOSFET is the most immediate choice when beginning to plan the control electronics for quantum computers and, although we will not necessarily see the sole implementation of CMOS (i.e. the complementary MOSFETs technology), understanding its functioning enables us to easier understand how novel devices operate, particularly as many still work as field-effect devices in a similar fashion to the Si MOSFET.

1.2.1 Structure and basic principles of operation

The structure of the MOSFET is at first degree already explained by its name: Metal-Oxide-Semiconductor Field-Effect-Transistor.

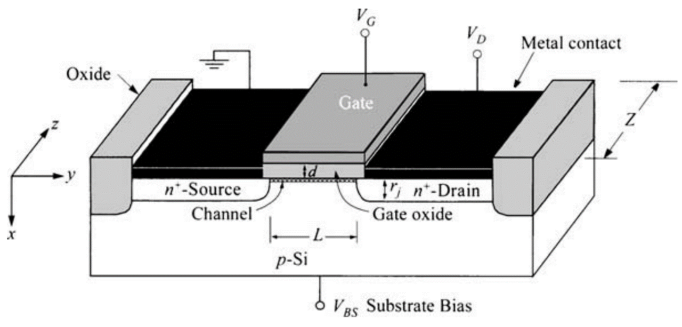


Figure 1.2: *Structure of MOSFET as depicted in [25]*

As we can see from Figure 1.2 [25], the basic structure of a MOSFET is a sandwich of three layers (a metal, an insulating oxide, and a doped semiconductor) with a region

of semiconductor with high opposite doping at each side. Although this structure has recently evolved into a more complex ones (e.g. FDSOI, FinFET, NWFET, etc.), as further shown by [26, 27], the functioning principle of the MOSFET is still the same, for the new blocks we find added to the geometry are only capacitors studied to reduce leakages or boost the performances in the case of extremely down-scaled devices or specific applications. Therefore we can still consider this as a MOS capacitors with two metal-like reservoirs of carriers at the side.

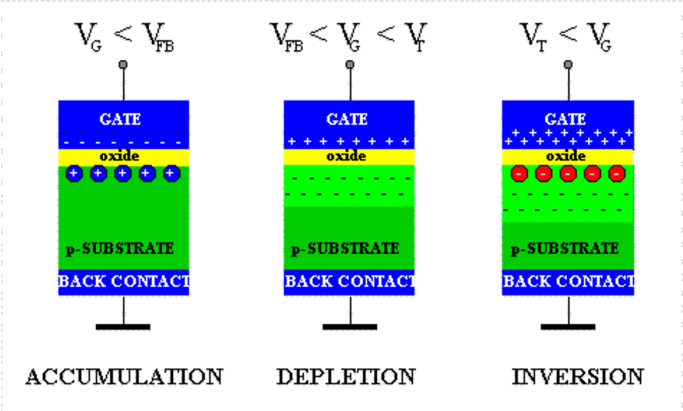


Figure 1.3: *Different operation regions of a MOS capacitor as described in [28]*

As shown in Figure 1.3, a MOS capacitor (and consequently, also a MOSFET) can be operated in different ways (operation regions), but within this work, we will mainly look at the inversion mode for characterization purposes. Forgetting for a moment about the reservoirs at the sides, the inversion mode of a MOS capacitor is when minority carriers (electrons for a p-type substrate and holes for n-type substrate) condense from the substrate into a 'channel' close to the interface with the oxide. As the applied voltage on the metal plate of the MOS capacitor pulls electrons from a p-doped semiconductor substrate, these electrons gather near the oxide-semiconductor surface, for the oxide acts as the insulator of the capacitor.

Yet, to be more precise, the difference between a MOS capacitor alone and the MOS structure we see in a MOSFET is that, having two highly doped regions at the sides, carriers in inversion are also, if not mainly, coming from these reservoirs, moreover granting the MOSFET a higher cutoff frequency (in case of AC biasing of the metal plate) with respect to the MOS capacitor alone. By applying a voltage in between the two highly-doped (n-doped in the case of electrons in the inversion channel) reservoirs at the side, electrons will flow from one side to the other of the channel that has been formed. For this reason, the two highly doped regions take the names of Source and Drain.

Finally, the metal contact at the top of the MOS structure takes the name of Gate, being the one tuning the carrier density in the channel. While the bottom contact, connected at the substrate, stays normally grounded, determining the reference potential with respect to the bias of the Gate, V_g. Therefore, we can finally see the MOSFET operating as depicted in Figure 1.4 [29]: once the inversion channel is formed, it acts as a blunt piece of semiconductor, with an associated equivalent resistance, and electrons flow through it from Source to Drain.

As we can see from the left axis of Figure1.5a, the logarithm of I_d increases linearly for small values of the Gate bias. This linear slopes represents indeed the quality of the switching of the device: this linearity is referred to as subthreshold slope. As a matter

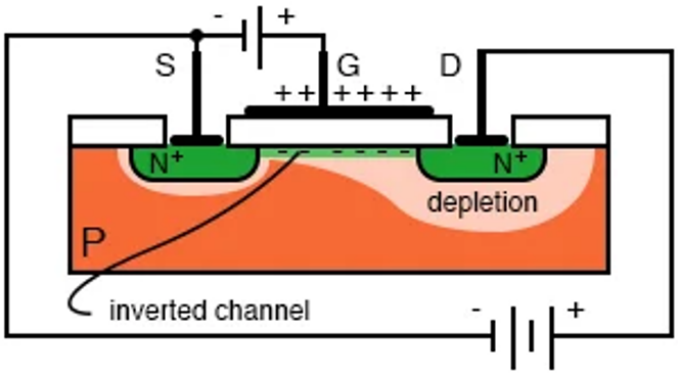


Figure 1.4: *Functioning of a MOSFET in inversion mode as described in [29]*

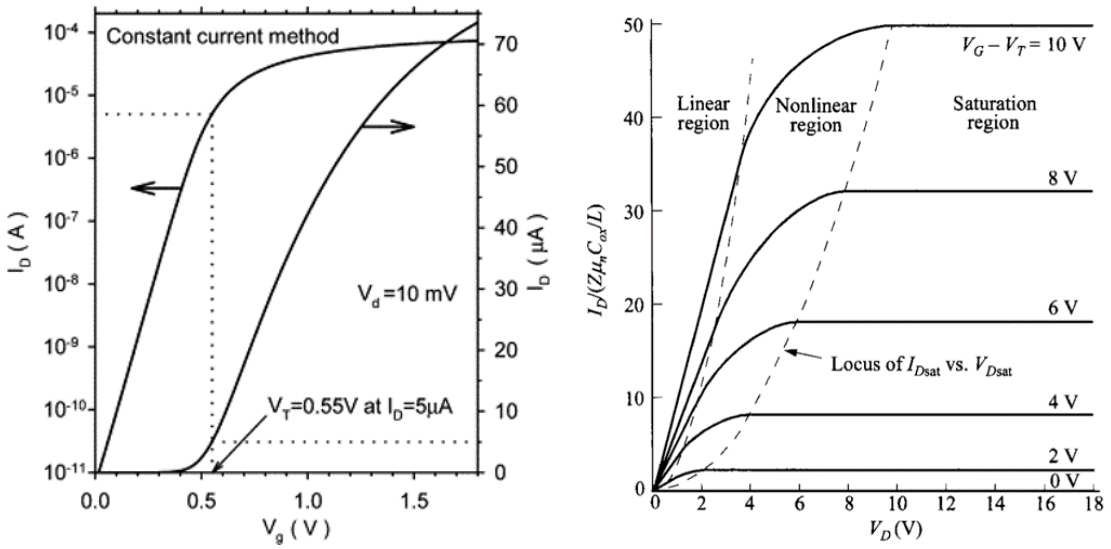
of fact, the sharper this slope is, the bigger is the separation in between the OFF and ON states, with less values of I_d in between the two. The inverse of this slope, is the subthrehsold swing.

For every MOSFET device there is a value of V_g, past which the device is surely operating in strong inversion: this is the threshold voltage, V_t. Taking a look at Figure 1.5a, we can see how V_t is marked with a vertical dotted line cutting both the logarithmic and liner plots of $I_d(V_g)$. On one hand the logarithmic plot (left axis) stops having a linear shape after V_t. On the other hand, the linear plot (right axis) assumes a linear shape (even if briefly). It is important to remark that the exact concept or operation region associated to V_t may vary according to the definition or the application, but as long as taken consistently within a work of characterization of benchmark, it allows to understand how the switching of the MOSFET varies across different geometries and technologies. So far, we have only addressed the MOSFET as device piloted by the V_g bias, as it is in fact described more in detail in Figure 1.5a for small values of the Drain voltage V_d.

Indeed, only for small values of V_d the inversion channel works as a resistor, as we can also see from Figure 1.5b [25]. Conversely, as we move towards bigger values of V_d, we can see how the behavior of the channel changes with respect to the one of a simple resistor, to the point where we reach values so high of the Drain bias that we enter a region of the $I_d(V_d)$ (output) characteristics of a MOSFET where the output current is actually constant: this is the saturation region.

In order to better understand a MOSFET's saturation we have to recall the concept of reference potential that was introduced for the biasing of the substrate. Indeed, every point where a bias is applied induces a field through the device, which in turn determines a local depletion region. As we understand this, it becomes clear how the electrostatic control of the gate is only effective as a function of the reference potential nearby. Therefore, as we approach the Source, the inversion in the channel will depend on the value V_g-V_s; as we approach the Drain, we will have to consider the value of V_g-V_d; and in the center of the channel, it will be V_g-V_B. As in general the Source terminal is always grounded (V_s = 0V), near the source region, the channel inversion induced by the gate will be the same, independently of the value of V_d. Contrarily, near the Drain reservoir, the bias V_d will have to be considered as the reference potential when applying V_g.

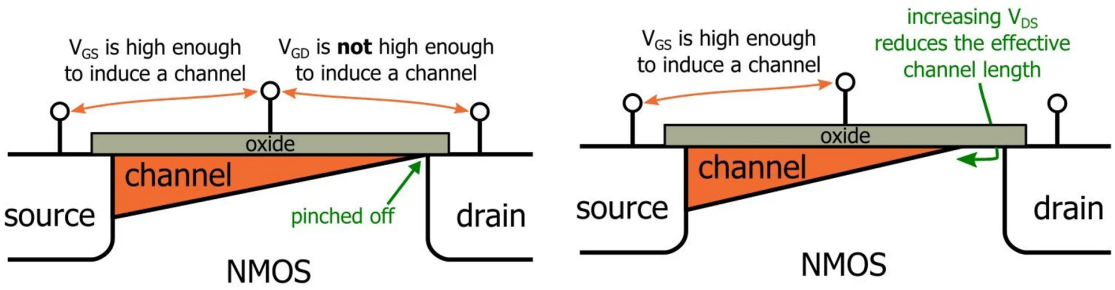
By looking at Figure 1.6a [31], we can see how the channel starts to 'pinch off' near the Drain, as V_d passes a certain value, therefore restricting the passage of electrons through the channel. As we move towards higher values of V_d, we see that not only the channel gets 'pinched off', but the depletion region induced by the biasing of the



(a) *$I_d(V_g)$ (transfer) characteristics of a MOSFET [30]* ***(b)*** *$I_d(V_d)$ (output) characteristics of a MOSFET [25]*

Figure 1.5

Drain becomes so big the channel cannot stay inverted (i.e. formed) anymore near the Drain region, as shown in Figure 1.6b. What is interesting though, recalling Figure 1.5b, is that although the Drain voltage keeps increasing, past a certain point the output current I_d stays constant. This is readily explained by a balancing in between the acceleration on the electrons towards the Drain (higher V_d) and the increase in the equivalent resistance on their path.

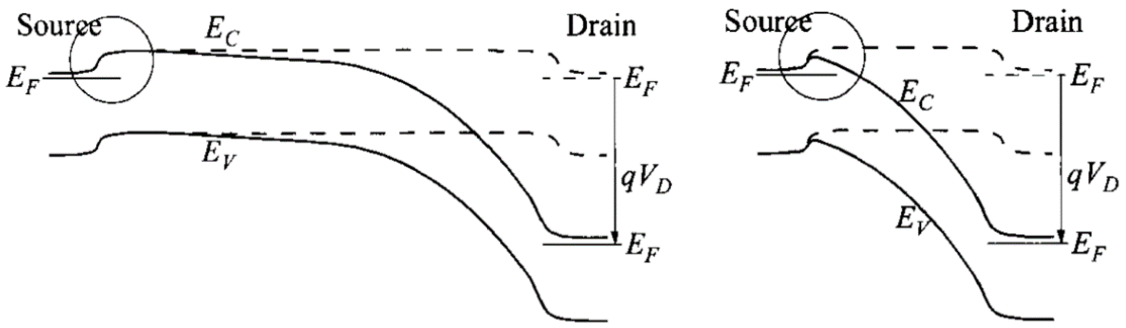


(a) *Pinch off in a MOSFET* ***(b)*** *Channel length Modulation in a MOSFET*

Figure 1.6: *MOSFET saturation [31]*

1.2.2 Short-channel effects

Over the years, the increasing need for faster and more densely-packed electronics brought industry to downscale more and more the geometry of the MOSFET. As [25] explains, reducing the length of the channel in a MOSFET impacts in turn the shape, and consequently the strength, of the potential in between the Source region and the channel. Figure 1.7 clearly shows how the potential barrier at the Source junction is 'deformed', allowing electrons to flow with more ease for lower values of the V_g bias or if the drain voltage is pushed too far. As this barrier lowering is induced by the bias applied at the Drain, this effect is named Drain-induced barrier lowering, or just DIBL.



(a) *Long-channel device* ***(b)*** *Short-channel device*

Figure 1.7: *Band diagram of a MOSFET across channel direction, under high drain bias [25]*

For the point of view of the operation of the device and its performances, the DIBL translates into a worsening of the subthreshold swing for short-channel devices as V_d increases: this efefct can be seen in Figure 1.8 for the devices with length 1.5 and 3 μm. Taking a further look at Figure 1.8, we can see how the threshold voltage V_t decreases (threshold roll-off) for progressively smaller lengths of the channel: in fact, the device 'starts' to turn on for lower values of the Gate bias V_g. Moreover looking only at the values of the subthreshold current, we see that I_d below threshold has values increasingly higher for shorter channels. As the move towards shorter channels, the slope of the OFF current with V_g decreases: indeed, this equivalent worsening of the subthreshold swing implies a worse switch-on/switch-off capability of the device.

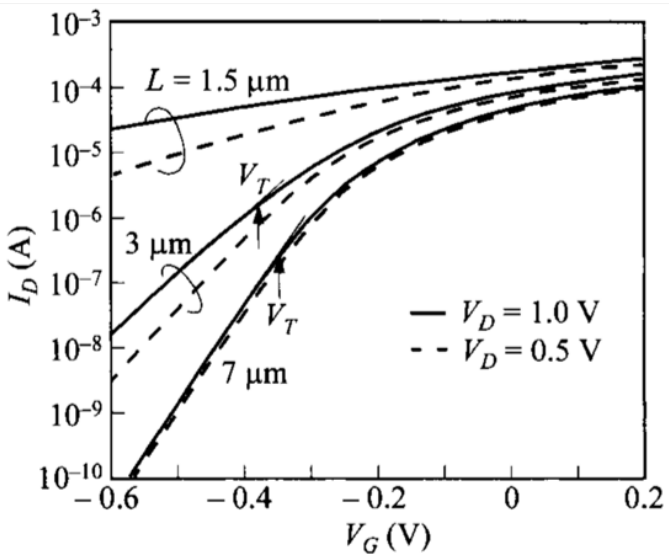


Figure 1.8: *Effect of a shortening channel length on the transfer characteristics of a MSOFET [25]*

1.2.3 mobility attenuation

Already in the 80's, MOSFET were showing a drain current that was not fully linear with respect to an increasing V_g (above threshold), therefore not respecting anymore the

behaviour described by (1.1) for the linear region of the MOSFET (low V_d, high V_g) [32]. As explained in 1986 by Ghibaudo [33], I_d was displaying this sublinearity due to the effect of the series resistance, originating from the Source and Drain regions and their contacts.

$$I_d = \frac{W}{L}\mu C_{ox}(V_G - V_t)V_d \tag{1.1}$$

Consequently, a new term was introduced to model such 'mobility attenuation': Equation (1.2) reports in fact, a new formulation of the effective mobility that takes into account the attenuation for high V_g thanks to a factor θ. It is to be noted that μ_0 is addressed as low-field mobility and represent the highest value reached by the mobility, before the attenuation at high V_g.

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_g - V_t)} \tag{1.2}$$

This θ term indeed incorporated both the effect of the Coulomb scattering and the attenuation induced by the effect of the series resistance. Particularly, it has to be remarked that device down-scaling, by shortening the channel, has increased the proportional weight of the series resistance over the one of the channel. As MOSFETs faced always smaller geometries, though, given the natural affinity of Silicon dioxide with crystal Silicon, these new high-k materials naturally brought in a worsened quality of the interface, characterized by stronger surface roughness. Therefore, newer and smaller devices presented a sub-linearity of I_d in the high V_g region much stronger with respect to their predecessors. Ong, Ko, and Hu have first reformulated in 1987 the effective mobility with the influence of surface-roughness, which became increasingly important for thin oxides [34]: this contribution would later (1994) be redefined from η_2/T_{ox}^2 to simply θ_2 [35], as also used in 1996 by Reichert and Ouisse et al. [36, 32].

This θ_2 term, as it will be referred to in the rest of this thesis, accounts for mobility attenuation at the highest values of the Gate bias. These effects are proportional to the square of the electric field and ,therefore, we reformulate the effective mobility from Equation (1.2) as in (1.3):

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1(V_g - V_t) + \theta_2(V_g - V_t)^2} \tag{1.3}$$

Furthermore, Lin studied surface-roughness scattering down to low temperature, differentiating for different quantized subbands [37]. To briefly recall the concept of subbands, as the thickness of the layer where electrons travel reduces below a certain value, the conduction band splits into several subbands. Therefore, for each valley (minimum) of the band, there will actually be several energy levels to which conducting electrons can belong Thus, Lin explains how surface-roughness scattering dominates at lower temperatures: as the temperature drops towards 0K, electrons tend to populate always more exclusively the ground state E_0 [38], where they resent more from the effect of surface roughness, being closer to the Si-oxide interface. Also, as we take into account different quantized subbands, their populating electron are further from the interface as the energy state increases with respect to the ground state, being less influenced by surface roughness. According to [37], the attenuation of the mobility was reformulated in a trend much similar to a Taylor expansion, accounting for always higher-order attenuation factors (i.e. $\theta_n(V_g - V_t)^n$), as shown in equation (1.15). Finally, Rais et al. showed in 1994 that all of

these higher-order attenuation factors are indeed inter-correlated, accounting for different amplitudes of the surface-roughness scattering [39].

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_1(V_g - V_t) + \theta_2(V_g - V_t)^2 + ... + \theta_n(V_g - V_t)^n} \tag{1.4}$$

1.2.4 Noise: Carrier Number Fluctuation and more noise models

Although MOSFETs are nowadays a very advanced technology and seem to be more and more stable, if we actually look at 'under a microscope', we can see that indeed it is fluctuating over very small intervals of time. In fact, the amplitude of these current oscillations is generally very small (excluding RTN can rise up to 10-20% of the DC value) compared to the value of the current itself and this allows to regard MOSFETs as stable, but on the other hand these fluctuations can allow us to better understand the physics of the mechanisms taking place within the device and therefore, drawing insights on its quality and functioning. To clarify, all the noise studied in this thesis work will only take into account the oscillations of the transfer characteristics $I_d(V_g)$. Still referring to the standard of MOSFET we have seen so far, we can already observe five different mechanisms that can induce these current fluctuations, hence this noise:

1. electrons can be temporarily trapped in the semiconductor/oxide interface or even in the oxide itself: as they have to tunnel from the channel to the oxide [40], this will create trapping/detrapping mechanisms that will contribute to the Carrier Number Fluctuations

2. electron can moreover be trapped in the crystalline defects of the semiconductor constituting the channel: indeed, this will yield a different kind of trapping/detrapping

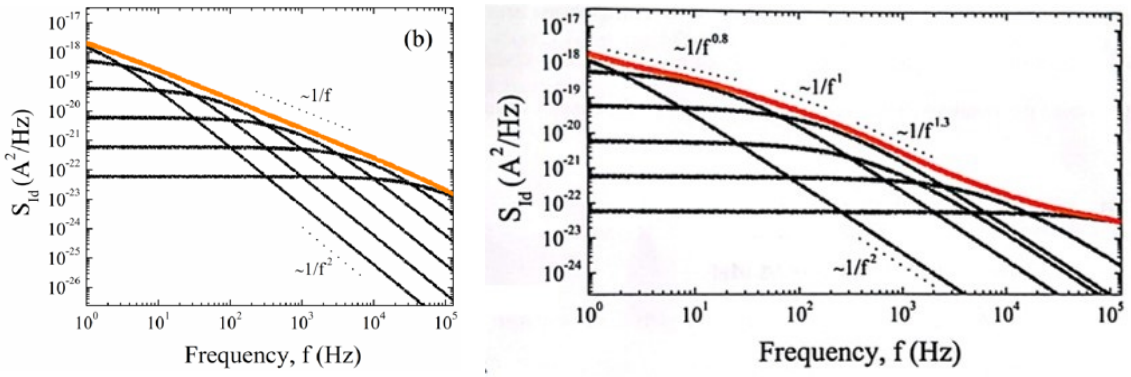
3. as electrons get trapped, they create a fixed center of charge nearby where the free electrons are flowing in the channel: the electrons traveling too close to the field originating from this trap will be deviated from the free path and therefore slow down with respect to the normal flow of current

4. in some cases, for high values of the drain current , also the access regions of the MOSFET can contribute to the noise in the device

5. finally, electrons can be deviated from their normal path due to simple scattering

In fact, when there is a high number of noise-causing mechanisms with characteristic time constants, the spectra (representation with respect frequency) of the out-coming noise will have a level that decreases as the inverse of the frequency. This concept becomes more clear as we look at Figure 1.9a, where we can see how many noise-causing mechanisms take place at the same time, yet with different but uniformly distributed in log-scale cutoff frequencies (i.e. they have different average duration lengths): as they juxtapose in the overall spectra, a 1/f behavior is shown. On the other hand, looking at Figure 1.9b, it is clear how if there is not a uniform distribution over the frequency range, the overall slope of the spectra can deviate from 1/f.

As already explained there are many causing mechanisms contributing to this type of noise, which is referred as Flicker noise or '1 over f noise'. Going back to the first two noise-causing mechanisms, we recall how the McWhorter model suggests that 1/f can be the result of trapping/detrapping through tunneling in uniformly distributed oxide



(a) *Uniform density of noise events* ***(b)*** *Non-uniform density of noise events*

Figure 1.9: *Noise spectra in a MOSFET [41]*

interface traps [40]. Due to the presence of the interface in between the semiconductor and the oxide, traps are indeed the main contributor to noise in a MOSFET. Carrier Number Fluctuations (CNF) will generate a spectrum (Power Spectral Density, PSD) that will behave according to

$$S_{I_D} = g_m^2 S_{V_{fb}}, \tag{1.5}$$

where $S_{V_{fb}}$ is the flat-band voltage PSD and is proportional to the ration between the interface trap density N_t and the area of the device WL.

For simplicity the PSD is often represented in the form of S_{I_D}/I_D^2; we can reformulate equation (1.5) into

$$\frac{S_{I_D}}{I_D^2} = \frac{g_m^2}{I_D^2} S_{V_{fb}} \tag{1.6}$$

As mentioned above, these trapped charges create a localized field that can influence the electrons flowing in the channel. Ghibaudo [42] and Hung [43], explained how the fluctuation of trapped charges in the oxide (and interface) can affect the flow of electrons through Coulomb scattering, deviating them from their free path, and therefore, effectively reducing their mobility. In turn, the overall mobility in the channel would present oscillations, addressed as Correlated Mobility Fluctuations (CMF). This type of noise would impact the PSD as reported in equation 1.7, adding up to the contribution of CNF:

$$\frac{S_{I_D}}{I_D^2} = \frac{g_m^2}{I_D^2} S_{V_{fb}} \left(1 + \alpha_{SC}\mu_{eff} C_{ox} \frac{I_D}{g_m}\right)^2 \tag{1.7}$$

α_{SC} is the remote Coulomb scattering coefficient and would later [44] be incorporated with the mobility and the capacitance into $\Omega = \alpha_{SC}\mu_{eff}C_{ox}$,because the product $\alpha_{SC} * \mu_{eff}$ was found to be gate bias independent. We can so rewrite equation (1.7) into:

$$\frac{S_{I_D}}{I_D^2} = \frac{g_m^2}{I_D^2} S_{V_{fb}} \left(1 + \Omega \frac{I_D}{g_m}\right)^2 \tag{1.8}$$

When regarding a MOSFET, we readily see how the output noise is so dependent on the gate voltage noise, particularly as MOSFETscan be viewed as voltage-to-current amplifiers. Thus, it becomes useful to define the gate voltage noise as:

$$S_{V_g} = \frac{S_{I_D}}{g_m} = S_{V_{fb}} \left(1 + \Omega \frac{I_D}{g_m}\right)^2 \tag{1.9}$$

As better shown by Kolarova et al. [45], there can be a contribution to the noise in the signal of the drain current also due to the access regions and the resistance associated to the them. Particularly, [45] has modeled this contribution as follows:

$$\frac{S_{I_D,R_{SD}}}{I_D^2} = S_{R_{SD}} \left(\frac{I_D}{V_D}\right)^2 \tag{1.10}$$

Finally, we have to address the fluctuation of mobility that are not caused by trapping/detrapping mechanisms. Indeed this model has been initially introduced by Hooge [46], who further suggested that these mobility fluctuations would only be caused by phonon scattering [47] and contribute to the PSD as follows:

$$S_{I_D} = I_D^2 \frac{q\alpha_H}{fWLQ_i} = I_D^2 S_{\Delta\mu} \tag{1.11}$$

α_H is referred to as Hooge parameter and is indeed the one characterizing this type of noise-generating mechanism. This modeling of noise has furthermore proven useful in semiconductors and metals [48]. Yet, in MOSFETs, due to the presence of the oxide and the interface it creates with the semiconductor, the dominating source of noise in the '1 over f' type is most widely accepted to be the trapping/detrapping in the oxide.

Let us finally put together all this contribution to see how, in present days, the drain current noise in a MOSFET can be modeled according to the several contributions:

$$\frac{S_{I_D}}{I_D^2} = \frac{g_m^2}{I_D^2} S_{V_{fb}} \left(1 + \Omega \frac{I_D}{g_m}\right)^2 + S_{R_{SD}} \left(\frac{I_D}{V_D}\right)^2 + S_{\Delta\mu} \tag{1.12}$$

Moreover, by looking at the sketch reported in Figure 1.10, we can understand how each contribution affects the PDS, or better its normalized value with respect to the square of the drain current at a given low frequency:

1. CNF appears to yield an initial plateau that decays at higher values of I_d
2. CNF + CMF slows down the decay of the graph, shifting cutoff towards higher current values with respect to CNF alone
3. the access region might boost the noise level at even higher current
4. the noise induced by mobility fluctuation decreases (in a log-log scale) linearly with respect to the increasing drain current; yet, it is only visible when not masked by CNF + CMF; thus, it is plotted separately

1.3 Basics of low temperature effects

Since before the interest for quantum computing, cryogenic electronics has appealed the interest of many research institutions: indeed, it could be foreseen an improvement of performances as temperature decreased. Different effects have been seen across the evolving technologies based on MOSFET (bulk, SOI, partially- and fully-depleted) [49], but in this section we will focus only on those common to all, for they are intrinsic to the physics of the semiconductor.

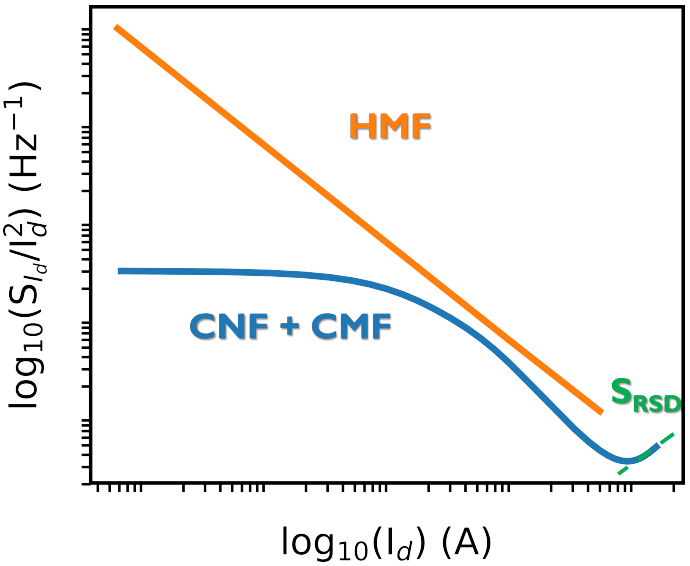


Figure 1.10: *Qualitative representation of the effects of different noise contributions on the PSD*

1.3.1 Swing decrease and threshold increase

First off, we have to recall that the carrier density in the inversion channel of a MOSFET is depending on the operation temperature. Whether we want to look at the Fermi function or to a more simplified Boltzmann statistics, the promotion of electrons to the conduction band (CB) is a thermally activated process. As a matter of fact, the statistics get steeper as temperature drops down, yielding lower probability of electron promotion at a given Gate bias. Conclusively, moving from the probability of a single electron to the effective density we see in the channel, we have that for every given V_g point we will see less electrons as the temperature decreases, resulting in a shift forward of the threshold voltage.

In a very simplified rephrasing, the MOSFET will need a higher V_g bias to reach a carrier density such that its behavior will comply with what we defined before as 'above threshold'.

The sharpening of the Fermi-Dirac statistics is not only affecting the threshold voltage: indeed, the transition from almost certainly not having an electron in the CB to almost certainly having it becomes sharper. The parameter that is directly representing this switching is the subthreshold swing SW, that, referring to the carrier density rather than the probability of a single electron, indicates the abruptness in between the ON and OFF state of a MOSFET. Indeed, SW decreases for a decreasing temperature (better switching capability of the device), reaching different values according to the type of technology, as we will see further on.

1.3.2 Phonon reduction and mobility in shorter channels

The third and last main effect induced by low temperatures is a direct consequence of the operating temperature of the device. As we can regard it as a measure of the vibrational energy, a decrease in the operating temperature yields a decrease in the vibrational energy in the lattice, whose phonons are the solid-state-physics equivalent. Less phonons present in the channel imply therefore a weaker phonon scattering (at room temperature very

influential) allowing a boost of the low-field mobility μ_0.

On the other hand, while this is one of the main advantages of low temperature operation when studying cryogenic MOSFETs in the past, with present down-scaled geometries, this boost of μ_0 is not so accentuated in short channels, as they are dominated by the scattering process induced by neutral-defects [50]. The high doping of the Source and Drain regions yields a diffusion of such dopants in the parts of the channel that are close. Therefore, as the channel shrinks and Source and Drain get closer, the parts of the channel where neutral defects are diffusing and causing scattering will predominate over the central part of the channel that is unaffected by neutral defects; hence shorter channel will be predominantly ruled by neutral-impurity scattering, rather than phonon scattering.

1.3.3 Mobility power law

If on one hand, the effective mobility μ_{eff} can be considered as a function of the Electric field at room temperature, on the other hand, Emrani et al. realized in 1994 that this case was no longer holding once the temperature dropped below a certain value [51]. A bit later they realized how actually the weight of the attenuation factors seen before was changing with a decreasing temperature. Thus, they finally defined a formulation of the effective mobility for deep cryogenic temperatures [52]:

$$\mu_{eff,LT} = \frac{2\mu_0\theta_{LT}(V_g - V_t)}{1 + \theta_{LT}^2(V_g - V_t)^2} \tag{1.13}$$

Equation (1.13) sees a term θ_{LT} accounting for mobility attenuation, independently whether it is coming from surface roughness, Coulomb scattering or access resistance.

Again in 1994, Rais et al. have generalized the effective mobility in such a way to have a continuous evolution of the equation from room- down to liquid He-temperatures [35]:

$$\mu_{eff} = \frac{\mu_0[\theta(V_g - V_t)]^{n-2}}{1 + [\theta(V_g - V_t)]^{n-1}} \tag{1.14}$$

Moreover, [35] showed that the phenomenon of the negative trans-conductance at large gate overdrive voltages increased at low temperatures. In the end, the reworked Equation (1.14) separating the effects of surface roughness from Coulomb scattering and access resistance:

$$\mu_{eff} = \frac{\mu_0[\theta_1(V_g - V_t)]^{n-2}}{1 + [\theta_1(V_g - V_t)]^{n-1} + [\theta_2(V_g - V_t)]^n} \tag{1.15}$$

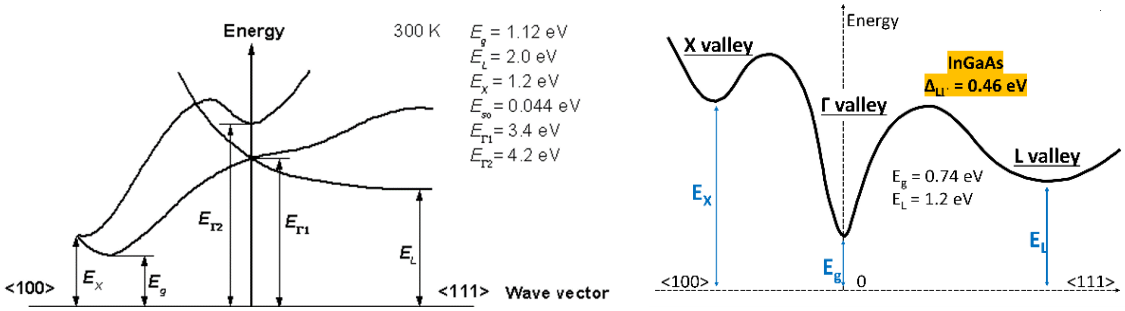
Finally, as we mentioned in the section above, Rais et al. have further studied the effect of the second-order attenuation factor: following the work of [37], they showed that the attenuation of effective mobility can indeed be looked at as a Taylor expansion and all terms above the first order account for different weights of the surface-roughness scattering, being thus inter-correlated.

1.4 Satellite valleys in III-V

In the present section, we will highlight one of the main difference in between Si (Silicon) and InGaAs (Indium-Gallium Arsenide) for what concerns carrier transport. Let

us recall briefly what the bandstructure of a semiconductor is: this is a tool that relates the energy E of a particle in the crystal with its momentum $\vec{k}$ [53]. From the point of view of this work, the band-structure is allowing to understand how valleys are being populated with electrons and therefore, the type of scattering and mobility we see in through carrier transport.

[53] explains that when the conduction band gets filled up by electrons, the population of the band starts from the lowest available energy state, therefore from the minimum of the band. Moving forward to how actually this structure is in the two crystals under study, Figure 1.11 shows the structure for both. Indeed, we can see how the minimum of the conduction band in Si belongs to a valley centered close to the point X; moreover, we can see that there is a significant energy separation from the minimum of the lowest valley to the minimum of the next one available. Conversely, in InGaAs, as it is also the case for the minimum of the lowest available valley is not only centered exactly in the central region of the band-structure (Γ point), but it also is reasonably close to the minimum of the next valley. Thus, in InGaAs we can expect electrons to travel through the channel with different mobility, if we fill up the CB enough (i.e. pushing the Gate bias so to start populating the next available valley as well). It is finally important to underline that, according to both [54] and [55], the next available valley for electron population after Γ is the L one, which is furthermore in line with the studies carried on by O'Reghan et al., as we will later discuss.



(a) *Silicon [56]* ***(b)*** *InGaAs [56]*

Figure 1.11: *Band structures of crystals under study*

1.5 State of the Art

In order to better understand the novelty of the work presented in this thesis, the following section highlights the research work carried out so far on the topics concerned.

1.5.1 DC characterization of cryogenic Si FETs

Surely, QC has pushed much of the recent research effort into cryogenics, but characterizing the operation of electronics at low temperatures is not something so new. For example, [57] investigated the freeze-out effect in bulk MOSEFT in 1987, and Ghibaudo worked out the modeling of MOSFETs through the Kubo-greenwood formalism in 1986 and 1989 [58, 59]. Much (if not all) of the MOSFET physics at room temperature that we referred to is indeed reported in [25]. In the same way, the work of characterization and understanding of solid state physics at cryogenic temperatures (up to 2001) is reported in

[49], such as the kink effect in bulk MOSFETs and sharpening of the subthreshold swing in all several FET devices.

In recent year, new works have emerged to characterized more modern FDSOI [60] and ever newer geometries/structures, such as ultra thin body and buried oxide (UTBB) [61] and ultra-thin single- and double-gate SOI devices [62]. Also, thorough independent studies have been carried out on the effects of back bias at deep cryogenic temperatures in different classes of FDSOI [63, 64, 65]

Furthermore, the EPFL group has recently deployed a lot of effort in both characterizing [66] and modeling [67, 68] cryo FDSOI, granting essential understanding to integrate their functioning into more systemic models and simulations. Yet, in the field of FDSOI modeling, more models that go beyond EPFL's EKV have been used over the years. In [69] has used the Lambert W-function to characterize 14nm FDSOI and to extract trends that could be further applied for their modeling. [70] showed a modeling of FDSOI and FinFET devices down to deep cryogenic temperatures, particularly employing a substitute of the ambient temperature to better describe the effective quantities present in the device for the corresponding temperatures. [71] has modeled FDSOI devices down to deep cryogenic temperatures through TCAD simulations.

Concerning the DC operation of Si FETs, one topic that has over the years drawn much attention is the subthreshold swing. As explained above, it indeed marks the quality of the transition in between OFF and ON state, i.e. how abrupt the switching is. Going to deep cryogenic temperatures, it has been shown how this value improves and the transition becomes sharper, and therefore the separation in between the two states is more distinct. Yet, as the operating temperature approaches 0K, the value of the swing stops decreasing and starts to settle. [72] showed that this settling could not be attributed to the interface states, but it has rather to be seen as deriving from the "localized states situated in the band tails below the mobility edge of the two-dimensional subband". More recently, [73] has pointed out how this limit is present in other classes of FETs beyond bulk or FDSOI MOSFET and has modeled it for a recent class of FDSOI. Finally, [74] modeled the behavior of the swing down to deep cryogenic temperatures starting form the modeling of subbands in two-dimensional materials.

1.5.2 DC characterization of cryogenic III-V FETs

Yokoyama et al. have in the past greatly contributed to characterizing and understanding the physics of InGaAs MOSFETs [75, 76] and then, later on, studying mobility at low temperatures in InGaAs MOSFET [77] and the interface states in InAs MOS down to deep cryogenic temperatures [78]. On the other hand, IBM Zurich has fabricated and characterized at room temperature InGaAs-on-insulator FinFETs [79, 80] and MOSFET [81].

Within the context of what will later presented as the cryogenic behavior of L valley carriers, much effort in the past was made to simulate and understand how these carriers should behave in III-V (InGaAs particularly) MOS structures: amongst these, [82] showed how carrier for L valley are indeed 'inverting closer to the interface with respect to those coming from the Γ valley.

1.5.3 DC characterization of cryogenic HEMTs

With the uprising interest for HEMT technology, the research investigated InGaAs HEMTs concerning their performances at room temperature [83] and GaN [84, 85] and InP [86] HEMTs being investigated at cryogenic temperatures.

On the other hand, many works on HEMT, particularly when about cryogenics, focus on either noise temperatures or their RF performances, such as [87, 88].

1.5.4 Low-frequency noise

The main noise models elucidated so far, have recently been employed to study at room temperature modern Si tri-gate fin-shaped devices [89], showing how, with the presence of an interface oxide, these devices still abide the CNF+CMF model. 22nm FDSOI have instead been investigated down to very low temperatures, namely 4.2 K [90], confirming how they still abide to the CNF+CMF model through out temperature.

Though, as it is now well understood by the scientific community, noise takes a strange trend as the temperature drops below a certain level, 100K in the case of FDSOI. In investigating this 'excess 1/f noise', [91] suggests it can be related to the band tail states, as there is a correspondence in between this 'excess' and the settling of the subthreshold swing.

At room temperature, low-frequency noise has been studied in both InGaAs MOSFETs [92] and GaN HEMT [93], showing how both comply with the CNF+CMF model. Finally, concerning III-V alloys, it is important to remark how [94] suggests that in presence of intervalley scattering, the 1/f noise is governed by pure mobility fluctuation as can be described through the Hooge model.

1.5.5 Magnetoresistance analysis

Referencing the work in [95], we report in this section the results form a set of magnetoresistance measurements on the HEMT devices. Magnetoresistance mobility characterization (in MOSFETs) relies on how the Drain current decreases due to a resistance induced by the increasing magnetic field. We thus report equation (2) from [95]:

$$\frac{I_{d,0} - I_{d,B}}{I_{d,0}} = \mu_{MR}^2 B_z^2 \tag{1.16}$$

As equation (1.16) shows, the relative decrease of the value of the Drain current from null magnetic field ($I_{d,0}$) to a set value of the field ($I_{d,B}$) is equal to the square of the product of the magnetoresistance mobility, μ_{MR}, and the transverse magnetic field, B_z [96, 97, 98]. This physical phenomenon becomes very interesting in our particular case, as we see different mobilities dominating at different values of the Gate voltage, due to different conducting valleys predominating. We would therefore expect that, given the mobilities from different valleys, for different values of the Gate voltage, to see different increases in the magnetoresistance.

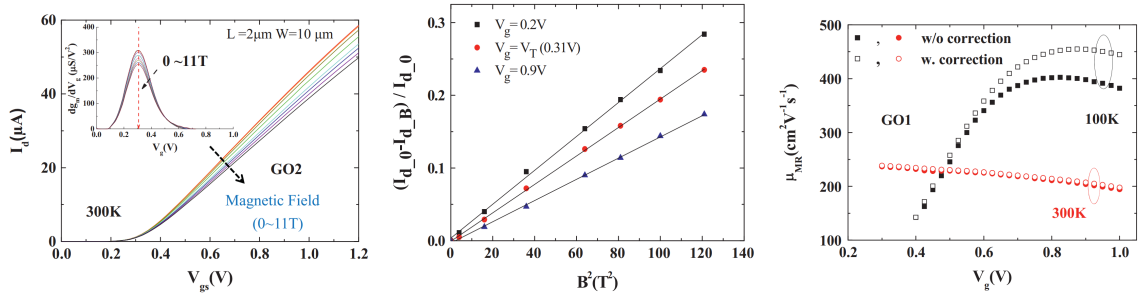
What is crucial for this type of measurement is to have wide and short device. For this, we measured a device with a channel width, W_g, of 100 μm and a length, L_g, of 100 nm. As for the standard of this technology, the Source-Drain distance remains of 1.4 μm.

Figure 1.12 reports some of the experimental results from [95]. Figure 1.12a clearly shows how, for an increasing magnetic field, the Drain current decreases in the strong inversion region and how the trans-conductance sees its peak diminish. Figure 1.12b

shows how, for different values of the Gate bias, the relative decrease of the Drain current varies linearly with respect to the square of the magnetic field: recalling equation (1.16), the slope is indeed the square of measured mobility for the specific value of V_g.

Lastly, Figure 1.12c shows the difference in the extracted μ_{MR} with and without the correction for the Source-Drain resistance. As reported in equation (1.17), [95] shows how we need at least two measurements for different channel lengths in order to extract the intrinsic mobility of the channel with magnetoresistance measurements.

$$\mu_{ch}^2 B^2 = \frac{\Delta R_{ch1} - \Delta R_{ch2}}{R_{ch1} - R_{ch2}} \tag{1.17}$$



(a) *Fig. 1(a) from [95]* ***(b)*** *Fig. 1(b) from [95]* ***(c)*** *Fig. 2(a) from [95]*

Figure 1.12: *(1.12a) Transfer characteristic at linear region for different B values at 300 K for a (W = 10 μm and L = 2 μm) device. (1.12b) Relative drain current variation versus B^2 at V_{gs} = 0.2 V, 0.31 V, 0.9 V. (1.12c) μ_{MR} without/with R_{SD} correction in (L_g = 300 and 120 nm) devices as function of gate voltage at 100 K and 300 K*

1.5.6 Self-Heating Effect (SHE)

Self-heating is one particular issue in cryogenics as it indeed determines at which actual temperature the device is operating and therefore if it is indeed at deep cryogenic temperature. For this, SHE has been investigated since very long time to understand how to better model the physics in these devices. Moreover, in more recent times, self heating effect has also drawn a lot of attention form the reliability community for the degradation it induces on the device.

Starting from the bases, SHE has been thoroughly characterized in the past on SOI technology in between 1994 and 1998 [99, 100, 101], laying the foundations of characterization method that helped characterize newer classes of devices, such as FDSOI in 2019 [102]. In 2022 [103], the data and understanding collected over the past works, allowed to draw a model for SHE in present FDSOI and bulk Si devices.

Self-heating has been thoroughly studied in FinFET devices as well, as reported in the PhD thesis of Paliwoda [104]. Also, nanowire transistors have been investigated for what concerns SHE and how it related to hot carrier degradation [105].

With the coming of quantum computers, much interest has been dedicated to HEMT devices, for their high density of carriers, their bulk structure and the absence of oxide that made them so suitable to be employed in low-noise amplification of qubit signals. Yet, [106] only investigates GaAs HEMTs in terms of noise temperature, [107] investigates InGaAs HEMTs only down to 20 K, and [108] investigates GaN HEMTs through proton irradiation.

1.6 Objectives of the thesis

Following what the present state of the art, this thesis will firstly try to confirm the present results for Si FDSOI down to cryogenic temperature, moreover inspecting the applicability of models based on the Kubo-Greewood integral and Lambert W function at those temperature. I-V analysis has been carried out down to 10 K on InGaAs devices (MOSFET and HEMT) to study if these devices follow the same trends as the Silicon devices. Furthermore, concerning the study of L valley conduction in III-V, this work will try to find experimental confirmation with respect to the modeling work done in 2010.

Concerning low-frequency noise, its study in InGaAs will be extended down to 10 K with respect to what has been shown by the works cited in the 1.5 section. To complete the understanding on the behavior of cryogenic HEMTs, the InGaAs high-electron-mobility transistors studied in the work have also been characterized down to 10 K concerning the self-heating effect, in order to understand how their operation follows the ambient temperature

2. *Methods and Equipments*

When looking at the architecture of a Quantum Computer (present, as shown in Figure 1.1 and planned for the future), we see they all resemble a big fridge, more specifically a fridge with multiple stages. At the bottom, where the cooling source is located, there is the coolest stage with the qubits ($\sim$ 30 mK), at the top the hottest stages with all the room temperature circuitry. In order for this fridge to reach the coldest temperature, the all quantum computing world revolves around the same cooling agent: liquid Helium.

Element	Symbol	Boiling Point
Helium-3 (1 neutron, more expensive)	^{3}He	3.2 K
Helium-4 (2 neutrons, more common)	^{4}He	4.15 K
Nitrogen	N	77.2 K

Table 2.1: *main refrigeration liquids used in cryogenics*

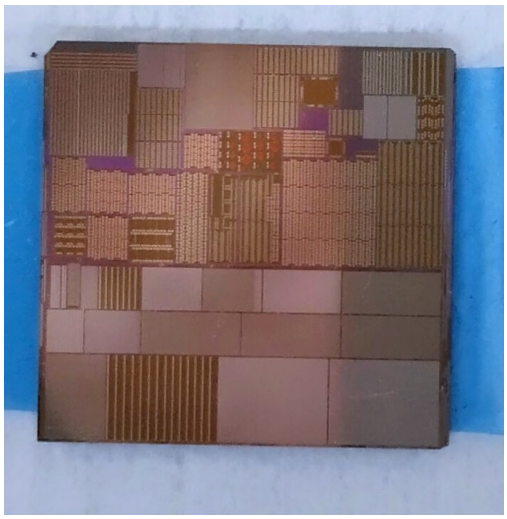
If we observe Table 2.1, we can see how different cooling liquids have different cooling powers, due to the different characteristic temperatures for transitioning from gaseous to liquid state (boiling or condensation point). Particularly, it was already shown in 1966 by [109] how combining the two different isotopes of Helium through a dilution would grant a refrigeration below 100 mK. Nowadays, technological improvement and scientific advancement of cryogenic techniques has granted us the availability to go down to 1.75 mK [110], although already in 1978 there was evidence of cooling down to 2 mK [111].

2.1 Measurement equipment

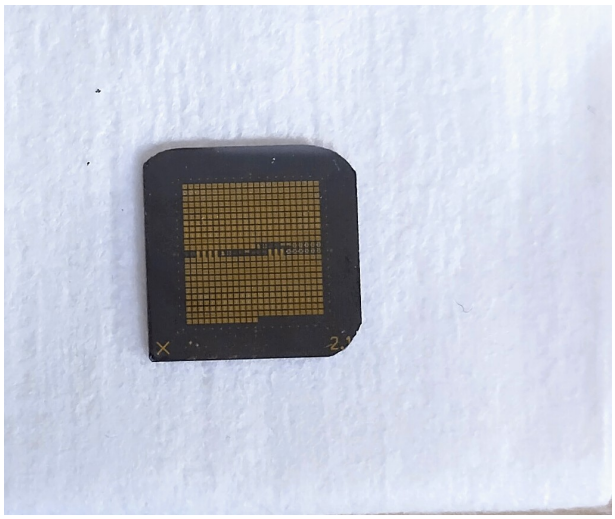
2.1.1 Cryoprober

If on one hand, Quantum Computers operate in a few 10s of mK range, to the purposes of electrical characterization of the devices under study it is enough to work in the temperature range of liquid ^{4}He, not only making characterization and experiments cheaper but also easier to handle due to a higher degree of simplicity of the related pumping and recovery systems. Characterization was therefore undertaken by placing the samples (wafer chips, Figure 2.1) inside the SUSS MicroTec PMC-150 Cryoprober, shown in Figure 2.2.

It is important to recall this is an open-loop station, therefore the achievable minimum temperature is 10 K on this specific appratus. Yet, as mentioned before, to the means of the electrical characterization this is enough. The station consists of a chuck (sample stage), which is refrigerated by cooling pipes where the Helium is pumped through. The sample cools down by thermalization as it is placed on the chuck (under vacuum) before



(a) *sample from ST/LETI, FDSOI*



(b) *sample from IBM Zurich, HEMT*

Figure 2.1

the cooling down. It is of paramount importance to achieve high-quality ultra vacuum ($\sim 10^{-6}$ mbar) for all cryogenic measuring setups (this one included), because the absence of molecules inside the chamber forbids any heat transfer, ensuring the chuck and the sample maintain the target temperature. This concept is indeed analogous to open space: the temperature is very low ($\sim$ 2.7 K) and the pressure as well ($\sim$ 1.3 10^{-16}). The station has six arms, four for DC and noise measurements and two for RF measurements.

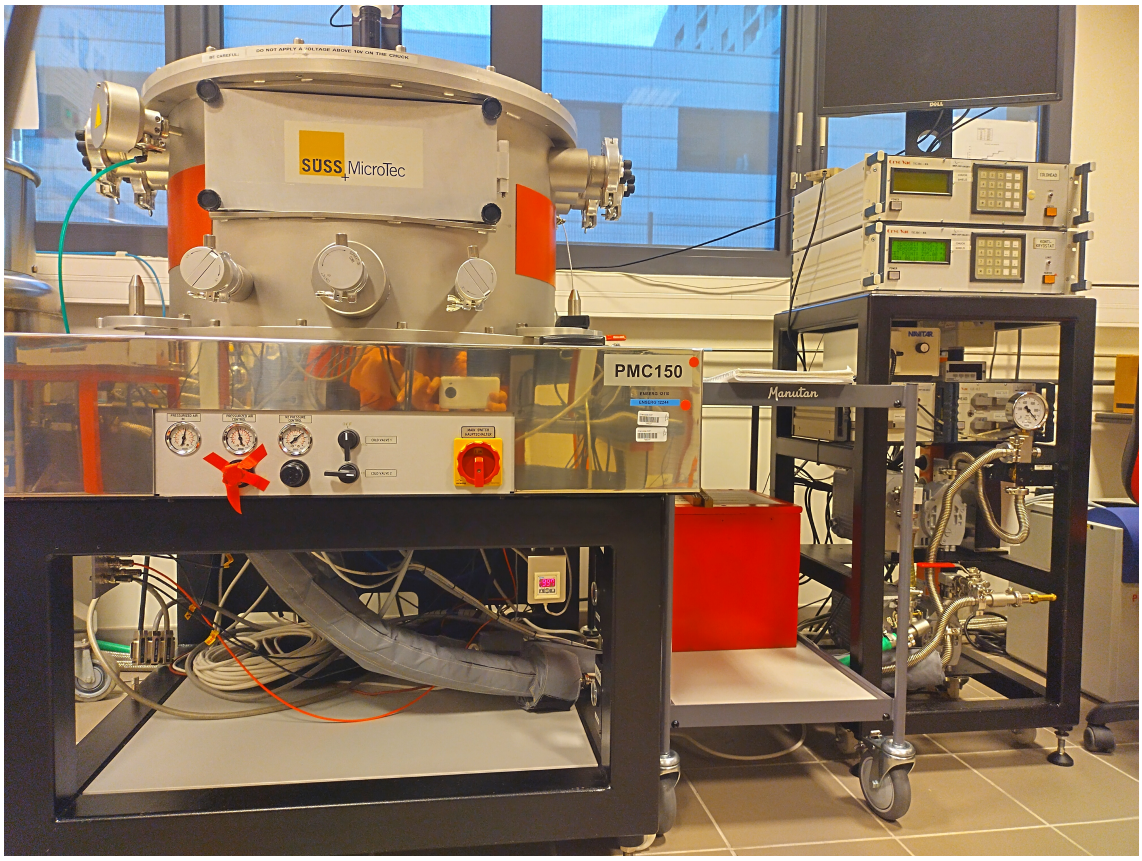
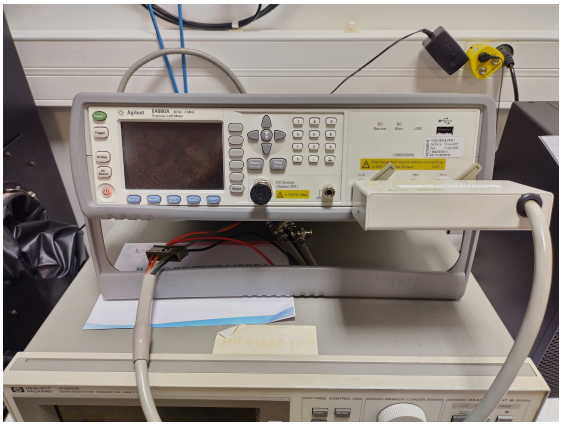


Figure 2.2: *SUSS MicroTec PMC-150 Cryoprober*

2.1.2 DC measurements

In order to carry out the required measurements, different machines had to be connected through triaxial cables. DC measurements were performed by employing the Agilent B1500 analyser, shown in Figure 2.3a for what concerns current-voltage (I-V) characteristics and measurements of self-heating. On the other hand, capacitive measurements (C-V) were performed using the Agilent E4980 (Figure 2.3b).

(a) Agilent B1500A



(b) Agilent E4980A

Figure 2.3

2.1.3 Noise measurements

Noise measurements have been performed with the NOISYS7 measurement system by Synergie Concept, shown in Figure 2.4a. It consists of three triaxial exits:

1. The first is a Source Measure Unit (SMU) different from the other two, which only work as biasing sources. This is used to set the value of the voltage V_d and measure the current I_d fluctuation. Moreover, we applied a specific splitter (Figure 2.4b, so to drive the low of the signal to the Source, ensuring same and isolated ground in between the two signals, and indeed avoiding equipment-induced fluctuations in between them.

2. The second connection is generally used to set the value of the gate voltage V_g. As explained before, this cannot be used to measure noise fluctuation.

3. The third and last connection works just like the second one, yet it was used to set the value of the voltage applied to the back (or bulk) V_b, which we kept to 0V across the several set of measurement we had.

One final remark concerns how sensitive noise measurements are: as a matter of fact, a strong shielding from radiation sources is necessary, particularly to overcome electric field-induced fluctuations that would eventually contaminate (cause harmonic peaks) the Power Spectral Density from our measurements. To this very regard, in order to avoid fluctuations induced by the AC power originating from the building's source, the Noisys box was powered with a set of two DC batteries, which are reported in Figure 2.4c.

(a) *NOISYS7 PBA (programmable bias amplifier) and DSA (digital signal acquisition) units*

(b) *SMU signal splitter*

(c) *batteries for NOISYS7*

Figure 2.4

2.2 Parameter extraction methods

2.2.1 Mobility attenuation factors

As explained in section 1.2.3, the transfer characteristics $I_d(V_g)$ suffers from an downwards bending induced at first-order approximation by Coulomb scattering and Source-to-Drain resistance, and in second order to the surface scattering. By exploiting the peak value G_m of the trans-conductance g_m we can compute the effective attenuation Θ_{eff} as a function of the increasing gate voltage V_g, as shown in equation 2.1:

$$\Theta_{eff} = \frac{G_m}{I_d} - \frac{1}{V_g - Vt} = \theta_1 + \theta_2(V_g - V_t) \tag{2.1}$$

This allows to plot and visualize the attenuation factors in such a way that the intercept (with the y-axis) is the first order attenuation factor θ_1 and the slope is the second order factor θ_2. Moreover, recalling the first chapter, θ_1 contains mobility attenuations induced both by Source-to-Drain resistance and Coulomb scattering. we can therefore write:

$$\theta_1 = \theta_{1,0} + \beta R_{SD},$$

with $\theta_{1,0}$ accounting for intrinsic first order attenuations such as Coulomb scattering,

$$\text{and } \beta = \frac{W}{L} C_{ox} \mu_0 = G_m / V_d \tag{2.2}$$

2.2.2 Y function for V_t and μ_0 extraction

When it comes to the determination of the threshold voltage, V_t, of a MOSFET, there are various ways. Often V_t is regarded as the intersection in between the V_g-axis and the straight line interpolating the linear part of I_d, which corresponds to the strong inversion

region. From the beginning of MOSFET downscaling, the first-order mobility attenuation factor has influenced the transfer characteristics of these devices, limiting the effectively linear region of I_d to a very short range of the gate voltage, therefore yielding difficulties in the extraction of V_t. For this very reason Ghibaudo defined in 1988 [112] the so-called Y function, as shown in (2.3).

$$Y = \frac{I_d}{\sqrt{g_m}} = \left(\frac{W}{L} C_{ox} \mu_0 V_d\right)^{1/2} (V_g - V_t) = \sqrt{G_m}(V_g - V_t) \tag{2.3}$$

It can be observed how indeed Y is free from any effect of access resistance or any 1st order degradation: as a matter of fact when recalling how [112] applies Y to a 5 μm channel device, Y is extremely linear in the high V_g range. This property allows indeed to have a wide span of V_g for which $Y(V_g)$ is linear and we can therefore apply a simple linear regression with no doubt on the selected interval or the consequently extracted V_t.

Over time, many methods to extract/extrapolate V_t have been developed [30], but Y is the only one that visually simplifies the original idea to extract the intersection of the linear $I_d(V_g)$ with the x-axis. Section 1.2.3 reports how more modern devices suffer from mobility attenuation with V_g-dependence higher than first order: therefore, when considering Y, we would have to reformulate as:

$$Y = \sqrt{\frac{W C_{ox} \mu_0 V_d}{L[1 - \theta_2 (V_g - V_t)^2]}} (V_g - V_t) \tag{2.4}$$

Fleury et al. [113] have worked this matter suggesting in 2008 as correction for Y, based on a recursive type of algorithm as further explained in [114]. This gave the foundations for the algorithm mainly used throughout the present work. Therefore, we extrapolate an initial V_t as the x-axis intersection of the line which is tangent to $I_d(V_g)$ in the point where $g_m(V_g)$ has its maximum G_m; then, we move to a V_g value about 200 mV higher and firstly computed Y as in ([112]). This is in a second iteration corrected with the θ_2 extraction from (2.1), yielding Y', with a higher (if not total) degree of linearity in the high V_g region with respect to Y:

$$Y' = Y \sqrt{1 + \theta_2 (V_g - V_t)^2} \tag{2.5}$$

Moreover, Y is not only useful to extract the threshold voltage, but if coupled with measurements of gate-to-channel capacitance $C_{gc}(V_g)$ that allow us to extract the value of the oxide capacitance C_{ox}, it can provide the value of the low-field mobility μ_0:

$$\mu_0 = G_m \frac{L}{W} \frac{1}{C_{ox} V_d} \tag{2.6}$$

G_m being the square of the slope of $Y(V_g)$

This results in a good estimation of μ_0 independently from the weight of the attenuation factors, given the correction of Y to Y' has been performed properly; yet in our team's experience, one iteration has proven sufficient to reach this level. It is important to understand here the strength of the Y function: this is a tool that by definition is only looking at what happens in the inverted channel: if on one hand it needs to be applied exclusively in the strong inversion regime, on the other hand it leaves out anything outside the channel region.

It is now due to assert how Y has to be addressed in the low-temperature context. As it has already been shown in section 1.3.3, the effective mobility μ_{eff} in the transistor's

channel is different with respect to (V_g, V_t, θ_1, θ_2) as we move from room temperature down to the liquid-Helium temperature range. For this very reason, in 1989 Ghibaudo and Balestra [115] reformulated Y for deep cryogenic temperatures, in order to keep Y independent from any effect of series resistance:

$$Y_{\text{liquid He}} = \frac{I_d^{2/3}}{g_m^{1/3}} = \left(\frac{W}{L} C_{ox} \mu_0 \theta_{\text{liquid He}} V_d\right)^{1/3} (V_g - V_t) \tag{2.7}$$

Finally Emrani [116] generalized Y as both a function of V_g and n (power exponent for the mobility law) so to have Y(V_g, n) evolving continuously and smoothly across the full temperature range:

$$Y(V_g, n) = (I_d^2/g_m)^{1/n} \tag{2.8}$$

We have seen how from 1988 to 2008, Y has been rephrased to face throughout time the challenges of emerging technologies or research field (such as cryogenics). But it is now time to fast forward to present days, where indeed the technologies at hand are tackling the nanometer scale and the temperatures are facing units of Kelvin: indeed, according to our experimental experience, we have well seen that all of the devices we have characterized could, with good approximation, be analysed with a simple Y function corrected by θ_2 (1 iteration only!). Moreover, as shown by [39], the attenuation factors above the first order account together for surface roughness and are inter-correlated, giving us good confidence on Y-based analysis only for what concerns V_t, μ_0, $theta_1$, and R_{SD} (see next subsection). To better inspect the effect of surface roughness at deep cryogenic temperature, the Lambert-W function proved more effective thanks to its recursive self-calibrating algorithm (see section 3.4).

Although, we have only so far talked about Y applied to the linear region (low $V_d << V_g$-V_t) in strong inversion (high gate overdrive V_g-V_t), Diouf [117] applied the original Y from 1988 [112] to the saturation (high V_d) region of n- and p- MOSFETs. Moreover [118] has applied Y to the characterization of ultra-thin-body (UTB) and gate-recessed-channel (GRC) transistors, showing great benefit from the method thanks to a good estimation of R_{SD}, which was very influential in the latter devices.

2.2.3 Source-to-Drain resistance

As shown in the previous subsection, the square of the slope of Y returns the theoretical peak value G_m of the trans-conductance. Indeed, recalling equation (2.2), we can plot the first order attenuation factor for different G_m peaks, each corresponding to a different channel length.

Therefore, given the accuracy of the effective channel length L_{eff} taken into consideration, we extract R_{SD} as the slope of $\theta_1(G_m)$ at a fixed temperature, as follows:

$$R_{SD} = \frac{d\theta_1}{dG_m/V_d} \tag{2.9}$$

3. *FDSOI MOSFETs*

This chapter is dedicated to the analysis of an industrial-level class of FDSOI devices fabricated by LETI CEA in collaboration with STMicroelectronics. To get into more details, these devices belong to a 28nm technology of fully depleted Silicon on insulator (FDSOI). Also, they present a high-k metal gate processed through a Gate-First architecture [119]. They present a thickness t_{Si} of the Silicon film of 7 nm, while the buried oxide is 30nm (t_{BOX}) thick, as shown in Figure 3.1. Moreover, the equivalent oxide thickness (EOT) is of 1.7 nm. More specifically, we only measured devices with n-type Source and Drain, working at positive biasing of the gate ($V_g > 0$ V).

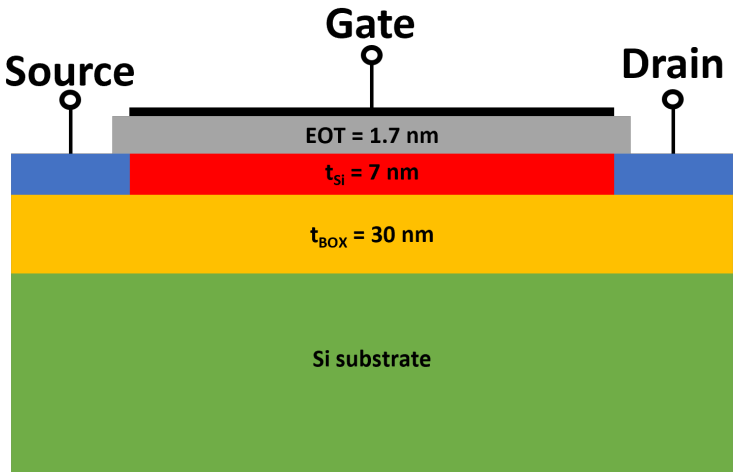


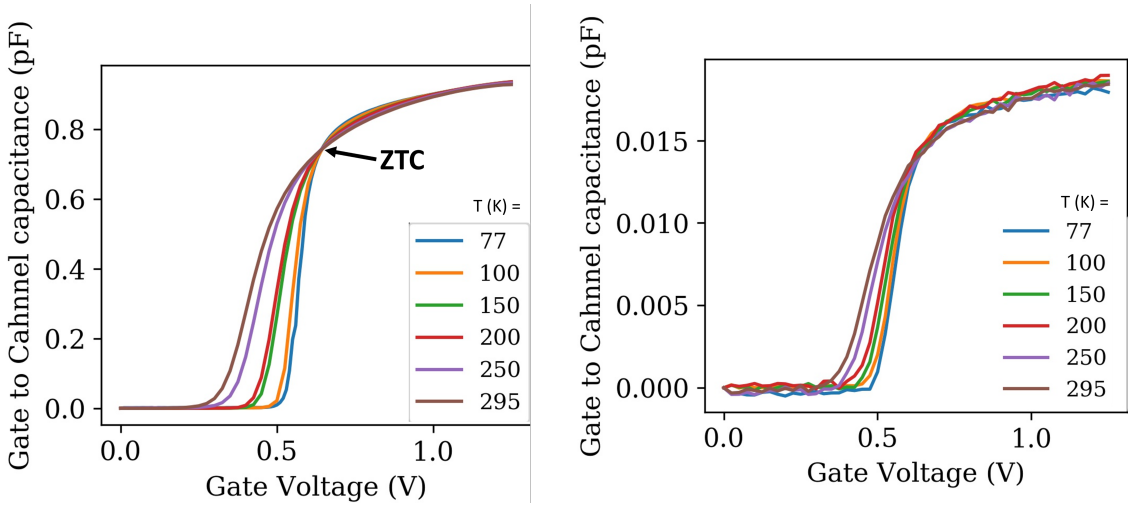
Figure 3.1: *qualitative structure of FDSOI by LETI CEA*

3.1 C-V analysis

As explained in 1.2.1, the basic component of a MOSFET is actually a MOS capacitor, whose value of the oxide capacitance C_{ox} plays a crucial role in the inversion of carrier charges at the interface, therefore affecting the magnitude of the output current of the device itself. Furthermore, the Y function, as many (if not the entirety) current-based extraction methods are not able to discriminate in between μ_0 and C_{ox}, but they only see their product as an effective quantity. As a consequence, if on one hand, the $\mu_0 C_{ox}$ product has a satisfying definition at the means of modeling, on the other hand, when characterizing the devices and their materials, this has to be broken apart to actually quantify and contextualize the variations of the low-field mobility, particularly with regards to a varying temperature as in the case of the present work.

Therefore, the study and characterization of these devices started in our case with the split-capacitance measurement (C-V) to determine C_{ox}. Due to the limitations (sensitivity) of the instrument (Figure 2.3b), the area of the measured device needs to be sufficiently big: we found that in the case of this technology, the limit was an oxide gate area of $\sim$1 μm^2. As we look at the raw measurements of the gate-to-channel capacitance in Figure 3.2, we see that although a bit of noise at high values of the gate voltage for the smaller geometry (Figure 3.2b), the 2 measurements were quite consistent and stable with temperature. This is indeed a confirmation of the high industrial level of the technology, which as a matter of fact, can be expected in the case of fully depleted silicon devices.

Moreover, from Figure 3.2a, given the cleanliness of the signal, it is easy to determine the presence of the of the Zero Temperature Coefficient, which is the point where the $C_{gc}(V_g)$ curves cross independently of the temperature. This point is always present in the C-V measurement of a MOSFET and results from a mirroring of the evolution of the Fermi function with respect to temperature [120]. Finally, always recalling the shape and change of the Fermi distribution for decreasing temperature T, we can see how the raise of the measured capacitance towards the final C_{ox} value sharpens for lower T's: this will, as explained in in the first chapter, yield an improvement (i.e. sharpening) of the Subthreshold Slope in the output current of the device.



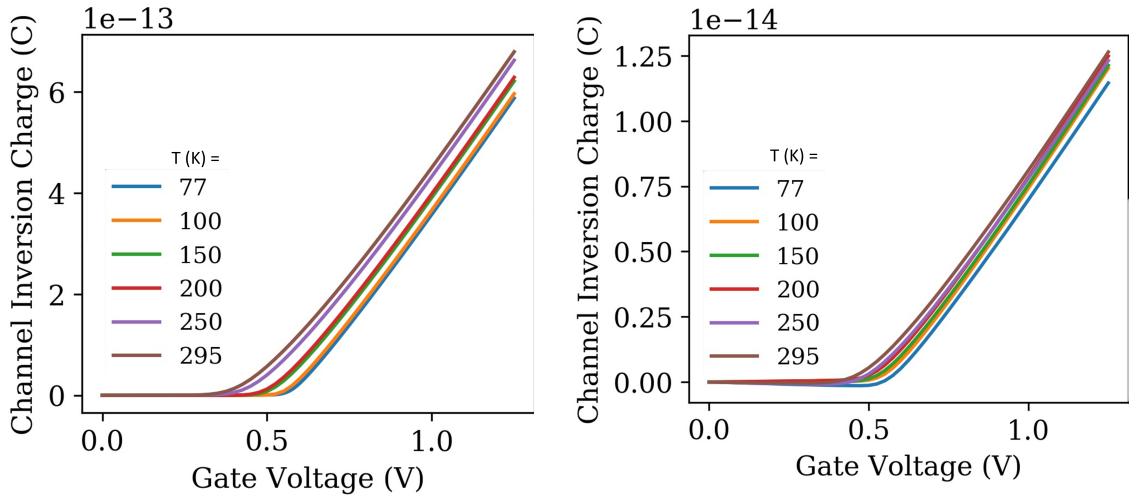
(a) W_g = 5 μm, L_g = 10 μm ***(b)*** W_g = 1 μm, L_g = 1 μm

Figure 3.2: *Gate-to-channel capacitance vs Gate voltage*

As we can see, the gate-to-channel capacitance C_{gc} varies with respect to the gate voltage V_g: this is due to its dependence form the inversion charge Q_i in the channel, being $C_{gc} = dQ_i/dV_g$. Therefore, we can rebuild Q_i from simply integrating C_{gc} over the gate voltage span. The reconstructed inversion charge is reported in Figure 3.3 for both geometries under study: the bigger one (Figure 3.3a) with gate width of 5 μm and length of 10 μm; the smaller one (Figure 3.3b) with gate width and length both equal to 1 μm.

If on one hand Q_i presents similar (if not parallel at all) slopes for the same device at different temperatures, it is clearly visible how these lines shift forward with respect to the gate voltage, as the temperature T decreases: this is a first, yet intuitive reminder of how the threshold voltage V_{th} is increasing at cryogenic temperatures, as yielded by the Boltzmann statistics (see section 1.3.1).

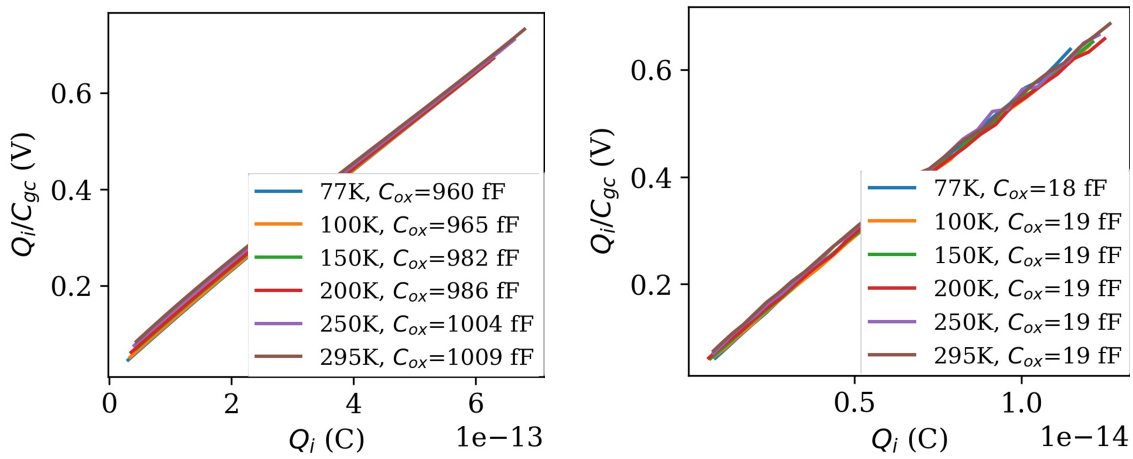
If we plot the ratio of the inversion charge Q_i by the gate-to-channel capacitance C_{gc}, with respect to the inversion charge itself, we see in Figure 3.4 juxtaposed straight lines for



(a) W_g = 5 μm, L_g = 10 μm *(b)* W_g = 1 μm, L_g = 1 μm

Figure 3.3: *Channel inversion charge vs Gate voltage*

all measurement temperatures. The inverse of the slope coefficient is in fact the effective value of the oxide capacitance C_{ox} of the device. As a further proof of the stability of these devices, not only the values of C_{ox} are reasonably stable from room temperature down to 77K, but when normalized by the area, they furthermore match between the two different geometries: this allows to confirm a value of roughly 2 μF/cm^2 for the oxide capacitance per unit area of these devices.



(a) W_g = 5 μm, L_g = 10 μm *(b)* W_g = 1 μm, L_g = 1 μm

Figure 3.4: *Extraction of the oxide capacitance through linearization*

It is finally worth making some considerations on Figure 3.5: it shows the evolution of the gate-to-channel capacitance $C_{gc}(V_g)$ for different values of the back bias V_b. As shown and explained in [90] and [63], it is possible to start carrier inversion in (”turn on”) the back channel of a MOSFET by applying a bias to the substrate.

In the specific case of the technology at hand, an increasingly positive back bias progressively strengthens the promotion of electrons to the conduction band in a physical region of the Si film very close to the buried oxide. Figure 3.5 shows how independently

from the temperature, the $C_{gc}(V_g)$ curves start their slope at lower values of the gate voltage for $V_b = 4$ V: indeed this is due to the presence of a back channel "turning on" before the main channel at the front gate.

Concerning the effects of cryogenic temperatures on the back bias, if we compare the 77 K (liquid N) and the 295 K (room temperature, RT) cases for the high values of V_b, the transition from back to front channel in the gate-to-channel curve becomes more evident. As explained in [71], as T gets lower the thickness of the inversion layers reduces, as if the inversion channel itself was compacting. This effect is indeed the reason why the separate effects of the two channels at 77 K become easier to distinguish: the separation in between the two improves, for they compact each towards their relative interface.

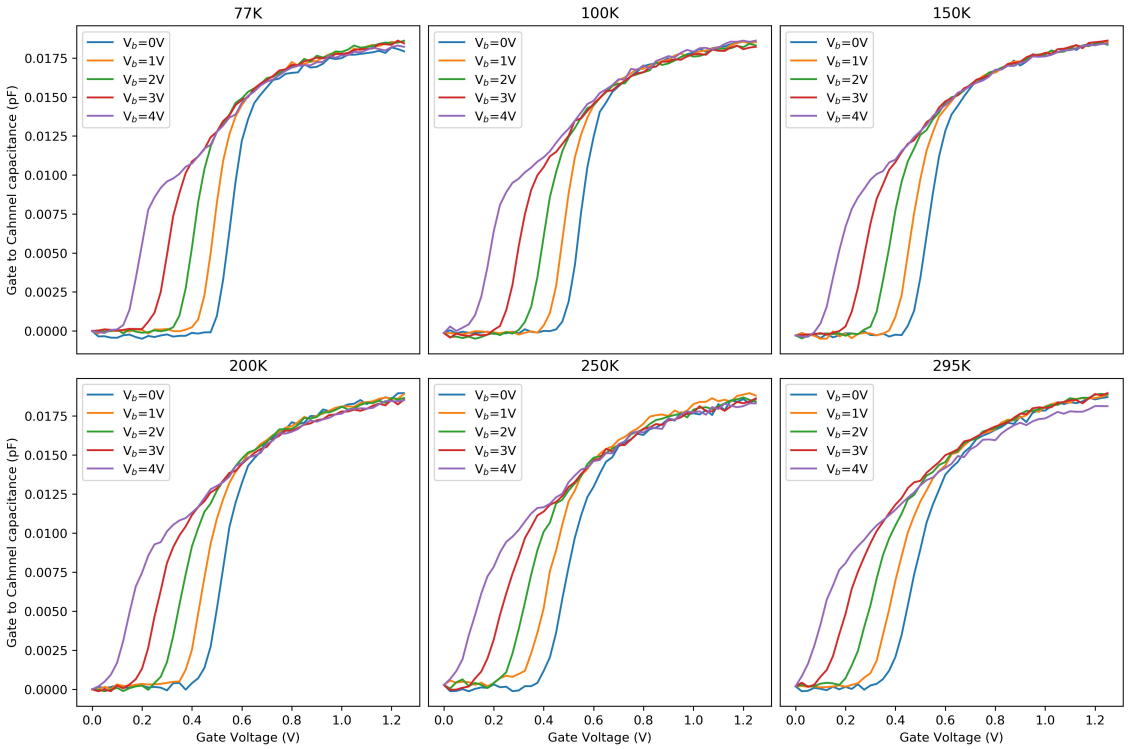


Figure 3.5: *Gate-to-channel capacitance measurement on a $W_g = L_g = 1$ μm geometry at different back biases*

3.2 Cryogenic electrical characterization

In order to study the main electrical parameters (i.e. the quality of the performance) of these devices, we started from the analysis of the transfer characteristics $I_d(V_g)$ at a low value of the drain voltage V_d, namely 30 mV, therefore operating the MOSFETs in the linear region of the output characteristics $I_d(V_d)$. This allowed firstly to apply the Y function to extract the parameters and secondly, to take them without any attenuation due to operating in saturation, as it is the case for the low-field mobility μ_0, which decreases for high values of the longitudinal field induced by V_d.

As we can see from Figure 3.6, having a first look at the transfer characteristics $I_d(V_g)$ of a relatively big (i.e. $W_g = L_g = 1$ μm) MOSFET, therefore slightly (if not at all) affected by short channel effects, this class of FDSOI falls in line with the three main predictions of low temperature as explained in Chapter 2. Indeed, from the plot in linear scale (on

the left vertical axis) it is clear how the threshold voltage increases and the value of I_d at high V_g is boosted for low temperatures. On the right side instead, the logarithmic plot reveals how the subthreshold region gets steeper and steeper, referring to a more abrupt switch-on/switch-off of the device.

Furthermore, at around $V_g = 0.75$ V, we can see a a quite clear appearance of the zero-temperature point. As explained by Catapano et al. in [120], in long channel devices the predominance of phonon-scattering-limited mobility allows to have a zero-temperature "region" that approximates much more a single point.

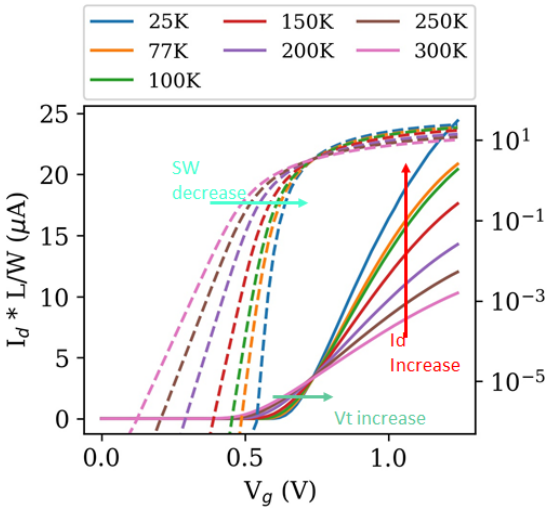


Figure 3.6: *Drain current as a function of the gate voltage for a $W_g = L_g = 1$ μm device, normalized by the length-to-width ratio [121]*

This part of the work, has focused on devices with a reasonably small area: they share a common gate width W_g of a 1 μm and gate length L_g spanning from 1 μm down to 30 nm. Particularly, in a first moment the characterization was only carried out down to 25 K, as published in the conference WOLTE14 in 2021 [121]. Given the good maturity and the high level of industrialization of this technology, this was already enough to show the trends of the main extracted parameters down to deep cryogenic temperatures.

As a matter of fact, Figure 3.7 compares the $I_d(V_g)$ on the longest and shortest devices. This does on a first stance, confirm the current boost typical of shorter channels and the threshold voltage V_t roll-off, which seems to appear independently of temperature. Also, the plot is showing how, once shorter channels are taken into account, a stronger sublinearity becomes more visible in the regions where the gate voltage takes higher values: indeed, this is the sign of a stronger mobility attenuation at shorter channels, as it will be better explained further in this section and in the modeling section of this same chapter.

Figure 3.8 offers a view on how the Y function is performing on this technology. Indeed Y has been thoroughly applied on FDSOI over the past, as shown in section 2.2.2. As a matter of fact Figure 3.8a show how the Y function is progressively evolving when T decreases down to 25K: it can be seen that linearity is well preserved throughout the whole temperature range, ensuring the correctness of this extraction method. On the right, Figure 3.8b shows instead the slope of Y for devices with different channel length L_g at 25K: in this way, we can verify that at deep cryogenic temperatures Y is preserving its linearity for all the geometries under study. From the previous observations, we can further proceed in processing the linear regression of Y to extract V_t and μ_0 as functions

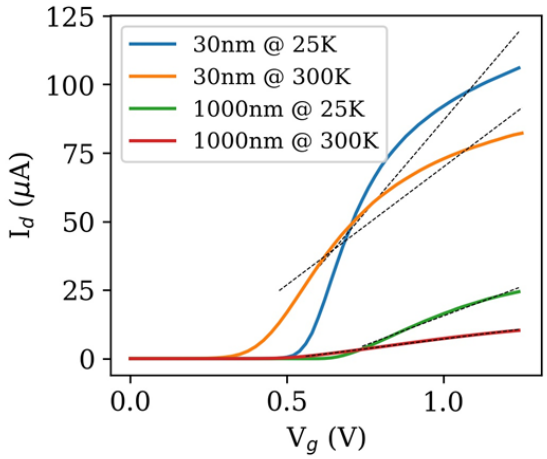
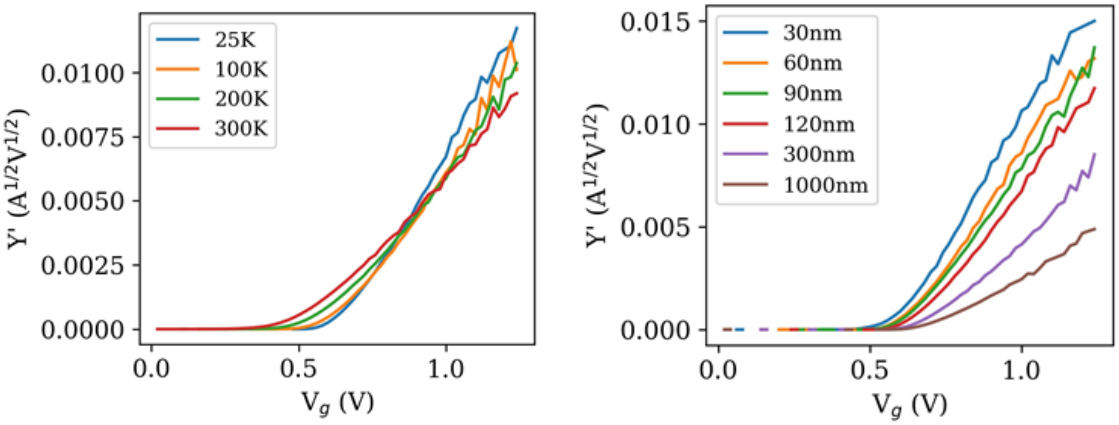


Figure 3.7: *Drain current as a function of the gate voltage, comparing the devices with L_g = 1 μm and 30 nm, normalizing by the length-to-width ratio [121]*

of T.



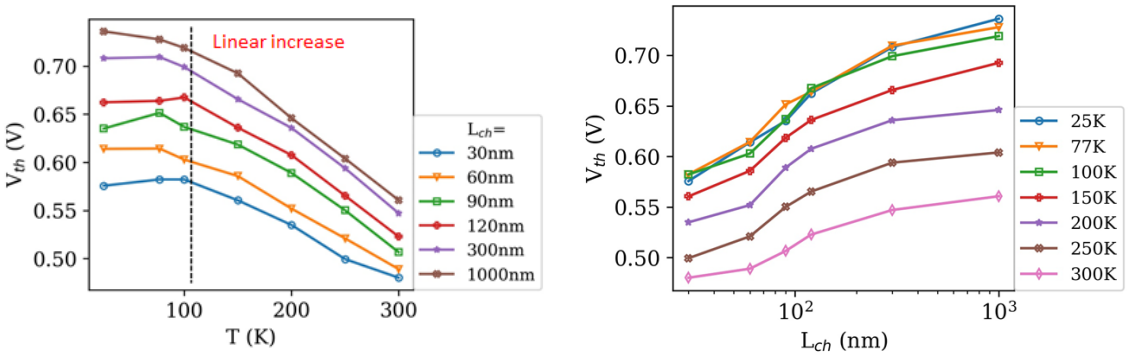
(a) *device gate length L_g = 120 nm* ***(b)*** *Temperature T = 25 K*

Figure 3.8: *Y function as a function of the gate voltage [121]*

Recalling the effects elucidated in Section 1.3.1, we can see the confirmation of the increase of V_t in Figure 3.9a: indeed, all devices, independently of their length, display a linear increase of the threshold voltage with respect to a decreasing temperature T. Yet, past the 100 K point, this increase settles to a more or less stable value: this is well explained by the semiconductor transitioning from a non-degenerate Boltzmann statistics to a degenerate one [16].

On the other hand, Figure 3.9b plots the same extracted values with respect to a varying gate length (L_g, in the axis figure). It is clearly visible how the threshold roll-off is almost perfectly preserved consistently for different T values: indeed it is important to recall that the gate electrostatics is supposed to be independent from the temperature and therefore for different T we should see the same decrease of V_t as we move towards shorter lengths.

Colder temperatures reduce the thermal vibration and in turn, the phonons in the lattice: as we would expect, in fact, the low-field mobility μ_0 is strongly boosted at deep

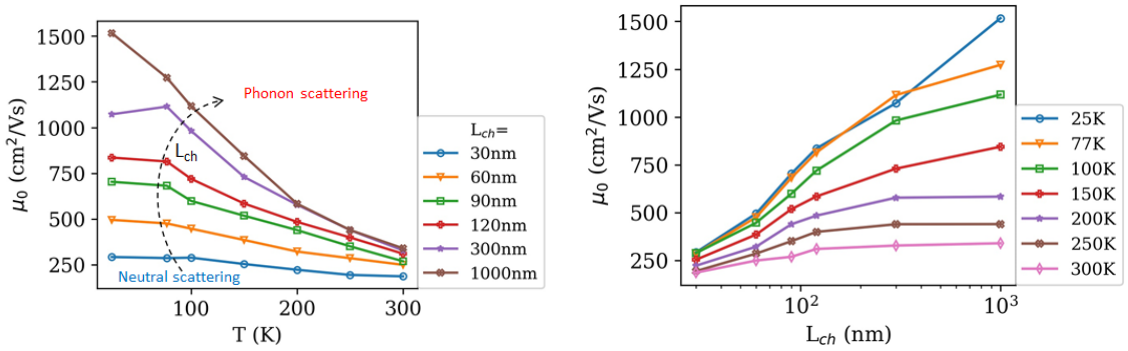


(a) with respect to the measurement temperature *(b) with respect to the device gate length*

Figure 3.9: *Extracted threshold voltage for different temperature and all measured devices [121]*

cryogenic temperatures. We can though see from Figure 3.10a that the low temperature-induced boost is more effective on longer-channel devices than on ones with a shorter channel: very simply, as the channel length reduces, Source and Drain regions get closer and the neutral impurities originating from their doping start to permeate a bigger percentage of the channel [50].

This effect is once more confirmed in Figure 3.10b: as phonon scattering is the predominant mobility-limiting mechanism in long-channel devices, the latter experience a strong increase in μ_0 at low T; yet, as in short-channel devices the predominant mechanism is neutral-impurities scattering, they barely show boost in the low-field mobility at all.



(a) with respect to the measurement temperature *(b) with respect to the device gate length*

Figure 3.10: *Extracted low-field mobility for different temperature and all measured devices [121]*

From a simple linearization of the logarithm of the subthreshold current with respect to the gate voltage V_g, we can extract the subthreshold slope , showing the quality of the switch-on/off of the device.

Given the high grade of maturity of this technology, it is no surprise that the room temperature values of the subthrehsold swing SW (inverse of the subthreshold slope) is so close to 60 mV/dec at room temperature: this is indeed the limit for Si MOSFETs [122]. However at room temperature, we can observe how, due to short channel effects, the subthreshold swing degenerates (i.e. increases) for the 60 and 30 nm devices, reaching for the latter a value of $\sim$80 mV/dec.

Yet, as our focus moves towards the very low temperatures, we see that all lengths settle around 10 mV/dec, which is the experimental limit for Si MOSFETs [73] due to the band tail states. Particularly, at low temperature, the short-channel effects for what concerns the increase of the subthreshold swing are reduced.

Figure 3.11 report the extracted values of the subthreshold swing for these 28nm FD-SOI devices. It has to be remarked that the measurements (going down to 10 K) were carried out in a later time with respect to the ones that gave the other results shown so far.

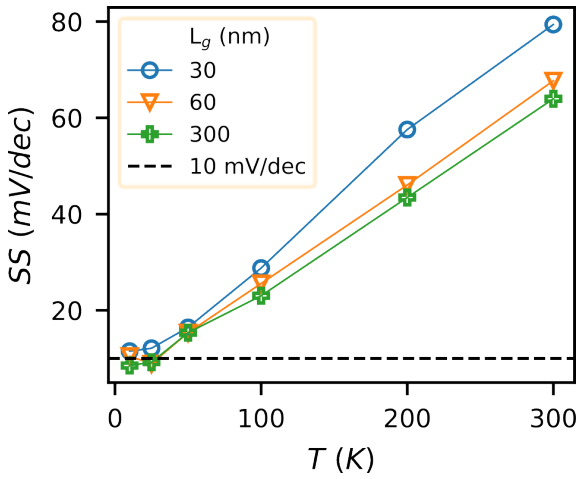


Figure 3.11: *Extracted subthreshold swing for all measured temperatures and devices*

Through the computation of Θ_{eff}, we can extract with good confidence θ_1, reported in Figure 3.12 versus T for several channel lengths. Independently from the operating temperature, θ_1 has a heavier impact in short-channel devices: indeed, as the channel length decreases, so does the channel resistance R_{ch}, becoming more and more comparable to the one originating from the access regions, which in turn gains more impact.

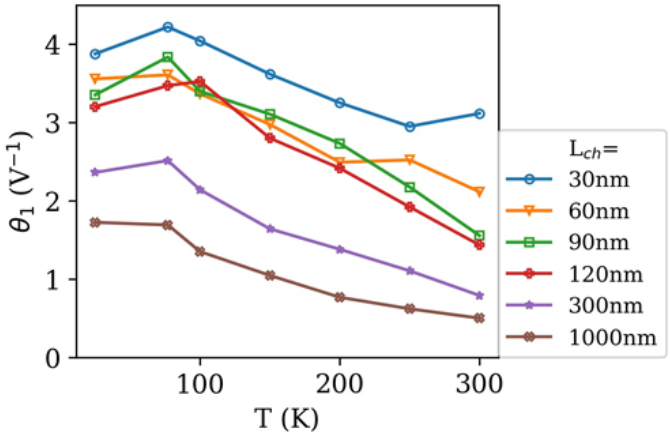


Figure 3.12: *Extracted first-order attenuation factor θ_1 for all measured devices, with respect to temperatures [121]*

Recalling $\theta_1 = \theta_{1,0} + G_m R_{SD}$, Figure 3.13 clearly shows the linear dependence of the first-order attenuation factor on the squared slope G_m of the Y function. Moreover, for every temperature, we can extract the slope of this linear dependence, being in fact R_{SD}(T), which is finally shown in Figure 3.14.

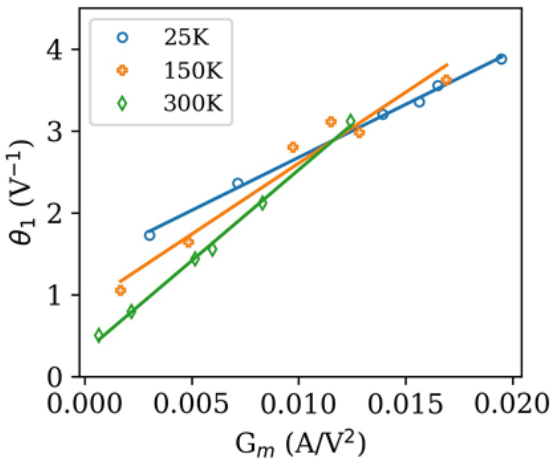


Figure 3.13: *Extracted first-order attenuation factor θ_1 with respect to the peak G_m of the trans-conductance g_m [121]*

As expected, the Source-Drain resistance displays a metallic behavior with respect to temperature, therefore decreasing together with a decreasing T, down to a final remaining value which may correspond to the contact resistance.

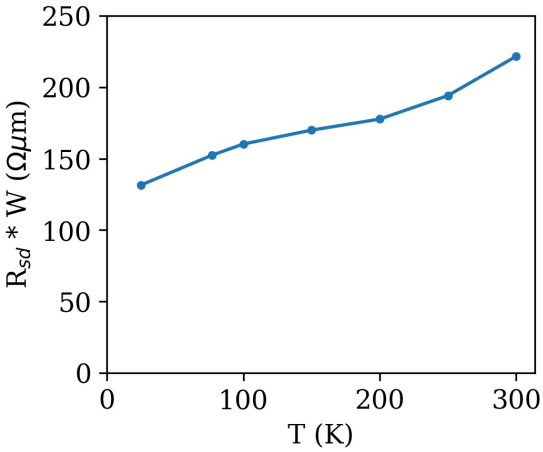


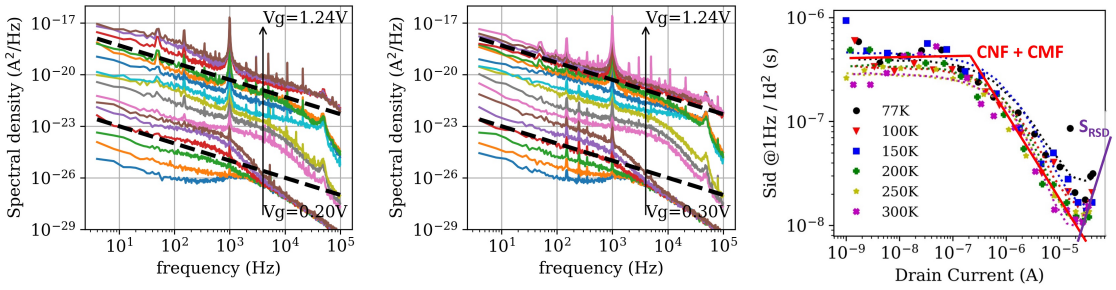
Figure 3.14: *Extracted average of the Source-to-Drain resistance with respect to temperature [121]*

3.3 Low-frequency noise

Low-frequency noise analysis was carried out on this technology from room temperature down to liquid Nitrogen temperature on a device with Gate length and width both equal to 1 μm. The influence of bottom gate bias was also examined. As can be seen from figures 3.15a and 3.15b, this FDSOI technology kept displaying a 1 over f behavior from 300 K down to 77 K. Therefore, we normalized with respect to the square of the Drain current the PSD at 10 Hz, as reported in Figure 3.15c.

Indeed, we were able to analyze all the normalized spectra with a Carrier Number Fluctuation model coupled with correlated mobility fluctuations (CNF +CMF). As it can

be seen in Figure 3.15c, there was a slight influence of the access resistance on the normalized PSD at high Gate biases.

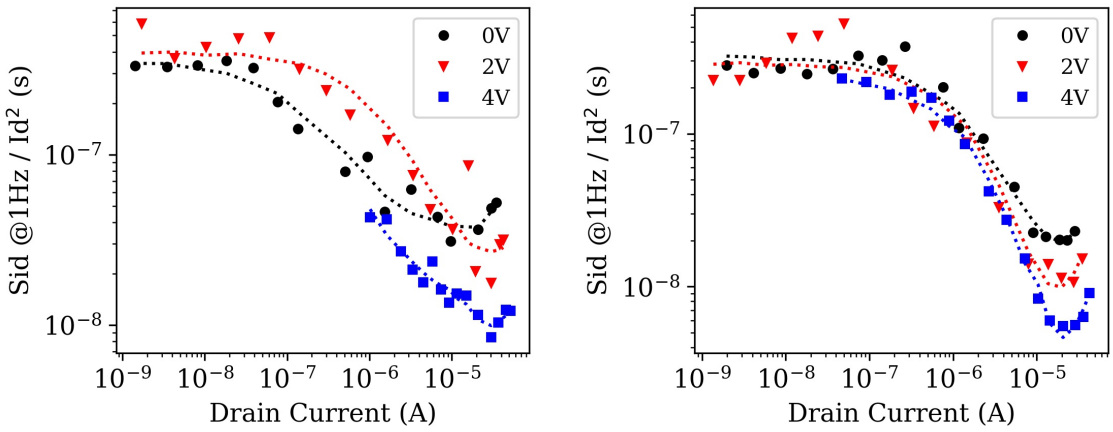


(a) PSD at 77 K *(b) PSD at 300 K* *(c) Normalized PSD*

Figure 3.15: *Figures of merit from the noise analysis of Si FDSOI at V_B = 0 V. The black dashed lines in (a) and (b) show a pure 1/f trend for reference*

Figure 3.16 shows the normalized PSD for different values of the back bias, V_B and as dotted lines, the fittings according to the CNF + CMF model. From Figure 3.16a, we can see how at 77 K the S_{I_d}/I_d^2 changes with a V_B increasing from 0 up to 4 V. Yet, for all values of the back bias, the normalized spectra can be analyzed with a CNF + CMF model.

Conversely, at 300 K, as shown in Figure 3.16b, the spectra seem to remain more invariant with respect to a changing back voltage, at least at low values of the Gate bias. At higher V_g, we can see a possible reduction of both CMF and $S_{R_{SD}}$ influence. Concerning the remote Coulomb scattering, it has been shown in [123] how moving the channel position towards the bottom interface by applying positive V_b can actually decrease the CMF strength, due to the distance created between electrons and trapped charges. As for the $S_{R_{SD}}$, it's reduction with V_b could mean that it actually originates from the junction regions between channel and S/D instead of the contacts. In that scenario, a lower $S_{R_{SD}}$ when the channel is positioned closer to the bottom interface means that the junction quality is improved closer to the BOX. As for the 77 K case, all spectra could be analyzed with the CNF + CMF model.



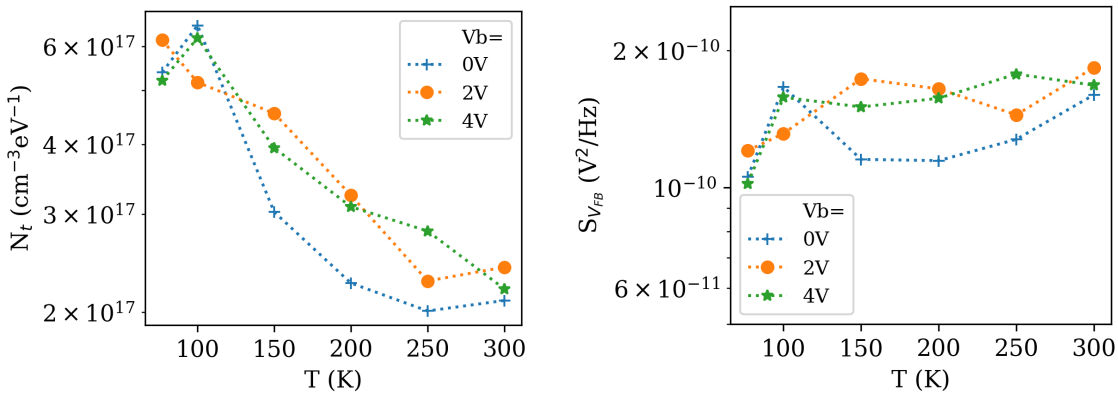
(a) T = 77 K *(b) T = 300 K*

Figure 3.16: *Normalized PSD with respect to the temperature, for different values of V_B*

Finally, Figure 3.17 reports two crucial parameters that have been extracted from this

low-frequency noise analysis of this 28nm Si FDSOI technology. Figure 3.17a reports the trap density at the interface with respect to temperature and for different back bias points. As it has already been reported in [91, 90], we can see here as well find that increasing level of the trap density as we move towards lower temperature. This has been attributed to band tails by Asanovski et al. [91], however a different explanation was given by Ghibaudo [124]. Also, the trap density is displaying similar values independently from the applied back bias.

Figure 3.17b shows instead the flat-band voltage PSD, $S_{V_{fb}}$ for different values of V_B and with respect to the temperature. As also reported by [90] for a similar 22nm Si FDSOI technology, $S_{V_{fb}}$ is about constant with respect to temperature; particularly, in this specific case, we measured a value around $1.5\text{x}10^{-10}$, that moreover seems not to variate with respect to the increasing value of V_B.



(a) *Trap density* ***(b)*** *Flat-band voltage PSD*

Figure 3.17: *Extracted noise parameters for FDSOI 28 nm*

3.4 Lambert-W modeling

In recent years, MOSFET parameters were also extracted at cryogenic temperatures using compact models like, e.g., EKV in FDSOI MOS devices [125] or BSIM in bulk MOS transistors [126]. In addition, a full gate voltage range Lambert-W function-based methodology was recently developed allowing electrical parameters extraction in FDSOI MOSFETs at room temperature [69]. It should also be mentioned that the Lambert-W function has been used for the MOSFET modeling as it is a rigorous solution of undoped body MOS transistors [127] and an approximate solution for a doped MOS device [128].

In this section it is reported how the Lambert-W (LW) function has been applied for the inversion charge and drain current modeling as a function of gate voltage and, by turn, for MOSFET parameter extraction down to deep cryogenic temperatures. To this end, we first show the validity of the Lambert-W function for the description of the gate-to channel capacitance and inversion charge with gate voltage from weak to strong inversion in large area 28 nm FDSOI MOSFETs down to liquid helium temperatures. Then, we demonstrate the applicability of the Lambert-W function-based method to fit the drain current down to very low temperatures using a classical mobility law, providing the dependence of subthreshold slope ideality factor, threshold voltage and mobility parameters with gate length and temperature.

To properly calibrate this model we incorporated to the experimental data from the previous section additional CV and IV measurements on a W_g = L_g = 10 μm device belonging to the same technology [129]. The gate-to-channel capacitance $C_{gc}(V_g)$ was measured with an HP 4284 LCR meter at 1MHz frequency and 10mV AC level using the standard split C-V technique. The drain current $I_d(V_g)$ MOSFET transfer characteristics were recorded in linear region (V_d = 30-50 mV) with an HP4156 parameter analyzer. All the measurements were made at zero back bias. Influence of body bias can be found in [130].

The MOSFET parameter extraction was performed on the $C_{gc}(V_g)$ and $I_d(V_d)$ characteristics using the same Lambert-W function based procedure as in for room temperature. The equations and parameters used for the curve modeling are recalled below.

The $C_{gc}(V_g)$ and $Q_i(V_g)$ curves were fitted with Equations (3.1) and (3.2) with C_{ox} and b as fitting parameters [69]:

$$C_{gc}(V_g,T) = \frac{bQ_iC_{ox}}{C_{ox}+bQ_i} \tag{3.1}$$

$$Q_i(V_g,T) = C_{ox}\eta k_BT/qLW(e^{\frac{V_g-V_t}{\eta k_BT/q}}),$$

with

$$LW(e^{\frac{V_g-V_t}{\eta k_BT/q}}) = \left(ln(1+\lambda)\frac{1-ln(1+ln(1+\lambda))}{2+ln(1+\lambda)}\right)^{-1}, \tag{3.2}$$

where

$$\lambda = exp\left(\frac{V_g-V_t}{\eta k_BT}\right)$$

$$\frac{Q_i}{C_{gc}} = \frac{1}{b}+\frac{Q_i}{C_{ox}} \tag{3.3}$$

where k_BT/q is the thermal voltage, C_{ox} is the gate oxide capacitance, η is the subthreshold slope ideality factor, V_t is the threshold voltage and with b=q/(ηk_BT).

The effective mobility μ_{eff} and $I_d(V_g)$ curves were modeled using Equations (3.4) and (3.5) with fitting parameters η, V_t, μ_0, θ_1 and θ_2 [69]:

$$\mu_{eff}(Q_i) = \frac{\mu_0}{1+\theta_1(Q_i/C_{ox})+\theta_2(Q_i/C_{ox})^2} \tag{3.4}$$

$$I_d(V_g,T) = \frac{W}{L}\mu_{eff}Q_iV_d \tag{3.5}$$

A conventional Levenberg-Marquardt algorithm was used for the curve fitting optimization. $C_{gc}(V_g)$ characteristics were measured on large area MOSFETs with W_g = L_g = 10 μm for better accuracy. The inversion charge was obtained after integration of the $C_{gc}(V_g)$ curves starting from V_g = 0 V as it is usual in split C-V technique. Typical $C_{gc}(V_g)$ and associated $Q_i(V_g)$ characteristics are shown in Figure 3.18 (a)-(b)-(c) for various temperatures from 300K down to 4.2K. Note the steeper onset of the inversion charge with the temperature lowering. As proposed in [131, 132], the plot Q_i/C_{gc} vs Q_i (Figure 3.18(d)) can be used, according to Equation (3.3), to extract the gate oxide capacitance from the slope, giving here $C_{ox} \approx 2$ μF/cm^2 independently of temperature. Indeed, the nice superposition of the $Q_i/C_{gc}(Q_i)$ curves for all the temperatures is revealing the rather temperature independence of the slope and so of C_{ox}.

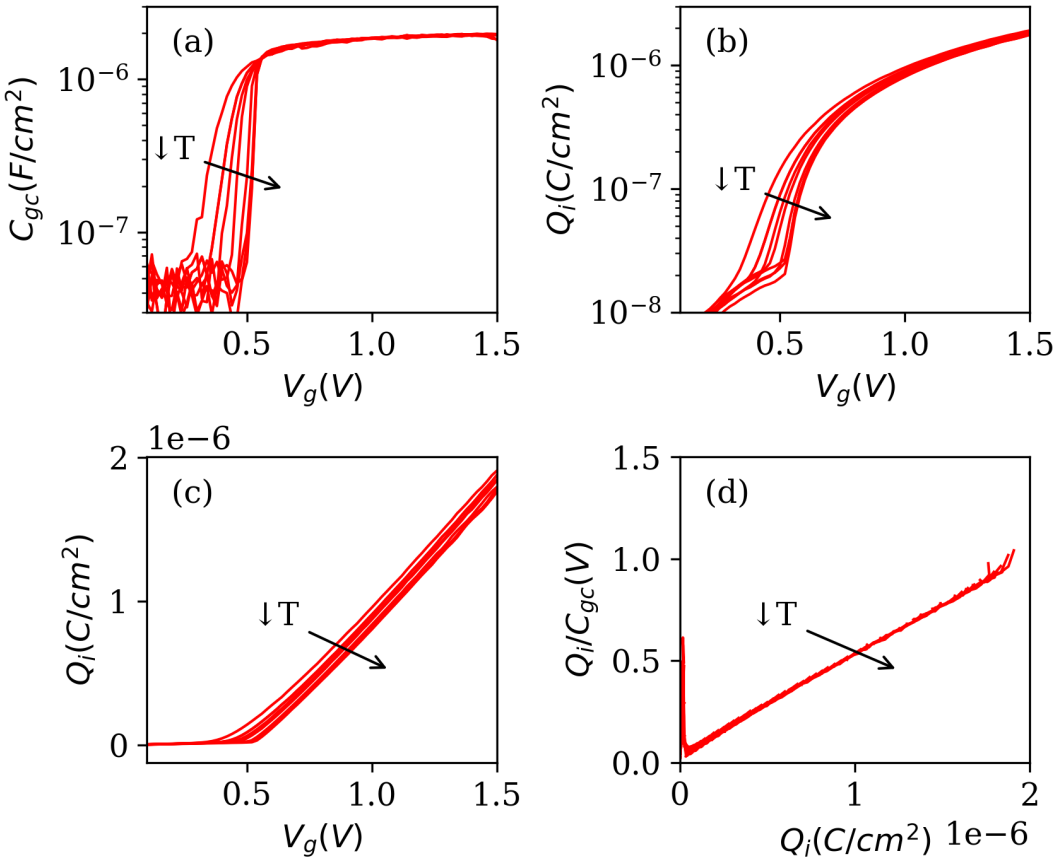


Figure 3.18: *$C_{gc}(V_g)$ (a), $Q_i(V_g)$ (b) and (c), and $Q_i/C_{gc}(Q_i)$ (d) characteristics for various temperatures T(K) = 4.2, 10, 20, 50, 100, 150, 200, 250 and 300 (W_g = L_g = 10 μm) [129]*

Figures 3.19 (a)-(b)-(c) show the best fits of the $Q_i(V_g)$ and $C_{gc}(V_g)$ characteristics, which can be obtained with the Lambert-W function model of Equations (3.1) and (3.2) for temperatures varying from 300 K down to 4.2 K. The extracted fitting parameters for V_t and η are plotted in Figure 3.19 (d), indicating a quasi-linear increase of V_t with temperature decrease and a ≈1/T dependence of η (see below). The excellent agreement achieved between model and experiment emphasizes the validity of the Lambert-W function to adequately describe the capacitance and inversion charge MOSFET characteristics with respect to the gate voltage down to deep cryogenic temperatures. The latter feature fully justifies that the Lambert-W $Q_i(V_g)$ model can further be used for the drain current transfer characteristics modeling and, by turn, MOSFET parameter extraction.

Drain current $I_d(V_g)$ transfer characteristics were first measured in linear region (V_d = 50 mV) on long channel FDSOI MOSFETs with W_g = L_g = 10 μm to obtain the intrinsic parameters free from source/drain access resistance effect. Typical drain current $I_d(V_g)$, trans-conductance $g_m(V_g)$ and Y-function $Y(V_g) = I_d/\sqrt{g_m}$ characteristics are shown in Figure 3.20 (red solid lines) for various temperatures from 300 K down to 4.2 K. Similarly, one can notice again the strong increase of the subthreshold slope with the temperature decrease, as well as the significant increase of drain current at high gate voltage, maximum trans-conductance and average Y-function slope with temperature lowering. The three latter features are related to the improvement of the carrier mobility as the temperature

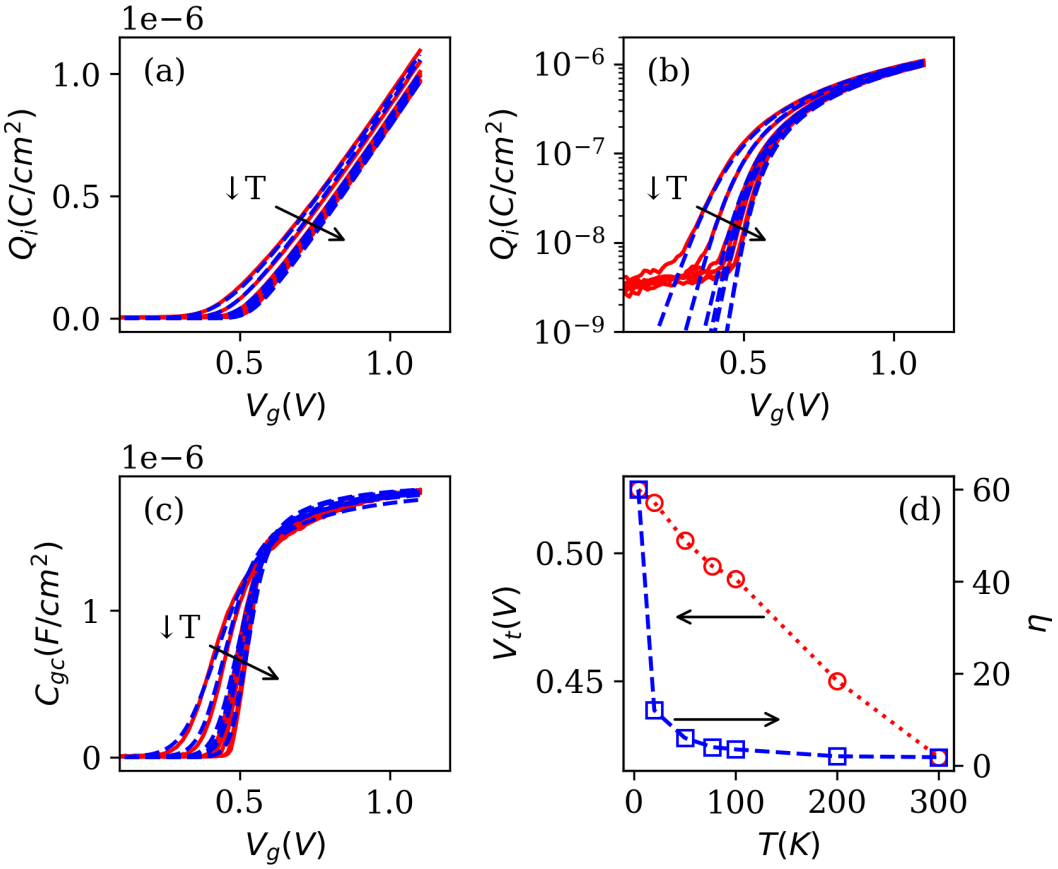


Figure 3.19: *Experimental (red solid lines) and Lambert-W model fitted (blue dashed lines) $Q_i(V_g)$ (a) and (b), $C_{gc}(V_g)$ (c) characteristics for various temperatures T(K) = 4.2, 20, 50, 77, 100, 200 and 300 (W_g = L_g = 10 μm). (d) V_t and η parameter variations with temperature T [129]*

is reduced, as will be shown below. Moreover, a zero temperature coefficient (ZTC) bias point [133] is also noticeable on all characteristics above threshold, around Vg=0.6V.

Figure 3.20 also displays the best fits of the $I_d(V_g)$, $g_m(V_g)$) and $Y(V_g)$ characteristics (blue dashed lines), which can be reached with the Lambert-W function model of Equations (3.2), (3.4) and (3.5) for temperatures ranging from 300 K down to 4.2 K. The very good agreement between model and experiment underlines the usefulness of the Lambert-W function to effectively describe the drain current, the trans-conductance and the Y-function as a function of gate voltage from weak to strong inversion, using a classical mobility law given by Equation (3.4) down to very low temperatures.

The extracted fitting parameters V_t, η, μ_0, θ_1, and θ_2 obtained from Figure 3.20 are plotted in Figure 3.21 as a function of temperature. As in the C-V extraction, the threshold voltage V_t is increasing almost linearly with the temperature reduction before saturating, whereas the ideality factor η nearly varies as 1/T. The low field mobility μ_0 increases with temperature lowering, as is usual, due to phonon scattering reduction [**chapter 1**, 49], before saturating. Both V_t and μ_0, flattening at very low temperature likely stems from inversion layer degeneracy [**chapters 1&2**, 49]. The first-order mobility attenuation coefficient θ_1 lies around ≈ -1 V^{-1} ($\pm$15%) over the temperature range, while the second-order attenuation coefficient θ_2 increases from 0.8V^{-2} to 1.6V^{-2} as the temperature is

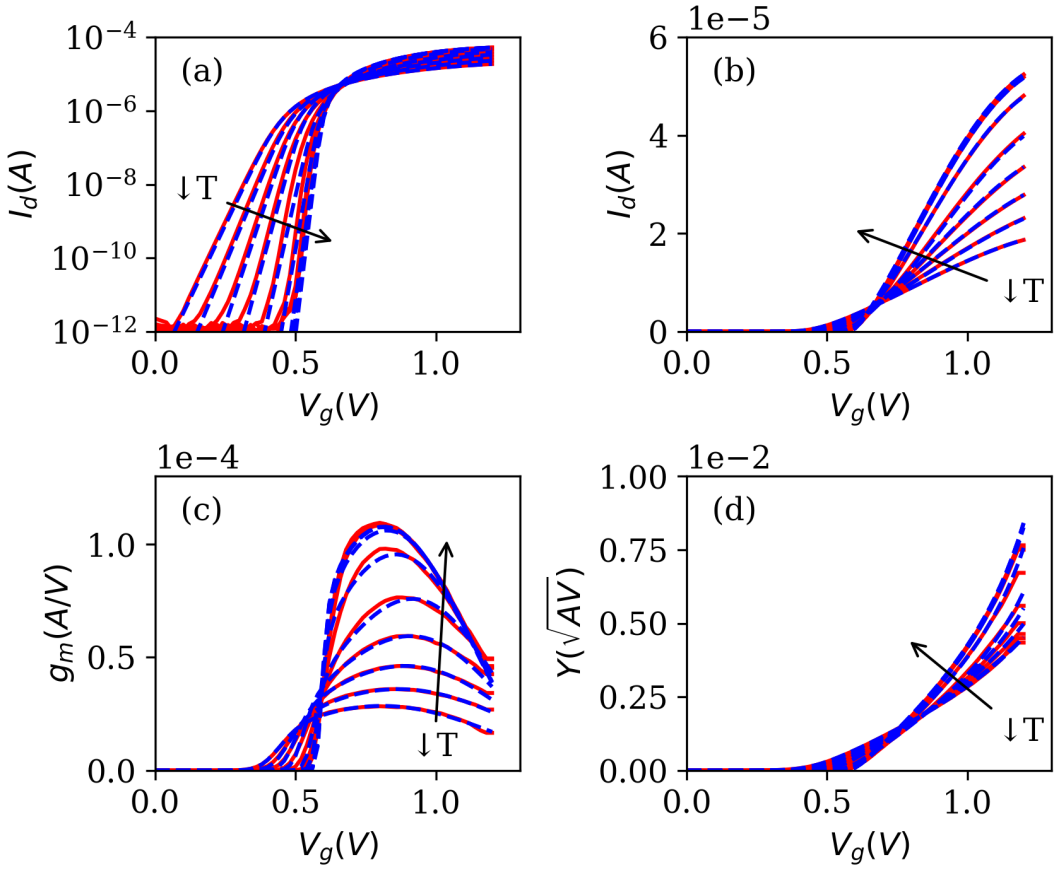


Figure 3.20: *Experimental (red solid lines) and Lambert-W model fit (blue dashed lines) $I_d(V_g)$ (a) and (b), $g_m(V_g)$) (c) and $Y(V_g)$ (d) characteristics for various temperatures T(K) = 4.2, 10, 20, 50, 100, 150, 200, 250 and 300 (V_d = 50 mV, W_g = L_g = 10 µm) [129]*

reduced. The latter θ_2 feature is related to the higher influence of surface roughness scattering at lower temperatures as the carriers get closer to the oxide/channel interface [**chapters 1&2**, 49].

It is also worth noticing in Figure 3.21 that the Lambert-W function extracted parameters V_t, η, μ_0 are close to those obtained by the Y-function method [112, 134], emphasizing once more the consistency of the Lambert-W function methodology.

The effective mobility μ_{eff} obtained from the Lambert-W function fits and defined in Equation (3.4) has been plotted in Figure 3.22 (a) (red solid lines) and compared to the effective mobility determined by standard split C-V method based on $Q_i(V_g)$ data of Figure 3.18 and drain current curves of Figure 3.20 (blue dashed lines). As can be seen, both μ_{eff} values merge well at moderate and strong inversion, while strongly differing just above and below threshold. The latter point can be explained, on one hand, by the finite μ_{eff} value (= μ_0) inherent to the classical mobility law used in Equation (3.4) reached below threshold, and, on the other hand, by the erroneous μ_{eff} zero value returned by the split C-V method close to and below threshold [135, 136]. Nevertheless, it should be noted that the maximum μ_{eff} values, μ_{max}, obtained by both methods and plotted in Figure 3.22 (b) are very close to each other, which proves again the physical consistency of the mobility extracted by the Lambert-W function fits. It is worth noting that the negative values of θ_1 obtained by the Lambert-W extraction allow modeling the increase

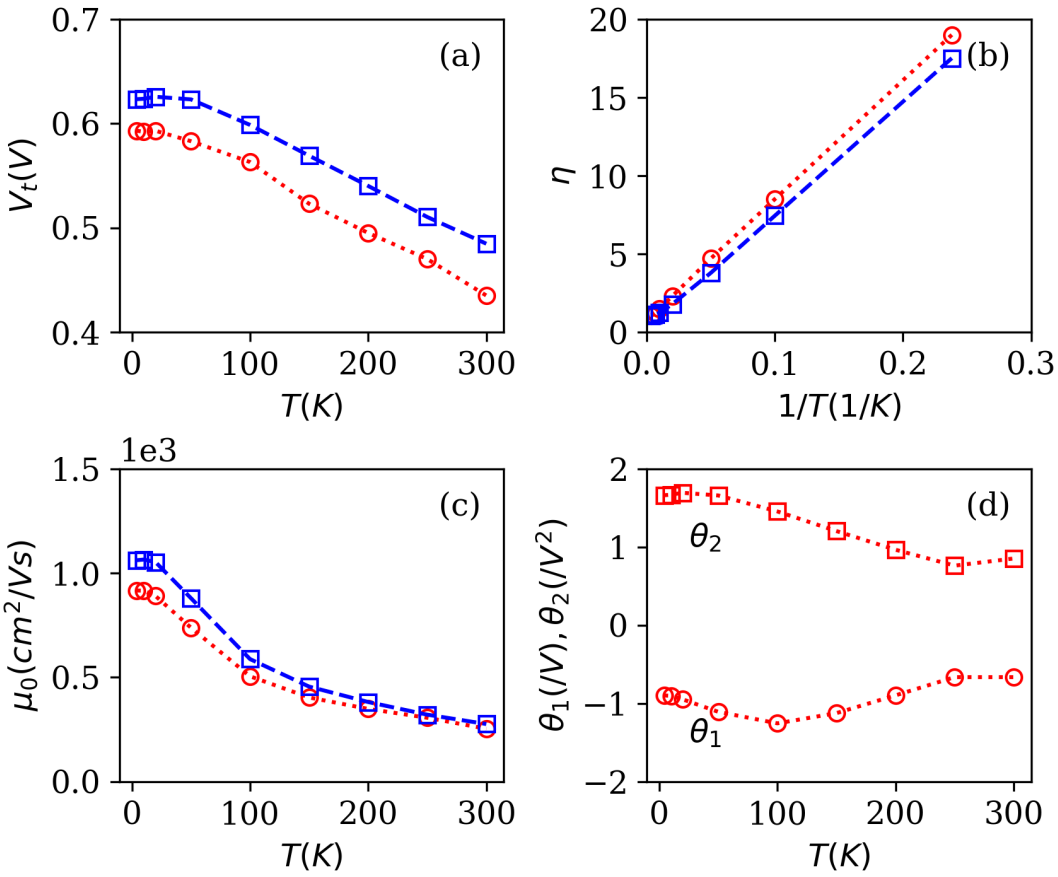


Figure 3.21: *V_t (a), η (b), μ_0 (c) parameter variations as extracted from Lambert-W function fits (red dotted lines) and from Y-function method (blue dashed lines), andθ_1 and θ_2 (d) versus temperature (V_d = 50 mV, W_g = L_g = 10 μm) [129]*

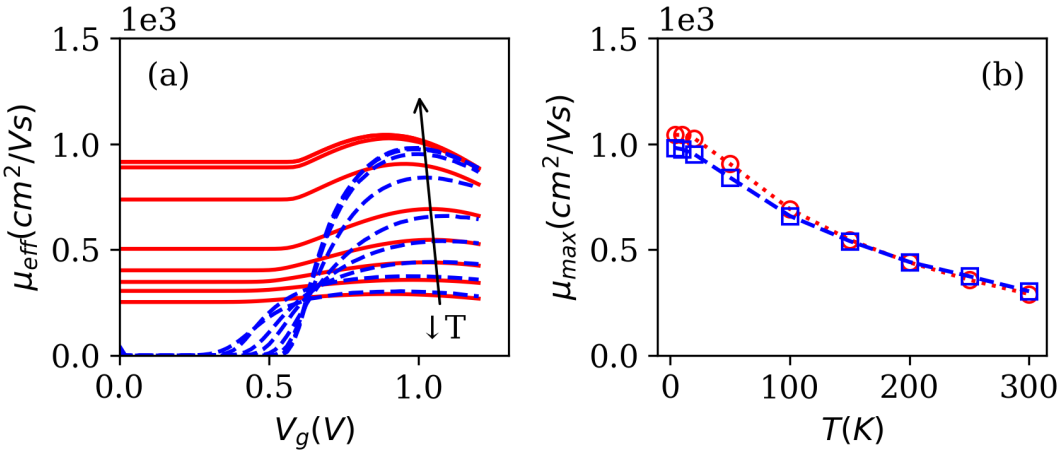


Figure 3.22: *(a) μ_{eff} variations with V_g and (b) maximum μ_{eff} variations with temperature as obtained from Lambert-W function fits (red lines) and split C-V technique (blue dashed lines). (V_d = 50 mV, W_g = L_g = 10 μm) [129]*

of μ_{eff} above threshold. This is necessary for mimicking the low temperature mobility law where Coulomb scattering induces such a mobility increase at very low temperatures [137, 58].

Drain current $I_d(V_g)$ transfer characteristics were then measured in linear region (V_d = 30 mV) on short channel FDSOI MOSFETs with gate length varying from 30 nm up to 1 μm and gate width W_g = 1 μm. Typical drain current $I_d(V_g)$, trans-conductance $g_m(V_g)$ and Y-function $Y(V_g)$ characteristics are presented in Figures 3.23 and 3.24 (red solid lines) for these various gate lengths and for T = 300 K and T = 25 K, respectively. Note the excellent vertical scaling of the characteristics with the gate length reduction for both temperatures.

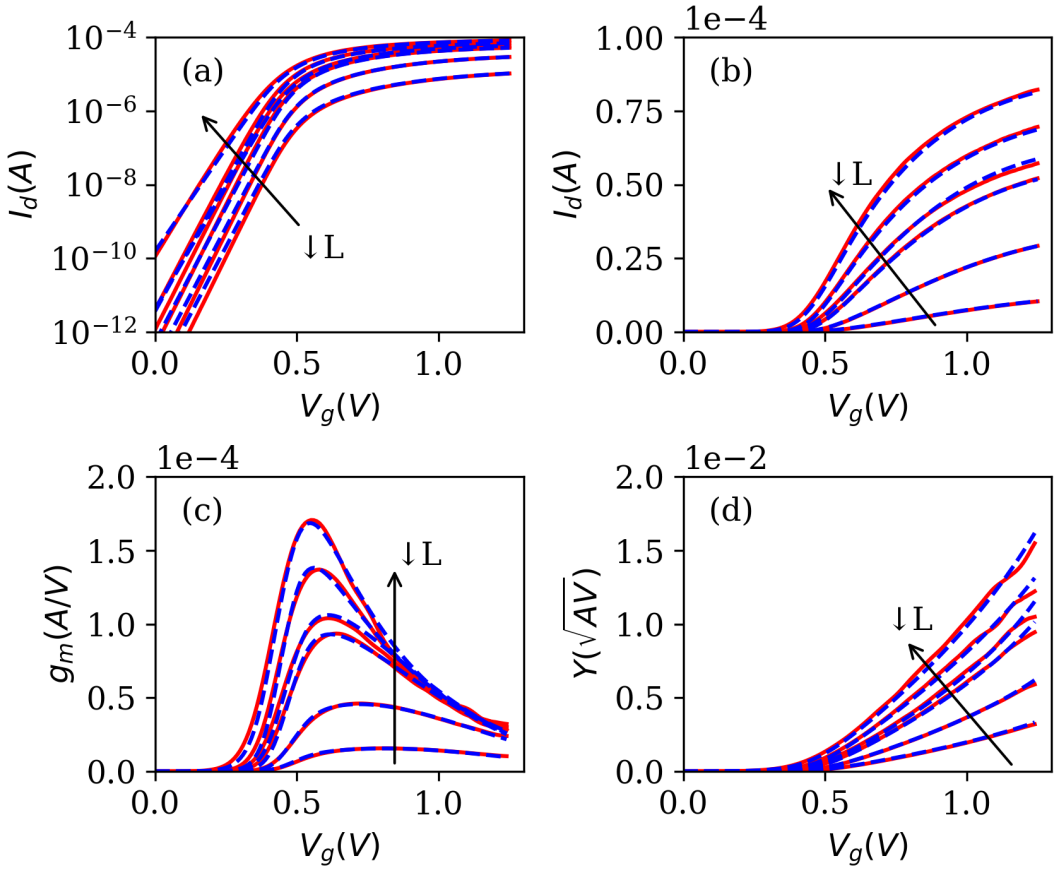


Figure 3.23: *Experimental (red solid lines) and Lambert-W model fit (blue dashed lines) $I_d(V_g)$ (a) and (b), $g_m(V_g)$ (c) and $Y(V_g)$ (d) characteristics for various gate lengths L(nm) = 30, 60, 90, 120, 300 and 1000 measured at T = 300 K (V_d = 30 mV, W_g = μm) [129]*

Figures 3.23 and 3.24 also illustrate the best fits of the $I_d(V_g)$, $g_m(V_g)$ and $Y(V_g)$ characteristics (blue dashed lines), which can be obtained with the Lambert-W function model of Equations (3.2), (3.4) and (3.5) for the corresponding experimental data. The overall good agreement between model and experiment infers again the effectiveness of the Lambert-W function to properly describe the transfer characteristics, even in short channel MOS devices, as a function of gate voltage from weak to strong inversion using a classical mobility law down to very low temperatures.

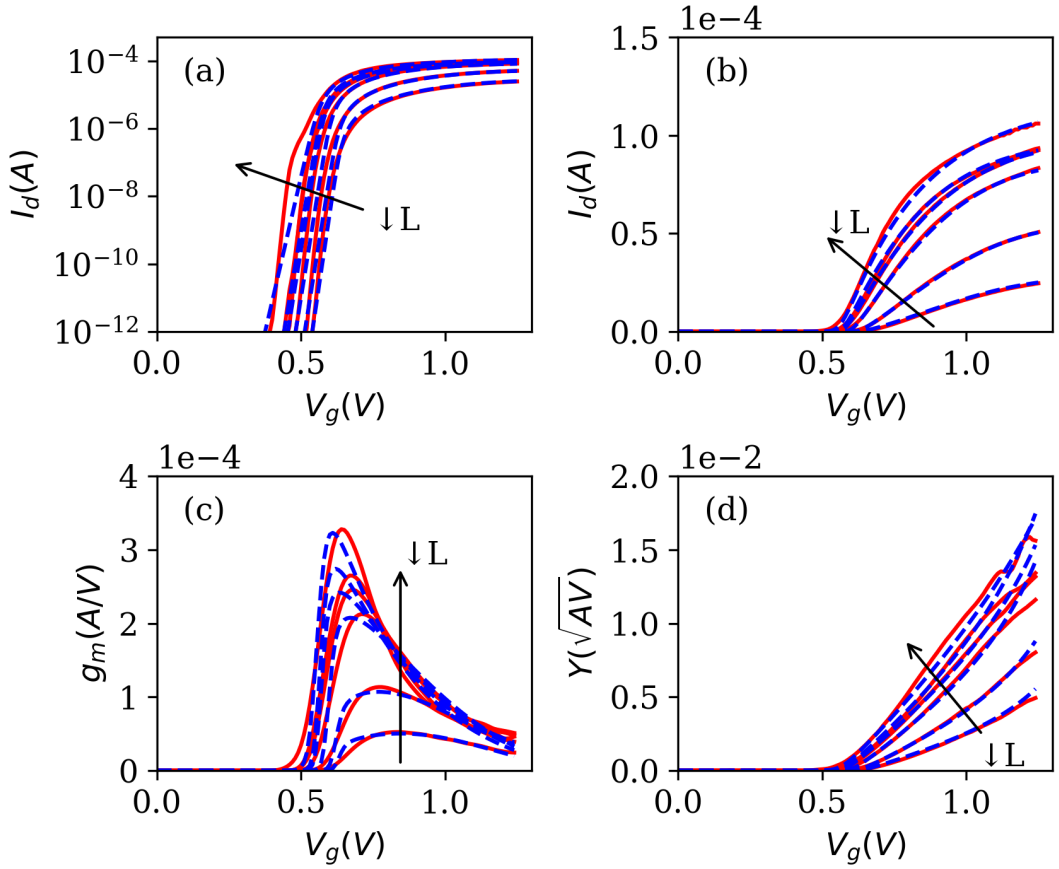


Figure 3.24: *Experimental (red solid lines) and Lambert-W model fit (blue dashed lines) $I_d(V_g)$ (a) and (b), $g_m(V_g)$ (c) and $Y(V_g)$ (d) characteristics for various gate lengths L(nm) = 30, 60, 90, 120, 300 and 1000 measured at T = 25 K (V_d = 30 mV, W_g = μm) [129]*

The extracted fitting parameters V_t, μ_0, θ_1, and θ_2 obtained from Figures 3.23 and 3.24 are plotted in Figure 3.25 versus gate length and for various temperatures from 25 K to 300 K. As can be seen, the threshold voltage V_t is exhibiting a small roll-off vs gate length due to short channel effects (SCE), whose trend are nearly independent of temperature, as expected, since SCE are mainly controlled by the device electrostatic properties [**chapter 1**, 49]. The low field mobility μ_0 displays a degradation as the gate length is reduced, more significant for lower temperatures. This mobility collapse has been previously attributed to enhanced defective scattering at small channel length, likely due to neutral point defects located near source and drain regions [136, 50]. The first order mobility attenuation coefficient θ_1 strongly increases, almost independently of temperature, as the channel length is reduced, due to the larger impact of access resistance R_{SD} in θ_1 expression (see Equation (3.4), [69]). Instead, the second order attenuation coefficient θ_2 weakly decreases with the gate length reduction, likely due to the decreased influence of vertical field in short devices.

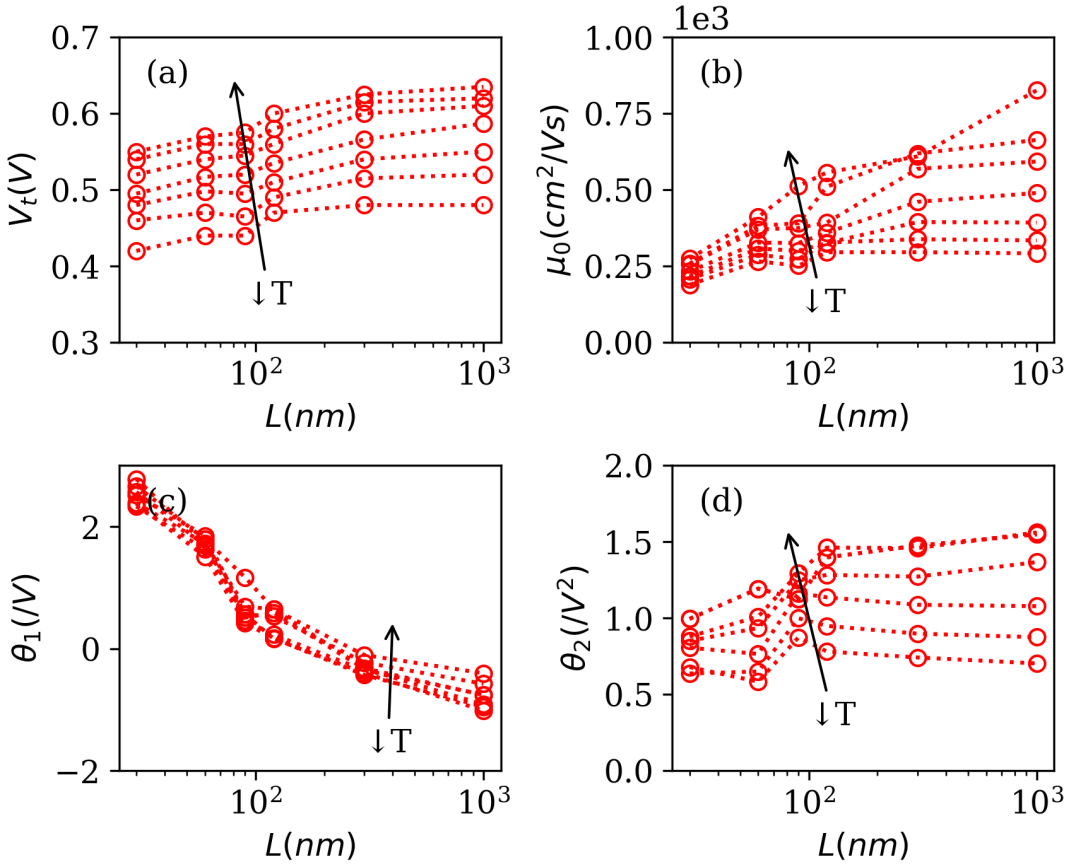


Figure 3.25: *V_t, μ_0, θ_1, and θ_2 parameter variations with gate length as extracted from Lambert-W function fits for various temperatures T(K) = 25, 77, 100, 150, 200, 250 and 300 (W_g = μm) [129]*

The extracted fitting parameters V_t, μ_0, θ_1, and θ_2 have also been plotted in Figure 3.26 versus temperature for various gate lengths in order to better analyze the temperature influence. As can be seen, the threshold voltage V_t varies in the same way with respect to temperature for long and short channel devices, as being governed by the same carrier statistics. In contrast, the low field mobility μ_0 variations with temperature clearly reveal a strong change in scattering mechanism signature, evolving from phonon-controlled one in long devices ($\propto T^{-1}$) to neutral defect one ($\propto T^0$) in short channels, as already reported for advanced CMOS technologies [136, 50]. The first order mobility attenuation coefficient θ_1 is nearly constant with temperature, whereas the second order attenuation coefficient θ_2 increases with temperature lowering, similarly for all gate lengths, likely due to the higher influence of surface roughness scattering at lower temperatures.

It is also worth mentioning that, following the mobility scattering analysis of [136, 50], the low field mobility μ_0 variations with channel length and temperature have been well modeled by Equations (3.6), in which the Matthiessen rule is used to combine phonon and neutral scattering mechanisms as,

$$\mu_{0,mod} = \left[\frac{1}{\mu_{ph}} \cdot \frac{T}{300} + \frac{1}{\mu_N} \cdot \left(1 + \frac{L_C}{L}\right)\right]^{-1} \tag{3.6}$$

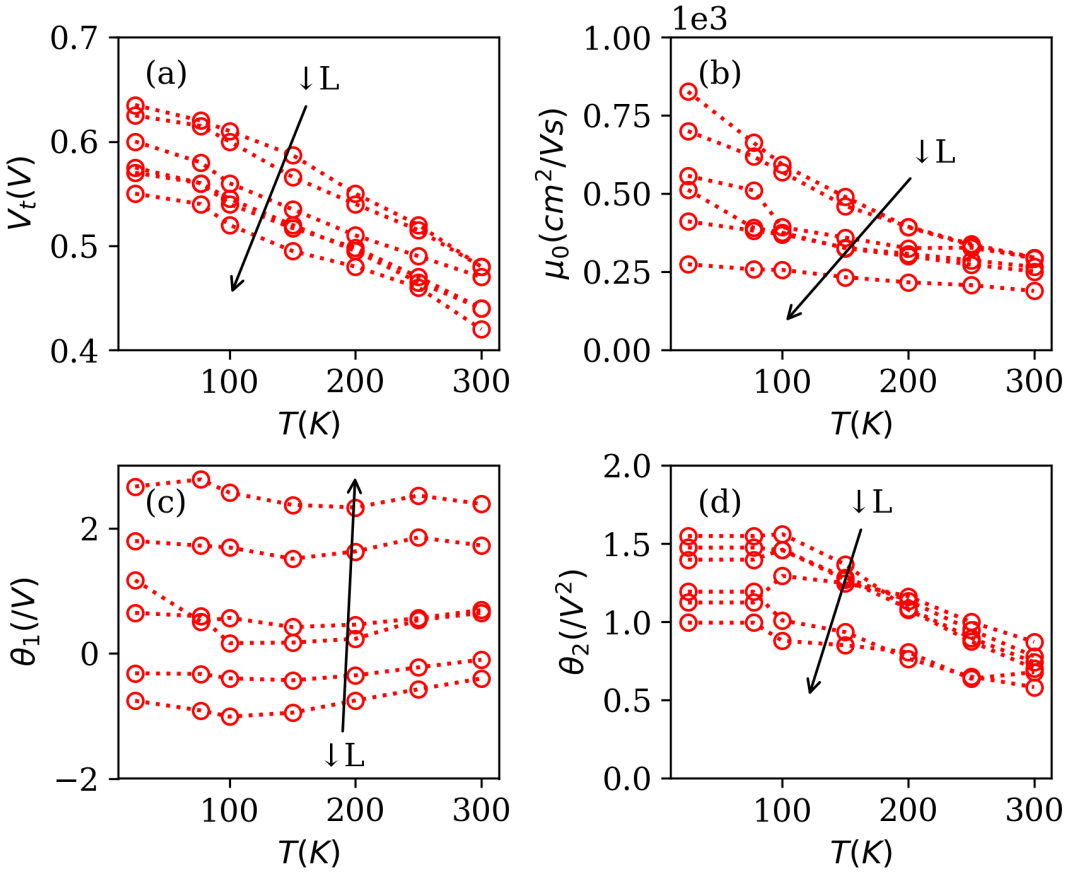


Figure 3.26: *V_t, μ_0, θ_1, and θ_2 parameter variations with gate length as extracted from Lambert-W function fits for various gate lengths L(nm) = 30, 60, 90, 120, 300 and 1000 (W_g = μm) [129]*

where μ_{ph} is the phonon-limited mobility at room temperature, μ_N is the temperature independent neutral defect-limited mobility for long channel, L_C being a critical channel length. As a matter of fact, Figure 3.27 (a) and (b) shows the best fits which can be achieved with Equation (3.6) on the low field mobility data of Figure 3.21(c) and Figure 3.26(b) with only 3 parameters (μ_{ph}, μ_N, L_C). In Figure 3.27 (c) and (d) are also displayed the variations of the neutral defect scattering rate percentage, % neutral, versus gate length and temperature, clearly revealing its increase with gate length reduction and/or temperature lowering. Therefore, these results confirm once more that the mobility degradation observed at short gate length in this 28nm FDSOI technology can be well interpreted by the enhanced presence of neutral defects as the channel is reduced, as was previously observed in other CMOS technologies [136, 50]. Moreover, it should also be mentioned that these low field mobility variations with channel and temperature are in full agreement with those obtained from Y-function extraction on the same technology [121], which emphasizes again the relevance of the Lambert-W function-based parameter extraction methodology for FDSOI MOSFETs.

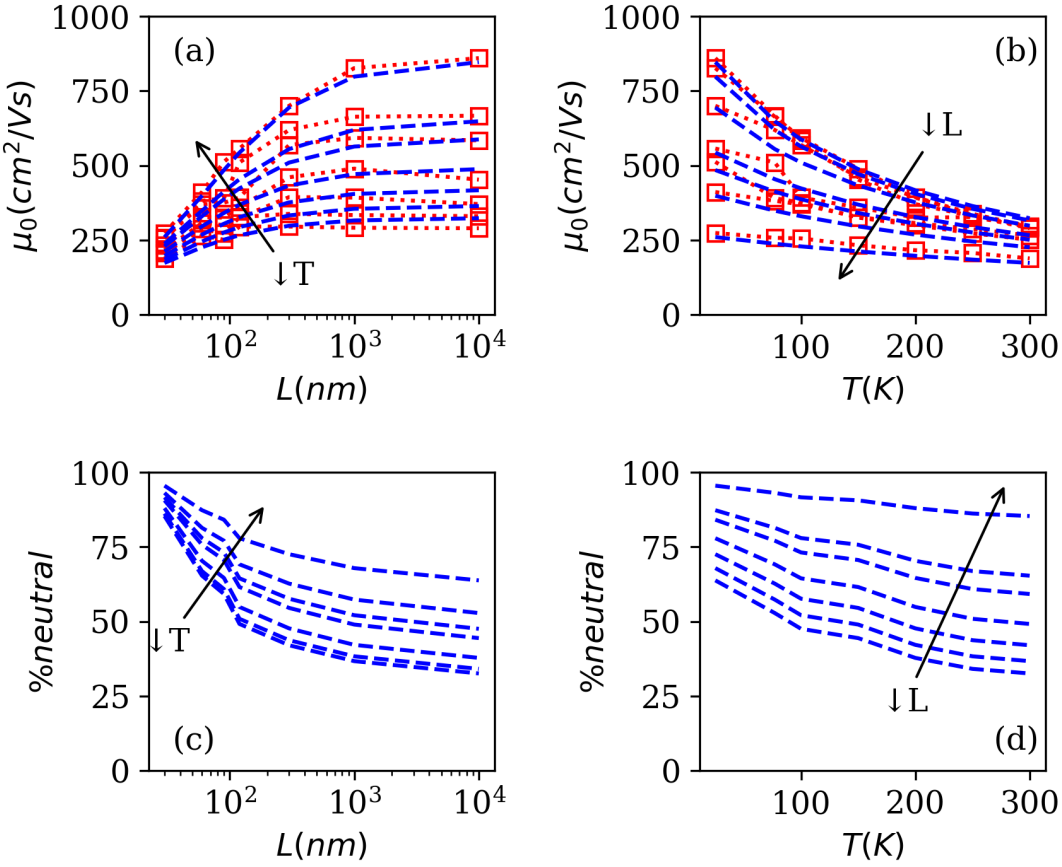


Figure 3.27: *Experimental (red dotted lines) and modeled (blue dashed lines) variations of low field mobility μ_0 with channel length (a) and temperature (b) as obtained from Equation (3.6) with parameters μ_{ph} = 480 cm^2/Vs,μ_N = 1000 cm^2/Vs and L_C = 80 nm (Experimental data from Figs 4c and 9b). Variations of the neutral defect scattering rate percentage % neutral versus gate length (c) and temperature (d) as obtained from mobility modeling with Equation (3.6) [129]*

Finally, Figure 3.28 (a) shows that the increase of the ideality factor η with the temperature reduction is similar for all gate lengths, with larger values for shorter devices due to short channel effect. Actually, this increase of η at lower temperature can be explained by the saturation of the subthreshold swing (SW) for temperatures below 30-40 K, since we have η = SW/(k$_B$T/q) [74, 73]. Figure 3.28 (b) displays the variations of the first order mobility attenuation coefficient $theta_1$ with the gain factor parameter β(L), parametrized by the channel lengths for various temperatures. As can be seen, θ varies linearly with β as expected due to the increased influence of R$_{SD}$ as the gate length is reduced. As is usual [69, 112], the access resistance is extracted from the slope $\theta_1(\beta)$, giving typical values of R$_{SD}$W varying from 230 to 260 $\Omega \cdot \mu$m for temperatures increasing from 25 K to 300 K (Equation 3.4).

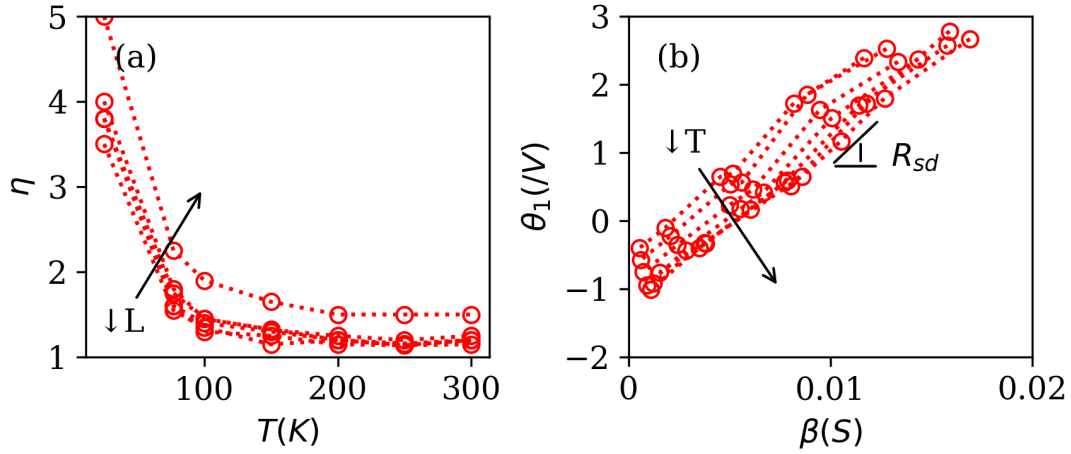


Figure 3.28: *(a) η parameter variations with temperature for various gate lengths L(nm) = 30, 60, 90, 120, 300 and 1000. (b) θ_1 parameter variations with β = W·Cox·μ_0/L gain factor for various temperatures T(K) = 25, 77, 100, 150, 200, 250 and 300 (W_g = μm) [129]*

3.5 Kubo-Greenwood integral modeling

Over the years, the Kubo-Greenwood integral for the conductivity [58] has been employed several times in an effort to describe and predict meticulously the behavior of MOSFETs and similar devices: [59] modeled bulk Si MOSFETs across a temperature range, [138] Si FDSOI, [139] bulk Si finFETs, and so many more works...

In the present section, starting from the work of [58] and [59], we applied and adapted the Kubo-Greenwood formulation on the the class of 28nm-FDSOI described in this section. We will therefore proceed step-by-step into the model starting by recalling:

1. g: subband degeneracy factor

2. m_d^*: DOS effective mass

3. $\hbar$: reduced Plank constant

4. k_BT: thermal energy

which can be combined into

$$A_{2D} = gm_d^*/(\pi\hbar) \text{ : 2D density of states} \tag{3.7}$$

We can thus proceed into the block that serve to the integral itself,

$$\begin{aligned} \sigma_E(E) &= qEA_{2D}\mu(E) \text{: energy conductivity function} \\ f &= 1/\left(1 + e^{\frac{E-E_f}{k_BT}}\right) \text{ : Fermi function} \end{aligned} \tag{3.8}$$

Starting from the single 2D subband approximation of inversion layer carrier density,

$$n(E_f, T) = kTA_{2D} ln\left(1 + e^{\frac{E_f - E_C}{k_B T}}\right) \tag{3.9}$$

We can finally proceed into the formulation of the Kubo-Greenwood integral describing the inversion layer sheet-conductivity,

$$\begin{gathered}\sigma(E_F, T) = \int_0^{+\infty} \sigma_E(E)\left(-\frac{\partial f}{\partial E}\right) dE \\ \text{which in our case can be resolved as } = \frac{\mu_{eff}}{qn(E_F, T)}\end{gathered} \tag{3.10}$$

As the effective mobility comes into play, we have to recall how in the channel the former can be limited by different scattering mechanisms. These each give rise to their own scattering-limited mobility: this one is the value the mobility would take, or better, be limited to, if only a specific scattering mechanism was active. Considering four different scattering processes, we get the following respective mobilities:

$$\begin{gathered}\mu_{ph}(T, F) = 1180\left[\left(\frac{T}{300}\right)^{2.11} + \left(\frac{T}{300}\right)^{1.7}\left(\frac{F}{F_0}\right)^{\alpha(T)}\right]^{-1}, \\ \mu_C(\mathrm{E}) = 1341\left(\frac{E}{E_{Coul}}\right) \text{ or } \mu_{C,eff}(n, T) = \left[\mu_C(2k_B T)^{a} + \mu_C\left(\frac{n}{A_{2D}}\right)^{a}\right]^{\frac{1}{a}}, \\ \mu_{SR}(T, F) = \frac{8.8\text{x}10^{14}}{F^2} e^{-\left(\frac{T}{850}\right)^2}, \\ \mu_N = cst\end{gathered} \tag{3.11}$$

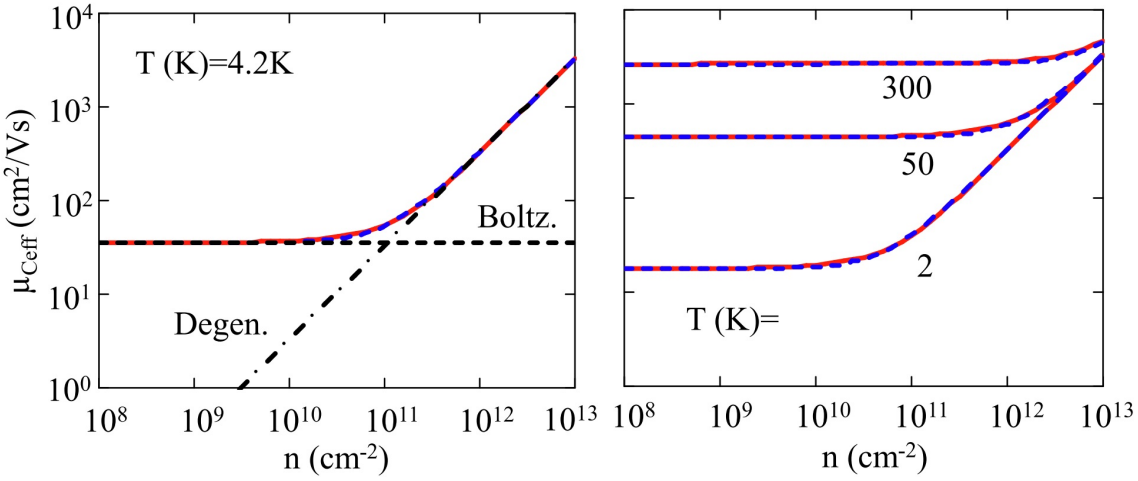
where μ_{ph} accounts for the mobility limited by phonon scattering, μ_C(E) accounts for the mobility limited by Coulomb scattering, with $\mu_{C,eff}$ being an "effective mobility" approximation, μ_{SR} accounts for the mobility limited by surface-roughness scattering, and μ_N accounts for the mobility limited by neutral-impurities scattering.

Indeed, the phonon-limited mobility has been retrieved from [140], with only a slight tuning of the highlighted factor to better fit our data. Recalling the general remarks made in 1.3.2, the phonon-limited mobility follows a behavior inversely proportional to the temperature, as there will be fewer phonons limiting mobility at lower temperatures.

On the other hand, following the initial argumentation of [141], Ghibaudo [58] formulated a simple compacted model for the Coulomb-limited mobility. It is important to notice that this mobility is proportional to carrier kinetic energy E and E_{Coul} is nothing but the kinetic energy at room temperature, i.e. 0.026 meV and therefore $\mu_C(E_{Coul})$ would be the value of the mobility at room temperature. Moreover, as the Coulomb mobility increases with the carrier kinetic energy, the screening effect gets masked: so we have chosen not to take it into account into this model. Furthermore, as we compute the Coulomb mobility through the Kubo-Greenwood integral and plot it vs the carrier number in Figure 3.29, we can see from 3.29a that it follows the Boltzmann statistics at high carrier densities and the degenerate statistics at low carrier densities. From Figure 3.29b we can see how for an increasing temperature, this transition point in between the two statistics progressively moves towards higher carrier densities. This finally allows to reformulate μ_C as $\mu_{C,eff}$, where the exponent a (highlighted) has been adjusted to better fit the transition in between the two statistics.

Following [142], μ_{SR} can be developed with an inverse proportionality to the effective electric field squared, where, in order to reach a better fit, we adjusted the numeric factors highlighted in equation (3.11).

Finally, we recall the independence of the neutral-impurities scattering of energy and temperature [143] and that therefore it can be expressed as a constant.



(a) *at 4.2 K* ***(b)*** *for all temperatures*

Figure 3.29: *Modeled Coulomb-limited effective mobility vs carrier number using the Kubo-Greenwood integral (solid red) and the $\mu_{C,eff}$ approximation (dashed blue) [144]*

$$\begin{gathered} \alpha(T) = 0.2\left(\frac{300}{T}\right)^{0.1} \\ F_0 = 7\text{x}10^4 \\ \text{a} \approx 1.5 \\ F(V_g, V_b) = \frac{\frac{Q_i(V_g,V_b,T)}{2} + C_b(V_s(V_g,V_b) - V_b)}{\epsilon_{Si}} \end{gathered} \tag{3.12}$$

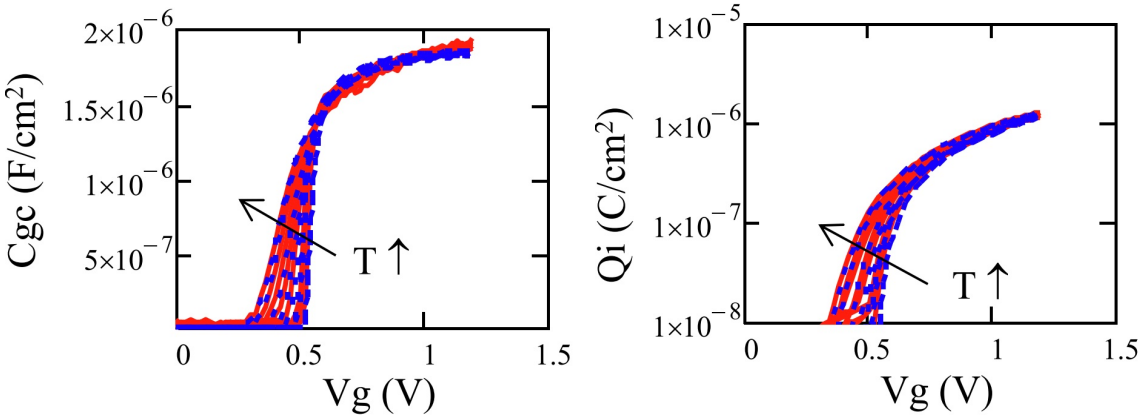
Equation (3.12) reports some complements to the main equation for scattering limited mobilities, where the parameters tuned within the present works are highlighted.

Before applying the Kubo-Greenwood method to the transfer characteristics of these devices, we indeed had to calibrate our equations on the $C_{gc}(V_g)$ and $Q_i(V_g)$ curves. As a matter of fact, this is a crucial step as a good part of the mobility equations at (3.11) are influenced through the effective field by the inversion charge. The inversion charge, as reported in (3.13), has been thus calibrated on the capacitance and charge curves of a W_g = L_g = 10 μm device, for a set of temperatures going form 300 K down to 4.2 K. As we can see from Figure 3.30 the fit resulting from calibration is actually quite satisfying and allows us to proceed to the $I_d(V_g)$ figure of merit.

Particularly, for this step the following model parameters were taken into account: C_{ox} = 2.1 μF/cm^2, C_{BOX} = 0.14 μF/cm^2, C_{Si} = 1.52 μF/cm^2, C_{it} = 0.16 μF/cm^2, V_0 = 0.5 V.

$$
\begin{aligned}
V_g = V_{fb} + V_s + \frac{Q_i}{C_{ox}} + \frac{C_{it}(V_s - V_0)}{C_{ox}} + \frac{C_b(V_s - V_b)}{C_{ox}}, \\
Q_i(E_f, T) = qn(E_f, T), \\
C_{it} = qN_{it}, \\
C_b = (C_{Si}C_{BOX})7(C_{Si} + C_{BOX})
\end{aligned}
\tag{3.13}
$$

where Q_i is the absolute inversion charge, V_s is the front surface potential, V_{fb} is the flat-band voltage, C_{it} is the front interface trap capacitance, and C_b is the substrate coupling capacitance.



(a) *Gate-to-channel capacitance* ***(b)*** *inversion charge*

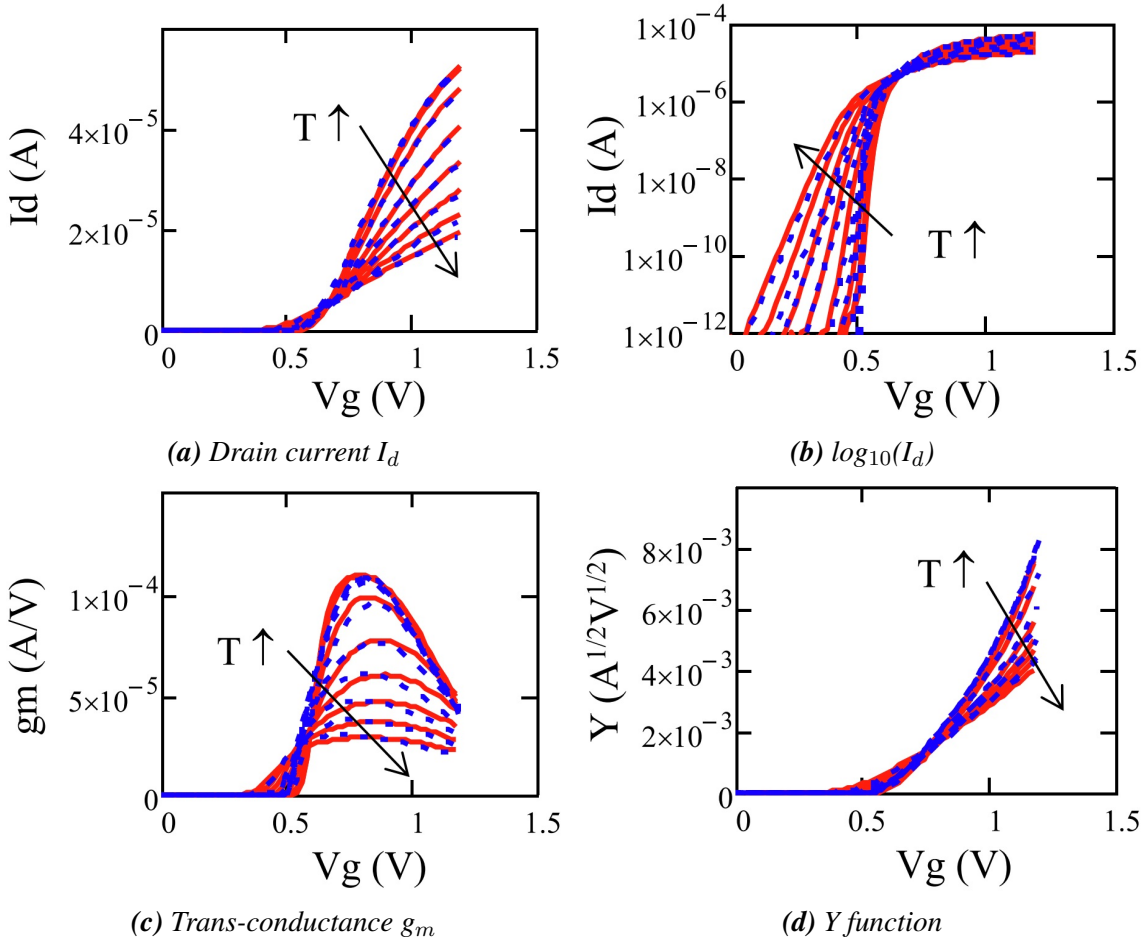
Figure 3.30: *Fitting on a experimental data (solid red) W_g = L_g = 10 μm down to 4.2 K with the model (dashed blue) [144]*

$$
\mu(E) = \left(\frac{1}{\mu_{ph}} + \frac{1}{\mu_N} + \frac{1}{\mu_C} + \frac{1}{\mu_{SR}} \right)^{-1} \tag{3.14}
$$

Using the equations above and combining the different scattering-limited mobilities through the Mathiessen rule as in equation (3.14), we can finally build a model of the trans-characteristics $I_d(V_g)$ for long-channel devices. Equation (3.15) provides the the final formula to reconstruct the current of the W_g = L_g = 10 μm. As we compared the model with experimental data in Figure 3.31, we can see in 3.31a that the model indeed matches almost perfectly the ON current down to the lowest temperatures. The modeling of the OFF current reveals to be quite reasonable across the full temperature range as seen in 3.31b. Same can be said for the trans-conductance in 3.31c and Y in 3.31d which are matched well-enough by the model at all temperatures.

$$
I_d(V_g, V_d, V_b, T, F) = \frac{W}{L}\sigma[E_f(V_g, V_b), T, F]V_d \tag{3.15}
$$

Particularly, at this point it interesting to see how the effective mobility obtained through the Kubo-Greenwood integral looks like, even before getting to the modeled $I_d(V_g$. For this goal, Figure 3.32 shows very well how the effective mobility gets modeled. Also, it is particularly interesting to notice how indeed for the coldest temperatures we can appreciate a bell-shaped behavior of μ_{eff}(n), as it is as well described in literature [49].

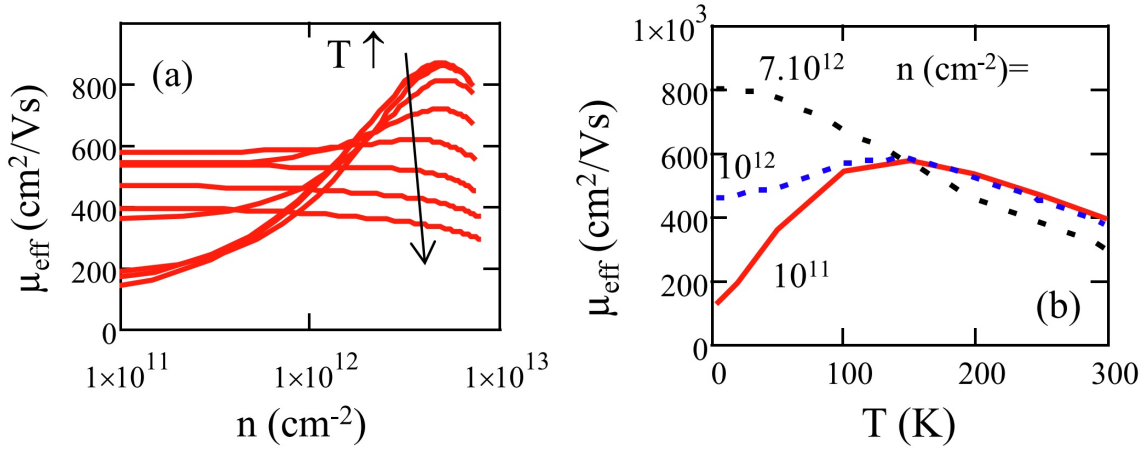


(a) Drain current I_d *(b) $log_{10}(I_d)$*

(c) Trans-conductance g_m *(d) Y function*

Figure 3.31: *Comparison of experimental (solid red) and modeled (dashed blue) curves for a $W_g = L_g = \mu m$ device down to 4.2 K [144]*

Moreover, it is of interest to highlight how, as we move to higher 2D carrier densities, the effective mobility increases moving to lower temperatures, rather than decreasing as it does for lower carrier densities.



(a) For various temperatures *(b) For different carrier densities*

Figure 3.32: *Modeled variations of the effective mobility for a $W_g = L_g = 10\ \mu m$ geometry, down to 4.2 K and for different 2D carrier densities [144]*

Figure 3.33 gives a good example of how the final modeled mobility takes into account all scattering process through the Mathiessen rule, as shown in equation (3.14). At high temperatures, due to the high vibrational energy, the effective mobility is limited by phonon scattering. On the other hand, at 4.2 K, the Coulomb scattering is the limiting mechanism for mobility in long-channel devices.

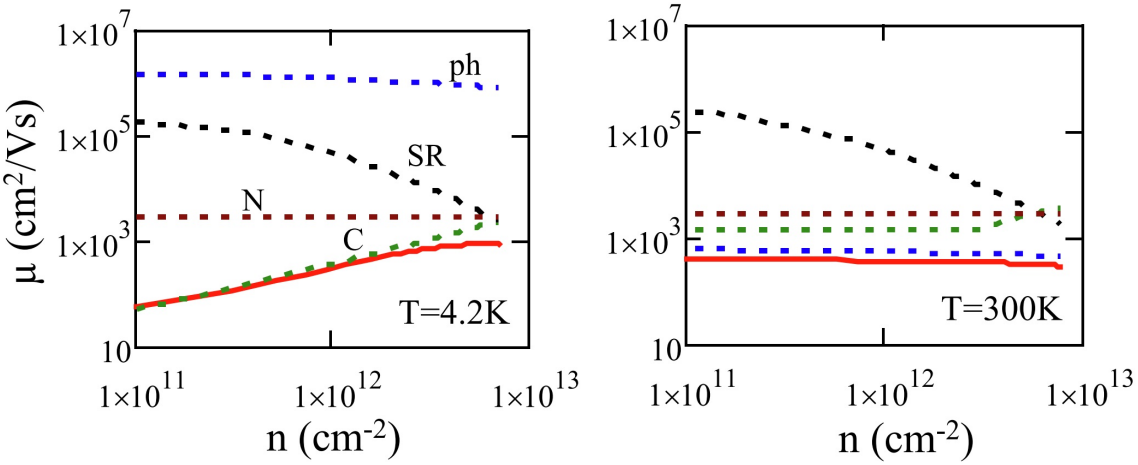


Figure 3.33: *Variations of different scattering-limited mobilities and the resulting effective mobility by Mathiessen rule (solid red), through modeling in a $W_g = L_g = 10$ geometry [144]*

To complete the study of long channel devices, Figure 3.34 reports a comparison in between the effective mobility resulting from the Kubo-Greenwood integral and the approximation for the coulomb scattering as in equation (3.11). At lower temperatures the two methods match almost perfectly, while at higher temperatures there is a difference from 10 to 20 %. In our opinion this is caused by an error due to the use of the Matthiessen rule outside of the Kubo-Greenwood integration.

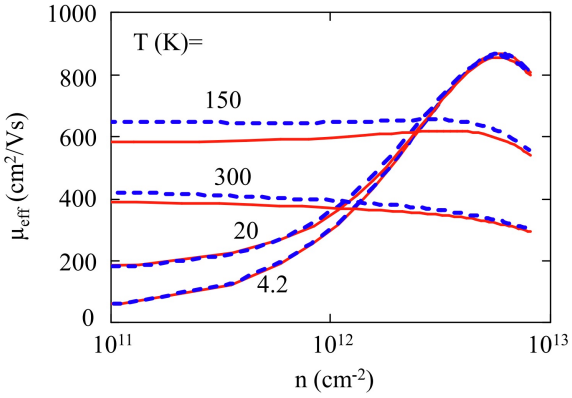


Figure 3.34: *Evolution of the effective mobility with respect to the 2D carrier density according to the Kubo-Greenwood modeling (solid red) and as coming from the Coulomb scattering effective mobility approximation as in 3.11 for various temperatures in the $W_g = L_g = 10$ geometry [144]*

Moving towards the analysis of smaller geometries, shorter-channel devices require a correction of equation (3.15) according to the effect of the Source-Drain resistance which

takes progressively more weight as the channel length decreases. Equation (3.15) finally integrates the effect of R_{SD} into the modeling of the drain current.

As we first employ this at 300 K, considering geometries with a common channel width of 1 μm and channel lengths going from 1 μm down to 30 nm. Figure 3.35 shows the model compared with respect to our experimental data at 300 K: indeed, the ON region is matched almost perfectly for what concerns drain current, trans-conductance, and Y function for all channel lengths. Still, the subthreshold slope is modeled with a quite close match with respect to experiments.

$$I_d(V_g, V_d, V_b, T, F) = \frac{\frac{W}{L}\sigma[E_f(V_g, V_b), T, F]V_d}{1 + R_{SD}\frac{W}{L}\sigma[E_f(V_g, V_b), T, F]} \tag{3.16}$$

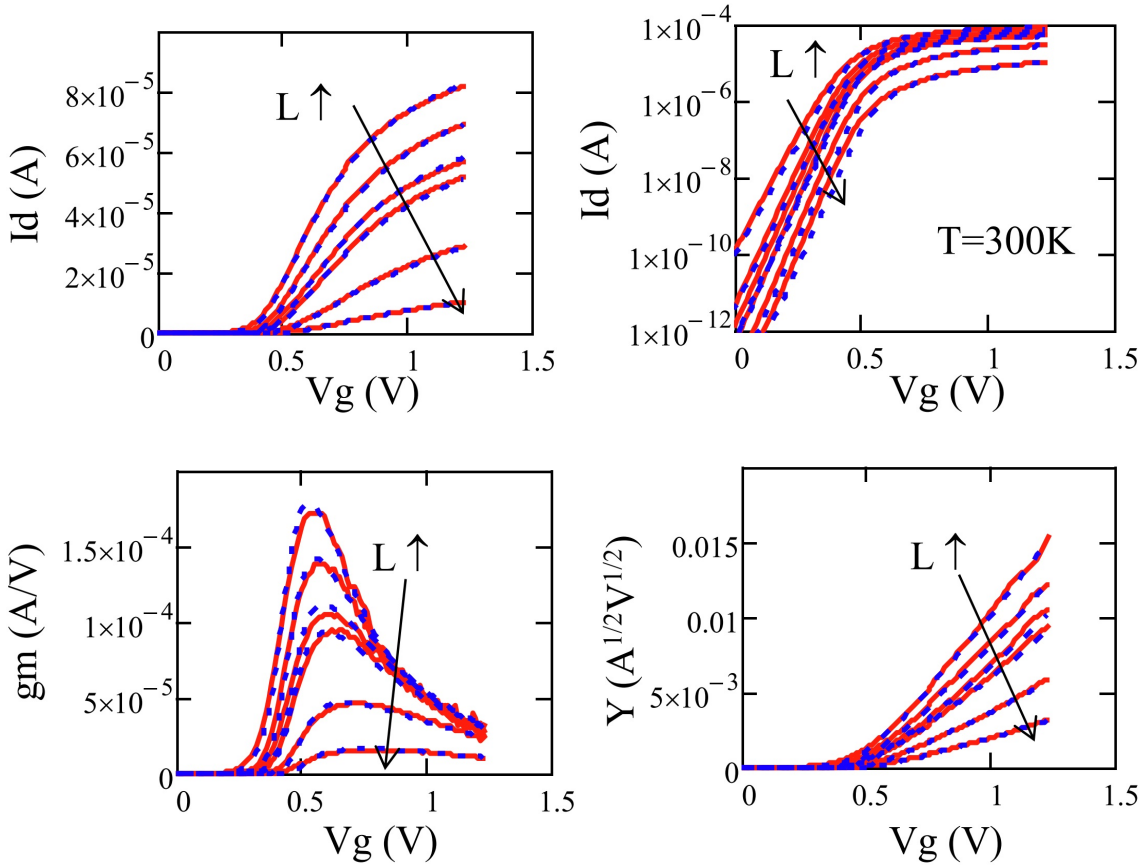


Figure 3.35: *Comparison at 300 K of the experimental (solid red) and modeled curves (dashed blue) for channel lengths of 30, 60, 90, 120, 300, 1000 nm and a channel width of 1 μm [144]*

As we move down to deep cryogenic temperatures, we can see from Figure 3.36 how the model still yields a quite reasonable prediction for the ON region. This prediction presents a good matching for all channel lengths at 77 K and even down to 25 K in both the drain current and the trans-conductance.

To complete the information that helped building this model, it is important to recall that inter-subband scattering impacts cryogenic temperatures only when the back channel is active at positive back biases [63]. Therefore, within this model this effect was not accounted for.

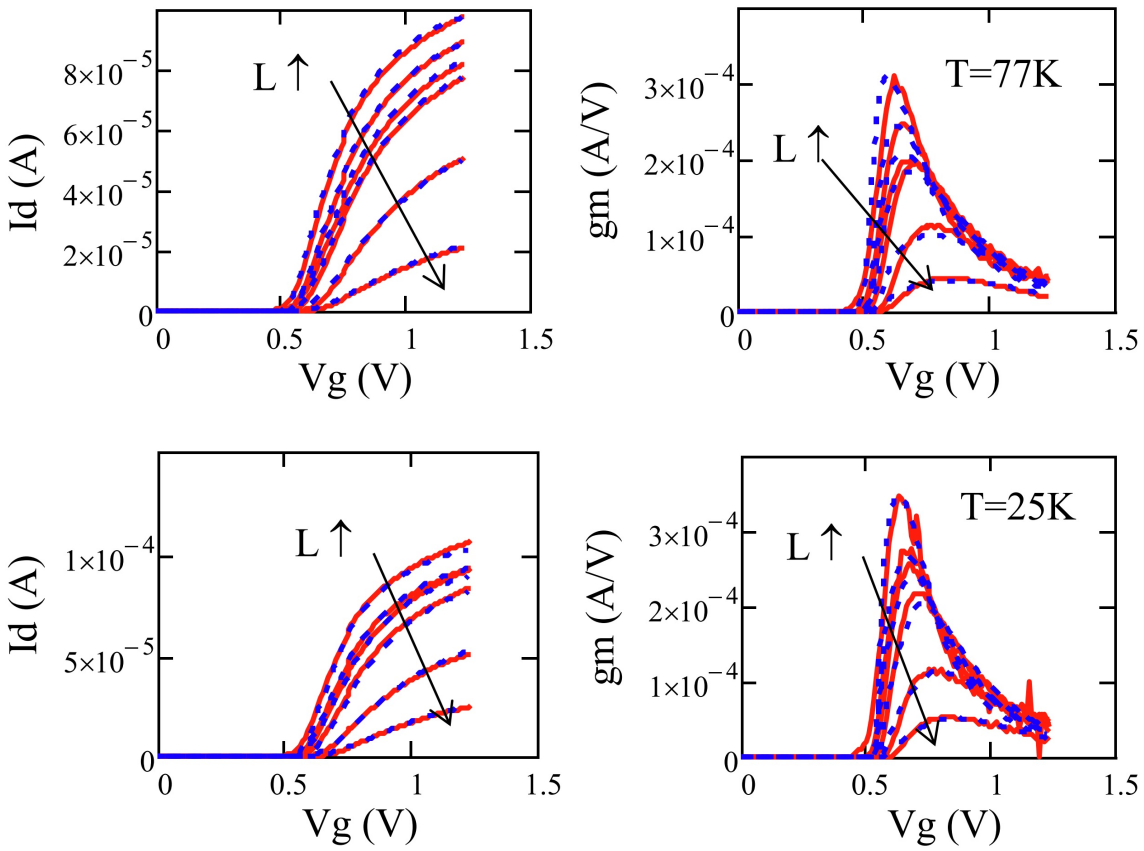
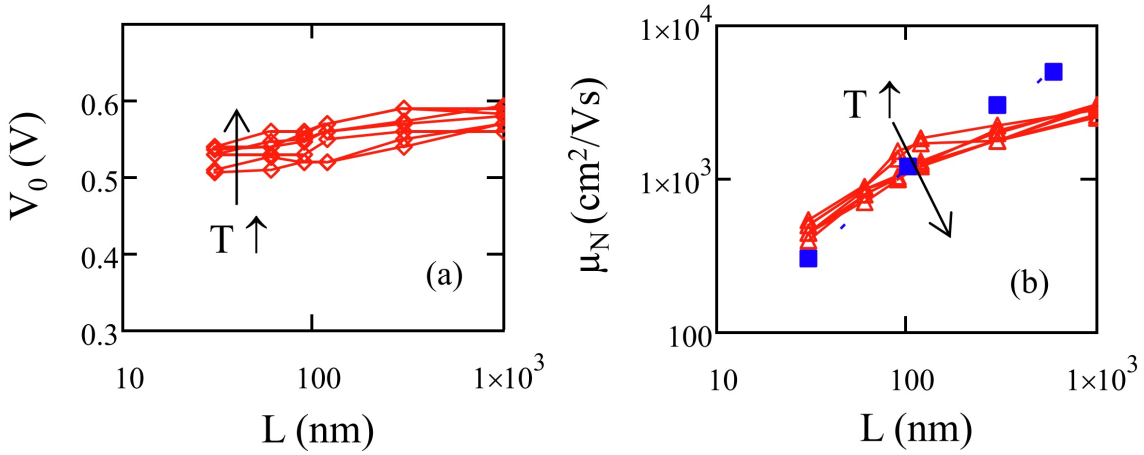


Figure 3.36: *Comparison at 77 and 25 K of the experimental (solid red) and modeled curves (dashed blue) for channel lengths of 30, 60, 90, 120, 300, 1000 nm and a channel width of 1 µm [144]*



(a) *Reference potential* ***(b)*** *Neutral scattering-limited mobility*

Figure 3.37: *Specially tuned parameters for short channel lengths [144]*

Moreover, while adjusting the model from the bigger geometry to the smaller ones, all mobility parameters were kept the same, except for the μ_N limited by neutral impurities and the reference potential V_0. These parameters were at each temperature point adjusted singularly for each channel length. Figure 3.37 shows the evolution of these tuned parameters with respect to the channel length for all temperatures. Particularly the

blue squares in figure 3.37b report the values form [50], which fall well in line with the ones we employed for the shortest geometries.

3.6 Conclusions

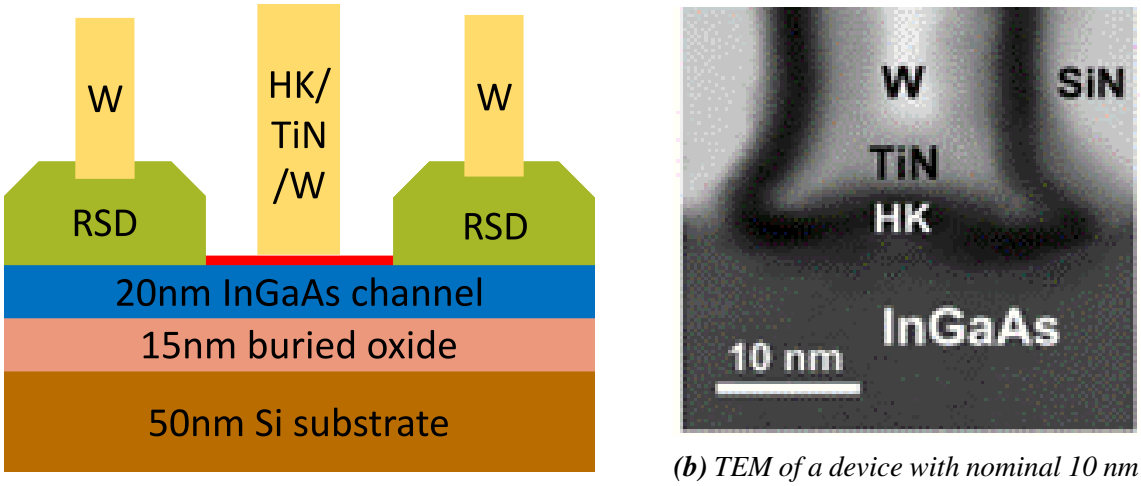
The first two sections have confirmed the behaviors we would have expected from the introduction chapter for both low-frequency noise and DC operation and short channel effects. Moreover, we could see how this class of devices confirms its highly industrial level, particularly given the performing values of the subthreshold swing. Also, we could find a confirmation of what modern studies describe as 'excess 1/f noise'. Given the quality and stability of these devices, we could further study them through two different modeling methods.

The applicability of the Lambert-W function-based MOSFET parameter extraction methodology on 28nm FDSOI MOSFETs has been demonstrated down to deep cryogenic temperatures, from long to short channel lengths. Thanks to the accurate Lambert-W function modeling of the inversion charge and drain current MOSFET characteristics from weak to strong inversion, the main parameters were extracted versus temperature and gate length, showing the temperature independence of short channel effects and the strong mobility degradation at short channel lengths due to increased defective scattering. It should also be mentioned that this Lambert-W function modeling of the drain current could easily be extended to nonlinear operation region as in [145], and, therefore, could next constitute a suitable MOSFET compact model to be used in circuit simulation at deep cryogenic conditions.

This chapter has also shown has shown how through the Kubo-Greenwood integral, it is possible to model the behavior of Silicon FDSOI MOSFETs down to deep cryogenic temperatures and for even small geometries of devices. Also, the good adherence if the model with the experimental data allows us to grasp detailed insights on the physics within this class of devices. The effective approximation of the effective mobility limited by Coulomb scattering could furthermore be employed in the future for compact modeling down to deep cryogenic temperatures.

4. *InGaAs MOSFETs*

As the research on quantum computers (QC) advances, the need for active electronic devices that operate at deep cryogenic conditions is increasing. This necessity is better understood when considering the qubit readout electronics [18]. In order to minimize signal transmission delays and noise amplification due to different temperatures amongst signal stages, readout electronics in QC have to be as close as possible to the qubits, therefore operating in the temperature range of a few units of Kelvins. Similar conditions hold true for the qubit control side. The cryogenic environment places stringent requirements on the supporting device technology, as the circuits must be dense and operate with extremely low power and noise at gigahertz frequencies. While it is currently an open question how many qubits cryogenic Si CMOS circuits will be able to support, other device technologies, such as III-Vs, may in the future be better suited. Thanks to their enhanced mobility, III-V MOS devices can provide the same ON current at lower power supply voltages, and by turn reduced power consumption and heat dissipation, crucial at QC operation temperature [146]. Thus, the precise identification of their electrical parameters' behavior with temperature and channel length is required for reliable modeling and circuit design. On the other hand, as this technology is not as mature as its Silicon-based counterparts (Bulk, FDSOI, and FinFETs), the need for full electrical characterization down to deep cryo-temperatures, becomes challenging and critical, particularly in view of the emerging technology of QC.



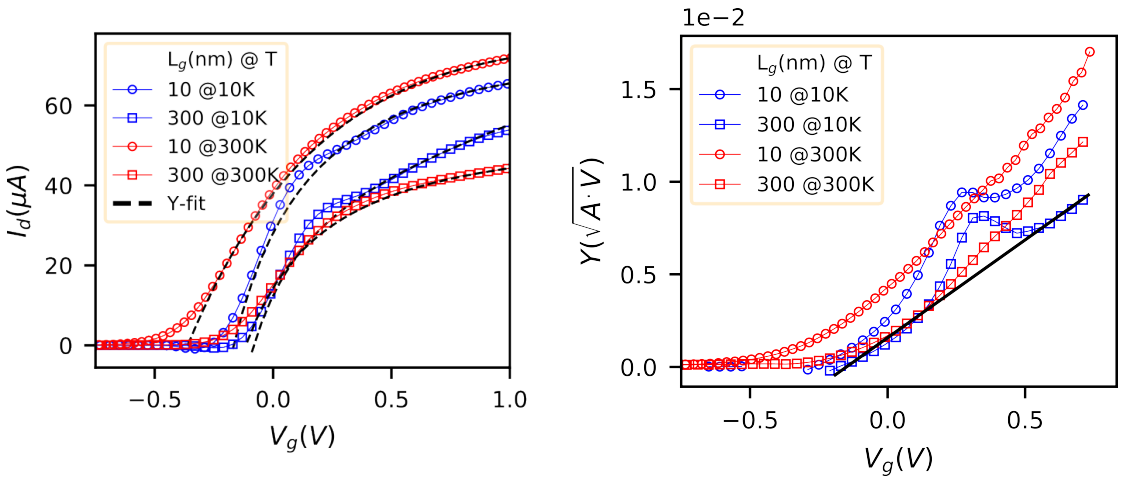
(a) *front schematics*

(b) *TEM of a device with nominal 10 nm gate length*

Figure 4.1: *Structure of the InGaAs-OI MOSFETs under study. Courtesy of IBM Zurich [146, 147]*

To date, Si CMOS has been extensively studied including at cryogenic temperatures [73, 117, 148, 129] and similar studies on InGaAs MOSFETs are currently lacking. The

devices treated in this chapter were fabricated by IBM Zurich [147], based on a III-V on insulator technology, incorporating a 20 nm InGaAs film, insulated by a buried oxide and integrated on Silicon substrates through direct wafer bonding, as shown in Figure 4.1. The fabrication process is CMOS-like with replacement metal gate, raised source/drain regrowth and a high-k metal gate. The devices share a common gate width value of W = 1 μm and channel lengths spanning from L = 300 down to 10 nm. Figure 4.1b also shows a TEM image of a L = 10 nm device. Note that this is the nominal value, the real L varies up to 14 nm. Henceforth, we will refer to the nominal value.



(a) *Drain current I_d* ***(b)*** *Y function*

Figure 4.2: *Measurements for a spanning gate voltage at V_d = 30 mV for L = 10 and 300 nm at T = 10 and 300K. The dashed lines represent the fitting of the plots, based on Y function and linear regression respectively [149]*

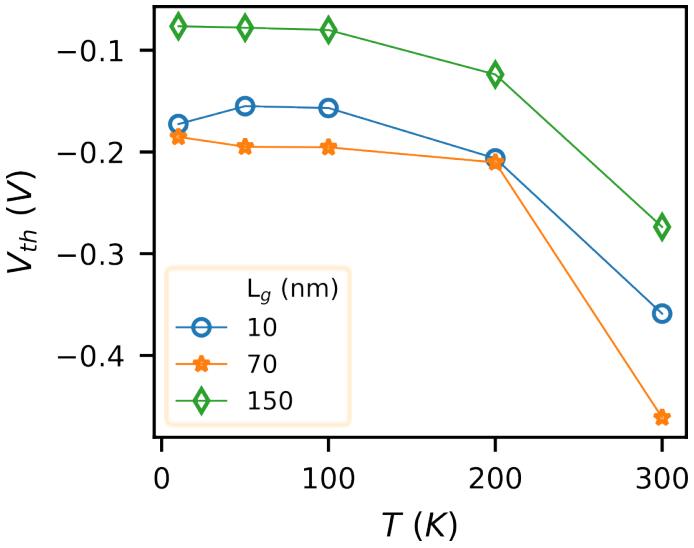


Figure 4.3: *Extracted threshold voltage versus temperature for V_d = 30 mV for various channel lengths [149]*

4.1 Cryogenic DC analysis

In this section, we study these scaled InGaAs MOSFET devices down to cryogenic temperatures, to determine their temperature- and size-dependent properties and compare them with Si CMOS. In particular, we compare the physical limits of the subthreshold swing at cryogenic temperatures. Finally, key cryogenic device properties are benchmarked against Si CMOS. The work provides valuable understanding of the cryogenic operation of III-V MOSFETs, and the results indicate that these devices are highly promising for cryogenic low-power quantum computer applications.

The measured $I_d(V_g)$ input characteristics in linear regime are plotted in Figure 4.2a, for the two temperature limits (10 K and 300 K). At first glance, we can already observe how the threshold voltage, V_t, is affected by both channel length and temperature: on one hand, for a shorter channel V_t shifts downwards ("V_t roll-off" short channel effect), while on the other hand, it increases for a decreasing temperature. Moreover, we can notice some kind of a shoulder/hump in the high V_g region, in both the $I_d(V_g)$ and the $Y(V_g)$ (Figure 4.2b) curves: this effect is most likely to be related to the onset of conduction in the L valley [150] of III-V. What is most important for this study, however, is that this hump does not impact the overall linear behavior of the Y function in strong inversion, allowing us therefore an easy and reliable extraction of the main intrinsic parameters.

As we go down to low temperatures (LT), we see several effects are taking place. First, recalling the evolution of the Boltzmann statistics with respect to temperature, we see an increase in threshold voltage as going towards lower temperatures. The extracted V_t values are plotted versus temperature for all measured gate lengths in Figure 4.3, increasing up to settling around 200 K due to the semiconductor transitioning to a degenerate statistics below that temperature [16].

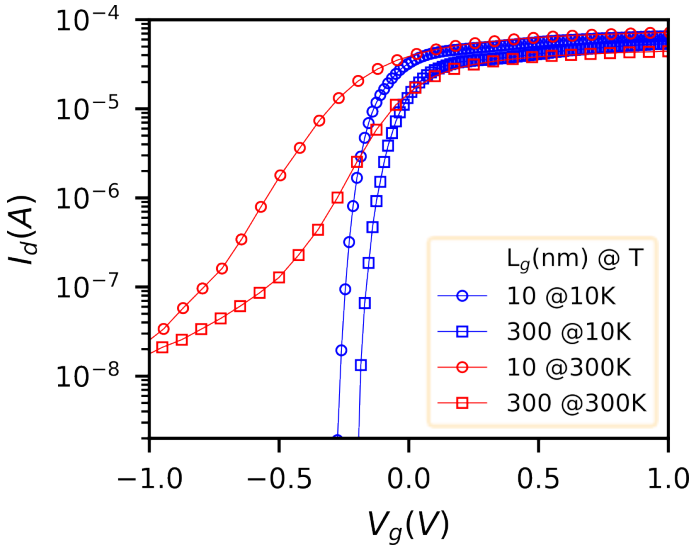


Figure 4.4: *Drain current versus gate voltage at V_d = 30 mV for L = 10 and 300 nm at T = 10 and 300K [149]*

Moreover, the transition between OFF and ON states becomes sharper as shown in Figure 4.4, yielding a consequent decrease of the subtreshold swing, SW, for low temperatures. This behavior of SW is finally reported in Figure 4.5, where the extracted values of SW are plotted versus temperature for certain channel lengths. Interestingly, as shown for Si MOSFETs in literature and in the chapter 3.6, also for these InGaAs MOSFETs, SW settles to values of approximately 10 mV/dec, which is attributed to the exponential band tails of states [73].

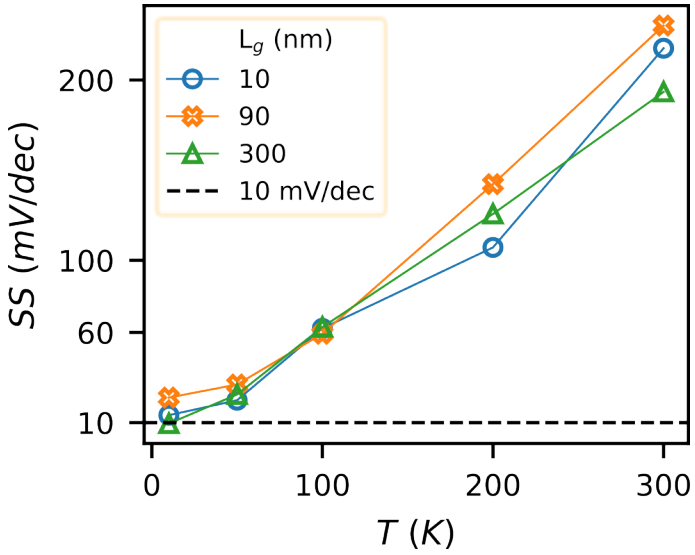


Figure 4.5: *Extracted subthreshold swing at V_d = 30 mV versus temperature for different lengths from 10 to 300 nm [149]*

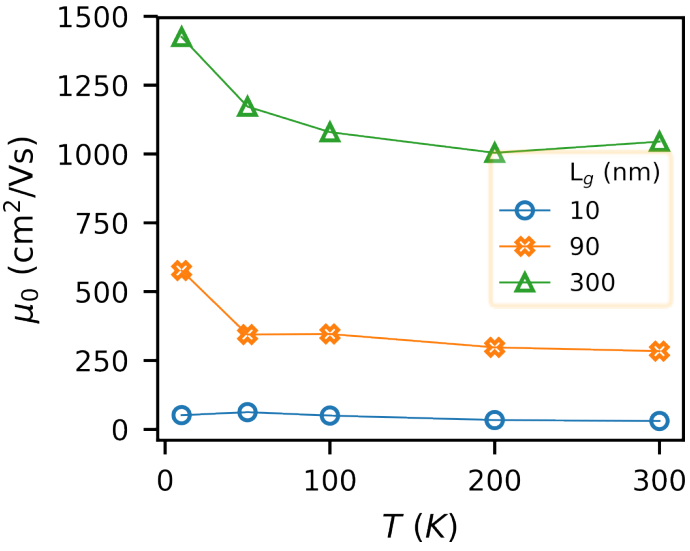


Figure 4.6: *Extracted low-field mobility at V_d = 30 mV versus temperature for different lengths from 10 to 300 nm [149]*

Conversely, the low temperature-induced decrease in phonon scattering allows an increase in the low-field mobility, μ_0, as shown in Figure 4.6, where the extracted values of μ_0 are plotted versus temperature for all measured gate channel lengths. This increase is evidently more pronounced in longer channel devices, whereas, in shorter channels, defect

(neutral impurity) scattering is prevailing due to source/drain regions proximity, yielding a generally lower mobility and also a less significant increase at lower temperatures [50].

In our case, only below 100K, the effect of L valley carrier population becomes visible as shown by [150] through Poisson-Schrodinger simulations, giving rise to specific structure in $I_d(V_g)$ and $Y(V_g)$characteristics as shown in Figure 4.2.

As we proceed towards the analysis of the device parameters in saturation region of operation (V_d = 1 V), we can observe the behaviour of both 10 and 300 nm length devices plotted in Figure 4.7. Neither of them shows significant variation in the ON region as going to low temperatures, except for an increased V_t for L_g = 10 nm at 10K. From the consequent extraction, the variation of the low-field mobility with respect to temperature in the saturation region is very small.

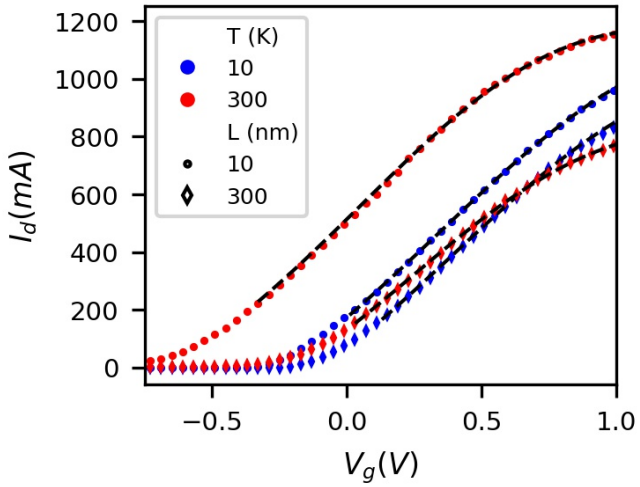


Figure 4.7: *. Drain current versus gate voltage at Vd = 1 V for L = 10 and 300 nm at T = 10 and 300K. the dashed line shows the fit reconstructed with the parameters extracted thanks to the Y function [149]*

On the contrary, we notice that in saturation region, the curvature created by the takeover of L valley is no longer visible at low temperature. This can be explained when considering that the drain current is obtained by integrating the inversion charge along the channel from source to drain [151]: close to the drain region the influence of high V_d does not allow the quasi Fermi level to fill the L valley, thus attenuating its effect.

When extracting the μ_0 values through Y function, plotted in Figure 4.8, compared to the linear region, the devices present a μ_0 reduction due to velocity saturation (v_{sat}) effect [117]. Moreover, it is worth noticing how the extracted mobility never reaches the ballistic limit [148], revealing that the exponential behavior of μ_0 with respect to channel length is in fact scattering-related. The extracted values of v_{sat} in saturation region are plotted in Figure 4.9, showing a good stability with respect to temperature and a slight increase for a decreasing channel length due to overshoot effect.

Figure 4.10 illustrates the extracted parameters of μ_0, SW and v_{sat} along with respective extractions done for Si channel Fully Depleted (FD) SOI MOSFETs [129]. When comparing the III-V MOSFET devices to this more mature, industrial-like FDSOI technology, we note that although SW is much higher for III-V at 300K, both technologies reach the lowest limit value at 10K. Moreover, despite the higher interface trap density at the Al_2O_3/InGaAs interface, III-V shows higher μ_0 and v_{sat} at all temperatures, revealing

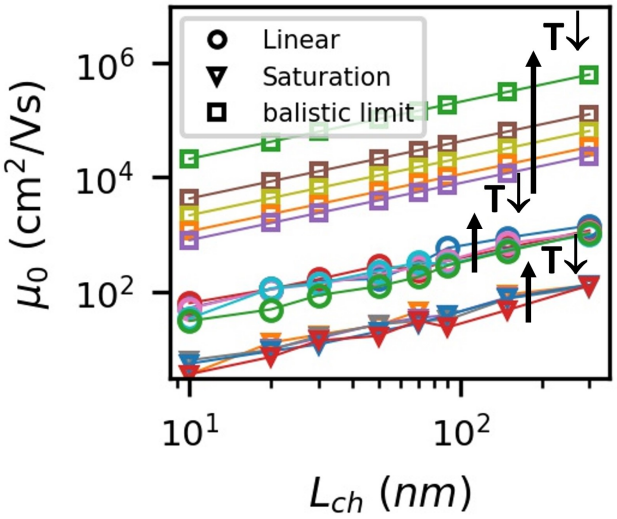


Figure 4.8: *Extracted low-field mobility versus channel length for linear and saturation regions along with theoretical ballistic limit [149]*

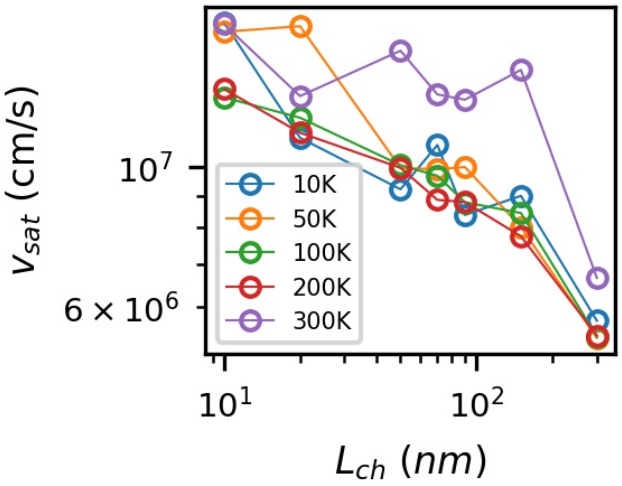


Figure 4.9: *Extracted saturation velocity versus channel length for various temperatures [149]*

a great III-V potential for cryo-related applications with further technology developments and the prospect to outperform Si FDSOI in certain cases.

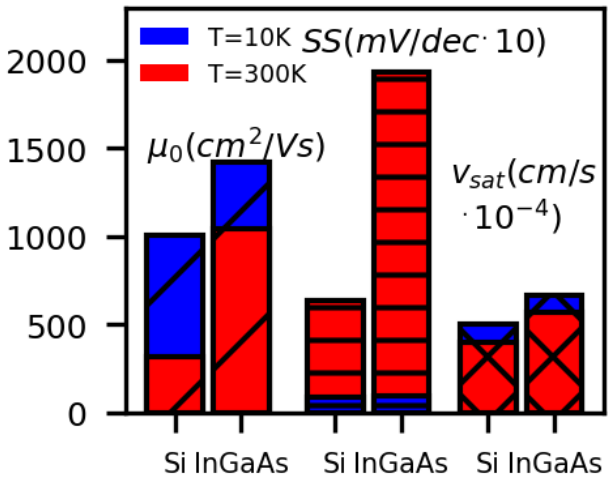
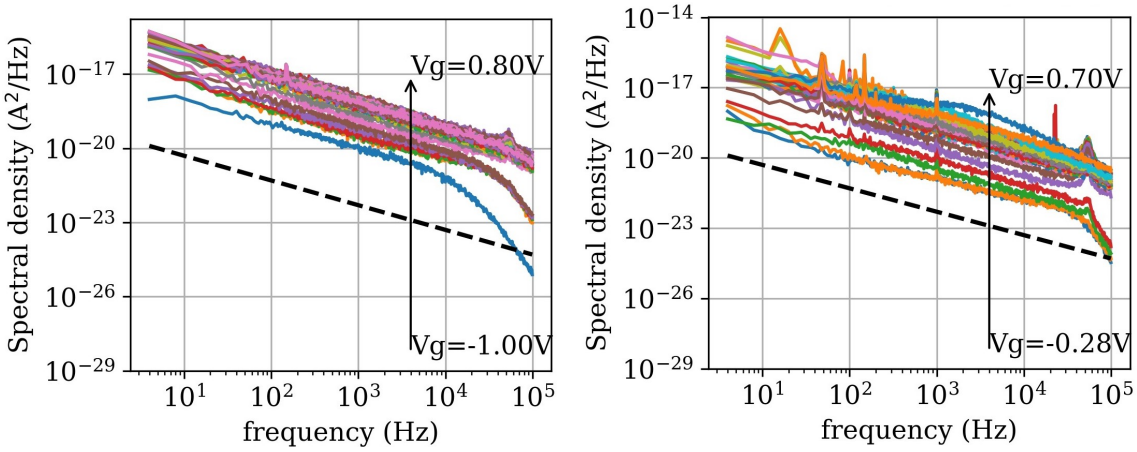


Figure 4.10: *Comparison of extracted parameters between III-V and Si [129] for a common channel length of 300 nm [149]*

4.2 Low-frequency noise

For this class of InGaAs MOSFETs, the low-frequency noise analysis has been performed down to deep cryogenic temperatures, namely 10 K. Figure 4.11 shows the raw PSD measured both at 300 and 10 K on a device with both a gate width, W_g, and a Gate length, L_g, of 1 μm. Both Figures 4.11a and 4.11b show that, independently from temperature, these devices are showing higher levels of noise with respect to the FDSOI devices studied in the previous chapter. This can, through an educated guess, be primarily attributed to the aluminum-oxide used as Gate dielectric. As already explained, the natural affinity of SiO_2 with Si allows for FDSOI to grow a dielectric much cleaner from defects/traps. Yet, the present technological level in the fabrication of the Al_2O_3 dielectric and its affinity to the InGaAs crystal could be the cause for the higher raw PDS.



(a) *T = 300 K* ***(b)*** *T = 10 K*

Figure 4.11: *Power spectral density of a device with W_g = 5 μm and L_g = 500 nm*

As the PSD displayed at all temperature a 1/f behavior, as shown in Figure 4.11 for

300 and 10 K, we tried to analyze them with a CNF + CMF model. Figure 4.12 reports the PSD normalized with respect to the square of the Drain current at both 300 and 10 K; also, the fittings according to the Carrier Number Fluctuation coupled with Correlated Mobility Fluctuations are reported as dotted lines. Only the dots (each corresponding to a measurement point) that are solid were taken into account for the CNF + CMF fitting: these were the only ones extracted from a raw PDS displaying a clear enough 1/f behavior at the corresponding Gate bias.

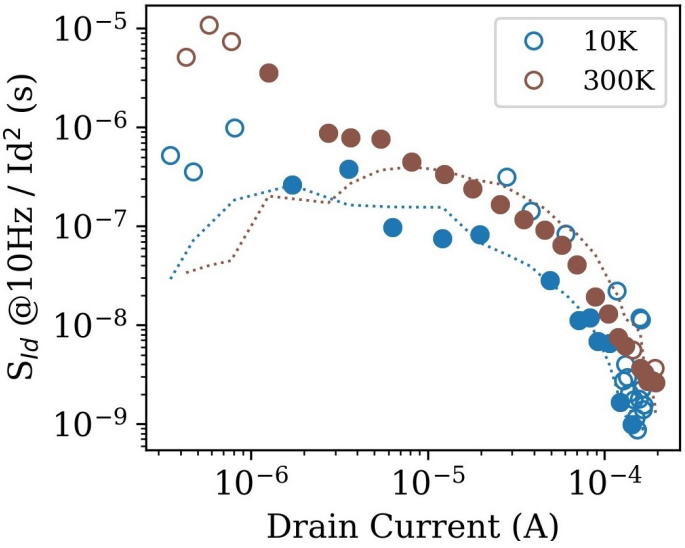


Figure 4.12: *Normalized PSD at 10 and 300 K with respective fittings*

Figure 4.13 shows the extracted power spectral density of the flat-band voltage normalized with respect to the area of the Gate. It is quite interesting and unexpected to see how variable the $S_{V_{fb}}$ is with respect to temperature and how it drops with a decreasing temperature and reaches a minimum value below 100 K, at the same region where the threshold voltage is saturated. Yet, we so far do not have an explanation for this and it will require further investigation.

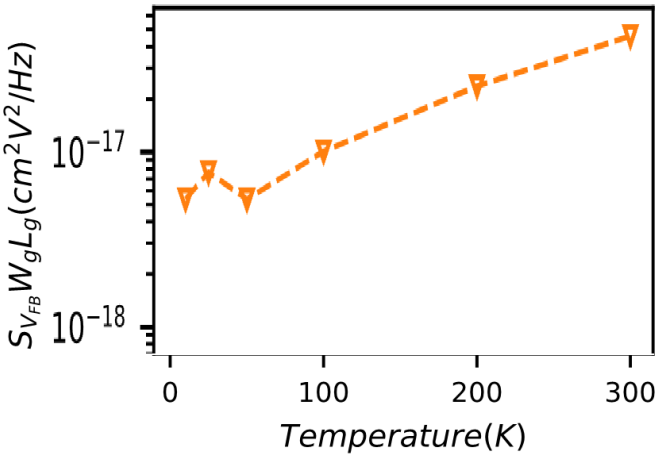


Figure 4.13: *Normalized PSD of flat-band voltage with respect to $W_g L_g$*

4.3 L valley

The results of DC characterization from the previous section, coupled with our simulation results, indicate the clear presence of L valley conduction. The interest is to clearly assess the behavior related to L valley conduction on top of Γ valley and to show how the effect becomes more and more evident as the operation temperature progressively decreases, an effect that is also validated through numerical calculations. Moreover, the importance of this section is enhanced by the simplicity of the devices under study, which, being free from any quantum well or 2DEG structure, manage to show already at the level of transfer characteristics the presence of L valley.

In III-V-based devices, the presence and effect of L valley are well known across the field of semiconductor device physics: O'Regan et al. have extensively simulated [150] how the gate-to-channel capacitance is influenced by the conduction in the satellite valleys. To briefly summarize, due to the small energy difference (interband offset) between the levels of the minima of the central Γ valley and of the satellite L valley, as shown in Figure 4.14, the Γ one gets quickly filled with carriers as the gate voltage increases, thus starting the population of the L valley [152]. This phenomenon results in two main effects: an increase of the oxide capacitance, as shown in [150], and a decrease of mobility. Firstly there is a thinning of the dark space [82] region in between the inversion channel and the interface with the oxide, as the inversion carriers generated in L valley are gathered closer to the interface with respect to the ones generated in the Γ valley: this results in a step in the channel capacitance $C_{gc}(V_g)$ curve [82]. Secondly, we have to consider that the two valleys present different effective electron masses: therefore, as carriers from L are effectively heavier, the conductivity (and thus the drain current) will increase less suddenly with the gate voltage which pushes forward the occupancy of the L valley, compared to lower voltages.

Actually, the experimental demonstration of L valley conduction is far from trivial and, to the best of our knowledge, it has not yet been clearly shown, particularly when it comes to static I-V behavior of planar InGaAs-on-insulator MOSFETs'. We believe that there might in fact be uncommented experimental behaviors in the literature, such as the capacitance curve for a multi-stack MOSFET-like structure in Fig.19 from [153], which could possibly be attributed to the L valley. Furthermore, Sumita et al. assessed how L valley conduction influences static properties of InAs down to 50K [154].

In this section, we present results from the electrical characterization of InGaAs-on-insulator MOSFETs'devices and the specific behaviors that brought us to the inquiry on the physical explanation behind them. Finally, we reproduce the same behaviors through numerical calculations, validating our hypothesis on the L valley conduction.

4.3.1 Experimental results and discussion

Given the small area of these transistors, C-V measurements were not possible, for the measured oxide capacitance is below the precision of the instrument (∼10 fF). Thus, our initial study was limited to the analysis of the transfer characteristics, therefore the drain current as a function of the gate voltage $I_d(V_g)$. Figure 4.15a shows the $I_d(V_g)$ curves obtained from room temperature down to 10 K in linear region (V_d = 30 mV). If on one hand the devices function as expected at room temperature, on the other hand we can observe a progressive appearance of a shoulder slightly above the threshold voltage V_t, while moving to lower temperatures. Taking a look at Figure 4.15b, we can see how

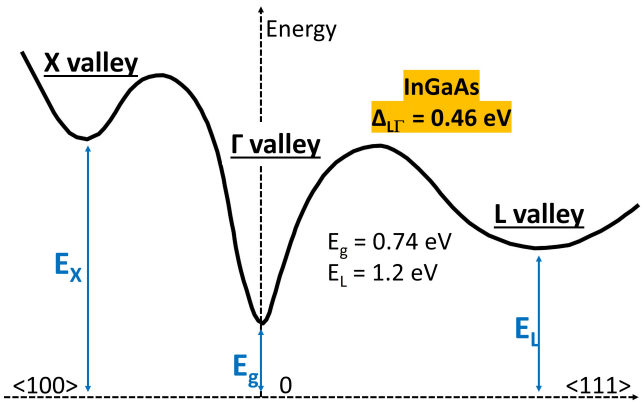
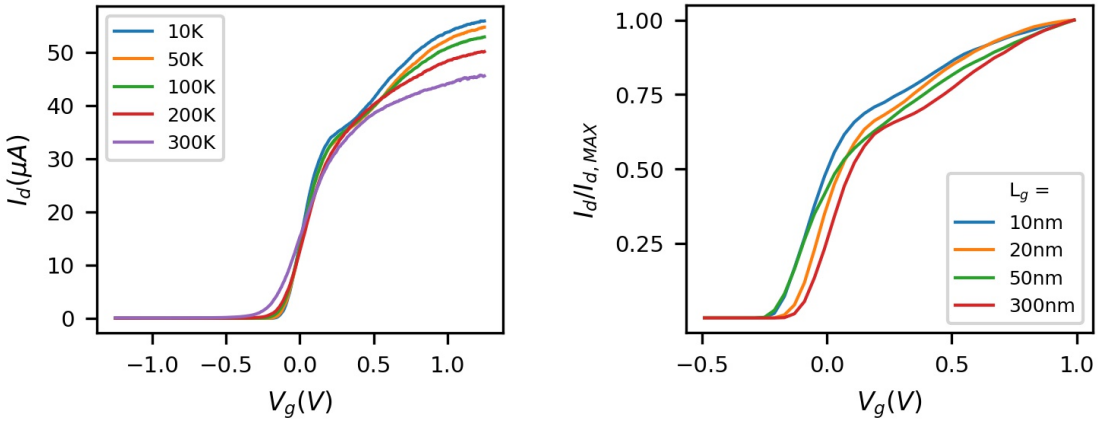


Figure 4.14: *Band structure of InGaAs [56]*

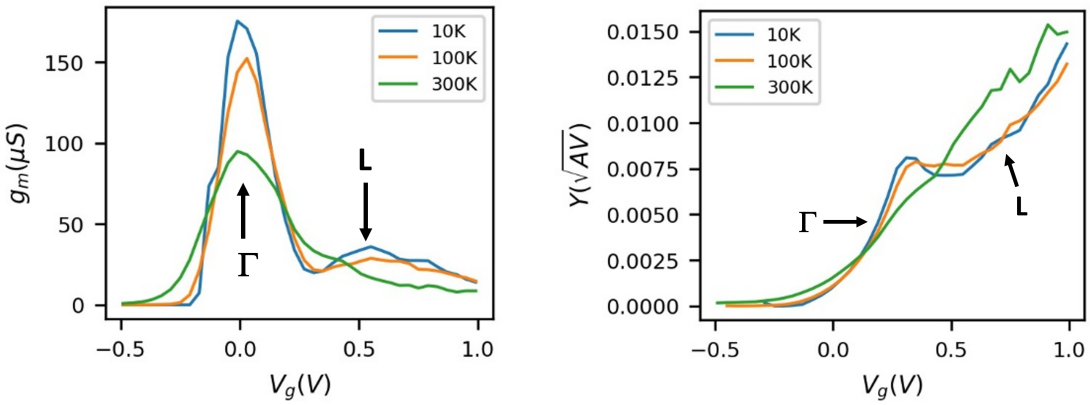
this shoulder, particularly visible at 10 K, is appearing across different lengths at deep cryogenic temperatures, making this effect non-specific to a single device.



(a) *L_g of 300 nm* ***(b)*** *T = 10 K*

Figure 4.15: *Transfer characteristics in linear region of operation (V_d = 30 mV)*

Interestingly, this behavior was also reflected as a hump, as shown in Figure 4.16, in the trans-conductance $g_m = dI_d/dV_g$ and the Y-function, $Y = \frac{I_d}{\sqrt{g_m}} = \sqrt{\frac{W}{L} C_{ox} \mu_0 V_d} (V_g - V_t)$ [112], which was used for characterization purposes to extract the threshold voltage and low-field mobility. The trans-conductance in MOSFETs reaches a peak directly proportional to the low-field mobility, μ_0, i.e. the maximum channel mobility value before any decrease related to intrinsic (scattering) or extrinsic (series resistance) degradation mechanisms. Yet here the presence of two peaks could in fact be attributed to two different μ_0 values appearing at different gate voltage bias, given they would belong to processes starting at two different values of V_g for the two valleys respectively. Particularly, the Y-function, being mathematically independent from any 1^{st} order degradation effects such as the access resistance, provides more clarity to directly observe the low-field mobility through its slope, $\sqrt{\frac{W}{L} C_{ox} \mu_0 V_d}$. It is indeed the Y-function that by displaying two different slopes before and after the peak, reveals the presence of two different low-field mobility values, that can be linked to the two different effective DOS masses belonging to different valleys of the conduction band.



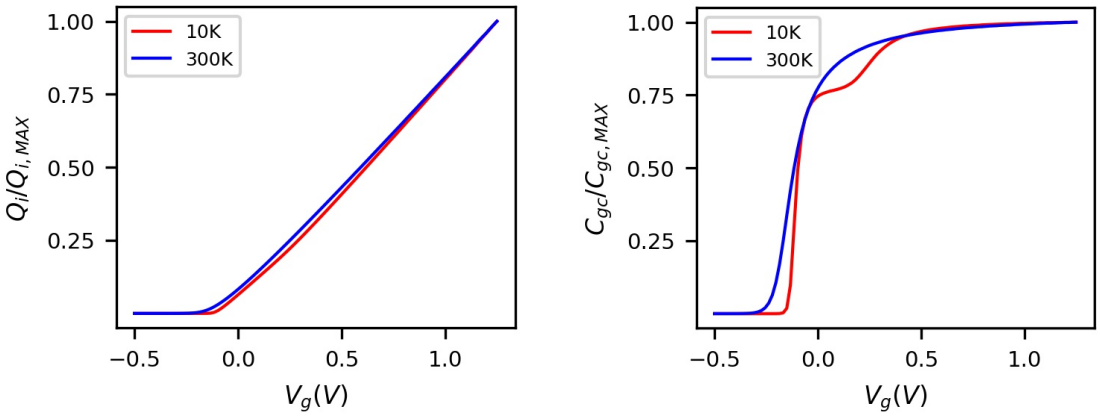
(a) *(b)*

Figure 4.16: *Trans-conductance (a) and Y function (b) for a device with L_g = 300 nm*

While experimentally we can see clearly this behavior only below 100 K, conversely [150] shows the knee in a gate-to-channel capacitance $C_{gc}(V_g)$ curve already at room temperature. However, this can be explained, as the inversion charge concentration Q_i, and consequently the drain current I_d, are measured and seen through an energy-integration over a span which is a function of k_BT, which at room temperature is too wide (compared to low T) to allow a clear distinction between the two valleys and their related mobilities.

4.3.2 Numerical calculations

To further verify our assumption, we built up a numerical calculation based on the Poisson-Shroedinger equations and the FlexPDE solver, coupled with the Airy approach [155, 156], taking into account the different conduction valleys of the crystal and multiple sub-bands for each valley. In Figure 4.17a we show the resulting inversion charge Q_i: as one can see, while we have a single-sloped linear Q_i at room temperature, at 10 K we see a slight bending, presumably showing the transition in between two slopes.



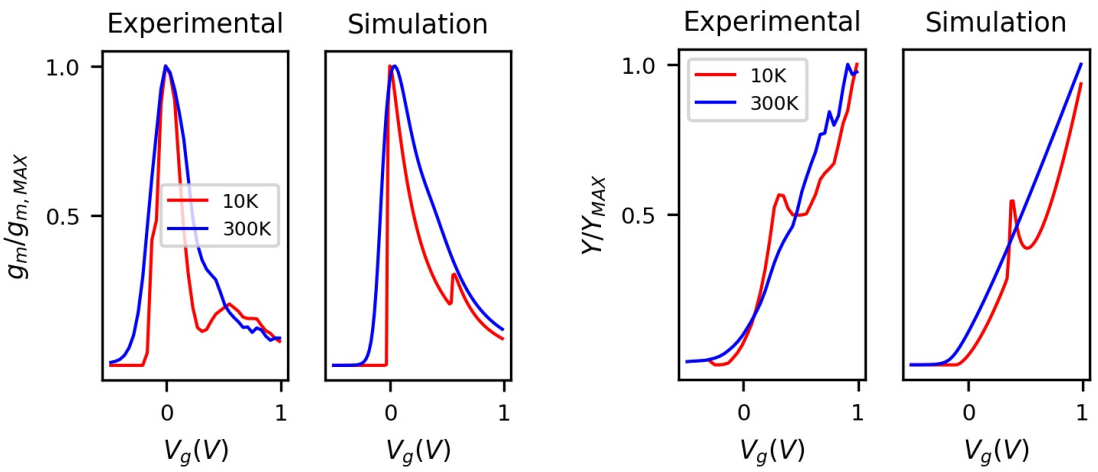
(a) *Inversion charge* ***(b)*** *Gate-to-channel capacitance*

Figure 4.17: *Normalized simulation results at 10 and 300 K for an InGaAs MOSFET, aconting for multi valley conduction*

From this calculated inversion charge, we can at first rebuild the gate-to-channel capacitance, C_{gc}, (Figure 4.17b) by integrating Q_i across the V_g range, which resembles the C_{gc} behavior shown in literature [150] at very low temperatures (T = 10 K), confirming the visibility of the L-valley conduction only at cryogenic temperatures (at least concerning the devices under study). We furthermore find important to underline that we adjusted the inter-band offset in order to get a behavior similar to the experimental results: it is possible that a different choice of this parameter in the simulation between this work and [150] can better explain the difference in between the two simulation results at 300 K.

Finally, from Q_i we can also rebuild the related g_m and Y function as shown in Figure 4.18: this finally confirms the two g_m peaks and Y function hump that we saw in our experimental curves. It is furthermore important to notice that in order to obtain more reliable results and interpretation, the mobility in the simulation was expressed through a power law as in [50], taking care of the transition to deep cryogenic temperatures, with n = 2 at room temperatures and n = 3 at 10K:

$$\mu = \frac{\mu_0[\theta(V_g - V_t)]^{n-2}}{1 + [\theta(V_g - V_t)]^{n-1}} \tag{4.1}$$



(a) *Trans-conductance* ***(b)*** *Y function*

Figure 4.18: *Comparison of normalized experimental and simulated results at 10 and 300 K*

4.4 Conclusions

Concluding, this section has reported a detailed electrical characterization of scaled planar InGaAs-on-Silicon MOSFETs from room temperature down to deep cryogenic temperatures (10K). The main MOSFET parameters (threshold voltage V_t, low-field mobility μ_0, and subthreshold swing, SS) were extracted in linear region of operation using the consolidated Y-function method for gate lengths down to 10 nm, despite the possible presence of L-valley conduction, and were bench-marked to Si CMOS. The results build on the understanding of the operation of cryogenic III-V MOSFETs and indicate that this technology may be promising for future low-power cryogenic quantum computer applications. The saturation velocity was also extracted and analyzed for all lengths and

temperatures. The extracted parameters of the III-V devices follow the expected behavior with temperature as in Si, while demonstrating competing advantages as compared to Si MOSFETs, particularly when going down to cryogenic temperatures.

Also, low-frequency noise has been investigated down to 10 K. Particularly, the devices, not only have displayed a 1/f trend in their PSD, but they also abed the CNF + CMF model

We have demonstrated the effect of carrier conduction in the L valley by both electrical measurements of InGaAs-on-insulator MOSFETs and numerical calculations. The way simulations and experimental results demonstrate similar behaviors, along with the fact that we only observe this effect at low temperatures, is for us a validating proof that the knee in the $I_d(V_g)$ and hump in $g_m(V_g)$ and $Y(V_g)$ can only be explained through conduction in the L valley. This rises an important concern when pushing the gate voltage too high in these devices when used in LNAs, given the risk of switching to a lower mobility, and therefore lower trans-conductance and in turn less amplifier gain. We estimate that opening this topic within the experimental frame at deep cryogenic temperature will surely boost further results, possibly confirming this kind of behavior in other classes of devices that might also present conduction in the L valley.

5. *InGaAs HEMTs*

III-V-based high electron-mobility transistors (HEMTs) are proving to be great candidates for cryogenic LNA and are already used today [157]; though, in order to enhance their performance for future scaled QCs, their characteristics have to be thoroughly investigated down to deep cryogenic temperatures.

High electron mobility is one of the major drivers for the research on III-V materials. In theory, any device based on III-V (therefore InGaAs as well) should present such advantage. Yet, as it has been shown in the previous chapter, this has not been the case. One of the reasons for which the InGaAs MOSFETs studied in the previous chapter did not display the expected high mobility is the quality of the interface. Thus, it has been found that a good and effective way to preserve the high mobility of such materials is to have conducting electrons 'sandwiched' in a two-dimensional electron gas (2DEG). Indeed, by confining the material of the channel within an heterostructure stack, we can decrease the amount of scattering and preserve the mobility intrinsic to the material

The devices under study were fabricated by IBM Research - Zurich and consist of an $In_{0.65}Ga_{0.35}As$ channel, stacked in-between two layers of InAlAs, as shown in Figure 5.1. The InAlAs serves at the bottom as a buffer connecting to a semi-insulating InP substrate, and at the top as a spacer separating the channel from the delta-doping plane, and a third layer of InAlAs, to reduce possible gate leakages, as they are shown in the schematics reported in Figure 5.1.

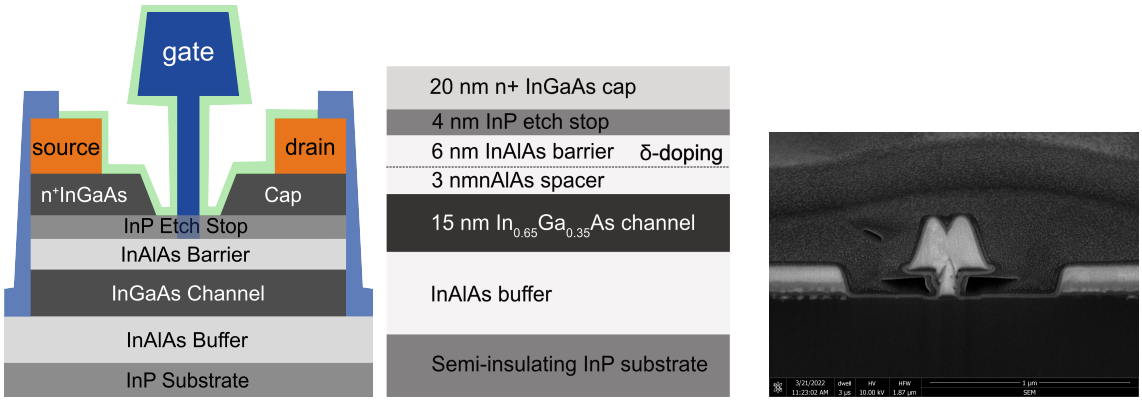


Figure 5.1: *HEMT structure under test: schematics (left), layer dimensions (center), TEM of the T-gate structure (right)*

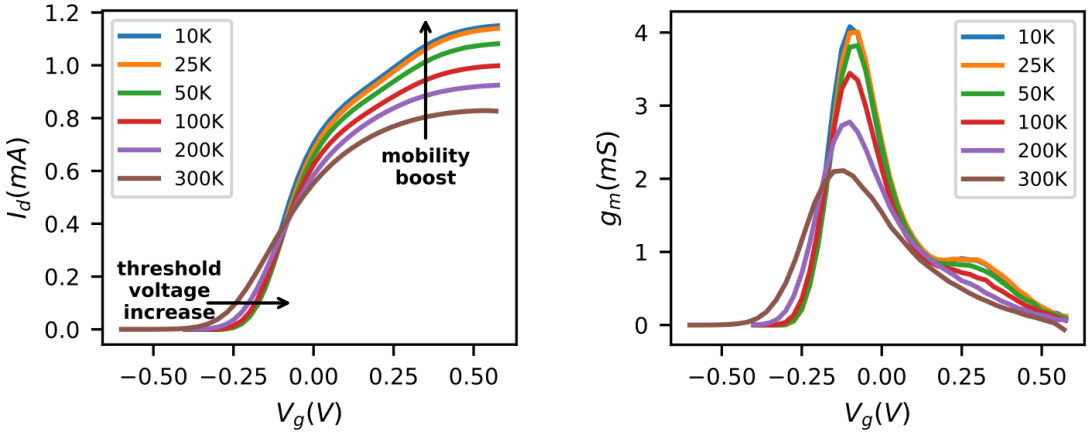
5.1 Cryogenic DC analysis

The present section investigates the behavior of this class of devices down to 10 K. Particularly, it will extract the main three parameters that have been already analyzed for the previous two technologies as well, i.e. subthreshold swing, low-field mobility, and threshold voltage.

For the DC investigation, the geometries adopted share a common Gate width, W_g, of 10 μm, while the investigated channel length, L_g, spans from 130 down to 70 nm. The Source-Drain region lengths, L_{SD}, was taken with a constant value of 1.4 μm for the measurements where different channel lengths were studied. On the other hand, in order to better understand the effects of the access resistance on this technology, we measure variable L_{SD} from 0.8 up to 2.0 μm for three devices, that were sharing same channel length of 100 nm and same width of 10 μm.

5.1.1 Initial observations

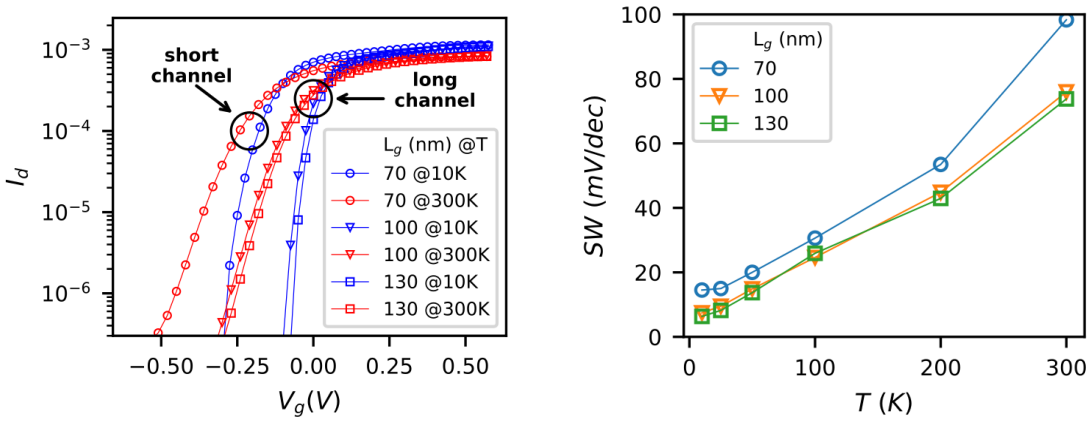
From the transfer characteristics shown in Figure 5.2a, which are corrected [158] with regards to current leakage at high gate voltage, V_g, at a first glance we see how as the temperature decreases, both the threshold voltage, V_t, and the mobility increase. Moreover, a shoulder in the curve can be observed above V_g = 0.1 V for low temperatures, which we attribute to the onset of the population of the L valley [150, 149] addressed in detail in a following section. This effect becomes even more evident when plotting the trans-conductance, g_m=dI_d/dV_g. Apart from showing the expected evolution of g_m with respect to the temperature, Figure 5.2b also reveals a second peak of the trans-conductance: indeed, besides the first peak boost going towards 10K, a clear second peak appears in strong inversion, presumably corresponding to the L valley conduction.



(a) *Transfer characteristics* ***(b)*** *Trans-conductance*

Figure 5.2: *Device with W_g = 10μm and L_g = 70 nm (V_d = 30 mV) at various T*

Concerning the subthreshold slope, Figure 5.3a clearly shows that it consistently increases as temperature decreases, whereas we see both a degradation of the slope and a roll-off of Vt due to short channel effect (SCE) [25] for the shortest channel regardless of T.



(a) Transfer characteristics for different channel lengths at T = 10 and 300 K

(b) Extracted values of subthreshold swing versus T for various gate lengths

Figure 5.3

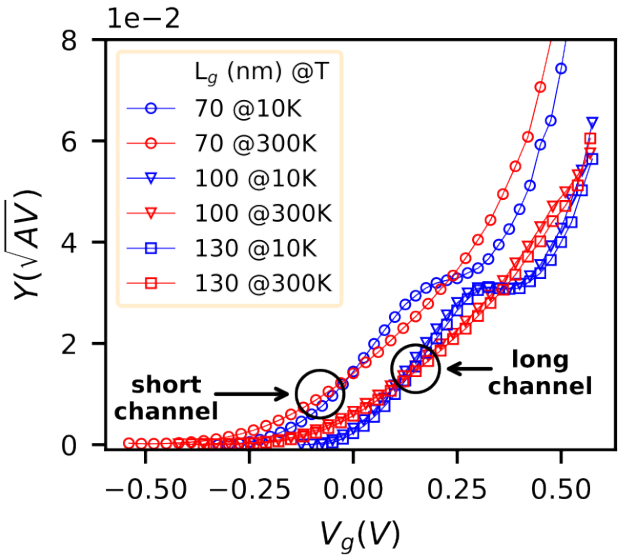


Figure 5.4: *Y-function versus gate voltage for different channel lengths at T = 10 and 300 K*

5.1.2 Extraction of DC parameters

As can be seen from Figure 5.3b, the extracted subthreshold swing (SW) at room temperature is much lower with respect to the values measured in InGaAs-channel MOSFETs [149], highlighting the improvement achieved by the eliminating the traps of the interface with the aluminum-oxide. In addition, we note that as T decreases below 25K for the longer channels, SW reaches values close to 6mV/dec. This value is significantly lower than 10 mV/dec, which is the reported lower limit for both Si [121] and InGaAs MOSFETs [149], attributed to disorder-induced band tails [73].

We claim that the high quality of the 2DEG/buffer interface helps overcoming this SW limit and achieving lower operating voltages, as i can be also seen for a similar technology studied by Ferraris et al. [159]. Yet, we see that the device with L_g = 70 nm not only

presents higher values with respect to the two longer channels due to SCE, but it would also seem to present a settling of the SW at low temperature. Due to the short size of the channel compared to both the access regions and the depth of the channel with respect to the gate contact, the Gate manufacturing process might have induced defects into the channel.

Extraction of low-field mobility, μ_0, and threshold voltage, V_t, has been performed using the series resistance-immune Y-function (5.1) [160], after a corrective iteration to account for the mobility attenuation factor θ_2 [113].

$$\begin{aligned} Y &= I_d/\sqrt{g_m}, \\ Y' &= Y\sqrt{1-\theta_2(V_g-V_t)^2} \end{aligned} \tag{5.1}$$

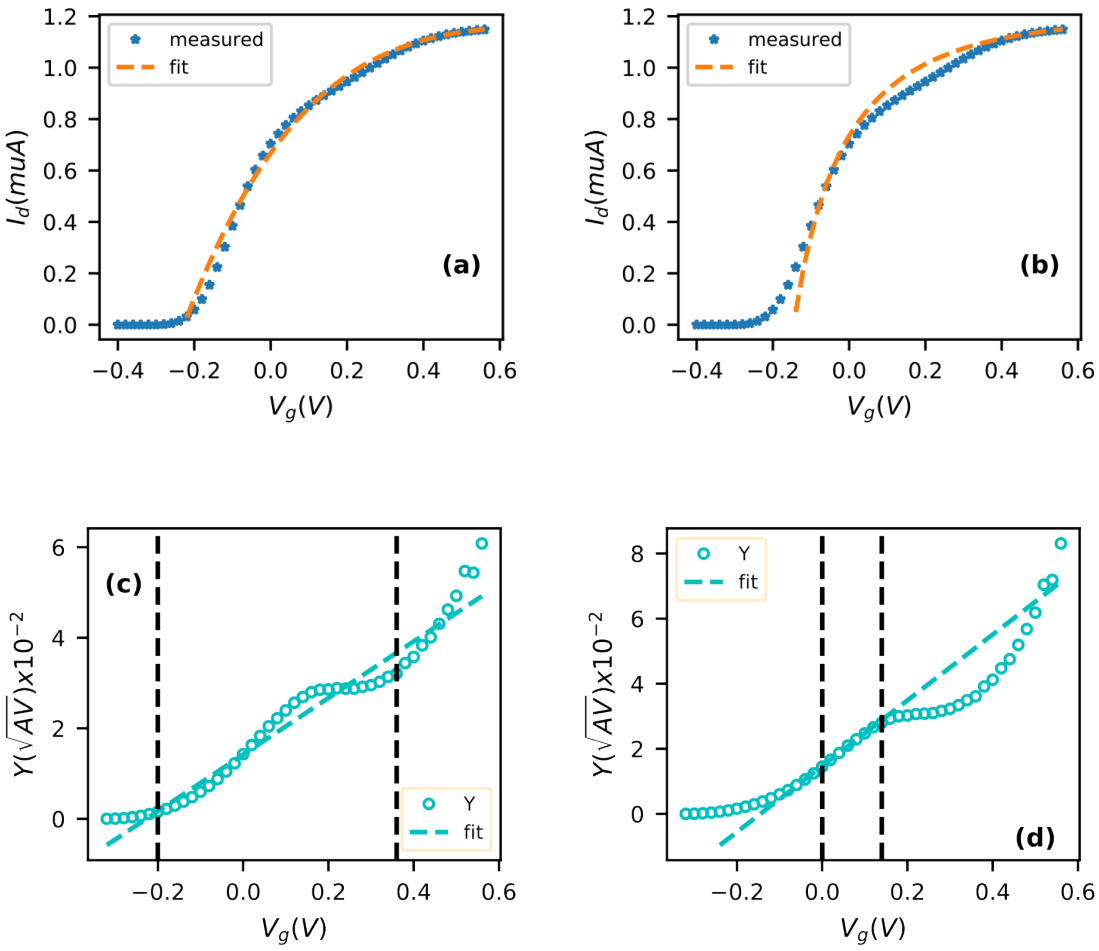


Figure 5.5: *Y-function linear fit over a broad V_g span (c) and a narrow one (d) and respective $I_d(V_g)$ (a and b) reconstruction through (5.2)*

As shown in Figure 5.4, the linearity of $Y(V_g)$ is affected at low temperatures (LT) by the onset of the L valley, confirming results in III-V MOSFETs [149].

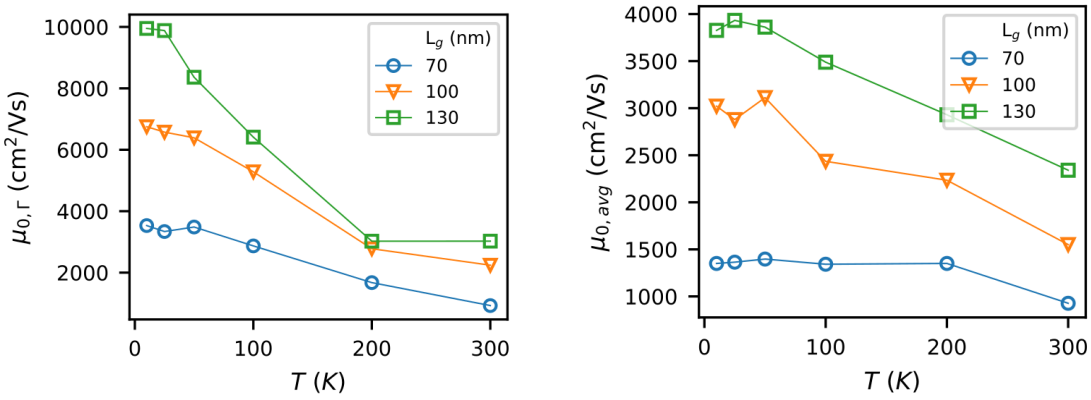
We nonetheless verified that taking into account an average slope of Y (Figure 5.5c) within a range of V_g representing strong inversion, yet before eventual leakages, we can extract the combination of average $\mu_{0,avg}$ and V_t that best fit the original transfer characteristics (Figure 5.5a) using equation (5.2).

$$I_d = \frac{WC_{ox}V_d(V_g - V_t)}{L} \frac{\mu_{0,avg}}{1 + \theta_1(V_g - V_t) + \theta_2(V_g - V_t)^2} \tag{5.2}$$

It is important to remark that, in order to perform this averaged reconstruction in between the influence regions of the two valleys, the attenuation factors used in equation (5.2) deviate from their original physical meaning and are in this case, more to be regarded as fitting parameters to help calibrate the extracted V_t and $\mu_{0,avg}$ within a model that can overall fit and describe the cryogenic behavior of these devices.

Following a different approach, Figure 5.5d shows that if the linear fit of $Y(V_g)$ is done only on its strictly linear part, which is the V_g range corresponding to Γ valley conduction, it allows the isolated extraction of the Γ valley mobility, $\mu_{0,\Gamma}$ (Figure 5.6a), which is far higher than results from [149, 121]: the 2DEG proves to preserve the high value of III-V mobility. Moreover, when looking at both $\mu_{0,\Gamma}$ and $\mu_{0,avg}$ (Figure 5.6b), we see how phonon scattering reduction at lower T causes an increase of mobility. Furthermore, μ_0 is consistently lower as the gate channel shortens likely due to stronger effect of neutral impurity scattering, as it was also shown in GaN HEMTs due to the etching processes of the Gate [93].

An additional indication of L valley conduction is found when comparing $\mu_{0,\Gamma}$ and $\mu_{0,avg}$: as L conduction is much more affected by phonon scattering due to higher effective mass, the average mobility drops to lower values. This is also evident by the lower value of the second peak of g_m at low T, as shown in Figure 5.2b.



(a) *From the linear fit of Y in the Γ interval (Figure 5.5d)*

(b) *From the linear fit of Y over a V_g span with both Γ and L valleys(Figure 5.5c)*

Figure 5.6: *Extracted low-field mobility versus T for different gate lengths*

Finally, Figure 5.7 shows that the extracted V_t value increases as T lowers from 300 K down to 100 K, following the Boltzmann statistics, yet it saturates at very low temperatures due to the onset of degenerate behavior [16]. Also, it is easy to confirm the SCE, as all the L_g = 70 nm values are significantly lower.

5.1.3 Impact of access region length

Even if the extracted attenuation factors, θ_1 and θ_2, did not maintain their strictly physical meaning through this extraction, θ_1 can still give an idea of the weight of the access resistance on the transport in the channel. Therefore, as we have done for FDSOI

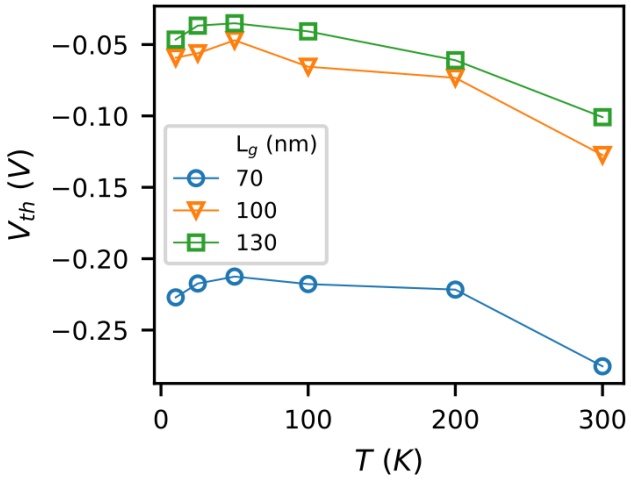


Figure 5.7: *Extracted threshold voltage with Y-function versus T for different gate lengths*

in [121], we plotted the extracted values of the first-order attenuation factor with respect to the peak of the trans-conductance, G_m, computed as the square of the slope of Y. Figure 5.8 indeed reports these values for all channel lengths and temperatures and moreover, the applied linear regression.

$$\theta_1 = \theta_{1,0} + \frac{WC_{ox}\mu_{0,avg}}{L} R_{SD} \tag{5.3}$$

The R_{SD} was extracted through equation (5.3) around 380 Ω regardless of T and L_{SD}, indicating that it is dominated by the Source-Drain access resistance.

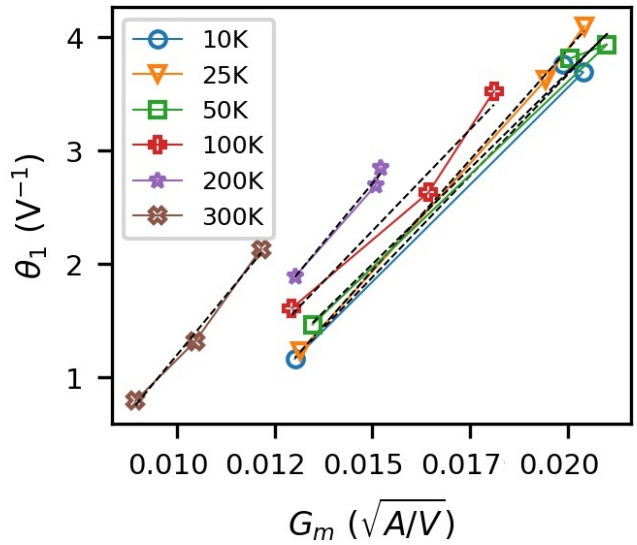
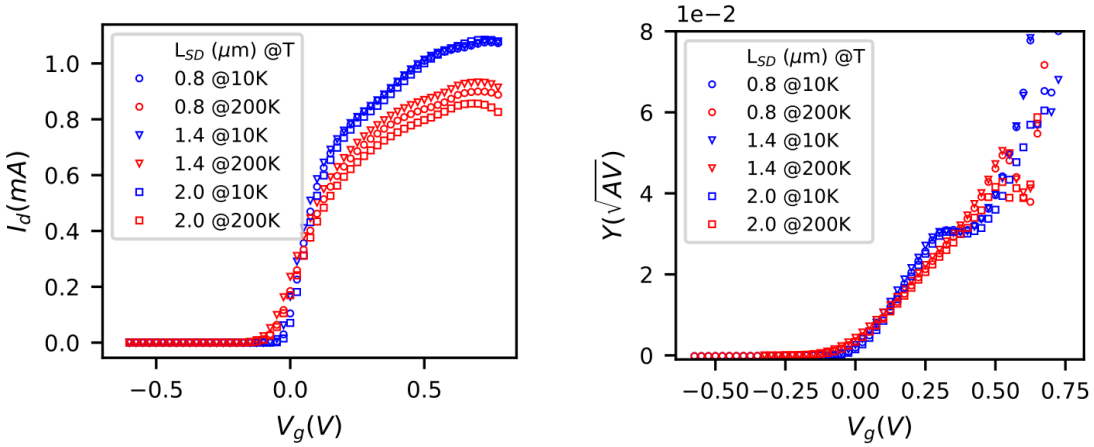


Figure 5.8: *Plot and linear regression of θ_1 with respect to the square of the slope of Y*

From Figure 5.9a, we can observe how various distances in between the source and drain regions, L_{SD}, influence differently the current degradation at high V_g. This difference is much stronger at higher temperature, while becoming almost negligible at 10K.

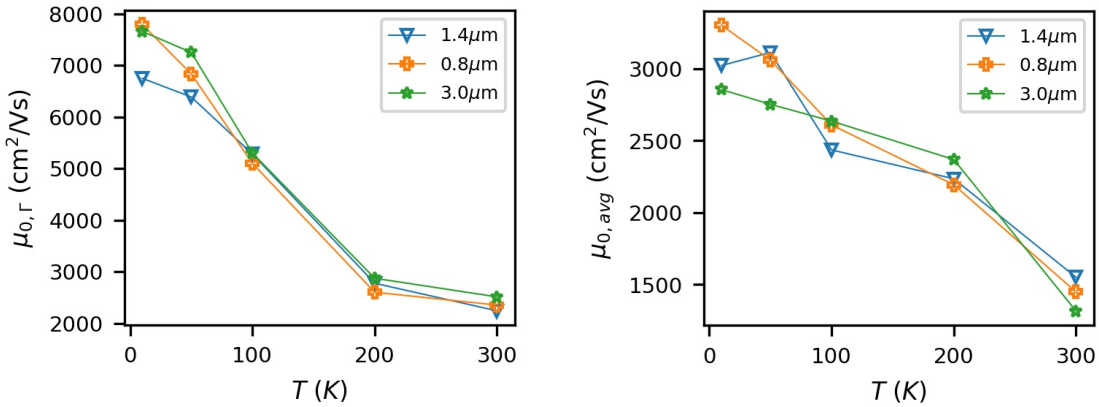
We can also clearly see that, as expected, thanks to the suppression of SD series resistance, R_{sd}, the corresponding Y-function (Figure 5.9b) is not affected by L_{SD}: in fact, the curves merge at each temperature, as W_g and L_g are identical for all three devices.



(a) *Transfer characteristics* ***(b)*** *Y function*

Figure 5.9: *Device with W_g = 10 μm, L_g = 100 nm and different Source-Drain distances at 10 and 200 K (V_d = 30 mV)*

Figure 5.10 reports the extracted values of the mobility for varying Source-Drain distances. If on one hand this analysis is not giving further insights on the effect of the access region, on the other hand, it shows at first impact how the values are consistent for each temperature point: not only this confirms the power of Y discriminate everything that is external to the channel, but it also shows a good degree of stability for this technology. Moreover, as we compare Figures 5.10a and 5.10b, we see a further confirmation of the effect of L valley. Indeed the mobility $\mu_{0,avg}$ extracted over a V_g span shared by both Γ and L valley is consistently much lower than the one only related to the carriers coming from the Γ valley.



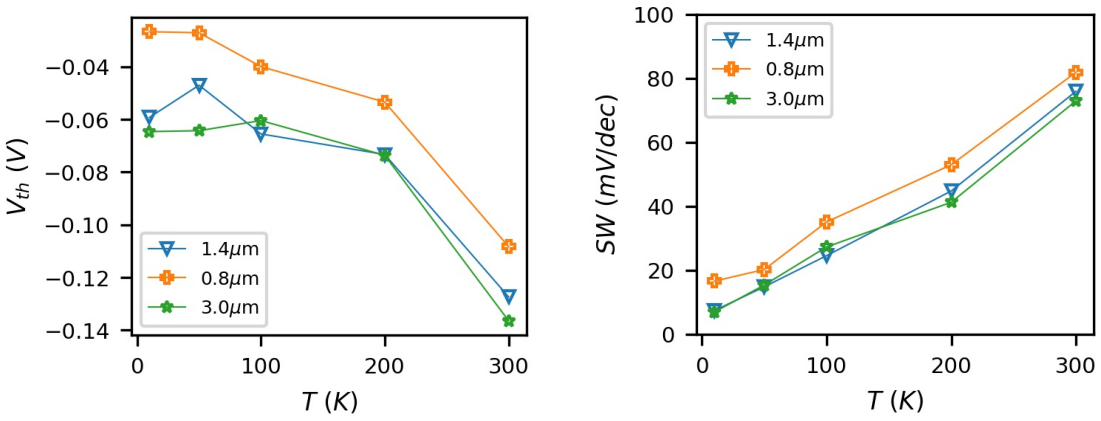
(a) *From the linear fit of Y in the Γ interval* ***(b)*** *From the average linear fit of Y*

Figure 5.10: *Extracted low-field mobility versus T for different Source-Drain distances*

Figure 5.11 reports the extracted values of threshold voltage and subthreshold swing for the different lengths of the access region. As we have a global look at Figure 5.11, it

is immediate to notice how the device with the shortest L_{SD} stands separately from the longer two. At this stage, it is not possible to conclude if this is either due to variability in the technology or to neutral defects penetrating a bigger percentage of the channel, as we suspected in the study for different channel lengths.

On the contrary, what we can confirm is that 1.4 μm seems indeed, for this technology, be the L_{SD} sweet-spot, as already shown by IBM Zurich (its manufacturer), who chose to use it as reference in the production.

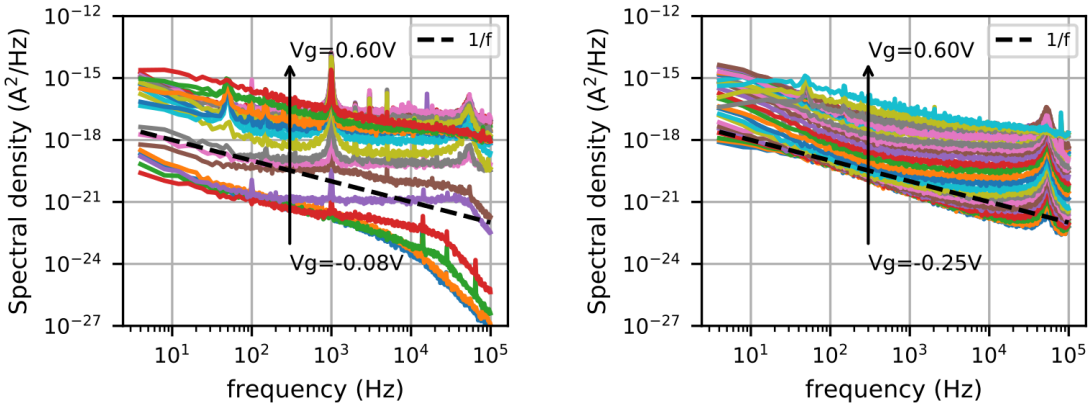


(a) *Threshold voltage* ***(b)*** *Subthreshold swing*

Figure 5.11: *Extracted V_t and SS versus T for different Source-Drain distances*

5.2 Noise

In heterostructure HEMTs, the lack of oxide may affect the uniformity of traps at the channel interface, especially when considering small devices. Figure 5.12 shows however that for the measured 2-channel device with W_g = 50 μm and L_g = 130 nm, the overall drain current power spectra at both 300 (Figure 5.12b) and 10 K (Figure 5.12a) abide a 1/f-like behavior, indicating a uniform distribution of traps.



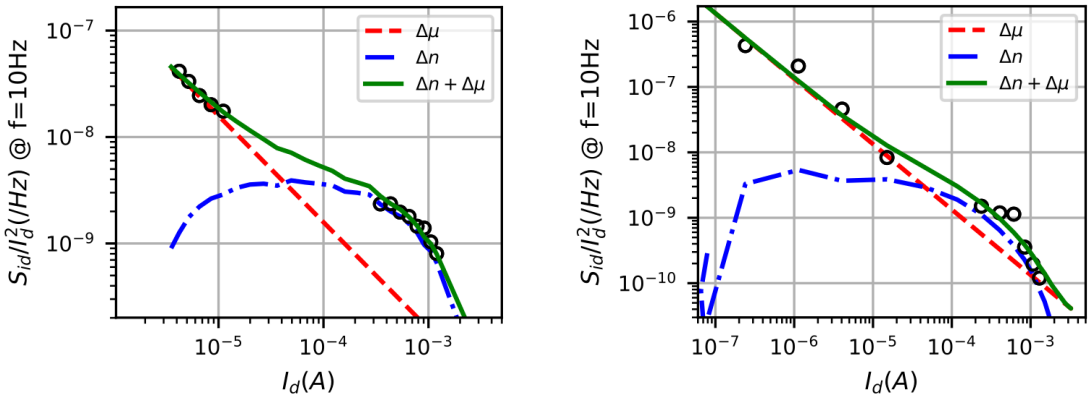
(a) *T = 10 K* ***(b)*** *T = 300 K*

Figure 5.12: *Measured drain current noise spectra for W_g =50 μm and L_g = 130 nm*

As Figure 5.13a shows, the extracted noise spectral density at 10 Hz seems to follow a $\sim 1/I_d$ trend in the low drain current range, revealing a dominance of channel mobility fluctuations ($\Delta\mu$), expressed by equations (1.11) and, as rephrased in [161], (5.4), where α_H is the Hooge parameter.

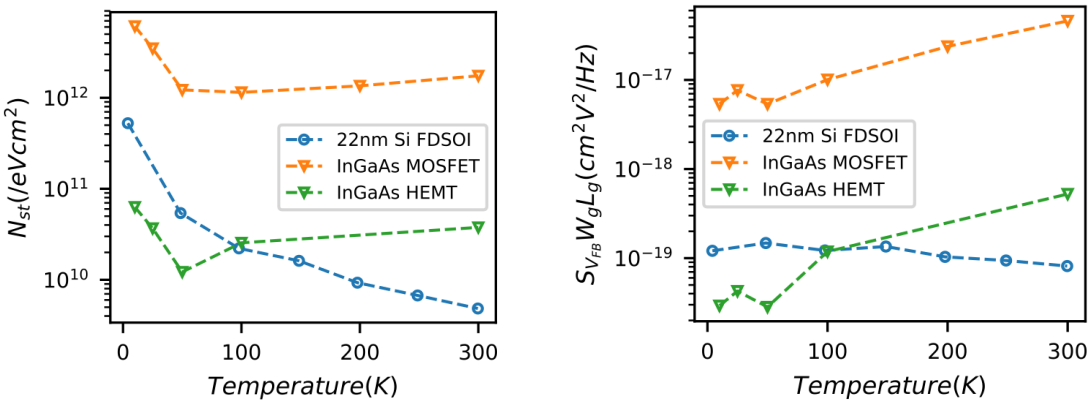
$$\frac{S_{I_D}}{I_d^2} = q\mu_0 C_{ox} V_d \frac{\alpha_H}{f L^2 I_d} \tag{5.4}$$

This effect usually takes place in bulk-conducting devices, such as the HEMTs in this work, which indeed conduct mainly in the volume of InGaAs before reaching strong inversion at the surface with InAlAs. Moreover, [94] suggests that in presence of inter-valley scattering, mobility fluctuations should dominate noise spectra in non-degenerate semiconductors.



(a) T = 300 K *(b) T = 10 K*

Figure 5.13: *Normalized drain current noise at f = 10 Hz with CNF and Hooge fittings (W_g = 50 μm and L_g = 100 nm, V_d = 30 mV)*



(a) Interface trap density *(b) Flat-band voltage PSD*

Figure 5.14: *Extracted parameters versus temperature for different technologies*

Above V_t, the data is well fitted with the Carrier Number Fluctuation (Δn) model (as explained in the section 1.2.4), meaning that the trapping/detrapping of carriers in the

InGaAs/InAlAs interface traps takes the lead once the channel is formed. These two noise mechanisms were both found to be still active at 10 K, as shown in Figure 5.13b.

The extracted interface trap density, N_{st}, shown in Figure 5.14a, was found to be significantly lower than the Al_2O_3-based InGaAs MOSFETs (studied in the previous chapter) reported again here for comparison, confirming the interface superiority of HEMTs. Furthermore, when compared to industry-level FDSOI MOSFETs [90], the N_{st} of HEMTs is found to be higher at 300 K, while outperforming them for $T < 100$ K. As a result, the HEMT area-normalized flat-band voltage noise, $S_{V_{fb}}$, which is a direct measure of the equivalent gate voltage noise, is significantly lower than FDSOI MOSFETs from 50 K and below, as shown in Figure 5.14b, revealing a promising advantage for amplifier applications, where the input signal-to-noise ratio is critical.

5.3 Self-Heating Effect

This section studies self-heating effects in InGaAs cryogenic HEMT devices, which aim at the enhancement of control/readout electronics performance in quantum computers. Starting from the well-known method of gate resistance thermometry, documented in literature for its reliable results, we characterized these devices down to deep cryogenic temperatures, namely 10 K, typical of signal-processing electronics for qubits, such as low-noise amplifiers (LNA). We furthermore compared the results with those belonging to far more industrialized silicon technologies (Si FDSOI and bulk), showing exceptional performance of the InGaAs HEMTs thanks to their lack of buried oxide and quantum well structure, which combined with their high electron-mobility, makes them a great study case for the technologies of the future.

Particularly, self-heating represents an issue that not only interferes with the low-temperature-induced boost in performances but also gives rise to the thermal noise in the amplifier, distorting the signal from the qubit before it can be processed.

Several studies have already been carried out on self-heating, more thoroughly for Silicon (Si) devices and with an increasing interest for III-V. Particularly, Choi et al. have characterized InGaAs-based HEMTs' SHE down to 20 K [107], while Ardizzi et al. have studied GaAs HEMTs down to liquid helium temperatures analyzing the noise temperature [106]. This work will instead study the self-heating effect of InGaAs-based HEMTs down to 10 K, revealing their capacity to dissipate heat efficiently and abide by their ambient temperature, while bench-marking them moreover with well-documented Si CMOS.

For the present study, we tested single channel devices with channel width of 10 μm and channel length spanning from 50 nm up to 200 nm. In all cases, the distance between source and drain regions was 1.4 μm.

As shown by Paliwoda et al., many methods have been developed to assess self-heating [163]. One of the most reliable methods amongst them is gate thermometry, which relies on 4-terminal gate resistance measurements using a custom test structure, as it is shown in Figure 5.15 for the technology at hand. As explained in [99] and [100], the increasing temperature in the channel causes a quasi-instantaneous heating of the gate metal which is measured through the induced change of the gate resistance. Thus, the gate resistance thermometry measurements consist of recording the current flowing between two metallic pads connected to the transistor's gate biased with a small differential voltage ΔV_g (30 mV in our case). As the drain voltage, V_d, increases and the device

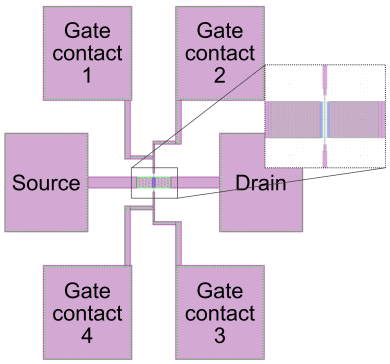


Figure 5.15: *Schematics of the contact pads, with multiple gate-pads dedicated for gate thermometry [162]*

enters saturation region, the current ΔI_g flowing between the gate pads decreases due to an increase in the resistance, caused by the self-heating of the device.

The raw gate thermometry experimental results we obtained are presented in Figure 5.16, for three different gate lengths and the two extreme temperatures, T = 10 K and T = 296 K. By looking at the right axis ΔI_g, we can at first glance already see, how self-heating has a bigger impact at cryogenic temperatures than it has at room temperature. This is a first confirmation of how important this effect truly is, particularly within the framework of LNAs. Moreover, looking at the left axis I_d, we see how the devices reach different current levels, and therefore dissipated power, for the same applied drain voltage V_d. Yet, although the 50 nm length device dissipates more power, it seems to perceive a weaker self-heating effect than the other two geometries.

We first extract the gate's metal pad resistance R_g using the following equation,

$$R_g = \frac{\Delta V_g}{\Delta I_g} \tag{5.5}$$

at the beginning (V_d = 0 V) and the end of each measurement, as it is shown in Figure 5.17.

By looking at the initial and final values of R_g in Figure 5.17, we can see how in terms of absolute value, the resistance change at the initial and final temperature is quite small, giving a first insight of the good heat dissipation of these devices.

Next, we compute the self-heating-induced temperature variation ΔT as,

$$\Delta T = \frac{R_{g,final} - R_{g,intial}}{dR_g/dT} \tag{5.6}$$

after linear regression of R_g(T). and we plot it in Figure 5.18 versus the dissipated power P, which can be expressed as,

$$P = I_d V_d \tag{5.7}$$

in the channel. The linear increase of ΔT with P can provide the thermal resistance R_{th} given by [102],

$$R_{th} = \frac{\Delta T}{P} \tag{5.8}$$

by linear regression.

Figure 5.18 confirms what we already observed in Figure 5.16: the devices reached different dissipated powers, it also shows that the self-heating is impressively low in the L_g

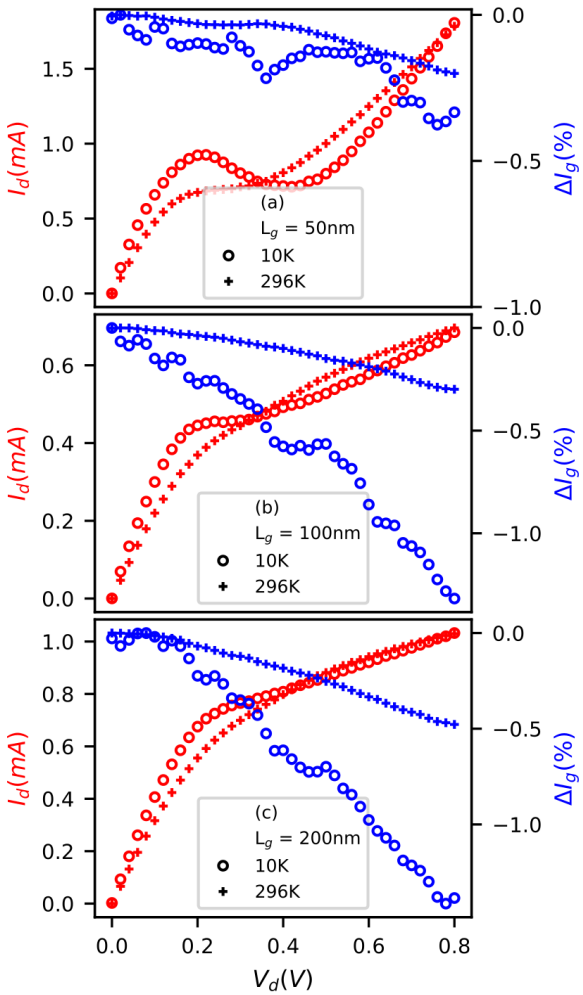


Figure 5.16: *Raw measurement of gate resistance thermometry at T = 10 and 296 K for all gate lengths L_g [162]*

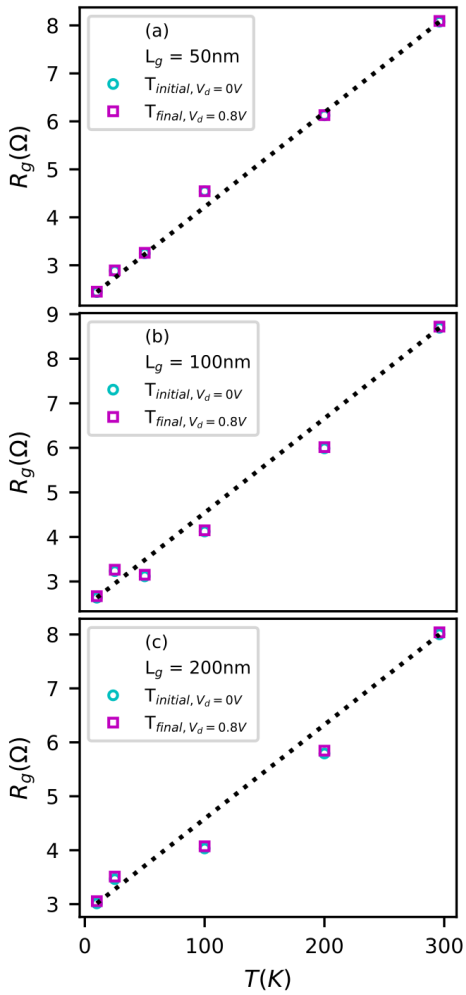


Figure 5.17: *Resistance of the gate metal vs temperature at initial and final stages of measurement for all gate lengths L_g [162]*

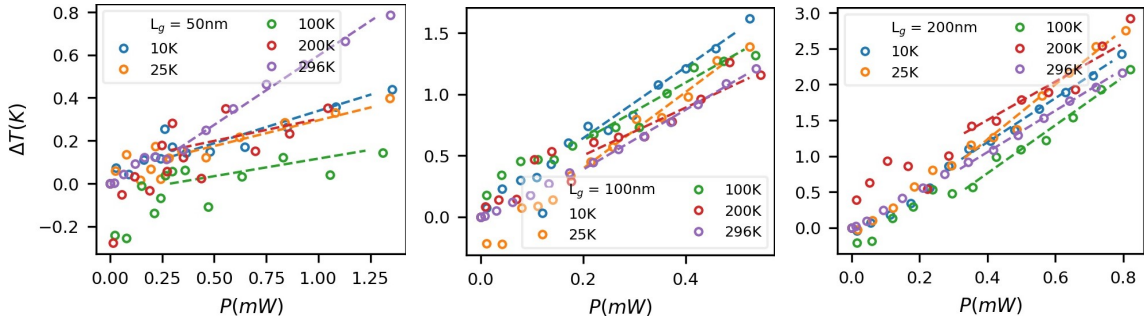
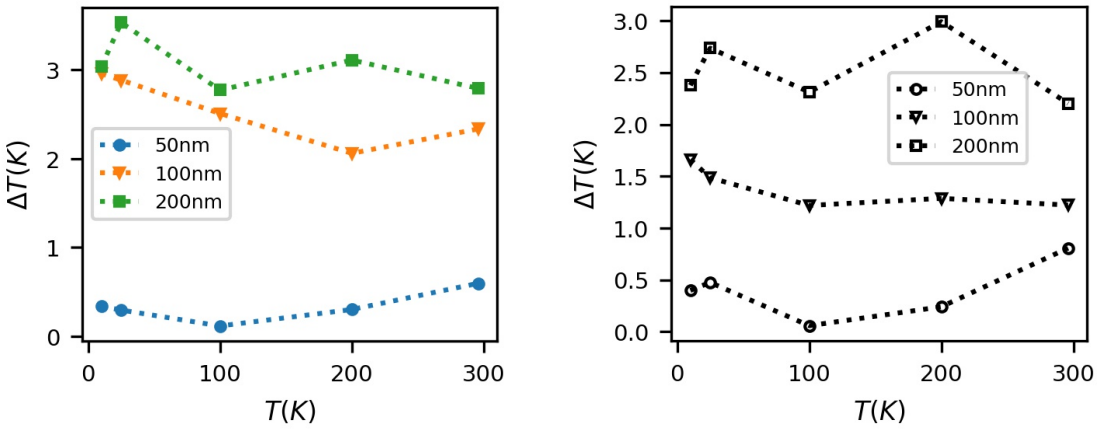


Figure 5.18: *Self Heating versus dissipated power in the channel for W_g = 10 µm and all gate lengths L_g [162]*

= 50 nm device. This forces us to only consider a higher P-range to extract R_{th}. To achieve a more consistent extraction approach, we applied this rule to all devices, extracting R_{th} only in the second half range of the dissipated power, as one can see form the extracted

linear slopes in Figure 5.18.

Finally, looking at the values of ΔT in Figure 5.18, we are reminded that the self-heating in these devices is indeed very low, as we could foresee from Figure 5.17.



(a) *at constant P* ***(b)*** *at constant V_d*

Figure 5.19: *Extracted Self Heating for W_g = 10 μm and different channel lengths versus temperature [162]*

Moreover, this allows to extract ΔT at a constant P of 1 mW, which is plotted vs temperature in Figure 5.19a; conversely, the values extracted at constant V_d are reported in Figure 5.19b. Note that longer channels present significant differences in ΔT according to the employed extraction, while the shorter device seems to display negligible ΔT in both cases: the channel of 50 nm is in fact sensibly shorter than the expected mean free path for these devices, which is in the order of 150-200 nm. A potential explanation would therefore be that the short-channel devices are operating in the quasi-ballistic regime, and self-heating occurs mainly at the drain region, rather than across the channel itself.

Surprisingly, increased R_{th} from phonon radiation at low temperature, which is observed for Si CMOS, is not visible here. Finally, Figure 5.20 demonstrates that the HEMTs under study, being bulk-like devices, have a very good heat dissipation (low R_{th}), close to state-of-the-art bulk Si CMOS [103] and much better than FDSOI MOSFETs [102].

5.4 Conclusions on LNA for QC

We have experimentally characterized self-heating effect in InGaAs cryogenic HEMTs fabricated by IBM Research – Zurich, through gate resistance thermometry. It was shown that R_{th} remains constant down to 10 K, with a significant improvement in aggressively short devices. The combination of a bulk structure and high mobility enables efficient heat exhaust, resulting in low levels of self-heating.

The results build up the understanding of the cryogenic operation of state-of-the-art HEMTs for qubit readout amplification and reassure that in terms of self-heating they can safely replace bulk Si CMOS. So far, we have studied these HEMT devices concerning their DC operation, the effect of the access regions, the low-frequency noise, and the self heating. Indeed, these devices have performed surprisingly positively with respect to any expectation.

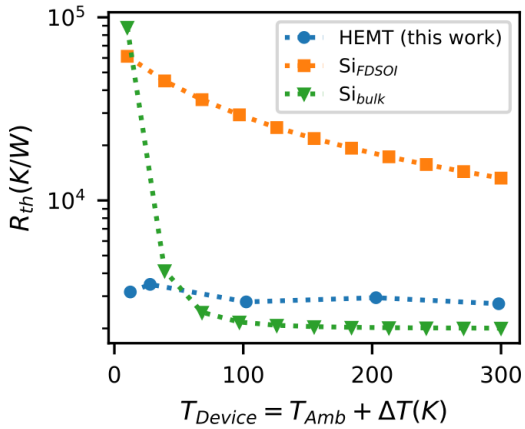


Figure 5.20: *Thermal resistance versus temperature for different technologies [162]*

When recalling the context of cryogenic low-noise amplifiers for quantum computers, we can readily see how they lay the bases to a class of devices that will perform as needed. Starting from the main concern of LNAs for QC, the self-heating has been managed very well, thanks to their bulk nature, allowing low levels of thermal noise, that will be in line with the ambient temperature the device is placed at.

When looking at the extracted mobility and the DC performances, we did see how as expected they resent of a strong gate leakage due to the absence of oxide. Conversely, given the high value of their low-field mobility at very small V_g and given the quality of the 2DEG, we can safely have them operate at very low power with nonetheless a high output current and gain. Indeed,their extremely low subthreshold swing at deep cryogenic temperatures will allow to operate them at very low V_g, working only with carriers from the Γ valley.

Finally, the LFN analysis has shown how, apart form the noise generated form the thermal vibration inside the devices, the signal coming from qubits will be amplified with a very low level of distortion from the amplification.

Conclusively, even if they do not share the same technological maturity of FDSOI, they have shown great potential and making a case for future research for cryogenic LNAs.

5.5 Further work on satellite valleys

This section does concern the study of InGaAs HEMT, but not within the context of LNAs: here these HEMT will be looked at as means to better understand the physics of InGaAs at cryogenic temperature. Their 'clean' performances and high-quality of 2DEG make a great study case to better observe unaffected the effects of solid state physics in these devices, as they should be less affected by scattering ideally.

As a matter of fact, what follows is not to be regarded as a mature output of this work but more as an input for future research, as the study of satellite valleys at cryogenic temperatures will need further study

5.5.1 C-V measurements

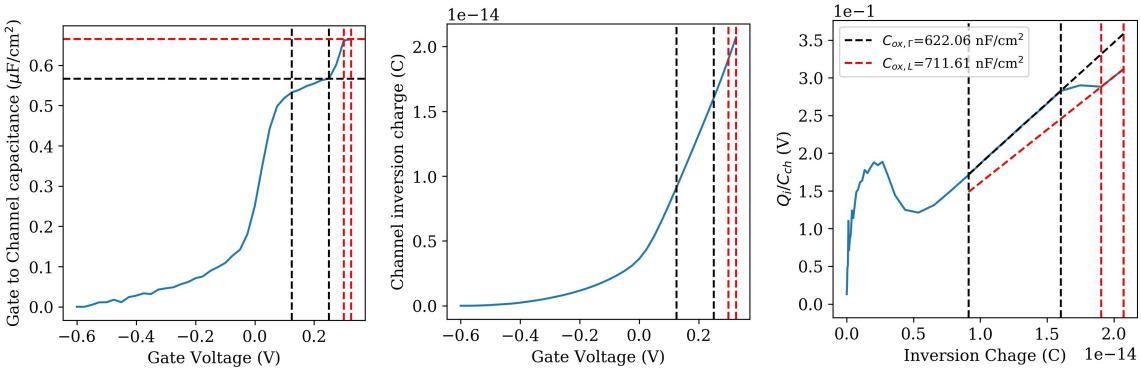
As already explained, due to their absence of Gate dielectric, HEMT are prone to Gate leakage when V_g is pushed towards high values. For this very reason, it comes indeed generally hard to measure the gate-to-channel capacitance as a function of the Gate voltage.

On one hand, at room temperature the available V_g span for the measurement is easily too small to correctly measure the equivalent oxide capacitance induced by the buffer layers. On the other hand, if extremely low operating temperatures expand this span, as we saw, L valley comes into play with its very own equivalent oxide capacitance.

It is hereby reported in Figure 5.21 the C-V measurement at 10 K of a HEMT device with an area of 10 μm^2. Indeed, the gate-to-channel capacitance, here reported with respect to V_g in Figure 5.21a, is not even remotely as neat as what we saw for 28nm Si FDSOI in the third chapter. Yet, it shows somewhat a co-existence of two different plateau levels, possibly to attribute to two different conducting valleys.

Moreover, the inversion charge reported in Figure 5.21b seems to be almost perfectly linear: this is in line with the modeling results form the fourth chapter. Though, as we move to Figure 5.21c, we can see how $Q_i/C_{ch}(Q_i)$ is displaying two linear parts with different slopes. We tried to analyze them separately, marking in between black vertical dashed line the span we believe to be related to the effect of the Γ valley, while the one for the L valley is marked in between dashed vertical red lines.

Finally, Figure 5.21c furthermore reports the extracted values for the equivalent oxide capacitance for both valleys: as we can see there is indeed an increase in the $C_{ox,eq}$ moving form Γ to L valley. This would confirm the predictions of [82] as carriers populating the L valley would concentrate closer to the interface (or in this case the limit plane of the 2DEG closer to the Gate), resulting in a higher equivalent capacitance. Moreover, an average (in between the two valleys) value of $\sim$675 nF/cm^2 could actually be in line with absence of Gate dielectric.



(a) *Gate-to-channel C-V* ***(b)*** *Inversion charge* ***(c)*** Q_i/C_{ch}

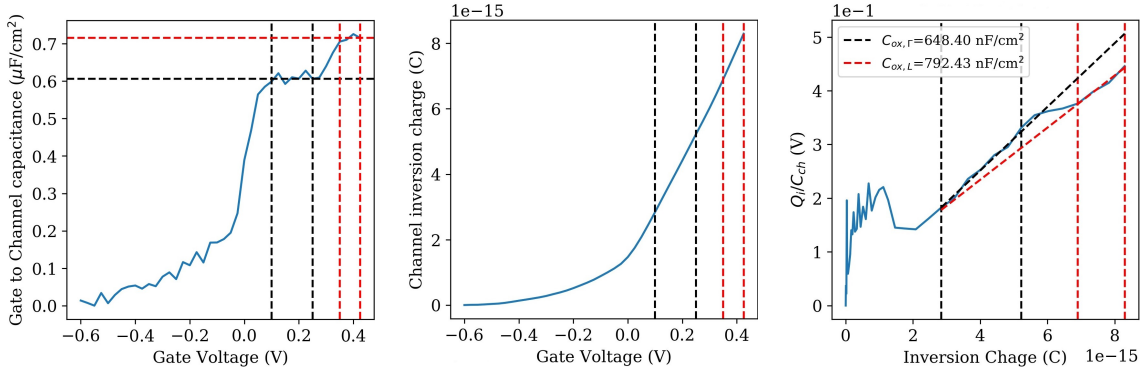
Figure 5.21: *C-V measurements at 10 K on a HEMT device with twin channels and W_g = 50 μm and L_g = 100 nm. the regions in between the vertical dashed lines mark what we considered as the regions of Γ (in black) and L (in red)*

The same measurement and analysis has been applied to smaller device with an area of 2.6 μm^2: Figure 5.22 reports the full measurement. As we can see form Figure 5.22a, this area is already small to the point the measured signal is not neat anymore. It is important to recall that in the case of FDSOI, where there was a Gate oxide, the areal limit we marked to have a clean measurement was 1 μm^2, less than half of the area measure in this

case. Yet, here once again the C_{gc} reported in Figure 5.22a is showing nonetheless two plateau.

When looking at the inversion charge, plotted in Figure 5.22b with respect to the Gate voltage, it is once again hard to spot any bending induced by the onset of the L valley. As we though move to Figure 5.22c, once again we see how the $Q_i/C_{ch}(Q_i)$ curve shows two different linear parts. This allows to extract, as well for the smaller geometry, the equivalent capacitances for both valleys.

Taking into account, the measurement noise due to the small area, the replacement of a simple dielectric layer with a semiconductor stack, and the possible variation in the depth of the 2DEG with the InGaAs layer, the two measurements would seem to give quite consistent results. Moreover, two more devices with the same small geometry have been measured at 10 K, producing similar results and the device with the bigger area has also been measured at 100K (not reported in this manuscript), once again showing similar trend and values in the extracted $C_{ox,eq}$.



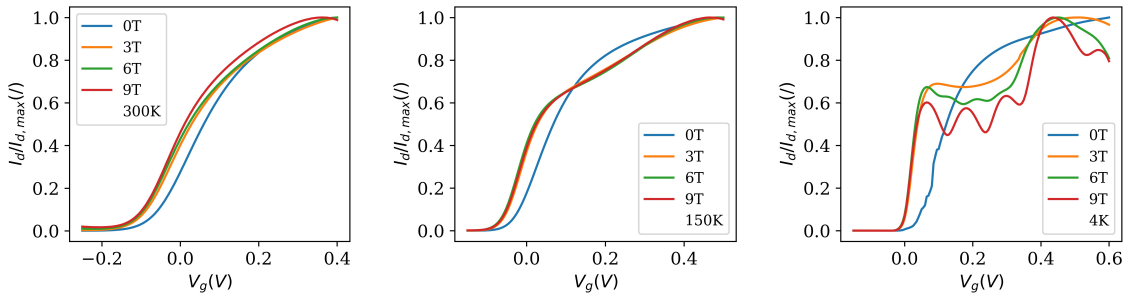
(a) Gate-to-channel C-V *(b) Inversion charge* *(c) Q_i/C_{ch}*

Figure 5.22: *C-V measurements at 10 K on a HEMT device with twin channels and W_g = 10 μm and L_g = 130 nm*

5.5.2 Magnetoresistance measurements

As we proceed to the measurements actually carried out in this work, we can see from Figure 5.23 the first effects of the increasing magnetic field on the transfer characteristic of the device at different temperatures. At B = 0 T, the $I_d(V_g)$ curves are similar to what we saw in the section on DC characterization: indeed, there only is a slight sign of L valley onset at 150 and 10 K. Yet, as B starts to increase, we see a downwards bending appear where the transition in between the two valleys should take place. Contrarily to what [95] shows, we see at all temperature a backward shift of the threshold voltage when the magnetic field is not zero, but as for now, we cannot give a solid explanation yet. From 150 K downwards, the $I_d(V_g)$ start to clearly show shoulders (and the humps at 10 K) over the two halves of the V_g range. Moreover, at 10 K, as the magnetic field reaches 9 T, we see that the downwards curvature becomes instead a series of fluctuations (Figure 5.23c).

As we move instead to Figure 5.24, it shows the results at 4 K of magnetoresistance measurements for relatively low values of the magnetic fields. Starting from Figure 5.24a, we see a confirmation of the results in Figure 5.23c, which shows the $I_d(V_g)$ curve normalized with respect to its maximum for different values of the magnetic field:



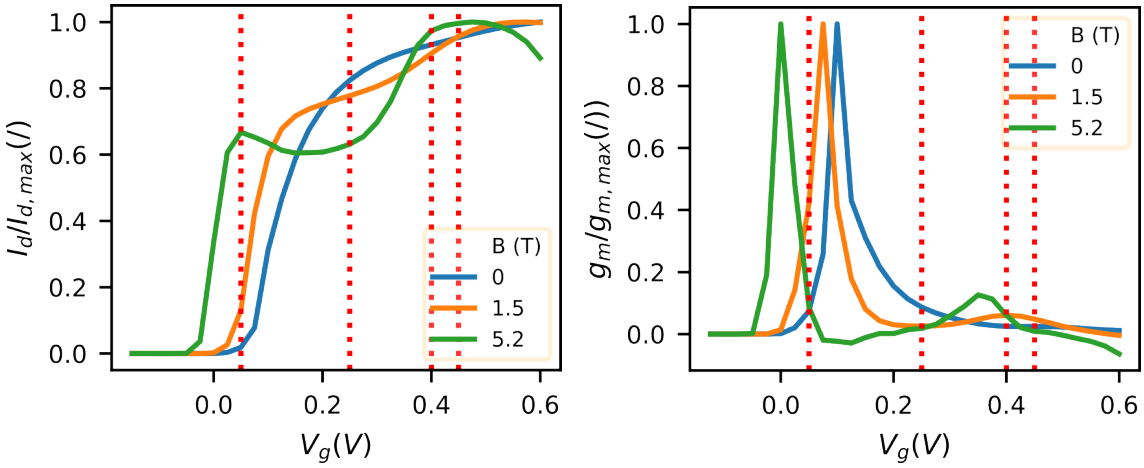
(a) T = 300 K *(b) T = 150 K* *(c) T = 10 K*

Figure 5.23: *Transfer characteristics of a device with W_g = 100 µm and L_g = 100 nm with respect to different magnetic fields $\vec{B}$*

1. The threshold voltage, V_t, shifts to lower values of the Gate bias, V_g, as the magnetic field increases

2. When the carrier conduction transitions from one valley (Γ) to another (L), we see a progressively deepening well (downwards curvature) for the increasing B

In parallel, Figure 5.24b shows the same effects reflected on the trans-conductance normalized with respect to its maximum: V_t is rolling off as shown by the main peak of g_m and with an increasing B, we see a progressively stronger second peak (in relative scale). The vertical lines present in both Figure 5.24a and 5.24b mark the values of V_g for which the relative change is plotted.



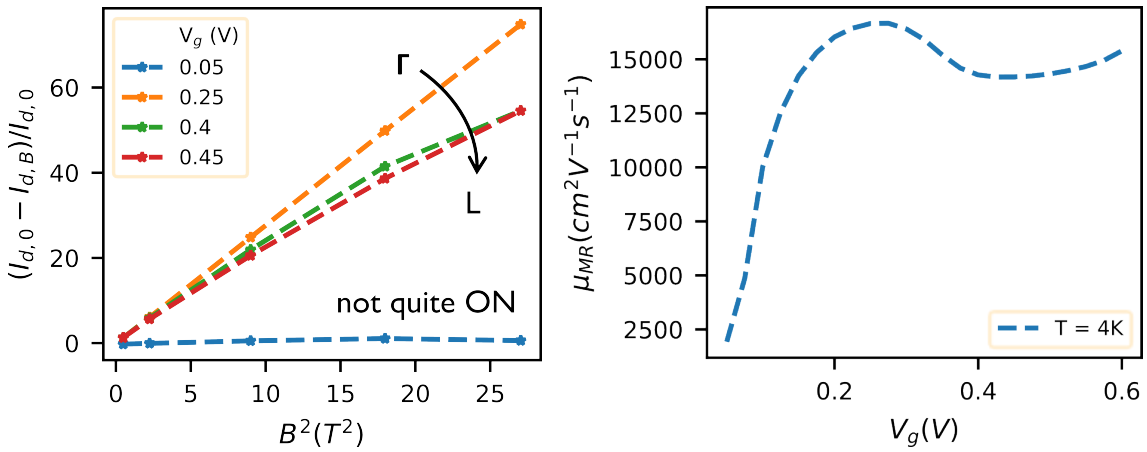
(a) Normalized transfer characteristics *(b) Normalized trans-conductance*

Figure 5.24: *4 K magnetoresistance measurement for a HEMT device with W_g = 100 µm and L_g = 100 nm*

Figure 5.25a shows indeed the relative change of the Drain current with respect to the square of the magnetic field, $\frac{I_{d,0}-I_{d,B}}{I_{d,0}}(B^2)$. As shown in equation (1.16), the slope we see for the different values of V_g is the square value of the mobility measured with magnetoresistance at that bias. Finally, Figure 5.25b shows the extracted μ_{MR}. As there was no availability for a different channel length at the time of the measurements, this mobility does not correspond to the one of the channel: we therefore reported it in arbitrary

units. What is though interesting is that, differently from the results shown by [95] for Si devices, we see μ_{MR} going back up after the first peak for this class of HEMT devices.

These results reveal a further hint of the presence of L valley conduction. On the other hand, due to the complicated physics behind multi-valley conduction and complicated set up of the magnetoresistance experiment, this is not enough to draw a solid conclusion on the topic. As shown by Lake Shore Cryotronics [164, 165, 166], Quantitative Mobility Spectrum Analysis (QMSA) is one very effective method of discriminating in between conducting carrier from one or another valley and could enlighten the unclear trends seen through these measurements.



(a) *Relative Drain current change* ***(b)*** *Extracted mobility*

Figure 5.25: *4 K magnetoresistance processing for a HEMT device with W_g = 100 μm and L_g = 100 nm*

5.5.3 Indications of X valley conduction

Before getting to the experimental data reported here, it is worth mentioning once again Figure 5.9a. Indeed, around a V_g value of 600 mV, there is, at 10 K, a second knee appearing in the transfer characteristics, much similar to the first we attributed to the onset of the conduction in the L valley.

We further investigated this effect and found it to happen systematically. Even if we hereby report the results for a single device for simplicity and ease of reading, it worth mentioning that we observed the same behavior in 13 devices:

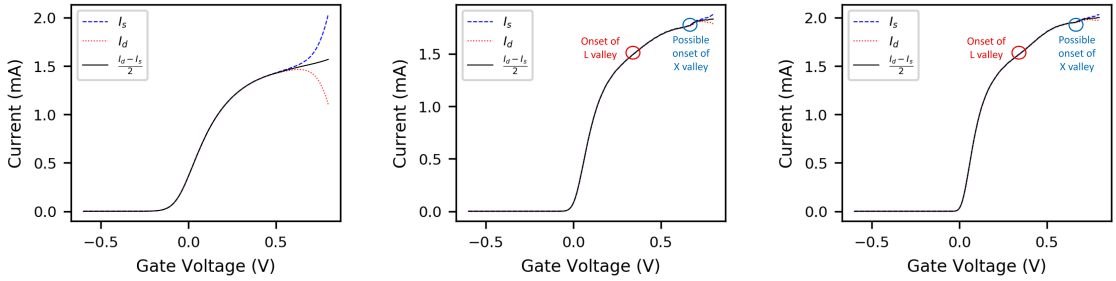
1. 5 devices with Gate width, W_g, of 10 μm and length, L_g, of 100 nm
2. 6 devices with Gate width, W_g, of 30 μm and length, L_g, of 100 nm
3. 2 devices with Gate width, W_g, of 50 μm and length, L_g, of 100 nm

Here, we only report the measurement for one device from the first group, therefore with W_g = 10 μm and L_g = 100 nm. Figure 5.26 shows the transfer characteristics of this device at 300, 100, and 10 K. We show altogether the raw Drain current (dashed red), the raw Source current (dashed blue), and the corrected Drain current [151] (solid black). Figure 5.26a shows the $I_d(V_g)$ at 300 K: comparing the raw Source and Drain current, we can readily see how the device is strongly affected by Gate leakage at room Temperature

for high values of the Gate bias. When looking instead at the corrected $I_d(V_g)$, there is no sign of any knee, as we had already learned form the DC study of the InGaAs MOSFETs and the HEMTs.

Contrarily, Figure 5.26b shows the same measurement at 100 K. Around V_g = 300 mV, we see the expected knee related to the L valley; strangely, around V_g = 650 mV, there is a second knee appearing. This behavior is once more confirmed at 10 K in Figure 5.26c, where we see the two knees appearing around the same V_g values as at 100K. The stability of the V_g values at which the knees appear is in fact in line with the constant behavior of V_t(T) below 100 K we saw in the DC analysis.

It is important to remark, we did not study this second knee in the DC characterization of HEMTs, as we initially kept the study limited to V_g = 600 mV, given the risk of Gate leakage. As a matter of fact, one could actually argue that, due to the leakage, this second knee appearing could indeed be an 'artifact' of the correction applied to the $I_d(V_g)$. Yet, we remark how this knee is appearing just slightly before the raw I_d and I_s split due to effects of leakage.



(a) T = 300 K *(b) T = 100 K* *(c) T = 10 K*

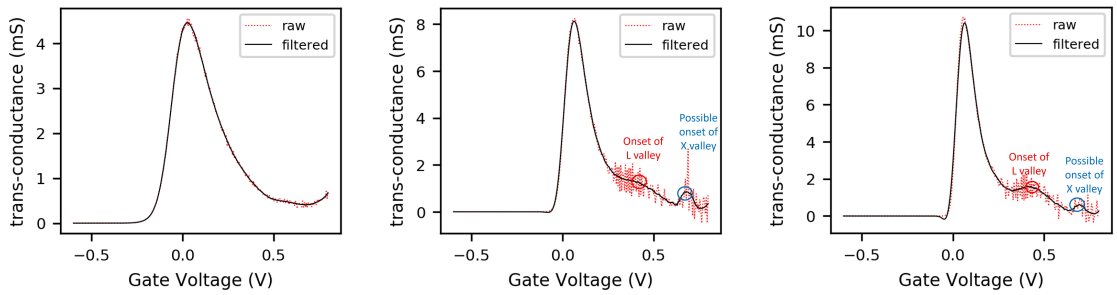
Figure 5.26: *Transfer characteristics of a device with W_g = 10 μm and L_g = 100 nm with V_g up to 800 mV. Drain current is reported in dotted red, Source current in dashed blue and the corrected I_d in solid black. The red and blue line mark the onsets of L and X valley respectively*

Figure 5.27 is instead showing the trans-conductance computed from the corrected Drain current. In order to present the problem in its entirety, we show both the raw data points coming from the corrected I_d and the filtering we applied to such g_m. If on one hand, g_m seems to be quite noisy, the filtered one, on the other hand, reports 2 clear peaks that appear at the lower temperatures. Particularly, the peak related to the L valley grows higher from 100 K (Figure 5.27b) to 10 K (Figure 5.27c).

Finally, in order to discriminate the effects induced by the Gate leakage on the trans-conductance, we compared in Figure 5.28 the g_m resulting from filtering the raw I_d, the raw I_s, and the corrected I_d for all temperatures As we can see from Figures 5.28b and 5.28c for a temperature of 100 and 10 K respectively, the different g_m start to split because of the leakage around the top of the second peak, indicating the second peak itself is an intrinsic effect we see in these devices at cryogenic temperatures.

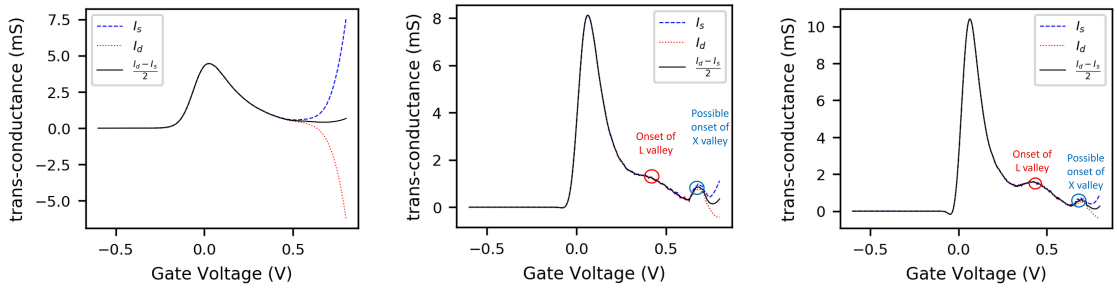
It would now be the moment of determining what this third peak is caused by. Indeed our first guess would be the onset of the X valley, but let us understand why.

one possible counter-explanation would be, if rather than the onset of satellite valley, this effect could be due to subbands of the same (Γ in this case) valley. Yet, we showed that the Y function is not only presenting a hump, but it also shows different slopes. Moreover, we have to recall two things:



(a) T = 300 K *(b) T = 100 K* *(c) T = 10 K*

Figure 5.27: *Trans-conductance of a device with W_g = 10 μm and L_g = 100 nm with V_g up to 800 mV. The red dots report the raw data, while the solid black line is the filtered g_m. The red and blue line mark the onsets of L and X valley respectively*



(a) T = 300 K *(b) T = 100 K* *(c) T = 10 K*

Figure 5.28: *Trans-conductance of a device with W_g = 10 μm and L_g = 100 nm with V_g up to 800 mV. The g_m computed from the raw Drain current is reported in dotted red, the one computed from I_s in dashed blue and in solid black there is the g_m computed from the corrected I_d. The red and blue line mark the onsets of L and X valley respectively*

1. As the temperature keeps on dropping, for each conducting valley, we see more and more only the ground state (i.e. $E_{0,\Gamma}$, $E_{0,L}$, and $E_{0,X}$). This is the same principle that allowed us to safely employ in the Kubo-Greenwood section the 'single subband approximation' and has been well explained in [38, 37].

2. The 2D electron gas where electrons flow through these HEMT devices is, by definition, very thin, similarly to a quantum well. Therefore as we recall the effects of 2D quantum confinements on conduction valleys, we see that the thinner the well, the higher up in energy the non-fundamental subbands are pushed away from the fundamental one.

Finally, considering how, in 2 different structures of InGaAs devices we have seen clear signs of conduction in the L valley, one possible and straightforward explanation would be that we are, by pushing the Gate bias to such high values, 'igniting' conduction in the satellite X valley as well.

6. *Conclusions*

This conclusion chapter is organized in the three following parts:

1. a comparative synthesis on cryogenic FET: this is summarizing what we have shown for the three technologies under study concerning DC and noise analysis

2. a conclusion on processing electronics within the framework of Quantum Computers

3. some considerations and outlook on how future research might address the still pending questions left after this work

6.1 Comparative synthesis on obtained results

6.1.1 motivation and structure

As explained before, this section is not apporting new results or considerations to the work. To better say, it reformulates some of the results shown in the previous sections. As DC and noise analysis were carried out thoroughly for all three technologies under study (28nm Si FDSOI, InGaAs MOSFET, and InGaAs HEMT), it will be useful, especially for the readers with less experties in the field.

Indeed, we report here the study of these technologies in parallel: this will allow to see how the physics at cryogenic temperature differs according to the channel material or the geometry. In fact, this 'synthesis' is meant to be a tool to quickly understand cryogenic MOSFETs at first hand in a comparative and all-round way.

The figures that follow in this section are taken form the previous chapters, either as they were originally shown or with slight layout modifications. As, we will focus on comparing trends and understanding the difference amongst the three technologies, the following figures are not commented in detail, as they were already in their original chapter. For this reason, each main figure is commented in such a way to describe the figure of merit under study and each subfigure only reports the label of the technology and the original figure it comes from (e.g. '(28nm Si FDSOI) F.1a') with a link within the pdf file.

Particularly, for the novices to the field, who seek to understand this type of cryogenic solid-state physics, more than the peculiarities of each technology, we foresee this section being of great use. This part, yet, does not summarize the introduction to cryogenic FET unraveled in the first chapter.

6.1.2 DC analysis

As we look at Figure 6.1, we can have a first glance at the evolution of the transfer characteristics as it goes down to deep cryogenic temperatures. Before commenting, it is important to recall the importance of this figure: the transfer characteristics $I_d(V_g)$ shows the output Drain current as a function of the spanning Gate voltage. When studying and understanding MOSFETs, this is our starting point because it gives right away a qualitative idea of the electrostatic control of the Gate, which is indeed the principle MOSFETs rely on (Metal-Oxide-Semiconductor Field-Effect-Transistors).

The $I_d(V_g)$'s shown allow us understand that all three technologies experience the first two effects of cryogenic temperatures. As we can firstly see, the threshold voltage of the curves is moving forward for a decreasing T: indeed, as the temperature goes down, we have to be reminded that electron promotions to the conduction band is thermally activated and therefore, we will progressively see always fewer electrons for the same value of V_g as T goes down (before strong inversion).

As we instead look at the higher V_g regions that account for strong inversion, we see the value of the Drain current increase for lower temperatures: this is in line with the reduction of phonons at cryogenic temperatures. Being the solid-state representation of the thermal vibration in the channel, as temperature decreases, phonons will decrease as well: this will imply a reduction of phonon scattering at cryogenic temperatures, that will yield a boost of the low-field mobility.

As we take a deeper look at Figure 6.1, we see how both InGaAs-based technologies present some shoulder appearing at cryogenic temperature. We attribute this to the onset of conduction in the L valley of the conduction band of InGaAs. This is in line with:

1. this is happening only in the InGaAs devices, as Silicon conducts only its lowest valley around the X point of the Brillouin zone, for the other satellite valleys are too high in energy

2. we see this shoulder appearing as a function of a spanning V_g: indeed the increasing Gate bias would fill up first the bottom valley (Γ for InGaAs) and progressively the satellite as well

3. the Drain current seems to experience a lower mobility past this knee, which would be in line with a satellite valley with an intrinsic lower valley

This effect would also be well explained by cryogenic temperatures, as they imply a decrease of the k_BT factor, which is a direct measure of the window width of the energy span the Drain current is integrated on. In other words, at 300K this transition is melted away, letting us see a seemingly single mobility.

These effects we have just explained transfer directly onto the Y function, reported in Figure 6.2. We briefly recall that the use of Y is to visually preserve the linearity of $I_d(V_g)$ in strong inversion, by eliminating the influence of the access impedance, which induces a downwards bending in the plot of the Drain Current.

The Y function shown for FDSOI lets us see how, even when going down to cryogenic temperatures, Y remains linear, thus being a powerful tool in the analysis of FETs at cold temperatures. Conversely, InGaAs devices see the shoulder appearing in the $I_d(V_g)$ translate into an actual hump in Y. Yet, as we see in Figure 6.2b, this hump can actually be overlooked in an attempt to extract the overall linearity of Y across a broader V_g span. This is indeed the method we used to extracted threshold voltage and low-field mobility for these technologies.

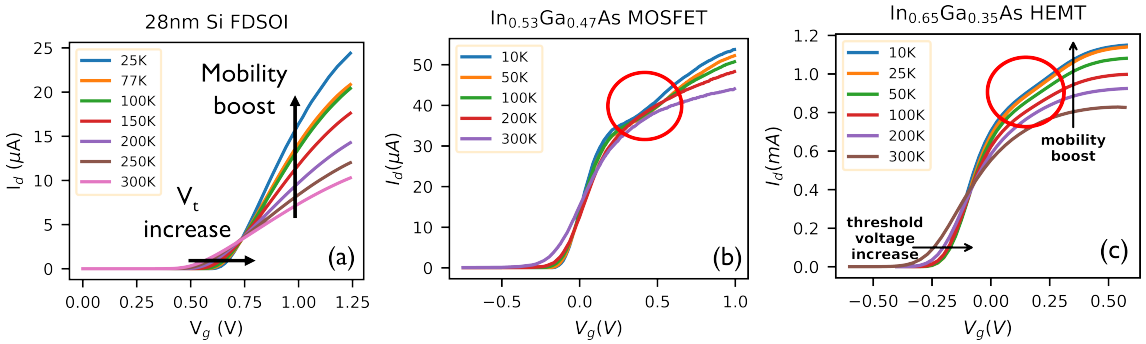


Figure 6.1: *Transfer characteristics down to cryogenic temperature at V_d = 30 mV; (a) F.3.6; (b) F.4.2a; (c) F.5.2a*

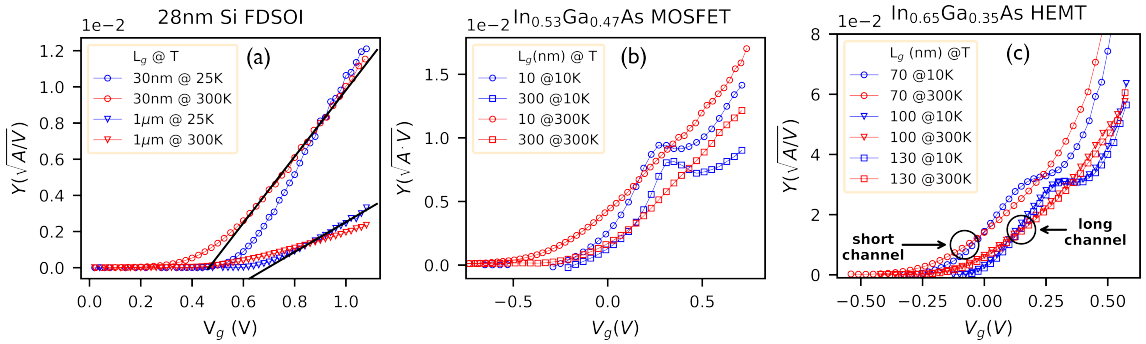


Figure 6.2: *Y function down to cryogenic temperature at V_d = 30 mV; (a) F.3.8a; (b) F.4.2b; (c) F.5.4*

Figure 6.3 reports the value of the threshold voltage, V_t, extracted with Y for all three classes of devices. As we firstly explained when analysing the Drain current, the thermally-activated nature of carrier promotion to the conduction band induces an increase of V_t for lower temperatures. We can see this increase is about linear, up to a certain temperature point, where V_t starts to settle. This settling is due to the semiconductor transitioning from a non-degenerate statistics to a degenerate one.

On one hand, we see the linear increase of V_t with respect to the temperature only for FDSOI, as they seem to have a transitioning point of the statistics lower ($\sim$ 100 K) with respect to the InGaAs devices ($\sim$ 200 K). On the other hand, we can see that, independently form the technology, devices with a shorter channel maintain across the full temperature span a lower V_t (roll-off) with respect to longer channels.

Indeed, the short channel effects, such as the threshold roll-off, are depending on the Gate electrostatic control over the channel, which becomes more difficult to handle for smaller geometries. Though, Gate electrostatics should not be affected by temperature, as it is proven by the extracted V_t. Particularly, for the InGaAs devices (MOSFET and HEMT), we see that longer channel and shorter channel are actually grouping apart, leaving a clean separation when the short-channel effects are triggered.

Figure 6.4 shows the second parameter extracted through the Y-function method, the low-field mobility, μ_0. This parameter represents indeed the mobility of the channel at its maximum carrier concentration, before any attenuation induced by access resistance or scattering at the interface with the oxide.

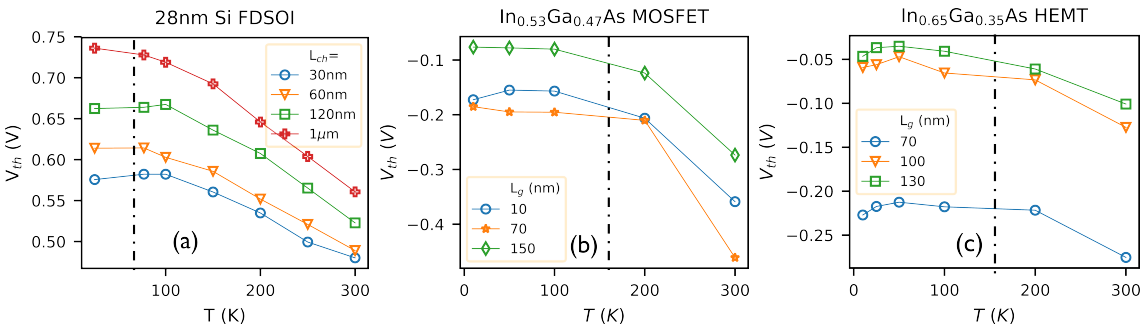


Figure 6.3: *Extracted threshold voltage with respect to temperature; (a) F.3.9a; (b) F.4.3; (c) F.5.7*

As explained before, the decrease in temperature allows a reduction in phonon scattering, which boosts the value of μ_0. Yet, as we look at the extracted values for the three technologies, we see a sensible increase only for devices with a long channel. Indeed, as we decrease the length of the channel we see a change in the predominant scattering mechanism: if long channels are ruled by phonon scattering, the shorter are governed by the influence of neutral impurities scattering (at least for MOSFETs), which is temperature invariant. To better understand the reason of this, we have to think that in a device with a shorter channel we are approaching the Source and Drain, whose high dopants concentration is inevitably going to diffuse in the attached section of the channel. Therefore, considering a constant overall length of the channel where the Source and Drain dopants diffuse, it becomes readily understandable how decreasing the length of the channel, we are actually cutting out the central part that was less affected by these diffusing dopants.

It has to be remarked that the extracted μ_0 values for 28m Si FDSOI and InGaAs MOSFET are actually comparable if taking into account the same channel length. This could as a matter of fact be adduced to the quality of the interface, which is much better in FDSOI, as Si and SiO_2 find a much better chemical affinity than InGaAs and Al_2O_3.

As we move to the HEMT technology, things have to be looked at in a slightly different way. Phonon scattering reduction is still a key in low temperature mobility, as can be seen for the longer channels. Indeed, μ_0 achieves very high values, thanks to lack of oxide and the high quality of 2DEG preserving the intrinsically high mobility of InGaAs. Yet, even here we can see that the mobility boost is mush limited for the device with shorter channel: the effect of neutral impurities is still present, but is not to be attributed to the approaching Source and Drain. In fact, besides the length of the channel, HEMT devices are structured in such a way to have additional access regions to separate Source and Drain: in the case of this class of devices, it is 1.4 μm. As a consequence, the neutral impurities taking over in the channel should most probably come from defects resulting from the fabrication of the Gate stack.

If the linear $I_d(V_g)$ reported in Figure 6.1 gives a good sense of the amplification of a MOSFET, its logarithmic plot grants an immediate understanding of good the Gate electrostatics is in terms of switching-ON/switching-OFF. Figure 6.5 reports the $log_{10}(I_d)$ as function of the panning Gate voltage for all three technologies.

Here we see the effect of the third main effect of low temperatures: the decreasing temperature induces a sharpening of the Fermi-Dirac statistics. As explained in detail in the introduction chapter, taken to a current-level concept, this statistics translates into an OFF/ON state of the MOSFET. Thus, its low-temperature-induced sharpening yields a

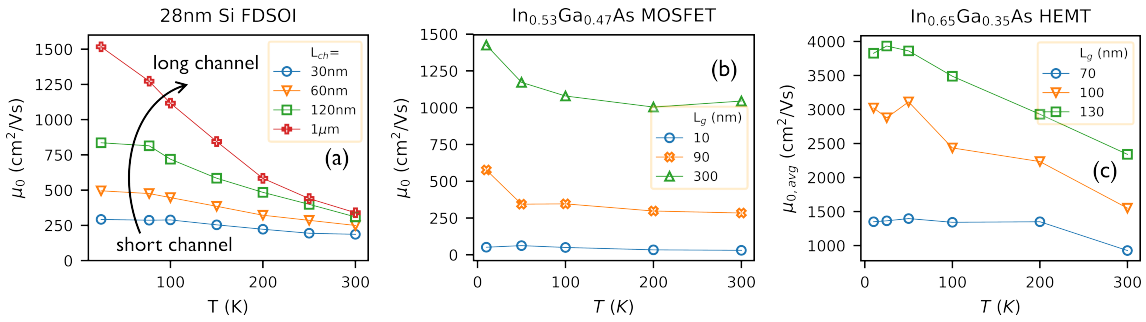


Figure 6.4: *Extracted low-field mobility with respect to temperature; (a) F.3.10a; (b) F.4.6; (c) F.5.6b*

sharper, more distinct transition in the switching of the device, therefore strengthening the control of the Gate and allowing to operate the device at overdrive voltages (V_g - V_t) not as high as at high temperatures.

Figures 6.5b and 6.5c furthermore show a degradation of this switching for shorter channels: this is one of the short channel effect explained in the introduction.

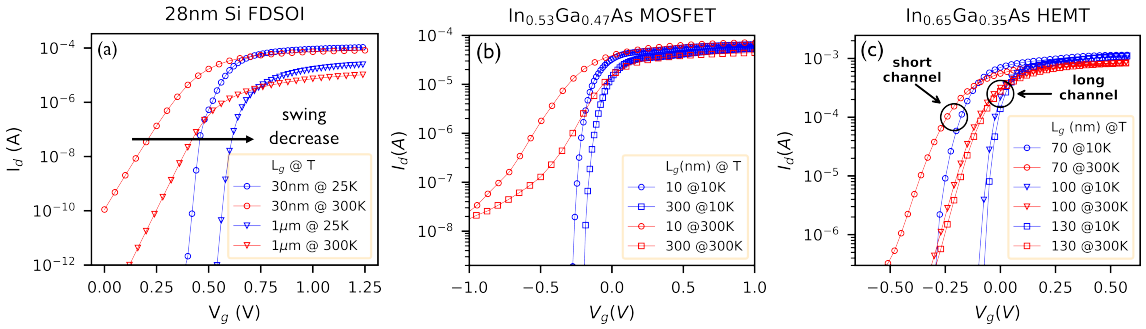


Figure 6.5: *Transfer characteristics (logarithmic) down to cryogenic temperature at V_d = 30 mV; (a) F.3.6; (b) F.4.4; (c) F.5.3b*

The improved low-temperature switching is finally quantified in the extracted values of the subthreshold swing, SW, reported in Figure 6.6. As a confirmation of what written just before, we see the values of SW decrease together with T for all technologies under study.

If we just focus on the values at room temperature, we see how FDSOI reach around 60 mV/dec for the longer channels: this is indeed the experimental limit observed for this technology. It is no surprise to see instead the InGaAs MOSFETs present much higher values, as a consequence of the poor (with respect to FDSOI) interface in between semiconductor and oxide. Conversely, the HEMT devices present competitive values ($\sim$ 80 mV/dec) thanks to the lack of oxide and to the good quality of the 2DEG.

At room temperature, a degradation of SW is visible for shorter channels in all technologies. If for MOSFETs this can be adduced to the short-channel effects explained above, for HEMTs the cause is rather to be sought in the Gate manufacturing process. Manufacturing short channel such as 70 nm, might induce, for the present state of the technology, some defects in the channel, particularly given the depth of the process.

Surprisingly, as we gown to deep cryogenic temperature, SW reaches similar values for all three class of devices, independently form the value at room temperature. More-

over, we see SW settle around 10 mV/dec in MOSFET: this is a well studied effect that has to be attributed to the band tail states, induced by lattice disorder. We know, from basic solid-state physics, that disorder changes the densities of states, transforming their low-energy end from sharp and neat to something that fades towards 0 as an exponential.

A confirmation of this effect can conversely be seen in HEMT devices: thanks to high purity of their 2DEG, the devices with longer channel would seem not to suffer from this effect, displaying a SW that seems not to settle. The values of the shorter channel are still higher at low temperatures, as the impurities form the Gate process would indeed affect the purity of the electron gas.

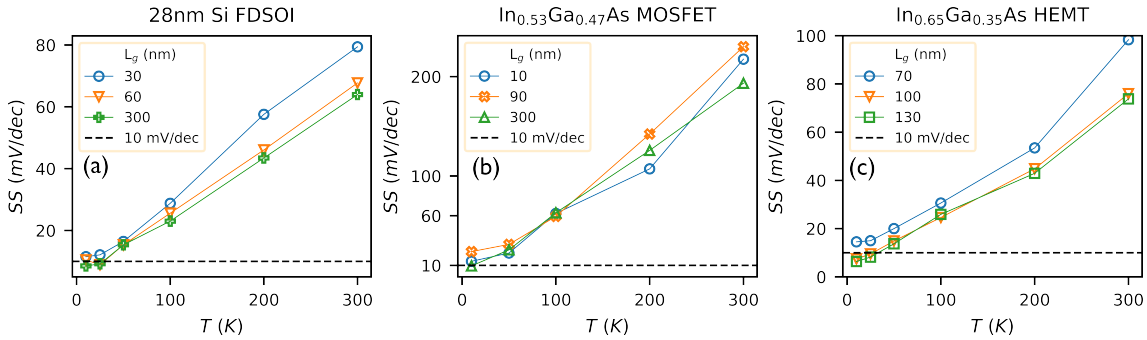


Figure 6.6: *Extracted subthreshold swing with respect to temperature; (a) F.3.11; (b) F.4.5; (c) F.5.3b*

6.1.3 Low-frequency noise analysis

This section focuse on the most immediate branch of low-frequency noise: Flicker, or 1-over-f noise. This is indeed a study that allows on first hand to understand the quality of the device and secondly, to see how clean the amplification of the device would be. As we explained in the previous chapters, Quantum Computing needs to amplify the signals of the qubits with the smallest possible distortion. As a matter of fact, a device that is highly noisy would put all that noise on the signal to amplify, outputting a distorted final signal.

As the basis of flicker noise have been already explained in the introduction, we can directly look at Figure 6.7, which reports the raw power spectral densities (PSD) at 300 K for all devices. Directly following the considerations on the oxide interface we have just presented, these PSD reflect the quality of the interface. In fact, in the case of the two MOSFET technologies, that present the same area in this figure, we see InGaAs MOSFETs present straight away a higher level of noise compared to FDSOI.

Moreover, we see that at 300 K all spectra have a reasonable 1/f behaviour, allowing us to apply the afore mentioned CNF + CMF model.

The 1/f trend seen above remain in the PDS at cryogenic temperatures, shown in Figure 6.8. It is important to remark that the PDS are more spread out in their values (for different values of V_g): this is a direct result of the increase of I_d at low temperatures. As I_d goes through a larger span at cryogenic temperatures, in the same way the respective PSD will see its values spread.

Figure 6.9 reports the PDS values normalized with respect to the square of the Drain current. This gives indeed a better idea of the distortion in the amplification induced by the device, as it is basically normalized on the amplification power of the device. Indeed,

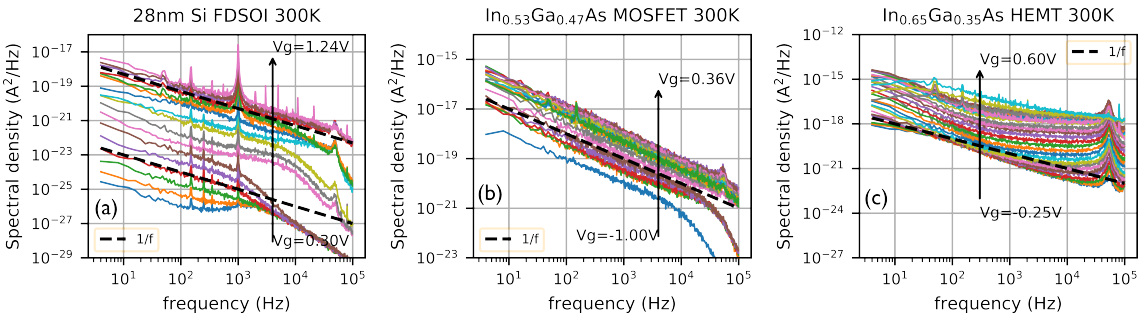


Figure 6.7: *Raw power spectral densities at 300 K; (a) F.3.15b; (b) F.4.11a; (c) F.5.12b*

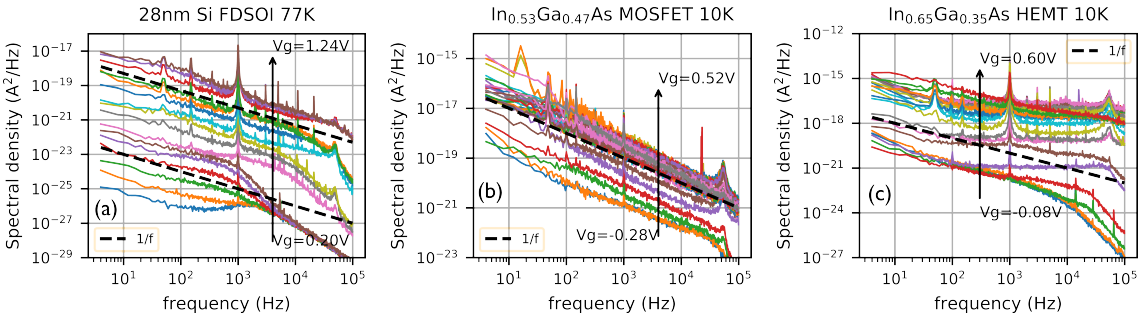


Figure 6.8: *Raw power spectral densities at cryogenic temperature; (a) F.3.15a; (b) F.4.11b; (c) F.5.12b*

as we could foresee, InGaAs MOSFETs show higher level of noise due to the quality of the interface, while HEMT devices seem to have values of noise comparable to the FDSOI devices.

As expected form the bibliography, MOSFET abide indeed to the model resulting from coupling the Carrier Number Fluctuation with the Correlated Mobility Fluctuation, with a slight effect of the access resistance in FDSOI for very high values of V_g. Conversely, HEMT devices presented a noise trend that could not be explained through the previous model: we had indeed to combing the Carrier Number Fluctuation (Δn) model with the Channel Mobility Fluctuations ($\Delta\mu$) model explained by Hooge. As can be seen from Figure 6.9c and 6.9d, resents of the noise induced by the channel mobility fluctuations at lower Gate biases.

This behaviour we see in HEMT devices is well explained by the lack of an interface with the relative defects. Therefore at low V_g values, where the $\Delta\mu$ noise is stronger than the Δn one, the scattering processes in the channel control the noise. For any electron, as a matter of fact, the number and types of scattering will differ and the direction of the path as well: this will mean that, for every moment, the electrons coming to the Drain will have had different traveling times, thus yielding small fluctuations in the mobility.

Finally, Figure 6.10 reports the flat-band voltage PSD down to 10 K: this is the most direct measure of the noise in the amplification acted by the FET device. It has to be remarked that as our 28nm FDSOI LFN study did not go down to 10 K, we reported here the results form a much alike class of FDSOI (22nm).

In this final, consideration concerning noise, we can see how InGaAs MOSFETs are maintaining across the full temperature range higher noise in the signal: this is an unavoidable consequence of the nature of the interface with the oxide used for InGaAs.

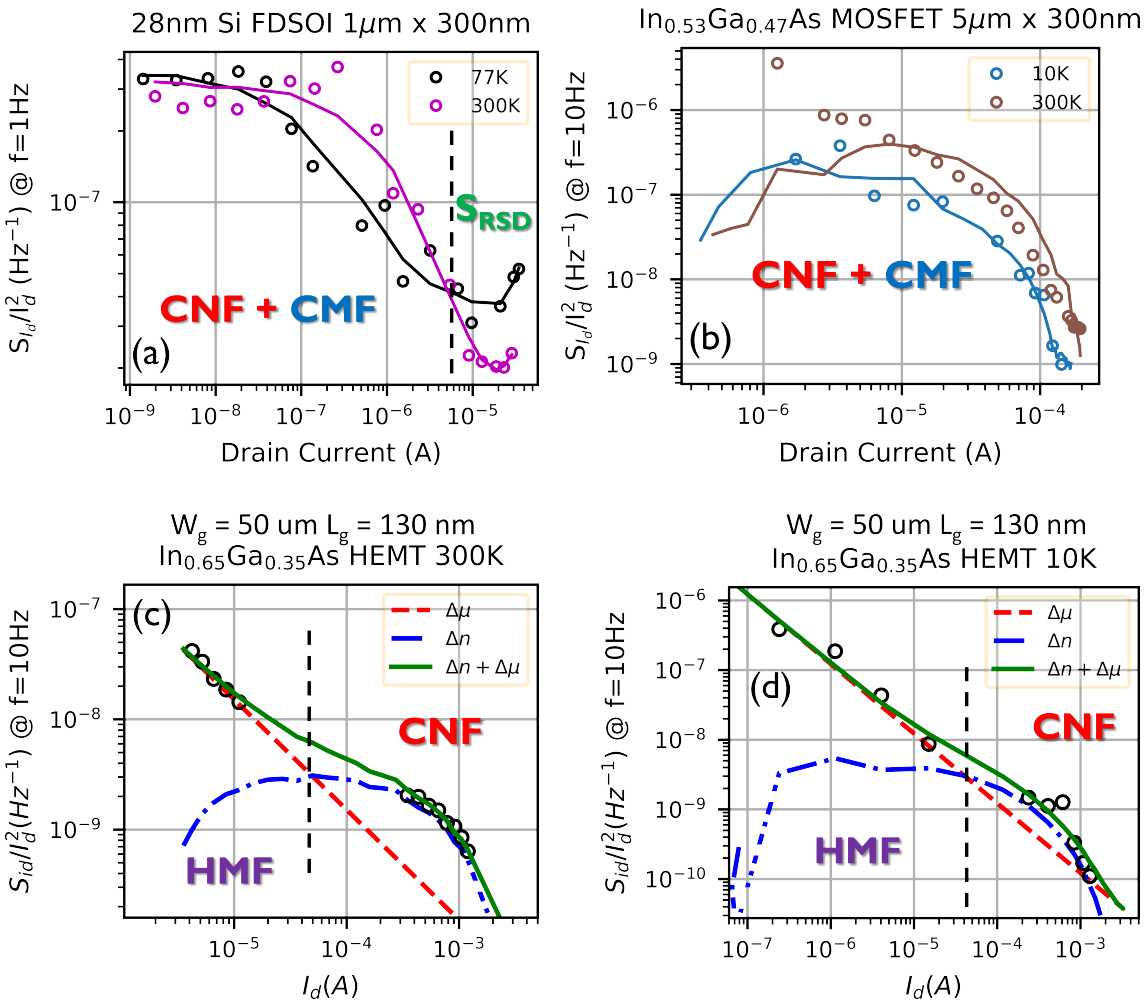


Figure 6.9: *Normalized PSD for all technologies with respect to I_d^2; (a) F.3.15c; (b) F.4.12; (c) F.5.13a; (d) F.5.13b*

FDSOI and HEMT show about comparable levels, but we surprisingly see HEMT devices outperforming FDSOI at deep cryogenic temperatures. If on one hand the high quality noise level in HEMT is explained by its lack of interface, on the other, future research will need to address why it decreases even below the levels of FDSOI.

6.2 conclusions on cryo for QC

When looking at the processing electronics in quantum computer, we see different needs and applications. Particularly, we have addressed as processing the readout electronics and the low-noise amplifiers (LNAs).

Readout electronics will find in quantum computers different architecturing, for which these different device will be better suited. Clearly FDSOI remain a standard: their highly industrial level makes their performances hard to match on an all-around scale. Therefore, in the need of readout electronics that needs to decode in mass the signals of the LNAs, FDSOI with its stable performance, low noise levels, and refined fabrication process will surely find its place.

Yet, if the readout electronics at hand was to be more focused towards low-power, we

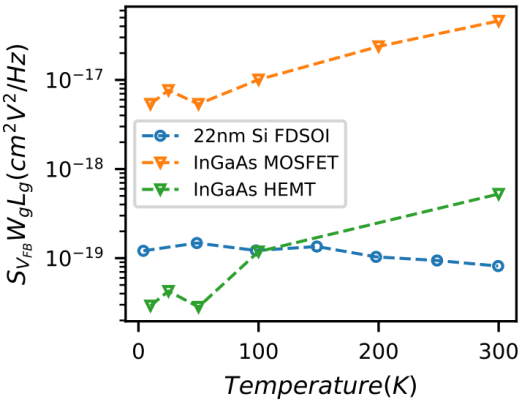


Figure 6.10: *Flat-band voltage PSD, F.5.14b*

saw how InGaAs MOSFETs maintaining a part of the high mobility of InGaAs crystal and are easily compatible in a CMOS process.

Finally when looking at the needs for low-noise amplifiers, HEMT devices are a good candidate. Thanks to their extremely low noise level and their bulk structure allowing ease of heat dissipation (i.e. low thermal noise), the noise within the device at the moment of signal amplification could result really competitive. Moreover, their high mobility, which preserves the InGaAs crystal properties at its best within the device structure thanks to the 2DEG, will allow to operate the device with extremely low power.

6.3 Outlook for future research

Most likely, throughout this whole work, the study on the satellite valleys in Indium-Gallium Arsenide has been the most unexpected and original part. Though, due to the novelty of the work and its complexity, there is a lot to further study. Particularly, as shown in the second half of the chapter on HEMT devices, quantitative mobility spectrum analysis is needed to differentiate in between conducting carriers originating from different valleys. Moreover, a more complete study has to be carried out concerning the potential X valley coming into play.

If those two studies, would assess firmly the presence of carriers from the satellite valleys, a study on how they influence noise and a reformulation of the so-far used models (such as Lambert) would further be needed.

Finally, we were left with two unanswered questions: the lower noise level of HEMTs at deep cryogenic temperatures and the very good heat dissipation that seemed to surpass even bulk silicon. Therefore special modeling in the noise and heat conduction of InGaAs devices will be needed.

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List of Symbols

T	Temperature
I_d	Drain current
I_g	Gate current
I_s	Source current
I_b	Bulk (or back) current
V_d	Drain voltage (bias)
V_g	Gate voltage (bias)
V_s	Source voltage (bias)
V_b	Bulk (or back) voltage (bias)
C_{ox}	Oxide capacitance
C_{gc}	Gate-to-channel capacitace (exceptionally, also C_{ch})
Q_i	Inversion charge (in the channel)
v_{sat}	Saturation velocity
σ	conductivity
μ_0	Low-field mobility
μ_{eff}	Effective mobility
μ_{MR}	Magnetoresistance mobility
μ_{ph}	Phonon-scattering-limited mobility
μ_C	Coulomb-scattering-limited mobility
μ_N	Neutral-impurities-scattering-limited mobility
μ_{SR}	Surface-roughness-scattering-limited mobility
Y	Y function
Y'	Corrected Y function
LW	Lambert-W function
g_m	transconductance
g_d	output conductance
G_m	Peak of the transconductance g_m
β	MOSFET gain factor
η	Subthreshold slope ideality factor
SW	Subthreshold swing
V_t	Threshold voltage
V_{FB}	Flat-band voltage
V_{GS}	Gate-to-Source voltage
V_{GD}	Gate-to-Drain voltage
E_F	Fermi energy level
E_V	Valence band energy level
E_C	Conduction band energy level
E_g	Energy gap of the bandstructure

E_A	Energy level of the bottom of a generic conduction valley A (Γ, L, X)
CB	Conduction band
VB	Valence band
DOS	Density of states
q	Electron charge
m_d^*	DOS effective mass
$\hbar$	Reduced Plank constant
k_B	Boltzmann constant
k_BT	Thermal voltage
L_g	Gate (channel) length (also L_{ch})
W_g	Gate (channel) width (also W_{ch})
θ	Mobility attenuation factor (generalized)
Θ_{eff}	Effective Mobility attenuation factor (assuming different orders of V_g-dependence)
θ_1	1st-order mobility attenuation factor
θ_2	2nd-order mobility attenuation factor
n	Mobility-law power exponent
R_{SD}	Source-to-Drain resistance
PSD	(Noise) power spectral density
S_{I_D}	PSD of the Drain current (also S_{I_d} or S_{Id})
f	frequency
$S_{V_{fb}}$	Flat-band voltage PSD
$S_{R_{SD}}$	PSD R_{SD}
N_{st}	Surface trap density
CNF	Carrier number fluctuation (model)
CMF	Correlated mobility fluctuation (model)

List of Publications

Journal publications

F. Serra di Santa Maria et al. “Lambert-W function-based parameter extraction for FDSOI MOSFETs down to deep cryogenic temperatures”. In: *Solid-State Electronics* 186 (Dec. 2021), p. 108175. ISSN: 00381101. DOI: 10.1016/j.sse.2021.108175

F. Serra di Santa Maria et al. “Comprehensive Kubo-Greenwood modelling of FDSOI MOS devices down to deep cryogenic temperatures”. In: *Solid-State Electronics* 192 (June 2022), p. 108271. ISSN: 00381101. DOI: 10.1016/j.sse.2022.108271

Conferences

F. Serra Di Santa Maria et al. “Low temperature behavior of FD-SOI MOSFETs from micro- to nano-meter channel lengths”. In: IEEE, Apr. 2021, pp. 1–4. ISBN: 978-1-7281-9306-9. DOI: 10.1109/WOLTE49037.2021.9555451

Francesco Serra Di Santa Maria et al. “In-depth electrical characterization of deca-nanometer InGaAs MOSFET down to cryogenic temperatures for low-power quantum applications”. In: vol. 2022-September. IEEE, Sept. 2022, pp. 257–260. ISBN: 978-1-6654-8497-8. DOI: 10.1109/ESSDERC55479.2022.9947142. URL: https://ieeexplore.ieee.org/document/9947142/

F. Serra Di Santa Maria et al. “Experimental Study of Self-Heating Effect in InGaAs HEMTs for Quantum Technologies Down to 10K”. in: IEEE, Mar. 2023, pp. 1–4. ISBN: 978-1-6654-5672-2. DOI: 10.1109/IRPS48203.2023.10118294

Co-authorship

G. Ghibaudo et al. “Modelling of self-heating effect in FDSOI and bulk MOSFETs operated in deep cryogenic conditions”. In: *Solid-State Electronics* 192 (June 2022), p. 108265. ISSN: 00381101. DOI: 10.1016/j.sse.2022.108265. URL: https://linkinghub.elsevier.com/retrieve/pii/S0038110122000375

M. Cassé et al. “FDSOI for cryoCMOS electronics: device characterization towards compact model”. In: *2022 International Electron Devices Meeting (IEDM)*. 2022, pp. 34.6.1–34.6.4. DOI: 10.1109/IEDM45625.2022.10019322