Switched-mode power supply impact on a Bluetooth Low Energy receiver inside a microcontroller

Pierre Malbec

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Pour obtenir le grade de

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Impact des pollutions d'une alimentation à découpage sur un récepteur Bluetooth Low Energy au sein d'un microcontrôleur

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Impact des pollutions d'une alimentation à découpage sur un récepteur Bluetooth Low Energy au sein d'un microcontrôleur

Résumé

Mots clés *– interférence électromagnétique, conversion de puissance, transmission sans fil, microcontrôleurs, circuits intégrés CMOS, modélisation système.*

Avec la croissance du marché de l'internet des objets, la demande de microcontrôleurs basse consommation intégrant également des solutions de transmission sans fil augmente constamment. À cet égard, STMicroelectronics a développé un microcontrôleur qui intègre un convertisseur DC/DC à haut rendement (une alimentation à découpage (SMPS)) ainsi qu'un transceiver Bluetooth Low Energy (BLE). Un problème a été identifié sur ce produit. Lorsque le SMPS est activé pour réduire la consommation d'énergie, une diminution des performances du récepteur BLE peut être mesurée ; sa sensibilité est dégradée.

L'objectif de la thèse est d'identifier, comprendre, décrire et quantifier les mécanismes de bruit induits par le SMPS et causant la perte de sensibilité du récepteur. L'objectif est de donner une vue d'ensemble de la question concernant l'impact des interférences électromagnétiques sur le récepteur RF et de proposer des directives ou des solutions assurant la cohabitation à l'intérieur d'un unique système sur puce, d'un convertisseur de puissance non linéaire et d'une solution de connectivité sans fil. Assurer le bon fonctionnement de ces deux fonctions au sein du microcontrôleur est essentiel pour le marché ciblé.

Différentes approches ont été utilisées pour mener ces travaux. La méthodologie consiste en l'utilisation combinée de l'analyse théorique des phénomènes en jeu, de la simulation électrique niveau transistor et de la mesure de la propagation des interférences ou des performances du récepteur. L'objectif est de comprendre les mécanismes liés à la génération d'interférences et les facteurs déterminant leur contenu spectral. Un autre aspect de ce travail comprend une approche novatrice visant à élaborer un modèle haut niveau du système permettant la simulation de la sensibilité du récepteur en présence d'interférences. Le développement est basé sur les simulations électriques et vise à identifier les chemins de propagation des interférences ou les défauts de conception du récepteur.

L'analyse de la génération et de la propagation d'interférences révèle une résonance critique, provoquant une dégradation de la sensibilité du récepteur. L'identification des éléments parasites définissant sa fréquence fournit un moyen de réduire l'impact du SMPS sur les performances du récepteur. La simulation de la sensibilité du récepteur par le modèle haut niveau indique un fort impact des interférences via un terminal spécifique du circuit du récepteur. Il met en évidence un défaut dans la conception du transceiver BLE et apporte des leviers d'actions pour améliorer sa robustesse face aux interférences.

La thèse propose une analyse approfondie des interférences générées par le SMPS, de leur propagation et de leur impact sur le récepteur BLE. Les résultats peuvent être extrapolés pour la résolution de problèmes liés à l'intégration dans un circuit intégré de tout convertisseur de puissance non linéaire et de toute solution de connectivité sans fil.

Switched-mode power supply impact on a Bluetooth Low Energy receiver inside a microcontroller

Abstract

Keywords *– electromagnetic interference, power conversion, wireless communication, microcontrollers, CMOS integrated circuits, system modeling.*

With the growth of the internet of things market, the demand for low-power general-purpose microcontrollers that also integrate wireless connectivity solutions is constantly increasing. In this regard, STMicroelectronics developed a microcontroller that integrates a high-efficiency DC/DC converter (a switched-mode power supply (SMPS)) as well as a Bluetooth Low Energy (BLE) transceiver. An issue has been identified with this product. When the SMPS is enabled to reduce power consumption, a decrease in the performance of the BLE receiver can be measured; its sensitivity is degraded.

The objective of this work is to identify, understand, describe, and quantify the noise mechanisms induced by the activity of the SMPS that cause the sensitivity loss in the BLE receiver. The aim is to give a good overview of the issue regarding electromagnetic interference impact on the RF receiver and propose guidelines or solutions to ensure cohabitation inside a unique system-on-chip of a non-linear DC/DC power converter and a wireless connectivity solution. Ensuring the correct operation of the SMPS and the BLE receiver within the microcontroller is critical for the targeted market.

Different approaches were used to conduct this research. The methodology consists of the combined utilization of theoretical analysis of occurring phenomena, transistor-level electrical circuit simulation of the system, and measurement of interference propagation and receiver performance. The goal is to understand the mechanisms linked to interference generation and the factors that determine their spectral content. Another aspect of this work includes an innovative approach intended to develop a high-level model of the system that allows the simulation of receiver sensitivity in the presence of interference. The development of the model is based on circuit simulation and aims to identify interference propagation paths towards the BLE receiver or flaws in its design.

The analysis of interference generation and propagation reveals a critical resonance, causing a degradation of the BLE receiver sensitivity. The identification of the parasitic elements that define its frequency provides a way to reduce the impact of the SMPS on the receiver performance by shaping the interference. The simulation of the receiver sensitivity by the high-level model indicates a strong impact of the interference via a specific terminal of the receiver analog circuitry. It highlights a flaw in the BLE transceiver design and introduces a lever to improve its robustness against interference.

The thesis proposes a deep analysis of interference generation by the SMPS, their propagation towards the BLE receiver, and their impact on its performances. The results can be extrapolated to help understand issues with the integration in a single integrated circuit of any non-linear DC/DC power converter or any wireless connectivity solution.

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Introduction 1

This PhD thesis was conducted in collaboration with the research laboratories TIMA[1], Laboratoire Ampère[2] and G2Elab[3]. It was carried out through a partnership with STMicroelectronics[4], a European semiconductor contract manufacturing and design company and funded by the association nationale de la recherche et de la technologie (ANRT).

1.1 Context

STMicroelectronics is one of the leaders in the development of general-purpose microcontrollers. A microcontroller is a small computer on a single integrated circuit (IC) chip that contains one or more central processing units (CPU) along with volatile and non-volatile memories and programmable input/output (I/O) peripherals. Nowadays, with the growth of the Internet of Things (IoT) market [1], the demand for general-purpose microcontrollers that also integrate wireless connectivity solutions is constantly increasing.

In this regard, STMicroelectronics designed a 32-bit microcontroller embedding a Bluetooth Low Energy (BLE) transceiver: the STM32WB55 [2]. It is commercialized since 2019 and available in four different packages. Figure 1.1(a) shows the microcontroller encapsulated inside a 48-pin QFN package. The IC is manufactured using a 90 nm CMOS process. The microcontroller contains two CPUs and their associated static random access memories (SRAM), as well as flash memories and peripherals. As for the range of general purpose microcontroller, the STM32WB55 integrates power management solution designed to reduce as much as possible the power consumption. This feature is critical for microcontroller intended to be used with IoT products, often portable and battery powered. The solution is based on a high-efficiency DC/DC power converter, a switched-mode power supply (SMPS) lowering the input voltage thanks to the fast switching of two power metal-oxide-semiconductor field-effect transistors (MOSFET). A diagram of the main functions integrated inside the microcontroller is presented in Figure 1.1(b).

An issue has been identified on the STM32WB55. When the SMPS is enabled to lower the microcontroller power consumption, a decrease in the performance of the receiver can be measured. The sensitivity of the BLE receiver is degraded by the activity of the SMPS. Sensitivity is one of the main characteristics defining the performance of a radio frequency (RF) receiver. It represents the smallest signal power that a receiver can detect correctly.

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[2]Laboratoire Ampère – Ecole Centrale Lyon, INSA Lyon, UCBL, CNRS – Lyon, France

[3]G2Elab – Université Grenoble Alpes, Grenoble INP, CNRS – Grenoble, France

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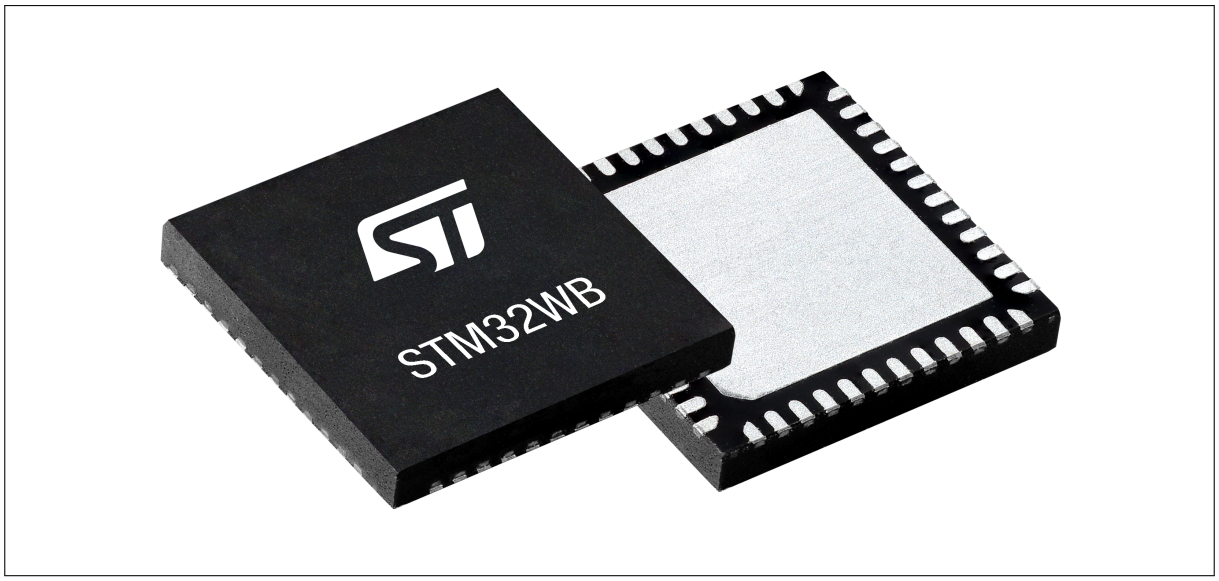

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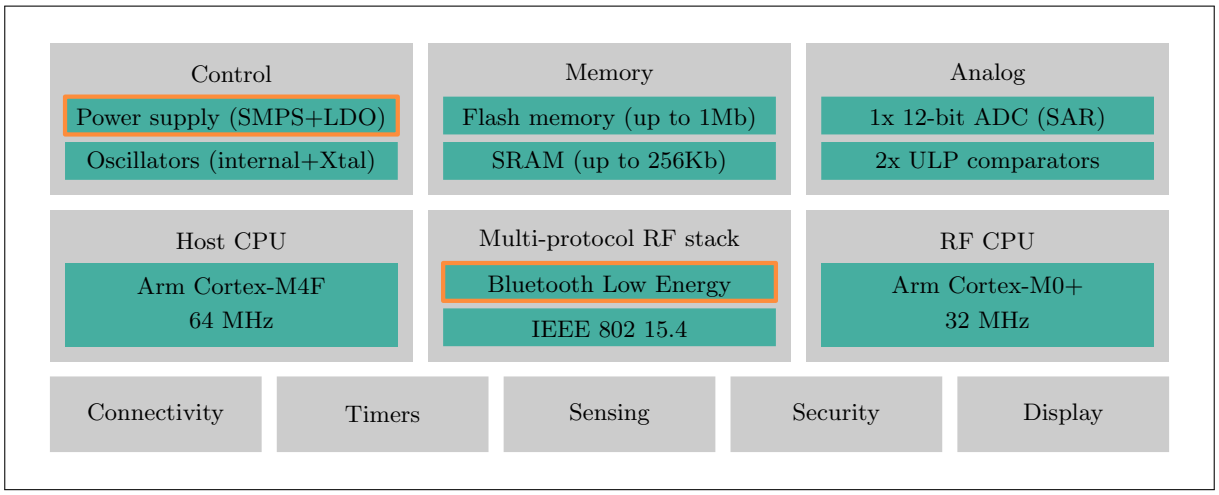


(b)

Figure 1.1: (a) The microcontroller IC encapsulated inside its package and (b) a simplified diagram of the STM32WB55 architecture.

As the microcontroller is intended for IoT products, usually battery-powered, ensuring the correct operation of the SMPS within the system to limit power consumption is critical. The objective of the thesis is to identify, understand, describe, and quantify the noise mechanisms induced by the activity of the SMPS that cause the sensitivity loss in the BLE receiver.

The STM32WB55 microcontroller

The STM32WB55 embeds a BLE and an 802.15.4 RF subsystem that interfaces with a generic microcontroller subsystem using an Arm Cortex-M4F CPU on which the host application resides. The RF subsystem is composed of an RF analog front end, BLE and 802.15.4 digital MAC blocks as well as a dedicated Arm Cortex-M0+ CPU, plus proprietary peripherals. The RF subsystem performs all of the BLE and 802.15.4 low layer stack, reducing the interaction with the Host CPU to high level exchanges. Some

functions are shared between the Host CPU and the RF subsystem CPU: flash memories, SRAMs, security peripherals, reset and clock control, and power control. A set of power-saving modes enables the design of low-power applications. The STM32WB55 offer four packages, from 48 to 129 pins: two quad-flat no-leads (QFN) packages, a wafer-level chip-scale package (WLCSP) and a ball grid array (BGA) package.

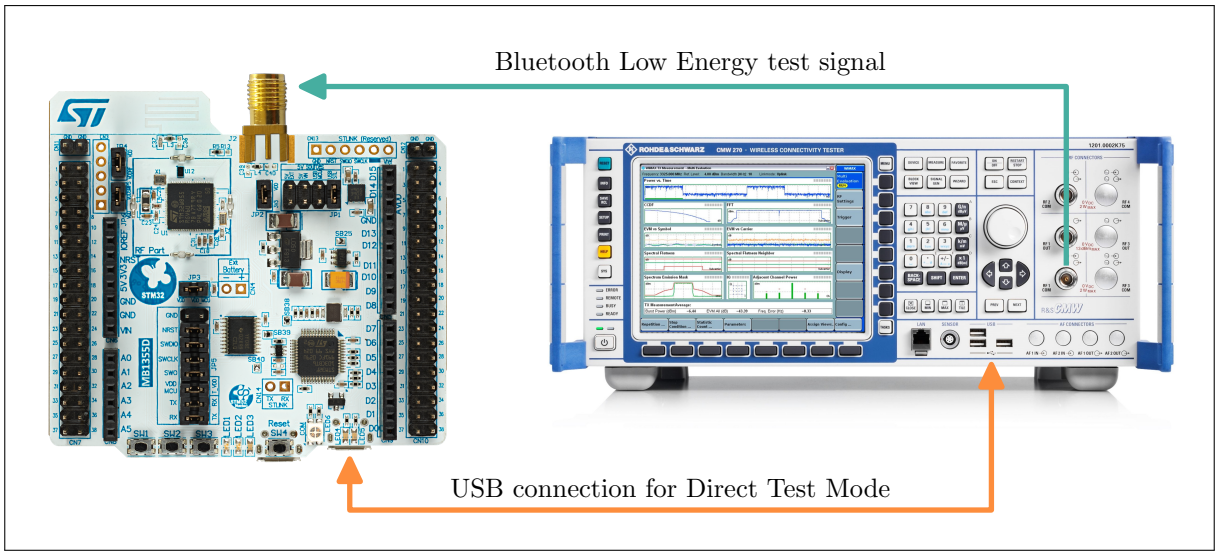
Power supply management: The STM32WB55 operates from a 1.71 V to 3.6 V power supply, and can be powered by a battery or a button cell. The device integrate an SMPS to improve low power performance when the V_{DD} voltage is high enough (comprised between 2.0 V and 3.6 V). This converter has an intelligent mode that automatically enters in bypass mode when the V_{DD} voltage falls below a user defined voltage. The device can be operated without the SMPS by just wiring its output to V_{DD}. This is the case for applications where the voltage is low, or where the power consumption is not critical. The SMPS can also be switched on or set in bypass mode at any time by the application software. More details are provided in 2.

RF subsystem: The STM32WB55 embeds an ultra-low power multi-standard radio BLE and 802.15.4 network processor, compliant with Bluetooth specification 5.3 and IEEE 802.15.4-2011. The BLE features 1 Mbps and 2 Mbps transfer rates. The BLE stack and 802.15.4 Low Level layer run on an embedded Arm Cortex-M0+ core. The stack is stored on the embedded flash memory, which is also shared with the Arm Cortex-M4 application. The RF front-end is based on a direct modulation of the carrier in the transmitter (Tx), and uses a low IF architecture in receiver (Rx) mode. Thanks to an internal transformer at RF pins, the circuit directly interfaces the antenna (single ended connection, impedance close to 50 Ω). The natural bandpass behaviour of the internal transformer, simplifies outside circuitry aimed for harmonic filtering and out of band interferer rejection. In receive mode the circuit can be used in standard high performance or in reduced power consumption (user programmable). The Automatic gain control (AGC) is able to reduce the chain gain at both RF and IF locations, for optimized interference rejection. Thanks to the use of complex filtering and highly accurate I/Q architecture, high sensitivity and excellent linearity can be achieved. The radio frequency source is synthesized form an external 32 MHz crystal. More details are provided in 3 and 4.

Issue on the microcontroller

Figure 1.2(a) shows the experimental setup used to measure the sensitivity of the BLE receiver embedded within the microcontroller. The sensitivity is the minimum signal power that the receiver can detect with "acceptable quality" and is defined precisely in 3.1.2. This example of measurement was performed on a development board integrating the STM32WB55 and commercialized by STMicroelectronics, the Nucleo-WB55RG. The microcontroller is configured to use a test mode defined by the BLE standard [3], called *direct test mode*, allowing a specialized tester to characterize the performances of the BLE transceiver. The sensitivity measurement procedure is presented with more details in 3.2.3.

Figure 1.2(b) shows a result of sensitivity measurements realized on the Nucleo-WB55RG test board. The BLE standard (presented in 3.1.1) uses 40 channels of 2 MHz bandwidth spanning from 2402 MHz to 2480 MHz. The integrated SMPS (presented in 2.1.2) is working at a frequency of 4 MHz and can be enabled or disabled at any time by



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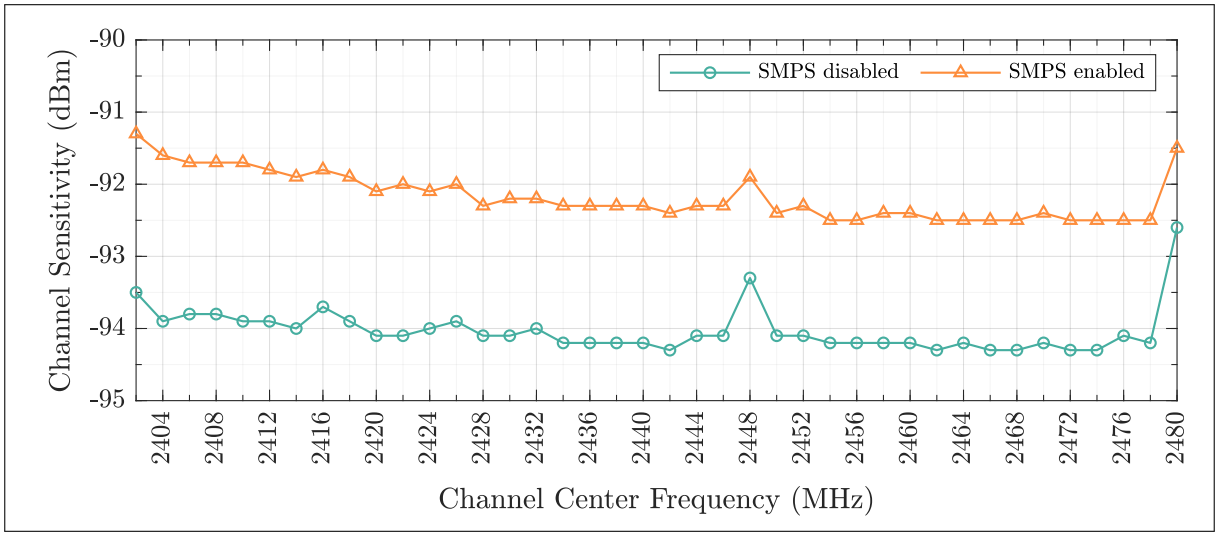


(b)

Figure 1.2: (a) BLE receiver sensitivity measurement setup and (b) measurement showing the sensitivity loss due to the SMPS.

writing in the dedicated register of the microcontroller memory. The sensitivity is measured for each of the 40 channels, with the SMPS enabled or disabled. The measurement reveals a loss in the BLE receiver sensitivity of approximately 2 dB when the SMPS is enabled, for this specific test board.

The issue measured on this test board is minor (only a few dB of loss on the sensitivity) and the integrated BLE receiver still exhibits good performances when the SMPS is activated. The BLE standard specifies that devices must be able to achieve a minimum receiver sensitivity of only -70 dBm [3]. However, this criteria is a major selling point used by the competition to define the performance of a BLE receiver, and so, achieving the best sensitivity is a critical concern. In addition, the underlying phenomena causing the sensitivity loss are not entirely understood and the issue could be more significant in a different system, making this study relevant:

- The spectral content of the electromagnetic interference (EMI) produced by the SMPS and causing the sensitivity loss in the BLE receiver should be impacted by elements in the system: IC package, printed circuit board (PCB), external components... Variations in the EMI spectral content can possibly give a different impact on the receiver performances.
- The minimum sensitivity the receiver must achieve is defined by the wireless standard employed, in our case, −70 dBm for the BLE standard. Some standards require a higher minimum sensitivity. For example, the GSM[5] standard specifies a minimum receiver sensitivity of −102 dBm and W-CDMA[6] specifies a minimum of −107 dBm [4]. Considering the same EMI amplitude and a received signal close to their respective sensitivity, the impact of the SMPS would be greater for these standards.
- The SMPS is powering the whole microcontroller (CPUs, memories, RF subsystem, etc.); the current load on its output depends on the microcontroller power consumption. The STM32WB55 studied here is a low-power microcontroller consuming only 10 mA to 20 mA (typical value). However, the BLE subsystem could be integrated into a high-performance microcontroller, or the microcontroller could integrate another wireless standard (e.g., Wi-Fi with Rx consumption 10 times higher [5]). A higher current load at the SMPS output generates a higher amplitude EMI [6] and, therefore, a more significant impact on the integrated receiver.

Depending on the application scenario, the adverse effects of EMI generated by the SMPS on an RF subsystem may be more problematic and must therefore be thoroughly understood.

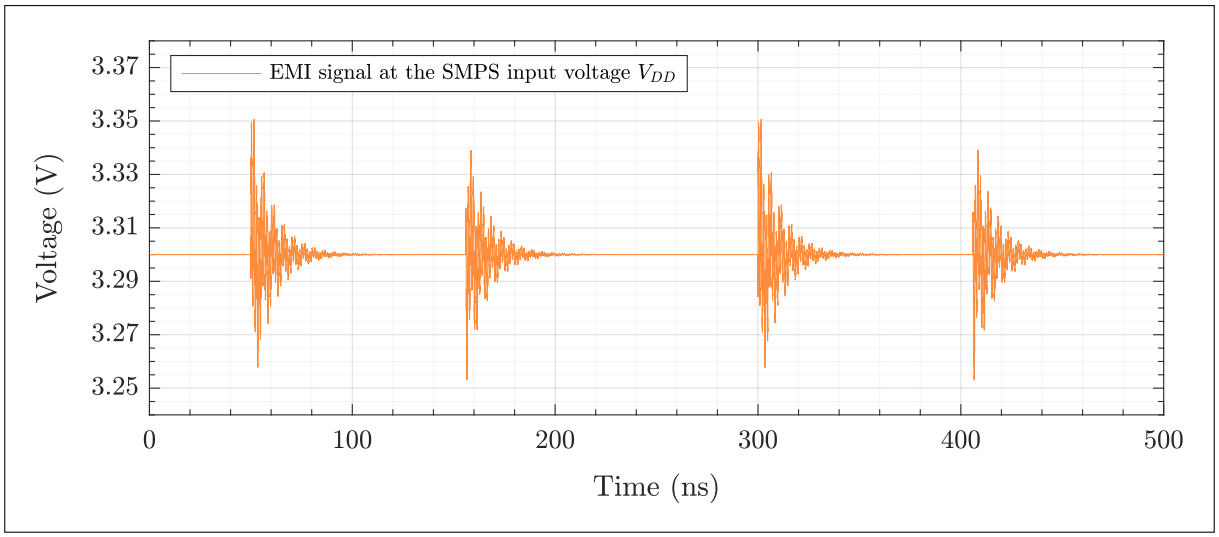
1.2 Research problem

The sensitivity measurements demonstrates the direct implication of the SMPS in the degradation of the BLE receiver performances. The SMPS is functioning at a frequency of 4 MHz. The abrupt switching of the transistors at this frequency generates resonating pulse signals (voltage overshoot/undershoot) at the SMPS input and output voltage nodes. The corresponding EMI spectrum contains the fundamental frequency at 4 MHz and its harmonics spanning over a wide range and resonating at certain frequencies depending of the system itself. Figure 1.3 plots an example of EMI generated at the SMPS input V_{DD} and its associated spectrum.

Figure 1.4 depicts a simple representation of the BLE receiver demodulation chain. The modulated BLE signal located between 2.40 GHz and 2.48 GHz is sensed by the receiver antenna and processed by a low noise amplifying stage. The wanted signal is located almost three decades above the SMPS switching frequency (4 MHz). The harmonics 600 to 620 of the 4 MHz pulse signal are falling in the BLE band, and could degrade the wanted signal if present at a significant level. Transposing this observation to 'classic' discrete power electronic devices, it means that a DC/DC power converter switching at a frequency of 20 kHz could generate unwanted noise until 12 MHz. This is quite possible

[5]Global System for Mobile Communications, a standard used in mobile telecommunications for voice and data transmission.

[6]Wideband Code-Division Multiple Access, a standard found in 3G mobile telecommunications allowing higher data rate transmission than GSM.



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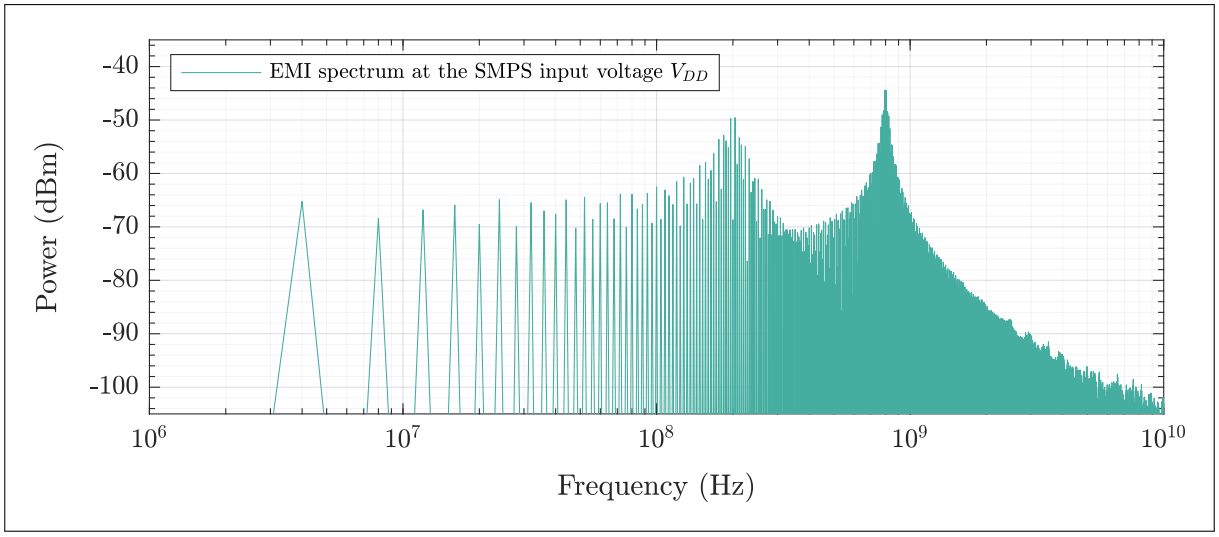


(b)

Figure 1.3: Representation of EMI generated by the SMPS at its input voltage V_{DD} (a) in the time domain and (b) in the frequency domain.

[7–9]. The BLE signal is then down-converted to an intermediate frequency at 1.6 MHz. The wanted signal is now located below the SMPS switching frequency. Unwanted noise below the 4 MHz fundamental could be present, due to non-linear phenomena such as inter-modulation [4]. After that, the analog signal is converted to the digital domain for further processing, and should be immune from EMI. The architecture of the BLE transceiver is detailed in 4.1.

How exactly the SMPS degrades the BLE signal and affects the receiver sensitivity? The global aim of this work is to give a good overview of an existing issue regarding EMI impact on a RF receiver and propose guidelines or solutions to ensure the cohabitation inside a unique system-on-chip (SoC) of a non-linear DC/DC power converter and a wireless connectivity solution. The objectives of the study are:

- To identify different phenomena causing EMI generation by the activity of the SMPS as well as the main elements of the system associated with each phenomenon.

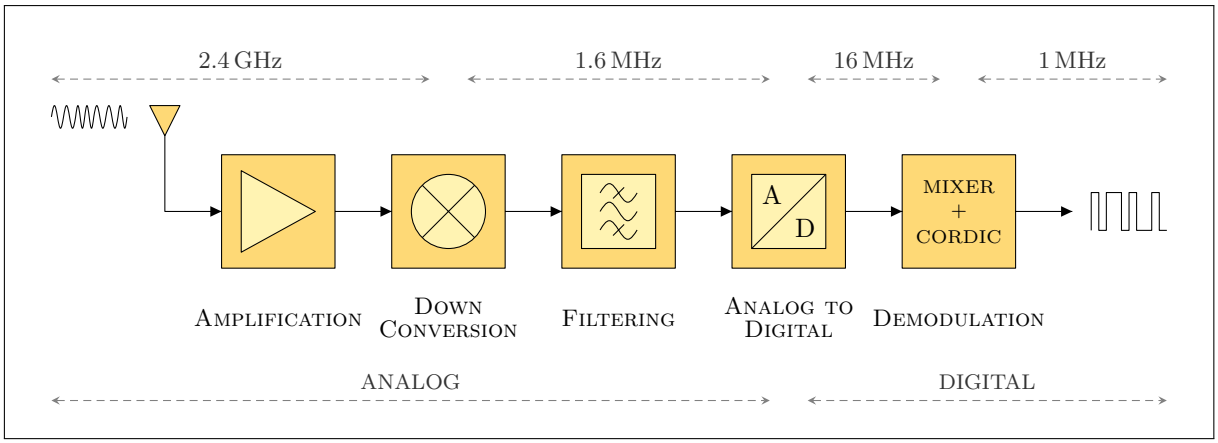


Figure 1.4: Simplified representation of the full BLE receiver demodulation chain.

- To understand how different elements can affect the spectral content of EMI generated by the SMPS, for each of the phenomena.
- To describe the propagation of EMI from the SMPS to the BLE receiver, as well as the propagation inside of the receiver analog circuitry.
- To quantify the impact of EMI on a specific sub-circuit of the BLE receiver, or for a specific propagation path.

The goal of this thesis is not to design a new architecture for the SMPS or the BLE receiver but to fully understand how EMI present in the system affects the BLE receiver performances. This work aims to give a good understanding of issue, helping taking the right decision when designing an IC or a PCB. The hypothesis is made that degradation of the BLE signal happens in the analog circuitry of the receiver. The impact of EMI will be studied on the BLE receiver from its RF input on the PCB (the antenna or in our case, the SMA connector) until its analog-to-digital converter (ADC) input. After that, the effect of EMI on the digital signal is considered negligible.

1.3 Methodology

This section first describes the methods selected to address the research questions. Available resources and their usage are presented here. Then, the outline for the rest of this document is detailed. It is made of three distinct chapters and a conclusion.

Resources and methods

Different resources allowing circuit simulation of the microcontroller IC, and measurements of EMI in the studied system as well as their impact on the BLE receiver are presented. The chosen method and associated tools to further analyze and obtain a deeper understanding of the research problem is also detailed.

Transistor-level electrical simulation of the system

The power stage, the BLE receiver, and their environment can be simulated precisely using a SPICE circuit simulator (Spectre by Cadence). The simulation test bench is made of:

- The transistor-level schematic of the SMPS power stage and its associated drivers from which the IC fabrication masks are issued for the STM32WB55. The transistor models are provided by the IC manufacturer ;
- The transistor-level schematic of the BLE receiver analog circuitry, also from which the fabrication masks are issued ;
- An RLCG model of the 68-pin QFN package inside which the STM32WB55 is encapsulated. The package model is coming from a 3D extraction realized with Ansys Q3D ;
- Parasitic models of the SMPS and BLE transceiver external components mounted on the PCB. The models are provided by the manufacturers ;
- A simple RL model of the PCB traces and vias. The values are calculated based on dimensions and PCB characteristics.

Transistor-level electrical simulations of the system, using precise models, greatly helps the understanding of interference related phenomena and are used for two main objectives. The first one is the analysis the different mechanisms behind the generation of EMI by the SMPS, and the identification of key parasitic elements implied in the interference resonances. The second usage one is the analysis of interference propagation inside the receiver, affecting the BLE signal.

Measurements on the system

For the purposes of validating simulation results and demonstrating the effect of the SMPS on the receiver, two types of measurements are conducted:

- The spectral analysis of conducted EMI on the PCB, used to confirm the presence of expected resonances in the interference and validate the circuit simulation results. These measurements are performed at the SMPS input and output voltages using a test board designed for the thesis.
- The measurement of the BLE receiver sensitivity depending on the SMPS activity and operating conditions showing the direct implication of the SMPS in the degradation of the sensitivity. The sensitivity can be determined for each of the 40 BLE channels using a specialized tester.

Non-intrusive measurement of RF signals inside the BLE receiver, inside the microcontroller, is feasible but complex to implement and the resources where not available for this thesis.

High-level modeling of the system

The observable issue is the BLE receiver performance degradation by the SMPS activity, measurable at system-level. What is happening inside the analog circuitry of the BLE receiver to explain it?

On one hand, sensitivity measurements present a limited interest to understand how the BLE signal is degraded by the interference through the analog circuitry of the receiver. On the other hand, transistor-level simulations don't reflect directly the impact of EMI at system level, on the sensitivity. As more advance measurements methods where not available for this thesis, new simulation tools are required to push further the investigation on this problem.

What if we want to use the transistor-level model of the system to simulate the sensitivity? To simulate its sensitivity, the whole receiver need to be simulated: from the received RF signal until the data bits retrieved by the digital demodulator. To observe the impact of the SMPS, it needs to be simulated as well. To obtain the sensitivity, the whole system needs to run for hundreds of milliseconds[7], and for several iteration (until the sensitivity is reached). Yet, the degradation of the signal may happen at the front end of the receiver dealing with high frequency signals located close to 2.5 GHz. It leads to complex circuit to simulate and a high number of simulation points[8].

Consequently, one goal of the thesis is to develop a high-level model of the system, allowing the simulation of the receiver sensitivity in presence of EMI generated by the SMPS, with acceptable simulation time. The model is designed using Matlab Simulink, and built based on transistor-level circuit simulation of the system. The model aims to identify critical interference propagation paths towards the BLE receiver or flaws in its design, leading to a degradation of the sensitivity.

Thesis outline

The outline of the thesis for the chapters following this introduction is detailed below.

First, the focus is made on mechanisms correlated with EMI generation and their spectral content. The power supply scheme in the microcontroller is described explaining the importance of successfully integrating the SMPS inside the IC. The SMPS operation and its environment are described. Parasitic elements playing a role in EMI spectral content are presented and calculated for the studied system. Interference resonances caused by different phenomena are detailed and their expected frequency determined.

Next, spectral analyses of conducted EMI measured on the PCB are presented validating the theoretical prediction of resonant frequencies. Shifting of a problematic resonant frequency is done by swapping external passive components. Radiated EMI are also measured, showing the wide spectrum of radiated EMI caused by the SMPS and the sources of these radiated EMI. Measurements exhibiting the degradation of the sensitivity, linked to SMPS activity and operating conditions are provided. The correlated measurements of EMI spectra and receiver sensitivity demonstrates the importance of considering the system resonant frequencies location. Guidelines to limit unwanted interference in a specific frequency band are given in this chapter.

Then, the methodology employed to develop the high-level model of the system is described. Results of the simulated receiver sensitivity are displayed and identified issues on the BLE receiver design are presented. Options to improve the BLE receiver integrity regarding EMI are given here.

Finally, the conclusion chapter details the main results obtained during this work and draws perspectives for a deeper analysis of this research problem.

[7]The receiver sensitivity is defined for a bit error rate of 0.1 % (one wrong data bit every thousand bits). For statistically significant results (enough significant figures), 100,000 bits need to be demodulated. This corresponds to 100 ms at a data rate of 1 Mb/s and a maximum of 100 tolerated errors.

[8]A signal at 2.5 GHz corresponds to a period of 400 ps. Considering a simulation time step ten times smaller to clearly defined the signals gives a time step of 40 ps. As the whole system needs to be simulated for at least 10 ms, it gives 250 millions simulation points.

Electromagnetic interference generation

2

This chapter focuses on the analysis of EMI produced by the SMPS: how are they generated and what defined their frequency content?

First, the power distribution of the studied microcontroller and the integrated SMPS are presented. Next, the different parasitic elements of the system and the associated mechanisms implied in EMI generation are detailed. Finally, the most important aspects regarding the research problem are summarized and discussed.

2.1 Power supply scheme and environment

This section describes the power supply distribution used in the studied microcontroller, showing the benefits of using an SMPS. Also, the architecture and operation of the implemented SMPS is detailed and its main characteristics are presented.

2.1.1 Power distribution

A diagram of the microcontroller power distribution is depicted in Figure 2.1. The microcontroller is powered by an external power source V_{DD} between 1.71 V and 3.6 V. The external source is either a DC power supply or a battery. A main regulator consisting of a single low-dropout (LDO) regulator is providing the 1.2 V supply for the digital part of the microcontroller. An RF regulator, consisting of six different LDO regulators, is providing the 1.2 V supplies for the BLE transceiver.

The microcontroller integrates also an SMPS to reduce the power consumption. The system can be operated with the SMPS enabled or disabled. When the SMPS is enabled, it is providing the input voltage for every LDO regulators, by converting the main supply V_{DD} to a voltage V_{SMPS} between 1.2 V and 1.95 V. When the SMPS is disabled, the node V_{LX} is tied to V_{DD} and the LDO regulators convert directly the main supply V_{DD} to generate the digital domain and the RF domain supplies. These two supply strategies are sum up in Table 2.1.

Why integrating a SMPS?

LDO regulators are a simple way to regulate an output voltage powered from a higher-voltage input. Figure 2.2 displays the architecture of the LDO regulators integrated inside the microcontroller. The output voltage is

$$V_{OUT} = V_{REF} * (1 + R_1/R_2) \tag{2.1}$$

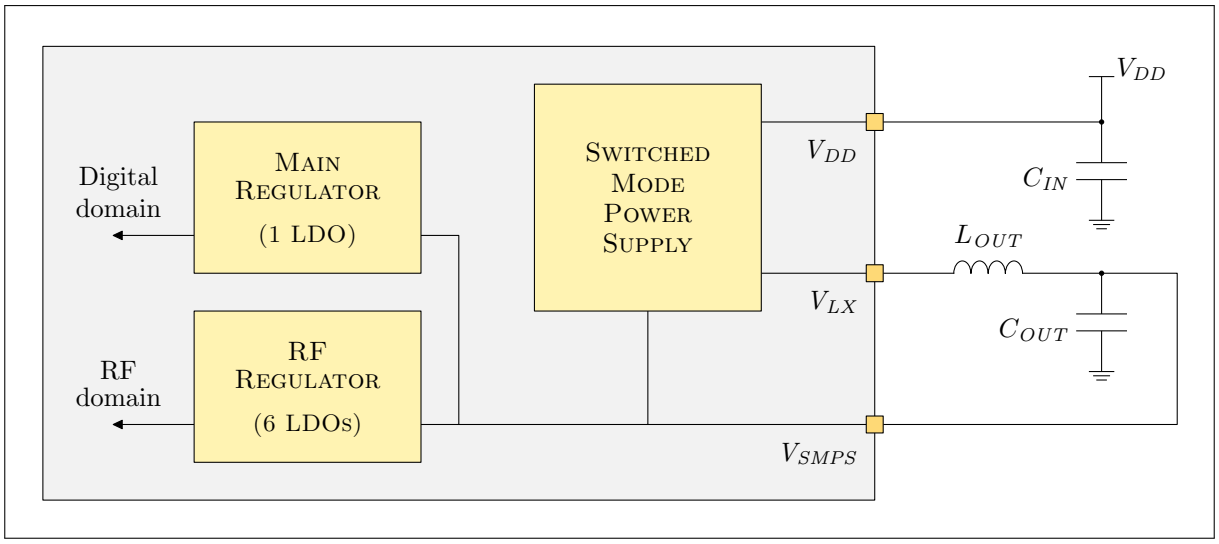


Figure 2.1: Microcontroller power distribution diagram. The power management unit generates the necessary supplies for the digital and the RF domains.

and is maintained at a constant value by regulating the output current I_{OUT} depending on the load demand (control of the MOS gate potential). LDO regulators are linear DC/DC converters, and therefore have a low noise contribution compared to non-linear DC/DC converters like SMPS (no switching). However, they display a lower conversion efficiency than SMPS, especially when the input voltage is far off from the desired output voltage. The theoretical efficiency for an ideal LDO regulator is plotted in Figure 2.2 and is given by:

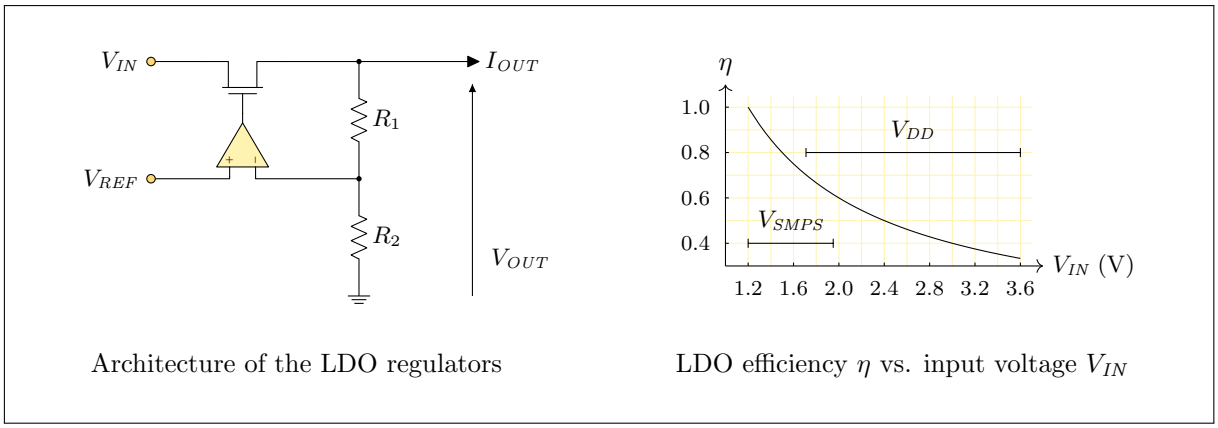
$$\eta = P_{out}/P_{in} = V_{out}/V_{in}. \tag{2.2}$$

When the SMPS is disabled, the LDO regulators input voltage is directly the main power supply V_{DD} ranging from 1.71 V to 3.6 V, giving an ideal efficiency of 70 % at best and 33 % in the worst case. If the main power supply is at its typical value $V_{DD} = 3.3$ V, the LDO regulators ideal efficiency is only 36 %. Moreover, for large voltage drops, the equivalent resistance of the LDO regulator MOSFET is high and generates important power losses by Joule heating process, causing thermal dissipation issues. For these reasons, the operation of the microcontroller with the LDO regulators only is intended for applications where the voltage is low (below 2.0 V), or if the power consumption is not a major concern.

However, when the the SMPS is enabled and convert first the main power supply to its typical output value $V_{SMPS} = 1.4$ V, the LDO regulators ideal efficiency is around 86 %. Figure 2.3 presents the efficiency of the integrated SMPS as well as the different loss sources. With an input voltage $V_{DD} = 3.3$ V, an output voltage $V_{SMPS} = 1.4$ V and a current load of 10 mA, the efficiency of the SMPS is around 80 % and reach 90 % as the

SMPS enabled				**SMPS disabled**			
LDOs input			LDOs output	LDOs input			LDOs output
min	*typ*	*max*	*typ*	*min*	*typ*	*max*	*typ*
1.2 V	1.4 V	1.95 V	1.2 V	1.71 V	3.3 V	3.6 V	1.2 V

Table 2.1: LDO regulators input and output voltages whether the SMPS is enabled or disabled.



Architecture of the LDO regulators

LDO efficiency η vs. input voltage V_{IN}

Figure 2.2: Architecture of the implemented LDO regulators and their ideal efficiency for the input voltage range.

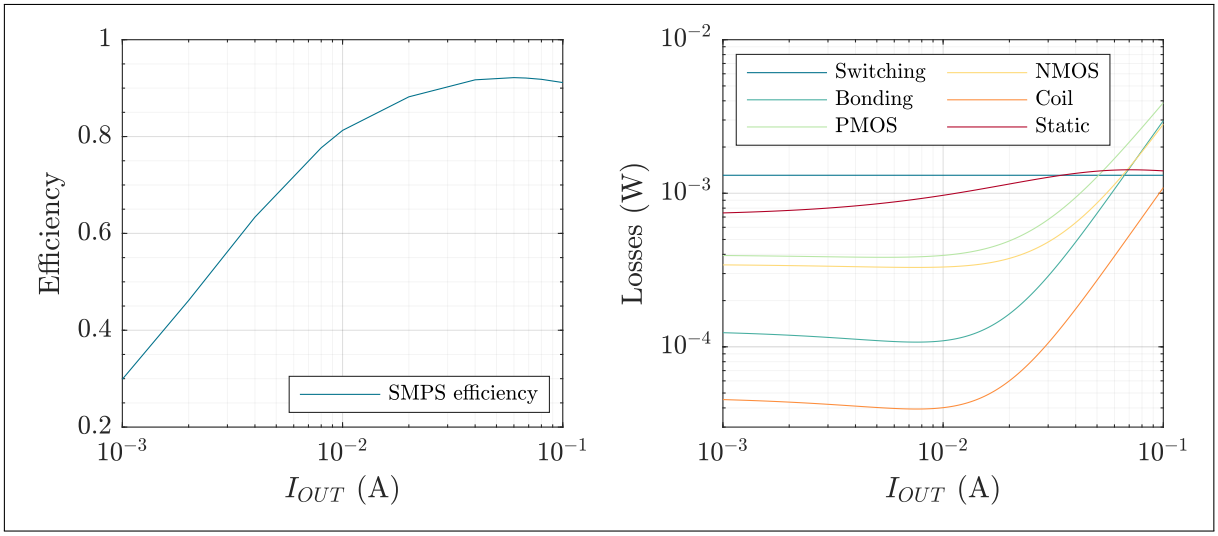


Figure 2.3: Power efficiency of the integrated SMPS versus its output current (left) and the associated losses (right) in typical conditions: V_{DD} = 3.3 V, V_{SMPS} = 1.4 V and f_{SW} = 4 MHz.

current load increase ($\eta > 90\,\%$ for $I_{LOAD} > 30\,\text{mA}$).

Table 2.2 shows the microcontroller power consumption in different operating modes, depending if the SMPS is bypassed or not. We observe a reduction of approximately 40% of the power consumption[1]. The SMPS is designed to work with a current load between 0 and 80 mA, and the SMPS efficiency increases with the current load. For higher current load (e.g. due to higher CPU activity or inputs/outputs power consumption), the benefit of using the SMPS is even greater.

Why a wide voltage supply range?

The microcontroller accepts a voltage supply between 1.71 V and 3.6 V while most of the circuit works under 1.2 V. This creates the need for an efficient DC/DC converter.

[1]The microcontroller power supply V_{DD} is considered at its typical value of 3.3 V in both cases (SMPS bypassed or not). The SMPS allow to reduce the microcontroller current consumption.

The digital circuitry as well as the RF subsystem run under 1.2 V to limit the power consumption of the microcontroller. The STM32WB55 is a general purpose microcontroller, intended to be used in a lot of application cases and therefore needs high power supply compatibility. It is designed to cover as much as possible the normal range of three JEDEC[2] standard defining power supply voltages for digital integrated circuits: the 3.3 V ±0.3 V standard [10], the 2.5 V ±0.2 V standard [11] and the 1.8 V ±0.15 V standard [12]. The targeted range of supply voltage for STM32 microcontroller is 1.65 V to 3.6 V. It also allows the microcontroller to be used with standard button cells.

2.1.2 The Switched-mode power supply

The integrated SMPS is a non-linear DC/DC converter relying on the fast switching of power MOSFETs to achieve high efficiency voltage conversion.

The SMPS is working as a step-down converter (also called 'buck converter') to lower the main power supply, typically at 3.3 V. The output voltage is regulated to a fixed value chosen between 1.2 and 1.95 V. The SMPS had been designed for a maximal current load of 80 mA. The main characteristics are summarized in Table 2.3. The SMPS input is connected to the main supply voltage V_{DD} and its output voltage is noted V_{SMPS}.

The SMPS architecture is depicted in Figure 2.4. Two power MOSFETs are switching at a frequency F_{SW}, letting either the current I^+ or the current I^- flow through L_{OUT}. Therefore, the voltage at V_{LX} node is a pulse wave signal alternating between the input voltage V_{DD} and the ground of the circuit. The duty cycle α of the pulse wave is defined by the MOSFETs control signal. The continuous output voltage V_{SMPS} is obtained by filtering V_{LX} with the second order low-pass filter formed by L_{OUT} and C_{OUT}. At first order[3], the output voltage V_{SMPS} corresponds to the average value of the pulse wave signal V_{LX},

$$V_{SMPS} = \alpha * V_{DD}. \tag{2.3}$$

The output voltage V_{SMPS} is fed back to the SMPS, and a current mode control is used to regulate the current flowing through the inductor L_{OUT}, according to the load. The main ideal voltage and current waveforms are illustrated in Figure 2.5. A non-overlapping

[2]JEDEC Solid State Technology Association, an independent semiconductor engineering trade organization and standardization body developing open standards.

[3]The output voltage DC value is affected by serial resistive losses (power MOSFETs R_{ON}, bonding, package and PCB parasitic resistances, output inductor R_{DC}...) and a small voltage ripple is present (not entirely filtered).

BLE transceiver mode	**SMPS operating mode**	**Consumption**	
Reception	Bypassed, $V_{SMPS} = 3.3$ V	7.9 mA	
	Active with $V_{SMPS} = 1.4$ V	4.5 mA	-43%
Transmission at 0 dBm	Bypassed, $V_{SMPS} = 3.3$ V	8.8 mA	
	Active with $V_{SMPS} = 1.4$ V	5.2 mA	-41%
Transmission at 6 dBm	Bypassed, $V_{SMPS} = 3.3$ V	12.7 mA	
	Active with $V_{SMPS} = 1.7$ V	7.8 mA	-38%

Table 2.2: Power consumption of the microcontroller including RF subsystem and digital processing for $V_{DD} = 3.3$ V.

V_{IN} (V_{DD})	V_{OUT} (V_{SMPS})	I_{OUT}	F_{SW}	Efficiency
2.0 to 3.6 V	1.2 to 1.95 V	0 to 80 mA	4 or 8 MHz	70 to 90%

Table 2.3: Switched-mode power supply main characteristics

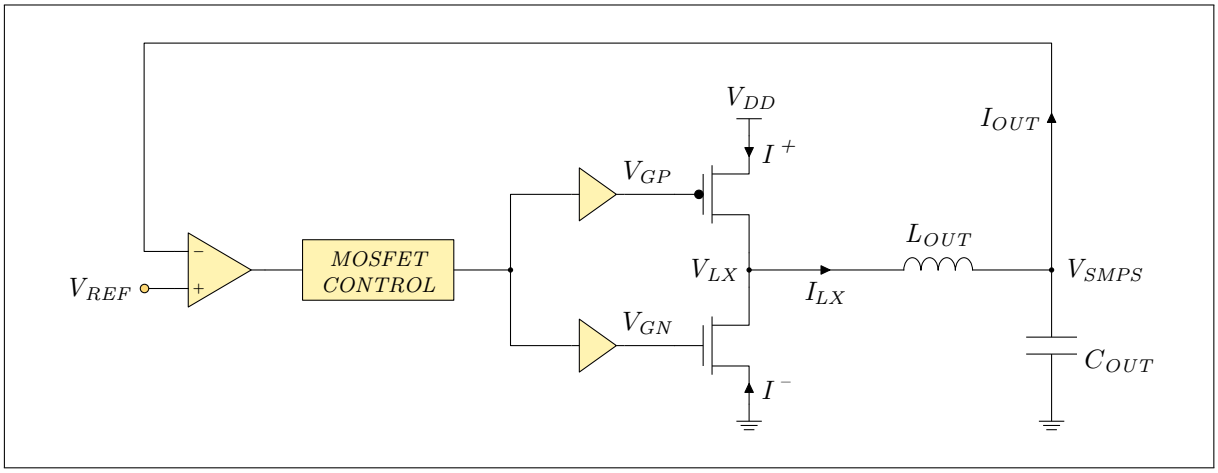


Figure 2.4: Simplified diagram of the SMPS architecture.

circuit delays either the gate voltage V_{GP} or V_{GN} depending on the transition to prevent cross-conduction: the two power MOSFETs can not be on at the same time or the power supply V_{DD} is shorted to ground.

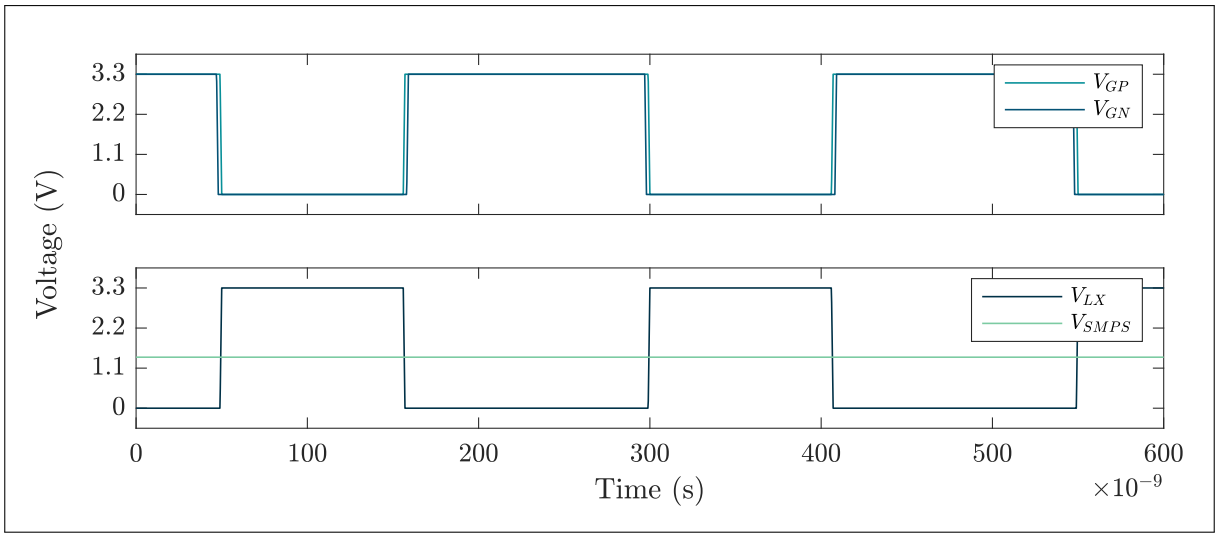
Depending on the chosen switching frequency F_{SW}, a specific LC couple is recommended to achieve the best performances [13]. For this thesis, a switching frequency of 4 MHz will be used in most cases. The pair $L_{OUT} = 10\,\mu H$ / $C_{OUT} = 4.7\,\mu F$ is chosen to minimize the current ripple at 4 MHz in the inductor and obtain a voltage ripple in the millivolt range on V_{SMPS}. It gives a cut-off frequency located around 23 kHz, two decades under the switching frequency. Due to the high value of both the inductance and the capacitance, these two passive components are not integrated inside the microcontroller as it would require a very large surface and nullify the economical interest of this microcontroller. L_{OUT} and C_{OUT} are surface mounted devices (SMD) soldered onto the PCB.

In the case of ideal voltage waveforms represented in Figure 2.5, the spectrum of the rectangular pulse signal V_{LX} contains every harmonics of the switching frequency F_{SW} (even and odd), with an amplitude that decrease following a cardinal sine function

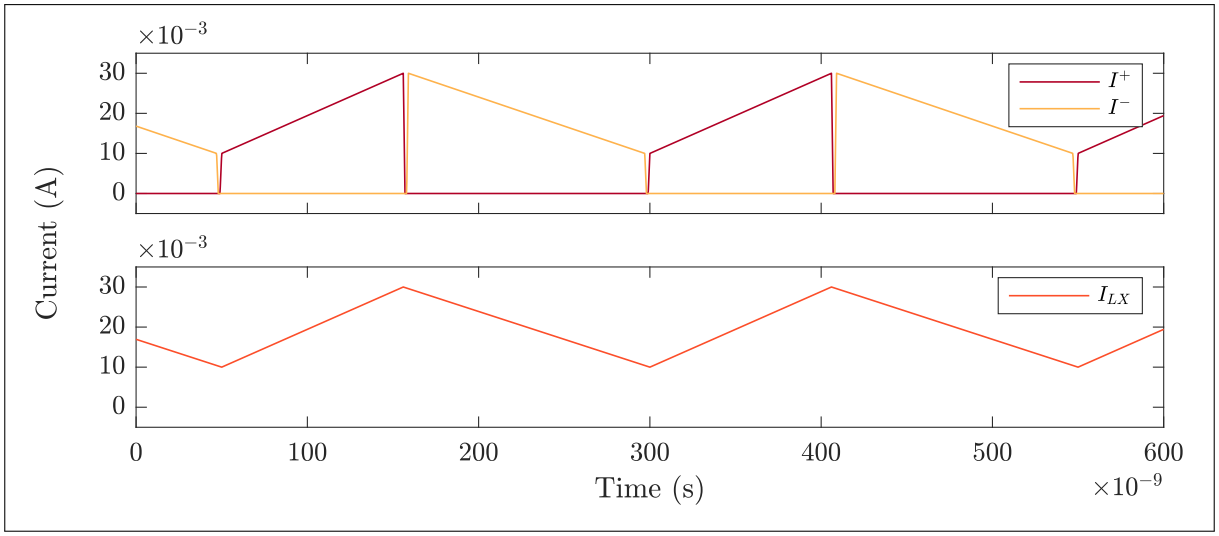
$$\mathrm{sinc}(x) = \frac{\sin(x)}{x}. \tag{2.4}$$

After an ideal second-order low-pass filter with a cut-off frequency located more than two decades below the fundamental frequency, the output voltage V_{SMPS} would be entirely filtered[4], only consisting of the DC component of V_{LX}.

[4]The 4 MHz fundamental would be attenuated by more than 80 dB, and the lower amplitude harmonics even more.



(a)



(b)

Figure 2.5: (a) Ideal SMPS voltage signals and (b) ideal SMPS current signals.

Architecture choice

The choice of architecture for the SMPS for this microcontroller (a buck converter with a current mode control) was mostly driven by economical constraints. It is a 'simple' architecture leading to a limited footprint in the microcontroller IC and cutting down silicon costs. Also, the integrated SMPS is based on a previously used intellectual property (IP), reducing design costs. Another type of controller is conceivable for the SMPS, however it would not affect the generated EMI for a constant switching frequency.

Architectures limiting the generation of EMI exist, like converters using soft-switching techniques (zero-voltage switching (ZVS) or zero-current switching (ZCS)) [14, 15] and isolated converters using a transformer [16]. However these architectures present constraints (extra external components or advanced silicon technologies) that are not compatible with low-cost microcontroller [17].

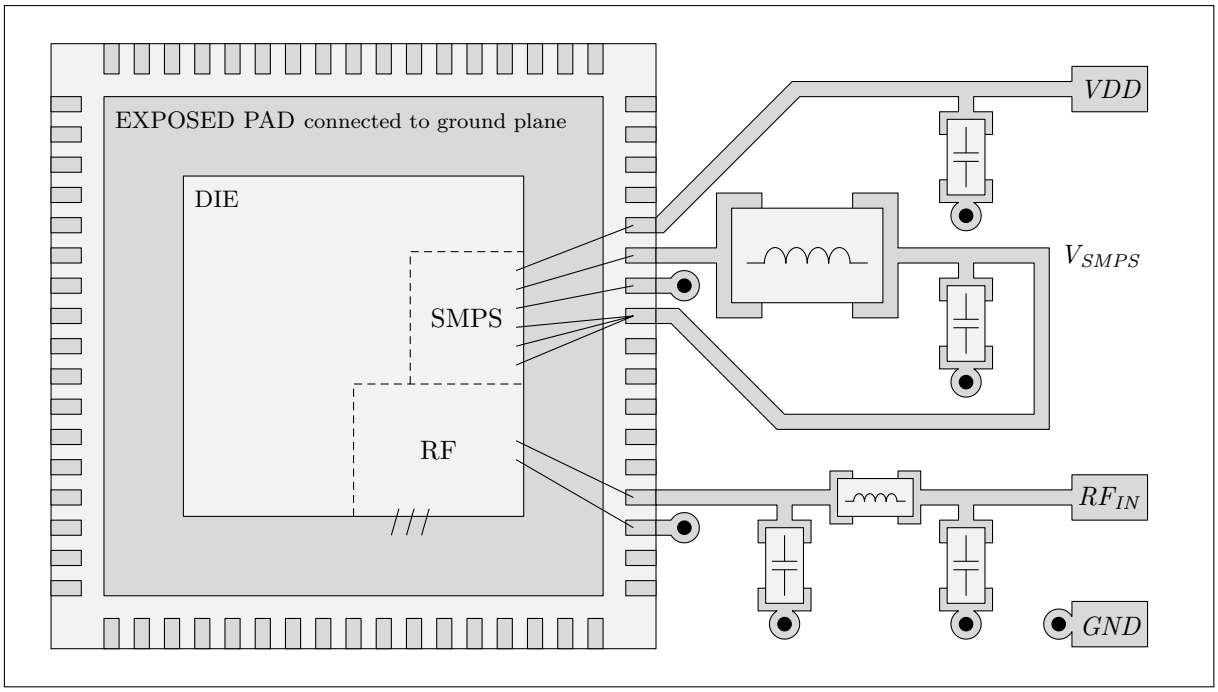


Figure 2.6: The microcontroller IC inside a 68-pin QFN package and the main SMPS and RF external components.

2.1.3 Microcontroller environment

The microcontroller needs to be embedded on a PCB with the required external components for any application case. The STM32WB55 is available on the market in 4 different packages: a 48-pin and a 68-pin quad-flat no-leads (QFN) package, a 100-ball wafer-level chip-scale package (WLCSP), and a 129-ball ball grid array (BGA) package.

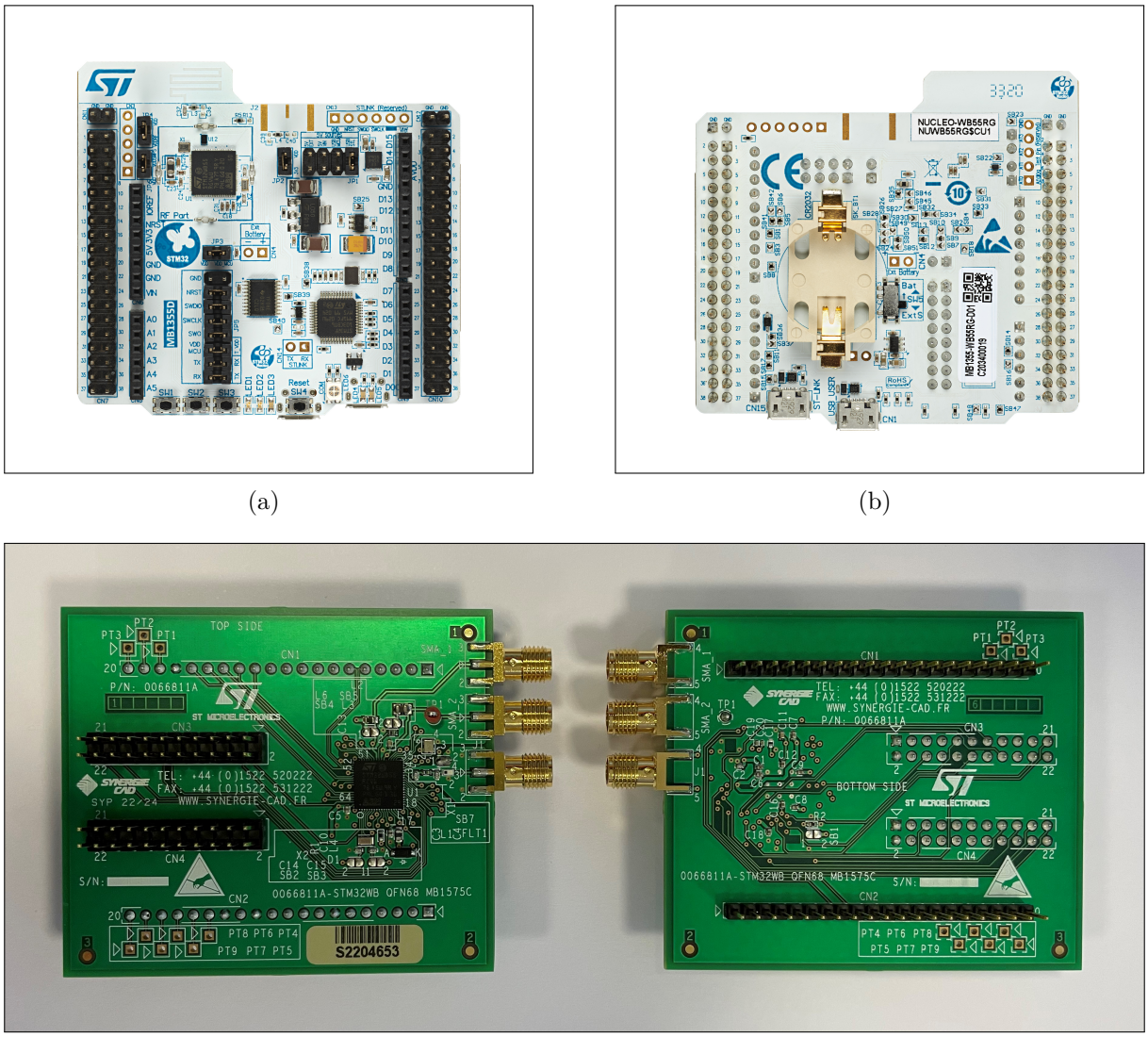
For this thesis, the QFN package is chosen as it is the most widely used option. Figure 2.6 depicts the studied system. The microcontroller die[5] is encapsulated inside a 68-pin QFN package and soldered onto the PCB. Among other external components, the SMPS input capacitor and output LC filter as well as the RF input/output pi matching network are embedded onto the PCB. An exposed pad soldered to the PCB ground plane ensure the connection for the different IC grounds. The SMPS power stage (MOSFETs and drivers) however possesses a dedicated ground pin to limit noise propagation.

The conducted EMI may propagates from the SMPS toward the BLE receiver via either the power supply V_{DD} (powering a part of the receiver), the SMPS output V_{SMPS} fed back into the microcontroller (powering most of the receiver), or the PCB ground plane (providing ground reference for the whole receiver and the RF input).

For the analysis of the generated interference and their impact, two test boards embedding the STM32WB55 in its 68-pin QFN package (referenced as VFQFPN68 for 68-pin very thin fine pitch quad-flat package no-leads) have been used: a development board commercialized by STMicroelectronics, the Nucleo-WB55RG, and test board designed for this thesis that will be named 'custom test board'.

Nucleo test board: The board is pictured in Figure 2.7(a) and 2.7(b). For this work, this test board is only used to measure the BLE receiver sensitivity under different operating

[5]a single copy of the integrated circuit cut from the silicon wafer.



(a) (b)

(c)

Figure 2.7: Nucleo-WB55RG development board (a) top view and (b) bottom view, and (c) custom test board embedding the STM32WB55 and dedicated SMA port on V_{DD} and V_{SMPS} for RF measurements.

conditions. The RF input/output is connected to a SMA port (J2, not fitted on the pictures) to limit the presence of radiated EMI in the environment during measurement.

Custom test board: The board is pictured in Figure 2.7(c). The custom test board has been designed based on [18] and modified to allow high frequency spectrum measurements of the noise generated by the SMPS on its input and output voltages. These two nodes are routed to separate SMA connectors via 50 Ω PCB trace, for a connection to a spectrum analyser.

Because high-frequency spectrum measurement is only possible on the custom test board, it is the system chosen for the analysis of EMI spectral content in the following section.

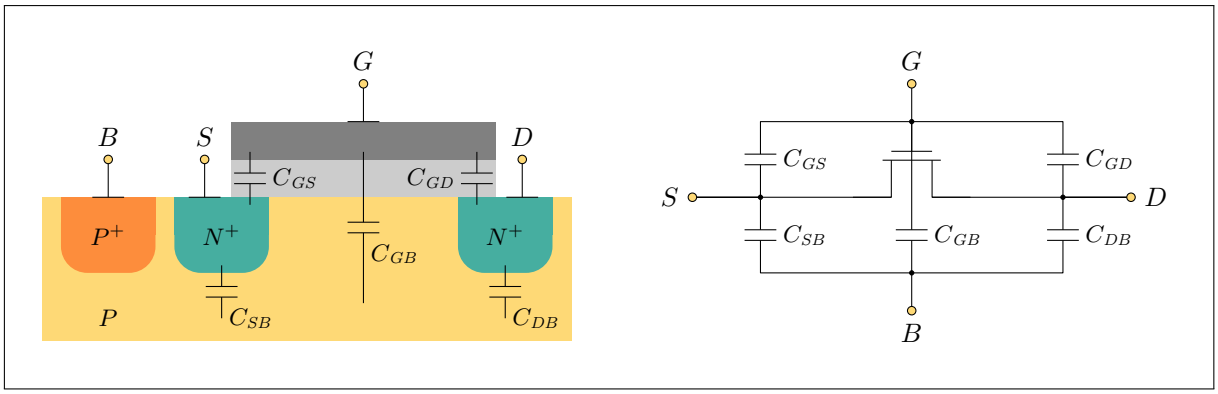


Figure 2.8: Cross section and schematic of a MOSFET parasitic capacitances.

2.2 Interference spectral content

This subsection focuses on the spectral content of the interference generated by the SMPS. Current and voltage discontinuities due to the non-linear operation of the SMPS produce unwanted high-frequency EMI [19–21]. Parasitic elements in propagation paths shape these interferences. The parasitic elements defining the resonances are first presented, and the two main interference generation mechanisms are then explained.

2.2.1 System parasitic elements

Parasitic resistances, inductances, and capacitances are present in the power MOSFETs, in the package, in the PCB traces and vias, and in the external passive components. Chosen package, PCB characteristics and external components corresponds to the custom test board. The parasitic elements needed for the following study and detailed in this subsection are summarize bellow:

- Power MOSFETs: Parasitic capacitance.
- Package: Parasitic resistance and inductance of bond wires and leads.
- Printed circuit board: Parasitic resistance and inductance of traces and vias.
- External passive components: Parasitic resistance, inductance, and capacitance.

The parasitic elements are presented as a schematic with their estimated value in Figure 2.11 at the end of this subsection.

Power MOSFETs

In order to deliver the required output current (up to 80 mA), the two power MOSFETs are relatively large ($L_N = 380\,\text{nm}$, $W_N = 2.4\,\text{mm}$, $L_P = 400\,\text{nm}$, $W_P = 7.2\,\text{mm}$). Thus, their parasitic capacitances are not negligible and play an important role in shaping the generated EMI, due to resonances with parasitic inductances in the system.

Because of the physical structure of the device, parasitic capacitances are present between each of the four terminals of the MOSFETs, with the capacitance between source and drain being negligible [22]. Figure 2.8 depicts the five parasitic capacitances in the MOS transistors and the corresponding schematic.

The device models provided by the founder allows for the extraction of parasitic capacitances for the implemented power MOSFETs. Table 2.4 presents the extracted parasitic

Parasitic capacitance		C_{GS}	C_{GD}	C_{GB}	C_{DB}
PMOS	'on' state	7.04 pF	5.83 pF	829 fF	×
	'off' state	×	1.20 pF	×	1.29 pF
NMOS	'on' state	2.06 pF	2.24 pF	173 fF	×
	'off' state	×	418 fF	×	511 fF

Table 2.4: Power MOSFETs parasitic capacitances extracted the 90 nm CMOS technology transistor models.

capacitance values for both the NMOS and PMOS, in their 'on' or 'off' state. The × value means that the parasitic capacitance is shorted (same potential on both terminals). The bulk is tied to the source for both transistor, C_{SB} is always shorted, giving four parasitic capacitances to consider.

Package

Figure 2.9 illustrates various views of a QFN package. A 32-pin QFN package (instead of 68-pin) is depicted to simplify the schematics.

The integrated circuit die is attached to the exposed pad using a thermal adhesive. The exposed pad is an exposed metal plate (here, made of copper) located on the bottom of the package. It is soldered to the PCB, and is employed to improve the power dissipation of the package. The exposed pad is also electrically connected to the PCB ground plane.

Each of the circuit pads are connected using bond wires either to the package leads for the circuit inputs/outputs (I/O) and supplies, or to the exposed pads for the circuit grounds. To limit EMI propagation, the supply and the ground of the SMPS power stage and drivers are connected to dedicated leads. The bond wires are made of gold 2N[6], a 99% purity gold alloy. The leads are made of copper.

The die, the exposed pad, the leads and the bond wires are encapsulated inside a moulding compound (here, an epoxy resin), leaving accessible only to the bottom of the leads and exposed pad, to be soldered onto the PCB. The main characteristics of the QFN package used in this thesis are sum-up in the Table 2.5.

Parasitic resistance: Most of the parasitic resistance is coming from the bond wire, as gold is more resistive than copper and the bond wire section area is much smaller than the leads section area ($\approx$ 100 times smaller). The electrical path between the die pads and the package pins is formed by the bond wires and the leads. Its total parasitic DC resistance can be calculated [4] based on the material resistivity ρ, the length L and the section area A using the relation

$$R_{DC} = \rho \cdot \frac{L}{A}. \tag{2.5}$$

As the signal frequency increases, the current tends to flow closer and closer to the conductor surface, reducing the conductive section area. This phenomenon is the skin effect and provokes a rise in conductor resistance with frequency. The skin depth δ represents the thickness under the conductor surface where the current is flowing and is given by

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0}}, \tag{2.6}$$

[6] 2N stands for "two nines" as in 99%

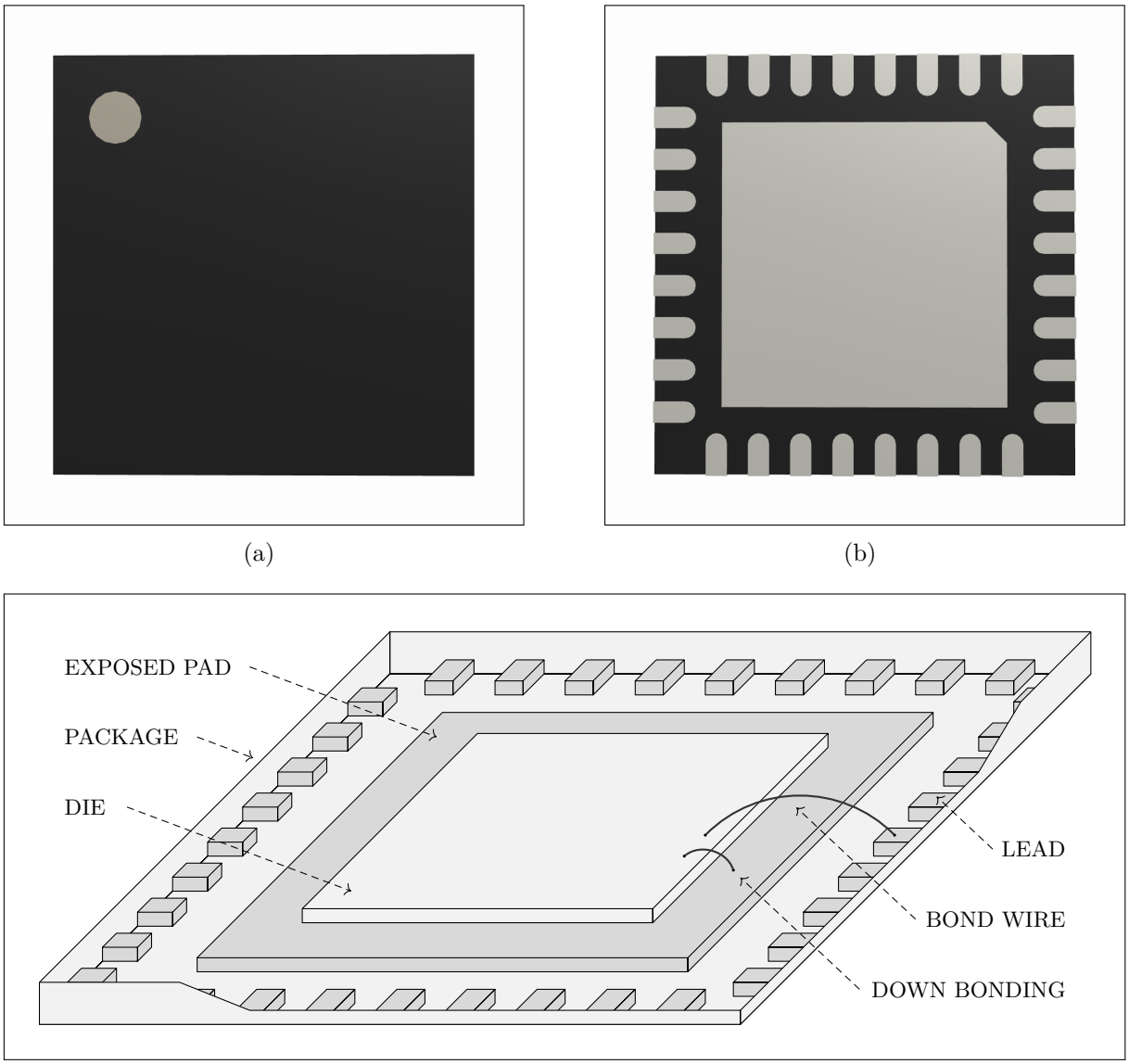


Figure 2.9: (a) Top view, (b) bottom view and (c) 3D cross section of a 32-pin quad-flat no-lead package.

where f denotes the frequency and $\mu_0 = 4\pi \times 10^{-7}$ H/m the vacuum magnetic permeability. The AC resistance of a conductor can be determined the same way as for the DC resistance with (2.5), but using the effective conductor section, based on the skin depth. The total resistance $R_{AC_{round}}$ of a round conductor of length L and radius r when $\delta < r$, and the total resistance $R_{AC_{rect}}$ of a rectangular conductor of length L, width W and height H when $\delta < 0.5 * \max(W, H)$ are given by

$$R_{AC_{round}} = \rho \cdot \frac{L}{\pi\delta(2r - \delta)} \qquad \textit{and} \qquad R_{AC_{rect}} = \rho \cdot \frac{L}{2\delta(W + H - 2\delta)}. \tag{2.7}$$

The parasitic resistance of the bond wires and the leads are given for reference at different frequencies in Table 2.6.

Package	Size	8.00 mm × 8.00 mm
	Height	900 µm
	Pitch	400 µm
	Material	Epoxy resin, $\varepsilon_r \approx 3.8$
Die	Size	4.41 mm × 4.41 mm
	Height	250 µm
Exposed pad	Size	6.40 mm × 6.40 mm
	Height	200 µm
	Material	Copper, $\rho \approx 1.7 \times 10^{-8}\,\Omega\,\mathrm{m}$
Leads	Length	500 µm
	Width	200 µm
	Height	200 µm
	Material	Copper, $\rho \approx 1.7 \times 10^{-8}\,\Omega\,\mathrm{m}$
Bond wires	Length	1.70 mm – 2.30 mm
	Diameter	20.3 µm
	Material	Gold 2N, $\rho \approx 4.0 \times 10^{-8}\,\Omega\,\mathrm{m}$

Table 2.5: Main characteristics of the chosen package for the STM32WB55 study (VFQFPN68).

Parasitic resistance	Bond wires	Leads	Total
DC value	210 – 284 mΩ	213 µΩ	210 – 284 mΩ
Value at 100 MHz	210 – 284 mΩ	1.67 mΩ	212 – 286 mΩ
Value at 2.4 GHz	577 – 781 mΩ	7.99 mΩ	585 – 789 mΩ
Value at 4 GHz	726 – 984 mΩ	10.3 mΩ	737 – 994 mΩ

Table 2.6: Parasitic resistance of the QFN package (bonding and lead) at different frequencies.

Parasitic inductance: The package bond wires and leads present internal (negligible) and external inductances, that can be calculated based on their geometry and environment [23]. The bond wires are considered as a circular wire of radius r_W at a distance d above the PCB ground plane considered infinite and perfectly conducting. The per-unit-length loop inductance of a wire above a ground plane is given by

$$L = \frac{\mu_0}{2\pi} \cdot \ln\left[\frac{d}{r_W} + \sqrt{\left(\frac{d}{r_W}\right)^2 - 1}\right] \quad \mathrm{H/m}, \tag{2.8}$$

The distance between the bond wire and the ground plane is $d \approx 470\,\mu\mathrm{m}$[7], giving a self-inductance of 906 pH/mm.

The leads are seen as a microstrip line [22] of width W at a distance d above the PCB ground plane considered infinite and perfectly conducting. The per-unit-length loop

[7] Average value as the distance between the bond wires and the PCB ground plane is not constant.

Parasitic inductance	Bond wires	Leads	Total
Value	1.54 – 2.08 nH	184 pH	1.72 – 2.27 nH

Table 2.7: Parasitic inductance of the QFN package (bonding and lead).

inductance of a microstrip line above a ground plane when $W/d \geqslant 1$ is given by

$$L = \frac{120\pi}{\nu_0} \cdot \left[\frac{W}{d} + 1.393 + 0.667 \cdot \ln\left(\frac{W}{d} + 1.4444\right)\right]^{-1} \quad \text{H/m}, \tag{2.9}$$

where $\nu_0 \approx 3 \times 10^8$ is the speed of light. The distance between the leads and the ground plane is $d = 100\,\mu\text{m}$, giving a self-inductance of 369 pH/mm. The parasitic inductance for the bond wires and the leads are given in Table 2.6.

Printed circuit board

Numerical values are given for the custom test board presented in 2.1.3. The parasitic DC and AC resistance of PCB traces can be calculated from (2.5) and (2.7).

The PCB traces are made of copper ($\rho \approx 1.7 \times 10^{-8}\,\Omega\,\text{m}$) with a thickness of 35 µm and a width of either 270 µm for the 50 Ω traces or 80 µm for the other traces. The DC resistance is $R_{DC} = 1.80\,\text{m}\Omega/\text{mm}$ for the 270 µm traces and $6.07\,\text{m}\Omega/\text{mm}$ for the 80 µm traces. For short traces (until $\approx 10\,\text{mm}$), it is negligible compared to the DC resistance of bond wires and external passive components. The AC resistance is $R_{AC} = 21.0\,\text{m}\Omega/\text{mm}$ at 2.4 GHz for the 270 µm traces and $56.5\,\text{m}\Omega/\text{mm}$ for the 80 µm traces. It need to be considered for traces longer than $\approx 2\,\text{mm}$. DC resistance value are presented in Figure 2.11 at the end of this subsection.

The parasitic capacitance between the PCB traces and ground plane have a limited influence on the observed phenomena and will not be presented here.

Parasitic inductance: The PCB trace and via inductances are calculated from [23]. The PCB traces are microstrip lines of width W at a distance d above the PCB ground plane considered infinite and perfectly conducting. The per-unit-length loop inductance of a microstrip line above a ground plane when $W/d \leqslant 1$ is given by

$$L = \frac{60}{\nu_0} \cdot \ln\left(\frac{8d}{W} + \frac{W}{4d}\right) \quad \text{H/m}. \tag{2.10}$$

As the decoupling capacitor C_{IN} is located on the bottom side of the PCB, a via is necessary to connect it to the SMPS positive supply input V^+. The via is considered as a simple wire of radius r_V and length h, and its inductance is given by

$$L = \frac{\mu_0}{2\pi} \cdot \left[\ln\left(\frac{2h}{r_V}\right) - 1\right] \quad \text{H/m}. \tag{2.11}$$

The PCB possesses two ground planes located just under the top and the bottom layer, at a distance $h = 65\,\mu\text{m}$. The via connecting top and bottom layer traces to the ground plane is considered negligible.

The PCB trace inductances needed for the following analysis are given in Table 2.8.

Trace	**Length**	**Width**	**Inductance**
From V_{LX} to L_{OUT}	9.6 mm	80 µm	3.68 nH
From L_{OUT} to C_{OUT}	6.9 mm	270 µm	1.50 nH
From C_{OUT} to V_{SMPS}	2.4 mm	270 µm	522 pH
From V^+ to via	2.9 mm	270 µm	630 pH
Via	**Height**	**Diameter**	**Inductance**
From V^+ via to C_{IN}	1.6 mm	200 µm	789 pH

Table 2.8: Parasitic inductance of the PCB traces and vias.

External passive components

External passive components embedded on the PCB are surface-mount devices (SMD). In surface-mount technology (SMT), the components are soldered directly onto the surface of the PCB, in comparison to through-hole technology where the components are inserted through holes drilled in the PCB and soldered to pads on the opposite side. SMT presents several advantages compared to through-hole technology: the components are smaller and usually cheaper, allow an higher component density (components placed on both sides and no through-holes required), present better RF performances (lower parasitic elements) and better electromagnetic compatibility (EMC) performances (smaller loop area and no leads), possess better mechanical performances and allow lower cost for mass production (simpler and faster automated assembly).

SMD exhibit parasitic resistance, inductance and capacitance affecting their high frequency behavior, playing an important role defining EMI resonant frequencies. Figure 2.10(a) depicts the model used to represent the low and high frequency behavior of an inductor and capacitor, using equivalent series and parallel components (ESx and EPx). Figure 2.10(b) shows the impedance variation with the frequency.

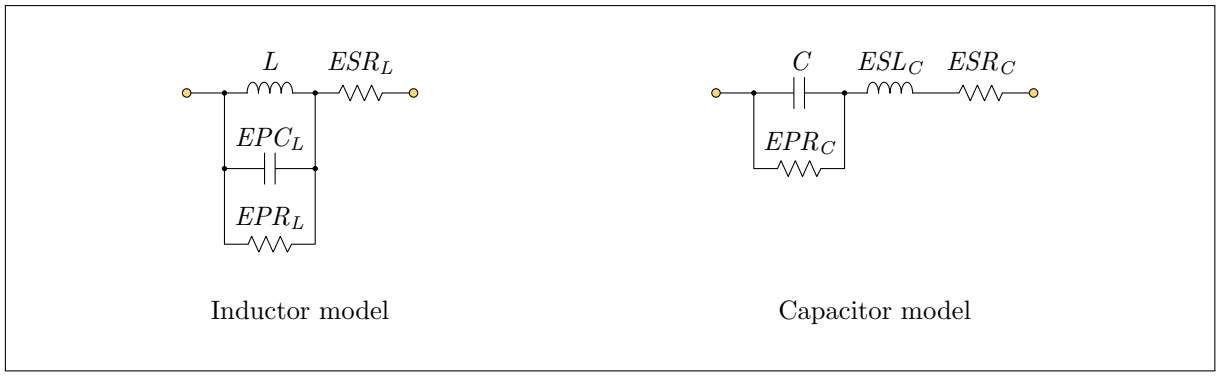
For the inductor, the impedance is dominated by its DC resistance ESR at low frequency. Above the self resonant frequency SRF caused by its parasitic capacitance ESC, the impedance is dominated by this parasitic capacitance. The equivalent parallel resistance EPR limit the impedance at the self resonance.

For the capacitor, the impedance is dominated by the equivalent parallel resistance EPR at low frequency. Above the self resonant frequency SRF caused by its parasitic inductance ESL, the impedance is dominated by this parasitic inductance. The DC resistance ESR limit the impedance at the self resonance.

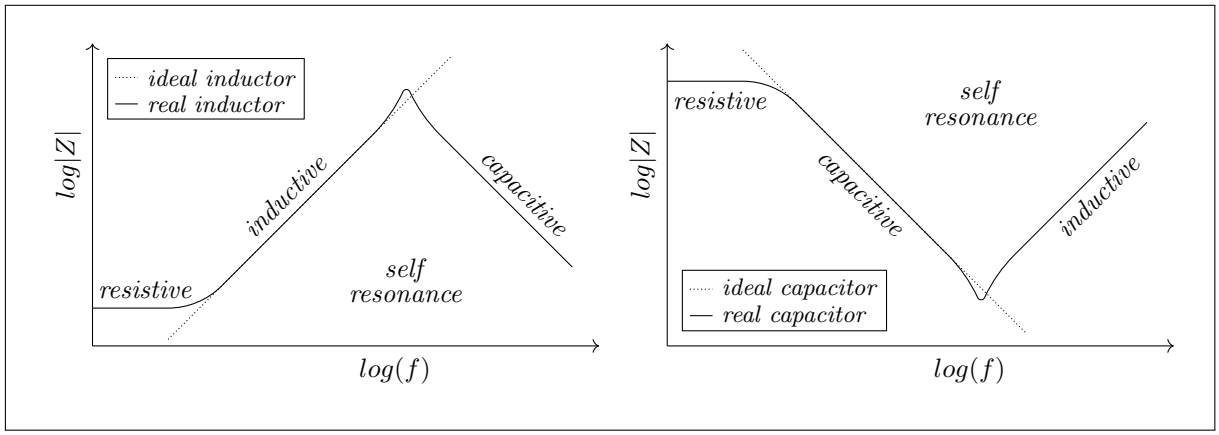
In Table 2.9 is presented the equivalent series and parallel elements as well as the self resonant frequency for the SMPS output filter inductor and capacitor. On the custom

L_{OUT}	**L**	**EPC**	**ESR**	**EPR**	**SRF**
	10 µH	2.2 pF	600 mΩ	6 kΩ	34 MHz
C_{OUT}	**C**	**ESL**	**ESR**	**EPR**	**SRF**
	4.7 µF	370 pH	3.75 mΩ	21 MΩ	3.8 MHz

Table 2.9: Model equivalent elements for the SMPS filter passive components.



(a)



(b)

Figure 2.10: (a) Parasitic model of an inductor and a capacitor and (b) impedance of the modelled inductor and capacitor.

test board, the 10 µH inductor L_{OUT} is manufactured by Murata[8] and the 4.7 µF capacitor C_{OUT} by TDK[9]. Values comes from models given by both manufacturers.

IC environment parasitic elements sum-up

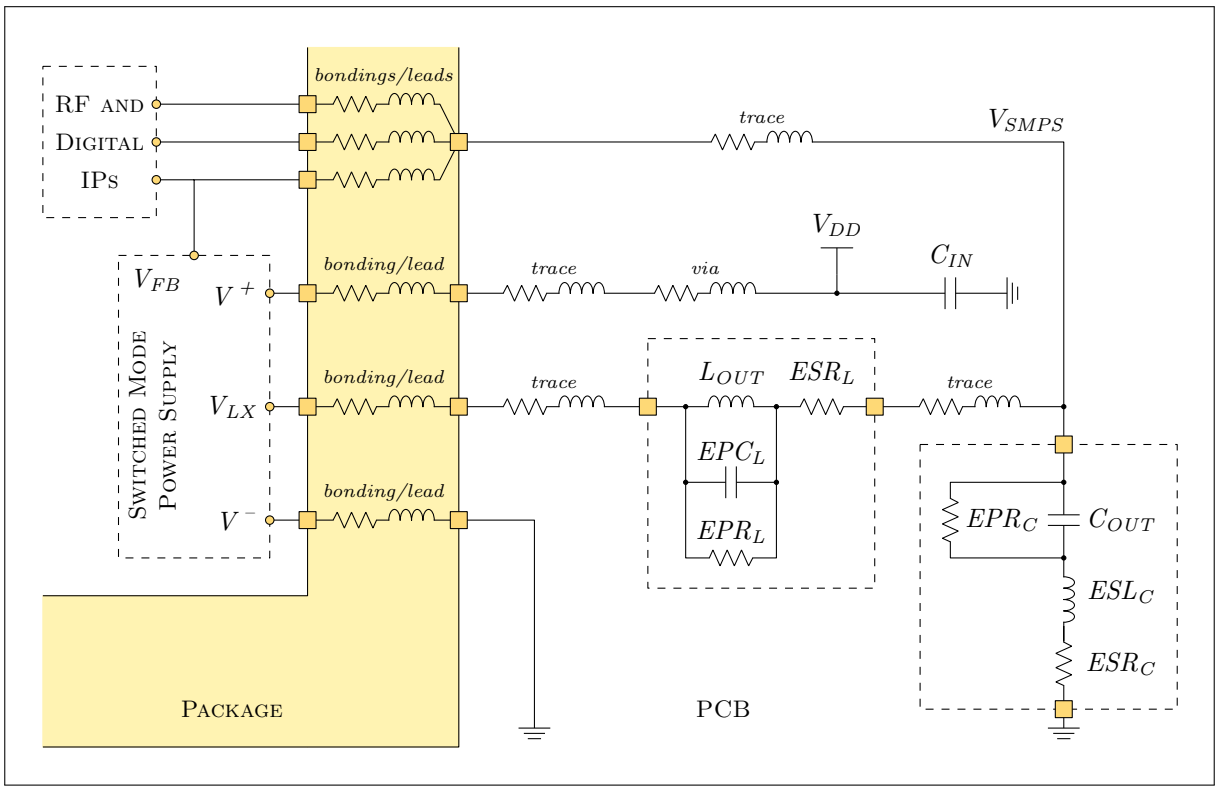
The main parasitic elements of the package, PCB, and external passives components[10] of the studied system and presented in this subsection are summarize in Figure 2.11(a). The values of the components are given in Figure 2.11(b).

These main parasitic elements of the IC environment, as well as parasitic elements inside the IC itself, are involved in two phenomena explaining the presence of resonance in the spectrum of EMI generated by the SMPS. The values of parasitic elements allow to estimate the frequency of each resonance The two phenomena are described in the following subsections.

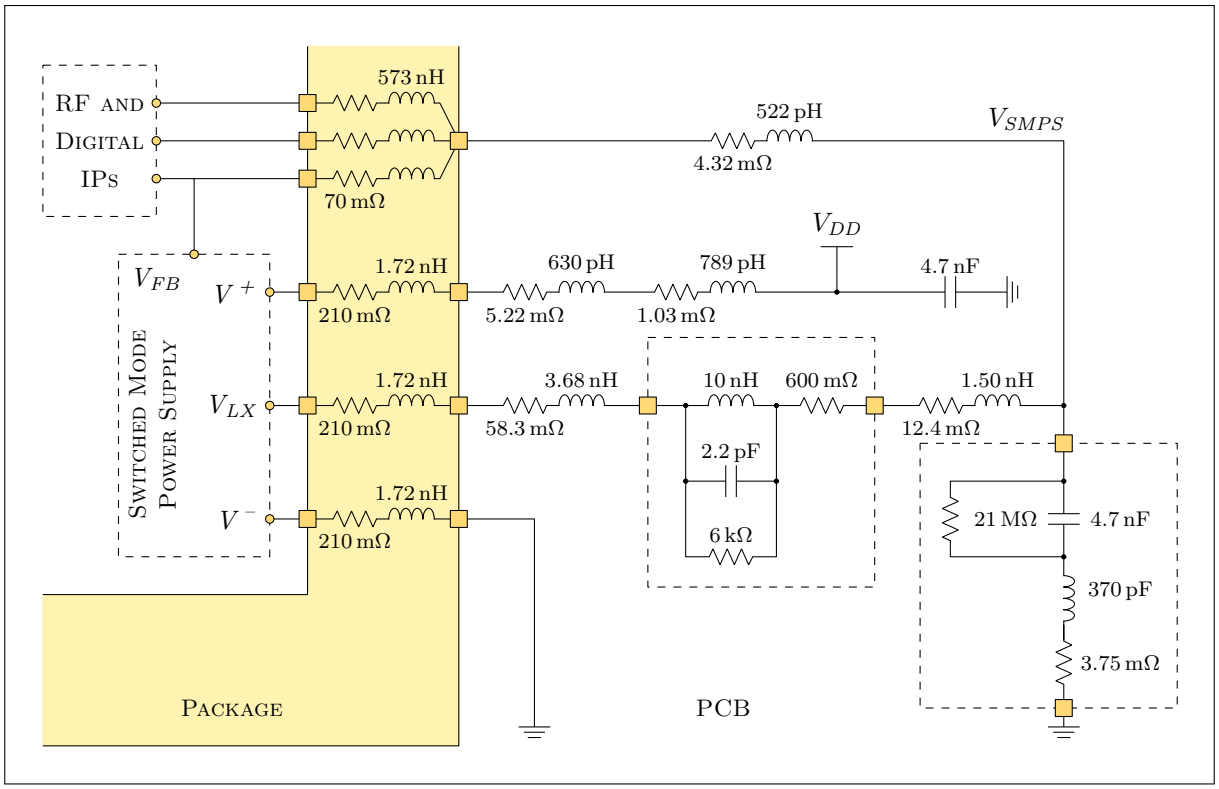
[8]Murata LQM21FN100M70L, 0805 package, 2.00×1.25 mm.

[9]TDK C1005X5R1A475K050BC, 0402 package, 1.00×0.50 mm.

[10]The input capacitor C_{IN} is identical to the output capacitor C_{OUT} and is modeled the same way (not represented in Figure 2.11).

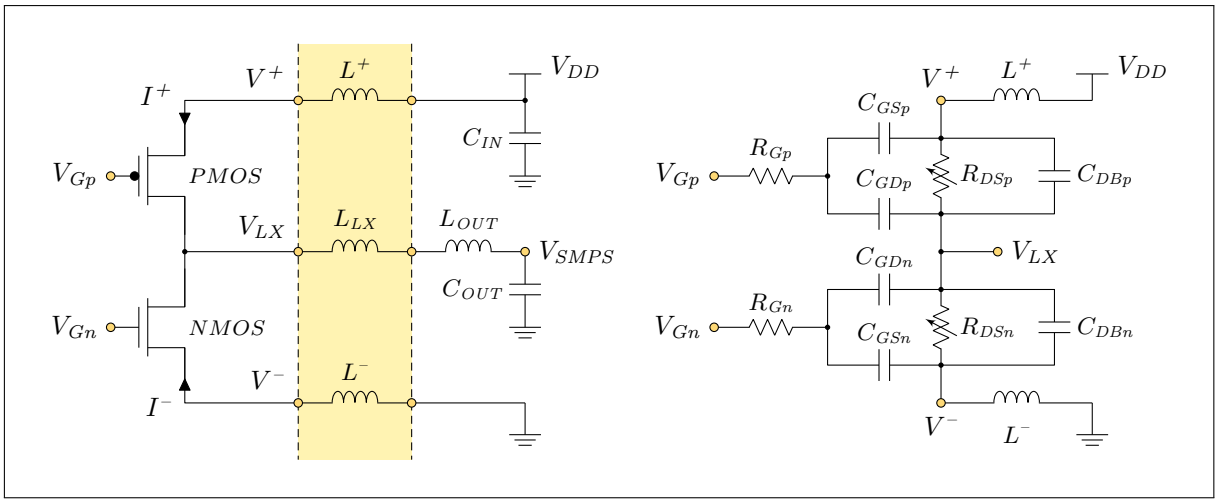


(a)

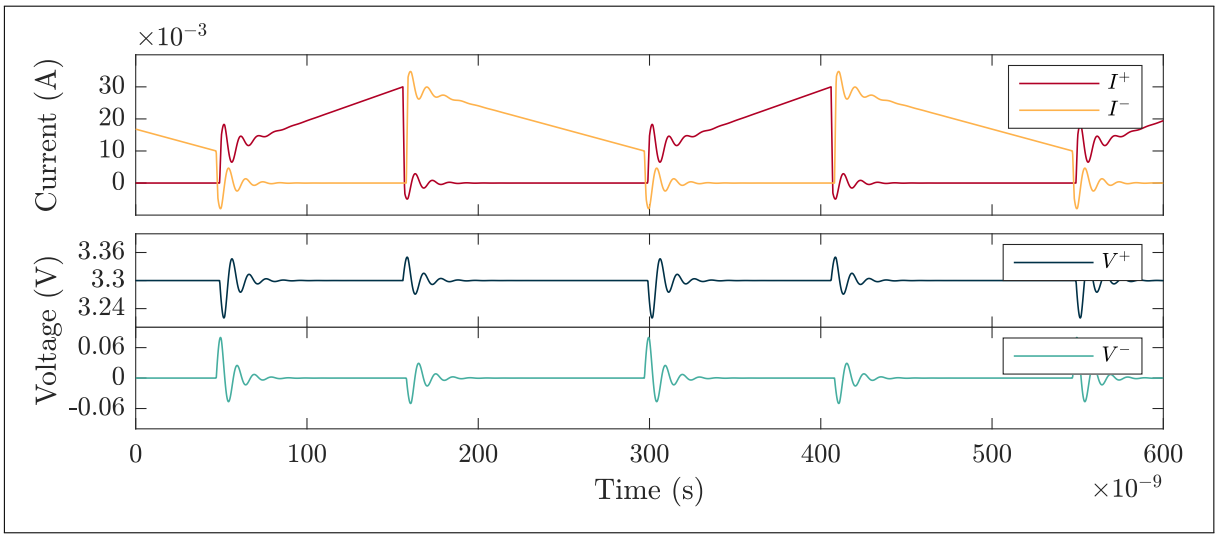


(b)

Figure 2.11: Parasitic elements in the IC environment considered for the following analysis.



(a)



(b)

Figure 2.12: (a) The SMPS power stage and its equivalent schematic (C_{GB} is note represented here as it is negligible) and (b) resonance on current and voltage signals caused by the power MOSFETs and package/PCB parasitics.

2.2.2 Current discontinuities

In this subsection, the focus is made on the analysis of resonances associated with parasitic elements of the integrated power MOSFETs.

Because of its mode of operation (i.e. fast switching of power MOSFETs), relatively large discontinue currents are flowing through parasitic inductances. Represented on Figure 2.12(a), current discontinuities through the package parasitic inductances, leads to voltage overshoots across them:

$$v_L = L * \frac{di}{dt}. \tag{2.12}$$

Figure 2.12(b) represents the main current and voltage signals for the SMPS, coming from transistor-level simulation of the power stage. Every time the power transistors are opening or closing, the current through them rise or fall abruptedly, in about a nanosecond.

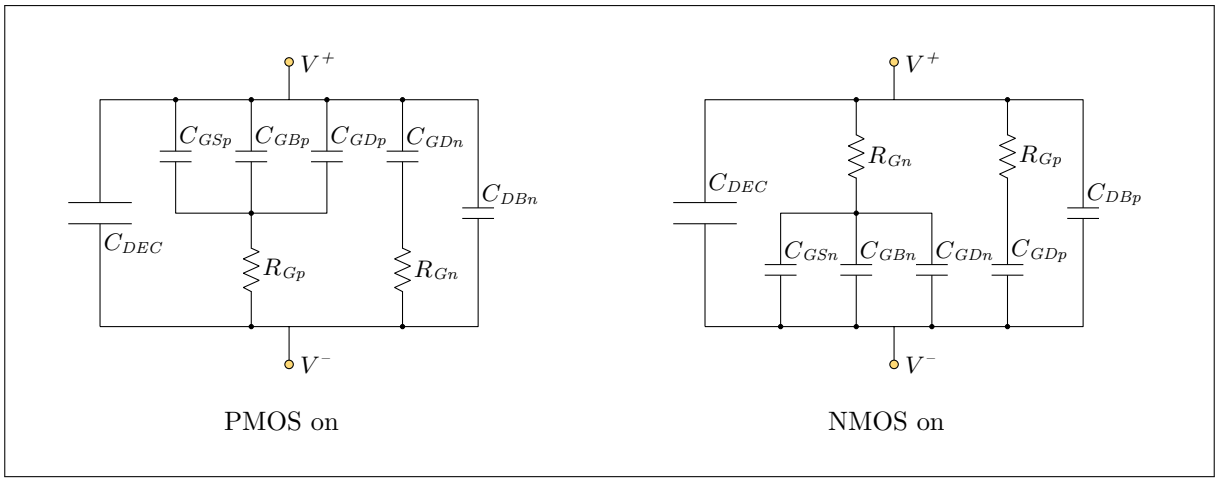


Figure 2.13: Equivalent parasitic network of the power MOSFETs during the two phases, with the integrated decoupling capacitor.

From (2.12), a current variation of 20 mA in 1 ns leads to a voltage overshoot of 40 mV across a 2nH package parasitic inductance.

During the SMPS operation, two states[11] are possible: a first state where the PMOS is 'on' and the NMOS is 'off' and a second state where the PMOS is 'off' and the NMOS is 'on'. During the transition from one state to another, the power MOSFETs equivalent parasitic network (shown in Figure 2.13) is stimulated, and resonates with the parasitic inductances of the package and PCB traces. This phenomenon is well described in [24] and from it, it is possible to predict resonances in the generated EMI.

Resonant frequencies estimation

Two resonances f_{res} linked to the two equivalent parasitic networks presented in Figure 2.13 are expected[12]. The integrated decoupling capacitor C_{DEC} present between the positive and negative supply of the power stage is also represented as its value is relatively large compared to the parasitic capacitance and affects the resonance values. At first order, the two resonance are located at

$$f_{res1} = \frac{1}{2\pi\sqrt{(L^+ + L^-)C_{Pon}}} \quad and \quad f_{res2} = \frac{1}{2\pi\sqrt{(L^+ + L^-)C_{Non}}}. \tag{2.13}$$

The terms L^+ and L^- represents the total parasitic inductance on the positive and negative supply path, respectively, coming from the package and the PCB traces/vias. The terms C_{Pon} and C_{Non} represents the equivalent capacitance of the 'PMOS on' and 'NMOS on' networks presented in Figure 2.13, respectively.

Based on the parasitic component values presented in the previous subsection, it is possible to estimate the frequencies of expected resonances in the EMI spectrum. From the values for parasitic inductance and capacitance implied in the resonance presented in table 2.10 it gives:

$$f_{res1} = 373\,\text{MHz} \quad and \quad f_{res2} = 418\,\text{MHz}. \tag{2.14}$$

[11] a short third state where both MOSFETs are 'off' to avoid cross conduction also exists but is not relevant for this analysis.

[12] A third resonance due to substrate coupling is also given in [24] but negligible in our system, it will not be detailed here.

L^+	L^-	C_{Pon}	C_{Non}
3.14 nH	1.72 nH	37.4 pF	29.8 pF

Table 2.10: Parasitic inductance and capacitance mainly implied in the resonance.

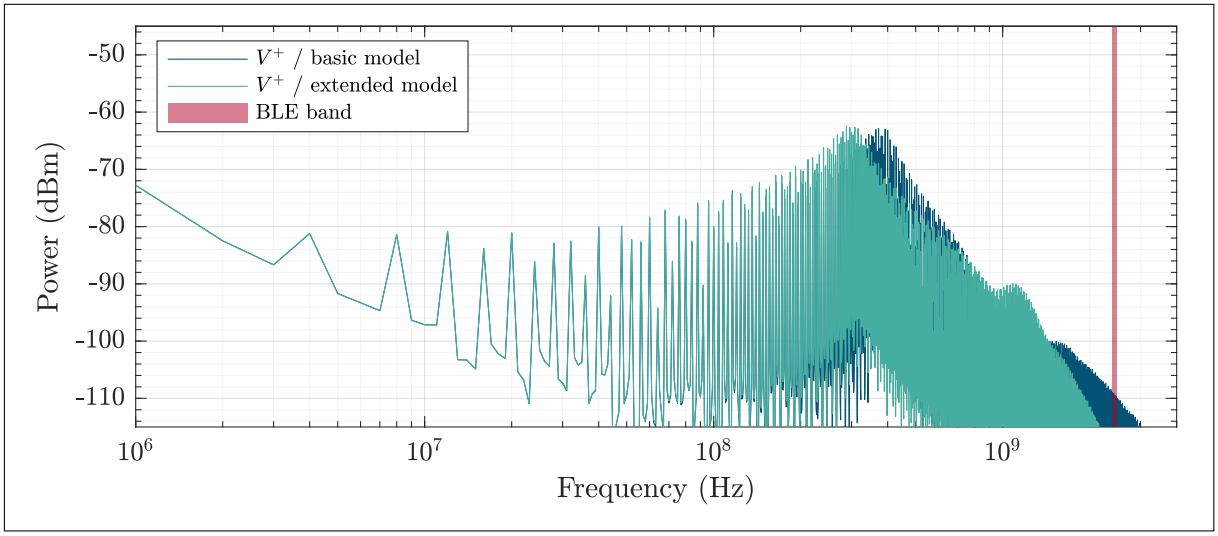


Figure 2.14: Simulated EMI on the SMPS input voltage V^+: (a) simple model and (b) more complete model.

These two resonance are predicted at a relatively low frequency compared to the BLE signal (around 2.4 GHz) and shouldn't be a major concern.

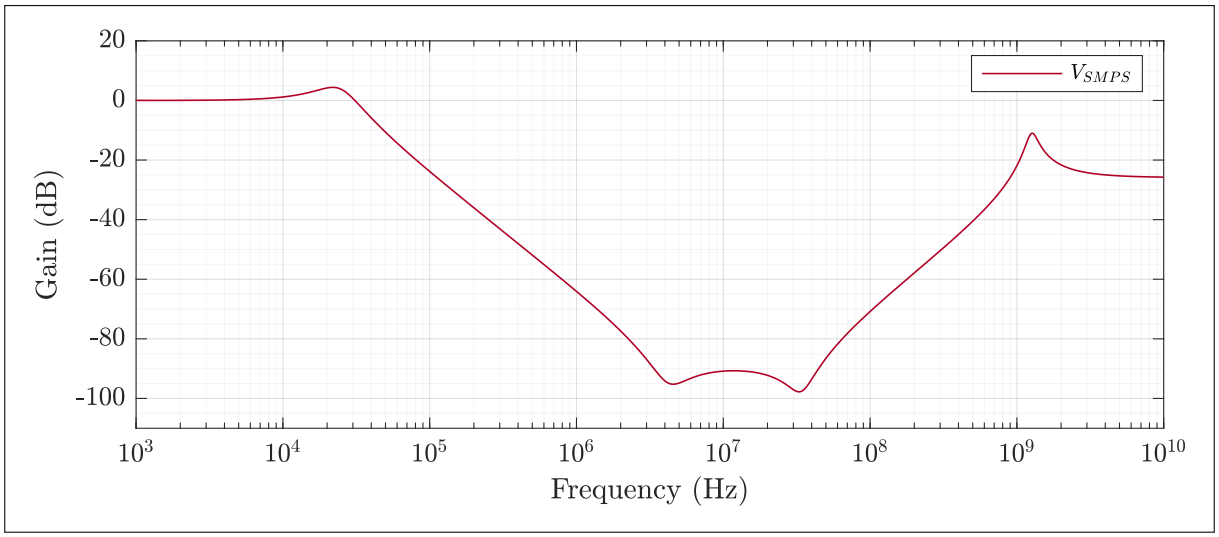
Power stage circuit simulation

The power stage and its environment (cf. Figure 2.11) are simulated with Cadence Spectre.

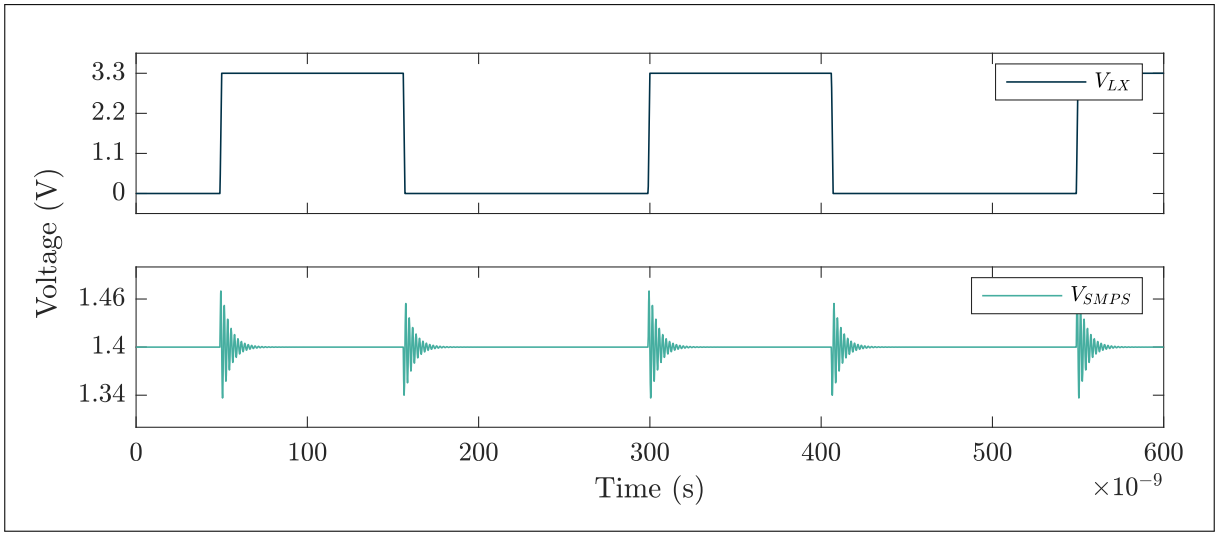
The simulated EMI on the SMPS input voltage V^+ is displayed in Figure 2.14 ('basic model' spectrum). The 4 MHz fundamental and its harmonics, shaped by the system resonances are visible. Only one resonance located around 385 MHz is discernable, however the two predicted resonances are close to each other (45 MHz apart).

Figure 2.14 presents also the same simulation is realized on a more complete test bench ('extended model' spectrum). The main difference between the simulated systems resides in the integrated decoupling capacitor. The simple test bench takes into account only the integrated decoupling capacitors connected between V^+ and V^- while the more complete test bench adds the decoupling capacitors between V^+ and the main IC ground, connected to the PCB ground plane through the package exposed pad. With this added capacitor, the stimulated equivalent network becomes more complex, and solving the circuit by hand to predict the theoretical resonant frequencies is much more difficult. The simulated resonance is now located approximately 100 MHz lower, at a frequency around 300 MHz. From (2.13), we can estimate the value of the total equivalent capacitance corresponding to this resonance at 58.0 pF.

However, this more complete test bench still does not represent the whole microcontroller system, and the equivalent resonant network involves more capacitors. Because of the extra capacitors, the total equivalent resonating capacitance should be higher and so,



(a)



(b)

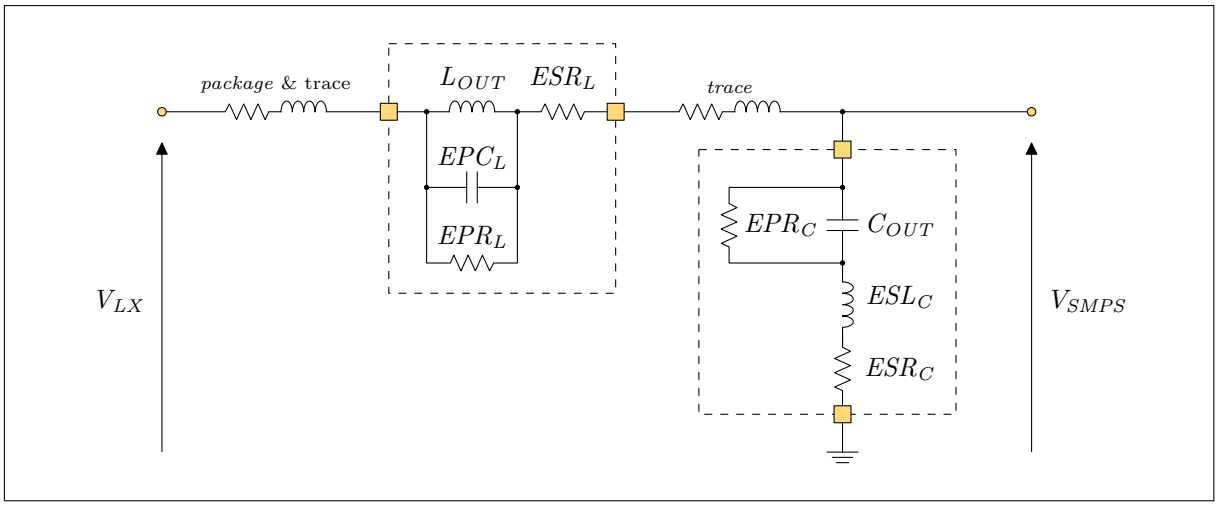
Figure 2.15: (a) Frequency response of the SMPS output filter and (b) a pulse signal V_{LX} through this filter

the resonance lower (than 300–400 MHz). As the resonance linked to this phenomenon can be expected at least a decade below the BLE signal, it should not be a major concern in this study.

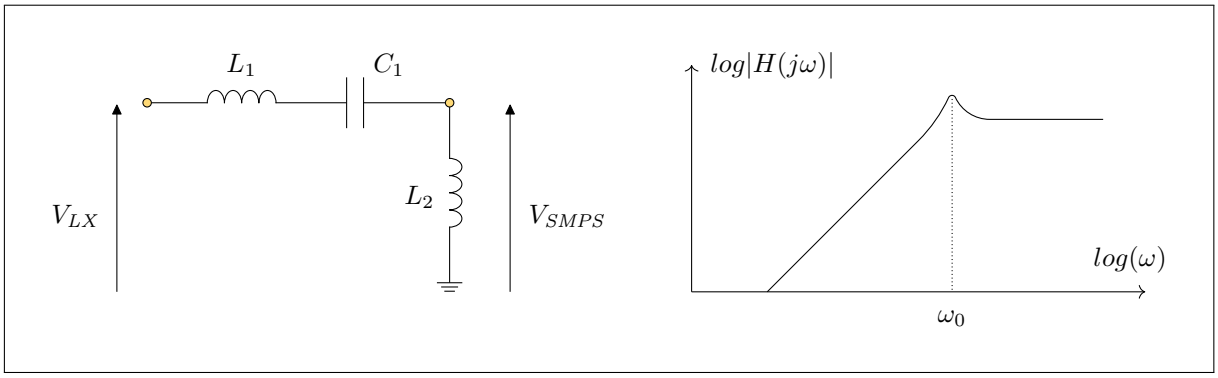
2.2.3 Voltage discontinuities

In this subsection, the focus is made on the analysis of a resonance associated with parasitic elements of the external output filter.

The output filter is a second order LC low-pass filter, with a cut-off frequency located around 23 kHz (L_{OUT} = 10 µH and C_{OUT} of 4.7 µF). This is roughly two decades below the SMPS switching frequency f_{SW} = 4 MHz to properly filter the fundamental and the first harmonics of the pulse signal V_{LX} that carries most of the energy. The BLE band is located five decades above the filter cut-off frequency, it is difficult to filter properly with only two passive components on such a wide frequency range.



(a)



(b)

Figure 2.16: (a) Parasitic model of the external filter and (b) high-frequency equivalent circuit (resistances are ignored).

[25] and [26] show the importance of considering parasitic elements in EMI filters as it play an important role in their performance. High-frequency resonance can occur due to parasitic inductance and capacitance in the SMPS output filter. [26–29]. High frequency harmonics in V_{LX} are not entirely filtered and high frequency content is present on V_{SMPS}. This phenomenon is represented in Figure 2.15.

Solutions presented in [30] and [31] include adding high frequency common-mode choke in noise source loop and bead core on input ground line that increase the final cost for the client (more components and larger PCB).

Resonant frequency estimation

A model of the SMPS output filter is presented in Figure 2.16(a), for now, ignoring the load connected on the feedback branch. For frequencies greater than the SRF of both the output inductor and capacitor ($f > 100\,\text{MHz}$), L_{OUT} is considered open (impedance dominated by EPC_L) and C_{OUT} shorted (impedance dominated by ESL_C). Therefore, for frequencies above 100 MHz, the low-pass LC filter behaves like a high-pass filter.

The high-frequency equivalent circuit and its frequency response are depicted in Figure 2.16(b). The focus is made on the frequency of the resonances, not their amplitude, we are not considering parasitic resistances here. Elements represented in the high-frequency

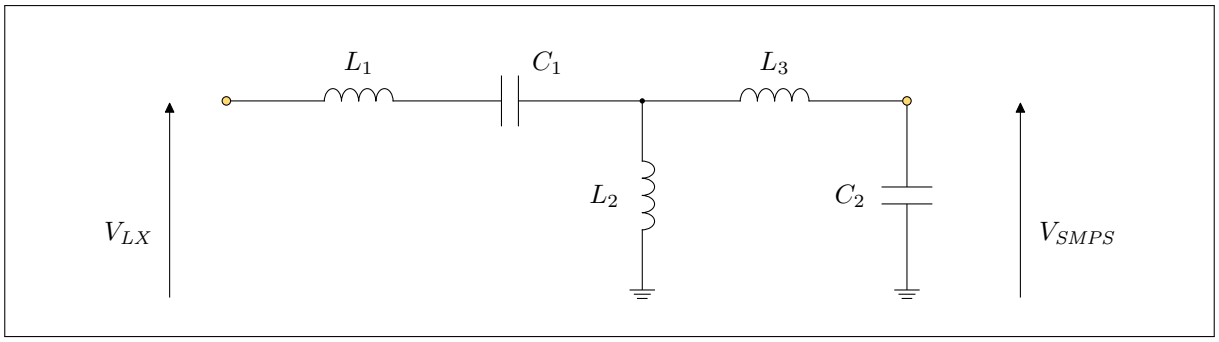


Figure 2.17: High-frequency equivalent circuit for the output filter.

equivalent circuit are:

- L_1, the total parasitic inductance on the series branch of the output filter: the parasitic inductance of the package and PCB traces,
- L_2, the total parasitic inductance on the parallel branch of the output filter: the parasitic inductance of the output capacitor C_{OUT} only as the PCB trace and the via connection to the ground plane are negligible,
- C_1, the parasitic capacitance of the output inductor L_{OUT}.

For this simple equivalent circuit, the transfer function $H(s)$ gives one pole ω_{p0},

$$H(s) = \frac{s^2 L_2 C_1}{1 + s^2(L_1 + L_2)C_1} \quad \rightarrow \quad \omega_{p0} = \frac{1}{\sqrt{(L_1 + L_2)C_1}}. \tag{2.15}$$

The filter frequency response is affected by the load connected on its output: the LDO regulators and the part of the IC they power. The high-frequency equivalent circuit in this case is depicted in Figure 2.17, with:

- L_3, the total parasitic inductance on the feedback branch: the parasitic inductance of the PCB traces and package,
- C_2, the equivalent parasitic capacitance of the IC load.

The analysis of the frequency response for this equivalent circuit is more complex and detailed in Appendix A. The transfer function possesses one zero ω_z and two poles ω_{p1}, ω_{p2}. In our case $C_1 \ll C_2$, poles can be simplified to obtain:

$$\omega_z = 1/\sqrt{L_3 C_2} \tag{2.16}$$

$$\omega_{p1} = \frac{1}{\sqrt{(L_2 + L_3)C_2}} \quad \omega_{p2} = \frac{1}{\sqrt{(L_1 + L_2 /\!/ L_3)C_1}} \tag{2.17}$$

Based on the parasitic elements values presented in 2.11, summed-up from the previous subsection, it is possible to calculate the frequencies of expected resonances in the EMI spectrum. For the first high-frequency model, ignoring the IC load, (2.15) gives:

$$f_{p0} = 1.26\,\text{GHz} \tag{2.18}$$

For the second high-frequency model, taking into account the IC load, (2.16) and (2.17) give:

$$f_z \approx 215\,\text{MHz} \quad ; \quad f_{p1} \approx 186\,\text{MHz} \quad ; \quad f_{p2} = 1.27\,\text{GHz} \tag{2.19}$$

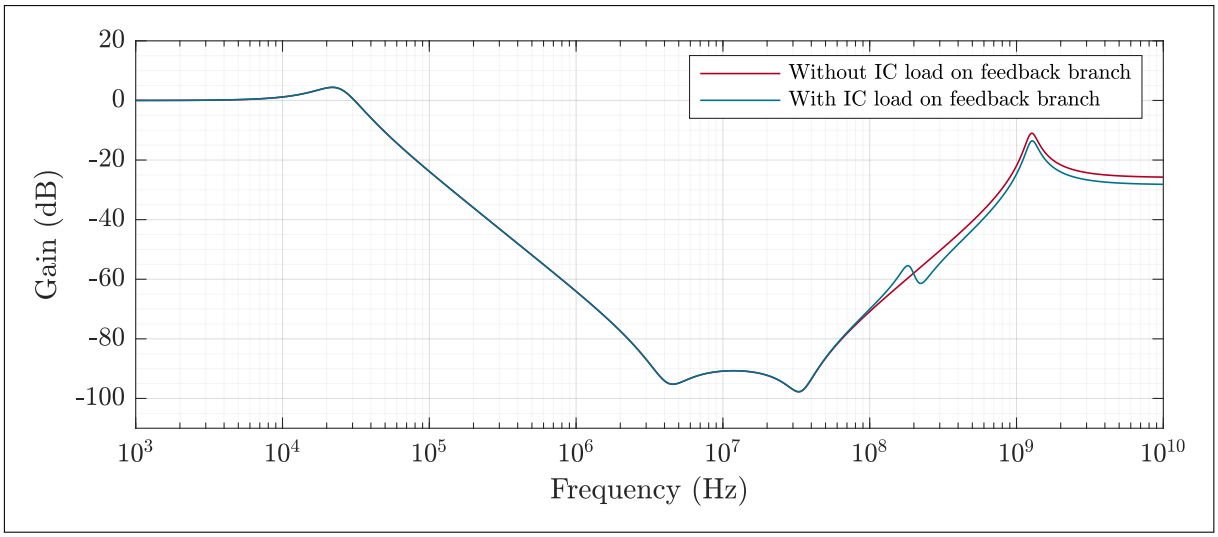


Figure 2.18: Simulated frequency response of the output filter.

On this test board, the values of L_2 and $L_2 /\!\!/ L_3$ are close, and negligible comparing to L_1. For this reason, both equations gives very close results for the high-frequency resonance. When the IC load is taken into account, a lower resonance is to be expected, but difficult to determine because the IC equivalent capacitive load is difficult to estimate.

Figure 2.18 displays the filter response, with or without a 50 pF (estimation for C_1) load on the feedback branch. The estimated value for the parasitic inductance (L_2 and L_3)

$L_1 = 6.90\,\text{nH}$	Package bond wire and lead on V_{LX}	1.72 nH
	PCB trace from V_{LX} to L_{OUT}	3.68 nH
	PCB trace from L_{OUT} to C_{OUT}	1.50 nH
$L_2 = 370\,\text{pH}$	Output capacitor parasitic inductance	370 pH
$L_3 = 1.10\,\text{nH}$	PCB trace from C_{OUT} to V_{SMPS}	522 pH
	Package bond wire and lead on V_{SMPS}	573 pH
$C_1 = 2.19\,\text{pF}$	Output inductor parasitic capacitance	2.19 pF
$C_2 \approx 500\,\text{pF}$	IC equivalent capacitive load	$\sim$ 500 pF

Table 2.11: Estimation of the main parasitic elements implied in the high-frequency resonance.

involved in the lower resonance at f_{p1} are rather small (very short traces) and should not be much smaller in another system. Therefore, the resonance linked to this phenomena should not come close to the BLE band and is is not a major concern in this study. However, the higher resonance at f_{p2} is more problematic: it is located close to the BLE band, increasing the in band noise level, and could be located at an higher frequency for different external components or PCB layout (here L_{OUT} is placed far away, increasing trace length).

Filter response circuit simulation

The power stage and its environment is simulated using Cadence Spectre, now with the output filter modeled with its parasitic elements.

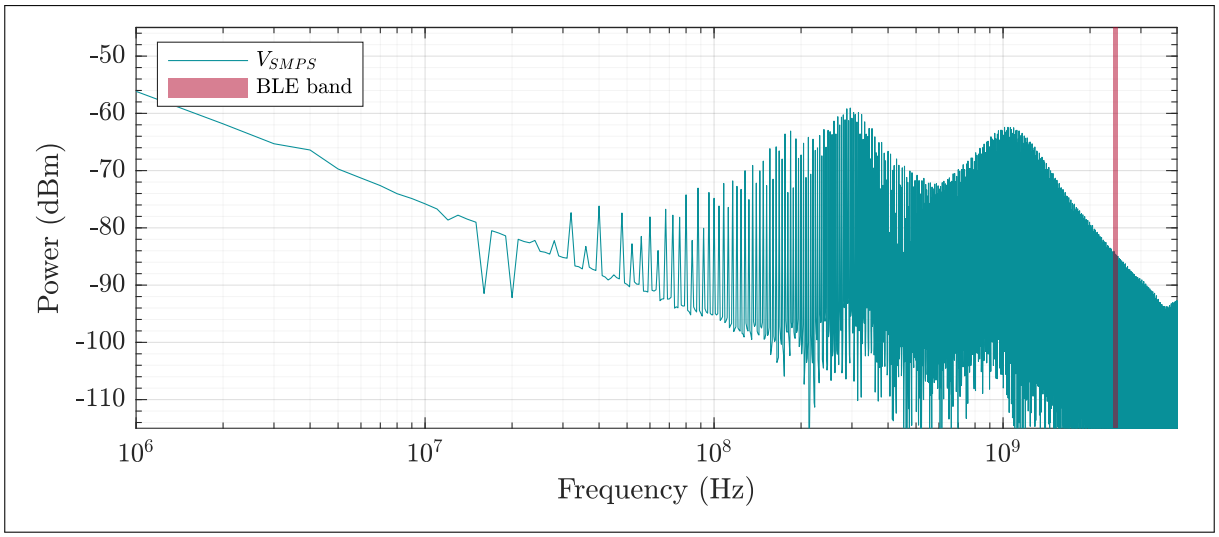


Figure 2.19: Simulated EMI spectrum on the SMPS output voltage V_{SMPS}.

Figure 2.19 displays the simulated EMI on the SMPS output voltage V_{SMPS}. The noise power in the BLE band reach $-84\,\text{dBm}$, while it reached only $-110\,\text{dBm}$ when only the phenomenon presented in the previous subsection was considered[13] (cf. Figure 2.14). The resonance due to the first phenomenon presented in 2.2.2 is visible around 300 MHz. The low resonance linked to the IC load is visible around 200 MHz. The second resonance coming from parasitic elements in the external output filter is present and located around 1.2 GHz as predicted. These simulations demonstrate that the resonance linked to the output inductor parasitic capacitance increase considerably the noise level in the BLE band, and might be an issue for the correct reception of a BLE signal.

2.3 Key Findings and discussion

This chapter covered the analysis of EMI produced by the non-linear operation of the SMPS. This study is required to comprehend how interferences affect the performance of the BLE receiver. A theoretical analysis coupled with circuit-level simulations of the studied system allows the identification of two distinct phenomena related to the generation of EMI:

- Current discontinuities at the SMPS power supply terminals V^+ and V^- (cf. Figure 2.12): fast current transients in parasitic inductances cause voltage overshoots across them.
- Voltage discontinuities at the SMPS output terminal V_{LX} (cf. Figure 2.15): the high-frequency content in the voltage pulse signal V_{LX} is not entirely filtered due to the non-ideal high-frequency response of the output filter.

The spectral content of EMI generated by these two phenomena is shaped by several elements of the system causing resonances. The frequencies at which these resonances occur are highly dependent on the values of the main components involved in the two different mechanisms. For the custom test board presented in 2.1.3, the component values are

[13]The EMI spectrum for the previously described phenomenon was performed on V^+ and not V_{SMPS} because it is where the EMI level are the highest.

calculated based on their physical characteristics and geometry, allowing the estimation of the location of the resonant frequencies. Three main resonances are expected:

- For the first phenomenon (current discontinuities), one resonance is expected around 300 MHz mainly due to the resonant network formed by inductances on the power supply path (parasitic inductance of the package bond wires/leads and PCB trace/via) and capacitances present in the integrated power stage (MOSFETs parasitic capacitance and decoupling capacitors).
- For the second phenomenon (current discontinuities), two resonances are expected mainly, due to the SMPS output filter response dominated by parasitic elements at high frequency:
  - A resonance around 200 MHz mainly due to parasitic inductances on the feedback path (mainly the inductance of the package bond wires/leads and PCB trace/via in the feedback branch and in the inductance of the output capacitor) and the capacitive load of the IC.
  - A resonance around 1.2 GHz due to parasitic inductances on the filter path (mainly the inductance of the package bond wires/leads and PCB trace/via in the L_{OUT} branch) and the parasitic capacitance of the output inductor L_{OUT}.

Degradation of the BLE receiver sensitivity by the SMPS activity

In regard to the research problem, the higher-frequency resonance linked to the L_{OUT} parasitic capacitance seems to be a bigger issue: it is located close to the BLE signal, raising the noise level in this frequency band. Depending on the system implementation and the involved component values, the resonance could be located even closer to the 2.4 GHz band.

The impact of out-of-band EMI on the receiver sensitivity cannot be totally neglected nonetheless. The down-conversion stage mainly consists of the mixer, a non-linear stage, and phenomena like inter-modulation can produce components falling into the BLE band [4]. This will be discussed in the following chapters.

What's next?

The theoretical analysis presented in this chapter predicts that the EMI generated by the SMPS spans across a wide range of frequencies and that their spectral content is highly linked to certain elements of the system.

The next chapter focuses on the spectral analysis of EMI measured on a test board embedding the microcontroller and its external components in order to validate the theoretical predictions. Measurements of the BLE receiver sensitivity, linking the degradation of its performance with the spectral content of EMI, are also presented.

Impact on the receiver sensitivity

3

The degradation of the receiver performances due to SMPS-generated EMI is proven by sensitivity measurements. This chapter focuses on several measurements realized on the studied system that highlight the issue.

First, the BLE standard is briefly described and the sensitivity of the receiver is carefully defined. Next, the setups used to measure conducted and radiated EMI, and used to measure the receiver sensitivity are presented. Then, measurement results are displayed, demonstrating the effect of the SMPS operation on the BLE receiver, depending on its operating conditions or output filter response. Finally, important aspects arising from measurements results are discussed.

3.1 The Bluetooth Low Energy receiver

This section presents the most important aspects of the BLE standard regarding this work, including the BLE signal characteristics, the receiver performances and the method employed to determine the receiver sensitivity.

3.1.1 Bluetooth Low Energy standard

Bluetooth is a wireless technology intended for short-distance data transmission between devices, initially developed by Ericsson Mobile in 1989. The Low Energy version is optimized for low power consumption in battery-powered devices requiring extended battery life.

The Bluetooth Low Energy standard operates in the unlicensed 2.4 GHz Industrial, Scientific & Medical (ISM) band spanning between 2400 MHz and 2483.5 MHz. It utilizes 40 RF channels with center frequencies separated by 2 MHz between 2402 MHz and 2480 MHz. A frequency hopping transceiver is used to overcome interference and fading.

Two modulation schemes are defined: a mandatory modulation scheme using a symbol rate of 1 Msym/s, and an optional modulation scheme using a symbol rate of 2 Msym/s. Both modulation schemes are available on the studied microcontroller, but only the 1 Msym/s modulation is employed here. The 1 Msym/s modulation supports two physical layers (uncoded or coded data). Only the mandatory physical layer with uncoded data at 1 Mbit/s is employed for measurements or simulation in this work.

Signal characteristics

To minimize the transceiver complexity, the BLE standard employs a shaped binary frequency modulation. More specifically, a Gaussian Frequency Shift Keying (GFSK)

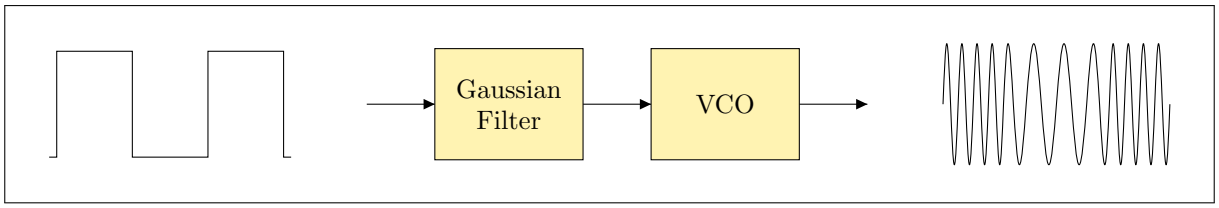


Figure 3.1: Exemple of GFSK modulation using a Gaussian filter and a VCO.

modulation with a bandwidth/bit-period product BT = 0.5. For uncoded data at 1 Mbit/s, the bandwidth B is 500 kHz and the bit-period T is 1 ms. The modulation index must be comprise between 0.45 and 0.55.

A binary one is represented by a positive frequency deviation, whereas a binary zero is be represented by a negative frequency deviation. For uncoded data at 1 Mbit/s, the frequency deviation is typically $\Delta f = \pm$ 250 kHz and shall never be less than $\pm$ 185 kHz. Figure 3.1 displays a simple way to obtain a GFSK modulated signal from data bits, using a Gaussian filter and a voltage controlled oscillator (VCO).

Receiver performances

The receiver takes the modulated 2.4 GHz BLE signal as input and provides the corresponding demodulated data bits at 1 Mbit/s. In the studied microcontroller, the 2.4 GHz BLE signal is first down-converted to an intermediate frequency IF = 1.6 MHz by the analog part of the receiver, then converted to a digital signal using an analog-to-digital converter (ADC), and finally demodulated by a digital demodulator. The receiver performances are defined by several characteristics listed here:

- Receiver sensitivity: this is the most important characteristic, it determines the weakest signal the receiver can successfully "understand".
- Co-channel or adjacent channel interference performance: the receiver performance is evaluated in the presence of interference from other BLE transmissions in the co-channel or adjacent channels.
- Out-of-band blocking performance: the receiver performance is evaluated in the presence of interference from other wireless transmissions outside the ISM band.
- Intermodulation performance: the receiver performance is evaluated in the presence of interference due to intermodulation produced by two or more transmitters.
- Maximum usable input level: the receiver performance is evaluated in the presence of relatively strong signals that can occur due to spatial proximity between devices.

System measurements revealed a degradation of the receiver sensitivity linked to the SMPS operation. The sensitivity is defined in the following subsection.

3.1.2 Sensitivity of the receiver

The sensitivity is defined as the minimum signal power $P_{sig,sen}$ that the receiver can detect with "acceptable quality" [4]. Figure 3.2 presents the main elements defining the sensitivity of the demodulation chain (from the BLE signal to the data bits). The numerical values corresponds to the studied system. For the BLE standard, the quality of the demodulated signal is characterized by its bit error ratio

$$BER = \frac{number\ of\ incorrect\ bits}{total\ number\ of\ bits\ transferred}. \tag{3.1}$$

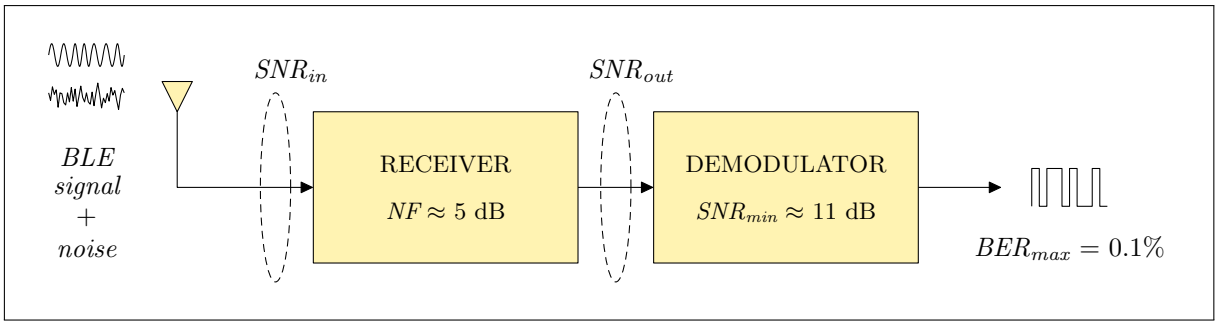


Figure 3.2: Main elements in the system defining the receiver sensitivity.

The maximum BER accepted by the standard is $BER_{max} = 10^{-3}$, one incorrect bit for a thousand bits [32, 33]. To achieve the required BER, the demodulator necessitates a sufficient signal-to-noise ratio SNR_{min} at its input. The required SNR depends on the type of modulation (specified by the BLE standard) and the architecture of the implemented demodulator. For our system we have

$$SNR_{min} = 11\,\text{dB}. \tag{3.2}$$

If we consider a noiseless receiver, the only noise contributor is the one present at the input of the receiver. Because of the thermal agitation of charged particles, the natural environment surrounding the receiver emits radio waves (black-body radiation). The antenna is constantly receiving a "background noise". In receiver design, the background noise collected by the antenna is commonly modelled by a single resistive white noise source, with a power spectral density (PSD) of $4kTR_{antenna}$, where k is the Boltzmann constant ($\approx 1.38 \times 10^{-23}\,\text{J K}^{-1}$) and T the absolute temperature in kelvin. When the receiver is matched to the antenna, we have

$$PSD_{noise}\,|_{\text{dBm/Hz}} = 10 * \log(kT) \approx -174\ \text{dBm/Hz at } 300\,\text{K}. \tag{3.3}$$

The background noise power P_{noise} actually seen by the demodulator is limited by the equivalent bandwidth BW of the receiver. In our case, the bandwidth is defined by the IF complex band pass filter and is equal to 1.6 MHz. The corresponding noise power is

$$P_{noise}\,|_{\text{dBm}} = -174\ \text{dBm/Hz} + 10\log BW = -112\,\text{dBm}. \tag{3.4}$$

The analog circuit achieving the down-conversion, ahead the demodulator, is not perfect and adds a certain amount of noise to the signal. This added noise characterised by the noise figure NF, and is evaluated at approximately 5 dB in our system. It is defined as

$$NF|_{\text{dB}} = 10 * \log\left(\frac{SNR_{in}}{SNR_{out}}\right) = 10 * \log\left(\frac{P_{sig}/P_{noise}}{SNR_{out}}\right). \tag{3.5}$$

From the equations (3.4) and (3.5), we can write the minimum signal power $P_{sig,sen}$ that the receiver can detect (i.e. the sensitivity)

$$P_{sig,sen}\,|_{\text{dBm}} = -174\,\text{dBm/Hz} + 10\log BW + NF|_{\text{dB}} + SNR_{min}\,|_{\text{dB}}. \tag{3.6}$$

The three first terms represent the total integrated noise of the system, also called the "noise floor". The presence of extra noise at the receiver input, or inside the receiver leads to a degradation of the sensitivity. For our system we have

$$P_{sig,sen}\,|_{\text{dBm}} = -174\,\text{dBm/Hz} + 10\log\left(1.6 \times 10^6\,\text{Hz}\right) + 5\,\text{dB} + 11\,\text{dB} = -96\,\text{dBm}. \tag{3.7}$$

Quantity	Level	Power	RMS voltage	Peak-to-peak
Value	$-96\,\text{dBm}\vert_{50\,\Omega}$	251 fW	$3.54\,\mu\text{V}_{\text{RMS}}$	$10.0\,\mu\text{V}_{\text{PP}}$

Table 3.1: Level, power and amplitude of the BLE signal at the receiver sensitivity.

Table 3.1 gives the corresponding power and amplitude for a signal level of $-96\,\text{dBm}$, sensed by a $50\,\Omega$ antenna, or generated by a $50\,\Omega$ source. This is the smallest signal that the receiver is able to demodulate correctly.

What happened when the SMPS is active?

When the SMPS is active and generates electromagnetic interference, the BLE signal can be corrupted by noise either before entering the microcontroller RF inputs, due to coupling on the PCB, or inside the receiver circuitry, trough grounds and power supplies, or different couplings. Either way, the noise floor is raised, and the SNR at the demodulator input reduced. In (3.6), it can be seen as if the noise factor NF of the receiver is increased by the SMPS operation. Thus, the minimal power $P_{sig,sen}$ of the signal that the receiver can demodulate correctly (i.e. the sensitivity) is increased.

Direct test mode

The Bluetooth standard defines a "direct test mode" for BLE. It enables the physical layer to be characterized by sending or receiving test packet sequences. The direct test mode bypasses the host stack and communicates with the physical layer directly. The device under test (DUT) can be controlled via a serial bus (UART or USB), and using special commands for the host controller interface (HCI). The DUT can thus be controlled by a computer or a specialized tester.

The standard specifies the test packets to be used for each test case in order to facilitate the tests and ensure reproducibility. To test a receiver sensitivity for a BER = 10^{-3}, and for uncoded data at 1 Mbits/s, a minimum of 1500 packets with a payload[1] of 37 bytes needs to be transmitted, giving 296 bits of payload.

Packet error ratio

In direct test mode, the sensitivity of the receiver is determined by the DUT returning the packet error ratio (PER) to the tester. The power of the transmitted RF signal is lowered until the PER reaches a certain limit. The PER is defined as

$$PER = \frac{number\ of\ incorrect\ data\ packets}{total\ number\ of\ data\ packets\ transferred}. \tag{3.8}$$

The packet error probability p_p is linked to the bit error probability p_b and depends on the number of bits per packet N

$$p_p = 1 - (1 - p_b)^N. \tag{3.9}$$

A packet is composed by 8 bits of preamble, 32 bits of sync word, 16 bits defining the packet type, a variable length payload (296 bits in our case) and 24 bits of cyclic redundancy check (CRC). Except for the 8 preamble bits, any bit error leads to the lost of the

[1]The bit pattern of the payload is a pseudorandom bit pattern with a length of $2^9 - 1$, called PRBS9.

packet. Thus, the number of significant bits per packet is $N = 368$ bits. We can determinate the maximum admissible packet error rate PER_{max} corresponding to a BER_{max} of 0.1%

$$PER_{max} = 1 - (1 - BER_{max})^N \approx 30.8\%. \tag{3.10}$$

3.2 Measurement setups

This section presents the setups used to realize different type of measurements on the test boards presented in 2.1.3 and embedding the STM32WB55. These measurements showcase the EMI generated by the integrated SMPS as well as their impact: conducted EMI propagating on the PCB, near field radiated EMI above the surface of the PCB, and BLE receiver sensitivity. Main results obtained with the setups are presented in the next section.

It is possible to write in dedicated registers of the microcontroller to configure the integrated SMPS [34]. It can be enabled or disabled, its switching frequency can be chosen between 4 MHz or 8 MHz and its output voltage can be adjusted from 1.2 V to 1.95 V.

3.2.1 Conducted electromagnetic interference

Figure 3.3 depicts the experimental setup employed to analyze the spectral content of the EMI caused by the SMPS operation. On the custom test board, EMI are measured at the SMPS input V_{DD} and output V_{SMPS}, thanks to the 50 Ω traces and SMA connectors.

The spectrum analyzer (Rohde & Schwarz FSV3013) can be connected to the SMA connectors, allowing non-intrusive high-frequency measurements. The main power for the microcontroller test board is provided by an external DC power supply and allow measurements for the whole supply range[2]. A current source (Keithley SourceMeter) is connected to the SMPS output in order to simulate a higher current consumption from

[2]The microcontroller power supply range varies from 1.71 V to 3.6 V but is limited between 2.0 V to 3.6 V when the SMPS is enabled.

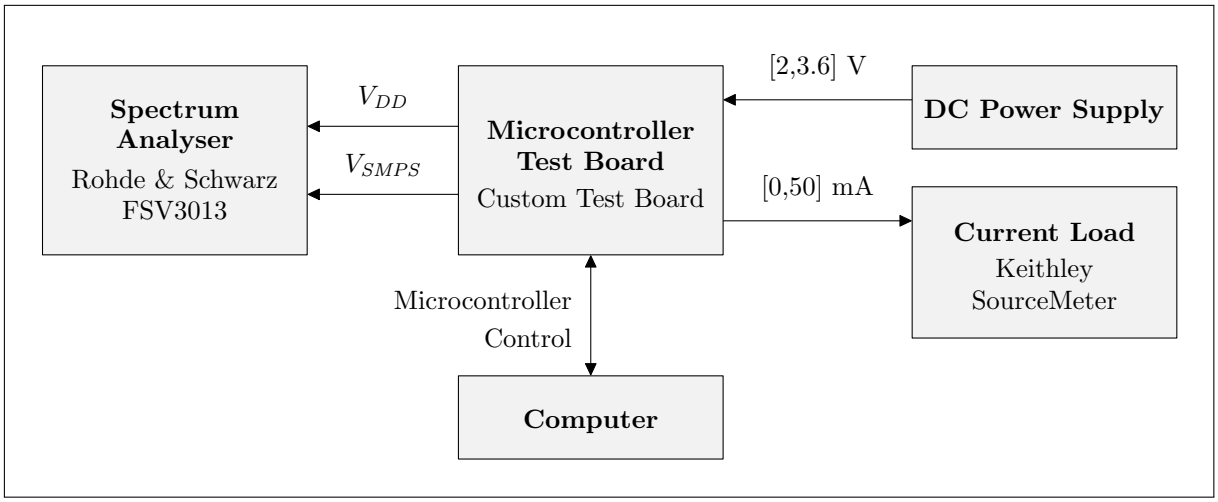


Figure 3.3: Experimental setup for the spectral analysis of conducted EMI on the PCB.

the microcontroller[3].

The microcontroller is controlled via a laptop (USB to UART connection), and with the direct test mode programmed in its host CPU, it can be set in Rx mode. Even without a BLE signal injected at the RF input, the receiver chain is functioning normally, trying to recover data by demodulating the environment noise sensed at its input. Therefore, the gain of each stage of the receiver are set to their maximum by the automatic gain control (AGC). These are the same conditions as when the receiver is demodulating a very small BLE signal, close to its sensitivity.

3.2.2 Radiated electromagnetic interference

Figure 3.4 illustrates the experimental setup employed to measure the near-field radiated EMI above the PCB, around the microcontroller and its external components. These measurements have been realized at NEXIO Rhône-Alpes using their BAT-Scanner.

The scanner determines the spatial distribution of the electromagnetic field (in the near-field region) by displacing a field probe above the surface of the test board. The separation between the scanned surface and the probe is around 1 mm. Signal processing based on fast Fourier transform is used to extract the frequency content of the near-field emission.

3.2.3 Receiver sensitivity

Figure 3.5 depicts the experimental setup employed to measure the receiver sensitivity for each BLE channels. A specialized tester is utilized, the Rohde & Schwarz CMW270

[3]The maximum current the SMPS is able to deliver is 80 mA.

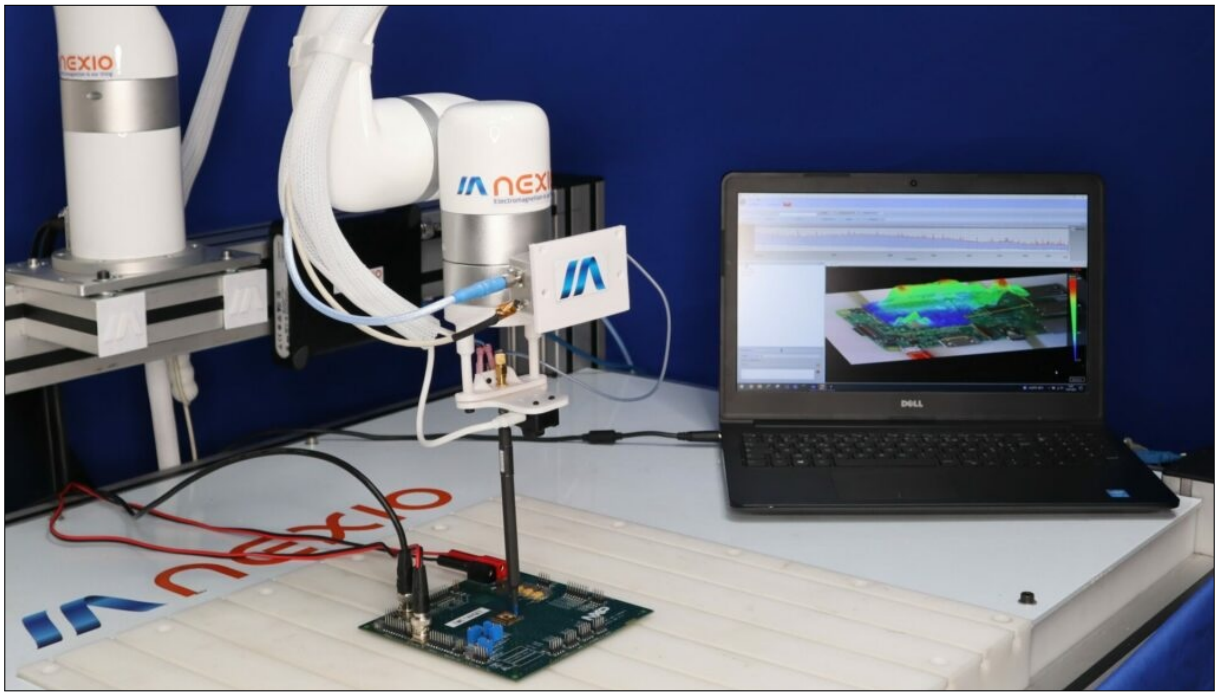


Figure 3.4: The BAT-Scanner from NEXIO, a EMI near-field scanner (representative picture of the setup).

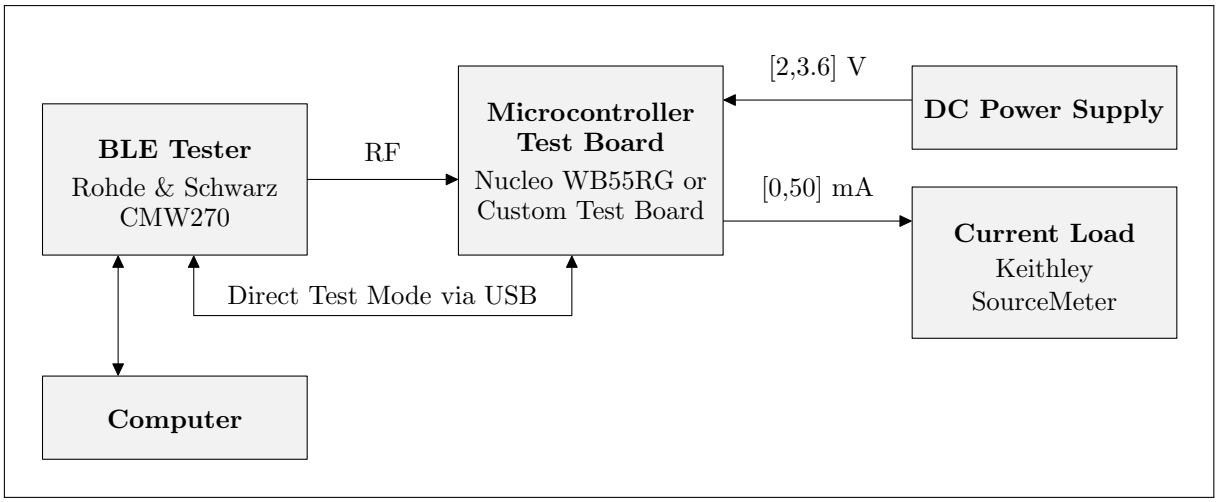


Figure 3.5: Experimental setup for the measurement of the BLE receiver sensitivity.

wireless connectivity tester. With the direct test mode programmed in the host CPU, the tester can communicate with the microcontroller through a USB connection to configure it to be ready for the desired characterization test, and automate the test. In our case, we are testing receiver sensitivity for uncoded data at 1 Msym/s (as defined in the BLE standard).

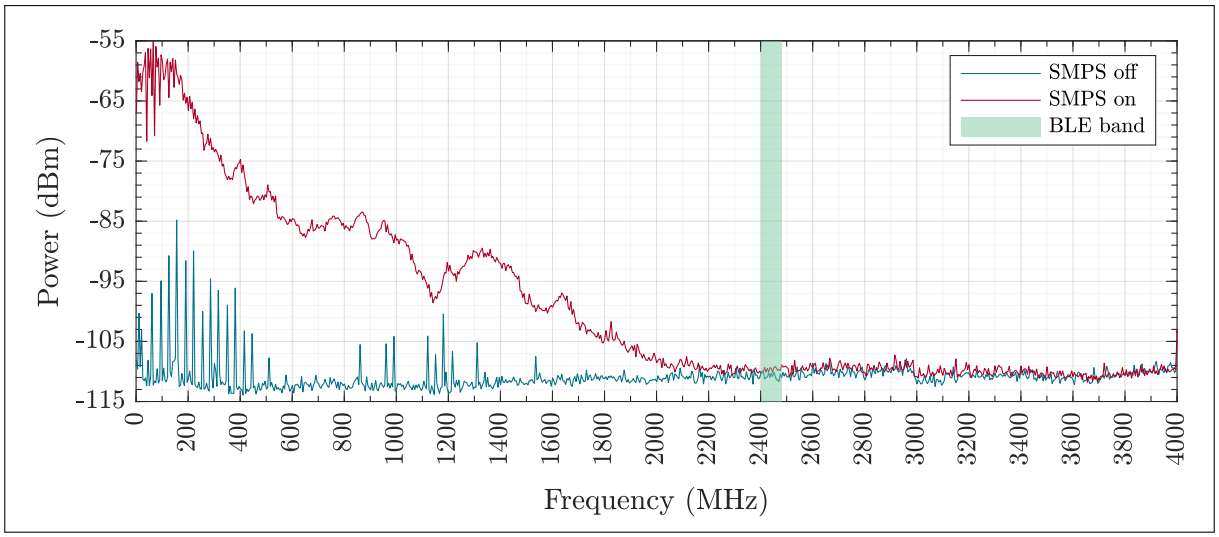
The tester sends predefined test packets to the microcontroller. The RF output of the tester is directly connected to the RF input on the microcontroller, via a coaxial cable and SMA connectors. Because the test packets are predefined by the BLE standard, the microcontroller knows the content it should receive for each packet. The microcontroller counts how many packets contain at least one incorrect bit and returns the PER to the tester. The power of the BLE signal is lowered until the sensitivity is reached, that is until $PER \geq PER_{max}$.

The BLE standard indicates at least 1500 packets of 296 bits are necessary for this test, giving 444,000 bits per PER measurements. At a data rate of 1 Mb/s, this corresponds to 444 ms for each PER measurement at a certain BLE signal power and repeated until the sensitivity is reached, and for every BLE channels. Depending on the signal power step and how far from the sensitivity the measurement starts, the total time duration to determine the sensitivity of the 40 BLE channel vary from approximately 5 min to 20 min. It is a relatively long measurement, difficult to simulate at circuit level.

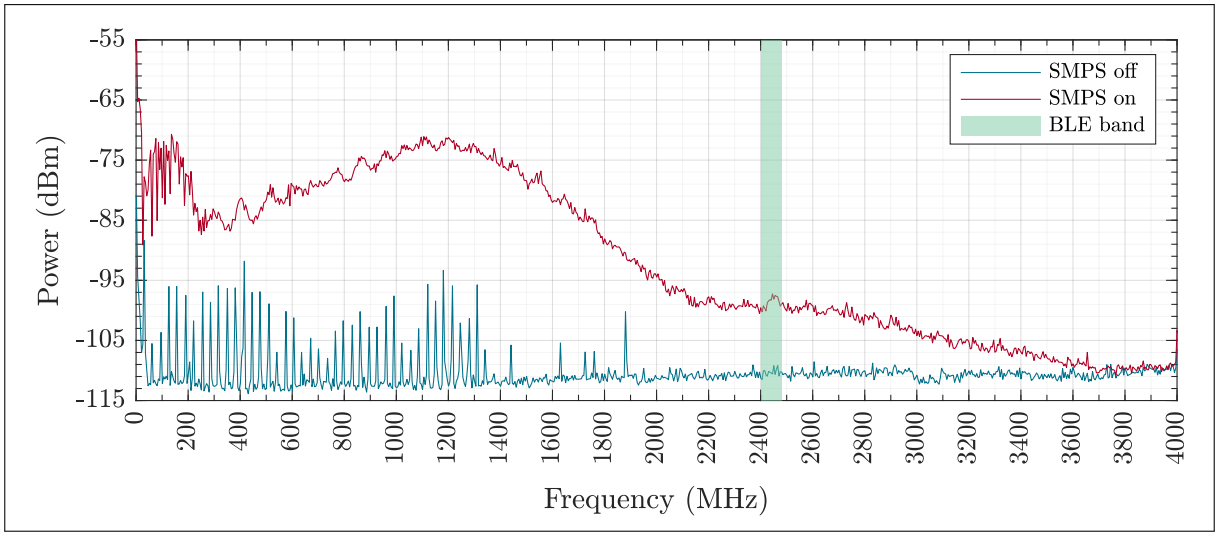
The DC power supply and the current load allow to measure the receiver sensitivity under different operating conditions (microcontroller main power supply and power consumption).

3.3 Main results

This section exhibits some of the main results obtained with the setups presented beforehand. These results demonstrate the influence of different parameters such as the SMPS operating conditions or external filter on the generated EMI, and therefore, on the degradation of the receiver sensitivity.



(a)



(b)

Figure 3.6: EMI spectrum measured on the custom test board for $V_{DD} = 3.3\,\text{V}$ and $V_{SMPS} = 1.4\,\text{V}$ at (a) the SMPS input V_{DD} and (b) the SMPS output V_{SMPS}.

3.3.1 SMPS operation

By enabling or disabling the SMPS, it is possible to observe the interference it generates. Here are presented conducted and radiated EMI measured on the test boards, depending on the SMPS status.

Conducted EMI on PCB

Figure 3.6 displays the electromagnetic interference propagating at the SMPS input V_{DD} and output V_{SMPS}, measured on the custom test board via the $50\,\Omega$ traces and SMA connectors.

When the SMPS is disabled (blue spectrum in Figure 3.6(a) and 3.6(a)), we are at the spectrum analyzer noise floor. The 32 MHz fundamental and its harmonics raising above the measurement noise floor at the SMPS input and output are due to the 32 MHz crystal

embedded on the PCB and used by the microcontroller to generates digital clocks. These signal are present at the SMPS input and output because of couplings at PCB level.

When the SMPS is enabled (red spectrum in Figure 3.6(a) and 3.6(a)), a first resonance located approximately at 100 MHz is visible in both the SMPS input and output. The measured amplitude of this resonance is higher at the SMPS input V_{DD}. A second resonance located approximately at 1.2 GHz is visible this time only at the SMPS output V_{SMPS}, causing an increase in the noise power around these frequencies and until the BLE signal frequency band.This demonstrates that the SMPS, functioning at a switching frequency of 4MHz, generates EMI with a spectral content spreading as far as approximately 3.6 GHz. This is higher than the BLE operating frequency band, located between 2400 MHz and 2483 MHz.

Based on the analysis of the phenomena implied in EMI generation presented in 2.2.2 and 2.2.3, we can identify these two resonances:

- The lower resonant frequency ($\sim$ 100 MHz) is caused by the current discontinuities on the positive and negative SMPS power supply V^+ and V^-. The resonance is present on the power stage output node V_{LX} and filtered by the SMPS output filter, explaining why its amplitude is lower on V_{SMPS} than V_{DD}. The value of the measured resonant frequency is lower than the expected value of the theoretical analysis, as this value is hard to predict because of the complexity of the resonant network and therefore not all of the implied parasitic elements are taken into account.
- The higher resonant frequency ($\sim$ 1.2 GHz) is caused by the parasitic elements in the output filter affecting its frequency response. The value of the measured resonant frequency matches the expected value of the theoretical analysis ($\sim$ 6 % error).

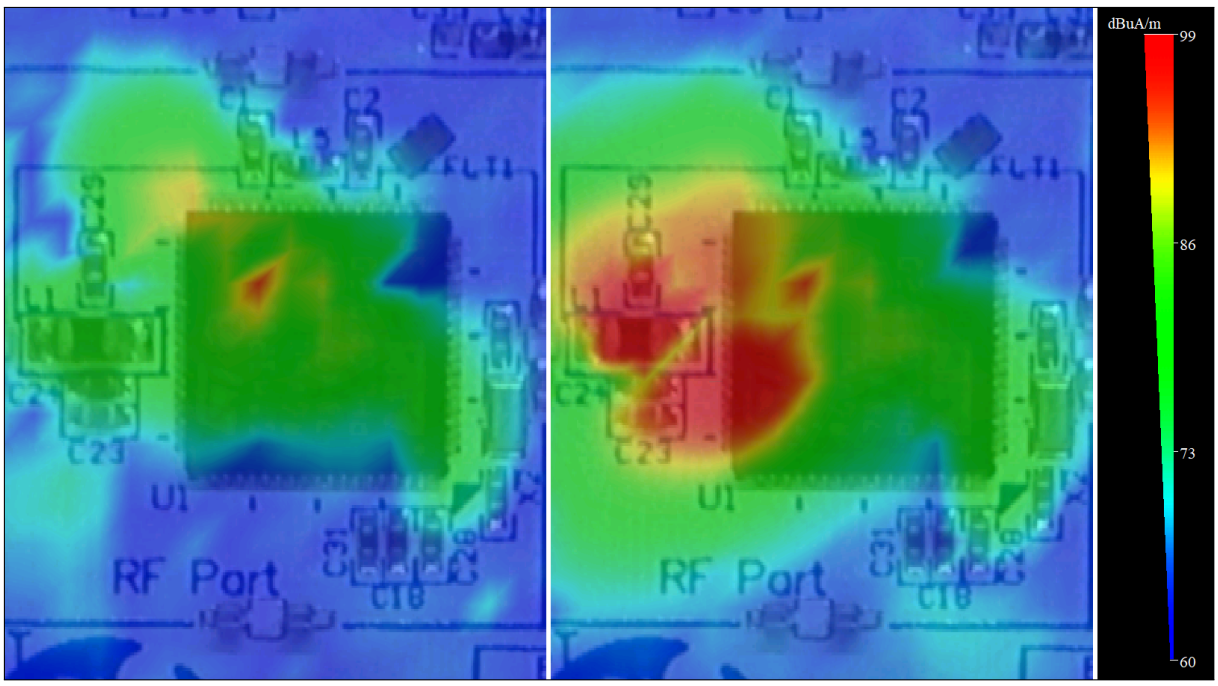
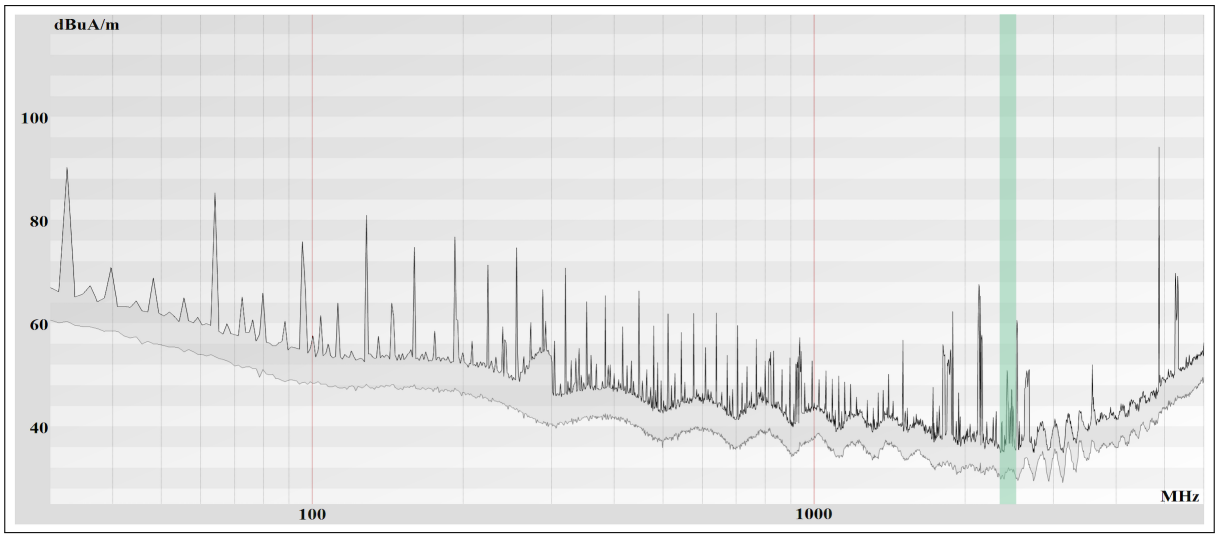
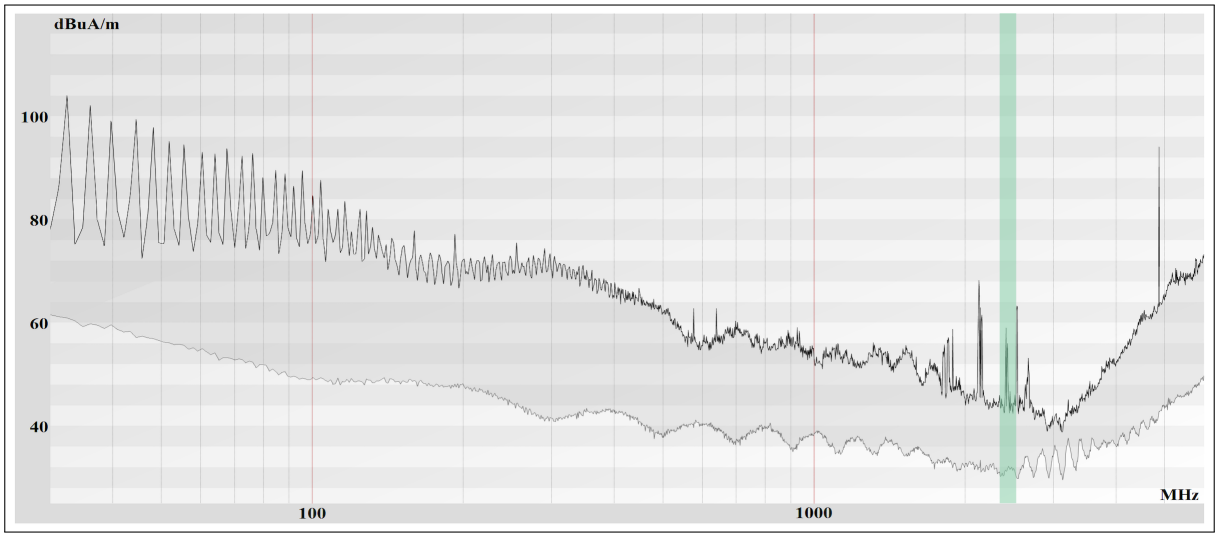


Figure 3.7: Near-field radiated interference map in the region surrounding the microcontroller (left) with the SMPS disabled and (right) with the SMPS enabled.



(a)



(b)

Figure 3.8: Near-field radiated interference spectrum corresponding to the interference map (a) with the SMPS disabled and (b) with the SMPS enabled.

Near-field radiated EMI

Figure 3.7 pictures the near-field radiated interference map above the microcontroller and its external components and Figure 3.8 displays the associated spectral content, whether the SMPS is enabled or not. The measurements were realized on the Nucleo test board. They have not been realized inside a Faraday cage, thus unwanted interference of the environment are visible on the spectra.

When the SMPS is disabled, the main source of near-field radiated emission is the transceiver local oscillator functioning at a frequency around 4.8 GHz. It is measured at the same amplitude whether the SMPS is enabled or not. As it is two times the frequency of the BLE signal, interference coming from this source are filtered out by the receiver and should not be an issue regarding the sensitivity.

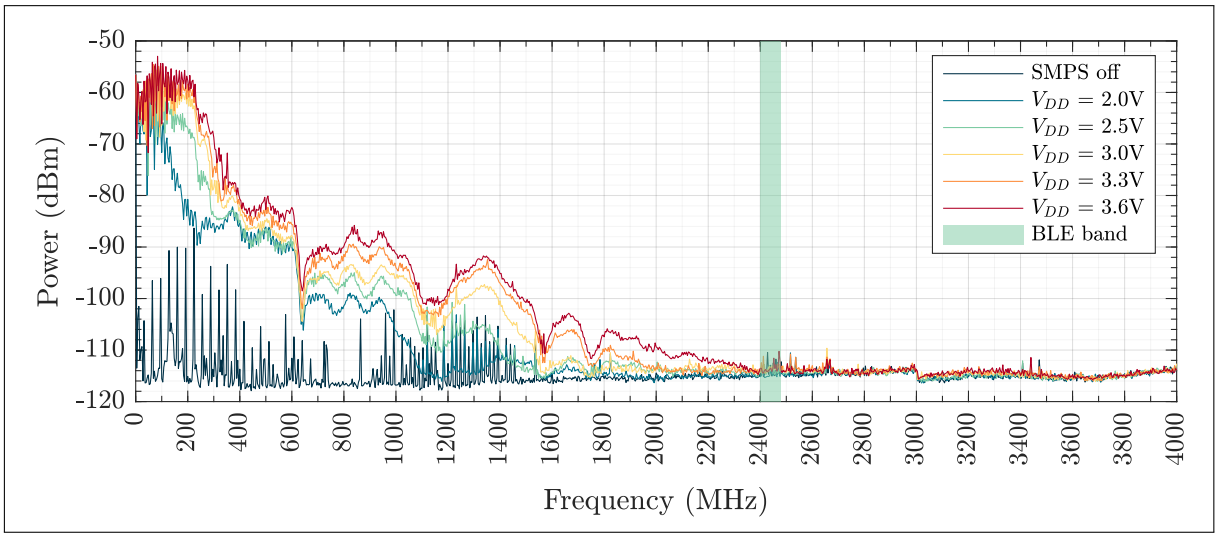
When the SMPS is enabled, the emission map reveals that the strongest sources of radiated interference are now the SMPS power stage and its input/output pins as well

as the SMPS output filter, mostly with its inductor. The spectrum shows the 4 MHz fundamental and its harmonics (SMPS switching frequency), spreading across the entire measured spectrum (1 MHz – 6 GHz) and raising the noise floor.

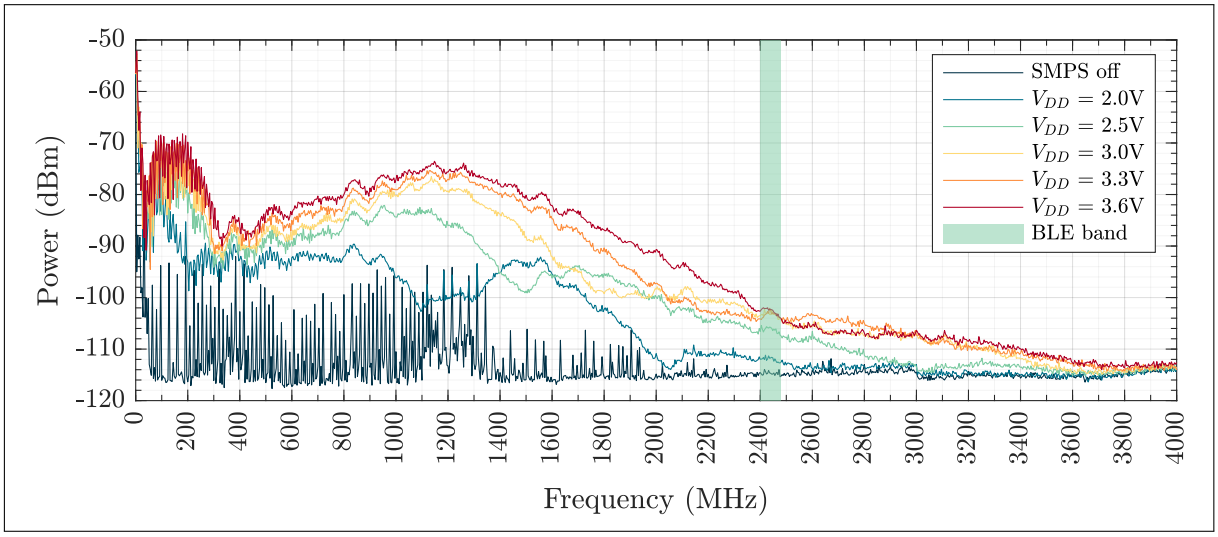
The hypothesis is that the conducted EMI propagating toward the BLE receiver are sufficient to explain the degradation of sensitivity, and the effect of radiated EMI on the receiver sensitivity will not be studied. However these measurements remains interesting as they demonstrates the wide spectrum of radiated EMI caused by the SMPS and the sources of these radiated EMI.

3.3.2 Operating conditions influence

The microcontroller operating conditions affect the generated EMI and consequently, the degradation of the receiver sensitivity. Here are presented measurements of EMI spectra

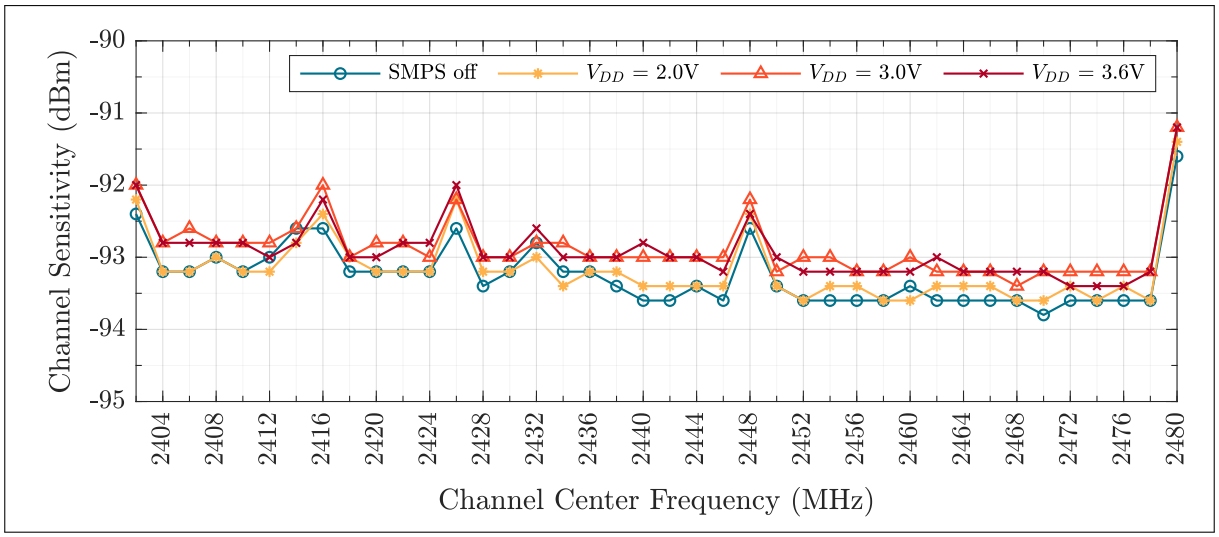


(a)

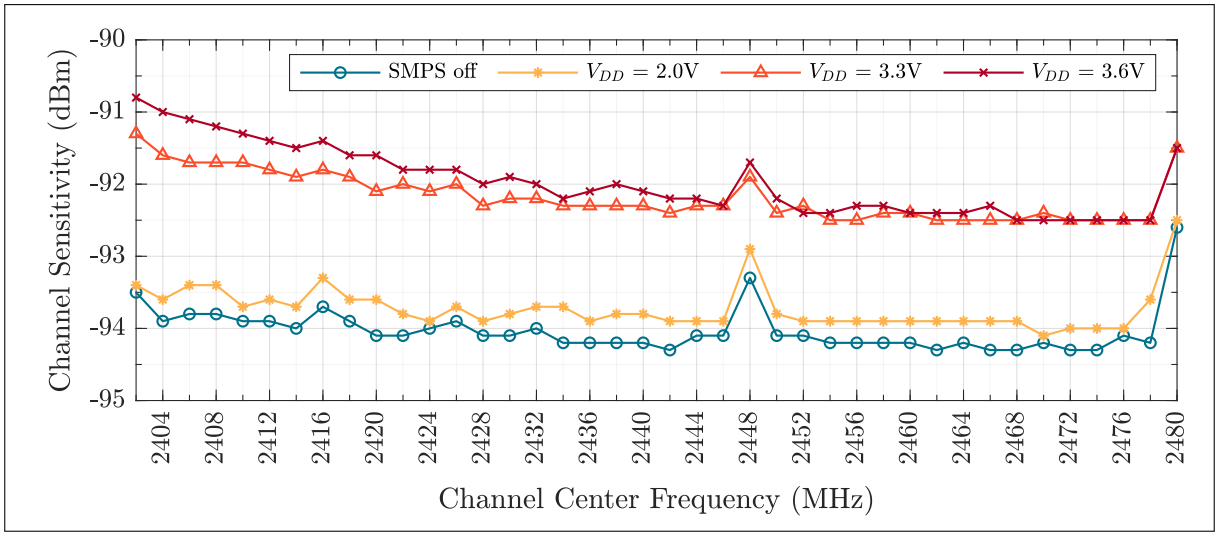


(b)

Figure 3.9: EMI spectrum measured on the custom test board depending on the power supply at (a) the SMPS input V_{DD} and (b) the SMPS output V_{SMPS}.



(a)



(b)

Figure 3.10: Receiver sensitivity per channel depending on the power supply measured on (a) the custom test board and (b) the Nucleo test board.

and receiver sensitivity under different operating conditions such as the microcontroller power supply or current consumption.

Input voltage

Figure 3.9 depicts EMI spectra at the SMPS input and output on the custom test board, depending on the SMPS input voltage V_{DD}. On both nodes, there is a tendency for the EMI amplitude to reduce as the input voltage is lowered. This is explained by the reduced voltage drop on the pulse signal V_{LX} oscillating between V_{DD} and the ground. In the BLE band, the EMI reduction with the input voltage is observable mostly on the the SMPS output V_{SMPS}.

Figure 3.10 presents measurements of the receiver sensitivity for both test boards. Unfortunately, because of the differences between these two boards regarding external passive components and PCB layout, the custom test board (on which it is possible to

measure EMI spectra) exhibit much less impact from the SMPS on its sensitivity. The differences between the test boards explaining this observation will be discuss in the conclusion section of this chapter. An harmonic of the USB clock at 48 MHz is the likely cause of the constant sensitivity loss observed at 2448 MHz.

These results show the correlation between the amplitude of EMI generated by the SMPS and the degradation of the receiver sensitivity: the higher the EMI amplitude, the higher the receiver sensitivity degradation.

Output current load

The measurement set-up allow to artificially increase the current load at the SMPS output as the microcontroller power consumption depends on the application case.

Figure 3.11 depicts EMI spectra measured on the custom test board at the SMPS output V_{SMPS}, depending on the current load I_{LOAD}. Below approximately 1 GHz, EMI amplitude follows the output current load: the higher the current load, the higher the EMI amplitude. Above 1 GHz however, the behavior is more unpredictable and does not follow the previous observation, with various states across frequency bands.

Figure 3.12 depicts the receiver sensitivity measured on the Nucleo test board, depending on its current load I_{LOAD}. The receiver sensitivity versus the SMPS output current load displayed in Figure 3.12(a) presents a similar behavior as the EMI amplitude above 1 GHz: the amplitude does not follow the output current load. Figure 3.12(b) depicts the receiver sensitivity versus the output current load for one BLE channel only chosen arbitrarily (the channel 17 at 2434 MHz) showing more clearly the evolution of the sensitivity with the current load.

This results tends to indicate that the higher frequency content of EMI (above 1 GHz) is responsible for the degradation of the sensitivity.

⚠ EMI and sensitivity measurements have been realized on two different boards as the sensitivity measurement on the custom test board didn't give exploitable results because of the too small variation in EMI amplitude. ⚠

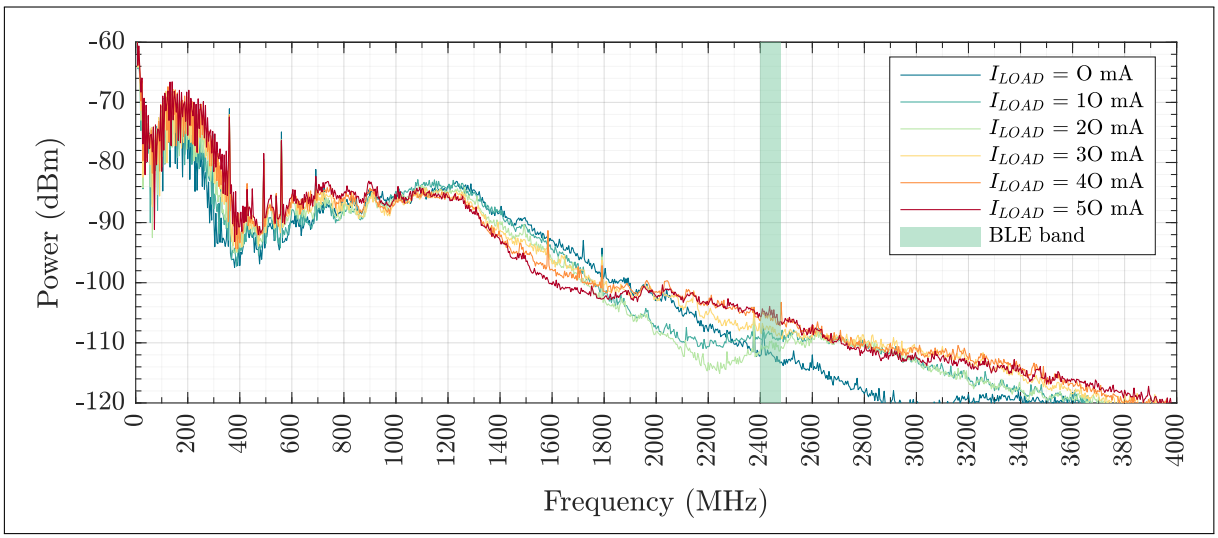
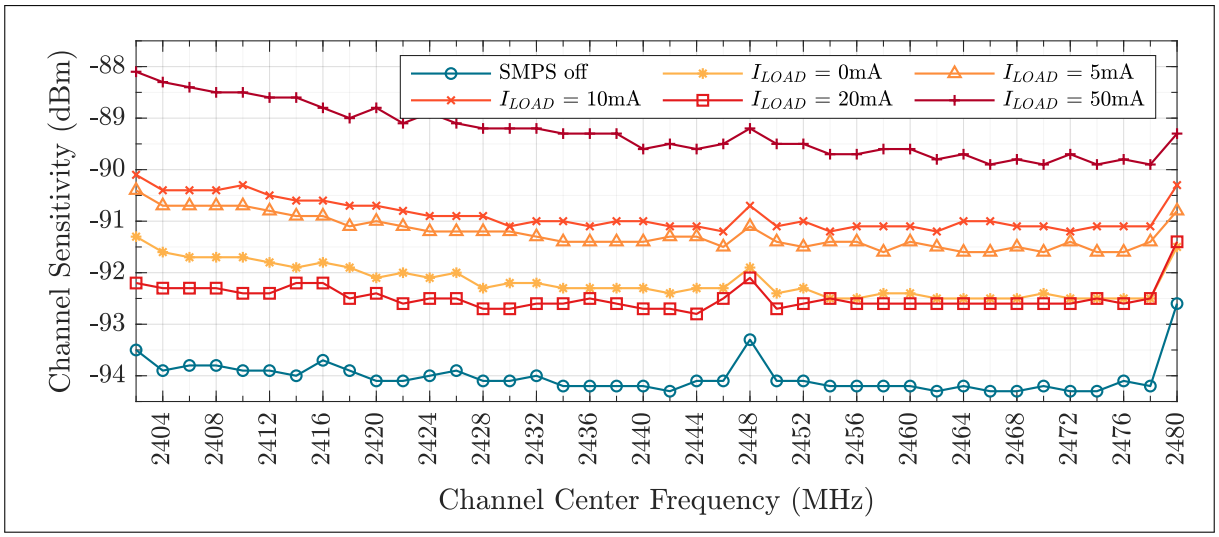
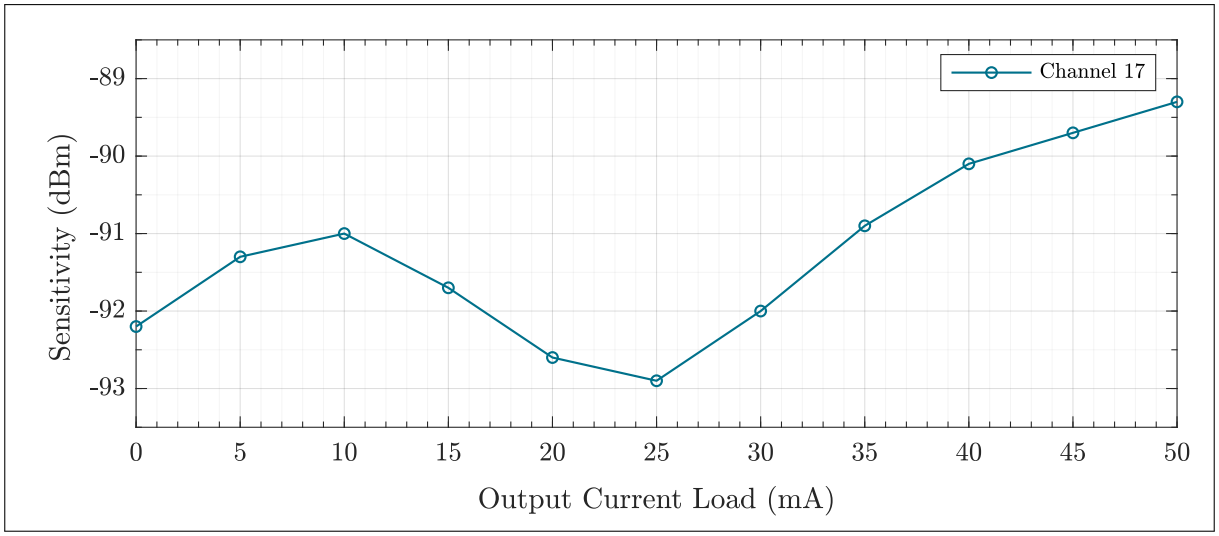


Figure 3.11: EMI spectrum measured on the custom test board at the SMPS output V_{SMPS}, depending on the output current load.



(a)



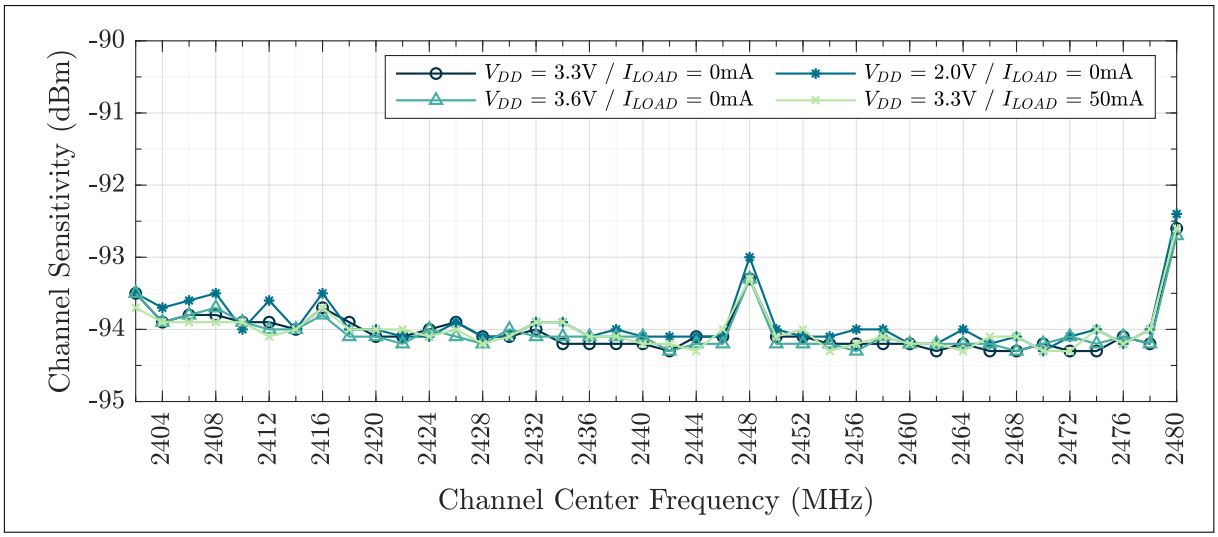
(b)

Figure 3.12: Receiver sensitivity depending versus SMPS output current load on the Nucleo test board (a) for every BLE channels and (b) for the channel 17 (2434 MHz).

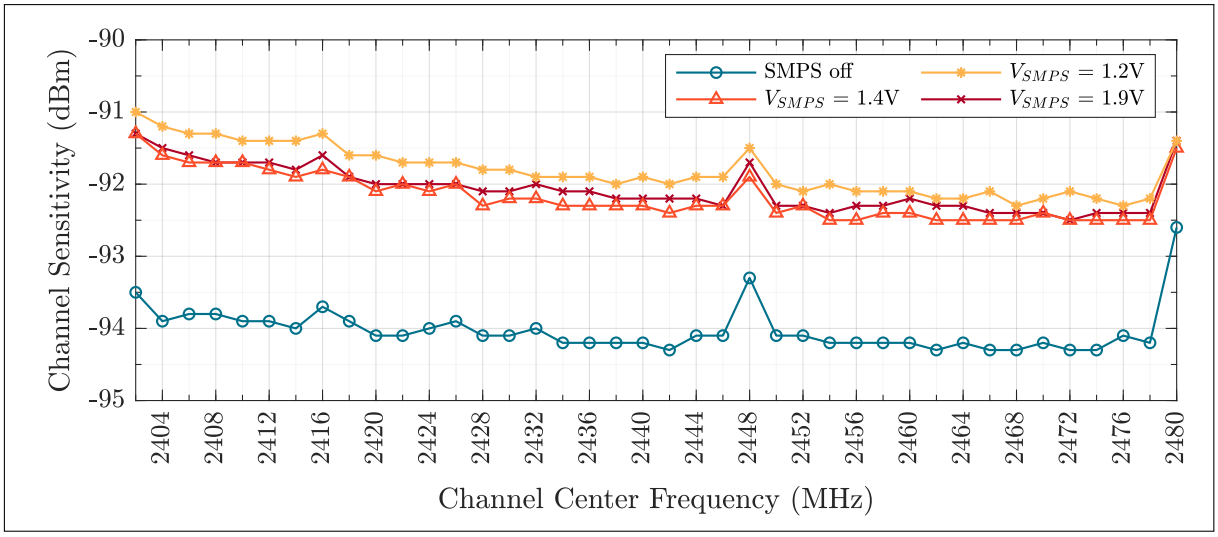
Other parameters

Figure 3.13(a) presents the receiver sensitivity measured on the Nucleo test board when the SMPS is disabled, and for the different operating conditions presented before; it doesn't impact the receiver sensitivity.

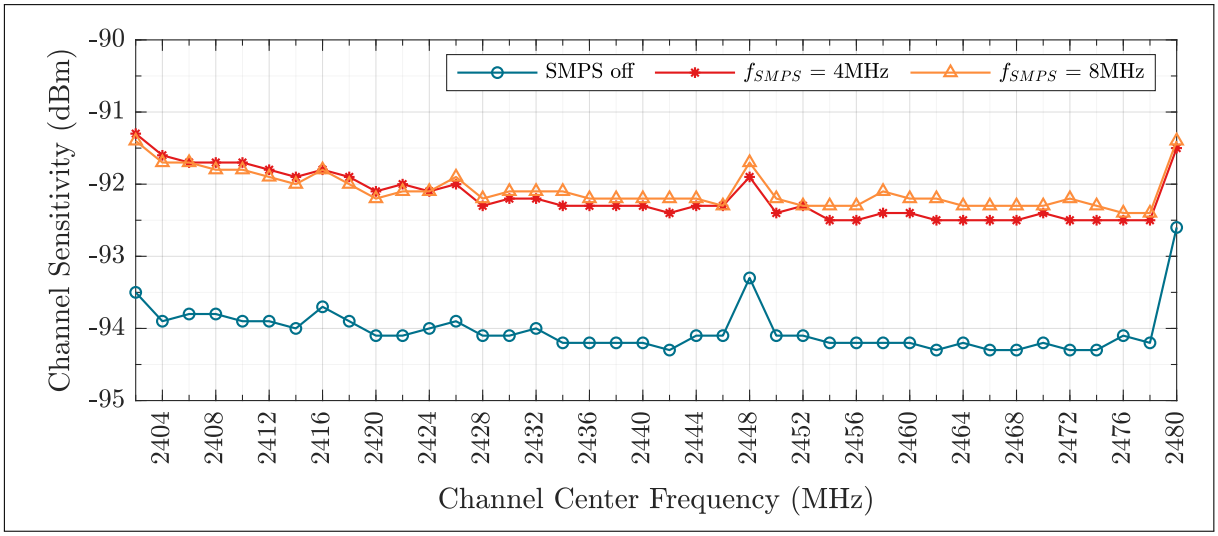
Figure 3.13(b) and 3.13(c) displays respectively the influence of the SMPS output voltage value and the SMPS switching frequency on the receiver sensitivity. These parameters have a very limited influence on the degradation of the receiver sensitivity.



(a)



(b)



(c)

Figure 3.13: Receiver sensitivity on the Nucleo test board (a) when the SMPS is disabled (b) versus SMPS output voltage V_{SMPS} and (c) versus SMPS switching frequency F_{SW}.

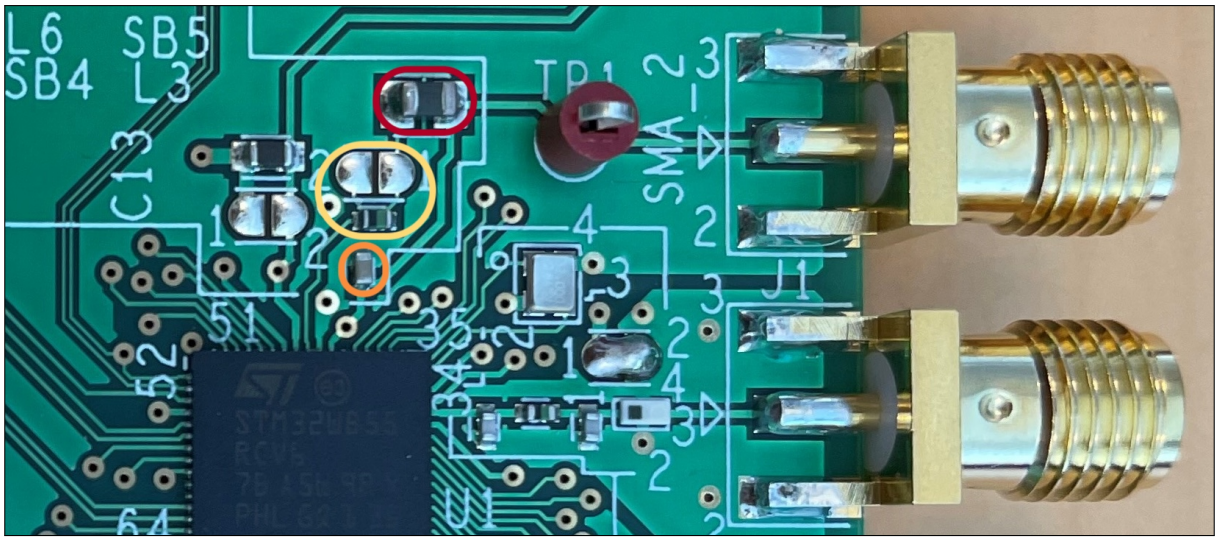


Figure 3.14: Close view of the SMPS output filter on the custom test board with L_{OUT} circled in red, C_{OUT} circled in orange, and the extra RF inductor circled in yellow.

3.3.3 Filter response influence

The frequency response of the SMPS output filter is affected by parasitic elements and differs from the ideal wanted response. As presented in 2.2.3, a consequence is the presence of a high-frequency resonance in the filter response, causing an increase in the noise spectral density at high-frequency (400 MHz – 3 GHz).

As the higher frequency content in EMI seems to have a strong impact on the receiver sensitivity, it is interesting to study the effect of the SMPS filter response on the BLE receiver sensitivity.

High-frequency filter resonance

As (2.17) demonstrates, the output filter high-frequency resonance depends on the parasitic inductance of the package and PCB traces of the filter nodes, the parasitic inductance of the SMD capacitor, and the parasitic capacitance of the SMD inductor.

Figure 3.14 pictures the SMPS output filter on the custom test board. The test board embeds a small value (a few nH) RF[4] inductor L_{RF} between the power stage output node V_{LX} and the output filter inductor L_{OUT}, circled in yellow. This RF inductor L_{RF} can be bypassed thanks to the solder bridge jumper. It allows to artificially increase the total inductance L_1 detailed in Table 2.11, and implied in the resonance frequency value.

Figure 3.15 plots the EMI spectrum measured at the SMPS output V_{LX}, whether the inductor L_{RF} is bypassed, or equal to either 10 nH or 33 nH. As the parasitic inductance L_1 increases, the total inductance implied in the resonance increases too, and the frequency of the resonance decreases. This result shows a reduction of the noise density above 1 GHz (and in the BLE signal frequency band) with the increase of the parasitic inductance L_1, as the resonance is lowered.

Table 3.2 compares the measured and predicted frequency values for the resonance linked to the output filter response. The predicted resonance value is calculated from

[4]This inductor is denoted as 'RF' inductor as its parasitic elements are small enough to have a negligible effect in the frequency band of interest, below 4 GHz.

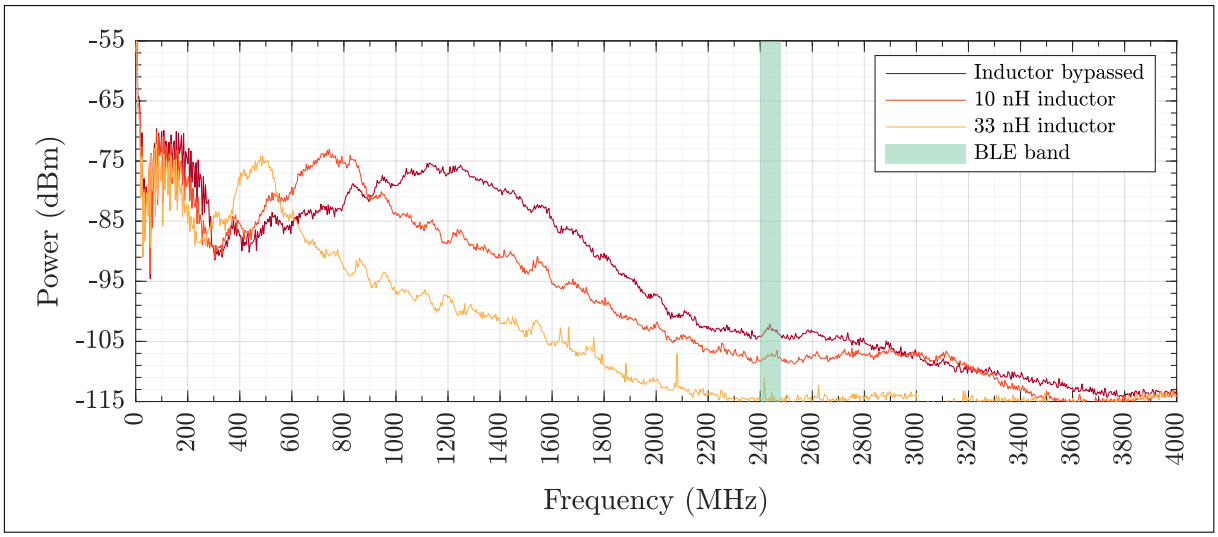


Figure 3.15: EMI spectrum measured on the custom test board at the SMPS output V_{SMPS}, depending on the value of the RF inductor added.

No inductance added to L_1 $\rightarrow L_1 = 6.90\,\text{nH}$	Measured resonance	$\sim 1.20\,\text{GHz}$	
	Predicted resonance	$1.27\,\text{GHz}$	$+ 5.8\,\%$
$10\,\text{nH}$ inductor added to L_1 $\rightarrow L_1 = 16.9\,\text{nH}$	Measured resonance	$\sim 760\,\text{MHz}$	
	Predicted resonance	$821\,\text{MHz}$	$+ 8.0\,\%$
$33\,\text{nH}$ inductor added to L_1 $\rightarrow L_1 = 39.9\,\text{nH}$	Measured resonance	$\sim 480\,\text{MHz}$	
	Predicted resonance	$536\,\text{MHz}$	$+ 11.7\,\%$

Table 3.2: Estimation of the main parasitic elements implied in the high-frequency resonance.

(2.17), by adding the value of the RF inductor L_{RF} to the parasitic inductance L_1.

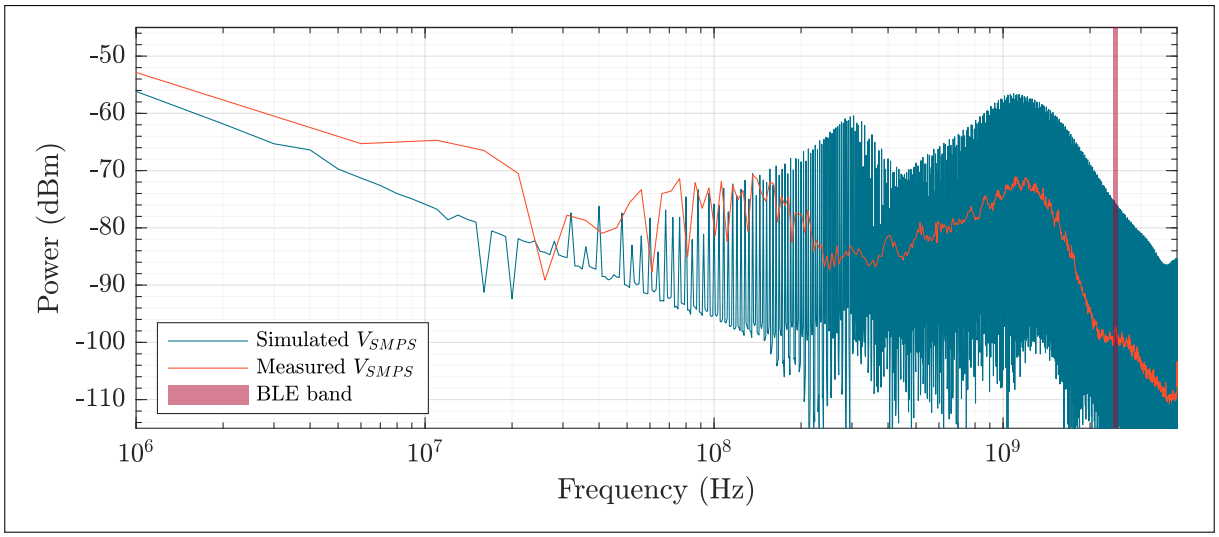
Measurement versus simulation

Figure 3.16 compares the measured and simulated impact of adding a 10 nH RF inductor between the node V_{LX} and the inductor L_{OUT}. Simulation results are obtained with the test bench developed with Cadence tools and presented in 1.3. The simulated test bench aim to give precise frequency results, not precise amplitude level.

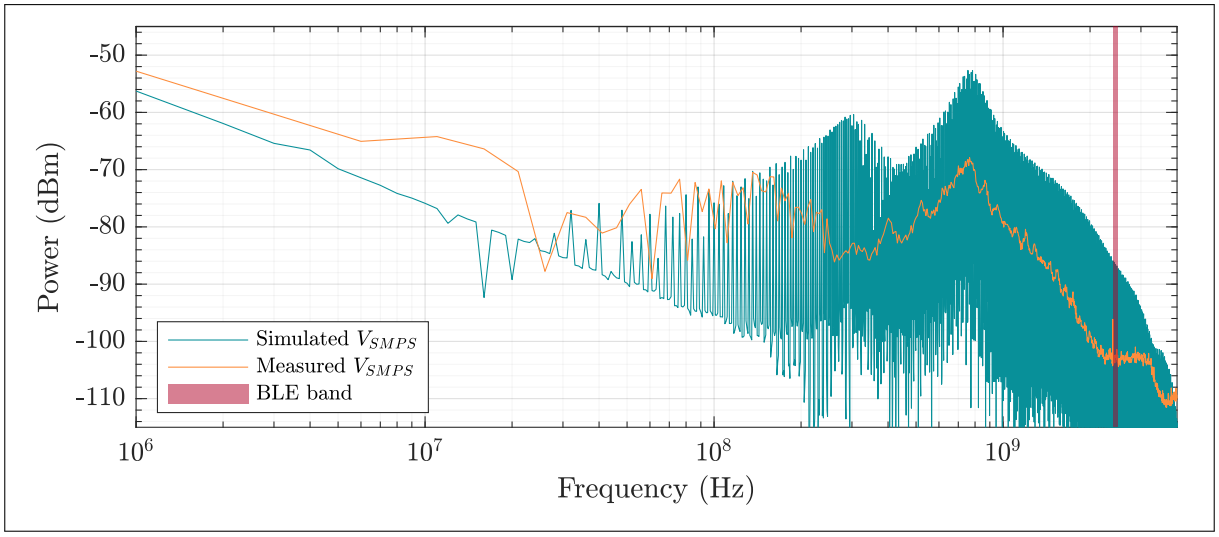
The lower frequency resonance is linked to the current discontinuities in the SMPS power stage, stimulating several parasitic capacitances and inductances in the system power distribution. As the whole power supply management is not simulated, the value of the lower frequency resonance obtained by simulation does not match the measured one. However, we can see that both measurement and simulation results exhibit a minor influence of the added RF inductor L_{RF} on the lower frequency resonance.

For the higher frequency resonance linked to the the output filter response, the measurement and simulation results match. The influence of the added RF inductor L_{RF} on the resonance value and shape is similar for both results.

The parasitic inductance L_1 affects mostly the resonance due the the SMPS output filter response and causes a reduction in the noise spectral density mostly at high-frequencies (above $\sim$1 GHz).



(a)



(b)

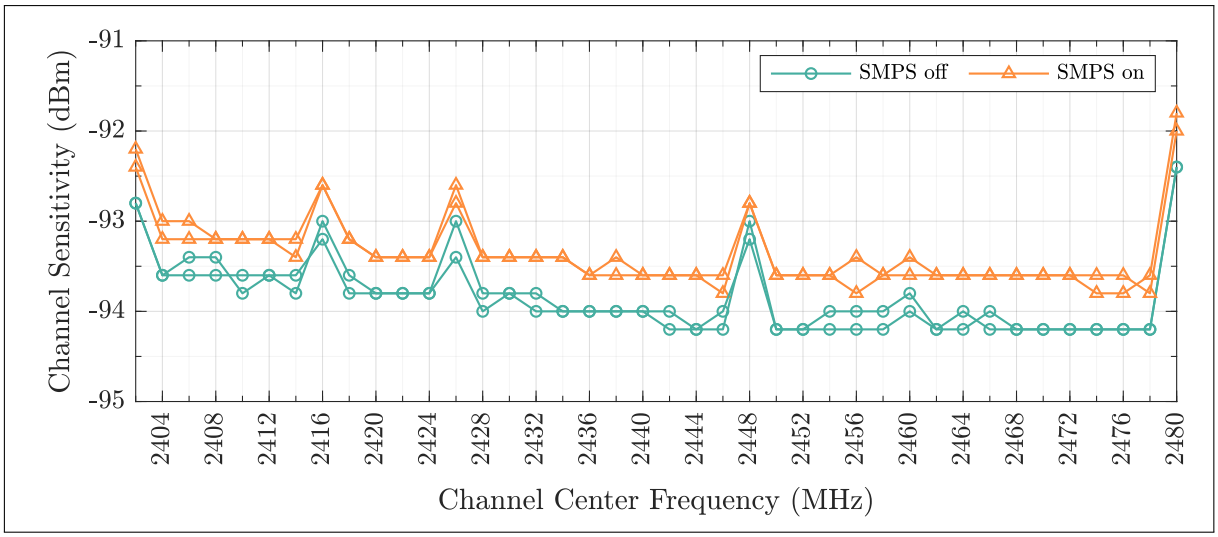
Figure 3.16: Influence of the 10 nH inductor in the output filter on the EMI generated on V_{SMPS}: (a) whithout the 10 nH inductor and (b) with the 10 nH inductor.

Effect on sensitivity

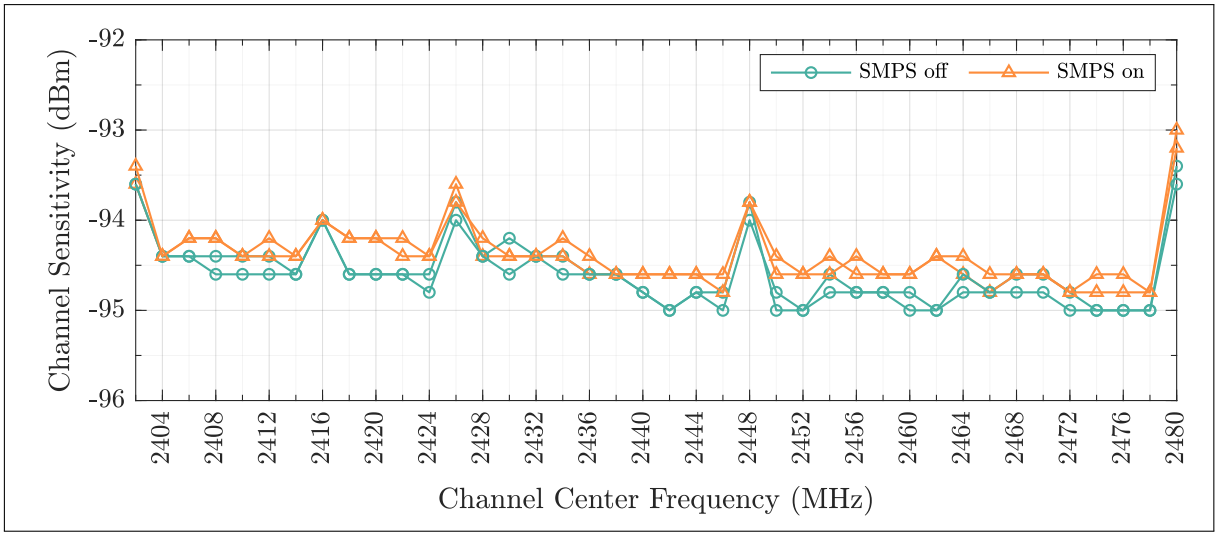
Figure 3.17 displays measurements of the receiver sensitivity for two different filter responses, leading to two different EMI spectral contents. Figure 3.17(a) corresponds to the case where the RF inductor L_{RF} is bypassed: the red spectrum in Figure 3.15. Figure 3.17(b) corresponds to the case where the RF inductor L_{RF} value is equals to 10 nH: the orange spectrum in Figure 3.15[5].

The sensitivity of the BLE receiver is less degraded when the 10 nH RF inductor L_{RF} is added between the node V_{LX} and the output inductor L_{OUT}. From the corresponding EMI spectra in Figure 3.15, the 10 nH RF inductor causes a reduction in the noise spectral density from around 1 GHz to 2.8 GHz. EMI in this frequency band tends to affects more

[5]The sensitivity measurement when the RF inductor L_{RF} value is equals to 33 nH could not be carried out due to a technical issue on the test board.



(a)



(b)

Figure 3.17: Receiver sensitivity per channel, two runs per measure: (a) without the 10 nH inductor and (a) with the 10 nH inductor

the BLE signal across the receiver circuitry.

Unfortunately, and as said in the previous subsection, the custom test board (on which it is possible to measure EMI spectra) exhibit much less impact from the SMPS operation comparing to the Nucleo test board. An hypothesis explaining this observation is the difference in the SMPS output filter on the two boards. On the custom test board, the PCB traces of the output filter are longer than on the Nucleo test board, due to the added and bypassable RF inductor, as it is visible in Figure 3.14. The Nucleo test board, with shorter PCB traces leads to a reduction of the parasitic inductances L_1 and L_3 detailed in Table 2.11, causing a higher resonant frequency in the output filter, a higher noise spectral density at high-frequency, and so, a stronger impact on the BLE receiver sensitivity.

3.4 Key Findings and discussion

Several types of measurements under different conditions have been performed on the system embedding the microcontroller. They reveal some interesting results that are summarize below.

- The SMPS operating at a switching frequency of 4 MHz generates EMI with a spectral content spanning over a wide frequency range, until above 3 GHz (almost 3 decades above the SMPS switching frequency). It is revealed by both the measurement of conducted EMI on the PCB and near-field radiated EMI above the PCB.
- The amplitude and spectral content of the generated EMI depends on the SMPS operating conditions as well as the parasitic elements of the system. External components choice and PCB layout of the SMPS output filter highly affect the spectral content of EMI.
- The BLE receiver sensitivity is directly affected by the SMPS operation, and by the variation in the spectral content of the generated EMI. The amplitude of high-frequency EMI (above 1 GHz) directly affects the sensitivity of receiver.
- Modifying the SMPS external filter response to shape EMI spectral content allow to limit the sensitivity degradation: EMI from the SMPS are not propagating toward the BLE signal inside the microcontroller IC, but through the PCB.

Degradation of the BLE receiver sensitivity by the SMPS activity

The operating conditions of the SMPS as well as its output filter response have a significant influence on the generated EMI and therefore play a crucial role in the BLE receiver sensitivity degradation. The parasitic elements of the system must be considered to predict high-frequency resonance and limit the noise spectral density in the BLE signal frequency band.

The microcontroller operating conditions depend on the application case and might vary during operation. Also, many of the parasitic elements involved in the high-frequency behavior of the SMPS output filter are not located in the integrated circuit or its package. Therefore, the amplitude and location of problematic resonances will highly depend on the application and system implementation decided by the user, making it hard to guarantee a correct operation.

However, it is possible to define guidelines for PCB layout and external component choice in order to limit the negative impact of the SMPS on the BLE receiver.

PCB guidelines

Figure 2.11 presented in the previous chapter details the main parasitic of the SMPS output filter involved in the high-frequency resonance. From 2.17, it is possible to determine the frequency of this resonance. To avoid high-amplitude in-band EMI, we can either push the resonance above or below the BLE signal frequency band.

To move the high-frequency resonance above the BLE signal frequency band, it is necessary to reduce the output filter parasitic elements as much as possible. That way, the SMPS output filter behaves as a low-pass filter until the signal frequency band. It proves difficult, and it is not possible in our case as the IC package brings too much

parasitic inductance and the SMD inductor with much lower parasitic capacitance does not exist.

Moving the high-frequency resonance below the signal frequency band is possible by the choice of external components or by their placement on the PCB. It is possible to choose an output inductor with a higher parasitic capacitance, lowering the high-frequency resonance. To avoid using an extra component in the external output filter, it is possible to increase the length of the relevant PCB trace of the filter at the cost of PCB layout density. The goal is to lower the frequency of the resonance to avoid having it too close to the BLE band and reduce the amplitude of in-band EMI.

What's next?

The EMI generated by the SMPS, and therefore the degradation of the BLE receiver sensitivity, are highly dependent on user choices (system operating conditions and implementation). Also, the predicted EMI spectral content will differ due to variations in the values of external component or their parasitic elements. Keeping the generated EMI under control is a difficult task; thus, it is worthwhile to work on improving the robustness of the receiver against EMI.

In this regard, the next chapter focuses on the study of the propagation of EMI inside the receiver and the study of their impact on the BLE signal. This task is accomplished by the development of a high-level model of the system that allows the simulation of receiver sensitivity in the presence of EMI generated by the SMPS.

High-level system model

4

Due to the complex architecture of the integrated BLE transceiver, it is difficult to predict how EMI would propagate through it, and what would be their effect on the received signal. On one hand, electrical simulation at transistor level proves very useful to analyze EMI propagation on small circuit blocks but cannot be used to simulate the whole system in order to analyze the impact of EMI on the sensitivity of the receiver. It would lead to excessive simulation time as explained previously in 1.3. On the other hand, functional simulation at system level doesn't take into account EMI propagating through every node of the receiver, affecting the BLE signal, and causing the sensitivity loss.

This chapter focuses on the development of the high-level model of the full BLE receiver, that will allow the simulation of its sensitivity in presence of EMI generated by the integrated SMPS with acceptable computing time. The goal is to identify critical propagation paths to and through the receiver, leading to a reduction of its sensitivity. The model is developed under MATLAB Simulink, and based on transistor level simulation under Cadence Spectre.

First, the architecture of the transceiver integrated into the STM32WB55 microcontroller is presented, with particular attention to the receiver architecture and its analog circuitry. Next, the method employed to design the high-level model is detailed, and applied to the first analog circuit blocks of the receiver. Then, simulation results of the receiver sensitivity in presence of EMI, obtained with the high-level model, are presented and discussed. Finally, results obtained with the model, further application for the model, and the approach to develop the model are discussed.

4.1 Transceiver architecture

The analog circuitry of the integrated BLE transceiver is depicted in Figure 4.1. The receiver (Rx) and the transmitter (Tx) share the same RF input/output. The microcontroller single-ended input/output RF_1 is connected to the primary side of a transformer. The low noise amplifier (LNA) input of the Rx chain and the power amplifier (PA) output of the Tx chain are both connected to the secondary side of the transformer. The PA is disable during Rx mode, and the LNA inputs are internally shorted to ground during Tx mode. The impedance transformation performed by the transformer ensure a good trade-off to satisfy at the same time the highest output power for the PA and the lowest NF for the Rx chain. An external impedance matching network is required between the antenna (or SMA connector) and the microcontroller input/output pin RF_1.

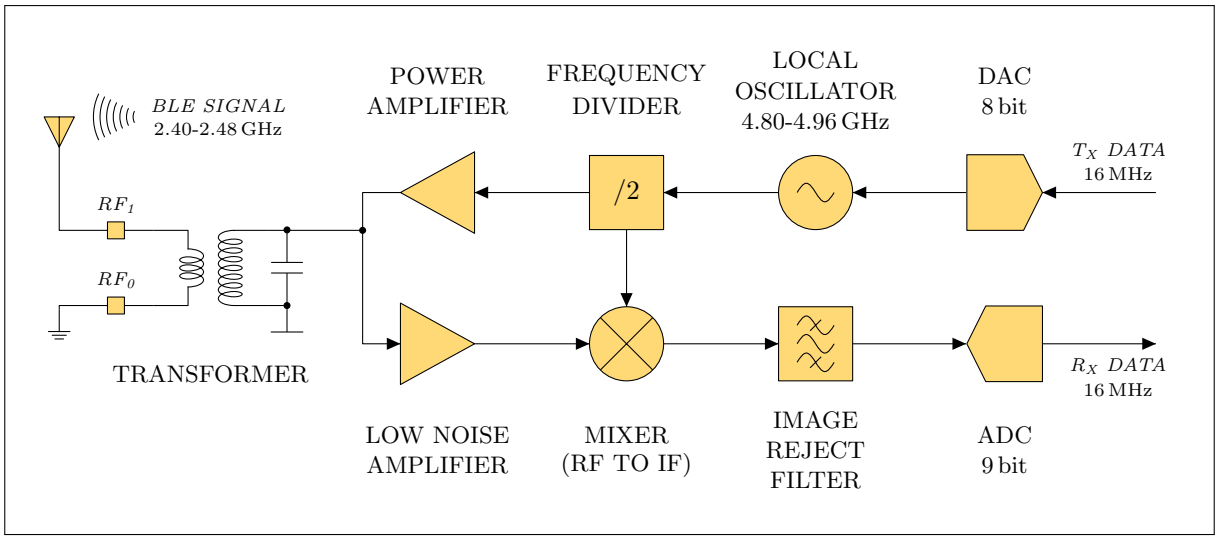


Figure 4.1: Architecture of the BLE transceiver analog circuit.

4.1.1 Transmitter

The modulation scheme employed by the BLE standard is called Gaussian frequency shift keying (GFSK), and is detailed in 3.1.1. In the digital circuitry of the transmitter, the 1 Mb/s Tx data bits are shaped by a Gaussian filter generating a smoother signal, sampled at 16 MHz. The digital signal is converted into an analog signal by the 8 bit digital-to-analog converter (DAC).

This signal is driving the voltage controlled oscillator (VCO) generating a frequency modulated square signal between 4.80 GHz and 4.96 GHz. A frequency divider convert the VCO output into a frequency modulated square signal with a center frequency comprised between 2402 MHz and 2480 MHz (BLE channels), and a frequency deviation of ±250 kHz. The PA amplify the modulated signal for an emission by the antenna at the desired power comprised between $-20\,\text{dBm}|_{50\,\Omega}$ and $6\,\text{dBm}|_{50\,\Omega}$.

The inductor at the secondary side of the transformer forms with the parallel capacitor, a resonant tank circuit tuned at 2.45 GHz, which aids in the extraction of the required signal from the pulsed output of the PA transistor and contribute in the attenuation of all other frequencies.

4.1.2 Receiver

The analog circuitry architecture of the receiver is depicted in Figure 4.2. The BLE signal is sensed by the 50 Ω antenna, or in our case, directly injected through an SMA connector at the RF input RF_1 via a 50 Ω source (the wireless conectivity tester). An impedance matching network transform the impedance of the IC input pin to 50 Ω in order to limit power losses at PCB-level.

We can divide the analog circuitry of the BLE receiver into three stages corresponding to the three main function it achieves: An amplification stage, a downconversion stage, and a filtering stage.

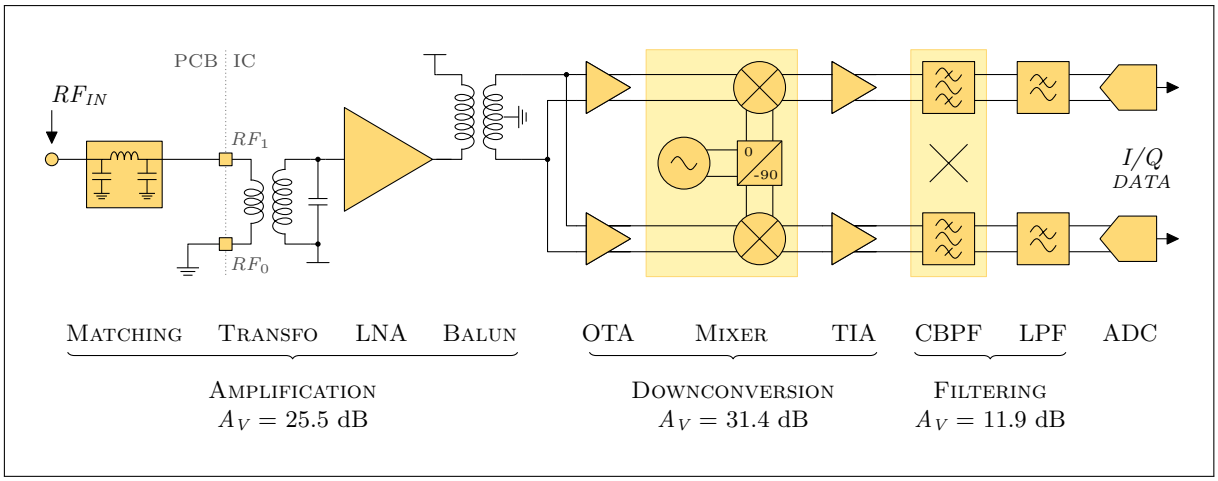


Figure 4.2: Architecture of the receiver analog circuitry.

Amplification stage

We consider the amplification stage comprised of the matching network, the transformer, the LNA and the balun. The amplification stage provides a voltage gain of 25.5 dB.

The pi-shaped matching network placed on the PCB ensure the correct impedance matching between the 50 Ω RF source and the microcontroller pin RF_1. The transformer ensure the correct impedance matching between the RF_1 pin and the LNA input (around 200 Ω) The LNA converts the power signal to a voltage signal with low reduction in the signal to noise ratio (SNR). The resonant LC tank formed by the transformer secondary and the capacitor acts as a band-pass filter centred around 2.45 GHz and helps filtering unwanted out of band noise. The LNA amplify the RF signal (2.45GHz) with low reduction in the signal to noise ratio (SNR). Because the LNA is a sensitive block, its NMOS are isolated using deep n-wells[1] to protect them against the substrate pollution (SMPS, digital...). The balun (balanced to unbalanced) generates a differential (balanced) voltage signal from the single-ended (unbalanced) voltage signal of the LNA output.

Down-conversion stage

The down-conversion stage is comprised of an operational transconductance amplifier (OTA), a passive mixer and a transimpedance amplifier (TIA). The down-conversion stage provides a voltage gain of 31.4 dB.

The differential voltage signal at the balun output is fed through two OTAs to generates two identical differential current signals. The 2.4 GHz BLE signal is down-converted to a low intermediate frequency (IF) at 1.6 MHz. and producing two differential I & Q channels[2] The receiver architecture first convert the received signal to a fixed intermediate frequency (IF) (heterodyne receiver) The IF is 1.6 MHz.

Filtering stage

The filtering stage comprised of a complex band-pass filter (CBPF) and a low-pass filter (LPF). The filtering stage provides a voltage gain of 11.9 dB.

[1] the NMOS p-well is surrounded by an extra n-well to isolate it from the p-type substrate

[2] to explain a minimum

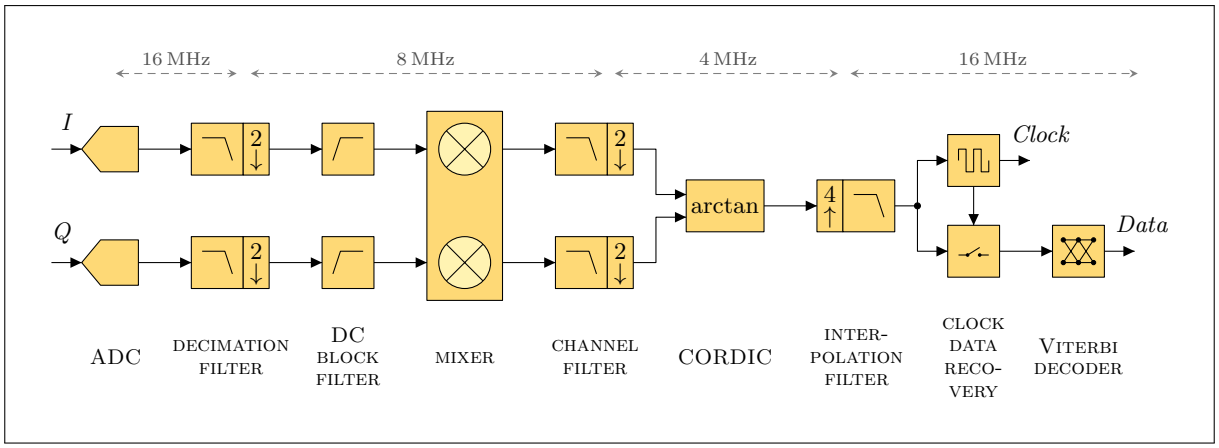


Figure 4.3: Architecture of the receiver digital circuitry.

The CBPF is a polyphase filter employed to suppress the sprectral content at the image frequency. The BLE signal signal is now at a relatively high amplitude, a relatively low frequency, and with a relatively limited bandwidth. It is possible to convert it to a digital signal to pursue the demodulation process in the digital realm for more accurate results. At this point, the hypothesis is made that the BLE signal is not affect by the EMI generated by the SMPS (not studied here).

The amplitude of the signal across the different stages of the analog circuitry of the receiver, as well as its centre frequency, is shown in Table 4.1. The RF front end[3], where the signal is low amplitude and at a frequency above the SMPS switching frequency is where the signal is most likely to be impacted by EMI generated by the SMPS. The analysis method described in the following sections was applied to the amplification stage (as defined in 4.2).

Position	RF input	Balun output	TIA output	LPF output
Amplitude	10.0 μV_{PP}	188 μV_{PP}	7.00 mV_{PP}	27.5 mV_{PP}
Frequency	2.40-2.48 GHz	2.40-2.48 GHz	1.6 MHz	1.6 MHz

Table 4.1: Peak-to-peak voltage and center frequency of the signal through the receiver analog chain.

Digital demodulation

The digital circuitry architecture of the receiver is depicted in Figure 4.3. The complex I and Q analog signals are sampled at 16 MHz by the 9 bit analog-to-digital converter (ADC). Both I and Q channels are filtered and down-sampled (decimation filter), reducing the sample frequency to 8 MHz and any voltage offset is removed (DC block filter). The signals are down-converted from the 1.6 MHz IF to baseband (centred around 0 Hz) by the digital mixer. The low-pass channel filter complete the filtering done before the ADC. The final demodulation step is operated using a CORDIC[4] algorithm. The algorithm

[3]all the circuitry between the receiver antenna input to and including the mixer stage.

[4]Stands for 'coordinate rotation digital computer', simple and efficient algorithm to calculate trigonometric functions.

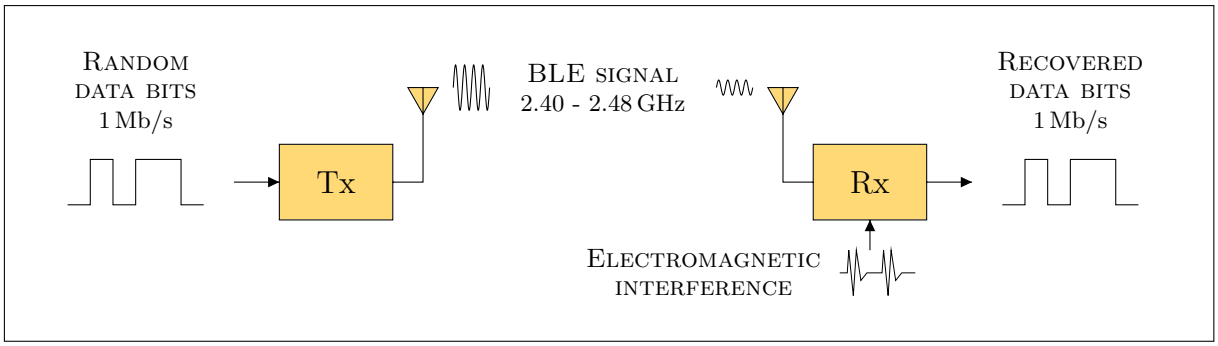


Figure 4.4: Simplified representation of the Simulink high-level model of the studied system.

calculate the arctangent of the ratio The demodulated signal is up-sampled to its original sampling frequency of 16 MHz by the interpolation filter. The clock is extracted from the demodulated signal and is used to sample the data bits with the best timing thanks to the clock and data recovery circuit. Viterbi algorithm is applied to the 1 Mb/s data bits to reduce the number of errors.

4.2 System modeling

A simplified representation of the high-level model designed under MATLAB Simulink is depicted in Figure 4.4.

An ideal BLE signal is generated from a stream of random bits using a basic transmitter architecture. The received signal power is chosen by user input. The background noise of the environment, as well as the noise figure of the receiver analog circuitry are added to the BLE signal. The signal is then processed by the analog and digital circuitry of the receiver, modeled on the architecture of the STM32WB55 receiver presented in 4.1.2.

At the receiver output, the 1 Mb/s stream of demodulated data bits is compared with the original stream of random bits to determine the bit error rate. To obtain the simulated receiver sensitivity, the signal power is lowered until the maximum acceptable bit error rate is reached.

The method employed to integrate EMI impact on the simulated sensitivity is detailed further on. The full MATLAB Simulink model is available in Appendix C.

4.2.1 High-level model scope

As part of this thesis and presented in the following sections, only the amplification stage of the receiver has been fully modeled for the study of EMI impact on the sensitivity. The reasons for this limited scope and its definition are detailed below.

Pre-thesis work

The functional model of the full BLE receiver comprised of the analog and digital circuitry has been developed during the internship preceding the thesis. It is based on the architecture of the receiver integrated into the STM32WB55, and allows the simulation of its sensitivity. The background noise sensed by the antenna and the noise figure of

the analog circuitry has been implemented as they are essential to determine the receiver sensitivity, as presented in 3.1.2.

During that internship, the impact of EMI on the receiver has only been studied and integrated to the model for the filtering stage[5]. The study shown that there is little to no impact of conducted EMI on the signal when processed by the filtering stage. A BLE signal reaching the system RF input[6] at the receiver sensitivity ($-96\,\mathrm{dBm}$) corresponds to a voltage signal with an amplitude of $10\,\mu\mathrm{V_{PP}}$. By the time it reaches the filtering stage input, the signal has been amplified to $7\,\mathrm{mV_{PP}}$, and at its output the voltage amplitude is $27.5\,\mathrm{mV_{PP}}$ (cf. Table 4.1). The signal is already relatively large and not really sensitive to EMI generated by the SMPS. Moreover, at the filtering stage input, the signal has already been down-converted to 1.6 MHz, below the SMPS switching frequency of 4 MHz. Only non linear phenomena like inter-modulation can generate unwanted noise in the signal band. It have been determined that realistic level of EMI cannot degrade the signal through the filtering stage.

Scope of the model

The RF front end[7], where the signal is at its lowest amplitude and still at a frequency above the SMPS switching frequency is where the signal is most likely to be impacted by EMI. The scope of the following analysis is limited to the receiver amplification stage, comprised of the transformer, the LNA and the balun.

Figure 4.5 depicted the simplified electrical circuit of the studied system. It consists of the analog circuitry of the receiver amplification stage (transformer, LNA, and balun), the SMPS power stage, the IC package, and the required external components. This simplified circuit allows to grasp the difficulty in determining which elements of the BLE receiver are the most sensitive to EMI and are leading to a degradation of performances. Several hypothesis are to consider:

- Interference generated on V_{DD} propagates towards the receiver via the LDO regulators power supplies, and so, to the receiver blocks power supplies,
- Similarly, interference generated on V_{SMPS} propagates towards the receiver via the LDO regulators inputs, and so, to the receiver blocks power supplies,
- Interference present in the PCB ground plane due to capacitive coupling or directly injected by the power stage ground reference propagates towards the receiver via the multiple receiver ground references connected to the exposed pad,
- Interference present in the PCB ground plane can also propagates towards the receiver either via the RF_0 pin, or via the RF_1 pin polluted due to capacitive coupling.

The high-level model aim to help determining the contribution in the sensitivity degradation for each EMI propagation path.

[5]The filtering stage is linear and processes signals around 1.6 MHz. It's the simplest stage and its study is feasible during a six-month internship.

[6]The system RF input is either the antenna or the SMA connector

[7]The circuitry between the receiver antenna input to and including the mixer stage.

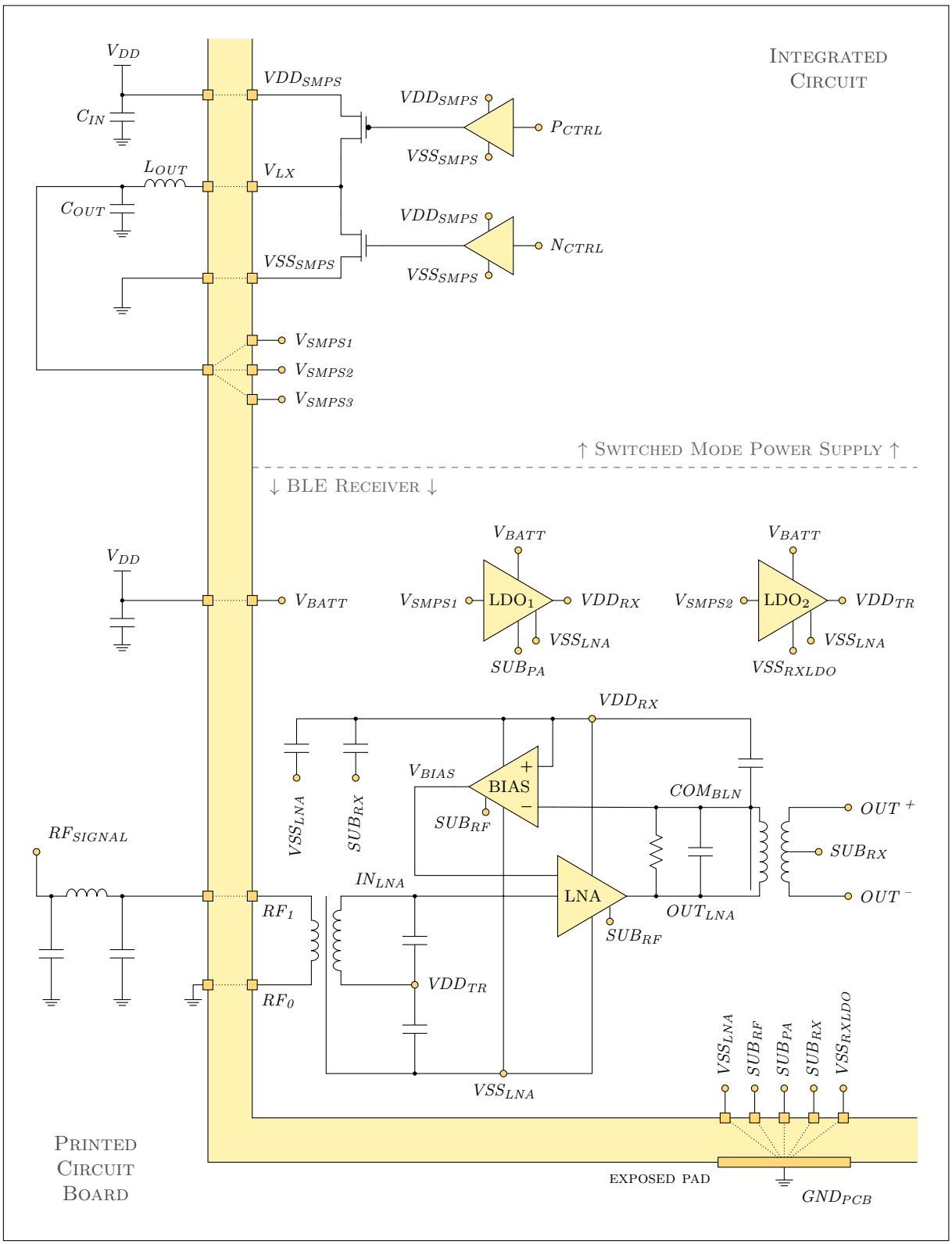


Figure 4.5: Simplified electrical schematic of the SMPS and receiver analog circuitry.

4.2.2 Modeling procedure

This subsection describes the chosen method employed to integrate the effects of EMI to the functional model described beforehand (Figure 4.4). The method have been applied on the amplification stage described in the previous section, from the RF input at PCB-level until the balun output.

EMI can propagate towards the wanted signal through any terminal (I/Os, supplies, biasing) of each sub-circuit. For the receiver amplification stage, the transformer possesses 5 terminals, the LNA possesses 6 terminals, and the balun possesses 4 terminals. A functional model of each sub-circuit (ignoring supplies and biasing terminal) is not sufficient to simulate EMI impact on the receiver sensitivity. The choice have been made to model each sub-circuit by each transfer function from its input terminals to its output terminal. The different steps of the modeling procedure are sum-up hereafter:

- Using AC transistor-level electrical simulations, the frequency and phase response is determined for each sub-circuit input terminals toward its output terminal.
- Corresponding transfer functions are estimated from the frequency and phase responses. Each sub-circuit are modeled under MATLAB Simulink by the sum of its transfer function blocks. Each sub-circuit of the receiver amplification stage are modeled with all their terminals.
- Transient transistor-level electrical simulation of the whole system are run, with the SMPS activated and the BLE receiver in Rx mode. The polluted voltage waveforms present at each terminals of the receiver sub-circuits are extracted.
- Polluted voltage waveforms are injected into the high-level MATLAB Simulink model through each terminal, allowing to simulate the receiver sensitivity in presence of EMI generated by the SMPS.

Transistor-level electrical simulation

One part of the modeling procedure is achieved with electronic design automation (EDA) tools, namely Cadence Virtuoso (schematic design entry) and Spectre (analog simulation). The test bench for transistor-level electrical simulation and the data obtained from it are presented below.

Simulation test bench: The simulation test bench contains all of the most relevant elements of the studied system. It is utilized for transistor-level transient and AC simulation. The complete Cadence Virtuoso test bench in available in Appendix B. It is comprised of:

- The transistor-level schematic of the SMPS power stage and its associated drivers from which the IC fabrication masks are issued for the STM32WB55. The transistor models are provided by the IC manufacturer ;
- The transistor-level schematic of the BLE receiver analog circuitry, also from which the fabrication masks are issued ;
- An RLCG model of the 68-pin QFN package inside which the STM32WB55 is encapsulated. The package model is coming from a 3D extraction realized with Ansys Q3D ;
- Parasitic models of the SMPS and BLE transceiver external components mounted on the PCB. The models are provided by the manufacturers ;

- A simple RL model of the PCB traces and vias. The values are calculated based on dimensions and PCB characteristics.

The 3D-extracted model for the IC package is valid up to 8 GHz. For the transformer and the balun, S-parameters are directly used in circuit simulations. This is due the complexity of transformer models, and the difficulty to determine values for each component of the model [4]. The transformer S-parameters are described from 100 MHz to 8 GHz, and the balun S-parameters from 100 MHz to 3 GHz.

Frequency and phase responses: The amplification stage is simulated in its environment: with the rest of the Rx chain, inside the IC package, and with the external impedance matching network. To obtain the frequency and phase responses for the three amplification stage sub-circuits (transformer, LNA, balun), a frequency sweeping AC sinusoidal voltage is injected sequentially on every input terminal of a given sub-circuit, and the voltage response at the sub-circuit output is plotted. The input pin RF_1 is loaded with a 50 Ω load and a pi-shaped impedance matching network, as it is in the studied system.

The frequency response for the three sub-circuits are plotted in Figure 4.6. Because the transformer and the balun are modeled with S-parameter files on a limited frequency range, discontinuities in the frequency and phase responses are present, happening at 100 MHz, 3 GHz or 8 GHz.

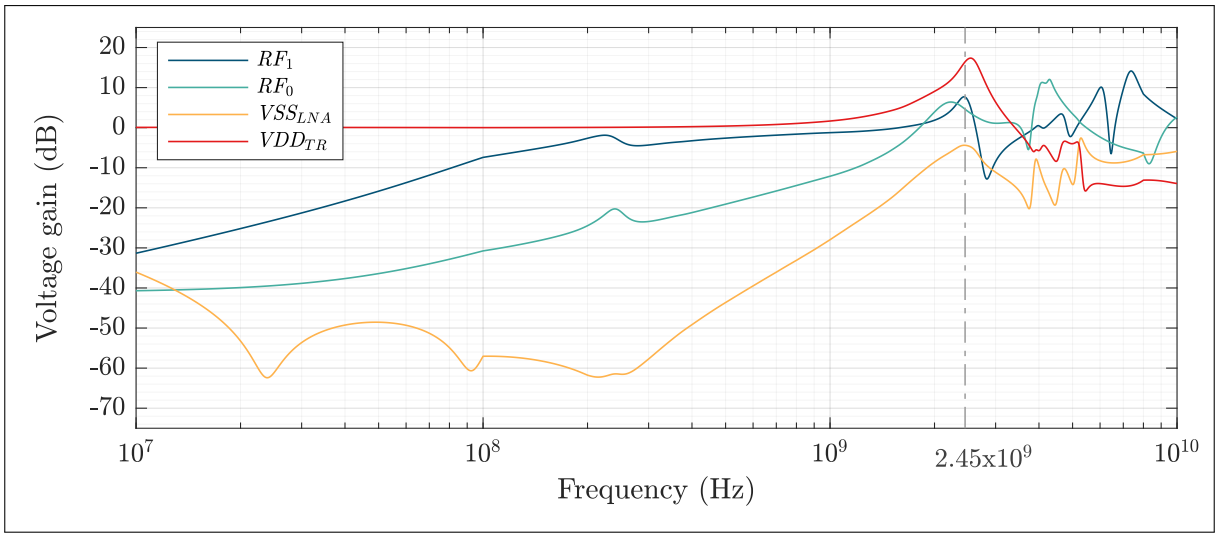
The plotted frequency responses gives an idea of the potential transfer of EMI present at any terminal of the receiver amplification stage to the BLE signal.

Polluted terminal voltage: The amplification stage is simulated in its environment, configured in Rx mode[8] and powered by the SMPS. Transient electrical simulations are run with the SMPS activated and switching at a frequency $f_{SW} = 4$ MHz. EMI generated by the SMPS propagates towards the amplification stage, through the modeled IC package, PCB traces or external components.

The extracted polluted terminal voltage are plotted in Figure 4.7, for the different terminals of the amplification stage sub-circuits (cf. Figure 4.5 for terminal name reference). High-frequency ringing is visible on each voltage waveforms. Ringing occurs every time the power stage transistors are switching, due to phenomena detailed in 2.2.

Each of the voltage waveforms will be injected into the high-level MATLAB Simulink model as a polluted bias voltage source through its corresponding terminal, allowing for the simulation of receiver sensitivity in the presence of EMI generated by the SMPS.

[8]No BLE signal is injected at the receiver input, the gain of every sub-circuits are set to their maximum by the AGC. The receiver is working in the same conditions as when it is processing a BLE signal with a power close to its sensitivity (−96 dBm corresponding to 10 μV_{PP} at 50 Ω).



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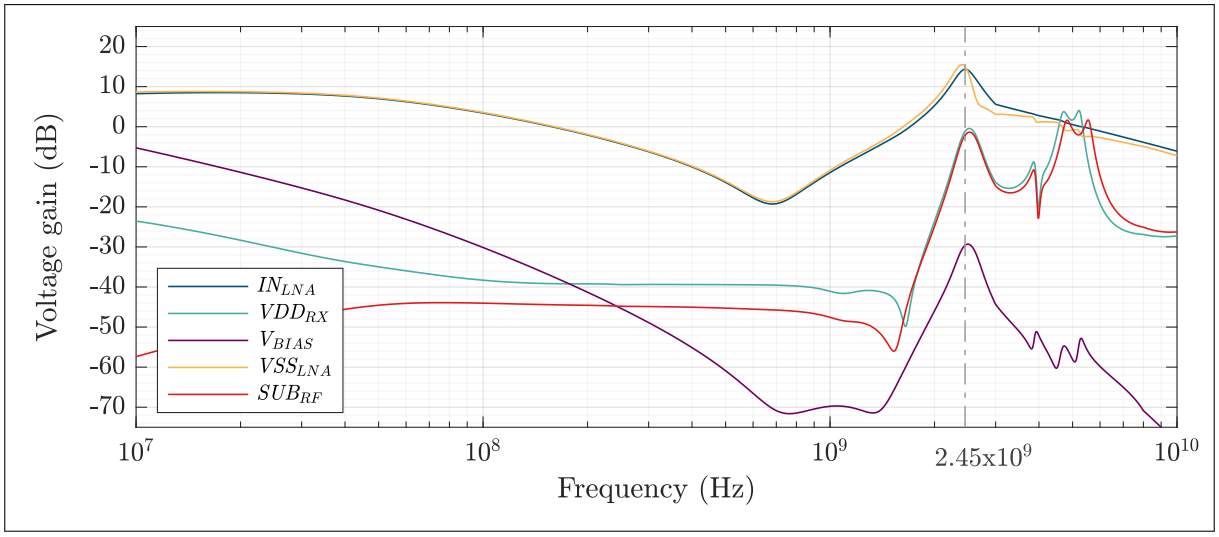
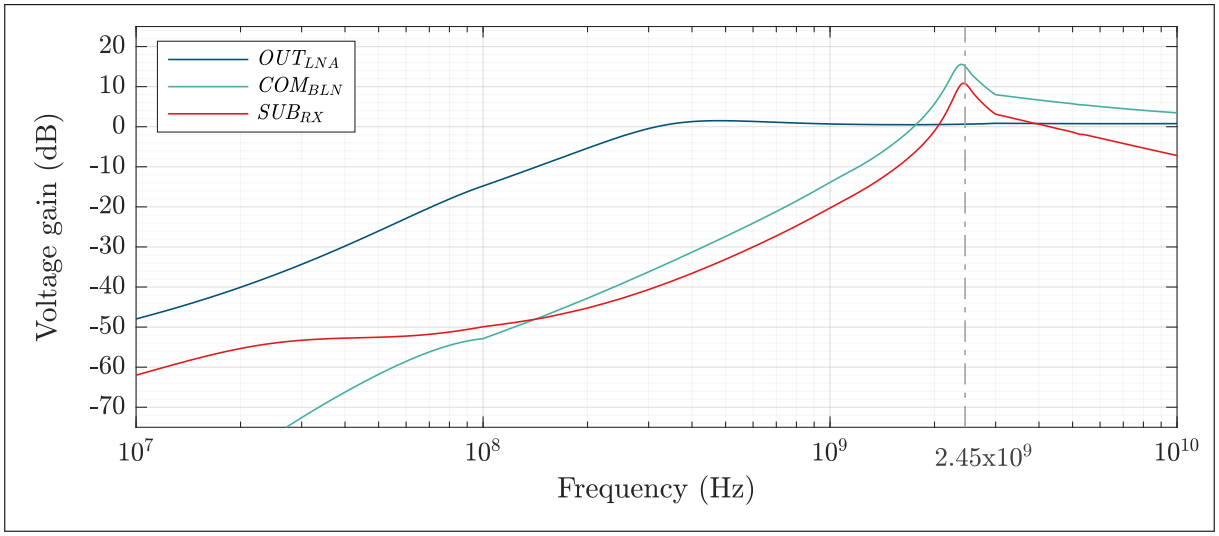


(b)



(c)

Figure 4.6: Input terminals to output terminal frequency response for (a) the transformer, (b) the LNA, and (c) the balun.

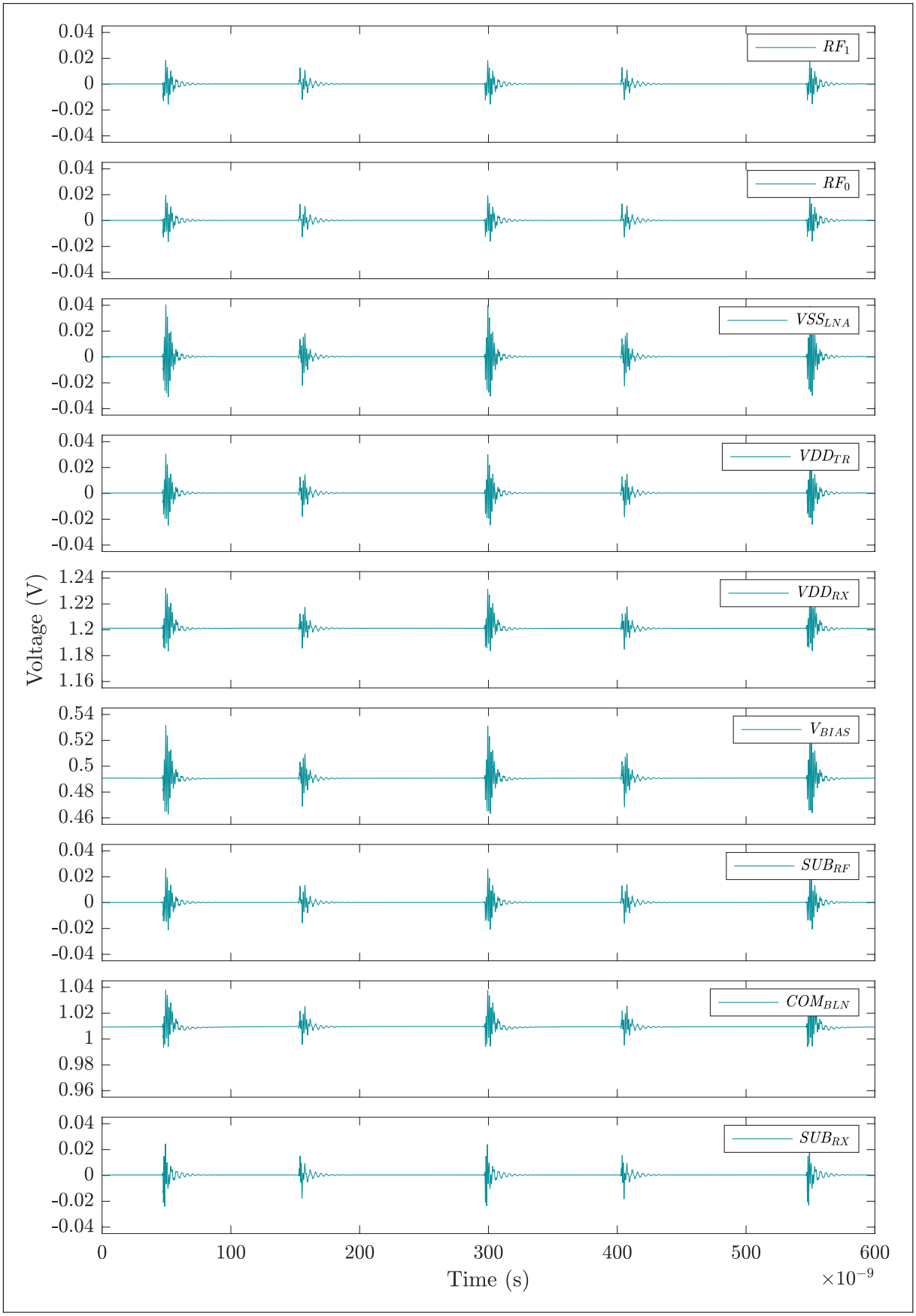


Figure 4.7: Extracted polluted terminal voltage for each amplification stage sub-circuits.

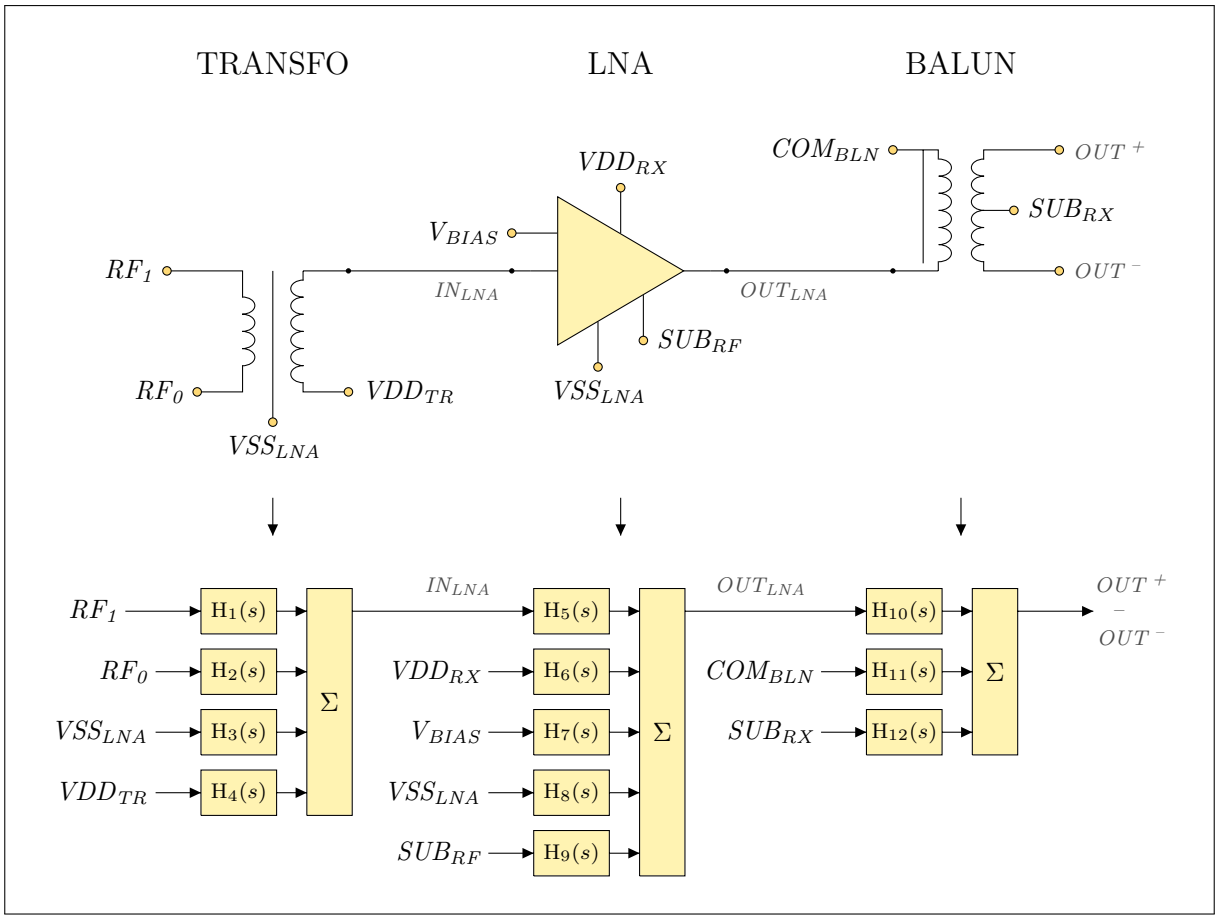


Figure 4.8: Modeling of the receiver amplifying stage.

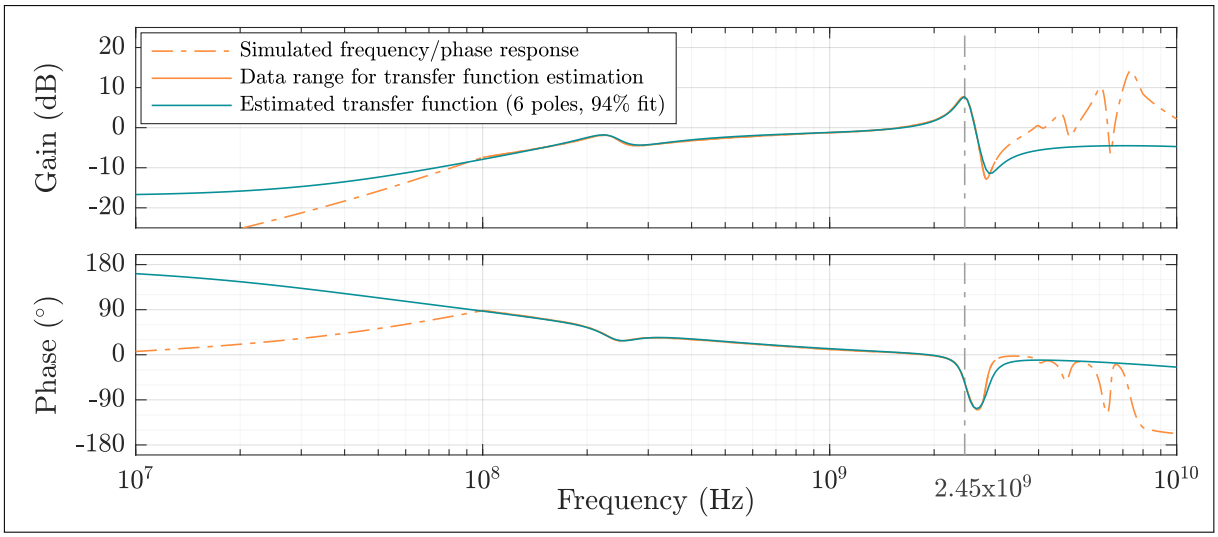
High-level modeling

Figure 4.8 represents the method applied to model the three amplifying stage sub-circuits. The integrated sub-circuits are modeled by the sum of each of their input-to-output transfer function ($H_1(s), H_2(s), ..., H_{12}(s)$), and EMI are injected through every input terminals ($RF_1, RF_0, ..., SUB_{RX}$). The BLE signal is carried through the outputs of the three amplifying stage sub-circuits (IN_{LNA}, OUT_{LNA} $OUT^+ - OUT^-$). The wanted signal contains EMI generated by the SMPS, transferred through the different sub-circuit terminals.

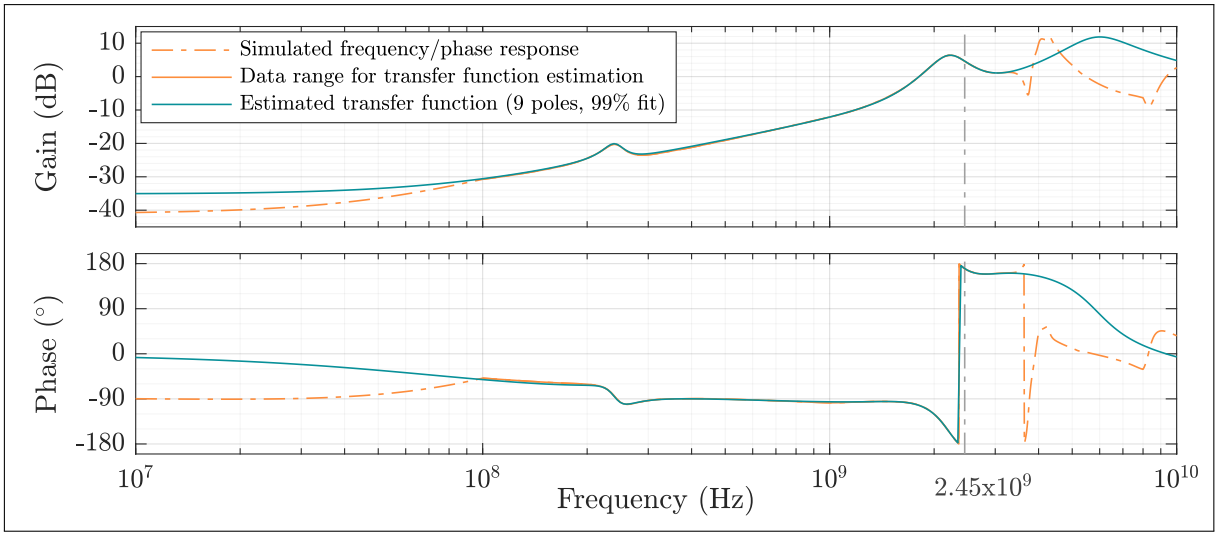
Transfer function estimation: Transfer functions are estimated from the frequency and phase responses obtained through the transistor-level electrical AC simulation presented previously. The MATLAB function **tfest** estimates a continuous-time transfer function with n_p poles and n_z zeros using frequency-domain data. The obtained transfer functions are in the form:

$$H_n(s) = \frac{(s - z_1)(s - z_2)...(s - z_{n_z})}{(s - p_1)(s - p_2)...(s - p_{n_p})}. \tag{4.1}$$

Because the transformer and the balun are defined by their s-parameter on a limited frequency range, the transfer function estimations are performed on a limited data range to avoid false estimation due to discontinuities observed at 100 MHz, 3 GHz and 8 GHz (S-parameter file boundaries). Estimations are performed on data from 100 MHz to 3 GHz, where the three sub-circuits are defined and can be simulated properly.



(a) Transformer primary input terminal RF_1 to its output terminal IN_{LNA}.



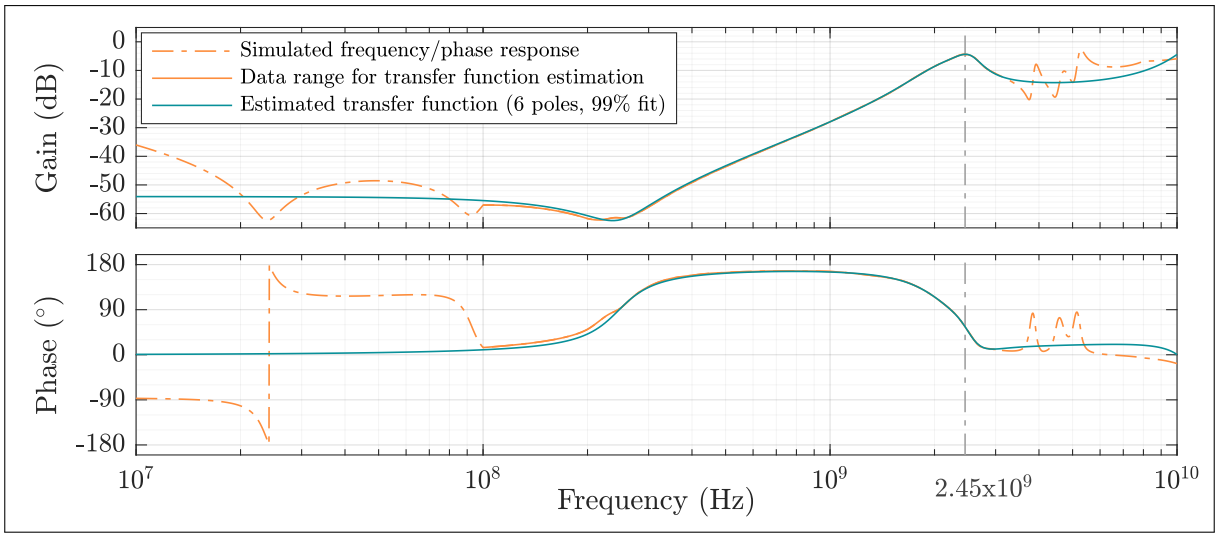
(b) Transformer primary reference terminal RF_0 to its output terminal IN_{LNA}.

Figure 4.9: Estimated transfer functions for the transformer input terminals toward its output terminal, obtained with the MATLAB function **tfest**.

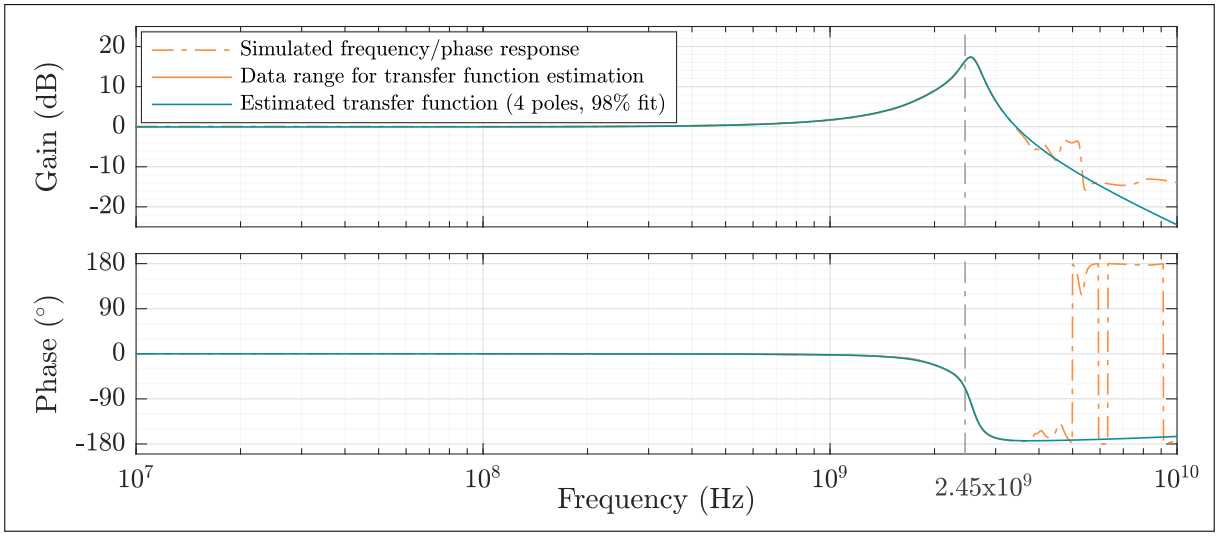
The number of poles is chosen arbitrarily for each transfer function. A trade-off is made between ensuring the best fit on the frequency range 100 MHz – 3 GHz (especially around 2.45 GHz), and ensuring that no incoherent behavior is present outside of this range (no abrupt poles or zeros that doesn't match the frequency response for example).

The four transfer functions describing the input-to-output responses for each terminal of the transformer are plotted in 4.9. The same graphs for the five LNA input terminals and the three balun input terminals are plotted in Appendix D. The chosen number of poles as well as the model response fitting to the data[9] are given for each transfer function in the plot's legend.

[9]The MATLAB function tfest returns the normalized root mean squared error (NRMSE) that is a measure of how well the response of the model fits the estimation data, expressed as the percentage fitpercent = 100(1-NRMSE).



(c) Transformer common reference terminal VSS_{LNA} to its output terminal IN_{LNA}.



(d) Transformer secondary reference terminal VDD_{TR} to its output terminal IN_{LNA}.

Figure 4.9: Estimated transfer functions for the transformer input terminals toward its output terminal, obtained with the MATLAB function **tfest**. (cont.)

EMI injection: Only the integrated part of the amplifying stage circuit is modeled[10] as the goal is to study the robustness of the design in presence of EMI. The voltage signals extracted from transistor-level electrical transient simulation presented in the previous subsection and plotted in 4.7 take into account the parasitic of the system (power stage, package, PCB and external components) as the whole system is simulated.

The voltage signals extracted from each sub-circuit terminals are injected in the high-level MATLAB model as EMI sources, as an input for the corresponding transfer function.

[10]The path from the PCB RF input (the SMA connector) to the transformer primary RF_1, through the matching network, is also modeled as it affected the front-end chain response.

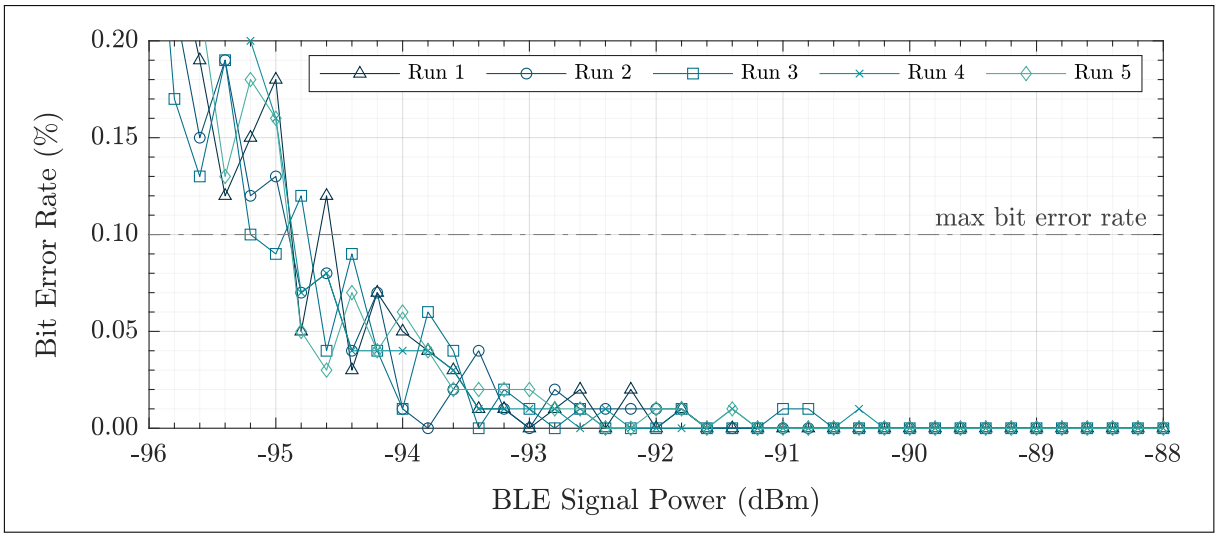


Figure 4.10: Simulation results of the receiver sensitivity using the high-level model, without EMI injection. Five runs of the same simulation are plotted.

4.3 Simulated sensitivity

This section presents results of the simulated receiver sensitivity obtained with the high-level MATLAB model. First, simulations of the receiver sensitivity without EMI injection[11] are presented. Then, EMI extracted from transistor-level simulation are injected into the high-level model in order to simulate the degradation of sensitivity in presence of interference.

The maximum acceptable bit error rate defined by the BLE standard is $BER_{max} = 0.1\,\%$. The bit stream is comprised of 10,000 bits, as a trade-off between simulation duration and statistically valid results.

Simulated sensitivity without EMI

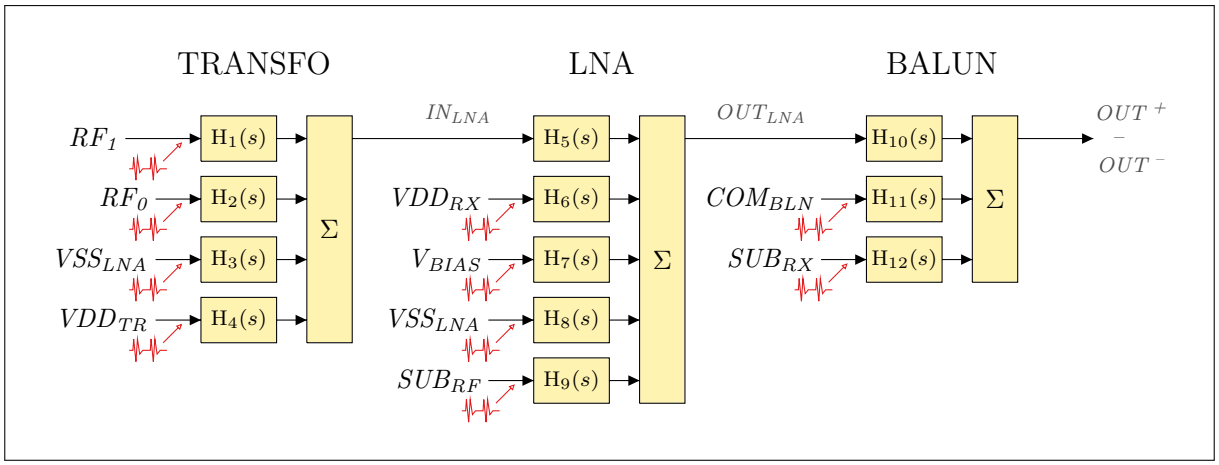
Figure 4.10 plots the simulated receiver sensitivity for five BLE channels chosen arbitrarily. The obtained sensitivity is approximately $-94.8\,\mathrm{dBm}$.

The intended purpose for the high-level model is to obtain qualitative results more than precise quantitative results. The goal is not to precisely predict the sensitivity loss in dB, but to understand what provokes the sensitivity loss.

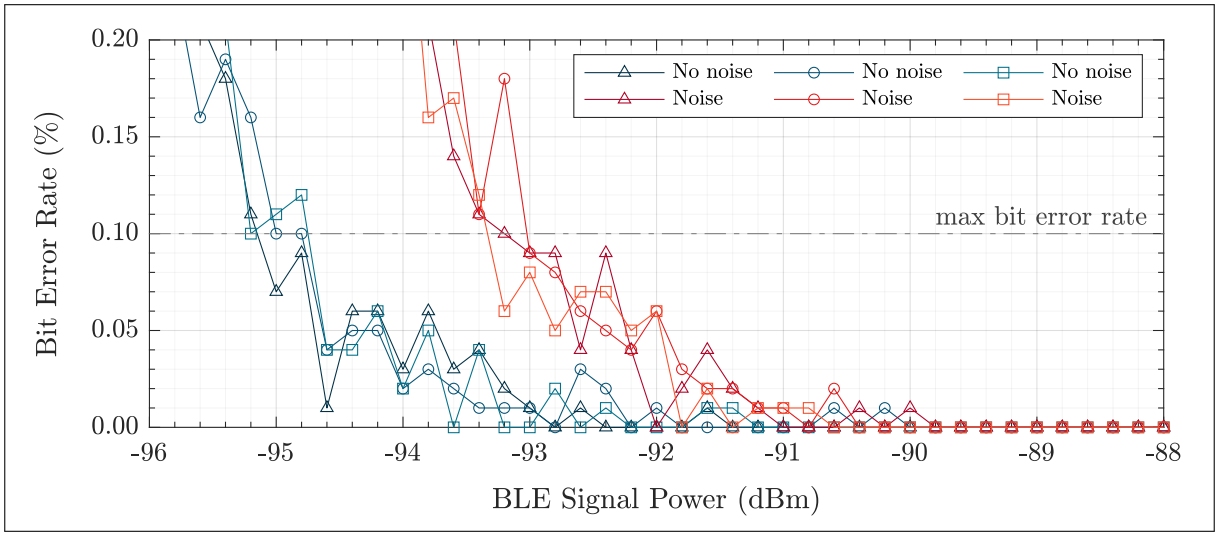
As the data bits and the added white noise to modulated signal (background noise and noise figure) are random, each simulation run gives different results. Here, 10,000 bits are transmitted per simulation run and five runs under the same conditions are preformed.

The modeled receiver is comprised of every elements of the "real" receiver, except for the Viterbi decoder placed after the digital demodulator and helping to reduce the number of errors. The Viterbi decoder improves the receiver sensitivity by 1 to 2 dBm. Because of that, the sensitivity of the modeled receiver only reaches around $-95\,\mathrm{dBm}$ (in comparison to $-96\,\mathrm{dBm}$ specified in the data sheet for the studied receiver).

[11] The background noise sensed by the receiver as well as the receiver noise figure are always taken into account, and added to the signal before the receiver input.



(a)



(b)

Figure 4.11: (a) EMI injection at every input terminals of the amplifying stage and (b) the corresponding degradation of the receiver sensitivity. Tree simulations are run under the same conditions, for each case.

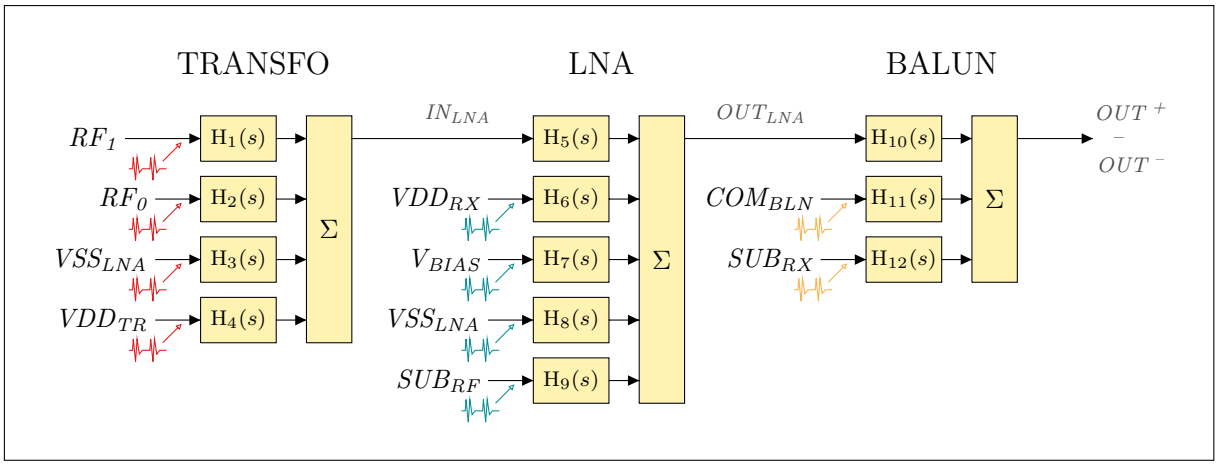
4.3.1 EMI injection

The polluted voltages extracted from transistor-level simulation and presented in the previous section can be injected into the high-level model through the different sub-circuit terminals, to simulate the sensitivity degradation caused by the SMPS generated EMI.

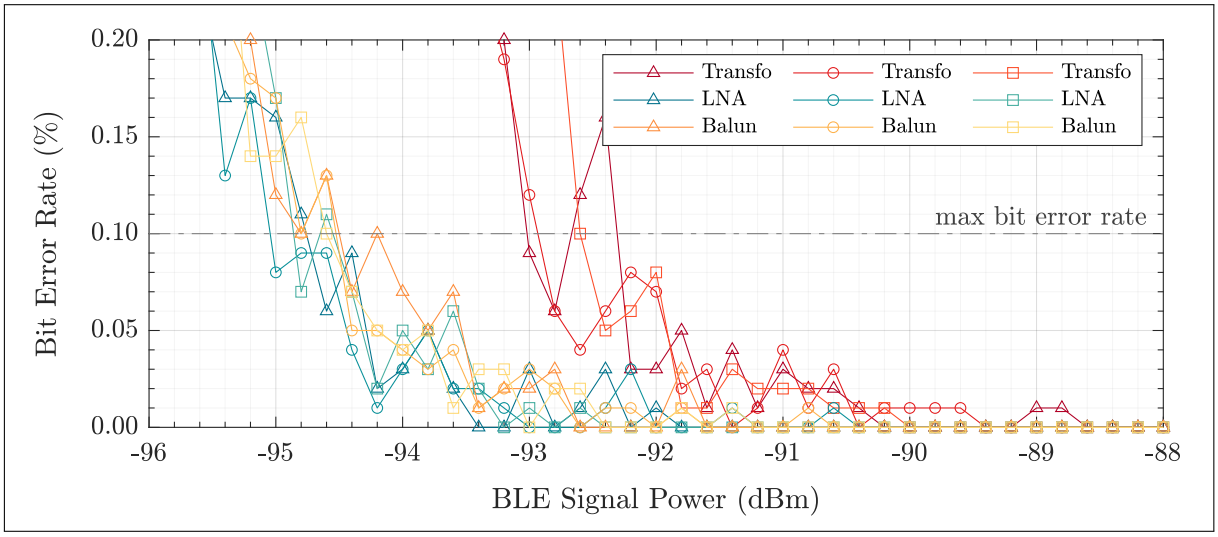
Injection on the amplification stage

Figure 4.11(b) presents the simulated sensitivity of the receiver when EMI are injected at every input terminals of its amplifying stage. The injection of EMI causes a degradation of approximately 1.8 dB, bringing the sensitivity of the receiver around −93.2 dBm.

It is worth noting that the simulated degradation of the sensitivity falls in the same order of magnitude than the measured one. However, this model has been designed for qualitative analysis more than quantitative analysis.



(a)



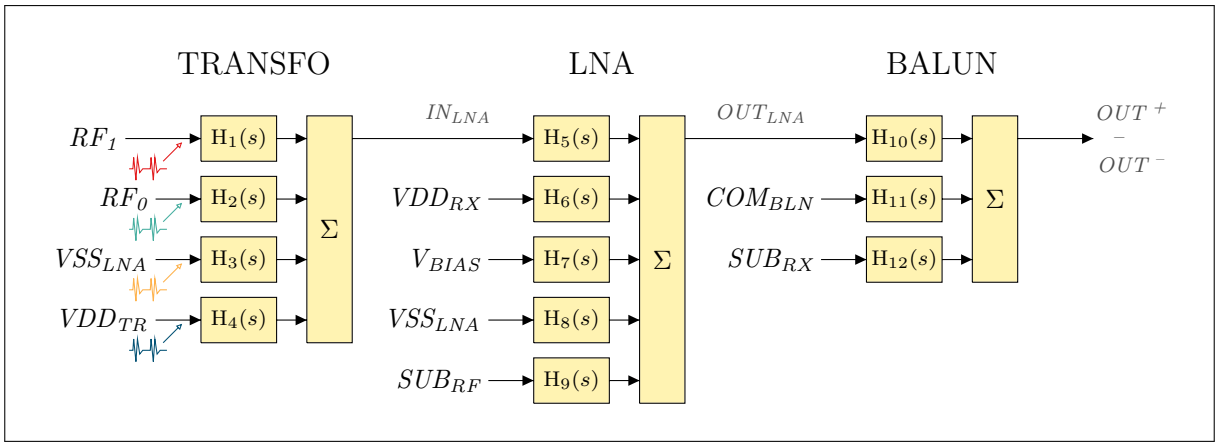
(b)

Figure 4.12: (a) Sequential EMI injection at every input terminals for each amplifying stage sub-circuits and (b) the corresponding degradation of the receiver sensitivity. Tree simulations are run under the same conditions, for each case.

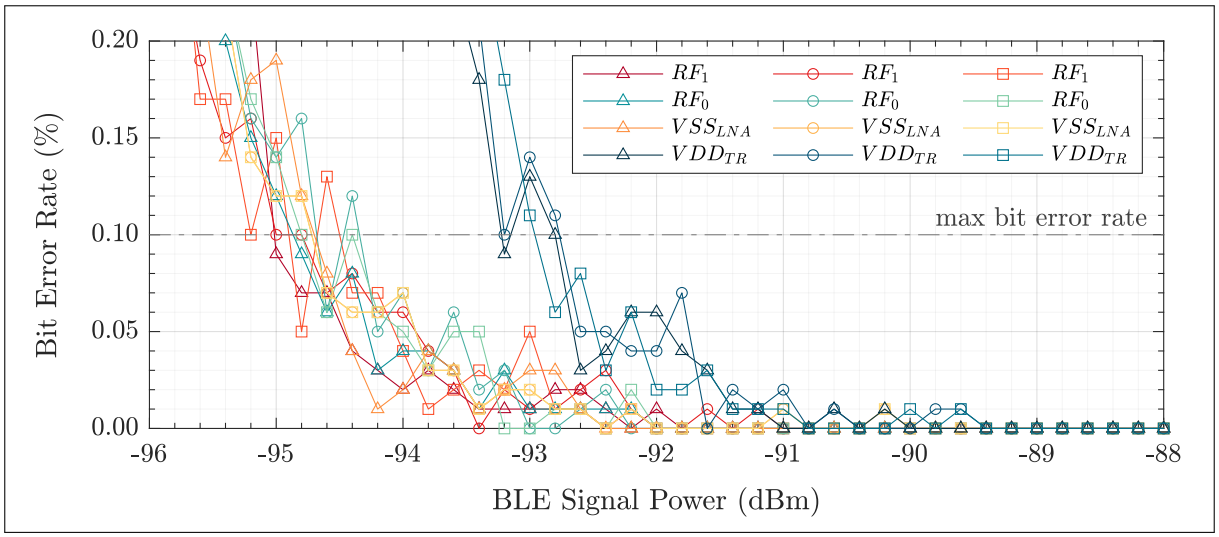
Injection on the sub-circuits

Figure 4.12(b) presents the simulated sensitivity of the receiver when EMI are injected only on one of the three sub-circuit input terminals. For the transformer sub-circuit, the injection of EMI causes a degradation of approximately 2.2 dB, bringing the sensitivity of the receiver around −92.8 dBm. For the LNA sub-circuit, the injection of EMI causes a degradation of approximately 0.2 dB, bringing the sensitivity of the receiver around −94.8 dBm. For the balun sub-circuit, the injection of EMI causes a degradation of approximately 0.4 dB, bringing the sensitivity of the receiver around −94.6 dBm.

The injection of EMI on the transformer sub-circuit leads to a comparable degradation of sensitivity as when the EMI are injected in the whole amplifying stage while the injection of EMI on the LNA and balun sub-circuits leads to a minor degradation of sensitivity.



(a)



(b)

Figure 4.13: (a) Sequential EMI injection for each input terminals of the transformer and (b) the corresponding degradation of the receiver sensitivity. Tree simulations are run under the same conditions, for each case.

Injection on the transformer

Figure 4.13(b) presents the simulated sensitivity of the receiver when EMI are injected only on one of the four input terminals of the transformer. The injection of EMI on the terminals RF_1, RF_0 or VSS_{LNA} causes a degradation varying from approximately 0 dB to 0.4 dB, giving a sensitivity of the receiver around −95.0 dBm / −94.6 dBm. The injection of EMI on the terminals VDD_{TR} causes a degradation of approximately 2.0 dB, bringing the sensitivity of the receiver around −93.0 dBm.

All the results of the receiver sensitivity degradation presented in this subsection are summarize in Table 4.2.

Amplifying stage	**Degradation**	**Sensitivity**
No EMI injection	–	−95.0 dBm
EMI njection	1.8 dB	−93.2 dBm
Sub-circuits	**Degradation**	**Sensitivity**
Injection on the transformer	2.2 dB	−92.8 dBm
Injection on the LNA	0.2 dB	−94.8 dBm
Injection on the balun	0.4 dB	−94.6 dBm
Transformer	**Degradation**	**Sensitivity**
Injection on RF_1	0.0 dB	−95.0 dBm
Injection on RF_0	0.4 dB	−94.6 dBm
Injection on VSS_{LNA}	0.2 dB	−94.8 dBm
Injection on VDD_{TR}	2.0 dB	−93.0 dBm

Table 4.2: Simulated degradation of the receiver sensitivity due to EMI injection under different conditions.

4.3.2 Identified design flaw

The simulation of the receiver sensitivity in presence of EMI indicates a strong impact of interference on the transformer sub-circuit, and more precisely on its terminal VDD_{TR}. To understand the root cause, we need to look at the PA topology and at the transceiver front-end architecture.

Power amplifier topology

The power amplifier topology is depicted in Figure 4.14(a). It consist of a single-stage common source amplifier[12] where an LC tank operates as the load.

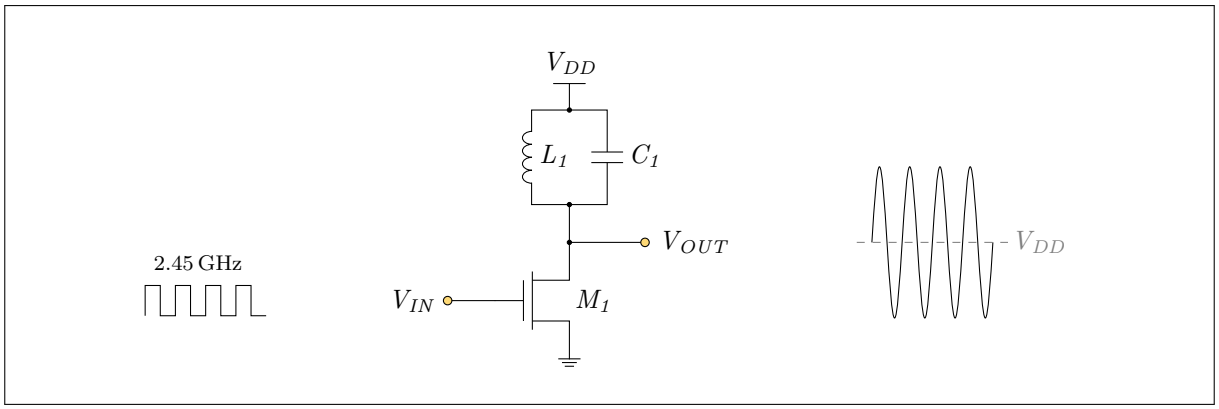
The input signal V_{IN} is a pulse signal modulated around 2.45 GHz to carry the data to transmit. The LC tank formed of L_1 and C_1 is tuned to resonate at the frequency of the input signal. The transistor M_1 produces a series of current pulses according to the input and the LC tank circuit aids in the extraction of the required signal since the resonant circuit oscillates at only one frequency. Mostly the fundamental of the pulse signal is amplified and remaining harmonics are removed before emission using additional filters. A BLE signal is obtained at the PA output V_{OUT}. As the series resistance of the inductor L_1 is negligible, the DC voltage is close to V_{DD}.

Front-end architecture

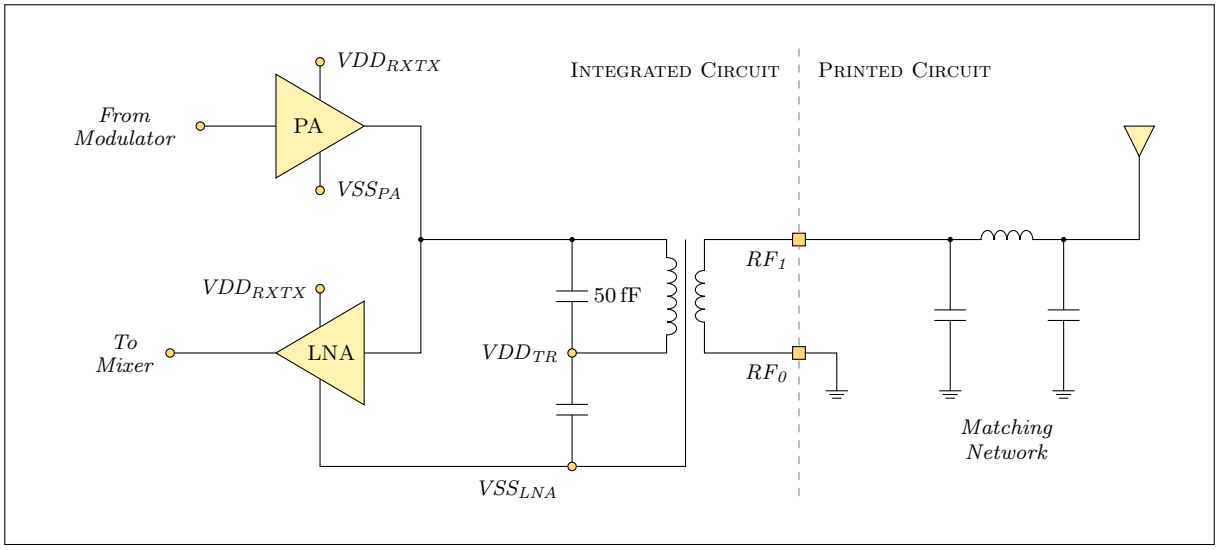
The architecture of the transceiver front-end is presented in Figure 4.14(b). The single-ended low noise amplifier and the single-ended power amplifier are sharing the input/output pin RF_1.

When the transceiver is in Tx mode, the LNA inputs are internally shorted to ground and a dedicated LDO regulator (LDO_2 in Figure 4.5) provides the voltage VDD_{TR}, adjustable from 0.75 V to 1.5 V depending on the desired output power. When the

[12]The actual power amplifier implemented in the transmitter uses a cascode topology.



(a)



(b)

Figure 4.14: (a) Power amplifier topology, a common source stage with an LC tank load and (b) Simplified schematic of the transceiver front-end.

transceiver is in Rx mode, the PA is turned off as well as the dedicated regulator LDO_2. The voltage VDD_{TR} is tied to ground.

The LC tank is formed of the inductor at the transformer secondary ($\approx 80\,\text{nH}$) and the 50 fF capacitor, resonating at 2.45 GHz.

Impact of the LC tank in Rx mode

In Rx mode, the noise at each of the transformer ground reference terminals (RF_0, VSS_{LNA} and VDD_{TR}) and at its input terminal (RF_1) is present at a similar level (cf. Figure 4.7). However, due to the LC tank, the noise at the transformer terminal VDD_{TR} is amplified at 2.45 GHz.

This was already visible in the extracted frequency responses for the transformer, presented previously in Figure 4.6(a). The gain at 2.45 GHz is much stronger for the transfer function from the terminal VDD_{TR} to the transformer output (13.5 dB) than for the transfer function from the terminal RF_1 to the transformer output (8 dB). EMI at the terminal VDD_{TR} are more amplified at 2.45 GHz by the transformer sub-circuit than the BLE signal is.

When the SMPS is disabled, the noise spectral density of EMI in the BLE band is very low (cf. Figure 3.6), and even after amplification by the LC tank, EMI do not lead to degradation of the receiver sensitivity. On the other hand, when the SMPS is enabled, the noise spectral density of EMI in the BLE band is increased by high-frequency resonances (cf. 2.2.3), and after amplification by the LC tank, EMI provoke a degradation of the receiver sensitivity.

EMI injected in the BLE band at the very beginning of the Rx chain through the terminal VDD_{TR}, where the signal is at its lowest amplitude, will be processed by the entire Rx chain (as they are at the same frequency as the wanted signal).

4.4 Key findings and discussion

The simulation of the receiver sensitivity with the injection of EMI at its amplification stage indicates a strong impact of EMI via a specific terminal of the receiver analog circuitry. This terminal is the transformer secondary reference.

The transformer is located between the RF input pin and the LNA. It serves both for the emission and the reception of BLE signals, and a LC tank resonating at 2.45 GHz is present on its secondary side. The LC tank is designed for the operation of the transceiver in Tx mode; however, in Rx mode, the EMI present on the transformer secondary reference are being strongly amplified at 2.45 GHz.

Degradation of the BLE receiver sensitivity by the SMPS activity

> The high-level model suggests that the BLE signal is significantly more affected by the EMI at the beginning of the Rx chain before it gets amplified by the LNA. After the signal is processed by the LNA, the signal is more robust against EMI because of the high amplification gain.

The LNA amplifies the wanted BLE signal almost 19 times (+25.5 dB), making that signal much less sensitive to EMI. However, after the amplification stage, the signal is processed by the down-conversion stage. It mainly consists of a mixer, a non-linear stage, and phenomena like inter-modulation could produce components falling into the BLE band [4], and should be looked after.

Conclusion

5

The aim of the thesis was to give a thorough review of an existing issue related to the influence of electromagnetic interference generated by a switched-mode power supply on a Bluetooth Low-Energy receiver. The main objectives were to set up a methodology intended for the analysis of the impact of EMI generated by the SMPS on the BLE receiver analog circuitry and to develop tools allowing the qualitative prediction of the sensitivity degradation caused by the SMPS activity.

The defined objectives were achieved during the PhD thesis. The research work carried out to reach the desired objectives led to application guidelines and design optimization proposals for the studied system, aiming to ensure cohabitation inside a unique system-on-chip of a non-linear DC/DC power converter and a wireless connectivity solution.

5.1 Synthesis

In order to address the research problem, two different approaches are conceivable. The first approach consists of dealing with the issue at its source by reducing the EMI generated by the SMPS. It necessitates a full understanding of how EMI are generated, how they propagate through the system, and what defines their spectral content. The second approach consists of dealing with the consequences of the issue by improving the BLE receiver robustness against EMI. It requires a full understanding of how EMI propagate inside the receiver sub-circuits and how they affect the BLE signal, leading to a degradation of the receiver sensitivity.

Reducing interference generation

The deep analysis of EMI generation by the SMPS and their propagation through the system allowed the identification of two distinct phenomena. One source of EMI generation is related with the fast switching at $F_{SW} = 4\,\text{MHz}$ of the SMPS power MOSFETs. Relatively large discontinue currents are flowing through parasitic inductances, leading to voltage overshoots across them. The other source of EMI generation is linked to the high-frequency response of the SMPS output filter. Above 100 MHz, the filter response is dominated by its parasitic elements, and the high-frequency content of the pulse signal at the power MOSFETs output is not entirely filtered.

For both phenomena, the spectral content of the generated EMI is determined by specific elements of the system (mostly parasitic elements) causing resonances. One resonance has been identified as greatly problematic as it significantly raises the noise spectral density up until the BLE frequency band, located around 2.4 GHz. It is a resonance in the

SMPS output filter response, occurring at a frequency mostly dependent on the package and PCB trace parasitic inductances and the output inductor parasitic capacitance.

The two phenomena and their associated parasitic elements have been identified using electrical circuit simulations of the system comprised of the integrated circuit, its package, the printed circuit board, and the external components. It allows for the prediction of the frequencies at which resonances occur in the EMI spectrum. This analysis has been validated by measurements of the spectral content of EMI propagating on a test board.

It was shown that the degradation of the BLE receiver performances by the SMPS activity, highlighted by measurements of its sensitivity, can be reduced by the modification of the SMPS output filter. By changing its frequency response based on the system parasitic elements, it is possible to shift the frequency of problematic resonances and limit the negative impact of the SMPS.

Measurements of the near-field radiated interference were conducted above the microcontroller and its external components. They demonstrate the wide spectrum of radiated EMI caused by the SMPS and the sources of these radiated EMI, generated by the SMPS power stage and the SMPS output filter, mostly by the inductor. However, the conducted EMI propagating toward the BLE receiver are sufficient to explain the degradation of sensitivity, and the effect of radiated EMI on the receiver sensitivity was not studied further.

Many of the parasitic elements involved in the degradation of the receiver sensitivity are not located in the integrated circuit or its package. Therefore, the location of problematic resonances will highly depend on the system implementation decided by the user, and it is hard to guarantee the correct operation of the system. For this reason, a part of this work was focused on the second approach to address the research problem, consisting of improving the robustness of the BLE receiver in regards to EMI.

Improving the receiver robustness

The complex architecture of the integrated BLE transceiver makes it difficult to predict how EMI would propagate through it and what their effect would be on the received signal. On one hand, electrical simulation at transistor-level proves very useful to analyze EMI propagation on small sub-circuits but cannot be used to simulate the whole system in order to analyze the impact of EMI on the sensitivity of the receiver as it would lead to excessive simulation time. On the other hand, functional simulation at system-level doesn't take into account EMI propagating through every node of the receiver, affecting the BLE signal, and causing the degradation of sensitivity.

In this regard, this work included an innovative approach intended to develop a high-level model of the system that allows the simulation of receiver sensitivity in the presence of EMI generated by the SMPS. The development of the model was based on AC transistor-level electrical simulations to extract the frequency and phase response of each of the receiver sub-circuit input terminals toward their output terminal; estimation of the corresponding transfer function and modeling in MATLAB Simulink of sub-circuits by the sum of their transfer function blocks; extraction of polluted voltage waveforms from transistor-level electrical simulation of the whole system; and injection of the polluted voltage waveforms into the high-level model through each sub-circuit terminal.

The high-level model allowed for the simulation of the studied system (the complete BLE receiver and EMI present at its terminals) to observe the degradation of the sensitivity by the SMPS with acceptable computation time. The simulation of the receiver

sensitivity indicates a strong impact of the interference via a specific terminal of the receiver analog circuitry, a terminal of the transformer located between the input pin and the LNA. The model suggest a higher sensitivity to EMI at the beginning of the Rx chain, before the BLE signal is amplified by the LNA. It highlights a flaw in the BLE transceiver design and introduces a lever to improve its robustness against interference.

The thesis proposes a deep analysis of interference generation by the SMPS, their propagation towards the BLE receiver, and their impact on its performances. The results can be extrapolated to help understand issues with the integration in a single integrated circuit of any non-linear DC/DC power converter or any wireless connectivity solution.

5.2 Perspectives

Further exploration of the SMPS filter output response and its impact on the receiver sensitivity should be conducted. Measurements correlating the filter response with the EMI spectrum and receiver sensitivity degradation could be obtained for various filter implementations by using external components with significantly different parasitic elements or by varying PCB trace lengths. Also, non-intrusive measurements inside the receiver analog sub-circuits, using the microcontroller in test mode, could be realized.

The high-level model and the development method presented in this work could be improved. The detailed method based on the use of transfer functions is only applicable to linear sub-circuits. The architecture of the mixer performing the RF signal down-conversion is based on switching transistors; therefore, a new modeling method is required. As for now, the model integrates the impact of SMPS-generated EMI on the amplification stage only, which is linear. In-band EMI directly adds up to the BLE signal; however, the impact of out-of-band EMI on the receiver sensitivity should not be totally neglected, as phenomena like inter-modulation could produce components falling into the signal band.

In future work, a complete and refined high-level model of the receiver could be used for more applications. The injection of narrow band noise could help determine the maximal acceptable noise per frequency band (inside, outside, or close to the BLE frequency band) that does not degrade the receiver BER. Also, the impact of EMI generated by sources other than the SMPS, like internal digital clocks or I/Os, could be investigated. The developed methodology could be applied to other RF systems, particularly transceivers with lower interference tolerance, on which the impact of a non-linear DC/DC converter would be greater.

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Appendices

SMPS output filter response

A

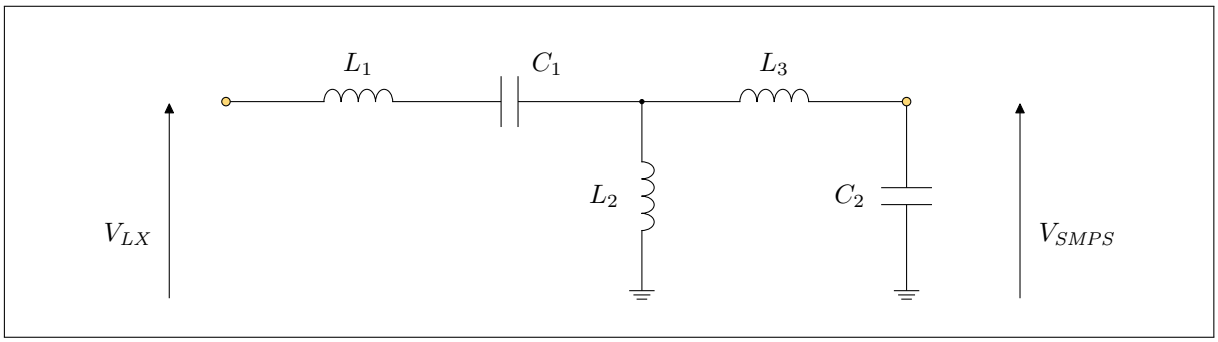


Figure A.1: High-frequency equivalent circuit for the SMPS output filter.

Transfer function:

$$H(s) = \frac{Z_{eq}}{Z_{L1} + Z_{C1} + Z_{eq}}$$

$$Z_{eq} \;=\; Z_{L2} /\!\!/ (Z_{L3} + Z_{C2}) \;=\; sL_2 /\!\!/ (sL_3 + \frac{1}{sC_2}) \;=\; sL_2 /\!\!/ (\frac{s^2 L_3 C_2 + 1}{sC_2})$$

$$Y_{eq} \;=\; \frac{1}{sL_2} + \frac{sC_2}{s^2 L_3 C_2 + 1} \;=\; \frac{s^2(L_2 + L_3)C_2 + 1}{s^3 L_2 L_3 C_2 + sL_2} \quad ; \quad Z_{eq} \;=\; \frac{s^3 L_2 L_3 C_2 + sL_2}{s^2(L_2 + L_3)C_2 + 1}$$

$$Z_{L1} + Z_{C1} + Z_{eq}$$

$$= sL_1 + \frac{1}{sC_1} + \frac{s^3 L_2 L_3 C_2 + sL_2}{s^2(L_2 + L_3)C_2 + 1}$$

$$= \frac{s^2 L_1 C_1 + 1}{sC_1} + \frac{s^3 L_2 L_3 C_2 + sL_2}{s^2(L_2 + L_3)C_2 + 1}$$

$$= \frac{s^4 L_2 L_3 C_1 C_2 + s^2 L_2 C_1 + s^4(L_2 + L_3)L_1 C_1 C_2 + s^2(L_2 + L_3)C_2 + s^2 L_1 C_1 + 1}{(sC_1)(s^2(L_2 + L_3)C_2 + 1)}$$

$$= \frac{s^4(L_1 L_2 + L_1 L_3 + L_2 L_3)C_1 C_2 + s^2[(L_1 + L_2)C_1 + (L_2 + L_3)C_2] + 1}{(sC_1)(s^2(L_2 + L_3)C_2 + 1)}$$

$$H(s) = \frac{s^4 L_2 L_3 C_1 C_2 + s^2 L_2 C_1}{s^4(L_1L_2 + L_1L_3 + L_2L_3)C_1C_2 + s^2[(L_1 + L_2)C_1 + (L_2 + L_3)C_2] + 1}$$

$$H(j\omega) = \frac{\omega^4 L_2 L_3 C_1 C_2 - \omega^2 L_2 C_1}{\omega^4(L_1L_2 + L_1L_3 + L_2L_3)C_1C_2 - \omega^2[(L_1 + L_2)C_1 + (L_2 + L_3)C_2] + 1}$$

One pole:

$$\omega^4 L_2 L_3 C_1 C_2 - \omega^2 L_2 C_1 = 0$$

$$\omega^2 L_3 C_2 = 1$$

$$\omega_z = \frac{1}{\sqrt{L_3 C_2}}$$

Two zeros:

$$\omega^4(L_1L_2 + L_1L_3 + L_2L_3)C_1C_2 - \omega^2[(L_1 + L_2)C_1 + (L_2 + L_3)C_2] + 1 = 0$$

$$\Omega = \omega^2 : \quad \Omega^2(L_1L_2 + L_1L_3 + L_2L_3)C_1C_2 - \Omega[(L_1 + L_2)C_1 + (L_2 + L_3)C_2] + 1 = 0$$

$$\Delta = [(L_1 + L_2)C_1 + (L_2 + L_3)C_2]^2 - 4 * (L_1L_2 + L_1L_3 + L_2L_3)C_1C_2$$

$$\Omega_{p1,2} = \frac{(L_1 + L_2)C_1 + (L_2 + L_3)C_2 \pm \sqrt{\Delta}}{2 * (L_1L_2 + L_1L_3 + L_2L_3)C_1C_2}$$

$$\omega_{p1} = \frac{1}{\sqrt{(L_2 + L_3)C_2}} \quad ; \quad \omega_{p2} = \frac{1}{\sqrt{(L_1 + L_2 /\!/ L_3)C_1}}$$

Cadence Virtuoso test bench

B

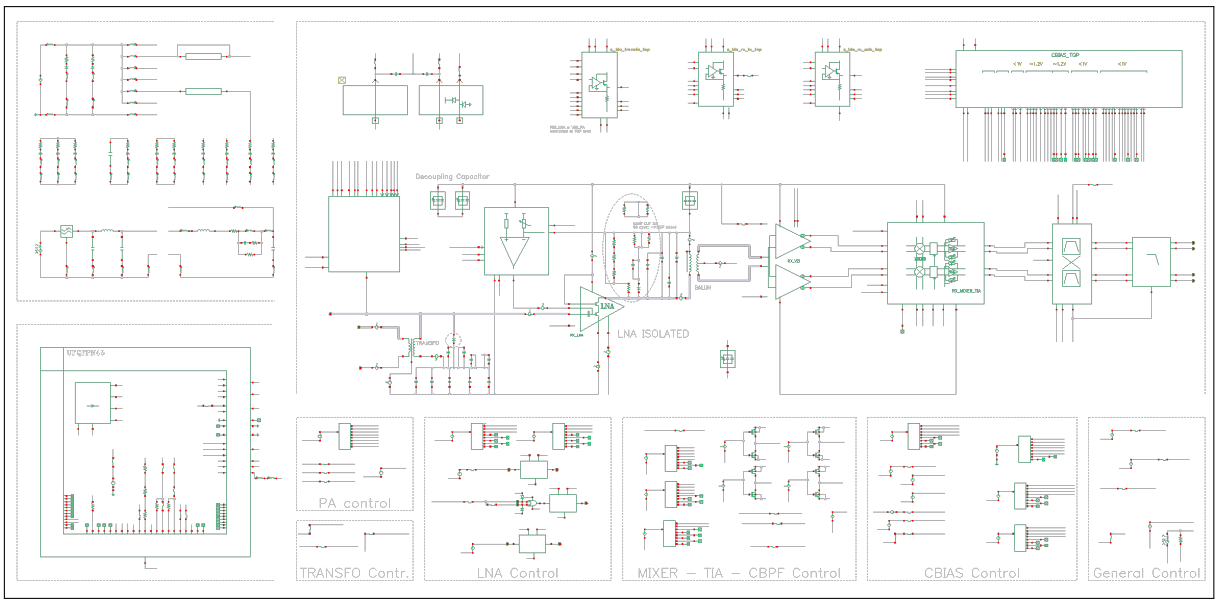


Figure B.1: Cadence Virtuoso test bench of the system with analog circuitry schematics for the receiver and the SMPS, and models for the package and the PCB.

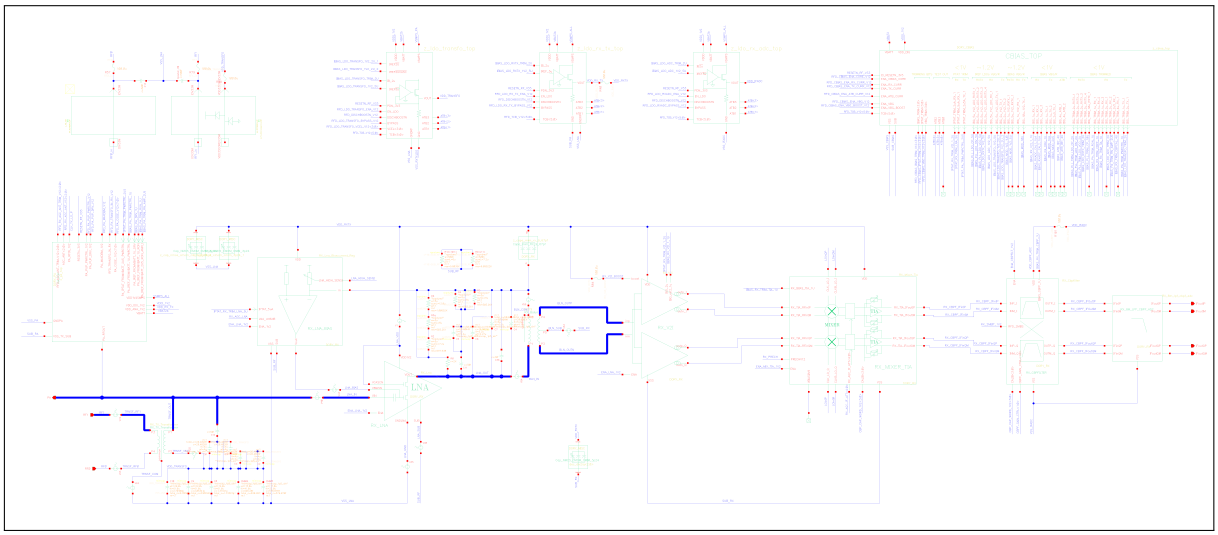


Figure B.2: Analog circuitry of the receiver with its input pads, LDOs and biasing.

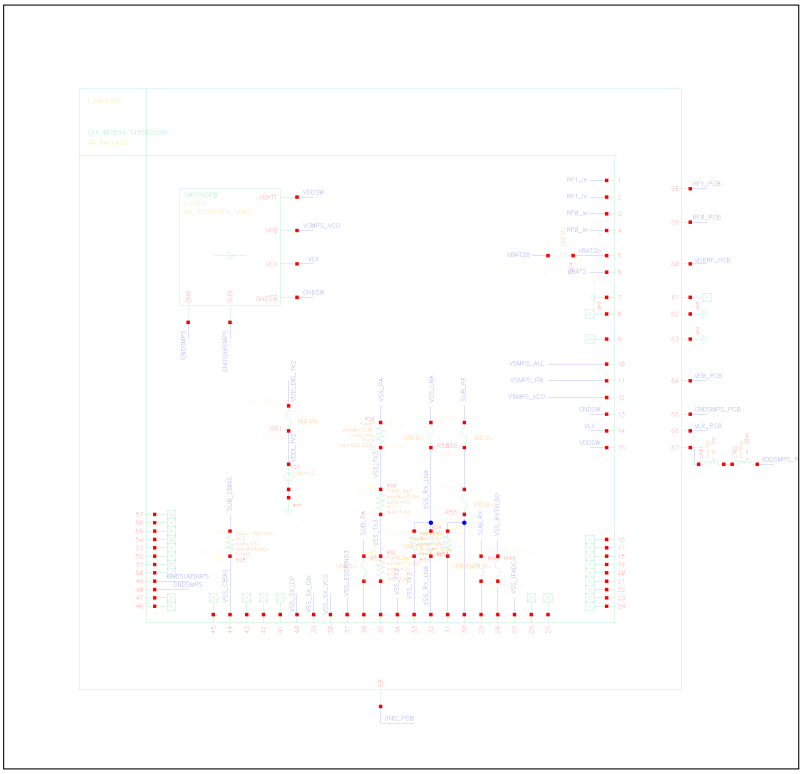


Figure B.3: RLCG model of the 68-pin QFN package and the transistor-level schematic of the SMPS power stage and its associated drivers powering the test bench.

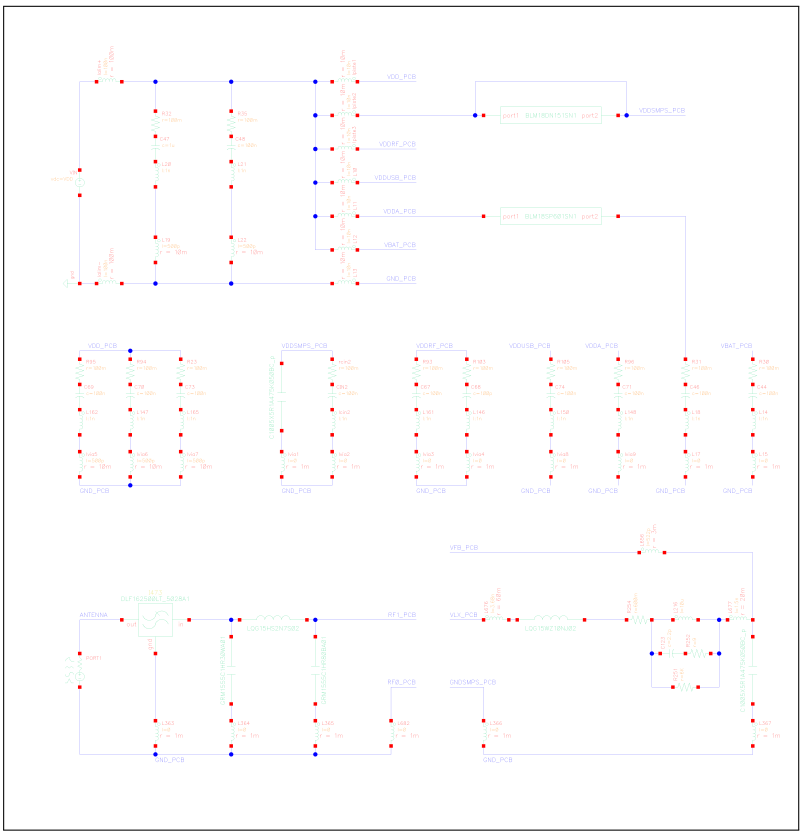


Figure B.4: RLC parasitic models of the external components mounted on the PCB and simple RL model of the PCB traces and vias.

MATLAB Simulink model

C

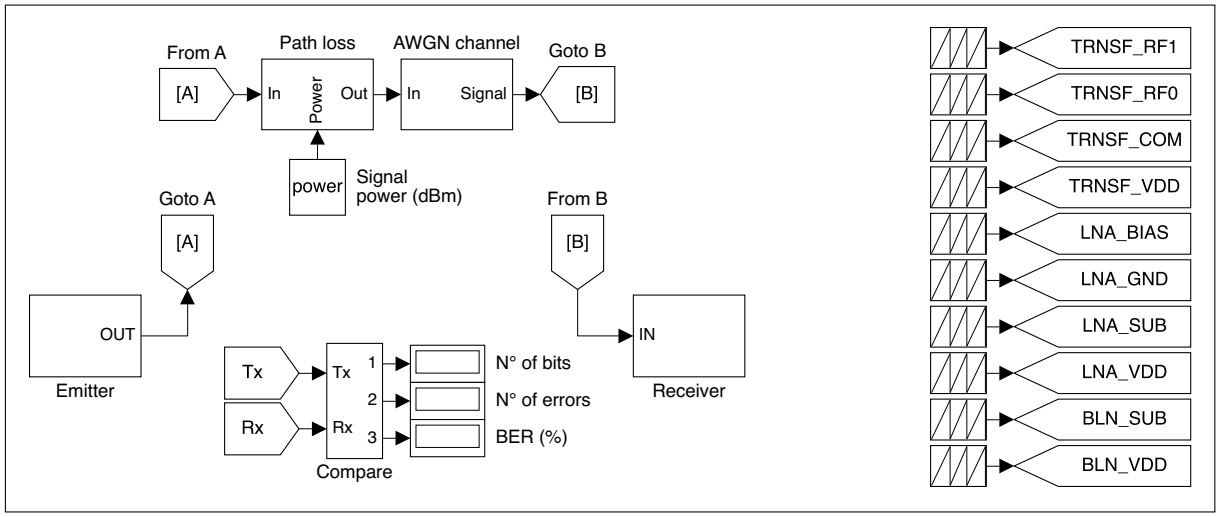


Figure C.1: High-level MATLAB Simulink model of the transceiver. The emitter generates an ideal BLE signal ; the signal is attenuated and the background noise and receiver noise figure are added to it ; the reciever demodulates the BLE signal ; the modulated bits are compared with the demodulated ones to obtain the bit error rate. On the right side, the polluted voltage waveforms are sent to the corresponding terminal of the receiver amplification stage.

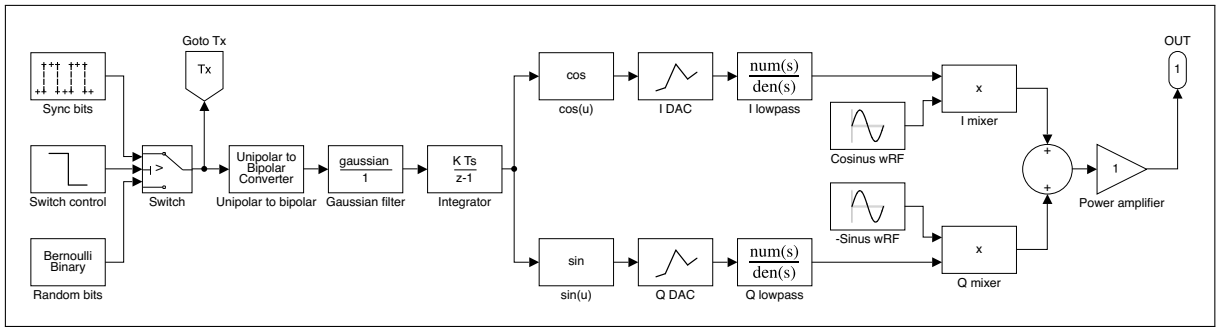


Figure C.2: Model of the BLE emitter generating an ideal BLE signal, not based on the architecture of the BLE transmitter integrated in the STM32WB55.

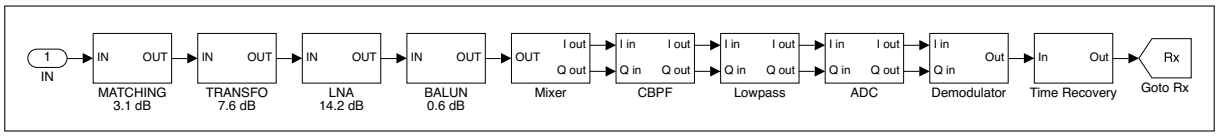
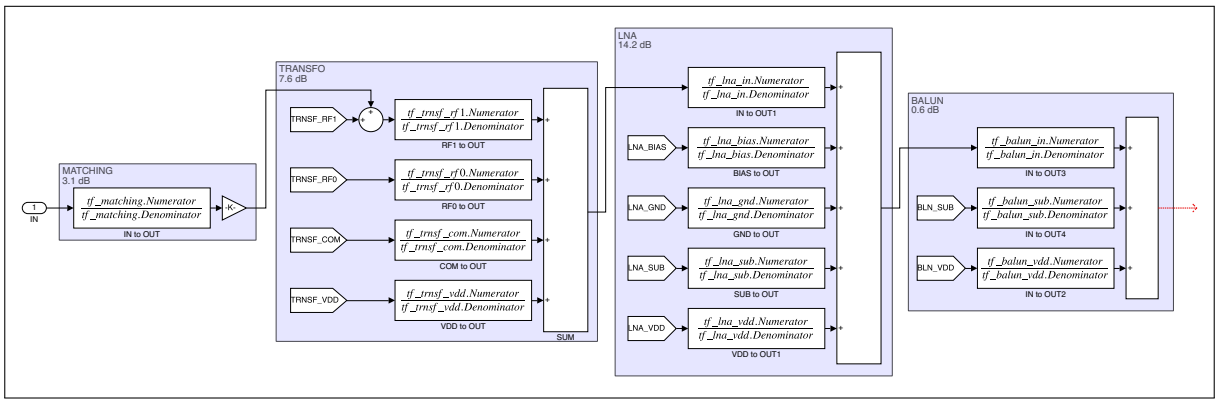
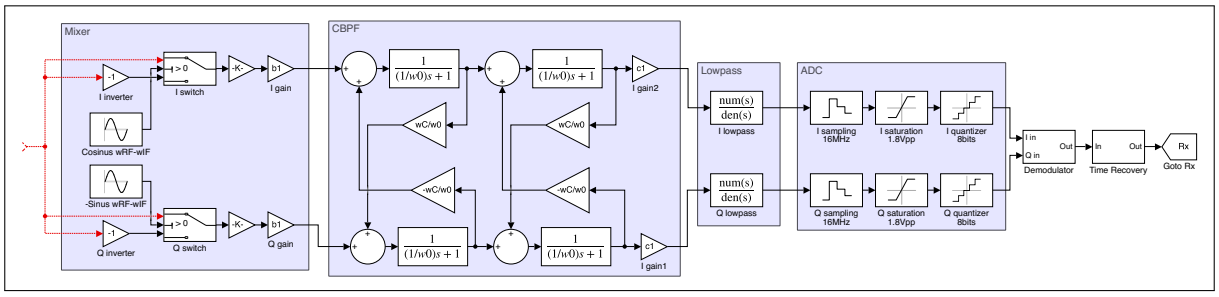


Figure C.3: Model of the BLE receiver demodulating the BLE signal, based on the architecture of the BLE receiver integrated in the STM32WB55.



(a) Model of the BLE receiver amplification stage, allowing the injection of EMI in the system to study their impact on the receiver sensitivity.



(b) Functional model only of the BLE receiver down-conversion and filtering stages, not allowing the injection of EMI in the system to study their impact on the receiver sensitivity.

Figure C.4: Expanded view of the model of the analog circuitry of the BLE receiver.

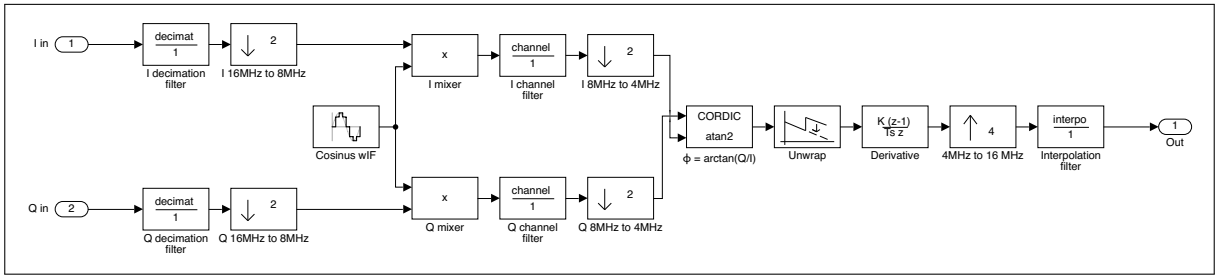
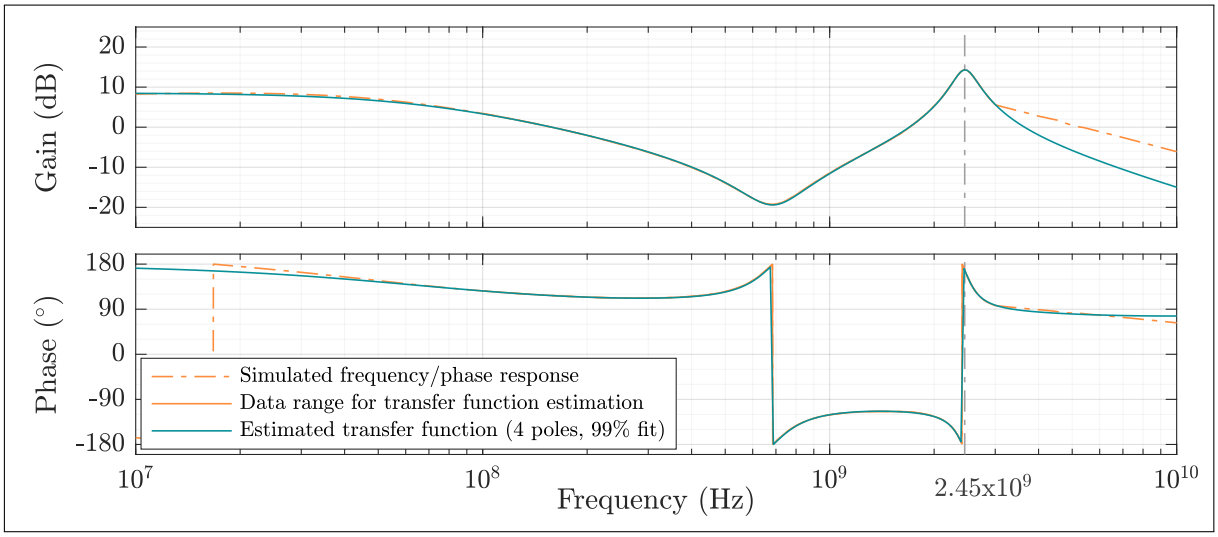


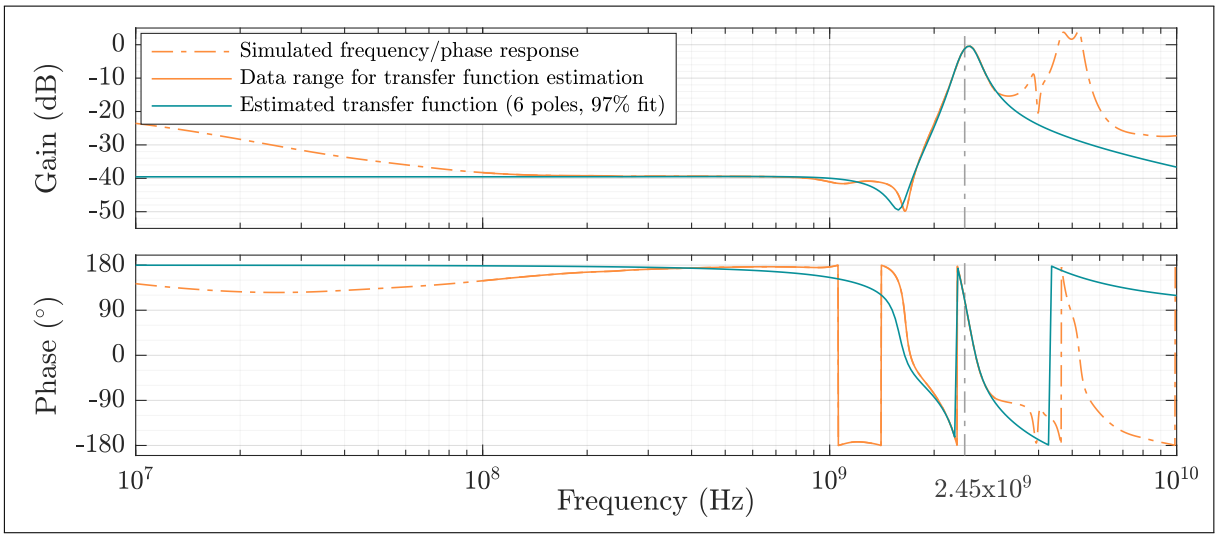
Figure C.5: Model of the digital demodulator of the BLE receiver, based on the architecture of the BLE transmitter integrated in the STM32WB55.

Estimated transfer functions

D

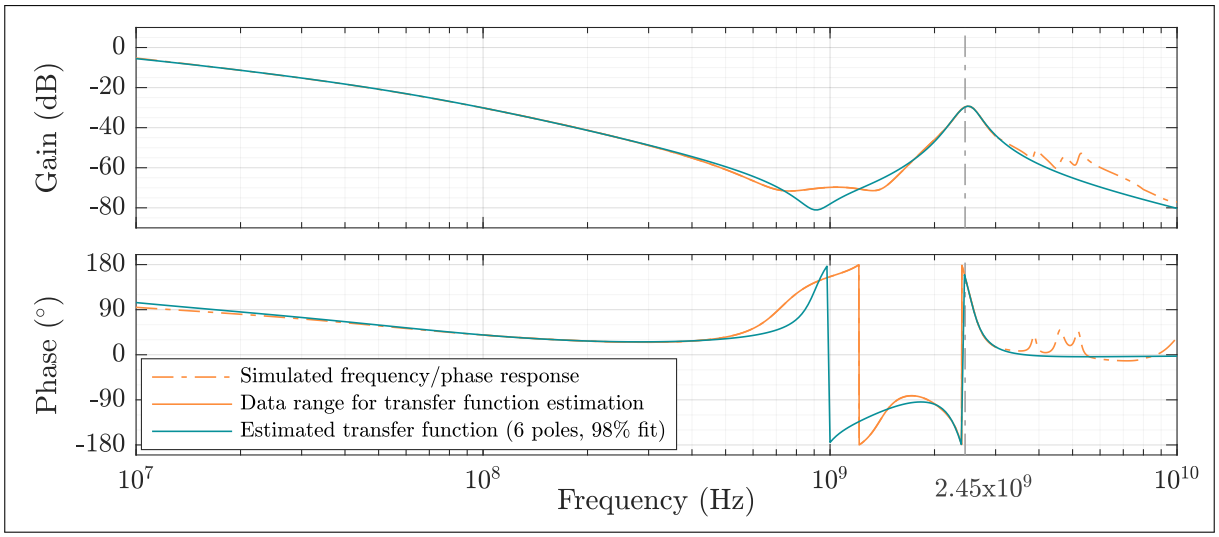


(a) LNA input terminal IN_{LNA} to its output terminal OUT_{LNA}.

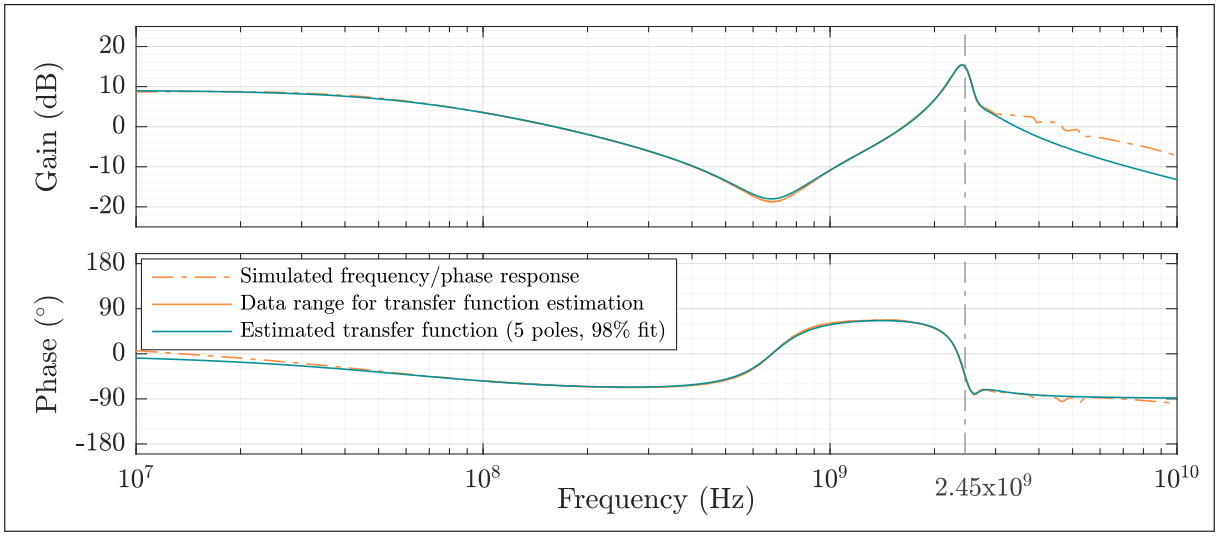


(b) LNA power supply terminal VDD_{RX} to its output terminal OUT_{LNA}.

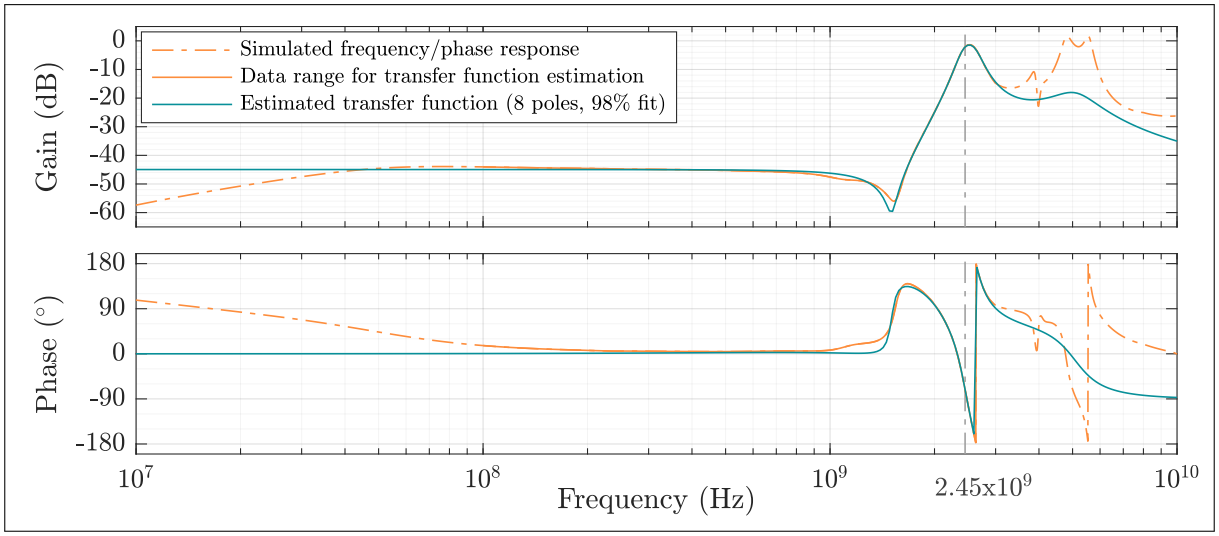
Figure D.1: Estimated transfer functions for the LNA input terminals toward its output terminal, obtained with the MATLAB function **tfest**.



(c) LNA biasing terminal V_{BIAS} to its output terminal OUT_{LNA}.

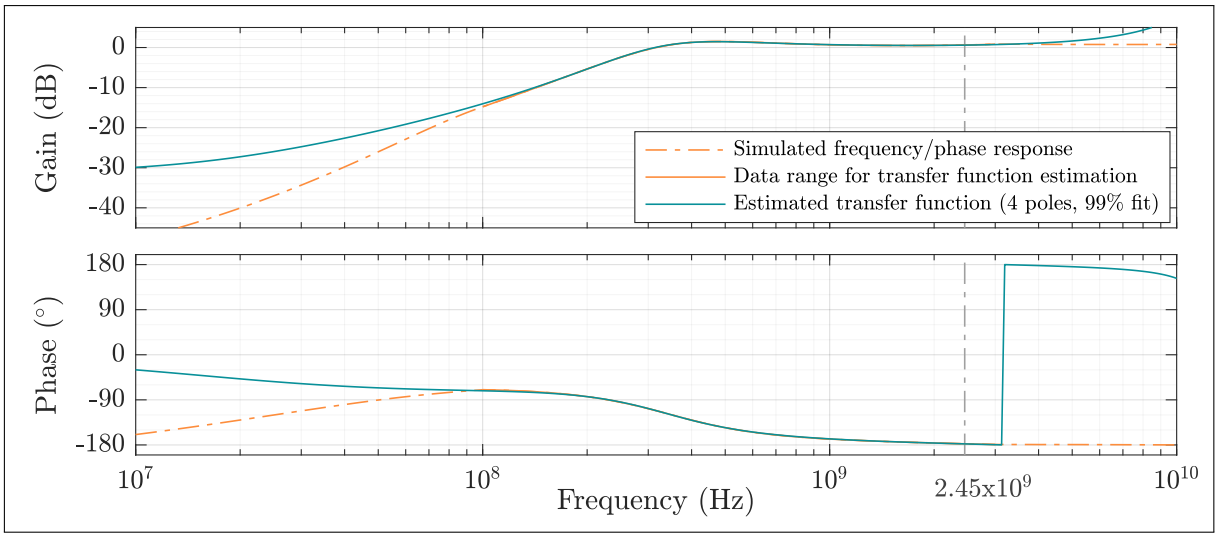


(d) LNA ground reference terminal VSS_{LNA} to its output terminal OUT_{LNA}.

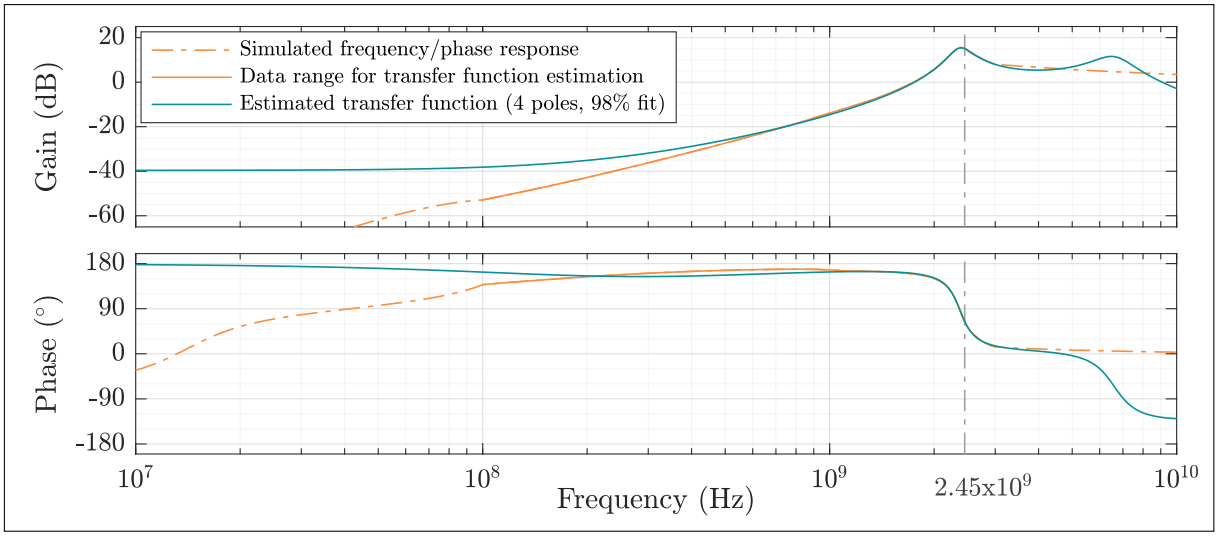


(e) LNA substrate reference terminal SUB_{RF} to its output terminal OUT_{LNA}.

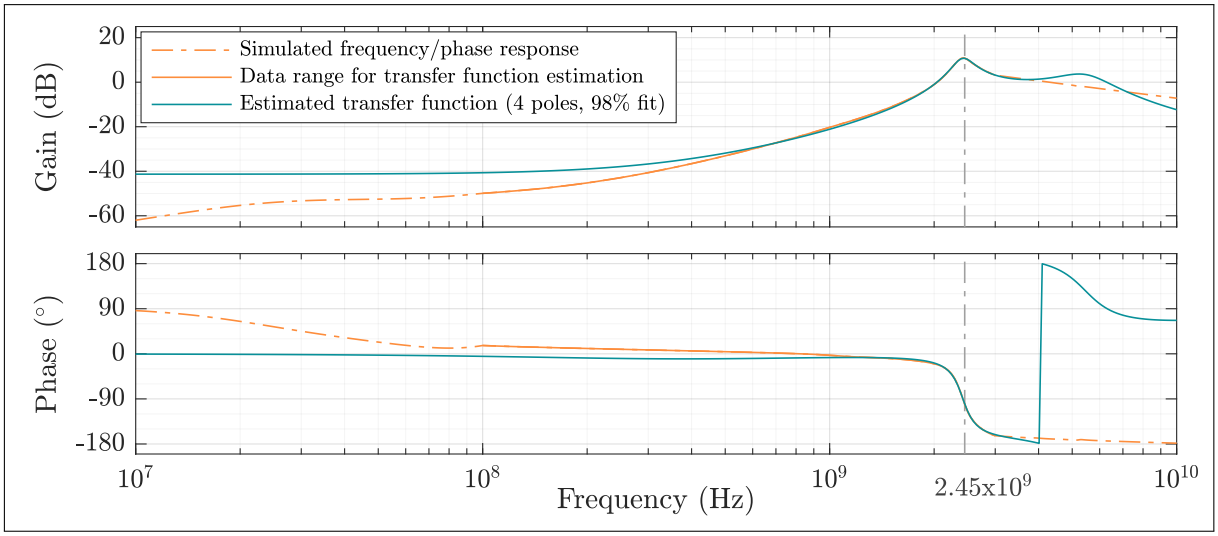
Figure D.1: Estimated transfer functions for the LNA input terminals toward its output terminal, obtained with the MATLAB function **tfest**. (cont.)



(a) Balun input terminal OUT_{LNA} to its output $OUT^+ - OUT^-$.



(b) Balun common reference terminal COM_{BLN} to its differential output $OUT^+ - OUT^-$.



(c) Balun ground reference terminal SUB_{RX} to its differential output $OUT^+ - OUT^-$.

Figure D.2: Estimated transfer functions for the balun input terminals toward its differential output, obtained with the MATLAB function **tfest**.