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Non-Destructive Testing (NDT) Method for reliability assessment of Power Electronic Modules

Anusha Gopishetti

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Anusha Gopishetti. Non-Destructive Testing (NDT) Method for reliability assessment of Power Electronic Modules. Mechanical engineering [physics.class-ph]. Université de Pau et des Pays de l'Adour, 2023. English. NNT : 2023PAUU3083 . tel-04715087

HAL Id: tel-04715087

<https://theses.hal.science/tel-04715087v1>

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THÈSE

UNIVERSITE DE PAU ET DES PAYS DE L'ADOUR (UPPA)
École doctorale Sciences Exactes et leurs Applications

Présentée et soutenue le 22/12/2023

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pour obtenir le grade de docteur
de l'Université de Pau et des Pays de l'Adour
Spécialité : Génie électrique

Non-Destructive Testing (NDT) method for reliability assessment of power electronic modules

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In 2020, I embarked on this ambitious project with excitement and apprehension. Today, with similar excitement, here is a note on completing my thesis. This journey spanned three years at PRIMES laboratory as a part of project EFICIENCE, which carried a mixture of emotions. I extend my deepest gratitude to all those who have made the completion of this thesis possible.

First and foremost, I thank Mr. Nadir IDIR and Mr. Zoubir KHATIR for agreeing to review my manuscript. I acknowledge the significant time and effort invested in reviewing this manuscript with sincere appreciation. Your dedication to excellence and commitment to advancing the field of power electronics through rigorous scholarly review left an indelible mark on my work. Your expertise in high-frequency power conversion and online health monitoring using broadband characterization and packaging has undoubtedly benefited this thesis.

I extend my sincere appreciation to all other members of the jury, Mrs. Alexandrine GRACIA, Mr. Arnaud BREARD, Mr. Laurent PECASTAING, Mr. Philippe LASSERRE, and Mr. Thanh Long LE, for your constructive feedback and valuable suggestions, which significantly enhanced the quality of this work.

Reflecting on the years spent immersed in research, learning, and growth, I am grateful and express my deepest thanks to my thesis supervisors, Mr. Paul-Etienne VIDAL and Mr. Stéphane BAFFREAU. They have been instrumental in guiding me through this process. Your expertise, patience, and encouragement were invaluable throughout this research journey.

I must acknowledge the Energy Environment Solutions project (I-SITE) of the University of Pau and Pays de l'Adour (UPPA) for their financial support, which is greatly appreciated. Eventually, I thank every partner of this project: LGP, UPPA, DEEP concept, SAFRAN Tech Paris, Tarbes-Lourdes Pyrénées, and CIRIMAT-Toulouse. Thank you for your involvement in several scientific committees and for carrying out fruitful discussions.

Special thanks to PRIMES and LGP laboratory for their assistance, especially to Karim MAROUFI for helping me to conduct experiments on the Climatic Temperature System (CTS), Davy COLIN for the active cycling test on Mentor Graphics, Caroline MARRANT, Marie TEIXEIRA, and José FERRAO for helping me in administrative stuff.

I want to thank my fellow lab mates, Romain, Mariem, Jordan, and Lola, for sharing moments of triumph and struggle, exchanging knowledge, and the collaborative environment we fostered.

I want to thank my parents, Mr. G. Anjaneyulu and Mrs. G. Manga, my sister, Likitha, and my extended family, Mr. C. Yves, Mrs. C. Sylvie, François, Rémy, and Davy, for their endless love, patience, and encouragement, which have been my stronghold. Thank you for believing in me and being there through this academic pursuit's highs and lows.

Completing this thesis has been a formidable, challenging, transformative, and enriching experience, and I am grateful for having had the support of such a wonderful community.

Acronyms

A	P
Active Metal Brazing: (AMB)..... 143	Power Cycling Test: (PCT) 55
Active Power Cycling: (APC)..... 165	Printed Circuit Board: (PCB)..... 30
Aluminum: (Al) 30	Pulsed Eddy Current: (PEC) 68
D	R
Device Under Test: (DUT) 73	Radio Frequency: (RF)..... 67
Die Attach Process: (DAP) 39	
Direct Bonded Copper: (DBC) 32	
E	S
Eddy Current Technique: (ECT)..... 68	Scanning Acoustic Microscopy: (SAM).. 173, 199
End Of Line: (EOL) 39	Self-Resonating Frequency: SRF 97
F	Silicon Carbide: (SiC)5
Front Of Line: (FOL)..... 39	Surface-Mount Device: (SMD) 30
G	T
Gallium Nitride: (GaN)5	Temperature Cycling Test: (TCT).....55, 166
	Through-Hole Device: (THD) 30
I	Time-Domain Network Analyzer: (TDNA) 72
Infrared thermography: (IRT)..... 65	Time-Domain Reflection: (TDR) 73
N	Time-Domain Transmission: (TDT)..... 73
Non-Destructive Examination: (NDE) 62	Transistor Outline: (TO) 30
Non-Destructive Inspection: (NDI)..... 62	V
Non-Destructive Testing: (NDT).....6	Vector Network Analyzer: (VNA)68, 76
	W
	wide band gap: (WBG)5

General Introduction

A variety of industries, including automotive, transportation, Information Technology (IT), and energy infrastructure (i.e., power grid), have a growing need for power electronics (power semiconductor) systems. As this trend continues, it adds critical challenges to the field of research. The major evolution of power electronics technology has always looked towards higher efficiency, high power density, and more integrated systems. This emphasis poses an increasing challenge to develop new design protocols, innovative packaging, and even new semiconductor material, as it is widely believed that Si technology has finally reached its fundamental physical limits [1]. These limitations have paved the path for introducing Wide Band Gap (WBG) devices, which show outstanding characteristics, i.e., much lower leakage current, higher operating temperatures, lower on-resistance, and higher thermal conductivity [1]. In this world where new technologies and tools are available and compelling energy problems exist, some research is devoted to integrating and optimizing different parts. Aiming to migrate perspective advantages into real-world applications. This is why well-established parts and components of power converters and systems are experiencing substantial remodeling or even a completely new design [2]. Integrating new technologies into components or modules with higher power-to-mass or power-to-volume ratios raises the question of reliability and lifetime assessment [2]. These two factors, together with ubiquitous cost-effectiveness, are the drivers for developing new technologies for power conversion. Consequently, with the usual and new technologies, there is a question of the reliability of monitoring electrical parameters as an indicator of potential failures. In such context, Non-Destructive characterizations along with monitoring parameters show some interest, as they can detect partial and complete failures. High density and high reliability are pursued, focusing research on various aspects of power converters [3]. The current evolution of static converter performances is associated with the maturity and the availability of new technologies of power semiconductor components playing the role of electronic switches, particularly in the field of transport based on Silicon Carbide (SiC) of electronic switches, and more particularly in the field of transport those based on Silicon Carbide and Gallium Nitride (GaN). These technologies must be combined with next-generation hybrid integration techniques to improve the performance of power electronic modules. Indeed, the targeted applications imply that these modules must operate in a

severe environment under strong constraints: high power density at high temperatures, switching at high frequencies, etc., with the constant objective of optimizing electrical efficiency and improving the reliability of the system. The challenges for the development of these new modules are multiple. For example, they can aim at minimizing the footprint of a conversion function by integrating several conversion architectures as well as passive elements. Within this framework, the overall project, EFICIENCE chair, to which this PhD is related, aims to enhance the efficiency of electrical energy conversion. This is achieved through a combination of approaches applied to power electronics modules. To target the problems of integration and the evaluation of the packaging damage state in power electronics, failure characterizations along with online monitoring parameters are of great interest.

Project EFICIENCE:

The project EFICIENCE (Figure 1) under the grant number PIA ANR-16-IDEX-0002, involves different partners from industry and academics, it is part of the Energy Environment Solutions project (I-SITE) of the University of Pau and Pays de l'Adour (UPPA). The global aim of this project is to improve the power converters' efficiency. Thus, the project EFICIENCE will address the integration of materials, functions, and diagnostic methods for the power electronic converters. Power electronics integration and health monitoring of power electronics packaging issues are two objectives of the chair. Combined approaches applied to power electronics modules will be studied in 3 work packages:

- 1) New materials and their implementation processes, to optimize the energy efficiency of power efficiency of power modules (materials aspect) → Objective 1
- 2) A Non-Destructive Testing (NDT) method by analysis of electromagnetic interactions (reliability aspect) → Objective 2
- 3) Power modules allowing multilevel static conversion by integrating new technologies (conversion aspect) → Objective 3



Figure 1: Logo of the project EFICIENCE

This thesis falls under the objective number 2 and deals with the NDT method for failure mode detection. The non-destructive test is based on analysis of electromagnetic interactions. In such work-package it is targeted to characterize the packaging damage state in power electronics.

Purpose and objectives of the PhD:

Power electronic modules which are widely used in the harsh environment are the core components in most of the power electronic systems, playing a major role in energy generation, transmission, and consumption systems. A converter failure will result in high maintenance cost. The system reliability, risk, and maintenance cost can be greatly improved by replacing semiconductor devices when incipient failures are detected. Therefore, building an accurate online condition monitoring model is becoming an increasingly important issue to investigate. However, the condition monitoring of power modules is still a challenge [4].

This thesis concerns the evaluation of the state of damage of the packaging of power electronics systems by an innovative non-destructive testing method. This method is developed to detect early the potential presence of defects. This method has never been proposed in power electronics. The objectives are listed as follows:

- To evaluate the state of damage of power electronic systems assembly by an innovative NDT.

- To reveal the information related to the state of damage in the temporal and/or frequency content, simulated or measured, of the conducted or radiated signals of a power module.
- To predict by simulation over a wide frequency band as well as in the non-linearities of signals, the signatures of a failure mechanisms.

The NDT must be independent of the package and the die technology. This thesis will highlight the newly developed NDT methodology applied on different power assemblies. The main target is to detect the failure signatures following wide frequency band characterization using S and Z parameters.

To demonstrate these objectives the document is organized in four chapters.

The first chapter reviews the state of the art on the discrete packages and power modules describing packaging and assembly. Following the advancement, the evolution of Wide Band Gap (WBG) power devices is mentioned. The evolution of new technologies calls for the interest of integration and optimization which indeed rise the question of reliability and lifetime of the devices. In regards of that, reliability challenges, failure mechanisms, failure mode characterizations (destructive and Non-destructive) are addressed. Also, the interest of online health monitoring and difficulties of finding good failure indicators following the new technologies are pointed out.

In Chapter 2, different characterization techniques are described. During the study S-parameters characterization is developed through a Vector Network Analyzer (VNA). This choice was made due to following reasons:

- They are available to perform wide frequency band characterizations like in Radio Frequency (RF) and microwave level
- They are easier to measure and work with high frequencies
- It is reliable to measure power waves rather than voltage and current at least at high frequencies
- They provide flexibility to convert between other parameters of the same family (Z, H, Y, ABCD parameters, etc.,)

Also, in this chapter, different steps of newly developed NDT methodology are described. This methodology is based on the periodic Radio Frequency (RF) characterization. The Spice and electromagnetic simulations are detailed.

In Chapter 3, the proposed NDT methodology is applied on the healthy state power assemblies to study their behavior. The power assemblies include TO packages and Active Metal Brazed (AMB) ceramic substrate. TO package is seen as an “unknown assembly” whereas the ceramic substrate base assembly is fully designed. The experimental setup, interface details to perform two-port characterization will be detailed.

The Chapter 4 is dedicated to present the failure signature detection using newly proposed NDT methodology. To induce failure, accelerated and manual aging tests are conducted which are detailed in this chapter. The selected accelerated aging test are Temperature Cycling Test (TCT) and Active Power Cycling (APC) test. The online monitoring parameters from these tests are presented. Bond wire related and aging of brazing failure mechanisms are highlighted. A numerical analysis has been presented following the different failure modes. Failure indicators are pointed out.

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Chapter 1 : State of the art of power modules

1.1 Introduction

Power electronics devices play a crucial role in controlling and managing electrical power in various applications. These applications ranging from basic voltage regulation in consumer electronics to complex power conversion in industrial systems and renewable energy setups. Advances in power electronics continues to drive improvements in energy efficiency and performance across various industries. The emergence of these new technologies has ignited interest in integration and optimization, leading to inquiries about the reliability and the durability of these devices. In such context, this chapter describes the issues related to reliability, failure mechanisms, and the classification of failure modes, covering both destructive and non-destructive evaluation techniques. Furthermore, it highlights the importance of online health monitoring and the associated challenges in finding effective failure indicators in the context of these evolving technologies.

1.2 Power electronics packaging technologies

Power electronics can be packaged discretely (Figure 2) or in modules (Figure 3) [5]. However, it is important to distinguish between components and modules. One of the most noticeable tradeoffs when comparing discrete power devices with power modules relates to the physical space they occupy and the power density they provide [6]. Figure 2 (c) presents the inner view of the discrete package which contain single die.

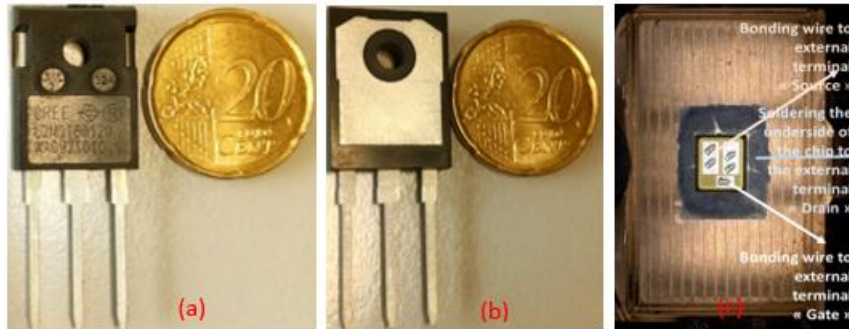


Figure 2: Discrete packaging (a) top view (b) bottom view (c) inner view of the package

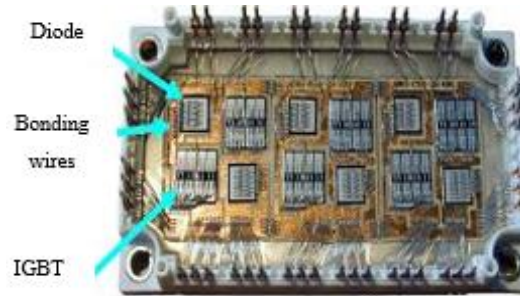


Figure 3: Power module [4]

1.2.1 Power discrete devices

Power discrete devices are single semiconductors like diodes, transistors or IGBTs, etc. [7]. These components find applications within various systems and can be broadly categorized into two main groups: power rectifiers and power switches [8]. Power transistors are significant as discrete devices, serving diverse roles to regulate voltages, mitigate power consumption, and reduce heat generation. Emerging wide-bandgap power devices, such as GaN and SiC, have expanded the possibilities, offering solutions for both low and high-power applications at high frequencies. These technologies spread to various sectors, including consumer electronics, power grid infrastructure, energy, transportation, and the automotive industry [7].

Power devices come in two primary material categories: those based on silicon and those employing wide-bandgap materials. Examples include power metal-oxide-semiconductor field-effect transistors (MOSFETs), power diodes, thyristors, and insulated gate bipolar transistors (IGBTs). Notably, some of these technologies possess the characteristics required to meet the demands of high-reliability systems, such as those used in aerospace applications like airplanes, helicopters, and satellites. Consequently, there is a pressing need for in-depth research into the packaging techniques and reliability assessment of these power devices [9].

1.2.2 Power discrete device packaging and assembly

Packaging is crucial in unlocking electronic devices' complete potential [10]. There exist different components following the mounting technology of the electronic components. The two main families of components:

- Through-Hole Devices, commonly known as THDs
- Surface-Mount Devices (SMDs)

The through-hole involves the use of leads on the components that are inserted into the holes drilled in Printed Circuit Boards (PCBs). These leads are then soldered to pads on either the same side or the opposite side of the PCB, and this assembly process can be achieved through manual placement (by hand) or by employing automated insertion mount machines [11].

Surface mount devices, often referred to as SMDs, are electronic components that are fixed to the surface of a PCB using Surface-Mount Technology (SMT). Initially, this technology was known as planar mounting [11].

Following the JEDEC standards, a standard mark called “Transistor Outline (TO)” is defined to distinguish different TO packages following their characteristics [12]. TO power product is a typical discrete power package still used today. Figure 4 presents the design of a typical discrete power package TO-220. Its construction consists of a power MOSFET or IGBT die, solder paste for die attach, lead frame and pad, bond wires, and Epoxy Mold Compound (EMC) [13].

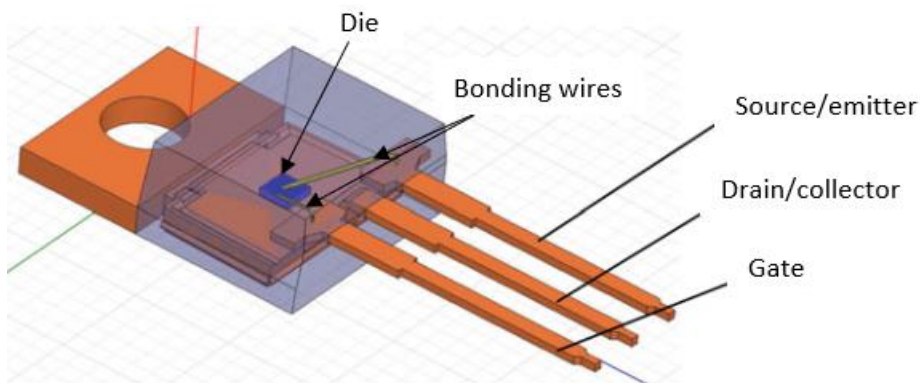


Figure 4: The design of a typical power discrete package TO-220 [13]

The power MOSFET/IGBT connects the source/emitter lead through a larger diameter metal (such as Aluminum (Al) bond wire). The gate of the MOSFET/IGBT connects to the gate lead with a smaller diameter bond wire. The basic assembly process for a discrete power device includes: the power wafer dice, die pick up and die attaches to the dap of the lead frame, wire bonding the source/emitter of the power die to the source/emitter of

leads and gate of the power die to the gate lead, molding, trim/form and singulation [14]. Normally, the designs often require custom mounting process which basically includes leads forming and the heat sink mounting. Improper handling of lead forming of the devices and the heat sink mounting can result in immediate or latent failure from cracked epoxy, epoxy delamination, die fractures, and bond-wire shearing [15].

Table 1 presents different TO packages that were studied during this thesis. It presents the device reference, type of package, type of power device, maximum voltage and current ratings followed by the image of the device.

Device	Package & device type	Voltage (V)	Current (A)	Image
C2M0160120D	TO-247-3 SiC MOSFET	1200	18	
IRL520NPBF	TO-220AB Si MOSFET	100	10	
STF11NM60ND	TO-220FP Si MOSFET	600	10	
STW26NM60ND	TO-247-3 Si MOSFET	600	21	
SCT3080ALGC11	TO-247N SiC MOSFET	650	30	
SCT2160KEC	TO-247 SiC MOSFET	1200	22	
IRLI540NPBF	TO-220 Si MOSFET	100	23	
FQU13N10LTU	TO-251 I-Pak Si MOSFET	100	10	

Table 1: Different discrete devices

1.2.3 *Power electronic modules*

Power modules are widely used, especially in converter applications. They are comprehensive assemblies that contain multiple power chips, primarily power semiconductor devices, as well as insulating materials, electrical connections, mechanical supports, and encapsulation. These components work together for efficient power conversion. In some cases, these modules also include control electronics like gate drivers, sensing components, and protection functions. When these control elements are integrated within the power module package, they are known as Intelligent Power Modules (IPMs) [16].

Power modules offer several benefits, including the tight integration of multiple power semiconductor devices, the capability to handle high current and power ratings by paralleling multiple semiconductor dice within the module, effective thermal management, and mechanical durability. Perhaps the most significant advantage is the minimization of parasitic elements, especially parasitic inductances, thanks to this close integration.

Figure 5 illustrate different components of standard power module. The semiconductor chips/dice are brazed on a Direct Bonded Copper (DBC) substrate and interconnected with wire bonds. The substrate is then fixed onto a sole which provides mechanical support for the assembly and heat transfer to the cold source. The ceramic substrate also plays an insulating role. The electrical connections inside the power modules are achieved by wiring, or bonding. Finally, the assembly is boxed and encapsulated with a silicone gel to enhance the performance, reliability, and longevity of power modules. To maintain the junction temperature of components below a critical value during the operating cycle, the power module is fixed on a cooling system [16]. It can be clearly seen that the power electronic modules have a combination of materials that will behave differently under thermal and vibrational loading [17].

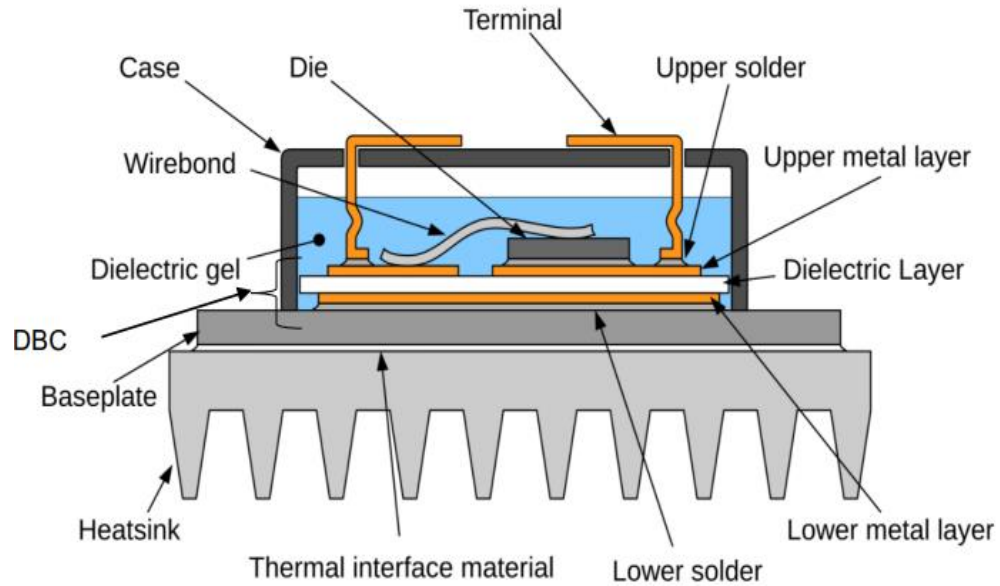


Figure 5: Standard power module [18]

Different elements of the power module are described below:

- (a) *Semiconductor chips*: it serves as the foundation of a power electronic module, where semiconductor chips dictate the voltage, current, and power specifications of the module. Power modules come in various power converter configurations, like half-bridge and full-bridge, based on how the semiconductor chips are interconnected internally. To achieve a high current capacity, multiple semiconductor chips can be parallel within the power electronic module [16].
- (b) *Direct bonded copper (DBC) substrate*: the DBC “Direct Bonded Copper” substrate acts as a bridge between the electric components in the power module and the heat sink (cooling system). It comprises a ceramic insulator layer with copper bonded to one or both sides by a high-temperature melting and diffusion process. Its primary role is to provide electrical insulation between the active elements (chips) and the sole (in contact with the outside environment). The upper layer of the copper allows the chips to interconnect. This substrate adds thermal resistance between the chips and the sole, which mainly depends on the properties of the insulation material used and significantly characterize the efficiency of the heat exchange [19].

- (c) *The baseplate*: the baseplate functions as a foundational support for all the elements within a power module. Its primary purpose is to provide mechanical stability for the module's components and facilitate their placement on heat exchangers. To fulfill its role effectively, the baseplate needs to possess desirable mechanical attributes such as stiffness, low weight, and a minimal coefficient of Thermal Expansion (CTE). Typically crafted from copper, it is usually a few millimeters thick.
- (d) *The solder*: the soldering case serves a multifaceted role by simultaneously fulfilling several functions. It enables the assembly of various components and plays a vital role in facilitating the thermal transfer between the active elements and the substrate. Furthermore, it establishes the connection between the semiconductor and the metalized substrate, which in turn connects to the external power interfaces. The lower and upper solder layers provide mechanical integrity between the substrate (DBC) and the chip. The thickness of the soldering layer can vary from a few tens to hundreds of micrometers. It is essential for this soldering to exhibit low thermal resistance and excellent electrical conductivity, especially in the context of the lower part of the chip, which corresponds to an electrode connected to the DBC through the upper solder layer [16].
- (e) *Dielectric gel*: the module case, once assembled, is filled with silicone gel. This gel serves as a protective barrier with stable dielectric strength, enhancing resistance to partial discharges and safeguarding the module from oxidation and ambient humidity. However, it comes with the drawback of having a restricted temperature tolerance, up to 200 °C, and relatively low thermal conductivity.
- (f) *Case*: the entire power module is enclosed within a polymer or metal casing to shield it from environmental contaminants and fluctuations. This casing is designed with low thermal resistance, ensuring efficient heat transfer between the modules and its external surroundings.
- (g) *Wire bonding*: the electrical connection between the top connections of semiconductor chips and module terminals are established through a process known as wire bonding [16]. Wire bonding is a solid-phase metal welding method that employs heat, pressure, and/or ultrasonic energy to create a bond between a

wire and a pad through the sharing of electrons or atom interdiffusion [20]. Wire bonding is the most established and widely adopted technology in the industry due to its simplicity, versatility, and cost-effectiveness. Currently, it is estimated that over 90% of manufactured packages rely on this method [21]. Wire bonds can be formed using a range of machines, from manual to automated models. The primary aim is to create a connection with minimal resistance, strong mechanical durability, and exceptional reliability under various conditions. Nevertheless, achieving these fundamental goals depends on factors such as the substrate material and its characteristics as well as various wire bonding parameters like temperature, duration, and applied force during the wire bonding procedure [22]. The bonding wires used for the power part are often aluminum and have a diameter between 100 μm and 150 μm . For the transport applications, specifically for railways it can go to maximum of 500 μm . The aluminum of bonding wires is often combined with alloys which reduce the risk of corrosion (Nickel) or even increase its hardness (Silicon) [21].

Two basic techniques are currently used: *wedge wire bonding* and *ball wire bonding*. For each technique, there are three wire-bonding processes shown in Figure 6: *thermo-compression* (thermal energy is applied to form a wire bond), *ultra-sonic* (energy for the weld comes from ultrasonic forces), and *thermo-sonic* (uses ultrasonic and thermal energy to form a wire bond). Figure 6 presents the schematic illustration of different bonding process.

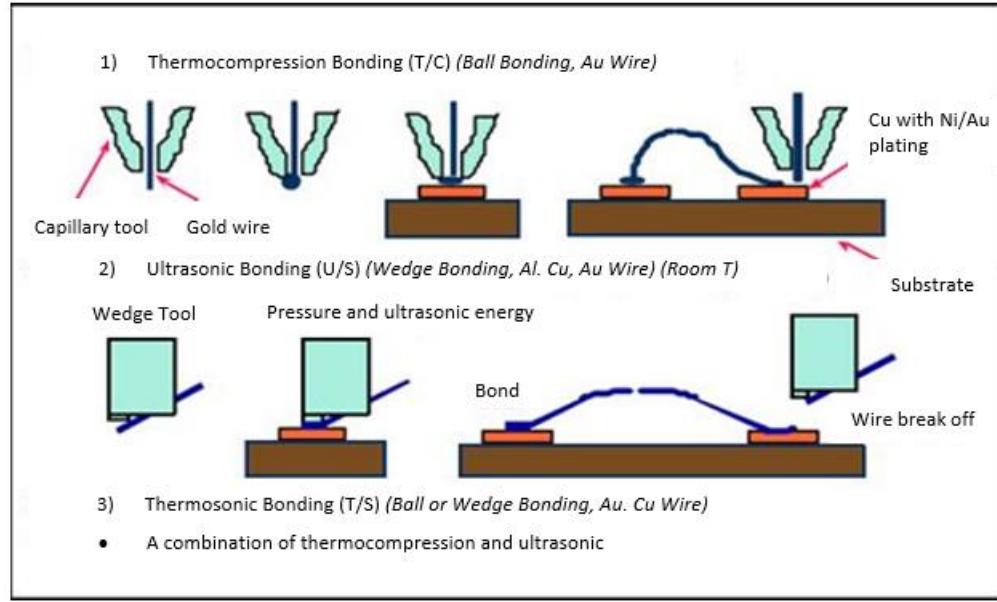


Figure 6: Schematic illustration of different bonding processes [22]

Process	Force (cN)	Temperature °C	Ultrasonic Power	Wire	Pad
Thermocompression (TC)	30 - 150	250 - 500	-	Au	
Ultrasonic (US)	25 - 45	Ambient	100 – 150 mW (@ 60 – 120 kHz)	Al, Au	
Thermosonic (TS)	30 - 90	80 - 200		Au	Al, Au

Table 2: Parameter description of Wire-bonding processes [20]

Wedge wire bonding typically uses the thermo-sonic and ultra-sonic techniques depending on the application requirements. The aluminum wire is placed in a movable head comprising a guide and a knife. The welding between the wire and the metallization is carried out by applying a force of the order of 150 gf (gram force) on the wire, combined with a vibration whose energy is adjustable in time and power [20]. This ultrasonic energy causes heating of the bonding foot and its welding. The head then rises and moves horizontally before descending and making one or more additional welds, if necessary. The knife then makes it possible to cut the wire.

Ball wire bonding involves passing a wire through a heated capillary to create a molten ball at the end, followed by applying force to crush the ball, enabling atom diffusion and chip metallization. Subsequently, the tool is lifted to form a loop, perform a second weld, and cut the wire. Parameter descriptions for the process are available in Table 2.

Ribbon bonding is another possible bonding wire technique presented in Figure 7. Ribbon bonders are essentially wedge bonders with flat ribbon wire, offering a larger bond area for potentially increased reliability. The advantages of this technique are as follows [21]:

- Higher current density
- Stronger attachment area with respect to thermo-mechanical cycling
- At higher frequency, the low thickness to the width ratio makes it possible to reduce the parasitic inductance

Also ribbon connection provides low impedance and the considerable heat dissipation. Due to these characteristics' ribbons are frequently used, for example in RF technology [23].

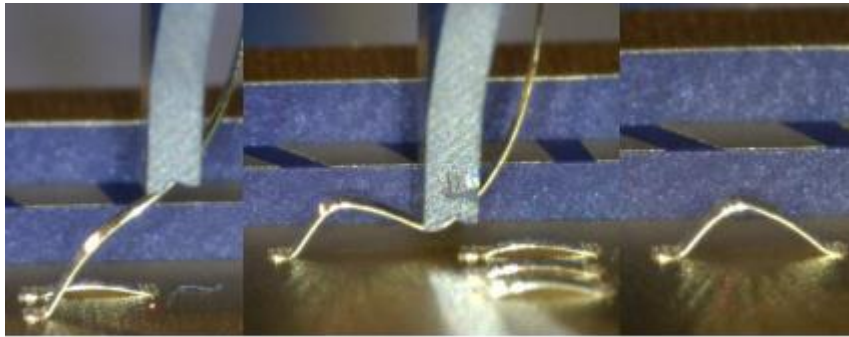


Figure 7: Bonding process with ribbon wedge [23]

Other techniques are possible such as connection by balls (solder bump) or connections by nano and micro-posts. However, these techniques are still far from the industrial applications.

To assess the quality of a wire bond, electrical testing is carried out to confirm the establishment of a low-resistance path, and pull tests are commonly employed to gauge the bond's strength. Challenges arise when making wire bonds on substrates with smaller bond pads compared to larger ones, as the increased vertical pressure from the wire bonder on smaller pads can lead to potential deformation of the bonding pad and substrate material, especially at elevated bonding temperatures [22].

1.2.4 Power module packaging

Packaging is an important step in the assembly process of an electronic chip. A package must assure the following functions [21]:

- *Die protection and mechanical resistance:* the aim is to ensure the die disposing (as a function of package dimensions, shape, weight, etc.), and its mechanical and chemical protection against environment (vibrations, temperature variations, dust, moisture, etc.).
- *Consistence with the needs of the system:* a specific interest is granted to electrical properties (electrical insulation and conduction), heat transfer capacity.
- *Interface between the die and the electrical system (outside world)*
- *Favorable costs*

The field of power electronic packaging is experiencing rapid technological progress. It is driven mainly by the expanding market for power electronic applications. This applications include automotive, railway, home electronics, consumer electronics, and high-power industry [24]. However, due to intrinsic high-power dissipation, the performance requirement for power electronics is incredibly high, especially in handling harsh thermal and electrical environments. The advancement of power packages depends on the integration progress of power devices. Current power devices have two major integration mode: *Monolithic integration* and *hybrid integration*.

- *Monolithic integration* includes power integrated circuits, High Voltage Integrated Circuits (HVIC), and intelligent discrete power devices combined with functional integration and the integration of passive elements
- *Hybrid integration* includes the standard power module and the intelligent power module

Today, the trends of monolithic integration favor 3D heterogeneous and hybrid integration for higher switching frequencies, reduced bulky components, and soft switching for efficiency and low harmonics. Silicon carbide (SiC) and other wide band gap (WBG) semiconductor devices are ultimately important elements for hybrid integration to advance

system dynamic characteristics, overload capability, device ruggedness, and thermal and electrical performance [25].

The power integration is usually presented in three subsets shown in Figure 8:

- Semiconductor elements (packaging level 0)
- The assembly, composed of the metallized insulating substrate, the sole, the electrical connections, and soldering allowing the mechanical maintenance of the whole (packaging level 1)
- Protection to the device with the case and the gel (packaging level 2)

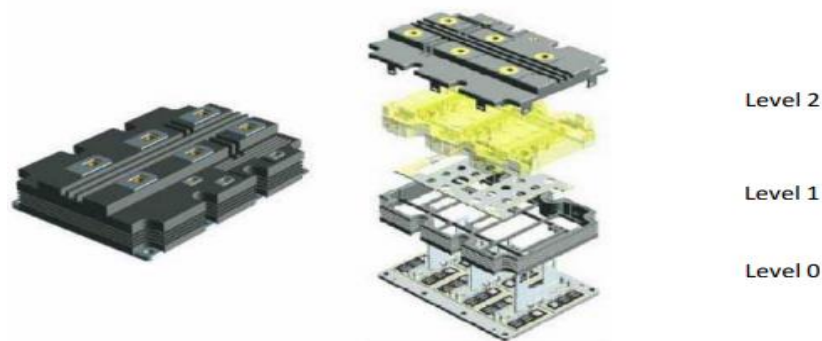


Figure 8: Typical power module packaging levels [26]

Integration in power electronics is rather a complex process due to incompatibility of materials, processing methods used in fabrication, high density levels, and electrical isolation requirement. Packaging involves the solution of electrical, mechanical, and thermal problems [24]. Once the device is packaged, the next step is to assemble the rest of the power electronic circuit [27].

1.2.5 Power module assembly

Assembly manufacturing processes can be categorized into two blocks: Front of Line (FOL) and End of Line (EOL), with multiple process steps in each.

Front of line (FOL): in *FOL* manufacturing, the standard procedure involves the wafer handling process. This procedure includes picking up dice from a tape, which can become more intricate as dice thinning becomes more extreme, die-attach, and wire bonding [24].

End of line (EOL): the typical processes in *EOL* includes molding process, molding ejection, and clamping process.

Here, the major focus is on the Die Attach Process (DAP). Inspecting all components thoroughly before die assembly is the recommended step. Regardless of precise assembly processes, the component condition, as well as the environment, greatly influence the final assembly quality [28]. The selection of die attach material becomes critical to ensure package robustness and reliability [29].

Die attach: die attach is the process of attaching a die/chip to a substrate or package. For example, in the power module of Figure 9, the IGBT chip and the diode chip are attached to the top copper layer of the DBC substrate [16].

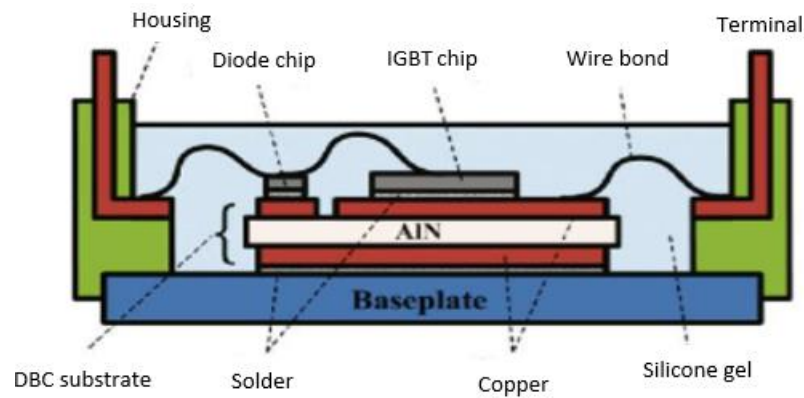


Figure 9: Cross section of IGBT power electronic module [16]

There are different die attaching techniques. The two most commonly used are *eutectic die attach* and *adhesive die attach*. Both of these processes use special die attach equipment and die attach tools to mount the die.

- a) *Eutectic die attach:* this technique is commonly employed in hermetic packages, uses a eutectic alloy to attach the die to the cavity. A eutectic alloy is the alloy with the lowest melting point possible for the metals combined in the alloy. The gold-silicon (Au-Si) eutectic alloy is the most commonly used die attach alloy in semiconductor packaging [30]. For example, the preform formed by combining gold and silicon contains melting point of 363°C while the individual melting point of gold and silicon is 1640°C and 1414°C respectively [16]. Table 3 presents different composition of alloys and their melting points in liquids and solids state.

Composition	Temperature (°C)	
	Liquids	Solids
80% Au, 20% Sn	280	280
92.5% Pb, 2.5% Ag, 5% In	300	-
97.5% Pb, 1.5% Ag, 1% Sn	309	309
95% Pb, 5% Sn	314	310
88% Au, 12% Ge	356	356
98% Au, 2% Si	800	370

Table 3: Compositions and Melting Points of some Eutectic Die Attach Preforms [30]

A typical soft solder DAP is shown in the Figure 10. A lead frame is held on the surface of the heater block. The soft solder is then placed on the lead frame. A die holder (vacuum collect head) picks the die with metallization from the tape. The temperature of the heater block is raised up to the melting temperature of the solder wire which makes the wire fuse. Finally, the die which is held by the die holder is placed on the melt solder which on the lead frame, and as soon as the solder cools down a solid connection is established. The most commonly used preforms for the power electronics nowadays are SAC305 or SnAg.

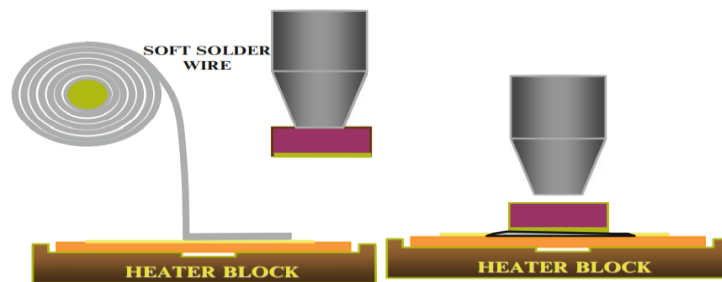


Figure 10: Soft solder die attach process [24]

- b) *Adhesive die attach*: this technique uses a polymer-based die attach adhesive, typically epoxy resin for attaching the die to the substrate. Figure 11 presents the adhesive DAP as the grainy material between the die and the die pad. Due to its lower thermal and electrical conductivity properties this technique is limited its application. In addition, power modules often experience high levels of thermal stresses due to their operational demands. Adhesive materials may not withstand repeated thermal stresses as effectively solder or eutectic materials. Over time, the

adhesive can degrade, leading to potential reliability issues and module failure [16].

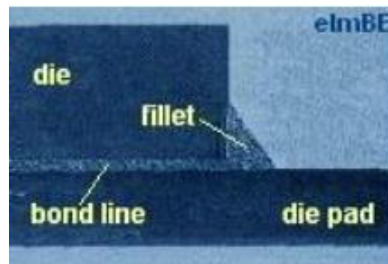


Figure 11: Adhesive DAP as the grainy material between the die and the die pad [30]

In all of the methods discussed above, to select the right material and maintaining the correct thickness of soldering is the key to optimizing the reliability. Great care must be taken when placing the die into wet paste. The die needs to be flat and level, with respect to the substrate.

1.3 Semiconductor device functioning and characteristics

A power semiconductor device is typically employed in a “commutation mode” (i.e., it is either on or off), and therefore has a design optimized for this specific mode of operation. The most common power semiconductor devices used in power electronics are power MOSFETs, power diodes, IGBTs, and thyristors [16]. Power MOSFETs and power diodes function similarly to low-power counterparts but handle higher current and tolerate larger reverse-bias voltage in the off-state.

1.3.1 Power diode

A power diode, frequently employed in power electronics circuits, shares the fundamental attributes of a standard diode. It possesses two terminals and allow current flow in a single direction. Nevertheless, a power diode is specially designed to accommodate higher current ratings, leading to variations in its construction compared to a standard diode [31].

Diodes represent the most basic semiconductor devices, characterized by their simple structure comprising just two layers, two terminals, and a single junction. In the case of typical diodes, this junction is created by the combination of p-type and n-type semiconductors. The lead connected to the p-type is known as the anode, while the opposite lead attached to the n-type is referred to as the cathode [31].

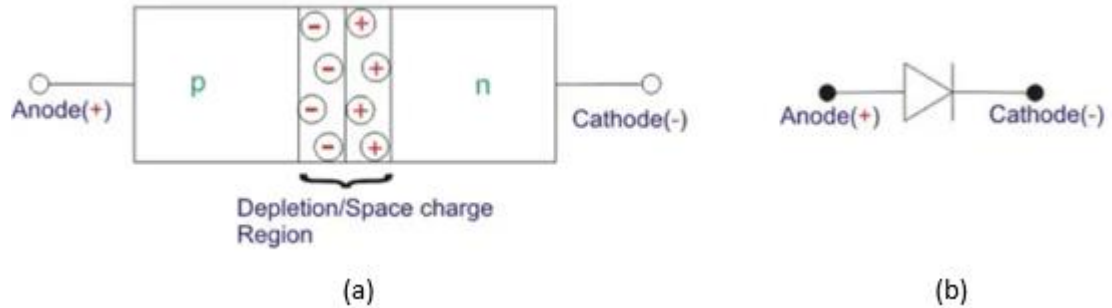


Figure 12: (a) Structure of diode (b) symbol of diode [31]

Figure 12 presents the structure of an ordinary diode and its symbol. Regular diodes have a PN junction, where both P and N sides have the same doping level. In contrast, power diodes feature a junction between a heavily doped P^+ and a lightly doped N^- layer, with the N-layer epitaxially grown on a heavily doped N^+ layer, resulting in the structure shown in Figure 13 [31].

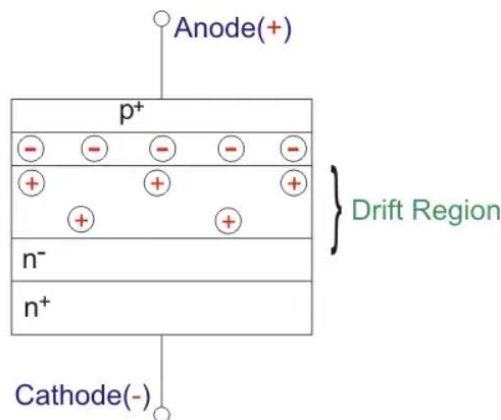


Figure 13: Power diode structure [31]

The light doping of the N- layer increases the thickness of the depletion region, allowing the diode to withstand higher reverse-biased voltages, resulting in a greater breakdown voltage. However, this N- layer also raises the diode's ohmic resistance, causing increased heat generation during forward conduction. Consequently, power diodes require specific heat dissipation methods and mountings [31].

Figure 14 presents the I-V characteristics of a power diode. In signal diodes, forward bias results in exponential current growth, but in power diode, high forward current causes a significant ohmic drop, leading to a nearly linear current increase [31].

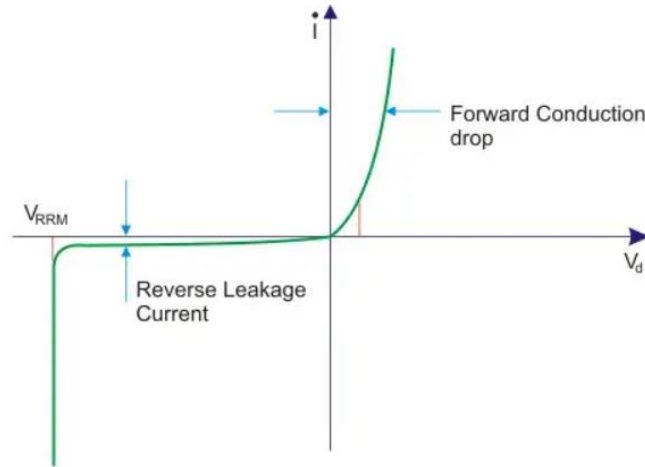


Figure 14: I-V characteristics of diode [31]

The diode's maximum reverse voltage tolerance is represented by V_{RRM} , known as peak reverse repetitive voltage. Exceeding this voltage causes a sudden surge in reverse current, potentially damaging the diode as it is not designed to handle such high heat. This voltage is also referred to as peak inverse voltage (PIV) [31].

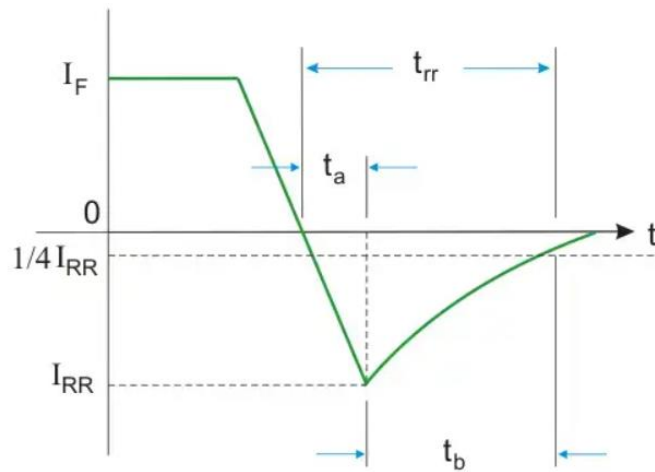


Figure 15: Reverse recovery characteristics of power diodes [31]

Figure 15 illustrates a power diode's reverse recovery behavior. When the diode turns off, the current decreases from I_F to zero and further continues in reverse direction owing to stored charges in the space charge and semiconductor regions. This reverse current reaches a peak, I_{RR} , and gradually returns to zero, signifying the diode's off state after the t_{rr} time. The t_{rr} , or reverse recovery time, is the duration between the point where the forward current reaches zero and when the reverse current drops to 25% of I_{RR} , indicating that the diode has regained its reverse blocking capacity [31].

1.3.2 Power MOSFET

The power metal-oxide semiconductor field-effect transistor (MOSFET) is a unipolar, majority carrier, and voltage-controlled device. It is of the most commonly used power device because of its high attractive properties like fast switching speed, easy gate driving, and low loss dissipation.

Over recent years, power semiconductor electronics have undergone rapid advancements to fulfill the demands of emerging applications characterized by shrinking technology sizes and increasing current density. Vertical trench technology is the prevailing configuration in the market for low-power and high-current-density applications. Figure 16 presents the DMOSFET design featuring a double-diffusion structure, comprising of a P-base region and an N^+ source region [32]. The channel of electrons is formed in the p-type region under the gate when the gate to source voltage is polarized above the threshold. From the packaging point of view, most importantly, the source (S) terminal is placed over the drain (D) terminal forming a vertical structure. As a result, the power current flows beneath the gate area vertically between the source and drain terminals through numerous n^+ sources conducting in parallel.

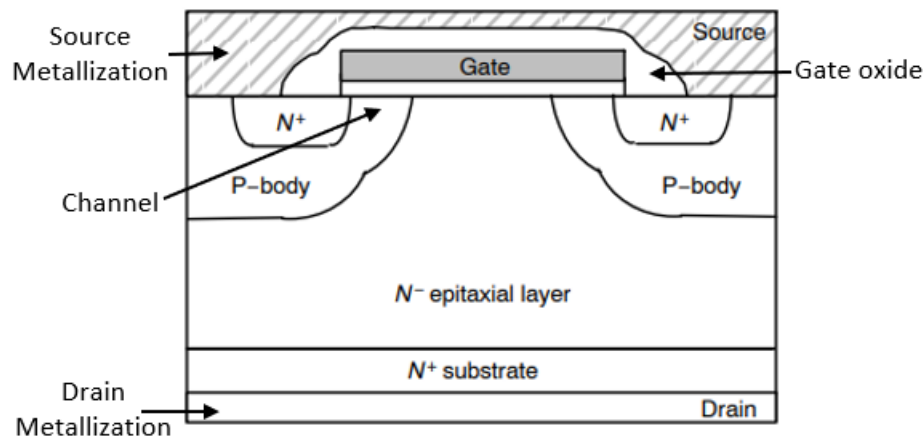


Figure 16: Schematic of n-substrate power MOSFET [33]

Due to its vertical design, the primary advantage of a VDMOS (Vertical Double-Diffused Metal-Oxide-Semiconductor) device lies in its capacity for extensive integration of numerous small symmetrical cells. These cells are interconnected parallel to the same surface source metallization and drain layer, directly linked to the device's substrate. In this configuration, the gate width becomes the critical factor determining the number of

cells that can be incorporated within a single VDMOS device. In a vertical structure, the VDMOS transistor's voltage rating is determined by the doping and thickness of the N^+ epitaxial layer, while its current rating is based on the channel width. This feature enables the VDMOS to support both high blocking voltage and high current in a compact silicon package, setting it apart from planar structure [34].

Power MOSFET characteristics:

The static behavior of the device is defined by the output characteristics which is shown in the Figure 17.

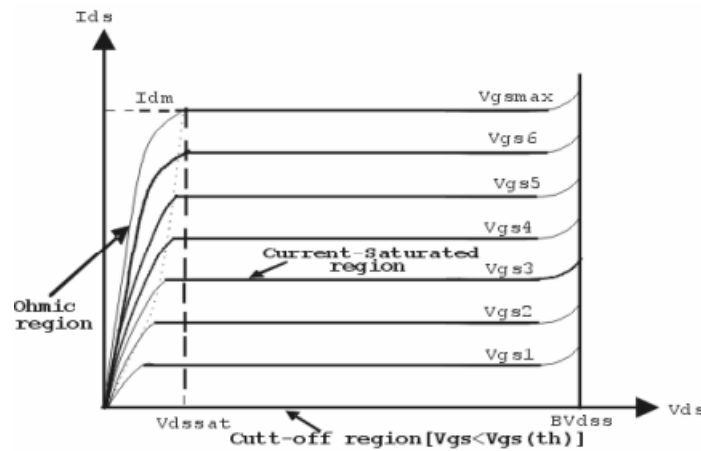


Figure 17: Output characteristics of N-channel MOSFET [35]

It has regions labeled as Cut-off, Ohmic, and Current saturated. In power electronics applications the normal functioning is ohmic. In the ohmic region, the device acts as a resistor with almost a constant on-resistance, ($R_{DS(on)}$) defined by V_{ds}/I_{ds} [35].

The MOSFET's dynamic behavior is highly dependent on the parasitic capacitances. In a power MOSFET, the gate is insulated by a thin silicon oxide [36]. Therefore, a power MOSFET has capacitances between the gate-to-source C_{gs} , gate-to-drain C_{gd} , and drain-to-source C_{ds} as shown in Figure 18. The capacitance C_{gs} and C_{gd} are determined by the capacitance of the gate oxide film and C_{ds} is the junction capacitance of the parasitic diode.

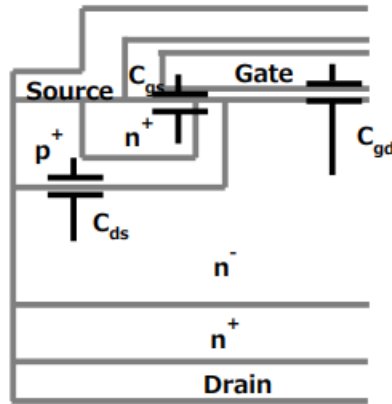


Figure 18: Location of intrinsic capacitances of a power MOSFET [37]

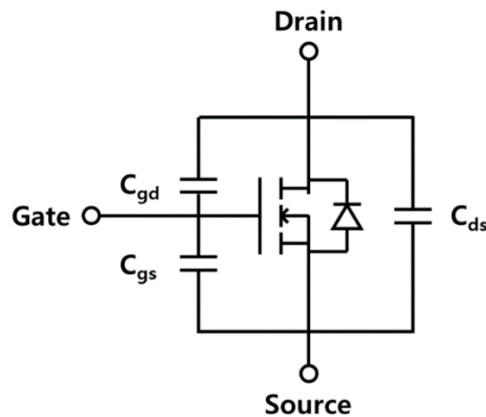


Figure 19: Power MOSFET equivalent circuit including parasitic capacitances [38]

Figure 19 presents the power MOSFET equivalent circuit including parasitic capacitances. Semiconductor capacitances typically depend on both voltage and the frequency at which capacitance is measured. Gate-to-drain capacitance, C_{gd} , exhibits non-linear behavior with voltage and holds paramount significance as it establishes a feedback loop between the circuit's output and input. It is often referred to as the Miller capacitance because it increases the total dynamic input capacitance, surpassing the sum of the static capacitances [36].

Typical values of input (C_{iss}), output (C_{oss}), and reverse transfer (C_{rss}) capacitances are provided in the datasheets and are used by circuit designers as a starting point in determining circuit component values. The datasheet capacitances are defined in terms of the equivalent circuit capacitances as presented in Eq. 1, Eq. 2, and Eq. 3:

$$C_{iss} = C_{gs} + C_{gd}, C_{ds} \text{ shorted} \quad \text{Eq. 1}$$

$$C_{rss} = C_{gd} \quad \text{Eq. 2}$$

$$C_{oss} = C_{ds} + C_{gd} \quad \text{Eq. 3}$$

C_{iss} is the input capacitance and is the capacitance as a whole, as seen from the input. To activate the MOSFET, this capacitance must be charged. It is important parameter to study the drivability of an input device or input losses [39].

C_{rss} is the gate-drain capacitance C_{gd} itself, and is called reverse transfer or feedback capacitance. If C_{rss} is large, the rise and fall in drain current is delayed even after the gate is turned on and off respectively. In other words, this parameter greatly affects switching speed.

C_{oss} is the output capacitance and is the total capacitance on the output side. If C_{oss} is large, a current arising due to C_{oss} flows at the output even when the gate is turned off, and time is required for the output to turn off completely [39].

1.3.3 Power IGBT

The Insulated-Gate Bipolar Transistor (IGBT) Blend the advantages of MOS gate with the high current-carrying capacity and low saturation voltage found in bipolar transistors, as depicted in Figure 20. They are preferred choice for high-current and high-voltage applications. The operation of IGBTs closely similar to that of MOSFETs. When a positive voltage is applied from the emitter to the gate terminals, it initiates an electron flow toward the gate within the body region. Suppose the gate-emitter voltage equals or exceeds the threshold voltage. In this case, electrons migrate toward the gate, forming a conductive channel across the body region. This enables the current flow from the collector to the emitter (electrons moving from the emitter to the collector). This electron flow also attracts holes or positive ions from the p-type substrate toward the drift region near the emitter [40].

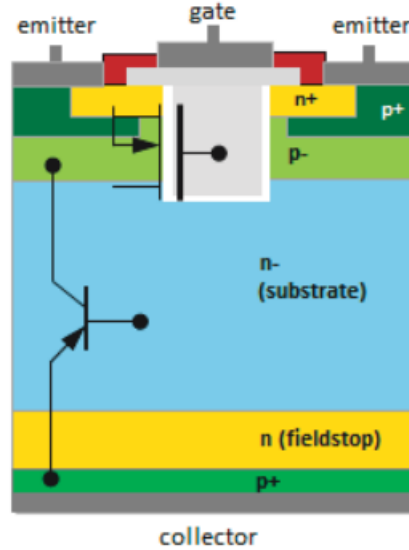


Figure 20: Cross section of a trench field-stop IGBT [40]

Figure 21 present the transfer characteristics of IGBT. To obtain the essential static characteristics of an IGBT, the gate-emitter voltage (V_{GE}) is adjusted while measuring the collector-emitter voltage (V_{CE}) and collector current (I_C). Subsequently, a graph representing the relationship between I_C and V_{CE} is constructed [40].

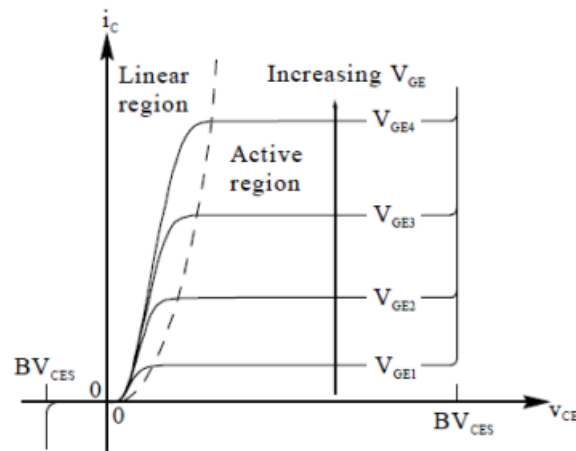


Figure 21: IGBT static characteristics [40]

The other important parameter is $V_{CE(sat)}$. It is the collector-to-emitter voltage drop during IGBT conduction, signifying power dissipation. It depends on collector current (I_C), gate-emitter voltage (V_{GE}), and junction temperature (T_J). The specified values for $V_{CE(sat)}$ are at rated I_C , V_{GE} of 15 V, and the three temperatures: 25°C, 125°C, and 175°C. IGBTs are

typically used as switches within the saturation region of V_{CE} . Raising V_{GE} enhances channel conductivity, lowering $V_{CE(sat)}$, while increasing I_C also elevates $V_{CE(sat)}$ [40].

The dynamic characteristics of IGBTs are impacted by parasitic capacitances. These capacitance values are typically determined under specific conditions: $V_{CE} = 25 \text{ V}$, $f = 1 \text{ MHz}$, and $V_{GE} = 0 \text{ V}$. The reduction in capacitance is inversely related to the voltage applied across the collector-to-emitter junction [40]. Figure 22 illustrates the IGBT section and equivalent model with parasitic capacitance between the terminals.

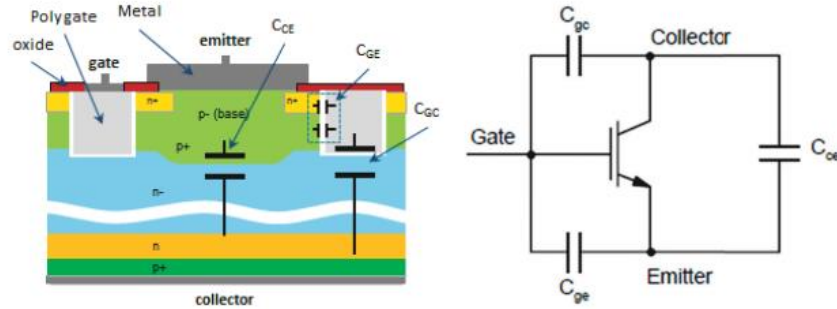


Figure 22: IGBT section and equivalent model with parasitic capacitances between terminals [40]

Eq. 4, Eq. 5, and Eq. 6 gives the typical input, reverse transfer, and output capacitances of IGBT.

$$C_{ies} = C_{ge} + C_{gc}, C_{ce} \text{ shorted} \quad \text{Eq. 4}$$

$$C_{res} = C_{gc} \quad \text{Eq. 5}$$

$$C_{oes} = C_{ce} + C_{gc} \quad \text{Eq. 6}$$

The input capacitance, known as C_{ies} , is measured between the gate and emitter terminals while the collector is shorted to the emitter, specifically for AC signals. C_{ies} is a combination of the gate-to-emitter capacitance (C_{ge}) and the gate-to-emitter capacitance (C_{gc}). Charging C_{ies} to the threshold voltage is necessary for the device to start turning on, and discharging it to the plateau voltage is essential for the device to begin turning off. Consequently, both the impedance of the drive circuitry and C_{ies} directly affect the turn-on and turn-off delays of the device [40].

The reverse capacitance (C_{res}), is measured between the collector and gate terminals with the emitter grounded. It is identical to the gate-to-collector capacitance and is commonly called the Miller capacitance. It is one of the significant factors in voltage rise and fall

times during switching, tends to decrease as the collector-to-emitter voltage increase, particularly in the case of the output and reverse transfer capacitances. This various is associated with gate charge data [40].

C_{oes} is the output capacitance, determined by measuring it between the collector and emitter terminals while shorting the gate to the emitter for AC voltages. C_{oes} combines the collector-to-emitter capacitance (C_{ce}) and the gate-to-collector (C_{gc}) in parallel. In soft switching applications, C_{oes} can have an impact on the circuit's resonance [40].

1.4 Aging mechanisms and failure modes in power electronics

The power electronic devices experience thermal, chemical, electrical, mechanical stresses, and degrade gradually, leading to a complete failure [41]. The familiar failure rate curve (bathtub curve), as illustrated in Figure 23, distinguish several cases between early failures, random failures (failures with constant failure rate), and failures resulting from wear-out and fatigue.

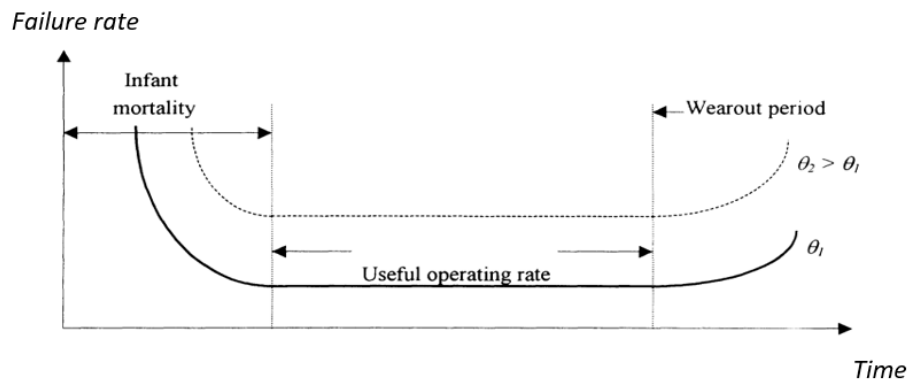


Figure 23: The “bathtub” failure curve of a large population of statistically identical items, for two ambient temperatures $\theta_2 > \theta_1$ for electronic components [42]

It is reliable to mitigate the early failures at the manufacturing level to be cost-effective [24]. During the infant mortality phase, the elevated failure rate is linked to significant inherent defects that promptly lead to part failures. Random (or sudden) failures are normally referred to the catastrophic failures as a result of component defects or overstress conditions. Their occurrences are mainly reduced by manufacturing and fabrication quality control, optimized design and de-rating operation [43]. Wear-out failures are attributed to the accumulation of incremental physical damage under the functional and environmental load (stress) conditions. If left untreated, the progressive degradation may

exceed a yield point to trigger an imminent overstress failure mechanism (i.e., fracture, melting or another thermal fault, etc.) [43].

Modern semiconductor designs, manufacturing processes, and process controls, there have been substantial advancements, leading to almost negligible failure rates in the early stages (infant mortality) and throughout the operational lifespan of semiconductor devices. Furthermore, when a device operates within specified limits, the wear-out phase of its performance curve has been significantly delayed, extending well beyond the typical useful life of most products [44]. Power semiconductor devices are central to power electronic systems and are crucial for reliability. As power electronic converters play a growing role in critical applications particularly in safety-sensitive human transport, attributes like reliability, lifespan, health monitoring, and predictive maintenance have gained greater importance [45].

1.4.1 Reliability challenges

Reliability is the ability of an item to work properly; it is its feature not to fail during its operation. It is today defined as the probability that an item will perform its required function under given conditions for a stated time interval. The component reliability involves the study of both reliability physics and reliability statistics. They have an important contribution to a better understanding of the ways in which the components fail, and how the failures are developing in time. This provides an invaluable background for understanding and assessing the real-world failure patterns of component reliability that come to us from field failure studies [42]. To fully understand the concept of reliability it is essential to clarify additional terms like failure and operating time. The failure is the termination of the ability of an item to perform a required function. The operating time is the period of time during which an item performs its required functions. For a non-repairable item, the operating time until the failure is named lifetime [42].

Power electronics enables efficient energy conversion and control through innovative solutions in components, circuitry, control methods, sensors, digital processors, and system integration. While efficiency goals for power electronic systems are within reach, increasing reliability requirements are creating new challenges due to the following factors [46]:

- Mission profiles critical applications (e.g., aerospace, military, more electrical aircrafts, railway tractions, medical electronics, etc.);
- Emerging applications under harsh environment and long operation hours (e.g., onshore and offshore wind turbines (WTs), photovoltaic (PV) systems, air conditioning, and pump systems);
- Cost constraints, reliability requirements and stricter safety standards, such as the demand for failure rates in the parts per million (ppm) range in future products;
- Ongoing need for higher power density in power converters and further integration of power electronics systems, which can lead to new failure mechanisms and thermal problems;
- Uncertainty of reliability performance for new materials and packaging technologies (e.g., SiC and GaN devices);

Figure 24 presents the evolution of reliability challenges from industry point of view.

	Yesterday	Today	Tomorrow
Customer expectations	<ul style="list-style-type: none"> - Replacement if failure - Years of warranty 	<ul style="list-style-type: none"> - Low risk of failure - Request for maintenance 	<ul style="list-style-type: none"> - Peace of mind - Predictive maintenance
Reliability target	<ul style="list-style-type: none"> - Affordable market returns (%) 	<ul style="list-style-type: none"> - Low market return rates 	<ul style="list-style-type: none"> - ppm market return rates
R&D approach	<ul style="list-style-type: none"> - Reliability test - Avoid catastrophes 	<ul style="list-style-type: none"> - Robustness tests - Improve weakest components 	<ul style="list-style-type: none"> - Design for reliability - Balance with field load / mission profile
R&D key tools	<ul style="list-style-type: none"> - Product operating and function tests 	<ul style="list-style-type: none"> - Testing at the limits 	<ul style="list-style-type: none"> - Understanding failure mechanisms, field load, root cause - Multi-domain simulation - ...

Figure 24: Reliability challenges in industry [46]

From this perspective, there are opportunities for power electronics to expand its role in efficient and reliable energy processing in various types of applications. Similarly, future research on power electronics reliability involves multidisciplinary knowledge as defined and presented in Figure 25:

- 1) analytical analysis to understand the nature of why and how power electronic products fail;
- 2) Design For Reliability (DFR) and robustness validation process to build reliability and sufficient robustness into power electronic products during each development process;

- 3) intelligent and control monitoring to ensure reliable field operation under specific mission profiles.

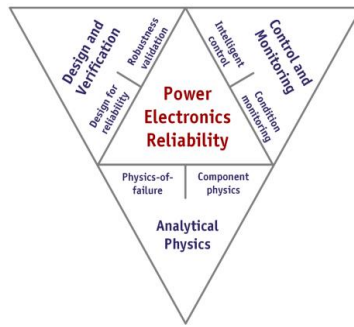


Figure 25: Power electronics reliability research needs seen from today [46]

1.4.2 Aging test

In the one hand, in many applications, there is a growing interest for power electronics which can operate at high temperature environment or high temperature cycling. In the other hand, the longevity of these have become an essential factor in the qualification of the component [45]. Aircraft applications pose a unique challenge, as the device and packaging may undergo severe temperature cycling, ranging from -55°C to 200°C , with a rate of approximately $\pm 10^{\circ}\text{C}$ per minute, mainly when converters are situated within the engine. This can influence the transmitted power and therefore, its ability to accomplish its mission. Moreover, these applications necessitate an operational duration of approximately 50,000 hours, which translates to 5,000 to 20,000 cycles. The realm of power electronics operating in high-temperature environments is particularly relevant to drilling and automotive applications [47]. Therefore, many industries adopt accelerated aging test to make reliability studies of the product before releasing it into the market. In order to accelerate this aging process accelerated aging tests are adopted.

The aging tests are set up in order to reproduce identified failure modes and mechanisms, as illustrated in [48]. Thus, probability of occurrence and critical combinations and cycles of stress are highlighted. This approach involves the implementation of accelerated aging tests, coupled with destructive and non-destructive methods [3], which will be detailed later in the following.

There exist different reliability testing methods, the major ones are addressed. In the case of encapsulated power semiconductors (power MOSFETs, diodes, Insulated Gate Bipolar

Transistors (IGBTs), etc.) the main stressors are maximum junction temperature, temperature swings during a single thermal cycling, blocking voltage, relative humidity, and gate voltage. Each of these stressors accelerate at least one of the failure modes [49]. The origin of temperature cycles is twofold: *passive temperature cycles* coming from the environment (climate) and *active temperature cycles* generated by power module operation. *Temperature cycling* and *power cycling* tests represent these conditions [50].

Temperature cycling: In Temperature Cycling Test (TCT), the temperature of a power module is changed by variation of the ambient temperature (TST: Thermal Shock Test) or the temperature of the case (TC: thermal Cycle Test) without electrical stressing. This test is applied mainly to evaluate the lifetime of the solder joints and to evaluate the resistance to the sudden changes in temperature the device can experience during storage or transportation [42], [50].

Power cycling: Active Power Cycling (APC) test is performed to assess the durability on the system receiving stress repetition effect and also to determine the resistance of a semiconductor device derived from chip ON/OFF switching. Thermal stress is repeatedly applied during self-heating and cooling operations at the time of ON and OFF. The PCT is representative to high temperature operating life [42], [49].

Accelerated aging tests are done according to the monitoring of an indicators. For example, on-state voltage-drop (V_{on}) at the applied heating current, Junction temperature (T_j), the thermal resistance between the junction and the baseplate (R_{TH}), and on state resistance ($R_{DS(on)}$), etc., for power cycling test.

The aging test process, experimental setup, and more information on this part will be detailed in chapter 4.

1.4.3 Failure mechanisms and failure modes in power electronics

To establish the failure modes and mechanisms, life test results and operation failures must be investigated through the characterization and classification of the failure mechanisms which occur either during the accelerated tests or in the field applications [42], [51]. This information will be useful for the establishment of the error and failure

sources. As far as power electronics' failure modes are concerned, the state of the art allows pointing out the main failure modes and mechanisms [45].

Previous studies have grouped failure mechanisms of power electronic devices into two categories, namely chip-related (or intrinsic) failures and package-related (extrinsic) failures. Intrinsic failure mechanisms are mostly related to electrical overstress i.e., high current and high voltage, while extrinsic failures are commonly induced by thermo-mechanical overstress. The primary cause of the failure is almost always (excepting the overvoltage) an abnormal increase of the temperatures, often spatially limited ("hot spot") and consecutive to an abnormal operation (second breakdown – avalanche operation – wrong base command). All these phenomenon produces:

- An abnormal operation of the component (electron – hole pairs formed by thermal agitation) that may lead later to a thermal turn-on.
- A variation of the physical properties of the component (solders – surface damages – local melting of the eutectic silicon/metal)

Sometimes, some abnormal stresses, even limited and occurring once, lead to a progressive degradation (in normal operating conditions), going up to the failure of the component. This progressive degradation occurs after some minutes or even thousands of hours after the initial accident [42].

As technology advancements continue to mature, addressing issues within the manufacturer's production processes, intrinsic failures are reduced. Consequently, emphasizing the growing importance of extrinsic failures in ensuring device reliability [42]. A power module when exposed to severe temperature cycles of different origins, experience different failure mechanisms. The typical degradation mechanisms caused by these are given in Figure 26. The main cause of failures is different heating of the individual area/layers and the different thermal expansion coefficients of the materials used in the inside of the power module. The typical wear-out mechanisms are as follows [50]:

- Bond wire lift-off
- Delamination of the upper side copper layer
- Solder cracks between the base-plate and DBC

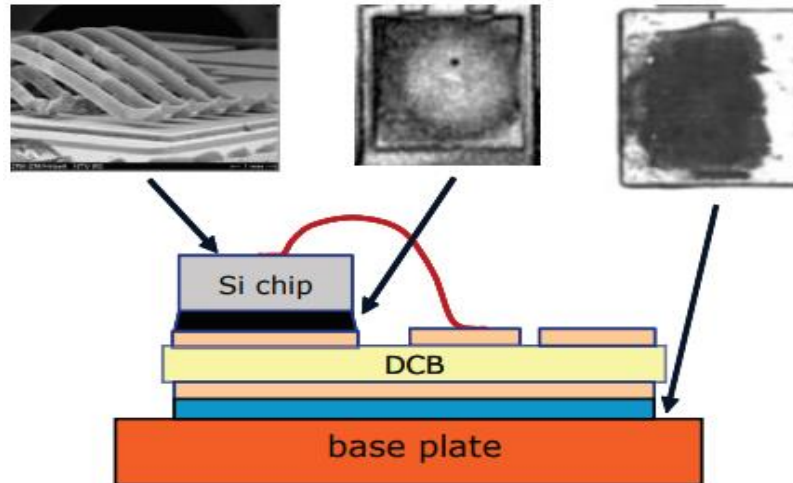


Figure 26: Wear out mechanisms of standard technologies [50]

Wire bonding failure modes, are known as the main defects. Wire bond failures primarily result from fatigue, either due to shear stresses at the bond pad-wire interface or from repeated wire convolution. The failure modes differ depending on the stress level that the devices are encountered with.

Bond wire failures can be further classified into two types: (1) bond wire heel cracking (2) bond wire lift-off.

Bond wire heel cracking: Wire bond heel (Figure 27) cracking occurs when the wire breaks above the bonded region due to fatigue from the repeated expansion and contraction of the wire loop during temperature cycling. This failure mechanism is primarily attributed to thermo-mechanical effects [45].

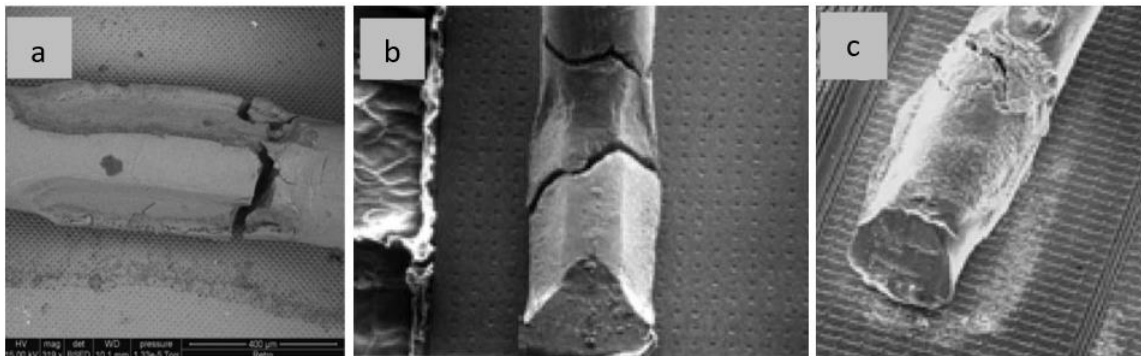


Figure 27: Bond wire (a) Heel crack (b) Heel crack due to low-cycle fatigue stressing (c) Heel crack due to improper bond wire coating [45], [51]

Bond wire lift-off: In power modules, one of the most common failure modes during active cycling is bond wire lift-off. The main reason for bond wire lift-off is the mismatch of a coefficient of thermal expansion (CTE) between Si and Al interfaces. The bond wire has a high coefficient of thermal expansion (CTE) compared to the other components of the power module shown in Table 4. The significant difference in CTE between aluminum (23-24 ppm/k) and silicon (2.6 ppm/k) results in thermomechanical stress at the bonding wire / chip interface. The primary malfunction in bond wires begins with cracks at the point of contact with the metallization shown in Figure 28 (a), which when progressed leads to the bond wire lift-off shown in Figure 28 (b). This chain reaction causes an increase in current density in nearby wires, leading to localized temperature rises due to surface irregularities on the chip. Over time, these factors contribute to the gradual failure of all interconnect wires [45], [51].

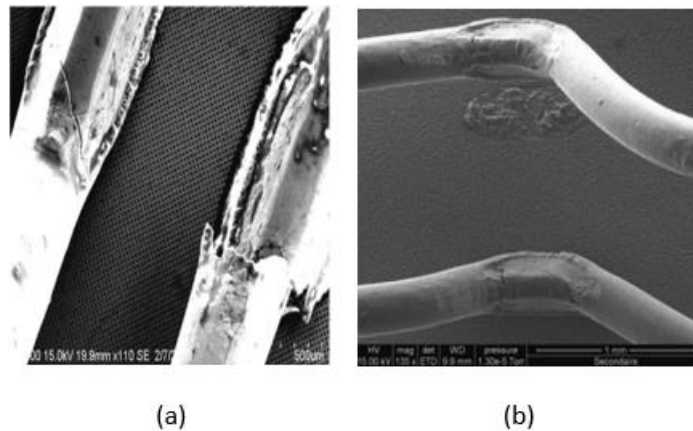


Figure 28: (a) Bond wire fracture (b) Bond wire lift-off [45]

	Material	CTE (ppm/K)
Chip	Silicium	2,6
Ceramic	AlN	3,1
	Al2O3	5,5
Baseplate	Cu	16
	AlSiC	6,5 - 12
Wire Bondings	Aluminium	23 - 24

Table 4: CTE values of power assembly material [42]

Delamination of the upper side of copper layer: This failure mode also results from the incompatibility of CTE between the different layers of power module. During the thermal

cycling, periodical compressive and tensile stresses are introduced in the thin metallization film by different CTEs of aluminum and of the silicon chip. Due to the large thermo-mechanical mismatch between both the materials and due to the stiffness of the silicon substrate, the stresses, which rises within the aluminum thin film during pulsed operation of the device can be far beyond the elastic limit. In such a scenario, the failure is observed in particular at the level of the thin copper metallization layer which leads to its deformation. Figure 29 presents the comparison of metallization before and after cycling.

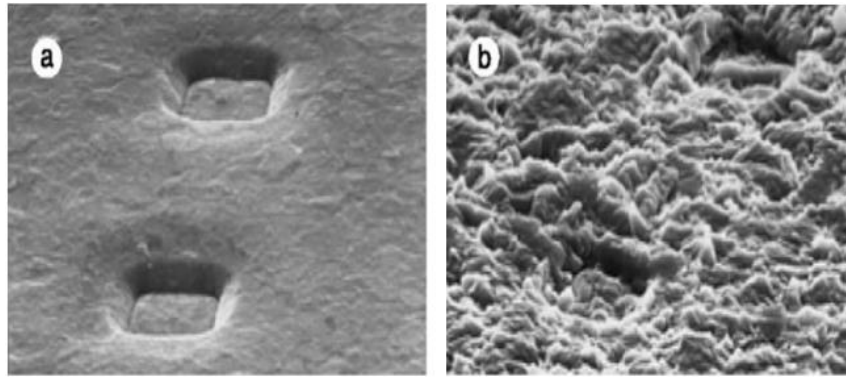


Figure 29: (a) Metallization before active cycling, (b) Reconstruction of metallization after cycling [45]

Soldering cracks: As far as the reliability of the electronic packages and modules are concerned, their weakest links are usually the solder interconnections such as mechanical shocks, temperature changes caused by device on/off operation, and ambient temperature variations, just a few to mention. The impact of these issues can be made smaller by taking them into consideration in the design aspect [52].

A power module is a multi-layer structure (silicon, copper, ceramic, etc.), each material has its own coefficient of thermal expansion. As seen in Figure 26, there are two solder layers in a typical power module, i.e., one between the Si device and DBC and another between the substrate and the baseplate. A larger CTE mismatch is between the substrate and baseplate which makes it more susceptible to solder fatigue [41]. This incompatibility of the CTE requires that the solder be compliant to avoid stresses at the level of the silicon components. Degradation of the solder anywhere increases the thermal resistance between the silicon component and the heat sink. Indeed, it results in the change of temperature cycle during the operation producing the shear strains and eventually produces cracks due to fatigue, which reduces the critical capacity for heat transfer [52].

1.5 Failure mode characterization

There are different inspection methods to characterize failure modes. *Shear strength testing* (MIL-STD-883, method 2019) and *pull testing* methods which are based on the application of force on to the die. These tests can also recover the force required to induce failure. Both of these tests are destructive and hence are only used for initial evaluation of materials and final sampling. The other testing methods X-ray, Scanning Acoustic Microscopy (SAM), Infrared Thermography (IRT), and visual inspection testing can be performed if 100% non-destructive screening is required.

1.5.1 Destructive testing methods

Destructive testing: This test destroys or changes the testing device in some way such that even if it passes the test, it is no longer fit for the service. For example: shear strength testing, pull testing, etc.,

Shear strength testing: this test can be performed to determine the strength of a die and bond wires referred as die shear strength and bond shear testing, respectively. This aim of these tests is to determine the strength of the component under test. In this test, a chisel-shaped shear tool is used [53]. Figure 30 presents the shear strength test on ball bond, wedge bond wire, and die shear.

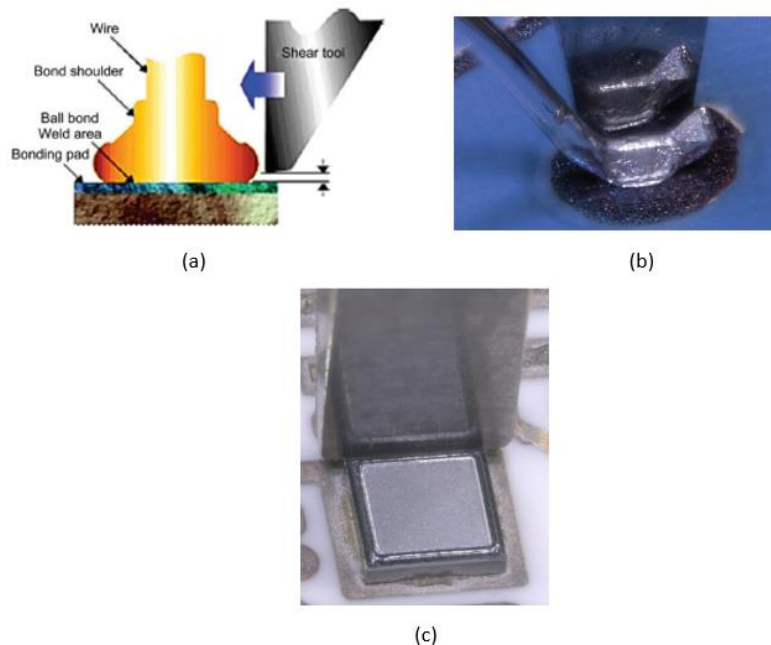


Figure 30: Shear strength test (a) ball bond [54] (b) wedge bond [54] (c) die [53]

For the bond wire shear test, the tool is placed parallel to the bond foot on the pad and a horizontal force is applied. The force required to shear the bond from the pad is measured and recorded together with the failure mode (first bond lift, pad lift, cratering).

Die shear test (Figure 30 (c)) evaluates the die attach process quality using a shear tool to apply uniform force alongside the die's edge. This force is applied perpendicularly to the die edge and parallel to the substrate plane, and required force to shear the die from the substrate is measured. Typical die shear failures include die interface break, fracture, and substrate interface break [53].

Pull testing: wire or bond pull test is one of several available tests used to assess the strength and quality of bond wires. In the wire pull test, an upward force is applied on the bond wires, drawing the wire away from the substrate or die using the hook, as illustrated in Figure 31. This process continues until there is a bond failure or the wire breaks. The test can be conducted on various bonds, including wire-to-die, wire-to-substrate, and wire-to-package lead bonds within the wire-connected devices, which are bonded using soldering, thermo-compression, ultrasonic, or relayed techniques [55].

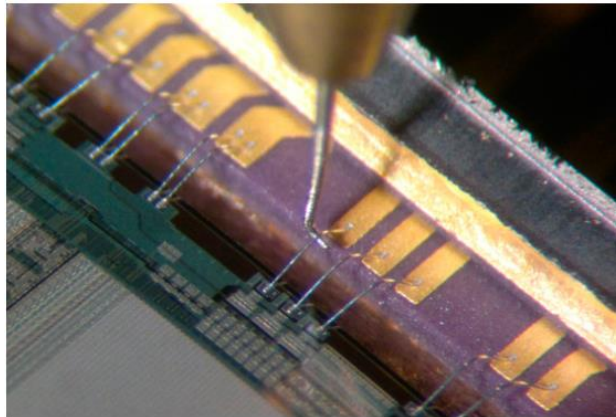


Figure 31: Wire bond strength test (Bond pull test) [55]

1.5.2 *Non-Destructive testing (NDT) methods*

Non-destructive testing: This test does not destroy or change the device under test such that it is still fit for service if it passes the test.

This is the reason why it is interesting and is adapted by many industrial applications. This section briefs about the non-destructive testing, most used methods in NDT.

Usually, the reliability studies are done prior to market product availability. Nevertheless, during its operating, it is relevant to monitor sensitive parameters in order to establish lifetime prediction. For that purpose, it could be interesting to use Non-Destructive Test (NDT) for online health monitoring [56].

Non-Destructive Testing (NDT) consists a range of non-invasive inspection techniques employed to assess material properties, components, or entire process unit. The techniques can also be utilized to detect, characterize, or measure the presence of damage mechanisms (for example corrosion or cracks). NDT, known as Non-Destructive Examination (NDE), Non-Destructive Evaluation (NDE), and Non-Destructive Inspection (NDI), involves techniques to locate and characterize defects in components, including size, shape, and orientation. The goal is to inspect equipment safely, reliably, and cost-effectively without causing damage or halting operations.

NDT can be conducted during or after manufacturing and even on equipment in service. While in operation, NDT inspections help evaluate the current equipment condition, track damage mechanisms, and inform decisions regarding remaining equipment life [56], which is the scope our study.

NDT employs multiple techniques for collecting diverse data types, each demanding specific tools, training, and preparation. Some techniques enable full volumetric inspections, while others are limited to surface inspections. Additionally, the effectiveness of certain NDT methods depends on the material type, with some techniques, like Magnetic Particle NDT, restricted to specific materials that can be magnetized [57].

In the following, the most commonly used NDT methods are described briefly. These methods include X-ray, Scanning Acoustic Microscopy (SAM), Infrared Thermography (IRT), and visual inspection. These are often employed methods in reliability studies of power electronic components and devices. They are used for fault detection, failure analysis, quality control, and performance assessment studies [58].

X-ray: When an X-ray is emitted from a source and directed towards a receiver, X-ray photons interact with the specimen. Some X-ray photons are observed by the specimen. The extent of X-ray absorption is contingent on the material's elemental composition and the specimen's geometries. Consequently, the presence of defects leads to variations in

the absorbed or transmitted X-ray energy detected by the receiver. These properties allow X-ray to measure and inspect the density and shape of various objects [57]. Figure 32 presents the detection of cracks in solder interconnects (with size of less than $10\ \mu\text{m}$) using improved X-ray methods.

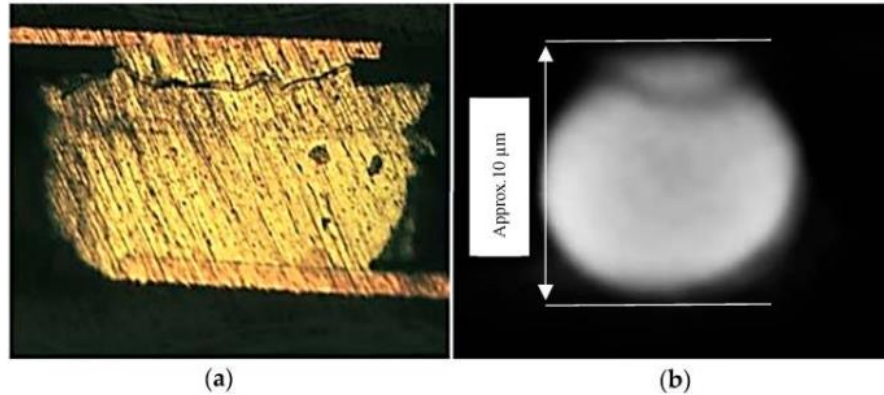


Figure 32: Crack detection in a micro solder bump: (a) metallographic microscopic image, (b) slice-by-slice inspection of μCT images [58]

Enhanced X-ray inspection methods show promise in assessing micro bump soldering and component alignments in packaging, even for parts under $10\ \mu\text{m}$. However, challenges remain, particularly in achieving sub-micron defect detection to resolution limitations. Additionally, extended data acquisition and processing times (several hours) and radiation concerns are drawbacks associated with current X-ray methods [58].

Scanning Acoustic Microscopy (SAM): the SAM method employs acoustic waves to generate visual images that depict variations in the mechanical properties of samples. The main part of the acoustic microscope is the probe or transducer (usually a piezoelectric or loudspeaker depending on the applications), which converts electrical signals into acoustic signals. The acoustic waves are focused and transmitted to the sample through a coolant (normally water). When the generated waves interact with the sample, a portion of the waves reflects back to the transducer while the rest is transmitted. Subsurface imaging is also possible due to the fact that acoustic waves can penetrate opaque solids. As a result of the interaction of sound with samples. SAM can accurately determine properties such as thickness, stiffness, density, shape roughness, and attenuation.

The utilization of SAM method for failure analysis of the surface and internal microstructure of solid or IC packaging goes back more than two decades. Figure 33

provides schematic illustration of SAM method for inspection of IC packaging and the actual SAM setup available in TNO Eindhoven (The Netherlands) [59].

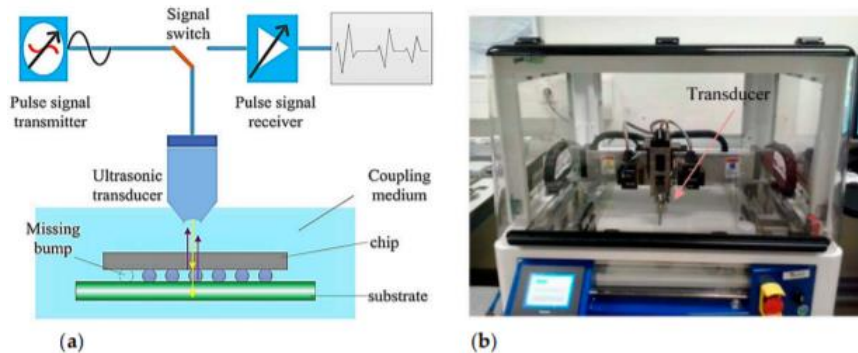


Figure 33: SAM method for inspection of IC packaging (a) schematic diagram of SAM method, (b) SAM inspection setup [59]

SAM method can detect flaws (Figure 34) such as solder bump defects, laminar cracks (with sizes less than $50\ \mu\text{m}$ and frequency range of 100-150 MHz), void defects (as small as $125\ \mu\text{m}$ in diameter).

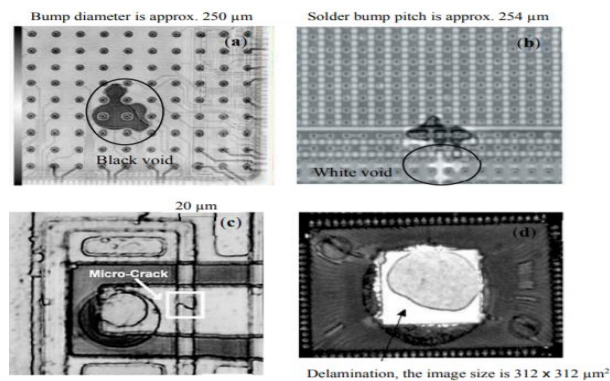


Figure 34: Various types of defects detected by SAM: (a) Black void below under fill level, (b) White void above under fill, (c) Micro-crack at wafer level, and (d) Delamination between the die top and the encapsulates [59]

Scanning Acoustic Microscopy (SAM) is an effective method for assessing layer thickness, delamination, underfill delamination, and void defects within the materials. However, it cannot detect defects at packaging edges due to the “edge effect.” SAM requires a coupling medium (typically deionized water) for acoustic energy transmission and has sub-micron resolution limitations. Resolution can be enhanced by using higher GHz frequencies, but this reduces penetration depth, leading to a trade-off between resolution and depth [59].

Figure 35 presents the detection of crack formations following the thermal cycling using SAM. The crack has mainly propagated in the ceramic-metallization interface during the first 300 cycles. The solder joints are represented as circle in the image.

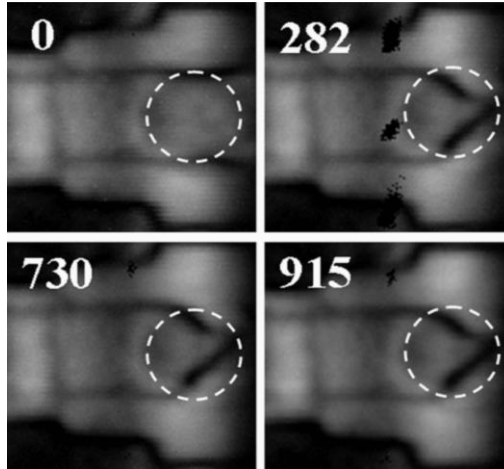


Figure 35: SAM image of crack propagation in solder joints for different thermal cycles [52]

Infrared Thermography (IRT): infrared thermography (IRT) stands as one of the prevalent NDT methods for material assessment. The fundamental principle of the IRT method involves capturing the heat radiated from a surface within the electromagnetic spectrum's infrared (IR) wavelength range (2 -14 μm). It records the surface's temperature distribution, with temperature resolution varying 0.020 $^{\circ}\text{C}$ to 0.075 $^{\circ}\text{C}$, depending on the type of IR detector. IR detectors function in various infrared bands, with the middle wave (2–5 μm) and the long wave (8–12 μm) being the most common. The application of thermography for IC packaging inspection has a history goes back to more than half a century. IRT is used to inspect flip chips, solder joint defects, edge defects, misalignment of solder bumps, presence and location of micro solder bumps (as small as approximately 100 μm in diameter and 250 μm in pitch), silicon crack, under fill void, delamination defects with minimum size about 2 μm , and subsurface defects (up to 4 mm in depth). Figure 36 present the defect detection using IRT method [59].

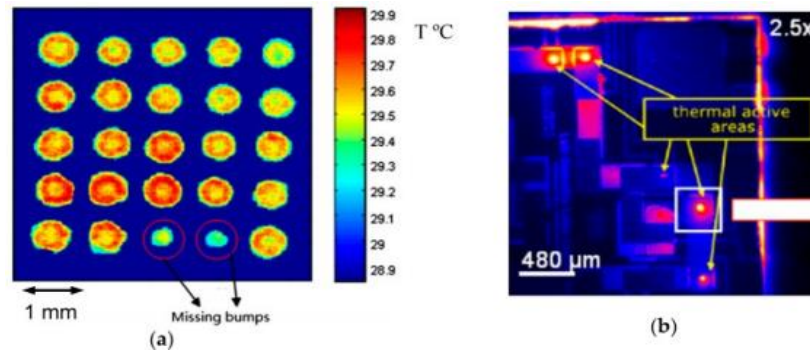


Figure 36: Defect detection using infrared thermography method: (a) missing bumps with lower temperature and (b) failed device emitting increased heating [59]

Though this method proved its place in NDT applications, there are still challenges: It primarily detects surface or near-surface defects due to limited heating penetration depth. Spatial resolution is constrained by camera pixel resolution and infrared wavelength. Active methods may risk damaging the specimen due to heat propagation [58].

Surface Acoustic Waves (SAW): Surface Acoustic Waves (SAWs) are waves travelling along a material's surface, with their amplitude decreasing as they penetrate deeper. SAWs can be generated and measured using contact transducers (like piezoelectric materials), contact actuators with non-contact sensors, or fully non-contact systems like laser-based or air-coupled transducers. One approach involves using a pulsed laser to induce heat, generating ultrasound waves in electronic packages. A laser Doppler vibrometer measures the resulting displacement response. This method helps to identify defects like missing solder bumps by analyzing response variations across the specimen surface.

SAW is effective at detecting voids and cracks with a lateral spatial resolution of around 100 μm . However, it cannot access areas like underfill and regions with bump pitches smaller than 100 μm . A limitation is the relatively long inspection time required.

There exists several other techniques not used for power electronics [56].

Online health monitoring has become a crucial tool for real-time device state-of-health (SOH) assessment to enhance reliability and prevent catastrophic failures. Tracking electrical parameters is crucial for identifying device degradation or early faults. Since monitoring all electrical parameters is impractical in power converters, specific ones

should be selected based on the dominant aging mechanisms. In recent years, considerable research has been devoted to identifying aging indicators in Si devices. The gradual change in the ON-state resistance ($R_{ds(on)}$) of MOSFETs and the saturation voltage of IGBTs are commonly used indicators of aging. In contrast, there is limited research of failure indicators in SiC MOSFETs. The primary reliability concerns for SiC MOSFETs are gate oxide degradation and bias-temperature instability. As a result, most SiC MOSFET reliability studies concentrate on identifying the indicators related to gate oxide issues, with the threshold voltage (V_{th}) being the most commonly used indicator for monitoring gate oxide charge trapping. Eventually, the degradation of SiC MOSFET packaging is evaluated through accelerated high-temperature power cycling tests, revealing an increasing trend in ON-state resistance during the aging process. Additionally, the voltage drop across the body diode (V_{SD}) and thermal impedance are recognized as indicators for packaging-related degradations [60]. Each new technology raises the problem of finding good monitoring parameter for a specific failure mode.

In addition to these traditional NDT methods, the research interest in power electronics is now more attracted towards the wide frequency band characterizations connecting the NDT techniques. This thesis is more dedicated to this approach while adopting some of the above discussed NDT methods. Each NDT method has its own particular advantages, disadvantages and applications. A suitable selection among all the NDT methods for a specific case is up to the users. Some aspects (i.e., types of damage to be monitored, detection reliability, cost, portability, equipment setup, scanning time, and safety concerns) must be well understood.

Many studies have proposed different NDT methods but radio frequency (RF) based NDT techniques are not well covered while they are receiving extensive attention in recent years. The frequency of interest is in the range of around 3 kHz to 300 GHz which occupies the lower range of the whole electromagnetic (EM) spectrum. The instrumentation becomes complicated when the inspection frequency goes above 300 GHz [61]. However, the frequency range is limited or adapted following the equipment limitations and application requirement. Based on the detection mechanism, the RF NDT methods can be classified into four groups:

Electromagnetic induction methods: the induction methods are primarily based on the Faraday's principle of electromagnetic induction. Commonly used electromagnetic induction method is Eddy Current Technique (ECT), this method is widely used for the detection of corrosion and cracks, and measurement of thickness and conductivity for metals. The other type of technique is the microwave open-ended waveguide imaging, the microwave frequency extends from 300 MHz to 300 GHz with the corresponding wavelength from 1 m to 1 mm, respectively. In this test, the electromagnetic wave radiates from an open-ended waveguide or horn antenna to the specimen under test. This technique reveals the information of the cracks or dents on the surface by the attenuation/phase images of the reflection coefficient (S_{11}), which can be acquired from Vector Network Analyzer (VNA) [61].

Resonance methods: the resonance methods mainly transform the defect information into the variation of the resonance frequency in the resonant circuit. A typical type of resonance method is near field scanning microwave microscopy (NSMM), which is generally composed of a resonant cavity and a sharp tip [61].

RF-based thermography: one of the efficient RF-based thermography techniques is Pulsed Eddy Current (PEC) thermography (Figure 37). It was developed for damage detection, which is fast and efficient method. This technique works on the phenomenon that any change in the microstructure of the composites could locally change the electrical conductivity of the medium. Thus, by applying electrical potential difference, the temperature of the medium rises due to joule effect. Changes in the induced current flows would be revealed by an infrared (IR) camera. The pulsed excitation provides a low frequency spectrum, which subsequently offers a greater penetration depth than the eddy current technique (ECT) [61].

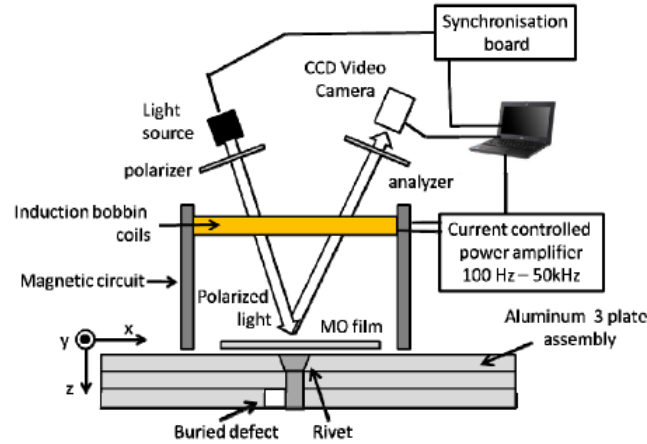


Figure 37: Basic principle of the pulsed eddy current imaging (PECI) device [62]

RF wave propagation method: the active Radio Frequency Identification Technology (RFID) with the capability of remote inspection and long-term structural health monitoring has also attracted extensive attention [63], [64]. Each RFID tag contains an integrated circuit (IC) chip (which is made up of the impedance matching network, energy harvesting system and microcontroller) and an antenna encapsulated together with the help of suitable packaging. The defect information is transferred from antenna to the detector by backscattering [61].

Following the state of the art, it is noticed that monitoring the state of the health of a package ask for prior knowledge about the package. Therefore, it becomes difficult to manage the state of the health of an unknown package. It is interesting to look for such kind of methods which monitor the state of the damage of package, whatever the die technology is and can detect any potential failures.

1.6 Conclusion

This chapter presents the packaging and assembly of discrete and power modules detailing the constituent elements. The reliability challenges following the evolution of power electronics technologies are pointed out. Concerning these challenges, there is a need for multidisciplinary knowledge, which is main interest of today's research. Eventually the problems related to packaging failures like bond wire related, solder fatigue related failures are described. Concerning the reliability studies, the research interest to combine

failure characterization techniques with the online monitoring of electrical parameters represent an effective way of detecting the potential failures.

This thesis focuses on the development of a non-destructive characterization methodology to detect the failure mechanisms of switch assemblies in power electronics. The method is based on the electromagnetic characterization over a wide frequency range. The characterization technique towards the NDT adds value to this method. A characterization technique, S – parameter also known as scattering parameter acquired from Vector Network Analyzer (VNA) is followed. The S – parameters represent the reflection and transmission waves following the power injection. As the simulations aids design for reliability (DFR), the characterization can help future monitoring. The working principles, experimental setups, characterizing process, etc., of these equipment's will be detailed in the coming chapters.

Chapter 2 :
Wide frequency band characterization and its
equivalent model construction

2.1 *Introduction*

Power electronics have recently experienced remarkable evolution in terms of Wide Band Gap (WBG) semiconductors and power electronics packaging techniques. Whereas these new trends in packaging also create new challenges in electrical and thermal characterization [65]. The chip package is an essential and integral part of any semiconductor product. It is a critical competitive factor, as it affects operating frequency, power, complexity, reliability, and cost. As a result, it is desirable to account for an equivalent electrical model, representing both the chip and the package behavior effects early in the design stage. Of primary interest are the bonding and the insulation which make each packaging process a unique problem [66]. One of the obstacles related to package characterization is usually due to the strong mechanical interface made by adhesive glue or epoxy matrices. On the one hand, internal on-chip package ports cannot be probed from the outside without partially destroying the sealing [67], [68]. On the other hand, electromagnetic simulations may be used to overcome this problem [69], [70]. Unfortunately, the electromagnetic simulations require detailed knowledge of the 3D package and bonding structure, the material parameters, and the grounding schema [66]. In this context, the research shows great interest in characterizing techniques more prone towards Non-Destructive Testing (NDT). This chapter provides the broadband characterization applied to different types of packages. It addresses different broadband characterization techniques while focusing more on the frequency domain characterization process.

The broadband characterization techniques are mainly addressed in two main domains: Time-domain network described in section 2.2 and Frequency-domain network described in section 2.3.

2.2 *Time-domain network*

The time-domain network involves the examination of mathematical functions or physical signals with respect to time. In the time domain, the value of a signal or function is defined across all real numbers in continuous time or at distinct discrete moments in discrete time. A time-domain plot illustrates the evolution of a signal over time [71]. The Time-Domain Network Analyzer (TDNA) is used to measure the time-domain networks. The operation

of the TDNA is based on the well-known echo principle [72]. The general working principle of the TDNAs is as follows: the generator injects a pulse or step-like signal E_i in the Device Under Test (DUT) as shown in Figure 38. Some of the injected power is reflected at the discontinuities of the Device Under Test (DUT). The incident (E_i) and the reflected (E_r) voltage waves compose the Time-Domain Reflection (TDR) signal. The signal that propagates through the DUT is measured as the transmitted signal (E_t). The voltage wave in transmission is named the Time-Domain Transmission (TDT) signal. The TDR/T-signals are measured with a broadband digital oscilloscope [72].

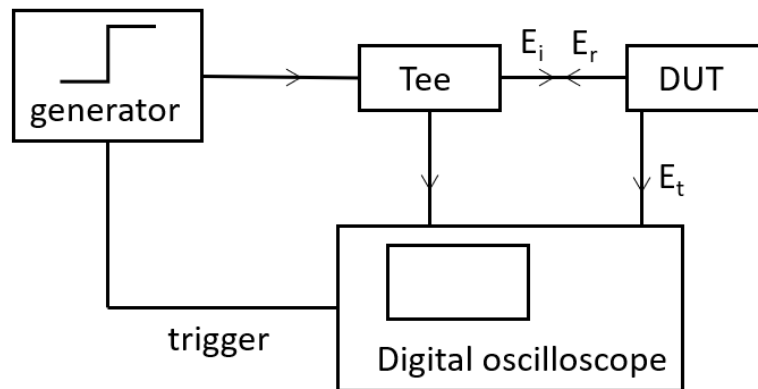


Figure 38: Time-Domain Reflectometry (TDR) and Transmission (TDT) set-up [72]

The TDR/T-measurement technique has been originally developed for the localization of defaults in cables [72]. The TDR/T-technique has diverse applications, including interconnection modeling, dielectric material measurements, and interconnection and package-related applications [73].

Reflectometry is a non-destructive technique for analyzing physical systems, highlighted for its application in Spread Spectrum Time-Domain Reflectometry (SSTDR) for live electrical system monitoring. This includes various domains like airplane cabling, power systems, and battery health. The study [74] presents SSTDRs principles, challenges such as detecting minor and intermittent faults, and potential advancements including its application in medical imaging and the improvement of signal processing through machine learning. Further exploration into SSTDR circuitry customization for specific applications suggests a future of enhanced diagnostic capabilities. [75] evaluates SSTDR and Sequence Time-Domain Reflectometry (STDR) for cable fault localization, particularly in AC and digital signal transmission, underscoring SSTDR's superior

performance in high-noise environments and with digital signals, including those meeting the Mil-std 1553 standard. This study emphasizes the critical role of these methodologies in ensuring safety by early fault detection, including open and short circuits. It supports the careful optimization of test signals to minimize interference and accurately detect impedance changes. This approach facilitates the development of preventative maintenance strategies, potentially preventing system failures.

On the other hand, [76] [77] study focused on diagnosing and monitoring the health of Insulated Gate Bipolar Transistor (IGBT) modules following the SSTDR technique. [76] focused on using SSTDR to detect bond-wire lift-offs in IGBTs, a common aging-related issue that significantly affects the performance and reliability of these devices. The study outlines the experimental setup and methodology, where SSTDR signals are applied to IGBT modules subjected to accelerated aging processes to simulate bond-wire lift-off. The results showcase the capability of SSTDR to identify minute changes in the electrical characteristics of the IGBT modules, indicative of the early stages of bond-wire lift-off.

[77] addresses reflectometry, which is not detailed but presumably includes techniques like SSTDR for active power cycling and condition monitoring of IGBT modules. This approach suggests a proactive strategy in managing the lifecycle and reliability of IGBT modules by detecting defects such as bond-wire lift-off and assessing the modules' overall condition through active power cycling. This method likely involves the application of stress through controlled power cycles to evaluate the robustness and aging status of the IGBTs, combined with reflectometry to monitor changes in their electrical characteristics that could indicate impending failures.

Eventually, [78] [79] conducted their study on condition monitoring of power electronics. [78] presents a new method for online condition monitoring of IGBTs and IGBT modules using SSTDR. This technique aims to detect bond wire lift-offs and estimate the state of health of IGBT power modules. The research focuses on the gate terminals of the IGBT device rather than the collector side. It proposes a novel RL-equivalent circuit to represent the bond wires for simulation and measurement of reflection amplitudes. The RL-equivalent of the bond wires in the IGBT module is detailed, and simulation results using CST Studio Suite are presented, showing a correlation between the simulated and

experimental data. The study demonstrates the effectiveness of SSTDR-based condition monitoring, independent of current levels and locations, providing valuable insights for future researchers in the field and contributing to improving the reliability of power electronic semiconductors and converters. The experimental results further validate the capability of SSTDR in detecting bond wire liftoffs and estimating the state of health of IGBT power modules.

[79] presents a preliminary experimental study on the condition monitoring of power modules using S-parameters, time-domain reflectometry (TDR), and time-domain transmission (TDT) measurements. The study aims to demonstrate the viability of using these techniques to monitor the degradation of a power module. The research was conducted on a standard high-current power module, artificially aged by cutting wire bonds one by one. The study reveals that it is feasible to use these techniques, mainly scattering parameters, to continuously track the simulated wear and tear of the power module.

However, the intricate architecture of the power module (PM), coupled with a design unsuitable for RF applications, results in the measurement data exhibiting complex and somewhat unpredictable patterns. These complexities hinder the straightforward physical interpretation of the data.

Despite these challenges, the observed alterations in RF behavior serve as indicators of the PM's deterioration, especially significant for S-parameters within the 200 MHz to 1 GHz range. Monitoring various components of the scattering matrix, both in reflection and transmission, makes it possible to pinpoint the deterioration's location and characteristics.

Though these techniques are widely used in various applications, including RF, there are some limitations which need to be considered when applying these techniques in RF contexts. Some of these limitations are mentioned in the following

- Frequency dependency: TDR measurements, conducted at a fixed frequency, may inadequately represent the behavior of RF systems that function over a spectrum of frequencies. This discrepancy can lead to incomplete assessments of broadband quality and impedance variations at different frequencies.

- Discontinuity detection: Reflectometry techniques excel in identifying discontinuities, such as open or short circuit, on transmission lines. However, in scenarios with multiple discontinuities, the accuracy of Standing Wave Ratio (SWR) measurements in isolating these faults can be compromised.
- Complex structures: TDR relies on a simple transmission line model. For intricate RF architectures, like multi-layer PCBs, inter-layer reflections can interact, leading to ambiguous results.
- Signal-to-Noise Ratio (SNR): TDR measurements are challenged by low signal-to-noise ratio due to the wideband receiver design. In RF environment, where detecting small impedance changes or discontinuities is crucial, noise interference can mask the signal, compromising the accuracy of measurements.

In addition to these, propagation effects where dispersion, skin effect, and dielectric losses are neglected by TDR techniques. In RF applications, these effects become significant, affecting the accuracy of measurements.

2.3 *Frequency-domain network*

The frequency domain involves analyzing mathematical functions or signals in terms of frequency rather than time. To put in simple terms, a frequency-domain graph shows how much of the signal lies within each given frequency band over a range of frequencies [80]. The two basic measuring instruments that exist for signal characterization of gigabit interconnects following frequency domain are: Impedance analyzer and Vector Network Analyzer (VNA).

2.3.1 *Impedance Analyzer*

Impedance analyzer or *LCR* (inductance-capacitance-resistance) *analyzer* is used for the measurement of an impedance. The instrument applies a time-harmonic voltage to the DUT's access port and measures the current's amplitude and phase in that port. BY dividing the voltage by the current, the input impedance at the port is calculated. To reduce inaccuracies, four-terminal measurements are performed with 4 shielded needles and the SOL (short, open, and load)- calibration compensates for the parasitic elements of the set-

up [72]. The one-port calibration, known as a Short/Open/Load (SOL) calibration, effectively eliminates source matching, directivity, and frequency response errors [81].

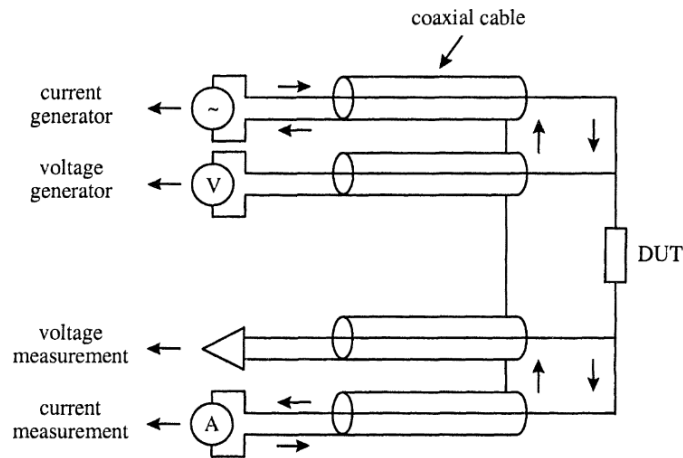


Figure 39: Schematic set-up for a four-terminal pair impedance measurement [72]

Figure 39 presents schematic set-up for a four-terminal pair impedance measurement. By using independent signal current paths and voltage sensing cables, the effect of the measurement wire impedance is reduced. Following the measurement of the input impedance at the package leads or interconnection line in out, it becomes feasible to establish a straightforward circuit model utilizing lumped elements such as resistors, capacitors, and inductors. This model can then be utilized in a circuit simulator like SPICE. One of the major limitations of this measuring technique is that, the lumped element model is only valid for frequencies for which the length of the leads or interconnection lines is small with respect to the wavelength (λ) of the time-harmonic signals propagating on the leads or lines ($\lambda = \frac{v}{f}$, where v = propagation speed, f = frequency). Therefore, this measurement can introduce non negligible uncertainties when the device under test (DUT) violates limiting conditions. These uncertainties arise due to frequency range restrictions and signal propagation effects, especially in the context of packages, connectors, and interconnects, where accounting for transmission line effects is essential to maintain accurate signal integrity and minimize losses. Additionally, in NDT applications, precise material characterization necessitates the measurement of properties like dielectric constant and loss tangent, which can vary with frequency. Accounting wavelength effects becomes crucial to ensure reliable results.

This thesis took the opportunity to compute the dielectric constant using the capacitance measurement from the Impedance analyzer (E4990A from Keysight's Technologies). The operating frequency of this impedance analyzer range from 20 Hz to 120 MHz. The dielectric constant, a fundamental parameter of insulating or dielectric materials, is calculated from the capacitance value when the material is used as a dielectric. There are three measurement methods (Appendix 4-1), Contacting Electrode method (Rigid Metal electrode), Contacting Electrode method (Thin film contact) shown in Figure 40, and non-Contacting method (Air Gap method) to obtain the dielectric constant and dissipation factor. Each method follows a typical measurement procedure, assumptions, and experimental requirements which are detailed in [82]. The contacting method (Thin film contact) is adapted to test the epoxy dielectric material. The method is chosen based on the testing device material, and dimensions.

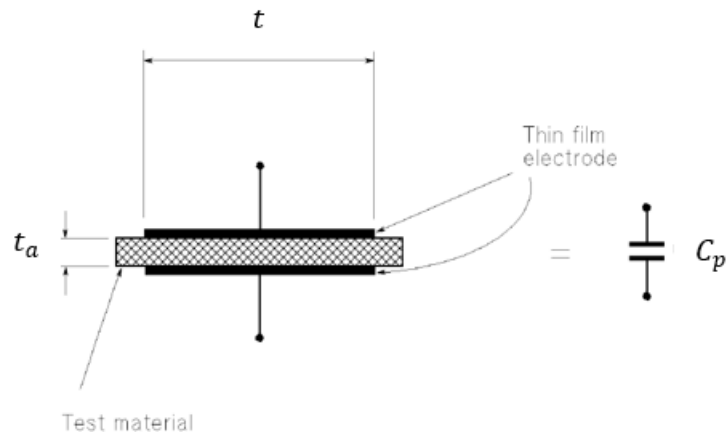


Figure 40: Contacting Electrode method (Thin film Electrode) [82]

The dielectric constant and dissipation factor of a test material can be obtained using the following equations [82].

Parameters needed:

C_p Equivalent parallel capacitance [F]

D Dissipation factor

t_a Average thickness of test material [m]

A Area of Guarded thin film electrode [m²]

d Diameter of Guarded thin film electrode [m]

ϵ_0 Vacuum permittivity = 8.854×10^{-12} [F/m]

Equations:

$$\epsilon_r = \frac{t_a * C_p}{A * \epsilon_0} \quad \text{Eq. 7}$$

Eq. 7 can be updated to Eq. 8 for DUT in cylindrical shape

$$\epsilon_r = \frac{t_a * C_p}{\pi * \left(\frac{d}{2}\right)^2 * \epsilon_0} \quad \text{Eq. 8}$$

$$\tan(\delta) = D \quad \text{Eq. 9}$$

Where,

ϵ_r *Dielectric constant of test material*

$\tan(\delta)$ *Dissipation factor of test material*

The dielectric fixtures (16451B) provide two applicable electrodes, Electrode-C (electrode for large thin film electrodes) and Electrode-D (electrode for small thin film electrodes). The electrode is chosen following the test material dimensions and the test requirements (Appendix 4-2).

2.3.1.1 Characterization of epoxy substrate

A cylindrical epoxy tablet (Figure 41) of diameter 15.8 mm and dielectric thickness of 1.47 mm is considered as test material. This is an epoxy based dielectric material which is quite used during the thesis and will be detailed in coming chapters. For instance, it will be used in every specific interface. A part of this dielectric material (epoxy) in cylindrical shape is considered to compute the dielectric constant and dissipation factor. The diameter and thickness of copper layer are 14.2 mm and 35 μm , respectively.

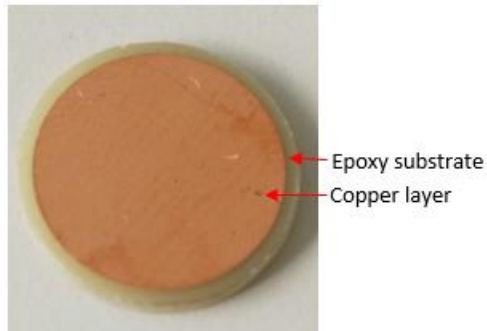


Figure 41: Cylindrical epoxy substrate

Characterization process:

- The SOL calibration is performed
- The test material is set between the electrodes (Appendix 4-3)
- The capacitance (C_p) and the dissipation factor (D) are measured

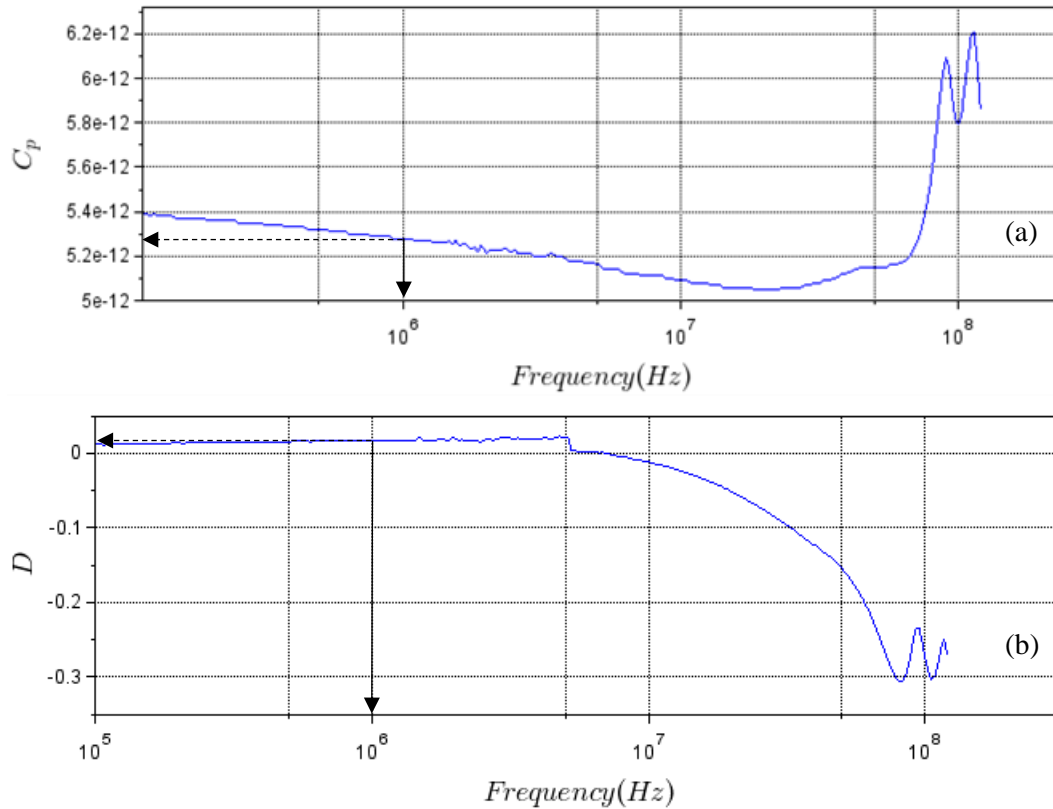


Figure 42: (a) Parallel capacitance (C_p) and (b) Dissipation factor (D) measurements from impedance analyzer

By taking the measurement data from Figure 42 and following the equations (Eq. 7, Eq. 8, and Eq. 9), the dielectric constant and the dissipation factor of the test material are calculated.

A material's relative permittivity is not constant but varies with frequency. At extreme low frequencies near DC, conductivity plays a significant role in the material's behavior. Conversely, different electromagnetic effects come into play at very high frequencies (GHz and above). Using a 1 MHz frequency range strikes a balance, as it is in a range where extreme effects are less pronounced, making it a practical choice for a wide range of real-world applications. Also, 1 MHz has gradually become a standard reference frequency for indicating relative permittivity in numerous data sheets and specifications.

Therefore, the capacitance of 5.28 pF and dissipation factor of 0.0169 are recovered at 1 MHz from Figure 42 (a) and (b), respectively. Having dielectric thickness of 1.47 mm, copper diameter of 15 mm and substituting these values into Eq. 8 and Eq. 9 gives relative permittivity and dissipation factor of 4.959 and 0.0169 respectively. The obtained values for relative permittivity and dissipation factor are under the range of standard values of 3.5 to 4.8 (at 1 MHz) and 0.01 to 0.03 (at 1 MHz), respectively. The achieved $\tan(\delta)$ and ϵ_r values are confirmed from Figure 43 (a) and Figure 43 (b) respectively.

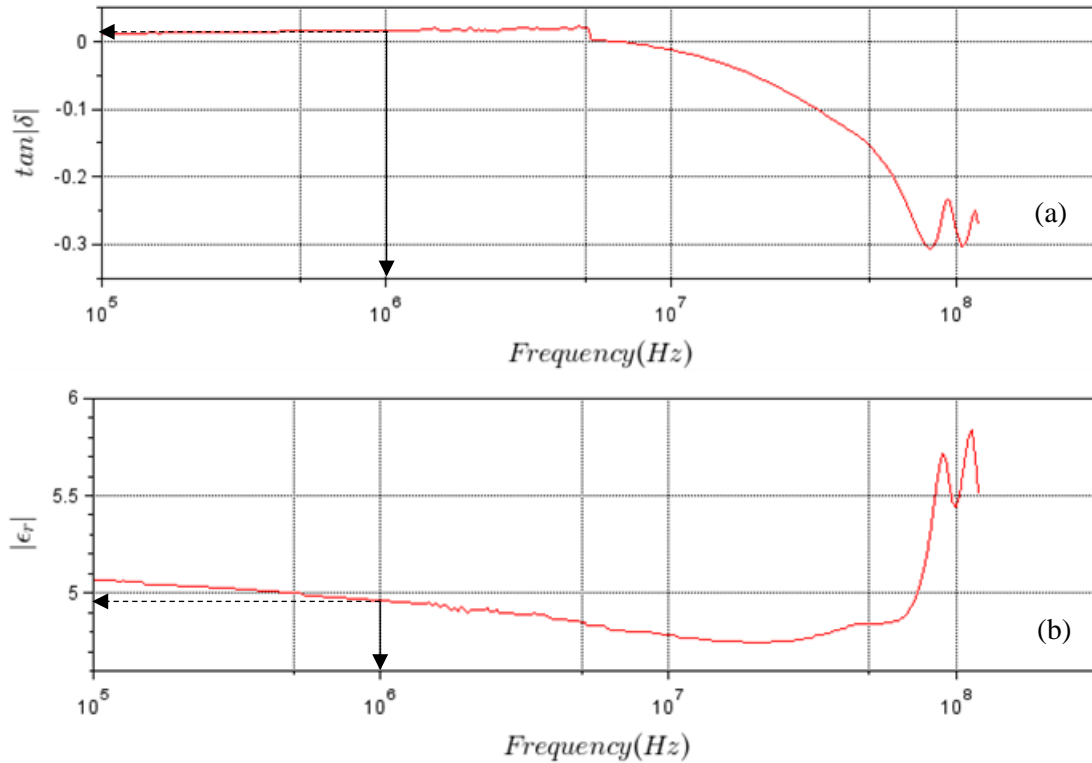


Figure 43: (a) Relative permittivity (b) dissipation factor as a function of frequency

2.3.2 Vector Network Analyzer (VNA)

Vector Network Analyzers (VNAs) are test instruments that measure electrical network parameters. They are essential for radio frequency (RF) and microwave component analysis of various passive and active devices including filters, antennas, and power amplifiers [83]. They are mostly used for the high frequency applications ranging from 1 Hz to 1.5 THz. Special types of network analyzers can also cover low frequency ranges down to 1 Hz [84]. Scattering parameters (detailed in section 2.4) are typically measured with a vector network analyzer [72].

VNA has several ports, commonly 2, to connect the DUT. Each VNA port include both signal source and receiver. The receivers detect changes to the output signal from a device (or network) and compares that to the source signal input into that device. To assess the device's effect on the current and voltage, a VNA measures both the amplitude and phase responses of the scattering parameters caused by the device [83].

In order to understand fully how a vector network analyzer operates to generate the scattering parameters, it is useful to see a basic block diagram (Figure 44) of the test instrument.

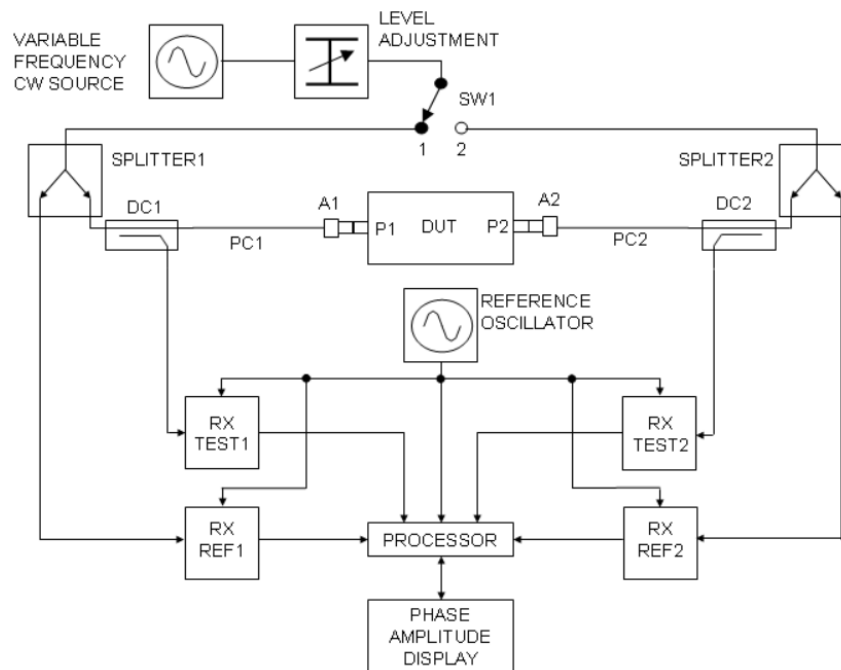


Figure 44: Block diagram of an RF Vector Network Analyzer (VNA) [84]

The Figure 44 shows the essential parts of a typical 2-ports vector network analyzer. The two ports of the DUT are denoted port 1 (P1) and port 2 (P2). PC1 and PC2 are the precision cables which are extended and connected to P1 and P2 using suitable connector adaptors A1 and A2 respectively. The test frequency is generated by a variable frequency Carrier Wave (CW) source and its power level is set using a variable attenuator. The position of the switch SW1 activates the source connection to the selected port and therefore, sets the direction that the test signal passes through the DUT. Initially consider that SW1 is at position1 so that the test signal is incident on the DUT at P1 which is appropriate for measuring S_{11} and S_{21} . The test signal is fed by SW1 to the common splitter

1 whose one arm (the reference channel) feeding a reference receiver for P1 (RX REF1) and the other (the test channel) connecting to P1 via the directional coupler DC1, PC1, and A1. The third port of the DC1 couples off the power reflected from P1 via A1 and PC1, then feeding it to the test receiver 1 (RX TEST1). Similarly, signals leaving P2 (from P1 through DUT) pass via A2, PC2 and DC2 to RX TEST2. RX REF1, RX TEST, RX REF2, RX TEST2 are known as coherent receivers as they share the same reference oscillator, and they are capable of measuring the test signal's amplitude and phase at the test frequency. All of the complex receiver output signals are fed to a processor which does the mathematical processing and displays the chosen parameters and format on the phase and amplitude display. When SW1 is set to position 2, the test signals are applied to P2, the reference is measured by RX REF2, reflections from P2 are coupled off by DC2 and measured by RX TEST2 and the signals leaving P1 (from P2 through DUT) are coupled off by DC1 and measured by RX TEST1. This position is appropriate for measuring S_{22} and S_{12} [84].

Several key specifications must be considered when determining the need for a VNA. The top four specifications that can guide the selection process are frequency range, dynamic range, trace noise, and measurement speed [85].

The frequency range selection is typically determined by the instrument's specific application requirements or constraints related to its operating frequency. Nevertheless, it is advisable to take into account both immediate requirements and potential future needs when making this choice.

The dynamic range represents the measurable attenuation span from maximum to minimum within a specific frequency range. To achieve the desired performance of the DUT, it is essential to ensure that the DUT's maximum attenuation specifications are at least three to six dB lower than the VNA's dynamic range specification. Most modern VNAs provide an excellent dynamic range, typically around 120 dB, which is generally suitable for various applications [85].

Trace noise quantifies how much a VNA introduces random noise into measurements. This noise is commonly expressed in milli-dB (0.001 dB) units [86]. Consequently, trace noise can play a significant role in assessing the precision of specific components.

Another vital specification is measurement speed, which signifies the time needed to carry out a single sweep or measurement. Minimizing test at very high volume is critical to the success of the component measurement. Nevertheless, in numerous research and low-volume applications, the measurement speed of the VNA is typically sufficient [85].

Calibration and error corrections:

Although a factory calibration can be beneficial for confirming the accuracy of specific aspects of a VNA, like the stimulus power and receiver frequency response, other characteristics related to the measurement setup, such as cable length, cannot be accurately addressed through factory calibration. Consequently, user calibration becomes a critical step, addressing variables due to measurement configurations and compensating for instrument variations across temperature and frequency [87]. Therefore, before making any measurements with the VNA, it must be calibrated to reduce the systematic errors affecting the measurements [88]. An understanding of measurement error is helpful before proceeding to calibrate a VNA because not all errors can be minimized this way [85].

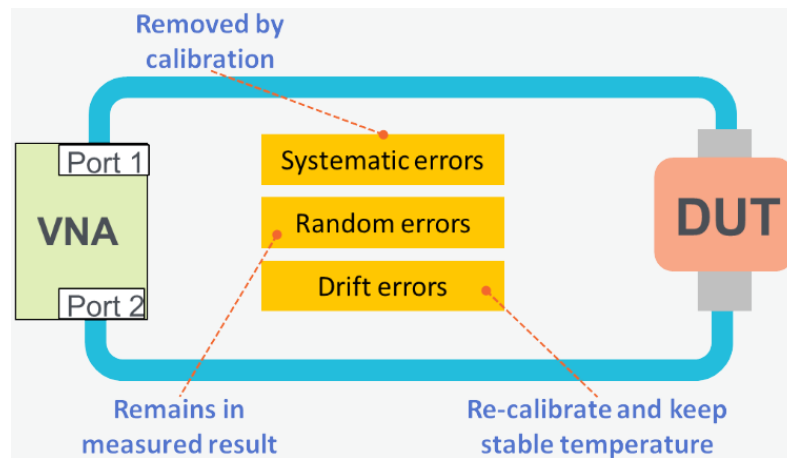


Figure 45: Type of VNA measurement errors [85]

There are three main types of measurement error (Figure 45). The measurement error types include systematic, random, and drift errors. Systematic errors are imperfections in the test equipment or setup and are typically predictable [14]. A vector network analyzer attains exceptional measurement precision by rectifying systematic errors inherent in the instrument and the properties of cables, adaptors, and test fixtures. This corrective procedure, often called calibration, is distinct from other processes and may be conducted

multiple times within an hour. At times, it is referred to as user calibration to distinguish it from periodic calibrations carried out by manufacturers or third parties [85].

The second source of measurement error is caused by random error. This error arises from fluctuating noise generated by the test equipment or setup over time. Notably, this error persists in the measured outcomes even after user calibration. It plays a pivotal role in defining the achievable measurement accuracy. As previously mentioned, trace noise is a prime illustration of random errors [85].

A third error category is drift error, which pertains to the gradual changes in measurements over time. These fluctuations manifest in both the test equipment and the test setup after a user calibration has been executed. This can include temperature shifts, humidity variations, and mechanical movement within the test setup. Employing controlled environments, such as temperature and humidity-regulated rooms, helps mitigate drift errors. The extent to which the test setup undergoes drift over time dictates the frequency at which recalibrations are required [85].

Among RF and microwave test equipment, VNAs have a unique calibration technique. While they are equipped with a factor calibration feature like any other RF and microwave test equipment, VNAs offer an additional user calibration option that users can execute before conducting measurements. The unique advantage of VNAs lies in their integrated stimulus and receivers within a single instrument, facilitating this “user calibration. As previously mentioned, VNAs measure both magnitude and phase, enabling the user calibration to perform vector error correction. This capability sets VNAs apart as one of the most precise RF instruments. User calibration empowers VNAs to account for the impact of cables, adapters, and various accessories used in correcting the DUT. By eliminating the influence of these accessories, user calibration enables the VNA to achieve precise measurements of the DUT’s performance in isolation [85].

There are wide range of methods to calibrate a VNA, depending on the number of ports, the frequency range, the available calibration standards, and even the port type of the DUT. The port type of the VNA can be coaxial, on wafer, in fixture, or waveguide. Furthermore, different types of VNA calibration also involve a trade-off between precision and speed. In the case of a two-port VNA designed for full S-parameters

measurements, distinct calibration methods are applied based on the specific measurement needs. The three most commonly used calibration types are presented in Figure 46.

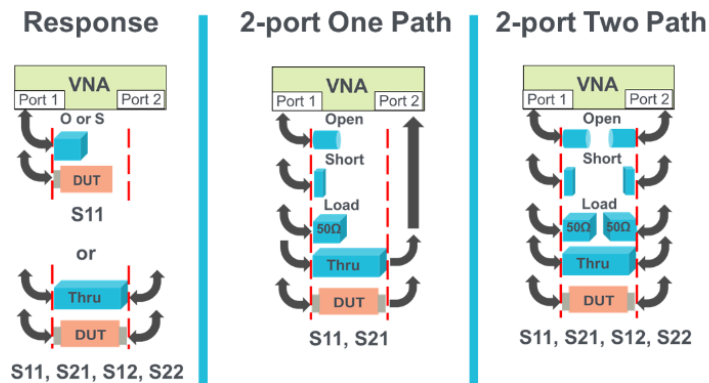


Figure 46: VNA calibration methods [85]

Frequency response calibration: It is the simplest of all calibration types, primarily addressing the instrument's frequency response. Typically, it is used when a basic understanding of the linear performance of a DUT is adequate [87]. For example, if only S_{11} or S_{22} measurement is needed, an open or short standards can be employed to measure the test setup response. Likewise, for S_{12} or S_{21} measurement only a through (thru) standard can be performed [85].

Two-port one path calibration: This method is accurate and works well when interested in measurement of limited set of S-parameters (e.g., S_{11} and S_{21} for $a_2 = 0$). In this case, the VNA exclusively transmit from port 1 [85] presuming that port 2 is optimally matched and enabling reasonably accurate S_{11} and S_{21} measurements [87].

Two-port two path calibration: This is the most common and complete calibration approach for a two-port VNA, often called full two-port or S-parameters calibration. This method is highly accurate and all four S-parameters are fully corrected using various calibration techniques. In coaxial systems, the widely employed calibration technique is SOLT (Short, Open, Load, and Through) which uses the 12-term error model [88]. SOLT is the simplest method, which requires access to known standards with a short circuit and open circuit, a precision load (usually 50 ohms), and a through connection [84]. However, this method requires an 8-step procedure to get both ports calibrated [88]. This thesis employed a 2-port VNA (E5061B from Keysight's Technologies) for characterizations. The calibration process and the operation of this VNA are detailed in section 2.5.

2.3.3 *Comparison between impedance analyzer and vector network analyzer*

A VNA is capable of measuring a wider array of parameters, including S-parameters whereas impedance analyzers are primarily geared toward impedance measurements. Nevertheless, it is worth noting that measurements obtained with both instruments can be transformed from one format to another. However, when undertaking such conversions, it is vital to take into account any particular requirements or specifications that may apply [72].

A notable difference between a VNA and an impedance analyzer is their handling of reference impedance. VNAs commonly employ a fixed reference impedance, often set at 50 ohms, which allows for easy matching with transmission lines. This setup facilitates the use of cables and Printed Circuit Board (PCB) fixtures with matched lines, thereby reducing the impact of parasitic inductance and capacitance, especially at higher frequencies. In contrast, an impedance analyzer can dynamically adjust its reference impedance to suit specific measurement requirements, thereby improving measurement accuracy. Nevertheless, utilizing cables and fixtures in this manner introduces additional parasitic elements into the system [72].

Furthermore, it is essential to emphasize that an impedance analyzer is typically designed as a one-port device, restricted to measuring the input impedance at the single port of multi-port devices. In contrast, a VNA can measure both reflection and transmission between ports.

SOL calibration is commonly employed to address linear systematic errors introduced in the setup of an impedance analyzer. Conversely, VNAs offer more advanced error correction techniques [72]. Consequently, both instruments hold significance, particularly in distinct frequency ranges. VNAs excel in high frequency applications, whereas impedance analyzers are better suited for low-frequency applications. Typically, impedance analyzers find utility in the DC to 10s of MHz range, while VNAs prove valuable in the MHz to 10s of GHz range.

2.3.4 Comparison between Time-domain and Frequency-domain network

Although both techniques are complementary and even in principle, equivalent- scattering parameters and TDR/T-data can be converted into each other through the use of Fourier Transform which has both advantages and drawbacks.

TDR/T-measurements use a step-like or pulse-like signal with a broadband frequency spectrum, due to which the measurements are very sensitive to the noise in the broad spectrum of the time-domain signal. Also, the dynamic range of TDNA is limited. On the other hand, frequency-domain measurements are small-banded and hence less sensitive to noise which provides a technique with a large dynamic range (~ 120 dB). The bandwidth is variable. They are preferable if the resonant circuits must be characterized. Therefore, they are suitable to characterize analogue systems. The TDR and TDT techniques are mainly used to study the reflection and transmission properties of linear stationary circuits. However, non-linear and/or non-stationary circuits may also be characterized with the TDNA [72]. In general, a VNA measures and displays data in the frequency domain. One example is scattering coefficients of a component versus frequency. The S-parameters are coefficients of linear model and are ratio of absolute quantities where the stimulus frequency is the same as the response frequency. However, if a component exhibits nonlinear behavior, there may not be one-to-one relationship between the input and output frequencies [89]. The analyzers to model the nonlinear characteristics are quite available but are at high cost. The time-domain analysis and frequency-domain analysis are invaluable analysis tools. The use of either networks depends on individual design needs [90] .

Taking into account various considerations, this thesis opts for the characterization of S-parameters using a Vector Network Analyzer (VNA). VNAs have the advantage of operating across an extensive frequency spectrum, typically ranging from RF to microwave frequencies, rendering them well-suited for diverse applications, especially those involving high-frequency RF and microwave circuits. With their inherent two-port measurement capabilities, VNAs facilitate the concurrent measurement of both forward and reverse scattering parameters. This dual assessment of transmission and reflection coefficients is instrumental in understanding how power electronic components interact

with input and output signals, thus enabling the timely detection of potential failures through the analysis of reflection and transmission waves. Furthermore, VNAs offer advanced calibration techniques that ensure precise measurements by mitigating the influences of test fixtures and cables. In contrast, in this context, impedance and time-domain network analyzers exhibit reduced versatility. Consequently, the chosen approach aligns with the thesis objectives, presenting a well-suited technique for characterizing the system under study.

2.4 S-parameters (Scattering parameter) characterization

Any linear network can be described using S-parameters and Y-parameters (Admittance parameters), Z-parameters (Impedance parameters), T-parameters (Scattering transfer parameters), H-parameters (Hybrid parameters), and ABCD-parameters (Cascade or transmission parameters). Each of these has its specific advantages and disadvantages. In comparison, S-parameters are more familiar as they are easier to measure and calculate on a network analyzer. Additionally, S-parameters do not use open or short circuit conditions to characterize a linear network. Instead, matched loads are used [91]. All the other parameters relate their measurements to total voltages and currents at each port. However, this becomes a challenge at higher frequencies as the equipment cannot measure total voltages and currents. Also, active devices become unstable when terminating by a short or open circuit. Therefore, it is more suitable to use traveling waves instead of total voltages and currents. Hence S-parameters are a preferred method of characterizing a device at RF and microwave frequencies as they are expressed in terms of reflected and transmitted waves with respect to the incident wave.

This section focuses more on answering three questions: what are scattering parameters? Why are they used? And how are they used?

S-parameters describe the electrical behavior of linear electrical networks when undergoing various steady-state stimuli by electrical signals [91]. They represent the linear characteristics of radio frequency electronic circuits and components. To understand how to use a VNA to characterize a DUT, it is essential to understand the basics of S-parameters [85].

S-parameters provide a relationship between the incident wave (denoted a_i , i being 1 or 2) and reflected (denoted b_i) and transmitted (denoted b_{i+1} or b_{i-1}) wave at each port over a range of frequencies. Both a and b waves are phasors, having both magnitude and phase at the specified terminals of the network port [85]. For a 2-ports device, a four-element matrix of S-parameters data represents the bidirectional behavior of the network as a function of frequency [92], as shown in Figure 47. The S-parameters denoted S_{11} , S_{21} , S_{12} , and S_{22} are obtained through a relation between a_1 , a_2 , b_1 , and b_2 [93].

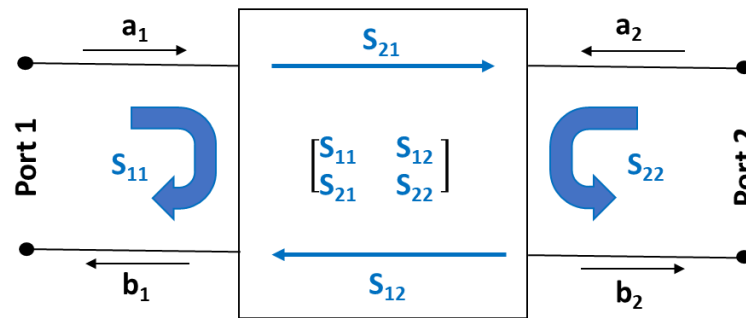


Figure 47: Two-ports S-parameters representation

S_{11} = Input reflection coefficient

S_{21} = Transmission from port 1 to port 2

S_{12} = Transmission from port 2 to port 1

S_{22} = Output reflection coefficient

In the S-parameters nomenclature, S_{yx} , the second number (x) represents the originating port, while the first number (y) is the destination port [85]. The common practice used to evaluate the behavior of a multi-port network is to use incident waves as excitations at each port and to measure the resulting exiting waves that are either reflected from the port where power is applied or transmitted through the DUT to the remaining port.

The S-parameters generation from VNA has been clearly explained in the Figure 44. Using this knowledge, the S-parameters theory can be more elaborated. Firstly, a portion of the stimulus signal is taken as a reference signal. S-parameters are defined as ratios of signals coming from various ports relative to this reference. The four-element matrix of S-parameters obtained from 2-port network as shown in Figure 47 is as follows:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad \text{Eq. 10}$$

$$b_1 = S_{11}a_1 + S_{12}a_2 \quad \text{Eq. 11}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \quad \text{Eq. 12}$$

Considering 2-ports network, the VNA measurements uses the two following cases to get four S-parameters (i.e., when the source is connected to port 1 and to the port 2) shown in Figure 44.

Case 1: Forward case, depicted in Figure 48.

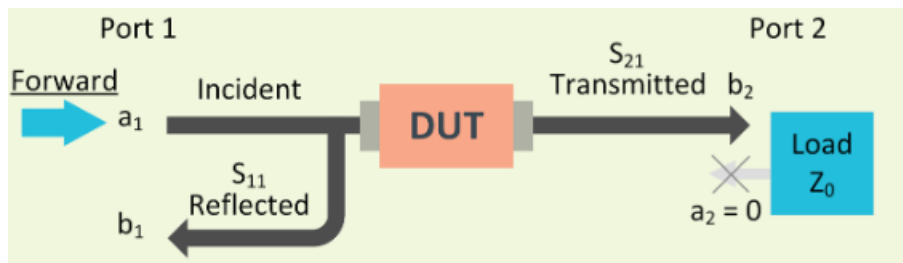


Figure 48: S_{11} and S_{21} measurement [85]

Port 1 is transmitting the a_1 signal (incident wave) and a matched load is applied to port 2, resulting in zero signal reflection at the load ($a_2 = 0$). Substituting the condition ($a_2 = 0$) in Eq. 11 and Eq. 12 provides S_{11} (Eq. 13) corresponds to the reflection coefficient at port 1 and S_{21} (Eq. 14) the forward transmission coefficient through the DUT.

$$S_{11} = \frac{b_1}{a_1} \Big|_{a_2=0} \quad \text{Eq. 13}$$

$$S_{21} = \frac{b_2}{a_1} \Big|_{a_2=0} \quad \text{Eq. 14}$$

Case 2: Reverse case is depicted in Figure 49.

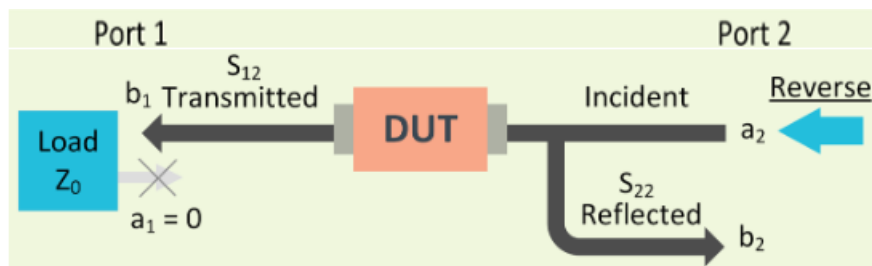


Figure 49: S_{12} and S_{22} measurements [85]

In the reverse case, port 2 is transmitting the a_2 signal and a matched load is applied at port 1 ($a_1 = 0$). Substituting the condition ($a_1 = 0$) in Eq. 11 and Eq. 12 provides S_{22} (Eq. 15) corresponds to the reflection coefficient at port 2 and S_{12} (Eq. 16) the reverse transmission coefficient through the DUT.

$$S_{22} = \frac{b_2}{a_2} \Big|_{a_1=0} \quad \text{Eq. 15}$$

$$S_{12} = \frac{b_1}{a_2} \Big|_{a_1=0} \quad \text{Eq. 16}$$

Finally, four S-parameters are obtained. The S-parameters can also be expressed in terms of voltage and current. Consider a 2-port network consisting of a single impedance Z connected in series (Figure 50).

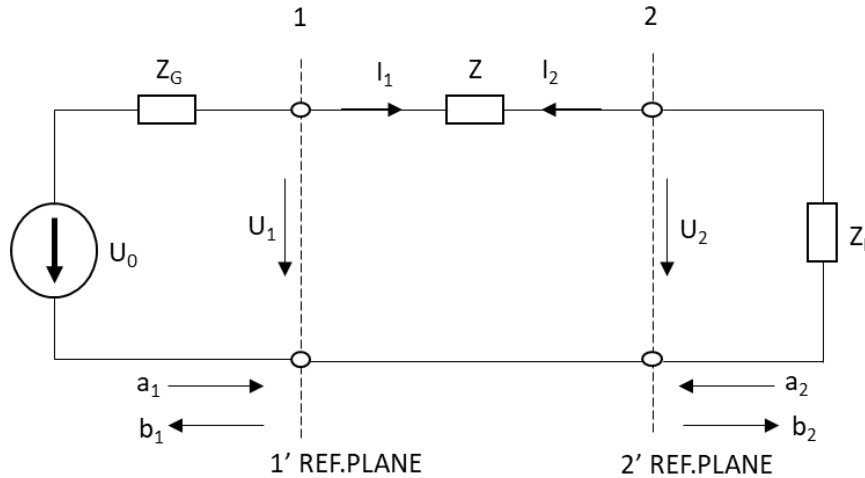


Figure 50: Example for a 2-port network: a series impedance Z [94]

The generator and the load impedances are denoted as Z_G and Z_L , respectively. In the case where, $Z = 0$ and $Z_L = Z_G$ (assuming real Z_G), a matched load is achieved, resulting in the maximum available power being delivered to the load, and $U_1 = U_2 = U_0/2$. It is important to note that all the voltages and currents are given as peak values. Now, U_0 , U_1 , and U_2 can be related to a and b power waves. The waves travelling towards port 1 and port 2 are a_1 and a_2 , respectively. The waves travelling away from the port 1 and port 2 are b_1 and b_2 , respectively. Likewise, for the n -ports the waves travelling towards and away from the port can be generalized as (a_1, a_2, \dots, a_n) and (b_1, b_2, \dots, b_n) , respectively. By definition, currents entering the n -port are considered positive, while currents leaving the

n-ports are considered negative. The wave a_1 , entering the n-port at port 1, is derived from the voltage wave entering a matched load. To maintain consistency with the conservation of energy, the voltage is normalized by $\sqrt{Z_0}$. Z_0 is typically an arbitrary reference impedance, but often used as the characteristic impedance of a line (e.g., $Z_0 = 50 \Omega$), and frequently, $Z_L = Z_G = Z_0$. The general definition of the waves a_i travelling into and b_i out of an n-port are provided in Eq. 17 and Eq. 18 [94].

$$a_i = \frac{U_i + I_i Z_0}{2\sqrt{Z_0}} \quad \text{Eq. 17}$$

$$b_i = \frac{U_i - I_i Z_0}{2\sqrt{Z_0}} \quad \text{Eq. 18}$$

Now, substituting Eq. 17 and Eq. 18 in equations from Eq. 13 to Eq. 16, gives the S-parameters in terms of voltage and current waves.

$$S_{11} = \frac{b_1}{a_1} = \frac{U_1 - I_1 Z_0}{U_1 + I_1 Z_0} \quad \text{Eq. 19}$$

$$S_{21} = \frac{b_2}{a_1} = \frac{U_2 - I_2 Z_0}{U_1 + I_1 Z_0} \quad \text{Eq. 20}$$

$$S_{22} = \frac{b_2}{a_2} = \frac{U_2 - I_2 Z_0}{U_2 + I_2 Z_0} \quad \text{Eq. 21}$$

$$S_{12} = \frac{b_1}{a_2} = \frac{U_1 - I_1 Z_0}{U_2 + I_2 Z_0} \quad \text{Eq. 22}$$

2.4.1 Relationship between S-parameters and Z-parameter (Impedance parameter)

S-parameters are analytically convenient to measure when working with RF and microwave systems [93]. Network parameters are traditionally used in circuit design to represent the behavior of components or subcircuits. Frequently, these components or subcircuits can be represented by equivalent circuit models composed of lumped passive components as well as controlled voltage and current sources. In such context, it is interesting to read these propagation waves (S-parameters) in terms of parasitic elements behavior (RLCG). Therefore, the measured S-parameters can be converted into Z-parameters using the conversion expression given in Eq. 23 to Eq. 30 [93]. The various

scattering parameters are all normalized considering $Z_0 = 1$. This impedance is usually the characteristic impedance of the transmission line in which the network of interest is embedded. Normalizing the scattering parameters makes them readily applicable to transmission lines of any impedance. Therefore, the conversion of S-parameters at any network parameters is normalized to Z_0 .

$$Z_{11} = Z_0 \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \quad \text{Eq. 23}$$

$$Z_{21} = Z_0 \frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \quad \text{Eq. 24}$$

$$Z_{12} = Z_0 \frac{2S_{12}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \quad \text{Eq. 25}$$

$$Z_{22} = Z_0 \frac{(1 + S_{22})(1 - S_{11}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \quad \text{Eq. 26}$$

To point out that for the four above conversion equations S_{11} , S_{21} , S_{12} , S_{22} are complex. A specific Scilab script is developed to make this conversion. Though there is straightforward conversion between S-parameters and Z-parameters, it is important to understand the fundamental theory of Z-parameters.

Z-parameters or impedance parameters describes the behavior of any linear network that can be regarded as a “black box” with number of ports. In this context, a port refers to a set of electrical terminals through which equal and opposite currents flow into and out of the network, and between which a specific voltage exists. Although a network may have any number of ports, let us consider a network with only two ports, an input port and an output port, like the network shown in Figure 51.

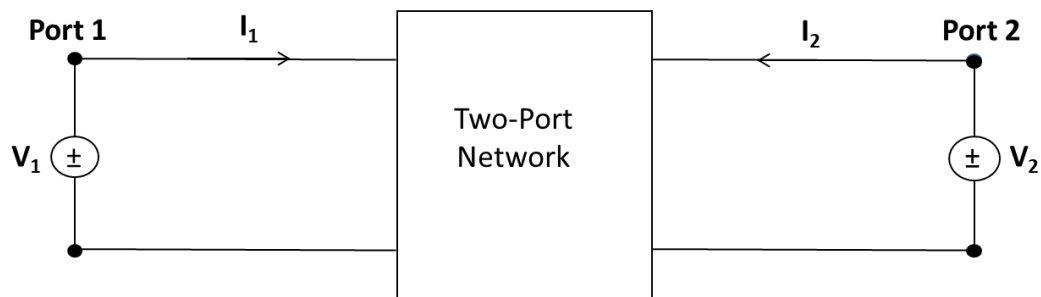


Figure 51: General two-port network of Z-parameters

Z-parameters are often used to describe the small-signal (linearized) response of non-linear networks [95]. They are also useful in the design and analysis of impedance-matching networks and power distribution networks [96].

From the Figure 51, the terminal voltages can be related to the terminal currents as follows:

$$V_1 = Z_{11}I_1 + Z_{12}I_2 \quad \text{Eq. 27}$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2 \quad \text{Eq. 28}$$

Eq. 27 and Eq. 32 can be expressed in the matrix form, where Z terms are called impedance or Z-parameters and have unit of ohms.

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad \text{Eq. 29}$$

The Z-parameters are determined by open circuiting conditions, i.e., $I_x = 0$, where $x = 1, 2$ refer to input and output currents flowing through the ports (of a two-port network in this case), thus the name open-circuit impedance parameters [95].

Case 1: Open-circuit at port 2 (i.e., $I_2 = 0$) is depicted in Figure 52.

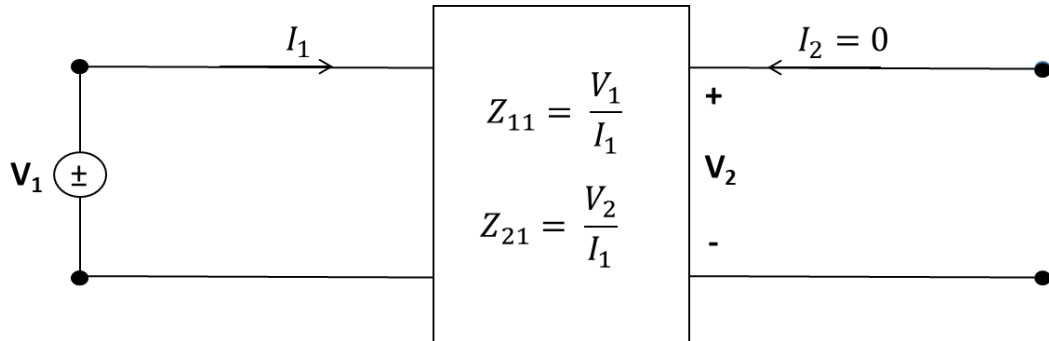


Figure 52: Finding Z_{11} and Z_{21}

Applying input current I_1 at port 1 measures the voltages V_1 and V_2 at ports 1 and 2, respectively. Substituting the condition ($I_2 = 0$) in Eq. 27 and Eq. 28 provides Z_{11} (Eq. 30) open-circuit input impedance at port 1 and Z_{21} (Eq. 31) open-circuit transfer impedance from port 2 to port 1.

$$Z_{11} = \frac{V_1}{I_1} \Big|_{I_2=0} \quad \text{Eq. 30}$$

$$Z_{21} = \frac{V_2}{I_1} \Big|_{I_2=0} \quad \text{Eq. 31}$$

Case 2: Open-circuit at port 1 (i.e., $I_1 = 0$) is depicted in Figure 53.

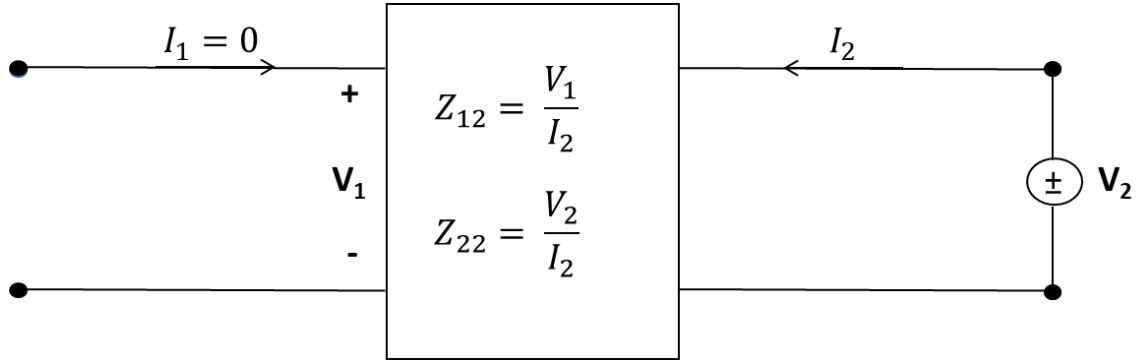


Figure 53: Finding Z_{22} and Z_{12}

Applying input current I_2 at port 2 measures the voltages V_1 and V_2 at ports 1 and 2, respectively. Substituting the condition ($I_1 = 0$) in Eq. 27 and Eq. 28 provides Z_{22} (Eq. 32) open-circuit output impedance at port 2 and Z_{12} (Eq. 33) open-circuit transfer impedance from port 1 to port 2.

$$Z_{22} = \frac{V_2}{I_2} \Big|_{I_1=0} \quad \text{Eq. 32}$$

$$Z_{12} = \frac{V_1}{I_2} \Big|_{I_1=0} \quad \text{Eq. 33}$$

In this way all the four Z-parameters can be obtained. Let us remark that, S-parameters are converted into Z-parameters only when it is needed to study the propagation waves in terms of parasitic elements. Specifically, to build the electrical equivalent circuits and perform circuit simulations. The fundamental theory of Z-parameters helps to extract the RLCG elements from Z-parameters explained in Section 2.4.2.

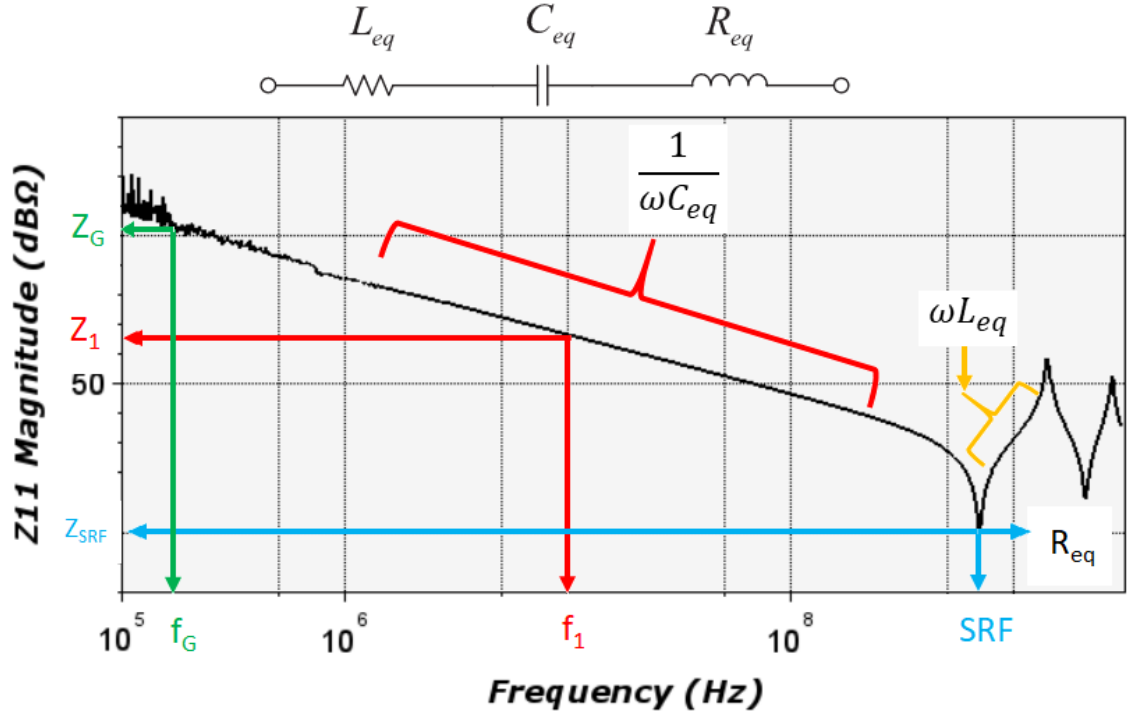
2.4.2 RLCG extraction from Z-parameters

In the literature, there are two primary approaches to extract the parasitic elements: calculation-based and measurement-based approach. The calculation-based approach can rely on techniques such as Finite Element Analysis (FEA) or electromagnetic solvers like

ANSYS Q3D (detailed in Section 2.8.1). This method involves computations based on package property and material properties. However, it has drawbacks, including extended computation times and convergence issues, especially when dealing with complex or poorly understood package structures. On the other hand, measurement-based approach can be subdivided into two categories: time-domain measurements and frequency-domain measurements. Time-domain measurements, which is based on transmission line theory extracts parasitic components by analyzing the reflected signal in relation to time delay. Nevertheless, this method has seen limited practical adoption due to uncertainties mentioned in [97].

Frequency-domain measurements can be carried out using impedance or vector network analyzers (as mentioned in Section 2.3.1 and 2.3.2). Though the impedance analyzers can compute RLC parameters, their limitations compared to VNA measurements are explained in Section 2.3.3. Therefore, the RLCG extraction process considering the VNA measurements (S-parameters) and converted Z-parameters are detailed in the following.

Each of the two-port network Z-parameters Z_{11} , Z_{21} , Z_{12} , and Z_{22} reveals a second-order RLC circuit, formed in a series combination of the individual inductances, capacitances, and resistances. Figure 54 shows a typical impedance plot (Z_{11}) of a series RLC circuit, where the frequency dependent impedance has its minimum value at the Self-Resonating Frequency (SRF). The low-frequency impedance is dominated by the capacitive components while the high-frequency impedance is dominated by the inductive components. The resistive components determine the minimum value at the SRF [97].


 Figure 54: Z_{11} magnitude for RLC computation

The total impedance is represented as shown in Eq. 34,

$$Z_T = R + j(X_L - X_C) \quad \text{Eq. 34}$$

Z_T = Total impedance in Ohms

R = Resistance (Real part of Z_T) in Ohms

X_L = Inductive reactance (imaginary part of Z_T) in Ohms and

X_C = Capacitive reactance (imaginary part of Z_T) in Ohms

The inductive and capacitive reactance can be further expressed as $X_L = 2 * \pi * f * L_{eq}$

$$\text{and } X_C = \frac{1}{2 * \pi * f * C_{eq}}$$

The impedance recovered from the impedance plot is in Decibel. For the computation the impedance is usually used in ohms. Therefore, Eq. 35 gives the conversion expression from dB to ohms. Furthermore, $Z_{(linear)}$ consist of real part, denoted as $Z_{(real)}$ and imaginary part, denoted as $Z_{(img)}$.

$$Z_{(linear)} = 10^{\left(\frac{Z_{(dB)}}{20}\right)} \quad \text{Eq. 35}$$

From the impedance plot (for example Figure 54), to extract the capacitance the zone below SRF is considered which is dominated by capacitive components. Therefore, in this case the inductive and resistive elements are neglected [97]. From which the Eq. 34 can be simplified to Eq. 36.

$$|Z_{1(img)}| = \frac{1}{2 * \pi * f_1 * C_{eq}} \quad Eq. 36$$

By rewriting Eq. 36 in terms of C_{eq} Eq. 37 is obtained.

$$C_{eq} = \frac{1}{2 * \pi * f_1 * |Z_{1(img)}|} \quad Eq. 37$$

To compute inductance, the self-resonating expression given in Eq. 38 is used. By rewriting Eq. 38 in terms of L_{eq} and substituting the required values, the value of inductance is obtained.

$$SRF = \frac{1}{2 * \pi * \sqrt{L_{eq} * C_{eq}}} \quad Eq. 38$$

$$L_{eq} = \frac{1}{(2 * \pi * SRF)^2 * C_{eq}} \quad Eq. 39$$

The resistance value is obtained by using the minimum impedance value at self-resonating frequency.

$$|Z_{SRF(real)}| = R_{eq} \quad Eq. 40$$

$$R_{eq} = 10^{\left(\frac{|Z_{SRF(real)}|}{20}\right)} \quad Eq. 41$$

Consequently, the conductance (the parallel resistance to capacitance) value is computed at the low frequency (i.e., 100 kHz). The average value of magnitude (Z_G) is considered as measurement contain noise at frequency (f_G). To compute the average first 50 default values are used. The computation is similar to the resistance value computation presented in Eq. 40 and Eq. 41.

$$|Z_G| = R_G \quad Eq. 42$$

$$R_G = 10^{\left(\frac{|Z_G|}{20}\right)} \quad Eq. 43$$

2.5 Understanding different steps of the NDT methodology using a simple case study (microstrip line)

This section is dedicated to demonstrate different steps of the NDT methodology using simple example of two-port microstrip transmission line. The idea is to introduce the two-port characterization process using VNA, which covers defining parameters on VNA, calibration process, measurement process, analysis of S-parameters.

Printed transmission lines are widely used specifically at RF and microwave frequency applications, with microstrip lines being common type. The microstrip line is a transmission-line configuration consisting of a single conductor trace on one side of a dielectric substrate and a single ground plane on the opposite side, as depicted in Figure 55. This open structure facilitates straightforward interconnections and adjustments [98].

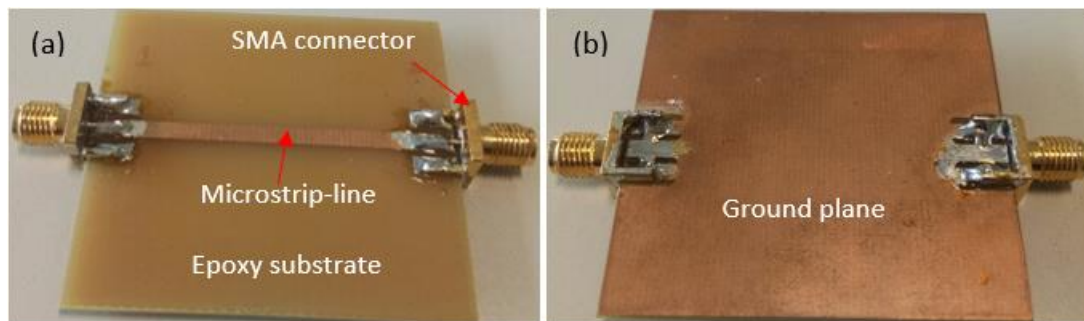


Figure 55: Microstrip line (a) Top view and (b) Bottom view

A microstrip line consists of a conductor of width W , thickness T , and length l , a dielectric substrate of thickness d and relative permittivity ϵ_r . Figure 56 and Table 5 presents the dimensions of the microstrip line.

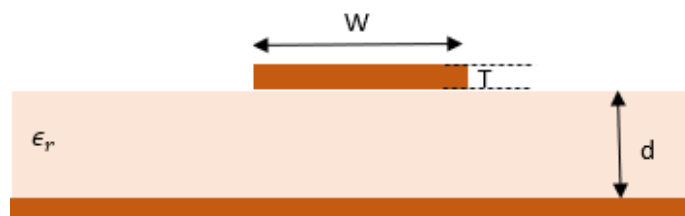


Figure 56: Microstrip line representation

Parameter	Value (mm)	Description
D	1.47	Thickness of the dielectric
W	2.67	Width of the microstrip line
L	51.05	Length of the transmission line
T	0.035	Thickness of copper conductor

Table 5: Dimensions of microstrip line

The relative permittivity (ϵ_r) value of epoxy substrate used here is 4.959 which was computed in section 2.3.1.1.

The proposed NDT methodology is explained in different steps.

Step 1: Defining parameters of VNA

Vector Network Analyzer (E5061B) from Keysight technologies, shown in Figure 57, is used for the characterization during this thesis. It is a two-port network analyzer, and the operating frequency of this equipment is from 5 Hz to 3 GHz. Figure 57 is captured just after performing SOLT calibration on VNA, that is why a stable curve is displayed.

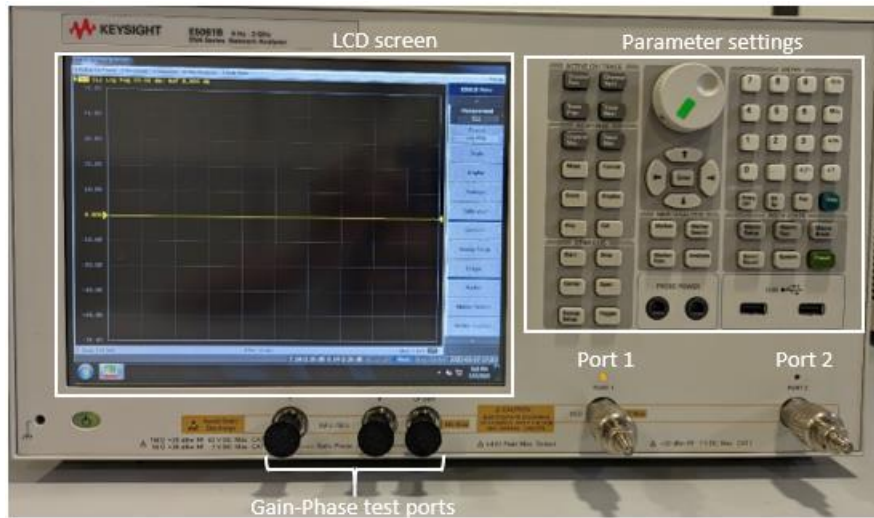


Figure 57: Vector Network Analyzer (E5061B)

Firstly, a VNA is turned on at least half an hour before performing any action on VNA. Like any test equipment, a VNA is subject to some degree of thermal drift, and it is essential to address this issue. To achieve the highest measurement accuracy, a VNA should be allowed to warm up and stabilize its internal temperature to match the ambient

conditions. Then, the VNA is preset to ensure no previous data is stored and influencing the current measurements. Then after, the coaxial cables are connected to each port to transmit the RF signals from the VNA to the device under test (DUT) and back. Usually, coaxial cables are equipped with connectors (e.g., SMA, N-type, BNC) that are compatible with the VNA's ports. These connectors ensure a secure and reliable electrical connection between the VNA and the DUT. Coaxial cables are designed to have a specific characteristic impedance (e.g., 50 ohms) to match the impedance of the VNA and the most RF components. The cables are included in the calibration, thereby any effects due to cables can be removed from the measurements of the DUT. During this thesis, the coaxial cables of SMA connector type with an operating frequency of 0 to 12.4 GHz and 50 Ω connector impedance (Appendix 4-4) are used. The cables are marked at the connecting points to VNA ports to identify and maintain a similar cable connection to respective ports for every measurement. Before performing the calibration, it is to be noted that it is essential to use identical hardware and software settings to calibrate the VNA and measure the DUT. Typical parameter settings are presented in Table 6 and are followed throughout the thesis.

Parameters	Settings
(Frequency) _{low}	10 kHz
(Frequency) _{high}	3 GHz (max)
Sweep type	Log
No. of points per sweep	1601 (max)
Averaging factor	16 (max)
IF Bandwidth	30 kHz
Source power	10 dBm (max)

Table 6: VNA parameter settings

The start frequency is set to 10 kHz to avoid noise traces, and the stop frequency to the maximum frequency available (3 GHz). A considerable trade-off exists between averaging factor and IF bandwidth, as both refer mainly to the measurement speed and accuracy. Decreasing IF bandwidth will reduce the uncertainty of the measurements at the cost of increased measurement time and is an alternative to averaging. In this case, the IF bandwidth is considered concerning the future potential, i.e., the measurement speed, as

more measurements are expected to be performed in a limited time. Therefore, the maximum averages are used throughout the calibration and measurement. The source power is chosen as high as possible to achieve the slightest uncertainty for a given IF bandwidth.

Step 2: Calibration process

Calibration kits can be either manual (mechanical) or automatic (electronic). The VNA (E5061B) is provided with individual mechanical standard calibration kit, 85032E (N-Type) shown in Figure 58. The most popular coaxial calibration technique SOLT (Short-Open-Load-Through) has been adopted.

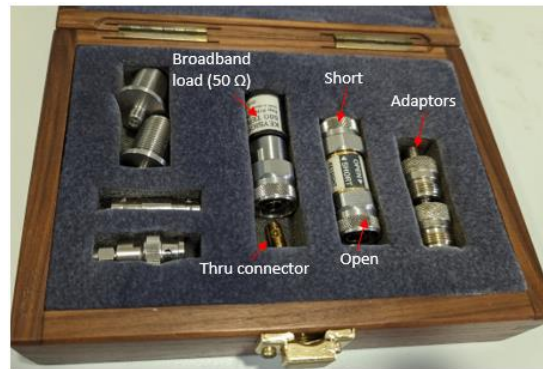


Figure 58: Calibration kit (85032E)

This calibration technique involves the process of connecting well-known reference standards to each port. Next, both the ports are physically connected to each other. In simple case, when preparing to measure an insertable coaxial device, which has mating connectors, both calibration ports can be directly connected to each other resulting in a zero-length through or flush through [87]. The calibration procedure consists in measuring 7 different reference standards (2 Opens, 2 Shorts, 2 Loads (50 Ω), and a Thru) illustrated in Appendix 4-5. Once 7 different reference standards are performed, the calibration is finally validated. Thereby, it allows to move to the next step to perform measurements.

Step 3: S-parameters measurements

The DUT is connected between the two ports as shown in Figure 59. Two female 50 Ω adapted SMA connectors are connected on either side of the copper conductor. This SMAs are coaxial connector type which fits into the male coaxial cables (Appendix 4-4). Once

DUT is well connected all four S-parameters are saved in Touchstone format (S_{11} , S_{21} , S_{12} , S_{22}).

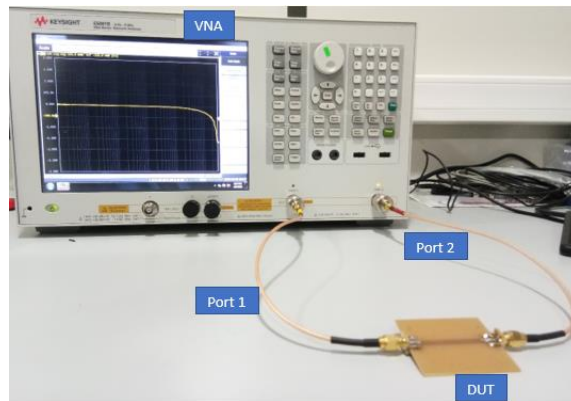


Figure 59: VNA characterization of microstrip line

Step 4: S-parameters analysis

The measured S-parameters from VNA are plotted using Scilab. A Scilab script has been developed to read the Touchstone files of VNA and plot S-parameters as a function of frequency. The DUT contains a conducting path (transmission line) with two connecting points on either side, providing the two-port connection. Therefore, it is expected to transmit injected signal from originating port to the destination port when looking into transmission parameters (S_{12} or S_{21}). On the other hand, it is expected to have low reflection when looking at reflection parameters (S_{11} or S_{22}). The magnitude is measured in decibel (dB) and phase in degree.

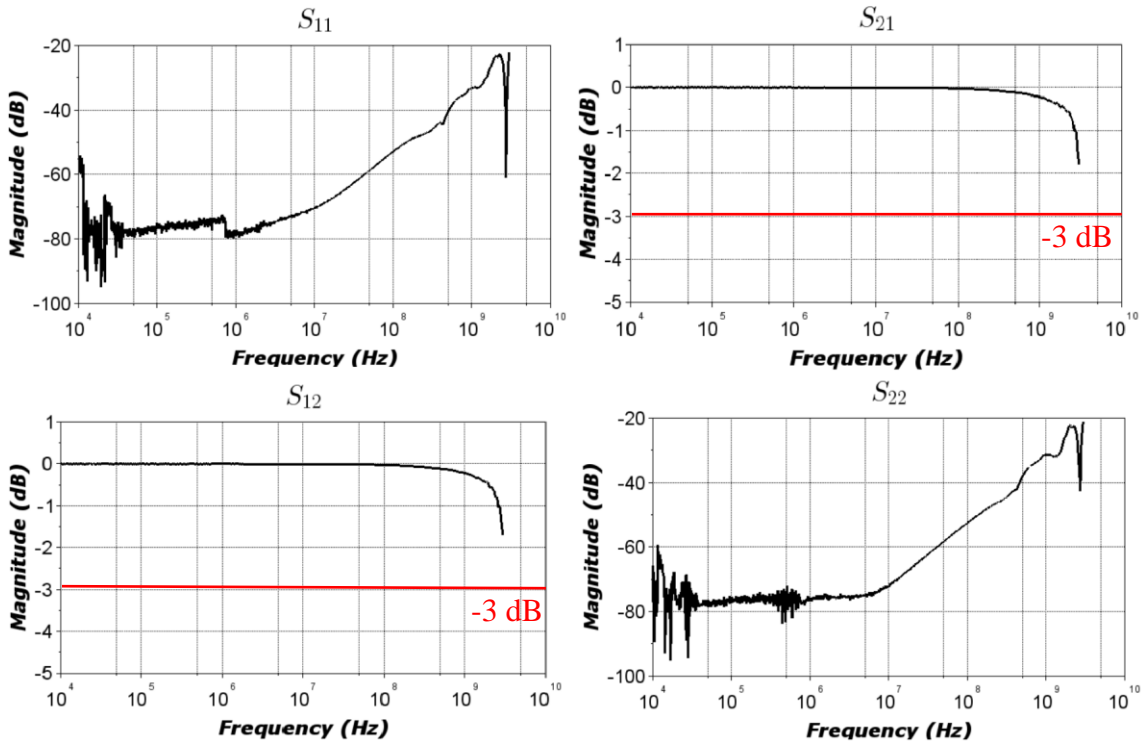


Figure 60: S-parameters magnitude of microstrip line

The most important parameters to analyze in this case would be the transmission parameters (S_{21} and S_{12}). As shown in Figure 60, considering -3 dB standard reference, S_{12} and S_{21} recovers 100% transmission from 10 kHz to 300 MHz and gradually drops to -1.8 dB at 3 GHz. On the other hand, the reflection parameters (S_{11} and S_{22}) recover the low reflection as expected. However, it is important to know why 3 dB is considered as the standard reference.

The decibel (dB) is a logarithmic way for expressing a ratio. The ratio can be based on power, voltage, current in electrical engineering. It is often referred as a logarithmic unit however it is actually not the base unit. The base unit is the Bel (which was named after famous scientist Alexander Graham Bell). Bel is defined as the logarithm to the base 10 of a ration of two powers P_1 and P_2 as shown in Eq. 44. The Bel is converted to decibel by multiplying Eq. 44 with 10.

$$Bel = \log_{10} \left(\frac{P_2}{P_1} \right) \quad Eq. 44$$

$$dB = 10 * \log_{10} \left(\frac{P_2}{P_1} \right) \quad \text{Eq. 45}$$

Power gain in decibel is expressed using Eq. 45. In the ratio of power P_1 and P_2 , the denominator P_2 is referred as reference value. Therefore, the numerator P_1 is compared to the reference value. The Eq. 45 can also be expressed in terms of voltage and currents following Ohm law (i.e., $P = V * I, V = I * R$).

$$dB = 20 * \log_{10} \left(\frac{V_2}{V_1} \right) \quad \text{Eq. 46}$$

$$dB = 20 * \log_{10} \left(\frac{I_2}{I_1} \right) \quad \text{Eq. 47}$$

Bandwidth refers to the frequency range between the upper and lower limits within which the signal or communication channel functions adequately. Figure 61 presents a graphical definition of the bandwidth. Usually, 3 dB point (at f_L and f_H) is considered as a threshold value relative to the maximum value. At this point the output power of the signal reduced to half of its input power (70.7% of its maximum).

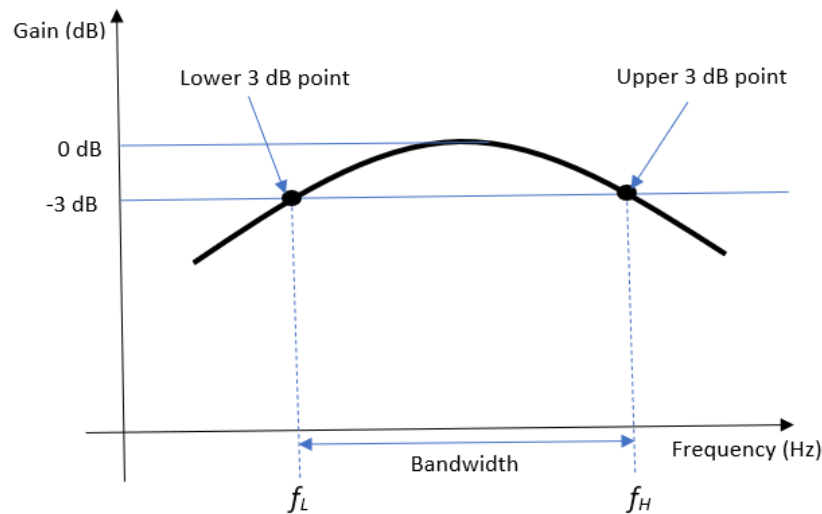


Figure 61: Definition of bandwidth

To illustrate, consider a system like in Figure 62 which has input power P_1 and output power P_2 .



Figure 62: A system with input and output

For the case when the output power is halved (i.e., $P_1 = 1 \text{ W}$, $P_2 = 0.5 \text{ W}$)

$$dB = 10 * \log_{10} \left(\frac{0.5}{1} \right) = -3 \text{ dB} \quad \text{Eq. 48}$$

Therefore, considering different factors like the VNA (E5061B) measurement sensitivity [99] and output behavior following power injection -3 dB is referred as a standard reference. It is the point at which the power at the output is half than the input.

Likewise, Figure 63 represents the S-parameters phase of a microstrip line. In general, the S-parameters phases are not often used in analysis. Whereas, they play an important role in the conversion of S-parameters to Z-parameters and mainly for the extraction of parasitic elements.

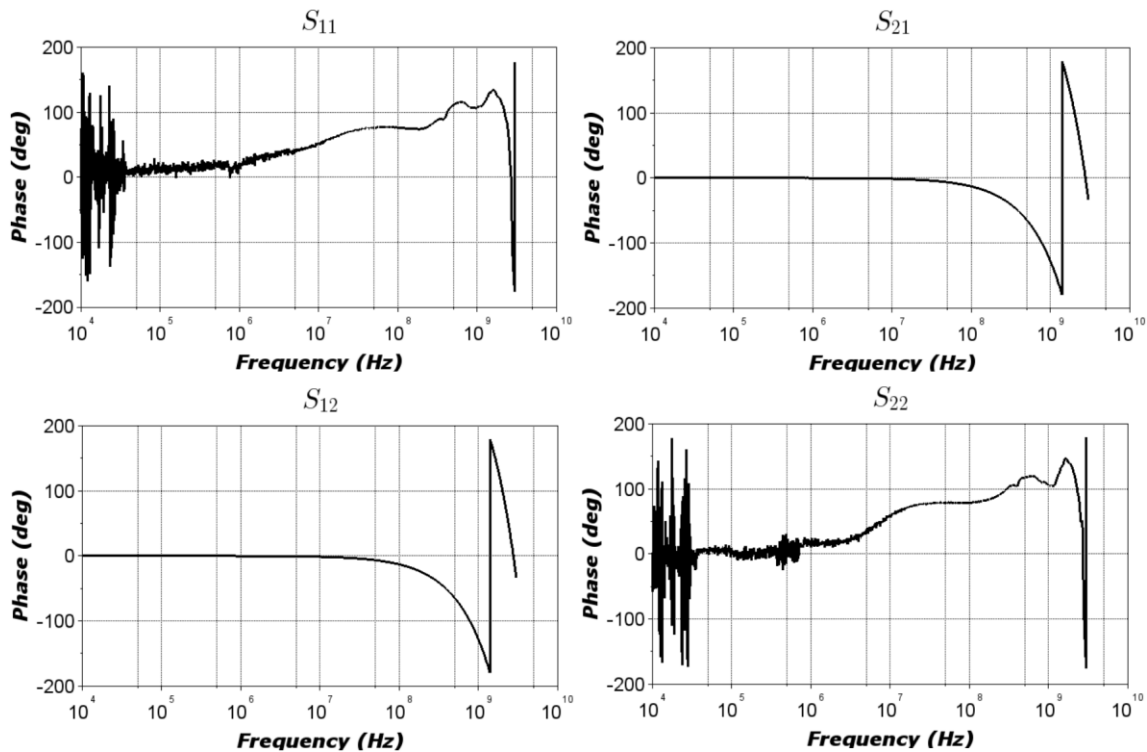


Figure 63: S-parameters phase of microstrip line substrate

To understand the behavior of DUT in electrical parameters, reading the propagation waves in terms of parasitic (RLCG) elements would be interesting. They can also bring additional information, which indeed deepens the analysis.

Step 5: S-parameters to Z-parameters conversion

The S-parameters can then be converted into Z-parameters, thanks to the conversion expressions (Eq. 23 to Eq. 26) [93]. The converted Z_{11} parameter (magnitude and phase) is presented in Figure 64.

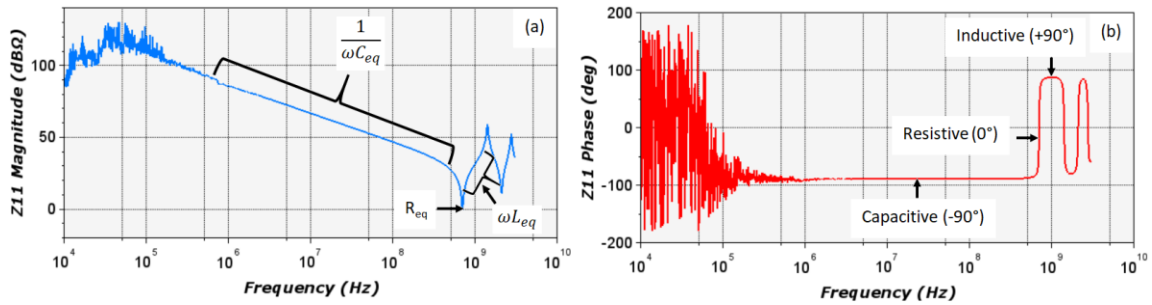


Figure 64: Z_{11} parameter converted from measured S-parameters (a) Magnitude (b) Phase

As annotated on the curve Z_{11} , it delivers RLC behavior. The steady downward slope, indicated by the term $(\frac{1}{\omega C_{eq}})$, signifies capacitive behavior with an associated phase of -90° . Conversely, the consistent upward slope denoted by (ωL_{eq}) signifies inductive behavior and corresponding phase is $+90^\circ$. At the resonance frequency, where the impedance is minimum (R_{eq}), this signifies a resistance with a phase of 0° . Similarly, Figure 65 presents the other three Z-parameters (Z_{21} , Z_{12} , and Z_{22}) which also delivers the RLC behavior.

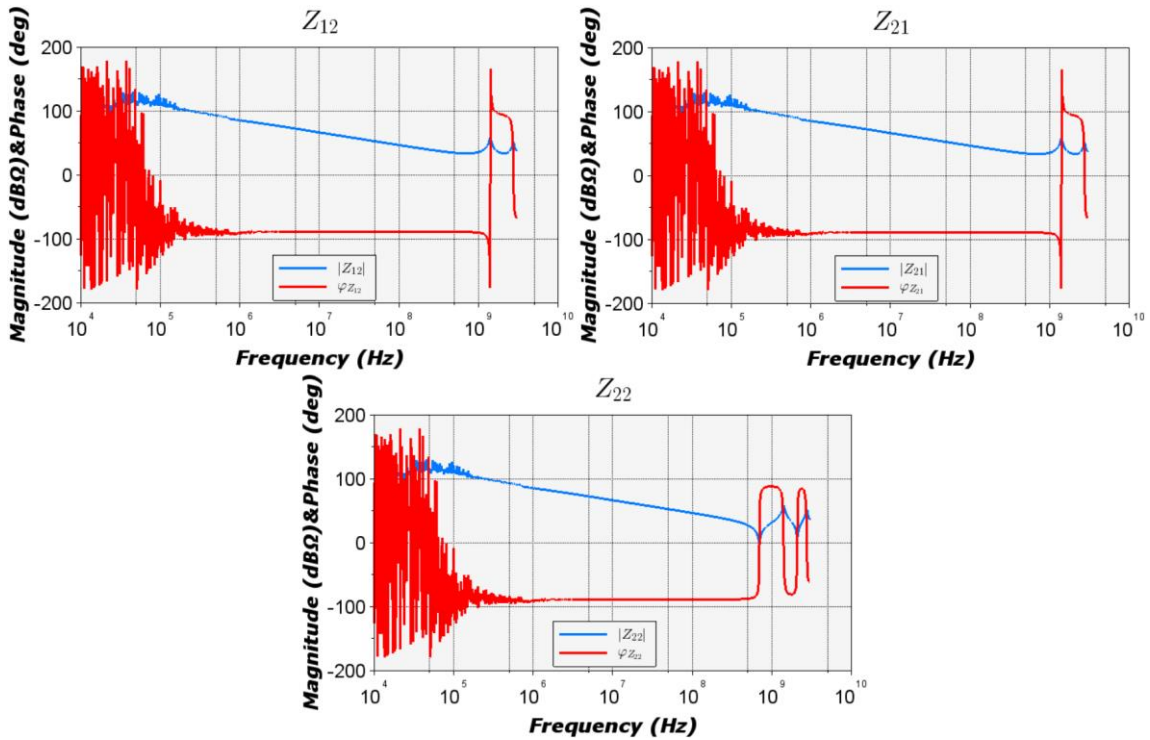


Figure 65: Magnitude and phase of Z_{21} , Z_{12} , and Z_{22} parameters

As it can be seen, at low frequency from 10 kHz to about 100 kHz the noise signal is measured. It can be due to two main reasons:

- 1) parameter settings to speed up the measurement time concerning number of measurements to be performed in limited time.
- 2) the equipment low frequency measurement accuracy

As the behavior of the curves in this frequency range (i.e., from 10 kHz to 100 kHz) is known, further curves are presented from 100 kHz to 3 GHz. Once the impedance plots are established, the RLC parameters can be extracted to construct the equivalent model.

2.6 Equivalent model construction

Equivalent models are effective method of representing the experimental measurements. They help to predict the behavior of components, circuits and systems [93]. Two-port networks are extensively employed in linear circuit analysis and design. The system being studied is characterized by a descriptive matrix that establishes the relationship between its input and output variables, including voltages and currents. Such models simplify the

input/output response of active and passive devices and circuits into a "black boxes" where the internal details become irrelevant [100].

A two-port equivalent model made of three impedances can be used as an equivalent model. To establish this model, the system should pass through a mandatory step i.e., to respect reciprocity (i.e., Z_{12} is strictly equals to Z_{21}) [100].

Step 6: System reciprocity check

In networks, reciprocity refers to the principle that the impedance observed when examining one terminal of the network from another terminal remains consistent with the impedance encountered when investigating the first terminal from the second terminal. This holds true regardless of the signal flow's direction, signifying that the network exhibits analogous behavior for signals moving in either direction. In electrical terms, this step states that the current at one point in a circuit due to a voltage at a second point is the same as the current at the second point due to same voltage at the first point [101]. Where one point and second point can be related to port 1 and port 2 respectively. The measurement parameters (S_{12} and S_{21}) of the microstrip line substrate undergo for reciprocity check as shown in Figure 66. It is also verified using converted Z-parameters (Z_{21} and Z_{12}) as shown in Figure 67.

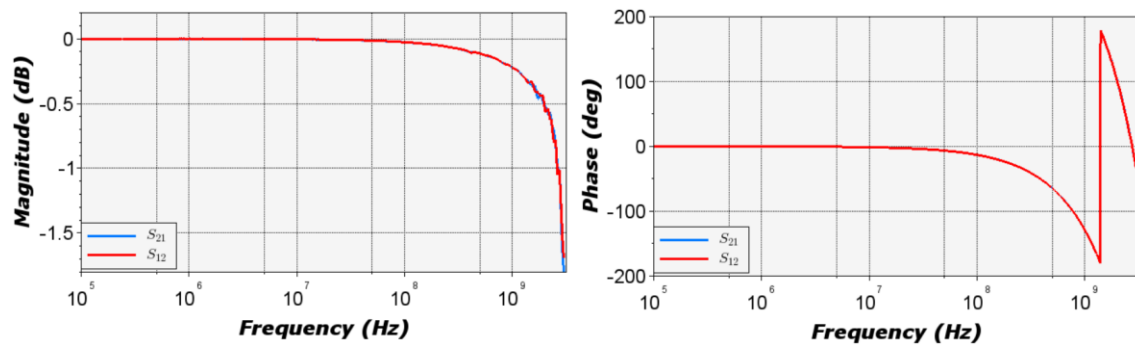


Figure 66: Reciprocity check of S-parameters (S_{21} and S_{12}) (a) Magnitude (b) Phase

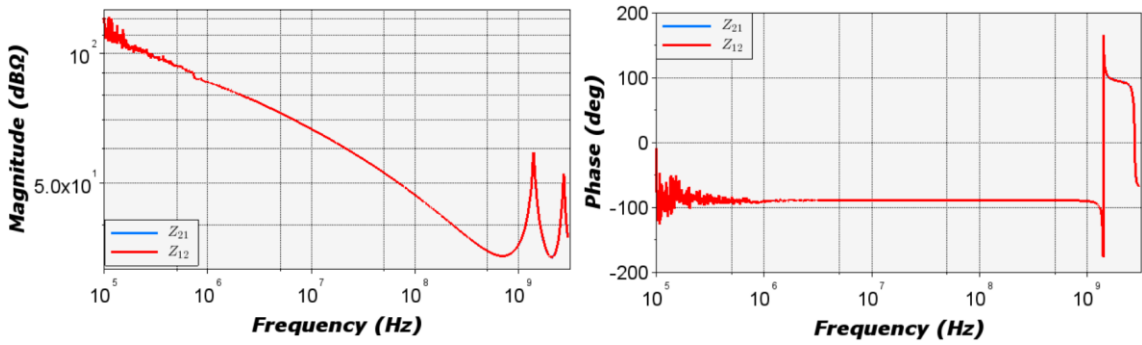


Figure 67: Reciprocity check of Z-parameters (Z_{21} and Z_{12}) (a) Magnitude (b) Phase

Thereby, a two-port three impedances model can be built using two reflection coefficients (Z_{11} and Z_{22}) and one of the transmission coefficients (Z_{21} or Z_{12}). Let us remark that, this model is only considered if the network pass reciprocity checks otherwise the model can be complex (should consider all the parameters of the network). It is one of the important steps to build equivalent models and perform simulations which is followed and validated throughout this thesis.

Step 7: Two-port equivalent impedance model

The port-based impedance parameters are considered based on total port voltages and currents for the two-port as described in Figure 51 and Eq. 29. The equivalent impedance model for a reciprocal network can be described as a T-network shown in Figure 68.

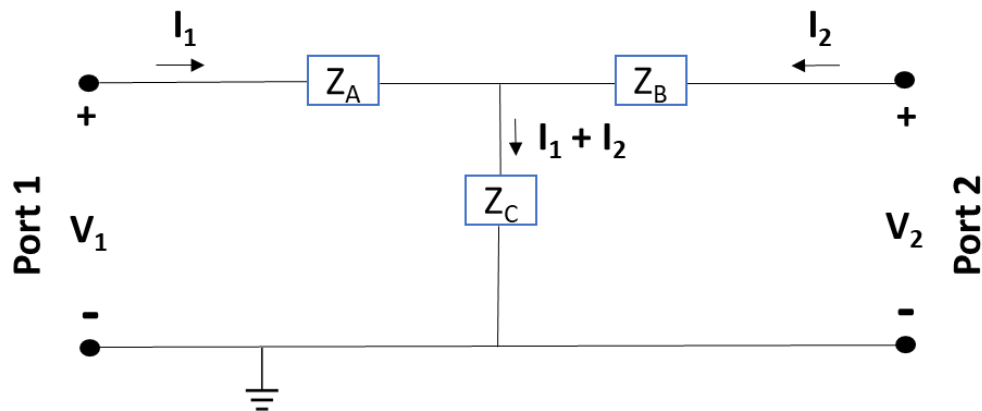


Figure 68: General equivalent circuit from a reciprocal impedance matrix

Knowing the impedances matrix, the equivalent impedances Z_A , Z_B , and Z_C can be deduced following Eq. 49, Eq. 50, and Eq. 51.

$$Z_A = Z_{11} - Z_{21} \quad \text{Eq. 49}$$

$$Z_B = Z_{22} - Z_{12} \quad \text{Eq. 50}$$

$$Z_C = Z_{12} = Z_{21} \quad \text{Eq. 51}$$

The steps that are presented so far i.e., from step 1 to step 7 remains as common steps for this proposed NDT methodology. The next step is to identify the parasitic elements representing the impedance network shown in Figure 68. As a matter of facts, the equivalent RLCG model is rather dependent on the device under test.

Step 8: Equivalent RLCG circuit construction

For example, if considered the same study case i.e., microstrip line, the equivalent RLCG elements are represented as shown in Figure 69.

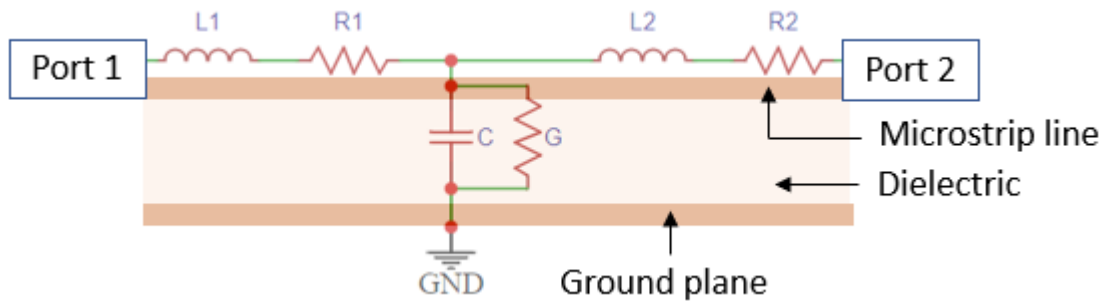


Figure 69: Lumped-element model for a microstrip line

Where R_1 , L_1 are the resistance and inductance of conducting path corresponding to port 1 connection. Likewise, R_2 , L_2 are the resistance and inductance of conducting path corresponding to port 2. C and G are the capacitance and conductance of the dielectric. As it can be seen, the RLCG elements represented are following the two-port measurement therefore they indeed represented as lumped parameters.

The next step is to compute the RLCG values and perform simulation. Thereby, the final step will be to make comparison between the experimental and simulation.

2.7 RLCG elements extraction and simulation analysis of a microstrip line

The parasitic elements are extracted considering the impedance plot and following the computation process described in Section 2.4.2 (from Eq. 35 to Eq. 43). Therefore, the Z-parameter curves achieved in step 5 are used to extract RLCG elements. As prior mentioned, the internal equivalent circuit made of RLCG is rather dependent on the device

under test. Therefore, a simple T-network shown in Figure 70 can be used to represent the transmission line.

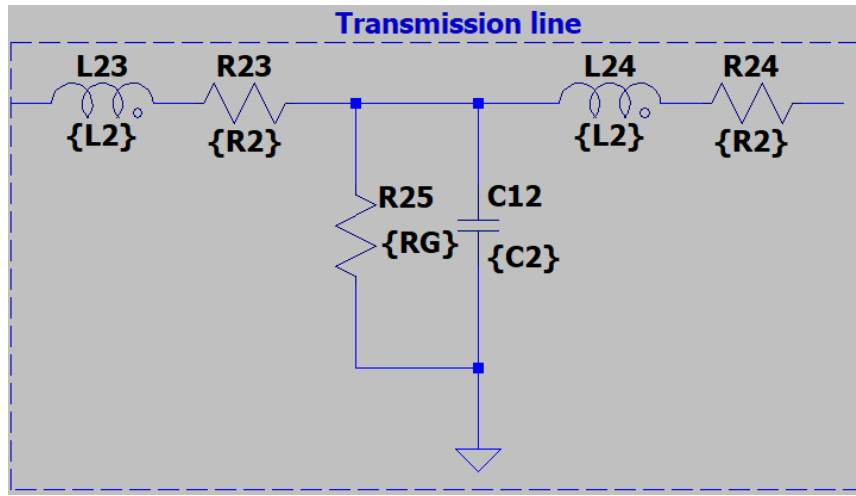


Figure 70: T-network representing transmission line

R_2 , L_2 , C_2 , and R_G are the values respectively assigned to resistance, inductance, capacitance, and parallel resistance or conductance. These values need to be identified, which is demonstrated in step 9.

Step 9: Parasitic element extraction

The RLCG extraction of microstrip line from Z_{11} , Z_{21} , Z_{12} , and Z_{22} parameters following the extraction process detailed in Section 2.4.2 (from Eq. 35 to Eq. 43) are presented in Table 7.

Parameters	Z_{11}	Z_{21}	Z_{12}	Z_{22}
R_{eq} (m Ω)	505.755	21.068	21.068	744.873
L_{eq} (nH)	6.26	6.07	6.07	6.26
C_{eq} (pF)	8.36	8.35	8.35	8.35
R_G (k Ω)	422.127	422.128	422.128	422.126

Table 7: RLCG values of microstrip line extracted from experimental data (converted Z-parameters)

As it can be seen, Figure 70 only presents the transmission line modelling, whereas to complete, the SMA model needs to be added. To remind, the DUT constitutes a transmission line with two SMAs connected on either side to provide two-port characterization. To perform the final simulation, the RLCG elements corresponding to the transmission line were extracted given in Table 7. To be realistic, the RLCG elements

corresponding to two SMAs needs to be identified. To do so, an epoxy interface with two SMAs connected through a small 50 ohms adapted transmission line was developed as shown in Figure 71.

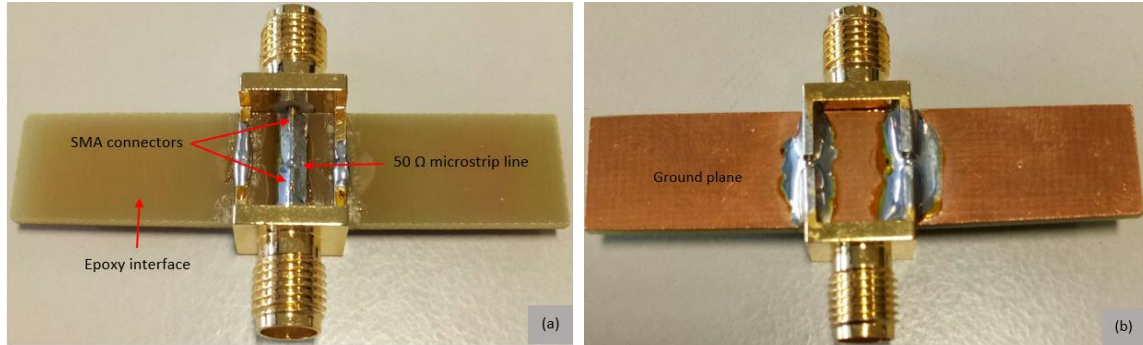


Figure 71: Epoxy interface to model SMAs (a) top view (b) bottom view

The outer part of the SMA is connected to ground plane shown in Figure 71 (b). The dimensions of the interface are shown in Table 8.

Parameters	Length (mm)	Width (mm)	Height (um)
Microstrip line	10.63	2.67	35
Epoxy substrate	-	-	1.48

Table 8: Epoxy substrate with short microstrip line dimensions

Two-port characterization explained in (section 2.5) is now applied on to this epoxy substrate (Figure 71). Figure 72 shows an electrical equivalent circuit of SMA connectors representing Figure 71. The circuit constitutes two T-networks presenting SMA 1 and SMA 2 assuming that the impact of microstrip is negligible.

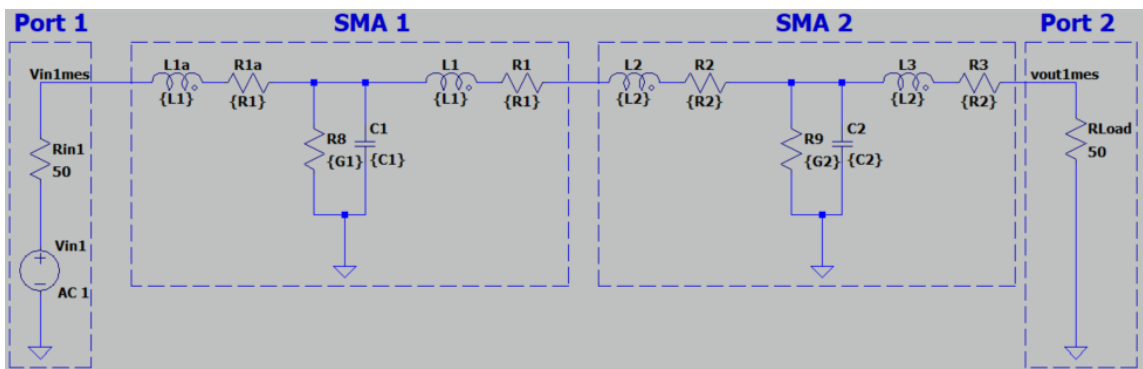


Figure 72: Electrical equivalent circuit of SMA connectors

Applying a similar RLCG extraction methodology, i.e., from Eq. 35 to Eq. 43, the RLCG values of SMA 1 and SMA 2 are obtained given in Table 9. The values R_i , L_i , C_i , and G_i corresponds to SMA 1 and R_2 , L_2 , C_2 , and G_2 corresponds to SMA 2.

Parameters	SMA 1	SMA 2
R_i (m Ω)	166.23	129.67
L_i (nH)	1.48	1.60
C_i (pF)	1.08	1.08
G_i (kS)	22.29	22.35

Table 9: RLCG values of SMA connectors extracted from experimental data

Table 9 presents R_i , L_i , C_i , and G_i (where $i = 1,2$), i being 1 presents SMA 1 values and 2 for SMA 2 values. It is interesting to point out, the RLCG values obtained for SMA 1 and SMA 2 are close to each other. These values are plugged into the electrical equivalent circuit (as detailed in Figure 72) to perform the LTspice simulation. Thereby, the experimental and simulation results are compared as presented in Figure 73.

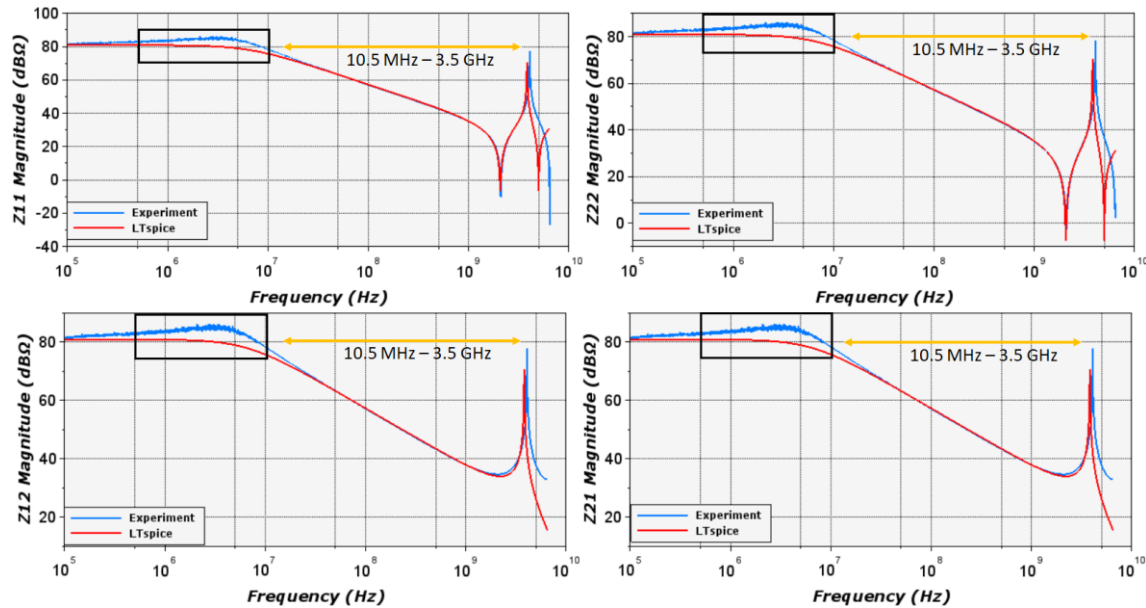


Figure 73: Experimental and simulation comparison of SMA modelling

The comparison of experimental and LTspice curves are shows a good agreement from 10.5 MHz to 3.5 GHz with any difference between experimental and simulation curves less than 2 dB. At low frequency, using the parallel resistance R_G , it fits the experimental curve from 100 kHz to 500 kHz. Whereas, in the bandwidth highlighted in black box the

difference of around 5 dB is noticed as it is difficult to obtain the exact conductance value due to some high oscillations at low frequency.

Having modelled the SMA connectors, the equivalent electrical schema shown in Figure 70 is updated to Figure 74.

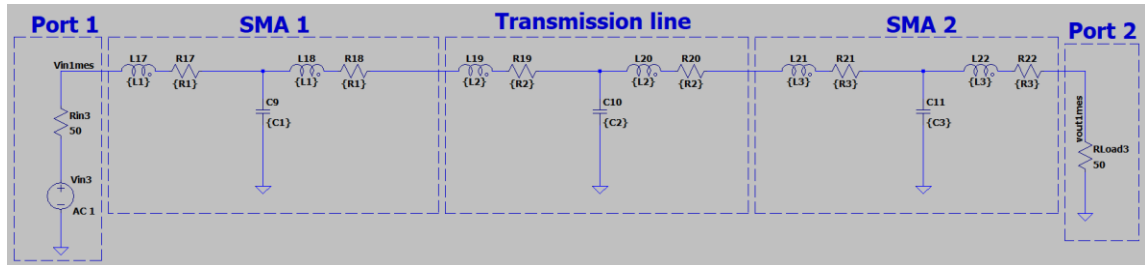


Figure 74: Two-port electrical equivalent circuit of a transmission line with SMA connectors

The RLC values presented in Table 7 are the values of microstrip line which includes SMA. For a precise modelling the RLC values of SMA alone are extracted given in Table 9. The RLC values given in Table 9 are plugged into SMA 1 and SMA 2 model of Figure 74. As the transmission line model includes the SMA, the SMA model values are deduced from the transmission line model in Figure 74. The parallel resistance (RG) is not included in the equivalent circuit as it exhibits no impact. The experimental and LTspice simulation curves are compared and shown in Figure 75.

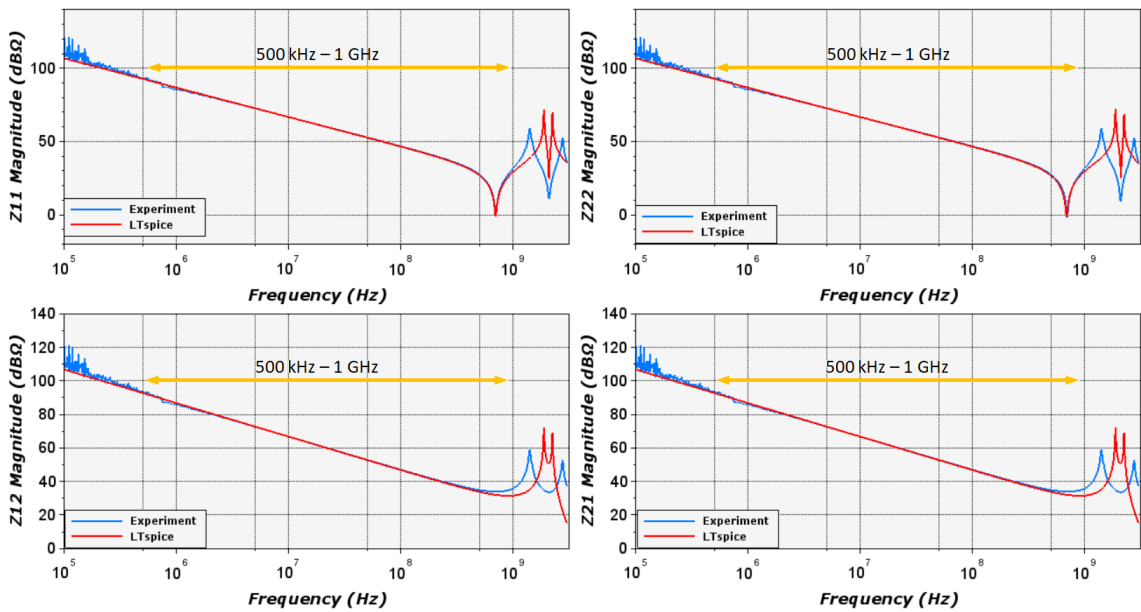


Figure 75: Experimental and simulation comparison of microstrip line substrate

As highlighted in Figure 75, the experimental and LTspice simulation curves are in good agreement from 500 kHz to 1 GHz with any differences less than 3 dB. Modeling the microstrip line by a single T-network is justified by the fact that its length is much shorter than the wavelength λ up to 1 GHz. It means to approximate the transmission line as a single RLC cell (or single T-network) the line should be electrically short (i.e., shorter than $\frac{\lambda}{10}$). A simple way to overcome the fact that the length of the studied line is longer than $\frac{\lambda}{10}$ is to subdivide this line.

$$\lambda = \frac{v}{f} \quad \text{Eq. 52}$$

Where, λ is the wavelength, v is the velocity of propagation (m/s), and f is the operating frequency transmission line (Hz). The wave speed of the transmission line can be obtained using Eq. 53.

$$v = \frac{l_T}{\sqrt{L_{eq} * C_{eq}}} \quad \text{Eq. 53}$$

Where, l_T is the length of the transmission line in mm, L_{eq} and C_{eq} are the inductance and capacitance of the transmission line expressed in nH and pF, respectively. For l_T of 51.054 mm, L_{eq} and C_{eq} being 6.26 nH and 8.35 pF (given in Table 7), the velocity of propagation computed is $2.23e^8$ m/s. For a frequency of 2 GHz, the wavelength $\lambda = 11$ cm and so $\frac{\lambda}{10} = 1.1$ cm. Therefore, to achieve an accurate model until around 2 GHz, the transmission can be subdivided by 1.1 cm sublins. The electrical equivalent schema presented in Figure 74 has been updated to Figure 76 with two T-networks for the transmission line. RLC parameters constituting to transmission line are distributed accordingly following the division of the line (i.e., divided by 2), identified in Figure 76. The experimental and LTspice simulation curves are compared and presented in Figure 77.

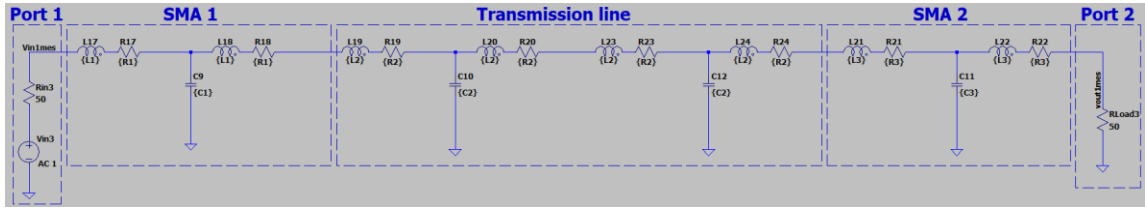


Figure 76: Electrical equivalent circuit with 2 T-networks for microstrip line

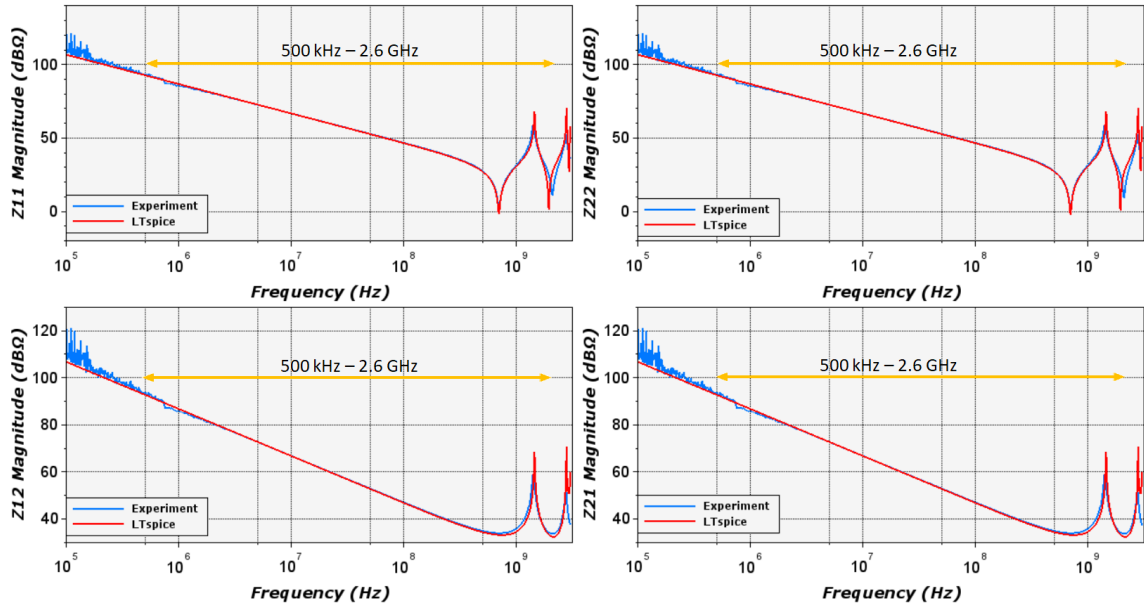


Figure 77: Experimental and simulation comparison of an equivalent circuit with 2 T-networks for microstrip line

The results are in good agreement from 500 kHz to 2.6 GHz following the post-processing of experimental and simulation data (Figure 77). Let us remark that below 500 kHz, the experimental data generate some oscillations. It is difficult to perfectly fit the simulation curve below 500 kHz, however, it recovers the slope. From 500 kHz to 2.6 GHz, some slight variations are observed (Figure 77). The differences are less than 1.5 dB. Modeling transmission line while respecting the wavelength is crucial for designing efficient and high-performance systems, especially in high-frequency applications. To achieve such models, it is important to take into account the physical dimensions of the transmission line relative to the wavelength of the signal being transmitted.

2.8 Other simulation tools

This section provides information about the other NDT simulations tools that are used during the thesis. Though an in-depth study has not been made on these tools, an attempt was made to support the future work. As mentioned, at the begin of this chapter using

electromagnetic solvers like Ansys Q3D is one of the ways to extract parasitic elements. The other tool is Advanced Design Systems (ADS) from Keysight Technologies. To begin with these tools a simple microstrip line substrate is chosen.

2.8.1 Ansys Q3D case study on microstrip line

The first step to proceed is designing 3-dimensional (3D) model on Q3D software. Considering the geometry and material information of the microstrip line prototype (Table 5), a 3D model was built on Q3D as illustrated in Figure 78. The design is assigned with “Nets” to define an electrical connection of conductors into an entity that interests for simulation. The current path is defined by exciting the conducting paths using source and sink terminals. The source and sink terminals are inputs and outputs. The terminals can be assigned before or after assigning nets. But every net needs one current sink and at least one current source in order to run the AC RL (AC Resistance and Inductance) solver [102]. The capacitance and conductance (CG) solver, can be run without any sources and sinks. The terminals are usually get assigned to 1D or 2D elements in the 3D modeler.

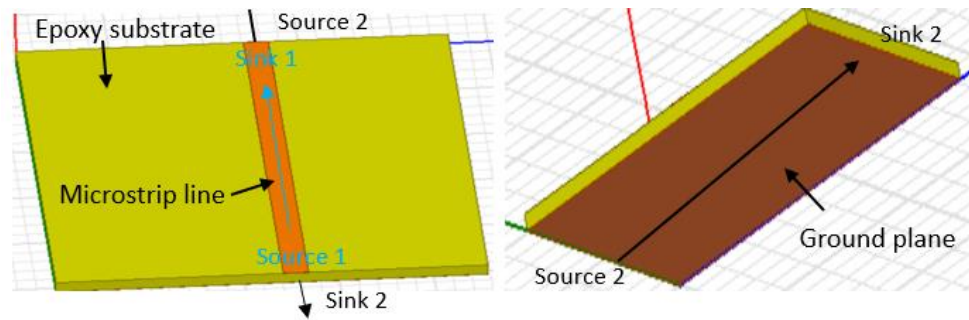


Figure 78: 3D design of microstrip line substrate on Ansys Q3D

For structures like a microstrip line, which has a large ground plane, a ground net can be used which is the ideal solutions. In the one hand, the ground plane can be excited by source and sink terminals which produce a path for the current and inductance in the ground plane. The next step is to define the analysis setup which specifies a solution frequency given in Appendix 4-6. This step allows to choose the matrix values (C, G and R, L) for the solution selection solvers. The frequency sweep is also possible explained in [102]. Having set all these parameters the simulations can be run and the solve setup display pops up determining what simulation results became available based on the choice made (Appendix 4-7). The extracted values from Q3D are plugged into the electrical

equivalent circuit developed to represent the microstrip line and compared with the experimental data given in Figure 79. The results agree with difference of close to 3.5 dB between experimental and LTspice simulation from 100 kHz to 500 MHz. The differences could be due to the fact that the SMA connectors are not included in the design. Whereas, the impact of SMA connectors is usually noticed at high frequency, which could justify that the resonances are not exactly recovered. On the other hand, a small difference of 1.5 dB observed in capacitance dominating region can be related to grounding considerations and type of capacitance matrix that is used for the extraction. This part of work still needs to be explored to give better conclusions.

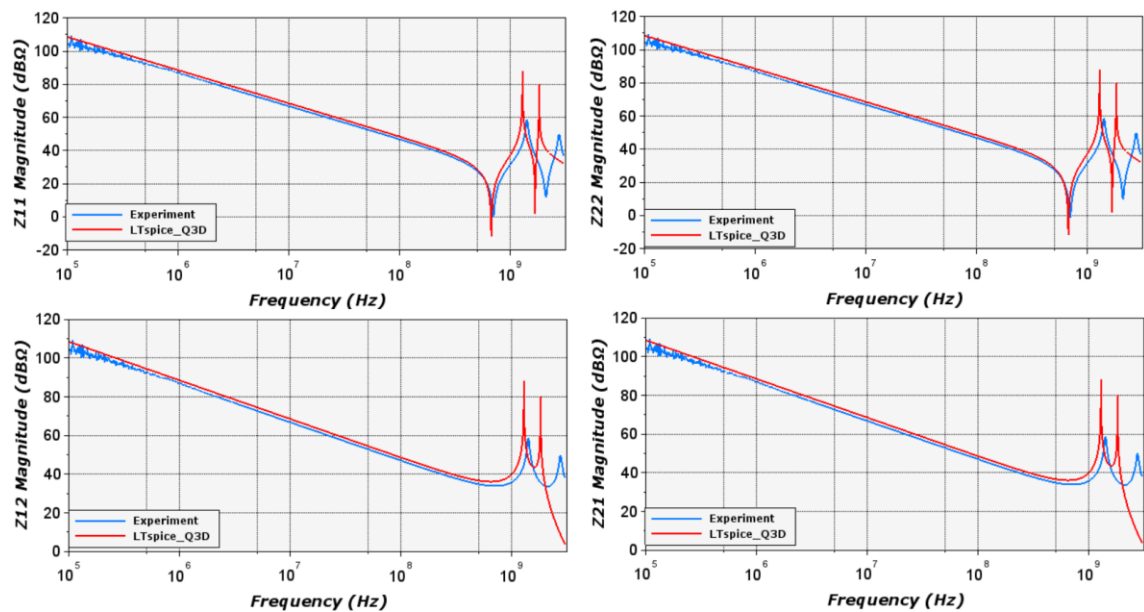


Figure 79: Comparison of experimental and LTspice simulation (using RLC extracted from Q3D) of a microstrip line

However, to give a try, we have updated the design, an SMA model is built and simulation of complete model (i.e., microstrip line substrate with SMA model) has been performed which is presented in Figure 80. The results agree with a difference of 2 dB between experimental and LTspice simulation from 100 kHz to 1.2 GHz for transmission coefficients and from 100 kHz to 350 MHz for reflection coefficients. However, the shift in resonance is pronounced from 170 MHz to 230 MHz. We have expected to see improvement in simulation results with updated model but difference in curves is still observed which is more pronounced above 1.2 GHz. We assume that it can be due to

grounding considerations, type of capacitance matrix that is used for the extraction. This part of work still needs to be explored to give better conclusions.

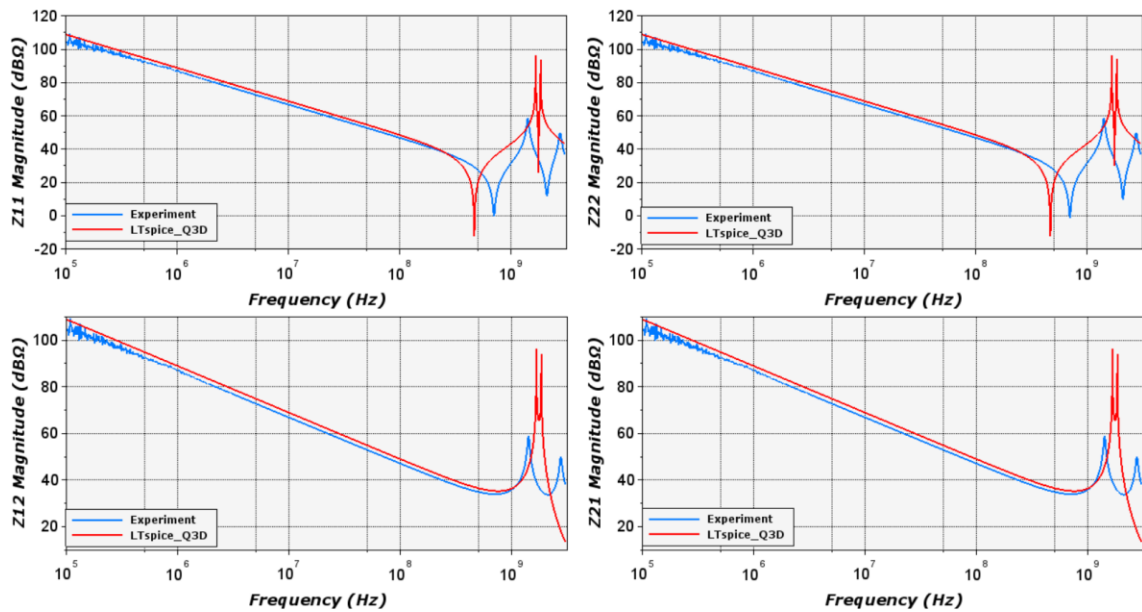


Figure 80: 3D design of microstrip line substrate with SMA and experimental and LTspice simulation comparison

For the frequency application above 1 GHz there is high possibility of significant inaccuracy following Q3D extractions. However, there are certain methods like segmentation method where the DUT can be divided into a set of electrically small segments to improve the accuracy of high frequency simulations [103]. This method can improve the accuracy but would be complicated with complex geometries. This thesis is not much focused on it however it can be a possibility for the future.

2.8.2 Advanced Design Systems (ADS)

ADS (Advanced Design System) is a wide-frequency finite element simulation software package, also used for electromagnetic compatibility modeling. It offers two simulation environments generating S parameters: a 2D environment (electrical circuit and cosimulation), and a 3D environment (EMPro). This section demonstrates the 2D and 3D simulations and its comparison with experimental data. This part of work is carried out with the help of an intern candidate (Gontran MANDAMBA) [104]. The microstrip line prototype is still chosen as a demonstrator. The homemade packaging will be studied later. The ADS environment allows several simulation possibilities i.e., it is possible to build a circuit simulation and then process to 2D and 3D models and vice versa. In addition,

tuning mode option in ADS allows to perform modeling by optimizing the parameters to be as close as possible to the experimental results. Figure 81 presents different possible simulation environments.

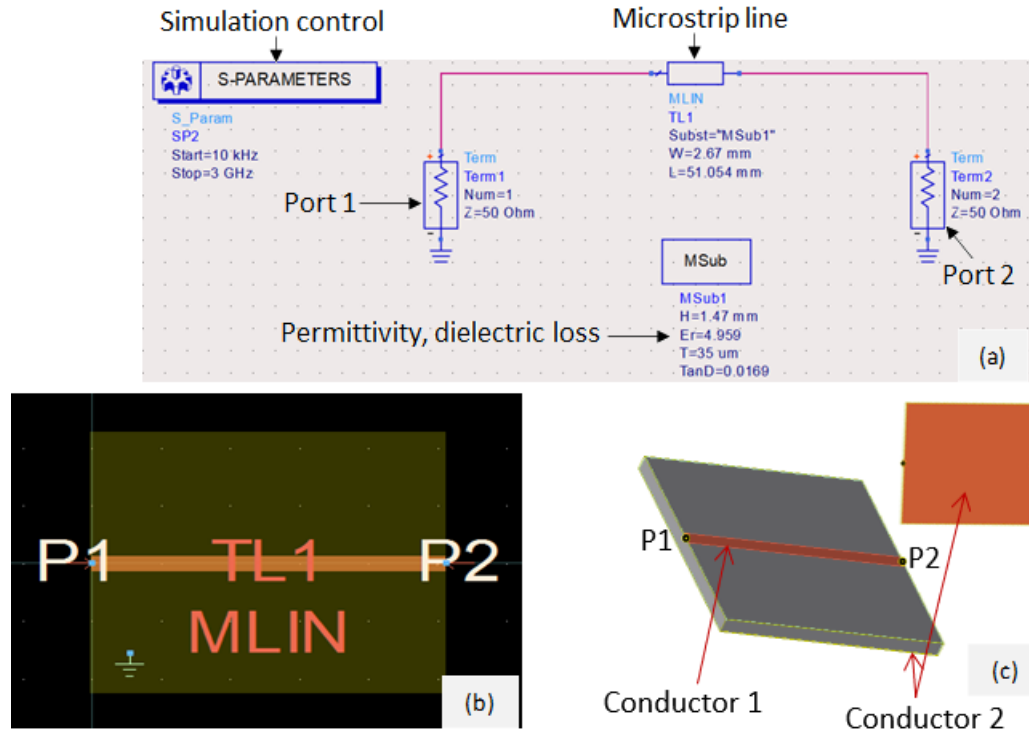


Figure 81: (a) Circuit simulation, (b) 2D model, and (c) 3D model

Circuit simulation which does not take into account all the elements of the module, the results obtained are quite far from the experimental measurement, and only precise tuning is able to correct certain discrepancies. Therefore, a 3D model is developed making the most of all the microstrip line's constructive elements. It is developed using 3D simulation environment. In this environment, the model established by defining the substrate (here epoxy) material and its properties on which the copper conductors rest are given in Appendix 4-8. Once having designed 3D model, a finite element simulation is run and is compared with experimental data given as illustrated in Figure 82. The transmission curves (S_{21} and S_{12}) are in good agreement with experimental with any difference 0.7 dB from 100 kHz to 1.5 GHz.

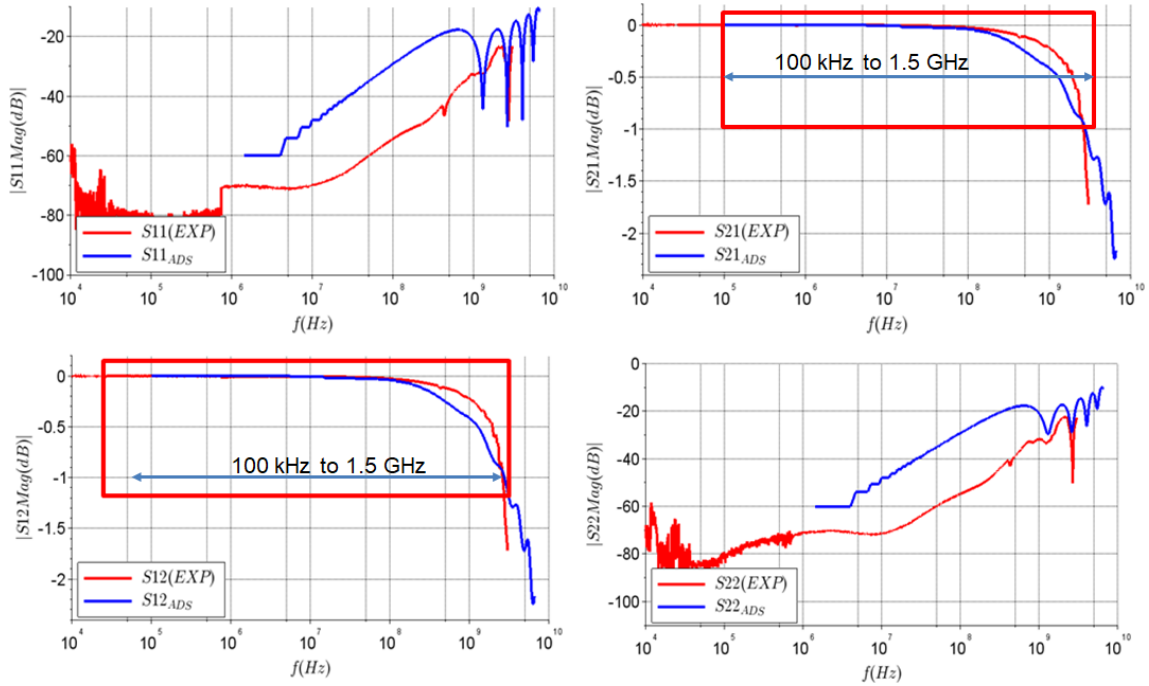


Figure 82: Comparison of VNA results and ADS simulation of the 3D model

A cosimulation is performed by adding the SMA circuit model and the 3D microstrip line symbol generated from the layout given in Figure 83. RLCG values used for SMA model are extracted from SMA characterization given in Table 9. Thereby, the simulation and the experimental data are provided in Figure 84.

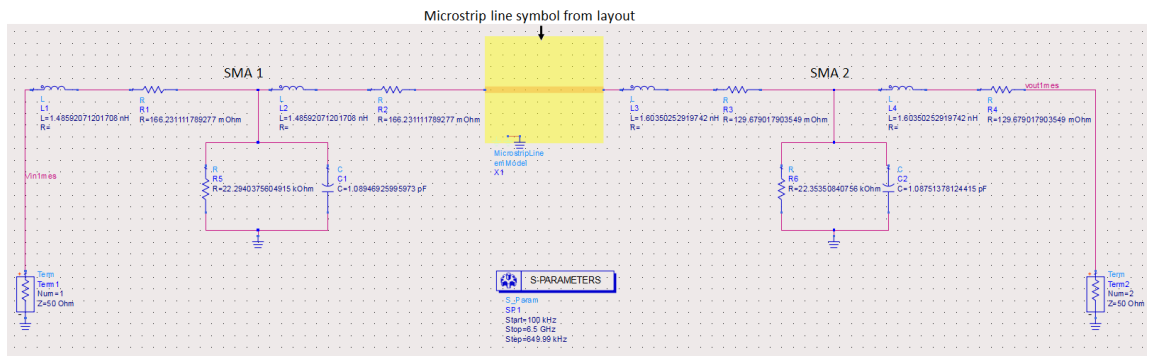


Figure 83: Cosimulation in the ADS circuit environment

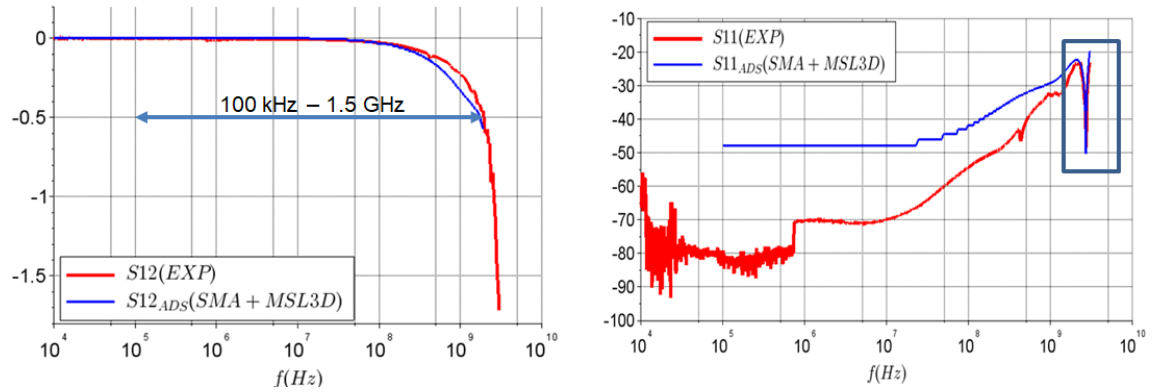


Figure 84: Comparison of VNA results and ADS cosimulation

The results obtained are interesting as the real structure of the module is respected as much as possible, taking all its components into account. The tuning mode allowed to get a model more precisely. The results recover good transmission with any difference < 0.4 dB from 100 kHz to 1.5 GHz and also recovers the resonance highlighted on reflection coefficient.

2.9 Conclusion

This chapter presents the NDT methodology, constituting the experimentation, computation, and equivalent model construction. The experimentation presents the two-port S-parameters characterization using Vector Network Analyzer (VNA). Although several parameters (Z, Y, H) can describe any two-port network, measuring total voltages and currents at high frequencies is challenging by performing open and short circuits. Also, the active devices become unstable when terminating by a short and open circuit. Hence S-parameters are the preferred method of characterizing, as they express the electrical networks using matched impedances. The methodology is explained in different steps considering a simple case study (microstrip line). For example, step 1 to 4 describes the calibration process, S-parameters measurement, and analysis, followed by S-to-Z parameter conversion in step 5. In step 6 to 7, described the construction of an equivalent model constituting the lumped-element model by validating the requirements to build the model. The parasitic element extraction which is one the crucial steps of the methodology allow to perform circuit simulations and compare with the experimental data. Wavelength of the transmission line is essential for accurate modeling, especially in high-frequency applications. It allows to predict and mitigate certain issues like impedance matching,

signal reflections, resonance, and other wavelength-dependent effects. Therefore, an effort has been made to improve the accuracy of modeling for a microstrip line prototype which led us to have quite interesting results. In addition, this chapter also discusses time-domain and frequency-domain networks and makes a comparison. The frequency-domain network and their corresponding measurement types of equipment are described in detail. The following chapter continues to describe the methodology and focuses more on experimental and simulation aspects applied to power electronic assemblies. In addition, two other simulation tools (Ansys Q3D and ADS) which were tried during this thesis are presented. Though these tools were not study in-depth, there were some interesting results which are presented.

Chapter 3 :
**Application of NDT methodology for a wide
frequency band characterization of power
electronic assemblies (experimental and
simulation analysis)**

3.1 Introduction

Power electronic assemblies often operate at high frequencies, comprising various passive and active components like capacitors, inductors, diodes, and transistors. Therefore, it is essential to study the behavior of these assemblies as they play crucial role in leading the reliability and efficiency of the system. The wide frequency band characterization is a measurement technique that addresses design, analysis, and validation of power electronic assemblies, especially in high-frequency and high-power applications. By considering the system as a black box, this characterization enables to assess the assembly's behavior as the signal integrity. Power electronic assemblies may have specific frequency response. In such a case, S-parameters measurements provide data on how the assembly behaves over a range of frequencies, helping to ensure that it meets performance specifications. This Chapter demonstrates the application of NDT methodology for a wide frequency band characterization of healthy power assemblies. The power assemblies that are specifically studied are TO packages and power modules based onto an Active Metal Brazing (AMB) ceramic substrate. The behavior of the assemblies is analyzed through reflection and transmission S-parameters coefficients and their conversion to Z-parameters. Electrical equivalent circuits and respective circuit simulations are also addressed.

3.2 Application of NDT methodology to discrete power devices

This section details the NDT methodology applied to discrete power devices. It is applied to different TO packages, some listed in Table 1. The global idea of the methodology is explained in different steps in Chapter 2. The TO packages that are used during this thesis have three connection pins. Therefore, the methodology is updated. The update is based on how these three terminals are used to perform the two-port characterization and its corresponding simulation.

3.2.1 Two-port S-parameters power device characterization

Before performing the S-parameters measurement, there are several requirements. The first preparation is to design an interface to ensure reliable and low inductance connections between the device terminals and VNA. To achieve high accuracy, the design should consider negligible loss, flat frequency response with linear phase, and good impedance

match [97]. Therefore, an epoxy interface was developed for interfacing between the VNA and DUT, which integrates two 50 Ω SMA female connectors. Figure 85 presents the epoxy interface where the discrete power device is vertically placed on the interface. The thickness of epoxy and metallization are 1.5 mm and 35 μm , respectively. The characteristic impedance of the access pad tracks is also designed to be 50 Ω adapted to ensure impedance matching. Figure 85 presents the interface designed to support the TO-247. Likewise, an interface is also developed for the packages following TO-220 package dimensions presented in Appendix 4-9.

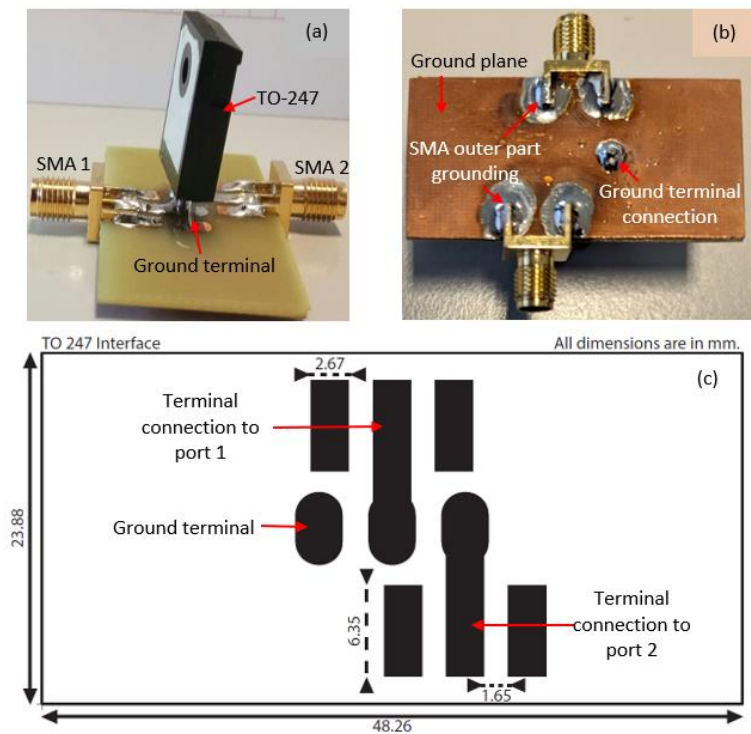


Figure 85: Epoxy interface of TO-247 package vertically placed (a) top view, (b) bottom view, and (c) footprint of top view

For any power device having three terminals, SiC MOSFETs or IGBTs, there exist three straightforward configurations given in Table 10. Figure 85 presents the interface corresponding to configuration 1, denoted config1. In similar way the interfaces corresponding to config2 and config3 are designed and manufactured.

Configuration's name	Gate	Drain/Collector	Source/Emitter
config1	Grounded	Port 1	Port 2
config2	Port 1	Port 2	Grounded
config3	Port 1	Grounded	Port 2

Table 10: Two-port configurations for three terminals TO packages

Sometimes a notation is used to represent configurations for this study (i.e., config1 = GCOM, eventually SCOM and DCOM for config2 and config3, respectively). In the following, the generic NDT methodology is applied to a three-terminal TO-247, SiC MOSFET (C2M0160120D) from “Wolfspeed” whose details are provided in [105]. The application of the methodology to other TO packages is summarized at the end of the Section 3.2.1.

In the following, the config1 (given in Table 10) is considered i.e., drain connected to port 1, source connected to port 2, and gate terminal grounded. However, a comparison with the other configurations (given in Table 10) is also made. The characterization is performed under zero DC biasing (i.e., when the device is in the off state). Figure 86 presents the two-port S-parameters characterization for a discrete power device.

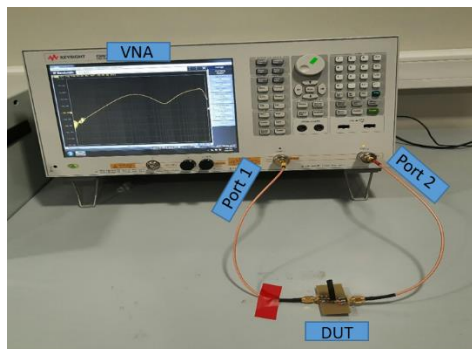


Figure 86: Two-port S-parameters measurement for a SiC power MOSFET

The S-parameters magnitude measured from VNA considering config1 are presented in Figure 87. When operating with zero DC bias, the graphs depicted in Figure 87 (a) & (b) demonstrate minimal transmission and significant reflection, ranging from 100 kHz to 550 MHz. These findings align with our expectations when the switch is in the “off” state. The measurements highlighting the high reflection and low transmission between the drain and source, affirm that the device is functioning as an electrical open circuit.

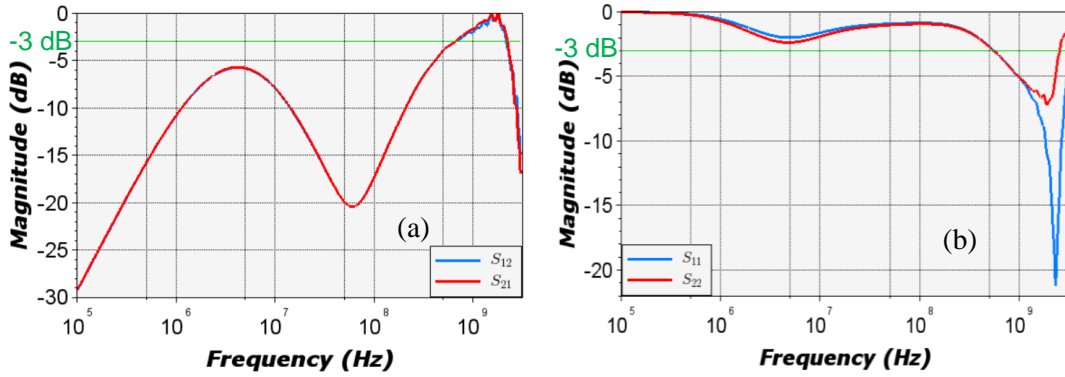


Figure 87: S-parameters magnitude (a) transmission (S_{12} & S_{21}) and (b) reflection (S_{11} & S_{22})

The measured S-parameters are then converted into Z-parameters using conversion expressions presented in Chapter 2 (from Eq. 23 to Eq. 26). Figure 88 presents the Z-parameters converted from S-parameters. Figure 88 (a) & (c) presents the magnitude and phase of reflection coefficients (Z_{11} & Z_{22}), respectively. Likewise, Figure 88 (b) & (d) presents the magnitude and phase of transmission coefficients (Z_{12} & Z_{21}), respectively. All the four parameters (Z_{11} , Z_{21} , Z_{12} , and Z_{22}) exhibit the RLC behavior confirmed from phase plots with -90° , 0° , and $+90^\circ$ representing the capacitive, resistive, and inductive behavior respectively.

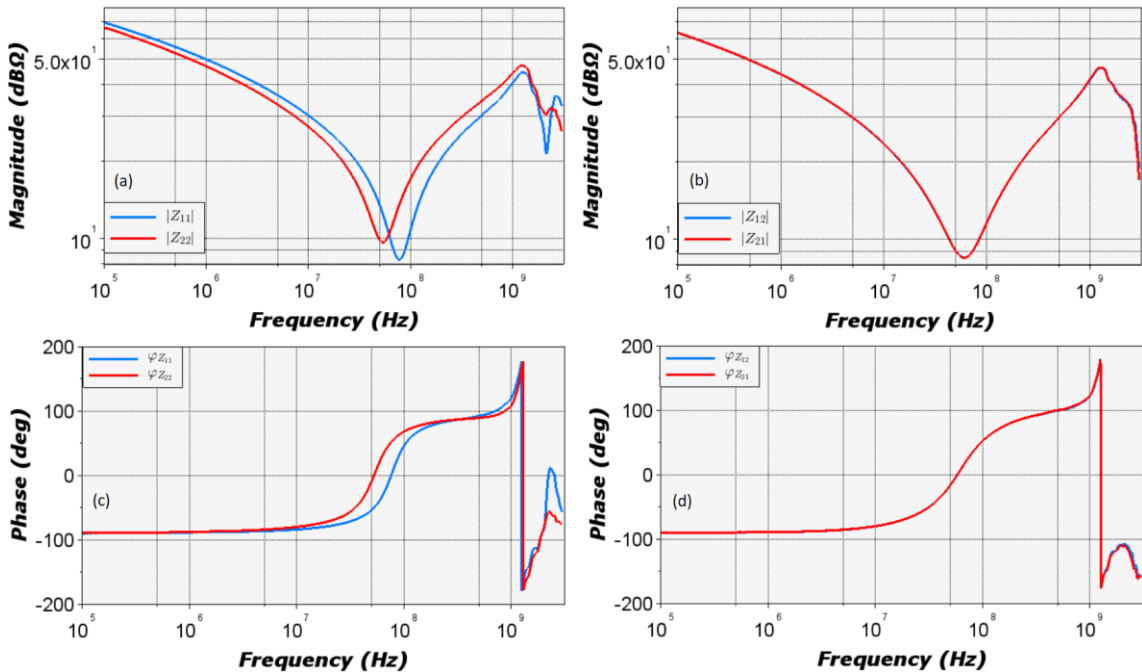


Figure 88: Z-parameters magnitude and phase of a TO-247 SiC MOSFET in a healthy state

The reflection parameters given in Figure 88 (a) & (c) presents some variations between Z_{11} and Z_{22} in magnitude and phase, meaning that the system is not symmetrical. On the other hand, the magnitude and phase graphs of Z_{21} and Z_{12} are superposed. This reveals the facts that the system respect reciprocity (i.e., Z_{21} is strictly equal to Z_{12}). Therefore, the two-port and three equivalent impedance model can be built given in Figure 89 (b).

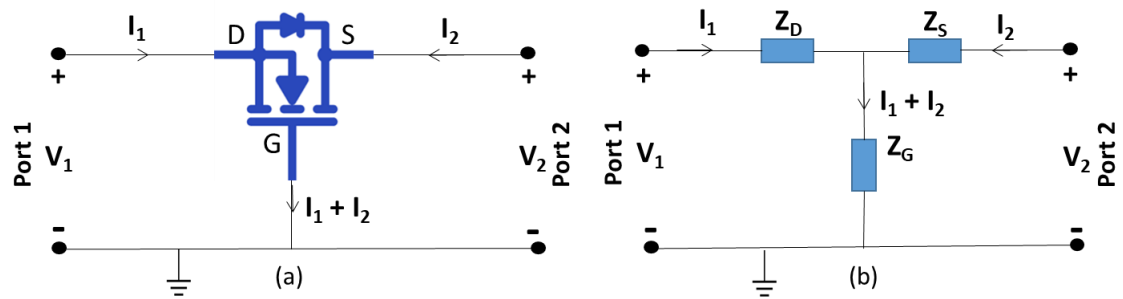


Figure 89: Two-port equivalent model representation (a) device model (b) three impedance model

Figure 89 presents the general equivalent two-port T-network considering config1 (D-G as port 1 and S-G as port 2) like presented in [97]. Under zero DC biasing, the small signal equivalent circuit is represented as shown in Figure 90 with all parasitic resistors, inductors, and capacitors.

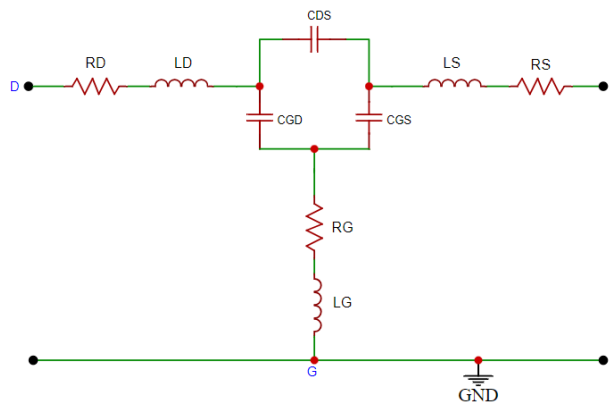


Figure 90: Two-port small signal equivalent circuit under zero DC biasing

The parasitic elements are identified following the assumptions. For example, from impedance plot shown in Figure 88, for the frequency below self-resonating frequency ($f_{low} < SRF$) the plot is dominated by capacitive components. Therefore, in such case the inductor and resistor elements are neglected and Figure 90 can be simplified to Figure 91 (a) which is then converted to star connection (Figure 91 (b)).

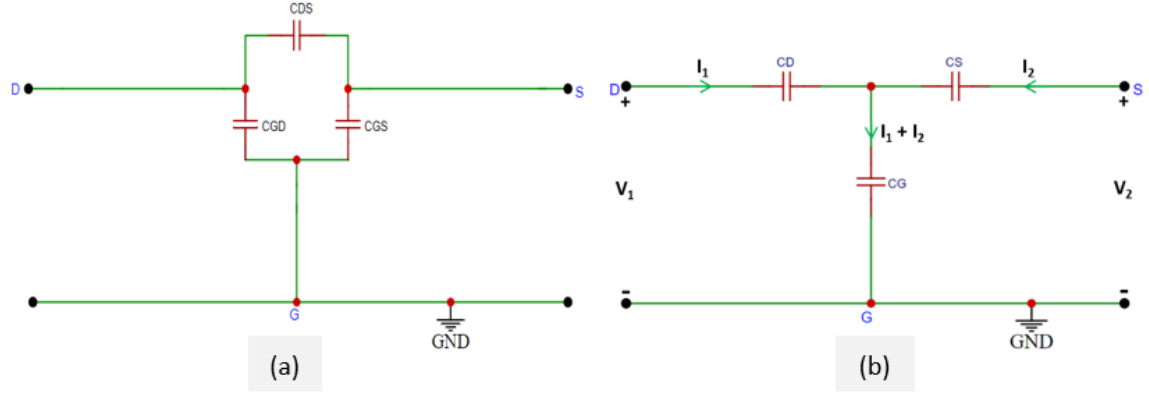


Figure 91: Simplified two-port network at low frequency for capacitance extraction (a) Delta and (b) Star connection

The complex capacitance in Delta connection is converted into Star connection following Eq. 54, Eq. 55, and Eq. 56 [97].

$$X_{C_G} = \frac{X_{C_{GS}} * X_{C_{GD}}}{X_{C_{GS}} + X_{C_{GD}} + X_{C_{DS}}} \quad \text{Eq. 54}$$

$$X_{C_D} = \frac{X_{C_{DS}} * X_{C_{GD}}}{X_{C_{GS}} + X_{C_{GD}} + X_{C_{DS}}} \quad \text{Eq. 55}$$

$$X_{C_S} = \frac{X_{C_{DS}} * X_{C_{GS}}}{X_{C_{GS}} + X_{C_{GD}} + X_{C_{DS}}} \quad \text{Eq. 56}$$

Where, X_{C_i} (i being G, S, and D) is capacitive reactance and is expressed as $\frac{1}{j*\omega*C_i}$ in ohms.

ω is the angular frequency and indeed expressed as $2 * \pi * f$.

Therefore, the capacitance contribution at low frequency (in the following at 1 MHz) for the two-port network, Z-parameters are defined [97] as follows referring to the Figure 91 (b):

$$Z_{11(low)} = \frac{V_1}{I_1} |_{I_2=0} = X_{C_D} + X_{C_G} \quad \text{Eq. 57}$$

$$Z_{21(low)} = \frac{V_2}{I_1} |_{I_2=0} = X_{C_G} \quad \text{Eq. 58}$$

$$Z_{12(low)} = \frac{V_1}{I_2} |_{I_1=0} = X_{C_G} \quad \text{Eq. 59}$$

$$Z_{22(low)} = \frac{V_2}{I_2} |_{I_1=0} = X_{C_S} + X_{C_G} \quad \text{Eq. 60}$$

Having respected reciprocity, either considering Eq. 58 or Eq. 59 and following the extraction process explained in Section 2.7, capacitance C_G can be extracted given in Eq. 61. Likewise, Eq. 57 and Eq. 60 gives combined equivalent capacitances presented in Eq. 62 and Eq. 63. To point out, the wording “low” and “high” added to impedances and frequencies into the following the equations represent the region below and above SRF, respectively. For example, f_{low} is the frequency below SRF and $Z_{12(low)}$ is the impedance value taken at f_{low} from Z_{12} graph. The impedance value used are in ohms.

$$C_G = \frac{1}{2 * \pi * f_{low} * |Z_{12(low)}|} \quad Eq. 61$$

$$\frac{C_D * C_G}{C_D + C_G} = \frac{1}{2 * \pi * f_{low} * |Z_{11(low)}|} \quad Eq. 62$$

$$\frac{C_S * C_G}{C_S + C_G} = \frac{1}{2 * \pi * f_{low} * |Z_{22(low)}|} \quad Eq. 63$$

The capacitances C_D and C_S can be computed by substituting C_G value in Eq. 62 and Eq. 63. Using C_D , C_G , and C_S values and solving Eq. 54, Eq. 55, and Eq. 56 the capacitances between the terminals C_{DG} , C_{GS} , and C_{DS} can be extracted.

Likewise, at self-resonating frequency (i.e., SRF) the model is simplified to Figure 92 (a). Following the resistance extraction process explained in Chapter 2, resistances R_G , and R_D , and R_S are computed from Eq. 64 to Eq. 66.

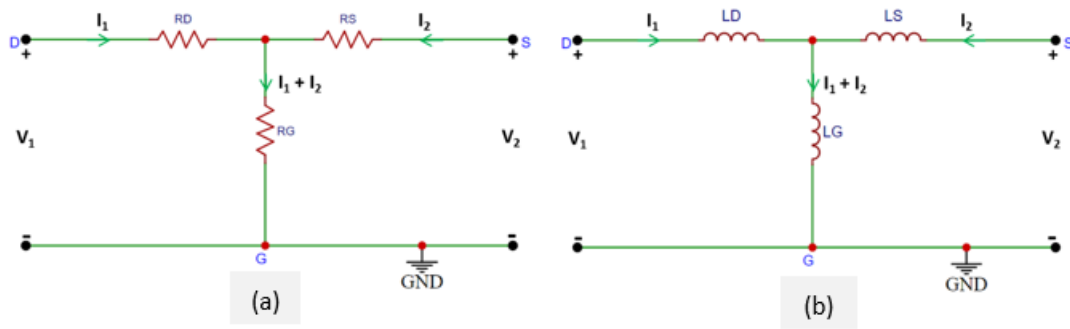


Figure 92: Simplified two-port network for (a) resistance extraction (b) Inductance extraction

$$R_G = 10 \left(\frac{|Z_{12(low)}|}{20} \right) \quad Eq. 64$$

$$R_D + R_G = 10 \left(\frac{|Z_{11(low)}|}{20} \right) \quad Eq. 65$$

$$R_S + R_G = 10^{\left(\frac{|Z_{22}(low)|}{20}\right)} \quad Eq. 66$$

The terminal inductances L_G , L_D , and L_S are extracted using the self-resonating frequency expression given in Eq. 67, Eq. 68, and Eq. 69, respectively. To point out, SRF used in Eq. 67, Eq. 68, and Eq. 69 is the self-resonating frequency taken from Z_{12} , Z_{11} , and Z_{22} impedance plots respectively.

$$L_G = \frac{1}{(2 * \pi * f_{SRF})^2 * C_G} \quad Eq. 67$$

$$L_D + L_G = \frac{1}{(2 * \pi * f_{SRF})^2 * \frac{C_D * C_G}{C_D + C_G}} \quad Eq. 68$$

$$L_S + L_G = \frac{1}{(2 * \pi * f_{SRF})^2 * \frac{C_S * C_G}{C_S + C_G}} \quad Eq. 69$$

All the parasitic elements that are extracted following NDT methodology for a discrete power device (C2M0160120D) are listed in the following Table 11.

Parameters	NDT methodology @ 1 V	Datasheet (CV curves) @ 1 V	B1505A (Curve tracer) @ 1 V
C_{GS} (pF)	552.33 @1 MHz	580 @1 MHz	547.36 @100 kHz
C_{DS} (pF)	530.58 @1 MHz	490 @1 MHz	433.1 @100 kHz
C_{GD} (pF)	229.21 @1 MHz	220 @1 MHz	233.53 @100 kHz
L_G (nH)	7.2	-	-
L_D (nH)	1.87	-	-
L_S (nH)	5.14	-	-
R_G (Ω)	2.64	-	-
R_D (Ω)	0.013	-	-
R_S (Ω)	0.4	-	-

Table 11: Parasitic elements extraction comparison

Let us remark that the Table 11 compares the capacitances extracted from the NDT methodology and those taken from the datasheet at 1 MHz. The capacitances extracted from methodology are verified by comparing with datasheet values and Keysight B1505A

power device Analyzer/Curve tracer. B1505A curve tracer can accurately evaluate and characterize the power devices [106]. The usual techniques performed by this power device analyzer are electrical I-V characterization for wide-bandgap semiconductor devices and capacitance (CV) measurements at high voltages bias (3 kV). The details about the CV and I-V-measurements from B1505A are presented in Chapter 6 and Chapter 7 of [106]. Appendix 4-10 presents the CV-measurement setup of B1505A. The capacitances extracted from NDT methodology are in good agreement with the datasheet and CV measurements. Following the NDT methodology all the parasitic elements can be extracted as listed in Table 11. On the one hand, datasheet hardly provides any information about inductance and resistance and B1505A curve tracer measures only capacitance. Let us point out that the proposed NDT methodology brings added value compared to datasheet information and B1505A characterization. On the other hand, the datasheet provides information about R_{DSon} and it can be computed from I-V characteristics of B1505A. Following the methodology, the resistance computed under zero DC biasing is the equivalent resistance.

The extracted parasitic elements are plugged into a two-port LTspice model shown in Figure 93. Thereby the LTspice simulation is compared with the experimental measurements given in Figure 94.

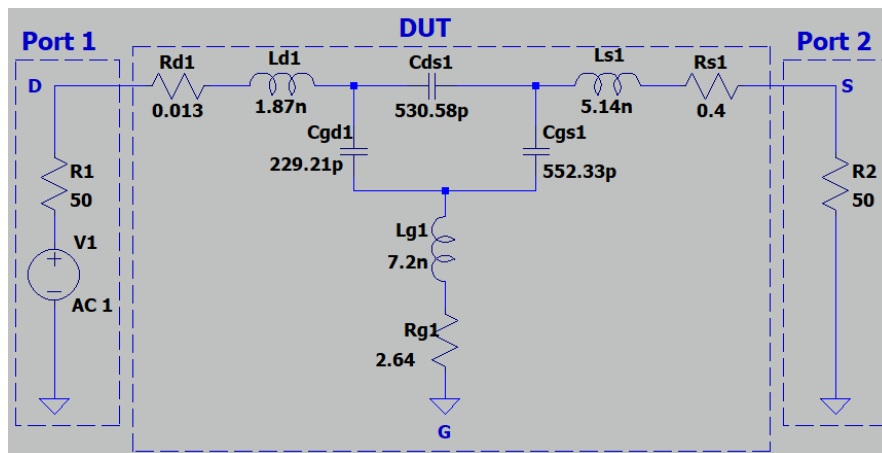


Figure 93: LTspice two-port electrical equivalent circuit with RLC extracted values of C2M0160120D

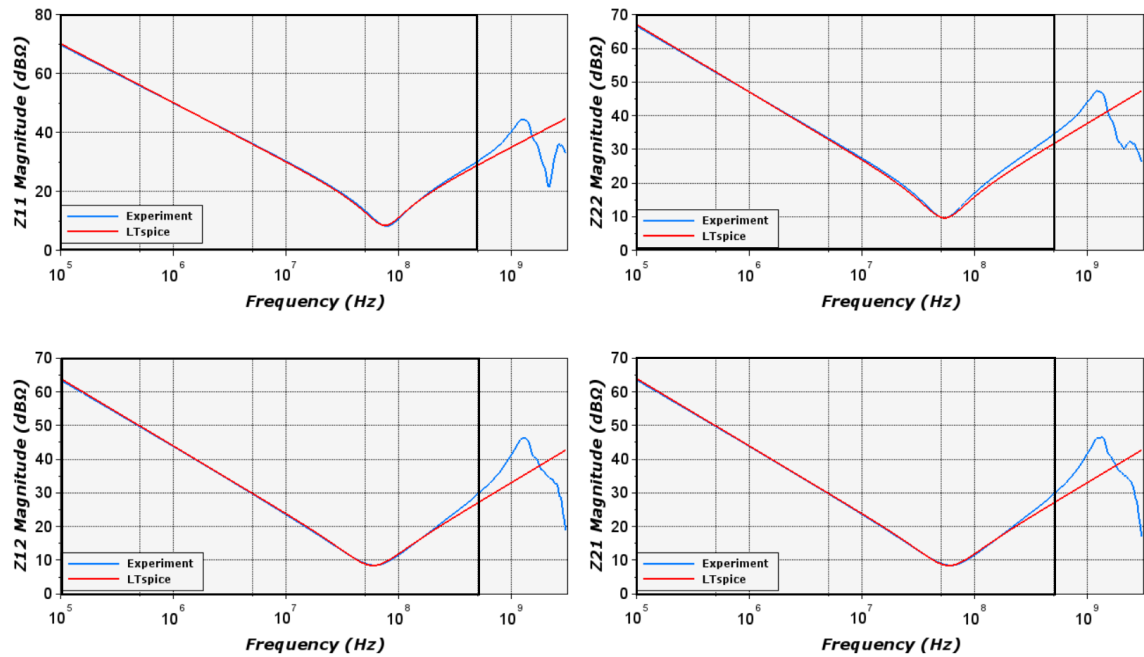


Figure 94: Experimental and simulation Z-parameters magnitude comparison of vertically placed TO-247 SiC MOSFET (C2M0160120D)

Figure 94 presents the four Z-parameters (magnitude), which compare the experimental and simulation curves of TO-247 SiC MOSFET (C2M0160120D). The results (Figure 94) agree from 100 kHz to 500 MHz with a difference of less than 3 dB. Likewise, Figure 95 presents the experimental and simulation comparison of Z-parameters phase.

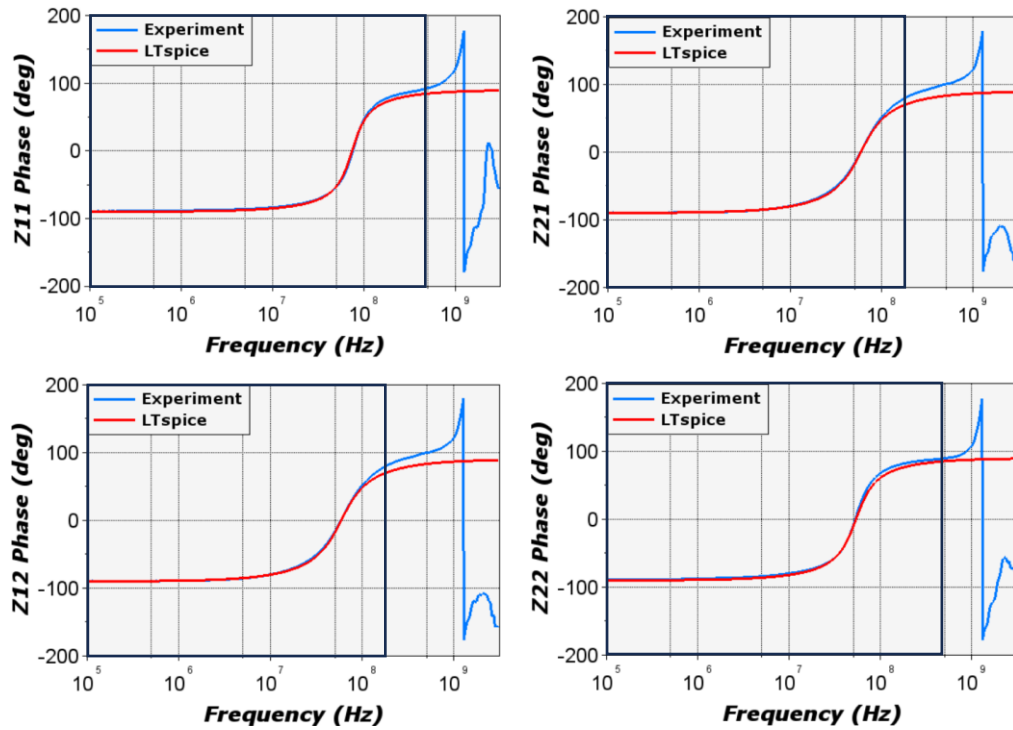


Figure 95: Experimental and simulation Z-parameters phase comparison of vertically placed TO-247 SiC MOSFET (C2M0160120D)

The results (Figure 95) are in good agreements with any difference less than 3 deg from 100 kHz to 500 MHz for Z_{11} and Z_{22} and from 100 kHz to 200 MHz for Z_{21} and Z_{12} .

The electrical schema presented in Figure 93 can be updated by adding the SMA connectors to represent the interface (Figure 85) used to perform the two-port characterization. The updated schema and its comparison with the experimental curves are presented in Figure 96. The results are in good agreement from 100 kHz to 1 GHz with differences less than 3 dB. Besides, they also recover the resonances at high frequencies. It is interesting to highlight, the results are improved in the range of frequency from the previous case.

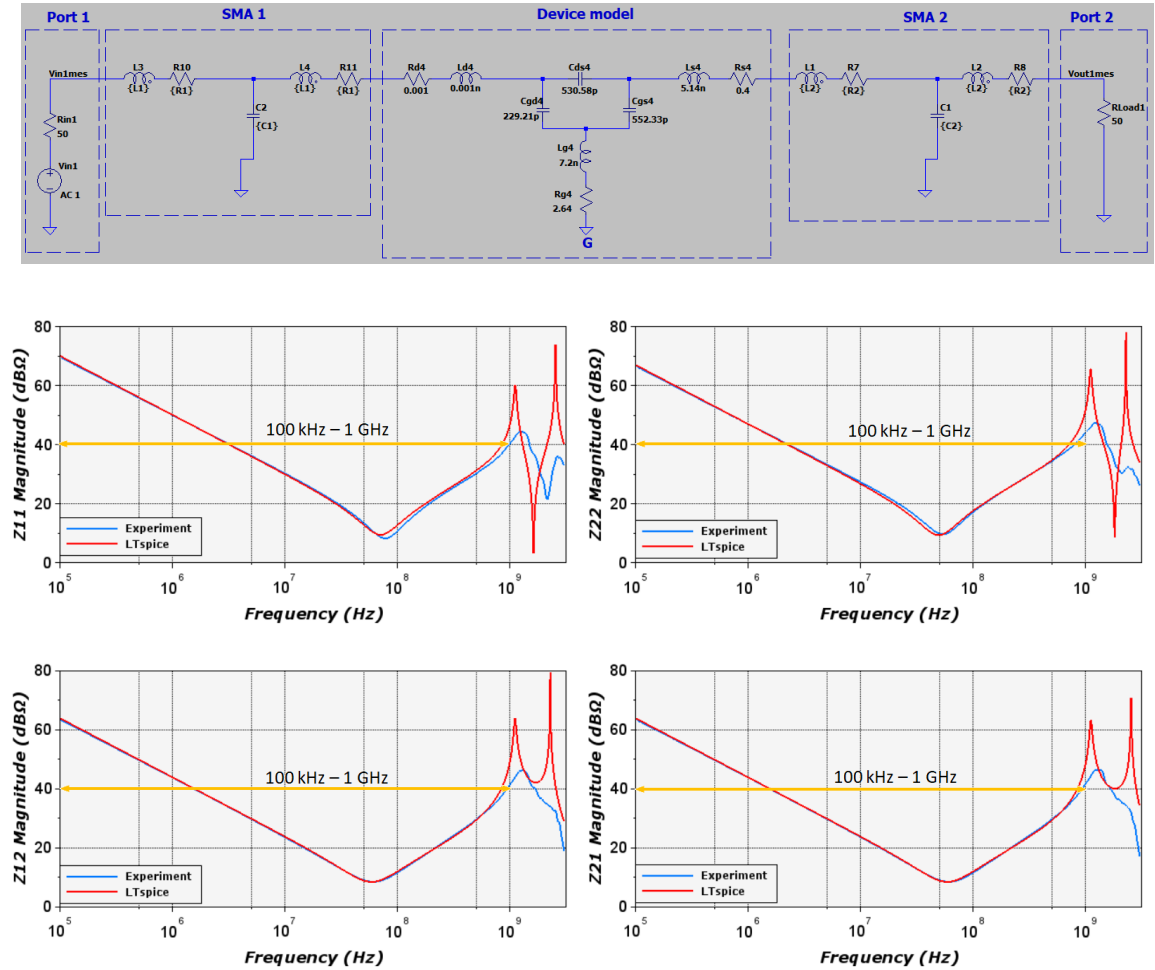


Figure 96: TO-247 SiC MOSFET (C2M0160120D) LTSpice model (including SMA model) and its comparison with experimental data

Likewise, this methodology is applied to different TO packages. The experimental and LTSpice simulation of three of these TO packages are presented in Appendix 4-11, Appendix 4-12, and Appendix 4-13. To point out, having added the SMA model to device model (Figure 93) recovers the resonance at high frequencies. However, to match the experimental curves the updated model still needs to be improved.

3.2.2 Improvement in measurement protocol of discrete power device

This section details the improvement made in measurement protocol. The improvement is mainly made on the interface used to perform the two-port characterization of discrete power devices. Like presented in the Figure 85, the TO package is placed vertically on to the epoxy interface by maintaining minimum length of device terminals (Appendix 4-14). It is due to the fact that having more than 1 cm of device terminal in air adds external

inductance. Though this measurement protocol is effective by providing interesting results as discussed but it suffers from certain factors:

- Firstly, having different configurations (Table 10) possible to perform two-port characterization, three interfaces (one per configuration following Table 10) need to be prepared for the characterization.
- Characterizing the same power device requires three different configurations (Table 10), each of which entails three soldering and unsoldering operations. Consequently, assuming the integrity of the power device and its interface cannot be taken for granted. Moreover, the soldering/unsoldering operations consumes a significant amount of time.
- Appendix 4-10 illustrates the capacitance characterization using B1505A curve tracer. Considering Figure 85, it implies that the device must be characterized for CV measurements priory to eliminate the extra length of terminals for VNA measurement.

Therefore, to overcome these uncertainties the interface has been updated as illustrated in Figure 97. Figure 97 is designed for TO-247 dimensions. The interface is made of three 50Ω adapted access pad tracks on which the three terminals of the power device are placed and connected to three respective SMA connectors. A supporting box is fixed: it covers the maximum length of the device terminals and ensure the electrical connection onto the line length. The supporting box is made of Polylactic acid (PLA) and its dimensions are provided in Appendix 4-15. At the beginning of the characterization process, the power device terminals connections to the access pad tracks are checked by a DC meter measurement.

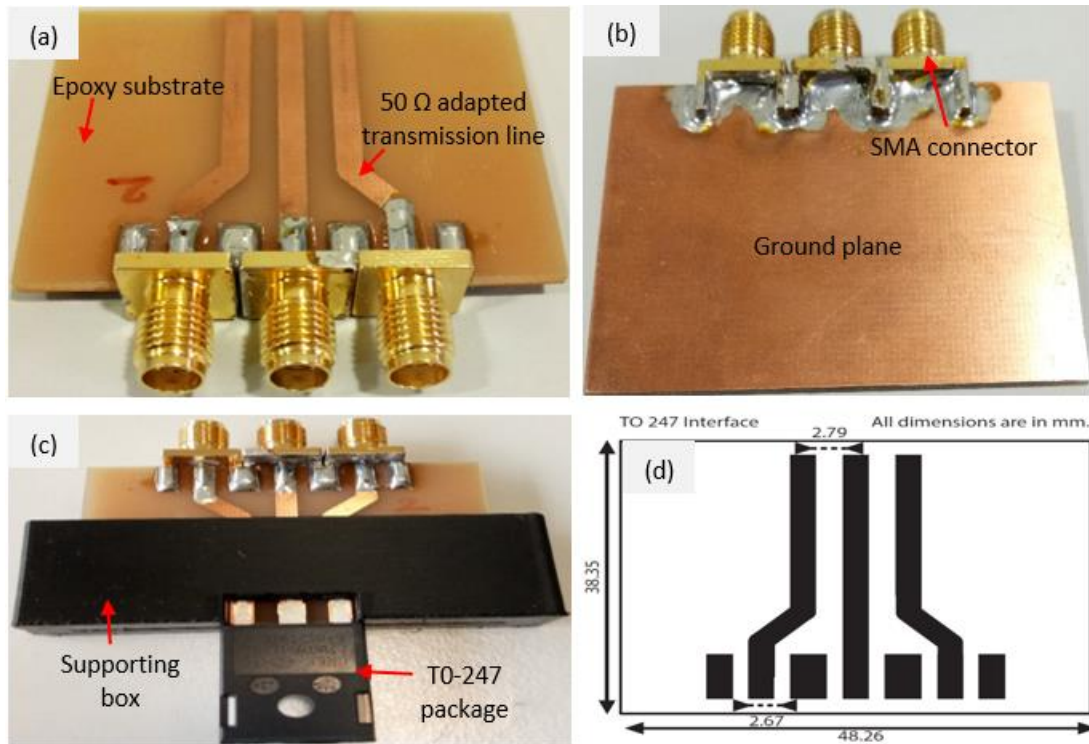


Figure 97: Epoxy interface of TO-247 package horizontally placed (a) top view, (b) bottom view, (c) interface with device, and (d) interface footprint

The two-port characterization is performed by connecting two terminals to port 1 and port 2 respectively, and the third terminal is short circuited. To be clear, for example considering config1 (refer Table 10), drain and source terminals are connected to port 1 and port 2 respectively while gate terminal is connected with a short circuit load. The measurement setup and port connection visuals are provided in Appendix 4-16. Likewise, the interface to support TO-220 dimensions is presented in Appendix 4-17.

The NDT methodology is again applied to TO-247 SiC MOSFET (C2M0160120D) now using the optimized interface given in Figure 97. From Figure 98, the results are in good agreement from 100 kHz to 200 MHz with any difference of less than 2 dB in this bandwidth.

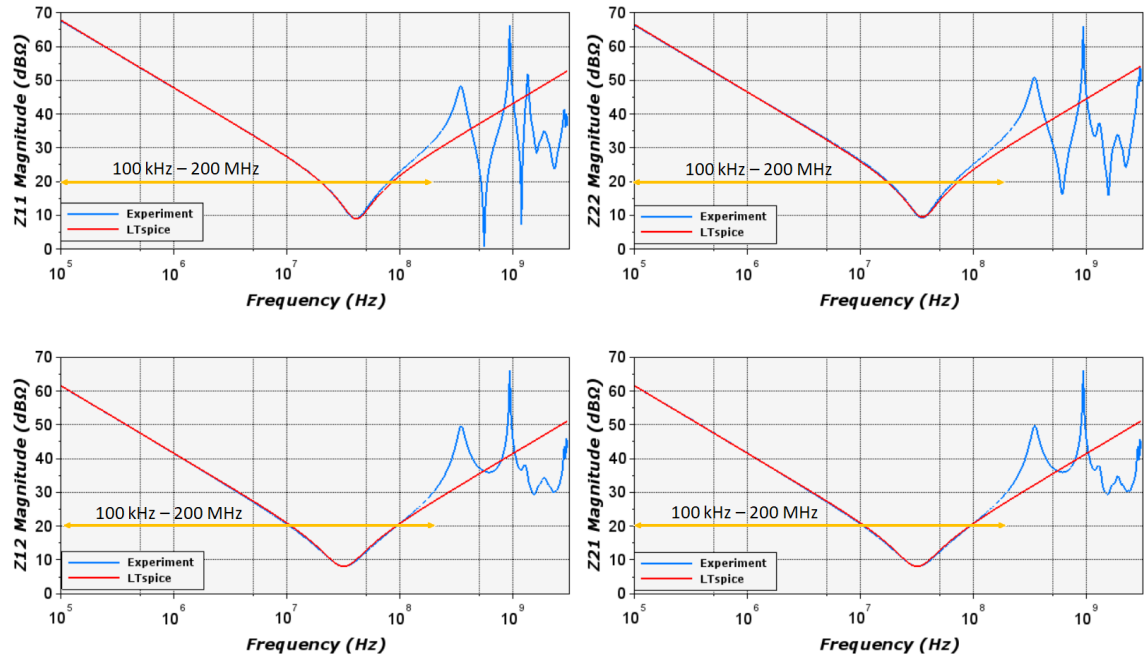


Figure 98: Experimental and simulation comparison of horizontally placed TO-247 SiC MOSFET (C2M0160120D)

The electrical equivalent model is further updated by adding three SMA connectors. Two SMAs are used for two-port connection and the third SMA is grounded using short circuit load. The connection to the ports and grounding are based on configurations given in Table 10. The updated model and its results are presented in Figure 99. The RLC values used for the SMA1, SMA2, and SMA3 are similar and are the average values of SMA model (mentioned in Table 9). The experimental and simulation curves are in good agreement from 100 kHz to 200 MHz with any difference less than 2 dB. In addition, the updated model recovers the resonances at high frequencies. To enhance the simulation model, can imagine to formulate certain hypothesis as follows:

- The interface can be characterized and extract RLCG values when no device is connected
- Thereby an electrical equivalent circuit representing the interface can be built
- To improve the accuracy of model, the transmission lines can be split into number of cells (as described in Chapter 2 for the modelling of microstrip line)
- Finally, the device model can be added and common elements can be deduced

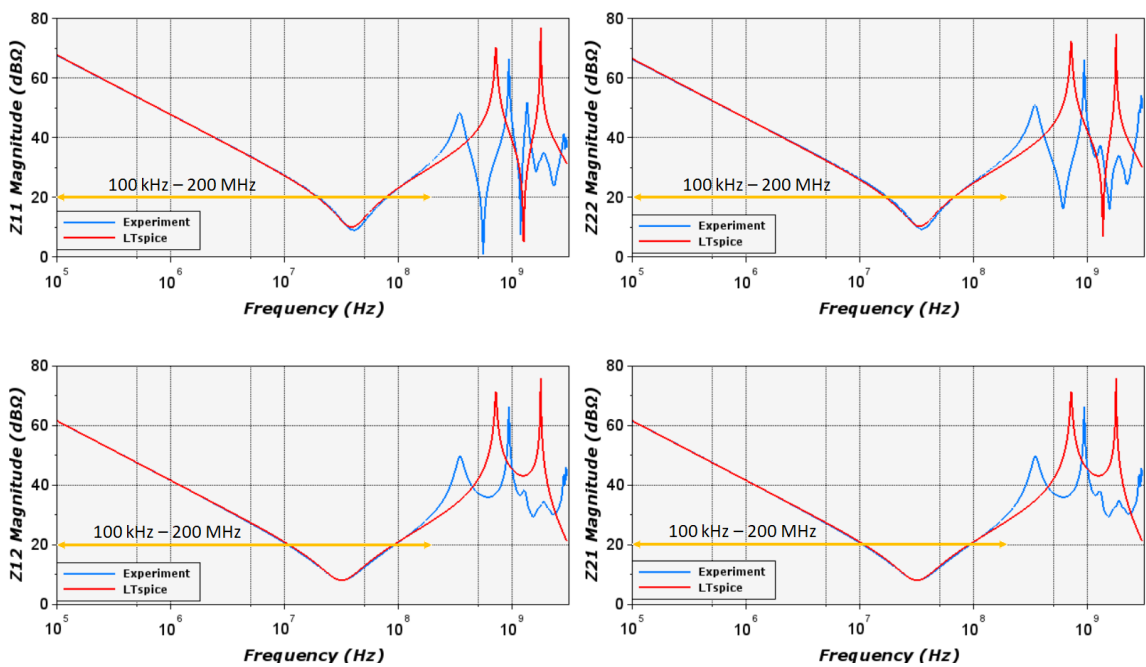
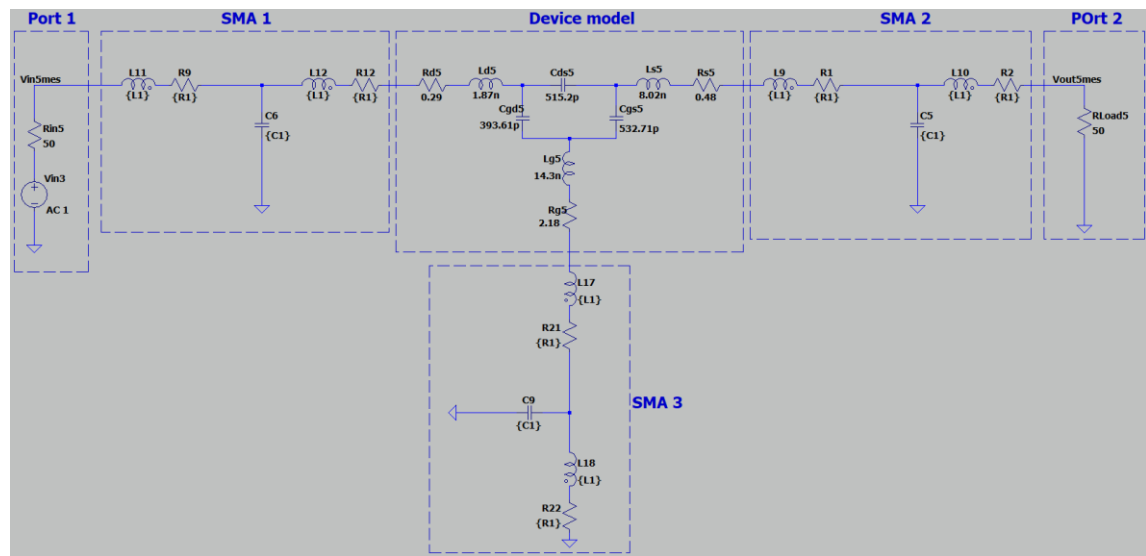


Figure 99: Epoxy interface horizontally placed device (TO-247 SiC MOSFET (C2M0160120D)) LTspice model including SMA and its comparison with experimental data

3.3 Application of NDT methodology to a ceramic substrate

This section demonstrates the application of NDT methodology to a homemade package. Firstly, it provides the details about the homemade packaging. Secondly, to understand the behavior of prototype in healthy state by applying NDT methodology. An initial study has been made on an isolated prototype made of epoxy. The two copper tracks were connected with several wire bonding.

Based on that study, our prototype is a Silicon nitride (Si_3N_4) ceramic substrate, which is sometimes used as ceramic substrate in highly constrained power assemblies. More precisely, this ceramic substrate specified in previous study for an aeronautical application [107]. The prototypes base on such a ceramic are denoted for this thesis as “homemade packaging”. Therefore, the detailed description about the homemade packaging and the improvements made for an accurate characterization, are presented in Section 3.3.1.. This substrate is chosen due to several reasons as follows:

- They can support the objective of this thesis
- They are readily available and in bulk
- Silicon nitride is a high-performance ceramic known for its excellent mechanical, thermal, and electrical properties. These properties make it suitable for a wide range of applications, particularly in high-temperature and high-stress environments. Therefore, this thesis aims to perform reliability study on such substrate to investigate different failure mechanisms.

3.3.1 Homemade packaging details

The homemade packaging is based on Active Metal Brazing (AMB), Silicon nitride (Si_3N_4) ceramic substrate as usually done in power electronics modules shown in Figure 100. The copper tracks are brazed onto the ceramic substrate using AMB technique which provides excellent mechanical properties and high temperature resistance. The metallization presented in Figure 100 are made of copper and covered with a thin layer of passivation gold. The thickness of ceramic substrate and metallization is 330 μm and 225 μm respectively. The dimensions of the ceramic substrate are presented in Appendix 4-18. On the top side of the substrate, 4 copper tracks numbered Track 0 to Track 2b as illustrated in Figure 100. The tracks allow the brazing of semiconductor dies, the soldering of the interconnections like bonding wires or clips. The underside features a large copper surface to dissipate the excess heat generated during switching operation. Usually, it is connected to the thermal dissipator.

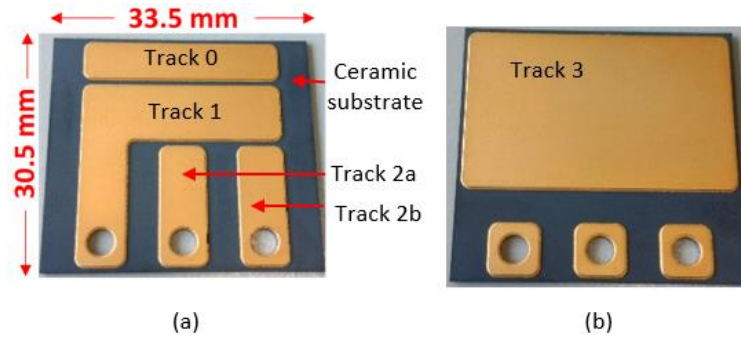


Figure 100: Active Metal Brazing ceramic substrate (a) top view (b) bottom view

To support two-port VNA characterization of a ceramic substrate a specific interface made of epoxy has been developed shown in Figure 101 (a). This interface was designed for being 50 ohms adapted and using non-electromagnetic materials for mechanical supports. The dimensions of the interface are precisely detailed in Appendix 4-19.

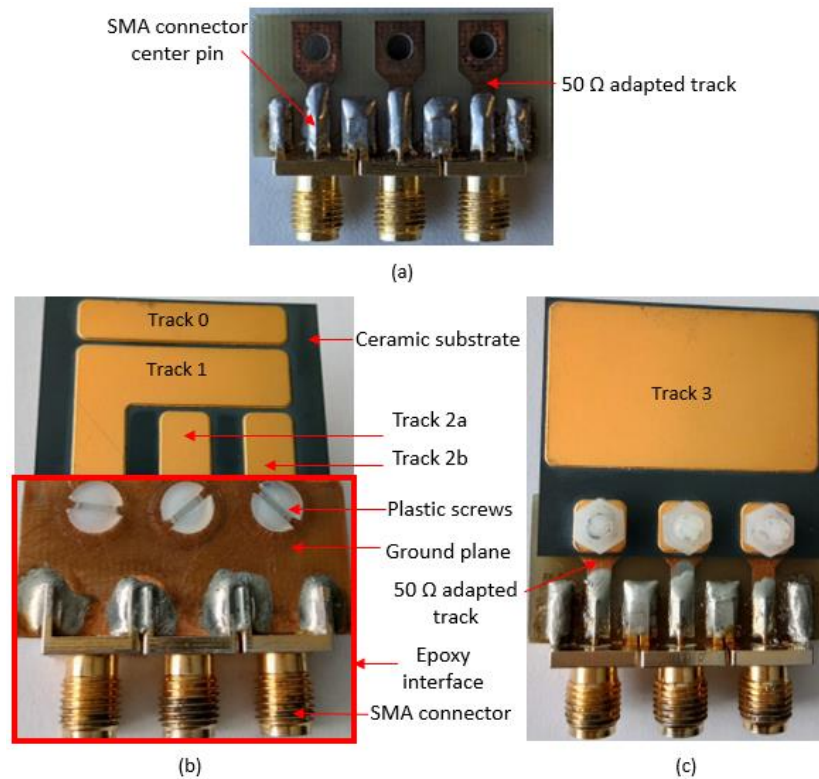


Figure 101: (a) Epoxy interface and ceramic substrate with epoxy interface in measurement condition, top view (b), bottom view (c)

The interface contains 3 SMA connectors whose center pin (measurement pin) is connected to 50 Ω adapted tracks. The top plane of the interface and the outer part of the SMA are grounded together. In measurement condition, the ceramic substrate is connected

to the epoxy interface using plastic screws depicted in Figure 101 (b). This connection achieves the electrical connection between the interface and ceramic substrate by connecting the 50 Ω adapted tracks to its respective homemade prototype tracks (Track 1, Track 2a, and Track 2b) shown in Figure 101 (c).

Therefore, the 3 tracks denoted Track 1, Track 2a and Track 2b are connected to three SMA connectors, through the epoxy interface. Thereby, to perform a two-port characterization there exists several possible configurations detailed in the Table 12.

Parameters	Track 1	Track 2a	Track 2b
config1	Port 1	Port 2	Short or 50 Ω load
config2	Port 1	Short or 50 Ω load	Port 2
config3	Short or 50 Ω load	Port 1	Port 2

Table 12: Measurement configurations of ceramic substrate

It is noticed that Track 1, Track 2a, and Track 2b are used to perform two-port characterization while Track 0 and Track 3 are not used. To prevent any undesired electromagnetic coupling with the unused tracks, Track 0 and Track 3 are grounded as shown in Figure 102. At first, the Track 3 was connected to the outer part of SMA connectors through additional grounding wires as illustrated in Figure 102 (a). Then, Track 0 is also connected to the Track 3 through two smaller grounding wires as depicted in Figure 102 (b). The use of additional grounding wire will be later discussed.

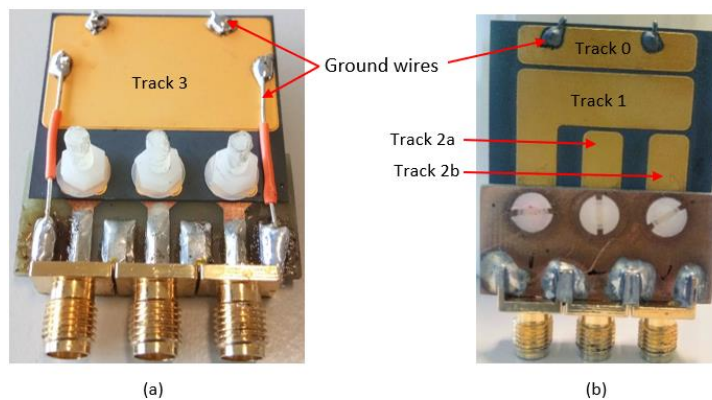


Figure 102: Ceramic substrate with epoxy interface and grounding floating tracks in measurement condition

3.3.2 Ceramic substrate healthy state characterization

This section presents the two-port characterization of the ceramic substrate to study its behavior in healthy state. The measurement setup is detailed in Appendix 4-20. Let us consider config1 from Table 12 meaning that, port 1 and port 2 of VNA are connected to Track 1 and Track 2a, respectively, and Track 2b is grounded. As there is no connection between the two tracks the injected signal demonstrates pronounced reflection (S_{11} & S_{22}) and diminished transmission (S_{21} & S_{12}) as shown in Figure 103.

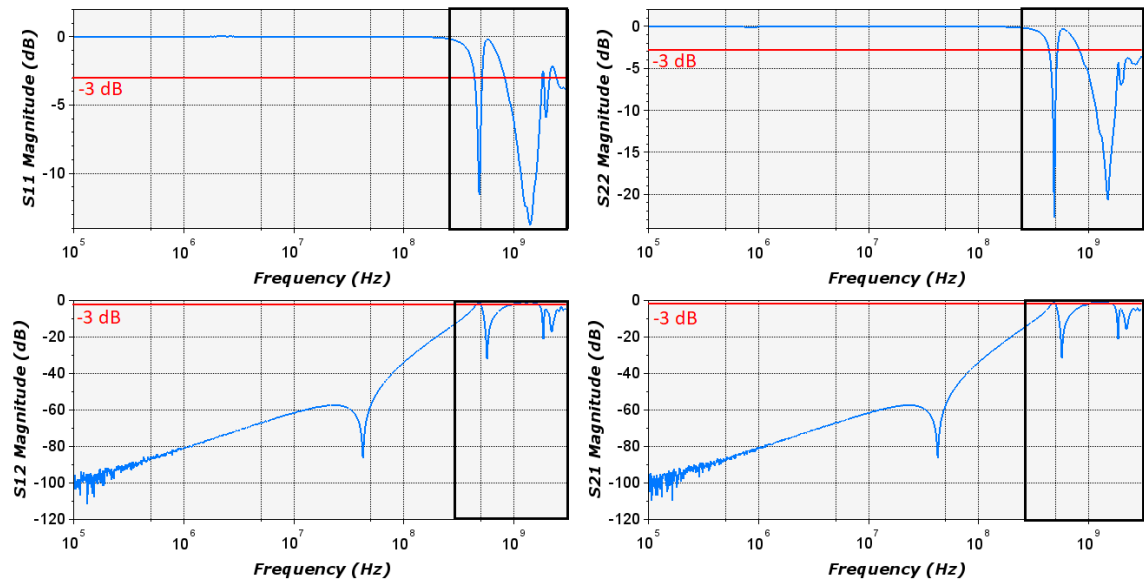


Figure 103: S-parameters magnitude of two-port healthy state characterization of ceramic substrate

From 100 kHz to 440 MHz, considering -3 dB reference the injected signal is highly reflected. A low transmission is noticed. Above 440 MHz (highlighted with black box), the substrate exhibit changes in behavior which can be due to other elements of the prototype. Track 2a and Track 2b have same dimensions as shown in Figure 100. Therefore, config1 and config2 exhibit almost similar behavior with a shift in first resonance and above depicted in Figure 104. The difference can be due to the track length of Track 1 involved in measuring config1 and config2. On the other hand, config3 (i.e., measurement between Track 2a and Track 2b while Track 1 is grounded) measures different behavior compared to config 1 and config2 shown in Figure 105. It is due to the fact that, config3 involves different geometry of tracks measurement compared to config1 and config2.

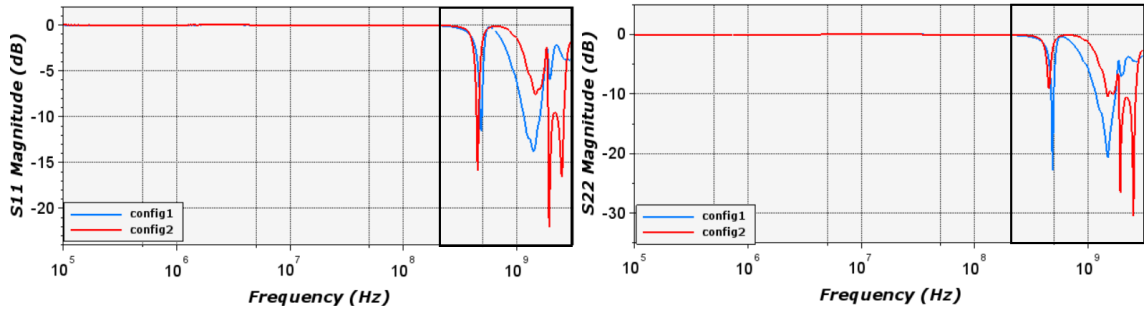


Figure 104: Comparison of config1 and config2 of a healthy state ceramic substrate Reflection coefficients (S_{11} & S_{22})

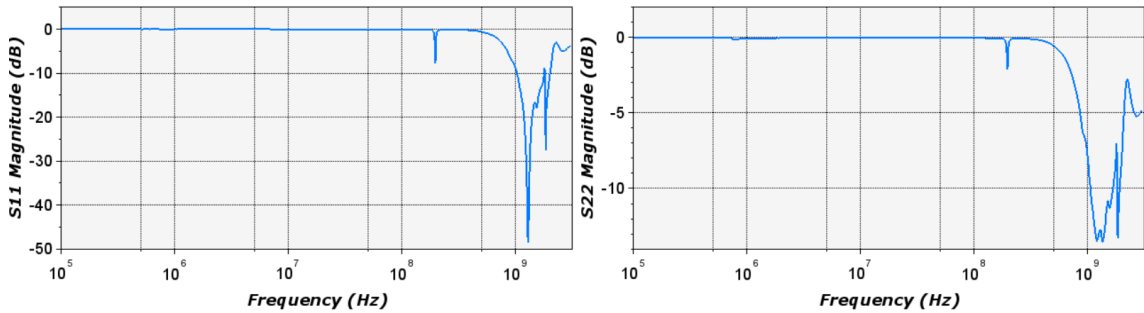


Figure 105: Comparison of config3 of a healthy state ceramic substrate Reflection coefficient (S_{11} & S_{22})

3.3.3 Ceramic substrate with copper tracks connected by bonding wires

Bonding wires play a crucial role in power electronic modules, facilitating electrical connection between various components such as semiconductor chips, substrates, and lead frames. Apart from electrical connections bonding wires also play important role in signal transmission, providing mechanical support to fragile semiconductors from mechanical stresses and vibrations. However, bond-wire failures are the most dominant failures in power electronic components. Therefore, is the interest of this thesis to study its behavior and detection of bond-wire related failures. This section demonstrates the two-port characterization of homemade packaging with copper tracks connected by bonding wires (in healthy state). The bonding wires used during this thesis are made of aluminum. As shown in Figure 106, Track 1 and Track 2b are connected through 4 bonding wires of 300 μm diameter each using wedge bonding technique (ultrasonic energy is used to connect the bond wires as mentioned in Chapter 1). The measurement setup to perform the two-port characterization remains similar. In the following example the config2 is analyzed. In such a case, the healthy state two-port characterization measures high transmission (S_{21} & S_{12}) and low reflection (S_{11} & S_{22}) from 100 kHz to 100 MHz as shown in Figure 107. Some variations are observed above 100 MHz (highlighted with black box).

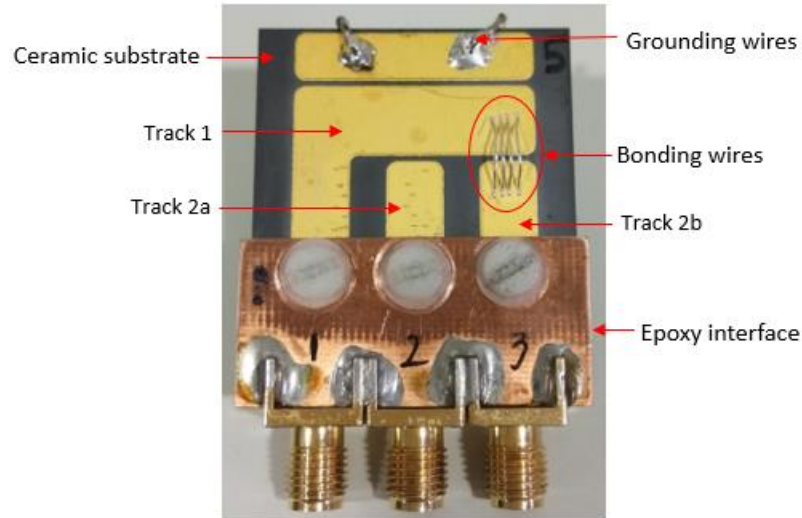


Figure 106: Ceramic substrate with bonding wires connected between two tracks in measurement condition

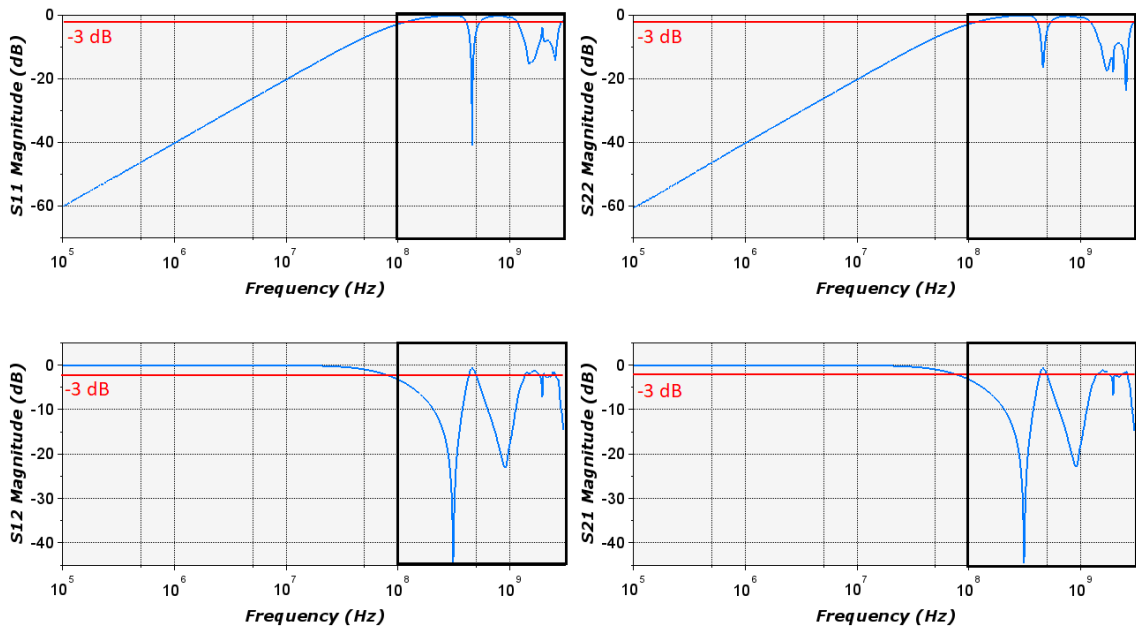


Figure 107: S-parameters magnitude of healthy state two-port characterization following config2

3.3.4 Homemade packaging with IGBT die mounted on a copper track

This section demonstrates the application of NDT methodology to homemade packaging with an IGBT die (1200 V, 25 A, part number: FGH25T120SMD) from Fairchild is brazed on one of the copper tracks. Figure 108 presents the top view of the prototype with the IGBT die mounted on to the Track 2a. The bottom view is similar to the one presented in Figure 102 (a). The technical details of the IGBT die (FGH25T120SMD) is given in [108]. Top side of the die is metallized with emitter and gate pads while the bottom side with

collector. The die is brazed on Track 2a making this track connected to the collector. Track 2b is connected to emitter of the die through 5 bonding wires. The gate pad is connected to Track 1 through 1 bonding wire. The diameter of the bonding wires is 300 μm and are connected using ultrasonic wedge bonding technique.

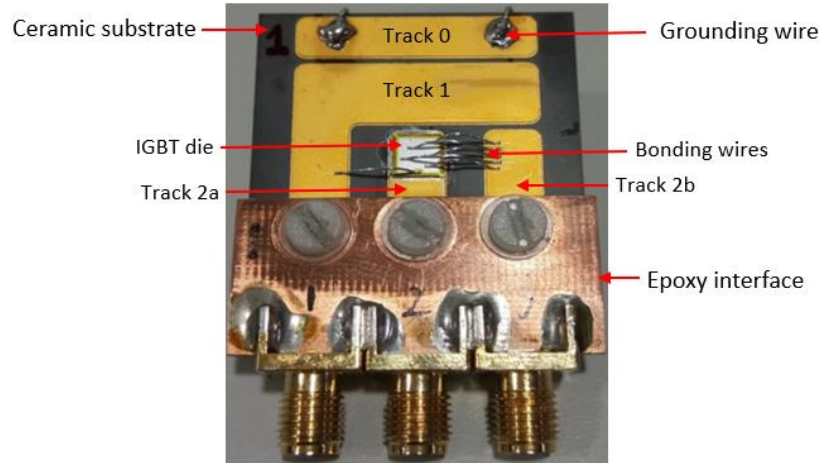


Figure 108: Homemade packaging with IGBT die mounted on Track 2a in measurement condition

Having three terminals (gate, collector, and emitter) of the die connected to Track 1, Track 2a, and Track 2b respectively, implies that there exist the three possible configurations to perform a two-port characterization as detailed in Table 13.

Parameters	Gate	Collector	Emitter
config1	grounded	Port 2	Port 1
config2	Port 2	grounded	Port 1
config3	Port 2	Port 1	grounded

Table 13: Two-port configuration of homemade packaging with IGBT die mounted on Track 2a

In total 5 prototypes, namely Proto1, Proto2, Proto3, Proto4, and Proto5 were developed. They are presented in Appendix 4-21. It is noticed that Proto4 is no longer used nor presented, as it has defects. Therefore, Proto4 is eliminated for further study. Considering the config1 from Table 13, the healthy state two-port characterizations of Proto1 (under zero DC biasing, meaning $V_{GS} = 0 \text{ V}$) are presented in Figure 109.

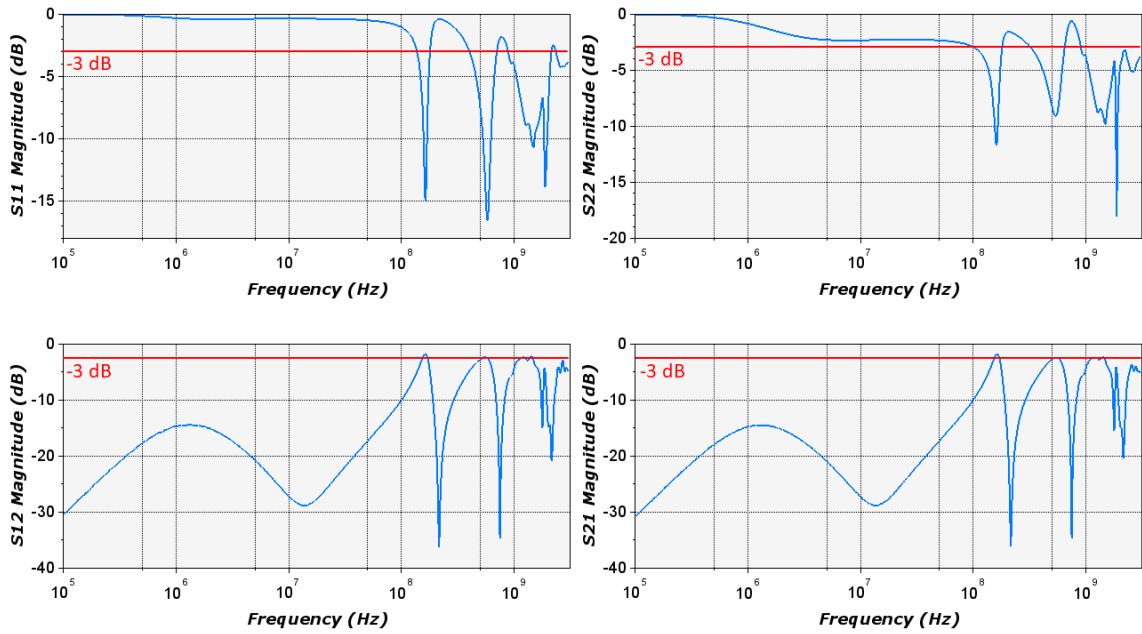


Figure 109: Proto1 S-parameters magnitude healthy state characterization following config1

As the characterization is performed between collector and emitter while the gate is grounded, high reflection and low transmission is expected. It is recovered in the frequency bandwidth (100 kHz to 120 MHz) as demonstrated in Figure 109. Likewise, Figure 110 and Figure 111 present the reflection coefficients magnitude following config2 and config3, respectively.

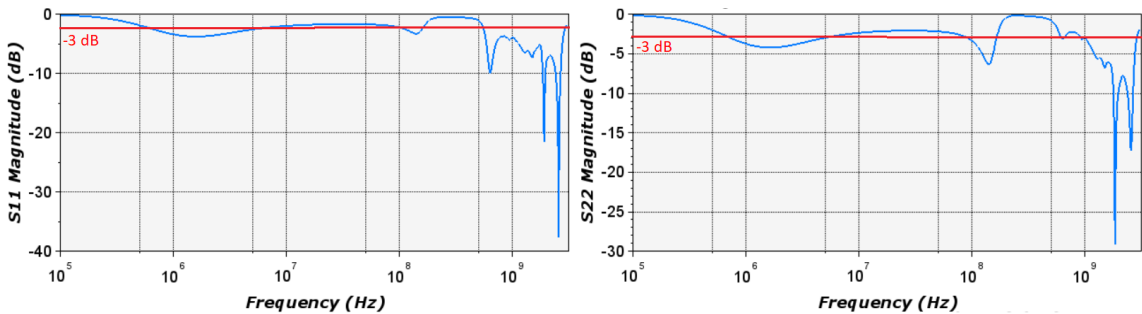


Figure 110: Proto1 Reflection parameters magnitude healthy state characterization following config2

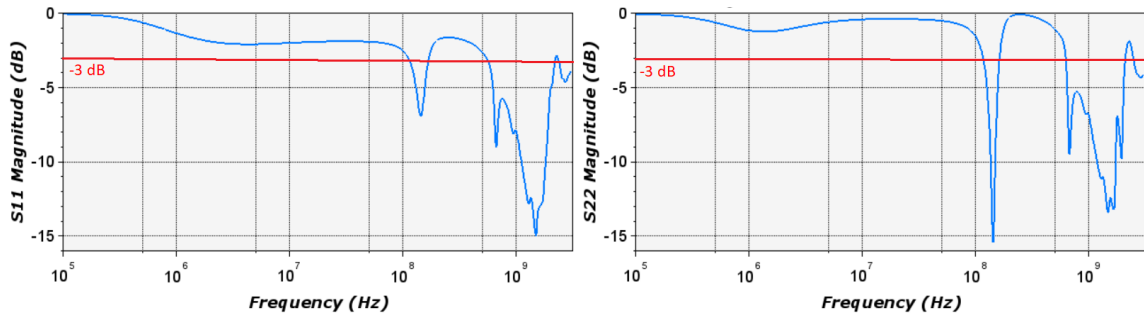


Figure 111: Proto1 Reflection parameters magnitude healthy state characterization following config3

Considering -3 dB reference, config2 recovers reflection from 100 kHz to 500 MHz while config3 recovers from 100 kHz to 100 MHz. In both the configurations (config2 and config3), it doesn't recover full reflection as difference in magnitude is observed in the mentioned bandwidth.

Likewise, two-port characterization performed on Proto2, Proto3, and Proto5 recovered dominant reflection behavior and minimal transmission. Once having S-parameters measured and analyzed for 4 samples (Proto1, Proto2, Proto3, and Proto5) they are converted into Z-parameters using conversion expression. The converted Z-parameters for 4 samples provide RLC behavior. Thereby, following parasitic elements extraction process, RLC elements for respective samples are extracted. In order to compare capacitance values, the CV measurements are performed using B1505A curve tracer for every sample. Let us remark that a specific interface is used to support the homemade packaging to perform CV measurements. The measurement setup, the interface details and description are provided in Appendix 4-22. The average capacitance values extracted from the NDT methodology (at 1 MHz) are compared to the datasheet values (at 1 MHz) and to the CV measurements from B1505A (at 100 kHz). The comparison is done in Figure 112. The indicator denoted "Error1 %" is calculated between datasheet values and averages capacitance values (B1505A and NDT methodology). The values obtained from methodology shows good agreement with data sheet values recording lowest error percentage of 0.28% (C_{oes}) and highest of 21.12% (C_{res}). The indicator denoted "Error2 %" is calculated between average capacitance value of B1505A and NDT methodology. The results present lowest error percentage of 8% (C_{ies}) and highest of 19% (C_{oes}). This difference could be due to the fact that the capacitance is measured at 100 kHz with B1505A curve tracer, while the methodology extracts capacitance at 1 MHz.

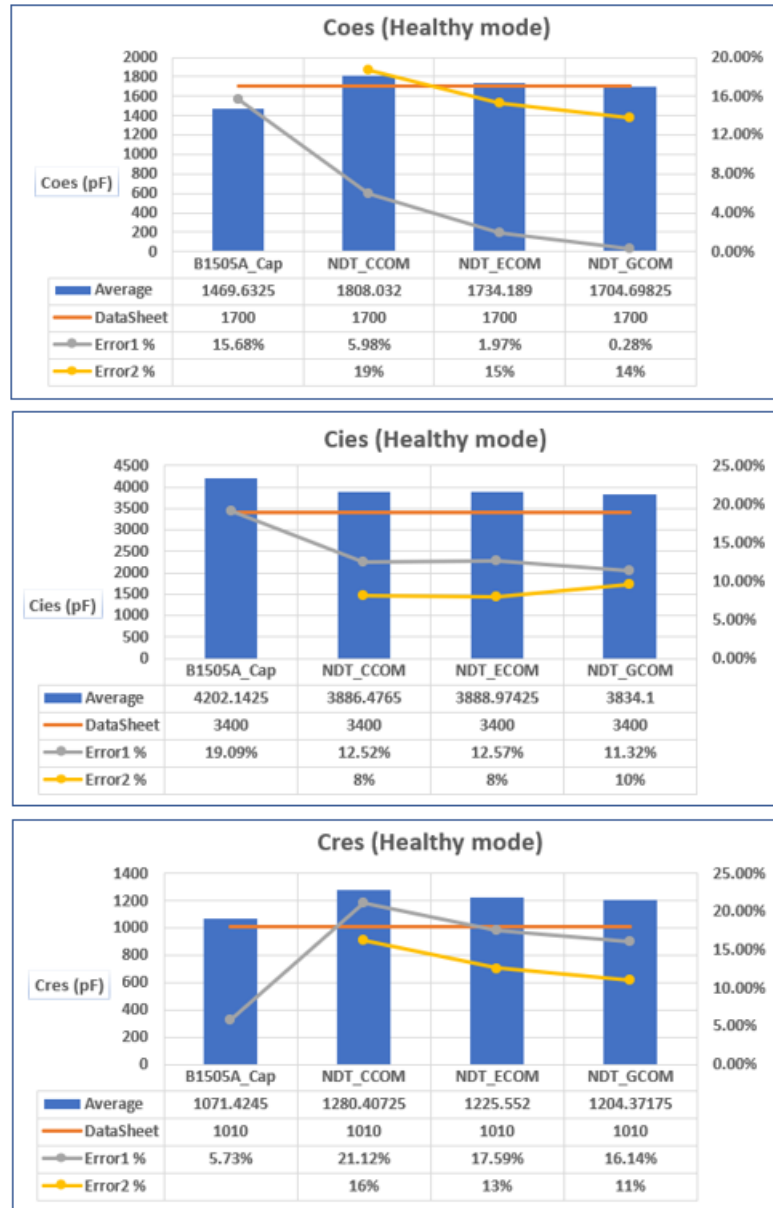


Figure 112: Comparison of capacitances extracted from methodology to the datasheet and CV measurements from B1505A curve tracer

For the electrical equivalent circuit, the device model presented in Figure 93 is adapted and updated with IGBT terminology as presented in Figure 113. The values used here are the average values of RLC extracted from NDT methodology. More precisely, for example, R_{g1} used here is the average of R_g extracted from (Proto1, Proto2, Proto3, and Proto4). Thereby, the LTspice simulation is compared with the experimental data as shown in Figure 114.

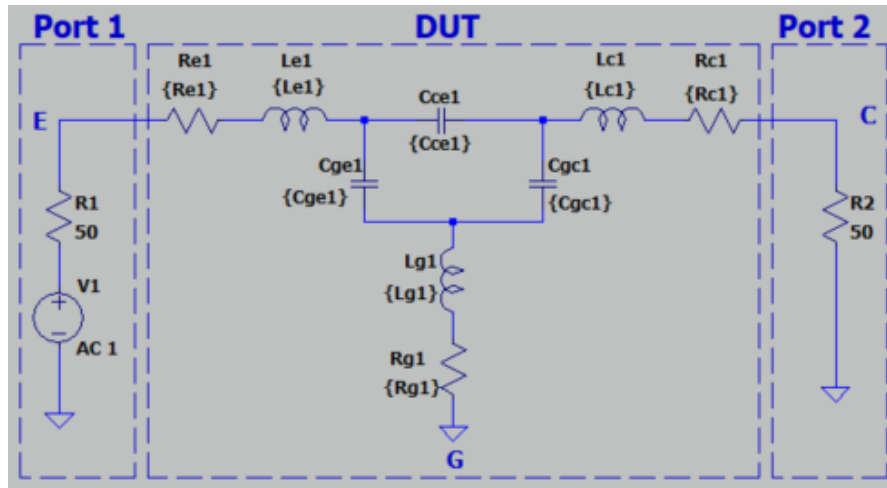


Figure 113: LTspice two-port electrical equivalent circuit (GCOM) with RLC extracted values of IGBT die (FGH25T120SMD)

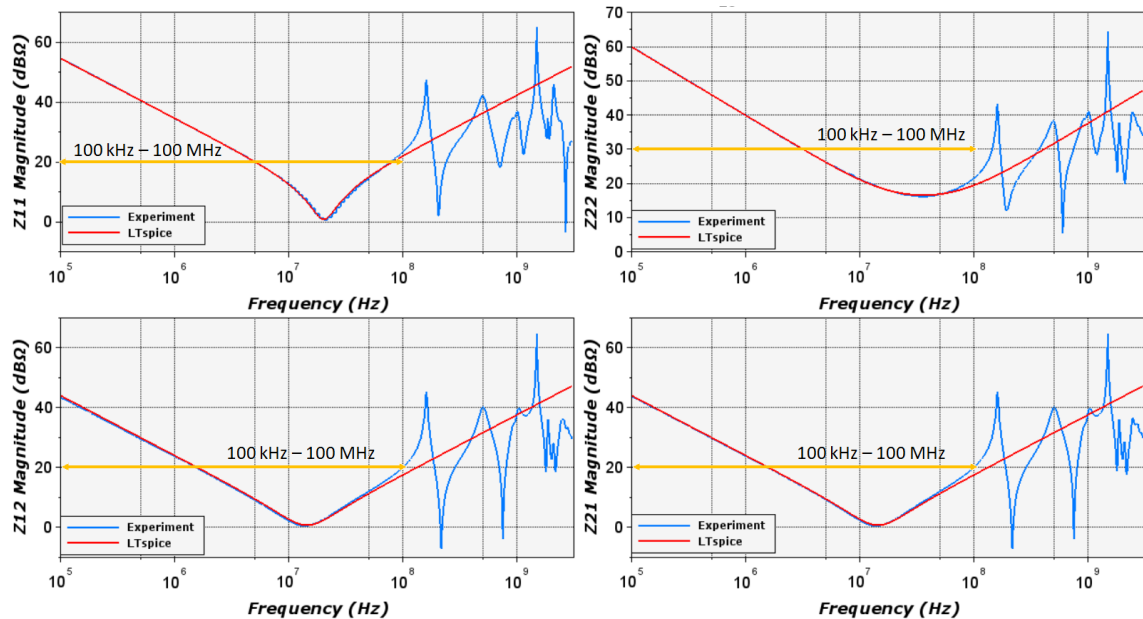


Figure 114: Experimental and LTspice comparison of healthy state homemade packaging with IGBT die following config1

For config2 and config3, the comparison is presented in Appendix 4-23. As presented in Figure 114, the simulation results are in good agreement from 100 kHz to 100 MHz for all possible configurations (listed in Table 13) with <1% of error. It is possible that the impact of die is dominant in this bandwidth (100 kHz – 100 MHz) which is recovered using the device model. The other elements of the prototype can have a significant impact above 100 MHz which are not included in the electrical equivalent model. The other elements include copper tracks, bonding wires, epoxy interface. Therefore, the electrical

equivalent circuit can be improved by considering every element of the DUT involved in measurement.

3.3.5 Characterization of a ceramic substrate with IGBT die and bond wires by polarizing the die

In contrast to RF applications, power electronics transistors necessitate characterization under high voltage and current conditions. To assess the S-parameters of these transistors at various bias voltages, specialized devices known as « Bias Tee » are developed. These devices facilitate the coupling of DC bias signals with high-frequency signals sourced from the VNA [109]. The equivalent circuit of a bias tee device is given in Figure 115.

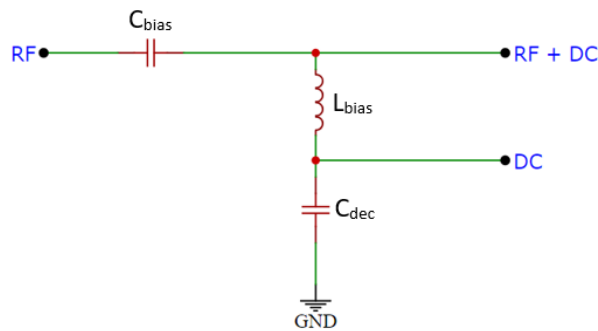


Figure 115: Equivalent circuit of a bias tee

A bias tee is a three-port network made of inductor and capacitor. The C_{bias} capacitor allows high-frequency signals to flow and blocks DC signals. Conversely, the L_{bias} inductor allows the DC signal to circulate, blocking the high frequency part of this signal. Capacitor C_{dec} is used to decouple the DC supply to the tee.

This part of the thesis explains the design of our own bias tee to polarize the DUT. The bias tee design is adapted to our application requirements. The process to design bias tee explained in [110] is followed. One of the most important factors to be considered while designing a bias tee, is the operating bandwidth. In our case, the interested bandwidth is from 100 kHz to 3GHz. However, it is difficult to achieve bias tee design for such a huge bandwidth. Therefore, the bandwidth is compromised to 100 MHz to 1.5 GHz. In order to detect failures that appear close to 1 GHz such as bond wire lift-off. The required passive elements are chosen accordingly. The WE-SD inductor, manufactured by Würth Electronics, was chosen and its details are given in Table 14. Additionally, its equivalent

schematic, sourced from the manufacturer’s data is used. The equivalent impedance is made of parallel parasitic capacitance (C_{Lbias}) and resistance (R_{Lbias}), as depicted in Figure 116.

Parameters	Value	Unit
Inductor	6 ($\pm 25\%$ tolerance)	μH
Rated current	2.5	A
Self-Resonant Frequency	140	MHz

Table 14: Specifications of the Inductor from Würth Electronics

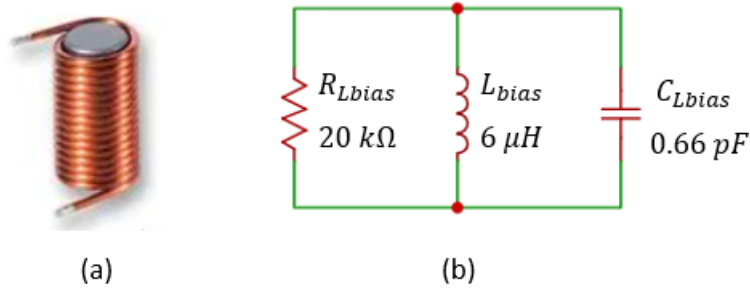


Figure 116: (a) Inductor used in bias tee (b) Electrical equivalent model of the inductance

After selecting the inductor, the C_{bias} capacitor is then determined in a manner that ensures the characteristic impedance of the Z_{bias} tee is precisely 50Ω . The value of the capacitor can be derived using the relationship defined in [110].

$$C_{bias} = \frac{L_{bias}}{Z_{bias}^2} = 2.4 \text{ nF} \quad \text{Eq. 70}$$

The C3216C0G2J222K115AA, a ceramic capacitor manufactured by TDK, is chosen. The capacitor details and its corresponding equivalent circuit with series parasitic inductance and resistance is presented in Table 15 and Figure 117.

Parameters	Value	Unit
Capacitor	2.2 ($\pm 25\%$ tolerance)	nF
Rated voltage (DC)	630	V
Self-Resonant Frequency	90	MHz

Table 15: Specifications of the ceramic capacitor from TDK

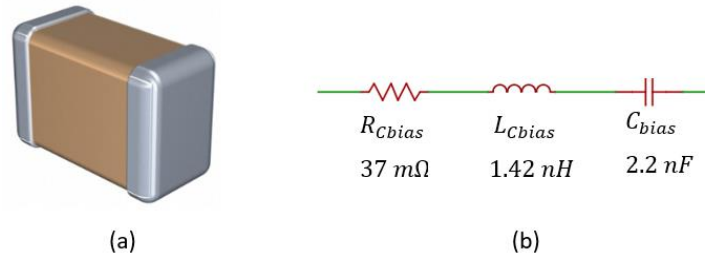


Figure 117: (a) Ceramic capacitor (b) Electrical equivalent model of the capacitor

To decouple the DC supply within the frequency range of 100 MHz to 1.5 GHz, a ceramic capacitor of 1 nF with its series connected parasitic inductance of 1.12 nH and resistance of 60 mΩ are employed. Before proceeding with the device implementation, an initial validation step is conducted using ADS circuit simulation diagram depicted in Figure 118.

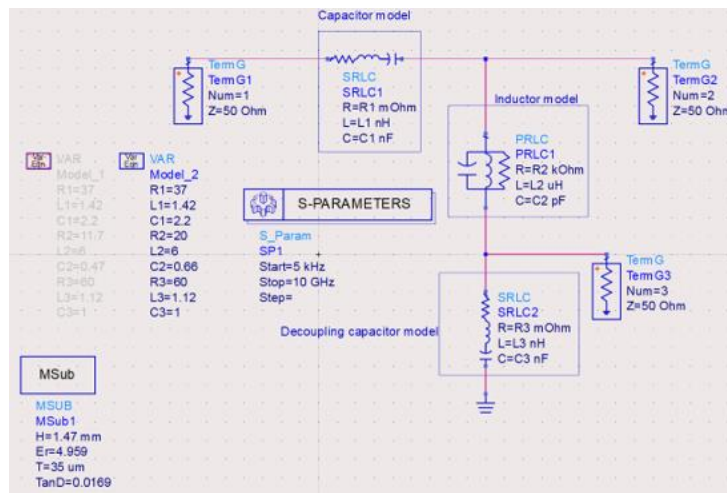


Figure 118: ADS circuit simulation of an electrical equivalent model of the bias tee designed

This validation entails performing an S-parameters simulation between the RF input and RF+DC output of the bias tee circuit simulation. The outcome, represented by the S_{21} magnitude is displayed in Figure 119 (a). The bandwidth suitable for S-parameters measurement is insured. This theoretical bandwidth ranges from 1.7 MHz to 4.26 GHz, comfortably encompassing the intended frequency range of 100 MHz to 1.5 GHz for S-parameters measurement. In addition, the simulation performed between RF input and DC output defines the bandwidth related to the isolation between RF and DC. Figure 119 (b) determines the isolation bandwidth of 6 MHz to 1.8 GHz between RF and DC signal.

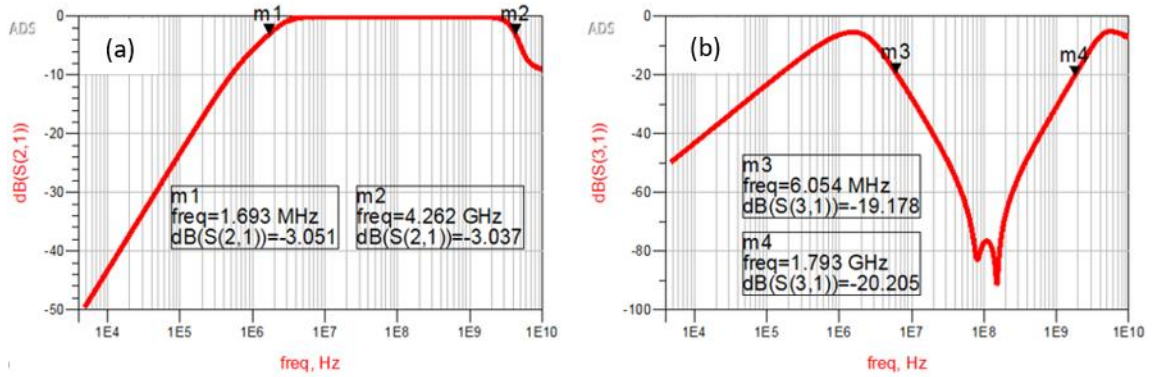


Figure 119: S-parameters magnitude measurement between (a) RF and RF+DC (b) RF and DC

Figure 120 (a) is the CAD PCB design layout of a bias tee. The S-parameters measurements are performed on Figure 120 (b) between RF input and RF + DC output by connecting DC connection to 50 Ω load, to validate the design.

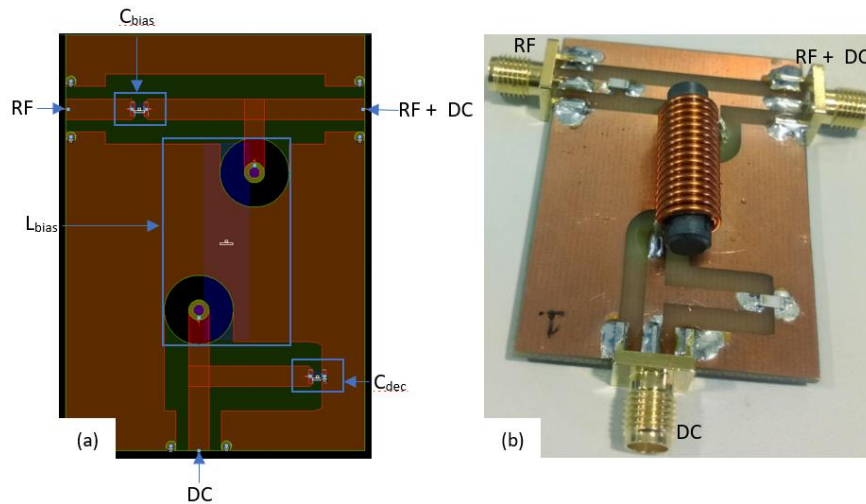


Figure 120: Bias tee PCB design (a) ADS design (b) bias tee realization

In fact, four bias tees shown in Figure 120 (b) are developed concerning the application requirement. S-parameters measurement of four individual bias tees between RF input and RF + DC output are presented in Figure 121. Considering the standard reference of -3 dB, the lower cut-off frequency achieved is 1.25 MHz and the higher cut-off frequency is 1.52 GHz for the transmission between RF and RF + DC. For the isolation between RF and DC a bandwidth of 1.48 MHz to 800 MHz is achieved considering -20 dB reference. All the four bias tees present similar characteristics.

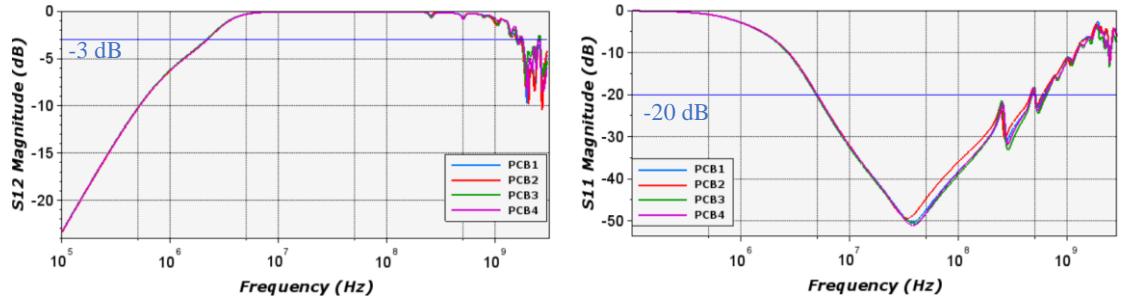


Figure 121: S-parameters measurement between (RF and RF + DC) in S_{12} and (RF and DC) in S_{11}

In this section, a bias tee with a bandwidth that encompasses the desired characterization frequency range, spanning from 1.25 MHz to 1.52 GHz is developed. The completed system allows to bias power device.

3.3.5.1 Experimental setup

This section describes the test plan considering the equivalent circuit given in Figure 122. The idea is to see if the polarization of the die brings some new results. The main use of the bias-tee is to isolate the DC and RF side to avoid any damage to VNA and DC supply. Considering a three terminal IGBT given in Figure 122, each terminal is connected to the RF + DC side of respective bias – tee. V_{com} is used to bias the gate of the IGBT, which is connected to gate and emitter through bias – tee 1 and 2. Port G and port E provide port connections to the VNA. R_{load} is placed between DC port of bias-tee 3 and positive pole of V_{dc} . The other end of the V_{dc} is connected to DC port of bias – tee 2 to close the circuit. The R_{load} allows to vary the applied current. Likewise, port C provides the port connection of collector with the VNA. To point out, the setup is ensured with proper grounding and appropriate shielding to minimize noise.

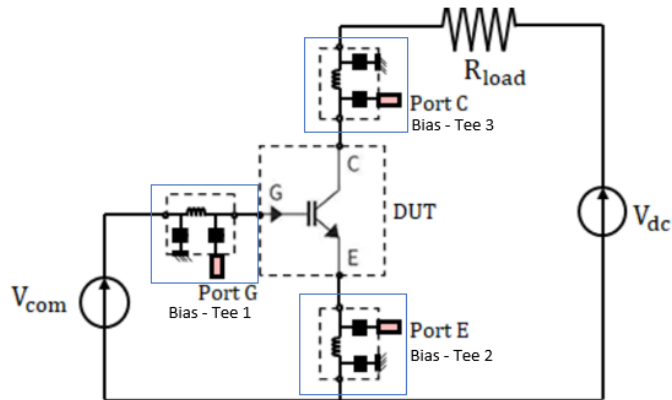


Figure 122: Test setup equivalent circuit with bias-tee to polarize the IGBT die

Before performing the measurements, a prior calibration (SOLT) is performed including 2 bias – tees in series. So, it is important to consider this impact on the measurement bandwidth. To answer, a characterization of 2 bias – tees connected in series has been done and the results are presented in Figure 123. The new reduced bandwidth is from 3.08 MHz to 1GHz for the transmission between RF and RF + DC. For the isolation between RF and DC a bandwidth of 5 MHz to 500 MHz is achieved considering -20 dB reference. Therefore, the next outcomes will be presented according to the new reduced bandwidth.

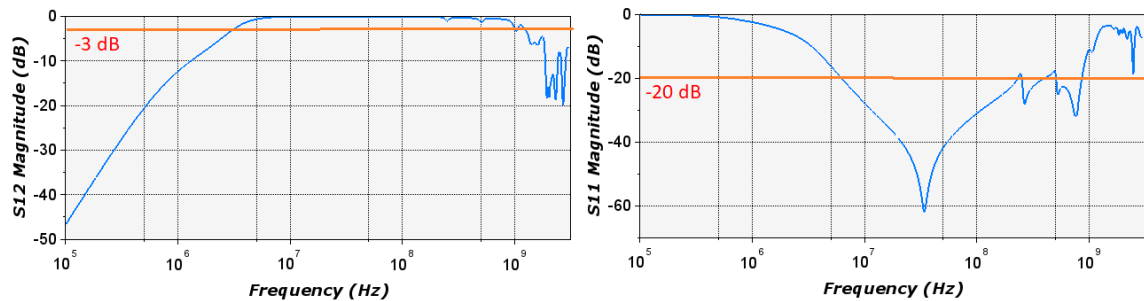


Figure 123: Characterization of 2 bias - tees in series

The interesting configuration to measure would be connecting port C and port E to the VNA port 1 and Port 2 respectively, while port G is left floating or connected to 50 Ohm-load. Figure 124 presents the experimental setup inspired from the equivalent circuit presented in Figure 122.

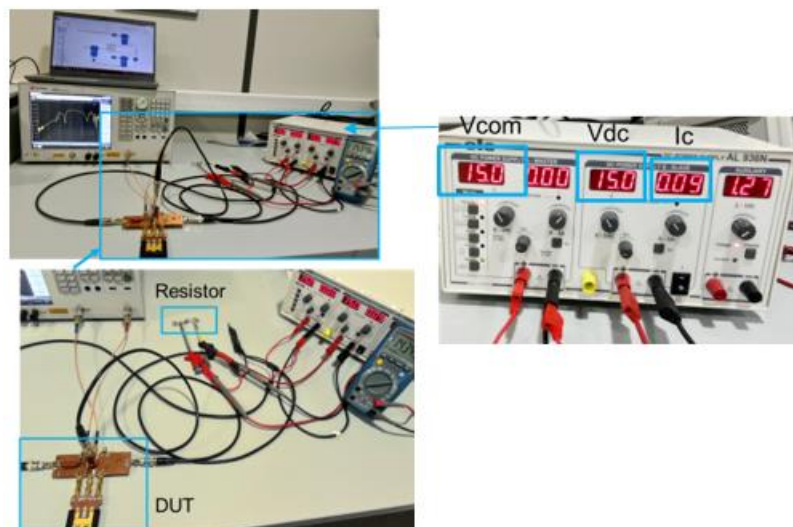


Figure 124: Experimental setup to polarize the IGBT die mounted on ceramic substrate

Following the measurement on healthy prototype, the gate is biased by applying 15 V between gate and emitter (V_{com}) which is greater than the threshold voltage. V_{dc} voltage

of 15 V is applied and measurements are carried for two different currents (100 mA and 2 A). Figure 125, illustrates the S_{11} and S_{21} measurement of a ceramic substrate with IGBT die polarized in a healthy mode by connecting port 1 to port C and port 2 to port E. On the whole bandwidth, there is no huge difference between the measurements following 100 mA and 2A.

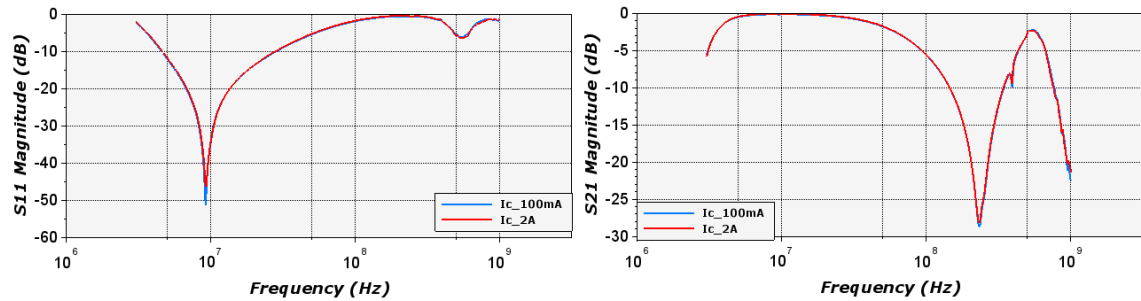


Figure 125: S_{11} and S_{21} measurement between collector and emitter of ceramic substrate with IGBT die in healthy mode in bandwidth (3 MHz – 1 GHz)

3.4 *Homemade packaging design and simulation on ADS software*

This section demonstrates the design and simulation of ceramic substrate using ADS software. As presented in Section 2.8.2 performing ADS simulation on microstrip line, the process is now followed to design and simulate homemade packaging. As this package contains two individual parts (i.e., AMB ceramic substrate plus an epoxy interface for characterization) it adds difficulty. Therefore, epoxy interface and ceramic substrate are designed separately following the process (as described in Section 2.8.2). Details are provided in Appendix 4-24 and Appendix 4-25 for epoxy interface and ceramic substrate, respectively. The interesting point in this 3D designing process is that at every stage the model can be simulated. Finally, using the individual design of epoxy interface and ceramic substrate the overall module is built shown in Figure 126 (a) and (b). The 3D simulation is compared with the experimental data as depicted in Figure 127.

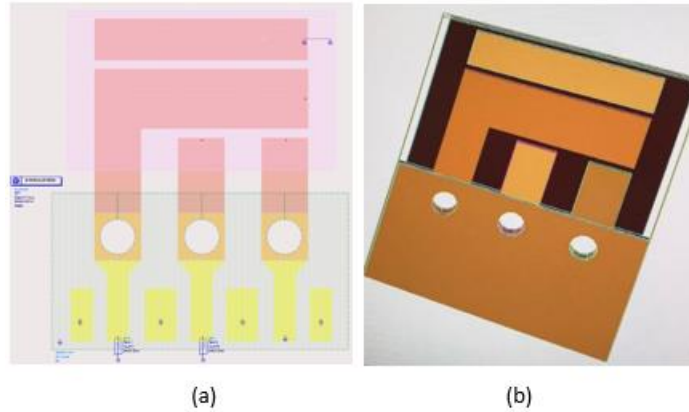


Figure 126: Ceramic substrate with epoxy interface (a) Visualization in layout, and (b) 3D environment

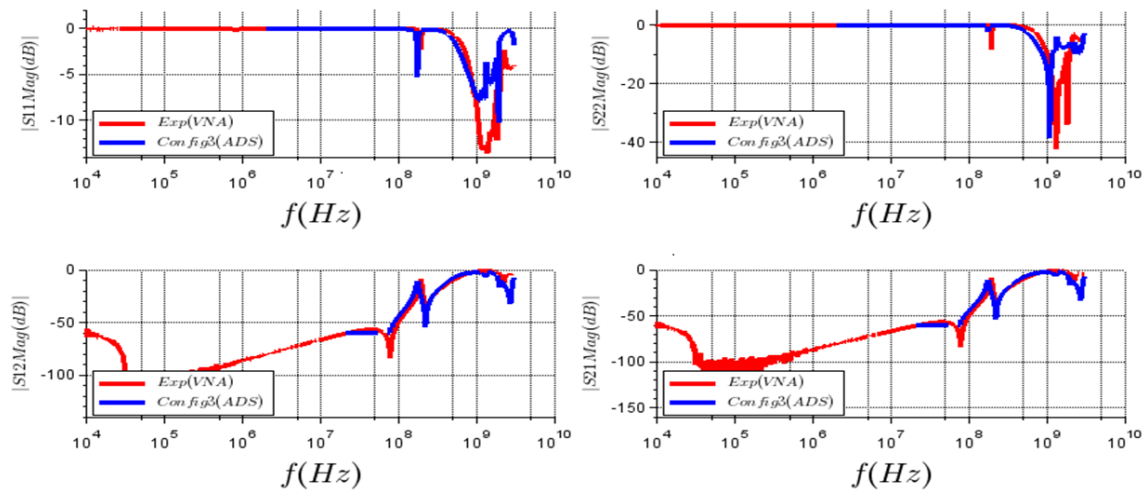


Figure 127: Comparison of experimental and ADS 3D simulation results of ceramic substrate following config3

The results are quite interesting. Effectively, the resonance frequencies are recovered in the bandwidth of 100 kHz to 1 GHz with any difference less than 3 dB. Some variations are observed above 1 GHz. Let us remind that, the SMA model is still not considered in this simulation. It can be assumed that, the SMA model combined with the other elements of the prototype have an impact above 1 GHz.

3.5 Conclusion

This Chapter demonstrated the application of NDT methodology to power assemblies in healthy state. It allowed us to study the behavior of assemblies in healthy state. The methodology applied to discrete packages result in good agreement between experimental and LTspice simulation in frequency bandwidth of 100 kHz to at least 100 MHz following the packaging. The parasitic elements extraction of discrete package is detailed which

adds some additional steps having three terminal connections. The RLCG elements extracted from methodology are compared with datasheet and CV measurements from B1505A curve tracer. B1505A measures only the capacitances and datasheets hardly provide complete data about the parasitic elements while the proposed methodology is able to extract all the elements. This is the innovative and added value of the proposed NDT method. An interface has been developed to support the two-port characterization of discrete devices which ease and save the measurement time.

The methodology is then applied to Si_3N_4 AMB ceramic substrate which was developed for an aeronautical application and is supported to achieve the objectives of this thesis. To support the characterization of this package with VNA an epoxy interface has been developed. The copper tracks brazed on the ceramic substrate allows to integrate semiconductor chips and to form connections with the other tracks through bond wires which is common phenomenon in power electronic modules. This prototype is close representative of power module. In addition, the design and simulation of ceramic substrate using ADS software are presented. ADS tool recovered some excellent results in designing and simulating the ceramic substrate.

Chapter 4 :
Application of NDT methodology to identify
failure induced manually or by accelerated aging
tests

4.1 Introduction

This chapter presents the identification of failure using NDT methodology. The failure can be obtained in different ways like through aging tests or can be done manually. Let us remark that this chapter is not a reliability analysis of devices. The accelerated aging tests are just used as a tool to induce failure modes in power assemblies. However, for each aging tests a brief description will be provided. The accelerated aging test used in power electronics are the Passive cycling test, commonly known as Temperature Cycling Test (TCT) and Active Power Cycling (APC) simply called as Power Cycling (PC). In the following, these two aging tests plus manual test are performed to accelerated aging of power assemblies. The two power assemblies that are studied in the following are discrete power devices (TO packages) and a homemade power assembly, based on a Si_3N_4 ceramic substrate whose details are provided in Section 3.3.1. During several aging campaigns, a huge amount of data was produced. To give an idea about the different sections that are going to be addressed a summary is presented in Table 16. This table summarizes the different tests conducted on different power assemblies. Each failure mechanisms observed is also reported.

Device under test	TCT	APC	Manual
Substrate	No failure detected but robustness of the measurements is addressed		
Substrate + bond wires			Bond wire failure
Substrate + IGBT + bond wires			Bond wire failure
Substrate + IGBT (polarize) + bond wires			Bond wire failure
TO packages		Bond wire failure	
TO packages	Bond wire failure		
Substrate + clips	Brazing failure		

Table 16: Summary table of different tests and failure observed

In such a context, this chapter is organized as follows: firstly, to present accelerated aging test describing the objectives, the test benches, the working principles, etc., Secondly, the

application and analysis of failure detection using NDT methodology are illustrated. Similar failure mechanisms are grouped together which allow us to conclude on different aspects following different test. Following the sequence of Table 16, wire bonding lift-off will be first present and then aging of brazing.

4.2 General tips on accelerated aging tests

Accelerated aging tests are widely adopted to evaluate electronic components' reliability. Power electronic components are expected to provide longer service life, including working in harsh environments, continuous switching, and instant load variations. Every component experience aging in regular life however this aging process is slow. Therefore, to accelerate the aging process the aging tests are conducted. The usual aging tests practices in power electronics include passive and active cycling tests. Both tests are crucial for assessing the reliability, durability, and performance of power electronics components and systems. When evaluating the reliability of power electronics packaging, it is essential to encompass factors beyond environmental hazards. In reality, the chip's functioning can contribute to the deterioration of the packaging. This thesis focuses more on failure identification related to device packaging such as bond wire and solder fatigue related failures. The devices are exposed to change of temperature by maintaining the required temperature difference to stress the components. The temperature difference is set based on aeronautical norms. Different types of accelerated tests exist to match several stresses distinguishing the passive and active types mentioned in [111].

4.3 Selected aging tests

During this thesis three type of aging tests: Active Power Cycling (APC), Temperature Cycling Test (TCT), and manual aging test are performed on power electronic assemblies. All tests were achieved onto the PRIMES Platform.

Active Power Cycling (APC) distinguishes itself from TCT test by its heat source. In APC, the chip serves as an internal source (active), while in TCT, the environment provides the heat source (passive). Consequently, the temperature distribution within the tested device differs: APC yields a non-uniform temperature distribution, whereas, TCT maintains a uniform module temperature. Additionally, cycle times for APC are typically ten to a hundred times shorter (ranging from 0.2 seconds to 1 minute) compared to TCT (ranging

from 15 minutes to 1 hour). A brief description of each of these tests is presented in the following.

4.3.1 Temperature Cycling Test (TCT)

Temperature Cycling Test (TCT) in power electronics typically involve subjecting components or devices to several cycles between different operational conditions (such as temperature). The failure mechanisms observed in this test are linked to failure modes such as open circuits resulting from the thermomechanical fatigue. The primary aim of this test is to assess the solder interfaces' fatigue life connecting the semiconductor chips, substrates, and baseplates [112]. This goal is accomplished by fixing the device under test onto a plate that undergoes external heating and cooling to replicate the cycling conditions. This test is performed using Climatic Temperature System (CTS) or thermal shock which consists of climatic chamber, where the DUTs are placed inside the test chambers to expose to rapid temperature changes. Typical environmental conditions that DUT can be exposed in climatic chamber include extreme temperatures, sudden and extreme temperature variations, moisture or relative humidity and more. In the following, solely the temperature is changed. Figure 128 presents details of the Climatic Temperature System (CTS) [113] used during this thesis. Usually, the distribution of temperature in the climatic chamber is almost uniform. The cycle scheduled must insure the uniform temperature assumption for DUT.



Climatic Temperature System (CTS)	
Temperature range (°C)	-70 /+180
Temp. change rate cooling (K/min)	5, 10, 15
Temp. change rate heating ((K/min)	5, 10, 15
Temperature fluctuation (K)	≤±0.3
CID software	Programming and documentation

Figure 128: Climatic Temperature System details [113]

Figure 129 provides the temperature profile of 1 cycle used for passive cycles on CTS. One cycle is programmed for an hour with extreme temperatures (-70 °C and +180 °C) and slope rate of 12.5 °C/min. The cycles are related to the IEC 60068-3-5 norm.

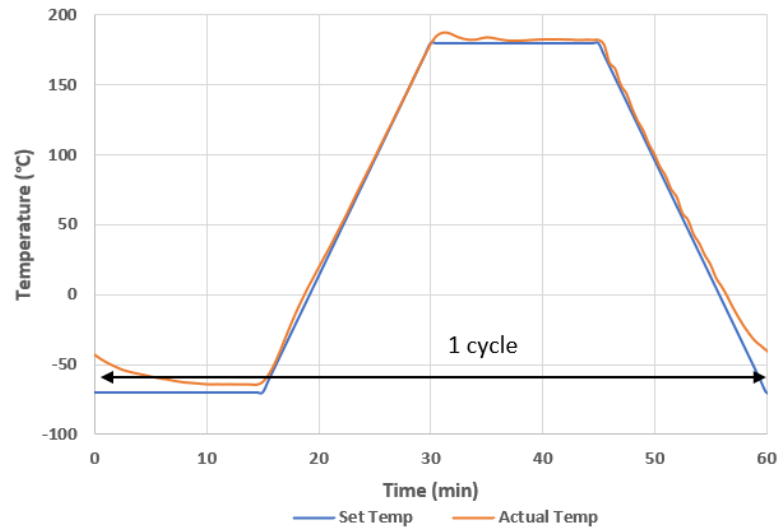


Figure 129: Temperature cycle as a function of time

The temperature profile presented in Figure 129 is the default profile that is used for TCT test during this thesis until any changes are mentioned. The actual temperature variation in climatic chamber is monitored using thermocouple of type K (withstand up to 400 °C) along with Graphtec (data logger, GL220). One end of the thermocouple is placed inside the climatic chamber and the other end is connected to the data logger to monitor the temperature inside the chamber. The comparison of the set and actual temperature is provided in Figure 129, which are very close to each other. It is noted that the steady state is reached and an error is made during the transient state.

4.3.2 Active Power Cycling (APC)

Accelerated active cycling tests which also known as Active Power Cycling (APC) tests are the other crucial aging tests in power electronics to determine the reliability and lifetime of the components.

APC testing simulate accelerated aging. The cycles applied consist of a heating phase (T_{on}) induced by a controlled power current (I_{cst}) circulating within the module, as illustrated in Figure 130. The chip, experience a rise in its junction temperature, referred to as T_j Within each cycle, a distinction is drawn between the peak temperature (T_{jmax}), and the lowest temperature (T_{jmin}) reached. Due to their minimal thermal inertia, the chips promptly reach T_{jmax} at the end of heating phase. Subsequently, a cooling phase (T_{off}) allows the chips to attain T_{jmin} . During cooling phase, the test bench records a

thermosensitive parameter. These parameters include on-voltage drop (V_{on}) at the applied heating current (which can also be referred as on-state drain-source voltage (V_{DS_ON}) while operating in transistor mode, forward voltage (V_F) in diode mode), I_{cycle} (heating current), P (heating power), $T_{j(hot)}$ (maximum junction temperature), $T_{j(cold)}$ (minimum junction temperature), ΔT_j (junction temperature change), and more. The test bench records complete thermal transients at predefined intervals. If any monitored parameter surpasses the predefined limit, the system automatically stops, necessitating the deactivation of the effected device, after which the cycling process can be continued with the remaining devices. These recorded parameters can act as indicators to state the failure occurrence. If the values of these parameters exceed a predetermined threshold (e.g., 20% increase), it's the end of the life criteria for the components [114]. The usual failure mechanisms that are observed from these tests are bond wire related failures, and solder fatigue. The failure mechanisms can be targeted by setting the cycle times depending on the characteristics of DUT. Usually, bond wire failures are encountered by setting shorter time cycles (seconds) and higher time cycles for solder fatigue (minutes) which corresponds to thermal time constant.

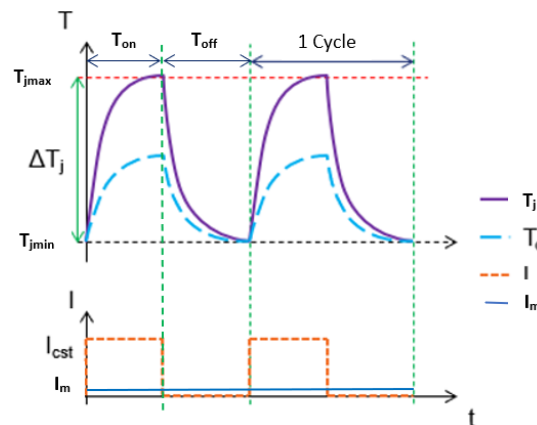


Figure 130: Typical thermal profile of power cycles [115]

The test bench that is used to perform APC is Mentor Graphics (MicReD Industrial, 1500A Power Tester [116]) given in Figure 131. This test bench enables testing of multiple devices by providing 3 testing channels with rating of 500 A and 12 V per channel.

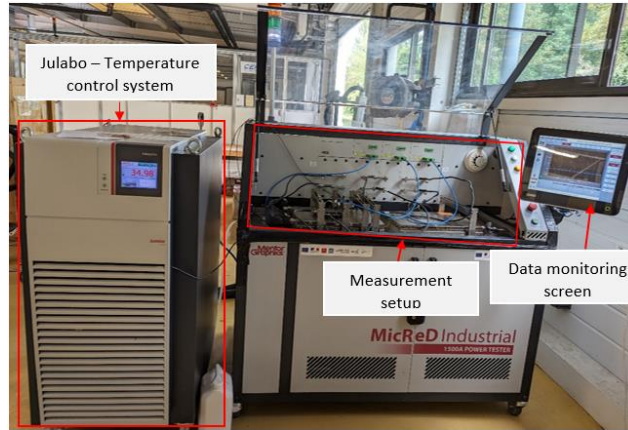


Figure 131: Mentor Graphics (MicReD Industrial, 1500A Power Tester)

4.3.3 *Manual aging test*

This process involves physically removing the wire bonds. This test needs a bit of attention, especially when performing this action on a cluster of closely interconnected bond wires in parallel, as errors may occur. To mitigate this, a fine-tip wire cutter can be employed to individually lift-off a particular bond wire without the need for excessive force.

4.4 *Reliability of the measurement process*

This section demonstrates the robustness of the measurement process all along the aging process. The measurement process remains similar for TCT, APC and manual. In the following section the case study is the TCT aging of the ceramic substrate. The aging and characterization algorithm illustrated in the following was applied on ceramic substrate for over 8 months. Additionally, a discussion is provided to present the measurement constraints due to grounding techniques and the needed improvements in the measurement protocols. Let us note that the ceramic substrates do not embed any interconnects.

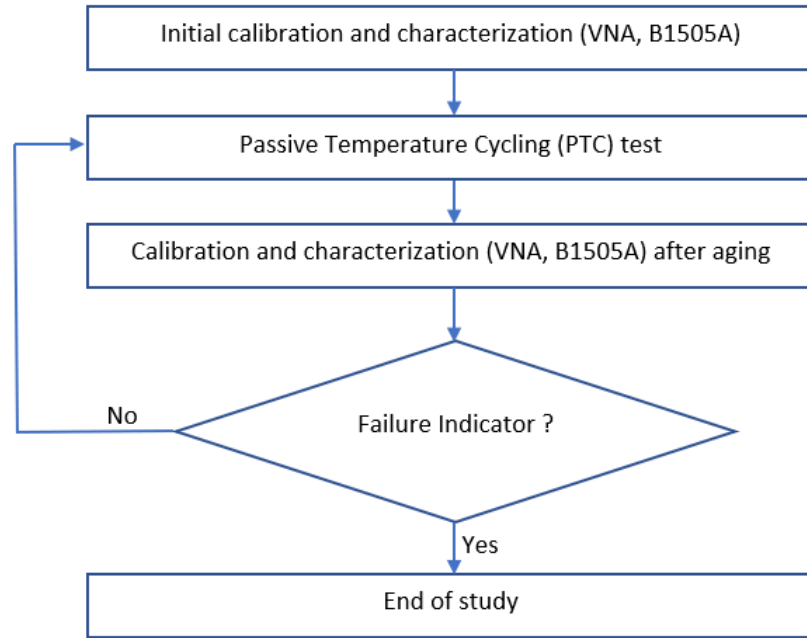


Figure 132: Aging and characterization algorithm

Figure 132 illustrates the process combining health characterization and accelerated aging of the component under test. The aging test, characterization, and its comparison with the reference measurement are repetitive process until failure of the component under test is detected. When this occurrence is reached, the process ends i.e., peculiar behavior of aged components compared to the reference measurement. In this case, it can be modification in impedance magnitude or resonance frequency.

Considering this first aging test, 10 ceramic substrates are chosen to perform passive cycles. It is expected to see degradation of interface between metallic parts and the ceramic substrate, as well as possible crack formations. Figure 133 presents different steps involved in aging and the characterization process.

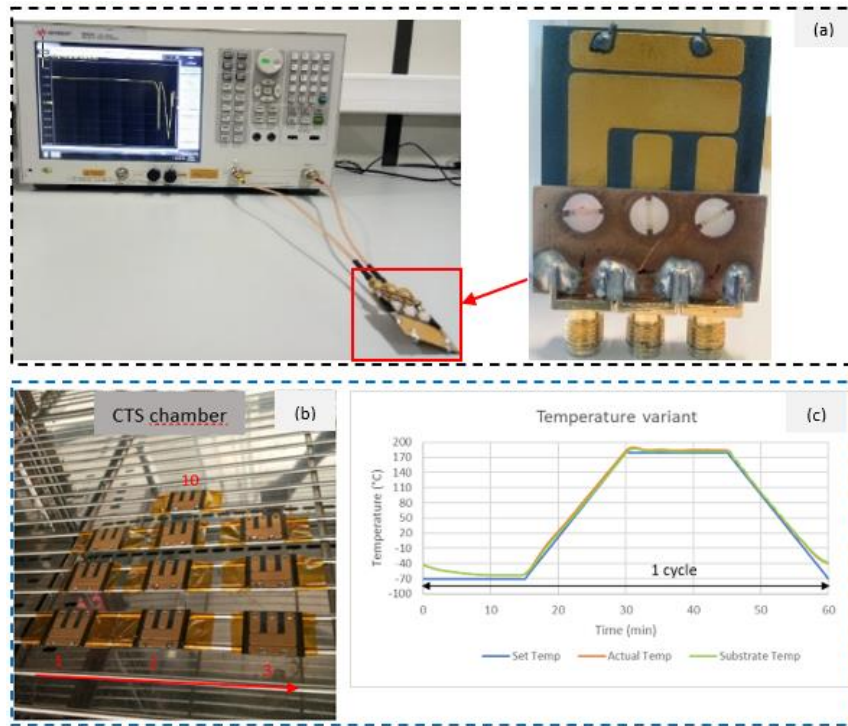


Figure 133: (a) VNA characterization process, (b) DUT in climatic chamber, and (c) Temperature monitoring

Figure 133 (a) presents the two-port VNA characterization. Figure 133 (b) illustrates the placement of DUT in CTS chamber. Figure 133 (c) presents the comparison of set temperature to the actual temperature inside the CTS chamber and temperature experienced by DUT. An initial broadband characterization to measure S-parameters from VNA (Figure 133 (a)) are performed on 10 healthy prototypes. This measurement provides a reference for the subsequent characterizations. To point out, the VNA characterization of ceramic substrate is supported by the epoxy interface (detailed in Section 3.3.1). However, these interfaces are not included in aging process. The ceramic substrate is connected with the grounding wires to connect unused tracks to the ground (detailed in Section 3.3.1). The ceramic substrates with grounding wires are then placed into climatic chamber using Kapton tape (Polyimide film, Hi-Bond HB830) given in Figure 133 (b). The Kapton tape provides good insulation with withstanding temperature of 250 °C. The prototypes are numbered from 1 to 10 from left to right in ascending order for identification. Thereby, the CTS is programmed to obtain required number of passive cycles with the temperature variation from -70°C to 180°C as provided in Figure 129. The substrate temperature is monitored by placing type K thermocouple onto one of the copper

tracks of the substrate and connecting the thermocouple to the data logger. 10 prototypes are divided into two series: series 1 has prototype 1 and 2, while series 2 is from prototype 3 to 10. The only difference between series 1 and series 2 is that series 1 prototypes are 144 cycles ahead of series 2 prototypes. This division of prototypes into two series is with an intention to see an intermediate failure (e.g., propagation of cracks).

The aging cycles are set for a week or 15 days following the availability of the CTS machine, and characterization schedule. The characterization is performed at the end of each set of cycles that are planned. The S-parameters (from VNA) are analyzed to verify the impact of aging tests compared with reference measurements.

4.4.1 Measurement constraints

After 318 cycles, a shift in resonance frequency is observed on prototype 1 and 4 from series 1 and series 2 respectively. Figure 134 presents the S-parameters magnitude at 0 cycles and 318 cycles of prototype 1 following config1 (Section 3.3.1). The shift in frequency resonance is highlighted with blue box. The results are better analyzed using reflection coefficients (S_{11} and S_{22}) which are expected to show complete reflection of injected.

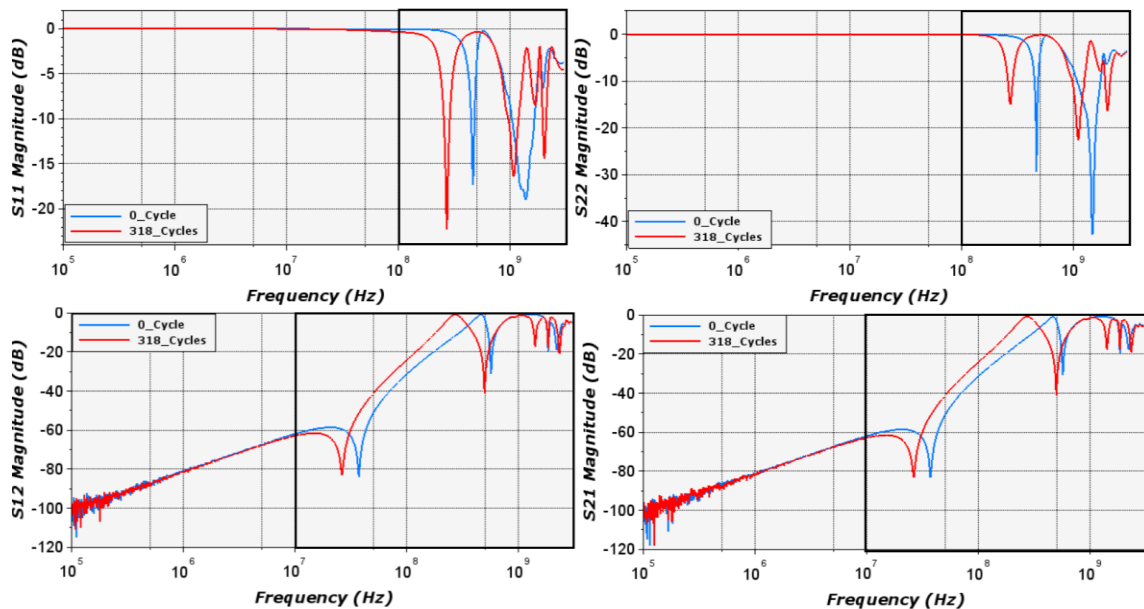


Figure 134: S-parameters magnitude at 0 cycle and 318 cycles of prototype 1 following config1

The very first question to be asked is, this shift in frequency is due to failure occurrence? If so, is it not too early to detect the failure at such early number of aging cycles according

to the literature study [117]. Indeed, [117] presents the thermal shock and Scanning Acoustic Microscopy (SAM) results comparing substrate technology with number of aging cycles. This paper reveals the reliability check of Si_3N_4 ceramic substrate following Active Metal Brazing (AMB) technology over number of thermal cycles. Si_3N_4 shows effective performance over 8500 thermal cycles compared with the other substrate technologies presented in Figure 135. In our case, the applied aging test is less stressful than thermal shock but a change appears. So, it seems to be not a real failure.

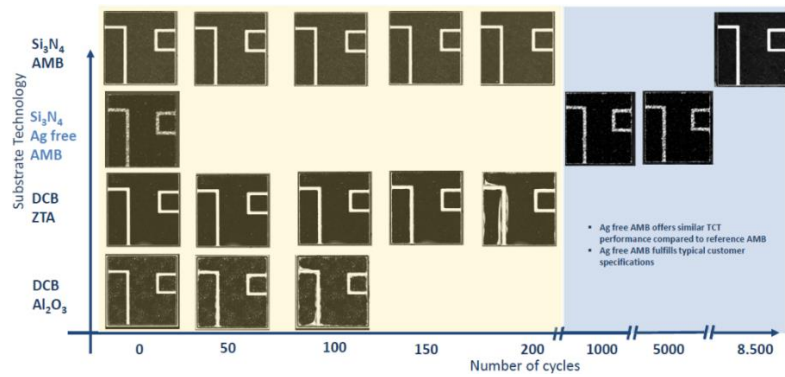


Figure 135: SAM evaluations of various Metal Ceramic Substrates (MCS) types after thermal cycling [117]

To make a deeper analysis, S-parameters presented in Figure 134 are converted into Z-parameters given in Figure 136.

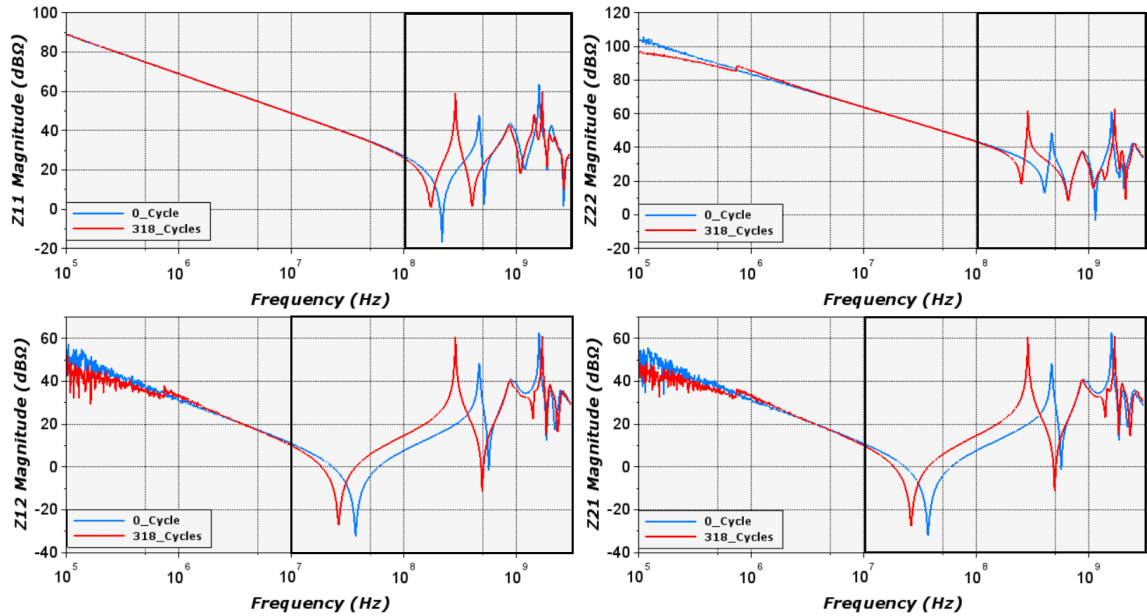


Figure 136: Z-parameters magnitude at 0 cycle and 318 cycles of prototype 1 following config1

The Z-parameters reveal identical capacitive behavior. As a matter of fact, the shift in the resonance frequencies results of a different inductive behavior. It is highlighted with a black box. Therefore, the impact might be related to the aging of element which exhibit inductive and resistive behavior. The most inductive elements of the prototype are the grounding wires. To confirm this hypothesis, at the end of 405 cycles the aged grounding wires are replaced by new ones with identical electrical and geometrical characteristics. Let us remark that, the difference in the number of cycles (318 and 405) can be explained by the fact that the aging stage lasts several days, whereas the characterization stage lasts few hours. As a result, as soon as characterization is complete, the substrates are again subjected to aging, and data processing is then carried out. This explains why the failure of grounding wires is identified at 318 cycles, but were only able to change the wires at 405 cycles. Then, the aging test is relaunched and continued until 405 cycles. The characterizing curves after 405 cycles shift back to the initial measurement curves (0 cycle measurement) as shown in Figure 137. The comparison of Z-parameters is also presented Figure 138 which establish the similar results.

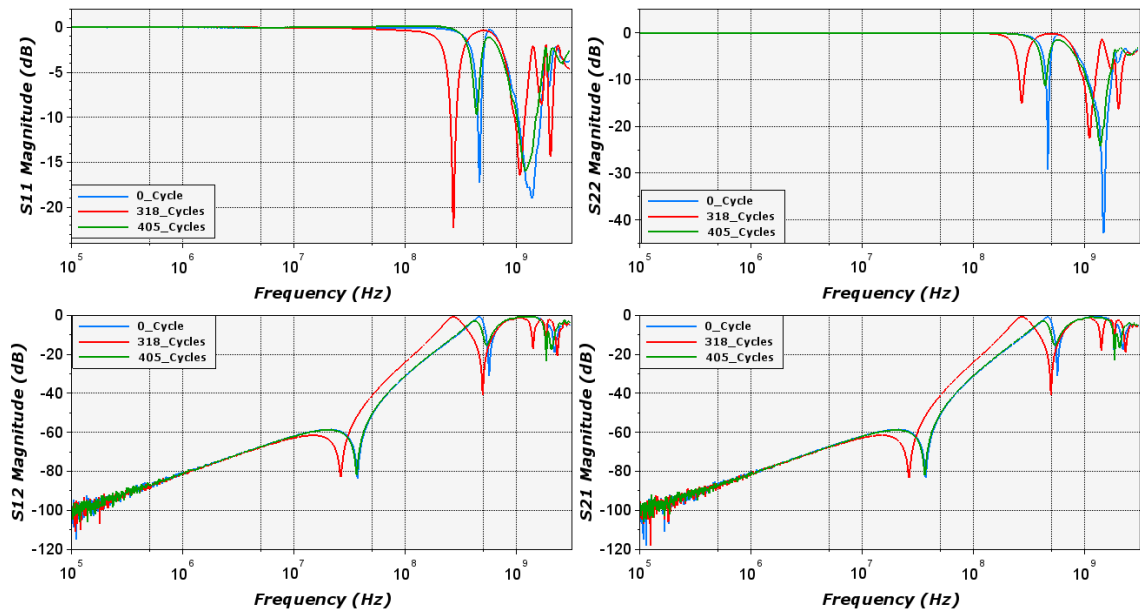


Figure 137: S-parameters magnitude at 0 cycle, 318, and 405 cycles of prototype 1 following config1

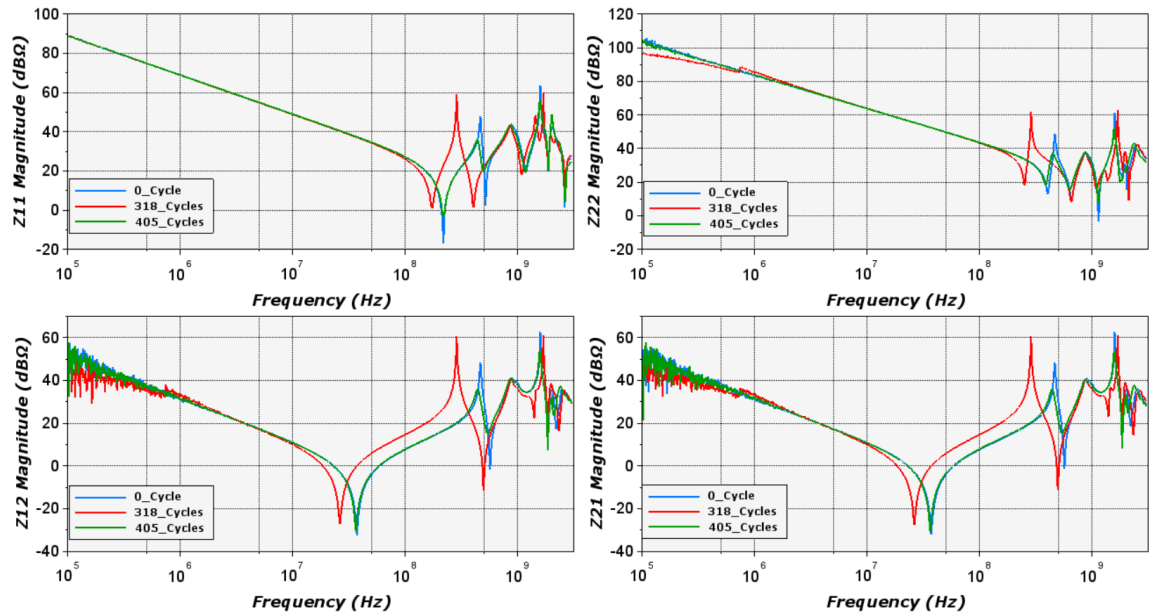


Figure 138: Z-parameters magnitude at 0 cycle, 318, and 405 cycles of prototype 1 following config1

It is interesting to point out that, the other configurations reached the same conclusions (Appendix 4-26 and Appendix 4-27). Following these measurements (reference, failure after 318 aging cycles, and after 405 cycles with renewed grounding wires) an impedance extraction was carried out and is presented in Table 17. The impedance characterization uses the methodology described in previous Chapter.

DUT	R ₁₁ (Ω)	R ₁₂ (Ω)	R ₂₂ (Ω)	L ₁₁ (nH)	L ₁₂ (nH)	L ₂₂ (nH)	C ₁₁ (nF)	C ₁₂ (nF)	C ₂₂ (nF)	G ₁₁ (μS)	G ₁₂ (μS)	G ₂₂ (μS)
Healthy (0 cycle)	0.12	0.03	4.6	4.53	4.72	12.63	58.47	3854	9.2	45.11	45.94	44.73
Faulty (318 cycles)	1.06	0.04	7.81	6.37	8.18	31.32	59	4513	10.18	0.908	1.04	0.169
Renewed (405 cycles)	0.68	0.03	8.1	4.8	4.5	11.94	57.85	4321	10.42	0.276	0.354	0.301

Table 17: RLCG parameters extracted from measurements for healthy, faulty, and renewal of grounding wires

The values obtained confirm a slight change in capacitance, but a clear increase in the inductance of the device under test. Furthermore, due to the dimensions and geometry of the substrate tracks, their equivalent impedance is capacitive in nature. In contrast, the impedance of the brazed grounding wires is essentially inductive. As far as conductance variations are concerned, it should be noted that between healthy, faulty and renewed the variations are important. It is assumed that conductance change is not directly related to

the aging of the grounding wires. Furthermore, the device under test involves different materials (copper and grounding wire insulation, solder and probably few flux droplets, substrate materials), making it difficult to analyze certain phenomenon in detail.

4.4.2 Optimization of the measurement protocols

Though the grounding technique using grounding wires is effective but experience constraints when performing aging tests. Therefore, a new specific 3D interface has been designed to ground the floating tracks. It is presented in Figure 139 (a). The 3D interface, made of polyamide material, has been realized in additive manufacturing. The dimensions of the 3D interface are given in Appendix 4-28.

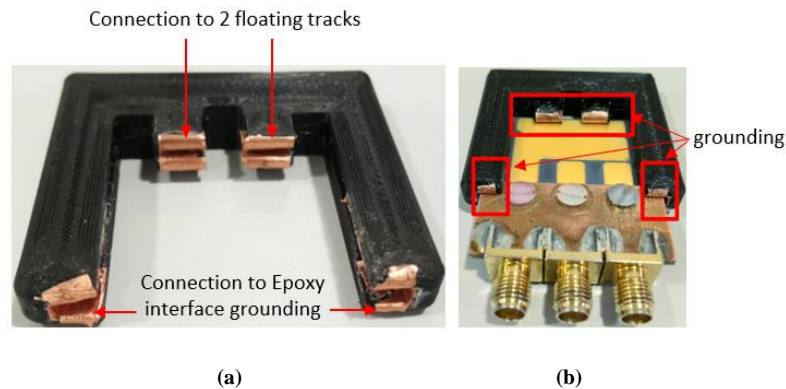


Figure 139: 3D interface to ground floating tracks (a) 3D interface (b) in measurement condition

When the prototype is inserted into the 3D interface, the forks, made of copper tape, present on the rear part of the 3D interface allow to connect the two floating tracks to the same potential. As for the two lateral grooves, they establish the electrical connection between the floating tracks and the ground plane present onto the top side of the epoxy interface. It is depicted in Figure 139 (b). Let us remark that the 3D and epoxy interfaces are only used during the characterization process. Let us insist on that the grounding is always verified earlier to any VNA measurement using DC meter.

A comparison of characterization curves following both the grounding techniques is presented in Figure 140. Analysis of the amplitude of the reflection coefficient (S_{11}) shows that, for frequencies above a few hundred megahertz, the 3D interface is much more efficient than simple brazed wires. Shift in resonance to higher frequencies is seen on transmission coefficient (S_{12}). Furthermore, analysis of the amplitude of Z-parameters

illustrated in Figure 140 (c & d) indicates that the main differentiation between the two technical solutions lies in the inductive nature of the solution.

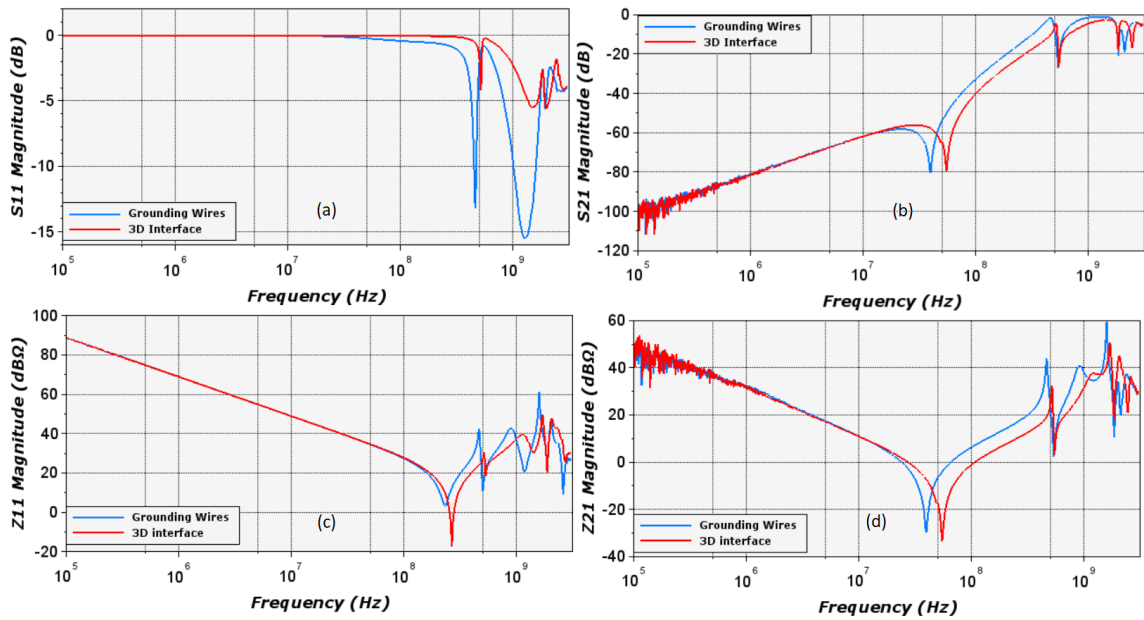


Figure 140: S and Z parameters magnitude comparing the grounding technique

Therefore, the 3D interface is used for the next analyses. This result is published and presented in [118]. One important point to be noted here is that, the constraint on measurement due to grounding technique raised only from aging otherwise both the techniques are effective. Therefore, in the further analysis, any of the grounding technique can be used if there are no constraints. Let us remark that, if one of these grounding techniques is adopted to perform test, it will be followed until the end of the aging campaign of this particular test.

Parameters	Series 1	Series 2
No. of prototypes	2	8
Temperature variation (°C)	-70/+180	-70/+180
No. of cycles	3338	3194
Aging period (months)	8	8
Characterization	Every 10 days	Every 10 days
Type of characterization	VNA	VNA

Table 18: Summary table of passive cycling test on homemade packaging with no interconnects

Table 18 summarize the aging test and the characterization performed on ceramic substrates. Considering the measurement improvements, the aging has been continued for 8 months reaching 3338 cycles for series 1 prototypes and 3194 cycles for series 2. The comparison of VNA characterization for different aging cycles including the latest aging cycle is presented in Figure 141.

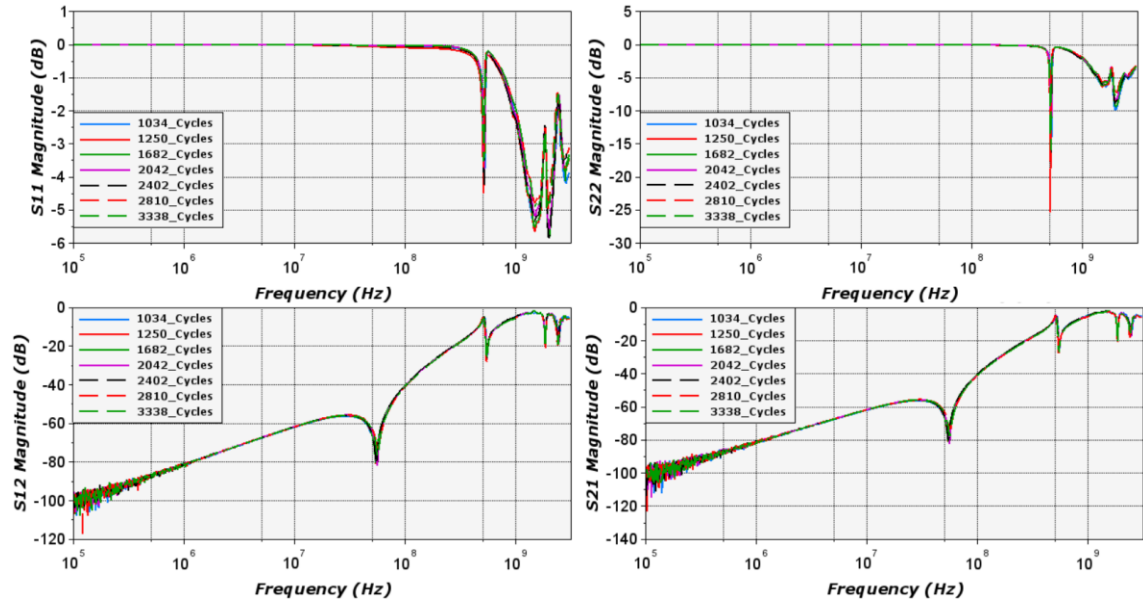


Figure 141: S-parameters magnitude of successive aging cycles from 1034 cycles to 3338 cycles of prototype 1 following config1

The comparison of VNA characterization for different cycles reveal similar behavior by superposing the curves shown in Figure 141. It is noted that no failure was identified. The comparison of Z-parameters is presented in Figure 142, which reach the same conclusions.

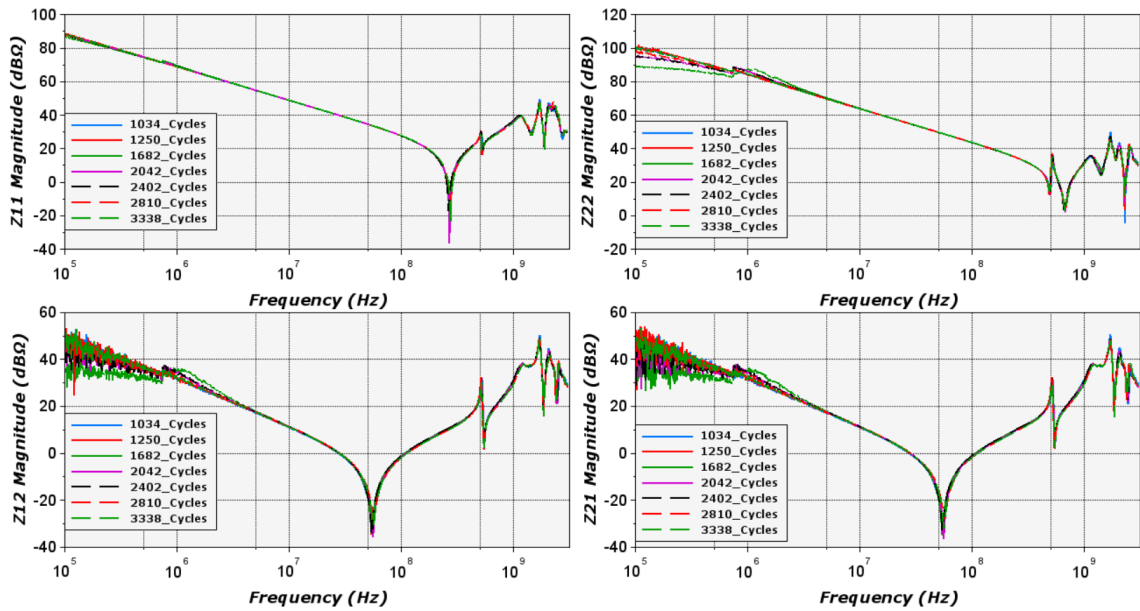


Figure 142: Z-parameters magnitude of successive aging cycles from 1034 cycles to 3338 cycles of prototype 1 following config1

All the 10 prototypes provide similar characterization curves as no failure was detected. For example, Figure 143 presents the comparison of S parameters magnitude for all 10 prototypes considering the latest aging cycle (3338 cycles for series 1 and 3194 cycles for series 2) following config1. This results again proves the robustness of the measurements and confirms no huge changes observed on all the 10 prototypes until the latest aging cycles.

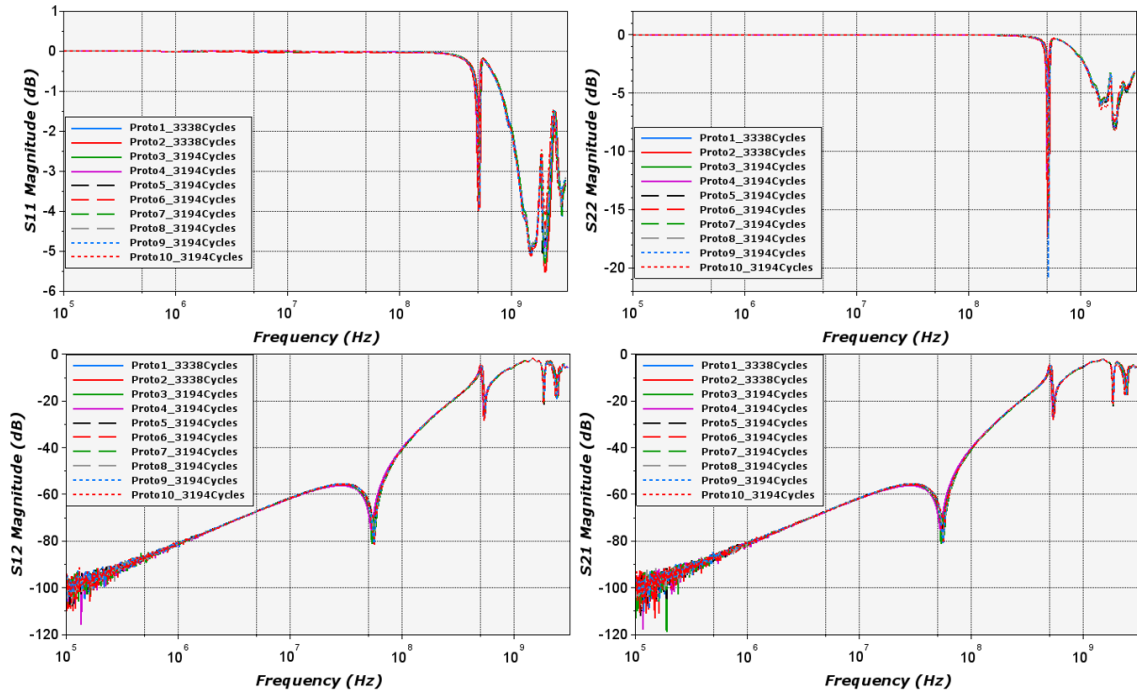


Figure 143: S-parameters magnitude of series 1 (3338 cycles) and series 2 (3194 cycles) prototypes following config1

The Temperature Cycling Test (TCT) on ceramic substrate on 10 samples has been carried out for 8 months. Considering the reliability of Si_3N_4 ceramic substrate as mentioned in [117], no failure has been detected covering 3338 passive temperature cycles. The characterization results of this campaign demonstrate the robustness of the measurements. To add, a systematic procedure has been followed considering improvements made from beginning to the end of process.

4.5 Bond wire failure analysis following NDT methodology

As presented in Chapter 1, bond wire lift-off is one of the most important failure in power devices. This section aims to illustrate the bond wire failure analysis using the newly developed NDT methodology. The bond wire failure is induced in three different ways: By manual cut off (Section 4.5.1, 4.5.2 and 4.5.3), by APC test (Section 4.5.4), and by TCT (Section 4.5.5). The analysis is carried out following the hypothesis « Occurrence of failure changes the electrical impedance »

4.5.1 Ceramic substrate with bond wires between Track 1 and Track 2b

This section presents the two-port characterization of ceramic substrate with bond wires by inducing the bond wire lift-off manually. The bond wire lift-off is done on the tail of

the bond wires (from left to right) connected to Track 1 side. Figure 144 illustrates the healthy state of ceramic substrate with bond wires and indicates the direction of manual lift-off action (black arrow).

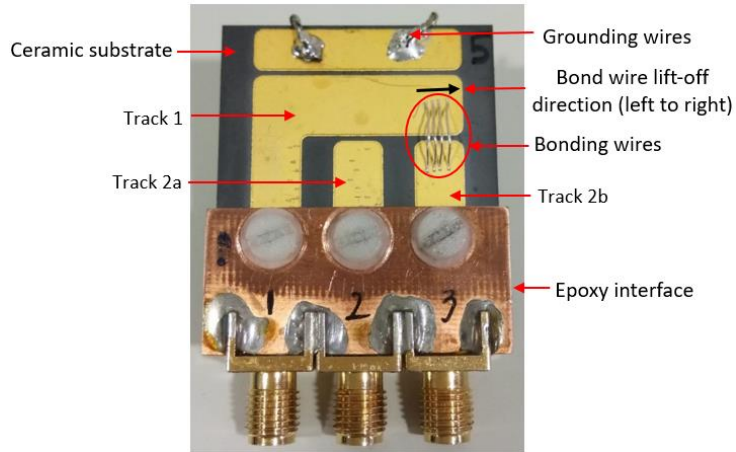


Figure 144: Ceramic substrate with bonding wires in measurement condition indicating the direction of manual lift-off of bond wire

The characterization process is as follows:

- Firstly, the VNA is calibrated and healthy state characterization is performed to measure S-parameters (i.e., when 4 bond wires are all connected) as illustrated in curve 4BW_T1&2b
- 1 bond wire is lifted-off manually to plot curve 4(-1)BW_T1&2b
- Two-port characterization using VNA to measure S-parameters
- Then after the second bond wire is lifted-off curve 4(-2)BW_T1&2b. Then the two-port characterization is achieved. Etc. This process is successively done until 3 bond wires are lifted-off and 1 bond wire remains connected curve 4(-3)BW_T1&2b.

Once the process is done, the measured S-parameters following the four successive measurements are compared, as provided in Figure 145.

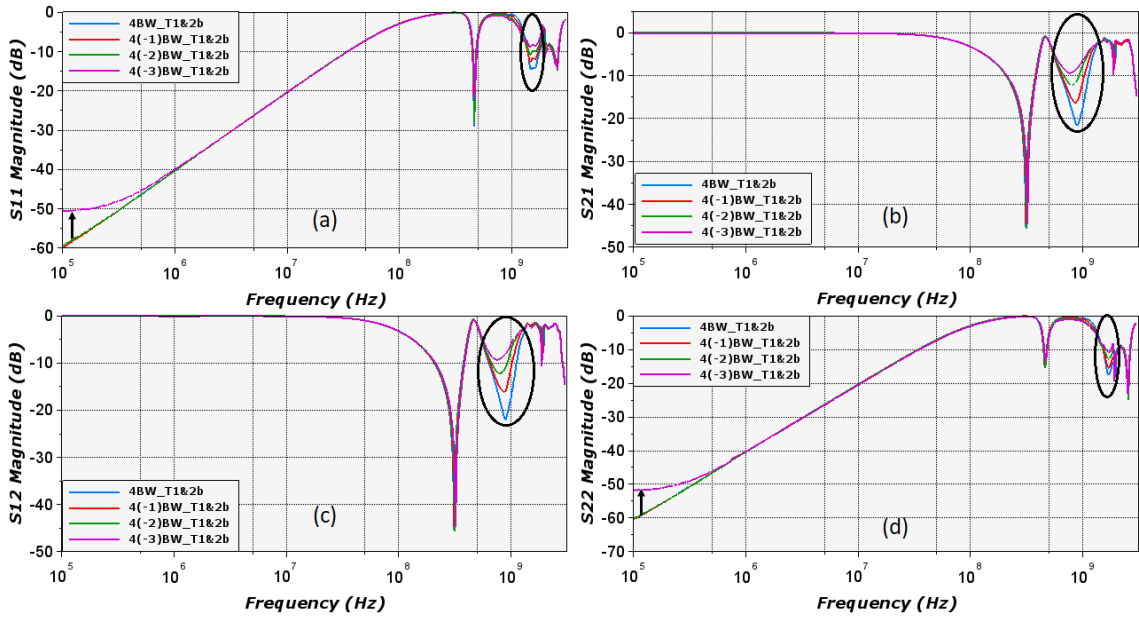


Figure 145: S-parameters magnitude following state of health of bond wire connected between Track 1 and Track 2b

Figure 145 is annotated with black circle, to point-out the noticeable changes of the curves following the state of the health of bond wires. At such resonant frequencies, a significant reduction in magnitude and an eventually shift in frequency is observed following successive measurements. Specially, the changes are pronounced in transmission coefficients. In addition, for the reflection coefficients increase in magnitude is noticed at low frequency and annotated with black arrow in Figure 145 (a & d). Though this change in magnitude is interesting to point out, it appeared for the first time after 3 bond wires lift-off. So, it could not be a good failure indicator. Whereas, the changes marked in black circle provide information for every step of the bond wire lift-off. Therefore, it is interesting to explore the results at high frequency. For the analysis of the results, the transmission parameters (S_{21} or S_{12}) appear to be more representative. Indeed, some variations are observed above 500 MHz specifically, in the bandwidth of 700 MHz to 1.2 GHz. The zoom view of the curves is presented in Figure 146.

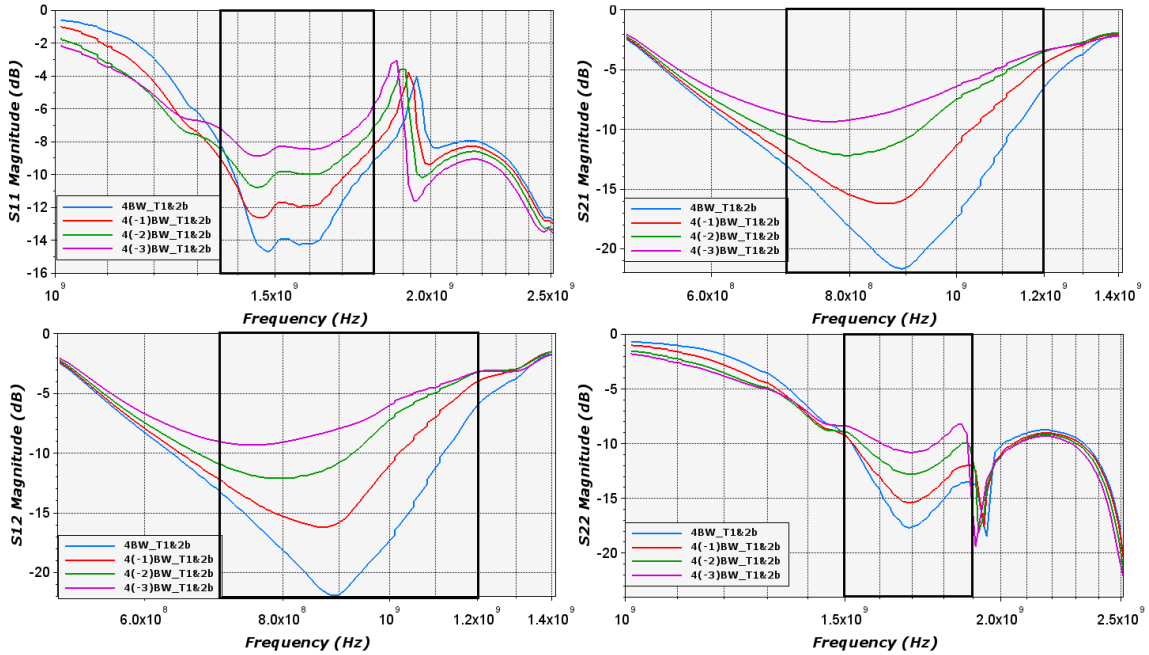


Figure 146: S-parameters magnitude following state of health of bond wire connected between Track 1 and Track 2b zoom view

It can be clearly seen in Figure 146, the shift in frequency and modifications in magnitude highlighted using black box. The shift in frequency following the state of the health of bond wires is listed in Table 19. The percentage is computed considering healthy state as a reference.

Resonance Frequency	Healthy	4 (-1)	4 (-2)	4 (-3)
S ₁₁ curve (GHz)	1.48	1.45	1.45	1.45
% Decrease (S ₁₁ curve)	-	2%	2%	2%
S ₂₁ curve (MHz)	892	846	790	762
% Decrease (S ₂₁ curve)	-	5%	11%	15%
S ₁₂ curve (MHz)	899	861	773	746
% Decrease (S ₁₂ curve)	-	4%	14%	17%
S ₂₂ curve (GHz)	1.69	1.69	1.69	1.69
% Decrease (S ₂₂ curve)	-	0%	0%	0%

Table 19: Resonance frequency and its % decrease following the state of the health of bond wires of a ceramic substrate with bond wires from S-parameters magnitude

S₁₁ and S₂₂ curves experience 2% and 0% of decrease in frequency which is around 30 MHz and 0 MHz, respectively. The transmission coefficients show a significant reduction

in frequency. S_{21} curve experience 5%, 11%, and 15% for 1, 2, and 3 bond wires lift-off which is 46 MHz, 102 MHz, and 130 MHz, respectively. The percentage decrease in frequency of S_{21} and S_{12} are close to each other.

Eventually, Table 20 presents the modification in magnitude at respective resonance presented in Table 19. The percentage increase in magnitude is computed considering healthy state as a reference. The modification in magnitude is pronounced in reflection and transmission coefficients.

Magnitude	Healthy	4 (-1)	4 (-2)	4 (-3)
S_{11} curve (dB)	-14.7	-12.6	-10.8	-8.88
% Increase (S_{11} curve)	-	14%	27%	40%
S_{21} curve (dB)	-21.7	-16.2	-12.2	-9.35
% Increase (S_{21} curve)	-	25%	44%	57%
S_{12} curve (dB)	-21.9	-16.2	-12.1	-9.31
% Increase (S_{12} curve)	-	26%	45%	57%
S_{22} curve (dB)	-17.7	-15.4	-12.8	-10.8
% Increase (S_{22} curve)	-	13%	28%	39%

Table 20: Magnitude and its % increase following the state of the health of bond wires of a ceramic substrate with bond wires from S-parameters magnitude

S-parameters are converted into Z-parameters depicted in Figure 147. Similar to the S-parameters, Z-parameters demonstrate no major changes in the bandwidth 100 kHz to 500 MHz. Some variations are noticed above 500 MHz (highlighted using black box), which are noticeable in transmission coefficients. Therefore, it is interesting to zoom in this bandwidth to explore the data.

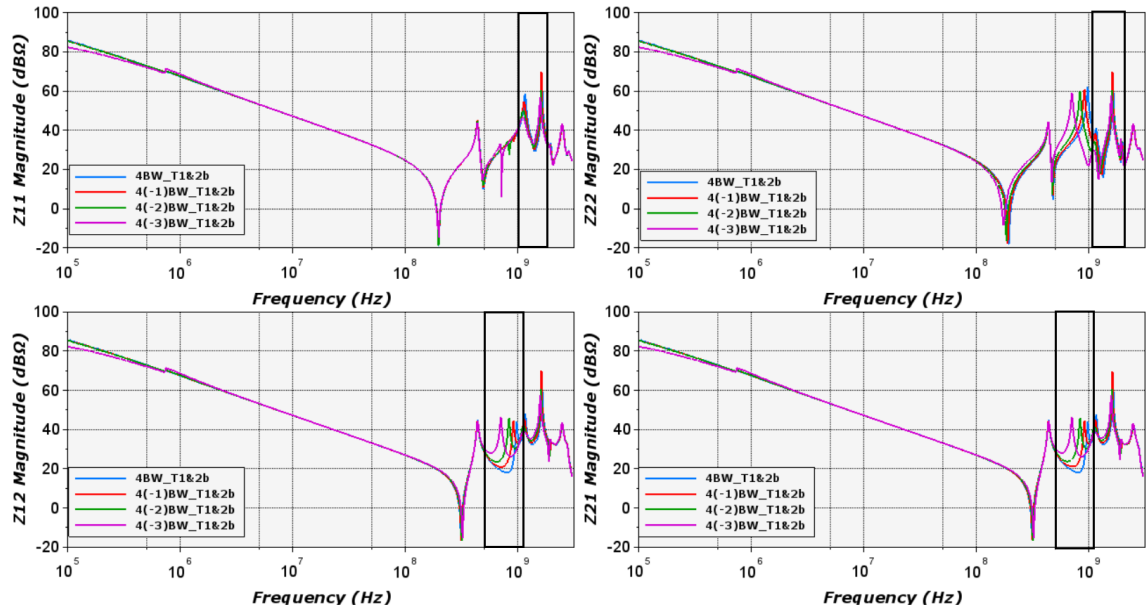


Figure 147: Z-parameters magnitude following state of health of bond wire connected between Track 1 and Track 2b

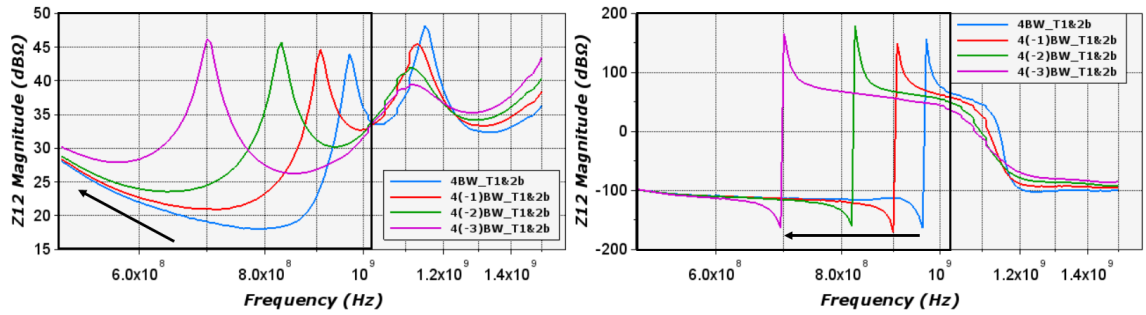


Figure 148: Z_{12} magnitude and phase following the successive measurements

Figure 148 presents the Z_{12} magnitude and phase, it can be clearly noticed a significant decrease in resonance frequency due to inductance changes and in magnitude due to resistance modifications. In the following, Table 21 provides the percentage decrease in resonance frequency recovered from reflection and transmission curves in the highlighted region of Figure 147. The decrease in resonance frequency is more pronounced in transmission parameters (Z_{21} and Z_{12}).

Resonance Frequency	Healthy	4 (-1)	4 (-2)	4 (-3)
Z ₁₁ curve (GHz)	1.39	1.39	1.38	1.37
% Decrease (Z ₁₁ curve)	-	0%	1%	1%
Z ₂₁ curve (MHz)	796	707	640	568
% Decrease (Z ₂₁ curve)	-	11%	20%	29%
Z ₁₂ curve (MHz)	790	712	640	572
% Decrease (Z ₁₂ curve)	-	10%	19%	28%
Z ₂₂ curve (GHz)	1.33	1.28	1.25	1.21
% Decrease (Z ₂₂ curve)	-	4%	6%	9%

Table 21: Resonance frequency and its % decrease following the state of the health of bond wires of a ceramic substrate with bond wires from Z-parameters magnitude

Having 4 bond wires connected in parallel, means that the equivalent inductance can be computed using Eq. 71.

$$\frac{1}{L_{eq}} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} + \frac{1}{L_4} \quad Eq. 71$$

Inducing bond wire lift-off one after the other gradually increases the equivalent inductance, thereby the self-resonating frequency is reduced, for a same parallel capacitance. This increase in magnitude can be justified in a same manner using the equivalent resistance. Table 22 provides the increase in resistance and its percentage following the state of the health of bond wires. The increase in resistance is more pronounced in transmission parameters (Z₂₁ and Z₁₂), almost multiplied by 4 times when three bond wires are lifted-off. A gradual increase in resistance is also noticed on Z₁₁ curve, whereas Z₂₂ shows a sudden decrease in resistance when three bond wires are lifted-off. Therefore, it is convenient to consider transmission parameters to interpret the results in this case.

Resistance	Healthy	4 (-1)	4 (-2)	4 (-3)
Z ₁₁ curve (Ohms)	28.917	31.053	35.979	43.756
% Increase (Z ₁₁ curve)	-	7%	24%	51%
Z ₂₁ curve (Ohms)	7.903	11.329	15.326	25.092
% Increase (Z ₂₁ curve)	-	43%	94%	217%
Z ₁₂ curve (Ohms)	7.923	11.075	15.081	24.847
% Increase (Z ₁₂ curve)	-	40%	90%	214%
Z ₂₂ curve (Ohms)	6.142	7.301	7.752	5.608
% Increase (Z ₂₂ curve)	-	19%	26%	-9%

Table 22: Magnitude and its % increase following the state of the health of bond wires of a ceramic substrate with bond wires from Z-parameters magnitude

4.5.2 Ceramic substrate with IGBT die mounted on Track 2a and connected to other tracks through bond wires

This section demonstrates the two-port characterization of the ceramic substrate with IGBT die with several failure of bonding wires. The bond wire lift-off is induced manually onto the bonding wires connected on Track 2b from top to bottom (as pointed out by the black arrow) as shown in Figure 149.

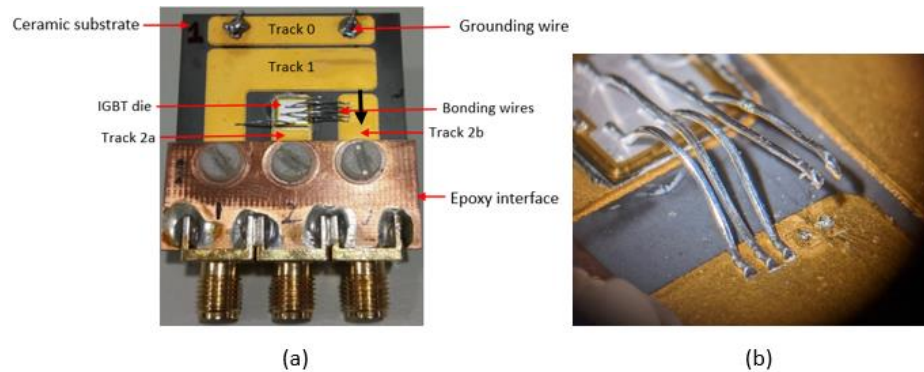


Figure 149: Ceramic substrate with IGBT die and bond wires (a) bond wire lift-off direction (b) after two bond wires lift-off

The failure process is similar to the ceramic substrate with bond wires. As it is performed on Track 2b it is interesting to analyze the results following config1 (gate grounded). S-parameters magnitude measured from 100 kHz to 3 GHz considering config1 are presented in Figure 150.

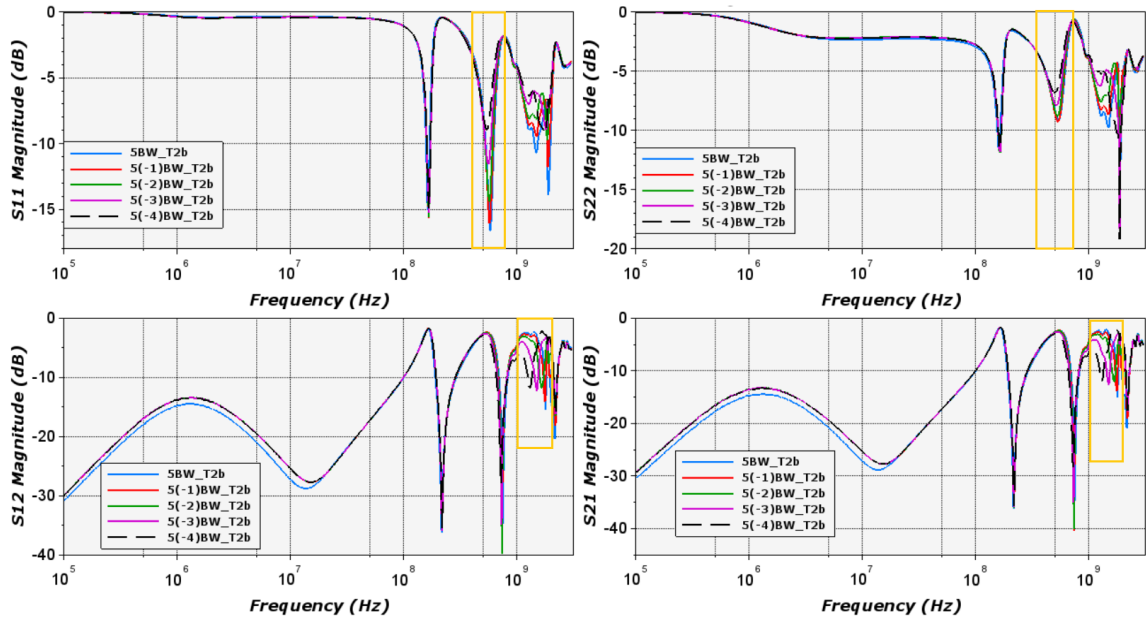


Figure 150: S-parameters magnitude of ceramic substrate with IGBT die following successive measurements

The impact of bond wires lift-off is mainly noticed in the bandwidth of 500 MHz to 700 MHz for reflection parameters and 1 GHz to 1.8 GHz for transmission parameters highlighted with yellow box. Figure 151 presents the zoom view in this bandwidth. A significant decrease in frequencies is observed following the number of bond wires lifted off, indicated with yellow arrow. The decrease in resonance frequencies and its percentage are listed in Table 23.

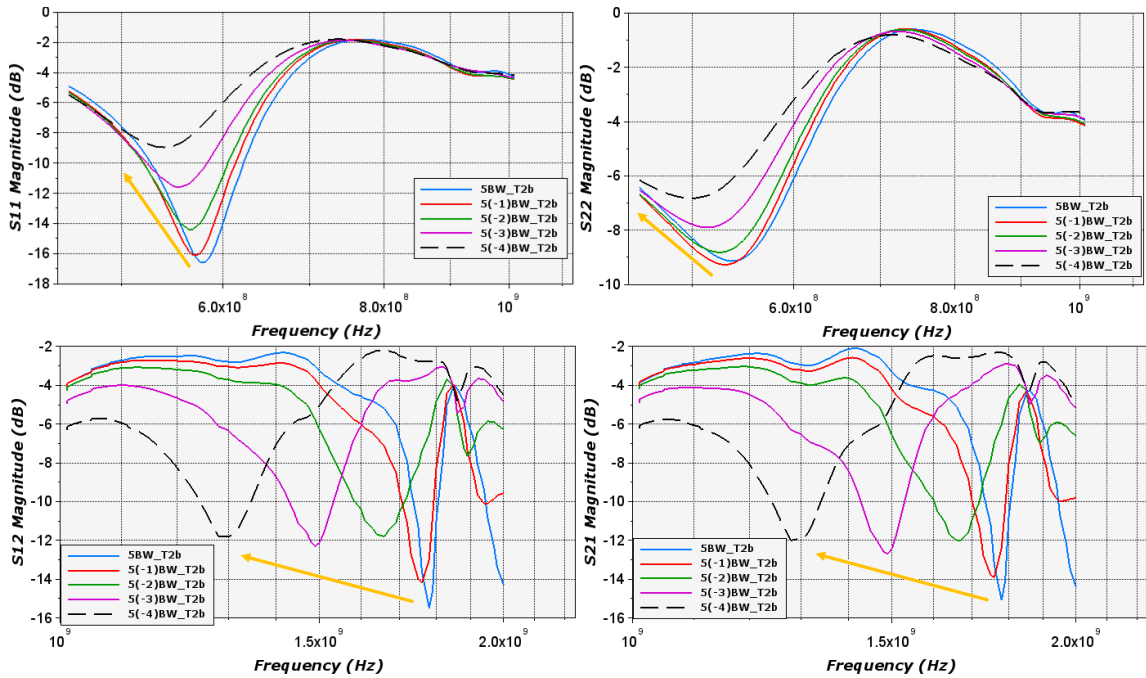


Figure 151: S-parameters magnitude of ceramic substrate with IGBT die following successive measurements

Resonance Frequency	Healthy	5 (-1)	5 (-2)	5 (-3)	5 (-4)
S ₁₁ curve (MHz)	580	568	564	552	54
% Decrease (S ₁₁ curve)	-	2%	3%	5%	7%
S ₂₁ curve (GHz)	1.78	1.76	1.66	1.49	1.28
% Decrease (S ₂₁ curve)	-	1%	7%	16%	28%
S ₁₂ curve (GHz)	1.78	1.76	1.66	1.49	1.28
% Decrease (S ₁₂ curve)	-	1%	7%	16%	28%
S ₂₂ curve (MHz)	536	528	524	516	499
% Decrease (S ₂₂ curve)	-	1%	2%	4%	7%

Table 23: Resonance frequency and its % decrease following the state of the health of bond wires of a ceramic substrate with bond wires and IGBT die from S-parameters magnitude

A significant decrease in frequency resonance of 500 MHz (28%) is noticed between healthy and four bond wires lifted-off in S₂₁ and S₁₂. Likewise, Table 24 presents the increase in magnitude following successive measurements at the resonance frequency mentioned in Table 23. The magnitude modification is pronounced in reflection parameter (S₁₁) by 2 times to the initial values. The transmission parameters show a gradual increase in magnitude.

Magnitude	Healthy	5 (-1)	5 (-2)	5 (-3)	5 (-4)
S ₁₁ curve (dB)	-16.6	-16.1	-14.4	-11.6	-8.96
% Increase (S ₁₁ curve)	-	6%	29%	78%	141%
S ₂₁ curve (dB)	-15.1	-13.9	-12	-12.7	-12
% Increase (S ₂₁ curve)	-	15%	43%	32%	43%
S ₁₂ curve (dB)	-15.5	-14.2	-11.8	-12.3	-11.8
% Increase (S ₁₂ curve)	-	16%	53%	45%	53%
S ₂₂ curve (dB)	-9.14	-9.27	-8.82	-7.9	-6.82
% Increase (S ₂₂ curve)	-	1%	4%	15%	31%

Table 24: Magnitude and its % increase following the state of the health of bond wires of a ceramic substrate with bond wires and IGBT die from S-parameters magnitude

S-parameters are converted into Z-parameters to read the curves in terms of RLC presented in Figure 152. The noticeable changes are highlighted using yellow arrow in Figure 152. The zoom view focusing in this region is presented in Figure 153.

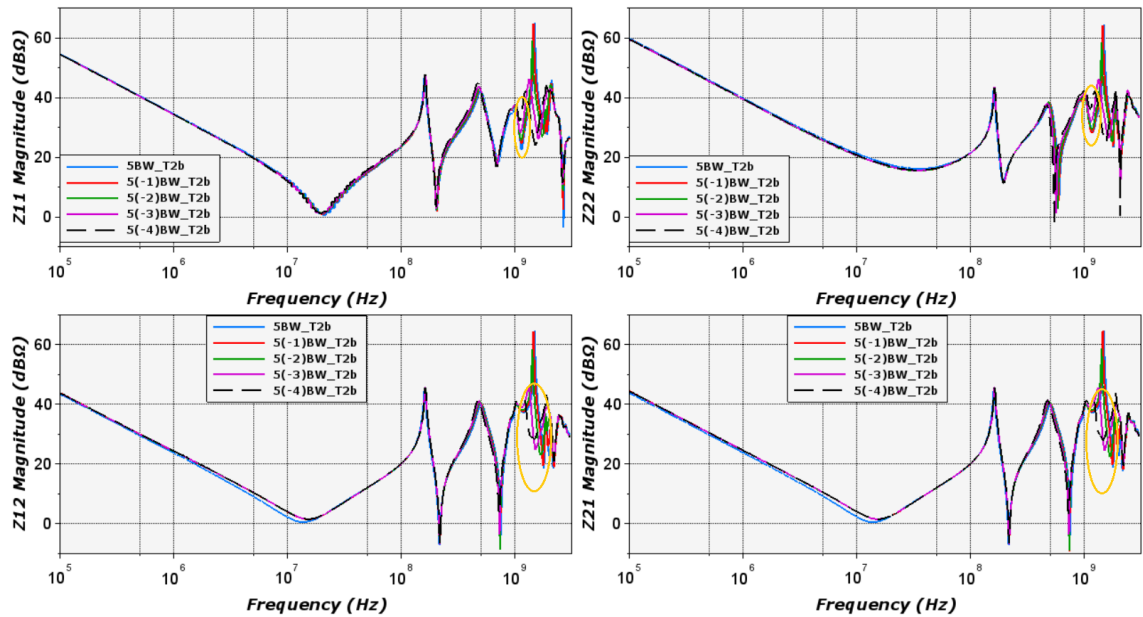


Figure 152: Z-parameters magnitude of ceramic substrate with IGBT die following successive measurements

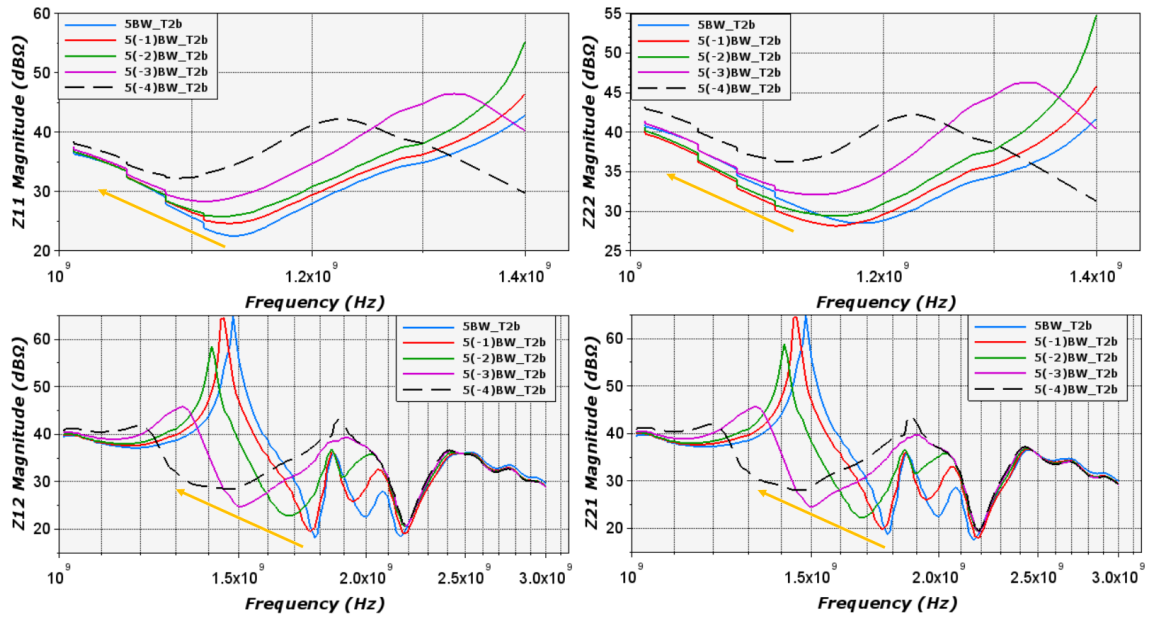


Figure 153: Z-parameters magnitude of homemade packaging with IGBT die following the state of the health of bond wires

The decrease in resonance frequencies is noticed in the bandwidth of 1.2 GHz to 1.8 GHz in Z_{21} and Z_{12} magnitude and from 1 GHz to 1.2 GHz in Z_{11} and Z_{22} magnitude (highlighted with yellow arrow).

Resonance Frequency	Healthy	5 (-1)	5 (-2)	5 (-3)	5 (-4)
Z_{11} curve (GHz)	1.13	1.13	1.12	1.11	1.09
% Decrease (Z_{11} curve)	-	0%	1%	2%	4%
Z_{21} curve (GHz)	1.78	1.76	1.69	1.5	1.45
% Decrease (Z_{21} curve)	-	1%	5%	16%	19%
Z_{12} curve (GHz)	1.78	1.76	1.69	1.5	1.48
% Decrease (Z_{12} curve)	-	1%	5%	16%	17%
Z_{22} curve (GHz)	1.19	1.16	1.16	1.14	1.12
% Decrease (Z_{22} curve)	-	3%	3%	4%	6%

Table 25: Resonance frequency and its % decrease following the state of the health of bond wires of a ceramic substrate with bond wires and IGBT die from Z-parameters magnitude

The increase in resistance following bond wire lift-off action is noted in Table 26. The modification in resistance is highly pronounced in reflection and transmission parameters. The increase in resistance for four bond wires lift-off compared to initial state is multiplied by 3 times for Z_{11} , Z_{21} , and Z_{12} curves and 2.5 times for Z_{22} curve.

Resistance	Healthy	5 (-1)	5 (-2)	5 (-3)	5 (-4)
Z ₁₁ curve (Ohms)	13.421	16.997	19.512	25.844	40.912
% Increase (Z ₁₁ curve)	-	27%	45%	93%	205%
Z ₂₁ curve (Ohms)	8.582	9.680	13.016	16.746	25.153
% Increase (Z ₂₁ curve)	-	13%	52%	95%	193%
Z ₁₂ curve (Ohms)	8.196	9.351	13.787	17.335	26.356
% Increase (Z ₁₂ curve)	-	14%	68%	112%	222%
Z ₂₂ curve (Ohms)	26.651	25.509	29.457	40.355	65.258
% Increase (Z ₂₂ curve)	-	4%	11%	51%	145%

Table 26: Magnitude and its % increase following the state of the health of bond wires of a ceramic substrate with bond wires and IGBT die from Z-parameters magnitude

The modifications are also noticed in phase plots following the state of the health of bond wires in Figure 154.

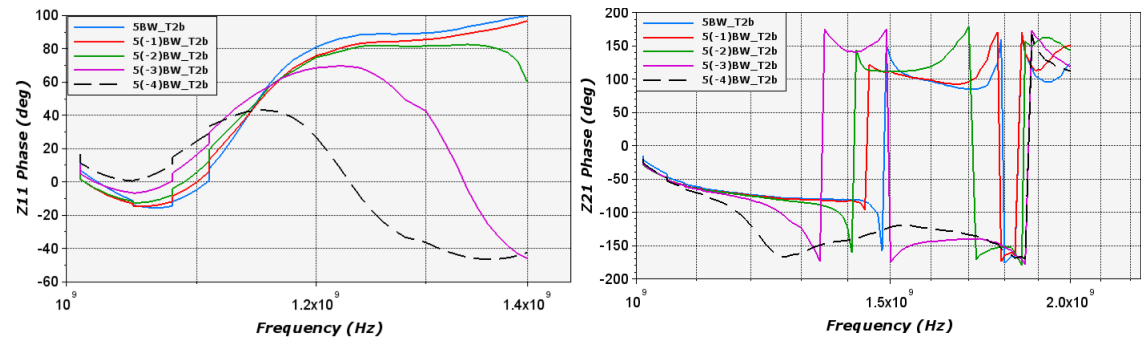


Figure 154: Z₁₁ and Z₂₁ phase plots following successive measurements of ceramic substrate with IGBT die and bond wires

4.5.3 Comparison of healthy and faulty mode ceramic substrate with bond wires and IGBT die polarized:

This section demonstrates the healthy and faulty (four bond wires lifted-off) state by polarizing the IGBT die. The polarization is performed with the values $V_{com} = 15\text{ V}$, $V_{dc} = 15\text{ V}$, and measurements are made for $I_c = 100\text{ mA}$ and 2 A . Figure 155 presents the measurement curves focusing in the reduced bandwidth (3 MHz to 1GHz) for which bias tee has no influence. The comparison of healthy and faulty mode by polarizing the die present some variation above 300 MHz (highlighted with blue box), while the curves are superposed below 300 MHz. The comparison curves show variations with shift in frequency in the bandwidth that is highlighted.

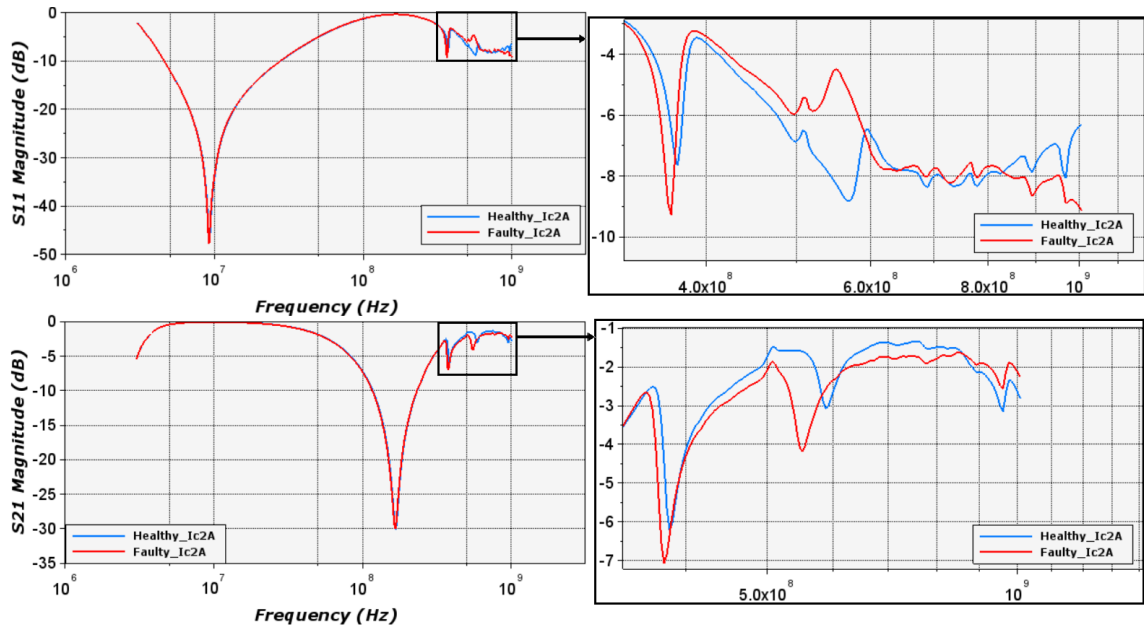


Figure 155: S_{11} and S_{21} measurement between collector and emitter of ceramic substrate with IGBT die in healthy and faulty mode in bandwidth (3 MHz – 1 GHz)

The modifications in frequency and magnitude are listed in Table 27 and Table 28, respectively. Following these experiments, the smooth shift in frequency and change in magnitude behavior seems to be a representative of failure detection.

Resonance frequency	Healthy	Faulty 5 (-4)
S_{11} curve (MHz)	568	551
% Decrease (S_{11} curve)	-	3%
S_{21} curve (MHz)	588	552
% Decrease (S_{21} curve)	-	6%
S_{22} curve (MHz)	373	364
% Decrease (S_{22} curve)	-	2%

Table 27: Resonance frequency and its % decrease following the state of the health of bond wires of a ceramic substrate with bond wires and IGBT die (polarized) from S-parameters magnitude

Magnitude	Healthy	Faulty 5 (-4)
S ₁₁ curve (dB)	-8.83	-4.48
% Increase (S ₁₁ curve)	-	49%
S ₂₁ curve (dB)	-3.06	-4.19
% Decrease (S ₂₁ curve)	-	37%
S ₂₂ curve (dB)	-7.86	-6.80
% Increase (S ₂₂ curve)	-	13%

Table 28: Magnitude and its % change following the state of the health of bond wires of a ceramic substrate with bond wires and IGBT die (polarized) from S-parameters magnitude

S-parameters are converted into Z-parameters and illustrated in Figure 156.

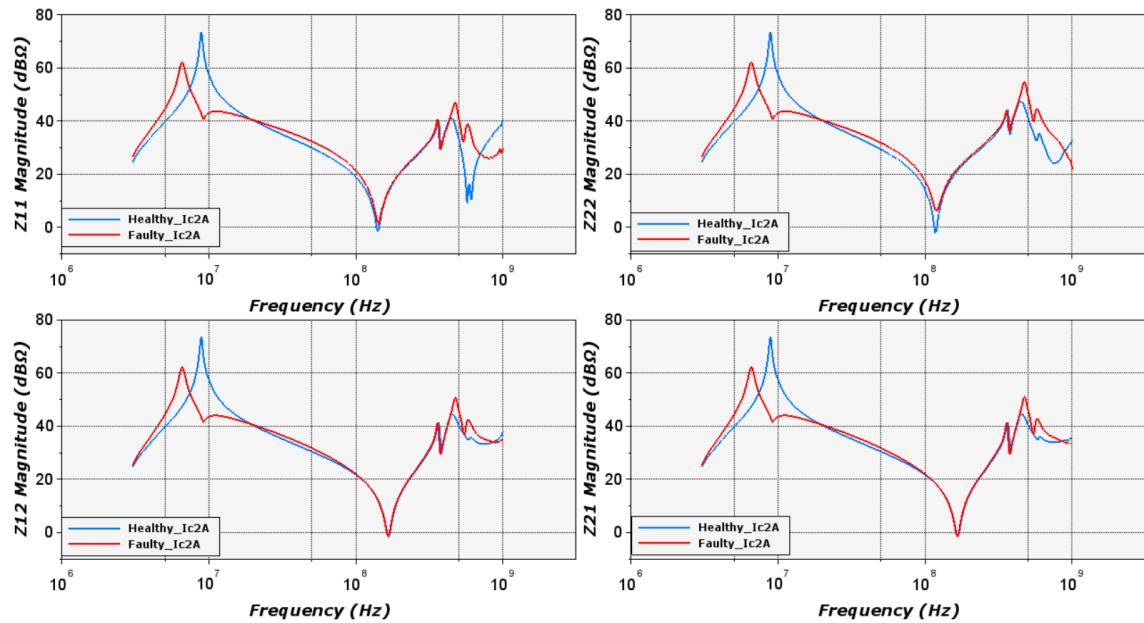


Figure 156: Z-parameters magnitude between collector and emitter of ceramic substrate with IGBT die in healthy and faulty mode in bandwidth (3 MHz – 1 GHz)

Due to the change in the shape of all Z-parameters, the bond wire failure is well identified both at low frequency (<10 MHz) and at high frequency (some hundreds of MHz). Whereas, this first attempt have only been done at healthy and after 4 bond wires lifted-off. Therefore, it is difficult to quantify the changes because the trend of intermediate states is not available.

4.5.4 Active Power Cycling (APC) test on TO-247 SiC MOSFET

An Active Power Cycling test was chosen to activate the damage mechanisms in the assemblies. The principle described in Figure 130, is to induce periodic heating of the component by circulating a current whose intensity and duration are initially adjusted, in order to obtain a controlled variation in the temperature measured at the assembly. TO-247 SiC MOSFET, (part number: C2M0160120D) is considered to perform APC test, whose healthy state characterization followed by electrical equivalent model was detailed in Chapter 3 Section 3.2. The electrical parameters of the component are presented in Table 29. The values applied for accelerated component aging are summarized in Table 30.

Parameters	Ratings	Unit
Device	TO-247 (SiC MOSFET)	-
V_{DSmax}	1200	V
V_{GSmax}	-10/+25	V
I_D	18	A
$V_{GS(th)}$	4	V

Table 29: Electrical parameters of TO-247 SiC MOSFET (C2M0160120D)

Parameters	Ratings	Unit
Cycling current	20	A
T_{Jmax}	150	°C
T_{Jmin}	20	°C
ΔT_J	130	°C
T_{on}	1	s
T_{off}	1.5	s

Table 30: Values applied to the aging test

The desired temperature variation, $\Delta T_J = 120\text{ }^\circ\text{C}$, places a high load on the packages' internal interconnect elements, such as bonding wires and solder joints [119], [120]. The test implemented stresses the component's internal power diode: the component is negative biased (detailed in Section 4.5.4.1). The current value applied complies with the manufacture's specifications for the chosen reference. Each cycle consists of 1 second of

heating followed by 1.5 seconds of cooling, ensuring that the device adequately cools down before the subsequent heating pulse.

4.5.4.1 Device under test and test setup

Active power cycling test setup is shown in Figure 157, with three TO-247 SiC MOSFETs. For the testing phase, the components are fixed onto a temperature stabilized cold plate with water cooling. As the drain of the transistor is connected to the backside of the TO-247 packages, it is necessary to insulate them from direct. Indeed, thermal gap pads (GP300S) are placed between the heat sinks of the packages and the cold plate as depicted in Figure 157 (green color pad under each device).



Figure 157: APC test setup

The test can be operated in two modes: transistor mode or diode mode. For easier handling, diode mode (i.e., body diode of the MOSFET) is frequently employed instead of the transistor mode. This way the trapping effect of the transistor can also be avoided. Therefore, a negative voltage of -4 V is supplied to V_{GS} , which push the diode into conduction while blocking the transistor. The on voltage drop at the applied heating current (V_{on}) is used as a failure indicator for this test. In our case, the device under test is characterized (VNA, B1505A) before and after APC test to see the impact of aging.

As this test is mainly targeted to see bond wire lift-off, to have an internal view of the TO-247 SiC MOSFET (C2M0160120D) one of the devices (not participating in the test) was mechanically open, as illustrated in Figure 158. It presents 1 bond wire for the gate pad and 4 bond wires divided in two blocks and attached to the source. The underside of the chip is soldered on the substrate and finally, to the external drain terminal.

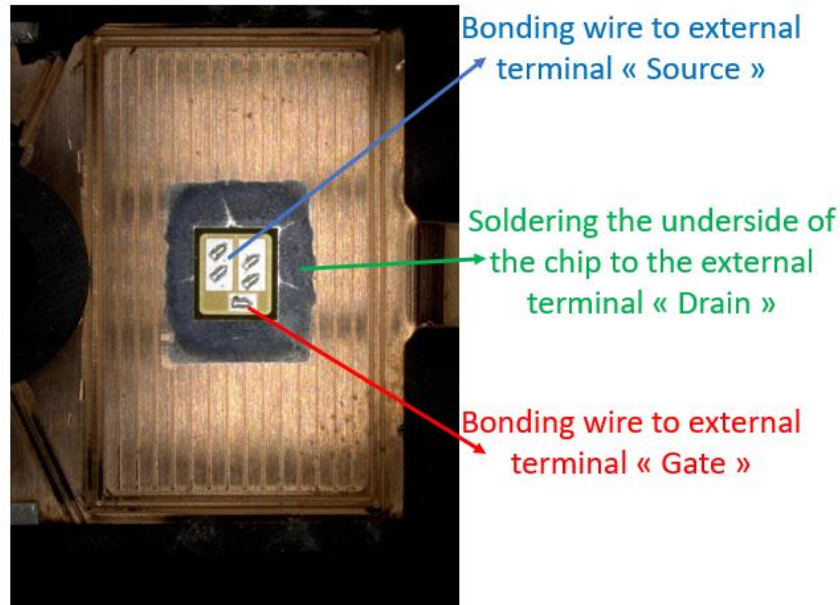


Figure 158: TO-247 SiC MOSFET (C2M0160120D) internal view

Two campaigns which are referred as Group1 and Group2 were achieved. The respective devices of each group participated in APC test are listed in Table 31.

Group1	Group2
G24	C24
K24	E24
I24	O24

Table 31: Device under test for APC test

Concerning the APC test conducted on Group1, after 19796 cycles, the test was automatically stopped, indicating a huge rise on V_{on} monitoring parameter of I24. Therefore, the sample I24 was removed from the test bench and continued the test with G24 and K24 until 22830 cycles. At 22830 cycles the test was intentionally stopped due to availability of the test bench. The failure indicator, namely the voltage drop (V_{on}) is presented in Figure 159. This figure presents the different step-wise changes of V_{on} for each device of Group1. In situations where devices are exposed to heat in an open state, the gradual alteration in device voltage results from the degradation of device characteristics and the propagation of cracks in the bond wires. Conversely, rapid fluctuations occur due to increased serial ohmic resistance resulting from the detachment or breakage of individual bond wires [119]. When one or few bond wires fail, it disrupts

the current distribution within power devices, accelerating the wear-out failure of the remaining bond wires. Ultimately, this cascade effect can lead to open-circuit failures or catastrophic failures in power devices, such as thermal runaway or chip destruction.

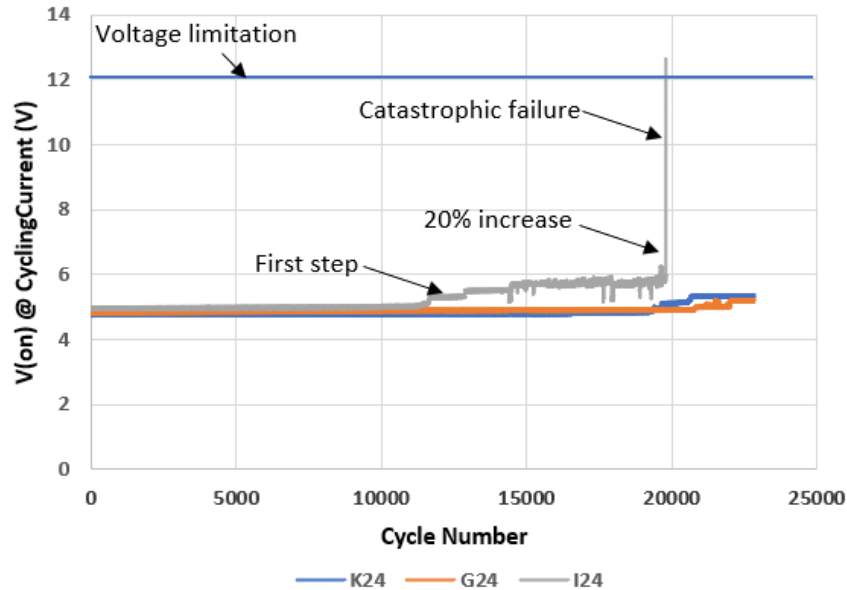


Figure 159: voltage drop on the device at heating current level as a function of applied power cycles of Group1 devices

Device I24 experienced smaller step changes and catastrophic failure. Also, K24 and G24 experienced smaller step changes. The initial steps appear relatively smaller because the overall resistance of the parallel bond wires experiences only a slight shift due to the rupture of just one of them. However, as the number of bond wires decrease, the proportional change in resistance becomes significantly more pronounced, leading to larger step increments. Table 32 presents the percentage increase in resistance, computed for each step changes of V_{on} of three devices for constant cycling current of 20 A. Percentage is computed by considering V_{on} at 4000 cycles as a reference value. It is because at 4000 cycles, no device shows any step-wise changes as illustrated in Figure 159.

Device	Cycle numbers	V _{on} (V)	Resistance (Ω)	% Increase (Resistance)
I24	4000	4.984	0.249	-
	12400	5.315	0.266	7%
	13610	5.507	0.275	11%
	17290	5.663	0.283	14%
K24	4000	4.783	0.239	-
	18100	4.842	0.242	1%
	20464	5.146	0.257	8%
	22840	5.349	0.267	12%
G24	4000	4.851	0.243	-
	13000	4.897	0.245	1%
	20797	4.95	0.247	2%
	22840	5.195	0.260	7%

Table 32: Percentage increase in resistance of Group1 devices for each step of V_{on}

After 19796 cycles, the Von curve of I24 reach the voltage limitation (12 V) of the channel to which I24 is connected. Towards the end, it becomes challenging to differentiate between individual bond wire failures as the overload destroys the remaining bonds following the earlier failures. This could explain the specific behavior of Von curve for the last step-wise change. The devices underwent Scanning Acoustic Microscopy (SAM) to validate the findings delivered from electrical measurements. Figure 160 shows the SAM pictures of the three devices of Group1 after aging. Unfortunately, a baseline SAM measurement prior to the power cycling test were not captured. Consequently, a direct comparison with the initial state using the captured images is unattainable. Nonetheless, Figure 158 can serve as a reference point for identifying the bond wires that are connected to the chip. Whereas it becomes difficult to comment on brazing as they cannot be compared to the initial state.

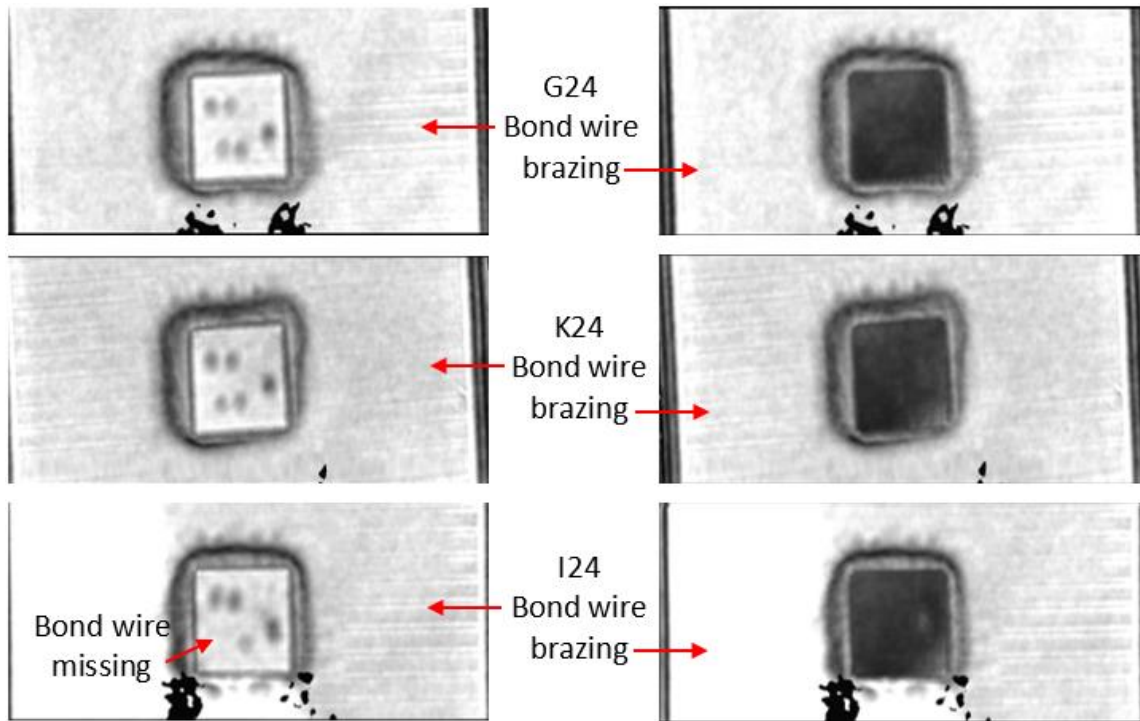


Figure 160: SAM images highlighting bond wire and brazing connection after aging of three devices of Group1

By effectively processing the recorded transient data, it becomes possible to identify the time constant inherent in the curve, enabling the creation of a one-dimensional Cauer RC model for the system. This model incorporates thermal resistance (R_{th}) and thermal capacitance (C_{th}). The formation of a cumulative structure function involves plotting cumulative thermal resistances along the horizontal axis and cumulative thermal capacitance along vertical axis. The cumulative structure function encapsulates valuable insights into the physical packaging structure, facilitating the detection of issues like delamination or degradation [119]. Figure 161 shows the structure function of Group1 devices. The initial state of the structure function was captured before the cycling (i.e., at 0 cycles) in brown color. Likewise, 4000 cycles (red color), 8000 cycles (yellow color), 12000 cycles (light blue color), and 14415 cycles (navy blue color) were also captured and compared with initial state. These curves continue to exhibit a good fit up to approximately 1 K/W, with any disparities becoming noticeable only beyond this thermal resistance threshold. This provides compelling evidence that no alterations occurred in the examined packages' structure. The devices' failure can only be attributed to bond wire degradation rather than any structural modifications.

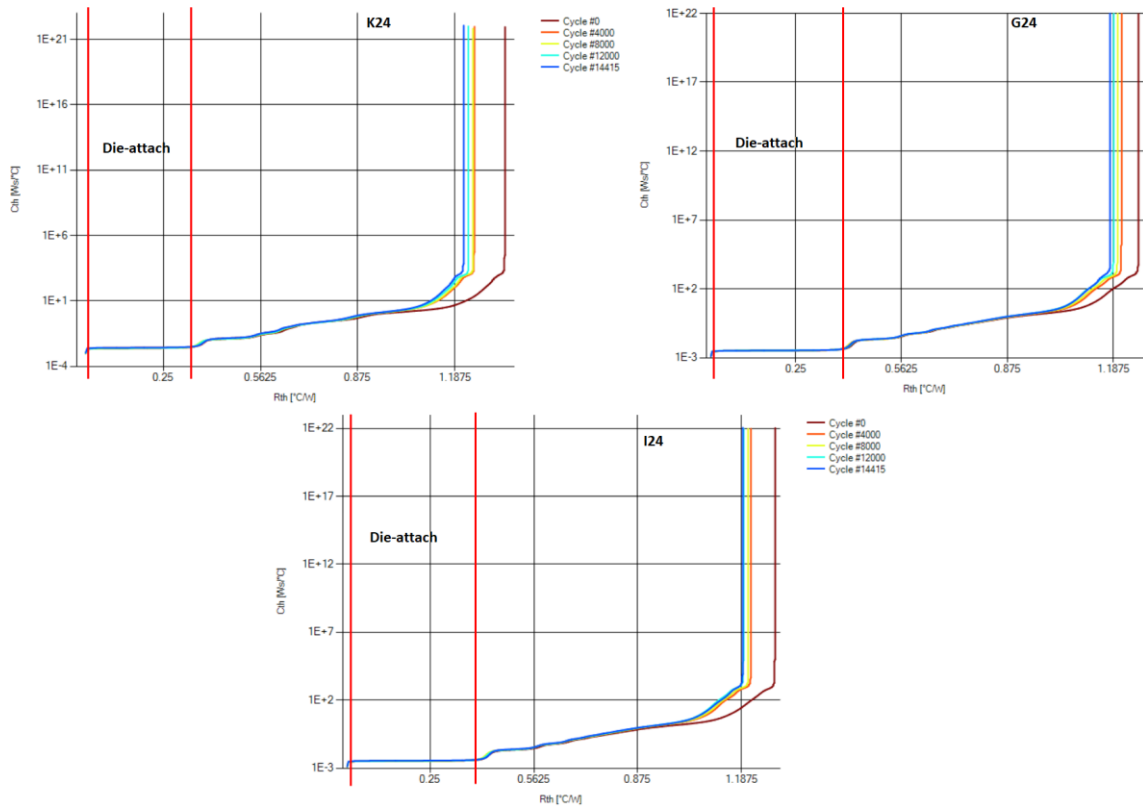


Figure 161: Structure function of Group1 devices for different aging cycles

The V_{on} graph (Figure 159) of each device of Group1 shows the complete failure of I24 and smaller step changes on G24 and K24. Whereas, the SAM results show one bond wire missing on I24 and recovers all bond wire connection of G24 and K24. This could be due to the formation of bond wire cracks or bond wire lift-off at pad level. It is difficult to identify these cracks and bond wire lift-off at pad level (due to material constraints) from SAM results.

The VNA characterization was performed before and after aging on the three devices following three possible configurations. The results are analyzed highlighting the best configurations. The S-parameters magnitude comparison of three devices of Group1 before and after cycling where port 1 and port 2 are connected to drain (D1) and source (S2) respectively while gate terminal is grounded (GCOM) are shown in Figure 162. The S-parameters magnitude presented in Figure 162 in complete bandwidth (100 kHz to 3GHz) allows to point out the visible changes following the aging test compared with their original state (before aging).

Firstly, considering the device I24, which is believed to be completely failed based on V_{on} online monitoring parameter, shows visible changes in all the S-parameters' curves given in Figure 162. It is interesting to take a look first to Figure 162 (d) source connected port. A complete reflection from 100 kHz to 1 GHz is recovered (highlighted with black box).

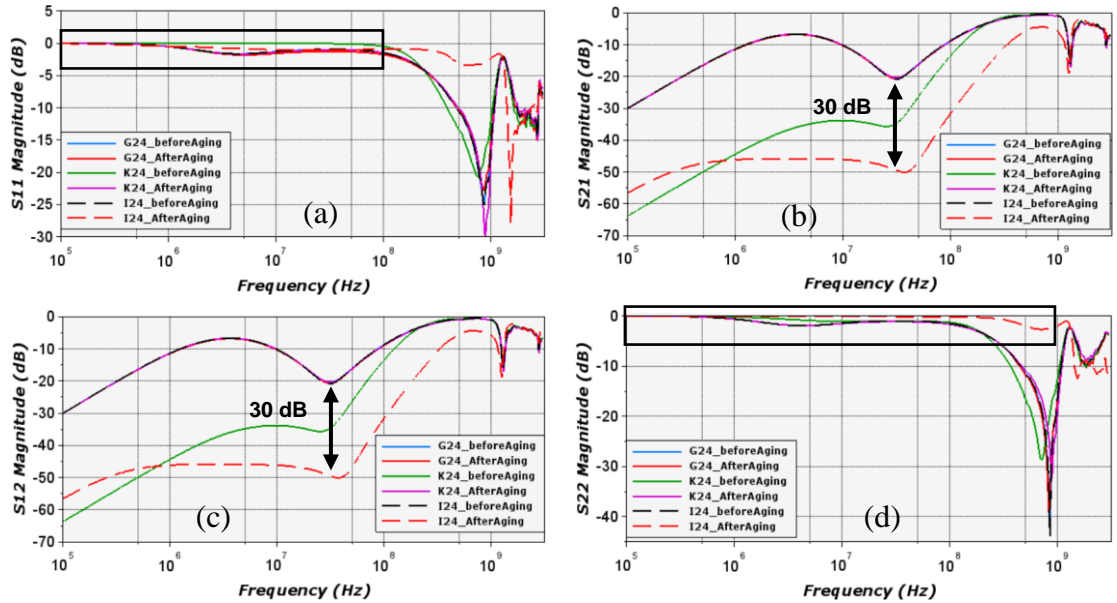


Figure 162: S-parameters magnitude of Group1 devices before and after aging following configuration GCOM (DIS2)

The reflection parameter on port 1 (Figure 162 (a)), the drain connected port recovers almost similar characteristics compared to healthy state curves (highlighted with black box). However, the impact is seen after 100 MHz in Figure 162 (b). The transmission parameters (Figure 162 (b & c)) after aging falls to 30 dB confirms the “open circuit” condition.

The S-parameters are converted into Z-parameters and are presented in Figure 163. The source connected port (Z_{22} magnitude) of I24 experience a huge shift in first resonance indicated with black box. The phase of this parameter (Z_{22} phase) provides the fact that inductive behavior of healthy state becomes capacitive for faulty state. On the other hand, the Z_{11} magnitude and phase (drain connected port) of I24 exhibit no changes from 100 kHz to 200 MHz. Some variations are seen above 200 MHz.

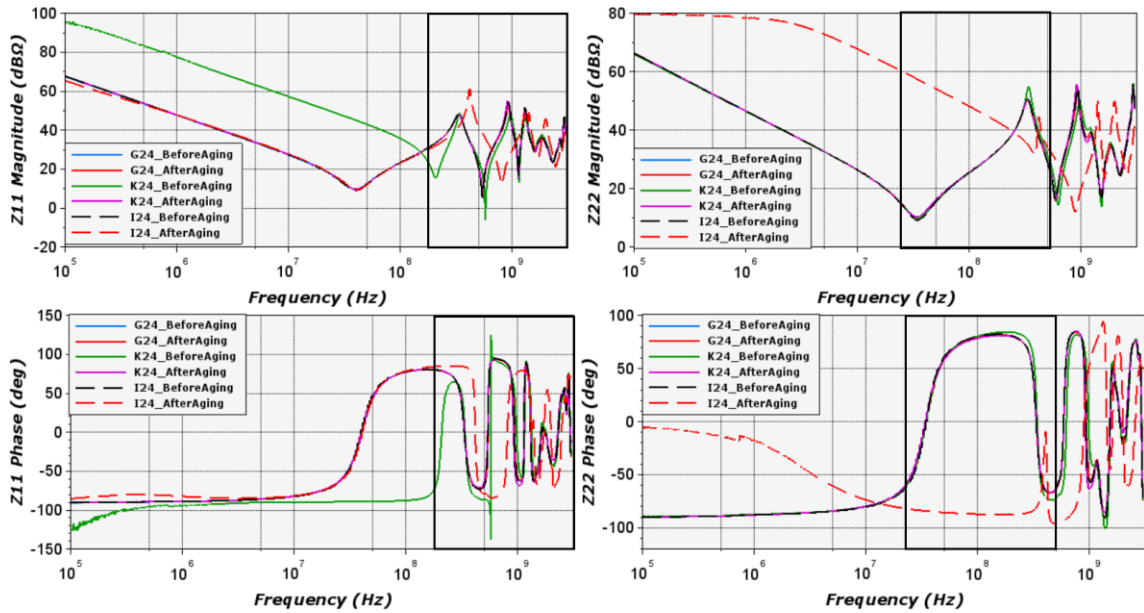


Figure 163: Reflection parameters magnitude and phase of Group1 devices before and after aging following configuration GCOM (D1S2)

In both the figures, Figure 162 and Figure 163, device K24 shows specific behavior before aging. This led us to think about two possibilities: it could be due to manufacturing defect as it is seen before aging otherwise due to measurement error. It is strongly believed that it is due to measurement error due to following reasons:

- After aging curves of K24 perfectly fits with curves of other device when no failure is detected. If considered Figure 162 (S_{11} magnitude) though the difference in magnitude (after aging of K24) at the first resonance is observed, this difference is neither observed on transmission parameters nor on S_{22} .
- This behavior of K24 before aging is not observed in the other configurations.

The change in behavior of K24 in Z_{11} (drain connected port) is more pronounced, while the change disappeared on Z_{22} . This can lead to a question, is there any early defect due to brazing of die on the substrate? If it is so, the impact is mainly observed on capacitance. The capacitance measurement performed on B1505A curve tracer before and after aging are presented in Figure 164. These results show no change of capacitance for all the devices before and after aging except for I24 after aging. The first conclusion is the confirmation of measurement error hypothesis regarding K24 device. The second and interesting conclusion is that, as all the devices exhibit similar characteristics if not

complete failure is detected, it is difficult to identify any intermediate changes using B1505A CV measurements.

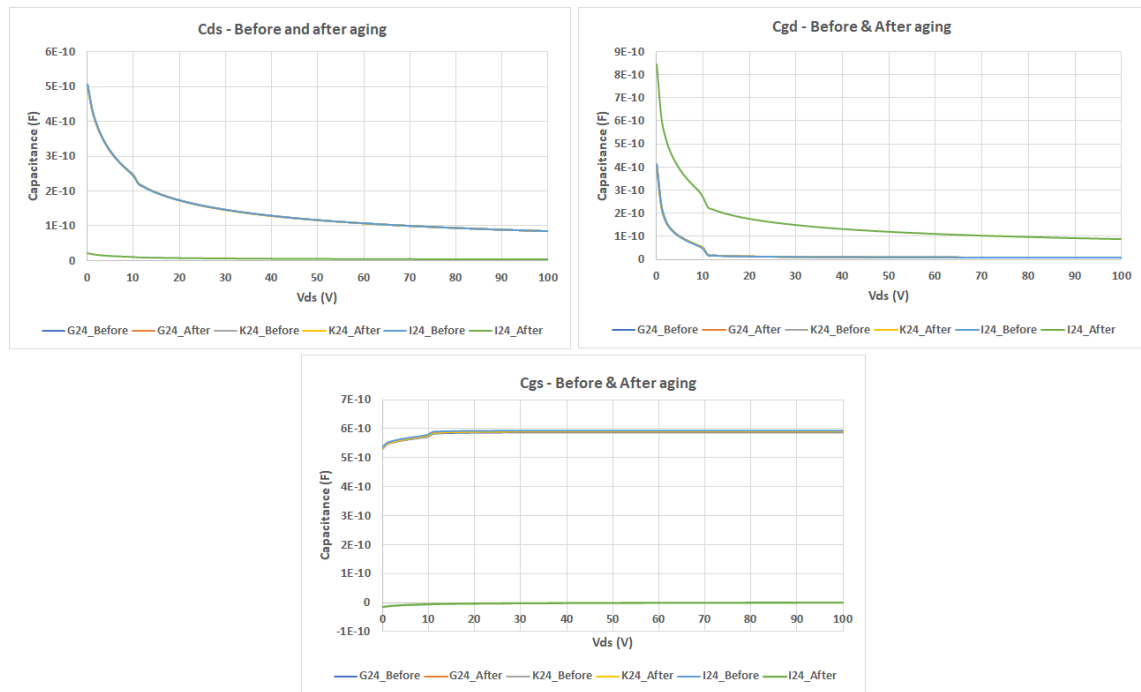


Figure 164: CV measurements on B1505A curve tracer of Group1 devices before and after aging

The other interesting two-port VNA configurations to be discussed is gate connected to port 1 (G1) and drain connected to port 2 (D1) while source is grounded (SCOM) whose equivalent impedance model is given in Figure 165.

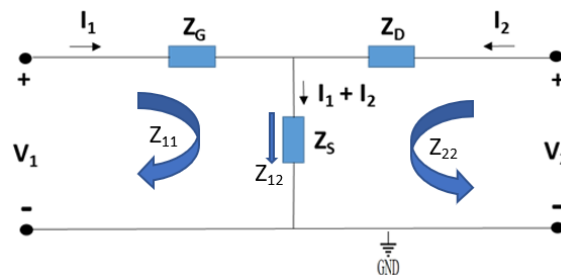


Figure 165: Two-port impedance model representing the configuration SCOM (G1D2)

The comparison of Z-parameters magnitude of Group1 devices before and after aging following this configuration is shown in Figure 166. It is interesting to point out, as the source terminal is grounded and is involved in reflection behavior thereby any impact due to source is expected to be visible on every parameter presented in Figure 166. The impact on I24 after aging is clearly visible while the other curves are superposed. Whereas a

significant change in impedance magnitude is observed at the self-resonating frequency, specifically on transmission parameters highlighted in Figure 167.

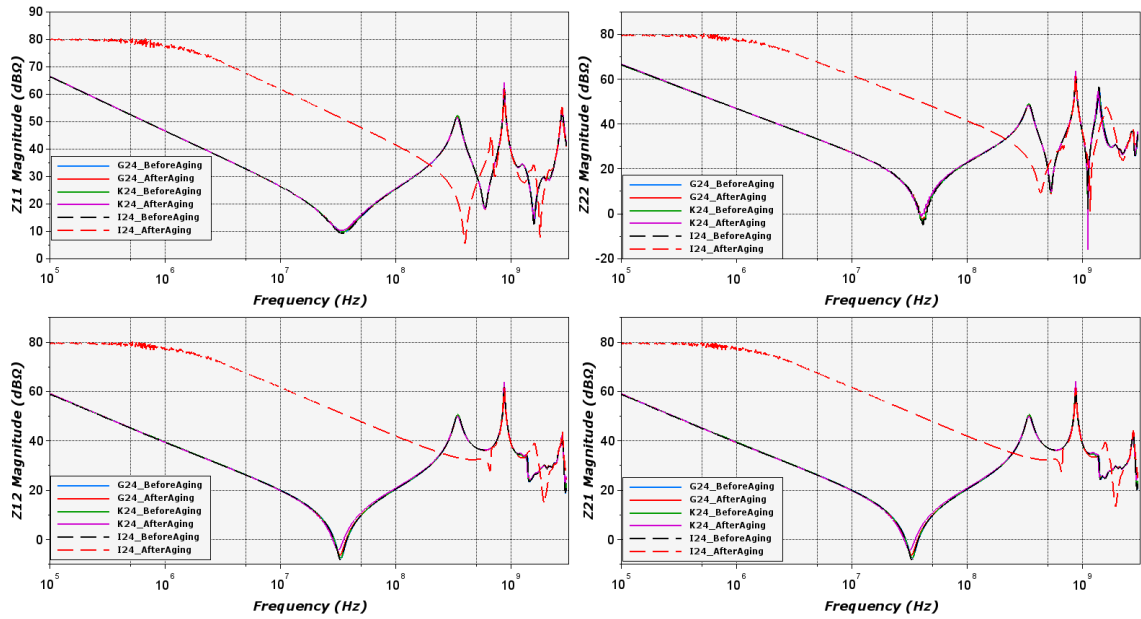


Figure 166: Z-parameters magnitude of Group1 devices before and after aging following configuration SCOM (G1D2)

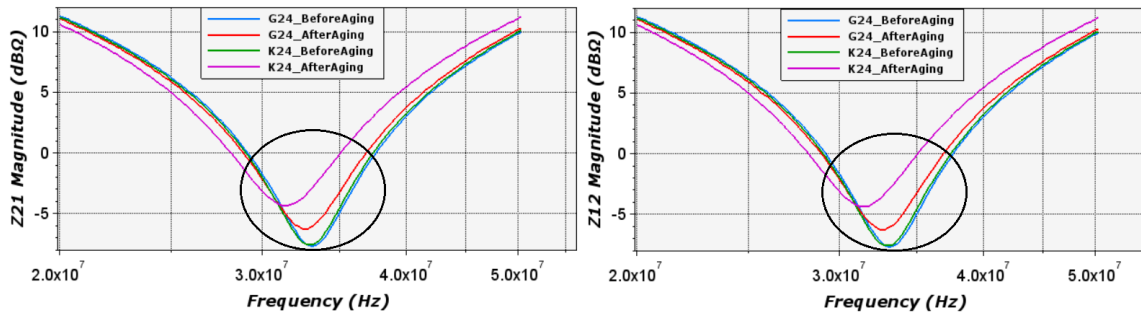


Figure 167: Z-parameters magnitude of Group1 devices before and after aging following configuration SCOM (G1D2) in bandwidth 20 MHz-50 MHz

It is clearly observed, the increase in resistance after aging for all the three devices. As the difference is quite visible for I24, the increase in resistance and its percentage of K24 and G24 after aging compared to before aging is given in Table 33. To point out that, G24 and K24 curves before aging are superposed. The percentage increase in resistance after aging for G24 and K24 curves is 18% and 46%. This shows a significant change in resistance. On the other hand, no huge shift in frequency is measured as depicted in Table 34.

Parameters		G24	K24
Z_{11} (Ω) (R_g+R_s)	$Z_{11}(\text{before})$	3.019	3.076
	$Z_{11}(\text{after})$	3.076	3.248
	$Z_{11}(\text{after}) - Z_{11}(\text{before})$	0.057	0.172
	% Increase	2%	6%
Z_{12} (Ω) R_s	$Z_{12}(\text{before})$	0.412	0.418
	$Z_{12}(\text{after})$	0.486	0.609
	$Z_{12}(\text{after}) - Z_{12}(\text{before})$	0.073	0.191
	% Increase	18%	46%
Z_{22} (Ω) (R_d+R_s)	$Z_{22}(\text{before})$	0.607	0.628
	$Z_{22}(\text{after})$	0.689	0.898
	$Z_{22}(\text{after}) - Z_{22}(\text{before})$	0.082	0.270
	% Increase	14%	43%

Table 33: Increase in resistance of K24 and G24 after aging extracted from Z_{11} , Z_{12} , and Z_{22} following SCOM (G1D2) configuration

Parameters		G24	K24
f_{11} (MHz) (Resonance Frequency from Z_{11} curve)	$f_{11}(\text{before})$	34.935	34.634
	$f_{11}(\text{after})$	34.935	34.031
	$f_{11}(\text{after}) - f_{11}(\text{before})$	0	0.602
	% Decrease	0%	2%
f_{12} (MHz) (Resonance Frequency from Z_{12} curve)	$f_{12}(\text{before})$	33.127	33.428
	$f_{12}(\text{after})$	32.825	31.832
	$f_{12}(\text{after}) - f_{12}(\text{before})$	0.302	1.596
	% Decrease	1%	5%
f_{22} (MHz) (Resonance Frequency from Z_{22} curve)	$f_{22}(\text{before})$	41.565	40.661
	$f_{22}(\text{after})$	41.565	40.36
	$f_{22}(\text{after}) - f_{22}(\text{before})$	0	0.301
	% Decrease	0%	1%

Table 34: Decrease in resonance frequency of K24 and G24 after aging extracted from Z_{11} , Z_{12} , and Z_{22} following SCOM (G1D2) configuration

Following this configuration, the respective resistance can be extracted are R_g+R_s from Z_{11} curves, R_s from Z_{12} curve, and R_d+R_s from Z_{22} curves. This increase in resistance

could mean crack propagation in bond wires or start of lift-off not visible on SAM results, but visible using V_{on} monitoring parameter.

The IV characteristics of diode and transistor of each device before and after cycling are presented in Figure 168. It is noted that, B1505A IV characteristics measure V_{drain} as a function of I_{drain} for applied V_{gs} voltage. Both the curves show significant change before and after aging for the devices G24 and K24. I24 after aging allow no more current which is seen on IV diode characteristics. Due to constraint on V_{gs} , the I_{drain} and V_{drain} of transistor provide only a single point close to zero which is not visible in the IV transistor curve.

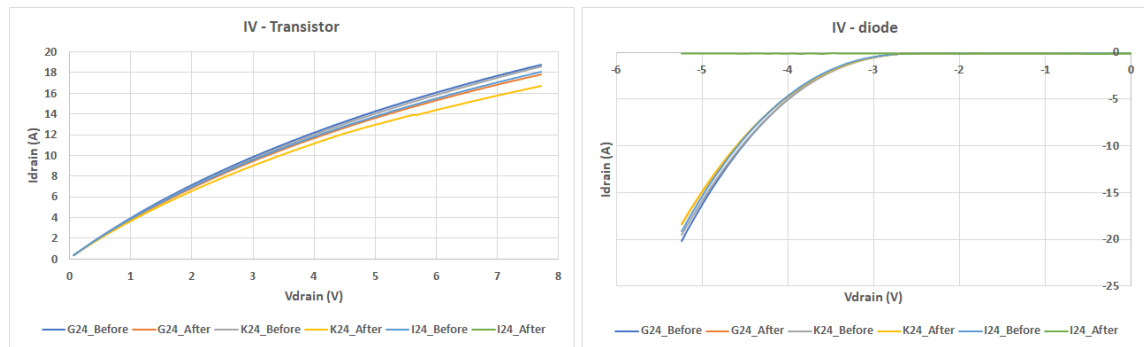


Figure 168: IV characteristics of transistor and diode of Group1 devices before and after aging

Likewise, another test has been launched on the Group2 devices, whose identifications are given in Table 31. The test was intentionally stopped due to scheduling of the Mentor Graphics, by which all the three devices experienced 26954 cycles. Figure 169 presents the V_{on} online monitoring and SAM images after aging of Group2 device. The V_{on} curve presents sudden and high step on E24 and smaller step on C24 and O24. Whereas, SAM images show bond wire connection on C24 and E24 after aging and a typical image of O24. These results are verified with the VNA and B1505A characterization results. Eventually, Table 35 presents the percentage increase in resistance at each step of V_{on} for constant power cycling current of 20 A. C24 and O24 measure change of 1% for the first step. E24 measure 1% and 4% for the first step and at end of the curve for the next step.

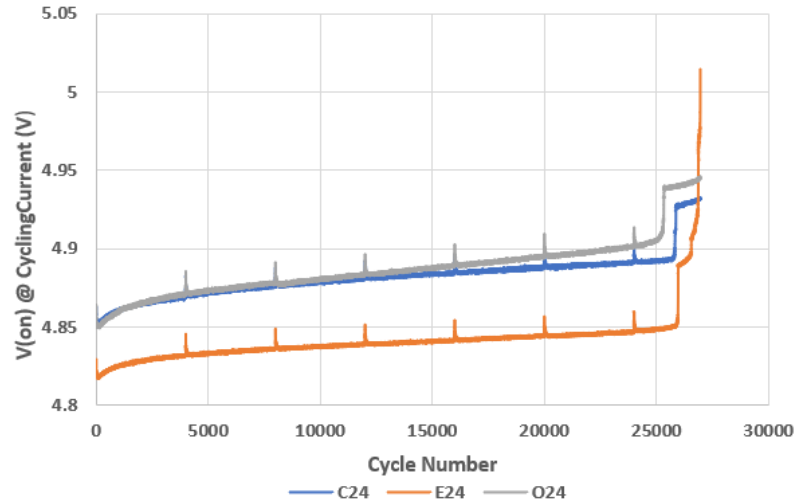


Figure 169: voltage drop on the device at heating current level as a function of applied power cycles of Group2 devices



Figure 170: SAM images highlighting bond wire connection after aging of three devices of Group2

Device	Cycle numbers	V_{on}	Resistance (Ω)	% Increase (Resistance)
C24	5000	4.871	0.244	-
	26852	4.931	0.247	1%
E24	5000	4.833	0.242	-
	26500	4.895	0.245	1%
	26954	5.015	0.251	4%
O24	5000	4.874	0.244	-
	26080	4.939	0.247	1%

Table 35: Percentage increase in resistance of Group2 devices for each step of V_{on}

As presented for Group1, one of the interesting configurations of VNA characterization is SCOM (G1D2). The S and Z parameter magnitude comparing the before and after aging characterization of Group2 device are presented in Figure 171.

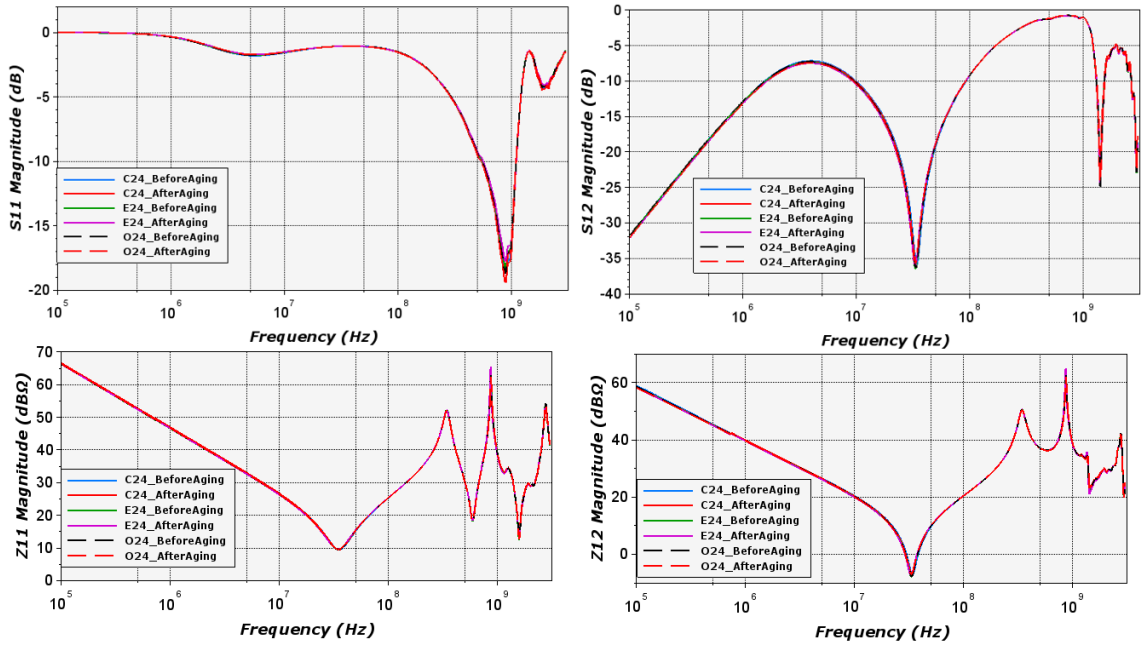


Figure 171: S₁₁, S₁₂, Z₁₁, and Z₁₂ comparison of Group2 devices before and after aging

All the three devices before and after aging VNA characterization curves are superposed, indicating no complete failure of device. However, a slight change in impedance is observed at the first resonance whose zoom view is presented in Figure 172.

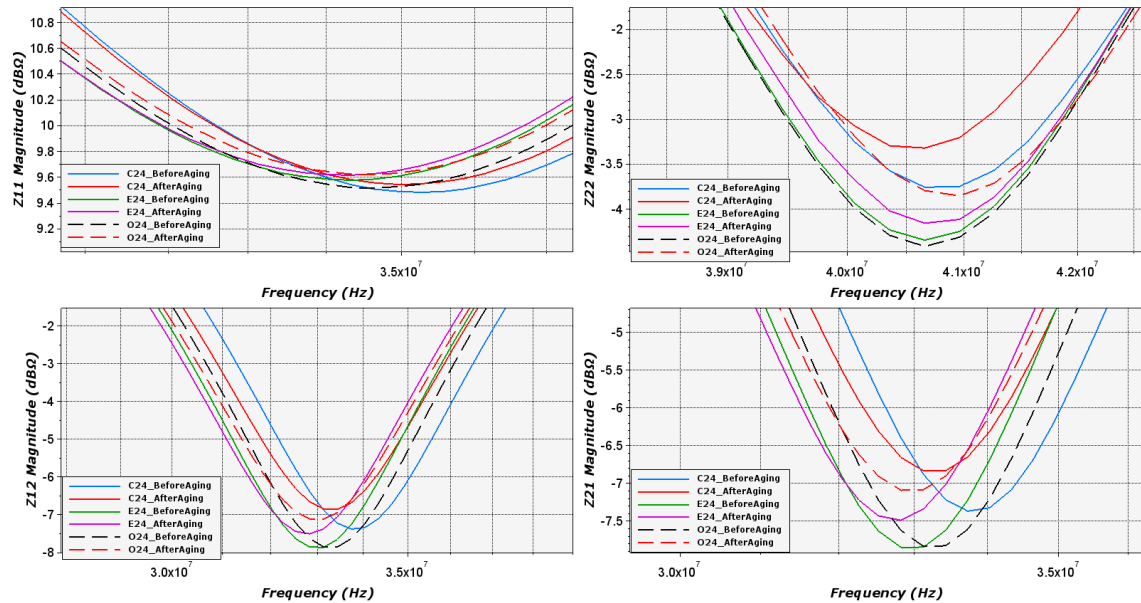


Figure 172: Z-parameters magnitude of Group2 devices before and after aging in the bandwidth of 30 MHz - 45 MHz

The increase in resistance and its percentage compared to before aging curves of each device of Group2 is listed in Table 36. No huge increase in resistance is observed. E24,

which experienced a sudden rise on V_{on} curve measure 4% of increase in equivalent resistance (Z_{12}). This rise on V_{on} curve of E24 on the last cycles can be due to sudden shut down of the test. However, as there is step change observed on V_{on} at several cycles before shut down of bench, it can be an indication of beginning of wear out mechanisms.

Parameters		C24	E24	O24
$Z_{11} (\Omega)$ (R_g+R_s)	$Z_{11}(\text{before})$	2.979	3.012	2.991
	$Z_{11}(\text{after})$	3.002	3.026	3.027
	$Z_{11}(\text{after}) - Z_{11}(\text{before})$	0.022	0.014	0.036
	% Increase	1%	0%	1%
$Z_{12} (\Omega)$ R_s	$Z_{12}(\text{before})$	0.428	0.404	0.405
	$Z_{12}(\text{after})$	0.454	0.421	0.441
	$Z_{12}(\text{after}) - Z_{12}(\text{before})$	0.026	0.017	0.036
	% Increase	6%	4%	9%
$Z_{22} (\Omega)$ (R_d+R_s)	$Z_{22}(\text{before})$	0.649	0.606	0.602
	$Z_{22}(\text{after})$	0.682	0.620	0.642
	$Z_{22}(\text{after}) - Z_{22}(\text{before})$	0.033	0.013	0.040
	% Increase	5%	2%	7%

Table 36: Increase in resistance of Group2 devices after aging extracted from Z_{11} , Z_{12} , and Z_{22} following SCOM (G1D2) configuration

Likewise, Table 37 presents the decrease in resonance frequencies and its percentage. As it can be seen, maximum of 1% decrease is observed for three devices.

Parameters		C24	E24	O24
f ₁₁ (MHz) (Resonance Frequency from Z ₁₁ curve)	f ₁₁ (before)	35.236	34.332	34.634
	f ₁₁ (after)	30.02	34.332	34.634
	f ₁₁ (after) - f ₁₁ (before)	0.002	0	0
	% Decrease	0%	0%	0%
f ₁₂ (MHz) (Resonance Frequency from Z ₁₂ curve)	f ₁₂ (before)	33.729	33.127	33.428
	f ₁₂ (after)	33.428	32.825	33.127
	f ₁₂ (after) - f ₁₂ (before)	0.301	0.301	0.301
	% Decrease	1%	1%	1%
f ₂₂ (MHz) (Resonance Frequency from Z ₂₂ curve)	f ₂₂ (before)	40.661	40.661	40.661
	f ₂₂ (after)	40.661	40.661	40.963
	f ₂₂ (after) - f ₂₂ (before)	0	0	0.301
	% Decrease	0%	0%	1%

Table 37: Decrease in resonance frequency of Group2 devices after aging extracted from Z₁₁, Z₁₂, and Z₂₂ following SCOM (G1D2) configuration

This increase in resistance could be due to crack formation at the bond wires tail as the capacitance and IV characteristics of these devices show no huge changes given in Figure 173 and Figure 174.

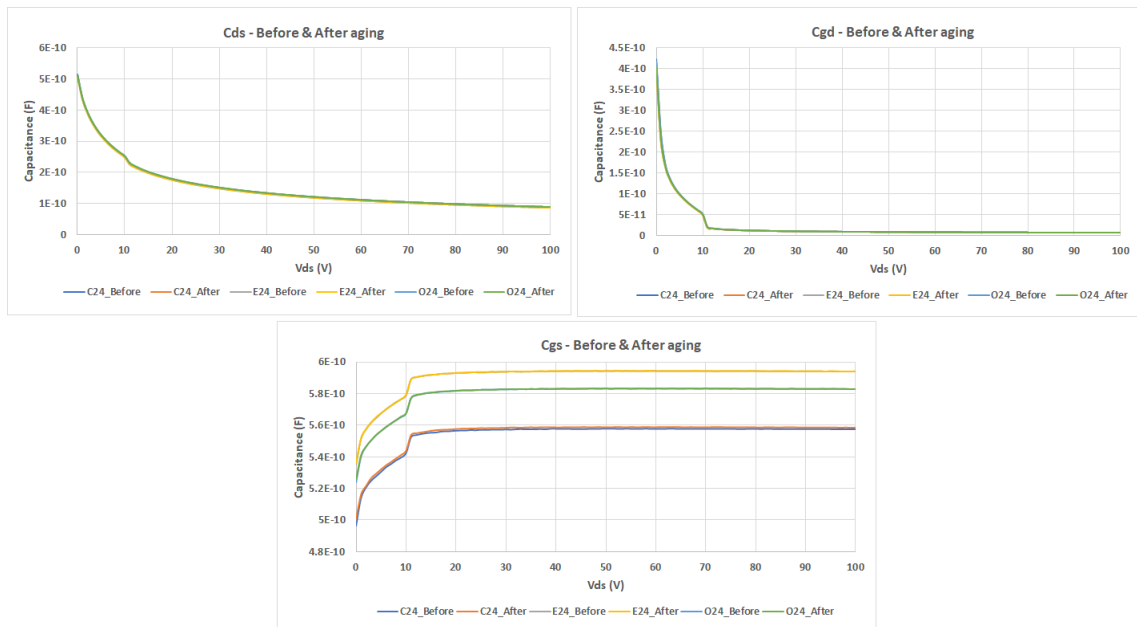


Figure 173: CV measurements on B1505A curve tracer of Group2 devices before and after aging

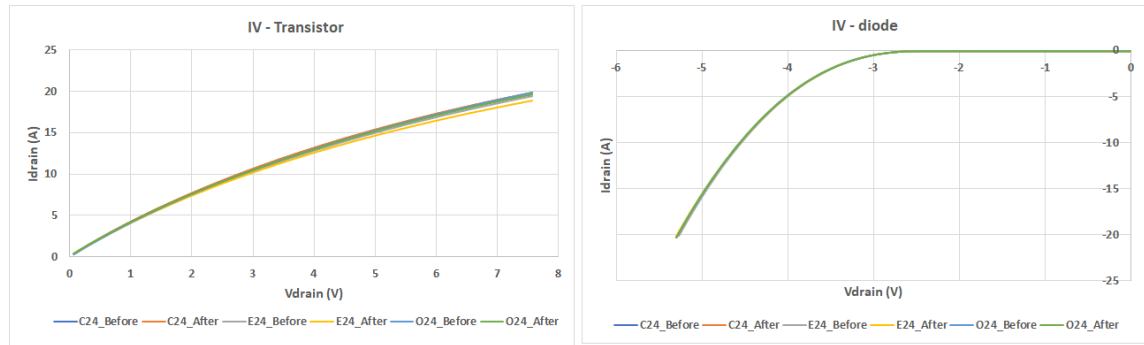


Figure 174: IV characteristics of transistor and diode of Group2 devices before and after aging

4.5.5 Temperature Cycling Test (TCT) on TO-220 Si MOSFET

This section presents the passive cycling test on discrete package using the Climatic Temperature System (CTS). In the passive cycling the device under test are subjected to an external temperature which is distributed uniformly inside the climatic chamber. The details about the passive cycling test using CTS are provided in Section 4.3.1. The samples are subjected to temperature variation of -55 °C to 180 °C. Figure 175 presents the test setup where the samples are arranged on flat surface using Kapton tape and placed inside the climatic chamber.



Figure 175: Discrete power samples placed inside climatic chamber

This test is carried out on TO-220 Si MOSFET, part number STF11NM60ND. The VNA characterization was performed on two samples at original state (0 cycle) and at different aging cycles (365, 665, and 907). As the samples were exposed to external temperature there can be different failure mechanisms to encounter. Therefore, it is necessary to verify all the possible characterization configurations and then to identify which element of the

component is subjected to failure. Following the analysis, the interesting configurations are presented highlighting the possible failure mechanisms.

Figure 176 presents the S-parameters magnitude of sample1 for different aging cycles following the configuration gate connected to port 1 (G1) and source connected to port 2 (S2) while drain is grounded (DCOM). The initial state and after 365 cycles curves are superposed (i.e., blue and red curves) for reflection and transmission parameters. After 665 cycles, S_{22} and S_{12} provide similar behavior of initial state while S_{11} produce a reduction in magnitude from 1 MHz to 500 MHz. After 907 cycles, S_{11} recover complete reflection of signal. S_{22} curve recover similar behavior of the initial state for 365, 665, and 907 cycles from 100 kHz to 100 MHz. Above 100 MHz, 365 and 665 cycles still present the similar behavior of initial state (0 cycle) while some variations are observed for 907 cycles. The transmission parameter (S_{12}) falls 28 dB in magnitude compare to the previous three aging cycles. S_{12} curves also prove a low transmission between gate and source.

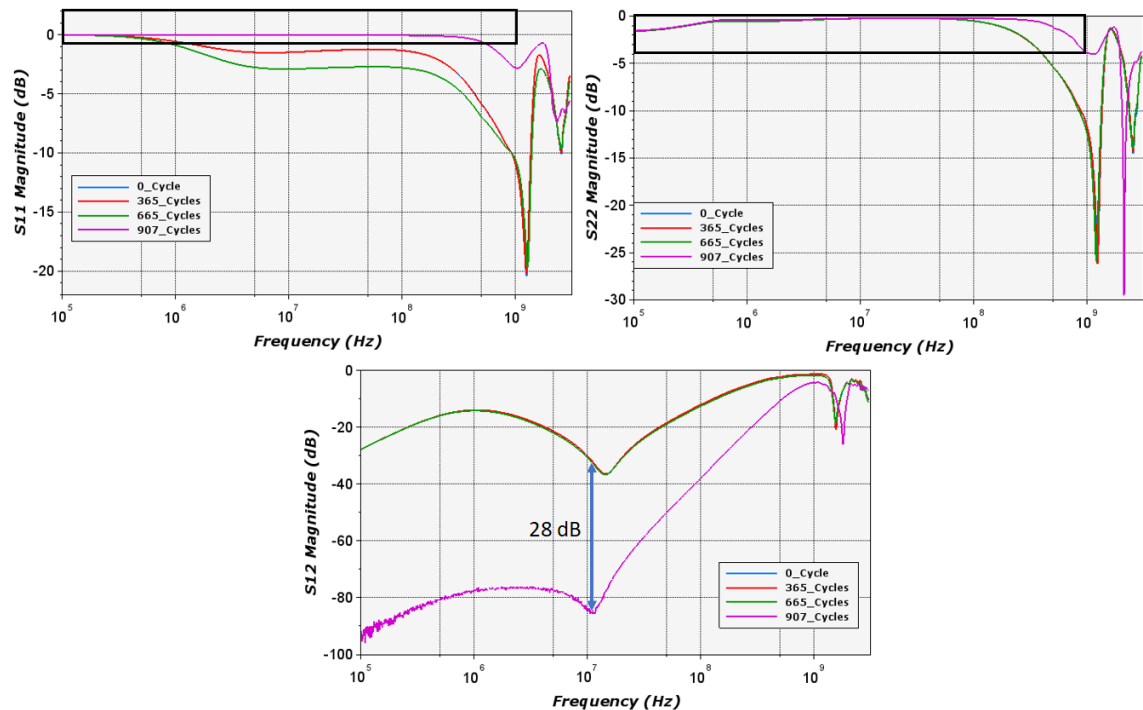


Figure 176: S-parameters magnitude of Sample1 for different aging cycles following the configuration DCOM (G1S2)

S-parameters are then converted into the Z-parameters to predict the influence of the occurrence of failure shown in Figure 177. The Z-parameter curves presented in

Figure 177 are considering DCOM (G1S2) configuration (i.e., the gate and source are connected to port 1 and port 2 respectively, and the drain is grounded).

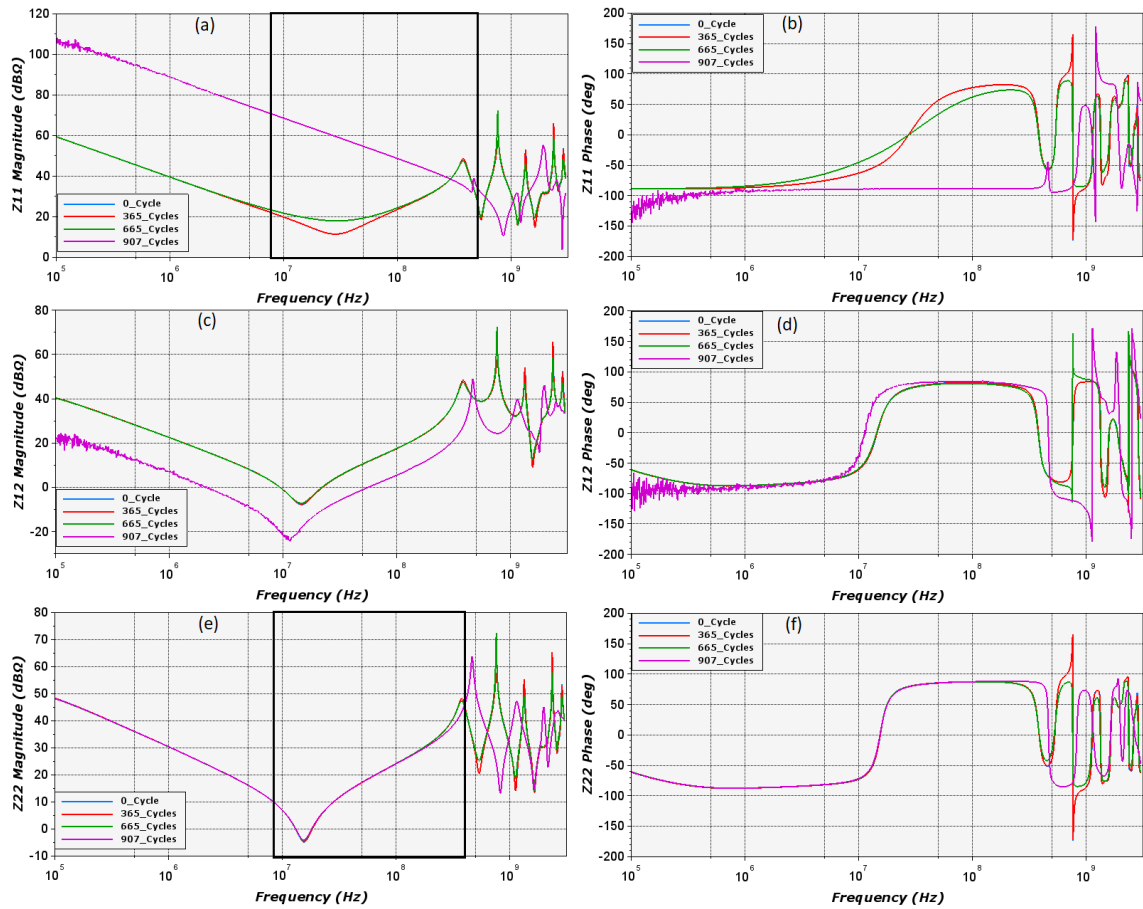


Figure 177: Z-parameters magnitude and phase of sample1 for different cycles following the configuration DCOM (G1S2)

The initial state and 365 cycles (i.e., blue and red curves) are superposed in all the six graphs (magnitude and phase) depicted in Figure 177. This illustrates the fact that, no impact is seen until 365 cycles. For 665 cycles, an increase in impedance magnitude is observed on gate connected port (Z_{11}) depicted in Figure 177 (a) which is neither seen on Z_{12} (Figure 177 (c)) nor on Z_{22} (Figure 177 (e)). Likewise, Z_{11} phase show a progressive change directing towards -90° illustrated in Figure 177 (b), again this change is not observed on Z_{12} (Figure 177 (d)) and Z_{22} (Figure 177 (f)). Moreover, to point out that the magnitude and phase curves of Z_{12} and Z_{22} are superposed with red and blue curves. This highlights the fact that, only gate connected port (Z_{11} magnitude and phase) experienced changes after 665 aging cycles.

For 907 cycles, a huge shift in resonance frequency is noticed on Z_{11} magnitude depicted in Figure 177 (a). Moreover, Z_{11} phase shifts the inductive ($+90^\circ$) behavior of the curve to capacitive (-90°), illustrated in Figure 177 (b). On the other hand, the grounding impedance (Z_{12}) presents moderate variations (Figure 177 (c) & (d)). Source connected port (Z_{22}) illustrate no changes ($< 1\%$ error) from 100 kHz to 300 MHz and some variations are observed above 300 MHz depicted in (Figure 177 (e) & (f)). These variations in Z_{12} and Z_{22} magnitude and phase after 907 cycles is can be mainly due to huge changes on gate connected port. This confirms the hypothesis that, drain and source had not experienced any failure and gate connected bond wire is failed.

It is interesting to highlight the fact that, only one measurements configuration is used to detect the failure. The analysis of two other configurations reaches the same conclusions and are presented in Appendix 4-29 and Appendix 4-30.

In similar way, the VNA characterization results of sample2 are analyzed as follows: Figure 178 presents the S-parameters magnitude of sample2 for different cycles following the configuration gate (port 1) and source (port 2) i.e., drain grounded (DCOM). S_{11} curve present reduction in magnitude following the state of the damage from 500 kHz to 900 MHz. Also, every resonance exhibit changes in magnitude. On the other hand, S_{22} and S_{12} present superposition of all the four cycling curves while presenting change in impedance magnitude. Table 38 and Table 39 present the frequency and magnitude modifications respectively, at resonance highlighted in Figure 178 for different aging cycles compared to initial state (0 cycle).

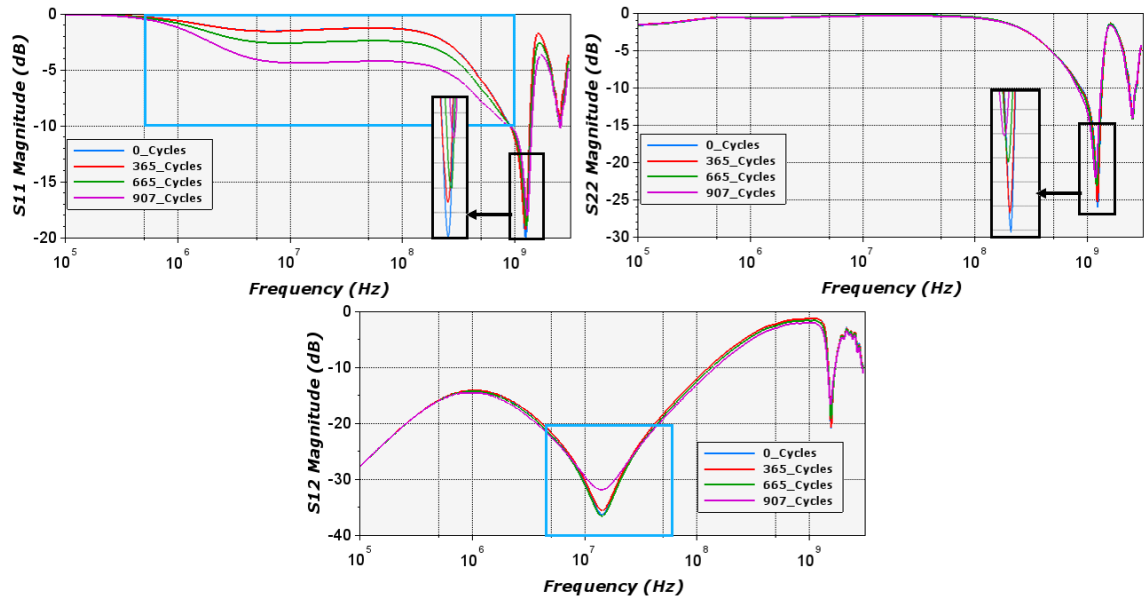


Figure 178: S parameters magnitude of sample2 for different aging cycles following the configuration DCOM (G1S2)

Resonance Frequency	Healthy	365 cycles	665 cycles	907 cycles
S ₁₁ curve (GHz)	1.24	1.24	1.26	1.28
% Increase (S ₁₁ curve)	-	0	2%	3%
S ₁₂ curve (GHz)	1.56	1.56	1.55	1.54
% Decrease (S ₁₂ curve)	-	0%	1%	1%
S ₂₂ curve (GHz)	1.23	1.22	1.21	1.18
% Decrease (S ₂₂ curve)	-	1%	2%	4%

Table 38: Resonance frequency and its percentage change compared to initial state from S-parameters magnitude of sample2 following the configuration DCOM (G1S2)

As it can be seen, the resonance frequencies experienced no huge changes following the state of the damage. On the other hand, the magnitude of different aging cycles increased compared to the initial state.

Magnitude	Healthy	365 cycles	665 cycles	907 cycles
S ₁₁ curve (dB)	-20	-19.3	-19	-18
% Increase (S ₁₁ curve)	-	4%	5%	10%
S ₁₂ curve (dB)	-20.9	-20.8	-19.2	-16.6
% Increase (S ₁₂ curve)	-	0%	8%	21%
S ₂₂ curve (dB)	-26.1	-25.3	-23.2	-22.1
% Increase (S ₂₂ curve)	-	3%	11%	15%

Table 39: Magnitude and its percentage change compared to initial state from S-parameters magnitude of sample2 following the configuration DCOM (G1S2)

The S-parameters are converted into Z-parameters and are presented in Figure 179.

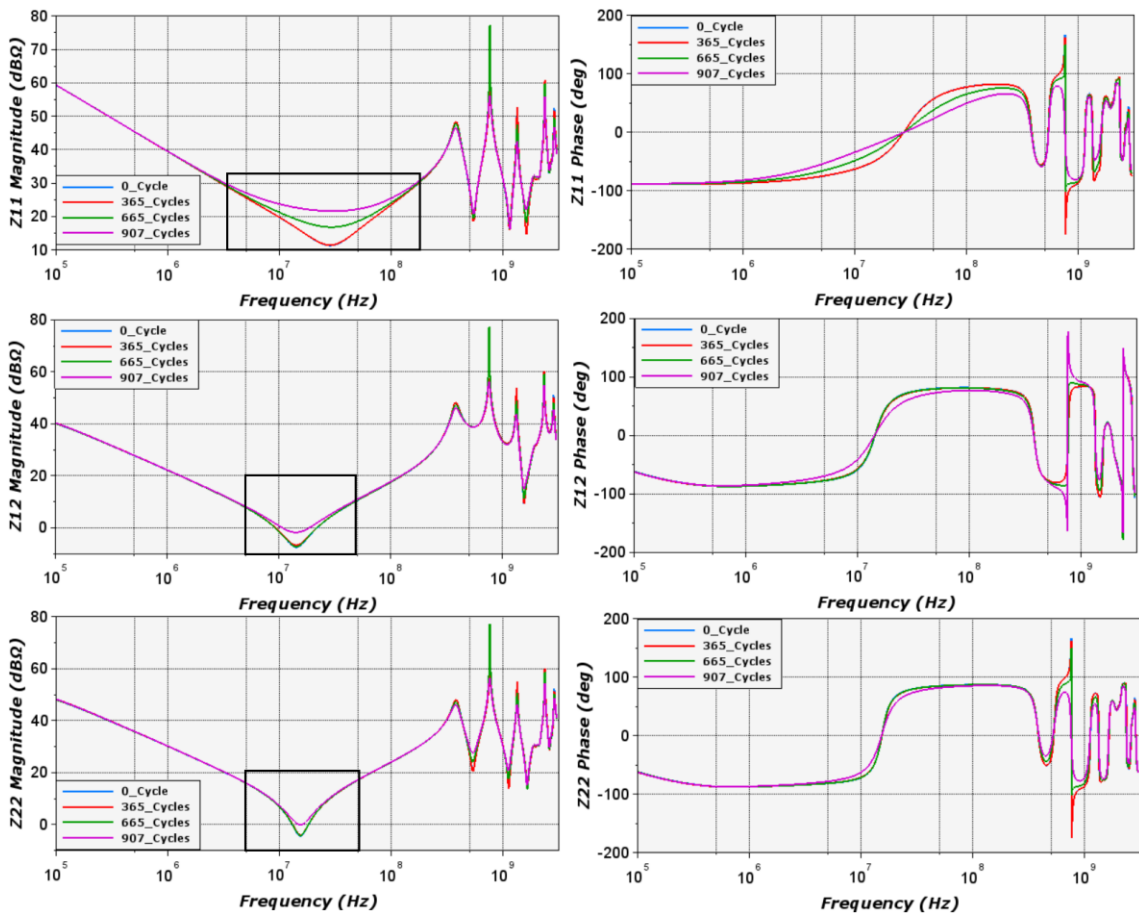


Figure 179: Z₁₁ and Z₂₂ phase curves of sample2 for different aging cycles following the configuration DCOM (G1S2)

Concerning Z₁₁ curves, Z₁₁ magnitude and phase present superposition of red and blue curves. The impedance increased by 10 dB for 907 cycles (pink curve) which increase the resistance by 226% as given in Table 40. The green curve (for 665 cycles) present

intermediate change in impedance (between (red & blue) curve and pink curve). Z_{11} phase present a progressive change for green and pink curve.

On the other hand, Z_{12} and Z_{22} present superposition of all the four cycling curves while presenting change in impedance magnitude listed in table. The resonance frequency recovered from Z_{11} , Z_{12} and Z_{22} listed in Table 41 present no huge changes.

Eventually, all these information reach to the detection of a partial failure at gate connection. It is probably a propagation of a crack or the beginning of a bond wire lift-off.

Parameters		Value	Increase	% Increase
Z_{11} (Ω) (R_g+R_d)	0 cycle	3.69	-	-
	365 cycles	3.72	0.032	1%
	665 cycles	6.92	3.23	88%
	907 cycles	1.20	8.34	226%
Z_{12} (Ω) R_d	0 cycle	4.22	-	-
	365 cycles	4.58	0.037	9%
	665 cycles	4.32	0.012	3%
	907 cycles	8.11	0.38	92%
Z_{22} (Ω) (R_s+R_d)	0 cycle	5.98	-	-
	365 cycles	6.32	0.034	6%
	665 cycles	6.13	0.015	2%
	907 cycles	9.86	0.39	65%

Table 40: Magnitude and its percentage change compared to initial state from Z-parameters magnitude of sample2 following the configuration DCOM (G1S2)

Parameters		Value	Increase	% Increase
f ₁₁ (MHz)	0 cycle	28.124	-	-
	365 cycles	28.124	0	0%
	665 cycles	28.996	0.873	3%
	907 cycles	29.651	1.527	5%
f ₁₂ (MHz)	0 cycle	14.164	-	-
	365 cycles	14.278	0.114	1%
	665 cycles	14.164	0	0%
	907 cycles	14.05	-0.114	-1%
f ₂₂ (MHz)	0 cycle	15.307	-	-
	365 cycles	15.307	0	0%
	665 cycles	15.307	0	0%
	907 cycles	15.192	-0.114	-1%

Table 41: Resonance frequency and its percentage change compared to initial state from Z-parameters magnitude of sample2 following the configuration DCOM (G1S2)

The proposed NDT methodology is well adapted to detect partial failure or full bond wire lift-off of power devices in various situations. It can be applied either to homemade prototype (with or without power device die) or unknown discrete package. Likewise, the methodology is able to detect all kind of bond wire failure: on command path like the gate of MOSFET or at power path like source termination. In all cases the detection is performed at frequencies lower than 1 GHz and it is mainly characterized by either a shift in frequency, or an increase in resistance value or both.

At last, but not least, some attempts have been made to detect failure with polarized active device. Here, again the NDT methodology has made its proofs and in a similar way compared to the unpolarized active power device. So, the polarization can be used according to the request of the electrical configuration but it is not mandatory.

4.6 Other failures (Aging of brazing)

This Section presents the application of NDT methodology on ceramic substrate with clip. Such power clips are used in power modules to connect two copper tracks. They are useful to increase power level and power density while providing low parasitic inductance and resistance [121] [122]. In the following, the aging of an inner power interconnect brazing

is studied explicitly as a component of a power module assembly. To achieve this, the brazing and its interconnect are isolated and analyzed independently from the active die.

This part of study aims to observe the failure of the brazing and/or clips by monitoring the change in transmitted and reflected waveforms. The failure detection is performed by comparison of healthy and faulty power module assembly states. Some intermediate aging results will be analyzed and discussed. This part of the study was published in [123].

4.6.1.1 *Device under test*

Four specific prototypes with brazing and clips, named Proto0, Proto1, Proto2, and Proto3, are used. Proto0 is the reference prototype and is without clip. The three other prototypes (Proto1, Proto2, and Proto3) possess 1 or 2 copper clips brazed at different locations onto the copper tracks as illustrated in Figure 180. The clip is made of copper with nickel-plated. The clip bond is placed between two tracks and acts as a solid copper bridge for the current. The clips are soldered using SAC305 solder paste with a typical melting temperature (liquidus) of 220 °C [124].

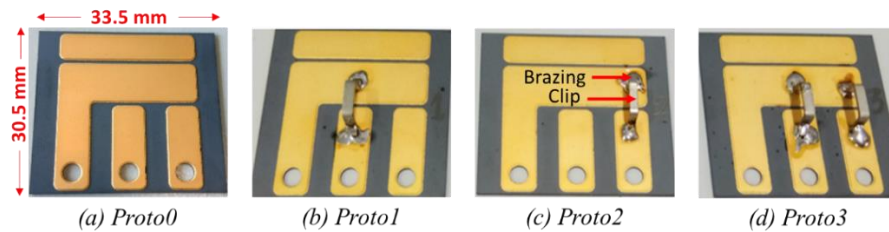


Figure 180: Homemade packaging with brazing and clips at different locations

All the four prototypes (Proto0, Proto1, Proto2, and Proto3) are placed in a climatic chamber. The temperature profile is given in Figure 129. TCT process is same as described in Section 4.3.1.

4.6.1.2 *Healthy and faulty state characterization*

In Proto1, a single clip is placed between Track 1 and Track 2a. A two-port characterization is achieved following config1, where port 1 and port 2 are connected to Track 1 and Track 2a, respectively while Track 2b is short-circuited. In healthy state, a complete transmission of the signal and a low reflection is expected. Figure 181 presents

the two-ports measurement with clip bonding between the measuring tracks, validating the transmission behavior.

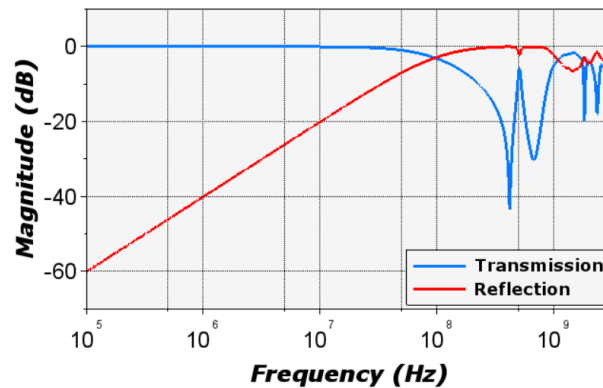


Figure 181: S_{21} (Transmission) & S_{11} (Reflection) magnitude in healthy state

After 504 passive cycles, the clip of Proto1 failed. The end-of-life picture is shown in Figure 182 (a). Figure 182 (b) presents the comparison of the transmission coefficient (S_{21}) magnitude in healthy and faulty states. In faulty state, at frequencies lower than 100 MHz, no signal transmission is observed and means that clip contact is in open circuit. So, a failure of the clip is detected. The comparison of reflection parameters in healthy and faulty states reach the same conclusions.

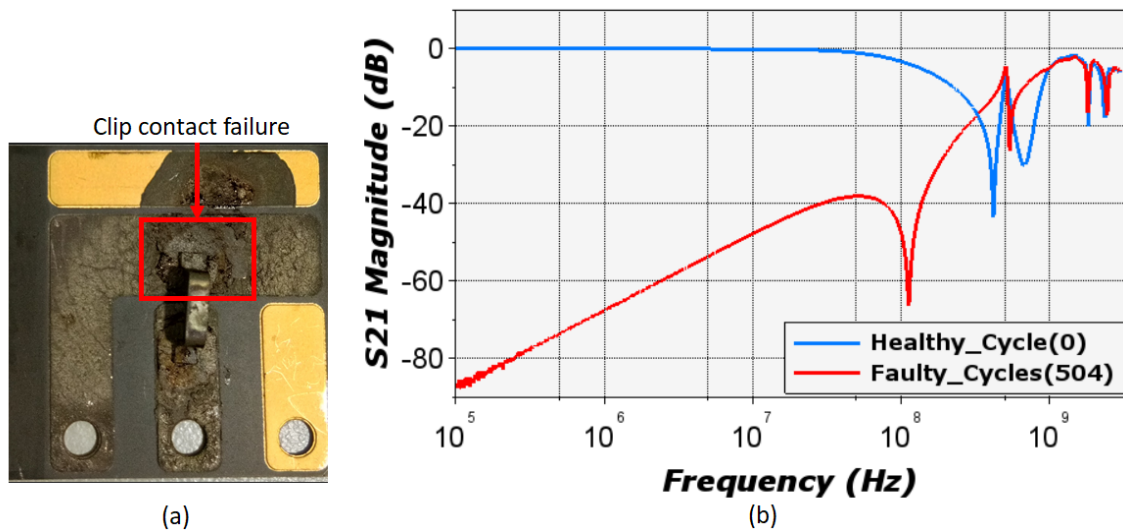


Figure 182: (a) Proto1 after 504 cycles (b) S_{21} magnitude in healthy and faulty states

The brazing does not ensure anymore the electrical continuity and adhesive contact between tracks 1 and 2a. Let us remark that the migration of the brazing is noticed soon, e.g., after the first 24 cycles, which is mainly due to gold finishing on copper tracks.

4.6.1.3 *Impact of track length*

When considering Proto1 and Proto2, the clip is positioned on different tracks with Track 1 as a common point, as illustrated in Figure 183. Blue and red color paths representing the interesting configurations for the analysis are highlighted. Therefore, this section aims to detail if there is any impact on the characterization regarding the conducting path. So similar configurations (transmission behavior) are considered for both prototypes. The common port connection for config1 and config2 is port 1, which is connected to Track 1. The length of the conducting path for Proto1 is lower than the length for Proto2.

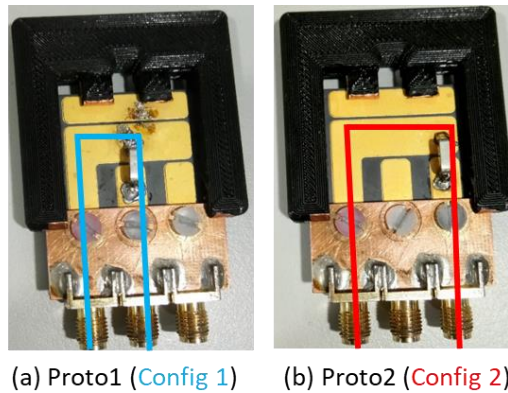


Figure 183: Proto1 and Proto2 path for a transmission behavior characteristic

The comparison of characterization of Proto1 and Proto2 in a healthy state is presented in Figure 184. The impact due to the difference in length of common track is seen after 100 MHz (indicated with blue box on Figure 184 (a)) where a shift in every peak resonance is observed. It is interesting to identify which parameters of the equivalent R-L-C circuit are affected. Therefore, S-parameters are converted into Z-parameters. Figure 184 (b) and (c) presents Z_{12} magnitude and phase of Proto1 and Proto2 in a healthy state. Likewise, the variations in Z-parameters are observed from 100 MHz. The electrical parameters behavior of Z_{12} magnitude is confirmed by the phase.

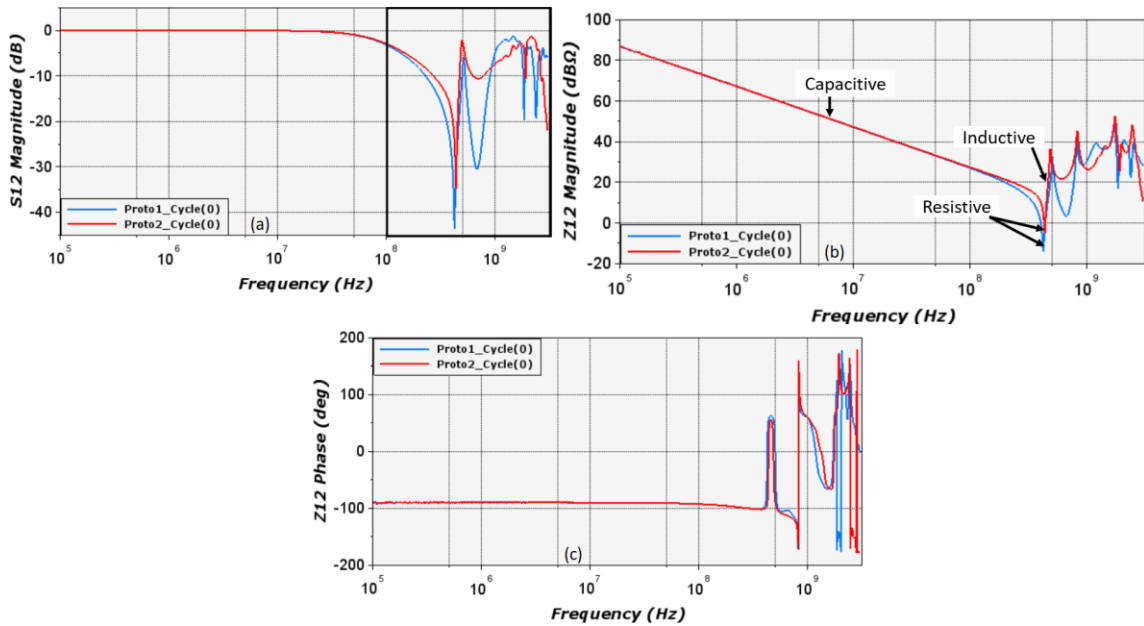


Figure 184: Comparison of Proto1 and Proto2 in a healthy state (a) S_{12} magnitude, (b) Z_{12} magnitude, and (c) Z_{12} phase

The interpretation is mainly noticed on resistance, slight changes on inductance while the capacitance remains unchanged (annotated on Figure 184 (b)). The changes in capacitance, inductance, and resistance in the annotated region of Figure 184 (b) are 0.2%, 7.84%, and 229% (almost 4 times increase) respectively. Therefore, it illustrates that the length of tracks involved in conducting path influences the inductive and resistive behavior with no or negligible influence below 100 MHz.

The various resistances, inductances, capacitances correspond to those of the DUT are shown on the electrical schematic of the experiment in Figure 185. The RLC values extracted following the NDT methodology are presented in Table 42.

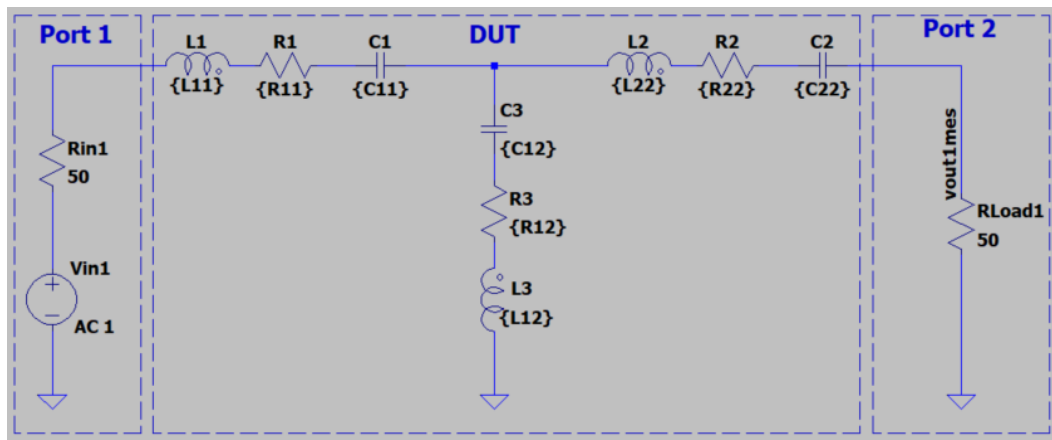


Figure 185: Electrical equivalent schema

Parameters	C ₁₁ (pF)	C ₁₂ (pF)	C ₂₂ (pF)	L ₁₁ (nH)	L ₁₂ (nH)	L ₂₂ (nH)	R ₁₁ (Ω)	R ₁₂ (Ω)	R ₂₂ (Ω)
Proto1	70.3	70.3	70.3	6.02	2.04	10.2	0.15	0.17	0.05
Proto2	70.1	70.1	70.1	6.42	2.2	9.4	0.19	0.56	0.05

Table 42: RLC extraction of Proto1 and Proto2 in a healthy state

The extracted RLC values of Proto 2 provided in Table 42 are plugged into the electrical schema given in Figure 185. The Z-parameter results of healthy state Proto 2 using the extracted RLC values is then compared with the experimental data depicted in Figure 186.

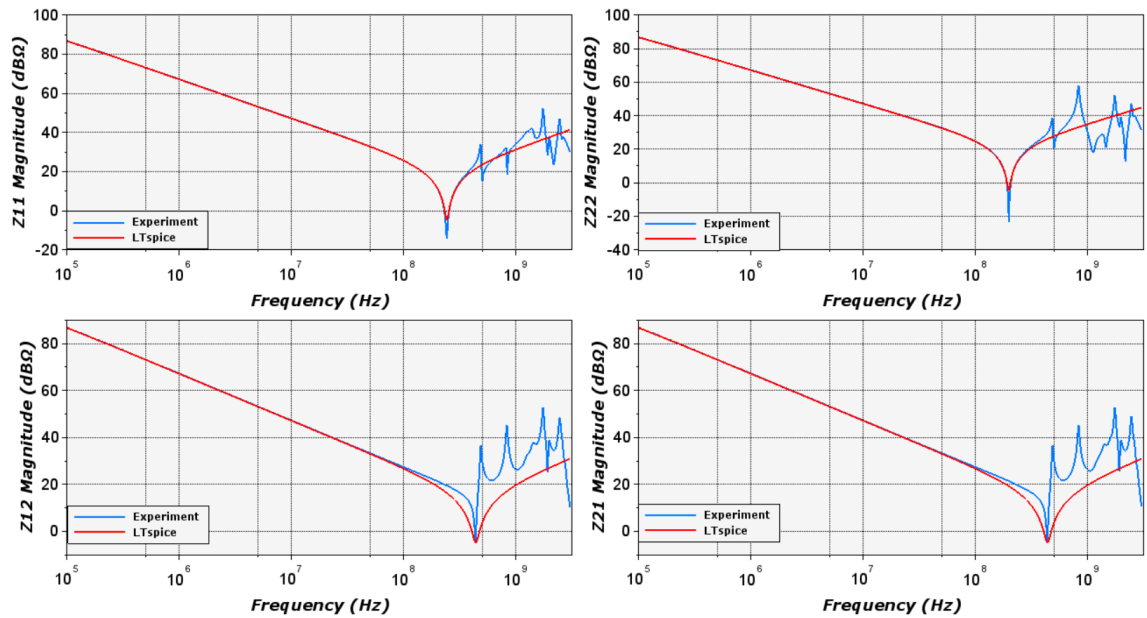


Figure 186: Experimental and LTspice simulation Z-parameters magnitude comparison of Proto2 in a healthy state

All the four Z-parameters magnitudes recover the resonance. Reflection coefficients (Z_{11} and Z_{22}) establish a good agreement between experimental and LTspice simulation from 100 kHz to 400 MHz with any difference of less than 1.7 dB. However, it was difficult to recover the exact resistance value. The transmission coefficients show good agreement from 100 kHz to 200 MHz, while recovering the exact value for the resistance.

4.6.1.4 Successive clip failure

In the following the purpose is to demonstrate that the successive failure can be monitored. The same measurement protocol, i.e., port 1 and port 2 connected to Track 1 and Track 2a, respectively with 50-ohm load on Track 2b, is used. The successive clip failure is obtained using Proto3. The failed samples figures are presented in Figure 187

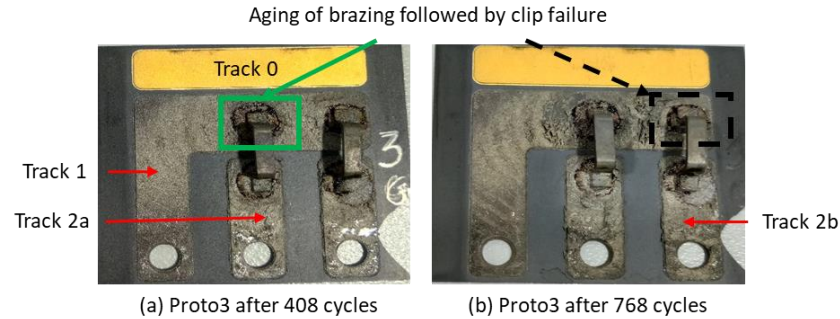


Figure 187: Successive failure of clips

The clip between the Track 1 and Track 2a failed after 408 cycles (highlighted using the green box). The clip between the Track 1 and Track 2b failed after 768 cycles (highlighted using the black dashed box). S-parameters characterization following config1 with 50-ohm load is followed throughout the analysis for this case. In such a case, the system acts as a three-port network. The failure analysis is made at frequencies below 100 MHz, which provided interesting results. S-parameters characterization following the state of health of clips of Proto 3 is presented in Figure 188. To point out, the blue and red curves of Figure 188 (a), (b), and (c) are superposed. The green and black dashed curves illustrate the cycles at which clips failed as represented in Figure 187.

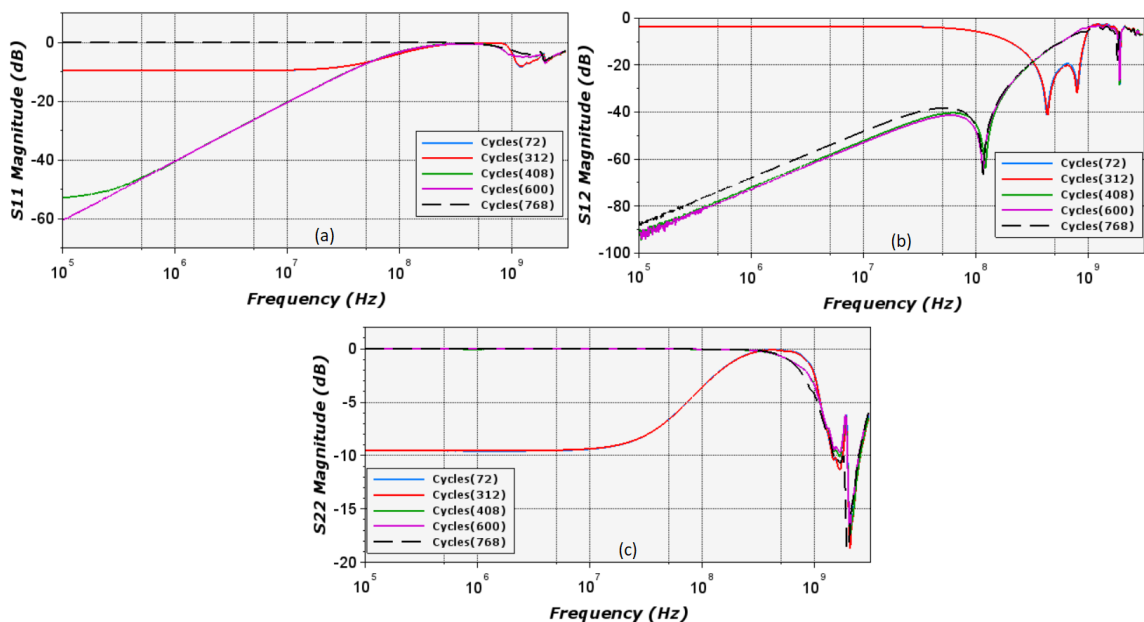


Figure 188: S-parameters magnitude for successive failure of clips

In healthy state, the injected signal is expected to be transmitted which is illustrated in Figure 188 (blue and red curves). As the termination load is 25-ohms (illustrated in Figure

189) due to parallel connected 50-ohms load on Track 2b, a partial reflection is seen on Figure 188 (a & c) with -10 dB. And a partial transmission on Figure 188 (b) is noticed.

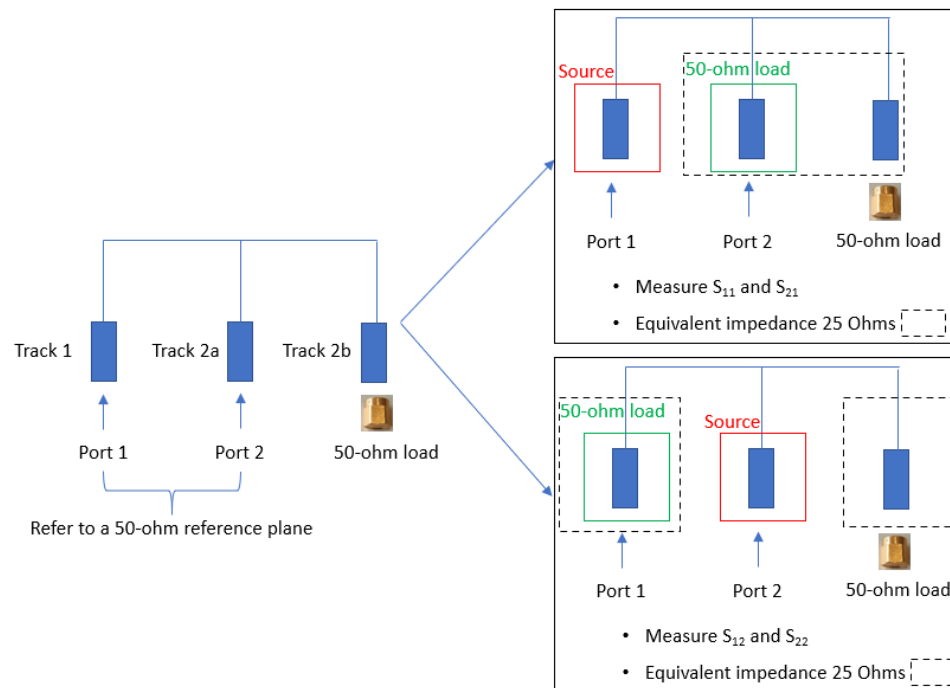


Figure 189: Equivalent impedance following config1

After the first failure, the S_{11} magnitude depicted in Figure 188 (a) measured a full transmission which is neither recovered on S_{22} (Figure 188 (c)) nor on S_{12} (Figure 188 (b)). Therefore, it means that the signal is only transmitted through Track 2b to the 50-ohm load. In other words, the Track 2a is disconnected and a failure on this electrical path is detected. As a matter of facts, an indirect measurement allows to detect full failure. The pink curve is measured after the first failure and before the second failure. In all the three curves, it is superposed with the curve which is expected as it represents the case of first failure.

After the second failure, the magnitude of S_{11} and S_{22} measured a complete reflection as it represents an “open circuit”, which is highlighted in Figure 188 (a & c). A small change in transmission coefficient (S_{12}) magnitude is observed confirming the different failure compared to the previous case (after the first failure) depicted in Figure 188 (b).

4.7 Conclusion

This Chapter presented analysis of different failure mechanisms using the broadband characterization. Three different tools were used to induce the failure i.e., Active Power Cycling (APC), Temperature Cycling Test (TCT), and manual failure. Following these tests two main failure mechanisms are studied in this Chapter: bond wire related failures, and brazing failure. Discrete power device and Si_3N_4 ceramic substrate are used to study these failure mechanisms.

TCT conducted on 10 ceramic substrates followed by regular characterization for about 8 months have experienced no degradation which are confirmed from VNA and B1505A characterization. However, it demonstrates the robustness of the measurement process.

The bond wire failures obtained after APC, TCT, and manual aging, are interesting to point out. APC test conducted on SiC power MOSFET (in TO package) is prepared in such a way to target the bond wires. The thermosensitive online monitoring parameter of the test is used as an aging indicator. This parameter provides step-wise changes indicating the state of the health of bond wires. The impedance modification analyzed from S and Z parameters compared before and after aging detect the failure and predict its influence. These results were also supported by SAM images, which reveal information related to bond wire lift-off whereas, chasing bond wire cracks is difficult task. As the power device under test possess similar characteristics, B1505A $I=f(V)$ and $C=f(V)$ measurements can identify only the complete failure. Temperature Cycling Test (TCT) conducted on Si power MOSFET aimed to see different possible failures from the test. Though this test is not defined its targeted failure, it resulted in bond wire failures in the span of 907 cycles. Two samples investigated from this test reveal impedance modifications on gate connected port. It is interesting to point out that:

- Impedance analysis resistance and inductance must be considered
- The phase analysis of impedance parameter helped to identify the complete and intermediate failure of bond wire connected to gate. The phase shifting from inductive behavior in healthy state (0 cycle) to capacitive behavior (after 907 cycles) confirm the complete failure of sample1. On the other hand, the

intermediate failure of bond wire connected to gate is identified by analyzing the phase which move from $+90^\circ$ towards -90° .

A shift in frequency with slight variations in impedance magnitude also allows to detect wire lift-off.

To get further, a first attempt was made to polarize the die. It also demonstrates the faculty to detect failure with device on state. However, the efficiency of the failure detection is similar to the non-polarized device process.

NDT methodology is applied to a ceramic substrate with clip bonding. The reliability of the clip boning and the aging of the brazing are tested by conducting passive cycling test. For a single clip prototype, the state of damage is monitored which reveal healthy and completely failed state. A successive failure of two clips is demonstrated which reveals the possibility of an indirect measurement to detect the partial failure.

Overall, this Chapter illustrates the fact, the newly developed NDT methodology is a generic approach which can be applied several power assemblies to identify different possible failure mechanisms. The strong belief beyond this methodology is that « Occurrence of a failure changes electrical impedance ». Thereby assuming that each failure mode is revealed following a frequency dependent signature.

General conclusion and perspectives

In this thesis, it was demonstrated the newly developed Non-Destructive Testing (NDT) methodology and its application to different power assemblies. The main target of detecting failure signatures following wide frequency band characterization using S and Z parameters is achieved. We have validated our hypothesis to detect the failure signature: « Occurrence of a failure changes electrical impedance. »

The first chapter reviewed a bibliographic study on discrete power devices and power module packaging and assembly and failure mechanisms related to them. The problems related to the integration of new technologies are highlighted. We have demonstrated the causes of failure occurrence, i.e., thermo-mechanical stress inside the package leading to package-related failures and over-voltage and over-current issues leading to chip-related failures. The major reliability testing methods related to accelerated aging tests are briefed. The set of destructive and non-destructive failure diagnosis methods are explored. The new technologies limit the importance of online monitoring parameters to indicate the failure modes. Each new technology raises the problem of finding a good monitoring parameter for a specific failure mode. This bibliographic study positioned us to propose a generic methodology to detect failure independent of package details, die technology, and potential failure.

In the second chapter, we have described different characterization methods, focusing more on the choice of our interest, i.e., S-parameters characterization using Vector Network Analyzer (VNA). The NDT methodology is detailed in different steps using a microstrip line as a study case. The steps of the NDT methodology are summarized as follows:

- To define the parameters of VNA (like operating frequency, sweep type, number of points per sweep, averaging factor, etc.)
- To perform the calibration (coaxial calibration technique SOLT) to eliminate systematic errors.
- To measure S-parameters (four complex S-parameters are measured from two-port VNA) and analyze these parameters
- To study the S-parameters in terms of electrical-equivalent elements. Therefore, S-parameters are converted into Z-parameters using the conversion expressions.

- To construct a two-port equivalent impedance model having respected reciprocity of the system (i.e., S_{21} is strictly equal to S_{12})
- To extract the RLCG elements from the impedance plots (Z_{11} , Z_{21} , Z_{12} , and Z_{22})
- To perform simulations by plugging the extracted RLCG into the electrical-equivalent circuit
- To compare experimental and simulation results

The above-mentioned steps are divided into two main blocks: experimentation and computation (based on experimental data). The experimentation part includes the calibration process and S-parameters measurement from VNA. The computation includes S to Z parameters conversion, RLCG element extraction, and simulations. The later block is performed when needed to analyze the results in terms of impedance parameters and to build equivalent models.

This methodology aims to be used as a generic method for several power assemblies and failure modes. The assumption is that each failure mode is revealed following a frequency-dependent signature.

In the third chapter, the developed NDT methodology is applied to the healthy state power assemblies. The power assemblies studied during this thesis were TO-packages and Active Metal Brazing (AMB) ceramic substrates, namely Si_3N_4 . The aim is to study the healthy state behavior of these assemblies in terms of propagating waves. In addition, the measurement process, the interfaces developed, the configurations used to perform two-port S-parameters measurement, and the update in the RLCG extraction process following the construction of these assemblies are detailed. The RLCG elements obtained through our methodology are compared with the datasheet and the B1505A curve tracer (which only measures capacitance). Datasheets often lack to present information about parasitic elements. In contrast, our proposed methodology excels at extracting all these elements, offering an innovative and invaluable feature. Moreover, the experimental and LTspice simulation comparison of SiC TO-247 power MOSFET presented good agreement in the bandwidth of 100 kHz to 100 MHz. Eventually, the results comparison of other TO packages are also presented. Concerning the ceramic substrate, the behavior of the substrate with bond wires between the copper tracks and with IGBT die brazed onto one

of the tracks and connected to other tracks through bond wires was studied. A bias-tee was developed to polarize the die and perform RF characterization by isolating the RF side and DC.

In the fourth chapter, the NDT methodology is applied to two power assemblies (as described in Chapter 3) to detect different failure mechanisms and modes. The two main failure mechanisms observed during this thesis are bond wire-related failures and aging of brazing. Accelerated aging tests (Temperature Cycling Test (TCT) and Active Power Cycling (APC)) and manual aging tests were conducted to induce different failure modes. The aging tests were just a tool to produce failures. A brief description of these aging tests was presented. In addition, the robustness of the measurement process is ensured.

Concerning the bond wire failures, the proposed NDT methodology is versatile and suitable for detecting partial and complete bond wire failures in power devices, including homemade prototypes (with or without power device die) and unknown packages. It effectively identifies various bond wire failure types in control or power paths. Detection involves frequencies below 1 GHz, primarily indicated by frequency shifts, increased resistance, or a combination of both factors, which can be used as a failure indicator. The online monitoring parameter V_{on} from the APC test was used as a failure indicator for the power cycling test conducted on TO-247 SiC MOSFETs.

Concerning the brazing failure, the NDT methodology is employed on a ceramic substrate with clip bonding. To assess the reliability of the clip bonding and the aging of the brazing, a passive cycling test (TCT) was conducted. In the case of a single clip prototype, the condition was closely monitored, revealing either a healthy state or a complete failure. Furthermore, a successive failure of two clips was demonstrated, highlighting the potential for an indirect measurement method to detect complete failure.

Lastly, it is interesting to mention that the proposed methodology can be applied to a known or unknown package, regardless of die technology and ability to identify potential failures.

Perspectives:

TCT on ceramic substrate:

The Temperature Cycling Test (TCT) with temperature variations of $-70\text{ }^{\circ}\text{C}$ to $180\text{ }^{\circ}\text{C}$ applied on a ceramic substrate to detect the degradation of metallic parts was not encountered during eight months of the testing process covering 3338 cycles.

In some studies concerning the thermal cycling temperature variations ($-50\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$), Si_3N_4 AMB ceramic substrates show efficient performance with no sign of failure until around 8500 cycles [117]. [125] presents degradation phenomenon observed in AMB Si_3N_4 power substrates with copper metallization, nickel-plated, and gold finish. It is interesting to point out this study presents that the degradation is noticed following severe thermal cycles of the temperature range ($-55\text{ }^{\circ}\text{C}/+245\text{ }^{\circ}\text{C}$) while it was not observed in less severe thermal cycles such as ($-40\text{ }^{\circ}\text{C}/+150\text{ }^{\circ}\text{C}$).

Following these studies, we have planned to accelerate the aging process by switching to thermal shock. The main difference between TCT using a climatic chamber and thermal shock lies in the rate and severity of temperature change. Thermal cycling in a climatic chamber simulates gradual, long-term temperature variations, while thermal shock testing mimics sudden and extreme temperature transitions. Both methods serve distinct purposes in assessing the reliability and performance of materials and components in different environmental conditions. However, this aging test plan with thermal shock is on pause due to maintenance issues of thermal shock at the platform.

Active Power Cycling (APC) test:

Usually with APC test we can target the expected failures by parameterizing the cycle time. However, sometimes we encounter some unexpected failures. In order to further study different failure mechanisms, the other campaigns can be launched using TO packages. In our case it could be interesting to conduct APC on ceramic substrate with bond wires and IGBT die. As it is open package prototype, we can visualize the failure more clearly. However, this test needs some preparation like experimental setup, to think about the way to make connections for the test etc.,

Partial failure indicator using ceramic substrate with clip bonding:

Considering the hard failures (complete failure), a partial failure function can be developed. To achieve this analysis, a partial failure function (PFF) is defined (Eq. 72). Where $Z_{healthy}$ is the impedance at healthy state (0 cycle), Z_{faulty} is the impedance at the first complete failure occurrence, and Z_{int} is the impedance at intermediate states (before or after failure).

$$PFF = \frac{Z_{int} - Z_{healthy}}{Z_{int} - Z_{faulty}} \quad Eq. 72$$

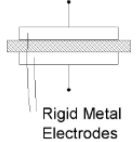
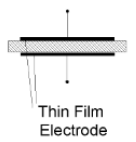
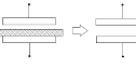

This approach is based on numeric computations of different impedances and establishes errors between impedances, taken at different cycles.

This method can be applied on different tests where healthy, intermediate and complete failure information is available. However, this indicator is applicable only when the complete failure information is provided. On the other, the numerical analysis can be done by considering soft failures. In this case, we can simplify the PFF by considering healthy and soft failures state (intermediate failure).

Eventually, this methodology can be applied to detect different failures that were not tested during this thesis. For example, voids characterization, possible defects that are inherent of the die, top side metallization quality etc.,

Appendices

Chapter 2:

Measurement Method	Contacting Electrode Method (used with Rigid Metal Electrode)	Contacting Electrode Method (used with Thin Film Electrode)	Non-contacting Electrode Method (Air Gap Method)
Electrode* Structure	 Rigid Metal Electrodes	 Thin Film Electrode	
Operation	Simple  Complex		
Applicable Test Material	<ul style="list-style-type: none"> ○ Thick material ○ Smooth material 	Materials on which thin film electrode can be applied without changing its characteristics	<ul style="list-style-type: none"> ○ Including contacting Method's applicable test Materials ○ Highly compressible material ○ Soft material
Electrodes of 16451B	Electrode-A Electrode-B	Electrode-C Electrode-D	Electrode-A Electrode-B

AE030305

* Guard electrodes are omitted

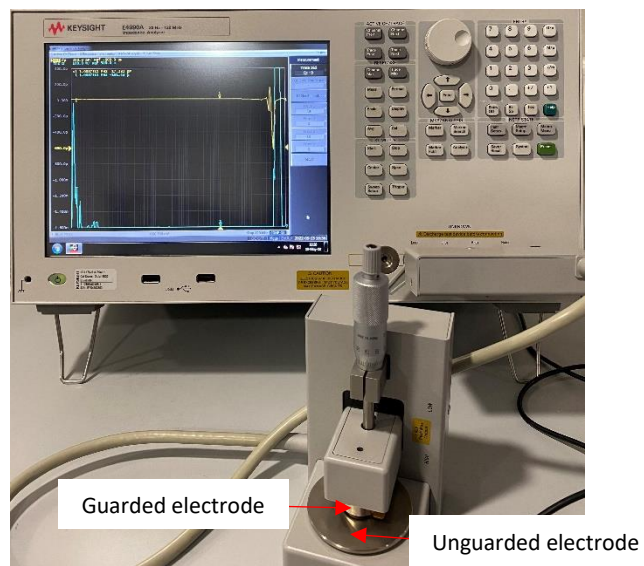
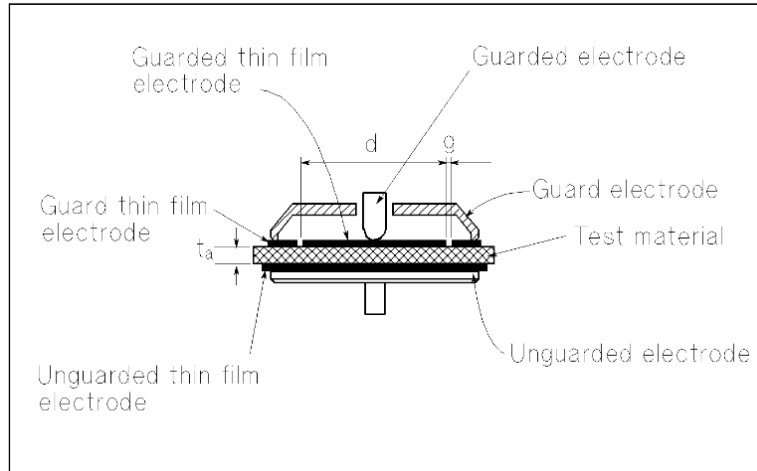
Appendix 4-1. Summary of Measurement Methods using impedance analyzer

Electrode Used	Diameter	Thickness	Guarded Electrode Diameter
Electrode-A	40 to 56 mm	≤10 mm	38 mm
Electrode-B	10 to 56 mm	≤10 mm	5 mm
Electrode-C	56 mm	≤10 mm ^{*1}	5 to 50 mm ^{*2}
Electrode-D	20 to 56 mm	≤10 mm ^{*1}	5 to 14 mm ^{*2}

*1 Including thickness of thin film electrodes

*2 As a diameter of the thin film electrode

Appendix 4-2. Available Test Material Dimensions and corresponding electrode used for impedance analyzer characterization

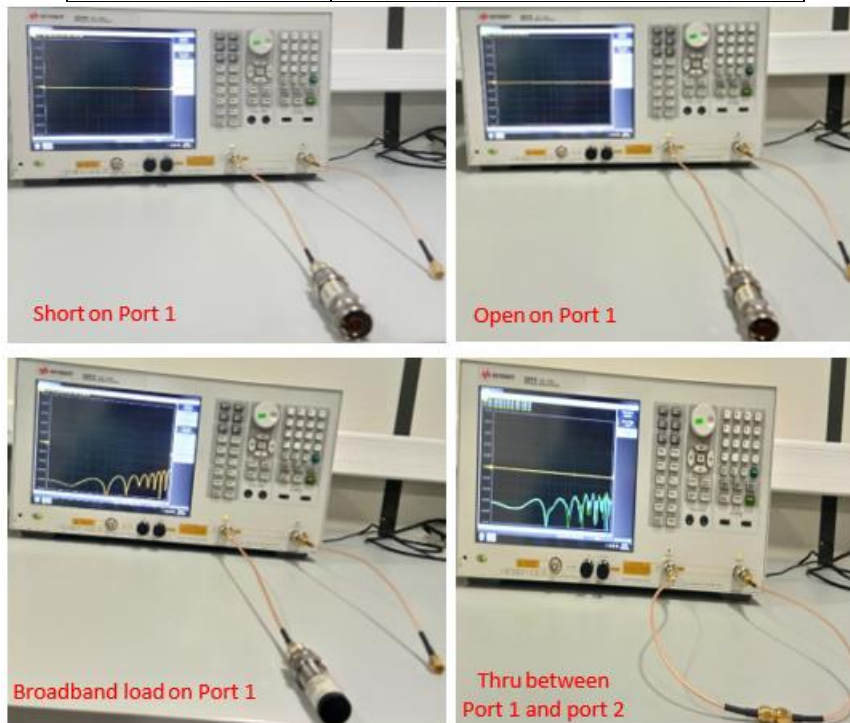


Appendix 4-3. Contacting electrode method (Thin film electrode)

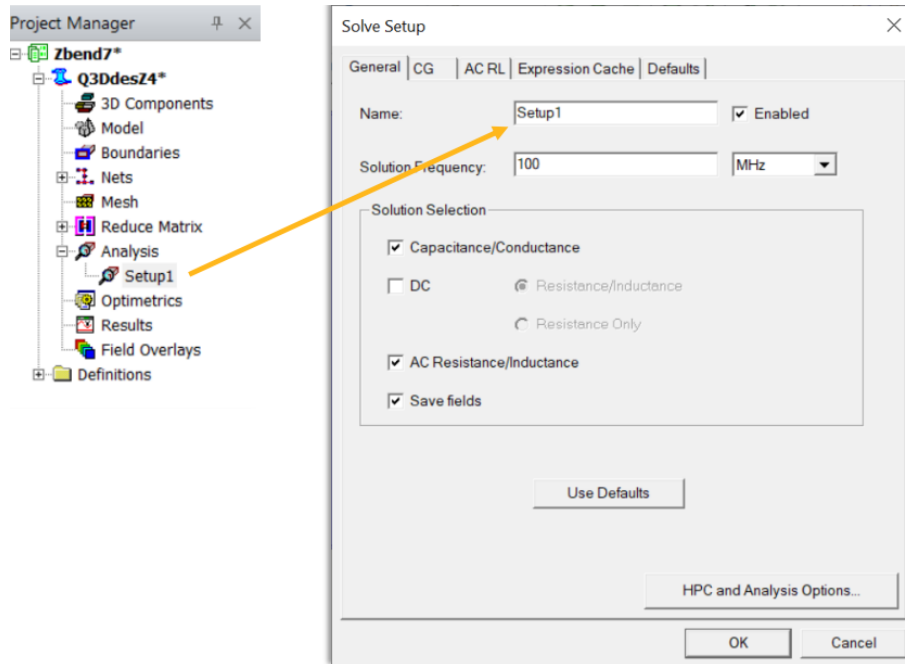


Appendix 4-4. Coaxial cables - SMA with male contact, $L=304.8$ mm, characteristic impedance is 50 ohms

Calibration step	Connexion
1	Short to Port 1
2	Open to Port 1
3	Broadband load to Port 1
4	Short to Port 2
5	Open to Port 2
6	Broadband load to Port 2
7	Thru between Port 1 and Port 2



Appendix 4-5. SOLT calibration on VNA (E5061B)



Appendix 4-6. Analysis setup for single frequency on Ansys Q3D [102]

Solutions: MSbX_Q3D_3 - 3_Q3D_MSbend_Sw

Simulation: Setup1GHz1 MSbX_021GHz

Design Variation: Substrate_Thickness='1mm' TraceWidth='2mm' Xlength='20mm' Xline='-2mm' Ylength='20mm'

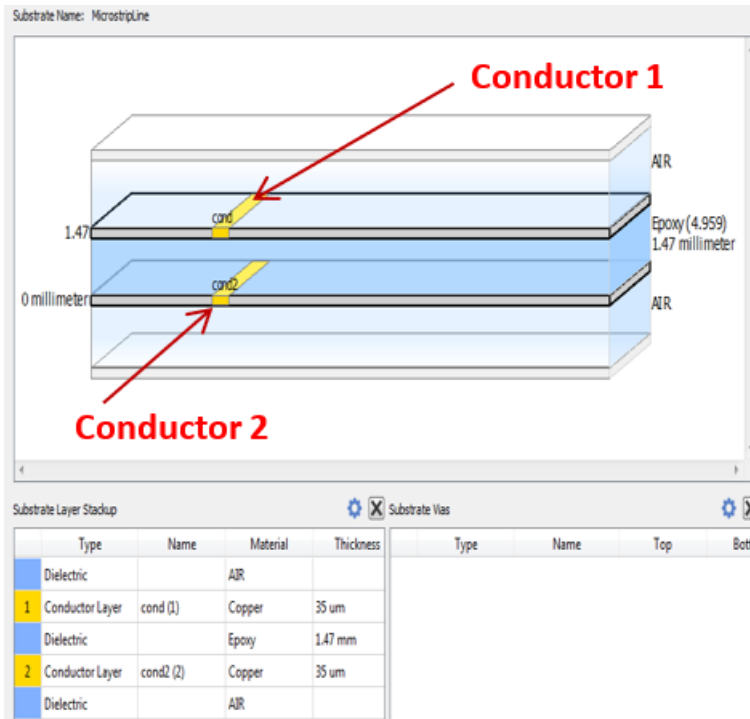
Profile | Convergence | Matrix | Mesh Statistics

Conductance Units: mSie Maxwell Matrix 0Hz
 Capacitance Units: pF Original All Freqs Edit Freqs...
 Self Terms

View Format Passivity Export

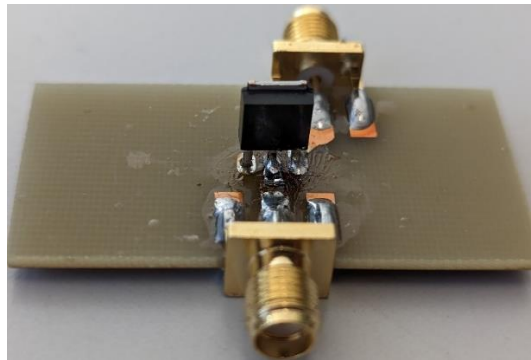
	Gnd	TraceXC	TraceYp
Freq: 0Hz			
Gnd	0.00000, 4.24290	-0.00000, -2.37302	-0.00000, -1.02345
TraceXC	-0.00000, -2.37302	0.00000, 2.39214	0.00000, -0.00803
TraceYp	-0.00000, -1.02345	0.00000, -0.00803	0.00000, 1.03893

Appendix 4-7. Matrix and field results based on solver choice [102]

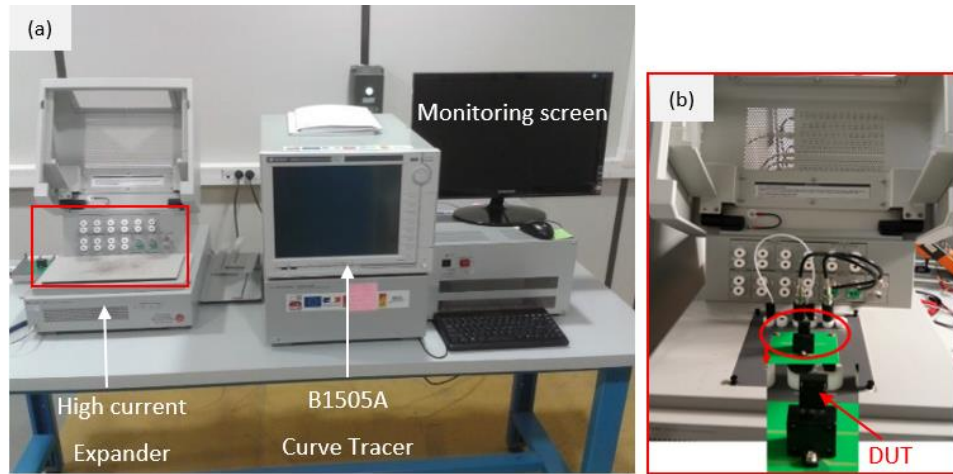


Appendix 4-8. Epoxy substrate parameters

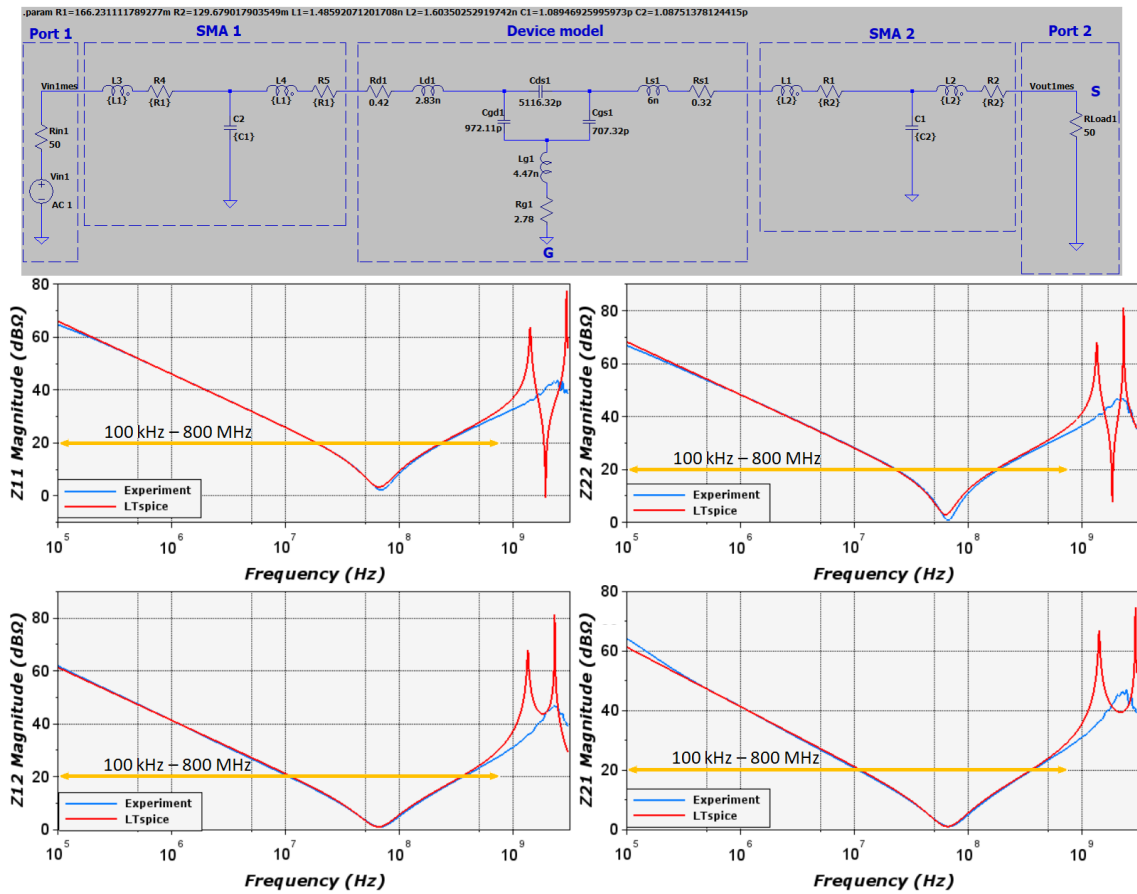
Chapter 3:



Appendix 4-9. Epoxy interface for TO-220 package placed vertically

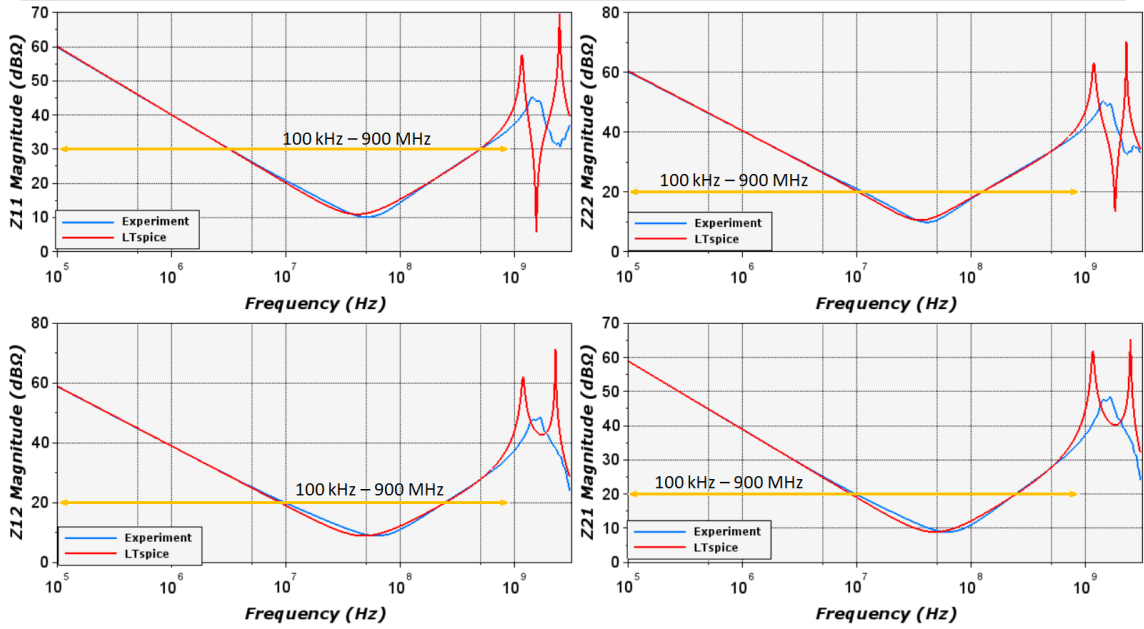
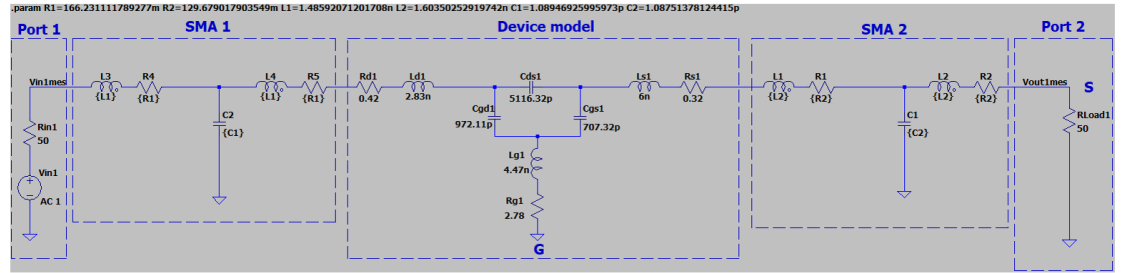


Appendix 4-10. (a) B1505A curve tracer (b) Device connection setup



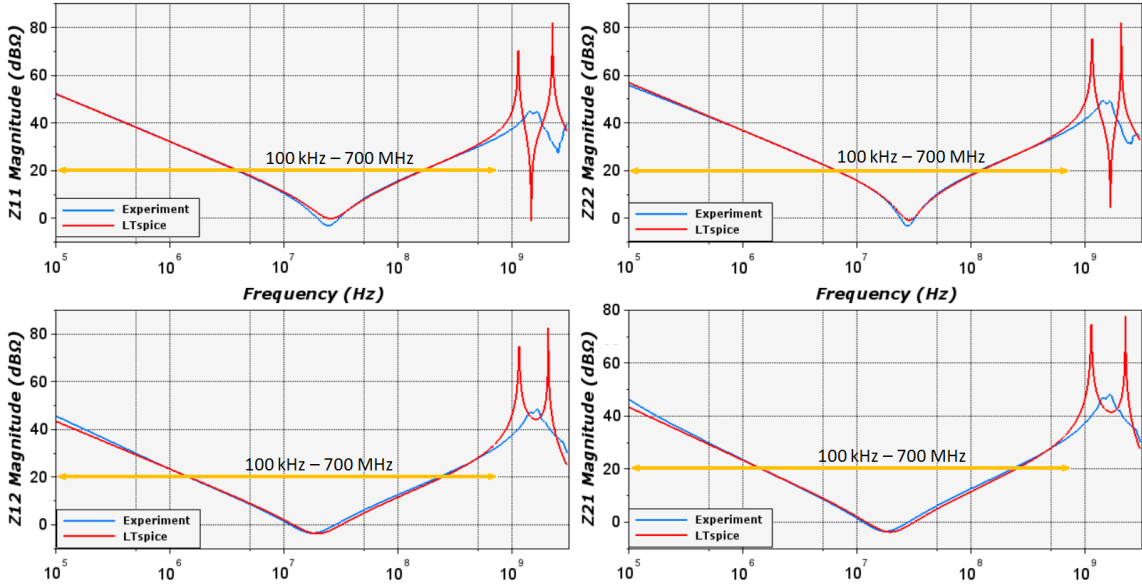
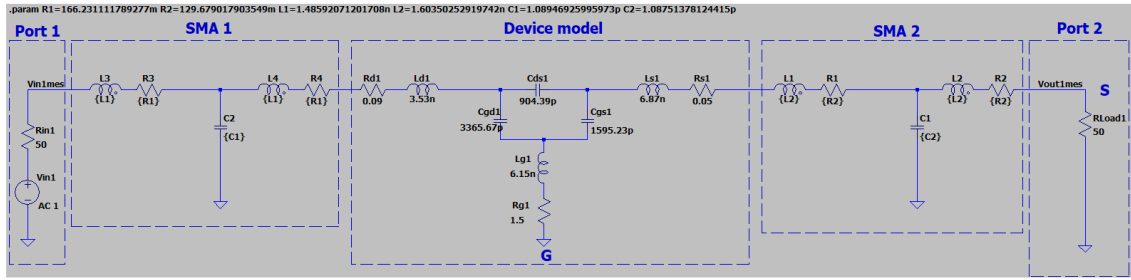
Appendix 4-11. TO-251 Si MOSFET (FQU13N10LTU) LTspice model and its comparison with experimental data

The experimental and simulation curves shown in Appendix 4-11 are in good agreement from 100 kHz to 800 MHz with any differences less than 2 dB within this bandwidth.



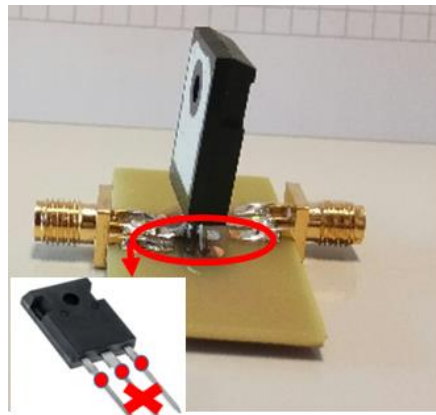
Appendix 4-12. TO-220 Full Pack Si MOSFET (STF11NM60ND) LTspice model and its comparison with experimental data

The experimental and simulation curves show in Appendix 4-12 are in good agreement from 100 kHz to 900 MHz with any differences less than 2 dB within this bandwidth.



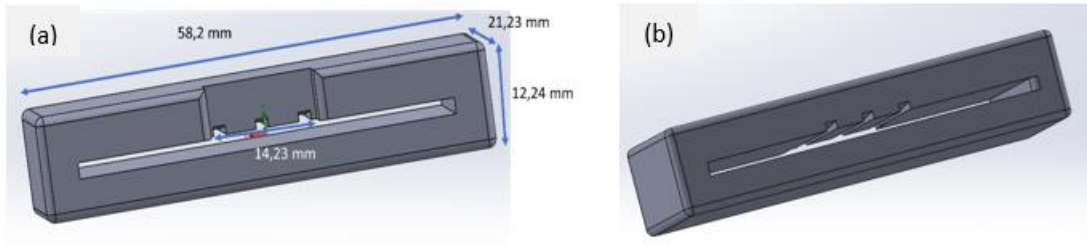
Appendix 4-13. TO-220 Si MOSFET (IRLI540NPBF) LTspice model and its comparison with experimental data

The experimental and simulation curves shown in Appendix 4-13 are in good agreement from 100 kHz to 700 MHz with any differences less than 2 dB within this bandwidth.

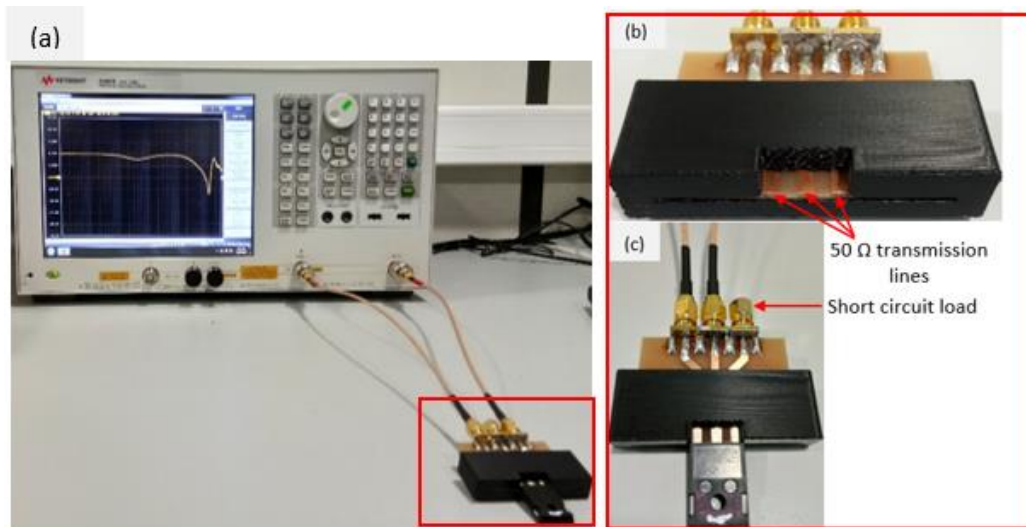


- Connection point
- ✗ Eliminated

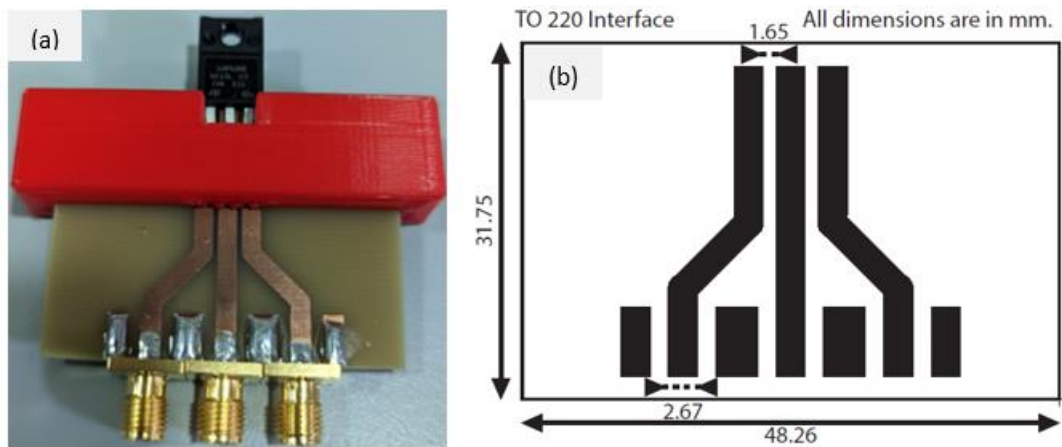
Appendix 4-14. TO package device connection for vertically placed epoxy interface



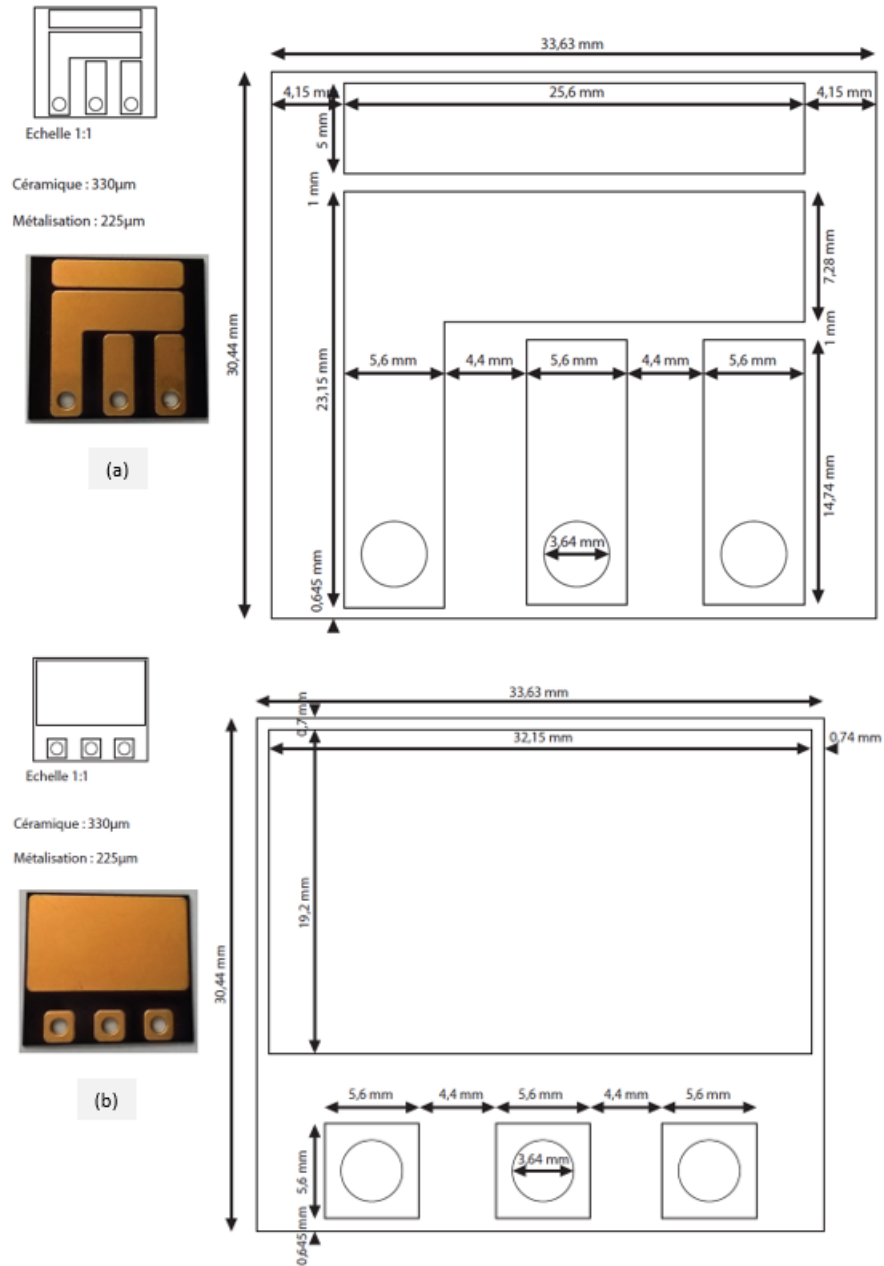
Appendix 4-15. Supporting box dimensions (a) front view, (b) back view



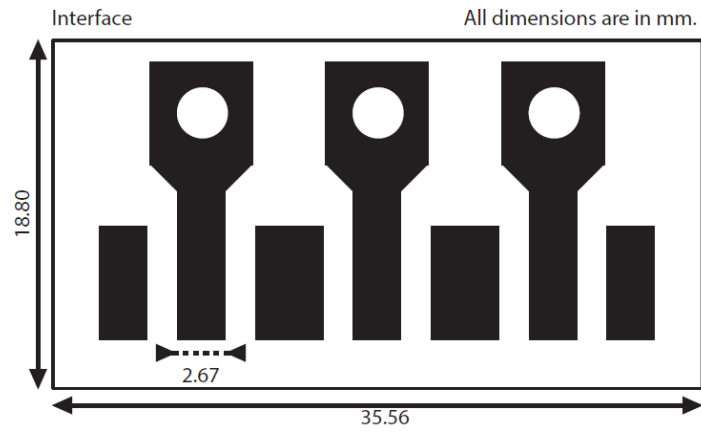
Appendix 4-16. Two-port VNA characterization of epoxy interface with horizontally placed TO package (b) Before placing the device, and (c) after placing the device



Appendix 4-17. Epoxy interface of TO-220 package horizontally placed (a) interface with device (b) interface foot print top side

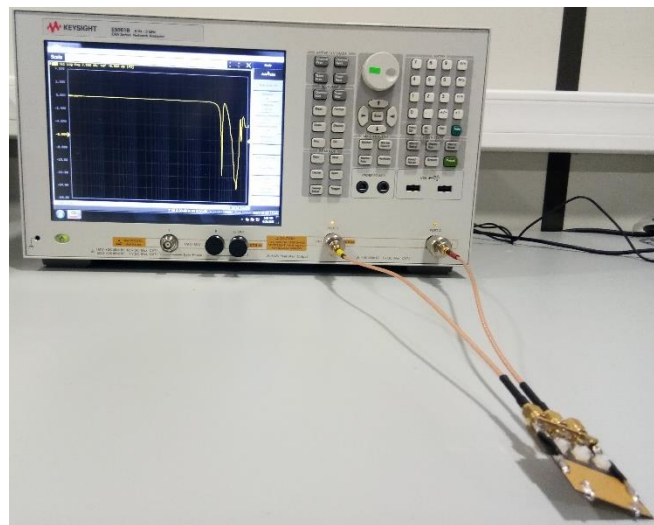


Appendix 4-18. Active Metal Brazing (AMB) ceramic substrate dimensions (a) top view (b) bottom view

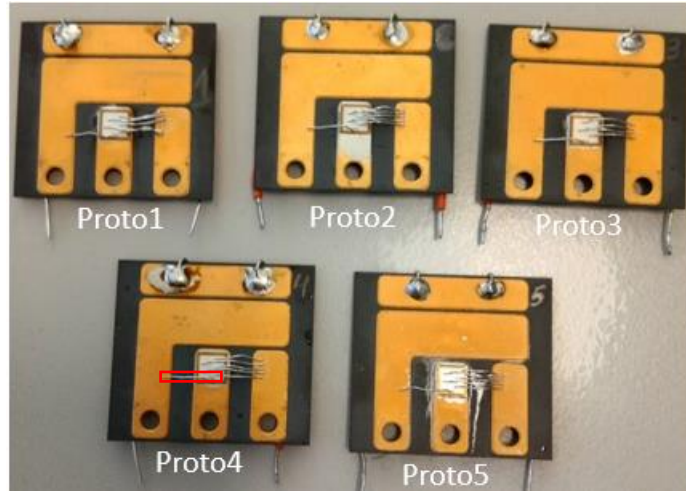


Appendix 4-19. Epoxy interface dimensions (50 Ω adapted) bottom side

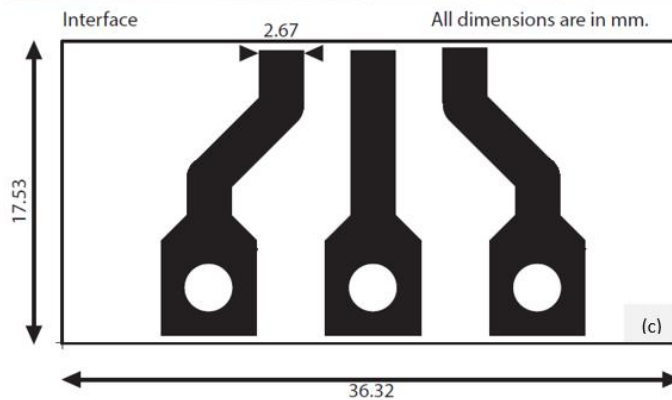
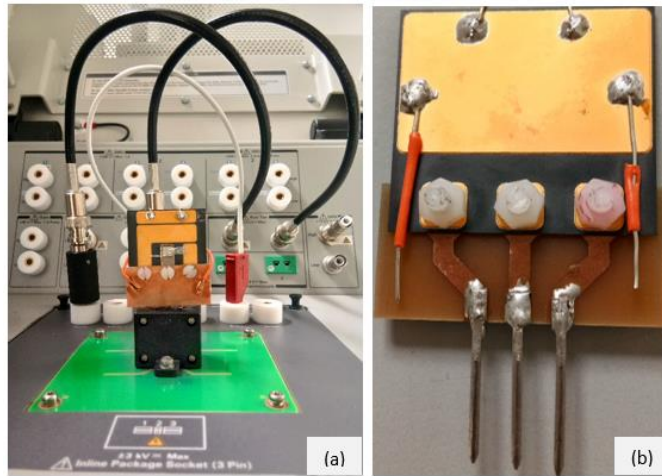
The thickness of epoxy and metallization are 1.5 mm and 35 μm respectively.



Appendix 4-20. Ceramic substrate two-port characterization on VNA



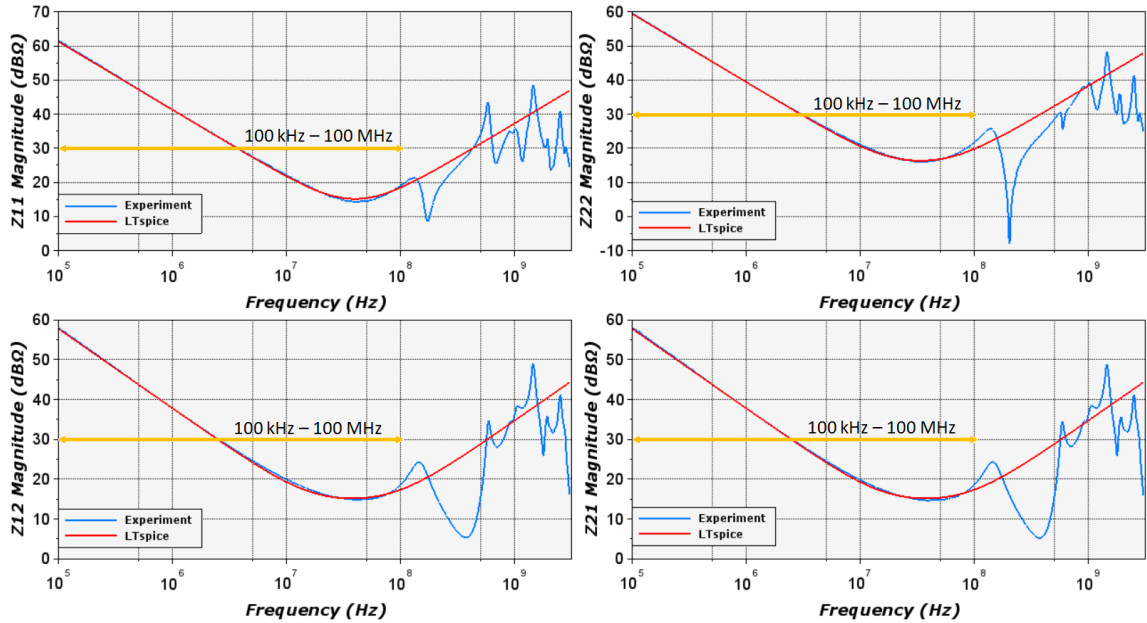
Appendix 4-21. Homemade packaging with IGBT die mounted on Track 2a (5 Samples)



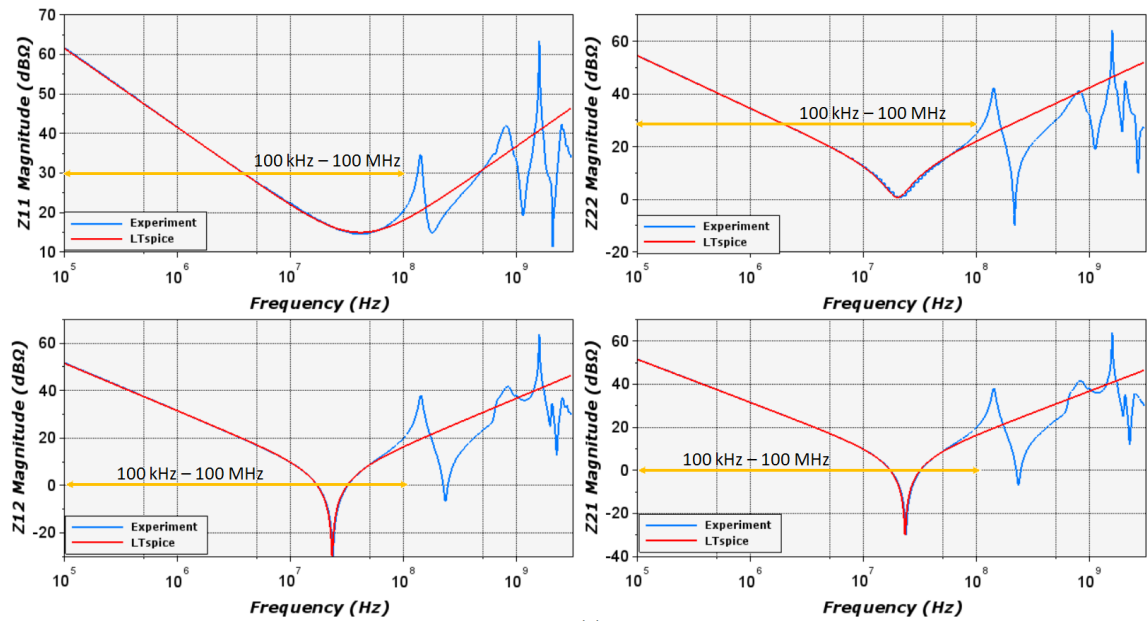
Appendix 4-22. Homemade packaging B1505A curve tracer setup and interface details

The interface is designed with ground plane on the upper face and 50Ω adapted tracks on the bottom face. The adapted tracks are used to connect the terminals which support to fix the DUT into the B1505A CV measurement sorting given in Appendix 4-22 (a). The

floating tracks of the DUT are connected to the ground plane using grounding wires shown in Appendix 4-22 (a) and (b). The dimensions of the interface are provided in Appendix 4-22 (c).

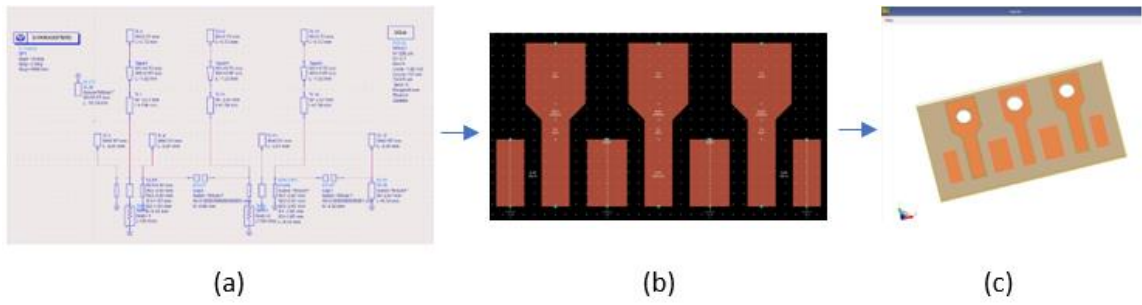


(a)

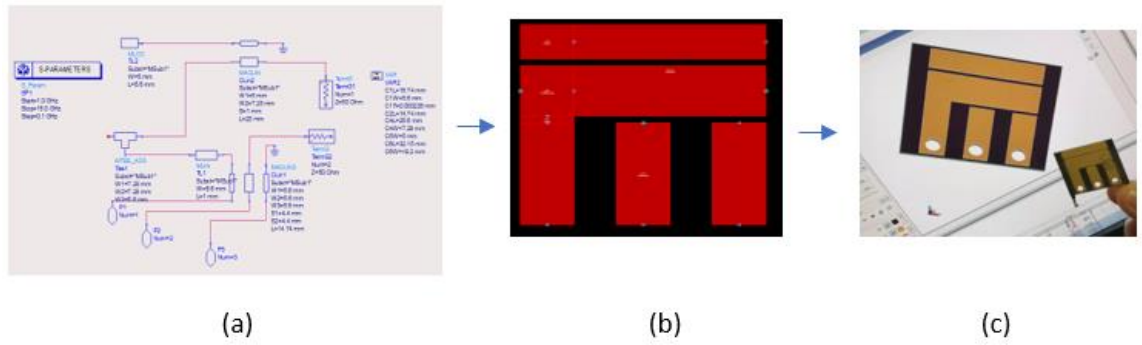


(b)

Appendix 4-23. Experimental and LTspice comparison of healthy state homemade packaging with IGBT die (a) config2 (b) config3

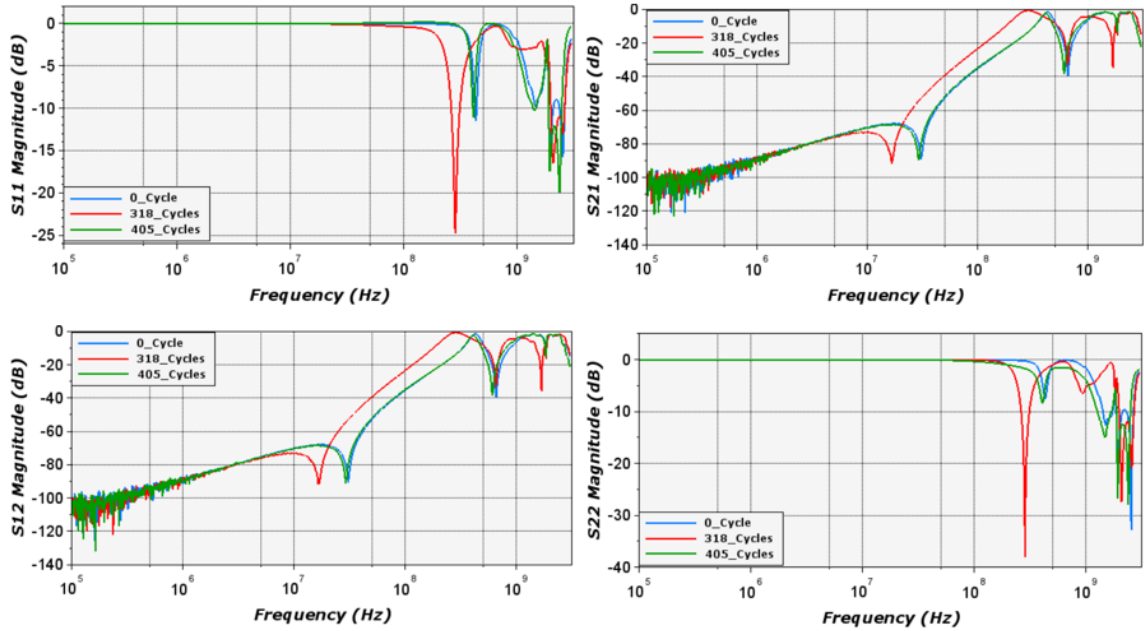


Appendix 4-24. Epoxy interface design (a) Circuit environment, (b) Visualization in layout, and (c) 3D environment

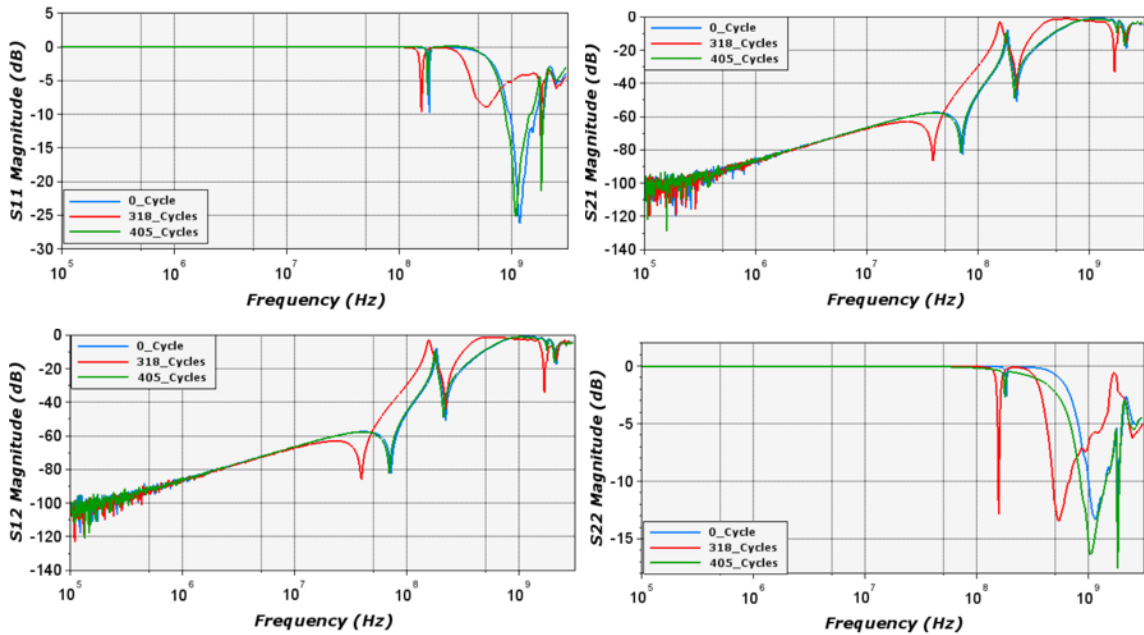


Appendix 4-25. Ceramic substrate design (a) Circuit environment, (b) Visualization in layout, and (c) 3D environment

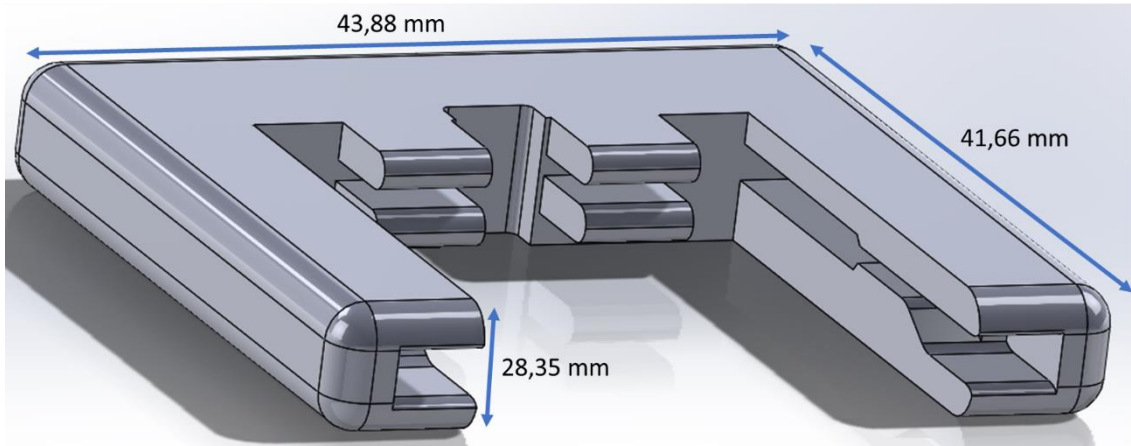
Chapter 4:



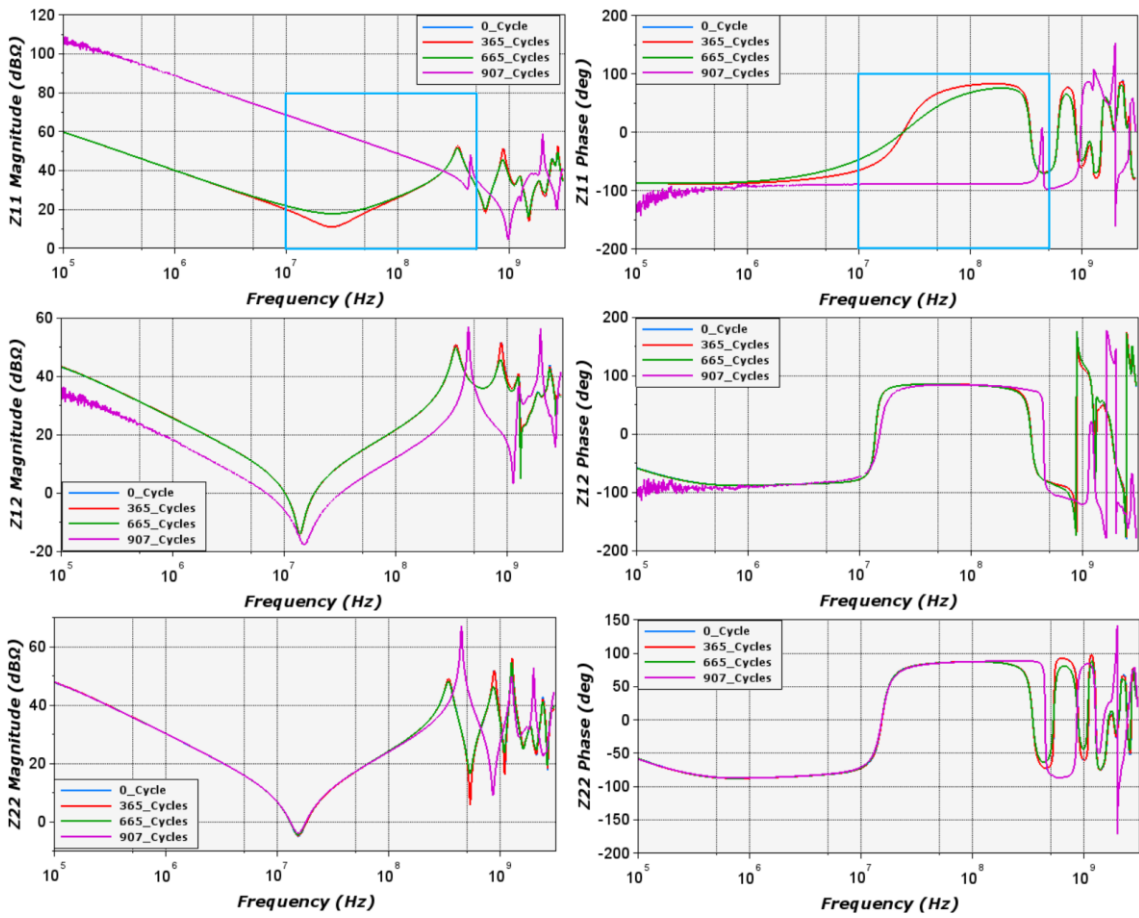
Appendix 4-26. S-parameters magnitude at 0 cycle, 318, and 405 cycles of prototype 1 following config2



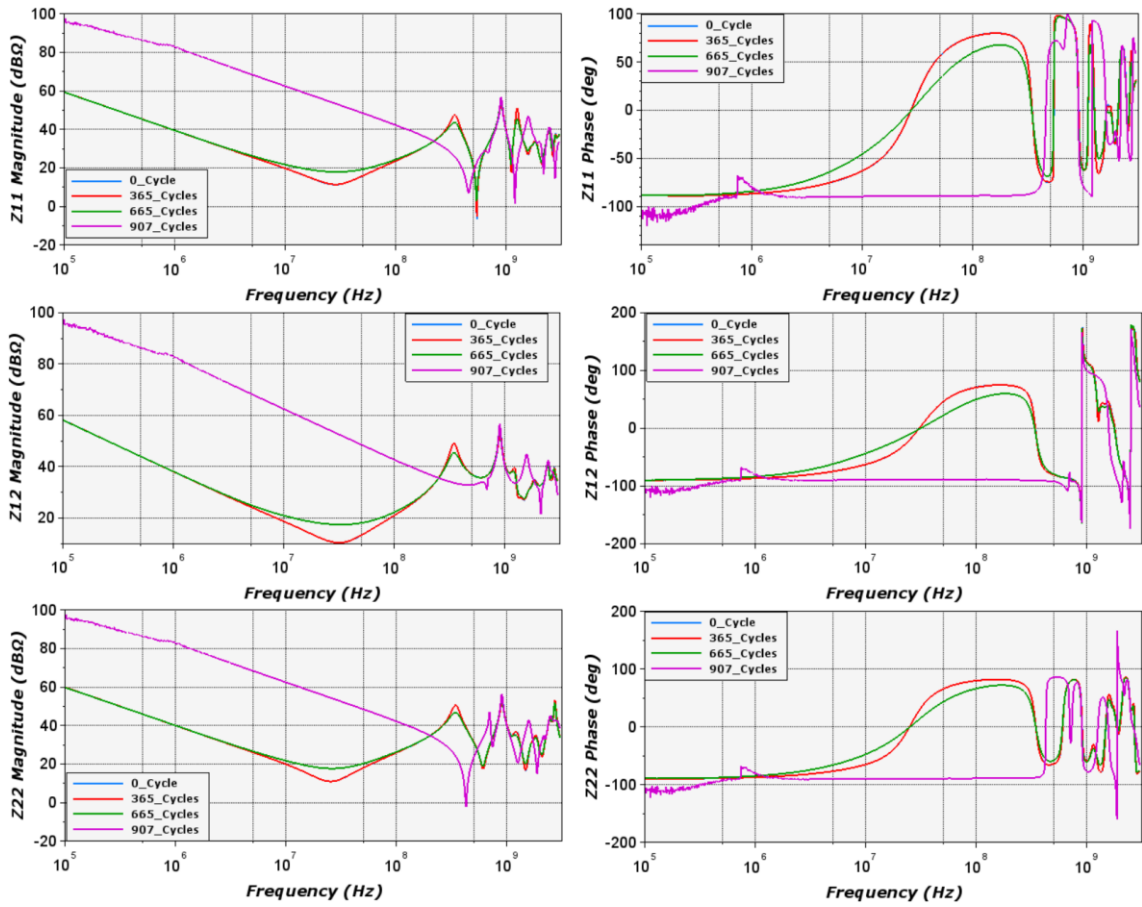
Appendix 4-27. S-parameters magnitude at 0 cycle, 318, and 405 cycles of prototype 1 following config3



Appendix 4-28. 3D interface dimensions



Appendix 4-29. Z-parameters magnitude and phase of sample1 for different cycles following the configuration SCOM (G1D2)



Appendix 4-30. Z-parameters magnitude and phase of sample1 for different cycles following the configuration GCOM (D1S2)

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