Study and design of integrated laser diode driver for 3D-depth sensing applications

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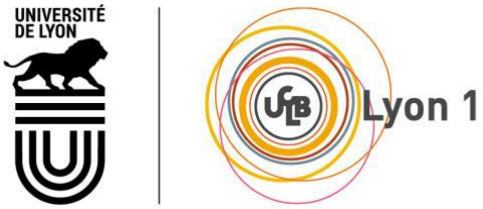

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Study and Design of Integrated Laser Diode Driver for 3D-Depth Sensing Applications

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"The very insistence on truth has taught me to appreciate the beauty of compromise."

MOHANDAS KARAMCHAND GANDHI

« Mon exigence pour la vérité m'a elle-même enseigné la beauté du compromis. »

MOHANDAS KARAMCHAND GANDHI

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List of Acronyms

APC Automatic Power Control

AR Augmented Reality

BCD Bipolar-CMOS-DMOS

BGA Ball Grid Array

BJT Bipolar Junction Transistor

BSDSB Bulk-Source-Drain-Source-Bulk

CAGR Compound Annual Growth Rate

CCD Charge-Coupled Device

CMOS Complementary Metal Oxide Semiconductor

CL Current Limiter

CW Continuous Wave

DAC Digital-to-Analog Converter

DC Direct Current

DC/DC Direct Current to Direct Current

DCR DC Resistance

DFT Discrete Fourier Transform

DMOS Diffused MOSFET

dToF direct Time-of-Flight

DUT Device Under Test

EEL Edge-Emitting Laser

EMI Electromagnetic Interference

ESD Electrostatic Discharge

ESR Equivalent Series Resistance

FFT Fast Fourier Transform

FoV Field-of-View

FWHM Full Width at Half Maximum

GaN FET Gallium-Nitride Field Effect Transistor

GR Guard Ring

GSG Ground-Signal-Ground

HFS High-Frequency Switching

HV-CMOS High-Voltage CMOS

I/O Input/Output

IC Integrated Circuit

iToF indirect Time-of-Flight

KPI Key Performance Indicator

LDD Laser Diode Driver

LDMOS Lateral DMOS

LDO Low Dropout

LED Light-Emitting Diode

LGA Land Grid Array

LiDAR Light Detection and Ranging

LRM Line-Reflect-Match

LVDS Low Voltage Differential Signaling

MIM Metal-Insulator-Metal

MLP Micro Lead frame Package

MOM Metal-Oxide-Metal

MOS Metal-Oxide-Semiconductor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MPD Monitor Photodiode

MR Mixed Reality

NMOS n-channel MOSFET

NMOS-AW NMOS with Active Well

PCB Printed Circuit Board

PCE Power Conversion Efficiency

PDN Power Delivery Network

PLL Phase-Locked Loop

PLS Post-Layout Simulation

PMOS p-channel MOSFET

PPD Pinned Photodiode

PRF Pulse Repetition Frequency

PVT Process, Voltage and Temperature

PWHM Pulse Width at Half Maximum

PWM Pulse Width Modulation

QFN Quad-Flat No-leads

QVGA Quarter Video Graphic Array

RDL Redistribution Layer

RMS Root Mean Square

SH Shunt

SMU Source-Measurement Unit

SOLT Short-Open-Load-Thru

SOT Small Outline Transistor

SPAD Single-Photon Avalanche Diode

STI Shallow Trench Isolation

TCSPC Time-Correlated Single-Photon Counting

TDC Time-to-Digital Converter

TLP Transmission-Line Pulse

ToF Time-of-Flight

TRL Thru-Reflect-Line

VCSEL Vertical Cavity Surface Emitting Laser

VGA Video Graphic Array

VIA Vertical Interconnect Access

VNA Vector Network Analyzer

WLCSP Wafer Level Chip Scale Package

Remerciements

Et voilà, c'est fini ! J'écris ces lignes le 02 avril 2021, presque un an jour pour jour après la fin de mon contrat de travail chez STMicroelectronics, et quelques semaines après la validation de ma soutenance, le 25 février 2021. En regardant en arrière, ce parcours n'aura pas été facile, comme tout doctorant j'imagine, mais riche d'enseignements. Laissez-moi vous replacer le contexte :

"Nous sommes le 16 mars 2020, la France entre officiellement en confinement général pour 15 jours minimum, afin de lutter contre la pandémie mondiale du COVID-19. J'ai pu effectuer mes derniers tests juste à temps, avant la fermeture temporelle de l'entreprise et la fin de mon contrat le 31 mars 2020. Ayant suffisamment de résultats, je m'inscris à Pôle Emploi et entame la rédaction du manuscrit de thèse, pensant finir en 2-3 mois.

Je ne le sais pas encore mais, étant plutôt perfectionniste, la rédaction me prendra finalement 7 mois à temps plein, jusqu'au 20 octobre 2020. Le confinement général aura duré 6 semaines, jusqu'au 11 mai 2020. Très éprouvant pour certains, c'est durant cette période où j'ai été le plus concentré, paradoxalement. Mais les beaux jours arrivent et un questionnement pseudo-philosophique s'installe en moi, comme beaucoup j'imagine, sur "le Monde d'Après". Se succèdent alors des périodes de démotivation, motivation, puis re-démotivation et re-motivation, jusqu'en octobre. Une première version du manuscrit est envoyée, ouf !

Un deuxième confinement est mis en place pour 6 semaines encore, à la suite de quoi un couvre-feu est instauré. Qu'à cela ne tienne, la soutenance est prévue le 16 décembre 2020, en visioconférence. On fait comme on peut. Mais à cause d'un planning trop court, elle sera finalement décalée au 25 février 2021. Plus qu'un dernier effort à fournir. Malgré un déroulement en visionconférence totale, tout s'est bien passé. C'est validée, enfin !"

Avant tout, j'aimerais grandement remercier ma famille qui m'a soutenu sans relâche durant ces 3 années de thèse et surtout la "4ème année", plus éprouvante que les autres. Je remercie aussi mes potes de Lyon, de Paris, de Grenoble et autres petites bourgades de France, ainsi que ceux de ma promo d'école d'ingé CPE Lyon avec qui j'ai gardé contact. Ils m'ont permis de me libérer l'esprit durant cette période et profiter de la vie, notamment autour d'un petit jaune avec 2-3 glaçons au fond d'un verre à pied ;)

De façon plus professionnelle, ce projet de thèse sous convention CIFRE a été supporté par le financement de l'ANRT ainsi que l'étroite collaboration entre STMicroelectronics et la laboratoire Ampère.

Je tiens à remercier chaleureusement mon encadrant industriel, Xavier Branca (designer analog de l'équipe Silicon & System - R& D du département AMS de STMicroelectronics) pour avoir porter ce projet au sein de l'entreprise, de m'avoir offert l'opportunité d'effectuer cette thèse, de m'avoir soutenu jusqu'à la fin. Et surtout d'avoir été présent quand j'en avais besoin, c'est le plus important selon moi. Étant son premier doctorant, j'espère avoir été à la hauteur de ses attentes.

Je remercie aussi respectivement mes directeur et co-directeur de thèse Charles Joubert et Bruno Allard du laboratoire Ampère, pour les nombreux conseils qu'ils m'ont apportés sur le plan scientifique et académique, les relectures de publications et de ce manuscrit ainsi que les présentations blanches de soutenance.

Je souhaite également remercier Aleksandar Prodic et Marc Cousineau d'avoir accepter être rapporteur de ce manuscrit, Sonia Ben Dhia d'avoir accepter présider la soutenance de thèse ainsi que Nathalie Batut, Estelle Lauga-Larroze et Fabien Mieyeville d'avoir accepter être membre du jury.

Enfin, pour préserver l'authenticité, je tiens à retransmettre tel quel mes remerciements adressés par mail à mes collègues de STMicroelectronics lors de mon départ le 31 mars 2020 :

From: Romain DAVID
Sent: mardi 31 mars 2020 11:32
To: Equipe STMicroelectronics,
Subject: Croissants virtuels pour mon départ.

"Bonjour à tous,

C'est mon dernier jour aujourd'hui et à défaut de ne pouvoir vous convier tous à mon bureau pour partager les traditionnelles viennoiseries, je vous envoie quand même une petite photo pour faire style ! Mais le cœur y est, ne vous y trompez pas ;)

Je tenais à tous vous remercier de m'avoir accueilli dans l'équipe depuis presque 4 ans maintenant. J'étais arrivé en 2016 pour mon stage de fin d'études, puis j'ai poursuivi en thèse en 2017.
Je ne savais pas à quoi m'attendre et j'ai beaucoup appris auprès de vous, même si je n'ai pas eu l'occasion de travailler ou parler longuement avec tout le monde. En tout cas, les discussions, que ce soit au niveau du travail, à table ou aux pauses cafés, ont été très variées et m'ont beaucoup enrichi. En tout cas, j'ai pris notes vis-à-vis des enfants et de

l'immobilier, je pense que je vais attendre encore un peu.

Je voulais remercier tout particulièrement Xavier qui m'a soutenu pendant ces 4 années et qui m'a transmis tout son savoir-faire, niveau microélec et design bien sûr mais aussi ses petites astuces de bricolo. Ça n'a pas été facile tous les jours, il y a eu des hauts et des bas, avec des discussions parfois musclées, mais au moins il y avait moyen de débattre et il m'a appris à prendre du recul quand je voyais tout noir. Comme il le répète souvent : « on fait pas d'omelette sans casser des œufs » ! Je pense que ça me resservira plus tôt que prévu.

Merci à mon camarade de thèse, Samuel (Rigault), sans qui la thèse aurait été moins fun. On a bien galéré sur certains sujets comme tout bon thésard qui se respecte et notamment la rédaction (pas encore finie d'ailleurs), mais c'est en forgeant que l'on devient forgeron ! Nos parcours sont similaires, on vient de la même promo, on a travaillé en binôme chez Analog Devices pendant 1 an, on a fait notre PFE chez ST (pas la même division mais sur le site de Grenoble), et maintenant la thèse. Bref, on s'est bien marré quand même. J'espère que l'on se recroisera bientôt ;)

Enfin, merci aux personnes impliquées de près ou de loin sur le projet de thèse. Grâce à vous, j'ai quand même réussi à avoir beaucoup de résultats, négatifs ou positifs, qui me permettent d'avoir beaucoup de matières pour le manuscrit. C'est frustrant évidemment de ne pas aller jusqu'au bout, de comprendre vraiment l'origine des problèmes mais on avance petit à petit. J'espère que ce travail pourra servir pour les futurs projets. Merci aussi à la division Imaging et ST en général pour m'avoir offert cette opportunité de thèse. Je tiens à dire que j'ai été gâté pour mes test chip : 10 versions différentes de circuits au final pour 3 versions de cartes de test, rien que ça ! Sans compter les environnements de mesures électriques et optiques où j'ai quand même pu m'amuser un peu malgré les problèmes logistiques. Et je vous rassure, je vois touujmours dmees 2 yeeuixx, enfin je crois :)

Dans tous les cas, je reviendrais dans les prochains mois pour vous refaire une présentation blanche en anglais, plus académique cette fois. Et puis pour faire un pot de départ en bonne et due forme. Je vous souhaite à tous une bonne continuation et bon courage pour les futures projets, et j'espère vous recroiser dans le monde de la microélec ou autre ;)

Histoire de faire un peu philosophe, je me suis inspiré de Xavier pour trouver la traditionnelle citation de thèse et je vous laisse sur ces mots :
« Mon exigence pour la vérité m'a elle-même enseigné la beauté du compromis », Gandhi.

A bientôt ;)
Romain"

Malheureusement, compte tenu du contexte de crise sanitaire du COVID-19 et de mon planning de rédaction/soutenance, je n'ai toujours pas eu l'occasion de revoir mes anciens collègues de STMicroelectronics et du laboratoire Ampère pour faire un pot de fin de thèse en "présentiel". Notez comme ce mot est rentré dans le langage courant. Un troisième confinement est actuellement mis en place. Je ne perds cependant pas espoir de pouvoir trinquer incessamment saoul peu :)

Bonne lecture.

Dissemination

The thesis work has been published or is being published through various conferences and journal publications, as well as miscellaneous contributions to workshops :

Conferences

- **Conférence des Jeunes Chercheurs en Génie Electrique (JCGE 2019)**

Romain David, Bruno Allard, Xavier Branca and Charles Joubert, "Etude et conception d'un circuit intégré de pilotage de diode laser (200MHz, 1W) pour un capteur d'image 3D reposant sur la mesure indirecte du temps de vol des photons," Conférence des Jeunes Chercheurs en Génie Electrique (JCGE), Oléron, France, 2019. [Digest & Poster]

- **International Conference on Integrated Power Electronics (CIPS 2020)**

Romain David, Bruno Allard, Xavier Branca and Charles Joubert, "Study and Design of an Integrated CMOS Laser Diode Driver for an iToF-based 3D Image Sensor," 11th International Conference on Integrated Power Electronics Systems (CIPS), Berlin, Germany, 2020. [Publication only]

- **European Conference on Power Electronics and Applications (EPE'20 ECCE Europe 2020)**

Romain David, Bruno Allard, Xavier Branca and Charle Joubert, "A 3A Low Voltage Laser Diode Driver IC in a CMOS technology for an iToF-based 3D image sensor," 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), Lyon, France, 2020. [Publication only]

Journal

- **Microelectronics Journal, Elsevier (submitted on February 2021)**

Romain David, Bruno Allard, Xavier Branca and Charles Joubert, "Design of an Integrated Laser Diode Driver for 3D-Depth Sensing Applications," Microelectronics Journal, Elsevier.

Miscellaneous

- **International Power Supply on-Chip Workshop (PowerSoC 2018)**

Romain David, Bruno Allard, Xavier Branca and Charles Joubert, "Study and Design of an Integrated VCSEL Driver (150MHz, 1W) for an iToF 3D-based CMOS Image Sensor," International Power Supply on-Chip Workshop (PowerSoC), Taïwan, 2018. [Poster only]

Abstract

Three-dimensional (3D) image sensors are key enablers for unlocking emerging applications in consumer electronics such as facial recognition, presence detection, gesture control or Augmented Reality (AR). These sensors mostly rely on range measuring techniques such as structured-light or Time-of-Flight (ToF) principles. The indirect Time-of-Flight (iToF) principle offers the advantage of a simple, reliable and cost-effective solution for mobile applications by using a laser transmitter and an image sensor. Its operating principle is to calculate a distance by measuring the phase shift between a modulated infrared laser signal and the optical signal received by the sensor after reflection on an object from the scene.

The thesis focused on the development of the laser transmitter, including the emitter and its driving circuitry. Laser pulses with a duty cycle close to 50% are usually sent through the scene by modulating the current through a semiconductor laser diode. The scientific contribution of the work is the study and the design of a compact, cost-effective and efficient Laser Diode Driver (LDD) for 3D-depth sensing applications used in mobile phones. The major objective is to validate an integrated architecture for the driver capable of generating short current pulses of few Amps with a 2.5ns pulse width up to a 200MHz pulse repetition frequency in order to reach a millimeter depth accuracy at few meters of distance. Primary issues addressed in this work are the high level of current and the shaping of short-duration pulse at high repetition frequency because of the parasitic elements in passive components, packages and PCB interconnections. In addition, mobile phones bring strong constraints on design choices such as dealing with the restricted available space and accommodating the limited input voltage range of a battery, typically from 2.8V up to 4.2V. Finally, high efficiency and low losses are critical for saving the battery lifetime and minimizing any self-heating.

The state-of-the-art of laser diode drivers for ToF applications is reviewed as well as a preliminary design study in order to evaluate the feasibility of several driver architectures in a STMicroelectronics' 130nm CMOS technology. Two different driving topologies, implementing a DC/DC converter connecting a switching element either in series or in parallel with a laser diode, have been retained as basis for designing the laser diode driver. The novelty here concerns the integration of the whole driver (except the laser diode and some

passive components) on a single chip while accommodating mobile phone constraints. Another important requirement concerns the high voltage spikes occurring during fast transients due to stray inductance. In order to save time and design resources, it has been decided to reuse an IC issued from previous developments, comprising two DC/DC converters for implementing the two drivers. In this way, only a single chip were considered. Various prototypes have been realized using the hcmos9a 130nm analog and mixed signal process. Both electrical and optical measurements have been performed in order to highlight performances and limitations. Both drivers are able to generate current pulses up to 3A with a 2.5ns pulse width at a maximum 200MHz frequency under a 3.6V supply voltage. Under theses conditions, the IC prototypes provide an average output electrical power of 4.5W to the laser diode with an electrical efficiency of around 60%. Nevertheless, more measurements are required to fully validate the prototypes at system level in a typical ToF application.

Keywords — "3D Image Sensor", "Time-of-Flight", "Laser Diode Driver", "VCSEL", "DC/DC Converter", "Integrated Power Management"

Résumé

Les nouveaux capteurs d'image 3D sont des éléments clés pour exploiter pleinement les applications émergentes dans les domaines de l'imagerie 3D et de la vision par ordinateur telles que la reconnaissance faciale, la capture de mouvement, la détection de présence ou encore la réalité augmentée. Ces capteurs reposent essentiellement sur une technique de mesure de distance. Parmi celles-ci, la mesure indirecte du temps de vol des photons présente l'avantage d'une mise en œuvre simple, fiable et économique appropriée aux applications mobiles grâce au fonctionnement conjugué d'un capteur d'image et d'une diode laser. Le principe consiste à calculer une distance en mesurant le déphasage entre un signal laser infrarouge modulé et le signal optique renvoyé après réflexion sur un objet de la scène.

Le travail de thèse se concentre sur le développement de l'émetteur laser, incluant la diode laser et sa circuiterie de pilotage. Des impulsions laser avec un rapport cyclique proche de 50% sont généralement utilisées comme signal laser en modulant le courant à travers une diode laser. La contribution scientifique de la thèse est l'étude et la conception d'un pilote de diode laser, qui soit à la fois compact, efficace et peu cher, pour des applications d'imagerie 3D utilisées dans les téléphones portables. Le principal objectif est de valider une architecture intégrée pour le pilote capable de générer de courtes impulsions de courant de quelques Ampères avec une largeur d'impulsion de 2,5ns à une fréquence maximale de 200MHz, dans le but d'atteindre une précision de mesure de l'ordre du millimètre à quelques mètres de distance. Les problématiques concernent le niveau élevé du courant et la formation d'impulsions très courtes à haute fréquence à cause des éléments parasites présents dans les boîtiers et les interconnexions. De plus, les applications mobiles apportent des contraintes supplémentaires dans les choix de conception, notamment vis-à-vis des plages de tension limitées des batteries utilisées (2,8V - 4,2V) mais aussi de la place disponible très restreinte à cause des nombreuses fonctions embarquées. Enfin, un fort rendement électrique s'avère indispensable dans le but de prolonger l'autonomie de la batterie et minimiser l'auto-échauffement.

L'état de l'art des pilotes de diode laser pour application "Temps de Vol" est passé en revue, ainsi qu'une étude préliminaire de conception afin d'évaluer la faisabilité de plusieurs architectures de pilotes dans une technologie CMOS 130nm de STMicroelectronics. Deux

topologies de pilotage différentes, mettant en oeuvre un convertisseur DC/DC associé à un élément de commutation connecté soit en série soit en parallèle de la diode laser, ont été retenues comme base pour concevoir le pilote de diode. La nouveauté ici concerne l'intégration du pilote entier (hormis la diode laser et quelques composants passifs) sur une seule puce tout en respectant les contraintes des téléphones portables. Un autre défi important concerne les pics de tension se produisant pendant les transitoires rapides dus aux inductances parasites. Afin de gagner du temps et des ressources de conception, il a été décidé de réutiliser un circuit intégré issu de développements précédents, comprenant deux convertisseurs DC / DC pour la mise en œuvre des deux pilotes. De cette manière, une seule puce a pu être considérée. Plusieurs prototypes ont été réalisés en utilisant la technologie analogiques et mixtes hcmos9a 130nm. Des mesures électriques et optiques ont été réalisées afin de mettre en évidence les performances et les limites. Les deux pilotes sont capables de fournir des impulsions de courant jusqu'à 3A avec une largeur d'impulsion de 2,5ns à une fréquence maximale de 200MHz sous une tension d'alimentation de 3,6V. Dans ces conditions, les prototypes de circuit intégré délivre une puissance électrique de sortie moyenne de 4,5W à la diode laser avec un rendement électrique d'environ 60%. Néanmoins, davantage de mesures sont nécessaires pour valider complètement les prototypes au niveau système dans une application "Temps de Vol" typique.

Mots clés — "Capteur d'Image 3D", "Temps de Vol", "Pilote de Diode Laser", "VCSEL", "Convertisseur DC / DC", "Gestion de l'Alimentation Intégrée"

Résumé étendu

Cette partie propose un résumé étendu en français du manuscrit de thèse.

Introduction Générale

Applications de détection de profondeur 3D

Les systèmes de détection de profondeur sont des capteurs capables de produire une image contenant des informations de profondeur d'une scène, aussi appelée carte de profondeur. Associés à des capteurs d'image conventionnels, produisant des images bidimensionnelles (2D) standards, ils sont capables de reconstituer une image en trois dimensions (3D).

Ces nouveaux capteurs d'image 3D sont des éléments clés pour exploiter pleinement les applications émergentes dans les domaines de l'imagerie 3D et de la vision par ordinateur telles que les véhicules autonomes, la reconnaissance faciale, la capture de mouvement, la détection de présence ou encore la réalité augmentée. Plus récemment, dans le contexte de la crise sanitaire de la Covid-19, une forte demande de technologies favorisant la distanciation sociale et permettant d'éviter de toucher les appareils émergera dans un avenir proche. Bien que des solutions existent déjà pour des applications similaires, la détection de profondeur pourrait être bénéfique pour répondre à cette nouvelle demande en développant des systèmes plus efficaces et moins coûteux.

Marché des capteurs d'image et motivations

Les capteurs d'image 3D reposent principalement sur des techniques de mesure de distance utilisant les ondes lumineuses. Selon la technique employée, les systèmes utilisent des composants optoélectroniques tels que des capteurs d'image et des émetteurs laser. En 2018, l'électronique grand public (smartphones, tablettes, PC portables, appareils photo numériques, etc...) reste le principal secteur du marché des capteurs d'image CMOS représentant 73% des parts de marché. Il semble donc être un secteur prometteur pour le développement de futurs capteurs d'image 3D spécialement pour les téléphones mobiles.

Malgré de nombreuses recherches sur les techniques d'imagerie tridimensionnelles lancées à la fin des années 1970, le premier produit grand public n'a émergé qu'en 2010 avec la caméra 3D nommée Kinect™ et développée par Microsoft en collaboration avec Prime Sense. La caméra était destinée aux jeux vidéos, permettant à l'utilisateur de contrôler le jeu grâce aux mouvements du corps.

Plus récemment, des entreprises dédiées aux applications d'imagerie 3D et des entreprises leaders dans l'industrie des semiconducteurs ont établi de solides collaborations afin de développer de nouvelles solutions pour les téléphones mobiles. STMicroelectronics a notamment lancé en 2014 son premier capteur de télémétrie VL6180X intégré à l'avant des téléphones mobiles en tant que capteur de proximité pour la détection des utilisateurs jusqu'à 10cm, principalement utilisé pour verrouiller le téléphone lors des appels. Ensuite, il a annoncé de nouveaux capteurs de télémétrie tels que le module VL53L0X mesurant des distances jusqu'à 2m utilisé pour la détection de présence et le module VL53L1 pour la détection multi-objets jusqu'à 4,5m aidant la mise au point automatique des caméras dans les smartphones par exemple.

Le département Analog, MEMS and Sensors" de STMicroelectronics, dans lequel se déroule cette thèse, souhaite étendre sa gamme de capteurs télémétriques en développant un nouveau capteur d'image 3D destiné aux téléphones portables et capable de cartographier une scène en trois dimensions.

Objectifs de la thèse

Dans ce contexte, plusieurs techniques de mesure de distance peuvent être envisagées pour le développement du capteur. Parmi celles-ci, la mesure indirecte du temps de vol des photons présente l'avantage d'une mise en œuvre simple, fiable et économique appropriée aux applications mobiles grâce au fonctionnement conjugué d'un capteur d'image et d'une diode laser. Le principe consiste à calculer une distance en mesurant le déphasage entre un signal laser infrarouge modulé et le signal optique renvoyé après réflexion sur un objet de la scène.

Le travail de thèse se concentre sur le développement de l'émetteur laser, incluant la diode laser et sa circuiterie de pilotage. Des impulsions laser avec un rapport cyclique proche de 50% sont généralement utilisées comme signal laser en modulant le courant à travers une diode laser. La contribution scientifique de la thèse est l'étude et la conception d'un pilote de diode laser, qui soit à la fois compact, efficace et peu cher, pour des applications d'imagerie 3D utilisées dans les téléphones portables.

Le principal objectif est de valider une architecture intégrée pour le pilote capable de générer de courtes impulsions de courant de quelques Ampères avec une largeur d'impulsion de 2,5ns à une fréquence maximale de 200MHz, dans le but d'atteindre une précision de mesure de l'ordre du millimètre à quelques mètres de distance. Les problé-

matiques concernent le niveau élevé du courant et la formation d'impulsions très courtes à haute fréquence à cause des éléments parasites présents dans les boîtiers et les interconnexions. De plus, les applications mobiles apportent des contraintes supplémentaires dans les choix de conception, notamment vis-à-vis des plages de tension limitées des batteries utilisées (2,8V - 4,2V) mais aussi de la place disponible très restreinte à cause des nombreuses fonctions embarquées. Enfin, un fort rendement électrique s'avère indispensable dans le but de prolonger l'autonomie de la batterie et minimiser l'auto-échauffement.

Contenu du manuscrit

- Le chapitre 1 présente l'état de l'art des pilotes de diode laser pour les applications "Temps de Vol", permettant d'identifier les topologies les plus appropriées pour concevoir le pilote de diode laser.
- Le chapitre 2 propose une étude de conception préliminaire pour évaluer la faisabilité de plusieurs architectures de pilotes dans une technologie CMOS 130nm de STMicroelectronics. Une analyse comparative est proposée pour mettre en évidence les avantages et les inconvénients de chaque solution.
- Le chapitre 3 se concentre sur la conception et la mise en œuvre du prototype de pilote de diode laser. Certains choix de conception étant conventionnels, certains blocs de construction issus de développements précédents ont été réutilisés afin d'économiser du temps et des ressources. Plusieurs prototypes ont été réalisés.
- Le chapitre 4 détaille les résultats de mesures électriques et optiques obtenus sur tous les prototypes.
- La conclusion générale résume les principales contributions obtenues au cours du travail de thèse. Des investigations supplémentaires sont nécessaires pour valider le prototype au niveau du système en considérant une application de "Temps de Vol" typique.

Chapitre 1: État de l'Art

Ce chapitre présente une revue de l'état de l'art des pilotes de diode laser dédiés aux applications "Temps de Vol". La méthodologie de l'étude consiste à trouver une classification des circuits à partir de la littérature et de l'industrie afin de mieux mettre en évidence leurs avantages et limites communs. Cela aidera à identifier la topologie pertinente pour la conception du pilote de diode laser conformément aux spécifications.

Cadre de l'étude

Le pilote, associé à une diode laser, doit être capable de générer de courtes impulsions optiques de forte amplitude à une fréquence élevée tout en fonctionnant sur une faible plage de tensions d'alimentation. Il existe deux types de méthode pour moduler un signal optique :

- Le méthode de modulation externe consiste à utiliser un modulateur électro-optique pour moduler le signal optique provenant de la diode laser, qui est toujours allumée, en fonction d'un signal de commande.
- La méthode de modulation directe consiste à moduler le signal optique en modulant directement le courant traversant la diode laser, en fonction d'un signal de commande.

La méthode de modulation externe produit un signal optique de meilleure qualité avec une largeur de raie spectrale plus étroite contrairement à la méthode de modulation directe, mais elle est généralement plus coûteuse et encombrante en raison du couplage requis entre la source laser et le modulateur externe. La méthode de modulation directe est donc préférée ici en raison de son faible coût et de sa complexité réduite. Les circuits de pilotages utilisant cette méthode de modulation directe sont généralement destinés aux applications de communications optiques pour la transmission de données à haute vitesse. Cependant, ces topologies restent limitées à des puissances optiques allant jusqu'à quelques centaines de mW. Par conséquent, la revue de l'état de l'art se concentre uniquement sur les circuits de la littérature et de l'industrie dédiés aux applications "Temps de Vol" ou autres applications où les ordres de grandeur de puissance et de vitesse sont similaires aux spécifications du travail de thèse.

Les pilotes étudiés peuvent être divisés en deux classes principales, selon Glaser *et al.* La classification dépend de la façon dont l'impulsion est contrôlée. Il existe des pilotes résonants à décharge capacitive et des pilotes à impulsion rectangulaire :

- Les pilotes à décharge capacitive génèrent des impulsions de courant uniquement en déclenchant le front montant. Le principe repose sur une décharge capacitive pour produire l'impulsion. La largeur d'impulsion de courant est généralement plus courte que la largeur d'impulsion de la commande appliquée au circuit d'attaque.

- Les pilotes à impulsion rectangulaire génèrent des impulsions de courant en déclenchant à la fois les fronts montant et descendant. La largeur d'impulsion de courant est à peu près égale à la largeur d'impulsion de la commande appliquée au circuit d'attaque.

Le principe de fonctionnement, les propriétés, avantages et limites de ces topologies de pilotes sont détaillés ci-après.

Topologies de pilote résonant à décharge capacitive

Trois configurations majeures peuvent être distinguées pour ce type de pilote. Elles reposent cependant sur le même principe de fonctionnement proposé initialement par Kilpelä *et al* : des impulsions de courant sont générées en chargeant un condensateur à une tension prédéfinie, puis en le déchargeant via un interrupteur et une diode laser. L'impulsion de courant est terminée lorsque le condensateur est totalement déchargé. La largeur de l'impulsion ainsi que sa valeur crête sont déterminées par les paramètres du circuit RLC équivalent. Les principales différences entre les trois configurations résident dans la façon de charger le condensateur. Une diode de serrage peut être ajoutée pour protéger la diode laser des éventuelles surtensions apparaissant lors des transitoires rapides.

Cette topologie de pilote à décharge capacitive présente de nombreux avantages, tels qu'une conception relativement simple acceptant l'inductance parasite dans son fonctionnement ainsi qu'un contrôle sur l'énergie de l'impulsion éliminant l'emballement thermique et offrant une meilleure répétabilité dans la génération d'impulsions. De plus, la largeur d'impulsion du signal de commande appliqué au circuit d'attaque peut être plus longue que la largeur d'impulsion de courant, ce qui donne plus de flexibilité pour sa conception en particulier sur les caractéristiques de vitesse.

En revanche, l'un des inconvénients majeurs concerne la largeur d'impulsion qui dépend des valeurs du condensateur et de l'inductance parasite, fixées pour une conception donnée, tandis que l'amplitude de l'impulsion dépend de la tension d'alimentation et du condensateur également. Par conséquent, il est impossible de contrôler séparément la largeur et l'amplitude de l'impulsion. Un autre problème est le temps nécessaire pour charger la capacité limitant ainsi la fréquence de répétition des impulsions. De plus, une tension d'alimentation relativement élevée peut être nécessaire pour obtenir un courant crête élevé, ce qui peut augmenter la complexité de conception, le coût et l'espace nécessaires au système.

Topologies de pilote à impulsion rectangulaire

Deux topologies principales peuvent être distinguées pour ce type de pilote :

- Les pilotes en mode tension reposent sur une source de tension pour contrôler la polarisation de la diode laser.

- Les pilotes en mode courant reposent sur une source de courant pour contrôler la polarisation de la diode laser.

Pilote en mode tension

Ce type de pilote peut être divisé en deux configurations : série et capacité commutée. Dans la configuration série, une source de tension est connectée en série avec une diode laser et un interrupteur. L'impulsion de courant est générée lorsque l'interrupteur s'active puis se désactive selon le signal de commande. La valeur crête de l'impulsion est déterminée par la source de tension polarisant la diode laser. La configuration à capacité commutée reprend la configuration série mais propose d'implémenter la source de tension à l'aide d'un convertisseur à pompe de charge synchrone avec l'interrupteur. Une diode de serrage, ou un autre interrupteur, peut être ajoutée pour protéger la diode laser des éventuelles surtensions apparaissant lors des transitoires rapides.

Cette topologie de pilote en mode tension bénéficie d'un contrôle de la largeur d'impulsion en raison du principe inhérent aux pilotes à impulsion rectangulaire. Une fréquence élevée peut être atteinte, notamment grâce à l'utilisation d'un fort condensateur de découplage, qui n'est que partiellement déchargé entre chaque impulsion. De plus, la valeur de courant crête est indépendante du réglage de la largeur d'impulsion et seule une commande de la tension de polarisation de la diode laser est nécessaire pour ajuster sa valeur. Ces propriétés permettent de configurer des séquences d'impulsions flexibles ne dépendant pas du condensateur et des inductances parasites, au premier ordre.

Cependant au second ordre, l'inductance parasite est une limitation majeure qui doit être prise en compte pour estimer la polarisation correcte de la diode laser. Habituellement, la tension d'alimentation doit être suffisamment élevée pour surmonter les inductances et résistances parasites. En outre, des boucles de contrôle peuvent être nécessaires pour assurer une meilleure répétabilité dans la génération d'impulsions en raison des variations de température et de tension. Toutes ces fonctionnalités supplémentaires peuvent augmenter la complexité de conception, le coût et l'espace nécessaires au système.

Pilote en mode courant

Ce type de pilote peut être divisé en deux configurations : source de courant et parallèle, qui reposent sur des principes de fonctionnement différents. Dans la configuration en source de courant, une diode laser est généralement associée en série à une source de courant et un interrupteur agissant alors comme une source de courant commutée. L'impulsion de courant est générée lorsque l'interrupteur s'active puis se désactive selon le signal de commande. La valeur crête de l'impulsion est déterminée par la source de courant polarisant la diode laser. Dans la configuration parallèle, une source de courant est connectée à la diode laser avec l'interrupteur en parallèle. L'impulsion de courant est générée lorsque l'interrupteur s'active puis se désactive en opposition de phase avec le

signal de commande.

Cette topologie de pilote bénéficie aussi d'un contrôle de la largeur d'impulsion avec une fréquence élevée. De plus, la valeur de courant crête est indépendante du réglage de la largeur d'impulsion et seule une commande sur le courant de polarisation de la diode laser est nécessaire pour ajuster sa valeur. Ces propriétés permettent de configurer des séquences d'impulsions flexibles ne dépendant pas des inductances parasites, au premier ordre.

Cependant au second ordre, une limitation majeure de la configuration source de courant concerne la tension d'alimentation relativement élevée nécessaire pour correctement polariser la source de courant, ce qui peut conduire à une augmentation de la dissipation de puissance. Concernant la configuration parallèle, la complexité pourrait provenir de l'implémentation de la source de courant où l'obtention d'un courant idéal n'est pas une pratique faisable. De plus, des boucles de contrôle peuvent également être requises pour une meilleure répétabilité dans la génération d'impulsions en raison des variations de température et de tension. Ces fonctionnalités supplémentaires peuvent augmenter la complexité de conception, le coût et l'espace nécessaires au système.

Discussion et conclusion

Pour rappel, l'objectif majeur de la thèse est de valider une architecture intégrée pour un pilote de diode laser capable de générer de courtes impulsions de courant de forte amplitude avec une fréquence élevé. Le courant de crête doit être configurable jusqu'à quelques ampères pour gérer les caractéristiques de la diode laser et conserver une certaine flexibilité de conception. Le fréquence doit également être programmable de dizaines à centaines de MHz pour répondre aux spécifications. En outre, il convient de rappeler que la plage de tension d'entrée est limitée, généralement de 2,8V à 4,2V, et que l'efficacité énergétique est considérée comme une exigence majeure à atteindre.

Il existe plusieurs topologies de pilote capables de fournir des impulsions de courant courtes et élevées. Les topologies de pilote à décharge capacitive sont très populaires en raison de leur conception relativement simple acceptant l'inductance parasite. Mais la dépendance des caractéristiques des impulsions sur les paramètres du circuit équivalent RLC et de la tension d'alimentation rend cette approche limitée par rapport aux objectifs visés. Pour ces raisons, ces topologies ne sont pas adaptées pour concevoir le pilote de diode laser.

En ce qui concerne les topologies de pilote à impulsion rectangulaire, la discussion est plus compliquée. Un inconvénient important pour les topologies d'attaque en mode courant en configuration source de courant, ainsi que pour les topologies d'attaque en mode tension, est la tension d'alimentation relativement élevée. Pour cette raison, la topologie d'attaque en mode courant en configuration parallèle pourrait être une solution potentielle pour le pilote de diode laser.

Parmi les topologies de pilote en mode tension, la configuration à capacité commutée est moins flexible que la configuration en série en raison de la structure inhérente du convertisseur à pompe de charge. En effet, cette architecture est destinée à fournir une tension constante fixant ainsi la tension de polarisation de la diode laser et la valeur du courant de crête. La configuration série pourrait être une solution plus polyvalente permettant de mettre en œuvre une architecture adaptée pour ajuster la tension de polarisation de la diode laser en fonction du courant souhaité.

En résumé, le pilote en mode tension en configuration série ainsi que le pilote en mode courant en configuration parallèle semblent être de bons candidats pour le pilote de diode laser. Cependant, même si le pilote en mode courant en configuration source de courant peut impliquer une dissipation de puissance plus élevée en raison de la marge de tension requise pour la polarisation de la source de courant, trop peu de résultats en termes de performances transitoires, de métriques de puissance et de fonctionnalités sont fournis dans la littérature pour conclure sur ce type de topologie.

Enfin et en conséquence, il est indispensable de réaliser une étude de conception préliminaire pour évaluer la faisabilité de ces trois solutions par rapport aux objectifs visés à l'aide d'une technologie adaptée. Cette étude se concentre principalement sur la faisabilité de l'intégration du pilote de diode laser sur une seule puce tout en tenant compte des contraintes de la téléphonie mobile et en considérant l'efficacité énergétique comme une exigence majeure.

Chapitre 2: Étude de Conception Préliminaire

Ce chapitre présente une étude de conception préliminaire pour évaluer la faisabilité de plusieurs architectures de pilotes. Des simulations simples utilisant des modèles issus de la technologie CMOS 130nm de STMicroelectronics sont effectuées afin d'identifier les principales caractéristiques et de mettre en évidence les avantages et les inconvénients de chaque solution. Une analyse comparative utilisant plusieurs indicateurs clés de performance est ensuite proposée. La solution la plus adaptée par rapport aux spécifications sera utilisée comme base pour la conception du prototype de pilote de diode laser.

Spécification du pilote de diode laser

Cette section détaille les conditions de fonctionnement et les spécifications du pilote de diode laser.

Conditions de fonctionnement

Le pilote de diode laser est destiné au secteur de l'électronique grand public et applications mobiles. Une plage de température ambiante maximale comprise entre 0°C et 70°C est nécessaire pour garantir le bon fonctionnement de l'appareil. La tension d'alimentation des batteries Li-ion, couramment utilisées dans ces applications, varie généralement de 2,8V à 4,2V. Dans l'hypothèse d'un scénario catastrophe, il a été décidé de considérer ici une plage de tension d'alimentation de 2,5V à 4,8V avec une valeur typique de 3,6V.

Modulation et budget de puissance optique

Pour rappel, Des impulsions laser avec un rapport cyclique proche de 50% sont généralement utilisées comme signal de modulation, correspondant à une méthode de modulation dite continue. Dépendant de la distance maximale, des conditions d'éclairage, de la réflectivité des objets, de l'efficacité du capteur et des normes de sécurité liées à l'utilisation des dispositifs lasers, des impulsions optiques jusqu'à 2,5W pour une fréquence de modulation de 50MHz à 200MHz sont requises pour atteindre une profondeur maximale de 3m avec une précision inférieure à 0,5% de la profondeur.

Séquence d'illumination

Une séquence d'illumination spécifique basée sur plusieurs trains d'impulsions est nécessaire au capteur d'image pour acquérir des données et fournir une carte de profondeur complète. En fonction des spécifications et des normes de sécurité oculaire, un cycle d'illumination (un train d'impulsions suivi d'un temps d'inactivité) est fixé à une période de 3ms avec un temps d'illumination maximum de 1ms et un temps d'extinction minimum de 2ms. Un rapport cyclique d'illumination typique de 33% peut être envisagé.

Choix de la diode laser

Deux types de diodes laser à semi-conducteur sont largement utilisés en électronique : la diode laser conventionnelle et la diode laser à cavité verticale émettant par la surface (VCSEL en anglais). Une caractéristique importante des VCSEL est que la lumière est émise à partir de la surface des couches semi-conductrices, contrairement aux diodes conventionnelles où la lumière est émise depuis la tranche des couches semi-conductrices. Les VCSEL présentent de nombreux autres avantages tels qu'une large bande passante, un faisceau laser de haute qualité ou un faible coût de fabrication, ce qui les rend très attractifs pour les applications d'illumination.

Un module de VCSEL haute puissance émettant par le haut a été choisie pour répondre aux contraintes de faible coût et de compacité. Il est emballé dans un boîtier en céramique sur mesure de 3,5x3,5x1,6mm. Il comprend également un diffuseur pour homogénéiser et personnaliser le profil d'intensité sur un champ d'éclairage de 60x45°. Les principales caractéristiques électro-optiques du module VCSEL sont issues de la fiche technique du composant mais ne sont renseignées qu'à 25°C en raison d'un manque de données du fournisseur (principalement pour des raisons de secret commercial ou de marketing). Un point important à noter est qu'une impulsion de courant de 3A est nécessaire pour générer une impulsion laser d'environ 2,5W, comme exigé selon les spécifications.

Modèle électro-optique du VCSEL

Un modèle électro-optique large signal du module VCSEL est indispensable pour simuler son comportement, valider la mise en œuvre du circuit et évaluer les performances du système. Malheureusement, un modèle suffisamment précis n'a pas été fourni par le fournisseur. Néanmoins, un modèle SPICE électro-optique simple est proposé pour les simulations DC et transitoires uniquement. Il comprend un modèle de diode Berkeley " niveau 1" (fichier SPICE) pour modéliser le comportement électrique du VCSEL, associé à des composants passifs pour modéliser les parasites du boîtier. Le fichier SPICE a été livré par le fournisseur tandis que les valeurs des parasites ont été extraites de mesures de paramètres S. Enfin, le comportement optique du module VCSEL est modélisé à l'aide d'équations DC simples basées sur la caractéristique typique de sortie. Comme ce modèle optique proposé n'est valable que dans des conditions DC, les résultats optiques des simulations transitoires devront être considérés avec précaution.

Contrôle de la puissance optique et boucle de courant

En raison de la forte dépendance à la température des caractéristiques électro-optiques du VCSEL, il semble essentiel d'utiliser une boucle de régulation afin de contrôler la puissance optique de sortie. Habituellement, une photodiode capture une partie de la puissance optique de sortie générant ainsi un courant qui peut être utilisé comme signal

de rétroaction pour ajuster le courant à travers la diode laser, donc la puissance optique de sortie. La méthode adoptée ici est de réguler directement le courant à travers le VCSEL sans utiliser de photodiode, réduisant ainsi le coût et la complexité mais au détriment de la précision. Cependant, cela peut toujours garantir un contrôle précis sur une plage de température limitée. En effet, le courant de seuil variant de manière parabolique avec la température, il peut être considéré comme constant pour une plage de température limitée.

Technologie CMOS

Une approche intégrée pour le pilote de diode laser s'avère indispensable pour développer un système compact, rapide et peu coûteux. Cela permet de s'affranchir des éléments parasites dus aux boîtiers de composants et aux interconnexions par rapport à une approche utilisant des composants discrets, améliorant ainsi les performances transitoires et réduisant les pertes. La technologie CMOS 130nm de STMicroelectronics est une technologie à faible coût bien adaptée pour intégrer des fonctionnalités analogiques, numériques et de puissance sur une seule puce. Plus particulièrement, la technologie analogique hcmos9a utilisée dans le cadre de ce travail, offre une large gamme de dispositifs actifs et passifs tels que des diodes P-N classiques et Schottky, des transistors bipolaires (BJT), des transistors à effet de champ à grille métal-oxyde (MOSFET) faible et forte tensions (1,2V, 4,8V et 20V), des résistances poly, actives et métalliques ainsi que des condensateurs métal-oxyde-métal (MOM), métal-isolant-métal (MIM) et métal-oxyde-semi-conducteur (MOS).

Efficacité énergétique

L'efficacité énergétique du système est ici une préoccupation majeure car elle impacte l'auto-échauffement des appareils, donc les performances, ainsi que la durée de vie de la batterie. Idéalement, plus le rendement électrique est élevé, mieux c'est. Dans ce contexte, une valeur minimale peut être définie en dessous de laquelle le système ne peut assurer un bon fonctionnement. Avec une puissance électrique de sortie autour de 1,35W, une valeur minimale de rendement de 70 % est considéré comme limite la plus basse afin de conserver une marge de sécurité.

Résumé

Pour résumer, le pilote doit être capable de générer de courtes impulsions de courant de forte amplitude avec une fréquence élevée sur une plage de tension d'alimentation de 2,5V à 4,8V. L'amplitude du courant, également appelée courant à l'état ON I_{ON} par la suite, doit être configurable jusqu'à 3A pour s'adapter aux caractéristiques du VCSEL en raison des variations thermiques et du processus de fabrication, mais aussi pour conserver une certaine flexibilité de conception. La fréquence de modulation f_{MOD} doit être également programmable de 50MHz à 200MHz pour répondre au principe de mesure indirecte du

temps de vol des photons. En supposant un rapport cyclique de modulation de 50%, cela conduit à générer des impulsions de courant avec une largeur d'impulsion allant de 2,5ns à 10ns. Bien que la spécification de rendement électrique ait été approximativement estimée, une valeur élevée est essentielle pour ce travail afin d'assurer de bonnes performances de l'ensemble du système. Ce rendement est donc considéré comme une exigence majeure à atteindre.

Méthodologie d'évaluation

La première partie de l'étude préliminaire concerne l'analyse des formes d'onde transitoires pour les trois architectures concernées, à l'aide de simulations simples utilisant les modèles du kit de conception. L'analyse pourrait être divisée en deux phases transitoires : la phase montante lorsqu'un courant s'établit à travers la diode laser pour initier l'impulsion laser et la phase descendante lorsque le courant s'éteint pour arrêter l'impulsion laser.

L'objectif principal n'est pas d'identifier en profondeur tous les mécanismes de transition à l'aide d'équations analytiques car assez complexes, mais plutôt de trouver des tendances à l'aide de calculs manuels qui restent prévisibles jusqu'à un certain point. Cela peut être utile pour mettre en évidence certains problèmes de conception et aider à sélectionner la topologie adéquate. Il faut préciser que l'analyse transitoire sera effectuée uniquement dans des conditions typiques (procédé typique, tension d'entrée de 3,6V et température ambiante de 25°C). De plus, le comportement du circuit vis-à-vis de la température ne sera pas étudié au cours de ces travaux.

Un dispositif MOSFET est généralement utilisé pour mettre en œuvre l'interrupteur. En effet, un dispositif BJT aurait des pertes de conduction trop importantes car contrôlé en courant. Puisque les modèles MOSFET fournis par le kit de conception sont assez complexes, un modèle simple est préféré pour l'explication, prenant en compte les paramètres de base tels que la résistance à l'état ON, la capacité drain-source, la capacité d'entrée ou encore l'effet de la body diode (lorsque le substrat et la source sont court-circuités).

Certaines considérations seront ensuite discutées dans la deuxième partie de l'étude préliminaire en introduisant les blocs fonctionnels majeurs. Le but ici n'est pas de concevoir et d'optimiser complètement chaque solution, mais plutôt d'aborder les principaux problèmes de conception et de mettre en évidence les fonctionnalités clés. Cela pourrait être utile pour comparer les solutions et concevoir le prototype de pilote de diode laser. Un point essentiel concerne le circuit de gestion de puissance pour polariser la diode laser en fonction de la plage de tension d'entrée et du courant visé. Il faut préciser que ce choix sera motivé par les spécifications en termes de puissance et de rendement.

La dernière partie de l'étude préliminaire concerne l'analyse comparative des solutions proposées. Les architectures n'étant pas complètes, il sera compliqué d'évaluer avec préci-

sion les performances de chacune d'entre elles, notamment en termes de rendement électrique et de puissance dissipée. Mais les pertes importantes pourraient être évaluées par des calculs manuels afin d'identifier les blocs critiques. Ensuite, une approche systémique sera préférée où les avantages et les inconvénients de chaque solution concernant divers indicateurs seront rassemblés et discutés à l'aide d'une analyse qualitative. Par exemple, le coût en termes de complexité de conception, de surface de silicium, de composants passifs, d'empreinte PCB et de puissances dissipées sera abordé. Une métrique dédiée à l'application "Temps de Vol" pourra être utilisée comme indicateur supplémentaire, proposant d'évaluer l'erreur systématique introduite sur la mesure de profondeur due à l'utilisation d'un signal de modulation pulsé au lieu d'un signal sinusoïdal traditionnellement utilisé dans les algorithmes conventionnels.

Solution 1: pilote en mode tension en configuration série

La première solution proposée repose sur la topologie du pilote en mode tension utilisant une configuration série. Le schéma du banc de simulation transitoire inclut une source de tension connectée en série avec la diode laser, un élément de commutation ainsi que les éléments parasites. Il a été choisi d'implémenter l'élément de commutation à l'aide d'un transistor MOSFET à canal n (NMOS) afin de simplifier le circuit car référencé à la masse. Le transistor est un NMOS à oxyde épais de 4,8V et a été dimensionné arbitrairement avec une longueur minimale (L=0,5µm) et une grande largeur (W = 50mm) pour bénéficier d'une résistance ON suffisamment faible. Les simulations ont été réalisées dans des conditions typiques pour un courant à l'état ON élevé (3A) et pour diverses valeurs de fréquence (50MHz et 200MHz). La tension de sortie a été réglée en fonction du courant à l'état ON.

L'introduction d'éléments parasites a un impact significatif sur les transitoires de courant et de tension, que ce soit pendant les phases de montée ou de descente, comme expliqué ci-après :

- Le temps de montée du courant est relativement lent. Il est clairement dominé par la constante de temps du circuit RL équivalent. Lorsque la constante de temps est du même ordre de grandeur que la largeur d'impulsion, le courant n'atteint pas sa valeur cible. Dans tous les cas, les éléments parasites pourraient ajouter un délai entre le déclenchement de l'impulsion et l'établissement du courant photo-générateur, ce qui pourrait provoquer une distorsion sur le signal laser.
- Lors de la phase de descente, une résonance sur le courant et la tension est observée à la fois à faible et forte fréquences de modulation, due au circuit RLC équivalent, mais qui semble bien amortie par la body diode du transistor NMOS. Cela traduit un temps de descente du courant relativement rapide. Aucun modèle optique n'étant valable pour les simulations transitoires, il est assez compliqué d'évaluer si cette

résonance a un impact sur le courant photo-générateur, donc le signal laser, mais il se pourrait que la diode laser émette des impulsions laser secondaires très courtes. De plus, des pics de tension supérieures à 15V sont observés sur la tension drain-source induisant de forts pics de courant négatifs. Ceci est causé par la coupure rapide du transistor associée aux inductances parasites. Ces pics de tension sont ici assez critiques car ils peuvent détruire le transistor, capable de supporter des tensions jusqu'à 4,8V seulement.

Le temps de montée du courant de diode est plus lent que le temps de descente provoquant une distorsion sur les impulsions laser. En conséquence, un point essentiel pour améliorer les performances transitoires de cette topologie consiste à minimiser les inductances parasites, confirmant l'intérêt d'utiliser une approche intégrée. De plus, cela contribue à réduire les pics de tension au niveau du nœud de commutation ainsi que l'éventuelle résonance. Augmenter la tension de sortie de la source de tension permettrait aussi d'améliorer les performances transitoires en prenant en compte les chutes de tension aux bornes des inductances parasites durant les transitoires.

Par la suite, quelques directives sur l'implémentation de la topologie proposée sont données pour répondre aux spécifications. La principale préoccupation concerne la source de tension. Elle doit être capable de fournir la bonne tension de sortie pour polariser la diode laser par rapport au courant à l'état ON et à la plage de tension d'entrée (2,5V - 4,8V). Elle doit également prendre en compte la chute de tension aux bornes des inductances parasites. Le choix sera également motivé par les exigences en terme de puissance telles que fournir un courant de sortie élevé avec un rendement électrique élevé. Par conséquent, il semble cohérent d'utiliser un convertisseur DC/DC qui est capable d'abaisser et d'augmenter la tension de sortie par rapport à la tension d'entrée avec n'importe quel rapport de conversion de tension tout en gardant la même polarité. Comme aucune isolation galvanique n'est requise, une structure de convertisseur DC/DC non isolée est préférable.

Comme d'habitude, choisir une structure parmi toutes les structures existantes nécessite des compromis entre performances, complexité, composants passifs, surface de PCB et de silicium, coût, etc. Pour simplifier l'étude, il a été décidé d'en limiter le cadre à des structures simples qui sont bien connues et décrites dans la littérature. Il existe trois grands types de convertisseurs : les régulateurs de tension linéaires, les convertisseurs DC/DC à capacité commutée (ou pompe de charge) et à inductance commutée. Tous ont des avantages et des inconvénients :

- Les régulateurs de tension linéaires, agissant comme un diviseur résistif, ne sont pas pertinents ici car ils ne peuvent être utilisés qu'en mode de fonctionnement abaisseur. Ils souffrent aussi d'un faible rendement (généralement de 20% à 60%).
- Les convertisseurs à capacité commutée utilisent un ensemble d'interrupteurs travaillant en association avec des condensateurs, en tant qu'élément de stockage d'énergie,

pour convertir la puissance. Ils peuvent être utilisés dans des modes de fonctionnement abaisseur ou élévateur en fonction de la topologie. Cependant, un rendement élevé n'est atteint que pour un rapport de conversion de tension particulier. Même si des topologies existent pour remédier à cette limitation, c'est au détriment d'une complexité accrue.

- Les convertisseurs à inductance commutée utilisent un ensemble d'interrupteurs travaillant en association avec des inductances et des condensateurs pour convertir la puissance. L'inductance est le principal composant de stockage de l'énergie. Ils peuvent être utilisés dans des modes de fonctionnement abaisseur ou élévateur et tout rapport de conversion de tension peut être atteint avec un rendement élevé, généralement de 70% à 95%. Néanmoins, des composants encombrants et hors puce, tels que des condensateurs ou des inductances de puissance, sont généralement nécessaires pour gérer des courants de quelques ampères ou obtenir une faible ondulation de tension de sortie.

Les convertisseurs à inductance commutée semblent être les plus appropriés dans ce contexte. Un convertisseur abaisseur-élévateur (dit buck-boost) non inverseur composé d'une seule inductance, d'un seul condensateur et de quatre interrupteurs est considéré ici, où la tension de sortie garde la même polarité que la tension d'entrée. Il bénéficie de moins de composants passifs hors puce que d'autres topologies, réduisant ainsi l'empreinte du PCB. La tension de sortie est ajustée en faisant varier le rapport cyclique appliqué aux interrupteurs. Il peut être utilisé dans trois modes différents (mode abaisseur ou buck, mode abaisseur-élévateur ou buck-boost et mode élévateur ou boost) en fonction des conditions de charge et de tension d'entrée. Un mode de conduction continue est préféré ici pour un rendement élevé, où une méthode de commutation monophasée pourrait être employée pour chaque mode afin de simplifier les circuits de commande.

Le pilote de diode laser comprend alors le convertisseur DC/DC, la diode laser et l'élément de commutation en série avec ses circuits de commande. Certaines recommandations spécifiques doivent cependant être prises en compte pour choisir les paramètres clés du pilote.

La fréquence de fonctionnement du convertisseur DC/DC pourra être suffisamment faible (<10MHz) par rapport à la fréquence de modulation (50MHz-200MHz). Ceci permettra de bénéficier à la fois d'une certaine flexibilité pour la mise en œuvre de la boucle de rétroaction ainsi que d'une impulsion de courant stable à l'état ON, due à l'ondulation de tension de sortie vue relativement constante par rapport à la courte impulsion de courant. Une inductance de puissance de faible valeur (quelques centaines de nH) et un condensateur de sortie de valeur élevée (quelques µF) peuvent être sélectionnés pour profiter de petits composants passifs tout en assurant une faible ondulation de la tension de sortie. Une méthode standard de modulation de largeur d'impulsion (PWM) utilisant une boucle de contrôle en courant pourra être employée afin d'ajuster la tension de sortie en fonction

de la valeur de courant souhaité. Le convertisseur DC/DC agit ainsi comme une source de tension commandée en courant. Il convient de préciser que le courant à surveiller ici est le courant moyen de la diode laser afin de bénéficier des techniques de détection de courant traditionnelles. Le courant à l'état ON sera contrôlé via le rapport cyclique de modulation du signal de commande. Enfin, l'étage de puissance du convertisseur doit être mis en œuvre à l'aide de dispositifs capables de gérer les contraintes en courant et tension dans toutes les conditions de fonctionnement possibles. Des transistors PMOS et NMOS pourraient être sélectionnés pour simplifier les circuits de commande.

Solution 2: pilote en mode courant en configuration parallèle

La deuxième solution proposée repose sur la topologie du pilote en mode courant utilisant une configuration parallèle. Le schéma du banc de simulation transitoire inclut une source de courant connectée à la diode laser avec un élément de commutation en parallèle. Comme précédemment, le schéma comprend aussi les éléments parasites. Le même transistor NMOS (L=0,5µm, W=50mm) est utilisé comme interrupteur.. Les simulations ont été réalisées dans des conditions typiques pour un courant à l'état ON élevé (3A) et pour diverses valeurs de fréquence (50MHz et 200MHz). Le courant de sortie a été réglé en fonction du courant à l'état ON.

L'introduction d'éléments parasites a un impact significatif sur les transitoires de courant et de tension, que ce soit pendant les phases de montée ou de descente, comme expliqué ci-après :

- Lors de la phase de montée, une résonance sur le courant et la tension est observée à la fois à faible et forte fréquences de modulation, due au circuit RLC équivalent, mais qui semble bien amortie par la body diode du transistor NMOS. Cela traduit un temps de montée du courant relativement rapide. Là encore, il est assez compliqué d'évaluer l'impact de cette résonance sur le courant photo-générateur en raison de l'absence de modèle optique pour les simulations transitoires. De plus, des pics de tension supérieures à 20V sont observés sur la tenson drain-source induisant ainsi de forts pics de courant. Ceci est causé par la coupure rapide du transistor associée aux inductances parasites. Il est possible que ces pics de courant induisent des pics laser, entraînant potentiellement des lésions oculaires.
- Lors de la phase de descente, la tension drain-source diminue rapidement alors que le courant diminue avec un temps de descente relativement lent à faible et forte fréquences. Cette lente descente semble être dominée au premier ordre par les inductances parasites ayant stocké de l'énergie sous 3A lors de la phase de montée. Au second ordre, une résonance sur le courant est remarquée, en particulier à basse fréquence. À haute fréquence, la résonance est directement interrompue par le déclenchement de l'impulsion. Par conséquent, cela peut encore provoquer une distorsion sévère du signal laser à haute fréquence.

Pour cette topologie, le temps de montée du courant de diode est plus rapide que le temps de descente ce qui provoque encore une distorsion sur les impulsions laser. En outre, des pics de tension se produisant au niveau du nœud de commutation lorsque le courant est passant peuvent également induire des pics sur le courant photo-générateur donc sur les impulsions laser. Comme expliqué précédemment, minimiser les inductances parasites s'avère indispensable.

Par la suite, quelques directives sur l'implémentation de la topologie proposée sont données pour répondre aux spécifications. La principale préoccupation concerne la source de courant. Elle doit être capable de fournir un courant de sortie constant, ce qui nécessite une impédance de sortie élevée, en fonction du courant à l'état ON et de la plage de tension d'entrée (2,5V - 4,8V). Le choix sera également motivé par les exigences en terme de puissance tel que fournir un courant de sortie élevé avec un rendement électrique élevé. L'approche pour sélectionner la structure de convertisseur DC/DC adéquate est différente de celle de la solution 1 car les structures conventionnelles agissent comme une source de tension en utilisant un condensateur de sortie avec une faible impédance de sortie.

Une méthode consisterait à utiliser une alimentation connectée à une inductance afin de créer une source de courant bénéficiant de l'impédance de sortie élevée de l'inductance. Des travaux ont été développés par Abramov *et al.* où un redresseur synchrone à demi-pont alimente une inductance pour fournir un courant de sortie constant à une charge. La tension de sortie est ajustée en faisant varier le rapport cyclique appliqué aux interrupteur du redresseur. Cela permet d'ajuster indirectement le courant de sortie en fonction des conditions de charge. Comme aucune capacité de sortie n'est utilisée, le courant de sortie fourni par l'inductance à la charge est alors relativement constant quelle que soit la tension instantanée de sortie. Cette structure, qui peut être vue comme un convertisseur abaisseur standard (ou buck) sans capacité de sortie, semble pertinente pour être employée ici en raison de sa simplicité et du peu de composants passifs requis, à savoir une seule inductance. Néanmoins, ce convertisseur doit être adapté selon les spécifications.

Dans ce contexte, une structure de convertisseur DC/DC abaisseur non isolée est préférable car aucune isolation galvanique n'est requise. Un convertisseur abaisseur à deux interrupteurs fonctionnant en mode de conduction continue et employant une méthode de commutation monophasée est considéré sans capacité de sortie. Le pilote de diode laser comprend alors le convertisseur modifié, la diode laser et l'élément de commutation en parallèle avec ses circuits de commande. Certaines recommandations spécifiques doivent cependant être prises en compte pour choisir les paramètres clés du pilote.

La fréquence de fonctionnement du convertisseur DC/DC pourra être suffisamment faible (<10MHz) par rapport à la fréquence de modulation (50MHz-200MHz). Ceci permettra de bénéficier à la fois de pertes de commutation relativement faibles et d'une certaine flexibilité pour la mise en œuvre de la boucle de rétroaction. Le courant de sortie fourni par le convertisseur est ainsi vu relativement constant pendant la durée de l'impulsion

conduisant à une impulsion de courant stable à l'état ON. Une valeur relativement élevée pour l'inductance de puissance (quelques µH) est nécessaire pour maintenir une faible ondulation du courant. Une méthode standard de modulation de largeur d'impulsion utilisant une boucle de contrôle en courant pourra être employée afin d'ajuster le courant de sortie en fonction de la valeur de courant souhaité. Le convertisseur DC/DC agit ainsi comme une source de courant commandée en courant. Contrairement à la solution 1, le courant à surveiller ici pourrait être le courant moyen traversant l'inductance puisqu'il correspond directement au courant à l'état ON afin de bénéficier des techniques de détection de courant traditionnelles. Enfin, l'étage de puissance du convertisseur doit être mis en œuvre à l'aide de dispositifs capables de gérer les contraintes en courant et tension liées à l'inductance. Des transistors PMOS et NMOS pourraient être sélectionnés pour simplifier les circuits de commande.

Solution 3: pilote en mode courant en configuration source de courant

La troisième solution proposée repose sur la topologie du pilote en mode courant utilisant une configuration source de courant. Le schéma du banc de simulation transitoire inclut une source de tension connectée en série à la diode laser, une source de courant et un élément de commutation (agissant comme une source de courant commutée). Il est supposé que la source de courant force un courant égal au courant à l'état ON mais uniquement lorsque l'interrupteur est allumé. Par ailleurs, la source de tension doit fournir une tension de sortie constante et fixe en tenant compte de la tension directe maximale nécessaire pour polariser la diode laser et d'une marge de tension suffisante pour que le générateur de courant fonctionne correctement.

Comme précédemment, le schéma comprend aussi les éléments parasites. Le même transistor NMOS (L=0,5µm, W=50mm) est utilisé comme interrupteur. La source de courant est implémenté par un transistor cascode fonctionnant en régime de saturation. Un transistor NMOS à oxyde épais de 4,8V est sélectionné et dimensionné arbitrairement tout en respectant une longueur minimale (L=0,5µm) et une largeur relativement importante pour assurer une marge de saturation suffisante au courant d'état ON considéré. Les simulations ont été réalisées dans des conditions typiques pour un courant à l'état ON élevé (3A) et pour diverses valeurs de fréquence (50MHz et 200MHz). La tension de polarisation du transistor cascode a été réglée en fonction du courant à l'état ON, tout en respectant les conditions de saturation (2,4V dans ce cas).

L'introduction d'éléments parasites a un impact significatif sur les transitoires de courant et de tension, que ce soit pendant les phases de montée ou de descente, comme expliqué ci-après :

- Le temps de montée du courant de diode est relativement rapide. Ceci est principalement dû à la tension de sortie élevée (5V ici) qui est distribuée de préférence à travers la diode laser puisque les deux transistors fonctionnent en régime linéaire

pendant cette phase. En effet, une tension plus élevée aux bornes des éléments parasites permet un temps de charge plus rapide. De plus et contrairement à la solution 1, le courant a atteint la valeur souhaitée, à faible et forte fréquences de modulation. Néanmoins, une marge de saturation d'environ 2V aux bornes du transistor cascode est constatée lorsque le courant est établi, ce qui provoque des pertes de conduction importantes.

- Lors de la phase de descente, une résonance sur le courant et la tension est observée à la fois à faible et forte fréquences de modulation, due au circuit RLC équivalent. Cela traduit un temps de descente du courant relativement rapide. Encore une fois, il est assez compliqué d'évaluer l'impact de la résonance sur le signal laser en raison du manque de modèle optique, mais il se pourrait que la diode laser émette des impulsions laser secondaires très courtes. De plus, des pics de tension d'environ 15V sont observés sur la tension drain-source induisant de forts pics de courant négatifs. Ceci est causé par la coupure rapide du transistor associée aux inductances parasites. Par contre, même si ces pics de tension peuvent endommager les dispositifs, il est intéressant de voir que le transistor de commutation semble protégé du fait de la structure cascode.

Contrairement aux deux solutions précédentes, cette topologie présente de très bonnes performances transitoires même avec l'introduction d'éléments parasites. Des temps de montée et de descente rapides sont obtenus sur le courant de la diode. Néanmoins, des pics de tension élevés se produisent toujours au niveau du nœud de commutation lorsque le courant est passant, en particulier à haute fréquence. Minimiser les inductances parasites comme indiqué précédemment pourrait réduire ces pics ainsi que la résonance potentielle, tout en améliorant les performances transitoires. Enfin, un inconvénient majeur de cette topologie concerne les importantes pertes de conduction à travers le transistor cascode, en raison de sa marge de saturation relativement élevée

Par la suite, quelques directives sur l'implémentation de la topologie proposée sont données pour répondre aux spécifications. La principale préoccupation concerne la source de tension. Elle doit être capable de fournir une tension de sortie constante en tenant compte de la tension maximale pour polariser la diode laser et d'une marge de saturation suffisante pour la source de courant, tout en respectant la plage de tension d'entrée (2,5V - 4,8V). En supposant une tension de sortie supérieure à 5V, il semble cohérent d'utiliser un convertisseur DC/DC fonctionnant en mode élévateur avec n'importe quel rapport de conversion de tension tout en gardant la même polarité. Comme aucune isolation galvanique n'est requise, une structure de convertisseur DC/DC non isolée est préférable. Le choix sera également motivé par les exigences en terme de puissance tel que fournir un courant de sortie élevé avec un rendement électrique élevé.

Les convertisseurs à inductance commutée semblent être les plus appropriés à utiliser dans ce contexte. Un convertisseur boost standard composé d'une seule inductance, d'un

seul condensateur et de deux interrupteurs est considéré ici. Il bénéficie de moins de composants passifs hors puce que d'autres topologies, réduisant ainsi l'empreinte du PCB. La tension de sortie est ajustée en faisant varier le rapport cyclique appliqué aux interrupteurs. La tension de sortie est ajustée en faisant varier le rapport cyclique appliqué aux interrupteurs. Cependant, il peut être remarqué qu'une tension de sortie trop proche de la tension d'entrée conduirait à un rapport cyclique très faible, ce qui pourrait avoir un impact sur les performances des stratégies de contrôle telles que les méthodes PWM, où un rapport cyclique supérieur à 10% est généralement recommandé. Par conséquent, une tension de sortie supérieure à 5,3V serait nécessaire dans ce contexte pour bénéficier de bonnes performances transitoires sans augmenter la complexité.

Le pilote de diode laser comprend alors le convertisseur DC/DC, la diode laser, le transistor cascode agissant comme source de courant etl'élément de commutation en série avec ses circuits de commande. Certaines recommandations spécifiques doivent cependant être prises en compte pour choisir les paramètres clés du pilote.

Les mêmes recommandations que pour la solution 1 fonctionnant en mode boost peuvent être considérées ici. La fréquence de fonctionnement du convertisseur DC/DC pourra être suffisamment faible (<10MHz) par rapport à la fréquence de modulation (50MHz-200MHz). Ceci permettra de bénéficier à la fois d'une certaine flexibilité pour la mise en œuvre de la boucle de rétroaction ainsi que d'une impulsion de courant stable à l'état ON, due à l'ondulation de tension de sortie vue relativement constante par rapport à la courte impulsion de courant. Une inductance de puissance de faible valeur (quelques centaines de nH) et un condensateur de sortie de valeur élevée (quelques µF) peuvent être sélectionnés pour profiter de petits composants passifs tout en assurant une faible ondulation de la tension de sortie. Une méthode standard de modulation de largeur d'impulsion (PWM) utilisant une boucle de contrôle en tension pourra être employée afin d'ajuster la tension de sortie en fonction de la tension d'entrée. Même si la tension de sortie est supposée être fixe, l'utilisation d'une référence de niveau de tension pourrait apporter une certaine polyvalence à la structure pour ajuster la tension de sortie et les performances, en fonction des besoins. Le convertisseur DC/DC agit ainsi comme une source de tension commandée en tension. Enfin, l'étage de puissance du convertisseur doit être mis en œuvre à l'aide de dispositifs capables de gérer le courant d'inductance maximal ainsi que la tension de sortie maximale. Des transistors PMOS et NMOS pourraient être sélectionnés pour simplifier les circuits de commande.

Enfin, la source de courant pourra être mise en œuvre à l'aide d'un transistor cascode comme décrit précédemment. Un circuit de polarisation pourrait être utilisé pour ajuster la tension de polarisation en fonction de la valeur de courant souhaitée, établie par une référence de niveau de courant. Cependant, la régulation du courant à l'état ON n'est pas faisable de façon simple. Les techniques classiques impliquent un fonctionnement en boucle fermée et nécessitent des amplificateurs d'erreur à large bande passante. Dans ce contexte où l'on considère de hautes fréquences, il serait assez difficile de concevoir un tel

amplificateur d'erreur sans impliquer une solution complexe, volumineuse et consommatrice d'énergie. Par conséquent, une technique en boucle ouverte sera préférée telle qu'une structure de miroir de courant. Même s'il s'agit d'une technique bien connue pour réaliser une source de courant dans le domaine de la conception analogique, elle nécessitera ici une conception très soignée puisque l'élément de commutation fonctionnant à haute fréquence est inclus dans la structure.

Analyse comparative

Cette section présente une analyse comparative des trois solutions proposées afin de mettre en évidence leurs avantages et les inconvénients.

Complexité de conception

La solution 2 se distingue des autres solutions en termes de complexité de conception car elle présente une conception relativement simple qui repose sur un convertisseur abaisseur très bien détaillé dans la littérature. De plus, en raison de son principe de fonctionnement, le courant à l'état ON est régulé en utilisant une technique de détection de courant traditionnelle assurant une précision relativement élevée contrairement à la solution 1 ou la solution 3. Étant donné que trois modes de fonctionnement sont considérés pour le convertisseur DC/DC de la solution 1, il nécessite un contrôleur PWM plus complexe que celui des autres solutions mais qui reste tout de même bien détaillé dans la littérature. La solution 3 nécessiterait une conception très pointue due à la structure de miroir de courant cascode.

Surface de silicium et taille de boîtier

La surface de silicium occupée par chaque solution peut être estimée en fonction des dimensions des transistors de puissance, considérés comme prédominants devant les transistors impliqués dans les fonctions analogiques et numériques. Afin d'obtenir une comparaison cohérente entre les solutions et parce que chaque étage de puissance a à peu près les mêmes spécifications, la même résistance de canal est considérée pour chaque transistor de puissance. L'élément de commutation, utilisé pour les simulations et implémenté à l'aide d'un transistor NMOS 4,8V à oxyde épais, est pris comme référence. En raison de la différence de mobilité entre les électrons et les trous, un transistor PMOS est généralement considéré comme trois fois plus large qu'un transistor NMOS, à résistance de canal constante. De même avec un transistor NMOS haute tension. Pour simplifier la comparaison, on a retenu un facteur 3 pour un transistor NMOS haute tension et un facteur 9 pour un transistor PMOS haute tension. De cette manière, il est possible de normaliser les estimations en fonction de la surface de silicium occupée par l'élément de commutation, notée A_{SW}.

La solution 2 présente la plus petite surface de silicium car elle utilise trois transistors de puissance équivalents à $5A_{SW}$, contrairement à la solution 1 qui occupe une grande

surface de silicium avec cinq transistors de puissance équivalents à $17A_{SW}$. La solution 3 occupe également une surface de silicium relativement grande avec trois transistors de puissance et un transistor cascode (représentant ~$0{,}3A_{SW}$) équivalent à $13{,}3A_{SW}$.

En pratique, la taille de la puce est également limitée par son boîtier. Ici, un boîtier WLCSP est considéré où sa taille est limitée par les billes de soudure donc le nombre d'entrée/sortie (E/S). En raison des effets thermiques, plusieurs billes peuvent être utilisées pour une seule E/S, en particulier dans le domaine de puissance où des courants élevés sont considérés. Les éléments de commutation et les étages de puissance de chaque solution ayant à peu près les mêmes spécifications en termes de courant maximum pour chaque branche, il est possible de normaliser les estimations en fonction du nombre d'E/S. Dans ce cas, la solution 2 nécessite au moins quatre E/S par rapport à la solution 1 et 3 où au moins six et cinq E/S sont respectivement nécessaires.

Empreinte PCB

L'empreinte PCB de chaque solution peut être estimée en fonction du nombre et de la taille des composants. Néanmoins, il semble assez compliqué d'estimer la taille globale des composants hors puce, tels que les condensateurs ou les inductances de puissance, car de nombreux boîtiers existent pour des composants avec les mêmes valeurs de capacité ou d'inductance. Concernant le nombre de composants, la solution 2 nécessite une seule inductance de puissance. Les solutions 1 et 3 nécessitent en plus un condensateur de sortie où, en pratique, quelques petits condensateurs de découplage sont inclus pour fournir du courant en réponse aux transitoires rapides. Par conséquent, la solution 2 nécessite moins d'empreinte que les autres solutions.

Puissance dissipée et rendement électrique

La puissance dissipée globale ainsi que le rendement électrique peuvent être estimés pour chaque pilote à l'aide de calculs manuels dans le but de se faire une idée des principaux contributeurs. La diode laser est ici considérée comme une charge donc les pertes principales concernent le pilote. Les pertes totales peuvent être évaluées en considérant les pertes par conduction et les pertes par commutation. Le rendement électrique correspond au ratio entre puissance de sortie et pertes totales. Tous les pilotes sont évalués dans les mêmes conditions de fonctionnement pour une tension d'entrée de 2,5V à 4,8V. Un courant à l'état ON de 3A est ciblé avec une fréquence de 200MHz à un rapport cyclique de modulation de 50%, conduisant à une puissance de sortie moyenne d'environ 4,5W.

Le pilote 3 a le pire rendement avec une valeur inférieure à 50% sur toute la plage de tension d'entrée. Elle est causée par les importantes pertes de conduction à travers le transistor cascode représentant plus de 70% des pertes totales. Le pilote 1 est plus efficace que le pilote 2 à des tensions d'entrée extrêmement faibles ou relativement élevées (inférieures à 2,8V ou supérieures à 3,4V) alors que c'est le contraire à de faibles tensions

d'entrée (entre 2,8V et 3,3V) où son efficacité chute à environ 70% . Cela est dû aux différents modes de fonctionnement utilisés par le convertisseur D /DC provoquant plus de pertes de conduction et de commutation en mode buck-boost lorsque les quatre transistors de l'étage de puissance sont activés. Le courant de l'inductance est également élevé (3A dans ce cas). Ces pertes pourraient être réduites en utilisant une méthode de commutation plus efficace pour le mode buck-boost mais au prix d'une plus grande complexité de conception. Il est aussi remarqué que les pertes dues aux composants passifs sont souvent significatives, en particulier pour les pilotes 2 et 3. Il est donc crucial de sélectionner des composants à faibles résistances parasites.

Performances transitoires

Comme expliqué dans les sections précédentes, la solution 3 présente de très bonnes performances transitoires avec des temps de montée et de descente rapides sur le courant de diode contrairement aux solutions 1 et 2 où le temps de montée ou de descente est fortement impacté par des éléments parasites.

Erreur systématique sur la mesure de profondeur

Il peut être intéressant d'évaluer l'impact de la forme d'onde du signal de modulation sur l'ensemble du système au niveau applicatif, en mesurant l'erreur systématique sur la mesure de profondeur. Le but est de retarder artificiellement une forme d'onde transitoire optique au moyen de simulations pour émuler le temps de vol des photons, ou déphasage dans ce cas, entre un signal laser émis et reçu après réflexion sur un objet de la scène. Ensuite, les calculs de déphasage sont effectués sur la forme d'onde optique retardée en utilisant un modèle de capteur "Temps de Vol". Le résultat est comparé à la valeur initiale afin d'estimer l'erreur de déphasage. Toutes les solutions sont évaluées dans les mêmes conditions à l'aide des bancs de simulation transitoire décrits précédemment, en utilisant le modèle optique de diode laser. Même s'il est incomplet, cela peut toujours donner une première estimation des erreurs systématiques pour comparer chaque solution.

Il est remarqué que l'amplitude d'erreur pour un signal laser pulsé idéal est symétrique par rapport à un rapport cyclique de 50% et est minimisée pour 33% et 66%, à la fois à 50MHz et 200MHz. En considérant maintenant les signaux des solutions à 50MHz, les courbes d'amplitude d'erreur sont similaires à celle du signal laser pulsé idéal avec un léger écart d'environ 60% pour la solution 1 et d'environ 40% pour la solution 2. Cela signifie que la distorsion introduite par les éléments parasites sur le signal laser de chaque solution est relativement insignifiant aux basses fréquences. Au contraire, les résultats à 200MHz sont assez hétérogènes pour les solutions 1 et 2 en particulier à des valeurs de rapport cyclique élevées tandis que les résultats pour la solution 3 sont relativement similaires à ceux du signal laser pulsé idéal.

Toutes les solutions semblent montrer des performances relativement similaires en termes de précision liée à l'erreur de profondeur systématique aux basses fréquences. Aux fréquences élevées, la solution 3 présente de meilleures performances que les autres solutions lorsque l'on considère un rapport cyclique de 50%. Dans ce cas, l'amplitude de l'erreur pour la solution 2 est relativement grande. Pour un rapport cyclique inférieur à 50%, l'amplitude d'erreur pour la solution 1 semble être relativement constante alors qu'elle augmente fortement pour les solutions 2 et 3 à des valeurs de rapport cyclique extrêmement faibles.

Discussion et conclusion

On voit que la solution 2 se démarque des autres solutions présentant une conception simple et compacte avec un circuit intégré potentiellement petit et comportant peu de composants hors puce. Cependant, de mauvaises performances transitoires sont constatées. Un autre point important est qu'un rendement relativement élevé est signalé sur toute la plage de tension d'entrée avec une valeur moyenne d'environ 77%, ce qui rend cette solution potentiellement bien adaptée à la conception du pilote de diode laser.

Bien que de très bonnes performances transitoires aient été notées pour la solution 3 par rapport aux solutions 1 et 2, un très faible rendement inférieur à 50% a été estimé pour cette solution du fait de l'utilisation d'un transistor cascode fonctionnant en régime de saturation. En conséquence, il n'est pas adapté au pilote de diode laser par rapport aux objectifs visés.

La discussion est plus compliquée concernant la solution 1. Alors qu'un gros circuit intégré occupant une grande empreinte PCB semble nécessaire du fait de l'utilisation d'un convertisseur buck-boost, de bonnes performances en termes de rendement et de pertes de puissance ont été estimées mais pas sur toute l'entrée plage de tension. L'efficacité étant une exigence majeure dans ce contexte, cette solution semble également être un bon candidat pour le pilote de diode laser. De plus, il pourrait être envisagé d'étudier un autre type d'architecture buck-boost afin d'améliorer l'efficacité en mode buck-boost même si cela se fait au détriment de la complexité de conception.

Cette étude de conception préliminaire a montré certaines limites pour le choix d'une solution unique, notamment en raison de l'indisponibilité d'un modèle optique précis pour la diode laser. Effectivement, il est assez compliqué de conclure sur le comportement optique des solutions 1 et 2, notamment au niveau de l'erreur systématique sur la mesure de profondeur. Il est donc proposé de mettre en œuvre les deux solutions.

Chapitre 3 : Conception du Prototype Intégré de Pilote de Diode Laser

Ce chapitre décrit la conception et la mise en œuvre des prototypes de pilote de diode laser en technologie analogique hcmos9a, reposant sur les architectures de pilote en mode tension en configuration série et en mode courant en configuration parallèle. La nouveauté du travail de thèse concerne l'intégration du driver sur une seule puce, y compris la solution de gestion d'alimentation mais à l'exception de la diode laser et de certains composants passifs.

Considérations de conception pour le circuit intégré

Les architectures de pilote en mode tension et en mode courant proposées reposent sur des blocs similaires. D'après les recommandations énoncées dans le Chapitre 2, les deux pilotes comprennent:

- Un convertisseur DC/DC pour polariser la diode laser. Il comprend un étage de puissance, un filtre de sortie et un circuit PWM standard utilisant une boucle de contrôle de courant afin d'ajuster la tension ou le courant de sortie en fonction du courant souhaité et fixé par une référence de niveau de courant. Le filtre de sortie est constitué d'un filtre LC ou d'une seule inductance de puissance pour les pilotes en mode tension et en mode courant respectivement.
- Un bloc de commutation haute fréquence (bloc HF) pour commuter le courant à travers la diode laser. Il comprend un élément de commutation commandé par un signal de modulation différentielle externe via un circuit de commande approprié. De plus, une source de courant pourra être utilisée pour le pilote en mode tension uniquement, afin de pré-polariser la diode laser pour réduire le délai entre l'impulsion électrique et optique.

Étant donné que certains choix de conception pour les convertisseurs DC/DC sont classiques, il a été décidé de réutiliser un circuit intégré issu de développements précédents afin de gagner du temps et des ressources de conception. Cette puce est bien adaptée pour implémenter à la fois les pilotes en mode tension et en mode courant car elle intègre deux convertisseurs DC/DC buck-boost non inverseurs assistés par pompe de charge. L'un des convertisseurs pourrait être utilisé tel quel pour implémenter le convertisseur DC/DC du pilote en mode tension tandis que l'autre pourrait être utilisé en mode buck uniquement et fonctionner sans condensateur de sortie afin de mettre en œuvre le convertisseur DC/DC du pilote en mode courant. De cette manière, une seule puce peut être réalisée. Enfin, le même bloc HF pourra être utilisé pour les deux pilotes car il a les mêmes spécifications, afin d'économiser de la surface de silicium pour le prototype. Cependant, un soin particulier doit être apporté aux niveaux du circuit et du système pour s'assurer qu'un seul pilote fonctionne à la fois.

Le choix d'un transistor approprié pour l'élément de commutation, ainsi que son dimensionnement par rapport aux spécifications, sont des étapes de conception très importantes. Une étude comparative des transistors pourra être réalisée en fonction de plusieurs indicateurs tels que la puissance totale dissipée, la surface d'oxyde de grille, la complexité de conception et le coût des étapes de fabrication. Une autre exigence importante concerne la tenue en tension qui est principalement impactée par les pics de tension élevés. L'utilisation de circuits de protection appropriés tels qu'une diode de serrage s'avérera nécessaire pour éviter tout dommage causé à la diode laser et aux dispositifs à l'intérieur de la puce. Malheureusement, les modèles de diodes fournis par le kit de conception sont incomplets. Pour cette raison et parce qu'un processus de caractérisation de dispositif aurait été incompatible avec le planning de conception lié au contexte industriel, il a été décidé de réaliser plusieurs prototypes de circuit intégré mettant en œuvre les différentes diodes pour tester en conditions réelles.

Détails de conception

La conception des pilotes en mode tension et courant sur une seule puce étant assez ambitieuse vis-à-vis des courts délais liés au contexte industriel, le travail a été réparti selon différents membres au sein de l'équipe. La contribution majeure de la thèse au niveau de la conception concerne l'élément de commutation, ses circuits de pilotage et de protection.

Concernant le pilote en mode tension, le convertisseur DC/DC buck-boost non inverseur assisté par pompe de charge inclut un contrôleur PWM analogique standard fonctionnant à une fréquence de 4MHz avec une boucle de contrôle en courant. Une résistance dite de shunt est insérée en série avec la diode laser, permettant de mesurer le courant moyen. Il est utilisé tel quel pour implémenter la source de tension contrôlée en courant. Une inductance de puissance de 470nH ainsi qu'un condensateur de sortie de 4,7µF ont déjà été sélectionnés.

L'autre convertisseur DC/DC buck-boost est utilisé en mode buck uniquement sans condensateur de sortie afin de mettre en œuvre la source de courant contrôlée en courant requise par l'architecture de pilote en mode courant. Il comprend un contrôleur PWM et une boucle de contrôle en courant. La résistance de shunt est ici insérée en série avec l'inductance de puissance, après l'étage de puissance. En revanche, une valeur d'inductance minimale de 1µH est requise pour maintenir l'ondulation de courant sous 10%. L'inductance de puissance doit être sélectionnée avec un courant nominal supérieur à 3A et une faible résistance DC. L'étage à condensateur commuté implémentant la pompe de charge n'est pas nécessaire.

Une exigence importante pour la sélection du transistor NMOS comme élément de commutation concerne la tenue en tension au niveau du drain. Cela dépend des contraintes de tension imposées à la fois par les pilotes en mode tension et en mode courant ainsi que

de la mise en œuvre des circuits de protection.

Une solution pour bloquer les pics de tension pendant les transitoires rapides consiste à ajouter une diode de serrage entre le nœud de commutation et une tension spécifique. Son objectif principal est d'évacuer l'énergie résiduelle des inductances parasites tout en empêchant le nœud de commutation de dépasser les tensions maximales supportées par l'élément de commutation et la diode laser. La tension spécifique de bloquage dépend cependant du mode de pilotage : la tension d'anode est préférée pour le pilote en mode tension alors que la tension d'entrée sera directement utilisée pour le pilote en mode courant. Les contraintes en tension les plus restrictives sont alors retenues pour choisir l'élément de commutation, à savoir supporter une tension supérieure à 7,2V. Bien que les modèles de simulation de diodes soient incomplets, leur dimensionnement a été directement réalisé au niveau du dessin des masques à l'aide d'exemples issus de développements précédents. Les diodes doivent être suffisamment larges pour évacuer l'énergie résiduelle des inductances parasites lors des transitoires, ce qui correspond à peu près à un pic de courant 3A sur 1ns.

Il est ensuite proposé de comparer les différents transistors NMOS selon divers indicateurs, comme cités plus-haut. Pour une comparaison juste, les simulations pour évaluer la puissance dissipée totale, sont effectuées dans les mêmes conditions typiques pour tous les transistors. Le même banc de simulation que décrit dans le Chapitre 2 a été utilisé ici. L'inductance parasite n'a par contre pas été incluse et la tension de sortie a été adaptée pour chaque transistor afin d'atteindre le même courant à l'état ON. La largeur de grille des transistors a été balayée de 10mm à 150mm par pas de 5mm pour trouver l'optimum des pertes totales.

Le transistor à simple oxyde (GO1) est le meilleur selon la figure de mérite qui rassemble tous les indicateurs, pour les cas d'utilisation à 50MHz et 200MHz. Cela est dû à sa faible tension de grille qui réduit considérablement les pertes par commutation. En revanche, il nécessite un régulateur de tension fournissant une tension d'alimentation de 1,2V à partir de la tension d'entrée disponible (2,5V - 4,8V), augmentant ainsi la complexité de conception et la taille du système. Le deuxième meilleur choix revient au transistor double oxyde (GO2). Considérant maintenant la contrainte en tension ($>$ 7,2V), il est constaté que les transistors simple et double oxydes (1,2V et 4,8V) ne conviennent pas et ne peuvent être utilisés seuls. Par conséquent, utiliser une configuration cascode semble être le meilleur compromis dans ce contexte.

Étant donné que le courant à l'état ON (jusqu'à 3A) et la fréquence de modulation (50MHz - 200MHz) sont flexibles, la grille du transistor de commutation est rendue programmable et est divisée en 16 parties égales afin d'optimiser les pertes par commutation et par conduction. Des résultats de simulation donnent une grille configurable de 5,4mm à 86,4m par pas de 5,4mm. Le transistor cascode est du même type que le transistor de commutation, à savoir double oxyde 4,8V mais dimensionné avec une grille fixe de 24mm respectant un compromis entre résistance de canal et capacité de sortie.

Comme les modèles de diodes de serrage fournis par le kit de conception sont incomplets, il a été décidé deux versions de prototype, toutes deux comprenant la structure cascode et la diode de serrage, l'une mettant en œuvre une diode à jonction P-N et l'autre une diode Schottky. Par ailleurs, trois autres versions sont proposées, mettant en œuvre un dispositif haute tension comme transistor cascode en cas de pannes techniques de la diode de serrage. Dans ce cas, un transistor HVDrift 18V est retenu, avec une largeur de grille de 51mm. Il pourrait également être intéressant de tester sans diode de serrage. Étant donné que chaque version comprend à la fois les pilotes en mode tension et en mode courant, cela conduira à tester 10 prototypes de circuit intégré.

Le bloc HF comprenant le transistor de commutation nécessite un circuit de commande approprié pour commuter à une fréquence de modulation allant jusqu'à 200MHz. La technique LVDS, capable de transmettre des données à des vitesses élevées avec une faible dissipation de puissance, est bien adaptée dans ce contexte. Un émetteur fournit un signal différentiel avec une tension de mode commun à travers une ligne de transmission tandis qu'un récepteur, agissant en tant que comparateur, récupère le signal de modulation à partir du signal différentiel. Il a été choisi de fournir un signal de modulation différentielle externe comme signal de commande au pilote via des ports d'E/S. Un récepteur LVDS est donc indispensable pour convertir ce signal différentiel en un signal de modulation asymétrique qui est ensuite délivré au transistor de commutation via un pilote de grille adéquat.

Ce pilote de grille est utilisé pour piloter la large capacité d'entrée du transistor de commutation à partir du signal de modulation asymétrique fourni par le circuit LVDS. Habituellement, une chaîne d'inverseurs est utilisée pour piloter ce type de charge capacitive, où chaque étage est plus grand que le précédent d'un facteur spécifique (appelé facteur de réduction). Étant donné que des courants élevés sont tirés de l'alimentation pour charger la capacité d'entrée, une ondulation peut apparaître sur la ligne d'alimentation en raison d'inductances parasites et avoir un impact sur le signal de grille de l'élément de commutation. Les valeurs parasites dépendent grandement de la conception du PCB. Pour cette raison, il a été choisi de concevoir un pilote de grille spécifique avec une capacité de commande programmable, en ajustant les temps de montée et de descente du signal de grille. Ce pilote de grille est ainsi divisé en 4 parties pour régler la résistance de sortie équivalente du dernier étage. Chaque partie est constituée d'un inverseur à trois états afin de bénéficier d'une sortie à haute impédance, évitant ainsi les courts-circuits au niveau de la grille du transistor de commutation.

Pour des raisons pratiques par rapport au transistor de commutation, l'ensemble du pilote de grille est divisé en 16 parties égales. Ainsi, une partie du pilote de grille est dimensionnée pour piloter une partie du transistor de commutation. Des simulations transitoires idéales (hors éléments parasites) ont été réalisées pour le dimensionnement en répondant à des contraintes transitoires, de surface de silicium et de consommation d'énergie. Un nombre raisonnable d'étages (5 ici) a été retenu ainsi qu'un facteur de réduction raisonnable

(~4).

Le bloc HF comprend également une source de courant pour pré-polariser la diode laser. En effet, lors de la pulsation du courant à travers une diode laser, un retard inhérent se produit entre les impulsions électriques et optiques. Ce phénomène est dû au temps nécessaire à la densité de porteurs pour atteindre sa valeur de seuil d'émission laser. Dans ce contexte, la source de courant repose sur une technique de miroir de courant. La cellule est connectée au drain du transistor de commutation afin de bénéficier de la protection du transistor cascode. Trois copies de courant ont été nécessaires pour fournir un courant correct et réduire les problèmes d'adaptation entre les tensions drain-source et le paramètre de modulation de la longueur de canal λ. De plus, il a été décidé de rendre le courant programmable pour s'adapter aux caractéristiques du VCSEL et pour conserver une certaine flexibilité de conception. Pour faciliter l'implémentation physique, la source de courant est divisée en 16 parties comme cela a été fait pour le transistor de commutation. Le courant est configurable de 0 à 550mA par pas de 35mA. Il est précisé que la source de courant de pré-polarisation est implémentée pour les deux toplogies de pilote, mais ne sera utilisée que pour le pilote en mode tension. Il peut être désactivé pour le pilote en mode courant.

Le bloc HF comprend aussi des dispositifs de protection pour protéger les E/S de la puce contre les décharges électrostatiques (ESD). Des diodes polarisées en inverse sont utilisés pour absorber l'éventuelle décharge externe, soit à la tension d'alimentation soit à la masse, limitant ainsi la tension appliquée aux port d'E/S. En outre, d'autres dispositifs tels que des circuits de serrage de rail d'alimentation sont utilisés pour bloquer les surtensions ESD sur les lignes électriques spécifiquement. Ils sont généralement désactivés lorsque le circuit est en fonctionnement normal pour éviter un blocage involontaire dû au comportement de commutation des convertisseurs DC/DC.

Habituellement, les circuits de protection sont situés à la périphérie de la puce à proximité de chaque E/S à protéger, adoptant ainsi une forme d'anneau. Ici, un WLCSP Fan-In est considéré pour le prototype, ce qui implique que les pistes de redistribution doivent être acheminées vers l'intérieur. Cela conduit à placer des circuits de protection dans la surface effective de la puce et non autour. Pour cette raison, certains circuits de protection regroupés en "cluster" se positionnent soigneusement à proximité d'E/S partageant les mêmes contraintes de tension. Chaque E/S dans un cluster partage un rail flottant comme tension d'alimentation de sorte que la tension la plus élevée entre chaque E/S soit préférée. Cette fonction est couramment adoptée sur les convertisseurs DC/DC lorsqu'ils permettent d'élever la tension.

Pour finir, un signal externe de modulation basse fréquence sera fourni afin de contrôler l'enveloppe des impulsions de courant, générant ainsi des trains d'impulsions. Une interface I^2C avec une banque de registres, réutilisée des développements précédents, sera embarquée afin de configurer le prototype. Un circuit de référence de tension à bande interdite est

également intégré pour fournir des références de tension et de courant pour les circuits de boucle de contrôle en courant.

Détails d'implémentation physique

Comme expliqué précédemment, aucune contribution directe n'a été apportée sur l'implémentation physique du point de vue de la thèse. Néanmoins, les sections suivantes passent en revue le travail réalisé par l'équipe de conception.

Un défi majeur concerne le bon fonctionnement de l'ensemble du circuit mélangeant à la fois des blocs de construction nouveaux et anciens. En effet, une ancienne puce comprenant deux convertisseurs DC/DC a été réutilisée et de nouveaux blocs de construction doivent donc être intégrés tout en minimisant leur impact sur le comportement des convertisseurs. La commutation à haute fréquence requise du courant jusqu'à 3A en utilisant des transistors génère des tensions et des courants parasites qui peuvent perturber les cellules adjacentes. Un placement approprié des nouveaux blocs dans la puce est alors nécessaire pour économiser de la surface de silicium et faciliter le routage.

Le processus comprend un empilement métallique de plusieurs niveaux pour connecter les éléments via des lignes métalliques et des VIAs. Un problème majeur réside dans les résistances et capacités parasites ajoutées par chaque interconnexion, qui peuvent dégrader les performances en augmentant les retards de signal et les pertes de puissance. Il est proposé d'augmenter la surface de contact (drain, source, grille) des transistors et la largeur des lignes métalliques en utilisant plusieurs VIA en parallèle afin de diminuer la résistance parasite. Un placement spécifique de VIA peut être utilisé pour réduire les capacités parasites. Un autre problème concerne l'électromigration des métaux. Elle est due à la migration des atomes métalliques lorsque les conducteurs transportent trop de courant laissant ainsi un vide et augmentant localement la résistance. Cela peut même provoquer une panne. L'électromigration du métal peut être atténuée en limitant la densité de courant maximale. Des niveaux plus élevés de métaux avec un grand nombre de VIA en parallèle sont également utilisés pour le routage de puissance.

La principale préoccupation au niveau des cellules est liée au couplage du substrat, dû à l'injection de charge depuis ou vers les cellules adjacentes pendant les transitoires rapides. Un bon isolement de chaque cellule est donc indispensable. L'une des principales fonctionnalités de la technologie utilisée est de proposer un triple caisson. Les dispositifs NMOS peuvent ainsi être isolés du substrat de la puce en utilisant un caisson P, agissant comme un volume, à l'intérieur d'un profond caisson N et entouré par un anneau de garde. Habituellement, le substrat de la puce est connecté à la masse, le caisson P à la source du dispositif NMOS et le caisson N à une haute tension pour s'assurer que les diodes de jonction soient polarisées en inverse. En plus, un anneau de garde constitué d'une zone de diffusion P+ peut être implanté autour du dispositif pour une polarisation efficace du

substrat de la puce, afin d'évacuer les porteurs par un chemin à faible impédance. Des isolations de tranchées peu profondes sont utilisées pour isoler les zones actives telles que les contacts de drain ou de source des anneaux de garde par exemple.

Les dispositifs PMOS bénéficient intrinsèquement d'une isolation adéquate puisque leur masse est généralement connectée à une haute tension polarisant les diodes de jonction en inverse. Cependant, l'isolation peut être améliorée en plaçant un profond caisson N sous la masse, afin de diminuer le gain du transistor bipolaire PNP parasite vertical formé par le drain, la masse et le substrat. Un anneau de garde constitué d'une région de diffusion P+ peut également être implanté autour du dispositif pour une polarisation efficace du substrat de la puce afin d'évacuer les porteurs par un chemin à faible impédance.

Même si elles consomment de la surface, ces techniques d'isolation peuvent être employées et adaptées à chaque bloc pour garantir une évacuation correcte des porteurs afin de minimiser le bruit. Un soin particulier doit être apporté à l'élément de commutation, au dispositif cascode et au pilote de grille où les transitoires de courant fort sont considérés. Une autre méthode pour minimiser l'impact du bruit entre chaque bloc consiste à utiliser un chemin de puissance dédié avec une broche dédiée pour chacun des domaines analogique, numérique et de puissance. Différents chemins suivant une stratégie de routage en étoile peuvent être utilisés pour fournir des blocs sensibles partageant le même domaine. De plus, du fait des effets thermiques, plusieurs billes de soudure peuvent être utilisées pour une seule E/S surtout si des courants élevés sont véhiculés.

Comme expliqué précédemment, il a été décidé de diviser l'élément de commutation en 16 parties égales. Pour des raisons pratiques, d'autres cellules transportant des courants élevés à l'intérieur du bloc HF, telles que le transistor cascode, le pilote de grille ou la source de courant de pré-polarisation, sont également divisées en 16 parties égales et intégrées dans chaque partie de l'élément de commutation. Un défi majeur ici est d'agencer correctement toutes les parties pour optimiser le flux de courant, qui doit être aussi symétrique que possible circulant du transistor cascode vers l'élément de commutation et la source de courant. La première partie doit être activée à partir du milieu de la structure, puis alternativement à gauche et à droite, afin d'avoir approximativement la même résistance métallique vue de chaque partie de l'élément de commutation et de la source de courant.

L'élément de commutation est implémenté en utilisant une structure inter-digitée. Les surfaces de source et drain ainsi que la résistance de grille peuvent être réduites avec cette approche mais au prix d'une plus grande capacité parasite des source et drain. De plus, le dispositif est divisé en plusieurs cellules unitaires connectées en parallèle évitant ainsi de longues géométries dans le schéma. Le nombre de doigts et la largeur de grille d'une cellule unitaire sont choisis de manière à ce que le bulk soit polarisé avec un chemin résistif faible pour empêcher un effet "snapback" dû au transistor bipolaire NPN parasite horizontal formé par le drain, le bulk et la source, qui peut conduire à des défaillances.

Le dispositif HVDrift 18V utilisé pour implémenter le transistor cascode dans l'un des prototypes, a une structure spécifique seule où seule une double grille peut être

obtenue, générant ainsi une cellule unitaire Bulk-Source-Drain-Source-Bulk (BSDSB) qui est symétrique centrée sur le drain. Elle peut ensuite être multipliée afin d'obtenir une structure de type inter-digitées. Le dispositif GO2 pour implémenter le transistor cascode dans un autre prototype, a une structure inter-digitée comme pour le transistor de commutation.

Il a été vu précédemment que des courants élevés peuvent être tirés depuis l'alimentation à travers le pilote de grille afin de charger la capacité d'entrée de l'élément de commutation. Pour cette raison, un réseau de distribution d'énergie dédié utilisant un chemin d'alimentation et un plan de masse à faible impédance avec des condensateurs de découplage appropriés est nécessaire afin d'alimenter correctement les différents blocs. Une méthodologie particulière pour concevoir un tel réseau repose sur l'optimisation de son impédance, en sélectionnant des condensateurs adaptés, afin que sa valeur ne dépasse pas une impédance cible spécifique selon plusieurs bandes passantes. Divers condensateurs tels que des condensateurs hors puce et sur puce peuvent être utilisés. Néanmoins, la valeur de capacité sur puce qui peut être obtenue avec une technologie intégrée est souvent limitée par la surface de silicium. Des condensateurs céramiques haute fréquence de différentes valeurs (de 1nF à 10µF) sont sélectionnés pour garder une impédance plate de 1MHz à plusieurs centaines de MHz. Ils sont connectés en parallèle pour réduire la résistance et l'inductance série équivalente globale.

L'impédance du réseau a été estimée avec des simulations dans le domaine fréquentiel. Malheureusement, bien que la méthode proposée tende à réduire les contraintes pour les basses fréquences, l'impédance cible est encore très restrictive pour les hautes fréquences. Ainsi, la sélection des condensateurs de découplage est réalisée de manière à ce que l'impédance du réseau soit aussi faible que possible tout en répondant aux contraintes typiques de coût et de surface de PCB de l'électronique grand public. Six condensateurs hors-puce différents sont retenues (100µF, 10µF, 22nF, 10nF, 4.7nF et 2.2nF) ainsi qu'une capacité intégrée totale implémentée à l'aide de capacités MOS et MIM (2.4nF au-delà de 2.5V).

Finalement, la puce complète, y compris les pilotes en mode tension et en mode courant, occupe une surface de silicium d'environ 20mm^2. En comptant la somme des surfaces de silicium pour chaque bloc requis par chaque pilote, on obtient une surface de silicium de 7mm^2 pour le pilote en mode tension et de 6mm^2 pour le pilote en mode courant, ce qui est plus représentatif d'un point de vue industriel.

Simulations transitoires des prototypes

Des simulations après implémentation physique de la puce complète avec des modèles parasites de boîtier et de PCB sont nécessaires pour valider l'implémentation du circuit et évaluer les performances du prototype de pilote de diode laser. Une netlist RLCG mod-

élisant les parasites pour les pistes de PCB a été extraite d'un PCB précédent. Néanmoins, il n'est pas ici question de modéliser en profondeur tous les parasites au sein du système. La netlist peut être réutilisée pour donner une première approximation de l'impédance pour les chemins de courant d'intérêt en modélisant principalement les inductances parasites. Pour le pilote en mode tension, l'inductance parasite équivalente à travers le chemin de courant de la diode laser a été évaluée à 1,5nH. Pour le pilote en mode courant, l'inductance parasite équivalente a été évaluée à 800pH à travers le chemin de courant de la diode laser et 700pH à travers le chemin de courant du bloc HFS.

Des simulations ont été effectuées dans des conditions typiques sur des périodes de commutation suffisantes pour faire fonctionner le convertisseur DC/DC en régime permanent. Chaque version parmi les 10 prototypes a été évaluée, ce qui a nécessité beaucoup de temps (15h chacun pour un seul point de fonctionnement). Bien qu'un signal de grille approprié soit fourni à l'élément de commutation, une forte distorsion sur le courant de la diode laser est remarquée. Elle est causée par les fortes inductances parasites, où le temps de montée est plus lent que le temps de descente pour le pilote en mode tension alors que c'est le contraire pour le pilote en mode courant, ce qui confirme les résultats de l'étude de conception préliminaire. Des pics de tension sont remarqués au niveau du nœud de commutation pour chaque cas, qui semblent être bloqués dans une certaine mesure par la diode de serrage. Même si des surtensions supérieures à 4,8V sont signalées, le transistor cascode assure toujours une protection pour l'élément de commutation. Il est également remarqué qu'une tension de sortie de 5V pour une tension d'entrée de 3,6V est nécessaire pour que le pilote en mode tension atteigne le courant ciblé, confirmant qu'une structure buck-boost est essentielle pour ce type de topologie de pilote vis-à-vis des spécifications. Enfin, même si des valeurs de rendement légèrement inférieures à 70% sont rapportées, les chiffres semblent raisonnables dans des conditions typiques au premier ordre.

En conclusion, bien que les inductances parasites aient un fort impact sur les performances transitoires, les résultats de la simulation valident la mise en œuvre du circuit, prouvant que les deux pilotes sont capables de générer de fortes impulsions de courant à haute fréquence. L'inductance parasite équivalente pourrait être réduite avec une conception de PCB appropriée. Ces résultats sont cependant insuffisants pour évaluer correctement les performances de l'ensemble du système, principalement en raison de modèles de diodes incomplets.

Chapitre 4 : Tests et Résultats de Mesure

Ce chapitre détaille les résultats des mesures électriques et optiques obtenus sur les prototypes de circuits intégrés. Certaines considérations pour concevoir une carte de test appropriée et effectuer des mesures sont passées en revue. Un processus de debug pour vérifier les différentes fonctionnalités du circuit est effectué avant de réaliser un ensemble de mesures. Les résultats de performance sont ensuite discutés.

Cartes et banc de test

Une carte de test est nécessaire pour le montage des composants ainsi que pour la configuration et les tests des prototypes. Un micro-contrôleur avec une interface I^2C doit être utilisé pour fournir les signaux de contrôle à la puce. Il a été décidé de développer trois cartes de test:

- une carte de validation des diverses fonctionnalités du circuit comprenant les deux pilotes (appelée carte de 'validation"),
- une carte de mesure des performances électriques et optiques, présentant une conception optimisée pour le pilote en mode tension uniquement (appelée carte "mode tension"),
- une carte de mesure des performances électriques et optiques, présentant une conception optimisée pour le pilote en mode courant uniquement (appelée carte "mode courant").

Les deux pilotes étant implémentés sur une même puce, un soin particulier doit être pris en compte au niveau de la conception de la carte pour effectuer des tests sans affecter les fonctionnalités et les performances d'un pilote par rapport à l'autre. Les pistes de PCB doivent être aussi moins résistives et inductives que possible pour les chemins de courant haute puissance. Le module VCSEL et les autres composants hors puce doivent être placés aussi près que possible de la puce. Un grand plan de masse et des VIA thermiques pourraient être utilisés pour améliorer la dissipation thermique de la carte.

Le défi majeur ici est d'effectuer des mesures électriques et optiques avec une précision suffisante sans impacter les performances du système. Le dispositif expérimental doit aussi faire face à de fortes contraintes liées aux niveaux de puissance élevés, aux impulsions de courte durée à des fréquences élevées, aux normes de sécurité oculaire ainsi qu'aux petites dimensions du circuit et des composants.

La principale préoccupation pour l'acquisition de signaux électriques et optiques dans le domaine temporel est la bande passante limitée de l'équipement ainsi que la méthode de sondage. Des sondes asymétriques et différentielles à large bande passant pourront être utilisées pour mesurer les tensions. La mesure du courant via la chute de tension à travers une résistance de shunt pourra être utilisé. Cependant, l'introduction d'une résistance de

shunt en série avec la charge peut augmenter la chute de tension et l'inductance parasite équivalente dans le chemin, ce qui est très critique dans ce contexte. En conséquence, cette méthode de mesure ne doit être utilisée qu'à des fins de débug. La valeur du courant crête sera estimée en utilisant la mesure de puissance optique et les caractéristiques du VCSEL issues de la fiche technique.

L'acquisition de la forme de l'impulsion laser permet de mesurer des performances transitoires telles que la largeur d'impulsion, les temps de montée et de descente. Un photodétecteur en espace libre à large bande passante pourra être utilisé pour simplifier la configuration.

La mesure de la puissance optique permet d'estimer le rendement électro-optique du système incluant le pilote et le module VCSEL, qui correspond au ratio de la puissance optique de sortie sur la puissance électrique d'entrée. Cette dernière étant fournie par l'alimentation, l'utilisation d'un équipement approprié tel qu'un générateur de puissance dit "sourcemeter" permettra d'accéder à cette valeur. La mesure de la puissance optique pourra être réalisée en utilisant une sphère d'intégration associée à un détecteur de puissance et un wattmètre. La sphère d'intégration permet la collecte totale du rayonnement électromagnétique d'une source. Le niveau de rayonnement intégré résultant est directement proportionnel au niveau de rayonnement initial et peut être mesuré à l'aide d'un détecteur de puissance. Ce type de configuration est cependant destiné aux sources de lumière à onde continue ou pulsée jusqu'à des fréquences d'impulsions de 250kHz. Dans ce contexte, il pourra être utilisé pour mesurer la puissance optique moyenne d'un train d'impulsions. La puissance optique crête des impulsions sera déterminée avec en connaissant la fréquence de modulation et le rapport cyclique.

Le rendement électrique du pilote sera estimer via la mesure des puissances électriques d'entrée et de sortie sur un train d'impulsions. La puissance d'entrée peut être facilement lue à l'aide du "sourcemeter". La mesure de la puissance de sortie est une tâche plus difficile. Il est proposé ici de l'estimer en utilisant la mesure de puissance optique et les caractéristiques du VCSEL issues de la fiche technique. Les estimations de la puissance électrique de sortie, ainsi que du courant crête, ne sont valables que si l'on considère les valeurs de courant dans la région linéaire de la courbe caractéristique VCSEL. Par conséquent, les résultats doivent être utilisés avec précaution.

Enfin, l'environnement de test devra être conforme aux normes de sécurité laser. Un boîtier de protection laser muni d'un verrouillage électrique sera utilisé pour effectuer les mesures, en utilisant de plus des lunettes de protection laser.

La conception et l'implémentation des circuits imprimés ont été réalisées par différents membres de l'équipe, sur la base des considérations précédemment détaillées. Toutes les cartes de test reposent sur un PCB double face utilisant 6 couches afin de router correctement tous les signaux et les chemins d'alimentation, avec un large plan de masse commun sur la couche 3. Les pistes du PCB sont en cuivre tandis que le diélectrique est un diélectrique en verre époxy FR4 . Les cartes ont une taille de 12,5cmx18cm. Des trous

sont usinés pour fixer la carte à la sphère d'intégration. Toutes les cartes de test incluent une version du prototype IC ($5mm^2$), une charge et des composants passifs hors puce situés dans une petite zone (environ $15mm_2$) en raison de contraintes physiques liées à la sphère d'intégration et pour limiter les éléments parasites. Il est précisé que les cartes en mode tension et en mode courant n'intègrent que quatre petits condensateurs céramiques 0603M (22nF, 10nF, 4.7nF et 2.2nF) comme condensateurs de découplage pour l'alimentation du bloc HF.

Les cartes de test présentent une disposition similaire et incluent des fonctionnalités communes pour simplifier les procédures de réglage et de mesure, comme une interface I_2C contrôlée à l'aide d'un microcontrôleur STM32F407 de STMicroelectronics, plusieurs chemins d'alimentation pour alimenter correctement les blocs analogiques, numériques et de puissance de la puce, plusieurs entrées via des connecteurs SMA pour les signaux de modulation, ainsi que des points de mesure pour accéder aux signaux d'intérêt.

Chaque carte comprend également des fonctionnalités spécifiques pour assurer un bon fonctionnement de la puce en fonction du pilote utilisé. La carte de validation comprend tous les composants liés aux pilotes en mode tension et en mode courant ainsi qu'une charge résistive pour le débug et la validation du prototype dans un environnement de test standard (sans contraintes optiques). Les cartes en mode tension ou courant comprennent tous les composants liés au pilote en mode tension ou courant respectivement. Le but de ces cartes est d'effectuer principalement des mesures optiques, seule la diode laser est donc assemblée.

L'équipement utilisé pour le banc de test comprend une alimentation "DC power analyzer" N6705B de Keysight, un générateur d'impulsions 81110A de Agilent et un générateur de signaux 33600A de Keysight pour générer le signal de modulation différentielle LVDS et le signal d'enveloppe fournissant le motif de trains d'impulsions. Les impulsions laser sont capturées par le photodétecteur rapide ic212 de iCHaus possédant une bande passante de 1.4GHz. Les signaux sont mesurées à l'aide de l'oscilloscope MSOS254A de Keysight possédant une bande passante de 2.5GHz. La sphère d'intégration 819D-SL-5.3-CAL2 de Newport ainsi que l'instrument de mesure de puissance optique 19336-R de Newport associé au détecteur optique 918D-SL-OD1R de Newport sont utilisés pour effectuer les mesures de puissance optique.

Débug des prototypes

L'étape de débug consiste à mettre la puce sous tension et à vérifier son comportement électrique dans des conditions DC. Cela permet de vérifier si le convertisseur DC/DC et le bloc HF fonctionnent comme prévu et indépendamment de la modulation haute fréquence. Les principales caractéristiques à vérifier sont la régulation du courant, la caractérisation de la résistance du canal de l'élément de commutation en fonction de sa largeur de grille configurable, la caractérisation de la source de courant de pré-polarisation (pour le pilote en mode tension uniquement) et la caractérisation de la diode de serrage. Il est précisé

que les cartes de validation ont été reçues début novembre 2019. En raison d'un calendrier restreint lié au contexte industriel, les principales caractéristiques n'ont été vérifiées que dans des conditions typiques.

Les premières mesures concernant la régulation du courant pour le pilote en mode tension ont montré que le convertisseur DC/DC fonctionnait correctement avec une fréquence de 4MHz, comme prévu. Le convertisseur est capable de générer le bon courant de sortie en balayant le courant de référence de 0 à 3A, dans des conditions typiques. Un très faible écart type du courant mesuré est également remarqué, ne montrant aucun problème de stabilité.

En revanche, les premières mesures pour le pilote en mode courant ont montré un comportement erratique avec des problèmes de stabilité, en particulier pour les faibles courants de sortie. Même si le convertisseur DC/DC fonctionne bien en mode abaisseur avec une fréquence de 4MHz comme prévu, le rapport cyclique du circuit PWM est instable à de faibles courants de sortie, perturbant ainsi la régulation du courant. De plus, le convertisseur ne semble pas être en mesure de fournir un courant de sortie élevé. En fait, cela est causé par la charge résistive induisant une tension de sortie élevée sous des conditions DC. Dans des conditions de fonctionnement normales (lors de la commutation du courant de diode laser), la tension de sortie effective devra être inférieure. Enfin, une ondulation triangulaire du courant de sortie est remarquée, mais cela reste un comportement attendu du faire de l'absence de condensateur de sortie. Quelques perturbations ont également été remarquées sur le circuit de référence de tension de bande interdite (1,22V) quel que soit le courant de sortie. Elles pourraient être causées par un couplage entre le convertisseur DC/DC et le circuit de bande interdite via des interconnexions internes et/ou externes.

Dû un problème technique, la résistance de canal de l'élément de commutation n'est pas accessible. Il est alors proposé de caractériser la résistance totale des transistors de commutation et cascode. La résistance totale diminue à mesure que la largeur de grille augmente, comme prévu. Néanmoins, un écart est remarqué pour les petites largeurs de grille, qui est dû au transistor cascode et à l'élément de commutation fonctionnant presque en régime de saturation. Le réseau de métallisation complexe reliant le transistor cascode à chaque partie de l'élément de commutation contribue également à augmenter la résistance totale. Pour cette raison, il est recommandé d'utiliser une largeur de grille supérieure à 15mm afin d'assurer une résistance totale suffisamment faible, en particulier pour le pilote en mode courant.

La source de courant de pré-polarisation est caractérisée pour le pilote en mode tension uniquement. Le courant augmente à mesure que le courant de référence augmente, comme prévu. Une légère déviation est cependant constatée à des valeurs de courant élevées pour un niveau de tension élevé (2,5V) au nœud de commutation. Ce problème provient à la fois de la différence d'adaptation des tensions drain-source et du paramètre de modulation de

longueur de canal λ. Cela est dû à la résistance de sortie finie des transistors ($\lambda \neq 0$). Quoi qu'il en soit, ce n'est pas un problème majeur puisque cette fonctionnalité est destinée à être testée dans un premier temps, et qu'une grande précision n'est pas indispensable dans ce contexte.

Enfin, les deux types de diode de serrage (jonction P-N et Schottky) sont caractérisées dans des conditions typiques (25 °C). Les courbes courant-tension de ces diodes sont obtenues comme attendu, avec une tension de seuil pour la diode Schottky estimée à environ 0,3V et 0,7V pour la jonction P-N.

Mesures des prototypes

La deuxième étape consiste à mesurer les performances du système, en termes de mesures transitoires (temps de montée et de descente, largeur d'impulsion) et de puissance (rendements électriques et optiques). Malheureusement, les cartes mode tension et courant ont été reçues fin février 2020 en raison de problèmes techniques. Par conséquent, seul un premier ensemble de mesures pour un cas d'utilisation typique (courant à l'état ON de 3A, fréquence de modulation 200MHz) a été effectué dans des conditions typiques (tension d'entrée 3,6V, 25°C) afin de valider le principe de fonctionnement du pilote. Il est proposé de vérifier le comportement électrique transitoire des pilotes mode tension et mode courant lors de la commutation du courant en utilisant une charge résistive dans un premier temps. Ensuite, la forme de l'impulsion laser est mesurée, en utilisant le module VCSEL comme charge, afin de vérifier le comportement transitoire électro-optique des pilotes. L'impact de la diode de serrage est rapidement étudié. Les performances en termes de puissance sont ensuite mesurées. En raison de problèmes techniques, il n'a pas été possible de tester la version 1 du prototype de pilote en mode tension. 9 prototypes sur 10 ont été testés au final.

Les premières mesures électriques ont montré que le pilote en mode tension est capable de générer des impulsions de courant. Cependant, des perturbations ont été remarquées sur le circuit de référence de tension de bande interdite, qui n'ont pas été observées dans des conditions DC. Dans ce cas, une valeur moyenne de 1,06V au lieu de 1,22V est signalée pendant le train d'impulsions, provoquant des imprécisions sur la boucle de contrôle en courant. Des perturbations plus accentuées ont été notées pour des fréquences plus élevées.

Pour le pilote en mode courant, les premières mesures électriques ont montré qu'il était capable de générer des impulsions de courant. Comme prévu, une ondulation sur le courant de charge est remarquée conduisant à une valeur crête oscillant entre 2,2A et 2,5A alors que 3A était ciblé. Bien qu'un comportement erratique similaire à celui observé en conditions DC ait été observé ici, le problème de la régulation du courant pourrait être expliqué par des interférences remarquées sur la tension de bande interdite, conduisant à une valeur moyenne de 0,92V au lieu de 1,22V. Les pics de tension sur la tension de

bande interdite semblent se produire de manière synchrone avec la commutation de l'étage de puissance. Des perturbations plus accentuées ont été notées pour des fréquences plus élevées.

La référence de tension de bande interdite (1,22V) est perturbée lors de la commutation du courant pour les pilotes en mode tension et en mode courant. Les interférences pourraient être causées par un couplage entre le convertisseur DC/DC, le bloc HF et le circuit de bande interdite via des interconnexions internes et/ou externes. En réalité, il a été remarqué que les pistes de masse analogique et de puisssance n'étaient pas fusionnées sur la bonne couche au sein du PCB, ce qui pourrait conduire à générer un bruit important à travers des blocs analogiques, tels que le circuit de bande interdite. La résolution de ce problème technique nécessite une nouvelle conception des cartes de test qui n'a pas pu être réalisée ici en raison de contraintes de temps. Il est alors proposé de contourner le problème en connectant la broche de masse analogique de la puce à la broche de masse du substrat située au centre de la puce en utilisant un fil métallique fin. Après de nouvelles mesures, une bonne amélioration est notée pour les cartes de test comportant la modification, confirmant que le couplage peut provenir de connexions à la masse. Néanmoins, une légère déviation est encore constatée pour des courants et fréquences élevés. Cela indique qu'un couplage à la masse subsiste et qu'il est probablement dû aux interconnexions à travers le substrat de la puce, à la métallisation, aux pistes PCB et/ou au plan de masse. Ce problème n'a pas pu être résolu durant le travail de thèse. Malgré ces perturbations rendant la régulation du courant moins précise, les pilotes peuvent tout de même être utilisés en boucle ouverte en ajustant le courant à l'état ON via l'interface I^2C pour atteindre la valeur souhaitée.

Par la suite, les premières mesures optiques ont montré que le pilote en mode tension est capable de générer des impulsions laser. Une distorsion est quand même constatée sur la forme de l'impulsion laser, en particulier pour les hautes fréquences. Le temps de montée de l'impulsion laser est plus lent que le temps de descente, comme pour en simulation. Cela confirme que les éléments parasites ont un impact sur le courant photo-générateur. De plus, une impulsion laser secondaire très courte se produit lorsque l'impulsion est coupée. Elle pourrait être provoquée par la forte résonance observée sur la tension du nœud de commutation qui devient suffisamment basse pendant un bref instant pour réactiver la diode laser. Des pics de tension d'environ 7,5V sont remarquées au niveau du nœud de commutation, suggérant que la diode de serrage est moins efficace que prévu. De plus, une tension d'anode de 4V pour une tension d'entrée de 3,6V est nécessaire, confirmant qu'une structure buck-boost est essentielle pour ce type de topologie de pilote en mode tension.

Pour le pilote en mode courant, les premières mesures optiques ont montré qu'il est capable de générer des impulsions laser, malgré son comportement erratique à de faibles courants de sortie. Une distorsion est cependant constatée sur la forme de l'impulsion

laser, en particulier pour les hautes fréquences. Le temps de descente de l'impulsion laser est plus lent que le temps de montée, comme en simulation. Les éléments parasites ont aussi un impact sur le courant photo-générateur. De plus, un léger dépassement est remarqué sur le signal laser lorsque l'impulsion est activée. Cela pourrait être dû à la forte résonance observée sur le nœud de commutation où un pic de tension autour de 6V-7V est reporté, ce qui suggère que la diode de serrage est également moins efficace que prévu. Il est rappelé que la tension de serrage est ici la tension d'entrée (3,6V). Enfin, une ondulation triangulaire a été observée sur le train d'impulsions laser, en raison de l'ondulation du courant comme attendu.

Il est proposé d'évaluer l'impact de la diode de serrage en mesurant le pic de tension se produisant au nœud de commutation dans des conditions normales de fonctionnement. Pour obtenir une comparaison équitable, les mêmes conditions, selon le mode tension ou courant, doivent être prises en compte. En raison de la configuration expérimentale limitée et des résultats de mesure, aucune distinction ne peut être faite entre les diodes Schottky et P-N. Néanmoins, l'utilisation d'une diode de serrage semble avoir un impact positif mais limité sur les pics de tension. Ce problème pourrait s'expliquer par la haute impédance des parasites sur le trajet du courant de la diode de serrage. En effet, la diode est acheminée vers le bloc HF via une piste étendue qui pourrait ajouter des inductances parasites supplémentaires. Une solution pourrait être de rapprocher la diode de serrage du nœud de commutation afin de réduire la métallisation, mais cela semble assez compliqué au regard du nombre élevé de fonctionnalités incluses dans le bloc HF. L'ajout d'un amortisseur dit "snubber" en parallèle à la diode de serrage pourrait également être intéressant afin de créer un chemin de courant supplémentaire. Ces options nécessitent cependant une re-conception complète de la puce, ce qui n'a pas pu être fait ici. Enfin, ce problème n'a pu être résolu dans le travail de thèse.

Les mesures en terme de puissance ont été effectuées en visant une puissance optique crête de 2,5 W. La valeur du courant ainsi que la largeur d'impulsion du signal différentiel externe ont alors été ajustés en conséquence, notamment à cause d'une potentielle distorsion du signal laser et des perturbations notées sur la boucle de régulation. De plus, la largeur de grille de l'élément de commutation a été correctement configurée pour minimiser les pertes totales (27mm et 54mm ont été retenues pour les cas d'utilisation 3A, 50MHz et 3A, 200MHz).

Le pilote en mode tension semble être plus efficace que le pilote en mode courant quelle que soit la version de prototype pour une fréquence de modulation de 50MHz. Les résultats doivent cependant être considérés avec précaution car ils sont principalement basés sur des estimations approximatives en raison de la configuration expérimentale limitée. De plus, ils sont assez hétérogènes pour une fréquence de 200MHz. On voit que le pilote en mode tension semble être plus efficace que le pilote en mode courant avec une diode Schottky (V2 et V4). Au contraire, le pilote en mode courant a un meilleur rendement énergétique que

le pilote en mode tension, mais uniquement avec une diode P-N ainsi que d'un transistor cascode GO2 (V3). Aucune distinction n'est faite pour la version 5. Par conséquent, aucune conclusion stricte ne peut être tirée sur la base de ces résultats de mesure.

Discussion et conclusion

En raison de certains problèmes techniques et de contraintes de temps liés au contexte industriel, seul un premier ensemble de mesures de transitoires et de puissance pour deux cas d'utilisation typiques (2,5W à 50MHz et 200MHz) a été obtenu dans des conditions typiques. Ces résultats reposent sur des estimations approximatives en raison de la configuration expérimentale limitée et du manque de données sur le module VCSEL. Par conséquent, ils doivent être considérés avec précaution. Même si cet ensemble de mesures peut prouver que le pilote en mode tension et le pilote en mode courant sont capables de générer des impulsions laser conformément aux spécifications générales, il ne démontre pas pleinement la faisabilité d'intégrer ce type d'architecture sur une seule puce prenant en compte les contraintes du téléphone mobile. Néanmoins, la caractérisation de diverses fonctionnalités dans des conditions DC et pulsées a mis en évidence des problèmes importants mais dont les causes ne sont pas encore clairement identifiées. Des investigations supplémentaires devront être poursuivies.

Conclusion Générale

La thèse fut axée sur l'étude et la conception d'un pilote de diode laser compact, peu cher et efficace pour des applications de détection de profondeur utilisées dans les téléphones mobiles. L'objectif principal était de valider une architecture intégrée pour le pilote de diode laser capable de générer de courtes impulsions de courant de quelques ampères avec une largeur d'impulsion de 2,5ns jusqu'à une fréquence de répétition d'impulsions de 200MHz tout en considérant l'efficacité énergétique comme une exigence majeure.

En raison de certains problèmes techniques et de contraintes de temps liés au contexte industriel, seul un premier ensemble de mesures pour deux points de fonctionnement typiques a été obtenu. Les pilotes en mode tension et en mode courant sont capables de générer des impulsions laser conformément aux spécifications générales. En revanche, la faisabilité d'intégrer ce type d'architecture sur une seule puce en tenant compte des contraintes de la téléphone mobile n'est pas pleinement démontrée. Effectuer un second ensemble de mesures (en balayant la fréquence de modulation, le courant crête et la tension d'entrée par exemple) s'avère essentiel afin de valider les performances des prototypes. Le banc de test pourra être consolidé pour améliorer la précision de mesure. De plus amples investigations sont également requises afin de confirmer les problèmes rencontrés par rapport au couplage de masse entre blocs analogiques et bloc HF. Il en va de même concernant l'efficacité de la diode de serrage. Enfin, le prototype pourra être confronté à un capteur d'image "Temps de Vol" afin de valider le fonctionnement globale du système au niveau applicatif.

Pour ce faire, il pourrait être proposé de suivre une méthodologie basée sur la reconception de deux circuits intégrés distincts mettant en œuvre séparément le pilote en mode tension et le pilote en mode courant. En effet, l'approche adoptée dans le travail de thèse a conduit à réaliser une seule puce pour implémenter les deux pilotes. Il comprend ainsi un très grand nombre de blocs de construction. Bien qu'un soin particulier ait été apporté aux niveaux du circuit et du système pour s'assurer qu'un seul pilote fonctionne à la fois, il existe toujours un risque de provoquer des interférences. Identifier les causes des problèmes peut alors s'avérer plus délicat. On pourrait se demander si le gain de temps et de ressources obtenu en utilisant cette approche de conception (une seule puce pour deux pilotes) ne serait pas perdu en induisant des investigations plus longues, retardant ainsi le projet global (une sorte d'effet rebond). Par conséquent, une approche de conception plus conventionnelle mettant en œuvre une architecture de pilote unique avec un nombre réduit de fonctionnalités pourrait être adoptée afin de faciliter les procédures de débug, de mesure et de validation. Ensuite, des améliorations et de nouvelles fonctionnalités pourraient être envisagées en développant un deuxième prototype, et ainsi de suite. Ce type de méthode itérative pourrait permettre de construire un pilote de diode laser robuste reposant sur des fondations solides.

Comme présenté dans l'introduction générale, les capteurs d'image 3D sont des éléments clés pour exploiter pleinement les applications émergentes dans les domaines de l'imagerie 3D et de la vision par ordinateur. Entre autres, la reconnaissance faciale a connu un intérêt croissant pour l'industrie des smartphones et les systèmes de sécurité ces dernières années. Bien qu'elle puisse être utilisée pour prévenir la fraude et améliorer l'identification des usagers pour divers installations et appareils par exemple, des usages inappropriés existent également, comme la surveillance de masse. Dans ce cas, qui est responsable ? Le concepteur ou l'utilisateur final ? Le même raisonnement pourrait s'appliquer à un large éventail de sujets. Ceci est laissé comme question ouverte au lecteur.

Au final, l'auteur invite à revoir le rôle de l'ingénieur et du chercheur scientifique en reconsidérant pleinement les exigences environnementales, sociales et éthiques dans le développement d'un concept, d'un produit ou d'un service. Un compromis existe, il faut juste prendre du temps pour le trouver.

General Introduction

3D-Depth Sensing Applications

Three-dimensional (3D) depth sensing systems are sensors able to produce an image containing depth information of the surrounding area. This image is called a depth map. A basic example is shown in Figure 1.

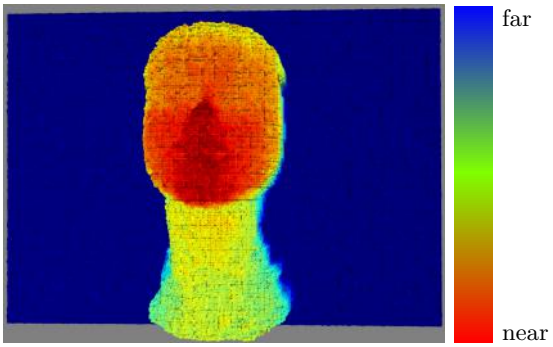


Figure 1 – Depth map of a polystyrene dummy face. Depth information is represented using a color gradient. Source: STMicroelectronics.

Combined with conventional image sensors, producing standard two-dimensional (2D) images, they are capable of taking three-dimensional pictures of the scene. These 3D image sensors are key enablers for unlocking emerging applications in 3D imaging and computer vision field [2][3]. Depth sensing would benefit autonomous vehicles such as self-driving cars, flying drones and robots for helping navigation, mapping and obstacle detection [4]. Such depth-sensing systems employed in automotive applications refers to Light Detection and Ranging (LiDAR) which uses pulsed laser light to measure distance and detect objects. For security systems, one prominent application is the facial recognition where depth sensing is essential for producing an accurate 3D face modeling making systems safer [5]. It could be used for preventing fraud and improving identity authentication for various facilities and devices. Depth sensing is also necessary for developing new user interfaces based on Mixed Reality (MR) requiring gesture detection and control [6]. These

interfaces are employed in industry for improving quality controls [7] or in medical for image-guided therapies for instance [8]. Depth sensing would benefit other applications in various sectors as well such as biometrics [9], agriculture [10], cartography and Earth science fields [11][12], 3D video and gaming [13][14] and many more.

More recently with the context of Covid-19 crisis, a high demand for technologies supporting social distancing and allowing to avoid touching devices will emerge in the near future [15]. Although solutions already exist for similar applications, depth sensing could be beneficial addressing this new demand by developing more efficient and cost-effective systems [16].

Image Sensor Market and Motivation

3D depth sensors mostly rely on light waves-based range-measuring techniques (further discussed below) [17]. Depending on the technique, systems employ optoelectronic components such as image sensors and laser transmitters. Optoelectronics market faces strong growth widely led in last decade by image sensor products and more recently by laser transmitters including devices for new 3D-depth sensing applications [1]. According to IC Insights, sales of Complementary Metal Oxide Semiconductor (CMOS) image sensors, leading technology over Charge-Coupled Device (CCD) image sensors, are expected to increase by a Compound Annual Growth Rate (CAGR) of 8.7% in the five-year forecast period (2018-2023) reaching $21.5 billions in 2023 while laser transmitter sales are projected to grow by a CAGR of 8.3% in the same forecast period, reaching $2.6 billions in 2023. In the ten past years, CMOS image sensor growth was driven by the rapid spread of embedded cameras in cellphones and portable computers. In 2018, consumer electronics including smartphones, tablet computers, portable PCs and stand-alone digital cameras is still the major sector of CMOS image sensor market representing 73% of market shares as illustrated in Figure 2. Although automotive applications are expected to be the fastest growing application for CMOS image sensors with 15% of market shares in 2023 according to IC Insights, consumer electronics seems to be a promising sector for developing future 3D image sensors specially for mobile phones with a 45% forecast of market shares in 2023.

Despite plenty of research on three-dimensional imaging techniques initiated in the late 1970's [18][19][20][21][22], the first consumer product started to emerge in 2010 with a range-imaging camera named Kinect™ and developed by Microsoft in collaboration with Prime Sense. This camera relied on a structured-light principle in which the deformation of a known pattern projected on an object is captured by an image sensor and analyzed to determine depth and three-dimensional shapes [23]. The device was intended for gaming allowing the user to control the game through body motions. The development of such range-imaging cameras for consumer electronics has accelerated in following years from companies dedicated to 3D imaging applications mostly using Time-of-Flight (ToF)

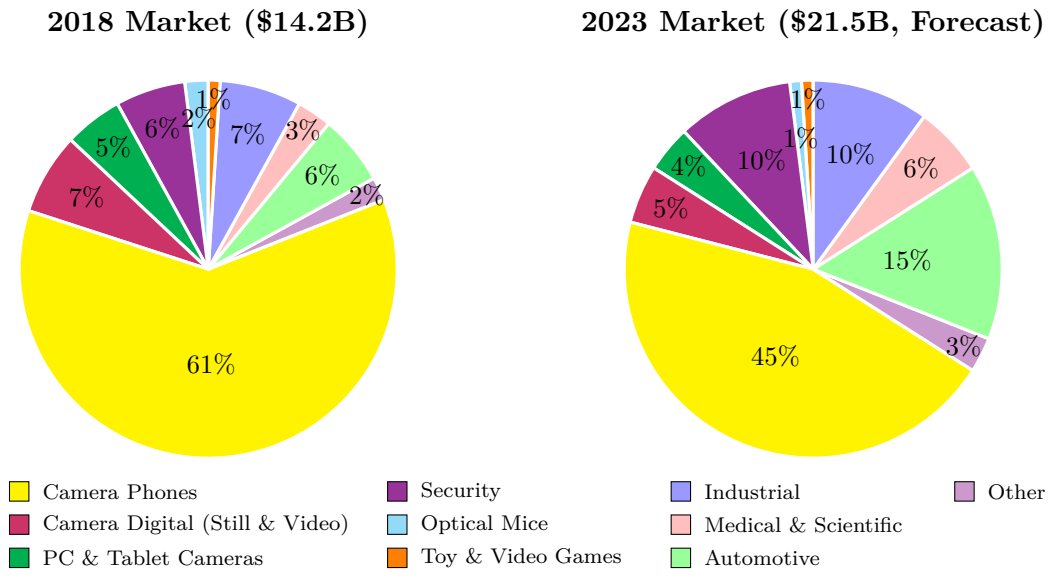


Figure 2 – Where CMOS image sensor sales are going. Source: IC Insights [1].

principle-based technologies [24]. Knowing the speed of light, ToF principle measures the time taken by emitted photons to reflect from an object back to an image sensor in order to determine depth. Pioneer companies such as pmdtechnologies, SoftKinetic or MESA Imaging have developed commercial 3D ToF cameras with various performances, sizes and costs intended for computers helping to sense the real world in 3D. A state-of-the-art of commercial ToF range camera modules dated 2016 can be found in [25].

More recently, companies dedicated for 3D imaging applications and leading companies in semiconductor industry have settled strong collaborations in order to develop new solutions for mobile phones. In 2014, Google initiated the Tango project for supporting Augmented Reality (AR) applications in mobile phones. In 2016, Lenovo, working in collaboration with Google, OmniVision Technologies, Infineon Technologies and pmdtechnologies, has introduced the first mobile phone named Phab 2 Pro with a ToF-based depth sensing camera module which is placed in the rear face for AR applications and enhanced photography. In 2015, Sony acquired SoftKinetic to propose ToF image sensors for smartphones in the coming years [26]. In 2013, Apple acquired Prime Sense and released in 2017 the first mobile phone named iPhone X with a structured light-based depth sensing camera module which is placed in the front face primarily for supporting facial recognition. It allows the user to unlock the phone and authorize electronic payments [26]. STMicroelectronics has launched in 2014 its first ToF ranging sensor named VL6180X embedded in front face of mobile phones as a proximity sensor for user detection up to 10cm, mostly used for locking the phone when calling. Then, STMicroelectronics announced new ToF ranging sensors such as the VL53L0X module measuring distances up to 2m used for pres-

ence detection and the VL53L1 module for multi-object detection up to 4.5m assisting autofocus cameras in smartphones for instance [26].

The department "Analog, MEMS and Sensors" at STMicroelectronics, in which this thesis took place, aims to extend its ranging sensor lineup by developing new 3D image sensors intended for mobile phones and capable of mapping a scene in three dimensions.

3D Image Sensor Requirements

Some requirements must be considered for developing the new 3D image sensor under STMicroelectronics' approach. A depth map of the scene should be acquired for a given Field-of-View (FoV) of 60x45°. Therefore, no scanning mechanism is necessary. Indoor conditions are assumed here meaning low background illumination. The sensor should be robust against the shape and reflectance of objects from the scene. A minimum Video Graphic Array (VGA) resolution (640x480 pixels) is specified for the depth map with a millimeter depth resolution from centimeters up to few meters operating range. Other requirements for the module depends on the application field. In the case of mobile phones, **the power efficiency is a major concern** as it impacts **the self-heating of the device**, thus performances, as well as **the battery lifetime**. In addition, a compact and cost-effective system is essential in order to propose a solution for consumer electronics that can be easily embedded in portable devices for an affordable cost.

In this context, light waves (usually $\lambda = 0.5 - 1\mu m$) are well suited for range measurement in contrast with radio and sound waves (usually $\lambda = 3 - 30mm$ and $\lambda = 0.1 - 1mm$ respectively) mainly due to diffraction effect limiting the spatial resolution, which is the ability of a sensor to distinguish details of an object [27]. It exists several techniques based on light waves for range measurement such as the stereovision, structured-light or Time-of-Flight principles [27][28][29]. More details can be found in Appendix A. Among these techniques, the indirect Time-of-Flight (iToF) principle offers the advantage of a straightforward, robust and low-cost implementation for mobile applications by using an optical emitter and an image sensor [30][31]. Its operating principle is slightly different from what was explained earlier. The depth is calculated by measuring the phase shift between a modulated optical signal and the optical signal received by the image sensor after reflection on an object from the scene. The depth z to each point of the scene is then given by

$$z = \frac{c}{4\pi f}\varphi \tag{1}$$

where φ is the measured phase shift (restricted to the range $[0\ ;\ 2\pi]$), f is the modulation frequency and c is the speed of light. The block diagram of a typical iToF-based 3D image sensor is depicted in Figure 3. The system consists of two parts:

- An optical transmitter including an emitter (Light-Emitting Diode, LED for short, or laser emitter) and its driving circuitry.

- The so-called image sensor including an array of iToF pixels and a ToF controller for synchronizing signals and providing raw data.

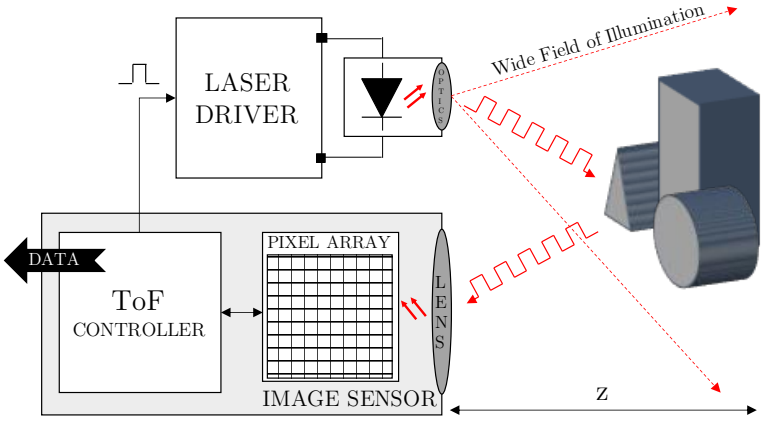


Figure 3 – Block diagram of a typical iToF-based 3D image sensor.

Each pixel from the pixel array contains depth information of a point of the scene. A microprocessor is necessary for processing this data into a depth map. The system however requires data acquired on several illumination cycles before providing a complete depth map. Optical elements, such as a diffuser or lens, are also used in order to condition the light. Usually, the optical transmitter and the image sensor are embedded on separate Printed Circuit Boards (PCBs) giving flexibility for positioning the optical emitter in such a way that its field of illumination is not obstructed by the sensor lens.

Foundations for developing such an iToF-based 3D image sensor under STMicroelectronics' approach have been set from several years thanks to studies and works described in [32][33]. Recently, an image sensor test chip based on iToF principle with a Quarter Video Graphic Array (QVGA) resolution (464x197 pixels) has been developed by STMicroelectronics in collaboration with CEA-Leti (research institute for electronics and information technologies in Grenoble) and the Institute of nanotechnologies of Lyon, as reported in [34]. It demonstrated promising results showing a depth map up to 2m acquired using a LED source modulated at 25MHz. Improving the sensor is necessary in order to fulfill the objectives stated earlier. This has led to define new specifications for the 3D image sensor.

Major specifications are listed in Table 1. The silicon CMOS technology is the best candidate for implementing the image sensor as it is a low cost, low power and mature technology. It is widely adopted for such iToF-based 3D image sensors [30][35][36][37]. For easy readability, key parameters of iToF principle, such as modulation type, unambiguous range, demodulation method, phase shift measurement, depth resolution and optical power budget are detailed in Appendix A. As a summary, optical pulses with a duty cycle

close to 50% are sent through the scene as a modulated signal, corresponding to the Continuous Wave (CW) modulation [28]. Infrared wavelengths are employed not to disturb users as they are invisible for the naked eye. In addition, the 940nm wavelength, totally invisible, is preferred in regards to solar irradiance [38] and eye-safety standards [39]. A high optical power of optical pulses as well as a high modulation frequency are desired to improve the depth resolution [40][31]. Depending on the maximum targeting range, lighting conditions, objects reflectivity, sensor efficiency and eye-safety standards, optical pulses up to 2.5W for a modulation frequency from 50MHz up to 200MHz have been established for reaching a 3m maximum depth with a resolution better than 0.5% of depth. Short pulse trains are also required to avoid human eye damages according to eye-safety standards and for thermal dissipation considerations as well. These specifications rely on iToF key parameters described in Appendix A and derive from prior works done by the "Analog, MEMS and Sensors" department at STMicroelectronics. The present thesis is not intended to detail this work.

Table 1 – Specifications for the iToF-based 3D image sensor.

Parameter	**Value**
Technology	silicon CMOS
Resolution	VGA (640x480 pixels)
Wavelength	940nm
Field of View	60x45°
Demodulation method	Continuous Wave
Depth range	30cm - 3m
Depth resolution	<0.5% of the range
Modulation frequency range	50MHz - 200MHz
Modulation duty cycle	50%
Peak optical power at optical emitter level	up to 2.5W

Thesis Objectives

The present thesis focused on the development of the optical transmitter, including the emitter and its driving circuitry, according to specifications and requirements given for the iToF-based 3D image sensor intended for mobile phones. For generating short optical pulses (2.5ns of pulse width at 200MHz), a semiconductor laser diode is the best candidate as optical emitter due to the inherent high speed of the lasing process. For that reason, the direct modulation method, consisting in modulating the laser signal by the current through the laser diode, is an attractive method to design a compact and low-cost driving circuitry, also known as a Laser Diode Driver (LDD) [41].

Objective

The scientific contribution of the thesis is the study and design of a compact, cost-effective and efficient laser diode driver for 3D-depth sensing applications used in mobile phones. The major objective is to validate an integrated architecture for the laser diode driver capable of generating short current pulses of few Amps with a 2.5ns pulse width up to a 200MHz pulse repetition frequency. The main concern is the power efficiency considered as a leading requirement.

Primary issues addressed in this work are the high level of current and the shaping of short-duration pulse at high repetition frequency because of the parasitic elements in passive components, packages and PCB interconnections. In addition, mobile phones bring strong constraints in design choices such as dealing with the restricted available space and accommodating the limited input voltage range of a battery, typically from 2.8V up to 4.2V [42][43]. Finally and as explained earlier, a high efficiency in the chip is critical for saving the battery lifetime and minimizing any self-heating.

Manuscript Content

The thesis manuscript is organized as follows:

- Chapter 1 presents the state-of-the-art of laser diode drivers for ToF applications. An insight on various circuits from the literature and industry is provided in order to highlight performances, design trends and trade-offs for this type of application. This has helped to identify the most suitable topologies for designing the laser diode driver according to targeted objectives.
- Chapter 2 proposes a preliminary design study for evaluating the feasibility of several driver architectures in a STMicroelectronics' 130nm CMOS technology. A comparative analysis using various indicators is proposed to point out pros and cons of each solution. The most suitable solution with respect to the specifications is used as a basis for designing the laser diode driver prototype.
- Chapter 3 focuses on the design and implementation of the laser diode driver prototype. The novelty here concerns the integration of the whole solution (except the laser diode and some passive components) on a single chip while accommodating mobile phone constraints. As some design choices are conventional, some building blocks issued from previous developments have been reused in order to save time and design resources. Various prototypes have been realized using the hcmos9a analog and mixed signal process.

- Chapter 4 details electrical and optical measurement results obtained on all prototypes. Their performances as well as limitations are then discussed. Issues related to prototypes and measurement setup are also reported.
- General Conclusion summarizes the key contributions achieved during this work. It covers the future work such as performing more measurements to fully demonstrate the feasibility of integrating this kind of driver on a single chip. Further investigations are also required to validate the prototype at system level by considering a typical Time-of-Flight application.

1 State-of-the-Art

Contents

This chapter presents a state-of-the-art review of laser diode drivers dedicated to ToF applications. The methodology of the study consists in finding a classification of circuits from the literature and industry in order to better highlight their common advantages and limitations. Performance results are discussed as well. This will help identifying the relevant topologies for designing the laser diode driver according to specifications.

1.1 Scope of the Study

The major objective of the present thesis is to validate an integrated architecture for a laser diode driver intended for the iToF-based image sensor, as discussed in the General Introduction. The objective of this section is to give some considerations in order to focus the study on relevant circuits with respect to the specifications.

The driver, associated to a laser diode, should be capable of generating short optical pulses of high amplitude at a high repetition frequency while operating at a low input voltage range. Rough specifications for the laser diode driver are reminded in Table 1.1. The Pulse Repetition Frequency (PRF) can also be referred to as the repetition rate or modulation frequency. The pulse duration is often defined as the Full Width at Half Maximum (FWHM) that is the width of the time interval during which the power is at least half the peak power [44]. In this context, the pulse duration or pulse width refers to the Pulse

Width at Half Maximum (PWHM).

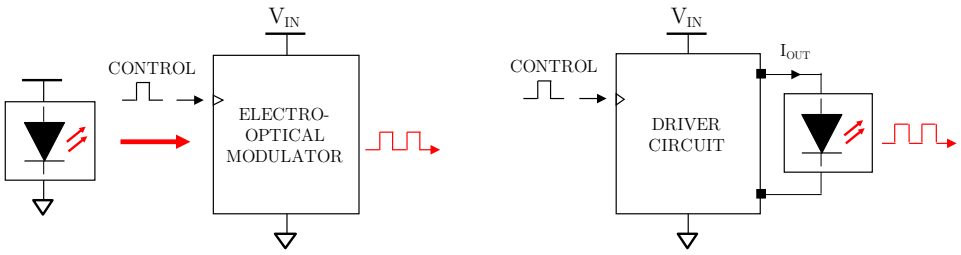
It exists two types of method for modulating an optical signal:

- The external modulation method consists in using an electro-optical modulator for modulating the optical signal coming from the laser diode which is always on, according to a control signal.
- The direct modulation method consists in modulating the optical signal by directly modulating the current through the laser diode, according to a control signal.

Conceptual schematics of the two main modulation methods are illustrated in Figure 1.1. The external modulation method produces a higher quality optical signal with a narrower spectral linewidth in contrast to the direct modulation method, but it is usually more costly and bulky due to the required coupling between the laser source and the external modulator [45][46]. The direct modulation method is thus preferred here due to its low cost and reduced system complexity.

Table 1.1 – Specifications of the laser diode driver.

Parameter	**Value**
Supply voltage range	typically from 2.8V up to 4.2V
Peak optical power	up to few Watts
Peak current	up to few Amps
Pulse repetition frequency (PRF)	from tens of MHz to hundreds of MHz
Pulse width at half maximum (PWHM)	from few ns to tens of ns
Modulation duty cycle	~50%



(a) External modulation. (b) Direct modulation.

Figure 1.1 – Conceptual schematic of the two main modulation methods.

There are many kinds of circuit to drive laser diodes using the direct modulation method. They are intended for various applications such as illumination applications [47], ranging

[48][49] or optical communications [50]. They are even used in printing systems and optical mice [51][52].

Topologies for high-speed modulation of laser diodes such as the ones used for data transmission are suitable for low power devices. In that case, optical power typically is in the range of tens to hundreds of mW [50]. A common topology for digital transmission is based on the current-steering circuit, also known as a differential current switch. A simplified schematic of the driver is shown in Figure 1.2 in a Direct Current (DC) coupled arrangement. The driver is represented with Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices. A differential pair, controlled by the differential input voltage $V^+ - V^-$, is used in order to switch the current either through the laser diode or a dummy load R_D. The bias current is the current provided by the current source I_B when transmitting a zero (laser diode off) while the modulation current, provided by the current source I_M, is added to the bias current when transmitting a signal (laser diode on) [50]. Ideally, the current drawn from the supply voltage V_{IN} is constant ($\simeq I_M+I_B$) causing a power dissipation that is twice that necessary to drive the laser diode.

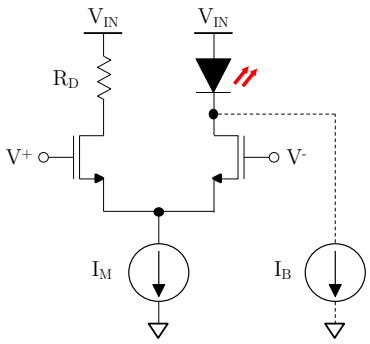


Figure 1.2 – Simplified schematic of the current-steering circuit.

Power losses considerations are usually not a major concern for optical communications. Although this kind of topologies allows high-speed laser operation, they are not compatible with the power range considered in this work, namely several Watts. Therefore, the following state-of-the-art review will focus only on circuits from the literature and industry dedicated to ToF applications or other applications where power and speed requirements are similar to specifications of the present work (see Table 1.1).

Since ToF applications are emerging applications, only few works have been published presenting different laser diode driver circuits with various specifications and performance results. All of them are however intended to generate pulses (whatever is the duty cycle). The methodology of the study consists in finding a classification of these circuits to better highlight their common advantages and limitations. This will help identifying the relevant

topologies for designing the laser diode driver according to targeted objectives.

Performance results are typically the peak current or optical power of pulses, pulse repetition frequency and pulse width. Since these results come from transient measurements, they greatly depend on test conditions. So it is quite complicated to fairly compare the published demonstrators. However, gathering the results can give an overview on trends and trade-offs on the driver topologies. Other results and design parameters such as the power consumption and efficiency, the implementation approach (discrete or integrated approaches) and technology, chip and package sizes, laser diode type and component values are also considered when available. Main results are summarized in Table 1.2.

Table 1.2 – Scope of the state-of-the-art review.

Parameter	**Value**
Number of papers	28
Year range	1997 - 2018/2019
Peak optical power range	50mW - 50W
Optical pulse width	100ps - 6ns
Peak current range	200mA - 155A
Current pulse width	500ps - 50ns
Pulse repetition frequency range	10kHz - 200MHz

In following sections, laser diode driver circuits from literature and industry for ToF applications are reviewed. The scope of the study is to be as exhaustive as possible, covering papers from 1997 up to 2018. It may be specified that several papers deal with the same circuit but present different results. About the design flow, even if steps have been launched in mid-2018, recent papers such as the ones published in 2019 are also included in the review in order to highlight design trends for this type of application.

Drivers may be divided into two major classes according to the classification described in [53]. The classification depends on how the pulse is controlled. There are resonant capacitive discharge drivers and rectangular pulse drivers:

- Resonant capacitive discharge drivers generate current pulses only by triggering the rising edge. The principle relies on a capacitive discharge to produce the pulse. The current pulse width is usually shorter than the pulse width of the control applied to the driving circuitry by using a single-edge control.
- Rectangular pulse drivers generate current pulses by triggering both the rising and falling edges. The current pulse width is roughly equal to the pulse width of the control applied to the driving circuitry by using a dual-edge control.

Operating principle and properties of these driver topologies are firstly described. Advantages and limitations as well as performance results are then presented. It must be specified that these results are mostly from published demonstrators. Results from Post-Layout Simulations (PLSs) are also reviewed but must be considered with caution since they do not prove the entire feasibility of the solution. Lastly, a discussion for selecting the most suitable topology for designing the laser diode driver with respect to targeted objectives is proposed (further discussed in Part 1.4).

1.2 Resonant Capacitive Discharge Driver Topologies

Driver circuits presented in [54][55][56][57][58][59][60][61][62][63][64][65][66][67] are considered here as capacitive discharge drivers.

1.2.1 Operating principle and properties

Although three major configurations can be distinguished from works previously mentioned, they are based on the same operating principle firstly proposed by Kilpelä *et al.* in [54]. Main differences lie in the way of charging the capacitor and the use of a clamping diode. Schematics of various configurations are shown in Figure 1.3 in their basic version for the sake of simplification.

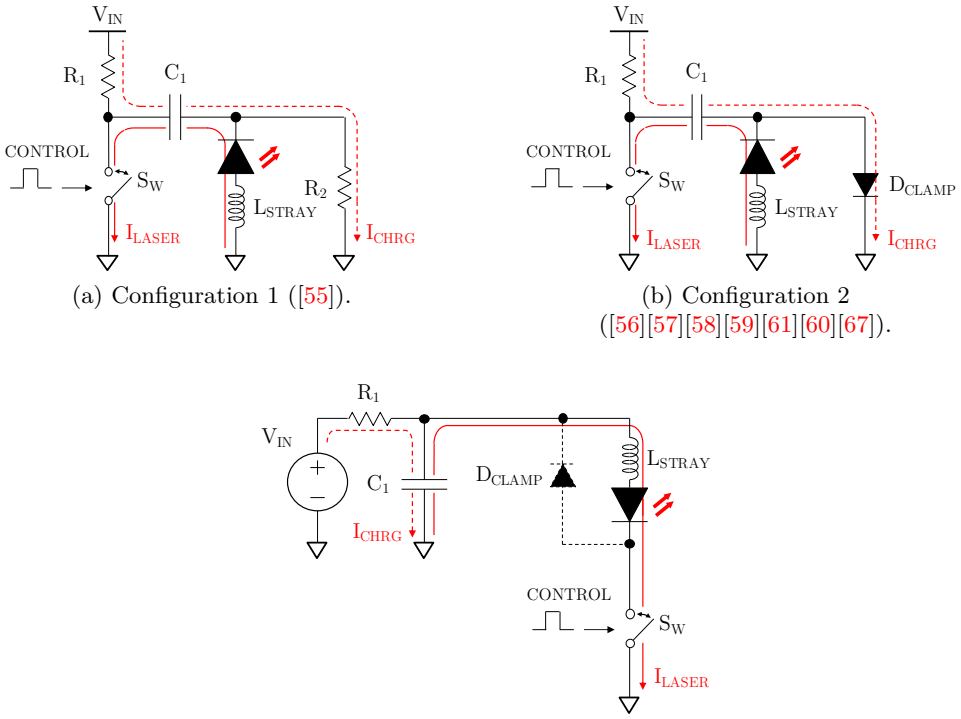
Configuration 1 Key waveforms are illustrated in Figure 1.4. When the switch S_W is turned off, the capacitor C_1 is charged to the supply voltage V_{IN} through resistors R_1 and R_2. The charging time constant is

$$\tau = (R_1 + R_2)C_1 \tag{1.1}$$

The laser diode is reverse-biased during this phase. Then, the capacitor C_1 discharges its energy through the load path as soon as the switch S_W is triggered by the control signal. This generates a current pulse through the laser diode that is now forward biased. At this point, the circuit behaves as a RLC-series circuit comprising the capacitor C_1 and the equivalent series inductance and resistance in the load path. This circuit can be oscillating or not depending on its damping ratio, approximated as

$$\zeta = \frac{R}{2}\sqrt{\frac{C_1}{L}} \tag{1.2}$$

where L and R are the equivalent series inductance and resistance in the load path respectively. Usually, L is the stray inductance L_{STRAY} and R accounts for the series resistance of the laser diode and the switch [55]. The pulse width of the current pulse as well as its peak value are thus determined by the parameters of the RLC equivalent circuit. As the control signal is maintained long enough (principle of a capacitive discharge driver) and



(a) Configuration 1 ([55]).

(b) Configuration 2 ([56][57][58][59][61][60][67]).

(c) Configuration 3 ([62][63][64][65][66]).

Figure 1.3 – Simplified schematics of resonant capacitive discharge driver topologies.

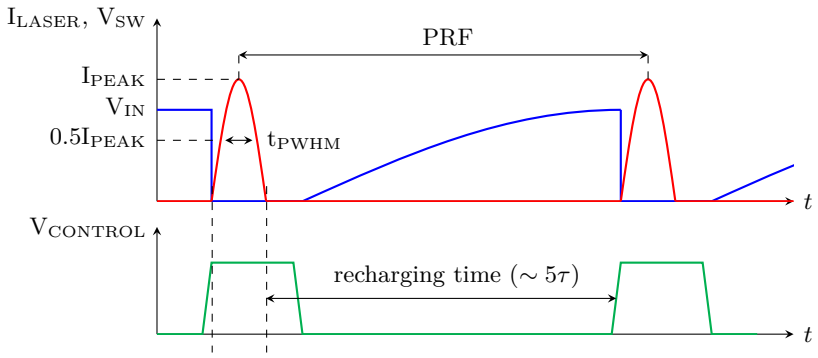


Figure 1.4 – Key waveforms for a capacitive discharge driver: laser diode current I_{LASER} (red), voltage across the switch V_{SW} (blue), control signal $V_{CONTROL}$ (green).

by assuming an optimally damped RLC circuit (when $R \simeq \sqrt{L_{STRAY} C_1}$) in order to avoid ringing, the current through the load path is roughly described by a half-cycle sine wave

[62] with a resonance frequency f_0 given by

$$f_0 = \frac{1}{2\pi\sqrt{L_{STRAY}C_1}} \tag{1.3}$$

The current pulse width t_{PWHM} and peak current I_{PEAK} can be approximated as

$$t_{PWHM} = \frac{1}{3f_0} = \frac{2\pi\sqrt{L_{STRAY}C_1}}{3} \simeq 2\sqrt{L_{STRAY}C_1} \tag{1.4}$$

$$I_{PEAK} = \frac{V_C - V_F}{R + Z_0} \simeq \frac{V_C - V_F}{2}\sqrt{\frac{C_1}{L_{STRAY}}} \tag{1.5}$$

where V_C is the capacitor charging voltage, V_F is the laser diode forward voltage and $Z_0 = \sqrt{L_{STRAY}/C_1}$ is the characteristic impedance of the LC resonator [55]. After this point, the current pulse is terminated and the capacitor C_1 is totally discharged. The switch S_W is then turned off allowing the capacitor C_1 to be charged again for the next pulse. The supply voltage V_{IN}, which is roughly the capacitor charging voltage V_C, can be derived from Equations 1.4 and 1.5 to find

$$V_{IN} \simeq \frac{2L_{STRAY}}{t_{PWHM}} I_{PEAK} + V_F \tag{1.6}$$

In addition, the average power consumption P_{AVG} can be approximated according to [57] as

$$P_{AVG} \simeq \frac{T_{CONTROL}}{T_{PRF}} . \frac{V_{IN}^2}{R_1} + C_{TOT} V_{IN}^2 f_{PRF} \tag{1.7}$$

where $T_{CONTROL}$ is the pulse width of the control signal, f_{PRF} and T_{PRF} are the pulse repetition frequency and its corresponding period respectively and C_{TOT} accounts for the capacitor C_1 plus the output capacitance of the switch S_W. It seems this equation only considers the power consumption from the supply voltage V_{IN} and neglects the power drawn from the gate drive voltage.

Configuration 2 The operating principle for generating current pulses is similar to the one of configuration 1 described above, except that resistor R_2 in Figure 1.3a) is replaced by a clamping diode (D_{CLAMP} in Figure 1.3b). It prevents the laser diode from high reverse voltage during transients [56]. The capacitor C_1 is charged to the supply voltage V_{IN} through resistors R_1 and the diode D_{CLAMP} when the switch S_W is turned off. The charging time constant τ is now

$$\tau = (R_1 + R_D)C_1 \tag{1.8}$$

where R_D is the series resistance of the clamping diode. Pulse width and peak current of pulses are determined by using Equations 1.4 and 1.5. The supply voltage is also derived

from Equation 1.6.

Key waveforms of configuration 2 are similar to the ones of configuration 1, as illustrated in Figure 1.4.

Configuration 3 The operating principle for generating current pulses is similar to the one of configuration 1 and 2 described above, except that the capacitor C_1 is charged to the supply voltage V_{IN} through resistor R_1 when the switch S_W is turned off, as illustrated in Figure 1.3c). In this case, the charging time constant τ is

$$\tau = R_1 C_1 \tag{1.9}$$

Then, the capacitor C_1 discharges its energy through the load path as soon as the switch S_W is triggered by the control signal. Therefore, it generates a current pulse through the laser diode in the same way as configurations 1 and 2. Pulse width and peak current are determined by parameters of the RLC equivalent circuit formed by the capacitor C_1 and the equivalent series inductance and resistance in the load path. They are given by Equations 1.4 and 1.5 as well. An additional current provided by the voltage source may flow through the load path when the switch is still turned on. It remains however acceptable if the recharging time is far larger than the pulse width ($5\tau \gg t_{PWHM}$) [66]. A clamping diode may be added to protect the laser diode from turn-off ringing [62].

Key waveforms of configuration 3 are similar to the ones of configuration 1 and 2, as illustrated in Figure 1.4.

1.2.2 Advantages and limitations

The resonant capacitive discharge driver topology has many benefits [53][62]. First of all, this topology has a relatively simple design accepting the stray inductance into its operation. Then, the laser pulse energy is well controlled, thus eliminating thermal runaway and providing an improved pulse-to-pulse repeatability. In addition, the pulse width of the control signal applied to the driving circuitry can be longer than the current pulse width giving more flexibility for its design, especially about speed characteristics. The switch and its driving circuitry can also be ground-referenced simplifying the overall design.

A major drawback concerns the pulse width that depends on the capacitor and stray inductance, which are fixed for a given design, while the pulse amplitude depends on the supply voltage and the capacitor too. Therefore, it is impossible to control the pulse width and amplitude separately. Another issue is the long time needed to charge the capacitance thus limiting the PRF. Moreover, a relatively high supply voltage may be required to achieve a high peak current what may increase the design complexity, cost and space needed by the whole circuit. Furthermore, for configuration 1 and 2, it exists

a secondary current path from the power supply to the ground through the resistor R_1 and the switch when it is turned on, leading to a current leakage. Though, it remains acceptable if the recharging time is far larger than the pulse width as for configuration 3 [66].

1.2.3 Performance analysis

The various works described above present many results from demonstrators of capacitive discharge drivers. As several sets of measurements with various use cases have been performed by authors, only the most relevant results and design parameters are summarized in Table 1.3. It leads to a very diverse set of results and parameters.

Implementation Both discrete and integrated approaches are employed here. The discrete approach refers to the use of a discrete-type transistor for implementing the switch while the integrated approach refers to the use of a transistor directly embedded with its driving circuitry and other blocks into the same chip.

One advantage of the integrated approach is that a transistor has a smaller gate capacitance in contrast to a discrete-type transistor. Moreover, the gate driver can also be implemented on the chip thus increasing the switching speed [55]. The chip can also be directly bonded on a PCB or a ceramic substrate in order to minimize the stray inductance [56][57]. Even if the size of the overall system can be reduced, such as the demonstrator in [57] with a 6x12mm^2 size, it may increase the design complexity and cost. For that reason, the discrete approach seems to be largely adopted using various packages such as the Small Outline Transistor (SOT), Quad-Flat No-leads (QFN), Micro Lead frame Package (MLP) or Land Grid Array (LGA).

Technology Different technology solutions are employed here. For simplification, they are designated as follows: BJT for Bipolar Junction Transistor, CMOS for Complementary Metal Oxide Semiconductor, HV-CMOS for High-Voltage CMOS, MOSFET for Metal Oxide Semiconductor Field Effect Transistor and GaN FET for Gallium-Nitride Field Effect Transistor. No trend can be identified when considering the technology with respect to performance indicators. However, it can be seen that the CMOS technology is preferred for the integrated approach probably due to its high maturity. In addition, discrete-type GaN FET devices seem to be more frequently considered in recent years. It is probably because cost-effective GaN FETs have become commercially available with significantly lower inductance and better switching speed than silicon MOSFETs [66].

Transient indicators As discussed above, transient indicators depend on test conditions. For instance, current measurements are usually derived from voltage measurements across a resistive load, such as in [55][56], or by measuring a voltage drop over a damping or

shunt resistance in series with the laser diode such as in [57][59][60][62][63][65]. Therefore, it is complicated to compare demonstrators.

Nevertheless, it is noticed that the current pulse width increases as the capacitor value, confirming Equation 1.4. In Figure 1.5, the graph on the left plots the current pulse width versus the capacitor value in order to highlight this trend. A similar observation can be made with the optical pulse width instead of the current pulse width but only with demonstrators using commercially available laser diodes. For custom laser diodes, such as in [57][59][60], extremely short optical pulses are reported in the range of hundreds of ps. These outstanding transient performances are achieved thanks to a specific laser diode structure based on an enhanced gain switching principle [57]. In short, this principle refers to an operating mode where the gain in the laser is modulated by a short intense pulse resulting in the emission of a short optical pulse proportional in duration to the photon lifetime [68]. Although short and high-energy optical pulses can be generated with moderate requirements as to the properties of the current pulse of the driver, one drawback of this approach is the cost associated to the development of a custom laser diode.

In the same way, the graph on the right in Figure 1.5 plots the peak current versus the supply voltage parametrized with the capacitor value. It helps to see that the peak current increases with the supply voltage and capacitor value, confirming Equations 1.5 and 1.6. The same trend can be deduced considering the peak optical power instead of peak current.

Another important point is that pulse repetition frequencies reported in papers are less than tens of MHz, even with low capacitor values. This confirms a major limitation of this kind of driver topology.

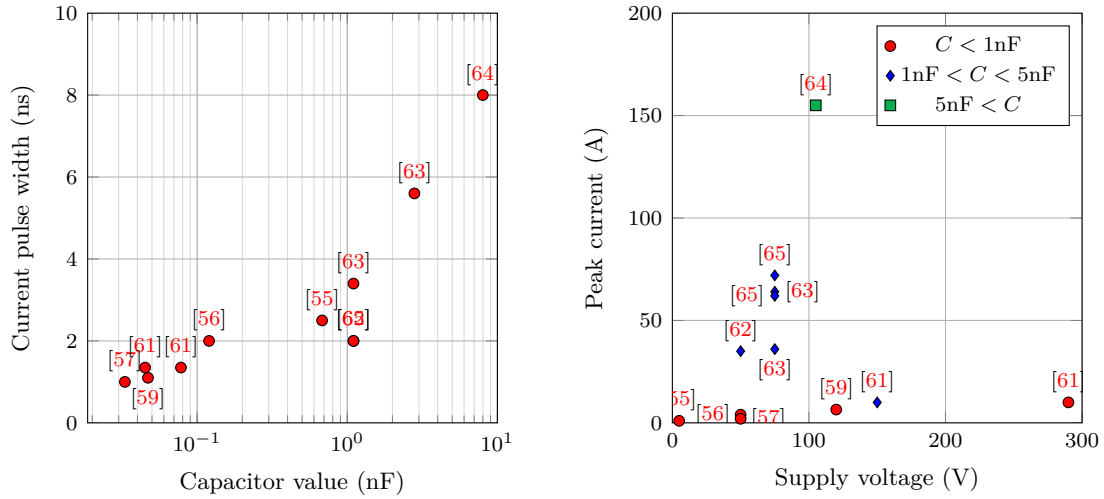


Figure 1.5 – Landscape graphs illustrating trends and trade-offs from relevant performance indicators and design parameters.

Power consumption Power consumption of demonstrators while operating is rarely reported in papers and there is no mention of power efficiency values at all. Whereas a formula is given in [57] in order to approximate the power consumption (see Equation 1.7), there is still a lack of data to estimate this value as well as the power efficiency of demonstrators. Therefore, it may indicate that power requirements are not a major concern for applications related to this kind of driver topology.

All these results are further discussed in Part 1.4 in order to select the most suitable topology with respect to targeted objectives.

Table 1.3 – Performance results of capacitive discharge driver circuits from literature.

Reference	[54] (1997)	[55] (2009)	[56] (2013)	[57] (2016)	[58] (2013)	[59] (2014)	[60] (2015)
Implementation	Discrete	Integrated	Integrated	Integrated	Discrete	Discrete	Discrete
Technology	BJT Zetex ZTX415	0.35µm CMOS	0.35µm 50V HV-CMOS	0.35µm HV-CMOS	MOSFET -	MOSFET Fairchild FDMC86244	MOSFET -
Chip or die size	-	1225x1248µm^2	3.3x2.2mm^2	3x4mm^2	-	-	-
Package size	SOT23 -	QFN24 4x4mm^2	Bonded on PCB -	Bonded on substrate -	-	MLP 3.3x3.3mm^2	-
Laser diode	Laser Diode Inc. LD65	Thorlabs L904P030	Perkin Elmer PGAS1S03H	Custom laser diode	-	Custom laser diode	Custom laser diode
Capacitor	1nF	680pF	120pF	33pF	320pF	47pF	-
Supply voltage	300V	5V	50V	50V	140V	120V	20V-150V
Gate drive voltage	-	3.3V	5.5V	5.5V	-	-	-
Pulse repetition frequency	-	10kHz	1MHz	500kHz	600kHz	100kHz	10kHz-1MHz
Current pulse width	-	2.5ns	2ns	1ns	-	1.1ns	~1ns
Peak current	-	1A	4A	2A	-	6.5A	<10A
Optical pulse width	~6ns	4.7ns	1.5ns	~100ps	4ns	125ps	~100ps
Peak optical power	20W	430mW	2.3W	3W	40W	~9W	<9W
Power consumption	-	-	300mW	175mW	-	-	-

Reference	[61] (2017)	[62] (2017)	[63] (2018)	[64] (2018)	[65] (2019)	[67] (2018)
Implementation	Discrete	Discrete	Discrete	Discrete	Discrete	Discrete
Technology	BJT / MOSFET Zetex FMMT415 / Fairchild FDMC86244	GaN FET EPC2016C	GaN FET EPC2016C / EPC2001C	GaN FET EPC2047	GaN FET EPC2016C	BJT Avalanche transistor
Chip or die size	-	-	-	-	-	
Package size	SOT23 / MLP 3x2.5mm^2 / 3.3x3.3mm^2	LGA 2.1x1.6mm^2	LGA 2.1x1.6mm^2 / 4.1x1.6mm^2	LGA 4.6x1.6mm^2	LGA 2.1x1.6mm^2	Bonded on substrate -
Laser diode	Commercial laser diode	OSRAM SPL PL90_3	Excelitas TPGAD1S09H	Excelitas TPGAD1S09H	Custom laser diodes: A / B	-
Capacitor	45pF / 78pF	1.1nF	1.1nF / 2.8nF	8nF	1.1nF	
Supply voltage	290V / 150V	50V	75V	105V	75V	140V
Gate drive voltage	-	5V	5V	-	5V	-
Pulse repetition frequency	-	10MHz	10MHz	10MHz	10MHz	10kHz
Current pulse width	~1.35ns	~2ns	3.4ns / 5.6ns	8ns	2.2ns / 2ns	-
Peak current	~10A	~35A	36A / 64A	155A	62A / 72A	-
Optical pulse width	~1.1ns	-	~3ns / ~5ns	~5ns	-	1.87ns
Peak optical power	~10W	-	-	-	-	50W
Power consumption	-	-	-	-		

1.3 Rectangular Pulse Driver Topologies

Driver circuits presented in [62][69][70][71][72][73][74][75][76][77] as well as in [78][79][80][81] are considered here as rectangular pulse drivers. Nevertheless, two types of driving mode can be distinguished:

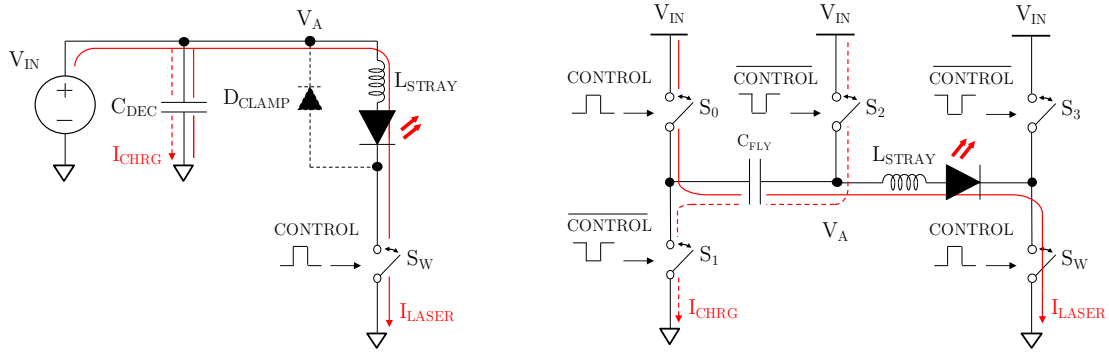
- The voltage-mode drivers are based on a voltage source for controlling the laser diode biasing.
- The current-mode drivers are based on a current source for controlling the laser diode biasing.

1.3.1 Voltage-mode driver

The driver topologies reported in [62][69][70][71][79] are considered here as voltage-mode drivers but rely on different operating principles. They can be divided into two configurations: series and switched capacitor.

1.3.1.1 Operating principle and properties

Schematics of both configurations are shown in Figure 1.6 in their basic versions for the sake of simplification. Their operating principles are described in the following.



(a) Series configuration ([62][69][79]).

(b) Switched capacitor-based (or voltage doubler) configuration ([70][71]).

Figure 1.6 – Simplified schematics of voltage-mode driver topologies.

Series configuration Key waveforms are illustrated in Figure 1.7. Basically, a voltage source V_{IN} is connected in series with a laser diode and a switch S_W, as proposed in [62] and [79]. This topology is similar to configuration 3 of capacitive discharge topology (see Figure 1.3c) except that capacitor C_1 is replaced by a large capacitor C_{DEC} acting as

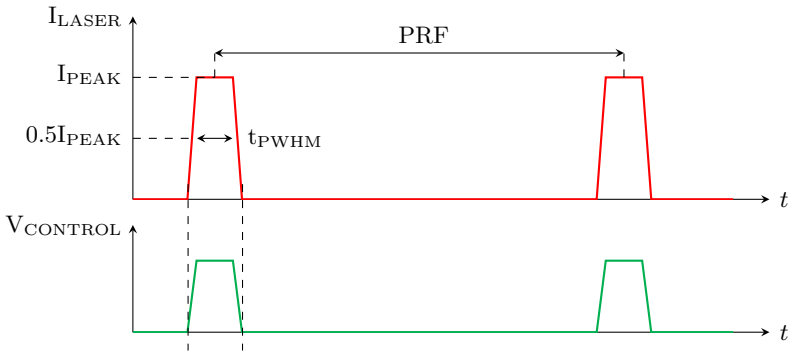


Figure 1.7 – Key waveforms for a voltage-mode driver in series configuration: laser diode current I_{LASER} (red), control signal $V_{CONTROL}$ (green).

a decoupling capacitor for the voltage source. Therefore, it stores a charge much larger than the one required for a current pulse [62]. Assuming a capacitor initially charged, a current pulse through the laser diode is initiated when the switch S_W is triggered by the control signal. The voltage source supplies a large portion of the current while the capacitor C_{DEC} ensures the current in response to fast transients. Then, the switch S_W is turned off according to the control signal, in order to cut off the current through the laser diode thus terminating the current pulse. A clamping diode may be added to protect the laser diode from turn-off ringing. The peak current value I_{PEAK} can be adjusted by controlling the anode voltage V_A expressed by

$$V_A = V_F + R_{SW} I_{PEAK} \tag{1.10}$$

where V_F is the laser diode forward voltage and R_{SW} is the series resistance of the switch. In [69], a boost Direct Current to Direct Current (DC/DC) converter, able to step-up the voltage, is proposed in order to adjust this anode voltage according to the input voltage to reach the desired laser diode current. Innovative control loops are implemented in order to ensure a constant peak current against voltage and temperature variations thus enhancing pulse-to-pulse reliability.

Switched capacitor-based configuration Key waveforms are illustrated in Figure 1.8. This configuration is based on the capacitive charge transfer between a capacitor C_{FLY} and a laser diode [70]. The operating principle is divided into two steps where switches S_0 and S_W are driven in phase by the control signal while switches S_1, S_2 and S_3 are driven in phase opposition. Firstly, switches S_0 and S_W are turned off while S_1 and S_2 are turned on in order to charge the capacitor C_{FLY} to the supply voltage V_{IN}. The charging time constant is

$$\tau = (R_1 + R_2) C_{FLY} \tag{1.11}$$

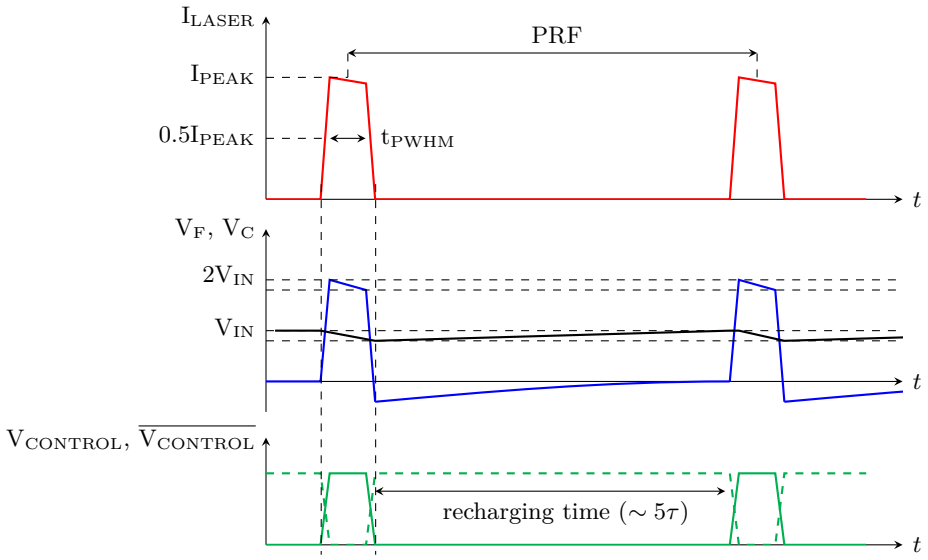


Figure 1.8 – Key waveforms for a voltage-mode driver in switched-capacitor based configuration: laser diode current I_{LASER} (red), laser diode forward voltage V_F (blue), voltage across the capacitor V_C (black), control signal $V_{CONTROL}$ (green), inverted control signal $\overline{V_{CONTROL}}$ (dashed green).

where R_1 and R_2 are the series resistances of switches S_1 and S_2 respectively. In the same time, switch S_3 is also turned on thus reverse-biasing the laser diode. Then, capacitor C_{FLY} discharges its energy through the load path as soon as switches S_0 and S_W are triggered by the control signal, while switches S_1, S_2 and S_3 are turned off. This initiates a current pulse through the laser diode that is now forward biased. Finally, switches S_0 and S_W are turned off according to the control signal in order to cut off the current through the laser diode thus terminating the current pulse. Switches S_1 and S_2 are turned on again for recharging capacitor C_{FLY}. Switch S_3 is turned on as well thus reverse-biasing the laser diode and ensuring a fast switch-off [71].

In this topology, the peak current value I_{PEAK} is controlled by the anode voltage V_A which is fixed due to the switch assembly S_0, S_1 and S_2 and the capacitor C_{FLY}. This capacitor must be large enough to prevent that the current drops during the whole pulse duration. The previous assembly can be seen as a switched-capacitor voltage doubler, thus the laser diode forward voltage V_F is given by

$$V_F = 2V_{IN} - (R_0 + R_{SW})I_{PEAK} \tag{1.12}$$

where R_0 and R_{SW} are the series resistances of switches S_0 and S_W respectively.

1.3.1.2 Advantages and limitations

The voltage-mode driver topology benefits from a control of the pulse width due to the inherent principle of rectangular pulse drivers [62]. High PRF can be reached due to the use of a relatively large decoupling capacitor which is only partially discharged between every pulses. Moreover, the peak current is independent of the pulse-width setting and only a control of the laser diode biasing voltage is required to adjust its value. These features allows flexible pulse sequences not depending on capacitor or parasitic inductance and resistance at first order. The switch S_W in Figures 1.6a and 1.6b and its driving circuitry can also be ground-referenced simplifying the design.

However at second order, the stray inductance is a major limitation. It must be taken into account in order to estimate the correct laser diode biasing. Usually, the supply voltage needs to be high enough to overcome this stray inductance as well as parasitic resistance. This is the case in [69] and [70][71] where a boost DC/DC converter or a switched-capacitor voltage doubler are included in the design. Furthermore, control loops may be required to ensure pulse-to-pulse repeatability due to temperature and voltage variations as described in [69]. An additional switch is also used in [70][71] in order to reverse-bias the laser diode and ensure a fast switch-off but it contributes to increase the power consumption due to an additional gate drive circuit. All these additional features may increase the design complexity, cost and space needed by the system.

1.3.1.3 Performance analysis

In contrast with capacitive discharge circuits reviewed earlier, few results are presented from voltage-mode driver circuits. Only the work in [69] presents performance results from a demonstrator while in [71] results are from post-layout simulations. The most relevant and recent results and design parameters are summarized in Table 1.4.

Implementation and technology Both discrete and integrated approaches are employed here with different technology solutions. In [69], the approach can be seen as semi-discrete. Indeed, the switch is implemented by using a discrete-type GaN FET device while its driving circuitry as well as the boost DC/DC converter with control loops are integrated into the same chip using a 55nm CMOS process. Although no further information is mentioned by authors, this specific approach could benefit from both the mature and low cost CMOS process for implementing the DC/DC converter Integrated Circuit (IC) and from the relatively cost-effective GaN FET process for implementing the switch capable of handling high current and voltage levels with an increased switching speed within a low inductance package.

On the other hand, a fully integrated approach is preferred in [70][71] implementing all switches as well as the capacitor C_{FLY}, the driving circuitry and other blocks onto the same chip using a 40nm CMOS process. This approach benefits from improved performances

and reduced size but at the expense of an increased design complexity and cost. It is also proposed to directly have the chip bonded on a substrate in order to minimize the stray inductance.

Transient indicators As explained before, transient indicators depend on test conditions. Although few information is provided in [69], the current measurement seems to derive from voltage measurements across a resistive load while an electro-optical model of a Vertical Cavity Surface Emitting Laser (VCSEL) diode (further discussed in Part 2.1.4) is used for simulation purpose in [71]. An important point to notice is that a current pulse width less than 1ns with a high pulse repetition frequency around 200MHz is reported in both articles. This highlights a major benefit of the voltage-mode driver topology where short current pulses can be achieved with a high PRF.

In [69], it seems that a high current amplitude (~28A) is obtained with a relatively high anode voltage (~10V) confirming Equation 1.10. In addition, the boost DC/DC converter with innovative control loops seems to demonstrate a good robustness against load variations where a constant 28A peak current is obtained whether a small or large resistive load is used.

Nevertheless, a low current amplitude (~230mA) is obtained in [71] even with a relatively high anode voltage (~5V). This could be explained by: the load characteristics, the voltage drops across switches, the significant impact of the stray inductance taken into account in simulations or the too small capacitor C_{FLY} that is not able to maintain the anode voltage level making the current to drop during the pulse.

Power consumption Power consumption and efficiency are reported in [71] only. It is thus quite complicated to contrast the figures since no data is provided in [69]. This may indicate that power requirements are also not a major concern for applications related to this kind of driver topology.

All these results are further discussed in Part 1.4 in order to select the most suitable topology with respect to targeted objectives.

1.3.2 Current-mode driver

The driver topologies reported in [72][73][74][75][76][77][78][79][80][81] are considered here as current-mode drivers but rely on different operating principles. They can be divided into two configurations: current limiter (CL for short) and shunt (SH for short).

1.3.2.1 Operating principle and properties

Current limiter configuration A similar operating principle is employed for circuits in [72][73][74][75][81]. However, slight differences are noticed leading to distinguish four

Table 1.4 – Performance results of voltage-mode driver circuits from literature.

Reference	[69] (2019)		[71] (2019 - PLS results)
Configuration	Series		Switched capacitor
Implementation	Semi-discrete		Integrated
Technology	GaN FET EPC2040	55nm CMOS Boost DC/DC converter IC	40nm CMOS
Chip or die size	-	1.85x1.96mm^2	0.32mm^2
Package size	LGA 1.2x0.8mm^2	-	Bonded on substrate (model) -
Laser diode	-		VCSEL diode (model)
Input voltage Anode voltage	5V 10V		2.5V 5V
Pulse repetition frequency	200MHz		200MHz
Current pulse width	900ps		460ps
Peak current	28A		230mA
Optical pulse width	-		~200ps
Peak optical power	-		~150mW
Power consumption	-		~110mW
Power efficiency	-		~50%

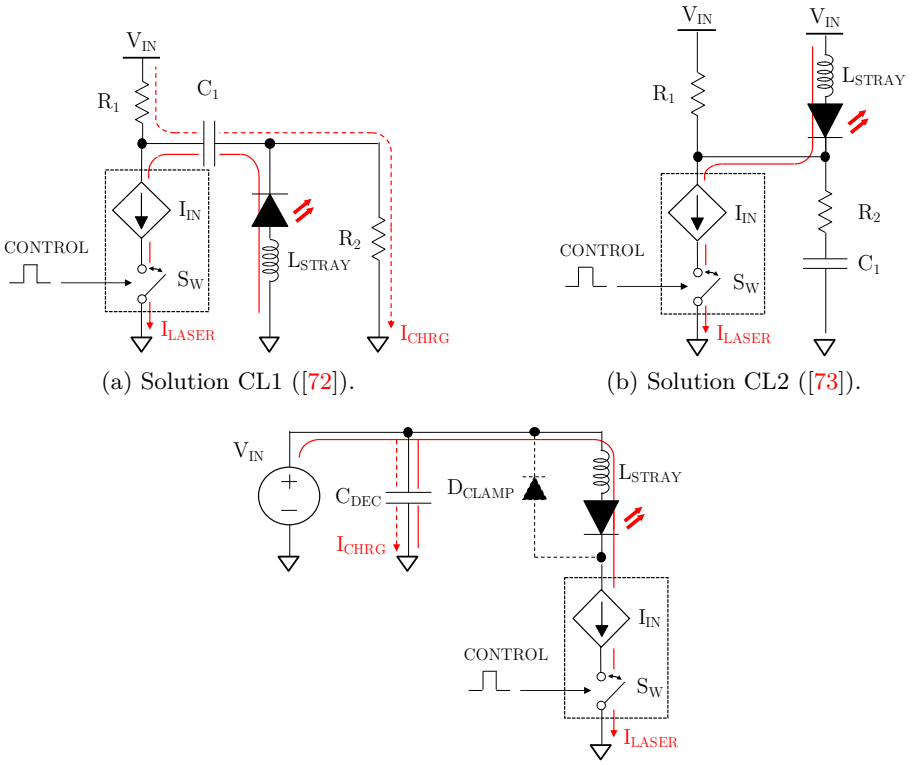
alternative solutions for the current limiter configuration. Schematics of various solutions are shown in Figure 1.9 in their basic versions for the sake of simplification. For all solutions, the controlled current source I_{IN} associated to the switch S_W can be seen as a current limiter. Operating principles are described in the following.

Solution CL1 Key waveforms are illustrated in Figure 1.10. This solution is similar to configuration 1 of the resonant capacitive discharge driver topology (see Figure 1.3a) except that a controlled current source I_{IN} is connected in series with the switch S_W in order to act as a current limiter. Firstly, it is turned off in order to charge the capacitor C_1 to the supply voltage V_{IN} through resistors R_1 and R_2. The charging time constant is

$$\tau = (R_1 + R_2)C_1 \tag{1.13}$$

The laser diode is reverse-biased during this phase. Then, the current limiter is triggered by the control signal initiating a current pulse through the laser diode that is now forward biased. As for resonant capacitive discharge drivers, the circuit behaves as a RLC-series circuit comprising the capacitor C_1 and the equivalent series inductance and resistance in the load path. This circuit can be oscillating or not depending on its damping ratio, approximated as

$$\zeta = \frac{R}{2}\sqrt{\frac{C_1}{L}} \tag{1.14}$$



(a) Solution CL1 ([72]).

(b) Solution CL2 ([73]).

(c) Solution CL3 and CL4 ([75][74][81]).

Figure 1.9 – Simplified schematics of various solutions using a current-mode driver topology in CL configuration.

where usually, L is the stray inductance L_{STRAY} and R accounts for the series resistance of the laser diode and switch. In this topology, it is assumed that the RLC circuit is designed to be oscillating during a brief moment after the pulse initiation leading to a fast rising time. Then, the current limiter allows to limit the current amplitude of the pulse and keep it constant during the whole pulse duration [72]. The capacitor C_1 must be large enough to prevent that the current drops during the pulse. The current limiter is finally turned off according to the control signal, in order to cut off the current through the laser diode thus terminating the current pulse. The peak current I_{PEAK} can be limited by controlling the current provided by the controlled current source I_{IN}. In addition, the supply voltage V_{IN} must be high enough to overcome the stray inductance and parasitic resistance, given by

$$V_{IN} \simeq \frac{L_{STRAY}}{t_{PWHM}} I_{PEAK} + V_F + R.I_{PEAK} \tag{1.15}$$

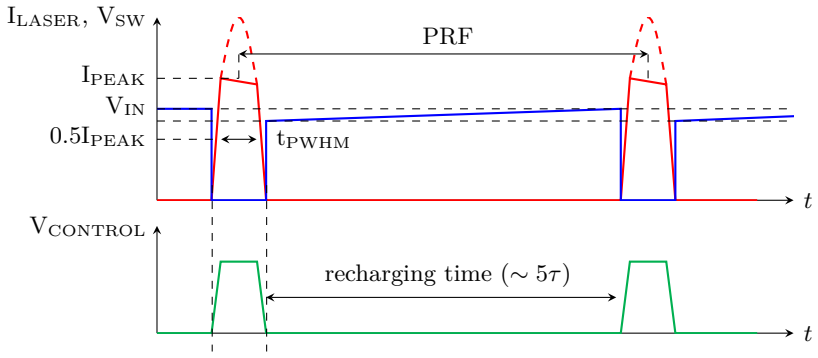


Figure 1.10 – Key waveforms for solution CL1 of current-mode driver in current limiter configuration: laser diode current I_{LASER} (red), voltage across the current limiter V_{SW} (blue), control signal $V_{CONTROL}$ (green). The red dashed curve represents the current pulse shape if the current is not limited by the current limiter.

where t_{PWHM} is the current pulse width, V_F is the laser diode forward voltage and R is the parasitic resistance in the load path. In [82], it seems that an integrated switched capacitor DC-DC converter based on a Dickson type implementation is proposed in order to provide the supply voltage V_{IN} of the current-mode driver circuit proposed in [72]. The operating principle of the converter is not detailed here, more information can be found in [82].

Solution CL2 In contrast with solution CL1 where a coupling capacitor is used, this solution proposes to directly connect the laser diode to a current limiter formed by the controlled current source I_{IN} and the switch S_W. A current pulse through the laser diode is initiated when the current limiter is triggered by the control signal. Then, it is turned off according to the control signal in order to cut off the current through the laser diode thus terminating the current pulse. The peak current I_{PEAK} is controlled by the controlled current source I_{IN}. The supply voltage V_{IN} is assumed to be high enough to overcome the stray inductance and parasitic resistance as for solution CL1 (see Equation 1.15).

According to [73], a resistor R_1 is placed in parallel to the laser diode in order to decrease the rising time of the current pulse. This resistor acts as a pull-up resistor shorting the laser diode when the current limiter is off. This seems to preserve the turn-on delay of the laser diode which is an inherent delay between the electrical and optical pulses [83] (further discussed in Part 3.2.3). The authors claim that the stray inductance L_{STRAY} can be pre-charged during this delay making the current rises faster. Moreover, a resistor R_2 and a capacitor C_1 are added in parallel to the current limiter but there is no information provided by authors about their functions.

Key waveforms for solution CL2 are similar to the ones of the voltage-mode driver topology

in series configuration as illustrated in Figure 1.7.

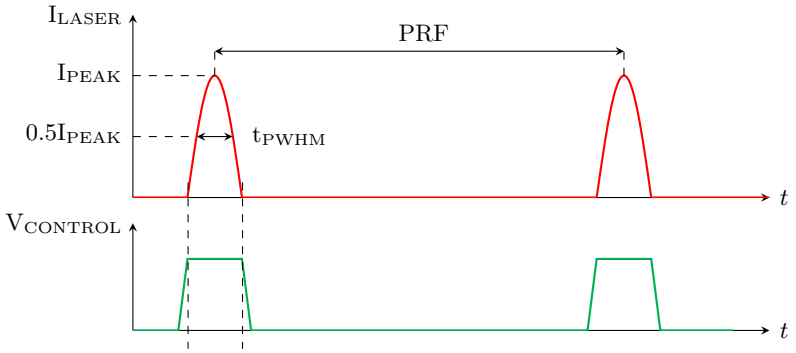


Figure 1.11 – Key waveforms for solution CL3 of current-mode driver in current limiter configuration: laser diode current I_{LASER} (red), control signal $V_{CONTROL}$ (green).

Solution CL3 Key waveforms are illustrated in Figure 1.11. This solution is similar to configuration 3 of the resonant capacitive discharge driver topology (see Figure 1.3c) except that a controlled current source I_{IN} is connected in series with the switch S_W in order to act as a current limiter and the capacitor C_1 is replaced by a large capacitor C_{DEC} acting as a decoupling capacitor for the voltage source. Assuming the decoupling capacitor C_{DEC} initially charged, a current pulse through the laser diode is initiated when the current limiter is triggered by the control signal. At this point and in contrast with resonant capacitive discharge drivers, the circuit behaves as a RLC-parallel circuit comprising the equivalent series inductance in the load path and the equivalent output capacitance and resistance of the current limiter. This circuit can be oscillating or not depending on its damping ratio, approximated as

$$\zeta = \frac{1}{2R_P}\sqrt{\frac{L_P}{C_P}} \tag{1.16}$$

where L_P is usually the stray inductance L_{STRAY} and R_P and C_P are the equivalent output capacitance and resistance of the current limiter respectively [75]. In this topology, it is assumed that the RLC circuit is designed to be strongly oscillating (strong under-damped response) causing overshoots after the rising phase of the current. The current limiter is then turned off, according to the control signal, right after the first peak to quench the secondary overshoots [75]. A clamping diode is thus required here to protect the laser diode from turn-off ringing. As for capacitive discharge drivers, the current pulse width is determined by the parameters of the RLC equivalent circuit but the peak current value is made independent of these parameters by minimizing the damping factor [75]. The latter requirement is obtained by increasing the output impedance of the controlled current source I_{IN}. The current through the load path is roughly described by a half-cycle

of a sine wave with a resonance frequency f_0 given by

$$f_0 = \frac{1}{2\pi\sqrt{L_{STRAY}C_P}} \tag{1.17}$$

The current pulse width t_{PWHM} and the peak current I_{PEAK} can be approximated as

$$t_{PWHM} \simeq \frac{1}{2f_0\sqrt{1-\zeta^2}} \tag{1.18}$$

$$I_{PEAK} \simeq 2I_0 \tag{1.19}$$

where I_0 is the current provided by the controlled current source I_{IN}. The supply voltage V_{IN} must be high enough to overcome the stray inductance and parasitic resistance and to make the current generator work in proper operation region during the rising phase. It is given by

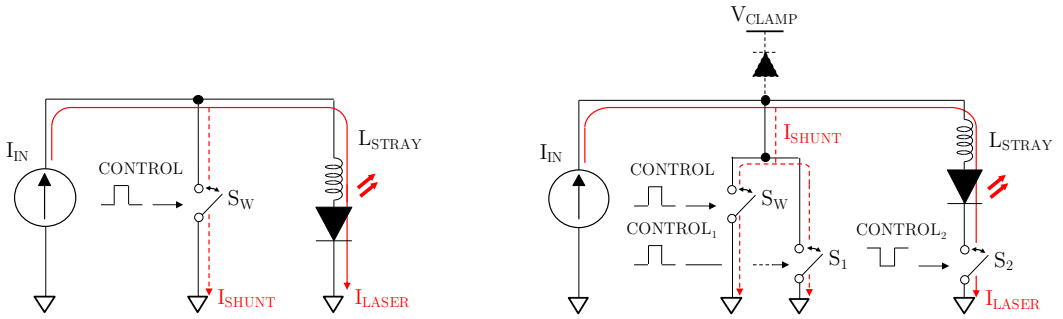
$$V_{IN} \simeq \frac{L_{STRAY}}{t_{PWHM}} I_{PEAK} + V_F + V_{SAT} + R.I_{PEAK} \tag{1.20}$$

where , V_F is the laser diode forward voltage, V_{SAT} is a sufficient voltage margin to bias the current generator and R is the parasitic resistance in the load path.

Solution CL4 In contrast with solution CL3 where the current pulse characteristics rely partly on the parameters of the RLC equivalent circuit, this solution proposes to directly use the current limiter for controlling current pulse characteristics such as pulse width and peak value, roughly as for solution CL1. Assuming a decoupling capacitor C_{DEC} initially charged, a current pulse through the laser diode is generated when the current limiter is turned on and off according to the control signal. The peak current I_{PEAK} is controlled by the controlled current source I_{IN}. The supply voltage V_{IN} is assumed be high enough to overcome the stray inductance and parasitic resistance and to make the current generator work in its proper operation region, as for solution CL3 (see Equation 1.20).

Key waveforms for solution CL4 are similar to the ones of the voltage-mode driver topology in series configuration as illustrated in Figure 1.7.

Shunt configuration Two alternative solutions can be distinguished for the shunt configuration from works described in [76][77][78][79][80]. The main difference lies in the use of additional switches. Schematics of various solutions are shown in Figure 1.12 in their basic versions for the sake of simplification. Operating principles are described in the following.



(a) Solution SH1 ([78][79][80]). (b) Solution SH2 ([76][77]).

Figure 1.12 – Simplified schematics of various solutions using a current-mode driver topology in SH configuration.

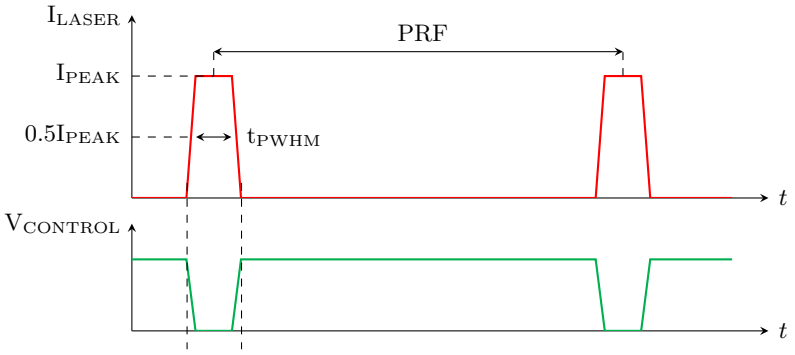


Figure 1.13 – Key waveforms for solution SH1 of current-mode driver in shunt configuration: laser diode current I_{LASER} (red), control signal $V_{CONTROL}$ (green).

Solution SH1 Key waveforms are illustrated in Figure 1.13. Basically, a current source I_{IN} is connected to a laser diode with a switch S_W in parallel, as proposed in [79][80]. The operating principle is divided into two steps. Firstly, the switch S_W is turned on for shunting the current from the current source I_{IN} to the ground thus shorting the laser diode. Then, it is turned off according to the control signal in order to initiate a current pulse from the current source I_{IN} to the laser diode. Finally, the switch S_W is turned on again by the control signal in order to shunt the current to the ground thus terminating the current pulse through the laser diode. The peak current I_{PEAK} can be adjusted by controlling the current provided by the current source I_{IN}.

In [78], the current source is implemented by connecting a power supply to a power inductor thus benefiting from its high output impedance. A power-distribution switch is placed between the power supply and the inductor for limiting the maximum current. In [80], a modified buck DC/DC converter is proposed as a current source in order to provide

a programmable current to the laser diode (further discussed in Part 2.4.3).

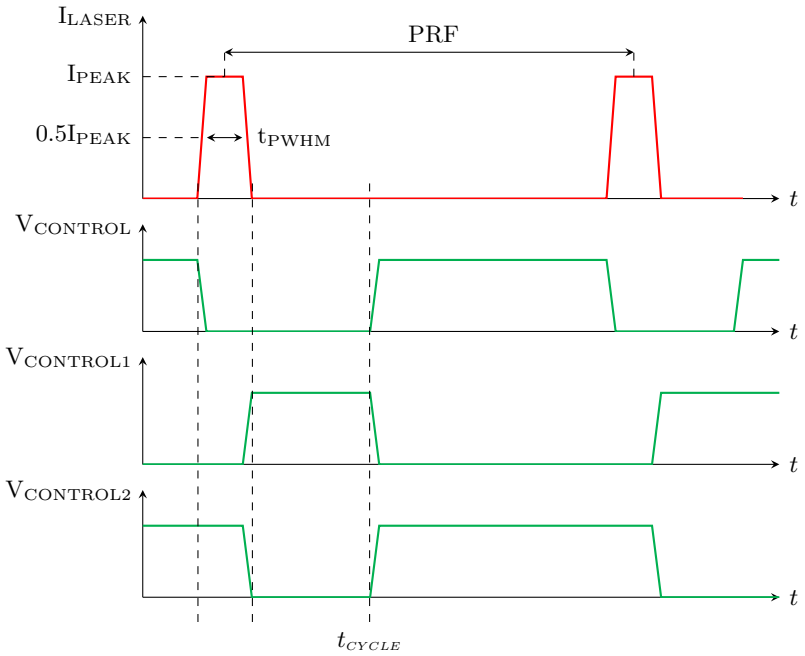


Figure 1.14 – Key waveforms for solution SH2 of current-mode driver in shunt configuration: laser diode current I_{LASER} (red), control signal $V_{CONTROL}$ (green).

Solution SH2 Key waveforms are illustrated in Figure 1.14. This solution is similar to solution SH1 except that a switch S_1 is connected in parallel to the switch S_W and a switch S_2 is connected in series with the laser diode. The operating principle is also divided into two steps where switches S_W, S_1 and S_2 are driven by independent control signals. Firstly, the switch S_W is turned on for shunting the current from the current source I_{IN} to the ground while switches S_1 and S_2 are turned off and on respectively. At this point, the laser diode is shorted. Then, the switch S_W is turned off according to its control signal in order to initiate a current pulse from the current source I_{IN}. Finally, switches S_1 and S_2 are simultaneously turned on and off by their control signals respectively in order to shunt the current to the ground again thus terminating the current pulse through the laser diode. A clamping diode may be added to protect the laser diode from turn-off ringing and avoid any failure risks of the driver circuit [76][77]. Depending on the pulsing sequence, switches S_W, S_1 and S_2 can be turned on, off and on respectively making the circuit operate in idle state and thus starting a new cycle (at t_{CYCLE} in Figure 1.14). The peak current I_{PEAK} can be adjusted by controlling the current provided by the current source I_{IN}.

In [76][77], a half-bridge synchronous rectifier feeding a power inductor is employed as a current source in order to provide a programmable constant current to the laser diode

(further discussed in Part 2.4.3). A voltage rail V_{CLAMP} is also provided for the additional clamping diode.

1.3.2.2 Advantages and limitations

The current-mode driver topology has different advantages and limitations depending on the configuration. Nevertheless, this topology benefits from a control of the pulse width for both current limiter and shunt configurations, except for solution CL3 where the current pulse width still depends on parameters of the RLC equivalent circuit. The peak current value is also configurable by means of a control on the laser diode biasing current only. Therefore, for most configurations and as for the voltage-mode driver topology, flexible pulse sequences can be achieved with a high PRF not depending on capacitor or parasitic inductance and resistance at first order. In addition, all switches with their driving circuitry can be ground-referenced simplifying the design.

However at second order, a major limitation of the current limiter configuration concerns the relatively high supply voltage required to overcome stray inductance and parasitic resistance. Hence, an additional circuit may be necessary to provide the correct supply voltage to the driver such as in [72][82]. About the shunt configuration, the complexity could come from the implementation of the current source where ideal current sourcing is not a feasible practice [77]. Moreover, control loops may be required as well to ensure pulse-to-pulse repeatability due to temperature and voltage variations, as described in [74] where a system including two Phase-Locked Loop (PLL) blocks is used for compensating the effect of Process, Voltage and Temperature (PVT) variations on current pulses. These additional features may increase the design complexity, cost and space needed by the system.

Another major drawback of the current limiter configuration is the relatively high dissipated power through the current limiter when turned on due to the sufficient voltage margin required for its proper biasing, such as in [74] where at least 2V is needed. In [73], despite no information is provided by authors, it seems that resistor R_2 and capacitor C_1 may only contribute to slow the current limiter. In addition, it exists a secondary current path from the power supply to the ground through the resistor R_1 and current limiter when it is turned on, leading to a current leakage. But the leakage may remain acceptable if the period of the pulse repetition is far larger than the pulse width, as for the resonant capacitive discharge driver topology [66]. Finally, whereas several switches are used for solution SH2 allowing a more precise control of the current pulse width compared to solution SH1, it contributes to increase the power consumption and chip size due to additional gate drive circuits.

1.3.2.3 Performance analysis

Some of the works described above present results from demonstrators or post-layout simulations. The most relevant and recent results and design parameters are summarized in Table 1.5. It can be noticed that only the work in [77] presents results for the shunt configuration. The other works are about the current limiter configuration.

Implementation It can be firstly noticed that all current-mode driver circuits consider an integrated approach benefiting from a higher switching speed compared to a discrete approach [72]. In addition, the circuits can be directly bonded on a PCB or using specific packaging techniques such as a soldered-bump flipped-chip Ball Grid Array (BGA) package in order to minimize the stray inductance [74][75].

Technology Different technology solutions are employed here. The CMOS technology seems to be relatively well adopted due to its maturity and low cost, although a more expensive 80V CMOS process is used in [72] where an n-type Diffused MOSFET (DMOS) device is implemented as a switch. On the contrary, a Bipolar-CMOS-DMOS (BCD) technology seems to be preferred when relatively high voltage and current levels are required such as in [75] or in [76][77] where customized n-type Lateral DMOS (LDMOS) power devices are designed with a 18V avalanche breakdown voltage for supporting currents up to 20A.

Transient indicators As already discussed, transient indicators depend on test conditions. Current measurements seems to derive from various methods such as using current probes acting as transformer in [72], average measurements from power supply in [73] or voltage measurements across a resistive load in [74]. Simulation results are obtained with a resistive load in [75] and no information is clearly mentioned in [77] thus results must be considered with caution.

It can be firstly noticed that various current pulse width and amplitude values are reported but with a relatively high PRF from tens to hundreds of MHz. This highlights a good advantage of the current-mode driver topology where a high PRF can be achieved but where pulse characteristics greatly depend on the configuration. For instance, results in [72] show high current pulses with a programmable pulse width while in [75] results show current pulses with a programmable amplitude but a fixed pulse width, confirming Equation 1.18. Although a short current pulse around 1ns is reported in [75], it must be specified that an additional programmable current source is also embedded in order to bias the laser diode above its threshold current to improve its response time by reducing the turn-on delay. The impact of this feature on the optical pulse shape is not demonstrated though. In [74], short current pulses with configurable pulse width and amplitude are reported, proving the flexibility of this solution. Even extremely short optical pulses are achieved with the use of an Edge-Emitting Laser (EEL) diode (further discussed in

Part 2.1.4) by isolating the gain-switching spike, as described in Part 1.2.3. Nevertheless, authors also recommend that the duration of the pulse must be configured to allow stabilization after switching off and proper heat dissipation at high PRF [74].

It is also seen that the maximum achievable peak current increases with the supply voltage for drivers in current limiter configuration, confirming Equations 1.15 and 1.20. On the other hand, short current pulses with a relatively high peak current of 5A are reported for the current-mode driver in shunt configuration by using a relatively low supply voltage of 5V for powering the driver [77]. This highlights a good benefit of the shunt configuration.

Power consumption Power consumption metrics are only reported in [72][74] but it is quite complicated to contrast the figures since they are not obtained in same conditions. It seems that power requirements are also not a major concern for applications related to this kind of driver topology.

In [74], it must be specified that the 1.8V power supply used for the current limiter is generated by an internal Low Dropout (LDO) regulator from the 5.5V power supply. Moreover, results provided by the authors do not consider the consumption from the 5.5V power supply used for biasing the laser diode. Therefore, the power consumption that is mentioned is roughly proportional to switching losses, increasing with the frequency.

Finally, the programmable current source used in [75] for biasing the laser diode above its threshold contributes to increase the power consumption but it remains acceptable if it is applied just before the main pulse. It is however at the expense of the design complexity since very short times are involved here.

All these results are further discussed in Part 1.4 in order to select the most suitable topology with respect to targeted objectives.

Table 1.5 – Performance results of current-mode driver circuits from literature.

Reference	[72] (2009)	[73] (2018)	[74] (2018)	[75] (2018 - PLS results)	[77] (2019)
Configuration	Current limiter				Shunt
Implementation	Integrated	Integrated	Integrated	Integrated	Integrated
Technology	0.35µm 80V CMOS n-DMOS	0.18µm CMOS	0.18µm CMOS	160nm BCD	0.18µm BCD n-LDMOS (18V)
Chip or die size	1x2mm^2	-	-	2.76x2.76mm^2	1.6x1.6mm^2
Package size	Bonded on PCB -	-	Bonded on PCB -	BGA (model) -	Soldered on PCB -
Laser diode	OSRAM SPLPL85	Vertilite 850nm 1W VCSEL Array	Axcel Photonics 808nm 200mW EEL	-	Excelitas PGAS1S03H
Supply voltage	70V	3.3V	5.5V	~50V	5V
Gate drive voltage	12V / 3.3V	3.3V	1.8V	-	5V
Pulse repetition frequency	-	100MHz	DC-200MHz	40MHz	20MHz
Current pulse width	10ns-50ns	5ns	~500ps - 2.5ns	1ns	5ns
Peak current	~10A	0.5A-2.2A	200mA-500mA	6A-20A	5A
Optical pulse width	-	~5ns	~100ps - 2.5ns	-	~5ns
Peak optical power	-	-	~50mW - ~250mW	-	-
Power consumption	~600mW	-	~20mW - ~100mW	-	-

1.4 Discussion and Conclusion

Using the direct modulation method, the LDD should be capable of generating short current pulses of high amplitude with a high PRF. The peak current should be configurable up to few Amps to deal with laser diode characteristics and to keep some design flexibility. The PRF should be programmable as well from tens to hundreds of MHz to fulfill iToF requirements. Assuming a 50% modulation duty cycle, it leads to generate current pulses from few ns to tens of ns. In addition, it must be reminded that the input voltage range is limited, typically from 2.8V up to 4.2V, and the power efficiency is considered as a leading requirement to achieve. It has been seen that it exists several driver topologies able to provide short and high current pulses, such as the resonant capacitive discharge driver topology as well as the voltage-mode and current-mode driver topologies using various configurations. They can be summarized using the classification shown in Figure 1.15.

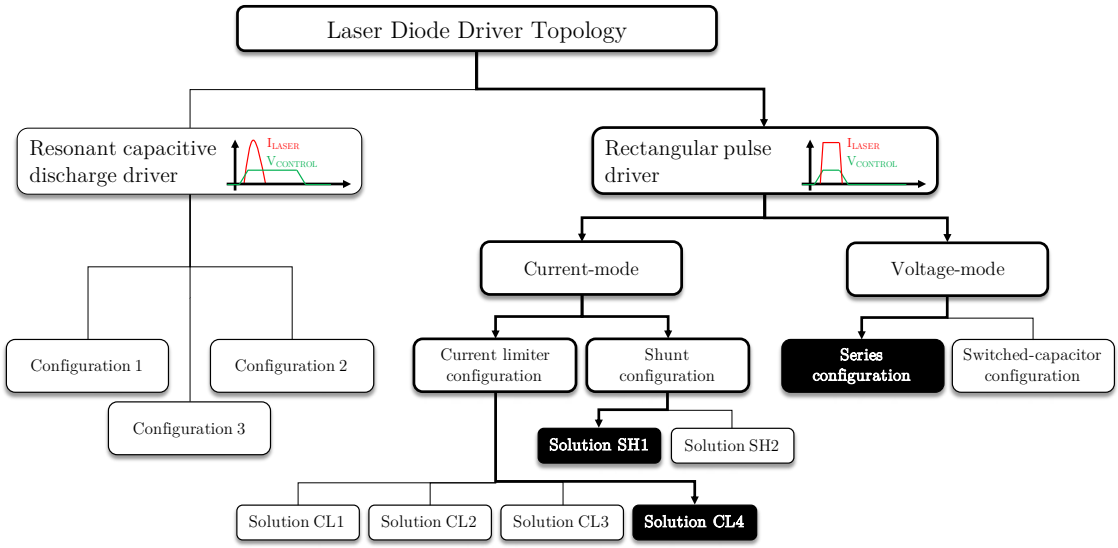


Figure 1.15 – Classification of laser diode driver topologies for ToF applications, with a focus on most suitable solutions in the thesis context.

The resonant capacitive discharge driver topology is quite popular due to its relatively simple design accepting the stray inductance. But the dependency of pulse characteristics on parameters of the RLC equivalent circuit and the supply voltage make this approach limited with respect to targeted objectives. Indeed, it is impossible to control the pulse width and amplitude separately. A flexible PRF seems not either easily achievable as it is fixed by the capacitor recharging time. For theses reasons, this topology is not suitable for designing the laser diode driver.

Regarding rectangular pulse driver topologies with all alternatives described above, the discussion is more complicated. One significant advantage for both voltage and current driving modes is the pulse width control allowing more flexibility. Therefore, for most configurations, flexible pulse sequences can be achieved with a high PRF not depending on parameter of the RLC equivalent circuit at first order. Nonetheless, it is not the case for solution CL3 where the pulse width is still determined by RLC circuit parameters, making this solution unsuitable. Among other solutions in current limiter configuration, which use a similar operating principle, solution CL4 seems a good candidate since no pull-up resistor is employed which could lead to a larger power dissipation in solution CL1 and CL2. Moreover, the function of an additional resistor and capacitor in solution CL2 is not clearly stated what makes this approach more questionable.

On the other hand, a significant drawback for this current limiter configuration as well as for voltage-mode driver topologies is the relatively high supply voltage required to overcome parasitic elements. For that reason, the current-mode driver topology in shunt configuration could be a potential solution for the laser diode driver. Due to the relatively complex and more consuming switch assembly required by solution SH2, solution SH1 could be preferred.

Considering now voltage-mode driver topologies, the switched capacitor-based configuration is less flexible than the series configuration due to the inherent structure of the switched-capacitor voltage doubler. Indeed, this architecture is intended to provide a constant voltage that is twice the supply voltage thus setting the laser diode biasing voltage and the peak current value. The series configuration could be a more versatile solution allowing to implement a suitable architecture to adjust the laser diode biasing voltage according to the desired current.

As a summary, the voltage-mode driver in series configuration as well as solutions CL4 and SH1 of the current-mode driver seem to be good candidates for the laser diode driver. However, even if the solution CL4 may involve a higher power dissipation than other solutions due to the sufficient voltage margin required for the current generator biasing, too few results in terms of transient performances, power metrics and functionality are provided from literature to conclude on these topologies regarding targeted objectives. The circuits considered in the state-of-the-art review are mostly intended for LiDAR applications where constraints in term of power losses are more flexible than for mobile applications and the technologies used might also be specific and incompatible with a low cost requirement.

At last and as a consequence, it is essential to carry out a preliminary design study for evaluating the feasibility of these three solutions with respect to the targeted objectives using a suitable technology. This study will primarily focus on the feasibility of integrating the laser diode driver on a single chip while accommodating mobile phone constraints and considering the power efficiency as a leading requirement. The three solutions that are concerned in this context are:

- The voltage-mode driver in series configuration (see Figure 1.6a and further discussed in Part 2.3).
- The current-mode driver in shunt configuration (corresponding to solution SH1, see Figure 1.12a and further discussed in Part 2.4).
- The current-mode driver in current limiter configuration (corresponding to solution CL4, see Figure 1.9c and further discussed in Part 2.5).

2 Preliminary Design Study

Contents

This chapter presents a preliminary design study for evaluating the feasibility of several driver architectures. They are based on the state-of-the-art topologies described in the previous chapter (see Chapter 1). Operating conditions and specifications for the laser diode driver are further detailed. The basic principle of each topology is explained before to carry out transient analysis of waveforms. For this purpose, simple simulations with device models from a STMicroelectronics' 130nm CMOS technology are performed in order to identify key features and highlight pros and cons of each solution. A comparative analysis using several Key Performance Indicators (KPIs) is then proposed. The most suitable solution with respect to the specifications will be used as the basis for designing the laser diode driver prototype.

2.1 Specifications of the Laser Diode Driver

This section details the operating conditions and specifications for the laser diode driver. They arise from major requirements considered for developing the iToF-based 3D image sensor (see the General Introduction).

2.1.1 Operating conditions

The laser diode driver is intended for hand-held consumer electronics. Since a commercial-grade product is considered, a maximum ambient temperature range from 0°C up to 70°C is required to ensure a proper operation of the device [84]. Li-ion batteries are commonly used in these mobile applications where the supply voltage typically varies from 2.8V up to 4.2V [42][43]. Assuming a worst-case scenario, it has been decided to consider here a supply voltage range from 2.5V up to 4.8V.

Thereafter, typical operating conditions will refer to an ambient temperature of 27°C and a supply voltage of 3.6V (corresponding to the nominal cell voltage of Li-ion batteries).

2.1.2 Modulation type and optical power budget

As explained in the General Introduction and Appendix A, short optical pulses with a duty cycle close to 50% are sent through the scene as a modulated signal, corresponding to the CW modulation. A high optical power as well as a high modulation frequency are desired to improve the depth resolution (see Equation A.17). Depending on the maximum targeting range, lighting conditions, objects reflectivity, sensor efficiency and eye-safety standards, optical pulses up to 2.5W for a modulation frequency from 50MHz up to 200MHz have been established for reaching a 3m maximum depth with a resolution better than 0.5% of depth.

2.1.3 Illumination pattern

A specific illumination pattern based on multiple pulse trains and idle times is needed by the iToF-based image sensor to acquire data and provide a complete depth map. Depending on general requirements and eye-safety standards, an illumination cycle (one pulse train followed by an idle time) is fixed to a 3ms period with a maximum illumination time of 1ms and a minimum off-time of 2ms. A typical 33% illumination duty cycle can be considered. An illustration of an illumination pattern is shown in Figure 2.1.

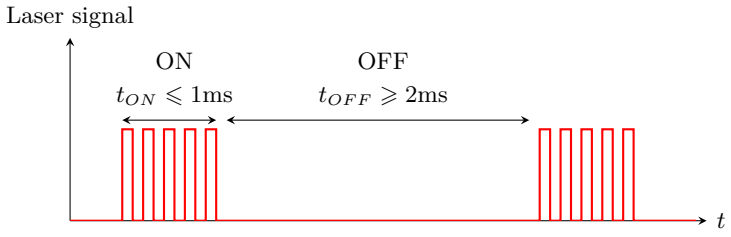
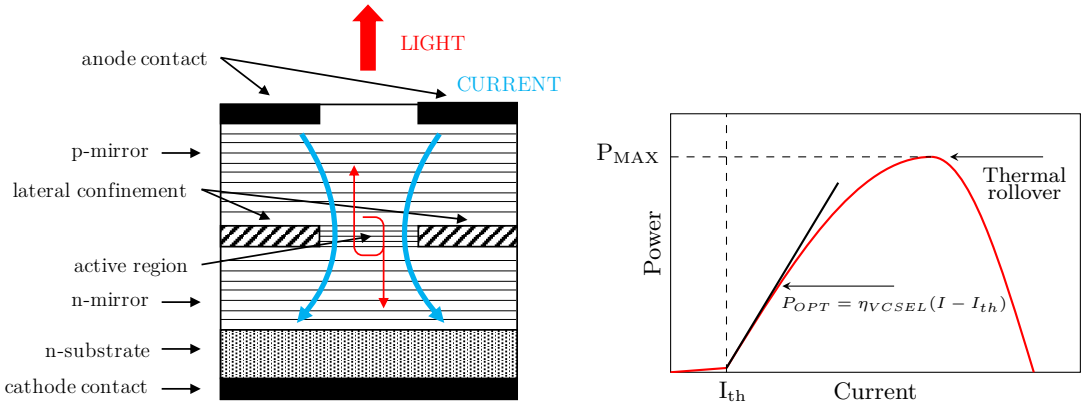


Figure 2.1 – Illustration of an illumination pattern.

2.1.4 Choice of the laser diode

Two types of semiconductor laser diodes are widely used in electronics: the EEL diode, referring to the conventional laser diode in the literature and the VCSEL diode [85]. An important feature of VCSELs is that the light is emitted from the surface of semiconductor layers compared to EELs where the light is emitted from the edge of semiconductor layers. VCSELs feature many other benefits against EELs, such as a wide bandwidth, a high quality laser beam or a low manufacturing cost, making them very attractive for illumination applications [86][87][47]. VCSEL device structure and output characteristic are quickly described in the following.



(a) Typical top-emitting VCSEL structure

(b) Typical output DC characteristic.

Figure 2.2 – Operating principle of a VCSEL [88].

Device structure A typical VCSEL cross-section is depicted in Figure 2.2a where the light is emitted from the top of semiconductor layers (top-emitting structure) [88]. Charge carriers are injected from anode and cathode contacts to be recombined into photons within the active region, which is located in the middle of the structure. The optical cavity is formed by two mirrors distributed on both sides of the active region. The reflectivity of mirrors must be high enough so that photons can go back and forth through the active region in order to amplify the light, allowing the lasing process to occur. For top-emitting structures, the VCSEL is designed for an emission through a ring contact. To ensure an efficient process, n-doped and p-doped semiconductor mirrors as well as a lateral confinement are used to create a vertical current and photons flow centered around the active layer. Finally, a n-type substrate is usually preferred over a p-type due to the lower concentration of defects.

More information about the VCSEL structure can be found in [88][89][90].

Output characteristic A typical output characteristic curve under DC conditions is plotted in Figure 2.2b. It represents the output optical power versus injected current. Below the threshold current I_{th}, the device operates under spontaneous emissions where the output optical power is very low, in the order of µW [90]. The device starts lasing above the threshold, thus operating under stimulated emissions where the output optical power P_{OPT} has a constant slope and is described by

$$P_{OPT} = \eta_{VCSEL}(I - I_{th}) \tag{2.1}$$

where η_{VCSEL} is the slope referring to the slope efficiency and I is the injected current. For high injected currents, the curve shows a characteristic rollover due to internal heating, leading to the extinction of the lasing process.

Since an individual VCSEL device is limited in term of output power, in the order of few tens of mW, monolithic 2D arrays of VCSEL devices are realized in order to deliver scalable output power from few mW to several W [91][92]. This important feature is made possible due to its inherent structure. The individual VCSELs in the array share the same electrodes and are thermally connected. All laser properties remain unchanged what means that a VCSEL array can be considered as a big VCSEL device [48]. In addition, the interference effect which arises from all individual VCSEL devices is very weak resulting in a speckle-free image quality [47]. Other benefits such as redundancy and low failure rates enabled by the large number of individual devices, make the VCSEL an ideal light source for ToF sensors. [48].

A top-emitting high-power VCSEL array module has been chosen to meet low cost and compact constraints. It is packaged into a 3.5x3.5x1.6mm custom ceramic package. A simplified cross-section of the VCSEL module is illustrated in Figure 2.3. Bond wires are used to connect the anode contact from the top of the die to a metallic ring plate surrounding the die. This interconnection plate is then connected to the external anode pad using Vertical Interconnect Accesss (VIAs). In the same way, the cathode contact from the bottom of the die lies on an interconnection plate connected to the external cathode pad using VIAs. These specific features introduce some parasitic elements such as a parasitic inductance L_{PKG} due to the bond wires as well as parasitic capacitances C_{PKG} and C_{PADS} due to anode and cathode contacts and pads respectively (further discussed in Part 2.1.5).

Finally, the package also includes a diffuser to homogenize and tailor the intensity profile over a field of illumination (sometimes referring to as FoV) of 60x45°, as stated in the General Introduction.

Major electro-optical parameters of the VCSEL module are summarized in Table 2.1. They derive from the datasheet **but are given at 25°C only due to a lack of data from the VCSEL supplier** (mostly because of trade secret or marketing reasons). The

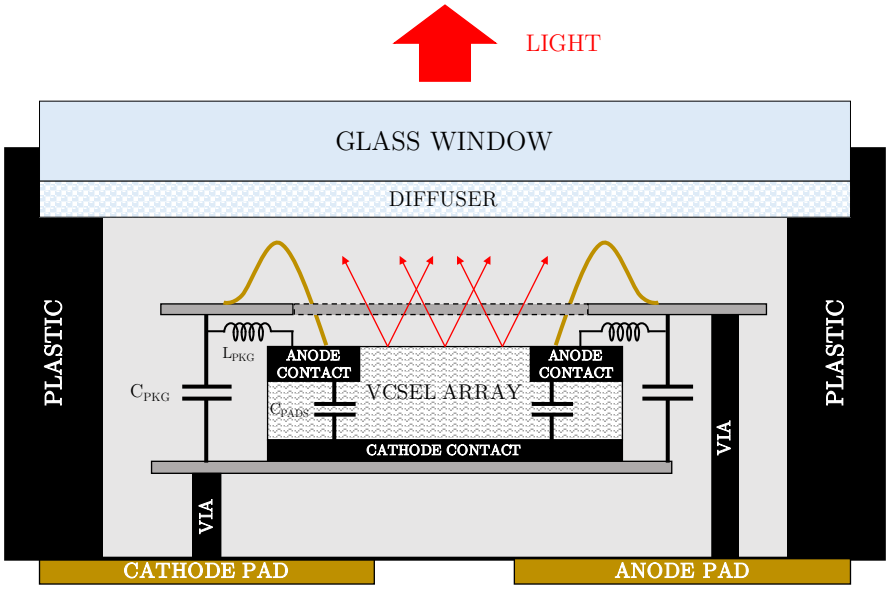


Figure 2.3 – Cross-sectional view of the VCSEL module superimposed with package parasitics.

slope efficiency η_{VCSEL} can be roughly considered here as the ratio of output optical power over current while the Power Conversion Efficiency (PCE), also referring to as wallplug efficiency, is defined as the ratio of output optical power over input electrical power, namely

$$PCE = \frac{P_{OPT}}{V_F I} \tag{2.2}$$

where V_F is the forward voltage across the VCSEL and I is the injected current [88]. An important point to notice is that a 3A current pulse is required to generate a laser pulse with a peak optical power of around 2.5W, as stated in Part 2.1.2.

2.1.5 Electro-optical model of the VCSEL

An electro-optical large signal model of the VCSEL module is essential in order to simulate its behavior, validate the circuit implementation and evaluate the performances of the system. Unfortunately, an accurate model has not been provided by the VCSEL supplier. Nevertheless, a simple SPICE-based electro-optical model is proposed for DC and transient simulations only. It comprises a Berkeley "Level 1" diode model (SPICE file) for modeling the electrical behavior of the VCSEL array as well as passive components for modeling package parasitics [93][94][95]. The SPICE file has been delivered by the VCSEL supplier while the values of package parisitics have been extracted from S-parameters measurements using a fitting procedure [96][97][98][99]. More details about the extraction procedure can be found in Appendix B. Finally, the optical behavior of the VCSEL module

Table 2.1 – Major electro-optical parameters of the VCSEL module from the datasheet (given at 25°C).

Parameter	Value
Wavelength	940nm
Field of illumination	60x45°
Output optical power P_{OPT} (under pulsed conditions)	2.4W
Threshold current I_{th}	300mA
Series resistance R_S	400mΩ
Nominal current I (under pulsed conditions)	3A
Forward voltage V_F (under pulsed conditions)	2.7V
Slope efficiency η_{VCSEL}	0.9W/A
Power Conversion Efficiency (PCE)	28%

uses simple DC equations based on the typical output characteristic (see Equation 2.1) [100].

The proposed equivalent circuit VCSEL model is illustrated in Figure 2.4 where C_{PKG} and C_{PADS} are parasitic capacitances due to anode and cathode contacts and pads respectively. L_{PKG} is the wire bonding inductance. R_S is the series resistance due to mirrors and contacts. R_j and C_j in parallel are respectively a junction resistance representing the active region where the photo-generating current flows and a non-linear capacitance representing the junction capacitance of the active region. Lastly D is an ideal diode representing the voltage drop due to the laser threshold [86][94][101][96]. Parameters R_S, R_j, C_j and D are part of the SPICE file, which is not detailed here.

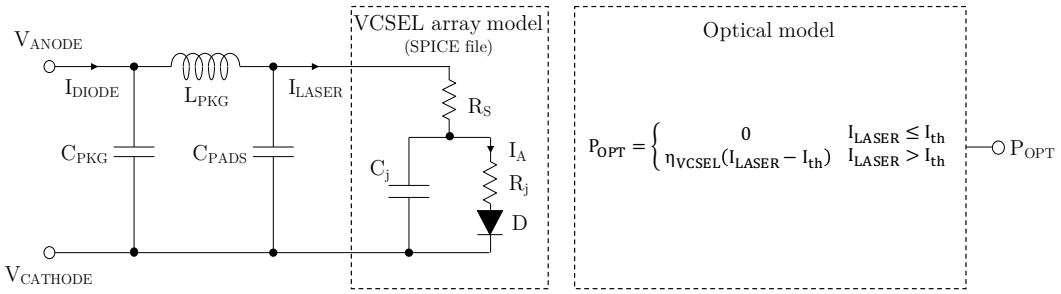
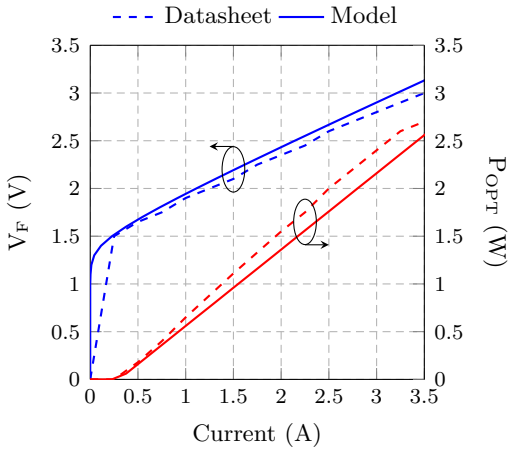


Figure 2.4 – Proposed equivalent-circuit VCSEL model.

The optical behavior is based on the typical VCSEL output characteristic under DC conditions and Equation 2.1 where the output optical power can be derived from the injected current through the active region, represented by the current I_A in Figure 2.4.

However, this current is not accessible due to the use of a SPICE file. For that reason, the current I_{LASER} representing the current injected through the whole VCSEL array is used instead. The output optical power is represented as the voltage P_{OPT} in Figure 2.4. Model parameters are summarized in Table 2.5b.

Figure 2.5a plots the electro-optical DC characteristic curves of the VCSEL module provided by the datasheet and from simulations using the proposed VCSEL model at 25°C. The plot shows a relatively good agreement between datasheet and simulation results. The slight deviation on the output characteristic curves are due to the different values used by the VCSEL supplier for the slope efficiency parameter. As this proposed optical model is only valid under DC conditions, optical results from transient simulations should be considered with caution.



(a) Characteristic curves from datasheet and DC simulations: forward voltage and output optical power vs. current.

Parameter	Value
Parasitic inductance L_{PKG}	700pH
Package capacitance C_{PKG}	60pF
Pads capacitance C_{PADS}	5pF
Threshold current I_{th}	300mA
Slope efficiency η_{VCSEL}	0.8W/A

(b) Model parameters.

Figure 2.5 – Electro-optical DC characteristics and model parameters for the proposed VCSEL model.

2.1.6 Optical power monitoring and current control loop

Because of the strong temperature dependence of the VCSEL's electro-optical characteristics, it seems essential to use a control loop in order to monitor the output optical power. In optical communication applications, some systems include an Automatic Power Control (APC) circuit in order to stabilize the output optical power of the VCSEL diode [50][102]. A Monitor Photodiode (MPD) captures a portion of the output optical power thus generating a current which can be used as a feedback signal to adjust the current through the VCSEL diode thus the output optical power. Usually, the MPD is placed near the VCSEL diode inside the same module where the captured light comes from its reflection on the cap window of the package. This solution means a compact component but at the

expense of an increased complexity and cost.

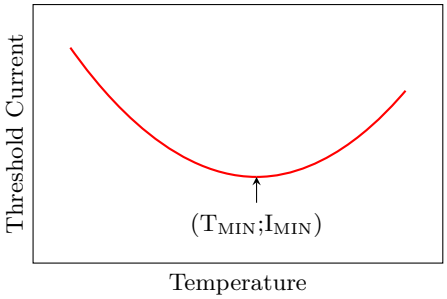


Figure 2.6 – Illustration of the typical temperature behavior of threshold current (as a reminder, data is provided at 25°C only).

The method adopted here is to directly monitor the current through the VCSEL diode without using a MPD, thus reducing cost and complexity but at the expense of the accuracy. However, it may still ensure an accurate control over a limited temperature range. Indeed, as the threshold current varies in a parabolic way with temperature, it can be considered constant for a limited temperature range as illustrated in Figure 2.6 [103]. An additional look-up table related to the temperature, current and optical power could be realized over a wide range of temperature during the characterization of the system for compensating this lack of accuracy.

2.1.7 CMOS technology and packaging

An integrated solution for the laser diode driver proves essential in order to develop a compact, fast and low cost system. It allows to overcome parasitic elements due to component packages and interconnections compared to an approach using discrete components, thus improving transient performances and reducing losses. This integrated approach may also save some PCB footprint.

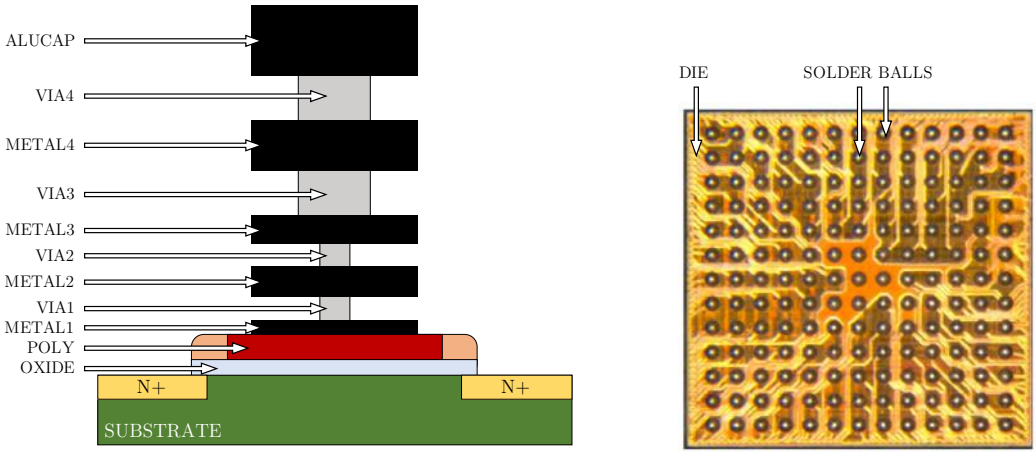
The 130nm CMOS technology from STMicroelectronics is a low cost technology well suited to embed analog, digital and power features into a single chip. The hcmos9a analog and mixed-signal process, which is intended for power management circuits in portable devices, has been used for this work. A key front-end feature of this process is to use a triple well process on a p-type substrate wafer. It means that n-well, p-well and deep n-well are available offering a wide range of active and passive devices.

Active devices The process includes conventional P-N junction diodes as well as Schottky diodes, Bipolar Junction Transistors (BJTs) and MOSFETs. MOSFET devices include

thin oxide (2.3nm) devices for digital functions supporting voltages up to 1.2V, thick oxide (8.5nm) devices for analog functions supporting voltages up to 4.8V and high-voltage devices using a thick oxide as well, for power functions capable of sustaining voltages up to 20V with specific design rules.

Passive devices The process includes poly, active and metal resistors as well as three types of capacitors such as Metal-Oxide-Metal (MOM) capacitors, Metal-Insulator-Metal (MIM) capacitors and Metal-Oxide-Semiconductor (MOS) capacitors.

In addition, the back-end process features a metallization composed of four copper metal layers with silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) inter-metal dielectrics as well as a final encapsulated aluminum layer (ALUCAP for short) on top of the last copper level. An illustration is shown in Figure 2.7a. Further details on this technology can be found in [104].



(a) (b)

Figure 2.7 – (a) Metallization of the considered technology (drawing not to scale) and (b) photograph of a WLCSP package. Source: NXP [105].

Finally, a Wafer Level Chip Scale Package (WLCSP) is used to package the integrated circuit in order to reduce the size of the chip, to minimize parasitic elements and to improve thermal characteristics. In fact, the package has the same size as the silicon die as shown in Figure 2.7b, on which Input/Output (I/O) pads are connected to an array pattern of bumps or solder balls through a Redistribution Layer (RDL). No bond wire nor interposer are required. This package can then be directly soldered on a PCB using traditional assembly processes. More information can be found in [105].

2.1.8 Power efficiency

The power efficiency of the system is a major concern here as it impacts the self-heating of devices, thus performances as well as the battery lifetime. In this context, a minimum efficiency value could be defined below which the system cannot ensure a proper operation or even worst, causing devices to burn and/or interconnections to melt. Since the optical efficiency of the system depends on VCSEL's characteristics, only the electrical efficiency of the driver is considered here which is defined by

$$\eta_{ELEC} = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \tag{2.3}$$

where P_{IN} is the input electrical power consumed by the driver from the battery, P_{OUT} is the output electrical power provided by the driver to the laser diode and P_{LOSS} is the total losses from the driver. All theses quantities are averaged over the time of operation (both during pulse trains and idle times). The output electrical power can be expressed as

$$P_{OUT} = \delta(\alpha V_F I_{ON}) \tag{2.4}$$

where δ is the duty cycle of the illumination pattern, α is the modulation duty cycle of the laser diode current, V_F is the laser diode forward voltage and I_{ON} is the ON-state current of the pulse. Total losses can be evaluated by considering the thermal Ohm's law given by [84]

$$P_{LOSS} = \frac{T_J - T_A}{R_{th}} \tag{2.5}$$

where T_J and T_A are the junction temperature of the chip and the ambient temperature respectively and R_{th} is the junction-to-ambient thermal resistance of the chip package. Actually, this thermal resistance depends on the package but also on several other system characteristics such as the PCB design and layout, pad size of the chip, etc...which values are very complicated to obtain. Nevertheless, it seems reasonable to take values reported from datasheets of various circuits, with similar specifications as the ones of the laser diode driver, in a first approximation. Considering circuits in [106][107][108], a thermal resistance value from 50°C/W up to 85°C/W can be assumed for roughly estimating a minimum efficiency requirement.

As a reminder, the VCSEL module and the driver are on separate chip. Assuming a worst-case scenario with junction and ambient temperatures of 125°C and 70°C respectively, total losses allowed by the chip are estimated around 650mW for a 85°C/W thermal resistance value. Using Equation 2.4 with $\delta = 0.33$, $\alpha = 0.5$, $V_F = 2.7V$ (given at 25°C only) and $I_{ON} = 3A$, the output electrical power is estimated around 1.35W leading to a minimum efficiency of 67.5%. A minimum value of 70% can be considered as a low boundary in any case to keep a safe margin.

2.1.9 Summary

All specifications detailed above are listed in Table 2.2. The driver should be capable of generating short current pulses of high amplitude with a high PRF over a supply voltage range from 2.5V to 4.8V (also referring as the input voltage V_{IN}). The current amplitude, also referring as the ON-state current I_{ON} thereafter, should be configurable up to 3A to accommodate VCSEL characteristics due to thermal and manufacturing process variations and to keep some design flexibility. The PRF, also referring as the modulation frequency f_{MOD} in the following, should be programmable as well from 50MHz up to 200MHz to fulfill iToF requirements. Assuming a 50% modulation duty cycle, it leads to generate current pulses with a pulse width at half maximum from 2.5ns up to 10ns. Although the electrical efficiency specification has been roughly estimated, a high value is essential for this work in order to ensure good performances of the overall system. It is thus considered as a leading requirement to achieve.

Table 2.2 – Specifications of the laser diode driver. (*see Appendix A).

Specification		**Value**	
CMOS Technology		hcmos9a 130nm analog and mixed signal process from STMicroelectronics	
Package		WLCSP	
Modulation type		Continuous Wave*	
Pulse repetition frequency range f_{MOD}		50MHz - 200MHz	
Modulation duty cycle α		50%	
Pulse width at half maximum t_{PWHM}		2.5ns - 10ns	
ON-state current I_{ON}		up to 3A	
Electrical efficiency η_{ELEC}		$\geq$70%	
Ambient temperature range		0 - 70°C, 27°C in typ.	
Battery type		Lithium-ion for mobile applications	
Supply voltage range V_{IN}	Capacity	2.5V - 4.8V, 3.6V in typ.	~3000mAh

2.2 Evaluation Methodology

Once specifications are defined for the laser diode driver, several architectures based on the topologies described in the previous chapter (see Chapter 1) are proposed and evaluated to meet objectives. Basically, proposed architectures focus on two classical driving topologies: the voltage-mode and current-mode drivers, meaning that the driver is respectively based on a voltage or current source for controlling the laser diode biasing according to the input voltage and the desired current. It is associated to a switching element to generate current pulses, thus laser pulses.

The first part of the preliminary study concerns the analysis of transient waveforms. The basic principle of each solution will be firstly explained. Then, transient waveforms will be analyzed with a simple simulation bench **using transistor device models from the design kit**. The analysis could be divided into two phases: the rising phase when a current settles through the laser diode for initiating the laser pulse and the falling phase when the current turns off for stopping the laser pulse. Modeling devices with ideal sources, switches, diodes, capacitances and resistances could help to understand the influence of each element on the circuit behavior. The main purpose is not to deeply identify all transition mechanisms with analytic equations as they are quite complex, but rather to find trends using hand calculations, which are predictable to some extent. This could be useful in order to highlight some design issues and help to select the adequate topology. It must be specified that the transient analysis will be performed **in typical conditions only** (typical process, 3.6V input voltage and 25°C ambient temperature). Moreover, the temperature-dependent circuit behavior will not be investigated during this work. Simulations will be carried out using the Virtuoso Analog Design Environment from Cadence® and the SPICE simulator Eldo from Mentor Graphics®.

The laser diode SPICE-based model described in Part 2.1.5 will be used as it is delivered. Nevertheless, only its electrical behavior will be simulated since the optical model is not valid for transient simulations. Therefore, simulation results should be used with caution. Moreover, the package capacitance C_{PKG}, as illustrated in Figure 2.8, will not be considered here as this parasitic component comes from the custom package provided by the VCSEL supplier and is not representative of typical VCSEL packages [47]. It will be however included in simulations for validating and evaluating performances of the laser diode driver prototype (further discussed in Part 3.4).

A MOSFET device is generally used for implementing the switching element. A BJT device would have significant driving losses since it is controlled in current [109]. Since MOSFET models provided by the design kit are quite complex, a simple model is preferred **for explanation only**, as the one used in [110]. It is illustrated in Figure 2.8. It takes basic parameters such as the on-channel resistance R_{ON}, the drain-to-source capacitance C_{DS} and the input capacitance C_{IN}. The turn-on and turn-off voltages of the switch S_W, similar to the threshold voltage $V_{th(MOSFET)}$ of the MOSFET device, are also required. In addition, the effect of the body diode (when bulk and source are shorted) can be modeled as an ideal diode, noted D_{BD}, turning-on or turning-off when the voltage across it is above or below its threshold voltage $V_{th(BD)}$. MOSFET device parameters could be extracted from the design kit models with quick simulations as described in [109].

Some considerations will be then discussed in the second part of the preliminary study by introducing major functional blocks. The purpose here is not to fully design and optimize

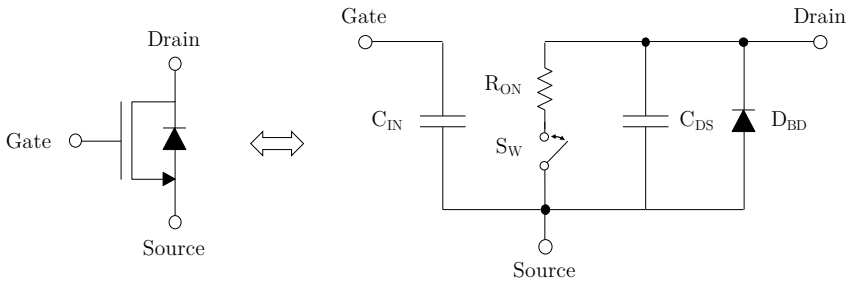


Figure 2.8 – Simple MOSFET model for explanation only (not for simulations).

each solution but rather to address main design issues and highlight key features. This could be useful for comparing the solutions and designing the laser diode driver prototype. One essential point concerns the power management circuit for biasing the laser diode according to the input voltage range (2.5V-4.8V) and the targeted current. It must be specified that the choice will be driven by power requirements such as providing a high output current with a high electrical efficiency.

The last part of the preliminary study concerns the comparative analysis of the proposed solutions. Since the architectures will not be fully designed, it will be complicated to accurately evaluate performances of each one, especially in terms of electrical efficiency and overall dissipated power. But major losses could be evaluated by hand calculations in order to identify critical elements. Then, a systemic approach would be preferred where pros and cons of each solution regarding various indicators will be gathered and discussed using a qualitative analysis. For instance the cost in terms of design complexity, silicon area, passive components and PCB footprint will be addressed.

A dedicated metric related to the ToF application could be used as an additional indicator. As explained in Appendix A, the phase shift measurement is based on the first harmonic of the modulation waveform only. In other words, conventional algorithms implemented to extract the phase shift and compute the depth are based on a sine wave laser signal. A pulsed laser signal is employed here introducing harmonics through the system that causes a systematic error on depth [111]. This error must be distinguished from any noise such as the photon shot noise. Therefore, it could be interesting to evaluate this systematic depth error for each solution. The purpose would be to perform the phase shift calculations using an iToF sensor model and transient simulation waveforms. Even if the optical laser diode model is not valid for transient simulations, the estimated error could still give an additional indicator for comparison assuming the same operating conditions of simulation for each solution. More details about the implementation of the iToF sensor model can be found in Part A.3.3.2.

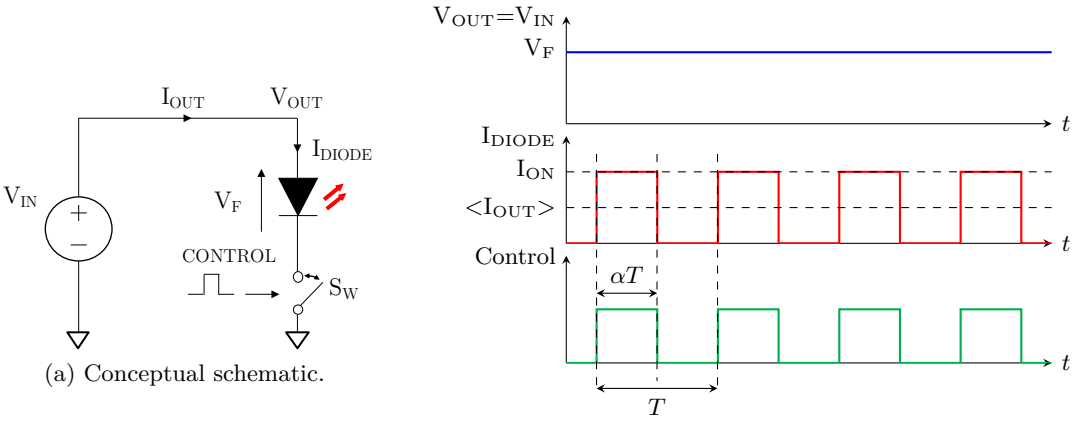
The evaluation methodology is summarized as follows:

- Basic principle description of each solution
- Transient analysis of waveforms based on simple models
- Design considerations related to each topology
- Comparative analysis of each solution using various indicators:
  - Complexity of the solution (primarily building blocks)
  - Silicon area and package size
  - Passive components and PCB footprint
  - Dissipated power and theoretical efficiency (major losses evaluated by hand calculations)
  - Systematic depth error

The most suitable solution with respect to the specifications will be used as the basis for designing the laser diode driver prototype.

2.3 Solution #1: Voltage-mode Driver in Series Configuration

2.3.1 Basic principle



(a) Conceptual schematic.

(b) Timing diagram.

Figure 2.9 – Basic principle of the voltage-mode driver topology using a series configuration.

The first proposed solution is based on the voltage-mode driver topology using a series configuration, as defined in Part 1.3.1. The conceptual schematic of the topology used

here is depicted in Figure 2.9a. Associated timing diagram is represented in Figure 2.9b. A voltage source V_{IN} is connected in series with a laser diode and a switching element S_W. It is assumed that the voltage source provides a constant output voltage V_{OUT} that must be sufficient to bias the laser diode according to the targeted ON-state current I_{ON}. In an ideal case, the output voltage is equal to the laser diode forward voltage V_F and the current I_{DIODE} through the laser diode is the photo-generating current. The operating principle is divided into two steps:

1. The switch is turned off so that no current flows through the laser diode. There is no light emission (OFF state).

2. The switch is turned on so that a current flows through the laser diode thus emitting light (ON state).

These steps are repeated for generating current pulses, thus laser pulses, according to the targeted current, frequency and modulation duty cycle. It can be noticed that the laser current is in phase with the control signal. Moreover, the average output current provided by the voltage source is expressed as

$$< I_{OUT} >= \alpha I_{ON} \tag{2.6}$$

where α is the modulation duty cycle of the diode current.

2.3.2 Transient analysis

The schematic of the transient simulation bench is depicted in Figure 2.10a, where parasitic elements have been included. As described in Part 2.2, the laser diode is modeled by using the electrical SPICE-based model without including the package capacitance. Then, it has been chosen to implement the switching element using a n-channel MOSFET (NMOS) device in order to simplify the circuit as it is ground-referenced. The transistor T_{SW} is a thick oxide 4.8V NMOS device and has been arbitrarily sized while respecting a minimum length (L=0.5µm) and a large width (W=50mm) to benefit from a sufficiently low on-channel resistance. The MOSFET is triggered by a control signal $V_{CONTROL}$ that is generated by a pulsed voltage source between 0 and 3.6V.

Simulations have been performed in typical conditions for a high ON-state current (3A) and for various frequency values (50MHz and 200MHz). The output voltage V_{OUT} has been set according to the targeted ON-state current. In a first approximation, it is expressed as

$$V_{OUT} = V_F(I_{ON}) + R_{ON}I_{ON} \tag{2.7}$$

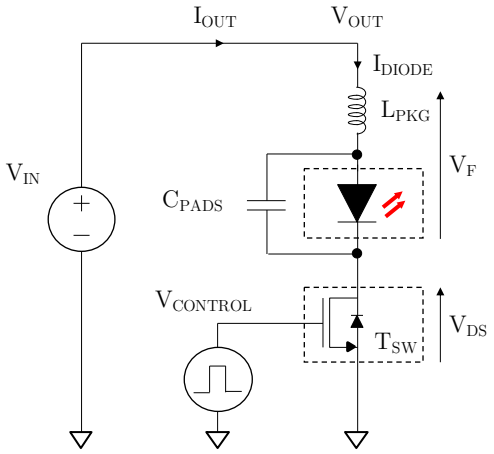
where $R_{ON}I_{ON}$ accounts for IR-drop through MOSFET channel and $V_F(I_{ON})$ is the laser diode forward voltage corresponding to the current I_{ON}. This voltage can be expressed as

a function of the current through the laser diode using the Shockley equation given by

$$V_F(I) = R_S I + nV_T \ln\left(1 + \frac{I}{I_S}\right) \tag{2.8}$$

where R_S is the series resistance, n is the ideality factor (or emission coefficient, usually $1 < n < 2$), V_T is the thermal voltage (~26mV at 25°C) and I_S is the saturation current. Since the laser diode model relies on a Berkeley "Level 1" diode model (SPICE file) that is not very accessible, these parameters have been extracted from DC simulations using a fitting procedure. Finally, Equation 2.7 gives $V_{OUT} \simeq 3V$ for $I_{ON} = 3A$ including an IR-drop of 120mV.

Parameters of interest are summarized in Table 2.10b. Basic parameters of the MOSFET model have been extracted as described in Part 2.2. Transient waveforms such as the current I_{DIODE} through the laser diode module, the drain-source voltage V_{DS} across the NMOS transistor T_{SW}, the control signal $V_{CONTROL}$ and the output voltage V_{OUT} are shown in Figure 2.11.



(a) Schematic.

Parameter	Value
Simulation	
V_{OUT}	3V
$V_{CONTROL}$	0-3.6V
I_{ON}	3A
f_{MOD}	50MHz & 200MHz
α	50%
t_r / t_f	250ps
MOSFET T_{SW} (thick-oxide)	
Length / Width	0.5µm / 50mm
$V_{th(MOSFET)}$	0.7V
$V_{th(BD)}$	0.7V
R_{ON}	40mΩ
C_{DS}	20pF
VCSEL	
$V_{th(VCSEL)}$	1.2V
R_S	490mΩ
I_S	2.34×10^{-14}A
n	1.7524
L_{PKG}	700pH
C_{PADS}	5pF

(b) Parameters and extracted values.

Figure 2.10 – Transient simulation bench.

The introduction of parasitic elements has a significant impact on current and voltage transients. Major mechanisms involved during both rising and falling phases are detailed

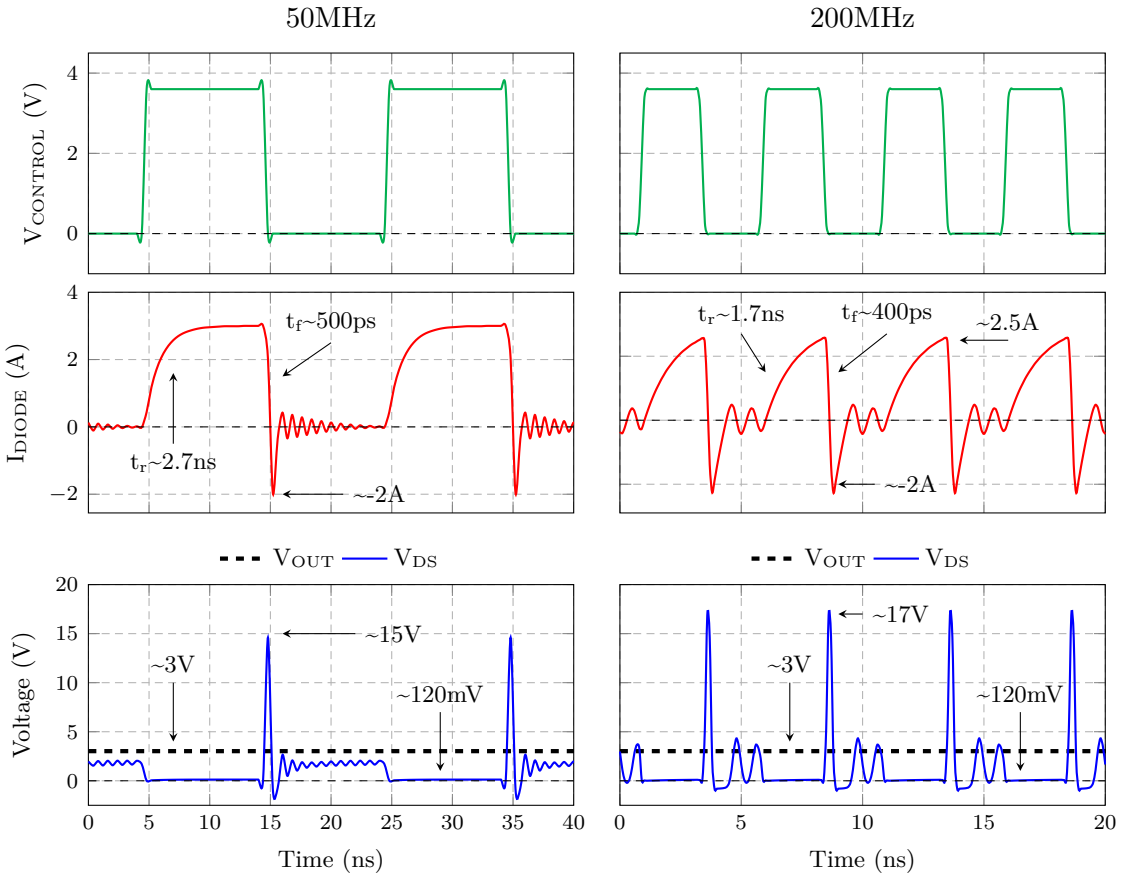
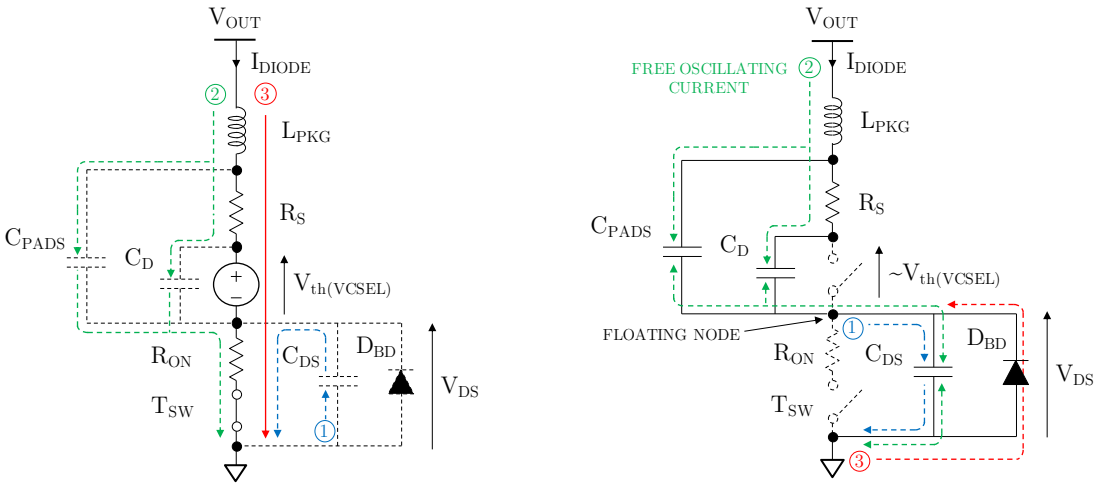


Figure 2.11 – Transient simulation waveforms for $I_{ON} = 3A$ at various frequencies. Typical conditions have been assumed (typ. process, 3.6V, 25°C).

hereafter. Equivalent circuits in Figure 2.12 may help to understand the transient behavior of the circuit.

2.3.2.1 Rising phase

The rising phase occurs when the transistor T_{SW} starts turning on (when $V_{CONTROL} \geq 0.7V$), discharging its output capacitance C_{DS} and decreasing its V_{DS} voltage (step 1 in Figure 2.12a). The current starts to increase. As V_{OUT} remains constant, the laser diode voltage increases accordingly, charging its parasitic capacitances C_{PADS} and C_D through the parasitic inductance L_{PKG}, the series resistance R_S and the MOSFET channel, seen as a resistance R_{ON} (step 2 in Figure 2.12a). Once these capacitances are fully charged, the diode junction is turned on and the circuit roughly behaves as a series RL circuit where



(a) Rising phase.

(b) Falling phase.

Figure 2.12 – Equivalent circuit during the two operating phases.

the current reaches its targeted value according to a time constant approximated as

$$\tau = \frac{L}{R} \tag{2.9}$$

where L and R are the equivalent series inductance and resistance in the laser diode path respectively (step 3 in Figure 2.12a).

In Figure 2.11, the rising time of the diode current is clearly dominated by the time constant of the equivalent circuit (~1.3ns with $L = L_{PKG}$ and $R = R_{ON} + R_S$). It is more significant at high frequency where the time constant is in the same order as the pulse width (assuming 2.5ns for 200MHz) causing the current not to reach its targeted value. A peak value of 2.5A is reached within ~1.7ns for 200MHz case whereas 3A was targeted. In both cases, parasitic elements could add a delay between the pulse initiation and the settling of the photo-generating current what may cause distortion in the laser signal.

2.3.2.2 Falling phase

The falling phase occurs when the transistor T_{SW} starts turning off (when $V_{CONTROL} \leq 0.7V$), charging C_{DS} and increasing its V_{DS} voltage (step 1 in Figure 2.12b). The current quickly decreases, discharging C_{PADS} and C_D until the diode junction is turned off. The switching node then becomes a floating node. The diode current still decreases, discharging L_{PKG} thus transferring its energy into C_{DS} through C_D, C_{PADS} and R_S and causing V_{DS} to ring up. Its peak value is reached when the diode current reaches 0 and can be

approximated as

$$V_{PEAK} = I_{ON}\sqrt{\frac{L}{C_{OUT}}} \tag{2.10}$$

where L is the equivalent series inductance in the laser diode path and C_{OUT} is the equivalent output capacitance at the floating node [112]. At this point, the circuit behaves as an RLC circuit without external excitation. The circuit can be oscillating or not depending on its damping ratio (step 2 in Figure 2.12b), approximated as

$$\zeta_{SERIES(OFF)} = \frac{R}{2}\sqrt{\frac{C_{OUT}}{L}} \tag{2.11}$$

where L and R are the equivalent series inductance and resistance in the laser diode path respectively and C_{OUT} is the equivalent output capacitance at the floating node. If it is oscillating (under-damped response, when $\zeta_{SERIES(OFF)} < 1$), it may cause V_{DS} to become sufficiently negative for triggering the body diode of the transistor S_W thus inherently damping the ringing (step 3 in Figure 2.12b).

In any case, the floating node settles around an operating point where no current flows, satisfying $V_F = 0V$. But practically, it depends on the leakage mechanisms induced by parasitic elements where time constants are far longer than pulse widths and frequencies considered here. Thus, the floating node settles around an operating point satisfying $V_F = V_{th(VCSEL)}$ so $V_{OUT} - V_{th(VCSEL)}$ before to be triggered by the next pulse.

In Figure 2.11, a ringing in the current and voltage waveforms is noticed at low and high frequencies which seems to be well damped by the resistive access of the body diode. Since no optical model is valid for transient simulations, it is quite complicated to evaluate if this ringing has an impact on the photo-generating current, thus the laser signal, but it could be possible that the laser diode emits very short secondary laser pulses. In addition, high voltage spikes above 15V are obtained on V_{DS} thus inducing strong undershoots on the current reaching around -2A. It is caused by the fast MOSFET turn-off associated to the parasitic inductances. The falling time of the diode current is around 500ps and 400ps at 50MHz and 200MHz respectively. These voltage spikes are quite critical here as they can destruct the transistor S_W able to support voltages up to 4.8V only.

2.3.2.3 Summary

It has been seen that parasitic elements impact current and voltage transient waveforms at low and high frequencies. The rising time of the diode current is slower than the falling time causing distortion on laser pulses. As a result, an essential point in order to improve transient performances of this topology concerns the parasitic inductance. It must be minimized as much as possible to reduce the rising time of the current, confirming the benefit of using an integrated solution (see Part 2.1.7). In addition, it contributes to

reduce voltage spikes at the switching node as well as the potential ringing.

Now, for a given parasitic inductance value and by considering the equivalent series RL circuit during rising phase, it can be seen that increasing the series resistance may also reduce the rising time but it is not recommended because it leads to increased conduction losses and voltage drops. Another point is to increase the output voltage provided by the voltage source in order to overcome the parasitic inductance and resistance as explained in Chapter 1. Equation 2.7 can thus be revised into

$$V_{OUT} = V_F(I_{ON}) + R_{ON}I_{ON} + L\frac{I_{ON}}{t_{PWHM}} \tag{2.12}$$

where L is the equivalent series inductance in the laser diode current path and t_{PWHM} is the pulse width at half maximum. For instance, it would lead to $V_{OUT} \sim 4V$ for I_{ON}=3A with a 2.5ns pulse width at 200MHz, what is achievable with respect to the input voltage range (2.5V-4.8V) by selecting the adequate power management circuit.

2.3.3 Power management considerations

The purpose here is to address some design issues and give some guidelines for implementing the proposed topology according to specifications described in Part 2.1. The major concern is about the voltage source V_{IN}. It must be capable of providing the correct output voltage to bias the laser diode with respect to the targeted ON-state current and the input voltage range (2.5V-4.8V). It must be also taken into account the voltage drop across parasitic inductances as previously explained. Therefore, it seems consistent to use a DC/DC converter which is able to step down and step up the output voltage against the input voltage with any voltage conversion ratio while keeping the same polarity. As no galvanic isolation is required, a non-isolated DC/DC converter structure is preferred.

As usual, choosing a structure among all existing ones requires some trade-offs between performances, complexity, passive components, PCB and silicon areas, cost, etc. Simplifying the study and future comparison, it has been decided to limit the scope at simple structures that are well understood and described in the literature [113][114][115][116][117]. It must also be recalled that the choice will be driven by power requirements such as providing a high output current with a high electrical efficiency.

It exists three major types of converters: linear voltage regulator, switched-capacitor and Switched-Mode Power Supply (SMPS) DC/DC converters. All come with advantages and drawbacks. Linear voltage regulators, acting as a resistive divider, are not relevant here as they can only be used for step-down operation and as they suffer from a low efficiency (typically from 20% to 60%) [114]. On the other hand, switched-capacitor (SC) converters uses an assembly of switches working in association with capacitors, as energy storage

element, for converting the power. They can be used in step-down or step-up operating modes depending on the topology. However, a well-known issue is that a high efficiency is only reached for a particular voltage conversion ratio. Even if topologies exist to address this limitation, it is at the expense of an increased complexity [116]. SMPS uses an assembly of switches working in association with inductors and capacitors for converting the power. The inductor is the main component for storing the energy. They can be used in step-down or step-up operating modes and any voltage conversion ratio can be reached with a high efficiency, typically from 70% to 95% [114][113][116]. Nevertheless, bulky and off-chip components, such as capacitors or power inductors, are usually required for handling currents of few Amps or achieving low output voltage ripple [118]. This type of converters seems to be the most suitable to use in this context.

Conventional SMPS converter topologies operating in both step-down and step-up modes include buck-boost type structures such as the well-known buck-boost converter as well as flyback converter, SEPIC converter, Ćuk converter, etc. More information can be found in [113]. A four-switch non-inverting buck-boost converter consisting of a single inductor, a single capacitor and four switches is considered here, where the output voltage keeps the same polarity as the input voltage. It benefits from less off-chip passive components than other topologies thus reducing PCB footprint. A simplified schematic is illustrated in Figure 2.13. Basically, the output voltage is adjusted by varying the duty cycle D applied

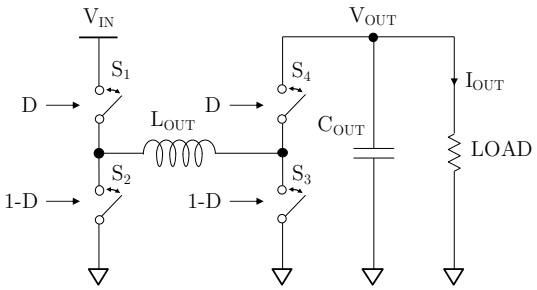


Figure 2.13 – Simplified schematic of the four-switch non-inverting buck-boost converter. It can be seen as a buck converter connected to a boost converter in cascade.

to the switches. It can be operated in three different modes (buck mode, buck-boost mode and boost mode) depending on load and input voltage conditions. A Continuous Conduction Mode (CCM) is preferred here for high efficiency, where a one-phase switching method could be employed for each mode in order to simplify the controlling circuitry. The operating principle is briefly described as follows:

- Buck mode (when $V_{IN} > V_{OUT}$): switch S_3 is kept turned-off while S_4 is turned-on. Then, switches S_1 and S_2 are alternatively toggled according to the duty cycle. The converter operates as a conventional buck converter.

- Buck-boost mode (when $V_{IN} \simeq V_{OUT}$): the four switches are alternatively toggled in each switching cycle according to the duty cycle. First, switches S_1 and S_3 are turned-on while switches S_2 and S_4 are turned-off. Then, the operation is inverted where S_1 and S_3 are turned-off and S_2 and S_4 are turned-on.
- Boost mode (when $V_{IN} < V_{OUT}$): switch S_2 is kept turned-off while S_1 is turned-on. Then, switches S_3 and S_4 are alternatively toggled according to the duty cycle. The converter operates as a conventional boost converter.

More details about the operating principle can be found in [119][120]. Fundamental equations in an ideal case are reminded hereafter. The voltage conversion ratio can be expressed as

$$\frac{V_{OUT}}{V_{IN}} = D \text{ when } V_{IN} > V_{OUT} \text{ (buck mode)} \tag{2.13}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{1-D} \text{ when } V_{IN} \simeq V_{OUT} \text{ (buck-boost mode)} \tag{2.14}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D} \text{ when } V_{IN} < V_{OUT} \text{ (boost mode)} \tag{2.15}$$

In the same way, the average current through the inductor $< I_L >$ can be expressed as

$$< I_L >=< I_{OUT} >= \alpha I_{ON} \text{ when } V_{IN} > V_{OUT} \text{ (buck mode)} \tag{2.16}$$

$$< I_L >= \frac{< I_{OUT} >}{1-D} = \frac{\alpha I_{ON}}{1-D} \text{ when } V_{IN} \simeq V_{OUT} \text{ (buck-boost mode)} \tag{2.17}$$

$$< I_L >= \frac{< I_{OUT} >}{1-D} = \frac{\alpha I_{ON}}{1-D} \text{ when } V_{IN} < V_{OUT} \text{ (boost mode)} \tag{2.18}$$

It is important to notice that the buck-boost mode brings large conduction losses where the average current through the inductor can be twice larger than the output current. For instance and by using Equation 2.6 with $\alpha = 0.5$ and $I_{ON} = 3A$, a duty cycle of 50% in buck-boost mode would lead to an average current of 3A through the inductor, increasing conduction losses through resistive elements (MOSFET channels, series resistance of inductor in a practical case) compared to buck or boost mode where less switches are used.

A simplified schematic of the proposed driver architecture is illustrated in Figure 2.14. It includes the buck-boost DC/DC converter, the laser diode and the switching element with its driving circuitry. Some specific recommendations must be considered here for choosing key parameter values of the driver. The switching frequency of the converter could be selected sufficiently low (f_{SW}<10MHz) compared to the PRF (50MHz-200MHz) in order to benefit from relatively low switching losses and some flexibility for implementing the feedback loop. The output voltage provided by the converter is thus seen relatively constant during the pulse duration leading to a stable ON-state current pulse. Then, as the converter can operate in three different modes, the most restrictive design criteria

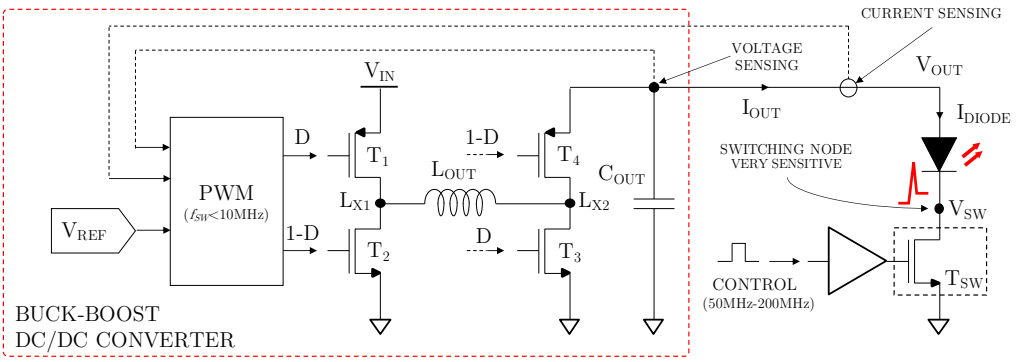


Figure 2.14 – Simplified schematic of the proposed voltage-mode driver architecture in series configuration.

among all modes must be taken into account for selecting the inductor, capacitor and switches.

In both buck-boost and boost modes, currents through the output pair of transistors (T_3 and T_4 in Figure 2.14) and the output capacitor are discontinuous therefore an output capacitor with a relatively high value and a low Equivalent Series Resistance (ESR) could be selected for ensuring a low output voltage ripple [113]. The minimum value $C_{OUT(MIN)}$ to limit the voltage ripple below ΔV is given by

$$C_{OUT(MIN)} = \frac{D_{MAX} I_{ON}}{f_{SW} \Delta V} \tag{2.19}$$

where D_{MAX} is the maximum duty cycle reached in buck-boost or boost mode. The capacitor must also support the highest output voltage provided by the converter and must handle the maximum output current, which is the ON-state current, when transistor T_4 is turned-off. A power inductor with a relatively high value could be selected to maintain a low inductor current ripple while still operating the converter in CCM [113]. The minimum value L_{MIN} to limit the current ripple below ΔI_L is given by

$$L_{MIN} = \frac{D_{MAX} V_{IN(MAX)}}{f_{SW} \Delta I_L} \tag{2.20}$$

where D_{MAX} is the maximum duty cycle reached in buck-boost or boost mode and $V_{IN(MAX)}$ is the maximum input voltage. The inductor also needs to be able to handle the peak switching current without saturating the core [121]. In addition, a relatively high switching frequency (~MHz) could be used to benefit from small off-chip passive components while still ensuring low ripple levels and low passive components losses. However, it would be at the expense of increased switching losses [115].

A standard Pulse Width Modulation (PWM) method using a current-control and voltage-control loops could be employed in order to adjust the output voltage according to the targeted current value set by a voltage-level reference, as described in [122]. The

DC/DC converter thus acts as a current-controlled voltage source. It must be clarified that the current to be monitored here is the laser diode current rather than the inductor current or the output current as usually performed in DC/DC converters. Nevertheless, as the pulse width of current pulse can be very short (2.5ns for a 200MHz PRF), it is difficult to sense the ON-state (or peak) value of pulses without involving a complex solution [123]. Instead, traditional current sensing techniques [124] could be used to monitor the average current I_{AVG} through the laser diode while the ON-state (or peak) value would be controlled by the modulation duty cycle α of the control signal, expressed as follows

$$I_{ON} = \frac{I_{AVG}}{\alpha} \tag{2.21}$$

where $I_{AVG} =< I_{OUT} >$.

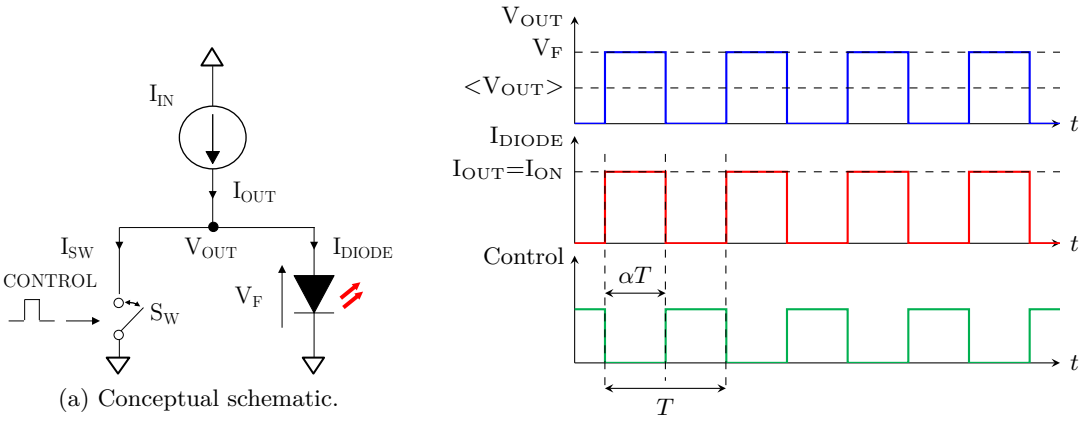
The power stage of the converter should be implemented using devices capable of handling current and voltage stress over all possible operating conditions. It could be either the inductor or output currents and either the input or output voltages depending on the device. Thus, high-voltage devices should be required specifically for the transistor pair at the node L_{X2} where the voltage swing can be higher than that of thin or thick oxide devices can handle (see Part 2.1.7). Thick oxide devices could be used for the transistor pair at the node L_{X1}. p-channel MOSFET (PMOS) and NMOS devices could be selected for simplifying the driving circuitry. Finally, the switching element could be implemented by a NMOS device as described earlier. Since strong constraints are considered here, its implementation is further discussed in Part 3.2.2. In addition, protection circuits such as a clamping circuit could be used for preventing any damage caused to the laser diode and MOSFET devices.

All these key design parameters are further discussed in Part 2.6.

2.4 Solution #2: Current-mode Driver in Shunt Configuration

2.4.1 Basic principle

The second proposed solution is based on the current-mode driver topology using a shunt configuration, as defined in Part 1.3.2. The conceptual schematic of the topology is depicted in Figure 2.15a. Associated timing diagram is represented in Figure 2.15b. A current source I_{IN} is connected to a laser diode with a switching element S_W placed in parallel. It is assumed that the current source provides a constant output current I_{OUT} equal to the targeted ON-state current I_{ON}. In an ideal case, the current I_{DIODE} through the laser diode is the photo-generating current. The operating principle is divided into two steps:



(a) Conceptual schematic.

(b) Timing diagram.

Figure 2.15 – Basic principle of the current-mode driver topology using a shunt configuration.

1. The switch is turned on for shunting the current to the ground so that no current flows through the laser diode. There is no light emission (OFF state).
2. The switch is turned off so that a current flows through the laser diode thus emitting light (ON state).

These steps are repeated for generating current pulses, thus laser pulses, according to the targeted current, frequency and modulation duty cycle. It can be noticed that the laser current is in phase opposition with the control signal. Moreover, the average output voltage provided by the current source is expressed as

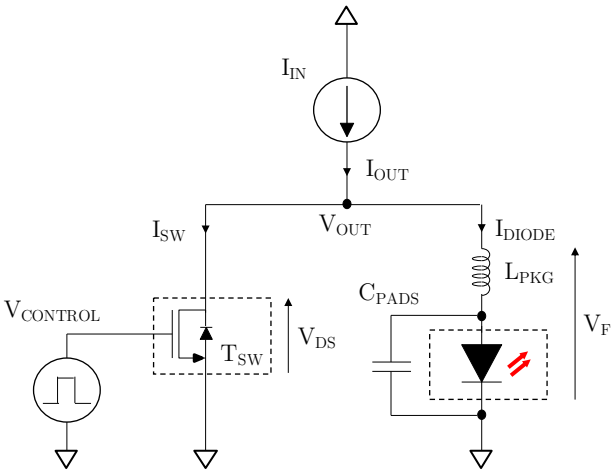
$$< V_{OUT} >= \alpha V_F \tag{2.22}$$

where V_F is the laser diode forward voltage and α is the modulation duty cycle of the diode current.

2.4.2 Transient analysis

The schematic of the transient simulation bench is depicted in Figure 2.16a. It includes the laser diode with parasitic elements and the same NMOS device (L=0.5µm, W=50mm) as switching element. The MOSFET is also triggered by the same control signal $V_{CONTROL}$. Simulations have been performed in typical conditions for a high ON-state current (3A) and for various frequency values (50MHz and 200MHz). The output current I_{OUT} has been set according to the targeted ON-state current (3A in that case). Parameters of interest are summarized in Table 2.16b. Transient waveforms such as the current I_{DIODE} through the laser diode module, the output current I_{OUT}, the drain-source voltage V_{DS} across the NMOS transistor T_{SW} (equal to the forward voltage V_F and the output voltage

V_{OUT}) and the control signal $V_{CONTROL}$ are shown in Figure 2.17. It must be specified that the forward voltage V_F is the voltage across the laser diode module including the forward voltage across the VCSEL die and the parasitic inductance.



(a) Schematic.

Parameter	Value
Simulation	
$V_{CONTROL}$	0-3.6V
I_{OUT}	3A
I_{ON}	3A
f_{MOD}	50MHz & 200MHz
α	50%
t_r / t_f	250ps
MOSFET T_{SW} (thick-oxide)	
Length / Width	0.5µm / 50mm
$V_{th(MOSFET)}$	0.7V
$V_{th(BD)}$	0.7V
R_{ON}	40mΩ
C_{DS}	20pF
VCSEL	
$V_{th(VCSEL)}$	1.2V
R_S	490mΩ
I_S	$2.34x10^{-14}$A
n	1.7524
L_{PKG}	700pH
C_{PADS}	5pF

(b) Parameters and extracted values.

Figure 2.16 – Transient simulation bench.

Parasitic elements have a significant impact on current and voltage transients. Major mechanisms involved during both rising and falling phases are detailed hereafter. Equivalent circuits in Figure 2.18 may help to understand the transient behavior of the circuit.

2.4.2.1 Rising phase

The rising phase occurs when the transistor T_{SW} starts turning off (when $V_{CONTROL} \leq 0.7V$), charging C_{DS} and increasing its V_{DS} voltage (step 1 in Figure 2.18a). As the output current I_{OUT} is constant, the current I_{SW} that decreases in the transistor path starts to be balanced in the laser diode path, thus increasing its forward voltage in the same way as V_{DS} and charging its parasitic capacitances C_{PADS} and C_D through the parasitic inductance L_{PKG} (step 2 in Figure 2.18a). The diode junction turns on once these capacitances are fully charged. At this point, the circuit acts as a RLC circuit pursuing to reach the targeted operating point (I_{ON}, $V_F(I_{ON})$) while still diverting the current from transistor path to the laser diode path (step 3 in Figure 2.18a). This circuit

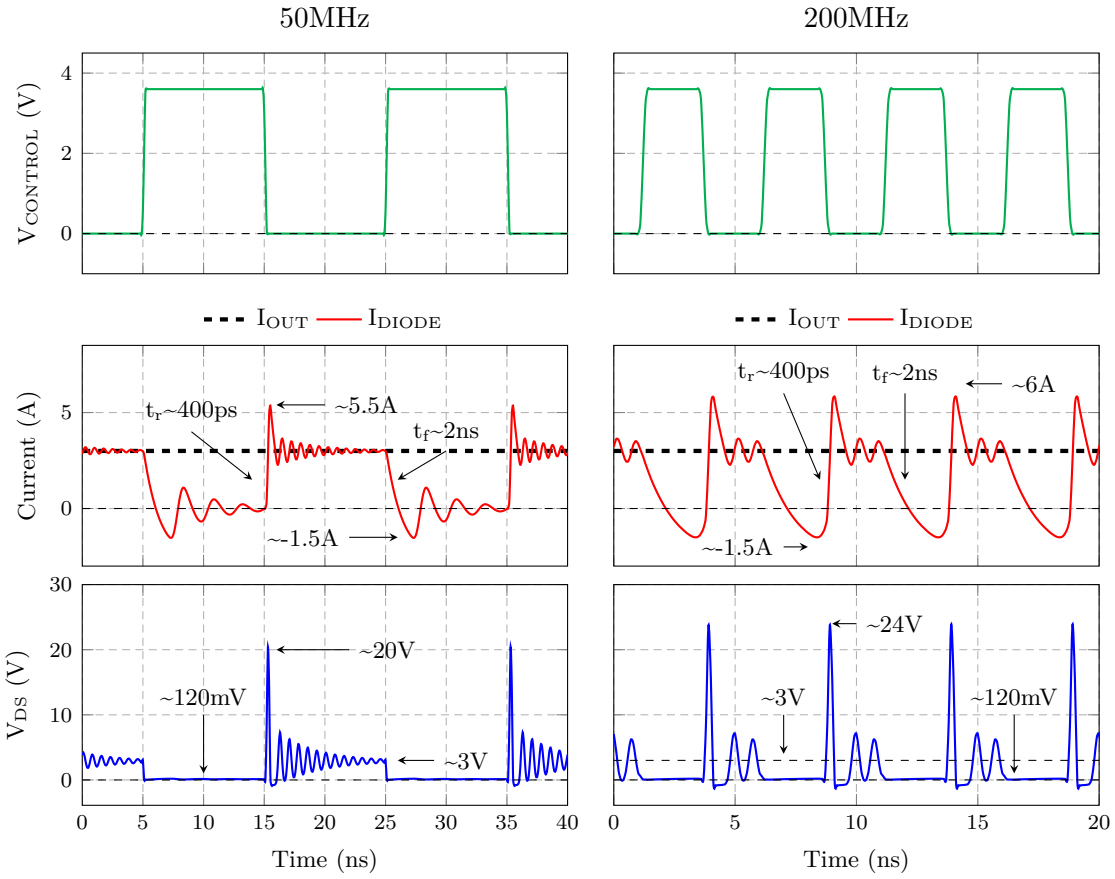
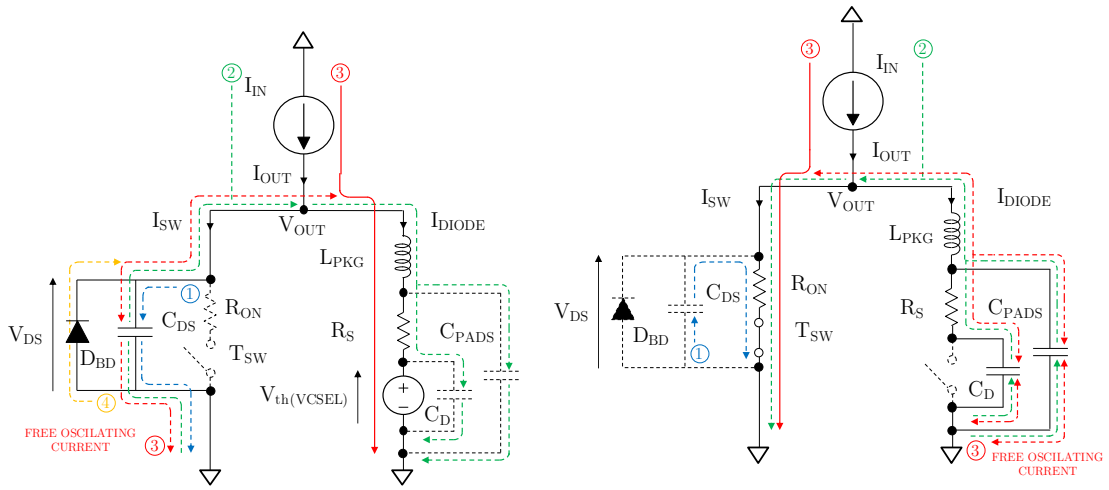


Figure 2.17 – Transient simulation waveforms for $I_{ON} = 3A$ at various frequencies. Typical conditions have been assumed (typ. process, 3.6V, 25°C).

can be oscillating or not depending on its damping ratio, approximated as

$$\zeta_{SHUNT(ON)} = \frac{R}{2}\sqrt{\frac{C_{OUT}}{L}} \tag{2.23}$$

where L and R are the equivalent series inductance and resistance in the laser diode path respectively and C_{OUT} is the equivalent output capacitance between the switching node and the ground. If it is oscillating (under-damped response, when $\zeta_{SHUNT(ON)} < 1$), it may generate a current loop within the laser diode and transistor paths. It could also cause V_{DS} to become sufficiently negative to trigger the body diode of the transistor S_W thus inherently damping the ringing (step 4 in Figure 2.18a). In any case, the entire output current provided by the current source is flowing through the laser diode path at the end of the phase, where current and voltage have reached the targeted operating point (I_{ON},



(a) Rising phase.

(b) Falling phase.

Figure 2.18 – Equivalent circuit during the two operating phases.

$V_F(I_{ON})$).

In Figure 2.17, a ringing in current and voltage waveforms is noticed at low and high frequencies which seems to be damped by the body diode. Once again, it is quite complicated to evaluate the impact of this ringing on the photo-generating current due to the lack of an optical model for transient simulations. Nevertheless, the negative voltage on V_{DS} occurring when triggering the body diode is due to the voltage drop across the parasitic inductance, what probably does not impact the forward voltage across the VCSEL die. In addition, high voltage spikes above 20V are obtained on V_{DS} thus inducing strong overshoots on the current reaching around 5.5A. It is caused by the fast MOSFET turn-off associated to the parasitic inductances. The rising time of the diode current is around 400ps at 50MHz and 200MHz. It could be possible that these current spikes involves the photo-generating current thus inducing overshoots on laser pulses resulting in potential human eye damages.

2.4.2.2 Falling phase

The falling phase occurs when the transistor T_{SW} starts turning on (when $V_{CONTROL} \geq 0.7V$), discharging its output capacitance C_{DS} and decreasing its V_{DS} voltage (step 1 in Figure 2.18b). As I_{OUT} is constant, the laser diode current I_{DIODE} starts to be diverted to the transistor T_{SW}, thus decreasing the forward voltage V_F in the same way as V_{DS}. It causes C_{PADS} and C_D to discharge through L_{PKG}, the series resistance R_S and the MOSFET channel, seen as a resistance R_{ON}, until the diode junction is turned off (step 2 in

Figure 2.18b). At this point, the circuit acts as a RLC circuit where parasitic inductances and capacitances from the laser diode path tend to discharge the energy they have stored during the previous phase into the ground through the MOSFET channel (step 3 in Figure 2.18b). This circuit can be oscillating or not depending on its damping ratio, approximated as

$$\zeta_{SHUNT(OFF)} = \frac{R}{2}\sqrt{\frac{C}{L}} \tag{2.24}$$

where L and R are the equivalent series inductance and resistance in the laser diode and transistor paths respectively, and C is the equivalent parasitic capacitance of the laser diode. If it is oscillating (under-damped response, when $\zeta_{SHUNT(OFF)} < 1$), it may generate a current loop within the laser diode and transistor paths. In any case, the entire output current provided by the current source is flowing through the transistor path at the end of the phase, where the current has reached the targeted value I_{ON} and the V_{DS} voltage accounts for IR-drop.

In Figure 2.17, the V_{DS} voltage quickly decreases whereas the diode current decreases with a relatively slow falling time (~2ns at 50MHz and 200MHz) in both 50MHz and 200MHz cases. The decay seems to be dominated at first order by the parasitic inductances having stored energy under 3A during the previous phase. At second order, a ringing on the current is noticed, particularly at low frequency, inducing strong undershoots reaching around -1.5A. Even if it induces short secondary current pulses, this probably involves the current through parasitic elements of the laser diode and not through the diode junction thus it may not impact the photo-generating current so the laser signal. In fact at high frequency, the ringing is initiated but directly interrupted by the initiation of the next pulse since the falling time is in the same order as the off time (assuming an off time of 2.5ns for 200MHz). Therefore, it may still cause a severe distortion in the laser signal at high frequency.

2.4.2.3 Summary

It has been seen that similar mechanisms as the ones in solution #1 are involved during transient phases at low and high frequencies. But for this topology, the rising time of the diode current is faster than the falling time what still causes distortion on laser pulses. Furthermore, high voltage spikes occurring at the switching node when the current is turning on may also induce spikes on the photo-generating current thus on laser pulses. As previously explained, minimizing as much as possible the parasitic inductances proves essential in order to reduce the falling time of the current reducing in the same way the potential ringing, and spikes at the switching node during the rising phase.

Another solution to improve transient performances could be to add a switching element in the laser diode path in order to quickly stop the current flow thus benefiting from a fast

turn-off delay whatever parasitic inductances are, as described in [76][77]. Nevertheless, it would involve a second driving circuitry thus increasing conduction and switching losses, what it is not recommended in the design of an efficient solution.

2.4.3 Power management considerations

The purpose here is to address some design issues and give some guidelines for implementing the proposed topology according to specifications described in Part 2.1. The major concern is about the current source I_{IN}. It must be capable of providing a constant output current, which requires a high output impedance, according to the targeted ON-state current and the input voltage range (2.5V-4.8V). The choice will also be driven by power requirements such as providing a high output current with a high electrical efficiency. The approach for selecting the adequate DC/DC converter structure is quite different from solution #1 since the conventional structures act as a voltage source using an output capacitor with a low output impedance.

A method would consist in using a power supply connected to an inductor in order to create a current source benefiting from the high output impedance of the inductor, as described in [125][79]. As detailed in Part 1.3.2, this concept has been developed by Texas Instruments for evaluating the OPT8241 3D Time-of-Flight sensor (OPT8241-CDK-EVM evaluation module). A power-distribution switch is employed to connect the power supply to the inductor where it allows to limit the maximum current [78]. For controlling the current, a solution could be to use a linear voltage regulator instead, monitoring current and voltage applied to the inductor according to the power supply but it would be at the cost of large conduction losses due to its working principle. Other works have been developed such as in [80] and in [76][77] where a half-bridge synchronous rectifier feeds an inductance to provide a constant output current to a load. A conceptual schematic is illustrated in Figure 2.19. Basically, the output voltage is adjusted by varying the duty cycle D applied

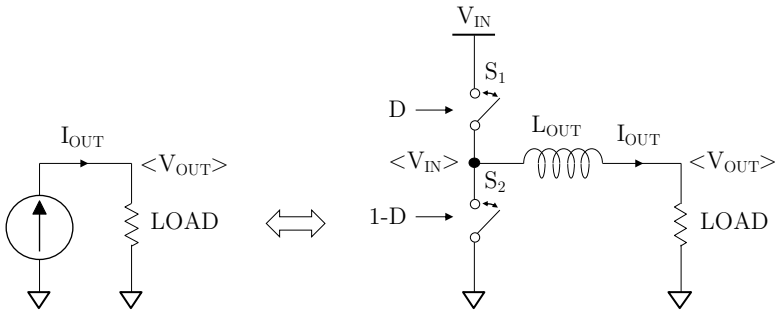


Figure 2.19 – Conceptual schematic of a current source using a half-bridge synchronous rectifier and an inductor.

to the switches of the rectifier where S_1 and S_2 are alternatively toggled. This allows to

indirectly adjust the output current according to load conditions ($I_{OUT} = f(V_{OUT})$). As no output capacitor is used, the output current provided by the inductor to the load is then relatively constant whatever is the instantaneous output voltage. Actually, the average output voltage $< V_{OUT} >$ is ruled by the average input voltage delivered by the rectifier in steady-state mode, expressed as follows

$$< V_{OUT} >=< V_{IN} >= D.V_{IN} \tag{2.25}$$

For instance and by using Equation 2.22 with $\alpha = 0.5$ and $V_F = 3V$ giving $< V_{OUT} >= 1.5V$, it can be seen that even an input voltage range from 2.5V to 4.8V would lead to a duty cycle range from 30% to 60% which is clearly achievable with conventional control strategies such as a PWM method. This structure, which can be seen as a standard buck converter without output capacitance, seems relevant to be employed here due to its simplicity and few required passives components, namely one inductor. Nevertheless, it must be tailored according to specifications.

A non-isolated buck DC/DC converter structure is preferred since no galvanic isolation is required. Details about its well-known operating principle can be found in [113][117][115]. But in this context, a two-switch buck converter operating in CCM and employing a one-phase switching method, is considered without output capacitance. A simplified schematic of the proposed driver architecture is illustrated in Figure 2.20. It includes the modified buck DC/DC converter, the laser diode and the switching element with its driving circuitry. The operating principle of the driver is derived from explanations above. The switching

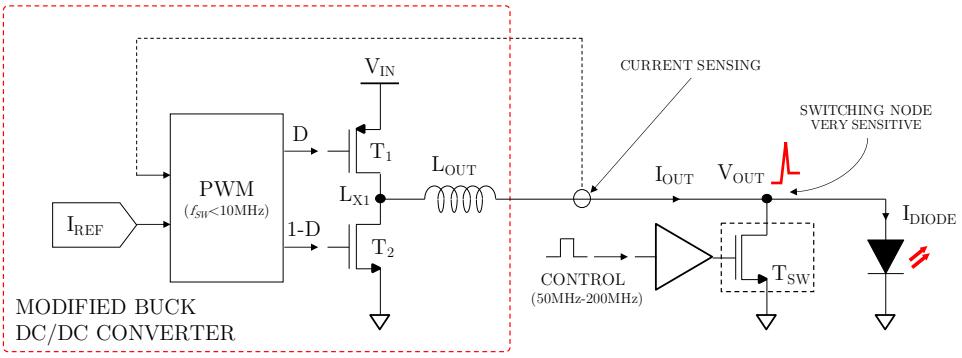


Figure 2.20 – Simplified schematic of the proposed current-mode driver architecture in shunt configuration.

frequency of the converter could be selected sufficiently low (f_{SW}<10MHz) compared to the PRF (50MHz-200MHz) in order to benefit from relatively low switching losses and some flexibility for implementing the feedback loop. The output current provided by the converter is thus seen relatively constant during the pulse duration leading to a stable ON-state current pulse. The output voltage is averaged over the inductor and adjusted by the duty cycle of the power stage. It is important to notice that this solution brings

relatively large conduction losses through the inductor where the average current can be approximated as

$$< I_L >=< I_{OUT} >= I_{ON} \tag{2.26}$$

A relatively high value for the power inductor is necessary to maintain a low inductor current ripple while still operating the converter in CCM. The minimum value L_{MIN} to limit the current ripple below ΔI_L is given by

$$L_{MIN} = \frac{D(1-D)V_{IN(MAX)}}{f_{SW}\Delta I_L} \Rightarrow L_{MIN} \leqslant \frac{0.25V_{IN(MAX)}}{f_{SW}\Delta I_L} \tag{2.27}$$

where D is the duty cycle and $V_{IN(MAX)}$ is the maximum input voltage. The inductor also needs to be able to handle the peak switching current without saturating the core. A relatively high switching frequency (~MHz) could be used to benefit from a small component but at the expense of increased switching losses.

A standard PWM method using a current-control loop could be employed in order to adjust the output current according to the targeted current value set by the current-level reference, as described in [122]. The modified DC/DC converter thus acts as a current-controlled current source. In contrast to solution #1, the current to be monitored here could be the average current through the inductor since it directly corresponds to the ON-state current. This approach could benefit from simple current sensing techniques as usually performed in DC/DC converters [124].

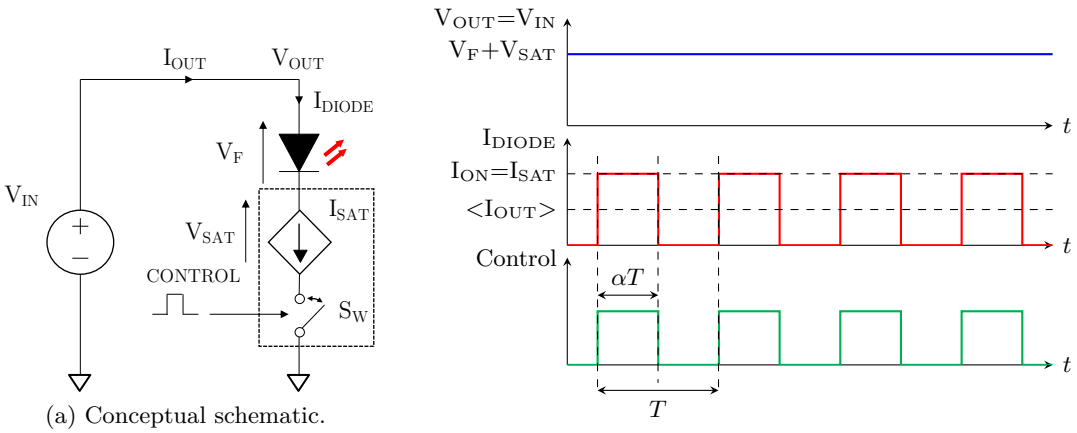
The power stage of the converter should be implemented using devices capable of handling the maximum inductor current and voltage. Thick oxide devices could be appropriate here. PMOS and NMOS devices could be selected for simplifying the driving circuitry. Finally, the switching element could be implemented by a NMOS device as described earlier. Since strong constraints are considered here, its implementation is further discussed in Part 3.2.2. In addition, a clamping circuit could be used especially for clamping laser spikes induced by voltage spikes, that may also help the current-control loop to correctly monitor the ON-state current.

All these key design parameters are further discussed in Part 2.6.

2.5 Solution #3: Current-mode Driver in Current Limiter Configuration

2.5.1 Basic principle

The third proposed solution is based on the current-mode driver topology using a current limiter configuration, as defined in Part 1.3.2. The conceptual schematic of the topology is depicted in Figure 2.21a. Associated timing diagram is represented in Figure 2.21b. A voltage source V_{IN} is connected in series with a laser diode, a controlled current source



(a) Conceptual schematic.

(b) Timing diagram.

Figure 2.21 – Basic principle of the current-mode driver topology using a current limiter configuration.

I_{SAT} and a switching element S_W. The controlled current source associated to the switch can be seen as a current limiter. It is assumed that the current source forces a current equal to the targeted ON-state current I_{ON} but only when the switching element is turned on. The voltage source must provide a constant and fixed output voltage V_{OUT} taking into account the maximum forward voltage for biasing the laser diode and a sufficient voltage headroom V_{SAT} to make the current generator to work on proper operational region during the rising phase. In an ideal case, the current I_{DIODE} through the laser diode is the photon-generating current. The operating principle is divided into two steps:

1. The switch and the current source are turned off so that no current flows through the laser diode. There is no light emission (OFF state).

2. The switch and the current source are turned on so that a current flows through the laser diode thus emitting light (ON state).

These steps are repeated for generating current pulses, thus laser pulses, according to the targeted current, frequency and modulation duty cycle. It can be noticed that the laser current is in phase with the control signal. Moreover, the average output current provided by the voltage source is expressed as

$$< I_{OUT} >= \alpha I_{ON} \tag{2.28}$$

where α is the modulation duty cycle of the diode current.

2.5.2 Transient analysis

The schematic of the transient simulation bench is depicted in Figure 2.22a. As before, it includes the laser diode with parasitic elements and the same NMOS device (L=0.5µm,

W=50mm) as switching element. It has been chosen to implement the controlled current source I_{SAT} as a cascode transistor operating in saturation region. A thick-oxide NMOS device is selected and arbitrarily sized while respecting a minimum length (L=0.5µm) and a relatively large width for ensuring a sufficient saturation margin ($V_{SAT} \geqslant 2V$) at the targeted ON-state current. The biasing voltage V_{BIAS} is tuned in order to provide the correct current while still respecting saturation conditions, such as

$$\begin{cases} V_{SAT} \geqslant V_{BIAS} - V_{th(MOSFET)} \Rightarrow V_{BIAS} \leqslant 2.7V \\ V_{BIAS} \leqslant 4.8V \text{ to be compliant with SOA of transistor } T_{SW} \end{cases} \tag{2.29}$$

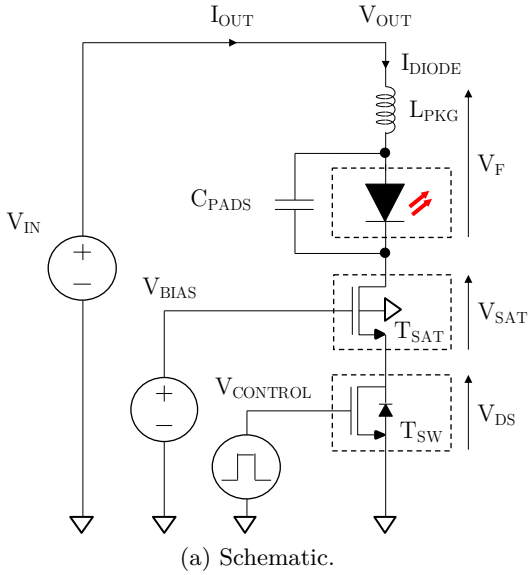
assuming $V_{GS} \simeq V_{BIAS}$. The output voltage V_{OUT} is fixed to 5V, assuming a laser diode forward voltage of around 3V for a maximum ON-state current of 3A. The MOSFET is also triggered by the same control signal $V_{CONTROL}$ as before.

Simulations have been performed in typical conditions for a high ON-state current (3A) and for various frequency values (50MHz and 200MHz). The biasing voltage V_{BIAS} has been set to 2.4V according to the ON-state current, thus satisfying Equation 2.29. Parameters of interest are summarized in Table 2.22b. Transient waveforms such as the current I_{DIODE} through the whole laser diode module, the drain-source voltages V_{DS} and V_{SAT} across the transistors T_{SW} and T_{SAT} respectively, the output voltage V_{OUT}, and the control signal $V_{CONTROL}$ are shown in Figure 2.23.

Parasitic elements have a significant impact on current and voltage transients. Major mechanisms involved during both rising and falling phases are detailed hereafter. Equivalent circuits in Figure 2.24 may help to understand the transient behavior of the circuit. For simplifying the analysis, it has been assumed that transistor T_{SAT} behaves as a current source during the ON state and as an open circuit during the OFF state with three capacitances representing the source/bulk and drain/bulk junction capacitances as well as the gate/source capacitance.

2.5.2.1 Rising phase

The rising phase occurs when the transistor T_{SW} starts turning on (when $V_{CONTROL} \geq 0.7V$), discharging its output capacitance C_{DS} and decreasing its V_{DS} voltage (step 1 in Figure 2.24a). During a very short time, V_{SAT} voltage quickly decreases causing the transistor T_{SAT} to operate in linear region. The current starts to increase. As V_{OUT} remains constant, the laser diode voltage quickly increases accordingly, charging the parasitic capacitances C_{PADS} and C_D through the parasitic inductance L_{PKG}, the series resistance R_S and the MOSFET channels of transistors T_{SAT} and T_{SW} (step 2 in Figure 2.24a). Once these capacitances are fully charged, the diode junction turns on. Then, as the current is still increasing, V_{SAT} increases until the transistor T_{SAT} operates in saturation region



(a) Schematic.

Parameter	Value
Simulation	
V_{OUT}	5V
V_{BIAS}	2.4V
$V_{CONTROL}$	0-3.6V
I_{ON}	3A
f_{MOD}	50MHz & 200MHz
α	50%
t_r / t_f	250ps
MOSFET T_{SAT} (thick-oxide)	
Length / Width	0.5µm / 15mm
$V_{th(MOSFET)}$	0.7V
MOSFET T_{SW} (thick-oxide)	
Length / Width	0.5µm / 50mm
$V_{th(MOSFET)}$	0.7V
$V_{th(BD)}$	0.7V
R_{ON}	40mΩ
C_{DS}	20pF
VCSEL	
$V_{th(VCSEL)}$	1.2V
R_S	490mΩ
I_S	$2.34x10^{-14}$A
n	1.7524
L_{PKG}	700pH
C_{PADS}	5pF

(b) Parameters and extracted values.

Figure 2.22 – Transient simulation bench.

causing the current to be limited at the targeted value (step 3 in Figure 2.24a).

In Figure 2.23, the rising time of the diode current is relatively fast (~1ns at 50MHz and 200MHz). This is mostly due to the relatively high output voltage (5V) that is distributed in preference across the laser diode since both transistors T_{SAT} and T_{SW} operate in linear region during this rising phase. Indeed, a higher voltage across parasitic elements allows a faster charging time. Moreover and in contrast to solution #1, the current has reached its targeted value in both cases. Nonetheless, a saturation margin of around 2V across the transistor T_{SAT} is noticed when the current is settled what causes large conduction losses.

2.5.2.2 Falling phase

The falling phase occurs when the transistor T_{SW} starts turning off (when $V_{CONTROL} \leq 0.7V$), charging C_{DS} and increasing its V_{DS} voltage (step 1 in Figure 2.24b). The current quickly decreases until the diode junction and the transistor T_{SAT} turns off. The two nodes on both sides of transistor T_{SAT} (drain and source nodes) then become floating nodes. At

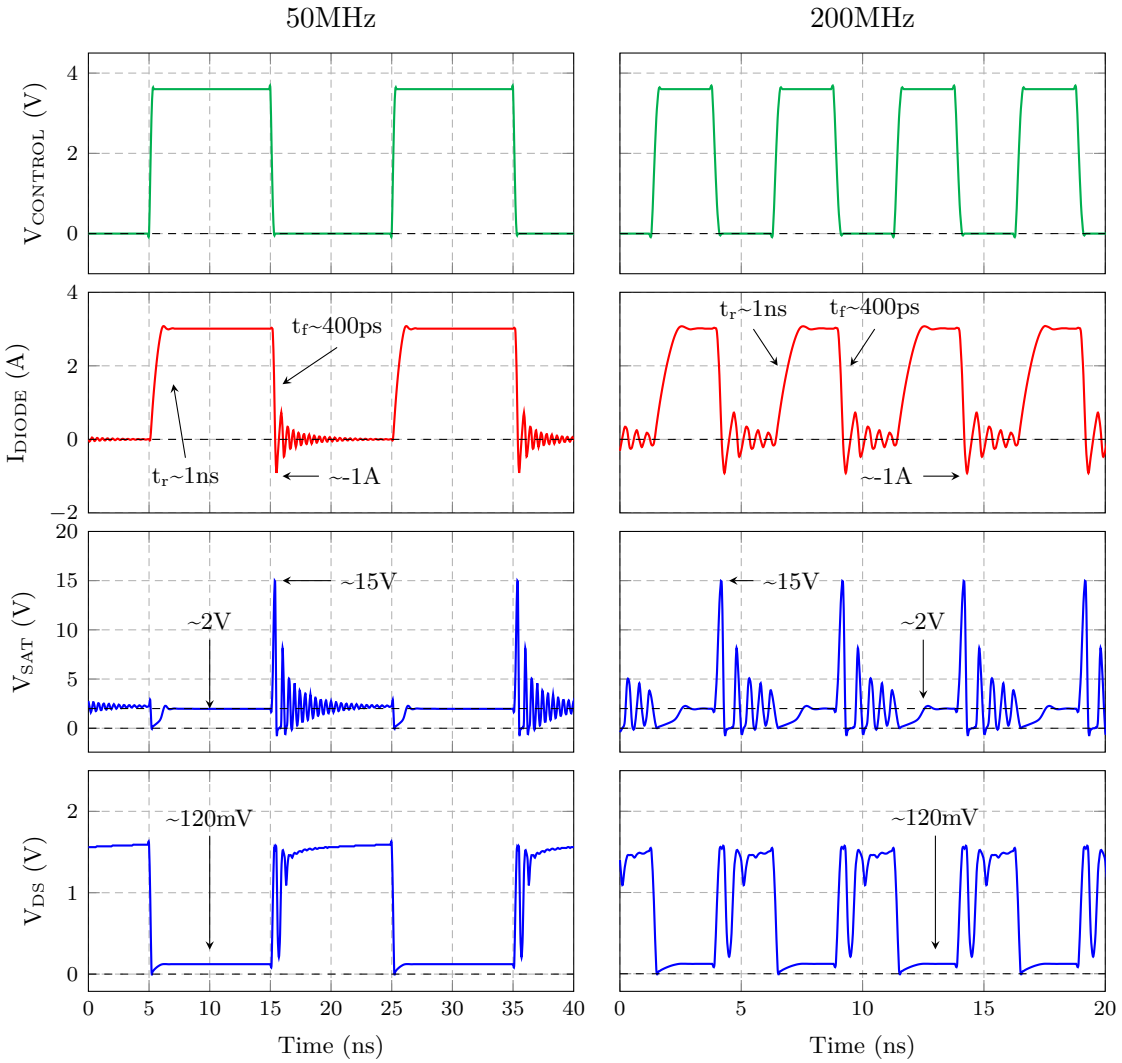
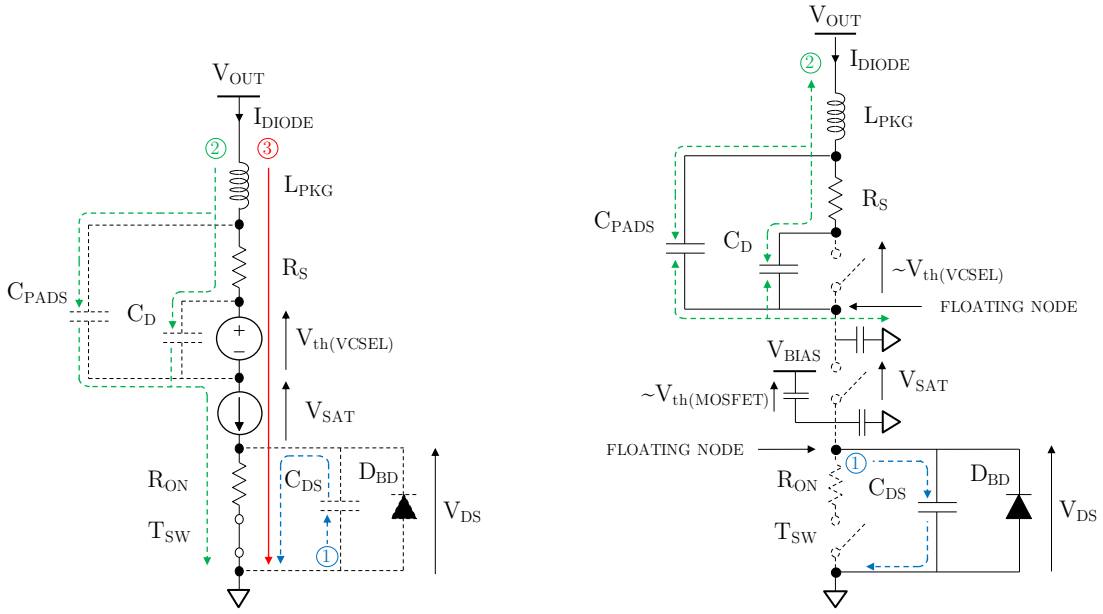


Figure 2.23 – Transient simulation waveforms for $I_{ON} = 3A$ at various frequencies. Typical conditions have been assumed (typ. process, 3.6V, 25°C). V_{DS} and V_{SAT} waveforms are plotted on separate graphs for easy readability.

this point, the circuit seen by the laser diode behaves as a RLC circuit discharging the energy stored in the parasitic inductance L_{PKG} into the drain/bulk junction capacitance of the transistor T_{SAT} through C_D, C_{PADS} and R_S. It may cause V_{SAT} to ring up. Its peak value is reached when the diode current reaches 0 and can be approximated as

$$V_{PEAK} = I_{ON}\sqrt{\frac{L}{C_{OUT}}} \tag{2.30}$$



(a) Rising phase. (b) Falling phase.

Figure 2.24 – Equivalent circuit during the two operating phases.

where L is the equivalent series inductance in the laser diode path and C_{OUT} is the equivalent output capacitance at the drain node of transistor T_{SAT}. The RLC equivalent circuit can be oscillating or not depending on its damping ratio (step 2 in Figure 2.24b), approximated as

$$\zeta_{SERIES(OFF)} = \frac{R}{2}\sqrt{\frac{C_{OUT}}{L}} \tag{2.31}$$

where L and R are the equivalent series inductance and resistance in the laser diode path respectively and C_{OUT} is the equivalent output capacitance at the drain node of transistor T_{SAT}.

In any case and because leakage mechanisms are too complicated to be considered here, floating nodes settle around an operating point satisfying $V_F = V_{th(VCSEL)}$ before to be triggered by the next pulse. Thus, the drain node of transistor T_{SAT} tends to be biased around $V_{OUT} - V_{th(VCSEL)}$ while its source node is kept around $V_{BIAS} - V_{th(MOSFET)}$ due to its input capacitance maintained by the biasing voltage.

In Figure 2.23, a ringing on the current and voltage waveforms is noticed at low and high frequencies. Once again, it is quite complicated to evaluate the impact on the laser signal due to the lack of optical model, but it could be possible that the laser diode emits very short secondary laser pulses during this ringing. High voltage spikes on V_{SAT} (~15V) are

obtained, inducing relatively strong undershoots on the current, reaching around -1A. It is caused by the fast MOSFET turn-offs associated to the parasitic inductances. The falling time of the diode current is around 400ps at 50MHz and 200MHz. In addition, even if voltage spikes may damage the transistor T_{SAT}, it is interesting to see that the transistor T_{SW} seems protected against voltage spikes at its drain and source nodes, due to the cascode structure where the V_{DS} voltage is limited around $V_{BIAS} - V_{th(MOSFET)}$.

2.5.2.3 Summary

In contrast with the two previous solutions, this topology features very good transient performances even with the introduction of parasitic elements. Fast rising and falling times are obtained on the diode current. Nevertheless, high voltage spikes still occur at the switching node when the current is turning on, particularly at high frequency. Minimizing parasitic inductances as previously said could reduce these spikes as well as the potential ringing, while still improving transient performances. Finally, a major drawback of this topology concerns the large conduction losses through the transistor acting as a current limiter, due to its relatively high saturation margin (here $V_{SAT} \geqslant 2V$) (further discussed in Part 2.6.4).

2.5.3 Power management considerations

The purpose here is to address some design issues and give some guidelines for implementing the proposed topology according to specifications described in Part 2.1. The major concern is about the voltage source V_{IN}. It must be capable of providing a constant output voltage taking into account the maximum forward voltage for biasing the laser diode and a sufficient saturation margin for the controlled current source I_{SAT}, while respecting the input voltage range (2.5V-4.8V). Assuming an output voltage larger than 5V, it seems consistent to use a DC/DC converter operating in step-up mode with any voltage conversion ratio while keeping the same polarity. As no galvanic isolation is required, a non-isolated DC/DC converter structure is preferred. The choice of the converter will also be driven by power requirements such as providing a high output current with a high electrical efficiency.

As previously explained in Part 2.3.3, SMPS, against switched-capacitor converters and linear voltage regulators, seem to be the most suitable to use in this context. Conventional SMPS topologies operating in step-up mode include buck-boost type structures (used in step-up mode only) and boost type structures such as the well-known boost converter. More information can be found in [113][126][127]. A standard boost converter consisting of a single inductor, a single capacitor and two switches is considered here. It benefits from less off-chip passive components than other topologies thus reducing PCB footprint. A simplified schematic is illustrated in Figure 2.25. Basically, the output voltage is adjusted by varying the duty cycle D applied to the switches S_1 and S_2. It is assumed that the converter operates in CCM employing a one-phase switching method. Its operating

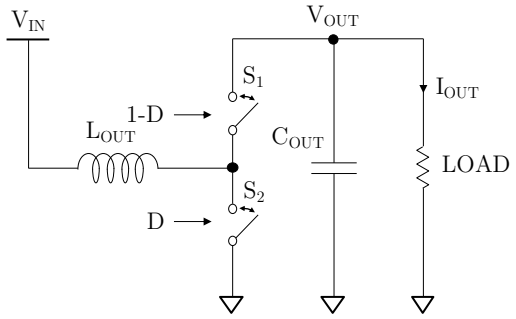


Figure 2.25 – Simplified schematic of the two-switch boost converter.

principle is well detailed in [113]. In an ideal case, the voltage conversion ratio can be expressed as

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D} \tag{2.32}$$

It can be seen that an output voltage too close to the input voltage would lead to a very low duty cycle. For instance, $V_{IN} = 4.8V$ and $V_{OUT} = 5V$ would give a duty cycle of 4% what could impact performances of conventional control strategies such as PWM methods, where a duty cycle greater than 10% is usually recommended [128]. Therefore, an output voltage larger than 5.3V would be required in this context to benefit of good transient performances without increasing the complexity. In addition, it is important to notice that the average current through the inductor is inherently larger than the output current, expressed in an ideal case as

$$< I_L >= \frac{< I_{OUT} >}{1-D} = \frac{\alpha I_{ON}}{1-D} \tag{2.33}$$

So this solution could bring relatively large conduction losses at low input voltage or high duty cycle. For instance and using Equation 2.28 with $\alpha = 0.5$ and $I_{ON} = 3A$, an input voltage of 2.5V would lead to a duty cycle of around 50% inducing an average current of 3A through the inductor.

A simplified schematic of the proposed driver architecture is illustrated in Figure 2.26. It includes the boost DC/DC converter, the laser diode, the cascode transistor acting as a current limiter and the switching element with its driving circuitry. Same recommendations as for solution #1 operating in boost mode can be considered here. The switching frequency of the converter could be selected sufficiently low (f_{SW}<10MHz) compared to the PRF (50MHz-200MHz) in order to benefit from relatively low switching losses and some flexibility for implementing the feedback loop. The output voltage provided by the converter is thus seen relatively constant during the pulse duration leading to a stable ON-state current pulse. An output capacitor with a relatively high value and a low ESR

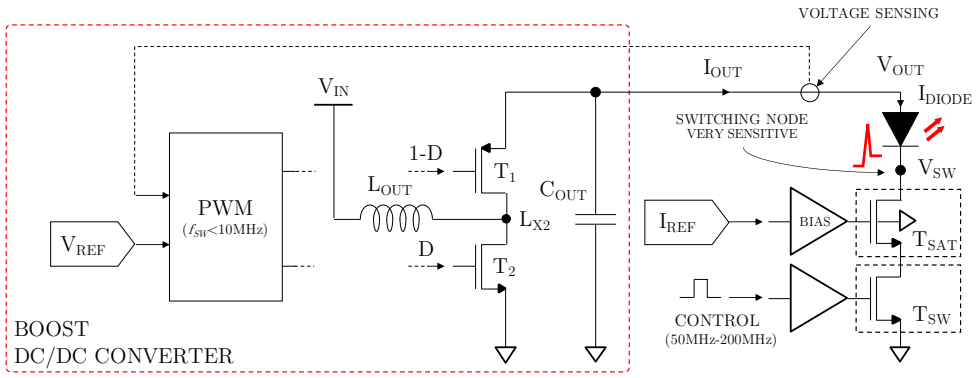


Figure 2.26 – Simplified schematic of the proposed current-mode driver architecture in current limiter configuration.

could be selected for ensuring a low output voltage ripple due to a discontinuous current. The minimum value is given by Equation 2.19. The capacitor must also support the highest voltage provided by the converter. A power inductor with a relatively high value could be selected to maintain a low inductor current ripple while still operating the converter in CCM. The minimum value L_{MIN} is given by Equation 2.20. The inductor also needs to be able to handle the peak switching current without saturating the core. In addition, a relatively high switching frequency (~MHz) could be used to benefit from small components while still ensuring low ripple levels and low conduction losses, but at the expense of increased switching losses.

A standard PWM method using a voltage-control loop could be employed in order to regulate the output voltage with respect to the input voltage range, as described in [129]. Even if the output voltage is supposed to be fixed, using a voltage-level reference could bring some versatility to the structure for adjusting the output voltage and performances, according to the needs. The DC/DC converter thus acts as a voltage-controlled voltage source. The power stage should be implemented using devices capable of handling the maximum inductor current as well as the maximum output voltage. High-voltage devices should be required as the voltage swing can be higher than the thin or thick oxide devices can handle (see Part 2.1.7). PMOS and NMOS devices could be selected for simplifying the driving circuitry.

Finally, the current limiter is implemented using a cascode transistor as previously described. A biasing circuit could be used to adjust the biasing voltage according to the targeted current value set by a current-level reference. However, monitoring the ON-state current is not feasible with a simple design as explained in Part 2.3.3 and monitoring the average current through the diode is not relevant due to the operating principle of the cascode transistor, which controls the ON-state current value. Moreover, conventional techniques for this kind of biasing circuits operating under close-loop control require high-bandwidth error amplifiers [130]. In this context where high frequencies are considered,

it would be quite difficult to design such an error amplifier without involving a complex, large and power-consuming solution [128]. Therefore, a technique under open-loop control is preferred such as a current-mirror structure as described in [74][75]. Even if it is a well-known technique for realizing current limiter in the field of analog design, it would require a very careful design here since the switching element operating at high frequency is included within the structure thus complicating the matching in drain-to-source voltages and channel-length modulation parameter, λ_{MOSFET} [131]. A simplified schematic of the biasing circuit is illustrated in Figure 2.27. The cascode transistor as well as the switching

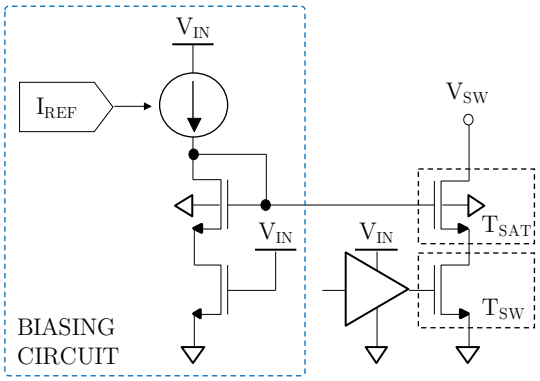


Figure 2.27 – Simplified schematic of the biasing circuit.

element would be implemented with a NMOS devices as described earlier. Since strong constraints are considered here, the implementation is further discussed in Part 3.2.2. In addition, protection circuits such as a clamping circuit need to be used for preventing any damage caused to the laser diode and MOSFET devices.

All these key design parameters are further discussed in Part 2.6.

2.6 Comparative Analysis

This section presents a comparative analysis of the three proposed solutions in order to highlight pros and cons. Indicators such as the design complexity, the silicon area and PCB footprint are discussed using a qualitative analysis while major losses and the theoretical efficiency of each architecture based on previous descriptions are estimated by hand calculations using simplifying assumptions. A ToF metric is also introduced. All indicators are summarized in Table 2.6.

2.6.1 Design complexity

The three proposed solutions are based on well-known architectures including more or less similar functional blocks. As the switching element has similar specifications for all solutions, it is not a key indicator for the comparison in terms of design complexity.

Solution #2 stands out from other solutions in term of design complexity as it presents a relatively simple design. It is based on a buck converter very well detailed in the literature and can be easily designed according to specifications. Moreover, due to its operating principle, the ON-state current of pulses is monitored using a traditional current sensing technique ensuring a relatively high accuracy in contrast with solution #1 monitoring the average current of pulses or solution #3 operating in an open-loop manner. Since three operating modes are considered for the DC/DC converter in solution #1, it requires a PWM controller more complex than that of other solutions but which is still well-detailed in the literature. Despite a well-known cascode current mirror structure used for controlling the current, solution #3 would require a very careful design involving a good matching of transistors while dealing with strong voltage and current variations due to the switching element operating at high frequency.

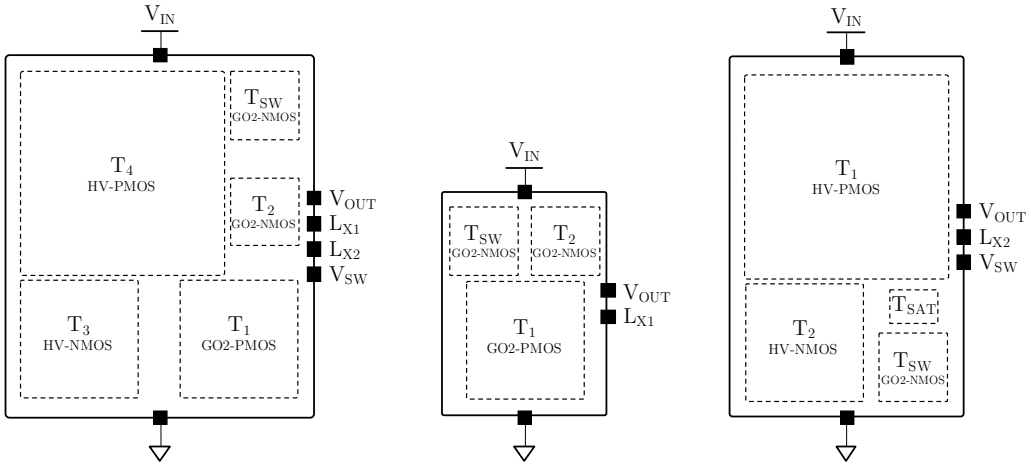
2.6.2 Silicon area and package size

The silicon area occupied by each solution can be estimated according to the size of power devices, which are considered to be very large in front of devices involved in analog and digital functions. In order to get a consistent comparison between solutions and because each power stage has roughly similar specifications, the same on-channel resistance is considered for each power device. The switching element T_{SW} described in previous sections is taken as the reference power device. It is implemented using a thick-oxide NMOS device. Due to the mobility difference between electrons and holes, an PMOS device is usually considered three times larger than an NMOS device for the same on-channel resistance [110]. Considering now a high-voltage NMOS device supporting up to 10V for instance, a width factor of 3 compared to a standard thick-oxide NMOS device (supporting up to 4.8V) for the same on-channel resistance is reported from the design kit. For simplifying the comparison, a factor of 3 between these two devices has been retained. A width factor of 9 between a high-voltage PMOS device (10V) and a standard thick-oxide NMOS device (4.8V) has been retained as well. In this way, it is possible to normalize the estimations according to the silicon area occupied by the switching element, referred as A_{SW}.

Solution #2 features the smallest silicon area as it uses three power devices equivalent to $5A_{SW}$ compared to solution #1 occupying a large silicon area with five power devices equivalent to $17A_{SW}$. Solution #3 also occupies a relatively large silicon area with three power devices and one cascode transistor (accounting for ~$0.3A_{SW}$ as W=15mm) equivalent to $13.3A_{SW}$.

Practically, the size of the chip is also limited by its packaging. As explained in Part 2.1.7, a WLCSP package is considered here where the size is limited by the pitch of solder balls (usually 0.5mm [105]) thus the number of I/Os. Due to thermal effects, several balls can be used for a single I/O especially in power domain where high currents are considered. Since switching elements and power stages of each solution have roughly similar specifications in terms of maximum current for each branch, it is possible to normalize the estimations according to the number of I/Os. Moreover, it has been assumed that each solution requires the same I/Os for analog and digital functions thus they are not taken into account for the comparison. Finally, solution #2 requires at least four I/Os compared to solution #1 and 3 with at least six and five I/Os respectively.

A graphic representation of the estimated silicon area including the number of I/Os for each solution is depicted in Figure 2.28 illustrating that solution #2 is the smallest chip among the proposed solutions.



(a) Solution #1. (b) Solution #2. (c) Solution #3.

Figure 2.28 – Illustration of the estimated silicon area including the number of I/Os for each proposed solution. Drawings are normalized according to the area of T_{SW} (a thick-oxide NMOS device).

2.6.3 PCB footprint

The PCB footprint of each solution can be estimated according to the number and size of components including the chip and off-chip passive components. Nevertheless, it seems quite complicated to estimate the overall size of off-chip components, such as capacitors or power inductors, since many packages exist for components with the same capacitance or inductance value. It also greatly depends on the application type and design specifications

(current and voltage ratings, output voltage ripple, operating frequency, etc...). Regarding the number of components, solution #2 requires a single power inductor. Solutions #1 and #3 require in addition an output capacitor where, practically, some small decoupling capacitors are included to provide current in respond to fast transients. For same reasons, decoupling capacitors are also added at the input node (V_{IN}) but they are not taken into account for the comparison as they are used for all solutions. Therefore, solution #2 requires less footprint than other solutions.

2.6.4 Breakdown of losses and theoretical efficiency

The overall dissipated power and power efficiency can be estimated for each driver by hand calculations with simplifying assumptions in order to get an idea of major contributors. The laser diode is considered as a load here therefore major losses concern the driver. Only electrical quantities are considered for this study. Thus, the theoretical electrical efficiency of a driver is defined by

$$\eta_{ELEC} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \tag{2.34}$$

where P_{OUT} is the average output power provided by the driver to the laser diode (seen as a target here) and P_{LOSS} is total losses from the driver. All these quantities are averaged over the pulse trains only, in order to focus the study when circuits are consuming the most part of the energy as compared to idle times. Here, the average output power can be expressed as

$$P_{OUT} = \alpha V_F I_{ON} \tag{2.35}$$

where α is the modulation duty cycle of the laser diode current, V_F is the laser diode forward voltage and I_{ON} is the ON-state current of the pulse. Total losses can be evaluated by considering conduction losses through passive components including the DC Resistance (DCR) of inductor and the ESR of output capacitor, as well as MOSFET channels (R_{ON}), and switching losses due to switching of MOSFET input and output capacitances (C_{IN} and C_{OUT}). Total losses are given by

$$P_{LOSS} = \sum_i P_{COND(i)} + \sum_i P_{SW(i)} \tag{2.36}$$

$$\text{with } P_{COND(i)} = R_{(i)} I^2_{RMS(i)} \text{ and } P_{SW(i)} = C_{IN(i)} V^2_{IN} f_{(i)} + C_{OUT(i)} V^2_{DS(i)} f_{(i)} \tag{2.37}$$

where $P_{COND(i)}$ and $P_{SW(i)}$ are respectively the average conduction and switching losses of the device of interest when possible. $R_{(i)}$ is the equivalent resistance of the device channel, $I_{RMS(i)}$ is the Root Mean Square (RMS) current through the device, $C_{IN(i)}$ and $C_{OUT(i)}$ are the input and output capacitances of the device resepctively (see Figure 2.29), V_{IN} is the driving circuitry input voltage, V_{DS} is the drain-to-source voltage of the device, $f_{(i)}$ is the switching frequency of the device (either the operating frequency of the power stage

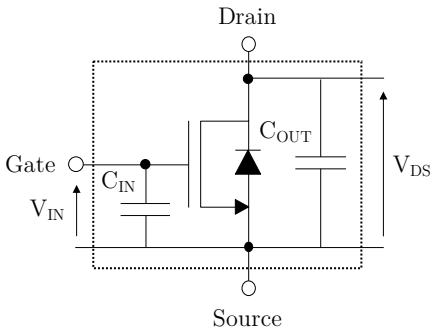


Figure 2.29 – Illustration of MOSFET capacitances.

or the PRF of the switching element). For easy readability, expressions concerning each device for each solution are detailed in Appendix C.

All drivers are evaluated in the same operating conditions for an input voltage from 2.5V to 4.8V. All parameters are listed in Table 2.3. A ON-state current of 3A is targeted with a PRF of 200MHz at 50% modulation duty cycle, leading to an average output power of around 4.5W (4.43W exactly using a 2.95V laser diode forward voltage). As operating principles of drivers are different, an output voltage of 3V is assumed for solution #1 in order to respect Equation 2.7 while an output voltage of 5.5V is assumed for solution #3 in order to respect boundary conditions for the PWM duty cycle described in Part 2.5.3. It leads to a saturation voltage V_{SAT} of around 2.5V. Equation 2.22 gives an average output voltage of 1.5V for solution #2. The switching frequency of the power stage f_{SW}, the inductor L and output capacitor C_{OUT} are arbitrarily chosen while respecting Equations 2.19, 2.20 and 2.27 so that ripple levels are below 20% of output values. This leads to a negligible inductor current ripple ΔI_L simplifying expressions. The parasitic resistance values are also arbitrarily chosen. These choices are not critical since the purpose here is to compare solutions in similar conditions.

In order to evaluate conduction and switching losses of MOSFET devices, all transistors are assumed to be sized as described in Part 2.6.2, taking the switching element T_{SW} as a reference power device. Thus, the same on-channel resistance value is considered for all transistors. On the contrary, the input capacitance value of each device is a direct function of the width. So it can be expressed as a function of the switching transistor input capacitance using width factors described in Part 2.6.2. The on-channel resistance and input capacitance of the switching element have been extracted from the design kit model for various input voltage values. They are plotted in Figure 2.30. As expected, the on-channel resistance is inversely proportional to the input voltage. The input capacitance can be considered relatively constant for an input voltage from 2.5V to 4.8V with a value

Table 2.3 – Operating conditions for evaluating the drivers.

Parameter	Value		
V_{IN}	2.5V - 4.8V		
I_{ON}	3A		
V_F	~3V (2.95V exactly)		
f_{MOD}	200MHz		
α	50%		
P_{OUT}	~4.5W (4.43W exactly)		
	Solution #1	Solution #2	Solution #3
V_{OUT}	3V	1.5V	5.5V
V_{SAT}	-	-	2.5V
f_{SW}	4MHz		
L (DCR)	2µH (50mΩ)		
C_{OUT} (ESR)	1µF (100mΩ)		

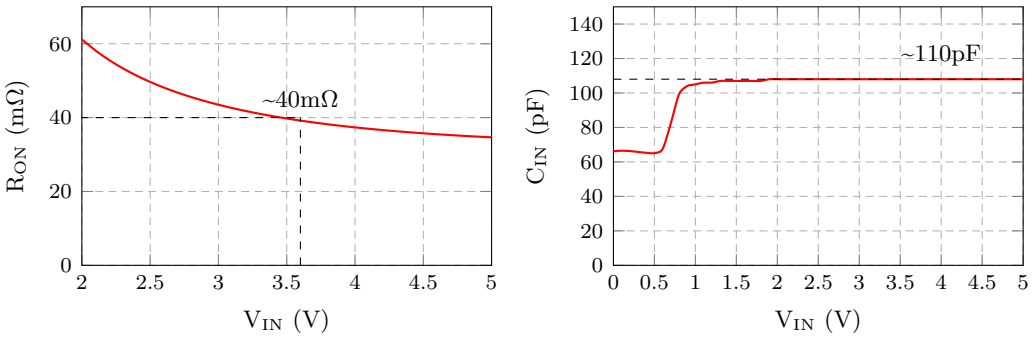


Figure 2.30 – Extracted on-channel resistance (left) and input capacitance (right) of the switching element T_{SW} (L=0.5µm / W=50mm). Typical conditions have been assumed (typ. process and 25°C).

of around 110pF. The output capacitance (accounting for the drain-to-source capacitance) has already been extracted for transient analysis in the previous sections. As its value is relatively small (~20pF) in front of the input capacitance, switching losses related to this output capacitance have been assumed negligible, thus simplifying expressions.

The duty cycle D as well as the inductor current I_L are determined using equations described in Part 2.3.3 for solution #1, in Part 2.4.3 for solution #2 and in Part 2.5.3 for solution #3. Even if these equations are valid for an ideal case without including parasitic elements, it can be used here at first approximation. Since the input voltage varies for the evaluation, the DC/DC converter of solution #1 may operate in different modes. With respect to an output voltage of 3V, it has been assumed to change from boost mode to

buck-boost mode when $D_{BOOST} < 10\%$ and to change from buck mode to buck-boost mode when $D_{BUCK} > 90\%$.

The theoretical efficiency of each driver is presented in Figure 2.31. The breakdown of losses evaluated for each driver at various input voltage values (2.5V, 3.6V and 4.8V) is presented in Figure 2.32. Losses have been split into four specific groups: "power stage" including losses due to MOSFET devices from the power stage, "passive components" including losses due to passive components, "switching element" including losses due to the switching transistor T_{SW} and "cascode transistor" used for solution #3 only including losses due to the cascode transistor.

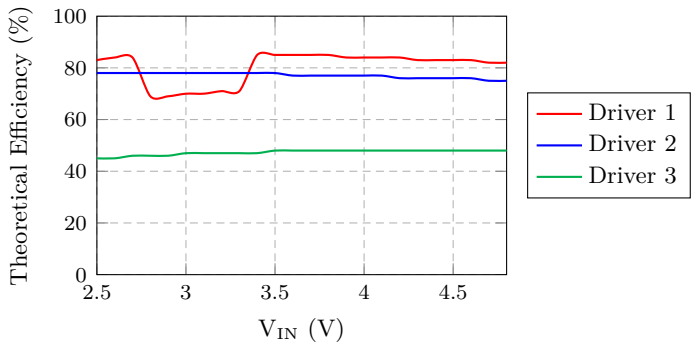


Figure 2.31 – Theoretical efficiency of each driver evaluated over the whole input voltage range for a ~4.5W output power at 200MHz.

Driver 3 has the worst efficiency with a value below 50% over the whole input voltage range. It is caused by the large conduction losses through the cascode transistor accounting for more than 70% of total losses. Driver 1 is more efficient than driver 2 at extremely low or relatively high input voltages (below 2.8V or above 3.4V) while it is the opposite at low input voltages (between 2.8V and 3.3V) where its efficiency drops around 70%. This is due to the different operating modes used by the DC/DC converter causing more conduction and switching losses in buck-boost mode as the four transistors of the power stage are enabled. The inductor current is also high (3A in this case). These losses could be reduced by using a more efficient switching method for the buck-boost mode as proposed in [119][120] but at the expense of an increased design complexity.

It can be noticed as well that losses due to passive components are often significant, particularly for drivers 2 and 3, so it is crucial to select components with low parasitic resistances. Moreover, losses due to the switching element are exactly the same for all drivers what is expected as similar specifications have been assumed. Nevertheless, conduction and switching losses could be minimized by achieving a proper sizing according

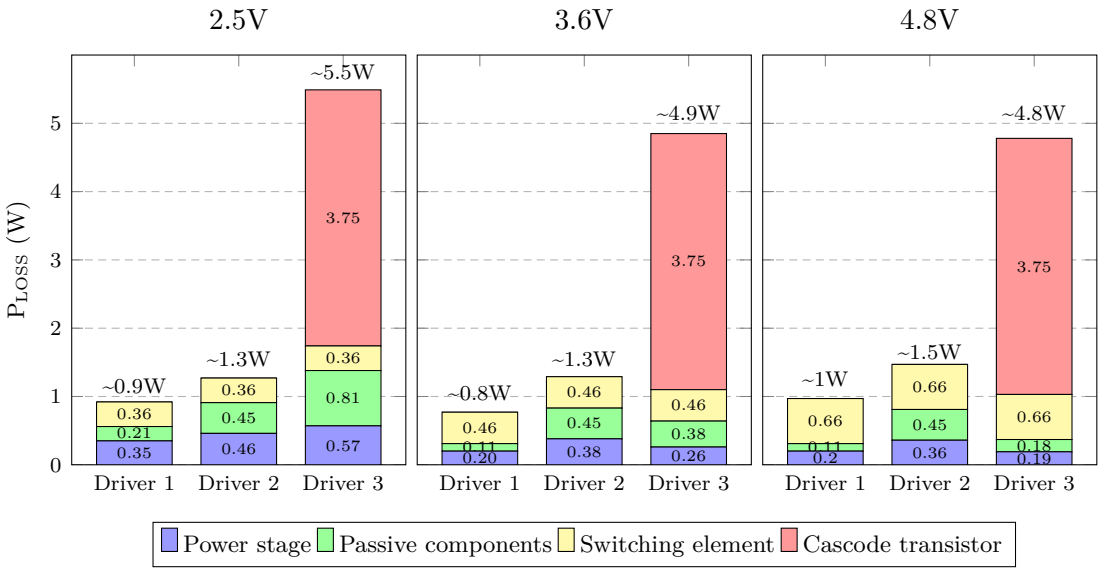


Figure 2.32 – Breakdown of losses for each driver evaluated under various input voltage values for a ~4.5W output power at 200MHz. Total losses are indicated above each bar.

to specifications (further discussed in Part 3.2.2.

2.6.5 Transient performances

As explained in Part 2.3.2.3, in Part 2.4.2.3 and in Part 2.5.2.3, solution #3 features very good transient performances with fast rising and falling times in the diode current in contrast to solution #1 and #2 where either the rising or falling time is greatly impacted by parasitic elements.

It could be interesting to evaluate the impact of the pulse shape on the overall system at the application level, what means considering the ToF sensor for calculating the phase shift then the depth. A figure of merit related to the ToF system could be introduced: the systematic depth error.

2.6.6 Introduction of a ToF metric: the systematic depth error

As explained in Part 2.2, the phase shift measurement is based on the first harmonic of the modulation waveform only. A pulsed laser signal is employed here introducing harmonics through the system that causes a "systematic error on depth". Therefore, it could be interesting to evaluate this error for each solution. The methodology is explained hereafter.

The purpose is to artificially delay an optical transient waveform by means of simulations

for emulating the so-called Time-of-Flight, or phase shift in this case, between an emitted and received laser signal after reflection on an object from the scene. Then, the phase shift calculations are performed on the delayed optical waveform by using the basic iToF sensor model (see Part A.3.3.2). The result is compared to the initial value in order to estimate the phase shift error φ_{err}. It is expressed as

$$\varphi_{\text{err}} = \varphi_{\text{extracted}} - \varphi_0, \text{ with } \varphi_0 \in [0; 2\pi] \tag{2.38}$$

where φ_0 is the initial phase shift value used for delaying the waveform and $\varphi_{\text{extracted}}$ is the phase shift extracted by the iToF sensor model. The error is in fact a relative error: it can be positive or negative thus indicating whether the extracted value is greater or lower than the initial value respectively. Since the phase shift wraps around every 2π, the phase shift error could be evaluated over the whole phase shift range meaning from 0 up to 2π. To be more intelligible, results could be expressed in terms of depth using Equation 1. The depth error D_{err} is then given by

$$D_{\text{err}} = D_{\text{extracted}} - D_0, \text{ with } D_0 \in [0; D_{AMB}] \tag{2.39}$$

where D_0 is the initial depth corresponding to the initial phase shift, $D_{\text{extracted}}$ is the depth extracted by the iToF sensor model and D_{AMB} is the maximum unambiguous range (see Equation A.11). The depth error is then evaluated between 0 and D_{AMB}.

All solutions are evaluated by using the transient simulation benches described in Part 2.3.2 for solution #1, in Part 2.4.2 for solution #2 and in Part 2.5.2 for solution #3. In addition, the optical laser diode model is used in this case to get optical transient waveforms which are a direct function of the diode current as explained in Part 2.1.5. Even if this optical model is not valid for transient simulations, it can give an estimation at first order of the depth errors for comparison purpose. Simulations have been performed in similar conditions as used for the transient analyses. Optical transient waveforms for a 3A ON-state current at 200MHz and a $\frac{\pi}{4}$ phase shift for each solution are shown in Figure 2.33. A 50% modulation duty cycle has been applied on the control signal. As it is for illustration purpose only, waveforms are normalized on y-axis according to their maximum value. Dashed waveforms represent the emitted laser signals while solid waveforms represent the received laser signals so the delayed waveforms. A fourth signal is used representing an ideal pulsed laser signal considered as a reference signal for the comparison.

The depth extraction is achieved using these optical waveforms at 50MHz and 200MHz and over the whole depth range. In a first approach, it is interesting to plot the extracted depth as well as the depth error as a function of the initial depth for the ideal pulsed laser signal (reference signal). Curves at 200MHz are shown in Figure 2.34. The black dashed line on the left curve represents the identity function meaning the depth as a function of itself.

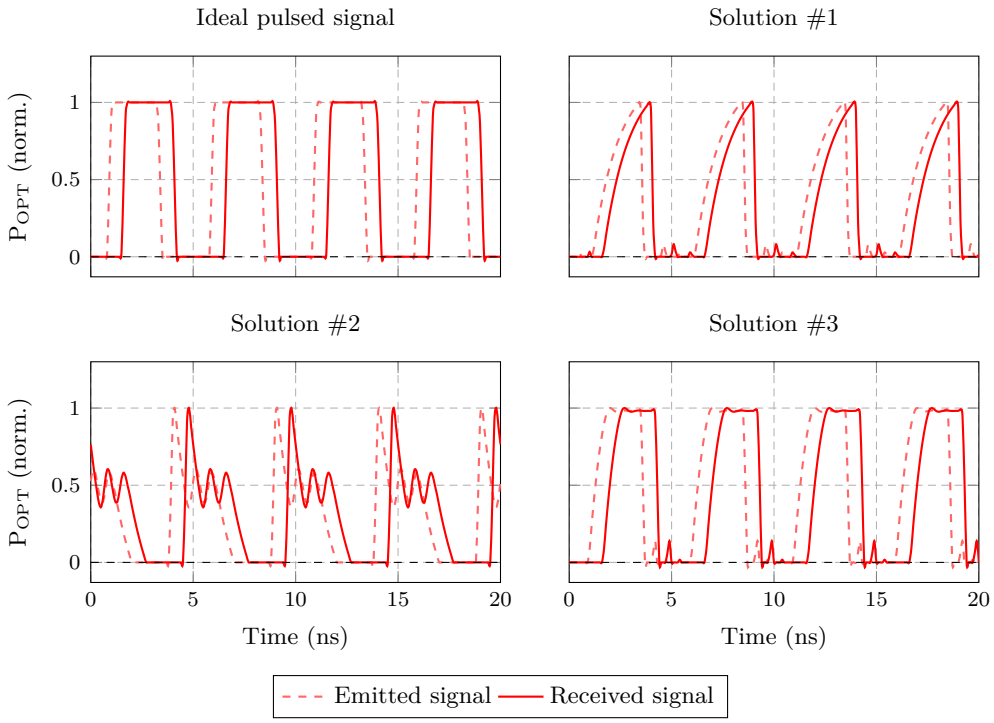


Figure 2.33 – Optical transient simulation waveforms for $I_{ON} = 3A$ at 200MHz and a $\frac{\pi}{4}$ phase shift for each solution. Typical conditions have been assumed (typ. process, 3.6V, 25°C). Waveforms are normalized on y-axis according to their maximum value. For illustration purpose only.

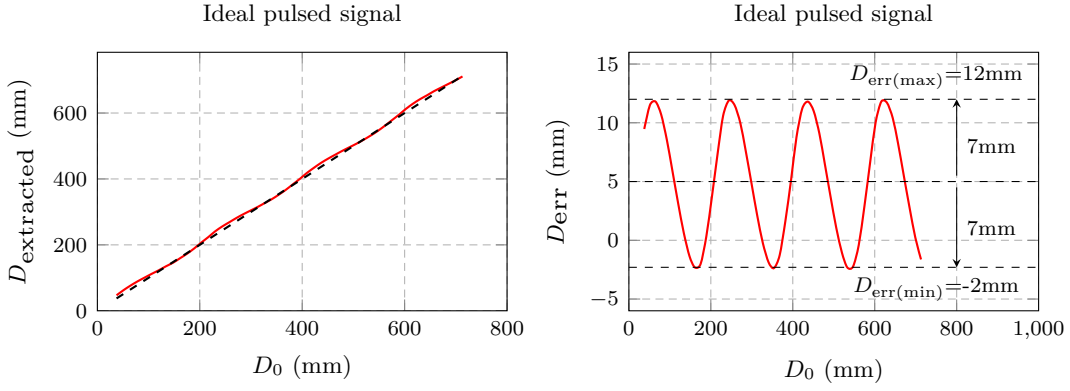


Figure 2.34 – Extracted depth (left) and depth error (right) for the ideal pulsed laser signal at 200MHz. The black dashed line on the left curve represents the identity function.

From Figure 2.34, it can be noticed that the extracted depth for the reference signal is oscillating over the whole depth range what means that the depth error periodically varies

around a given error value with a certain amplitude. In that case, the depth error is about 5mm ± 7mm. Similar results have been observed for the other signals and for various frequencies. In order to fairly compare each solution, it has been chosen to use the depth error amplitude as indicator, which can be expressed as

$$D_{\text{err(amp)}} = \frac{D_{\text{err(max)}} - D_{\text{err(min)}}}{2} \tag{2.40}$$

The depth error amplitude has been evaluated for all solutions including the ideal pulsed signal at 50MHz and 200MHz. A 50% modulation duty cycle has been applied to the control signal. The evaluated depth range for 50MHz is from 0 to 3m while it is from 0 to 0.75m for 200MHz. Values are gathered in Table 2.4.

Table 2.4 – Estimated depth error amplitude of each solution at 50MHz and 200MHz with a 50% modulation duty cycle applied on the control signal.

Frequency	**Depth error amplitude (mm)**			
	Ideal pulsed signal	Solution #1	Solution #2	Solution #3
50MHz	34	31	33	34
200MHz	7	8	8.5	8

The error amplitude is noticed nearly four times lower at 200MHz than at 50MHz what is explained by Equation 1 where the depth is inversely proportional to the frequency. Results are however quite similar for a given frequency except a slight difference for solution #1 at 50MHz. This difference could arises from the distortion on the laser signal causing a slight variation on the duty cycle obtained on the laser signal thus impacting harmonics and the depth error. For that reason, it is interesting to evaluate the depth error amplitude for various duty cycles applied on the control signal in order to sweep a wide range of duty cycle values obtained on the laser signal. Results for 50MHz and 200MHz over a duty cycle range from 20% to 80% are shown in Figure 2.35. Regarding solution #2, results have been rearranged taking into account the phase opposition between the control signal and the laser signal. For instance, a 20% duty cycle on the control signal indicated hereafter actually suggests a 80% duty cycle on the control signal for the solution #2 only.

From figure 2.35, it can be noticed that the depth error amplitude for an ideal pulsed laser signal is symmetrical regarding a 50% duty cycle and is minimized for a duty cycle of 33% and 66%, for both 50MHz and 200MHz cases. Considering now the signals from the solutions at 50MHz, the error amplitude curves are similar to that of the ideal pulsed laser signal with a slight deviation around 60% for solution #1 and around 40% for solution #2. It means that the distortion brought by parasitic elements on the laser signal of each solution is relatively insignificant at low frequencies. On the contrary, results at 200MHz

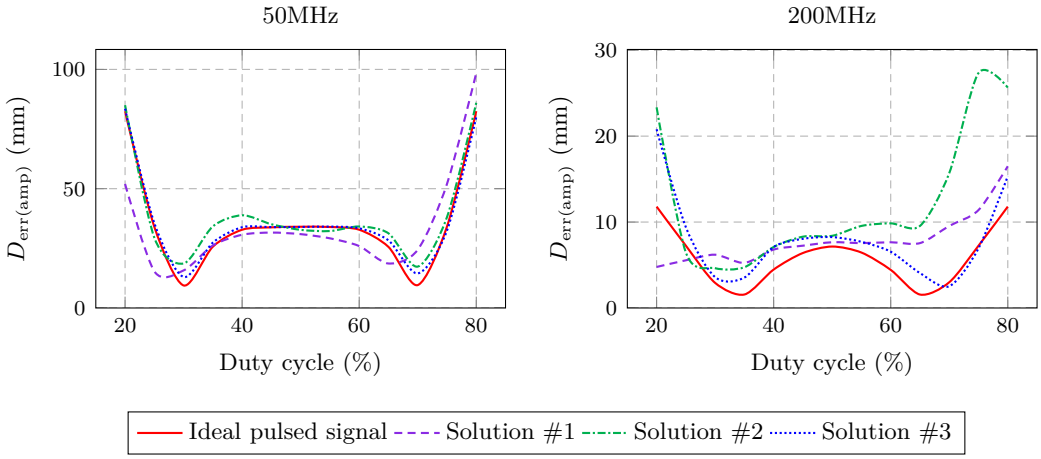


Figure 2.35 – Estimated depth error amplitude for each solution over a wide duty cycle range (20%-80%).

are quite heterogeneous for solutions 1 and 2 particularly at high duty cycle values while results for solution #3 are relatively similar to that of the ideal pulsed laser signal.

All solutions show relatively similar performances in terms of accuracy related to the systematic depth error at low frequencies. At high frequencies, solution #3 features better performances than other solutions when considering a duty cycle above 50%. In that case, the depth error amplitude for solution #2 is relatively large. For a duty cycle below 50%, the error amplitude for solution #1 seems to be relatively constant while it strongly increases for solutions 2 and 3 at extremely low duty cycle values.

Finally, the average value of estimated depth error amplitude values over the whole duty cycle range could be used as final indicator for comparing each solution. Values are gathered in Table 2.5. It can be noticed that solutions 1 and 3 essentially feature a lower average depth error amplitude than solution #2 over the whole duty cycle range.

Table 2.5 – Average value of estimated depth error amplitude values over the whole duty cycle range (20%-80%) for each solution at 50MHz and 200MHz.

Frequency	**Average depth error amplitude (mm)**			
	Ideal pulsed signal	Solution #1	Solution #2	Solution #3
50MHz	72	69	79	74
200MHz	12	16	25	16

2.7 Discussion

All key performance indicators for each proposed solution are listed in Table 2.6. Indicators have been summarized using a qualitative approach based on results previously described. They are stated relative to each other and must be considered for the scope of this preliminary study only. For instance, the complexity of solution #2 is low compared to other solutions presented here, but it does not indicate that solution #2 has a low complexity in absolute terms. About the discussion for choosing the most suitable solution with respect to the specifications, it must be reminded that a high power efficiency is considered as a leading requirement.

Table 2.6 – Summary of KPIs for each proposed solution. Best indicators are colored in green.

Indicators	**Solution #1** Voltage-mode driver in series configuration	**Solution #2** Current-mode driver in shunt configuration	**Solution #3** Current-mode driver in current limiter configuration
Complexity	medium	low	relatively high
Silicon area	large ($17A_{SW}$)	small ($5A_{SW}$)	medium (~$13A_{SW}$)
minimum number of I/Os	big (6)	small (4)	medium (5)
PCB footprint	large	medium	large
Efficiency	high (~84% in buck and boost mode, ~70% in buck-boost mode)	relatively high (~77%)	very low (~47%)
Transient performances	poor	poor	very good
Systematic depth error	good	poor	very good

It is seen that solution #2 stands out from other solutions presenting a simple and compact design with an integrated circuit potentially small including few off-chip components. However, poor transient performances are noticed where the falling time of the current through the laser diode is greatly impacted by parasitic elements that may cause some distortion in the laser signal. Indeed, a relatively large systematic depth error has been estimated for a duty cycle above 50% at high frequencies compared to solutions #1 and #3. Regarding now specifications where a duty cycle around 50% is required, transient performances for solution #2 seems acceptable. Another important point is that a relatively high efficiency is reported over the whole input voltage range with an average value around 77%, making this solution potentially well suited for designing the laser diode driver.

Although very good transient performances have been noted for solution #3 compared to solutions #1 and #2, a very low efficiency below 50% has been estimated for this solution due to the use of a cascode transistor operating in saturation region. As a consequence, it is not a feasible solution for the laser diode driver with respect to targeted

objectives.

The discussion is more complicated regarding solution #1. Whereas a large integrated circuit occupying a large PCB footprint seems necessary due to the use of a buck-boost converter, good performances in terms of efficiency and power losses have been estimated but not over the whole input voltage range. Actually, the efficiency drops down to 70% in buck-boost mode. Nevertheless, a low systematic depth error very close to results for an ideal laser signal is noticed when considering a duty cycle around 50% at low and high frequencies, even with a rising time of the laser diode current impacted by parasitic elements. As the efficiency is a leading requirement in this context, this solution seems to be a good candidate for the laser diode driver as well. Moreover, it could be considered to investigate on another type of buck-boost architecture in order to improve the efficiency in buck-boost mode even if it is at the cost of the design complexity.

It must be reminded that the depth error indicator must be considered with caution since it has been evaluated from transient simulations using the optical laser model only valid for DC simulations. For that reason, it is quite complicated to conclude on the optical behavior of solutions #1 and #2, particularly at application level through the depth error indicator. Therefore, it has been decided to pursue the work by choosing both solutions as a basis for the laser diode driver prototype in order to draw a conclusion based on measurement results obtained.

Conclusion

This chapter has presented a preliminary design study for evaluating the feasibility of several driver architectures based on the state-of-the-art topologies. A comparative analysis using various indicators has been performed to point out pros and cons of each solution. It indicates that the solution proposing a current-mode driver in current limiter configuration is unsuitable in the thesis context due to the potential huge conduction losses through the transistor operating in saturation region. The other solutions proposing a voltage-mode driver in series configuration as well as a current-mode driver in shunt configuration seem both well suited for designing the laser diode driver. However, this preliminary design study has shown some limits for choosing a single solution, in particular due to the unavailability of an accurate optical model for the laser diode. Thus, it is proposed to implement both solutions that will be referred to as voltage-mode and current-mode drivers thereafter.

The study has also identified the major power losses' contributors, such as the switching element, power stage and passive components. By the way, off-chip passive components must be considered here in order to handle currents of few Amps, making the solution not fully integrated. But it seems the best trade-off in order to benefit from a simpler and cheaper implementation compared to integrated passive components. Some design trends have been noticed as well such as using suitable MOSFET devices and protection circuits

for dealing with high voltage spikes during fast transients due to parasitic inductances. In addition, a pre-bias current source could be considered in order to reduce the optical turn-on delay.

3 Design of the Integrated LDD Prototype

Contents

This chapter describes the design and implementation of the laser diode driver prototype using the hcmos9a analog and mixed signal process. The contribution of the work concerns the integration of the driver as a **single chip**, including the power management solution but excepting the laser diode and some passive components. Both the voltage-mode driver in series configuration and the current-mode driver in shunt configuration have been selected as the basis for the LDD as explained in the previous chapter. Some considerations are presented before to give details about the design and layout of the IC prototype with a focus on the switching element and the driving circuitry.

3.1 Design Considerations

The proposed voltage-mode or current-mode driver architectures presented in Chapter 2 rely on similar building blocks. A global view of the systems is depicted in Figure 3.1. Based on power management considerations as explained in Parts 2.3.3 and 2.4.3, both drivers comprise:

- A DC/DC converter for biasing the laser diode. It includes a power stage, an output filter and a standard PWM circuit using a feedback loop in order to adjust the output voltage or current according to the desired current set by a current-level reference

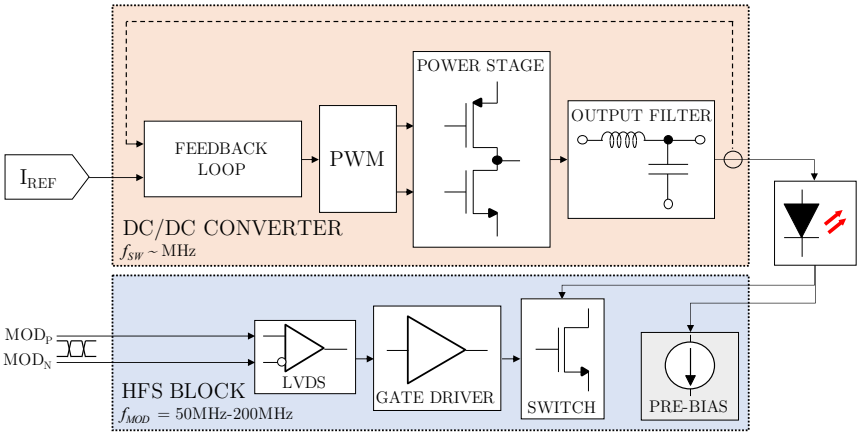


Figure 3.1 – Global view of the drivers with major building blocks. The pre-bias current source is intended for the voltage-mode driver only.

I_{REF}. The output filter is made of a LC filter or a single power inductor for the voltage-mode and current-mode drivers respectively.

- A High-Frequency Switching (HFS) block for switching the current through the laser diode. It includes a switching element driven by an external differential modulation signal (inputs MOD_P and MOD_N) through an appropriate driving circuitry. It consists of a gate driver and a Low Voltage Differential Signaling (LVDS) receiver. In addition, a current source may be employed for the voltage-mode driver only, in order to pre-bias the laser diode for reducing the optical turn-on delay.

The converter can operate at a relatively low frequency (f_{SW}~MHz) compared to the modulation frequency of the HFS block (f_{MOD}=50MHz-200MHz). Some considerations for the building blocks are detailed hereafter.

3.1.1 DC/DC converter

Since some design choices for the DC/DC converters are conventional, it has been decided to reuse an IC issued from previous developments in order to save time and design resources. This chip is well suited to implement both the voltage-mode and current-mode drivers as it embeds two charge-pump assisted non-inverting buck-boost DC/DC converters. One of the buck-boost converter could be used as it is delivered to implement the DC/DC converter of the voltage-mode driver while the other one could be used in step-down operating mode only and working without output capacitor in order to implement the DC/DC converter of the current-mode driver. In this way, only a single chip can be realized.

The two converters have an hybrid structure made of a typical buck converter ensuring step-down operations, associated to a switched-capacitor stage ensuring step-up

operations. In contrast with a four-switch non-inverting buck-boost converter, this structure allows to reach a higher efficiency but at the cost of an additional off-chip capacitor. The converter architecture and its operating principle are not detailed here. It can be seen as a **block able to step up or step down the output voltage according to the desired current**. Quick details are however given in Part 3.2.1.

Each converter includes a standard analog PWM controller working at a fixed operating frequency of 4MHz (imposed by design) with feedback loops. It is able to provide a programmable current up to 3A in steady-state mode. The settling time is in the order of few tens of µs. Thanks to the hybrid structure, the boost mode allows an output voltage up to 1.5 times the input voltage, which varies from 2.5V to 4.8V, in order to employ a wide range of loads. The IC has been designed in the hcmos9a process and is packaged in a WLCSP with an array pattern of solder balls (also referring to as bumps). Finally, the same HFS block could be employed for both drivers since it has similar specifications, in order to save silicon area for the IC prototype. However, a special care should be taken at circuit and system levels to make sure that only one driver works at a time.

3.1.2 HFS block

3.1.2.1 Modulation signals

The HFS block aims to switch the current through the laser diode according to a control signal with a modulation frequency up to 200MHz. The LVDS technique, capable of transmitting data at high speeds with low power dissipation, is well suited in this context [132]. A transmitter provides a differential signal with a common mode voltage through a transmission line while a receiver, acting as a comparator, recovers the modulation signal from the differential signal. More details about this technique can be found in [133].

It has been chosen to provide an external differential modulation signal as a control signal to the driver through inputs MOD_P and MOD_N (see Figure 3.1). A LVDS receiver is thus essential in order to convert this differential signal into a single-ended modulation signal that is then delivered to the switching element through an adequate gate driver.

3.1.2.2 Switching element and protection circuits

The high-frequency switching element plays a key role in the driver behavior. It is implemented using a NMOS device, as explained in previous chapters. The design kit proposes several NMOS devices intended for digital, analog or power functions. They feature various structures, which allows to withstand different operating voltages. Five devices are available:

- n-channel 1.2V MOSFET with thin oxide (referring to as GO1, see Part 2.1.7),
- n-channel 4.8V MOSFET with thick oxide (referring to as GO2, see Part 2.1.7),

- n-channel 6V drain-extended MOSFET with thick oxide (referring to as DEMOS),
- n-channel 10V Drift-MOSFET with thick oxide (referring to as Drift),
- n-channel high voltage 18V Drift-MOSFET with thick oxide (referring to as HVDrift 18V).

At least 21 manufacturing steps (also known as masks) are necessary for thin oxide devices (GO1). Other devices require additional steps depending on their structure. They are not detailed here. More information are provided in [104]. Characteristics of interest are listed in Table 3.1.

Table 3.1 – Characteristics of NMOS devices available in the hcmos9a process.

Characteristics					
Device	GO1	GO2	DEMOS	Drift	HVDrift 18V
Oxide thickness	2.3nm	8.5nm			
Min gate length	130nm	500nm			
Threshold voltage	~0.7V				
Max gate driving voltage	1.2V	4.8V			
Max supported voltage at drain	1.32V	4.8V	6V	10V	18V
Mask count	21	26	28	28	27

The selection of a suitable device for the switching element, as well as its sizing with respect to the specifications, are very important design steps. A comparative study of devices could be performed according to several indicators such as the total dissipated power under normal operation, gate oxide area, design complexity and cost of manufacturing steps. Transient performances such as rising and falling time are not considered here since they greatly depends on parasitic inductances. Another important requirement concerns the voltage withstand at the device drain (also referred to as the switching node V_{SW} in this manuscript), which is mostly impacted by high voltage spikes during fast transients due to the stray inductance arising from packages and PCB interconnection. As explained in previous chapters, using suitable protection circuits such as a clamping diode is necessary in order to prevent any damage caused to the laser diode and devices within the chip. It exists two types of diodes available from the design kit:

- a conventional P-N junction diode with around 0.7V threshold voltage and a 10V breakdown voltage,
- a Schottky diode with around 0.3V threshold voltage and a 20V breakdown voltage.

Their structure are further detailed in Part 3.3.8. Unfortunately, diode models provided by the design kit are incomplete, the series resistance and/or diffusion capacitance not being taken into account. It would lead to DC and transient simulation results not sufficiently accurate to select the appropriate device. For that reason and because a device

characterization process would have been incompatible with the design schedule related to the industrial context, it has been decided to realize several IC prototypes implementing each a different diode for testing in real conditions.

3.1.2.3 Pre-bias current source

As quickly discussed in Chapter 1, when pulsing the current through a laser diode, an inherent delay occurs between the electrical and optical pulses. This phenomenon is due to the time needed for the carrier density to reach its threshold value for the laser emission. Said in another way, it corresponds to the time needed to go from spontaneous emission to stimulated emission [83][134]. It is expressed as

$$t_d = \tau_n \frac{I_{ON} - I_{OFF}}{I_{ON} - I_{th}} \tag{3.1}$$

where τ_n is the carrier lifetime, I_{ON} is the ON-state current, I_{OFF} is the OFF-state current and I_{th} is the threshold current. The turn-on delay can be reduced by biasing the laser diode just below the threshold current during the OFF state. Applying a biasing current, often referred to as a pre-bias current, can also minimize the oscillations appearing during the rising phase of the laser pulse (called relaxation oscillations) and reduce thermal variations [41][135].

For these reasons, it seems interesting to implement a pre-bias current source. A programmable current could be considered to accommodate VCSEL characteristics due to thermal and manufacturing process variations as well as to keep some design flexibility. This feature will be investigated for the voltage-mode driver only. Some lines of inquiry related to the current-mode driver topology in shunt configuration are approached in [135] but not discussed in the present work.

3.2 Design Details

Since the design and implementation of both voltage-mode and current mode drivers into a single chip are quite ambitious within short time constraints related to the industrial context, the breakdown of work has been distributed through different members within the department "Analog, MEMS and Sensors" at STMicroelectronics. The major contribution of the thesis at design level concerns the switching element, its driving circuitry and protection circuits. Following sections focus on theses blocks. Other blocks such as the DC/DC converters, the pre-bias current source and I/O pads are however quickly presented.

3.2.1 DC/DC converters

3.2.1.1 Voltage-mode driver

One charge-pump assisted non-inverting buck-boost DC/DC converter, including a PWM controller and current-control and voltage-control loops, is used as it is delivered to implement the current-controlled voltage source required by the voltage-mode driver architecture, as defined in Part 2.3.3. Even if a current-level reference is used here to set the desired current, the converter output has a low impedance when considering a low operating frequency (f_{SW}=4MHz) compared to the modulation frequency of the HFS block (f_{MOD}=50MHz-200MHz). The driving mode of the diode is still considered in voltage mode. A simplified block diagram of the converter is depicted in Figure 3.2.

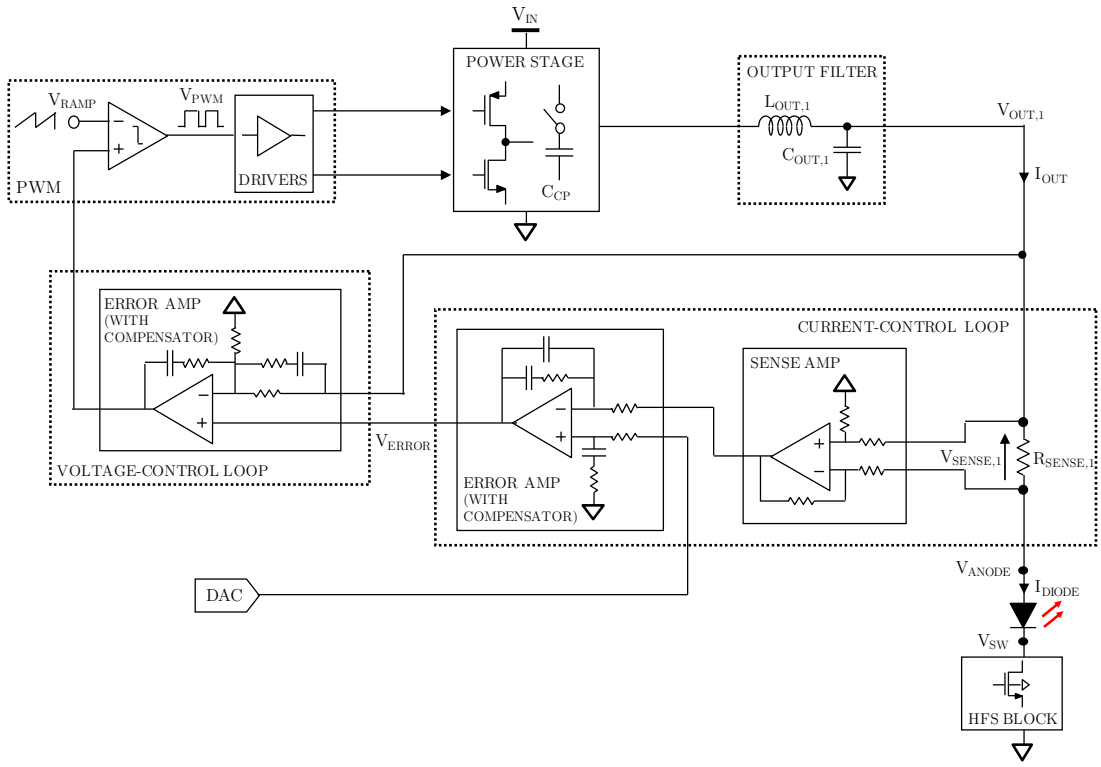


Figure 3.2 – Simplified block diagram of the DC/DC converter for the voltage-mode driver.

Power stage It transfers the power from the input supply to the output filter, according to switched signals provided by the PWM controller. The power stage has an hybrid structure made of a typical power stage of a buck converter associated to a switched-capacitor stage for step-up operations. Due to confidentiality, the structure and implementation are not provided in the present manuscript.

Output filter It smooths the output current and voltage. It includes a power inductor ($L_{OUT,1}$) and an output capacitor ($C_{OUT,1}$) for the buck converter as well as an additional capacitor (C_{CP}) for the switched-capacitor stage. It is reminded that they are off-chip components. They have been inherently selected from requirements of the reused DC/DC converter to ensure a proper operation. Characteristics are listed in Table3.2.

Table 3.2 – Component characteristics for the voltage-mode driver.

Function	Value	Manufacturer	Part number	Type	Rated voltage or current	Temperature characteristics	Size
Power inductor ($L_{OUT,1}$)	470nH	TDK	TFM201610ALM-R47MTAA	Thin Film Metal	5.8A	-40°C to 125°C	20mm x 16mm
Output capacitor ($C_{OUT,1}$)	4.7µF	Murata	GRM188C81E475KE11	MLCC	25V	X6S	1608M
Charge-pump capacitor (C_{CP})	4.7µF	Murata	GRM188C81E475KE11	MLCC	25V	X6S	1608M

Feedback loops It ensures a proper regulation of the output current according to the desired current. In this context, the current that must be monitored is the laser diode current. Nevertheless, a conventional current sensing technique is already implemented here, allowing to monitor the average current through the laser diode only, as explained in Part 2.3.3. The ON-state current value of the pulse is thus controlled by the modulation duty cycle of the control signal (see Equation 2.21).

A sense resistance $R_{SENSE,1}$ is inserted in series with the laser diode. The resistance value (~100mΩ) has been chosen according to a trade-off between the sensing loop accuracy, the voltage drop and conduction losses across the resistance for different load conditions. Then, an error amplifier compares the sense amplifier output voltage with a reference voltage, provided by a Digital-to-Analog Converter (DAC), as a function of the desired current. It generates an error voltage that is compared to the output voltage using a second error amplifier, thus generating a second error voltage used by the PWM controller. Compensators are included within error amplifiers in order to improve the feedback loop stability.

PWM controller It provides PWM signals to the power stage, through gate drivers. The error voltage is compared to a ramp waveform in order to generate PWM signals, that are used to control the power stage.

3.2.1.2 Current-mode driver

The other charge-pump assisted non-inverting buck-boost DC/DC converter is used in step-down operating mode without the output capacitor in order to implement the current-controlled current source required by the current-mode driver architecture, as defined in Part 2.4.3. It includes a PWM controller and a current-control loop. The switched-capacitor stage is unnecessary here. A simplified block diagram of the converter is depicted in Figure 3.3. The building blocks have similar roles as in the voltage-mode driver. They however slightly differ in their implementation as the converter must be modified to fulfill specifications related to the current-mode driver.

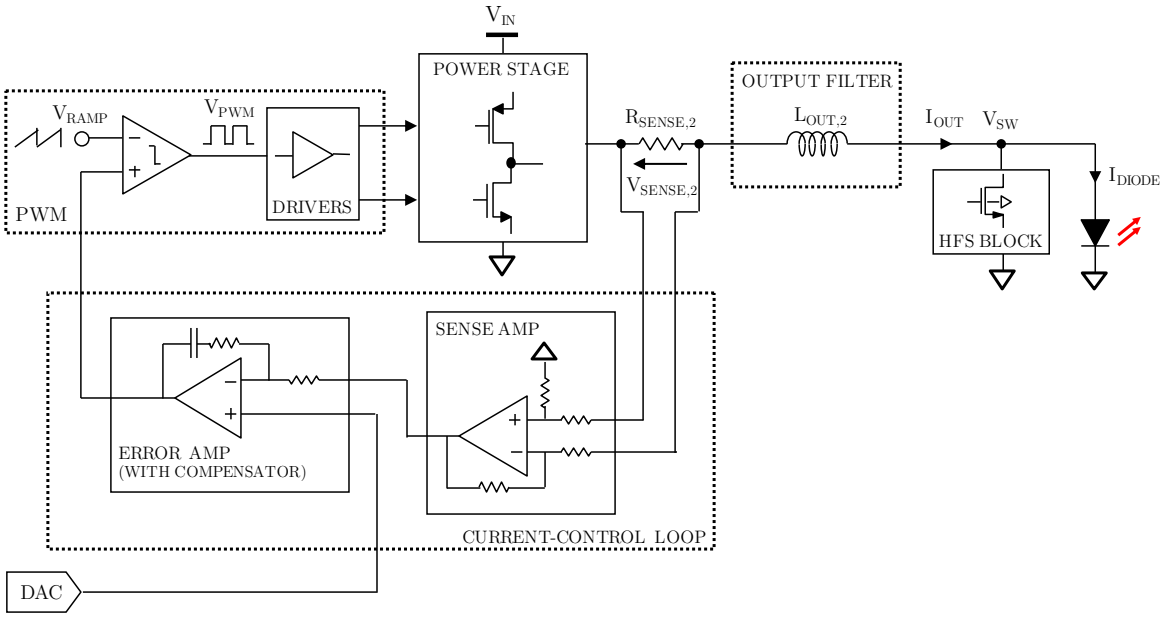


Figure 3.3 – Simplified block diagram of the DC/DC converter for the current-mode driver.

Power stage It has the typical structure of a standard buck converter, including two switches (see Figure 2.20). Due to confidentiality, implementation details are not provided in the present manuscript.

Output filter It only includes an off-chip power inductor ($L_{OUT,2}$). Since modifications are necessary here, its value is derived from Equation 2.27. Assuming a maximum inductor current of 3A, a maximum input voltage of 4.8V and an operating frequency of 4MHz, a minimum 1µH inductance value is required in order to maintain the ripple under 10% of the inductor current. The power inductor must be selected with a rated current higher than 3A and a low DC resistance. Its characteristics are listed in Table 3.3.

Table 3.3 – Component characteristics for the current-mode driver.

Function	Value	Manufacturer	Part number	Type	Rated voltage or current	Temperature characteristics	Size
Power inductor ($L_{OUT,2}$)	1µF	TDK	TFM201610ALM-1R0MTAA	Thin Film Metal	4.3A	-40°C to 125°C	20mm x 16mm

Current-control loop and PWM controller In this context, the current that can be monitored is the average current through the inductor since it directly corresponds to the ON-state value of the current pulse through the laser diode, as explained in Part 2.4.3. This approach benefits from the conventional current sensing technique already implemented.

A sense resistance $R_{SENSE,2}$ is inserted in series with the power inductor. It is placed on the left side of the inductor to be immune, as much as possible, to fast transients due to the high-frequency current switching from the HFS block. The resistance value (~40mΩ) is lower here because the inductor current is higher than the average current sensing through the laser diode in the voltage-mode driver topology. Its value has also been chosen according to a trade-off between the sensing loop accuracy, the voltage drop and conduction losses across the resistance for different load conditions. The gain of the sense amplifier and the compensator of the error amplifier are slightly different to meet current and voltage specifications. Finally, the principle of the current-control loop is similar to that of the voltage-mode driver explained earlier.

3.2.2 Switching element and protection circuits

An important requirement for selecting the NMOS device as a switching element concerns the voltage withstand at its drain node. That depends on voltage constraints imposed by both the voltage-mode and current-mode drivers as well as the implementation of protection circuits. It is firstly proposed to discuss protection circuits, then NMOS devices comparison in order to fully consider all requirements. Lastly, the sizing step is presented.

3.2.2.1 Protection circuits

One solution to overcome high voltage spikes during fast transients is to add a clamping diode. Its main purpose is to evacuate the residual energy from parasitic inductances while preventing the switching node to exceed a maximum supported voltage. Several ways are possible to use a clamping diode:

- Connecting the diode between the switching node and the ground, ideally triggering when the voltage spike is larger than the clamping diode threshold voltage. A Zener

diode is usually employed in a reverse biasing mode. A stacking of conventional P-N diodes in a forward biasing mode may be considered as well.

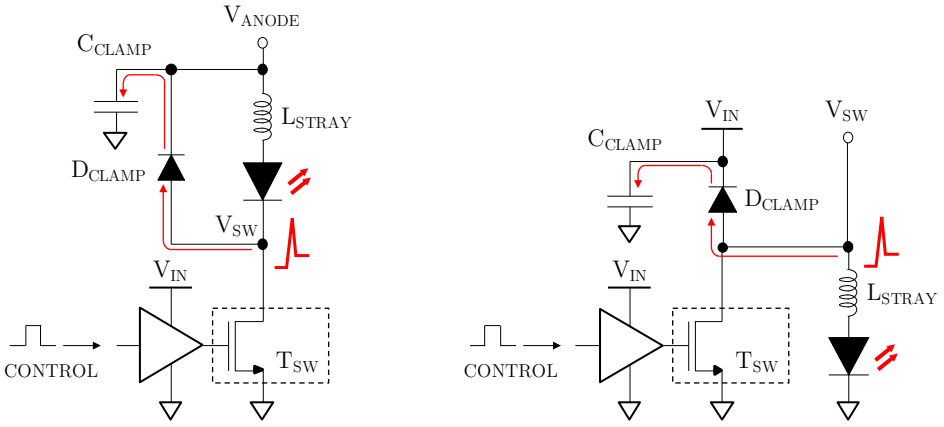
- Connecting the diode between the switching node and a specific clamping voltage, ideally triggering when the voltage spike is larger than the clamping voltage plus the diode threshold voltage.

It can be noticed that both approaches add extra parasitic capacitances at the switching node. The second approach is preferred in this work since no Zener diode is available for implementing the first approach, and because a large number of P-N diodes would be required to build a stacking of diodes, thus increasing the silicon area. Considering now the second approach, the clamping voltage V_{CLAMP} depends on the driving mode. Figure 3.4 depicts the proposed solution for both voltage-mode and current-mode drivers.

Voltage-mode driver The anode voltage is preferred as the clamping voltage because, depending on operating conditions, it can be the highest voltage within the circuit, particularly in boost mode where a 7.2V output voltage can be reached. In this way, this avoids current leakage through the clamping diode if another lower specific voltage would be used. On the other hand, the switching element should be able to withstand voltages higher than 7.2V.

Current-mode driver The input voltage (2.5V-4.8V) is preferred as the clamping voltage over a specific voltage in order to simplify the design. In this way, no voltage regulator (usually LDO regulator) is required thus silicon area and/or PCB footprint can be saved. However, the switching element should be able to withstand voltages higher than the maximum input voltage (4.8V).

Since both voltage-mode and current-mode drivers share the same HFS block, a special care should be taken at circuit levels to implement these two different clamping paths. Some small capacitors (C_{CLAMP}) should be included at the clamping voltage (either the anode voltage or input voltage) for an effective decoupling (further discussed in Part 3.3.10). Furthermore, the most restrictive voltage constraint is retained as a requirement for selecting the switching element, namely supporting a voltage higher than 7.2V. It is also noticed for the current-mode driver that a low input voltage (2.5V) may unintentionally trigger the clamping diode if the clamping diode threshold voltage is too low and the laser diode forward voltage too high. But for reducing the design complexity, it seems reasonable to assume typical conditions (typ. process, 3.6V input voltage, 25°C) for testing the IC prototype in a first step. Although simulation models of diodes are incomplete (see Part 3.1.2.2), their sizing has been directly realized at layout level by considering examples of implementation issued from previous developments. As a reminder, diodes must be large enough to evacuate the residual energy from parasitic inductances during transients,



(a) Voltage-mode driver.

(b) Current-mode driver.

Figure 3.4 – Simplified schematic of clamping solution for both drivers.

considering the maximum targeted ON-state current. This roughly corresponds to a 3A current spike of 1ns width, estimated through transient simulations.

3.2.2.2 NMOS device comparison

It is proposed to compare NMOS devices in terms of dissipated power under normal operation. Nevertheless, other external indicators must be taken into account such as the gate oxide area and the mask count. The figure of merit gathering these indicators can be defined as

$$FoM_{SWITCH} = P_{TOT}.A_{OX}.N_{MASK} \tag{3.2}$$

where P_{TOT} is the losses, A_{OX} is the theoretical gate oxide area accounting for the product of the gate width and length of the device and N_{MASK} is the mask count. The best device tends to minimize these indicators, thus the figure of merit. As defined in Part 2.6.4, total losses for the switching element accounts for conduction and input switching losses over a pulse train. Since conduction losses increase as the gate width decreases (through the channel resistance) and input switching losses increase as the gate width increases (through input and output capacitances), it is expected to find an optimum width leading to minimize total losses, for a given ON-state current and modulation frequency [109]. In this context, losses could be evaluated using transient simulations (over a pulse train) instead of hand calculations. Conduction losses P_{COND} are computed in simulation by using the product of the current i_D and voltage v_{DS} at the device drain, defined as

$$P_{COND} = \frac{1}{T_{train}} \int_0^{T_{train}} i_D.v_{DS}\, dt \tag{3.3}$$

where T_{train} is the duration of the pulse train. Input switching losses P_{SW} are computed using the product of current i_G and voltage v_{GS} at the device gate but only during the

charging phase of the input capacitance (positive quantity only), defined as

$$P_{SW} = \frac{1}{T_{train}} \int_0^{T_{train}} \left(\frac{i_G + |i_G|}{2} \right) . v_{GS} \, dt \tag{3.4}$$

For a fair comparison, simulations are carried out in same conditions for all devices. The simulation bench of the voltage-mode driver is used here (see Figure 2.10a). The bench of current-mode driver could be used as well since similar losses are noticed in the switching element when considering a 50% modulation duty (see Appendix C). The stray inductance has not been included and the output voltage has been tailored for each device in order to reach the same ON-state current. Simulations have been performed in typical conditions for a high ON-state current (3A) and for frequency values of 50MHz and 200MHz while sweeping the gate width of devices from 10mm to 150mm by step of 5mm. The gate length has been set to its minimum according to the evaluated device (see Table 3.1) in order to benefit from a sufficiently low on-channel resistance. The gate driving voltage has been set to 1.2V and 3.6V for thin and thick oxide devices respectively. Results are shown in Figure 3.5. Values for the optimum width and the corresponding total losses are gathered in Table 3.4 for all devices, with other indicators for computing the figure of merit.

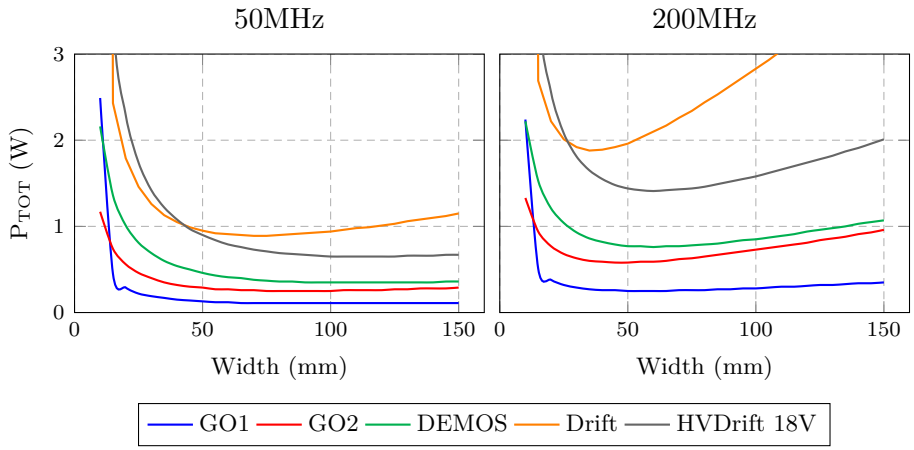
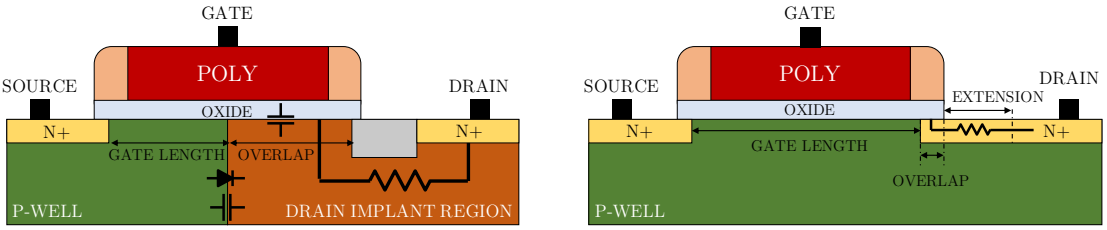


Figure 3.5 – Total losses for each device extracted over a gate width from 10mm to 150mm by step of 5mm, for a 3A ON-state current and modulation frequencies of 50MHz and 200MHz. Typical conditions have been assumed (typ. process and 25°C).

The GO1 device is the best candidate according to the figure of merit for both 50MHz and 200MHz use cases. It is due to its low breakdown voltage. High losses for Drift and HVDrift 18V devices are due to their structure [104]. They feature an important overlap of the gate area over the drain implant region (Drift region here) leading to a significant gate-drain overlap capacitance, thus increasing switching losses, as illustrated in Figure 3.6a. In the same way, the junction between the drain implant region and the p-well

Table 3.4 – Indicators for evaluating the NMOS devices. The best FoM is colored in green.

Results for 50MHz					
Device	GO1	GO2	DEMOS	Drift	HVDrift 18V
W_{OPT} (mm)	100	80	110	70	90
$P_{TOT(MIN)}$ (W)	0.11	0.25	0.35	0.89	0.59
A_{OX} (mm^2)	0.013	0.043	0.055	0.035	0.045
N_{MASK}	21	26	28	28	27
FoM_{SWITCH}	0.03	0.28	0.53	0.87	0.71
Results for 200MHz					
Device	GO1	GO2	DEMOS	Drift	HVDrift 18V
W_{OPT} (mm)	55	50	60	35	50
$P_{TOT(MIN)}$ (W)	0.25	0.58	0.76	1.88	1.27
A_{OX} (mm^2)	0.007	0.025	0.030	0.018	0.025
N_{MASK}	21	26	28	28	27
FoM_{SWITCH}	0.04	0.38	0.64	0.92	0.86



(a) Drift device.

(b) DEMOS device.

Figure 3.6 – Simplified cross-section of devices. Drawings not to scale.

contributes to increase the drain-to-source capacitance thus switching losses as well. In addition, the equivalent resistance of the channel device includes a significant extra resistance due to the Drift region, thus increasing conduction losses. As implant regions are different for Drift and HVDrift 18V devices, resulting losses are different. For similar reasons, total losses for the DEMOS device are higher than the ones of GO2 device mostly due to the relatively significant resistance added by the length extension between the gate and the drain contact, as illustrated in Figure 3.6b. It must be clarified as well that the theoretical gate oxide area A_{OX} in Table 3.4 does not consider the overlap length, so results for DEMOS, Drift and HVDrift 18V are quite optimistic.

Even if the GO1 device shows better results than other devices, it requires a voltage regulator providing a 1.2V supply voltage at the gate from the available input voltage (2.5V-4.8V) thus increasing the design complexity and size of the system. The overall

efficiency of the system could be impacted as well in spite of the benefit of low dissipated power from the GO1 device, because voltage regulators suffer from a low efficiency (typically from 20% to 60%) [114]. Considering now requirement in terms of voltage withstand (>7.2V), it is noticed that it goes beyond GO1, GO2 and DEMOS characteristics. These devices cannot be used alone. As a consequence, using a cascode configuration with a GO2 device as switching element and another device as cascode transistor seems to be a fair trade-off in this context. A second device comparison for selecting the cascode transistor is performed thereafter.

3.2.2.3 Sizing of the switching element

The goal of the sizing step is to define both the gate length and width of the GO2 device with respect to the specifications. Here, the device must fulfill requirements related to the application, meaning switching the current up to 3A over a modulation frequency from 50MHz to 200MHz, while minimizing the total losses and silicon area. As explained earlier, the gate length is set to its minimum (0.5µm) in order to benefit from a sufficiently low on-channel resistance while the gate width has an optimum value for minimizing total losses. It however depends on the current and frequency specifications, that are both programmable. As a consequence, it has been decided to make the gate width programmable for optimizing both conduction and switching losses by adjusting the on-channel resistance and input capacitance according to the targeted ON-state current and frequency. This allows more flexibility regarding the application and test measurements, but at the expense of the design complexity. A look-up table could be considered to handle this feature once the switch would be characterized.

Obviously, PVT variations have also an impact on electrical characteristics of the device, thus on the optimum width, but no compensation mechanism is proposed here. It seems reasonable to assume typical conditions (typ. process, 3.6V input voltage, 25°C) for sizing the device and testing the IC prototype in a first time.

Same transient simulations as before have been performed with a GO2 device for various use cases (I_{ON}, f_{MOD}) to get a relevant width range. From results listed in Table 3.5, it has been chosen to divide the width into 16 equal parts, configurable from 5mm to 80mm by step of 5mm. The 16 parts will be controlled by a 4-bit parameter. A major drawback of this approach could be an increase in switching losses since the equivalent output capacitance of the device is the sum of each individual output capacitance whatever is the number of enabled parts.

3.2.2.4 Sizing of the cascode transistor

An additional cascode transistor protecting the switching element is essential to fulfill voltage constraints (>7.2V). A simplified schematic of the cascode structure is depicted

Table 3.5 – Optimum width of the GO2 device for various use cases. Width parameter has been swept using a step of 5mm.

Use case	W_{OPT} (mm)	$P_{TOT(MIN)}$ (W)
(1A, 50MHz)	25	0.08
(1A, 200MHz)	15	0.19
(3A, 50MHz)	80	0.25
(3A, 200MHz)	50	0.58

in Figure 3.7. A cascode transistor T_{CASC} is placed in series with the switching element, between the drain node V_D and the switching node V_{SW}. The gate is tied to the input voltage V_{IN} in order to simplify the design, thus no voltage regulator would be required. In addition, the bulk is connected to the ground to prevent a capacitive coupling with the switching element through the output capacitance.

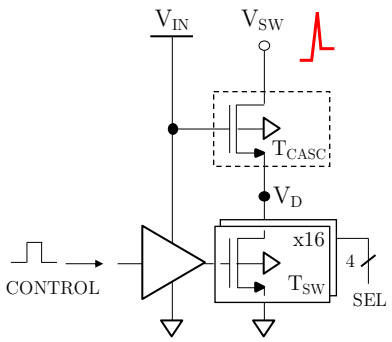


Figure 3.7 – Simplified schematic of the cascode structure.

It is proposed to compare all NMOS devices except the GO1 device, since requirements are beyond its characteristics and because a 1.2V supply voltage is required. In that case, it is not necessary to make the gate width programmable since major losses are due to conduction losses. Its width must be chosen large enough to ensure a low on-resistance but not too large to keep a low equivalent output capacitance. In contrast with the previous comparison, devices are compared in terms of output capacitance by considering the same on-channel resistance. Indicators such as the gate oxide area and the mask count are also considered. The figure of merit gathering these indicators can be defined as

$$FoM_{CASC} = C_{OUT}.A_{OX}.N_{MASK} \tag{3.5}$$

where C_{OUT} is the equivalent output capacitance at the switching node, A_{OX} is the theoretical gate oxide area accounting for the product of the gate width and length of the device and N_{MASK} is the mask count. The best device tends to minimize these indicators,

thus the figure of merit.

For a fair comparison, all devices have been evaluated in similar conditions. Here, the on-resistance value targeted for all devices is imposed by the current-mode driver. Indeed, the total on-resistance of the whole structure (switching element and cascode device) must be sufficiently low so that the resulting voltage drop during the OFF state (when the current is shunted to the ground) is lower than the laser diode threshold voltage (~1.2V). With a 3A ON-state current, it leads to a maximum total on-resistance of 400mΩ. In order to keep a safe margin, a worst-case scenario is assumed for sizing the devices, meaning a slow process, a 2.5V supply voltage and a 125°C junction temperature. The gate width of the switching element has been chosen for minimizing its on-resistance, giving 50mΩ for 80mm. Assuming a 5% margin on the total on-resistance, 330mΩ is thus targeted for sizing the cascode devices. The gate length has been set to its minimum (500nm). The output capacitance has been extracted as described in Part 2.2. Results are shown in Table 3.6 for all devices. Poor results for DEMOS, Drift and HVDrift 18V devices are due to their structure as explained before, even if they are optimistic according to the gate oxide area indicator. The GO2 device is the best candidate for implementing the cascode transistor. A gate width of 24mm is retained.

Table 3.6 – Indicators for evaluating the cascode devices. The best FoM is colored in green. Worst conditions have been assumed here (slow process, 2.5V, 125°C).

Parameter	**Switching element**	**Cascode device**			
Device	GO2	GO2	DEMOS	Drift	HVDrift 18V
R_{ON} (mΩ)	53	321	325	326	326
C_{OUT} (pF)	-	10	22	88	115
W (mm)	80	24	37	55	51
A_{OX} (mm^2)	0.04	0.012	0.018	0.028	0.026
N_{MASK}	26	26	28	28	27
$\mathbf{FoM_{CASC}}$	-	3	11	68	80

3.2.2.5 Versions of IC prototype

Two versions of the IC prototype are considered, both including the cascode structure and the clamping diode, with one implementing a P-N junction diode and the other a Schottky diode. In addition, three other versions are proposed, implementing a high-voltage device as cascode transistor in case of technical failures from the clamping diode. As said before, its electrical behavior could not be tested through transient simulations since models are incomplete. In that case, a HVDrift 18V device is retained with a gate width of 51mm (see Table 3.6). It could be interesting to evaluate without clamping diode as well. Various

versions of the IC prototype are summarized in Table 3.7. Since each version includes both voltage-mode and current-mode drivers, it would lead to test 10 IC prototypes.

Table 3.7 – Versions of the IC prototype. Only device references are indicated for easy readability.

Version	Switching element	Cascode device	Clamping diode
Version 1 (V1)	GO2	HVDrift 18V	w/o diode
Version 2 (V2)	GO2	GO2	Schotty
Version 3 (V3)	GO2	GO2	P-N junction
Version 4 (V4)	GO2	HVDrift 18V	Schottky
Version 5 (V5)	GO2	HVDrift 18V	P-N junction

3.2.3 Pre-bias current source

The pre-bias current is based on a current mirror technique [136]. The cell is connected to the drain node V_D in order to benefit from the protection of the cascode device. A simplified schematic of the pre-bias current source is depicted in Figure 3.8. Three current copies have been necessary for providing a proper current and reducing the mismatch in drain-source voltages and channel-length modulation parameter λ_{MOSFET} [131]. However, it is at the cost of a larger quiescent current. It has been decided to make the current programmable to accommodate VCSEL characteristics and to keep some design flexibility. For layout convenience, the current source is divided into 16 parts as considered for the switching element. The current is configurable from 0mA up to 550mA by step of 35mA, and will be controlled by a 4-bit parameter. Mirroring ratios as well as transistors dimensions are indicated in Figure 3.7. The current source has been implemented using GO2 devices. An integrated capacitance (~180pF) has been added at the gates of the last NMOS transistors pair for a better decoupling as strong current transients occur at the drain node.

It must be specified that the pre-bias current source is implemented for both driver toplogies but would be used for the voltage-mode driver only. It could be disabled for the current-mode driver. Nevertheless, this approach adds some extra parasitic capacitances at the drain node. Considering the voltage-mode driver topology, another important point is that generating a pre-bias current through the laser diode current path has an impact on the average current flowing through the laser diode. Therefore, this additional current must be taken into account when setting the current-level reference. Equation 2.21 can be revised into

$$I_{ON} = \frac{I_{AVG}}{\alpha} + \frac{(1-\alpha)I_{BIAS}}{\alpha} \tag{3.6}$$

where I_{AVG} is the average current flowing through the laser diode, I_{BIAS} is the pre-bias current and α is the modulation duty cycle.

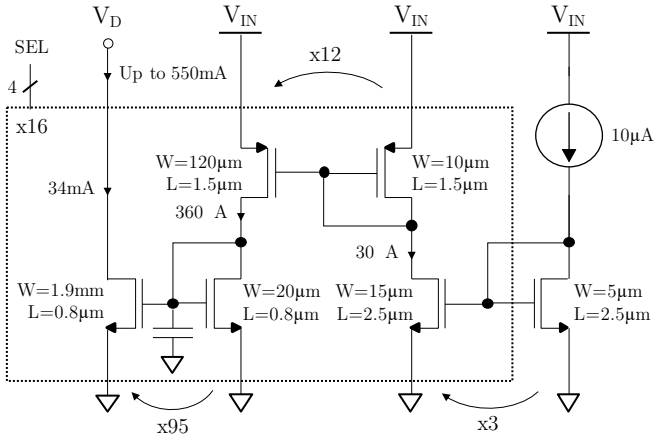


Figure 3.8 – Simplified schematic of the pre-bias current source, indicating mirroring ratios and transistor dimensions.

3.2.4 LVDS receiver circuit

A LVDS receiver circuit is used to convert the external differential modulation signal, through inputs MOD_P and MOD_N, into a single-ended modulation signal. A LVDS cell implemented using GO2 devices has been directly reused from previous developments. Its architecture is not detailed here. Depending on the driving topology, it has been noticed that the laser signal is in phase or in phase opposition with the control signal. Therefore, a simple logic block is required to adjust the control signal polarity according to the voltage-mode or current-mode driver. It acts on the LVDS output, for being then delivered to the switching element through a gate driver. This feature will be controlled by a 1-bit parameter. A simplified schematic of the transmission chain, including the LVDS receiver, the logic block and the gate driver, is depicted in Figure 3.9.

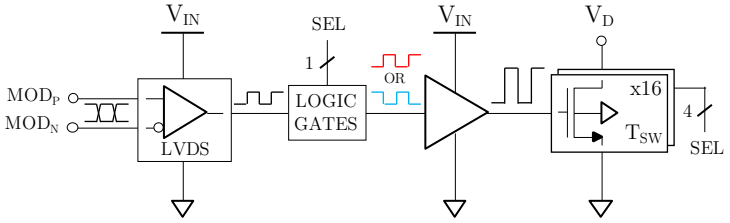


Figure 3.9 – Simplified schematic of the transmission chain, including the LVDS receiver, the logic block and the gate driver.

3.2.5 Gate driver

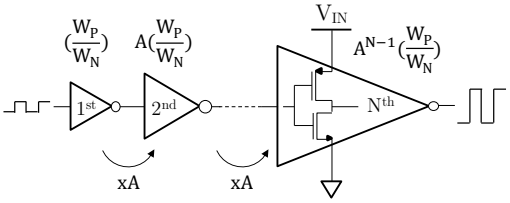
A gate driver is used to drive the large input capacitance of the switching element, from the single-ended modulation signal provided by the LVDS receiver circuit and logic block. Usually, a chain of inverters (also known as tapered buffer) is employed to drive this type of large capacitive load, where each stage is larger than the previous one by a specific factor A (named tapering factor) [137][138]. A conventional tapered buffer is shown in Figure 3.10a.

Since high currents are drawn from the power supply to charge the large input capacitance, a ripple may appear on the supply line due to parasitic inductances and impact the gate signal of the switching element. Parasitic values greatly depend on the PCB design and may remain uncertain. For that reason, it has been chosen to design a specific gate driver with a programmable driving capability, by adjusting rising and falling times of the gate signal. The gate driver is thus divided into 4 parts to adjust the equivalent output resistance of the last stage. Each part is made of a tri-state buffer in order to benefit from an output with a high impedance state. Indeed, this prevents short-circuits at the gate of the switching element. A simplified schematic of the proposed gate driver is depicted in Figure 3.10c, with details on the tri-state buffer in Figure 3.10b. It will be controlled by a 2-bit parameter.

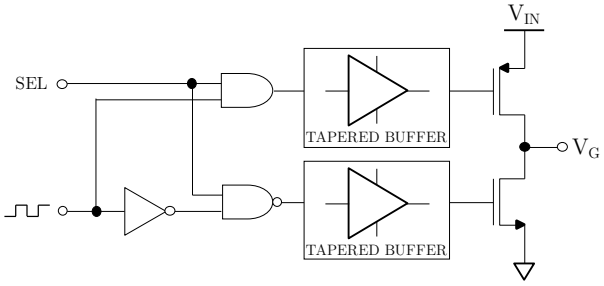
The last inverter stages of each tri-state buffer are sized in order to respect a linear programmability of rising and falling times, such as 200ps, 400ps, 600ps and 800ps for instance. Two tapered buffers are used to drive NMOS and PMOS transistors in the last inverter stages. For practical reasons against the switching element, the whole gate driver is divided into 16 equal parts. Thus, one part of the gate driver is sized for driving one part of the switching element. GO2 devices have been used for implementing the whole driver.

Ideal transient simulations have been performed in typical conditions for a 200MHz modulation frequency, by sweeping the gate width of devices to meet transient constraints while respecting a reasonable silicon area and power consumption. It is specified that the minimum gate length has been set for all devices. Moreover, PMOS devices are specifically sized two times larger than NMOS devices instead of three times in order to have similar rising and falling times as recommended for logic functions according to the design kit. A reasonable number of stages (5), maintaining the logic non-inversion with respect to the single-ended modulation signal, has been retained as well as a reasonable tapering factor (~4). Width ratios between the switching element and NMOS transistor in each last inverter stage, indicated in Figure 3.10c, have been determined through transient simulations.

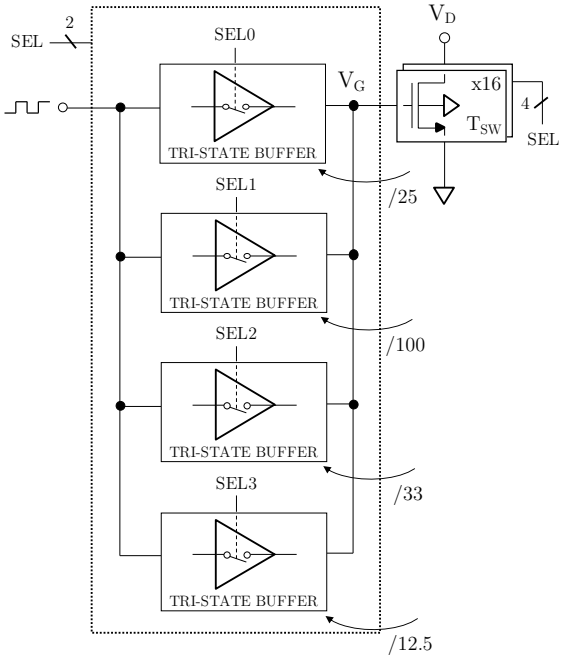
Transient results about the gate signal driving a unitary switching element (corresponding to a 5mm width) through a unitary gate driver are summarized in Table 3.8. Peak current



(a) Conventional Tapered buffer. Gate width ratio between PMOS and NMOS is indicated.



(b) Tri-state buffer.



(c) Gate driver. Gate width ratio between the switching element and NMOS transistors of each last inverter stage is indicated.

Figure 3.10 – Simplified schematic of the proposed gate driver including major building blocks.

values drawn from the power supply for charging the unitary input capacitance are also reported. It can be seen that the peak current increases with the driving capability due to fast rising and falling times, as expected. However, by assuming a full driving capability and a switching element set at its largest width (16x5mm), this leads to a peak current of around 3.5A drawn from the power supply during a very short time. As a consequence, a dedicated power path with a pin assigned to the supply voltage on PCB is necessary to minimize the resulting noise that could spread through adjacent circuits during fast

transients (further discussed in Part 3.3.2). A proper decoupling is also necessary for minimizing voltage ripple (further discussed in Part 3.3.10). Other dedicated current paths are to be assigned for analog and digital functions. Hence, the gate driver as well as the cascode transistor and the switching element share the same dedicated power supply while the pre-bias current source, LVDS circuit and logic block use both analog and digital supplies.

Table 3.8 – Transient results for a unitary gate driver.

Driving capability	**1 active part**	**2 active parts**	**3 active parts**	**4 active parts (full)**
Rising time	760ps	625ps	420ps	290ps
Falling time	500ps	425ps	285ps	240ps
Peak current	70mA	85mA	130mA	220mA

3.2.6 Electrostatic discharge ring

I/Os of the chip must be protected from Electrostatic Discharge (ESD) events. Protection devices such as reverse-biased diodes are used to clamp the external discharge coming from I/Os either to the supply voltage or ground, thus limiting the voltage applied to the I/O [139]. In addition, other devices such as power-rail clamp circuits are employed to clamp ESD over voltages across power lines specifically [140]. They are typically disabled when the circuit is under normal operation to prevent an unintentional clamping due to switching behavior from DC/DC converters for instance.

Usually, protection circuits are located in the periphery of the chip near each I/Os to protect, thereby adopting a ring shape. Here, a Fan-In WLCSP package is considered for the IC prototype, involving that tracks from the redistribution layer must be routed inward [141]. This leads to place protection circuits in the effective chip area. For that reason, some protection circuits grouped into clusters are carefully positioning close to I/Os sharing the same voltage constraints. The resulting ESD ring must be designed to ensure a continuous discharge current path between each I/O. A simplified schematic of a cluster within an ESD ring is shown in Figure 3.11. A dedicated ground is common to each I/O, where several assigned pins (GNDS pin) are located in the center of the chip to ensure a low impedance path. Each local ground referring to the analog, digital or power domain, is connected to the common ground through a back-to-back diode to ensure a bidirectional current path depending on which pin the ESD event occurs. Moreover, each I/O within a cluster shares a floating rail as a supply voltage so that the highest voltage between each I/O is preferred. This feature is commonly adopted on DC/DC converters when they allow step-up operations.

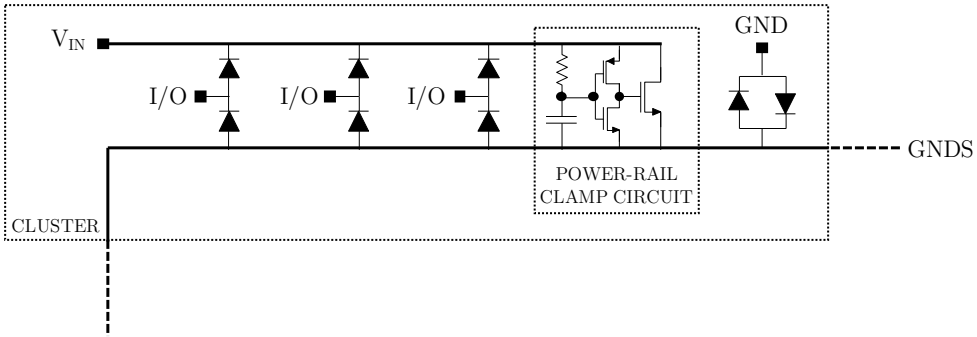


Figure 3.11 – Schematic of a cluster within an ESD ring.

3.2.7 Full block diagram

A full block diagram of the integrated LDD prototype is shown in Figure 3.12. It includes both the voltage-mode and current-mode drivers, sharing the same HFS block. The switching node V_{SW} (indicated in red) is common to both architectures. In addition to the output capacitor $C_{OUT,1}$ considered for the voltage-mode driver, another decoupling capacitor C_A is used to ensure an effective decoupling of the anode node V_A, assumed to be constant. For same reasons, decoupling capacitors C_{DEC} and $C_{DEC,INT}$ are employed for a proper decoupling of the HFS block power supply ($V_{IN,HFS}$ pin). The value, choice and sizing of these capacitances are further discussed in Part 3.3.10. A decoupling capacitor C_{IN} is also added at the input node (V_{IN}) ensuring an effective decoupling of DC/DC converters input voltage. The same capacitor than that of the output capacitor $C_{OUT,1}$ (4.7µF Murata MLCC GRM188C81E475KE11) is selected from requirements of the reused DC/DC converter.

Since a specific illumination pattern based on multiple pulse trains is required, an external low-frequency modulation signal (ENV in Figure 3.12) is provided in order to control the envelope of current pulses, thus generating pulse trains. An I^2C interface (SDA and SCL inputs) with a register bank, reused from previous developments, is embedded in order to configure the IC prototype. A bandgap voltage reference circuit is also embedded to provide voltage and current references for current-control loop circuits. Lastly, some test points (TP1, TP2 and TP3) are provided for debugging purpose only.

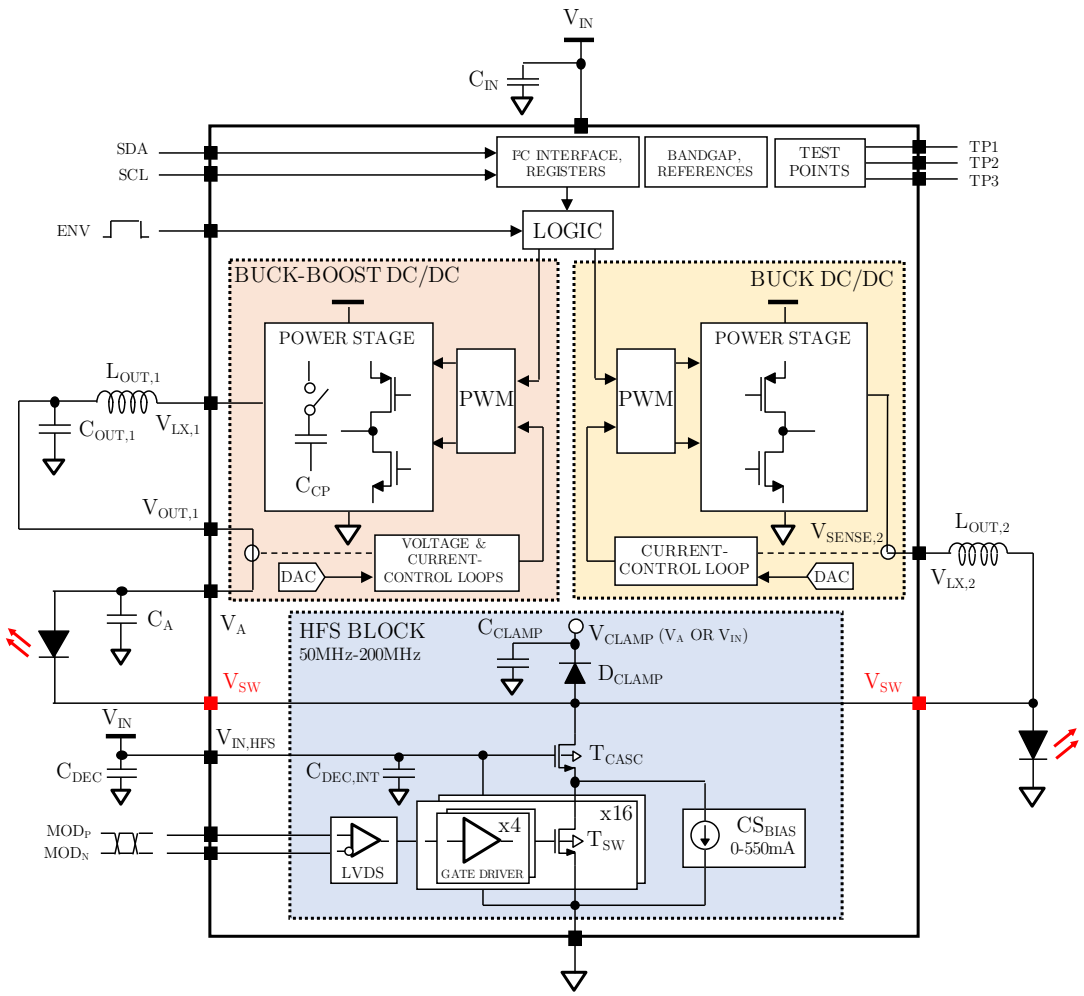


Figure 3.12 – Full block diagram of the integrated LDD prototype.

3.3 Layout Details

As previously explained, the work has been distributed over different layouters within the department due to a short schedule related to the industrial context. At layout level, no direct contribution has been provided from the thesis point of view. Nevertheless, following sections review the work realized by the layout team. Considerations on the layout of the chip at both top and cell levels are discussed before presenting the layout of various blocks of interest.

A major challenge concerns the proper operation of the whole circuit mixing both reused and new building blocks inducing strong voltage and current constraints. The required high-frequency switching of the current up to few Amps by using transistors generates parasitic voltages and currents that may disturb adjacent cells [109]. Some solutions are considered thereafter.

3.3.1 Top-level considerations

A suitable placement of the new blocks within the chip is required to save silicon area and ease the routing. As explained in Part 2.1.7, the process features a metal stack of several layers for connecting devices through metal lines and VIAs. A major issue is the resulting parasitic resistances and capacitances added by each interconnection that may degrade performances by increasing signal delays and power losses. It is proposed to increase the contact zone (drain, source, gate) of transistors and the width of metal lines while using several VIAs in parallel in order to decrease the parasitic resistance. A specific placement of VIAs can be employed for reducing parasitic capacitances [109]. Another issue concerns the metal electromigration. It is due to the migration of metal atoms when conductors carry too much current thus leaving a void and locally increasing the resistance [139][142]. It may even cause failure. The metal electromigration can be mitigated by limiting the maximum current density. Higher levels of metals with a large number of VIAs in parallel are also used for power routing [142].

3.3.2 Cell-level considerations

The main concern at cell level is related to substrate coupling, due to charge injection from or to adjacent cells during fast current transients. A proper isolation of each cell is thus essential. As explained in Part 2.1.7, a key front-end feature of the process is to use a triple well. NMOS devices can thus be isolated from the substrate of the chip by using a p-well, acting as a local bulk, inside a deep n-well and surrounding by a n-well Guard Ring (GR). This structure is also referred to as an NMOS with Active Well (NMOS-AW). It is detailed in [109]. Usually the substrate of the chip is tied to the ground, the p-well is tied to the source of the NMOS device while the n-well is tied to a high voltage to make sure that junction diodes are reverse biased. In addition, a guard ring made of a P+

diffusion region can be implanted around the device for an efficient biasing of the substrate of the chip, in order to evacuate carriers through a low impedance path. Shallow Trench Isolations (STIs) are used to isolate active areas such as drain or source contacts from guard rings for instance.

PMOS devices inherently benefit from a proper isolation since their bulk is usually tied to a high voltage making junction diodes reverse biased. However, the isolation can be improved by placing a deep n-well underneath the bulk in order to decrease the gain of the vertical parasitic PNP bipolar transistor formed by the drain, bulk and substrate. Usually the bulk is tied to the source of the PMOS device. A guard ring made of a P+ diffusion region can be implanted around the device as well for an efficient biasing of the the substrate of the chip to evacuate carriers through a low impedance path.

Another key front-end feature of the process is that a lightly doped epitaxial silicon layer is grown on the surface of a heavily doped p-type substrate wafer in order to reduce the substrate coupling as well as to improve the immunity to latch-up [143].

Even if they are area consuming, these isolation techniques can be employed and tailored for each block to guarantee a proper carrier evacuation so as to minimize electrical noise. A particular care must be given to the switching element, the cascode device and the gate driver where strong current transients are considered. Another method for minimizing the impact of noise between each block consists in using a dedicated power path with an assigned pin for each analog, digital and power domain [139]. Different paths following a star routing strategy can be used to supply sensitive blocks sharing the same domain. A low impedance path up to pins is necessary here. Moreover, due to thermal effects, several solder balls can be used for a singe I/O especially if high currents are carried, as explained in Part 2.6.2.

3.3.3 HFS block considerations

It has been decided to divide the switching element into 16 equal parts. For layout convenience, other cells carrying high currents within the HFS block, such as the cascode device, the gate driver or the pre-bias-current source, are also divided into 16 equal parts and integrated within each part of the switching element. Note that only the switching element and the pre-bias current source are configurable. A major challenge here is to properly route all the parts for optimizing the current flow that must be as symmetrical as possible flowing from the cascode device to the switching element and current source. The first part must be activated from the middle of the structure, then alternatively from left and right, in order to have approximately the same metal resistance seen from each part of the switching element and current source. A simplified schematic of the proposed solution is depicted in Figure 3.13. Note that these circuits are supplied using a dedicated power path with an assigned pin $V_{IN,HFS}$. Other blocks such as the clamping diode, LVDS

circuit and logic block must be located as close as possible to the HFS block.

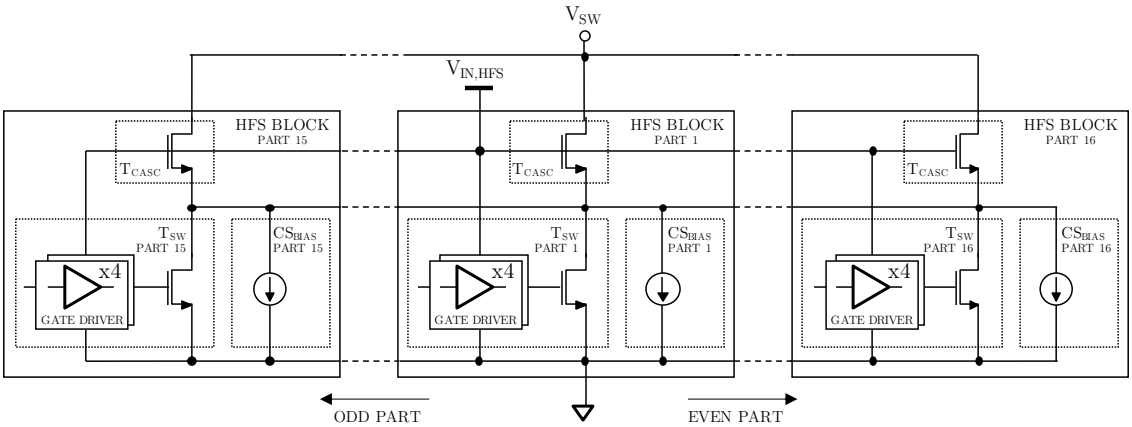


Figure 3.13 – Proposed solution for the HFS block partitioning.

3.3.4 Switching element layout

The switching element is implemented using a multi-finger structure, which is detailed in [109]. The source and drain junction areas and the gate resistance can be reduced with this approach but at the cost of a larger source and drain perimeter capacitances [139]. In addition, the device is divided into several unitary cells connected in parallel thus avoiding long geometries in the layout. The number of fingers and gate width of a unitary cell are chosen so that the bulk is biased with a low resistive path for preventing snapback effect due to the horizontal parasitic NPN bipolar transistor formed by the drain, bulk and source. This effect may occur when a high voltage is applied across the drain-bulk junction generating an avalanche current from the drain to the bulk [144]. The bulk resistance may cause a voltage drop across the bulk-source junction (equivalent to a base-emitter junction for the bipolar transistor) sufficiently high to trigger the parasitic NPN bipolar transistor leading to failures.

Structure It has been decided to implement a part of the switching element into 54 unitary cells of 4-fingers GO2 MOSFETs with a width of 100µm connected in parallel. It comes to an overall width of 5.4mm for one part thus 86.4mm for 16 active parts. Comparing to a 5mm part required at design level, it leads to an on-resistance slightly smaller and an input and output capacitances slightly larger but without impacting performances. Furthermore, the cell uses a common source and bulk which is less area-consuming. Due to the even number of fingers, each cell has two contacts for the drain and three contacts for the source which two of them are located at the edge of the cell, sharing two bulk contacts.

Isolation The switching element is isolated using an active well that is shared by each unitary cell. In order to benefit from a low resistive path for biasing the n-well guard ring, a n-well trench is added across the middle of the parts splitting the 54 cells into 2 groups of 27 cells each. Following design recommendations from the process, a minimum spacing of 3µm must be respected between the n-well guard ring and the nearest drain implant region (made of a N+ diffusion region) to avoid triggering the other horizontal parasitic NPN bipolar transistor formed by the n-well guard ring, bulk and drain. In addition, a second guard ring made of a P+ diffusion region surrounding the whole device is used to bias the substrate of the chip, tied to ground.

The layout of the switching element is depicted in Figure 3.14. The full device occupies a 1297x109µm^2 area.

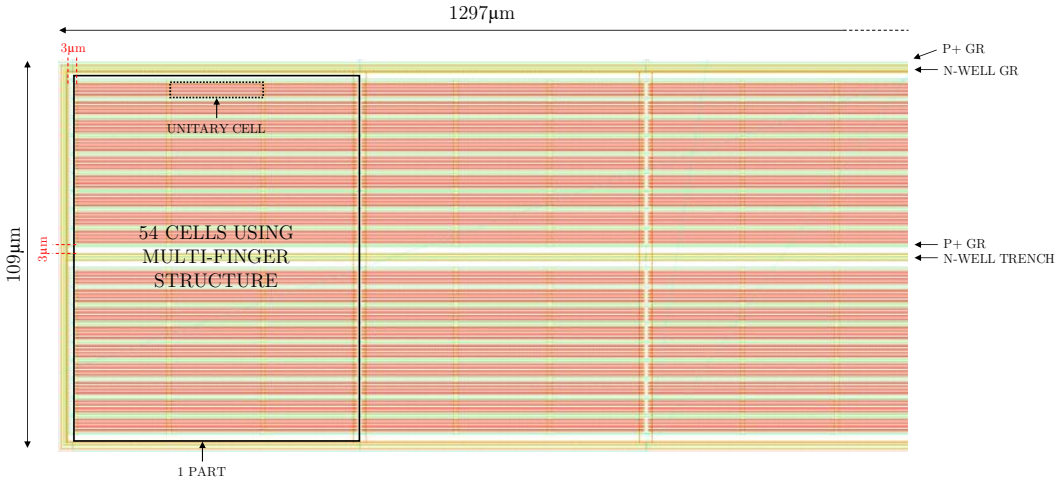


Figure 3.14 – Layout of the switching element. For easy readability, only few cells are illustrated without the metal routing.

3.3.5 Gate driver layout

Structure The gate driver has been divided into 16 equal parts and integrated into each part of the switching element (see Figure 3.13). Each gate driver part consists of four tri-state buffers of different dimensions. NMOS and PMOS devices of each inverter use a multi-finger structure with a common source and bulk. The number and sizing of fingers depend on the gate width.

Isolation Instead of using a NMOS-AW structure for each NMOS device of a tri-state buffer, all NMOS devices are grouped together and isolated from the substrate of the chip by using a global active well. Furthermore, two groups of NMOS devices are placed close

enough so that they can share the same active well, what is less area-consuming. A second P+ guard ring surrounding each group of devices is used for an efficient biasing of the substrate of the chip, thus minimizing latch-up susceptibility [139].

The layout of the gate driver is depicted in Figure 3.15. The full block occupies a 1293x149µm^2 area.

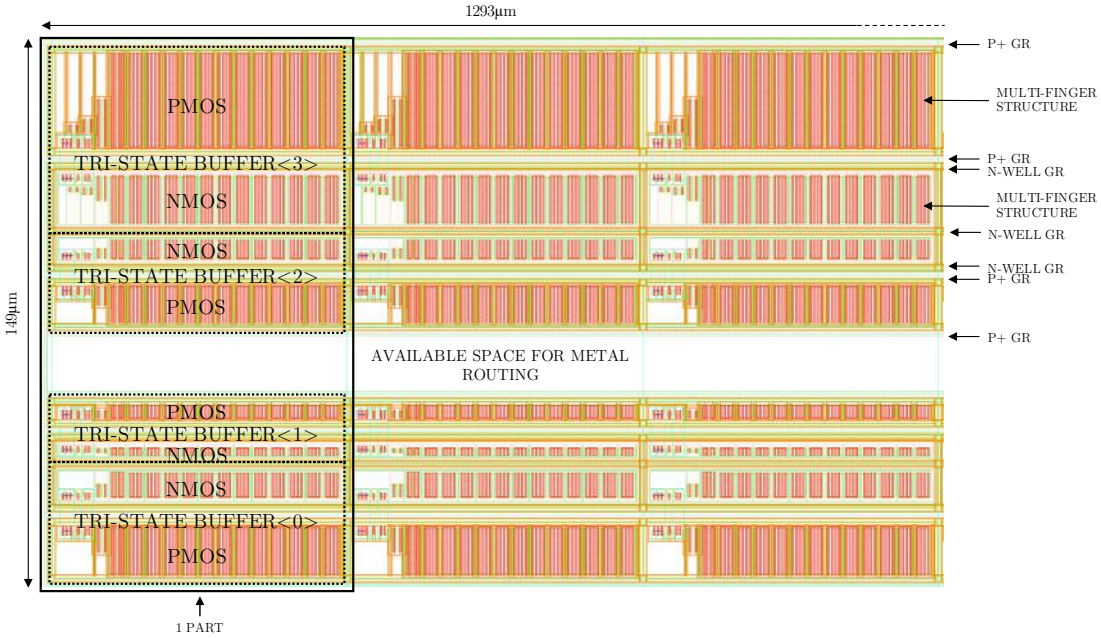


Figure 3.15 – Layout of the gate driver. For easy readability, only few cells are illustrated without the metal routing.

3.3.6 Cascode device layout

The cascode device is implemented using either a GO2 or HVDrift 18V device, depending on the version of the IC prototype (see Table 3.7).

3.3.6.1 HVDrift 18V device

Structure The HVDrift 18V device has a specific structure realized in a p-well and using a N-drift region with a drain access separated by a STI, as illustrated in Figure 3.16. For that reason, only a double gate structure may be achieved, thus generating a unitary Bulk-Source-Drain-Source-Bulk (BSDSB) cell that is symmetric drain centered. It can be then multiplied in order to get a multi-finger-like structure. For layout convenience, it has been decided to implement the device into 1056 unitary cells with a width of 25µm

connected in parallel and distributed into 16 parts (66 cells for each part). It comes an overall width of 52.8mm. Compared with the 51mm width required at design level, it leads to an on-resistance slightly smaller and a input and output capacitances slightly larger but without impacting the performances.

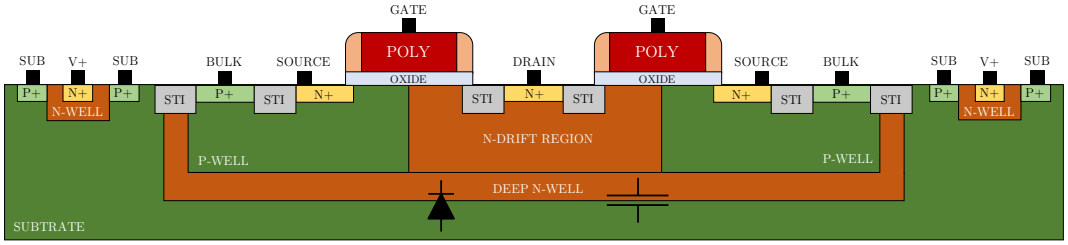


Figure 3.16 – Simplified cross-section of an isolated HVDrift 18V device with a triple guard ring. Drawing not to scale.

Isolation The HVDrift 18V device is isolated using an active well that is shared among unitary cells. Due to large dimensions, a proper isolation is ensured by splitting the whole device into 2 groups of 528 cells each. A P+ trench is added between the 2 regions to bias the substrate of the chip to ground. The deep n-well is however inherently connected to the drain through the Ndrift region. It thus results in a coupling between the drain and the substrate through the large deep n-well/substrate junction. For that reason, a triple guard ring made of successive P+, n-well and P+ regions surrounding the whole cascode device has been implemented to properly collect carriers, as illustrated in Figure 3.16. In addition, a dedicated low impedance path is required to connect the substrate to the ground pin GNDS of the chip, while the bulk is connected to a dedicated power ground.

The layout of the cascode device implementing a HVDrift 18V device is depicted in Figure 3.17. The full device occupies a 1316x172µm^2 area.

3.3.6.2 GO2 device

Structure The GO2 device is implemented using a multi-finger structure. But the bulk is connected to the power ground, thus a common bulk and source cannot be used. It has been decided to implement the device into 240 cells of 4-finger GO2 MOSFETs with a width of 100µm connected in parallel and distributed into 16 parts (15 cells each part). It comes an overall width of 24mm.

Isolation The device is isolated using an active well that is shared among unitary cells. As done for the switching element, a minimum spacing of 3µm must be respected between the n-well guard ring and the nearest drain implant region. In addition, a second guard

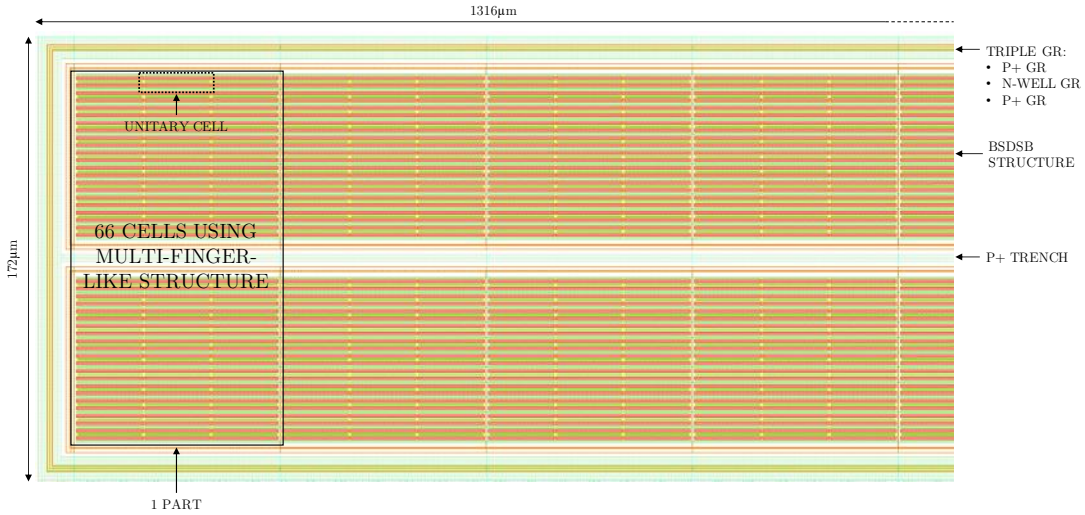


Figure 3.17 – Layout of the cascode device implementing a HVDrift 18V device. For easy readability, only few cells are illustrated without metal routing.

ring made of a P+ diffusion region surrounding the whole device is used to bias the substrate of the chip, tied to ground.

The layout of the cascode device implementing a GO2 device is depicted in Figure 3.18. The full device occupies a 1304x40µm^2 area.

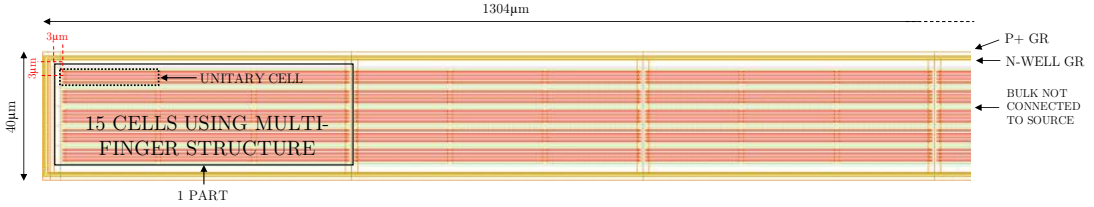


Figure 3.18 – Layout of the cascode device implementing a GO2 device. For easy readability, only few cells are illustrated without the metal routing.

3.3.7 Pre-bias current source layout

For layout convenience, it has been decided to split the pre-bias current source into 2 cells. A first cell includes devices for the first and second current mirrors (from 10µA to 360µA per channel) and a second cell includes devices for the third current mirror (from 360µA to 34mA per channel). The first cell is located as close as possible to the HFS block while the second cell is integrated into each part of the HFS block, as illustrated in Figure 3.19.

Note that the first cell is supplied using a dedicated power path (for minimizing the impact of noise between analog and power blocks) with assigned pins AV_{IN} and AGND for the supply voltage and ground respectively, while the second cell uses the same power ground as the switching element.

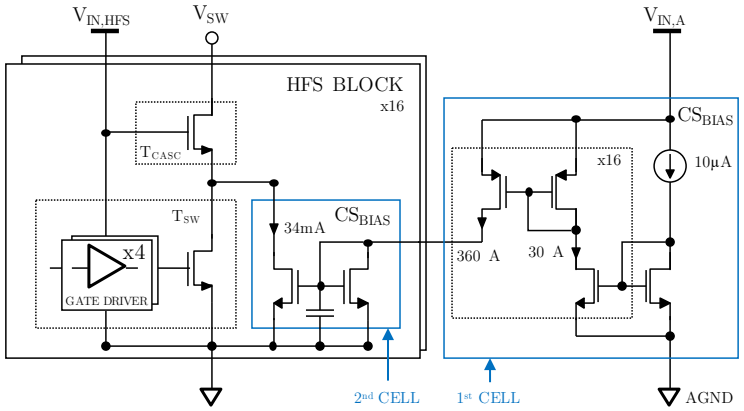


Figure 3.19 – Proposed solution for the pre-bias current source partitioning.

Structure A multi-finger structure has been used for the biggest NMOS devices, namely for the third current mirror. For optimizing the layout while respecting design recommendations, each part of the second cell includes 96 NMOS transistors with a width of 20µm connected in parallel. In the same way, it includes 36 NMOS transistors for implementing the integrated capacitance as a MOS capacitance, made using the polysilicon as positive electrode and the n-well as negative electrode.

Isolation All NMOS devices of the second cell are grouped together and isolated from the substrate of the chip by using a global active well. Active wells are used for devices of the first cell. A P+ guard ring is used for each group of NMOS and PMOS devices separately in order to bias the substrate of the chip.

The layout of the pre-bias current source is depicted in Figure 3.20. The first and second cells occupy a 95x216µm^2 and 1297x74µm^2 areas respectively.

3.3.8 Clamping diode layout

The clamping diode is implemented using either a Schottky or P-N junction diodes, depending on the version of the IC prototype.

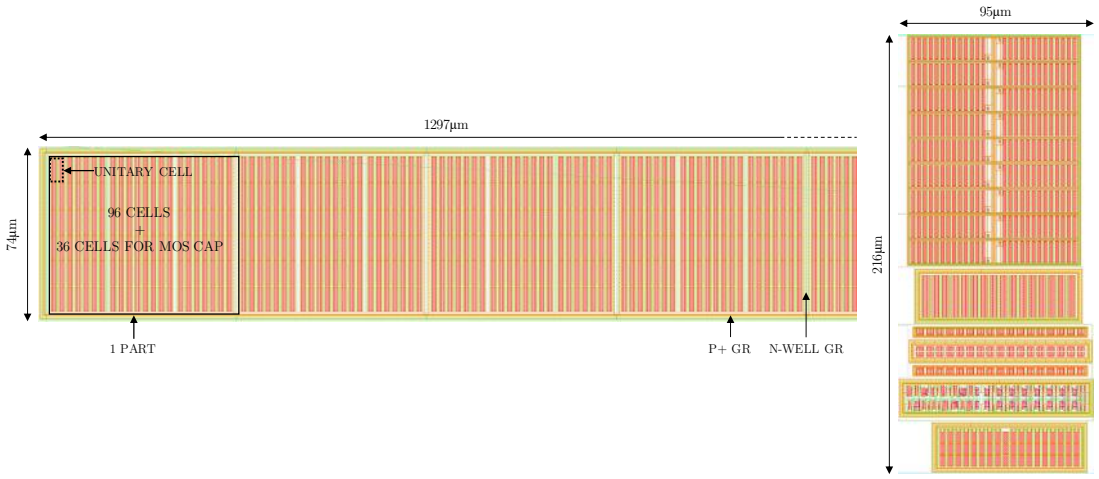


Figure 3.20 – Layout of the pre-bias current source: second cell (left) and firt cell (right). For easy readability, only few cells are illustrated without the metal routing.

Schottky diode The device is realized in a deep n-well, acting as a cathode, with a cobalt salicide layer as anode. Note that the parasitic junction diode between the deep n-well and the substrate may induce a coupling during fast transients. The device is thus implemented using 336 unitary cells connected in parallel and arranged in a matrix shape. It allows to properly bias the substrate with a P+ guard ring surrounding the unitary cells, thus reducing the substrate noise.

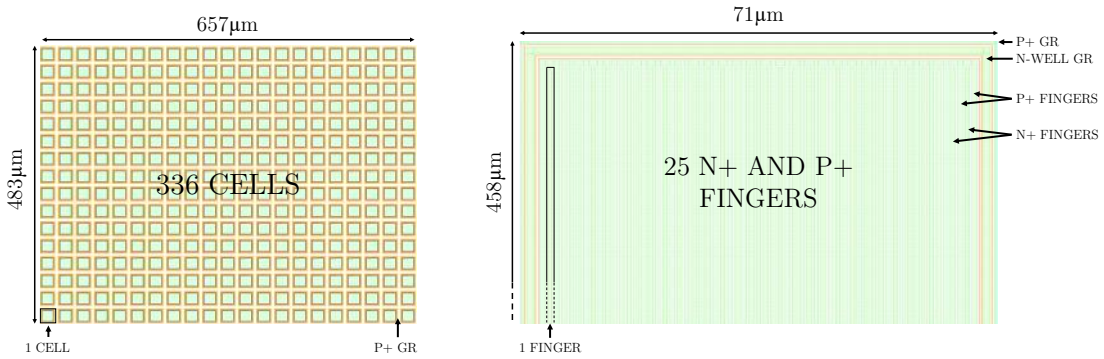
The layout of the Schottky diode is depicted in Figure 3.21a. The whole device has a total area of 657x483µm^2.

P-N junction diode The device is realized in a p-well, acting as anode, with a N+ diffusion region as cathode. The device is implemented using two interdigitated combs of 25 N+ and P+ fingers, such that a homogeneous current flows through the whole device. In order to reduce the substrate noise, the device is isolated using an active well, that is shared among the unitary cells. In addition, an P+ guard ring surrounding the whole device is used to bias the substrate of the chip, tied to ground.

The layout of the P-N diode is depicted in Figure 3.21b. The whole device occupies a total area of 458x71µm^2.

3.3.9 LVDS circuit layout

The LVDS circuit and logic block are located as close as possible to the HFS block. The layout of these blocks has been realized using conventional design rules related to the



(a) Schottky diode.

(b) P-N junction diode.

Figure 3.21 – Layout of the clamping diode.

process. Each block is isolated from the substrate using an active well and an P+ guard ring as previously explained. They occupy a total area of 312x60µm^2. Note that these circuits are supplied using a dedicated analog and digital power path with assigned pins.

3.3.10 Decoupling capacitors

A proper decoupling of several nodes within the circuit is essential for minimizing voltage ripples due to the high-frequency current switching. Three major nodes are concerned:

- The HFS block power supply ($V_{IN,HFS}$).
- The anode voltage (V_A), considered for the voltage-mode driver only.
- The clamping voltage (V_{CLAMP}).

3.3.10.1 Decoupling of the HFS block power supply

It has been seen that high currents can be drawn from the power supply through the gate driver in order to charge the input capacitance of the switching element (see Part 3.2.5). For that reason, a dedicated Power Delivery Network (PDN) using low-impedance power track and ground plane with appropriate decoupling capacitors is required in order to properly supply the building blocks [145]. A schematic of a typical PDN model considering the HFS block as an integrated circuit is shown in Figure 3.22 where V_{IN} and GND represent the power supply terminals on PCB. A methodology for designing a PDN is well described in the literature [145][146]. It relies on the optimization of the PDN impedance, by selecting suitable capacitors so that their values do not exceed a target impedance over a specific bandwidth. The target impedance Z_T (in Ω) is expressed as

$$Z_T = \frac{\Delta V}{\Delta I} \tag{3.7}$$

where ΔV is the allowed voltage ripple and ΔI is the transient current.

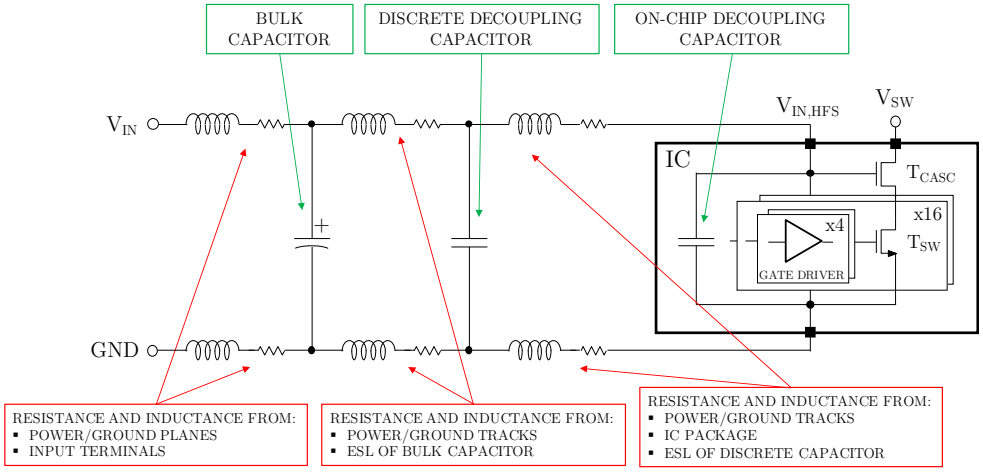


Figure 3.22 – Typical Power Distribution Network model. Major contributors that may impact the power integrity are indicated in red while decoupling capacitors that may reduce the voltage noise are indicated in green.

Usually, the resulting target impedance is very small and constraining. It leads to an overdesign by choosing a very large number of decoupling capacitors which is not realistic considering cost and PCB area [147][148]. The methodology proposed in [148] is considered here. It is based on the definition of the allowable voltage ripple and the corresponding current transient for different frequency ranges of interest. It allows to reduce constraints on the target impedance for various frequency ranges. This method is intended for digital circuits (processor, memory interface, etc...) targeting a reasonable jitter in order to properly transmit data at a fixed operating frequency. In this context, the method could be tailored by defining the rising time of gate signal as a target. Various modulation frequencies could be considered as well. Diverse capacitors such as off-chip and on-chip capacitors can be employed. Nevertheless, the on-chip capacitance value that can be achievable with integrated process is often limited by the silicon area.

It is proposed to determine the highest capacitance value for a reasonable silicon area in a first time, then to select off-chip capacitances according to the target impedance. Steps for determining this target impedance are detailed in Appendix D. It is however required to have an idea of parasitics for PCB tracks of interest. For that purpose, a RLCG netlist has been extracted using ANSYS Q3D from a previous PCB with specifications close to this work. It can give a first approximation of the impedance for high power paths. A loop inductance of approximately 6nH has been estimated for this PDN.

On-chip capacitance It must be located as close as possible to the HFS block. The total capacitance value can be obtained through several types of integrated capacitors for optimizing the area. As explained in Part 2.1.7, the process delivers three major types of integrated capacitors:

- MOS capacitor realized using the polysilicon as positive electrode and a n-well as negative electrode,
- MOM capacitor realized using a metal layer with two interdigitated combs. Several metal layers can be used to increase its density,
- MIM capacitor realized using two additional metal levels as electrodes (a bottom and top plates) located in an inter-metal dielectric between two metal layers.

The general structures are detailed in [109]. It has been decided to implement a MOS capacitor using the silicon area around the HFS block. It is made using a GO2 device. In addition, a MIM capacitor with a high density (5fF/µm^2 [104]) and a 4.8V maximum operating voltage is implemented above the MOS capacitor using bottom and top plates and connected through the ALUCAP layer. The MOM capacitor has not been used due to its relatively low density and a complex metal routing.

Elementary cells are adopted for properly biasing the substrate. The layout of a cell is realized using a unitary MIM capacitor stacked over four unitary MOS capacitors surrounded by a P+ guard ring. The area of a cell is of 40x42µm^2. Finally, 292 unitary cells are connected in parallel in order to get an overall value of around 2.4nF for a supply voltage larger than 2.5V. All MOS capacitors are isolated using a global active well. The layout of a unitary cell is depicted in Figure 3.23.

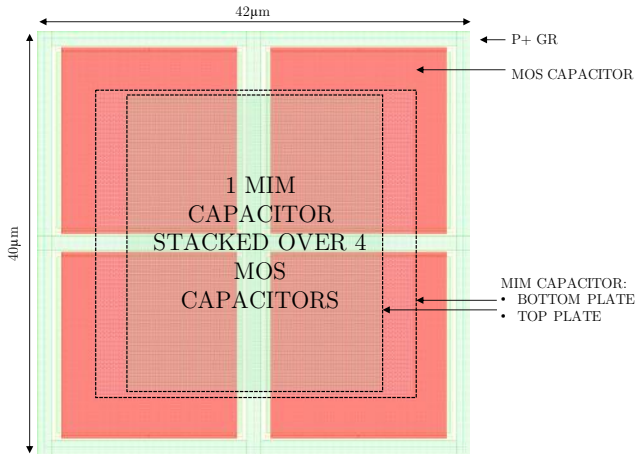


Figure 3.23 – Layout of a unitary cell made of 4 MOS and 1 MIM capacitors. For easy readability, the cell is illustrated without the metal routing.

Off-chip capacitance High frequency ceramic capacitors with various values (from 1nF up to 10µF) are selected to keep a flat impedance from 1MHz to several hundreds of MHz [145][149]. They are connected in parallel for reducing the overall equivalent series resistance and inductance (ESR and ESL). They must be placed as close as possible to the chip in order to minimize the effective loop inductance seen by the gate driver. A hierarchical placement based on the size must be adopted here to have an effective decoupling where the smallest possible capacitors are near the IC pins while biggest ones are adjacent to them. A bulk capacitor is also added close to power supply terminals on PCB to provide current at low frequencies and maintain a low impedance from kHz up to 1MHz [145].

The PDN impedance has been estimated with simulations in the frequency domain. Several capacitors have been tested using models from suppliers, such as Murata for instance, in order to respect the target impedance (see Appendix D). Unfortunately, although the proposed method tends to reduce constraints for low frequencies, the target impedance is still very restrictive at high frequencies. Thus, the selection of decoupling capacitors is realized so that the PDN impedance is as low as possible while dealing with typical cost and PCB area constraints in consumer electronics. Six different capacitance values are retained: 100µF, 10µF, 22nF, 10nF, 4.7nF and 2.2nF. The proposed PDN model and simulation waveforms of the PDN impedance with and without decoupling capacitors are depicted in Figure 3.24 and Figure 3.25 respectively. The complete list of capacitors with characteristics are summarized in Table 3.9.

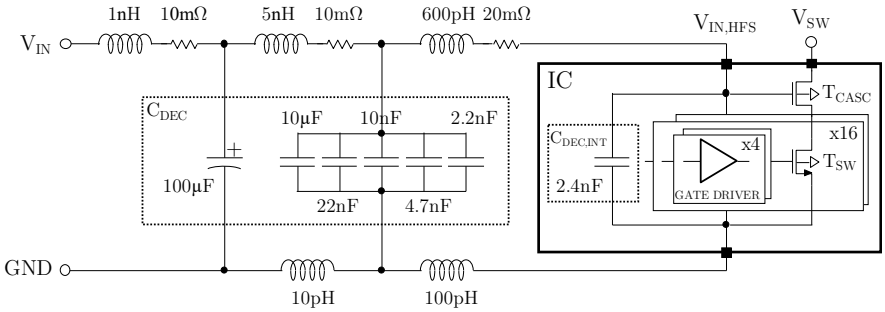


Figure 3.24 – Proposed PDN model.

Although the initial anti-resonance at 40MHz has been reduced, another unwanted peak around 120MHz is now caused by the on-chip capacitance (~2.4nF) and the effective loop inductance (~700pH). The supply noise may still be amplified at this frequency even if the parasitic resistance of metal tracks and on-chip routing may however contribute to reduce the peak amplitude. A solution for reducing the parasitic inductance would consist in adding a thin-film capacitance as a decoupling capacitor embedded within the PCB between the power and ground planes and/or using a silicon-type interposer [150][109][151].

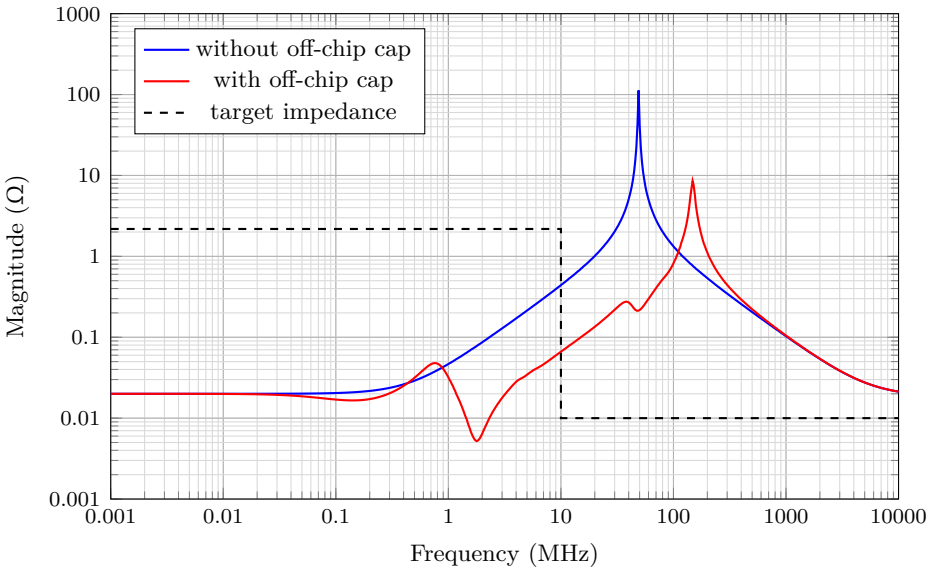


Figure 3.25 – Impedance of the PDN model with the target impedance.

These innovative solutions could improve performances and save PCB area but at the expense of the manufacturing cost. They have not been considered in this work. The solution adopted here will consist in minimizing as much as possible the remaining parasitic inductance with a proper PCB layout.

Table 3.9 – Characteristics of decoupling capacitors.

Function	Value	Manufacturer	Part number	Type	Rated voltage	Temperature characteristics	Size
Bulk capacitor	100µF	Panasonic	EEFCX0J101R	Organic Polymer Aluminum	6.3V	-55°C to 105°C	7.3mm x 4.3mm
Decoupling capacitor	10µF	Murata	GRM188R61E106MA73	MLCC	25V	X5R	1608M
Decoupling capacitor	22nF	Murata	GRM033R61A223KE84	MLCC	10V	X5R	0603M
Decoupling capacitor	10nF	Murata	GRM033R61A103KA01	MLCC	10V	X5R	0603M
Decoupling capacitor	4.7nF	Murata	GRM033R61A472KA01	MLCC	10V	X5R	0603M
Decoupling capacitor	2.2nF	Murata	GRM033R61A222KA01	MLCC	10V	X5R	0603M

3.3.10.2 Decoupling of the anode voltage

The anode voltage V_A must remain constant during operations. A voltage ripple, due to high voltage spikes during fast current transients may propagate through the sense resistance and disturb the current-control loop. Therefore, a decoupling capacitor (C_A in Figure 3.12) must be used in addition to the output capacitor $C_{OUT,1}$ to ensure an effective decoupling. A selection of small capacitors (in the order of tens of nF) is sufficient to provide current at high frequencies while not disturbing the loop stability, mostly based on the output capacitor value. These capacitors must be placed as close as possible to the VCSEL anode pad. The previous four 0603M ceramic capacitors (22nF, 10nF, 4.7nF and 2.2nF) can be used in this context, what seems to be a reasonable choice with respect to the cost and PCB area. It simplifies the PCB design as well.

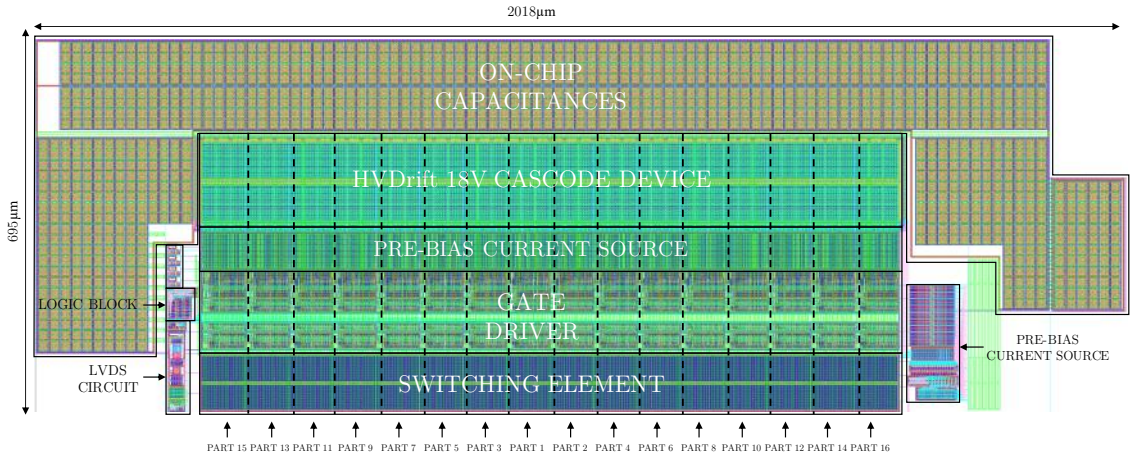
3.3.10.3 Decoupling of the clamping voltage

The clamping voltage V_{CLAMP} must remain constant during operations. As a reminder, it is either the anode voltage or the supply voltage. In addition to off-chip decoupling capacitors already proposed for the anode voltage (C_A in Figure 3.12) and the supply voltage (C_{IN} in Figure 3.12), an on-chip decoupling capacitance is implemented, thus providing a low impedance path in order to evacuate charges from the clamping diode. The same unitary cell made of MOS and MIM capacitors is used. Due to a limited silicon area close to the clamping diode, only 104 cells are implemented and connected in parallel, for a total area of 534x323µm^2. The overall capacitance value is 820pF for a supply voltage from 2.5V up to 4.8V.

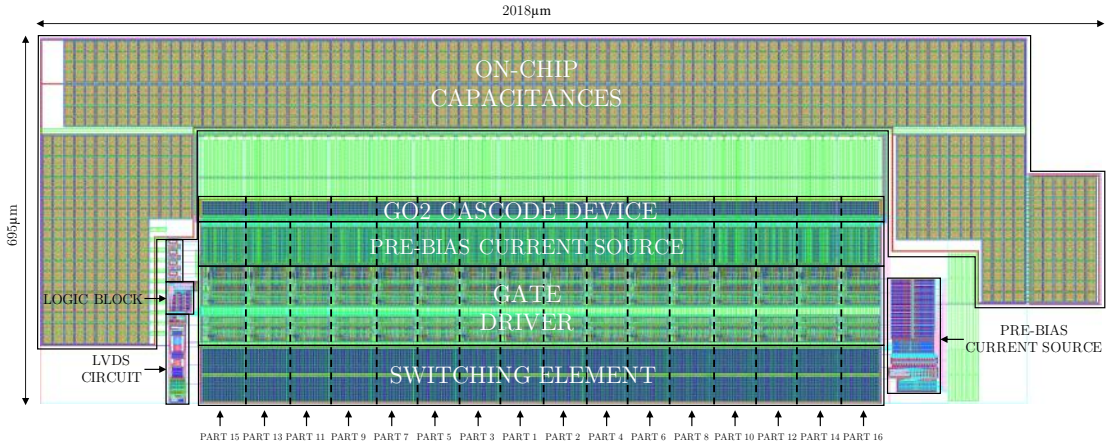
This kind of MIM and MOS integrated capacitors cannot withstand voltages up to 7.2V as required by voltage constraints at the anode voltage for the voltage-mode driver. At the date of the IC design, these capacitors were implemented but the voltage rating was a little bit forgotten in the process. From experimental point of view, this mistake is a limitation in the voltage applied at the anode voltage thus the current for the voltage-mode driver.

3.3.11 HFS block layout

The layout of the HFS block using HVDrift 18V or GO2 cascode devices is depicted in Figure 3.26. It occupies a 2018x695µm^2 area for both versions, including the on-chip capacitor. Note that the allocated silicon area for the cascode device is limited by the layout of the HVDrift 18V device as it is much larger than the GO2 device. Due to constraints on the layout of the full IC prototype, the clamping diode is located in another area of the chip.



(a) HVDrift 18V cascode device.



(b) GO2 cascode device.

Figure 3.26 – Layout of the HFS block. For easy readability, the block is illustrated without the metal routing.

3.3.12 Full chip layout

The layout of the IC prototype (V2) is depicted in Figure 3.27. The full chip, including both voltage-mode and current-mode drivers, occupies a silicon area of around 20mm^2 (roughly the same value for each version). By counting the sum of silicon areas for each block required by each driver, it comes a silicon area of around 7mm^2 for the voltage-mode driver and 6mm^2 for the current-mode driver (roughly the same values for each version), which is more representative from an industrial point of view.

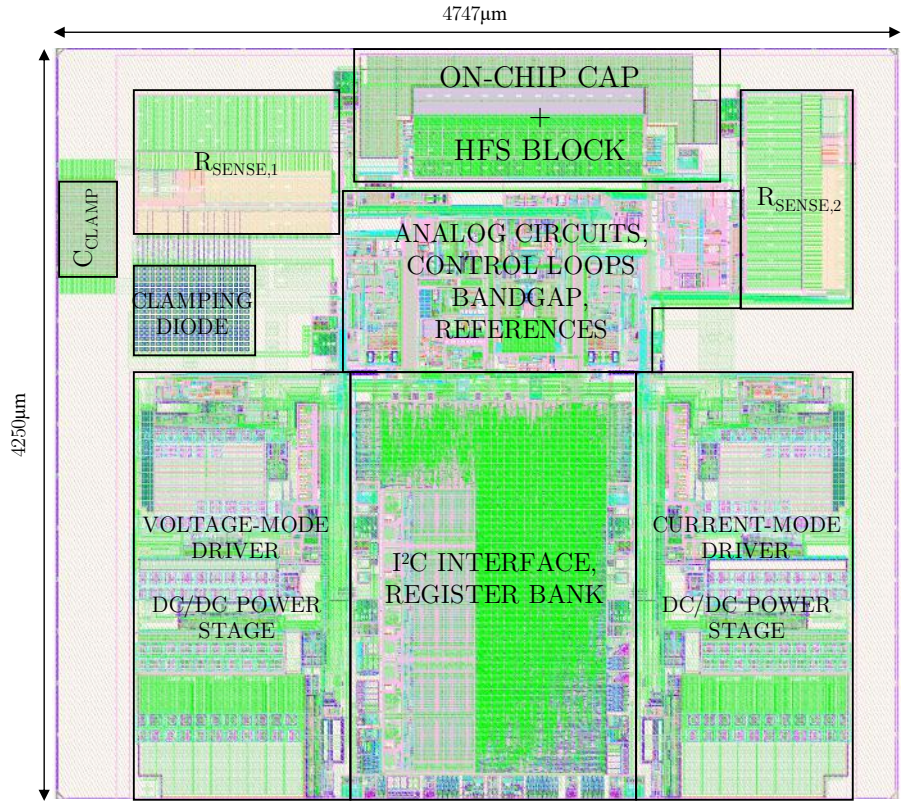


Figure 3.27 – Full layout of the IC prototype (V2). For easy readability, the cell is illustrated without the metal routing.

3.3.13 Redistribution Layer

Figure 3.28 shows the RDL of the chip. The new HFS block is intended to carry high currents. Therefore, I/Os such as V_{SW}, PGND (stands for power ground of the HFS block) and $V_{IN,HFS}$ must be connected to solder balls in a straight vertical way in order to optimize the current flow. They are located above the HFS block. The number of solder balls used for one I/O depends on the maximum DC current. For the HFS block power supply, two solder balls are located on both sides of the HFS block to ensure a symmetry of the current flow through the gate driver. Due to the placement of the clamping diode, a RDL track has been preferred over a conventional metal routing for connecting the anode and cathode pins to the HFS block, as this is less resistive and simplifies the routing. In the same way, the sense resistance $R_{SENSE,2}$ has been routed to the power stage of the current-mode driver through an extended RDL track.

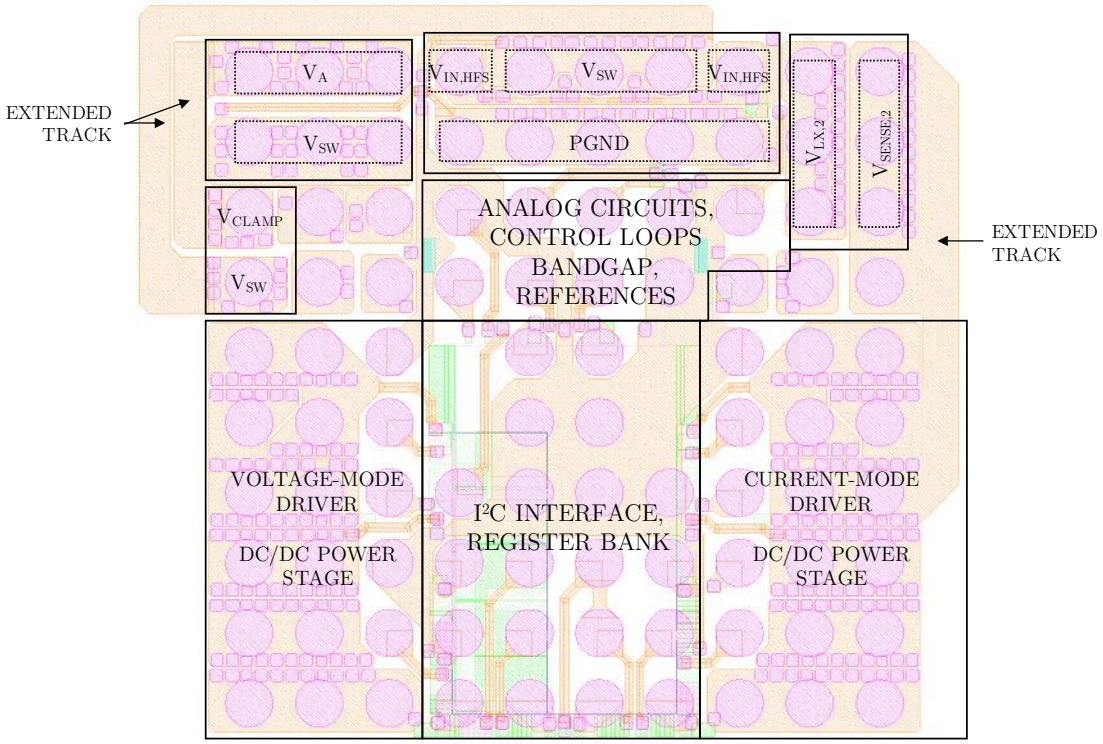


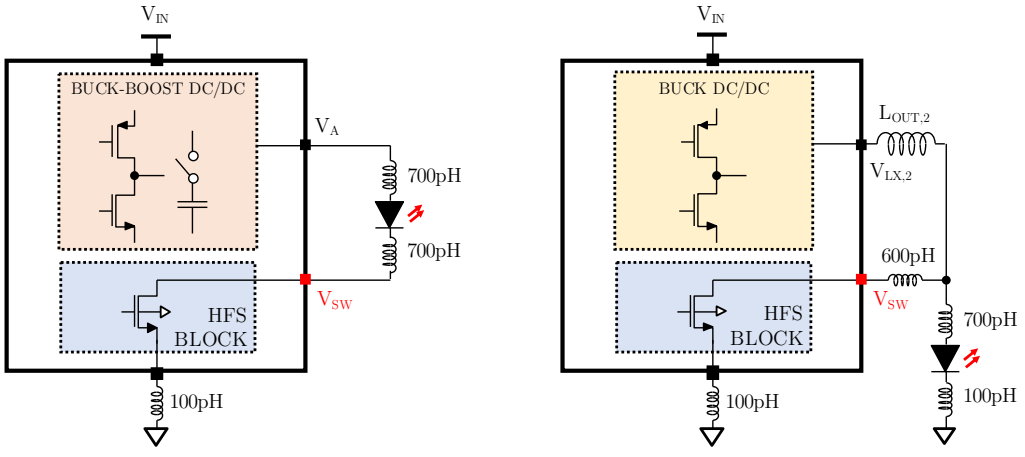
Figure 3.28 – Layout of the redistribution layer.

3.4 Transient simulations

3.4.1 Modeling parasitics

PLSs of the full chip with parasitic models of the package and PCB are necessary to validate the circuit implementation and to evaluate performances of the LDD prototype. The full electrical SPICE-based model of the laser diode is considered here (see Part 2.1.5). A RLCG netlist modeling parasitics for PCB tracks has already been extracted from a previous PCB with similar specifications. It is not the purpose here to deeply model all parasitics within the system. The netlist can be reused to give a first approximation of the impedance for high power and high speed current paths of interest, such as the laser diode path, by primarily modeling parasitic inductances, as illustrated in Figure 3.29.

For the voltage-mode driver, the equivalent stray inductance through the laser diode current path (including the HFS block as a series configuration is employed here) has been evaluated at 1.5nH where 700pH accounts for the laser diode package and 800pH for PCB track and solder ball. For the current-mode driver, the equivalent stray inductance has been evaluated at 800pH through the laser diode current path (700pH from the laser diode package and 100pH from the PCB track to the ground plane), and 700pH through the HFS block current path (as a shunt configuration is employed here). The PDN model previously described is used as well for modeling parasitics along the HFS block power supply rails (see Figure 3.24).



(a) Voltage-mode driver.

(b) Current-mode driver.

Figure 3.29 – Parasitic inductance model of high power paths for both drivers.

3.4.2 Simulation constraints

Transient simulations at transistor level of this kind of circuit including parasitic elements are extremely time and computing resource consuming. For that reason, the full IC prototype including both drivers as well as the digital block (I^2C and registers) has not been simulated. Both drivers, comprising analog and power blocks only, have been considered separately for PLS. Furthermore, only parasitic capacitances of the new HFS block have been extracted. Parasitic elements for each DC/DC converter including control loops have not been extracted. It has been assumed that modifications made for this work are insignificant to be evaluated using PLS, compared to the previous implementation.

3.4.3 Result analysis

Simulations have been carried out in typical conditions (typ. process, 3.6V, 25°C) for a high ON-state current (3A) and high modulation frequency (200MHz) over sufficient switching periods to make the DC/DC converter operating in steady-state. The full driving capability for the gate driver as well as the optimum gate width for the switching element (according to the operating point) have been set. No pre-bias current is considered here. Both 10 IC prototypes have been evaluated, what has required a lot of time (15h for one operating point). Since results for versions implementing a clamping diode are quite similar, only simulation results for V1,V2 and V4 are summarized in Table 3.10. Transient waveforms of interest for both voltage-mode and current-mode drivers (version 2) are illustrated in Figures 3.30 and 3.31 respectively. It is shown the laser diode current I_{DIODE}, the gate-source voltage V_{GS} across transistor T_{SW}, the switching node voltage V_{SW}, the anode voltage V_A and the laser diode forward voltage V_F.

Although a proper gate signal is provided to the switching element, a strong distortion on the laser diode current is noticed. It is caused by the strong parasitic inductances, where the rising time is slower than the falling time for the voltage-mode driver while this is the opposite for the current-mode driver, what confirms preliminary design study results described in Chapter 2. This particularly impacts the current-mode driver where the current is not totally shunted at the end of a pulse, as illustrated in simulation waveforms, bringing an offset that causes the average current through the laser diode to increase, as noticed in Table 3.10. It disturbs as well the average current regulation for the voltage-mode driver leading to a high peak current. The high-frequency distortion is however mostly due to parasitic capacitances from the laser diode electrical model.

Voltage spikes are noticed at the switching node in each case, what seems to be clamped to some extent by the clamping diode, when comparing V1 with other versions. Even if over voltages above 4.8V are reported, the cascode transistor still ensures a protection for the switching element. It can also be noticed that a 5V output voltage against a 3.6V input voltage is required for the voltage-mode driver to reach the targeted current, confirming that a buck-boost structure is essential for this kind of driver topology with respect to

Table 3.10 – Post-layout simulation results for $I_{ON} = 3A$ at 200MHz. Typical conditions have been assumed (typ. process, 3.6V, 25°C).

Parameter	**Value**					
Driver	Voltage-mode			Current-mode		
Version	V1	V2	V4	V1	V2	V4
Pulse width (50%)	3ns	2.6ns	2.7ns	2.3ns	2.7ns	2.3ns
Rising time (10%-90%)	1.2ns	1.8ns	1.8n	950ps	900ps	1.1ns
Falling time (90%-10%)	600ps	900ps	1ns	2.2ns	2ns	1.8ns
Peak current	3.90A	3.43A	3.30A	3.28A	3.6A	3.96A
Average current	1.45A	1.52A	1.45A	2.4A	1.85A	2.07A
Output voltage (V_A)	4.9V	5V	5V	-	-	-
Voltage spike (at V_{SW})	14.5V	7.8V	7.6V	10.3V	7.5V	6.5V
Output power	5.6W	4.2W	4W	7.5W	5W	5.8W
Input power	8.5W	6.9W	6.9W	10W	8.2W	8.9W
Dissipated power in IC	2.7W	2.6W	2.8W	1.9W	2.7W	2.5W
Electrical efficiency	66%	61%	58%	75%	61%	65%

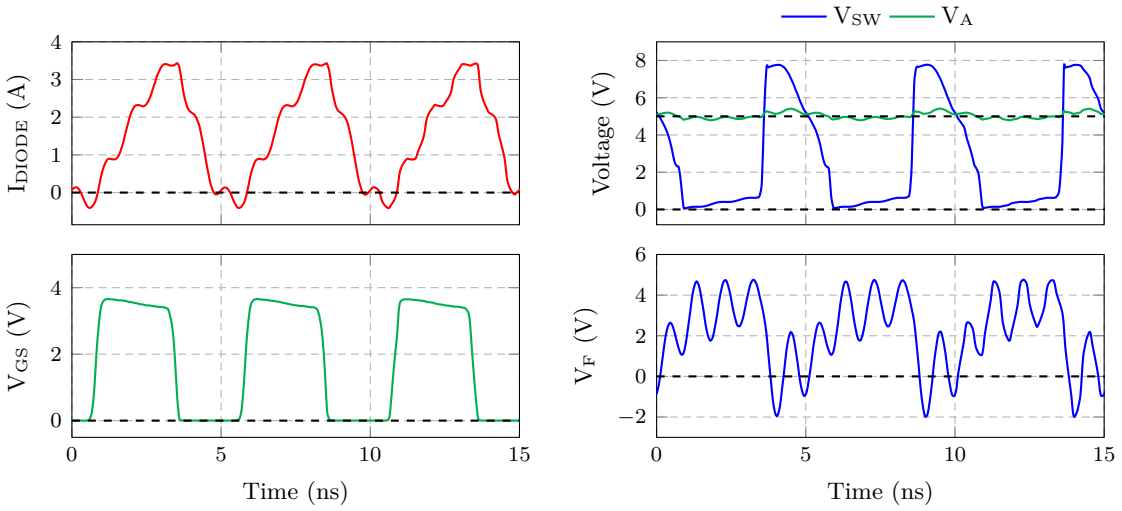


Figure 3.30 – Transient simulation waveforms for the voltage-mode driver (V2) for $I_{ON} = 3A$ at 200MHz. Typical conditions have been assumed (typ. process, 3.6V, 25°C)

specifications.

From Table 3.10, the output power accounts for the average power provided by the driver to the laser diode module during several modulation periods in steady-state while the

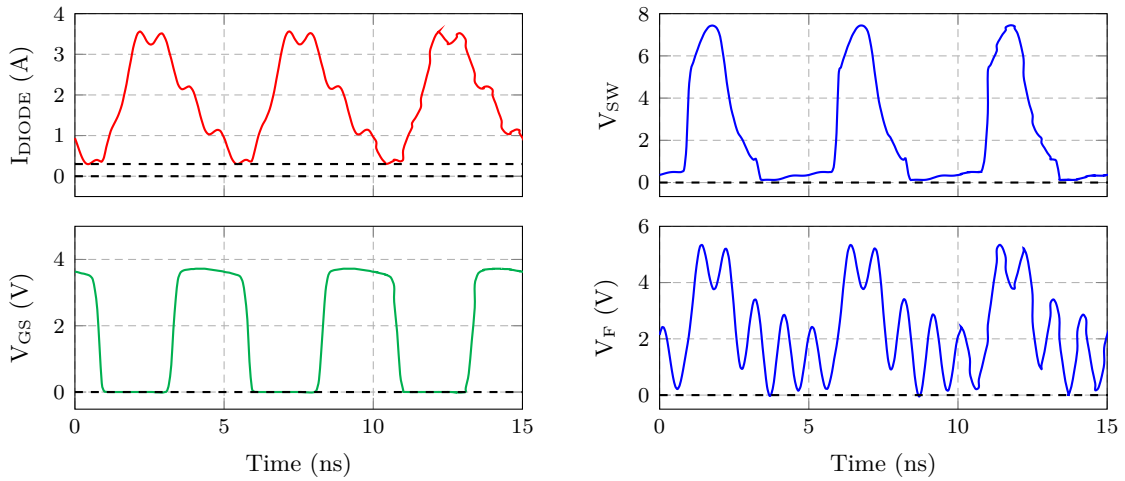


Figure 3.31 – Transient simulation waveforms for the current-mode driver (V2) for $I_{ON} = 3A$ at 200MHz. Typical conditions have been assumed (typ. process, 3.6V, 25°C)

input power is the average power provided by the power supply to the chip during the same time period. The electrical efficiency is calculated with Equation 2.3 using input and output power values. The dissipated power in IC accounts for total losses due to the integrated circuit only, not including off-chip passive components.

Note that the good efficiency result for the current-mode driver version 1 (75%) is quite misleading. As explained earlier, it is caused by parasitic effects that contribute to increase the average current. Even if efficiency values lower than 70% are reported for other versions, the figures seem reasonable in typical conditions at first order.

As a conclusion, although parasitic inductances have a strong impact on transient performances, simulation results validate the circuit implementation, proving that both drivers are able to generate high current pulses at high frequency. The equivalent stray inductance could be reduced with a proper PCB design. These results are however insufficient to properly evaluate performances of the whole system, mostly due to incomplete diode models (both clamping diode and laser diode). Analyzing the optical behavior of the laser diode is still essential for this kind of ToF application.

3.5 Conclusion

This chapter has described the design and implementation of the laser diode driver prototype using the hcmos9a process. In order to save time and design resources, it has been decided to reuse some previous developments, comprising two DC/DC converters for implementing both voltage-mode and current-mode drivers. In this way, only a single chip

was considered. A new HFS block has thus been designed to provide the high-frequency current switching. Protection circuits, such as a clamping diode and a cascode structure, were required to prevent any damage caused to the laser diode and devices within the chip, due to potential high voltage spikes occurring during fast transients. Since clamping diode models are incomplete, several prototypes implementing various combinations of devices have been considered for testing. A proper layout of the chip has been realized taking into account a strong isolation of devices and building blocks to minimize the substrate coupling and susceptibility to latch-up. Once the circuit implementation validated thanks to simulations, 10 IC prototypes have been sent for fabrication, comprising the die manufacturing and the packaging through several industrial partners. Unfortunately, no micro-photograph of the die is available.

A test board is required in order to configure and test the IC prototypes. A proper PCB design with optimized interconnections as well as a large ground plane and thermal VIAs is thus essential to reduce parasitic inductances and to improve the thermal dissipation [152]. Other considerations related to electrical and optical measurements are detailed in Chapter 4.

4 Tests and Measurement Results

Contents

This chapter details electrical and optical measurement results obtained on IC prototypes. Some considerations for designing a suitable test board and performing measurements are reviewed. Major issues concern the acquisition of the laser signal as well as current and voltage signals at such power and speed levels while accommodating eye-safety standards. Another concern is about electrical and optical power measurements, such as losses and efficiency. A debugging process for checking the various features of the circuit is done before to carry out a set of measurements. Performance results are then discussed.

4.1 Test Board and Experimental Setup

This section gives some considerations for designing the test board and performing measurements. It then presents an overview of the various test boards and describes the experimental setup. A design of experiment is also proposed.

4.1.1 Design considerations for the test board

A test board is required for mounting components as well as configuring and testing the IC prototypes. A microcontroller with an I^2C interface is used to provide control signals to the chip. It has been decided to develop three test boards:

- a board for debugging and validating various features of the circuit including both drivers (referred to as the "validation" board),

- a board for measuring electrical and optical performances, featuring an optimized design for the voltage-mode driver only (referred to as the "voltage-mode" board),
- a board for measuring electrical and optical performances, featuring an optimized design related to the current-mode driver only (referred to as the "current-mode" board).

Since both drivers are implemented within the chip, a special care must be considered at board design level to perform tests without affecting the functionalities and performances of one driver regarding the other. A careful layout, components placement and routing are required to ensure a proper operation of each board. PCB tracks must be as less resistive and inductive as possible for high power and high speed current paths. Stacked planes as well as tracks carrying current in reverse directions would be preferred in order to minimize loop inductances. The VCSEL module and other off-chip components must be placed as close as possible to the chip. A large ground plane and thermal VIAs are used to improve the thermal dissipation of the board [152].

4.1.2 Experimental considerations

The major challenge here is to perform both electrical and optical measurements with a sufficient accuracy without impacting performances of the system. The experimental setup must face strong constraints related to

- high levels of power and short-duration pulses at high repetition frequency,
- eye-safety standards due to the use of a laser diode at such levels of power,
- small dimensions of the circuit and components.

4.1.2.1 Laser safety enclosure

The testing environment has to be laser safety standard compliant in order to perform safe measurements when using the laser diode. A laser safety enclosure (or box) is used for that purpose, where the system under test (test board with assembled components) is placed. The box is also protected with an electrical interlock able to shutdown the power supply, thus switching off the laser diode, if the door is unintentionally opened. In addition, measurements could be performed in a dark room using laser safety glasses.

4.1.2.2 Time-domain measurement

The main concern for the acquisition of both electrical and optical signals in the time domain is the limited bandwidth of the equipment as well as the probing method. Here, electrical signals concern the current and voltage while optical signals concern the laser signal. The latter may also refer to as the laser pulse shape (optical power vs. time) [44].

Electrical signals When measuring current or voltage, any probe adds parasitic elements (resistance, capacitance and/or inductance) that may impact the waveforms and performances of the circuit [153][110]. A high-bandwidth measurement equipment with an appropriate probing technique is thus required in this context [154][155]. Both single-ended and differential probes could be used for measuring voltages, depending on whether ground-referenced or floating measurements are performed. Other selection criteria include the bandwidth, voltage range or probe loading.

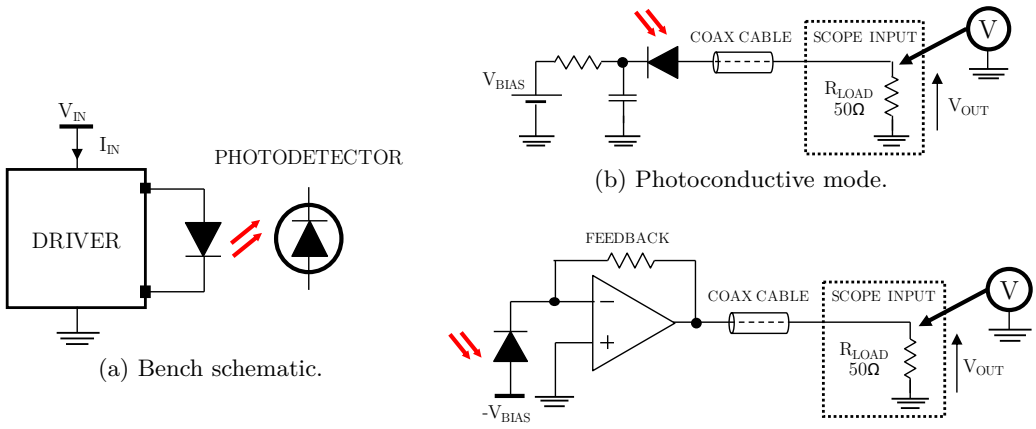
Measuring the current through the voltage drop across a current sense ("shunt") resistor built into the design could be preferred over the use of a current probe. Indeed, a current probe head must encircle a conductor which can be complex to implement against small dimensions of the circuit and components. However, introducing a shunt resistor in series with the load may increase the voltage drop and the equivalent stray inductance in the path, which is very critical in this context. As a consequence, this measurement method should be employed for debugging purpose only. In other cases, it has been decided not to measure the laser diode current waveform but only to estimate the peak current value I_{PEAK} by using optical power measurement and VCSEL's characteristics, such as

$$I_{PEAK} = \frac{P_{OPT(PEAK)}}{\eta_{VCSEL}} + I_{th} \tag{4.1}$$

where $P_{OPT(PEAK)}$ is the peak optical power of the laser pulse, η_{VCSEL} is the slope efficiency and I_{th} is the threshold current. The two latter parameters derive from the VCSEL's datasheet (see Part 2.1.4) and are still given for 25°C only. It has been assumed to consider η_{VCSEL}=90% and I_{th}=300mA.

Laser pulse shape Acquiring the laser pulse shape allows to measure transient performances such as the pulse width, rising and falling times. A high-bandwidth measurement equipment is thus necessary here. A high-speed free-space photodetector could be used for simplifying the setup, compared to a fiber-coupled configuration that involves a more complex and cumbersome optical instrumentation. Since the photodetector is very sensitive to the incident light beam divergence, a careful alignment with the laser diode would be required. Criteria for selecting a photodetector include sensitivity for the wavelength of interest, gain, noise and speed. It must be specified that a photodetector does not allow to measure optical power.

For pulse width measurement, the photodetector is used in photoconductive mode where the photodiode is reverse biased for reducing its junction capacitance thus improving the bandwidth [156][157] as illustrated in Figure 4.1b. The generated photocurrent is proportional to the incident light power. It is then converted into voltage through the scope input acting as a 50Ω load. The circuit may include a RC filter to remove any high frequency noise from the input supply, which otherwise may contribute to a noisy output. The photodetector can be used with a transimpedance amplifier to achieve a high gain [156][157] as illustrated in Figure 4.1c.



(a) Bench schematic.

(b) Photoconductive mode.

(c) Amplified photodetector circuit.

Figure 4.1 – Illustration of the optical bench for acquiring the laser pulse shape by using a photodetector.

4.1.2.3 Power measurement

Here, power measurement concerns both electrical and optical quantities, but different concerns must be addressed.

Optical power Measuring optical power allows to estimate the electro-optical efficiency of the system including the driver and the VCSEL module. It is given by

$$\eta_{OPT} = \frac{P_{OPT(AVG)}}{P_{IN}} \tag{4.2}$$

where $P_{OPT(AVG)}$ is the average optical power emitted by the VCSEL module and P_{IN} is the input electrical power consumed by the driver. Here, these quantities are averaged over a pulse train. Indeed, it is most interesting to study the driver behavior when it is consuming the most part of the energy compared to idle times. As the input power is delivered by the power supply, using a suitable equipment such as a Source-Measurement Unit (SMU) allows to access this value.

Measuring the optical power may be achieved by using an integrating sphere in association with a power detector and power meter. The integrating sphere allows for the total collection of the electromagnetic radiation from a source. Radiation hitting the reflective walls of the sphere is uniformly scattered, as illustrated in Figure 4.2. The resulting integrated radiation level is directly proportional to the initial radiation level and may be measured using a detector [158]. A major advantage of using an integrating sphere is to diffuse the input beam so that the detector readings are insensitive to errors caused by detector positioning or problems associated with overfilling, or saturation of the active

area of the detector. Nevertheless, the limited dimensions of the sphere input port should be taken into account for the placement and routing of components on PCB.

This kind of setup is however intended for continuous-wave or pulsed light sources, including frequency measurements of pulses up to 250kHz [159]. In this context, it could be employed for measuring the average optical power of a pulse train. The peak optical power of pulses $P_{OPT(PEAK)}$ is determined by knowing other temporal information such as the laser pulse shape, modulation frequency and duty cycle, as expressed in an ideal case by

$$P_{OPT(PEAK)} = \frac{P_{OPT(AVG)}}{\alpha} \tag{4.3}$$

where $P_{OPT(AVG)}$ is the average optical power emitted by the VCSEL module and α is the modulation duty cycle. Note that before use, the integrating sphere associated to the power detector and power meter must be calibrated.

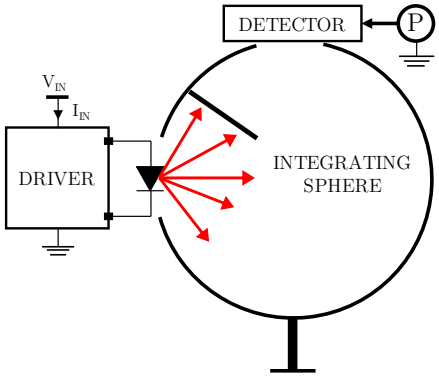


Figure 4.2 – Illustration of the optical bench for measuring optical power with an integrating sphere. The symbol "P" represents the power meter.

Electrical power Estimating the electrical efficiency of the driver involves to measure the input and output powers. The expression of the efficiency is reminded hereafter:

$$\eta_{ELEC} = \frac{P_{OUT}}{P_{IN}} \tag{4.4}$$

where P_{IN} is the input electrical power consumed by the driver and P_{OUT} is the output electrical power provided by the driver to the laser diode. As before, these quantities are averaged over a pulse train. The input power can easily be read using the SMU. On the other hand, the output power measurement is a more challenging task. Usually, a digital oscilloscope computing the product of the current and voltage is employed when low-frequency signals are considered. But the accuracy of digital measurement is greatly impacted at higher frequencies by the delays introduced between probes, phase shifts

between sampling channels of the digitizer, sampling errors and nonlinearities of analog-to-digital converter [160]. Another method relies on the calorimetry, measuring power losses as heat that a device dissipates when operating within a measurement chamber [160]. It is however complex to implement, particularly in this optical context.

It is thus proposed to estimate the output electrical power by using optical power measurement and VCSEL's characteristics, such as

$$P_{OUT} = \frac{P_{OPT}}{\text{PCE}(@I_{PEAK})} \tag{4.5}$$

where P_{OPT} is the average optical power emitted by the VCSEL module and PCE is the power conversion efficiency given for the corresponding peak current. The PCE parameter derives from the VCSEL's datasheet where it is given for a current from 0 up to 3.5A.

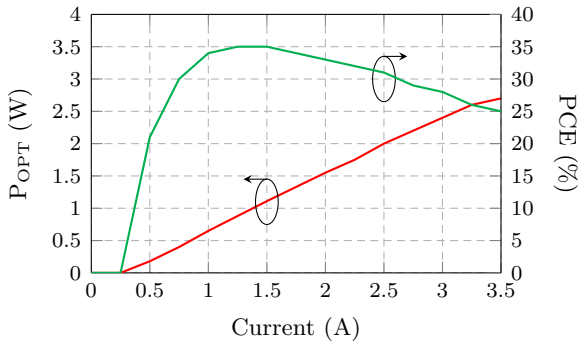


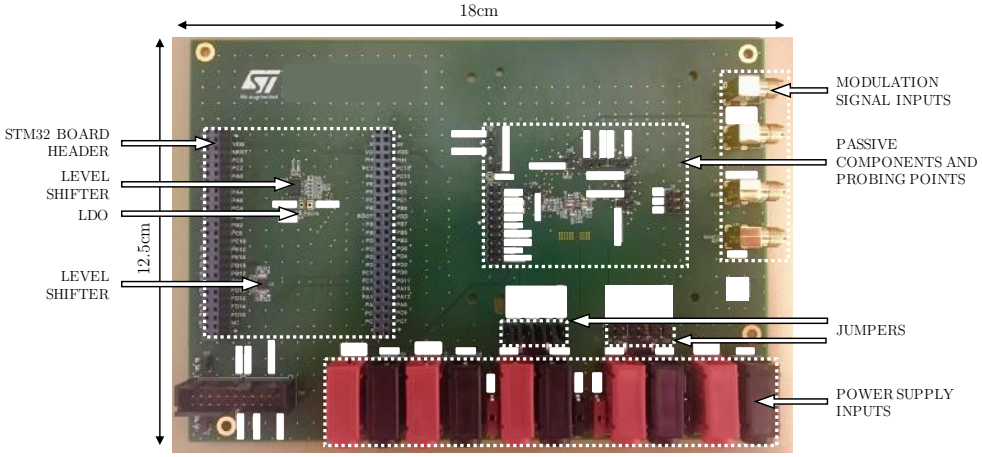
Figure 4.3 – VCSEL DC characteristic curves from datasheet: output optical power and power conversion efficiency vs. current (given at 25°C).

Estimations of the peak current as well as the output electrical power are only valid when considering current values within the linear region of the VCSEL characteristic curve. It cannot be applied for current values near the threshold current where non-linear effects are significant. Therefore, results should be used with caution.

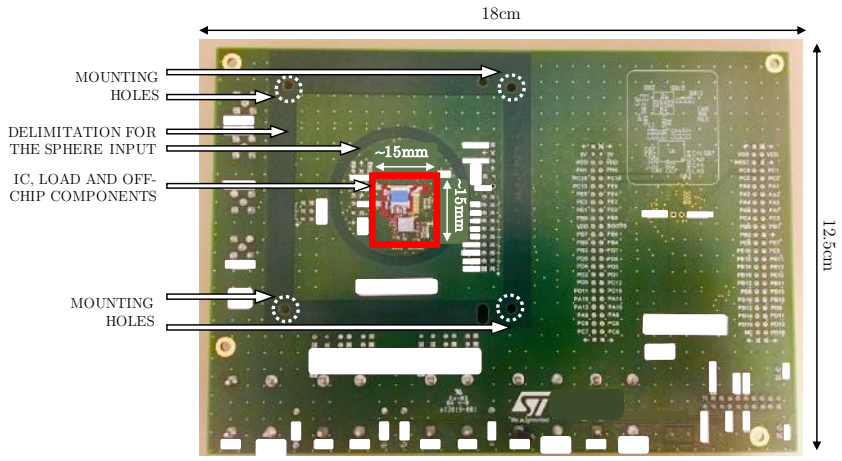
4.1.3 Test board overview

The PCB design and layout were realized through different members within the department at STMicroelectronics, based on considerations previously detailed. All test boards rely on a double-sided PCB using 6 layers in order to properly route all signals and power supply paths, featuring a wide common ground plane on layer 3. PCB tracks are made of copper while the dielectric is a FR4 glass epoxy dielectric. Boards have a size of 12.5cmx18cm. They feature a similar layout and include common features for simplifying the setting and measurement procedures. A picture of the validation board is shown in Figure 4.4 with features highlighted. Some mounting holes are machined to attach the

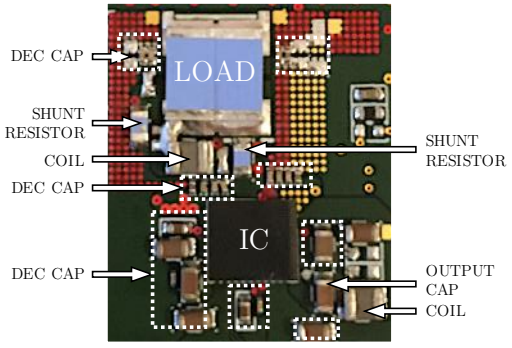
board to the integrating sphere. All test boards include a version of the IC prototype ($5mm^2$), a load and off-chip passive components located in a small area (red box in Figure 4.4b, around $15mm^2$) due to physical constraints related to the integrating sphere and for limiting parasitic elements. A zoom on this area is also presented in Figure 4.4. It is specified that the "voltage-mode" and "current-mode" boards embed only four small 0603M ceramic capacitors (22nF, 10nF, 4.7nF and 2.2nF) as decoupling capacitors for the HFS power supply in order to limite the PCB footprint. Common features are presented hereafter.



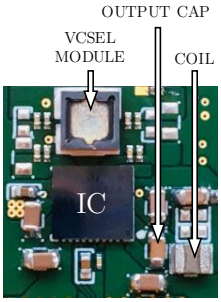
(a) Top view.



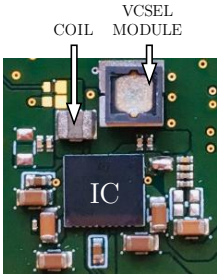
(b) Bottom view.



(c) Validation board.



(d) Voltage-mode board.



(e) Current-mode board.

Figure 4.4 – Pictures of test board: (a) top and (b) bottom views. For confidentiality reasons, labels have been hidden. Zoom views (c), (d) and (e) present the IC, load and off-chip components.

Control interface Headers for a microcontroller board are provided. A STMicroelectronics STM32F407 microcontroller board is well suited in this context. The reader could be asked why using another microcontroller ;) ? Level-shifters are however added to translate 3.3V control signals from the STM32 board to 1.8V signals required by the core digital block of the chip.

Power supply interface Multiple power supply paths are provided to properly supply analog, digital and power blocks of the chip, through input terminals (red and black banana connectors as usual). In this way, it allows to access the current consumption from each block by using the suitable equipment, such as a SMU. Sense connections are also provided for a better precision. Jumper connectors are used for flexibility.

A supply voltage from 2.5V up to 4.8V is required for the power and analog blocks, provided by an external generator, while a 1.8V supply voltage is necessary for the core digital block. A LDO regulator is used for that purpose, providing a 1.8V voltage level from the 5V supply voltage of the STM32 board.

Modulation signal interface Several inputs are provided for modulation signals, through SMA (standing for SubMiniature version A) connectors. The high-frequency differential modulation signal for controlling the switching element as well as the low-frequency modulation signal for controlling the pulse train envelope, are generated by external devices. Some passive components have been implemented in order to adapt LVDS inputs by using a termination resistor (usually 100Ω) and to ensure the impedance matching of the transmission line [133].

Probing points Some probing points are provided to access signals of interest. They must be used for a debugging purpose only as they may add parasitic elements, thus impacting high-frequency measurements.

Validation board It includes all components related to both the voltage-mode and current-mode drivers. A resistive load or a silicon diode instead of the laser diode can be used in a first approach for debugging and validating the IC prototype in a standard test environment (without optical constraints). Nevertheless, solder bridges and/or jumper connectors are used to connect or disconnect the relevant components, depending on the tested driver. It may help avoiding short circuits and give more flexibility to switch between the different loads. Moreover, adding a low inductance resistor in the load path can be useful to probe the current, as discussed earlier. A test bench schematic dedicated to the validation board is shown in Figure 4.5.

Voltage-mode board It includes all components related to the voltage-mode driver. It however remains some other components related to the current-mode driver to ensure

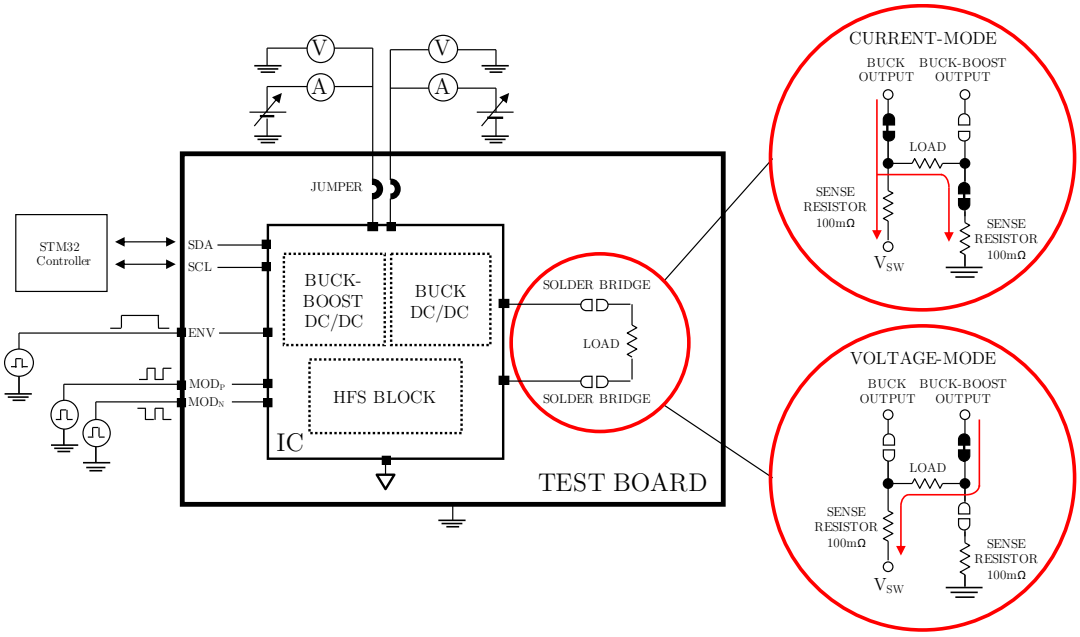


Figure 4.5 – Test bench schematic related to the validation board. A zoom presents solder bridge connections for the voltage-mode and current-mode configurations.

a proper operation of the system. Since the purpose of this board is to primarily perform optical measurements, only the laser diode is assembled.

Current-mode board It includes all components related to the current-mode driver. It however remains some other components related to the voltage-mode driver to ensure a proper operation of the system. Since the purpose of this board is to primarily perform optical measurements, only the laser diode is assembled.

4.1.4 Experimental setup

A test bench has been set up in order to perform electrical and optical measurements. A picture is shown in Figure 4.7. The equipment used is listed hereafter:

- DC voltage generator: Keysight N6705B DC power analyzer
- Pulse generator for high-speed modulation signals: Agilent 81110A pulse/pattern generator
- Waveform generator for envelope signal: Keysight 33600A waveform generator
- Oscilloscope: Keysight MSOS254A 2.5GHz mixed-signal oscilloscope
- Microcontroller: STMicroelectronics STM32F407 microcontroller board
- Spectrometer: Avantes ULS3647 high-resolution spectrometer
- Integrating sphere: Newport 819D-SL-5.3-CAL2 integrating sphere

- Power detector: Newport 918D-SL-OD1R optical power detector
- Power meter: Newport 1936-R optical power meter
- High-speed photodetector:
  - iC-Haus ic212 1.4Ghz high-speed free space photodetector (InGaAs detector with "No Slow Tail" option)
  - Thorlabs DET08CL 5GHz InGaAs free-space photodetector
  - Newport 818-BB-21 1.2GHz Si free-space photodetector
  - Newport 818-BB-21A 1.2GHz Si free-space amplified photodetector
- Probes:
  - Keysight N2752A 6GHz active differential probe
  - Keysight N2873A 500MHz passive probe
- Laser safety glasses: Thorlabs LG1 glasses

An important point must be specified when selecting a high-speed photodetector for acquiring the laser pulse shape. Four different photodetectors matched to this context have been tested with a laser diode driver. A "slow tail" has been noticed in the laser pulse shape when using the Thorlabs DET08CL and Newport 818-BB-21 (amplified or not) photodetectors, as compared to results when using the iC-Haus ic212 photodetector, as shown in Figure 4.6. It seems that high-frequency effects are filtered. In fact, this kind of slow tail is due likely to the diffusion current when carriers are generated outside the depletion layer of the detector [161]. This issue seems to be caused by the divergent beam of the VCSEL module that is not sufficiently focalized on the photosensitive area. In this context, it is highly recommended to use the iC-Haus ic212 photodetector.

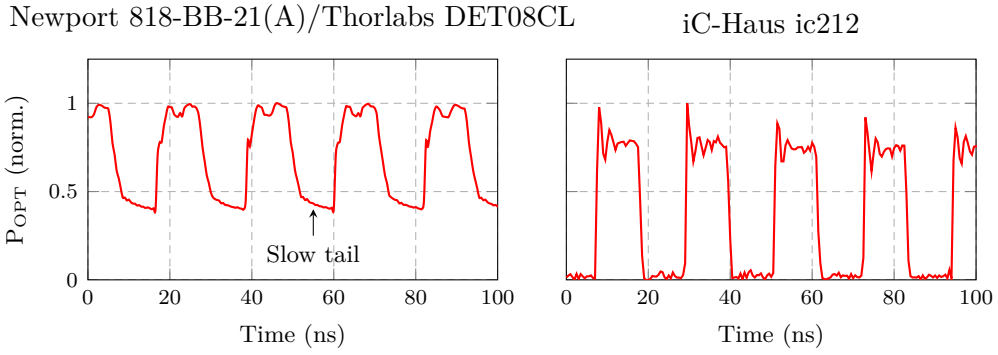
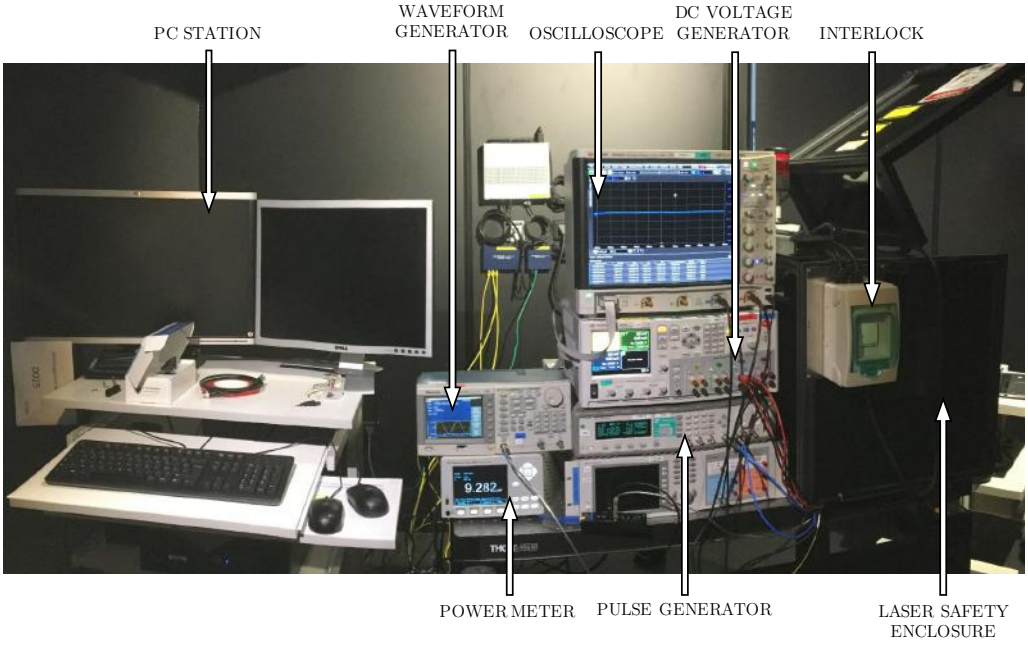
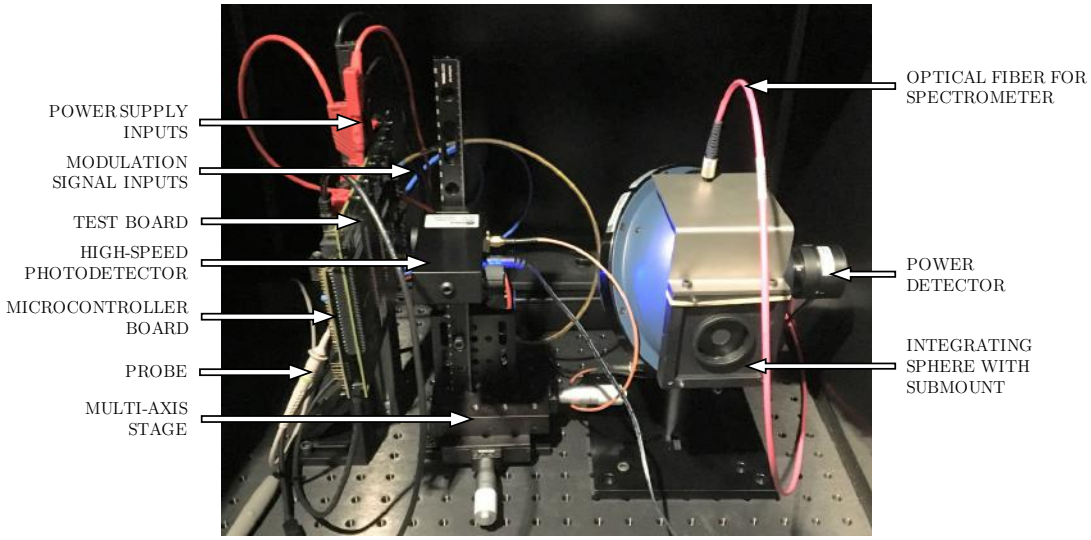


Figure 4.6 – Laser pulse shape acquired with various high-speed photodetectors. Waveforms are normalized on y-axis according to their maximum value. The modulation frequency is 50MHz.



(a) Test bench.



(b) View from inside the enclosure. In this configuration, the test board is used with the high-speed photodetector. It must be attached to the sphere submount for being used with the sphere.

Figure 4.7 – Pictures of the test bench, settled in a dark room. A view from inside the laser safety enclosure presents the test board along with the photodetector and integrating sphere.

4.1.5 Design of experiment

As a reminder, it has been chosen to implement both the voltage-mode and current-mode driving topologies due to limited results from the preliminary design study (see Chapter 2). In the same way, various versions of IC prototypes have been manufactured due to incomplete simulation models (see Chapter 3). It is thus proposed a design of experiment in order to check various features of the chip in a first time and to measure performances of both drivers in different versions in a second time.

4.1.5.1 IC prototype debugging

The first step is to turn on the chip and check its electrical behavior under DC conditions, meaning when operating with a load but without switching the current at high frequency. This aims to check if the DC/DC converter and HFS block are operating as expected and irrespective of the high-frequency modulation. Major features to be checked are the current regulation through current-control loop circuits, the on-channel resistance characterization of the switching element according to its configurable gate width, the pre-bias current source characterization (for the voltage-mode driver only) and the clamping diode characterization.

4.1.5.2 IC prototype measurement

The second step is to measure performances of the system, in terms of transient (rising and falling times, pulse width) and power (electrical and optical efficiencies) measurements. The LDD prototypes should be tested as well when operating with a ToF image sensor in order to validate the system at application level. Various features, such as the gate width selection of the switching element for optimizing losses, the configurable driving capability of the gate driver and the pre-bias current source should be investigated. Electromagnetic Interference (EMI) should be investigated as well by measuring the impact of the high-frequency current switching on the electrical and optical behaviors of the driver. Furthermore, measuring the impact of the clamping diode would allow distinguishing the different versions of IC prototypes.

A first set of measurements could performed for a typical use case (3A ON-state current, 200MHz modulation frequency) under typical conditions (3.6V input voltage, 25°C) in order to validate the driver operating principle. Then, parameters could be swept in order to test the drivers in various conditions. This would allow to get a relevant comparison of drivers. It must be clarified that the variation with temperature will not be investigated.

4.1.5.3 Comparative analysis

Lastly, a comparative analysis, gathering all measurement results, should be carried out in order to conclude about which driver is the most suitable for the iToF-based image sensor

with respect to specifications described in General Introduction.

4.2 IC Prototype Debugging

This section presents the debugging procedure of IC prototypes by using validation boards, that have been received in early November 2019. Only a resistive load (two 2Ω low inductance resistors connected in parallel) has been used for debugging the circuit. Due to a short schedule related to the industrial context, major features have been checked under typical conditions only. Parameters, such as the input voltage, have not been swept.

4.2.1 DC/DC converters

In order to check the behavior of DC/DC converters under DC conditions without inducing a self-heating effect, a relatively short current pulse (~200µs) is configured with a sufficiently long off-time. The current amplitude is set according to the targeted current through the I^2C interface. The output current is then measured by sensing the voltage across the resistive load. The gate width of the switching element has been configured on its maximum size (86.4mm, see Part 3.3.4) to benefit from a low resistance. Results for the voltage-mode and current-mode drivers are detailed hereafter.

4.2.1.1 Voltage-mode driver: current regulation

First measurements have shown that the DC/DC converter of the voltage-mode driver worked properly. Waveforms of interest for a 3A targeted current under typical conditions (3.6V, 25°C) are illustrated in Figure 4.8. The converter operates in boost mode with a 4MHz operating frequency, as expected. Results when sweeping the targeted current from 0 up to 3A, under typical conditions, are illustrated in Figure 4.9. A very good agreement between theory, simulation and measurement is shown as results are straight lines well superimposed. A very low standard deviation of the measured current is noticed as well, showing no stability issue. A similar behavior has been noticed for other IC prototype versions and for different input voltages, meaning that the DC/DC converter operates properly at first glance.

4.2.1.2 Current-mode driver: current regulation

First measurement for the current-mode driver have shown an erratic behavior with stability issues particularly for low output currents. Waveforms of interest for a 2.5A and 0.5A targeted current under typical conditions (3.6V, 25°C) are illustrated in Figure 4.10. The DC/DC converter operates in buck mode with a 4MHz operating frequency as expected. In addition, the switching of the power stage causes the output current to have a triangular ripple since no output capacitor is considered here, as expected as well. However, the duty cycle of the PWM circuit (named α in Figure 4.10) is unstable at low output currents,

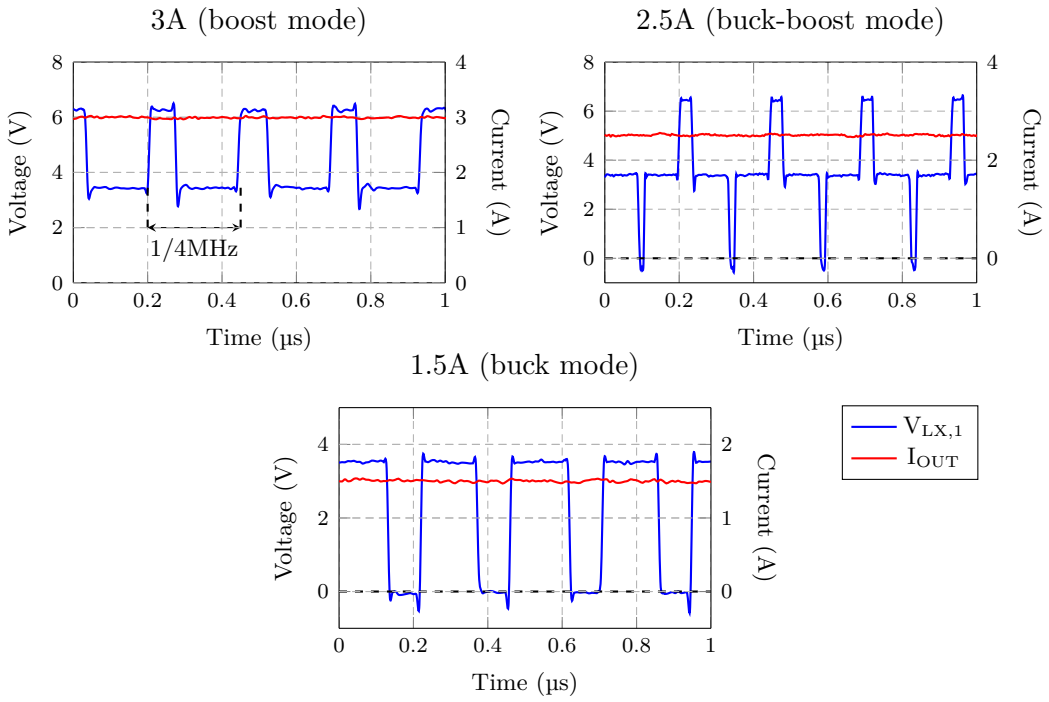


Figure 4.8 – Transient measurement waveforms for the voltage-mode driver (V1) for various targeted currents under typical conditions (3.6V, 25°C).

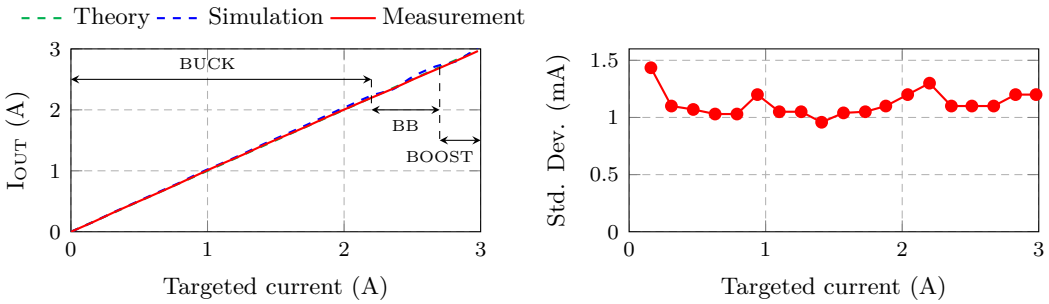


Figure 4.9 – Measured output current (left) and standard deviation (right) vs. targeted current for the voltage-mode driver (V1) under typical conditions (3.6V, 25°C). The operating mode of the converter is indicated.

thus disturbing the current regulation. The same behavior can be noticed for various low output currents, as shown in Figure 4.11. Furthermore, the converter does not seem to be able to provide a high output current. This is caused by the resistive load inducing a high output voltage (IR-drop) under DC conditions. Under normal operating conditions (when switching the laser diode current), the effective output voltage should be lower, as

explained by Equation 2.22.

Some disturbances have been noticed on the bandgap voltage reference circuit whatever is the output current, as seen in Figure 4.12. This circuit is intended to provide a fixed voltage of 1.22V used by current-control loop circuits. The bandgap voltage has been measured through a dedicated test point from the IC. In that case, although the average value is 1.22V, voltage spikes synchronously occur with the switching of the power stage. Disturbances could be caused by a coupling between the DC/DC converter and the bandgap circuit through internal and/or external interconnections (further discussed in Part 4.3.1.3).

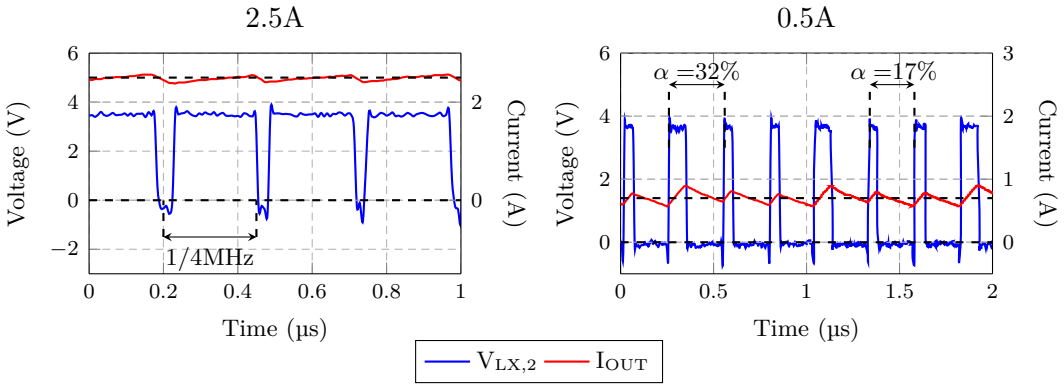


Figure 4.10 – Transient measurement waveforms for the current-mode driver (V1) for various targeted currents under typical conditions (3.6V, 25°C).

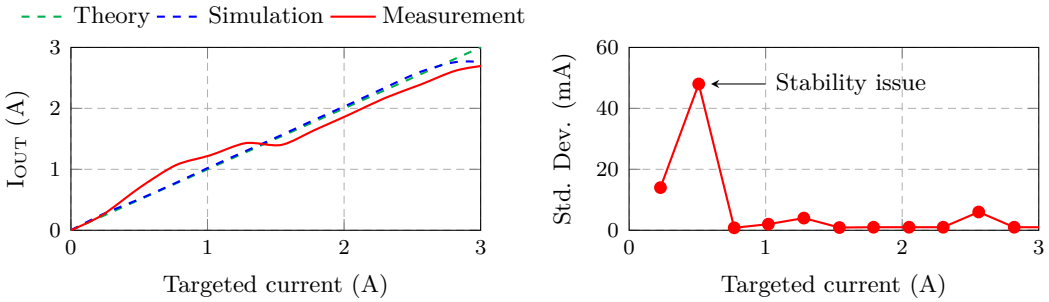


Figure 4.11 – Measured output current (left) and standard deviation (right) vs. targeted current for the current-mode driver (V1) under typical conditions (3.6V, 25°C).

At last, similar issues have been reported for other IC prototype versions and for different input voltages. This means that the DC/DC converter of the current-mode driver does not operate properly at first glance.

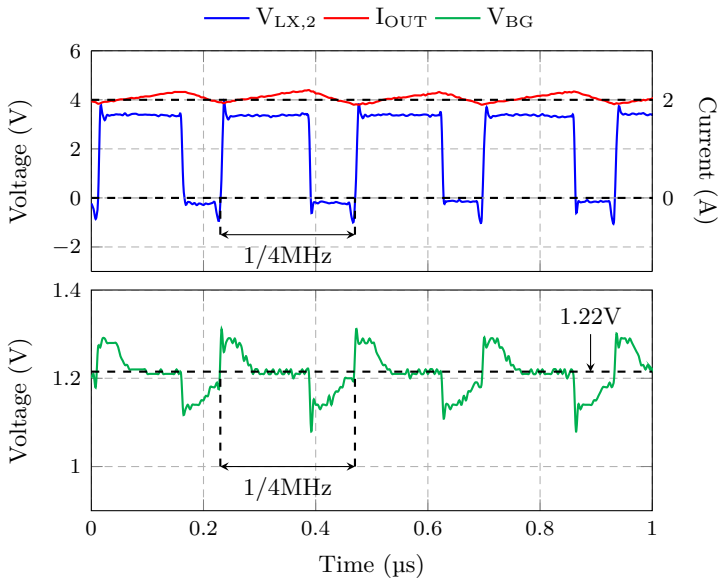


Figure 4.12 – Transient measurement waveforms for the current-mode driver (V1) for a 2A targeted current under typical conditions (3.6V, 25°C). It shows disturbances on the bandgap voltage.

4.2.2 HFS block

In order to characterize the on-channel resistance of the switching element, the pre-bias current source and the clamping diode without inducing a self-heating effect, pulsed conditions have been used. A relatively short voltage or current pulse (~200µs) with a sufficiently long off-time is thus provided by the power analyzer to the relevant pin of the chip.

4.2.2.1 On-channel resistance characterization

The on-channel resistance of the switching element is unfortunately not accessible due to technical issue. It is thus proposed to characterize the total on-resistance of the switching element and the cascode device by measuring the total drain-source voltage $V_{DS(TOT)}$ across both devices for a given DC current I_{DC} supplied by the power analyzer. Solder bridges and jumper connectors on the board have been arranged accordingly. The total on-resistance $R_{ON(TOT)}$ is expressed as

$$R_{ON(TOT)} = \frac{V_{DS(TOT)}}{I_{DC}} \tag{4.6}$$

The voltage measurement is performed as close as possible to pin V_{SW}. It may however include the voltage drop across bumps and residual PCB tracks. The total on-resistance has been characterized for various gate width values (from 5.4mm up to 86.4mm by step of 5.4mm). Results for both GO2 and HVDrift 18V cascode devices and for various DC

current levels under typical conditions (3.6V, 25°C) are shown in Figure 4.13.

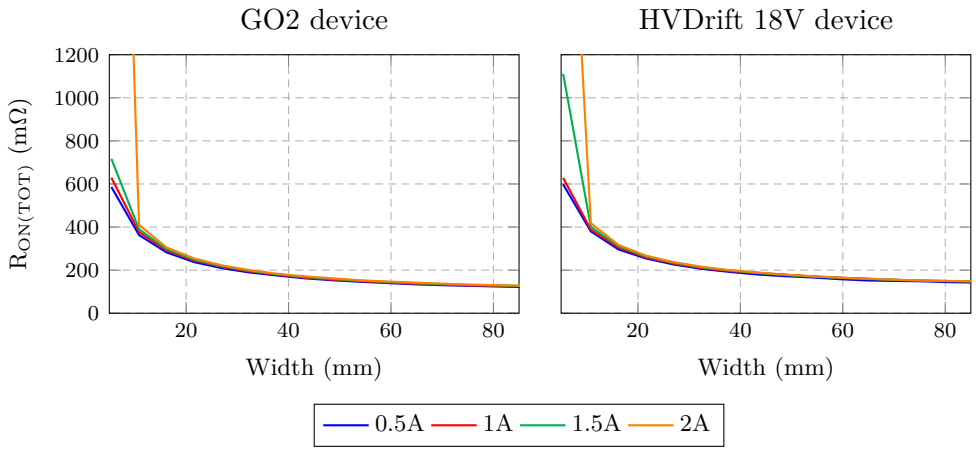


Figure 4.13 – Measured total on-resistance of the switching element and cascode device vs. gate width for various DC current levels and under typical conditions (3.6V, 25°C).

The total on-resistance decreases as the gate width increases, as expected. Nevertheless, measurement curves for various DC currents are supposed to be superimposed over the whole range. A deviation is noticed for small gate widths and high DC currents. This is due to the cascode device and switching element that operate close to the saturation region. The complex metallization network connecting the cascode device to each part of the switching element contributes to increase the total on-resistance as well (see Part 3.3.3). For that reason, it is recommended to use a gate width larger than 15mm in order to ensure a total on-resistance sufficiently low, particularly for the current-mode driver (<400mΩ, see Part 3.2.2.4).

4.2.2.2 Pre-bias current source characterization

The pre-bias current source is characterized for the voltage-mode driver only by measuring the current drawn by the power analyzer when applying a given voltage at pin V_{SW}. Solder bridges and jumper connectors on the board have been arranged accordingly. The pre-bias current is swept from 0mA up to 550mA by step of 35mA through the I^2C interface. Under normal operating conditions, the drain node V_D (see Figure 3.8) can be floating depending on the biasing conditions of the load and the cascode device. It is thus proposed to apply various voltage levels (1V and 2.5V for instance) at pin V_{SW} in order to evaluate the stability of the current source under different biasing conditions. Results under typical conditions (3.6V, 25°C) are shown in Figure 4.14.

The pre-bias current source increases as the targeted current increases according to a

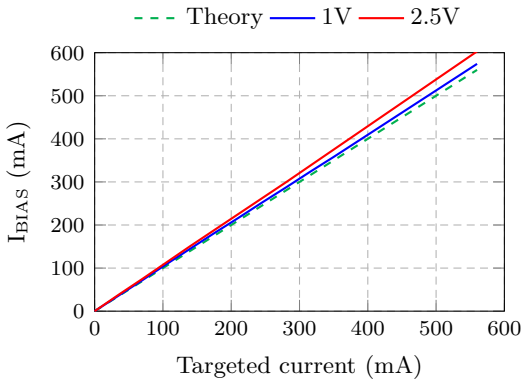


Figure 4.14 – Measured pre-bias current vs. targeted current for the voltage-mode driver (V1) for various voltage levels of the switching node and under typical conditions (3.6V, 25°C).

straight line, as expected. A deviation is however noticed at high current values for a high voltage level (2.5V). This issue comes from both the matching in drain-source voltages and channel-length modulation parameter λ_{MOSFET}. The third current mirror is impacted by the voltage variations while the first and second current mirrors are still powered under a fixed input voltage (3.6V). This is due to the finite output resistance of devices ($\lambda_{MOSFET} \neq 0$). A similar behavior has been noticed with a GO2 cascode device. Anyway, it is not a major issue since this feature is intended for testing in a first step, and because a high accuracy is not essential in this context. A cascode mirror structure could be used to improve the accuracy against voltage variations [131].

4.2.2.3 Clamping diode characterization

The clamping diode is characterized by measuring the current drawn by the power analyzer when applying a given voltage across the diode. Solder bridges and jumper connectors on the board have been arranged accordingly. The DC characteristic curves measured under typical conditions (25°C) for both Schottky and P-N junction diodes are plotted in Figure 4.15 along with simulation results. It is clarified that the forward voltage may include the voltage drop across bumps and residual PCB tracks.

A good agreement between simulation and measurement results is obtained for the Schottky diode. The threshold voltage is estimated around 0.3V, as expected. Nonetheless, a large deviation is noticed between simulation and measurement results for the P-N junction diode above the threshold voltage, estimated around 0.7V. This is due to the incomplete diode model used for simulation, what is an expected result so far.

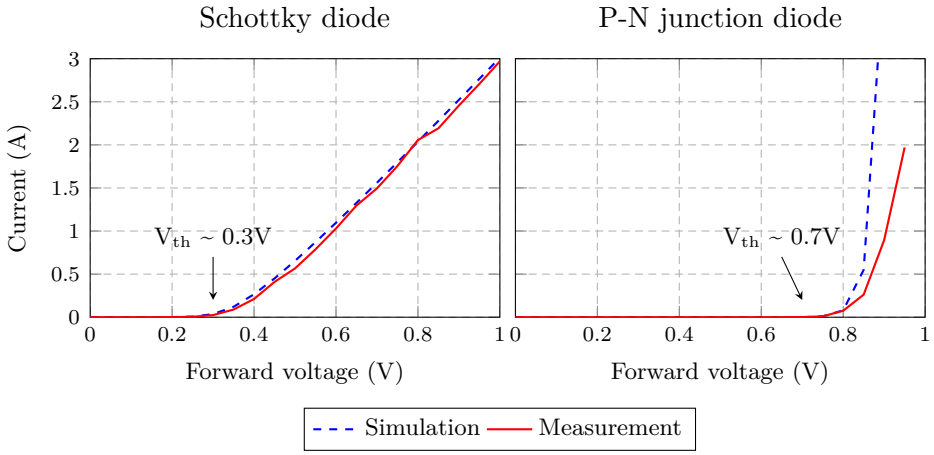


Figure 4.15 – Measured DC characteristic curves for Schottky and P-N junction diodes under typical conditions (25°C).

4.3 IC Prototype Measurement

This section presents measurement results for evaluating the performances of the system under normal operating conditions, by using the voltage-mode and current-mode boards with optimized interconnections. Unfortunately, these boards have been received in late February 2020 due to technical issues. Therefore, only a first set of measurements for a typical use case has been performed in typical conditions in order to validate the driver operating principle.

In a first time, it is proposed to check the electrical transient behavior of the voltage-mode and current-mode drivers when switching the load current. Then, the laser pulse shape is measured, by using the VCSEL module as load, in order to check the electro-optical transient behavior of the drivers. The impact of the clamping diode is quickly investigated. Due to unknown technical issues, it has not been possible to test the version 1 of the voltage-mode driver prototype. It has thus led to test 9 IC prototypes among 10. Performances in terms of power are then measured for each valid IC prototype. At last, results are summarized and discussed.

4.3.1 Driver current waveform

It is proposed to measure the driver current through a resistive load. The validation board is used for that purpose (embedding two 2Ω low inductance resistors connected in parallel). In order to avoid self-heating effects, a short pulse train (~200µs) with a sufficiently long off-time is configured. The ON-state current is set through the I^2C interface. The driver current is measured by sensing the voltage across the resistive load with the active differential probe placed as close as possible to its terminals. The gate width of the

switching element has been configured on its maximum size (86.4mm) to benefit from a low resistance. Results for the voltage-mode and current-mode drivers are detailed hereafter.

4.3.1.1 Voltage-mode driver

First electrical measurements have shown that the voltage-mode driver is able to generate current pulses. Waveforms of interest for a 3A ON-state current at 50MHz under typical conditions (3.6V, 25°C) are illustrated in Figure 4.16. For that case, an average load current of 1.3A for a 2.9A ON-state current value and a 52% duty cycle is reported, while a 1.5A average value was expected (due to the operating principle of the voltage-mode driver, see Equation 2.21). This slight deviation could be explained by the undershoot (~ -2.5A) noticed when the current is cutting off due to the predicted ringing, which is expected since no clamping diode is used here (the prototype V1 is used here, further discussed in Part 4.3.3). However, some disturbances have been noticed as well on the bandgap voltage reference circuit, which were not seen under DC conditions. In that case, a 1.06V average value is reported during the pulse train. This could also explain the current regulation issue. More severe disturbances have been noted at higher frequencies (further discussed in Part 4.3.1.3). A similar overall behavior has been noticed for other IC prototype versions.

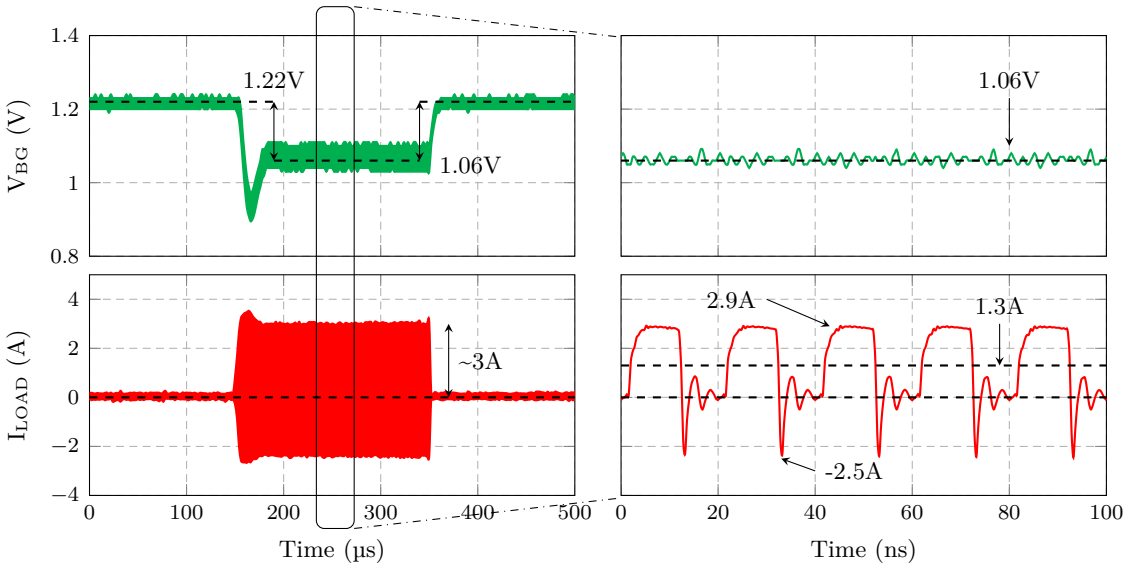


Figure 4.16 – Transient measurement waveforms for the voltage-mode driver (V1) for $I_{ON} = 3A$ at 50MHz under typical conditions (3.6V, 25°C). A zoom is presented on the right. A "peak detect" sampling mode was used for acquiring the waveform with the scope during a relatively long time (500µs, left waveform) while a high resolution mode (real time with averaging) was used for a short time (100ns, right waveform).

4.3.1.2 Current-mode driver

First electrical measurements have shown that the current-mode driver is able to generate current pulses. Waveforms of interest for a 3A ON-state current at 50MHz under typical conditions (3.6V, 25°C) are illustrated in Figure 4.17. In this context, an offset of 0.5A is noticed on the current waveform because the voltage across the resistive load is not quite 0 due to the resistance of the switching element when turning on, thus inducing a residual current through the load. This effect will not occur with the laser diode if the residual voltage is less than the threshold voltage.

As expected, a ripple on the load current is noticed but it leads to a ON-state value oscillating between 2.2A and 2.5A while around 3A was targeted. Although a similar erratic behavior as before has been seen here, the current regulation issue could be explained by interferences noticed on the bandgap voltage, leading to a 0.92V average value. Voltage spikes on the bandgap voltage synchronously to occur with the switching of the power stage, as seen under DC conditions. More severe disturbances have been noted at higher frequencies (further discussed in Part 4.3.1.3). A similar overall behavior has been noticed for other IC prototype versions.

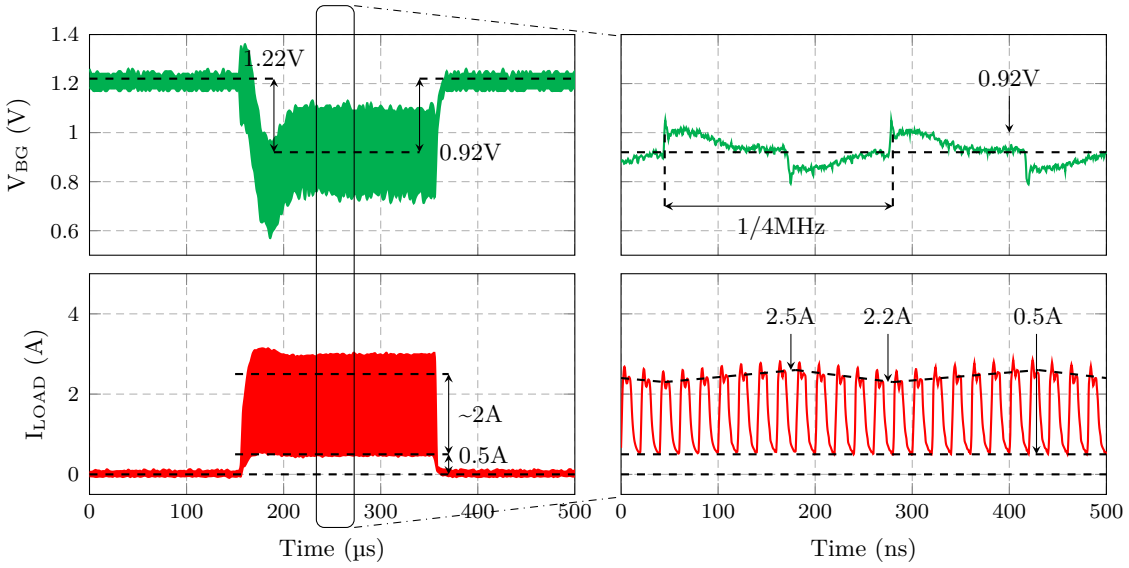


Figure 4.17 – Transient measurement waveforms for the current-mode driver (V3) for $I_{ON} = 3A$ at 50MHz under typical conditions (3.6V, 25°C). A zoom is presented on the right. Same modes as before have been used for acquiring the waveform with the scope.

4.3.1.3 EMI issues

The bandgap voltage reference (1.22V) is disturbed when switching the current for both voltage-mode and current-mode drivers. The interferences could be caused by a coupling between the two major building blocks (DC/DC converter and HFS block) and the bandgap circuit through internal and/or external interconnections. As a reminder, different power supply paths on PCB have been required to properly supply analog, digital and power blocks of the chip in order to minimize the impact of noise between each block. Moreover, the test boards rely on a double sided PCB using 6 layers with a wide common ground plane on layer 3. In fact, it has been noticed that analog and power ground tracks were not merged on layer 3 but rather on layer 4, which could lead to generate a significant noise through analog blocks, such as the bandgap circuit. Solving this technical issue requires a new design of test boards which could not be done here due to short time constraints. It is thus proposed to re-connect the analog ground pin ANGD of the chip to the substrate ground pin GNDS located in the center of the chip by using a thin metallic wire, as illustrated in Figure 4.18. The modification has been realized by an industrial partner.

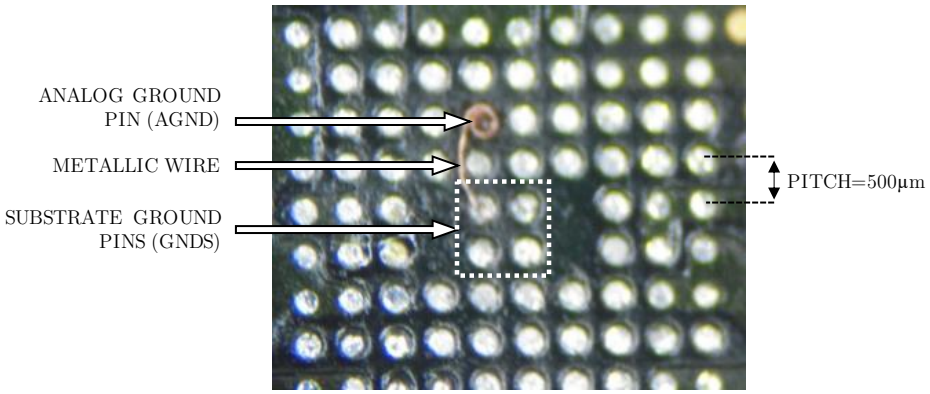


Figure 4.18 – Photograph of the proposed modification at pin level.

The bandgap voltage has been measured for both voltage-mode and current-mode driver for various ON-state current and frequencies. Results are shown in Figure 4.19. A good improvement is noticed for test boards with the modification, confirming that the coupling may come from ground connections. Nevertheless, a slight deviation is still noticed for high currents and frequencies. This indicates that a ground coupling remains and it is likely due to interconnections through the substrate of the chip, metallization, PCB tracks and/or ground plane. This issue could not be solved in the present work. Further investigations need to be pursued.

Despite these disturbances making the current regulation less accurate, the drivers can

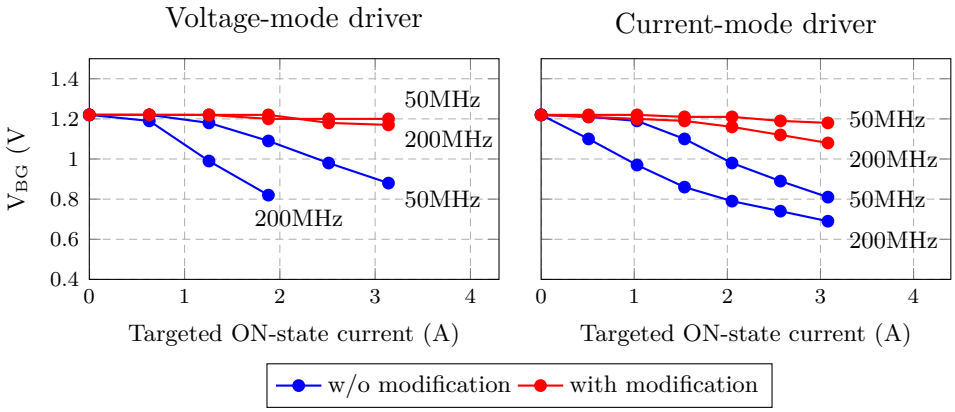


Figure 4.19 – Measured bandgap voltage vs. ON-state current for various frequencies under typical conditions (3.6V, 25°C).

be used with an open-loop control by adjusting the ON-state current through the I^2C interface to reach the desired value.

4.3.2 Laser pulse shape

It is proposed to measure the laser pulse shape by using the VCSEL module. Both the voltage-mode and current-mode boards with optimized interconnections are used for that purpose. In order to avoid self-heating effects, a short pulse train (~200µs) with a sufficiently long off-time is configured. The ON-state current is set through the I^2C interface but no adjustment is made for now, despite EMI issues on the bandgap circuit. Indeed, the purpose here is to check the electro-optical transient behavior of the drivers. The gate width of the switching element has been configured on its maximum size (86.4mm) to benefit from a low resistance. The laser pulse shape is acquired by using the iC-Haus ic212 high-speed photodetector. Results for the voltage-mode and current-mode drivers are detailed hereafter. However, the timing skew between electrical and optical signals could not be corrected due to lack of a de-skewing fixture. Thus, optical and electrical waveforms are not shown in phase.

4.3.2.1 Voltage-mode driver

First optical measurements have shown that the voltage-mode driver is able to generate laser pulses. Waveforms of interest for a 3A ON-state current at 50MHz and 200MHz under typical conditions (3.6V, 25°C) are illustrated in Figure 4.20. A distortion is noticed on the laser pulse shape, particularly for high frequencies. The rising time of the laser pulse is slower than the falling time, as seen for the laser diode current from simulation results (see Part 3.4). This confirms that parasitic elements have an impact on the photo-generated current. In addition, a very short secondary laser pulse occurs when the pulse

is cut off. It might be caused by the strong ringing observed on the switching node voltage V_{SW} where it becomes sufficiently low during a brief moment to re-activate the laser diode. It is however seen during the high-frequency switching only. Voltage spikes around 7.5V are noticed at the switching node suggesting that the clamping diode is less effective than expected (the prototype V2 is used here, further discussed in Part 4.3.3). Furthermore, a 4V anode voltage V_A against a 3.6V input voltage is required, confirming that a buck-boost structure is essential for this kind of voltage-mode driving topology. Slight voltage bounces are however observed on the anode voltage. This is mostly due to ESL of decoupling capacitors. A similar overall behavior has been noticed for other IC prototype versions.

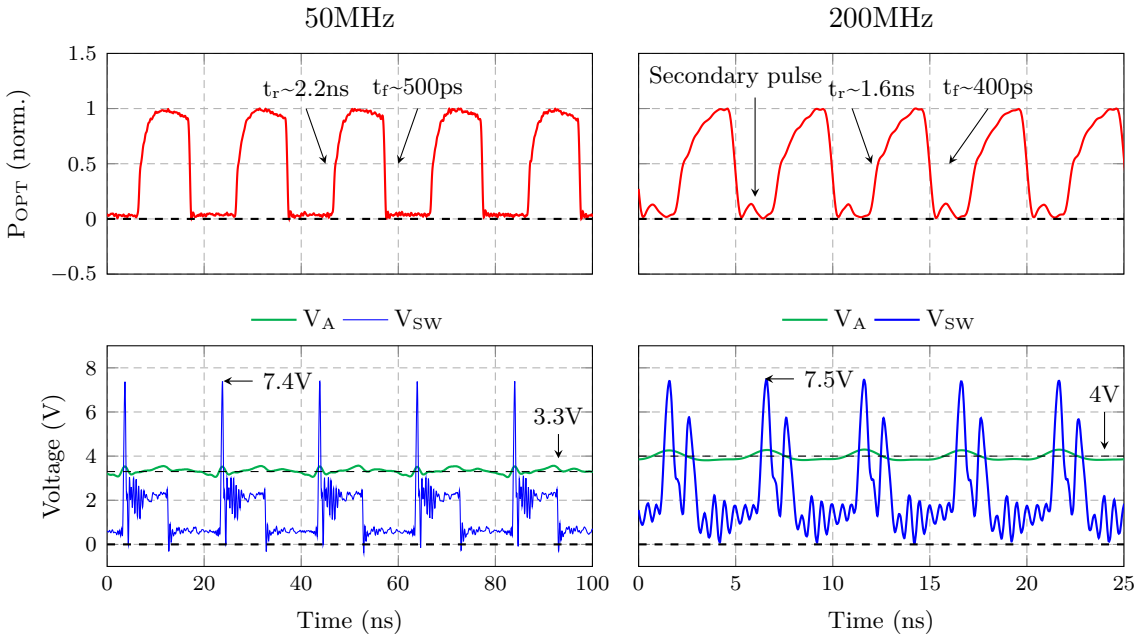


Figure 4.20 – Transient measurement waveforms for the voltage-mode driver (V2) for $I_{ON} = 3A$ at various frequencies under typical conditions (3.6V, 25°C). Laser pulse shape is normalized on y-axis according to its maximum value. Important: electrical and optical waveforms are not in phase (de-skewing issue).

4.3.2.2 Current-mode driver

First optical measurements have shown that the current-mode driver is able to generate laser pulses, despite its erratic behavior at low output currents. Waveforms of interest for a 2A ON-state current at 50MHz and 200MHz under typical conditions (3.6V, 25°C) are illustrated in Figure 4.21. A distortion is noticed on the laser pulse shape, particularly at high frequencies. The falling time of the laser pulse is slower than the rising time, as seen for the laser diode current from simulation results (see Part 3.4). As previously

explained, parasitic elements have an impact on the photo-generated current. In addition, a slight overshoot is noticed on the laser signal when the pulse is turning on. This might be caused by the strong ringing seen on the switching node V_{SW} where a voltage spike around 6V/7V is reported, what suggests that the clamping diode is also less effective than expected (the prototype V2 is used here, further discussed in Part 4.3.3). It is reminded that the clamping voltage is the input voltage here (3.6V).

This effect is however emphasized when no clamping diode is used, such as with the prototype V1 as illustrated in Figure 4.22. The strong overshoot causes a severe distortion on the laser signal for high modulation frequencies where the laser pulse only accounts for this overshoot. This could lead to pulse-to-pulse reliability issues with an increased peak optical power and a reduced pulse width, which is not desired in this context. Using a clamping diode is thus essential here.

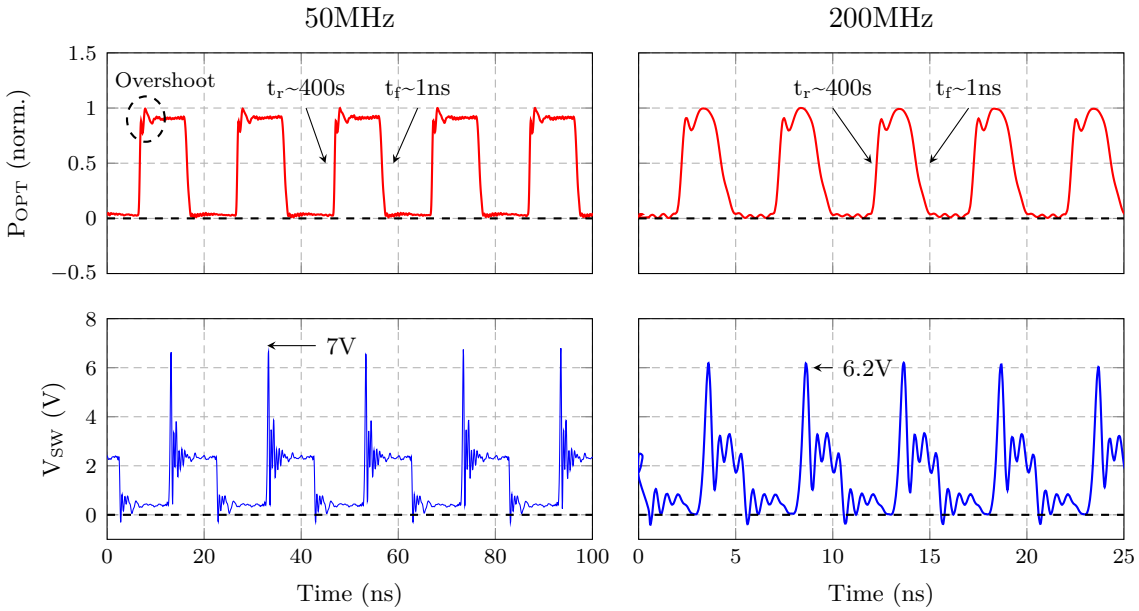


Figure 4.21 – Transient measurement waveforms for the current-mode driver (V2) for $I_{ON} = 2A$ at various frequencies under typical conditions (3.6V, 25°C). Laser pulse shape is normalized on y-axis according to its maximum value. Important: electrical and optical waveforms are not in phase (de-skewing issue).

At last, a ripple has been seen over the laser pulse train, due to the current ripple as expected. A similar overall behavior has been noticed for other IC prototype versions.

4.3.3 Impact of the clamping diode

Several IC prototypes implementing various combinations of devices have been realized for testing, since clamping diode models were incomplete (see Part 3.2.2.5). Usually, a

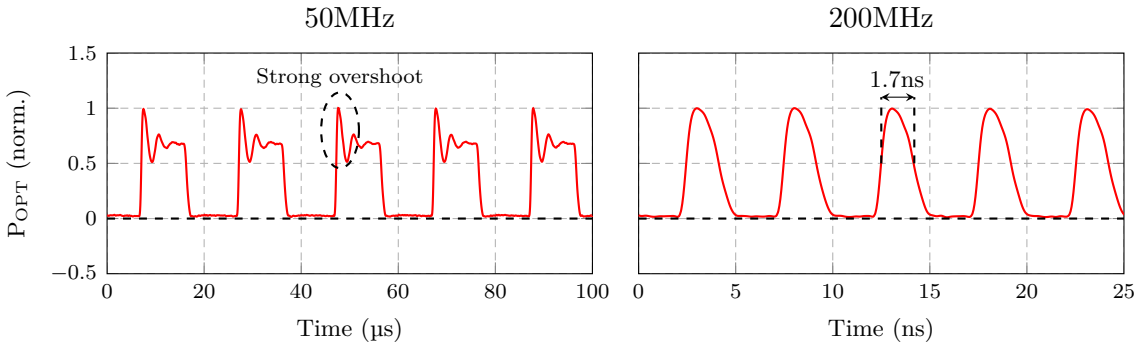


Figure 4.22 – Laser pulse shape for the current-mode driver (V1) for $I_{ON} = 2A$ at various frequencies under typical conditions (3.6V, 25°C). Laser pulse shape is normalized on y-axis according to its maximum value.

Transmission-Line Pulse (TLP) measurement is employed to investigate transient characteristics of semiconductor devices and integrated circuits in the high power time domain, such as ESD events [162][163]. However, it requires a dedicated experimental setup which could not be done here. To distinguish the different prototype versions, it is proposed to evaluate the impact of the clamping diode by measuring the voltage spike (defined as the peak voltage V_{PEAK}) occurring at the switching node under normal operating conditions. To get a fair comparison, same conditions, depending on the driving mode, should be considered. As different cascode devices are implemented as well, all prototype versions cannot be compared between each other: on one hand, versions 1, 4 and 5 could be compared and on the other hand, versions 2 and 3.

4.3.3.1 Voltage-mode driver

The anode voltage is considered as the clamping voltage for the voltage-mode driver. The voltage spike V_{PEAK} is measured here for various modulation frequencies while adjusting the ON-state current in order to define the anode voltage at the same level for each prototype. Due to a short schedule, only one operating point has been considered. Results for a 3V anode voltage under typical conditions (3.6V, 25°C) are illustrated in Figure 4.23. As a reminder, it has not been possible to test version 1 due to unknown technical issues. It is seen that there is no significant difference between versions 2 and 3 on the one hand, and versions 4 and 5 on the other hand. However, the voltage spike seems to be reduced when using a HVDrift 18V (V4 and V5) as cascode device compared to a GO2 device (V2 and V3). This might be explained by a larger equivalent output capacitance (see Part 3.2.2.4) added at the switching node that reduces current transients, thus the voltage spikes. Finally, the clamping diode, either a Schottky or a P-N junction diodes, seems less effective than expected as a peak voltage around 7V is reported for both devices (V2 and V3) at various modulation frequencies (further discussed thereafter). In any case, even

if over voltages above 4.8V are reported, the cascode transistor still ensures a protection for the switching element, as noticed from simulation results (see Part 3.4). Under these conditions, using a GO2 device as a cascode transistor could be satisfying compared to a more specific and bigger HVDrift 18V device.

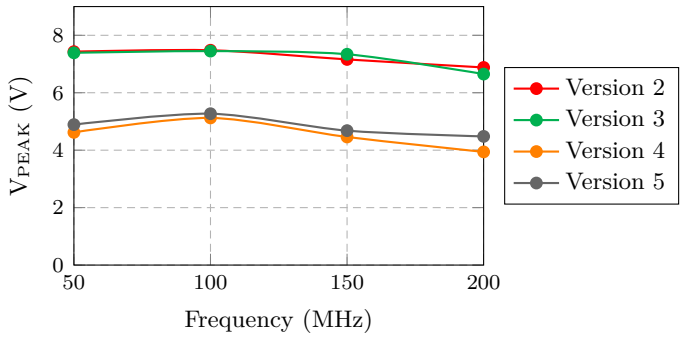


Figure 4.23 – Measured voltage spike vs. modulation frequency for a 3V anode voltage under typical conditions (3.6V, 25°C).

4.3.3.2 Current-mode driver

The input voltage is considered as clamping voltage for the current-mode driver. The voltage spike V_{PEAK} is measured for various ON-state current and modulation frequencies. Results for a 3.6V input voltage under typical conditions (25°C) are illustrated in Figure 4.24. When comparing version 1, 4 and 5, it is seen that using a clamping diode (either Schottky or P-N diodes) may contribute to reduce the voltage spike, particularly for high ON-state currents where a significant spike occurs. There is however no significant difference between versions 2 and 3 on the one hand, and versions 4 and 5 on the other hand. In addition, the voltage spike seems to be reduced when using a HVDrift 18V (V4 and V5) as cascode device compared to a GO2 device (V2 and V3), as for the voltage-mode driver. The clamping diode, either a Schottky or a P-N junction diodes, seems also less effective than expected as a peak voltage around 7V is reported for both devices (V2 and V3) at various modulation frequencies (further discussed thereafter). As for the voltage-mode driver and under these conditions, the cascode transistor still ensures a protection for the switching element and using a GO2 device as cascode transistor could be satisfying compared to a HVDrift 18V device.

4.3.3.3 Summary

Due to the limited experimental setup and measurement results, no distinction can be made between the Schottky and P-N junction diodes. Nonetheless, using a clamping diode seems to have a positive but limited impact on the voltage spike. This issue could

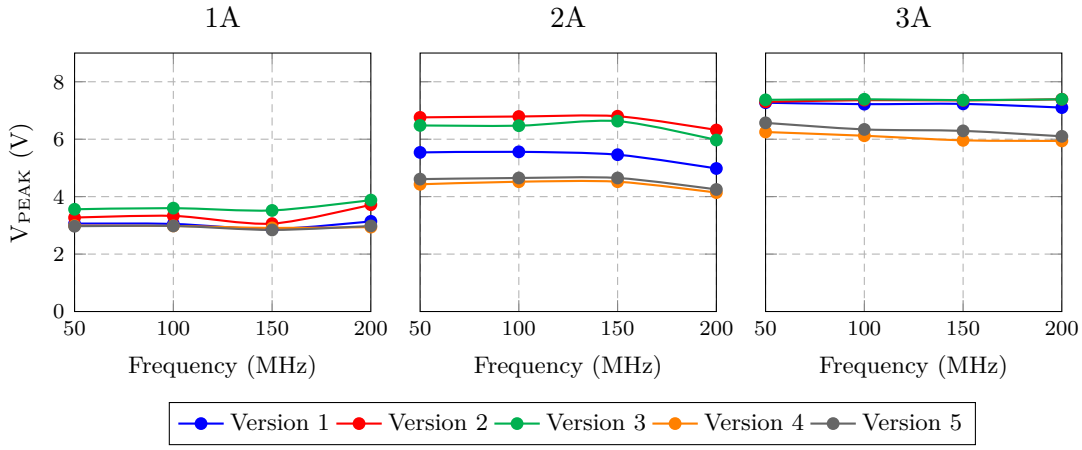


Figure 4.24 – Measured voltage spike vs. modulation frequency for various ON-state currents under typical conditions (3.6V, 25°C).

be explained by the high impedance of parasitics on the clamping diode current path. Indeed, the clamping diode is routed to the HFS block through an extended RDL track that might add some extra parasitic inductances (see Part 3.3.13). A solution could be to place the clamping diode closer to the switching node in order to reduce the metallization, but it seems quite complicated with respect to the high number of features included within the HFS block. Adding a snubber in parallel to the clamping diode could be interesting as well in order to create an additional current path. These options however requires a full re-design of the chip, which could not be done here. At last, this issue could not be solved in the present work. Further investigations need to be pursued, such as investigating the ESD protections of the chip (see Part 3.2.6).

4.3.4 Power measurement

It is proposed to perform a first set of measurement in terms of power metrics by using the VCSEL module under typical conditions. Both the voltage-mode and current-mode boards with optimized interconnections are used for that purpose. In order to avoid self-heating effects, a short pulse train (~500µs) with a sufficiently long off-time (99.5ms) is configured. Power measurements have been carried out while targeting a peak optical power of 2.5W as required from general specifications (see Part 2.1.2). For that purpose and because the current regulation may be disturbed due to EMI issues on the bandgap circuit, the ON-state current value, set through the I^2C interface, was swept until reaching the desired peak optical power. The pulse width of the external differential modulation signal has been finely tuned as well to face a potential laser signal distortion. A 50% modulation duty cycle on the laser pulse shape was targeted. Due to the different equipment to be used for performing transient and power measurements, this kind of tuning procedure was very

tedious and time consuming. Results for the voltage-mode and current-mode drivers are detailed thereafter. In addition, it is specified that the gate width of the switching element has been properly configured to minimize total losses. The characterization procedure is described hereafter for both GO2 and HVDrift 18V cascode devices.

4.3.4.1 Optimum gate width characterization

In this context, total losses accounts for conduction losses through both the switching element and the cascode device and switching losses due to the switching of the equivalent input capacitance of the switching element, the cascode device and the gate driver. Due to the limited experimental setup, conduction losses have been directly estimated by using Equation 2.37 with the measured total on-resistance of the switching element and cascode device (see Part 4.2.2.1) and assuming a perfect square wave. Switching losses have been estimated by measuring the product of the average current drawn by the HFS block power supply ($V_{IN,HFS}$ pin) with the input voltage assumed to be constant. Total losses for each device have been estimated over a pulse train while sweeping the gate width of the switching element for a 3A ON-state current and various modulation frequencies (50MHz and 200MHz) under typical conditions (3.6V, 25°C). Results are shown in Figure 4.25.

As expected, total losses corresponding to the HVDrift 18V cascode device are slightly higher than the ones of the GO2 device, due to the relatively higher on-resistance. Nonetheless, the optimum width seems to be quite similar for both devices. For a 50MHz modulation frequency, the optimum width can be found in a wide range from 40mm to 80mm, showing that conduction losses are predominant over switching losses. For a 200MHz modulation frequency, the optimum width is found in a smaller range. A 27mm and 54mm gate widths have been retained for the (3A, 50MHz) and (3A, 200MHz) use cases respectively. The total dissipated power through the HFS block depending on the cascode device is summarized in Table 4.1.

Table 4.1 – Optimum width and total dissipated power through the HFS block depending on the cascode device for various use cases.

Use case	**W_{OPT} (mm)**	**$P_{TOT(MIN)}$ (W)**	
		GO2	HVDrift 18V
(3A, 50MHz)	27	0.95	1.05
(3A, 200MHz)	54	1.5	1.6

4.3.4.2 Voltage-mode driver

Once the optimum gate width selected for each use case, power measurements targeting a peak optical power of 2.5W have been performed while following experimental considerations (see Part 4.1.2). Results for each version of the voltage-mode driver prototype

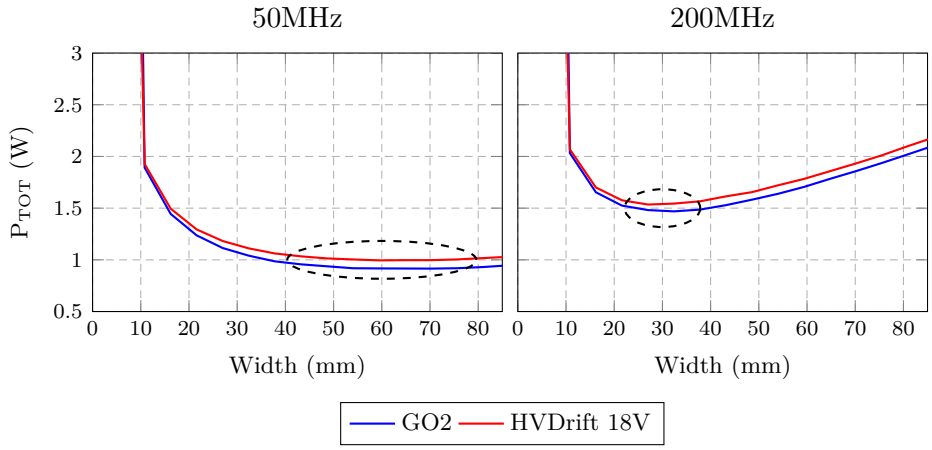


Figure 4.25 – Total losses, corresponding to the GO2 or HVDrift 18V cascode devices, estimated for a 3A ON-state current and various modulation frequencies (50MHz and 200MHz) under typical conditions (3.6V, 25°C).

are summarized in Table 4.2. As a reminder, it has not been possible to test the version 1 due to unknown technical issues. For other versions, measurement results are quite homogeneous where an electrical efficiency around 70% is reported at 50MHz and around 62% at 200MHz, which is in relatively good agreement with simulation results although the current waveform was more impacted by parasitic inductances (see Part 3.4). In the same way, an electro-optical efficiency around 20% and 17% is reported at 50MHz and 200MHz respectively.

Table 4.2 – Measurement results for the voltage-mode driver for $P_{OPT(PEAK)}$ at 50MHz and 200MHz under typical conditions (3.6V, 25°C).

Parameter	**Value**							
Frequency	50MHz				200MHz			
Version	V2	V3	V4	V5	V2	V3	V4	V5
$P_{OPT(PEAK)}$	2.49W	2.52W	2.51W	2.53W	2.44W	2.47W	2.50W	2.52W
I_{ON} (estimation)	3.07A	3.10A	3.09A	3.11A	3.01A	3.05A	3.08A	3.10A
V_A	3.33V	3.35V	3.31V	3.35V	3.99A	4.06A	4.06A	4.13A
P_{OUT} (estimation)	4.44W	4.46W	4.49W	4.46W	4.44W	4.50W	4.44W	4.44W
P_{IN}	6.21W	6.28W	6.19W	6.16W	7.06W	7.71W	6.77W	7.34W
η_{OPT}	20%	19.9%	20.3%	20.3%	17.6%	16.3%	18.4%	16.9%
η_{ELEC} (estimation)	71%	71%	72%	73%	63%	58%	66%	60%

The slight difference between these two use cases is caused by an increase in losses through

major blocks of the driver, such as the DC/DC converter (including off-chip components) and the HFS block (accounting for conduction and switching losses) as expected. The breakdown of losses for each prototype version is presented in Figure 4.26. Losses have been evaluated by using figures in Tables 4.2 and 4.1. From these results, it is clearly seen that the driver is less efficient at high frequency. Moreover, prototype versions implementing a Schottky diode as clamping diode (V2 and V4) seem to be a little bit less power consuming at 200MHz than versions implementing a P-N junction diode (V3 and V5). However, no trend can be identified between the two types of cascode devices in terms of power metrics for the voltage-mode driver.

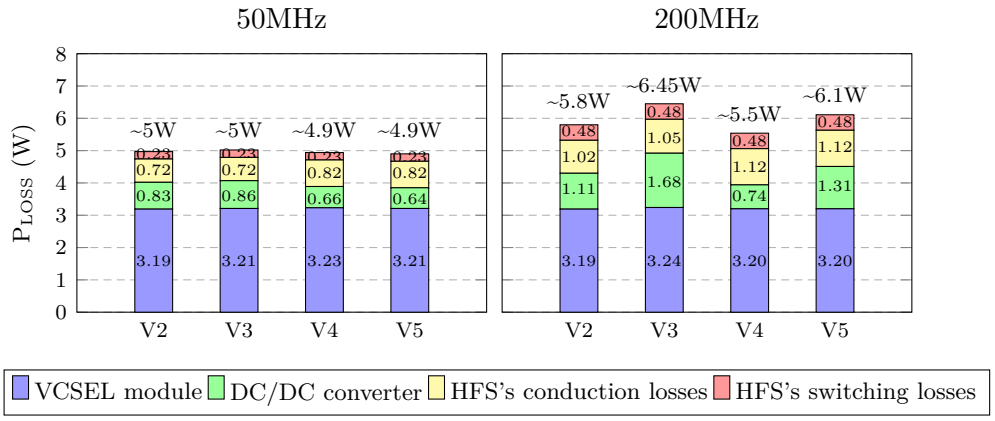


Figure 4.26 – Breakdown of losses for each prototype version of the voltage-mode driver for $P_{OPT(PEAK)}$=2.5W at various modulation frequencies under typical conditions (3.6V, 25°C). Total losses are indicated above each bar.

4.3.4.3 Current-mode driver

As before, once the optimum gate width was selected for each use case, power measurements targeting a peak optical power of 2.5W have been performed. Results for each version of the current-mode driver prototype are summarized in Table 4.3. It has not been possible to test the version 1 at 200MHz due to the severe distortion noticed on the laser pulse shape making impossible to reach a 50% modulation duty cycle. For other versions, results are quite homogeneous where an electrical efficiency around 66% is reported at 50MHz and around 59% at 200MHz, which is in relatively good agreement with simulation results although the current waveform was more impacted by parasitic inductances (see Part 3.4). In the same way, an electro-optical efficiency around 18% and 16% is reported at 50MHz and 200MHz respectively.

As for the voltage-mode driver, the slight difference between these two use-cases is caused by an increase in losses through the DC/DC converter and the HFS block, where the

Table 4.3 – Measurement results for the current-mode driver for $P_{OPT(PEAK)}$ at 50MHz and 200MHz under typical conditions (3.6V, 25°C).

Parameter	**Value**								
Frequency	50MHz					200MHz			
Version	V1	V2	V3	V4	V5	V2	V3	V4	V5
$P_{OPT(PEAK)}$	2.49W	2.51W	2.53W	2.45W	2.48W	2.47W	2.51W	2.48W	2.50W
I_{ON} (estimation)	3.07A	3.09A	3.11A	3.02A	3.05A	3.04A	3.09A	3.06A	3.08A
P_{OUT} (estimation)	4.50W	4.48W	4.48W	4.51W	4.47W	4.41W	4.49W	4.43W	4.45W
P_{IN}	6.84W	6.92W	6.74W	6.95W	6.63W	7.62W	7.25W	7.91W	7.39W
η_{OPT}	18.4%	18.1%	18.6%	18.2%	18.9%	16.2%	17.3%	15.7%	16.9%
η_{ELEC} (estimation)	66%	65%	67%	65%	67%	58%	62%	56%	60%

current-mode driver is also less efficient at high frequencies. The breakdown of losses, evaluated from previous figures, for each prototype version is presented in Figure 4.27. Nevertheless, prototype versions implementing a P-N junction diode as a clamping diode (V3 and V5) seem to be a little bit less power consuming at 200MHz than versions implementing a Schottky diode (V2 and V4). In addition, no trend can be identified between the two types of cascode devices in terms of power metrics for the current-mode driver.

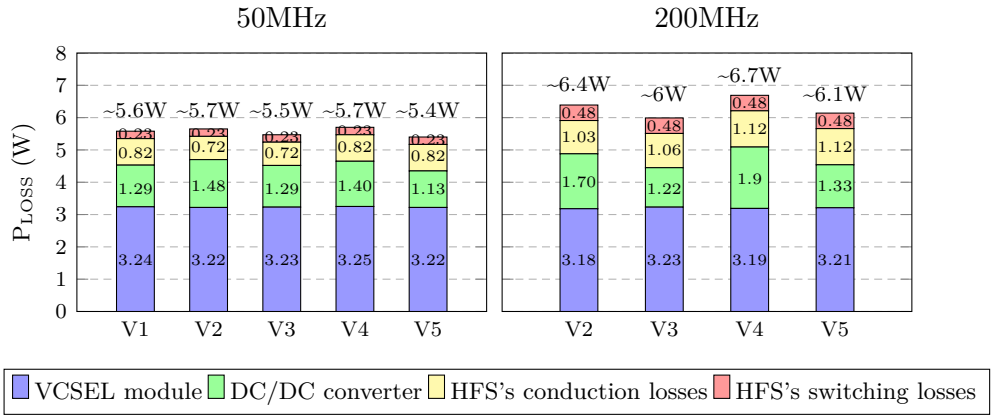


Figure 4.27 – Breakdown of losses for each prototype version of the current-mode driver for $P_{OPT(PEAK)}$=2.5W at various modulation frequencies under typical conditions (3.6V, 25°C). Total losses are indicated above each bar.

4.3.4.4 Comparative analysis

Major results in terms of power efficiency for each driver prototype version have been summarized under bar graphs for easy readability, as shown in Figure 4.28. As a reminder,

the same peak optical power was targeted for both drivers and measurement conditions were assumed to be similar. The voltage-mode driver seems to be more efficient than the current-mode driver whatever is the prototype version for a modulation frequency at 50MHz. Results should be however considered with caution since they are mostly based on rough estimations due to the limited experimental setup. In addition, they are quite heterogeneous for a 200MHz frequency. It is seen that the voltage-mode driver seems to be more efficient than the current-mode driver when implementing a Schottky diode as clamping diode (V2 and V4). On the contrary, the current-mode driver has a better power efficiency than the voltage-mode driver but only when implementing a P-N junction diode as well as a GO2 device as cascode device (V3). No distinction is made for the prototype version 5. As a consequence, no strict conclusion can be drawn based on these measurement results.

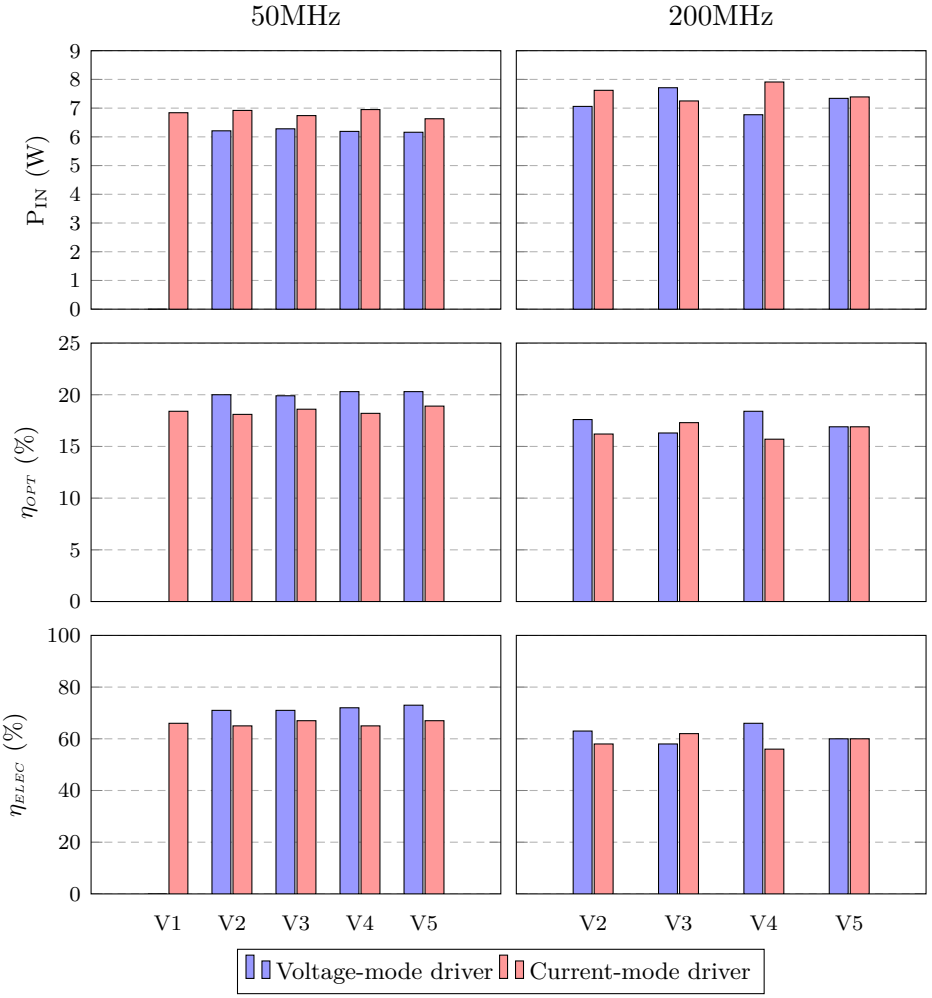


Figure 4.28 – Comparison of each driver IC prototype version in terms of power efficiency for $P_{OPT(PEAK)}$=2.5W at various modulation frequencies under typical conditions (3.6V, 25°C).

4.4 Discussion

Optical and electrical measurements have shown that both the voltage-mode and current-mode drivers are capable of generating laser pulses up to 2.5W with a 2.5ns pulse width at 200MHz under a 3.6V input voltage. Under these conditions, a relatively high power efficiency is reported for both drivers, roughly around 60%. Unfortunately it may not be compared to the state-of-art as efficiency values are rarely mentioned and the application is different in context. Nevertheless, an erratic behavior has been seen for the current-mode driver under DC conditions. EMI issues have been noticed for both drivers impacting the bandgap voltage reference circuit under pulsing conditions. This has thus led to operate the drivers with an open-loop control. Transient results have shown that using a clamping diode in the context of high-frequency switching has an impact for limiting voltage spikes due to parasitic inductances, but no significant distinction has been made between the Schottky and P-N junction diodes. Under these measurement conditions, it has been seen that using a GO2 device as a cascode device was satisfying compared to a more specific and bigger HVDrift 18V device since voltage spikes below 8V have been reported. Furthermore, no significant difference has been noticed in terms of power metrics when comparing the two configurations.

Due to some technical issues and time constraints related to the industrial context, only a first set of transient and power measurements for two typical use cases (2.5W at 50MHz and 200MHz) has been performed under typical conditions (3.6V, 25°C). These results rely on rough estimations due to the limited experimental setup and lacking data about the VCSEL module. Therefore, they must be considered with caution. Even if this set of measurements can prove that the voltage-mode driver using a series configuration and the current-mode driver using a shunt configuration are able to generate laser pulses, it does not fully demonstrate the feasibility of integrating the driver architecture on a single chip taking into account mobile phone constraints (voltage and temperature variations, high integration including digital, analog and power functions). Nevertheless, the characterization of various functionalities under DC and pulsing conditions has highlighted some important issues and which causes are not clearly identified yet. Further investigations are required that call for additional PCBs and a second set of IC prototypes.

Conclusion

This chapter has presented first electrical and optical measurement results obtained on different prototype versions of the voltage-mode and current-mode drivers. Major issues related to the acquisition of optical and electrical signals at such power and speed levels were addressed to build an experimental setup. However, some limitations have been noticed leading to estimate some performances more than measure them. Anyway, whereas good transient performances as well as a relatively high power efficiency have been reported for both voltage-mode and current-mode drivers for a typical use case, they cannot be

compared to the state-of-art circuits as efficiency values are rarely mentioned and the application is different in context. At last, some features such as the pre-bias current source, the configurable driving capability of the gate driver or the gate width selection of the switching element have not or little been investigated. Validating both IC prototypes at system level by considering a typical Time-of-Flight application is also essential in order to demonstrate optical performances of the two different driving topologies.

General Conclusion

The thesis focused on the study and design of a compact, cost-effective and efficient laser diode driver for 3D-depth sensing applications used in mobile phones. The major objective was to validate an integrated architecture for the laser diode driver capable of generating short current pulses of few Amps with a 2.5ns pulse width up to a 200MHz pulse repetition frequency while considering the power efficiency as a leading requirement.

Summary

The start-of-the-art review of laser diode drivers dedicated to ToF applications, presented in Chapter 1, has allowed to identify three relevant topologies, based on a voltage and current driving mode and using a series or shunt configuration. Chapter 2 has detailed a preliminary design study in order to evaluate the feasibility of these three solutions with respect to the targeted objectives using a 130nm CMOS technology from STMicroelectronics. Power management considerations were addressed to build realistic solutions. Pros and cons of each solution regarding various indicators have been discussed using a qualitative analysis to find the most suitable architecture. Due to a lack of simulation results on the optical behavior of the proposed solutions, it was decided to implement the two solutions featuring good estimations in terms of power efficiency in order to be validated experimentally. Key contributions of the work are:

- The layout in a previous IC comprising DC/DC converters has been reused to save time and design resources. In this way, only a single chip was considered.
- An HFS block for providing the high-frequency current switching has been designed. It is shared by both drivers.
- Protection circuits, such as a clamping diode and a cascode structure, were required to prevent any damage due to potential high voltage spikes occurring during fast transients.
- A proper layout of the chip has been realized taking into account a strong isolation of devices and building blocks to minimize the substrate coupling and susceptibility to latch-up.

- Other features, such as a pre-bias current source, have been embedded on chip for testing.
- Due to a lack of simulation models for the clamping diodes, 10 IC prototypes implementing various combinations of devices were realized for testing.
- Several test boards for debugging and measurement purposes, as well as an experimental setup were developed. Major concerns here were to perform electrical and optical measurements at nominal power and speed levels while accommodating eye-safety standards. Some limitations have led to make estimations on some metrics. Another issue was about the small PCB area required by the chip, VCSEL module and off-chip passive components to limit parasitic elements while facing physical constraints related to the optical equipment.
- Optical and electrical measurements have shown that both the voltage-mode and current-mode drivers were capable of generating laser pulses up to 2.5W with a 2.5ns pulse width at 200MHz under a 3.6V input voltage with an open-loop control. Under these conditions, a relatively high power efficiency is reported for both drivers, roughly around 60%.
- Transient measurement results have shown that using a clamping diode in this context has an impact for limiting voltage spikes due to parasitic inductances. However, no significant distinction has been made between the Schottky and P-N junction diodes.

Due to technical issues and time constraints related to the industrial context, only a first set of measurements for two typical operating points has been delivered. Whereas it can prove that the voltage-mode and current-mode drivers are able to generate laser pulses, it does not fully demonstrate the feasibility of integrating the driver architecture on a single chip taking into account mobile phone constraints. Some important issues, such as the limited impact of clamping diodes or interferences on the bandgap voltage reference circuit, have been highlighted as well but which causes are not clearly identified yet. In addition, some features such as the pre-bias current source, the configurable driving capability of the gate driver or the gate width selection of the switching element has not or little been investigated. As a consequence, further investigations must be pursued.

Future Works

Major concerns must be addressed for future works such as investigating issues and performing more measurements while sweeping a wide range of parameters (PRF, peak optical power, input voltage, temperature) to get exhaustive results. The experimental setup should be consolidated to ease the measurement procedure and improve accuracy. Validating the IC prototypes at system level by considering a typical Time-of-Flight application

is also essential in order to demonstrate optical performances of the two different driving topologies. In this way, it would allow to get a relevant comparison and to draw a conclusion on what topology suits the best the iToF application.

For that purpose, it is proposed to follow a methodology based on the re-design of two distinct integrated circuits implementing the voltage-mode driver and current-mode driver separately. Indeed, the approach adopted in the work has led to realize a single chip for implementing both drivers. It thus includes a huge number of building blocks (two DC/DC converters, a shared HFS block with a lot of features, sensitive analog blocks, a I^2C interface with a register bank). Although a special care has been taken at circuit and system levels to make it sure that only one driver works at a time, there is still a risk to face interferences. Identifying causes of issues can then lead to be more tricky. It could be asked if the time and resources saving obtained by using this design approach (a single chip for two drivers) would not be lost by inducing more time consuming investigations, thus delaying the global project (a kind of rebound effect).

Therefore, a more conventional design approach by implementing a single driver architecture with a reduced number of features could be adopted in order to ease the debugging, measurement and validation procedures. Then, improvements and new features could be considered by developing a second IC prototype, and so on. This kind of iterative method should allow to build a robust laser diode driver based on solid foundations.

A Last Word

As presented in General Introduction, 3D image sensors are key enablers for unlocking emerging applications in 3D imaging and computer vision field. Among others, the facial recognition has known a growing interest in smartphone industry and security systems these recent years. Although it could be used for preventing fraud and improving identity authentication for various facilities and devices for instance, improper usages exist as well, such as mass surveillance. In that case, who is responsible? The designer or the end user? Same logic could applied to a wide brand of topics. This is let as an open-ended question to the reader.

In the end, the author invites to review the role of the engineer and scientific researcher by fully re-considering environmental, social and ethical requirements in the development of a concept, a product or a service. A compromise exists, it just needs time to find it.

A Range Measuring Techniques

This appendix reviews various techniques for contactless range measurement mainly focused on light waves-based methods such as the triangulation, interferometry and ToF principles. A more detailed description of the iToF principle is covered as it is used for developing the 3D image sensor under STMicroelectronics' approach. Context and general requirements are described in General Introduction. A basic iToF sensor model is also proposed.

First of all, contactless range measurements can be performed using light (usually infrared light: $\lambda = 0.8 - 3\mu m$), radio (usually microwaves: $\lambda = 3 - 30mm$) or sound (usually ultrasonic waves: $\lambda = 0.1 - 1mm$) waves in a passive or active way. Passive method is a non-invasive technique that consists in sensing waves coming from the surrounding area in order to deduce depth information. On the contrary, active method consists in acting on the surrounding area by emitting waves for providing a true depth measurement. Since no emitter is required for passive methods, it could simplify the system design thus reducing cost. However, it cannot be employed in featureless areas such as planar surfaces limiting its use to specific applications [28].

For developing the 3D image sensor, light waves are well suited in contrast with radio and sound waves mainly due to diffraction effects [27][29]. This phenomenon occurs when a wave encounters an obstacle or aperture with dimensions close to its wavelength, causing the wave to diffuse in all directions from this obstacle or aperture. It thereby limits the spatial resolution of the sensor which is the ability to distinguish details of an object from the scene. In the case of a circular aperture, the Rayleigh criterion defines the smallest distance Δr for which two points of an object can be distinguished on a sensor, as given by

$$\Delta r \simeq 1.22 \frac{\lambda}{D} z \tag{A.1}$$

where λ is the wavelength, D is the aperture diameter and z is the distance between the object and the sensor [164][29]. It can be noticed that for a given distance, short wavelengths or large aperture diameters are required for providing high resolutions. Choosing short wavelengths such as light waves is more relevant in the context of developing a compact system.

Contactless range measuring techniques based on light waves can be classified in three groups: triangulation, interferometry and Time-of-Flight, as illustrated in Figure A.1. They are distinguished according to the relation between the depth and depth resolution (further discussed below). The scope of this appendix is limited to a quick review of triangulation and interferometry techniques and a more detailed description of Time-of-Flight principles. The classification and techniques are well detailed in the literature [21][22][27][28][33][29].

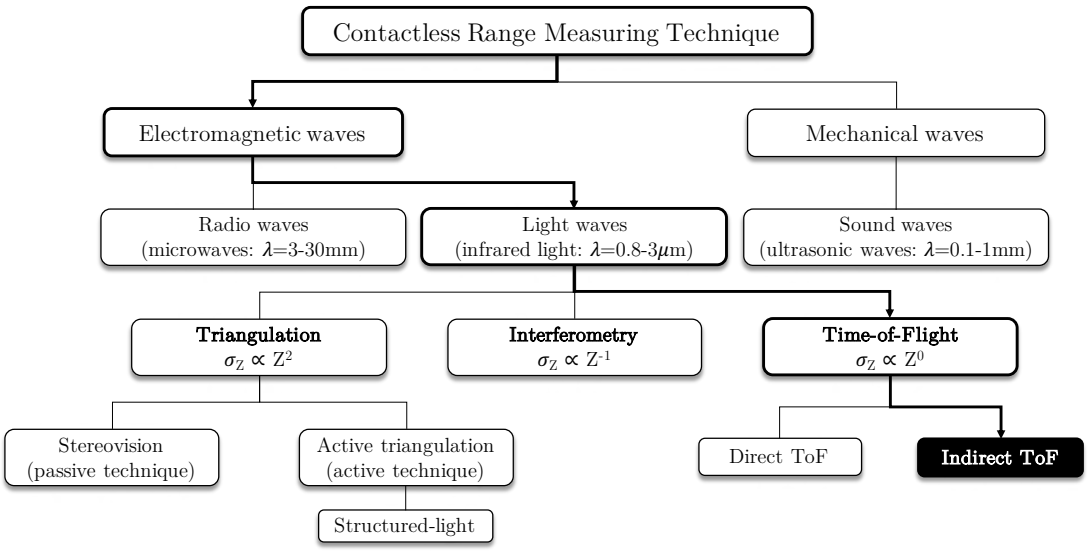


Figure A.1 – Classification of contactless range measuring techniques with a focus on major light wave-based methods. The indirect Time-of-Flight principle is the context of the present work.

A.1 Triangulation

Triangulation is based on geometrical calculations performed on a given configuration between the sensing system and a point of an object from the scene. It exists two major methods: passive triangulation and active triangulation.

A.1.1 Passive triangulation

An example of passive triangulation is the stereovision related to the binocular vision principle (called stereopsis). The depth calculation is realized using two sensors viewing an object from different angles as illustrated in Figure A.2. The depth z (the distance between the object and the two sensors) is given by

$$z = \frac{x}{\frac{1}{\tan\alpha} + \frac{1}{\tan\beta}} \tag{A.2}$$

where x is the triangulation base (the distance between sensors), α and β are the viewing angles of sensors.

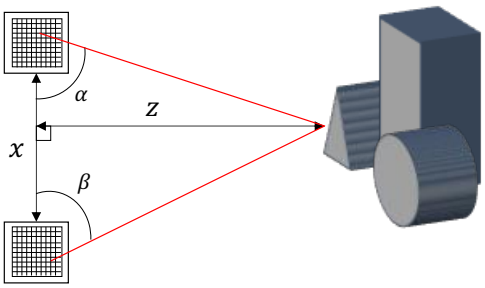


Figure A.2 – Simplified schematic of sterevision principle.

Passive triangulation can benefit from standard 2D image sensors featuring high resolution. Specific lighting conditions are however necessary for preventing shadowing effects and finding correspondences between images from both sensors. Moreover, an important computational effort is required for post-processing data to get a depth map what is not suitable for real-time applications [27].

A.1.2 Active triangulation

Active triangulation allows to reduce the need for specific lighting conditions by using an active illumination, such as a laser beam. The depth z is calculated from the triangle formed by a point of an object, the sensor (through optical elements such as lens) and the optical emitter, as illustrated in Figure A.3. The depth is given by

$$z = f\frac{x}{p} \tag{A.3}$$

where f is the focal length of sensor lens, x is the distance between the sensor and the optical emitter and p is the position of the beam on the sensor. The depth resolution, related to the standard deviation of depth [165], is defined as:

$$\sigma_z = \sqrt{\left(\frac{\partial z}{\partial p}\right)^2 \sigma_p^2} = \frac{z^2}{fx}\sigma_p \propto z^2 \tag{A.4}$$

according to the error propagation formula [166].

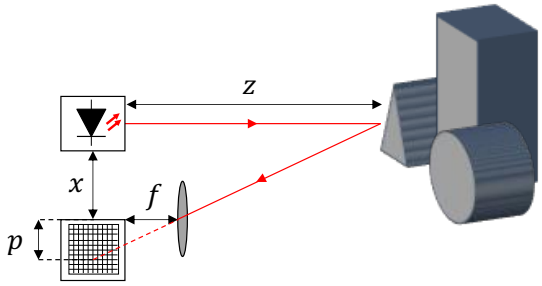


Figure A.3 – Simplified schematic of active triangulation principle.

It can be seen that depth resolution is determined by lateral resolution σ_p of the sensor which is limited by the pixel pitch [29]. As for passive triangulation, active triangulation can benefit from standard 2D image sensors with a high resolution. Moreover, the depth resolution can be improved by increasing the distance between the sensor and the optical emitter but leading to a bulkier system. The depth resolution is also proportional to z^2 making the active triangulation suitable for depth measurement up to few meters. For long ranges, depth resolution tends to get too coarse [28].

In addition, a scanning mechanism such as mirrors can be employed in order to reconstruct a depth map by measuring distance from all points of the object, but at the expense of the system cost and size. An alternative solution is to illuminate the scene with a specific 2D pattern what is called structured light. Depth calculations rely on a similar principle but using deformations of the pattern projected on the object. Nevertheless, it involves a high computational effort reducing the acquisition speed [29]. Shadowing effects can still occur causing a complete depth map difficult to obtain.

A.2 Interferometry

Interferometry relies on the evaluation of an interference pattern resulted from the interaction of two monochromatic light waves coming from the same source. An example of realization is based on the Michelson interferometer as depicted in Figure A.4. An incident light beam from an optical emitter is split in two parts propagating in orthogonal directions by using a beam splitter. One beam is reflected by a mirror located at a reference distance z_{REF} while the other beam is reflected by the object located at an unknown distance z, which is the depth. Both beams are then superimposed at the beam splitter and guided to a sensor. The length difference $z_{REF} - z$ traveled by beams involves a phase difference of the waves resulting in an interference pattern on the sensor. The light intensity I of the pattern depends on the length difference $z_{REF} - z$ and can be expressed

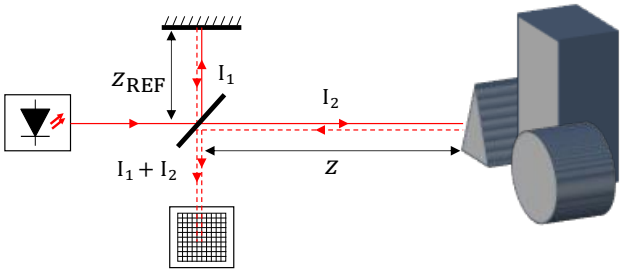


Figure A.4 – Simplified schematic of the Michelson interferometer.

in terms of the individual waves intensities as follows:

$$I = I_1 + I_2 + 2\sqrt{I_1 I_2}\cos\left(\frac{4\pi(z_{REF} - z)}{\lambda}\right) \tag{A.5}$$

where I_1 and I_2 are the intensities of individual waves and λ is the wavelength of the incident wave [29]. The depth z is then evaluated by adjusting the reference distance z_{REF} in order to form constructive or destructive interferences. Indeed, the light intensity I reaches a maximum or a minimum (constructive or destructive interferences respectively) when $z_{REF} - z$ is a multiple of $\frac{\lambda}{2}$ or $\frac{\lambda}{4}$ respectively. The depth resolution can be derived for smooth surfaces (roughness much smaller than $\frac{\lambda}{4}$ [167]) as follows:

$$\sigma_z \propto z^{-1} \tag{A.6}$$

This technique provides a high accuracy but it is limited to extremely short ranges (typically z<1µm) [28]. Furthermore, it requires high precision optics and mechanics not suitable for a compact and cost-effective system.

A.3 Time-of-Flight

A.3.1 Operating principle and optical power considerations

The Time-of-Flight principle is based on the measurement of time elapsed between the emission of a light wave and its detection by a sensor after reflection on an object from the scene, as illustrated in Figure A.5. The depth z is then calculated knowing the speed of light, as follows

$$z = \frac{c}{2}\Delta t \tag{A.7}$$

where c is the speed of light ($\simeq 3.10^8$ m/s) and Δt is the elapsed time or so-called Time-of-Flight. However, the optical emitter must be located as close as possible to the sensor in a coaxial configuration for considering that the distances between the optical emitter to the object and the sensor to the object are the same ($\simeq z$). In this way, the ToF principle

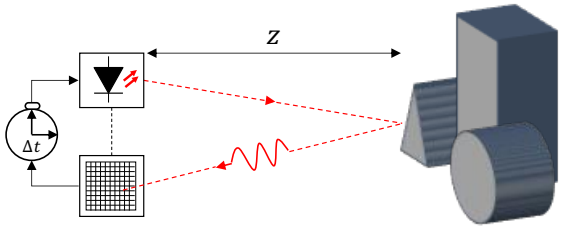


Figure A.5 – Simplified schematic of ToF principle.

is well suited for compact systems. In addition, correspondence or shadowing effects are not a concern [29].

The depth resolution, related to the standard deviation of depth, is defined as:

$$\sigma_z = \frac{c}{2}\sigma_t \tag{A.8}$$

It can be seen that the depth resolution depends on the time measurement accuracy σ_t, which theoretically leads to a distance-independent resolution (proportional to z^0). It thus provides the ability to measure depth from few cm up to tens of km [21]. But practically, the ToF Δt is acquired when a certain amount of light is detected by the sensor what depends on the optical system (lens, filter for instance), lighting conditions, object reflectivity and distance between sensor and object. This amount of light can be expressed in terms of the optical power (or radiant flux) received on the photosensitive area of a pixel Φ_{PIX} and previous parameters, which is given by:

$$\Phi_{PIX} \simeq \frac{\tau_{OPT}.\rho.\mathrm{FF}.A_{PIX}}{4F_{\#}^2}\left(\frac{\Phi_{SOURCE}}{(2z\tan\alpha)^2} + E_{BKG}\right) \tag{A.9}$$

where τ_{OPT} is the transmission coefficient of optical system, $F_{\#}$ is the f-number of optical system, ρ is the object reflectivity, FF is the pixel fill factor, $\mathrm{A_{PIX}}$ is the pixel area, α is the divergence half-angle of light source (considered as a point source), Φ_{SOURCE} is the optical power (or radiant flux) emitted by the light source and $\mathrm{E_{BKG}}$ is the irradiance of background light. The object surface has been considered as a Lambert reflector for simplification. More details about this optical power budget can be found in [27][33]. It can be noticed that the optical power received by a pixel Φ_{PIX} is inversely proportional to z^2 resulting in a depth resolution which is distance dependent [29].

From equation A.9, the influence of the background light level leads to emit a high optical power in order to detect a certain amount of light. This emitted optical power is however limited by eye-safety standards in order to avoid hazards for skin and eyes [39]. Restrictions also depends on the wavelength range of the optical signal. Practically, infrared wavelengths are employed not to disturb users as they are invisible for the naked eye.

Three major wavelengths are employed for ToF systems: 905nm is usually dedicated to automotive applications as it is not impacted by rain, smoke, smog or other atmospheric conditions while 850nm and 940nm are preferred in consumer electronics [168][169]. Both 850nm and 940nm wavelengths have benefits and drawbacks with respect to solar irradiance, quantum efficiency and eye-safety standards. Pros and cons are summarized in Table A.1. In this context, the 940nm wavelength, totally invisible, has been preferred over the 850nm wavelength as the background illumination level is lower [38], eye-safety standards are less restrictive and the silicon is still sufficiently sensitive [27][168]. In addition, an optical element such as a filter can be associated to the sensor in order to filter all the light except for the wavelength of interest, thus reducing the influence of background illumination.

Table A.1 – Pros and cons for choosing between 850nm and 940nm wavelengths.

Wavelength	Pros	Cons
850nm	▸ High quantum efficiency ($\simeq$ 30%)	▸ Red glow still visible ▸ High solar irradiance ($\simeq$ 35.9W.m^{-2}) ▸ Eye-safety standards more restrictive
940nm	▸ Totally invisible ▸ Low solar irradiance ($\simeq$ 15.7W.m^{-2}) ▸ Eye-safety standards less restrictive	▸ Low quantum efficiency ($\simeq$ 15%)

Finally, system parameters and lighting conditions must be carefully defined for targeting a specific depth range and resolution, which depends as well on the time measurement method. It exists two major ToF approaches: direct and indirect.

A.3.2 Direct Time-of-Flight and Time-Correlated Single-Photon Counting approaches

The direct Time-of-Flight (dToF) approach relies on the direct measurement of ToF Δt as a stopwatch would work. A timer is launched when a pulse is emitted by the optical emitter. The pulse is then reflected by the object back to the sensor which converts photons into electrons due to the photoelectric effect. The timer is stopped when a specific amount of photoelectrons (photogenerated electrons) is reached, providing ToF. High precision and high speed devices and circuits are however required due to the speed of light ($\simeq 3.10^8$ m/s). For instance, a depth resolution of 1mm is reached with a time resolution of 6.66ps. Another drawback is the detection threshold of photoelectrons that is highly sensitive to

electronic noise. The background illumination is another concern that could unintentionally exceed the threshold value and stop the counter. For that reason, a high peak power pulse can be employed but still limited to guarantee eye-safety. Despite its simplicity, the dToF measurement of optical pulses was not extensively adopted for 3D image sensors [28].

Another approach known as Time-Correlated Single-Photon Counting (TCSPC) is preferred over dToF for 3D image sensors and rangefinders as it allows to reduce the impact of background illumination and to avoid the detection threshold dependency of photoelectrons [29]. TCSPC technique relies on a similar principle to dToF but instead of measuring ToF based on a single back-reflected photon, a large number of detections is involved. A simplified schematic of TCSPC principle is illustrated in Figure A.6. Usually, a Single-Photon Avalanche Diode (SPAD), which is an avalanche diode operating in Geiger mode, associated to a quenching circuit and a Time-to-Digital Converter (TDC) are used for implementing a pixel. A start signal (either electrical or optical) is generated when a pulse is emitted by the optical emitter. A SPAD is then triggered when a photon is detected generating a large number of photoelectrons (avalanche breakdown). The resulting electrical signal is used as the stop signal. The TDC, acting as a high-speed timer, measures the arrival time of the photon with respect to the start signal. Finally, the quenching circuit stops the avalanche breakdown for starting a new cycle. Using a pulsed signal with a high repetition rate, this process can be repeated many times so that a photon distribution over time is built up, reproducing the illumination pulse shape. The ToF is then calculated from histogram data by determining the position of the peak within the histogram [28]. The basic principle of TCSPC measurement for building the histogram is illustrated in Figure A.7.

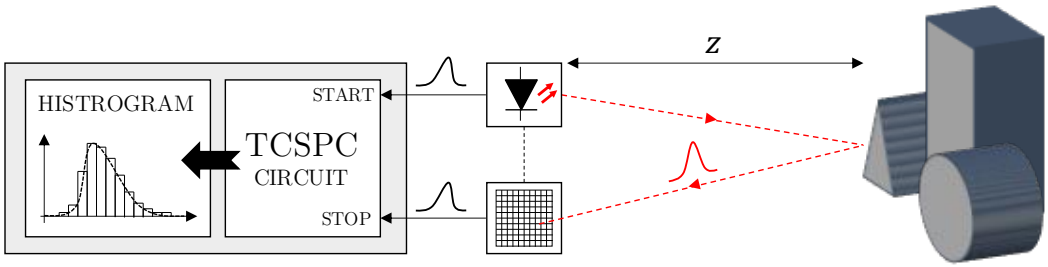


Figure A.6 – Simplified schematic of TCSPC principle.

This method still suffers from the need for high precision and high speed devices such as low-noise and low dark count-rate SPADs. This allows to reduce unintentional triggering due the random generation of electrons and holes (dark current). A high and short optical pulse is still required for limiting the impact of background illumination. In addition, another drawback concerns the high computational effort involved in the evaluation of

histograms [28].

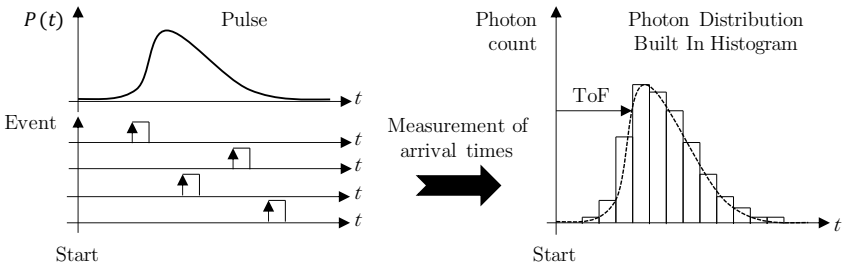


Figure A.7 – Basic principle of TCSPC measurement for building the histogram.

A.3.3 Indirect Time-of-Flight approach

The iToF approach relies on the measurement of the phase shift between a modulated optical signal and the optical signal received by the sensor after its reflection on an object, as illustrated in Figure A.8. The depth z is then given by

$$z = \frac{c}{4\pi f}\varphi \tag{A.10}$$

where φ is the phase shift (restricted to the range $[0\ ;\ 2\pi]$), f is the modulation frequency and c is the speed of light (in vacuum).

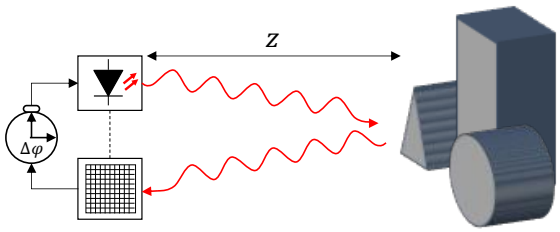


Figure A.8 – Simplified schematic of iToF approach. Here, the depth calculation is based on the phase shift measurement instead of the direct measurement of ToF.

Key parameters of iToF principle to provide specifications of the 3D image sensor with respect to general requirements are described hereafter.

A.3.3.1 Key parameters

Modulation type It exists two major modulation types: CW modulation and pulsed modulation. CW modulation encloses all types of modulation with a duty cycle close to

50% (sine or square waves for instance). Pulsed modulation stands for a waveform consisting of a train of short pulses where a very small duty cycle is typically used [28].

CW modulation is employed in this context for modulating the light signal. Optical pulses with a duty cycle close to 50% are sent through the scene (corresponding to a square wave). CW modulation is easier and cost-effective to implement at both sensor and optical emitter level because extremely fast transients are not required compared to pulsed modulation. Nevertheless, the square wave modulation used here introduces harmonics, thus EMI, through the system that may disturb other circuits within the mobile phone as well as algorithms for calculating the depth.

Unambiguous range As phase shift wraps around every 2π, one phase shift measurement value may actually leads to different depth values. The unambiguous range D_{AMB} is defined as the maximum measurable depth range for a given frequency:

$$D_{AMB} = \frac{c}{2f} \tag{A.11}$$

where f is the modulation frequency and c is the speed of light [170]. For instance, assuming $f = 50$MHz would lead to D_{AMB}=3m. In these conditions, an object could be located in a depth range from 0m up to 3m or from 3m up to 6m, and so on. Therefore, at least two different modulation frequencies must be used in order to find the correct location of the object, thus reducing the acquisition speed [170].

Demodulation method The phase shift measurement is usually based on the first harmonic of the modulation waveform only. It exists three major demodulation methods in order to extract the phase shift from the optical signal received on a pixel: demodulation by mixing, correlation or sampling.

- Demodulation by mixing (also known as homodyne or lock-in demodulation) consists in mixing the received signal with two electrical signals, one in phase with the emitted signal and the other in quadrature (I/Q). These mixed signals are then low-pass filtered leading to two components representing the real and imaginary part of the received signal, from which the phase shift is extracted [28]. Despite a method that is well known from RF communication circuits, it suffers from a high complexity resulting in a poor accuracy and a large pixel pitch due to demodulator and filter integrated in each pixel [29].
- Demodulation by correlation is similar to the first method but a cross-correlation function is used between the received signal and an electrical reference signal. The resulting correlated signal is then evaluated at four phases (0°, 90°, 180° and 270° for instance) in order to extract the phase shift [28].

- Demodulation by sampling consists in sampling the received signal according to a given number n of samples (three or more) per modulation period. A sample is also referred to as bin or tap in the literature and the demodulation process is named a n-bin or n-tap demodulation [27][33]. The phase-shift φ is then derived from the Discrete Fourier Transform (DFT) of the received signal by expressing its argument with the arctan function, as follows:

$$\varphi = \arctan\left(\frac{\sum_{k=0}^{n-1} x_k \sin\left(\frac{2k\pi}{n}\right)}{\sum_{k=0}^{n-1} x_k \cos\left(\frac{2k\pi}{n}\right)}\right) + C, \quad C \in \mathbb{R} \tag{A.12}$$

  where n is the total number of samples per modulation period, x_k is the k^{th} sample and C is a constant depending on real and imaginary parts' sign of the DFT in order to restrict the phase shift to the range $[0\ ;\ 2\pi]$.

Demodulation by sampling is employed in this context for its simplicity. For the present work, it has been assumed to consider a 4-bin demodulation method. An illustration of the sampling method is shown in Figure A.9. The phase shift φ can be approximated as

$$\varphi \simeq \arctan\left(\frac{x_1 - x_3}{x_0 - x_2}\right) \tag{A.13}$$

where x_0, x_1, x_2 and x_3 are the extracted samples.

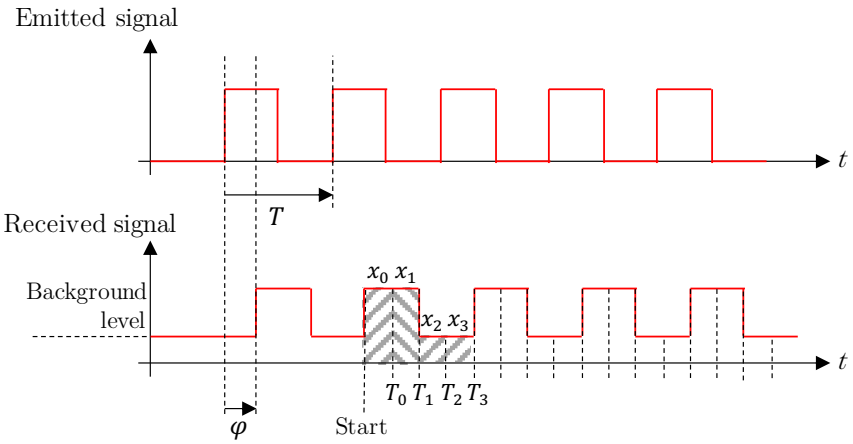


Figure A.9 – Simplified schematic of the sampling method assuming a 4-bin demodulation. The starting time is arbitrarily chosen for illustration purpose. Samples over each sampling period are represented by hatched areas during one modulation period. The demodulation process is repeated over the illumination cycle.

The number n of bins is a key feature of the sensor as it determines the implementation of pixels. Usually, a pixel is based on a Pinned Photodiode (PPD) at the center of the

photosensitive region connected to storage nodes (the so-called bins or taps) [32][34]. A simplified schematic of a typical pixel including one storage node is illustrated in Figure A.10. When the optical signal is impinging each pixel of the sensor, photons are converted into electrons over the sampling period. The charge is then stored into a bin and the sampling process is repeated during a modulation period. Samples are thus numbers of charge carriers as the result of the integration of a photo-current over time [31]. Then, a 4T-like readout circuitry is used to translate charges into voltage levels, in a similar way to that of standard CMOS image sensors [32]. Each pixel from the pixel array is able to extract the phase shift, thus the depth, from a given point of the scene. Therefore, the system can reconstruct a depth map of the whole scene. It however requires data acquiring on several illumination cycles, according to a specific illumination pattern (depending on general requirements, eye-safety standards and thermal considerations) before to provide a complete depth map.

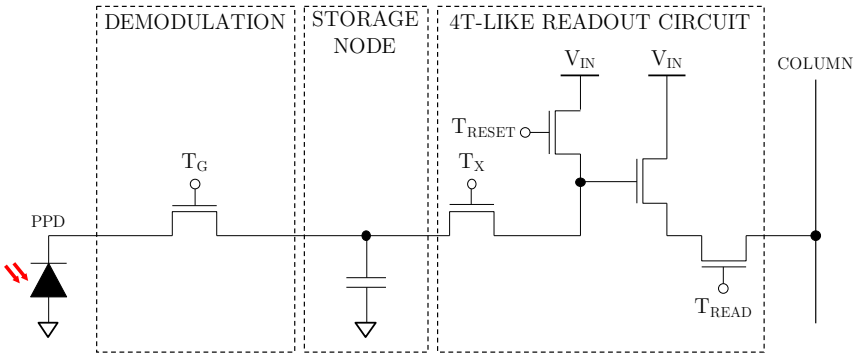


Figure A.10 – Simplified schematic of a typical iToF-based pixel including one storage node. Transistor T_G controls the path for transferring signal charges from the PPD into the storage node (the so-called bin). Other transistors compose the 4T-like readout circuitry for translating charges into voltage levels.

Depth resolution As stated earlier, the depth resolution depends on system parameters, lighting conditions and time measurement method. For iToF principle using a demodulation by sampling, the depth resolution depends on the quality of samples which is impacted by photonic and electronic noises. A major contributor is the photon shot noise (or quantum noise). It describes the statistical Poisson-distributed nature of the arrival process of photons and the generation process of electron-hole pairs [27]. Its standard deviation σ_N is given by:

$$\sigma_N = \sqrt{N} \tag{A.14}$$

where N is the number of photons or photogenerated charge carriers. In the case of a CW modulation method and a 4-bin demodulation process, the depth resolution, related to its

standard deviation, can be approximated as:

$$\sigma_z \simeq \frac{c}{4\sqrt{2}\pi f} \cdot \frac{\sqrt{A+B}}{c_d A} \tag{A.15}$$

where f is the modulation frequency, c is the speed of light and A and B are the mean numbers of electrons generated per sample (during the demodulation process) by the modulated optical signal after reflection and the background illumination respectively [31]. The parameter c_d is the demodulation contrast. It describes the overall demodulation performance of the sensor. It is given by:

$$c_d = \frac{A_{meas}}{A} \tag{A.16}$$

where A_{meas} and A are the measured amplitude and offset of the modulated optical signal after reflection (not including the background illumination) as a number of electrons respectively [31].

As the number of photogenerated electrons over a sampling period is related to the optical power received on a pixel of the sensor through its quantum efficiency, the depth resolution can be expressed in terms of optical power emitted from the optical emitter using Equation A.9. By assuming a CW modulation under indoor conditions, meaning a low-background illumination, the depth resolution can be approximated as:

$$\sigma_z \propto \frac{c}{4\sqrt{2}\pi f} \cdot \frac{\sqrt{P_{OPT}}}{P_{OPT}} \tag{A.17}$$

where f is the modulation frequency, c is the speed of light and $\mathrm{P_{OPT}}$ is the peak optical power at the optical emitter level. **Therefore, improving the depth resolution can be achieved by increasing the modulation frequency and the peak optical power.**

As explained in General Introduction, depending on the maximum targeting range, lighting conditions, objects reflectivity, sensor efficiency and eye-safety standards, optical pulses up to 2.5W for a modulation frequency from 50MHz up to 200MHz have been established for reaching a 3m maximum depth with a resolution lower than 0.5% of depth. These specifications rely on iToF key parameters described above and derive from a prior work done by the Analog, MEMS and Sensors department at STMicroelectronics. The present thesis is not intended to detail this work about iToF analysis.

A.3.3.2 iToF Sensor Model

An iToF sensor model is essential in order to evaluate performances of the system by using simulations. Considering the thesis context, only a basic model has been implemented as

a first approach. It aims to compute the phase shift between the emitted and received signals. The model relies on mathematical expressions describing the demodulation process.

Assuming a 4-bin demodulation process, the signal of interest is split over a modulation period into four equal sampling parts as illustrated in Figure A.9. The sampling period is given by:

$$T_S = \frac{T}{4} \tag{A.18}$$

where T is the modulation period. Samples are then extracted using the following expressions:

$$\begin{cases} x_0 = \int_{\text{start}}^{T_S} x(t)dt \\ x_1 = \int_{T_S}^{2T_S} x(t)dt \\ x_2 = \int_{2T_S}^{3T_S} x(t)dt \\ x_3 = \int_{3T_S}^{4T_S} x(t)dt, \text{ with } 4T_S = T \end{cases} \tag{A.19}$$

where x is the transient simulation waveform of interest and x_0, x_1, x_2 and x_3 are the extracted samples over a modulation period. Then, the arctan function is used to compute the signal phase as in Equation A.13. But practically, calculation algorithms use the "atan" function that limits the result to the range $]-\frac{\pi}{2}\ ;\ \frac{\pi}{2}[$. A constant must be added depending on numerator and denominator signs, in order to restrict the result to $[0\ ;\ 2\pi]$). It comes

$$\begin{cases} \varphi_x = \arctan\left(\frac{x_1-x_3}{x_0-x_2}\right) - \frac{\pi}{4}, \text{ if } (x_1-x_3) > 0 \text{ and } (x_0-x_2) > 0 \\ \varphi_x = \arctan\left(\frac{x_1-x_3}{x_0-x_2}\right) + \frac{3\pi}{4}, \text{ if } (x_1-x_3) > 0 \text{ and } (x_0-x_2) < 0 \\ \varphi_x = \arctan\left(\frac{x_1-x_3}{x_0-x_2}\right) + \frac{3\pi}{4}, \text{ if } (x_1-x_3) < 0 \text{ and } (x_0-x_2) < 0 \\ \varphi_x = \arctan\left(\frac{x_1-x_3}{x_0-x_2}\right) + \frac{7\pi}{4}, \text{ if } (x_1-x_3) < 0 \text{ and } (x_0-x_2) > 0 \end{cases} \tag{A.20}$$

where φ_x is the extracted phase for the signal of interest.

These operations must be performed for both the emitted and received signal in order to extract the phase shift φ, that is given by

$$\begin{cases} \varphi = \varphi_{\text{received}} - \varphi_{\text{emitted}}, \text{ if } (\varphi_{\text{received}} - \varphi_{\text{emitted}}) > 0 \\ \varphi = \varphi_{\text{received}} - \varphi_{\text{emitted}} + 2\pi, \text{ if } (\varphi_{\text{received}} - \varphi_{\text{emitted}}) < 0 \end{cases} \tag{A.21}$$

where φ_{emitted} and $\varphi_{\text{received}}$ are phases of the emitted and received signals respectively. In this way, the starting time for the sampling process can be chosen arbitrarily. Finally, the depth is extracted using Equation A.10.

The model is implemented as a text file suitable for the SPICE simulator Eldo from Mentor Graphics®. Inputs are the emitted and received signal transient waveforms, a starting time for sampling process as well as the modulation frequency, while the output is the depth result, as illustrated in Figure A.11.

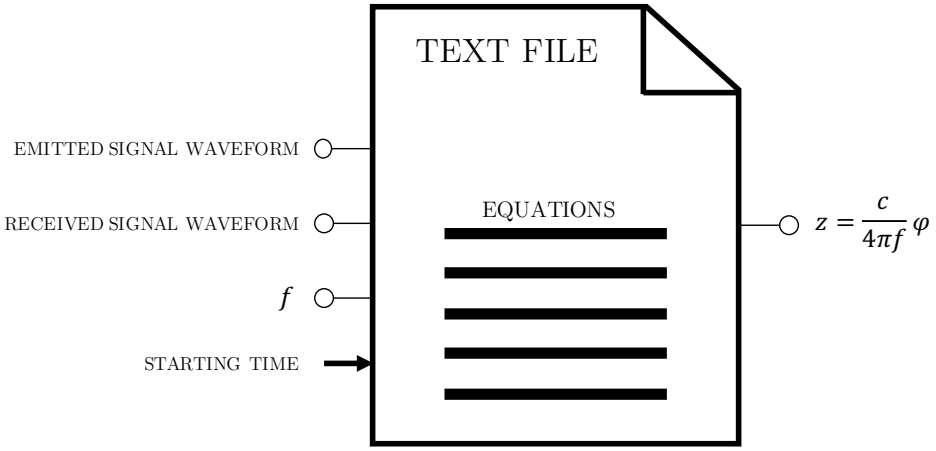


Figure A.11 – Illustration of the proposed iToF sensor model for extracting depth with a 4-bin demodulation method.

B Extraction of VCSEL Package Parastitics

Parasitics greatly impact the electrical and optical response of the VCSEL diode. Thus, it is essential to know these parameters in order to design the laser diode driver. Since a SPICE file has been provided by the VCSEL supplier for modeling the electrical behavior of the VCSEL array, only parasitics from the package module need to be extracted. This appendix describes the proposed method for extracting parasitics of the VCSEL package from S-parameter measurements by using a fitting procedure, as detailed in [171][97].

As a reminder, the electrical equivalent-circuit VCSEL model is depicted in Figure B.1. Parameters that need to be extracted are the wire bonding inductance L_{PKG} and the parasitic capacitance C_{PKG} due to anode and cathode contacts. The SPICE file is not detailed here. As these parameters vary with frequency, it is suggested to extract values from 100kHz up to 1GHz, at room temperature only (25°C). In addition, due to the use of a laser diode, measurements must be performed while accommodating eye-safety standards.

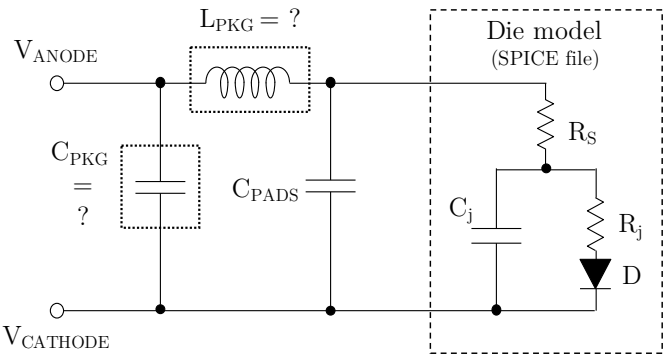


Figure B.1 – Electrical equivalent circuit VCSEL model.

B.1 Method of Extraction

It is proposed to extract parameters L_{PKG} and C_{PKG} from a measurement set of the two-port electrical S-parameters of the VCSEL module, considered here as the device to be tested, also referring to as Device Under Test (DUT). Scattering parameters (S-parameters) allow to characterize a two-port network in a well-defined environment by evaluating transmitted and reflected power waves from an electrical power injected through the network [172][173]. The network is usually connected to a Vector Network Analyzer (VNA) using a characteristic impedance of 50Ω. S-parameters, gathered into a matrix, can be described as a complex impedance. Then, values of parasitic components can be obtained by using a fitting procedure to match the VCSEL model with S-parameter measurement. Some concerns to perform measurements in this context, such as using a calibration procedure as well as a suitable de-embedding technique, are addressed thereafter.

B.1.1 Vector Network Analyzer

A VNA is used to measure the S-parameters. A simplified block diagram is illustrated in Figure B.2. It employs synthesized-frequency sources to provide a known test stimulus that can sweep across a range of frequencies or power levels. A more detailed description of network analyzer architecture can be found in [174]. In order to get S-parameters of a two port network, such as the VCSEL module, a signal is applied from port 1 to port 2, and vice versa, while measuring reflected and transmitted waves. A DC biasing can be applied to the DUT through a bias-T which consists of a simple LC circuit able to protect the VNA from the DC level as well as the DC generator from the RF stimulus.

As the VCSEL module is a two-terminal device acting as a high-impedance component for currents below threshold, the series-through technique is used here, which consists in connecting the VCSEL module in series from port 1 to port 2 as illustrated in Figure B.2. Moreover, it could be interesting to get S-parameters for two operating points such as without biasing (0A) and near the threshold current (300mA) when the VCSEL starts lasing.

B.1.2 Calibration procedure

Some additional components, such as coaxial cables, connectors and bias-Ts, are required to connect the DUT to the VNA ports. Usually, coplanar waveguide probe with Ground-Signal-Ground (GSG) contacts are placed as close as possible to the DUT for proper measurements. Therefore, the measurement system must be calibrated to define a reference plane at probe tips for measuring S-parameters [175]. This allows to overcome systematic errors from the VNA and connection components.

The calibration procedure consists in measuring standard mechanical test fixtures with well-known impedance characteristics in a first time. Then, systematic errors are esti-

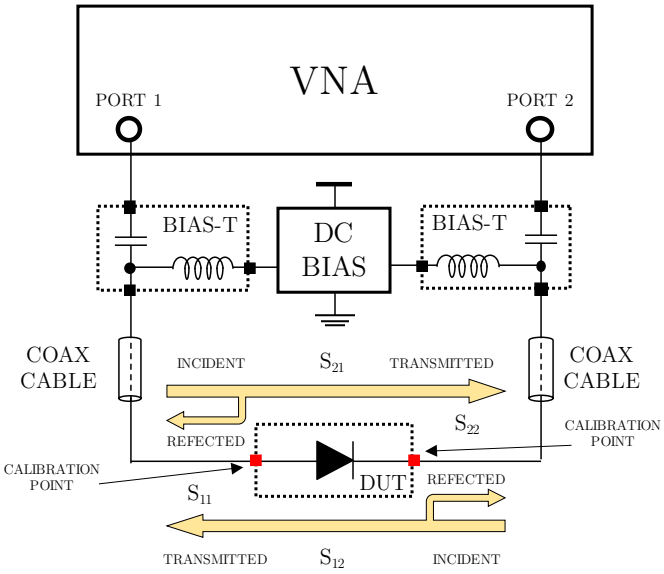


Figure B.2 – VNA block diagram superimposed with power waves.

mated and subtracted from the S-parameter measurements. It exists various calibration techniques such as Short-Open-Load-Thru (SOLT), Thru-Reflect-Line (TRL) or Line-Reflect-Match (LRM) for instance. Here, an electronic calibration is preferred making the procedure fast, easy and less prone to operator errors [175]. The impedance characteristics in the calibration module are switched with PIN-diode or FET switches, so the calibration standards never wear out.

B.1.3 De-embedding technique

Usually, the DUT is mounted on a test board with a coplanar waveguide to carry the RF stimulus, bringing extra parasitics due to transmission lines, pads and connectors. The equivalent schematic of the DUT after calibration, thus including parasitics, is illustrated in Figure B.3c. As a consequence, a de-embedding technique is required to define the reference plane at the DUT terminals taking into account parasitic elements. For that purpose, parasitics are characterized by using specific interconnect patterns. Then they are subtracted from S-parameters after calibration so that the actual DUT S-parameters can be obtained [171][97]. Two specific interconnect patterns are used, which equivalent schematics are illustrated in Figure B.3:

- An "open" pattern allows to evaluate capacitive effects between signal and ground lines, represented by admittances Y_1, Y_2 and Y_3 in Figure B.3a.
- A "short" pattern allows to evaluate resistive and inductive effects due to lines and pads, represented by impedances Z_1, Z_2 and Z_3 in Figure B.3b.

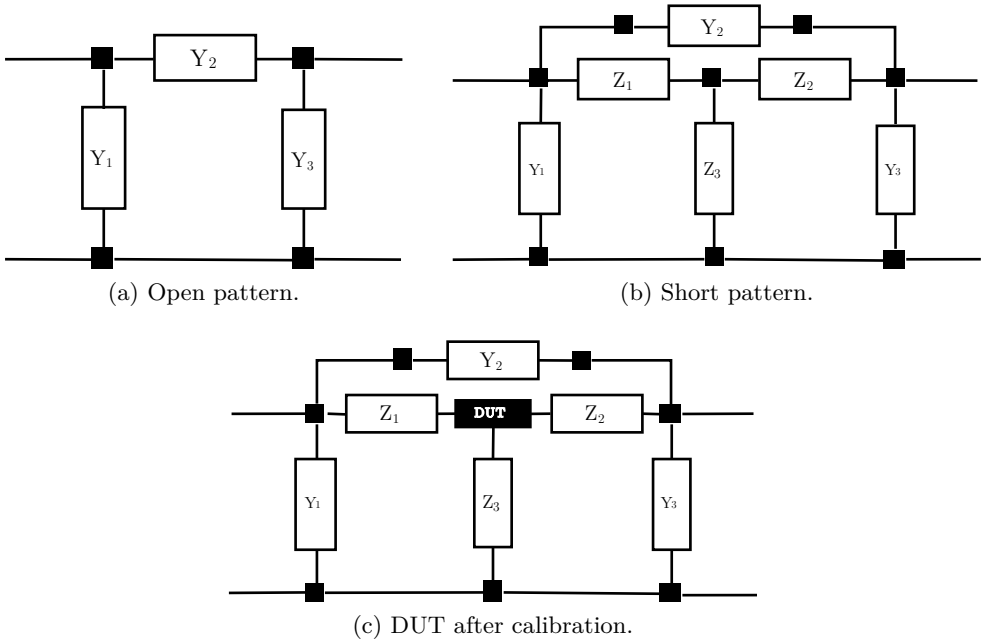
It can be noticed that the short pattern includes admittances Y_1, Y_2 and Y_3 as well. Therefore, the measured "short" S-parameters must be corrected by using "open" S-parameter measurements. Once S-parameters for open and short patterns are extracted, resulting in $[S_{OPEN}]$ and $[S_{SHORT}]$ matrices respectively, the actual DUT S-parameters, gathered into matrix $[S_{DUT}]$, can be obtained from S-parameters measured after calibration, gathered into matrix $[S_{TOT}]$, with calculations as follows:

$$[S_i] \longrightarrow [Y_i] \tag{B.1}$$

$$\Rightarrow [Y_{DUT}] = \Big(([Y_{TOT}] - [Y_{OPEN}])^{-1} - ([Y_{OPEN}] - [Y_{SHORT}])^{-1}\Big)^{-1} \tag{B.2}$$

$$\Rightarrow [Y_{DUT}] \longrightarrow [S_{DUT}] \tag{B.3}$$

Equation B.2 describes the conversion of each S-parameters into Y-parameters (admittance parameters). In contrary, Equation B.3 describes the conversion of the DUT Y-parameters into the final DUT S-parameters.



(a) Open pattern.

(b) Short pattern.

(c) DUT after calibration.

Figure B.3 – Equivalent schematics of interconnect patterns and DUT after calibration.

B.1.4 Extraction of parasitics

The DUT can be seen as a pi network including admittances Y_1, Y_2 and Y_3, as illustrated in Figure B.4, from which S-parameters can be extracted using the de-embedding technique

previously described. By using this pi network, admittance Y_2 is identified as the VCSEL model while admittances Y_1 and Y_3 represents the capacitive coupling with ground line. Admittance Y_2 is extracted from the DUT S-parameters as follows:

$$[S_{DUT}] \longrightarrow [Y_{DUT}] \tag{B.4}$$

$$\Rightarrow [Y_{DUT}] = \begin{bmatrix} Y_{11} & Y_{21} \\ Y_{12} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_1 + Y_2 & -Y_2 \\ -Y_2 & Y_3 + Y_2 \end{bmatrix} \tag{B.5}$$

$$\Rightarrow Y_2 = -Y_{12} = -Y_{21} \tag{B.6}$$

At last, values of parasitic components, such as L_{PKG} and C_{PKG}, are obtained by using a fitting procedure to match the VCSEL model admittance with the measured Y_{12} (or Y_{21}) coefficients over the whole frequency range. The package capacitance C_{PKG} can be extracted by fitting the total laser diode capacitance C_{TOT} without biasing (0A), with the imaginary parts of Y_{12} coefficient such as

$$C_{TOT} = C_j + C_{PKG} + C_{PADS} = -\frac{\Im\mathfrak{m}(Y_{12})}{2\pi f} \tag{B.7}$$

where C_j is the laser diode junction capacitance, C_{PADS} is the pads capacitance and f is the frequency swept over the whole range. The parasitic inductance L_{PKG} can be extracted by fitting the real and imaginary parts of Y_{12} coefficient over the whole frequency range.

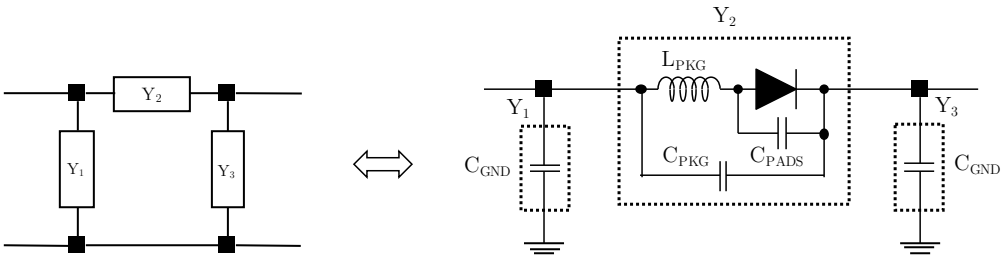


Figure B.4 – Equivalent schematic of the DUT seen as a pi network.

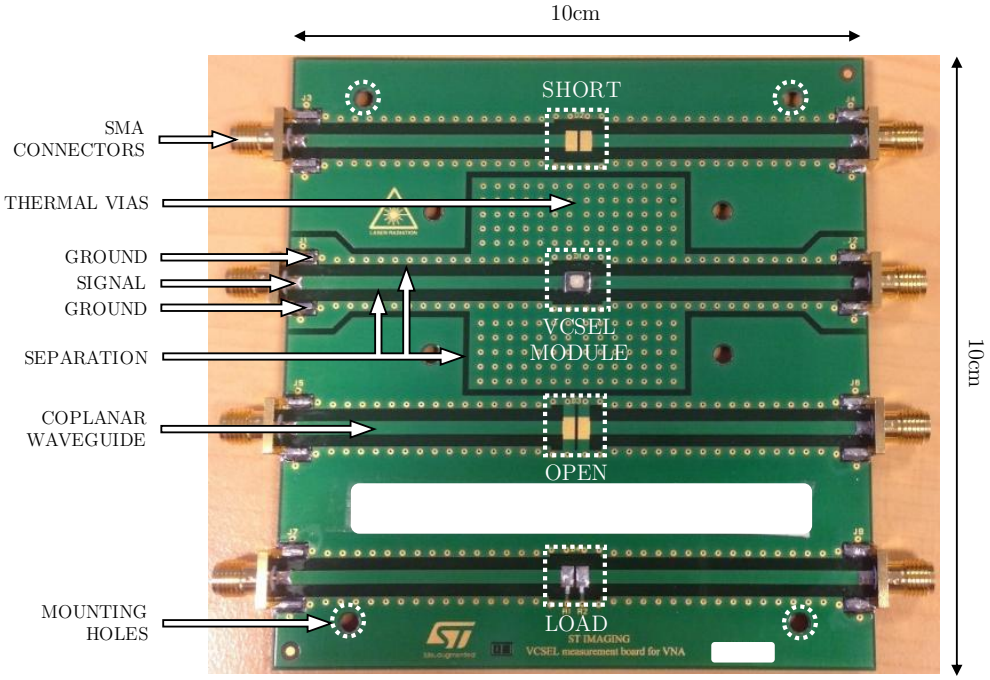
B.2 Test Board and Experimental Setup

This section gives some considerations for designing the test board and performing measurements.

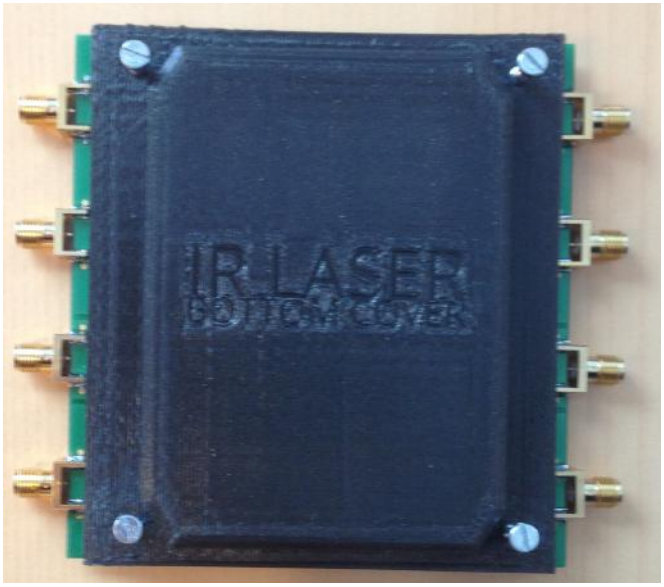
B.2.1 Test board overview

A test board has been realized in order to measure S-parameters of the VCSEL module. Open and short interconnect patterns have been included for the de-embedding technique.

Coplanar waveguides with a ground plane on the back side of the substrate are employed to convey RF signals, through SMA (standing for SubMiniature version A) connectors. The test board relies on a PCB using 2 layers with 35µm copper tracks and a standard FR4 glass epoxy dielectric. The board has a size of 10cmx10cm. A picture is shown in Figure B.5. Some mounting holes are machined to attach a protective cap over the front side of the board, thus blocking all laser radiations. Thermal VIAs surrounding the VCSEL module have been added in order to minimize the self-heating in case of applying a high DC biasing.



(a) Test board.



(b) Test board with laser safety covering.

Figure B.5 – Pictures of the test board. For confidentiality reasons, labels have been hidden.

B.2.2 Experimental setup

A test bench has been set up in order to perform S-parameter measurements. An electronic calibration module (ECal) has been preferred here to perform the VNA calibration. A mechanical calibration kit has been selected as well for caution. A pulsed measurement has been configured when a DC biasing was required in order to avoid self-heating effects. In addition, measurements have been performed in a dark room using laser safety glasses for caution. A picture is shown in Figure 4.7. The equipments are listed hereafter:

- DC voltage generator: Keysight N6705B DC power analyzer
- VNA: Keysight E5080A ENA vector network analyzer, 9kHz up to 9GHz.
- Calibration :
  - Keysight N4691B electronic calibration module
  - Keysight 85052D mechanical calibration kit
- Oscilloscope: Keysight MSOX3104T 1GHz mixed-signal oscilloscope
- Laser safety glasses: Thorlabs LG1 glasses

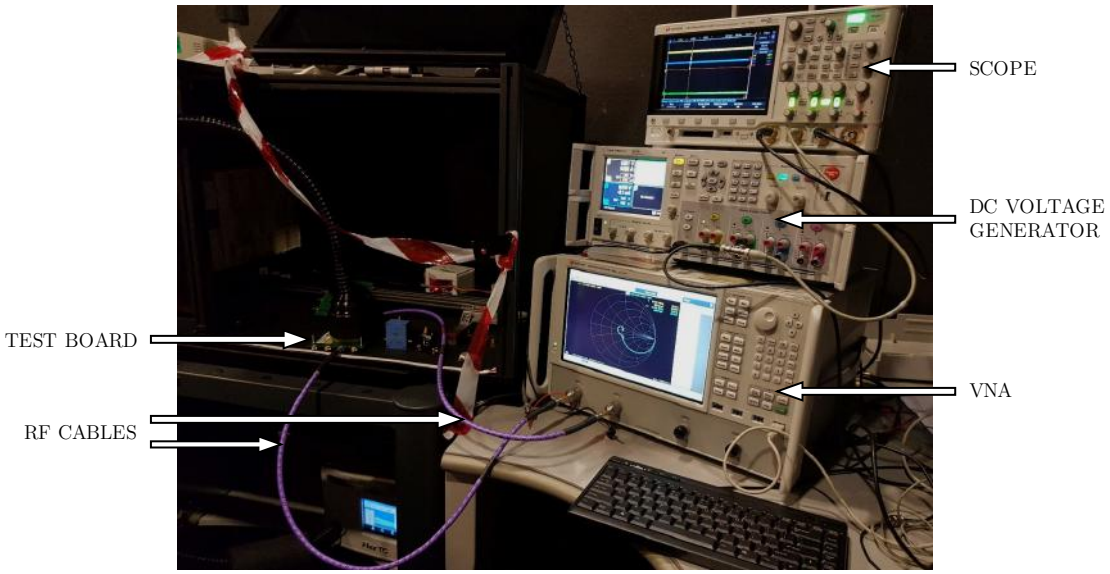


Figure B.6 – Pictures of the test bench, settled in a dark room.

B.3 Measurement Results

This section gives a quick analysis of S-parameters of the DUT after de-embedding. It then presents the extraction of parasitic values from these measurements. Due to technical reasons, S-parameters are valid up to 600MHz only.

B.3.1 Analysis of S-parameters

Figure B.7 plots the S_{11} coefficient of the DUT after de-embedding on a Smith chart. It is clarified that the S_{11} coefficient represents the reflection coefficient. When no biasing is applied, the VCSEL module is considered as an open circuit at low frequency due to capacitance behavior. As the frequency increases, the resistive part of the S_{11} coefficient is almost constant due to constant series resistance. At relatively high frequency, around 500MHz, the VCSEL module is considered as a through, meaning that its impedance is matched with the 50Ω characteristic impedance due to the resonance of parasitic inductances and capacitances. When a biasing is applied (300mA here), the VCSEL module is considered as a through up to around 500MHz due to its low impedance when on.

As a conclusion, the VCSEL module behaves as expected up to 600MHz.

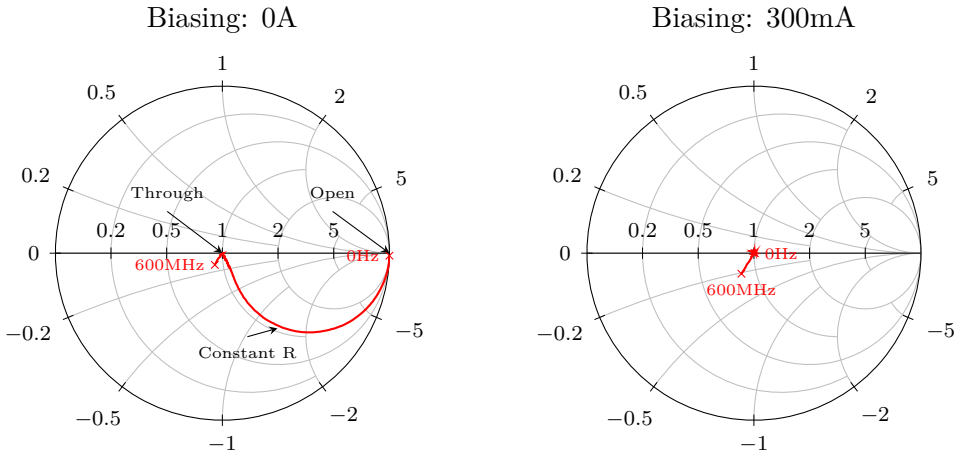


Figure B.7 – Smith chart: S_{11} coefficient of DUT after de-embedding for two biasing currents.

B.3.2 Extraction of Parasitics

B.3.2.1 Extraction of C_{PKG}

The total capacitance C_{TOT} has been evaluated from the measured Y_{12} coefficient without biasing by using Equation B.7. Figure B.8 plots the total capacitance evaluated around 230pF from measurement at low frequency. By knowing C_j (160pF) and C_{PADS} (5pF) from the VCSEL model, the value of C_{PKG} has been estimated around 60pF. A relatively good agreement is obtained between measurement and simulation at low frequency.

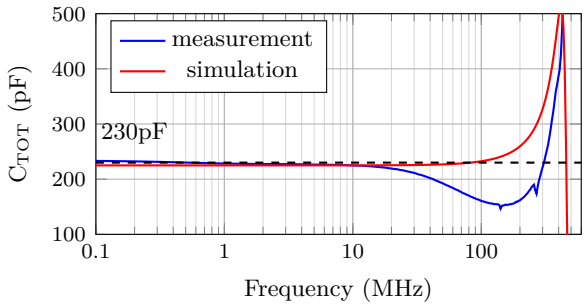


Figure B.8 – Total capacitance extracted from measured Y_{12} coefficient, with no biasing.

B.3.2.2 Extraction of L_{PKG}

Figure B.9 plots the real and imaginary parts of the measured Y_{12} coefficient. The parasitic inductance L_{PKG} has been estimated around 700pH by fitting real and imaginary parts of Y_{12} coefficient through simulation. A relatively good agreement is obtained between measurement and simulation at low frequency and without biasing.

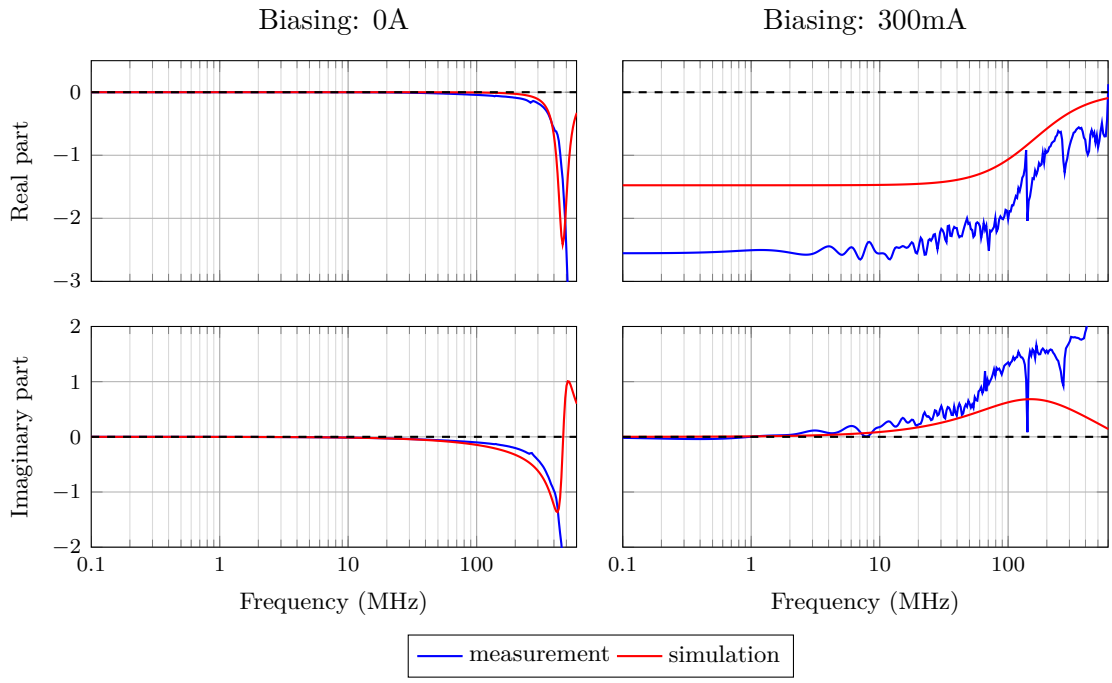


Figure B.9 – Real and imaginary parts of the measured Y_{12} coefficient, for two biasing currents.

B.4 Summary

Values of parasitics are summarized in Table B.1.

Table B.1 – Estimated parasitics of the VCSEL module.

Parameter	**Value**
Parasitic inductance L_{PKG}	700pH
Package capacitance C_{PKG}	60pF
Pads capacitance C_{PADS}	5pF

C Theoretical Expressions of Losses

This appendix details theoretical expressions of major losses for each device involved in each solution proposed in the preliminary design study (see Chapter 2). The laser diode is considered as a load therefore major losses concern the driver. Only electrical quantities are considered here. Losses are conduction losses through passive components (DCR of inductor, ESR of output capacitor) as well as MOSFET channels (R_{ON}), and switching losses due to switching of MOSFET input and output capacitances (C_{IN} and C_{OUT}). Total losses of a driver topology are given by the following expression:

$$P_{LOSS} = \sum_i P_{COND(i)} + \sum_i P_{SW(i)} \tag{C.1}$$

$$\text{with } P_{COND(i)} = R_{(i)} I^2_{RMS(i)} \text{ and } P_{SW(i)} = C_{IN(i)} V^2_{IN} f_{(i)} + C_{OUT(i)} V^2_{DS(i)} f_{(i)} \tag{C.2}$$

where $P_{COND(i)}$ and $P_{SW(i)}$ are respectively the average conduction and switching losses of the i^{th} device of interest when possible. $R_{(i)}$ is the equivalent resistance of the i^{th} device channel, $I_{RMS(i)}$ is the RMS current through the i^{th} device, $C_{IN(i)}$ is the input capacitance of the i^{th} device, $C_{OUT(i)}$ is the output capacitance of the i^{th} device, V_{IN} is the driving circuitry input voltage, $V_{DS(i)}$ is the drain-to-source voltage of the i^{th} device, $f_{(i)}$ is the switching frequency of the i^{th} device (in this case, either the operating frequency of the power stage or the PRF of the switching element). Expressions concerning each device for each solution are detailed hereafter.

A square shape for current pulses through paths of laser diode and switching elements has been assumed in order to simplify the study. Conduction losses through devices from the DC/DC converter are expressed as a function of the inductor current $I_{(L)}$. In addition, the same input voltage has been assumed for all MOSFET driving circuitries. It can also be recalled that D is the duty cycle of a switching cycle from the power stage and α is the modulation duty cycle of the diode current.

C.1 Solution #1: Voltage-mode Driver in Series Configuration

As a reminder, the driver described in solution #1 includes a four-switch non-inverting buck-boost DC/DC converter and a switching element. Since the converter can operate in three different modes (buck, buck-boost or boost modes) depending on operating conditions, some devices may not involve conduction or switching losses (see the operating principle described in Part 2.3.3). For easy readability, conduction and switching losses expressions for each device of interest are summarized in Tables C.1 and C.2 respectively.

C.2 Solution #2: Current-mode Driver in Shunt Configuration

As a reminder, the driver described in solution #2 includes a conventional buck DC/DC converter without output capacitance, and a switching element. For easy readability, conduction and switching losses expressions for each device are summarized in Tables C.3 and C.4 respectively.

C.3 Solution #3: Current-mode Driver in Series Configuration

As a reminder, the driver described in solution #3 includes a conventional boost DC/DC converter, a cascode transistor acting as a current source and a switching element. For easy readability, conduction and switching losses expressions for each device are summarized in Tables C.5 and C.6 respectively. It is reminded that V_{SAT} is the saturation voltage of the cascode transistor when operating in saturation region.

Table C.1 – Solution #1: expressions of conduction losses for each device of interest (see Figure 2.14).

Devices	$P_{COND(i)}$		
	Buck mode	Buck-boost mode	Boost mode
T_1	$R_{ON(T_1)}D(I_L^2+\frac{\Delta I_L^2}{12})$	$R_{ON(T_1)}D(I_L^2+\frac{\Delta I_L^2}{12})$	$R_{ON(T_1)}(I_L^2+\frac{\Delta I_L^2}{12})$
T_2	$R_{ON(T_2)}(1-D)(I_L^2+\frac{\Delta I_L^2}{12})$	$R_{ON(T_2)}(1-D)(I_L^2+\frac{\Delta I_L^2}{12})$	0
T_3	0	$R_{ON(T_3)}(D)(I_L^2+\frac{\Delta I_L^2}{12})$	$R_{ON(T_3)}(D)(I_L^2+\frac{\Delta I_L^2}{12})$
T_4	$R_{ON(T_4)}(I_L^2+\frac{\Delta I_L^2}{12})$	$R_{ON(T_4)}(1-D)(I_L^2+\frac{\Delta I_L^2}{12})$	$R_{ON(T_4)}(1-D)(I_L^2+\frac{\Delta I_L^2}{12})$
L	$R_L(I_L^2+\frac{\Delta I_L^2}{12})$	$R_L(I_L^2+\frac{\Delta I_L^2}{12})$	$R_L(I_L^2+\frac{\Delta I_L^2}{12})$
C_{OUT}	$R_{C_{OUT}}\frac{\Delta I_L^2}{12}$	$R_{C_{OUT}}[I_L^2D(1-D)+\frac{D\Delta I_L^2}{12}]$	$R_{C_{OUT}}[I_L^2D(1-D)+\frac{D\Delta I_L^2}{12}]$
T_{SW}	$\alpha R_{ON(T_{SW})}I_{ON}^2$	$\alpha R_{ON(T_{SW})}I_{ON}^2$	$\alpha R_{ON(T_{SW})}I_{ON}^2$
Total	$P_{COND(BUCK)}$	$P_{COND(BUCK-BOOST)}$	$P_{COND(BOOST)}$

Table C.2 – Solution #1: expressions of switching losses for each device of interest (see Figure 2.14).

Devices	$\boldsymbol{P_{SW(i)}}$		
	Buck mode	Buck-boost mode	Boost mode
T_1	$C_{IN(T_1)}V_{IN}^2 f_{SW}$ $+C_{OUT(T_1)}V_{IN}^2 f_{SW}$	$C_{IN(T_1)}V_{IN}^2 f_{SW}$ $+C_{OUT(T_1)}V_{IN}^2 f_{SW}$	0
T_2	$C_{IN(T_2)}V_{IN}^2 f_{SW}$ $+C_{OUT(T_2)}V_{IN}^2 f_{SW}$	$C_{IN(T_2)}V_{IN}^2 f_{SW}$ $+C_{OUT(T_2)}V_{IN}^2 f_{SW}$	0
T_3	0	$C_{IN(T_3)}V_{IN}^2 f_{SW}$ $+C_{OUT(T_3)}V_{OUT}^2 f_{SW}$	$C_{IN(T_3)}V_{IN}^2 f_{SW}$ $+C_{OUT(T_3)}V_{OUT}^2 f_{SW}$
T_4	0	$C_{IN(T_4)}V_{IN}^2 f_{SW}$ $+C_{OUT(T_4)}V_{OUT}^2 f_{SW}$	$C_{IN(T_4)}V_{IN}^2 f_{SW}$ $+C_{OUT(T_4)}V_{OUT}^2 f_{SW}$
T_{SW}	$C_{IN(T_{SW})}V_{IN}^2 f_{MOD}$ $+C_{OUT(T_{SW})}V_{DS}^2 f_{MOD}$	$C_{IN(T_{SW})}V_{IN}^2 f_{MOD}$ $+C_{OUT(T_{SW})}V_{DS}^2 f_{MOD}$	$C_{IN(T_{SW})}V_{IN}^2 f_{MOD}$ $+C_{OUT(T_{SW})}V_{DS}^2 f_{MOD}$
Total	$P_{SW(BUCK)}$	$P_{SW(BUCK-BOOST)}$	$P_{SW(BOOST)}$

Table C.3 – Solution #2: expressions of conduction losses for each device of interest (see Figure 2.20).

Devices	$\boldsymbol{P_{COND(i)}}$
T_1	$R_{ON(T_1)} D (I_L^2 + \frac{\Delta I_L^2}{12})$
T_2	$R_{ON(T_2)} (1-D) (I_L^2 + \frac{\Delta I_L^2}{12})$
L	$R_L (I_L^2 + \frac{\Delta I_L^2}{12})$
T_{SW}	$(1-\alpha) R_{ON(T_{SW})} I_{ON}^2$
Total	$P_{COND(TOT)}$

Table C.4 – Solution #2: expressions of switching losses for each device of interest (see Figure 2.20).

Devices	$P_{SW(i)}$
T_1	$C_{IN(T_1)}V_{IN}^2 f_{SW} + C_{OUT(T_1)}V_{IN}^2 f_{SW}$
T_2	$C_{IN(T_2)}V_{IN}^2 f_{SW} + C_{OUT(T_2)}V_{IN}^2 f_{SW}$
T_{SW}	$C_{IN(T_{SW})}V_{IN}^2 f_{MOD} + C_{OUT(T_{SW})}V_{DS}^2 f_{MOD}$
Total	$P_{SW(TOT)}$

Table C.5 – Solution #3: expressions of conduction losses for each device of interest (see Figure 2.26).

Devices	$\boldsymbol{P_{COND(i)}}$
T_1	$R_{ON(T_1)}(1-D)(I_L^2+\frac{\Delta I_L^2}{12})$
T_2	$R_{ON(T_2)}D(I_L^2+\frac{\Delta I_L^2}{12})$
L	$R_L(I_L^2+\frac{\Delta I_L^2}{12})$
C_{OUT}	$R_{C_{OUT}}[I_L^2D(1-D)+\frac{D\Delta I_L^2}{12}]$
T_{SAT}	$\alpha V_{SAT}I_{ON}$
T_{SW}	$\alpha R_{ON(T_{SW})}I_{ON}^2$
Total	$P_{COND(TOT)}$

Table C.6 – Solution #3: expressions of switching losses for each device of interest (see Figure 2.26).

Devices	$\boldsymbol{P_{SW(i)}}$
T_1	$C_{IN(T_1)}V_{IN}^2 f_{SW} + C_{OUT(T_1)}V_{OUT}^2 f_{SW}$
T_2	$C_{IN(T_2)}V_{IN}^2 f_{SW} + C_{OUT(T_2)}V_{OUT}^2 f_{SW}$
T_{SW}	$C_{IN(T_{SW})}V_{IN}^2 f_{MOD} + C_{OUT(T_{SW})}V_{DS}^2 f_{MOD}$
Total	$P_{SW(TOT)}$

D Power Delivery Network Design

This appendix details the methodology for designing a PDN dedicated to the HFS block. Using low-impedance power tracks and a ground plane with appropriate decoupling capacitors is required in order to properly supply the integrated circuit. A methodology for designing a PDN is well described in the literature [145][146]. It relies on the optimization of the PDN impedance, by selecting suitable capacitors, so that its value does not exceed a target impedance over a specific bandwidth. The target impedance Z_T (in Ω) is expressed as

$$Z_T = \frac{\Delta V}{\Delta I} \tag{D.1}$$

where ΔV is the allowed voltage ripple and ΔI is the transient current. Usually, the resulting target impedance is very small and constraining. It leads to an overdesign by choosing a very large number of decoupling capacitors which is not realistic regarding cost and PCB area constraints [147][148]. The methodology proposed in [148] is considered here. It is based on the definition of the allowable voltage ripple and the corresponding current transient for the frequency range of interest. It allows to reduce constraints on the target impedance for various frequency bandwidths. The design flow is summarized as follows:

1. Definition of the frequency ranges of interest: about one decade below and above the largest anti-resonance frequency of the PDN impedance (corresponding to peak impedance value).
2. Definition of the voltage ripple tolerance for each frequency range.
3. Estimation of the transient current for each frequency range (using the Fast Fourier Transform (FFT) and the inverse FFT of the current waveform).
4. Calculation of the target impedance for each frequency range.
5. Selection of decoupling capacitors to meet the target impedance.

It must be clarified that the PDN for the HFS block is designed by considering the largest devices (80mm gate width for the switching element, full driving capability for the gate driver, HVDrift 18V device for the cascode device).

D.1 Definition of the frequency ranges of interest

The largest anti-resonance of the PDN impedance is given by

$$f_{ar} = \frac{1}{2\pi\sqrt{LC}} \tag{D.2}$$

where C is the on-chip capacitance and L is the equivalent series inductance of the current-loop between integrated circuit pins and power supply terminals on PCB. The total on-chip capacitance is 2.4nF while the loop inductance has been estimated around 6nH (see Figure 3.24). It comes an anti-resonance around 40MHz. Thus, frequency ranges are defined as follows:

- Range 1 is from DC up to 10MHz,
- range 2 from 10MHz up to 1GHz,
- range 3 from 1GHz up to very high frequencies.

D.2 Definition of the voltage ripple tolerance

The voltage ripple tolerance is defined as the maximum voltage variation admissible on the power supply for ensuring a proper operation of the gate driver when switching. It is defined as

$$V_{\%} = \frac{\Delta V_{IN}}{V_{IN}} \tag{D.3}$$

where ΔV_{IN} is the voltage ripple and V_{IN} is the input voltage. In this context, the rising time of the gate signal is chosen as a target for representing a proper operation. A minimum of 350ps seems to be a reasonable constraint (see Table 3.8). In order to determine the voltage ripple tolerance for each frequency range, ideal transient simulations are performed by adding a sine wave ripple to the HFS block power supply, modeling parasitic effects. The ripple amplitude is swept from 1% up to 33% of the input voltage while the ripple frequency is arbitrarily set according to each frequency range (10MHz for range 1, 50MHz, 100MHz, 150MHz and 200MHz for range 2 and 1GHz for range 3). The rising time is then extracted and the maximum voltage ripple tolerance is identified to meet the target (>350ps) for each range. Results are summarized in Table D.1. Typical conditions (typ. process, 3.6V, 25°C) have been assumed for simulations. Various switching frequencies have been considered.

Table D.1 – Voltage ripple tolerance for each frequency range and various use cases.

Use case	Maximum voltage ripple tolerance (in %)		
	Range 1	Range 2	Range 3
Case 1: 50MHz	8%	1%	1%
Case 2: 100MHz	19%	1%	1%
Case 3: 150MHz	22%	1%	1%
Case 4: 200MHz	22%	1%	1%

D.3 Estimation of the transient current

Transient simulations in typical conditions are performed to extract the transient current drawn by the HFS block for charging input capacitances. A FFT is applied to convert results in the frequency domain. Then, an inverse FFT is applied by considering data only for the frequency range of interest to convert results back to the time domain. The maximum transient current is estimated as the peak current of the resulting current waveform. Results are summarized in Table D.2.

Table D.2 – Peak current for each frequency range and various use cases

Use case	Maximum peak current (in A)		
	Range 1	Range 2	Range 3
Case 1: 50MHz	0.09	2.89	5.02
Case 2: 100MHz	0.18	2.82	4.78
Case 3: 150MHz	0.28	2.55	4.89
Case 4: 200MHz	0.37	2.52	4.67

D.4 Calculation of the target impedance

The target impedance for each range is defined using Equation D.1 with the corresponding voltage ripple and peak current. Results are summarized in Table D.3. The most restrictive values are retained as a target impedance. A suitable bank of decoupling capacitors can be selected while respecting this target impedance (see Figure 3.25).

Table D.3 – Target impedance for each frequency range and various use cases. The most restrictive values are colored in red.

Use case	**Target impedance (in Ω)**		
	Range 1	**Range 2**	**Range 3**
Case 1: 50MHz	3.14	0.01	0.01
Case 2: 100MHz	3.66	0.01	0.01
Case 3: 150MHz	2.9	0.01	0.01
Case 4: 200MHz	2.18	0.01	0.01

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