Unidirectional high-ratio DC-DC converter for renewable energy sources

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Unidirectional High-Ratio DC-DC Converter for Renewable Energy Sources

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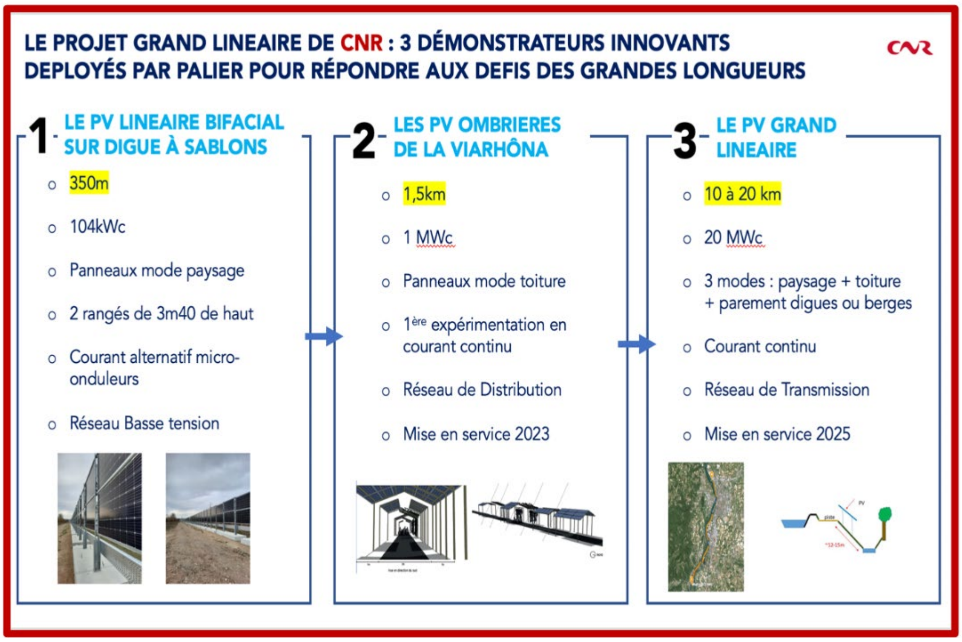
Résumé

Poussée par la nécessité de décarbonner la production d’énergie, l’intégration des sources d’énergie renouvelables dans le réseau électrique est devenue un sujet important du génie électrique moderne. Du fait de la faible densité de puissance des sources d’énergies renouvelables (par rapport aux solutions conventionnelles, fossiles ou nucléaire) un réseau de collection moyenne tension (HTA, MV) AC est généralement mis en place avant d’élever la tension du point de collection à une tension plus élevée (toujours MV ou haute tension (HTB, HV) en fonction de la puissance totale de l’installation) pour le transport sur le réseau. De la même façon que le passage au courant continu a été prouvé bénéfique pour la haute tension (HVDC pour le transport de fortes puissances sur de grandes distances), le MVDC est envisagé pour les réseaux de collection d’énergies renouvelables. Cependant, là où la solution AC dispose du bien connu et maîtrisé transformateur basse fréquence pour élever la basse tension (BT, LV) d’environ 1 kV vers des dizaines de kV, le convertisseur DC-DC réalisant la même fonction en MVDC est bien loin d’être une réalité industrielle. La palette de sujets abordées dans cette thèse s’étend de la définition des exigences auxquelles un tel convertisseur doit répondre jusqu’aux propositions d’implémentations matérielles le permettant, en passant par la sélection de la topologie la plus adaptée ainsi que par l’adaptation de son contrôle. Les différents points étudiés sont accompagnés de validations expérimentales utilisant différentes maquettes. Un prototype complet de convertisseur DC-DC 1.2 kV - 6.6 kV 83 kW dont le circuit circuit MV est immergé dans un fluide diélectrique est notamment construit et opéré à pleine puissance et tension.

Justification d’un réseau de collection MVDC et présentation du cas d’étude

Le producteur d’énergie Compagnie Nationale du Rhône (CNR) souhaite développer des parcs photovoltaïques (PV) linéaires le long de grands axes naturels tels que les fleuves (voir figure ci-dessous). On considérera cet exemple comme base de cas d’étude. Effectivement, du fait des longues distances sur lesquelles s’étend ce type d’installation, un réseau de collection de puissance en MVDC semble intéressant. Cependant, cet intérêt doit être vérifié et quantifié. Dans cette thèse, on se limite à l’analyse en termes de rendement, l’analyse économique étant laissée pour une autre étude.



LE PROJET GRAND LINEAIRE DE CNR : 3 DÉMONSTRATEURS INNOVANTS DEPLOYÉS PAR PALIER POUR RÉPONDRE AUX DEFIS DES GRANDES LONGUEURS

1 - LE PV LINEAIRE BIFACIAL SUR DIGUE À SABLONS

- 350m
- 104kWc
- Panneaux mode paysage
- 2 rangés de 3m40 de haut
- Courant alternatif micro-onduleurs
- Réseau Basse tension

2 - LES PV OMBRIERES DE LA VIARHÔNA

- 1,5km
- 1 MWc
- Panneaux mode toiture
- 1ère expérimentation en courant continu
- Réseau de Distribution
- Mise en service 2023

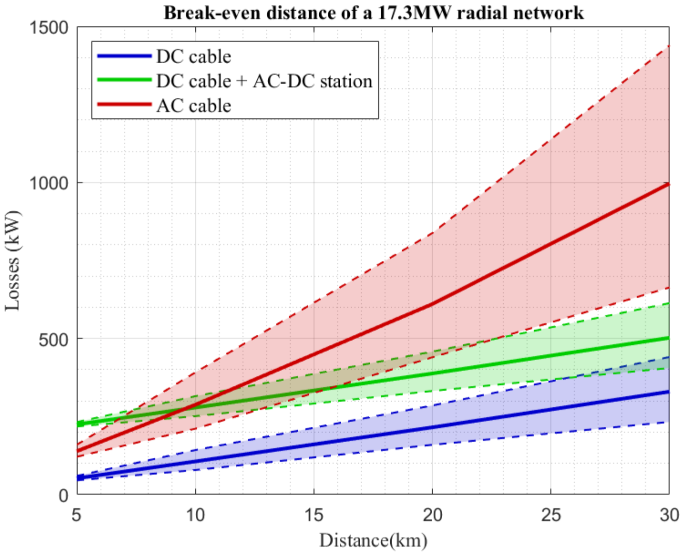
3 - LE PV GRAND LINEAIRE

- 10 à 20 km
- 20 MWc
- 3 modes : paysage + toiture + parement digues ou berges
- Courant continu
- Réseau de Transmission
- Mise en service 2025

Communiqué de presse de CNR détaillant leur plan de développement de parcs PV linéaires

L’étude de la “break-even distance” est réalisée pour un réseau moyenne tension. Cette distance correspond à la limite de longueur du réseau de collection à partir de laquelle les pertes de l’installation complète sont toujours plus faibles pour une architecture DC plutôt que AC. Effectivement les pertes dans le câble sont plus faibles en DC du fait de l’absence du courant associé au transport de la puissance réactive et des effets fréquentiels tels que les effets de peau et proximité. Cependant, un élement de conversion supplémentaire existe en DC (le convertisseur DC-AC connectant le réseau DC au réseau existant AC), ce qui ajoute des pertes dès le kilomètre 0. Trois cas sont étudiés: la connexion point à point, le réseau de collection distribué à puissance constante puis à puissance variable. L’hypothèse principale utilisée pour ces études est l’égalité du rendement des convertisseurs interfaçant les sources de puissance avec le réseau de collection pour les systèmes AC et DC.

Le résultat de l’étude concernant le réseau de collection distribué est montré dans la figure ci-dessous. Afin d’étudier l’effet de la distribution spatiale des sources de puissance, 1000 distributions sont simulées (calcul de load flow) pour une longueur de réseau grandissante. Cela donne naissance à trois “break-even distance” en considérant le cas moyen et les cas extrêmes.

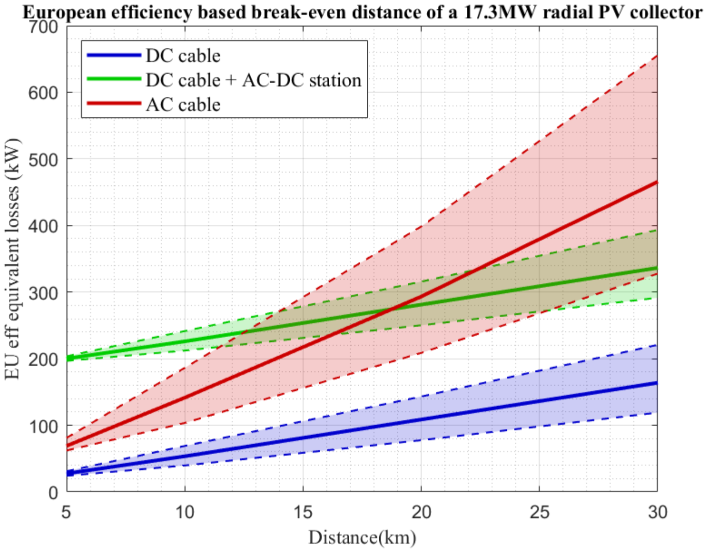


Break-even distance d’un réseau de collection distribué Uac=10 kV Udc=±10kV, 17.3 MW. Les lignes pointillées représentent les distribution extrêmes.

Dans le cas d’un réseau de collection pour parc PV, un puissance constante des sources ne peut pas être considérée raisonnablement. Le « rendement européen » est une moyenne pondérée des rendements d’un système PV à différentes fractions de sa puissance nominale. Ses coefficients proviennent de l’étude statistique des ensoleillements en Europe et cette grandeur est couramment utilisée par les fabricants de systèmes PV.

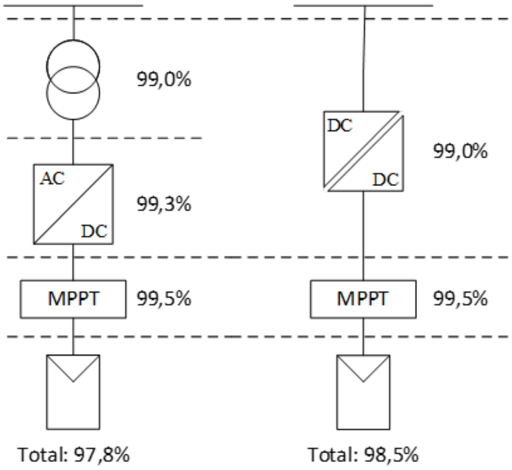
$$\eta_{euro} = 0.03\,\eta_{5\%} + 0.06\,\eta_{10\%} + 0.13\,\eta_{20\%} + 0.1\,\eta_{30\%} + 0.48\,\eta_{50\%} + 0.2\,\eta_{100\%}$$

Il est observé dans la figure ci-dessous que l’utilisation réduite de la ligne due à la variabilité de la puissance éloigne la “break-even distance” et augmente l’effet de la distribution spatiale des sources.



Break-even distance d’un réseau de collection PV distribué Uac=10 kV Udc=±10kV, 17.3 MW installé, puissance variable selon le rendement européen. Les lignes pointillées représentent les distributions spatiales extrêmes.

A partir de ce résultat, il est possible de revenir sur l’hypothèse d’égalité des rendements des convertisseurs d’interface des solutions AC et DC afin de déterminer un rendement objectif du convertisseur DC-DC. La figure ci-dessous donne les rendement objectif pour un « break-even » moyen à 5 km pour un parc PV Udc=±10kV, 17.3 MW.



Comparaison entre la solution de connexion à un réseau de collection MV en AC (gauche) et DC (droite) avec les rendements européens objectifs.

Le cas d’étude utilisé tout au long de cette thèse est présenté sur le schéma ci-dessous, avec les valeurs des paramètres principaux résumées dans le tableau.

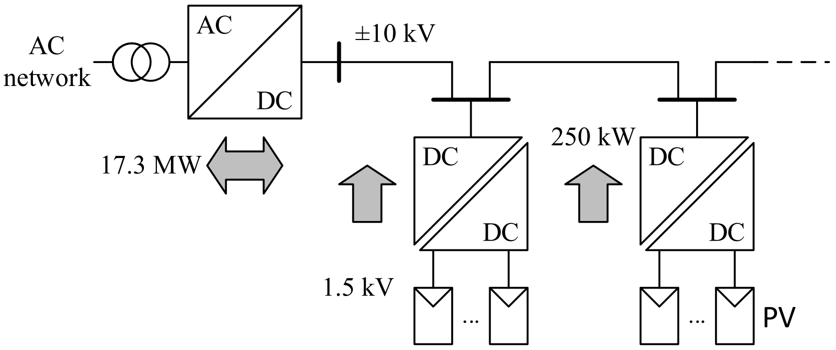


Schéma du parc PV avec réseau de collection MVDC utilisé comme cas d'étude

Parameter	Value
Converter rated power *P*	250 kW (variations from 0 to 1 p.u. following PV mission profile)
PV string voltage V_{PV}	MPP voltage : 900-1100 V ; open circuit : 1500 V
MVDC networkvoltage V_o	20 kV (±10 kV) ±10% nominal (with additional voltage thresholds, see Fig. 2.19)
European efficiency η_{euro}	98.5% (99% for the step-up DC-DC)

Etat de l'art des convertisseurs de puissance

L'étude de la structure des convertisseurs utilisés dans le domaine du PV amène à définir une organisation similaire pour la solution DC. Ainsi le sujet d'étude de la thèse est centré sur le convertisseur DC-DC élévateur encadré en rouge dans le schéma de principe ci-dessous.

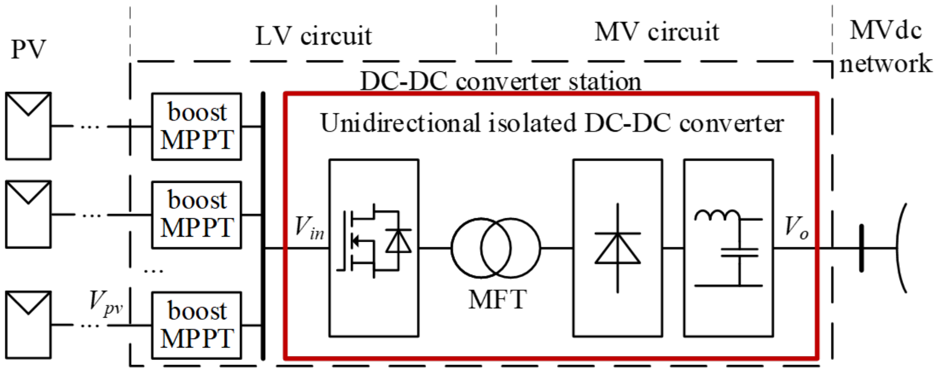
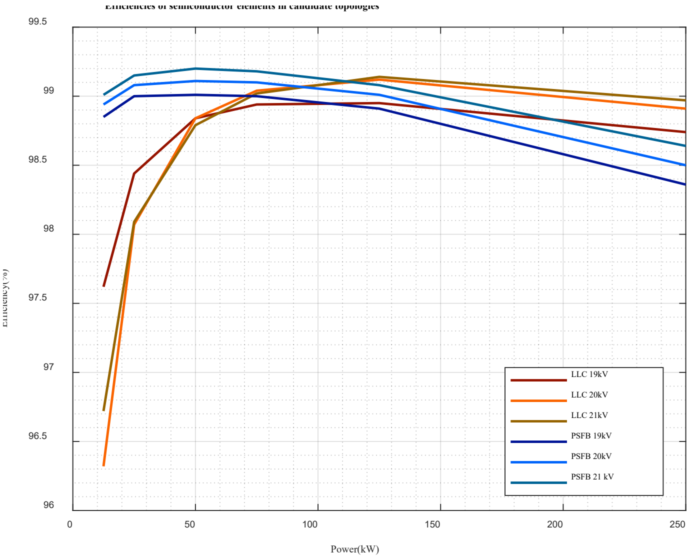


Schéma structurel du convertisseur connectant les groupes PV au réseau MVDC, le sujet de cette thèse étant le convertisseur élévateur encadré en rouge

Un état de l'art des réalisations de convertisseurs DC-DC se connectant à la moyenne tension est résumé dans le tableau ci-dessous. Deux familles de topologies sont identifées : les topologies résonnantes et les topologies basées sur les topologies classiques (Buck, Boost). Les topologies LLC (résonnante) et Phase-Shifted Full Bridge (PSFB) sont sélectionnées pour comparaison de leurs performances dans le contexte du cas d'étude.

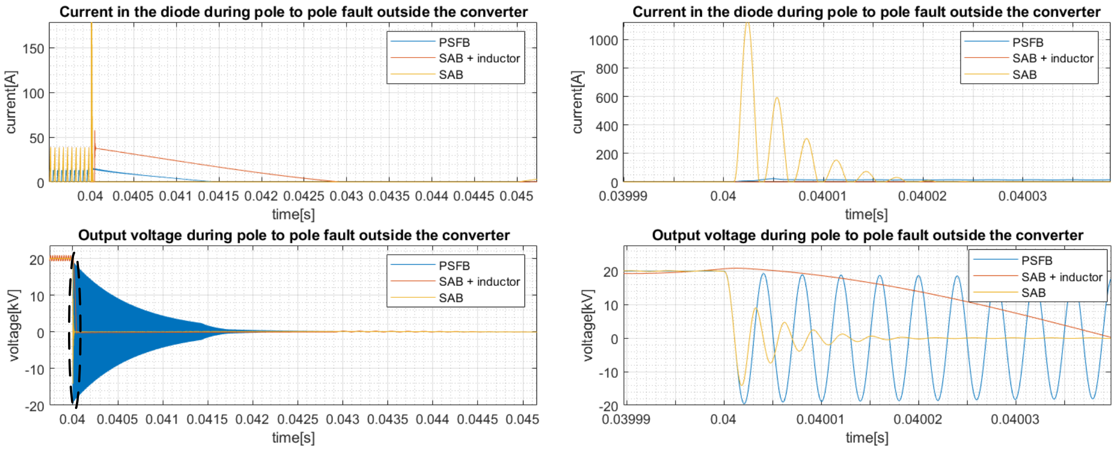
Comparaison des topologies de convertisseurs DC-DC pour l'application PV MVDC

La phase de dimensionnement du LLC montre que les spécifications du cas d'étude, en terme de variation de tension de sortie, amènent à des difficultés pour maintenir la fréquence de découpage dans une plage de variation raisonnable et un contrôle hybride incluant le déphasage entre les bras de l'onduleur doit être mis en place. La figure suivante montre que, malgré un rendement supérieur du LLC à pleine puissance, le PSFB garde un rendement européen similaire. Ceci s'explique par son courant magnétisant inférieur à basse puissance ainsi que les commutations à l'ouverture à quasi zéro courant du fait du fonctionnement en conduction discontinue à ces puissances.



Comparaison des rendement du PSFB et LLC considérant les spécification du cas d'étude

Du fait de l'impossibilité de départager les topologies candidates par leurs rendements, un nouveau facteur est sélectionné. Le convertisseur devant être connecté à un réseau MVDC, la réponse du convertisseur à un défaut sur ce réseau est décisive. On peut voir sur la figure ci-dessous que le filtre *LC* caractérisant le PSFB permet protéger le redresseur de courants destructifs apparaissant avec un simple filtre *C* (le SAB se comportant comme le LLC dans ce cas) dans le cas d'un court-circuit pôle-pôle sur le réseau MVDC.

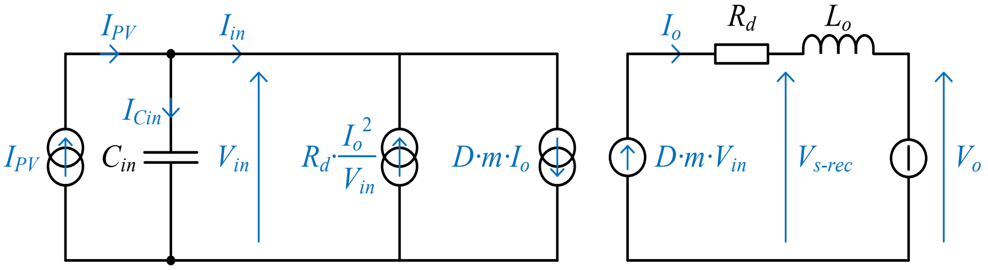


Comparaison des résponses à un court-circuit MVDC des filtres *LC* (PSFB), *CL* (SAB+inductor) et *C* (SAB)

Ainsi, le PSFB est sélectionné comme topologie de base pour les investigations suivantes visant à l'adapter à l'utilisation au cas d'étude de connexion de groupes PV à un réseau MVDC (PV MVDC).

Contrôle du PSFB spécifique à l'application PV MVDC

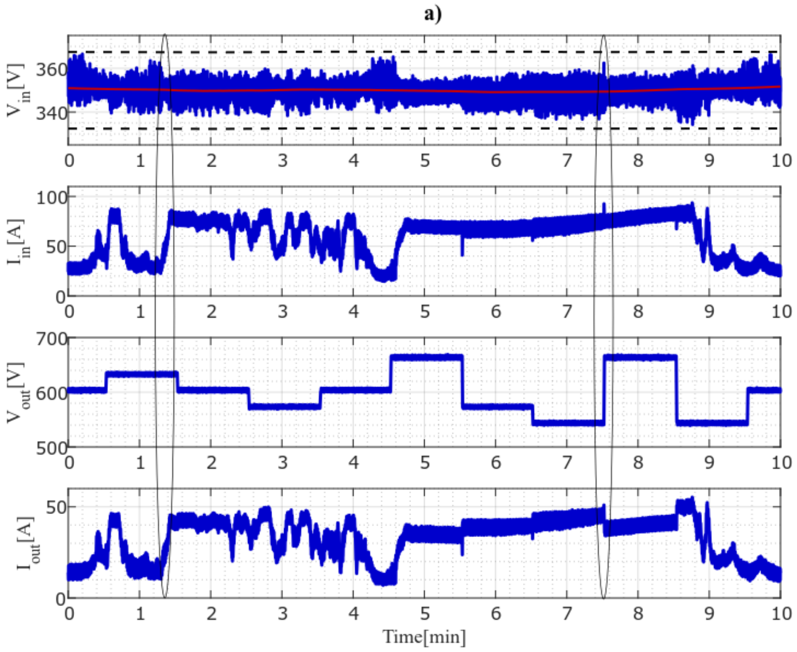
Le PSFB étant historiquement utilisé pour l'alimentation de charges et non pour la connexion de sources à un réseau, son contrôle doit être adapté à cette application. La tension du réseau MVDC étant considérée comme contrôlée par l'onduleur central connectant au réseau AC, le PSFB doit contrôler son bus d'entrée à une tension constante sur laquelle viennent se connecter les multiples convertisseur MPPT. Le modèle moyen et la fonction de transfert permettant de régler un correcteur PI régulant la tension d'entrée sont présentés ci-dessous.



Modèle moyen pour le contrôle de la tension d'entrée du PSFB

$$\frac{\widetilde{V_{in}}(s)}{\widetilde{D}(s)} = \frac{-mV_{in_S}^2\left(mV_{in_S}D_S - R_d I_{o_S} + L_o I_{o_S}\cdot s\right)}{\left(mV_{in_S}D_S - R_d I_{o_S}\right)^2 + R_d\left(C_{in}V_{in_S}^2 + L_o I_{o_S}^2\right)\cdot s + C_I L_o V_{in_S}^2 \cdot s^2}$$

Le contrôle de la tension d'entrée est vérifié expérimentalement sur un PSFB 300 V-600 V 30 kW avec de réelles données d'une installation PV un jour de météo variable.



Validation de la régulation de la tension d'entrée du PSFB face à des variations de puissances, provenant de données de terrain, et de tension de sortie

Design et implémentation d'un redresseur moyenne tension pour le PSFB

La seconde particularité de l'application considérée est le niveau de tension au secondaire du transformateur. Cette thèse propose l'intégration de l'ensemble du circuit MV dans une cuve remplie de liquide diélectrique (qu'on appellera huile), de manière similaire à un transformateur de distribution 50 Hz classique. La cuve contient le transformateur moyenne fréquence, le redresseur moyenne tension et le filtre de sortie.

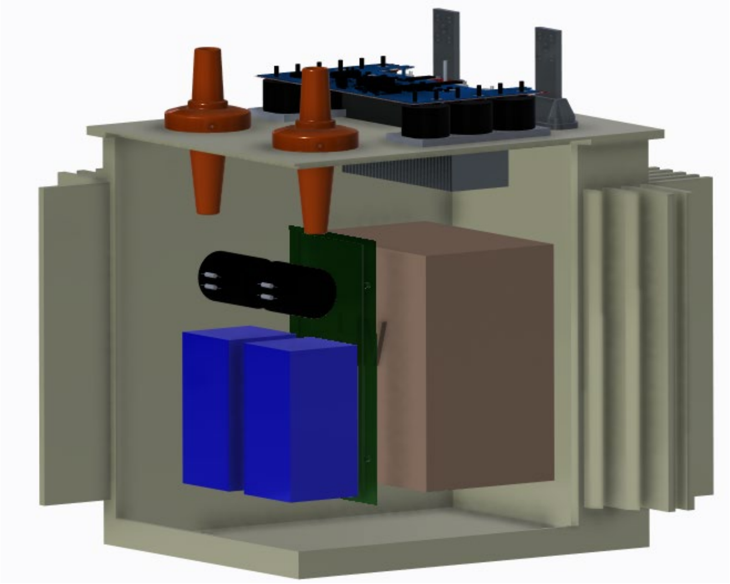
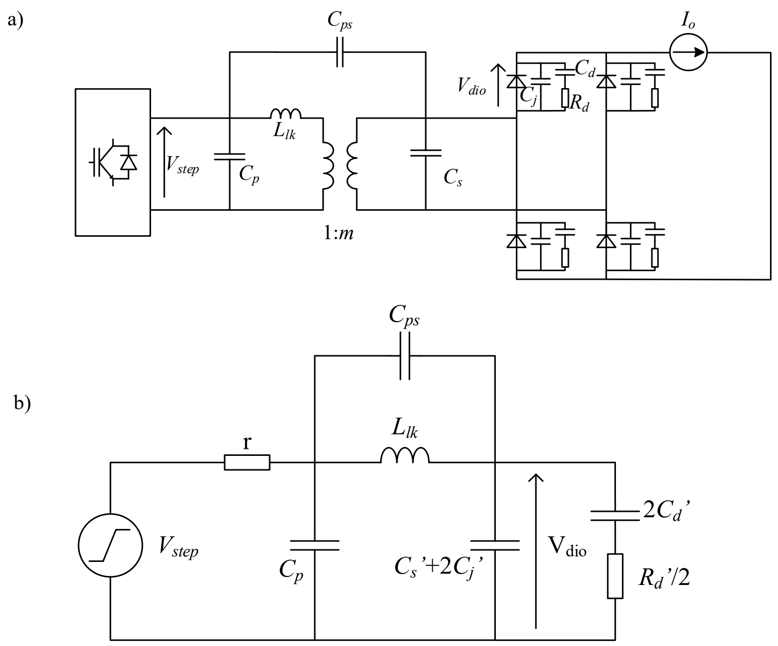


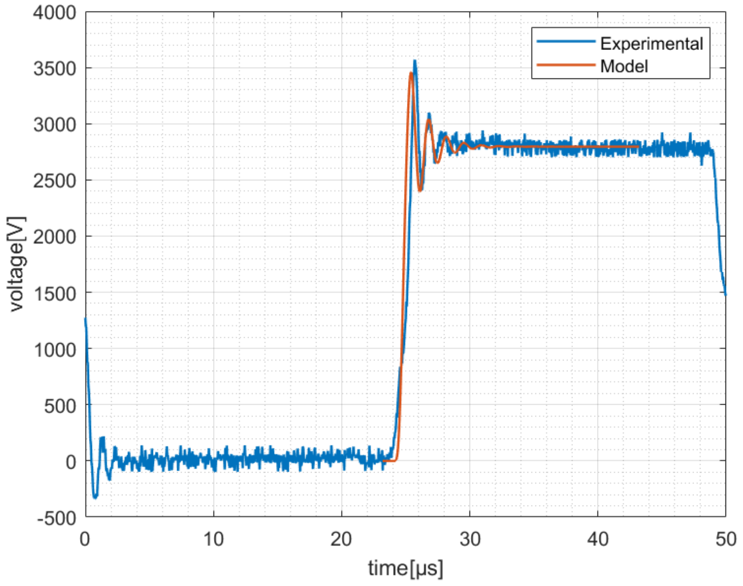
Illustration de la cuve incluant le MFT, redresseur et filtre de sortie, avec l'onduleur posé sur le dessus de la cuve

L'immersion de composants magnétiques dans l'huile étant déjà étudiée dans nombreux autres travaux, on s'intéresse en particulier au design du redresseur dans ce concept. Du fait du faible courant de sortie du convertisseur (12.5 A) et le besoin d'un fort rendement, le redresseur est réalisé par la mise en série de diodes Schottky SiC 1700V. Le dimensionnement du snubber associé à chaque diode doit prendre en compte l'équilibrage dynamique de la tension ainsi que la limitation des surtensions typiques sur le redresseur du PSFB (dues à la présence de l'inductance de sortie, la tension redresseur n'étant pas maintenue à la tension de sortie). Un modèle permettant de simuler ces surtensions, existant dans la littérature, est étendu et amélioré pour prendre en compte la structure de pont complet du redresseur et la vitesse de commutation du pont primaire.



Modèle simplifié permettant de simuler les surtensions à la commutation de la tension redresseur

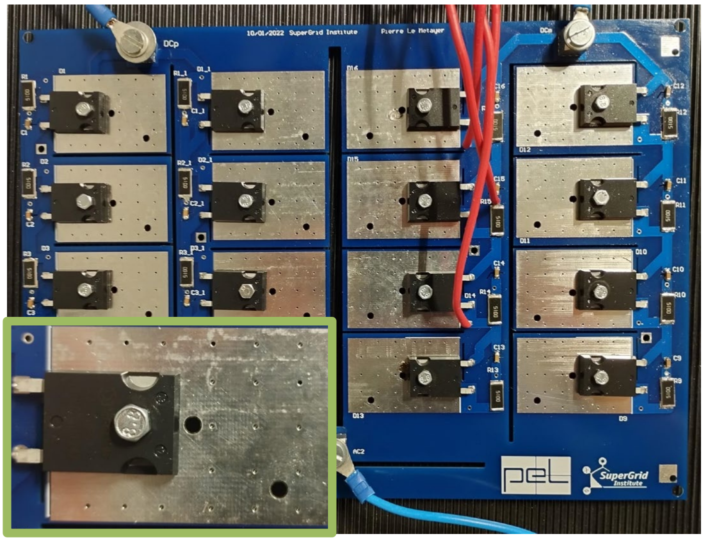
Un redresseur échelle réduite est développé pour une tension de 4 kV. Le résultat du modèle est comparé avec le test, montrant que le pic de la surtension est similaire. Ainsi, le design du snubber peut être réalisé en utilisant ce modèle simplifié.



Comparaison du résultat du modèle simplifié et du test

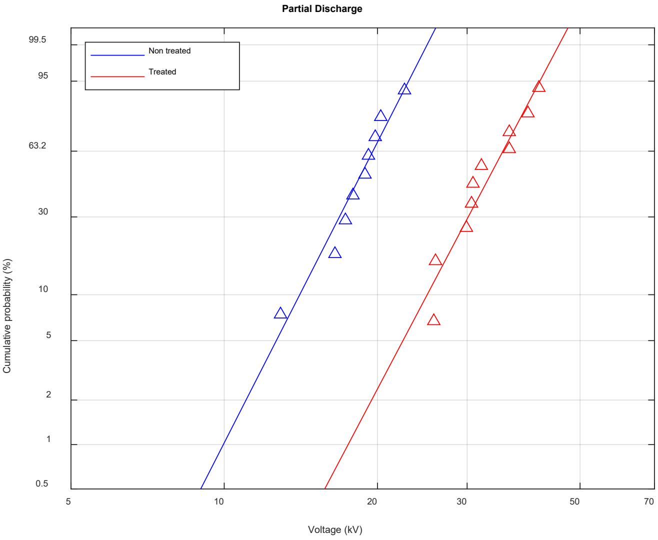
Les particularités du design du redresseur pour l'immersion dans l'huile incluent le refroidissement, le design diélectrique ainsi que la nécessité de compatibilité chimique des composants avec l'huile.

Cette thèse propose de réaliser le refroidissement du PCB redresseur dans l'huile par l'augmentation de la surface d'échange des diodes TO-247 par des patchs de cuivre. Des tests thermiques à courant nominal montrent que le design effectué est même pessimiste car la température de jonctions des diodes reste largement inférieure à la limite de 150°C.



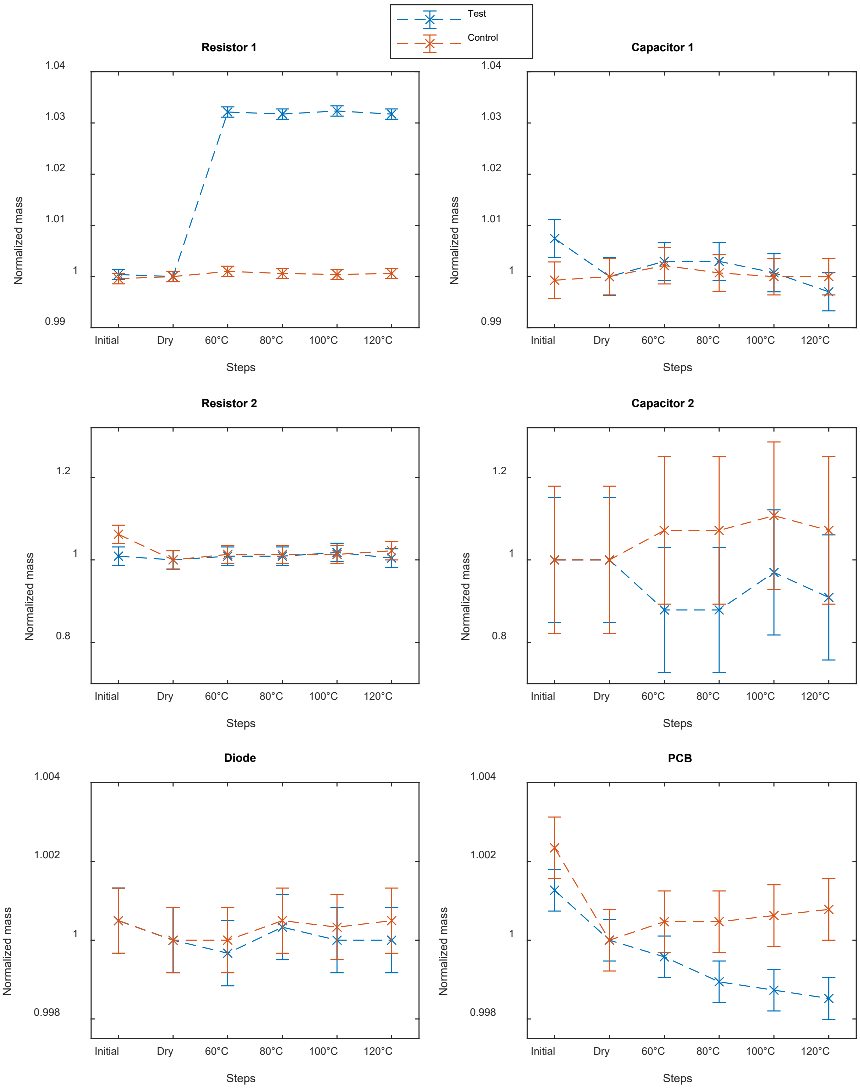
PCB redresseur avec refroidissement des diodes par augmentation de la surface d'échange par patch de cuivre

Les distances minimums entres les différentes pistes du PCB sont définies à partir de tests de claquage et de décharge partielle sur des échantillons de PCB. La règle de design de 3.3 kV/mm est définie pour garantir une probabilité de décharge partielle inférieure à 1% même dans une huile non traitée (voir figure ci-dessous).



Résultats de tests de décharge partielle pour un PCB avec une distance entre pistes de 3mm.

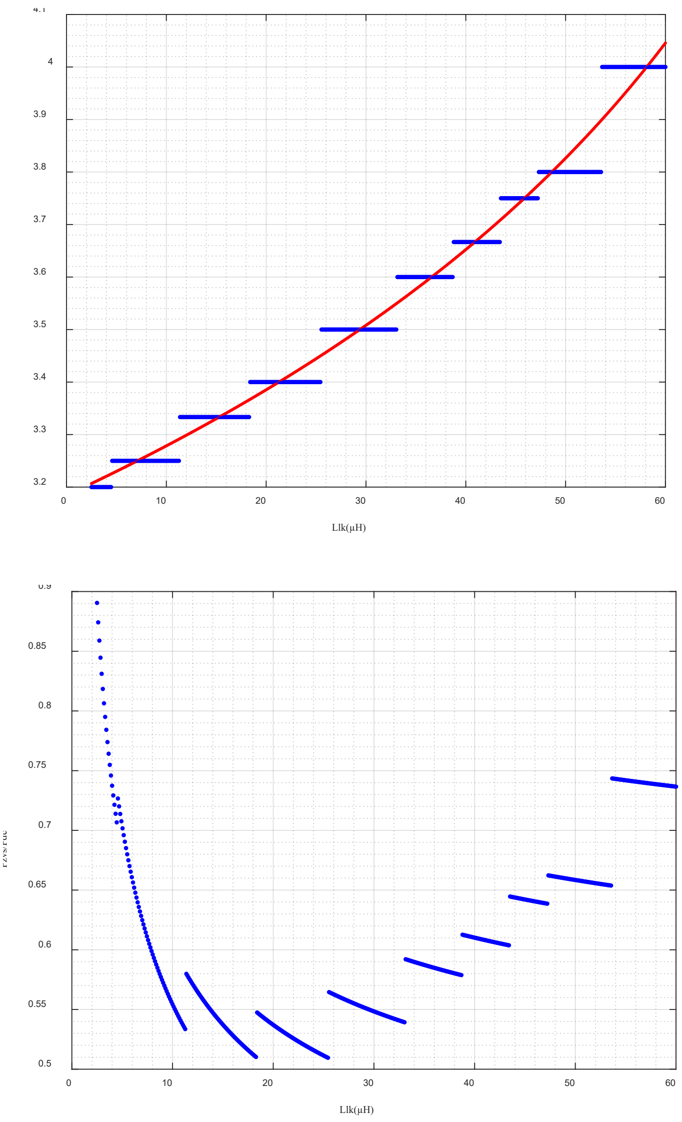
Différentes technologies de composants utilisés dans la réalisation du PCB redresseur sont immergées dans de l'huile et vieillies à différentes températures pour vérifier la compatibilité chimique. La seule interaction d'un composant avec l'huile est observée pour une résistance traversante montrant des signes d'infiltration d'huile. La technologie de composant monté en surface (CMS) est préférée pour l'implémentation du snubber étant donné que ces composants n'ont montrés aucun signe d'interaction avec l'huile.



Evolution de la masse de potentiels composants pour l'implémentation du redresseur durant une procédure de vieillissement dans l'huile

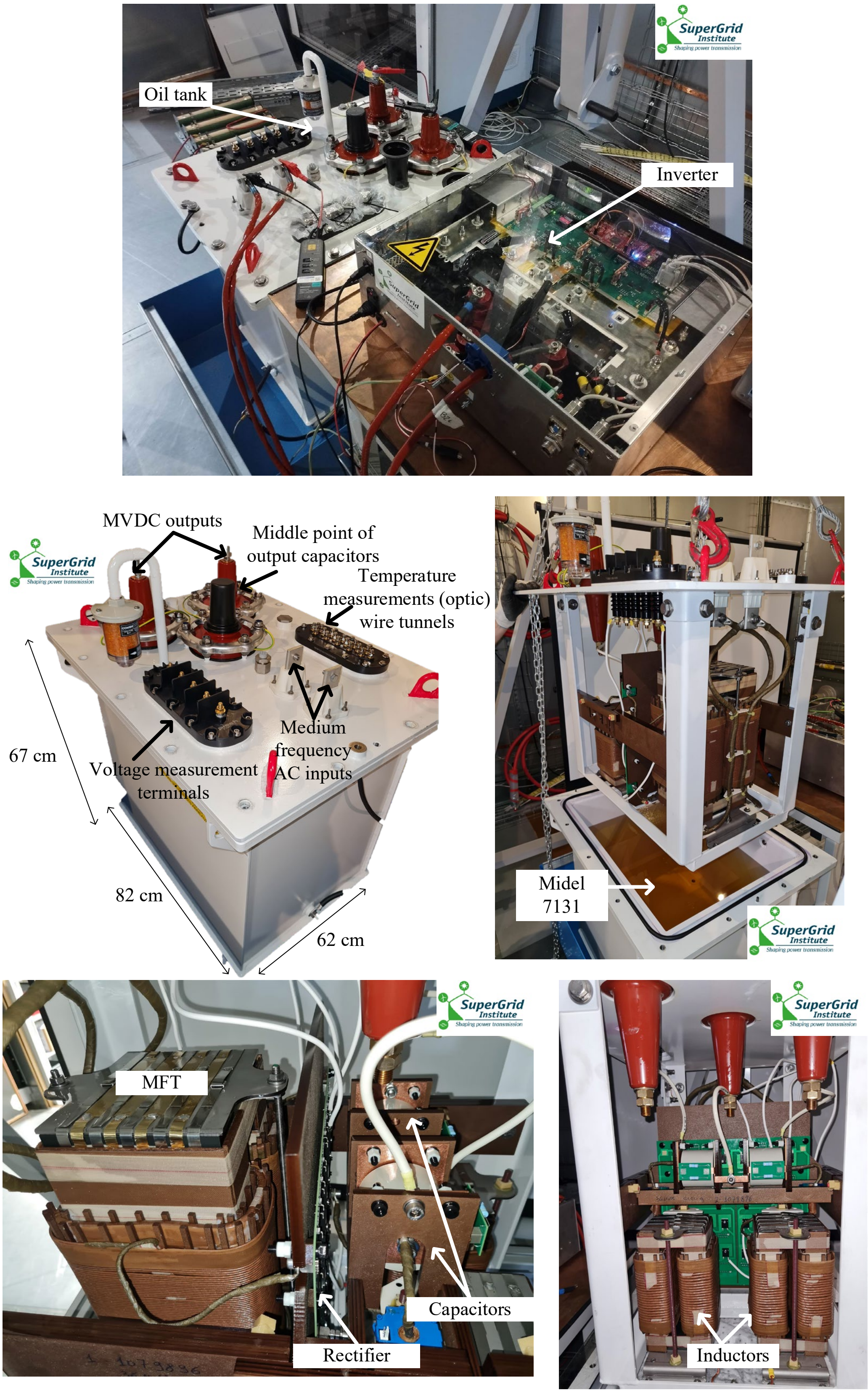
Prototypage d'un convertisseur DC-DC 1.2 kV vers 6.6 kV 83 kW

Le choix des valeurs des composants du circuit du PSFB est mis sous la forme d'un problème d'optimisation cherchant à maximiser le rendement européen de l'onduleur. A partir de ces valeurs, le MFT peut être conçu. Le graphique ci-dessous montre le compromis entre les différents paramètres et la zone de commutation douce complète de l'onduleur.



Compromis entre les différentes valeurs des paramètres du MFT et la zone de commutation douce complète de l'onduleur, en bleu pour des valeurs discrétisées de ratio de tension du MFT pour prendre en compte les aspects de réalisation

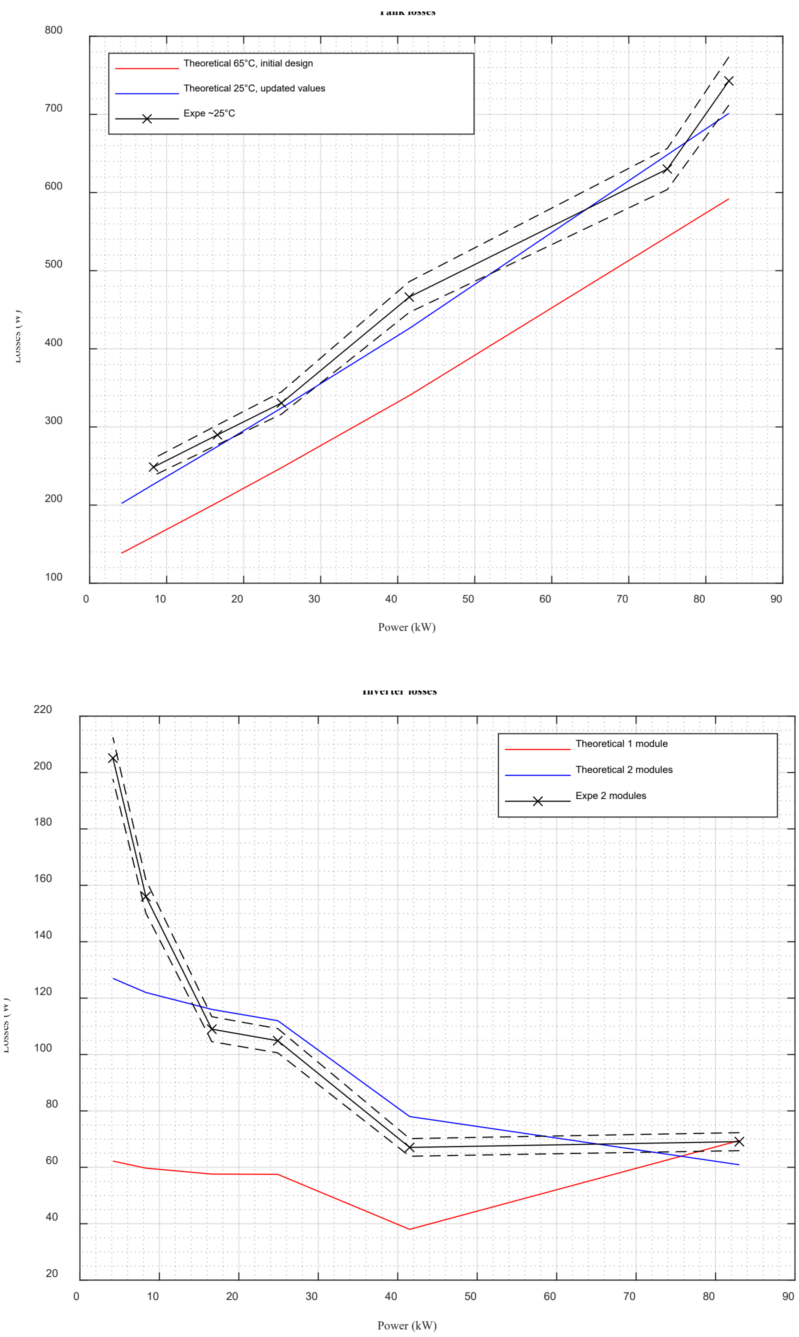
La figure suivante montre l'implémentation d'un prototype 1.2 kV vers 6.6 kV 83 kW utilisant les concepts presentés précédemment. Les tests à pleine tension et puissance sont permis par l'utilisation d'un montage en « back-to-back » avec un deuxième convertisseur réalisant le conversion inverse 6.6 kV vers 1.2 kV, permettant d'alimenter les pertes des convertisseurs uniquement.



Implémentation du prototype de convertisseur DC-DC, haut) onduleur et cuve, milieu) ouverture de la cuve, bas) intérieur de la cuve avec de gauche à droite : MFT, PCB redresseur, condensateurs de sortie et inductances

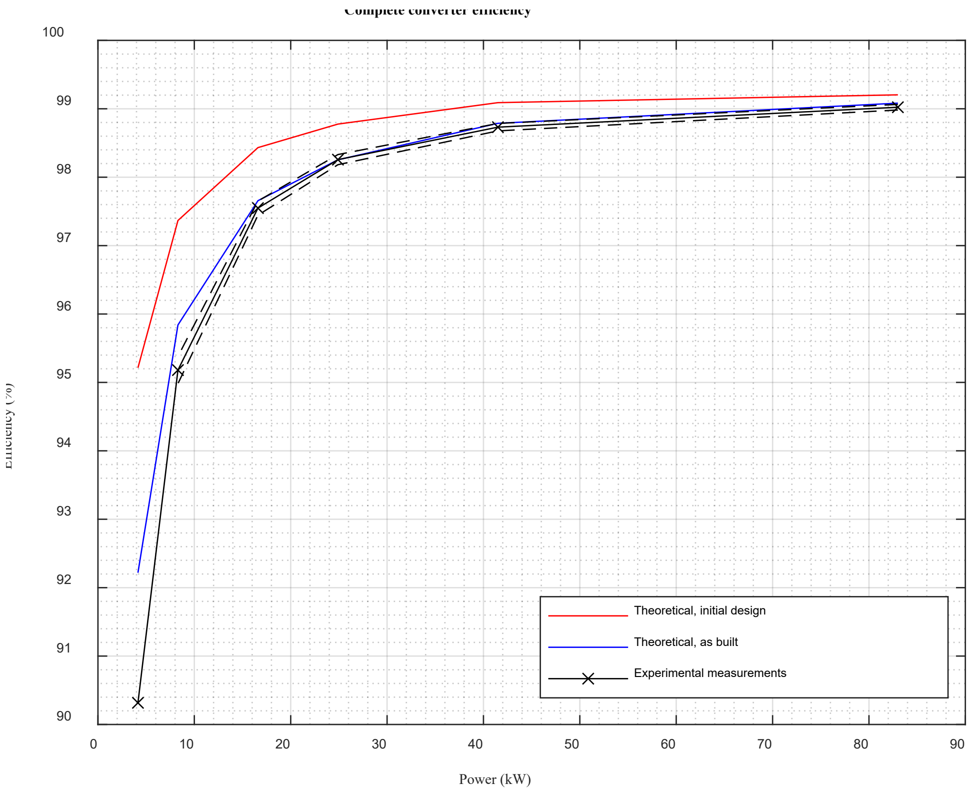
Mesure des pertes par méthode calorimétrique

Etant donné l'importance du rendement pour un tel convertisseur, une mesure électrique n'est pas satisfaisante. Effectivement les incertitudes associées sont de l'ordre de grandeur des pertes (très faibles) que l'on cherche à mesurer. Une méthode de mesure par calorimétrie transitoire dans l'air est sélectionnée dans la littérature et étendue à la mesure de pertes de la cuve à huile. Les résultats sont présentés dans la figure ci-dessous.



Comparaison des pertes mesurées (haut : cuve,bas :onduleur) avec les modèles correspondant au cas idéal (rouge) et aux éléments réellement fabriqués (bleu).

On observe que les mesures de pertes de la cuve suivent très bien le modèle. Pour l'onduleur, un phénomène de commutation parasite du switch opposé lors de la commutation dure d'un MOSFET entraîne des court-circuits partiels menant à des pertes bien plus élevées à basses puissances. Ceci, associé aux non-idéalités de la réalisation des éléments (différences entre courbes rouges et bleues dues notamment à des changement de matériau magnétique lors de la réalisation), mènent à un rendement Européen de 98.27% inférieur à l'objectif initial de 99%. Cependant ces non-idéalités peuvent être corrigées par une fabrication plus contrôlée du MFT et l'utilisation d'un onduleur non surdimensionné. Cela permettrait d'atteindre le rendement Européen de 98.85% correspondant au design initial du convertisseur (la courbe rouge dans la figure ci-dessous).



Comparaison des rendements mesurés (noir) avec les rendements théoriques du design initial (rouge) et du convertisseur implémenté (bleu)

Abstract

Driven by the need to decarbonise energy production, the integration of renewable energy sources into the power grid has become an important topic in modern electrical engineering. The use of medium voltage direct current (MVDC) collection network is currently researched as it is expected to bring higher energy efficiency, among other potential benefits. A missing piece to connect low voltage DC-native renewable energy sources to an MVDC network is the high ratio step-up DC-DC converter. This dissertation focuses on the DC-DC converter for PV application, addressing the range of topics extending from the definition of the requirements that such a DC-DC converter must meet to proposals for hardware implementations that enable it, via the selection of the most suitable topology and the adaptation of its control. A representative scale prototype is designed implemented and tested.

The motivation for an MVDC collection network is studied through the calculation of break-even distances, based on efficiency criteria. It is shown that a break-even distance can be found for MVDC in the 10s of kilometers. It is observed that, in the case of a PV collection network, the distribution of sources and their power variability, moves the break-even distance farther than in the point-to-point case. Based on these results, the European efficiency objective of 99% is set for the step-up DC-DC converter.

The PSFB and LLC DC-DC topologies are selected from a state of the art study for further comparison considering the case study specifications. The comparison of power losses alone is not sufficient as similar European efficiencies are found. The decisive factor is identified as the behaviour of the output filter during MVDC faults. The *LC* output filter of the PSFB proves highly beneficial to the protection of the rectifier circuit which faces destructive current levels with a simple *C* filter as in the LLC.

The PSFB being historically used to supply power to loads (controlling its output voltage), this thesis develops the control functions needed for the case study application. Indeed, the input voltage regulation of PSFB is required, which was not presented in the literature. The average model takes into account the leakage inductance of the transformer which, depending on its values, can have a damping effect on the $C_{in}\,L_o$ resonance. Tuning equations for a PI controller are proposed, considering the cases of damping and no damping. The proposed control is verified experimentally with a 350-600 V 30 kW converter prototype and a real field-measured load profile. A DC Fault Ride Through (FRT) control is also developed enabling the PSFB to continue outputting a close to nominal current during faults, facilitating the MVDC network protection scheme based on fuses.

This thesis proposed to immerse the complete medium voltage circuit of the PSFB in dielectric fluid in order to limit the insulations distance between the different components (MFT, rectifier, inductors and capacitors). In particular, the design of the rectifier is studied through the electrical, thermal, dielectric and chemical aspects. Because of the low output current and high efficiency requirements of the considered application the rectifier is implemented by series connection of discrete 1.7 kV SiC Schottky diodes. The associated snubbers are designed for voltage balancing and limitation of the PSFB rectifier overvoltages. This design is based on a model improved from the literature and verified experimentally on a 4 kV 12.5 A rectifier. The cooling of an oil-immersed PCB rectifier by simple patterned copper patches is proposed and verified experimentally at nominal oil temprerature. Dielectric characterisations of PCB samples is performed in order to define design guidelines for MV PCB rectifiers. The design guideline of 3.3 kV/mm is defined from the 1% probability of Partial Discharge Inception in non treated oil.

The chemical compatibility with the oil of the components used for the rectifier implementation is checked and the conclusion of the preference for SMD components for the snubbers is reached.

A 1.2 kV to 6.6 kV 83 kW prototype is designed and implemented. The converter is composed of two elements: an inverter and an oil-insulated circuit (MFT, rectifier, inductors, capacitors). The choice of the components values is formalised as an optimisation problem aiming at maximising the European efficiency. The converter operation at full power and voltage is performed in a back-to-back configuration with an active load.

The efficiency of the studied converter being one of its most important feature, work on its accurate measurement is performed. As the electrical methods are either not accurate enough or inapplicable in our case, this dissertation focuses on a calorimetric method. Because of the size and important thermal time constant of the prototype, a transient calorimetric method in ambient air is selected from the literature. The extension of the applicability of this method to the measurement of the tank losses is experimentaly demonstrated. The efficiency measurements performed on the final implementation of the converter prototype give an European efficiency of 98.27% (±0.1%). The differences compared to the original target of 99% are explained mainly by two phenomena. The first one is the manufacture of the transformer using a core material different to the planned one. The second one is the use of an oversized inverter (designed for 250 kW) adding large switching losses. However, the good fit with the theoretical values gives confidence that the European efficiency of 98.85% of the initial design can be reached by solving these pratical issues.

Acknowledgment

Contents

Acronyms

AC	Alternating Current
CIGRE	Conseil International des Grands Réseaux Electriques (International council on large electric systems)
DAB	Dual Active Bridge
DC	Direct Current
EMI	Electromagnetic Interference
HV	High Voltage
IGBT	Insulated Gate Bipolar Transistor
LV	Low Voltage
MFT	Medium Frequency Transformer
MMC	Modular Multilevel Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracking
MV	Medium Voltage
PDIV	Partial Discharge Inception Voltage
PSFB	Phase Shifted Full Bridge
PV	Photovoltaic
SAB	Single Active Bridge
SRC	Series Resonant Converter
SST	Solid State Transformer
VSC	Voltage Source Converter
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

1. Introduction

1.1. Context

Driven by the need to decarbonise energy production, the integration of renewable energy sources into the power grid has become an important topic in modern electrical engineering. Because of the low power density of renewable energy sources (compared with conventional fossil or nuclear solutions), a medium-voltage (MV) AC collection network is generally set up, before raising the voltage again at the collection point (to higher MV or HV depending on the total power of the installation) for transmission on the network. This is because the high current at the production origin at low voltage (LV) would result in too high Joule loss should it circulate in lengthy cables along large power plants. This need to step-up the voltage from the production level to a higher distribution level is what has historically made the AC solution the winner of the War of Current [1]. Indeed, even though the DC solution has the advantage of having no frequency related power losses, it was lacking a technical solution to step-up the voltage when the AC solution had the transformer.

It was thus to the author's surprise to find in a book on the applications of electricity [2], that belonged to its great-great-grandfather, the mention of a 22 kV MVDC transimission line connecting the hydroelectric power plant of Saint-Maurice to Lausanne in the 1900s, praising its lower cost compared to an AC solution. The medium voltage was reached by connecting DC machines in series. It is also mentioned the use of coupled DC machines performing an LV to MV step-up (see Fig. 1.1), effectively forming a DC-DC converter. It is however mentioned that only very few manufacturers (Thury in particular) were able to manage the demanding dielectric design and control effort needed for such realisations. This can probably explain the generalisation of the use of the easier to manufacture and operate AC transformer for stepping up the voltage.

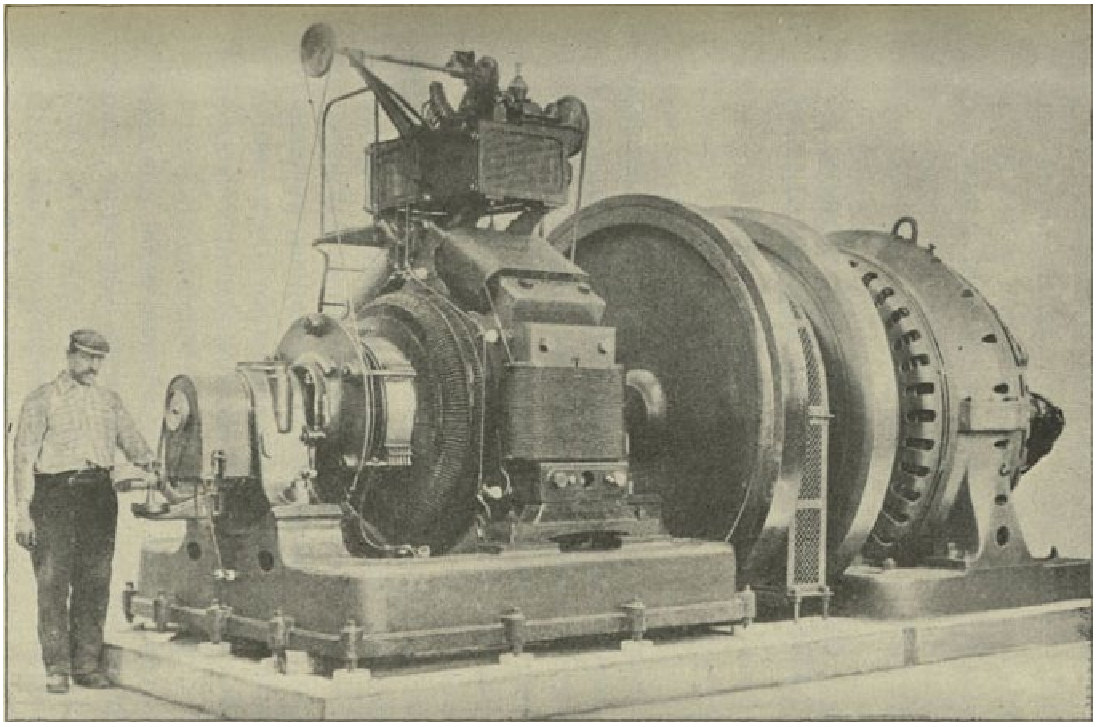


Fig. 1.1. LV/MV DC-DC converter, 120 years in the past [2].

However, DC solutions have not been abandoned completely as current switching components have emerged, enabling the manufacture of "static" (no moving parts) converters.

From mercury-arc valves in 1900, the development of power switches turned to semiconductors in the second part of the 20th century with the thyristors and then the fully-controllable MOSFETs and IGBTs. The use of IGBTs has in particular led to the development of very efficient HV converters (Modular Multilevel Converter) and enabled the use of HVDC for the transport of high power over long distances with low losses.

In the same vein, the use of MVDC is now under study for lower power levels and distances, as in the collection networks needed for the integration of the renewable energy sources. The particularity of renewable energy sources is that their native current form is the DC (directly for PV, after necessary rectification for wind and tidal turbines). This means that the converter necessary to step-up the voltage is a DC-DC converter. Here again this kind of converter is backed-up by an advance of switching technologies. The silicon carbide (SiC) semiconductors development in the 2000s and 2010s has enabled very low switching losses and the use of medium frequency transformers essential to the concept of isolated DC-DC converter.

Fig. 1.2 shows a mapping of applications already using power electronics converters to connect to an MVAC network and which may switch to MVDC. A missing piece for the transition of these applications from AC to DC MV connection is an appropriate DC-DC converter. Indeed, the vast majority of industrial DC-DC converters are used for low voltage applications.

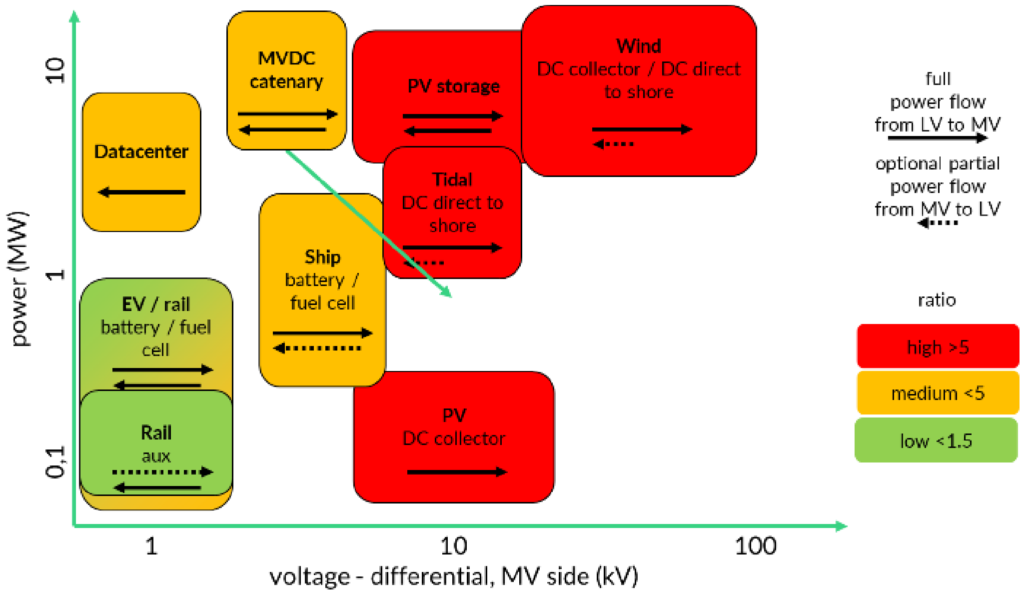


Fig. 1.2. Mapping of potential applications that may required DC-DC converters.

It can be seen in Fig. 1.2 that for renewable applications the main power flow is unidirectional, directed towards the power collection network. As the voltage produced by such sources is initially low (below 1.5 kV) the conversion ratio of the needed DC-DC converter connecting them to an MVDC network is high.

This dissertation focuses on the PV application, addressing the range of topics extending from the definition of the requirements that such a DC-DC converter must meet to proposals for hardware implementations that enable it, via the selection of the most suitable topology and the adaptation of its control. A representative scale prototype is implemented and tested.

1.2. Objectives

The objectives of this doctoral dissertation are the following:

- Assess the relevance of the MVDC collection network for PV power plants.
- Identify and quantify the specifications of a medium voltage DC-DC converter for a PV application.
- Select the best-suited DC-DC converter topology for the case study application.
- Design the selected topology for the optimisation of the efficiency according to the mission profile; specify the requirements of converter components.
- Propose a control scheme that satisfies the PV application and the MVDC network requirements.
- Design the medium frequency and medium voltage SiC diode rectifier in oil, considering electric, dielectric and thermal constraints.
- Design and implement a medium voltage DC-DC converter prototype.
- Accurately measure the efficiency of the DC-DC prototype.

1.3. Scope

Chapter 2 presents the MVDC collection network case study used throughout the thesis. The motivation for such an architecture is depicted through the lense of the study of the MVDC break-even distance.

Chapter 3 presents the state of the art of PV inverters and DC-DC converters. Discussions on the converter directionality and modularity are given. Candidate topologies are selected for comparison.

Chapter 4 compares the candidate topologies in terms of efficiency and fault behaviour. The PSFB topology is selected.

Chapter 5 develops the application-specific control of the selected PSFB topology. Controls suitable in normal and MVDC fault conditions are proposed.

Chapter 6 tackles the implementation challenges of the PSFB for medium voltage. The immersion of the complete MV circuit in dielectric fluid is proposed. The focus is put on the rectifier design.

Chapter 7 presents the design of an 83 kW 1.2 kV to 6.6 kV DC-DC converter prototype.

Chapter 8 verifies experimentally the performance of the prototype. Power losses measurements are performed with a calorimetric method.

Chapter 9 concludes this doctoral dissertation and provides some perspectives for future research.

The document contains 7 appendices.

2. Case study for an MVDC collection network

This chapter presents the case study used throughout the thesis: an MVDC power collection network for large photovoltaic (PV) generation plant. This is inspired by French energy producer Compagnie Nationale du Rhône (CNR) which is planning to develop PV farms [3] along long natural corridors (river, canal). First, the typical architectures of a PV plant are presented. The motivation for an MVDC power collection network is then presented through the general comparison of the power losses in AC and DC equivalent networks. The complexity of the studied network is gradualy increased from a point-to-point link to our case study which consists in a large network of distributed sources injecting variable power levels. Finally, the case study is fully defined and the system variables values are set.

2.1. Collection network architecture for PV

The main architectures for PV farms are divided between two types: string inverter-based and central inverter-based. These two architectures, classicaly based on AC power collection are described here and a DC solution is presented. Similarities and differences between AC and DC solutions are drawn.

2.1.1. String inverter-based architecture

The current typical string inverter-based architecture of a PV plant is presented in Fig. 2.1 [4]. PV panels are grouped in "strings", which are connected to an inverter. Different arrangements of these strings are possible. In Fig. 2.1, the strings are grouped in a subfield before connecting to the inverter. Alternatively, the configuration with one inverter per string is also very common [4].

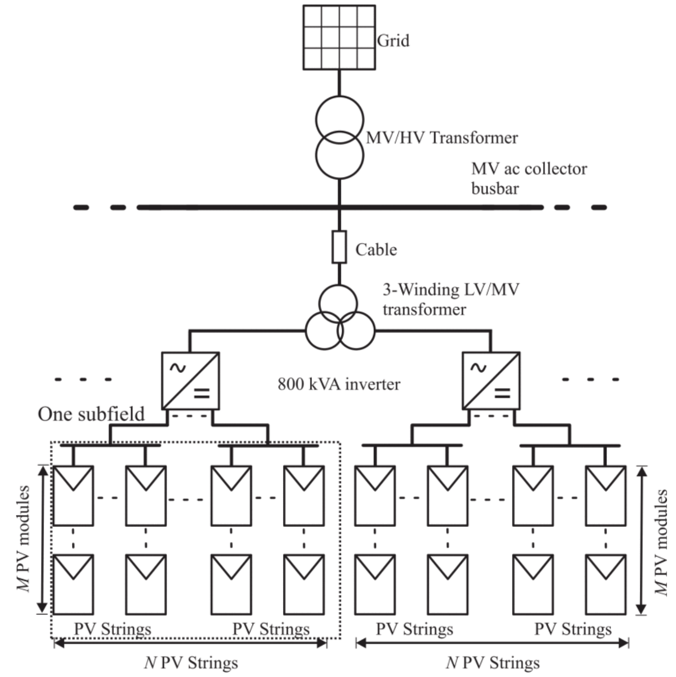


Fig. 2.1. Typical AC PV installation with string inverters [4]

The inverter main role is to convert the DC output of the PV panels to AC. Currently, the highest voltage standard at a PV string output is 1500 Vdc. This means that the output voltage of the PV string is 1500 V when in open circuit (which doesn't happen during power production).

During power production this voltage is controlled to maximize power generation, using a so-called Maximum Power Point Tracking (MPPT) algorithm [5], [6]. A typical voltage range at MPP is 900 V - 1100 V [7]. Multiple inputs are generaly present on such inverters in order to realise MPPT with minimum loss. This is done in order to limit the effects of partial shading of the connected strings on the harvested energy [8]. The impact of this on the converter structure will be discussed in the next chapter.

Typical 1500 Vdc string inverters are rated up to 300 kW with 800 Vac output [9], [10]. The output of the inverter is then connected to a step-up transformer in order to be interfaced to a medium voltage AC power collection network. This network regroups all production units and is then connected to the national grid by the means of a step-up transformer.

Fig. 2.2. String inverter [9] on site

2.1.2. Central inverter-based architecture

The second type of architecture is based on a central inverter and is presented in Fig. 2.3. This is characterised by the use of a single MW-level inverter for the complete plant. However the role of the inverter is the same as the one presented in the previous section about string-inverter based architectures.

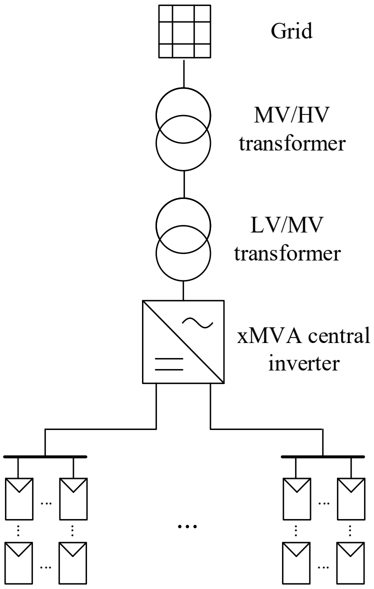


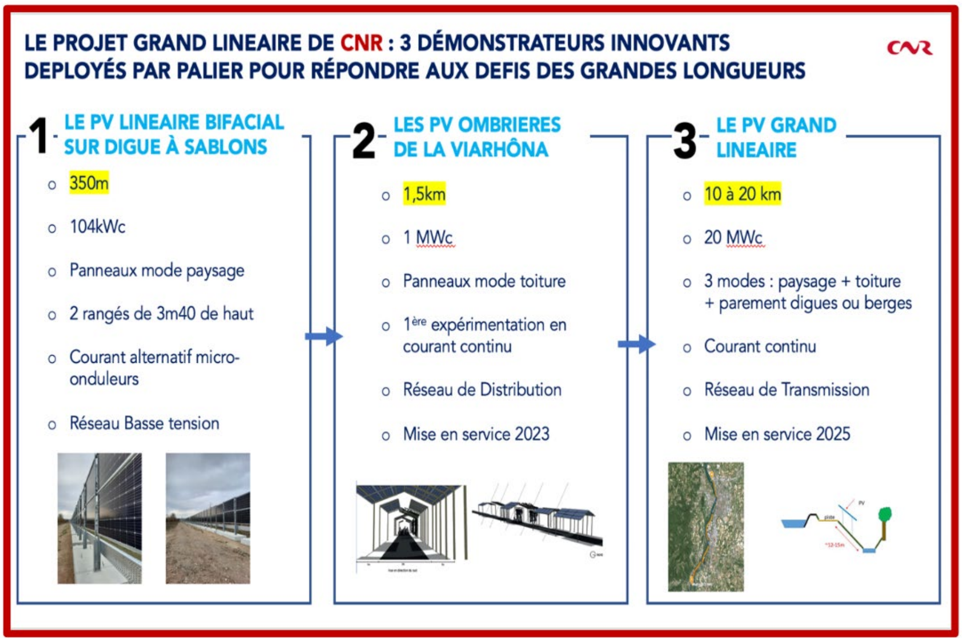
Fig. 2.3. Typical AC PV installation with a central inverter

The inverter usually comes in cabinets and is directly connected to the AC grid by the step-up transformer (Fig. 2.4). In this architecture there is no intermediate MVAC collection network and all of the power collection is realised at the LVDC level. One can understand that this architecture is mostly adapted for compact plants where the power is not collected over long distances at low voltage. A low number of MPPT inputs (commonly even just one) is usually present. This simplifies the converter structure and increases its efficiency but also reduces the harvested energy. The logic behind this choice is that above a certain power level it is advantageous not to try to harvest more energy but to try to deliver the most of it to the grid (having low converter power losses).

Fig. 2.4. Central inverter on site [11]

2.1.3. MVDC solution

Moving from traditional MVAC to MVDC collection networks has been investigated in several articles [4], [12]. The main advantage is the reduction of losses in the MV cables in DC [1]. This advantage is particularly visible in underground cables which are often used in new installations for aesthetic reasons. The French energy producer Compagnie Nationale du Rhône (CNR) aims to develop PV plants in linear fashion along the Rhône river, over tens of kilometres [3]. Following the previously given argument, CNR is looking at MVDC as a way to reduce the losses in the long cables of the collector network.



LE PROJET GRAND LINEAIRE DE CNR : 3 DÉMONSTRATEURS INNOVANTS DEPLOYÉS PAR PALIER POUR RÉPONDRE AUX DEFIS DES GRANDES LONGUEURS

1 - LE PV LINEAIRE BIFACIAL SUR DIGUE À SABLONS

- 350m
- 104kWc
- Panneaux mode paysage
- 2 rangés de 3m40 de haut
- Courant alternatif micro-onduleurs
- Réseau Basse tension

2 - LES PV OMBRIERES DE LA VIARHÔNA

- 1,5km
- 1 MWc
- Panneaux mode toiture
- 1$^{\text{ère}}$ expérimentation en courant continu
- Réseau de Distribution
- Mise en service 2023

3 - LE PV GRAND LINEAIRE

- 10 à 20 km
- 20 MWc
- 3 modes : paysage + toiture + parement digues ou berges
- Courant continu
- Réseau de Transmission
- Mise en service 2025

Fig. 2.5. CNR press release on their plan for linear PV plants [3]

A collection network as illustrated in the third part of Fig. 2.5 is represented in Fig. 2.6. It has a similar structure as the one in Fig. 2.1, only with an MVDC collector network. In this configuration the PV strings are not grouped again in subfields before being interfaced to the collection network. This makes sense, considering the linear aspect of the plant. Indeed, grouping enough panels for a for example 800 kW subfield (as in Fig. 2.1) would translate into long distances at the low voltage level and hence high power losses. The couple "inverter+transformer" previously realising the voltage step-up is now replaced by a DC-DC converter interfacing the low voltage DC of the PV strings to the MVDC collector network. The other difference with the AC collector is the need for a large inverter (rated for the complete installation power) at the end of the DC collector line to connect it to the national HVAC grid.

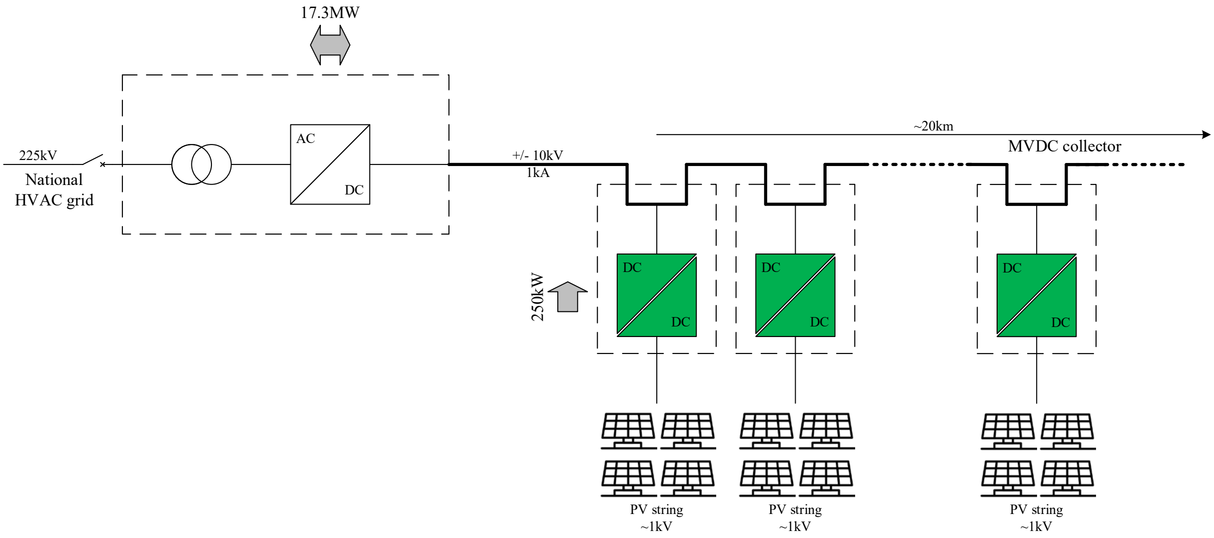


Fig. 2.6. MVDC linear PV collection network

General equivalences can be drawn between state-of-the-art MVAC installations and the MVDC ones, as shown in Fig. 2.7. The string inverters of the MVAC solution can be seen in the MVDC case as merged together into a single, centralised inverter which ensures connection to the existing AC grid. The voltage step-up function of the 50 Hz AC string transformer is performed by the DC-DC converter.

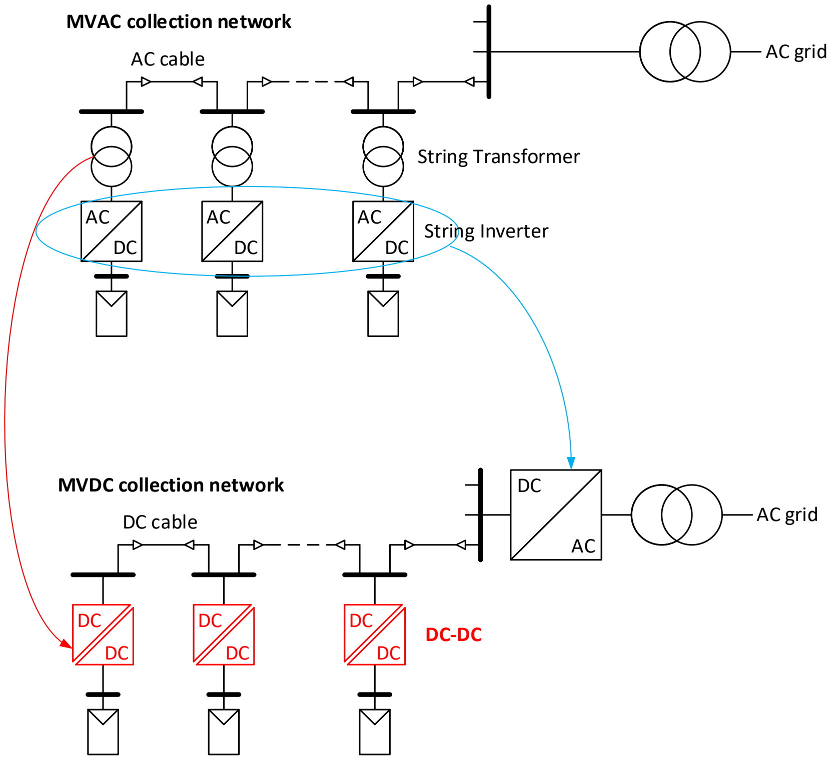


Fig. 2.7. PV MVAC vs. MVDC power collection network diagram

In the following section, the motivation for an MVDC collection network is presented through the general comparison of the power losses in AC and DC equivalent collection networks. The complexity of the studied network is gradualy increased from a point-to-point link to a power collection network with distributed generation.

2.2. Motivation for DC collection: study of MVDC break-even distances

The criteria for an application to switch to DC will strongly depend on a cost-benefit analysis. One of the important performance indicators is the energy efficiency which is a component of the operational expenditure (OPEX). Power losses in DC cables are lower than in AC cables, as there is no circulation of reactive current in DC and therefore no corresponding joule losses in the conductors. However, considering that the DC system has to be connected at some point to an existing AC system, a DC-AC converter station is required. This station comes at a given cost and adds power losses. For high voltage links, it has been demonstrated that a break-even distance exists, where HVDC becomes advantageous over HVAC. The HVDC/HVAC break-even-distance is approximately 50 km in case of submarine cables [13]. The equivalent for medium voltage is not available in the literature as MVDC grids are not yet a commercial and industrial reality.

In this section, an MVDC/MVAC break-even distance is calculated according to the overall energy efficiency criteria. The power losses in underground cables and DC-AC converter stations are considered, assuming some hypotheses, in particular regarding the equivalent voltage and power between AC and DC. This study strictly focuses on the efficiency criteria, as accurate cost estimations are not within the scope of the author’s work.

Three case studies are presented (Fig. 2.8). The first one is a point-to-point transmission, which is the simplest electrical circuit. The second one is a radial distribution network, a common type of network in today's grid. The third one is a collection network for a large PV installation, to give an example of a network with a particular production profile.

The novel aspects of this work are as follows:

- The calculation of break-even distances for MVDC, with clear underlying hypotheses,
- The study of the effect of the power repartition on the break-even distance in a multi-terminal network,
- The study of the effect of the production profile on the break-even distance.

This study resulted in a publication in [14].

2.2.1. Methodology

The DC electricity networks are expected to develop in parallel to AC networks following similar principles. The elementary electricity interconnection unit is the point-to-point (P2P) transmission line and it can be realised in AC or DC as presented in Fig. 2.8 a). In the current AC grid, a distribution network is commonly realised as a ring (closed through external networks 1 and 2) where the individual loads are supplied from a ring main unit (RMU) [15]. A normally open point (NOP) separates the system into two radial networks as presented in Fig. 2.8 b). The NOP can be moved after a fault on one end of the ring, so RMUs can be connected to the other end. The same ring network architecture can be considered for the collection network of renewable energy sources such as PV or wind.

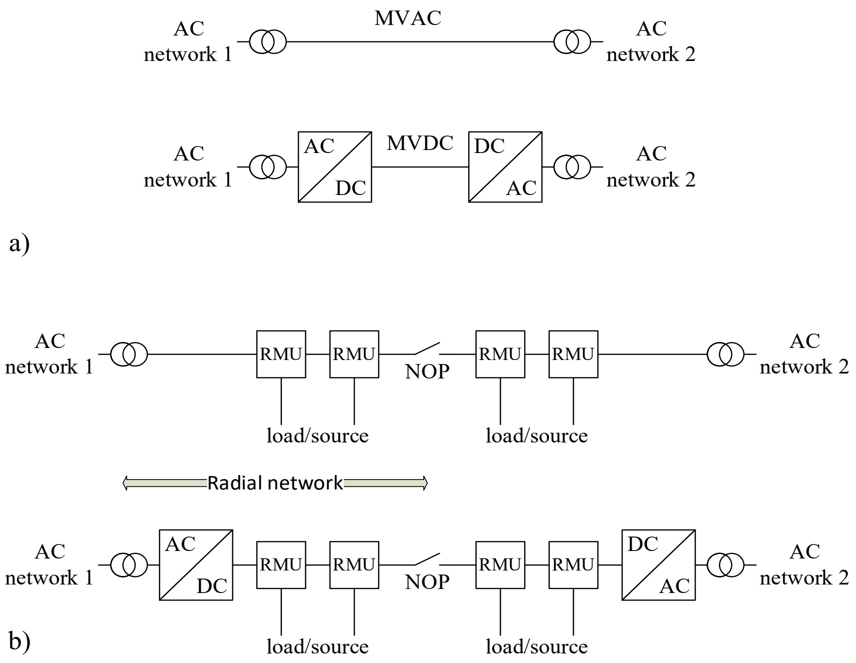


Fig. 2.8. Studied architectures in MVAC and MVDC: a) point-to-point transmission; b) distribution/collection ring network (two radial networks)

A symmetric monopole line configuration with high impedance grounding is selected for the MVDC line. It offers a good robustness to fault events while reducing isolation constraints compared to asymmetric monople configurations. Considering voltage source converter (VSC) AC-DC stations with sinusoidal pulse width modulation, the MVDC voltage is defined as:

$$U_{DC} > 2\sqrt{\frac{2}{3}}U_{AC} \approx 1.6U_{AC} \tag{2.1}$$

where U_{DC} is the DC pole-pole voltage and U_{AC} is the 3-phase AC line-line RMS voltage. Then, for the comparative analysis of AC and DC, the transmission voltages equivalence between both options can be assumed to be described by equation (2.1). A complementary approach to define the equivalence on voltages is to consider the DC voltage that a cable insulation can withstand compared to its AC ratings. In [16] a 12/20 kV MVAC cable was reported to pass a 55 kV DC test. The conclusion of the Cigre working group on MVDC networks [12] is that MVAC cables rated for X kV AC nominal voltage are recommended for ±X kV DC. This recommendation is followed for the choice of the voltage levels.

The comparative analysis of power losses takes into account the cable and AC-DC stations. Other elements of the network are not considered in this analysis: in particular, the transformers (Fig. 2.8) are assumed to have the same efficiency in both AC and DC systems. The same cables are considered for the DC and AC lines assuming that the MVDC market demand will not allow for the development of specific technology in the short term. One should note that three conductors are used in AC systems while only two are used in DC. This fact should be taken into account when analysing the cost. The cable parameters are presented in Table 2.1, according to [17]. For both AC and DC, single-core, unarmoured copper cables are considered. For the AC case the resistance is calculated taking into account the skin effect [18]. The cable temperature is assumed to be 70°C. Cable losses are evaluated based on load flow analysis [19].

Table 2.1. Cable parameters

Network nominal voltage	**Cable rating**	**Section [mm²]**	**DC resistance @ 20°C [Ω/km]**	**DC resistance @ 70°C [Ω/km]**	**AC resistance @ 70°C [Ω/km]**	**Inductance [mH/km]**	**Capacitance [µF/km]**	**Capacitive current [A/km]**
10 kVac/ ±10kVdc	12 kV	1000	0.0176	0.0211	0.0273	0.268	0.904	1.80
20 kVac/ ±20kVdc	22 kV	1000	0.0176	0.0211	0.0273	0.283	0.584	2.33
33 kVac/ ±33kVdc	36 kV	1000	0.0176	0.0211	0.0273	0.290	0.380	2.52

The nominal power of the network for each voltage level is calculated according to the maximum cable current. In this analysis a value of I_{max} = 1 kA is retained. The value of 1 A/mm^2 is a typical current density according to the Nexans cable catalogue [17]. Therefore, the nominal power is calculated as the minimal power between DC and AC transmission that gives the maximal current per cable as expressed in equation (2.2). Table 2.2 presents the nominal power obtained for each voltage level.

$$P_{nom} = min\left(\sqrt{3}U_{AC}I_{max}, U_{DC}I_{max}\right) \tag{2.2}$$

Table 2.2. Nominal power at different voltages

U_{AC}	$U_{DC}/2$	P_{nom}
10 kV	±10 kV	17.3 MW
20 kV	±20 kV	34.6 MW
33 kV	±33 kV	57.2 MW

The AC-DC stations are only required in the MVDC systems. The efficiency of each AC-DC station is assumed according to [20]; the reported efficiency of the studied 24 MW 3-level neutral point clamped (NPC) inverter based on IGCT is approximately 99.1% at low fractions of the nominal power. In this section a constant efficiency of 99% is considered in the entire power range of the AC-DC converter stations.

In the distribution or collection network, if the load or the energy source requires a power conversion equipment then it is assumed that this equipment has the same efficiency in both AC and DC. For example, considering a PV source, the PV inverter and transformer required for a MVAC network is assumed to have the same efficiency as the step-up DC-DC converter needed for the MVDC network.

2.2.2. Case 1: Point-to-point transmission

In this section the break-even distance for a point-to-point transmission is studied. In order to calculate it, the power losses in the cables are calculated for the different MV voltage levels defined in Table 2.2.

The power losses are calculated for different distances using the nominal power defined for each voltage level (Table 2.2) and cable parameters (Table 2.1). The results are presented in Fig. 2.9. The figure shows the losses obtained in the cable for the AC and DC interconnection, as well as the total losses for the DC case if the AC-DC station losses are included. In this case, two AC-DC stations are considered, one at each side of the interconnection, which increases losses by 2 percentage points.

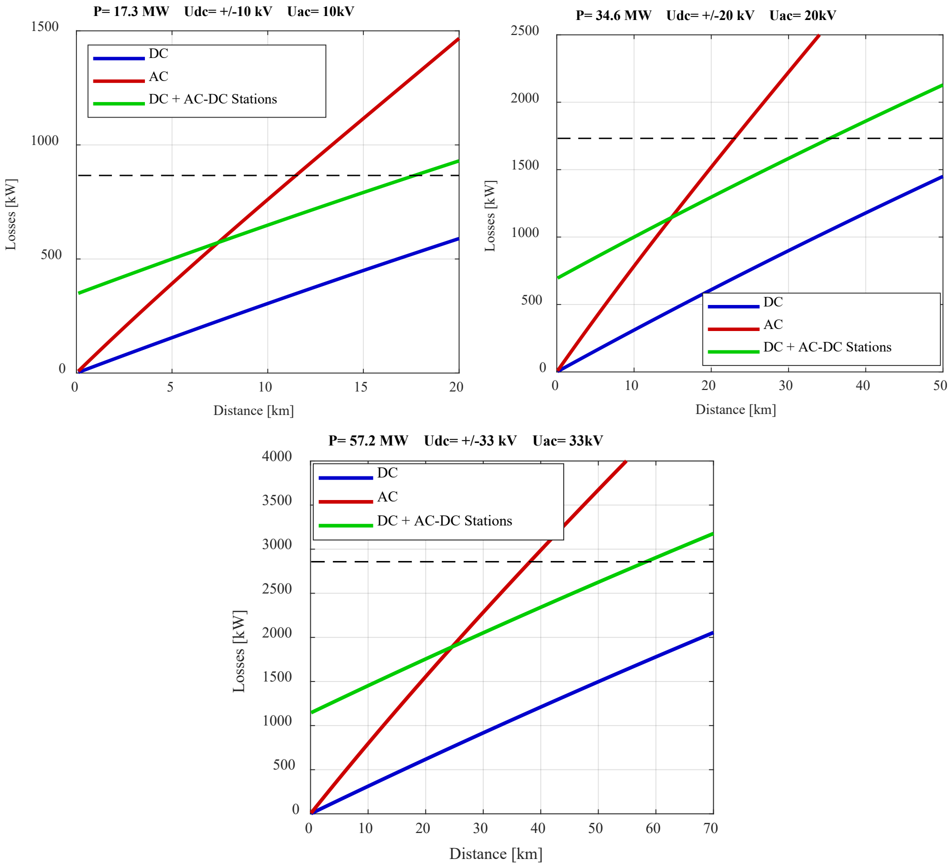


Fig. 2.9. Power losses in function of the distance for the point-to-point transmission at 3 different voltages. The dashed black line represents 5% of losses related to the nominal power.

For all the distances, cable losses are the lowest in the DC configuration. However, because the of the added losses of the AC-DC stations, the overall losses in the DC installations are higher for distances shorter than the break-even distance (crossing point of red and green curves in the figure). From this point, losses are lower in DC than in AC. It can be observed that the break-even distance changes with the voltage level: as the voltage increases, the break-even distance shifts to longer distances.

The dashed black line in the figure represents 5% of losses related to the nominal power on each case. This line is shown as reference and gives an idea of the maximum allowed distance for each configuration in terms of losses. From this point, changing to a higher voltage level could be interesting to decrease the losses to an acceptable value. The limit of 5% is given as reference but another limit could be taken from a technical and economic analysis.

The results of Fig. 2.9 were obtained at the nominal power of the line. However, according to the application, it could be expected that the line does not operate at nominal power all the time. This is the case when interconnecting renewable sources for example. Then, it is worth to analyse the losses for a fixed distance as a function of power. Fig. 2.10 shows the results of this analysis for a given case. For low power loads, the AC configuration has less losses than the DC option. However, from a *break-even power* point, the losses on the DC installation are less than in AC. Therefore, the load profile of the must also be considered when comparing DC and AC transmission. It is observed that the *break-even power* changes according to the length of the line.

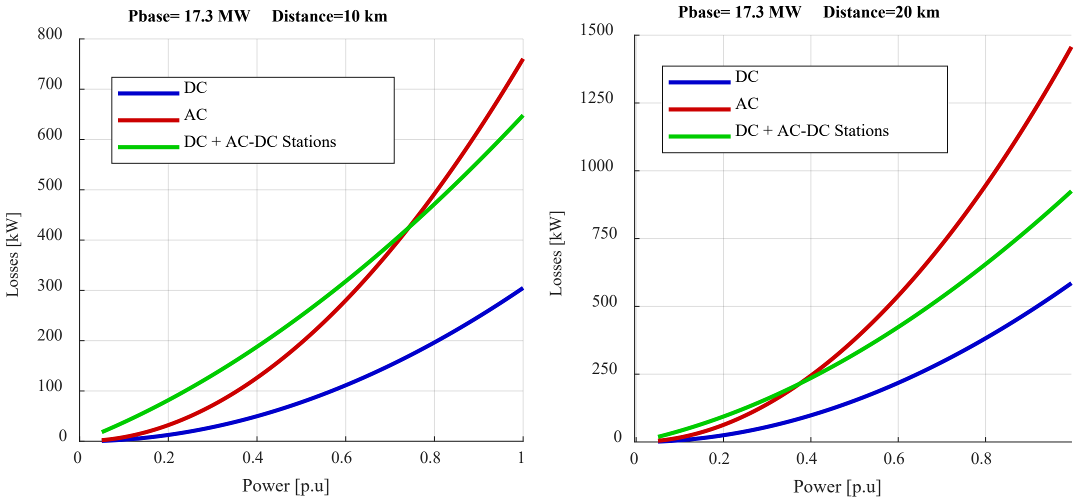


Fig. 2.10. Power losses in function of the power for the point-to-point transmission at fixed distances for the voltage level of 10 kVac / ±10 kVdc.

Fig. 2.11 shows the break-even distance and break-even power for each voltage level. The curves represent the distances and powers where the losses of the point to point transmission are the same for AC and DC. The area above each break-even curve (dashed zone) represents the zone where DC transmission gives lower losses. The area below each curve (coloured zone) represents the zone where AC transmission gives lower losses. The dashed lines for each case represent the limits of the transmission scheme. The maximal power is given for the maximal current allowed on the cable (1 kA is considered), and the maximal distances are given by a limit of 5% of losses. Above these limits the transmission should be done at a higher voltage level.

It can be observed that as the power decreases, the transmission distances and the break-even distance increase. At low power the trend for the break-even curve is inversed. This is due to the predominant influence of the capacitive current in the cable (see Table 2.1): in AC transmission at low power and long distance, the capacitive current can be of the same order of magnitude as the active current, which increases the Joule power loss in the conductors.

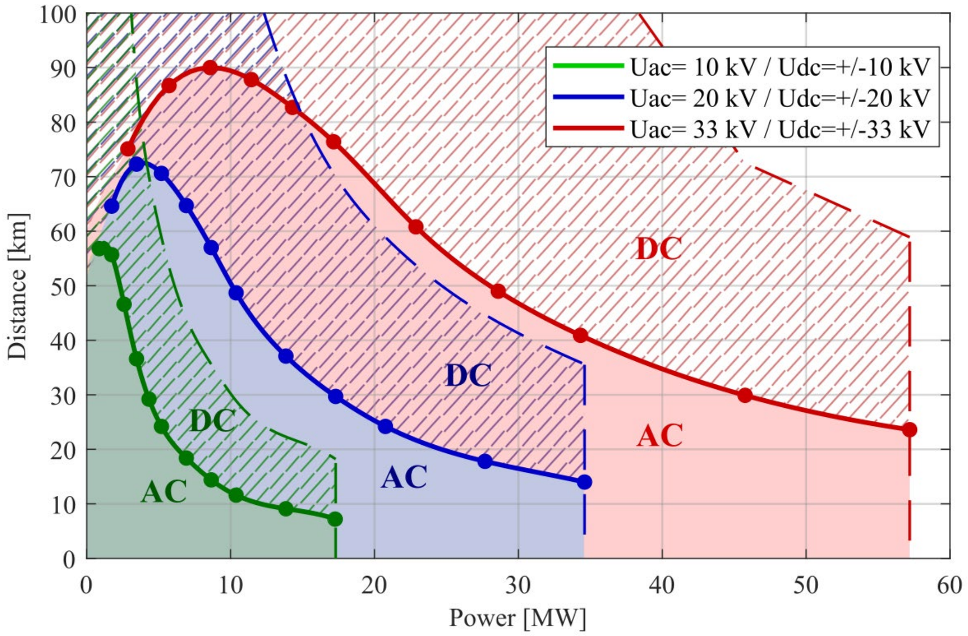


Fig. 2.11. Break-even distance and power of point to point transmission in terms of losses for different voltage levels.

2.2.3. Case 2: Distribution network at constant load

The radial distribution network differs from the previous case of point-to-point transmission by the fact that the total power of the installation does not transit through the total length of the cable. Indeed, for a radial network, the power in the cable decreases at each RMU to reach its minimum in the last segment of the cable. This means that the losses in the cables of a radial network, of total power *P,* distributed along a distance *d,* will be lower than its point-to-point counterpart. Contrary to the point-to-point configuration the distribution of loads along the line matters in the resulting power losses.

In this section, only the 10 kV 17.3 MW configuration from

Table 2.2 is studied. The power of a load P_{RMU} is fixed to 250 kW, giving in total 69 power loads. A constant power load is considered. In order to have representative values, a stochastic approach is taken. 1000 random distributions along increasing distances are generated while keeping a condition of minimum distance of 60 m between two RMUs. This is simply to take into account the fact that load/sources are not point-like (considering a PV power source, the panels are necessary for 250 kW generation take up space). The power losses in the cables are calculated based on load flow analysis for several sample network length. For each sample length a thinly discretized distance vector is created from 0km (beginning of the distribution network) to the sample length. The 69 RMUs are assigned randomly to an index of the distance vector, while checking for the minimum distance between two RMUs. This operation is repeated 1000 times, giving 1000 random distributions of RMUs which losses are evaluated in DC and AC. This procedure is summarised in Fig. 2.12.

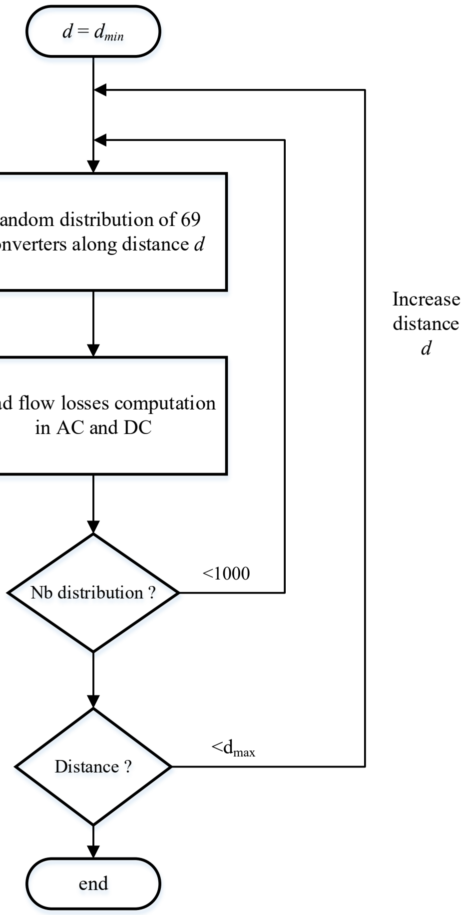


Fig. 2.12. Methodology for the calculation of losses in cables in distribution network

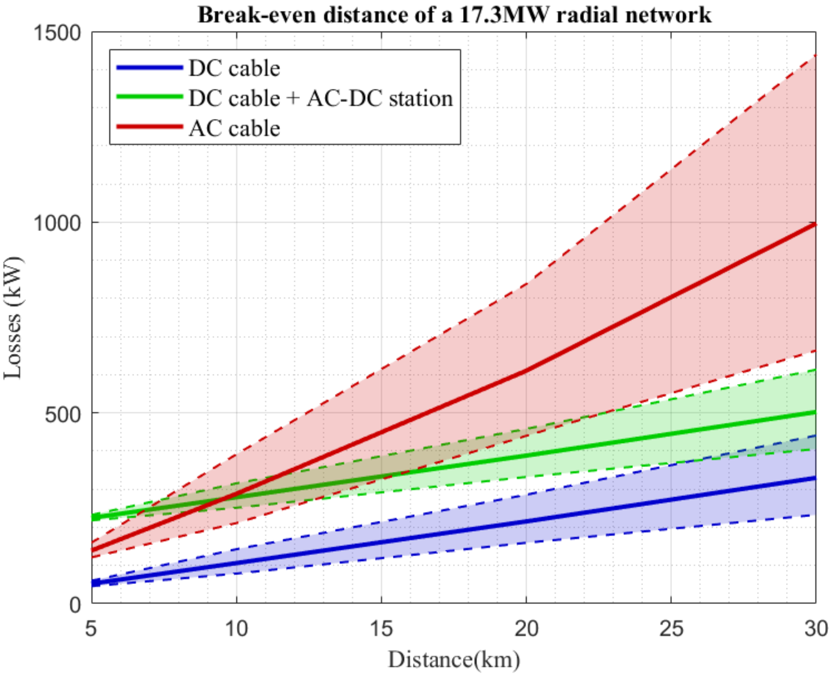


Fig. 2.13. Power losses in the 10 kV distribution network over increasing distances: solid line - average power losses, dashed line - min and max power losses according to the random distribution of loads.

It can be observed that for the same voltage/power as in the P2P case, the average break-even distance is farther away for the distribution network. This can be explained by the fact that all the power doesn't flow through the whole line. As in the case of the P2P transmission, the break-even distance moves farther away when the transmitted power decreases. The dashed lines correspond to the extreme repartitions giving the minimum and maximum losses. These extreme cases in AC and DC come from the same distributions. Thus the break-even distance range given in Fig. 2.13 is between 7.5 km and 13 km. This encompasses the break-even distance of the similar voltage/power shown in Fig. 2.9. However, it should be noted that the DC radial distribution network only adds one AC-DC station to its AC counterpart when two are added for the P2P transmission. This goes to show the impact of the distribution of loads. Indeed, having one fewer AC-DC station means the losses of the DC solution are less impacted by the converters and the effect of the cable losses are more noticeable.

It can be observed that for the extreme repartition cases, the deviation from the mean is larger in AC than in DC. Fig. 2.14 illustrates this point. The efficiencies of the cable transmission for AC and DC cases are represented for the 1000 random distributions, for the sample distance of 30km. This relatively large distance is chosen here as this effect is more and more noticeable with the increase of distance. The AC transmission efficiency ranges from 91.6% to 96.1% when the DC one ranges from 97.4% to 98.6%.

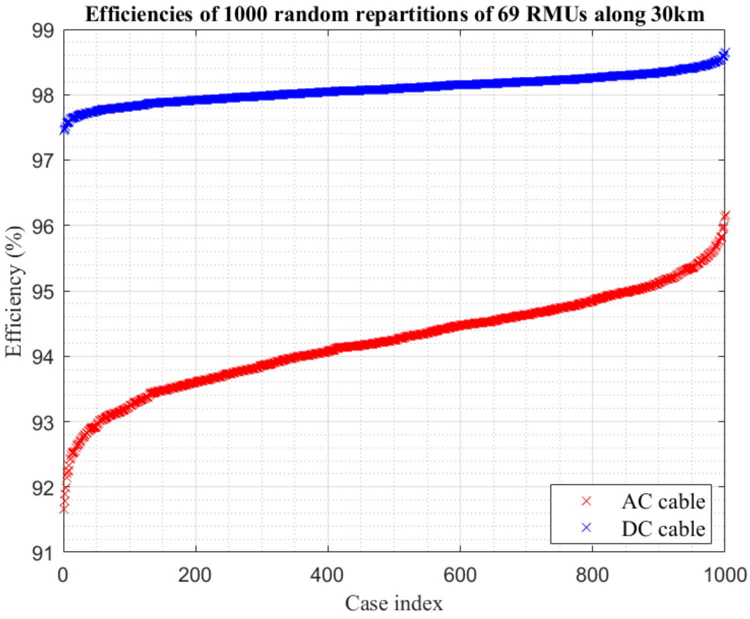


Fig. 2.14. Cable transmission efficiency of the 10 kV, 30km distribution network in function of repartition of RMUs: AC (red) and DC (blue)

It is observed again from Fig. 2.13 that for higher losses (low efficiency cases) the break-even distance is shorter. Fig. 2.15 shows the localisation of RMUs along one of the sample lengths (30km), sorted by increasing efficiencies. The density of black dots is higher at long distances and low efficiency (bottom right corner of the figure), and at short distances and high efficiency (top left corner). When most of the RMUs are located at the other end of the distribution network with respect to the AC-DC converter, the network tends to behave more like a P2P network (with the total power transmitted through the complete distance), with higher cable losses and closer break-even distance.

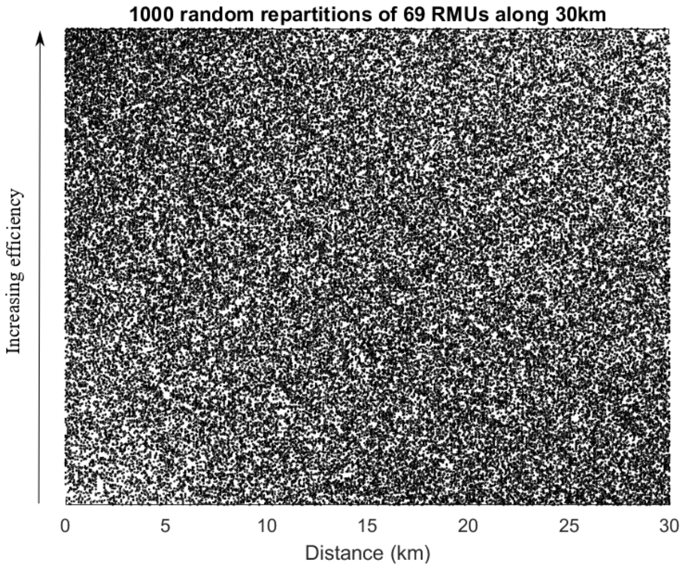


Fig. 2.15. Random repartitions of RMUs along one of the sample distance, black point is a RMU

2.2.4. Case 3: PV collection network with varying power production

Just as in the P2P case, the power transmitted in a distribution network is not necessarily constant over time. As seen in the P2P section, the effect of the transmitted power level on cable transmission efficiency should be considered when comparing AC and DC networks. The previous section presented a distribution network transmitting power to loads but the same radial network can be used for the collection of power from sources. The example of PV collection is taken here to illustrate a network with varying transmitted power. The nature of PV energy production is that the power varies over a very wide range according to the irradiation. This is shown in Fig. 2.16, which displays the irradiance level measured on a PV field during a variable weather day in Varennes, Canada on the 17/07/2014 [21].

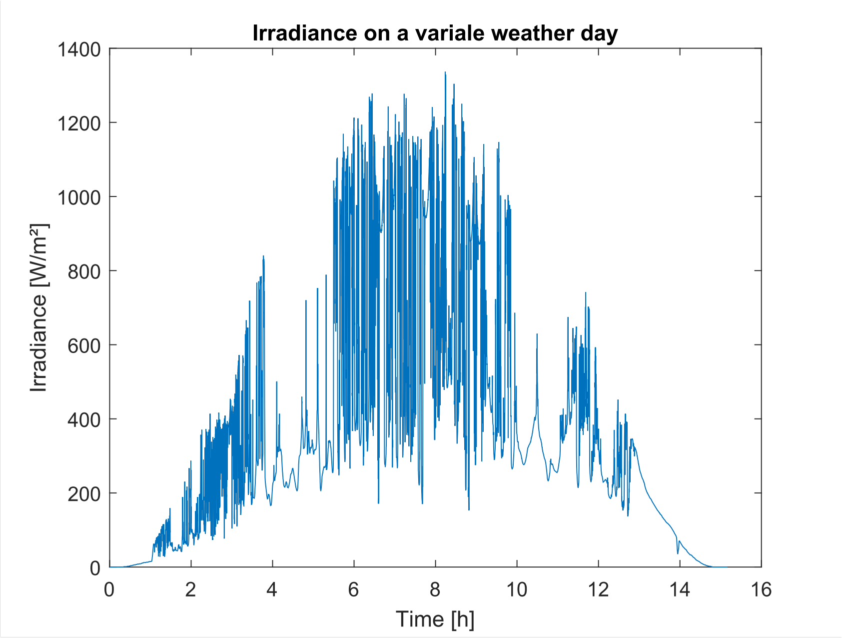


Fig. 2.16. Irradiance level during a variable weather day according to [21]

To capture the variable nature of PV generation in a single efficiency metric, weighted average efficiency were introduced [22]. The statistical study of irradiance rates gave different weighted average efficiencies that can be used to evaluate the performance of a PV system depending of its geolocation. The “European efficiency” [22] is used here. The European efficiency is a quantity often used to evaluate PV inverters and is based on a weighted average of the efficiency of the system at different fractions of the rated power. The formula is given in equation (2.3), with $\eta_{x\%}$ being the efficiency of the system at x% of the nominal power.

$$\eta_{euro} = 0.03\,\eta_{5\%} + 0.06\,\eta_{10\%} + 0.13\,\eta_{20\%} + 0.1\,\eta_{30\%} + 0.48\,\eta_{50\%} + 0.2\,\eta_{100\%} \tag{2.3}$$

By applying the coefficients of the formula to the losses found at different power levels of the sources the “European efficiency-based” break-even distance can be found. The knowledge of the production profile enables to find a break-even distance directly accounting for variable transmitted power, contrary to the general case presented in the P2P section where break-even powers had to be calculated.

In order to observe the effect of the variable irradiation, the same random 1000 distributions of RMUs are considered and the losses are evaluated at different power levels of the sources. All sources are considered to produce the same power simultaneously. The results can be seen in Fig. 2.17.

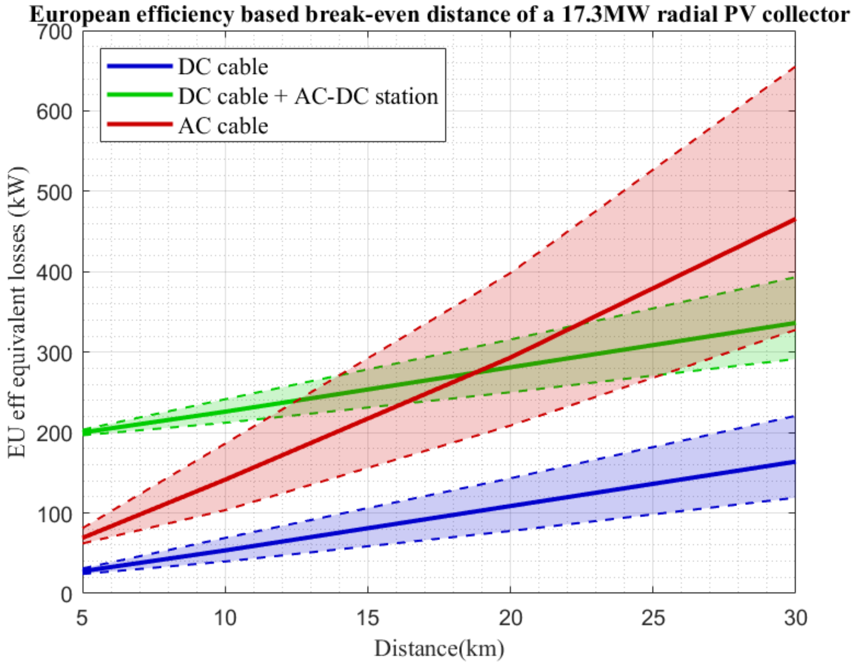


Fig. 2.17. European efficiency-based efficiency of the 10kV PV collection network over increasing distances: solid line - average power losses, dashed line - min and max power losses according to the random distribution of sources

It can be observed that taking into account the power variation of the sources results in a break-even distance farther away than in the constant maximum power case. Indeed, the average break-even distance shown in Fig. 2.17 is 18.8 km when it is only 9.6 km in Fig. 2.13. A second effect of the power variation is the increase in the spread between maximum and minimum break-even distances considering the extreme cases. This break-even distance “window” extends over 12 km in Fig. 2.17 and only 5.5 km in Fig. 2.13. This can be explained by the fact that the EU efficiency equivalent losses are smaller than the full power losses.

The results of this study can be used as guidelines for the design of the DC-DC used in the RMU of the DC architecture. The base hypothesis of the presented break-even distances is the equivalence of the RMU efficiency in both DC and AC architecture. Thus, by taking into account the efficiency of a state of the art AC RMU (in the PV example: string inverter and 50Hz transformer), one can estimate the target efficiency for the DC RMU corresponding to a target break-even distance.

2.3. Definition of case study values

The case study is fully defined here in order to have an environnement in which the DC-DC converter can be specified. The network presented in Fig. 2.18 is selected, with the specifiactions described in the following paragraphs.

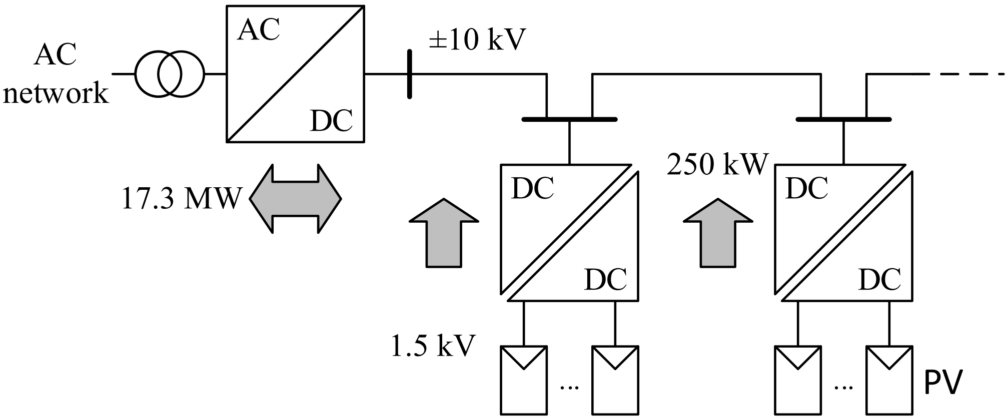


Fig. 2.18. Case study PV MVDC collection network

A 17.3 MW PV power plant spreading linearly over 20 km is considered here. This radial, ±10 kV collection network is connected on one end to the AC grid thanks to an AC-DC converter station [24]. The PV network voltage is 1.5 kV, corresponding to the maximum open circuit voltage of the PV, the PV voltage during production being always less than 1.1 kV. Multiple DC-DC converter stations are distributed along the collection network, each interfacing with multiple PV strings. Their nominal power is assumed to be 250 kW, in line with the power ratings of state-of-the-art PV inverters [9], [10]. The MVDC network voltage V_o (Fig. 2.20) is controlled by the voltage loop of the AC-DC converter station connected to the AC grid.

The MVDC network voltage level at the DC-DC converter terminals is considered to exhibit variations of ±10% in nominal operation as displayed in Fig. 2.19. The converter must be able to transmit the nominal power in the 0.9-1.1 p.u. output voltage range. In the 1.1-1.15 p.u. range, the output power is reduced following a controlled trajectory in order not to stress the network with important instantaneous power variations that could lead to instabilities. If the network voltage exceeds the 1.15 p.u. threshold, the DC-DC converter is blocked.

Voltages below 0.9 p.u. are considered to happen mostly during the MVDC bus precharge. This precharge would be done via the inverter station connected to the AC network. However, in the case of a fault at the DC-DC station, it would be separated from the network by a disconnector switch. After the fault has been cleared and in order to be able to close the disconnector switch again, the DC-DC converter would need to precharge its output to the network voltage. Thus the DC-DC converter needs to be able to start with a 0 V output and realise the precharge to the nominal voltage level. Another event considered in this voltage region is the MVDC Low Voltage Ride Throught (LVRT). This control ability of staying connected to the network, supplying a given current, during a voltage dip event is very commonly required for converters connected to an AC grid [25], [26]. A similar functionality is here envisaged for the converter connected to the MVDC network, as presented in the literature [27], [28]. This will be discussed in details in section 5.3.

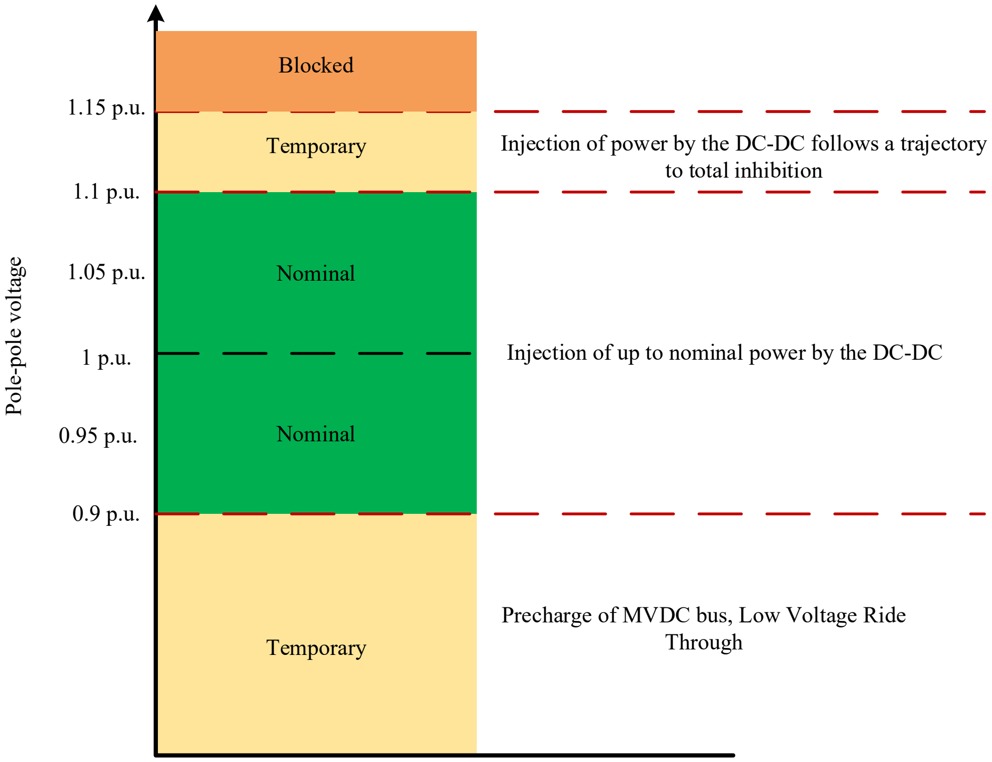


Fig. 2.19. Different operation modes MVDC voltage limits

The DC-DC converter station includes two functions. The MPPT must be realised for the different PV strings by setting the voltage at the PV buses V_{pv} to extract maximum power. The isolated DC-DC converter must also ensure the voltage step-up function from the PV low voltage to the MVDC collection network voltage. As presented in the break-even study, a symmetric monopole line configuration with high-impedance grounding is selected for the MVDC network. The PV network is ungrounded, offering the possibility to still operate after a single insulation fault. Because the grounding schemes differ between PV and MVDC networks, it is required that the DC-DC converter provides a galvanic separation. Also, an isolated converter structure is deemed more appropriate to high transformation ratio as in the presented case. The basic structure of the isolated DC-DC converter is shown in Fig. 2.20.

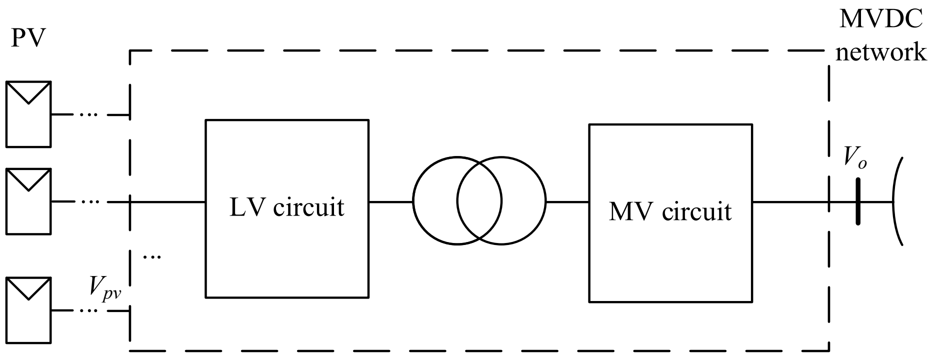


Fig. 2.20. Basic structure of the DC-DC converter interfacing PV strings with the MVDC power collection network

From the results presented in Section 2.2.4, one can reconsider the efficiencies of the DC and AC solution interface converters to be different. This enables to derive the needed European efficiency increase of the DC-DC converter, compared to its AC counterpart, so the break-even distance is moved to a certain value, as shown in Fig. 2.21.

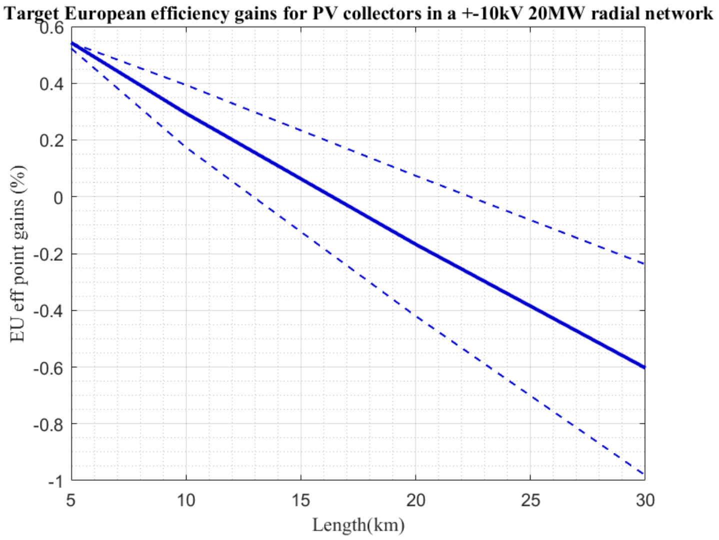


Fig. 2.21. Target European efficiency gains of DC-DC converter for targeted break-even distance

In order to translate this into an absolute value for target European efficiency, state of the art string inverters and transformer efficiencies need to be investigated. Values in Table 2.3 are taken from [10], [29], [30]. One can see in Fig. 2.22 that, in order to optimise the European efficiency, the efficiency curve with regard to transmitted power needs to remain quite flat for all fractions of power.

Table 2.3. European efficiencies of AC architecture elements

Element	EU efficiency
LV-MV transformer for PV application [29]	98.95 %
PV string inverter (multi-MPPT + inverter) [10]	98.8 %
Boost MPPT converter [30]	99.5 %

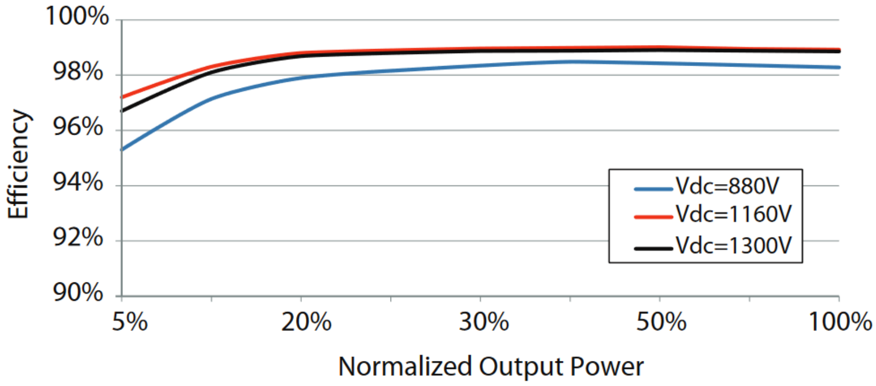


Fig. 2.22. Sungrow SG250HX-US 250 kVA PV string inverter [10]

From the values given in Table 2.3 and the efficiency increase targets given in Fig. 2.21, a target European efficiency of above 98.5% is considered for the complete converter (MPPT+step-up), translating in a break-even distance under 5 km for the ±10 kV 20 MW case. The figure below summarises the efficiency targets.

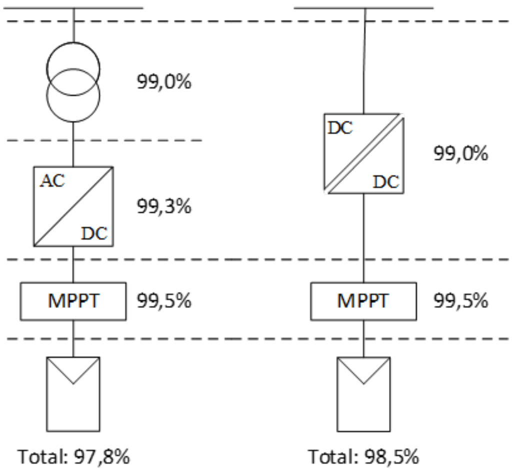


Fig. 2.23. Comparison between AC efficiency and DC target efficiency of PV converters

The parameters values defined in this section are summarised in Table 2.4.

Table 2.4. Specifications of the DC-DC converter for PV MVDC

Parameter	**Value**
Converter rated power *P*	250 kW (variations from 0 to 1 p.u. following PV mission profile)
PV string voltage V_{PV}	MPP voltage : 900-1100 V ; open circuit : 1500 V
MVDC network grid voltage V_o	20 kV (±10 kV) ±10% nominal (with additional voltage thresholds, see Fig. 2.19)
European efficiency η_{euro}	98.5% (99% for the step-up DC-DC)

2.4. Chapter conclusion

The break-even distance for HVDC has been studied extensively in literature. This chapter proposed an efficiency–based break-even distance for MVDC, considering different cases. The point-to-point case showed that the MVDC break-even distance is typically shorter than its HVDC counterpart (7 km for ±10 kV MVDC underground cable vs. around 50 km for HVDC submarine cables [13]) and depends on voltage and power levels. Compared to HVDC transmission networks, which are typically P2P lines connecting two AC grids, multipoint networks are more common in MV. The case study of the distribution network showed that the low utilisation factor of the line pushes the break-even distance farther away than in the P2P case (10 km average vs. 7 km). Finally it was observed that light load conditions of applications such as PV collection drives away the break-even distance even more (19 km average). One should note that this procedure could be done in a similar manner for a wind energy installation by using wind speed distributions [23]. Sensible MVDC break-even distances were found in all conditions (power, distribution of sources), demonstrating the advantage of MVDC in terms of efficiency. One should note that the asumption that the MVDC network should be connected to an AC grid results in a large penalty (1 percent of efficiency). In cases where this interconnections would not be needed, the break-even distance would be much shorter, making MVDC even more attractive. The economical side of this study still needs to be addressed in order to have an equivalent to the existing HVDC break-even distances. However, this is out of the scope of this work and the author will gladly let this item to individuals versed in economical studies.

It is important to note that the base hypothesis of the presented break-even distances is the equivalence of the RMU efficiency in both DC and AC architecture. Thus, by taking into account the efficiency of a state of the art AC RMU (in the PV example: string inverter and 50Hz transformer), one can estimate the target efficiency for the DC RMU corresponding to a target break-even distance. This will has been used in order to define a target European efficiency of 99% for the 250 kW 20 kV (±10 kV) step-up DC-DC converter studied in this thesis.

3. State of the art of power converters

This chapter presents the state of the art of power converters for the selected application of PV MVDC power collection. The first section describes the converters currently used in AC connected PV plants. The converter structure is then transposed to an MVDC connection scheme and refined from the previous chapter. The state of the art of DC-DC converters is then presented. First, a classification is proposed. Criteria such as of galvanic isolation, power directionality and modularity are discussed, with regards to the case study specifications. Unidirectional, isolated DC-DC topologies are particularly suited to this case study, and are given a special focus. Realisations of DC-DC converters connecting LV to MV are also taken from the literature and analysed. The last part of this chapter sumarises the characteristics of the converters which have been presented earlier. This analysis is used to select candidate topologies for further comparison.

3.1. State of the art of power converters used for PV

In order to define the converter structure of the DC-DC converter, the structure of state of the art PV string inverters is presented first. The multi-MPPT structure is then transposed to the DC collection and Fig. 2.20 is refined. The control objective of the step-up DC-DC is defined.

3.1.1. String inverter

The string inverter-based architecture was presented in Section 2.1.1. This paragraph shows the structure and topology of a typical string inverter in the power range of few hundreds of kilowatts.

Fig. 3.1 displays a string inverter schematic as can be found in [9], [10].

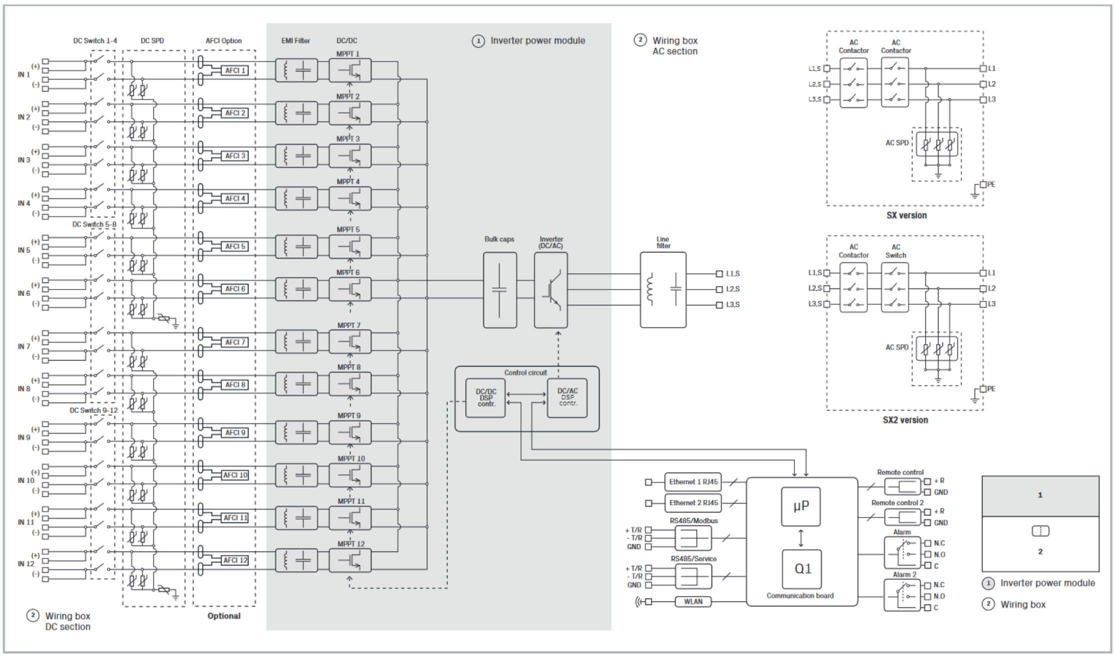


Fig. 3.1. Schematic of string inverter with multiple string inverter inputs [9]

One can observe that what is usually called string inverter is actually composed of multiple elements and not only of a DC-AC converter. On the left of the schematic, several inputs are represented. Indeed, PV panels groups are connected separately to the string inverter. Disconnector switches enable the separation of each PV panels group. Each LV input is also protected from overvoltages by varistors. Following this, EMI filters are present in order to comply with standards such as the EN 61000-6-2. The MPPT function is realised on each input by a DC-DC converter. This DC-DC converter is usually a non isolated step-up boost converter. In the power range of the tens of kilowatts per MPPT converter (as shown in this example), the multi-phased interleaved boost is often used. The outputs of the MPPT converters are then all connected in parallel to the DC-link input capacitor of the actual 3-phase DC-AC inverter. The inverter output is connected to the network filter components.

The use of multiple MPPT inputs for a single string inverter has consequences on the control roles of each element of the structure. Each MPPT converter controls its input voltage in order to extract the maximum power from the corresponding PV panels group. Because of the difference of irradiance on the different PV panels groups at a given instant, each MPPT converter will operate at a different input voltage. Hence, when using multi MPPT inputs, the input DC-link of the inverter must be controlled to a constant value independently of the transferred power. In state of the art string inverters, this is done by the DC-AC converter.

3.1.2. Towards the DC collection

In order to keep the DC-DC converter reasonably close to what currently exists in the AC solution, the structure of the LV circuit is kept. As presented in the previous section, a state of the art string inverter typically includes multiple smaller DC-DC converters at its input to perform the MPPT of different PV groups connected to this inverter. The outputs of these converters are connected in parallel to the inverter converting DC to AC. The same structure is kept for DC collection and shown in Fig. 3.2. The complete DC-DC is thus separated between the input boost converters which implement the MPPT and the unidirectional isolated DC-DC converter performing the voltage step-up function. The boost converters can be kept similar for the AC or DC collection configurations. This means the research item that must be thoughtfully studied is the step-up DC-DC converter interfacing the LV DC-link at V_{in} with the MVDC network at V_o. As in the string inverter case, the DC-link voltage V_{in} must be regulated to a constant value by the step-up DC-DC converter. Considering the MPP voltage range shown in Table 2.4, and the usual choice of boost converters for the MPPT, the DC-link voltage reference value is selected as 1200 V. The following section will present the DC-DC converters capables of realising these functions.

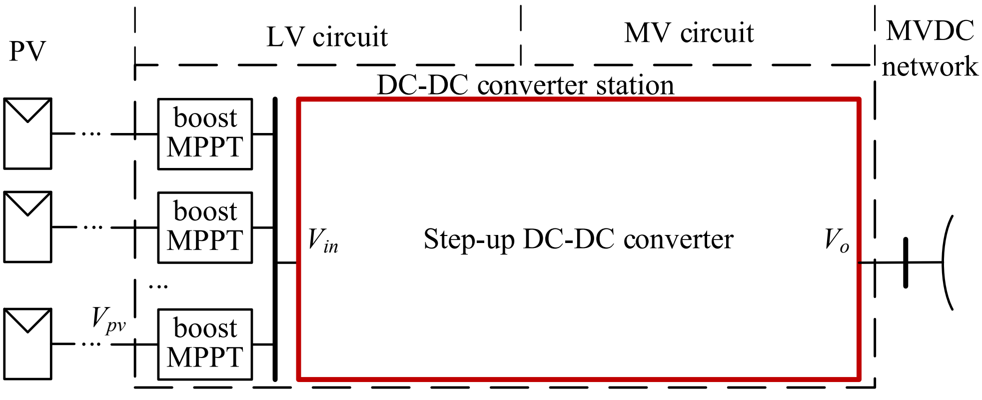


Fig. 3.2. Structure of the DC-DC converter station for PV MVDC with multiple boost MPPT converters and step-up DC-DC converter

3.2. Review of DC-DC converters topologies

This section proposes first a classification of DC-DC converters suited to MVDC networks. Part of this work has been published in [31]. A focus is made on DC-DC converters stepping up the voltage from the LV output of the MPPT converters to the MV collection network. The topics of galvanic isolation, power directionality and modularity are discussed, with regards to the case study specifications. Unidirectional isolated DC-DC topologies are then presented and classified. Implementations of DC-DC converters connecting LV to MV are also taken from the literature and analysed. Finally, their characteristics are summarised and the most promising topologies are selected for further comparison.

3.2.1. Classification

The suitability of DC-DC converters to MVDC network is analysed through three criteria: galvanic isolation, power flow directionality and modularity. The classification of DC-DC converters suitable for MVDC networks is summarised in Fig. 3.3.

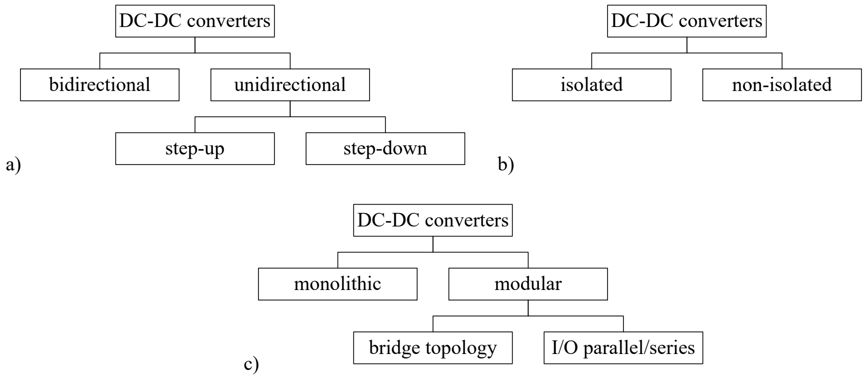


Fig. 3.3. Classification of DC-DC converters for MVDC networks according to power flow directionality (a), galvanic isolation (b) and modularity (c).

The choice between isolated and non-isolated DC-DC converters for DC systems is likely to be similar to the choice between transformers and autotransformers in AC systems. The galvanic isolation between two DC systems allows independent isolation coordination designs and grounding choice between lower and higher voltage circuits. If there were no galvanic isolation, then the DC system with lower voltage would have to respect the overvoltage constraints of the DC system with higher voltage, resulting in more bulky and costly equipment. The same approach applies to AC networks where the autotransformer is used in low ratio applications only. The choice of isolated DC-DC converters may be also driven by the power electronics design constraints. Isolated DC-DC converters based on the {DC-AC bridge / transformer / AC-DC bridge} conversion chain allow to decouple the constraints in a similar way with transformers: a transformer has a small number of turns of thick wire in its low voltage winding and a large number of turns of thin wire in its high voltage winding. Finally, a comparable quantity of copper is used in both low voltage and high voltage windings. In isolated DC-DC converters, the low voltage bridge can be optimised for high current, and the high voltage bridge can be optimised for low current. In non-isolated DC-DC converters, the semiconductor devices have to withstand both high current and high voltage. This results in a design which is far from the optimum which it is clearly visible when analysing a basic non-isolated converter like those [32] presented in Fig. 3.4. Finally, it can be concluded that a DC-DC converter with a high stepping ratio is likely to be isolated. According to [33], high stepping ratio is equal or higher than 5.

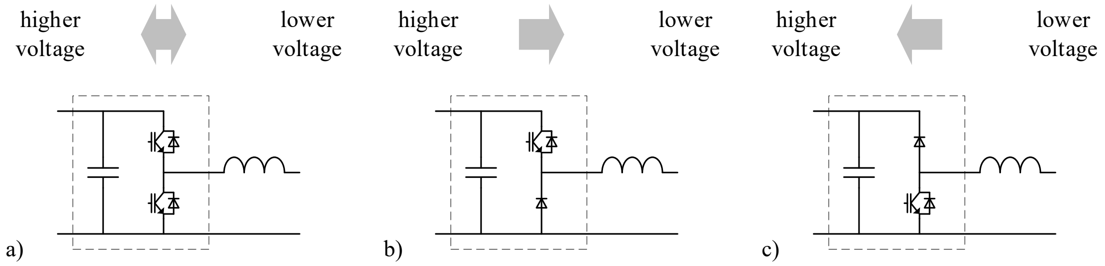


Fig. 3.4. Basic non-isolated DC-DC converters: bidirectional (a), unidirectional step down - buck (b) and unidirectional step up boost (c).

The power flow directionality is the one of the major functional differences between a DC-DC converter in DC systems and a transformer in AC systems: while the transformer is inherently bidirectional, a DC-DC converter can be designed to be either unidirectional or bidirectional. DC-DC converters can provide:

- bidirectional power flow (for example between two MVDC systems),
- unidirectional power flow stepping down (for example from HVDC to MVDC),
- unidirectional power flow stepping up (for example from LVDC to MVDC).

The general diagrams of isolated DC-DC converter topologies are presented in Fig. 3.5, and comprise a DC-AC bridge, a transformer and an AC-DC bridge. In a unidirectional converter, the rectifier bridge can involve diodes only. Obviously, a bidirectional DC-DC converter can be also used in an applications which require unidirectional power flow only. However, the performance to cost ratio of the unidirectional converter is expected to be higher than its bidirectional counterpart.

In the case of the DC-DC converter interfacing PV strings with an MVDC network, only unidirectional power flow is required. A unidirectional MVDC DC-DC converter is expected to offer a higher performance-to-cost ratio thanks to the use of diodes on the MV side. The use of diodes also avoids issues of power supply and driving of controled semiconductor devices on the MV side. In this idea, the proposed control scheme must be compliant with the simplicity of the unidirectional MV converter. Ideally, no sensor on the MV side would be used. The downside of having a simple passive rectifier made of diodes is that no control action can be taken on the MV side in cases of faults on the network. Once the low-voltage bridge is blocked, the only elements of the circuit affecting the fault response are the filter components.

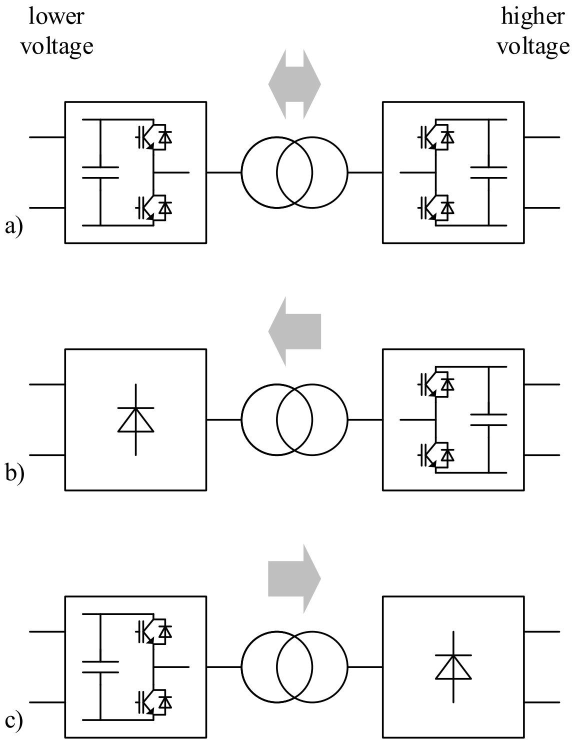


Fig. 3.5. General diagrams of isolated DC-DC converter topologies: bidirectional (a), unidirectional step down (b) and unidirectional step up (c).

DC-DC converters can be designed as monolithic or modular. In the monolithic isolated DC-DC converter design, there is one DC-AC bridge, one transformer and one AC-DC bridge which process the entire power. In the modular isolated DC-DC converter design, there are multiple bridges and transformers, each processing a fraction of power. The input and output bridges can be connected either in parallel or in series. For example, the input parallel and output series (IPOS) connection allows to reach high step-up ratio. DC-DC converter for MVDC applications proposed in the literature are often based on modular designs [27], [34], [35]. The following paragraphs discuss the motivations for modular or bulk power conversion considering the case study.

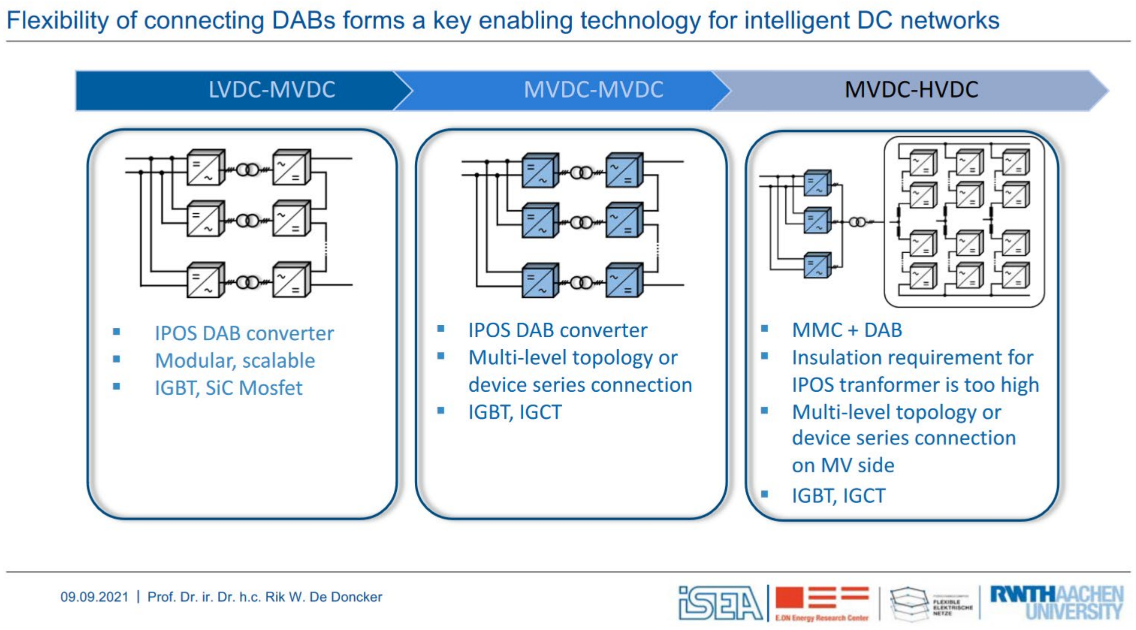
Modularity can appear at different levels in the isolated DC-DC converter:

- LV Inverter level: paralleling of low power inverters
- Converter level: connection of complete isolated converters, typically Input Parallel Output Series (IPOS) for LV/MV [36]
- MV Rectifier level: use of multi secondary transformer [37]

Regarding the inverter level modularity, several arguments can be made. Paralleling of complete LV inverters can be employed to give redundancy in critical applications. In this case, the full converter has to be designed so it can keep operating with one failed inverter. However, low power inverters to be paralleled would typically use discrete component and the number of devices to parallel to match power module performance can be quite important. Additionally, the current sharing has to be taken care of, when in power module this is already done between the inner chips. Finally, the inverter modular design, if not necessary for the application reliability requirements, is considered to be more a part of an industrial optimisation problem when dealing with very important number of devices.

Regarding converter-level modularity, monolithic converters are expected to be more compact, particularly because insulation constraints are present on only one device. On the contrary, as the vast majority of semiconductor devices is rated 6500V or less, converters can resort to modularity to reach higher voltages for MVDC applications. In [38], Pr. De Doncker promotes modular IPOS DABs for LV-MV converters (Fig. 3.6). One should note that the scalability usually linked to modular converters is not complete in IPOS configuration as output voltage and power are linked. The IPOS configuration is not suited to HV, because the isolation system of each transformer must be designed for the worst case (i.e. the topmost converter in Fig. 3.6). In such case, a single-transformer step-up converter is proposed instead of the IPOS configuration (Fig. 3.6, right). Although the limit between MV and HV is not clear, the MV converter presented in Pr. De Doncker's keynote at EPE21 [38] is 5 kV 400 kW (as a reminder, the ratings for the present study are 20 kV, 250 kW). The ratio between active parts and insulation volume is more probably the decisive factor, not voltage alone.

The modularity of DC-DC converters can also be achieved thanks to the modularity of the bridges. The typical modular bridge structures are neutral point clamped (NPC) [39] and modular multilevel converter (MMC) [40]. DC-DC converters based on MMC are suitable for HVDC applications [41] and may be also suitable for MVDC applications, when the 2-level and NPC are no longer cost effective (likely above 10/20 kV).


Flexibility of connecting DABs forms a key enabling technology for intelligent DC networks

LVDC-MVDC
- IPOS DAB converter
- Modular, scalable
- IGBT, SiC Mosfet

MVDC-MVDC
- IPOS DAB converter
- Multi-level topology or device series connection
- IGBT, IGCT

MVDC-HVDC
- MMC + DAB
- Insulation requirement for IPOS tranformer is too high
- Multi-level topology or device series connection on MV side
- IGBT, IGCT

09.09.2021 | Prof. Dr. ir. Dr. h.c. Rik W. De Doncker

Fig. 3.6. Slide from EPE21 conference keynote of Pr. De Doncker [38]

For unidirectional step-up converters, the output bridge can be formed of series-connected diodes, so no MV semiconductor device is needed. One can thus consider that, in this case, the use of converter level modularity is driven by the following points:

- The most straightforward one is the application specifications, typically redundancy for continuous operation as in [37] (3 modules but the converter is able to operate with only 2 modules).
- Converter level modularity enables interleaving, which can reduce the filters size for same ripple performance. However, if the filter is specified from short-circuit behaviour, this doesn't have beneficial effects.

- Sometimes the driver is rather the situational convenience, typically using already designed bricks for a new converter design. For example, the converters presented in [27], [35], [36] seem to reuse the same bricks.

Regarding the rectifier level modularity, the choice must be driven by transformer/rectifier integration. Paper [42] presents a 100 kW 30 kV transformer connected to 24 full-bridge rectifiers. Given the large number of terminals on the MV side, a special care is given to making them small enough, so that they do not end up taking a disproportionate space. However, one should note that the terminal are only designed to prevent partial discharge at 30kV; there is no indication that they meet standards requirements.

As a conclusion on modularity, modularity at inverter level is considered more of a matter of industrial optimisation based on available components. This aspect is not explored in this thesis work. The converter level modularity is attractive for bidirectional applications in order to use regular, controlled, semiconductors without using series connection. However, when increasing the output voltage, the insulation requirement of IPOS transformers becomes too cumbersome. For an unidirectional application such as our case study, the motivation for converter level modularity is less obvious. The initial argument of simplicity and compactness of the monolithic solution is thus kept for the studied converter. The rectifier level modularity is to be explored in the integration phase of the prototype.

To conclude this section, the schematic of the DC-DC converter station for PV MVDC from Fig. 3.2 can be refined with the considerations on galvanic isolation and unidirectional power flow. The converter of interest, the step-up bulk unidirectional isolated DC-DC converter is presented in Fig. 3.7. The schematic is divided between the input active inverter bridge, MFT (isolated), diode rectifier (unidirectional) and output filter. One should note that the output filter is represented with an inductor and a capacitor but only a capacitor can be used for certain topologies. The existing unidirectional isolated DC-DC converter topologies following this scheme will be presented in the following section.

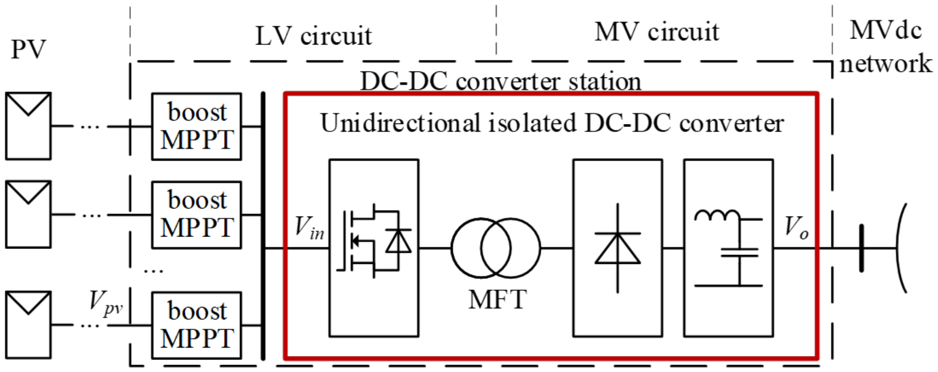


Fig. 3.7. Structure of the DC-DC converter station for PV MVDC with step-up bulk unidirectional isolated DC-DC converter

3.2.2. Topologies

Here is an overview of isolated DC-DC converter topologies with unidirectional power flow. A classification of the topologies with these characteristics is proposed in Fig. 3.8. Beyond the topology itself, converter control and modulation can further impact the performance of the converter. The variants associated to these considerations are shown in the round shapes but only the main representants of their categories are discussed in the text.

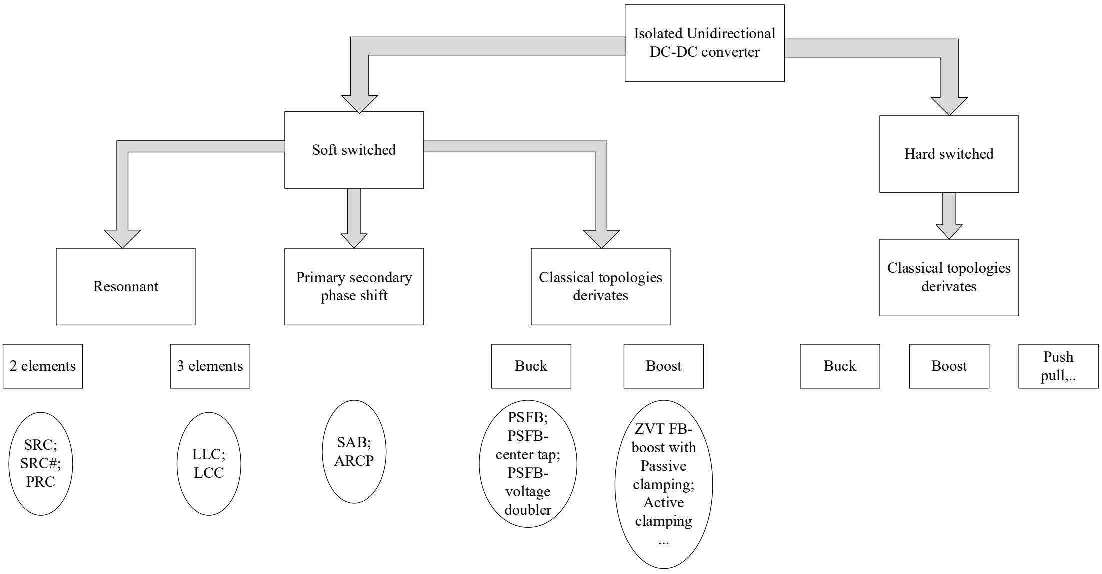


Fig. 3.8. Isolated unidirectional DC-DC converter topologies classification

The “hard switched” branch can be directly discarded because of the high efficiency requirement of the application as presented in Chapter 2. Indeed, with full switching losses of all switches, the input bridge would present power losses close to that of a typical string inverter (the modulation is different). Thus, the full DC-DC converter, having two more stages, would not be competitive. Hence, only soft switched topologies are presented below.

Three categories are identified in the soft-switching part of the classification. The first category relies on resonant circuits (with different number of elements) shaping the AC-link waveforms. It includes mainly the series resonant converter (SRC) and LLC. The second category uses the phase shift between the primary and secondary bridge of the isolated converter. This category is derived from the concept of the Dual Active Bridge (DAB) adapted to the unidirectional Single Active Bridge (SAB). The last category relies on the similar operation as traditional switched inductor topologies such as the Buck or Boost, only with an additional isolation stage. In this category, the soft switching is achieved thanks to the resonance of parasitic components during the dead-time intervals (necessary between turn-off and turn-on of two switches of an half-bridge to prevent cross-conduction). The main Buck-derivated isolated converter is the Phase-Shifted Full Bridge (PSFB) and the Boost-derivated is the ZVT Full Bridge Boost. The following paragrahs describe each of these topologies in more details.

The series resonant converter (SRC) is composed of an inverter, an LC resonant circuit (L_{ac}, C_{ac}), a transformer and a diode bridge with capacitor filter as presented in Fig. 3.9. It was proposed in [43] using thyristors where the LC circuit ensures the device commutation and energy transfer. However, the topology can be implemented with any power semiconductor device. The circuit offers a buck (step-down if the transformer ratio is 1) operation mode. The gain can be controlled by frequency modulation, changing the impedance of the resonant circuit. It must be noted that the operation at a switching frequency equal to the resonant frequency enables to have an unity voltage gain that is independent of the transmitted power. This makes this topology particularly attractive for applications where a constant voltage ratio is needed. The zero-voltage switching (ZVS) is achieved for all switches in a power range which depends on the circuit parameters.

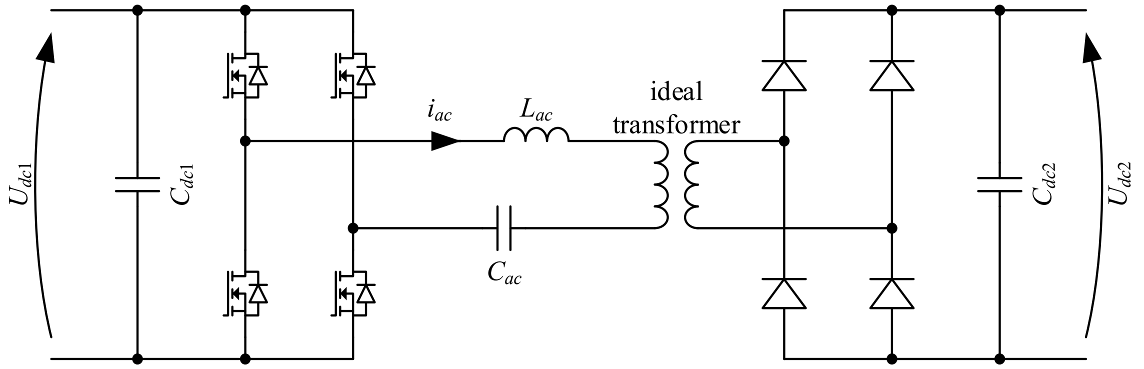


Fig. 3.9. Series resonant converter (SRC)

A SRC variant, the LLC converter uses an LLC resonant circuit (L_{ac}, L_m, C_{ac}) instead of an LC one, as presented in Fig. 3.10. The LLC circuit may be physically realised with the leakage (L_{ac}) and magnetizing (L_m) inductance of the transformer. The analysis of the circuit is presented in [44]. This circuit offers buck and boost operation through frequency modulation. The boost operation is obtained thanks to the parallel resonance between L_m and C_{ac}. The ZVS for all switches is achieved over the entire power range. This whole-range ZVS requires a small magnetizing inductance (typically in the high tens to low hundreds µH). Indeed, it is because the magnetizing current remains relatively large (compared to that of a traditional transformer) at any transmitted power level that ZVS can be ensured.

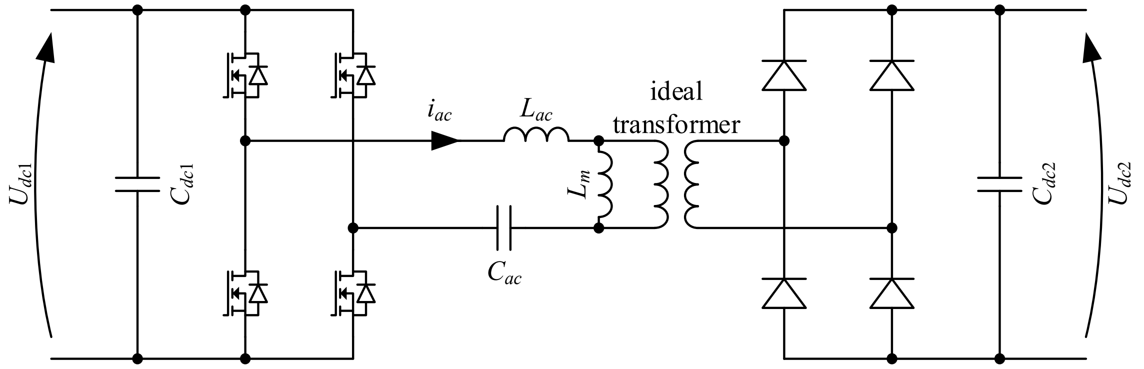


Fig. 3.10. LLC resonant converter (LLC)

The DAB was invented near 1989 and the patent [45] was granted in 1991. The DAB is composed of two VSCs connected with a transformer and it should be mentioned that the operation of the DAB requires the use of two VSCs. If the rectifier is replaced with a diode bridge then the topology becomes unidirectional and is referenced to as a Single Active Bridge (SAB) [46]. The SAB circuit diagram is presented in Fig. 3.11. The SAB is usually uncontrolled and variations of input or output voltages have an important impact on its ZVS range. This makes this topology not attractive for our case study application where the input voltage must be controlled, while the output voltage can have variations (Table 2.4).

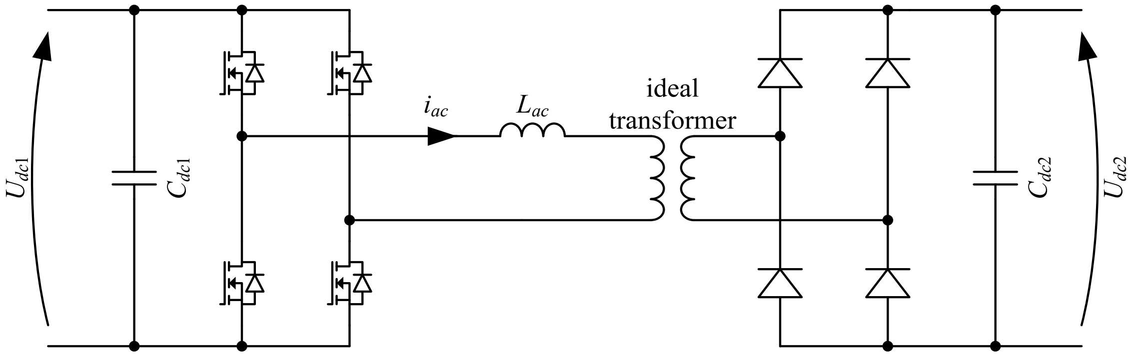


Fig. 3.11. Single active bridge (SAB)

The Phase-Shifted Full Bridge (PSFB) is composed of an inverter, a transformer and a diode bridge with an LC filter (L_{dc}, C_{dc2}) as presented in Fig. 3.12. It was proposed in [47] and is based on the Buck structure. ZVS is obtained through phase-shift control over the complete power range for one half-bridge. The ZVS range of the other half-bridge depends on the value of the leakage inductance L_{ac}. This ZVS limit is usually at around 50% of the maximum power. This topology offers the possibility of avoiding the LC resonant circuit, which may cause technological challenges in high power applications.

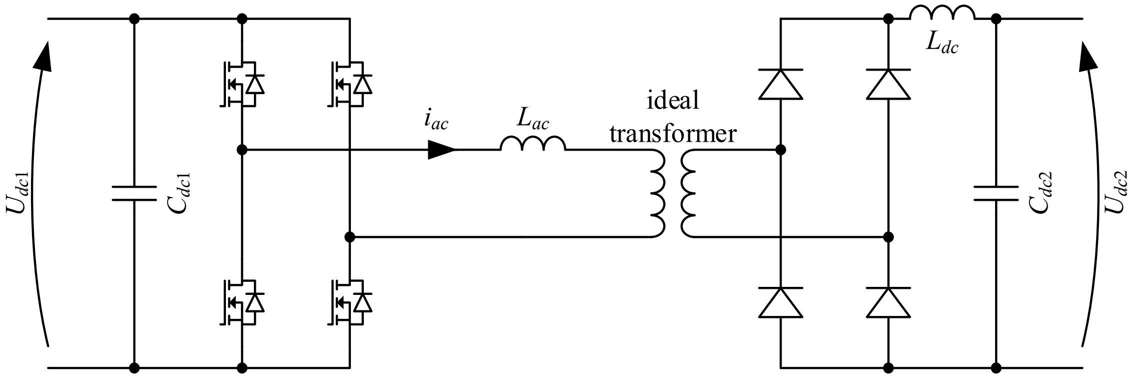


Fig. 3.12. Phase-shifted full bridge (PSFB)

The Isolated Full Bridge Boost is composed of an input inductor L_{dc}, an inverter with additional clamping circuit, a transformer and a diode bridge as presented in Fig. 3.13. It was proposed in [48]. This topology offers larger voltage gains than the PSFB because of its Boost operation. This enables the design of a transformer with a smaller winding turns ratio (corresponding to the lower boundary of the output voltage variation range). However, this also means that the converter needs additional circuits to start/operate if it is not connected to the network at nominal voltage. This drawback can prove to be problematic for certain grid-connected functionalities such as Low Voltage Ride Through (LVRT) [28]. Also, an additional clamping circuit (switching at twice the bridge frequency) is necessary in order to avoid large commutation overvoltages on the input inverter due to the connection of two current sources (the input inductor and the transformer leakage inductance). This clamping circuit increases the number of semiconductor components, which also have associated losses. Similarly to the PSFB, the ZVS range is not complete for all switches.

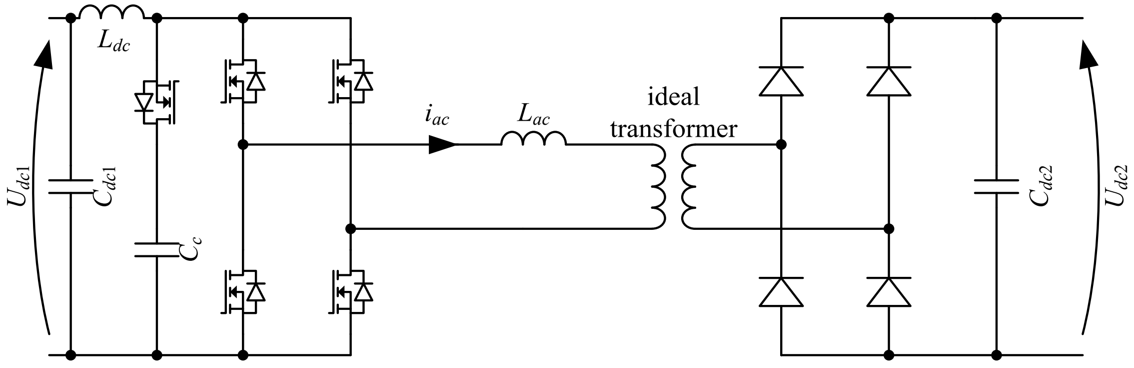
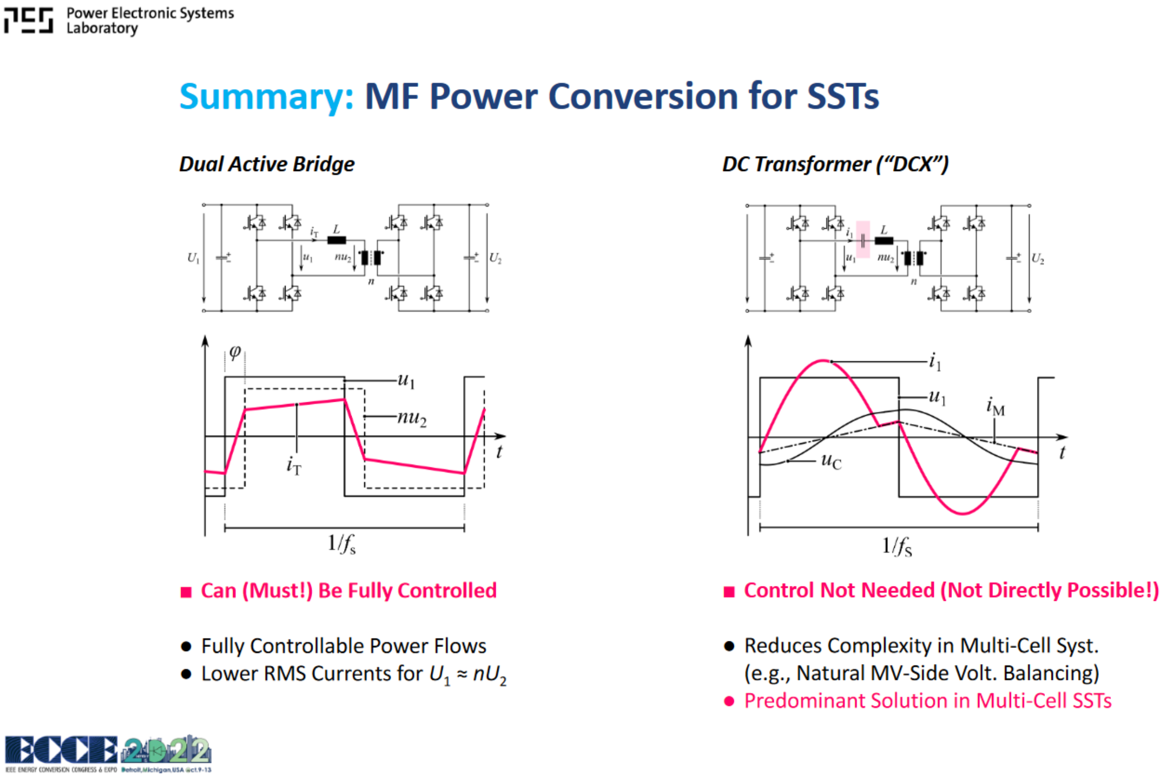


Fig. 3.13. Isolated Full Bridge Boost

In the ECCE '22 tutorial on Solid State Transformers [49] Pr. Kolar presented a distinction between two important categories of DC-DC converter topologies. The resonant converters are operated, in open-loop, in applications where the maximum efficiency is paramount and neither voltages need to be controlled. This is the closest to the function of a regular AC transformer, hence the name DCX (XFRM being the acronym for transformer). When control is needed at one of the converter port, the DAB is preferred. Considering the case study where only unidirectional power flow is needed that corresponds to topologies such as the PSFB or Isolated Full Bridge Boost.


Power Electronic Systems Laboratory

Summary: MF Power Conversion for SSTs

Dual Active Bridge

- **Can (Must!) Be Fully Controlled**

- Fully Controllable Power Flows
- Lower RMS Currents for $U_1 \approx nU_2$

DC Transformer ("DCX")

- **Control Not Needed (Not Directly Possible!)**

- Reduces Complexity in Multi-Cell Syst.
  (e.g., Natural MV-Side Volt. Balancing)
- Predominant Solution in Multi-Cell SSTs

ECCE 2022

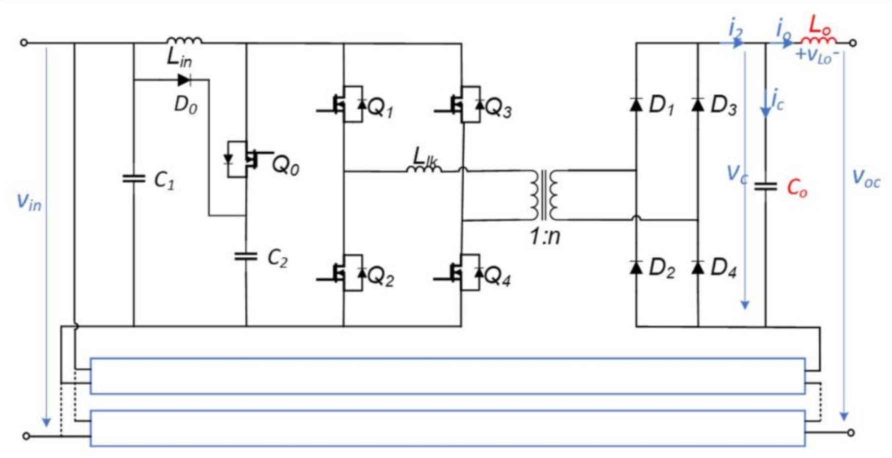
Fig. 3.14. Two main categories of DC-DC converters with their domain of use [49]

3.2.3. Examples of LV-MV DC-DC implementations

This section focuses on the DC-DC converter prototypes designed to connect LVDC to MVDC and which have been described in the scientific literature. The converters presented here are also selected based on their power ratings, in the hundreds of kW.

The converter presented in [27] is an IPOS connection of modules based on a modified Isolated Boost converter. One the particularity of this realisation is the addition of an inductor at the output, after the output capacitor. These inductors are added to protect the converter in case of faults in the MVDC network (these considerations will be discussed in a the following chapter). When compared with the PSFB, one can consider that this topology is using one additional inductor on the LV side. However, it must be noted that this converter ensures both the MPPT and voltage step-up functions, when the PSFB is only doing the voltage step-up function. The other modification the addition of the diode D_o shown in Fig. 3.15. One can see that with this modification this topology resembles the cascade of a bypassable boost converter (realising the MPPT) and a SAB doing the voltage step-up. The comparison must then be done between the PSFB (with its MV inductor between the rectifier and the output capacitor) and the SAB with an additional inductor at the network side, after the output capacitors. The implications of these differences will be discussed in the later section dealing with fault behaviour.

The implementation of the converter is shown in Fig. 3.15. The complete converter is installed in a cabinet. The circuit is separated in 3 elements: the LV circuit, the MFT and the MV circuit. One must note that the MV inductors are not included in the MV modules and are probably at least as voluminous as the MFT modules. The MFT modules are insulated with dielectric liquid. All semiconductors components are SiC MOSFETs and diodes used at a switching frequency of 50 kHz. The control is based on duty cycle modulation of switches Q_1 Q_3 and Q_0. The efficiency of the converter peaks at 98.9%. However the measurement method of the power losses is not given and no uncertainty bars are shown. Assuming the losses are measured electrically by a difference between input and ouput power, the efficiency value doesn’t convey much information. Indeed it was shown in [50] that such measurement of a high efficiency MV converter would be too uncertain (98.17…99.83% for a 99% efficient 10kV SiC-based inverter).



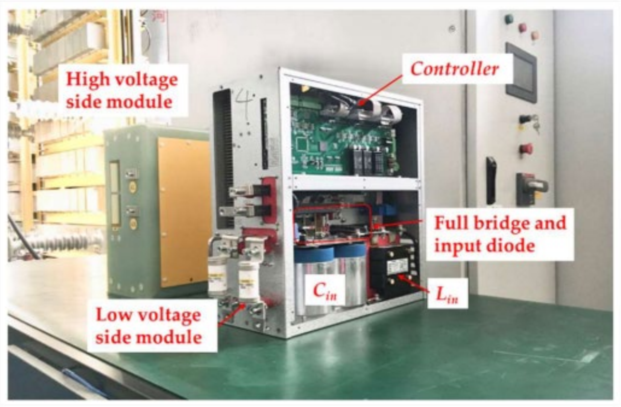


Figure 18. 5 kV/50 kW SiC dc–dc module.

Figure 19. ±10 kV/200 kW SiC PV MVDC converter.

Fig. 3.15. 20 kV 200 kW isolated boost converter for PV MVDC application presented in [27]

The converter presented in [42] Fig. 3.16 is based on a variant of the LLC resonant converter: the LCC. This variant is known for its high gain its shunt capacitor must whistand high current/voltage variations. The implementation of the MFT is of particular interest. Indeed, this 30 kV insulated MFT is immersed in a dielectric liquid. It has multiple secondary windings, enabling to have no series connection of diodes on the medium voltage side. The modularity is here used at the rectifier level. A particular care was given to the design of the MV bushings in order to keep a reasonable volume with so many of them. All semiconductors components are Si IGBTs and diodes at maximum switching frequency of 22 kHz. The control of the converter is described in [51]. The phase-shift modulation is selected over the frequency modulation for output voltage control. This is motivated by the reduction of semiconductor losses and thermal cycling. This consideration is likely oriented towards the cooling system design and not the efficiency itself. No measurement of losses is given. Indeed, the application doesn't require especially high efficiency but robustness and reliability.

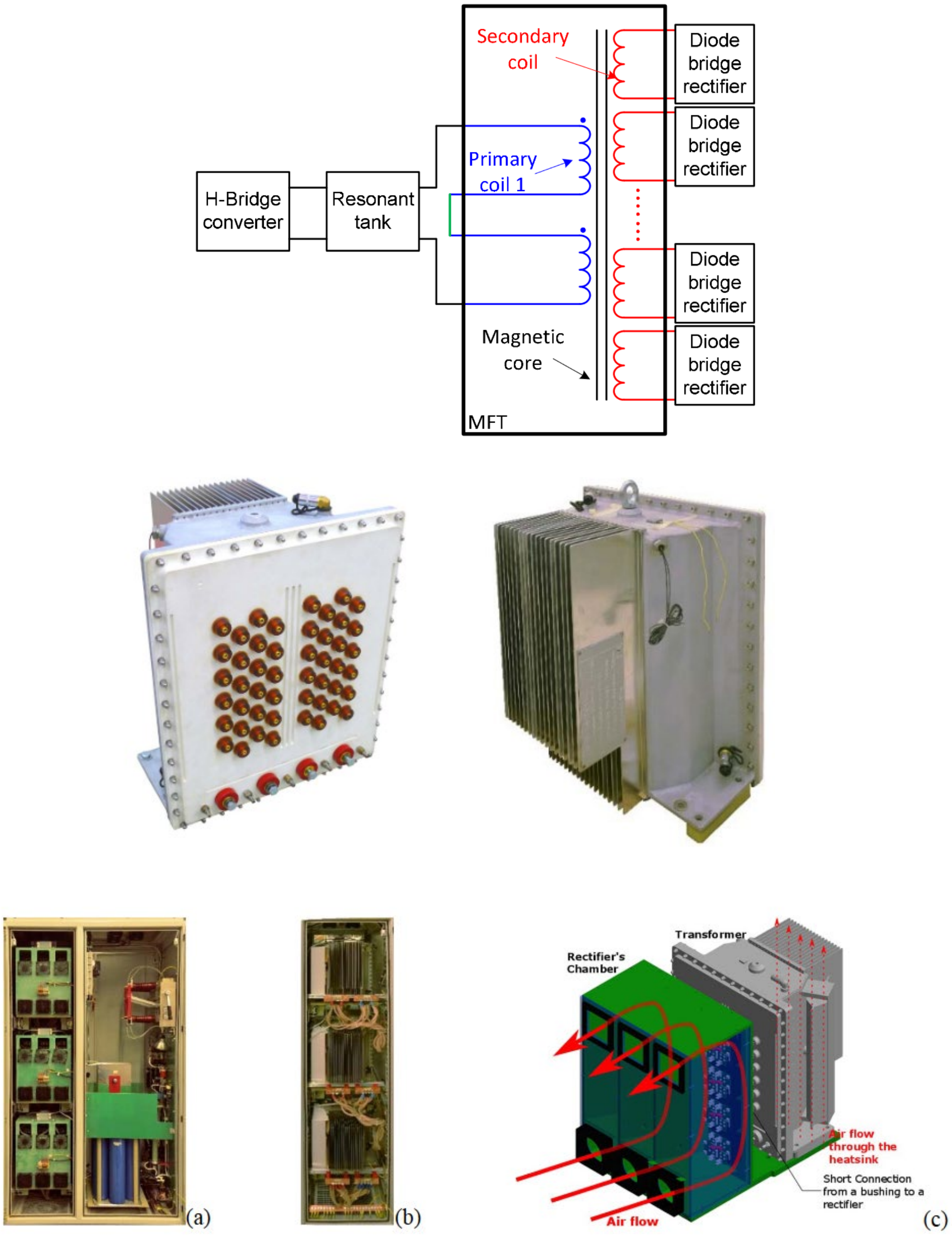
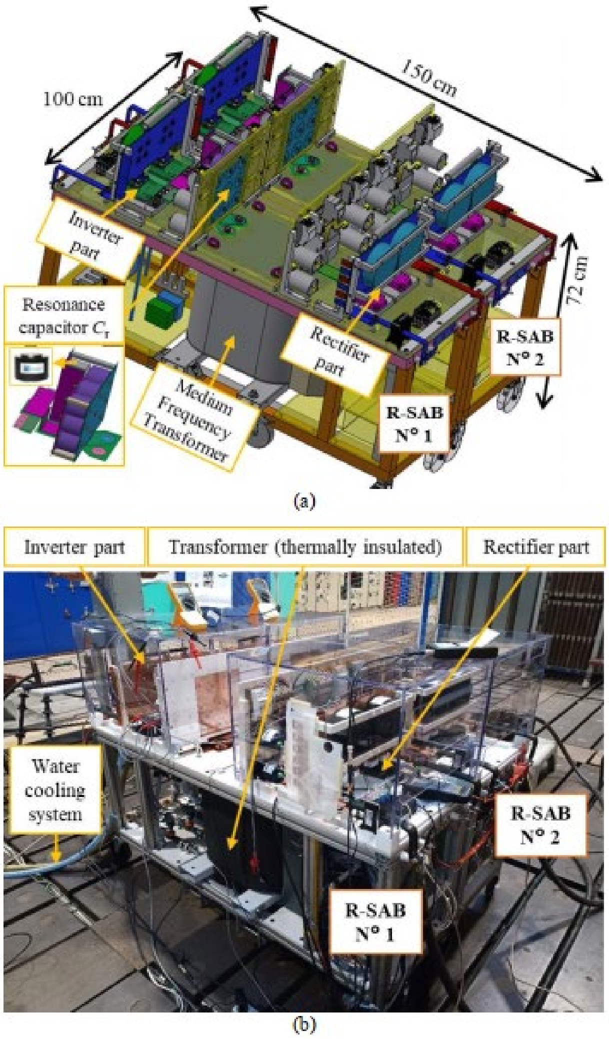


Fig. 3.16. 25 kV 200 kW LCC resonant converter CERN power supply presented in [37], [42], [51], [52]

The converter in Fig. 3.17 is an ISOP demonstrator of a 3.6 kV / 1.8 kV 600 kW traction converter [53]. 3.3 kV SiC MOSFET are operated at 15 kHz. It must be noted that these components are still not as mature as lower voltage rated SiC MOSFETs. The MFT is oil insulated. The uncontrolled "SAB-R" topology is used. This is a variant of the resonant topologies which is similar to the SRC. The converter is supposed to operate in open-loop at a constant frequency. The maximum efficiency is measured at 98.86%. The efficiency measurement is done with a calorimetric method, which gives more confidence in the results compared to an electrical measurement.



(a)

(b)

Fig. 3.17. 3.6 kV 600 kW SRC demonstrator for traction applications presented in [53]

The demonstrator of the thesis [54] consists in one module of an IPOS SRC# (SRC with a different control scheme), with a 5 kV output voltage. The MFT is insulated in dielectic liquid and the rectifier is proposed to be immersed in an other oil tank. No particular implementation of the complete converter is done as can be seen in the set-up shown in Fig. 3.18. All semiconductor components are Si IGBTs and diodes operated at a maximum frequency of 1 kHz. The efficiency of the low power prototype is electrically measured with a peak at 95.5%. However the full power converter composed of ten 1 MW modules is expected to have a 98.5% efficiency.

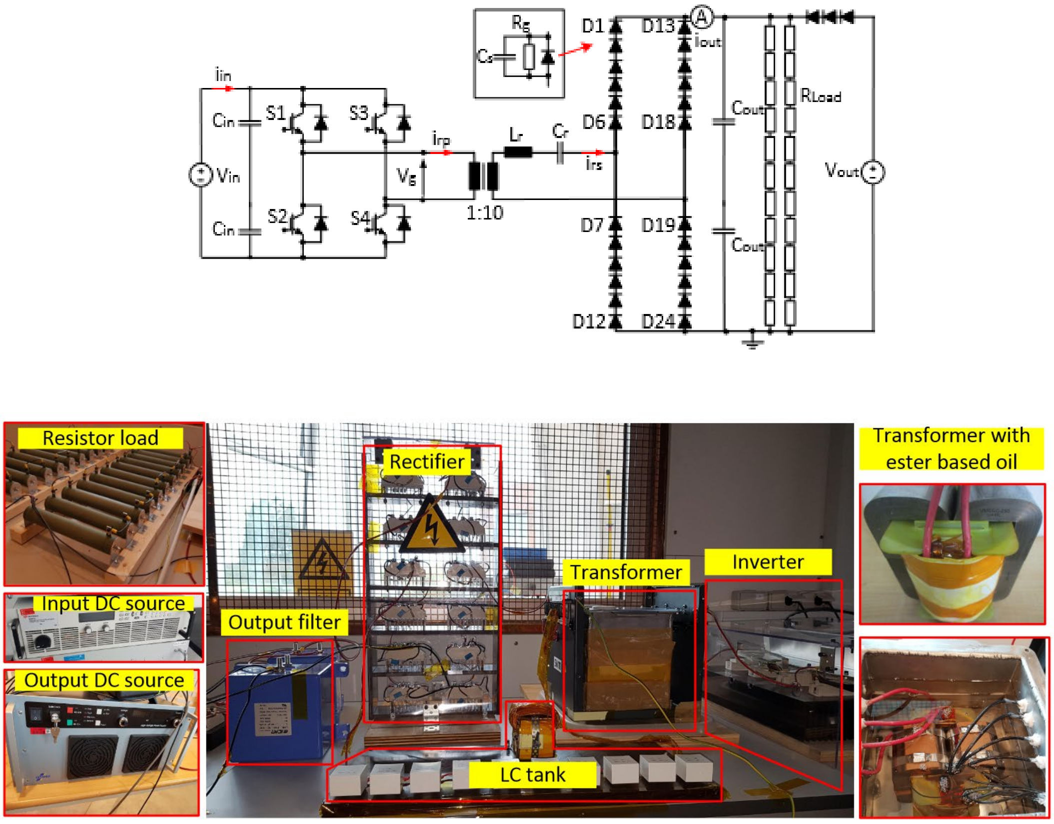


Fig. 3.18. 5 kV 10 kW SRC# small scale demonstator for MVDC wind turbine application [54]

The converter presented in Fig. 3.19 is a demonstrator of the Uniflex PM [55] European project. This converter has AC ports but includes a DC-DC converter at its core. The 25 kW module presented in Fig. 3.19 is meant to operate with 1.1 kV input and 3.3 kV ouput. An association of 11 modules in parallel was tested with a transmitted power of 300 kW. Here again, the dielectric liquid insulation is used for the MFT. The semiconductor components are all Si IGBTs operated at a switching frequency of 2 kHz. The control relies on phase-shift between the 2 bridges of the DC-DC converter. No efficiency measurement or estimation are given.

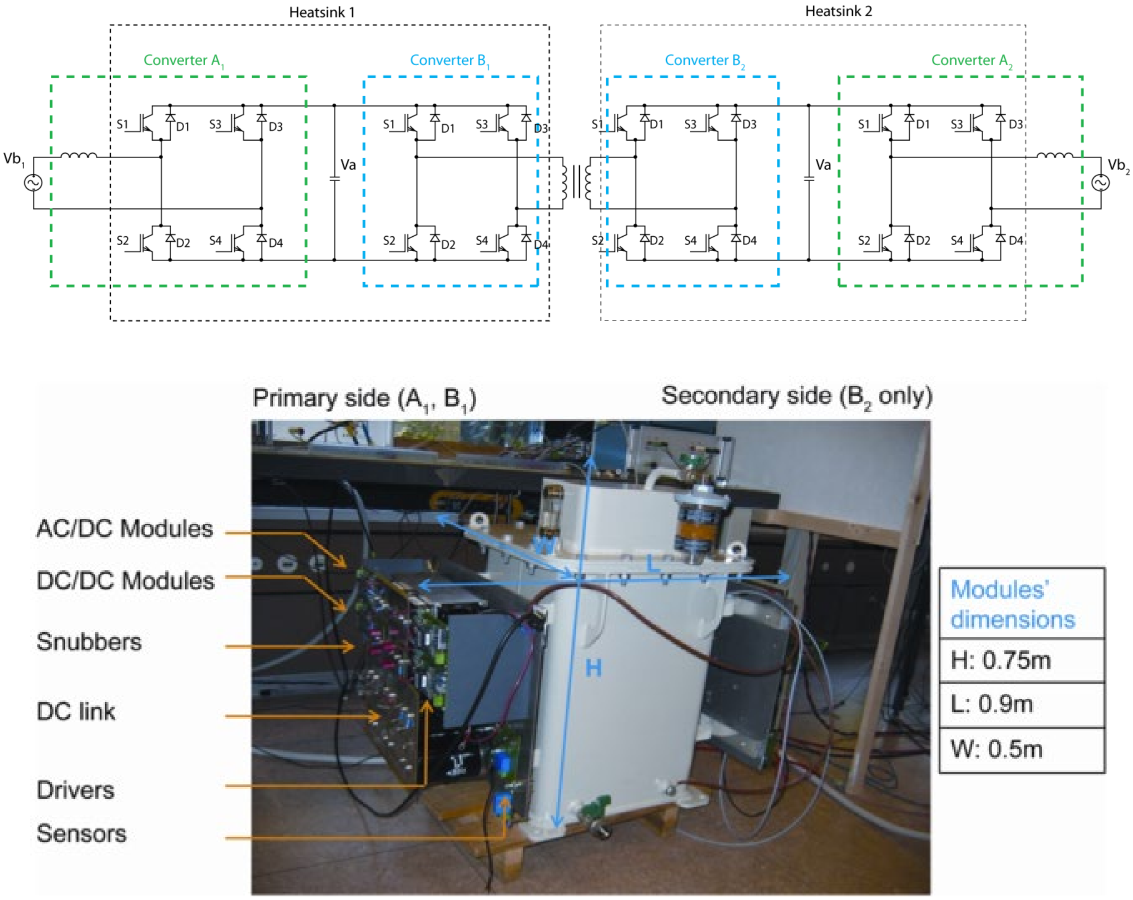


Fig. 3.19. 3.3 kV 25 kW module of the 11 modules UNIFLEX PM 300 kW demonstrator [55]

3.3. Chapter conclusion : selection of candidate topologies

The realisations presented in the previous section are summarised in Table 3.1. The converters are named by their institutions.

Table 3.1. Summary of LV/MV DC-DC demonstrators

	CAS	**CERN**	**LAPLACE**	**AALBORG**	**UNIFLEX**
Source	[27] [36]	[37], [42], [51], [52]	[53]	[54], [56]	[55], [57]
Topology	Isolated boost	LCC	SRC	SRC#	DAB
V_{in} (V)	800	540	3600	500	1100
V_{out} (kV)	20	25	1.8	5 (50)	3.3
P (kW)	200	200	600	10 (1000)	300
F (kHz)	50	22	15	1	2
Eff (peak) (%)	98.9	-	98.86	95.5 (98.5)	-
Semiconductor technology	SiC	Si	SiC	Si	Si
MFT insulation	Oil	Oil	Oil	Oil	Oil
Number of modules	4	3	2	1 (10)	11
Control	Duty cycle	Phase-shift	Open loop	Phase-shift + frequency	Phase-shift (Prim-Sec)

From Table 3.1 it is seen that both resonant and non-resonant topologies are used in LV/MV DC-DC demonstrators. Even though it is preferrable to use the resonant topologies in open loop at their optimal operating point, CERN and AALBORG cases show that they can also be selected when control is needed. However, one should note that the frequency is never used as their main control variable but rather the phase-shift.

For our considered application, the efficiency is important in the sense that below a certain level the MVDC collection concept loses its relevance over MVAC collection. However, the input voltage of the converter must be regulated because of the presence of multiple MPPT. The choice of the appropriate topology is thus not straightforward and candidate topologies from the resonant and non-resonant families must be evaluated with the case study values.

The resonant topologies will be represented by the SRC and LLC. Both these topologies will be studied together as they are ruled by the same equations. The study will show whether or not the Boost capabilities of the LLC can be used in this particular case.

The PSFB is selected as representable topology of the non-resonant group. Indeed the additional elements needed to operate the Isolated Full Bridge Boost as a grid connected converter (one more inductor after the output capacitor, bypassing diode for start-up, as shown for the CAS converter) make it less attractive.

It can be oberserved that, for applications requiring high efficiency, SiC components are used. The selected topologies will thus be evaluated considering this semiconductor technology. Based on Table 3.1, switching frequencies used for SiC-based prototypes range from 15 kHz to 50 kHz. Considering the high efficiency requirements, the initial choice of the quite “low medium” frequency of 20 kHz is made to be used during the topology evaluation.

The majority of the presented converter realisations use the modularity aspect at the converter level. However, following the discussion in Section 3.2.1, the motivation for a modular design for an unidirectional converter is not obvious. The bulk power conversion approach is selected for the following study of the candidate topologies. Both approaches seem appropriate but the lack of bulk power converters in the presented literature calls for this research path decision.

One can note that the presented realisations use dielectric liquid insulation for the MFT. This insulation method is the most common for 50 Hz distribution transformers of this voltage and power range. This observation will be used in the chapter dealing with implementation choices.

4. Comparison of DC-DC converter topologies for PV MVDC

In this chapter, the DC-DC converter topology that is the most suited to our application case is identified through a comparison between the various candidates. A dimensioning of the converter is realised for each candidate topology, based on the case study specifications derived in the previous chapters. The comparison of the topologies is first based on the sole criterion of efficiency. The losses are obtained by simulations. The calculated efficiencies are put in perspective with the break-even distance results from Chapter 2. A second comparison is realised, based on the behaviour of the circuit when faced with faults on the MVDC network. This study involves both simulation and experiments on a small-scale prototype and has been published in [31]. Finally, the choice of the preferred topology is made based on the obtained results.

4.1. Dimensioning

The designs used to evaluate the different isolated converter topologies are based on the specifications derived in the previous chapters and summarised below:

- **Power range**: The converter must be able to transmit the power over the full range of 0-250 kW.
- **Output voltage range**: From Fig. 2.19, the converter must be able to transmit the nominal power for an output voltage range of 19 to 21 kV. In the 21-22 kV range the power is limited the by MPPT converters. In the 22-23 kV range output power can be null but the converter must still operate.
- **Input voltage**: constant (1200 V), controlled by the DC-DC converter.

The following sections propose designs for the selected topologies: SRC/LLC resonant converter and phase-shifted full bridge (PSFB). Their control is investigated to determine whether or not it can meet the specifications: controlling the input voltage at 1200V over the whole power and output voltage ranges.

4.1.1. LLC/SRC converter

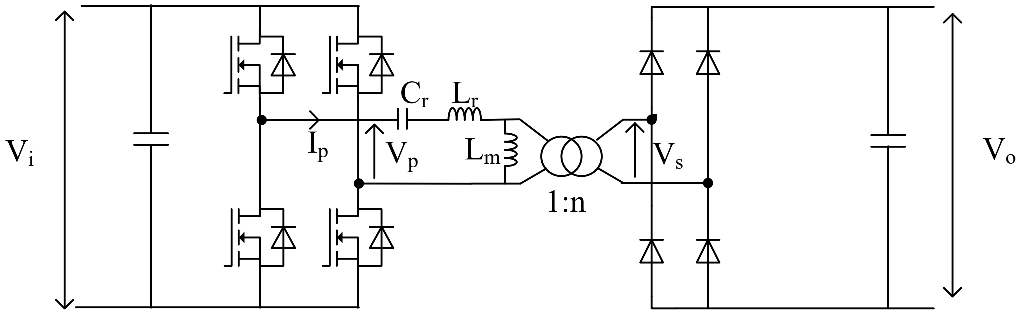


Fig. 4.1. SRC/LLC converter

The LLC is analysed first as it presents the highest complexity. The SRC differs only by the design choice of using a large ratio between series and parallel inductances (L_r and L_m in Fig. 4.1). Observations on the SRC can thus be made afterwards using the general equations of the LLC.

The input bridge waveforms of an SRC/LLC are presented for operation with switching frequency f_{sw} being lower than resonant frequency f_{res} (equation (4.1)) in Fig. 4.2 and with f_{sw} higher than f_{res} in Fig. 4.3.

$$f_{res} = \frac{1}{T_{res}} = \frac{1}{2\pi\sqrt{L_r\, C_r}} \tag{4.1}$$

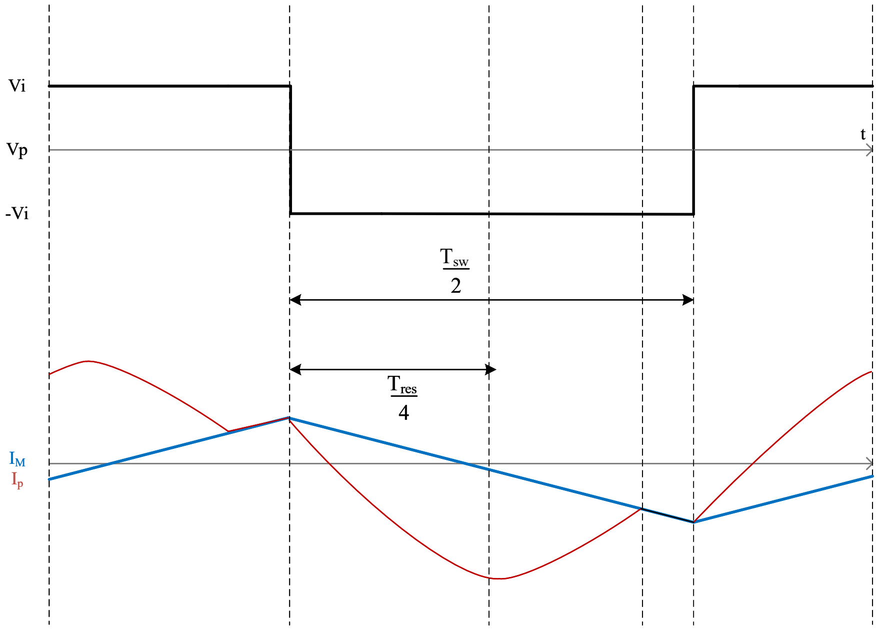


Fig. 4.2. LLC key waveforms for $f_{res}>f_{sw}$ (I_M amplitude is exaggerated to show its effect)

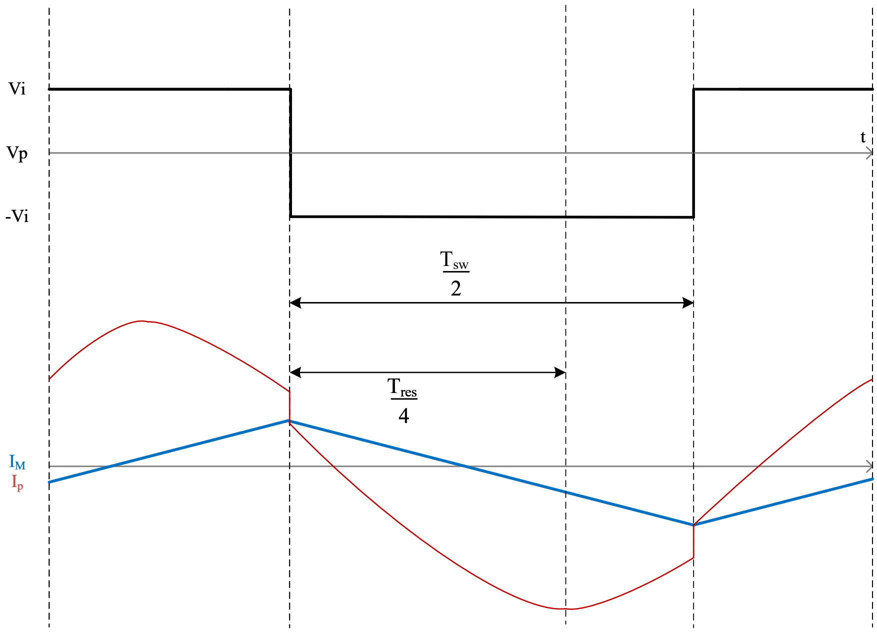


Fig. 4.3. LLC key waveforms for $f_{res}<f_{sw}$ (I_M amplitude is exaggerated to show its effect)

As the LLC can achieve boost and buck voltage ratio by operating below and above the resonant frequency, the turns ratio of the transformer can be defined as the ratio between nominal output and input voltages.

$$n = \frac{V_{o,nom}}{V_i} = 16.66 \tag{4.2}$$

It is considered that the resonant tank (*C_r*, *L_r*, *L_m*) is used to provide the gains needed to cover the output voltage range defined as:

$$V_o = m\, n\, V_i \tag{4.3}$$

$$m_{max} = \frac{V_{o,max}}{n\, V_i} = \frac{V_{o,max}}{V_{o,nom}} = 1.15 \tag{4.4}$$

$$m_{min} = \frac{V_{o,min}}{n\, V_i} = \frac{V_{o,min}}{V_{o,nom}} = 0.9 \tag{4.5}$$

Using the first harmonic approximation [58], the gain of the LLC tank can be expressed as:

$$m = \frac{1}{\sqrt{(\frac{1}{L_n} + 1 - \frac{1}{L_n\, {f_n}^2})^2 + Q^2\, (\frac{1}{f_n} - f_n)^2}} \tag{4.6}$$

with f_n the ratio between the switching frequency and the tank resonant frequency:

$$f_n = \frac{f_{sw}}{f_{res}} \tag{4.7}$$

and the ratio between magnetising and leakage inductance of the transformer called L_n:

$$L_n = \frac{L_m}{L_r} \tag{4.8}$$

One should note that to achieve ZVS the operating frequency has to always be on the inductive side of the gain curve (m decreasing with increasing f_n) [58]. The second condition is on the magnetising inductance which needs to ensure sufficient current to charge/discharge the MOSFETs output capacitance during the deadtime (arbitrarily chosen as 1% of the resonant frequency). The output capacitance is considered with a typical value for 1700 V SiC MOSFET C_{oss}=1.7 nF (Rohm BSM250D17P2E004).

$$I_m \geq \frac{V_i\, 2\, C_{oss}}{t_{dead}} \tag{4.9}$$

$$L_m \leq \frac{V_i}{4\, f_{res}\, I_m} = 1.67\, mH \tag{4.10}$$

This condition is always checked for the designs.

The resonant tank quality factor Q is the ratio between the tank impedance and the equivalent load AC impedance, determined from the DC load under the considered output voltage:

$$Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{Load,ac}} = \frac{n^2\, \pi^2\, P\, \sqrt{\frac{L_r}{C_r}}}{8\, {V_o}^2} \qquad (4.11)$$

From this it can be understood that for a given f_n and L_n, the higher the power P, the lower the gain m. Thus, the dimensioning condition is to ensure the maximal gain m_{max} at power P_{max}, and the minimal gain m_{min} at minimal power. A way of representing this is to plot the resulting input voltage as a function of the control variable, for the different output voltage levels of the specification. The crossing point with the 1200 V line is the value of the control variable needed to regulate the input voltage. This also shows how much the input voltage strays from its reference value when the control variable is not correct.

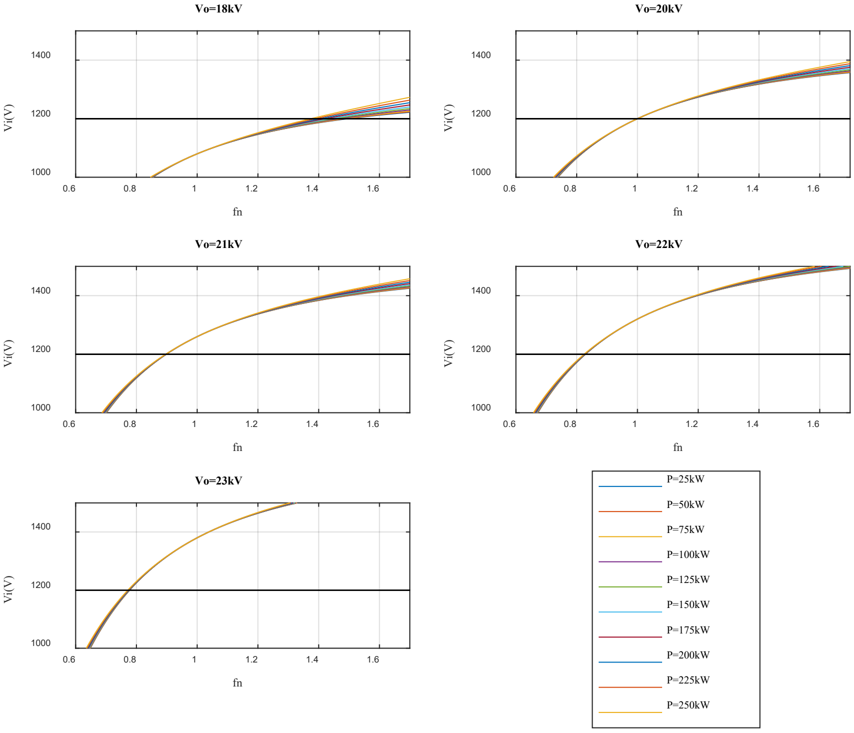


Fig. 4.4. LLC control space with L_n=5 and $Q(P_{max})$=0.22

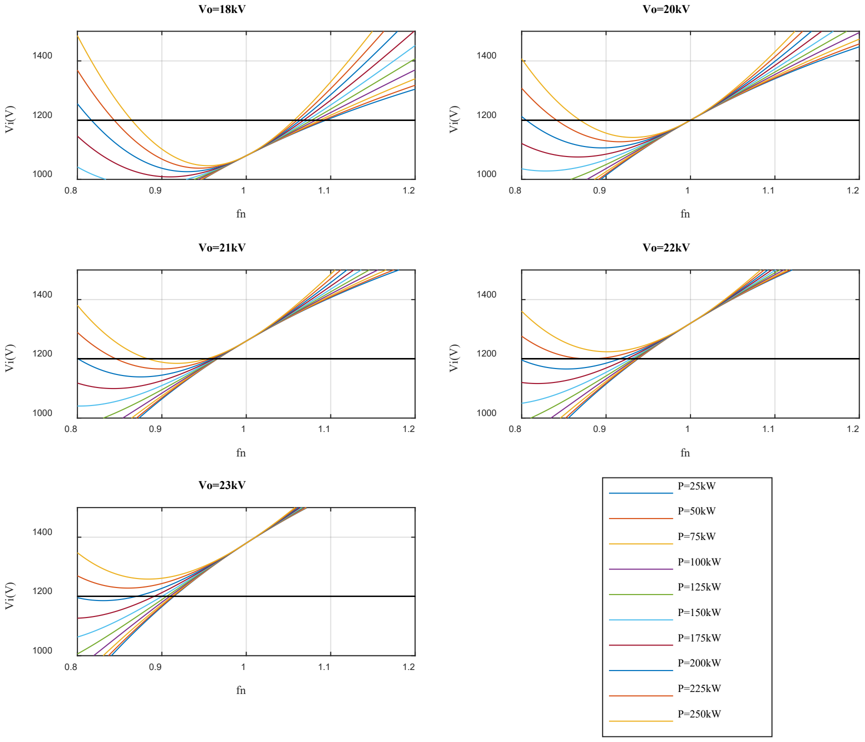


Fig. 4.5. LLC control space with L_n=1.5 and $Q(\mathrm{P_{max}})$=2

It is shown in Appendix 1 that meeting this condition requires either a large range of frequency variations (design with L_n=5 and $Q(\mathrm{P_{max}})$=0.22, Fig. 4.4) or designing for a high $Q(\mathrm{P_{max}})$ (with L_n=1.5 and $Q(\mathrm{P_{max}})$=2, Fig. 4.5). One should note that such a design with a high $Q(P_{max})$ leads to low values of C_r and thus large voltage variation across this capacitor, as described by the approximate formula given in [59]:

$$V_{Cr,peak} = \frac{n\,\pi}{2\,f_n}\sqrt{\frac{L_r}{C_r}}\,\frac{P}{V_o} \tag{4.12}$$

For the design with $Q(P_{max})$= 0.22 and L_n=5, the maximum voltage at the primary side of the transformer is 1.7 kV. For the design with $Q(P_{max})$= 2, enabling frequency variations in the range of f_n=[0.9 1.1] the voltage at the primary of the transformer reaches 5 kV. This would lead to an impractical implementation of the transformer and resonant tank.

The SRC can be seen as an LLC designed with the highest L_m given by equation (4.10) and a high L_n. Appendix 1 shows that with such a design, the boost area is now impossible to access without extreme frequency variations. Therefore, the transformer ratio must be set to make the maximum voltage gain.

$$n = \frac{V_{o,max}}{V_i} = 20.125 \tag{4.13}$$

Fig. 4.6 shows the result of a design with L_n=35 and $Q(\mathrm{P_{max}})$=3, in a similar manner as for the LLC. Increasing $Q(\mathrm{P_{max}})$ in order to reduce the needed frequency range is not desirable because of the implementation problems highlighted by equation (4.12).

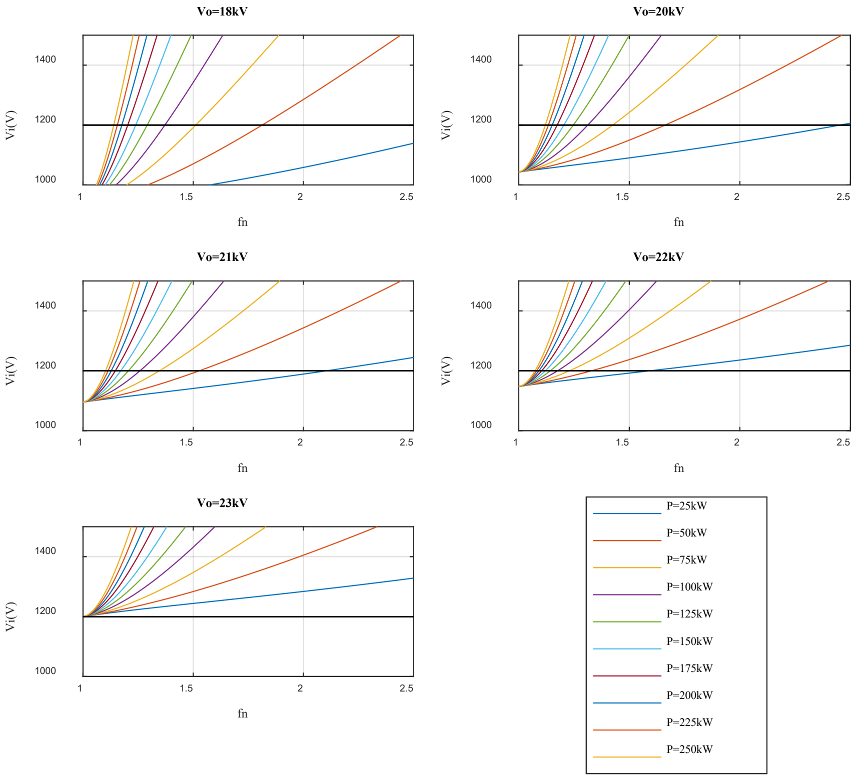


Fig. 4.6. SRC control space for L_n=50 and $Q(\mathrm{P}_{\mathrm{max}})$=3

This shows that the SRC is hardly considerable for applications where certain quantities need to be controlled while avoiding large frequency variations. It is more attractive in applications where no control is needed and a fixed gain is necessary. It must be noted that hybrid control methods can be implemented to answer the high frequency increase at low loads. Still, in the considered application the LLC is deemed to be the more relevant resonant topology and the SRC will not be compared further is this chapter.

One way to deal with the problem of higher frequency than wanted, to achieve low gain, is to use phase-shift modulation. The phase-shift modulation consists in introducing a delay between the gate signals of the two legs of the inverter. This phase shift δ in radians is defined in the range [0 : π] with respect to the switching period (0 means not shifted and π means shifted by half a period). Appendix 1 describes the implication of this control method with a fixed switching frequency equal to the resonant frequency. The problem with only relying on phase-shift to control the LLC is that the phase-shift at nominal voltage is important, resulting in important peak-to-RMS current ratio that is detrimental to the semiconductor switches. A hybrid frequency and phase shift control can be used so the converter still benefits from boost characteristics and the transformer turns ratio doesn't have to be defined from the maximum voltage. In [60], it is proposed to use phase shift control for switching frequencies higher than resonant (f_{sw}>f_{res}). Design guidelines for L_n and Q are also given as maximising their product, while keeping sufficient gain at f_{min} and staying in the inductive part of the gain curve for ZVS. This is represented in Fig. 4.7, where the resulting designs for combinations of Q and L_n are evaluated for the application specifications. The white region represents the combinations meeting the specifications and the black region the combinations not meeting the specifications. The red dot is the point inside the white region maximising the product of Q and L_n. One must note that it results in a design where the voltage ripple on the AC link is significant (2.6 kV).

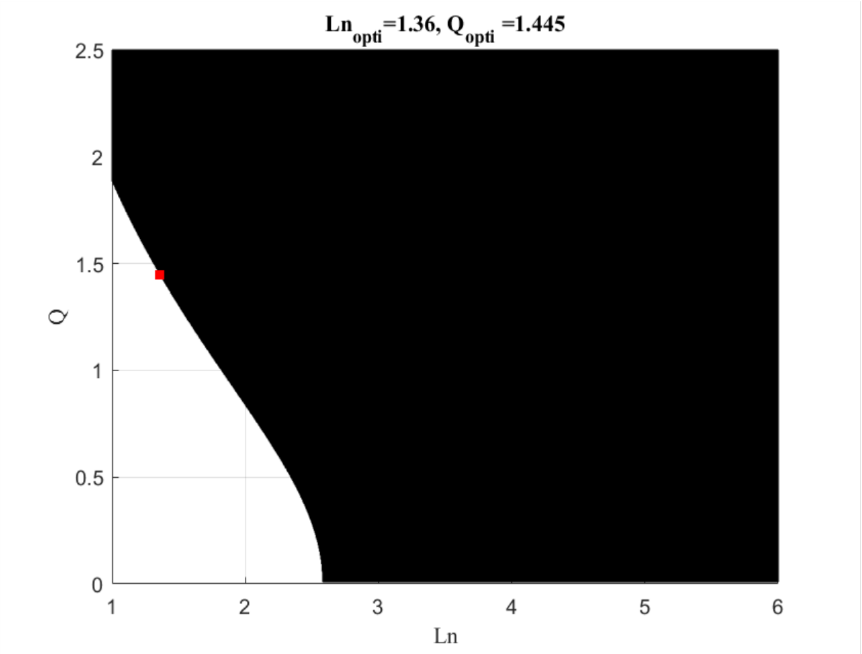


Fig. 4.7. Map of design parameters Q and Ln for the application specifications. White: specifications met, Black: specifications not met

For the comparison done in the end of this section, the LLC with the strategy of phase-shift control for switching frequencies higher than $f_{sw}>f_{res}$ is considered.

4.1.2. Phase-shifted full bridge (PSFB)

The PSFB is the topology that has been selected to represent the non resonant topologies. The main waveform and control parameters are defined in

Fig. 4.9 in CCM. The leg formed by MOSFETs Q_1 and Q_2 switching at $I_{p\text{-}pk}$ is called the leading leg and the leg Q_3 and Q_4 switching at I_{p1} is called the lagging leg.

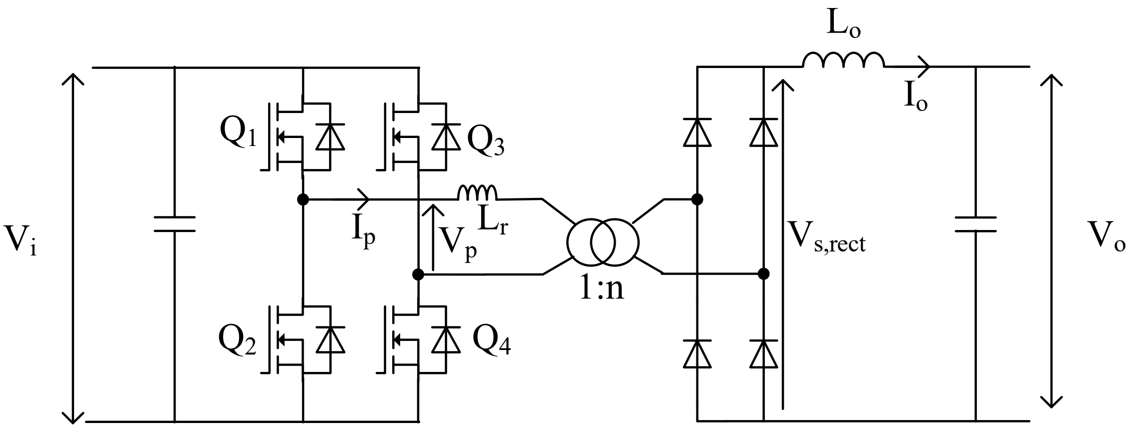


Fig. 4.8. Phase-Shifted Full Bridge

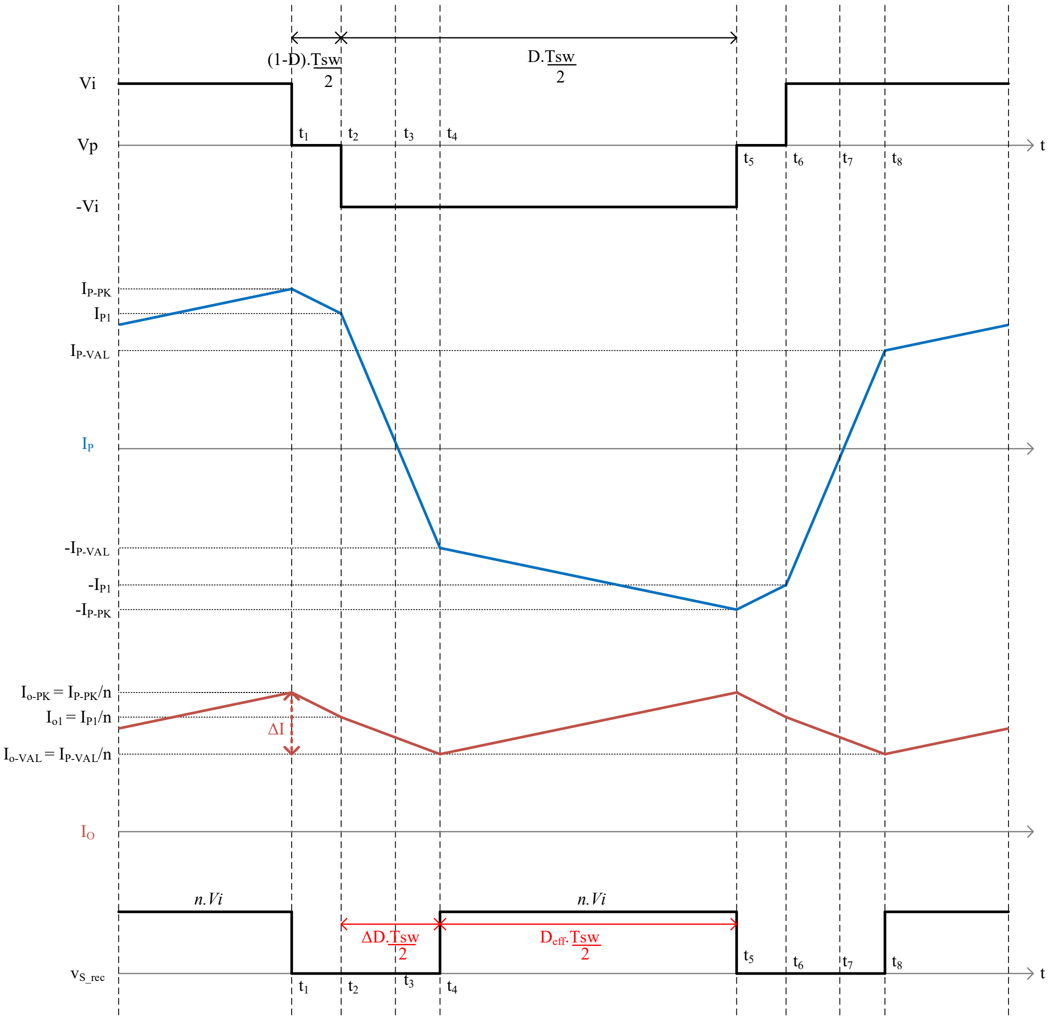


Fig. 4.9. PSFB key waveforms

The PSFB is a buck-type topology, actions on the control variable can only decrease the conversion ratio and thus the transformer ratio is calculated from the maximum output voltage:

$$n = \frac{V_{o,max}}{V_i} = 20.125 \tag{4.14}$$

The gain of the converter is defined from the duty cycle of the AC waveform obtained from the phase shift modulation as can be seen in Fig. 4.9.

$$m = \frac{V_o}{n\,V_i} = D_{eff} \tag{4.15}$$

The main parameters of the circuit are the leakage inductance of the transformer (named L_r here for similarity with the LLC section) and the output filter inductance L_o. The effect of the magnetising inductance is not taken into account at first.

The output inductance is chosen to limit the peak current in semiconductors through the limitation of the current ripple ΔI_o.

$$I_{p\_pk} = n\,(I_o + \frac{\Delta I_o}{2}) = n\left[\frac{P}{V_o} + \frac{V_o\,(1 - D_{eff})}{4\,f_{sw}\,L_o}\right] \tag{4.16}$$

Considering a 1700 V SiC MOSFET power module with 500 A peak current rating (Rohm BSM250D17P2E004) and a design margin of 15% for worst condition (maximum power, lowest output voltage) the output inductor is found to be $L_o = 8$ mH.

The leakage inductance value impacts the ZVS range of the converter. ZVS occurs in both inverter legs when the energy equation below is respected [61]:

$$I_{p\_pk} = n\,(I_o - \frac{\Delta I_o}{2}) \geq \sqrt{\frac{2}{L_r}\,(\frac{4}{3}\,C_{oss}\,V_i^2 + \frac{1}{2}\,C_{wind}\,V_i^2)} \tag{4.17}$$

The MOSFET output capacitance is considered with typical values from the power module described above (C_{oss}=1.7 nF). The transformer primary winding capacitance C_{wind} is neglected here as it is considered much smaller than C_{oss}. The leakage inductance is first considered as $L_r = 5$ µH. With this value, and considering the nominal output voltage, equation (4.17) gives the limit of the ZVS range at P_{max}/1.75. Below this limit, only the leading leg operates in ZVS.

The effective duty cycle D_{eff} (or gain equivalently) is defined from the control variable D (see Fig. 4.9) and the load dependant duty cycle loss ΔD [62]. This duty cycle loss happens because of the limited slope of the transformer current due to the presence of the leakage inductance. It is seen in Fig. 4.9 between t_2 and t_4. The gain can thus be calculated as:

$$m = D - \Delta D = D - \left[\frac{2\,n\,f_{sw}\,L_r}{V_i}\,(\frac{2\,P}{V_o} - \frac{V_o\,(1-D)}{L_o\,2\,f_{sw}})\right] \tag{4.18}$$

This is true under Continous Current Mode (CCM) operation. The PSFB operates in Discontinous Current Mode (DCM) for powers below the threshold of P_{crit} defined as [63]:

$$P_{crit} = \frac{\left(1 - \frac{V_o}{n\,V_i}\right)\,V_o^{\,2}}{4\,f_{sw}\,(L_r\,n^2 + L_o)} \tag{4.19}$$

In DCM the gain is calculated as [63]:

$$m_{DCM} = \frac{D^2\,(n\,V_i - V_o)\,V_o}{4\,f_{sw}\,(L_r\,n^2 + L_o)\,P} \tag{4.20}$$

With the expressions of the gains in both CCM and DCM it is possible to plot the input voltage as a function of the control variable, in a similar fashion as for the resonant topologies. The DCM operation is clearly noticeable when operating at low output power. The duty cycles needed to keep the input voltage at 1200 V become very small because of the square in equation (4.20).

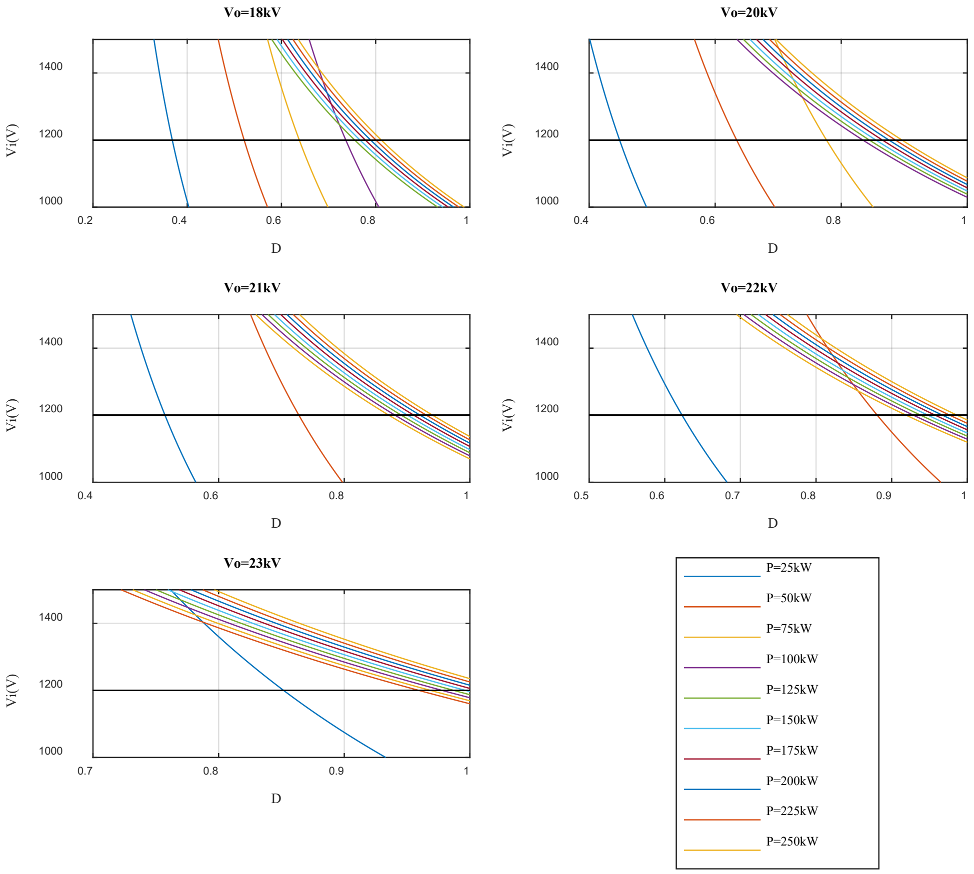


Fig. 4.10. PSFB control space with $L_r = 5$ µH and $L_o = 8$ mH

As for the phase-shift control of the resonant topologies, the peak-to-RMS current ratio increases with increasing phase-shift (decreasing D). The main difference is that in the PSFB case, the small duty cycles are needed for low power levels (while for resonant topologies it is for all power levels). Thus the value of the peak current is not a problem for the semiconductors.

If the PSFB is designed to have a larger ZVS range by increasing L_r, the duty cycle loss becomes a problem as it is not possible to have a high enough duty cycle at the secondary side to achieve the desired voltage ratio. In the following example the leakage inductance is designed to have full ZVS from $P_{max}/2$ to illustrate this issue. In this case, it can be seen from Fig. 4.11 that the input voltage cannot be controlled to 1200 V for the complete voltage and power ranges. The possible solution of increasing the transformer ratio n is not desirable as it would increase the duty cycle loss (equation (4.18)), the peak current (equation (4.16)) and the voltage applied on the diode rectifier (nVi, see in Fig. 4.9).

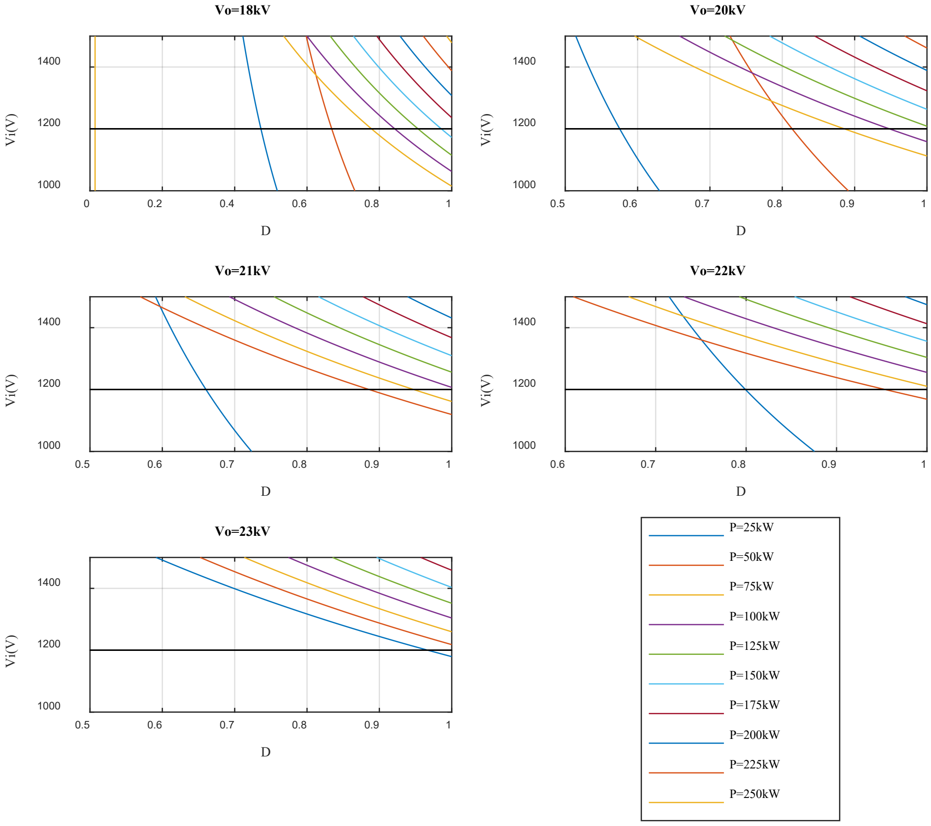


Fig. 4.11. PSFB control space with $L_r = 21.2$ µH to have $P_{zvs}=P_{max}/2$

The solution to increase the ZVS range without increasing the leakage inductance is to use the magnetising current. When the magnetising current is taken into account, the ZVS condition becomes:

$$I_{p\_pk} = I_m + n\,(I_o - \frac{\Delta I_o}{2}) \geq \sqrt{\frac{2}{L_r}\,(\frac{4}{3}\,C_{mos}\,V_i^2 + \frac{1}{2}\,C_{wind}\,V_i^2)} \qquad (4.21)$$

with I_m calculated from the magnetising inductance as:

$$I_m = \frac{D\,V_i}{4\,f_{sw}\,L_m} \qquad (4.22)$$

For the comparison, the magnetising inductance is considered to be 100 times larger than the leakage inductance of 5 µH, resulting in a full ZVS range starting at $P_{max}/2$.

4.1.3. Comparison

For the proposed designs, different operating points are simulated and summarised in the following table, with the relevant consequences of the designs.

Table 4.1. Summary of designs

Design	**$V_{o,min}$ (18kV), $P=P_{max}/2$**	**$V_{o,max(Pmax)}$ (21kV), P_{max}**	**$V_{o,max}$ (23kV), $P_{max}/100$**
LLC L_n=1.36 Q=1.44 Hybrid modulation f_{res}=22 kHz, $f_{n,max}$=1 P_{ZVS}=0 $V_{cr,peak}$=2.6kV	f=22 kHz D=0.71	f=21.24 kHz D=1	f=21.01 kHz D=1
PSFB Phase-shift modulation $P_{ZVS}=P_{max}/2$ $V_{cr,peak}$= N/A	f=20 kHz D=0.765	f=20 kHz D=0.96	f=20 kHz D=0.26

As can be seen in Table 4.1, both the LLC and PSFB topologies can be designed so as to meet the specifications of the PV MVDC collector case study. The phase-shift modulation is the preferred modulation to meet the output voltage variations. In resonant topologies the frequency modulation can still be used in small range to reduce the needed phase-shift. In the PSFB the phase-shift needed to achieve a certain gain is lower (higher D) than in the resonant topologies, leading to smaller peak-to-rms current ratio in the MOSFETs. It is noticeable that the ZVS operation in all power range is achieved for resonant topologies whereas PSFB would not be controllable in the whole power and voltage range if it needed to meet this condition. The comparison of the converters efficiencies will show if this drawback is critical or not regarding the overall converter performance.

4.2. Efficiency comparison

The previously defined topologies are evaluated in terms of losses. The study is realised using PLECS and only semiconductor losses are evaluated first. The other sources of losses are mainly the medium frequency transformer and the snubbers needed for the diode rectifier. One component per type of semi-conductors in the circuit is chosen a priori for the losses evaluation. Few SiC power module models are available and IGBTs are not likely to be competitive at this frequency/voltage/current level. The selection of the power module is thus also motivated by the availability (at the moment of this studied) of a PLECS model of the component. The choice of components for the actual implementation of the converter is discussed in Chapters 6 and 7. The junction temperature of the semiconductors is assumed constant at 125°C.

- Primary bridge MOSFET: 250A 1700V SiC MOSFET power module Rohm BSM250D17P2E004 (includes antiparallel SiC Schottky diode). The PLECS model of the module is given by the manufacturer.
- Rectifier diode: 23A 1700V SiC Schottky diode GeneSiC GB10MPS17-247. The PLECS is given by the manufacturer. The losses calculated for one diode are multiplied by 26 to account for the series connection of diodes necessary to withstand the maximum voltage of 23 kV. We assume the operating voltage of 1700 V diodes to be 900V (this assumption is discussed in Chapter 6).

The losses are evaluated for 3 output voltage levels: 19 kV, 20 kV and 21 kV. The voltages above 21 kV are not considered, as the total power is not transmitted for those voltage levels. The tables presenting the breakdown of losses for all voltages and powers can be found in Appendix 2. The results are summarised in the following figure.

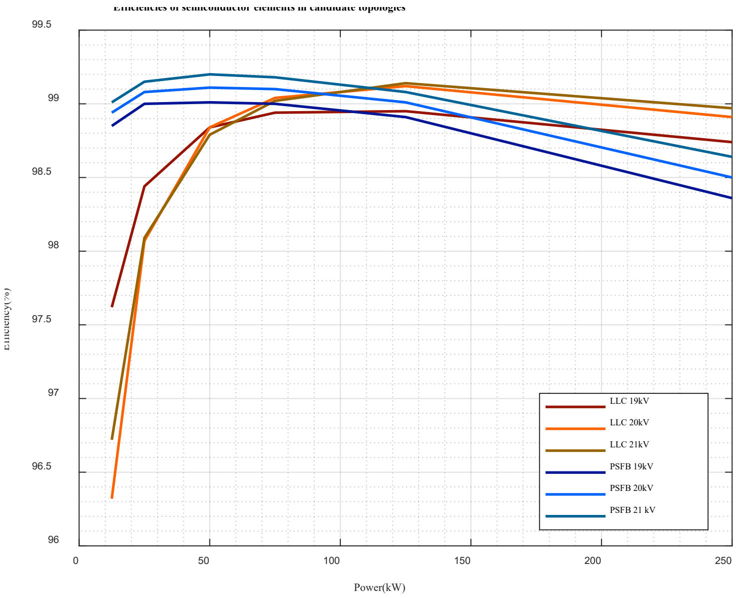


Fig. 4.12. Semiconductor efficiency curves

It can be observed that the PSFB has larger losses at maximum power than the LLC. This can be explained by the fact that at maximum power the turn-off current is high. On the other hand the PSFB efficiency exceeds the LLC at low power levels thanks to its lower magnetizing current. One must note that this downside of the LLC comes from the dimensioning needed to cover the desired gain range with small frequency variations. As seen in Chapter 3, the LLC is particularly efficient for applications with constant voltage ratio and no specific control needed. The high efficiency of the PSFB at low power is also explained by the fact that its ZVS power limit is close to the DCM power limit. Thus, although ZVS is lost for one leg at low power levels, ZCS is achieved in this range for all switches. This is of particular interest for the PSFB, as its turn-off current is higher than its turn-on current.

To compare the losses of both topologies a single indicator is used: the European efficiency. This weighted average is used in the PV industry to evaluate the efficiency of a device receiving varying power of the kind seen with European weather. It was defined previously in Equation (2.3). The following table presents the European efficiencies of the different topologies for the considered voltage levels.

Table 4.2. European efficiencies of the semiconductors at different voltage levels

Voltages (V)	PSFB	LLC
19000	98,83%	98,83%
20000	98,93%	98,89%
21000	99,02%	98,91%

It can be seen that because of the repartition of the coefficients of the weighted average, both topologies have almost the same European efficiency. The PSFB is the slight favourite here. However, one must also factor in the snubber components used for the series connected diodes, which add power-independent losses [64]. In the case of the LLC, the snubbers are only present to balance the voltage between the diodes. In the case of the PSFB, a voltage ringing between the transformer leakage inductance and the diodes junction capacitance also needs to be damped [65]. This topic will be addressed in the next chapters. At this stage, one can simply conclude from the simulation study that neither topology exhibit significant advantage over the other.

Some comments can be made regarding the value of the calculated efficiencies. Indeed, from the specifications given in Table 2.4, the target European efficiency of the step-up DC-DC converter is 99%. However, the efficiencies of the semiconductors alone given in Table 4.2 are below that threshold. To reduce semiconductor losses, it is possible to either connect several modules in parallel, use power modules with larger current ratings or decrease the switching frequency. This will be considered at the implementation stage for the prototype converter. The design of the transformer will also have to be optimised for European efficiency (repartition between core and winding losses) in order to comply with the objectives. The implementation of such a converter is discussed in Chapter 7.

As it is not possible to find a clear favourite topology from the losses comparison alone, another criteria must be compared. The studied DC-DC converter is intended to be connected to a network, so its operation during faults such as output short-circuit, is of critical importance. A second comparison factor is thus proposed below: the response to faults occurring on the MVDC network.

4.3. Fault behaviour

When connected to a collection network, converters do not only have to operate at their nominal voltage with the highest efficiency. They also have to survive fault conditions, without adding unbearable burden on the network components. An example of such fault which may occur is a pole-to-pole short circuit on the MVDC line.

This sections investigates the behaviour of both topologies when a fault happen at their output. Indeed, the downside of having a simple passive rectifier made of diodes is that no control action can be taken on the MV side in case of network faults. Once the low-voltage bridge is blocked, the only elements of the circuit affecting the fault response are the filter components. The fault response of the PSFB is studied here and compared to that of a single active bridge (SAB). The SAB is comparable to the PSFB, with the noticeable difference that it only has a capacitor C_o across its output whereas the PSFB has an inductor and a capacitor L_oC_o. The SAB represents here the family of converter having an only capacitive output filter. It is selected over the LLC for this comparison because of the ease of experimental validations. The PSFB ans SAB can be implemented from the same hardware, with a modification of the circuit. The resonant topologies (SRC and *LLC*) have similar output filters and thus should have similar responses under MVDC faults to the SAB. A variant of the SAB, with an additional inductor on the MV network side L_{ext} as in presented in the state of the art (CAS in Table 3.1), is also studied.

4.3.1. Simulation

The results shown in this section have been published in [31].

The electromagnetic transient simulation models were developed to support the analysis of the DC-DC converter in the case study MVDC network as presented in Fig. 4.13. The model is suitable for the analysis of DC-DC converter under faults in the MVDC network. The PSFB and SAB main design parameters used in this section are presented in Table 4.3.

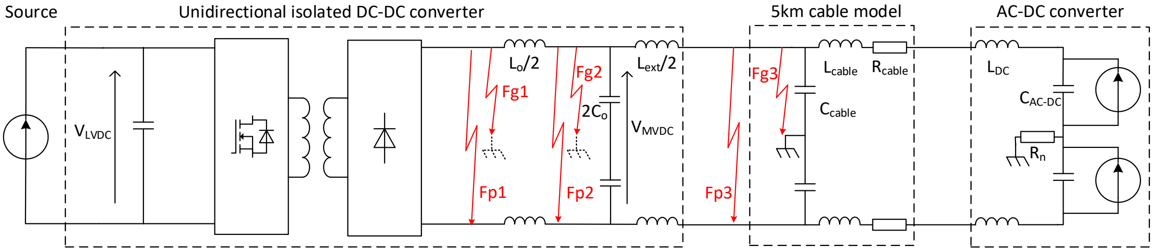


Fig. 4.13. Simulation model of the MVDC network with: DC-DC converter (detailed switched model), cable (π model) and AC-DC converter (average model). Fault cases defined in Table 4.5 are visualized.

Table 4.3. Design parameters of the selected DC-DC converters.

	Input capacitor	**MFT frequency**	**MFT turns ratio**	**MFT leakage inductance**	**Filter inductor**	**Filter capacitor**
PSFB	C_{in} = 250 µF	f = 20 kHz	m = 20.125	L_f = 5 µH	L_o = 8 mH	Co = 100 pF
SAB					NA	
SAB-L					L_{ext} = 8 mH	

A detailed switched model [66] of the DC-DC converter was used. The MV diode bridge is modelled with an equivalent diode with a forward voltage drop of 25.7 V and an on-state resistance of 30.4 mΩ. These values correspond to the series connection of silicon carbide (SiC) Schottky diodes [67]. The LVDC source is modelled with a current source controlled to deliver the nominal power. The 5 km cable section is represented by a π model (Table 4.4). The AC-DC converter is represented by the average model [66] which is detailed in [68] (Table 4.4).

Table 4.4. Design parameters of the MVDC cable and AC-DC converter.

Cable	
R_{cable}	8.8 mΩ/km x 5 km
L_{cable}	134 µH/km x 5 km
C_{cable}	1.81 µF/km x 5 km

AC-DC converter	
R_n	1 kΩ
L_{DC}	500 µH
$C_{AC\text{-}DC}$	1.8 mF

The fault cases are summarised in Table 4.5. The short circuit is modelled by a simple switch with internal resistance of 10 mΩ. The fault occurs at 0.04 s. The LV inverter bridge is blocked 5 µs after the fault instant, considering that the protection triggers due to overcurrent or overvoltage. In order to discard the influence of the AC-DC converter control on the analysis of DC-DC converter, its current reference is brought down to 0 A after 5 µs. The focus of this section is to study the influence of the output filter configuration on the diode rectifier bridge current during faults. All simulation results for the fault cases defined in Table 4.5 are presented in Appendix 4.

Table 4.5. Definition of fault cases.

Name	**Description**
Fp1	Pole-to-pole fault in the diode rectifier
Fg1	Pole-to-ground fault in the diode rectifier
Fp2	Pole-to-pole fault in the output filter
Fg2	Pole-to-ground fault in the output filter
Fp3	Pole-to-pole fault at the DC-DC converter terminals
Fg3	Pole-to-ground fault at the DC-DC converter terminals

The most severe fault case for the diode bridge is found to be the pole-to-pole fault at the DC-DC converter terminals (Fp3). This is also the essential pole-to-pole fault for studying converter safety, as in the cases of fault inside of the converter the rectifier survival is of lower importance. Fig. 4.14 shows a zoom at the time right after the fault instant for the Fp3 case.

In the SAB the diode current peaks above 1000 A because there is no inductor to limit the current. Such high current, even for a short time, would require a significant oversizing of the diode bridge to prevent its destruction. Indeed, the diode selected previously is rated for non-repetitive peak forward surge current of 750 A for a case temperature of 25°C. This case temperature is quite unrealistic and the actual surge current capability would be even lower. One can observe that the high current in the SAB is the result of voltage oscillations due to the discharge of output capacitance. The voltage polarity is reversed, forward-biasing the diodes. In the SAB-L the current does not reach high values as the L_{ext} inductor limits the capacitor discharge and there is no voltage polarity reversal. In the PSFB case, the oscillations are still present but they do not result in important current in the diodes thanks to the filter inductor L_o.

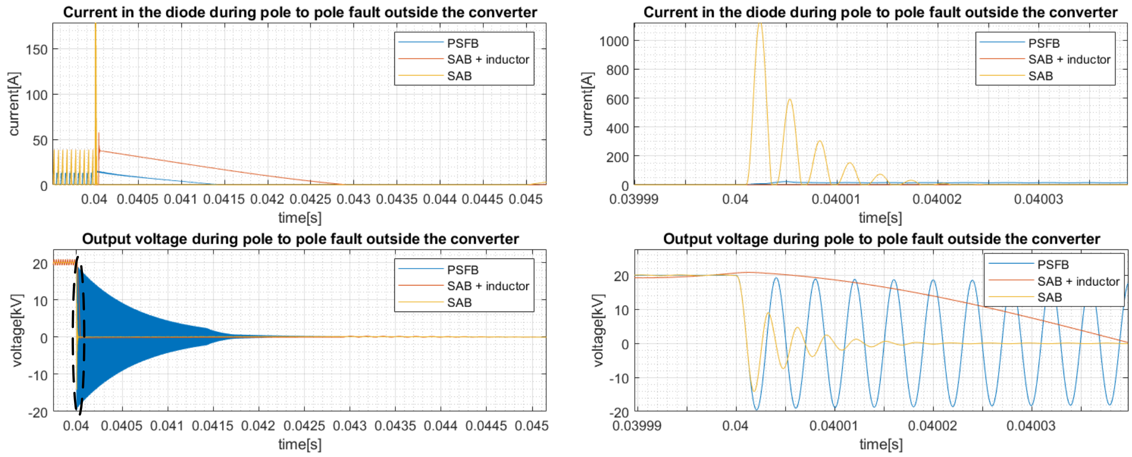


Fig. 4.14. Fault instant for the case Fp3, right) temporal zoom in the circled area, top right) amplitude dezoom to see the current peak value in the SAB

One must note that the same filter capacitor C_o was used for each DC-DC topology. For SAB and SAB-L, this results in a larger nominal output voltage ripple than in the PSFB, as there is no DC inductor inside the converter to reduce the current ripple. In order to have a similar voltage ripple in all topologies, the output capacitor would have to be increased for the SAB and SAB-L. In case of fault, this would result in even higher diode current due to capacitor discharge. The PSFB filter inductor fulfils both the role of current ripple filtering and fault current limitation.

4.3.2. Experimental validation

The behaviours observed in simulation in the previous paragraphs must be checked experimentaly. The experimental set-up described in Appendix 3 is used for test. The PSFB input is supplied by the DC power source and its output is connected to a short-circuiting switch (Fig. 4.15). A 640 Ω load is connected to ensure proper converter operation before the short circuit instant.

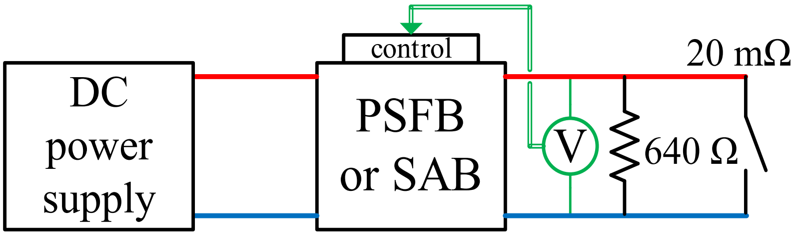


Fig. 4.15. Test set-up for fault response study

The fault response of the PSFB and SAB converters is tested by creating a low resistance (20 mΩ) short-circuit at output terminals as shown in Fig. 4.15. Experimental results are presented in Fig. 4.16.

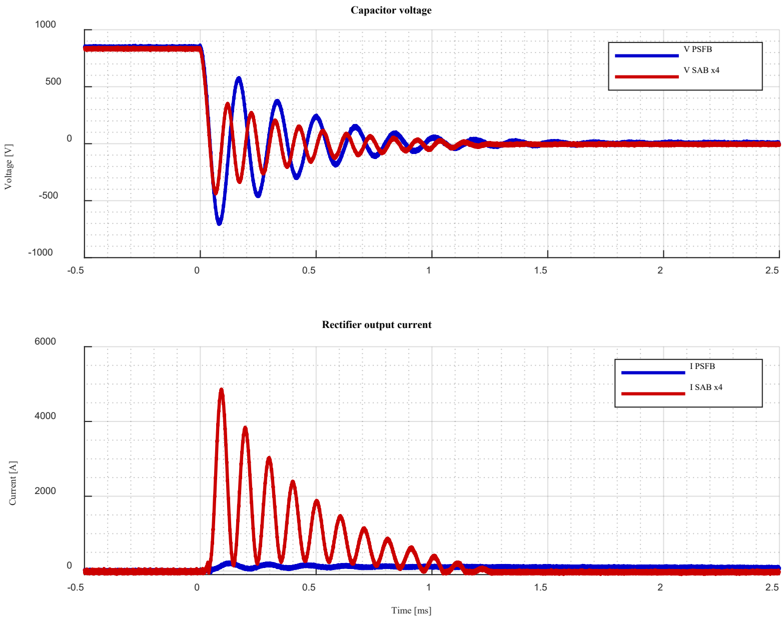


Fig. 4.16. Experimental waveforms of output capacitor voltage and rectifier output current of PSFB (blue) and SAB (red) after an output short-circuit at 800 V (200 V scaled to 800 V for SAB)

The output voltage is controlled at 800 V for the PSFB and 200 V for the SAB before closing the short-circuiting switch. The test voltage of the SAB was reduced to 200 V to avoid any damage to the rectifier bridge. The primary bridge is stopped shortly (≈5 µs) after the fault is declared for the primary bridge not to contribute to the short-circuit current. In Fig. 4.16 the voltage and current of the SAB are scaled to 800 V.

Experimental results show the same phenomenon of voltage reversal leading to forward-biaising of rectifier diodes as presented in simulations. The peak value of the SAB rectifier output current is 4.8 kA for an output voltage of 800 V. The current decreases back to 0 A in 1.2 ms. To withstand such a current pulse, the output rectifier would need to use diodes with significantly larger ratings.

4.3.3. Conclusions on fault behaviour

Three unidirectional step-up, isolated and monolithic DC-DC converter topologies were investigated focusing on the output filter design (*LC* for the PSFB, *C* for the SAB or *CL* for the SAB-L). The simulation model of the case study MVDC network and the DC-DC converters was presented. Six fault scenarios were defined including pole-to-pole and pole-to-ground faults within the DC-DC converter. The most critical case was presented, focusing on the fault current in the diode rectifier bridge (which appears to be the most demanding parameters during faults).

The most severe fault case was found to be the pole-to-pole fault at the DC-DC converter terminals. MVDC voltage polarity reversal occurs, forward biasing the rectifier bridge diodes. Pole-to-ground faults result in low fault current due the high value grounding resistance. The PSFB was observed to offer the best performance in fault conditions. The PSFB output filter inductor fulfils both the role of current ripple filtering and fault current limitation.

4.4. Chapter conclusion

The efficiency comparison has shown that although resonant topologies have higher efficiencies at peak power, their European efficiency is similar to that of the PSFB. This is due to the fact that resonant topologies are particulary well suited to fixed voltage ratio applications, which is not the case here.

A more decisive factor is the behaviour of the converter in cases of faults on the MVDC network. Indeed, this is highly important for such a grid connected converter. Simulation and experimental results have shown the benefits of having an inductor on the MV side in the PSFB topology. This inductor limits the current free-wheeling through the diodes during pole-to-pole faults. The current level observed in the case of a simple capacitive output filter (SAB, similar output filter as LLC) would be destructive for the rectifier. Considering these points, the PSFB topology is selected for further studies in the case study application.

This chapter has shown the PSFB to be the favourite topology regarding fault behaviour, while keeping a European efficiency on par with the resonant topologies for the case study. However, the PSFB has been historically used mostly to supply power loads. The next chapter proposes control principles specific to the PV MVDC application.

5. Control of the PSFB for the PV MVDC application

The PSFB has mainly been used to supply power loads so far. The scientific literature does not address its control principles in the case of a connection to an MVDC grid. Such control principles are thus developped here for both nominal and fault operation. This work has been published by the author in [69], [70].

This chapter proposes control principles for nominal operation and fault cases of an MVDC network-connected PSFB. In nominal operation, the PSFB must regulate its input voltage to a constant level as parallel MPPT converters individualy control their own input voltage (PV voltage). Control principles for fault and low voltage ride through events are also proposed. The PSFB must continue to supply current during the event in order to identify the fault and be ready to restart power transfer as soon as the event is finished.

First, a model of the PSFB is developed considering input voltage control. Tuning equations for the the input voltage control are given and tested in both simulations and small scale experiments. Control principles for Fault Ride Through (FRT) are proposed, taking into account the operation of the MPPT converters. These principles are tested and validated in simulation.

5.1. PSFB average model

In a first approximation, by neglecting the leakage inductance of the transformer, a PSFB can be seen as an isolated buck converter as demonstrated in [34]. From this buck analogy, we infer the average model presented in Fig. 5.1.

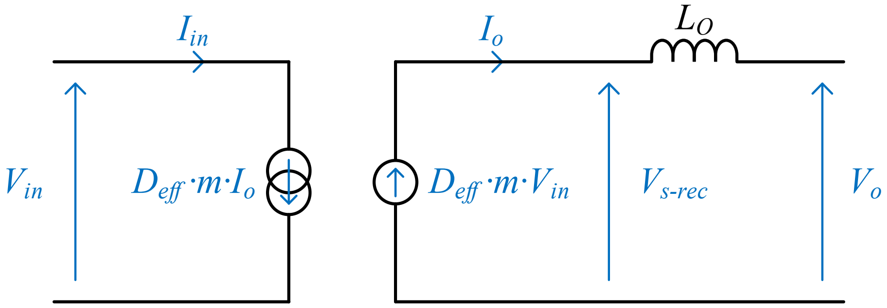


Fig. 5.1. Average model of the PSFB based on buck equivalence

However, this average model features a control variable (D_{eff}) that is not the duty cycle of the primary voltage D, but the duty cyle of voltage at the transformer secondary and therefore cannot be controlled directly. To overcome this limitation, a series resistor is added to the DC output to represent the RMS voltage drop across the leakage inductance. Its expression is derived from the duty cycle loss expression presented in [71]:

$$\Delta D = \frac{2mL_{lk}f}{V_{in}}\left(2I_o - \frac{V_o}{L_o}(1-D)\frac{1}{2f}\right) \tag{5.1}$$

where m is the turns ratio of the transformer, L_{lk} is the leakage inductance of the transformer, f is the switching frequency, V_{in} is the input voltage, I_o is the output current, V_o is the output voltage and L_o is the output inductor. From (5.1), we find:

$$D = D_{eff} + \frac{4mL_{lk}f}{V_{in}} I_o + \frac{mL_{lk}}{V_{in}} \frac{V_o}{L_o}(D-1) \tag{5.2}$$

In this expression, as long as L_o is much larger than mL_{lk}, the last term is negligible. If we define the equivalent resistance according to [62] as:

$$R_d = 4m^2 L_{lk} f \tag{5.3}$$

then we get:

$$DmV_{in} \cong D_{eff} mV_{in} + R_d I_o \tag{5.4}$$

The conservation of power yields:

$$I_{in} = DmI_o - \frac{R_d}{V_{in}} {I_o}^2 \tag{5.5}$$

The average model including the equivalent resistance and the control variable D is represented in Fig. 5.2.

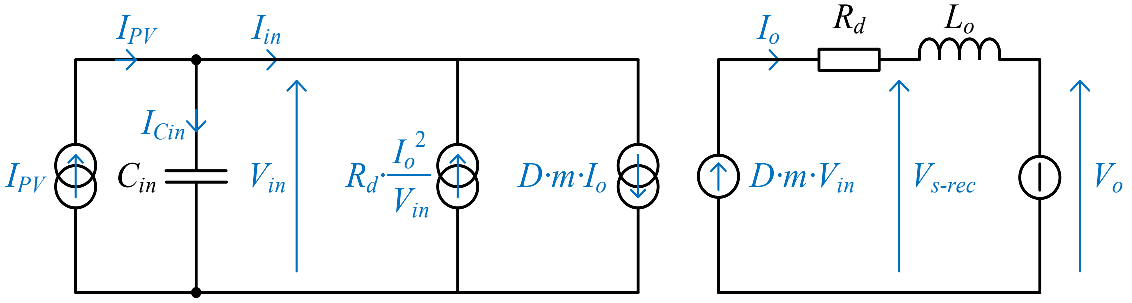


Fig. 5.2. Average model of the PSFB for input voltage regulation

The non-linear model is expressed as below, with g the non-linear function of states $\boldsymbol{x} = [I_o, V_{in}]$ and control input $u = D$, and f the function of disturbances $\boldsymbol{d} = [V_o, I_{PV}]$.

$$\dot{\boldsymbol{x}} = \mathrm{g}(\boldsymbol{x}, u) + \mathrm{f}(\boldsymbol{d}) \tag{5.6}$$

$$\begin{bmatrix} \dot{I_o} \\ \dot{V_{in}} \end{bmatrix} = \begin{bmatrix} -\frac{R_d}{L_o} I_o + \frac{m}{L_o} V_{in} D \\ -\frac{m}{C_{in}} I_o D + \frac{R_d}{C_{in}} \frac{{I_o}^2}{V_{in}} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L_o} V_o \\ \frac{1}{C_{in}} I_{PV} \end{bmatrix} \tag{5.7}$$

With steady-state values, for V_{inS} set to the voltage reference:

$$\dot{x_S} = f(x_S, u_S) = 0 \tag{5.8}$$

$$\overline{I_{o_S}} = \frac{mV_{inS} D_S - V_o}{R_d} \tag{5.9}$$

$$D_S = \frac{V_o^2 + I_{PV} R_d V_{inS}}{V_o m V_{inS}} \tag{5.10}$$

The linearisation of the system around the operating point in steady state allows getting the transfer function $H_2(s)$ that links the input voltage to the duty cycle. This transfer function (5.11) has stable poles and zeros.

$$\begin{aligned} H_2(s) &= \frac{\widetilde{V_{in}}(s)}{\widetilde{D}(s)} \\ &= \frac{-m{V_{in_S}}^2\left(mV_{in_S}D_S - R_d I_{o_S} + L_o I_{o_S}\cdot s\right)}{\left(mV_{in_S}D_S - R_d I_{o_S}\right)^2 + R_d\left(C_{in}V_{in_S}^2 + L_o I_{o_S}^2\right)\cdot \mathrm{s} + C_I L_o {V_{in_S}}^2\cdot \mathrm{s}^2} \end{aligned} \tag{5.11}$$

A parametric analysis of the value of the leakage inductance is presented in Fig. 5.3. One can observe the influence of the leakage inductance value on the damping of the resonance (visible for L_{lk}=1 µH). Indeed, this inductance is modeled as a resistance on the dc side, damping the $C_{in}\,L_o$ circuit.

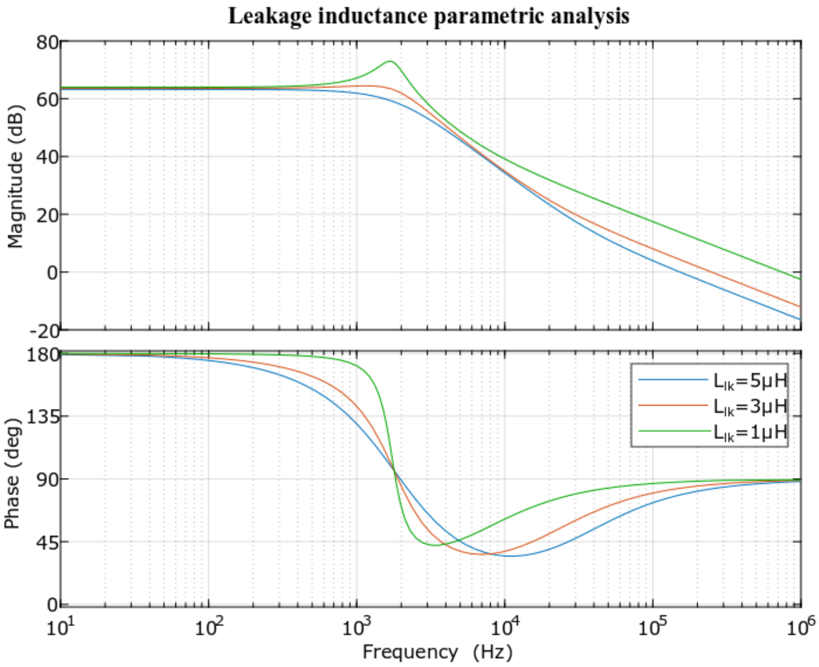


Fig. 5.3. Bode diagram of PSFB transfer function H2, with parameters from Table II and different values of leakage inductance L_{lk} =5 µH (blue), L_{lk} =3 µH (red), L_{lk} =1 µH (green)

From equation (5.3) describing this resistance R_d, one can also understand that the resonance is unlikely to appear for a high conversion ratio m. Indeed, a high conversion ratio would coincide with larger leakage inductance because of the increased insulation distances, ultimately resulting in even larger R_d.

5.2. PSFB input voltage control

The proposed control scheme is compliant with the simplicity of the unidirectional MV converter. Indeed, the only measured quantity is the voltage at the LVDC side and no sensor on the MV side is necessary. The closed-loop control system is depicted in Fig. 5.4 with $H_2(s)$ the converter transfer function and Gc the control transfer function. One should notice that the error signal e is computed from the measured value minus the reference, as the duty cycle should be increased to extract current from the input capacitor when the input voltage has to be decreased.

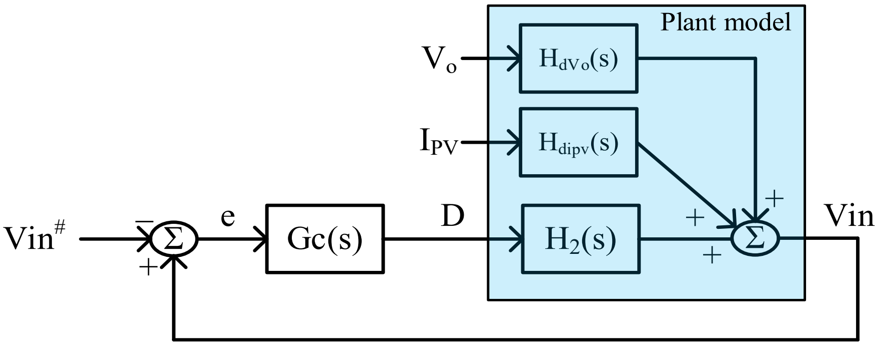


Fig. 5.4. PSFB input voltage control diagram, with disturbances V_o and I_{PV}

5.2.1. Controller tuning for the PSFB input voltage regulation

In [72] the authors propose a method to tune a Proportional Integral controller by setting the closed loop crossover frequency at 25 times the open loop crossover frequency. However, depending on circuit parameters and the cycle time of the controller, it is not always possible to include the resonance in the closed-loop bandwidth. If the open-loop transfer function crosses the zero gain axis around the resonance frequency shown in Fig. 5.3, the phase margin will be too small and the control would be prone to instability.

The PI controller is defined as:

$$G_c(s) = K_p(1 + \frac{\omega_I}{s}) \tag{5.12}$$

with K_p the proportional part and ω_I integral part of the PI controller.

The proportional gain of the PI controller is obtained by keeping the maximum of the converter transfer function below -6 dB (twofold margin). K_p is therefore obtained by:

$$K_p = \frac{1/2}{\max(|H_2(\omega)|)} \tag{5.13}$$

The integral part of the controller takes the form of a pole at the origin and a zero at a low frequency.

$$G_I = \frac{s + \omega_I}{s} \tag{5.14}$$

The zero is calculated to allow the gain of the open loop transfer function to become positive at the crossover frequency ω_c:

$$\omega_I = \omega_C \sqrt{\frac{1}{(|H_2(\omega_c)| \cdot K_P)^2} - 1} \tag{5.15}$$

A low crossover frequency ω_c is chosen when the transfer function H_2 exhibits a resonance, so the integral part does not influence the gain at the resonant frequency. For designs not exhibiting resonance, the previous equation can still be used, with the controller cycle time as the only restriction on crossover frequency.

5.2.2. PSFB input voltage regulation validation in simulation

The control is first tested in simulation using Matlab-Simulink. The PI controller on the input voltage is tuned following the method described in equations (5.13) and (5.15). For the design given in Table 4.3, the transfer function does not exhibit any resonance. Thus, the PI parameters can be calculated for a high cut-off frequency (see Table 5.1, full scale). The converter is tested with two typical disturbances expected in operation: an input power variation (variation of I_{PV}) and an output voltage variation. The results are displayed in Fig. 5.5. A power step from 0.5 p.u. to 1 p.u. is applied. The input voltage is regulated, with an overshoot at 1230 V (2.5%). An output voltage step from nominal to maximum (1.1 p.u.) is then applied. The input voltage is again regulated, with an overshoot at 1253 V (4.4%). One should note that such rapid step variation of power or voltage is not expected in the real application.

Table 5.1. PI controller parameters for the full-scale converter (simulations) and for the reduced-scale (experimental)

Parameter	**Full scale**	**Reduced scale**
Cut-off frequency f_c	1000 Hz	50 Hz
Proportional term K_p	3.45e-04	2.6e-04
Integral term ω_i	1.32e+04 rad/s	1669 rad/s

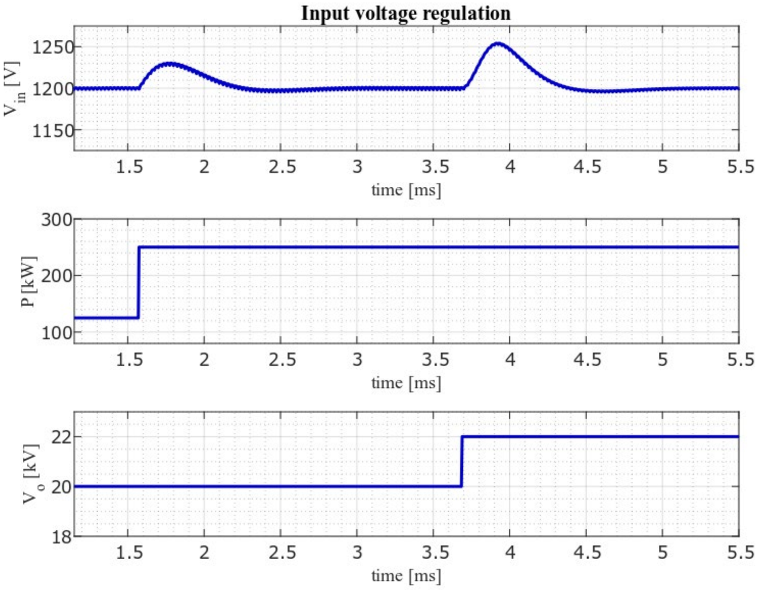


Fig. 5.5. Simulation of input voltage regulation under step changes of power and output voltage

5.2.3. Experimental validation of the PSFB control

To demonstrate the PSFB topology and control in a PV MVDC collection network experimentally, a reduced-scale system is set-up. The test bench is composed of two DC-DC converters, a DAB and a PSFB in a back-to-back configuration, with a DC power supply compensating for the losses of both converters (Fig. 5.6). The test bench is controlled and monitored by a Speedgoat real-time target and programmed through Matlab Simulink Real-Time using rapid control prototyping (RCP). The converters parameters are summarised in Table 5.2. The set-up is described in details in Appendix 3.

Table 5.2. PSFB test bench components

Parameter/Component	**Value**
Input voltage V_{in}	350 V
Output voltage V_o	600 V
Operating power P	30 kW
Switching frequency f	20 kHz
Input / Output capacitor C_{dc}	160 µF
MFT turns ratio m	2
MFT leakage inductance L_{lk}	3 µH
Switches M_x	1.7 kV, 8.0 mΩ SiC Half Bridge Module CAS300M17BM2
Snubber capacitor C_{snub}	33 nF
Snubber resistor R_{snub}	33,3 Ω
Output inductor L_o	200 µH

In this setup, the DAB acts as the MPPT by regulating its output power, while the DC power supply represents the MVDC network and sets the PSFB output voltage. The PSFB control regulates its input voltage, ensuring the power transfer from the DAB (MPPT) to the DC power supply (MVDC network).

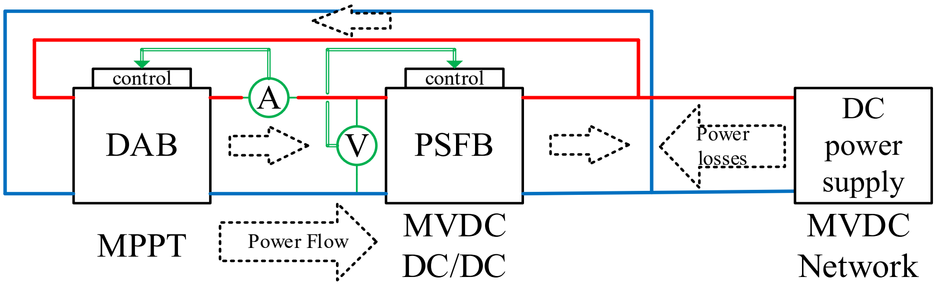


Fig. 5.6. Test bench set-up block diagram including the DAB, PSFB and dc power supply, with the PV MVDC collection network equivalents (MPPT, PSFB unidirectional isolated DC-DC converter and MVDC network)

The PI regulator on the input voltage is tuned following the method described in equations (5.13) and (5.15) for the parameters given in Table 5.2. For these values, the transfer function exhibits a pronounced resonance at 1520 Hz (Fig. 5.7). Thus, a slow controller with low ω_C is chosen (cut-off frequency 50 Hz) to ensure sufficient phase-margin (see Table 5.1, reduced scale). It is seen in Fig. 5.7 that the gain margin Gm is infinite in this case as the phase never reaches -180°. The phase margin Pm=103° is largely sufficient to ensure stability.

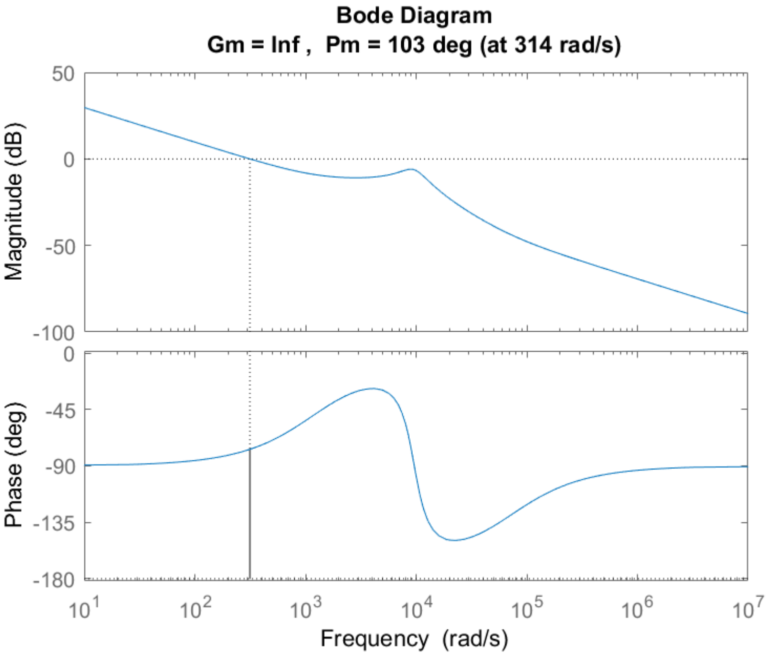


Fig. 5.7. Bode diagram of open loop transfer function of controlled system for reduced scale converter tuned for a cut-off frequency of 50 Hz with gains from Table 5.1 (reduced scale) and parameters from Table 5.2, with gain margin Gm and phase margin Pm.

The control performances of the converter are evaluated in the occurrence of realistic power and output voltage variations: solar irradiance measurements of a variable weather day in Varennes, Canada on the 17/07/2014 are taken from [21] and scaled to the test bench power. The high sampling rate of these data (up to 1 ms) enables a good reproduction of real PV dynamics (see Fig. 2.16). This power profile is reproduced by the DAB converter which regulates the power in the back-to-back configuration and mimics the MPPT in the target application. The DC supply voltage is also changed arbitrarily throughout the test. This represents voltage variations in the MVDC network. Experimental results are shown in Fig. 5.8.

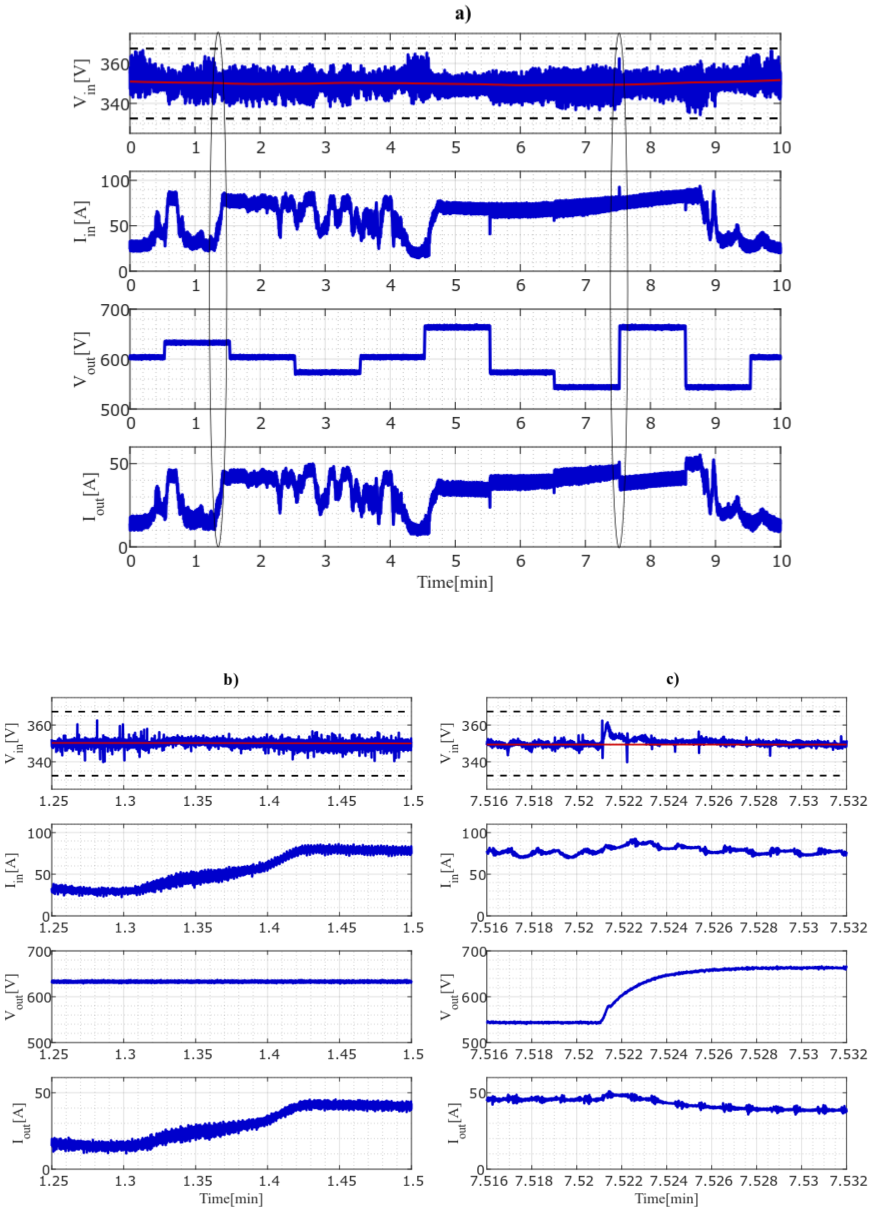


Fig. 5.8. Experimental waveforms: a) Input voltage V_{in} regulated to 350 V, input current I_{in} following the PV profile for maximum power of 30 kW, output voltage V_{out} = 600 V with step variations in the range ±10 % of output voltage, output current I_{out}. b) Zoom on input current change from 30 A to 80 A. c) Zoom on output voltage change from 540 V to 660 V.

One should note that this experimental validation is considered the worst case in terms of control compared to the full-scale system. Indeed, the presence of a non-damped resonance in the system results in the tuning of the controller with a low cut-off frequency, which translates to a slow response of the controller. Yet, it is observed that the input voltage is regulated to the target value of 350 V during the whole test with a maximum deviation of 5% when faced with an output voltage variation of ±10% at 400 V/s together with an input power varying from 6 to 30 kW with a time dynamic which replicates a day with a very variable irradiance. The regulation of the input voltage under these variations of input power and output voltage shows the reliability of the control for a wide variety of operating points.

5.3. PSFB control under MVDC fault

Any electrical equipment must comply with regulations and standards. Fault ride-through (FRT) is one of the requirements applicable to grid-connected generators. FRT ensures that in case of a fault in the network, the power system remains stable. While the network protection clears the fault, power generators stay connected so they restart as soon as the voltage is back in the network.

5.3.1. MVDC Fault ride-through requirements

The FRT requirement applies to AC grid-connected converters, including PV. The converter must stay connected in the event of a dip in the AC grid voltage. The voltage levels, time to recover full production, and voltage ramp differ according to local regulations [25]. Fig. 5.9 gives an example of the French DSO Enedis FRT profile [26]: after a voltage dip, the power generation of a unit must come back to its prior level as quickly as possible once voltage has recovered 85% of the nominal grid voltage. It is recommended that the converter provides some reactive current during the FRT.

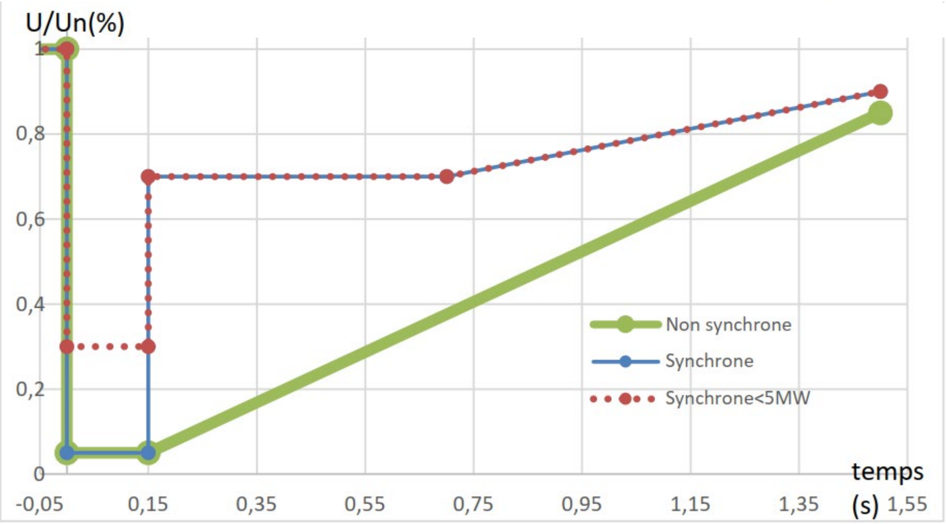


Fig. 5.9. FRT profile defined by the French DSO Enedis [26]

The regulations and standards for DC networks, including MVDC, are still under construction. One can expect that they will be similar to those of AC networks. In this section, it is assumed that the MVDC FRT profile is the same as in AC (Fig. 5.9).

The FRT profile depends on the protection strategy of the MVDC network. In the case of an MVDC short circuit, all generators, converter-interfaced AC grid, and capacitors contribute to the fault current which rises rapidly [24]. It was proposed in [68] the protection of radial MVDC network based on a single DC circuit breaker (DCCB) and multiple DC fuses (Fig. 5.10). This scheme is considered here as it is close to the existing AC protection schemes from which the FRT is taken.

An example of a situation that requires the DC-DC FRT is in the case of a DC pole-to-pole short circuit at MVDC terminals of the DC-DC 2 (Fig. 5.10). During the FRT profile (Fig. 5.9), it is assumed that the DC-DCs should all provide some current so the DC-DC 2 fuse blows and disconnects the faulty branch. The value of the current during the FRT profile is expected to be ≤1 p.u.. The DC-DCs and DC-AC remain connected during the transient voltage dip and should restart the power transfer as soon as the MVDC voltage is back.

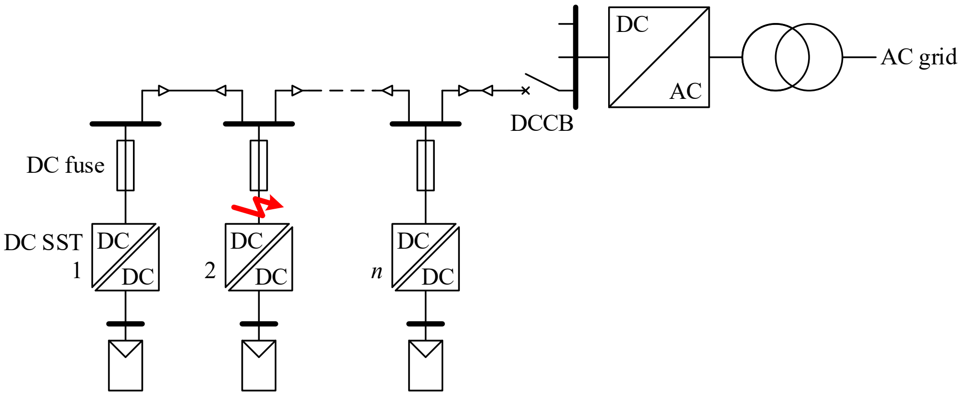


Fig. 5.10. Protection of radial MVDC network based a single DC circuit breaker (DCCB) and multiple DC fuses [68]. An example DC pole-to-pole fault location at MVDC terminals of DC-DC 2 is presented.

5.3.2. Control of the DC-DC converter for MVDC Fault ride-through

The structure of the converter multiple boost converters and a single isolated unidirectional step-up DC-DC converter is recalled in Fig. 5.11. Fig. 5.12 shows the circuit diagram of each converter and provides the definition of the quantities used for the control.

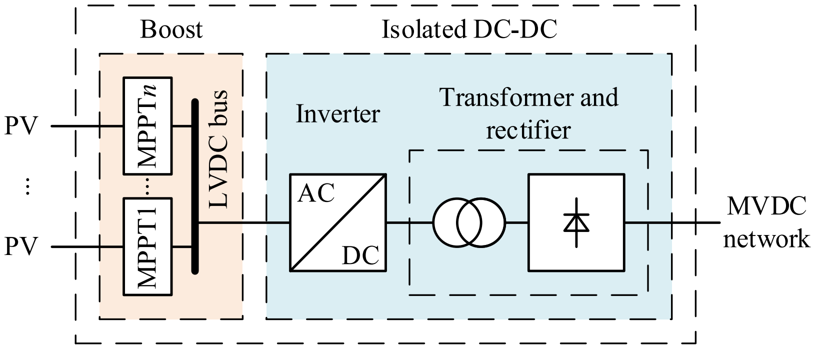


Fig. 5.11. DC-DC converter for MVDC PV application including multiple boost converters and a single isolated unidirectional step-up DC-DC converter.

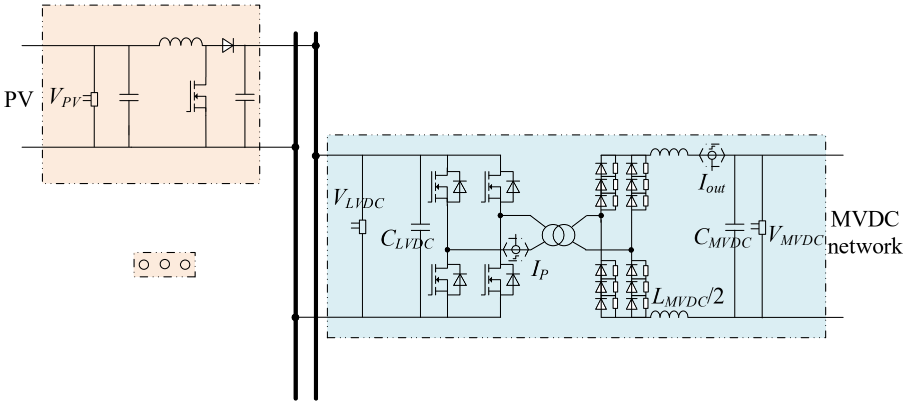


Fig. 5.12. Circuit diagram of the boost and isolated DC-DC converter, with the definition of controlled quantities.

The control structure of the DC-DC is separated between a normal operation mode and an FRT mode as presented in Fig. 5.13. The switch between the modes is triggered by an under-voltage detection function. The FRT mode is activated when the MVDC network voltage is lower than 0.85 p.u. In each mode, the boost converters and PSFB have distinct roles:

- In the normal operation mode, the MVDC network voltage V_{MVDC} is controlled to a constant value by the central inverter. The PSFB regulates the LVDC bus voltage V_{LVDC} to a constant value, with disturbances from MVDC voltage and PV power variations. The boost converters achieve the MPPT function by adjusting their input voltage V_{PV} individually.
- In the FRT mode, the control roles are reversed. The boost converter now regulates the LVDC bus voltage V_{LVDC} to a constant value. As explained in the Fault Ride Through requirements, the PSFB is expected to regulate its output current I_{out} close to its nominal value. This may not always be possible as the available PV power may not be sufficient to maintain a constant LVDC bus voltage and the nominal output current at all times. Thus, a maximum current tracker is implemented to generate the reference to the current controller. This ensures that the PSFB is controlling its output current as close as possible to its nominal value, while not interfering with the LVDC bus voltage control.

During the initial phase of the FRT, the decrease of the PSFB transformer secondary voltage leads to a fast rise of the primary current I_p (Fig. 5.12) during the transition period, where it is only limited by the leakage inductance of the transformer. The current dynamics of I_p during this period make it impossible to control, and an overcurrent detection is thus necessary to protect the PSFB inverter. It is considered that this function is done by a desaturation protection [73] included in the gate drivers. The control pulses are stopped for N_{sw}=5 switching periods when the protection is triggered. The current is still flowing at the secondary side because of the free-wheeling phenomenon described in section 4.3 involving the output inductor L_{MVDC} and capacitor C_{MVDC} (Fig. 5.12).

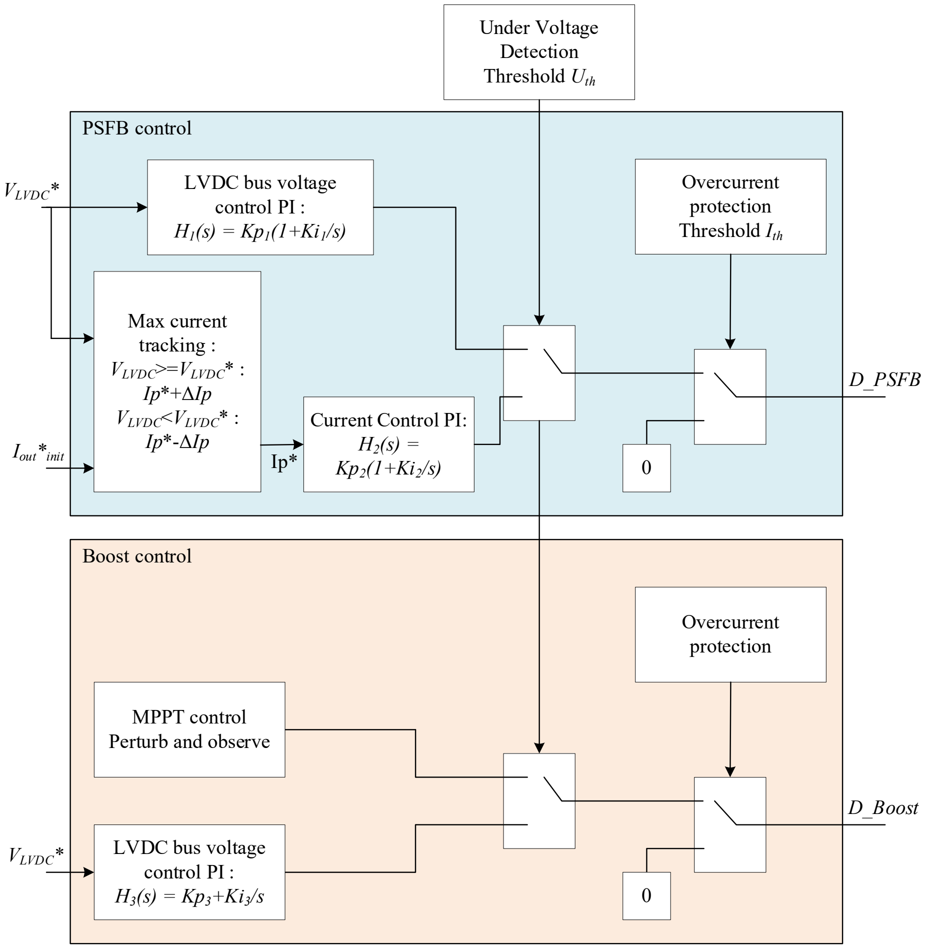


Fig. 5.13. Control structure synoptic of the complete converter including Boost and PSFB converters

The PSFB LVDC bus voltage regulation is presented in detail in section 5.2. The PI controller is tuned according to the presence of resonance in the transfer function of the system, dictated by the voltage ratio and leakage inductance of the transformer.

The PSFB current control is done with a PI controller based on the RMS current measured at the primary of the transformer I_P. A maximum current tracking function is added in order not to discharge the LVDC bus capacitor during an FRT event coinciding with low irradiance on the PV. Once the LVDC bus voltage drops below the reference level, the current control reference is incrementally decreased until the bus voltage can be maintained to its reference by the boost converters LVDC bus voltage control.

In normal operation, the MPPT control of the boost converter regulates the PV voltage so as to optimise the extracted power. The search for the voltage corresponding to this maximum power can be done through different algorithms largely discussed in the literature [6]. The “perturb and observe” algorithm [5] is selected for this particular implementation of the MPPT function.

In FRT mode, the LVDC bus voltage control of the boost converter is done with a PI controller tuned so as to be slower than the current control of the PSFB, thus avoiding instabilities. In practice, the bandwidth of the Boost LVDC bus voltage control is tuned to a third of that of the PSFB current control.

5.3.3. Fault ride-through control validation in simulation

A simulation model is developed under Matlab Simulink Simpower System. The MVDC network is modeled with a voltage source, controlled to follow the FRT profile. The MPPT boost converter is modeled by a controlled current source, with a saturation corresponding to the maximum PV power available. The control of the boost converter acts on the reference current of this source. The PSFB converter is modeled in detail with its switching components. The profile presented in Fig. 5.9 is accelerated (the entire event fits within 14 ms) to keep a reasonable simulation time using the switching model. The main parameters used for the simulation are given in the table below.

Table 5.3. Parameters used in the simulation

MVDC network	P_{MVDC}=20MW	V_{MVDC}=±10kV	
DC-DC	$P_{DC\text{-}DC}$=250 kW	V_{PVoc}=1.5 kV	C_{LVDC} = 250 µF L_{MVDC} = 8 mH C_{MVDC} = 200 nF
FRT parameters	U_{th} = 17 kV	I_{th} = 415 A	N_{sw} = 5
PSFB LVDC bus control	Kp_1= 3.4e^{-4}	Ki_1 = 1.3e^{4}	
PSFB current control	Kp_2 = 7e^{-4}	Ki_2 = 1e^{4}	ΔIp = 200 A/s
Boost LVDC bus control	Kp_3 = 5.3e^{-3}	Ki_3 = 710	

Two scenarios are studied, representing situations with high irradiance level and low irradiance level. In the low irradiance level scenario, the boost is not able to regulate the LVDC bus voltage to a constant value if the PSFB is regulating its nominal current. The maximum current search of the PSFB control is activated in this scenario.

The blue curves in Fig. 5.14 show the simulation results of the high irradiance level scenario. One can see that the LVDC bus voltage is regulated to 1 p.u. during the whole process with a deviation of 6% after the initial MVDC voltage dip. The initial output current increase after the voltage dip stays in the operating zone of diodes of typical rating for such a nominal current [74].

The red curves show the simulation results in a low irradiance scenario, with power at the PV side limited to 10% of the nominal power. This results in the PSFB supplying less current than in the previous case, so that the boost converter can maintain the LVDC bus voltage constant. A dip in the LVDC bus voltage can be observed at the moment the PSFB starts to transfer a current larger than the PV power limit, thus discharging the LVDC bus capacitor. The PSFB current is brought back down by the maximum current tracking control and the LVDC bus voltage is regulated to its nominal value. The slight bumps in the LVDC bus voltage and PV power are due to the way the maximum current tracking is done. As in the “perturb and observe” MPPT, there are constant perturbations in the control variable (here the reference current), causing little instabilities. Other algorithms could be explored to avoid this.

In both cases the output current is maintained to a level close to nominal right after the fault, enabling its identification, while the LVDC bus is kept at a constant voltage.

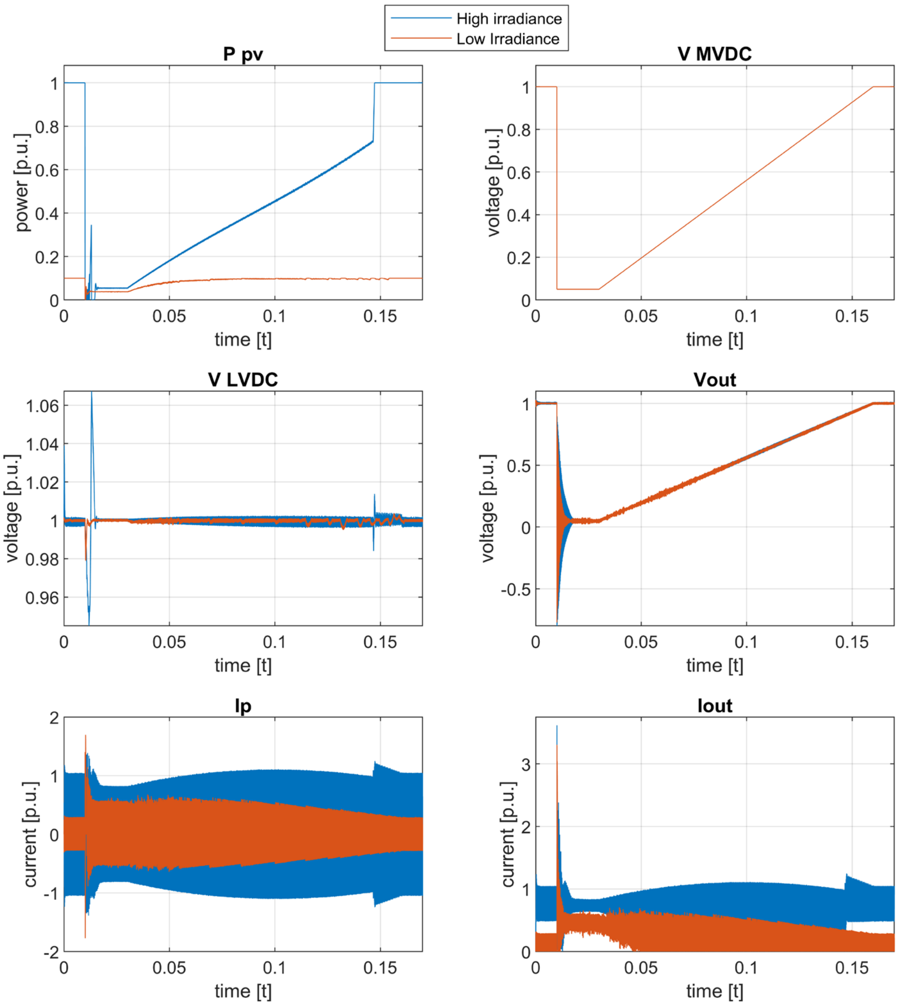


Fig. 5.14. FRT process in high irradiance scenario (blue) and low irradiance (red)

5.4. Chapter conclusion

In this chapter, the ability to control the PSFB for the needs of the PV application has been shown in both nominal and fault conditions.

As the PSFB has been mostly used for supplying loads, a model for input voltage regulation was missing from the literature. Hence, this thesis proposes an average model and tuning procedure for the nominal operation input voltage regulation of the PSFB. This scheme has been demonstrated experimentally. With the proposed controller, the influence of the value of the leakage inductance on the magnitude of the $C_{in}L_o$ resonance dictates the achivable bandwidth of the control. More advanced controllers can be proposed to achieve better dynamic performances even in the presence of an important $C_{in}L_o$ resonance. An other perspective is the developpement of a controller able to keep a similar dynamic when operating in CCM and DCM. Indeed, the controller presented here is tuned for CCM operation and DCM perfomances are incured (slower dynamics).

The PSFB being intrinsically safe in short circuit due to its output inductor, an additional control scheme could be proposed here to execute fault ride through. It has been shown in simulation that the converter is able to continue to output a current close to its nominal value, under different irradiance scenarios. This control involves the MPPT converter that takes up the role of LVDC bus voltage regulation during the fault event. In the presented scheme, communication is necessary between the PSFB and MPPT. A scheme relying only on individual converters measurements would robustify this delicate function from communication mishaps and delays.

The hardware implementation of the converter now needs to be studied in details. The constraints are mainly linked to the efficiency target and the medium voltage challenges such as series connection of components and dielectric design.

6. Design and implementation of a PSFB rectifier for MVDC

The previous chapter has shown the PSFB to be an attractive topology for the PV MVDC application and that it can be controlled in both nominal and fault conditions. However, in order for the DC-DC converter to be accepted in the PV application, not only does it have to fulfil efficiency requirements but it must also have a similar size as an equivalent 50 Hz transformer, despite its higher complexity (component count, control, etc.). The PSFB has four elements experiencing medium voltage: the MFT, the rectifier, the filter inductor and the filter capacitor. The large insulation distances required in air between all the components of the MV circuit may result in a bulky converter.

This thesis proposes to use a dielectric fluid, particularly the synthetic ester MIDEL 7131 [75] (referred to as “oil”), as an insulating material and cooling solution, not only for the MFT, but also for the complete MV circuit of the DC-DC converter, so that insulation distances can be minimised. An illustration of the complete DC-DC converter mechanical design is shown in Fig. 6.1 with its schematic in Fig. 6.2. The oil tank is supposed to integrate the MFT, rectifier and output filter composed of inductors and capacitors.

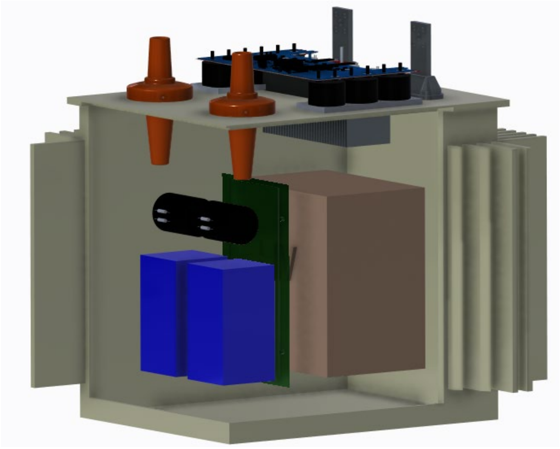


Fig. 6.1. Illustration of a DC-DC converter mechanical arrangement with MFT (brown), rectifier (green), inductors (blue) and capacitors (black) immersed in the oil tank and low voltage inverter sitting on top of the tank

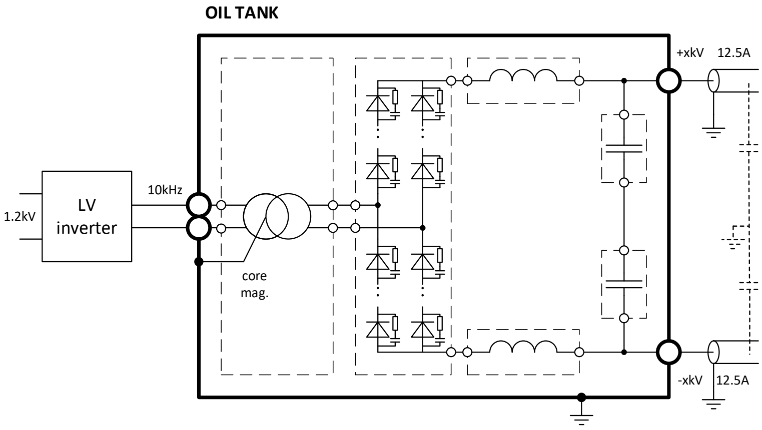


Fig. 6.2. Schematic of the converter, with entire MV circuit inside of the tank and LV inverter outside of the tank.

The integration of magnetic components in oil is usual for 50 Hz transformers and inductors and has also been done for MFT as it has been presented in the state of the art section 3.2.3. Oil immersed rectifiers reported in the litterature [54], [76], [77] are based on high power press-pack line frequency diodes. However, because of the low converter output current (250 kW/20 kV/12.5 A), the rectifier would be implemented using discrete diodes. Hence the rectifier is considered as the missing piece for the implementation of an oil-immersed PSFB medium voltage circuit.

This chapter discusses the challenges of the design of a medium voltage PCB-implemented diode rectifier as part of an oil-immersed DC-DC converter. The electrical design, cooling, dielectric design, and chemical compatibility topics are adressed. This work has been published by the author in [67], [78].

In a first section, the electrical design of a rectifier based on series connection of diodes is detailed, including the design of snubbers specific to the PSFB requirements. The ratings of this rectifier are motivated by the available material to test it and the reusability of the design for further work. The test bench presented in Appendix 3 is used. It is decided to keep the same current level as in the case study (12.5 A) and the voltage rating is selected as 4 kV. The same electrical design is then kept for the investigations on the other topics in further sections.

Two rectifiers of this design are in terms used in Chapter 7 for the implementation of a complete converter of ratings 1.2 kV to 6.6 kV (+15%, -10% as defined in section 2.3), 83 kW (always keeping the same output current rating).

6.1. Electrical design of a medium voltage rectifier for the PSFB

Diode assemblies are commercially available for medium voltage applications [79]. However, these assemblies usually use silicon bipolar diodes. Thus, reverse recovery happens at diode turn-off [80], yielding high power losses. In Section 2.2, it is shown that step-up DC-DC converters for MVDC collection network in PV applications are expected to reach efficiencies similar to those of state-of-the-art PV inverters cascaded with transformers (so that the global efficiency is comparabe to that of MVAC collection). Thus, very high efficiency is needed for all components of the converter. SiC Schottky diodes exhibit little to no reverse recovery current [80] and they are thus adapted for medium frequency, high efficiency applications. As a consequence, the use of series connection of SiC Schottky diodes in the output rectifier of the PSFB converter is investigated here.

The *LC* output filter of the PSFB was shown in section 4.3 to be advantageous compared with a simple output capacitor when the converter experiences faults on the MV side. However, the presence of an inductor between the rectifier and the output capacitor means that the rectifier bridge voltage is not clamped to the output voltage. Voltage oscillations occur at the diode turn-off, due to resonances between the transformer leakage inductance and parasitic capacitances of transformer and diodes, as described in [65], [81]. It is desirable to keep this voltage ringing low, so as to limit the peak voltage experienced by the diodes, and so as to limit electro-magnetic interferences (EMI). The *RC* snubber design for the series connection of SiC diodes must take into account the dynamic voltage balancing (due to potential diode parameters dispersion) as well as the voltage ringing in the PSFB converter.

The rectifier presented in this section is designed for a voltage of 4 kVdc, and maximum diode currents I_{mean} = 6 A, I_{rms} = 9 A, I_{peak}= 20 A. These values are the results of the PSFB design used in the comparison of topologies in section 4.1.2.

6.1.1. Selection of SiC diode

Commercially available diodes with suitable current ratings are mostly found in discrete packages, with voltage ratings up to 1.7 kV (3.3 kV diodes are less common and offer fewer choices in current ratings). In order to limit the number of series connected diodes, diodes with voltage ratings lower than 1200V are not considered. Therefore, we will only focus on 1200 V and 1700 V diodes here. Two diode models are selected for comparison: one 1200 V, 23 A (at 100°C case temperature) diode (GD10MPS12H, Genesic) and one 1700V 26 A (at 100°C cas temperature) diode (GD10MPS17H, Genesic).

The choice of the number of series connected diodes is motivated by the presence of overvoltages at the switching instant and failure mode considerations. Fig. 6.3 shows a simplified rectifier voltage waveform with an overvoltage at the switching instant, considered to be limited by the snubber design to 1.25 times the steady state voltage.

In addition to the effect of transient overvoltages, reliability requirements demand that the rectifier can operate with one faulty diode. Indeed, it is shown in [82] that for series connected diodes, an event of cosmic radiation interaction does not lead to single event burnout, as the blocking voltage is transferred to the other diodes of the series connection. However, this is only possible if the remaining diodes have enough blocking capability. If this is the case, the impacted diode does not fail and its blocking capability is recovered after a period of time dependent on the applied voltage [82]. The number of diodes n_{diodes} is chosen so as n_{diodes}-1 diodes rated blocking voltage is sufficient to withstand the switching instant overvoltage.

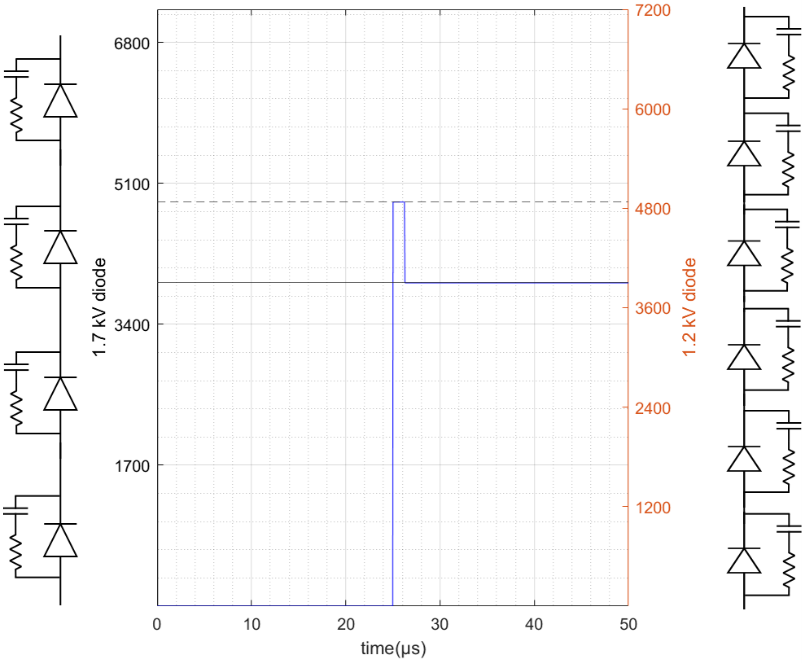


Fig. 6.3. Simplified rectifier waveform (blue) with overvoltage at switching instant, considered to be limited by the snubber design to 1.25 times the steady state voltage. Implementations with 6x1.2 kV or 4x1.7 kV series-connected diodes are represented. Each axis tick represents the breakdown voltage of a diode (1.7 kV on the left, 1.2 kV on the right)

Number of series connected diodes and resulting conduction losses (at nominal current) for both voltage ratings are presented in Table 6.1. The junction temperature is considered to be

125°C, as a worst-case scenario. Losses weighted with European efficiency coefficients (see equation (2.3)) are also presented. It must be noted that these values have no real physical meaning but they are relevant for comparisons.

Table 6.1. Comparison of rectifier bridge performance for 2 selected SiC Schottky diodes

Diode reference	Voltage rating	Number of diodes	Individual diode conduction losses at nominal current	Full bridge rectifier conduction losses at nominal current	Full bridge rectifier losses with EU efficiency coefficients
Genesic GB10MPS17H	1700 V	4	10.6 W	170 W	68.2 W
Genesic GD10MPS12H	1200 V	6	9.4 W	225 W	91.7 W

One can note that the 1.2 kV diode has lower individual losses compared to the 1.7 kV model. However, it is seen that 1.7 kV diodes choice leads to lower rectifier losses thanks to lower number of diodes, and this rating is thus selected. The losses weighted with EU efficiency coefficients confirm this choice, with proportionally an even slightly larger losses reduction compared to the 1.2 kV option. The 1.7 kV diode is thus considered for further design.

Thermal management of diode losses is met by individual heatsinks [83] at floating electrical potential, in natural convection condition. Each heatsink is referenced to the cathode of the diode, thus its potential varies according to ground in rectifier operation. Another solution would be to use a single, grounded heatsink to cool all the diodes of the rectifier. While it would simplify the mechanical structure, this would present a challenge in the electrical insulation of each diode, and yield relatively large parasitic capacitances between the cathode of each diode and the ground potential (typically tens to hundreds of picofarads). These parasitic capacitances are detrimental to the voltage balance in a series string [84], as they offer "escape paths" for the string current during diode switching. The proposed structure, with individual heatsinks, results in lower parasitic capacitances and therefore facilitates voltage balancing. It must be noted that the rectifier prototype presented in Fig. 6.4 is designed only to validate electrical properties and the thermal aspects are presented in a further section of this chapter dealing with oil-cooled rectifier.

Fig. 6.4. Full-bridge rectifier composed of 4 diode assemblies (series connection of 4 diodes and individual RC snubbers).

6.1.2. Snubber design

Snubbers are placed in parallel to each diode of the series connection, in order to ensure dynamic voltage distribution during commutations and to limit the overvoltages to values not exceeding diode breakdown voltage. The snubber is composed of a capacitor $C_{d1diode}$ and a resistor $R_{d1diode}$ in series. It is proposed to select the snubber values based on following equations, adapted from [85]:

$$C_{d_{1diode}} = k_{sc} \cdot C_{j_{1diode}} \qquad R_{d_{1diode}} = k_{sr} \cdot \sqrt{\frac{m^2 \cdot L_{lk}}{C_{d_{1diode}}}} \tag{6.1}$$

with $C_{j1diode}$ the junction capacitance of a single diode of the series connection, m the transformer ratio and L_{lk} the transformer leakage inductance (see Table 6.2). $C_{j1diode}$ is a non-linear capacitor, whose capacitance value depends on the reverse voltage across the diode. To simplify calculations, a constant value, taken at 50 % of the operating voltage, is used instead (80pF for the selected diode). Parameters k_{sc} and k_{sr} are design parameters that can be adjusted in order to reduce oscillating transient overvoltages at switching instants. It is proposed to initially set $k_{sc} = 3$ and $k_{sr} = 1$ following typical design rules of generic *RC* snubbers for dynamic balancing [85] and tune them for overvoltages concerns using the model presented below.

In order to analyse the voltage oscillations occurring at diode turn-off, the rectifier and transformer are modeled taking into account their parasitic elements. The model is derived according to [81], adapted to a full bridge rectifier and including the primary-secondary parasitic capacitance of the medium frequency transformer (MFT) modeled with lumped elements. The values of the parasitic elements of the MFT used in the test set-up can be found in Table 6.2. The circuit model is presented in Fig. 6.5. The voltage source is driven by rate-limited step functions representing the limited switching speed of the input bridge.

Table 6.2. MFT parameters of the rectifier tests set-up

Transformer ratio	**Leakage inductance**	**Primary winding capacitance**	**Secondary winding capacitance**	**Primary-secondary winding capacitance**
$m = 2.33$	$L_{lk} = 34$ µH	$C_p = 16$ pF	$C_s = 100$ pF	$C_{ps} = 30$ pF

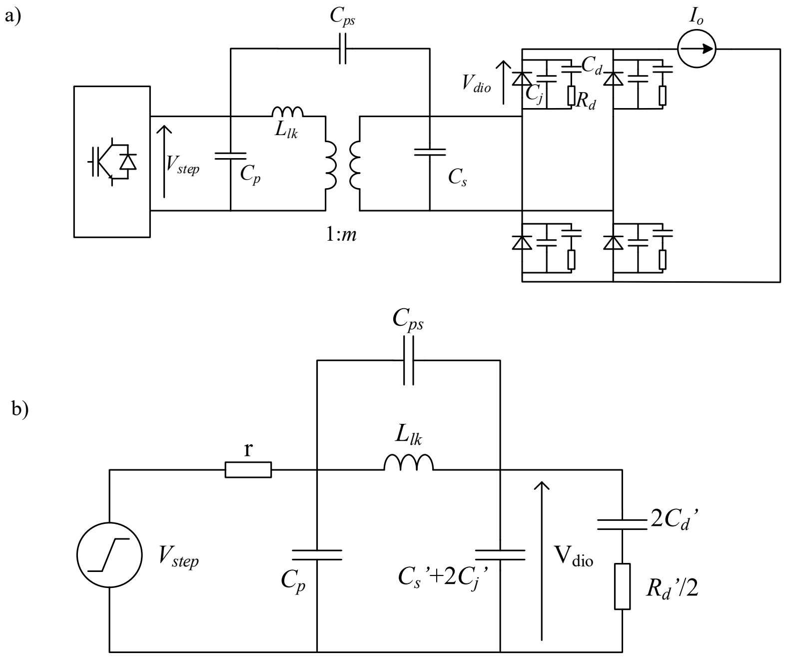


Fig. 6.5. a) Model of the PSFB converter including parasitic elements, b) Simplified PSFB model at diode turn-off used to study the voltage ringing phenomenon.

The diode symbols in Fig. 6.5 represent the series connection of n_{diodes}. Thus, the total junction capacitance C_j, snubber capacitor C_d, and snubber resistor R_d are defined as:

$$C_j = \frac{C_{j_{1diode}}}{n_{diodes}} \quad C_d = \frac{C_{d1diode}}{n_{diodes}} \quad R_d = R_{d1diode} \cdot n_{diodes} \tag{6.2}$$

The simplified model in Fig. 6.5b is represented as viewed from the primary side of the MFT; secondary side components are reflected to the primary following equations (6.3). Before the switching instant, the parasitic components of the pair of diodes in blocking state are in parallel to each other in the equivalent circuit of the converter. This results in the values of the aggregated components of the simplified model given in Fig. 6.5b.

$$C_s' = C_s \cdot m^2 \quad C_j' = C_j \cdot m^2 \quad C_d' = C_d \cdot m^2 \quad R_d' = \frac{R_d}{m^2} \tag{6.3}$$

The quantity of interest is the voltage across a diode string seen from the primary, V_{dio}. The actual diode string voltage (at the secondary) $m\ V_{dio}$ is shown in Fig. 6.6a for the tests set-up parameters. The effect of the switching speed is shown by driving the circuit with different rate-limited step functions. The inverter used for tests being IGBT-based, low switching speeds are represented but higher speeds are also shown to cover the use of SiC MOSFETs in the full converter prototype of Chapter 7.

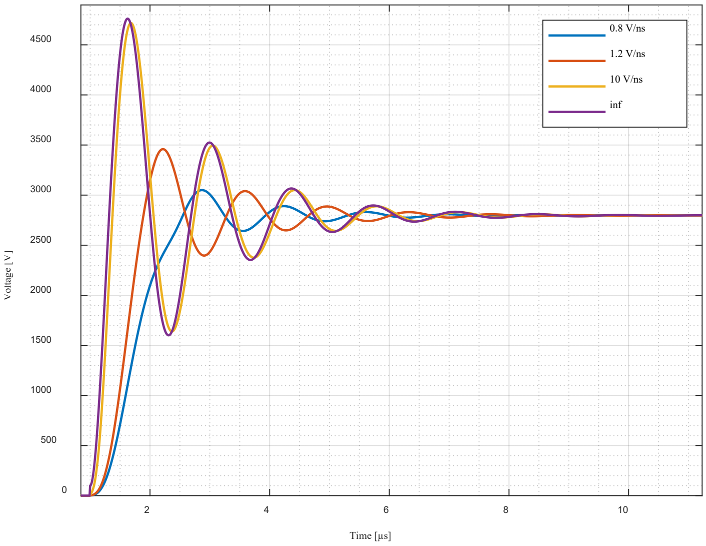


Fig. 6.6. Resulting $m\ V_{dio}$ (voltage across a diode string) using the model in Fig. 6.5b, with a) different switching speeds of Vstep (base case 1.2 V/ns, corresponding to the inverter used here for experimental validation)

It is observed that oscillations are more severe for high switching speed, with important overvoltages. Designing the snubber to attenuate the overvoltages associated with a perfect step input would lead to oversizing compared with a more realistic case (when using IGBTs as in our test set-up). However, for a switching speed of a SiC MOSFET power module (here 10 V/ns), considering a perfect step gives a good extimate of the overvoltage. The final values selected for this prototype are $C_{d1diode}$= 270 pF and $R_{d1diode}$ = 830 Ω.

Some high value resistors can be added in parallel of each diode for static voltage balancing so as to balance possible deviations in the leakage currents of the various diodes. However, considering the low value of leakage current of the selected diode (9 µA at 175 °C of junction temperature), the associated voltage deviations would be very low and these resistors are not implemented in this design.

6.1.3. Simulations

In order to validate the design performed using the model from Fig. 6.5b, a detailed circuit model was implemented using the Simulink Simscape Electrical library. Each diode is modeled with its own junction capacitance (with voltage dependency taken into account via a lookup table) and *RC* snubber. The input inverter bridge is also modeled. Rectifier voltage oscillations obtained with the detailed model (Fig. 6.7) are similar to those presented in Fig. 6.6a (simplified model) for similar rates of change in voltage (3500 V peak voltage of the diode string with a 1.2 V/ns step). This detailed simulation with each individual diode also enables to verify the voltage distribution across the series-connected diodes. Results are shown in Fig. 6.7.

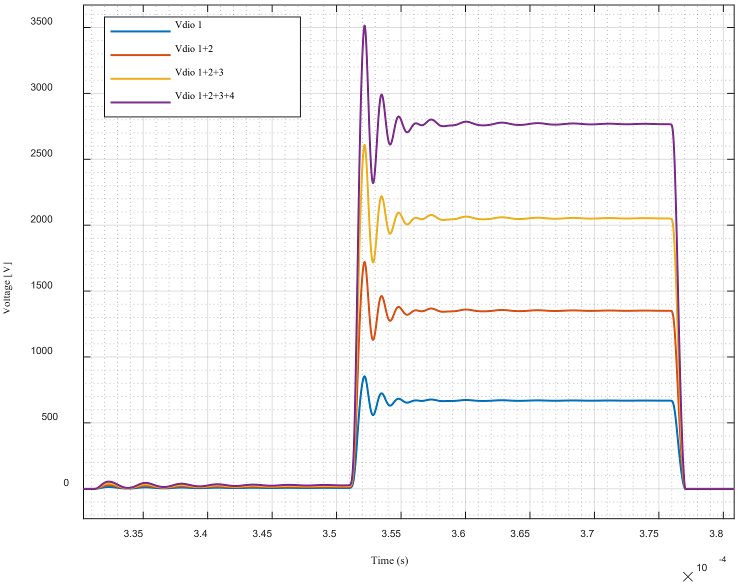


Fig. 6.7. Detailed simulation of a diode series connection, voltage distribution between the 4 diodes of the series connection. Voltages are stacked from the anode-side diode to the cathode-side diode.

The effect of value deviation (caused by manufacturing tolerances) of the snubber components on the voltage balancing can be seen in Fig. 6.8. Each snubber component of a string of 4 diodes is shifted from its nominal value in the range of ±5%. Snubber capacitor value deviation has a larger influence on balancing than that of snubber resistance (that has a very small effect on peak voltage, below 10 V).

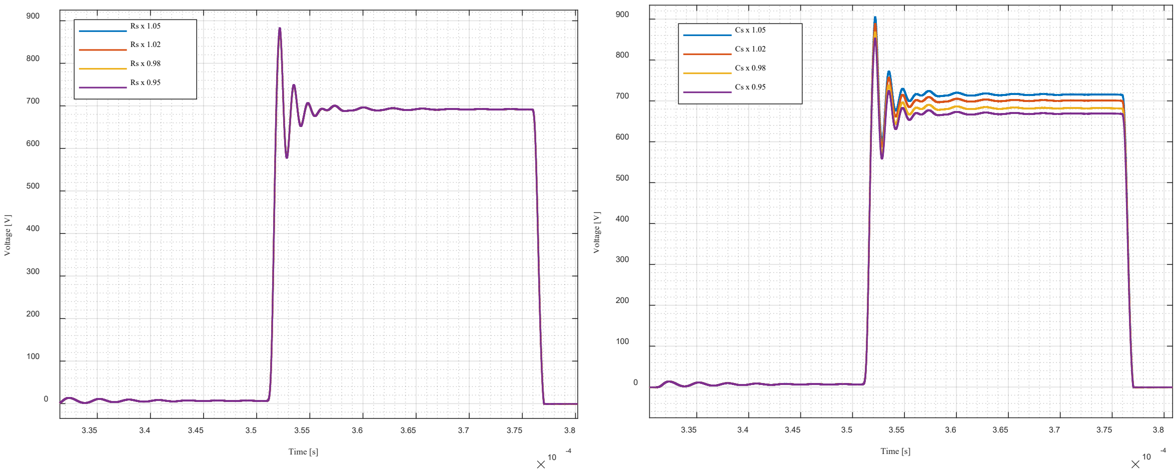


Fig. 6.8. Detailed simulation of a diode series connection, left) snubber resistor value deviation effect on voltage distribution, right) snubber capacitor value deviation effect on voltage distribution.

One should note that although complete simulations of the switching circuit enables to design the snubber precisely, the addition of so many parasitic components slows down the simulation that is already using a very small time step (typically inferior to 0.1 µs). The simplified model from Fig. 6.5b is thus more convenient for iterating on snubber components selection during the design phase.

6.1.4. Experimental verification

The designed rectifier is tested within the DC-DC converter test setup shown in Appendix 3 to validate the voltage balancing between the diodes and the overvoltages. The inverter is operated at 20 kHz, with a full wave modulation.

The rectifier is tested in a non-clamped voltage configuration (inductive output) with an input voltage of $V_{in} = 1200$ V. The voltage distribution between the 4 diodes of an assembly is shown in Fig. 6.9. It must be noted that because of the available transformer ratio, the rectifier is not tested at its full designed voltage rating of 4 kV. The maximum measured voltage imbalance is around 10%.

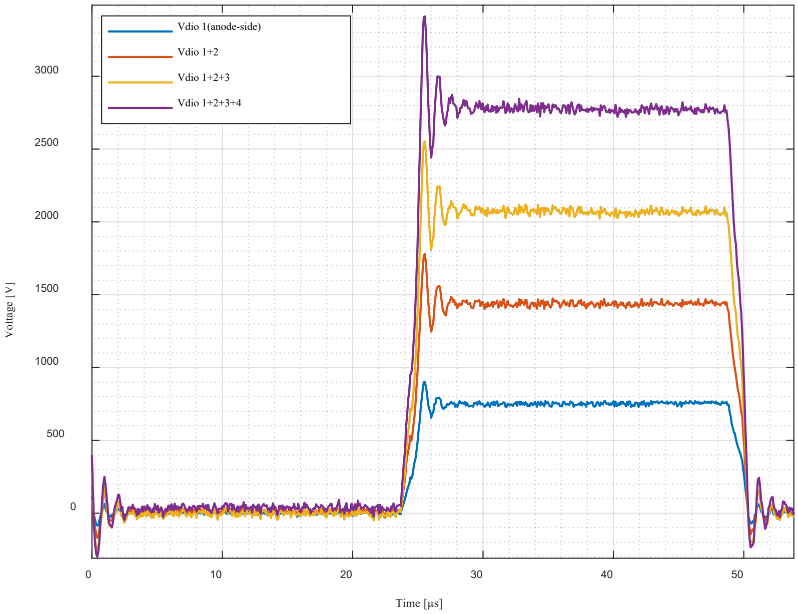


Fig. 6.9. Voltage distribution between the 4 diodes of the series connection. Voltages are stacked from the anode-side diode to the cathode-side diode.

The simplified model presented in the previous section (Fig. 6.5b) is ran with the same switching speed of the input bridge as observed in the measured waveforms (1.2 V/ns, the inverter is IGBT-based), the snubber components values from the design section, and the parasitic elements from Table 6.2. The measured voltage across one diode string is shown in Fig. 6.10, superimposed with the model result.

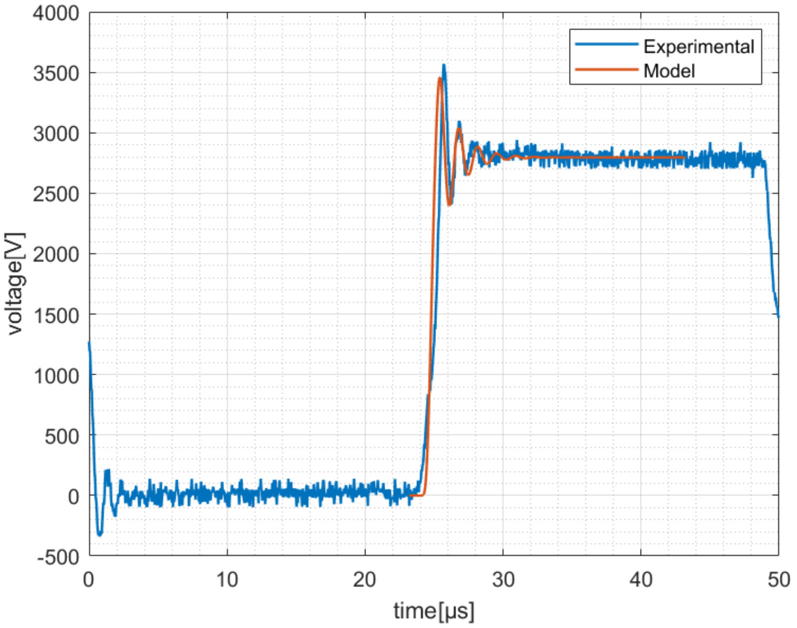


Fig. 6.10. Comparison between simulation results using the simplified model and experimental measurements of a diode assembly at turn-off.

The model result is close to the measured waveform. We can observe only small differences in terms of peak voltage, frequency of the oscillation and speed of the voltage step. These are considered to be due to inaccuracies in the transformer parasitic capacitances, as such small values (a few pF or tens of pF) are complicated to characterize with precision. However, the results still show the relevance of the simplified model for designing the snubber components in order to limit the overvoltage.

A rectifier for medium voltage medium frequency DC-DC converter has been designed and tested. The design choice in terms of number of series connected diodes is motivated by efficiency and reliability. The particular operation of the rectifier with an *LC* output filter ("unclamped operation") is studied and a simplified model is improved based on the literature. The model allows fast simulations of turn-off voltage oscillations, enabling snubber design, taking into account the DC-DC converter parasitic elements. Measurements confirm the proposed design and model. However, this air-insulated version version is large (because of insulation distances and heatsinks), and the next step is to propose a more compact design, which can be integrated together with the MFT and output filter.

6.2. Thermal characterisation

Following the integration of the different elements in the tank presented in Fig. 6.1, the rectifier should have a flat form factor and act as an interface where the MFT and inductors connect. In order to have this flat form factor affecting the tank volume at the minimum, diodes are mounted on a a single printed circuit board (PCB). The focus of this part is thus put on the cooling of the PCB-based rectifier circuit in oil. The use of oil-immersion cooling for PCB components has mostly been studied in the context of data centers servers [86], for low power IC components. The cooling of a medium frequency, medium voltage rectifier in oil has not been discussed in the literature.

6.2.1. Design of oil-immersed diode heatsink

As presented in section 6.1, the diodes selected for such a low current rectifier are packaged in standard TO-247 packages. The exchange surface with surrounding oil of this small package is limited and it is thus common to attach it to a finned heatsink, altering the favorable thin and flat form factor of the PCB. Indeed, in our case, using heatsinks attached to the diode packages is not desirable as it increases the box volume of the rectifier and therefore the total volume of the tank. Also, although oil has a better heat carrying capability than air, a DC-DC such as presented in Fig. 6.1 would rely on natural convection (whereas air cooling can be improved using forced convection), resulting in limited heat exchange coefficients. Therefore, effective use of oil to cool the diodes requires increasing the heat exchange surface around the diodes by creating patterned copper patches and thermal vias on both sides of the board. These "flat heatsinks" can be seen in Fig. 6.11.

A 4 kV full bridge rectifier is realised following the electrical design principles presented in section 6.1 with four 1.7 kV diodes connected in series per rectifier diode function. The concept presented above is used for the thermal design.

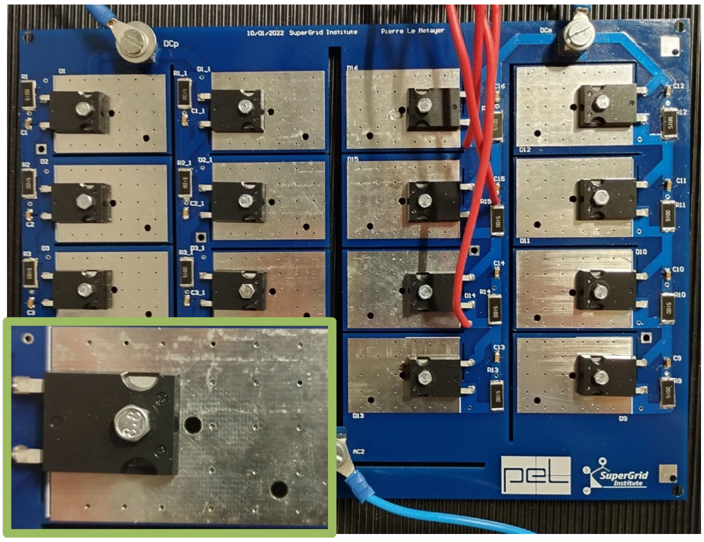


Fig. 6.11. 4 kV PCB-implemented diode rectifier, with zoom on patterned copper patch used as heatsinks on both sides (bigger holes are for thermocouple mounting).

In order to choose the size of the copper patch around each diode, a simplified thermal model is used. It is considered that all of the copper surfaces on each side of the board represent a complete plate of surface S and height H. The model of the Vertical Parallel Plates [87] is used, with the second plate representing the MFT as shown in Fig. 6.1, and with the space between the two plates defined as L. This enables to compute the thermal resistance $R_{th\_conv\_oil}$ of the rectifier to oil interface with equations (6.4) to (6.9) and the MIDEL 7131 properties given in Table 6.3.

$$\mathrm{Gr} = \frac{\mathrm{g}\,\beta\,\Delta T\,L^3}{\nu^2} \tag{6.4}$$

$$\mathrm{Pr} = \frac{c_p\,\nu\,\rho}{\lambda} \tag{6.5}$$

$$\mathrm{Ra} = \mathrm{Gr}\,\mathrm{Pr} \tag{6.6}$$

$$\widetilde{\mathrm{Ra}} = \mathrm{Ra}\,\frac{L}{H} \tag{6.7}$$

$$\mathrm{Nu} = \left(\frac{576}{\widetilde{\mathrm{Ra}}^2} + \frac{2.873}{\widetilde{\mathrm{Ra}}^{0.5}}\right)^{-0.5} \tag{6.8}$$

$$\mathrm{R}_{th\_conv\_oil} = \frac{L}{\mathrm{Nu}\,\lambda\,\mathrm{S}} \tag{6.9}$$

Table 6.3. Thermal model parameters

PCB parameters	
Height of the PCB *H*	19 cm
Exchange surface *S*	432 cm²
Gap between 2 “plates” *L*	> 5 mm
Midel 7131 properties at 60°C	
Thermal expansion coefficient β	$77e^{-5}$ /°C
Kinematic viscosity ν	$13.7e^{-6}$ m²/s
Specific heat capacity c_p	1995 J/kg °C
Density ρ	939 kg/m³
Thermal conductivity λ	0.144 W/m °C
Diode parameters	
Diode model	Genesic GD25MPS17H
Junction to case thermal resistance R_{th_jc}	0.3567 °C/W
Case to patch thermal resistance R_{th_cp}	0.2151 °C/W

With the values used in this study given in Table 6.3, it is found that the space between the two plates has little to no influence on the thermal resistance.

The surface of a copper patch is designed so the junction temperature of the diode does not exceed 100°C, considering losses corresponding to the operation at nominal current, with the oil temperature being 60°C. One should note that this is really conservative, as SiC diodes can operate with junction temperatures above 150°C. The junction-to-case thermal resistance of the diode R_{th_jc} and the case-to-patch thermal resistance R_{th_cp} are known (Table 6.3) and patch dimensions are adjusted in order to obtain the required $R_{th\_conv\_oil}$. This results in the design shown in Fig. 6.11, with identical copper patches on both sides of the PCB. The complete PCB size is 19 cm by 27 cm. The individual surface of a copper patch is S_{patch_face} = 13.5 cm², resulting in the total exchange surface S = 432 cm².

6.2.2. Experimental verification

The rectifier shown in Fig. 6.11 is tested at nominal power losses to validate the performance of the presented thermal design. The test set-up including the oil reservoir, pre-heating system, and rectifier board can be seen in Fig. 6.12.

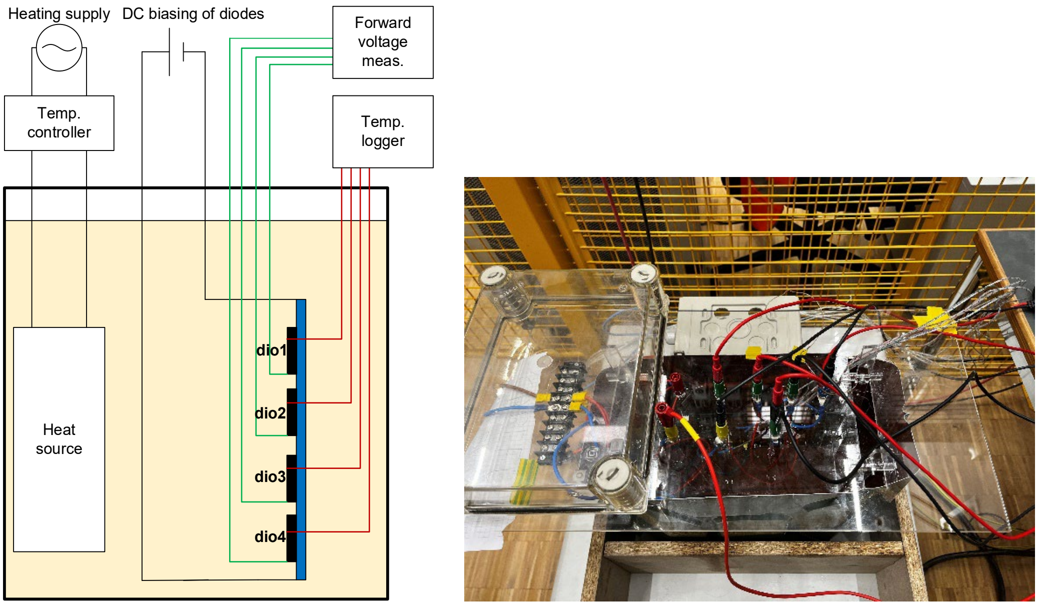


Fig. 6.12. Test set-up of the 4 kV prototype of oil-immersed diode rectifier PCB (represented in blue in the schematic)

The case temperatures of 4 vertically stacked diodes are measured with thermocouples. The MIDEL 7131 oil in which the rectifier is immersed is first heated up to 60°C by resistors in front of the PCB, to represent the DC-DC oil tank environment. The nominal diode current is reached by applying the correct biasing voltage with a DC source. Results can be seen in Fig. 6.13.

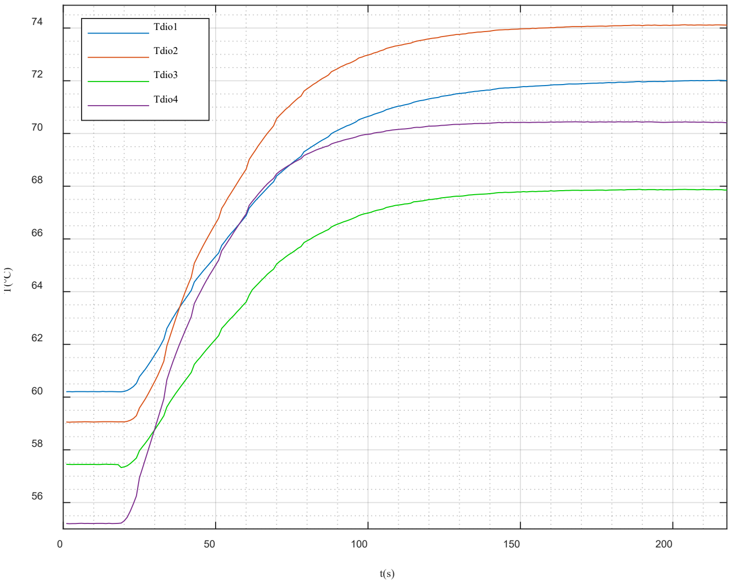


Fig. 6.13. Temperature of diodes for a power loss step from zero to nominal diode power loss.

One can first observe that the initial temperature is not 60°C for all diodes. Indeed the pre-heating was done with its reference measuring the oil temperature near the top of the reservoir. Thus the initial temperatures of some diodes is lower than 60°C, with the diodes in the bottom of the reservoir having lower temperatures. The maximum final case temperature is 74°C. Based on the value of R_{th_jc} and the previously estimated case-to-patch thermal resistance R_{th_cp} results in the junction temperature of 90.6°C. This is well below the limit originally fixed. This gives the conclusion that the model used is sufficient to design a thermally safe rectifier but a better model should be developed if the size of the copper patches needs to be optimised. Less conservative design margins on the junction temperature of the diode could also be taken to reduce the copper patch size.

It can be observed in Fig. 6.13 that temperature increases are different from diode to diode as the final temperatures are not correlated similarly as in the initial state. This can be mainly explained by differences in forward voltages and thus power losses as can be seen in Table 6.4. There is a clear correlation between forward voltage (dissipated power) and temperature rise.

Table 6.4. Forward voltages and temperature increases of series connected diodes at nominal losses

Diode	Forward voltage	ΔT
Dio1	1.11 V	12.7°C
Dio2	1.18 V	15.2°C
Dio3	1.09 V	10.4°C
Dio4	1.16 V	15.1°C

6.3. Dielectric characterisation

When designing the PCB rectifier for higher rated voltages, the objective of keeping a small volume will lead to layouts where some traces with high voltage differences run close to each other. To keep a safe but compact design, the necessary insulation distances must be precisely known. Dielectric breakdown of liquid-insulated PCB was studied in [88] but is limited to 35 µm-thick copper traces, whereas thicker copper would be needed for current levels above a few amperes. The breakdown voltage of the gap between two 70 µm thick traces on sample PCBs immersed in MIDEL 7131 oil is thus experimentally tested. The influence of the oil quality is also studied. Indeed, the dielectric strength of the oil is usually given for oil especially treated to remove impurity particles and humidity. The oil quality can degrade during operation, especially in the case of a free-breathing tank.

6.3.1. Experimental set-up for PCB dielectric characterisation in oil

The same test set-up set-up is used for breakdown voltage and partial discharge measurements. The voltage is applied on the sample PCBs using an auto transformer connected to a 100 kV step up transformer. A 1.04 µF coupling capacitor is used for electrical PD measurements in compliance with the IEC 60270 standard. An Omicron MPD600 system is used to detect and record the PD activity. The partial discharge inception voltage (PDIV) is considered to be the voltage value after which a sustained PD activity is observed over the 10 pC threshold. The voltage is continuously raised at approximatively 1 kV/s until breakdown occurs. The last voltage value is taken as the breakdown voltage. Voltage levels are given as RMS values.

A PCB with two electrodes made of 70 µm thick copper traces and a 3 mm gap is used as test sample as shown in Fig. 6.14. One electrode is connected to the output of the high-voltage transformer and the other to the ground. Tests are performed in a box with plastic separators so the oil doesn't flow to the next sample after a breakdown (Fig. 6.15). Tests are performed with treated and non-treated oil. Each test configuration is performed with 10 samples.

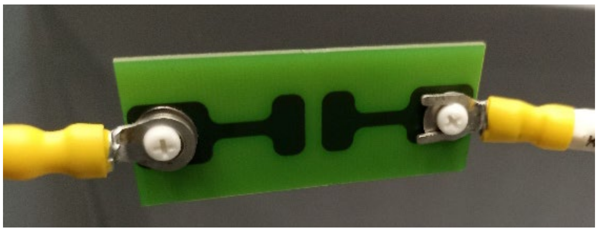


Fig. 6.14. Sample PCB with 3 mm gap and 70 µm thick traces

Fig. 6.15. Test set-up of the PCB samples, after a batch of tests (black spots where breakdown happened)

6.3.2. Breakdown voltage and PDIV results

The results are presented using Weibull plots. The sample results are fitted to a two-parameter cumulative Weibull distribution function:

$$F(V) = 1 - \exp\left[-\frac{\mathrm{V}}{\alpha}\right]^{\beta} \tag{6.10}$$

with V the breakdown voltage or PDIV, α the scale factor and β the shape parameter.

Results for breakdown voltage are shown in Fig. 6.16 and for PDIV in Fig. 6.17. It can be seen that most of the data points are aligned, indicating a good fit with the Weibull function. The Weibull parameters are summarised in Table 6.5.

Table 6.5. Weibull parameters for breakdown voltage and PDIV

Parameter	**Treated oil**	**Non-treated oil**
Breakdown		
α	37.5 kV	35.3 kV
β	4.9	5.5
Partial discharge		
α	35.3 kV	19.6 kV
β	6.6	6.8

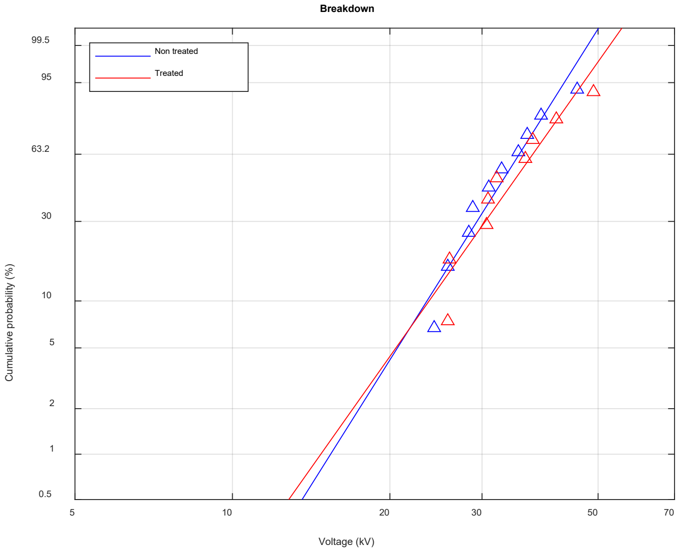


Fig. 6.16. Weibull plots for breakdown voltage in treated and non-treated oil. Markers: measurement data; plain line: Weibull fit.

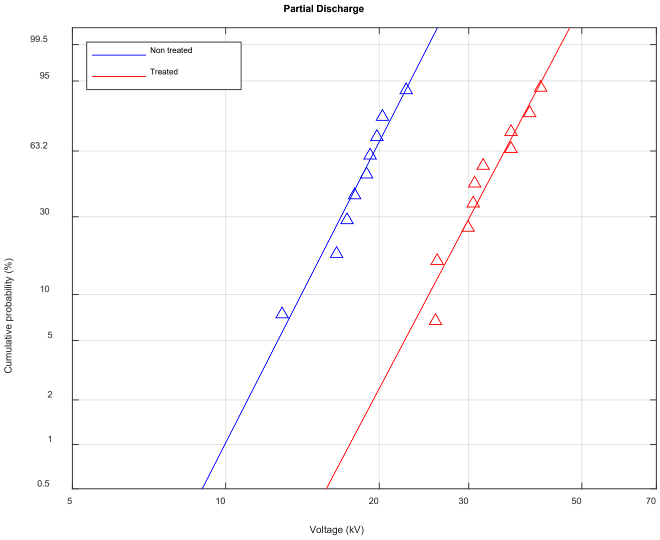


Fig. 6.17. Weibull plots for PDIV in treated and non-treated oil. Markers: measurement data; plain line: Weibull fit.

One can understand that appearance of PD at a relatively low voltage for non-treated oil comes from the fact that impurities are more likely to pass in the gap than with treated oil. The PDIV in treated oil, the breakdown voltage in non-treated oil and the breakdown voltage in treated oil are all very similar. This can be understood by looking at the different aspects of the gap after a breakdown (Fig. 6.18). Two distinct types of failures can be observed. The most commonly observed is the superficial breakdown (see Fig. 6.18, left), where arcing seems to have occurred in the oil at the surface of the PCB. In this case, the sample can be used again and shows similar breakdown voltages, as seen in Table 6.6. The second type of breakdown seems to happen inside of the varnish coating of the PCB and is only observed for the highest breakdown voltages (see Fig. 6.18, right). In both cases, it is observed that the varnish covering the edge of the copper trace has been damaged. The breakdown of the thin varnish coat on the copper would result in a breakdown in oil when impurities are present in the gap. In treated oil, it is less likely to have impurities, hence the slightly higher breakdown voltage. In certain cases, impurities would not pass in the gap during the test and the voltage could be increased until the point where the varnish would then break in the complete gap length as seen in Fig. 6.18. This kind of failure occurred for 3 out of 20 samples. It can be seen in Fig. 6.19 that in the case of breakdown of the varnish, the arc has carved the surface and the fiberglass present inside of the PCB is made apparent. This failure mode can no longer be attributed to the oil only, and consitutes a more intrinsic limitation of the immersed PCB sample.

Table 6.6. Repeated superficial breakdowns of one sample in non-treated oil, in chronological order

Breakdown number	1	2	3	4
Breakdown voltage (kV)	30.9	32.4	26.8	29.2

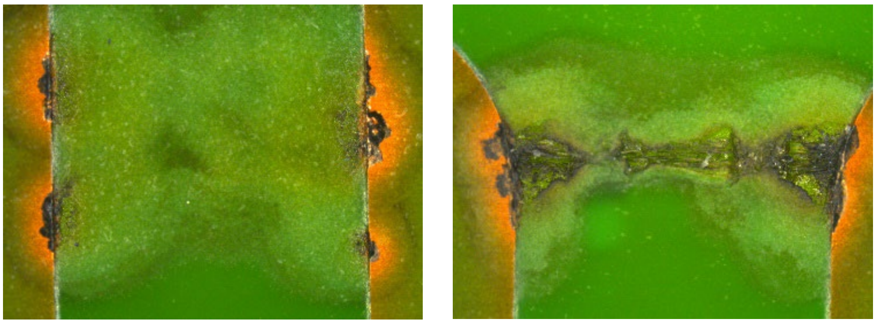


Fig. 6.18. Left) Superficial dielectric breakdown, Right) Varnish dielectric breakdown (3 mm gap)

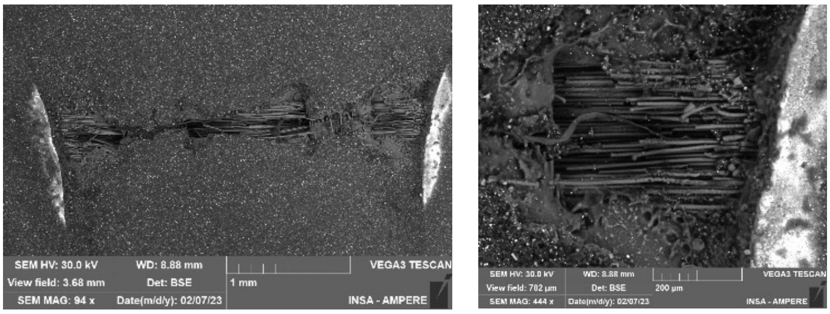


Fig. 6.19. Left) Electronic microscope capture of the trench created during the varnish breakdown event, Right) Zoom on the right electrode, with apparent fiberglass

One must note that, in a rectifier such as discussed in this section, most conductive traces are not exposed to pure AC voltage, and some even experience unipolar voltages. It is reported in [88] that breakdown voltages are different when the traces are exposed to bipolar or unipolar waveforms. Thus, similar tests with unipolar waveforms are still needed. Other investigations, with variations of gap length, varnish material and presence of traces on both sides of the PCB have been performed. The results are kept confidential by SuperGrid Institute.

For the rectifier used in the complete converter prototype presented in Chapter 7, a conservative design rule is defined from the available results. The 1% probability PDIV value, in non treated oil, from Fig. 6.17 is taken and divided by the gap length of the sample of 3 mm to define the design rule for distance between traces of 3.3 kV/mm. The value in non treated oil is selected because the prototype tank is supposed to be opened often. For a, non-prototype, sealed tank, the treated oil values can be used resulting in a design rule of 6 kV/mm.

6.4. Chemical characterisation

The immersion of power electronic components in oil is usually done in high power applications with press-pack components [89]. These use inorganic insulating materials (ceramic), which tend to have good chemical stability. The materials used for PCB and PCB-mounted components are different, with many of them (plastics, resins) potentially able to react with the oil. In this section, we present tests aimed at assessing the effect of oil immersion on these elements.

6.4.1. Experimental set-up for PCB and components

The studied components are listed in Table 6.7. A control sample is kept unaltered for each component. The test samples are initially dried at 80°C during 24 hours in order to remove any humidity that could be contained in the component. They are then weighted and photographed (Fig. 6.20). All of the components are immersed in the oil and stay in an oven at a given temperature for a week. After a week the components are removed from the oil, superficially wiped with blown nitrogen, weighed and photographed. Control samples are also weighed again. The scale error is given as ±5 mg. The procedure is then repeated, at a higher temperature. A mass decrease or increase of a component after immersion would indicate a disaggregation or an oil intake, respectively. Changes in appearance from the photographs (discoloration, swelling) would also indicate reaction with the oil.

Table 6.7. Tested components

Component	**Technology**	**Mass after drying**
PCB	FR4	9.473 g
Diode	TO-247	6.043 g
Resistor 1	Through-hole, cemented	4.978 g
Resistor 2	SMD, thin film	225 mg
Capacitor 1	Through-hole, polypropylene film	1.345 g
Capacitor 2	SMD, MLCC	33 mg

Fig. 6.20. Tested components before immersion, from top left to bottom right: PCB, diode, resistor 1, resistor 2, capacitor 1, capacitor 2.

6.4.2. Chemical characterisation results

The results are shown in Fig. 6.21. The measured masses are normalised to the mass of the component after drying in order to remove offset between the test and control samples.

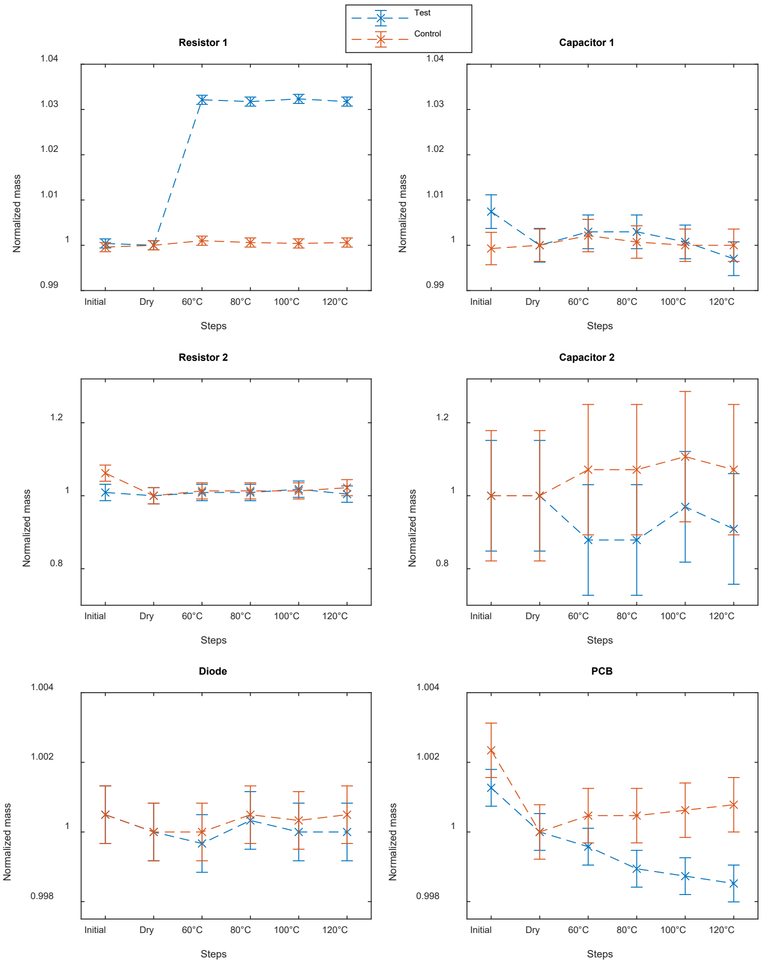


Fig. 6.21. Normalised mass of test and control samples with ±5 mg error bars.

The most noticeable change is seen in the through-hole cemented resistor 1. A mass increase is measured in the test sample after the first immersion. The oil intake of the resistor can be observed in Fig. 6.22 where we see bulges appearing after the first immersion. Comparing with the snapshot of resistor 1 before immersion in Fig. 6.20, it can also be seen that the color of the cement changed to a darker tone after immersion. The fact that no further mass increase is observed after other immersions would mean that porosity in the cement structure filled up entirely during the first immersion. One should note that this interaction is not essentially problematic, as the resistance value was not measured to be outside of its rated tolerance after the mass increase. This observation only shows that there is an interaction with the oil.

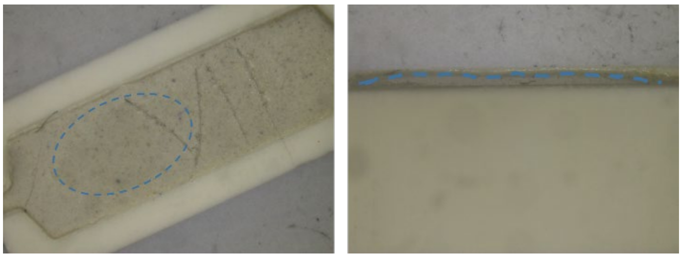


Fig. 6.22. Bulges appearing on the cement after the first immersion (VII is the component designator)

The other components don't show significant change in their mass during the experiment. In particular, the diode, the main component of the rectifier, has shown no interaction with the oil.

It can be seen that Capacitor 2 has the largest relative mass change. However, this is due to the fact that its initial mass of 33 mg is close to the scale error of ±5 mg. The other component showing a separation between the test and control samples is the PCB. The mass change of less than 0.3% is not considered significant.

Capacitor 1 shows a visible change in the aspect of its insulating material as can be seen in Fig. 6.23. However, this is believed to be caused not by oil interaction but by temperatures exceeding the capacitor rated temperature of 80°C. Indeed, the color of the insulating material starts to change at the 100°C step.

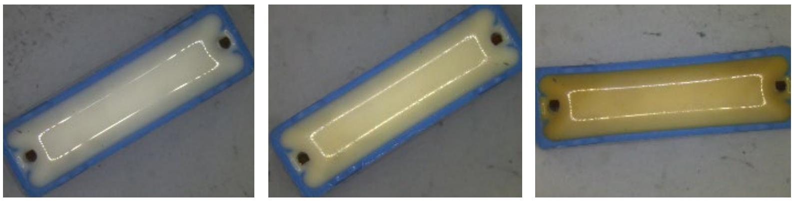


Fig. 6.23. Capacitor 1 insulating material after steps at temperature, from left to right, 80°C, 100°C and 120 °C.

The SMD components masses are not affected by the oil immersion and they show no alteration during the whole experiment. This kind of component is thus considered the preferred option for the implementation of the rectifier snubbers on the oil-immersed PCB, as they show no interaction with the oil.

6.5. Chapter conclusion

This chapter has presented the design of a medium voltage medium frequency rectifier, based on series-connected SiC Schottky diodes. The choices of diode rating and number of series connected diodes are discussed considering efficiency and reliability. The oscillations typical of the non-clamped voltage of the rectifier of the PSFB are modelled based on [81]. A contribution of this thesis is the adapatation of this model to series-connected assemblies of diodes, full-bridge rectifier and the inclusion of the effects of transformer primary-secondary capacitance and limited switching speeds. This simplified model enables rapid snubber design. Tests are performed on the designed rectifier and measured waveforms are compared with the results expected from the model. It is observed that the peak overvoltage is correctly estimated by the proposed model.

The concept of integrating all of the medium voltage components of an MVDC DC-DC converter in oil has been explored. In particular, a PCB-implemented diode rectifier has been studied regarding cooling, dielectric design and chemical compatibility.

This thesis has shown that patterned copper patches are usable as “flat heatsinks” for the cooling of discrete diodes in standard through-hole TO-247 package. This enables increasing the exchange surface with oil while keeping a thin and flat form factor. The comparison of the model results with the experiements shows that it gives pessimistic values, meaning that it should be improved if a more compact design is needed.

The influence of the quality of the oil on the PDIV and breakdown levels has been studied. A design rule for the distance between traces on the PCB rectifier is defined as 3.3 kV/mm for non treated oil (as in the prototype of Chapter 7) and 6 kV for treated oil. However, one should note that this design guideline should be verified with more representative voltage waveforms (unipolar, square wave).

Finally, it has been shown that SMD components are suitable for oil immersion as they show no degradations when exposed with prolonged immersion, even at high temperatures. Further studies can include the analysis of the oil of a complete DC-DC prototype after nominal operation.

With the design principles found in this chapter, a prototype can now be built in order to verify the efficiency performance needed for a DC-DC converter in a PV MVDC application.

7. 6.6 kV 83 kW DC-DC Prototype

This chapter presents the desing and implementation of the prototype used to verify the performance of the PSFB for PV MVDC. A dimensioning procedure is proposed to optimise the European efficiency. The implementation of the 1.2 kV to 6.6 kV 83 kW prototype is done based on the work presented in Chapter 6. Experimentals validations of ZVS and DCM limits are performed.

7.1. Dimensioning for European efficiency

The design of the PSFB aims at achieving the transmission of the nominal power in the voltage ranges shown in Table 2.4, while optimising the European efficiency. It is proposed to formalise the dimensioning in the optimisation problem standard form [90] shown below:

$$\begin{array}{lll} \text{minimise} & f(\boldsymbol{x}) & \text{(cost function)} \\ \text{subject to} & g_i(\boldsymbol{x}) \leq 0, i = 1, \dots, m & \text{(inequality constraints)} \\ & h_j(\boldsymbol{x}) = 0, j = 1, \dots, p & \text{(equality constraints)} \end{array} \tag{7.1}$$

with $\boldsymbol{x}$ the problem variables.

For the PSFB design, the problem variables are the component values, which are represented in the $\boldsymbol{x}$ vector below.

$$\boldsymbol{x} = [L_{lk}\ L_m\ m\ L_o] \tag{7.2}$$

The cost function is the weighted average of primary bridge MOSFET losses, using the European efficiency coefficients from equation (2.3).

$$f(\boldsymbol{x}) = 0.03\,\lambda_{5\%} + 0.06\,\lambda_{10\%} + 0.13\,\lambda_{20\%} + 0.1\,\lambda_{30\%} + 0.48\,\lambda_{50\%} + 0.2\,\lambda_{100\%} \tag{7.3}$$

with $\lambda_{k\%}$ the power losses of the inverter for the transmitted power $k\%$ of P_{max}.

The general form of the power losses in the 4-MOSFET inverter is::

$$\lambda_{k\%} = 2\,\lambda_{1,k\%} + 2\,\lambda_{2,k\%} \tag{7.4}$$

$$\lambda_{\alpha,k\%} = R_{ds,on}\left(i_{rms,\alpha,k\%}\right) i_{rms,\alpha,k\%}{}^2 + \left[E_{on}\left(i_{on,\alpha,k\%}\right) + E_{off}\left(i_{off,\alpha,k\%}\right)\right] f \tag{7.5}$$

with α the parameter for leading leg (coded as 1) or lagging leg (coded as 2), $R_{ds,on}$ the on-state resitance of the MOSFET and E_{on} and E_{off} the switching energies at turn-on and turn-off.

The turn-on losses cancel out when the ZVS conditions are met. This occurs when the inductive energy in the circuit at commutation time is sufficient to discharge/charge the parasitic capacitors of the switching cell. The leading leg is always in ZVS, as it benefits from the large output inductor energy. The lagging leg only relies on the energy stored in the leakage inductor of the MFT and is in ZVS when fulling the condition on switching current presented in section 4.1 and shown in equation (7.6).

$$i_{off,2,k\%} \geq \sqrt{\frac{2}{L_{lk}}\left(\frac{4}{3}\,C_{mos}\,{V_{in}}^2 + \frac{1}{2}\,C_{wind}\,{V_i}^2\right)} \tag{7.6}$$

with C_{mos} the MOSFET output capacitance and C_{wind} the primary winding capacitance of the transformer.

The analytical formulas for the RMS and switching currents of leading and lagging legs depending on the design parameters can be found in Appendix 5.

The inequality constraints are used to ensure only feasible magnetic designs are considered. In particular, the leakage inductance is given a lower boundary, because of the physical distances needed for insulation. The magnetising inductance is bounded by upper and lower limits. These two boundaries come from magnetics predesigns using [91]. The output inductor value is bounded by a lower limit so the primary peak current doesn't exceed the rated current of the MOSFET (see current equations from Appendix 5).

$$g_1(\boldsymbol{x}) = L_{lk,min} - L_{lk} \tag{7.7}$$

$$g_2(\boldsymbol{x}) = L_m - L_{m,max} \tag{7.8}$$

$$g_3(\boldsymbol{x}) = L_{m,min} - L_m \tag{7.9}$$

$$g_4(\boldsymbol{x}) = L_{o,min} - L_o \tag{7.10}$$

The equality constraint is the voltage ratio equation, taking into account the maximum of the voltage range and the duty cycle loss associated with the corresponding maximum power.

$$h(\boldsymbol{x}) = \left(D_{max} - \frac{4mL_{lk}fP_{max}}{V_{in}^2}\right)V_{in}m - V_{o,max} \tag{7.11}$$

With the problem in the standard form, an optimization algorithm can be used to determine the $\boldsymbol{x}$ parameters minimizing *f*. For the design presented in this chapter we used the Excel-embedded Generalized Reduced Gradient non-linear solver [92].

7.2. Implementation of 6.6 kV 83 kW PSFB

The dimensioning procedure given in section 7.1 is used for a reduced scale prototype of ratings 1.2 kV input, 6.6 kV output (one third of 20 kV) and 83 kW power rating (one third of 250 kW). The schematic of the converter is shown in Fig. 7.1. The choice of having two transformer secondaries is made following several considerations. First, it enables the use the rectifier design already tested and shown in section 6.2. It also permits the creation of a mid-point which may become useful for testing different groundings. Finally, it must be noted that two windings are natural anyway for a column type transformer.

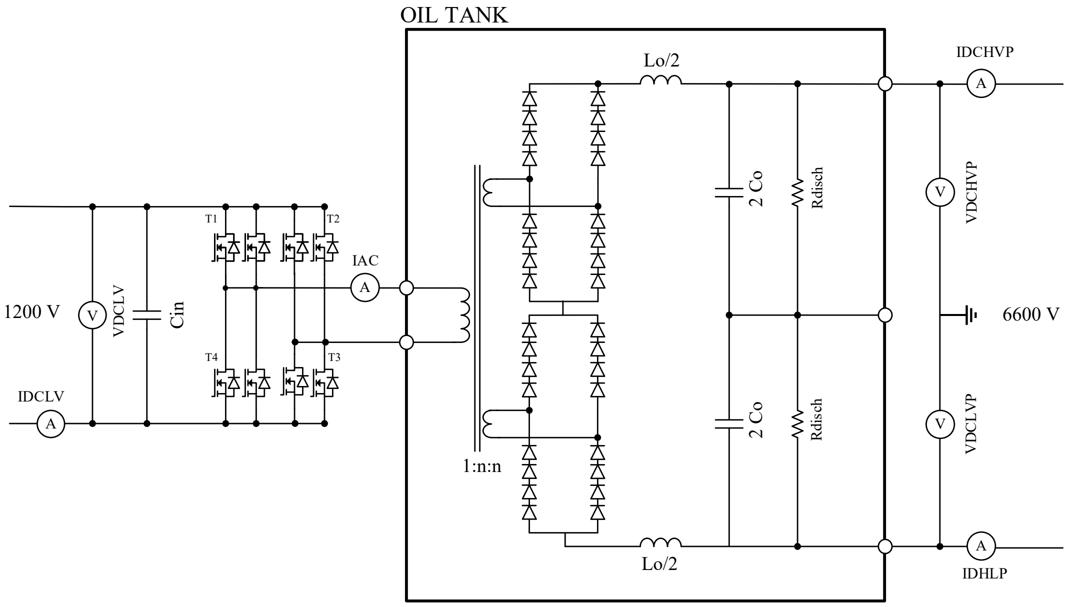


Fig. 7.1. Schematic of the 1.2 kV to 6.6 kV, 83 kW converter protoype

Section 7.1 describes the optimisation procedure giving base values for the components which are mainly inductors as they are impacting the current governing the inverter losses. Input and output capacitors must also be dimensioned. The table below summarises the design equations and their dependencies.

Table 7.1. PSFB parameter selection and final values

Component	Equation	Impact	Final Value
Input Capacitor C_{in}	$C_{in} = \frac{\Delta I_{in}}{\Delta t_{step}\ \Delta V_{in}}$	Limits ΔV_{in} to 5% of V_{in} with a step of power 0.5 *P* to *P* (simulations with control).	300 µF
Leakage inductance L_{lk}	From optimisation	Limit to ZVS operation / Duty cycle loss	8 µH
Magnetizing inductance L_m	From optimisation	Magnetizing current participating in ZVS / Efficiency at low power	1.9 mH
Transformer ratio $m=2*n$	From optimisation	Design to achieve needed maximum voltage ratio considering duty cycle loss. Tradeoff with leakage inductance.	2 * 3.25
Output inductor L_o	From optimisation	Output current ripple / Primary bridge switching currents	5.33 mH
Output capacitor C_o	$C_o = \frac{\Delta I_o}{16\, f\ \Delta V_o}$	ΔV_o of 5%	200 nF

It must be noted that the parameters obtained from the optimisation procedure are not used directly for the component designs. Indeed, the actual manufacturing of the MFT requires a value of transformer ratio resulting from integer number of turns. Equations (7.11) (voltage ratio condition) and (7.6) (lagging leg ZVS condition) are updated with this consideration and plotted in Fig. 7.2 and Fig. 7.3. The blue points represent the possible designs considering achievable transformer ratio considering reasonable interger number of turns. It shows that the best combination of leakage inductance, transformer ratio and ZVS limit is achieved for $m=2n=2\text{x}3.25=6.5$ and a value of leakage inductance close to L_{lk} = 10 µH. The target value of

8 µH is chosen for the MFT design in order to keep a safety margin and make sure to achieve the required voltage ratio at maximum power. One can note that a slightly lower ZVS limit can be achieved with a higher value of leakage inductance around 15-18 µH. However, this value strays from the value optained from the optimisation procedure. This means that the associated increase in transformer ratio to ensure the voltage conversion ratio must lead to a reflected current at the primary generating losses degrading the European efficiency.

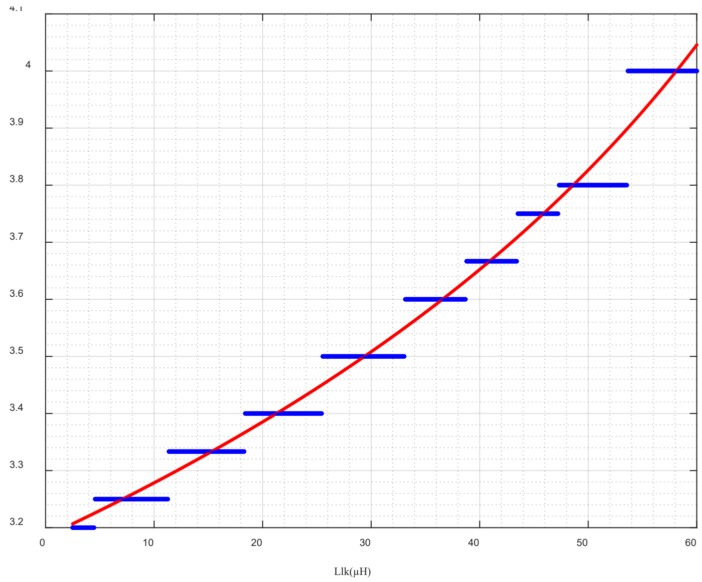


Fig. 7.2. Relationship between the transformer turn ratio and leakage inductance (continuous in red, considering integer number of turns in blue)

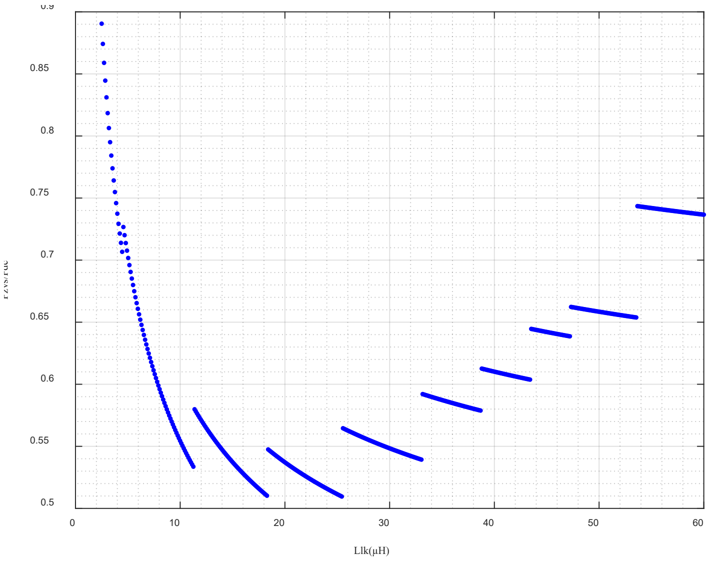


Fig. 7.3. Design trade-off between ZVS power limit and leakage inductance values resulting from integer number of turns condition

The magnetic elements were designed by the SuperGrid Institute team specialised in this domain, following the methods described in [91]. The diode rectifier is realised based on the association on a single PCB of two of the rectifiers presented in the previous chapter. The output capacitor is implemented with two capacitors in order to be able to output a middle point which can be used for experimental purposes. Each capacitor must be rated at least 2 C_o = 400 nF (from Table 7.1). From the existing components on the market, the ZES Silko PVDJP 21-4,5/1,5 is selected, of value 1.5 µF and nominal voltage rating 3.8 kV. The final designs and values of all elements are summarised in Appendix 6. The organisation of the elements inside of the tank is shown in Fig. 7.4. The design and manufacturing of the tank was performed by JST Transformateur in the context of a partenership with SuperGrid Institute.

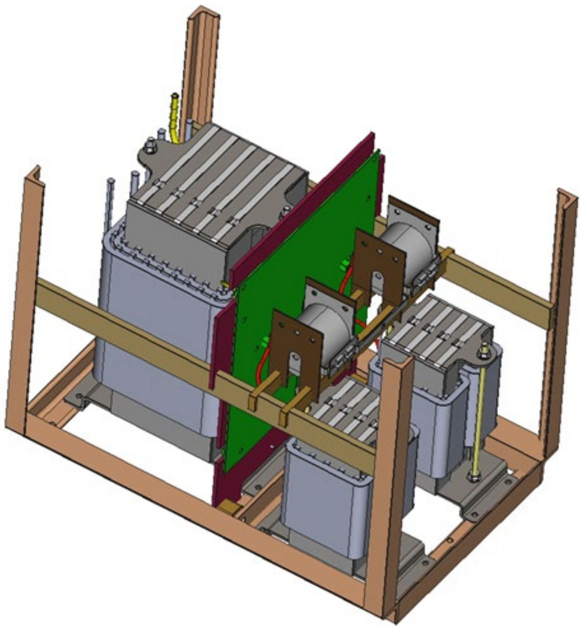


Fig. 7.4. Organisation of the elements inside of the tank, from left to righ: MFT, rectifier board, output inductors (bottom) and output capacitors (top)

The inverter is based on SiC MOSFET half-bridge power modules (Microchip MSCSM170AM039CT6AG). The choice of this module is not directly directed by the needs of the converter prototype of this thesis. Indeed, this inverter is designed for higher power operation, up to 250 kW. This specification leads to the choice of implementing the inverter with two power modules in parallel per leg. For the normal operation of the converter at 83 kW, the current rating of the modules (416 A) is thus much overrated. This design has the detrimental effect of not optimal power losses repartition. Indeed, the conduction losses will be very low but the important switching losses will impact the efficiency over the complete power range, especially its lower end. Moreover, the increase of number of modules increases the output capacitance of the switches, reducing the ZVS range.

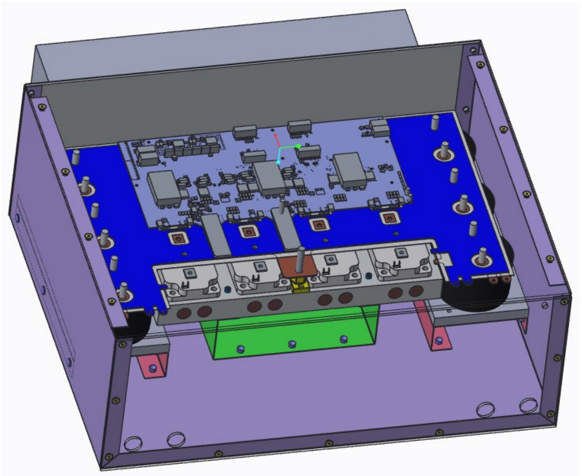


Fig. 7.5. 250 kW rated inverter implementation with two half-bridge power modules per leg (53 cm x 58 cm x 21 cm)

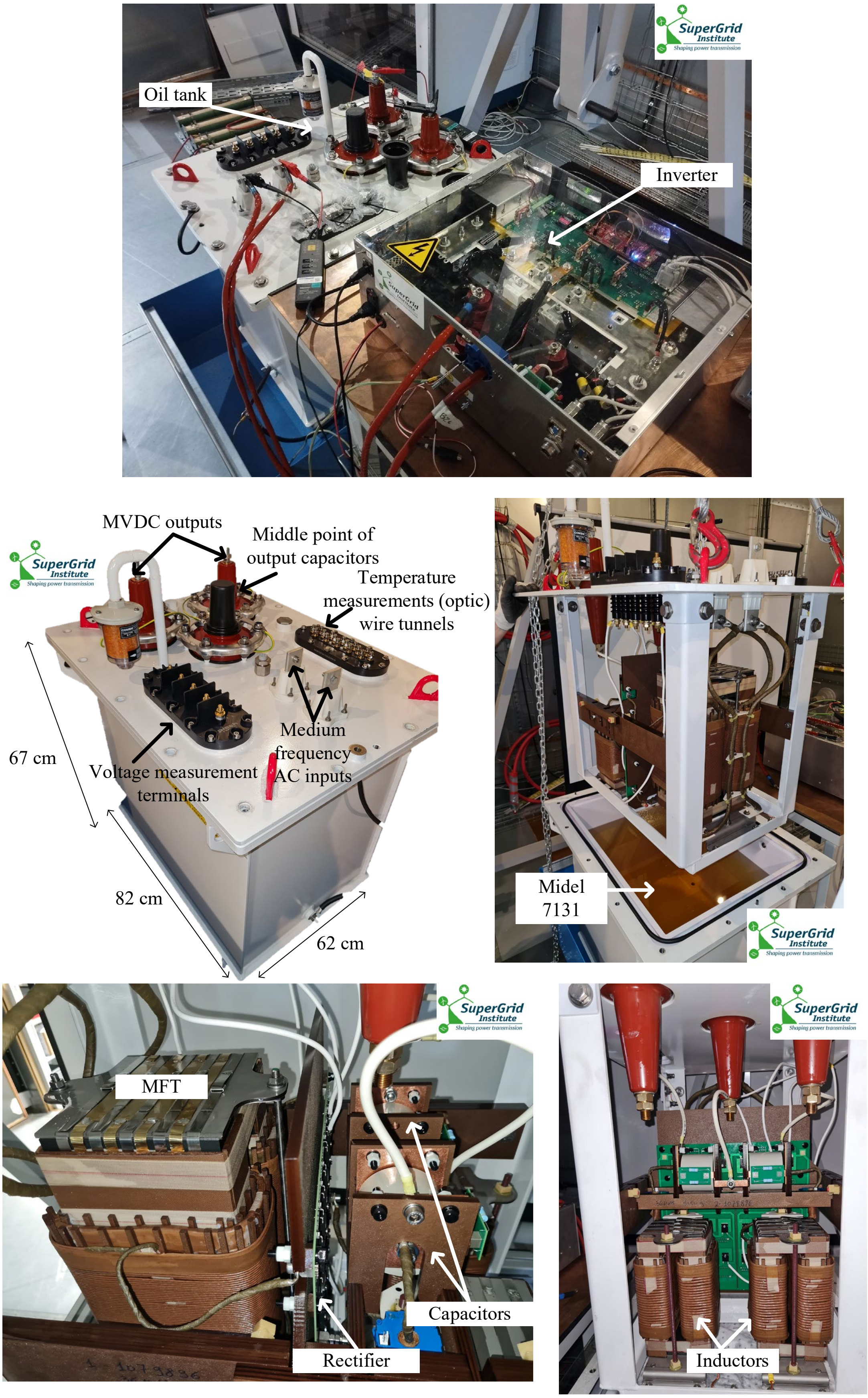


Fig. 7.6. Implementation of the DC-DC converter prototype, top) complete converter composed of the inverter and oil tank, middle) oil tank, closed and open, bottom) elements inside of the tank

The complete converter final implementation is represented in Fig. 7.6. In order to be able to test the converter at its rated power and voltage an active load converter is used to form a back-to-back circuit as shown in Fig. 7.7. The description of the test bench including the active load is given in Appendix 3.

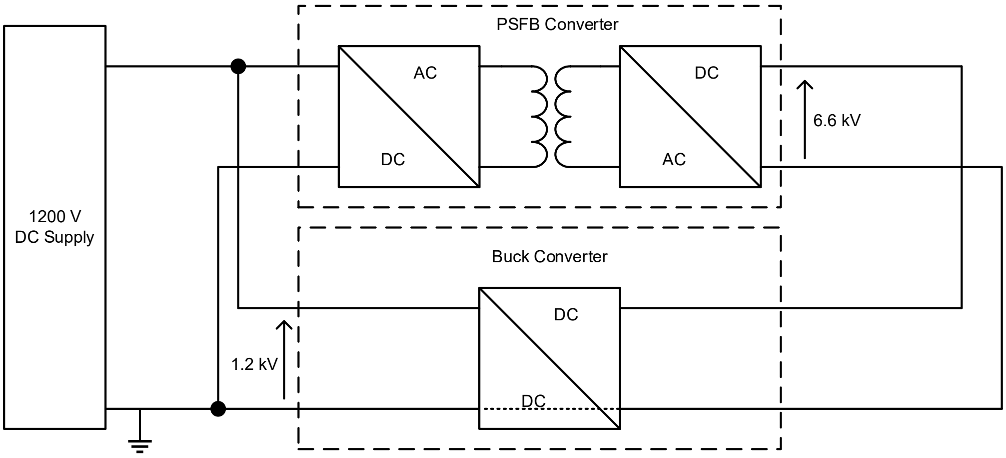


Fig. 7.7. Back-to-back circuit, with Buck converter used asan active load

7.3. Operation validation

In this section, the converter prototype is tested at different operating points in order to check several properties of the circuit. The converter simplified schematic with the definition of the observed quantities is reminded in Fig. 7.8. The operation of the inverter at nominal voltage and power is shown in Fig. 7.9.

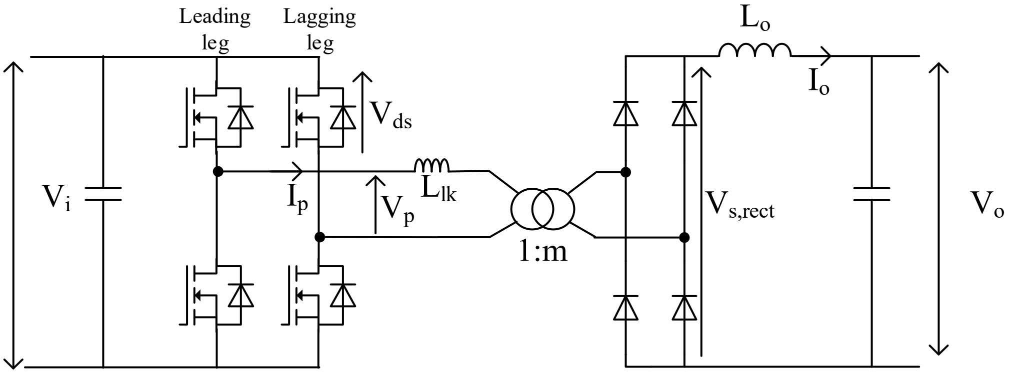


Fig. 7.8. Simplified schematic of the PSFB prototype

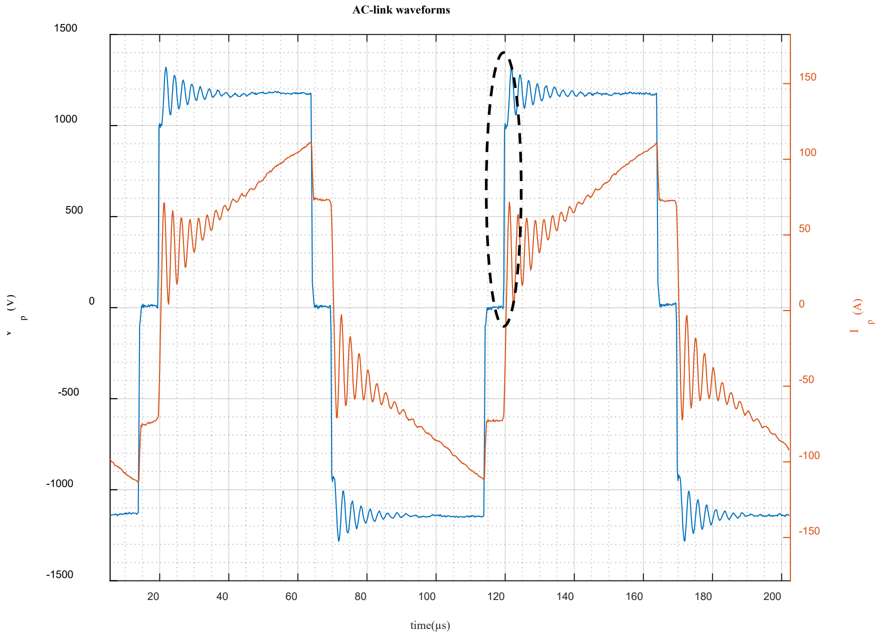


Fig. 7.9. AC-link waveforms at nominal voltage and power, voltage V_p in blue and current I_p in red

A first observation can be made on the important oscillations particularly apparent on the current. This is believed to be the result of a larger-than-expected primary to secondary and secondary winding parasitic capacitances of the transformer. Indeed the primary to secondary capacitance is measured as 1.8 nF, 50% larger than the design value given in Appendix 6. The secondary winding capacitances has not been measured. This leads to large oscillations on the rectifier voltage as can be seen in Fig. 7.10 showing the voltage $V_{s,rect}/2$ at the terminals of one of the two rectifiers represented in Fig. 7.1. However, the peak voltage doesn't translate into the diodes reaching their breakdown voltage. These oscillations also appear on the inductor voltage, as V_o is clamped. This leads to oscillations on the inductor current, which is reflected to the primary (Fig. 7.9).

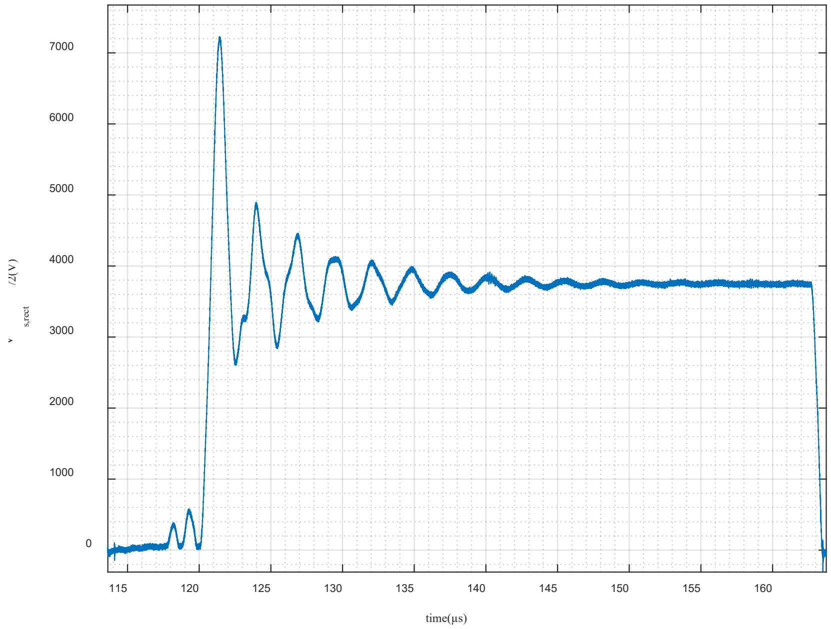


Fig. 7.10. Voltage at the terminals of one of the two rectifiers $V_{s,rect}/2$, showing large oscillations

Fig. 7.11 shows a zoom (represented by the circled zone in Fig. 7.9) of the AC-link voltage waveforms at the switching instant of the lagging leg. This is shown for several operating powers so as to observe the different operating modes.

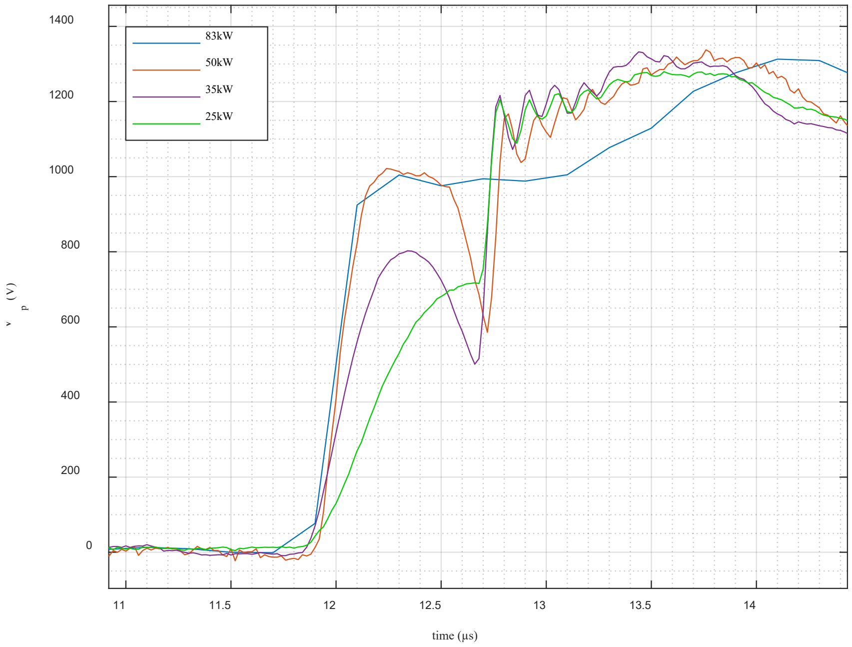


Fig. 7.11. AC-link voltage at turn-on of the lagging leg for different operating powers, showing the transition from ZVS to no ZVS.

Several observations can be made on these waveforms, leading to the identification of the ZVS and DCM limits. The different operating points exhibit typical sinus waveforms resulting from the resonance of the leakage inductance and the parasitic capacitances during the dead-time transition between the conduction periods of the two MOSFETs of the lagging leg. For the 83 kW and 50 kW points, the energy in the leakage inductance is sufficient to reach the DC-link level and the sinewave is thus clamped. This corresponds to the V_{ds} of the switch decreasing to 0 V before turn-on. The plateau is here observed slightly above 1000 V and not at the DC-link voltage due to the voltage drop of the cable inductance under the high di/dt occurring at the transition between the positive and negative alternance. Indeed, the measurement of V_p is done at the tank terminals. The 50 kW waveform shows that the ZVS limit is close to this value, as only the very peak of the sinewave is cropped. This coincides with the theoretical ZVS power limit of 47 kW given by Fig. 7.3 with the target leakage inductance of 8 µH. Below this limit, the energy in the leakage inductance is not sufficient and the peak of sinewave does not reach the plateau voltage, as can be observed for the 35 kW and 25 kW operating points.

Fig. 7.11 also shows what happens when the dead-time is too long (850 ns here). For the 50 kW operating point, the energy in the leakage inductance is enough for ZVS and the voltage reaches the plateau, clamping the sinewave. However since the dead-time is too long, the resonance ends up decreasing the voltage and partial hard switching happens (at approximately 12.7 µs). In Fig. 7.12, the V_{ds} waveforms of the lagging leg, with correctly tuned dead-time (600 ns), are shown in and out of the ZVS zone. It can be observed here that the complete DC-link voltage of 1200 V is discharged when in ZVS (no voltage plateau appears as the measurement is done at the inverter terminals). The dead-time is tuned at the quarter of the resonant period in order to minimise the voltage at the switching instant even when ZVS is not achieved.

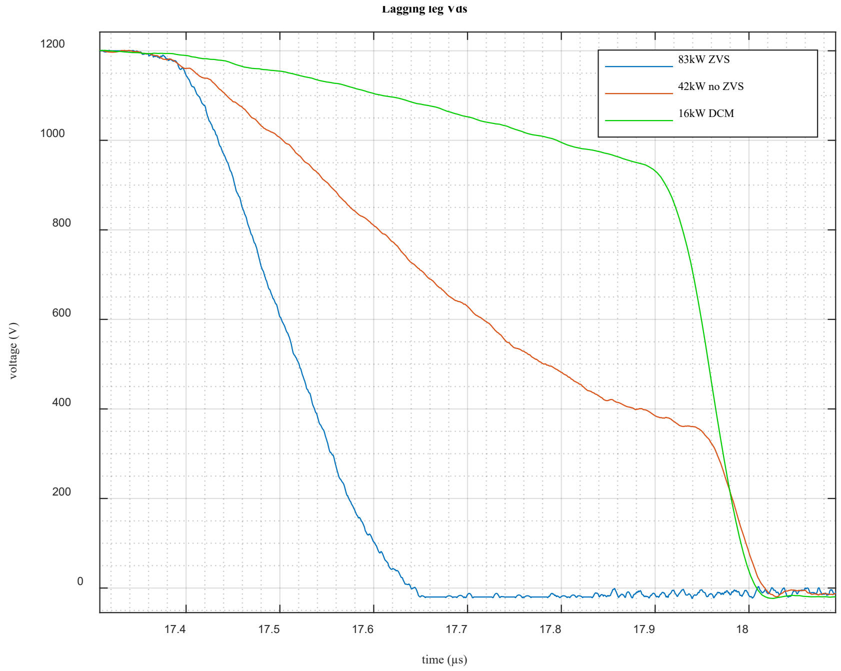


Fig. 7.12. Drain-source voltage of a lagging leg MOSFET during turn-on dead-time (600 ns)

One can also see in Fig. 7.11 that the frequency of the sinewave is different for the 25 kW operating point. This is a consequence of the DCM operation of the converter at this power level. Indeed, the resonance frequency of the circuit changes between the two modes because only one of the output capacitance of the bridge MOSFETs is involved in the resonance when two are in CCM. This also explains the relatively small difference in peak values of the sinewaves between 35 kW and 25 kW (800 V and 720 V, respectively), as less energy is required in the second case because of the lower capacitance value. This transition between CCM and DCM corresponds to the right power level range, as the theoretical value found from equation (4.19) is 29.8 kW.

Table 7.2. Comparison of measured and theoretical operating modes power limits

Operating Mode	Measured power limit	Theoretical power limit
ZVS / no ZVS	~50 kW	47 kW
CCM / DCM	25-35 kW	29.8 kW

7.4. Chapter conclusion

This chapter has presented the implementation of the 1.2 kV to 6.6 kV 83 kW DC-DC converter prototype. A formalisation of the dimensioning of the PSFB has been proposed as an optimisation problem aiming to maximise the European efficiency of the inverter while ensuring the right voltage conversion ratio. The implementations of the different elements of the converter are presented as well as their organisation inside of the oil tank. The ZVS and DCM zones transitions are observed experimentally and compared to the theoretical values, showing good match. However, it is also observed that the larger-than expected primary to secondary capacitor of the MFT results in important oscillations at the secondary, also impacting the primary current. This point must be carefully taken into account during the design and manufacturing of the MFT for an MV PSFB.

8. Losses measurements

From the motivation chapter of this thesis, the efficiency of the DC-DC converter has been identified as the criteria enabling a sensible use of MVDC for the integration of distributed PV sources. The objective of 99% European efficiency has been set. The accurate measurement of losses is thus paramount when one wants to verify the performance of such a high efficiency converter. This section presents the selection and implementation of an appropriate method to measure the power losses off the converter prototype and uses it to assess the performance of the 83 kW prototype.

8.1. Losses measurement methods

This section presents the different methods for measuring the efficiency of a converter. The short-comings of the electrical methods are highlighted and a calorimetric method is selected to be applied to the converter prototype.

8.1.1. Electrical methods

The first, obvious, method is based on electrical measurements of the input and ouput power of the converter using power analyser. The difference corresponds to the power losses. However, when using the input-output method for DC-DC converters carrying high levels of power, challenges are raised. Since the efficiency of the studied converter is very high, losses are small in proportion to the rated power, and therefore difficult to measure. Also, because of the medium voltage output, sensing the output voltage requires probes with a voltage divider, which adds a source of uncertainty to the probes own uncertainties. As the input and output voltages and currents are not perfectly DC, the high frequency harmonic content is also a source of uncertainty. It was shown in [50] that such input-output measurement of a high efficiency MV converter would be too uncertain. Indeed, the uncertainty associated with the electrical measurement of the 99% efficiency of a 25 kW, 7 kV inverter (based on 10 kV SiC MOSFETs) was found as ±0.83% (98.17…99.83%), which makes the measurement unsuable.

From this first observation (the uncertainties on the measurement of high transmitted powers are of the same order of magnitude as the power losses), one can understand that losses must be measured directly. In order to do so, a set-up such as the one shown in Fig. 8.1 can be implemented. In this scheme, the DC power supply only provides the power losses of the circuit, while the rated power only flows in the closed loop. Here, the measurement of the power supplied is accurate since the losses are measured directly, and not as the small difference between two large quantities. However, losses of the complete circuit are measured, including the cables.

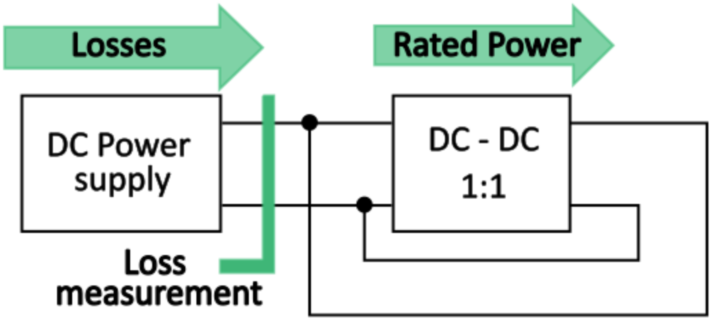


Fig. 8.1. “Stand-alone” test set-up for the measurement of power losses

Alas, this method is only applicable for converters with a voltage ratio of 1:1 since the output is connected to the input. This limitation can be overcome by using the “back-to-back” or opposition method [93] scheme presented in Fig. 8.2, with one converter of ratio 1:r and the other of ratio r:1. In this case, the supplied power corresponds the power losses of both converters. The repartition between the two converters is known only in the case of identical, bidirectional converters. Indeed, bidirectional converters can be structuraly symmetrical, with the same components on their respective low voltage and medium voltage sides. With unidirectional converters (as is the case with the PSFB studied here), the 1:r converter would have diodes on the medium side where the r:1 would have controlled semiconductors. Therefore, the losses of the two converters cannot be considered equal and it is no longer possible to separate the losses of each converter from the measurement of the total losses.

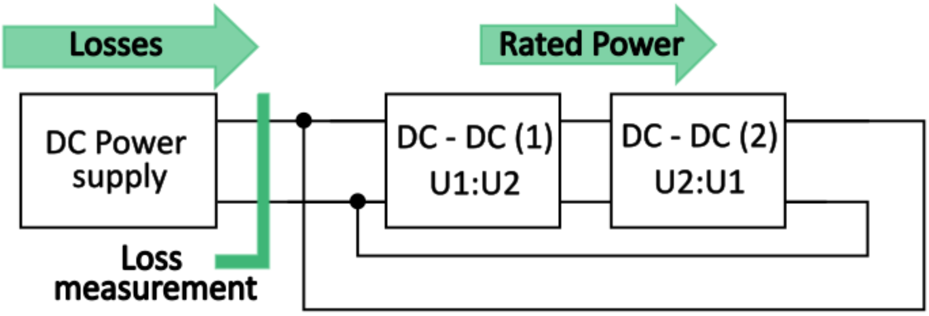


Fig. 8.2. “Back-to-back” test set-up for the measurement of power losses

Since the electrical methods are either not accurate enough or not implementable for an unidirectional step-up converter, one must resort to calorimetric methods.

8.1.2. Calorimetric methods

The different categories of calorimetric methods are summarised in the figure below.

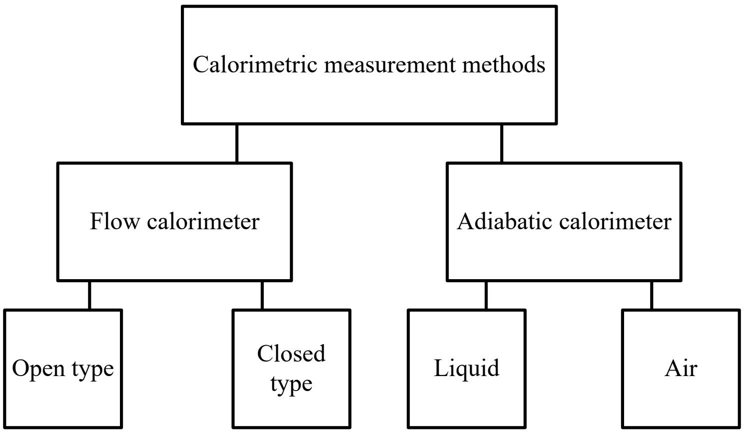


Fig. 8.3. Mapping of the different calorimetric methods

In flow calorimetry, a fluid is used to collect the heat generated by the power losses. The power losses can be estimated knowing the specific heat capacity c_p of the fluid, by measuring the temperature difference between inlet and outlet (ΔT) and the mass flow-rate $\dot{m}$ of the cooling fluid at equilibrium [94].

$$P_{loss} = c_p\,\Delta T\,\dot{m} \tag{8.1}$$

In open type calorimeters, the cooling fluid is air as the device under test is directly put in the measurement circuit. In closed type, a different fluid can be selected, such as water, as the measurement circuit uses an heat exchanger in contact with the device under test. This second type is generally more accurate as the cooling fluid is less sensitive to environmental conditions than air. As the converter prototype is passively air-cooled, the implementation of a flow calorimeter would require an additional cooling circuit. This makes this second kind of method difficult to apply, as it changes the general operation of the converter.

An adiabatic calorimeter does not use any flow-rate measurement as the device under test is fully immersed in the fluid that collects all of the heat generated by the power losses, with no exchanges with the environment. The power losses are then calculated as [95]:

$$P_{loss} = \frac{\Delta T \, C_{th}}{t} \tag{8.2}$$

with C_{th} the total heat capacity inside of the enclosure and t the duration of the test during which the liquid temperature has increased by ΔT. It is precised in [95] that equation (8.2) is true only for constant power dissipation over time, uniform temperature in the calorimeter, and constant heat capacity. The test is realised in a transient state as the liquid is continuously heated up. This is of parlicular interest to keep short the tests of massive objects such as the inverter and especially the tank. However, this kind of calorimeter is hardly conceivable considering the size of the converter prototype. This last point leads to the choice of a transient calorimetric method that uses air as the ambient medium.

8.1.3. Selected method

The method presented in [96] uses an open flow calorimeter (in the sense that heat is echanged with the surrounding air), but has a transient operation, much like an adiabatic calorimeter : this method is based on measuring the time-derivative of the temperature difference with the ambient air (ΔT), refered to as the slew rate (Sr) in this document. In [96] the method is applied to estimating the losses of power modules in an automotive inverter. Losses measurement using this method is divided into two stages: a first calibration stage, followed by a measurement stage. The figure below shows a diagram explaining the main steps of the method.

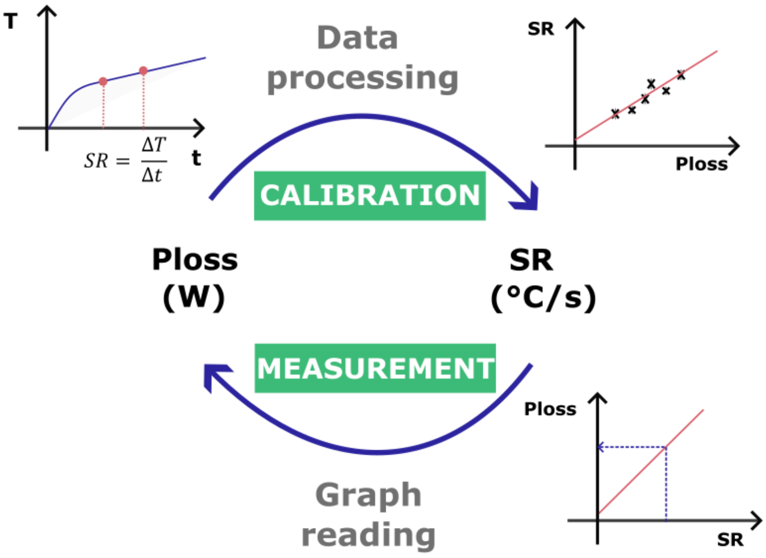


Fig. 8.4. Steps involved in the power losses measurements presented in [96]

For the calibration stage, temperature elevation data during the thermal transient response is monitored for different known values of DC power injected in the system under test. The temperature data is then processed (filtering out measurement noise) and the temperature Sr is calculated from the same temperature range for each operating point. These Sr values are processed and plotted on an Sr vs Power injected graph. The resulting point cloud is used to fit a calibration curve, which establishes a relationship between Sr and electrical losses. One calibration curve is specific to an object and a test environment. The calibration step must therefore be repeated for any change in configuration or thermal conditions (air flow, temperature sensor position).

The measurement operation comes in a second stage, under the same thermal conditions as the calibration phase. During this stage, the transient temperature variation is monitored, when the inverter is operated under a given load, with unknown power losses. Following similar data processing steps as in the calibration stage, a Sr value is calculated. Finally, the corresponding loss value is deduced by reading the calibration graph.

The relative uncertainties associated with the power losses measurement using this method are estimated to be less than 5% in [96], with the temperatures measured using Negative Temperature Coefficient (NTC) resistor. This is considered very satisfactory compared to the other method that does not require changing the converter environment (the "input-output" electrical method).

8.2. Intermediate validations

Before it is applied on the whole converter, the transient calorimetric method is applied to different elements to validate its performance. This section is based on the work performed with Marion Bonnay during her internship [97].

8.2.1. Validation on the natural-air-cooled inverter

The methodology is applied on the prototype inverter in order to verify its accuracy. In the calibration stage, the circuit must generate known losses. For this purpose, a high-current source supplies the inverter DC input with reverse DC current, while the output is left unloaded. Conduction in the diodes generates heat, which is transferred to the aluminium plate. Transient temperature rise from 25°C to 60°C is measured by a PT100 temperature probe placed between the power modules, on the aluminium baseplate. The placement of the probe is shown is Fig. 8.5. A second probe is placed in the surrounding air, outside the inverter container, to measure the ambient temperature.

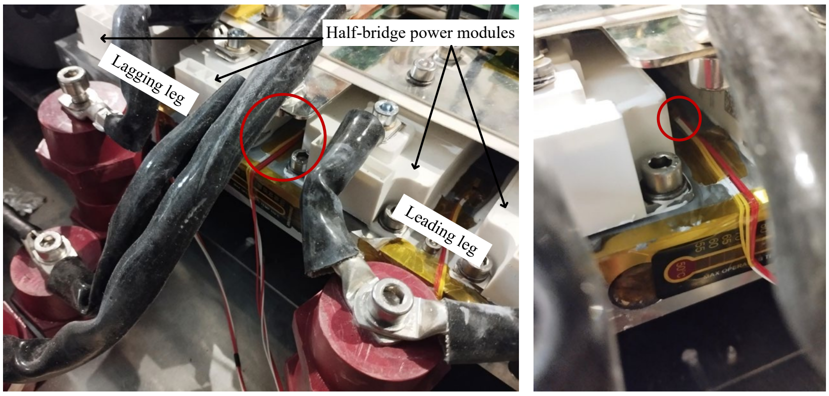


Fig. 8.5. Thermal calibration set-up of the inverter, red circle: position of the PT100 used for baseplate temperature measurement

Operating tests are carried out for a range of known power input values in the interval [50 W – 800 W], to cover light-load regions as well as rated-power operation. The result of the calibration are shown below.

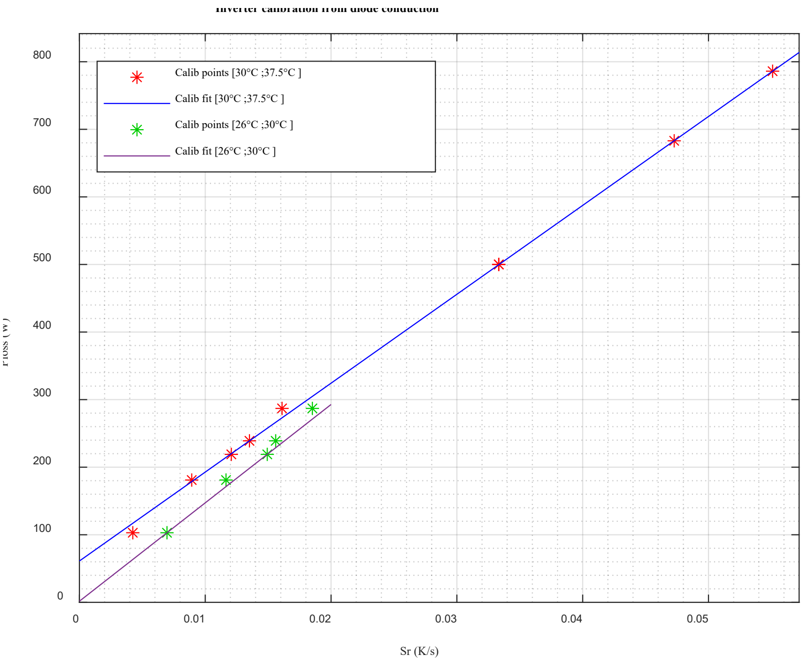


Fig. 8.6. Thermal calibration of the inverter, the temperatures in brackets are the temperature ranges of the aluminium baseplate from which the Sr are calculated.

It was not found possible to cover the complete power range with a single linear curve. Indeed it can be seen in Fig. 8.6 that the blue curve has an offset making it unsuable to detect powers below roughly 100 W. Therefore, in order to keep linear fitting as in [96], two temperature pairs are used to compute slew rates. The fitting of the purple curve is done only for power points below 300 W. When measuring a Sr on the tested object, if its value is below 0.015 K/s the purple calibration curve must be used and the blue curve conversely.

To validate the method, the calibration curve must then be applied in switching conditions, with known losses. This requires to measure the losses by other means. The circuit used for the method's validation is shown in Fig. 8.7: the inverter is connected to an inductive load (air-core inductor), and the power loss in the inverter is calculated from the basic definition:

$$P_{loss,inverter} = P_{DC\ injected} - P_{load} \tag{8.3}$$

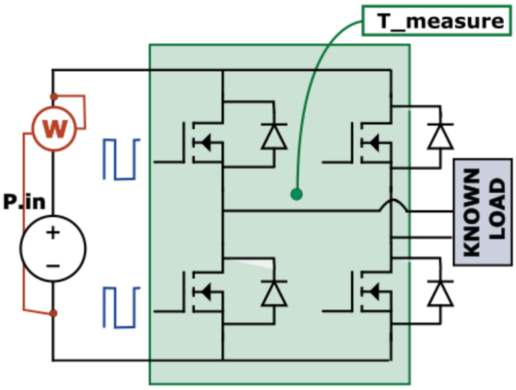


Fig. 8.7. Validation set-up schematic

In this electrical measurement method, the power loss in the inverter is obtained by subtracting the power loss in the inductor to the power injected. The power injected on the input is measured using a wattmeter, the current flowing through the load is measured using a current probe, and the time data for this switched current is collected using an oscilloscope. The temperature of the winding is also monitored to be used in the calculation of the losses in the inductor.

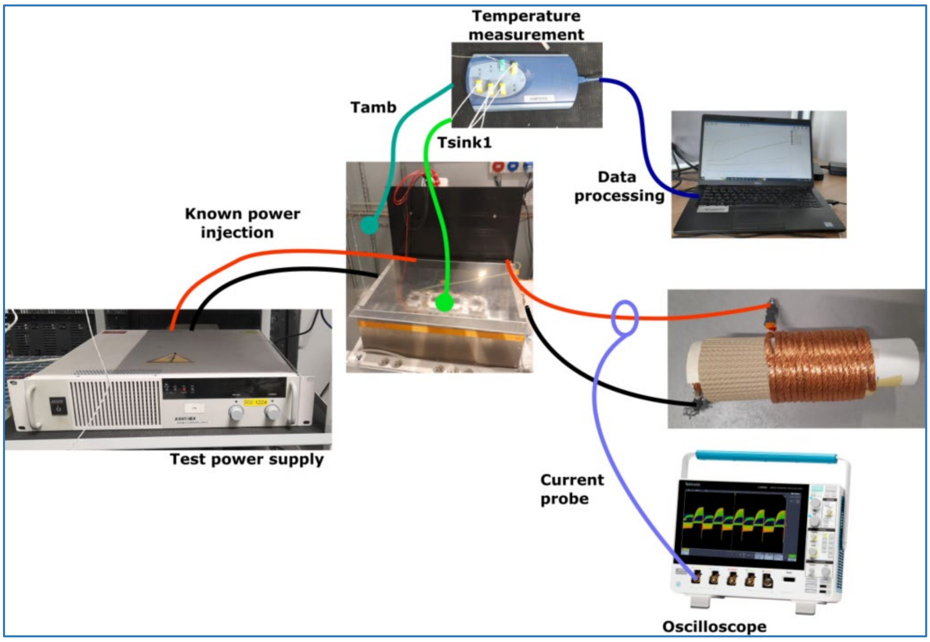


Fig. 8.8. Validation set-up implementation

In terms of layout, the test air-core inductor must be placed away from metal parts, to avoid induction phenomena and only have winding losses which are easier to estimate from a simple model. For the tests, it is therefore suspended in the air.

The losses in the test inductor are calculated by summing the joule losses generated by the conduction of each harmonic of the current delivered by the inverter. The following equation gives the expression for these losses:

$$P_{loss\text{,}inductance} = \sum_{i=1}^{n} R_{AC,i} \cdot {I_{AC,i}}^2 \tag{8.4}$$

where *i* corresponds to the order of the current harmonic generated on the output of the inverter, R_{AC} to the AC resistance of the test inductor at frequency corresponding to harmonic *i*, I_{AC} to the amplitude of the harmonic current. Thus, the calculation of losses in the inductance requires knowledge of the frequency content of the inverter output current, and of the AC resistance of the inductance for each current harmonic. The harmonic content is calculated by the FFT of the measured inductance current. The test inductor is characterised using an impedance analyser (Wayne Kerr 1J6505B). This characterisation gives the AC resistance of the test inductor over a given frequency range, at 20°C. In operation, since the windings temperature is higher than 20°C, the AC resistances vary and do not correspond to the characterisation data. To evaluate the AC resistance of the inductor for a different winding temperature, the Albach model detailed in [91] is used, which allows to fit the AC resistance of an inductor at a different winding temperature, from the $R_{AC}(f)$ characterisation data. The figure below shows the AC resistance vs. frequency graph, with the Albach model data fitted for a winding temperature of 20°C, compared to the characterisation measurement data.

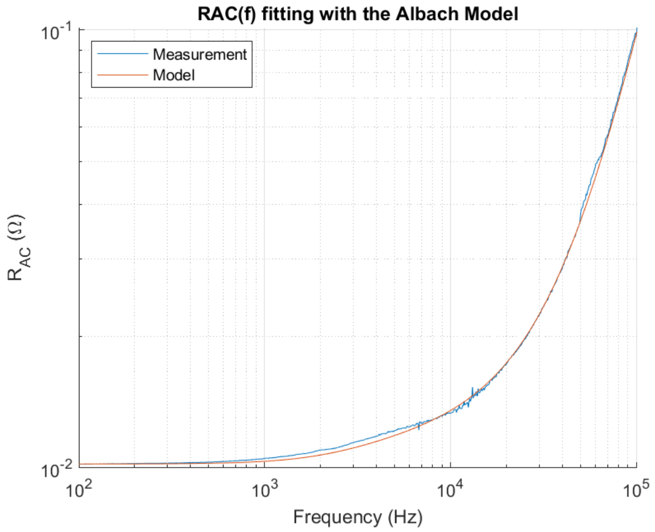


Fig. 8.9. AC Resistance over a frequency range - characterisation measurement (blue) and Albach model fit (orange)

Only two validation points are presented in Fig. 8.10 because of a material failure during the tests.

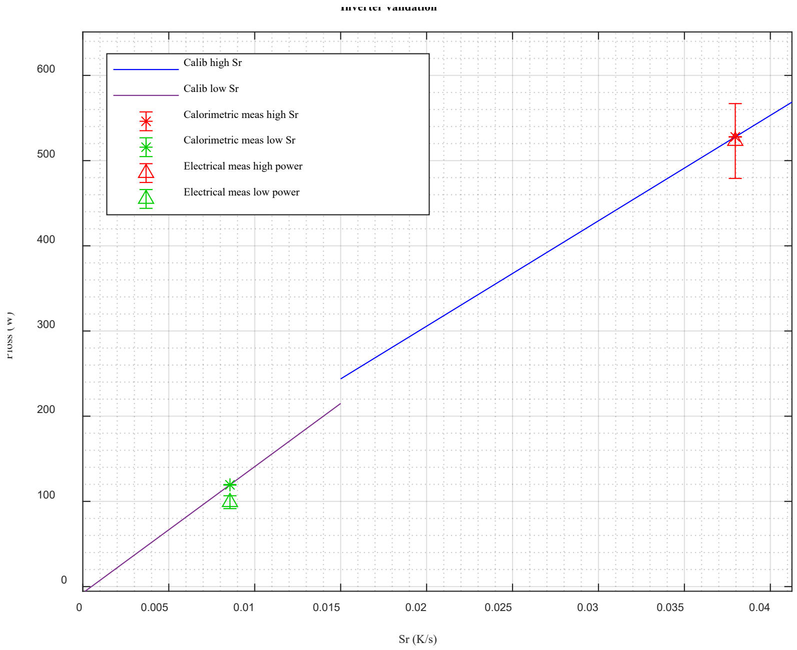


Fig. 8.10. Power losses calculated with the calorimetric and electrical methods

The following table gives the relative errors between the losses estimated using the calorimetric method and the losses estimated using electrical measurements.

Table 8.1. Relative errors between calorimetric and electrical measurements of the inverter losses

	Relative error	**Uncertainty**
Low power point	16%	±7.6%
High power point	1%	±8.4%

The important uncertainty comes mainly from the electrical method part, which has many uncertainty sources: current amplitude (probe), current frequencies (oscilloscope), R_{AC} (impedance analyser), source power (wattmeter). This shows the difficulty of measuring power losses electrically.

8.2.2. Validation of the applicability on the tank

The 83kW prototype is mainly composed of a natural-air-cooled inverter (discussed in the previous section) and an oil tank which contains the transformer and all the MVDC-side components. The validation of the selected method on the tank is particularly important as the original paper [96] is focusing on power module losses in an inverter, a configuration which is comparable to the input inverter of our PSFB. To that effect, a test bench with a small-scale model is set up. It consists of a cut-out jerrycan filled with Midel 7131 oil, into which resistors are immersed. A Plexiglas plate is placed on the upper part of the tank to limit convective exchanges with the ambient air. The configuration of the test bench is adapted to investigate the following items: location of the temperature probe and representativity of the calibration resistor.

The oil in the tank is in contact with all the components, so it collects all the heat they generate. Measuring the oil temperature should therefore give a perfect image of the losses. Unfortunately, the oil temperature is not uniform in the tank, as natural convection occurs in the oil. Furthermore, there is no certainty that the oil flows caused by natural convection remain identical when the distribution of the losses change between the components. Evaluating these sources of uncertainty is the objective of the test described here.

Regarding the location of the temperature probes, a first probe is placed on the outer wall of the oil tank, and a second probe is placed inside the tank, immersed in the oil. Indeed, the oil tank gives the opportunity to measure the temperature of a liquid containing all of the power loss sources, similarly as in the adiabatic calorimeter method. The measurement on the tank wall is closer to the method implemented on the inverter. Another temperature probe is also placed in the ambient air in order to calculate the relative temperature increase. The set-up is shown in Fig. 8.11. The thermal camera picture shows that the temperature of the tank wall is constant for a certain horizontal level. A gradient is observed from high temperatures at the top to lower temperatures at the bottom.

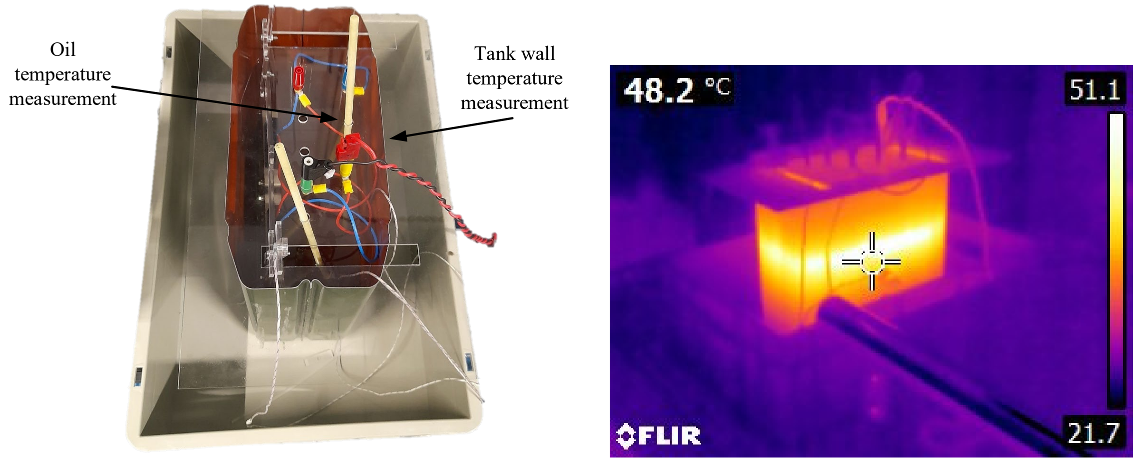


Fig. 8.11. Left) small-scale tank for intermediate validations, right) thermal camera picture during test

To assess the effect of the distribution of the heat sources in the tank, first a calibration campaign is carried out using a flat rectangular resistor (Stego HV 031, 132 Ω) immersed in the tank of the small-scale model. Known power steps are injected into the calibration resistor and the temperature rises in the oil and on the tank are measured. The corresponding Sr are calculated. In a validation stage, a second, identical, resistor is added. The aim is to emulate a different location and distribution of losses in the tank, as it would be the case with the actual tank components (MFT, rectifier, inductors). A resistor with a cylindrical ceramic heatsink is also selected to observe the influence of thermal properties on the temperature rise measurements. Tests are carried out by injecting power into this resistor placed vertically and then horizontally in the tank, to study the influence of convection conditions in the tank on the various measurements. The different set-ups are summarised in Fig. 8.12.

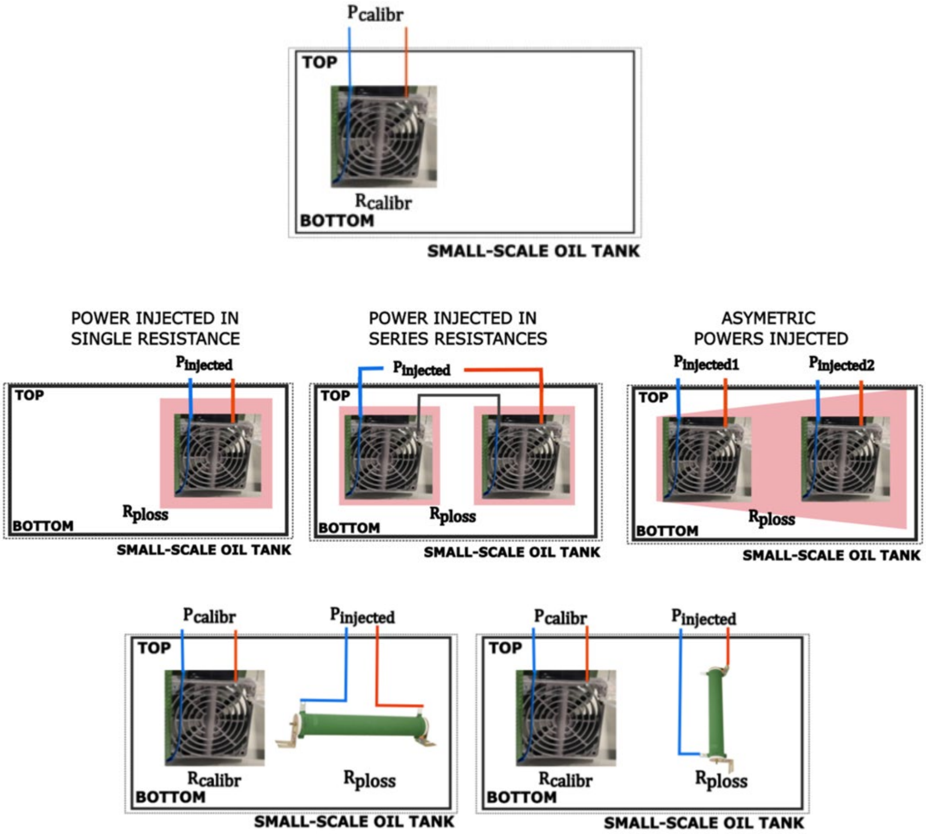


Fig. 8.12. Test set-ups for the study of representativity of resistor-based calibration: calibration stage (top), validation stage with modification of the location of the losses source (middle), validation stage with the modification of the thermal characteristics of the losses source (bottom).

The temperature ranges over which the Sr is calculated are [35°C 45°C] for the tank wall and [45°C 55°C] for the oil measurement. The results of the calibration and validation stages are shown in Fig. 8.13 and Fig. 8.14.

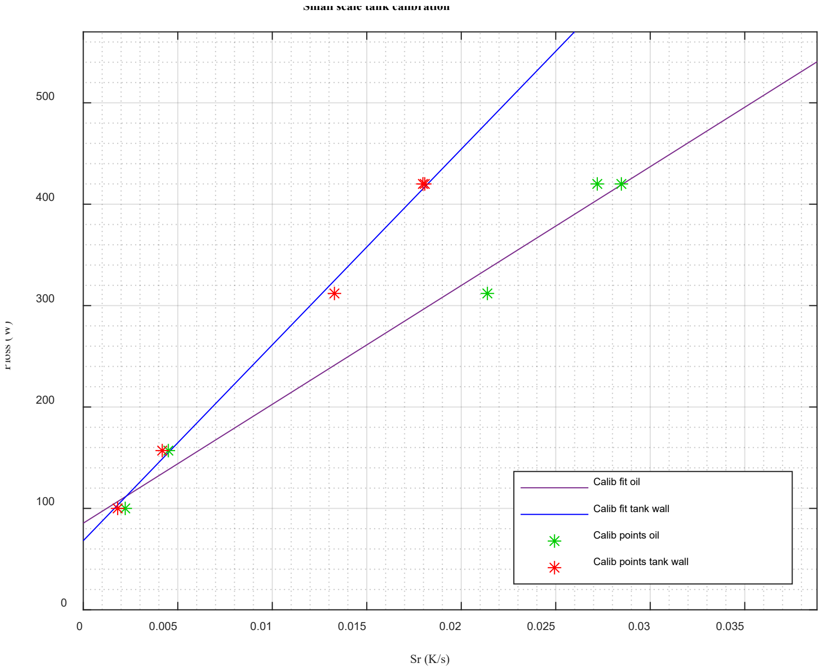


Fig. 8.13. Calibration points and fitted curves for the oil measurement (green,purple) and tank wall (red,blue)

The maximum relative error between the calibration points and the calibration curves are 11% of the oil measurement and 5.2% for the outer wall.

Measurements performed on the outer wall of the tank result in a more linear distribution of losses as a function of temperature rise. The calibration point at 420 W is performed twice at a different ambient temperature (24°C, 28°C). This second point also allows to note that the measurement on the outer wall of the tank is more robust to ambient temperature variation than the measurement in the oil.

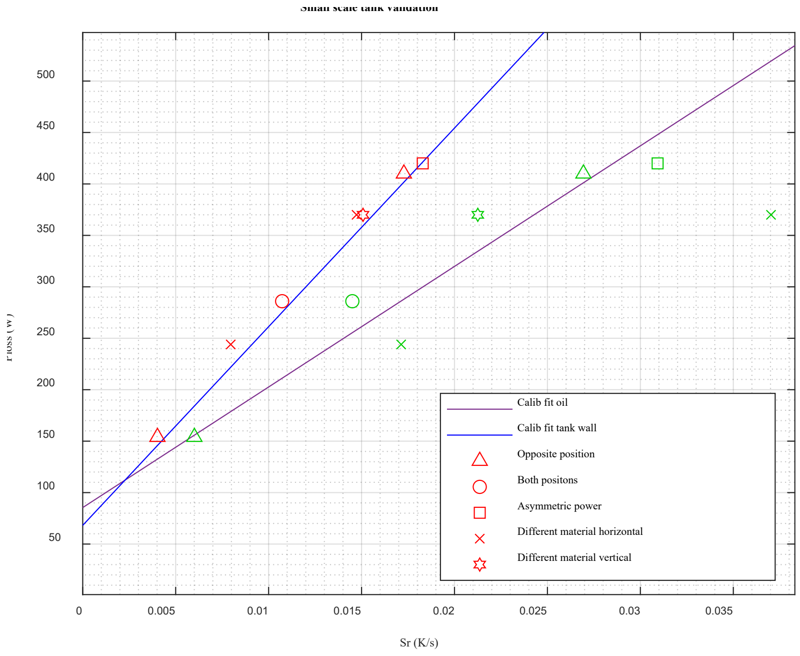


Fig. 8.14. Calibration curves and validation points for the oil measurement (purple,green) and tank wall (blue,red)

The maximum relative error between the validation points and the calibration curves are 40% for the oil measurement and 9% for the tank outer wall measurement. For both the temperature measurements the biggest relative errors between the electrical measurement and the respective calibration curve occur for the setup with the ceramic resistor positioned horizontally in the tank. One could have predicted that the oil measurement method would lead to worst results as it was stated in section 8.1.2 that the adiabatic liquid calorimeter method relies on an uniform temperature in the calorimeter. This is absolutely not the case here since no stirring is performed, contrary as in [95].

It can be deduced from these tests that the temperature measurement on the outer wall of the tank is more robust to variations in the geometry or technology of the loss source. Heat conduction in the metallic wall of the tank probably produces an averaging phenomenon, which makes the measurement on the outer wall of the tank more robust to changes in the convection conditions and the proprieties of the heat source. With a maximum relative error of 9%, this measurement method is considered satisfactory (compared to the high uncertainties of electrical methods) and selected for the power losses measurement of the full prototype.

8.3. Results on 6.6 kV 83 kW prototype

The previously described method is applied to the full-scale prototype in order to measure its efficiency. The measurements are compared with the theoretical models and difference are explained. The prototype European efficiency is finally computed and compared to the objective efficiency.

8.3.1. Calibration and measurements

Both the inverter and the tank are calibrated in their final implementation. The calibration of the inverter is done using a current source dissipating power in antiparallel diodes (as previously). Resistors (4, 132 Ω Stego HV 031) are placed in the tank for the calibration step together with the other elements, and supplied with DC power using the feedthrough connectors visibles in Fig. 8.15.

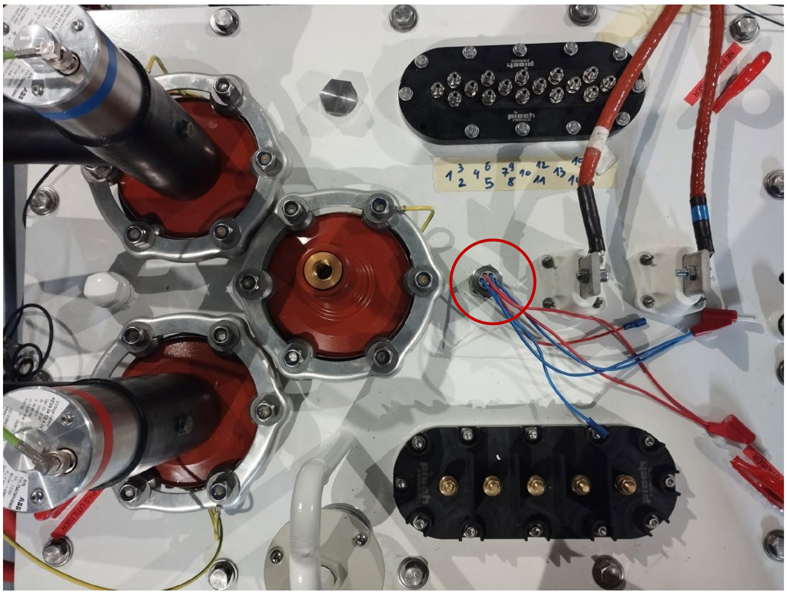


Fig. 8.15. Top view of the tank, with feedthrough connector circled in red

The temperature transient curves are presented in Fig. 8.16, with their associated Sr calculation zones (black lines). Only one Sr zone is used for the calibration of the inverter here, as it was found that the linear fitting is correct for all points in the targeted power losses area. One can appreciate the advantage of the transient calorimetric method by looking at the duration of the tests. Indeed, with the selected Sr calculation zones, the inverter tests can be kept below 20 minutes and the tank test below 2 hours. This is especially important for the tank as its thermal stability would be reached after more than a day (the estimated thermal time constant of the tank is 4.9 hours).

The resulting calibration curves are shown in Fig. 8.17. It can be observed that the uncertainties associated with the tank calibration are higher than those associated with the inverter. That is because the temperature elevation used to calculate the slew rate of the tank wall is lower than for the inverter. The formulas used for uncertainty calculations can be found in Appendix 7.

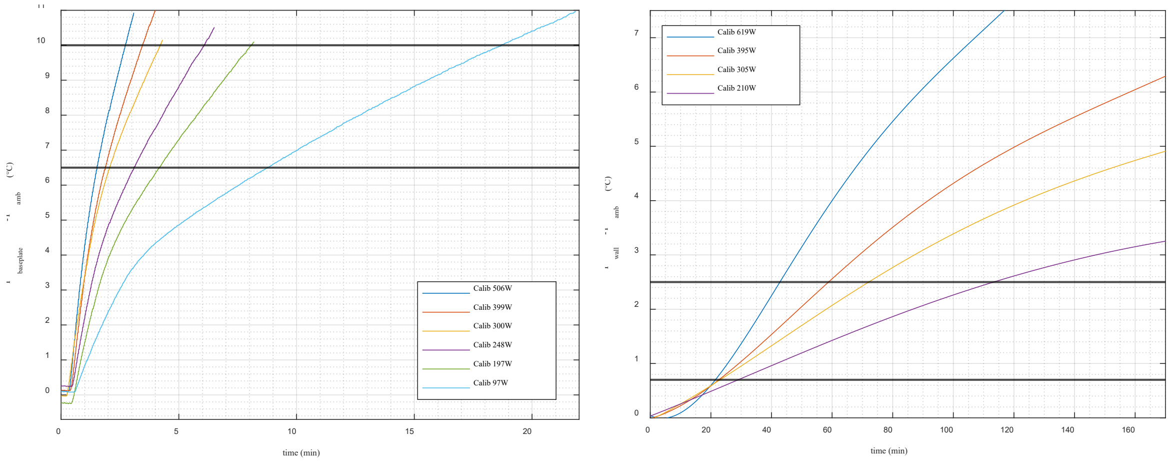


Fig. 8.16. Left) inverter: transient increase of the temperature difference between the aluminium baseplate and the ambient (black lines represent the [6.5 10]°C temperature range over which the Sr are calculated), right) tank: transient increase of the temperature difference between the tank wall and the ambient (black lines represent the [0.7 2.5]°C temperature range over which the Sr are calculated)

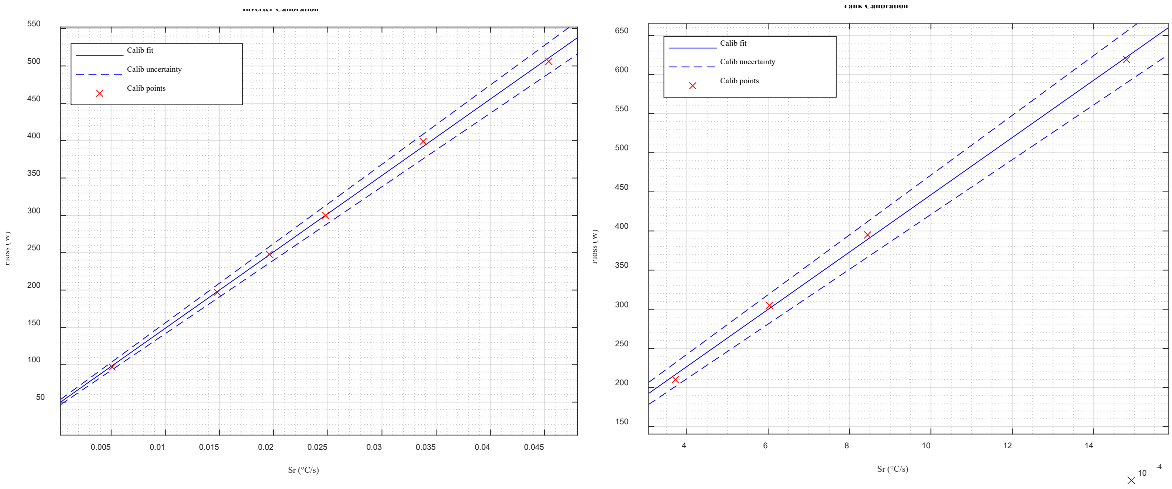


Fig. 8.17. Left) calibration curve of the inverter from diode conduction, right) calibration curve of the tank from resistive heating (low Sr values are not represented as no measurements are done in this range)

The converter prototype is operated at the different power loads needed to compute the European efficiency. Power steps are applied and the temperature of the inverter and the tank is measured. Measured slew rates are plotted as vertical lines in Fig. 8.18. The points where the vertical lines cross the calibration curves are the estimated losses.

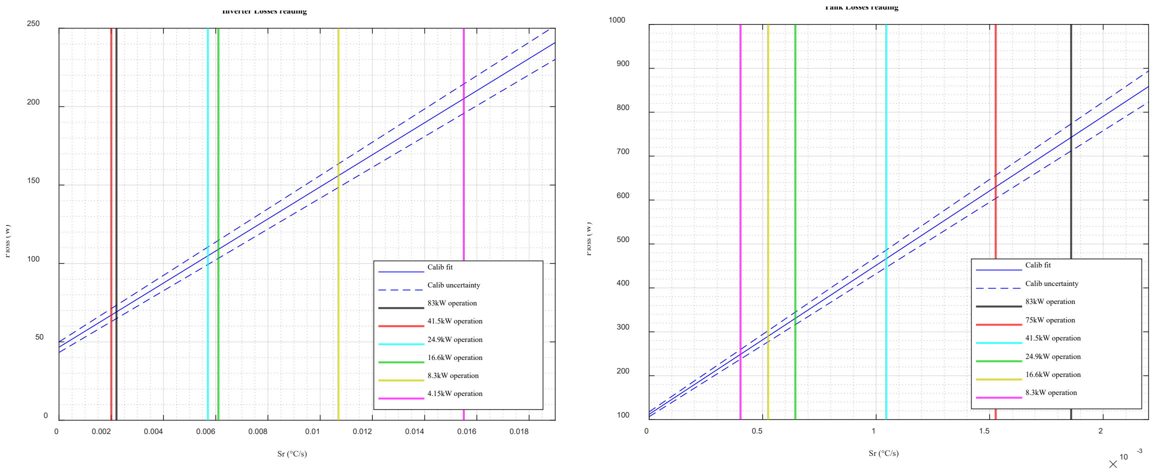


Fig. 8.18. Left) reading of power losses values from measured inverter slew rate during converter operation, right) reading of power losses values from measured tank wall slew rate

The point corresponding to the operation at 5% of the nominal power (4.15 kW) is missing for the tank as the temperature elevation is too small to use the calibration curve in Fig. 8.17.

8.3.2. Comparison with theoretical power losses

The measured inverter power losses are plotted in Fig. 8.19. The blue curve corresponds to the actual implementation (2 modules per leg, as the inverter was designed to operate up to 250 kW) and the red curve to a more ideal design for the 83 kW operation (1 power module per leg). It can be seen from the theoretical curves that the parallelisation of modules decreases the losses at high power levels (on-resistance is lower) and increases losses at low power levels (higher switching losses). Overall, power losses of 2-module inverter are higher than 1-module inverter.

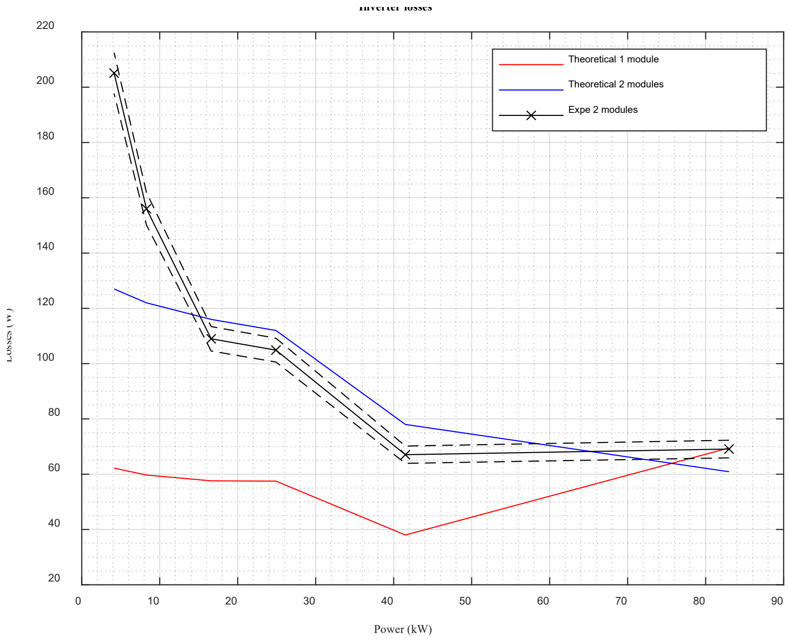


Fig. 8.19. Power losses curves of the inverter from theoretical design and experimental measurements (uncertainties in dashed lines)

It can be seen that the measured power losses are higher than the theoretical values at maximum and low power levels. For the maximum power point the difference is small, and can be explained by an increase in on-state resistance with the temperature (in the model, a junction temperature of 50°C was assumed). There is a much larger difference between measured and expected power dissipation at low power (<10 kW). Measuring the current in one of the modules in the low power range, an important peak can be observed at commutation time as shown in Fig. 8.20. Considering the values of the parasitic capacitances of the circuit, the charging of these cannot explain alone the amplitude of the observed current. The preferred hypothesis is that a spurious turn-on of the opposite MOSFET in the inverter leg creates a transient short circuit. It is shown in [98] that high dV/dt can lead to such a phenomenon at light loads.

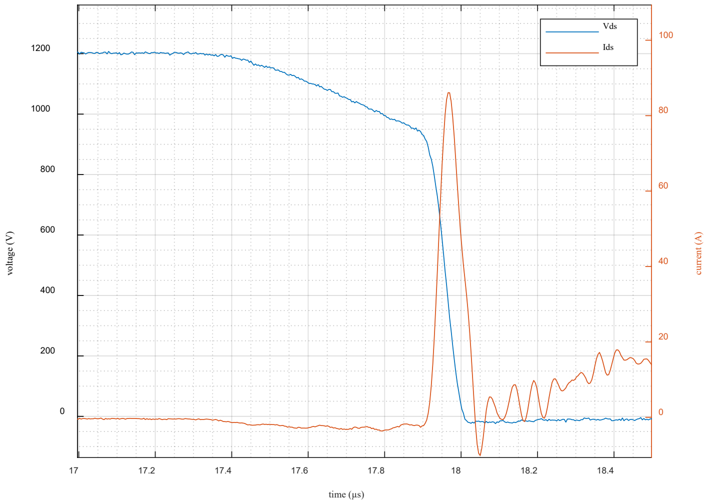


Fig. 8.20. Current spike at commutation of a lagging leg MOSFET during operation at 8.3 kW

The measured power losses of the tank are plotted in Fig. 8.21, along with theoretical calculations from the design phase. A good fit is observed between the measured curve and the theoretical curve at 25°C. Thus, as the 5% power point is missing from the measurements, the blue curve value of this power point will be used in further efficiency calculations.

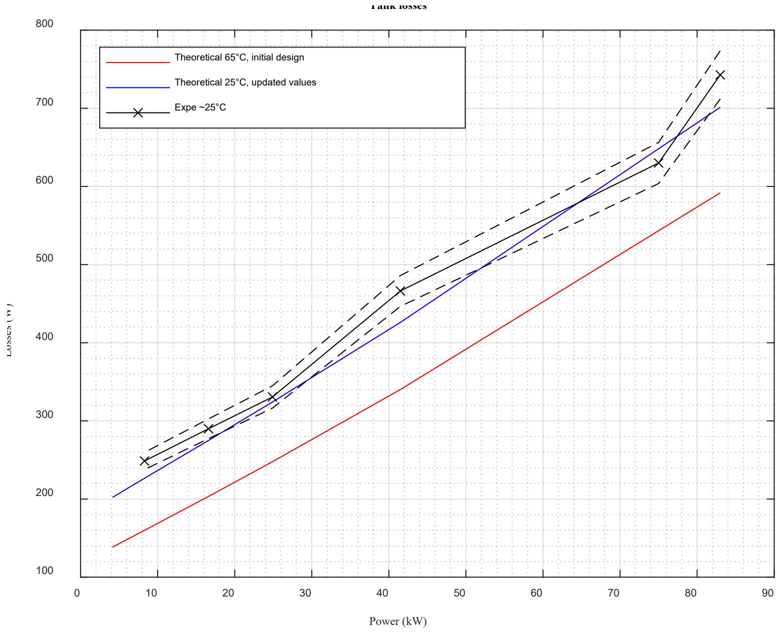


Fig. 8.21. Power losses curves of the tank from theoretical design and experimental measurements (uncertainties in dashed lines)

The difference between the theoretical red and blue curves are associated with the MFT only. The red curve corresponds to the losses estimated with the target design of the MFT and the blue curve corresponds to the MFT which was actually manufactured. Indeed, several changes have been made at manufacturing, after the design. The winding length is found to be larger because of practical manufacturing reasons, resulting in a measured 20% higher DC resistance compared to the original design. Because of availability issues, the magnetic core material used in transformer implementation (Ferroxcube 3C90) also differs from the original design (TDK N87). The used material has higher core losses, with higher dependence on the core temperature. This last point is particularly important as the experimental measurements are performed with the transient calorimetric method starting at ambient temperature. Thus, the blue curve is represented for 25°C operation, instead of the anticipated steady-state temperature of 65°C, in order to be compared to the measured values. This short-coming of the transient calorimetric method could be avoided by pre-heating the oil tank with the resistors used to perform calibration. This is not applied here because of time constraints.

8.3.3. DC-DC converter efficiency

The efficiency curve of the complete converter is shown in Fig. 8.22. The red curve corresponds to the theroretical efficiency of the design adapted to 83 kW, with one module per leg and the MFT initial design. The blue curve corresponds to the theoretical efficiency updated with the characteristics of the actually implemented components.

From the measured efficiencies of the inverter and tank, the European efficiency of the complete converter can be found according to Eq. (2.3) to be equal to 98.27 (±0.1) %. This value is quite lower than the objective value of 99%. However, it must be noted that the value of 98.27% is very close to the European efficiency of the AC solution {string inverter + 50 Hz transformer} shown in Fig. 2.23 to be 98.3%.

The reasons for the lower-than-expected efficiency have been given above, with the main ones being the use of two power modules per postion (design of the inverter for 250 kW) and the MFT higher DC resistance and different core material.

Except for the very low power levels (spurious turn-on phenomenon), the measured efficiencies fit very well with the theoretical curve taking into account the actually implemented components. This fact gives confidence that changing the transformer and reducing the number of power modules would bring the European efficiency of the PSFB up to that of the red curve calculated at 98.85%, much closer to the 99% target.

Table 8.2. Comparison of European efficiencies of the 83 kW prototype

Objective	Initial design	As built	Measured
99.00%	98.85%	98.38%	98.27(±0.1)%

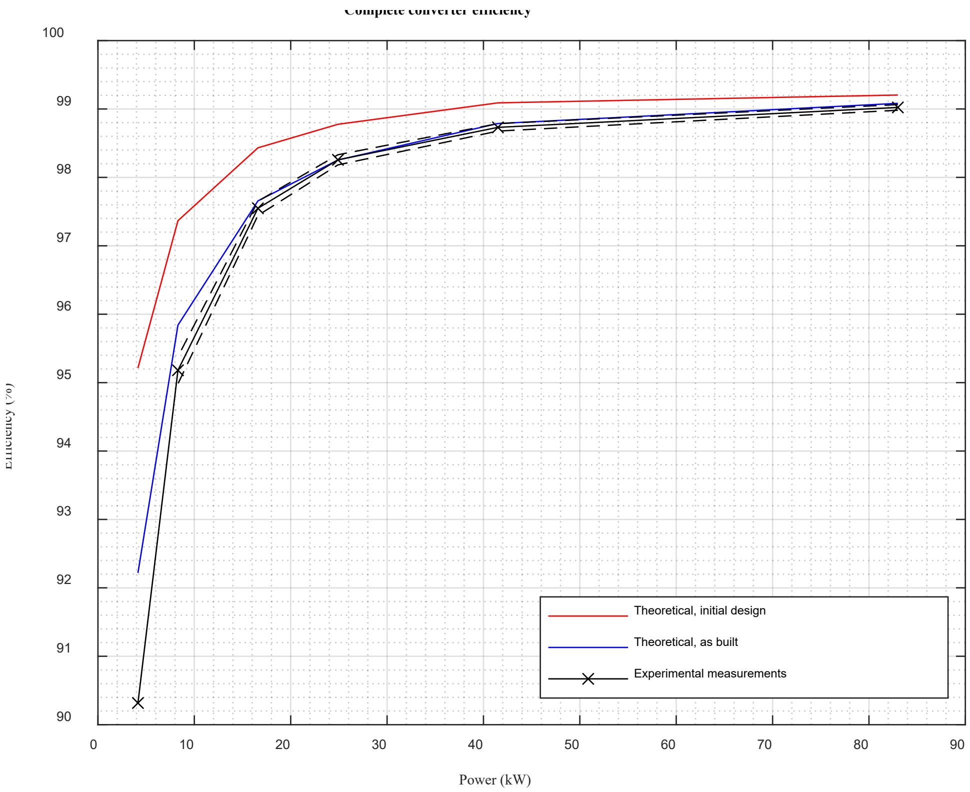


Fig. 8.22. Efficiency curve of the complete converter

8.4. Chapter conclusion

A review of the different power losses measurement methods has shown that, for high efficiency unidirectional MV converters, a calorimetric method is necessary to achieve satisfactory accuracy. An in-air, transient calorimetric method is selected from the litterature, driven by its applicability to large, passively cooled converters. This method is applied on its original target, the inverter, to verify its perfomances. The use of two slew rate ranges is proposed to improve the fitting at low power fractions. The extension of the applicability of this method to the measurement of the power losses of the oil tank is demonstrated. In particular, it has been shown that the position and thermal characteristics of the calibration resistor has a low impact on the accuracy of the measurement. Using this method, the power losses of the complete converter are measured, showing a good match with theoretical calculations. The European efficiency of the converter is measured at 98.27 %. The important difference with the objective of 99% is mainly explained by manufacturing problems in the MFT and the use of an oversized inverter. However, the good fit with the theoretical values gives confidence that the European efficiency of the initial design (98.85%) can be reached by solving these pratical issues.

9. Conclusions and perspectives

Driven by the need to decarbonise energy production, the integration of renewable energy sources into the power grid has become an important topic in modern electrical engineering. The use of medium voltage direct current (MVDC) collection network is currently researched as it is expected to bring higher energy efficiency, among other benefits. A missing piece to connect low voltage DC-native renewable energy sources to an MVDC network is the high ratio step-up DC-DC converter.

It is known that, for HVDC power transmission, a break-even distance exists, from which the gains in cable power losses (compared to HVAC) overcompensate the losses of the additional converters connecting to the AC grid. It has been shown in this dissertation that a break-even distance can also be found for MVDC in the 10s of kilometers. It has been observed that, in the case of a PV collection network, the spatial distribution of sources and their power variability, moves the break-even distance farther than in the point-to-point transmission case. In particular, the mean break-even distance for a ±10 kV 17.3 MW collection network, with individual converters rated at 250 kW, was found at 19 km. This distance is valid for to a DC-DC converter having the same European efficiency as the AC interface {string inverter + 50 Hz transformer} (98.25%). The European efficiency objective of 99% was set for the step-up DC-DC converter to have a break-even distance for PV collection network at 5 km.

A review of the state of the art in PV converters has been presented and used to define the general structure of a DC-DC converter interconnecting PV strings to an MVDC network. The multiple MPPT converters are kept from the traditional string inverter structure and the {string inverter output stage + 50 Hz transformer} is replaced by the step-up DC-DC converter. A literature review of DC-DC topologies and realisations of LV to MV converter prototypes has shown two main families of converters: the resonant topologies and the topologies based on classical Buck or Boost. The general consensus was found to be that resonant topologies are better suited to applications where a constant voltage ratio and no control is needed, while the classical topologies are more adapted when some quantity (input or output voltage, power) must be regulated. The LLC and PSFB have been selected for further investigations.

The comparison of the LLC and PSFB considering the case study specifications has shown a slight preference for the PSFB. Indeed, the comparison of losses alone could not discriminate between the two as the LLC has a better peak power efficiency but the PSFB efficiency stays more constant at low powers, resulting in similar European efficiencies. The decisive factor has been identified as the behaviour of the output filters during MVDC faults. The *LC* output filter of the PSFB proves highly beneficial to the protection of the rectifier circuit in the case of a short circuit at the output (fault on the MVDC line). On the contrary, because of its capacitive output, a short circuit at the output of the LLC results in an uncontrolled current surge which can destroy the rectifier. A converter prototype operating at 800 V output voltage was used to verify experimentally the fault behaviour of both output filter types. An additional inductor could be added to the output of the LLC (on the network side), but the PSFB already includes an inductor, which fulfils two purposes: the limitation of the current ripple in the circuit and the protection in case of MVDC faults.

Typically, PSFB converters are used to supply power to loads, which requires controlling their output voltage. In this thesis, the PSFB must control its input voltage, as the output voltage is dictated by the MVDC network. A controlled LVDC voltage is required as multiple MPPTs are connected to the input of the PSFB, and they themselves control their respective input voltages. Such PSFB control scheme has not been published so far, and was thus proposed in this dissertation. The developed average model takes into account the leakage inductance of the transformer which, depending on its values, can have a damping effect on the resonance between DC input capacitor and output inductor. Tuning equations for a PI controller have been proposed, considering the cases of damping and no damping. The proposed control has been verified experimentally with a (350-600 V, 30 kW) converter and a real field-measured load profile. The fact that the PSFB has a safe behaviour during MVDC faults has permitted to develop a control scheme for DC Fault-Ride-Through based only on low voltage side control actions. This control scheme involves the MPPT converters to keep a constant LVDC bus voltage and enables the PSFB to continue outputting a close-to-nominal current during faults, facilitating the MVDC network protection scheme.

Regarding the practical implementation of the PSFB, it has been proposed to immerse the complete medium voltage circuit in oil to limit the insulations distance between the different components (MFT, rectifier, inductors and capacitors). As the integration of magnetics in oil is well known, the focus was put on the medium voltage, medium frequency rectifier. The design of the rectifier has been studied through the electrical, thermal, dielectric and chemical aspects. Because of the high efficiency requirements of the considered application, the rectifier was implemented by series connections of discrete 1.7 kV SiC Schottky diodes. Snubbers must be associated with each diode to ensure voltage balancing and to limit overvoltages at turn-off.. A model used to simulate this overvoltage has been improved from the literature to take into account the effect of the input bridge switching speed, showing a significant reduction of its amplitude for low switching speeds (in the few V/ns range) but not for typical SiC switching speeds (in the 10s V/ns). The accuracy of the model has been demonstrated experimentally with the design of a 4 kV rectifier and its operation in a relevant converter environment. The cooling of such an oil-immersed PCB rectifier by simple patterned copper patches has been proposed. A prototype has been built and operated in a dedicated test bench enabling the validation of the thermal design at nominal oil temperature. The design was found to be safe but pessimistic as the maximum junction temperature at nominal current was found to be 91 °C (below the design target of 100°C and far below the maximum operating temperature of the diodes at 150°C). Dielectric characterisations of PCB samples has been performed in order to define design guidelines for MV PCB rectifiers. The results of breakdown and Partial Discharge Inception Voltage tests on 3 mm gap PCB samples have been observed to follow a Weibull distribution for both treated and non treated oil. The effect of the oil treatement was found to be apparent on the PDIV but not the breakdown voltage. A design guideline of 3.3 kV/mm is defined from the 1% probability of Partial Discharge Inception in non treated oil. Finally, the chemical compatibility of the rectifier's components and PCB with the oil has been checked by monitoring their change in weight over time at different temperatures. The conclusion of the preference for Suface Mounted Device components for the snubbers has been reached.

A 1.2-to-6.6 kV, 83 kW PSFB prototype has been designed and implemented. The converter is composed of two elements: an inverter and an oil-insulated circuit (MFT, rectifier, inductors, capacitors). The choice of the components values has been formalised as an optimisation problem aiming at maximising the European efficiency. The converter operation at full power and voltage has been performed in a back-to-back configuration with an active load. The Zero Voltage Switching and Discontinous Current Mode operation power limits have been validated experimentally by observing the drain-source voltage of a MOSFET of the lagging leg. In particular, the importance of the dead-time tuning for the proper achievement of ZVS has been showcased.

The efficiency of the studied converter being one of its most important features, it must be measured accurately. As the electrical methods have been found either not accurate enough or inapplicable in our case, this thesis has focused on a calorimetric method. Because of the size and important thermal time constant of the prototype, a transient calorimetric method in ambient air was selected from the literature. This method is not commonly used, so it was first applied to the input inverter, a case relatively close to that in an already published article. The tests showed a good accuracy when compared with electrical measurements. The extension of the applicability of this method to the measurement of the tank losses has then been experimentaly demonstrated. Small scale experiments have shown that the use of tank wall temperature measurements gives more accurate results compared to oil temperature measurements (9% maximum relative error compared to 40%).

The efficiency measurements performed on the final implementation of the converter prototype have given an European efficiency of 98.27% (±0.1%). The differences compared to the original target of 99% are explained mainly by two phenomena. The first one is the manufacture of the transformer using a core material different to the planned one. The second one is the use of an oversized inverter adding large switching losses. However, the good fit with the theoretical values gives confidence that the European efficiency of 98.85% of the initial design can be reached by solving these pratical issues.

The main achievements of this dissertation include the following:

- The calculation of break-even distances for MVDC, with clear underlying hypotheses, for point-to-point transmission and radial networks, taking into account the spatial distribution of loads/sources, and the varying power of the case study (PV plant) [14].
- The comparison of the typical DC-DC topologies output filter responses to MVDC faults, showing that the PSFB output inductor performs both the function of current ripple limitation and protection of the rectifier during short-circuits. Fault behaviour has been studied in simulations [31] and verified experimentally with a converter prototype operating at 800 V [69].
- The formalisation of the choice of the electrical parameters of the PSFB circuit as an optimisation problem to maximise the European efficiency of the inverter.
- The propostion of a PSFB control model and tuning method for the input voltage regulation. The demonstration that this simple control meets the application requirements has been done experimentally with real field-measured load profile on a 350 V to 600 V 30 kW converter protopype [69].
- The demonstration that the PSFB topology is suited to DC Fault-Ride-Through operation. The proposition of a control algorithm involving MPPT converters and PSFB [70].
- The improvement of a simple circuit model for the simulation of the PSFB rectifier voltage oscillations, taking into account the effects of the transformer primary-to-secondary winding capacitance and of the limited switching speed of the input bridge, and adapting it to full bridge rectifiers. The accuracy of the estimation of the peak voltage has been experimentally shown using a designed 4 kV rectifier in a representative converter structure [67].
- The implementation of an oil-immersed MV rectifier, based on series-connection of SiC Schottky diodes on a PCB, showing that the cooling of diodes can be realised by simple patterned copper patches. The thermal design has been verified experimentally using a dedicated test set-up allowing for operation at the nominal oil temperature [78].
- The proposition of guidelines for the implementation of an oil-immersed PCB MV rectifier concerning the dielectric design and the choice of components with regards to the chemical compatibility with the oil. Guidelines have been defined from dedicated experiments on samples [78].

- The implementation of a 1.2 kV-to-6.6 kV converter and demonstration of its operation at 83 kW, proving the electrical, dielectric and thermal design soundness on a representative scale prototype. The converter has reached the European efficiency of 98.27%.
- The extension of a transient calorimetric method in ambient air to the measurement of power losses of an oil-immersed circuit from a simple tank wall temperature increase, with experimental verifications on both a small test set-up and the full scale converter prototype.

The work realised during the doctoral studies has resulted in several publications:

- 1 journal article published in IEEE Access [69]
- 4 conference papers [14], [67], [70], [78]
- 1 co-authored conference paper directly linked with this study [31].

The author has identified some perspectives including:

- Removing the front-end MPPTs and integrating the MPPT function in the step-up converter. The consequences on the design of the DC-DC converter and efficiency of the overall system must be evaluated.
- Improving the input voltage control of the PSFB so its dynamic perfromances are similar in CCM and DCM. Tuning two controllers on differents operating point and working on the smooth transition between the two is a possible approach. Using a more advanced control is an other.
- Improving the FRT control by removing the need for communication between the PSFB and MPPT converters.
- Physically integrating the PSFB inverter with the oil tank, possibly exchanging heat with the oil to form a fully-integrated PSFB unit equivalent to a 50Hz transformer.
- Improving the thermal model used for oil-immersed PCB rectifier cooling design in order not to oversize the copper patch surface and achieve more compact design. This would be useful for higher voltage rated rectifier needing more series connected diodes.
- Refining the dielectric design rules for MV rectifier taking into account the effect of unipolar square waveforms.
- Defining the voltage limit at which the PSFB MV implementation challenges become too important. This involves a conjoint work on MFT and snubber dimensioning. The author suspects that the combination of required leakage inductance, insulation distances and MFT parasitic capacitances would, as the output voltage increases, lead to either impractical snubber design (too lossy) or the addition of diodes only to widthstand overvoltages. The use of more advanced snubber than simple RC should be investigated.

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Appendices

Appendix 1. LLC design details

LLC

In a first approach, a frequency control is considered as to regulate the input voltage. The switching frequency is varied which means f_n varies and thus the gain varies. It is first considered that the range of f_n should not extend past [0.9 1.1] as to keep the design frequency of the transformer at medium frequency. The resonant frequency of the tank is selected to be f_{res}=22 kHz. An hypothesis for the inductance ratio to be L_n=5 is taken initialy. From this, the value of Q corresponding to the maximum gain would be calculated from Eq. (4.6).

$$Q(P_{max}) = \frac{\sqrt{\frac{1}{{m_{max}}^2} - \left(\frac{1}{L_n} + 1 - \frac{1}{L_n\, {f_{n,min}}^2}\right)^2}}{\left(\frac{1}{f_{n,min}} - f_{n,min}\right)} \tag{A.1}$$

It is actually not possible to compute for the given case, as the expression under the square root is negative for the chosen values of frequency range and inductance ratio. Either the inductance ratio has to be changed, which will have an impact on the magnetizing current and efficiency, or the minimum switching frequency, which will have an impact on the size of the transformer.

The scenario where the minimum frequency ratio is changed is explored first; the inductances ratio is kept at Ln=5. In order to keep the expression under the square root in (A1.1), the minimum frequency ratio becomes:

$$\frac{1}{{m_{max}}^2} - \left(\frac{1}{L_n} + 1 - \frac{1}{L_n\, {f_{n,min}}^2}\right)^2 \geq 0 \tag{A.2}$$

$$f_{n,min} \leq \sqrt{\frac{1}{1 + L_n - \frac{L_n}{m_{max}}}} = 0.829 \tag{A.3}$$

The corresponding value of the quality factor calculated from (A.1) is $Q(P_{max})$=0.22. The resonant elements are then calculated from Q, f_{res} and L_n, using, in order, equations (4.11) (4.1) and (4.8):

$$C_r = \frac{1}{2\pi\, f_{res} \frac{8}{\pi^2\, n^2} \frac{{V_{o,max}}^2}{P_{max}}\, Q(P_{max})} = 5.82\ \mu F \tag{A.4}$$

$$L_r = \frac{1}{(2\pi\, f_{res})^2\, C_r} = 8.99\ \mu H \tag{A.5}$$

$$L_m = L_n\, L_r = 44.9\ \mu H \tag{A.6}$$

The gain of the converter with respect to frequency ratio can be plotted for its complete operating area from equation (4.6).

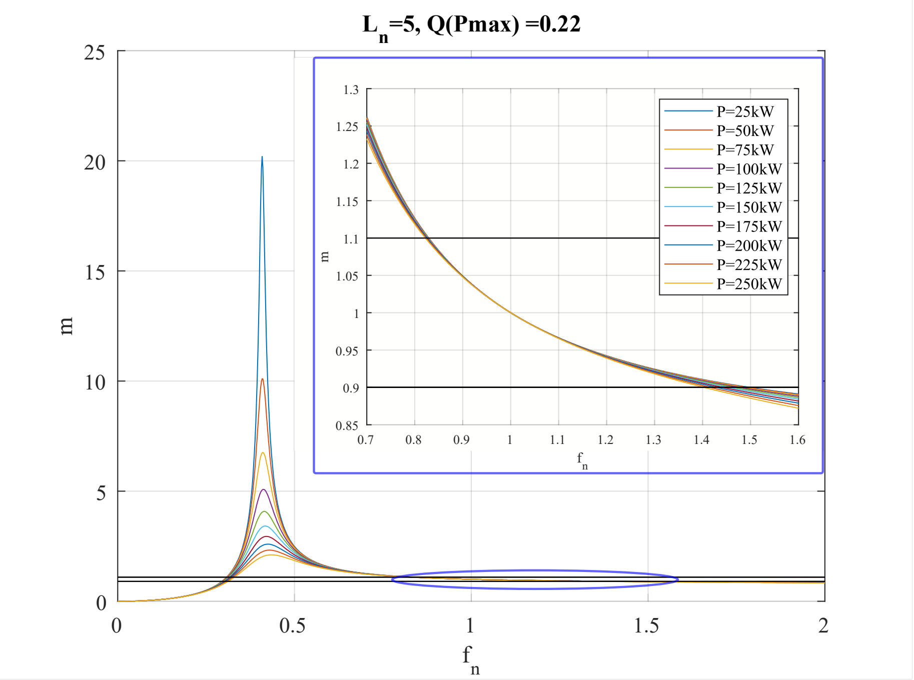

Fig. A.1. Gain of the designed LLC with respect to normalised frequency with a zoom on the frequency region of interest. Black lines represent the gain conditions.

It can be seen from Fig. A.1 that the frequency ratio to reach maximum gain at full power is indeed 0.82. It can also be seen that the maximum frequency ratio to attain minimum gain is quite high, at 1.5. It is observed that with this design, the gain is not heavily dependent on the load.

The other way of achiving the positive value in Eq. (A.2) (for example if the frequency ration must be contained within some specific boundaries), is to change the inductance ratio:

$$L_n \leq \frac{{f_{n,min}}^2 - 1}{{f_{n,min}}^2 \left(\frac{1}{m_{max}} - 1\right)} = 2.58 \tag{A.7}$$

If the frequency range specification given earlier is considered, it is possible to identify a suitable inductance ratio by tuning Q and L_n and looking at the gain graphs. In order to beneficiate from the resonant peak for the gain, it is necessary to decrease the inductance ratio and increase the quality factor.

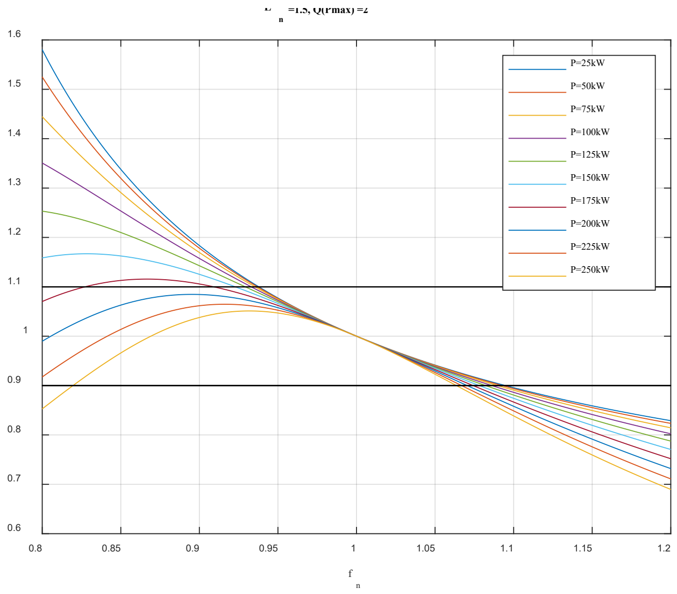

Fig. A.2. LLC gain with low Ln=1.5 and high Q(Pmax)=2

This design has a high quality factor at P_{max} and a low inductance ratio. Here the gain is much more load-dependent and it is necessary to take into consideration a particularity of the case study specifications: indeed, for gains higher than 1.05 the maximum power doesn't have to be transmitted. From Fig. 4.5, it can be seen that this allow the design to satisfy the specfications. At maximum power the 1.05 gain is attained and the 1.1 gain is attained for powers inferior to 200 kW. All of this within the frequency ratio range of [0.9 1.1].

One way to deal with the problem of higher frequency than wanted to achieve low gain is to use phase-shift modulation. The phase-shift modulation consists in introducing a delay between the two legs gate signals. This phase shift δ in radians is defined in the range [0 π] with respect to the switching period (0 means not shifted and π means shifted by half a period). With this definition it is possible to write the new gain of the LLC with phase-shift modulation m_{ps} by considering the Fourier transform of the inverter voltage V_p and secondary voltage of the transformer V_s as proposed in [99].

$$\frac{V_s}{V_p} = \frac{\frac{4\,V_o}{\pi}}{\frac{4\,V_i}{\pi}\,sin\frac{\delta}{2}} \tag{A.8}$$

$$m_{ps} = \frac{V_o}{n\,V_i} = \frac{sin\frac{\delta}{2}}{n\sqrt{(\frac{1}{L_n}+1-\frac{1}{L_n\,{f_n}^2})^2 + Q^2\,(\frac{1}{f_n}-f_n)^2}} \tag{A.9}$$

By working at resonant frequency the gain becomes independent of the load since f_n=1 and the Q related term is thus zero. Also the inductance ratio related term equates to 1 for f_n=1.

$$m_{ps} = sin\frac{\delta}{2} = sin\frac{\pi\,D}{2} \tag{A.10}$$

The results of this control method on the characteristics of the converter at all considered output voltage are shown in Fig. A.3.

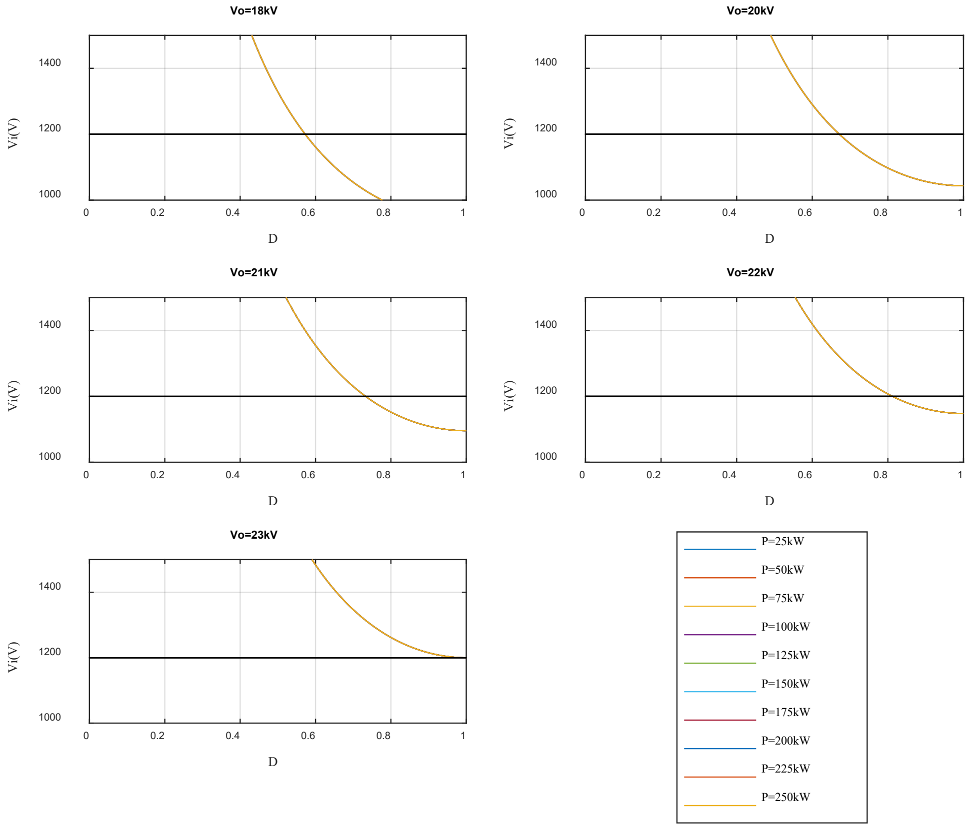

Fig. A.3. LLC control space at resonant frequency with phase-shift only

However, this non dependency to load only occurs when the switching frequency is exactly equal to the resonant frequency and this can be hard to achieve with parasitics having an impact on the resonant frequency.

SRC

The equations describing the SRC are the same as for the LLC. Indeed, the only difference is that in the SRC the magnetizing inductance is considered much bigger than the leakage inductance, which is equivalent to having a very large L_n from the LLC point of view. Thus the resonant peak is pushed very far to the low frequency ratios as can be seen in Fig. A.4 where a low quality factor is first kept.

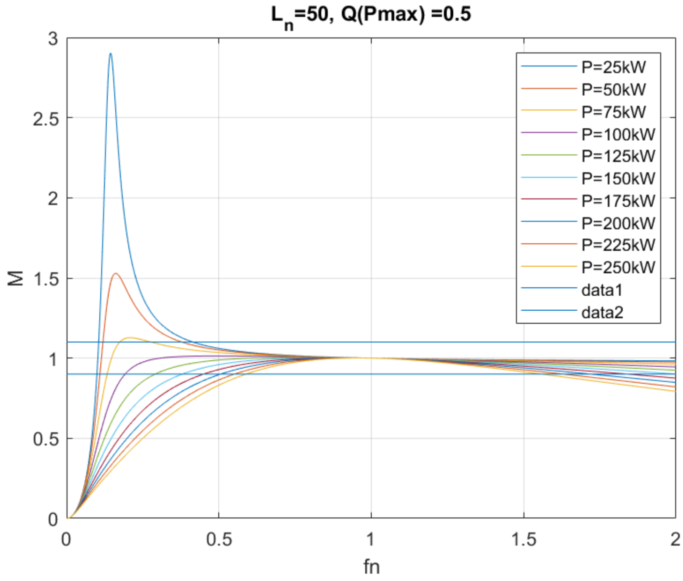

Fig. A.4. LLC with very high Ln => SRC

With such a design, the boost area is now impossible to access without extreme frequency variations. Therefor, the transformer ratio is directly set to make the maximum voltage gain.

The quality factor has to be much higher in order to achieve the desired gains within a reasonable frequency range. In Fig. A.5 it can be seen that even with $Q(P_{max})$=3 when staying above resonant frequency (to keep inductive behaviour), it is not possible to have sufficient gain only from frequency modulation at low powers. However as we saw in the LLC study, increasing Q means that the resonant capacitor will see a higher voltage ripple.

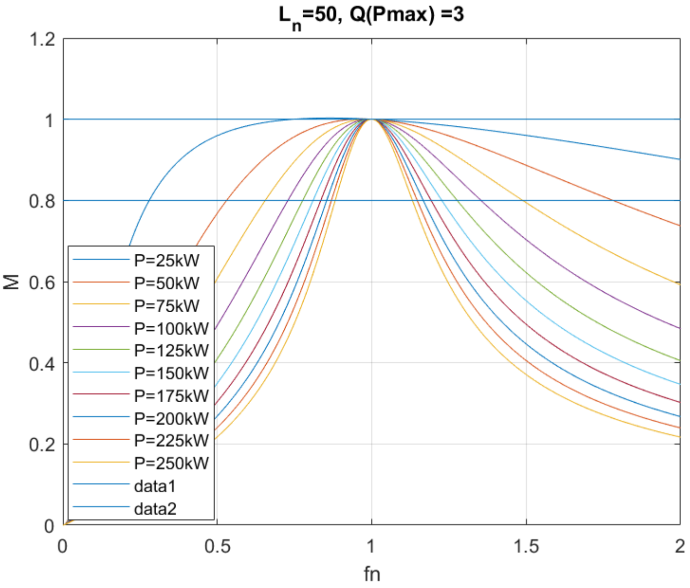

Fig. A.5. SRC gains with increased Q factor

Appendix 2. Efficiency evaluation of the candidate topologies

LLC

LLC losses at Vo = 19kV

% Pmax	100%	50%	30%	20%	10%	5%
MOSFET cond (W)	1375	420	213	142	90	67
MOSFET switch (W)	471	388	316	274	224	192
Diode MOSFET (W)	15,5	12	9	7,59	6	5
Diode RECT (W)	1279	487	254	156	70	33
Total (W)	3140,5	1307	792	579,59	390	297
Eff (/250kW)	98,74%	98,95%	98,94%	98,84%	98,44%	97,62%

LLC losses at Vo= 20 kV

% Pmax	100%	50%	30%	20%	10%	5%
MOSFET cond (W)	1197	346	191	144	114	107
MOSFET switch (W)	305	290	288	286	280	278
Diode MOSFET (W)	7,3	7,9	8,1	8,2	9	7,9
Diode RECT (W)	1205	450	231	140	80	66,9
Total (W)	2714,3	1093,9	718,1	578,2	483	459,8
Eff (/250kW)	98,91%	99,12%	99,04%	98,84%	98,07%	96,32%

LLC losses at Vo= 21 kV

% Pmax	100%	50%	30%	20%	10%	5%
MOSFET cond (W)	1155	347	204	159	117	95
MOSFET switch (W)	290	297	302	302	290	278
Diode MOSFET (W)	7	8	8,6	8,8	8,4	8
Diode RECT (W)	1112	421	221	137	63	29,5
Total (W)	2564	1073	735,6	606,8	478,4	410,5
Eff (/250kW)	98,97%	99,14%	99,02%	98,79%	98,09%	96,72%

The high value of magnetizing current, resulting from the design of the LLC that enables to have control over the entire voltage/ power range, shows in the low powers efficiencies. The turn-off current minimum value being the magnetising current value which is not load dependent. Thus, even at light load the turn-off losses are important and bring the efficiency down.

Phase-shifted full bridge

PSFB losses at Vo= 19 kV

% Pmax	100%	50%	30%	20%	10%	5%
MOSFET cond (W)	1606	403	183	99	34	12,3
MOSFET switch (W)	1218	468	293	226	137	93,5
Diode MOSFET (W)	55	16,7	9,5	6	3,34	1,9
Diode RECT (W)	1213	479	261	164	76	35,8
Total (W)	4092	1366,7	746,5	495	250,34	143,5
Eff (/250kW)	98,36%	98,91%	99,00%	99,01%	99,00%	98,85%

PSFB losses at Vo= 20 kV

% Pmax	100%	50%	30%	20%	10%	5%
MOSFET cond (W)	1434	358	164	90	32	11,8
MOSFET switch (W)	1165	436	269	204	127	87,5
Diode MOSFET (W)	19,9	4,72	1,6	0,43	0	0
Diode RECT (W)	1124	443	240	152	70,8	33,45
Total (W)	3742,9	1241,72	674,6	446,43	229,8	132,75
Eff (/250kW)	98,50%	99,01%	99,10%	99,11%	99,08%	98,94%

PSFB losses at Vo = 21 kV

% Pmax	100%	50%	30%	20%	10%	5%
MOSFET cond (W)	1226	303	136	75	27	10
MOSFET switch (W)	1111	421	250	180	117	82
Diode MOSFET (W)	33,7	11,8	6	4,4	2,5	1,5
Diode RECT (W)	1032	408	220	140	65	30,7
Total (W)	3402,7	1143,8	612	399,4	211,5	124,2
Eff (/250kW)	98,64%	99,08%	99,18%	99,20%	99,15%	99,01%

Appendix 3. Test set-ups

Test bench for control demonstration and fault tests

To demonstrate the PSFB topology and control in a PV MVDC collection network, a reduced-scale system is set up. The test bench is composed of two DC-DC converters, a DAB and a PSFB in a back-to-back configuration, with a DC power supply compensating for the losses of both converters. The test bench is controlled and monitored by a Speedgoat real-time target and programmed through Matlab Simulink Real-Time using rapid control prototyping (RCP).

In this setup, the DAB acts as the MPPT by regulating its output power, while the DC power supply represents the MVDC network and sets the PSFB output voltage. The PSFB control regulates its input voltage, ensuring the power transfer from the DAB (MPPT) to the DC power supply (MVDC network).

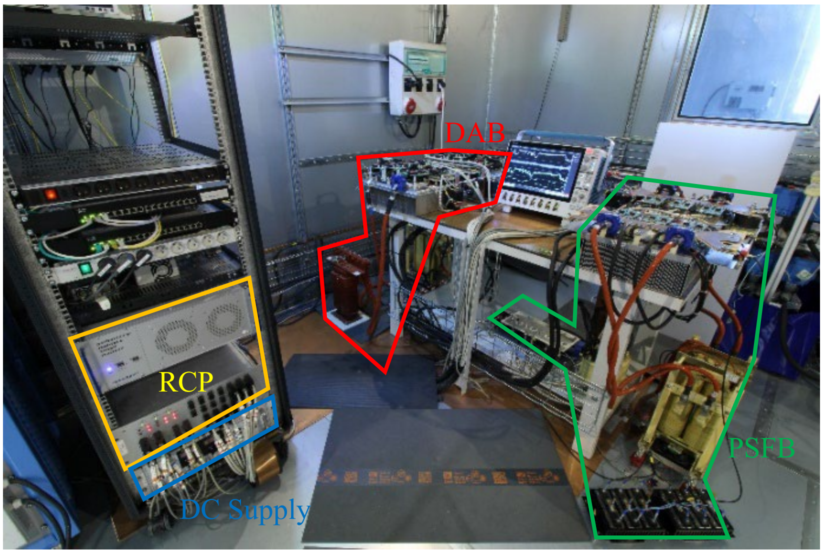

Fig. A.6. Test bench used for the validation of the control of the PSFB

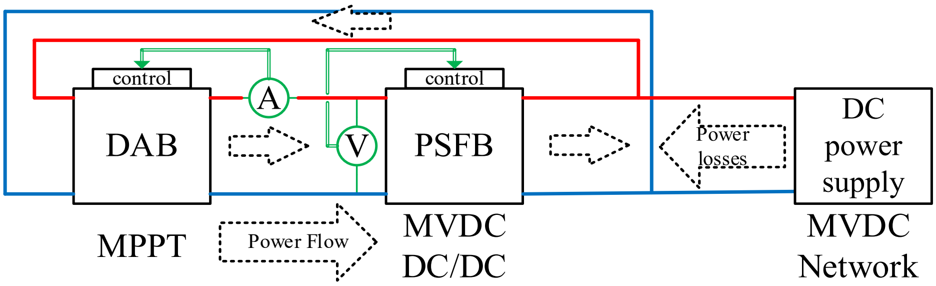

Fig. A.7. Circuit of the test bench, with equivalences with the case study

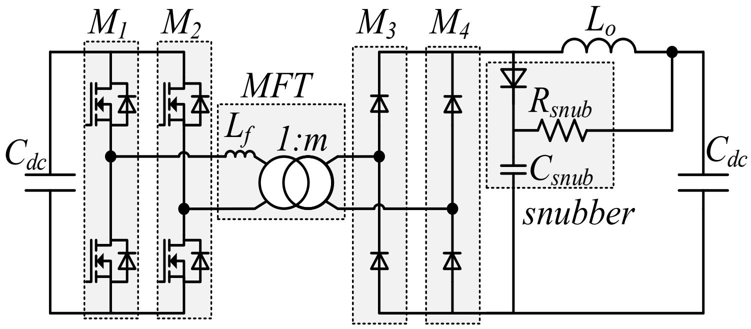

Fig. A.8. Schematic of the PSFB used in the control test bench

The DAB converter design was detailed in [100]. The figure above presents the implementation of the PSFB converter. Because of the low voltage output of this reduced-scale demonstration (600 V), there is no need for series-connected diodes in the rectifier bridge. As a result, the PSFB rectifier snubber is implemented using a single *RCD* snubber across the output [65] instead of multiple discrete snubbers, one for each diode. This implementation differs from the rectifier with series-connected diodes but the experimental verification of the topology and control remains valid. Components values of the test bench converter are summarised in the table below.

Parameters of the PSFB used for control validation

Parameter/Component	Value
Input voltage V_{in}	350 V
Output voltage V_o	600 V
Operating power P	30 kW
Switching frequency f	20 kHz
Input / Output capacitor C_{dc}	160 µF
MFT turns ratio m	2
MFT leakage inductance L_f	3 µH
Switches M_x	1.7 kV, 8.0 mΩ SiC Half Bridge Module CAS300M17BM2
Snubber capacitor C_{snub}	33 nF
Snubber resistor R_{snub}	33,3 Ω
Output inductor L_o	200 µH

The PSFB presented above is also operated alone for the fault tests described in section 4.3.2. The ouput short-circuit is performed using the mechanical switch shown in the figure below. The short-circuit resistance of 20 mΩ is realised by the assembly shown on the right.

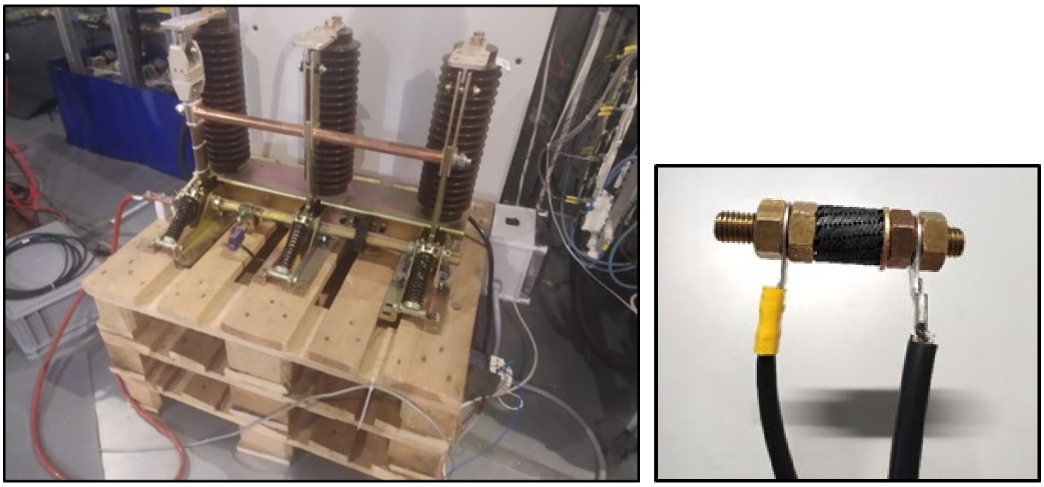

Fig. A.9. Left) Switch used for short-circuiting the output of the PSFB, right) 20 mΩ short-circuit resistance

Test bench for validation on 4 kV air-insulated rectifier

The PSFB topology is implemented to test the rectifier presented in section 6.1. The inverter is IGBT-based and operated at 1200 V, 20 kHz, with a full wave modulation. The solid insulated MFT is largely overrated (300 kW). Its parasitic elements shown in Table 6.2 were characterised following the procedure given in [101]. The control of the converter is realised in open loop using an ABB real-time target using rapid control prototyping solution.

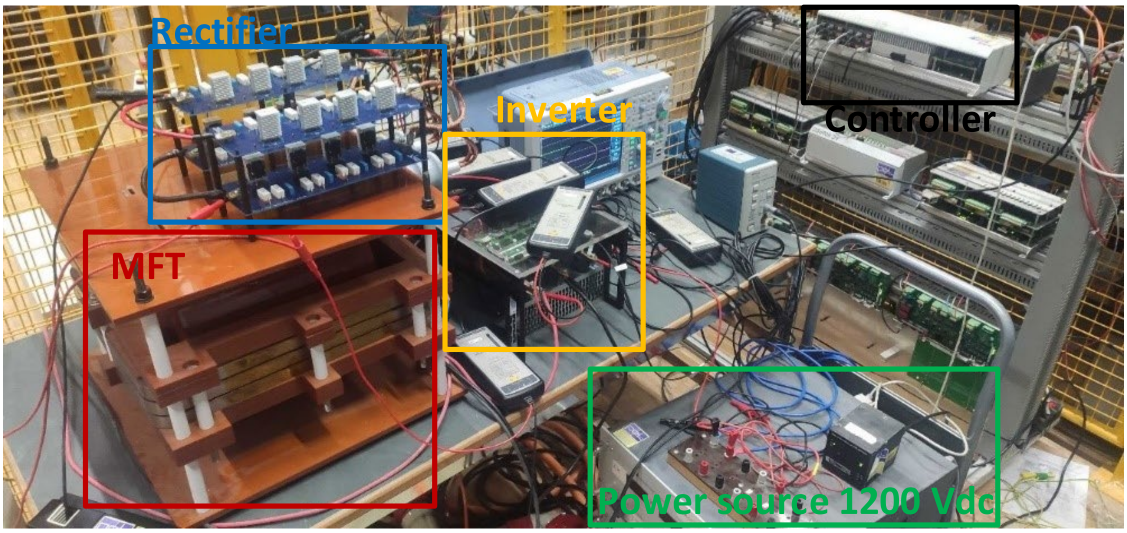

Fig. A.10. Test bench used for the validations on the 4 kV rectifier

MFT parameters of the rectifier tests set-up

Transformer ratio	Leakage inductance	Primary winding capacitance	Secondary winding capacitance	Primary-secondary winding capacitance
$m = 2.33$	$L_{lk} = 34$ µH	$C_p = 16$ pF	$C_s = 100$ pF	$C_{ps} = 30$ pF

6.6 kV 83 kW full converter prototype test bench

The 6.6 kV 83 kW PSFB prototype is operated in a back-to-back configuration, with a Buck converter performing the voltage step-down from 6.6 kV to 1.2 kV. The PSFB controls MV to 6.6 kV while the Buck converter controls the circulating power by current control. The Buck converter is implemented with series connected 3.3 kV SiC MOSFETs, as presented in the figure below. This converter is the results of the thesis work presented in [102]. The power supply is on the 1.2 kV low voltage side and supplies the power losses of both converters. The tests bench and converters are controlled by a Rapid Control Prototyping (RCP) solution from Speedgoat.

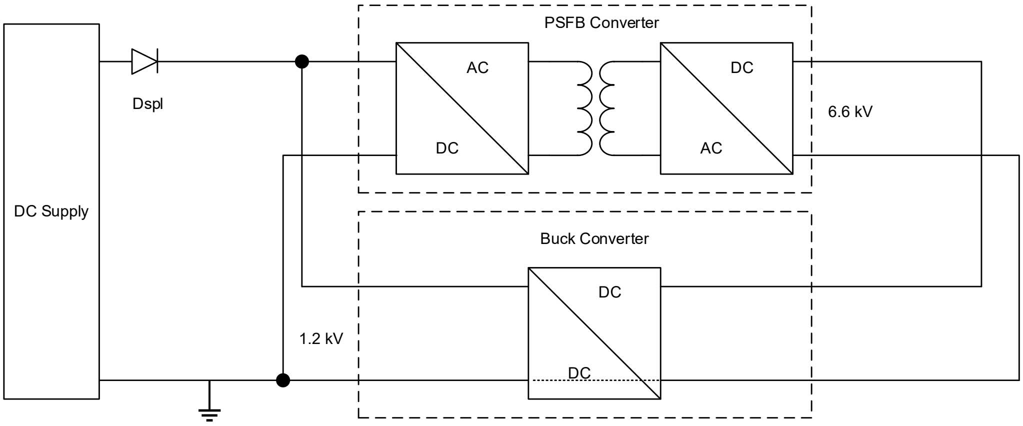

Fig. A.11. Back-to-back circuit used for the test of the 6.6 kV 83 kW PSFB prototype

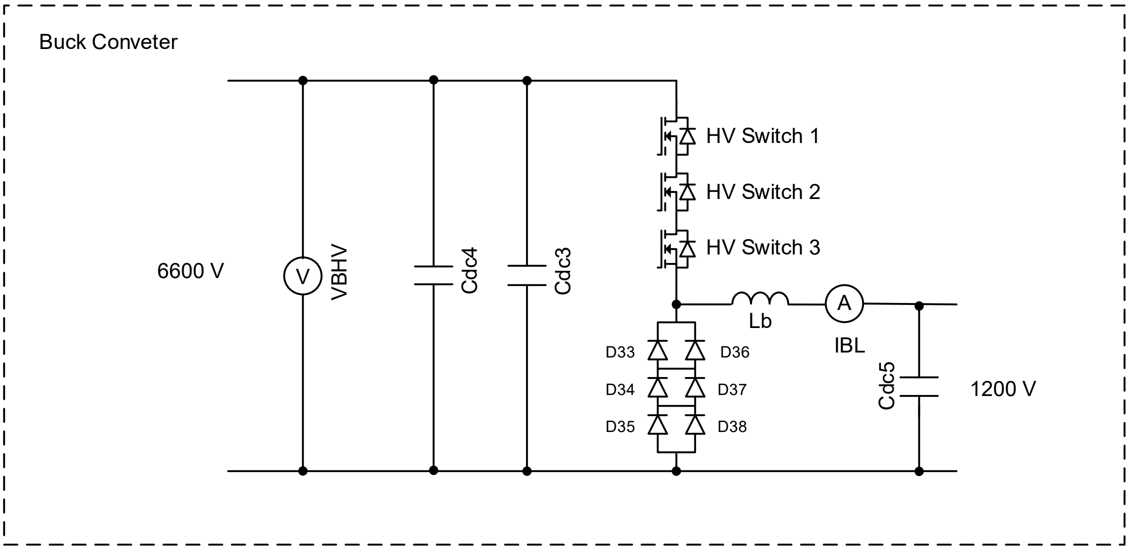

Fig. A.12. Buck converter used as an active load for the test of the 6.6 kV PSFB prototype

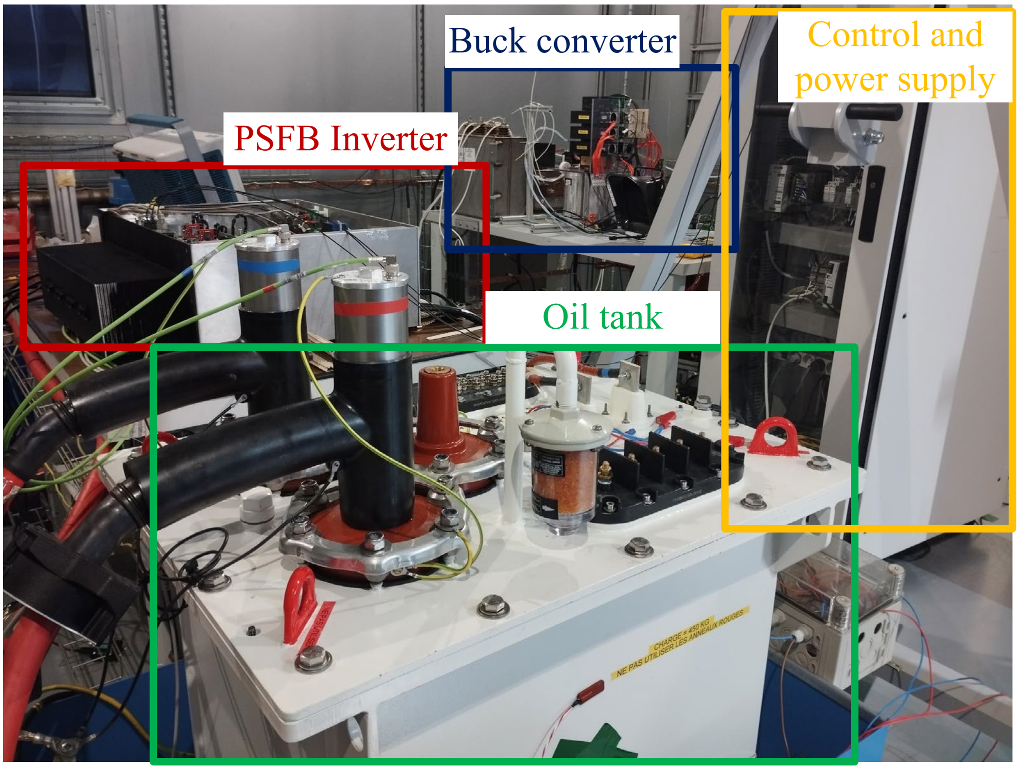

Fig. A.13. Test bench of the 6.6 kV 83 kW prototype

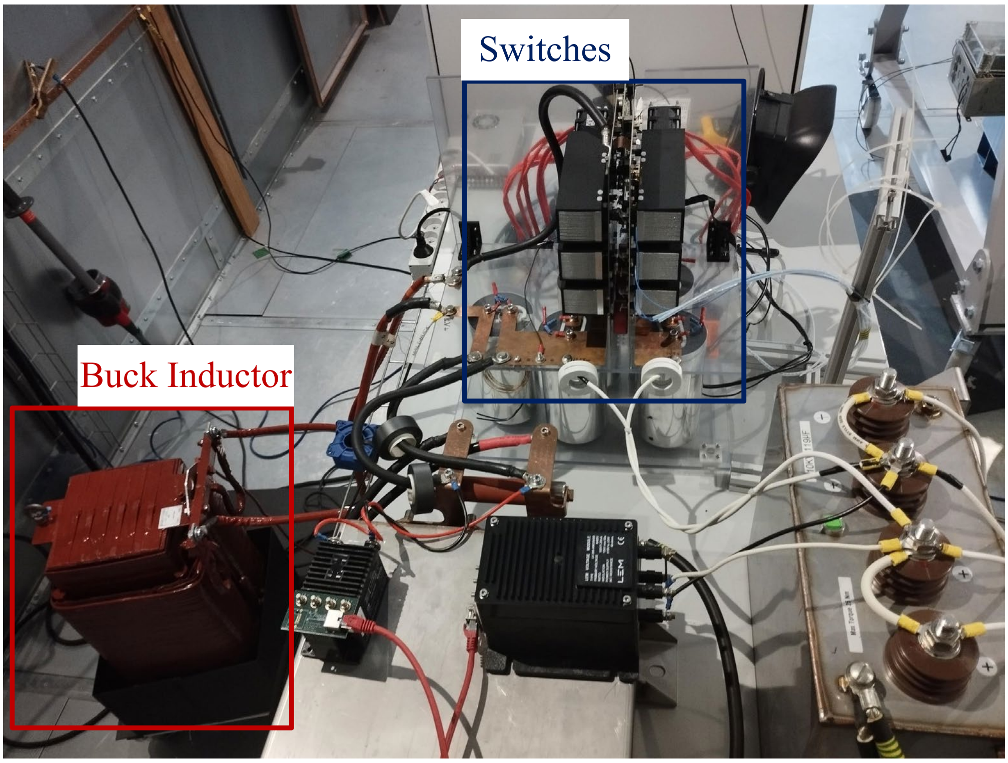

Fig. A.14. Implementation of the Buck converter

Appendix 4. MVDC fault cases simulation results

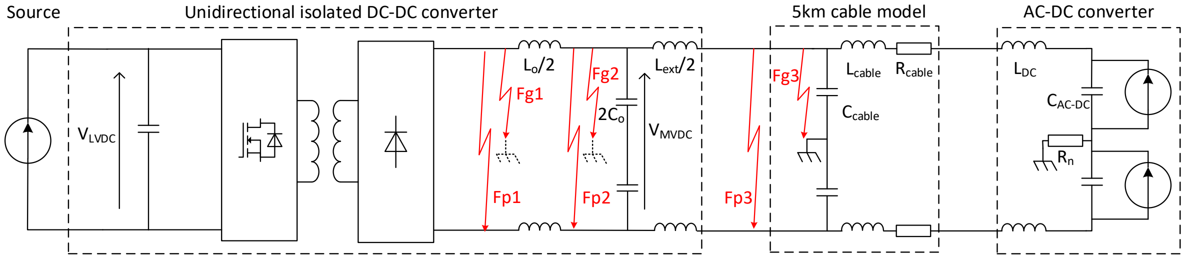

Fig. A.15. Definition of the different simulated fault cases

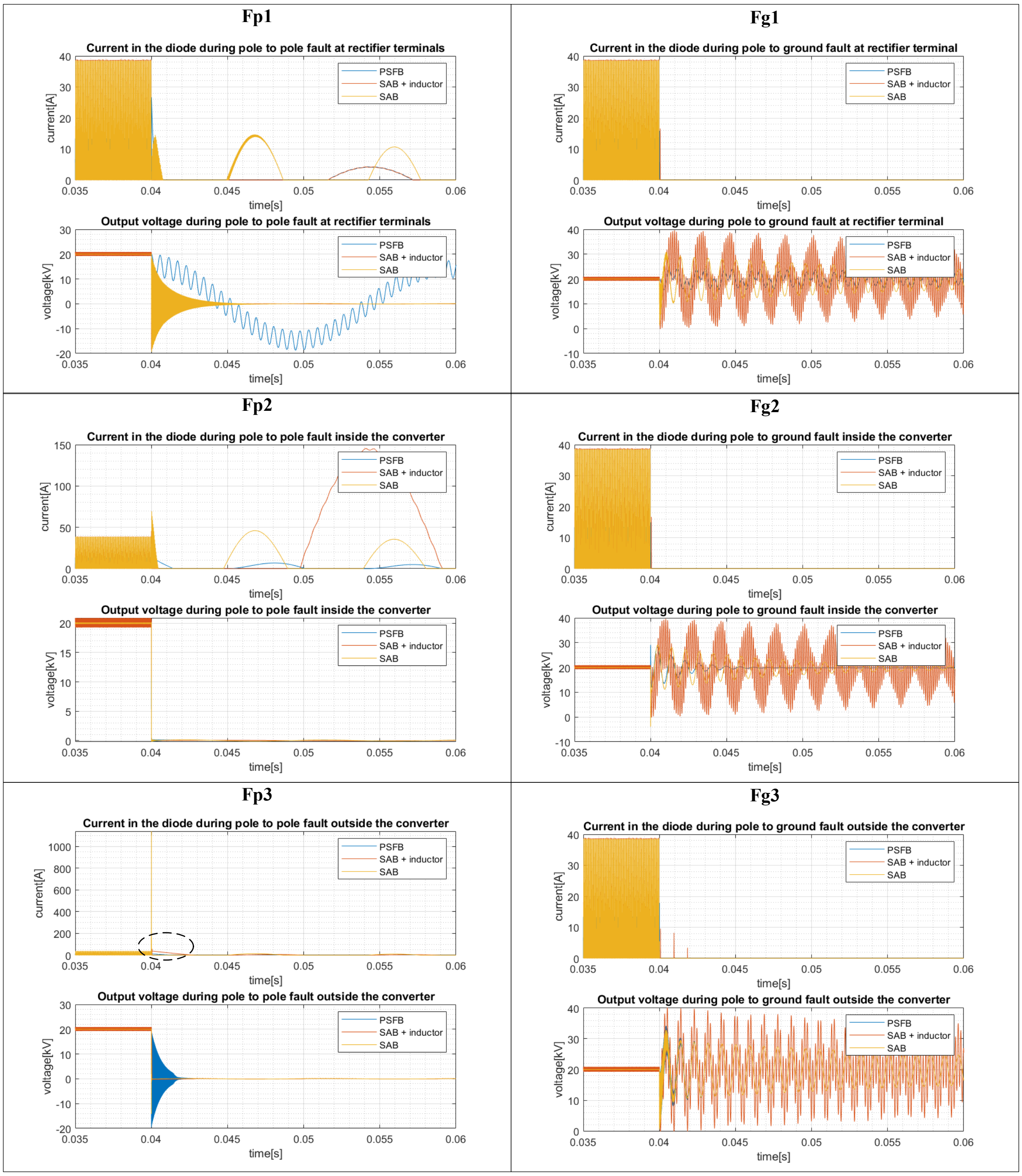

Fig. A.16. Simulation results of the different fault cases

It can be observed that the pole-to-pole faults in the output filter, in the diode rectifier or at the DC-DC converter terminals, do not result in high current in diodes. In the Fp1 case, it is seen that the output voltage polarity is reversed. However, this does not result in large diode current because the fault is localised between the filter capacitor (energy source) and the rectifier. The fault current simply does not flow through the diodes.

The pole-to-ground faults have no impact on the diode bridge but it can be observed that output voltage oscillations are triggered. The SAB-L presents the most severe oscillations. However, the output capacitor voltage never exhibits the voltage polarity reversal, so the diodes are never forward biased.

Appendix 5. Analytical formulas of PSFB currents for losses cost function

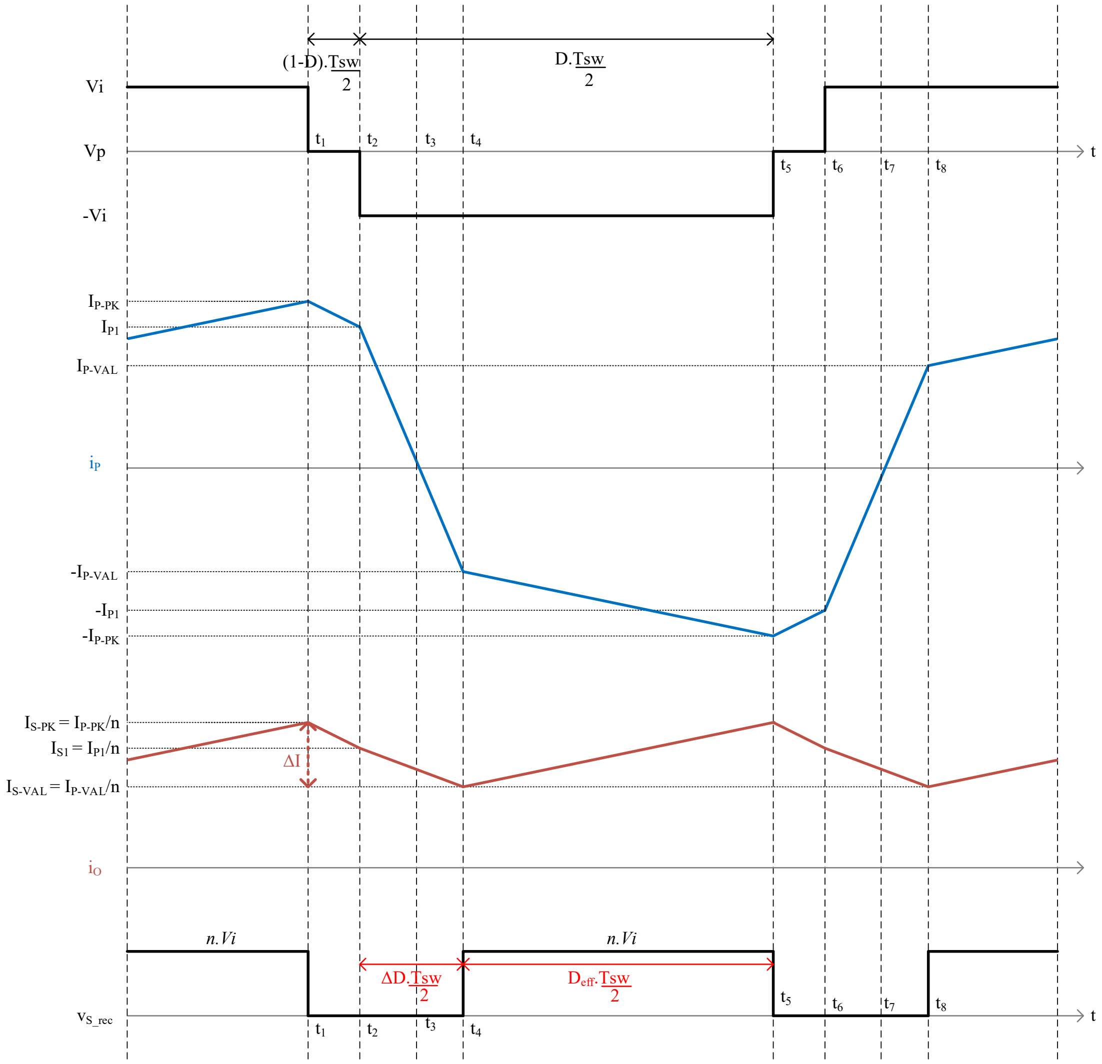

Fig. A.17. Simulation results of the different fault cases

$$I_{p\_pk} = I_m + m\,\left(\frac{V_o}{P} + \frac{\Delta I}{2}\right) \tag{A.11}$$

$$I_{p1} = I_m + m\,\left(\frac{V_o}{P} - \frac{\Delta I}{2}\right) \tag{A.12}$$

$$I_{p,val} = -I_m + m\,\left(\frac{V_o}{P} - \frac{\Delta I}{2}\right) \tag{A.13}$$

$$I_m = \frac{D\,V_i}{4\,f_{sw}\,L_m} \tag{A.14}$$

$$I_{RMS,lead} = \sqrt{(I_{p\_pk} - I_{p,val})^2\,\frac{D}{6} + I_{p,val}(I_{p\_pk} - I_{p,val})\,\frac{D}{2} + {I_{p,val}}^2\,\frac{D}{2}} \tag{A.15}$$

$$I_{RMS,lag} = \sqrt{(\,{I_{p\_pk}}^2 + I_{p\_pk}\,I_{p_{val}} + {I_{p_{val}}}^2)\,\frac{D}{6} + (\,{I_{p\_pk}}^2 + I_{p\_pk}\,I_{p1} + {I_{p1}}^2)\,\frac{D}{6}} \tag{A.16}$$

In CCM:

$$D = \frac{V_o}{m\,V_i} + \frac{4\,P\,m\,f_{sw}\,L_{lk}}{V_i\,V_o} \tag{A.17}$$

$$\frac{\Delta I}{2} = \frac{(m\,V_i - V_o)D}{4\,f_{sw}\,(L_o + \ m^2 L_{lk})} \tag{A.18}$$

In DCM:

$$D = \sqrt{\frac{4\,P\,f_{sw}\,(L_o + \ m^2 L_{lk})}{m\,V_i\,(m\,V_i - V_o)}} \tag{A.19}$$

$$\frac{\Delta I}{2} = \frac{V_o\,\left(1 - \frac{V_o}{m\,V_i}\right)}{4\,f_{sw}\,(L_o + \ m^2 L_{lk})} \tag{A.20}$$

Appendix 6. Elements inside of the tank

MFT

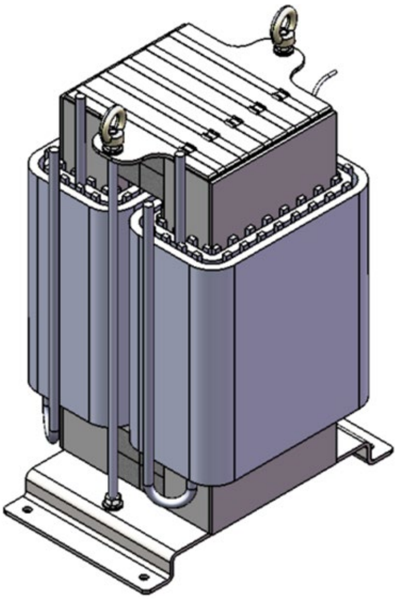

Fig. A.18. MFT used in the prototype

MFT design parameters

Property	Design value	Comments
Volume	37 dm^3	24 L without mechanical fixture
Height	450 mm	420 mm without mechanical fixture
Width	254 mm	
Depth	320 mm	250 mm without mechanical holders
Weight	65 kg	48 kg without chassis
Losses at nominal power	218 W	
Core Losses	34 W	
LV Winding Losses	48 W	
HV Winding Losses	135 W	
Dielectric Losses	2 W	
Efficiency at nominal power	99.73%	Nominal power = 83 kW
EU Efficiency	99.74%	Specification: >99.6%
Maximal temperature	66 °C	Specification: <100 °C
Leakage inductance	7.1 µH	Specification: Between 6 µH and 9 µH
Magnetizing inductance	1.90 mH	Specification: 1.9 mH ±5%
Primary capacitance	71 pF	Specification: 85 pF (indicative, low impact)
Secondary capacitance	40 pF	Specification: 33 pF (indicative)
Capacitance between windings	1200 pF	Specification: 278 pF (indicative)

Rectifier board

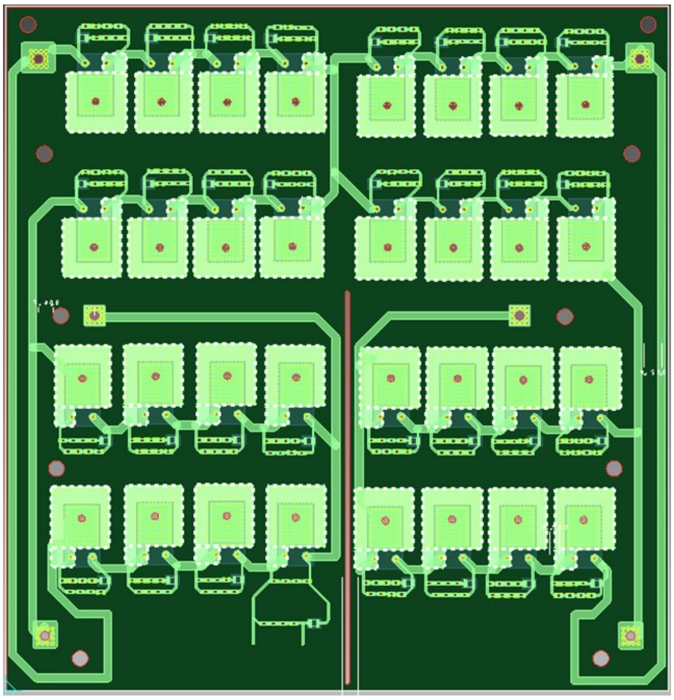

Fig. A.19. 6.6 kV rectifier used in the prototype

Rectifier design parameters

Property	Design value
Height	335 mm
Width	350 mm
Depth	1.6 mm
Weight	<1 kg
Losses at nominal power	317 W

Inductor

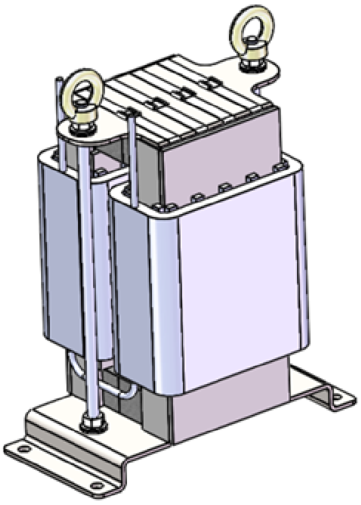

Fig. A.20. Inductor (1 of 2) used in the prototype

Inductor design parameters

Property	Design value	Comments
Volume	9 dm^3	6,3 L without mechanical fixture
Height	272 mm	240 mm without mechanical fixture
Width	145 mm	
Depth	230 mm	180 mm without mechanical holders
Weight	12 kg	
Losses at nominal power	25 W	Target value
Core Losses	8 W	
Conductor losses	18 W	
Inductance value	2.67 mH	

Output capacitors

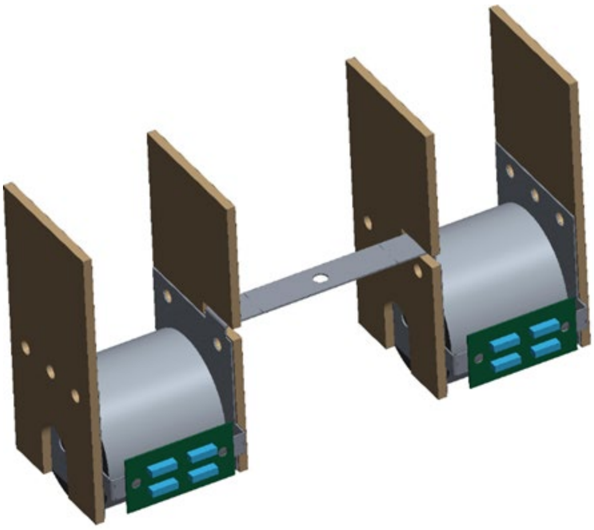

Fig. A.21. Capacitor assembly (series connection of 2) used in the prototype

Capacitor assembly design parameters

Property	Design value
Capacitor reference	ZES Silko PVDJP 21-4,5/1,5
Individual capacitor voltage rating	3.8 kV U_n / 4.5 kV U_{rp}
Total capacitance	750 nF
Discharge resistor (per capacitor)	13.5 MΩ

Appendix 7. Uncertainty formulas for calorimetric method

The calculation of uncertainties for the calibration curves is based on the work presented in [96]. For each calibration point, the uncertainties come from the tolerance of the instrumentation used to measure temperature and power. The expressions below give the respective tolerances of the PT100 temperature sensor, and the power analyser.

$$U(S_r) = 0{,}05\ °C/s$$

$$U(P_{dc}) = 0{,}01\ W$$

The calibration curve for power losses is an affine function with coefficients A and B such that:

$$P_{loss}(S_r) = A\ S_{r,measured} + B$$

Considering points $(S_{r,1};\ P_{dc,1})$ and $(S_{r,2};\ P_{dc,2})$, it is obtained the following relationships for the slope coefficient A, and the offset B:

$$\frac{\mathrm{U(A)}}{A} = \sqrt{\left(\frac{U(P_{dc,1})}{P_{dc,2} - P_{dc,1}}\right)^2 + \left(\frac{U(P_{dc,2})}{P_{dc,2} - P_{dc,1}}\right)^2 + \left(\frac{U\left(S_{r,1}\right)}{S_{r,2} - S_{r,1}}\right)^2 + \left(\frac{U\left(S_{r,2}\right)}{S_{r,2} - S_{r,1}}\right)^2}$$

$$\frac{\mathrm{U(B)}}{B} = \sqrt{\frac{\left(S_{r,2}\ U\left(P_{dc,1}\right)\right)^2 + \left(S_{r,1}\ U\left(P_{dc,2}\right)\right)^2}{(P_{dc,2}\ S_{r,1}\ - P_{dc,1}\ S_{r,2})^{\ 2}} + \frac{\left(P_{dc,2} - P_{dc,1}\right)^2\ (\left(S_{r,2}\ U\left(S_{r,1}\right)\right)^2 + \left(S_{r,1}\ U\left(S_{r,2}\right)\right)^2)}{(S_{r,2} - S_{r,1})^2\ (P_{dc,2}\ S_{r,1}\ - P_{dc,1}\ S_{r,2})^2}}$$

To assess the uncertainty in the estimated value of P_{loss}, the error propagation formula, where the a_i are the errors which affect P_{loss}:

$$U(P_{loss}) = \sqrt{\sum_{i=1}^{n}\left(\frac{\partial P_{loss}}{\partial a_i} \cdot U(a_i)\right)^2}$$

This gives the following uncertainty for the P_{loss} value estimated for a given efficiency measurement:

$$U\left(P_{loss,estimated}\right) = \sqrt{\left(A\ U(S_r)\right)^2 + (S_r\ U(A)^2 + \left(U(B)\right)^2}$$

FOLIO ADMINISTRATIF

THESE DE L'INSA LYON, MEMBRE DE L'UNIVERSITE DE LYON

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RESUME :
Les travaux réalisés au cours de cette thèse se concentrent sur le thème du convertisseur DC-DC pour les applications d'énergies renouvelables connectées à un réseau moyenne tension DC. La palette de sujets abordées s'étend de la définition des exigences auxquelles un tel convertisseur doit répondre jusqu'aux propositions d'implémentations matérielles le permettant, en passant par la sélection de la topologie la plus adaptée ainsi que par l'adaptation de son contrôle. Les différents points étudiés sont accompagnés de validations expérimentales utilisant différentes maquettes. Un prototype complet de convertisseur DC-DC 1.2 kV - 6.6 kV 83 kW est notamment construit et opéré à pleine puissance et tension.

MOTS-CLÉS : Convertisseur DC-DC, MVDC, Moyenne Tension, Photovoltaïque

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