Di-electric liquid cooling for future 20 kV power modules

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Contents

Part I

French summary

Refroidissement pour modules 20 kV

À mesure que la demande en puissance et en efficacité énergétique des systèmes d'électronique de puissance haute tension continuent d'augmenter, de nouvelles solutions de packaging et de refroidissement deviennent nécessaires pour garantir un fonctionnement fiable et sûr. Avec le récent développement de la technologie du carbure de silicium (SiC), des dispositifs de puissance à tension élevée (10 kV et plus) deviennent possibles. Ces systèmes génèrent une quantité significative de chaleur lors de leur fonctionnement, ce qui peut entraîner une dégradation des performances et la défaillances des composants. Par conséquent, la conception et la mise en œuvre de solutions de packaging et de refroidissement efficaces sont essentielles pour garantir la longévité et les performances optimales des systèmes électroniques haute tension.

Ce travail examine une solution de packaging pour les semi-conducteurs haute tension (20 kV), permettant une réduction spectaculaire de la taille et de la complexité des modules électroniques de puissance.

Ce chapitre introductif commence par une motivation pour les modules haute tension, en mettant l'accent sur la transmission à courant continu haute tension (HVDC). Il met ensuite en évidence l'objectif de la thèse et les défis liés au développement de solutions efficaces d'encapsulation et de refroidissement pour les systèmes électroniques de haute tension.

Motivation

Aujourd'hui, les réseaux à courant alternatif (CA), qui fonctionnent à une fréquence de 50 Hz ou 60 Hz, dominent dans la transmission de l'énergie électrique. Cependant, les récents progrès dans le domaine des dispositifs semi-conducteurs permettent d'utiliser une transmission d'énergie électrique à courant continu (CC) plus efficace que le CA.

Généralement, une haute tension (HV) est nécessaire sur de longues distances pour réduire les pertes de puissance. La perte de puissance P_{loss} est principalement causée par l'effet Joule et est le produit de la résistance linéique ohmique (R) et du courant linéaire I au carré ($P_{loss} = R \cdot I^2$). Par conséquent, transférer la même puissance active

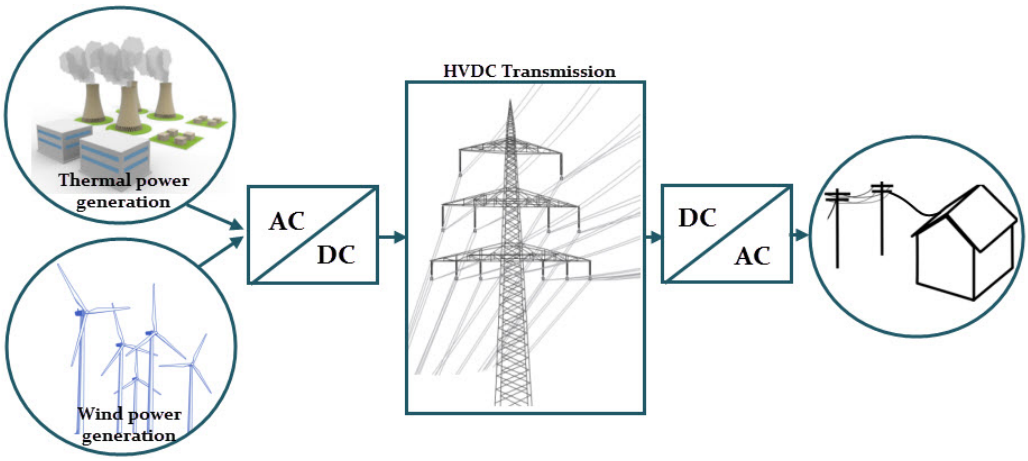


Figure 1: Système électrique à courant continu haute tension: station de convertisseur, section de transmission et station d'onduleur [1]

($P_{active} = I \cdot V$) en utilisant une tension V plus élevée et un courant I plus faible conduit à des pertes de puissance plus faibles.

Les principaux inconvénients des systèmes à courant alternatif haute tension sont la circulation de puissance réactive et l'effet de peau. Aucun de ces phénomènes n'apparaît avec le courant continu, ce qui limite les pertes dans la ligne. De plus, le CC présente une meilleure capacité de transmission de puissance en raison des distances d'isolation : les câbles CA sont conçus pour la tension de crête maximale, qui est plus grande que la tension efficace. Les valeurs RMS dictent en réalité le niveau de transfert de puissance. Par conséquent, un pylône CA peut être utilisé pour le CC à une tension 73 % plus élevée sans modifier sa structure. Cela se traduit par un triplement de la puissance transmise, car une ligne CC n'utilise que deux conducteurs isolés au lieu de trois dans une ligne CA.

Cependant, les lignes CC nécessitent des stations de conversion à leurs extrémités pour se connecter au réseau de transmission en CA. La Figure 1.1 illustre le système électrique à courant continu haute tension, depuis la station de génération jusqu'à l'utilisateur final.

Une étude de cas [2] compare le coût des systèmes de transmission CC et CA. Il est constaté (Figure 1.2) que pour les lignes de transmission les plus longues (plus de 700 kilomètres), la transmission CA est plus coûteuse que la transmission CC ayant la même capacité de transmission. Pour de telles lignes de transmission à grande distance, le coût moins élevé de la ligne en CC compense le coût des stations de conversion.

La Figure 1.3 montre une station de conversion de la société ABB [3]. Les stations de conversion actuelles sont basées sur des modules à un interrupteur ou à demi-pont IGBT (transistor bipolaire à grille isolée) de 3.3 kV. La station de conversion est une installation immense comprenant des centaines de modules IGBT. Augmenter les tensions nominales des modules de puissance de 3.3 kV à 20 kV entraînerait une réduction

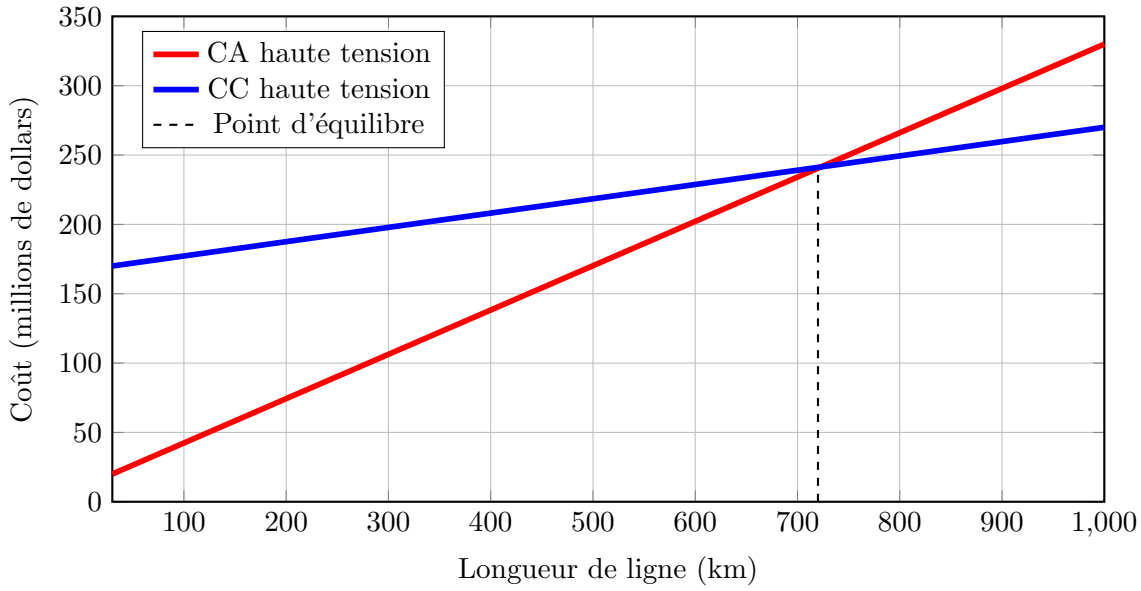


Figure 2: Coûts de lignes de transport d'électricité CA et CC en fonction de leur longueur.

spectaculaire du nombre de modules et donc de matériaux (notamment isolants), et de liquides de refroidissement seraient nécessaires pour gérer les modules. La station de conversion deviendrait beaucoup plus petite. Cependant, isoler de tels modules haute tension représente un défi. De plus, des densités de dissipation de puissance plus élevées sont générées. Par conséquent, une structure de refroidissement avancée est nécessaire pour maintenir le module en dessous des températures critiques. Ce travail vise à combiner le refroidissement et l'isolation en utilisant un liquide diélectrique à la fois comme fluide de refroidissement et comme isolant, offrant à la fois une gestion thermique améliorée et des performances d'isolation électrique simultanément.

Objectif de la thèse

Ce travail explore une solution de packaging pour l'électronique de puissance haute tension (20 kV). Cette solution présente moins de couches de matériaux et moins de complexité, tout en offrant de bonnes propriétés électriques et thermiques pour le module. L'objectif principal de ce travail est d'optimiser les performances de refroidissement.

Les objectifs de la thèse sont les suivants :

- Sélection de liquides diélectriques
- Optimisation de l'échangeur de chaleur intégré pour un fonctionnement avec refroidissement par liquide diélectrique, en visant une faible résistance thermique (R_{th}) et de faibles pertes hydrauliques.

Figure 3: An HVDC converter station [3]

- Optimisation de la conception pour uniformiser la résistance thermique (R_{th}) de chaque puce dans un module multi-puces.
- Validation et preuve de concept expérimentale.

L'utilisation de liquides diélectriques en combinaison avec des ailettes de refroidissement en céramique est une nouvelle idée qui n'a pas été étudiée dans la littérature. Ce travail compare différents concepts de packaging et leur impact sur les performances de refroidissement. Le nouveau packaging présente les meilleures performances, en plus de sa capacité à supporter des tensions plus élevées. Dans cette thèse, un design mêlant jet impactant et écoulement est proposé.

Véhicule d'essai mono-puce

L'accent principal est mis sur l'optimisation d'un refroidisseur à jet impactant à l'aide de simulations numériques de dynamique des fluides (CFD). Ce processus d'optimisation est suivi d'une analyse comparative entre la configuration optimisée et un concept de refroidissement par écoulement en canal. Afin d'assurer une isolation électriques atisfaisante, le choix est fait d'un fluide de refroidissement diélectrique, bien qu'une comparaison soit également faite avec un mélange d'eau et de glycol (non diélectrique). Le Novec 7500 est utilisé comme fluide de refroidissement en raison de sa permittivité élevée, soutenant efficacement les objectifs d'isolation.

L'influence des structures d'ailettes sur les performances de refroidissement est examinée. La méthodologie d'optimisation numérique est décrite. Un véhicule d'essai expérimental est ensuite réalisé, et ses performances sont mesurées.

La structure étudiée dans ce chapitre est un module à puce unique conçu pour gérer la dissipation de chaleur d'un MOSFET SiC de 10 kV mesurant $8.1 \times 8.1\,\mathrm{cm}^2$. Ce MOSFET spécifique génère une charge thermique de 125 W. Il est crucial de noter qu'après les simulations CFD, la disponibilité de cette configuration de MOSFET sur le marché commercial a cessé. Par conséquent, le MOSFET SiC est remplacé par un IGBT plus grand de $9.1 \times 9.1\,\mathrm{cm}^2$ pour les investigations expérimentales, assumant le rôle de source de chaleur.

Optimisation du refroidisseur avec des ailettes

Afin d'augmenter la surface de transfert de chaleur entre le fluide et le solide, des structures à ailettes ou à broches sont placées dans le canal. En plus d'offrir une plus grande surface de transfert de chaleur, les broches forment des constrictions qui forcent l'accélération du fluide dans le canal sous la puce. Les broches conduisent également à une formation de vortex (turbulence) plus importante dans le canal, ce qui favorise un meilleur transfert de chaleur. Différents paramètres de conception sont étudiés afin d'optimiser le refroidissement.

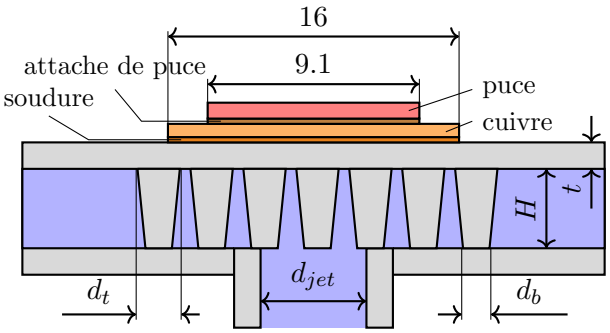
Géométrie

La géométrie du problème de transfert de chaleur conjugué (CHT) est présentée dans la figure 4. La figure montre la conception du dissipateur thermique à puce unique utilisant le concept de jet impactant, fabriqué en matériau AlN. Les ailettes du dissipateur thermique ont une forme conique avec des diamètres inférieur d_b et supérieur d_t. Les ailettes peuvent également être cylindriques lorsque les deux diamètres sont égaux ($d_b = d_t$). Le système de refroidissement comporte une entrée (le jet) et deux sorties situées sur les côtés gauche et droit. Le canal de refroidissement a une longueur de 50 mm, une largeur de W mm, et les ailettes ont une distance de s mm entre leurs axes. Le dissipateur thermique en AlN varie en épaisseur au sommet (t), tandis que toutes les autres parois ont une épaisseur constante de 2 mm. L'entrée a un diamètre de jet de d_{jet}. Le semi-conducteur de dimensions 8.1 mm$\times$ 8.1 mm est situé au milieu du dissipateur thermique directement sous le jet. Les variables, épaisseur supérieure du matériau AlN t, diamètre des ailettes d_{pins}, largeur du canal W et diamètre du jet D_{jet} permettent d'optimiser les performances thermiques du dissipateur thermique.

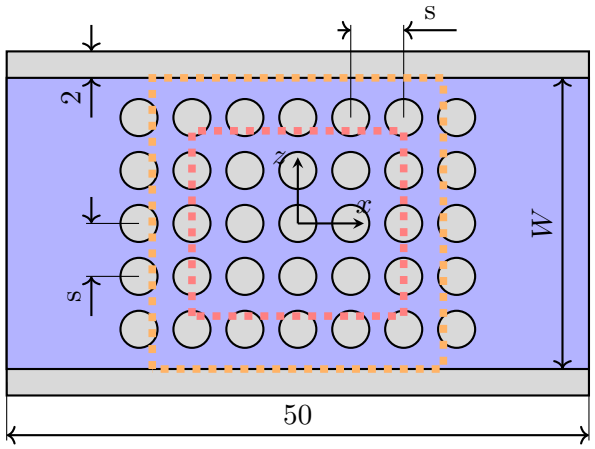
Résultats de CFD

Comme mentionné dans la section précédente, en plus du débit $\dot{V}$, cinq paramètres de conception (d_{pins}, H, d_{jet}, W et t) sont étudiés pour obtenir la conception optimale. Pour simplifier le processus d'optimisation, l'épaisseur supérieure d'AlN et la largeur du canal W restent initialement constantes, avec $W = 16$ mm et $t = 1.5$ mm. De plus, des ailettes cylindriques sont utilisées avec des diamètres fixes ($d_t = d_b = d_{pins}$). La Figure 5 montre les résultats des calculs numériques pour la résistance thermique en fonction de la puissance de pompage. Le graphique affiche un grand nombre de points, chacun représentant une configuration différente. La zone verte sur le graphique représente la cible souhaitée pour la conception, avec une puissance de pompage inférieure à 1 W et une résistance thermique inférieure à 0.48 K/W. Les points sur le graphique sont également différenciés par leur forme, avec cinq formes différentes représentant différents diamètres de broches allant de 1 mm à 3 mm. Le graphique montre que des débits plus élevés conduisent généralement à une résistance thermique plus faible, mais entraînent également une puissance de pompage plus élevée. La relation spécifique entre la résistance thermique et la capacité de pompage pour chaque paramètre de conception est indiquée par la distribution des points sur le graphique. Le grand nombre de points affichés permet une analyse complète de la relation entre ces paramètres, contribuant à identifier la conception optimale pour l'ensemble des exigences données. Les broches avec un diamètre de 2 mm présentent les meilleures performances de refroidissement.

En plus des résultats du refroidisseur avec broches, le graphique représente également



(a) Paramètre de CAO du concept de refroidissement par jet impactant



(b) Section transversale au milieu du canal sous la puce

Figure 4: Structure étudiée, montrant les paramètres de conception pour un refroidisseur avec des structures à broches

les résultats pour un refroidisseur sans structures internes dans le canal. Le refroidisseur avec des broches est plus efficace. La zone cible ne peut pas être atteinte pour un refroidisseur sans broches.

La Figure 5 montre qu'une meilleure performance de refroidissement est obtenue pour un plus grand diamètre de broches d_{pins}. Cependant, au-delà de 2 mm, la résistance thermique augmente, ce qui dégrade le refroidissement. La distance entre broches est maintenue à 1 mm, ce qui fait que la densité de broche n'évolue pas linéairement avec leur diamètre. Les petites broches ont une section réduite qui nuit à la conduction de la chaleur, et une surface d'échange avec le fluide réduite. En revanche, des broches très grandes bloquent le passage du fluide et augmentent ainsi la puissance de pompage. Une hauteur de canal plus élevée est préférée dans cette étude car elle offre une plus grande distance d'isolation entre le côté supérieur (où se trouve le dispositif SiC) et le côté inférieur du dissipateur thermique (où la masse de terre potentielle devrait être située). Le processus de fabrication des refroidisseurs en AlN limite le diamètre des broches à 2 mm pour une longueur de broche de $h = 6$ mm.

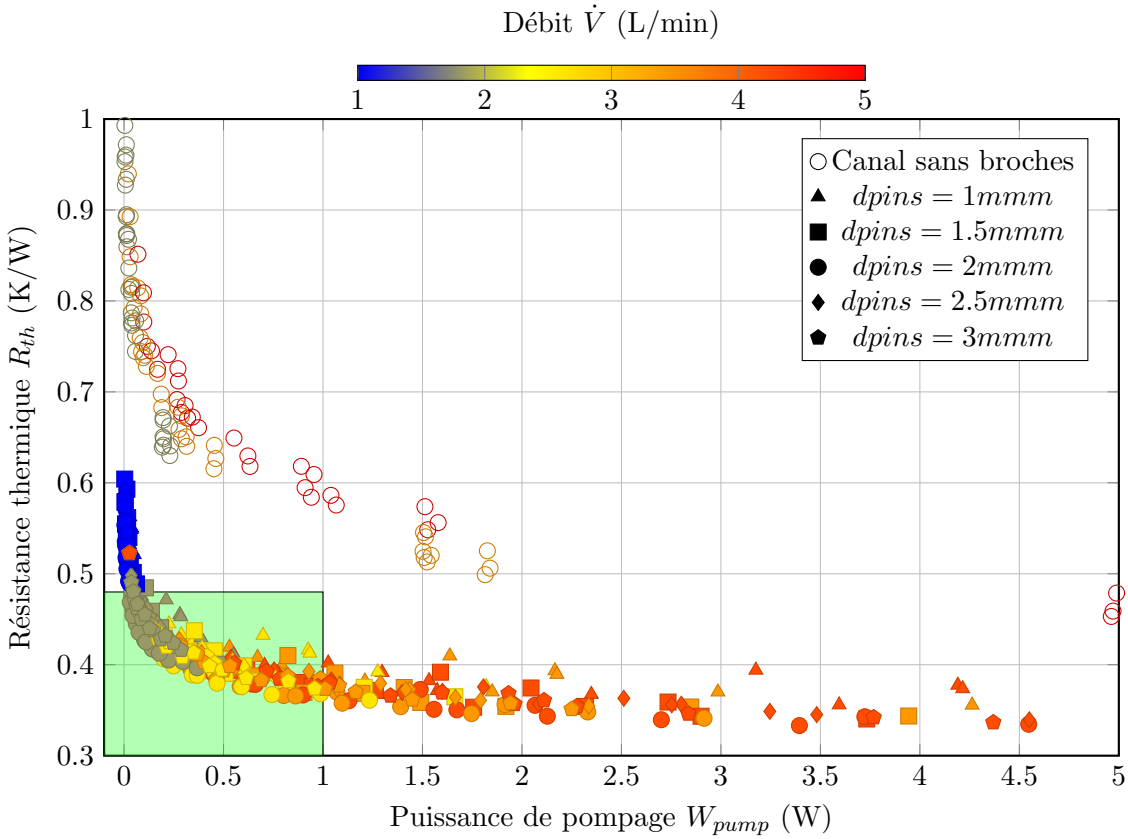
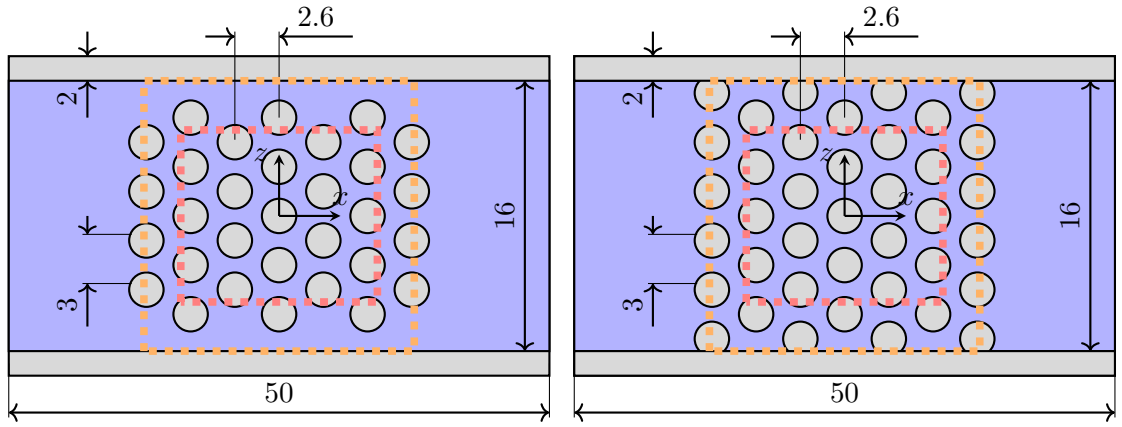


Figure 5: Résistance thermique en fonction de la puissance de pompage avec différents diamètres de broches d_{pins}; barre de couleur : débit $\dot{V}$

Comparaison entre différentes configurations de broches

Dans le refroidissement par écoulement en canal et par jet impactant, les configurations de broches jouent un rôle crucial dans la détermination des performances de refroidissement. Cette section se concentre sur la comparaison de deux distributions de broches différentes, (en ligne ou décalées) dans un canal. Les performances des configurations en ligne et décalées sont évaluées pour le refroidissement par écoulement en canal et par jet impactant. Les courbes de front de Pareto de la résistance thermique en fonction de la capacité de pompage sont tracées dans la figure 7. Toutes les ailettes utilisées dans cette comparaison sont cylindriques, avec un diamètre de 2 mm et une longueur de 6 mm. L'espacement entre les ailettes est de 1 mm, ce qui équivaut à une distance de 3 mm entre les axes dans les deux directions pour les ailettes en ligne, tandis que pour les ailettes décalées, elle est de 2.6 mm dans la direction x et de 3 mm dans la direction z. Cela rend les ailettes décalées plus denses que les ailettes en ligne. La figure 6 montre les deux configurations d'ailettes avec les paramètres de conception.

En refroidissement par écoulement en canal, les motifs de broches décalées présentent



(a) ailettes décalées (staggered1)

(b) ailettes décalées avec ailettes murales (staggered2)

Figure 6: Les deux variantes de la configuration d'ailettes décalées avec les paramètres de conception

de meilleures performances de refroidissement que les motifs en ligne. En revanche, les motifs en ligne donnent de meilleurs résultats dans le refroidissement par jet impactant.

Effet de l'épaisseur d'AlN

Un autre paramètre d'influence est l'épaisseur de la céramique AlN entre broches et puce (paramètre t dans la Fig. 4). La Figure 8 représente les flux de chaleur vers le liquide de refroidissement à travers le dissipateur thermique en AlN. Une plaque de base plus épaisse t permet un plus grand flux de chaleur le long des axes x et z (« étalement de la chaleur »), tandis que le gradient de température diminue dans l'axe y.

Un bon étalement de la chaleur produit une distribution de température plus uniforme dans la puce. Cela est dû au fait que l'étalement de chaleur le long des directions x et z réduit la densité de chaleur dans la direction y. Cependant, un AlN excessivement épais peut entraîner un trajet plus long de la puce au liquide de refroidissement dans les trois directions. L'épaisseur t doit donc être optimisée pour assurer une dissipation maximale de chaleur dans les directions x et z tout en maintenant un gradient de température approprié dans toutes les directions.

Les simulations CFD sont réalisées pour différentes valeurs de t (allant de 1 à 5 mm), tandis que les autres paramètres sont maintenus constants à l'exception du diamètre du jet, qui varie dans la plage de $5\,\text{mm} < d_{jet} < 9\,\text{mm}$, et des débits dans la plage de $1\,\text{L/min} < \dot{V} < 5\,\text{L/min}$. Des broches cylindriques de longueur $h = 6\,\text{mm}$ et de diamètre $d_{pins} = 2\,\text{mm}$ sont utilisées pour les calculs numériques. La Fig. 5.23 montre les dépendances de la résistance thermique en fonction de l'épaisseur de la céramique. La valeur optimale de t est trouvée à 3 mm, car elle forme le front de Pareto (des couches d'AlN plus minces ou

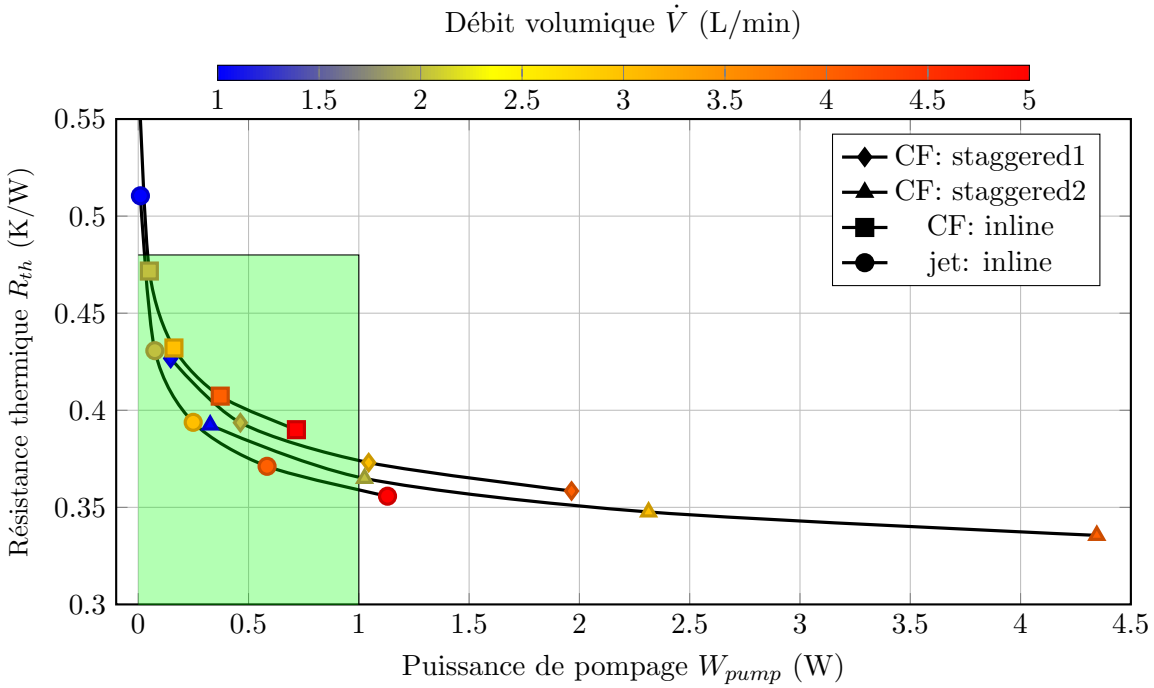
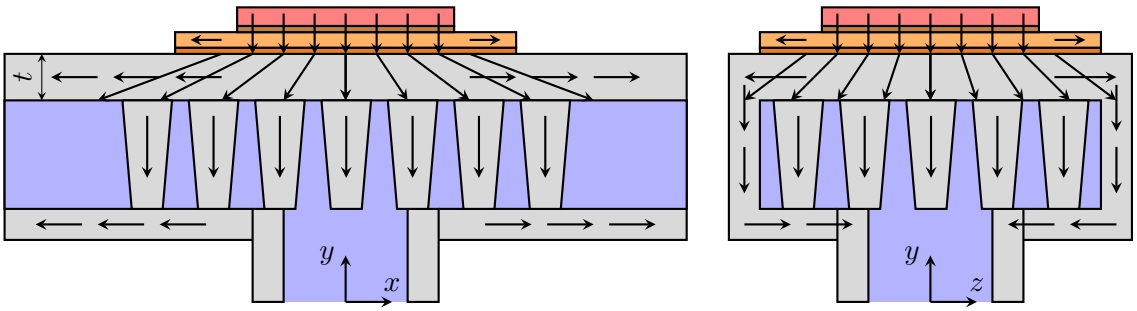


Figure 7: "Résistance thermique en fonction de la puissance de pompage pour toutes les configurations considérées (simulations CFD, pour le Novec 7500)

plus épaisses se traduisent par des valeurs de résistance thermique plus élevées).

Comparaison entre différentes structures de packaging

Cette section présente les performances de refroidissement des différentes structures de packaging. L'objectif est de démontrer l'avantage de la solution proposée dans cette thèse par rapport à des solutions plus classiques, y compris des déclinaisons très performantes (DBC intégré dans le dissipateur thermique), voir figure 10. Les simulations CFD sont réalisées pour un refroidisseur par jet impactant utilisant de l'eau comme fluide de refroidissement. Les couches de cuivre des DBC ont une épaisseur de 0.3 mm dans les deux structures, figure 10a et 10b. L'isolant en AlN du packaging traditionnel a une épaisseur de 0.65 mm, tandis que dans la structure intégrée, il a une épaisseur de 3 mm, la même que dans le packaging innovant, afin de voir les performances thermiques des deux structures avec la même capacité d'isolation électrique. Le dissipateur thermique du packaging traditionnel est en alliage d'aluminium et celui du packaging intégré est en cuivre. Les propriétés de l'alliage d'aluminium sont considérées comme identiques à celles de l' AlN ($\lambda = 170\,\mathrm{W/mm^2}$). La semelle du packaging traditionnel est fixée sur le dissipateur thermique à l'aide d'une graisse thermique (TIM). Le TIM a une épaisseur de 50 µm et une conductivité thermique de 5 W/mK (une valeur optimiste). Les trois structures ont la



(a) Coupe le long du canal (b) Coupe en travers du canal

Figure 8: Représentation schématique des flux de chaleur dans le refroidisseur AlN à jet impactant

même conception interne de broches avec une hauteur de canal de 6 mm et des ailettes coniques avec un diamètre supérieur de 2.8 mm et un diamètre inférieur de 1.8 mm.

La Figure 11 présente les résultats numériques de la distribution de température dans les trois structures de packaging à 3 L/min. Dans cette configuration, la résistance thermique est réduite de 0.32 K/W (packaging traditionnel) à 0.26 K/W (packaging innovant). De plus, le dissipateur thermique en AlN offre des avantages supplémentaires en termes d'isolation électrique : dans le packaging traditionnel, l'isolation électrique est assurée au niveau du substrat, où la céramique est mince (généralement 0.65 mm), tandis que le dissipateur thermique en céramique utilise une couche beaucoup plus épaisse (ici 3 mm). De plus, on peut s'attendre à un stress thermomécanique plus faible pour le packaging innovant, car le coefficient de dilatation thermique de l'AlN (4-5 ppm/K) est beaucoup plus proche de celui des puces (de l'ordre de 3 ppm/K) que de l'alliage d'aluminium (19-25 ppm/K) et du cuivre (17.8 ppm/K).

La résistance thermique obtenue en fonction du débit est résumée dans la figure 12. Elle montre la résistance thermique attendue des trois variantes de packaging étudiées en fonction du débit.

Conclusion des simulations CFD pour le module à une puce

Un refroidisseur sans ailettes internes ne parvient pas à atteindre la résistance thermique cible de 0.48 K/W avec une puissance de pompage inférieure à 1 W. Une optimisation CFD est effectuée sur des paramètres tels que le concept de refroidissement (jet impactant et écoulement en canal), la forme des ailettes (circulaires, coniques et carrées), l'agencement des ailettes (en ligne et décalées) et l'épaisseur du substrat en céramique (AlN). L'étude révèle que les ailettes coniques sont les plus performantes. L'agencement des ailettes en ligne convient mieux au refroidisseur à jet impactant, tandis que l'agencement des ailettes décalées est plus efficace pour le refroidisseur à écoulement en canal. L'AlN plus

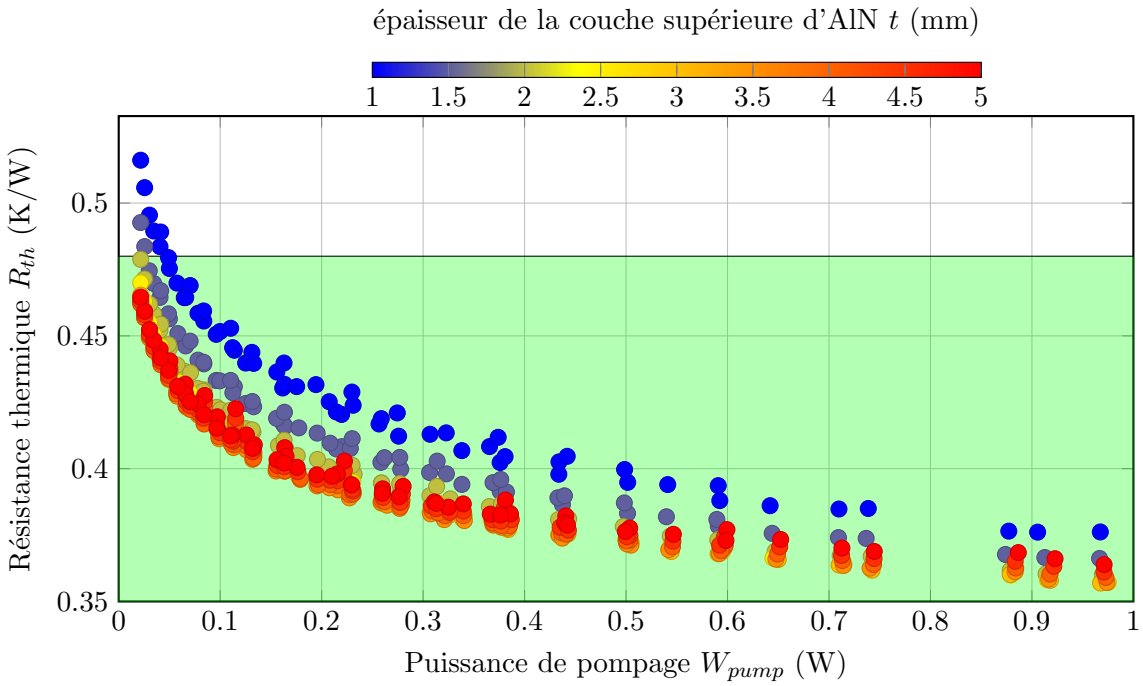


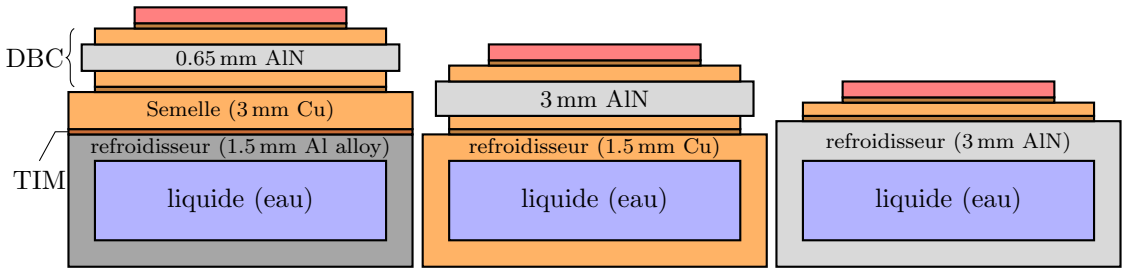
Figure 9: Résistance thermique en function de la puissance de pompage, pour différentes épaisseurs d'AlN t (simulations CFD, pour du Novec 7500 et $d_{pins} = 2\,\text{mm}$).

épais (jusqu'à 3 mm ou 3.5 mm) améliore les performances de refroidissement en raison de son effet d'étalement thermique supérieur. La résistance thermique cible est facilement atteinte avec une puissance de pompage inférieure à 1 W. Enfin, la structure de packaging novatrice proposée dans ce travail est comparée aux packagings existants, démontrant que la structure suggérée surpasse significativement les autres structures de packaging.

Les contraintes de fabrication nécessitent de légères modifications à cet optimum, notamment des diamètres supérieurs et inférieurs d'ailettes de 2.8 mm et 1.8 mm. Le diamètre de l'orifice d'entrée est fixé à 7.5 mm étant choisi en raison de la disponibilité de raccords correspondants pour la production du prototype. Le tableau 1 présente les paramètres considérés pour la configuration optimale, comprenant une hauteur de canal de 6 mm pour des ailettes de 2 mm. Une épaisseur d'AlN de 3.3 mm a été déterminée comme choix optimal.

Table 1: Paramètres géométriques optimaux de la conception du refroidisseur à jet pour un module à une puce

configuration	d_t	d_b	d_{jet}	H	t_{AlN}
broches cylindriques	2 mm	2 mm	6 to 8 mm	6 mm	3 to 3.5 mm
broches coniques	1.5 mm	2.5 mm	6 to 8 mm	6 mm	3 to 3.5 mm
broches réalisées	1.8 mm	2.8 mm	7.5 mm	6 mm	3.3 mm

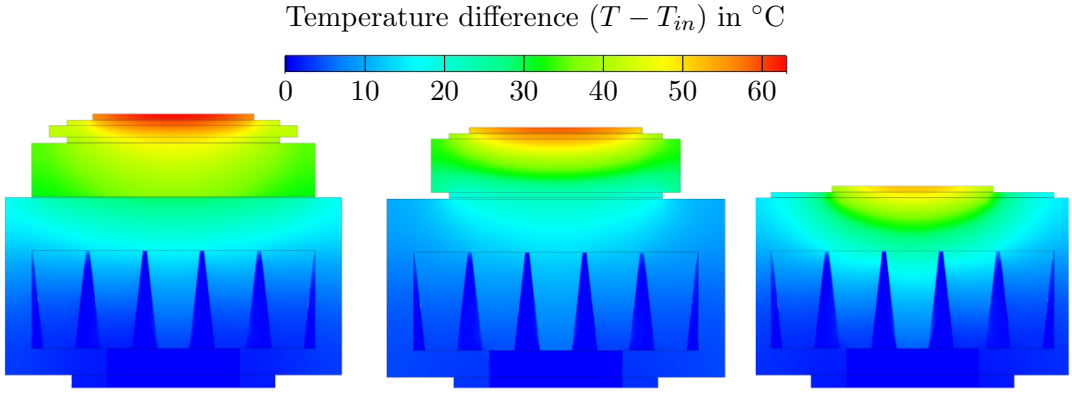


(a) Structure de packaging traditionnelle

(b) Module de puissance avec dissipateur thermique intégré dans la semelle

(c) Structure de packaging innovante

Figure 10: Comparaison schématique entre les trois packagings différents utilisés pour les simulations CFD



(a) Traditional packaging $R_{th} = 0.32\,\mathrm{K/W}$

(b) DBC on copper heatsinks $R_{th} = 0.3\,\mathrm{K/W}$

(c) Novel packaging $R_{th} = 0.26\,\mathrm{K/W}$

Figure 11: Distribution de température dans les trois solutions de packaging à 3 L/min

Validation expérimentale du module mono-puce

Cette section traite des essais expérimentaux sur le module à une seule puce. Tout d'abord, la production des véhicules d'essai est détaillée. Ensuite, la configuration de test est présentée. Enfin, les résultats expérimentaux pour différents liquides de refroidissement sont discutés et comparés aux résultats CFD.

La figure 13 montre une vue schématique des refroidisseurs. Le refroidisseur à jet comporte une entrée et deux sorties, tandis que le refroidisseur à écoulement en canal comporte une entrée et une sortie. La structure supérieure du refroidisseur en AlN est identique pour les deux modules. Trois prototypes différents sont construits pour le test thermique, un refroidisseur à écoulement en canal avec une épaisseur de céramique AlN de 3 mm, un refroidisseur à jet impactant avec une épaisseur de 1.5 mm et un refroidisseur à jet impactant avec une épaisseur de 3 mm.

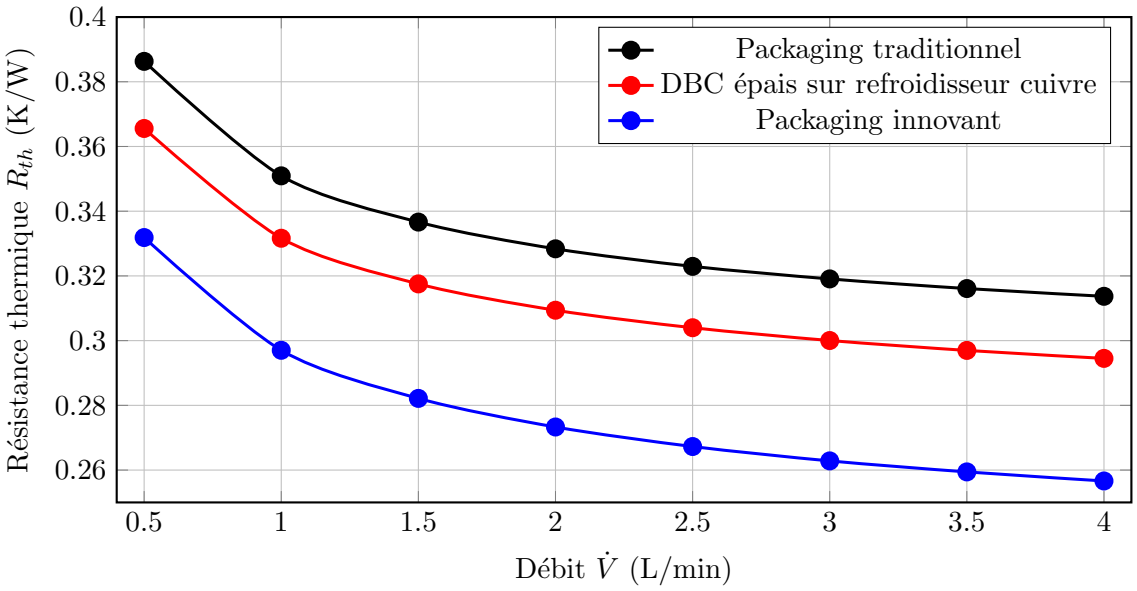
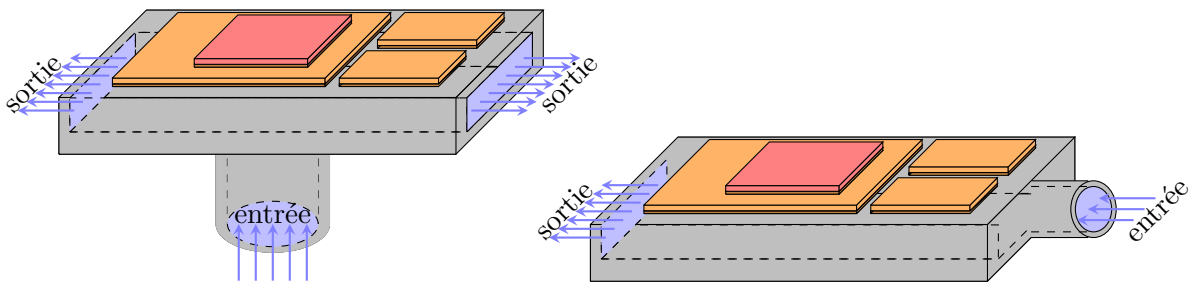


Figure 12: Comparaison de la résistance thermique entre trois packagings possibles (CFD, refroidisseur par jet impactant avec les mêmes géométries de broches)

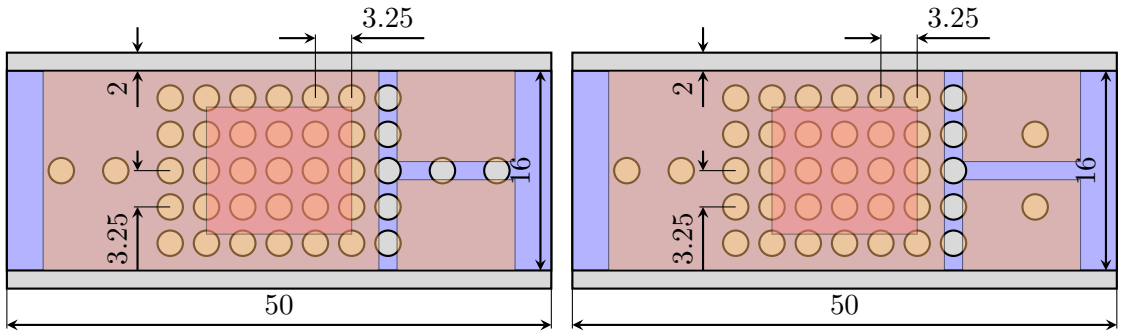


(a) jet impactant (b) écoulement en canal

Figure 13: Conception schématique du module pour le test thermique : effet jet et écoulement en canal

Conception des refroidisseurs en AlN

Les deux refroidisseurs ont des broches identiques sous la puce. Quatre broches supplémentaires (deux de chaque côté) sont placées aux extrémités du canal pour des raisons de résistance mécanique. Les broches sont disposées en ligne avec le flux de liquide. Pour l'écoulement en canal, les broches sont placées en parallèle à l'entrée pour éviter une chute de pression plus élevée, car ces broches sont proches de l'entrée. La figure 5.30 montre les structures d'ailettes pour les deux refroidisseurs. Les broches sont espacées de 3.25 mm. La conception des broches a été discutée avec le fabricant "CeramTec GmBH, Marktredwitz", en tenant compte des possibilités techniques et des limitations liées à la fabrication d'un dissipateur de chaleur en céramique. Les refroidisseurs ont une longueur de 50 mm et une largeur de canal de 16 mm. La puce est frittée à 2 mm du bord droit de la plaque de cuivre principale (16 mm × 26 mm) au centre du canal. Les deux autres plaques de cuivre ont une taille de 7 mm × 12 mm et servent aux connexions électriques.



(a) refroidisseur par jet impactant (b) refroidisseur à écoulement en canal

Figure 14: Schéma de la coupe transversale au centre du canal sous la puce montrant les paramètres de conception

Vue d'ensemble de l'expérience

Après leur fabrication, les modules sont intégrés dans un banc d'essai comprenant une boucle de refroidissement de fluide et des circuits électriques. Cette section présente en détail la configuration expérimentale. La construction est divisée en deux parties : la boucle de fluide et les connexions électriques pour faire fonctionner le semi-conducteur.

Circuit liquide

Étant donné que les fluides diélectriques sont agressifs pour certains plastiques (joints notamment), une pompe à entraînement magnétique résistante aux produits chimiques est utilisée. Le liquide est pompé dans un échangeur de chaleur pour contrôler la température d'entrée, puis est dirigé vers le DUT. Ensuite, le liquide s'écoule vers la sortie dans un

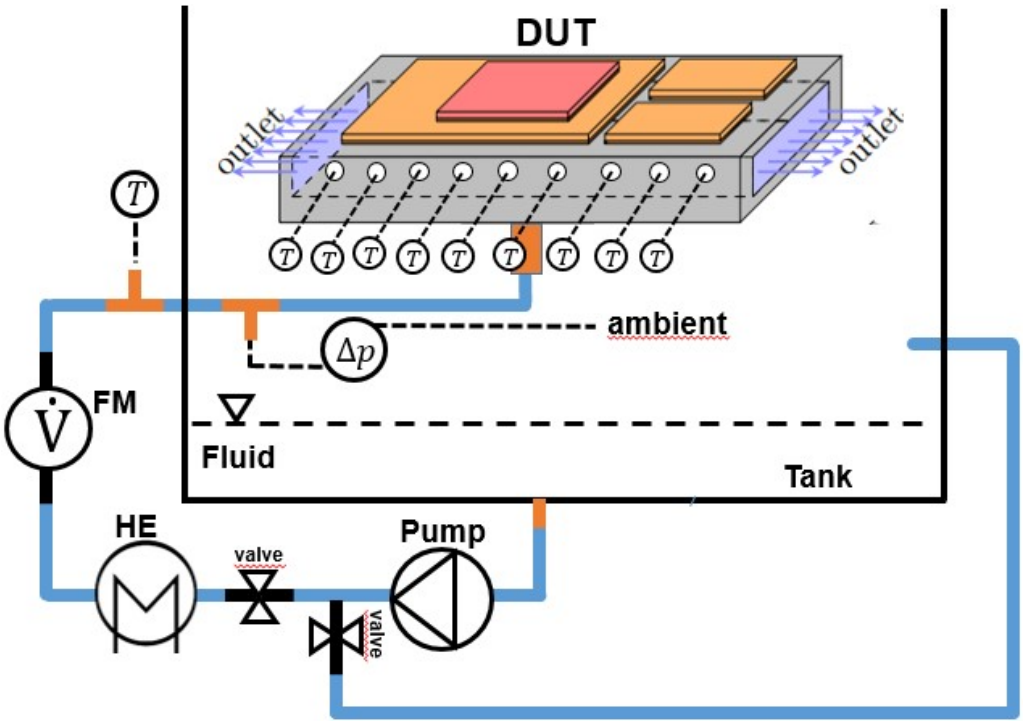


Figure 15: Vue d'ensemble schématique de la configuration de la boucle fluidique pour le refroidisseur à une puce

réservoir. Un débitmètre est placé en amont du refroidisseur. Deux vannes permettent de contrôler le débit: une vanne est située juste avant l'échangeur de chaleur, l'autre permet de contourner le refroidisseur au cas où un débit très faible serait nécessaire. Un soin particulier est apporté à la conception du circuit de refroidissement pour éviter les matériaux élastomères qui pourraient réagir avec le Novec 7500: tous les tubes utilisés sont en cuivre, des raccords de compression en cuivre et en acier sont utilisés pour connecter les tuyaux. La figure 15 montre le schéma du circuit liquide. Pour estimer la capacité de pompage du refroidisseur, la perte de pression entre l'entrée et la sortie (pression atmosphérique dans ce cas) est mesurée. La puissance hydraulique (W_{pump}) est ensuite le produit du débit ($\dot{V}$) et de la perte de pression (Δp) :

$$W_{pump} = \dot{V} \times \Delta p \tag{1}$$

De plus, la température à l'entrée est mesurée, ce qui est utilisé ultérieurement pour calculer la résistance thermique. Neuf thermocouples sont utilisés pour mesurer la température de l'AlN au centre du canal. Ces données sont ensuite utilisées pour valider les résultats de la CFD. Un débit de liquide de 0.5 L/min à 3 L/min est utilisé lors de la mesure.

Connexions électriques

Afin de faire fonctionner la puce sur le refroidisseur, elle doit être connectée électriquement. Un courant de chauffe est appliqué entre le collecteur et l'émetteur à l'aide d'un analyseur thermique (Phase 12B, Analysis Tech), sous une polarisation grille-émetteur constante (9 V). L'analyseur thermique mesure la chute de tension collecteur-émetteur, qui est une image de la température. Une vue d'ensemble de la configuration de test électrique est présentée dans la figure 16.

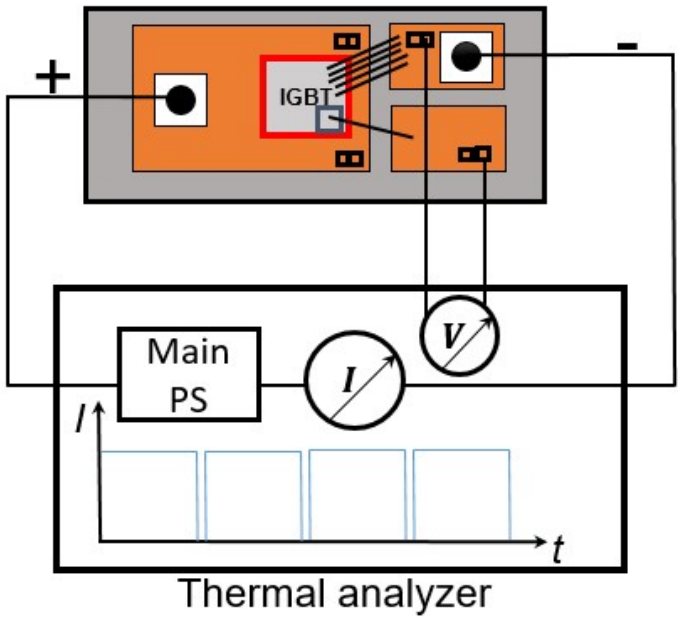


Figure 16: Vue d'ensemble de la configuration de test électrique pour le refroidisseur à une puce

Résultats des tests

La résistance thermique mesurée (R_{th}) en fonction de la capacité de pompage du refroidisseur est présentée dans la figure 17 avec de l'eau et du Novec7500 comme fluides de refroidissement. Les données numériques et expérimentales concordent relativement bien, avec de légères déviations. Le refroidisseur à jet impactant présente une résistance thermique plus faible à une puissance de pompage réduite. Les refroidisseurs à jet ont une meilleure frontière de Pareto par rapport au refroidisseur à écoulement en canal, en raison de leur vitesse plus élevée et de leur turbulence accrue. Alors que les résultats de la CFD indiquent que le refroidisseur à jet en AlN avec un substrat plus mince fonctionne légèrement mieux, les résultats expérimentaux montrent que la frontière de Pareto du refroidisseur avec un substrat plus épais est plus basse. Cette déviation peut être attribuée

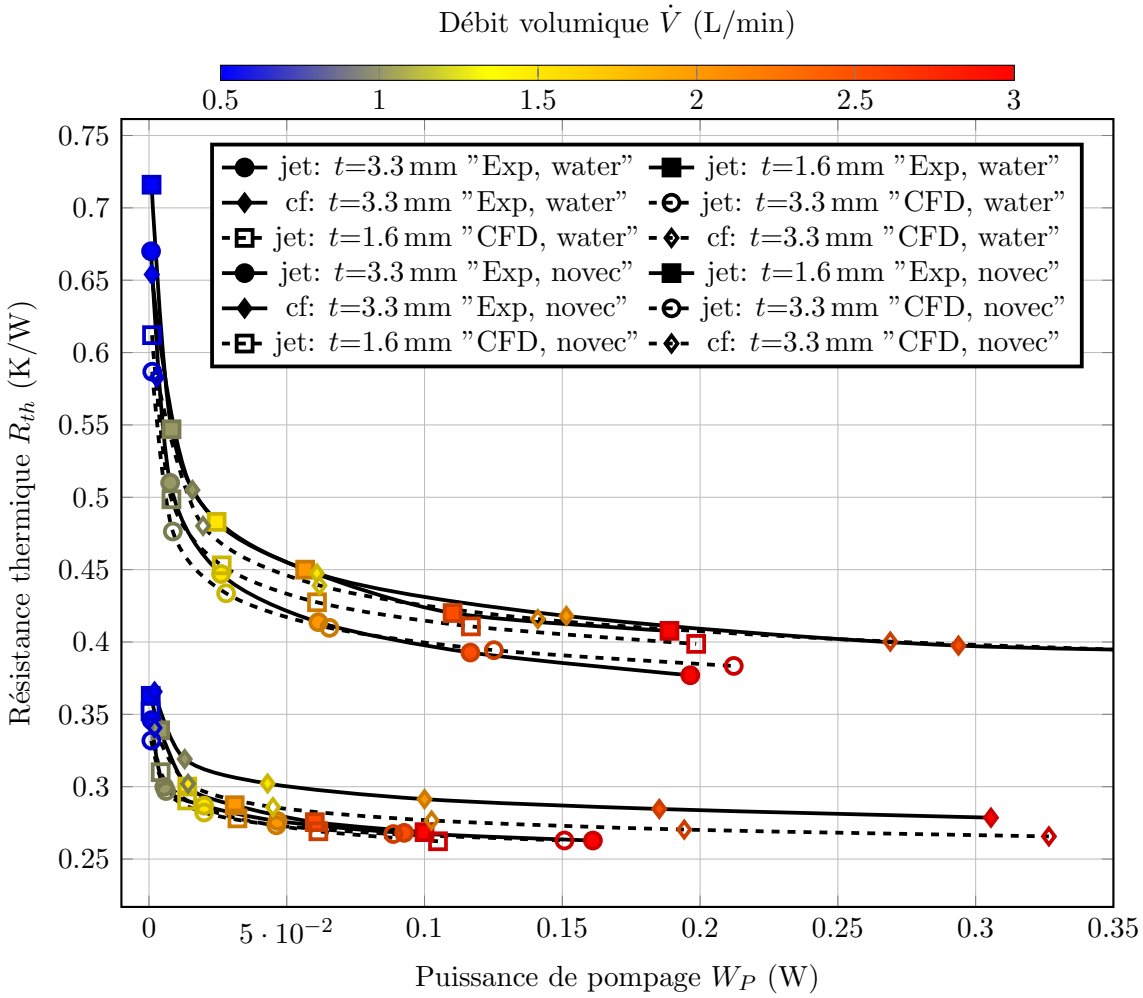


Figure 17: La résistance thermique mesurée comparée aux résultats numériques en fonction de la capacité de pompage à différentes vitesses d'écoulement d'eau

à des différences entre les ailettes des deux refroidisseurs, en raison de contraintes de fabrication. Le refroidisseur à eau avec un AlN plus mince devrait présenter de meilleures performances en raison de la capacité thermique élevée de l'eau (selon les simulations CFD). Cependant, le refroidisseur AlN plus mince a des ailettes légèrement plus petites que le refroidisseur AlN plus épais.

La figure 18 présente les températures mesurées dans la paroi supérieure (3.3 mm) du refroidisseur à jet pour différents débits. Les données expérimentales et simulées présentent une forte concordance.

La figure 19 présente la courbe d'impédance thermique pour les trois refroidisseurs, à différentes vitesses d'écoulement (0.5 L/min, 1 L/min et 3 L/min). Ces résultats corroborent les valeurs de résistance thermique obtenues dans la figure 17. Des débits plus élevés entraînent une dynamique thermique plus rapide, avec un régime permanent (résistance

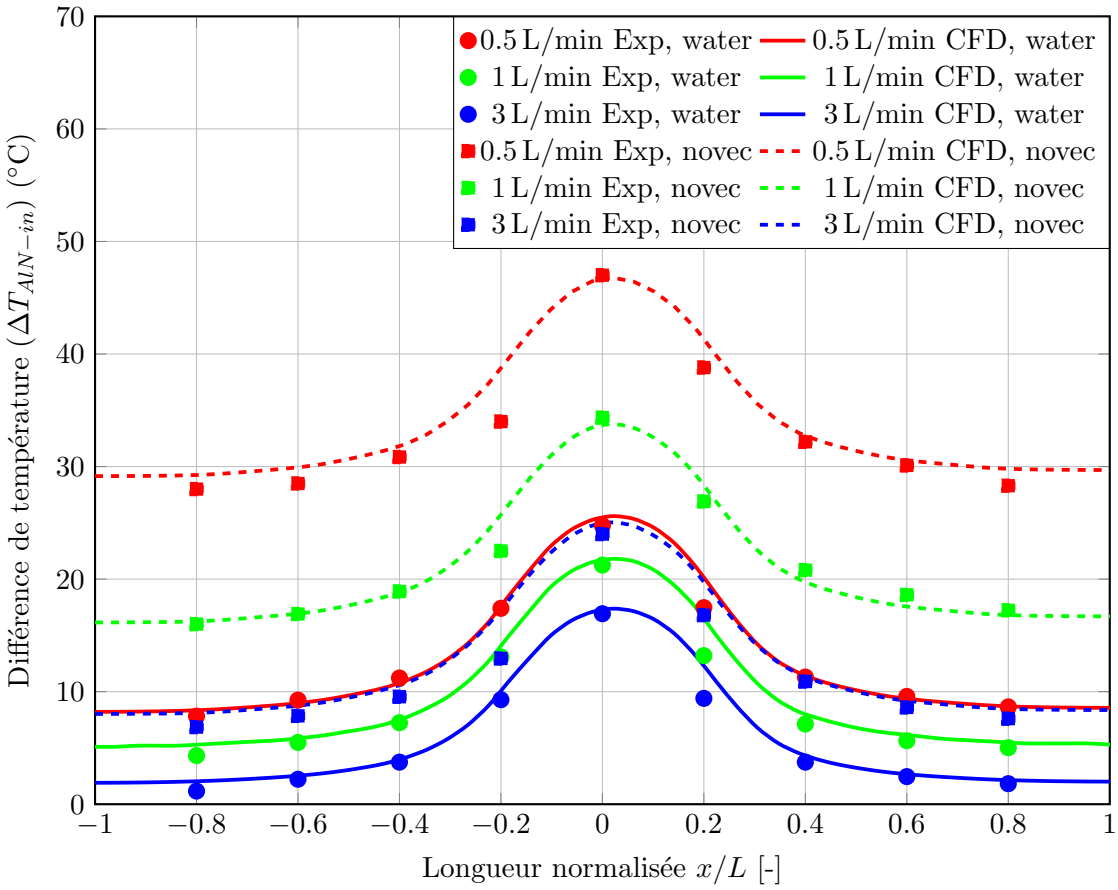


Figure 18: Distribution de température dans l'AlN pour le refroidisseur à jet. Mesure (Exp.) et simulation (CFD) avec de l'eau comme fluide caloporteur

thermique) atteint lus tôt. Il faut plus de temps au refroidisseur à écoulement en canal (ligne en pointillés) pour atteindre le régime permanent. À faible débit, le refroidisseur à jet avec 3.3 mm (ligne continue) présente de meilleures performances, avec une valeur de résistance thermique plus faible que les deux autres refroidisseurs. À des débits plus élevés (par exemple, 3 L/min), la courbe Z_{th} du refroidisseur à écoulement en canal se rapproche des courbes des refroidisseurs à jet. Cependant, la conception à écoulement en canal nécessite une puissance de pompage beaucoup plus importante que les refroidisseurs à jet, comme indiqué dans la figure 17.

Conclusions sur le module mono-puce

L'optimisation de la conception du refroidisseur d'un module à une seule puce est réalisée grâce à des simulations de dynamique des fluides (CFD). Cette analyse met en évidence qu'atteindre les conditions cibles, caractérisées par une résistance thermique inférieure à

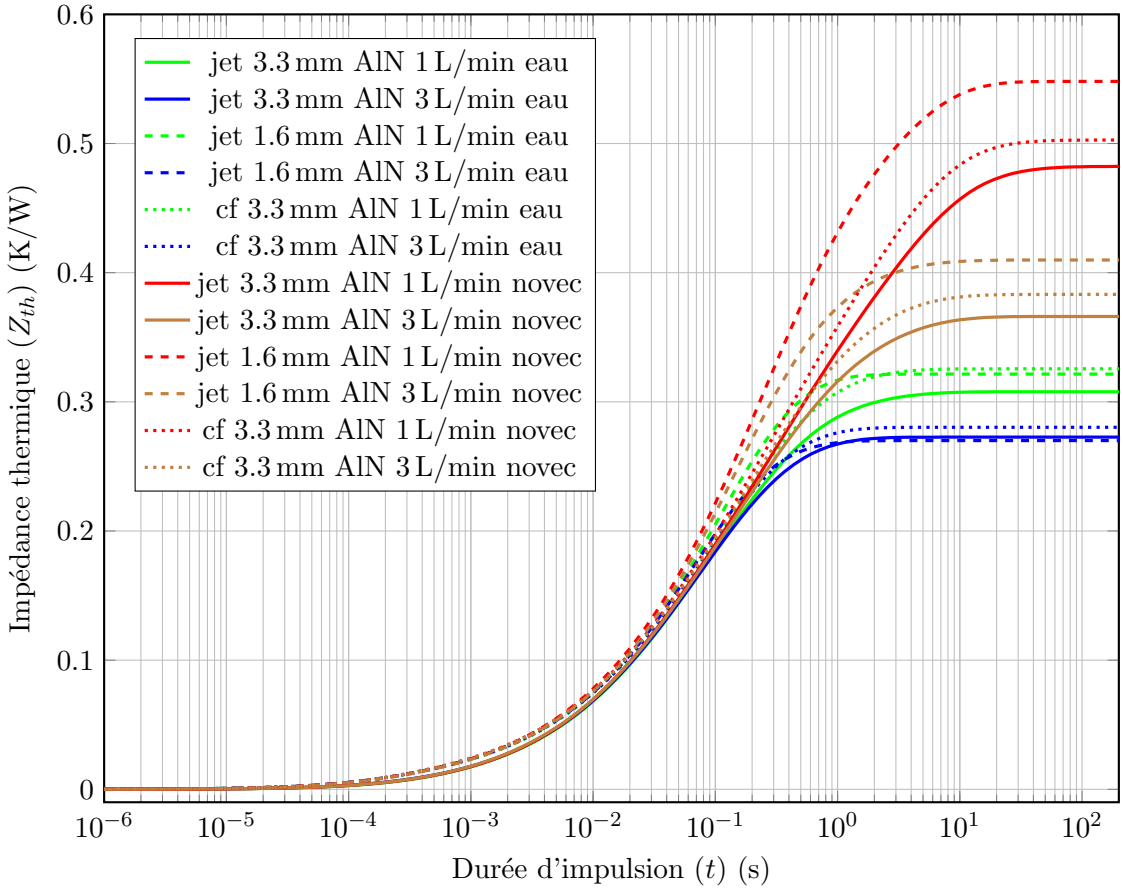


Figure 19: Impédance thermique mesurée (Z_{th}) pour les trois refroidisseurs avec de l'eau comme fluide caloporteur à différentes vitesses d'écoulement

0.48 K/W et une puissance de pompage inférieure à 1 W, est inatteignable sans l'ajout d'ailettes. L'introduction de structures d'ailettes entraîne une amélioration significative des performances de refroidissement et permet d'atteindre les conditions spécifiées. Différents fluides de refroidissement sont comparés, l'eau démontrant les performances de refroidissement les plus efficaces. Novec7500, bien que moins performant, permet cependant d'atteindre les objectifs fixés.

À la suite du processus d'optimisation du refroidisseur, un test expérimental thermique est réalisé pour valider les résultats de la CFD. Cette expérience implique la mesure de la résistance thermique, de la puissance de pompage et de la distribution de la température dans l'AlN. Les résultats de la CFD et de l'expérience présentent une forte concordance, renforçant la confiance dans les résultats de la simulation. Cela ouvre la voie à de nouvelles simulations visant à optimiser la conception de modules multi-puces, promettant des performances de refroidissement et d'efficacité accrues.

Système de refroidissement pour le module de 20 kV

Un refroidisseur mono-puce a été présenté dans le chapitre précédent, mais un véritable module de puissance est plus complexe et se compose de nombreux composants. L'idée originale était de construire un module à demi-pont avec deux SiC MOSFET de 10 kV. En connectant les deux commutateurs en série, une tension de blocage de 20 kV pour l'ensemble du module devait être démontrée. En raison de l'indisponibilité des composants 10 kV, une approche alternative a été développée [4], qui repose sur la connexion en série de six MOSFET SiC de 3.3 kV (GeneSiC, G2R50MT33-CAL). Pour équilibrer la tension (statiquement et dynamiquement), un circuit d'équilibrage sophistiqué est requis, ce qui génère des pertes supplémentaires.

Le but de ce travail est de maintenir la température de jonction du SiC-MOSFET en dessous de 100 °C pour une température de fluide de 40 °C. Chaque puce dissipe 120 W (densité de puissance de $q = 367\,\mathrm{W/cm^2}$), ce qui signifie que le système de refroidissement doit avoir une une résistance thermique R_{th} inférieure à 0.5 K/W.

Conception du Module

Le refroidisseur multi-puces mesure 50 mm de large et 100 mm de long. Quatre plaques de cuivre sont frittées sur le refroidisseur en AlN, à une distance de 5 mm par rapport aux bords de l'AlN, ce qui est nécessaire pour l'isolation. Les MOSFETs de 3.3 kV ont une taille de 3.676 mm × 8.9 mm. La Figure 20 montre la vue de dessus de la conception utilisée pour les simulations numériques.

La Figure 21 présente une coupe schématique du module montrant les matériaux utilisés pour les simulations numériques. Le refroidisseur en AlN a une hauteur totale de 12.5 mm, ce qui est l'espace nécessaire pour bloquer une tension de 20 kV. Les broches mesurent 6 mm de long, ce qui est la longueur optimale des broches optimisées dans les modules à une puce (voir la section I). Le dessus en AlN a une épaisseur de 3.3 mm pour bloquer la tension requise. Une grande plaque de cuivre est brasée sur le refroidisseur.

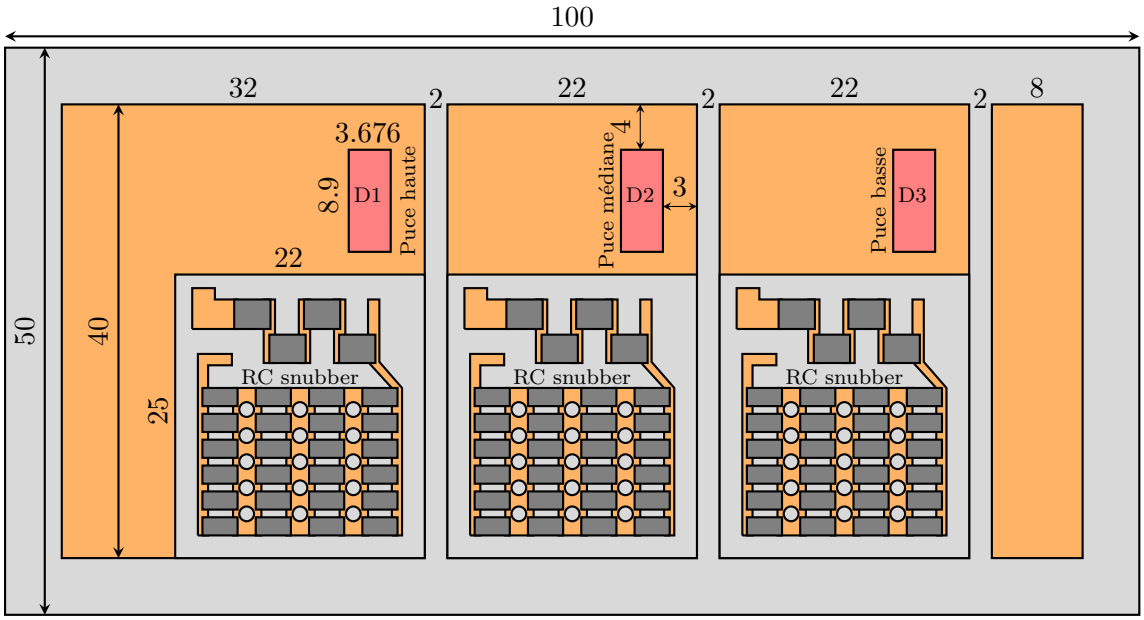


Figure 20: Vue de dessus d'un refroidisseur équipé de ses puces et de ces circuits d'équilibrage, avec les dimensions utilisées pour la simulation.

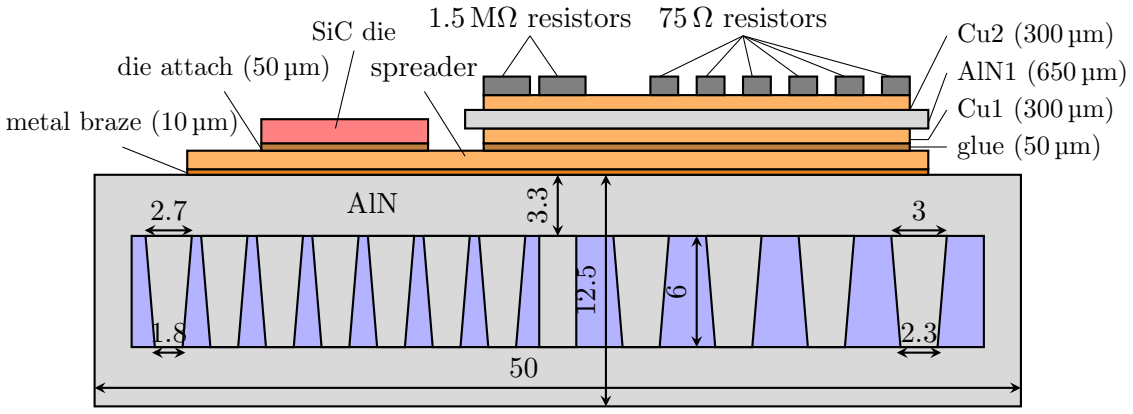


Figure 21: Structure prise en compte pour la conception, montrant les matériaux utilisés et les paramètres de conception

Une puce SiC est frittée sur le cuivre et un circuit d'équilibrage est collé avec un adhésif conducteur thermique.

Optimisation numérique du module à trois puces

Conception des ailettes

Le module haute tension complet est composé de deux refroidisseurs. Chaque refroidisseur en AlN comporte de trois MOSFETs SiC et trois circuits d'équilibrage. Toutes ces pièces doivent être refroidies. Cependant, les circuits d'équilibrage génèrent une densité de chaleur beaucoup plus faible que les éléments SiC. De plus, la température des circuits d'équilibrage est moins critique que celle des MOSFETs (elle doit simplement rester inférieure à 150 °C). Par conséquent, aucun processus d'optimisation n'est nécessaire pour les structures d'ailettes situées sous les circuits d'équilibrage. Pour faciliter la fabrication, des ailettes plus grandes, espacées davantage que celles situées sous les puces SiC sont placées sous les circuits d'équilibrage.

La figure 22 montre une section transversale au milieu du canal de refroidissement montrant la distribution des ailettes. Les puces sont placées sur la partie supérieure du refroidisseur et les circuits d'équilibrage sur la partie inférieure. Une paroi large de 2 mm et longue de 75 mm est placée au centre du canal pour séparer les deux parties afin de contrôler l'écoulement du fluide. Les ailettes sous les puces SiC ont un diamètre de 2 mm, tandis que des ailettes de 3 mm sont utilisées sous les circuits d'équilibrage. Les ailettes en ligne sont situées sous la puce du milieu, où se trouve la buse d'entrée, et toutes les ailettes sous les autres composants sont décalées. Le liquide s'écoule verticalement en frappant la surface inférieure de la puce SiC du milieu, puis se divise en deux courants s'écoulant vers les puces latérales. Le fluide s'écoule à travers l'espacement latéral vers la sortie, qui est située directement sous le circuit d'équilibrage du milieu. La distribution de la vitesse au milieu du canal à 3 L/min est illustrée dans la figure 23.

La puce supérieure (D3) à droite devrait être à une température plus élevée en raison de sa position à l'extrémité d'une plaque de cuivre plus petite par rapport à la puce supérieure (D1). La figure 24 montre la résistance thermique minimale et maximale des puces SiC. Le graphique compare la structure d'ailettes symétrique à la structure d'ailettes asymétrique (comportant plus d'ailettes sous la puce SiC inférieure, voir la figure 22). On peut voir que le front de Pareto de la puce la plus chaude s'améliore à mesure qu'il y a plus d'ailettes sous la puce inférieure, offrant une meilleure uniformité entre les 3 puces du module.

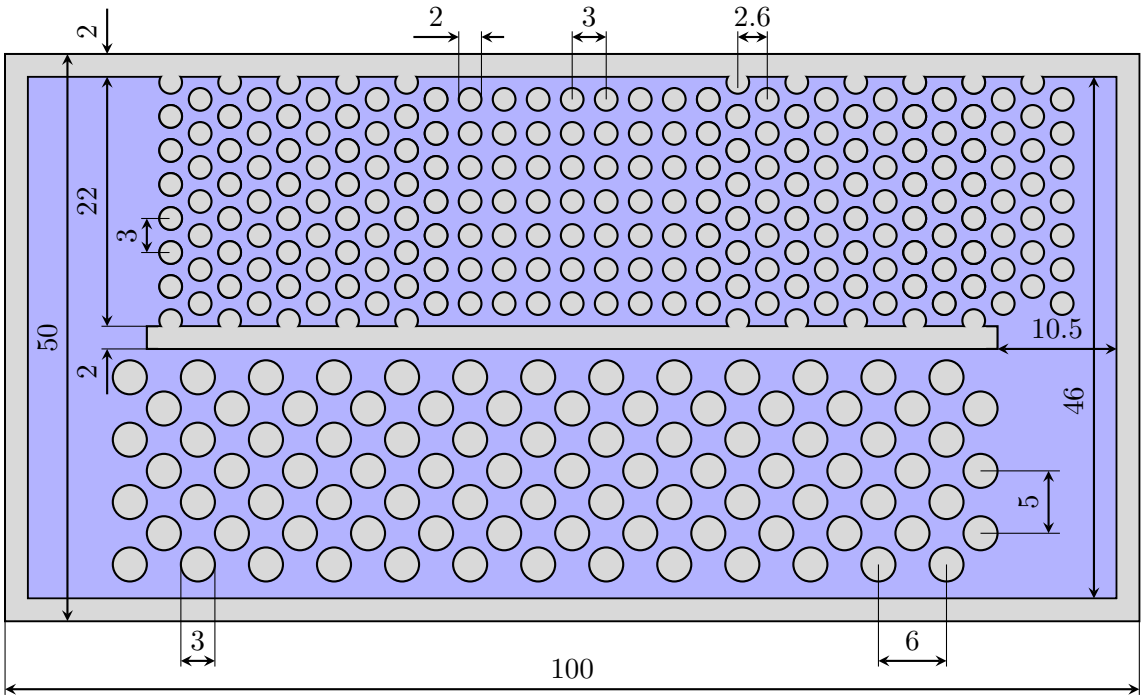


Figure 22: Une section transversale au milieu du canal sous les puces, montrant la conception et les paramètres des broches (ailettes).

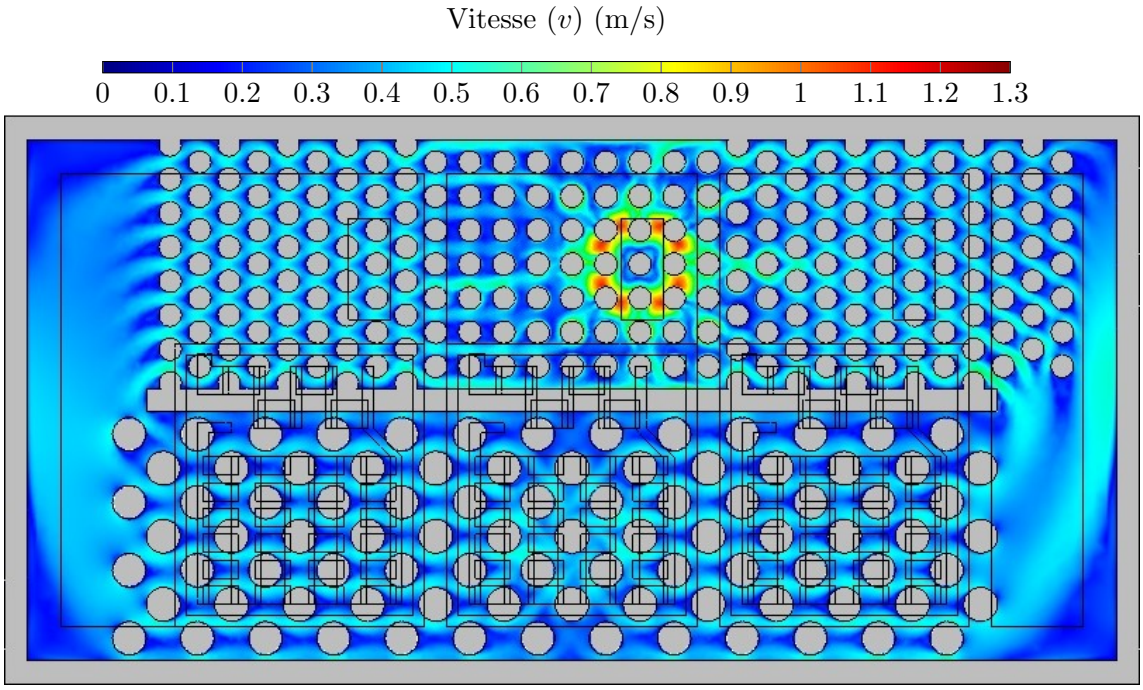


Figure 23: Distribution de vitesse au milieu du canal à 3 L/min

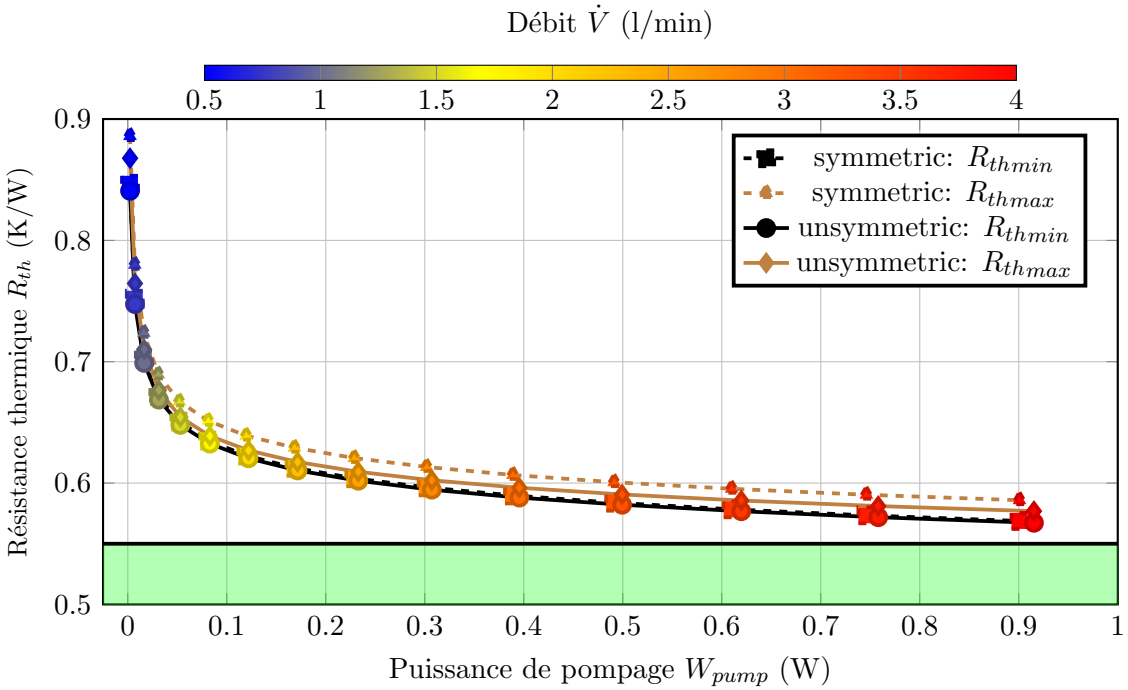


Figure 24: Résistance thermique minimale et maximale des puces avec distribution symétrique et asymétrique des ailettes en fonction de la puissance de pompage, échelle des couleurs : débit $\dot{V}$

Épaisseur du cuivre

Comme on peut le voir à partir des simulations précédentes, une résistance thermique de 0.5 K/W n'a pas encore pu être atteinte. La dissipation de chaleur vers le refroidisseur peut encore être améliorée en augmentant l'épaisseur du cuivre sur le refroidisseur en nitrure d'aluminium (AlN). En raison de la très haute conductivité thermique du cuivre, un cuivre plus épais permet à la chaleur dissipée de se propager sur une plus grande surface, plutôt que de rester cantonnée sur une petite surface directement sous les puces. La résistance thermique maximale des puces en fonction de l'épaisseur du cuivre est représentée dans la figure 25.

La résistance thermique souhaitée (zone verte) est ainsi atteinte avec une épaisseur de cuivre supérieure à 0.5 mm. Au delà d'une épaisseur de cuivre de 2 mm, la R_{th} s'améliore peu.

Effet du fluide de refroidissement

Les performances thermiques de l'eau et du Novec7500 sont présentées dans la figure 26 pour différentes épaisseurs de cuivre. Comparée au fluide diélectrique (Novec7500), l'eau montre des performances de refroidissement nettement supérieures en raison de sa conduc-

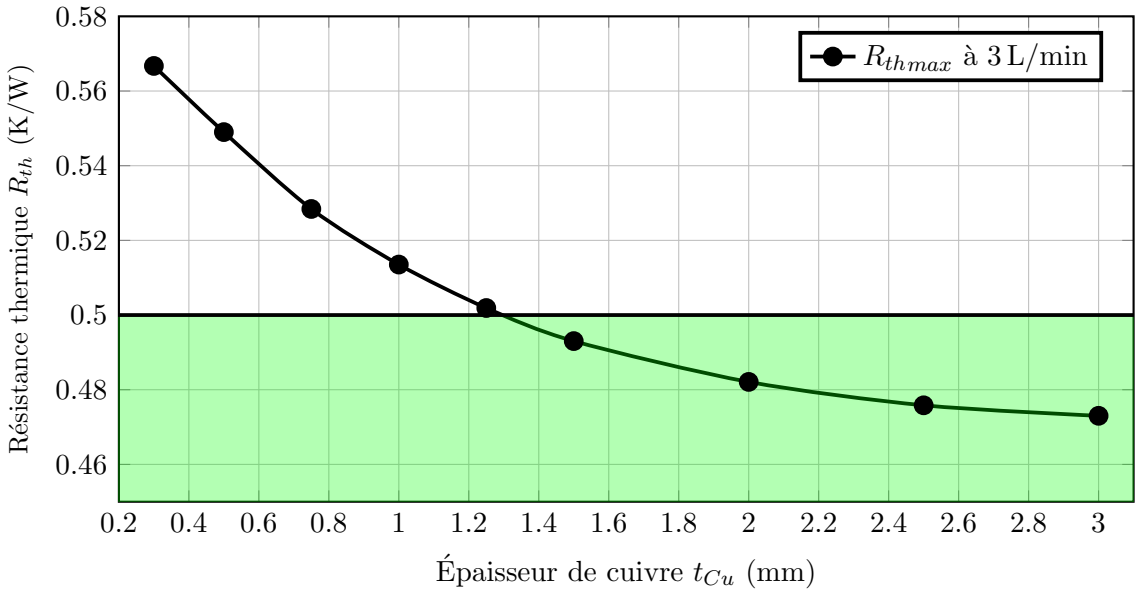


Figure 25: Résistance thermique en fonction de l'épaisseur du cuivre à 3 L/min

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tivité thermique et de sa capacité thermique plus élevées. En raison de sa viscosité plus faible, l'eau nécessite moins de puissance de pompage. La résistance thermique souhaitée de moins de 0.5 K/W peut ainsi être atteinte avec un débit et une puissance de pompage très faibles (<10 mW).

Étude expérimentale

Véhicules de test

Trois véhicules de test sont fabriqués pour des essais expérimentaux. Les trois ont tous des dissipateurs thermiques identiques et des structures similaires, mais avec trois épaisseurs différentes de cuivre. Comme pour le refroidisseur à une puce, les refroidisseurs en AlN métallisés sont fabriqués par CeramTec. Des feuilles de cuivre avec une métallisation en nickel et or sur la surface supérieure sont brasées sur le dessus du refroidisseur. La figure 27 montre le module à trois puces avec tous les composants.

Méthode de test

La configuration des tests est la même que celle utilisée pour le module simple à une puce dans le chapitre précédent (section I). Toutes les puces et les circuits d'équilibrage sont exploités et chauffés en même temps. La figure 28 montre la configuration de test pour la mesure du refroidisseur à trois puces. La figure 28 décrit la configuration de test. Un

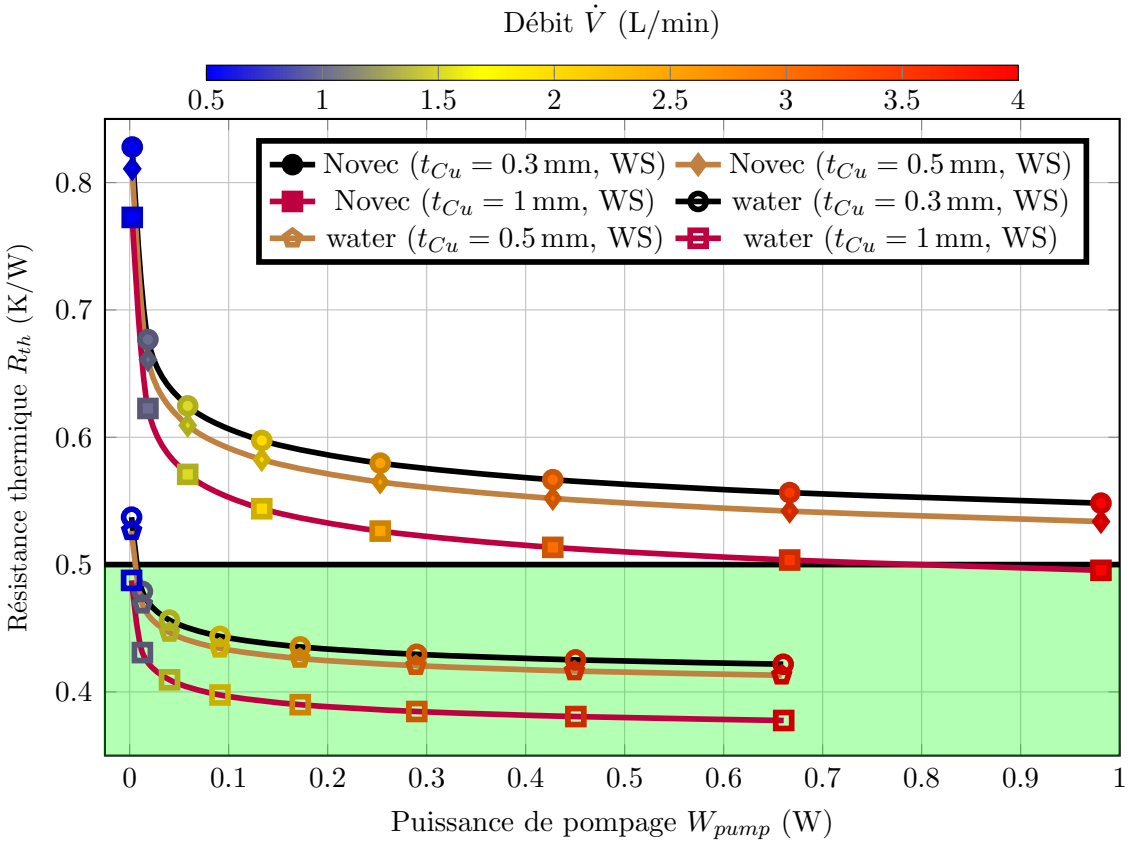


Figure 26: La résistance thermique maximale en fonction de la puissance de pompage avec Novec7500 et de l'eau comme liquides de refroidissement pour différentes épaisseurs de cuivre (WS : avec circuit d'équilibrage, NS : sans circuit d'équilibrage).

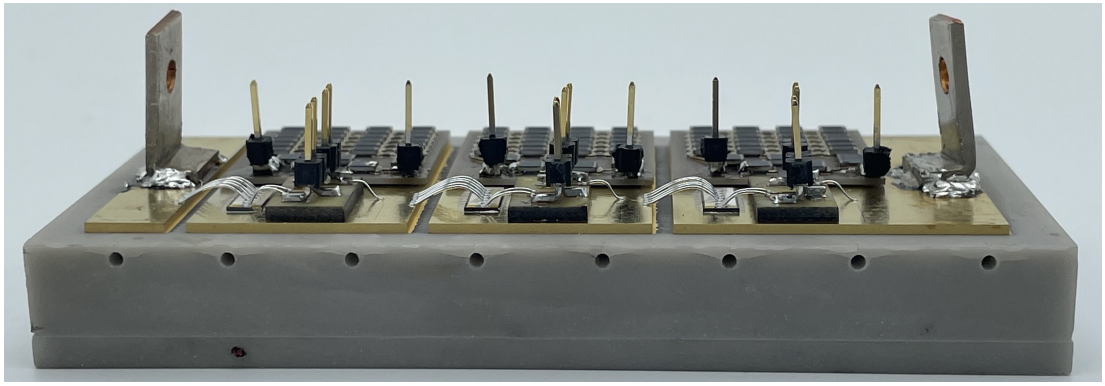
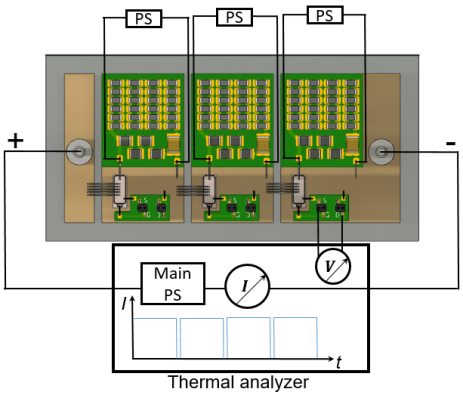
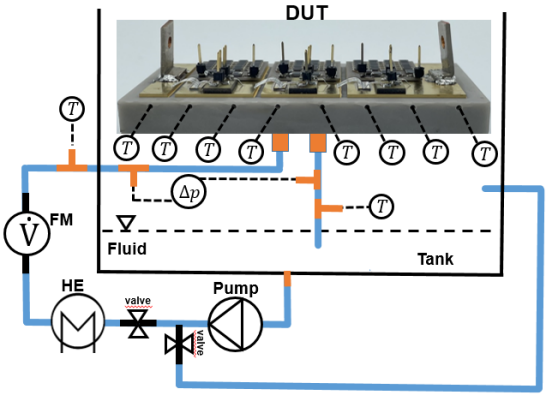


Figure 27: Le sous-module complet à trois puces avec tous les composants sur le refroidisseur



(a) Connexions électriques aux circuits d'équilibrage et au puces pour la mesure thermique.



(b) Circuit de refroidissement utilisé.

Figure 28: Circuit fluide et connexions électriques du module

analyseur thermique est utilisé pour mesurer la température de jonction des puces SiC. Chaque circuit d'équilibrage est connecté à une alimentation électrique indépendante, et dissipe 54 W. En plus de la température des puces SiC, la température de l'AlN dans l'AlN est mesurée, voir la figure 28a.

Résultats expérimentaux

Une série d'essais est réalisée avec du Novec7500 et de l'eau. La comparaison entre valeurs de R_{th} mesurées et simulées est donnée figure 29. Les puissances de pompage mesurées correspondent bien aux valeurs simulées. Les mesures de R_{th} pour l'eau sont légèrement au-dessus des prédictions CFD, mais cela reste acceptable. Pour le Novec7500, les résultats expérimentaux sont légèrement meilleurs qu'attendu.

Résumé du module multi-puce

La conception des sous-modules a été élaborée et optimisée par CFD. Cette conception intègre une disposition hybride de broches, comprenant à la fois des configurations décalées et en ligne. Pour améliorer l'efficacité du refroidissement, un unique jet a été positionné de manière stratégique sous la puce centrale, qui utilisait des broches en ligne, tandis que les deux autres puces bénéficiaient d'un refroidissement par un système à écoulement en canal, utilisant des dispositions de broches décalées.

Par la suite, les refroidisseurs en AlN ont été fabriqués et des véhicules d'essai à puces multiples ont été assemblés. Trois sous-modules distincts ont été fabriqués, chacun variant en termes d'épaisseur de cuivre (0.3 mm, 0.5 mm et 1 mm). À la suite de cela, nous avons

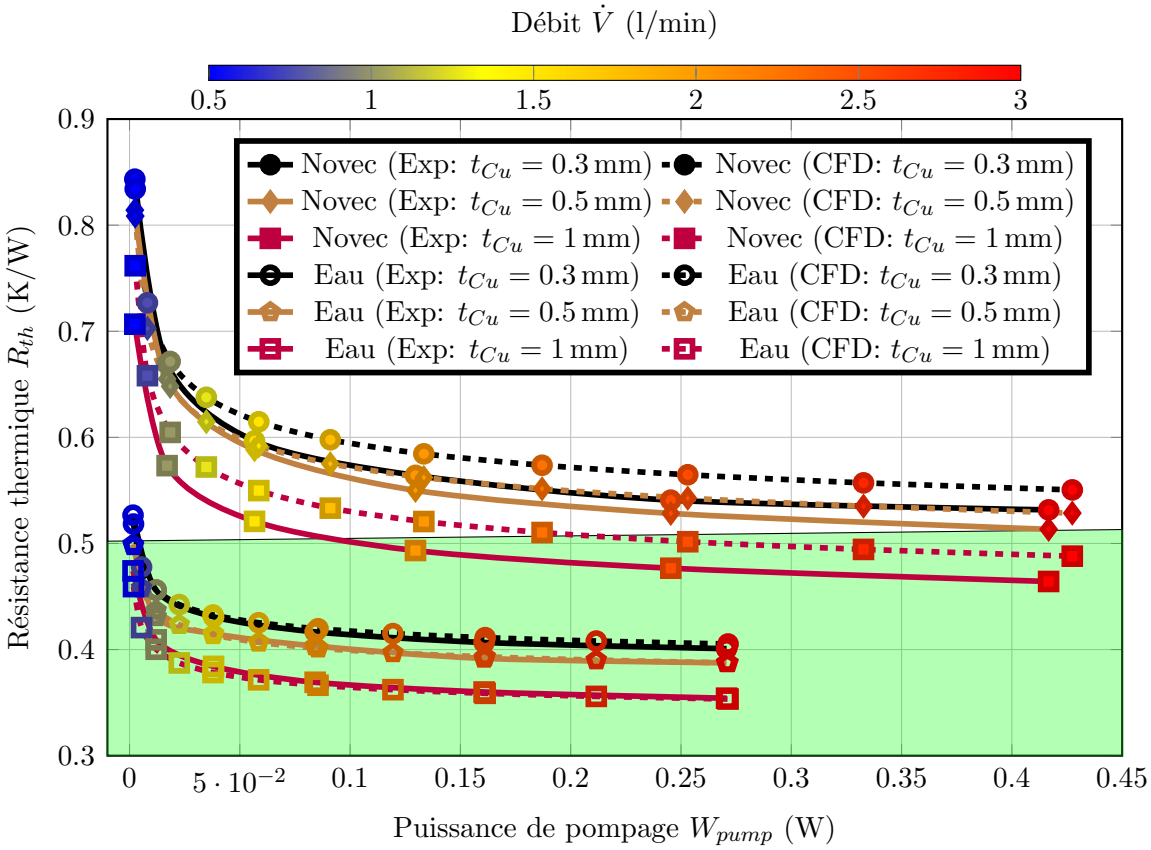


Figure 29: La résistance thermique maximale mesurée et calculée en fonction de la puissance de pompage avec Novec7500 et de l'eau comme fluides caloporteurs pour différentes épaisseurs de cuivre

réalisé une évaluation expérimentale complète des performances thermiques de ces trois refroidisseurs et avons comparé les résultats ceux des simulations CFD.

Les résultats expérimentaux correspondaient aux prédictions numériques. En particulier, nous avons observé que l'augmentation de l'épaisseur du cuivre améliorait la dissipation de chaleur et l'efficacité globale du refroidissement. Nous avons pu atteindre facilement notre résistance thermique cible de 0.5 K/W en utilisant de l'eau comme fluide de refroidissement. Bien que le fluide diélectrique Novec 7500 soit moins efficace que l'eau, l'objectif a pu être atteint en augmentant l'épaisseur de métallisation du cuivre sur les refroidisseurs en AlN. De manière remarquable, cette cible est atteignable avec une très faible puissance de pompage dans le système, spécifiquement $P_{\text{pompe}} < 500\,\text{mW}$. De plus, il est possible d'obtenir une distribution de température uniforme sur l'ensemble des trois puces.

Le tableau 2 résume les résistances thermiques obtenues grâce aux essais expérimentaux et aux simulations CFD pour les trois refroidisseurs avec des épaisseurs de cuivre de

Table 2: Résultats expérimentaux et numériques avec de l'eau comme fluide caloporteur

Débit [L/min]	0.5	1	1.5	2	2.5	3	Erreur
$R_{th,CFD}$ [K/W] (0.3 mm Cu)	0.537	0.48	0.456	0.444	0.435	0.43	2%
$R_{th,Exp}$ [K/W] (0.3 mm Cu)	0.527	0.456	0.431	0.417	0.407	0.4	
$R_{th,CFD}$ [K/W] (0.5 mm Cu)	0.528	0.47	0.447	0.434	0.426	0.42	3%
$R_{th,Exp}$ [K/W] (0.5 mm Cu)	0.5	0.431	0.415	0.403	0.392	0.388	
$R_{th,CFD}$ [K/W] (1 mm Cu)	0.489	0.431	0.41	0.397	0.39	0.384	2%
$R_{th,Exp}$ [K/W] (1 mm Cu)	0.479	0.41	0.388	0.371	0.362	0.356	

Table 3: Résultats expérimentaux et numériques avec Novec7500 comme fluide caloporteur

Débit [L/min]	0.5	1	1.5	2	2.5	3	Erreur
$R_{th,CFD}$ [K/W] (0.3 mm Cu)	0.83	0.67	0.615	0.584	0.565	0.55	2%
$R_{th,Exp}$ [K/W] (0.3 mm Cu)	0.84	0.674	0.6	0.567	0.544	0.532	
$R_{th,CFD}$ [K/W] (0.5 mm Cu)	0.809	0.648	0.592	0.562	0.543	0.529	1%
$R_{th,Exp}$ [K/W] (0.5 mm Cu)	0.814	0.655	0.588	0.55	0.528	0.513	
$R_{th,CFD}$ [K/W] (1 mm Cu)	0.762	0.605	0.55	0.52	0.502	0.488	3%
$R_{th,Exp}$ [K/W] (1 mm Cu)	0.707	0.573	0.522	0.497	0.482	0.469	

0.3 mm, 0.5 mm et 1 mm lors de l'utilisation de l'eau comme fluide de refroidissement. Pour les refroidisseurs utilisant le Novec 7500, les résistances thermiques sont résumées dans le tableau 3. Il convient de noter que l'erreur entre les résultats numériques et expérimentaux est restée à 3 % ou moins, ce qui indique un fort accord entre les deux résultats.

Conclusion et perspectives

Cette thèse apporte une contribution à la résolution des problèmes d'encapsulation des semi-conducteurs haute tension. Cette innovation offre la possibilité de réduire considérablement la taille et la complexité des modules électroniques de puissance. Les structures d'encapsulation conventionnelles ont depuis longtemps été confrontées au compromis entre l'isolation électrique, qui exige des couches isolantes épaisses, et la performance thermique optimale, qui privilégie des couches minces à haute conductivité thermique. Ce travail présente un concept novateur visant à résoudre ce dilemme en utilisant un refroidissement direct par un liquide diélectrique et des dissipateurs thermiques en céramique.

Les principales conclusions et contributions de ce travail sont les suivantes :

- Sélection du liquide diélectrique : Une évaluation approfondie a abouti à la sélection du Novec7500 en tant que liquide de refroidissement diélectrique. La haute permittivité du Novec7500, proche de celle de l'AlN, facilite une meilleure distribution du champ électrique entre ces matériaux. De plus, il présente des propriétés thermiques favorables.

- Haute tension de claquage (BDV) : L'encapsulation proposée, comprenant un dissipateur thermique en AlN et Novec7500, démontre une remarquable BDV. Avec une épaisseur d'AlN de 1.5 mm sur les deux côtés supérieur et inférieur, une BDV moyenne de 50 kV est atteinte. Notamment, en augmentant l'épaisseur de l'AlN à 3 mm, le nouveau boîtier peut supporter encore des tensions plus élevées, jusqu'à 62 kV.

- Performance thermique : l'utilisation de substrats d'AlN plus épais améliorent non seulement la BDV, mais également considérablement la performance de refroidissement.

- Simulations CFD : La simulation permet d'explorer un nombre considérable de configurations (écoulement en canal, jet impactant, nombreux paramètres géométriques des ailettes...). Les résultats expérimentaux démontrent une très grande précision des prévisions issues de la simulation.

- Conception de sous-module multi-puces : un sous-module multi-puces contenant trois puces et trois circuits d'équilibrage est conçu. Ce refroidisseur innovant intègre un mélange de broches en ligne et décalées, avec un jet central facilitant le refroidissement pour la puce centrale et le refroidissement par écoulement en canal pour les deux autres puces. Cette conception réduit au minimum les besoins en puissance de pompage et atteint des valeurs R_{th} uniformes.

- Impact de la métallisation cuivre : L'étude met en évidence l'importance de l'épaisseur de métallisation, qui améliore considérablement la performance de refroidissement en raison de sa conductivité thermique supérieure. Avec une couche de cuivre épaisse de 1 mm, l'objectif de résistance thermique est atteint même avec le Novec7500. Le refroidisseur atteint une résistivité thermique de $0.155\,\mathrm{cm^2K/W}$ avec le Novec7500, et cette valeur est encore réduite à $0.114\,\mathrm{cm^2K/W}$ avec de l'eau. Ces résultats permettent le refroidissement de dispositifs présentant des pertes de puissance allant jusqu'à $500\,\mathrm{W/cm^2}$ tout en maintenant une différence de température entre la jonction et le liquide de refroidissement de 60 °C.

Les conclusions et les méthodologies présentées ici ouvrent de nouvelles perspectives pour des modules électroniques de puissance performants, compacts et efficaces.

Perspectives

Pour garantir la sécurité des modules haute tension dépassant les 20 kV, des études supplémentaires sont encore nécessaires. Il faut en particulier approfondir les tests de tension de claquage et effectuer des mesures de décharges partielles.

En parallèle, il serait intéressant d'évaluer l'utilisation du Novec7500 à la fois en tant qu'encapsulant et liquide de refroidissement en face supérieure des puces. Cette approche offre des perspectives prometteuses pour plusieurs raisons: Premièrement, elle introduit un refroidissement des deux côtés des puces. De plus, cette approche peut avoir un impact positif sur les propriétés électriques du module. Novec7500 présente une constante diélectrique élevée, proche de celle de l'AlN, ce qui pourrait entraîner une distribution plus uniforme du champ électrique à l'intérieur du module. Cela nécessite cependant une validation expérimentale rigoureuse dans les études futures.

Part II

Thesis content

Chapter 1

Introduction

Power electronics packaging and cooling is a critical aspect of high voltage power electronics systems. As the demand for high power and energy efficiency continues to increase, the need for effective packaging and cooling solutions becomes more important to ensure reliable and safe operation. With the recent development of the silicon carbide (SiC) technology, higher voltage (10 kV and more) power devices become possible. These systems generate a significant amount of heat during operation, which can cause performance degradation, component failure, and safety issues if not properly managed. Therefore, the design and implementation of effective packaging and cooling solutions are essential to ensure the longevity and optimal performance of high voltage power electronics systems. This work investigates a packaging solution for high voltage semiconductors (20 kV), allowing for a dramatic reduction in size and complexity of power electronics modules.

This introductory chapter starts with a motivation for high voltage modules, focusing on high voltage direct current (HVDC) transmission. It then highlights the objective of the thesis and the challenges associated with the development of effective housing and cooling solutions for high-voltage power electronic systems.

1.1 Motivation

Electricity is indispensable, as almost every aspect of modern life depends on it. A transmission network is required to move electricity across a country. Today's alternating current (AC) networks, which are operated with a frequency of 50 Hz or 60 Hz, dominate in the transmission of electrical energy. However, recent improvements in the field of semiconductor devices enable efficient direct current (DC) electric power transmission to be used instead of AC. Indeed, DC transmission is more efficient over long distances, as we will see below.

Generally, high voltage (HV) is required over long distances to reduce power losses. The power loss P_{loss} is mainly caused by Joule effect, and is the product of the ohmic line

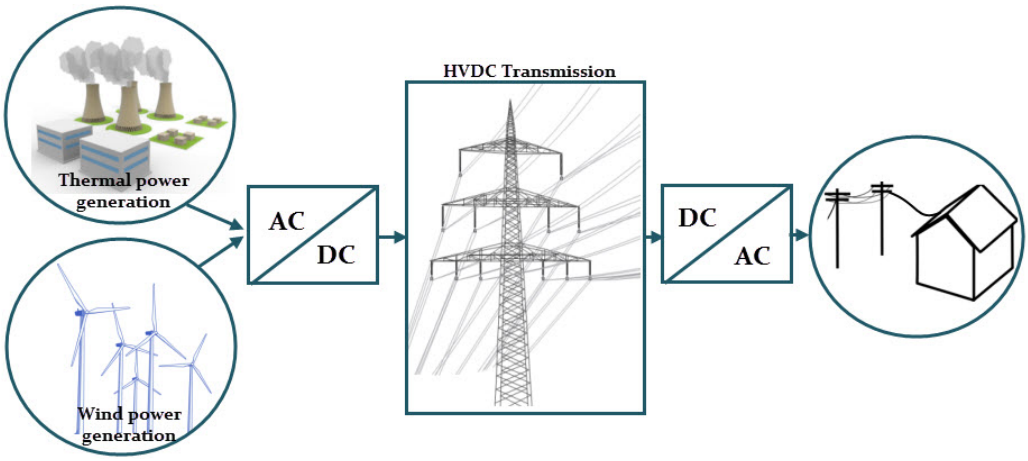


Figure 1.1: HVDC power system: converter station, transmission portion and an inverter station [1]

resistance (R) and the line current I squared ($P_{loss} = R \cdot I^2$). Therefore, transferring the same active power ($P_{active} = I \cdot V$) using a higher voltage V (and consequently a lower current I) leads to lower power losses.

The main disadvantages of high voltage alternating current (HVAC) systems are the reactive power circulation and skin effect [5]. None of these occur with high voltage direct current (HVDC), which leads to lower power losses in the line. In addition, HVDC has better power transmission capability due to isolation ratings: the HVAC cables are designed for the maximum peak voltage, which is larger than its effective value (Root Mean Square, RMS). RMS values actually dictate the power transfer level. In consequence, an HVAC tower (pylon) can be used for HVDC with 73 % higher voltage rating without altering its structure [6]. This results in a threefold increase in power flow since an HVDC line only uses two sets of insulated conductors instead of three in an HVAC line [7].

However, compared with HVAC, HVDC lines require conversion stations at their ends, to connect to the AC transmission grid. A converter station (AC/DC) is required to convert AC power to HVDC power prior to transmission. At the end of the HVDC transmission line, an inverter station (DC/AC) is needed to convert the HVDC into AC power that is distributed to the end user. Figure 1.1 illustrates the HVDC power system from the generator station to the end user.

A case study [2] compares the cost of HVDC and HVAC transmission systems. It is found that for the longest transmission lines (more than 700 km), HVAC transmission is more expensive than HVDC transmission with the same transmission capacity. For such long transmission systems, the lower cost of the line in HVDC compensates the cost of the conversion stations. Figure 1.2 illustrates a comparison of the costs of HVAC and HVDC found in [2].

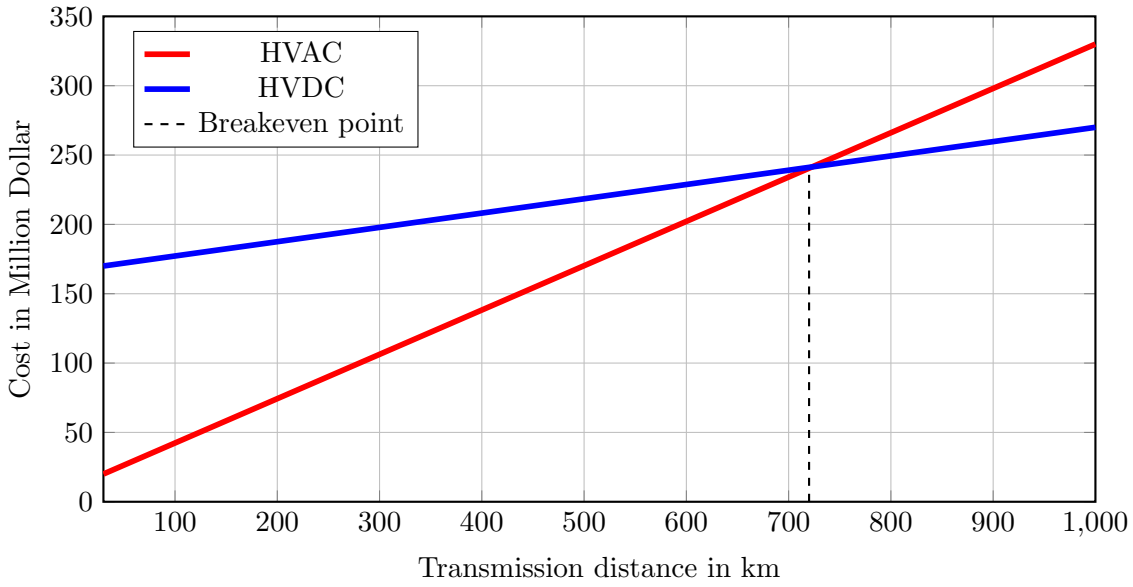


Figure 1.2: Distance versus cost for HVAC and HVDC transmission lines

Figure 1.3 shows the photograph of an HVDC converter station from the company ABB [3]. HVDC converter stations are based on 3.3 kV IGBTs, single switch or half-bridge modules. The converter is a huge system comprising hundreds of IGBT modules. Increasing the voltage ratings of power modules from 3.3 kV to 20 kV would lead to a dramatic reduction in the number of modules. As a result, much less insulating materials, cables, insulation, potting materials and coolants would be needed to manage the modules. The converter station would become much smaller, resulting in lower costs and footprint. However, it is a challenge to insulate such high voltage modules. In addition, higher power dissipation densities are generated. Therefore, an advanced cooling structure is required to keep the module below critical temperatures. This work aims at combining cooling and insulation by using a dielectric liquid, both as a coolant and as an insulator, providing improved thermal management and electrical insulation performance at the same time.

Why cooling ?

Temperature is one of the critical factors affecting the reliability of power electronics systems. High operating temperatures can degrade electronic components, and in severe cases can lead to complete system failure. The reliability of power electronics systems is a significant concern, particularly in high power applications such as HVDC conversion, where these systems are expected to operate continuously for tens of years. The increase in power density in these systems have led to higher operating temperatures, which further exacerbates the reliability challenges. Therefore, proper thermal management is crucial to ensure the long-term reliability and performance of power electronics systems.

The failure of a semiconductor device in a power module leads to direct and conse-

Figure 1.3: An HVDC converter station [3]

quential damage, which incurs high costs. Temperature increase is the main cause for the failure of these components. These cause over 55% of electrical devices failure [8], see figure 1.4. Therefore, efficient cooling is of utmost importance in power electronics.

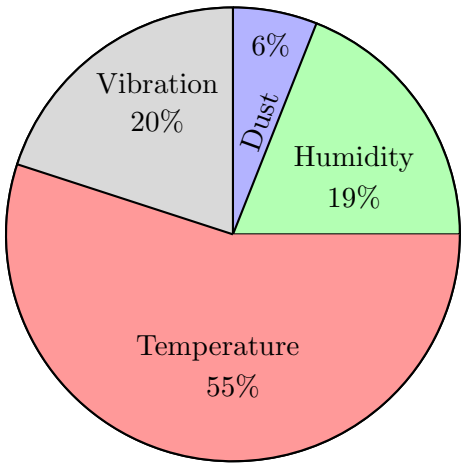


Figure 1.4: Major failure causes of electronics devices (data from [8])

1.2 Objective of the thesis

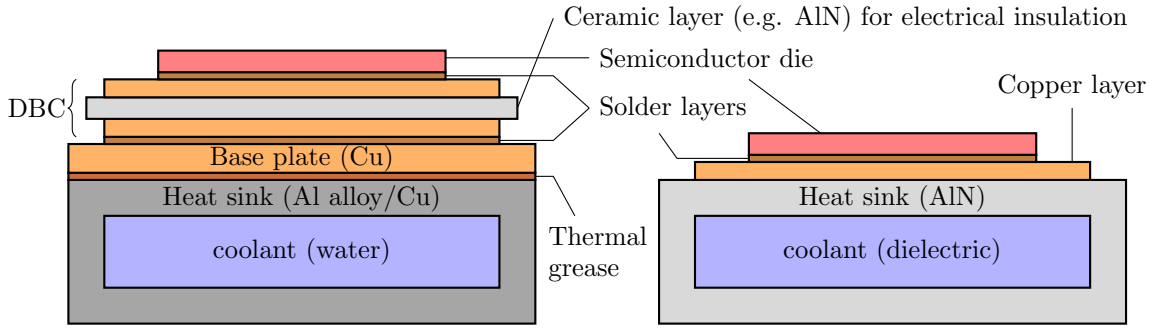
This work investigates a packaging solution for high-voltage power electronics (20 kV). The novel packaging structure is simpler, having fewer layers of materials, and has good electrical and thermal properties (quantified metrics are given further below). The main purpose of the work is to optimize the cooling performance of the integrated heat sink. Detailing further, this requires the following steps:

- Selection of dielectric coolants
- Design and optimization of the integrated heat sink for operation with the dielectric liquid cooling, with the objective of achieving both low thermal resistance (R_{th}) and low hydraulic losses in the cooling circuit.
- Ensuring uniform cooling in multi-chip module (i.e. minimizing R_{th} spread from chip to chip).
- Experimental validation of the design on a prototype.

This thesis constitutes the first use of a dielectric liquid in combination with integrated ceramic heat sinks: most heatsinks are made out of metal (typically aluminium or copper), and may be associated with deionized water cooling when electrical isolation is required; occasionally, ceramic heatsinks are used to ensure electrical isolation, in which case no special care is given to electrical properties of the cooling fluid.

1.2.1 Integrated cooling system

Figure 5.26 shows a comparison between the traditional power module structure and this work's proposed integrated packaging. The traditional power module structure (figure 5.26a) comprises many layers of materials, which degrade the cooling efficiency as they lengthen the path between dies and cold source (heat sink). In such packaging structure, the chip is soldered onto a Direct Bonded Substrate (DBC). The DBC's copper layers conduct both heat and current, while the ceramic layer provides electrical insulation and heat conduction. The ceramic layer of the DBC has a limited thickness (typically 1mm or less), which limits the maximum isolation strength). Additionally, the DBC structure introduces parasitic package capacitances that degrade the switching performance of high voltage power devices and increase their power losses. For greater mechanical strength and better heat distribution, the DBC is attached to a thick metal baseplate (typically copper or an aluminium-silicon carbide composite) that is screwed onto a water-cooled cold plate through a layer of thermal interface material (TIM). Typically, TIM materials have low thermal conductivity (lower than 5 W/mK), which affects the overall thermal performance.



(a) Traditional module packaging (b) Novel embedded packaging

Figure 1.5: Schematic comparison between the traditional and the novel power module packaging

The proposed structure (figure 5.26b) integrates the liquid cooling plate directly into the ceramic layer. This structure reduces the number of material layers of the module. A dielectric fluid is used as both a coolant and an electrical insulator to relieve some of the constraint of the solid insulation layers, and a ceramic structure provides mechanical support, internal insulation and heat exchange surface. The novel embedded packaging structure offers the following advantages over the traditional packaging:

1. Dramatic reduction in size, material count and complexity of the packaging.
2. Higher electrical insulating ability can be achieved because the dielectric liquid and the ceramic heatsink participate to the electrical insulation.
3. Significant reduction in the thermal path from the semiconductor device to the heat conductor, resulting in better thermal performance.
4. Reduction of the parasitic capacitance of the package, which is an attractive feature for high voltage semiconductors.

1.3 ARCHIVE project overview

This thesis work is a part of the international project ARCHIVE (ARchitecture Ceramic for HIgh Voltage power Electronics). ARCHIVE aims at demonstrating a breakthrough power electronics module technology for 20 kV semiconductor devices. It addresses both electrical insulation and thermal management. The technical solutions investigated in ARCHIVE are based on an advanced ceramic substrate, with specific features on the top-side, designed to limit the reinforcement of electrical field observed in standard substrates, and an innovative cooling approach on the backside, which distributes the electrical insulation between the ceramic and the dielectric fluid.

Two companies and two academic research groups are involved in the ARCHIVE consortium:

- LAPLACE (Toulouse, France): design of innovative topside structures for metallized ceramic substrates to improve their electrical strength.
- CeramTec (Marktredwitz, Germany): manufacturing of the ceramic parts.
- Kempten University of Applied Science (Kempten, Germany): design and optimization of the cooling structures.
- SuperGrid Institute (Villeurbanne, France): design of a 20 kV power module including the ceramic parts and module-level testing (electrical and thermal).

1.4 Thesis outline

This work contains the flollowing chapters:

Chapter 2 gives an overview of the state-of-the-art on power electronics packaging. It details the packaging structure of different packaging introduced in the literature and compares them to the novel structure proposed in this work. Furthermore, this chapter reviews cooling methods and different ways for improving the cooling performance. At the end, the chapter summarises and discusses the cooling performance of different results from the literature.

Chapter 3 addresses the materials used in the thesis, providing an overview of the solid layers in the package and the coolants used, with a focus on their thermal and dielectric properties. It includes a systematic evaluation of the cooling fluid candidates to identify the most suitable ones. The chapter aims at selecting the ideal coolant based on its performance and compatibility with system requirements.

Chapter 4 is the "methods" chapter in the thesis. It begins by exploring the theoretical aspects of heat transfer mechanisms to establish a foundation for understanding the cooling aspects. It then exposes the specific methods utilized in this work. The chapter delves into the necessary methods for conducting Computational Fluid Dynamics (CFD) simulations, covering essential aspects such as meshing and boundary conditions. Additionally, it outlines the various methodologies employed to determine thermal resistances, providing detailed explanations for each approach. Finally, the chapter presents the measurement methods employed to gauge thermal resistance, pressure drop, and flow rates.

Before going in depth with a complex multi-dies module, **Chapter 5** introduces a simple, single-chip module. This reduces the complexity of the module and allows for a better understanding of the package and the cooler. An optimization process is carried out

for the single chip module structure. The built-in pins are optimized by changing different design parameters. Then, one-die modules are manufactured for the experimental test. Finally, the CFD and experimental results are compared and discussed.

Chapter 6 introduces the multi-chip module with all needed components. The CFD results of the single chip device are used here and extended for the multi-chips module. After CFD optimization of the cooler, test vehicles are manufactured. Experimental test are carried out and compared with the CFD results.

Chapter 7 gives a general conclusion of the thesis and all important results. It summarize the scientific contributions and perspectives drawn from the thesis.

Chapter 2

Literature review

This chapter presents an overview of the cooling and packaging of power electronics. The chapter begins with an introduction to high voltage power electronics, highlighting their significance in various applications. Subsequently, the chapter discusses different packaging structures found in the literature. The various package designs and materials used in power electronics are explored. The chapter then focuses on cooling issues. Various cooling techniques, are analyzed in terms of their effectiveness in removing the heat generated by power electronics. The concept behind the cooling designs is explored, along with the design considerations for heat sinks, including material selection and design optimization. Finally, the chapter concludes with a summary of the key findings from the literature review.

2.1 High voltage power electronics

High voltage power electronics have been extensively used in various applications, including renewable energy systems, railways, and smart grids. The development of high voltage ($> 6.5\,\mathrm{kV}$) power semiconductor devices has been a challenging task due to the limitations of conventional Silicon (Si) technology. However, with the recent advancements in Silicon Carbide (SiC) technology, high voltage power semiconductor devices rated at $10\,\mathrm{kV}$ and more [9, 10] have become possible.

The development of high voltage SiC power semiconductor devices has been investigated extensively in recent years. For instance, a survey of wide bandgap power semiconductor devices by Millan et al. [11] shows that SiC has much better thermal and electrical properties than Si. SiC has around ten-fold higher critical electric field strength compared to Si. Beside that, SiC has better switching speeds, lower conduction losses and about ten times higher blocking voltage compared to conventional Si-based devices [12, 13, 14]. SiC devices could work with higher current density and the thermal conductivity of SiC ($490\,\mathrm{W/mK}$) is three times higher than that of Si ($150\,\mathrm{W/mK}$) [15, 16]. These permit to

reduce the size and weight of the semiconductor devices as well as minimizing the volume of their associated cooling systems.

Several references show that high voltage power devices can be achieved with SiC technology. For example, Raynaud et al. [17] discusses SiC power devices with rated from 6.5 kV up to 50 kV. Kimoto [18] analyze, both numerically and experimentally, ultra-high voltage SiC devices ($> 10\,\text{kV}$). He shows up to 30 kV SiC has attractive performance, with good carrier lifetime and low on-resistance. Furthermore, a numerical study by Jiang et al. [19, 20] analyzes the DC and AC properties of SiC MOSFETs numerically. This shows that the static and switching performance of SiC MOSFETs could be improved by changing the gate structures, allowing for even better results than traditional SiC devices. G. Walden et al. [21] optimize a 10 kV SiC DMOSFET for minimal forward voltage drop in the on-state. This optimized device enables power modules for high-frequency ($> 20\,\text{kHz}$) megawatt power conversion. A low on-state resistance R_{on} of about $250\,\text{m}\Omega$ at 100 °C is measured. Howell et al. [22] demonstrate a performance subthreshold characteristics of 10 kV DMOSFET in temperature range of 25 °C to 200 °C showing a low off-state leackage current of $0.4\,\mu\text{A}$ at 200 °C. Furthermore, resistive and inductive switching tests of 20 kV SiC IGBT with 20 A is demonstrated in [23]. The turn-on and turn-off curves are measured as a function of the temperature from 25 °C to 150 °C.

The on-state resistance of power devices, R_{on} depends strongly on the materials and breakdown voltage. SiC allows much higher breakdown voltages than Si [24, 25]. Figure 2.1 shows the specific on-resistance (R_{on}/A) as a function of the rated breakdown voltage for Si and SiC.

The literature shows that R_{on} also increases with the temperature [26, 27]. Consequently, the corresponding power losses increase dramatically with the junction temperature. The conduction losses of 3.3 kV and 10 kV SiC MOSFETs could be calculated as follow:

$$P_{loss}(10\,\text{kV}) = R_{DS}(T_j) \times I_D^2 = R_{on}(25\,^\circ\text{C}) \times \left(\frac{T_j}{398.15\,\text{K}}\right)^{2.5} \times I_D^2 \quad [26] \tag{2.1}$$

$$P_{loss}(3.3\,\text{kV}) = R_{DS}(T_j) \times I_D^2 = R_{on}(25\,^\circ\text{C}) \times \left(\frac{T_j}{398.15\,\text{K}}\right)^{2.42} \times I_D^2 \quad [27] \tag{2.2}$$

Therefore, efficient cooling is needed to maintain R_{on} at an acceptable value, by keeping the junction temperature T_j of power devices low. This requires suitable packaging as well as an advanced thermal management system.

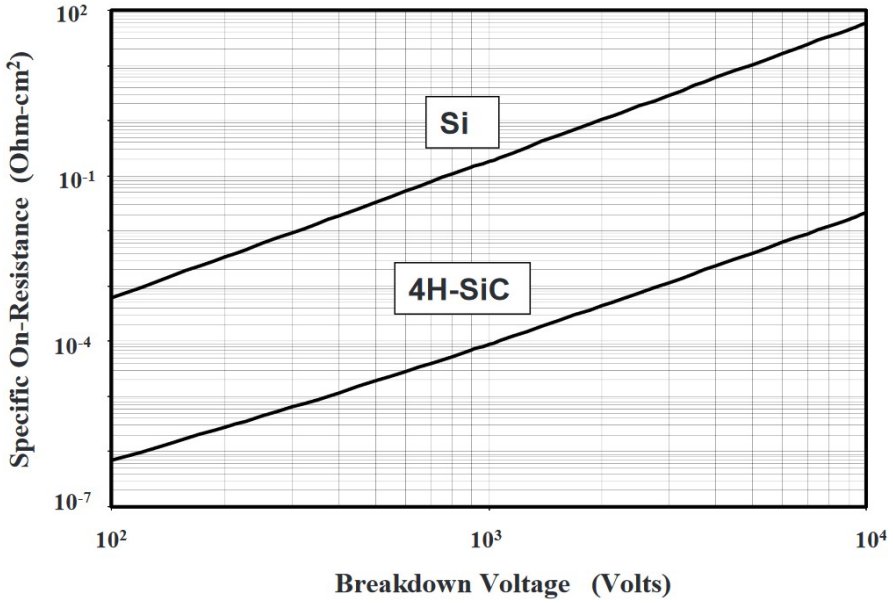


Figure 2.1: Typically on-resistance as a function of breakdown voltage for Si and 4H-SiC power devices [24]

2.2 Packaging of power electronics

Packaging is an essential aspect of the design of power devices. It is crucial to the performance, reliability, and safety of power electronic systems. A typical package for power electronics, as shown in Figure 2.2, consists of more than just the semiconductor device. It includes additional materials and components that play important roles. To begin with, a substrate is utilized in the package to provide mechanical support and electrical insulation to the bottom side. Interconnects, such as wire bonds, solder joints, or conductive traces on a printed circuit board (PCB), establish electrical connections between the power electronic devices and other components within the package. To address the issue of excess heat generated during operation, heat sinks are employed to dissipate the heat efficiently. These heat sinks help maintain the temperature of the power electronic devices within acceptable limits. Furthermore, an encapsulation material, often in the form of a gel or resin, is used to protect the power electronic devices from environmental factors like moisture, dust, and vibrations, and to provide electrical insulation. In addition to these components, the power electronic package incorporates various electrical connections to the external world. These include power input/output terminals, control signal inputs, and communication interfaces. These electrical connections enable the integration of the packaged device into larger electrical systems.

The main purpose of power electronics packaging can be summarized as follows:

- Protection: Power electronics packaging provides physical protection to the sensitive

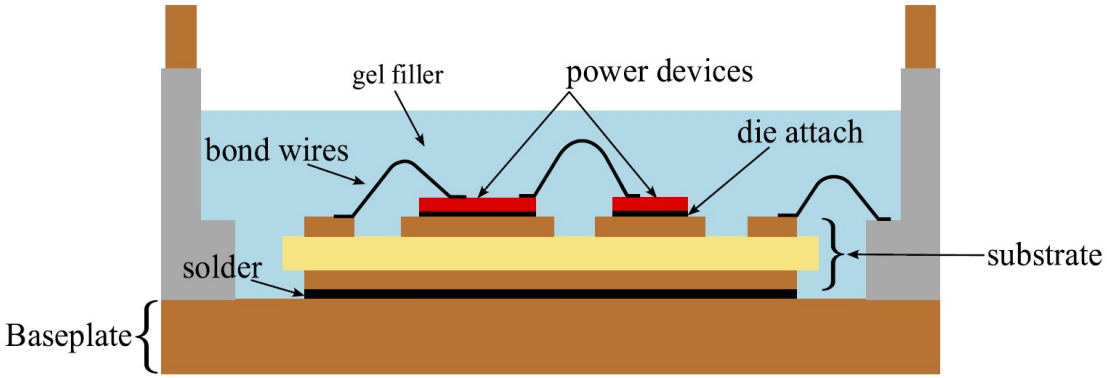


Figure 2.2: Conventional packaging of power electronics [28]

electronic components from external mechanical stresses, temperature variations, humidity, and other environmental factors. It helps to ensure the reliability and longevity of the power electronic system.

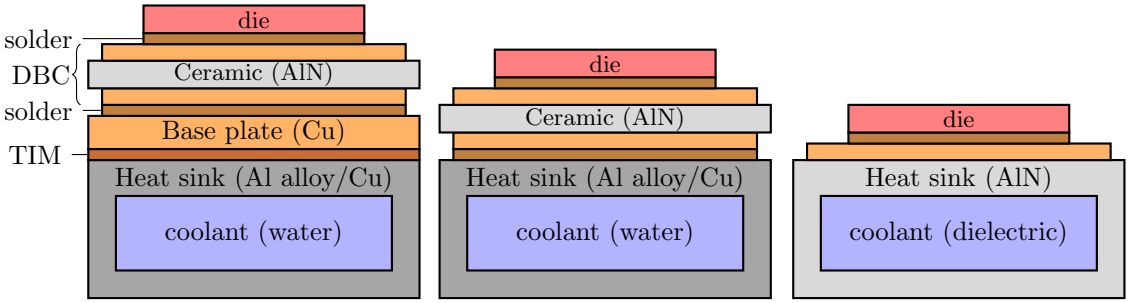
- Thermal Management: Power electronic devices generate significant heat during their operation. Effective power electronics packaging incorporates heat dissipation mechanisms, such as heat sinks, thermal interface materials, and cooling channel, to efficiently remove heat and maintain the operating temperature within acceptable limits. Proper thermal management enhances the performance and reliability of power electronic devices.

- Electrical Isolation: Power electronics packaging includes electrical isolation barriers to ensure the safety of users and separate high-voltage and low-voltage sections of the circuit. On the top side of the chips, the insulation is ensured through an encapsulant, while a substrate (e.g. AlN) provides the insulation to the bottom side.

- Interconnectivity: Power electronics packaging facilitates the interconnection of various components within the system. It includes the design and integration of power and control interconnects to ensure reliable electrical connections and efficient signal transfer.

- Size and Weight Optimization: Power electronics packaging aims to minimize the size and weight of the overall system without compromising its performance. Compact and lightweight packaging enables easy integration into space-constrained applications, such as automotive, aerospace, or portable electronic devices.

- Manufacturability and Cost-Effectiveness: Power electronics packaging is designed to be manufacturable at a large scale with high yield and low cost. This includes



(a) Traditional structure (b) state-of-the-art structure (c) novel proposed sructure

Figure 2.3: Schematic comparison between the traditional and the novel power module packaging

factors such as material selection, assembly processes, and testing methods to achieve efficient manufacturing and cost-effective production.

- Reliability and Serviceability: Power electronics packaging is designed to ensure the reliability and serviceability of the system. It includes features like fault detection and protection mechanisms, modular designs for easy replacement of faulty components, and diagnostic capabilities to identify and troubleshoot issues.

The packaging structure of the module strongly influences its electrical and thermal properties. Therefore, various module structures have been reported in the literature, and much effort is being made to improve the packaging of semiconductor devices.

While most research studies focus on the high voltage semiconductor devices themselves, their packaging also presents some technical challenges, particularly regarding electrical insulation and thermal management. In traditional high voltage packages, a thick solid layer (typically aluminium nitride ceramic) is required for the electrical insulation, which degrades the cooling performance (for which a thin ceramic layer would be preferable). In general, liquid cooling solution can be classified into three structures, as shown in figure 2.3. The figure only considers the thermal path from chip to coolant within the package.

Figure 2.3a shows the traditional packaging, consisting of seven layers between chip and heat sink. These are a metalized ceramic substrate (Direct Bonded Copper – DBC –, three layers), two layers of solder at the interfaces, a base plate placed between the DBC and the heat sink and a thermal interface material (TIM) to attach the base plate to the heat sink. Before moving to the other packaging structures, the following is an overview of the important solid layers:

- **Direct bonded copper (DBC)** is a technology used in power electronics packaging to provide a low thermal resistance and high electrical isolation path between a semiconductor device and a heat sink. It involves bonding a layer of copper to

a ceramic substrate, such as aluminum oxide (Al_2O_3), Beryllium Oxide (BeO) or aluminum nitride (AlN), using a high-temperature process. The DBC substrate typically has a thickness of 0.3 mm-0.7 mm and a copper layer thickness of 0.125 µm-0.7 µm [29]. The copper layer acts as a heat spreader, allowing heat to be dissipated more efficiently from the semiconductor device to the heat sink. The ceramic substrate provides electrical isolation between the semiconductor device and the heat sink. Many studies [30, 31, 32, 33] investigate DBC technology and study different ceramic substrates. The studies show that AlN has lower thermal resistance than other substrates such as Al_2O_3 [29, 30]. This is due to high thermal conductivity of the AlN ($\sim 170\,W/mK$) In addition, AlN offers a close match in CTE to Si and SiC as well as good thermal stability [34].

Despite the many advantages of Direct Bond Copper (DBC) in power electronics packaging, there are also some disadvantages that should be considered. DBC is generally expensive due to the additional manufacturing steps required to bond the copper layer to the ceramic substrate. Beside that, DBC has limited thickness due to the manufacturing process, which can limit its use in high voltage applications. DBC also has a lower coefficient of thermal expansion (CTE) than copper, which can lead to thermal stress and cracking over time.

Some Publications [35, 36, 37] investigate DBA (direct bonded aluminium) instead of DBC in power electronics packaging. The studies show that the the thermal stability of DBA is better than DBC for the applications in high-power electronics [37]. DBA has significantly higher thermo-cycling capability lifetime compared to DBC [35]. However, the disadvantage of the DBA is the low thermal conductivity of the aluminium results in degradation of the cooling performance of the package.

- **The base plate** is a metal plate that forms the bottom of a power module. It is typically made of copper or aluminum, and it serves several important functions in the package. First, the base plate provides mechanical support and stability to the semiconductor devices and other components within the package. A base plate provides a convenient surface for attaching the power device and other components, making assembly and manufacturing processes more efficient. It also helps to protect the devices from mechanical stress and vibration during operation and handling. However, a base plate adds extra weight and volume to the packaging and requires additional materials and manufacturing processes, which can add to the overall cost of the packaging [38, 39]. Beside that, the base plate increases the thermal path from the semiconductor device to the heat sink, which affects the thermal performance of the packaging. This is critical in high-power applications where efficient heat dissipation is required to prevent overheating and damage to the devices.

- **Soldering/sintering materials** play a crucial role in power electronics packaging. Solders have good thermal and electrical properties. They are used to join the DBC onto the base plate. They can also be used to attach the semiconductor die to the DBC and provides electrical and thermal connections between the die and the package. There are several different types of solder materials investigated in the scientific literature (eg. [40, 41, 42, 43]. Several publications [44, 45, 46] use soldering processes to attach semiconductor devices onto the DBC.

  Die sintering is an alternative to traditional soldering for attaching a semiconductor die to a substrate in power electronics packaging. Instead of using solder, a layer of metal powder with micrometer or nanometer-sized particles is deposited on the die or substrate surfaces. Then the two surfaces are pressed together and heated to form a solid metallurgical bond thanks to solid diffusion mechanisms. The die sintering process is applicable to various materials such as silver, copper, aluminum, and nickel. Die sintering has several advantages over traditional soldering. First, it can provide a more reliable and robust connection, as the metallurgical bond between the die and substrate is stronger than a solder joint. This can improve the thermal and electrical performance of the package, as well as its long-term reliability. Second, die sintering can be used with a wider range of materials, including those that are difficult to solder, such as silicon carbide (SiC) and gallium nitride (GaN) [47]. However, die sintering also presents some challenges. The process requires high temperatures and pressures, which can cause thermal and mechanical stress on the die and substrate. This can lead to cracking or delamination of the materials, especially if they have different coefficients of thermal expansion. In addition, the die sintering process can be more expensive and complex than traditional soldering, as it requires specialized equipment and expertise. Sintering process is studied and in the literature [48, 49, 50] and may soon replace lead-based solders as the standard attachment technology for semiconductor devices, especially SiC dies [51].

- **Thermal inteface material (TIM)** is used to improve the thermal transfer between two surfaces. In power electronics, TIM is mostly used to improve the thermal conduction between the base plate and the heat sink. The TIM fills in the microscopic gaps between the two surfaces, reducing the thermal resistance and allowing heat to flow more efficiently from the device to the heat sink. However, TIM has normally a relatively low thermal conductivity ($< 5\,\mathrm{W/mK}$) compared to other solid layers. Therefore, removing or replacing the TIM with other layer (e.g. solder material) could improve the heat dissipation from the die to the heat sink. In addition, some types of TIM can degrade over time due to exposure to high temperatures, humidity, or other environmental factors. This can lead to increased thermal resistance

and reduced performance of the power electronics system.

There are many types of TIM available, including greases, adhesives, and tapes, each with different thermal and mechanical properties. Different types of TIM are investigated and compared in the literature [52, 53, 54]. The choice of a TIM depends on the specific application and requirements of the power electronics system.

The conventional packaging (2.3a) exhibits low mechanical reliability due to its many layers (and interfaces) and CTE mismatches between the different materials in the package. Additionally, this complexity makes the thermal path longer, and thermally less efficient. Figure 2.3b shows a more advanced solution. This structure integrate the base plate and the heat sink into one single part, removing two layers (a base plate and a layer joint). Different studies are performed to improve the mechanical and thermal performance and reduce the layer count (e.g. [55, 56, 57]). For example a study by Morozumi et al. [56] shows a better cooling performance when using fewer layers. A study by Hitachi et al. [57] shows that the thermal resistance is reduced by 30 % using a heat sink structure integrated into the base plate (2.3b) compared with the traditional structure. The reason behind that is the elimination the TIM material, which has a low thermal conductivity and of the base plate, resulting in shorter heat path to the heat sink.

Mouawad [58] and Johnson [59] introduced a packaging (figure 2.3b) technology for a highly integrated 10 kV SiC MOSFET module which addresses both the insulation constraint and the thermal management. The module uses stacked DBA (Direct Bonded Aluminium) substrates (selected for their high thermal-cycling capability) to provide a more uniform electric field distribution. The integrated structures reduces the parasitic inductances and capacitances in the module and also offers a good thermal performance.

To have better CTE matching between the base plate and the ceramic substrate, a Metal Matrix Composite (MMC) is introduced by Romero et al. [55]. The MMC material (AlSiC) has a low CTE (6.8 ppm/°C) compared to that of copper (17 ppm/°C), while the AlN ceramic substrate has a CTE of 4.5 ppm/°C and 6.7 ppm/°C for Alumina substrate. The MMC package allowed the integration of the base plate and the heat sink into one piece part. This approach removes two layers (a base plate and a layer joint). With better match of the CTE and package integration, the module provides a better reliability compared to a copper base plate and traditional packaging. The disadvantage of this package is the high cost of MMC material. Additionally MMC material (AlSiC) has lower thermal conductivity affecting the heat dissipation from the semiconductor devices. AlSiC has a thermal conductivity of 180 W/mK compared to 393 W/mK for copper [55].

A metalized ZBC substrate (ultra-thin Zirconia Bonded Copper) can be used instead of DBC, as introduced by Zhao et.al [60]. 20 µm and 40 µm thick ZBC substrate are investigated. It is found that thicker dielectric substrate reduces the parasitic capacitance of the package. The main disadvantage of standard DBC substrates for high voltage

applications is the occurrence of partial discharges at relatively low voltages [61]. To solve this problem Schulz-Harder and Exel [61] introduce an improved etching technology and an advanced DBC with an AlN layer to be used in high voltage applications. Ling Xu et al. [62] and Zhang et al. [63] present a novel integrated base package (IBP) by removing the bottom copper of the DBC and attaching the substrate (AlN) directly onto an AlSiC base plate. Therefore, a solder and a copper layer are removed, thus enhancing module reliability by reducing solder crack possibilities. Also thermal fatigue is reduced, as AlSiC base plate and ceramic layer (AlN) have matching CTEs.

The DBC (and its bonding process) is a main cause of the thermal fatigue and reduction of power cycling capability, which affects the reliability and lifespan of the module [64, 65]. Additionally, the DBC is a source of parasitic capacitance in the module. This is due to the metal-insulator-metal (Cu-AlN-Cu) structure, which forms a plane capacitor. The parasitic capacitances charge and discharge during every switching transient. This slows down both turn-on and turn-off transient and can cause significant increase in switching energy losses and electromagnetic interference issues in the module [66, 67]. Several publications investigate the thermo-mechanical reliability [68, 69, 70] and the parasitic capacitances [71, 72, 73] of package structures.

While most of these publications try to improve the packaging structure through optimization the DBC material and its layer thicknesses, this work removes these layers (DBC and solder layers) altogether. Figure 2.3c shows the integrated package structure, with just three layers between the die and heat sink. The die is sintered on a copper plate for electrical connections and heat spreading. The copper is soldered (or metal brazed) onto the AlN heat sink. The AlN heat sink provides electrical insulation and heat removal for heat dissipation from the die using the advantage of its high thermal conductivity. This approach eliminates the parasitic capacitances, potentially resulting in a reduction of switching losses and electromagnetic interference issues. The novel integrated package could have a better reliability thanks to its lower material count. Integrating the liquid cold-plate directly in the ceramic layer results in a dramatic reduction in size and complexity of the thermal path, which can lead to a better cooling performance. Additionally, the thickness of AlN substrate in the proposed package can be very thick (which is limited in DBC structure) allowing the use in very high voltage power electronics ($> 20\,\mathrm{kV}$). Furthermore, using a dielectric coolant instead of water or water/glycol mixture allows the coolant to take a part in the insulation process.

2.3 Power electronics cooling methods

Various cooling methods are available for power electronics and the choice of cooling method depends on the application, performance level and cost. Some of the most com-

monly used cooling methods are:

1. Air Cooling: This is the most common and cost-effective cooling method for power electronics. This method may use a fan or blower to force air circulation over the heat sink to dissipate heat. Air cooling is suitable for low to medium power applications. The limitation of forced air cooling with different sink materials is examined in [74].

2. Liquid Cooling: Liquid cooling is a more efficient cooling method than air cooling and is suitable for high power applications. In this process, a liquid is circulated through a heat sink to absorb heat. The liquid can be water or a dielectric liquid such as oil or synthetic liquids.

3. Phase Change Cooling, or two-phase cooling, is a high performance cooling method that uses a refrigerant to absorb heat. In this process, the refrigerant absorbs heat and changes its physical state from liquid to gas. The gas then condenses back into a liquid at a second heat exchanger and releases the heat in the process. Criscuolo et al. [75] examine this concept for cooling power electronics and compared it with other references. A comparison between single-phase and two-phase cooling is shown in [76]. Heat pipes are another category of phase-change systems. These are passive heat transfer devices that use a closed loop, phase change system to transfer heat from the heat source to the heat sink. This cooling concept is explained in various references (e.g. [77, 78]) and is also used in power electronics cooling (e.g. [79, 80]).

4. Thermoelectric Cooling uses the Peltier effect to cool devices. In this method, a thermoelectric module is used to create a temperature difference between the heat source and heat sink, resulting in cooling of the device. For more details, [81] examines the cooling performance of this cooling method.

5. Immersion cooling: The power electronics are immersed in a dielectric liquid such as oil or synthetic liquids. The liquid absorbs heat and is circulated through a heat exchanger to remove the heat. This cooling technique is examined in the literature (e.g. [82, 83]).

Each cooling concept has advantages and disadvantages, and the choice of cooling method depends on the specific application and performance requirements. Different cooling methods could also be combined in order to cool the semiconductor components. In this work, a high heat density is generated in the SiC components. Therefore, a high-efficiency cooling method is chosen for the cooling. Liquid and two-phase cooling have the best cooling performance. Since there are no details on how the dielectric properties change between the vapour and liquid phases, a two-phase cooling system is not suitable

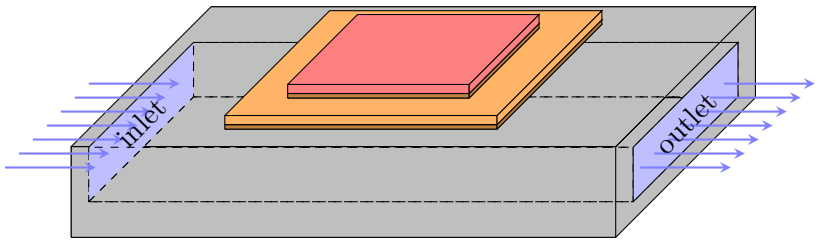


Figure 2.4: Channel-flow cooling concept

for the purpose of this work. Therefore, a single phase liquid coolant is preferred here for the cooling system of the high voltage module.

The flow pattern of the fluid changes the cooling performance. In general, there are two common liquid cooling concepts used in power electronics. These are microchannel (or minichannel) and jet impingement concepts. These two cooling concepts and their structure are explained in the following.

2.3.1 Channel flow

In channel flow cooling, the coolant flows through channels in the heat sink or cold plate. The coolant absorbs heat as it flows through the channels, and the heated coolant is then delivered to a secondary heat exchanger. In general, the heat sink has a simple structure. The coolant enters on the one side ("inlet"), flows to the channel and exits the other side ("outlet"). A channel flow concept is shown in figure 2.4 with an inlet on the left and an outlet on the right while a heat source (semiconductor) is placed on top of the channel.

Channel flow can be effective at removing heat from larger heat sources [84] such as power modules and inverters with large semiconductor devices. It also tends to provide more uniform cooling over a large area compared other methods. However, channel flow may not be as effective at removing heat from small, high power density components, and the channels may be more complex to design and manufacture. Microchannel flow is a well-known cooling concept in power electronics. Microchannels are small channels with hydraulic diameters in the range of several hundred micrometers to millimeters.

2.3.2 Jet impingement

In jet impingement cooling, high velocity jets of coolant are directed at the heat source, typically through a nozzle or array of nozzles. The jets hit the heat source directly, creating a high heat transfer rate and a thin coolant boundary layer. The boundary layer is constantly replenished by the flow of coolant, which increases the rate of heat transfer. Jet impingement can help remove heat from small, high-power-density components effectively. However, it can be difficult to achieve uniform cooling across a large heat source [84].

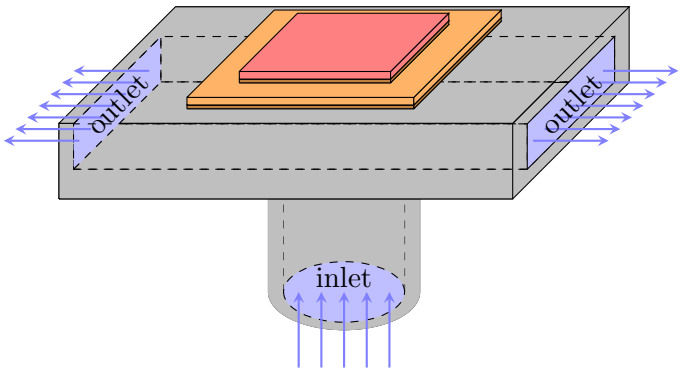


Figure 2.5: jet-impingement cooling concept

A simple jet-impingement concept is shown schematically in figure 2.5. An inlet is located at the bottom of the heat sink, under the chip, causing the liquid to impinge on the top internal surface of the heat sink. In the schematic view, both the left and right sides of the heat sink serve as outlets. In real implementations, one single outlet is preferred for practical reasons. This makes the internal structure of the heat sink more complex.

2.4 Heat sinks

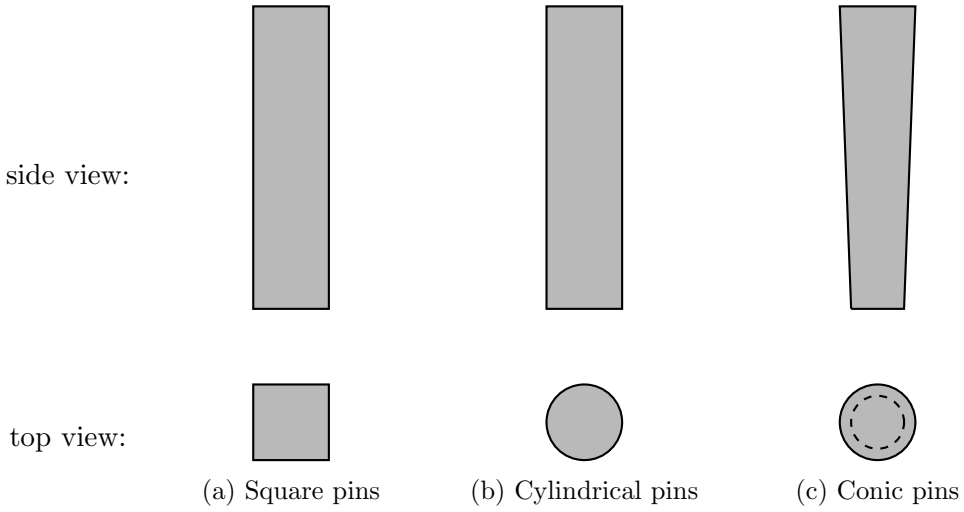
Heat sinks are passive components used to dissipate heat generated by electronic devices. They are usually made of aluminum or copper due to their high thermal conductivity. In this work the heat sinks are made of Aluminium nitride (AlN) ceramic. Heat sinks work by increasing the surface area of the device, which allows more heat to be dissipated into the surrounding fluid by convection. They are designed to maximize the surface area-to-volume ratio. The most common shapes are plate fins and pin fins heat sink. Plate fin structures separate the flow in smaller channels, leading to higher dissipation surface and higher fluid velocity. Pin fins are many small, closely spaced pins that extend from the base of the heat sink. The pins create a large amount of surface area, which increases the amount of heat that can be dissipated. Additionally, the closely spaced pins create a significant amount of turbulence due to the separation effect, which leads to better mixing fluid flow, further increasing the rate of heat transfer. Several publications show that the thermal performance of pin fins is better than plate fins (e.g. [85, 86]). Therefore, in this work the focus is on pin fin heat sink.

2.4.1 Pin-fin structures

Different shapes of heat sink structures and pin fins could be used in the cooling channel. In [87], three types of pin fin heat sink are investigated: square, circular and triangular

pins. It is found that circular pins are more efficient for heat transfer, compared with other fins with lower pressure drop. On the other hand the square fins cause the highest pressure drop.

In this work, mainly square, circular and conical pins are investigated, because they are easy to manufacture compared with other complex shapes like elliptical and mix-formed pins. Figure 2.6 shows these pins structures. The size and design parameters of the pins investigated in this work are discussed in chapter 5.

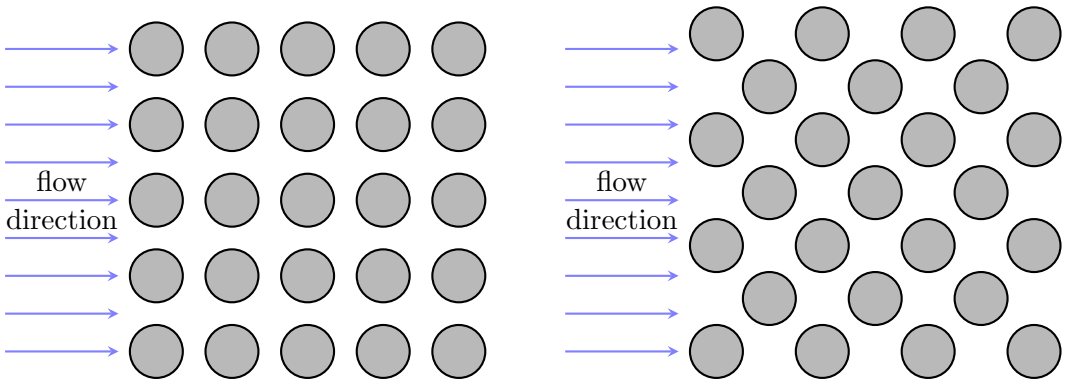


(a) Square pins (b) Cylindrical pins (c) Conic pins

Figure 2.6: Three different pins structures

2.4.2 Pins arrangement

In addition to different pin structures, the pins could be arranged in different layouts. In-line and staggered pins are two common layouts for pin-fin heat sinks. In-line pins are arranged on a grid pattern. The pins are evenly spaced, allowing for even fluid flow through the heat sink. On the other hand, a staggered pattern creates more turbulence (vortex) flow through the heat sink. Staggered pins generally dissipate heat more effectively than in-line pins because they create more turbulence in the fluid flow [88]. A comparison between in-line and staggered pins is investigated by Khan [89]. The thermal resistance of a cooler with staggered pins is about 44 % than that of the cooler with in-line pins. However, staggered pins deliver higher pressure drop. Furthermore, they may be more expensive to manufacture as they require more complex tooling. Both pins layouts are shown in Figure 2.7. Both layouts are considered in this work.



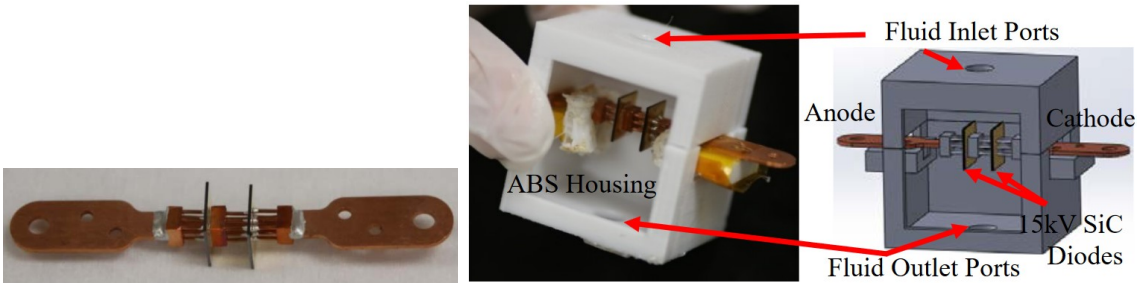
(a) in-line pins (b) staggered pins

Figure 2.7: Two different pin layouts

2.5 Cooling of high power density devices

Powerful small chips and high voltage semiconductor devices generate high power densities ($> 200\,\mathrm{W/cm^2}$). The heat generated must be dissipated efficiently, otherwise the temperature of the power electronics devices would increase too much, which would affect the efficiency and reliability of the modules. In this section, we focus on packaging solutions presented in the literature which integrate the heat sink in the package (figure 2.3b). This because integrated cooler is more efficient, has better cooling performance especially for high power density and it is the state-of-the-art packaging structure.

Boteler et al. [90, 91] introduce a novel package for stacked diodes, capable of handling voltages up to 30 kV. This package consists of two junction barrier schottky (JBS) diodes ($5\,\mathrm{mm} \times 5\,\mathrm{mm}$), each rated at 15 kV. The unique feature of this design is the elimination of direct bonded copper (DBC) substrates, as the diodes are submerged in a dielectric fluid. Electrical connections and heat dissipation are achieved using three multi-functionality connectors (MFCs) made out of copper. These MFCs serve as both electrical connectors, connecting the diodes internally and externally, and as heat sinks. The diodes are attached to the MFCs using a high conductivity silver epoxy, and leads are soldered to the left and right MFCs to serve as terminals (see Figure 2.8a). To ensure the integrity of the package, a sealed dielectric housing is applied to contain the dielectric fluid. Figure 2.8b showcases the completed module with the stacked series diodes. The module uses 3M Novec 7500 Engineered fluid, chosen for its satisfactory dielectric performance and heat transfer properties. Under a heat density of $15\,\mathrm{W/cm^2}$ and a flow rate of approximately $2.25\,\mathrm{L/min}$, the device exhibits a temperature rise of $10.2\,^{\circ}\mathrm{C}$. This results in a calculated thermal resistance of $0.68\,\mathrm{cm^2K/W}$. Additionally, a pumping power of 40 mW is measured at the aforementioned flow rate. This innovative approach holds promise for high voltage semiconductors. However, a significant challenge lies in securely bonding the connectors



(a) Fabricated central structure (b) Fabricated module

Figure 2.8: The integrated pins into the paseplate and the investigated pin shapes by Hitachi [57]

to the dies, as high voltage chips are sensitive to mechanical handling. Furthermore, the presence of fluid flow may introduce bubbles into the system, potentially compromising the module's insulation properties. Lastly, the achieved thermal resistance is relatively high due to the low thermal capacity of Novec 7500 and the limited area of the heat dissipation surfaces.

Based on our research, we have found that there are currently no other publications available on the cooling system for high voltage power modules exceeding 20 kV. This is primarily due to the lack of packaging solutions available for such high voltage devices. However, there is a growing need to explore and develop cooling and packaging solutions for these modules in order to ensure their effective operation. As power electronics are rendered ineffective without proper packaging and cooling systems, it is expected that future investigations will focus more on addressing this critical aspect. Generally, there is a lack of publications addressing the cooling of power electronic devices rated at > 10 kV and only a few of them give details about the investigated cooling methods. This review will focus more on cooling of high power density modules.

Three publications [92, 93, 60] describe the cooling of a 10 kV module. A module of 18 10 kV MOSFETs mounted to a cold plate is studied by Passmore et al. [92]. A junction-to-case thermal resistance of 0.026 K/W per switch position with 3000 W heat dissipation is achieved. No further details about the cooling system are given. The same can be said about Zhao et al. [60], where a package design for 10 kV is numerically investigated without further details about the cooling design. A thermal resistance of 0.44 K/W is reached for a module housing two 4 mm $\times$ 4 mm SiC dies. Mouawad et al. [93] use a jet impingement cooling system with water as coolant for a 10 kV module. To evaluate the performance of the integrated direct-substrate jet-impingement cooler, thermal impedance measurements are carried out on a Mentor Graphics Power Tester. The thermal resistance is measured at different flow rates with power losses of 139 W. The lowest measured junction-to-fluid thermal resistance of the module is 0.38 K/W (0.26 cm^2K/W) at 3 L/min

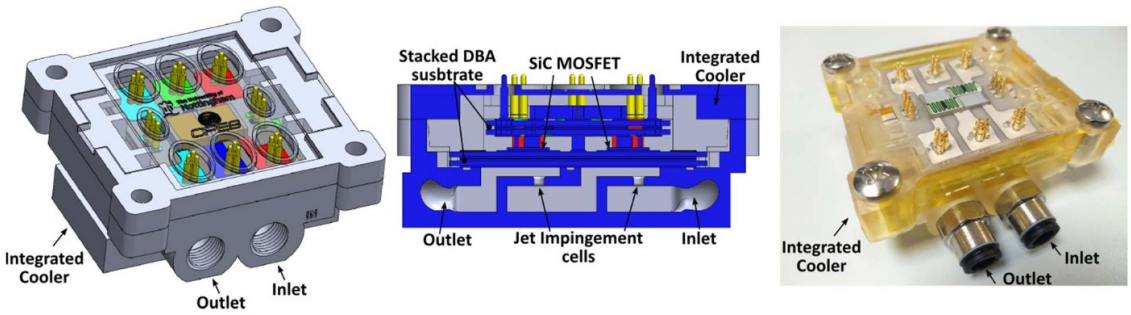


Figure 2.9: jet impingement integrated cooler in [93]

with 2.5 W pumping power. Figure 2.9 shows the investigated module with the integrated cooler. direct bonded aluminum (DBA) is used instead of direct bonded copper (DBC) as it offers better CTE matching between the layers. Furthermore, two stacked 1 mm thick AlN DBAs are joined together to achieve higher voltage isolation and reliability (by reducing the parasitic capacitance and produce a more uniform electric field distribution). Water is directly impinged on the bottom side of the stacked DBAs under each die to dissipate the heat generated by the SiC MOSFETs.

An integrated micro-channel water cooling system is presented in [94, 95, 96]. The integrated microchannel heat sinks are etched directly into the lower copper layer of the DBC substrate (320 µm). Figure 2.10 shows their modules with two IGBTs and two diodes with a schematic view of the heat sink. The bottom copper layer contains a row of 135 25 mm parallel microchannels with a height of 300 µm, a width of 100 µm and a Pitch of 200 µm. The base plate includes a set of inlet and outlet manifolds for uniform distribution of the water flow. This approach eliminates multiple layers of thermal resistance between the devices and the heat sink. With 3 L/min water flow and a pumping power of 6.65 W, a thermal resistance of 0.076 K/W for the IGBTs is achieved. This is about 1.71 cm^2K/W thermal resistance (thermal resistance multiplied by chip size). Such a cooling approach is thermally efficient, but at the expense of high pumping power (large pressure drop). In addition, such a heat sink and manifold design is complex to manufacture and expensive. This cooling design cannot be used for high-voltage power electronics ($>$ 10 kV) with a ceramic thickness of 320 µm due to insufficient electrical insulation.

Agbim [97] studies the integration of single-phase jet impingement cooling at the power electronics substrate level. Figure 2.11 shows a schematic view of the integrated jet cooler with the three jet array designs tested. This design eliminates the thermal resistance of the base plate and brings the coolant closer to the heated area. The array with 8 jets is found to have the best cooling performance. These jets have a diameter of 889 µm. A heat flux of 100 W/cm^2 is applied to a single 1 cm^2 chip heater mounted on a DBC substrate. The specific thermal resistance of 0.21 cm^2K/W is at a flow rate of 1.9 L/min and a pumping

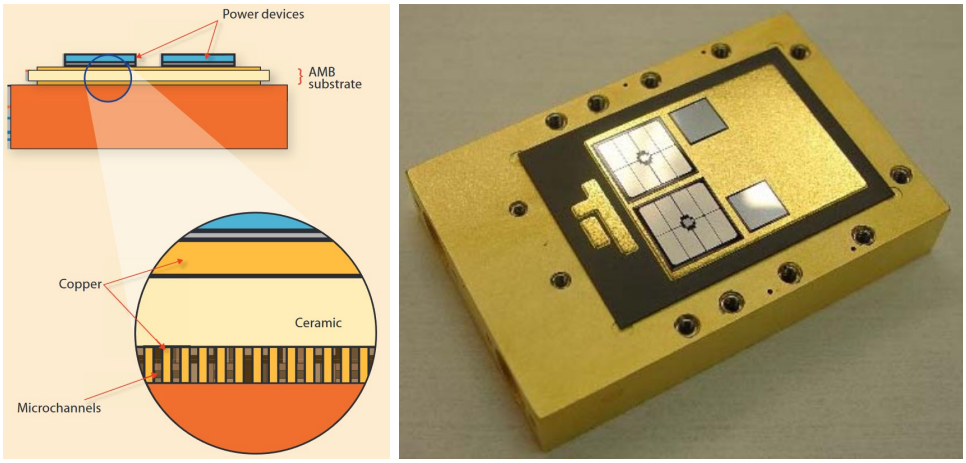


Figure 2.10: The integrated heat sink design and module with two IGBTs and two diodes [94, 96]

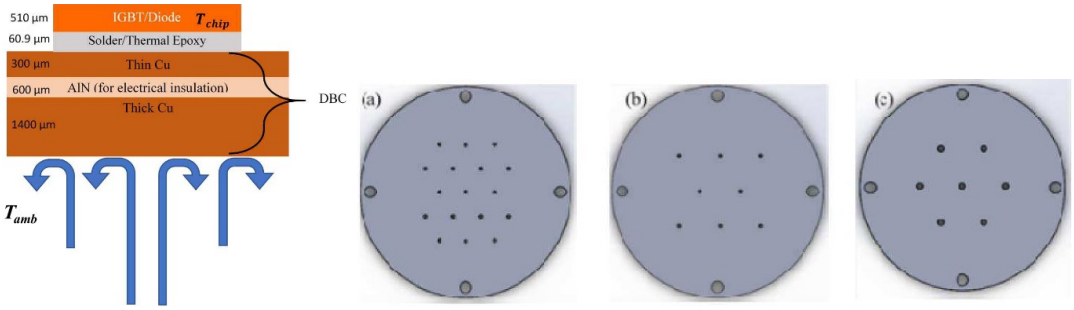


Figure 2.11: A schematic view of the integrated jet impingement cooler and jet array designs used for the test [97]

power of 2.6 W.

Another cooling method is the "shower-power" cooling. This cooling is a mini-channel cooler, but uses a fin array to control the direction the coolant in multiple directions instead of in one direction (standard micro-channel). The fins in the shower-power cooler act as a heat sink and as a liquid distributor in the channel. This results in more even coolant distribution and a larger effective heat transfer area, which can improve cooling performance. Bahman and Blaabjerg [98] perform a numerical optimization of shower-power coolers with water as coolant. Figure 2.12 shows the used design of the shower-power cooling system. The design is applied to a 1700 V/1400 A module with 12 IGBTs and 12 diodes. Various design parameters are changed to find the optimal cooling design. The final design has a thermal resistance of 0.2 K/W (0.39 cm^2K/W) with 5 L/min flow rate and 2.17 W pumping power.

This cooling method is interesting when water is used as the coolant because of the water's high heat capacity and low viscosity. The use of a dielectric fluid (usually with

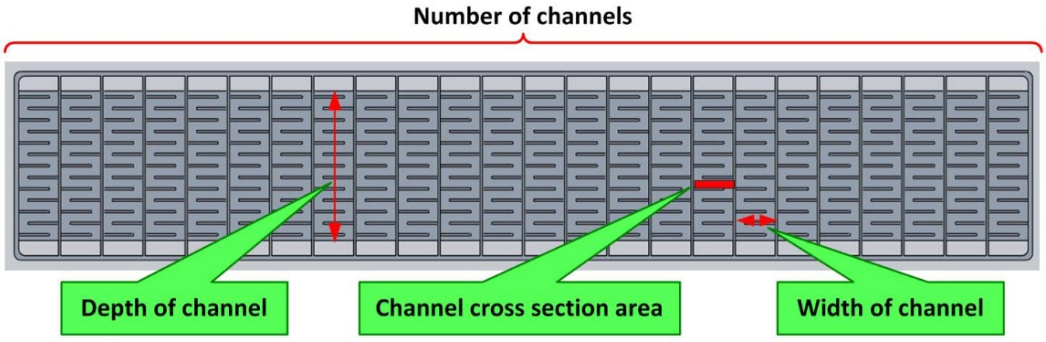
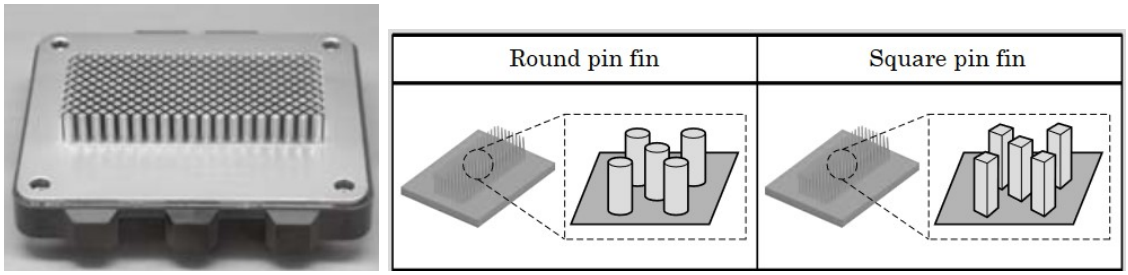


Figure 2.12: Design of the shower-power cooling system [98]



(a) integrated pins (b) investigated pin shapes

Figure 2.13: The integrated pins into the base plate and the investigated pin shapes by Hitachi [57]

lower heat capacity and higher viscosity) increases pumping power significantly due to the long fluid flow path. Also, due to the low heat capacity of the liquid, dielectric liquid requires more dissipation area to dissipate the heat.

The research paper [57] examines the effectiveness of direct liquid cooling for an IGBT module with 6 IGBTs and 6 FWD (Free-Wheeling Diode). During the inverter operation, the IGBTs and FWD generate power losses of 258 W and 31 W respectively. The study compares the cooling performance of round and square pins using LLC 50 % (Liquid manufacturer's brand of AISIN) as the coolant. The pins are integrated into the base plate of the power module. Figure 2.13 shows the integrated cooler and the two investigated pins shapes. The results show that the square pins have lower thermal resistance compared to the round pins. However, the square pins require a higher pumping power. At a flow rate of 10 L/min, the thermal resistance achieved with square pins is 0.27 K/W and is therefore lower than 0.29 K/W as achieved with round pins. The required pumping power is 1 W for both square and round pins.

Gould et al. [99] conduct a study comparing microchannel cooling and jet impingement cooling methods. In their experiment, a silicon carbide (SiC) module containing 16 JFET dies, each measuring 2 mm × 2 mm, is cooled. The microchannel cooler consists of 42 channels, each with a width of 200 µm and a height of 4.8 mm. On the other hand,

the jet cooler had 16 jets distributed beneath each die, with a jet diameter of 200 µm. To cool the module, they use a coolant mixture of water and ethylene glycol (WEG) with a volume ratio of 50 %, flowing at a rate of 0.195 L/min. The thermal resistance was reduced from 0.76 K/W (corresponding to a specific thermal resistance of 0.486 cm^2K/W) to 0.45 K/W (corresponding to a specific thermal resistance of 0.288 cm^2K/W). However, the pumping power required for the jet cooler is 5 times higher compared to the microchannel cooler. The jet cooler consumes 0.112 W of power, while the microchannel cooler requires 0.0224 W. This difference in power consumption should be considered when choosing between the two cooling methods.

Colgan et al. [100] examine the effectiveness of a microchannel cooler integrated into a single silicon (Si) chip module. The Si chip has dimensions of 20 mm × 20 mm and is etched to include staggered blunt fins measuring 250 µm × 25 µm. The channels between the fins are 75 µm wide and 195 µm deep, with no gaps between the rows of fins. A power of 1100 W is applied to the chip, resulting in a heat flux of 275 W/cm^2. By using the average temperature instead of the junction (maximum) temperature, they calculate the lowest average specific thermal resistance to be 0.105 cm^2K/W, with a water flow rate of 2.3 L/min and a pressure drop of 32.4 kPa (corresponding to a pumping power of 1.242 W). However, it is important to note that the specific thermal resistance calculated using the junction temperature would be higher than the average temperature. This can be estimated by adding half of the inlet-outlet temperature difference ($\Delta T_{out-in}/2$) to the average temperature, resulting in a specific thermal resistance of approximately 0.12 cm^2K/W. The utilization of water as a coolant in this cooling approach shows great promise. Compared to dielectric coolants, water has significantly higher thermal capacity, more than twice that of dielectric coolants. This means that when using dielectric coolants, the temperature rise will be approximately double compared to using water as a coolant. For instance, at water flow rate of 1.25 L/min, the temperature difference between the outlet and inlet of the coolant ($\Delta T_{out-in}/2$), is measured 19 °C when dissipating a heat flux of 400 W/cm^2. In contrast, if dielectric fluids were used, the temperature rise would be approximately 38 °C or even higher. In the case of a multi-die module, the temperature rise of the coolant would be even more significant, resulting in various and higher thermal resistances for the dies located under the warmer coolant. The use of high flow rates in this cooling approach may result in increased mechanical pressure and stress on the chip, potentially causing damage. As a result, this cooling method may not be suitable for high voltage power electronics. Additionally, the conductivity of water poses a risk in this application. Alternatively, dielectric coolants have lower thermal capacity, leading to significantly higher fluid temperature rises and may lead to phase change.

Gillot et al. [101] introduce another integrated cooler design for cooling a single 50 A 1.6 kV IGBT with dimensions of 14 mm × 14 mm. In this design, the IGBT silicon chip is

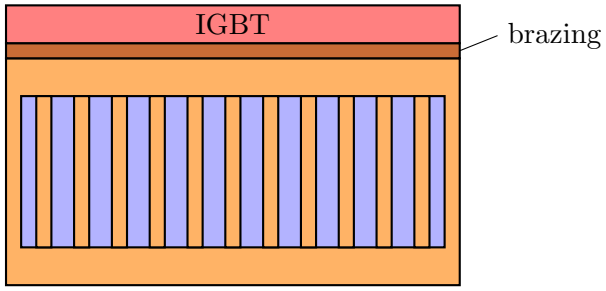


Figure 2.14: schematic representation of the integrated cooler investigated by Gillot et al. [101]

attached to a copper substrate with microchannels. Figure 2.14 illustrates this integrated cooler. The heat sink consists of finned parallel-plate channels with a channel height of 730 µm, width of 165 µm, and a pitch of 230 µm. The copper substrate contains 41 parallel fins. The study compares the performance of a single-phase cooler using water as the coolant with a two-phase heat exchanger using two coolants: water and the dielectric fluid "FC72". At a power dissipation of 300 W, the single-phase cooling (water) achieves a specific thermal resistance of 0.21 cm^2K/W with a flow rate of 1350 mL/min. The two-phase cooler slightly improves the specific thermal resistance to 0.21 cm^2K/W at a flow rate of 30 mL/min, while significantly reducing the pumping power from 360 mW to 0.135 mW. This improvement in thermal performance can be attributed to the higher heat transfer coefficient of the two-phase cooling method compared to single-phase cooling. The use of FC72 as a coolant results in a specific thermal resistance of 0.25 cm^2K/W at a flow rate of 300 mL/min Additionally, the pumping power required for FC72 is measured to be 13.5 mW, which is approximately 100 times higher than that of water.

The cooling approach used by Gillot et al. [101] offers low thermal resistance, but it lacks electrical insulation. When water is used as a coolant, an insulated plate (such as AlN) must be added between the chip and the copper block to ensure insulation. On the other hand, FC72, being a dielectric fluid, eliminates the need for an additional insulated substrate between the die and copper. However, it is still necessary to mount the copper onto an insulator to provide bottom side insulation. For two-phase cooling, further investigation is also required to understand the impact of phase change on the dielectric properties of dielectric fluids.

A similar cooling approach is employed by Schnur et al. [102] but with some differences. Instead of channel-flow cooling, they use a single-phase flow using jet impingement. They also use a dielectric liquid called Trafosynth2, which is manufactured by Panolin. Their study focuses on cooling a module containing 6 IGBTs and 6 diodes, rated at 1.2 kV/50 A. A flow rate of 15 L/min of Trafosynth2 is chosen. The researchers re able to achieve a specific thermal resistance of 0.43 cm^2K/W at a heat density of 60.4 W/cm^2. The pumping

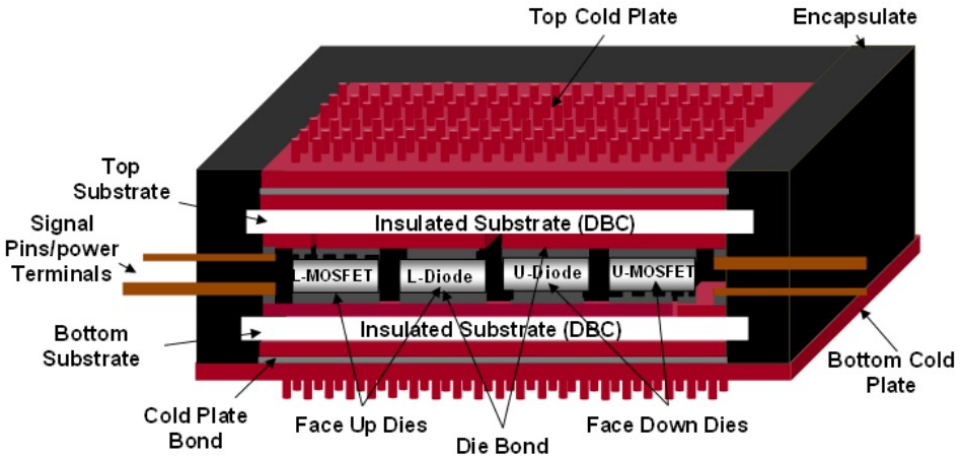


Figure 2.15: Cross sectional view of the module with dual cold plates presented by Liang [103]

power required for this cooling setup is measured at 3.05 W.

Liang [103] introduces a dual-sided direct cooling system for a 100 A/1200 V module, which consists in two paralleled 50 A/1200 V dies. Figure 2.15 illustrates the cross-sectional view of the module, showcasing the inclusion of dual pin-fin cold plates. Instead of using multiple tiny wire bonds, Liang's approach employs planar bonding, which allow for a larger area of contact with the die's top electrodes. This method facilitates the sandwiching of the dies between two DBC substrates. Furthermore, two cold plates (coolers) are directly bonded to the outside of these substrates, enabling double-sided, integrated heat sink. To achieve dual side liquid cooling, the module is assembled into a specific manifold that guides the flow of coolant through the pins of the cold plates. By implementing dual-sided cooling, Liang [103] is able to significantly improve the thermal resistance of the module. The double-sided cooling approach achieves a specific thermal resistance of 0.334 cm^2K/W, which is considerably lower than the 0.47 cm^2K/W obtained with integrated single cooling and the 0.541 cm^2K/W with conventional packaging. This demonstrates the superior heat dissipation capabilities of the dual-sided cooling system, making it a more efficient solution for managing thermal performance. Nevertheless, the implementation of a packaging concept that incorporates dual-sided cooling necessitates a more intricate design and the utilization of additional materials, resulting in increased costs.

The concept of dual-sided cooling in a packaging design was introduced previously by Buttay et al. [104]. In their study, they present a double-sided cooled, half-bridge module consisting of two schottky barrier diodes (SBD) and two IGBTs. They employ thin DBC substrates made of alumina (0.3 mm-thick), and layers of copper (0.6 mm). The use of a thin dielectric substrate results in lower thermal resistance, while the thick copper layers

facilitate heat spreading. Buttay et al. [104] compare the performance of the single-sided and double-sided cooling approaches. During the measurement process, a 5 mm × 5 mm SiC SBD is subjected to heating. The junction temperature of the SBD is subsequently determined using a thermal analyzer. Using single side cooling, the lowest specific thermal resistance achieved is 0.145 cm^2K/W with a flow rate of 3 L/min. This value is reduced to 0.09 cm^2K/W when employing double-sided cooling. It should be noted that the pumping power required for this system is relatively high, at 6.8 W for a single-module.

Other publication also investigate similar cooling concepts mentioned above (eg. [105], [106], [107]). Table 2.1 summarizes some of the articles on cooling of high power electronics, with a focus on specific thermal resistance as a fair comparison metric because thermal resistance value doesn't include the size of the semiconductor device, while the specific thermal resistance take the die size in account ($r_{th} = A \times R_{th}$). Some of these publications do not report the pumping power and specific thermal resistance, which makes it difficult to compare the results with other studies. Some of the specific thermal resistance values in table 2.1 are based on a chip size estimation based on the photographs provided in the articles.

2.6 Summary

This chapter has provided an overview of previous studies related to the cooling of high-power density and high voltage power electronics. The literature demonstrates that SiC semiconductors enable higher voltage capabilities and exhibit lower heat dissipation compared to Si semiconductors. Different packaging structures are discussed, highlighting their advantages and disadvantages, along with the solid layers used in these structures. Simplifying the packaging structure by reducing the number of solid layers can have several benefits. It can lead to a smaller package size and potentially improve the mechanical reliability of the package. Additionally, this simplification can also result in a shorter thermal path from the semiconductor to the coolant, thereby reducing the overall thermal resistance.

Various cooling methods, such as jet-impingement and channel-flow, are explored in the literature. Additionally, different heat sink designs with pin fins structures are examined. The chapter summarizes publications that specifically focus on cooling high-power density power electronics and presents a comparative analysis of these studies using specific thermal resistance as the parameter of comparison. Table 2.1 is provided to summarize the findings from these publications.

The chapter also compares the findings from the literature review to this work conducted by the author (referred to as TW in table 2.1). The specific thermal resistance of this work is found to be better than most of the literature, even with lower pumping

Table 2.1: Cooling performance comparison of different publications (CF: channel-flow; 2Ph: two-phase; DS: double-side; IC: Immersion cooling, TW: This Work)

Lit.	Description	Fluid (coolant)	Cooling system	Heat flux W/cm^2	r_{th} cm^2K/W	W_{pump} W
[56]	1.2 kV/500 A module (6 IGBTs)	LLC	CF	200 W	0.425	-
[57]	100 kW IGBT module	LLC	CF	258	0.27	1
[60]	10 kV power module	water	CF	104.2	0.21	-
[91]	30 kV Diode	Novec7500	IC	15	0.68	0.04
[92]	10 kV/240 A module 18 10 kV SiC MOSFETs	water	CF	300	0.33	-
[93]	10 kV SiC module	water	CF	212	0.26	2.5
[94]	200 A/1200 V IGBT (2 IGBT + 2 Diodes)	water	CF	470	0.17	6.65
[97]	single chip heater	water	jet	100	0.21	2.6
[98]	1700 V/1400 A module (12 IGBTs + 12 diodes)	WPG	CF	25.5	0.39	2.17
[99]	50 A/600 V (16 JFETs)	WEG	CF	236	0.49	0.0224
[99]	50 A/600 V (16 JFETs)	WEG	jet	236	0.29	0.112
[100]	High power chips (1 Chip)	water	CF	275	0.12	1.242
[101]	1.6 kV/50 A IGBT	water	CF	153	0.21	0.37
[101]	1.6 kV/50 A IGBT	water	CF: 2Ph	153	0.2	0.000135
[101]	1.6 kV/50 A IGBT	FC72	CF: 2Ph	153	0.25	0.0135
[102]	1.2 kV/50 A modue (6 IGBTs + 6 Diodes)	Trafosynth2	jet	60.4	0.43	3.05
[103]	planar SiC power module	-	CF	-	0.47	-
[103]	planar SiC power module	-	CF:DS	-	0.33	-
[104]	single-module (SiC SBD)	water	jet	220	0.145	-
[104]	single-module (SiC SBD)	water	jet: DS	220	0.09	6.8
[105]	High heat flux applications	water	jet	200	0.23	-
[106]	High power devices	water	jet	78.125	0.256	0.4
[107]	4 IGBTs + 4 diodes	water	CF	400	0.17	7.6
TW	20 kV module	water	CF+jet	367	0.114	0.27
TW	20 kV module	Novec7500	CF+jet	367	0.155	0.44

power. Only one publication (Buttay, 2007 [104]) is found to have slightly better thermal resistance than the author's work, but it used double side cooling and has a significantly higher pumping capacity. Furthermore, the packaging structure in this work is capable of blocking higher voltages ($> 20\,\mathrm{kV}$) with fewer solid layers and less complexity. Even when using a dielectric coolant (Novec7500), the recent work achieves better specific thermal resistance compared to other reported values in the literature.

Chapter 3

Materials

This chapter gives an overview of the materials used in this work and of their properties.

3.1 Power semiconductors

The power semiconductor devices serve as the primary component in any power module. They are electronic components made from semiconductor materials, typically silicon, silicon carbide or gallium nitride. These devices play a crucial role in modern electronics, enabling the control and manipulation of electrical signals. As technology continues to advance, semiconductor devices are becoming smaller, faster, more efficient and the ability to block higher voltage.

In this thesis, three different dies are used for the thermal investigations. The initial objective was to create a 20 kV module by connecting two 10 kV MOSFETs in series. Each die measures 8.1 mm × 8.1 mm. The computational fluid dynamics (CFD) optimization for the one-die module was conducted using these 10 kV MOSFET dies. However, due to the high cost of these devices, they were substituted with 9.1 mm × 9.1 mm Si IGBTs for the experimental tests. As the objective of the tests was to validate the CFD simulations, the IBGTs were considered a good substitute for the SiC MOSFETs.

After completing the optimization process for the one-die module and transitioning to the multi-die 20 kV module, the 10 kV MOSFETs were found not to be available any longer. As a result, the only solution was to replace them with other available MOSFETs. 3.3 kV MOSFETs have been chosen, with six dies being required for a 20 kV module. The 3.3 kV devices measure 8.9 mm × 3.676 mm. Table 3.1 provides an overview of the chips used in this work, including their size and purpose.

Table 3.1: The different semiconductor devices used in this work

Die type	Purpose	Size in mm^3
10 kV SiC-MOSFET (Cree)	CFD optimization of one-die module	$8.1 \times 9.1 \times 0.46$
1.2 kV Si-IGBT (ABB, 5SMY12H1280)	experimental test of one-die vehicle	$9.1 \times 9.1 \times 0.14$
3.3 kV SiC-MOSFET (GeneSiC, G2R50MT33-CAL)	CFD and experimental test of the multi-die vehicle	$8.9 \times 3.676 \times 0.39$

3.2 Ceramic cooler

Ceramic materials have gained significant attention in various industries due to their unique properties and potential applications. In particular, Aluminium nitride (AlN) has proven to be highly effective for thermal management. This section explores the advantages, disadvantages, and limitations of ceramic coolers with a focus on AlN as a prominent ceramic material.

AlN heat sinks offer several advantages over traditional cooling methods, such as metal-based cooling systems. Some of the key advantages include:

- AlN has a thermal conductivity in range of 160 to 200 W/mK depending on processing conditions and raw material purity, a value which is close to that of aluminium (237 W/(m K)). This property makes it ideal for applications requiring high-power electronics cooling.
- High-temperature stability: Ceramic coolers can withstand high operating temperatures (up to 1000 °C) without significant degradation in performance. This advantage is particularly crucial in industries such as aerospace and automotive, where components are exposed to extreme heat conditions.
- Electrical insulation: Ceramic materials are excellent electrical insulators. This property is particularly beneficial in power electronics.
- Thermal Expansion match with Si and SiC: AlN has a similar coefficient of thermal expansion (4-5 ppm/K) to Si and SiC (in the order of 3 ppm/K) comared to Aluminium alloy (19- 25 ppm/K) and copper (5 ppm/K). This similarity reduces thermo-mechanical stresses in the assembly.
- Chemical resistance: Ceramic coolers, including AlN, exhibit high chemical resistance, making them suitable for applications in corrosive environments.

While AlN coolers offer numerous advantages, they also have some disadvantages and limitations that need to be considered:

- Brittleness: Ceramic materials, including AlN, are inherently brittle and prone to cracking or breaking under mechanical stress. This brittleness can limit their use in applications that require high mechanical strength or resistance to impact.
- Cost: Ceramic materials, especially those with high-performance properties (e.g. AlN), can be more expensive than traditional cooling materials like metals.
- Complex manufacturing process: The manufacturing process for ceramic coolers require specialized equipment and expertise. This complexity can lead to longer production times and higher manufacturing costs.
- Limited design flexibility: Unlike metals, which can be easily shaped and molded into complex geometries, ceramics have more limited options for intricate designs. This can restrict the ability to create customized or unique cooling solutions for specific applications.

Additionally, the brittleness of ceramics can further limit design flexibility as it may impose constraints on the shape, size, and structural integrity of the cooler. This can be a challenge when trying to optimize the cooler's performance or integrate it into compact or unconventional spaces.

Although manufacturing AlN coolers can be costly, it offers the advantage of reducing the size and complexity of the packaging structure. This can help offset the total cost of the package. Additionally, AlN heat sinks bring the semiconductor devices closer to the heat sink and eliminate certain interface layers, reducing the potential for failure.

Some industrial companies produce AlN coolers and heat sinks due to their superior advantages. CeramTec (a partner of the ARCHIVE project) and AnCeram are leading companies in Europe for ceramic cooler manufacturing. AlN AMB substrates (Active Metal Brazing) have emerged as a cost-effective and reliable alternative to other assembly techniques. CeramTec has developed various AlN coolers with different designs. Figure 3.1 showcases two examples of metallized ceramic coolers manufactured by CeramTec.

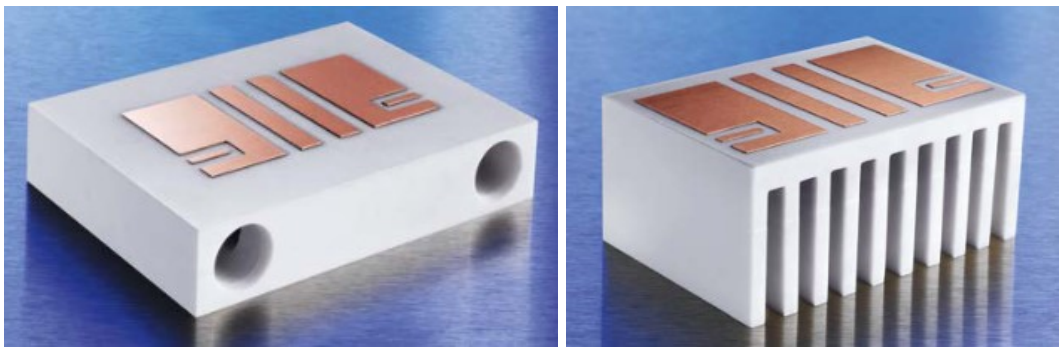


Figure 3.1: Tow metallized ceramic coolers/heat sinks manufactured by CeramTec

All AlN coolers used in this study are sourced from CeramTec. It's imperative to recognize that these AlN coolers are subject to particular design constraints. For example, the length of the pins should not exceed three times their diameter, and there should be a minimum spacing of 1 mm between the pins. These design limitations play a significant role in the optimization of coolers using computational fluid dynamics (CFD) simulations. According to CeramTec, AlN coolers have a breakdown voltage of at least 15 kV/mm or higher. Additionally, they possess a thermal conductivity of 170 W/mK or higher.

3.3 Solid layers of the package

In addition to the semiconductor device and the ceramic cooler, copper is essential for both electrical connections and heat spreading. Copper exhibits high thermal conductivity, which helps improve heat transfer to the AlN cooler and subsequently to the coolant.

To attach the copper tracks to the ceramic cooler, an interface material is required. This work utilizes active metal brazing as the attachment process. Metal brazing is a high-temperature process in which a brazing material melts to joins different parts. An active solder is used by CeramTec for brazing. It provides high thermal conductivity (361 W/mK, similar to that of copper, at 394 W/mK). The power semiconductor device is affixed to the copper using a silver sintering process. Sintering forms a robust mechanical connection with good thermal conductivity (150-250 W/mK), surpassing other techniques such as soldering [108].

For simulations in which a "traditional cooling" (i.e a power module attached to a heatsink) is considered, a layer of thermal interface material (TIM) must be placed between the module and the heatsink. TIM materials typically have low thermal conductivity, often below 5 W/mK.

In the final module, snubber circuits are required to handle the transient voltage and current of the semiconductor devices. These snubbers consist of capacitors and resistors, typically made of alumina (Al_2O_3). Al_2O_3 has a thermal conductivity range between 20 to 30 W/mK [109]. These components contains other different elements (terminations, coating and resistive layer), which can affect their thermal conductivity but are not considered to simplify the CFD model. As the overall thermal conductivity of the components is expected to be lower than that of pure Al_2O_3, a thermal conductivity of 13 W/mK is considered here. The snubber components are soldered to a DBC, with the solder material (SAC) typically having high thermal conductivity (> 50 W/mK). However, in the CFD simulation, this material is neglected due to its low thermal resistance and to simplify the system. To attach the snubber substrates to the heatsinks, an adhesive glue with a thermal conductivity of 11 W/mK (as stated in the data sheet) is used. Other materials in Table 3.2 will be discussed later.

Table 3.2 shows the thermal properties of the solid materials used for the numerical calculations.

Table 3.2: The thermal conductivity and thicknesses of the solid materials employed in this study for the CFD simulations

Material	Thermal conductivity λ[W/(mK)]	Thickness b[µm]
Chip (4H-SiC)	370	390
Die Attach (Ag)	100	50
spreader (Cu)	394	300 to 1000
Metal braze (active solder)	361	10
AlN	170	1000 to 5000
Resistors (Al_2O_3)	13	650
Cu1	394	300
AlN1	170	650
Cu2	394	150
TIM (epoxy adhesive glue)	5	50
Glue (epoxy adhesive)	11	50

3.4 Cooling fluid

Water and water/glycol mixture are commonly used as coolants due to their excellent thermal properties. However, these coolants are not suitable for applications with high voltage due to their electrical conductivity. While deionised water is non-conductive, it requires constant de-ionisation, which is challenging to maintain in a circulating cooling loop. Additionally, water has a high permittivity, which is not desirable in certain applications. In this case, it is important to have a coolant with a similar permittivity to that of AlN ceramic ($\epsilon_r \approx 8-9$). Having a close permittivity between materials ensures a homogeneous distribution of the electrical field in the heatsink filed with the cooling fluid.

The dielectric fluid used as a coolant in the system should obviously have high electrical insulation and its permittivity closely match that of the cold plate AlN ceramic ($\backsim 8$) so that the electric field is uniformly distributed over ceramic/fluid domain. The electrical resistivity of the fluid has to be higher than $9 \times 10^5\,\Omega\,\mathrm{m}$. To avoid two-phase flow, the boiling temperature of the liquid should be higher than 80 °C. Beside good dielectric properties, good thermal properties are required for the fluid. These aspects will be discussed in details later in this chapter.

In high voltage applications, the choice of coolant plays a crucial role in ensuring the safety and efficiency of the system. Two important features to consider are the Global Warming Potential (GWP) and the toxicity and flammability of the coolant. GWP refers to the potential of a substance to contribute to global warming, and it is essential to choose

Table 3.3: Requirements of the dielectric fluid

- Dielectric properties
  - Electrical resistivity: $9.0 \times 10^5 \Omega$m
  - high permittivity value
- Thermophysical properties
  - Boiling temperature: $T_b > 60\,^{\circ}$C
  - High specific heat capacity: $c_p > 1000\,$J/kgK
  - High thermal conductivity and low viscosity
- Environmental requirements
  - Global Warming Potential: $GWP \leq 200$, Non-toxic, Non-flammable

coolants with low or zero GWP to minimize their environmental impact. Additionally, non-toxic and non-flammable coolants are crucial for high voltage applications as they reduce the risk of harm to personnel and equipment. These features help to mitigate the potential hazards associated with leaks or accidental exposure to the coolant.

Table 3.3 summarizes the specification and requirements of the dielectric fluid.

3.4.1 Systematic evaluation and shortlist for further investigations

Tables 3.4 and 3.5 present some dielectric fluid candidates, which are non-toxic and have permittivity values above 2 (only fluids for which a permittivity value is provided by their manufacturers are considered). These fluids are compared with water/glycol mixture and water, which have a high heat capacity but are electrically conductive. Table 3.4 shows the thermal properties of the fluids and table 3.5 their dielectric properties. These fluids can be sorted into three groups: the "Novec" group (a commercial name for a family of fluids from the company 3M) (gray), other dielectric fluids (white), and water & glycol/water mixture (brown). Novec fluids have a much higher permittivity compared to the dielectric liquids. Beside that, Novec fluids have a low viscosity but in the other hand a lower thermal capacity. The electrical properties of the coolant are coloured green if they meet the requirements, blue if they are near the requirements, and red if they are very far from the requirements.

The most promising fluids are selected based on four characteristics:

Table 3.4: Overview of the thermal properties of the fluid candidates

Fluid	Sp. heat c_p[J/(kg K)]	Density ρ[kg/m^3]	Viscosity η[m Pa s]	Conductivity λ[W/(m K)]	Boiling/Flash T_b[°C)]
Novec 7100 [110]	1213	1448	0.47	0.0659	61
Novec 7200 [110]	1241	1389	0.3625	0.0661	76
Novec 7300 [110]	1166	1621	0.92	0.0625	98
Novec 7500 [110]	1151	1582	0.98	0.0625	128
Novec 7600 [110]	1319	1540	2.4	0.071	131
Novec 7700 [110]	1045.8	1760	2.83	0.0624	167
MIVOLT DF7 [111]	1907	916	15	0.129	> 194
MIVOLT DFK [111]	1902	968	72.6	0.147	> 250
Alpha-6 [112]	2203	815	25.265	0.1561	246
Alpha-4 [112]	2206	805	15.38	0.1470	220
Alpha-2 [112]	2205	799	4	0.1358	160
OptiCool-H [112]	2206	825	3	0.1346	> 135
OptiCool PH5 [112]	2203	825	4.9	0.1363	> 151
EC-120 [113]	2212	832.66	4	0.1359	157
BIO ELECTRA [114]	1970	910	36	0.1691	> 250
Silicone Transformer [115]	1510	960	48	0.151	> 300
Trafosynth 2 [116]	2040	900	11.7	0.13	< 240
Water/Glycol [117]	3420	1060	2.45	0.404	110
Water [118]	4135	992	0.65	0.63	100

Thermal properties

From the thermal point an ideal coolant has high heat capacity, high thermal conductivity, low viscosity. Higher thermal conductivity (diffusivity) allows faster and more effective heat dissipation from the power element to the coolant. The viscosity of a fluid is a measure of its fluidity, i.e the internal friction between the fluid's molecules. Lower fluid viscosity means a reduced pressure drop (lower pumping power) in the cooling loop.

An other important thermal property is the specific heat capacity c_p [J/(kg K)] of the fluid. This describes how much energy is required to change the temperature of 1 kg of the fluid by 1 K. A fluid with high heat capacity can absorb more heat with the same (or lower) temperature increase. Taking the liquid with the lowest heat capacity (Novec 7700) from the list and comparing it with water, then at 0.5 L/min and 450 W heat flow (corresponding to the full module presented at the end of this memoir), the water temperature rises by about 13 °C, against 30 °C for Novec 7700. These values drop to 2 °C for water and 5 °C for Novec7700 at 3 L/min (the target flow rate in our case). Therefore, a heat capacity

Table 3.5: Overview of the insulation properties of the fluid candidates

Fluid	Permittivity ϵ [–]	Diel. Strength [kV]	Resistivity [MΩ m]	GWP [–]
Novec 7100	7.4	28	33	297
Novec 7200	7.3	32	4	59
Novec 7300	6.1	26.7	10^3	210
Novec 7500	5.8	35	2	100
Novec 7600	6.4	≈ 40	10	700
Novec 7700	6.7	35	5×10^3	420
MIVOLT DF7	3.2	> 75	$> 9 \times 10^4$	< 1
MIVOLT DFK	3.2	> 75	$> 9 \times 10^4$	< 1
Alpha-6	2.11	58	-	< 1
Alpha-4	2.10	58	-	< 1
Alpha-2	≈ 2	58	-	< 1
OptiCool-H	2.12	58	10^6	< 1
OptiCool PH5	2.12	58	10^6	< 1
EC-120	2.1	60	$> 10^6$	< 1
BIO ELECTRA	3.1	65	74	< 1
Silicon Transormer	2.7	50	10^6	< 1
Panolin Trafosynth 2	3.7	80	229	< 1
DI water	78.57 [119]	33.7 [120]	0.182 [121]	< 1

of more than 1000 J/(kgK) is acceptable as it would result in less than 5 °C temperature difference over the entire module.

Permittivity

As mentioned in chapter 1, the permittivity of the coolant must match closely as possible that of the AlN ceramic substrate. All Novec fluids match this requirement, since they all have a permittivity value above 5.

The second group has low permittivity values. However, one fluid from group two is chosen to compare it with the other groups. Trafosynth2 from the company "Panolin" is chosen from the second group, because it has the highest dielectric constant and good thermal and insulating properties. The second reason for Trafosynth2 is its availability in our lab.

Environmental requirements

This work also aims to not damaging the natural environment by using fluids withlow global warming potential (GWP). The GWP is a measure of the warming effect of a molecule once it is in the atmosphere, over a certain period of time (usually 100 years). In other words, it indicates how much a certain mass of a greenhouse gas (emitted by the materials/fluids) contributes to global warming compared to the same mass of CO_2. As could be seen in table 3.3, the GWP value should be lower than 200. Therefore, Novec 7700 and 7600 fall out of the shortlist. All fluids in second group have a GWP value smaller than one.

Boiling temperature

To avoid two-phase cooling in the system, the maximum temperature of the liquid in operation must remain under its boiling temperature. From a thermal management point-of-view, dual phase cooling would be more efficient. However, the formation of gas bubbles in the cooling channel could lead to inhomogeneities electric field and possibly to issues with the electrical insulation. Therefore, it is decided to select coolants which will remain in the liquid phase in normal operation. The maximum temperature the fluid can achieve correspond to the maximum temperature at the bottom side of the AlN substrate. This temperature can be estimated using the following equation, assuming that the area of all layers are the same as the die area (i.e. no heat-spreading effect):

$$\begin{aligned} T_{f_{max}} - T_j &= \dot{Q}\left(R_{th_{SiC}} + R_{th_{Ag}} + R_{th_{Cu}} + R_{th_{Braze}} + R_{th_{AlN}}\right) \\ &= q\left(\frac{b_{Chip}}{\lambda_{Chip}} + \frac{b_{Ag}}{\lambda_{Ag}} + \frac{b_{Cu}}{\lambda_{Cu}} + \frac{b_{Braze}}{\lambda_{Braze}} + \frac{b_{AlN}}{\lambda_{AlN}}\right) \\ &= \frac{125\,\mathrm{W}}{8.1 \times 8.1\,\mathrm{mm}^2}\left(\frac{300}{394} + \frac{50}{100} + \frac{300}{394} + \frac{10}{35} + \frac{1500}{170}\right)\frac{\mu m}{W/(mK)} \\ &= 20.1\,\mathrm{K} \end{aligned} \tag{3.1}$$

with the thermal resistance of layer i being:

$$R_{th_i} = \frac{b_i}{\lambda_i A_i} = \frac{b_i}{\lambda_i A_{die}} \tag{3.2}$$

and the heat flow density:

$$q = \frac{\dot{Q}}{A_{die}} \tag{3.3}$$

where b_i and A_i are the thickness and heated area of each layer. This calculation estimates the temperature difference in the worst case. In reality, heat is distributed over a larger surface (heat spreading effects) so the heat flux and the thermal resistances decreases from one layer to the next.

Considering that the junction temperature is $T_j = 100\,°C$, the boiling temperature of the coolant should be at least $80\,°C$ ($100\,°C - 20.1\,°C$) in normal condition to avoid two phase flow. However, in overload condition the junction temperature could increase to more than $100\,°C$ which leads to higher fluid temperature. Therefore, a higher boiling temperature is preferred for the purpose of single-phase flow.

Shortlist of coolant candidates

Novec 7100 and Novec 7200 have the closet permittivity values to AlN, but their low boiling temperatures make them unsuitable. Novec 7600 and Novec 7700 have a high GWP value. Also, they have much higher viscosity than other liquids from the same group, resulting in higher pumping capacity. Therefore, these two liquids are removed from the short list. On the other hand, Novec 7300 and Novec 7500 are less harmful to the environment due to their lower GWP values. Both liquids have good thermal and electrical properties. Novec 7300 is slightly better than Novec 7500 from a thermal perspective, but Novec 7500 is more environmentally friendly and has better dielectric strength, which might be required to block the desired voltage ($20\,kV$).

Because of good thermal properties, high boiling/flash point, and the highest permittivity value ($\epsilon_r = 3.7$) from the second group, Panolin Trafosynth2 is also selected to be investigated from group two. That means the shortlist retains just three fluids "Novec 7300", "Novec 7500", "Trafosynth2" as well as water and glycol/water mixture as references.

3.4.2 Thermal properties of the selected coolants

The thermal properties of the coolant are very important for the thermal management of the power modules, and these properties are strongly affected by the temperature. This is described in this section, so that suitable models can be identified for the CFD simulations in the next chapters. All data mentioned in this section are provided by manufacturer of the fluids or found in other publications. All references for the fluids are stated in table 3.4.

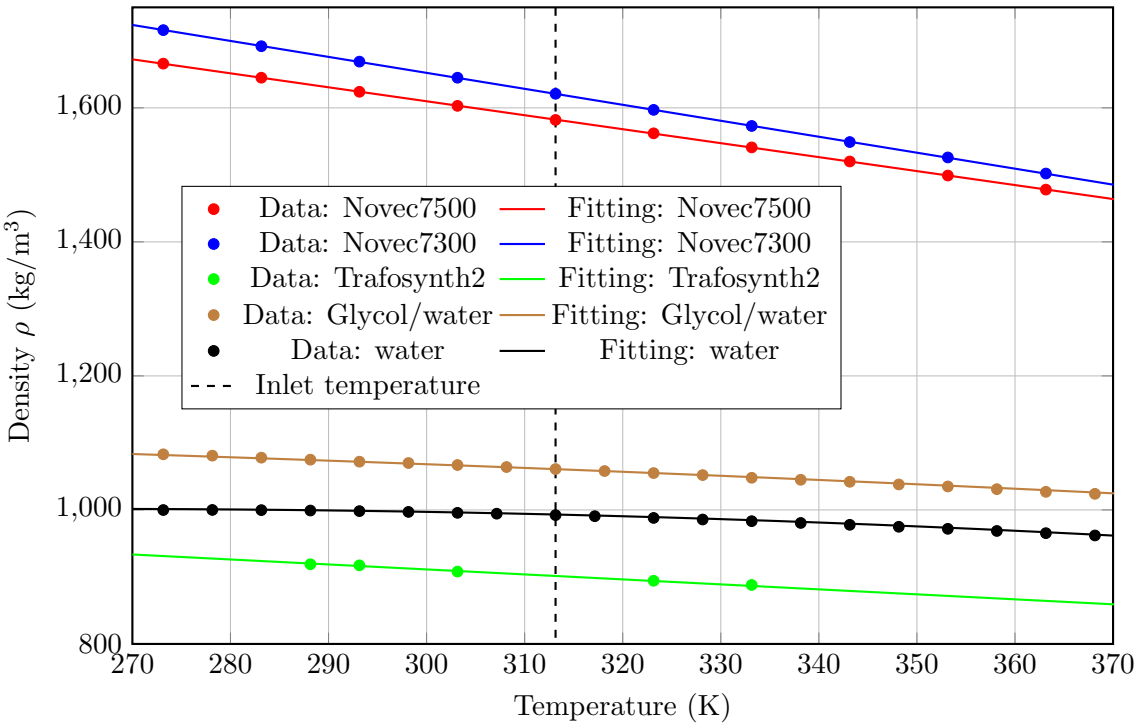


Figure 3.2: The density of the selected fluids as a function of the temperature

Density ρ

The density (weight per cubic meter) of the selected liquids as a function of temperature is shown in figure 3.2. Polynomial functions (regression curves) are generated from the given raw data. It can be seen that Novec fluids are about 60 percent denser than water. On the other hand, Trafosynth2 is 10 percent lighter than water. The dashed line in the diagram represents the considered inlet temperature ($T_{in} = 40\,°\text{C} = 313.15\,\text{K}$).

The "fitting" curves are plotted using the following polynomials:

$$\text{Novec7500:} \quad \rho(T) = -2.0845T + 2235.2 \tag{3.4a}$$

$$\text{Novec7300:} \quad \rho(T) = -2.3829T + 2367.1 \tag{3.4b}$$

$$\text{Trafosynth2:} \quad \rho_(T) = -0.7436T + 1134.2746 \tag{3.4c}$$

$$\text{water/glycol:} \quad \rho_(T) = -1.12 \cdot 10^{-3}T^2 + 0.13T + 1137 \tag{3.4d}$$

$$\text{water:} \quad \rho_(T) = -0.00365471T^2 + 1.93017T + 746.025 \tag{3.4e}$$

Specific heat capacity c_p

The specific heat capacity plays a major role in heat transfer. It is a measure of the fluid's ability to store thermal energy. Figure 3.3 shows the specific heat capacity changes with temperature for the shortlisted fluids.

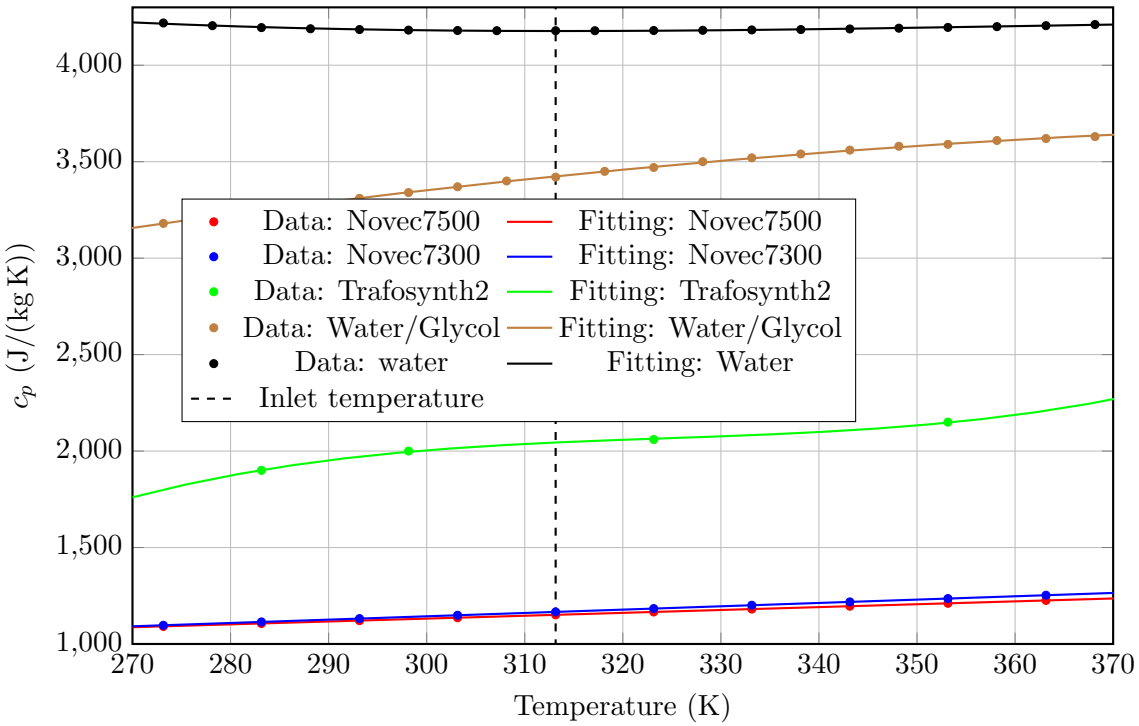


Figure 3.3: The specific heat capacity of the selected fluids as a function of the temperature

C_p increases with the temperature. The Novec fluids have similar values, which are about four times lower than those of water and two times lower than those of the Panolyn Trafosynth2.

The fitting polynomials in Figure 3.3 are as follows:

$$\text{Novec7500:} \quad c_p(T) = 1.498 \cdot T + 681.76667 \tag{3.5a}$$

$$\text{Novec7300:} \quad c_p(T) = 1.73 \cdot T + 624.45 \tag{3.5b}$$

$$\text{Trafosynth2:} \quad c_p(T) = 0.0013 \cdot T^3 - 1.26 \cdot T^2 + 410.24 \cdot T - 42696.8 \tag{3.5c}$$

$$\text{water/glycol:} \quad c_p(T) = -0.0238 \cdot T^2 + 20.0774 \cdot T - 526.8311 \tag{3.5d}$$

$$\text{water:} \quad c_p(T) = -0.000127 \cdot T^3 + 0.137 \cdot T^2 - 48.67 \cdot T + 9850.7 \tag{3.5e}$$

Dynamic viscosity μ

The dynamic viscosity gives the ratio between the shear stress and the velocity gradient. In Figure 3.4, it can be seen that the viscosity decreases with increasing temperature, because the distance between the molecules increases. Higher temperatures lead to less inter-molecular attraction between them, which reduces viscosity. The dynamic viscosities of the Novec fluids are slightly higher than that of water, while Trafosynth2 has much higher dynamic viscosity. Therefore, Trafosynth2 requires a much higher pumping power

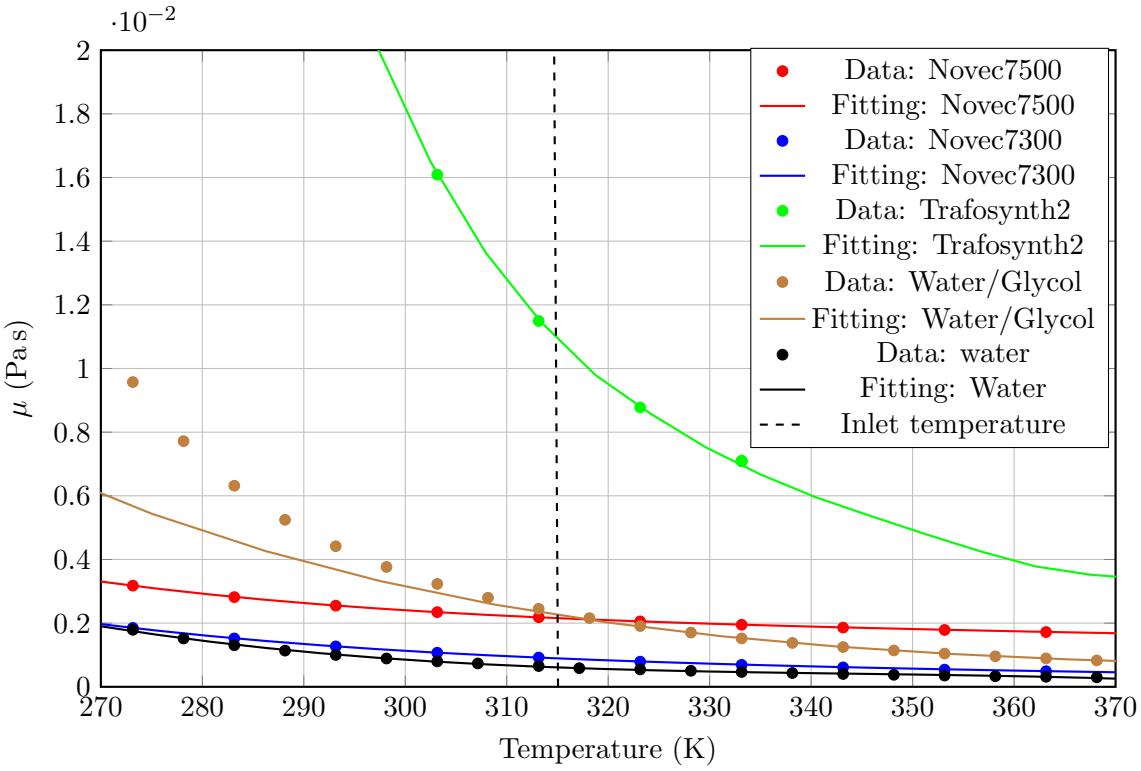


Figure 3.4: The dynamic viscosity of the selected fluids as a function of the temperature

to be circulated in the cooling system than other liquids.

The following equations give the dynamic viscosity of the fluids as a function of the temperature:

Novec7500:

$$\mu(T) = 9.8 \cdot 10^{-12} T^4 - 1.4 \cdot 10^{-8} T^3 + 7.75 \cdot 10^{-6} T^2 - 0.002T + 0.18 \tag{3.6a}$$

Novec7300:

$$\mu(T) = 8 \cdot 10^{-12} T^4 - 1.16 \cdot 10^{-8} T^3 + 6.4 \cdot 10^{-6} T^2 - 0.0016T + 0.15 \tag{3.6b}$$

Trafosynth2:

$$\mu(T) = 1.11 \cdot 10^{-9} T^4 - 1.56 \cdot 10^{-6} T^3 + 8.15 \cdot 10^{-4} \cdot T^2 - 0.2T + 16.53 \tag{3.6c}$$

water/glycol:

$$\mu(T) = 7.6 \cdot 10^{-12} T^4 - 1.3 \cdot 10^{-8} T^3 + 8.5 \cdot 10^{-6} \cdot T^2 - 0.0024T + 0.26 \tag{3.6d}$$

water:

$$\mu(T) = -2.81 \cdot 10^{-9} T^3 + 2.9 \cdot 10^{-6} T^2 - 0.001T + 0.117 \tag{3.6e}$$

High order polynomials are chosen for the viscosity regressions so that they never achieve the zero value ($\mu = 0$), because would be physically invalid (it's impossible to have

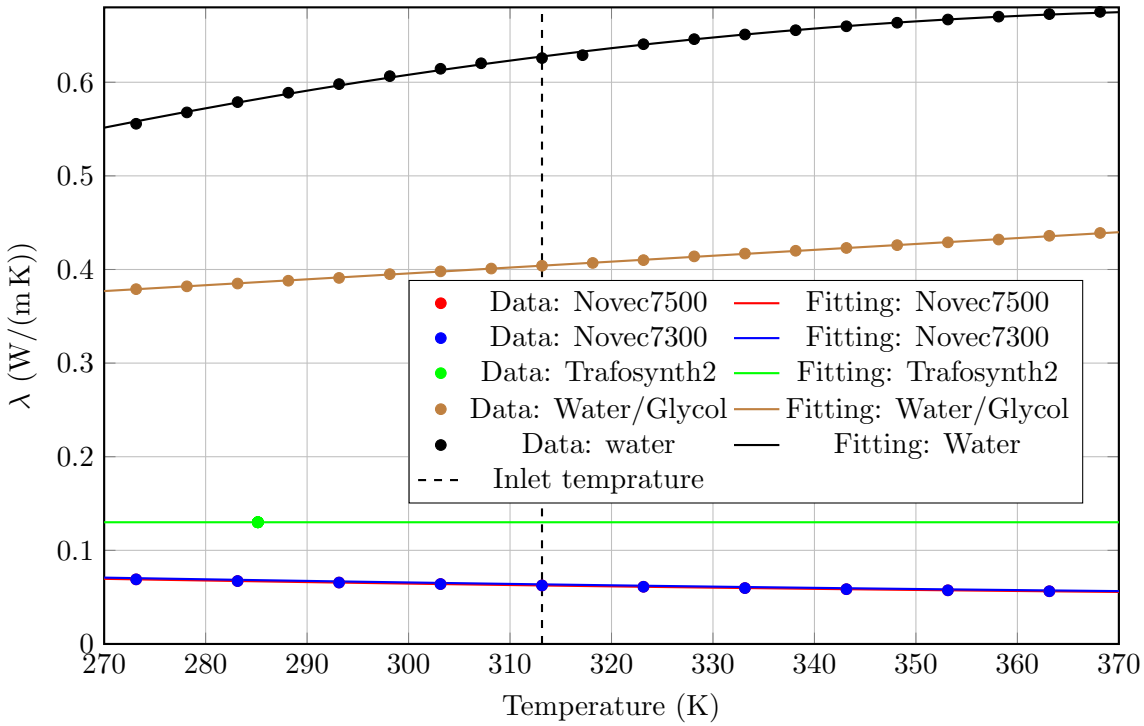


Figure 3.5: The thermal heat conductivity of the selected fluids as a function of the temperature

a material with negative viscosity). That will also avoid bad convergence behavior during the CFD simulations, in case a high temperature is achieved during the first numerical iterations. The fit of the glycol/water mixture appears to be poor, below the inlet temperature, which is not an issue here, as the fluid temperature cannot drop below the inlet temperature.

Thermal heat conductivity λ

Thermal conductivity increases with temperature, as shown in Fig. 3.5. All three dielectric liquids have much lower conductivity than water, about ten times lower for Novec fluids and 5 times for Trafosynth2.

The following expressions describe the thermal conductivity of the fluids:

$$\text{Novec7500:} \quad \lambda(T) = 4.24 \cdot 10^{-7} T^2 - 4.1 \cdot 10^{-4} T + 0.15 \tag{3.7a}$$

$$\text{Novec7300:} \quad \lambda(T) = 4 \cdot 10^{-7} T^2 - \cdot 10^{-4} T + 0.15 \tag{3.7b}$$

$$\text{Trafosynth2:} \quad \lambda(T) = 0.13 \tag{3.7c}$$

$$\text{water/glycol:} \quad \lambda(T) = 6.29 \cdot 10^{-4} T + 0.2071 \tag{3.7d}$$

$$\text{Water:} \quad \lambda(T) = -9.3 \cdot 10^{-6} T^2 + 0.0072 T - 0.711 \tag{3.7e}$$

Unfortunately there are no measured thermal conductivity data for the Traofsynth2. However, the manufacturer (Panolin) gives a measured value at 25 °C of $\lambda(T = 25\,°C) = 0.13\,W/(mK)$. Therefore, a constant value is assumed here for Panolin Trafosynth2.

3.5 Summary

In this chapter, the materials used in the thesis work are presented. Three power semiconductor devices are considered for both the CFD simulation and experimental tests. Among the materials of proposed package, AlN is given a special care, as it is used for the cooler. Despite some drawbacks, such as high cost and limited design flexibility, AlN coolers exhibit promising thermal performance and excellent electrical insulation properties.

The chapter then investigates the dielectric fluids that can be used in the application. The focus is on dielectric fluids with high dielectric constants, close to that of AlN, to achieve a uniform electric field distribution. Other properties such as electrical insulation, global warming power, or toxicity are also considered. Three dielectric liquids are shortlisted as possible candidates.

The thermal properties of these fluids ("Novec 7300," "Novec 7500," and "Trafosynth2") are compared with water and a water/glycol mixture, which serve as references. In particular, the effect of the temperature on the physical properties of the fluids is studied. Models (polynomias) are identified for the density, heat capacity, dynamic viscosity and heat conductivity of the fluids. These models are later employed in CFD simulations.

Chapter 4

Methods

The aim of this chapter is to familiarize the reader with the techniques employed throughout the study and to provide a theoretical background for better understanding of these methods. The use of appropriate methods is crucial in any scientific endeavor, as they serve as the foundation for reliable and accurate results. In this regard, the range of techniques are carefully selected and applied.

To begin, we outline the theoretical concepts of heat transfer. Understanding the underlying principles and assumptions is essential for interpreting the results of an experiment and drawing meaningful conclusions. We provide a comprehensive overview of the relevant theories, models, and equations, ensuring that readers can grasp the fundamental concepts and principles that guide the application of these methods.

A second section is dedicated to numerical simulation. It presents the models and assumptions involved in Computational Fluid Dynamics (CFD), the numerical simulation tool we use in this work for the optimisation of the coolers.

Then, we describe the experimental setups and equipment used in this work. This includes a description of the apparatuses and instrumentation used, as well as any modification made to suit the specific requirements of our study. Additionally, will discuss the rationale behind our choices, highlighting their advantages and limitations.

4.1 Heat transfer

The energy that is transported across a system boundary due to a temperature difference is referred to as heat. According to the second law of thermodynamics, heat always flows in the direction of decreasing temperature across the system boundary. Heat transfer is the process of energy transfer from a high-temperature region to a low-temperature region. Heat can be transported by three mechanisms: conduction, convection and radiation.

4.1.1 Heat conduction

Heat flows in a material as a result of the interaction between neighboring molecules due to an existing temperature gradient in the material. This is called thermal conduction. Heat is transported in radiation-opaque solids solely by conduction [122]. In power electronics packaging, heat is transported through the solid layers from the semiconductor device to the heat sink by conduction.

The heat flow $\dot{Q}(\mathbf{x})$ per unit area, is a measure of the heat flux $\dot{q}(\mathbf{x})$ in a given direction represented by the vector $\mathbf{x}$. The cause of heat flow in a material is the temperature gradient, and there is proportionality between this cause and its effect. The following relationship therefore applies to the heat flow density:

$$\dot{q}(\mathbf{x}, t) = -\lambda(T)\nabla T(\mathbf{x}, t)\,. \tag{4.1}$$

This equation from Biot and Fourier represents the basic law of heat conduction [123]. The minus sign indicates that the heat flux is pointing in the opposite direction of the temperature gradient. The proportionality coefficient λ stands for the so-called thermal conductivity and depends on the temperature and the material. It has the SI unit $\mathrm{W}/(\mathrm{m\,K})$ [124, 125].

convection

Energy transport also takes place through the macroscopic movement of a flowing fluid. This is called convection. In power electronics cooling, the heat is dissipated from the heat sink to the fluid and carried away by convection.

Convective heat transport depends on the material properties of the fluid and process parameters such as the flow velocity and the degree of turbulence. In engineering, the heat transfer between a flowing fluid and a solid is of great importance. This is called convective heat transfer. The fluid layer near the solid boundary (wall) is called the boundary layer. [123]

Heat convection is more complex to describe analytically than heat conduction due the heat transported through convection depends on many parameters such the geometry, heat transfer area, flow type (laminar or turbulence), etc.

Thermal radiation

The transport of energy by electromagnetic waves is called radiation. The resulting heat flux radiated by a body can be calculated with the Stefan–Boltzmann law described by J. Stefan [122]:

$$\dot{q}_w = \epsilon\sigma {T_w}^4 \tag{4.2}$$

where σ is the Stefan-Bolzmann constant ($\sigma = 5.67 \times 10^{-8}\,\mathrm{W/m^2K^4}$), ϵ is the emissivity of the radiating body, and T_w is the total temperature of the body.

The investigations in this work are carried out with solid bodies which are opaque to radiation. Furthermore, at the temperature values at which power electronics operate ($< 200\,^\circ\mathrm{C}$), radiated heat flux densities are usually negligible. Therefore, no heat transport by radiation is considered in this work.

4.1.2 Balance equations

Basically, all mathematical models for fluid mechanical calculations are balance equations for mass, momentum and energy. These equations cannot be solved analytically (except in greatly simplified, special cases). Alternatively, these equations can be solved numerically, considering the initial and boundary conditions.

The **continuity equation** has the following form:

$$\frac{\partial \rho}{\partial t} + \nabla \cdot (\rho \mathbf{v}) = \mathbf{0} \tag{4.3}$$

It describes the change in the mass over time in a volume element [126]. The symbol ρ in the equation represents the fluid density, and $\mathbf{v}$ signifies the velocity vector.

The **momentum equation** is based on Newton's second law. It represents the relationship between the momentum and the forces on a fluid element. It states that any change in the momentum of a body over time corresponds to the sum of all surface and volume forces. It can be expressed as follows:

$$\rho \left(\frac{\partial \mathbf{v}}{\partial t} + \mathbf{v} \cdot \nabla \mathbf{v} \right) = -\nabla p + \nabla \cdot \mathbf{T} + \mathbf{f} \quad . \tag{4.4}$$

The left side of equation (4.4) represents the change in momentum over time and the right side all forces acting on the fluid element. The symbol $\mathbf{f}$ denotes the volume force per unit volume. The expression $-\nabla p$ corresponds to the compressive forces and $\nabla \cdot \mathbf{T}$ to the frictional forces.

The **energy equation** for fluids can be derived from the first law of thermodynamics. It can be expressed for an incompressible flow as follows:

$$\rho \frac{\partial (e + \frac{1}{2}\mathbf{v} \cdot \mathbf{v})}{\partial t} + \rho \mathbf{v} \cdot \nabla (e + \frac{1}{2}\mathbf{v} \cdot \mathbf{v}) = \mathbf{v} \cdot (-\nabla p + \nabla \cdot \mathbf{T}) + \mathbf{v} \cdot \mathbf{f} + \nabla \cdot (\lambda \nabla T) \quad . \tag{4.5}$$

The left side of the equation (4.5) indicates the change in the total energy of a fluid element over time. The expression $\nabla \cdot (\mathbf{v} \cdot \mathbf{T})$ corresponds to the dissipation power of the surface forces and $\mathbf{v} \cdot \mathbf{f}$ to the power of the volume force. e is the specific internal energy and $\frac{1}{2}\mathbf{v} \cdot \mathbf{v}$ is the kinetic energy of the fluid. The energy equation can also be formulated

using the temperature (T) with the thermodynamic relationship $e = c_p \cdot T$

4.1.3 Conjugate Heat Transfer (CHT)

A conjugate problem is generally to be understood as meaning that several states or state variables depend on one another. All states influence each other. According to Zienkiewicz [127], there is a conjugate problem between two domains if

- no solution of one of the two domains can be found without depending on the solution of the other domain.
- No set of dependent variables can be eliminated to formulate the problem.

A conjugate heat transfer problem is a heat transfer between a solid and the adjacent fluid. The temperature fields of both subsystems, solid and fluid, are dependent on each other and must therefore always be determined simultaneously.

Heat transfer problems are often solved by specifying certain thermal boundary conditions. The standard conditions, such as a constant temperature or heat flux are not realistic, e.g. due to the temperature change along an interface. The temperature field at the interface is part of the solution of a larger system. It is therefore appropriate to calculate the temperature fields in the solid and in the fluid simultaneously [128].

A detailed description of the conjugate problems with examples and applications can be found in [127] and [129]. [130] is recommended specifically for conjugate heat transfer problems.

The boundary condition at the interface Γ between the two areas must fulfill the following FSI (Fluid-Solid-Interaction) conditions[131]:

$$T_s(x, y) = T_f(x, y) \tag{4.6}$$

$$\lambda_s \frac{\partial T_s}{\partial x} = \lambda_f \frac{\partial T_f}{\partial x} \tag{4.7}$$

The symbols "s" and "f" correspond to the solid (s) and fluid (f), respectively. These two conditions state that there is no discontinuities in the temperatures and heat fluxes at the interface. To ensure that both boundary conditions are met, these two boundary conditions are used for the two subdomains [132]. Since the interface condition includes the temperature distribution for both areas (subdomains), both subdomains must be solved simultaneously. It should be noted that the conjugate problem only exists due to the interface temperature. Once known, both domains can be solved independently and do not need to be solved simultaneously, since all boundary conditions are fully specified.

Equation (4.7) can be written explicitly as follows:

$$\lambda_s \frac{T_s - T_w}{\Delta_s} = \lambda_f \frac{T_w - T_f}{\Delta_f} \tag{4.8}$$

where Δ_f and Δ_s are the perpendicular distance to the interface in the fluid and solid region, and T_w is the wall (interface) temperature. By reformulating the above equation, the interface temperature can be obtained. This reads:

$$T_w = \frac{\lambda_s \Delta_f T_s + \lambda_f \Delta_s T_f}{\lambda_s \Delta_f + \lambda_f \Delta_s}. \tag{4.9}$$

By inserting the derived wall temperature (Eq. (4.9)) into Eq. (4.7), separate Neumann boundary conditions at the boundary wall are obtained for both regions. These are explicitly described as follows:

$$\left(\frac{\partial T}{\partial n}\right)_s = \frac{\lambda_s (T_s - T_f)}{\lambda_f \Delta_s + \lambda_s \Delta_f} \tag{4.10a}$$

$$\left(\frac{\partial T}{\partial n}\right)_f = \frac{\lambda_s (T_f - T_s)}{\lambda_f \Delta_s + \lambda_s \Delta_f} \tag{4.10b}$$

These two constraints correspond to the "conservative flux" constraint in "ANSYS CFD". Conjugate heat transfer calculations are performed by performing iterations after updating the boundary conditions until the desired number of iterations or accuracy is reached.

4.2 Computational Fluid Dynamics (CFD)

CFD is a numerical tool used to simulate fluid flow and heat transfer in a system. CFD calculations are essential in the design and optimization of cooling systems, as they provide detailed information on the fluid dynamics and heat transfer characteristics. CFD simulations can predict the temperature distribution, fluid velocity profile, and pressure drop in a system. The use of CFD simulations in cooling design has greatly facilitated the development of efficient and reliable cooling systems.

Finite volume method (FVM)

The Finite Volume Method (FVM) is a numerical technique used to solve partial differential equations (PDEs) in Computational Fluid Dynamics (CFD). The FVM divides the computational domain into discrete control volumes, which are typically polyhedral or hexahedral in shape. The control volumes are interconnected by faces, which form the

boundaries of the control volumes. The method then applies conservation principles to the control volumes to compute the flow variables such as velocity, pressure, temperature, and density, on the faces. Most CFD tools use FVM to determine the numerical solutions. The software used in this work ("ANSYS CFD") is based on FVM.

The FVM involves discretizing the Navier-Stockes equations governing the fluid flow into an algebraic from that can be solved using numerical techniques. The method applies the conservation laws of mass, momentum, and energy to each control volume to obtain the algebraic equations. The equations are solved iteratively, using an appropriate numerical method (such as the Gauss-Seidel method) to obtain the flow variables at each control volume. The method also uses boundary conditions to specify the flow variables at the boundary faces of the computational domain.

The FVM has several advantages over other numerical methods used in CFD. The method is conservative, meaning it preserves the mass, momentum, and energy in the system, which is essential in fluid flow simulations. It is also a flexible method that can handle complex geometries and boundary conditions. The FVM is also computationally efficient, since it only requires the computation of the flow variables at the control volumes and faces, making it suitable for large-scale simulations. More details about FVM and the discretization methods are described in different documents (e.g. [133, 134]).

Numerical Mesh

The accuracy of the CFD simulations heavily relies on the numerical mesh, which describes the discretization of the fluid domain into small control volumes or cells. The numerical mesh plays a crucial role in determining the accuracy, stability, and convergence of the numerical solution.

A good numerical mesh is crucial for obtaining accurate and reliable results in CFD simulations. The following are the criteria for a good mesh [135, 136]:

- Mesh Density: The mesh should have sufficient resolution to capture the important features of the flow field. The mesh density should be high in regions of high velocity gradients, boundary layers, and regions of interest, and low in regions where the flow is relatively uniform.

- Mesh Quality: The mesh should consist of well-formed and not skewed cells. Distorted cells can lead to numerical instability and inaccuracy. In addition, the mesh should be free of mesh tangles, overlaps, and self-intersections.

- Mesh Independence: The numerical solution should be independent of the mesh size. The solution should not change significantly upon refining or coarsening the mesh. Mesh independence is achieved when the numerical solution converges to a stable and consistent value with increasing mesh density.

- Computational Efficiency: The mesh should be computationally efficient. The number of cells should be minimized while maintaining sufficient resolution to capture the important flow features.

In CFD simulations, it is essential to perform mesh sensitivity analysis to determine the optimal mesh size and resolution required to obtain accurate and reliable results. Mesh sensitivity analysis involves varying the mesh density and analyzing the effect on the numerical solution. The optimal mesh size is the one that meets the criteria for a good mesh and provides accurate and reliable results at a reasonable computational cost.

Turbulence models

In engineering applications, predominantly turbulent flows are encountered. Turbulent flows show a stochastic flow movement. They are heavily entangled. The aim of the turbulence models is to simulate these turbulent fluctuations and swirls in the flow. The flow variables ϕ have unsteady fluctuations in space and time and can be broken down according to the Reynolds decomposition into a mean value $\overline{\phi}$ and the unsteady fluctuation $\phi^{'}$ [137] .

$$\phi = \overline{\phi} + \phi^{'} \tag{4.11}$$

Viscosity is increased by the turbulent effects.

$$\mu_{eff} = \mu + \mu_t \tag{4.12}$$

It is then the sum of the viscosity of the flowing substance μ and the turbulent viscosity μ_t.

For incompressible flows, the Reynolds stresses and Reynolds-average momentum equations can be written as follows, based on the material law [134]:

$$-\rho\overline{\mathbf{v}\mathbf{v}} = \mu_t \left[\nabla\overline{\mathbf{v}} + (\nabla\overline{\mathbf{v}})^T\right] - \frac{2}{3}\rho k I \tag{4.13}$$

$$\frac{\partial(\rho\mathbf{v})}{\partial t} + \nabla\cdot(\rho\overline{\mathbf{v}\mathbf{v}}) = \nabla\left(\overline{p} + \frac{2}{3}\rho k\right) + \nabla\cdot\left[\mu_{eff}(\nabla\overline{\mathbf{v}} + \mu_{eff}(\nabla\overline{\mathbf{v}}))^T\right] + \mathbf{f} \tag{4.14}$$

where $\overline{\mathbf{v}}$ is the mean velocity, $\overline{p}$ is the mean pressure, and k is the turbulent kinetic energy:

$$k = \frac{1}{2}\overline{v'^2}, \tag{4.15}$$

The turbulent viscosity μ_t depends on the turbulent kinetic energy k, the characteristic

frequency ω, the shear rate and the wall distance. This is modeled by additional equations. There are different turbulence models. k-ϵ, k-ω and k-ω-SST turbulence models are the most commonly used turbulence models. These models provide two additional transport equations to determine μ_t.

For k-ϵ, the turbulent kinetic energy k and the dissipation rate ϵ are introduced and calculated. The turbulent viscosity μ_t is defined as follows:

$$\mu_t = C_\mu \rho \frac{k^2}{\epsilon}, \tag{4.16}$$

where C_μ is the turbulence model constant ($C_\mu = 0.09$) [138]. In the k-ω model, the transport equations for k and the turbulent frequency ω are solved. The two quantities are related with the following equation:

$$\mu_t = \rho \frac{k}{\omega}. \tag{4.17}$$

The k-ω-SST turbulence model is a combination of the k-ϵ and k-ω model. The k-ω model is used in the boundary layer area, close to the wall, and the $k - \epsilon$ model in the area far away from the wall. Formulations of the transport equations for k and ω can be found in [139].

Boundary conditions

In order to solve the system of differential equations, the specification of the boundary conditions is necessary. There are mainly two types of boundary conditions [140]:

- Dirichlet conditions: For specifying fixed values at the boundaries.
- Neumann condition: For specifying gradients of the variable in the direction of the vector normal to the boundary.

Different situations can be modeled with these two types of boundary conditions, such as:

- Entry into the computational domain: At the inlet, the Dirichlet condition applies to the fluid velocity components and temperature. A Neumann condition of zero gradient is to be specified for the static pressure.
- Exit from the calculation area: A zero-gradient condition is specified here for the velocity components and the temperature. The static pressure takes a fixed value here.
- Walls: The no-slip condition applies to the velocity on the walls. That is, the fluid velocity is set to zero. A zero gradient condition is used for static pressure. There

are three types of boundary conditions to be distinguished for the temperatures and heat flow density on the walls [141, 142]:

- Boundary condition of the 1st type: The temperature at the boundaries of the considered body are given as a function of time and place.
- Boundary condition of the 2nd type: Here the heat flow density is specified as a function of time and location. Adiabatic walls also frequently occur; here the zero gradient condition applies to the temperature.
- Boundary condition of the 3rd type: This is a heat transfer from a solid body to a fluid or to another solid body. The temperatures of the fluid and solid at the interface are the same. The heat supplied to the fluid corresponds to the heat flow removed from the solid at the interface.

- Symmetry: The zero gradient condition applies to the symmetry surfaces.

yPlus

In CFD simulations, the yPlus (y^+) value is an important parameter that is used to determine the accuracy of the solution at the wall boundary. It is defined as the dimensionless distance from the wall to the first grid point in the fluid domain, normalized by the viscous length scale, which is the kinematic viscosity ν of the fluid divided by the wall shear stress. Mathematically, the y+ value can be expressed as:

$$y^+ = \frac{y \rho u_\tau}{\mu} \tag{4.18}$$

where y is the distance from the wall to the first cell of the mesh (near wall), ρ is the fluid density, u_τ is the friction velocity, and μ is the dynamic viscosity of the fluid.

Normally, the temperature gradient at the boundaries is much higher than that of the velocities. Therefore, in conjugate heat transfer (CHT) analysis, the $y+$ value plays an extra important role in determining the accuracy of the temperature resolution at the solid-fluid interface. This is because the y^+ value affects the heat transfer coefficient, which determines the rate of heat transfer between the solid and fluid domains. In CHT analysis, the y^+ value should be carefully chosen to ensure that the temperature and velocities profiles are accurately resolved at the solid-fluid interface. If the y^+ value is too large, the velocity and temperature gradient near the wall will be poorly resolved, leading to inaccurate heat transfer coefficient predictions. On the other hand, if the y^+ value is too small, the computational cost of the simulation will increase significantly, as more grid points will be required to resolve the near-wall region.

Generally y^+ values of $y^+ \sim 1$ ensure that the temperature profile is accurately resolved at the solid-fluid interface. However, a value of or less than 1 will increase significantly the

computational cost of the simulation. For minimizing time and storage space of the computational simulation, while having a good accuracy of the solution at the wall boundary, it's recommended to keep the yPlus (y^+) value less than 5. For CHT simulations $y^+ < 3$ is recommended due to smaller temperature gradients than those of velocity. In this work y^+ value is chosen to be less than 3 for accurate solution [134, 143].

The approach of the CFD simulation

The CFD simulations are carried out using the "ANSYS" software. The CFD solver "CFX" is the main solver for the simulations in this work due to its performance and its availability at the university. Ansys CFX provides the ability to model thermal fluid-structure interactions, which is needed in this work, since the generated heat is to be transferred from the electrical device to the fluid through solid materials. The CFD software includes 3D modeling features to create and modify geometries, automated meshing tools that generate the mesh for the CFD simulations and a preprocessor to define the boundary conditions and the solver setup. After the simulation, the CFD results are visualized using the CFD postprocessor included in the ANSYS package.

The design tool "DesignModeler" in the ANSYS package is used to generate the geometry. The design parameters are defined as variables by giving each design parameter a name. The variable names are automatically included in a table called "table of Design Points". Different values can be entered in the table in each column of each parameter. The second step is to setup the mesh parameters. The mesh size of every component and the number and size of interface layers (inflation) could be defined in the mesh tool included in ANSYS CFX. The mesh and all related parameters used in this work are discussed in next chapter.

The material properties of each element of the system are defined in the ANSYS CFX preprocessor. The material properties of solids and liquids are already shown in 3.3. In addition, all boundary conditions are defined for each body/surface. The system boundary conditions used are shown in 5.1.3. A constant power loss is specified on the chip as a boundary condition. A constant volumetric flow at the inlet (this is defined as input parameter in the table) and a zero-pressure boundary condition at the outlet are given. For all interface regions (walls), a conservative flow boundary condition is applied. All other walls are defined as adiabatic, i.e. no heat is released into the environment from the defined system of the cooling channel. These boundary conditions will be discussed in details in the section 5.1.3.The boundary conditions could also be specified as changeable parameters. For example, the flow rate at the inlet and the power losses of the devices can be defined as input parameters and changed later from the design point table. In addition, the turbulence model of the fluid flow should be defined to take into account the turbulence occurring in the liquid. Furthermore, the maximum number of interactions

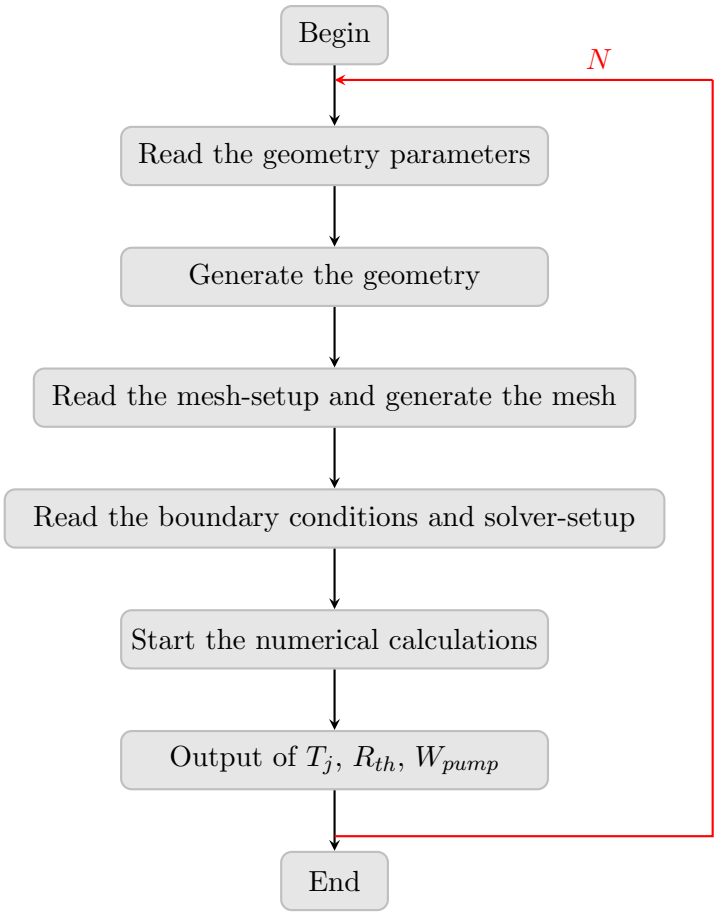


Figure 4.1: Procedure for the CFD simulation

and also the sufficient convergence of all calculated parameters are defined. All required settings are shown later in next chapter.

When all required settings are ready, the first numerical calculation can be started. The solver automatically shows the convergence behavior of the calculated variables. The simulation stops when the residuals reach a user-defined value. After the simulation has stopped, the post processor can be opened to visualize the CFD results. All required parameters can be defined there as output parameters and the software automatically enters these parameters in the table of design points. The output parameters are also defined as a function of other parameters, e.g. pumping power is defined as the product of flow rate and pressure drop. Later on, the output parameters can be easily monitored from the table instead of opening the post processor every time after each simulation. pressure drop (Δp), pumping power (W_{pump}), junction temperature (T_j), thermal resistance (R_{th}), differential outlet-inlet fluid temperature (T_{out-in}) and yPlus value ($y+$) are the main parameters monitored in this work.

The simulations are repeated according to the table of design points. ANSYS CFX starts reading the sorted geometry parameters from the table. Based on these parameters the geometry design is be regenerated. A new mesh is generated accordingly. This automated meshing algorithm generates an unstructured grid. The parameters of the mesh (mesh size, number and size of layers) are set in advance by the user. Then, ANSYS reads the defined boundary conditions and solver-setup (number of iterations, residual target, material properties, turbulence model). After reading all input parameters, ANSYS CFX starts the numerical calculations. When the calculation is complete, the output parameters are updated in the design point table. The solver iterates over the table of design points, and this process continues until all calculations are completed (N times). Figure 4.1 summarizes the workflow of the CFD simulation.

4.3 Experimental analysis

The experimental tests aim at validating the simulation results, and at demonstrating the coolers in realistic conditions. Hence, the primary focus is on two key metrics: thermal resistance and pumping power.

4.3.1 Thermal measurement (T_j, R_{th}, Z_{th})

Accurate measurement of thermal resistance and impedance is essential for proper thermal management of power semiconductor device, and for performance assessment of the coolers. This subsection explores the different methods used in this work for the thermal measurement and discusses the methodology involved.

Thermocouple onto the DUT

In this approach, the measurement of junction temperature (T_j) involves the use of a thermocouple that is directly mounted on top of the semiconductor die (see Figure 4.2). This method is relatively straightforward, and does not require extensive electrical connections or additional devices. However, it can be challenging to ensure that the thermocouple remains securely attached to the middle of the die. Even a slight movement of the thermocouple on the die can significantly impact the accuracy of the measured temperature, as there are often high temperature gradients present on the chip. Additionally, it is crucial to ensure good thermal contact between the thermocouple junction and the semiconductor die for accurate temperature measurement. Furthermore, there is a risk of damaging the semiconductor device due to the mechanical connection between the thermocouple and the chip. For particularly expensive devices, this method can be quite costly, as there is a possibility of damaging the device through the use of the thermocouple.

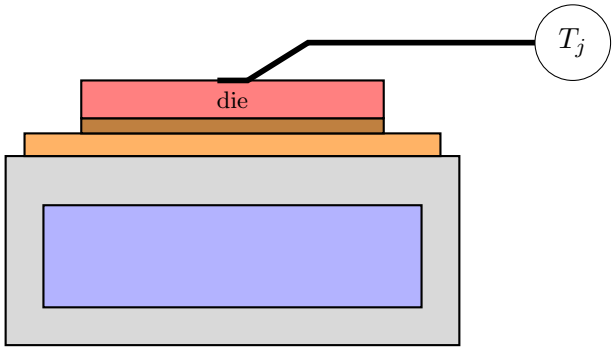


Figure 4.2: Schematic overview of the DUT while junction temperature (Tj) is meausred by a thermocouple

In order to calculate the thermal resistance (R_{th}), it is necessary to establish a reference temperature beside the junction temperature (T_j). In this particular study, the coolant's inlet temperature (T_{in}) is chosen as the reference. By obtaining the power losses (P_{loss}) of the device, the thermal resistance of the die can be calculated using the following equation:

$$R_{th} = \frac{T_j - T_{in}}{P_{loss}} \tag{4.19}$$

The power loss is simply obtained by multiplying the current and voltage across the device ($P_{loss} = V \times I$).

Thermal imaging

Here, a thermal imaging camera is employed to visualize the distribution of the temperature and to detect any area with inefficient cooling or hotspots.

As thermal imaging is based on measuring the intensity of the IR light emitted by the Device Under Test (DUT), the emissivity of its surfaces must be uniform and as close to 1 as possible (black body). Because the surfaces of the module have vastly different emissivity values (AlN, copper, aluminium, etc.), they must be painted with a thin coat of black paint that has an emissivity value close to one. For practical reasons, we use a photosensitive resin (Positiv 20, Kontakt Chemie) as the black paint: it produces a relatively thin coat (2–8 µm-thick), is easy to apply (spray) and to clean (it washes away with acetone).

An infrared (IR) camera (Fluke TiR125) is then used to measure the junction temperature. The IR camera is fixed above the DUT at a specific distance, as depicted in Figure 4.3. The camera manufacturer's software (Fluke SmartView) is utilized to process the images and generate a thermogram (2D). This enables a better understanding of the temperature distribution and facilitates the identification of hotspot areas on the module. The junction temperature (T_j) of the dies is extracted from the thermal camera image

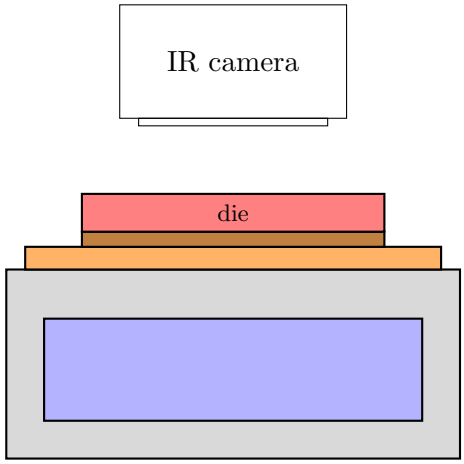


Figure 4.3: A Simple overview of the thermal imaging method for junction temperature measurement

using the maximum temperature acquired over each die's surface. The thermal resistance of a die is then calculated using eq. (4.19), with a thermocouple measurement for T_{in}.

One advantage of thermal imaging is that it allows for the visualization of the temperature distribution across the DUT, rather than just a single point measurement. This enables the detection of hotspots, as well as any unseen defects or unusual current distribution on the chip. However, it is important to note that this approach may have lower accuracy compared to other methods, such as using a specific thermal analyzer for measurement. One challenge is achieving an even coat of black paint on the module, as any unevenness can lead to inaccuracies. Furthermore, the actual emissivity value of the paint is not well controlled, especially after it has been exposed to high temperatures (for example if one of the semiconductor dies has heated so much it has burned the paint). Therefore, it is necessary to consider potential variations in emissivity when interpreting the temperature readings obtained from the device. As a result, in the rest of this work, thermal imaging mainly is used to measure temperature distributions that can be compared with simulation results, rather than to calculate R_{th} values.

Temperature-Sensitive Electrical Parameter (TSEP)

With this method, the junction temperature (T_j) of a semiconductor device is estimated from the measurement of one of its electrical parameters which exhibits a particular sensitivity to the temperature (TSEP). For example, it can be the collector-emitter voltage drop (V_{CE}) for IGBTs, or the source-drain voltage drop across the body diodes of MOSFETs (V_{SD}) [144].

Before conducting thermal measurements, the semiconductor device is first calibrated in an oven. The device is biased by a small reading current (a few milliamps, to avoid

significant heat dissipation), and its temperature is controlled by the oven. Because the device dissipates little heat, its junction and case temperatures can be considered identical. The junction temperature can therefore be simply measured with a thermocouple placed on the DUT. The calibration process also involves measuring the voltage drop between the collector-emitter (for IGBTs) or source-drain (for MOSFETs) at different temperature settings. A calibration curve is then generated, which relates the voltage drop V_{CE}/V_{SD} to the corresponding junction temperature (T_j). The calibration curve typically exhibits a linear relationship, with the voltage drop decreasing as the temperature increases.

The calibration and the following measurement are controlled using a "thermal analyzer" (Phase 12B, Analysis Tech). It is comprised of thermocouples, a power source, and data acquisition system/controller. A thermocouple is placed at the coolant inlet of the DUT to capture the inlet temperature. The power source supplies the necessary current to the device, while the data acquisition system records the temperature and power measurements. The control system switches rapidly between power injection (to cause the DUT to heat up), and reading current (to estimate the junction temperature of the DUT).

Figure 4.4 presents a schematic overview of the measurement setup. The load current is continuously supplied to the DUT through a switch board, with power being provided by a power supply. The load/heating current switch is controlled by a PC. A constant gate bias and sense current are also provided to the DUT from a current source. Following each power pulse, the voltage drop across the device is measured. Using the calibration curve obtained earlier, the thermal analyzer determines the junction temperature by measuring the voltage drop between the collector-emitter or source-drain terminals.

Once the junction temperature is determined, the thermal resistance can be calculated by dividing the temperature difference between the junction and inlet temperature by the power dissipation (eq. (4.19). The power loss of the semiconductor device is calculated as the product of collector-emitter voltage V_{CE} and collector current I_{CE} or source-drain voltage V_{SD} and drain current I_{SD}. The thermal analyzer (Phase12) monitors all needed values, using 4-point measurement for the voltage to improve accuracy, and calculates the thermal resistance automatically.

In addition to thermal resistance, the thermal impedance of the device can also be measured. Thermal impedance represents the dynamic behavior of the device's thermal response. It is calculated by dividing the temperature change by the power change over a specific time period.

Extended V_{CE}/V_{SD}-Method

The thermal analyzer requires that the heating current and the reading current share a common ground potential. This means that for series-connected dies, as with the multi-chip module presented in the last chapter, it is only possible to monitor the "bottom" die.

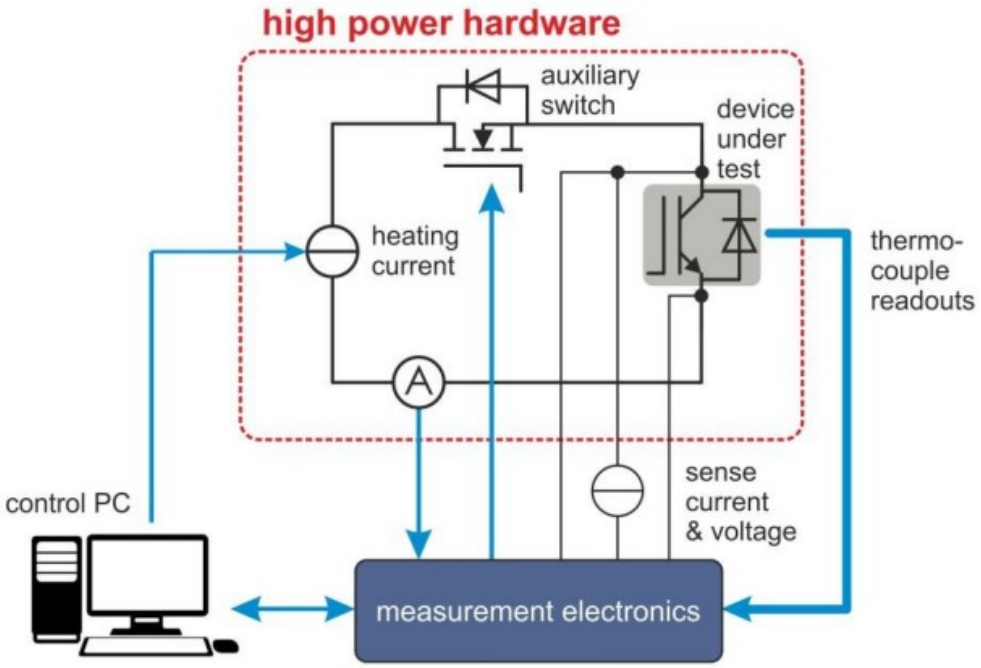


Figure 4.4: Thermal measurement system of the junction temperature and thermal resistance/impedance (R_{th}/Z_{th})

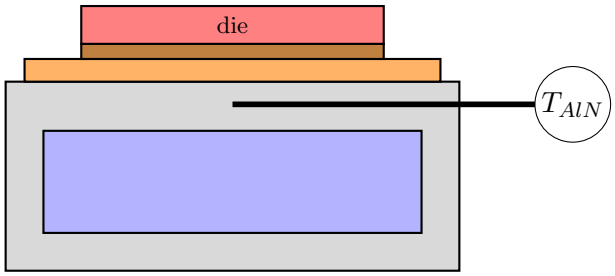


Figure 4.5: Overview of the AlN heatsink's temperature measurement location

Another way should be used to measure the thermal resistance of the other two chips.

Some of the AlN coolers are designed with a central hole in the top AlN layer, aligned with each die. This design allows for temperature measurement of the AlN heatsink beneath each semiconductor device using thermocouples. The location of the hole for temperature measurement is illustrated in Figure 4.5.

Because of the temperature linearity in the solids (we assume constant thermal conductivity over the temperature range considered), a constant temperature difference (ΔT_{j-AlN_i}) between the junction temperature T_j and the AlN temperature (T_{AlN_i}) under the die i is expected (for a multi-die module, assuming identical power dissipation in each die). Therefore, the thermal resistance of every die could be estimated using the following

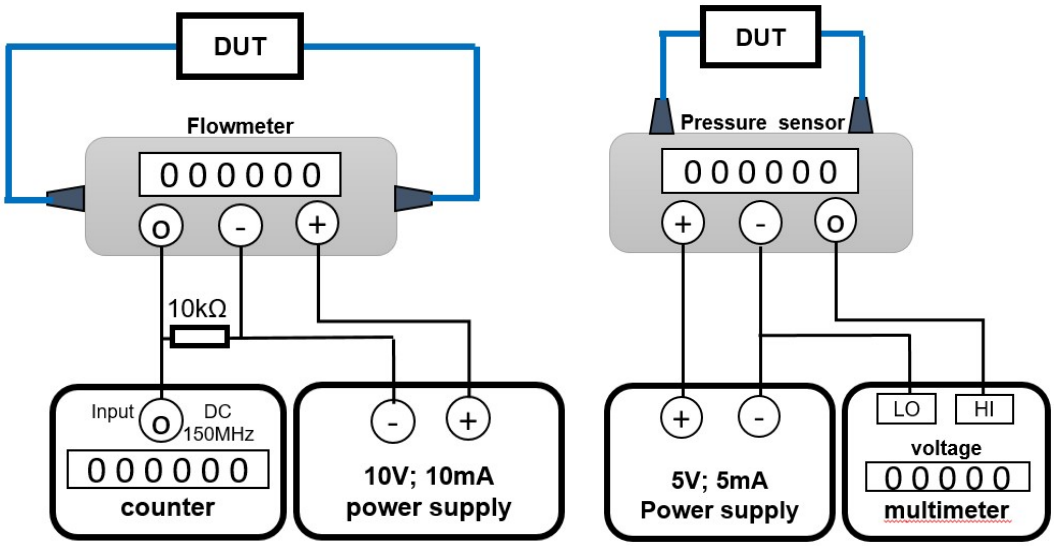
equation:

$$R_{thi} = \frac{T_{j_i} - T_{in}}{P_{lossi}} = \frac{T_{j_i} - T_{AlN1} + T_{AlN1} - T_{in}}{P_{lossi}} = \frac{\Delta T_{(j-AlN)_1} + T_{(AlN-in)_i}}{P_{lossi}} \tag{4.20}$$

4.3.2 pressure and flow rate measurement

Pumping power, a key parameter, is determined by multiplying the fluidic pressure drop by the flow rate.

A turbine flowmeter (V10982, RS PRO) is used to measure the flow rate. Inside the flowmeter is a Pelton wheel turbine, whose rotation speed is proportional to the flow rate. Each turn of the turbine generates an electrical pulse, so measuring the frequency of these pulses gives the flow rate. Figure 4.6a shows the electrical connections of the flowmeter to the digital counter used for readout.



(a) Flowmeter (b) Pressure drop sensor

Figure 4.6: The electrical connection of the flowmeter and pressure drop sensor

For the pressure drop measurement, a piezoresistive pressure sensor (MPX5010) is used. The sensor uses the change in electrical resistance of a material when stretched to measure the pressure. The connection of this sensor is depicted in figure 4.6b.

The frequency output signal of the flowmeter can be converted to L/min unit and pressure sensor's voltage signal to kPa unit using the conversion table in table 4.1. According to the datasheets, the pressure sensor exhibits an accuracy error of $\pm 5\,\%$, while the flow meter has a lower error rate of $\pm 0.25\,\%$.

Table 4.1: Conversion of the flow meter output signal in L/min and the pressure sensor output in kPas

Flow rate $\dot{V}$ [L/min]	Frequence [Hz]	pressure drop Δp [kpa]	Output voltage V_{out} [V]
0	0	0	0.2
0.5	15.5	1	0.65
1	32.3	2	1.1
1.5	49	3	1.55
2	65.7	4	2
2.5	82.5	5	2.45
3	99.2	6	2.9
3.5	115.9	7	3.35
4	132.6	8	3.8
4.5	149.3	9	4.25
5	166.1	10	4.7

4.4 Breakdown-Voltage (BDV) test

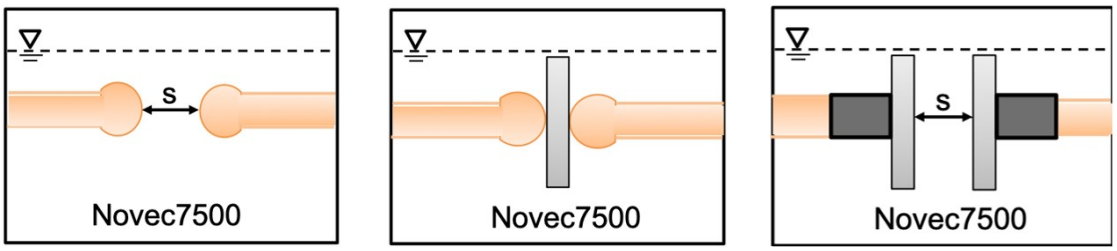
The Breakdown Voltage (VBD) test is a critical assessment method used to evaluate the electrical insulation strength and reliability of various components and systems. It measures the ability of a material or device to withstand high voltage stress without experiencing electrical breakdown. During the VBD test, a voltage is applied to the specimen, and it is gradually increased until it reaches a point where the electrical breakdown occurs.

In this work, VBD is measured to ensure the cooler designs will be able to sustain the rated voltage of the power module (20 kV), and that both insulating materials considered (AlN and Novec 7500) can operate together without any detrimental effect regarding electrical insulation.

This section gives an overview of the methodology and standards used. Furthermore, as this work mainly focuses on thermal aspects, VBD results are also presented in this section, together with a discussion about the insulating materials and the factors that can influence the breakdown voltage.

4.4.1 test configurations

The BDV tests are conducted following the guidelines of IEC60156:1995 using the commercially available BAUR DTA 100C set-up. A test cell is filled with the dielectric fluid "Novec 7500" during the measurements. The measurement methodology involves applying a continuously increasing voltage at a rate of 2 kV per second with a frequency of 60 Hz. Six series of tests are performed, with a waiting time of two minutes between each test and five minutes between every six series.



(a) Config. I (b) Config. II (c) Config. III

Figure 4.7: The three confifurations used for BDV test

Three different configurations are considered for the BDV measurements, corresponding to 3 different arrangements of the test cell (see Figure 4.7):

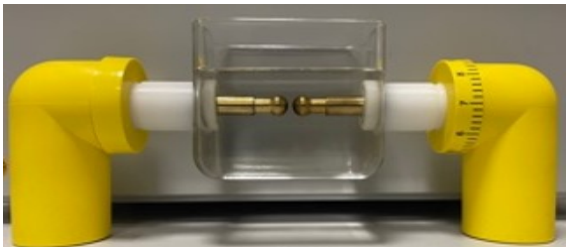
- Configuration I is used to measure the BDV of Novec 7500. Two spherical electrodes are used with a fixed distance of either 2.5 mm or 5 mm between them. This variation in distance helps observe the effect of the liquid's thickness on the BDV.
- Configuration II measures the BDV of AlN substrates. It uses the same spherical electrodes to measure the BDV of AlN substrates manufactured by CeramTec.
- configuration III allows for BDV measurement of two AlN substrates with Novec7500 in between, mimicking the design of the module where an AlN heatsink is filled with Novec 7500. One-side metallized substrates are used for the measurement. The spherical electrodes are removed, and the copper on the substrates serves as the electrodes. The measurement methodology is the same as in configuration I, only with the continuously increasing voltage applied at a rate of 1 kV per second.

The used fluid (Novec7500) remains unchanged and unfiltered both prior to and between test series. Testing for Configuration I is conducted one day after the fluid is poured into the cell. For Configuration II and III the test is performed directly after the AlN samples have been mounted. After each test, the BDV measurement is recorded as the voltage at which a breakdown occurs and the dielectric strength of the material is compromised. Figure 4.8 shows the test cell and some of the samples prepared for the tests.

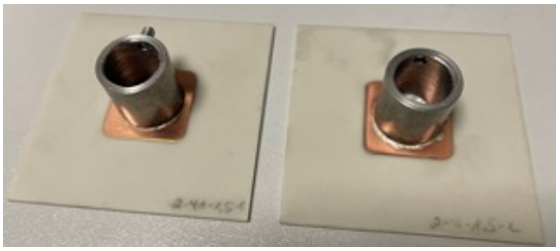
4.4.2 BDV results

Configuration I

The breakdown voltage (BDV) of Novec 7500 is assessed across gaps of 2.5 mm and 5 mm under two conditions: with and without stirring. The outcomes are illustrated in Figure 4.9. Initially, the test was conducted without liquid stirring, resulting in an average BDV of 60 kV with an associated error of ±8 kV. Upon widening the gap, the average BDV increased to 82.4 kV with an error of ±11 kV.



(a) test cell filled with Novec 7500



(b) Metallized AlN substrate samples

(c) BDV test device

(d) All prepared metallized AlN substrates

Figure 4.8: Test setup and the prepared samples

The implementation of liquid stirring leads to a small reduction in breakdown voltage (BDV), potentially due to the presence of contaminants and particles within the insulating liquid. Upon implementing liquid stirring, a marginal BDV reduction is observed. Specifically, for a 2.5 mm gap, the BDV is diminished to 52 kV (a reduction of 13 %), while for a 5 mm gap, it lowers to 80 kV (a 3 % reduction). More importantly, the incorporation of a stirring system provides a significant advantage by mitigating the variability of breakdown voltages. This advantage is particularly evident in scenarios involving lower breakdown voltages. For a 2.5 mm gap, the associated error is reduced from ±8 kV to ±4 kV when stirring is employed. Similarly, when using a 5 mm gap, the error decreases to ±8 kV during stirring, in contrast to the original error of ±11 kV without stirring.

The utilization of a stirring system effectively addresses error reduction, as indicated by the decreased standard deviations of the breakdown voltages. This enhancement can be attributed to the stirring system's capability to eliminate decomposition products and air bubbles that might form within the insulating liquid between the electrodes during prior breakdown tests.

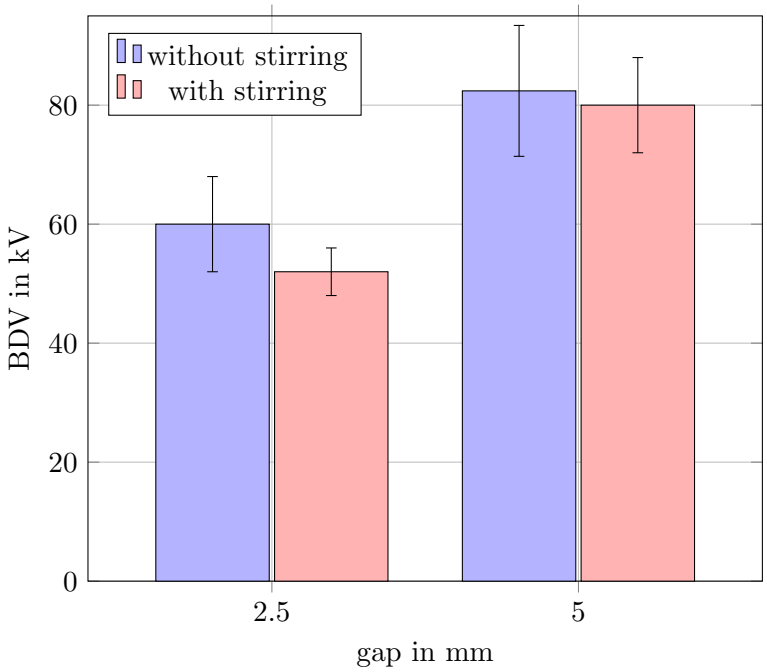


Figure 4.9: The measured BDV of Novec 7500 at 2.5 mm and 5 mm gap length, with spherical electrodes. Error bars correspond to ± 1 standard deviation value.

Configuration II

The BDV of AlN substrates with two different thicknesses, namely 1.5 mm and 3 mm, is presented in Figure 4.10. The bar graph illustrates the measured BDV values along with their corresponding average values and error ranges for each thickness. According to the graph, the average BDV for the 1.5 mm thick AlN film is found to be 35 kV ±4 kV. In contrast, the 3 mm thick AlN substrate exhibits an average BDV of 40.2 kV ±4 kV. Although the BDV increases with increasing thickness (as can be expected), this increase is very limited, as doubling the AlN thickness only results in a 15 % increase in BVD. Furthermore, the error bars in the graph demonstrate the variability in the measured BDV values, highlighting the importance of considering the error range when interpreting the experimental results.

Configuration III

With this configuration, three distinct samples set are considered. Due to a scarcity of metallized AlN substrates, only three measurements are executed for the 1.5 mm AlN thickness, four measurements for 2 mm AlN, and a more substantial ten measurements for the 3 mm AlN thickness. A constant 2.5 mm gap is maintained between the internal surfaces of the AlN substrates, corresponding to an inter-electrode distance of 5.5 mm with 1.5 mm AlN, 6.5 mm with 2 mm AlN and 8.5 mm with with 3 mm AlN.

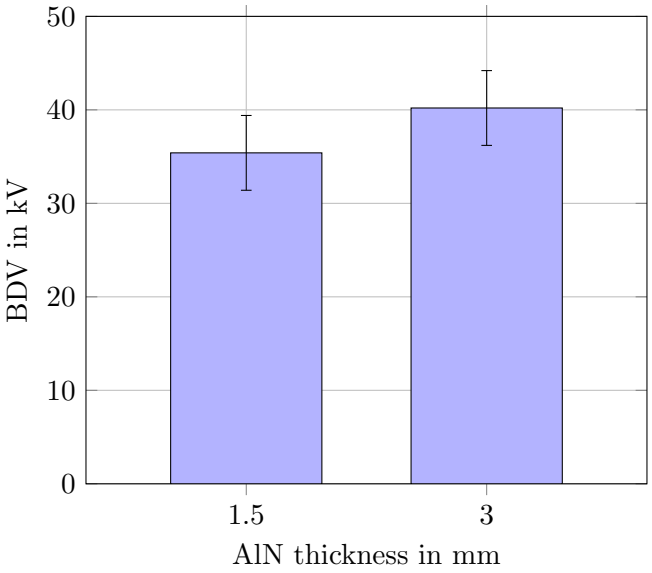


Figure 4.10: The measured break-down voltage for 1.5 mm and 3 mm AlN thickness. Error bars correspond to ± 1 standard deviation value.

Figure 4.11 illustrates the measured breakdown voltage (BDV) of this AlN/Novec 7500/AlN configuration. As anticipated, the BDV demonstrates an upward trend with escalating AlN thickness. An average BDV of 50.6 kV is achieved for 1.5 mm AlN thickness, increasing to 58.9 kV with 2 mm AlN and to 65.8 kV with 3 mm AlN thickness. The errors associated with these measurements remain consistently low across all three layout scenarios, measuring around 1.2 kV for the layouts with 1.5 mm and 2 mm AlN, and approximately 3 kV for the layout featuring 3 mm AlN. The diminished errors observed for the first two sets are likely due to the limited number of samples (only three or four measurements) available for analysis.

Conclusion

Table 4.2 provides a comprehensive summary of the measured data across the three configurations.

Upon initial examination, it is intriguing to note that the third configuration, which involves the combination of two AlN substrates and Novec 7500, exhibits BDV values either slightly lower or marginally higher than those of Novec 7500 alone (Config. I with 2.5 mm). However, the distinctive shape of the electrodes exerts a substantial influence on the BDV, owing to its impact on the distribution of the electric field. In Configuration I and II, spherical electrodes are employed, while for Configuration III, copper on the AlN substrates acts as the electrodes. The utilization of spherical electrodes fosters a more uniform electric field, contributing to elevated BDV values. Conversely, rounded rectangle

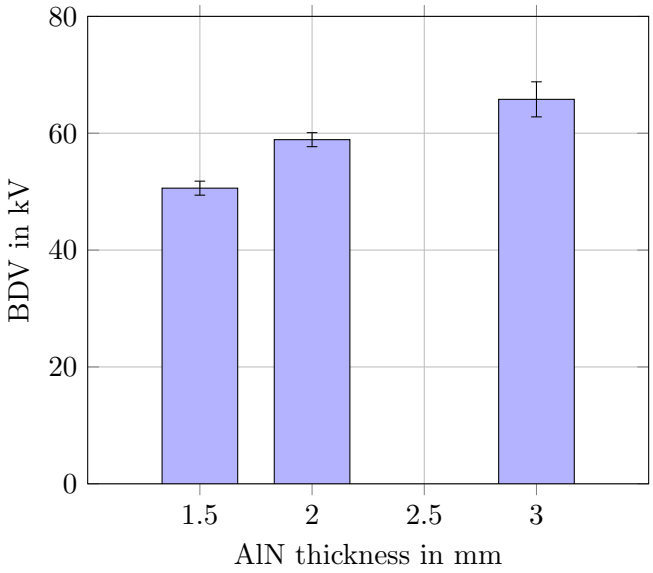


Figure 4.11: Breakdown voltage measurements for Configuration III, for a Novec gap of 2.5 mm surrounded by AlN substrates of different thicknesses. Because of the complexity of the test structure, only a limited number of samples were tested: 3 for 1.5 mm AlN, 4 for 2 mm AlN and 10 for 3 mm AlN. Error bars correspond to ± 1 standard deviation value.

copper electrodes (see Figure 4.8b) generate an uneven electric field distribution, resulting in intensified electrical stress at the electrode edges and diminished electric field in the center. This non-uniform distribution leads to reduced BDV due to the heightened electric field along the electrode edges. The constrained number of test samples accounts for the low standard deviation observed in Configuration III, as a greater number of tests are conducted on Configurations I and II.

The measurements indicate a significantly higher BDV than the desired threshold of 20 kV, even in the case of flat electrodes, which are more representative of the target application than spherical electrodes. This shows that the cooler structure considered in the remaining of this work can meet the requirements in terms of electrical isolation. Nevertheless, further investigations are imperative to assess the long-term blocking capability of Configuration III, ensuring the reliability and safety of the module.

4.5 Summary

The first part of this chapter presents the techniques crucial for achieving accurate Computational Fluid Dynamics (CFD) simulation results. The discussion encompasses pivotal aspects including boundary conditions, numerical mesh refinement (expressed by y^+), and the selection of an appropriate turbulence model. Notably, the $k-\omega$-SST turbulence

Table 4.2: Overview of measured BDV for the three configurations

Config.	detail	Av. BDV [kV]
I	2.5 mm gap; no stirring	60
I	2.5 mm gap; with stirring	52
I	5 mm gap; no stirring	82.4
I	5 mm gap; with stirring	80
II	1.5 mm AlN thickness	35
II	3 mm AlN thickness	40.2
III	1.5 mm AlN; no stirring	50.6
III	2 mm AlN; with stirring	58.9
III	3 mm AlN; no stirring	65.8

model, which amalgamates elements from both the $k-\omega$ and $k-\epsilon$ models, is chosen for its enhanced accuracy, and it serves as the cornerstone of the CFD simulations undertaken in this study.

The chapter further examines diverse methodologies for conducting thermal and hydraulic measurements in experimental analyses. These methods are strategically employed in varying manners, aligning with specific circumstances, the test vehicle, and the experimental setup.

Towards the conclusion of this chapter, a comprehensive exploration of Breakdown Voltage (BDV) measurements across three distinct configurations is presented. The findings reveal remarkably elevated BDV values, reaching up to 65 kV, a significant increase over the 20 kV target. However, it is emphasized that these investigations necessitate further scrutiny to substantiate the module's ability to withstand and sustain these elevated values during extended operational periods.

Chapter 5

Single-chip test vehicle

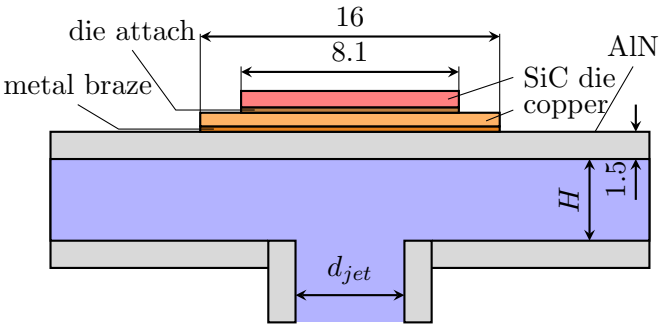
This chapter provides a comprehensive overview of the cooling methodology, detailing the optimization process of a single-die cooler using CFD simulations. It subsequently delves into the comprehensive analysis of experimental outcomes.

The chapter starts with a CFD analysis of a cooling channel, initially without the presence of pin-fins. Various coolants are compared in this context. Subsequently, a comparison is made between cooling performance with and without pin-fins. The impact of pin-fin structures on cooling performance is assessed, including an examination of different pin-fin structures and their arrangements.

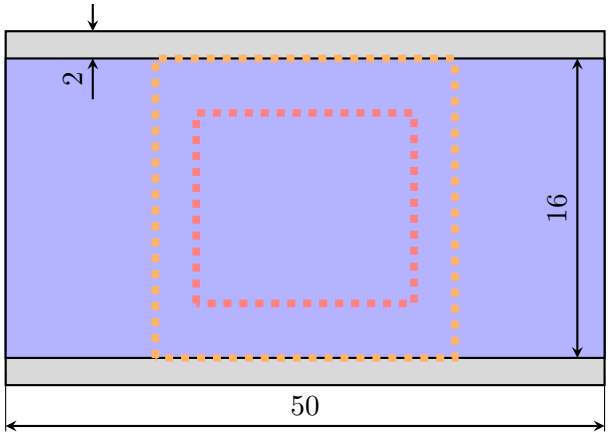
In order to ensure reliable insulation, the selection of a dielectric fluid as the primary coolant is made. However, this choice is subjected to a comparison with water and a water/glycol mixture. In the initial simulation phase, Novec 7500 is utilized as the coolant due to its high permittivity, effectively supporting the insulation objectives.

As the study transitions into the experimental domain, the fabrication of a dedicated test vehicle marks a significant step for comprehensive analysis. The ensuing discussion critically examines the experimental results, offering a thorough understanding of the implications and outcomes of the cooling strategy under examination. The experimental results are subsequently juxtaposed with the outcomes derived from the CFD simulations.

As previously indicated (please see section 3.1), the focus of the Computational Fluid Dynamics (CFD) calculations is on the cooling of a single-die module designed to manage the heat dissipation of an 10 kV SiC MOSFET measuring $8.1 \times 8.1\,\mathrm{cm}^2$. This specific MOSFET generates a thermal load of 125 W. It's crucial to note that subsequent to the CFD simulations, the availability of this MOSFET configuration in the commercial market has ceased. Consequently, the SiC MOSFET is replaced with a larger $9.1 \times 9.1\,\mathrm{cm}^2$ IGBT for the experimental investigations, taking on the role of the heat source.



(a) CAD parameter of the pure jet impingement cooler



(b) Cross section in middle of the channel under the chip

Figure 5.1: Structure considered for the design, showing the design parameters

5.1 Preliminary analysis: cooling performance of a smooth wall

Before investigating more intricate cooler setups, the analysis of a jet-impingement cooler devoid of integrated pin-fin structures is in order. This preliminary analysis demonstrates the impact of channel height and flow rate on factors such as velocity distribution within the channel, power element temperature, and the magnitude of pressure drop experienced within the system.

5.1.1 Overview of the design

One power semiconductor device with a base area of 8.1 mm × 8.1 mm is to be cooled. It dissipates 125 W of heat, which corresponds to a heat flux density of 190.5 W/cm^2. This heat should be dissipated through a cooling channel with a rectangular cross section. Figure 5.1 shows the jet impingement cooler with all the design parameters. The geometry has one inlet and two symmetrical outlets.

The analysis of this structure aims at finding how sensitive the temperature and the resulting pressure loss are to a change in the geometry parameters. The jet diameter d_{jet}, height H and width W of the channel can influence the fluid velocity and consequently the temperature of the device and the pressure drop. The channel has a total length of 50 mm and a variable width of W mm. The copper pad has the same size as the channel width to help spread the heat over the entire channel width, and it is considered to be square. The top AlN layer has a thickness of t mm. All other walls have a fixed thickness of 2 mm. The power electronic device (8.1 mm × 8.1 mm) is centered into the middle of the channel between the two outlets and directly under the jet impingement.

The height, the jet diameter and the flow rate are variables of our parametric study. The flow rate is investigated between $2\,\mathrm{L/min} \leq \dot{V} \leq 6\,\mathrm{L/min}$, the channel height H between 2 mm and 6 mm and the jet diameter ranges between $2\,\mathrm{mm} \leq d_{jet} \leq 6\,\mathrm{mm}$. These are the main parameters that define how strong the jet hits the bottom surface of the AlN under the chip, because these define the fluid velocity there. These parameters are summarized in table 5.1.

Table 5.1: Geometry parameters of the pure channel

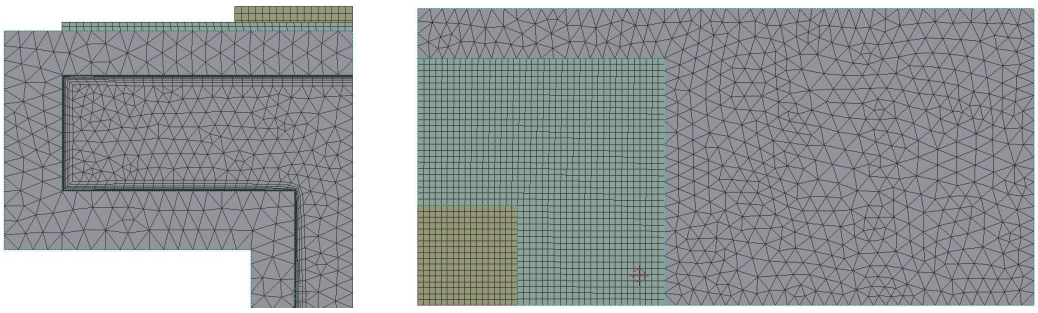
Design parameter	Interval
Channel height H in mm	$2 \leq h \leq 6$
Jet diameter d_{jet} in mm	$2 \leq d_{jet} \leq 6$
Volumetric flow $\dot{V}$ in L/min	$2 \leq \dot{V} \leq 6$

The other geometric parameters are as follows: the semiconductor device is considered to be 500 µm-thick; it is attached to a 300 µm-thick copper layer through a layer of sintered silver measuring 100 µm in thickness; the copper layer is brazed to the AlN cooler through a 10 µm thick layer of active solder. The material properties of the materials are presented in chapter 3.

5.1.2 Numerical mesh

ANSYS CFD is based on finite volume method, which require a discretization of all the system regions (the solids and the fluid) to solve the Navier-Stokes equations. The resolution of the velocity and temperature gradient during the conjugate heat transfer simulation depends on the mesh quality. A value of $y^+ < 3$ (see subsection 4.2) is set as a target for the simulations. Figure 5.2 shows an example of a numerical mesh used in this work. Thanks to symmetry, only a quarter of the geometry is simulated for jet cooler and a half for the channel flow cooler.

Due to high gradients in the temperature and velocity fields at the fluid-solid interface, inflation mesh layers are applied there. The first layer has a thickness of 5 µm and growth



(a) side view at symmetry plane (b) top view

Figure 5.2: Meshing of the geometry for the CFD simulations

rate of $g_l = 1.4$. 10 layers (N_l) are applied at the boundary. Because the die, copper and die attach are thin, they are meshed with 100 µm elements and the 10 µm-thick metal braze with 10 µm elements. An element size of 500 µm is set up for the AlN walls as well as for the fluid. The AlN and liquid with are meshed with tetrahedrons elements and all other components with hexahedron elements. Table 5.2 summarizes the mesh parameters.

Table 5.2: Parameters used for meshing the geometry

Layer material	cell size	Interface layers
Fluid	0.5 mm	$N_l = 10$, $g_l = 1.4$, t_l=0.005 mm
AlN	0.5 mm	-
Copper	0.1 mm	-
Metal braze	10 µm	-
Die attach	0.1 mm	-

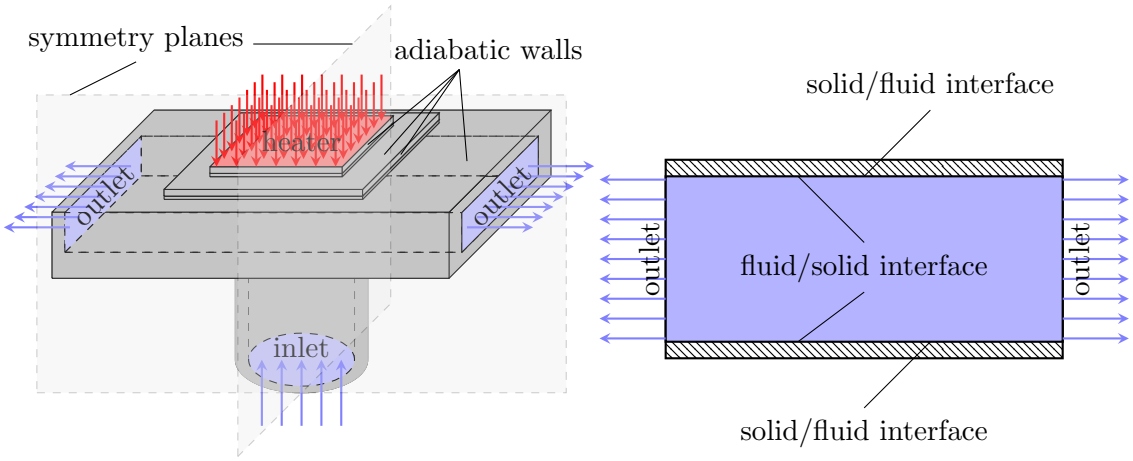
5.1.3 Boundary conditions

The boundary conditions of the problem are defined according to figure 5.3. No-slip condition applies to all walls. This means that the velocity takes a zero-value there because the walls are fixed and not moving. A fixed value for the mass flow, and thus for the fluid speed, is specified at the inlet. At the outlet, the velocity gradient in the normal direction is zero due to the free flow. The initial temperature at the fluid inlet is given as $T_{in} = 313.15\,\mathrm{K}$ (40 °C). All outside walls (all gray walls in figure 5.3) are considered to be adiabatic. This means that the temperature gradient in the normal direction with respect to the walls is be zero ($\frac{\delta T}{\delta x}$). The temperatures of the fluid and of the solid are the same at their interface ($T_f = T_s$). The heat flow supplied into the fluid must correspond to the heat removed from the solid (conservative heat flow). This boundary condition must be

Table 5.3: Boundary conditions

Boundary	velocity v	pressure p	temperature T
inlet	constant mass flow	0	313.15 K
outlet	zero gradient (0,0,0)	calculated	calculated
adiabatic	-	-	zero gradient (0,0,0)
fluid/solid interface	fixed value (0,0,0)	calculated	conservative flux
solid/fluid interface	-	-	conservative flux
heater	-	-	uniform heat 125 W
symmetry planes	zero gradient (0,0,0)	zero gradient (0,0,0)	zero gradient (0,0,0)

specified twice: as a fluid/solid and solid/fluid boundary conditions (see figure 5.3). Table 5.3 summarizes the boundary condition for the CFD simulations.



(a) Boundaries and symmetry planes

(b) Cross section at channel flow

Figure 5.3: Definition of the boundary conditions

5.1.4 Convergence behaviour

Good convergence of the numerical solution is important to provide good quality results. The smaller the numerical error, the higher the calculation accuracy. Figure 5.4 shows an example of the residual curves for the calculations with the $k-\omega$-SST turbulence model. It can be seen that the residuals all converge, as they keep decreasing from one iteration to the next. The relative convergence tolerance is set to a value of 5×10^{-5} for the pressure, 10^{-6} for the temperature and 5×10^{-4} for all the other quantities. Due to the sufficient accuracy of the solution, the maximum number of iterations for the next simulations is set

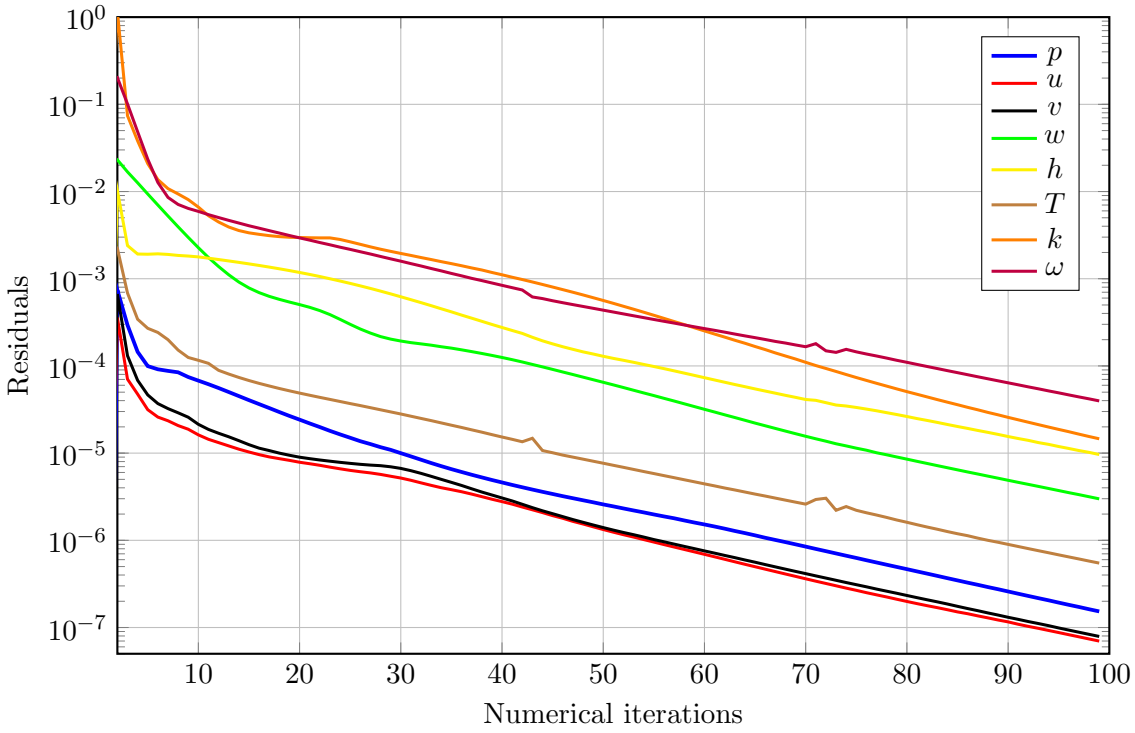


Figure 5.4: Evolution of the residuals over numerical iterations (pressure p, velocity components (u, v, w), enthalpy h, temperature T, kinetic turbulence energy k and the specific dissipation rate ω)

to 100 steps. The convergence behaviour for the calculations changes with different CAD parameters. However, small errors are achieved for all the calculation variants.

5.1.5 Validation

Before analysing the numerical results, the accuracy of the CFD solution must be ensured. Pressure is an important quantity for this work and it is part of the Navier-Stokes and energy equations. It depends on the velocity and temperature of the fluid. Therefore, an accurate calculation of the pressure is an indication of the quality of the model. Here, the pressure drop predicted using the CFD model is compared with that of an empirical model (considering water as the cooling fluid, as it is the fluid used for most empirical correlations). Using the Prandtl's equilibrium between the pressure loss and the shear stresses, the following equation applies the pressure drop in a pure channel of length L [145]:

$$\Delta p = \kappa \frac{L}{D_h} \frac{\rho_f {v_m}^2}{2} \quad \text{with} \quad D_h = \frac{4A_{flow}}{U_{flow}}. \tag{5.1}$$

With v_m is the average velocity in the channel. The hydraulic diameter D_h is the ratio between the cross-sectional area A_{flow} and the perimeter U_{flow} of the flow multiplied by four. According to Blasius [146], the pressure loss coefficient *kappa* is directly dependent on the Reynolds number and can be calculated for turbulent flow in a smooth channel with the following relation:

$$\kappa = \frac{0.3164}{Re^{0.25}} \quad \text{with} \quad Re = \frac{v_m D_h}{\nu} \tag{5.2}$$

where ν is the kinematic viscosity of the fluid. This equation applies to circular pipes as well as rectangular ducts in case of turbulent flow [147]. The empirical correlation of Blasius is valid for turbulent flow below $Re = 80000$. In pipes, turbulent flow occurs from a Reyolds number of $Re > 2300$ [148]. All calculation for the validation are executed in the range of $3700 < Re < 44000$. Figure 5.5 shows the CFD results for the pressure loss compared with the empirical equation (5.1). The comparison is done for different flow rates, and shows good agreement between the CFD and empirical models. The slight deviation (<5 %) can be attributed to the temperature change in the fluid, which is not considered in the empirical model. Furthermore, a constant fluid velocity across the inlet is defined in the simulation while the empirical calculation applies just for fully developed turbulent.

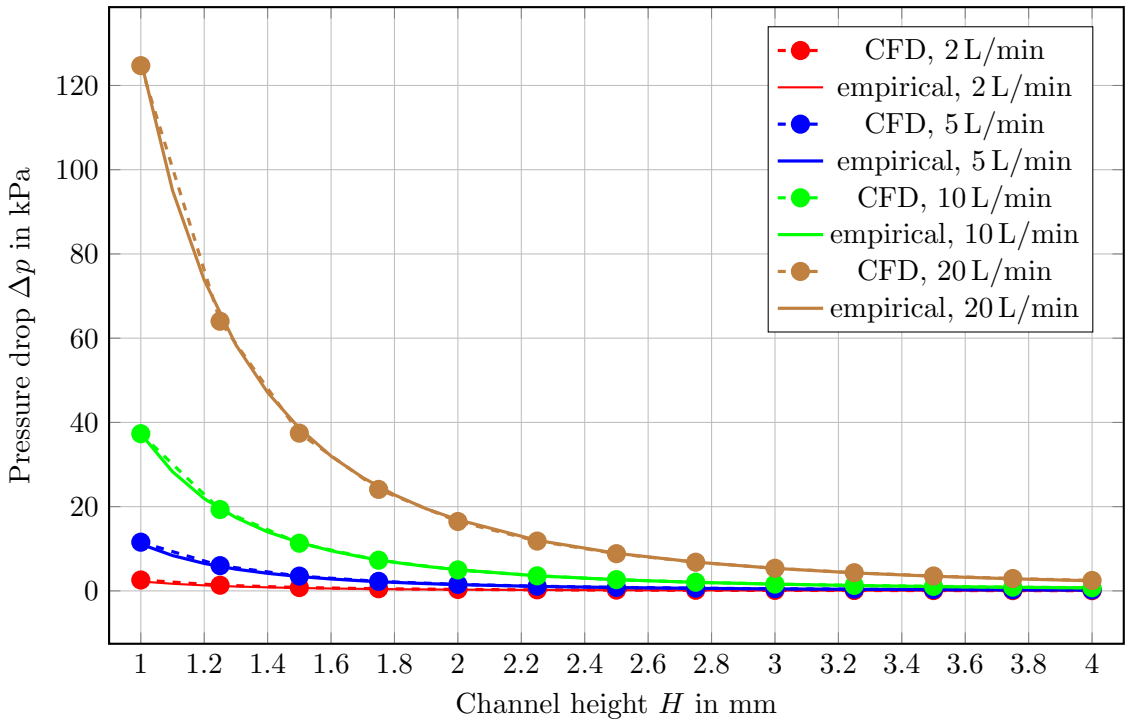
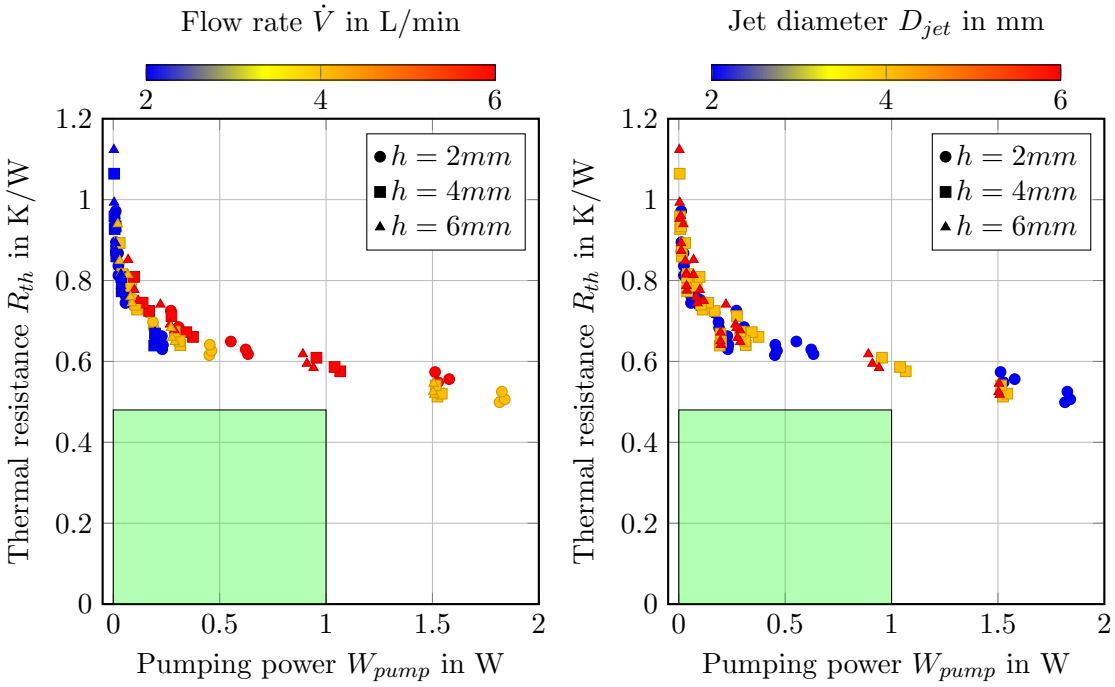


Figure 5.5: Comparison between the numerical and empirical pressure drop results as a function of the channel height h at constant water volume flow

5.1.6 Evaluation of the CFD results

In this section, the influences of the jet diameter d_{jet} and the height H of the rectangular cooling channel on the temperature and the pressure drop Δp (pumping power) are examined.

Figure 5.6 shows the CFD results for the jet impingement cooler with smooth walls. The thermal resistance R_{th} is calculated based on the junction/maximum temperature of the die. Both graphs present the same simulation results but with different color maps: the points are colored after volumetric flow in figure 5.6a, and after jet diameter in figure 5.6b. The green area in the figures is the target performance area ($R_{th} < 0.48\,\mathrm{K/W}\,\&\,W_P < 1\,\mathrm{W}$). Each point in the figures represents a simulation with different design parameters. The different marker shapes correspond to different channel heights h.



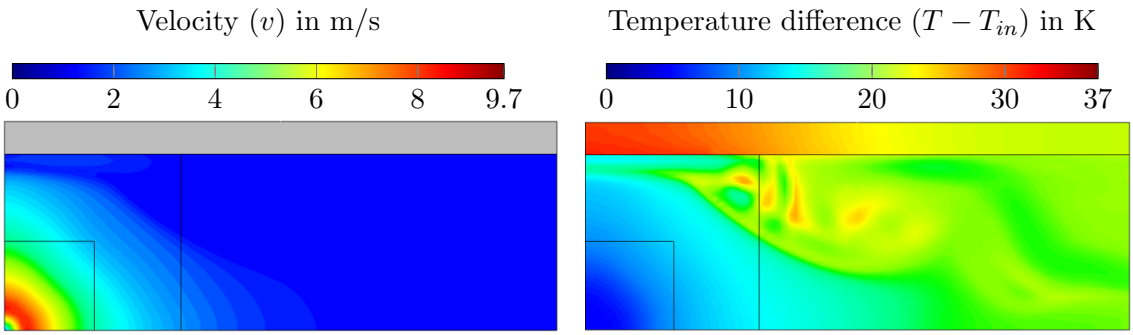
(a) colored after flow rate ($\dot{V}$)

(b) colored after jet diameter (D_{jet})

Figure 5.6: Thermal resistance as a function of pumping power, for different heights, width and jet diameter (CFD simulations, for Novec 7500)

The study is performed for three different channel height ($h = 2, 4, 6\,\mathrm{mm}$), three jet diameters ($D_{jet} = 2, 4, 6\,\mathrm{mm}$) and three flow rates ($\dot{V} = 2, 4, 6\,\mathrm{L/min}$). As expected, higher flow rates result in lower thermal resistance due to higher velocities and more turbulence. A smaller jet diameter accelerates the liquid flow upon hitting the top surface under the die, also resulting in lower thermal resistance. However, with this simple construction (no pin-fin structures), the target area cannot be reached.

The special feature of jet impingement is that the liquid velocity can be manipulated by changing the jet diameter. Figure 5.7 shows the velocity and the temperature at 20 µm distance from the upper wall. Figure 5.7a shows that the fluid velocity at the bottom of die is higher than anywhere else in the structure. The fluid velocity near the walls goes to zero (see figure 5.7a right side). Consequently, the temperature follows the opposite distribution to the velocity. The cold liquid from the inlet hits the AlN surface with high speed and moves on to the outlet, reducing its speed until it goes almost to zero far away from the jet, which allows the fluid to heat up. The fluctuation of the temperature in figure 5.7b is due to the turbulences and fluid mixing caused by high velocities.



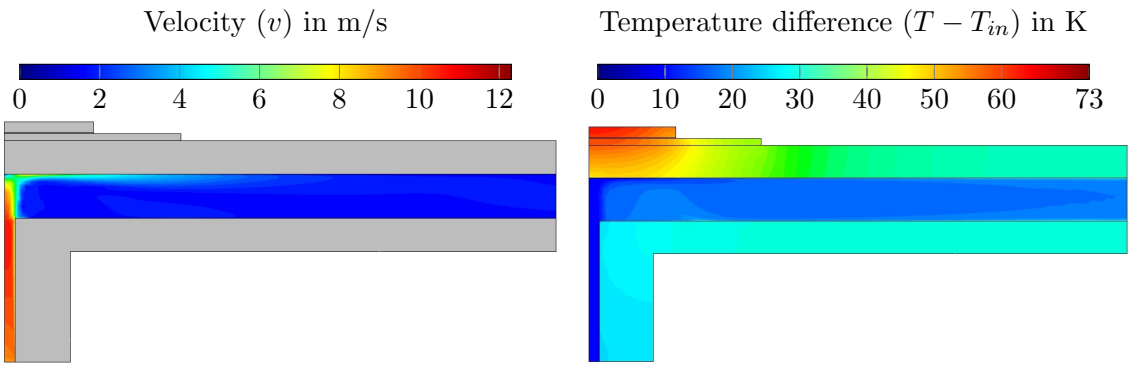
(a) Velocity (b) Temperature

Figure 5.7: Velocity and temperature near wall (20 µm from the upper wall) at 2 L/min (CFD simulations, for Novec 7500)

Figure 5.8 shows velocity and the temperature distributions at the middle of the system (the side view). This view confirms that the jet hits the surface at high speed. Fluid velocity decreases towards the outlet down to almost zero. Figure 5.8b shows the corresponding isothermal contours. The die is the hottest part of the system. The heat flows from the die to the coolant through the solid layers. Due to the smooth heat transfer surface, the target temperature of 100 °C (Temperature difference of 60 K with the 40 °C inlet temperature) is not achieved.

5.2 Optimization of the cooler with pin-fins

As was seen in the previous section, achieving a thermal resistance of $R_{th} = 0.48\,\mathrm{K/W}$ is not possible with a cooler with smooth walls. In order to increase the heat transfer surface between the fluid and the solid, pin-fin structures can be placed placed into the channel. In addition to a larger heat transfer area, pin fins offer higher fluid velocities by restricting the flow. Pin fins also lead to more vortexes (turbulence) in the channel, increasing the heat transfer further. This section shows the effect of the pin-fins on the cooling performance compared to a cooler with smooth walls. Different design parameters are



(a) Velocity (b) Temperature

Figure 5.8: Velocity and temperature at the symmetry plane in the middle of the channel at 2 L/min (CFD simulations, for Novec 7500)

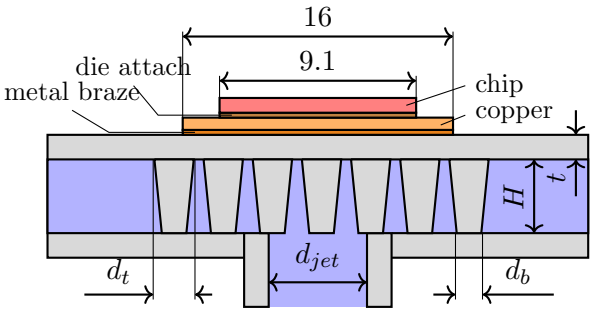
investigated in order to optimize cooling performance. Two cooling concepts are examined: jet impingement and channel flow. Initially, a jet impingement cooler is investigated and subsequently compared with the channel flow cooler.

5.2.1 Geometry

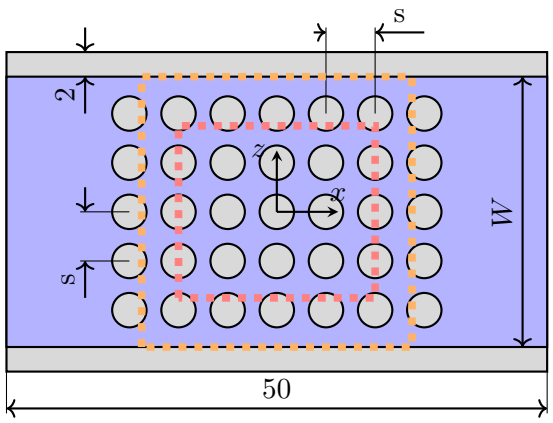
The geometry of the Conjugate Heat Transfer (CHT) problem is presented in figure 5.9. The pins in the heat sink have a conical shape with bottom d_b and top d_t diameters. The pins can be also cylindrical when both diameters are equal ($d_b = d_t$). The cooling system has one inlet (the jet) and two outlets located on the left and right sides. The cooling channel has a length of 50 mm, a width of W mm, and the pins have a distance of s mm between their axes. The top layer thickness of the AlN heat sink (t) can be varied, while all other walls have a constant thickness of 2 mm. The inlet has a jet diameter of d_{jet}. The 8.1 mm × 8.1 mm semiconductor is located in the middle of the heat sink directly under the jet.

5.2.2 Setup of the numerical simulation

The same calculation setup used here is the same as in the previous section. In particular, the mesh has 10 inflation layers between the pins and the fluid. This means that the mesh is designed to have a high level of refinement near the pins, where the velocity gradients are the highest to accurately capture the boundary layer. A parameter y^+ value of less than 3 is typically used to ensure accurate modeling of the turbulent boundary layer. In this case, the mesh has been tested to ensure that the y^+ value stays below 3 for flow rates up to 5 L/min. A cross section of the mesh at the middle of the channel is shown in figure 5.10. The boundary conditions and convergence criteria are those described in sections 5.1.3 and 5.1.4.



(a) Cross section (side view)



(b) Cross section in middle of the channel under the chip

Figure 5.9: Drawing of the cooler with pin fin structures, showing the design parameters.

Table 5.4 shows the range of design parameters used for the CFD simulations of the heat sink design. The spacing between the pins is constant at 1 mm, which is the smallest distance that can be manufactured (the pin pitch s is adjusted between 2 mm and 4 mm according to the pin diameter to ensure a spacing of 1 mm). This small distance is chosen to ensure we have as many pins as possible under the chip. This provides more heat dissipation surface and also increases the velocity of the fluid, allowing more turbulence in the flow and a better heat transfer coefficient.

5.2.3 Effect of the pin fins

As mentioned in the previous section, beside the flow rate $\dot{V}$, five design parameters (d_{pins}, H, d_{jet}, W and t) are investigated to obtain the optimum design. To simplify the optimization process, the top AlN thickness and channel width W remain initially constant with $W = 16$ mm and $t = 1.5$ mm. Additionally, cylindrical pins are considered ($d_t = d_b = d_{pins}$). Figure 5.11 shows the corresponding simulation results. The graph displays a large number of points, each corresponding to a different set of design parameters. The points on the graph are colored according to the flow rate. The green area on the graph

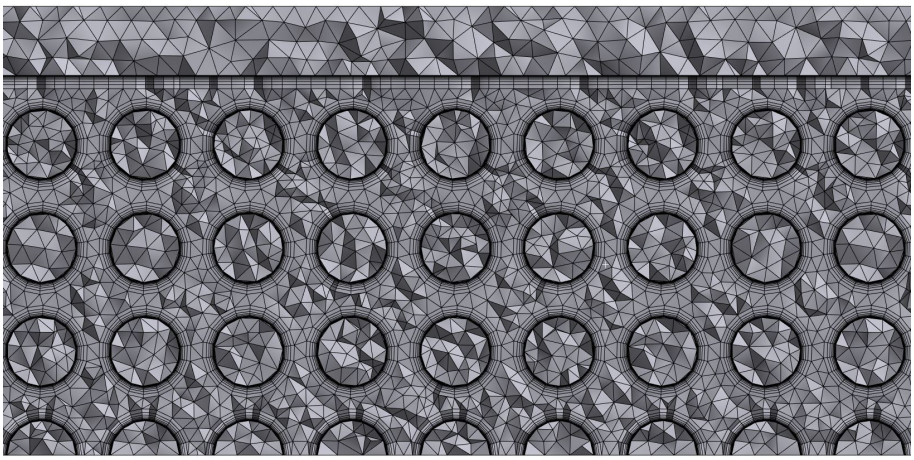


Figure 5.10: Example of mesh around the pins

Table 5.4: Geometry parameters of the cooler with pin-fin structures

Design parameter	Interval
Bottom pin diameter d_b in mm	$1 \leq d_b \leq 3$
Top pin diameter d_t in mm	$1 \leq d_t \leq 3$
Height H in mm	$1 \leq H \leq 9$
Jet diameter D_{jet} in mm	$5 \leq d_{jet} \leq 9$
Channel width W in mm	$10 \leq d_{jet} \leq 22$
Number of pins in x-direction N_x	$5 \leq N_x \leq 9$
AlN thickness t in mm	$1 \leq t \leq 5$
Volumetric flow $\dot{V}$ in L/min	$1 \leq \dot{V} \leq 5$

represents the desired target for the design, with a pumping power lower than 1 W and a thermal resistance lower than 0.48 K/W. Finally, the points are also differentiated by the marker shape, according to the pin diameters. As for the smooth wall case (shown with empty markers in Figure 5.11), the graph shows that higher flow rates generally lead to better thermal resistance, but also result in higher pumping power. However, the cooler with pin fins can achieve much lower thermal resistance that that with smooth walls for the same pumping power. The target area can easily be reached with pin fins.

Figure 5.11 shows that a pin diameter of 2 mm leads to the lowest thermal resistance. Smaller pins offer smaller heat transfer area affecting the heat disssipation. Because of the constant 1 mm spacing between the pins, the pin density does not scale proportionally to the pin diameter. For small pin diameters, this translates into comparatively smaller pin cross section (for heat transfer) and smaller heat exchange surface with the fluid. On the opposite, very large pins reduce the flow, blocking the jet inlet and therewith increasing the the pumping power.

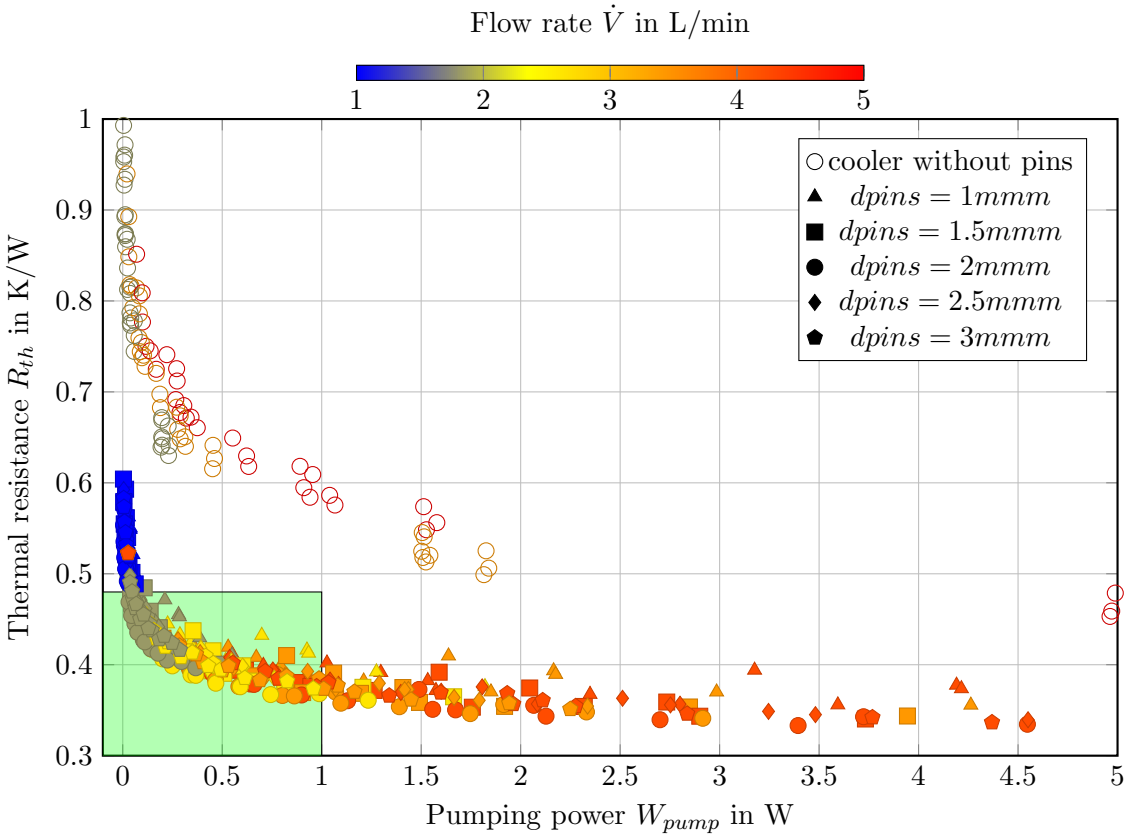


Figure 5.11: Thermal resistance as a function of pumping power with different pins diameter d_{pins}; colorbar: flow rate $\dot{V}$ (CFD simulations, for Novec 7500)

Figure 5.12 shows the same CFD results as in figure 5.11. This time, the colorbar is scaled according to the jet diameter and the markers shape correspond to three different height to pin diameter ratios H/d_{pins}. Because of higher velocity and more turbulence, smaller jet diameters lead to lower R_{th}, at the expense of a larger pumping power. This is particularly obvious outside the target interval (green area), for high pumping powers. However, considering the target area, the advantage of a small jet diameter is less obvious, with 6 mm to 8 mm jet configurations sometimes on the pareto front. Bigger pins (higher H/d ratio) results in a larger heat dissipation area and reduces the pressure drop due to the bigger fluid volume in the channel. However, higher channel reduces the velocity degrading the cooling performance. The pareto front of the pins with $H/d = 1$ is the worst due to the smaller dissipation volume and higher pumping power. For a low pumping power, a height to pins diameter ration of 3 show the best results with lower thermal resistance. A ratio of $d/h = 2$ is the best in case of higher pumping power. Since the target is to reduce the thermal resistance by lower pumping capacity and flow rates, the ratio of $H/d = 3$ is considered to be the best design. Beside that higher channel is preferred in this work,

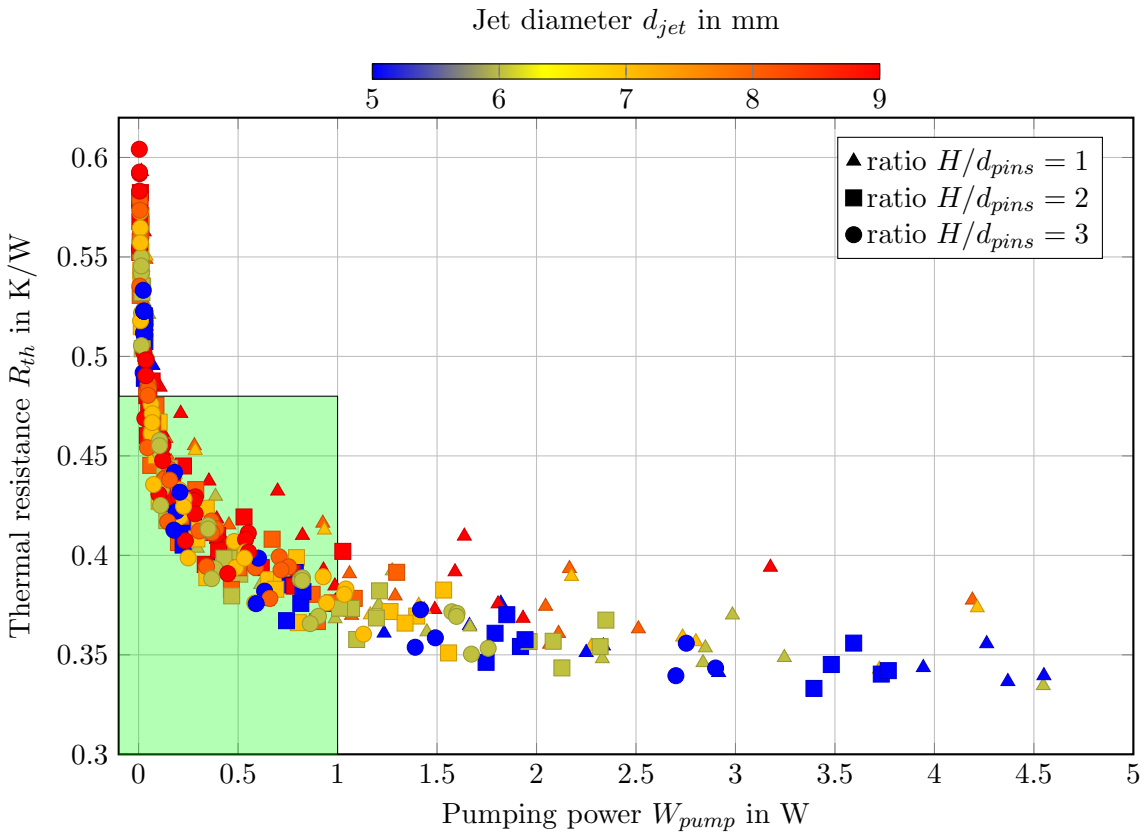


Figure 5.12: Thermal resistance as a function of pumping power with different height to pin diameter ratios (H/d_{pins}); colorbar: jet diameter d_{jet} (CFD simulations, for Novec 7500)

because they offer more insulation distance from the top side (at semiconductor device) to the bottom side of the heat sink (the potential ground should be located at the bottom).

According to the previous paragraphs, we can set $d_{pins} = 2\,\text{mm}$ and $H/d_{pins} = 3$ ($H = 6\,\text{mm}$), and start investigating the effect of the channel width W. Figure 5.13 shows the numerical results for three different channel widths, ranging from 10 to 22 mm. While a clear reduction in thermal resistance can be observed when moving from 10 to 16 mm, it is much less obvious between 16 and 22 mm. Therefore, no wider channel are investigated and 22 mm channel width is considered to be the best design parameter. Due to higher material and manufacturing costs of minor improvements, For practical reasons, and because it causes only a very small increase in thermal resistance $W = 16\,\text{mm}$ is preferred for further investigation for the single die module.

The points in figure 5.13 are coloured after the number of the pins in the x-direction (N_x). More pins in the channel leads to more heat exchange surface, reducing the thermal resistance. However, the gain is small, because the additional pins are far away from the heat source and thus play little role in heat transfer.

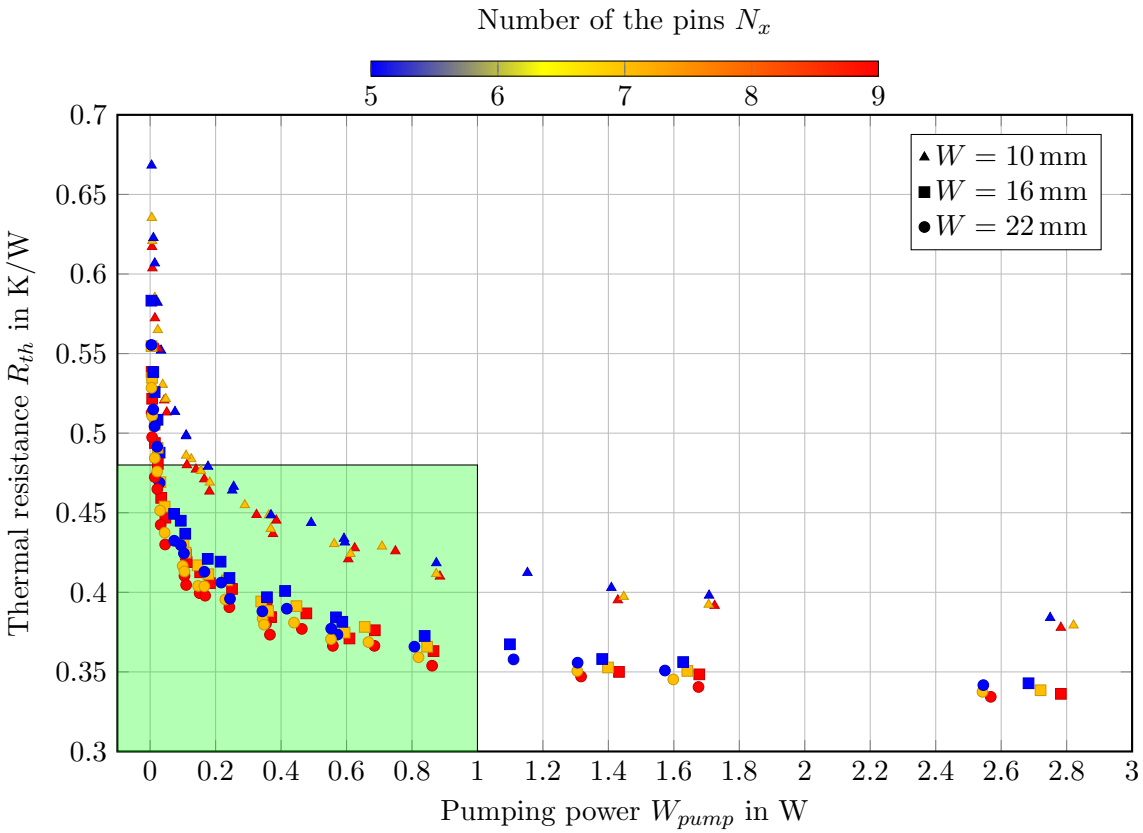


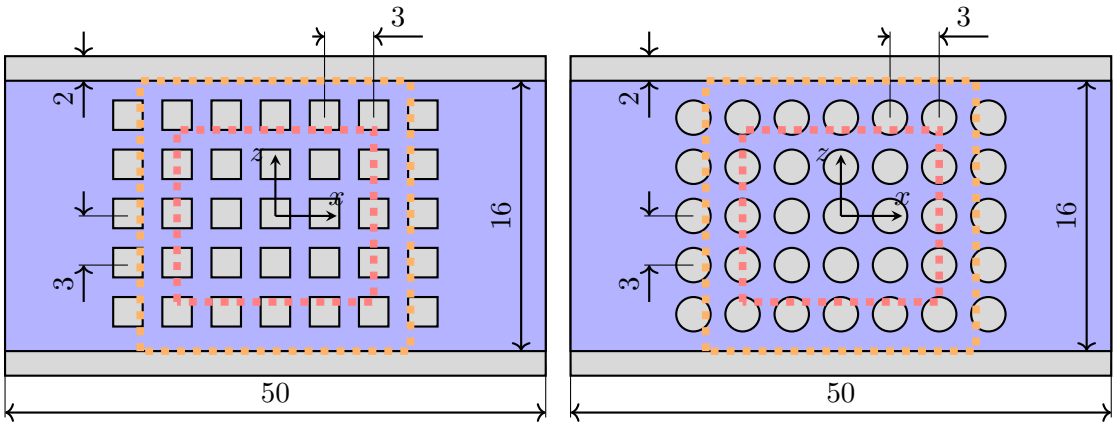
Figure 5.13: Thermal resistance as a function of pumping power, for different channel width W (CFD simulations, for Novec 7500)

5.2.4 Comparison between jet impingement and channel flow with different pin-fin structures

As described in chapter 2, channel flow is another common used cooling concept besides jet impingement. In jet impingement and channel flow coolers, the use of pin structures is a common approach to enhance the heat transfer performance (as it has been demonstrated previously in this chapter). To further analyze the benefits of using pin structures, here we consider different pin shapes (square, circular, conical) as shown in Figure 5.14b.

The geometry considered here is as follows: constant channel height of $H = 6\,\text{mm}$, top AlN thickness of $t = 1.5\,\text{mm}$ and a pin pitch of $s = 3\,\text{mm}$. The channel has a size of $50\,\text{mm} \times 16\,\text{mm}$. The circular pins have a diamter of $d_{pins} = 2\,\text{mm}$ and the square pins have a size of $(2\,\text{mm} \times 2\,\text{mm})$. In case of jet impingement cooler, an inlet jet of $7\,\text{mm}$ diameter is choosen (has better performance as discussed in the previous section).

The thermal resistances of the jet impingement (jet) and channel flow (CF) coolers with square and circular pins are plotted in figure 5.15 as a function of pumping power. The green area in the figure is the target area ($R_{th} \leq 0.48\,\text{K/W}$ & $W_p \leq 1\,\text{W}$). The color



(a) square pins (b) circular pins

Figure 5.14: Square and circular pins with design parameters

bar above the figure shows the magnitude of the flow rate for each point on the graph. The points of each configuration are connected by a smooth line that forms the Pareto front.

The graph shows that circular pins have a better pareto front for both cooling concepts. In particular, the pumping power is much lower for circular pins (this is particularly visible for 5 L/min flow rate). Globally, jet impingement shows better performance than channel flow.

To understand why circular pins and jet impingement perform better, a comparison of fluid velocities in the system is given in Figure 5.16. Velocity distribution in the channel under the die is a decisive factor in the heat transfer. In the case of jet impingement, the coolant hits the surface under the chip normally, causing higher velocity there and more turbulence, which improve the heat transfer coefficient. Furthermore, the jet impingement geometry offer a shorter path from inlet to outlet and the splitting of the flow between both outlets. This causes a dramatic decrease in the pressure drop ($\Delta p \sim \dot{V}^2$) when compared with the channel flow configuration. As a consequence, pumping power is significantly lower for the jet impingement configuration at a given flow-rate.

Figure 5.16 compares the fluid flow distribution with square and circular pins at a distance of 500 µm from the top wall for both cooling concepts, jet and channel flow coolers. Taking advantage of symmetries in the coolers, one quarter of the jet impingement cooler and one half of the channel flow cooler are considered to reduce the computing effort. It can be observed that the square pins result in slightly higher maximum velocities compared to the circular pins for both cooling concepts. This is due to the larger cross-section of the square pins ($2 \times 2 = 4\,\text{mm}^2$ for square pins versus $\pi \times 1^2 = 3.14\,\text{mm}^2$ for the circular pins). It also explains why the pressure drop is higher with square pins than with circular pins.

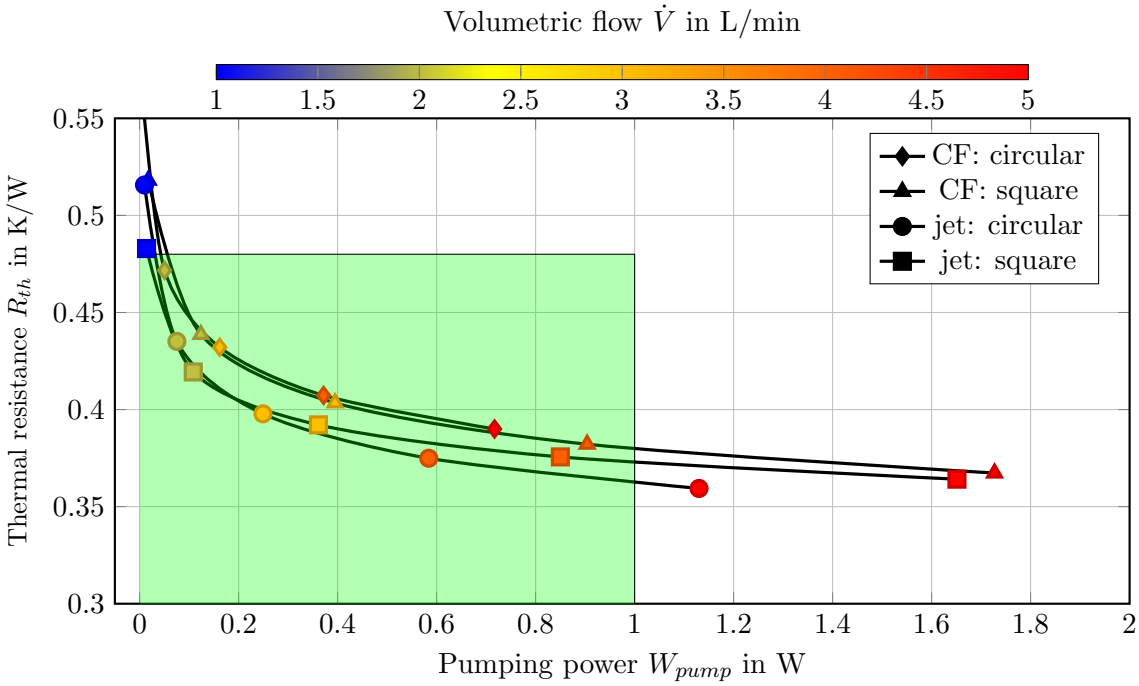
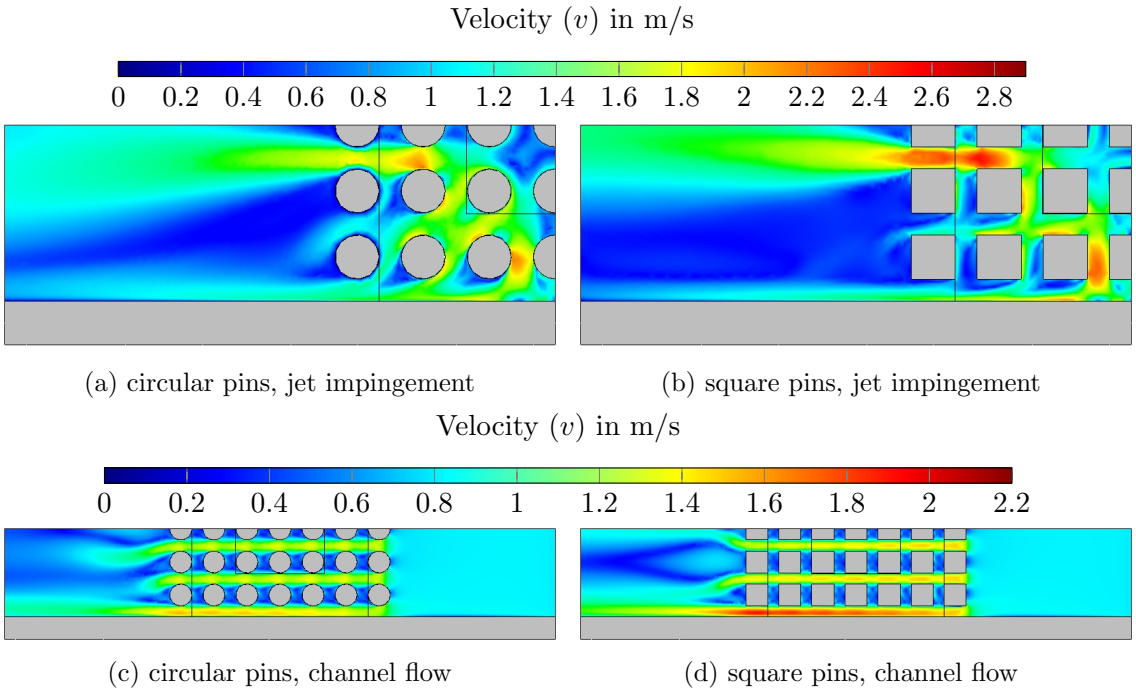


Figure 5.15: Thermal resistance as a function of pumping power for all configurations considered (CFD simulations, for Novec 7500).



(a) circular pins, jet impingement

(b) square pins, jet impingement

(c) circular pins, channel flow

(d) square pins, channel flow

Figure 5.16: Velocity distribution of the jet impingement and channel flow cooler with circular and square pins at 3 L/min at a distance of 500 µm from the top wall (CFD simulations, for Novec 7500)

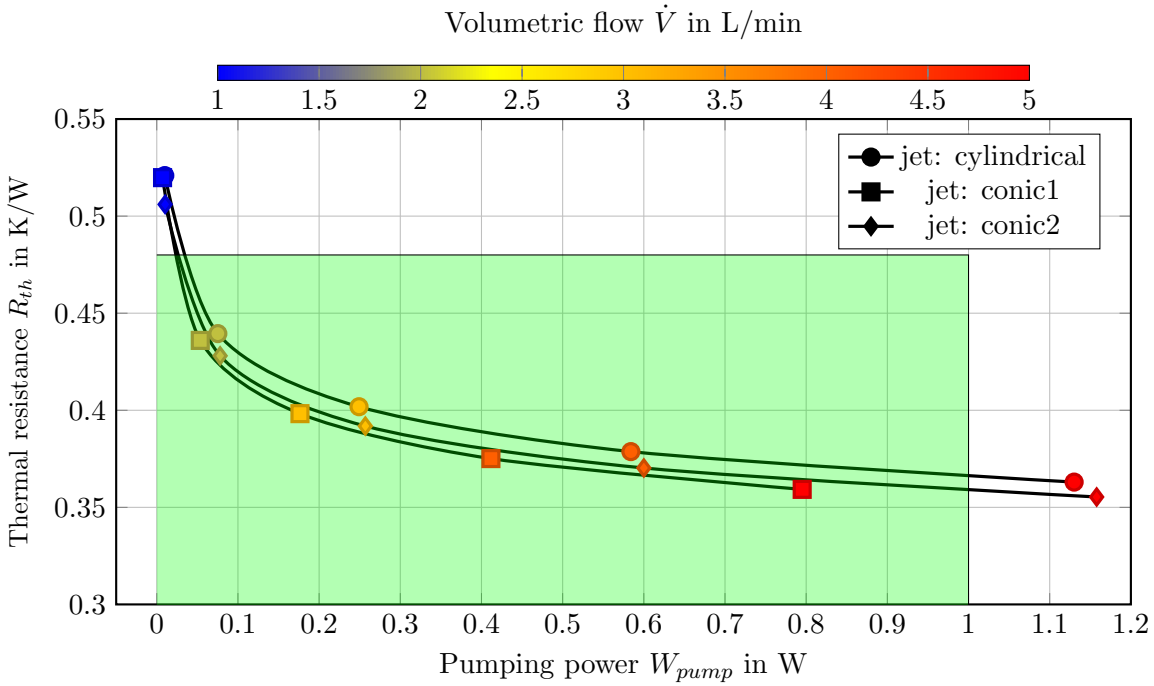


Figure 5.17: Thermal resistance as a function of pumping power for jet cooler with cylindrical and conical pins (CFD simulations, for Novec 7500)

However, the thermal resistance of the cooling system employing square pins exceeds that of the circular pins, primarily because of the superior overall velocity distribution beneath the die. Furthermore, the larger cross-sectional area of the square pins partially obstructs the coolant inlet jet, resulting in increased pumping power requirements and a less favorable velocity distribution.

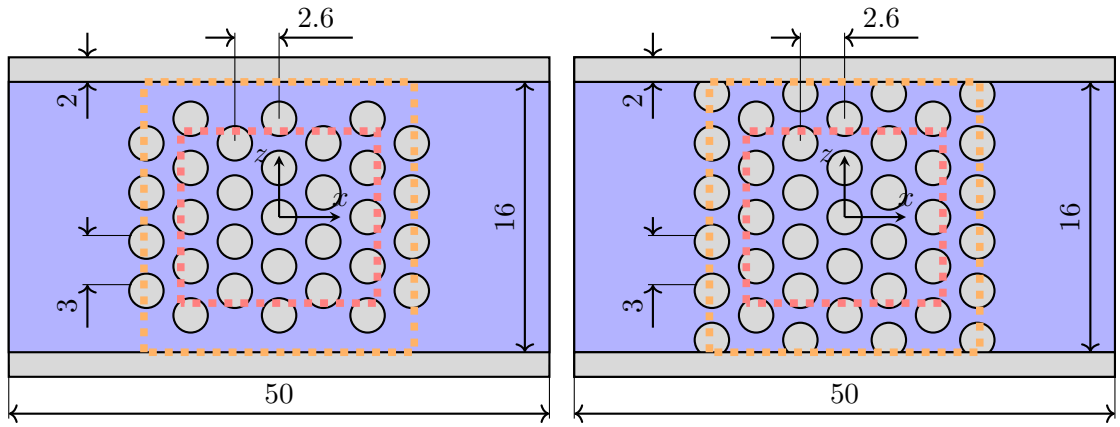
In addition to cylindrical pins with a constant diameter, conical pins are also examined. Two tapered pin configurations are considered. The first (conic1) has an upper diameter of $d_t = 2.5\,\text{mm}$ and a lower diameter of $d_b = 1.5\,\text{mm}$. This configuration is chosen to keep the mean diameter of the pins 2 mm, which was the best diameter previously envisaged. However, these specific pin configurations cannot be manufactured due to limitations associated with production costs in the manufacturing process. The manufacturer (CeramTec) can supply 6 mm-long pins with an upper diameter of $d_t = 2.7\,\text{mm}$ and a lower diameter of $d_b = 1.8\,\text{mm}$ (conic2). A comparison of the cooling performance of cylindrical and conical pins is shown in figure 5.17.

Conical pins show a better Pareto front due to larger diameter under the die, which improves the heat transfer. Due to the smaller bottom diameter of the pins, conic1 has a decreased blockage at the nozzle inlet, leading to a reduced pressure drop. This design results in a notably lower pumping power. On the other hand, conic2 exhibits the highest pressure drop, primarily due to its larger blockage area. Consequently, Conic1 outperforms

the other two configurations in terms of cooling efficiency, primarily attributed to its lower pumping power requirements.

5.2.5 Comparison between different pin arrangements

In channel flow and jet impingement cooling, pin arrangements play a crucial role in determining the cooling performance. This subsection focuses on the comparison of two different pin layouts, namely inline (pins arranged along a grid, as considered so far) and staggered pins (see Figure 5.18). The performance of inline and staggered pin arrangements is evaluated for channel flow and jet impingement cooling. All used pins in this comparison are cylindrical with a diameter of 2 mm and a height of 6 mm. The spacing between the pins is 1 mm. This corresponds to different pin densities for inline (3 mm distance axis-to-axis along the x-axis) and staggered (2.6 mm distance axis-to-axis along the x-axis) layouts. Staggered pins are therefore denser than inline pins.



(a) staggered pins (staggered1) (b) staggered pins with wall pins (staggered2)

Figure 5.18: The two variants of staggered pins arrangement with the design parameters

The Pareto front curves of thermal resistance over pumping capacity are plotted in figure 5.19 In channel flow cooling, staggered pin arrangements show better cooling performance than inline pin arrangements. On the other hand, inline pin arrangements perform better in jet impingement cooling.

The comparison of the velocity distribution for inline and staggered pin arrangements helps in understanding the cooling performance of these two pin arrangements. Figure 5.20 shows a comparison of the velocity distribution in two different types of pin arrangements, staggered and inline, in two cooling configurations, channel flow and jet impingement.

In the channel flow cooler, the staggered pin arrangement shows a higher and more uniform velocity distribution compared to the inline pin arrangement. This is because the staggered pins provide a longer flow path for the fluid, resulting in higher velocity

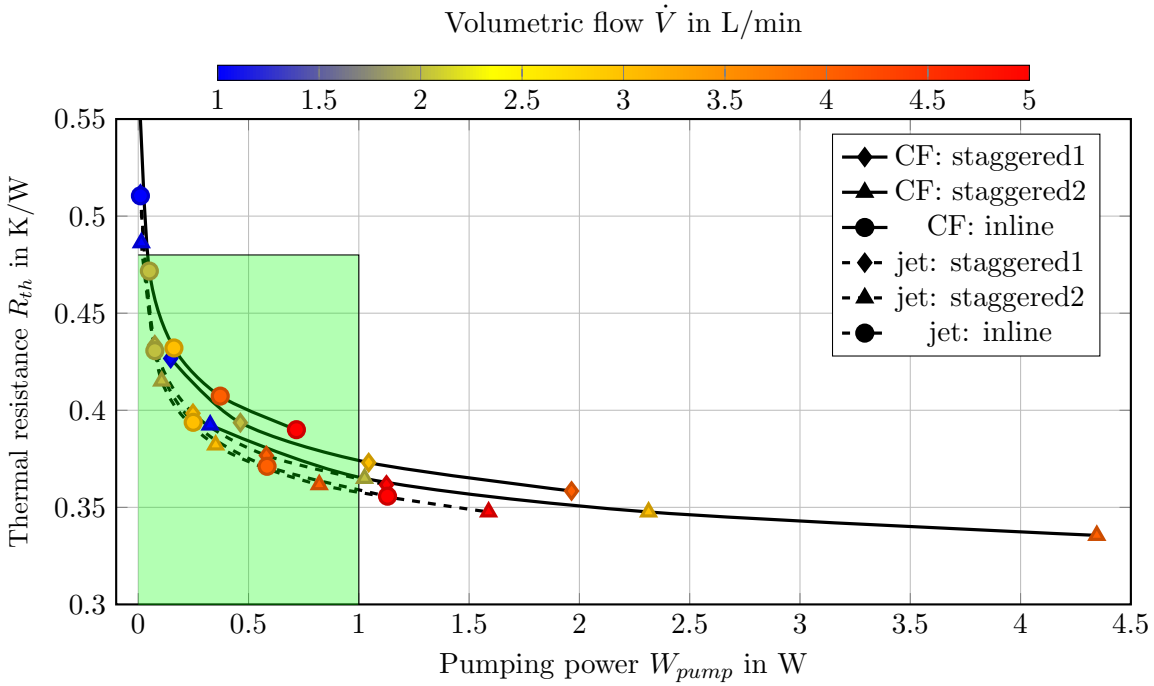
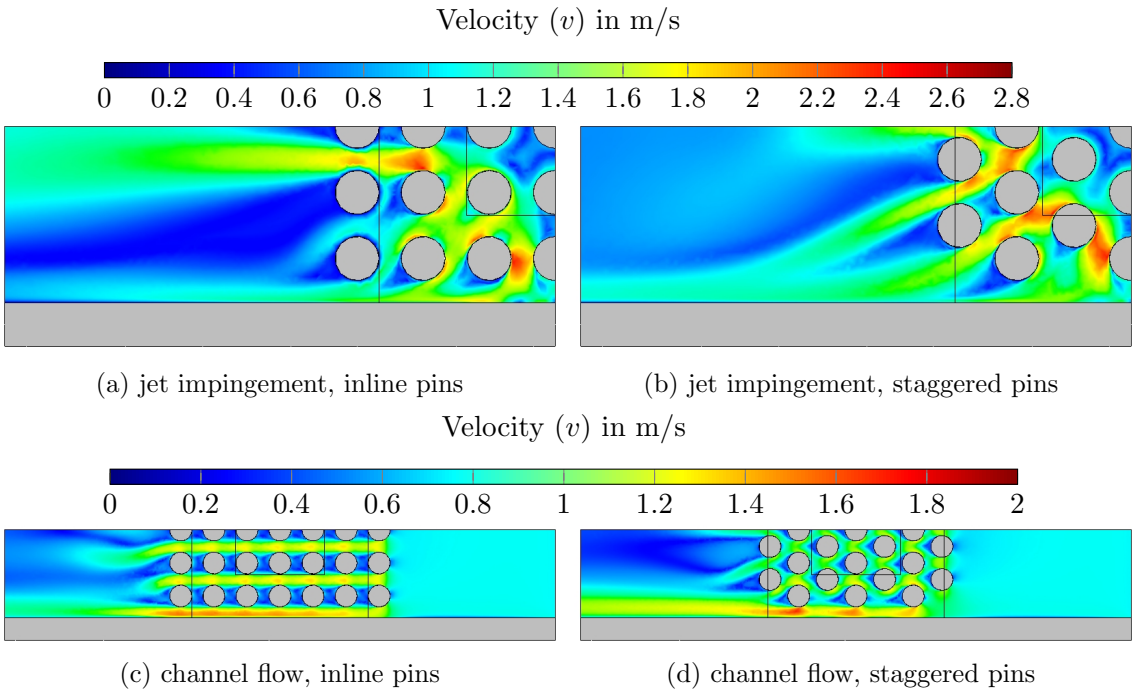


Figure 5.19: Thermal resistance as a function of pumping power for staggered and inline pin layouts, for jet impingement and channel flow coolers (CFD simulations, for Novec 7500).

and better mixing. However, in the jet impingement cooler, the inline pin arrangement is more efficient compared to the staggered pin arrangement. This is because the inline pins provide a longer path for the fluid to flow through, resulting in better contact between the fluid and the pins. In contrast, the staggered pins provide a linear (radiating from the inlet) path for the fluid, reducing turbulence and contacts between the fluid and the pins. Overall, a staggered pin arrangement is more efficient for a channel flow cooler, and an inline arrangement for a jet impingement cooler.

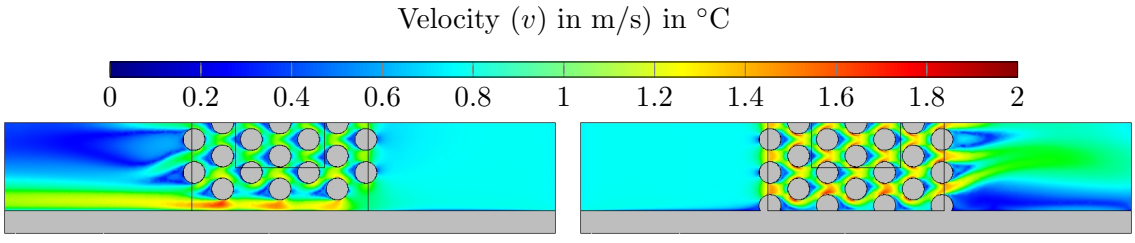
Figure 5.21 compares the velocity distribution in a channel with staggered pins arranged according to the two variants described in Figure 5.18: with or without rows of pins attached to the cooler walls. In the first case (figure 5.21a), higher fluid velocity is observed between the walls and pins due to lower fluidic resistance in this region. However, this results in a degradation of the cooling performance, as can be seen in Figure 5.19. In the second case (figure 5.21b), where wall pins are present, higher velocities are observed between the pins under the die. This is because the wall pins block the fluid from flowing along the walls, where little heat is dissipated, and redirect the flow toward the die, resulting in more efficient cooling. Nevertheless, the pressure drop resulting from the staggered2 of pins is significantly greater, primarily attributed to the increased fluidic resistance within the channel.



(a) jet impingement, inline pins (b) jet impingement, staggered pins

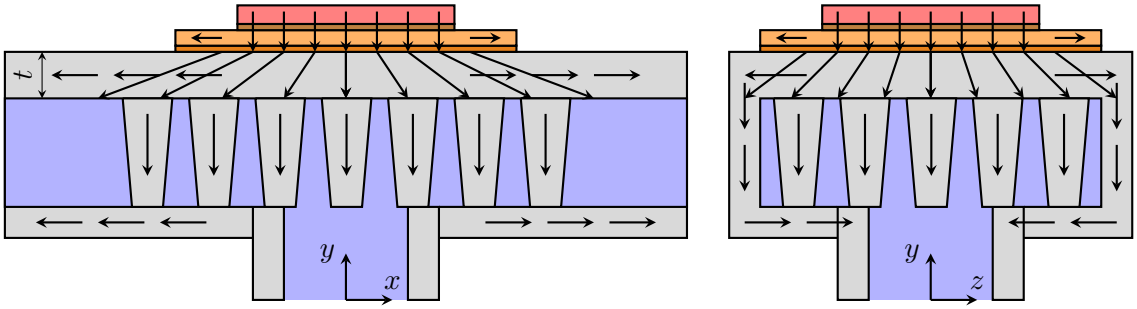
(c) channel flow, inline pins (d) channel flow, staggered pins

Figure 5.20: Velocity distribution of the jet impingement and channel flow cooler with inline and staggered ("staggered1" layout) pins at 3 L/min at a distance of 500 µm from the top wall



(a) "staggered1" layout (b) "staggered2" layout

Figure 5.21: Velocity distribution in the channel flow cooler for staggered layouts without and with wall pins ("staggered" and "staggered2", see Fig. 5.18) at 3 L/min at a distance of 500 µm from the top wall



(a) Cross section along the channel (b) Cross section across the channel

Figure 5.22: Schematic representation of the direction of heat flow in the AlN for a jet cooler

5.2.6 AlN thickness effect

An other parameter of influence is the thickness of the AlN ceramic on top of the pins (parameter t in Fig. 5.9). Prior to delving into the CFD results, it is crucial to understand the fundamental principles of heat dissipation from the chip to the coolant. This will facilitate the analysis of the CFD results.

Heat flows through solid materials by a thermal conduction process governed by Fourier's law, which states that the rate of heat transfer through a material is proportional to the temperature gradient. Furthermore, the heat transfer rate is also influenced by the size of the material, as larger surfaces offer more area for heat to flow. The steady state heat flow from the die to the coolant can be described using the following equations:

$$P_{loss} = \dot{Q} = \lambda \, \mathbf{A} \cdot grad\, T = \lambda \begin{bmatrix} A_{yz} \\ A_{xz} \\ A_{xy} \end{bmatrix} \cdot \begin{bmatrix} \partial T/\partial x \\ \partial T/\partial y \\ \partial T/\partial z \end{bmatrix}; \qquad \mathbf{A} \propto \frac{1}{grad\, T} \propto t \tag{5.3}$$

where $\dot{Q}$ is the heat transfer rate, in our case the power losses P_{loss} generated in the semiconductor device. The heat transfers through the surface areas A_{yz}, A_{xz}, and A_{xy}. This equation demonstrates that the temperature gradient is inversely proportional to the surface area when considering constant power losses. The distribution of heat flow within the AlN material hinges on the dissipation surface of the AlN (thickness t). A larger dissipation surface leads to an overall reduced temperature gradient, signifying a more uniform dispersion of heat throughout the heat sink, thereby resulting in a lower junction temperature for the semiconductor device.

Figure 5.22 depicts the movement of thermal energy $\dot{Q}$ from the semiconductor device to the coolant through the AlN heat sink. A thicker base plate t allows for greater heat flow along the x and z axes ("heat spreading"), while the temperature gradient decreases in the y axis.

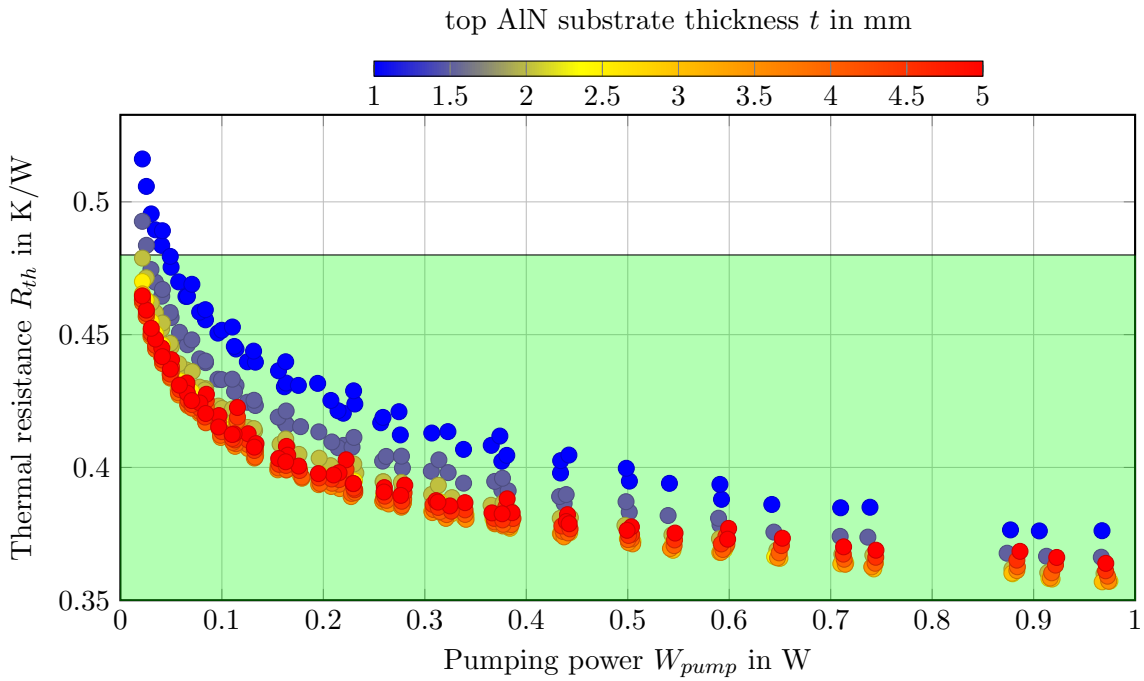
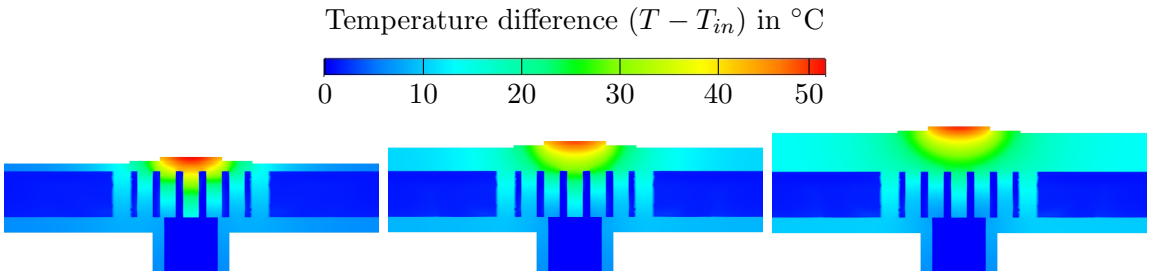


Figure 5.23: Thermal resistance as a function of pumping power, for different values of AlN thickness t (CFD simulations, for Novec 7500 an $d_{pins} = 2\,\text{mm}$).

The use of thicker AlN baseplate in the heat sink leads to better heat dissipation, as it allows for more efficient transfer of thermal energy from the semiconductor device to the coolant through the baseplate in the x and z directions, where the liquid has a lower temperature. This relieves some of the constraints of heat dissipation in the y direction, allowing for a more uniform temperature distribution in the chip. This is because heat spreading along the x and z directions reduces the heat density in the y direction. However, excessively thick AlN can result in a longer path from the chip to the coolant in the three directions. This means a lower temperature gradient, which is the ratio of the temperature difference ($\partial T \approx \Delta T$) and the path ($\partial \mathbf{x} \approx \mathbf{\Delta x} \propto \mathbf{t}$). The thickness t must therefore be optimized to ensure maximum heat dissipation in the x and z directions while maintaining a suitable temperature gradient in all directions.

CFD simulations are performed for different t values (ranging from 1 to 5 mm), while the other parameters are kept constant except for the jet diameter, which varies within the range of $5\,\text{mm} < d_{jet} < 9\,\text{mm}$ and the flow rates within the range of $1\,\text{L/min} < d_{jet} < 5\,\text{L/min}$. Cylindrical pins with $h = 6\,\text{mm}$ length and diameter of $d_{pins} = 2\,\text{mm}$ are used for the numerical calculations. Fig. 5.23 shows the thermal resistance dependencies on the ceramic thickness. The optimum t value is found to be 3 mm, as it forms the Pareto front (thinner or thicker AlN layers result in a thermal resistance values).

Figure 5.24 shows the temperature distribution in the middle of the cooler with different



(a) $t = 1\,\text{mm}$ (b) $t = 3\,\text{mm}$ (c) $t = 5\,\text{mm}$

Figure 5.24: Temperature distribution at the symmetry plane in the middle of the channel at 2 L/min

AlN thicknesses ($t = 1\,\text{mm}$, $3\,\text{mm}$, and $5\,\text{mm}$). The extremities of the geometries are colder for $t = 1\,\text{mm}$ than for $t = 3$ or $5\,\text{mm}$, while the AlN directly under the die is hotter, indicating that the heat dissipation is less efficient in this configuration. The extremities of the $t = 5\,\text{mm}$ geometry are the warmest of all 3 configurations, demonstrating the good heat spreading enabled by the thick AlN layer. The temperature gradient across $t = 5\,\text{mm}$ geometry is smaller than in the other coolers, indicating that the thicker AlN provides a more uniform temperature distribution. However, the maximum die temperature is higher for the $t = 5\,\text{mm}$ geometry than for $t = 3\,\text{mm}$. This indicates that the thicker AlN layer causes a longer path from die to coolant, overcoming the beneficial effect of improved heat spreading. Overall, $t = 3\,\text{mm}$ offers a lower thermal resistance. Two t values are selected for the experimental investigations at the end of the chapter: $1.5\,\text{mm}$ (to explore thin designs) and $3\,\text{mm}$ (thermal optimal).

5.2.7 Comparison between different coolants

This section analyzes the effect using cooling fluids with different properties. According to chapter 3, the used coolants are Novec 7500, Novec7300, Trafosynth2, ethylene glycol (glycol/water mixture), and water.

The simulations are done using geometry similar to that presented in figure 5.9. The pins are cylindrical with $2\,\text{mm}$ diameter and $6\,\text{mm}$ length. The results are presented in figure 5.25. From the graph, it can be observed that water has the lowest thermal resistance and pumping power, making it the most efficient coolant. Glycol/water micture (50:50) has slightly higher thermal resistance and pumping power compared to water. Due to their higher viscosity, which leads to different velocity distribution and low velocity at walls, Trafosynth2 have the highest thermal resistance and pumping power among the five coolants, making them the least attractive. Novec 7500 and Novec 7300 both have a very similar performances, and offer lower thermal resistance at a given pumping power than the Trafosynth2, without reaching the performance of water.

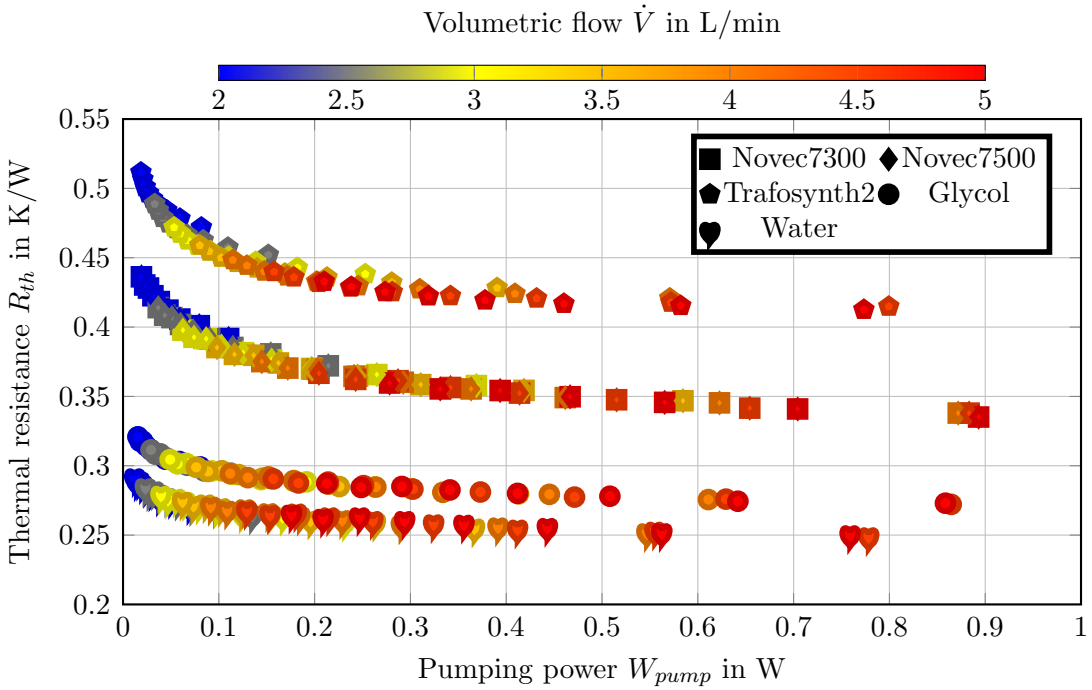


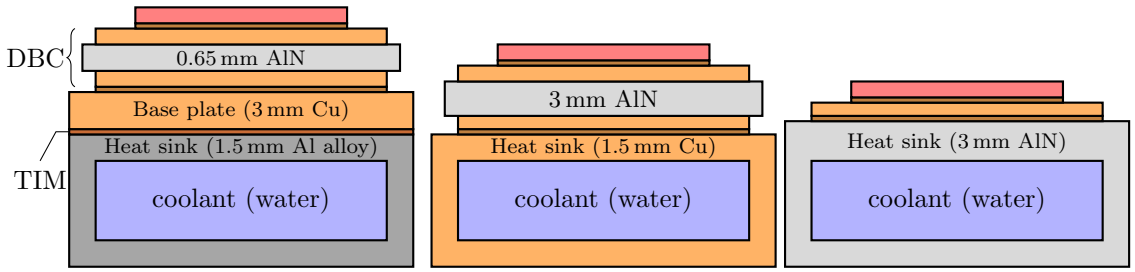
Figure 5.25: The cooling performance of the six chosen coolants

5.2.8 Comparison between different packaging structures

The aim of this section is to show the advantage of the proposed packaging solution, based on an AlN heatsink, compared to more established packaging solutions, as depicted in figure 5.26. The "traditional" packaging solution corresponds to a power module attached to a separate cold plate. The "state-of-the-art" structure is a more integrated solution, in which a DBC substrate is directly attached to a high performance cooler.

CFD simulations are carried out, considering that all three coolers use jet impingement of water. The material properties from table 3.2. The copper layers of the DBC substrates have a thickness of 0.3 mm in both structures, figure 5.26a and 5.26b. The AlN insulator of the traditional packaging is 0.65 mm thick while in the integrated structure is 3 mm thick, the same as in the novel package, to compare the thermal performance of both structures with the same insulation capability (providing all the insulation by ceramic). The heat sink of the traditional packaging is made out of aluminium alloy ($\lambda = 170\,\mathrm{W/mK}$) and that of the state-of-the art of copper. The base plate of the traditional package is mounted on the heatsink using a layer of Thermal Interface Material (TIM), with very optimistic properties (thickness 50 µm, thermal conductivity 5 W/mK). All three structures have the same internal pin-fin design with channel height of 6 mm, conical pins with top and bottom diameters of 2.8 and 1.8 mm respectively.

Figure 5.27 shows the temperature distribution in the three packaging structures at

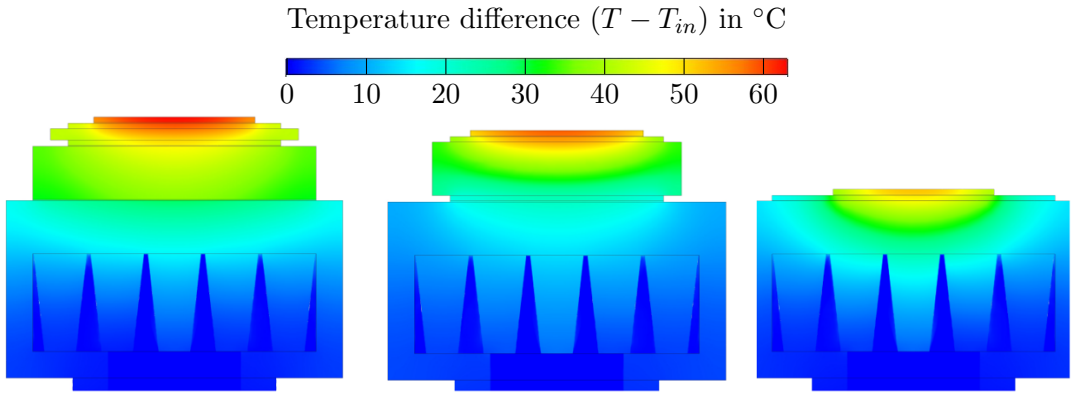


(a) Traditional package structure with TIM between base plate and external cooler

(b) State-of-the-art power module with integrated heat sink into the baseplate

(c) Novel packaging structure with pin-fin cooler integrated into ceramic substrate

Figure 5.26: The three different packaging configuration used for the CFD simulations



(a) Traditional packaging $R_{th} = 0.32\,\mathrm{K/W}$

(b) DBC on copper heatsinks $R_{th} = 0.3\,\mathrm{K/W}$

(c) Novel packaging $R_{th} = 0.26\,\mathrm{K/W}$

Figure 5.27: Temperature distribution in the three different packaging structures at 3 L/min

3 L/min. In this case, the thermal resistance is reduced from 0.32 K/W (traditional package) to 0.26 K/W (novel package). Furthermore, the AlN heatsink offers additional advantages in terms of voltage isolation: in the traditional package, electrical insulation is provided at the substrate level, where the ceramic is thin (typically 0.65 mm), while the ceramic heatsink uses a much thicker layer (here 3 mm). Furthermore, lower thermo-mechanical stress can be expected for the novel package, as the coefficient of thermal expansion of AlN (4-5 ppm/K) is much closer to that of the chips (in the order of 3 ppm/K) than Aluminium alloy (19-25 ppm/K)and copper (17.8 ppm/K).

The thermal resistance over flow rate is summarised in figure 5.27. It shows the expected thermal resistance of the three investigated packaging variants over the flow rate.

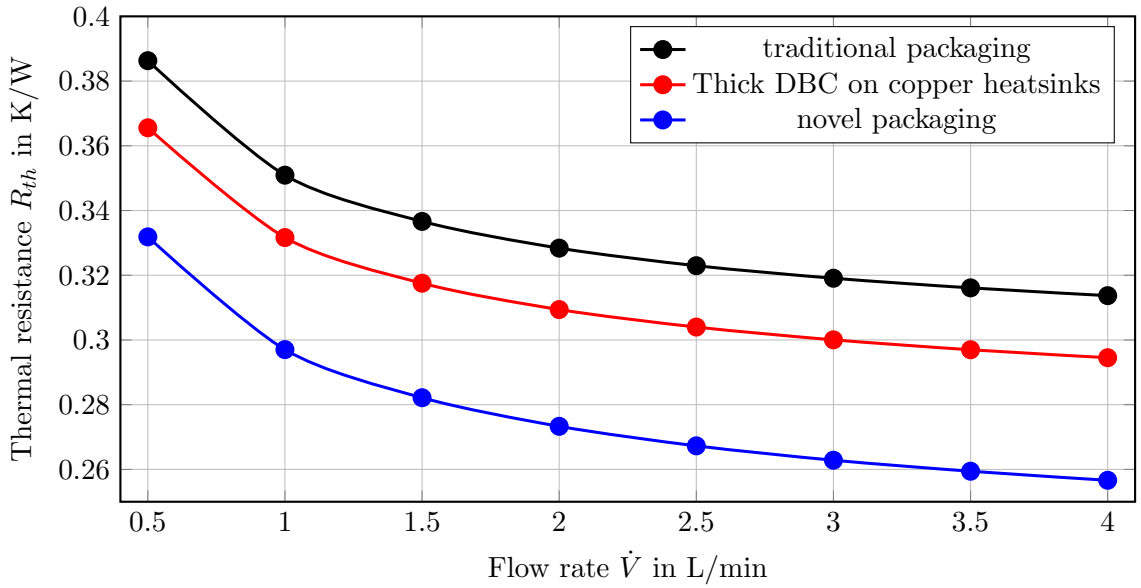


Figure 5.28: Thermal resistance comparison between three packaging configurations (CFD, jet impingement coolers with the same pin fin layout).

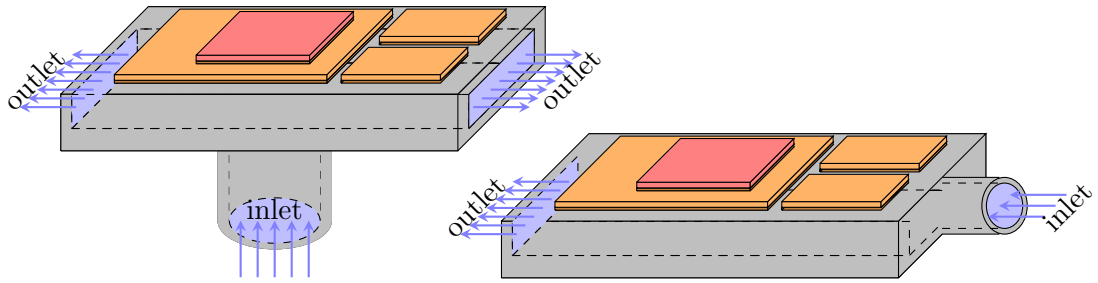
5.2.9 Conclusions on the CFD investigations

The preliminary investigations show that a cooler with smooth walls (no internal pins) fails to achieve the target thermal resistance of 0.48 K/W with a pumping power lower than 1 W. Therefore, pins are added to the structure and further CFD investigations are conducted to optimize their geometry. The optimization process involves testing different design parameters, including cooling concept (jet-impingement and channel-flow), pins shape (circular, conical, and square), pins arrangement (in-line and staggered) and the thickness of the AlN substrate. The study reveals that conical pins perform the best, whereas square pins perform the worst. Additionally, the investigation indicates that in-line pin arrangement is better suited for jet impingement cooler, while staggered pin arrangement is more effective for channel-flow cooler. Furthermore, the study shows that relatively thick AlN (3–3.5 mm) improves cooling performance due to its superior spreading effect. The target thermal resistance is easily achieved with a pumping power lower than 1 W. Finally, the novel package structure proposed in this work is compared with traditional and state-of-the-art packages, demonstrating that it outperforms the other packaging structures significantly.

Because of manufacturing constraints, the chosen pin size differs from the optimal design (top and bottom diameters of 2.8 mm and 1.8 mm respectively, versus $d_t = 2.5$ mm and $d_b = 1.5$ mm for the optimized design). The ideal inlet jet diameter (d_{jet}) falls within the range of 6 mm to 8 mm, so a diameter of 7.5 mm is chosen due to the availability of the corresponding inlet fitting for the prototype's production. An AlN thickness of 3.3 mm is

Table 5.5: Final geometry parameters of jet cooler design of one-die module

design	pin shape	d_t	d_b	d_{jet}	H	t_{AlN}
Optimal design	conical	1.5 mm	2.5 mm	6 to 8 mm	6 mm	3 to 3.5 mm
Practical design	conical	1.8 mm	2.8 mm	7.5 mm	6 mm	3.3 mm



(a) jet impingement (b) channel flow

Figure 5.29: Schematic design of the module for the thermal test: jet impingement and channel flow coolers

determined to be the optimal choice.

Table 5.5 presents the parameters considered for the optimal configuration, and those used practically.

5.3 Single die module – experimental validation

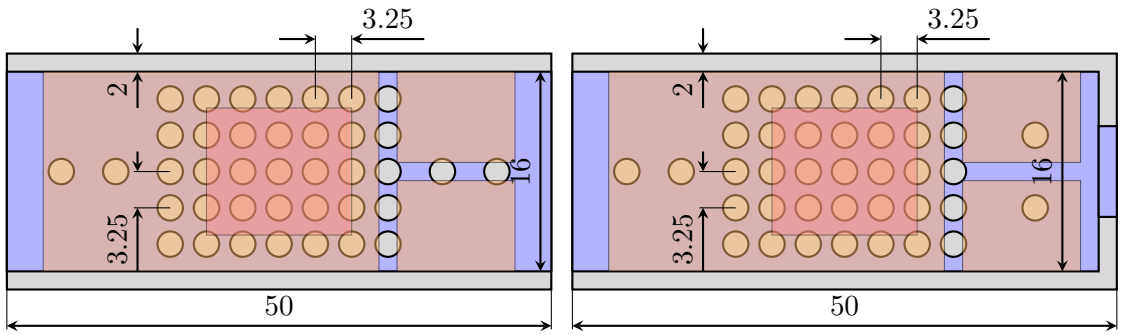
In the previous section, CFD simulations are used to optimize a one-die cooler. This section aims at validating the simulation results through experiments. First, the production of the test vehicles is detailed. Then, the test setup presented. At the end, the experimental results are discussed and compared to the CFD results.

Figure 5.29 shows a schematic view of the coolers. The jet cooler has one inlet (jet) and two outlets, while the channel flow cooler has one inlet and one outlet. Three different prototype configurations are built for the thermal tests: a channel flow cooler with 3 mm top AlN thickness, and two jet impingement coolers with 1.5 mm and 3 mm AlN thickness. More design details are given in the next section.

5.3.1 Design of the AlN coolers

The electrical connections of the device require more complex design of the metal pattern on the ceramic cooler than the one considered in section 5.2. The main difference is that the CFD model contains only one rectangular copper pad, whereas the test vehicle has two additional small copper pads to provide connections to the semiconductor chip (see Figure 5.29). Furthermore, the chip cannot be sintered in the center of the large copper

pad, as the connections between the top of the chip and the two small copper pads (wire bonding) have a limited length. The chip is sintered 2 mm from the right edge of the main copper sheet (16 mm × 26 mm) in the center of the channel. The other two copper sheets have a size of 7 mm × 12 mm and receive the emitter and gate connections.



(a) jet cooler (b) channel flow cooler

Figure 5.30: Schematic cross section in the center of the channel under the chip showing the design parameters

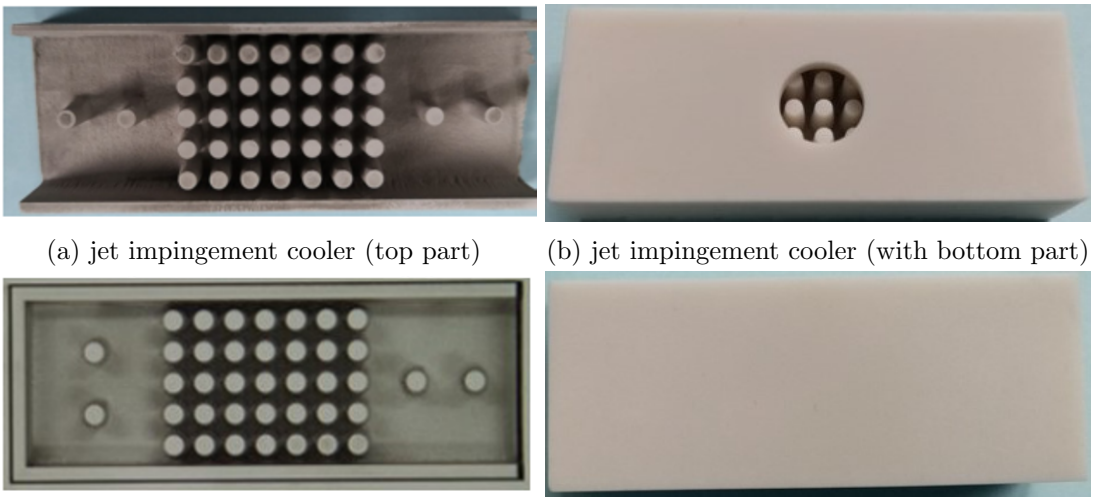
The coolers have a length of 50 mm and a channel width of 16 mm. Both coolers have identical built-in pins under the die (same layout and pin size). Figure 5.30 shows the pin-fin structures for both coolers (jet and channel flow). The pins are spaced 3.25 mm apart. They are conical with a diameter of 2.8 mm at the top and 1.8 mm at the bottom. Four additional pins (two on each side) are placed in the channel sides for mechanical strength (at the inlet side of the channel flow cooler, these support pins are placed on the side, so as to interfere as little as possible with the incoming flow). This design of the pins is the result of iterations with the manufacturer CeramTec GmBH, considering manufacturability. The pins design is chosen according to the optimized design for jet impingement. The channel flow cooler employs an identical pin fin design as the jet impingement cooler, enabling a direct performance comparison between the two cooling concepts with uniform pin configurations.

5.3.2 Preparation of the test vehicles and test setup

As already mentioned, three different prototypes (one channel flow cooler and two jet impingement coolers with different ceramic thicknesses) are designed for thermal testing. The metallized AlN coolers are manufactured by CeramTec. They are processed further (mounting of the semiconductor die and of the connectors, wirebonding) in the electronics integration lab (EI-Lab, Kempten University). This section describes this manufacturing process:

Manufacturing of the AlN cooler

Two ceramic parts are made, a flat bottom and a top with pin fin structures. Both parts are joined together to form one cooling unit. Figure 5.31 shows the upper and lower part of the cooler. The upper part of the jet cooler has no walls on the sides (left and right). These will later form the outlets to the ambient. The upper part of the channel flow cooler has no wall on one side for the outlet and on the other side another wall with an opening in it to form the inlet. The lower part of the jet cooler has an opening that forms the inlet.



(a) jet impingement cooler (top part) (b) jet impingement cooler (with bottom part)

(c) channel flow cooler (top part) (d) channel flow cooler (with bottom part)

Figure 5.31: Manufacturing of the prototypes: channel flow and jet impingement

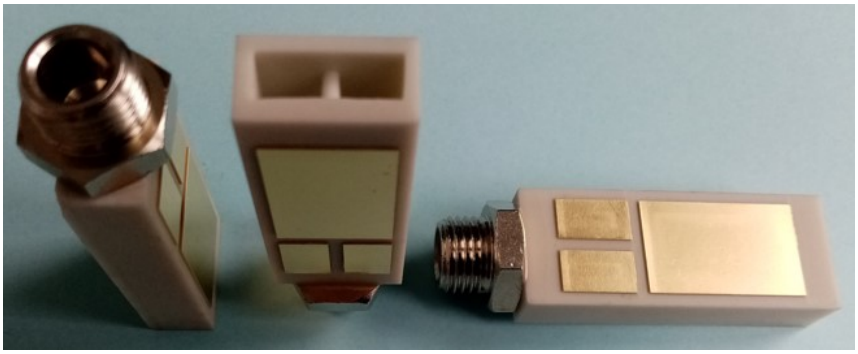
Copper metallizations and brass fitting

The copper plates are brazed to the AlN coolers. Brazing uses a thin layer (10 µm-thick) of a high thermal conductivity ($\sim 360\,\mathrm{W/mK}$) active metal braze alloy (active solder). A nickel-gold finish is the plated onto the copper pads to protect them from oxidation and facilitate die attach and wirebonding.

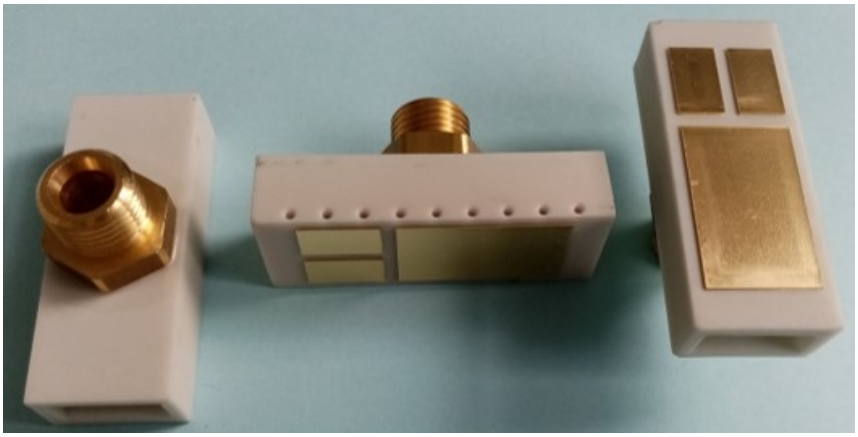
Brass fittings are then glued (Delo AD295) to the ceramic coolers to form the inlets. The inner diameter of the fittings is 7.5 mm for the jet impingement coolers and 6 mm for the channel flow coolers. Figure 5.32 shows the metallized coolers with the attached brass fitting.

Attaching the Si IGBT die onto the cooler and thick Al wire-bonding

As described in section 3.1, 10 kV SiC MOSFETs with a $8.1 \times 8.1\,\mathrm{mm}^2$ chip size are considered for the CFD optimization. However, these are found not be available any



(a) metallized channel flow coolers



(b) metallized jet impingement coolers

Figure 5.32: The metallized AlN coolers: channel flow and jet impingement

longer at the time of the experiments. Here, 9.1 mm × 9.1 mm IGBT (5SMY 12H1280, ABB Switzerland Ltd) are used instead.

The IGBT chips are sintered on the largest metal pad, using a pressure-assisted process. The die to be used is picked up from the wafer using a Finetech Fineplacer Pico chip bonder. The die is pressed onto a silver film (Alpha Argomax 8050, 50 µm-thick) with a force of 250 N (3 MPa). This causes the silver film to be transferred to the underside of the chip. The cooler is placed on a hot plate (150 °C). The semiconductor device is placed at the desired position on the copper pad (still using the die bonder). The placement tool is heated to 280 °C, and force of 450 N (5.5 MPa) is applied on top of the chip for 2 minutes, after which the process is complete.

After sintering, the pads of the IGBTs are wire-bonded with thick (300 µm-thick) Al wedge bonds. Five wire bonds are connected to the source surface to carry about 50 A, which is needed to heat the chip to 125 W. A single wire bond is used to connect the gate. Figure 5.33 shows the sintered dies on the metallized cooler and the wire bonds.

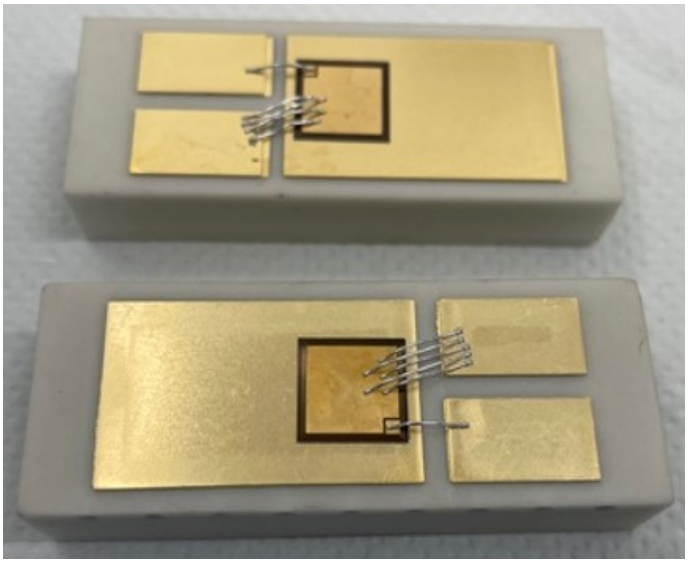


Figure 5.33: The sintered IGBTs on AlN coolers and wirebonding

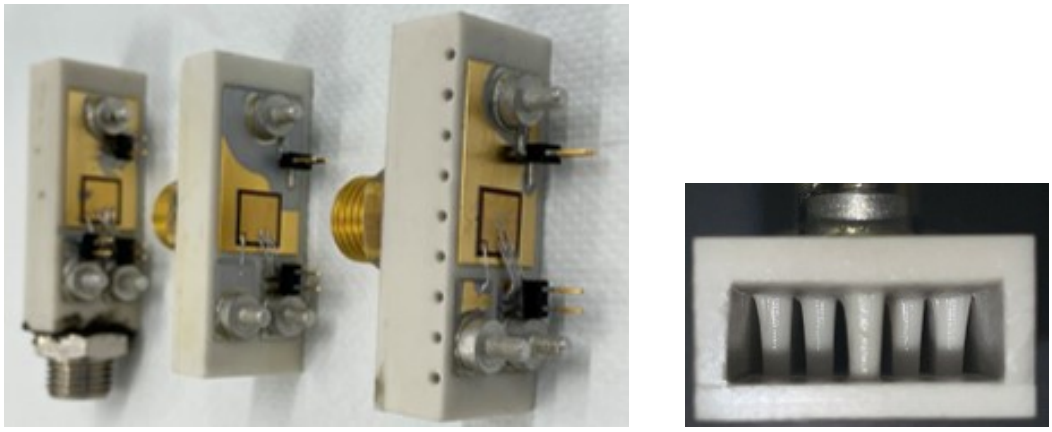
Soldering the connectors

Figure 5.34: Soldered power connectors and auxiliary pins for the connection to the outside world.

The final step is to attach the connectors on the metal pads for the electrical connection to the outside world. A SMD power element (7466213, Würth Elektronik), which is capable to carry 50 A is soldered on each metal pad using SAC solder paste (SMD291SNL50T3). Additionally, pins connectors (M50-3630242, Harwin Inc.) are soldered on the collector and source pad for voltage measurement during the thermal test. Soldering is performed by placing the assemblies into an oven at 250 °C for 5 minutes. The coolers with the

soldered components are shown in figure 5.34.

The one-die test vehicles are now ready for the thermal test. The three different coolers are shown in figure 5.35. One module with channel flow concept and 1.5 mm thick AlN, two modules with jet impingement cooling concept with two different top AlN thicknesses (1.5 mm and 3 mm). The 3 mm jet cooler has nine holes in the top AlN which run down to the middle of the layer. These holes are designed to host thermocouples to measure the temperature of the AlN. Figure 5.35b shows a view look at the conical pins in the channel from the side.



(a) The three prototypes (b) Side view showing the pins

Figure 5.35: The three prototypes: channel flow, jet impingement with two AlN thicknesses (1.5 mm and 3 mm) and a view of the pins

5.3.3 Overview of the experiment

Once they are assembled, the test vehicles are integrated into a test setup that includes a fluid cooling loop and electrical circuits. This section presents the experimental setup in detail. The construction is separated into two parts: the fluid loop and the electrical connections to operate the semiconductor.

Cooling circuit

A cooling circuit is needed to manage the liquid (Figure 5.36). Because dielectric fluids are aggressive to some plastics, a chemical-resistant magnetic coupled pump is used to avoid chemical reactions. The liquid is pumped into a heat exchanger to control the inlet temperature (a separate chiller controls the heat exchanger temperature). The liquid is then directed into the DUT to cool the module. Then the liquid flows through the outlet into an open tank (ambient pressure) and then into the pump to keep it circulating. A flow meter is installed before the cooler. Two valves are installed after the pump to control

the flow rate: one is in series with the cooler, while the other is a bypass in case a very low flow rate is desired for the module. A special care is given to the design of the cooling loop to avoid elastomeric materials which may react with Novec 7500. All the tubes are made from copper and brass and steel compression fittings are used to connect the pipes.

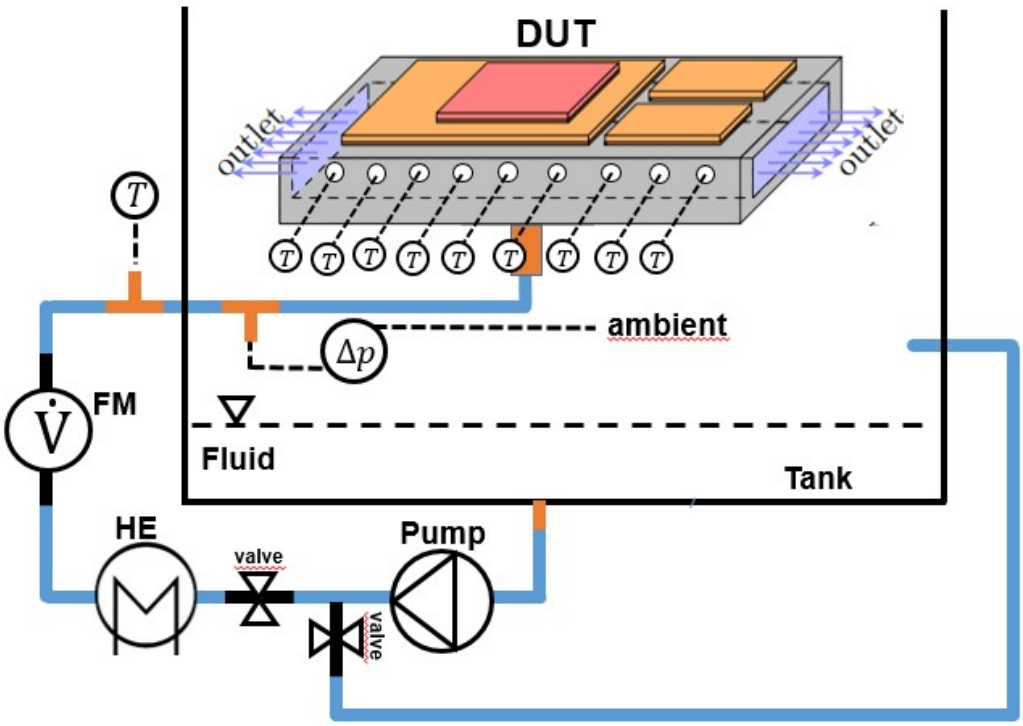


Figure 5.36: schematic overview of the fluidic loop setup for the one-die cooler

The pumping power is calculated for the pressure drop between inlet and outlet (ambient pressure in this case) and the flow rate:

$$W_{pump} = \dot{V} \times \Delta p \tag{5.4}$$

In addition, the temperature at the inlet is measured, which is later used to calculate the thermal resistance. In the case of the 3 mm jet impingement cooler, nine thermocouples (1 mm sheath, K-type) are inserted in the top AlN holes.

Electrical connections

In order to operate the chip on the cooler, it should be electrically connected. A load current is applied to the drain-source using a thermal analyzer (Phase 12B, Analysis Tech). A constant 9 V voltage is applied between gate and emitter to turn the transistor on. The thermal analyzer applies a large (up to 100 A current between collector and

emitter to force the DUT to heat-up; periodically, it briefly interrupts the heating current and applies an small (5 mA) reading current to estimate the chip junction temperature (see section 4.3.1). The thermal analyzer performs the measurements automatically. A schematic overview of the electrical test setup is shown in 5.37.

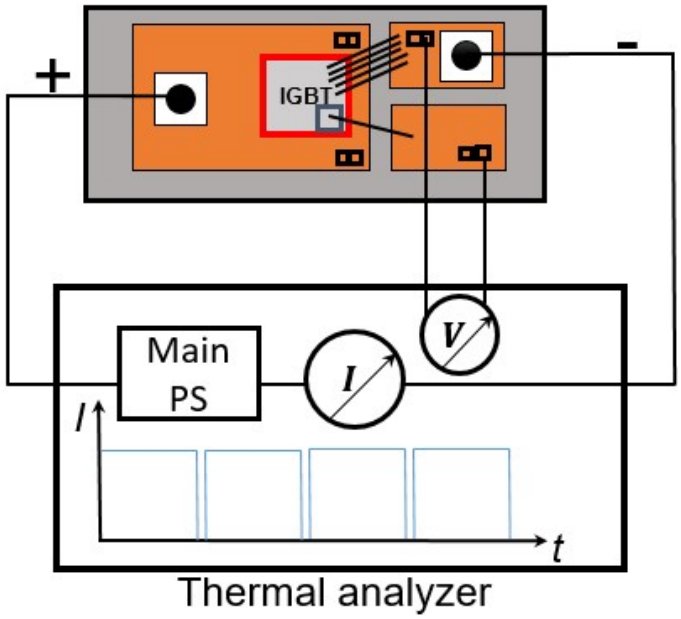


Figure 5.37: schematic overview of the electrical test setup for the one-die cooler

Before the thermal analyzer can be used to measure R_{Th}, a calibration step is performed to characterise the relationship between V_{CE} and T_j. The device under test (DUT) is put into an oven to control its temperature (measured using a thermocouple) and the corresponding V_{CE} value is monitored using the thermal analyzer under a low reading current (5 mA) to limit self heating. Figure 5.38 shows the prepared prototype in the oven for calibration. The resulting calibration curve is presented in figure 5.39.

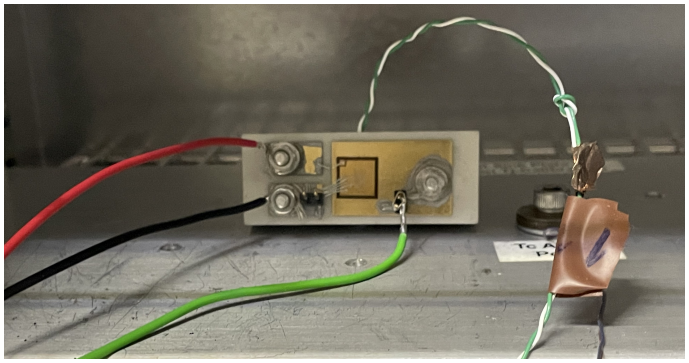


Figure 5.38: schematic overview of the electrical test setup for the one-die cooler

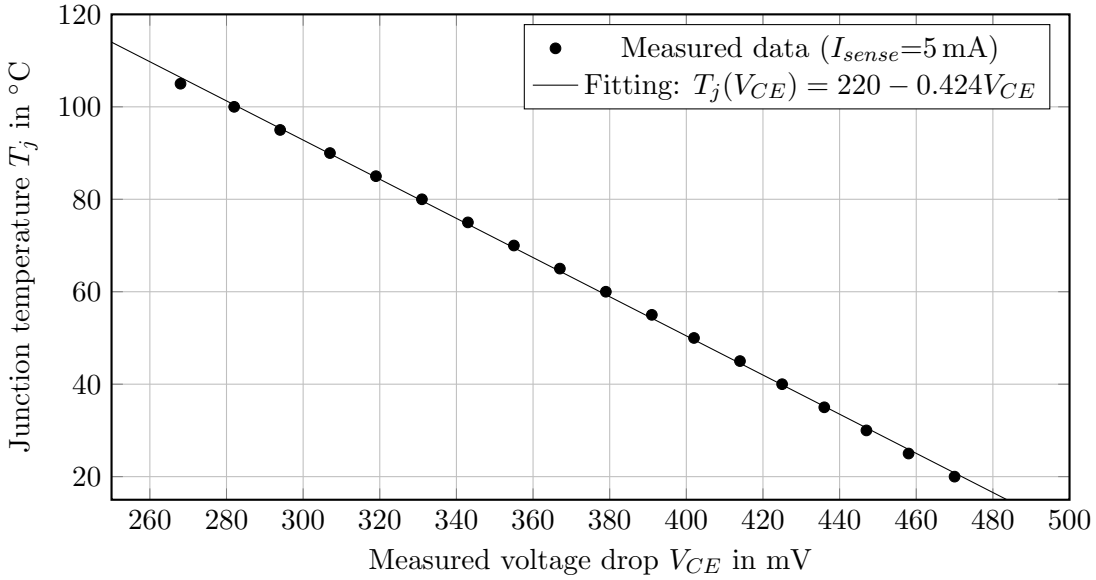


Figure 5.39: Calibration the temperature-sensitive electrical parameter used for junction temperature monitoring: V_{CE} with 5 mA sense current and 9 V gate voltage.

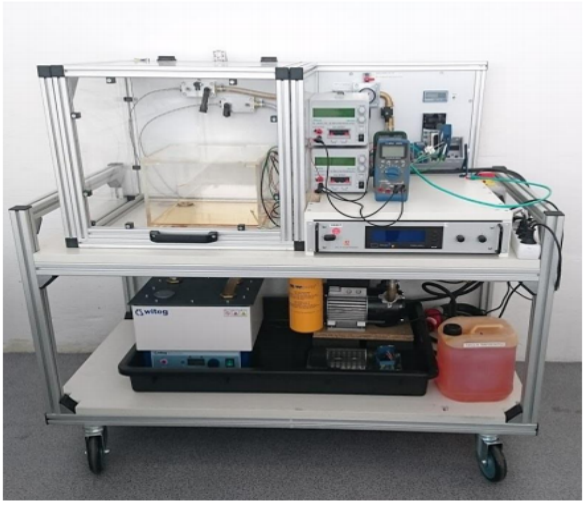
5.3.4 Test setups

Two different test setups are used in this work, to accommodate the different cooling fluids (Trafosynth2, water and Novec 7500). Trafosynth2 is a high-viscosity fluid which needs a dedicated pump. Figure 5.40 shows the test setup for Trafosynth2 and the three coolers attached to the liquid circuit. This setup is located in Kempten, and it is not connected to the thermal analyzer. The junction temperature is measured using a thermocouple mounted directly on top of the IGBT device (see figure 5.40b). In addition to the junction temperature, the liquid flow-rate and the pressure drop of the coolers are measured. Besides that, for the jet cooler with 3.3 mm AlN thickness, the temperatures in the 9 holes of the top AlN layer are monitored (see figure 5.40c).

A similar test setup is installed in Lyon for water and Novec 7500. This setup is connected to the thermal analyzer to perform junction temperature, R_{th}, Z_{th} measurements. Photographs of this test setup is shown in figure 5.41. The jet and channel flow coolers are shown during test in figures 5.41b and 5.41b. Again, the temperature distribution in AlN is measured with thermocouples.

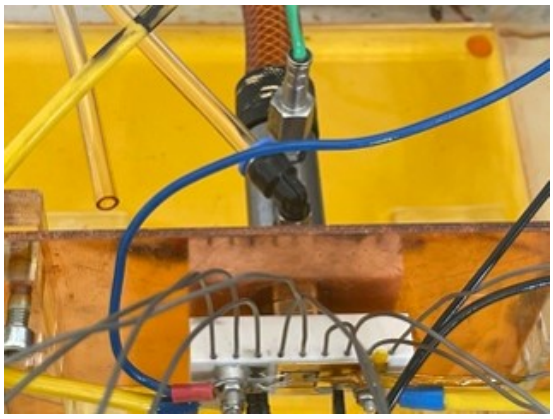
5.3.5 Test results

The test is performed for the three prototypes using three different coolants, Trafosynth2, water and Novec 7500. In this section all experimental results of the three liquids are presented.

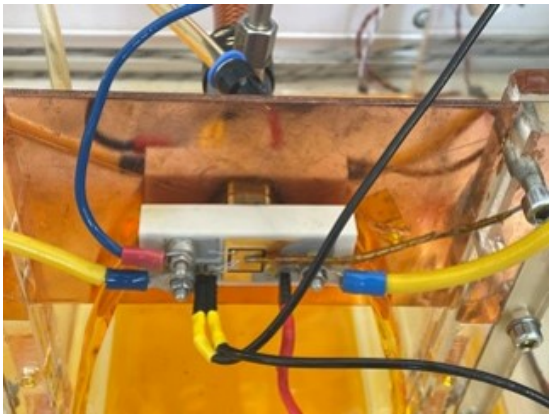


(a) A photograph of the test setup

(b) DUT channel-flow cooler



(c) DUT jet cooler (1.6 mm)



(d) DUT jet cooler (3.2 mm)

Figure 5.40: Test setup for Trafosynth2 liquid and the three devices under test (DUT)

Trafosynth2

The measured and simulated thermal resistances for flow rates ranging from 0.5 L/min to 4 L/min are shown in figure 5.42 for the three coolers. The channel-flow cooler shows the worst performance with high pump power compared to jet coolers. The jet cooler with 3.3 mm AlN thickness performs slightly better than that with1.6 mm AlN. In general, the CFD simulations show good agreement with the experimental results. The standard deviation between the experimental and simulated results varies, falling within the range of 2 to 11 percent, depending on the flow rates and the type of coolers. The main cause for this deviation is probably the pin structure which may differ slightly from that used for the simulation. The pins in the middle of the channel (below the chip) cannot be seen or measured (especially for channel-flow cooler, as some of the pins in the jet impingement cooler can be observed through the inlet). Additionally, measuring the junction tempera-

ture using a thermocouple directly on the die is not accurate, since even a small move of the thermocouple can strongly affect the temperature measurement because of the large temperature gradient over the semiconductor surface. Finally, the quality of the thermal contact between the die and the thermocouple is unknown.

A comparison is made in figure 5.43 between the temperature distribution obtained from the Computational Fluid Dynamics (CFD) simulations and the temperatures measured in the top AlN layer of the jet cooler with a diameter of 3.3 mm. The y-axis displays the temperature difference between the local temperature (measured using thermocouples as shown in Fig. 5.40c and the inlet temperature of 40 °C. The x-axis represents the distance normalized with respect to the half-length of the cooler ($L/2 = 25$ mm), with 0 being the center of the cooler, under the chip.The measured data agree well with the CFD results. The temperature is highest under the die, and decreases in both directions towards the extremities. Higher flow rates reduce AlN temperature, with most of the reducing effect occurring when the flow rate increases from 0.5 L/min to 1 or 2 L/min. The temperature reduction is much less obvious when increasing the flow rate from 3 L/min to 4 L/min.

Water

Water is the most commonly used liquid coolant due to its excellent performance compared to other coolants. Here, the thermal resistance measurement R_{th} is performed with the thermal analyzer, using V_{CE} to estimate junction temperature. The measured and simulated R_{th} values of the three coolers is shown in figure 5.44.

Again, the numerical and experimental data agree well, with small deviations. The jet impingement cooler exhibits a lower thermal resistance at a low pumping power. Both jet impingement coolers offer better performance than the channel-flow cooler, owing to their higher fluid velocity and increased turbulence.

Figure 5.45 shows the AlN temperatures for the jet cooler with 3.3 mm-thick AlN at different flow rates, and demonstrate very good agreement between simulation and experiment.

The thermal impedance Z_{th} of the three coolers is shown in Figure 5.46, for three flow rate values (0.5 L/min, 1 L/min, and 3 L/min). The steady state Z_{th} values correspond to the thermal resistance presented in figure 5.44. This steady state value is reached faster for high flow rate (3 L/min), indicating that heat reaches the cooling fluid faster. This means that its path within AlN is shorter, and therefore that heat spreads less over the cooler surface. This is also true for the 1.6 mm jet impingement cooler, for which steady state is reached faster than for the 3.3 mm cooler. For time constants shorter than 50 ms, there is no difference in behaviour, indicating that heat has not reached the solid-liquid interface yet.

Novec 7500

In this work, Novec 7500 is selected as the dielectric coolant, as mentioned in section 3.4. Figure 5.47 compares the measured and simulated thermal resistances versus pumping power using Novec 7500 as the coolant. It is evident from the graph that the jet impingement cooler displays superior cooling performance, as it offer both lower thermal resistance and pumping power. Both the CFD and experimental data concur that thicker AlN (3 mm) exhibits a lower thermal resistance because of the better heat spreading it offers, resulting in a larger surface area for solid-liquid exchange.

The measured thermal impedance is plotted in figure 5.48 for different flow rates. The same conclusions can be drawn as for water as a coolant, with the differences in time constant being more obvious here: steady state is reached much later for low flow rate (indicating that strong heat spreading is needed before reaching thermal equilibrium). For 0.5 L/min, both the jet cooler with 1.6 mm-thick AlN and the channel cooler offer the same steady state thermal resistance. However, the pumping power is much higher in case of channel-flow design (e.g. about 2.5 times higher pumping power at 3 L/min), see Fig. 5.47.

A comparison between measurement and simulation results of the temperature distribution in the AlN substrate is presented in figure 5.49. Here again, the CFD and experimental results show a very good agreement.

Comparison between the coolants

This section analyzes the results presented so far, to provide a comprehensive understanding of how the coolant type affects the cooling performance.

Thermal resistance Figure 5.50 displays the measured thermal resistances of the three coolers with respect to pumping power using the three coolants. It is evident that water has the most effective cooling performance due to its unique thermal properties such as high thermal conductivity and specific heat capacity. On the other hand, Trafosynth2, which is a dielectric fluid, exhibits the poorest performance due to its high viscosity leading to low coolant velocity. Novec 7500 is an intermediate coolant with good cooling performance. It shows lower pumping power at given flow rate than Trafosynth2 due to its lower viscosity.

With all three fluid, it is possible to achieve the desired thermal performance ($R_{th} < 0.48\,\mathrm{K/W}$ and $W_{pump} < 1\,\mathrm{W}$).

In addition to its cooling performance, Novec 7500 has good electrical insulation properties. The permittivity of Novec 7500 (5.8) is higher than that of Trafosynth2 (3.7), which should result in a more uniform electrical field distribution between AlN and the coolant.

Temperature distribution in AlN Figure 5.51 shows the temperature distribution in the top AlN wall as a function of the normalized distance ($2x/L$) for the three coolants

and two flow rate values. The heat capacity effect of the fluids is evident in the graph. Water, which has the highest heat capacity, exhibits a low temperature on the cooler sides. At a water flow rate of 3 L/min, the side temperature of the AlN is close to the fluid temperature. This is because the cooling mainly occurs below the die. As a result, water does not require the entire surface of the AlN.

In contrast, Novec 7500 has a low heat capacity, and its heat absorption effect is lower. Hence, the cooler requires as much dissipation surface as possible to transfer the heat to Novec 7500. The heat flows to the sides of the cooler to use the entire cooler volume for transferring the heat to the fluid. On the other hand, Trafosynth2 has a higher thermal capacity than Novec 7500. However, due to its higher viscosity and density, a low fluid velocity (especially near walls) is achieved, which negatively affects the cooling performance. Additionally, less turbulence is produced in the channel due to the lower velocity. These factors explain the better AlN temperature distribution of Novec 7500 compared to Trafosynth2.

Thermal impedance The thermal impedance is only measured for water and Novec 7500. The data are presented in figure 5.52. For water, steady state is achieved in approximately 2–3 seconds at a flow rate of 3 L/min, whereas Novec 7500 requires approximately 20 seconds at the same flow rate. This highlights the superior cooling capabilities of water, and confirms that less heat spreading is required over the cooler surface for water than for Novec 7500. At low flow rates, the thermal resistance of Novec 7500 is found to be very high. However, increasing the flow rate from 0.5 L/min to 3 L/min results in a nearly 40 % decrease in thermal resistance. In contrast, water shows a much smaller change in thermal resistance with varying flow rates ($\sim$ 20 % from 0.5 L/min to 3 L/min).

5.4 Summary

In this chapter, the optimization of a single die module cooler design is conducted through comprehensive CFD simulations. Initially, an investigation is carried out on an AlN cooler devoid of any internal pin-fin structures. The outcomes of this analysis highlight that achieving the target conditions, characterized by a thermal resistance lower than 0 48K/W and a pumping power lower than 1W, is unattainable without the pin-fins. Subsequently, the introduction of pin-fin structures is explored, leading to a significant enhancement in cooling performance and enabling the attainment of the specified target conditions.

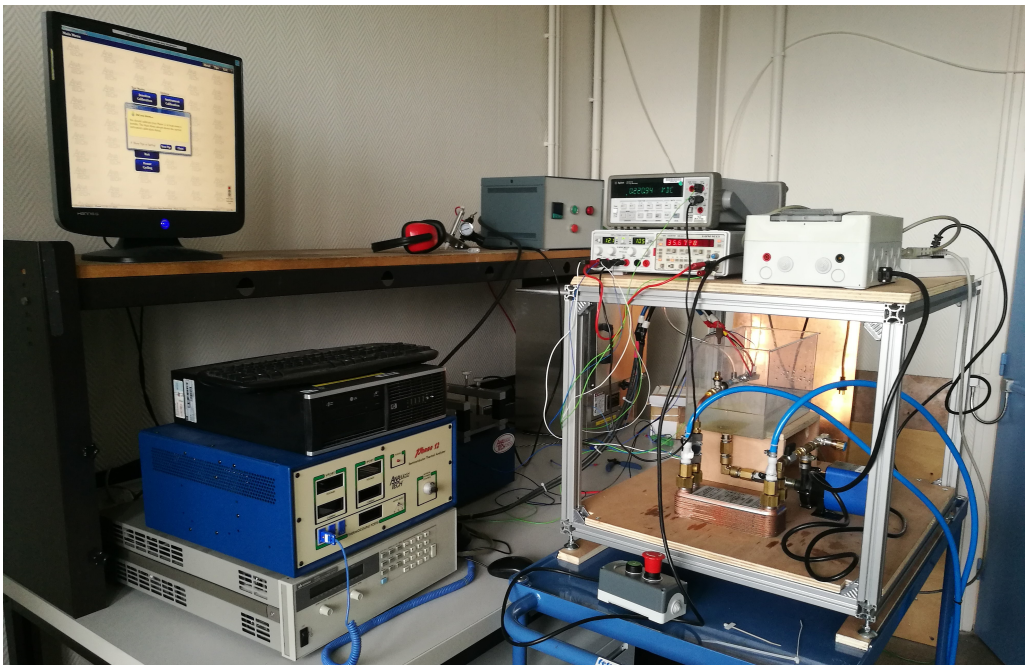
Several pin-fin structures, including cylindrical, square, and conical shapes, are examined in detail. The results demonstrate that conical pins exhibit superior cooling performance, while square pins exhibit less favorable performance characteristics. Additionally, it is observed that a cooler with a relatively thick AlN baseplate leads to improved cooling

performance due to the improve heat spreading it allows.

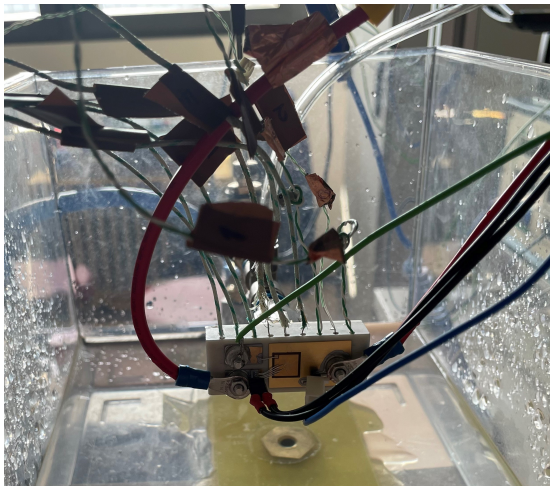
The investigation extends to two distinct cooling concepts: jet impingement and channel flow cooling. The results reveal that inline pins are more effective when integrated into a jet impingement cooler, whereas staggered pins yield superior performance when utilized in a channel-flow cooler configuration.

Furthermore, different coolant options are compared, with water demonstrating the most effective cooling performance. Novec 7500 is identified as a viable alternative to conventional dielectric fluids like Trafosynth2, exhibiting favorable cooling capabilities.

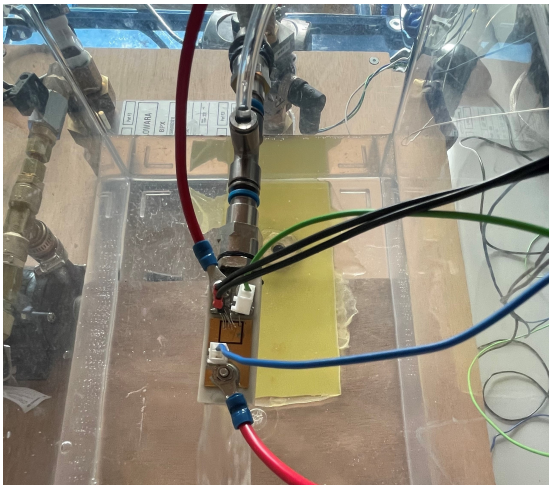
Following the cooler optimization process, a thermal experimental test is conducted to validate the CFD results. This experiment involves the measurement of thermal resistance, pumping power and the temperature distribution in AlN. Remarkably, the CFD and experimental findings exhibit strong agreement, bolstering the confidence in the simulation results. This alignment paves the way for further simulations aimed at optimizing the design of multi-die modules, promising enhanced cooling performance and efficiency.



(a) A photograph of the test setup



(b) DUT jet cooler



(c) DUT channel-flow cooler

Figure 5.41: Test setup for water and Novec 7500 liquids and the jet and channel-flow coolers under test (DUT)

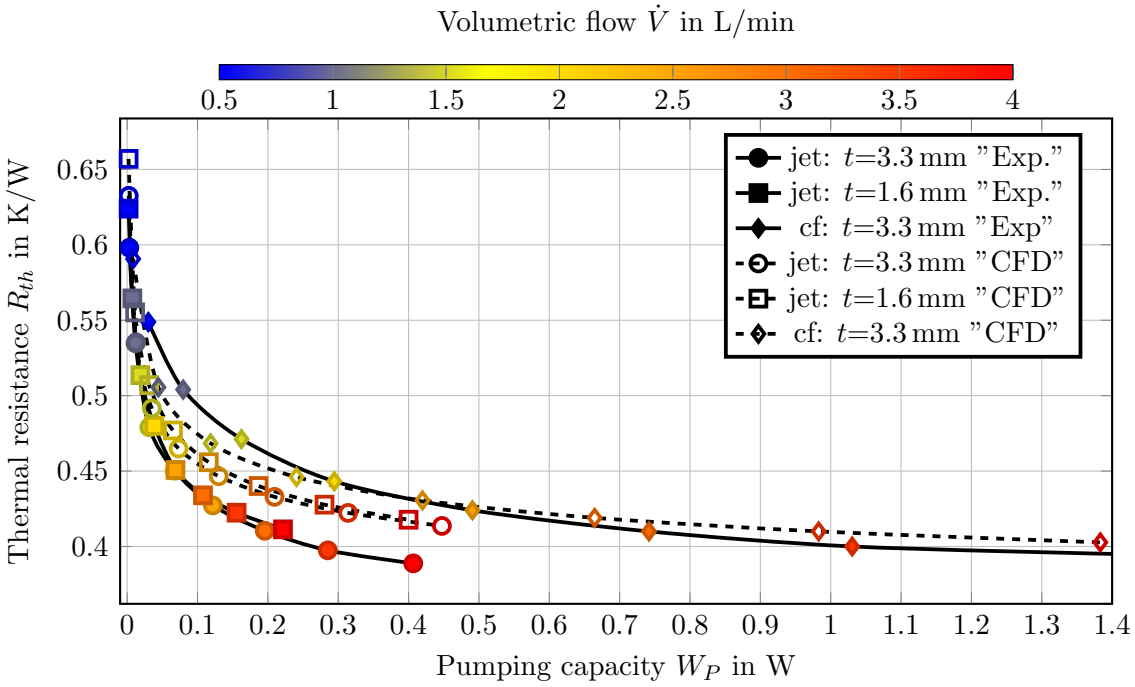


Figure 5.42: The measured thermal resistance compared to the numerical results over the pumping capacity at different Trafosynth2 flow rates

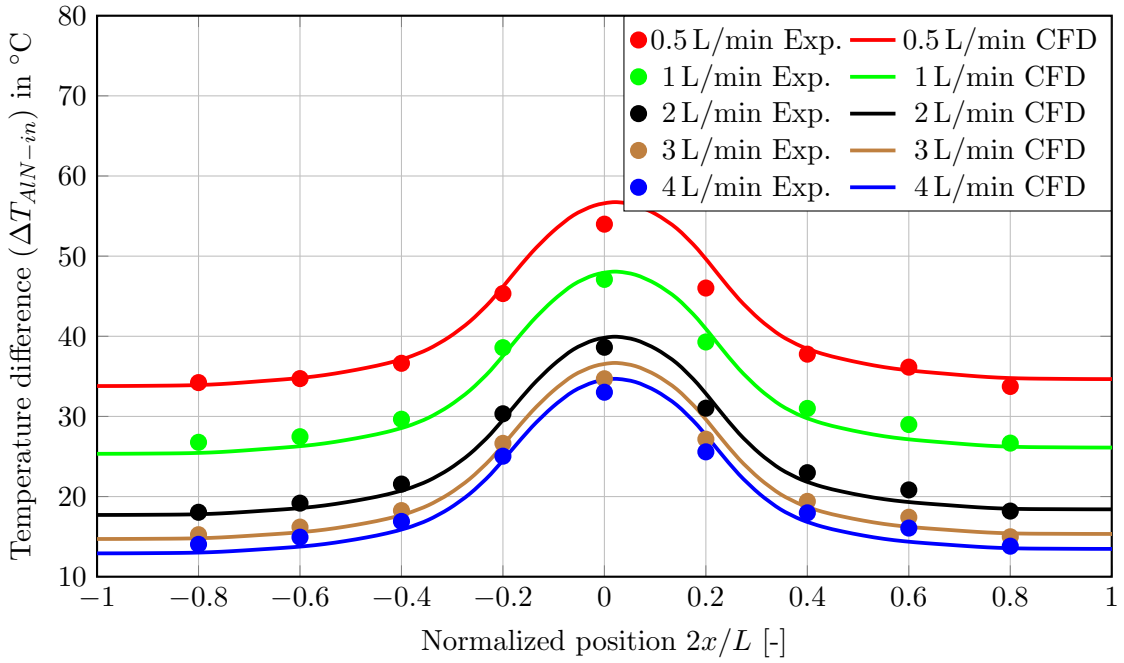


Figure 5.43: The temperature distribution in the AlN for the jet cooler. experimental (Exp.) and numerical (CFD) data with Trafosynth2 as coolant.

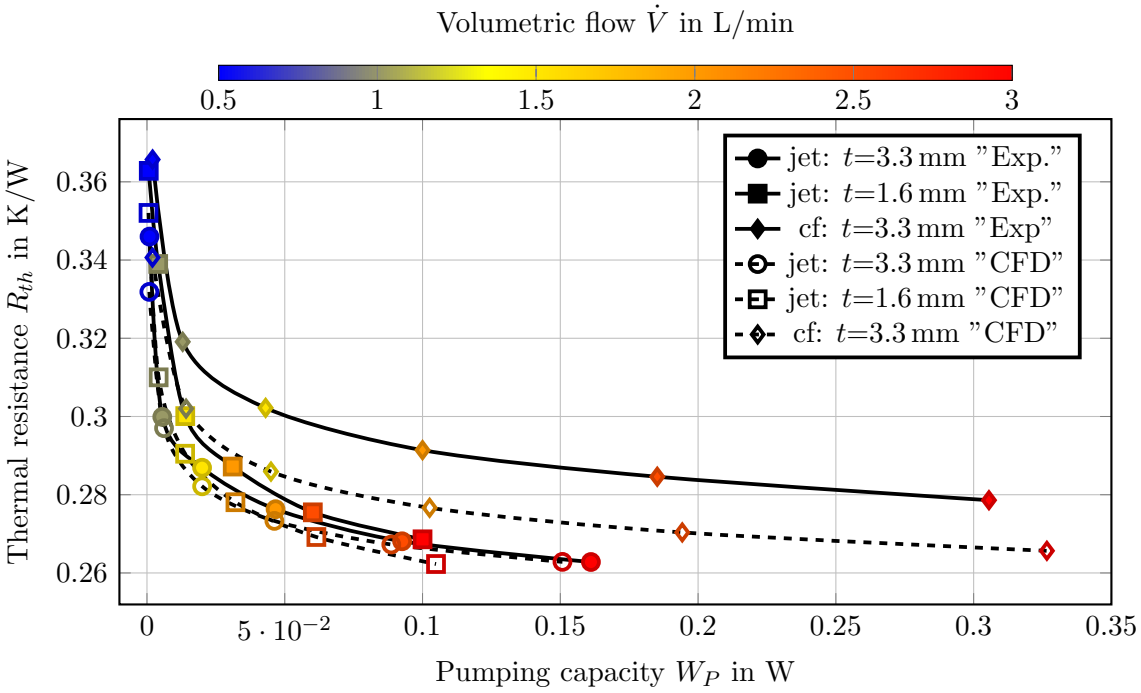


Figure 5.44: The measured thermal resistance compared to the numerical results over the pumping capacity at different water flow rates

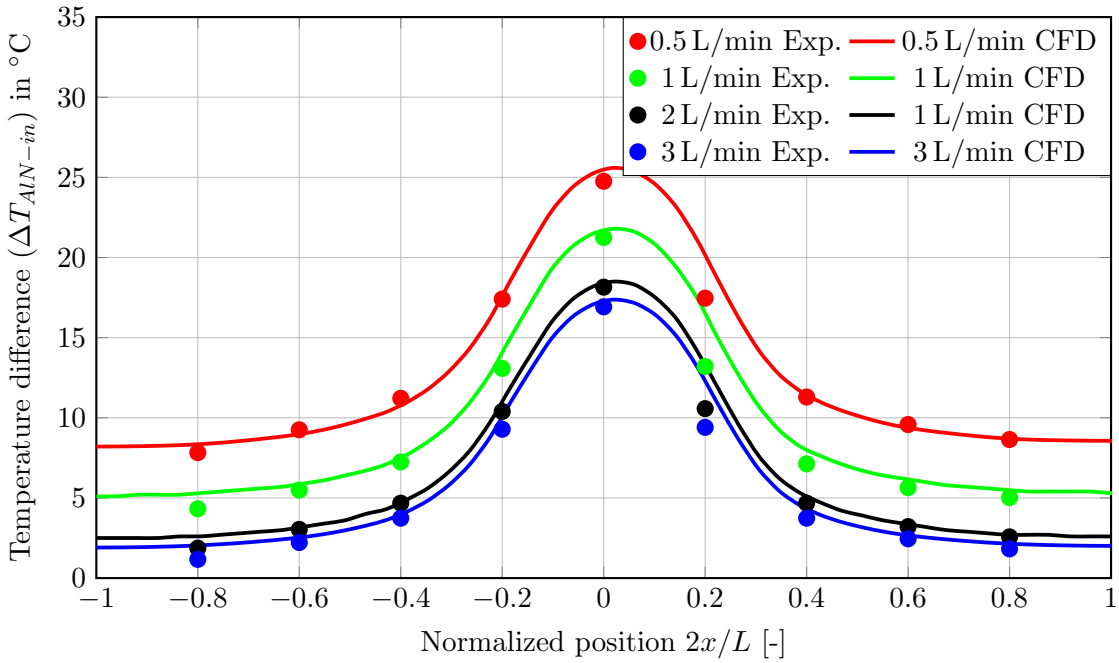


Figure 5.45: The temperature distribution in the AlN for the jet cooler experimentaly (Exp.) and numerically (CFD) with water as coolant

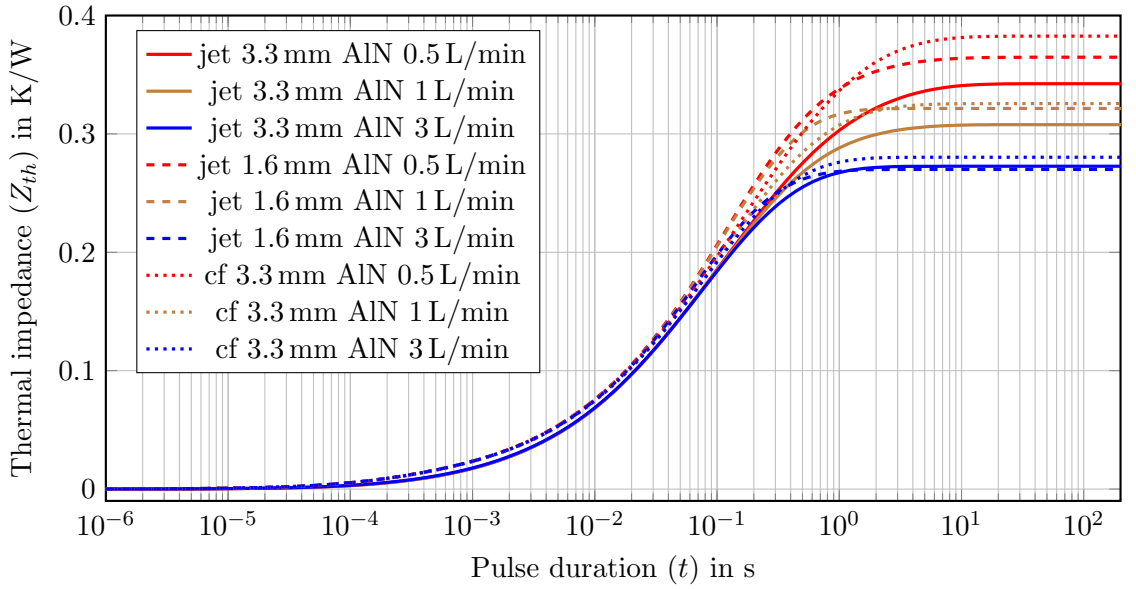


Figure 5.46: Measured thermal impedance (Z_{th}) for the three coolers with water as coolant at different flow rates

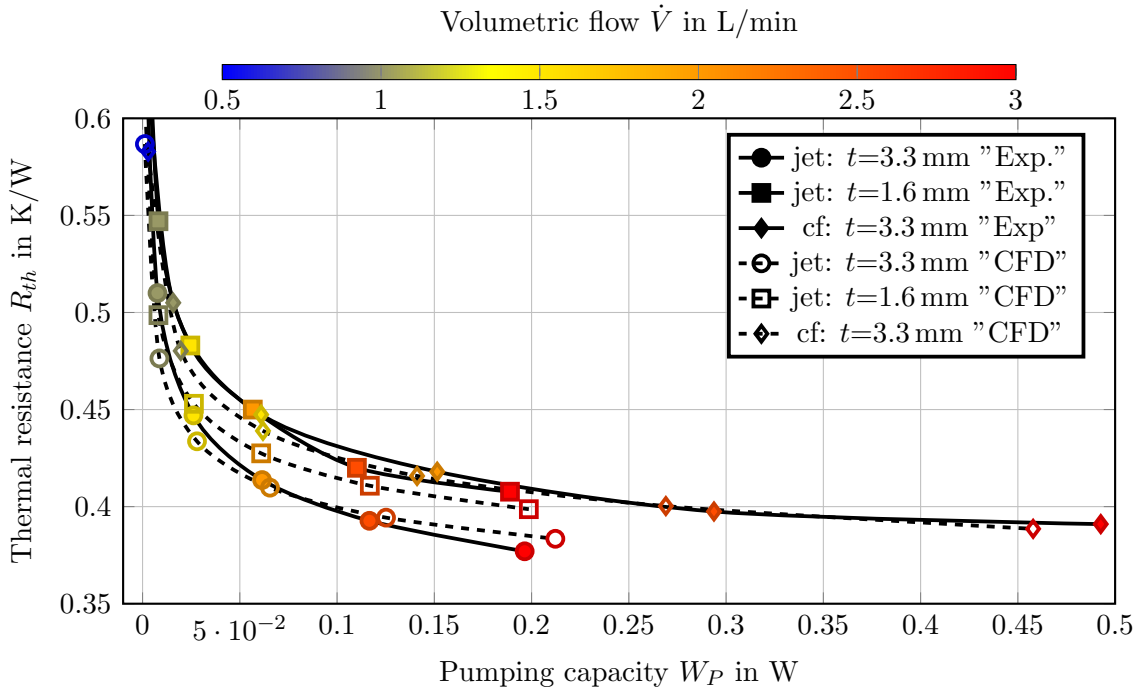


Figure 5.47: Measured and simulated thermal resistance for the three coolers at various Novec 7500 flow rates

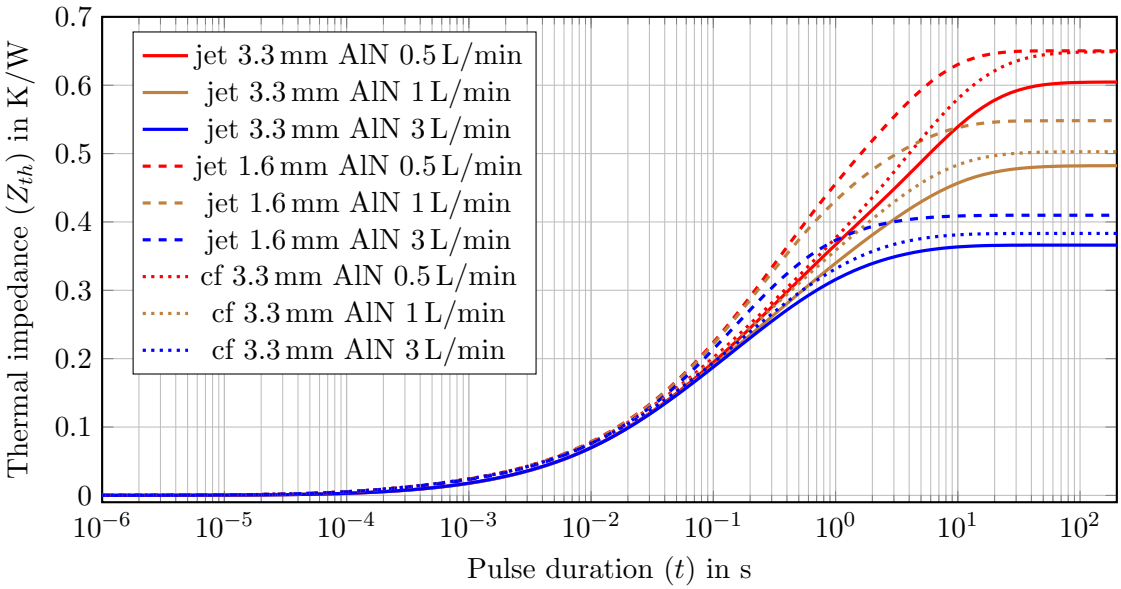


Figure 5.48: Measured thermal impedance (Z_{th}) for the three coolers with Novec 7500 as coolant at different flow rates

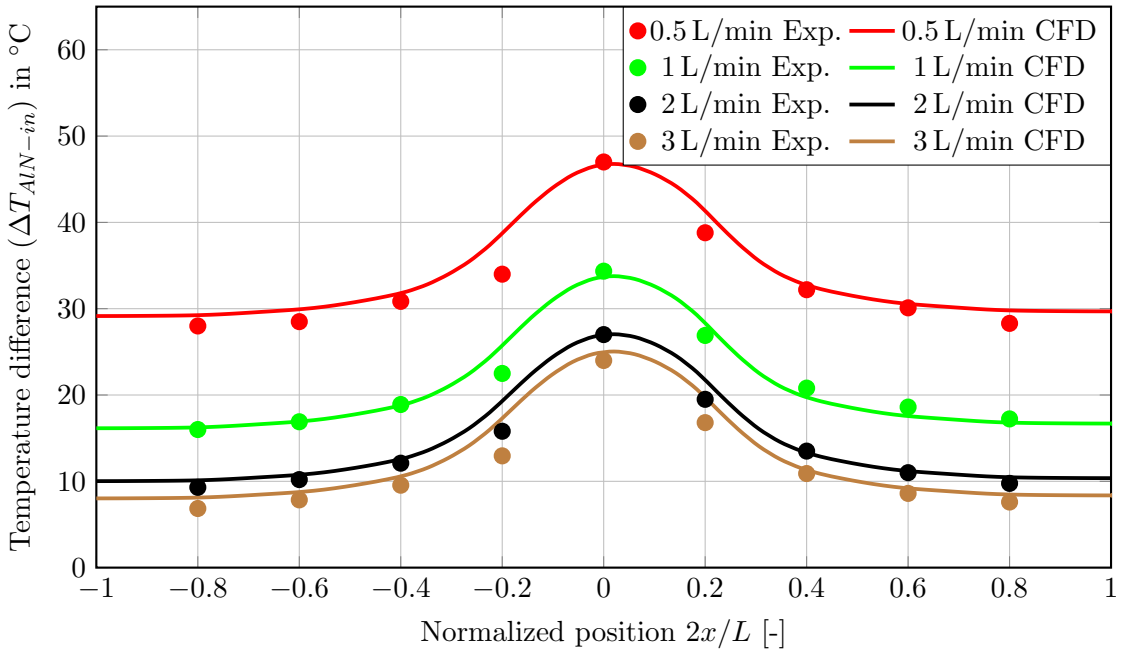


Figure 5.49: The temperature distribution in the AlN for the jet cooler experimentaly (Exp.) and numerically (CFD) with Novec 7500 as coolant

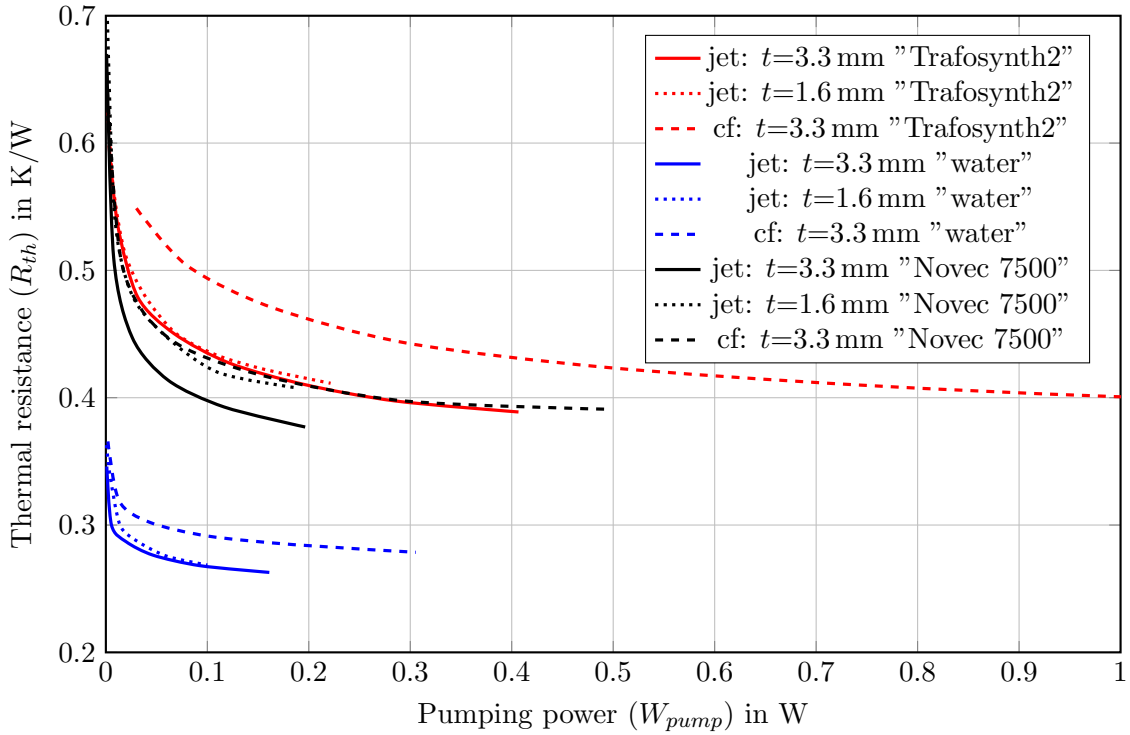


Figure 5.50: The measured thermal resistance over the pumping capacity with the three coolants

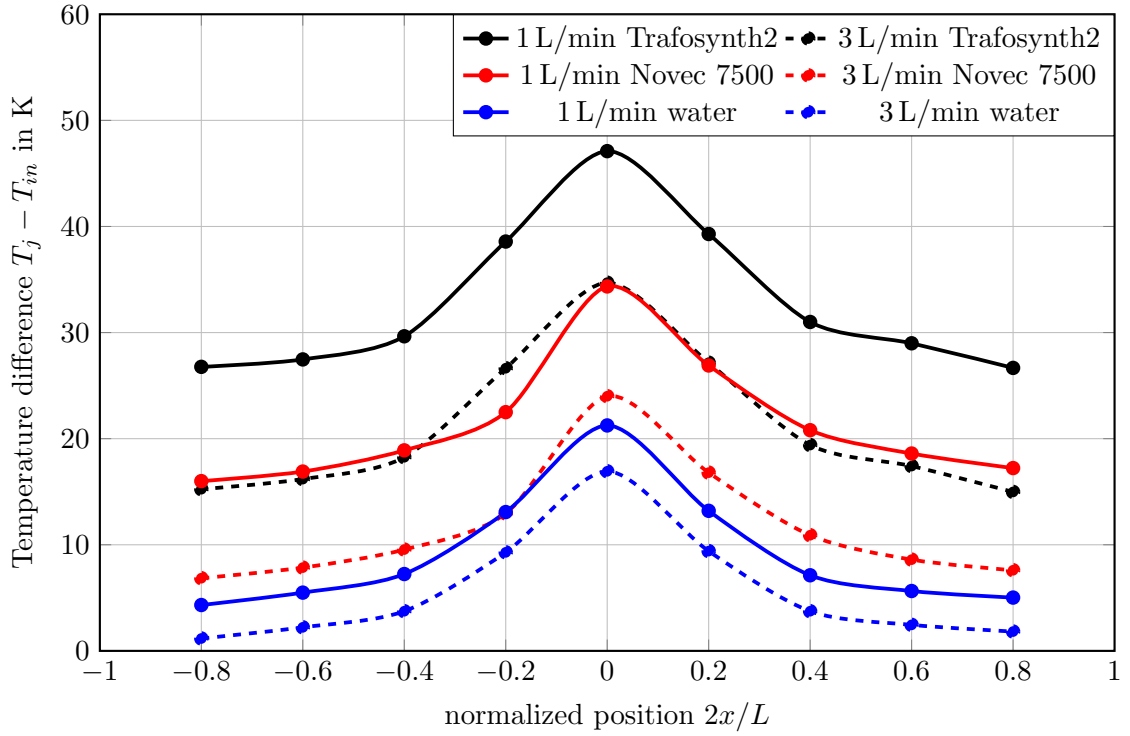


Figure 5.51: Temperature distribution in the AlN for the jet cooler ($t = 3.3\,\mathrm{mm}$).

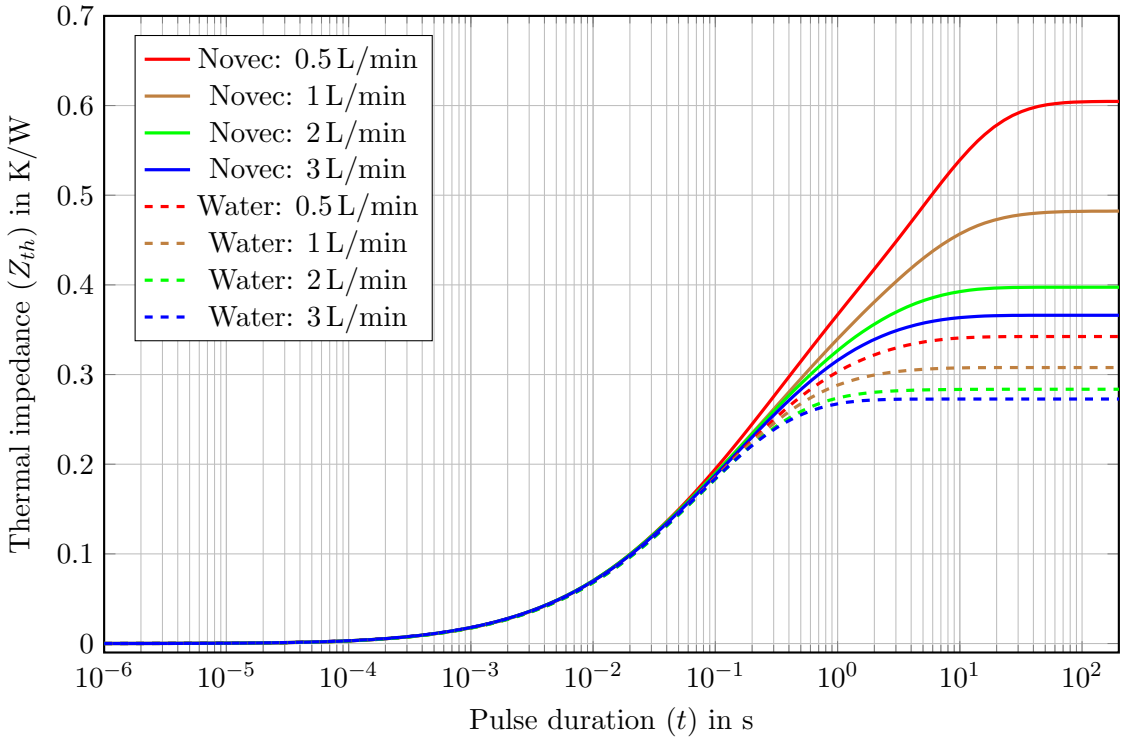


Figure 5.52: Measured thermal impedance (Z_{th}) for the jet cooler with two different coolants (water and Novec 7500) at different flow rates

Chapter 6

Cooling system for 20 kV module

In the last section, the focus was on the cooling of single-die power modules. However, a real power module is more complex and consists of many components. This requires a more sophisticated cooling system, in which the cooling fluid is guided to extract heat from several places, with a single inlet and outlet connection for a complete cooler.

As mentioned in chapter 1, the original idea was to build a half bridge module with two 10 kV SiC MOSFETs. By connecting the two switches in series 20 kV blocking voltage for the entire module could be demonstrated. Due to the unavailability of the 10 kV devices, an alternative approach was developed by SuperGrid Institute [4]. It is based on a series connection of six 3.3 kV MOSFETs (GeneSiC, G2R50MT33-CAL). To balance the voltage (statically and dynamically) a sophisticated snubber circuit is required, which generates additional losses. One snubber circuit is connected across each SiC device. Figure 6.1 shows the electrical connections of the 20 kV module.

6.1 Module Design

6.1.1 Target performance

The aim of this work is to keep the junction temperature of the SiC-MOSFETs below 100 °C at a fluid inlet temperature of 40 °C.

The total power losses of a MOSFET is the sum of conduction and switching losses. If we assume on-time to be half of the switching period (50 % duty cycle), and the drain current to be constant, the conduction losses (Joule losses) correspond to:

$$P_{cond} = \frac{1}{2} R_{on} \times I_D^2 \tag{6.1}$$

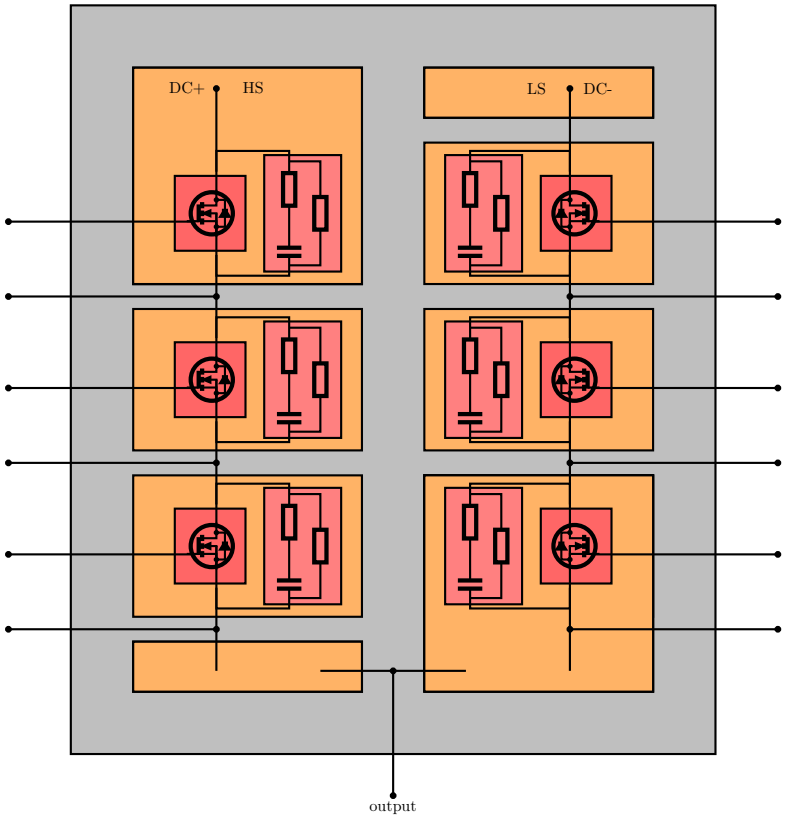


Figure 6.1: Electrical circuit of the half-bridge power module with 3× 3.3 kV SiC MOSFETs in series for each of the two switches, and the associated RC snubber circuits to balance voltage across the MOSFETs.

The switching losses can be estimated as [149]:

$$P_{SW} = \frac{1}{2} I_D \cdot V_{DS} \cdot (t_{off} + t_{on}) \cdot f + \frac{1}{2} C_{OSS} \cdot {V_{DS}}^2 \cdot f \tag{6.2}$$

All the parameters (R_{on}, t_{on}, t_{off}, C_{OSS}) in this equation are given in the MOSFET datasheet. In particular, the drain-source on-resistance R_{on} is 65 mΩ at $T_j = 100\,°C$ and 20 V gate-source voltage V_{GS}. Assuming 2500 V drain-source voltage (V_{DS}) and 20 kHz switching frequency, the power losses of the SIC-MOSFET can be estimated as shown in figure 6.2 as a function of the drain current.

The original goal of the work was to build a 20 kV module with 15 A rating, the same ratings as the 10 kV MOSFETs. The 3.3 kV dies used instead have a rated current of 49 A. However, with such a high current, the SiC MOSFETs would dissipate 230 W each. As a consequence, a more realistic goal of operating the module at 25 Ais set, to use the dies at at least half of their rated current. At this current level, total heat losses are about 120 W at 20 kHz switching frequency (f). The total losses are then similar to those assumed for single-die module (125 W). However, due to the much smaller chip size (8.9 mm×3.676 mm

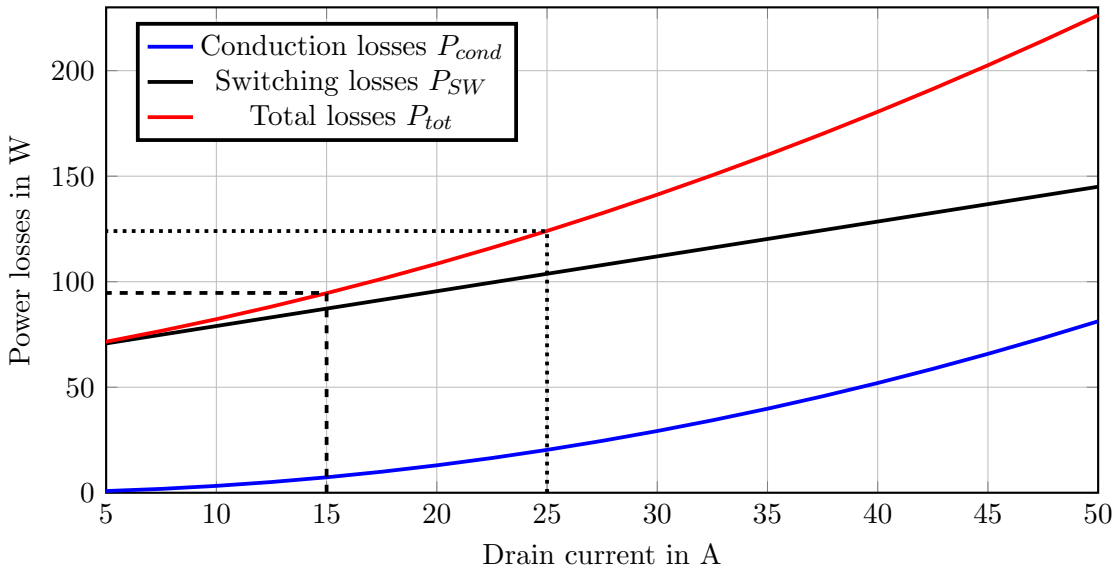


Figure 6.2: The power losses of the 3.3 kV MOSFETs as a function of its drain current at 20 kHz switching frequency and 2.5 kV nominal drain-source voltage

for the 3.3 kV chips instead of 8.1 mm × 8.1 mm for the 10 kV MOSFETs considered in the previous chapter), the heat density is almost doubled, which makes the cooling task more demanding.

At 120 W, each 3.3 kV MOSFETs experiences a power density of $q = 367\,\mathrm{W/cm^2}$. Keeping $T_j < 100\,^\circ\mathrm{C}$ at 40 °C inlet temperature ($\Delta T < 60\,\mathrm{K}$) requires a thermal resistance R_{th} of less than 0.5 K/W. Furthermore, the objective of this research is to achieve a highly uniform temperature distribution across all dies, resulting in similar junction temperatures (R_{th}).

6.1.2 Implementation

Before optimizing the cooling structure, some design choices are made *a priori*, for manufacturing reasons: first, two identical coolers (one for each series of 3 series-connected MOSFETs) are used for each module. This simplifies manufacturing by making the parts smaller, and improves assembly yield (fewer components to assemble, and only half of the module has to be replaced in case of failure of one component). From a design and test point-of-view, half modules are also faster to optimize, simulate and test.

A second design choice is the size of the coolers, at 50 mm wide and 100 mm long. The length is dictated by manufacturing constraints; the width is chosen to allow fitting all the components while leaving a large ceramic border free (5 mm) for electrical insulation purposes.

Finally, because of their relative complexity (29 surface-mount components each), it is

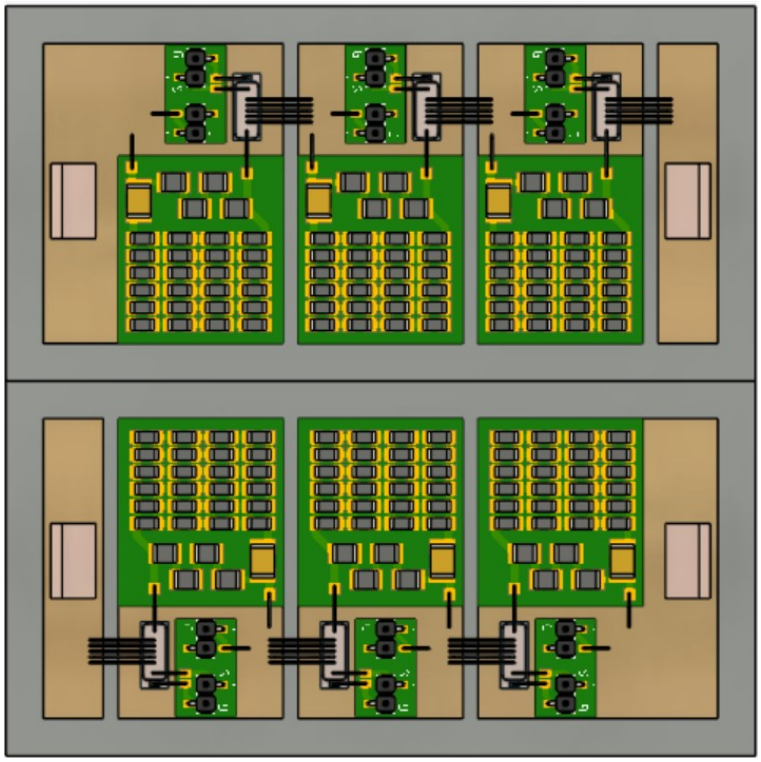


Figure 6.3: The top view of the planned 20 kV module with six 3.3 kV SIC MOSFETs and six snubbers on AlN coolers with all the parts and electrical connections on it

decided to build the snubber circuits as sub-assemblies on separate AlN DBC substrates. These populated substrates are then assembled on the metallized coolers. From a thermal point of view, it would be preferable to pattern the metallization of the coolers and mount the snubber components directly, but this would substantially complicate manufacturing.

Figure 6.3 shows the top view of the 20 kV half-bridge module with six dies. A half-module cooler consists of three dies and three snubbers. The snubber design is presented further below. Besides the MOSFETs and the snubbers, a small PCB is used to connect the gate, source and drain of the MOSFETs. SMD pins are soldered onto the PCBs for the outside connections. Power connectors are also soldered on both ends of each cooler to carry the high voltage and current to and from the module.

Figure 6.4 shows an AlN cooler with all the power-dissipating parts and the dimensions. Four copper pads are brazed on the top AlN surface, 5 mm distance from the edges of the cooler (for electrical insulation). The first copper pad is longer than the others, at 32 mm, because it hosts the DC+ connector. The fourth copper pad is smaller, as it does not receive MOSFET nor snubber (only the DC- power connector).

The ideal position for the dies would be in the middle of the copper pads to maximize the heat spreading effect. However, their actual position is dictated by maximum wirebond

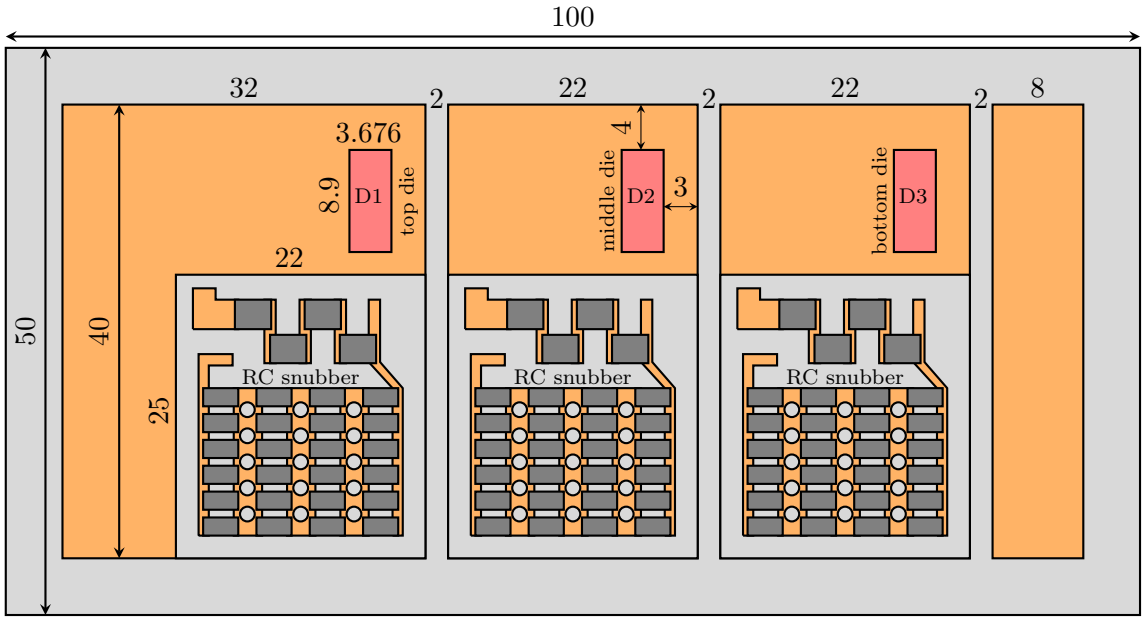


Figure 6.4: The top view of the used design for the CFD simulation

length and by the presence of snubbers. As a consequence, the dies are placed 4 mm from the top edge of the copper, about 2 mm away from the snubbers, and 3 mm from the right edge of the copper pads. Figure 6.5 shows a schematic cross-section of the module. The

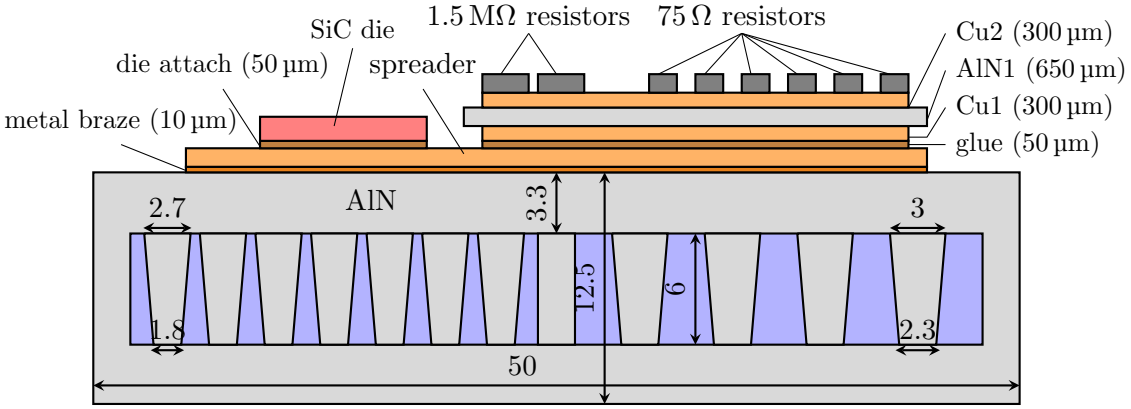


Figure 6.5: Structure considered for the design, showing the material of the layers and design parameters

figure details the materials used. The AlN cooler has an overall height of 12.5 mm, which is the clearance needed to block a voltage of 20 kV. The pins are 6 mm long, which is the optimal length of pins optimized for the single-die modules (see chapter 5). The top AlN is 3.3 mm, also in accordance with the single-die optimization. Copper pads are brazed onto the cooler. A SiC die is sintered onto the copper and a snubber is bonded with some conductive adhesive.

Table 6.1: Components used for the snubbers

Original component	Replaced component	Qty	Manufacturer part number
75 Ω resistor	11 Ω resistor	24	CRCW120611R0FKEAHP
1.5 MΩ resistor	150 Ω resistor	4	CRCW1210150RFKEA
680 pF capacitor	0 Ω resistor	1	ERJ-S120R00U

6.1.3 Snubber

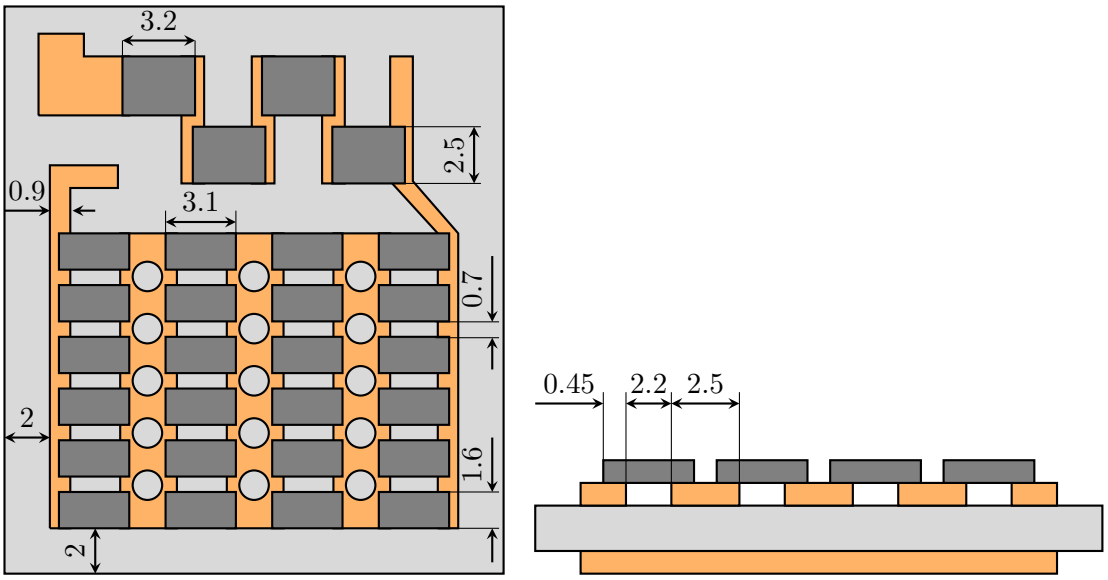
The snubbers are used for balancing the voltage across the MOSFETs, both when they are switching (dynamic balancing) and when they are in the off state (static balancing). Static balancing is performed thanks to high-values resistors (4 series-connected 1.5 MΩ resistors). Dynamic balancing relies on a RC circuit with much smaller resistor values (24 resistors connected in series and parallel, 75 ohm each). Overall, at the rated voltage/switching frequency, each snubber is expected to dissipate 54 W.

However, for the thermal tests performed in this work, there is no need to apply high voltage to the system. For safety and practical reasons, the thermal tests are performed at low voltage. In order to get the same heat losses with only 20 V being applied on the snubbers (and no switching), the snubber components are replaced with different values. The capacitor is replaced with zero-ohm resistor since it doesn't dissipate significant power, and because there is no dynamic balancing to perform. The twenty-four 75 Ω resistors are replaced with 11 Ω and the four 1.5 MΩ resistors with 150 Ω resistors. To achieve approximately 54 W power dissipation, a current of 2.7 A is applied to each snubber. The 11 MΩ resistors dissipate 2.22 W (equivalent to 44.76 W/cm^2) each, while the 150 Ω resistors dissipate 0.17 W (equivalent to 2.13 W/cm^2) each. Table 6.1 shows the components used for the thermal tests ("Replaced component") and those used for the high voltage snubbers ("Original component").

Figure 6.6 shows a detailed view of the snubber design. Figure 6.6a shows the top view of the snubber and the copper structure. The right figure (6.6b) is a cross section of the snubber to see the layers of the DBC/snubber. The twenty-four small resistors have a size of 3.1 mm × 1.6 mm. The four larger resistors are 3.2 mm × 2.5 mm. It should be noted that all these components have a small contact surface with the DBC metallization (0.45 mm wide), which limits the thermal dissipation capability. This corresponds to a maximum thermal resistance of $R_{th} = 51.8\,\mathrm{K/W}$ and a specific thermal resistance of $r_{th} = 2.57\,\mathrm{cm^2K/W}$."

6.2 Numerical optimization of the three die coolers

Building on the findings of the previous chapter, this CFD based optimization aims at finding the best cooling approach and cooler geometry. First, the model definition and



(a) The components of the snubber and the to structure of the top side of the snubber

(b) Cross section in middle of the snubber

Figure 6.6: The design of the snubber

simulation parameters are described, before moving on to the parametric analysis.

6.2.1 CFD setup

The first step in CFD calculation is to design the problem as a CAD file. All important parts are considered in the numerical simulations. These parts are the SiC chips and the snubbers with their resistors, as they are the heat sources in the system, and the cooler structure. The snubber capacitors do not generate significant heat so they are not included in the CFD simulations. Connectors, wirebonds, etc. are not considered either, as they have little effect on the cooling performance.

After preparing the CAD design of the 3-die module, the material properties of the system are defined for the CFD solver. The snubber is a DBC (Direct Bonded Copper) substrate consisting of a tile of AlN material with a copper foil bonded on both sides. Resistor elements are soldered onto the DBC. The resistors are modeled as homogeneous block of Al_2O_3 and the solder interface is ignored.

The thermal properties of the used materials are shown in section 3.1, p. 35 and thickness are defined in table 3.2. The parameter names refer to figure 6.5.

The numerical setup remains that detailed in pervious chapter (section 5.1). In particular, a value of $y^+ < 3$ for a flow rate up to 5 L/min, is considered here. The mesh structure in the fluids and solids is similar to that used for the single-die module in chapter 5. However, the mesh size of the SiC dies is adjusted due to their smaller size. Also, a

finer mesh is used for snubbers components since they are tiny. Figure 6.7 shows the used mesh for the dies and snubber components.

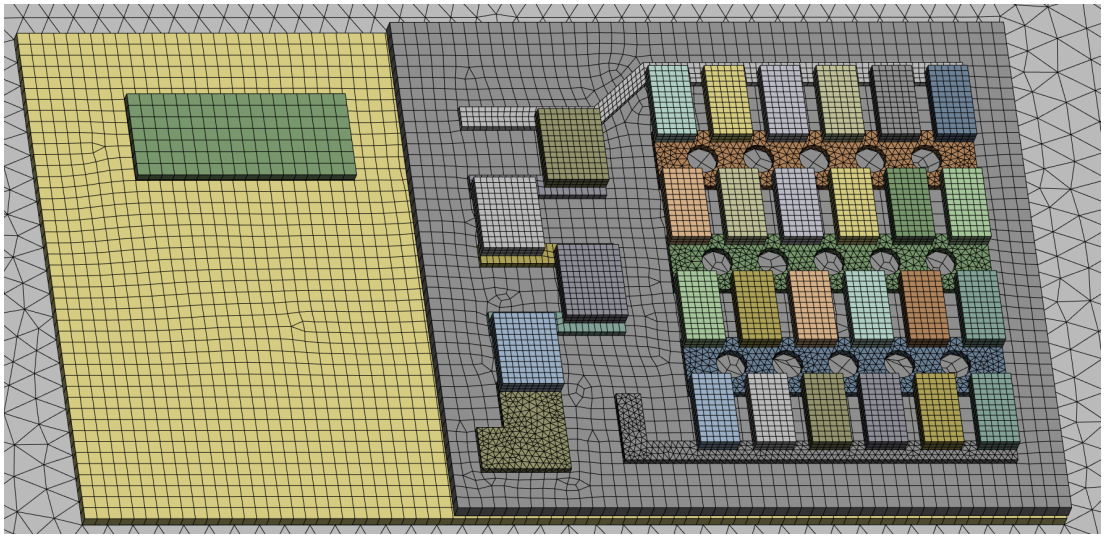


Figure 6.7: The used mesh for the dies and snubber elements for the CFD calculations

Regarding the boundary conditions, all external walls are defined as adiabatic, and get non-slip ($\mathbf{v} = \mathbf{0}$) conditions. To ensure energy conservation, liquid-solid and solid-solid interfaces are given the "Conservative Interface Flux" boundary condition. There is a constant mass flow at the inlet, at a temperature of 40 °C. A relative zero-pressure is applied at the outlet. A constant heat flow of 120 W is applied to each SiC die. A total heat dissipation of 53.3 W (2.22 W each) is set for all small resistors and 0.7 W (0.17 W each) for the big resistances. Table 6.2 summarizes the defined boundary conditions for the CFD simulations.

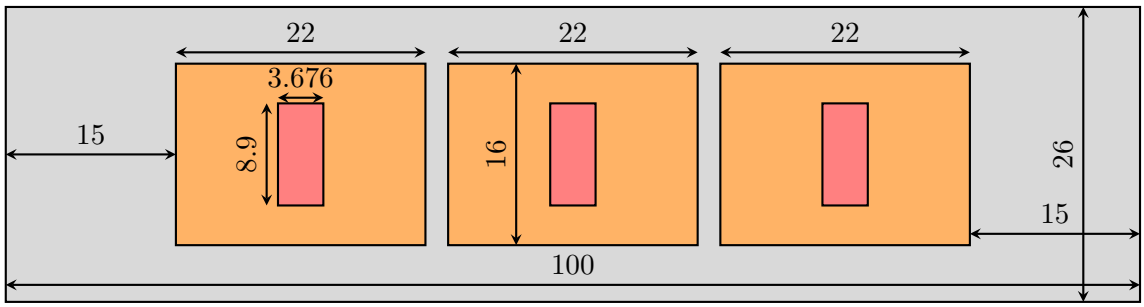
Table 6.2: Boundary conditions

Boundary	velocity v	pressure p	temperature T
inlet	constant mass flow	calculated	313.15 K
outlet	zero gradient	zero pressure	calculated
walls	-	-	zero gradient (0,0,0)
fluid-solid interface	no-slip ($\mathbf{v} = \mathbf{0}$)	calculated	Conservative Interface Flux
solid-solid interface	-	-	Conservative Interface Flux
SiC dies	-	-	120 W each
small resistors	-	-	2.22 W each
big resistors	-	-	total heat: 0.17 W

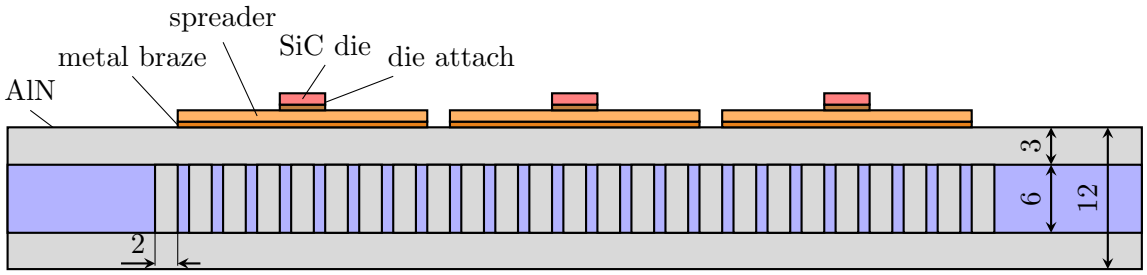
The CFD simulation for each parameter is stopped when the numerical error (convergence) drops below a value of 5×10^{-5} for the pressure, 10^{-6} for temperature and 5×10^{-4} for all other quantities.

6.2.2 Effect of the pin layout

Proposed layouts



(a) Top view

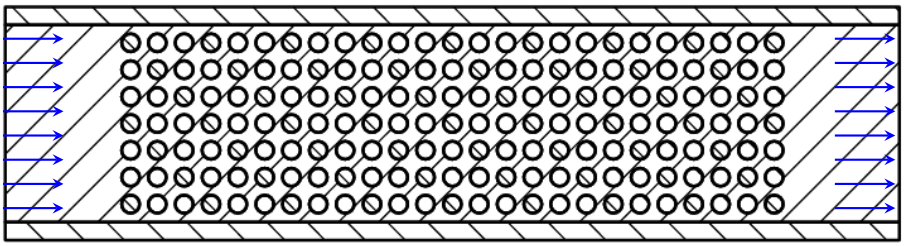


(b) cross section in the middle of the system

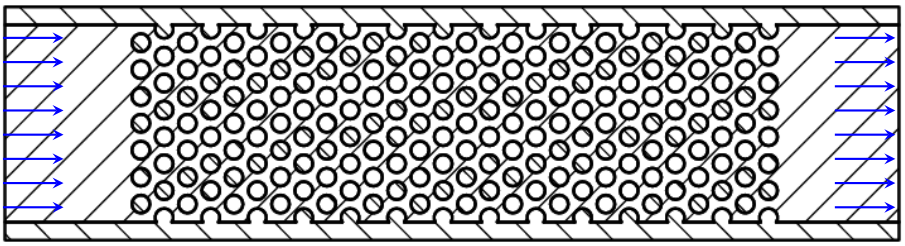
Figure 6.8: The design of the simplified module with three dies

For this first analysis, a simplified version of the cooler, where only the chips are considered (and not the snubbers) is used, to save computing time and storage space. Figure 6.8a shows the corresponding geometry. Three 22 mm × 16 mm copper sheets are brazed onto the AlN. A 3.676 mm × 8.9 mm chip is placed onto the middle of each copper plate. The symmetries of the geometry are used to reduce computation time. Based on the results from chapter 5 the pins have a diameter of 2 mm and a height of 6 mm; for jet impingement, the inlet has a diameter of 7.5 mm.

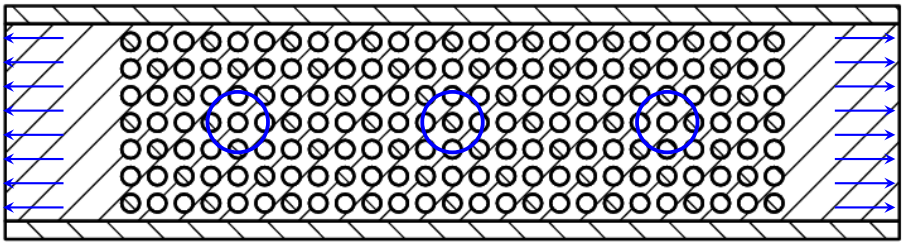
Chapter 5 showed that jet impingement offers better performance than channel flow cooling, with in-line pins preferable over a staggered layout in case of jet impingement cooling. With channel flow, the staggered pins provide more effective heat dissipation. Therefore, four cooling designs are examined to find the best cooling method for the multi-die nodes. The first design is a channel flow cooler with inline pins, figure 6.9a. The second design has the same cooling principle but with a staggered pin order, figure 6.9b. A multi-jet (three inlets, figure 6.9c) cooler design with inline pins is also investigated. The final design combines jet impingement and channel. In this design (figure 6.9d), a liquid jet hits the middle die with inline pins and then flows through staggered pins under the side SiC dies.



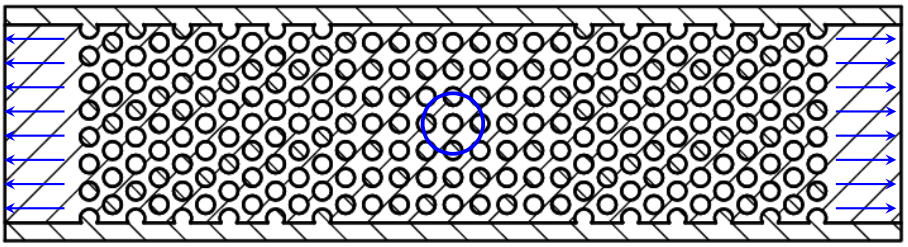
(a) Channel flow with inline pins



(b) Channel flow with staggered pins



(c) Three jets under each die with inline pins



(d) One jet under middle die with mixture pins order

Figure 6.9: The different cooling methods and pin fin structures considered for the three die cooler

Pin layouts – CFD results

Simulations are run for a flow rate ranging from 0.5 l/min to 5 l/min. For the design with three jets, the same flow rate is applied thrice, which means that the total flow rate is three time more than the other designs. Figure 6.10 shows the thermal resistance of the hottest die over the pumping power.

The channel flow design with inline pins shows a low pumping power due to low fluidic

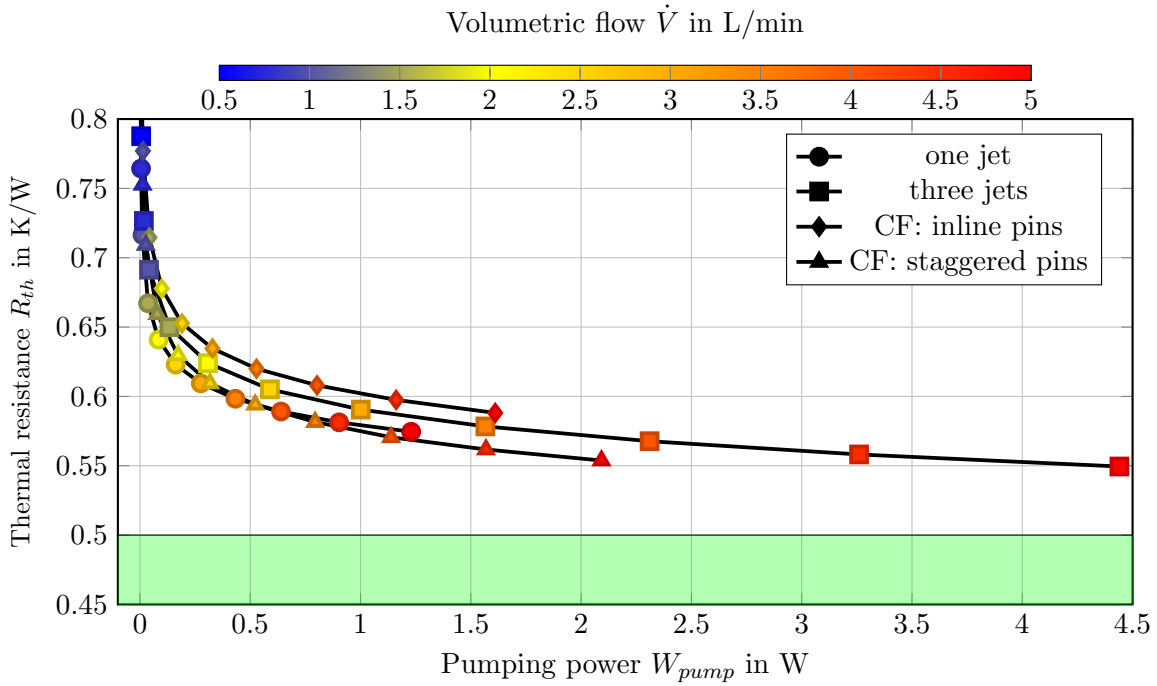
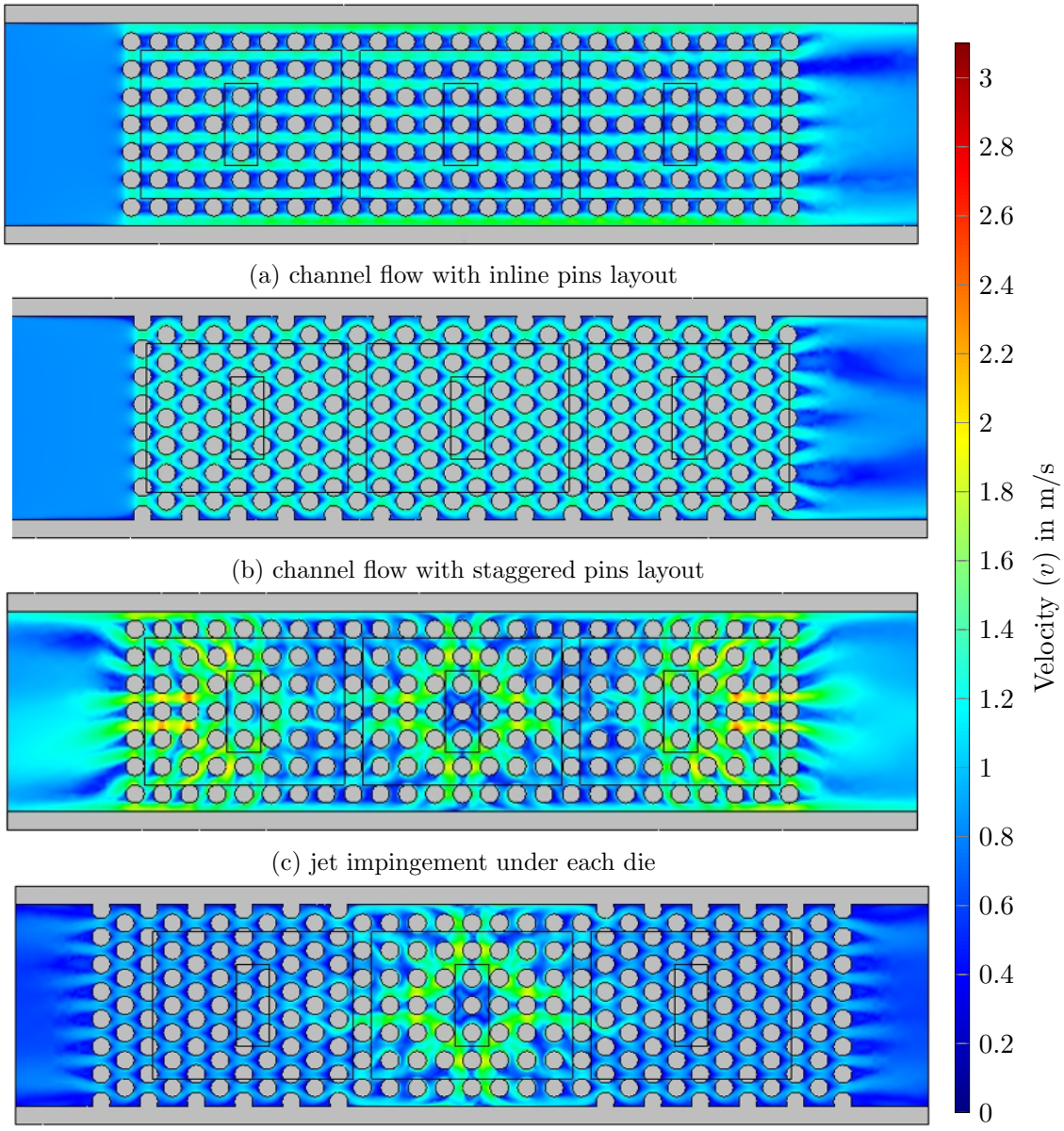


Figure 6.10: Thermal resistance for the four different pin layouts (CFD simulation).

resistance in the channel, which also leads to higher thermal resistance. Performance improves when moving to staggered pins, because of the larger pin density and the longer path followed by the coolant from the inlet to the outlet. The cooler with three jets provides a low thermal resistance but with a very high pumping power due to the three-fold higher flow rate. Finally, a good thermal performance with low pumping power is achieved by the cooler with one jet. However, none of the coolers achieves the target performance of 0.5 K/W thermal resistance.

The velocity distribution near the upper wall for the four design at 3 L/min is shown in figure 6.11. For channel flow, inline pins allows a straight fluid flow through the pins, with high fluid velocity between the pins and the walls. The design with multi-jets has the highest velocity, mainly because of the larger flow rate. The maximal velocity does not occur directly under the side chips because the liquid coming from the middle jet drags the side inlet liquid with it. To optimize the multi-jets design, the position of the side inlets should be optimized so that the velocity is highest under the side dies.

The corresponding temperature distribution at the top side of the module with the same 3 L/min flow rate is shown in figure 6.12. Because of high velocity and longer fluidic path, channel flow with staggered pins and multi-jets designs show the lowest temperature in the system. The single-jet cooler with mixed pin layout offers a more uniform temperature distribution across the three dies compared to the other designs. The temperature variation between the warmest and coolest dies across all four designs



(a) channel flow with inline pins layout

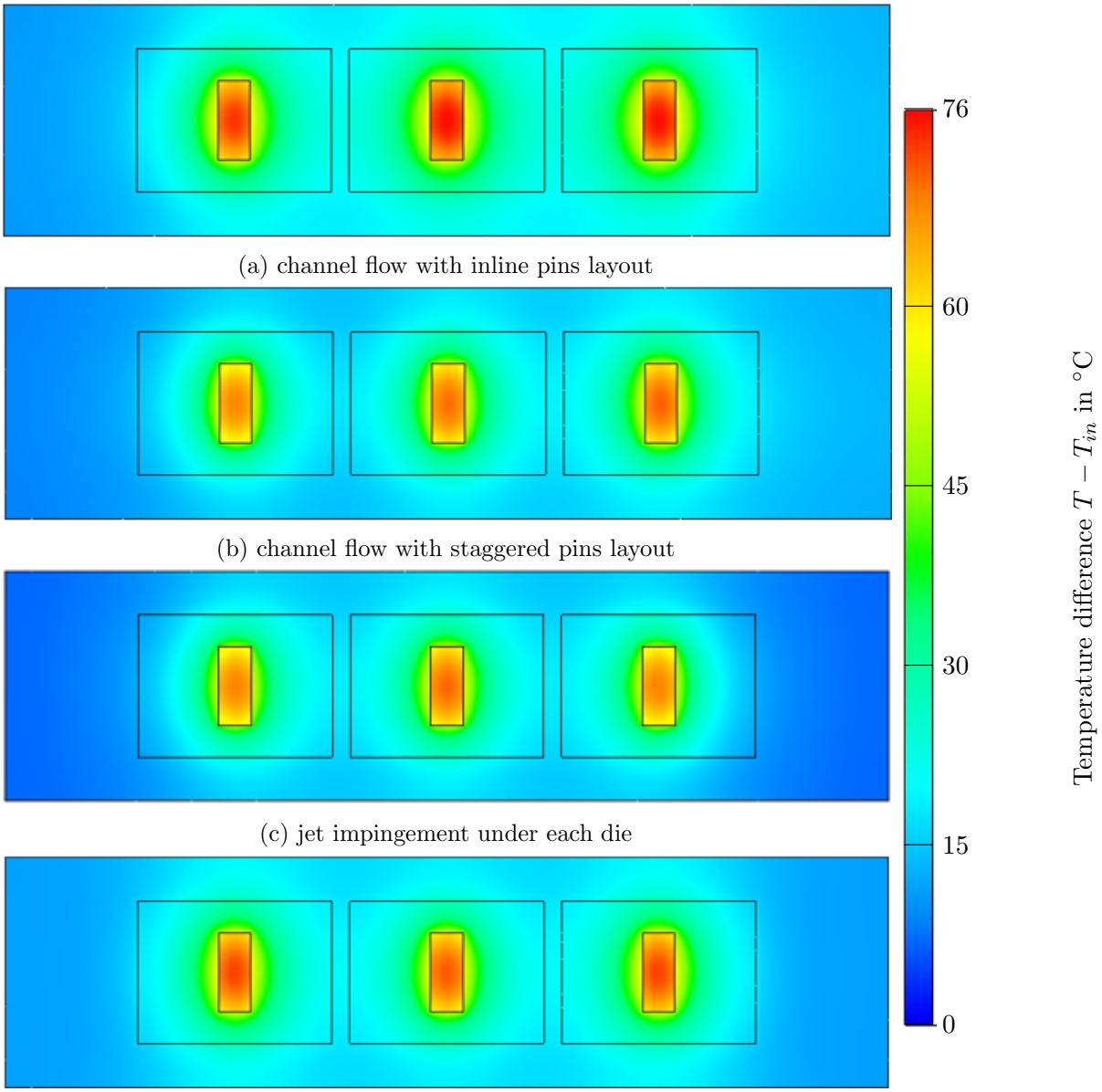
(b) channel flow with staggered pins layout

(c) jet impingement under each die

(d) combination between jet impingement and channel flow, with mixed pins layout

Figure 6.11: Velocity distribution at 1 mm distance from the upper wall, at 3 L/min (CFD, Novec 7500)

at a flow rate of 1 L/min is as follows: For channelflow with inline pins, it's 8 °C; in the case of channelflow with staggered pins, it's 7.5 °C; the design featuring three jets shows a difference of 3 °C; and the design with a single jet exhibits a temperature delta of 2.5 °C. A key issue with the 3-jet design is that to achieve a homogeneous temperature distribution for the all three dies, jets should have different diameter and different flow rates. Additionally, a manifold should be designed to route the fluid to the three jets while



(a) channel flow with inline pins layout

(b) channel flow with staggered pins layout

(c) jet impingement under each die

(d) one jet under the middle die with mixed pin layout

Figure 6.12: Temperature distribution at the top of the module for the different pin layout configurations at 3 L/min (CFD, Novec 7500)

causing a low pressure drop.

Figure 6.13 shows the maximum thermal resistance of the dies (i.e. the thermal resistance calculated for the hottest die on a cooler) over the coefficient of performance ($COP = \frac{P_{losstotal}}{W_{pump}}$). Compared with the data in Figure 6.10, the single-jet cooler exhibit indisputably better performance thanks to its low pumping power at high flow rate. This is why, this combination of one jet impingement over inline pins and channel flow with

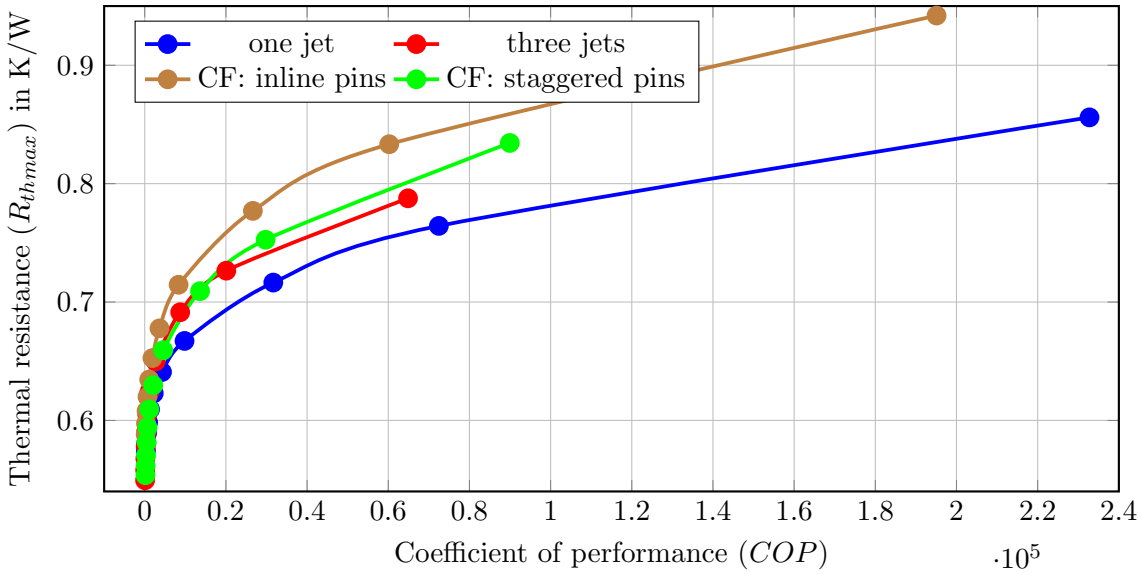


Figure 6.13: maximum thermal resistance for the four cooling principles over coefficient of performance (CFD, Novec 7500)

Table 6.3: The examined parameters on the cooling performance

Parameter	value
Flow rate ($\dot{V}$)	0.5 L/min to 5 L/min
Pin pattern	Symmetric/Asymmetric
Pins type	cylindrical/conic pins
Copper thickness t_{Cu}	0.3 mm to 3 mm
Cooling fluid	Water/Novec 7500

staggered pins is considered in the rest of this work.

6.2.3 Full-cooler optimization

As already mentioned, an AlN cooler manages not just three SiC MOSFETs (as considered in the previous section): there are also three snubbers. All these parts should be cooled. Therefore, the geometry considered here covers the entire $100 \times 50\,\mathrm{mm}^2$ cooler. However, the snubbers generate a much lower heat density ($44.76\,\mathrm{W/cm}^2$ than the SiC elements ($367\,\mathrm{W/cm}^2$), and they can operate at a higher temperature (155 °C). Therefore, cooling performance under the snubbers is much less critical than it is under the dies, and coarser pin structures can be used for easier manufacturing.

Various design parameters are investigated using CFD simulations. They are summarized in Table 6.3, and detailed in the following sections.

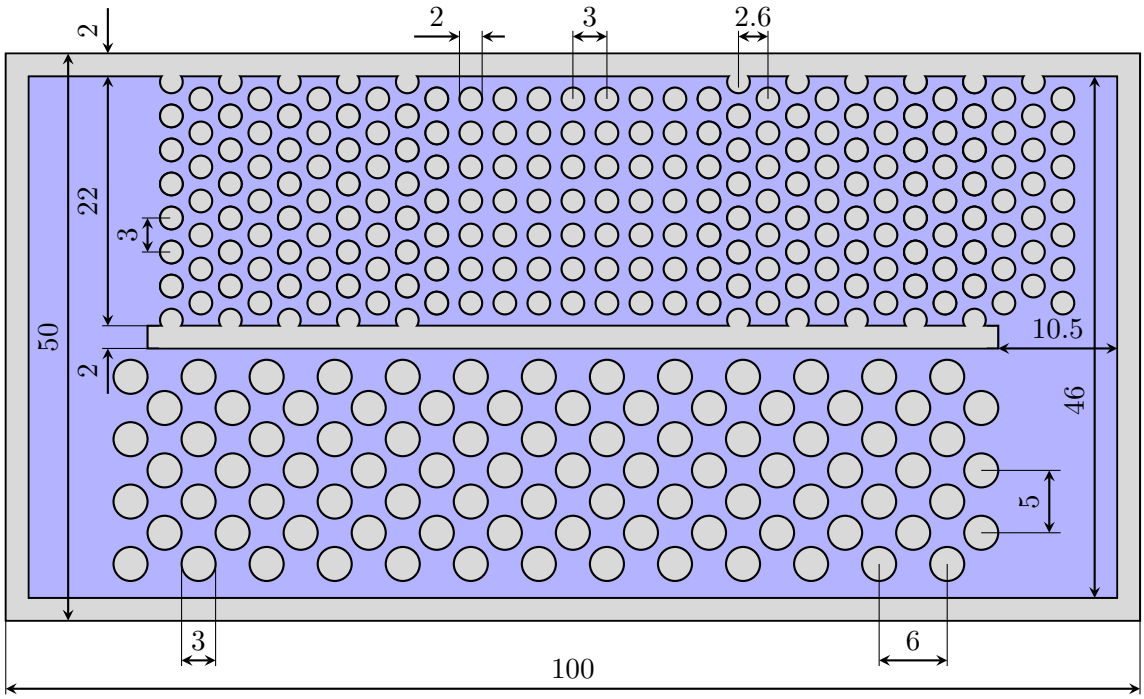


Figure 6.14: A cross-section in the middle of the channel under the chips, showing the design and parameters of the pins

Asymmetry of the coolers

The top view of the system and a cross section are shown in figures 6.4 and 6.5. Because of the various design constraints described earlier, there is an asymmetry in the location of the dies (they are offset to the right of the cooler). This means that while it is split between two channel flow sections, the path of the fluid cannot be fully symmetric after the jet impingement section. This can be seen in Figure 6.14, which shows the internal layout of the cooler. The upper part corresponds to the dies, and is similar to the "single jet with mixed pin patterns" discussed previously. A 2 mm wide and 75 mm long wall is placed in the center of the cooler to guide the fluid to the lower part, which cools the snubbers with 3 mm, staggered pins, and towards the outlet. In the drawing from Figure 6.14, there are more staggered pins in the channel flow section under the right die than under the section under the left die, to compensate for the die offset and the shorter inlet-outlet path. The corresponding velocity distribution in the middle of the channel at 3 L/min is shown in figure 6.15.

To illustrate the beneficial effect of the asymmetric pin distribution, Figure 6.16 shows the minimum and maximum thermal resistance of the SiC chips for a symmetrical pin pattern (same number of pins for the left and right channel sections) and asymmetrical pin pattern shown in Figure 6.14. It can be seen that the asymmetrical pattern (plain

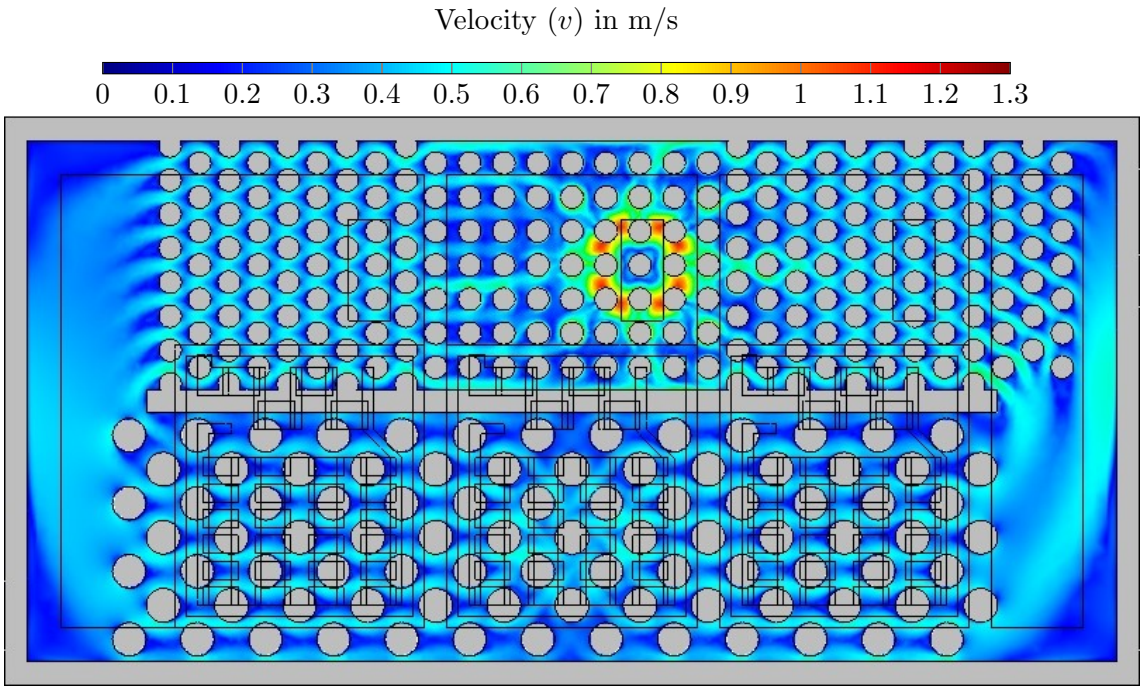


Figure 6.15: Velocity distribution in the middle of the channel at 3 L/min

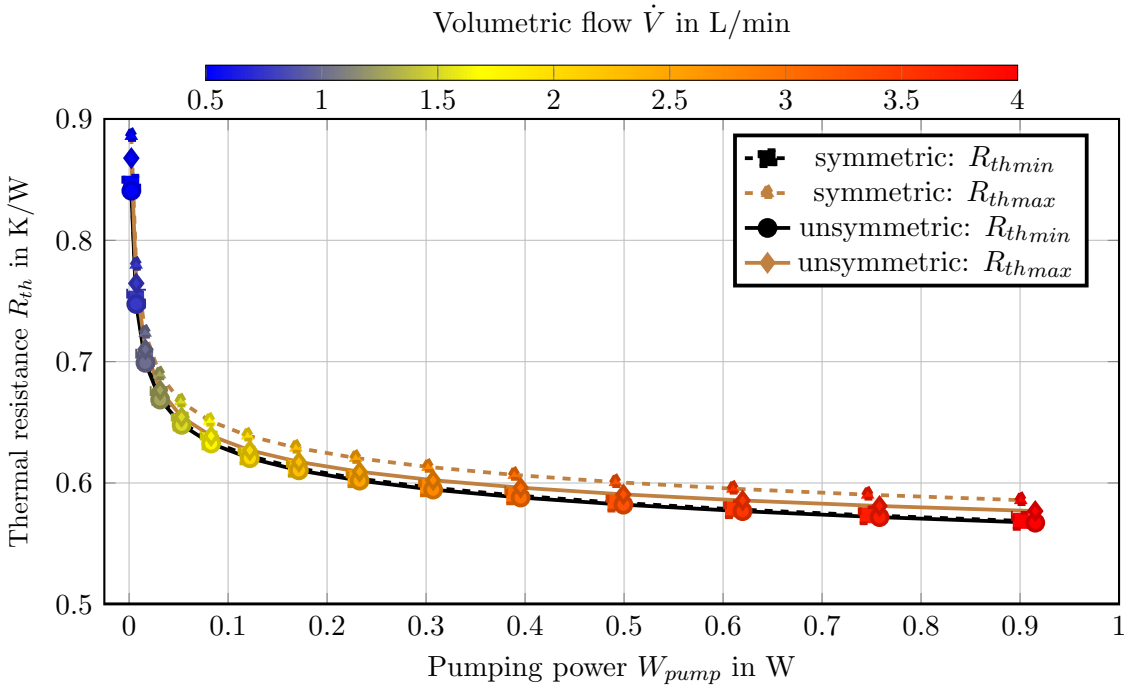


Figure 6.16: Minimum and maximum thermal resistance of the dies with symmetrical and unsymmetrical pins distribution as a function of pumping power (CFD, Novec 7500).

lines) result in a more uniform cooling, with less difference between the R_{th} of the best and worst-cooled dies.

Effect of the copper thickness

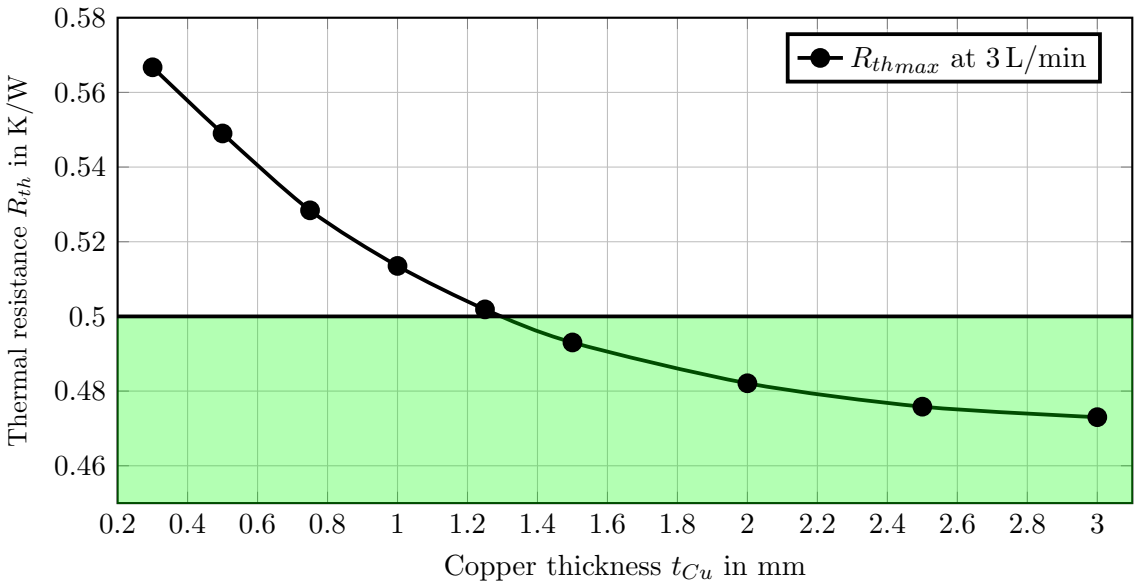


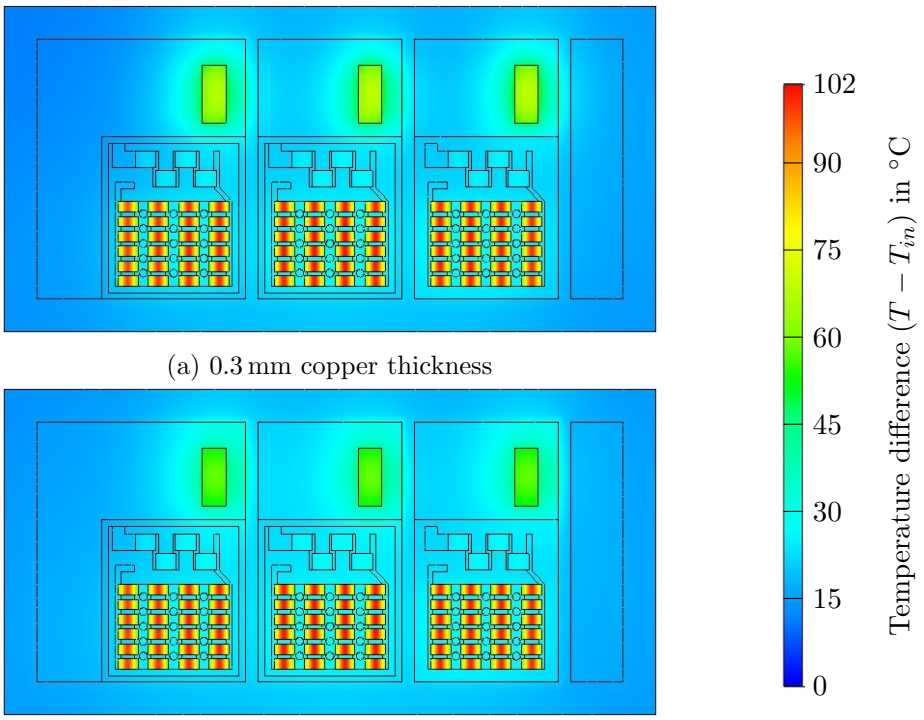
Figure 6.17: Maximum thermal resistance as a function of the copper thickness at 3 L/min (CFD, Novec 7500)

.

As can be seen from the previous simulations, a thermal resistance of 0.5 K/W could not yet be achieved. The heat dissipation to the cooler can be improved further by increasing the copper thickness on the AlN cooler. Due to copper's very high thermal conductivity, thicker copper allows the dissipated heat to spread over a larger surface area on the AlN, thus reaching more pins.

The maximum thermal resistance of the SiC dies as a function of copper thickness is plotted in figure 6.17. As expected, better thermal resistance is be achieved with thicker copper. The desired green area is achieved for thicknesses greater than 0.5 mm. Above 2 mm, R_{th} improves only slightly, as any improvement in lateral conduction is compensated by the longer vertical path through the copper. Figure 6.18 compares the temperature distribution on the top of the module for 0.3 mm and 2 mm copper. With thicker copper, SiC die's temperature is reduced as less heat flows directly to the AlN under the dies while more heat ($\dot{Q}$) flows through the copper to the side areas. The temperature gradient (∇T) is lower around the dies because of higher dissipation surface ($A_{dissipation}$) of the copper:

$$\dot{Q} = A \times \lambda \times \nabla T \quad \Longrightarrow \quad \nabla T \propto \frac{1}{A_{dissipation}}.$$



(a) 0.3 mm copper thickness

(b) 2 mm copper thickness

Figure 6.18: Temperature distribution at the top of the module for 0.3 and 2 mm copper thickness, at 3 L/min (CFD, Novec 7500)

The temperature gradient is inversely proportional to the dissipation area for a constant heat flow and material's thermal conductivity (λ). The temperature of the snubbers (resistors) is not affected by thicker copper because given their size and the fact that they are aligned with the copper edges, there is little room for heat to spread.

Due to practical manufacturing constraints, the copper spreader thickness is restricted to 1 mm. Consequently, the upcoming study will prioritize coolers with copper thickness ranging from 0.3 mm to 1 mm.

Influence of the snubber

The snubber is part of the module. The heat dissipated by the snubbers affects the junction temperature of the SiC dies, as they share common copper pads and AlN heatsink. This influence is shown in figure 6.19. If the snubbers don't produce heat, the cooling performance of the AlN cooler is significantly better, and a thermal resistance below the required specification of $R_{th} < 0.5\,\mathrm{K/W}$ can be achieved even with a copper thickness $t_{Cu} = 0.5\,\mathrm{mm}$.

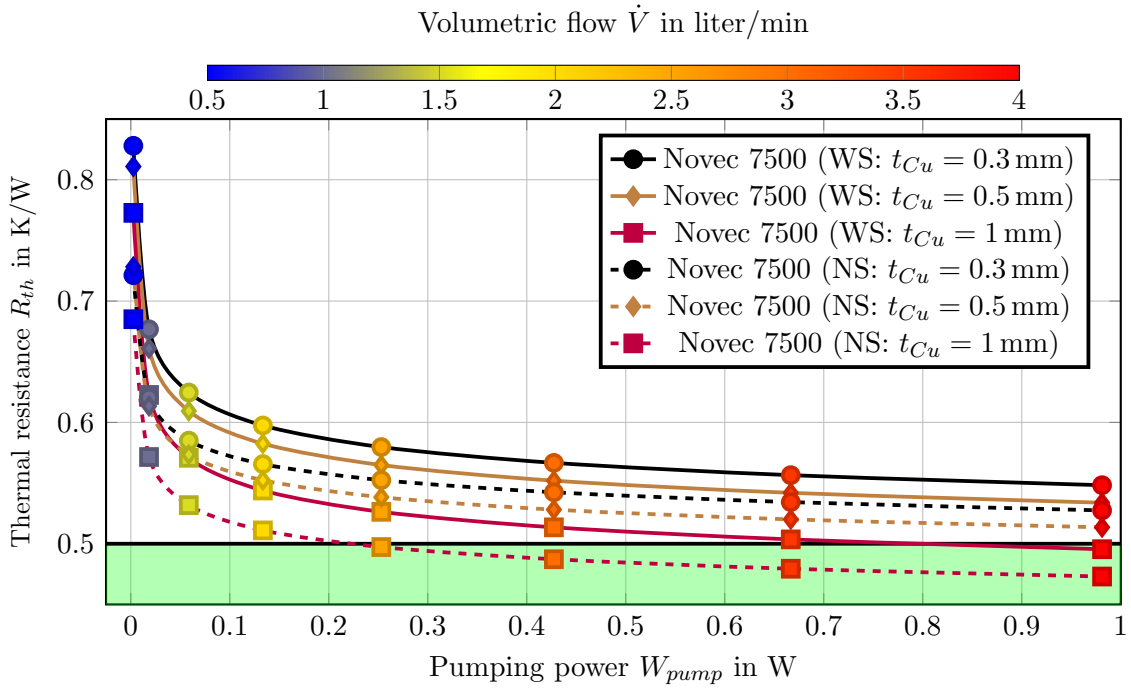


Figure 6.19: Thermal resistance as a function of pumping power for various copper thicknesses and with (WS) or Without (NS) heat generation from the snubbers (CFD, Novec 7500)

Novec 7500 vs. water

Although Novec 7500 is chosen as a coolant for its dielectric properties, it is interesting to compare its performances with those of water since water is the most commonly used coolant (Figure 6.20). Water shows a significantly better cooling performance because of its higher thermal conductivity and capacity. Due to its lower viscosity, water also requires lower pumping power. The desired thermal resistance of less than 0.5 K/W can thus be achieved with a very low water flow rate and pump power (< 10 mW).

Figure 6.21 shows the temperature distribution at the top of the module at 0.5 L/min and 3 L/min for Novec 7500 and water. For Novec 7500 at 0.5 L/min could be seen that the heat flows through the entire module and the temperature rises well above the liquid inlet temperature due to the low heat capacity of the dielectric liquid. At the same flow rate as water, the temperature of the areas away from the heat sources is close to the liquid temperature. The temperature rise of water is much lower than that of Novec 7500 ($c_p \propto \dot{V}\rho_{fluid}$), especially at low flow rates $\dot{V}$. With Novec 7500 at 3 L/min the temperature of AlN decreases significantly. However, the areas away from the chips and snubbers are still hotter than the liquid temperature. On the other hand, water keeps the areas away from the heat sources very close to the inlet temperature ($T_{in} = 40\,°C$).

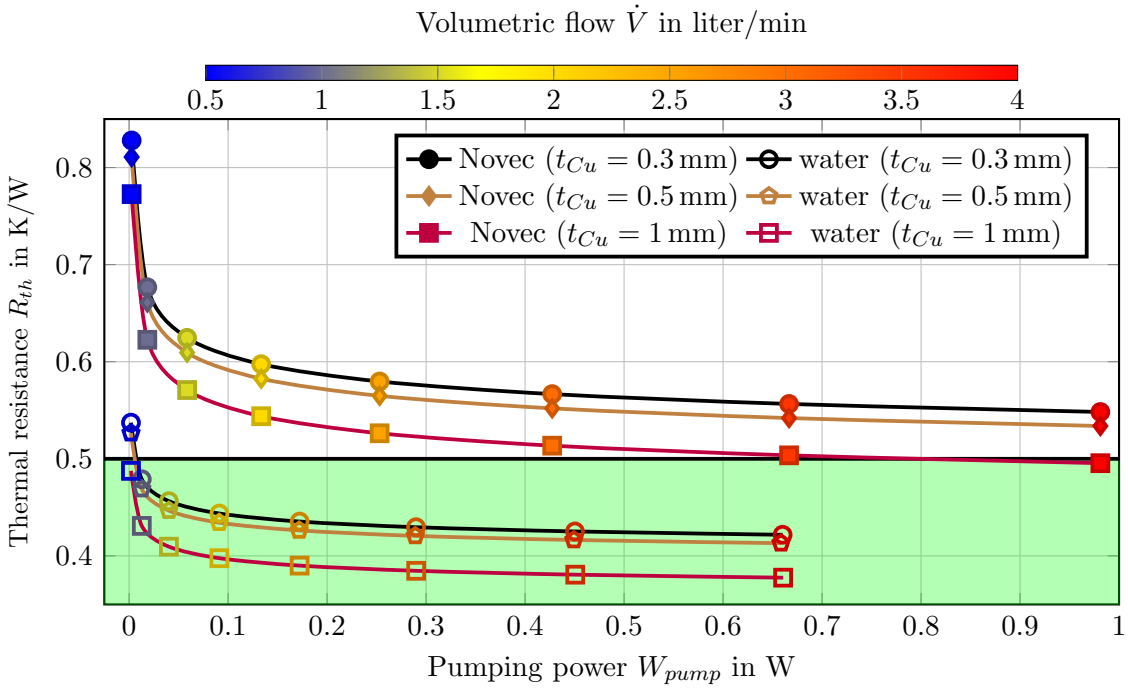
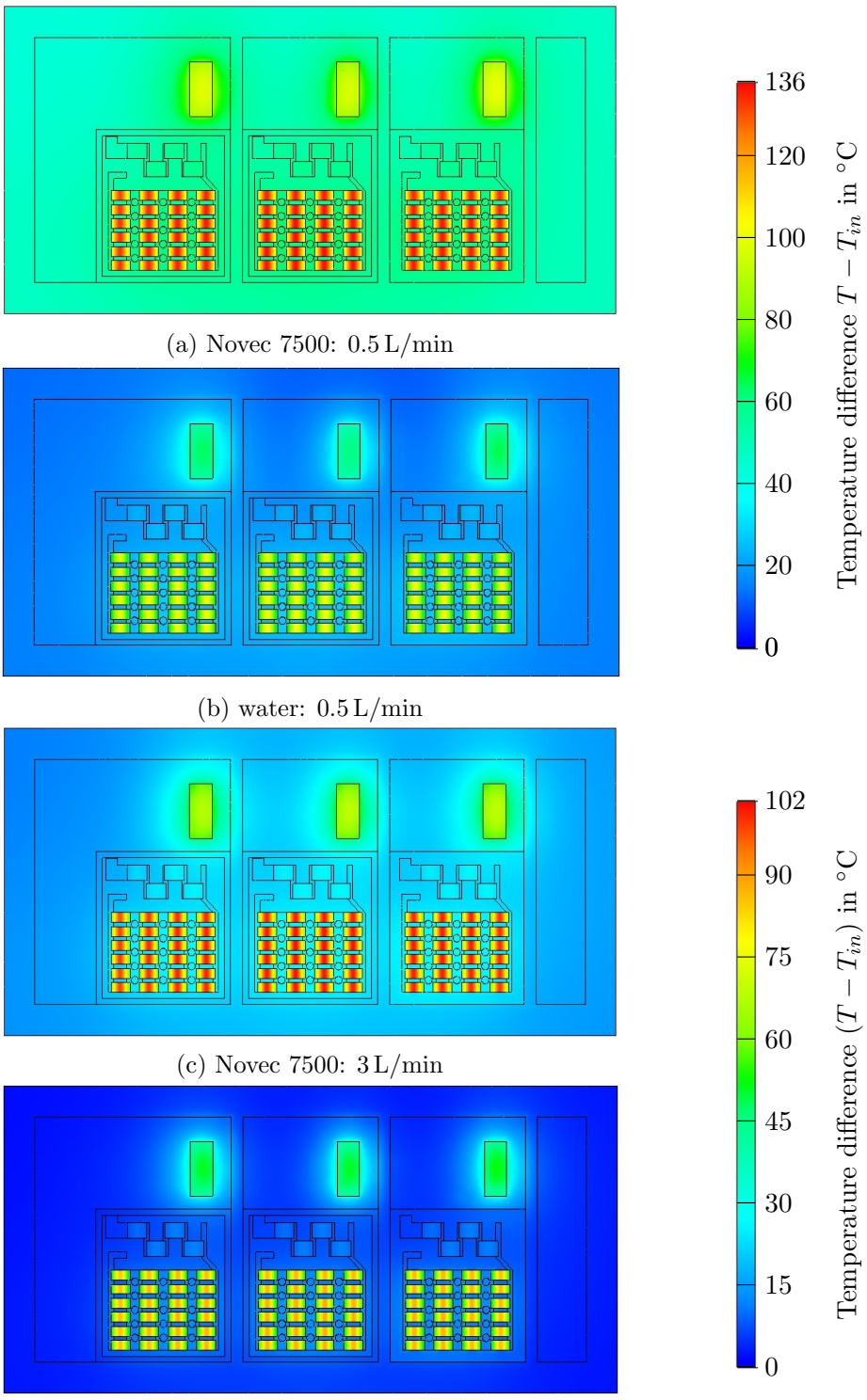


Figure 6.20: The maximum thermal resistance as a function of pumping power with Novec 7500 and water as coolants for different copper thicknesses.

In addition to the junction temperature of the dies, the maximum temperature of the snubbers using both coolants is compared. Figure 6.22 shows the temperature difference between the maximum temperature of the snubbers and the inlet temperature of the liquids (40 °C) over the flow rates for water and Novec 7500. With low flow rates of Novec 7500, the temperature of the snubbers remains above the required temperature (150 °C), at about 180 °C at 0.5 L/min. With increasing volume flow, the temperature drops quickly and reaches a temperature difference to the inlet temperature of about 102 °C with a volume flow of 4 L/min. With water, the temperature is already below the critical temperature by 144 °C at low flow rates and drops to approximately 128 °C at a flow rate of 4 L/min.

6.2.4 Conclusion on the cooler optimization

We investigated four different configurations for a three-die cooler and identified the one with a single jet inlet featuring inline pins at the jet impingement location and staggered pins elsewhere as the most effective cooler due to its excellent cooling performance at low pumping power requirements. Numerical optimization of the cooler revealed that increasing the thickness of the copper spreader, up to 3 mm, enhances cooling performance. However, manufacturing constraints restrict the copper thickness to a maximum of 1 mm.



(a) Novec 7500: 0.5 L/min

(b) water: 0.5 L/min

(c) Novec 7500: 3 L/min

(d) water: 3 L/min

Figure 6.21: Temperature distribution at the top of the module with Novec 7500 and water as coolants at 0.5 L/min and 3 L/min

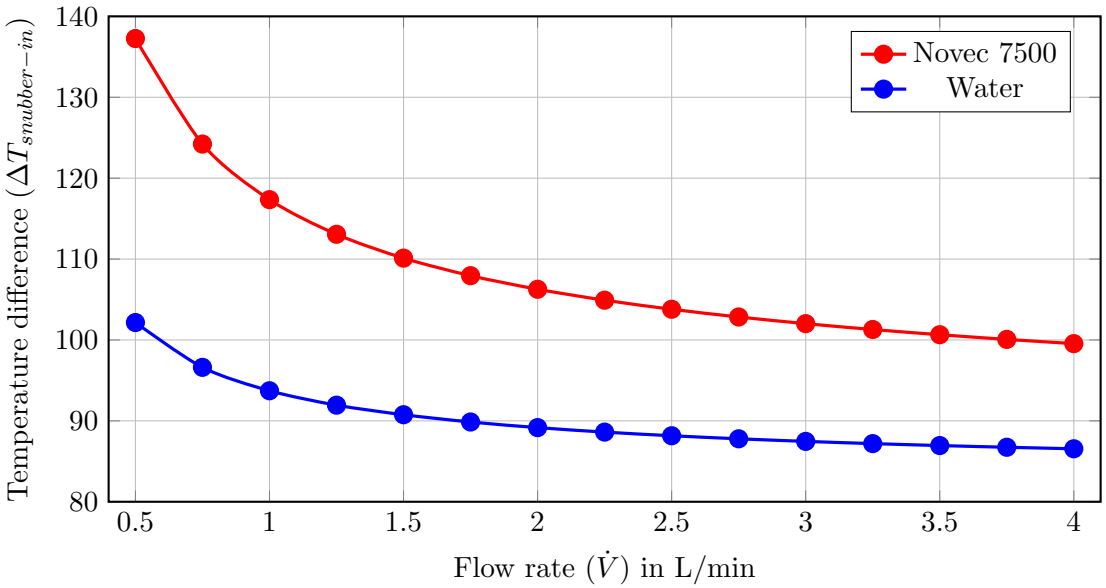


Figure 6.22: Numerical calculated maximum temperature of the snubbers over the flow rate for water and Novec 7500 as coolants

Consequently, prototypes with copper thickness not exceeding 1 mm are manufactured.

Within the cooling channel, conical pin structures are employed because they outperform cylindrical pins. The pins beneath the SiC dies have an upper diameter of 2.7 mm and a bottom diameter of 1.8 mm, while the pins beneath the snubbers feature an upper diameter of 3 mm and a bottom diameter of 2.3 mm.

6.3 Experimental study

This section presents the manufacturing procedure of the 3-die module, discusses the test setup and shows the test results compared with the numerical simulations.

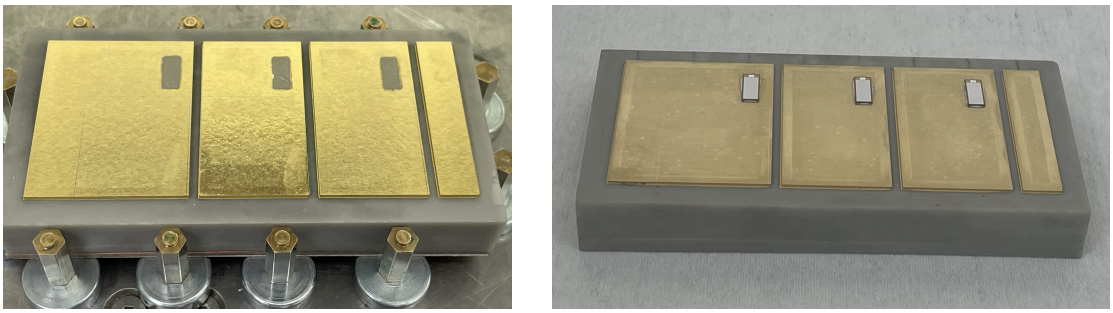
6.3.1 Preparation of the test vehicles

Three test vehicles configurations are produced for experimental tests. All three share identical AlN cooler geometry, and differ by the thickness of their copper metallizations. The manufacturing process for the coolers and their metallizations is identical to that of the single-die coolers.

Once the metallized coolers are produced by Ceramtec, they are marked with a laser to define the location of the various components (dies, snubbers, connecting PCB). The assembly process is then as follows

1. Sintering the 3 SiC dies on the cooler. The thin (100 nm) gold finish tarnishes when

exposed to high temperatures and pressure. Therefore, the dies are sintered simultaneously to reduce exposure time at high temperature. Pressure-assisted sintering of multiple dies is not available in our lab. Therefore, pressureless sintering is used instead: a stencil is used to print 70 µm nanosilver paste (NJ-One nano-join) onto the dies positions. After that, the coolers are put into an oven at 100 °C for twelve minutes to let the paste dry. Then, the dies were placed on the silver paste with 1.5 N force. Then the cooler is placed into an oven applying a heating profile (see [150]) for the sintering process to complete. Figure 6.23 shows the paste and the sintered dies onto the cooler.



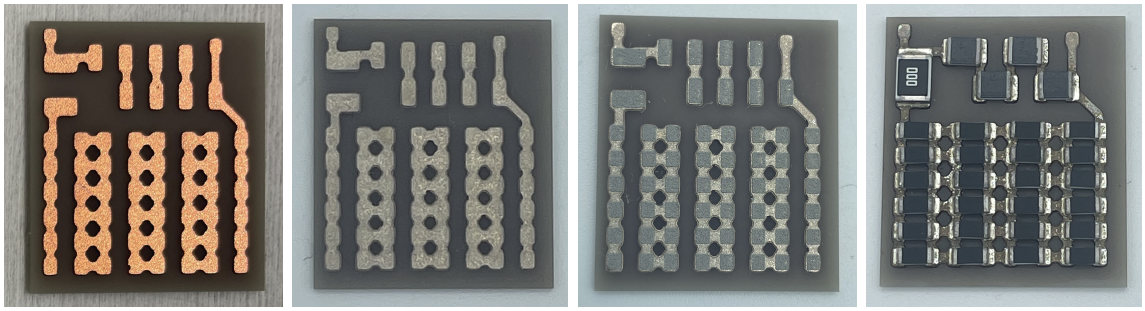
(a) nanosilver paste on the metallized cooler (b) The sintered die on the cooler

Figure 6.23: pressureless sintering of the SiC-MOSFETs onto the metallized cooler

2. Manufacturing of the snubber: An AlN DBC mastercard (Rogers-Curamik) is patterned and singulated to form the snubber substrates (Figure 6.24a). Figure 6.24b shows the DBC top surface which is plated silver using an immersion process. A stencil is used to apply 100 µm thick solder paste to the pads of the SMD components (Figure 6.24c). Then, the SMD components are placed with 1.5 N force. Finally, the populated substrates are re-flowed to solder the components. Figure 6.25d shows a manufactured snubber.

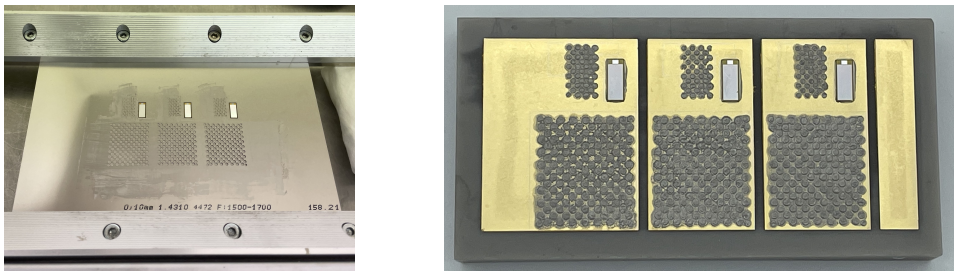
3. Manufacturing of the PCBs: to connect the dies to the outside world interconnect PCBs are needed. These PCBs have been designed to have dimensions of 8 mm × 13 mm and a thickness of 1 mm. These are featured with 35 µm copper layer with Electroless Nickel Immersion Gold (ENIG) surface finish. The PCBs are manufactured by a commercial supplier.

4. Adhesive bonding of the snubbers and PCBs to the cooler: A silver conductive epoxy (RS 186-3616) is used for the attachment the parts because it offers a reasonably good heat conductivity and is easy to process (no need for high temperature reflow). The adhesive is applied by stencil printing using 100 µm stainless steel stencil. The stencil pattern (holes) is designed to cover 50 % of the snubbers and PCBs surfaces,

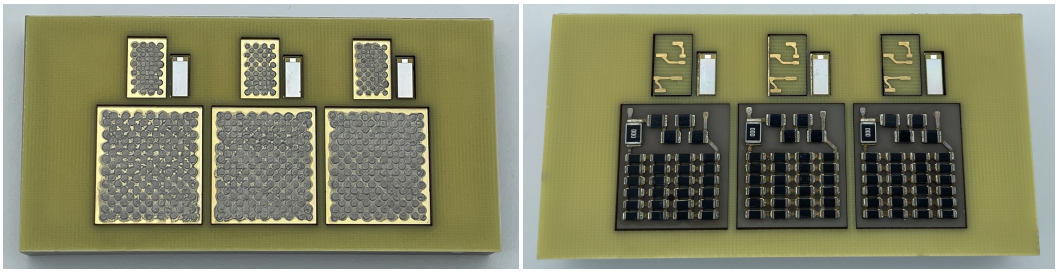


(a) top side DBC (b) copper silvering (c) solder paste on DBC (d) fabricated snubber

Figure 6.24: Snubber manufacturing



(a) Applying the glue on the stencil (b) Glue distribution on copper sheets



(c) placing the alignment jig (d) place the components to their positions

Figure 6.25: Attaching the DBC and PCB on the metallized cooler

in order to end up with 50 µm adhesive thickness. A custom alignment jig is used to place the components to the right positions. A weight (ca. 1 kg) is applied on the snubbers and PCB to ensure proper attachment. The curing time of the epoxy is 36 hours at ambient temperature. Figure 6.25 summarize the attachment process of the components.

5. Thick wire bonding: A thick wire bonder (TPT HB30) is used to connect the dies pads to the PCBs and to the other dies. Table 6.4 summarizes the parameters for the 300 µm-thick wire bonding. Figure 6.26 shows the 3-dies Module with the wire bonding. Note that for the thermal tests, the snubbers are not wirebonded to the power module as shown in Figure 6.3. Instead, they are left unconnected so they can be driven by a separate power supply.

Table 6.4: process parameters of the wire bonder

Bond	length	height	US power	US time	force
Source-Drain	8000	6000	1500	750	1200
Source-PCB	5000	4000	1500	750	1200
Gate-PCB	5000	4000	1500	750	1200
Drain-PCB	3000	4000	1500	750	1200

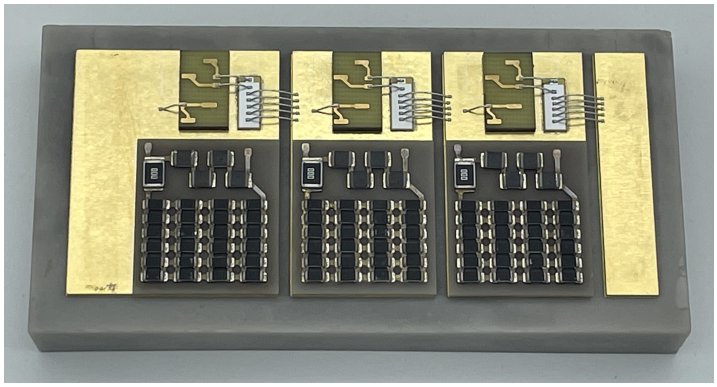


Figure 6.26: Thick Al wire bonding

6. Soldering the pin headers and the terminals to the module: the cooler is placed on a hot plate at 190 °C and SMD pin headers (2.54 mm) are soldered to the PCBs and to the snubbers using a solder iron and some solder paste (CHIPQUIK, SMD291SNL50T3) using a dispensing unit. The same process is repeated to solder the power terminals to the high side (DC+) and low side (DC-) of the module.

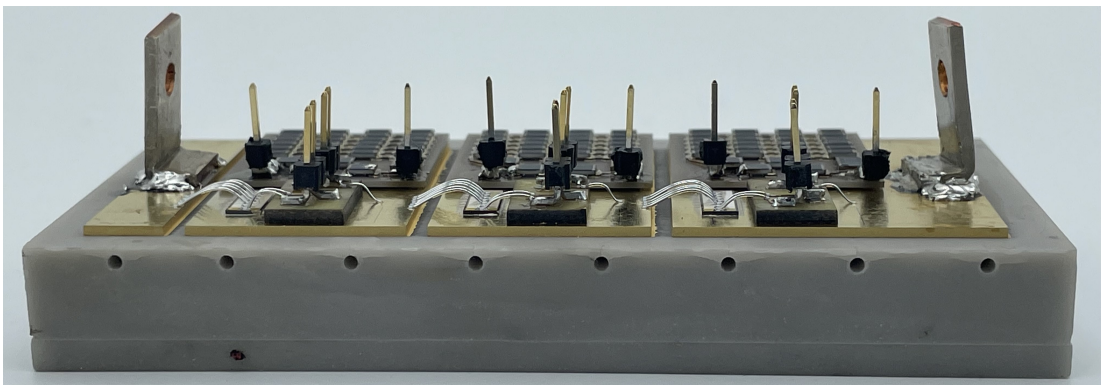
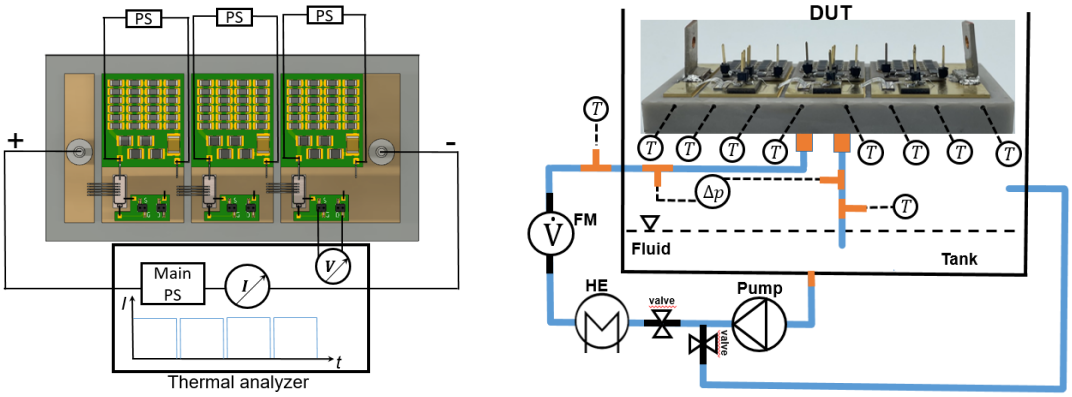


Figure 6.27: The completed 3-dies module with the all components on the cooler. The 8 holes on the front are prepared to host thermocouples.



(a) Electrical connections of the snubbers and SiC dies to the thermal analyzer

(b) schematic cooling loop and all sensors used for the measurement

Figure 6.28: Fluidic loop and electrical connections of the module

6.3.2 Test setup

The test setup is the same as used for the simple single-die module in chapter 5, with a few differences:

- the pressure difference is measured with reference to the outlet pressure, and not to the ambient pressure
- The snubbers are powered using external power supplies, and their temperature is measured using thermography only (the thermal analyzer cannot monitor the snubbers). 20 V (54 W power loss) are applied across each snubber.
- All three MOSFETs are powered at the same time by the thermal analyzer. However, the measurement is done separately because the thermal analyzer can measure one die temperature only (that of the top MOSFET of the series assembly, because of grounding issues).

Figure 6.3.2 describes the schematic test setup. Beside the temperature of the SiC chips, the AlN temperature in the AlN is measured, see figure 6.28a.

6.3.3 R_{th} characterisation

Because the thermal analyzer can only monitor the thermal resistance of the top die (the one which has the source connected to DC-, for grounding reasons), another approach must be used for the other two dies. Two methods can be used to measure the thermal resistance of all chips: thermal Imaging camera and an extension of the V_{SD} method (both are detailed in section 4.3.1).

The extended V_{SD} method relies on the measurement of the temperature in the AlN under each die using thermocouples. The junction temperature of the top die is measured by the thermal analyzer (V_{SD} method). Then, considering the temperature difference between the junction temperature of each chip and the AlN temperature underneath it is constant yields:

$$\Delta T_{j-AlN} = T_{j1} - T_{AlN1} = const = T_{j2} - T_{AlN2} = T_{j3} - T_{AlN3} \tag{6.3}$$

(note that die numbering and position correspond to that described in Figure 6.4: "top die": D1, "middle die": D2, "bottom die": D3.) Therefore, the thermal resistance of every die can be estimated using Equation 4.20

6.3.4 Experimental results

At first, the measured temperature difference between the outlet and inlet is compared with an analytical calculation. This provides a validation of the test setup (showing that all devices work and produce the desired heat). From the first law of thermodynamics, the temperature difference can be estimated by dividing the total generated heat $\dot{Q}$ by the product of heat capacity c_p and mass flow $\dot{m}$:

$$\Delta T_{out-in} = \frac{\dot{Q}}{\dot{m} c_p} = \frac{P_{loss}}{\rho_f \dot{V} c_p} \tag{6.4}$$

The heat flow of the test vehicle is equivalent to the total power losses of all parts on the AlN cooler. Every SiC die produces power losses of 120 W and every snubber 54 W, which gives total power losses of 522 W. The mass flow is a product of the flow rate $\dot{V}$ and the coolant density ρ_f. The test is carried out with water and then with Novec 7500. Figure 6.29 shows the measured outlet-inlet temperature difference for different flow rates compared with the analytical solution.

The measured data and the analytical calculations are in good agreement. After checking the functionality of the test setup, the tests are carried out with water and Novec 7500. The experimental results for both fluids are discussed separately in the following sections. In the end, both sets of results are compared.

Water

Figure 6.30a show a cooler during test: its surface is painted black to control its emissivity; thermocouples are inserted in cooler's wall, Electrical wires are connected for power and sensing. An IR thermography, captured from the same point-of-view for a cooler with 300 µm-thick copper at 3 L/min water flow is shown in figure 6.30b (using the software Fluke SmartView [151]). The top green rectangles correspond to the three SiC dies, while

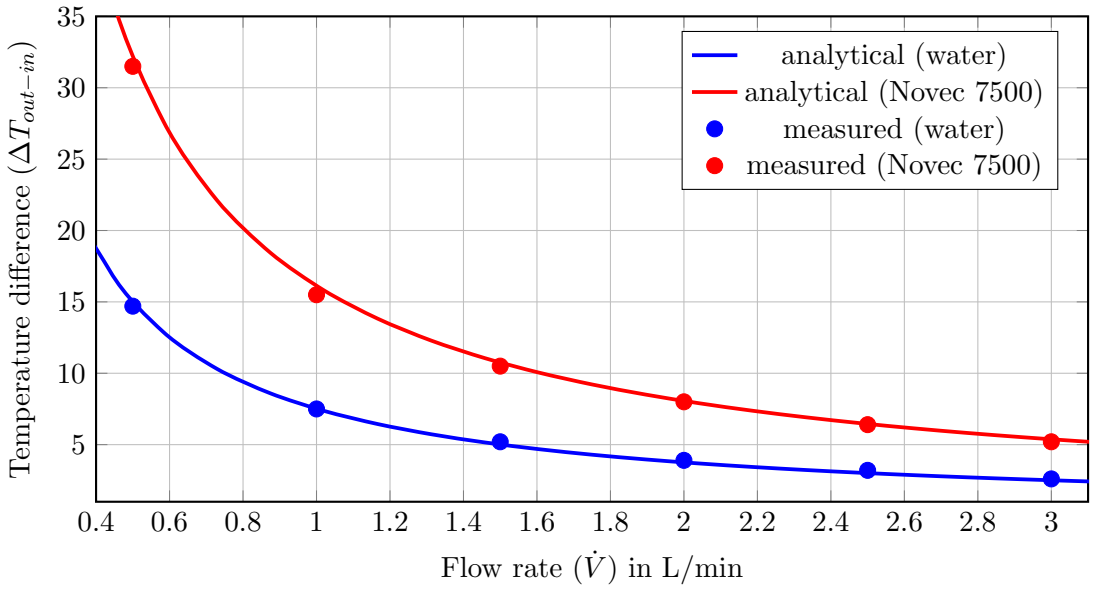
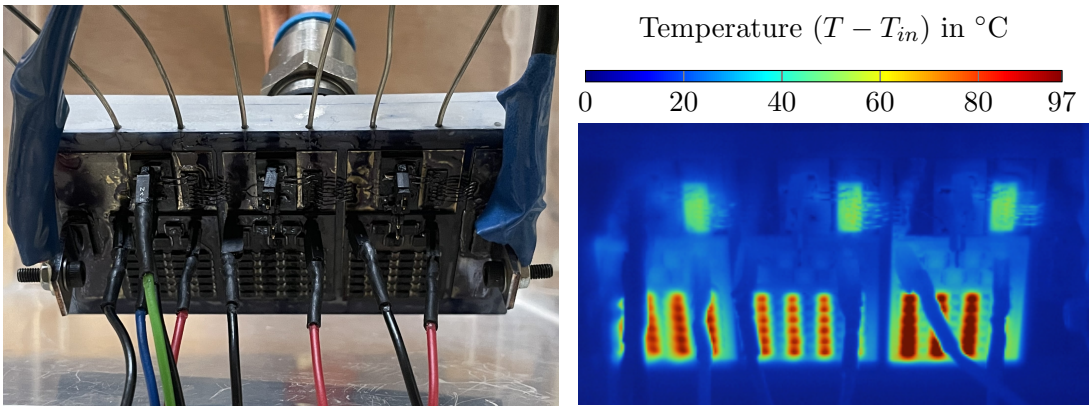


Figure 6.29: Comparison between analytical and measured temperature change in the fluid between inlet and outlet, for a 522 W power dissipation.

the resistors of the snubbers are dark red, because of their high temperature. Some of the resistors are hidden behind the electrical wiring, which appears blue. The thermal resistance is calculated with Equation 4.20 using the chips' junction temperature reading from the thermography.



(a) painted DUT (b) IR thermography

Figure 6.30: The painted DUT and the IR thermography of the top side of the module at 3 L/min (water)

Another way to calculate the thermal resistance is by measuring the temperature under each SiC chip with a thermocouple and using equation 4.20 (extended V_{SD}). Here, eight thermocouples are inserted in the top AlN wall, three of them directly under the three SiC

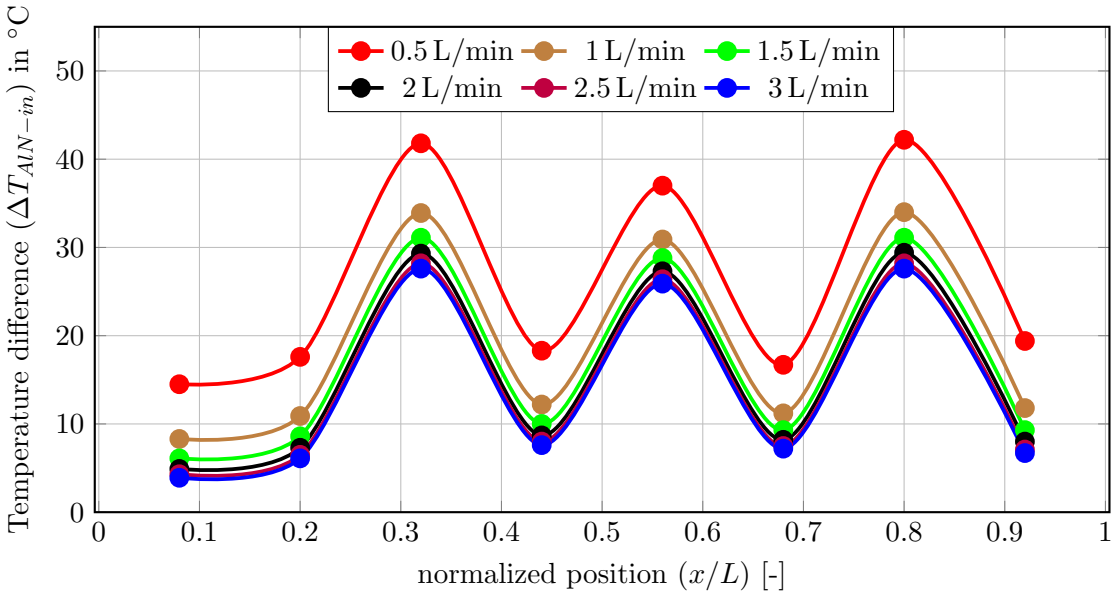


Figure 6.31: Temperature distribution in the AlN for coolers with different 300 µm-thick copper for different flow rates (experiment, water)

dies. The measured temperature in the AlN cooler with 300 µm copper for different flow rates is shown in figure 6.31. These measurement points are connected with a smooth line to facilitate reading. As can be expected, higher flow rates deliver lower temperature on the AlN due to higher fluid velocities and turbulence in the cooler. Higher flow rates also result in more homogeneous temperature distribution between the chips.

The V_{SD} method is used to measure the junction temperature of the top SiC chip. The measured junction temperature of the chip and the inlet and AlN temperatures under the top chip for different water flow rates are shown in table 6.5. The junction temperature at each flow rate is subtracted from the measured AlN temperature and then the average temperature is calculated. The measurements indicate that the temperature difference between the junction and AlN temperature remains consistently similar across various flow rates. The test results reveal that the temperature difference remains constant, irrespective of whether the snubbers are powered or not. The average difference between the

Table 6.5: Temperature measurement of the top die and in the AlN

$\dot{V}$ [L/min]	0.5	1.0	1.5	2.0	2.5	3.0	Average temperature
T_{in} [°C]	22.6	22.9	23.0	23.0	23.0	23.1	
T_{j_1} [°C]	88	80.6	78	76	74.8	74.2	
T_{AlN1} [°C]	64.8	56.9	54.1	52.3	51.2	50.6	
T_{j-in_1} [°C]	65.4	57.7	55	53	51.8	51.1	
$\Delta T_{(j-AlN)_1}$ [°C]	23.20	23.70	23.9	23.7	23.6	23.6	23.62

junction and AlN temperature ΔT_{j-AlN} is applied in equation 4.20 to calculate the thermal resistance $R_{thV_{DS}}$ of other dies (D2 and D3) using the second method (extended V_{DS}). In parallel, the junction temperature IRT_j of each die is measured using the IR camera. Applying equation 4.20, the corresponding thermal resistance R_{thIR} can be calculated.

The measured thermal resistances of both methods for the three SiC chips on the module with 300 µm copper metallization are shown in figure 6.32. Both methods give similar results. Because of its simplicity (direct thermocouple measurements, no image post-processing required), the extended V_{DS} method is used in the remaining of the study. IR thermography are only used for more qualitative comparisons.

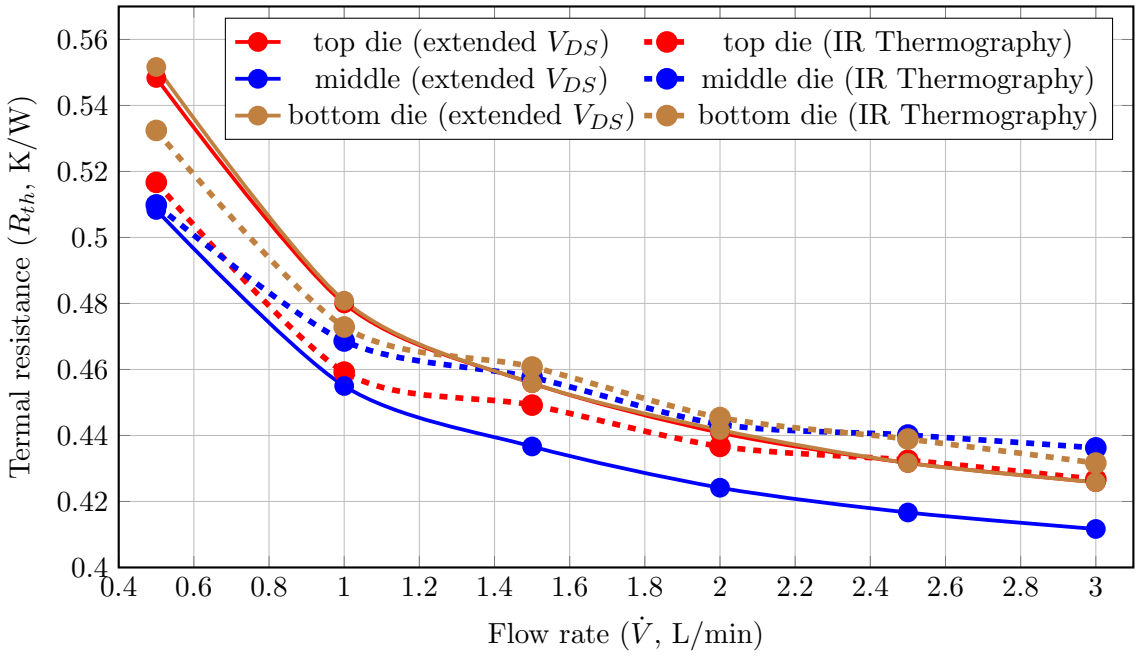


Figure 6.32: Thermal resistance of the three dies with two different methods: 1) IR camera, 2) extended V_{SD} method (experiment, water)

Beside the SiC elements, the snubbers also dissipate heat (54 W each). The influence of the snubbers on the die's temperature for the 300 µm metallized cooler is shown in Figure 6.33. The temperature in the AlN is measured first with operational SiC dies ($P_{lossSiC} = 120$ W each) and energized snubbers ($P_{lossS} = 54$ W each). The temperature is measured again while the snubbers are turned off ($P_{lossS} = 0$ W) to see the snubber's effect on the dies temperature. The AlN temperature on the dies side decreases slightly when the snubbers are turned off leading to a better cooling of the SiC chips.

In addition to the AlN cooler with 300 µm-thick copper, two other coolers with 500 µm and 1000 µm-thick metallizations are characterized. The temperature distribution in AlN over the flow rate for the three different copper thicknesses is shown in figure 6.34. Thicker copper leads to better cooling and better temperature distribution on the AlN. It is in-

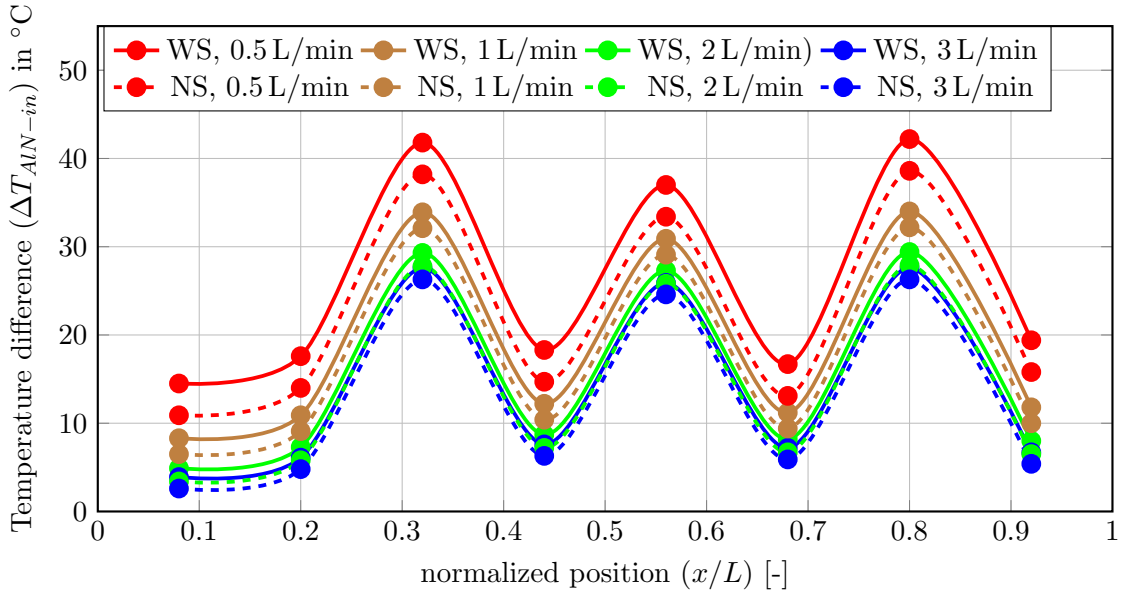


Figure 6.33: Temperature distribution in the AlN with snubber (WS) and without snubbers (NS) for the cooler with 300 µm copper metallization for different flow rates (experiment, water)

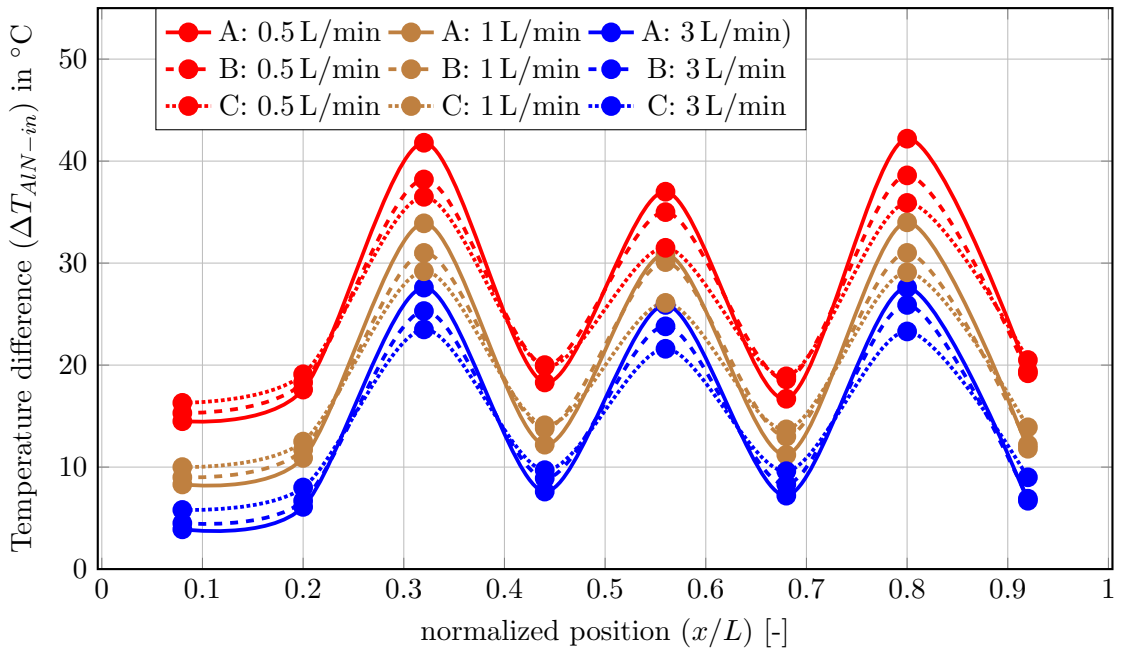


Figure 6.34: Temperature distribution in the AlN for the coolers with 300 µm (A), B=500 µm (B) and 1000 µm (C) copper metallization for different flow rates (experiment, water)

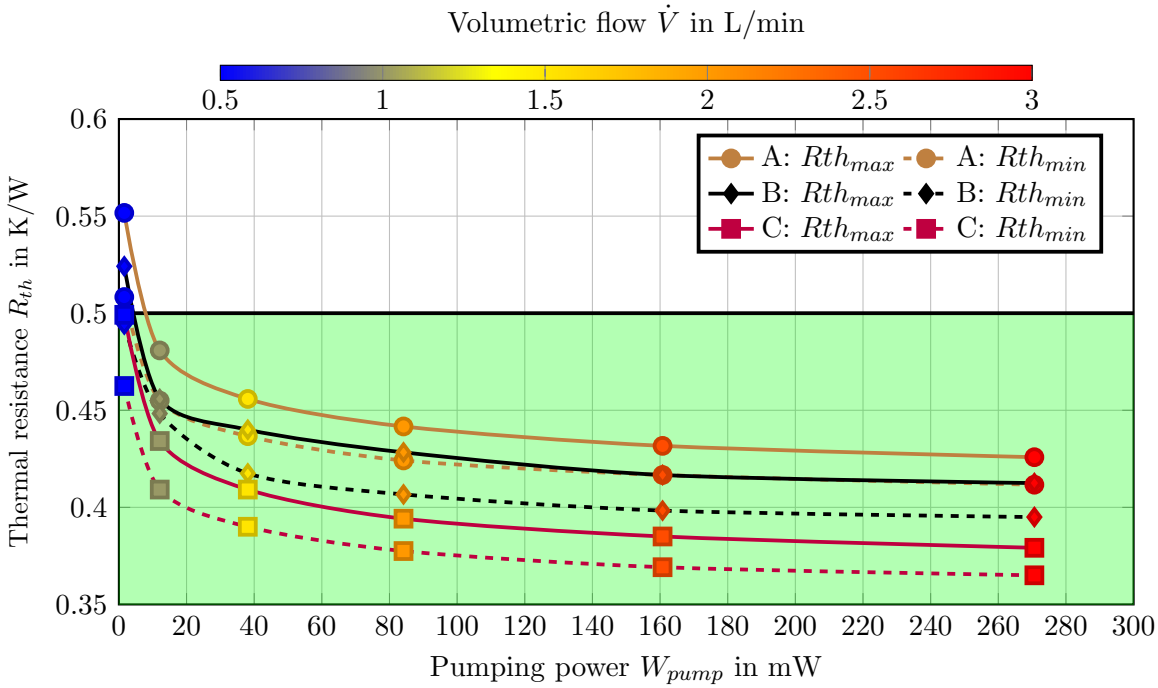


Figure 6.35: Maximum and minimum thermal resistance as a function of pumping power for the AlN coolers with different copper thicknesses (A=300 µm, B=500 µm, C=1000 µm copper) with water as coolant

teresting to note that the measured AlN temperatures away from the chips increase with thicker copper compared with thinner copper. This demonstrates the spreading effect of thick copper.

The corresponding thermal resistances for the three prototypes are shown in figure 6.35 as a function of pumping power. It confirms that the cooler with thicker copper has better cooling performance, with lower R_{th} at a given pump power. The thermal specifications ($R_{the} < 0.5\,\mathrm{K/W}$ and $W_{pump} < 3\,\mathrm{W}$) are easily achieved using water as coolant, regardless of the copper metallization thickness.

Beside the (steady state) thermal resistance, transient thermal impedance (Z_{th}) is an important metric for power electronics cooling. The measurement is performed only for one chip on and the other two chips and the snubbers off. SMD connectors are soldered onto each copper sheet of the submodule to perform the Z_{th} measurement of all dies. Figure 6.36 shows the measured thermal impedances of the three dies at 1 L/min and 3 L/min flow rates. The graph's x-axis represents the pulse duration (heating time) in seconds, while the y-axis represents the transient thermal impedance in Kelvin per watt. At 1 L/min the three curves show a similar behavior with a slightly higher thermal resistance of the top die. The curves reach a steady state after a shorter time when the flow rate is increased to 3 L/min. The three chips have nearly identical thermal impedance curves and the same

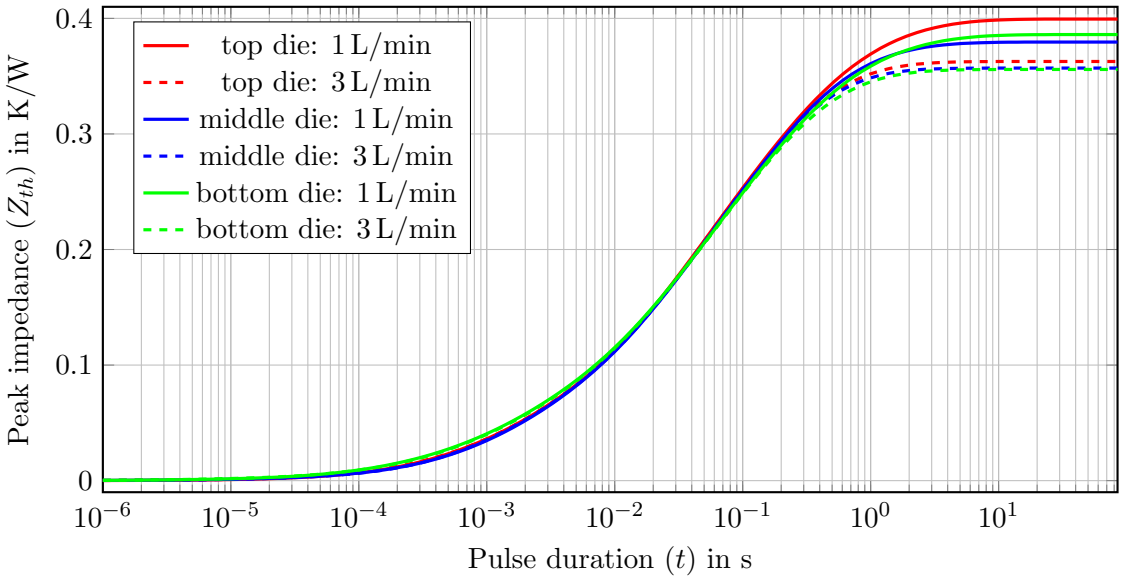


Figure 6.36: Measured thermal impedance (Z_{th}) for the three dies of the cooler with 1 mm copper at 1 L/min and 3 L/min water flow rates with water as coolant

steady-state thermal impedance (thermal resistance). This Z_{th}-measurements confirm the measured thermal resistance values presented earlier and shows that the AlN-cooler offers good cooling performance by achieving a uniform junction temperature across the three chips.

Novec 7500

The same measurement method as used with water test is applied here with Novec 7500. The measured temperatures on the AlN for different flow rates for the first module with 300 µm are shown in figure 6.37. As expected, higher flow rates lead to lower temperature.

At 0.5 L/min, the AlN temperatures under the side dies are very similar, and the middle die has a slightly lower temperature due to the jet. For higher volumetric flows, the temperature distribution is very similar under the three dies. Figure 6.37 show the temperatures with all the components working (snubbers included). The effect of turning the snubbers off is shown in Figure 6.38: at 0.5 L/min, the AlN temperature drops by about 10 °C without the snubbers. By increasing the fluid velocity, the influence of the snubber on the AlN temperature decreases due to better cooling of the components and also because the temperature change in the liquid decreases, as shown in Figure 6.29.

In addition to the AlN cooler with 300 µm copper, coolers with copper thicknesses of 500 µm and 1000 µm are also characterized. The measured AlN temperatures for the three devices are shown in figure 6.39. The temperature decreases significantly when the copper

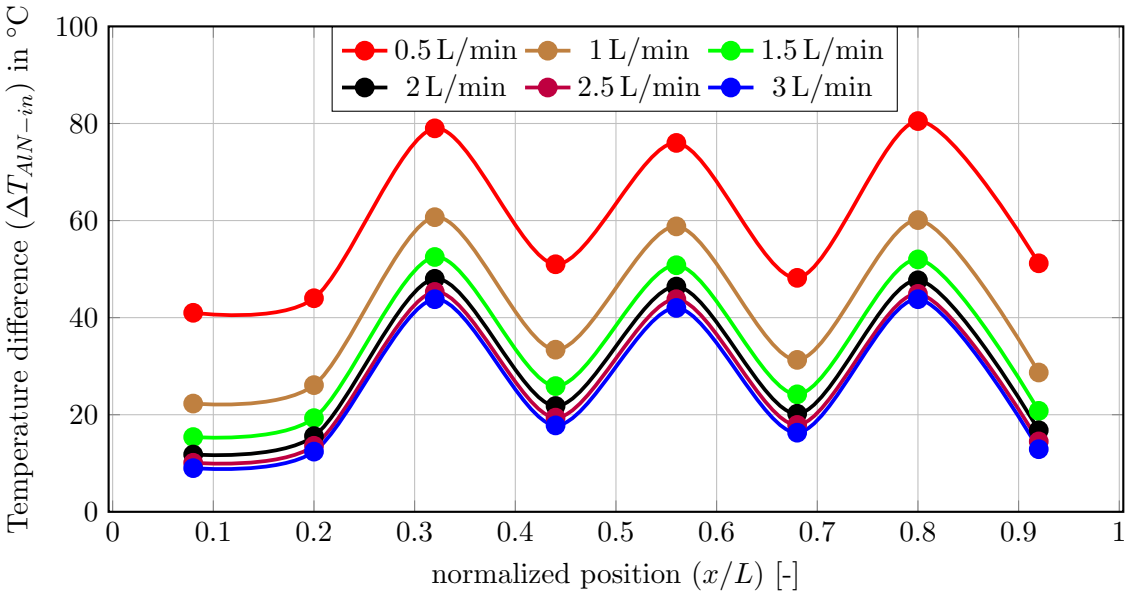


Figure 6.37: Temperature distribution in the AlN for coolers with Novec 7500 and 300 µm-thick copper, for different flow rates (experiment, Novec 7500)

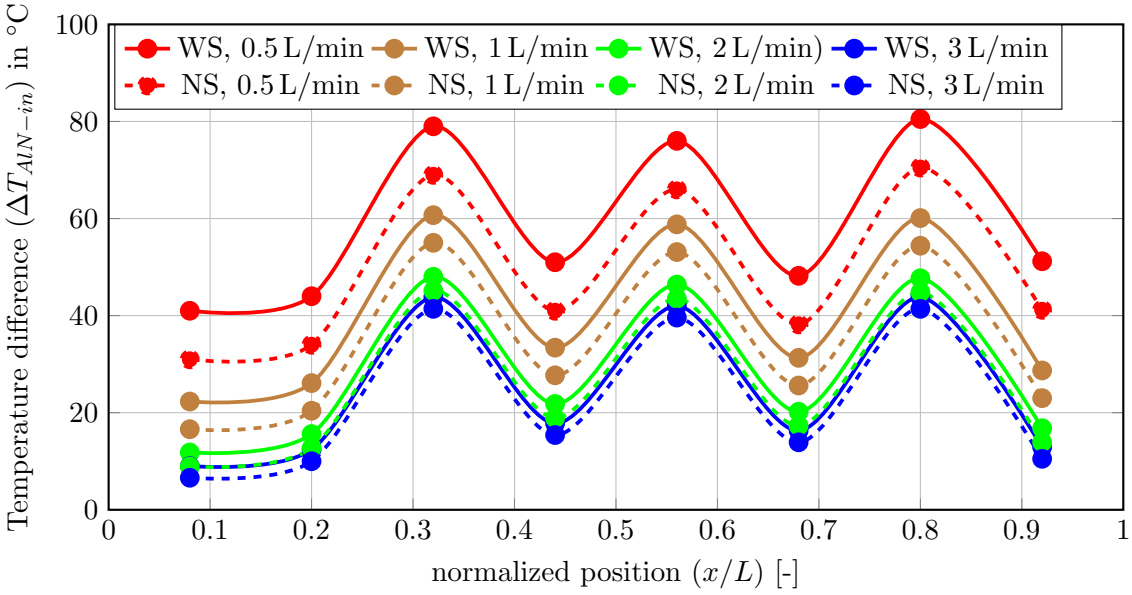


Figure 6.38: Temperature distribution in the AlN with snubber (WS) and without snubbers (NS) for the cooler with 300 µm copper metallization for different flow rates (experiment, Novec 7500)

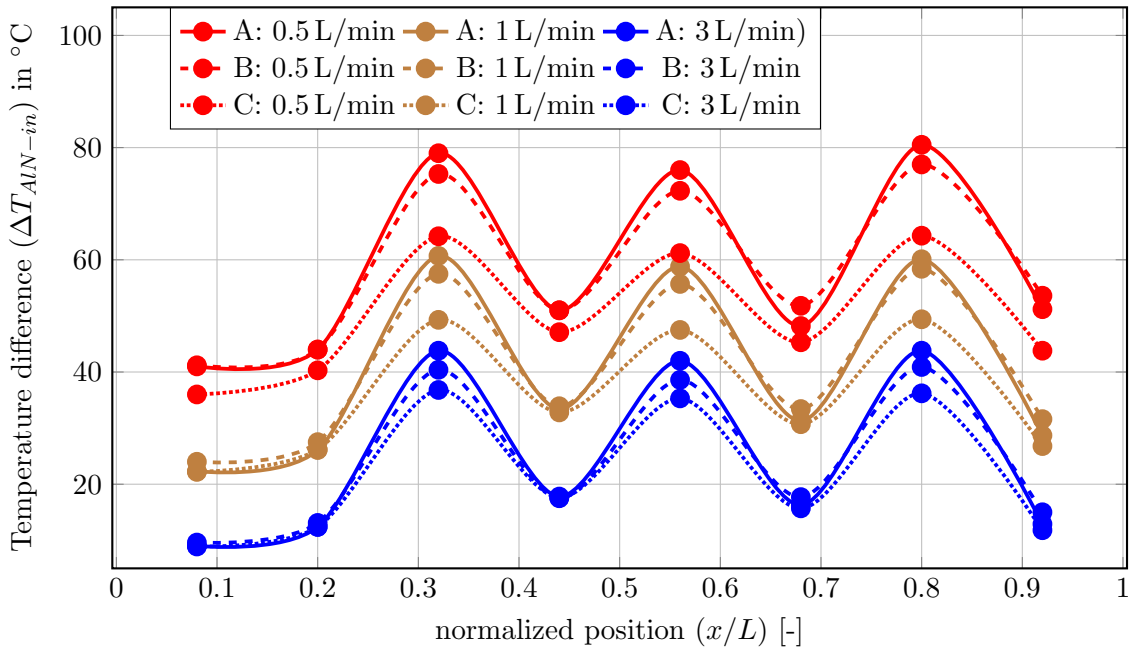


Figure 6.39: Temperature distribution in the AlN for the coolers with 300 µm (A), B=500 µm (B) and 1000 µm (C) copper metallization thickness at different flow rates (experiment, Novec 7500)

thickness is increased to 1000 µm, especially at low liquid flow rates. At higher flow rates, the influence of the copper thickness on the measured temperatures is smaller but still high.

Figure 6.40 shows the minimum $R_{th\,min}$ and maximum $R_{th\,max}$ thermal resistance of the dies versus pump power with Novec 7500 as coolant. The desired thermal resistance ($R_{th} < 0.5\,\mathrm{K/W}$) can only be achieved at a flow rate of at least 2 L/min for 1 mm copper. The heat spreading effect of the copper thickness is fundamental in achieving the target values.

Novec 7500 vs. water

The IR thermographies on the top of the 300 µm Cu cooler at 0.5 L/min and 3 L/min are shown in Figure 6.41 for water and Novec 7500. A poor bonding between the snubber and cooler explains the very high temperatures reached by the right side snubber. In general the snubbers have higher temperature than that of the dies due to limited dissipation heat area under the resistors. However, the temperature limit for the snubber resistors is set at 155 °C (110 °C temperature difference between the inlet and resistor temperature), which is reached here at 3 L/min with Novec 7500 as a coolant.

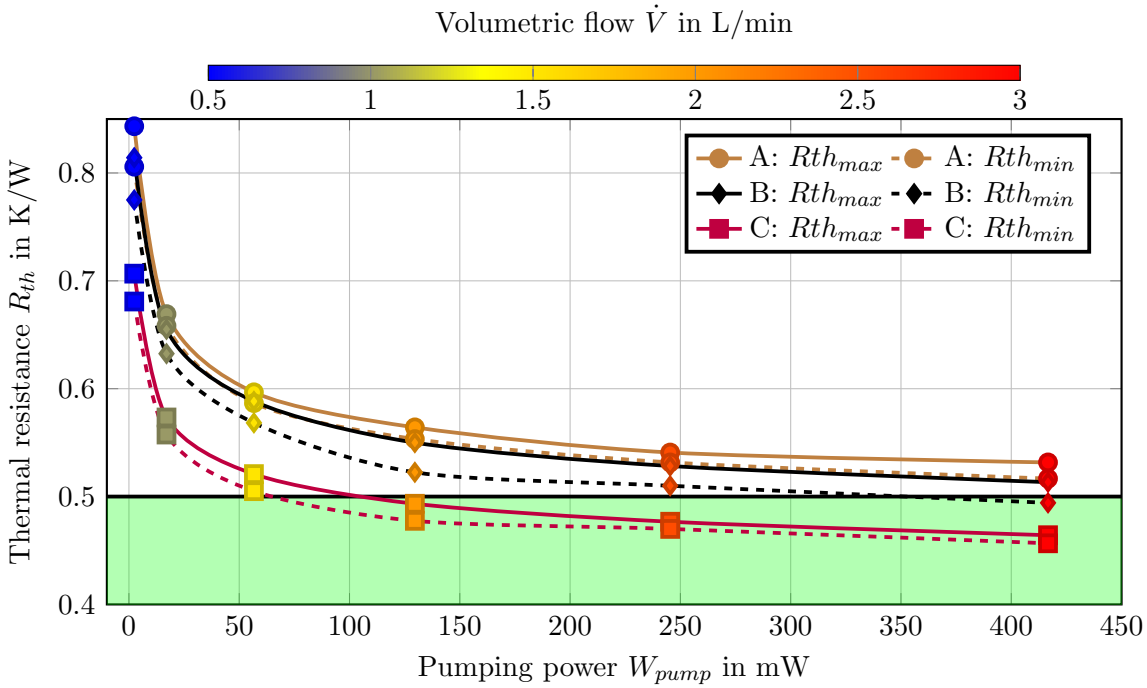


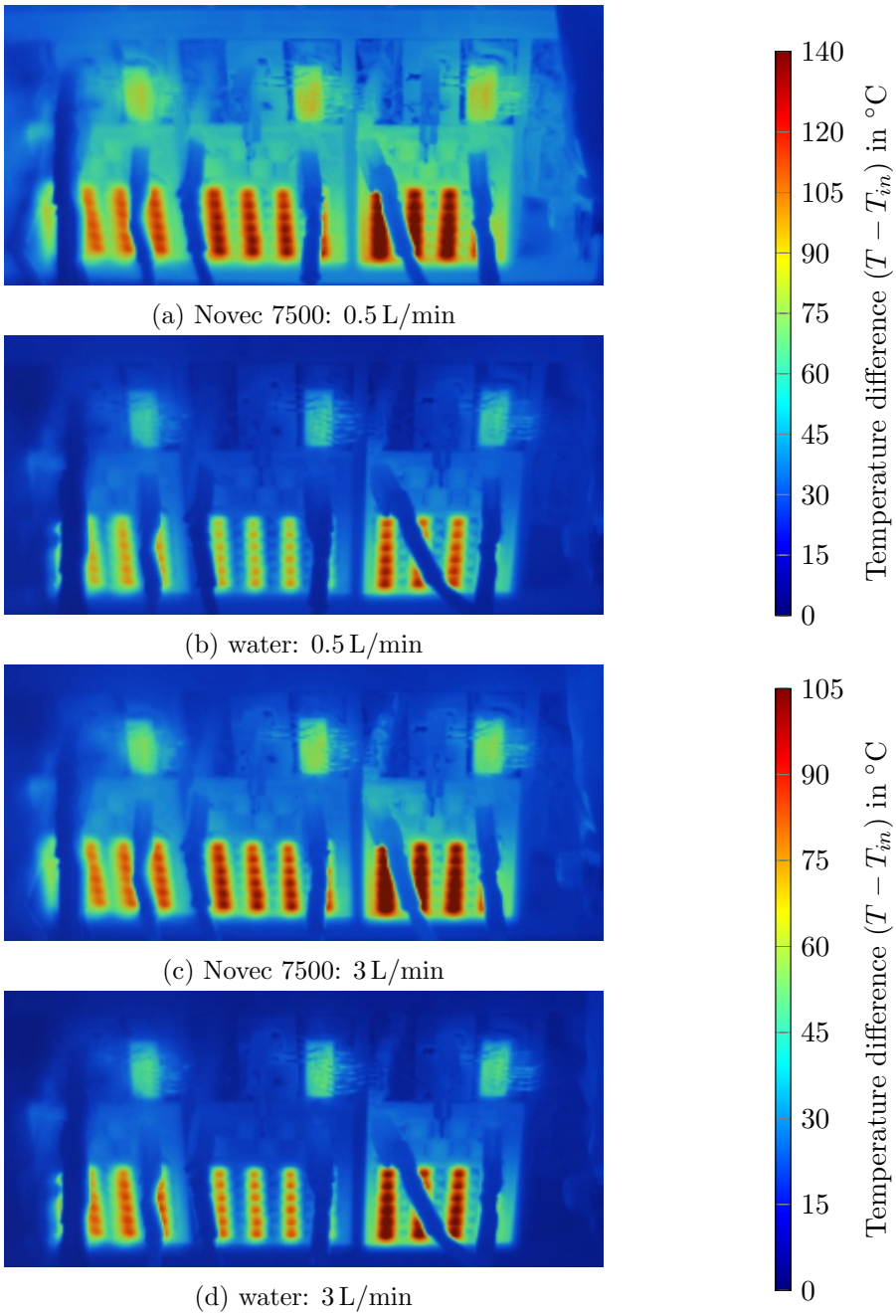
Figure 6.40: Maximum and minimum thermal resistance as a function of pumping power for the AlN coolers with different copper thicknesses (A=300 µm, B=500 µm, C=1000 µm copper) at for different flow rates (experiment, Novec 7500)

6.3.5 Evaluation of the CFD and experimental results

The last step after the measurement is to compare the experimental data with the numerical (CFD) results. The numerical and measured temperatures in the AlN for 3 L/min are shown in Figure 6.42, and show a good agreement. The experimental results are slightly better than the CFD results.

The measured and calculated R_{th} values are shown in Figure 6.43. For water, the results are in very good agreement. For Novec 7500, there is a visible difference between simulation and experiments, which probably denotes that the properties of Novec 7500 are not known with as much accuracy as those of water. However, even for Novec 7500, the measured pumping power is very close to that of the numerical calculation, and proximity between simulated and experimental results is satisfying. It is also worth noting that for Novec 7500 the experimental results are better than the CFD results (lower R_{th} and lower pressure drop).

The temperature distributions (temperature difference with the inlet temperature) on top of the coolers, simulated by CFD or captured with the IR camera at a 3 L/min flow rate of water and Novec 7500 are shown in figure 6.44. Figure 6.44a shows the temperature distribution calculated by CFD for water, with the same color scale as Figure 6.44b, which



(a) Novec 7500: 0.5 L/min

(b) water: 0.5 L/min

(c) Novec 7500: 3 L/min

(d) water: 3 L/min

Figure 6.41: Temperature distribution at the top of the module of 300 µm with Novec 7500 and water as coolants, at 0.5 L/min and 3 L/min

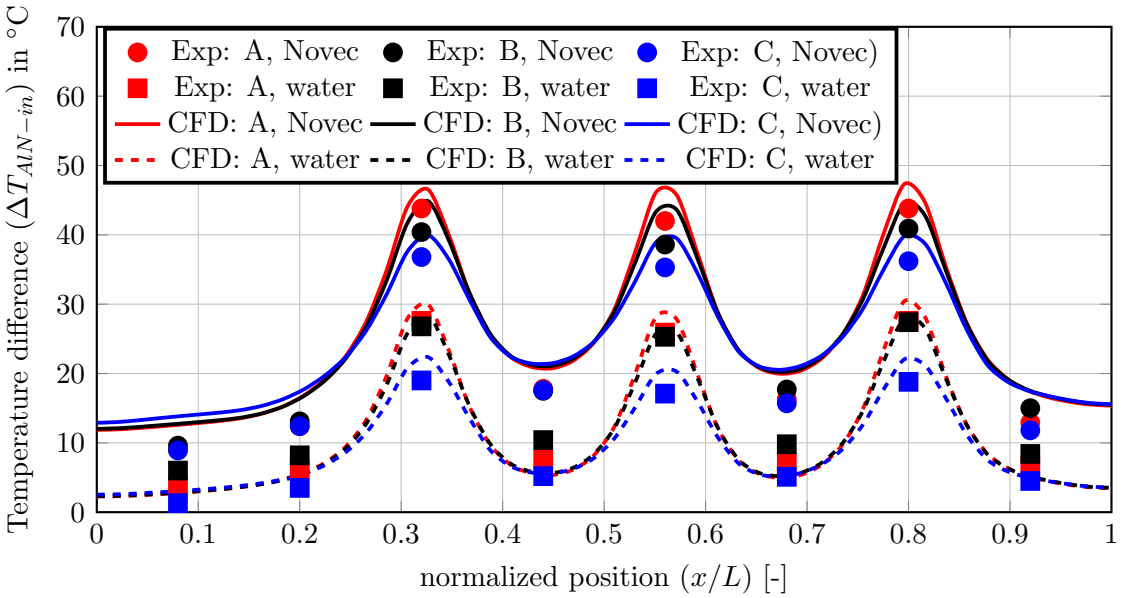


Figure 6.42: Temperature distribution in the AlN for the coolers with 300 µm (A), B=500 µm (B) and 1000 µm (C) copper metallization for a 3 L/min flow rate of water and Novec 7500

shows the corresponding experimentally-acquired thermography. The snubbers appear to be significantly warmer than the dies due to the limited area of contact of the resistors with the DBC, and the right snubber is even hotter because of its poor bonding to the cooler. Overall, the temperature distributions of both figures are similar. The snubbers are slightly warmer in the experiments than in the CFD, likely due to simplifications in the CFD model (the model doesn't consider the solder material between the resistors and the DBC). The temperature of the dies are very similar for both figures.

The bottom figures (6.44c and 6.44d) are taken at the same conditions but with Novec 7500 as coolant. Again, the temperature distribution is relatively uniform, with only minor variations in temperature between the dies and snubbers.

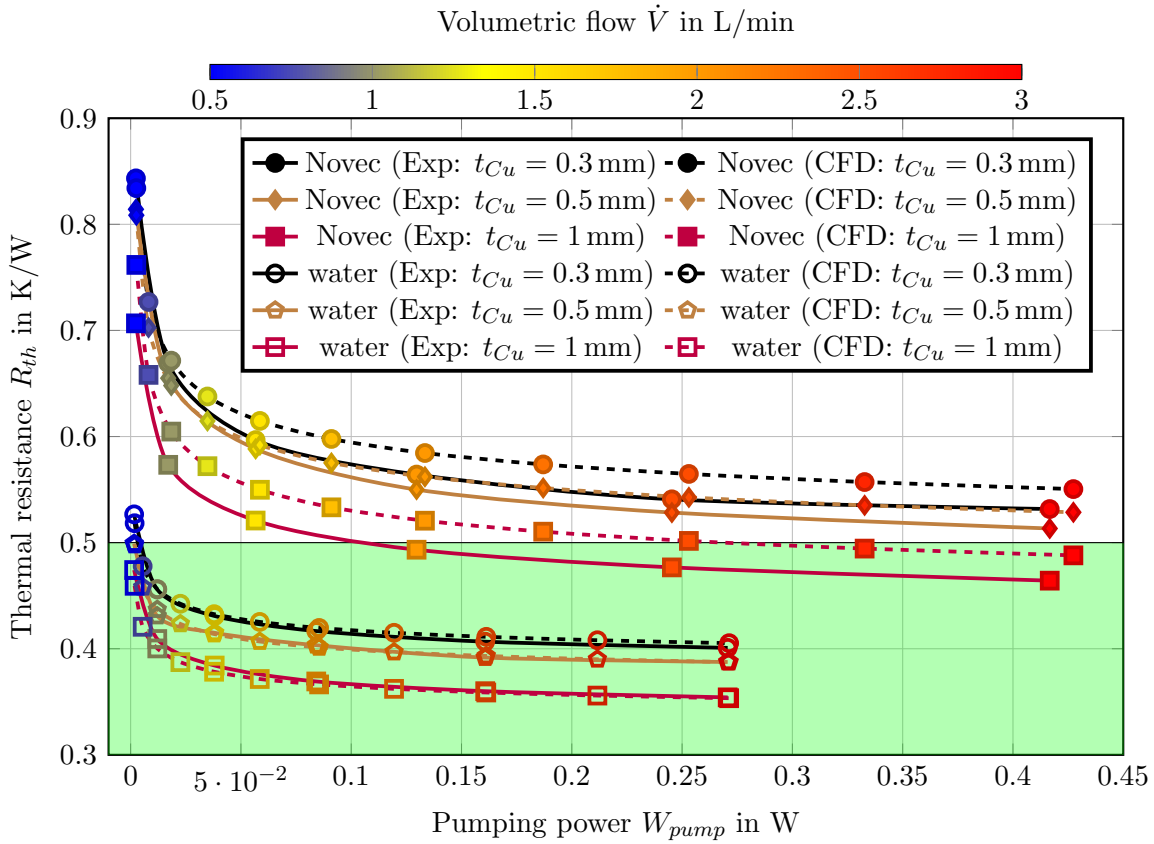
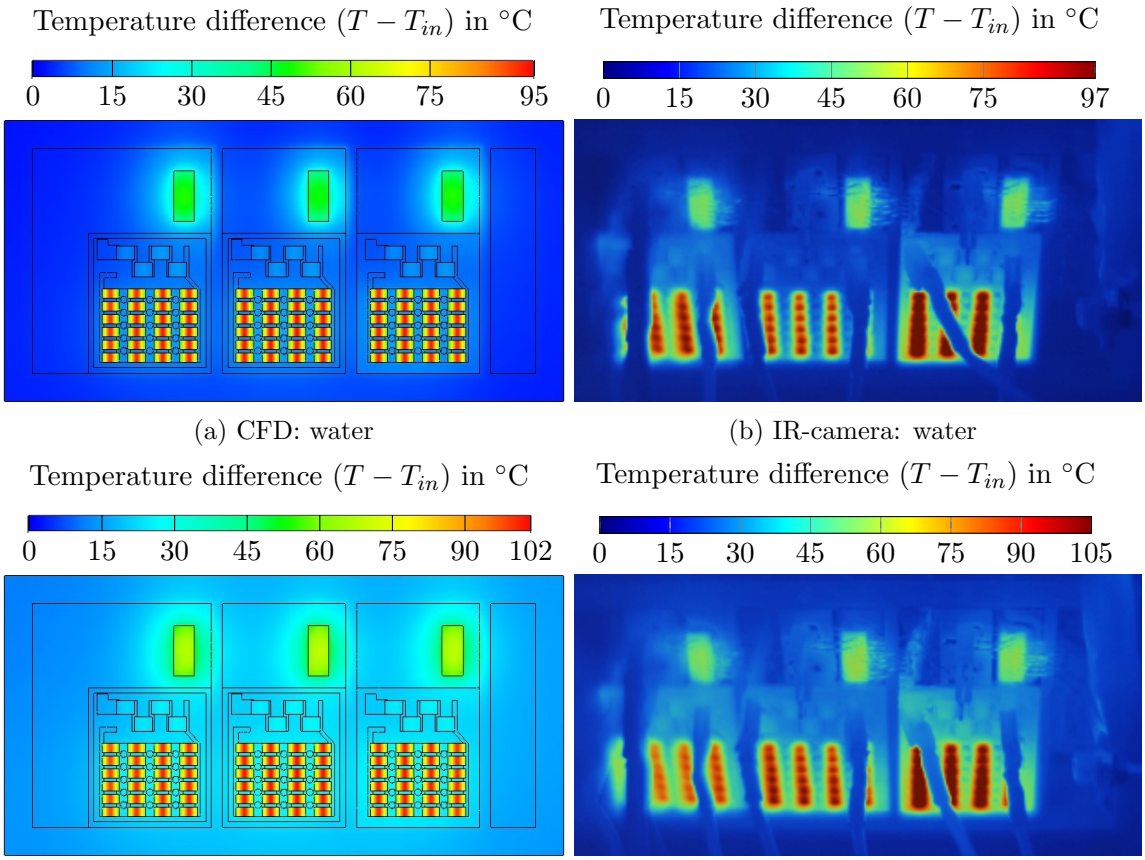


Figure 6.43: The measured and calculated maximum thermal resistance as a function of pumping power with Novec 7500 and water as coolants for different copper thicknesses



(a) CFD: water

(b) IR-camera: water

(c) CFD: Novec 7500

(d) IR-camera: Novec 7500

Figure 6.44: Temperature distribution at the top of the module obtained by CFD and IR-camera with Novec 7500 and water as coolants at 3 L/min for the cooler with 300 µm copper

6.4 Summary

The submodules design is conceived and optimized through the utilization of Computational Fluid Dynamics (CFD) simulations. This design incorporates a hybrid arrangement of pins, featuring both staggered and inline configurations. To enhance cooling efficiency and simplify connections, a single jet is positioned beneath the central die, in an area with an inline pin layout, while the remaining two dies are cooled through a channel flow system with staggered pin layout.

Subsequently, three variants of the AlN coolers are manufactured with various copper metallization thicknesses (0.3 mm, 0.5 mm, and 1 mm), while maintaining identical internal pin-fin structures. They are populated with all the required components (power dies, snubbers, connectors). Following this, a comprehensive experimental assessment of the thermal performance is performed on these three coolers and the results are compared with those obtained from the CFD simulations.

The experimental findings closely match the numerical predictions. Specifically, we observe that increasing the copper thickness improves heat dissipation and overall cooling efficiency. We are easily able to achieve our target thermal resistance of 0.5 K/W using water as the coolant. With "Novec 7500", the objective can still be met by increasing the copper metallization thickness on the AlN coolers (1 mm and using a high coolant flow rate (> 2.5 L/min). Remarkably, this target is achieved with very low pumping power in the system ($P_{pump} < 500$ mW). Furthermore, a uniform temperature distribution is observed between all three dies.

Table 6.6 provides a summary of the thermal resistances obtained through experimental tests and CFD simulations for the three coolers with copper thicknesses of 0.3 mm, 0.5 mm, and 1 mm when using water as the coolant. For the coolers using Novec 7500, thermal resistances are summarized in table 6.7. It is worth noting that the error between numerical and experimental results remains at or below 3 %, indicating a strong agreement between the two results.

Table 6.6: Summary of experimental and simulated results with water.

Flow rate [L/min]	0.5	1	1.5	2	2.5	3	Error
$R_{th,CFD}$ [K/W] (0.3 mm Cu)	0.537	0.48	0.456	0.444	0.435	0.43	2%
$R_{th,Exp}$ [K/W] (0.3 mm Cu)	0.527	0.456	0.431	0.417	0.407	0.4	
$R_{th,CFD}$ [K/W] (0.5 mm Cu)	0.528	0.47	0.447	0.434	0.426	0.42	3%
$R_{th,Exp}$ [K/W] (0.5 mm Cu)	0.5	0.431	0.415	0.403	0.392	0.388	
$R_{th,CFD}$ [K/W] (1 mm Cu)	0.489	0.431	0.41	0.397	0.39	0.384	2%
$R_{th,Exp}$ [K/W] (1 mm Cu)	0.479	0.41	0.388	0.371	0.362	0.356	

Table 6.7: Summary of experimental and simulated results with Novec 7500.

Flow rate [L/min]	0.5	1	1.5	2	2.5	3	Error
$R_{th,CFD}$ [K/W] (0.3 mm Cu)	0.83	0.67	0.615	0.584	0.565	0.55	2%
$R_{th,Exp}$ [K/W] (0.3 mm Cu)	0.84	0.674	0.6	0.567	0.544	0.532	
$R_{th,CFD}$ [K/W] (0.5 mm Cu)	0.809	0.648	0.592	0.562	0.543	0.529	1%
$R_{th,Exp}$ [K/W] (0.5 mm Cu)	0.814	0.655	0.588	0.55	0.528	0.513	
$R_{th,CFD}$ [K/W] (1 mm Cu)	0.762	0.605	0.55	0.52	0.502	0.488	3%
$R_{th,Exp}$ [K/W] (1 mm Cu)	0.707	0.573	0.522	0.497	0.482	0.469	

Chapter 7

Conclusion and perspectives

This thesis addresses packaging solutions for high voltage semiconductors, specifically those exceeding 20 kV. Such innovation holds the potential for a remarkable reduction in the size and complexity of power electronics modules. Conventional packaging structures are faced with a trade-off between electrical insulation, necessitating thick insulating layers, and optimal thermal performance, favoring thin, highly thermally conductive layers. This work introduces a groundbreaking concept aimed at reconciling this competition by employing direct cooling with a dielectric liquid.

The key findings and contributions of this work are summarized as follows:

- Dielectric Coolant Selection: an extensive evaluation of various dielectric liquids results in the selection of Novec7500 as a promising dielectric coolant candidate. Novec7500's high permittivity, closely matching that of AlN, facilitates improved electric field distribution between these materials. Furthermore, it exhibits favorable thermal properties. A comparative analysis is conducted against alternative dielectric coolants, as well as water and water/glycol mixtures serving as reference coolants.

- High Breakdown Voltage (BDV): The proposed packaging, incorporating an AlN cooler and Novec7500, demonstrates a remarkable BDV. With AlN thicknesses of 1.5 mm on both top and bottom sides, an average BDV of 50 kV is achieved. Notably, increasing the AlN thickness to 3 mm empowers the novel package to withstand even higher voltages, up to 62 kV.

- Thermal Performance: An intriguing revelation emerges as thicker AlN substrates not only enhance BDV but also substantially improve cooling performance. Due to its exceptional thermal conductivity, thicker AlN facilitates more efficient heat spreading, enhancing overall cooling efficiency.

- CFD Simulations: This work delves into numerical investigations employing Compu-

tational Fluid Dynamics (CFD) simulations, exploring jet impingement and channel flow cooling concepts. Various pin-fin configurations and arrangements are examined. The findings underscore the superior efficiency of conical pins compared to cylindrical and square alternatives. The research further demonstrates that inline pins excel in jet-impingement cooling, while staggered pins prove more effective in channel-flow cooling scenarios.

- Multi-Chip Submodule Design: Leveraging the differential performance of inline and staggered pins with distinct cooling concepts, a multi-chip submodule, housing three dies and three snubber circuits is designed. This innovative cooler incorporates a blend of inline and staggered pins, with a central jet facilitating cooling for the middle die and channel-flow cooling for the other two. This design minimizes pumping power requirements, and successfully balances the thermal resistance (R_{th}) across different chips within a single module, achieving uniform R_{th} values.

- Copper Spreader Impact: The study highlights the significance of a thicker copper spreader atop the AlN, which substantially enhances cooling performance owing to its superior thermal conductivity. With a 1 mm thick copper layer, the thermal resistance target is met when using Novec7500 as the coolant. Notably, the cooler achieves a specific thermal resistance of $0.155\,\mathrm{cm^2K/W}$ with Novec7500, and this value is further reduced to $0.114\,\mathrm{cm^2K/W}$ when water is employed as the coolant. These results enable the cooling of devices with power losses of up to $500\,\mathrm{W/cm^2}$ while maintaining a junction-to-coolant temperature difference of 60 °C.

In conclusion, this thesis demonstrates a packaging techniques which allows to fully take advantage of high voltage SiC semiconductor devices, by enabling them to operate at both full voltage and low junction temperature (less tan 100 °C, resulting in low on-state resistance). A very good agreement is found between the CFD predictions and the experimental validation, making it possible to use simulation to further optimize the coolers, and adapt them to new specifications.

Perspectives

To advance the understanding and ensure the safety of high-voltage modules exceeding 20 kV, further investigations are imperative. Specifically, a comprehensive examination involving partial discharge breakdown voltage tests should be undertaken. These tests are essential in confirming the module's safety considerations.

Moreover, there is an exciting avenue for enhancing the cooling system's efficiency and performance. This can be achieved by incorporating Novec7500 both as an encapsulant and a coolant at the top of the module. This innovative approach holds promise for several

reasons. Firstly, it introduces dual-sided cooling, effectively immersing the dies on the top side and jet-impingement (or/and channel-flow) cooling of the bottom side, thus potentially improving cooling efficiency. Furthermore, this approach may have a positive impact on the electrical properties of the module. Novec7500 boasts a high dielectric constant that closely aligns with that of AlN, potentially leading to a more uniform distribution of the electrical field within the module.

However, it is essential to emphasize that the realization of these potential benefits necessitates rigorous experimental validation in future studies. Such experiments will provide empirical evidence regarding the safety, cooling performance, and electrical properties enhancements achievable through the application of Novec7500 as both encapsulant and coolant. This represents a critical avenue for future research, offering promising prospects for advancing the state-of-the-art in high-voltage module technology.

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FOLIO ADMINISTRATIF

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NOM : M. Al-HINAAI
(avec précision du nom de jeune fille, le cas échéant)

DATE de SOUTENANCE : 07/06/2024

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TITRE : Doctorat

NATURE : Doctorat

Numéro d'ordre : 2024ISAL0035

Ecole doctorale : N° ED160 Electronique, Electrotechnique, Automatique (EEA)

Spécialité : Génie électrique

RESUME : Cette thèse apporte une contribution à la résolution des problèmes d'encapsulation des semi-conducteurs haute tension. Cette innovation offre la possibilité de réduire considérablement la taille et la complexité des modules ´électroniques de puissance. Les structures d'encapsulation conventionnelles ont depuis longtemps été confrontées au compromis entre l'isolation électrique, qui exige des couches isolantes épaisses, et la performance thermique optimale, qui privilégie des couches minces à haute conductivité thermique.

Ce travail présente un concept novateur visant à résoudre ce dilemme en utilisant un refroidissement direct par un liquide diélectrique et des dissipateurs thermiques en céramique. Avec une épaisseur d'AlN de 3 mm, le nouveau boîtier peut supporter encore des tensions plus élevées, jusqu'à 62 kV. Le refroidisseur atteint une résistivité thermique de 0.155 cm²K/W avec le Novec7500, et cette valeur est encore réduite à 0.114 cm²K/W avec de l'eau. Ces résultats permettent le refroidissement de dispositifs présentant des pertes de puissance allant jusqu'à 500 W/cm².

MOTS-CLÉS : Thermal management, Computational Fluid Dynamics (CFD, CHT), Cooling system, High voltage power electronic, Insulation, Breakdown voltage (BDV), Dielectric liquid cooling

Laboratoire (s) de recherche : Ampère

Directeur de thèse: BUTTAY Cyril

Président de jury : M. FENOT Matthieu

Composition du jury : M. BUTTAY Cyril, M. HUESGEN Till, M. WILDE Jürgen, M. PLATEL Vincent, MME SARTRE Valérie, M. FENOT Matthieu