Self-referenced BIST for random jitter measurement with sub-picosecond resolution at GHz frequency

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"Live as if you were to die tomorrow; learn as if you were to live forever" - Mahatma Gandhi

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1 Introduction

1.1 Context

In the current age of Internet of Things (IoT), high speed communication between interconnected devices has become ubiquitous. The rates of data transfer between devices have only been increasing to support seamless communication between devices connected on a given network. As the data processing capacity of devices increases with each technology, the trend of higher throughputs is here to stay.

The speed of communication is defined by the number of bits transmitted and/or received per second. This is termed as bit/s or more commonly as 'bps'. Throughput has also been measured in bytes per second, abbreviated as B/s. Throughput rates have now reached the speed of Gigabits per second. With such a high rate of transfer, the time available for transmitting or receiving a bit over a given link also reduces. Hence the signals which provide the timing reference in these systems, generally termed as clock signals have to be very precise and accurate. Any error in the periodic occurrence of these clocks will impact the quality of the communication link. Jitter in clocks can cause the clock edges to either lead or lag with respect to the ideal time instant. By characterizing the jitter content of the clocks, this can be factored in the timing budget of the link to evaluate the feasibility for a given Bit Error Rate (BER). With current BER close to 10^{-12}, measuring clock jitter content has become a necessity.

As the throughput rates increase, the clock signal frequency have also increased accordingly. Clock frequencies in the range of Gigahertz is today common. This implies that the clock periods have shrunk to the picoseconds range. In order to respect the tolerable level of BER, the jitter in the clock must be in the order of picoseconds or even sub-picosecond. It requires high precision and expensive instruments to measure jitter of that low value with the desired accuracy. Further, tapping out high-speed clocks for making an off-chip measurement itself adds to inaccuracies by adding additional RLC effects.

On-chip measurement of clock jitter is a viable solution that can overcome the inaccuracies of the off-chip measurement. This also is cost effective since a high resolution equipment is needed for the off-chip measurement and such instruments are expensive. Hence the design of an on-chip instrument that can measure clock jitter with a high resolution is a one-stop solution to the challenges faced in jitter measurement.

1.2 Clock jitter

Jitter is the movement in the rise and fall edges of a clock signal away from their ideal reference. This movement impacts the periodicity of the clock signal and thus when used as a source of timing reference in communication systems, problems arise during transmission and reception of data. There are many causes for jitter in a system. Thermal noise, power supply variations are a few commonly found causes. Jitter can be looked at as deterministic or random clock jitter, depending on the cause of it. Further more, jitter can be measured in many ways, for example, as period jitter, cycle-to-cycle jitter as required for the application. More has been explained about the causes and types of clock jitter in the next chapter.

1.3 Challenges in on-chip clock jitter testing

The measurement of clock jitter with a high resolution has become imperative in the design of high-speed interfaces. The jitter decomposition into deterministic and random components helps in figuring out the sources of deterministic jitter within the system. Measurement of jitter on-chip with such high precision has its own challenges. The requirement starts with the tolerable noise contribution of the devices in the measurement circuitry. Low noise circuits which can also measure with sub-picosecond resolution across process and temperature variations adds stringent specifications on the design parameters. Operation at frequencies in the Gigahertz range adds to further challenges in the design complexity.

1.4 Thesis contribution and outline

This thesis aims to address the challenges in on-chip jitter testing by proposing a novel architecture of an embedded test instrument for jitter estimation implemented in 28 *nm* FD-SOI. In the proposed implementation, the need for an external reference clock for sampling has been taken away by using a self-referenced architecture. Electrical simulations demonstrate the capability to measure jitter for clock signals of frequency 1 GHz or higher with a sub-picosecond resolution of measurement. With a minimal area overhead as a result of using a combination of a Vernier Delay Line and a Time difference amplifier, the implementation proposed in this thesis also explains the use of a fully digital test interface without any need to tap RF pads. The rest of the chapters describe in detail the process of design of the on-chip instrument. The chapters are arranged as follows:

Chapter 2 covers the basics of clock jitter and its significant impact on timing budgets of systems that employ high-speed clock signals. It outlines the various sources of jitter that can exist in a given clock generation circuitry and the different terminologies used for quantifying it.

Chapter 3 describes the challenges in measurement of clock jitter for high frequency signals that are ubiquitous in a high-speed communication system. The different techniques of on-chip clock jitter measurement that have been developed over the years has been presented. Simulations at the behavioral level that draws comparison between the two major techniques used in on-chip measurement is also given. This chapter introduces the self-referenced technique of measurement that is the chosen technique of this thesis.

Chapter 4 delves into the implementation process of the proposed test instrument. System-

level specifications that serve as a guideline for transistor level implementation are derived. The elements of the proposed architecture and their design constraints are presented. The trade-offs linked to the design of the BIST circuitry are also considered.

Chapter 5 is about the circuit-level design of a proof-of-concept prototype. A complete design of an on-chip jitter test instrument is presented, including the implementation of digital control circuitry implemented in an FPGA. Simulation results at transistor and post-layout level are provided to validate the feasibility of the proposed on-chip test technique.

Finally, Chapter 6 summarizes the work performed in this thesis and discusses the directions for future research on this topic.

The list of publications resulting from this work and the references used in the development of the instrument are added towards the end of the document.

2
Clock jitter

This chapter presents a brief introduction to clock jitter and its impact on communication quality of high speed systems. It also describes the various sources of clock jitter, typically classified as random and deterministic jitter. The different types of clock jitter measurement and the resulting jitter terminologies that are common practice in industry and academia have also been explained.

Contents

2.1 Introduction to Clock jitter

In the domain of signal processing, a timing reference is required to carry out signal processing operations. The signals used to provide this time reference are termed as clock signals. These signals have periodically occurring transitions in their amplitude levels - the amplitude of the clock changes from a logical level of a 0 to 1 and 1 to 0 at regular intervals and is defined as a unit clock cycle. The duration of this clock signal, called as *'Time Period'* determines the smallest unit of time reference for signal processing possible in a given system. Clock frequency is the inverse of time period. Fig. 2.1 shows a generic diagram for a clock signal. Data transmission operations are timed at the rising edge and/or the falling edge instants. In the age of IoT, clock signals in the Gigahertz range are commonplace.

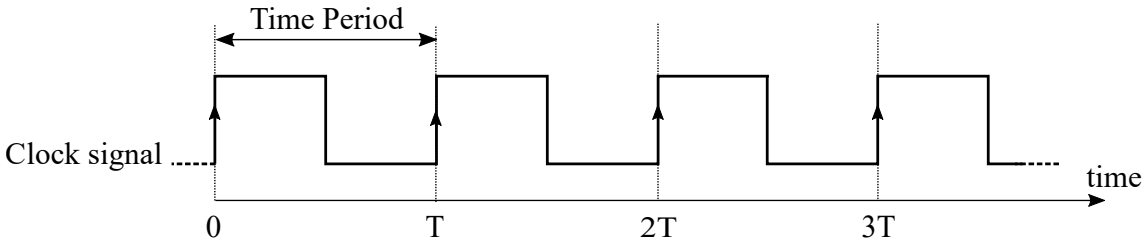


Figure 2.1: Clock signal

Clock signals play a very important role in communication systems. Higher the frequency of the clock signal used, higher is the speed of data transfer that can be supported. Enhancing the rate of data communication has enabled seamless connectivity of devices. The current age of IoT (Internet of Things) and Virtual Reality (VR) has been enabled thanks to the improved throughput rates of communication. Data throughput or the speed of data transfer is the number of bits or bytes that are transmitted within a given clock cycle and is specified as *bits per second* (bps) or *bytes per second* (B/s). Typically seen data transfer speeds in Wireless Local Area Networks (WLAN) is hundreds of Megabits per second (Mbps). The Universal Serial Bus (USB) standard that supports high speed interface between a computer and peripheral devices can transfer data upto 5Gbps.

Current trends in the field suggests that the communication speeds will only be augmented towards faster links and increase in the number of connected devices, which will require more data throughput. In keeping with this trend of a faster rate of data transfer across and between devices, the clock signals that provide the time reference for this transfer to occur have been increasing in frequency. Clock frequencies in the Gigahertz range are commonplace as of today.

An ideal clock signal has periodically occurring rising edges and falling edges. However, fluctuations occur in the time instants of signal edges because of a variety of reasons. The timing variations of these signal edges from their ideal values is termed as *clock jitter*. Fig. 2.2 depicts the concept of clock jitter. The waveform 'Ideal clock' shows clock cycles with a time period of 'T', with 50% duty cycle. Jitter in clock signals is typically caused by noise or other disturbances in the system. Contributing factors include thermal noise, power supply variations, loading conditions, device noise, and interference coupled from nearby circuits.

2.1.1 Causes and impact of clock jitter

Noise in a clock signal can be fundamentally identified as undesired variation in the zero crossings or threshold crossings. These fluctuations termed as jitter can be caused by perturbations in the rise and fall transition time instants of the clock or can arise from noise in the amplitude levels which eventually impact the time instants of zero crossing of a signal. Variation in the supply voltage of the oscillator and thermal noise of the devices used in the oscillator and the clock generation circuitry can cause timing perturbations. Any coupling of a switching activity that is happening

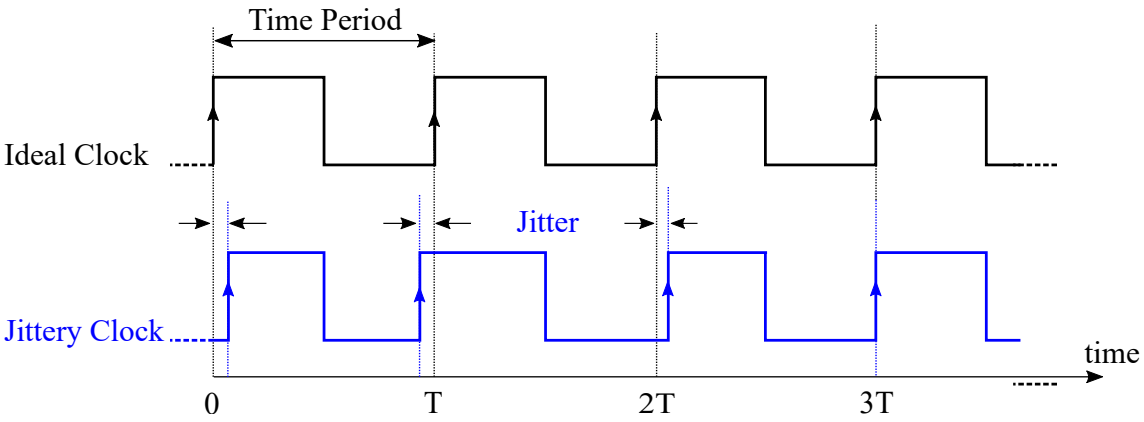


Figure 2.2: Clock jitter

on the SOC, crosstalk and any variation in the amplitude of the generated signal can also add to the jitter of the clock.

Jitter in the clock can impact the performance and reduce the quality of SoCs. We now look at the adverse impact of clock jitter on different applications.

Impact of clock jitter on serial communication

Serial communications are one of the most area efficient solutions for chip to chip data transfer at very high speeds. These transceivers convert parallel data to serial at the transmitter and vice versa at the receiver. Data transfer speeds have reached 100 Gbps and work is underway to improve the speeds further to support applications such as High Performance Computing (HPC), Artificial Intelligence (AI), IoT, automotive etc. in SoCs.

Clocks used in the transmitter allow for serialization. In the receiver side, a Clock recovery circuit extracts a bit rate clock from the incoming serial data. This recovered clock "clocks" the incoming bit stream as shown in Fig. 2.3. The received bit stream is then converted back to parallel byte sized data. Hence, this circuitry known as Clock/Data recovery (CDR) determines the conversion of serial data back to parallel.

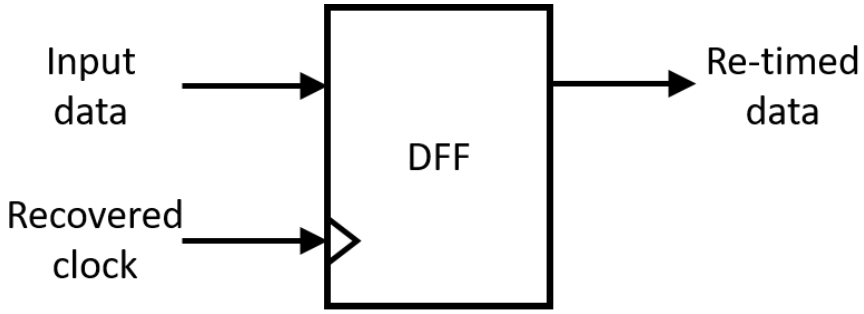


Figure 2.3: Re-timing with recovered clock at SerDes receiver [1]

The bit rate, i.e. the duration of one data bit, is generally considered as a unit interval or *UI* [1]. During the process of data recovery, the clock signal samples the data at instants that are each one UI apart. These instants can correspond to the rising and/or falling edges of an ideal clock free of jitter. In the case of an ideal clock, these instants are exactly one UI apart, and the input data is sampled without any error to form the re-timed data. Fig. 2.4 shows data re-timed using a recovered clock without jitter. After every time duration 'T', the rising edge of the ideal clock samples the input data stream and generates the re-timed data. Jitter in the recovered clock causes the sampling instants to move away from their ideal locations. This leads to errors in the

re-timed data as compared with the input data. Fig. 2.5 shows jittery data compared against an ideal data stream.

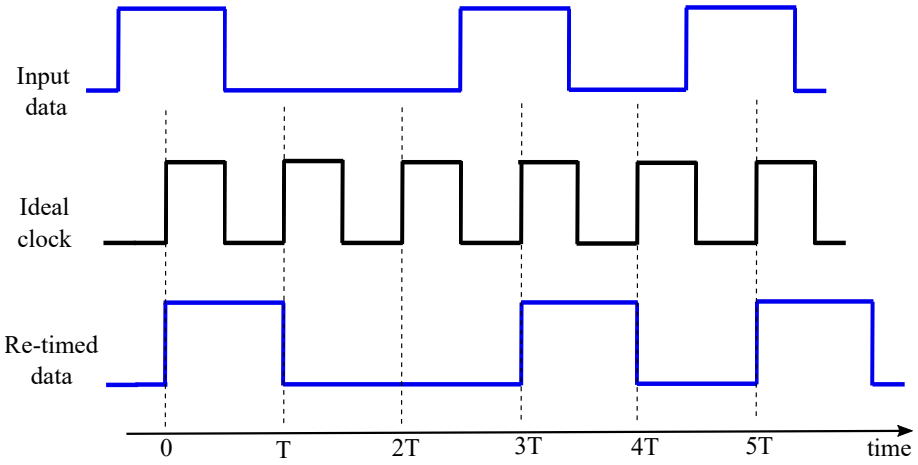


Figure 2.4: Input data is re-timed with an ideal clock [1].

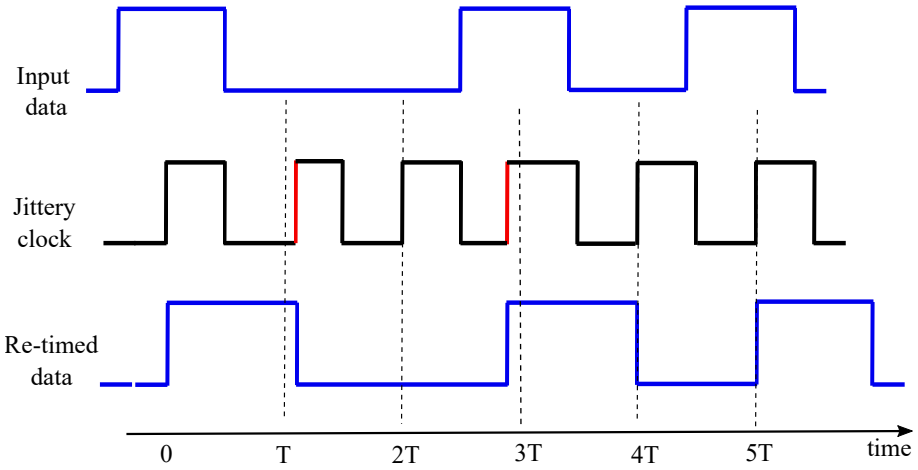


Figure 2.5: Input data is re-timed with a jittery clock [1].

High-speed serial links like SerDes use eye-diagrams to analyze performance and for compliance testing. An eye diagram is generated by overlaying segments of the data-stream over one (or multiple) UI in succession. This allows for visual analysis of the recovered data and evaluate for paramaters like jitter, Inter-Symbol Interference (ISI) etc.

Fig. 2.6 shows an ideal eye diagram with the sampling point annotated. The sampling point is the time instant at which the signal amplitude that represents “0” and “1” are farthest apart. This is referred to as the eye height and is also known as the vertical eye opening. This sampling point provides the ideal time instant at which the data can be sampled by the rising edge of the clock, without making any errors in the sampling. The width of the eye provides the time margin for error-free sampling of data. The more open the eye, the lesser the chances that an error is made at the receiver, and hence, the lesser the BER.

Fig. 2.7 shows a rising clock edge impacted by clock jitter. The diagram reveals how jitter can cause the clock edges to move away from its ideal location and hence the sampling point might not be located in the middle of the eye. This means that the data can be sampled before or after the sampling point and errors can occur in the sampled data. Fig. 2.8 shows an eye diagram affected by jitter. The lead and lag of the edges can accumulate over time in such a way that the eye can sometimes get closed in the horizontal direction. The wider the eye opening, the larger the margin

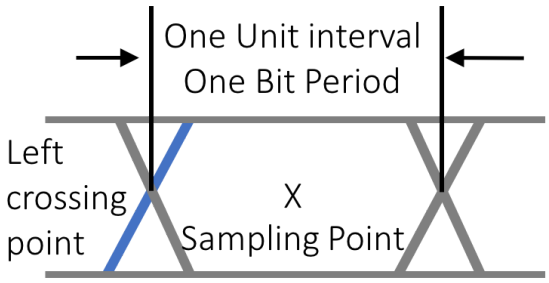


Figure 2.6: An ideal eye diagram

for error-free operation. By closing the eye horizontally because of jitter in the clock, there will be no margin left for the operation that can guarantee an error-free detection. Noise in the amplitude of the clock signal can also exist along with jitter as shown. This affects the vertical height of the eye. Interference from a closely located signal can impact the signal amplitude adversely, causing fluctuations in the threshold crossings in the time domain. An eye diagram showing the impact of noise perturbations and jitter is shown in Fig. 2.9 .

The presence of all of these noise sources can cause the eye to be completely closed in both the horizontal and vertical direction. This means that a value of "1" and "0" cannot be distinctly sampled since there exists no time instant for an error free sampling. This is called closure of the eye. Communication systems employ equalization and jitter cleaning for data detection in such instances of closed eye. Most of these fluctuations can occur because of the filtering of high frequency components by the transmission channel. By carefully selecting equalizer co-efficients that can offset the effect of the channel and delay in propagation, such eye closures can be tackled.

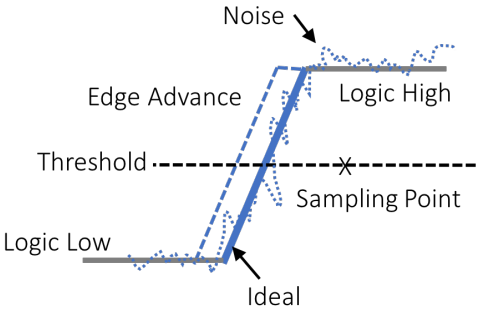


Figure 2.7: A clock edge affected by jitter

Jitter in ADCs and DACs

In data converters, where analog data is sampled to generate a digital bit stream and vice versa, the clock frequency determines the rate of sampling. The higher the clock frequency, the higher the possible data conversion rate from Analog to Digital (ADC) and Digital to Analog (DAC). The sampling instants for the data conversion is also determined by the clock. In an ideal scenario, if the clock has a time period 'T', then the data is sampled every 'T' seconds for the conversion as shown in Fig. 2.10 . Once the data is sampled at a given time instant, decision of a bit being $'1'$ or $'0'$ is made. Since the data is continuously changing, it is required that the sampling is done periodically at the correct instants.

In the presence of jitter in the clock, the sampling for the conversion may not happen at the correct time instants, leading to errors in the sampled and converted data. This can be quantified by the impact of jitter on the Signal to Noise (SNR) of the converter. In addition, as the input data

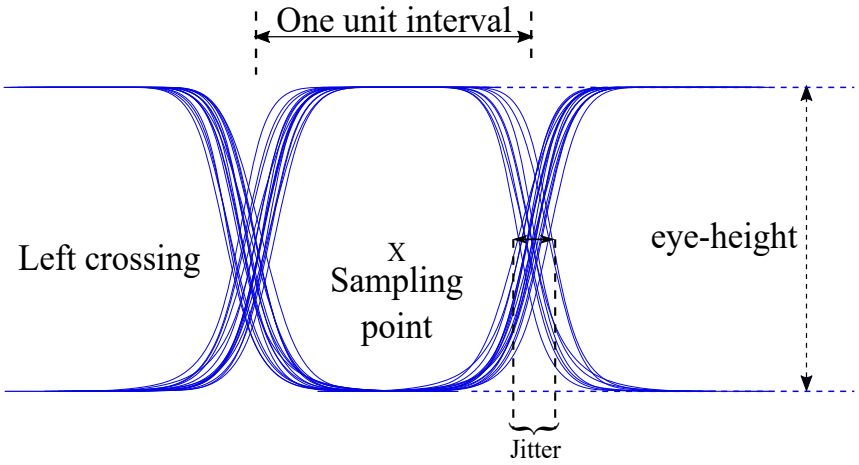


Figure 2.8: An eye diagram with clock jitter

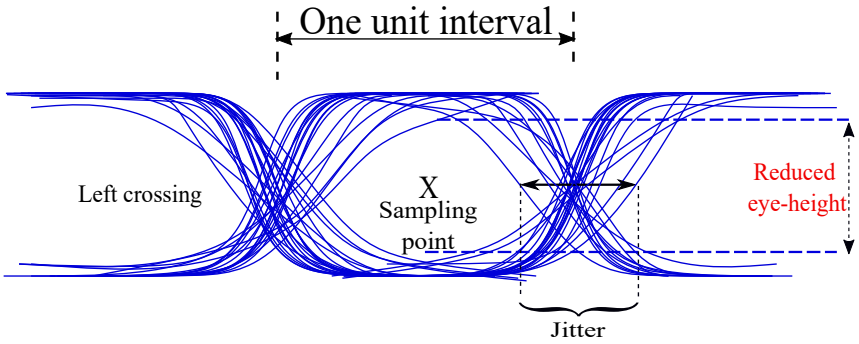


Figure 2.9: An eye diagram with noise and jitter

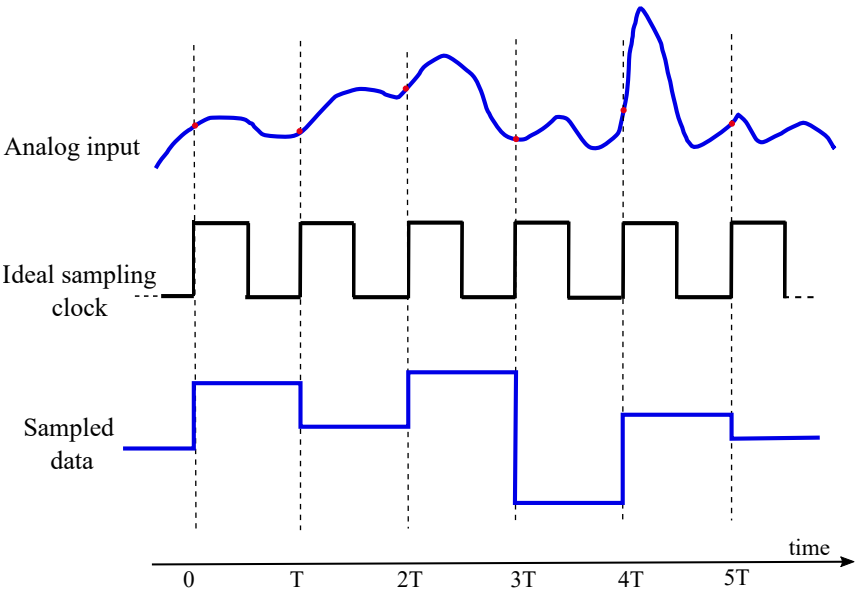


Figure 2.10: Sampling in ADC

frequency increases, a higher slew rate in the data signal leads to more noise during the conversion. Fig. 2.11 shows the resulting noise ΔV during sampling for two signals with different slew rates. As the slew rate increases, the noise increases for the same amount of jitter in the sampling clock.

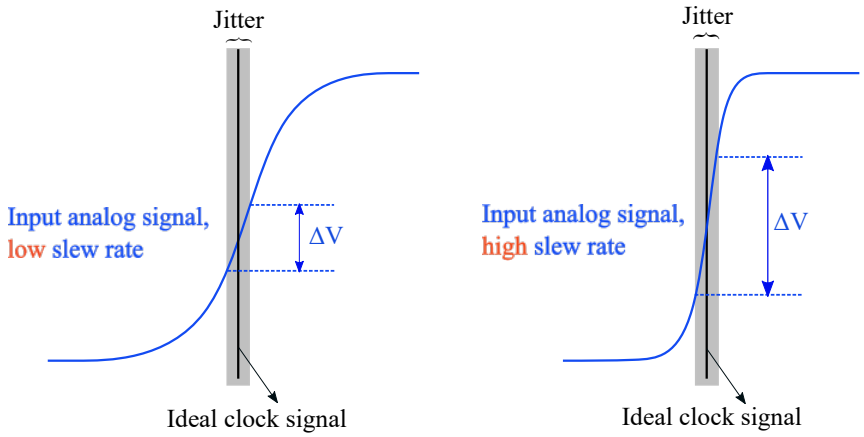


Figure 2.11: Impact of jitter on sampling noise

2.1.2 Classification of clock jitter

Timing deviations that can occur in a given clock signal can be broadly classified as random or deterministic depending on the underlying sources producing them. Fig. 2.12 illustrates this classification with the sources briefly mentioned.

The main source of random jitter (RJ) is electrical noise within system components that is Gaussian in nature [11]. Electrical noise can cause fluctuations in the transition time of signals. These fluctuations interact with the slew rate of signals and produce timing errors at the threshold crossing points. The other source of random jitter could be shot noise. This type of jitter is not bounded in nature, which means that a minimum or a maximum bound for the value of such jitter cannot be measured. It can then only be described by its statistical properties, such as the (Gaussian) probability distribution. Random jitter is often characterized by its standard deviation (RMS) value.

The other main category called deterministic jitter (DJ) is always bounded in amplitude and occurs because of specific causes. DJ has a non-Gaussian probability density function and is characterized by its peak-to-peak value. Sources of deterministic jitter can often be attributed to the presence of noise or switching activity from another closely located signal. If the switching activity from a closely located digital signal or in the power rail gets coupled to the clock signal, the jitter will have periodic properties and is often quoted as period jitter or sinusoidal jitter. This jitter is represented by the amplitude and frequency components. Another cause could be clock feed-through from the PLL. The next category of deterministic jitter is bounded uncorrelated jitter, which arises from crosstalk. Period jitter and bounded uncorrelated jitter are both data-independent jitter. On the other hand, data dependent jitter can be further categorized into jitter because of Intersymbol interference (ISI) and that due to duty cycle distortion. Jitter due to ISI is because of lossy channel characteristics. The interconnects are mostly capacitive in nature and hence the high frequency components of the clock are filtered out. This causes slower transitions in the bit stream. As a result of the capacitive nature of interconnects, a memory effect is created. A transition from an amplitude level of 1 to 0 or from 0 to 1 doesn't complete within the bit rate and can extend into the time slot of the adjacent bit and hence this interference of adjacent symbols can lead to jitter. Since the jitter depends on the pattern of data being transmitted, it is categorized as "data dependent jitter".

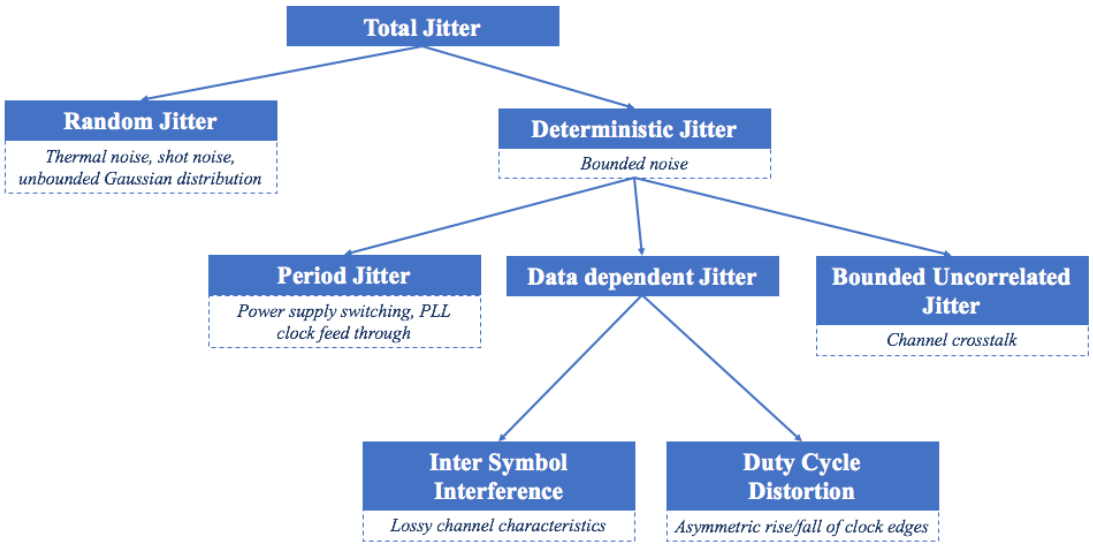


Figure 2.12: Jitter classification based on sources

Jitter histogram

In order to better analyze jitter, a graphical representation in the form of histograms is employed. A generic jitter histogram is shown in Fig. 2.13, where the x-axis represents numerical values of jitter divided into equally spaced intervals called 'bins', and the corresponding value in the y-axis is the number of occurrences of jitter values falling into the specific interval, and is labelled as the 'Hits' for a given bin. Fig. 2.14 shows a histogram generated from the jitter values of random jitter. Random jitter is unbounded in value, hence the range of values increase with the sample size. The shape of the histogram resembles a bell curve since the distribution is Gaussian in nature.

The shape of the histogram depends on the source of jitter. As another example, consider sinusoidal jitter of frequency 1MHz with an amplitude of 10ps added to a 1GHz clock. The resulting histogram will have a dual-Dirac distribution, as shown in Fig. 2.15 where the distance between the peaks is also the peak to peak amplitude of the sinusoidal jitter.

In most cases, several jitter sources can exist simultaneously, resulting in jitter that includes both deterministic and random jitter components. The resulting jitter is the sum of its components. While random noise is uncorrelated, the total variance of RJ from all components will be the sum of variances of each RJ component. The total deterministic jitter could be calculated as the linear sum of every DJ component. In the histogram shown in Fig. 2.16, random jitter (RJ) and sinusoidal jitter (SJ) are both present. The dual-Dirac and Gaussian curves can be seen in the histogram. Analysis of jitter from such composite histograms involves decomposing jitter into its RJ and DJ components.

2.2 Measurement of clock jitter

Jitter in a clock signal can be be measured by its statistical properties, and analyzed from its histogram shape. An alternate way of characterizing jitter is by treating it as a discrete-time signal. This type of characterization helps to analyse jitter regardless of its type or cause.

Let us consider a generic equation for a clock signal as [1]:

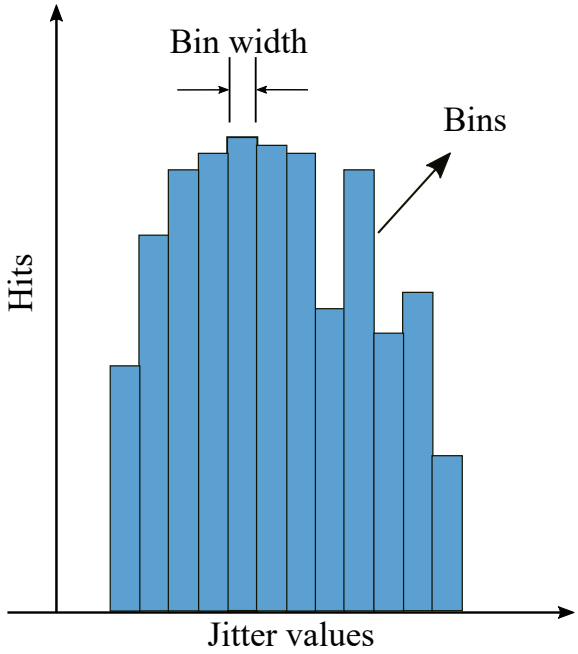


Figure 2.13: Generic jitter histogram

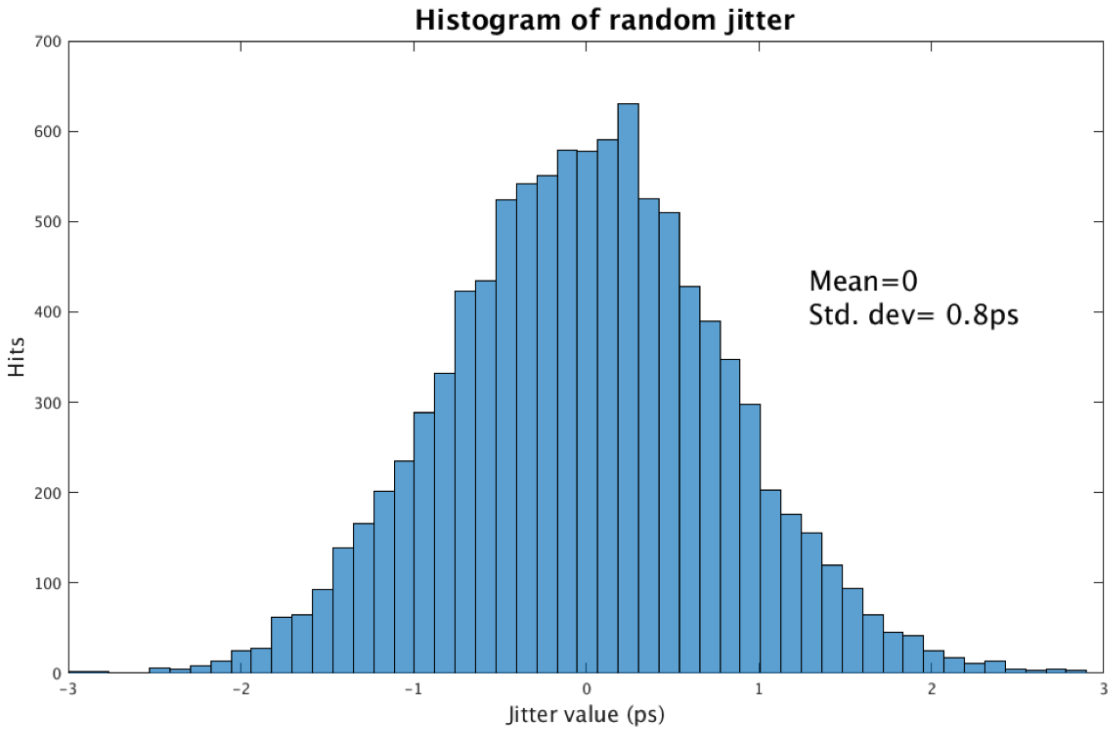


Figure 2.14: Histogram of Random Jitter

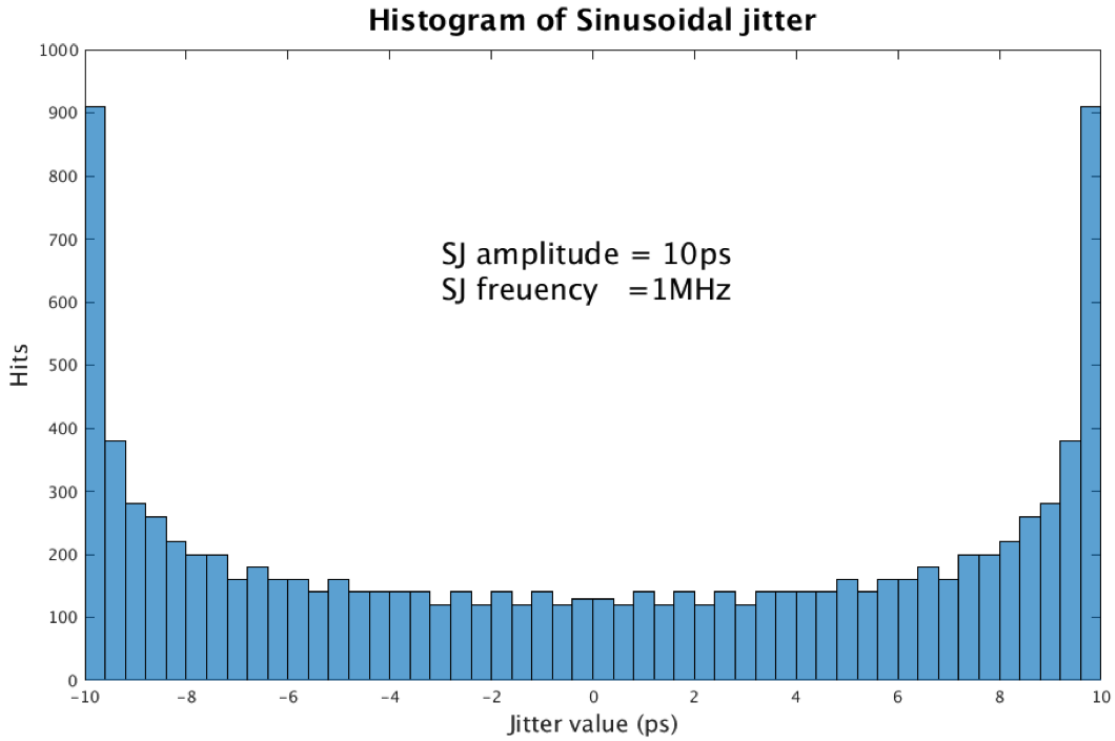


Figure 2.15: Histogram of Sinusoidal Jitter

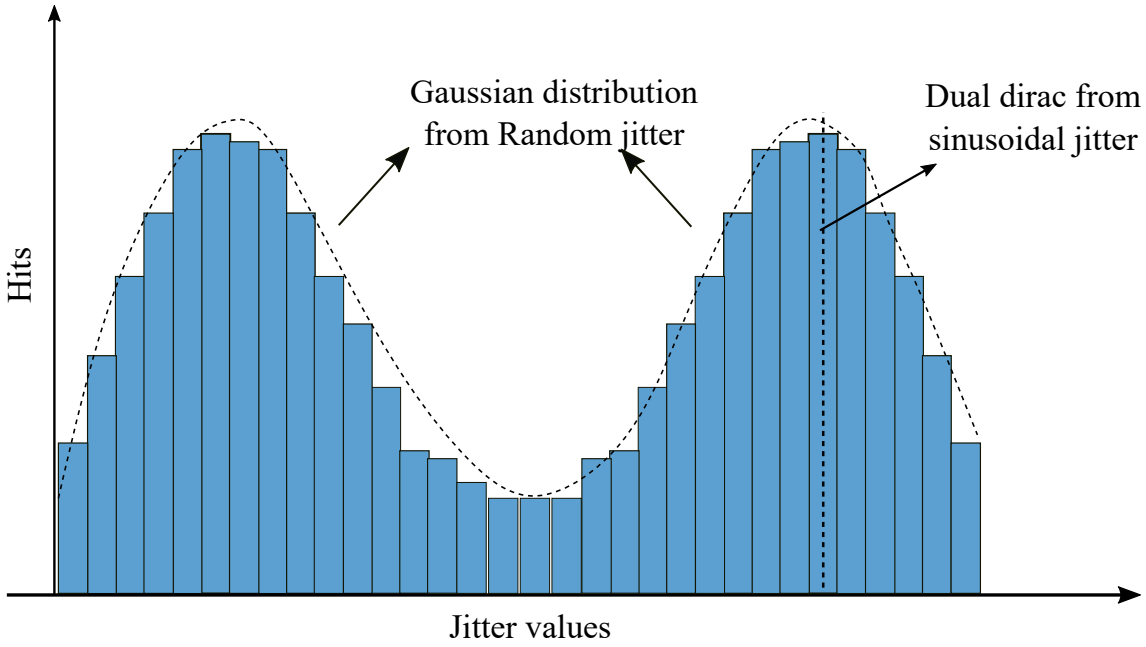


Figure 2.16: Histogram of composite Jitter

$$s(t) = A(t)sin(\omega_0(t) + \varphi(t), \tag{2.1}$$

$A(t)$ is the amplitude of clock signal which will be considered to be a constant for the treatment on jitter. The quantity $\omega(t)$ is the frequency of the clock, and $\varphi(t)$ is the variation in phase due to jitter. For an ideal clock signal, $\varphi(t)$ is zero, and the factor $\omega(t)$ is independent of time. The time period of $s(t)$ is given by $T = 2\pi/\omega_0$. The zero crossings of signal $s(t)$ are kT apart, where k is an integer.

In the presence of any fluctuations because of noise and other factors, both $A(t)$ and $\varphi(t)$ could be nonzero and hence vary with time. The quantity $A(t)$ captures the variation in the amplitude of the signal, which could occur because of amplitude noise or distortion. Even though $A(t)$ is non zero, the zero-crossing time instants of the signal still occur at kT, and hence this signal can still be considered as an ideal clock without jitter as there are no time related perturbations. For the further analysis on jitter, we consider $A(t)$ to be constant.

On the other hand, the quantity $\varphi(t)$ added to the ideal phase $\omega_0(t)$ in the argument of the sinusoid causes the zero crossings to deviate from the ideal instants kT , which is termed as clock jitter. The quantity φ is also called excess phase, phase deviation, phase noise or phase jitter. The following sub-sections define the various terminologies used to mathematically represent jitter content of a signal.

2.2.1 Jitter terminologies

The phase and excess phase of the sinusoidal signal can be measured in many ways depending on the application or requirement. The mathematical representation of the different ways in which jitter can be measured for a signal is given in this section.

Absolute jitter

The rising and falling edges of a clock are moved around from their ideal locations in the presence of jitter. When we compute jitter content by comparing the position of edges in the jittery clock with the corresponding edges of an ideal clock (it is not affected by jitter), this measurement is termed as 'absolute jitter'. The measurement here is done with an absolute value for time instants of the ideal clock edge and hence the name. The clock period of the ideal clock is considered as T. For the jittery clock, we assume the clock period to be T, as every clock cycle will either be shorter or longer than the ideal time period, but the mean value would be close to the nominal value.

For measuring absolute jitter, we compute the time difference between corresponding rising edges in the ideal and the jittery clock. Fig. 2.17 explains the concept of this measurement.

Absolute jitter can thus be defined as given in (2.2), where a_k is the value of absolute jitter for the $k-th$ clock edge, and is the time displacement of the $k-th$ rising edge t_k of the jittery clock with respect to the corresponding edge of the ideal clock. The ideal clock has rising edges at every time instant kxT, where T is the time period.

$$a_k := t_k - kT \tag{2.2}$$

Period jitter

An alternate way of analyzing clock jitter is by comparing the time instant of clock edge with the previous edge of the same clock. This measurement is termed as period jitter. It can be defined as a discrete time sequence p, where the element p_k is the variation around its nominal value of the position of one clock edge with respect to the previous edge. This measurement effectively considers variation in the duration of one clock period with respect to the previous, and hence p

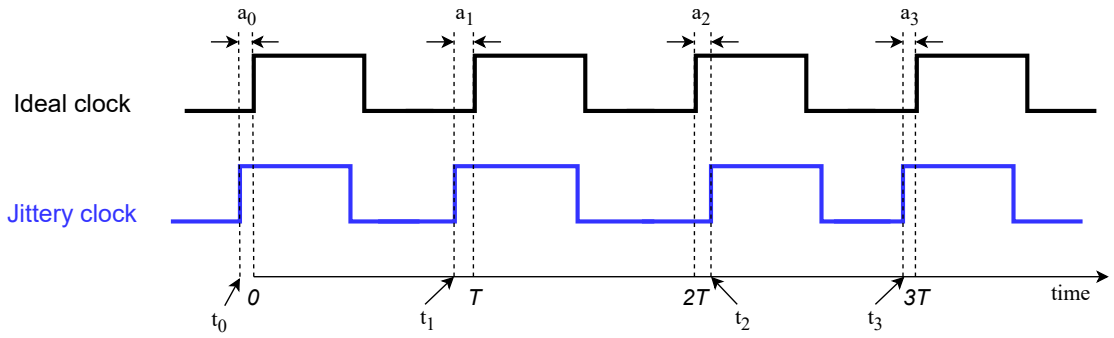


Figure 2.17: Absolute Jitter

is a random process which is equivalent to the variation of the actual clock period with respect to the nominal period.

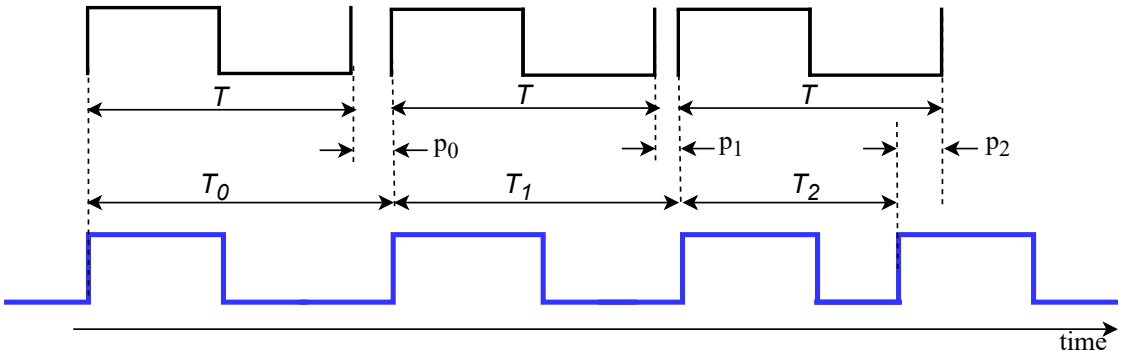


Figure 2.18: Period Jitter

Fig. 2.18 illustrates the concept of period jitter measurement. Each period of the clock is compared to the nominal period (blue clock signals). Any deviation in the time duration contributes to period jitter. The $k-th$ sample of the period jitter will be indicated as pk and can be mathematically defined as given in equation (2.3):

$$p_k := (t_{k+1} - t_k) - T = T_k - T \tag{2.3}$$

where t_k and t_{k+1} are the time instants of two consecutive rising edges of the clock, T is the nominal clock period, and T_k is the actual clock period. The period jitter can be expressed in terms of absolute jitter as:

$$p_k = a_{k+1} - a_k \tag{2.4}$$

For the case of digital processing systems, a constant clock period is required for computations to be timed. This time duration allows for propagation delays, transition times of the signals, etc. These computations occur as part of a state machine and hence follow a certain sequence of operation. Any variation in the clock period decreases or increases the time available for computations, which might lead to erroneous data for the consecutive computation. Hence in such applications, the jitter measurement of interest is the period jitter.

Cycle-to-cycle jitter

The cycle-to-cycle period jitter, mostly known as cycle-to-cycle jitter, is defined as the variation in cycle time of a signal between adjacent cycles. This variation is measured over a random sample

of adjacent cycle pair. It is the difference between two consecutive clock periods and it indicates how much the duration of one clock period differs from the previous one. If we denote with T_k the $k-th$ period of the clock, the cycle-to-cycle jitter cc_k is defined as given in (2.5):

$$cc_k := T_{k+1} - T_k \tag{2.5}$$

The cycle-to-cycle jitter can also be expressed in terms of the period jitter as given in (2.6). From the equation, it can be seen that cycle-to-cycle jitter is the first order derivative of period jitter

$$cc_k = p_{k+1} - p_k \tag{2.6}$$

and, in terms of absolute jitter, the cycle-to-cycle jitter can be defined as shown in (2.7). As can be seen from the equation, cycle-to-cycle jitter can be defined as the second order derivative of absolute jitter.

$$cc_k = a_{k+2} - 2a_{k+1} + a_k \tag{2.7}$$

2.2.2 Phase noise and jitter

Clock jitter is a measurement of the time deviation of clock edges. Phase noise denotes the frequency domain equivalent of this variation. It is defined as the power of a signal in 1Hz bandwidth at offset f from the carrier, divided by the power of the carrier, as given by [1]

$$L(f) = \frac{S'_v(f_0 + f) \text{ in 1 Hz bandwidth}}{P} \tag{2.8}$$

where S'_v is the one-sided voltage PSD of a voltage periodic signal with frequency f_0, power P, and affected by random excess phase modulation φ. It should be noted that the random excess phase modulation is used to model the variation in phase which leads to jitter as of a clock defined by (2.1), and is a continuous-time process. Clock jitter on the other hand is a discrete time sequence, since it can be measured at the zero-crossings of the clock.

Fig. 2.19 shows a typical plot of the phase noise curve. The y-axis shows the signal power with respect to the carried measured in *dBc* and the x-axis is for the frequency in the logarithmic scale. For measuring the jitter value over a range of frequencies, we can measure the area under the curve for the frequency range of interest.

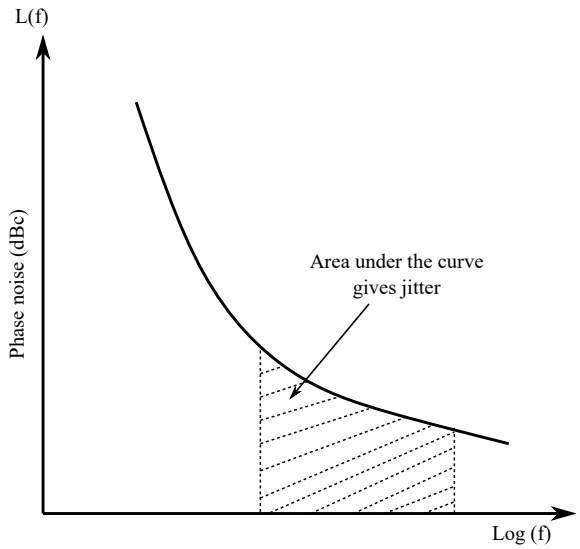


Figure 2.19: A generic plot of phase noise

2.2.3 Need for sub-picosecond resolution for jitter measurement

At the current data transfer speeds of multi Gigabits per second, it is important to measure jitter with higher accuracy [2]. The most important measure of quality for a communication system is the BER (Bit Error Rate). For high speed I/O found in the market today, the BER is typically of 10^{-12} and even smaller. At this BER, when transmitting at 10 Gbps (10^{10} bits/s), the average time to find a bit error is about 25 hours. Clearly, testing BER in production is impractical [4].

The relationship between BER and total jitter is described in Equation (2.9) [2]. Total jitter is the addition of RJ and DJ components, which can be computed by the heuristic given in Equation (2.9), where the function $N(BER)$ is the total peak-to-peak jitter of a unit normal distribution (i.e., a Gaussian with zero mean and a standard deviation of 1) at the specified BER and the constants RJ and DJ represent all of the components of random and deterministic jitter respectively. The random jitter is modeled by a Gaussian, and the deterministic jitter by a pair of impulses separated by the value of the parameter DJ. The total jitter is therefore a function of BER and is related to a distribution consisting of a Gaussian convolved with a pair of impulses, as shown in Fig. 2.20. As a result of RJ, the location in time of the clock transitions varies over a range of values. The longer the transitions are observed, the greater this range will be since RJ is unbounded. Suppose during a data transfer, a transition in the data signal occurs for every rising edge in the clock. Thus, a clock transition at the wrong time will lead to a bit error. In other words, the probability of a clock edge deviation is equal to the bit error rate contribution due to jitter.

$$Total\,jitter = N(BER) * RJ + DJ \tag{2.9}$$

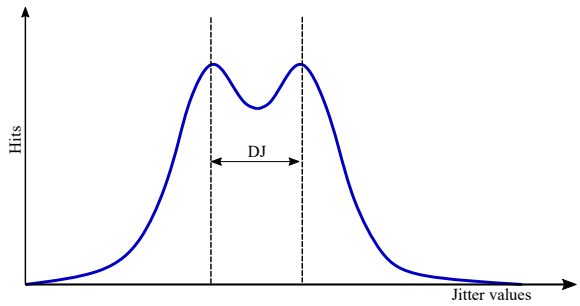


Figure 2.20: Jitter PDF model corresponding to the heuristic in Equation (2.9) [2]

Fig. 2.21 shows a plot of BER variation with jitter, where y-axis represents BER variation and x-axis is the period of transmission of one single bit 'T'. The DJ component is bounded, but the RJ component increases with the sample size. The edges of the curve are directly related to the tails of the Gaussian functions that describe RJ. The distance between the jitter curves is the timing margin available for the corresponding BER. The further the left edge of the curve is from the right edge at a specified BER, the more margin the design has for jitter. Hence, this plot also gives the confidence interval for the transmission to occur for a specified BER [2]. For data transfer speeds of multi Gigabits, the available bit duration and hence the clock time period will be in the range of hundreds of picoseconds. For a good quality communication link, the tolerable deviation in the clock edges needs to be several orders of magnitude smaller than the time period. This necessitates the measurement of clock jitter with a sub-picosecond resolution.

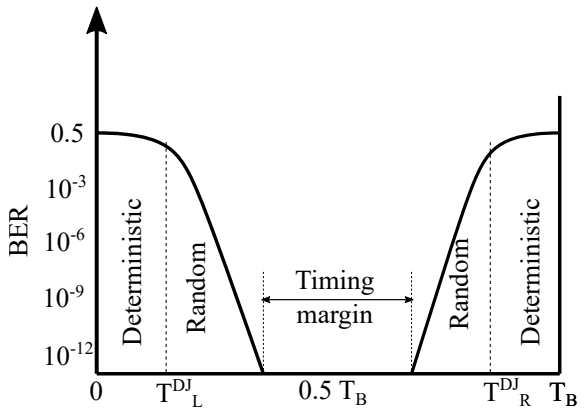


Figure 2.21: BER bathtub plot

2.3 Conclusion

This chapter covers a brief introduction to the concept of clock jitter and the various causes and terminologies used to analyse and describe jitter in a system. At present, communication speeds have reached hundreds of Gigabits/s, which can tolerate jitter levels up to few tens of picoseconds to maintain a very low BER. This requirement necessitates a sub-picosecond resolution for the measurement of clock jitter. The following chapter describes existing methods of measurement and provides a review of relevant literature.

3

Implementation of self-referenced technique

This chapter presents a study on existing methods for on-chip clock jitter measurement. It also gives an introduction to the self-referenced technique of jitter measurement. A detailed description about the architecture of an instrument that measures clock jitter using the self-referenced technique has also been included.

Contents

3.1 Introduction

Many techniques of on-chip measurement have been developed by the industry and academia over the last two decades. The basic principle for jitter measurement is to sample the clock of interest around the vicinity of the expected clock edge to observe the possibility of occurrence of a clock edge. In the presence of deterministic jitter which is bounded, the clock edge deviates within a minimum and maximum range. In the case of random jitter which is unbounded, the deviations increase with sample size. By obtaining statistical information about the behaviour of a clock edge, the jitter histogram is generated. The shape of the histogram is altered by the type of jitter contained as has been explained in Section 2.2 . This histogram is processed to compute the jitter content in the signal.

In practical applications, both deterministic and random jitter content are present and this is termed as composite jitter. Hence the obtained jitter histogram will look similar to Fig. 2.16 and an annotated version of this histogram is reproduced here in Fig. 3.2 The first step in jitter measurement in the presence of composite jitter is jitter decomposition, which is used to separate the deterministic and random content. A commonly found technique for jitter decomposition in the time domain is tail-fitting and is described in [12]. The histogram in the presence of only random jitter is Gaussian in nature and hence the tail part of the composite jitter is identified for fitting the curve. This gives the name 'tail-fitting'. The peak to peak value of the deterministic jitter can be calculated from the histogram directly. For the calculation of random jitter, the root mean square (RMS) value is calculated from the distribution function. In [13] and [14], techniques for jitter decomposition using a comparator based-technique have been shown.

The plethora of techniques employed for the measurement can be broadly classified into those that require a clean external clock for sampling and those that do not. Sampling using an external clock can be further classified as those that use over-sampling and those that use the technique of under-sampling. On the other hand, techniques without the use of an external clock are termed as self-referenced jitter measurement. Fig. 3.1 shows the classification of jitter measurement.

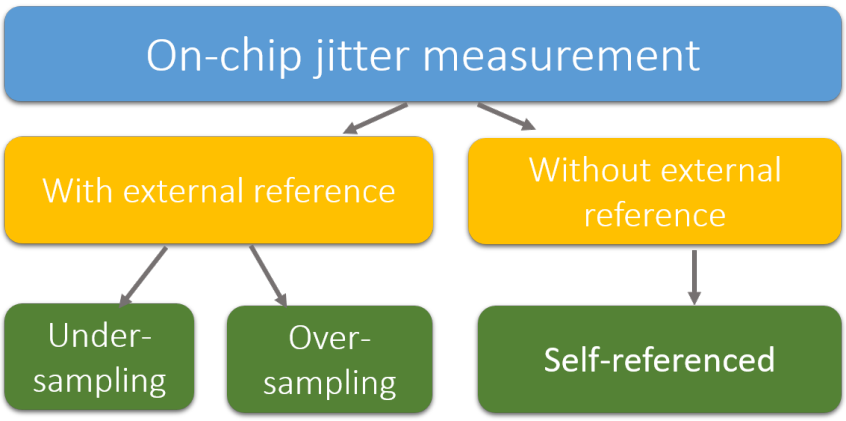


Figure 3.1: Classification of on-chip jitter measurement

In addition to jitter measurement of a clock signal under test with respect to time reference of a jitter-free clock, in a few scenarios jitter in a clock relative to data is also of interest. In [15], jitter injection is used to measure the rms relative jitter between the clock and data at the CDR input with sub-picosecond accuracy in measurements of a 28 Gb/s half-rate digital CDR fabricated in 28 nm CMOS.

Clock jitter can also be measured using an on-chip oscilloscope as demonstrated by [16], where measurement results show sub-picosecond resolution when the input signals consist of a 10-GHz clock signal and a 12.5-Gb/s pseudo-random binary sequence.

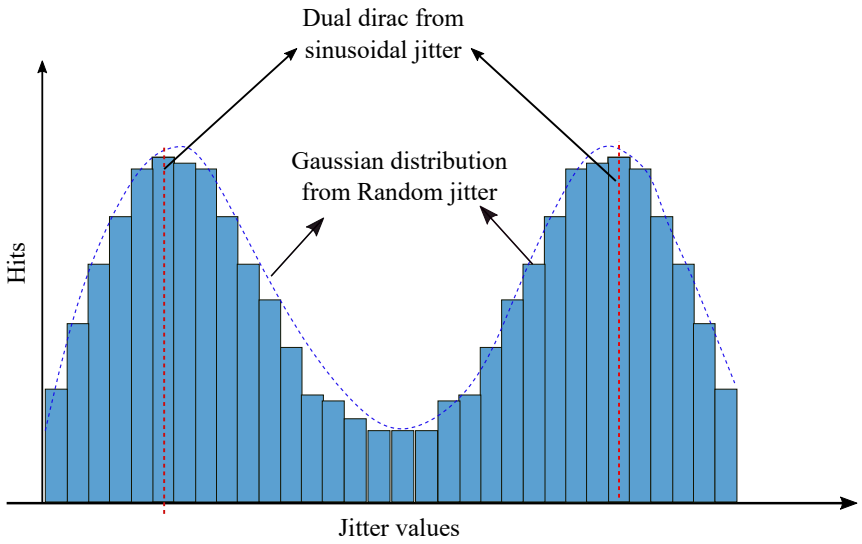


Figure 3.2: Histogram of composite jitter

3.2 Jitter measurement with an external clock

3.2.1 On-chip jitter measurement using sub-sampling

This technique of on-chip jitter measurement uses a clean external reference clock to coherently under-sample the clock signal of interest. Fig. 3.3 shows the concept of sub-sampling. A reference clock of frequency f_{ref} (period T_{ref}) under-samples the observed clock signal of frequency f_{obs} (period T_{obs}), with f_{ref} being slightly lower than f_{obs}. The jitter in the external clock must be negligible with respect to the jitter in the signal under measurement. If this is not the case, the jitter of the reference and measured clocks will be convoluted.

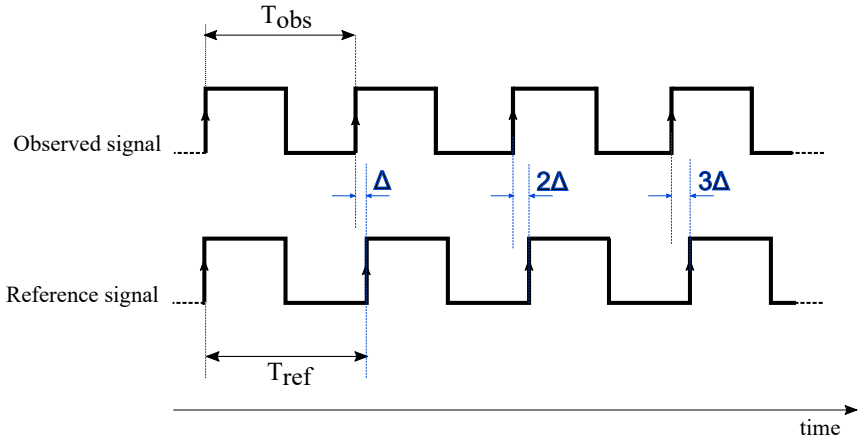


Figure 3.3: Principle of sub-sampling [3]

The time difference between the periods of both signals differ by Δ, which is also the resolution of the measurement. As a result of the time difference Δ, the rising edges of both signals slide in time by a value Δ with respect to each other during each clock period, as illustrated in Fig. 3.3. Initially, both rising edges are aligned, but their phase difference increases by a value Δ after each clock period. A coherent frequency is built when the two clock signals are re-synchronized. This results in a beat signal, shown in Fig. 3.4, which has a time period given by:

$$T_beat = \frac{1}{f_beat} = \frac{1}{f_{obs} - f_{ref}} = \frac{T_{ref} * T_{obs}}{\Delta} \tag{3.1}$$

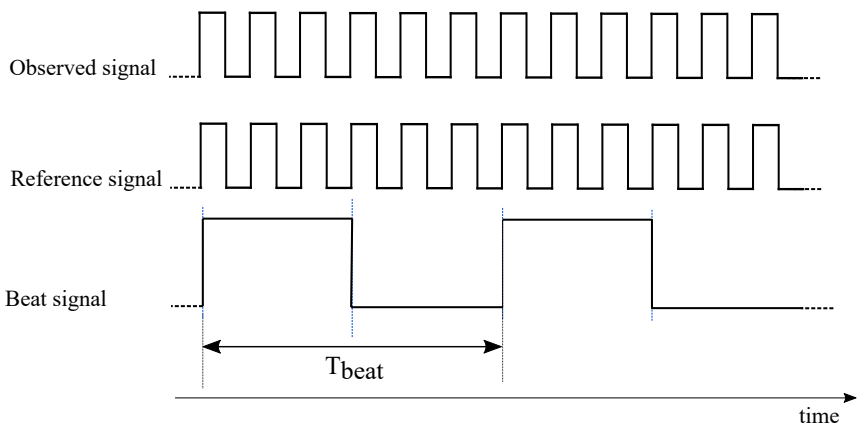


Figure 3.4: Jitter free beat signal

In the case when jitter is present in the clock signal under measurement, there are unstable edges in the beat signal, as shown in Fig. 3.5.

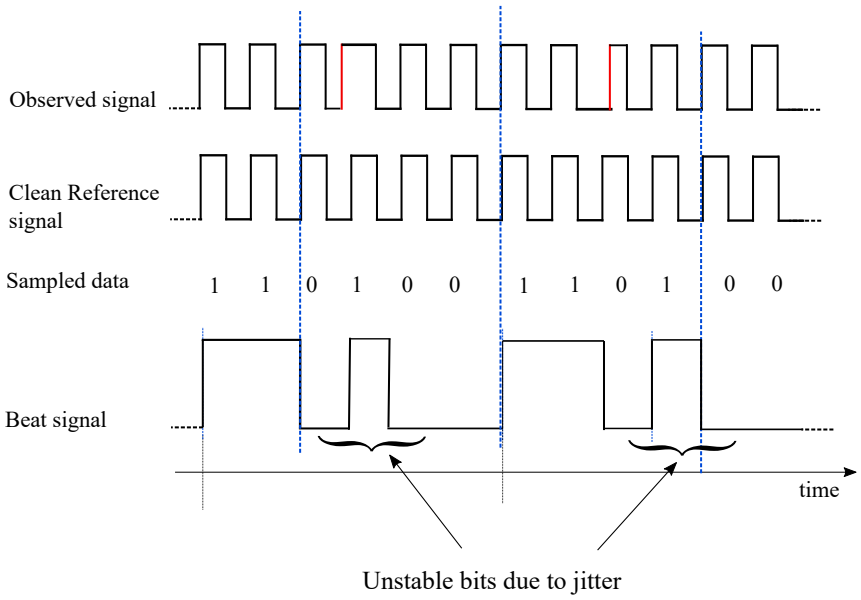


Figure 3.5: Beat signal with unstable bits due to jitter

The technique of sub-sampling is also sometimes referred to as under-sampling, and [4] shows this technique for measuring jitter for a 3 Gbps SERDES IC. An analysis of these unstable edges can be used to measure the jitter content in the signal. [4] shows that samples of unstable bits in the sub-sampled clock can be captured to generate a histogram, which could be used to estimate jitter. By adding many groups of the unstable bits, each group comprising between zero and 100 unstable bits, an accurate cumulative distribution function (CDF) can be derived. To add the bits for the CDF, the groups can be aligned according to their timing relative to a constant beat period edge, or their timing relative to each group's median as shown in Fig. 3.6 . The work in [17] shows that high frequency jitter can be measured by analyzing the unstable bits relative to the median edge of each transition region. With this technique, the work demonstrates measurement of jitter and phase shifts hardware results with near-picosecond repeatability in tens of milliseconds, including generation of jitter histograms and comparison of RMS values to test limits using an off-the-shelf SerDes at 3.1 Gbps. In [18], an ULTRA (UnLimited Time-Resolution Analysis) module demonstrates that a SerDes undersampling DFT technique can be adapted to test multiple PLLs and DLLs for jitter, output frequency, duty cycle, and other parameters. The frequency range of measurement is in multi-GHz range, and it has a sub-picosecond jitter noise floor, and minimal

silicon and needs no calibration or analog circuitry.

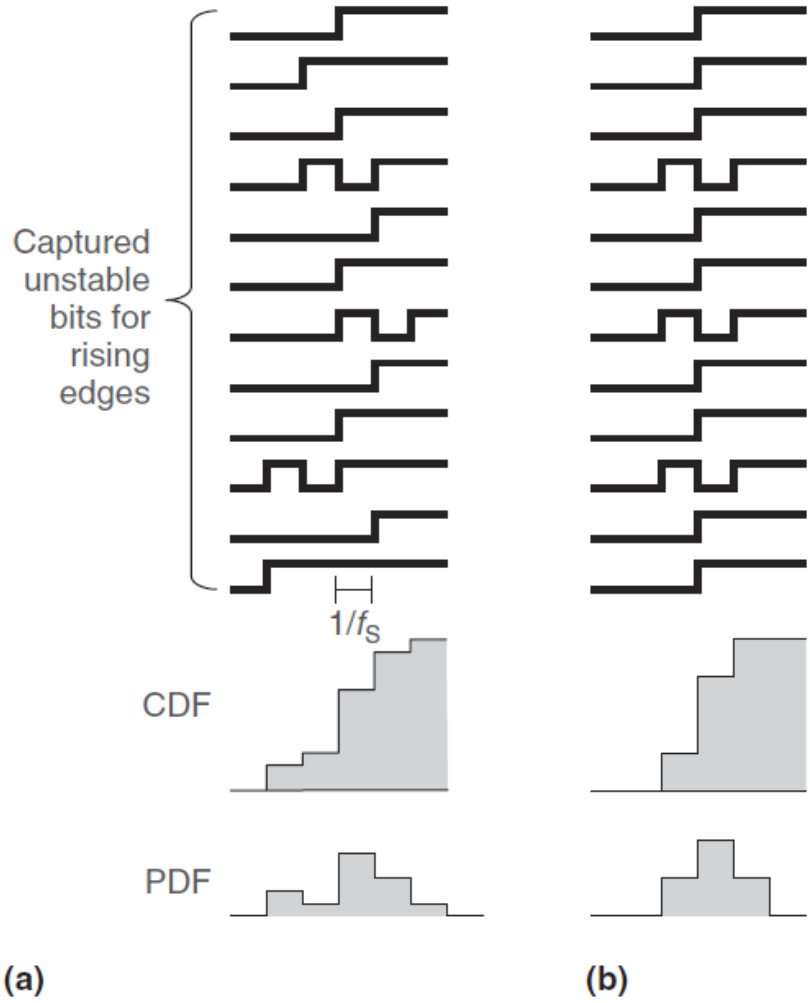


Figure 3.6: Grouping of unstable bits: period aligned (a) and median aligned (b), each with a derived cumulative distribution function (CDF) and probability distribution function (PDF, or histogram). [4]

Jitter computation can also be carried out without the analysis of the PDF/CDF. The number of such transitions has been shown to be directly proportional to high frequency jitter content in the signal [3]. The work presents an Embedded Test Instrument (ETI) and has introduced a theoretical model that describes the ETI transfer function. The unwanted transitions (unstable bits shown in Fig. 3.5) observed during a given window of time has been described as a function of the input high frequency. The transfer function has been derived by a Monte-Carlo simulation, and the high frequency jitter is expressed as

$$\sigma_m = 0.6253.\Delta.\overline{N_{tr}} \tag{3.2}$$

where $\overline{N_{tr}}$ represents the number of measured transitions and σ_m is the RMS value of the input high frequency jitter. The ETI architecture is as shown in Fig. 3.7, where the jitter detection unit provides two outputs: $\#T_r$, which is the total number of bit transitions and the unstable bits due to jitter have been filtered to provide the mean transitions of the beat signal represented by BEC (Beat Edge Count). The work shown in [3] measures high-frequency jitter with sub-picosecond resolution for frequencies less than 1 GHz using the technique of sub-sampling.

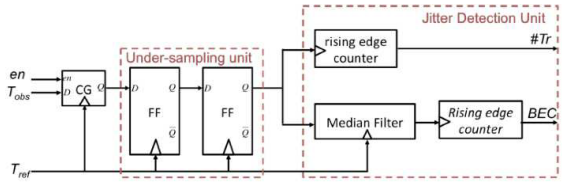


Figure 3.7: Basic architecture of the ETI in [3]

Further study using this approach for estimating jitter has been carried out in collaboration with STMicroelectronics to explore the feasibility of measuring low frequency jitter. A Matlab model was developed and the test bench included the blocks shown in Fig. 3.8.

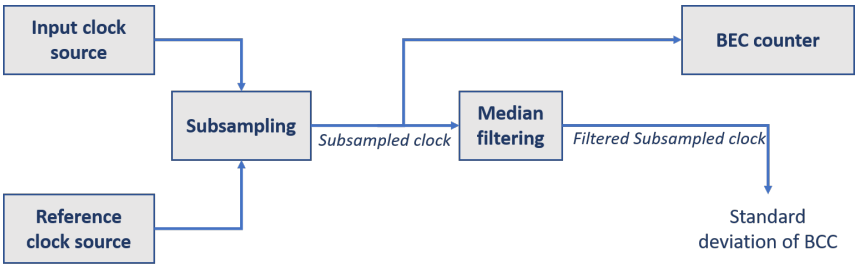


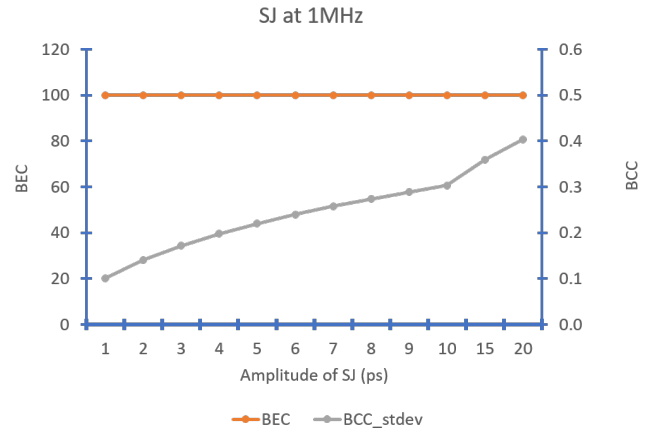
Figure 3.8: Matlab test bench to study jitter estimation using sub-sampling

The number of unstable bits/transitions is denoted by BEC (Beat Edge Count). The number of reference clock cycles that occur in one nominal beat period is represented as Beat Clock-ref Count (BCC). BCC is related to the nominal beat period T_{beat} and reference clock T_{ref} by the following equation:

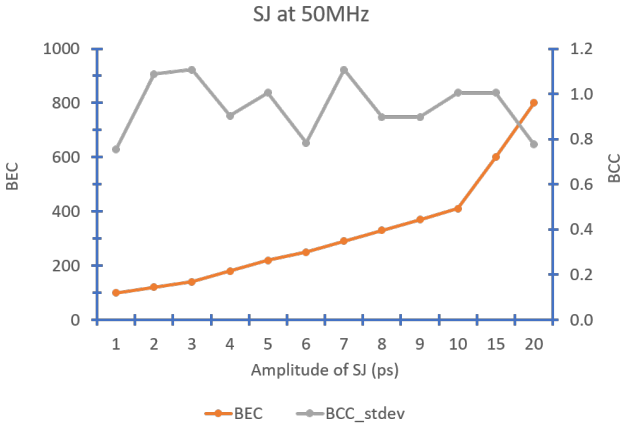
$$BCC = \frac{T_{beat}}{T_{ref}} \tag{3.3}$$

A sinusoidal jitter was introduced to the input clock source running at 500 MHz. Three frequencies of sinusoidal jitter (SJ) have been considered at 1 MHz, 50 MHz and 100 MHz. This is to analyze the impact of a slow-moving sinusoid (1 MHz) and sinusoid at $1/10$th of the clock frequency (50MHz). In the presence of SJ, duration of beat period varies from one beat cycle to the next. This variation can be captured by counting the number of reference clock cycles within each beat period. Standard deviation of this BCC count has been observed to estimate SJ. For SJ at 1MHz, standard deviation of BCC increases with the amplitude of jitter introduced to the clock, as seen in Fig. 3.9. For SJ at 1 MHz, standard deviation of BCC increases with the amplitude of jitter introduced to the clock, as seen in Fig. 3.9(a). The beat edge count is constant across all amplitudes of SJ. At 50 MHz and 100 MHz, standard deviation of BCC no longer increases proportionately with the amplitude of jitter introduced to the clock, as seen in Fig. 3.9(b) and (c). The beat edge count, increases with amplitude of SJ. The curves of BEC and BCC do not show any dependency on the SJ amplitude or frequency and hence it will not estimate the SJ component of the clock signal.

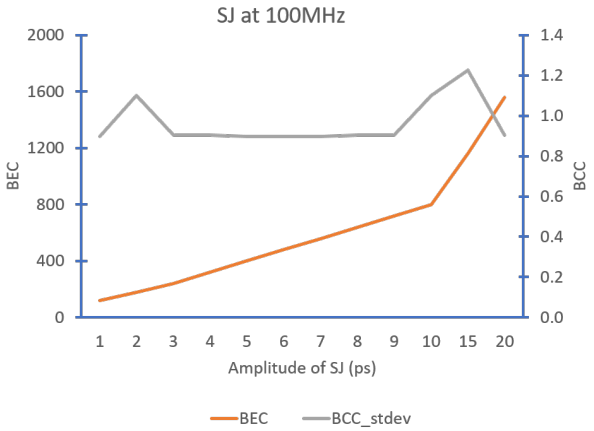
[19] also uses the technique of sub-sampling to measure absolute and period jitter with a sub-picosecond resolution for frequencies up to 6 GHz. The proposed jitter-measurement circuit uses a slow voltage controlled oscillator (VCO) that is designed such that its edges arrive at arbitrary times relative to the edges of the clock signal under test and an external reference. The probability density function (PDF) of the VCO edges is made to be approximately uniformly distributed along one period of the clock signals. By using the slow noisy VCO which acts as a random sampler, the data is undersampled. The advantage of this technique is that the resulting circuitry is quite simple with the addition of a low power VCO. The second advantage is that, apart from the latch,



(a)



(b)



(c)

Figure 3.9: BCC and BEC plots for SJ

all the circuit blocks including the counters are low frequency circuits. Hence, jitter measurement of very high speed clocks is possible.

Thus the technique of under-sampling in general lends itself to very minimal circuitry comprising of few latches for sampling and additional digital circuitry for processing the data for jitter measurement. On the other hand, the requirement of a clean reference clock for making the measurement itself leads to a disadvantage of this technique. Generation of a clean, jitter-free reference signal is a requirement for measuring jitter with high accuracy and this in turn requires complex circuitry.

3.2.2 On-chip jitter measurement using over-sampling

The previous section describes the measurement of jitter on-chip by sub-sampling the clock of interest. The alternate technique is to achieve the same using over-sampling. This requires sampling the clock of interest at a rate higher than its frequency. Such a measurement offers advantages in terms of reduction in the noise spectral power intensity because of over-sampling. The implementation proposed in [5] shows jitter measurement using interpolated jitter oversampling and has been used with a feed-forward measurement technique. The timing diagram that describes the concept of over-sampling is shown in Fig. 3.10. The figure shows the jitter spectrum with the noise intensity P_N reduced to $P_N/4$ when over-sampled at twice the frequency. It makes use of coarse and fine Vernier delay lines to achieve a 1 *ps* resolution of jitter measurement.

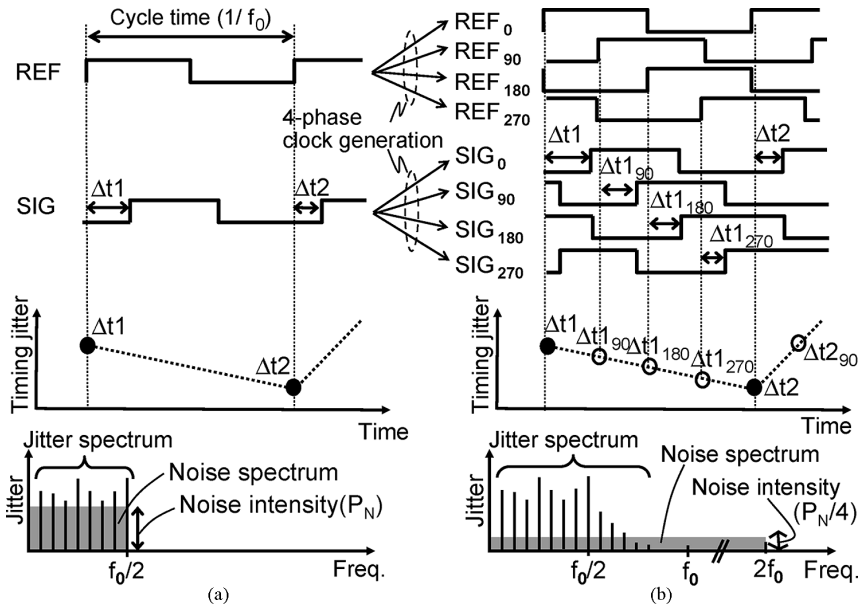


Figure 3.10: Timing diagram and power spectrum for jitter measurement. (a) Conventional jitter measurement. (b) Interpolated jitter oversampling [5]

3.3 On-chip jitter measurement using self-referenced technique

Jitter measurement techniques without the need of an external reference clock have been generally termed as 'self-referenced' technique. A delayed version of the clock is used for sampling the clock of interest. It is to be noted here that the procedure of estimation results in the measurement of N-period jitter.

Fig. 3.11 shows the principle of the self-referenced technique. Here the clock Signal Under Test (SUT) is denoted by S. This clock is delayed by integral number of time periods to generate the delayed version of SUT which acts as the sampling clock S'. The diagram shown in Fig. 3.11(b) explains the process of sampling the SUT with its delayed version. The process of measurement captures high-frequency jitter content, which is typically random-jitter. Hence the PDF of edge 'B' in the diagram has been denoted by the bell-curve. In the presence of jitter, the edges deviate from their ideal time instants and the area in the vicinity of the expected clock edge can be divided into multiple sections called as 'bins' denoted by red solid lines in Fig. 3.11 (b). The probability that the rising clock edge of the delayed SUT leads or lags the corresponding clock edge of SUT gives rise to the probability distribution. Fig. 3.12 shows the Cumulative Distribution Function (CDF) of the case where clock edge 'B' leads clock edge 'A'. The CDF curve of (B leads A) is superimposed on the Probability Distribution Function (PDF) of clock edge B. The probability that edge B leads or lags the clock edge A depends on the jitter content of the SUT. In this diagram the nominal time period of the SUT is denoted as 'T'. Since the time period of the clock varies because of jitter, a nominal value is used by calculating the average time period over many clock cycles. As the probability of the rising edge B (denoted by the PDF of B) increases, the probability that B leads A also increases. The maximum probability of rising edge, which is 0.5 occurs at the time instant of 'T'. Thereafter, as the PDF of edge B goes towards 0, the cumulative distribution of B leads A moves towards the theoretical maximum of 1.

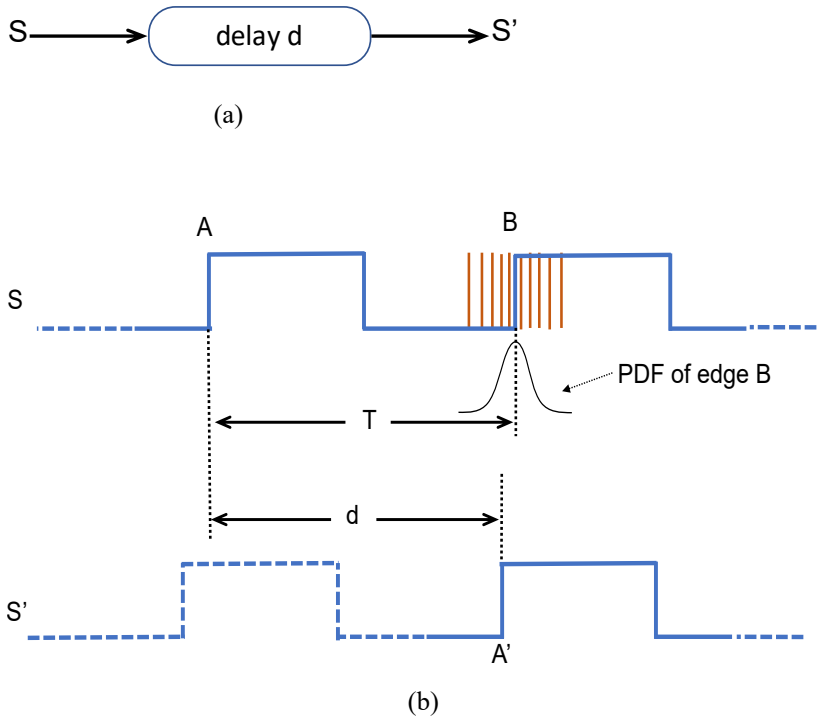


Figure 3.11: Self-referenced technique [6]

Many contributions towards on-chip measurement using self-referenced technique have been made over the years. One of the early works in [20] shows the measurement of period jitter using the self-referenced technique. The basic principle of sampling the SUT by its delayed version has been used. As can be observed from Fig. 3.12, the probability of the edge B leading or lagging is a function of both the delay 'd' and the jitter content of the signal. The idea is to measure the probabilities for two unique values of delay and compute RMS of period jitter. Fig. 3.13 shows the proposed idea of [20] for jitter measurement. Here, p_1 and p_2 are the two probabilities on the CDF corresponding to two delays d_1 and d_2 respectively. The corresponding jitter values are j_1

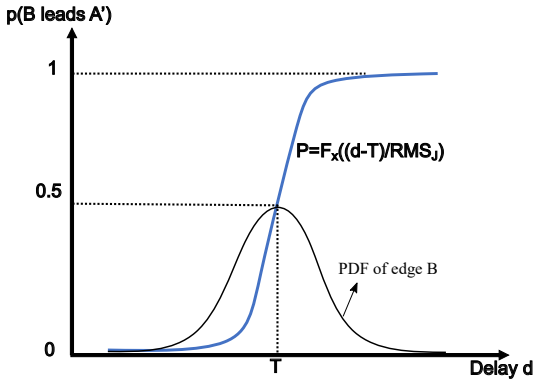


Figure 3.12: Generating CDF using self-referenced technique [6]

and j_2. These jitter values from the CDF are related to the delay 'd' such that

$$j_i = d_i - T \tag{3.4}$$

where T is the nominal time period of the clock under test. If $F_X(x)$ is the normalized Gaussian CDF, then the measurement is done in the following two steps [20]:

1. Solve for x_1 and x_2 that satisfy $F_X(x_1) = p_1$ and $F_X(x_2) = p_2$

2. Since the difference between the jitter values is equal to the difference in delay values according to (3.4), $\Delta j = \Delta d$.

   Therefore the RMS value of period jitter can be calculated as $RMS_J = \frac{\Delta d}{x_1 - x_2}$

The values of j_1 and j_2 are chosen based on the expected RMS jitter value. This choice of jitter values also determines measurement accuracy possible from the calculations. The advantage of this method is that the entire CDF curve need not be generated, but two values of jitter are sufficient. Thus, the required test circuitry would be simple. Spice simulation results reported in [20] show less than 5% error for RMS jitters ranging from 40 to 60 ps. [6] reports an infrastructure IP core to facilitate on-chip clock jitter measurement using self-referenced technique.

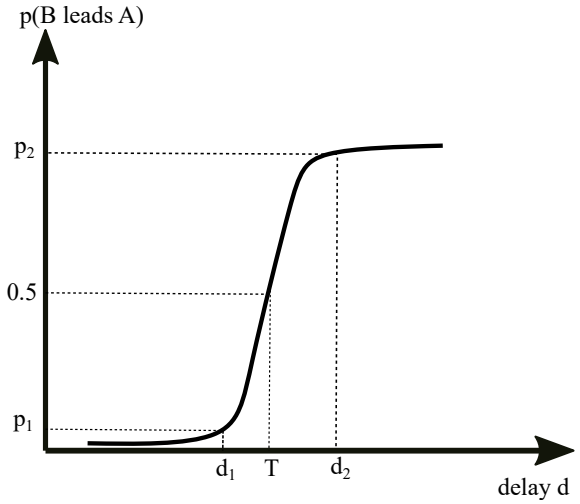


Figure 3.13: RMS jitter measurement using self-referenced technique

3.3.1 On-chip jitter measurement using delay lines

The work proposed in [7] makes use of delay lines for the measurement of jitter with resolution better than 0.4 ps rms. They have implemented a circuit in a $0.13\mu m$, $1.2V$, CMOS technology, with a very compact circuit, occupying $3200\mu m^2$. The measurement circuitry operates up to 2.5 GHz in the used technology. A delay chain implemented by a series of inverters has been used as shown in Fig. 3.14. The variable delay chain is calibrated by converting the chain to a ring oscillator. The delay of the inverters is controlled with separate externally controlled supply voltage. The resolution of delay elements will depend on the minimum delay change that can be implemented using the external supply voltage.

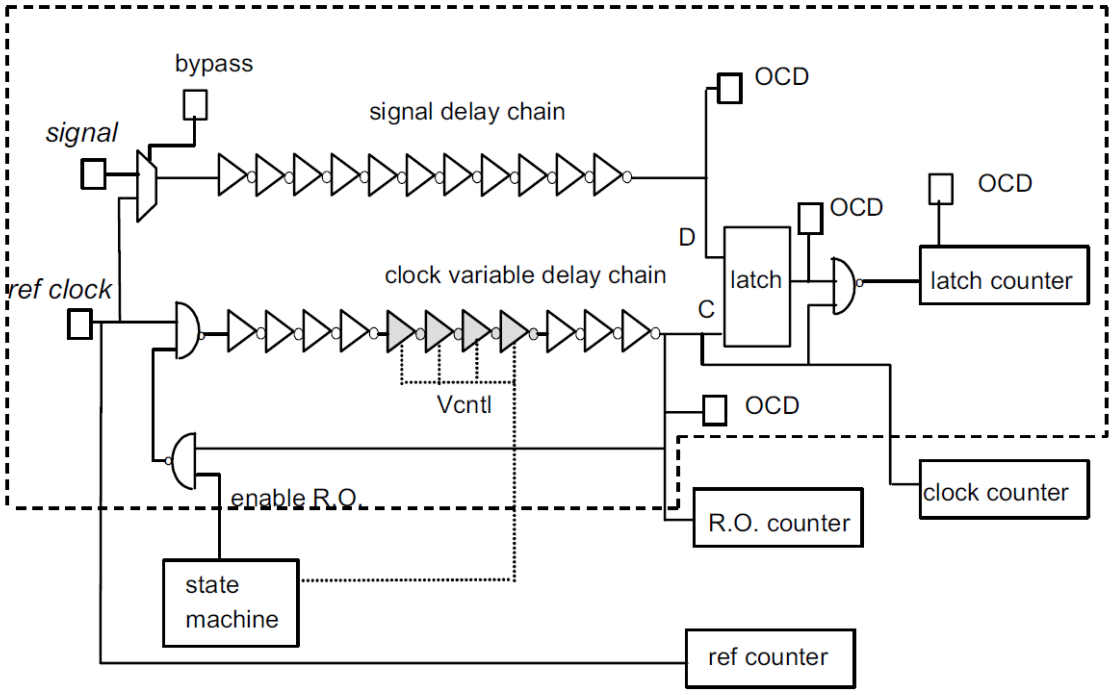


Figure 3.14: Block diagram for jitter measurement [7]

A digital jitter measurement instrument using delay lines has been proposed in [21], where a time resolution of 5.5 *ps* has been achieved in a 28 *nm* technology at frequency of 1.06 *GHz*. They have proposed an on-chip auto calibration for resilience against variation in Process, Voltage and Temperature.

3.3.2 Self-referenced technique using a combination of delay lines and a TDA

The self-referenced technique of measurement has also been used in the work mentioned in [8], where a cascaded Time Difference Amplifier (TDA) has been used to achieve a time resolution of 31 fs for frequency at 820 MHz. They have designed and fabricated test chips using 65 nm and 40 nm CMOS technologies. Time resolution of 2.8 ps has been achieved without TDA at 3.36 GHz in 65 nm and up to 820 MHz in 40 nm. The areas occupied by the circuits are $1350\mu m^2$ (with TDA, 65 nm), $490\mu m^2$ (without TDA, 65 nm), $470\mu m^2$ (with TDA, 40 nm), and $112\mu m^2$ (without TDA, 40 nm). Fig. 3.15 shows the a diagram depicting the measuring circuitry using TDA. Here, the SUT and its delayed version generated by the nT-delay elements pass through a TDA, and then through variable delay elements controlled by a digital word. Latches are used for sampling and the counter output is used to build the CDF. A unique digital word needs to be sent for each of the bins of the histogram.

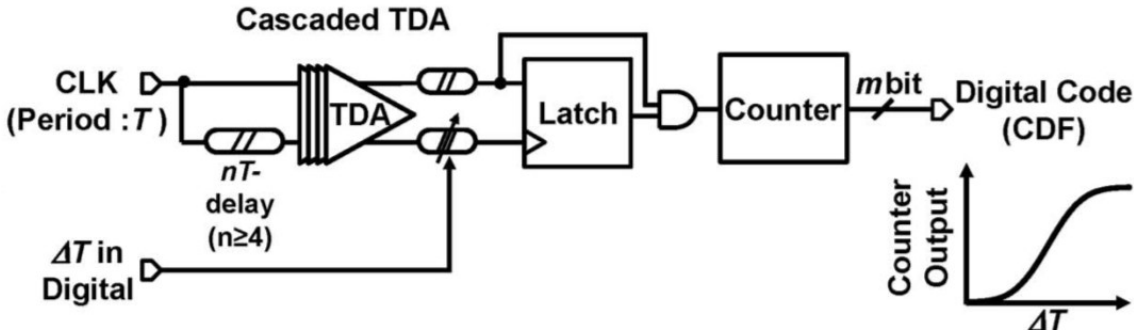


Figure 3.15: Timing jitter measurement using TDA [8]

It is important to note that [22] has shown that it is possible to extract a good estimate of timing jitter, which is often also referred to as absolute jitter [1], from the self-referenced N-period measurement. The calculations for extracting jitter from the N-period measurement has been described in detail in Section 4.2.1

3.4 Proposed random jitter BIST measurement using self-referenced technique

3.4.1 Generic measurement procedure using self-referenced technique

The procedure for measurement using self-referenced technique compares the phases of adjacent clock edges between a clock and its delayed version [20] [6]. A general block diagram of self-referenced jitter BIST which achieves this functionality is shown in Fig. 3.16. The jitter BIST consists of an 'N'T delay block, which generates the delayed version of the SUT. A variable delay element that sweeps the delay across the CDF is shown, and requires precise calibration to achieve the required accuracy. followed by a phase comparator and finally a counter for generating the histogram.

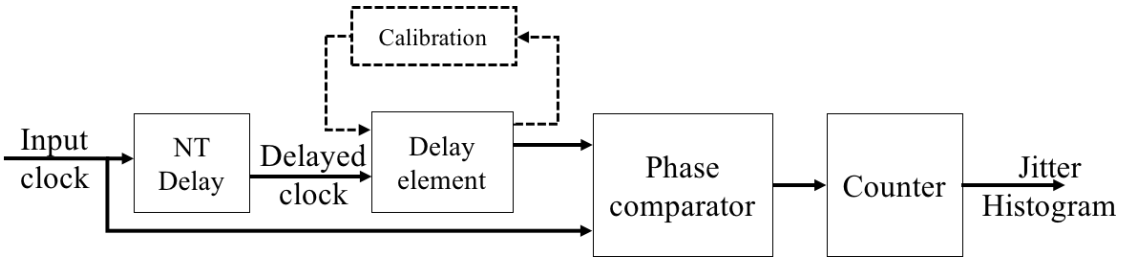


Figure 3.16: Generic block diagram for jitter measurement using self-referenced technique

The NT delay block delays the input clock by an integral N number of time periods T, where T is the nominal time period of the clock. The NT delayed clock, will be hereafter referred to as the sampling clock. The variable delay element allows for sampling the input clock at various instants of time in the vicinity of the expected clock edge. The jitter estimation procedure now follows.

The sampling clock is progressively delayed by Δ time with respect to the input clock. The time Δ here refers to the resolution of the jitter estimate. After each Δ delay, the sampling clock samples the input clock. If a rising edge is found, the phase comparator goes high and this hit

increases the counter value. The number of such hits for each Δ value is the probability of having a clock edge at a time Δ away from the expected clock edge. Such probabilities at integer multiples of Δ time away from the expected clock edge are captured by the jitter histogram. Statistical measurements of the jitter can then be obtained from the histogram.

A calibration path is included for estimating the frequency of the input clock signal, and to calibrate the delay of the variable delay elements for the measurement of each histogram bin. The different bins of the histogram are measured sequentially with a calibration step for each histogram bin as has been done in [7] and [8], which is time consuming.

3.4.2 Proposed measurement technique using self-referenced technique

The measurement procedure described in section 3.4.1 requires implementation of precise delay elements, since the resolution of measurement is determined by the minimum value of Δ that can be implemented in a given technology. This delay needs to be robust against variation in process, temperature and voltage. At the same time, the robust delay element should also be implemented using minimal number of transistors to reduce noise contribution by these elements to the overall jitter measurement. Also, the calibration circuitry should allow for accurate delay variation across the bins of the histogram. The entire process of calibration should also take as less time as possible to reduce the total time for testing.

We propose a novel fully integrated architecture for jitter measurement to achieve the required sub-picosecond resolution at GHz frequencies. In this technique, the delay elements are implemented using Vernier cells for better accuracy. A combination of Vernier cells with a Time Difference Amplifier (TDA) has been used to achieve a sub-picosecond resolution.

Vernier delay line

The concept of Vernier delay can be found in the implementation of time to digital converters where Vernier delay has been used to improve resolution [23] [24] [25]. The minimum delay possible in any implementation is the gate delay and this delay also varies with process variations. Hence a Vernier delay line has been proposed, where the absolute delay of the elements does not matter. It is the difference in the delay values of two unique delay elements that implements the value of Δ. Section 4.2.2 gives more details of our implementation of the Vernier Delay Line, but the basic idea of a Vernier cell is given in Fig. 3.17. To implement an additional delay between the signals A and B, we pass each of the signals through a delay element which provides a delay of τ_A and τ_B, respectively. The delay between the rising clock edges at the output signals A_o and B_o will be the delay at the input increased by $(\tau_A - \tau_B)$. Hence the added delay depends on the difference between two delay cells and not the absolute delay of a delay element. By carefully choosing the individual values of τ_A and τ_B, a very low value for Δ can be achieved. Since the minimum value for Δ does not depend on device geometry, implementation at the transistor level gets simplified. In addition, any variation in the individual delays of the Vernier cells because of process or temperature gets cancelled out since this variation will occur in both the individual elements. By taking care to place the delay cells close-by in the layout, any process variation will impact both the cells in the same direction. Hence the Vernier delay will be robust to such variations except for mismatch deviations that need to be accounted for.

The proposed implementation consists of a Vernier Delay line (VDL) formed by a cascade of Vernier cells of the type shown in Fig. 3.17. We have chosen a Vernier delay line with 25 elements to build an histogram that will thus have 25 bins. This approach greatly simplifies the calibration procedure since a one-shot calibration is sufficient for the entire histogram. The output of each Vernier delay cell in the delay line is required for the measurement of a different bin in the histogram. By connecting the cascade of Vernier cells in the form of a ring oscillator, they are all tuned at the same time to the required value of resolution. The proposed calibration procedure requires only two calibration cycles, one for each delay line in the VDL, and the calibrated Vernier

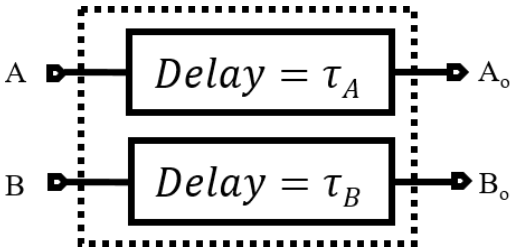


Figure 3.17: Block diagram of Vernier delay cell

cells can then be used to build a histogram of 25 bins. The bin number chosen is a trade-off between hardware area and the measurement accuracy. The higher the number of bins, the more accurate will be the computed values from the generated histogram. At the same time, in the proposed implementation, the higher the number of bins, the longer will be the cascade of Vernier cells, which increases the occupied area. Complexity also arises with more Vernier cells as the length of the cascade increases. Mismatch between the devices cause the individual Vernier delays in the delay line to vary with respect to each other. Higher the number of elements in the cascade, the accumulated error due to mismatch at the end of the Vernier delay line also increases. Hence a nominal value for the number of bins which is determined by the number of Vernier cells in the Vernier delay line has been chosen.

Time Difference Amplifier

The implementation of delay elements described above still suffers from mismatch between elements. Any variation in the individual delays of the elements will not allow all the bins in the resulting histogram to be of uniform width. In order to achieve sub-picosecond resolution, Vernier delay cells which achieve a Vernier delay smaller than 1 ps and with a precision in the femtosecond range have to be implemented. Such small delays are very difficult to implement under process variations and mismatch. At the same time, the lower the value of the Vernier delay, the higher is the resolution of the measurement. To navigate this trade-off, a Time Difference Amplifier (TDA) has been used in combination with the Vernier Delay Line as has been done in [26]. Fig. 3.18 shows the block diagram with the input and output waveforms of the TDA illustrated.

The time difference between the corresponding rising edges of two signals A and B gets amplified by the gain of the TDA as shown in Fig. 3.18(b). Hence the input time difference of ΔT gets amplified to a value of $\Delta T x Gain_{TDA}$. We propose the use of the TDA at the input of the Vernier delay cell explained in section 3.4.2. This helps to reduce the minimum delay value that needs to be implemented by the Vernier cell. Hence the width of each of the bins of the histogram gets expanded by a factor equal to the gain of the TDA. Since the specifications of the delay elements are now relaxed by the use of the TDA, the implemented circuitry is now more robust to variations because of mismatch and process variations.

A block-diagram of the proposed technique for the test prototype

The VDL and the TDA described in the previous sections have been included in the proposed test instrument. Hence the generic block diagram shown in Fig. 3.16 can be modified as shown in Fig. 7.1. The SUT and its delayed version now first pass through a TDA, where the input time difference between its rising edges are amplified by a factor of its gain. The output of the TDA passes through 25 elements in the VDL. For each Vernier cell in the VDL, a phase comparator is used to detect the presence of a rising clock edge for the corresponding bin. When the delayed clock samples a rising edge on the SUT, a 'hit' is counted by the counter at the output of the phase comparator. Thus the implemented time width of each bin of the histogram is not Δ as described in section 3.4.1, but it is amplified by the gain of the TDA and hence the new bin width will be

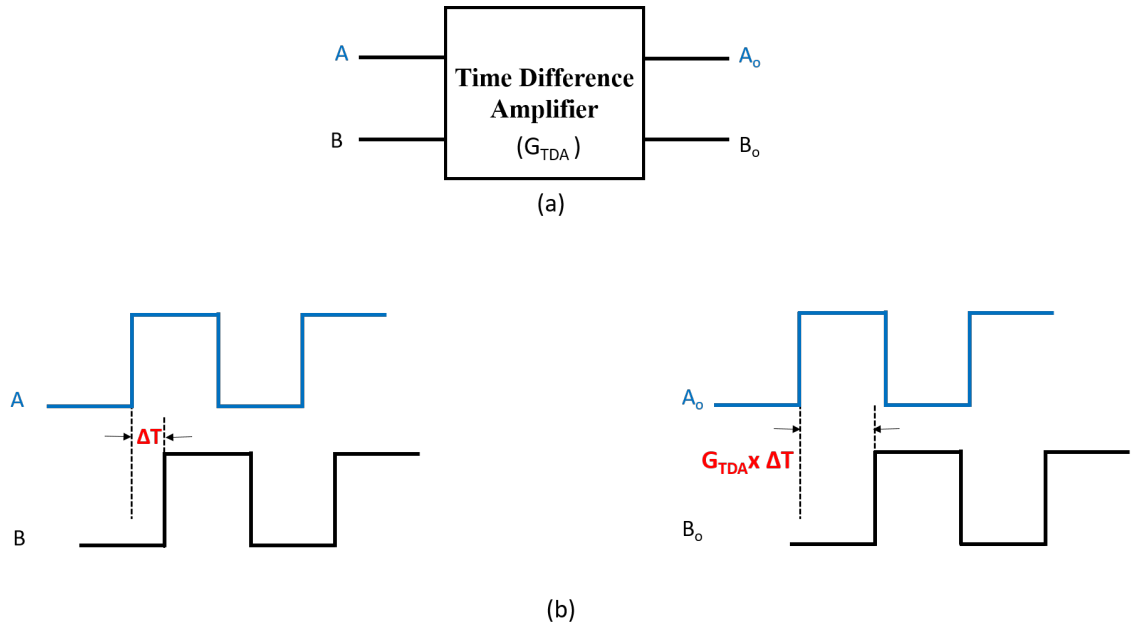


Figure 3.18: Time Difference Amplifier (a) Block diagram (b) waveforms for illustration

(Delay of Vernier Cell) x (Gain of TDA). This relaxes the constraints placed on the design of the delay elements without compromising on the resolution of measurement. The effective resolution from the resulting histogram will still be given by Δ.

The process of histogram generation using the described method can be summarized in Fig. 3.20. Here, the SUT is sampled by the delayed version of itself referred to as 'Sampling clock' in the diagram. The demarcations shown on the CDF curve show the 25 sections from S_1 to S_{25}, which correspond to the 25 Vernier delay cells. However, the width of each bin during the implementation is now $Gain_{TDA}x\Delta$. After the SUT and the sampling clock pass through the TDA, these signals pass through the cascade of 25 Vernier delay cells. The time delay between the SUT and sampling clock (after TDA) increases linearly by a value equal to $Gain_TDAx\Delta$ as they pass through the VDL from left to right. The output of each cell in the VDL is tapped one at a time to detect the presence of a rising edge and thus to accumulate the hits for each bin. The hits for each bit are accumulated in the counter which is readout before starting the counting for the next bin. The histogram obtained this way produces directly the CDF curve.

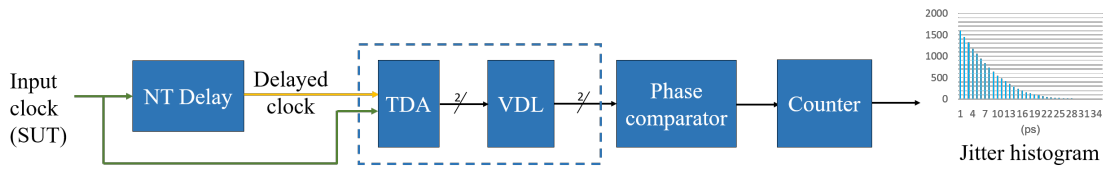


Figure 3.19: Block diagram for the proposed test instrument

3.4.3 Improvements with respect to state of the art

The proposed instrument in section 3.4.2 offers the following improvements over the state of the art:

1. The use of a Vernier delay line for implementing the variable delay required in the self-referenced architecture allows for a single calibration cycle for all the delays required to generate a histogram. In comparison, the delay element in [7] and [8] needs to be calibrated

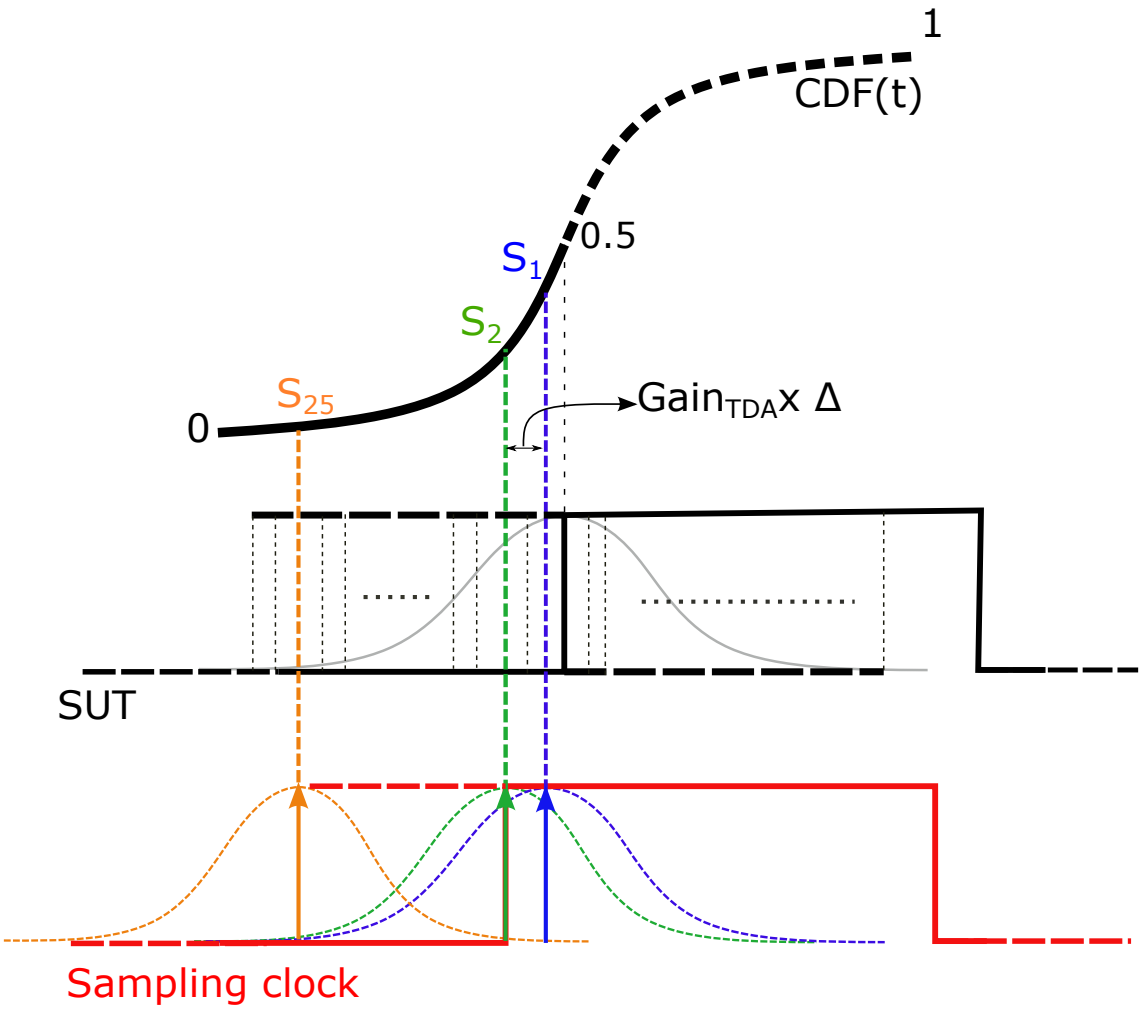


Figure 3.20: Generation of CDF curve

to generate the hits for each bin. By making use of a Vernier Delay Line and the proposed calibration scheme, time required for calibration is saved as it is a one-shot scheme for the entire histogram.

2. The use of highly tunable delay elements by utilizing the coarse and fine tunability of the delay element described in [9] allows a delay sensitivity of 1 ps/mV. This high sensitivity delay elements when used in a Vernier configuration offer the advantage of both robustness and tunability of delay elements. An RO (Ring Oscillator) based calibration proves sufficient for delay calibration. In [7], an external reference clock is required for delay calibration. By utilizing highly tunable delay elements, a simple RO based without the need of an external clock for calibration has been demonstrated.

3. Additionally, the proposed architecture supports a standard digital test interface for ease of programmability of the test instrument.

3.5 Architecture of the instrument

The detailed architecture diagram that implements the proposed idea is shown in Fig. 3.21. The blocks contained in the block diagram given in Fig. 7.1 have been supplemented by additional digital circuitry to support a JTAG interface. The phase comparator block in this diagram contains a phase comparator array connected at the output of each VDL cell, and the outputs of this array are multiplexed to select one of the 25 bins of the histogram. 5 select lines are used to select the appropriate bin number for multiplexing. The 10-bit hit counter at the output of the multiplexer counts the number of hits at the output of a phase comparator. A 10-bit shift-register is connected to the hit counter to store the count value once measurement is completed for each bin of the histogram. A second counter called the 'control counter' of 16 bits is used for the calibration of the delay elements. The connected 16-bit shift register stores the count value of the control counter. A third shift-register of 16 bits has been included to support digital based programmability of the instrument. The operation of the instrument is controlled by two unique digital signals sent from the TAP controller. The START signal is used to signal the start of an operation, as all operations are time bound. The LOAD/SHIFT signal is used to load the counter value onto the shift-register upon completion of the corresponding operation. The 3 shift registers form a scan chain and a single-bit interface termed TDI is used to serially load bits into the scan chain. The TCK is a slow digital clock for clocking the shift registers. After completion of each measurement, the output of each shift register is shifted out serially through the single bit digital interface termed TDO in the diagram. More details about the implementation of each of the blocks in the architecture, including the bit description of the program control shift register is given in 4.

3.6 Conclusion

This chapter presents a study of the state of the art for on-chip measurement of jitter. The two main categories of techniques include self-referenced techniques and those that use an external clean clock for reference. The proposed idea for measurement of random jitter using self-referenced technique has been explained. The next chapter provides details of the transistor level implementation of a test instrument for measuring jitter with a sub-picosecond resolution.

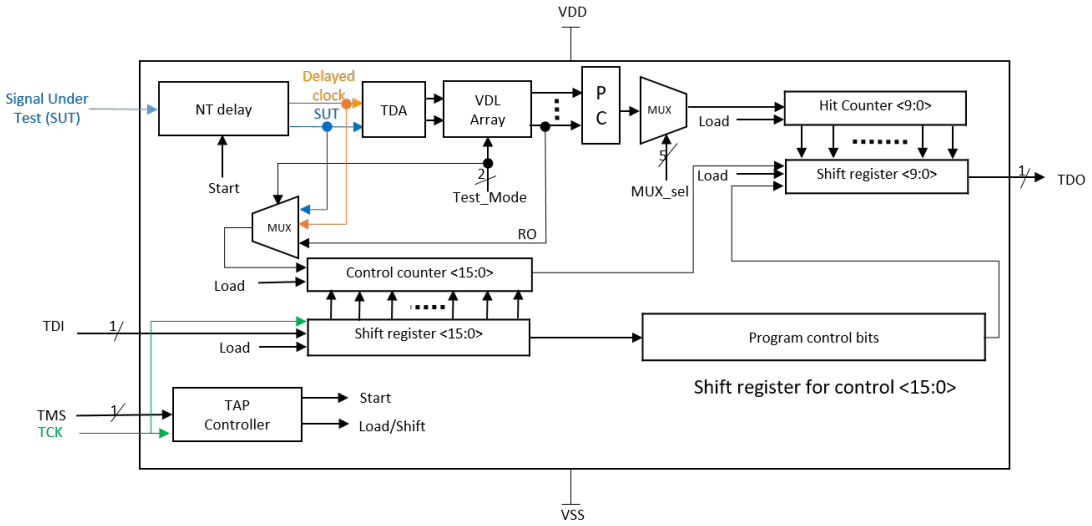


Figure 3.21: Architecture for the proposed test instrument

4

Design of an on-chip clock jitter test instrument

This chapter describes the transistor level implementation of all the blocks of the proposed architecture. The technology used is 28 nm FD-SOI from STMicroelectronics. The instrument consists of delay cells to implement the self-referenced architecture. The time difference amplifier expands the instrument resolution. The interface of the test instrument to the external equipment is supported by digital circuitry. Several additional digital blocks support detection and collection of test data for the generation of a jitter histogram.

Contents

4.1 Delay element

The proposed test instrument aims to measure the random jitter content of a clock signal using the self-referenced technique. This architecture requires delay elements to generate a delayed version of the Signal Under Test (SUT) to generate the sampling clock. The sampling clock is then delayed progressively around the vicinity of the rising edge of the SUT and a histogram is generated which shows the probability of a rising clock edge occurring within a particular bin of the histogram. This operation requires delay elements which can precisely delay the delayed version of the SUT. The lesser the value of the delay that can be implemented, the higher is the resolution of the measurement. In other words, the minimum delay that can be implemented using the delay elements defines the resolution of the instrument. Therefore, the design of the delay elements is at the heart of the instrument design problem.

Designing delay elements which can implement precise delay values also has its own challenges. The minimum delay that can be implemented in a given technology cannot be less than the minimum gate delay. The test instrument has been designed using 28 *nm* FD-SOI from STMicroelectronics. With this technology, the minimum delay that can be implemented has been found to be in tens of picoseconds through electrical simulations. This means that the highest resolution that can be achieved gets limited to tens of picoseconds. The objective of the proposed test instrument is to measure jitter with a sub-picosecond resolution. Furthermore, this delay can vary with process, temperature and voltage. The implication of this variation is that the bin widths of the generated histogram will not be uniform and hence the calculated jitter from the histogram will not be accurate.

The test instrument also requires delay elements to generate the delayed version of the SUT that acts as the sampling clock. We denote these elements as the NT-delay elements in this document, as the required delay is an integer 'N' multiple of the clock time period T. The jittery clock will have irregular rising and falling edges and hence the time period also varies. The value of T used for implementation purposes is the nominal time period value. As the frequency range targeted by the proposed instrument is in GHz, the time delay required would be in the range of a few nanoseconds. Although such delays are easier to implement in the technology used, the main challenge comes from implementing delay elements that can generate this delay value that is robust against process, voltage and temperature variations. Any deviation of this delay even in the range of picoseconds could lead to the sampling clock going out of the vicinity of the rising clock edge and hence we will not be able to capture any hits in the histogram.

The variation in the delay of elements with process and temperature can be addressed by having a calibration procedure. Once the delay elements have been fabricated, any deviation in the implemented delay because of process related variations could be corrected if there is an on-chip calibration procedure. This requires tunability of delay elements by using external knobs. The minimum tunable delay using the external knob also matters as this helps to achieve a precise tuning. Another advantage of having tunable delay elements is that the bin width of the histogram could be varied as per measurement need. The third advantage of having tunable design elements is that the NT-delay elements could also be tuned to various *'NxT'* values, and hence the instrument can be used to measure jitter for different frequencies.

4.1.1 Design of delay element in 28 nm FD-SOI

A tunable design element that also features coarse and fine tuning has been described in [9]. The delay element is essentially implemented using a current starved inverter as shown in Fig. 4.1. Here the delay between the signals (V_{IN},V_{OUT}) is tuned by varying the bias voltages. We can understand the working as follows: as the gate voltage V_{GP} is increased, the rising edge of V_C takes a longer transition time because by increasing the gate voltage of the PMOS device, the current carrying capacity for the charging current is reduced. Since V_C passes through three inverters,

we observe that the falling edge of V_{OUT} is delayed. The variation because of varying V_{GN} can be described similarly and it affects the rising edge delay at the output V_{OUT}. Additional tuning knobs of the body bias voltages V_{BP} and V_{BN} have been included for fine tuning purposes. The delay between the corresponding rising and falling edges of V_{IN} and V_{OUT} is more sensitive to a change in the gate voltage. Hence to achieve a linear variation in the edge delay with respect to biasing voltage, the body bias voltages have been used. The body bias acts as a back-gate terminal since the device is implemented in *FDSOI* technology. The insulation layer between the channel and the back-gate terminal ensures that the change in the delay because of body bias change is not as drastic as that due to gate voltage variation. The entire operation of the current starved inverter which allows for a linear delay variation is based on reverse body bias. The layout for the current starved inverter which depicts well arrangement with the body biasing stage is shown in Fig. 4.2.

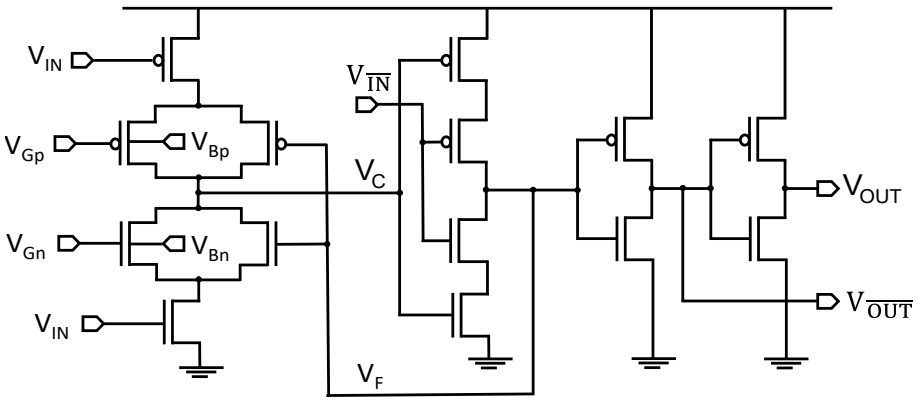


Figure 4.1: Tunable delay element [9]

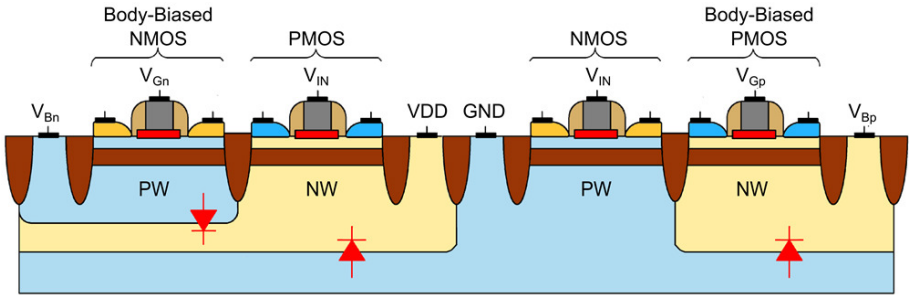


Figure 4.2: Well arrangement layout showing body biasing stage [9]

The three stages of the delay cell can be explained as shown in Fig. 4.3. The first stage is the current starved inverter which has coarse and fine tuning knobs depicted. The coarse and fine tuning of the *rising edge* delay between V_{IN} and V_{OUT} is achieved by varying V_{GN} and V_{BN} respectively. On the other hand, the coarse and fine tuning of the *falling edge* delay between V_{IN} and V_{OUT} is achieved by varying V_{GN} and V_{BN} respectively. The second stage is the gated inverter stage, which generates a feedback signal V_F. This signal V_F prepares for the upcoming switch in the rising to falling and vice-versa and provides a way to overcome short circuit current loss. The third and final stage help to drive the output since by varying the tuning knobs, the transition time during rising edge and falling edge is impacted. If the transition time is very long, the output may not be able to drive the gate of the next device in the chain. The buffer in the third stage formed by two inverters helps to drive the voltage levels to the rail voltage and provide isolation between the current starved inverter and the next stage.

The variation between the delay and body bias voltage has been simulated and plotted in Fig. 4.4. On the y-axis, the rising edge delay between corresponding edges of V_{IN} and V_{OUT} is plotted

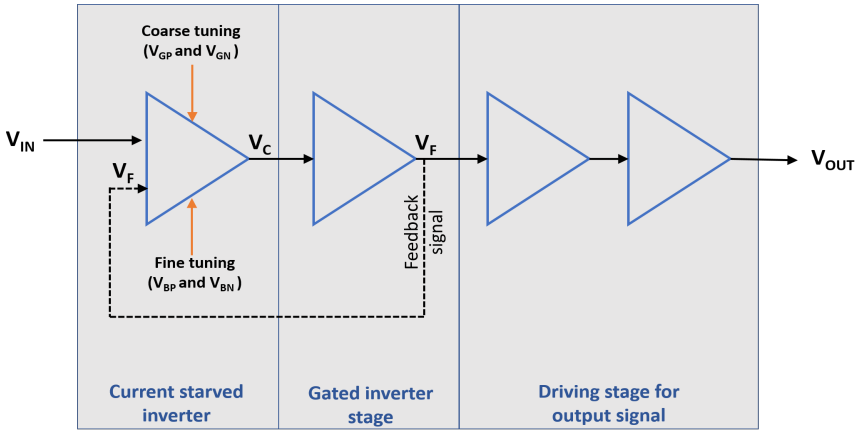


Figure 4.3: Description of delay element

and is denoted as T_d. On the x-axis, the value of V_{BN} is varied between $-3V$ to $+3V$. The device structure in FD-SOI technology permits body bias voltage variation upto $3V$, with the body reverse biased for negative voltages of V_{BN} and forward biased for positive values of V_{BN}. We can observe from the plots that for gate voltage V_{GN} close to the device threshold voltage, the variation in delay with the body bias voltage is exponential. This is because at low V_{GN} the device has just turned on and a small variation in the body bias leads to a huge change in the biasing conditions. As V_{GN} is increased and the device is turned on strongly, the variation in T_d with respect to V_{BN} is almost linear. By identifying the combination of (V_{GN},V_{BN}) for which delay variation is linear, we can implement a highly tunable delay element. The body biasing direction for V_{BP} is the opposite of V_{BN} and has been shown in Fig. 4.5, where *FBB* stands for Forward Body Bias and *RBB* stands for Reverse Body Bias. The direction of interest for the test instrument is the RBB, as the charging and discharging current of the current starved inverter is essentially reduced causing a delay in the falling and rising edges at the output respectively. Hence the combination of gate and body bias voltages provide a linear tunability of the rising and falling edges of the delay element.

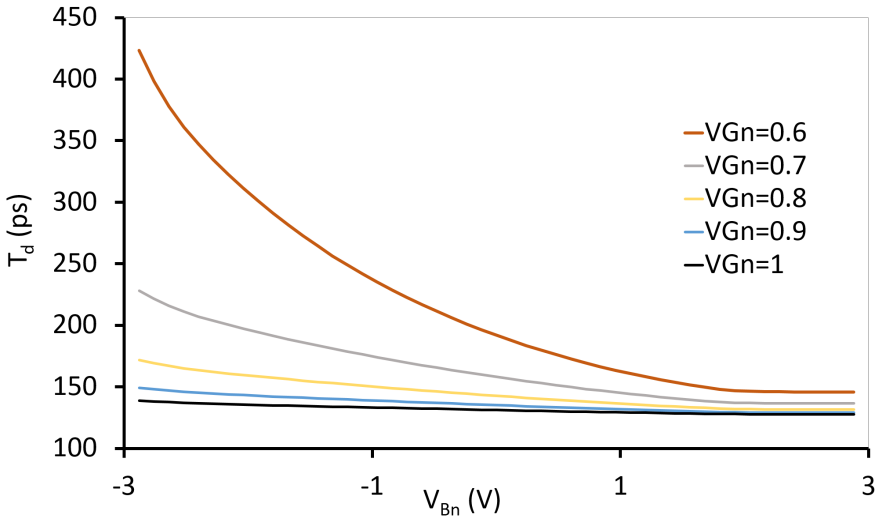


Figure 4.4: Falling edge delay variation with V_{BN} for different values of V_{GN}

The falling edge delay variation by tuning V_{BP} and V_{GP} can be seen in Fig. 4.6. The diagram shows that the delay variation in falling edge is highly sensitive to the gate bias voltage. At certain combinations of gate and body bias voltage the delay variation is linear.

The aim of the architecture is to design an instrument with a very small footprint. Thus the

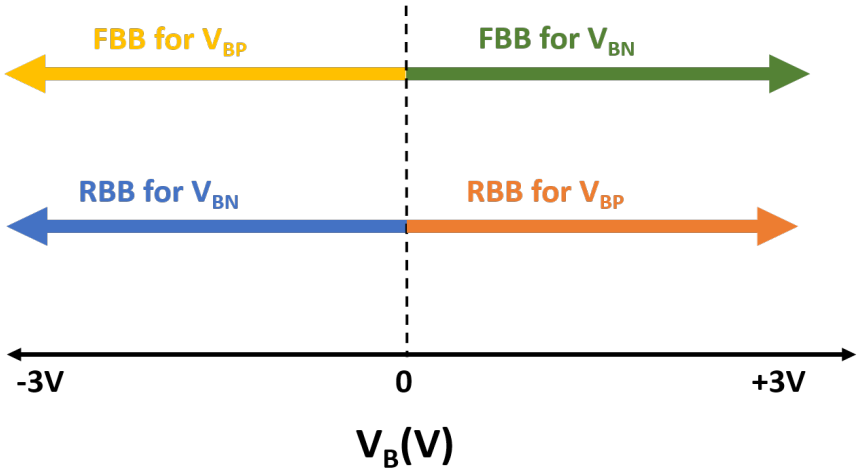


Figure 4.5: Direction of body bias with V_{BN} and V_{BP}

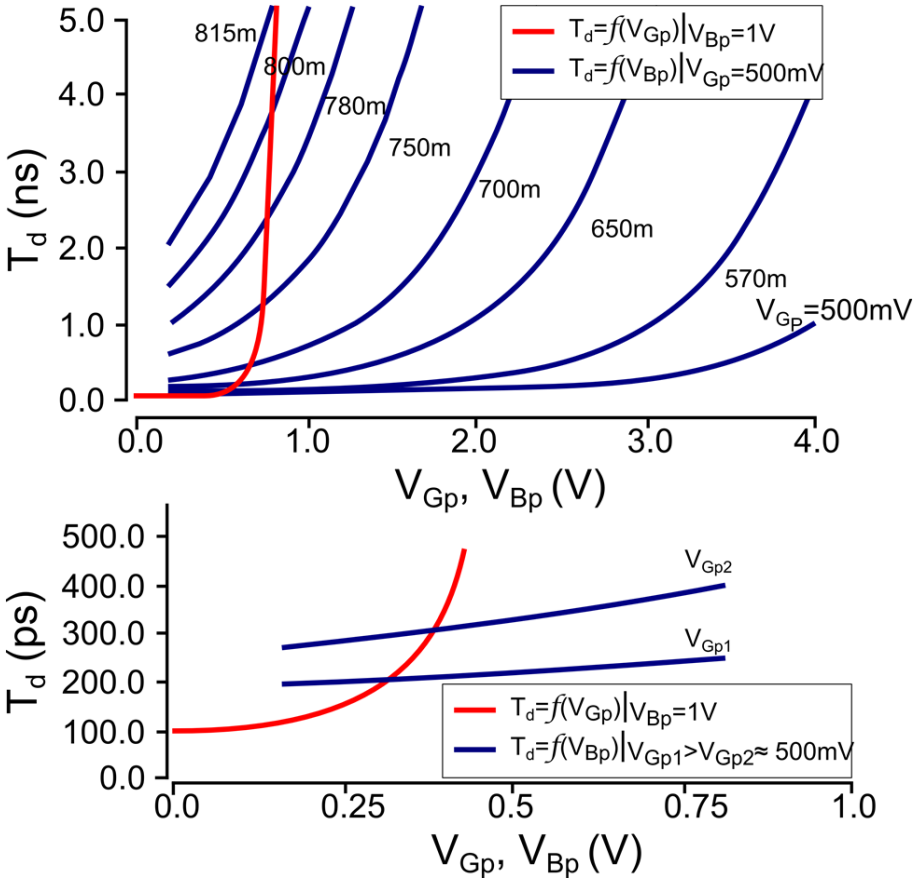


Figure 4.6: Falling edge delay variation with V_{GP} and V_{BP} [9]

sizing of these transistors are also optimized for small footprint and low power consumption. The minimum channel length is used. The widths of the PMOS and the NMOS devices are adjusted to give similar variation in the rising and falling edge delay with respect to the biasing voltage.

4.2 Delay line

4.2.1 NT delay

The proposed architecture uses the delay element described in section 4.1.1 to implement delay lines required to realize the architecture. The first block that has been designed using the delay element described is the NT delay block. This block is the first block that receives the SUT from the external interface.

The NT delay block generates a delayed version of the SUT. The delay is an integral multiple of the time period T of the clock signal. The nominal time period is taken for implementation purposes. The SUT could be delayed by one time period, which leads to the measurement of period jitter [8].

Effective RMS jitter using self-referenced technique

In the general process of measurement of clock jitter, a jittery clock SUT is sampled by a reference clock 'REF'. Let us denote the Root Mean Square (RMS) value of the timing fluctuations that cause jitter in the SUT as $\Delta\phi^{sut}_{RMS}$ and that of the reference clock which will be sampling the SUT as $\Delta\phi^{samp}_{RMS}$. These signals pass through a phase comparator where essentially one of the clocks latches the other to detect the occurrence of a rising edge. Then, as per [8] and [27], we can say that the latching process can be regarded as a random skew measurement. The RMS of timing fluctuations between the SUT and the reference version named as 'SAMP' can also be characterized as random skew. The total RMS of this fluctuation can be calculated as given in (4.1)

$$\sigma_{total} = \sqrt{(\Delta\phi^{sut}_{RMS})^2 + (\Delta\phi^{samp}_{RMS})^2 - 2\rho\Delta\phi^{sut}_{RMS}\Delta\phi^{samp}_{RMS}} \tag{4.1}$$

The correlation coefficient ρ denotes the cross-correlation between the jitter sequences corresponding to SUT and the sampling clock. The value of $|\rho|$ falls between 0 and 1, where 0 denotes no correlation between the jitter sequences of SUT and the sampling clock. In the particular case of self-referenced architecture, this occurs when the jitter is purely random in nature and hence there is no correlation between corresponding edges of the SUT. Therefore the value of cross correlation co-efficient is zero between SUT and the delayed version of itself. But in most cases, there is deterministic jitter also present in addition to random jitter. In cases like these, the jitter sequence of SUT and its delayed version will have correlation since deterministic jitter of periodic nature, commonly called as sinusoidal jitter, will have repetitive values.

Let us look at the effective RMS value for the case of self-referenced architecture where the reference clock is the delayed version of the SUT. Here the value of the correlation co-efficient ρ depends on the value 'T' by which the sampling clock is delayed. For the case $T = 1$, we are comparing the jitter at clock instants of '0' and the adjacent edge 'T', and therefore $\rho \approx 1$ can be assumed. Thus we have from the equation (4.1)

$$\begin{aligned}\sigma_{total} &= \sqrt{(\Delta\phi^{sut}[T])^2 + (\Delta\phi^{sut}[0])^2 - 2\rho\Delta\phi^{sut}[T]\Delta\phi^{sut}[0]} \\ &\approx \sqrt{(\Delta\phi^{sut}[T] - \Delta\phi^{sut}[0])^2},\ \rho \cong 1 \\ &\approx J_{RMS}\end{aligned} \tag{4.2}$$

Here $\overline{\phi}$ represents the average of ϕ. Thus, using the self-referenced technique it is possible to extract period jitter J_{RMS} from the SUT. By setting $N > N_{uncorrelated}$, that is if the delay of the NT block is multiple clock periods such that the SUT and the delayed version can be considerered to be uncorrelated, we have $\rho \approx 0$ [28] [8]. From (4.1), the total RMS timing fluctuation can be calculated as

$$\begin{aligned} \sigma_{total} &= \sqrt{\overline{(\Delta\phi^{sut}[nT])^2 + (\Delta\phi^{sut}[0])^2}} \\ &\approx \sqrt{2}\Delta\phi^{sut}_{RMS},\ \rho \cong 0 \end{aligned} \tag{4.3}$$

This is the proposed method to measure the RMS jitter $\Delta\phi^{sut}_{RMS}$ using the self-referenced technique with the designed test instrument. The equation (4.3) describes that for NT delay of multiple clock periods, the measured RMS value of jitter is multiplied by a factor of $\sqrt{2}$. This can also be explained as follows. The SUT with jitter is delayed by multiple time periods. Assuming that the delay circuitry has minimal jitter, the delayed version of the SUT will have the same jitter profile of the SUT. Specifically in the presence of purely random jitter, jitter values between SUT and delayed version is uncorrelated. Thus by sampling a jittery clock using another jittery clock, the jitter noise is measured twice. Since we are calculating the Root Mean Square of two uncorrelated random variables with the same individual RMS values, the resultant RMS value will be $\sqrt{2}$ times the individual RMS value of $\Delta\phi^{sut}_{RMS}$.

Implementation of NT delay

The delay element described in section 4.1 has been used to implement the NT-delay block. Fig. 4.7 shows a simplified block diagram for the NT delay block, where the cascaded delay elements can be seen. Each 'Delay cell' consists of two cascaded delay elements and they are typically biased to give a total delay of 200 *ps*. That is, each Delay cell shown in Fig. 4.7 gives a typical delay of 200 *ps* and the delay line is made of 15 such delay cells. The delay cells all share the same tuning voltages for biasing and its delay is calibrated using a combination of gate and body bias.

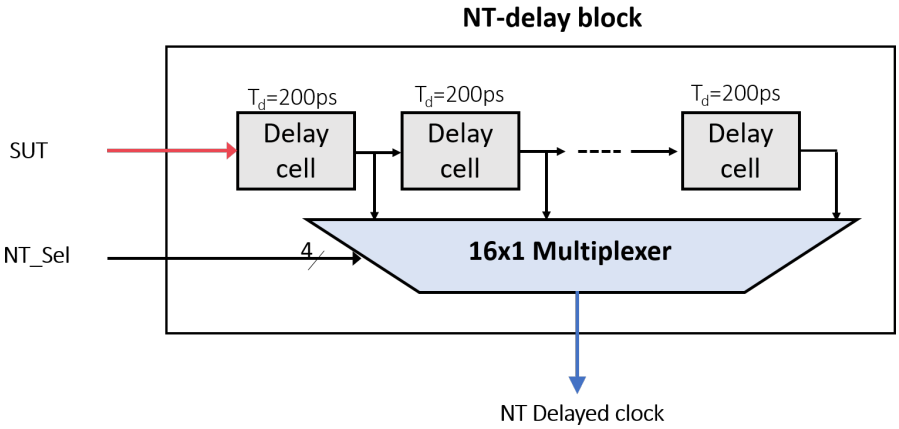


Figure 4.7: NT delay block diagram

The delay between the rising edges of SUT and the NT Delayed clock is calibrated such that the delay is an integral multiple of the SUT time period T. Fig. 4.8 shows the NT delay blocks in calibration mode. To set the NT delay block in calibration mode, a 'Cal_mode' signal is set to 1. The input mux to the delay cells selects the inverted output of the 15^{th} delay cell as the input to the first delay cell. Hence the entire delay line is connected in the form of a ring oscillator. The ring oscillator is allowed to run for a sufficiently long period of time for a given combination of bias

voltages. The gate control voltages (VGP, VGN) and body bias voltages (VBP, VBN) are used to control the delay of the current starved inverter inside each delay cell. VGN and VBN control the delay of the rising edge and VGP and VBP tune the delay of the falling edge. A 16-bit counter counts the number of cycles of oscillation of the Ring Oscillator (RO) formed by the delay line. The body bias voltages act as additional fine-tuning knobs for the delay, with the gate voltages providing large tuning ranges.

The calibration procedure starts by selecting nominal voltages for the gate and body bias. The RO is run for a fixed amount of time and the time period of the RO can be calculated by dividing the run time of the RO by the number of RO cycles counted in the calibration iteration. The oscillation period is given by $Tosc = 2d$, where 'd' is the delay of each delay cell. If the rising or falling edge delay has to be tuned, the calibration procedure is repeated with a new set of tuning voltages and the delay of the cells are calculated.

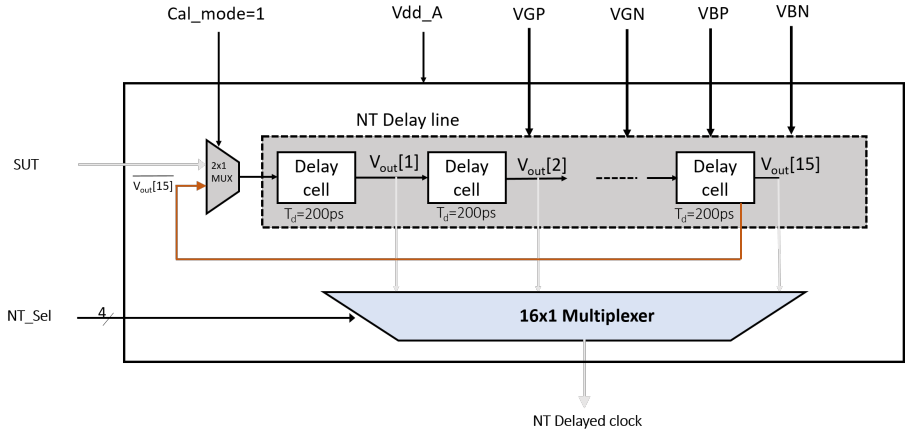


Figure 4.8: Description of NT delay block in calibration mode

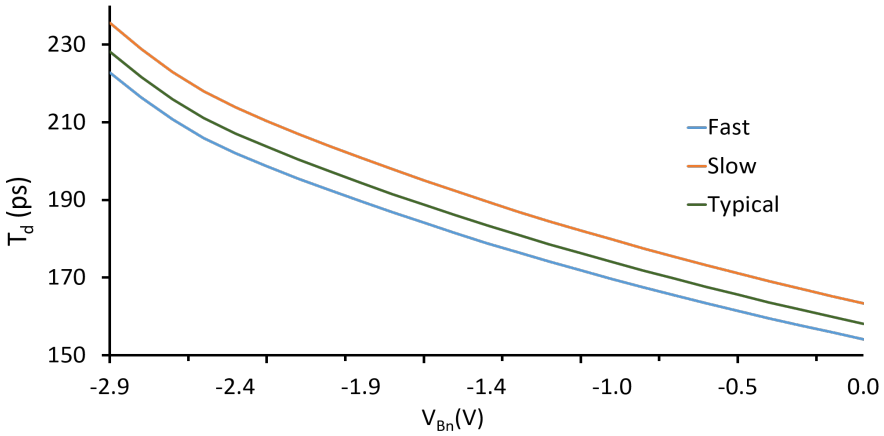


Figure 4.9: Rising edge delay variation with V_{BN} across process corners

Electrical simulations post layout have been carried out for the NT delay block and the variation in the delay values of a delay cell biased to 200 *ps* across process corners is as shown in Fig. 4.9. For the delay of 200 *ps*, a value of VGN around 0.7 V can be used. For this value, the plot shows that delay variation with body bias control is almost linear with a sensitivity of about 20 fs/mV. In Fig. 4.9, for slow process corner, the delay shows about 6% increase from the typical. This is because the rising edge transition which is impacted by V_{BN} is further slowed because of the process corner. On the other hand, for the fast process corner a 4.8% decrease in the delay values with respect to the typical process corner is shown. This is because even though the rising

edge transition time is increased because of body bias, the fast process corner causes this increase to be subdued. The shifts due to process corners can easily be tuned with the body bias voltage, with a resolution which does not need to be better than $1mV$. The availability of a large linear range of body bias allows for precise tuning, while the gate voltage can be used for coarse tuning of delay.

Fig. 4.10 shows the NT delay block during the normal mode of operation during measurement. This mode is set by asserting the value of 'Cal_mode' to 0. The input to the first delay cell is the buffered SUT. Since the jitter measurement instrument targets SUTs up to a few GHz, the NT delay block must provide a SUT delay from hundreds of picoseconds up to several nanoseconds. The selection of a delay of N clock periods is done via the multiplexer that selects the required number of cascaded delay elements.As an example, considering delay cells made of two delay elements, for a 1 GHz signal and $N = 3$, 15 delay cells biased with a typical delay of 200 ps each can be used, or 6 delay cells biased with a delay of 500 ps each. A lower number of delay elements will have less inherent noise, but it is necessary to consider also the sensitivity to the gate and body bias control voltage noise.

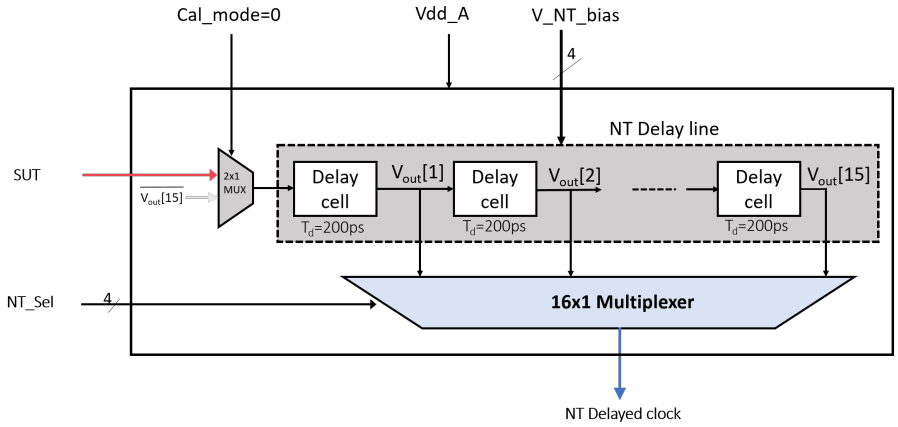


Figure 4.10: Description of NT delay block in measurement mode

The delay elements are designed using transistors of minimal size in spite of larger process and mismatch deviations with smaller sizes. Fig. 4.11 shows a histogram of mismatch variation for one delay cell biased to a delay value of 200 ps. For $V_{GN} = 0.7V$ and $V_{BN} = -2.13V$ that gives a 200 ps delay in the typical case. The histogram in Fig. 4.11 shows the effect of mismatch deviations using a Monte Carlo simulation with 200 samples. A standard deviation of 10.9 ps and a mean value of 201.3 ps are obtained. This variation can be tuned with the body bias voltage, or the gate control voltage in case of extreme deviations.

Fig. 4.12 shows the RMS delay noise at the output of one delay element obtained with a post-layout transient noise simulation of the nominal design. The noise bandwidth is set to $fmax = f$ and $fmin$ is limited by the simulation time of 1000 SUT cycles used for the calculation of one bin histogram. As f increases, this inherent noise also increases but less delay elements are required in the NT delay block. The block must be biased so that the minimum number N of delay elements are used. Delay noise will also be due to noise via the bias voltages, but with a sensitivity of a few fs/mV, it is not expected to be larger than inherent noise. The calculated RMS delay noise at 1 GHz (68 fs) shows that it will be possible to reach the target resolution of 100 fs for signals working at several GHz with a single delay element in the NT-delay.

4.2.2 Vernier delay line

In the architecture described in section 3.5, we utilize a Vernier Delay Line(VDL) to implement the fine delay value required for defining the histogram bin width. In other words, the smaller the

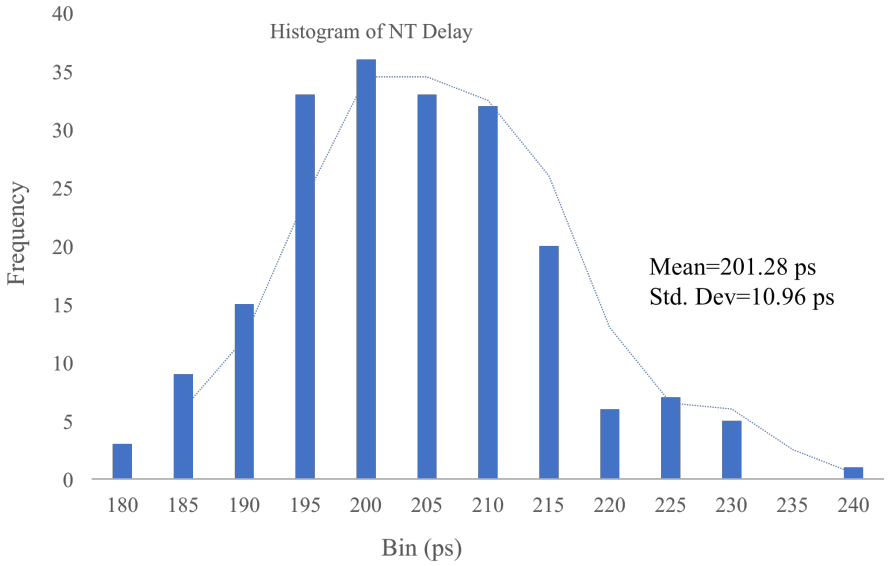


Figure 4.11: Histogram showing mismatch in NT delay values

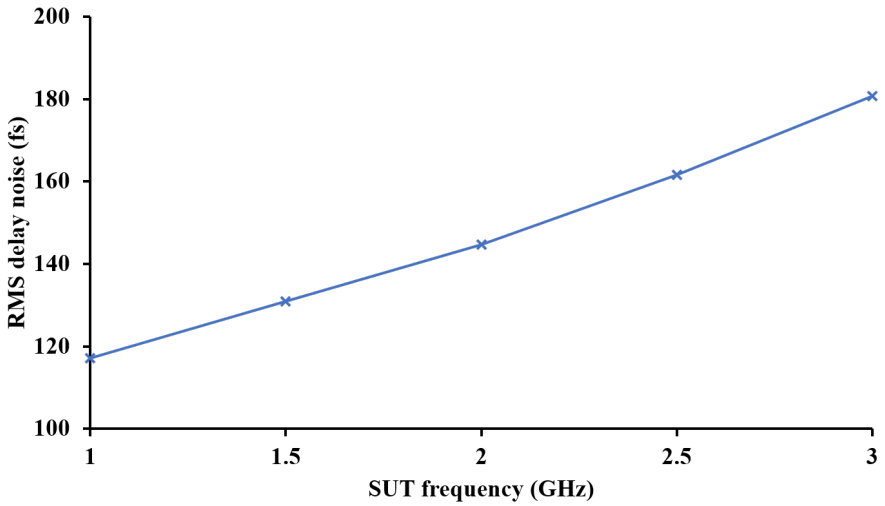


Figure 4.12: Output RMS delay noise of the typical single delay element

delay implemented by the VDL, higher the resolution Δ of the instrument. Fig. 4.13 shows the role and significance of a delay element in generating the jitter histogram using self-referenced technique. The delayed version of the SUT has to sample the SUT in the vicinity of its rising edge. The area in the vicinity of the expected rising edge can be divided into segments in time that are Δ *s* wide. First, the sampling clock is delayed by Δ *s* and the SUT is sampled for rising edges. The sampling clock is next delayed by 2Δ *s* and the SUT is again sampled for rising edges in this region of time. This process is repeated multiple times to generate the jitter histogram.

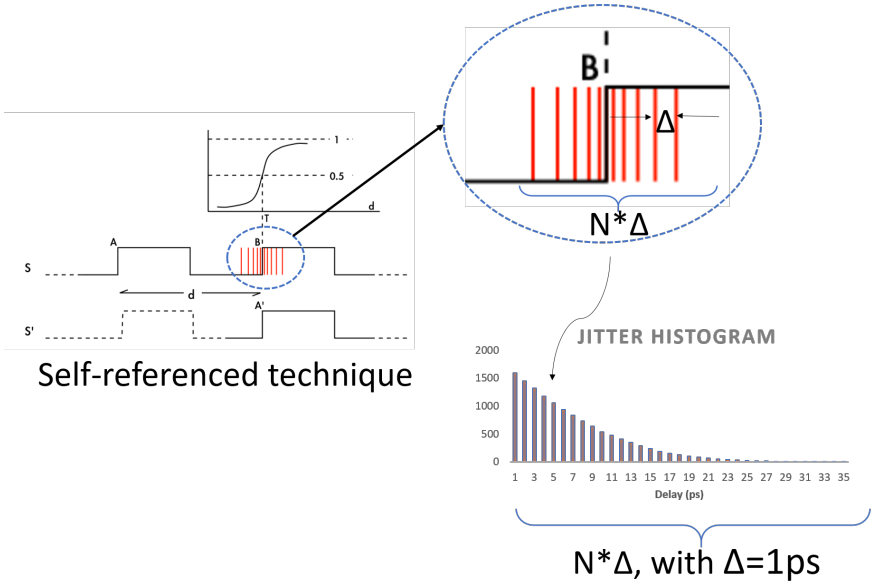


Figure 4.13: Significance of delay element in the test instrument

The width of time segment over which sampling is carried out defines the resolution Δ. For the proposed test instrument, we aim to achieve a sub-picosecond resolution. This means that the sampling clock has to be delayed exactly by a time duration smaller than 1ps. Implementing such small delays presents tight constraints on the design, as the minimum delay achievable in a given technology is the delay for the gate to charge to a logical 1 or to discharge to a logical 0. Furthermore, these delays are susceptible to process, voltage and temperature variation. There could also be mismatch variations that could impact the accuracy of Δ achievable. Hence we propose implementing delay elements using the Vernier delay technique. Fig. 4.14 shows the concept of Vernier delay. In Fig. 4.14(a), a delay is implemented between the signals V_{IN_A} and V_{IN_B} by passing one of the signals (V_{IN_B}) through a delay element which offers the required delay Δ. Here the delay is not robust to variations. On the other hand, in the Vernier structure shown in Fig. 4.14(b), the first signal V_{IN_A} is delayed by τ_A and the second signal V_{IN_B} is delayed by τ_B. The delay τ_B is calculated as $\tau_B = \tau_A + \Delta$. Hence, effectively the two signals V_{IN_A} and V_{IN_B} have a time delay of Δ between them.

There are advantages to using a Vernier delay structure. The first advantage comes from the fact that the delay to be implemented does not depend anymore on the absolute delay that can be implemented in a given technology. It is the difference between the delays τ_A and τ_B that has to be equal to the desired delay. The constraints on implementation of the delay elements have thus been described. For example, if a delay element is designed to give a 75 *ps* delay and another element with 85 *ps* delay, then by using the Vernier structure shown in Fig. 4.14(b), the effective delay will be 10 *ps*. It is easier to implement delay elements in the range of tens of *ps* than exactly 10 *ps*. The second advantage comes from the structure itself. If during fabrication there are differences in doping profiles for a given lot, if these Vernier elements are closely spaced in the layout, then they will see the same variation in the doping profile. Hence the difference between the delays

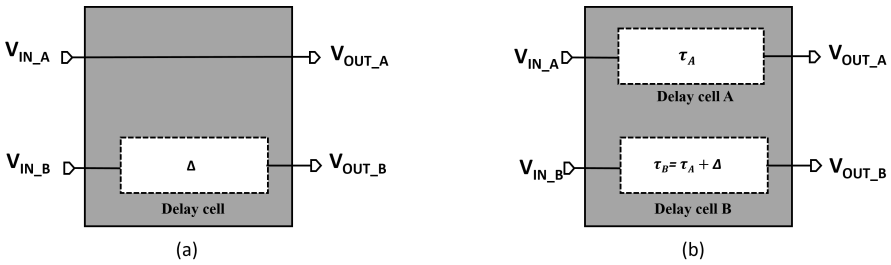


Figure 4.14: Concept of Vernier delay: (a) Delay implementation without Vernier (b) Delay implementation with Vernier

remains constant irrespective of differences in the absolute delay values because of process.

In ST 28 *nm* FD-SOI technology, it is possible to implement Vernier delay elements of $1ps$ delay. But through simulations, a mismatch variation of 5% was observed. This means that the width of each bin could be off by $+/-50fs$. This can lead to substantial errors in the calculation of RMS jitter value from the histogram. Hence a combination of a Time Difference Amplifier (TDA, explained in section 4.3) and the Vernier delay elements are used. Thus by making use of a TDA, the bin width is expanded by the gain of the TDA. By implementing a TDA with a gain of 100, the effective delay that needs to be implemented will be $\Delta xTDA_{gain}$. For example, to implement a Δ of 1 *ps*, it is sufficient to design delay elements with a delay of 100 *ps*.

The proposed test instrument is designed to generate a histogram with 25 bins with typically 100 fs of bin width. This requires that in combination with the TDA, there will be delay elements that provide a delay of 10 *ps*, 20 *ps*, and so on. To implement delay elements of this order, multiple calibration cycles have to be carried out to precisely calibrate the elements for the delay of a particular bin width. This is very time intensive. Hence to reduce the overall calibration time, a Vernier Delay Line has been used where 25 tunable Vernier cells of the type shown in Fig. 4.15 have been cascaded. Thus, it is sufficient to calibrate each Vernier cell for a delay of 10 *ps*. By cascading multiple Vernier cells each of 10 *ps*, we can form multiples of Δ.

Each Vernier cell is implemented by using two delay elements of the type described in section 4.1. Tuning knobs of V_{Bp_A}, V_{Gp_A} V_{Gn_A} and V_{Bn_A} are used for tuning the delay of element A to give a delay of τ_A. Similarly the delay element B is tuned to give a delay of τ_B by using the tuning knobs of V_{Bp_B}, V_{Gp_B} V_{Gn_B} and V_{Bn_B}. The cascaded structure of the Vernier Delay Line is as shown in Fig. 4.16. At each stage of the Vernier cell, the output can be tapped by using a multiplexer. For example, to generate the histogram for the tenth bin, we tap at the output of the tenth Vernier cell, and so on. Thus by progressively increasing the delay by a value of $\Delta xTDA_{gain}$ by passing from left to right of the VDL, an entire histogram can be generated by a one-time calibration cycle.

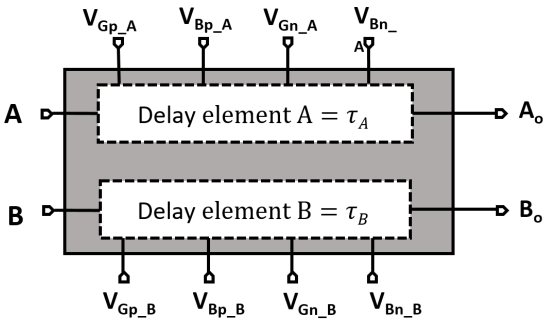


Figure 4.15: Vernier cell

The delay line A is biased to give a delay of τA, while line B is biased to give τB. The delay

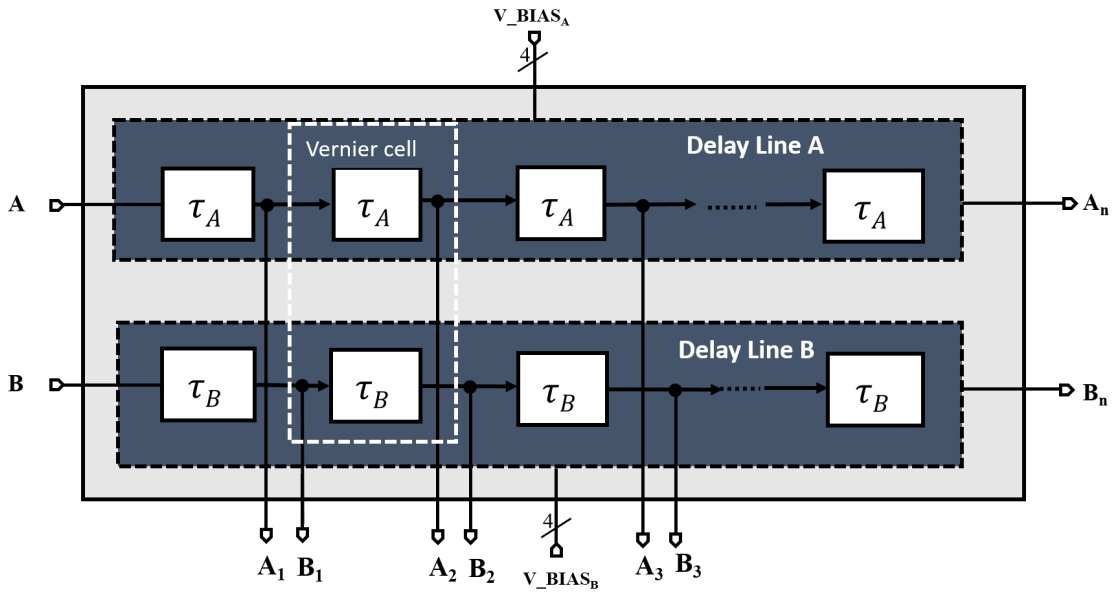


Figure 4.16: Vernier Delay Line

d_i between the two tapped lines at the output of the i^{th} Vernier delay cell is no longer dependent on the delay of each individual delay cell, but rather on the delay difference Δ between two delay cells and the number of Vernier delay cells so that $d_i = ix\Delta$. With this, it is possible to obtain a delay resolution smaller than the delay of an individual delay cell.

The SUT signal and the sampling clock are fed at the two inputs of the VDL. The tapped outputs of the i^{th} Vernier delay cell are sent to a phase comparator described in section 4.4. As a result, the SUT signal is sampled by the NT-delayed sampling clock with an additional delay $d_i = ix\Delta$ added between both signals. For a given number of periods of the SUT signal, the number of hits at the output of the phase comparator is counted to give the value of the i^{th} histogram bin.

Uncorrelated mismatch deviations within a Vernier cell will affect the typical delay Δ added by each cell. It is not intended to calibrate each Vernier cell individually since this would require a large number of control and bias voltages. Instead, the delay cells of each tapped delay line are calibrated altogether, ensuring that the overall delay of the line meets the specifications. For this, each delay line of the VDL is configured as a RO and calibrated as discussed already in the previous section. Clearly, there will be deviations from the typical Vernier cell delay Δ from cell to cell, and the delay difference d_i at the output of the i^{th} Vernier delay cell will not be exactly $di = ix\Delta$, producing non linearities in the VDL.

A nominal resolution of Δ=10 ps can be obtained by biasing delay cells A and B with $VGn =$ 0.7 V, $VBn(A) = -0.36$ V and $VBn(B) = -1.97$ V. The sensitivity to the bias voltages at these points is of $15fs/mV$ and $30fs/mV$ for cells A and B, respectively. For a random instance of the simulated VDL at transistor-level in 28 nm FD-SOI under process and mismatch deviations, Figs.4.17 (a), 4.17(b) and 4.17(c) give, as a function of the VDL cell depth, the variability of Δ, the time difference at the output, and the Integral Non-Linearity (INL) error, respectively. The average value of Δ is 8.8 ps with a standard deviation of 1.5 ps which referred to the input of the TDA results in 15 fs, below the delay noise level of a delay cell. The INL fluctuates between 4 ps with a maximum linearity error about 2% referred to the full delay. For the whole set of Monte Carlo instances, these values do not vary significantly.

The typical time difference at the VDL output is $25x8.8 = 220$ ps with a standard deviation of $1.5\sqrt{25} = 7.5ps$. Since this is rather close to Δ=10 ps, the calibration of the VDL can enhance accuracy. The average delay for each delay cell in line A is 72.6 ps with a standard deviation of 2.78 ps. The total delay of delay line A will be $d_A = 72.6x25 = 1815$ ps (with a standard deviation

of $2.78\sqrt{25} = 13.9ps$). The average delay for each delay cell in line B is 81.4 ps with a standard deviation of 2.03 ps. The total delay of delay line B will be $d_B = 81.4x25 = 2035$ ps (with a standard deviation of $2.03 * sqrt25 = 10.1ps$). Delay line A can be calibrated with a resolution of 1 ps by counting its oscillation cycles that must be in the range $N_A = [2 * d_A/-1, 2 * d_A/+1]$= $[3629, 3631]$ with a measurement time of $T_A = N_A * 2 * dA = 13.177$ s. For delay line B, $NB =$ $[4069, 4071]$ with a measurement time of $TB = 16,565$ s.

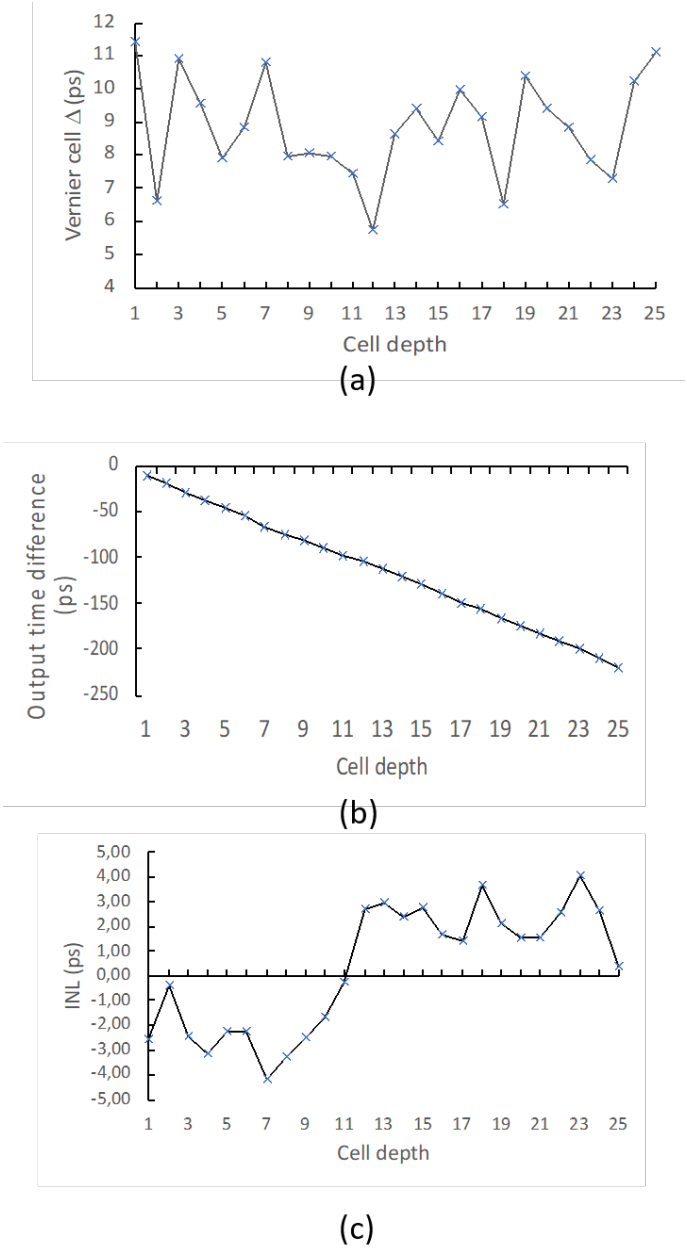


Figure 4.17: VDL simulation at transistor-level in 28 nm FD-SOI under process and mismatch deviations. As a function of cell depth for a random instance: (a) Δ of the Vernier cells, (b) time difference at the output of a Vernier cell, and (c) INL.

4.3 Time Difference amplifier

A Time Difference Amplifier (TDA), as the name implies, takes two signals with an input time difference of T_{in} as input and amplifies this difference by its gain $Gain_{TDA}$ to give the output time difference $T_{out} = T_{in}xGain_{TDA}$. The working concept of the TDA is presented in Fig. 4.18.

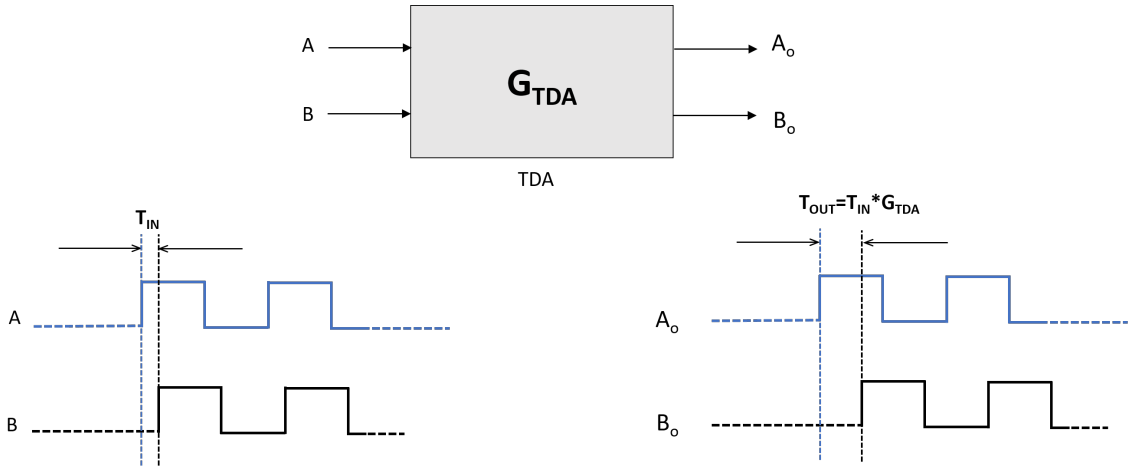


Figure 4.18: Concept of Time Difference Amplifier

In the proposed instrument, we use the TDA described in Fig. 4.19 [10] which is an improvement of the one proposed in [29] with increased gain and range control. It is composed of two unbalanced SR latches. When two signals are almost simultaneously incident on an SR latch, the latch takes a longer time to come out of metastability. The latch finally settles its outputs in a state that depends on which signal slightly advances the other at its inputs. This property is exploited to amplify the latch input time difference T_{in} into an output time difference T_{out}. As shown in Fig. 4.20(a) in a discontinuous trace, the characteristic gain function of the SR latch $T_{out} = f(T_{in})$ is symmetrical. The output tends to a large value when the input tends to 0, and to a small value for large absolute values of the input. The actual gain depends on the NAND gate transconductance during metastability and the output capacitance. By adding a time offset T_{off} in opposite branches of the two latches, the gain characteristic of each latch is shifted in opposite directions as shown in Fig. 4.20(a) in continuous traces. The characteristic gain function of the TDA $T_{out} = f(T_{in})$ is shown in Fig. 4.20(b). It is just the difference of the characteristic gain functions of the two SR latches. The NAND outputs from the SR latches are fed to capacitors that help to further boost the gain of the TDA which should be operated in its linear region in the range $[-T_{off}, T_{off}]$.

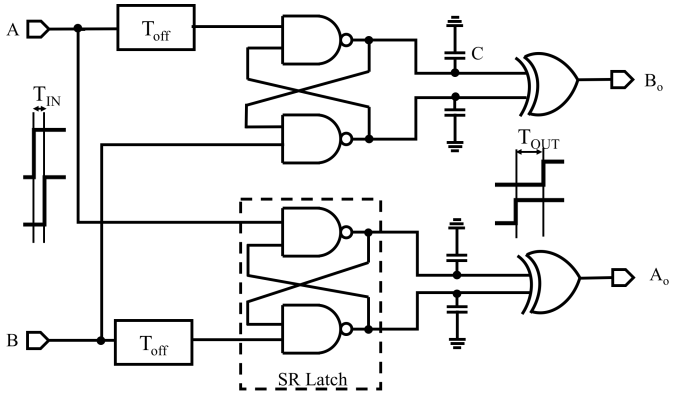


Figure 4.19: Single stage Time Difference Amplifier [10]

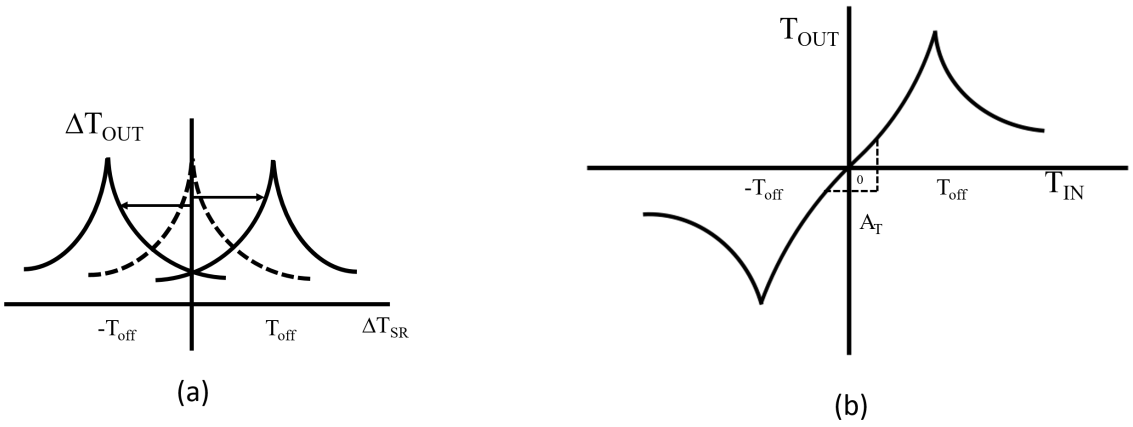


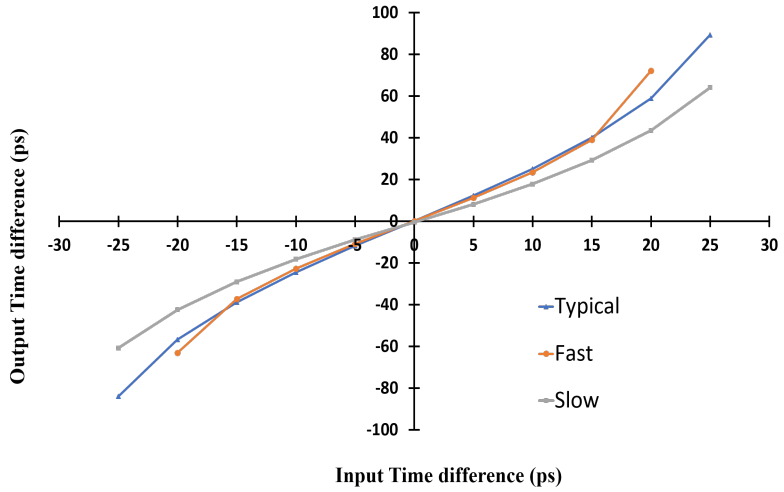
Figure 4.20: TDA:(a) conceptual gain characteristics of the two SR latches and (b) conceptual gain characteristic of the TDA [10]

The TDA placed at the input of the VDL must guarantee a Δ of at least 100 fs. Fig. 4.21(a) shows the post-layout gain characteristic of a single TDA stage in 28 *nm* FD-SOI technology under process corners with an input range $[-25,25]$ ps, which results in an output range about $[-90,90]$ ps. The average gain is about 3.6. The worst-case INL can reach 13.9 ps giving a maximum non-linearity of 15% referred to the output range. Since the gain must be about 100, four stages of this TDA must be cascaded. Fig. 4.21(b) zooms in the input range $[-2.5,2.5]$ ps that is required for a $\Delta = 100$ fs at the TDA input. There is no significant non-linearity in this range and the typical stage gain is about 2.5. Mismatches between latches and between capacitive loads result in a zero-output offset of a maximum of 250 fs. Since this is larger than the target of 100 fs, this can result in a shift of the output histogram. This is easily corrected using the NT delay block.

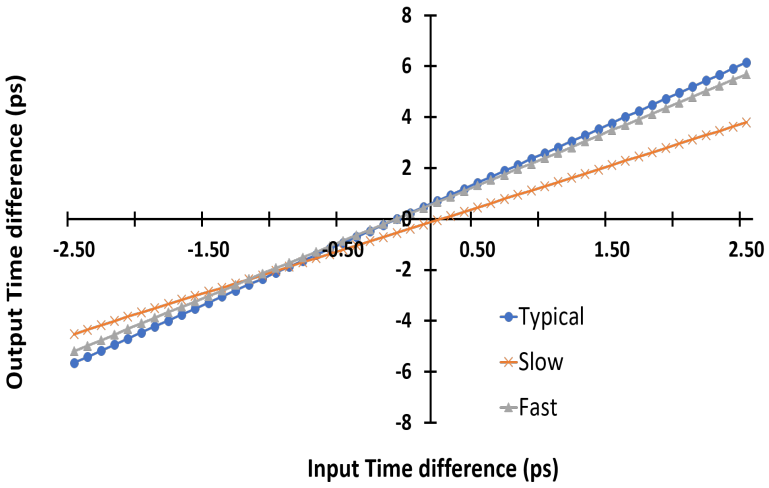
The inherent noise of the TDA ultimately limits the resolution of the test instrument. Table 4.1 shows the equivalent RMS noise delay at the input of one TDA stage obtained with post-layout transient noise simulation of the nominal design. The test instrument will not be able to have a resolution better than this noise level which fits well with our target of 100 fs for GHz signals. Although noise increases with frequency, the gain of the stage also increases and input referred noise is steady.

Table 4.1: Equivalent Input RMS Noise delay of a TDA stage for the typical design

SUT (GHz)	RMS delay noise (fs)	Average stage gain	Input referred RMS delay noise (fs)
1	147	3,4	44 1
1,5	161	3,5	46
2	171	3,8	44
2,5	181	4,5	40
3	192	5,2	37



(a)



(b)

Figure 4.21: Post-layout simulation under process corners of the gain characteristic of one stage of the 28 nm FD-SOI TDA for an input range of: (a) $[-25, 25]$ *ps, and (b)* $[-2,5, 2.5]$ *ps.*

4.4 Phase comparator

The test instrument requires a phase comparator to sample the SUT by its delayed version. This phase comparison is repeated for each bin. At each stage of the VDL, the tapped outputs are sent to the phase comparator and the hits are counted. If the delayed version of the SUT samples a rising edge in the SUT for a given bin, the output of the phase comparator goes high. A 10-bit counter counts the number of hits for each bin.

The output of the tapped VDL is sent to the phase comparator. Each stage has its own phase comparator to avoid errors in the sampling of the rising edge because of propagation delays in the signals from the output of the VDL to the input of the phase comparator. A D flip-flop has been used as the phase comparator with a classical Master-Slave architecture shown in Fig. 4.22. The setup time of the D flip flop across process corners is 11 *ps* at typical corner, 14 *ps* at slow corner and 9 *ps* at fast corner. Thus a convenient value of setup-time of 15 *ps* has been considered for design purposes.

The outputs of the 25 phase comparators are sent to a multiplexer that selects the input based on the pin number.

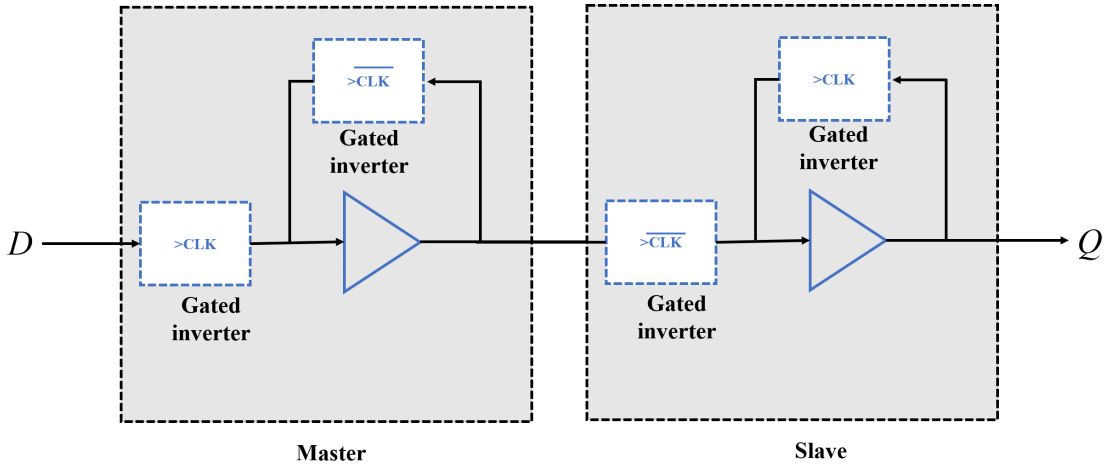


Figure 4.22: Schematic of master_slave D Flip-flop used as a phase comparator

4.5 Digital interface

The core of the instrument formed by the blocks described in the previous sections are supported by a digital section of the instrument. The select lines for the various multiplexers used to assert calibration and measurement modes, counters and shift registers to count and store the hits, etc are a part of the digital circuitry. Hence the programmability of the test instrument and control signals for the instrument operation are supported by the digital section of the instrument.

4.5.1 Scan registers for digital interface

The control bits required for program control of the instrument is achieved by a scan chain register. This is a 16-bit shift register with load and scan functionality. This control register is used to program the different operation modes which include the calibration of the NT delay, the calibration of the delay lines, the selection of the measurement bin, and the operations of shifting data in and

out for instrument programming and readout. The scan-chain is made by cascading D Flip-flops of the type shown in Fig. 4.22 with additional circuitry for the choice of scan and load.

There is also a 16-bit shift register used to store the counter output from the 16-bit counter used during calibration. Another 10-bit shift-register stores the value from the 10-bit counter that has the number of hits for a given bin. A 16-bit shift register has 13 of its bits used for program control. The input to the scan chain is the one-bit input TDI from the external digital interface. The scan chain is initially loaded with the desired input digital word by using the digital clock of TCK. Once the value is loaded, the operation is issued a START/STOP signal. After the programmed operation is completed, the bits from the scan chain now loaded with the operation's output is serially output from the TDO pin of the instrument.

Pin description of the instrument and note on program control bits

The architecture of the test instrument shown in section 3.5 has been reproduced in Fig. 4.23 highlighting the digital circuitry that supports the signal path. The pin description of the instrument is given in Table 4.2.

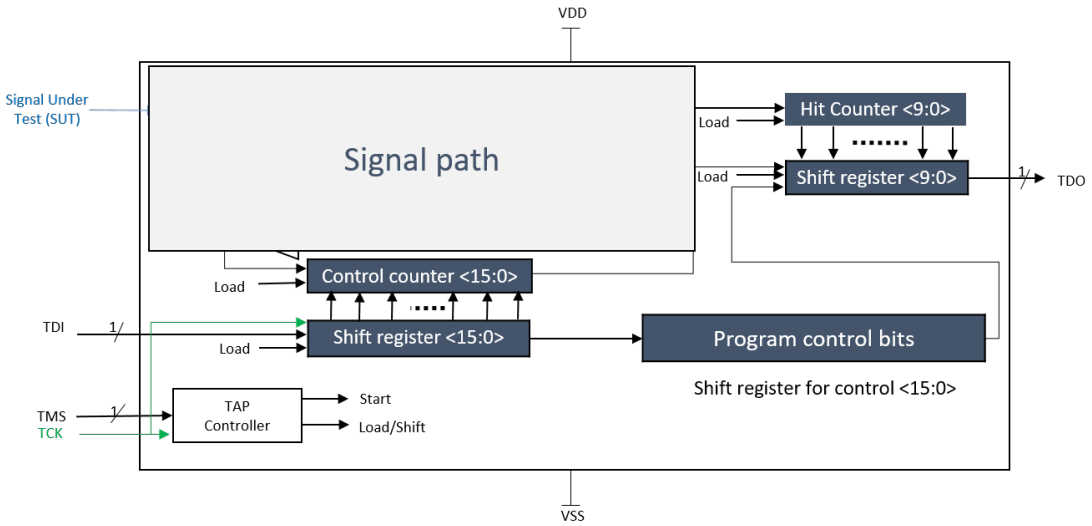


Figure 4.23: Architecture highlighting the digital circuitry

Table 4.2: Pin description of the proposed test instrument

Pin	Direction	Description
SUT	Input	Input for the Signal Under test
TDI	Input	Input control bits
TCK	Input	System clock for the counters and shift registers
TDO	Output	Output of the BIST
VDD		Power supply
VSS		Ground

The 16-bit shift register for control holds the control bits that support programmability for the measurement. The description of the various control bits in this register is as shown in Fig. 4.24.

	Bit	Reset state	Description
Test_mode	1	0	• 0: Calibrate mode • 1: Test mode
TDA_sel	2	00	• 00: TDA stage 1 output connected to DFF • 01: TDA stage 2 output connected to DFF • 10: TDA stage 3 output connected to DFF • 11: TDA stage 4 output connected to DFF
N_sel	3	000	Control inputs to program 'NT' delay
Mux_sel	5	00000	• 00000: First VDL element connected to TDA • 00001: Cascade of 2 VDL elements connected to TDA • 00010: Cascade of 3 VDL elements connected to TDA ⋮ • 11001: Cascade of 25 VDL elements connected to TDA

Figure 4.24: Program control bits description

4.6 Simulation results of the test prototype

The test instrument has been simulated for an input SUT frequency of 1GHz and an added random jitter of RMS 0.8 *ps*. The Fig. 4.25 shows the results of one instance of a noise transient transistor-level simulation of this instrument, considering 1000 SUT cycles for the measurement of each bin, and a noise bandwitdth with $fmax = f$. This simulation includes a 5-stage NT delay ($N = 4$), 4-stage TDA, 25-stage VDL and output flip-flops. The digital control circuitry is not included in the test bench and has been simulated and verified separately. The simulation of the histogram is highly resource intensive given that the time of 1µs is being simulated. Hence to save run time for simulation, 25 test benches with one histogram bin per test bench were created for faster results.

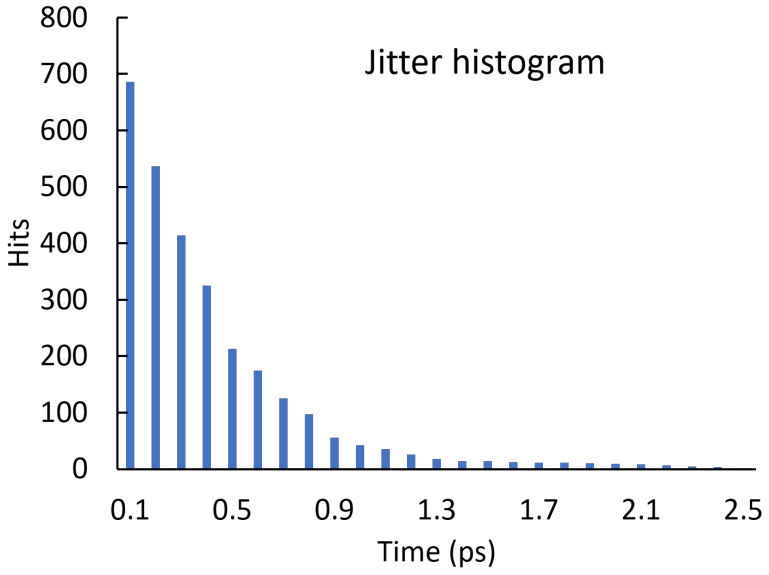


Figure 4.25: Jitter histogram

The principle for the generation of the jitter histogram is illustrated in Fig. 3.20 for a VDL that contains 25 delay cells. The outputs of each VDL cell allow computing one point of the Cumulative Distribution Function (CDF) of the jitter, at regular delays in the vicinity of the expected clock edge of the SUT. For each delay cell, the SUT is processed for 1000 SUT cycles in order to

produce the value of the corresponding CDF bin that is scanned out from the chip. The calculated bin values are assembled to produce the CDF. The jitter PDF is obtained off-chip by derivation of the CDF, and the absolute RMS jitter is calculated from it after correction by a factor of $\sqrt{2}$. It must be noticed that the implementation only considers sampling one side of the SUT random jitter PDF that is considered symmetrical. The calculated histogram of Fig. 4.25 results in a RMS jitter of 0.71 ps which fits well into the target resolution.

4.7 Layout of the prototype

A snapshot of the layout of the test chip sent for fabrication is shown in Fig. 4.26, with the jitter test instrument situated in the center left and is highlighted. The test chip was sent for fabrication in the PANDA run during 1S of 2022. The test chip is pad limited and the overall size of the test chip is 1.43 mm^2. The size of the core instrument is 340x230 μm^2. The area of the chip including pads is 1205x1187 μm^2.

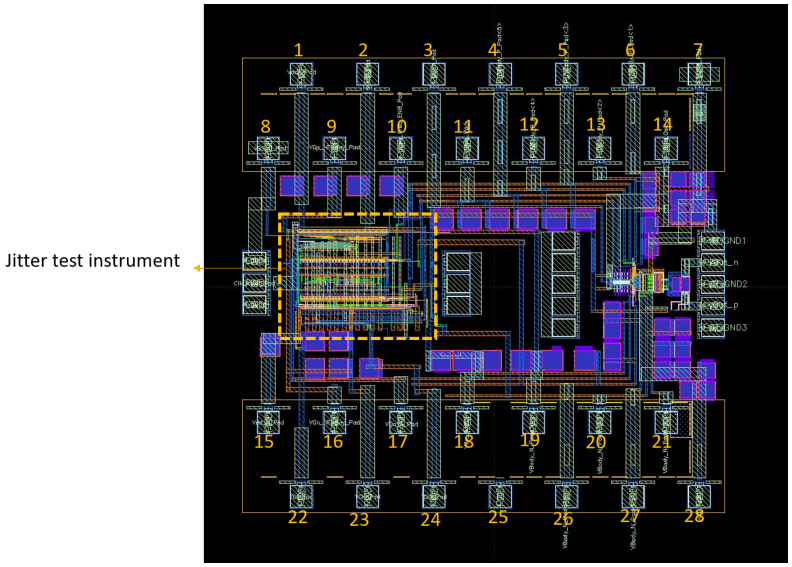


Figure 4.26: Layout of the test-chip

4.8 Conclusion

This chapter describes the transistor level implementation of the test instrument. The signal path consisting of delay lines and the TDA has been explained. The programmability of the instrument and measurement procedure is supported by a digital section consisting of shift-registers and counters. Electrical simulation results carried out on the designed instrument have been discussed and results show estimation of random jitter content within the desired resolution of measurement. Finally, the layout of the instrument has been presented.

5

Design of a Sub-sampling TDA

This chapter presents the motivation and design description of a sub-sampling TDA to mitigate the challenges faced by traditional TDA architectures at high frequencies. Operation of the traditional TDA at higher frequencies leads to missing pulses at the TDA output. A sub-sampling TDA overcomes this challenge and hence this design can be used to estimate jitter content of signals up to 5GHz. Electrical simulation results that demonstrate sub-picosecond resolution of jitter measurement for a 5GHz clock signal are presented in this chapter.

Contents

5.1 Jitter measurement at high frequencies

High-speed communication in the current day utilizes clock signals in the Gigahertz frequencies, with the jitter content barely a couple of picoseconds. The jitter requirements get more constrained as the BER rates for communication links also decrease. For example, a local oscillator (LO) for $5G$ new radio requires sub-100 fs rms jitter to support $64-$OAM and 2×2 MIMO under non-ideal channel conditions [30]. The trend towards high frequencies continues with frequencies reaching close to 5 GHz, with jitter in the range of few picoseconds. [31] shows a PLL working with a VCO in the range of 1.5 to 4 GHz, where they propose an attachable fractional divider that transforms an Integer-N PLL into a Fractional-N PLL with only 0.35 ps of integrated RMS jitter degradation. In [32], a digital Fractional-N Sampling PLL has been designed in 28 nm CMOS that offers $0.16ps$ RMS-jitter and has a frequency range of 2.7-to-4.3 GHz. [33] presents a 6GHz fractional-N sampling PLL in a 14 nm process with a Digital-to-Time Converter Range-Reduction Technique Achieving 80 fs Integrated Jitter and 93 fs at Near-Integer Channels. A PLL that generates a 4-phase 10-GHz clock for a 40-Gb/s serial link transmitter has been proposed in [34] in which the measured integrated jitter of the PLL is 214 fs from 1.2-V supply.

The measurement of jitter at such high frequencies for maturity testing necessitates on-chip jitter measurement as tapping lock signals in the range of Gigahertz itself is difficult. For the on-chip measurement using the test instrument described in Chapter 4, additional design constraints arise because of higher operational frequency. While the delay line that forms the NT-delay will have fewer elements and hence less noise contribution, the major source of concern will be the Time Difference Amplifier. The TDA works with a constant output regeneration time which is irrespective of input frequency. At frequencies close to 5 GHz or more, the outputs will not have sufficient time to be regenerated before the next clock cycle arrives. The operation of a high-gain TDA in multiple GHz range results in missing pulses at the output because of a trade-off between the gain and the output regeneration time constant. This has been discussed in detail in section 5.2. The role of the TDA is to relax the design constraint placed on the Vernier delay elements and still allow for sub-picosecond resolution of measurement. Since a high resolution instrument requires a high-gain TDA, overcoming this challenge becomes crucial. A sub-sampling TDA has been designed to mitigate this challenge and has been described in section 5.2.3. Section 5.3 describes the modified jitter test instrument that includes a sub-sampling TDA. Simulation results for the modified jitter test instrument are presented in Section 5.4.

5.2 Challenges in TDA operation at high frequencies

5.2.1 Working principle of TDA

The circuit schematic of the TDA described in Chapter 4 has been reproduced here for convenience in Fig. 5.1. The TDA consists of two SR latches, where one arm of each of the SR latches is deliberately unbalanced with a value of T_{off}. The TDA uses the concept of metastability when both inputs to an SR latch go high simultaneously. Depending on which of the input arrives earlier at the input of the latch, the output in the metastable state will resolve to 1 or 0 after a certain delay. The SR latch followed by an XOR gate in Fig. 5.2(a) forms a single branch of the TDA. Fig. 5.2(b) shows the input and output waveforms of the SR latch followed by XOR gate. When both inputs go high, the initial voltage developed at the output of SR latch, denoted by $A(0)$ varies proportional to the time difference at the inputs between S and R ΔT_{SR}. Fig. 5.2(b) shows the regeneration process because of the positive feedback in the latch. The regeneration of the outputs S_o and R_o follows an exponential curve. The SR latch output voltage difference is given by [10]

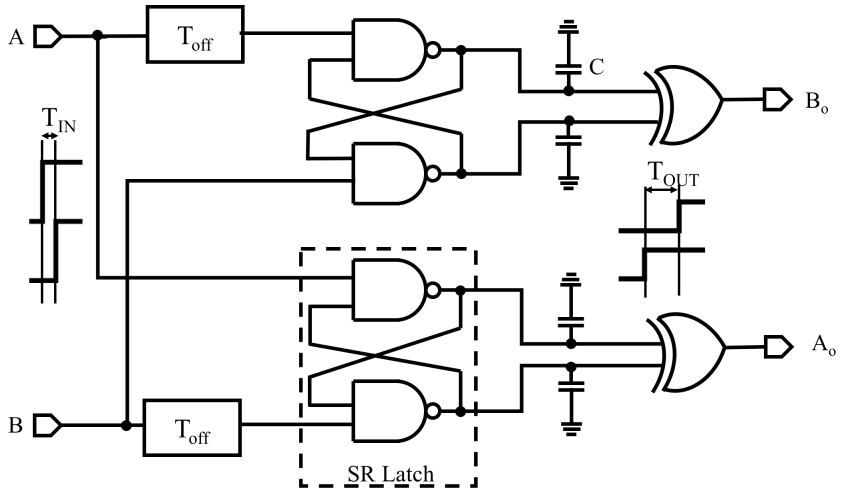


Figure 5.1: Single stage Time Difference Amplifier [10]

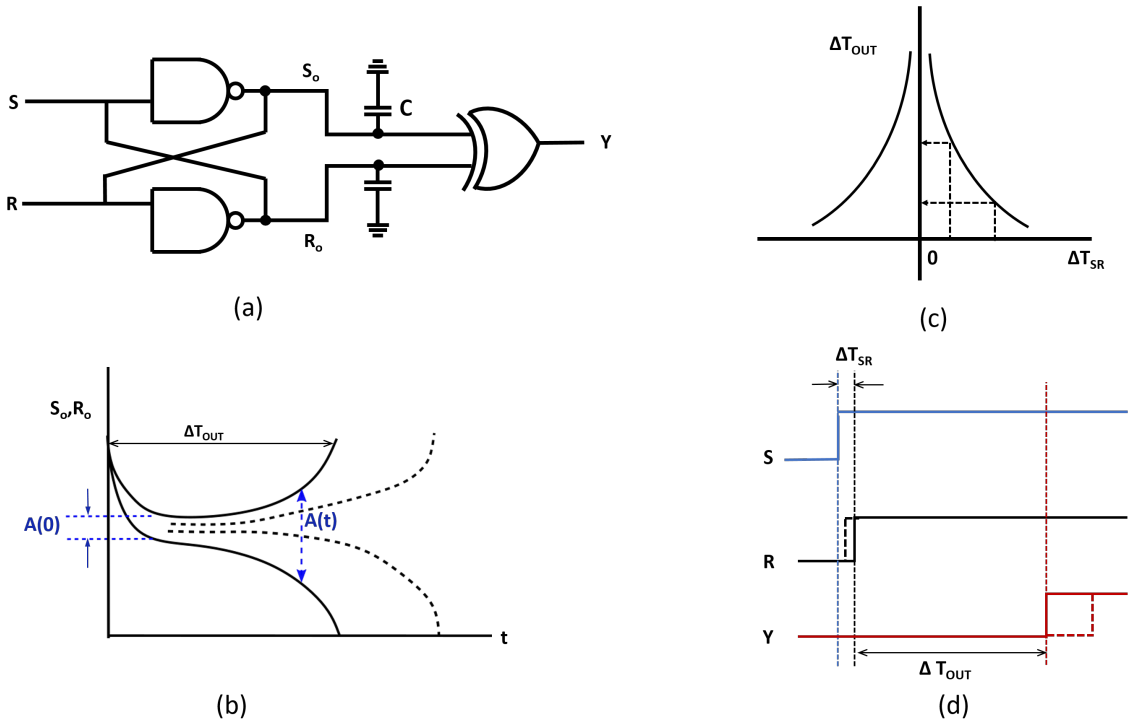


Figure 5.2: (a) SR latch followed by an XOR. (b) Regeneration process in SR latch. (c) Relationship between the regeneration time and the initial time difference. (d)input and output waveforms of the SR latch followed by XOR [10]

$$A(t) = A(0)e^{\frac{t}{\tau}}$$
$$for\ A(0) = \alpha.\Delta T_{SR} \tag{5.1}$$

where α is the proportional factor and τ is the regeneration time constant given by $\tau = \frac{C}{g_m}$. Here, C is the capacitance seen at the output of the NAND gate of the SR latch, and g_m the transconductance of the NAND gate in the state of metastability. Regeneration time of the output therefore depends on the capacitance C and the transconductance g_m. The outputs are resolved to a 0 and 1 when the difference between the output voltage levels reaches the threshold voltage. The XOR gate goes high when the regeneration process is complete. From the graph shown in Fig. 5.2(c), we can observe that as the input time difference ΔT_{SR} decreases, the output regeneration time ΔT_{out} increases. This is because the closer the input signals that incident on the SR latch, the latch stays in metastability for longer since it is more difficult to resolve at the output. The time for the output voltage difference to cross the threshold voltage also increases. The regeneration time T_{out} and the initial time difference T_{SR} are related by a logarithmic function given by [10]

$$\Delta T_{out} = \tau.(\log V_{TH} - \log|\alpha.\Delta T_{SR} \tag{5.2}$$

When a time offset is added to the SR latch, the characteristic shown in Fig. 5.2(c) shifts either left or right depending on the value of T_{off}. From the characteristic curves, it can be observed that T_{off} also defines the operation region of the TDA. The TDA schematic has two SR latches and they are unbalanced by adding delays in opposite inputs and the characteristic shifts as shown in 5.3(a). The SR latch characteristics are moved in two opposite shifts: one to the left and the other to the right and the final delay characteristic is reproduced in Fig. 5.3(b). The final characteristic is thus the difference of curves in 5.3(a) from each other. The time difference taken at the outputs of the TDA implements this subtraction. The characteristics follow an exponential path, but a small segment of the curve around the origin is linear. This gives the operation region of TDA. It is to be observed that the direction of time difference at the input is preserved at the output. If in Fig. 5.1 the input A leads B, then the output A_o leads B_o and so on.

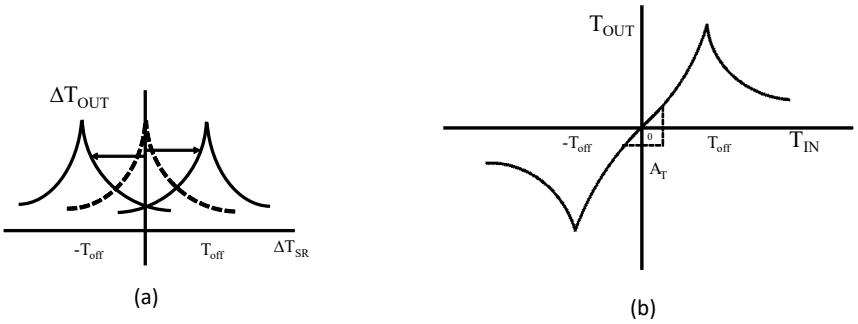


Figure 5.3: TDA (a) Shifted SR latch delay characteristics. (b) TDA characteristic [10]

5.2.2 Challenges in TDA operation at high frequencies

The small-signal gain of the TDA is given by

$$G_{TDA} = \frac{2C}{g_m T_{off}} \tag{5.3}$$

where T_{off} is the offset added to the input of the SR latch, C is the capacitance at the output of the NAND gate and g_m the transconductance at metastability.

The gain is directly proportional to the regeneration time constant $\tau = C/gm$ [29] and inversely proportional to T_{off}. Higher the gain required, higher is the regeneration time constant, and the

intrinsic delay or response time of the TDA also increases. As the frequency of the input signal increases, for the same gain, the response time of the TDA remains the same irrespective of the frequency. Hence, for signals with lower time period (higher frequency), the output regeneration time may now become longer than the time period of input. This causes the consequent falling edges at the inputs of the TDA to reset the output of a SR latch before the TDA could regenerate the result required for the previous rising edges. Fig. 5.4 shows the outputs of a SR latch for two cases, one at lower frequency for which the latch has sufficient time to regenerate before the consequent falling edge arrives, and one at higher frequency where the SR latch outputs are reset to high before it could get out of the meta-stability state. At lower frequencies, the outputs *Latch_Out_A* and *Latch_Out_B* at the output of the SR latch have sufficient time for the latch to recover from metastability as was described earlier in Fig. 5.2(b). For the second case shown in Fig. 5.4, the outputs of the SR latch are still resolving between 0 and 1, and before the resolution the SR latch inputs see a falling edge which resets the latch outputs. The difference between the voltage levels at the SR latch do not cross the threshold voltage before the next falling edge arrives. The output of the XOR gate for both the SR latches never goes to 1 and hence the TDA output shows missing pulses at higher frequencies.

One possible solution for this problem is to increase the duty cycle of the input of the TDA so that the SR latch will have more time to get out of the meta-stability state when solving for the rising edges [8]. However, for frequencies in the GHz range and on times in the range of picoseconds, this becomes quickly insufficient. As the regeneration time at the output does not scale with the input time period, the implementation shown in Fig. 5.1 has missing pulses at the output. A sub-sampling TDA has therefore been proposed that has been demonstrated to overcome this limitation and hence make it possible to measure jitter using the designed test instrument at higher frequencies.

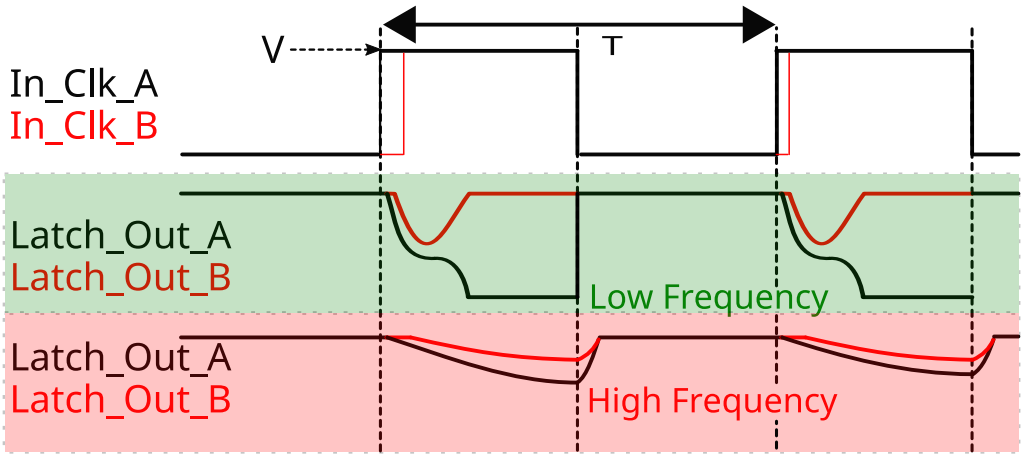


Figure 5.4: Missing pulse for high frequency TDA operation

5.2.3 Sub-Sampling TDA

A novel subsampling mode of operation for the classical TDA has been proposed and the implementation is described in this Section. With the help of an additional digital control circuitry, the input to the TDA is monitored to ensure that the outputs for a given cycle of input are regenerated before passing the falling edges at the input of the TDA. Once the time difference between the input rising edges being processed has been amplified, the TDA inputs are sent a falling edge to start the next cycle of operation. This way, instead of passing all edges, selected edges are passed along with an interval defined by the inherent delay of the TDA. This results in a sub-sampled input set sent to the TDA for time amplification, but ensuring there are no missing pulses at the

output since each selected input is amplified. The under-sampled jitter will be a random process with the same characteristics as the jitter in the clock signal.

A sub-sampling TDA with four stages is shown in Fig. 5.5. The asynchronous operation of the digital control circuit is explained in Algorithm 1 and illustrated by the waveforms shown in Fig. 5.6. The first block shown in Fig. 5.5 is a latch that is controlled by a Select_Rise_Fall signal . This signal controls whether the rising or falling edges of In_Clk_A and In_Clk_B are sent to the 4-stage TDA. Once the TDA operation starts, the digital control circuitry monitors the TDA outputs to see if a given input time difference has been amplified and the next operation cycle can start. The digital control block has three inputs: The TDA inputs In_Clk_A , In_Clk_B and an *RST* signal. When the reset signal (RST) is high, the inputs and outputs of the TDA are at logic zero. This helps to reset the entire modified TDA and prepares it for the next cycle. When RST becomes low, the TDA is enabled. The operation of the control circuit requires two internal signals TR and TF that define if rising or falling edges are passed to the TDA inputs, via two control latches by generating pulse signals Select_Rise and Select_Fall with a time duration that depends on the input clock signals.

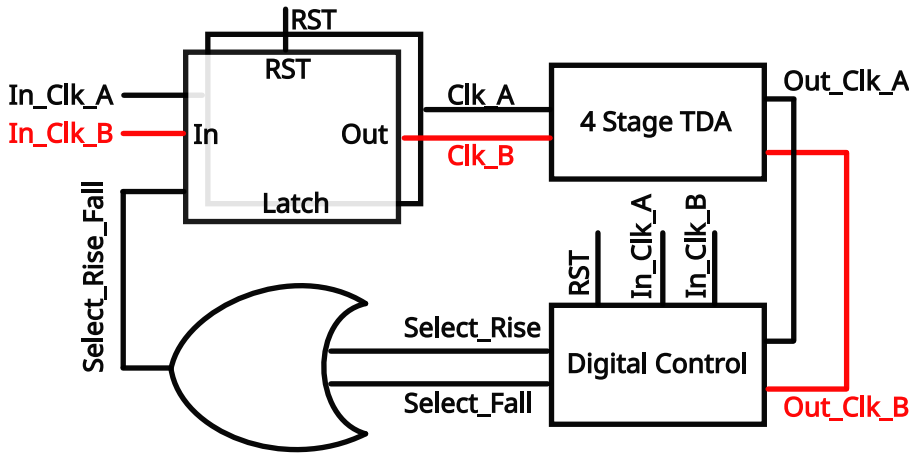


Figure 5.5: Sub-sampling TDA

Algorithm 1: Algorithm of Digital Control

if *RST* is logic high
$Out\_Clk\_A = 0, Out\_Clk\_B = 0, i = 1$
$Select\_Rise = 0, Select\_Fall = 0;$
else
$TR = (Out\_Clk\_A \& Out\_Clk\_B),$
$TF = (Out\_Clk\_A \| Out\_Clk\_B)$

always @ (Negedge(TF) OR (i==1))
Generate **Select_Rise** Pulse
$i = 0$
always @ (Posedge(TR))
Generate **Select_Fall** Pulse

From Fig. 5.6, it can be observed that when RST is low and Select_Rise is set high, the rising edges of the input signals In_Clk_A and In_Clk_B are latched by the input latch and sent to the 4-stage TDA. The digital circuitry then monitors the output of the 4-stage TDA Out_Clk_A and Out_Clk_B. When the TDA finishes the amplification and the output signals are available, the signal Select_Fall is set high. The signal Select_Rise_Fall is the logical "OR" function of

Select_Rise and Select_Fall. Select_Rise_Fall finally controls the latching of TDA inputs for amplification by the 4-stage TDA is sent half a clock period in advance and hence setup and hold time requirements of the input latches will be respected. Mismatch between the two control latches will shift the output jitter histogram, but this is corrected during a simple calibration step of the instrument similarly as in 4.2. The digital control circuitry in the sub-sampling TDA makes the TDA transparent to the inputs during the regeneration time.

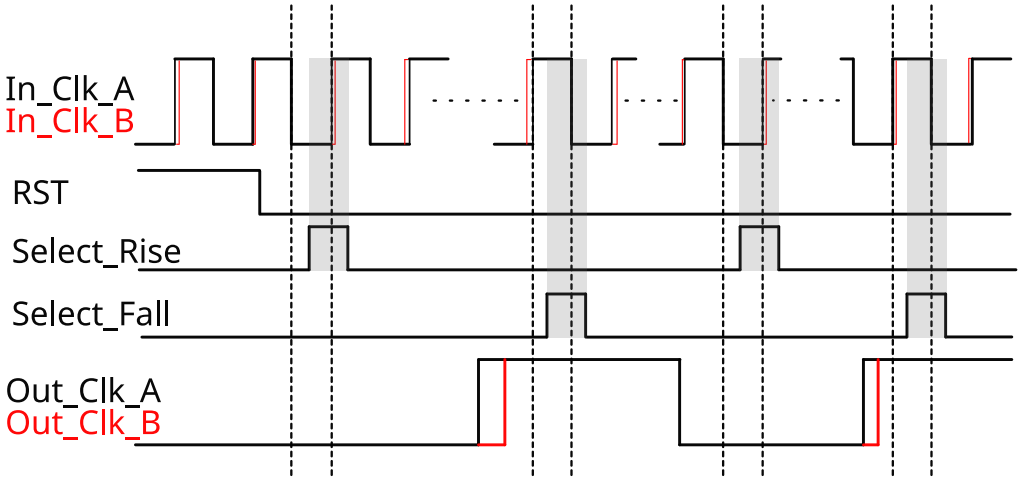


Figure 5.6: Timing diagram of sub-sampling TDA

5.3 Jitter test instrument with modified TDA

The test instrument described in chapter 4 has been modified to include the sub-sampling TDA discussed in this chapter. Fig. 5.7 shows a simplified block diagram of the modified jitter test instrument using the self-referenced technique. The limitation posed by the TDA in scaling up the operating frequency of the SUT into the GHz range is overcome by the sub-sampling TDA as described in Section 5.2.3.

The jitter test instrument takes Input_clk as the Signal Under Test (SUT) and generates a delayed version of itself using the NT Delay block. The SUT and the delayed version are then denoted by In_Clk_A and In_Clk_B for ease of explanation in this diagram. The modified TDA is of the type described in section 5.2.3. The outputs of the sub-sampling TDA Out_Clk_A and Out_Clk_B pass through a Vernier Delay line and the SUT is sampled for rising edges and counted by the Phase Detector and Counter. A histogram is generated using the data stored in the counter. The additional digital circuitry in the sub-sampling TDA takes the inputs In_Clk_A and In_Clk_B for monitoring and generating necessary digital control signals and so never appears in the signal path. The only addition to the signal path because of the sub-sampling TDA is the input latches shown in Fig. 5.5. Since the input latches for both the inputs of the sub-sampling TDA are designed in the same manner, the propagation delays are equal unless there is significant mismatch in the devices forming the latch. Thus in a typical scenario, the signal will not see any delay difference because of the sub-sampling TDA.

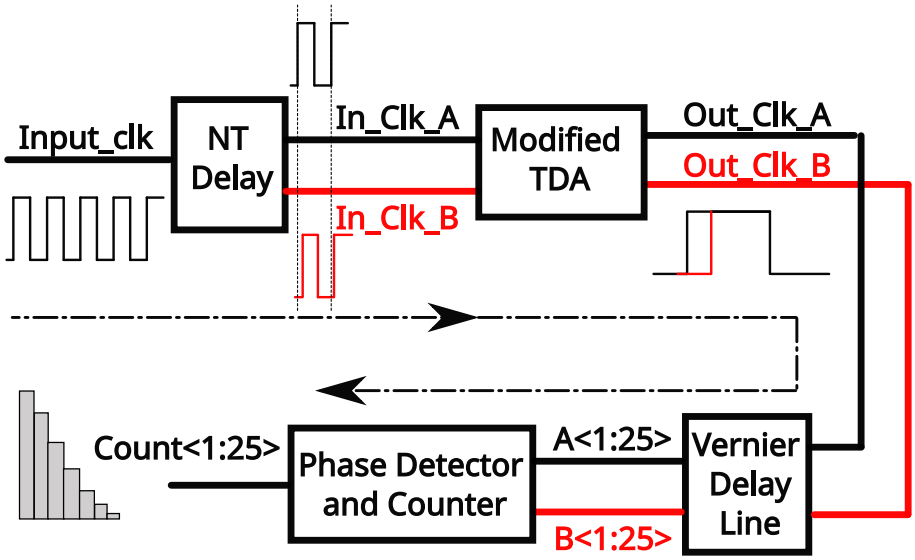


Figure 5.7: Jitter test instrument with modified TDA

5.4 Simulation Results

This Section describes the simulation of the modified jitter test instrument shown in Fig. 5.7 which utilizes the sub-sampling TDA, and reports the results obtained for jitter measurement of signals up to 5 GHz. This instrument is built on the basis of the jitter estimation instrument decribed in chapter 4, where operation at such high frequency is not possible due to limitations in the classical TDA. A clock signal injected with a known value of RMS jitter is fed as input Signal Under Test (SUT) to the test instrument. The jitter histogram is obtained by observing the output of the counter for each of the 25 bins, as described in Section 4.6. Transient simulations have been carried out for a transistor-level implementation of the subsampling TDA in 28 nm FDSOI technology.

An example of simulated jitter histogram generated with a SUT frequency of 5 GHz and an input RMS jitter of 800 fs is shown in Fig. 5.8. The vertical axis of the histogram shows the number of hits for each bin considering the same simulation time per bin. These hits were counted at the output of the phase comparator and form the Cumulative Distribution Function (CDF) from which the Probability Distribution Function (PDF) can be derived to calculate the standard deviation of jitter. Thus, the estimated RMS jitter results in 737 fs, which is in agreement, within the resolution of the instrument, with the expected 800 fs of RMS jitter that was injected into the input SUT.

Simulations were performed at different input frequencies and injected RMS jitter. Table 5.1 shows the simulation results of the estimated RMS jitter at two frequencies of 1 GHz and 5 GHz, demonstrating the feasibility of the modified TDA to operate at frequencies in the GHz range with sub-picosecond resolution.

Table 5.1: Simulation results of on-chip jitter measurement

Input RMS Jitter (fs)	Frequency (GHz)	Calculated RMS Jitter (fs)
500	1	438
	5	440
800	1	733
	5	737

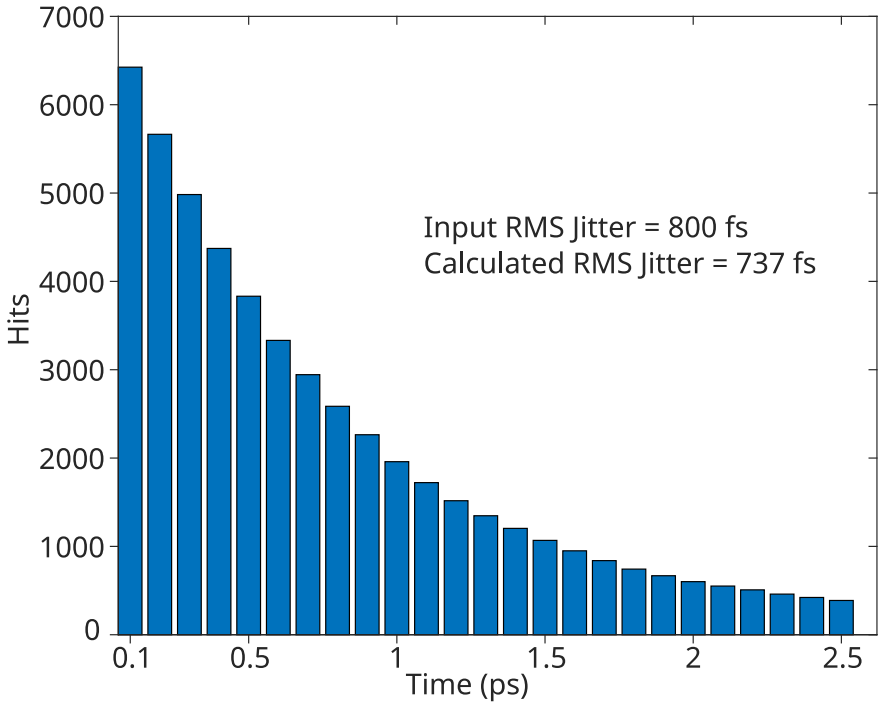


Figure 5.8: Jitter histogram for 5 GHz clock frequency

5.5 Conclusion

This Chapter has presented a novel technique to mitigate the limitations of a high-gain TDA when it is used at GHz frequencies for on-chip random jitter measurement. The trade-off in the TDA between its output regeneration time constant and its gain leads to missing pulses as clock frequency is increased in the GHz range. A sub-sampling TDA has been proposed to overcome these limitations. By actively monitoring the TDA outputs to enable sufficient time for output generation before latching the next input into the TDA, this novelty specifically addresses the limitations in the functioning of the conventional high-gain TDA at high frequencies. The modified TDA is transparent to the input clocks until the current outputs are generated, and the input clock frequency can be scaled up well into the GHz range. The modified jitter test instrument employing the sub-sampling TDA has been described. Simulation results demonstrate the feasibility of a sub-picosecond resolution for jitter estimation for clocks up to 5 GHz.

6

Test-setup measurement

This thesis has been carried out as part of the Nano 2022 program in collaboration between TIMA Laboratory and STMicroelectronics, Crolles. The main goal of this thesis defined following the industry aims is to develop a test instrument with the capability to measure jitter with a sub-picosecond resolution for signals at Gigahertz frequencies and without the use of an external clean clock. This instrument designed in ST 28nm FD-SOI has been fabricated and tests have been carried out via the CIME Nanotech Service in Grenoble. This chapter describes the test environment and the results from the experiments.

Contents

6.1 Prototype of the test instrument

A jitter test instrument designed in STMicroelectronics 28nm FD-SOI has been fabricated and a test environment has been setup for validating the design. The details of the designed test instrument have been described in Chapter 4. The designed instrument is a test prototype and has tuning knobs for calibration and measurement purposes. A first attempt at sub-picosecond resolution with a self-referenced architecture at Gigahertz frequencies includes many challeges with the design of accurate delay elements. Hence a test prototype has been fabricated to evaluate the proposed design. The novelty lies in the usage of the Time Difference Amplifier coupled with a Vernier Delay Line. A simple calibration procedure is required in order to obtain a 25-bin histogram from which jitter can be readily extracted for a quick pass/fail production and on-line test.

The intention is to add the proposed design to an SoC with clock sources implemented by PLLs. This on-chip test instrument takes the clock signal from the clock generation circuitry as the input and generates a pass or fail signal based on the calculated jitter content. As a first step to the development of the on-chip test instrument, a test prototype has been fabricated to evaluate the feasibility of sub-picosecond resolution measurement at the desired frequency range.

In addition to tunability of delay elements in the self-referenced architecture of the test prototype, a digital scan chain register has been included in the instrument. This scan chain allows for programmability of the test chip. There are options to choose the type of calibration, since there are three chains of delay elements in the test-chip. We can also select the required bin number during the histogram generation in the measurement mode as described in Chapter 4.

In order to carry out the test of this instrument prototype, we have considered an external clock source from a high quality signal generator as the jittery clock source. Multiple interface signals have to be generated to support the tunability and programmability added to the test chip. There are also variable bias voltages required for tuning the delay knobs. All of these requirements have led to an elaborate design specification of a PCB. The next few sections in this chapter describe in detail the PCB that houses the test chip and the test environment developed for the instrument test.

Fig. 6.1 shows the layout of the instrument along with a photograph of the fabricated die. A naked die has been used for testing to simplify the test procedure. The test-chip contains two contributions, one of which is the jitter test instrument that has been highlighted. The area of the design is $340x230\mu m^2$ without pads and the total die area is $1205x1187\mu m^2$. The test chip is wire bonded on a PCB that has additional elements for interfacing the die to the test environment. This interface is described in the next section.

6.2 Interface of the test chip

The fabricated test-chip resides on a Printed Circuit Board (PCB) which has been designed to interface the chip to the external instruments required for the testing. The PCB is connected to an FPGA for digital program control, NI DAC for bias tuning, and to the supply and ground voltages. It also connects to the jittery clock source for making the measurement.

6.2.1 PCB for testing

A PCB with the block diagram shown in Fig. 6.2 has been designed to provide an interface between the jitter instrument and the test environment. KiCad software has been used to design the PCB. As shown in the block diagram description, the top portion of the PCB has jumper connections for the Voltage supply and ground. Decoupling capacitors placed on the PCB help

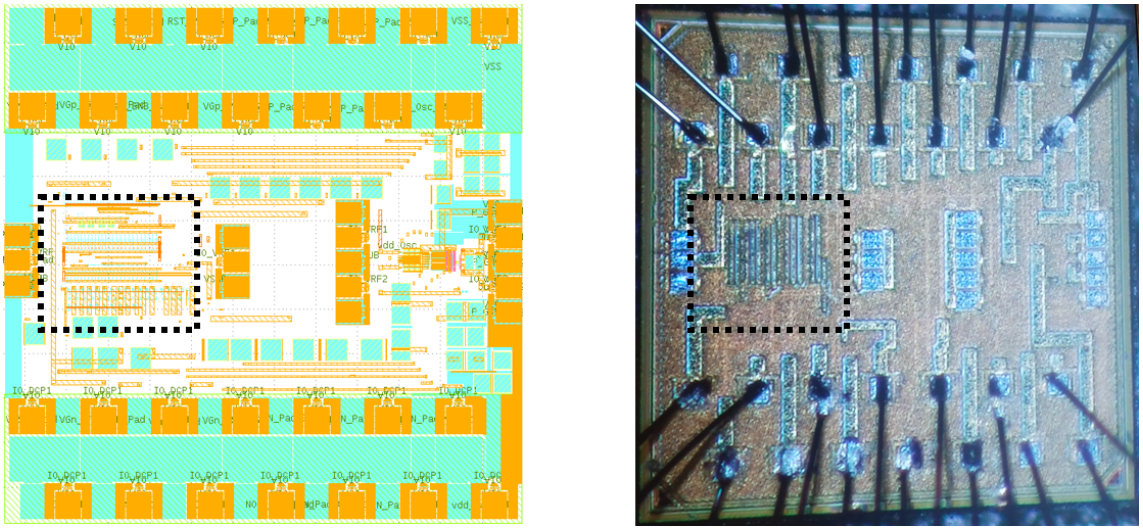


Figure 6.1: Jitter test instrument : (a) layout, and (b) photograph of the fabricated die showing wire bonding

with any surcharge during power up and down of the test chip.

The die with the instrument sits in the middle of the board with the orientation shown in Fig. 6.1. The RF signal to be measured is provided via the RF probe in the left side of the PCB.The layout of the PCB is shown in Fig. 6.3. The bottom left of the PCB houses level shifters with part number $NLSV2T244$. This is a $2-$bit configurable dual-supply voltage level translator. The level shifters are needed to convert the $3.3V$ digital program signals coming from the FPGA board into the $1V$ domain of the jitter test instrument. The digital output of the test chip is converted back to $3.3V$ by another level shifter and sent back to the FPGA for further processing. The FPGA that provides the digital control signals required for the operation of the instrument is on a *Basys*3 board and this interface is described in detail in section 6.2.2. The bottom right part of the PCB has connectors to a National Instruments (NI) Data Acquisition board (DAC). The test instrument requires multiple bias voltages for tuning the delay elements that form the core of the instrument, and the NI DAQ is used for this purpose. Section 6.2.3 describes the details of interface to the NI DAC.

6.2.2 FPGA interface for digital control

The test instrument requires a set of 4 input digital signals for controlling the various operational modes of the jitter BIST. These signals are the START, SHIFT, TDI and TCK and they are provided by the programmed FPGA.

Fig. 6.4 shows a diagram of the test chip with the various signals that form the interface between the instrument and the test environment. The output signal TDO is observed on the oscilloscope. In addition, the TDO from the test chip is sent back to the FPGA via another level shifter at the output. This helps to monitor the test-chip output from the FPGA if needed for further processing.

The 'TCK' is a low frequency digital clock for the scan chain shift registers. A combination of START and SHIFT help to program the scan chain in various modes. The TDI is a 1-bit wide digital input pin to serially load the scan chain with the required program sequence. A VHDL code has been written to generate the required sequence of these 4 program control signals. The code has separate sections for generating the low frequency TCK and the combinatorial logic of the digital signals. All signal values are updated on the falling edge of TCK. This works well for the positive edge triggered scan-chain as the digital signal is ready for the test-chip at the next rising edge. This takes care of any setup and hold-time requirement of the signals. Table 6.5 lists

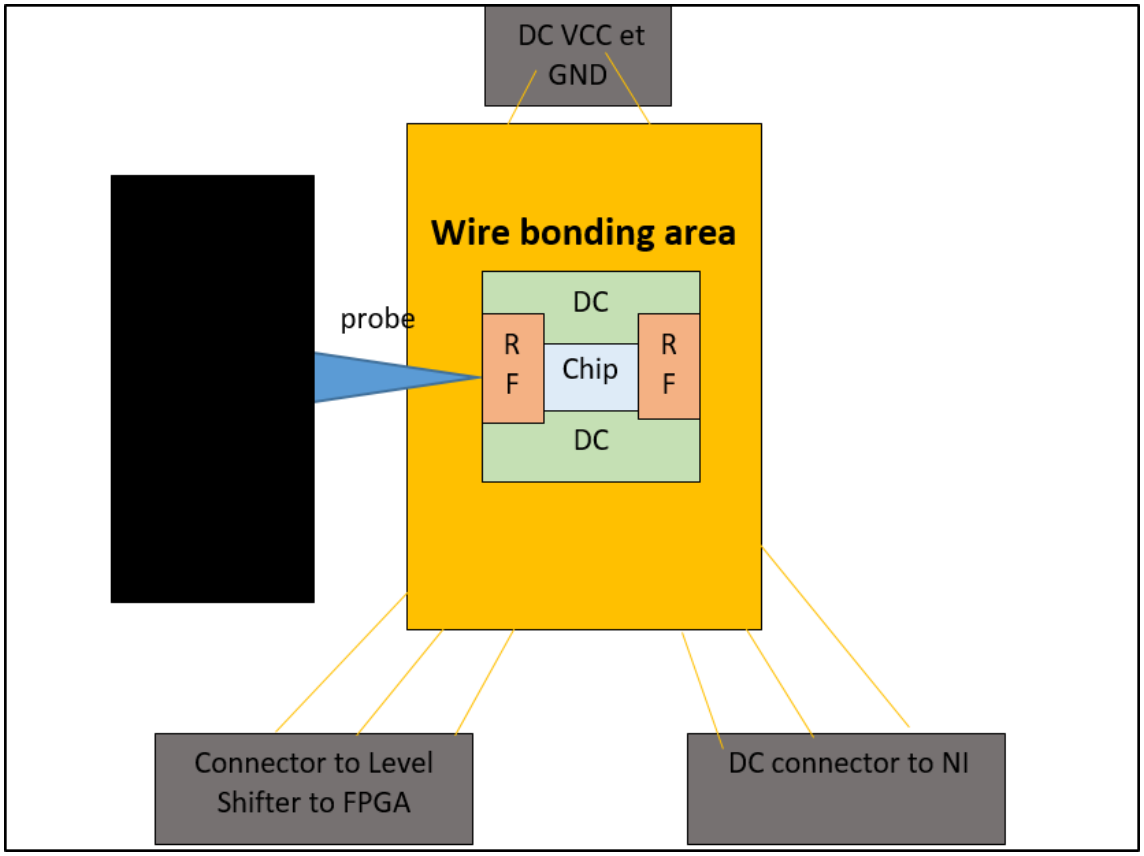


Figure 6.2: Description of blocks in the PCB

the values and functionality given by these control signals.

The START and SHIFT control pin combination internally generates the four modes of operation as defined below in Table 6.6.

The following sequence of control signals needs to be generated for running a single test (calibration/measurement) sequence:

1. Initial Reset mode
   (a) Internally all the counters and shift registers are pulled down to ground and the shift registers now read a value of '0'.
   (b) Denoted as $Currentstate = '0'$ in the code
2. Scan-in mode
   (a) TDI pin is given the required order of digital bits to conduct the required test procedure of either calibrating the delay lines or looping through the bin numbers for histogram generation
   (b) Denoted as $Currentstate = '1'$ in the code
3. Run mode
   (a) The dedicated counters start running and count the cycles for a given duration. This duration is specified in the code and hence this time can be accurately controlled and programmed.
   (b) Denoted as $Currentstate = '2'$ in the code

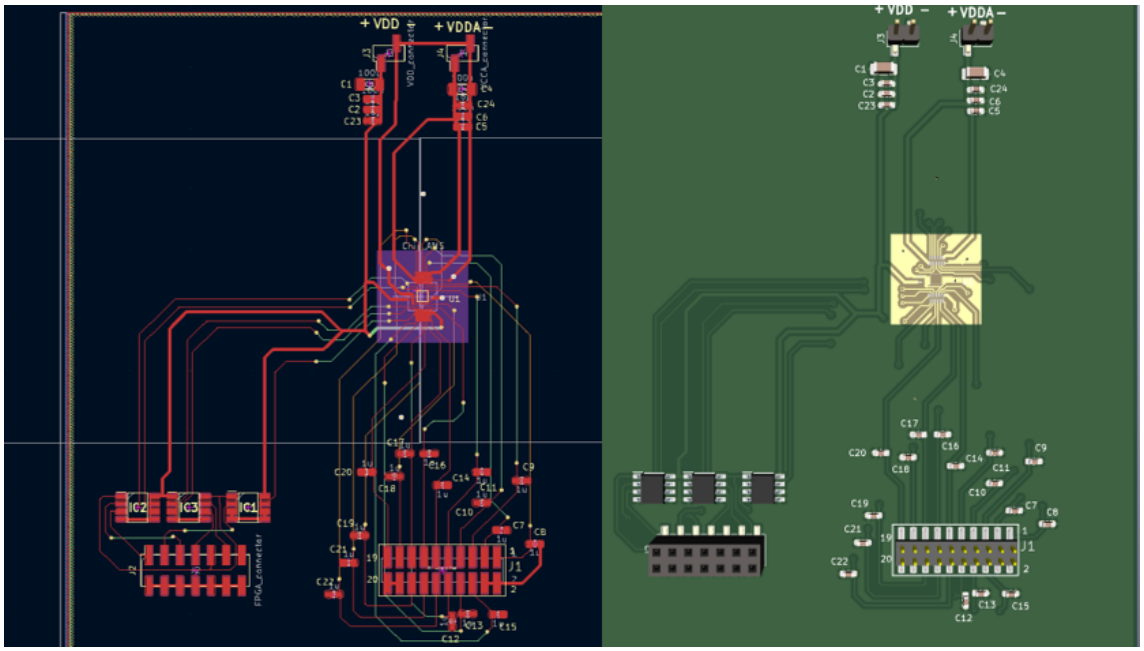


Figure 6.3: Layout of the PCB showing the different blocks

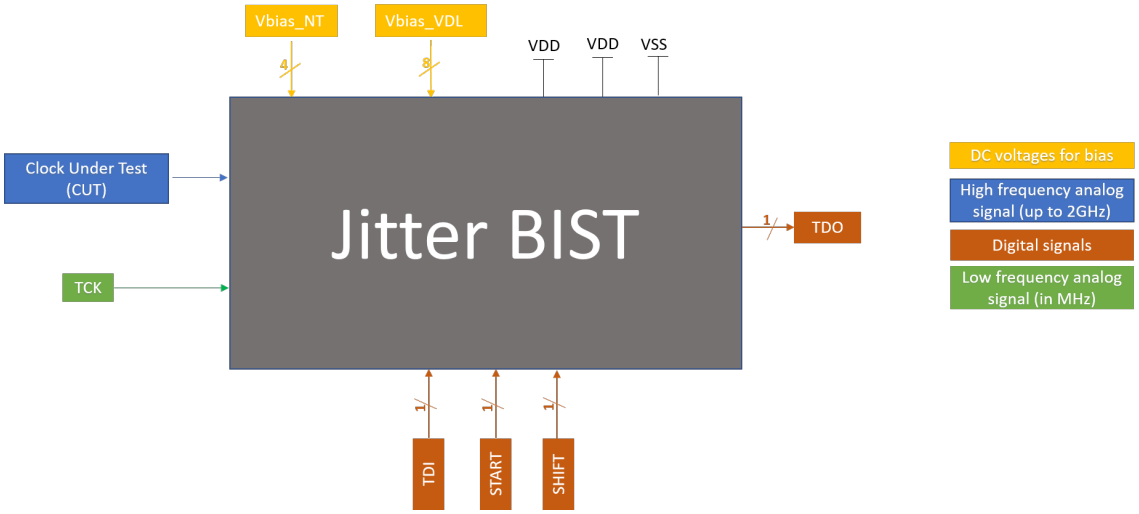


Figure 6.4: Interface to test-chip

Signal	Values	Definition	Direction for the test instrument	Pin on the FPGA board
START	1 : Start operation and start counters 0: Stop operation, stop counters and wait for load signal.	Gives a START/STOP functionality to all operations to measurement procedures run by the instrument.	Input	JB4
SHIFT	1: Shift the scan register bits from left to right. Output can be observed at the TDO pin 0: Load the counter values onto the Shift registers	Control pin to either load the counter values onto the shift register or to shift the values in the scan chain towards the TDO.	Input	JB3
TDI		Input pin for the shift registers	Input	JB2
TCK		Low frequency clock signal (1-10MHz) for clocking the Shift registers	Input	JB1
TDO		Output pin for observing the values from the shift registers	Output	

Figure 6.5: Digital program control

START	SHIFT	Definition	Comment
1	1	Reset mode	Internally generated reset, sets all the counters and shift registers to 0
0	1	Scan-in/Scan-out mode	TDI pin is active and receives and scans in the control bits. During scan-in mode, serial bits sent in through TDI. During Scan-out mode, TDO pin is observed to see the values stored in the scan registers
1	0	Run mode	The operation specified by the scan chain starts, the counters (either the calibration or the measurement counters) start counting.
0	0	Load mode	The operation in progress during 'Run mode' is stopped and the counter values are loaded onto the Shift registers.

Figure 6.6: Truth table for test sequence

4. Scan-out mode

   (a) TDI pin is continuously fed with a value of '1' and the shift registers contents are shifted out into the TDO.

   (b) Denoted as $Current state = '3'$ in the code

This sequence programmed in the FPGA can be observed in the diagram shown in Fig. 6.7. A VHDL program has been written to achieve this functionality. A Basys3 board from Xilinx has been used that supports digital development based on Artix-7 FPGA and is shown in Fig. 6.8. Out of the 3 PMOD ports available, the port JB has been used for the control signals.

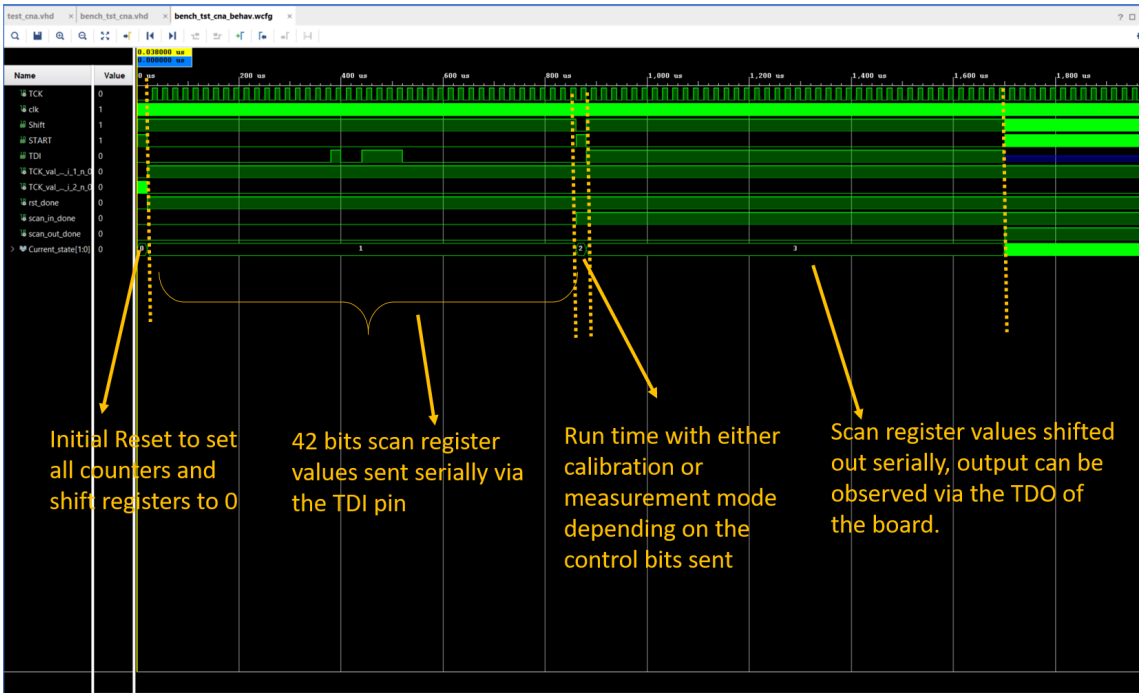


Figure 6.7: Test sequence generated by FPGA

6.2.3 NI DAC for providing the bias voltages

The test chip requires 12 bias voltages as shown in Fig. 6.4. The NI-9264 DAC from National Instruments shown in Fig. 6.9 is used to provide these bias voltages. It has 16 analog output channels, and we use a DSUB type of connector to connect these outputs to the PCB. Out of the 16 channels, 12 are used for the test instrument according to Table 6.10.

Python scripts have been written to remotely control the NI DAC voltages as required for the tuning. The resolution of the DAC allows for control in tens of microvolts range which helps explore a wide range of possible bias voltages. This ensures that a precise calibration can be achieved.

The delay elements designed in ST 28 nm FD-SOI allow for a variability of 1ps of delay/V. Hence the NI DAC supports this range of tunability.

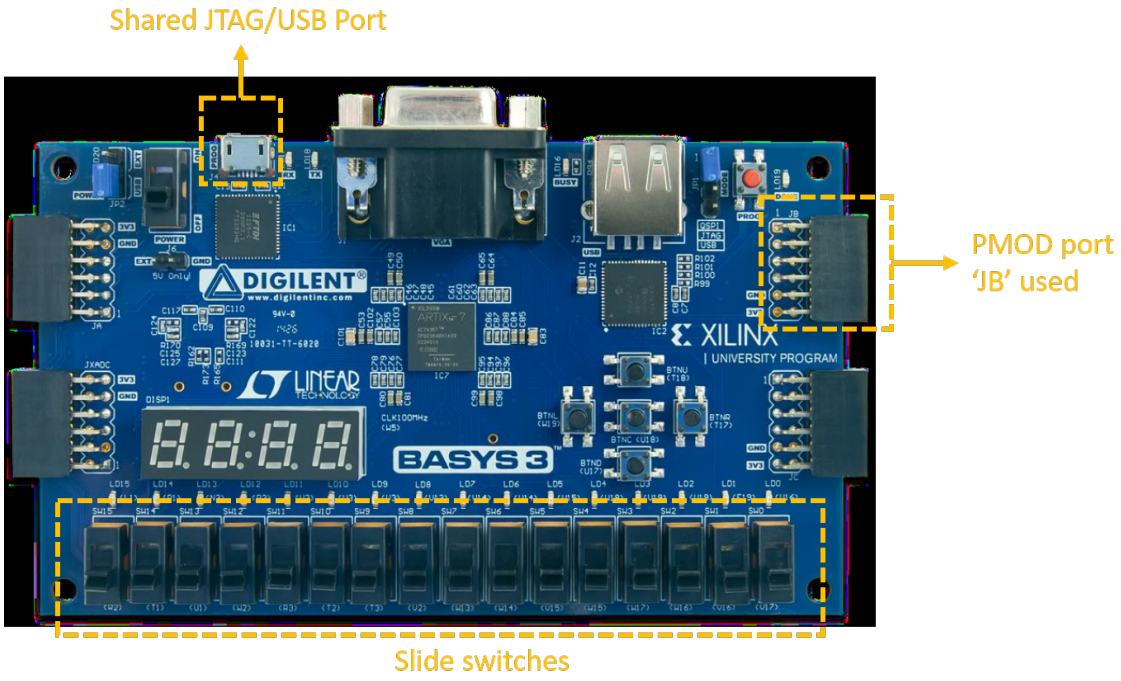


Figure 6.8: Basys3 FPGA board

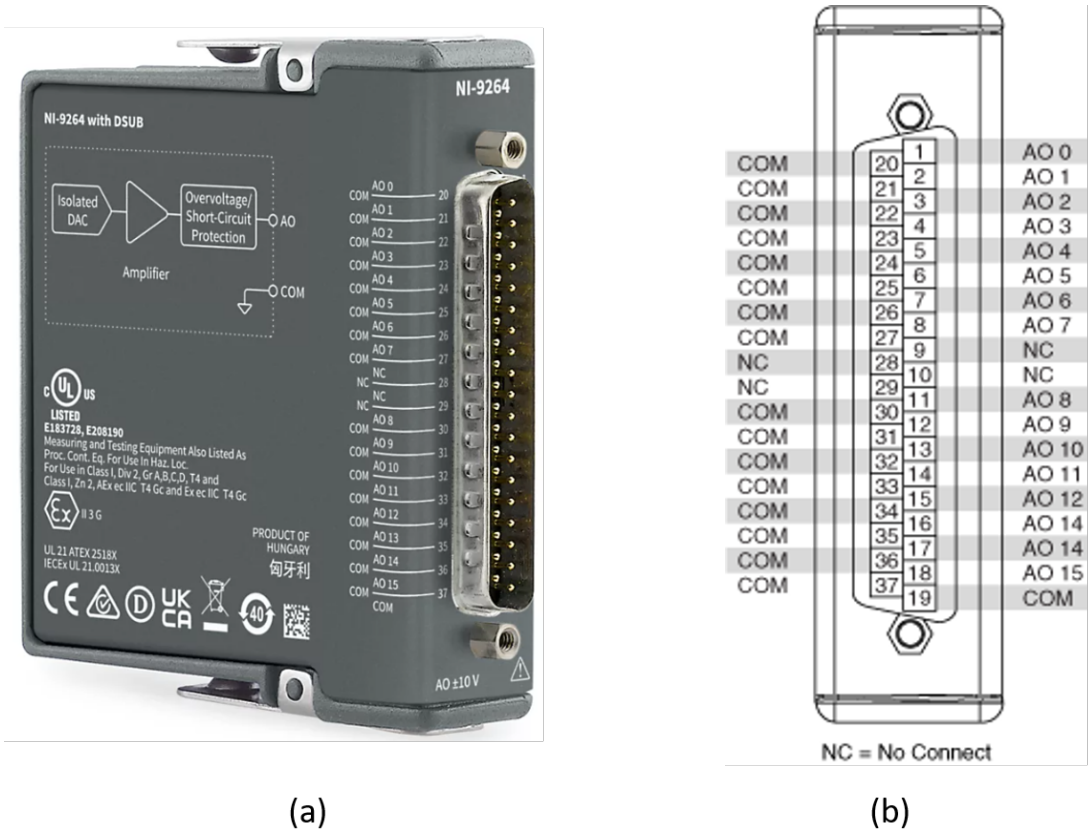


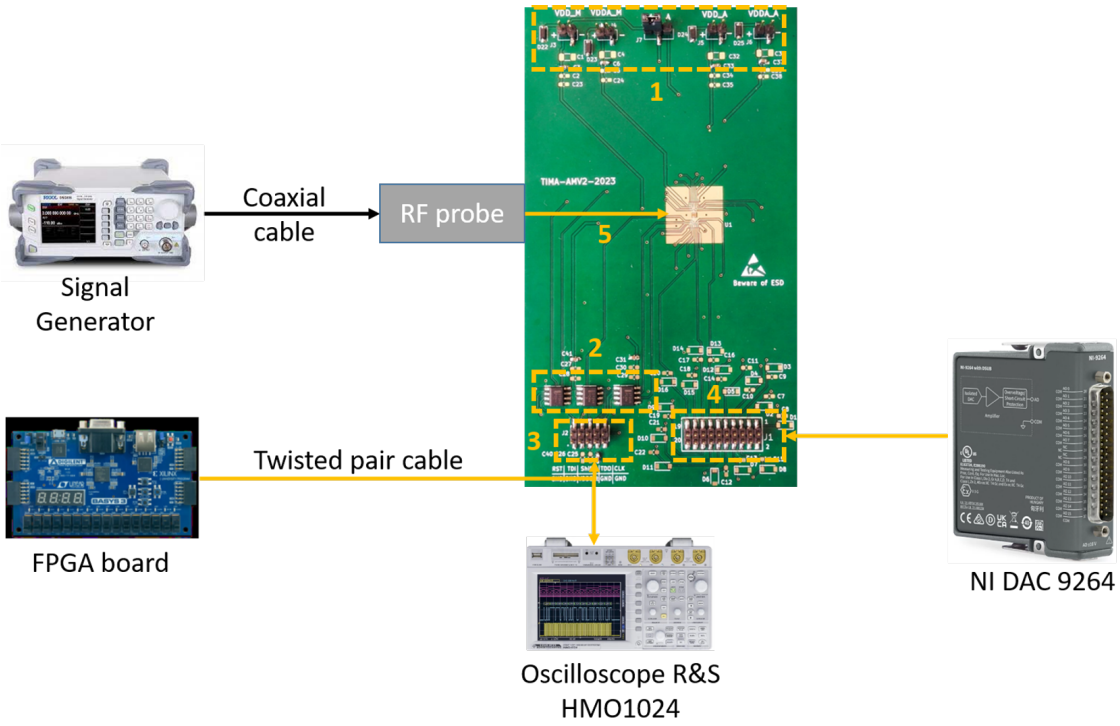
Figure 6.9: NI DAC 9264: (a) DAC with DSUB pins, and (b) DSUB pinout

Pin Number DSUB-37 NI 9264	Name of DC signal of module NI-9264	Name of signal DC on Chip
1	AO00	VBN_VDL_A
2	AO01	VBN_NTdelay
3	AO02	VBN_VDL_B
4	AO03	x
5	AO04	x
6	AO05	VGN_NTDelay
7	AO06	VGN_VDL_A
8	AO07	VGN_VDL_B
9	x	x
10	x	x
11	AO08	VGP_NTdelay
12	AO09	VGP_VDL_A
13	AO10	VGP_VDL_B
14	AO11	VBP_NTdelay
15	AO12	VBP_VDL_A
16	AO13	VBP_VDL_B
17	AO14	x
18	AO15	x
19	COM	VSS
20	COM	VSS
21	COM	VSS
22	COM	VSS
23	COM	VSS
24	COM	VSS
25	COM	VSS
26	COM	VSS
27	COM	VSS
28	x	x
29	x	x
30	COM	VSS
31	COM	VSS
32	COM	VSS
33	COM	VSS
34	COM	VSS
35	COM	VSS
36	COM	VSS
37	COM	VSS

Figure 6.10: Pin correspondence for NI DAC

6.3 Test environment for the instrument

The test setup consists of the PCB and all the other external instruments for providing the analog and digital inputs for the measurements. A diagram to illustrate the connections is shown in Fig. 6.11 with a description of the instruments and connection directions. The tests have been carried out in the CIME Nanotech Service. A photograph of the complete test environment can be seen in Fig. 6.12.



Number	Definition
1	Voltage supply and
2	Level shifters for the FPGA
3	Connector pins for signals coming from FPGA
4	Connector for NI DAC
5	Probe to connect to the GSG pad on the test chip

Figure 6.11: Diagram of the overall test setup

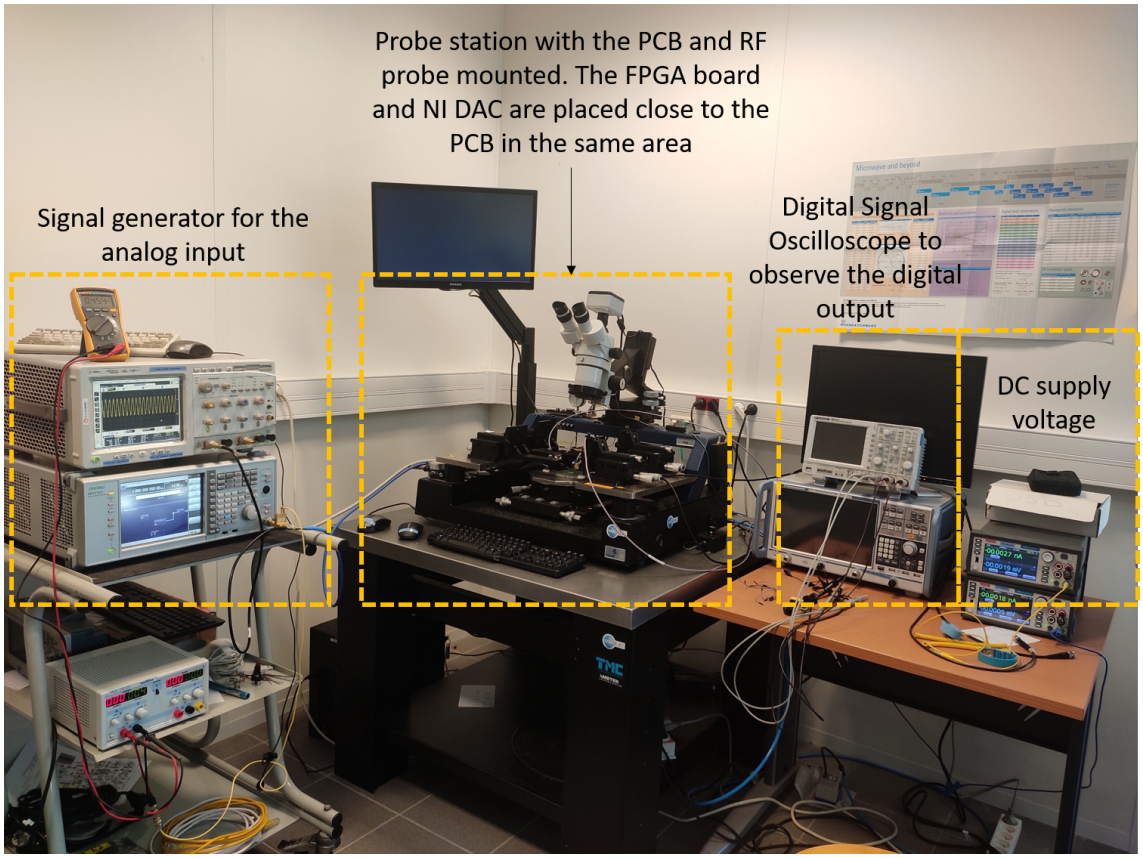


Figure 6.12: Test environment

6.4 Measurement methodology

The test procedure can be divided into calibration and measurement modes. The calibration procedure starts with the NT-delay calibration. The delay elements have to be calibrated to generate a delayed clock. The delay must precisely be an integral number of clock period delays. This delayed clock acts as the reference clock for sampling and any error in the calibration will lead to the histogram shifting far to the right or left and in the worst case would not be captured at all. For the calibration, the NT-delay is configured as a ring oscillator and the time period is measured with a counter. The detailed procedure to calibrate the NT delay is given in the flow chart in Fig. 6.13.

The next step is the calibration of the Vernier Delay Line. The procedure for the calibration of the delay elements is similar to the calibration of the NT delay. We proceed with calibration of the first delay line consisting of 25 elements to a nominal value. The first delay line is configured as a ring oscillator and the time period is measured. The next step is to calibrate the second delay line such that the measured ring oscillator period exceeds the time measured by the first delay line by $25 * (Vernierdelay)$, considering that there are 25 elements in the delay lines. As an example, if the desired Vernier delay is $10ps$, then if the first delay line is calibrated to give a total delay of $2.25ns$, then the second Vernier line should be calibrated for a delay of exactly $2.5ns$. Care should be taken such that the first delay line should be biased in such a range that the second delay line is not forced to come out of saturation to achieve the delay difference. The corresponding flowchart for the Vernier delay calibration is given in Fig. 6.14 and Fig. 6.15, where the two delay lines are named 'VDL_A" and 'VDL_B". The flowchart demonstrates the procedure for a 10 ps Vernier delay.

Once the calibration has been completed, we proceed to the measurement mode, by sending the

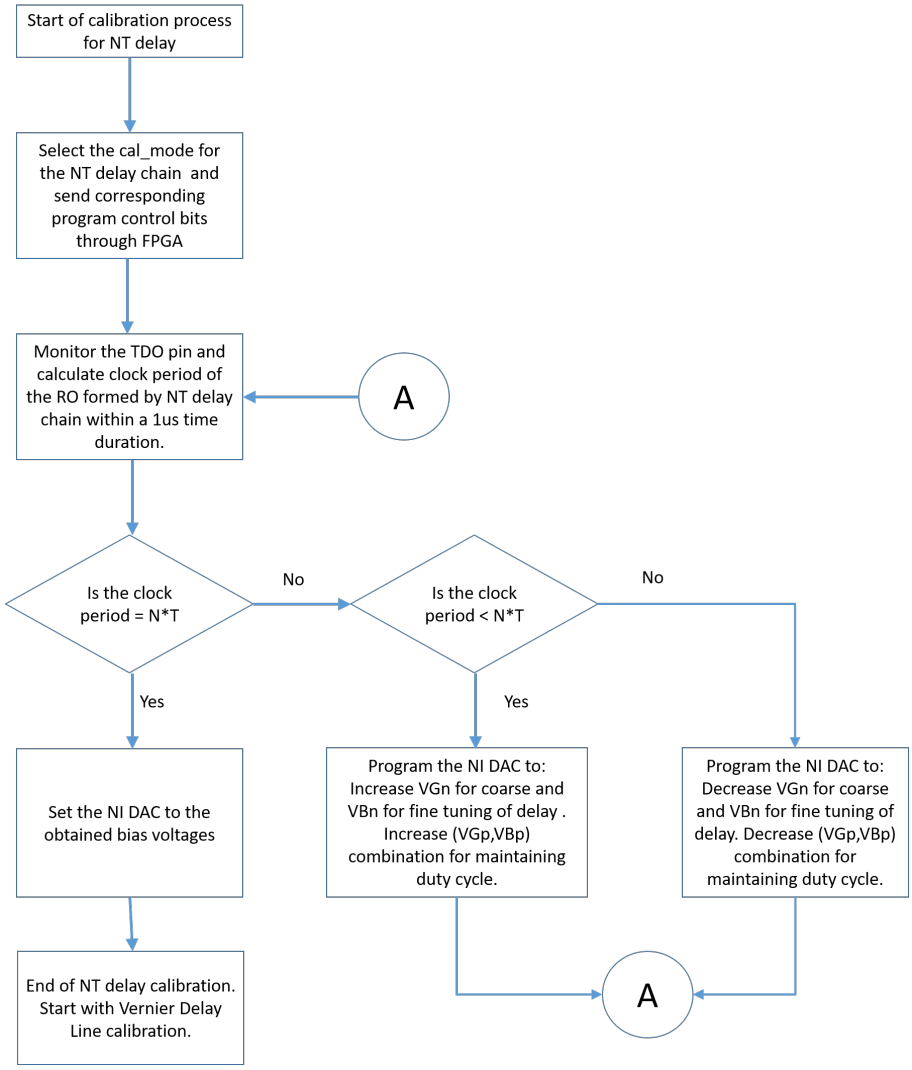


Figure 6.13: Flow chart for NT delay calibration

appropriate bits to the scan chain. By choosing the bin number from Bin-1 to Bin-25, we collect the data from the TDO to generate the histogram. From the histogram which is the Cumulative Distribution Function, a PDF (Probability Distribution Function) will have to be generated and then the curve will be fitted to derive the root mean square value of the random jitter of the clock under test. The procedure for histogram generation has been described in Section 3.4.2.

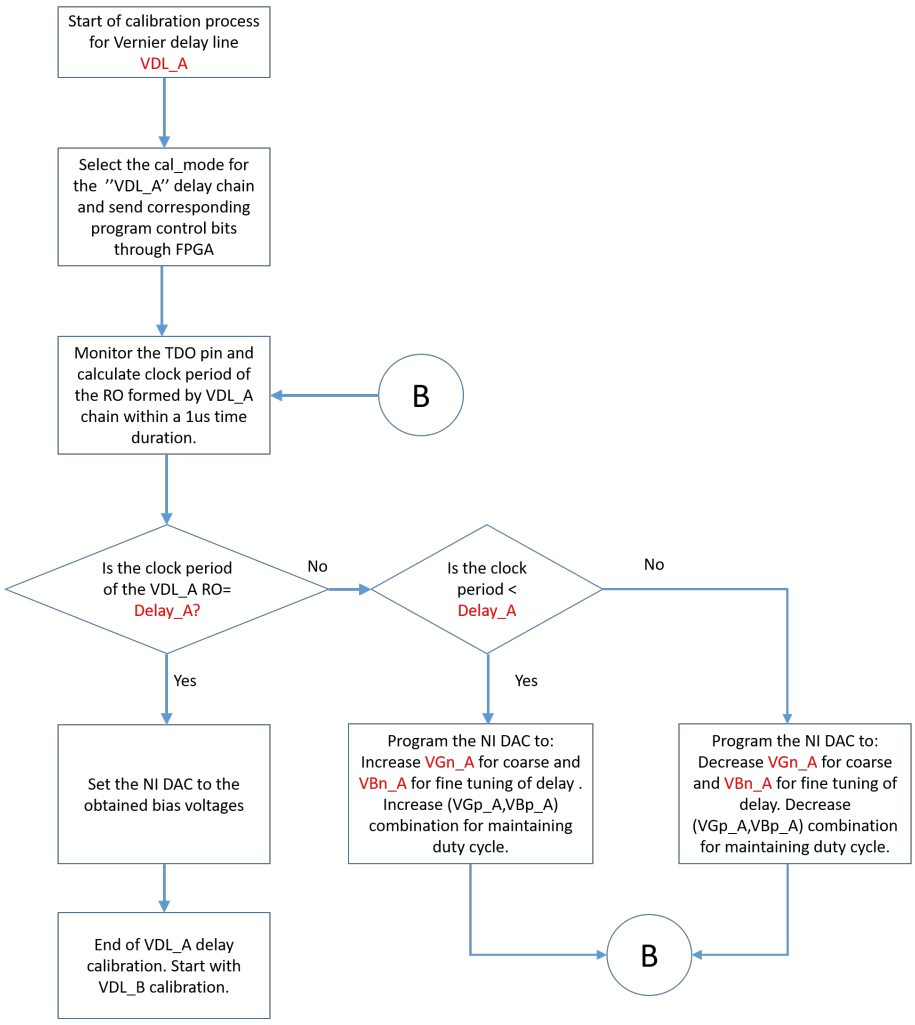


Figure 6.14: Flow chart for VDL A calibration

6.5 Experimental measurements and results

Experiments were carried out in the CIME Nanotech Service with the test environment described in the previous section. As part of the test procedure, the code written in VHDL for the generation of the digital control signals and implemented on the FPGA as described in Section 6.2.2 has been verified. As part of the test sequence, a combination of START and SHIFT signals are given for scanning in the program control and setting the control bits that are necessary for carrying out any test, while selecting between calibration and measurement modes.

As shown in the control bits of Table 6.5, the shifting of data in and out of the test registers and the loading of the test registers with the counters data is all expected to be carried out with the SHIFT signal. This was done in order to limit the number of circuit pads. SHIFT=1 is considered for scanning in the binary bit sequence for program control at the same time that the data in the registers is scanned out, while SHIFT=0 implements the LOAD operation for loading the counter values onto the test register once the iteration has completed. Thus both of these modes are controlled by the same pin. SHIFT and LOAD signals are not generated independently of each other, but they are derived as an inverse of the other since at a given time we either shift bits into the chain or load the counter values onto the scan chain for reading the output.

Unfortunately, the usage of a single pin corrupts the values loaded into the scan chain register. When the LOAD signal is being derived out of the SHIFT signal sent by the FPGA, there comes a time instant when the counter values loaded onto the shift register can be corrupted. This leaves

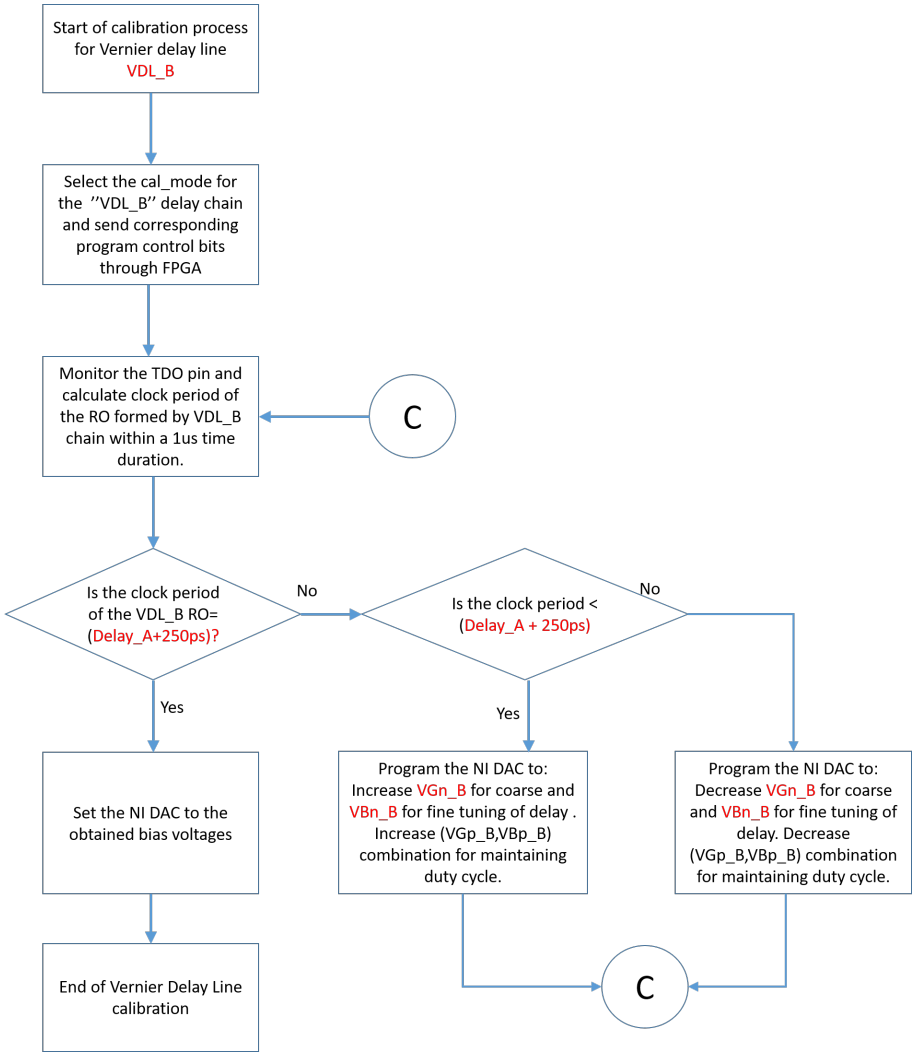


Figure 6.15: Flow chart for VDL B calibration

us to miss out on the actual counter value that has to be read out. Since the entire output has been derived as a set of binary values coming out serially via the TDO pin, we have been unable to read a single valid measurement at the TDO pin, while the SHIFT operation on its own is functional. The usage of a single pin for SHIFT/LOAD functionality was verified by simulation with a fast value of the transition time from SHIFT=1 to SHIFT=0. Since there is a practical maximum limit to the transition time of digital signals sent by the FPGA and received at the transistor gate inside the shift register, this functionality of SHIFT/LOAD could not be correctly executed. This design error cannot be corrected as it is related to the digital hardware that was full custom designed.

The design error could be addressed by having the entire digital portion implemented by synthesis of a HDL (Hardware Description Language) code. The digital portion consists of the scan chain registers and counters. This synthesized code will have to be interfaced with the analog portion of the test chip with a separate pin for the SHIFT and LOAD functionality, thereby overcoming the error observed in the current hardware. The new test chip will also include the circuitry for the sub-sampling TDA as a separate portion that can be tested and verified.

6.6 Conclusion

This Chapter has described the overall environment for the testing of the jitter instrument. Efforts have been made to introduce automation wherever possible in the test environment. Unfortunately, because of a design bug described in the previous section, no hardware jitter measurements could be carried out. Work is underway towards fabrication of another version of the test chip with the corrected design bug.

7 Conclusions

This research work was carried out with the aim of developing an instrument to measure clock jitter with sub-picosecond resolution for signals in the Gigahertz range. In the framework of the Nano 2022 project and in collaboration with STMicroelectronics, Crolles, an instrument was designed and fabricated using the ST 28nm FD-SOI technology. This final chapter of the document summarizes the contributions of the research work. Some perspectives about the scope of future work are also presented in this chapter.

Contents

7.1 Thesis contributions

In the on-going effort towards Internet of Things (IoT), wearable technology, Virtual Reality, etc, where more and more devices are being interconnected, design of high-speed ICs which offer simultaneous and seamless connectivity between multiple devices becomes necessary. The requirement of seamless connectivity between devices translates to high-quality or error-free data transmission and reception. This in turn sets the need for a very low BER (Bit Error Rate). For example, [35] talks about a SERDES link having a BER as low as 10^{-15}. Additionally, high data throughput is also needed to support the data transfer speed requirements for these applications. Throughput in the range of multiple Gigabits per second has become commonplace. The clock signals for such high speeds usually fall in the Gigahertz range.

Need for jitter measurement and associated challenges

An essential requirement of any high-quality communication system is a jitter-free clock signal, which can provide a periodically occurring time reference for processing of data transmission and reception. At the same time, a jitter-free clock signal is an ideal case scenario, as clock generation circuitry or clock recovery circuitry as the case maybe have transistors which inherently introduce thermal noise during their operation. The high-speed ICs commonly use switched regulators for low power and higher efficiency, the operation of which could lead to very low frequency periodic jitter because of the coupling of switching noise in the presence of parasitics. As most data transmission systems make use of digital signal processing for ease of data manipulation, high-speed digital circuitry resides close by their analog counterparts on SoCs. The transmission and reception involve analog and sometimes RF (Radio Frequency) circuits, while data manipulation is majorly carried out in the digital section. In such an SoC, switching noise in a closely located digital element could also get coupled onto a highly sensitive signal in the clock generation circuitry causing a shift in the amplitude levels. This can also appear as jitter because of fluctuations in the threshold crossing. All these commonly found sources of jitter can also co-exist in an SoC leading to a composite jitter profile.

The design of systems with a very low BER requires a very well thought out timing budget, where jitter and delay contribution from all the blocks in the communication link is accounted for. A few picoseconds or even lesser is the jitter tolerable. The measurement of clock jitter is therefore essential in the design and validation process of a high quality high-speed IC. At the same time, it is also challenging to measure jitter accurately at a high resolution for clocks in the Gigahertz range because of the complexity involved in the design for high-frequency operation. Additionally, in the case of composite jitter, the analysis and measurement starts with decomposition of jitter into random and deterministic components. The random jitter content is quantified by its statistical properties given its unbounded nature which usually follows a Gaussian distribution. On the other hand, the bounded deterministic jitter is quantified by its minimum and maximum value and where applies, the frequency and amplitude of the periodic jitter component.

The process of jitter measurement in itself has therefore been an ongoing topic of research in both the industry and academia. Complex external equipment like spectrum analyzers are available in the market that provide a detailed jitter profile. These equipments are also expensive as the signal being analyzed has to be broken down into its frequency components and then analyzed for jitter. This requires collection of many samples which in turn needs memory and highly accurate signal processing circuitry. Time domain measurements of jitter are also possible using an oscilloscope. By collecting information of signal transitions and creating an eye-diagram, the jitter in the signal can be analyzed. Data processing algorithms and signal processing circuitry for these external equipments have been a complex research topic. While significant progress has been made in jitter measurement using external equipments, the very process of tapping high speed clock signals from SoCs can lead to inaccuracies in the measured data because of RLC effects. Additional

planning during the layout phase has to be carried out for routing these high-speed signals out onto the IC pad before it can be tapped for measurement. Therefore it adds to the timing and area cost involved during jitter testing. In the case of post-production maturity testing of SoCs (System on Chip) having one or multiple PLLs (Phase Locked Loop) for example, huge number of ICs have to be validated with jitter data to qualify them as a 'pass' or 'fail' category. Jitter measurement using external equipments is hardly feasible in such cases. A solution to the above mentioned bottlenecks is the use of on-chip jitter measurement circuitry

On-chip jitter measurement

On-chip jitter measurement, as the name implies is an additional circuitry on the chip that takes the clock signal as an input and generates the jitter information as output. As this circuitry resides within the same IC as that of the clock generator, tapping of clock signal becomes easier as it is just an additional routing from the clock generation circuitry to the test circuitry, and by careful layout planning, the instrument and the clock generator could be located close-by avoiding loss of slew rate due to capacitive nature of metal trace.

The measurement of jitter in the time domain in the on-chip instrument is done by repeatedly sampling the clock Signal Under Test (SUT) to collect timing information of the occurring clock edge. Most systems use a rising clock edge for generating a timing reference with a few exceptions like a Bang-Bang Phase detector where both rising and falling clock edges are used as a timing reference. In the presence of clock jitter the occurrence of the rising clock edge is no more strictly periodic and hence by repeated sampling of the rising clock edge, a Probability Distribution Function (PDF) or the histogram is generated. Mathematical computation from the histogram can give an estimate of the jitter content in the signal.

Objective of thesis work

In the implementation of on-chip jitter measurement, there arises two possibilities - one where an external clock reference is used for the sampling, where both random and deterministic jitter measurement is possible. The circuitry is simplistic with a latch for sampling and a counter for generating the histogram. This advantage is offset by the necessity to have a clean or a jitter-free clock reference for the sampling. Another disadvantage is the need for additional pad and routing for tapping in the external clock reference without adding any noise. There could also be signal degradation in the external clock once it is tapped as it has to traverse the additional routing from the source through a capacitive pad and metal routing until the latch. The other category of on-chip measurement is the self-referenced topology where a delayed version of the SUT is used for the sampling and histogram generation. This architecture does away with the need for an external clock. The clock signal from the generation circuitry on the SoC can be directly routed to the on-chip jitter measurement circuit without the need for any external signal for measurement. The SUT and its delayed version pass through a series of delay elements that form the bins of the histogram. For each bin, the SUT is sampled by its delayed version and the jitter computed from the histogram. Hence additional circuit elements are needed in comparison with the externally referenced alternative. In addition, as each rising edge in the SUT is being sampled by its adjacent or closely located edge, only high-frequency jitter content is captured in the histogram. After a careful consideration of the advantages and disadvantages of both categories of on-chip measurement, a self-referenced architecture has been chosen for this research work. This also aligns with the interest of STMicroelectronics that requires on-chip jitter measurement without the need for external clock.

Thus, an on-chip jitter test instrument using a self-referenced architecture that can estimate the random jitter content of a clock signal in the Gigahertz range with a sub-picosecond resolution was chosen as the objective of this thesis in order to make a meaningful and relevant contribution in the area of research. The reasons can be summarized as follows:

- Tolerable jitter for clocks in Gigahertz range is a few picoseconds - this sets the range of jitter to be measured and the input clock signal frequency
- Jitter needs to be measured accurately for working with a better timing budget. Accurate measurement also needed for post-production maturity testing - this forms the specification for the required resolution of measurement.
- The self-referenced architecture lends itself to a fully on-chip implementation without the need for any external signal for jitter measurement. This simplifies the additional circuitry required for tapping the SUT and making a measurement.

7.1.1 Features and contributions of proposed instrument

In concurrence with the objectives of this thesis, a test instrument to measure jitter was designed in ST 28 *nm* FD-SOI and sent for fabrication in the PANDA run during 1S of 2022. The instrument designed can be described by a simplified block diagram which has been described in Section 3.4.2 and reproduced here for convenience. The following are the features that introduce novelty and make a contribution towards the design of on-chip jitter measurement using a self-referenced architecture:

1. The use of tunable delay elements for implementing all the delays required in the self-referenced architecture.
    - The delay element described in [9] demonstrates coarse and fine tunability using front gate and back gate bias. Hence this aids is precise tuning to achieve desired delay values. Delay slope of almost $1mV/ps$ have been observed by simulation.
    - The self-referenced architecture uses delay elements for both generating the NT-delay and for delaying the SUT for sampling across the histogram bins. By using the same delay elements for designing all the delay blocks, the broad tuning range of the delay element has been well utilized. This also simplifies the design effort. The coarse tuning range is within $1V$, but the fine tuning range is between $(-3,3)V$.
2. Use of Vernier Delay Line (VDL) for sampling the SUT across the histogram
    - Vernier delay structures have been typically used in Time to Digital Converters for robustness to mismatch variations.
    - By designing a Vernier delay line using tunable delay elements, there is an added advantage of highly tunable and yet robust delay elements that helps achieve high resolution.
    - Simulation results have shown that the Integral Non Linearity (INL) of a 25 element VDL with a Vernier delay of 10 ps fluctuates between 4 ps and the maximum linearity error is about 2% referred to the full delay of 250 ps.
3. The use of the Vernier Delay Line in combination with a TDA can support sub-picosecond resolution at Gigahertz frequency.
    - The Vernier delay line with the tunable delay elements when used together with the TDA has multiple advantages.
    - The design constraint of a sub-picosecond delay of the VDL elements is relaxed and the required delay is a product of the desired resolution and the TDA gain.
    - With a TDA gain of around 100, to achieve a sub-picosecond resolution of around 100 fs, it is sufficient to have Vernier delays in the range of 10 ps and this value has been demonstrated to be robust to mismatch variations that exist after calibration.

4. A single shot fully on-chip calibration scheme.

    - The calibration of the the delays for generating the entire histogram can be achieved by using a single cycle of calibration.
    - By connecting the entire Vernier delay line in the form of a Ring Oscillator (RO), all the delays required for generating the histogram are calibrated in the same cycle. Each individual delay element corresponding to a unique bin in the histogram need not be calibrated separately and this saves time to test.
    - As all the components of the calibration reside on the same chip with only the control signals provided externally, a fully-on chip calibration scheme has been proposed.

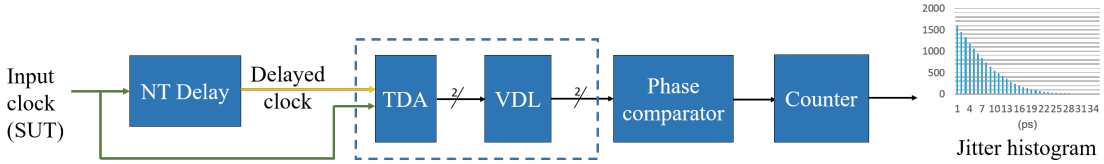


Figure 7.1: Simplified block diagram of the proposed test instrument

7.1.2 A summary of the thesis work

A careful study of the state of the art for on-chip jitter measurement was carried out owing to the need for jitter measurement with high accuracy. A comparison between the on-chip measurement techniques of externally referenced and self-referenced technique was done and evaluation was carried out by system level simulations performed in Matlab. Finally, a self-referenced architecture was chosen and the research direction also aligned with the interest of the Nano 2022 project from STMicroelectronics.

The technology used for the implementation of this instrument is the 28 *nm* FD-SOI from ST. In order to achieve the objective of the thesis work and to make a contribution to the field, few novelties were introduced which have been outlined in section 7.1.1. Chapters 3 and 4 elaborate further on the system level modelling and transistor level implementation details of the proposed test instrument respectively. Simulation results demonstrate possibility of achieving the objective of this thesis of a sub-picosecond resolution at Gigahertz frequency.

Finally, a test environment was developed in the CIME lab to carry out experiments on the fabricated test chip. The test methodology and experimental results are discussed in chapter 6.

7.2 Perspectives and scope of future work

The proposed test instrument using a self-referenced architecture has potential for further research and enhanced performance. An existing limitation on the scaling of SUT frequency because of missing pulses at TDA output has been addressed and the details are elaborated in chapter 5. The same line of research inquiry can be carried out to scale-up the SUT frequency even further. This would also need a redesign of phase comparators which are implemented currently using a generic master slave topology D flip-flop.

Another area of continued research in this direction would be to enhance the linearity and operational range of the Time Difference Amplifier (TDA). The total bin width in the histogram also depends on the linear range of the TDA under which it can be operated.

A potential area of research would be to design delay elements with very few transistors and reduce even further their noise contribution to the measured jitter. Design elements with longer channel lengths can be experimented with for better immunity to mismatch and noise.

The power consumption of the instrument was not a design criteria as the architecture and implementation was focused on developing a test prototype that demonstrates the feasibility of on-chip measurement with high resolution. Hence this could be the next step for enhancement.

The designed chip has many external knobs for calibrating the required delay of the delay elements. The front and back gate bias of all the delay elements are externally controlled. These bias voltages could also be generated by an internal high resolution DAC to limit the required number of pads in the interface.

Finally, the digital circuitry that supports the counting of hits for the histogram and the shift register/scan chain functionality which is used for program control can be made to reside as a separate section in the chip. This allows the blocks that are associated with the signal path to be isolated from the digital circuitry that is essential for the interface and program control.

The designed instrument generates the data for histogram, but computations need to be carried out to measure the random jitter content. This computation could be carried out by a dedicated software program which takes the 1 bit wide, serial output of the instrument as an input and slices the incoming bit stream based on the word length of hit counter and calculates the root mean square of the distribution function.

8 List of Publications

8.1 International Conference Proceedings

1. M. Madhvaraj, S. Mir and M. J. Barragan, "A self-referenced on-chip jitter BIST with sub-picosecond resolution in 28 nm FD-SOI technology," 2022 IFIP/IEEE 30th International Conference on Very Large Scale Integration (VLSI-SoC), Patras, Greece, 2022, pp. 1-6, doi: 10.1109/VLSI-SoC54400.2022.9939620.

2. C. Mangelsdorf et al., "Innovative Practices Track: Innovative Analog Circuit Testing Technologies," 2022 IEEE 40th VLSI Test Symposium (VTS), San Diego, CA, USA, 2022, pp. 1-1, doi: 10.1109/VTS52500.2021.9794191.

3. A. Mamgain, M. Madhvaraj, S. Mir, M. J. Barragan and J. N. Tripathi, "A sub-picosecond resolution jitter instrument for GHz frequencies based on a sub-sampling TDA," 2023 21st IEEE Interregional NEWCAS Conference (NEWCAS), Edinburgh, United Kingdom, 2023, pp. 1-5, doi: 10.1109/NEWCAS57931.2023.10198132.

4. M. Madhvaraj, S. Mir and M. J. Barragan, "Special Session: On-chip jitter BIST with sub-picosecond resolution at GHz frequencies," 2023 IEEE 24th Latin American Test Symposium (LATS), Veracruz, Mexico, 2023, pp. 1-2, doi: 10.1109/LATS58125.2023.10154493.

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Résumé

Cette thèse propose une nouvelle implémentation de la mesure de gigue sur la puce avec une résolution sub-picoseconde en utilisant une architecture auto-référencée dans la technologie FD-SOI 28 nm de STMicroelectronics. La gigue d'horloge est la déviation des instants des fronts d'un signal périodique qui peut avoir un impact négatif sur divers paramètres en fonction de l'application. La mesure de la gigue avec une résolution inférieure à la picoseconde pour les signaux de l'ordre du gigahertz est devenue une nécessité à l'ère du transfert de données à grande vitesse. La thèse propose une combinaison de ligne de retard Vernier (VDL) et d'amplificateur de différence de temps (TDA) en plus d'éléments de retard hautement accordables pour atteindre une résolution inférieure à la picoseconde de la mesure de gigue aléatoire. Le prototype fabriqué de l'instrument occupe une surface de $340x230\mu m^2$, sans pads. Les simulations électriques démontrent la possibilité d'une résolution sub-picoseconde de la mesure de la gigue pour un signal d'horloge dans la gamme des gigahertz. Ce travail a été réalisé dans le cadre du programme Nano 2022 en collaboration avec ST Microelectronics, Crolles.

Mots-clés : gigue d'horloge, sub-picoseconde, $28\ nm$ FD-SOI

Abstract

This thesis proposes a novel implementation of on-chip jitter measurement with a sub-picosecond resolution using a self-referenced architecture in STMicroelectronics 28 nm FDSOI technology. Clock jitter is the deviation in the time instants of signal edges of a periodic signal that can have an adverse impact on various parameters depending on the application. Jitter measurement with a sub-picosecond resolution for signals in the Gigahertz range has become a necessity in this age of high-speed data transfer. This thesis addresses proposes a combination of Vernier Delay Line (VDL) and Time Difference Amplifier (TDA) in addition to highly tunable delay elements to achieve a sub-picosecond resolution of random jitter measurement. The fabricated prototype of the instrument occupies a die area of $340x230\mu m^2$ without pads. Electrical simulations demonstrate the possibility of sub-picosecond resolution of jitter measurement for clock signal in the Gigahertz range. This work has been carried out in the framework of the Nano 2022 program in collaboration with ST Microelectronics, Crolles.

Keywords : clock jitter, sub-picosecond, $28\ nm$ FD-SOI

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